LSI Databook

SIXTH EDITION

- PROM • PAL®/HAL® CIRCUITS
- SYSTEM BUILDING BLOCKS/HMSI™
- PLE™ • FIFO • MEMORY SUPPORT
- ARITHMETIC ELEMENTS AND LOGIC
- 8-BIT INTERFACE • ECL10KH
- DOUBLE-DENSITY PLUS™ INTERFACE
- CMOS • MULTIPLIERS/DIVIDERS

Monolithic Memories

LSI DATABOOK

SIXTH EDITION

Monolithic Memories

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Introduction

This book has been prepared to give the user a concise list of all LSI Products offered by Monolithic Memories. It is divided by products into sections on Military Products Division, PROMs, PLE™, PAL®/HAL® Circuits, System Building Blocks/HMSI™, FIFOs, Memory Support, Arithmetic Elements and Logic, Multipliers/Dividers, 8-Bit Interface, Double-Density PLUS™ Interface, (CMOS products included), ECL10KH and General Information which has a Listing of Available Literature. Each section has been designed to allow the user the most useable format for the products described. The PROM section gives data in the "generic" form allowing a quick review of the trade-off between devices. Inserted also are newer PROM data sheets shown with more detail. Cross references and selection guides are given where applicable. FIFO, PAL/HAL Circuits, HMSI, Arithmetic Elements, Multipliers/Dividers, 8-Bit Interface, Double-Density PLUS Interface, ECL10KH and Interface data sheets are shown in detail for each product. Advanced Information Sheets are included to inform you of soon-to-be released products. This LSI data book was formatted with you, the user, in mind. For more information, contact the local Monolithic Memories sales representative or franchised distributor. In section 17 of this book Monolithic Memories Sales Reps and Franchised Distributors are listed, for your convenience.

Products listed in the Advanced Information section were due for imminent release at the time of printing. Please contact Monolithic Memories for current availability and full parametric specifications.

PAL®
Programmable Array Logic Circuits

PAL16L8 -2 M J SHRP P01234

- PAL = Programmable Family
- HAL = Hard Array Family
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE
  - H = Active High
  - L = Active Low
  - C = Complementary
  - P = Programmable
  - R = Registered
  - RA = Registered Asynchronous
  - S = Shared
  - X = Exclusive OR Registered
  - A = Arithmetic Registered
- NUMBER OF OUTPUTS
- SPEED/POWER
  - A = High Speed
  - -2 = 1/2 Power
  - -4 = 1/4 Power
  - A-2 = High Speed and 1/2 Power
  - A-4 = High Speed and 1/4 Power
- BIT PATTERN NUMBER
- OPTIONAL PROCESSING
  - SHRP = Commercial Reliability Enhanced
  - XXXX = Hi-Rel
- PACKAGE
  - N = Plastic Dip
  - J = Ceramic Dip
  - F = Flat Pack
  - NL = Plastic Leadless Chip Carrier
  - NS = Plastic SKINNYDIP
  - JS = Ceramic SKINNYDIP
  - L = Leadless Chip Carrier
  - P = Pin Grid Array
- TEMPERATURE CODE
  - C = Commercial
  - M = Military

Standard Performance PROMs

5341 -2 J 883B

- TEMPERATURE CODE
  - 6 = Commercial
  - 5 = Military
- PRODUCT
  - 3 = Programmable Read Only Memory (PROM)
- UNIQUE TWO-DIGIT PART NUMBER
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Class B
  - XXXX = Other Hi Rel
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack - Side Brazed
  - L = Leadless Chip
  - W = Cerpack
- PERFORMANCE
  - -1 = Schottky Process (PROMs)
  - -2 = Improved Performance Over-1

High Performance PROMs

53S328 1 A J 883B

- TEMPERATURE CODE
  - 6 = Commercial
  - 5 = Military
- PRODUCT
  - 3 = Programmable Read Only Memory (PROM)
- FAMILY
  - S = Schottky
  - RA = Registered Asynchronous
  - RS = Registered Synchronous
  - D = Diagnostic
  - DA = Diagnostic Asynchronous
- MEMORY SIZE
  - 1 = 1024 bits 8 = 8192 bits
  - 2 = 2048 bits 16 = 16384 bits
  - 4 = 4096 bits 32 = 32768 bits
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Class B
  - XXXX = Other Hi Rel
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack - Side Brazed
  - L = Leadless Chip
  - W = Cerpack
- PERFORMANCE
  - None = Standard
  - A = Enhanced
- OUTPUT DESIGNATOR
  - 0 = Open Collector
  - 1 = Three State
  - 3 = Two State
- NUMBER OF OUTPUTS
  - 4 = 4 bits
  - 8 = 8 bits

PLE™
Programmable Logic Element

PLE5P8 M J 883B

- PROGRAMMABLE LOGIC ELEMENT
- NUMBER OF INPUTS
- OUTPUT TYPE
  - P = Programmable Polarity
  - R = Registered
- NUMBER OF OUTPUTS
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Class B
  - XXXX = Other Hi Rel
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack - Side Brazed
  - L = Leadless Chip
  - W = Cerpack
- TEMPERATURE CODE
  - C = Commercial
  - M = Military

8-Bit/Double-Density PLUS™ Interface

SN54LS373 J 883B

- STANDARD PREFIX
- TEMPERATURE CODE
  - 74 = Commercial
  - 54 = Military
- FAMILY
  - S = Schottky
  - LS = Low-Power Schottky
  - ACT = Advanced CMOS, TTL-Compatible
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Class B
- PACKAGE TYPE
  - J = Ceramic Dip
  - L = Leadless Chip
  - W = Cerpack
- UNIQUE THREE-DIGIT PART NUMBER

Prices

All prices are in U.S. dollars and are subject to change without notice.

Minimum Order Requirements

For all orders placed in the factory there is a minimum order requirement of $1000 ($250 per line item) except for the following:

HAL® Circuits—The $3-4K N.R.E. and mask charge can be amortized over the initial production commitment. The minimum initial production commitment is 5K units within one year; the minimum quantity per line item release is 2K.

ProPAL Circuits—When purchased the initial phase of HAL Circuit, there is no additional N.R.E. and there is a nominal adder for programming and testing. The minimum quantity per release is 500 units. When purchased without a follow-on the $1-2K N.R.E. can be amortized over a minimum initial production commitment of $2500 units.

There will be a minimum of $250 and $50 per line item for drop-ship orders.

Terms

70%/30 days, 30%/45 days from date of invoice, FOB Sunnyvale, California.

Commercial/Military Codes

The letter codes "C" and "M" are used to denote commercial and military device limits as follows:

Commercial—TA = 0°C to +75°C
VCC = 5V±5%
Military—TA = −55°C to +125°C
VCC = 5V±10%

Package Codes

All devices ordered must include a package code as a suffix to the part number. The package code definitions are shown below.

PACKAGE CODE	DESCRIPTION
J	Ceramic dual-in-line—see below
JS	Ceramic dual-in-line—see below
N	Plastic dual-in-line—see below
NS	Plastic dual-in-line—see below
NL	Molded leadless chip carrier
F	Flat Pack—Bottom Brazed
L	Leadless—Ceramic
T	Inverted "D" package
W	Ceramic Flat Pack

See "Part Numbering Systems" for complete part descriptions.

Dip Package Width Configuration

	300 mil	600 mil
20 pin	N, J	
24 pin	NS, JS	N, J

General

Unless otherwise specified the standard packages are "J" or "N" packages. In some instances the "D" package is the only package available. Other non-standard packages and other military Level 883B devices not listed may be available. Contact a sales representative of Monolithic Memories. Non-standard devices are considered nonreturnable by distribution to Monolithic Memories.

Screening Options

PROCESS LEVEL	PART MARKING
MIL-STD-883 Method 5004 and 5005 Level B	883B (Suffix)
SHRP Super High Reliability Product	SHRP

In-House PROM Programming Guide Lines

1) Minimum Order Size:
   ¼K-8K 5K pcs/yr/pattern
   500 pcs/shipment
   16K-32K 2.5K pcs/yr/pattern
   250 pcs/shipment
2) Lead Time: Initial code acceptance six weeks.
   Standard lead time plus two weeks after code acceptance.
3) Cancellations: 60 Days
4) Schedule Change: 30 Days
5) Price Adder:

	ORDER SIZE		
Density	Min-10K	10K-25K	25K+
¼K-2K	50¢	40¢	30¢
4K-8K	60¢	50¢	40¢
16K-32K REG/DIAG	85¢	70¢	55¢

Price includes ink marking with customer pattern number.

6) Inputs: Truth Table
   Paper Tape
   Disk
   Master
   A combination of two inputs are required.
   If only one input is supplied, a sample lot must be signed off by the customer.

Monolithic Memories Software Support

SYSTEM	PALASM1 OBJECT	PALASM1 SOURCE	PALASM2 OBJECT	PALASM2 SOURCE	PLEASM OBJECT	PLEASM SOURCE
	$200	$500	Contact Factory		No Charge	No Charge
DEC VAX VMS MT	PAL1-VMSE-MT	PAL1-VMSS-MT	PAL2-VMSE-MT	PAL2-VMSS-MT	PLE-VMSE-MT	PLE-VMSS-MT
DEC VAX UNIX MT	PAL1-UNXE-MT	PAL1-UNXS-MT	PAL2-UNXE-MT	PAL2-UNXS-MT	PLE-UNXE-MT	PLE-UNXS-MT
DEC PDP-11 RSX MT		PAL1-RSXS-MT			PLE-RSXE-MT	PLE-RSXS-MT
DEC PDP-11 RSX 8D		PAL1-RSXS-8D			PLE-RSXE-8D	PLE-RSXE-8D
IBM MAINFRAME MT	PAL1-IBME-MT	PAL1-IBMS-MT			PLE-IBME-MT	PLE-IBMS-MT
IBM PC (DOS) 5D	PAL1-IPCE-5D	PAL1-IPCS-5D	PAL2-IPCE-5D	PAL2-IPCS-5D	PLE-IPCE-5D	PLE-IPCS-5D
IBM PC (CPM) 5C	PAL1-IPCE-5D	PAL1-IPCS-5C			PLE-IPCE-5C	PLE-IPCS-5C
INTEL MDS SD	PAL1-MDSE-8S	PAL1-MDSS-8S			PLE-MDSE-8S	PLE-MDSS-8S
INTEL MDS DD	PAL1-MDSE-8D	PAL1-MDSS-8D			PLE-MDSE-8D	PLE-MDSS-8D
APPLE (CPM) 5D	PAL1-APLE-5C	PAL1-APLS-5C			PLE-APLE-5C	PLE-APLS-5C
IBM-3740 CPM 8D	PAL1-CPME-8C	PAL1-CPMS-8C			PLE-CPME-8C	PLE-CPME-8C
KAYPRO (CPM) 5D	PAL1-KAYE-5C	PAL1-KAYS-5C			PLE-KAYE-5C	PLE-KAYS-5C
ASCII MT	PAL1-ASCE-MT	PAL1-ASCS-MT			PLE-ASCE-MT	PLE-ASCS-MT
EBCDIC MT	PAL1-EBDE-MT	PAL1-EBDS-MT			PLE-EBDE-MT	PLE-EBDS-MT
SPECIAL FORMATS	PAL1-GENE-XX	PAL1-GENS-XX			PLE-GENE-XX	PLE-GENS-XX
MANUAL	PAL-MANUAL					

Notes: PALASM1: Supports small and medium PAL Devices (20/24 pin non-registered devices)
PALASM2: Supports MegaPAL devices and Registered devices (RA and RS) as well as standard 20/24 pin parts.
PLEASM: Supports PLE/PROM devices up to 4096x12.
APPLE and CPM versions require 64 Kb RAM.
IBM PC versions require 128 Kb RAM

Please contact IdeaLogic before placing orders for Special Formats.

Source Code orders require a signed Source License Agreement before order is shipped. Contact Idealogic.

Military Ordering Information

Products have different numbering formats. These formats in conjunction with the product selection guides by function will enable you to select the proper military level component.

PAL®
Programmable Array Logic

PAL14L4 M J 883B

- PROGRAMMABLE ARRAY LOGIC FAMILY
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE
  - H = Active High
  - L = Active Low
  - C = Complementary
  - P = Programmable
  - R = Registered
  - RA = Registered Asynchronous
  - S = Shared
  - X = Exclusive OR Registered
  - A = Arithmetic Registered
- NUMBER OF OUTPUTS
- SPEED/POWER
  - A = High Speed
  - A-2 = High Speed and 1/2 Power
  - A-4 = High Speed and 1/4 Power
- TEMPERATURE RANGE
  - M = -55°C to +125°C
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack - Side Brazed
  - L = Leadless Chip
  - W = Cerpack
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Class B

PLE™
Programmable Logic Element

PLE5P8 M J 883B

- PROGRAMMABLE LOGIC ELEMENT
- NUMBER OF INPUTS
- OUTPUT TYPE
  - P = Programmable Polarity
  - R = Registered
- NUMBER OF OUTPUTS
- TEMPERATURE CODE
  - C = Commercial
  - M = Military
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack - Side Brazed
  - L = Leadless Chip
  - W = Cerpack
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Class B
  - XXXX = Other Hi Rel

8-Bit/Double-Density PLUS™ Interface

SN54LS373 J 883B

- STANDARD PREFIX
- TEMPERATURE CODE
  - 74 = Commercial
  - 54 = Military
- FAMILY
  - S = Schottky
  - LS = Low-Power Schottky
  - ACT = Advanced CMOS, TTL-Compatible
- UNIQUE THREE-DIGIT PART NUMBER
- PACKAGE TYPE
  - J = Ceramic Dip
  - L = Leadless Chip
  - W = Cerpack
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Class B

Standard Performance PROMs

5341 -2 J 883B

- TEMPERATURE CODE
  - 6 = Commercial
  - 5 = Military
- PRODUCT
  - 3 = Programmable Read Only Memory (PROM)
- UNIQUE TWO-DIGIT PART NUMBER
- PERFORMANCE
  - -1 = Schottky Process (PROMs)
  - -2 = Improved Performance Over-1
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack - Side Brazed
  - L = Leadless Chip
  - W = Cerpack
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Class B
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High Performance PROMs

53S328 1 A J 883B

- TEMPERATURE CODE
  - 6 = Commercial
  - 5 = Military
- PRODUCT
  - 3 = Programmable Read Only Memory (PROM)
- FAMILY
  - S = Schottky
  - RA = Registered Asynchronous
  - RS = Registered Synchronous
  - D = Diagnostic
  - DA = Diagnostic Asynchronous
- MEMORY SIZE
  - 1 = 1024 bits
  - 2 = 2048 bits
  - 4 = 4096 bits
  - 8 = 8192 bits
  - 16 = 16384 bits
  - 32 = 32768 bits
- NUMBER OF OUTPUTS
  - 4 = 4 bits
  - 8 = 8 bits
- OUTPUT DESIGNATOR
  - 0 = Open Collector
  - 1 = Three State
  - 3 = Two State
- PERFORMANCE
  - None = Standard
  - A = Enhanced
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack - Side Brazed
  - L = Leadless Chip
  - W = Cerpack
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Class B
  - XXXX = Other Hi Rel

DESC Drawing Numbering System

82008 B1 J X

- DRAWING NUMBER FOR PRODUCT OR FAMILY
- PROGRAMMING PROCEDURE/ DEVICE TYPE
- CASE OUTLINE (same as JAN 38510 Outlines)
- LEAD FINISH
  - A = Hot Solder Dip
  - B = Tin Plate
  - C = Gold Plate
  - X = Any Lead Finish

JAN Part Numbering System

JM38510/ 503 01 B R A

- JAN DESIGNATOR
  - Parts cannot be marked with a "J" unless qualified and approved for listing on QPL.
- GENERAL PROCUREMENT SPEC
- REFERS TO DETAIL SPEC
  - 203 = 1K PROM (256 x 4)
  - 204 = 2K PROM (512 x 4)
  - 206 = 4K PROM (1K x 4)
  - 207 = 256 PROM (32 x 8)
  - 208 = 4K PROM (512 x 8)
  - 209 = 8K PROM (1K x 8, 2K x 4)
  - 210 = 16K PROM (2K x 8, 4K x 4)
  - 211 = 32K PROM (8K x 8)
  - 503 = Programmable Array Logic
  - 504 = Programmable Logic
- DEFINES DEVICE TYPE
- PROCESSING LEVEL
  - Class S
  - Class B
- PACKAGE TYPE
  - E = 16 Lead 1/4 x 7/8 Dip
  - F = 16 Lead 1/4 x 3/8 Flatpack
  - J = 24 Lead 1/2 x 1-1/4 Dip
  - K = 24 Lead 3/8 x 5/8 Flatpack
  - R = 20 Lead 1/4 x 1-1/16 Dip*
  - V = 18 Lead 1/4 x 15/16 Dip
  - 2 = 20 Lead 0.35 x 0.35 LCC
  - X = 24 Lead 3/8 x 3/8 Flatpack**
  - Y = 20 Lead 3/8 x 3/8 Flatpack*
  - Y = 20 Lead 5/16 x 1.0 Dip**
  - Z = 24 Lead 1/4 x 3/8 Flatpack
  - 3 = 28 Lead 0.45 x 0.45 LCC
- LEAD FINISH
  - A = Hot Solder Dip
  - B = Tin Plate
  - C = Gold Plate
  - X = Any Lead Finish

* PAL Slash Sheet
** PROM Slash Sheet

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Terms and Conditions of Sale

General Provisions

1. **ACCEPTANCE** THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BUY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold hereunder.

2. **TAXES** Unless otherwise specifically provided herein, the amount of any present or future sales, revenue, excise or other tax applicable to the products covered by this order or the manufacture of sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authorities. In the event Seller is required to pay any such tax, fee, or charge, at the time of sale or thereafter, the Buyer shall reimburse Seller therefore.

3. **RELEASE** Prices apply only if the quantity hereunder is released within twelve (12) months and shipments scheduled no more than eighteen (18) months from the date of Seller's receipt of Buyer's order; otherwise, Seller's standard prices in effect at the time of release date shall apply to the quantity shipped, and Buyer shall be invoiced for the difference in price, if any.

4. **FOB POINT** Shipments of goods within and outside the U.S. shall be delivered FOB Seller's plant, and title and liability for loss or damage thereto shall pass to Buyer upon Seller's tender of delivery of the goods to a carrier for shipment to Buyer, and any loss or damage thereafter shall not relieve Buyer of any obligation hereunder. Buyer shall reimburse Seller for taxes and any other expenses incurred or licenses or clearance required at port of entry and destination. Seller may deliver the goods in installments. Unless otherwise agreed, all items shall be packaged and packed in accordance with Seller's normal practices.

5. **DELIVERY** All shipping dates are estimates only and are dependent upon prompt receipt of all necessary information from Buyer. Shipments may be made in installments. Seller shall be excused from performance and shall not be liable for any delay in delivery or for nondelivery, in whole or in part, caused by the occurrence of any contingency beyond the reasonable control of Seller, including but not limited to, war (whether or not an actual declaration thereof is made), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof affecting the terms of this contract or otherwise, judicial action, labor dispute, accident, defaults of suppliers, fire, explosion, flood, storm or other acts of God, shortage of labor, fuel, raw material or machinery or technical or yield failures where Seller has exercised ordinary care in the prevention thereof. If any such contingency occurs, Seller may at its sole discretion allocate production and delivery among Seller's customers.

6. **PAYMENT TERMS** (a) Unless otherwise agreed, payment terms are 70% thirty (30) days; 30% forty-five (45) days after date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and condition or security satisfactory to such department.

(b) If in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefore shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

7. **INSPECTION** Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the materials. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. **LIMITED WARRANTY AND LIMITED REMEDY** The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not furnished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as-is, where-is.

9. **PATENT INDEMNIFICATION** Buyer shall hold Seller harmless from and defend Seller against any cost, expenses, damages or liabilities arising from Seller's compliance with Buyer's designs or specifications. Except as set forth above, the Seller agrees to protect and hold harmless the Buyer from any and all claims, demands, proceedings, actions, liabilities and costs resulting from any alleged infringement of patents in the United States owned by third parties by Products purchased by Buyer from Seller, provided the Buyer gives to Seller prompt notice of any such claim made against the Buyer and authorizes the Seller to settle or defend any such claim, demand, proceeding or action and assists the Seller in so doing (at the Seller's expense) upon request by the Seller. Should, as a result of any such claim, demand, proceeding or action, the Buyer be enjoined from selling or using the product, the Seller shall either (1) procure for the Buyer the right to use or sell the product; (2) modify the product so that it becomes noninfringing; (3) upon return of the product provide to the Buyer a noninfringing product meeting the same functional specifications as the product; or (4) authorize the return of the product to the Seller and upon its receipt refund to the Buyer the cost of the product plus transportation charges. The foregoing states the entire liability of the Seller for infringement of the patents of third parties and, in particular, the Seller has no obligation to indemnify the buyer for infringement of patents resulting from combinations of the product with other products whether or not supplied by the Seller. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

10. **DAMAGE LIMITATION** INDEPENDENTLY OF ANY OTHER LIMITATION HEREOF AND REGARDLESS OF WHETHER THE PURPOSE OF SUCH LIMITATION IS SERVED, IT IS AGREED THAT IN NO EVENT SHALL SELLER BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES OF ANY KIND UNDER THIS ORDER.

11. **SALE CONVEYS NO LICENSE** Seller's products are offered for sale and are sold by Seller subject in every case to the condition that such sale does not convey any license, expressly or by implication, estoppel or otherwise, under any patent claim with respect to which Seller can grant licenses covering a completed equipment, or any assembly, circuit, combination, method or process in which any such products are used as components (notwithstanding the fact that such products may have been designed for use in or may only be useful in, such patented

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General Provisions

equipment, assembly, circuit, combination, method or process and that such products may have been purchased and sold for such use). Seller expressly reserves all its rights under such patent claims.

12. RETURNS AND ADJUSTMENTS Products may only be returned with prior written approval of Seller. Adjustments for defective products are subject to Seller's concurrence that the alleged defects exist, to Seller's satisfaction, after suitable inspection and test by Seller. Adjustments may include credit or replacement at the option of the Seller.

13. TERMINATION AND CANCELLATION (a) Buyer may terminate this contract in whole or, from time to time, in part upon written notice to Seller. In such event Buyer shall be liable for termination charges which shall include a price adjustment based on the quantity of goods actually delivered, and all costs, direct and indirect, incurred and committed for this contract together with a reasonable allowance for prorated expenses and anticipated profits.

(b) Unless otherwise specified on the face hereof, all quantities must be released no more than twelve (12) months and shipments scheduled no more than eighteen (18) months from the date of Seller's receipt of Buyer's order, otherwise this contract may be cancelled by Seller and Buyer shall be liable for termination charges as provided herein.

14. NONWAIVER OF DEFAULT In the event of any default by Buyer, Seller may decline to make further shipments. If Seller elects to continue to make shipments, Seller's action shall not constitute remedies for any such default.

15. APPLICABLE LAW The validity, performance and construction of this contract shall be governed by the laws of the State of California.

16. U.S. GOVERNMENT CONTRACTS If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Federal Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be—i.e., "Contracting Officer" shall mean "Buyer," "Contractor" shall mean "Seller," and the "Contract" shall mean this order.

52.202-1. Definitions: 52.232-11, Extras; 52.212-9, Variation in Quantity; 52.232-23, Assignment of Claims; 52.228-2, Additional Bond Security; 52.225-11, Certain Communist Areas; 52.222-4, Contract Work Hours and Safety Standards Act —Overtime Compensation; 52.222-20, Walsh-Healy Public Contracts Act; 52.22-25, Equal Opportunity; Officials Not to Benefit; 52.203-5, Covenant Against Contingent Fees; 52.249-1, Termination for Convenience of the Government (Fixed Price) (Short Form) (only to the extent that Buyer's contract is terminated for the convenience of the government); 52.2-1, Contractor Inspection Requirements; 52.227-1, Authorization and Consent; 52.227-2, Notice and Assistance Regarding Patent and Copyright Information; 52.247-1, Commercial Bills of Lading Notations; 52.223-35, Affirmative Action for Special Disabled and Vietnam Era Veterans; 52.222-1, Notice to the Government of Labor Disputes; 52.215-1, Examination of Records by Comptroller General; 52.220-3, Utilization of Labor Surplus Area Concerns.

17. ASSIGNMENT This contract shall be binding upon and inure to the benefit of the parties and the successors and assigns of the entire business and good will of either Seller or Buyer, or of that part of the business of either used in the performance of this contract, but shall not be otherwise assignable.

18. MODIFICATION This contract constitutes the entire agreement between the parties relating to the sale of goods described on the face hereof, and no addition to or modification of any provision upon the face or reverse of this contract shall be binding upon Seller unless made in writing and signed by a duly authorized representative of Seller located in Santa Clara, California. Buyer hereby acknowledges that he has not entered into this agreement in reliance upon any warranty or representation by any person or entity except for the warranties or representations specifically set forth herein.

19. GENERAL The Seller represents that with respect to the production of the articles and/or the performance of the services covered by this order, it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended.

20. PROPERTY RIGHTS AND TOOLING The design, development or manufacture by Seller of a product for a specific customer shall not be deemed to produce a work made for hire and shall not give to the customer any copyright interest in the product or any interest in all or any portion of the mask works relating to the product. All such rights shall remain the property of Seller. Notwithstanding the foregoing, Seller will provide a custom product (e.g., personalized gate array, cell library or full custom) utilizing a logic design supplied by a customer exclusively to that customer absent written agreement to the contrary with the customer.

21. VARIATION IN QUANTITY If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity ordered.

Quality System

The quality system at Monolithic Memories is based on MIL-Q-9858, "Quality Program Requirements," MIL-I-45208, "Inspection System Requirements," and MIL-M-38510, Appendix A, "Product Assurance Program." Mil-M-38510 plays a significant role in structuring Monolithic Memories' Quality Program as specified herein.

Monolithic Memories has facilities certified by DESC, Defense Electronics Supply Center, to qualify and manufacture Class B Schottky Bipolar PROMS and Programmable Array Logic devices, in accordance with the requirements of MIL-M-38510. This certification included a successful audit of our quality system to the stringent requirements of Appendix A of MIL-M-38510 which defines a Product Assurance Program tailored for integrated circuit manufacturers by DESC. This same quality system has also met the strict requirements of both "controlled" and "captive" line programs connected with our special Hi-Rel programs.

The quality accent at Monolithic Memories is on process control as reflected in the use of many monitors and audits rather than gate inspection. This philosophy is consistent with building in quality and reliability rather than attempting to screen for it.

Process Control

Monolithic Memories manufacturing process uses advanced techniques to reduce random defects and produce consistent optimum quality. Typical techniques employed are:

- Redundant Masking
- Pellicalized Masks
- Direct Step on Wafer Processing

These processes although more costly, result in significant quality and reliability improvements. During the initial production stages of new designs and periodically thereafter, engineering characterizes the design process compatibility by careful sample selection of lots reflecting process variable extremes.

Product Reliability Programs

Monolithic Memories has an ongoing reliability program for military and commercial products, each utilizing the appropriate test methods of MIL-STD-883. This program provides for a consistent database in the following areas:

- Product/Process Reliability Data
- Qualification of Raw Materials
- Customer Quality Conformance
- Reliability verification of state of the art design and production techniques.

Quality Monitors

MMI constantly monitors product quality and reliability through the following ongoing programs:

- Reliability assessments of all products, processes and packages.
- Inprocess and Final product quality measurements.
- Process and product quality feedback at all key manufacturing points.
- Positive corrective action and verification.

Screening

Much of the assembly and processing is performed offshore at facilities owned by or qualified by MMI. These facilities are routinely monitored by Monolithic Memories personnel to our quality system requirements.

Standard Commercial product receives the following screens and monitors to insure the highest possible quality.

• Precap Inspection	MIL-Standard 883 Level B
• Temperature Cycle • Constant Acceleration • Fine and Gross Leak • Final Electrical Test • Visual and Mechanical Inspection	Ongoing daily monitor to confirm the AQL levels are met or exceeded.

The standard product AQL levels which Monolithic Memories guarantees are listed in the table on this page.

Quality Assurance (AQL) Levels

TEST	AQL TEMPERANCE
Hermeticity (includes fine and gross)	.1
Electrical	
DC at 25°C	.065
Functional at 25°C	.065
AC at 25°C	.25
DC at Temperature Extremes	.25
Functional at Temperature Extremes	.25
AC at Temperature Extremes	.25

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MILITARY PRODUCTS DIVISION

Introduction

In August, 1982 Monolithic Memories Inc. formed a Military Products Division. Although Monolithic Memories has participated in the defense market for some time, we feel that by focusing on this very demanding customer base with a totally dedicated resource, we can provide aerospace and military systems manufacturers with a new industry standard of service and responsiveness.

Monolithic Memories offers devices to a full complement of military screening levels:

Monolithic Memories Inc. Level S
JAN 38510 Class B
DESC Drawing Program
Mil-Std-883 Class B
Monolithic Memories Inc Mil-Temp Product

In addition, we welcome the opportunity to review and quote to customer source control drawings. Our spec Review group is measured to a 2 week turn-around time on drawing reviews, so our customers will receive a timely response on our ability to meet custom requirements.

Monolithic Memories is Certified by the Defense Electronics Supply Center to assemble and test JAN 38510 Class B devices 38510 Class B devices at its Sunnyvale, California.

Offshore Assembly facilities for Mil-Std-883 Class B devices are located in Penang, Malaysia.

Standard Processing Flows

Monolithic Memories Processing and Screening flows are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows.

Standard processing flows which the Military Products Division currently operates to include:

Monolithic Memories Inc. Modified Level S
JAN 38510 Class B
DESC Drawing Program
Mil-Std-883 Class B
Monolithic Memories Inc. Mil-Temp Product

In addition, these flows are expanded to provide for factory programming on PAL circuits and PROMS, when required by our customers.

Major benefits can be realized by ordering product to standard flows whenever possible:

- Minimize need for source control drawings.
- Cost savings on unit cost — no price adders for custom processing.
- Improved lead time — no spec review or negotiation time, plus the ability to pull product from various work-in-process stages or purchase product from finished goods inventory.

For your reference, we have included our Modified Level S flow, our Mil-Std-883 Class B flow and our Mil-Temp Product flow. For your planning purposes, we have included typical throughput times for each operation, as product proceeds through the processing flow.

It is the policy of Monolithic Memories, to always operate to the most current revision of Mil-Std-883.

JAN Program

Monolithic Memories is certified by the Defense Electronics Supply Center to fabricate wafers in our 4-inch fab lines and to assemble and test MIL-M-38510 Class B PROMs and PAL circuits in our Sunnyvale facilities. Monolithic Memories has, in addition, been awarded full laboratory suitability to conduct all qualification and quality conformance testing in accordance with MIL-STD-883, Method 5005.

Monolithic Memories has listed in the Qualified Parts List Part I*, a 5301-ID (M38510/20302BEA) and a PAL16R4AJ (M38510/50404BRA), and in Part II a PAL10H8J (M38510/50301BRA) PAL14H4J (M38510/50303BRA), PAL10L8J (M38510/50306BRA), PAL16R8AJ (M38510/50401BRA), PAL16L8AJ (M38510/50402BRA), PAL16R6AJ (M38510/50403BRA) and a 53S841J (M38510/20908BVA).

Near Future QPL I plans include the:

PAL10H8J	PAL16R8AJ	
PAL14H4J	53S441J	(1K×4 PROM)
PAL10L8J	53S841J	(2K×4 PROM)
PAL16R6AJ	53S1681J	(2K×8 PROM)
PAL16L8AJ	53S3281J	(4K×8 PROM)

* Listings are based on QPL-38510-61, dated 1 October 1984.

Selected devices will be further qualified in leadless chip carriers.

Long term QPL I plans include FIFO's, Low-Power PAL circuits, New PAL Families as they are introduced, and Registered PROMs.

Our goal in the Military Products Division is to support the JAN38510 Program with a continual flow of new high-performance, Advanced Technology Products.

Monolithic Memories Products for which slash sheet specifications currently exist are listed in the "M38510 Slash Sheet Cross Reference to Generic Part Number."

M38510
Slash Sheet Cross Reference to Generic Part Number

M38510	01	02	03	04	05	06	07	08	09	10
203	5300-1	5301-1								
204	53S240	53S241								
206	53S440	53S441								
207	53S080	53S081								
208	5340-2	5341-2		5348-2	5349-2					
209	53S840	53S841	5380-2	5381-2						
210		53S1681			(Will be adding 53S1641)					
211		53S3281								
503	10H8	12H6	14H4	16H2	16C1	10L8	12L6	14L4	16L2	
504	16L8A	16R8A	16R6A	16R4A	16X4	16A4	16L8A-2	16R8A-2	16R6A-2	16R4A-2
505	20L8A	20R8A	20R6A	20R4A						

DESC Drawing Program

Monolithic Memories is an active participant in the DESC Drawing Program. For contracts invoking MIL-STD-454 we offer our full PAL product line to DESC Drawings 81035 and 81036. Monolithic Memories is also approved to supply the 32K PROM to DESC Drawing 82008. The idea behind the DESC Drawing Program is to standardize MIL-STD-883B microcircuits where fully qualified JAN product is not available. The advantage to the user is that DESC Drawings are a cost effective alternative to source control drawings and are offered as off-the-shelf stocking items by IC manufacturers participating in the program.

Since semiconductor demand is on the rise, and lead times will be a major concern, DESC Drawings should always be considered to improve availability over source control drawings. It is standard practice at Monolithic Memories to convert our 883B processing to DESC Drawings for all products which we are approved to supply. Monolithic Memories Inc. then dual marks devices with both the DESC Drawing Number and the Generic Part Number. DESC approved products can then be procured to either part number as standard product through both OEM and distributor channels.

The following cross reference will allow you to determine the appropriate DESC Drawing part numbers for each PAL product and the 32K PROM. Future DESC print activity will inclde new PAL products and registered PROMs. Monolithic Memories will work with DESC to continually generate new drawings, which will provide a steady flow of advanced technology products to standardized specifications.

DESC Drawing/Generic Part Type Cross Reference

DESC DRAWING PART NO.: 81035	01	Y	X
DRAWING NO.	DEVICE TYPE	CASE OUTLINE	LEAD FINISH

Small PAL 20 Devices:

DESC Drawing	Generic Part Number	Replacement JAN Specification Part Number
8103501RX	PAL10H8MJ883B	M38510/50301BRX
81035012X	PAL10H8ML883B	M38510/50301B2X
8103501YX	PAL10H8MF883B	M38510/50301BYX
8103502RX	PAL12H6MJ883B	M38510/50302BRX
81035022X	PAL12H6ML883B	M38510/50302B2X
8103502YX	PAL12H6MF883B	M38510/50302BYX
8103503RX	PAL14H4MJ883B	M38510/50303BRX
81035032X	PAL14H4ML883B	M38510/50303B2X
8103503YX	PAL14H4MF883B	M38510/50303BYX
8103504RX	PAL16H2MJ883B	M38510/50304BRX
81035042X	PAL16H2ML883B	M38510/50304B2X
8103504YX	PAL16H2MF883B	M38510/50304BYX
8103505RX	PAL16C1MJ883B	M38510/50305BRX
81035052X	PAL16C1ML883B	M38510/50305B2X
8103505YX	PAL16C1MF883B	M38510/50305BYX
8103506RX	PAL10L8MJ883B	M38510/50306BRX
81035062X	PAL10L8ML883B	M38510/50306B2X
8103506YX	PAL10L8MF883B	M38510/50306BYX
8103507RX	PAL12L6MJ883B	M38510/50307BRX
81035072X	PAL12L6ML883B	M38510/50307B2X
8103507YX	PAL12L6MF883B	M38510/50307BYX
8103508RX	PAL14L4MJ883B	M38510/50308BRX
81035082X	PAL14L4ML883B	M38510/50308B2X
8103508YX	PAL14L4MF883B	M38510/50308BYX
8103509RX	PAL16L2MJ883B	M38510/50309BRX
81035092X	PAL16L2ML883B	M38510/50309B2X
8103509YX	PAL16L2MF883B	M38510/50309BYX

New DESC Drawing Number Insert
Medium PAL20 Devices

DESC DRAWING	GENERIC PART NUMBER	REPLACEMENT JAN SPECIFICATION PART NUMBER
8103601RX	PAL16L8MJ883B	M38510/50401BRX*†
81036012X	PAL16L8ML883B	M38510/50401B2X*
8103601YX	PAL16L8MF883B	M38510/50401BYX*
8103602RX	PAL16R8MJ883B	M38510/50401B2X*†
81036022X	PAL16R8ML883B	M38510/50402B2X*
8103602YX	PAL16R8MF883B	M38510/50402BYX*
8103603RX	PAL16R6MJ883B	M38510/50403BRX*
81036032X	PAL16R6ML883B	M38510/50403B2X*
8103603YX	PAL16R6MF883B	M38510/50403BYX*
8103604RX	PAL16R4MJ883B	M38510/50404BRX*†
81036042X	PAL16R4ML883B	M38510/50404B2X*
8103604YX	PAL16R4MF883B	M38510/50404BYX*
8103605RX	PAL16x4MJ883B	M38510/50405BRX
81036052X	PAL16x4ML883B	M38510/50405B2X
8103605YX	PAL16x4MF883B	M38510/50405BYX
8103606RX	PAL16A4MJ883B	M38510/50406BRX
81036062X	PAL16A4ML883B	M38510/50406B2X
8103606YX	PAL16A4MF883B	M38510/50406BYX
8103607RX	PAL16L8AMJ883B	M38510/50401BRX†
81036072X	PAL16L8AML883B	M38510/50401B2X
8103607YX	PAL16L8AMF883B**	M38510/50401BYX
8103608RX	PAL16R8AMJ883B	M38510/50402BRX†
81036082X	PAL16R8AML883B	M38510/50402B2X
8103608YX	PAL16R8AMF883B**	M38510/50402BYX
8103609RX	PAL16R6AMJ883B	M38510/50403BRX†
81036092X	PAL16R6AML883B	M38510/50403B2X
8103609YX	PAL16R6AMF883B**	M38510/50403BYX
8103610RX	PAL16R4AMJ883B	M38510/50404BRX†
81036102X	PAL16R4AML883B	M38510/50404B2X
8103610YX	PAL16R4AMF883B**	M38510/50404BYX
8103611RX	PAL16L8A-2MJ883B	M38510/50407BRX
81036112X	PAL16L8A-2ML883B	M38510/50407B2X
8103611YX	PAL16L8A-2MF883B**	M38510/50407BYX
8103612RX	PAL16R8A-2MJ883B	M38510/50408BRX
81036122X	PAL16R8A-2ML883B	M38510/50408B2X
8103612YX	PAL16R8A-2MF883B**	M38510/50408BYX
8103613RX	PAL16R6A-2MJ883B	M38510/50409BRX
81036132X	PAL16R6A-2ML883B	M38510/50409B2X
8103613YX	PAL16R6A-2MF883B**	M38510/50409BYX
8103614RX	PAL16R4A-2MJ883B	M38510/50410BRX
81036142X	PAL16R4A-2ML883B	M38510/50410B2X
8103614YX	PAL16R4A-2MF883B**	M38510/50410BYX
8412901JX	PAL20L8AMJ883B	M38510/50501BJX
84129013X	PAL20L8AML883B	M38510/50501B3X
8412902JX	PAL20R8AMJ883B	M38510/50502BJX
84129023X	PAL20R8AML883B	M38510/50502B3X
8412903JX	PAL20R6AMJ883B	M38510/50503BJX
84129033X	PAL20R6AML883B	M38510/50503B3X
8412904JX	PAL20R4AMJ883B	M38510/50504BJX
88412904JX	PAL20R4AMJ883B	M38510/50504BJX
84129043X	PAL20R4AML883B	M38510/50504B3X
PROM:		
82008B1JX	53S3281MJ883B	M38510/21102BJX
82008B2ZX	53S3281ML883B	M38510/21102B2X

* For New Medium 20-pin PAL Designs, only the "A" versions of these products are recommended. (See DESC Nos 8103607 through 8103610). Only the "A" versions of the medium PAL family are planned for JAN qualification by Monolithic Memories Inc., and will be more readily available for customer production needs over time.

** The Military Products Division will be converting from the bottom-brazed flatpack to a "W" package cerpack during 1985.

† Inactive for *new* design for the R Case outline only. Use applicable QPL M38510 device.

Quality Programs

The Military Product Division quality system conforms to the following Mil-Standards:

Mil-M-38510, Appendix A, "Product Assurance Program"
Mil-Q-9858, "Quality Program Requirements"
Mil-I-45208, "Inspection System Requirements"

Monolithic Memories facilities in Sunnyvale are certified by the Defense Electronics Supply Center (DESC), to manufacture and qualify Schottky Bipolar PROMs and PAL circuits in accordance with Mil-M-38510 Class B. This certification was a result of a successful audit of our production and quality systems to the stringent requirements of Mil-M-38510. Monolithic Memories has also demonstrated compliance with the strict requirements of both controlled and captive lines connected with special Military programs.

Quality Assurance

Following 100% screening, the Military Products Division samples all products processed in conformance with MIL-STD-883 Class B to the following LTPD levels:

Test	LTPD
DC 25°C	2
DC +125°C	3
DC -55°C	5
Functional at 25°C	2
Functional at Temperature Extremes	5
AC 25°C	2
AC +125°C	3
AC -55°C	5

The Military Products Division ensures outgoing product quality and integrity by performing inspection Lot Group A's and B's per Mil-Std-883 Method 5005, conducting self audits in all areas involved in screening tests per Method 5004 of Mil-Std-883, gating all shipments to our customers, and maintaining a calibration control system in accordance with Mil-Std-45662.

For products requiring programming prior to AC tests, testing is performed utilizing MIL-M-38510 Slash Sheet sample plans.

Product Qualification/ Quality Conformance Inspection (QCI)

The Military Products Division has a quality conformance testing program in accordance with Mil-Std-883, Method 5005. Quality Conformance Testing provides necessary feedback and monitors several areas:

- Reliability of Product/Processes
- Vendor Qualification for Raw Materials
- Customer Quality Requirements
- Maintain Product Qualification
- Engineering Monitor on Products/Processes

Standard procedures for new product release specify that Monolithic Memories' Reliability Department, as a minimum, conduct full qualification testing per Method 5005 of Mil-Std-883. Once qualified, each package type (from each assembly line) and device (by technology group as delineated in Mil-M-38510) are incorporated into Monolithic Memories Quality Conformance Inspection program which utilizes the requirements of Mil-M-38510.

When Military Programs do not require that QCI data be run on the specific lot shipped, Monolithic Memories Quality Conformance program allows customers to obtain generic data on all product families manufactured by the Military Products Division. Generic Qualification Data enables customers to eliminate costly qualification and desctruct unit charges, and also improves delivery time by a factor of eight to ten weeks. The following generic data is available:

Group B—Package related tests

- QCI is performed every 6 weeks of manufacture on each package type.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor assembly integrity.

Group C—Product/Process related tests

- QCI is performed every 13 weeks of manufacture, on representative devices from the same microcircuit group.
- Life test data may be used to qualify similar technologies.
- Purpose: To monitor the reliability of the process and parametric performance for each product technology.
- Monolithic Memories Group C Generic Families:
  1. Programmable Product
     —PROMS-Schottky Nichrome
     —PROMS-Titanium Tungsten
     —PAL Circuits
  2. Logic, Multipler, Fifo
  3. Octal Interface

Group D — In-depth package related tests

- QCI is conducted every 26 weeks using devices which represent the same package construction and lead finish.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor the reliability and integrity of various package materials and assembly processes.

Generic Data:

Monolithic Memories Generic Data Program is based on MIL-M-38510, which allows for shipments based on 26 weeks of coverage for Group C Testing and 36 weeks of coverage for Group D Testing

Should circumstances arise where generic coverage to MIL-M-38510 is not possible, Monolithic Memories reserves the right to ship product based on 52 weeks of generic Group C and/or D coverage per MIL-M-883 Revision C, Paragraph 1.2.1b (17) dated 15 August 1984.

Manufacturing and Screening Locations

JAN Products, Monolithic Memories Modified Level "S," and customer orders which call for U.S.A. assembly, are manufactured in our DESC certified assembly line in Sunnyvale, California.

Mil-Std-883 Class B products, and orders to source control drawings, where stateside build is not required, are assembled at our Penang, Malaysia facility. This facility is qualified by Monolithic Memories Quality Department, as well as by many of our customers, to manufacture Mil-Std-883 Class B product. Conformance to Mil-Std-883 requirements is routinely monitored through audits at the Penang facility, as well as incoming inspections in Sunnyvale prior to completion of Burn-In and Final Test. Manufacturing capabilities for each Monolithic Memories facility are highlighted on the chart below.

Manufacturing Capabilities

	Sunnyvale	Penang
Assembly	X	X
Precap Inspection	X	X
Environmental Testing	X	X
Electrical Pre-Test	X	X
Burn-In	X	X
Post Burn-In Electricals	X	X
Group A Testing	X	
Mark	X	X
Factory Programming (when applicable)	X	
Qualification and Quality Conformance Testing	X	

To identify the assembly location of each military device, the Country of origin is marked on all products prior to shipment. Products assembled in our stateside facility in Sunnyvale, California, will have "USA" marked on the topside of the device. The exception to this is JAN 38510 product, which is marked to the Mil-M-38510 requirements only.

Offshore built product, which is manufactured in Penang, Malaysia, will have "Malaysia" marked on the bottomside of the device.

Marking Example:

53S3281J883B
USA Δ 8335

ESD Designator

AC Testing

Although Monolithic Memories offers a large selection of programmable products, it must be pointed out that AC Testing cannot be performed on many of our product types without their being programmed. For those devices which must be programmed prior to AC Tests and are ordered unprogrammed, Monolithic Memories must "guarantee" their AC Performance.

Newer devices in the PROM and PAL families do allow preprogram AC testability.

Since the **guaranteeing** of parameters can be a serious concern for the Military user, we have outlined several approaches to address the AC screening issue.

1. Monolithic Memories can pull a **Sample** from a lot using our own **Standard patterns** (designed to blow in excess of 50 percent of the fuses) and perform AC testing at 25° C, and temperature extremes.
   a) PAL products processed to DESC prints include programmability samples and AC testing at room temperature as a standard.
   b) AC at high- and low-temperature extremes is a cost adder to standard processing.
2. Monolithic Memories can program parts using custom programs submitted by the customer. AC can then be done with the following options:
   a) Sample AC at 25°C
   b) Sample AC at 25° C, -55° C, 125° C
   c) 100% AC at 25° C
   d) 100% AC at 25° C, -55° C and 125° C (not available on PAL products)

Options b through d are cost adders to basic processing.

On PAL products where custom programming is performed and AC testing is required, additional vector generation and fault coverage analysis is required, as well as AC program checkout. Non-recurring engineering charges are applicable to this type of requirement.

To give you an idea of delivery differences for the options discussed above, general lead times are as follows:

- Unprogrammed:
  Cerdip, 4–6 weeks
  Flat pack, 8–12 weeks
  Leadless, 6–12 weeks
  (consult monthly leadtime guide for individual part types).
- Unprogrammed product using our standard pattern to verify AC at room temperature on sample basis (option 1). Add 2 weeks to standard delivery.
- Programmed product using customer programs with sample AC (option 2a and b). Contact factory for delivery. Delivery quoted will be after receipt of customer design package.
- 100% AC testing at 25°C—Standard Monolithic Memories pattern or customer pattern, (option c). Contact factory.

Remember, for ProPALs, customer must provide design package including Boolean Equations, "Seed" function test sequence, package stipulation and AC test vectors, when required. Delivery quotes for this type of product begin **after** receipt of this data from the customer.

VIL/VIH Parametric Information

VIL and VIH as specified are input conditions at which the device is designed to meet all D.C. and functional performance characteristics.

Typical test conditions used for VIL and VIH are 0.0 and 3.0 volts. When utilizing these as input conditions for testing purposes, consideration must be given to test equipment noise levels and equipment limitations. VIL and VIH limits are absolute values with respect to the ground pin(s) on the device and includes all overshoots due to test equipment noise.

ElectroStatic Discharge

The Military Products Division of Monolithic Memories has fully implemented static control procedures throughout its facilities in Penang, Malaysia and Sunnyvale, California.

All manufacturing areas where product is processed or handled, including our Reliability Labs, Engineering Labs, etc., have full static control such as wrist straps, antistatic smocks, grounded stainless steel tables, conductive mats and ion generators wherever necessary.

All product is moved throughout our facilities and shipped to customers in static shielded containers.

An ESD identifier is marked on all products in front of the date code, and all shipping containers are labeled with an ESD Caution Message. These procedures have been implemented, and will continually be reviewed, to ensure that our customers receive only the highest quality product form the Military Products Division.

Major Program Participation

Monolithic Memories is a supplier of Military components to most major Department of Defense Programs. A partial listing of program participation is provided.

AMRAAM	F-15	LAMPS	SUBACS
ASPJ	F-16	LATIRN	TRIDENT
AWACS	F-18	MILSTAR	UYK-43
B-1	HARM	PATRIOT	UYK-44
B-52	HARPOON	PERSHING	VLS
BATSON	HAWK	PHALANX	
CRUISE	HELLFIRE	SIDEWINDER	
DIVADS	IUS	SPARROW	

2

Military PROM Performance Analysis

(Max. Military Limits—Three State Only)

Size	MMI		AMD		Raytheon		Harris		National		Signetics		TI	
	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}
¼K	5331-1	60/125	27S19	50/115	—	—	7603-2	60/130	—	—	82S123	65/85	18S030	50/110
32 × 8	53S081	35/125	27S19A	35/115	—	—	—	—	54S288	45/110	82S123A	35/110	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1K 256 × 4	5301-1	75/130	—	—	—	—	7611-2	75/130	54S287	60/130	82S129	70/125	24S10	75/100
	53S141	55/130	27S21	60/130	—	—	7611A-2	65/130	—	—	82S129A	35/125	—	—
2K 256 × 8	5309-1	80/155	—	—	—	—	—	—	54LS471	70/100	—	—	28L22	75/100
2K 518 × 4	5306-1	75/130	27S13	60/130	29611A	60/130	7621-2	85/130	54S571	65/130	82S131	70/140	—	—
	53S241	55/130	27S13A	40/130	—	—	7621A-2	70/130	54S571A	60/130	82S131A	35/140	—	—
4K 512 × 8	5341-1	80/155	—	—	—	—	7641-2	85/170	54S474	75/170	82S141	90/185	28S46	70/135
	5341-2	70/155	27S31	70/175	—	—	7641A-2	70/170	—	—	—	—	—	—
	5349-1	80/155	—	—	29621	80/155	7649-2	80/170	54S472	75/170	82S147	75/165	28S42	70/135
	5349-2	70/155	27S29	70/160	29621A	60/155	—	—	54S472A	60/155	82S147A	60/165	—	—
	53RA481	*25/180	27S25	30/185	—	—	—	—	77SR474	—	—	—	—	—
	53RA481A	*20/180	27S25A	25/185	—	—	—	—	—	—	—	—	—	—
4K 1K × 4	53S441	55/140	—	—	—	—	—	—	54S573A	60/140	82S137A	70/150	—	—
	53S441A	50/140	27S33A	45/145	—	—	—	—	—	—	—	—	—	—
	53DA441	*25/180	27S65	30/190	—	—	—	—	—	—	—	—	—	—
	53DA442	*25/180	27S65	30/190	—	—	—	—	—	—	—	—	—	—
8K 1K × 8	5381-1	125/175	—	—	29631	90/170	7681-2	90/170	—	—	82S181	90/185	28S86	65/170
	5381-2	70/175	27S181	80/185	29631A	60/170	—	—	77S181	75/170	82S181A	80/185	28S86A	50/170
8K Reg 1K × 8	53RS881	*25/180	27S37	30/185	—	—	—	—	—	—	—	—	—	—
	53RS881A	*20/180	27S37A	25/185	—	—	—	—	—	—	—	—	—	—
8K 2K × 4	53S841	55/150	27S185	55/150	29651A	70/170	7685-2	90/170	77S185	75/140	82S185A	80/160	24S81	85/175
	53S841A	50/150	27S185A	45/150	—	—	—	—	—	—	—	—	—	—
16K 2K × 8	53S1681	60/185	27S191	65/185	29681A	70/180	76161-2	80/180	77S191	80/175	82S191A	70/185	—	—
	53S1681A	45/185	27S191A	50/185	—	—	—	—	—	—	—	—	—	—
16K Reg. 2K × 8	53RA1681	*25/185	27S45/47	30/185	—	—	—	—	—	—	—	—	—	—
	53RA1681A	*20/185	27S45/47A	25/185	—	—	—	—	—	—	—	—	—	—
	53RS1681	*25/185	27S45/47	30/185	—	—	—	—	—	—	—	—	—	—
	53RS1681A	*20/185	27S45/47A	25/185	—	—	—	—	—	—	—	—	—	—
16K 4K × 4	53S1641	65/175	27S41	65/170	—	—	76165-2	80/170	—	—	—	—	—	—
	53S1641A	50/175	27S41A	50/170	—	—	—	—	—	—	—	—	—	—
16K Diag. 4K × 4	53D1641	*25/190	27S85	30/190	—	—	—	—	—	—	—	—	—	—
	53DA1643	*25/190	27S85	30/190	—	—	—	—	—	—	—	—	—	—
32K 4K × 8	53S3281	60/190	27S43	65/185	29671A	80/195	76321-2	75/190	77S321	65/190	82S321	80/185	—	—
	53S321A	50/190	27S43A	55/185	—	—	—	—	—	—	—	—	—	—

* TCLK.

Package Information
Leadless Chip Carrier/Pin Grid Array

Monolithic Memories' Military Products Division offers, with few exceptions, our entire product line in square, ceramic/gold leadless chip carriers. In addition, we also offer the MEGAPAL 64R32 and the 54S556 in a square, ceramic/gold 88-pin-grid-array package.

INTERFACE CIRCUITS
- 20 square LCC

PROM CIRCUITS (Programmable Read Only Memories)
- 20 square LCC
- 28 square LCC

PLE CIRCUITS (Programmable Logic Elements)
- 20 square LCC
- 28 square LCC

PAL/*HAL CIRCUITS (Programmable Array Logic)
- 20 square LCC
- 28 square LCC
- 44 square LCC
- 84 square LCC

HMSI CIRCUITS (High-Complexity Medium Scale Integration)
- 28 square LCC

FIFO CIRCUITS (First-In-First-Out Memories)
- 20 square LCC
- 28 square LCC

8 BIT/DOUBLE-DENSITY INTERFACE CIRCUITS
- 20 square LCC
- 28 square LCC

ARITHMETIC ELEMENT/LOGIC CIRCUITS
- 20 square LCC

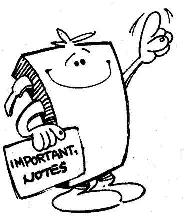
MULTIPLIER CIRCUITS
- 44 square LCC
- 84 square LCC (cavity down)**

DRAM CONTROLLERS/DRIVER CIRCUITS
- 52 square LCC

PAL/*HAL CIRCUIT (Programmable Array Logic)
- 88 square PGA

MULTIPLIER CIRCUIT
- 88 square PGA

* HALs are the mask-programmable versions of PALs.


IMPORTANT,
NOTES

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PROMs

PROM SELECTION GUIDE

PROMS

Device Number	Pins	Size	Output	T_{AA} (ns) Com'l/Mil	I_{CC} (mA) Com'l/Mil
53/63S080	16 (20)	¼K 32×8	OC	25/35	125
53/63S081			TS	25/35	
63S081A			TS	/25	
53/63S140	16 (20)	1K 256×4	OC	45/55	130
53/63S141			TS	45/55	
53/63S141A			TS	30/40	
53/63S240	16 (20)	2K 512×4	OC	45/55	130
53/63S241			TS	45/55	
53/63S241A			TS	35/45	
53/6308-1	20	2K 256×8	OC	70/80	155
53/6309-1			TS		
53/63S280	20 (20)		OC	45/50	140
53/63S281			TS	45/50	
53/63S281A			TS	28/40	
53/63S440	18 (20)	4K 1K×4	OC	45/55	140
53/63S441			TS	45/55	
53/63S441A			TS	35/50	
53/6340-1	24 (28)	4K 512×8	OC	70/80	155
53/6341-1			TS	70/80	
53/6341-2			TS	55/70	155/175
53/6348-1	20		OC	70/80	155
53/6349-1			TS	70/80	
53/6349-2			TS	55/70	155/175
53/63S480	20 (20)		OC	45/50	155
53/63S481			TS	45/50	
53/63S481A			TS	30/40	
53/63S841	18 (28)	8K 2K×4	TS	50/55	150
53/63S841A				35/50	
53/6380-1	24	8K 1K×8	OC	90/125	175
53/6381-1			TS		
53/6380-2			OC	70/90	170/175
53/6381-2			TS	55/70	
63S880*	24 (28)		OC	50/60	
63S881*			TS	50/60	
63S881A*			TS	30/40	
53/63S1641	20	16K 4K×4	TS	50/65	175
53/63S1641A				35/50	
53/63S1681	24 (28)	16K 2K×8	TS	50/65	185
53/63S1681A				35/50	
53/63S3281	24 (28)	32K 4K×8	TS	50/60	190
53/63S3281A				40/50	

*Preliminary information

( ) = Chip Carrier Package

REGISTERED PROMS

Device Number	Pins	Size	Output	T_{CLK} (ns) Com'l/Mil	I_{CC} (mA) Com'l/Mil
53/63RA481	24 (28)	4K 512×8	TS	20/25	180
53/63RA481A				15/20	
53/63RS881	24 (28)	8K 1K×8	TS	20/25	180
53/63RS881A				15/20	
53/63RA1681	24 (28)	16K 2K×8	TS	20/25	185
53/63RA1681A				15/20	
53/63RS1681			TS	20/25	185
53/63RS1681A				15/20	

DIAGNOSTIC-REGISTERED PROMS

Device Number	Pins	Size	Output	T_{CLK} (ns) Com'l/Mil	I_{CC} (mA) Com'l/Mil
53/63DA441	24 (28)	4K 1K×4	TS	18/25	180
53/63DA442				18/25	
53/63DA841	24 (28)	8K 2K×4	TS	20/25	185
53/63D1641	24 (28)	16K 4K×4	TS	20/25	190
53/63DA1643			2S	20/25	

PROM Part Number Cross-Reference

Memory Description: Organization	Pins	Output	MMI	AMD	Fairchild	Fujitsu	Harris	Motorola	National	Raytheon	Signetics	TI
¼K	16	OC	63S080	27S18	—	—	7602	—	74S188	—	82S23	18SA030
32 × 8		TS	63S081/A	27S19	—	—	7603	—	74S288	—	82S123	18S030
1K	16	OC	63S140	27S20	—	—	7610	—	74S387	—	82S126	24SA10
256 × 4		TS	63S141/A	27S21	—	—	7611	—	74S287	—	82S129	24S10
2K	20	OC	6308-1	—	—	—	—	—	—	—	—	18SA22
256 × 8		TS	6309-1	—	—	—	—	—	74LS471	—	82S135	18S22
		TS	63S281/A	—	—	—	—	—	74LS471	—	82S135	18S22
2K	16	OC	63S240	27S12	—	—	7620	7620	74S570	—	82S130	—
512 × 4		TS	63S241/A	27S13	—	—	7621	7621	74S571	29611	82S131	—
4K	20	OC	6348-1	27S28	—	7123	—	—	74S473	—	—	—
512 × 8		TS	6349-1, -2	27S29	—	7124	7649	—	74S472	29621	82S147	28S42
		TS	63S481/A	27S291	—	7124	7649	—	74S472	29621	82S147	28S42
	24	OC	6340-1	27S30	—	—	7640	7640	74S475	—	—	28SA46
		TS	6341-1, -2	27S31	—	—	7641	7641	74S474	—	82S141	28S46
4K Reg 512 × 8	24	TS	63RA481 63RA481A	27S25	—	—	—	—	87SR474	—	—	—
4K	18	OC	63S440	27S32	—	—	7642	7642	74S572	—	—	24SA41
1024 × 4		TS	63S441/A	27S33	93453	—	7643	7643	74S573	—	82S137	24S41
4K Diag. 1024 × 4	24	TS	63DA441 63DA442	27S65	—	—	—	—	—	—	—	—
8K 2048 × 4	18	TS	63S841 63S841A	27S185	—	7128	7685	7685	87S185	29651	82S185	24S81
8K Diag. 2048 × 4	24	TS	63DA841	27S75	—	—	—	—	—	—	—	—
8K	24	OC	6380-1, -2	27S180	93Z450	7131	—	7680	87S180	—	82S180	28SA86
1024 × 8		TS	6381-1, -2	27S181	93Z451	7132	7681	7681	87S181	29631	82S181	28S86
1024 × 8	24	TS	6381-1 JS	27S281	—	7132E-SK	—	—	87S281	29631S	82S181N3	—
SKINNYDIP			6381-2 JS	27S281	—	7132E-SK	6-7681	—	87S281	29631S	82S181N3	—
8K Reg	24	TS	63RS881	27S35/37	—	—	—	—	87SR181	—	—	—
1024 × 8			63RS881A		—	—	—	—	—	—	—	—
16K 2048 × 8	24	TS	63S1681 63S1681A	27S191	93Z511	7138	76161	76161	87S191	29681	82S191	28S166
2048 × 8	24	TS	63S1681 NS	27S291	—	7138E-SK	6-76161	—	87S291	29681S	—	—
SKINNYDIP			63S1681ANS	27S291A	—	7138Y-SK	—	—	—	29681AS	82S191BN3	—
16K Reg	24	TS	63RA1681/A	27S45/47	—	—	—	—	—	—	—	—
2048 × 8			63RS1681/A		—	—	—	—	—	—	—	—
16K 4096 × 4	20	TS	63S1641 63S1641A	27S41	—	7152	76165	—	—	—	—	—
16K Diag.	24	TS	63D1641	27S85	—	—	—	—	—	—	—	—
4096 × 4		2S	63DA1643		—	—	—	—	—	—	—	—
32K 4096 × 8	24	TS	63S3281 63S3281A	27S43	—	7142	76321	—	87S321	29671	82S321	—

NOTE: Only Commercial Specification part numbers are listed.

PROM Part Number Cross-Reference

High Performance 32x8 PROM TiW PROM Family

53/63S080 53/63S081 63S081A

Features/Benefits

- **15 ns maximum access time**
- **Reliable titanium-tungsten fuses (TiW) guarantees greater than 98% programming yields**
- **Low-voltage generic programming**
- **Pin-compatible with standard Schottky PROMs**
- **PNP inputs for low input current**

Applications

- **Programmable logic element (PLE™) 5 inputs, 8 outputs, 32 product terms per output**
- **Address decoder**
- **Priority encoder**

Description

The 53/63S080, 53/63S081 and 63S081A feature low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

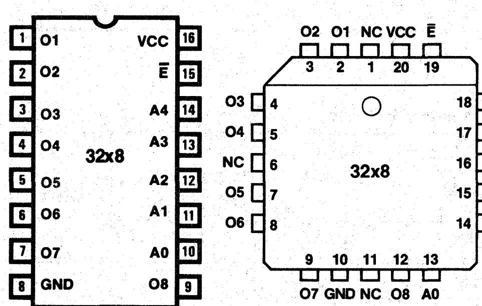
Programming

The 53/63S080, 53/63S081 and 63S081A are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

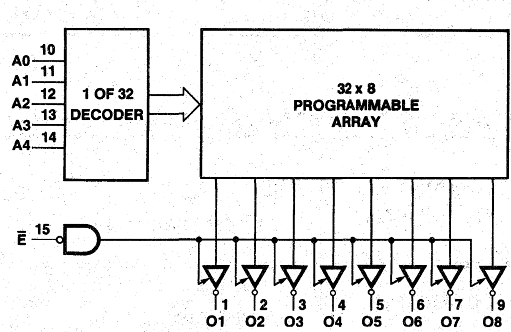
Selection Guide

MEMORY		PACKAGE		OUTPUT	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE			0°C to +75°C	-55°C to +125°C
1/4 K	32x8	16 (20)	N,J,F,W (NL),(L)	TS	Enhanced	63S081A	—
				TS	Standard	63S081	53S081
				OC		63S080	53S080

Pin Configurations



Block Diagram



PLE™ is a trademark of Monolithic Memories.

TWX: 910-338-2376
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Monolithic Memories MMI

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65 °C to +150 °C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	TYP†	MAX	COMMERCIAL MIN	TYP†	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

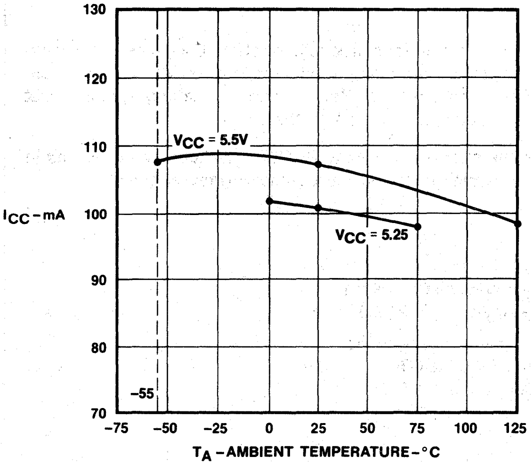
SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage*	V_{CC} = MIN	MIL I_{OH} = −2 mA		2.4			V
			COM I_{OH} = −3.2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open.				90	125	mA

Switching Characteristics Over Operating Conditions (See standard test load)

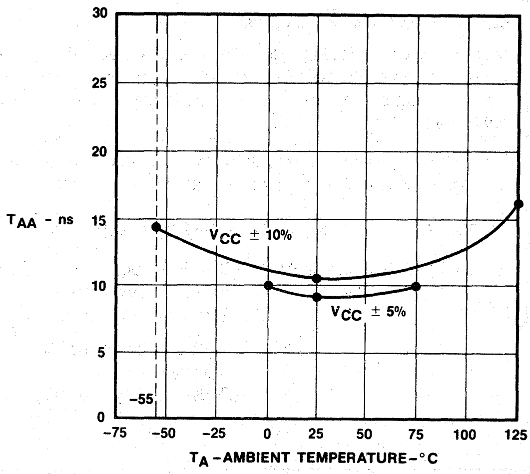
OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	MAX	UNIT
COMMERCIAL	63S081A	9	15	9	20	ns
	63S080, 63S081	9	25	9	20	
MILITARY	53S080, 53S081	9	35	9	30	

* Three-state only.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typicals at 5.0 V V_{CC} and 25° C T_A.

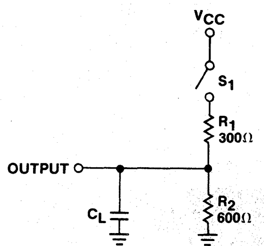
Typical I_{CC} vs Temperature



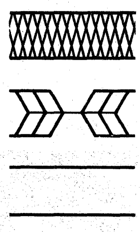
Typical T_{AA} vs Temperature



Switching Test Load

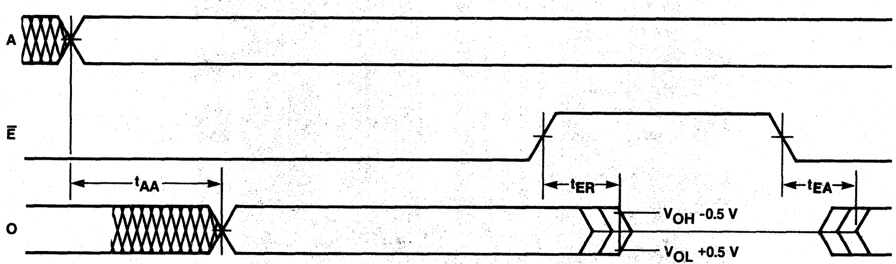


Definition of Timing Diagram



WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} and t_{EA} are tested with switch S_1 closed, C_L = 30 pF and measured at 1.5 V output level.
5. For open collector devices. t_{EA} and t_{ER} are measured at the 1.5 V output level with S_1 closed and C_L = 30 pF.
6. For three-state devices, t_{EA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   t_{ER} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} –0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION

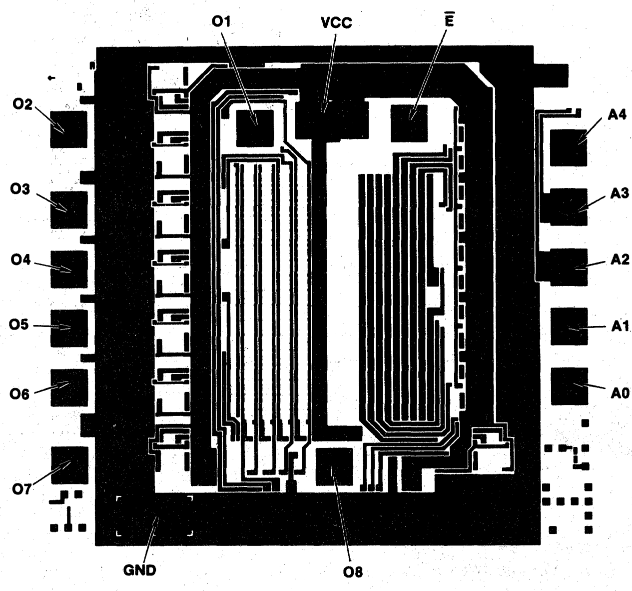
Data I/O Corp.
10525 Willows Rd. N.E.
Redmond, WA 98073

Kontron Electronics, Inc.
630 Price Ave.
Redwood City, CA 94063

Digelec Inc.
586 Weddell Dr. Suite 1
Sunnyvale, CA 94089

Stag Microsystems Inc.
528-5 Weddell Dr.
Sunnyvale, CA 94089

Metal Mask Layout



High Performance 256x4 PROM TiW PROM Family

53/63S140 53/63S141 53/63S141A

3

Features/Benefits

- **30 ns maximum access time**
- **Reliable titanium-tungsten fuses (TiW) guarantees greater than 98% programming yields**
- **Low voltage generic programming**
- **Pin-compatible with standard Schottky PROMs**
- **PNP inputs for low input current**
- **Open collector or three-state outputs**

Applications

- **Microprogram control store**
- **Microprocessor program store**
- **Look-up table**
- **Character generator**
- **Code converter**
- **Programmable Logic Element (PLE™) with 8 inputs, 4 outputs, and 256 product terms per output**

Description

The 53/63S140 and 53/63S141/A are 256x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

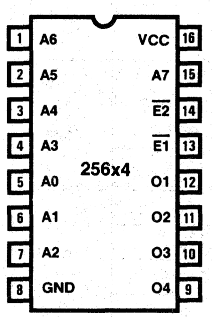
Programming

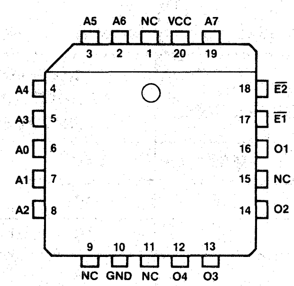
The 53/63S140 and 53/63S141/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

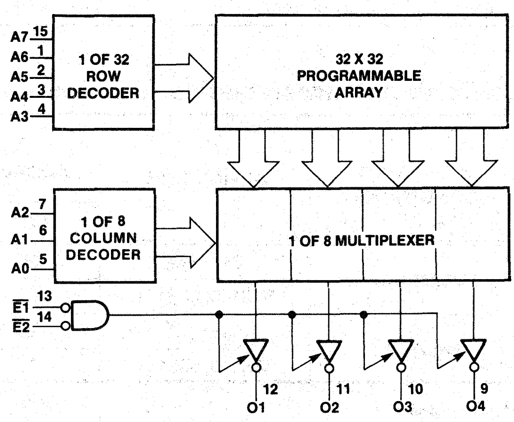
MEMORY		PACKAGE		OUTPUT	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE			0°C to +75°C	-55°C to +125°C
1K	256x4	16 (20)	N,J, (NL),(L), W,F	TS	Enhanced	63S141A	53S141A
				TS	Standard	63S141	53S141
				OC	Standard	63S140	53S140

Pin Configurations





Block Diagram



PLE™ is a trademark of Monolithic Memories

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	COM			0.45	V
				MIL			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN	COM I_{OH} = -3.2 mA		2.4			V
			MIL I_{OH} = -2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current***	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				80	130	mA

Switching Characteristics Over Operating Conditions (See standard test load)

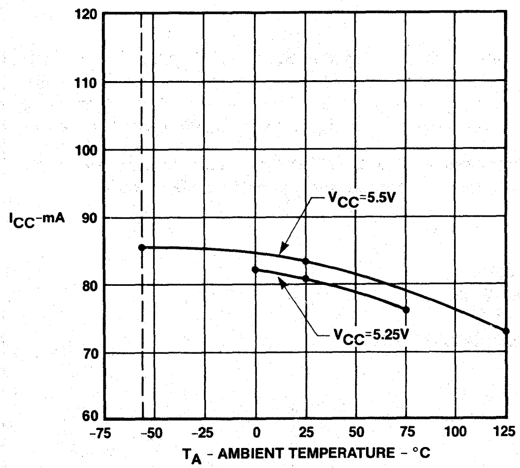
OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} MAX	UNIT
COMMERCIAL	63S141A	20	30	10	20	ns
	63S140, 63S141	20	45	10	25	
MILITARY	53S141A	20	40	10	25	
	53S140, 53S141	20	55	10	30	

* Three-state only.

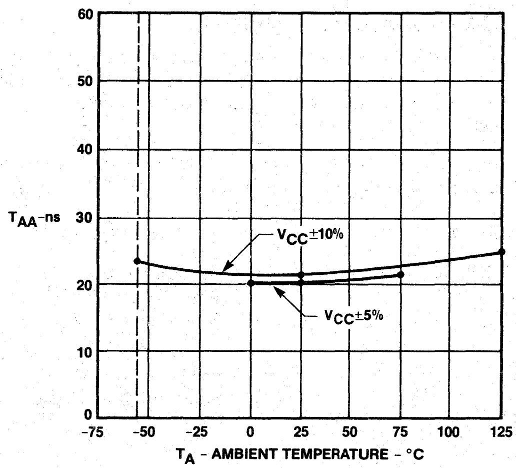
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

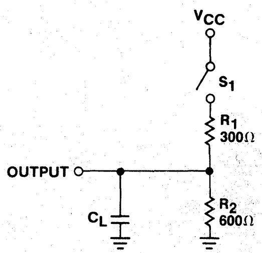
Typical I_{CC} vs Temperature



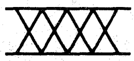
Typical T_{AA} vs Temperature



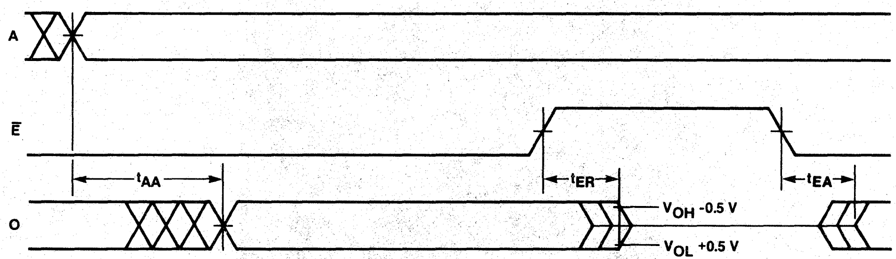
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30 pF and measured at 1.5 V output level.
5. For open collector devices, TEA and TER are measured at the 1.5 V output level with S_1 closed and C_L = 30 pF.
6. For three-state devices, TEA is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.

TER is tested with C_L = 50 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH}-0.5 V output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} +0.5 V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

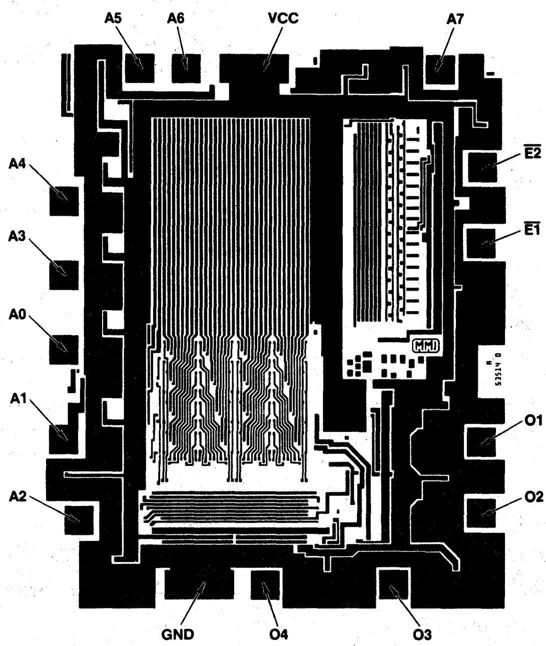
Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION	Data I/O Corp. 10525 Willows Rd. N.E. Redmond, WA 98073 Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94063	Digelec Inc. 586 Weddell Dr. Suite 1 Sunnyvale, CA 94089

Metal Mask Layout



High Performance 512x4 PROM Ti-W PROM Family

53/63S240 53/63S241 53/63S241A

Features/Benefits

- **35 ns maximum access time**
- **Reliable titanium-tungsten fuses (Ti-W) guarantees greater than 98% programming yields**
- **Low-voltage generic programming**
- **Pin-compatible with standard Schottky PROMs**
- **PNP inputs for low input current**
- **Open collector and three-state outputs**

Applications

- **Microprogram control store**
- **Microrocessor program store**
- **Look-up table**
- **Character generator**
- **Code converter**
- **Programmable logic element (PLE™) with 9 inputs, 4 outputs, 512 product terms per output**

Description

The 53/63S240 and 53/63S241/A are 512x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

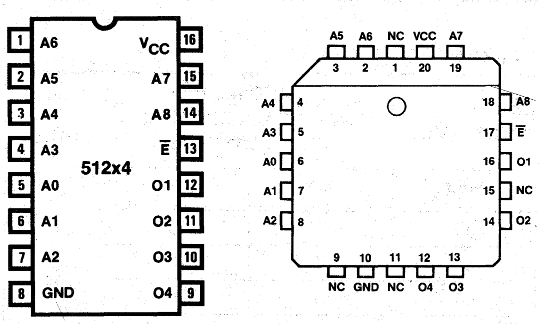
Programming

The 53/63S240 and 53/63S241/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic Ti-W PROMs. For details contact the factory.

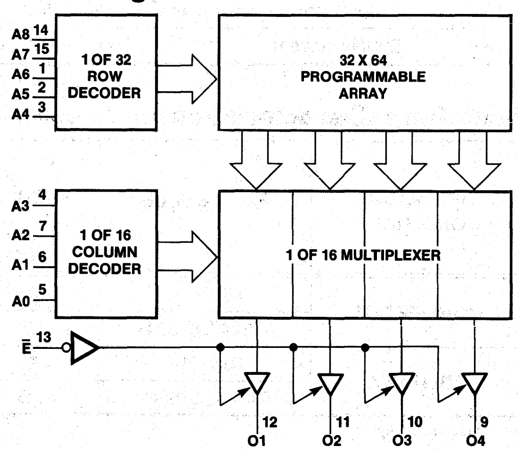
Selection Guide

MEMORY		PACKAGE		OUTPUT	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE			0°C to +75°C	−55°C to +125°C
2 K	512x4	16 (20)	N,J, (NL), (L),(W)	TS	Enhanced	63S241A	53S241A
				TS	Standard	63S241	53S241
				OC	Standard	63S240	53S240

Pin Configurations



Block Diagram



PLE™ is a trademark of Monolithic Memories.

TWX: 910-338-2376
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Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	COM			0.45	V
				MIL			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN	COM I_{OH} = −3.2 mA		2.4			V
			MIL I_{OH} = −2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current* **	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX, all inputs grounded, all outputs open.				80	130	mA

Switching Characteristics Over Operating Conditions (See standard test load)

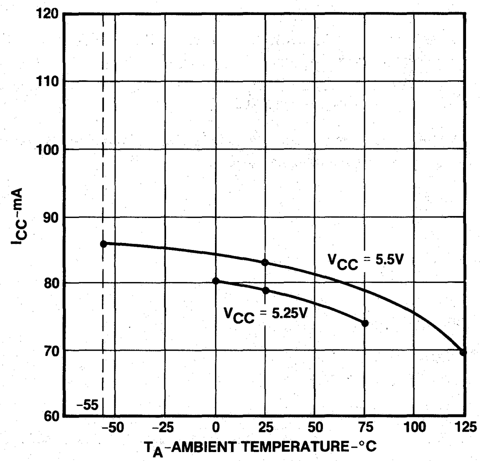
OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		UNIT
		TYP†	MAX	TYP†	MAX	
COMMERCIAL	63S241A	25	35	12	20	ns
	63S240, 63S241	25	45	12	25	
MILITARY	53S241A	25	45	12	25	
	53S240, 53S241	25	55	12	30	

* Three-state only.

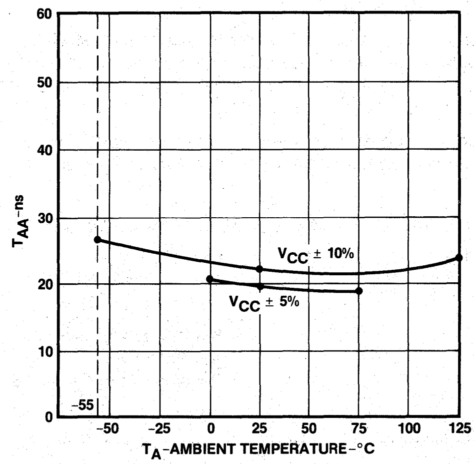
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

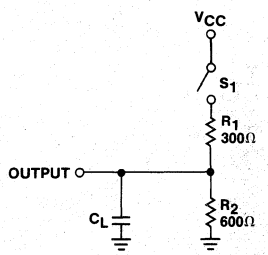
Typical I_{CC} vs Temperature



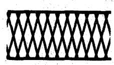
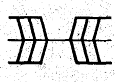
Typical T_{AA} vs Temperature



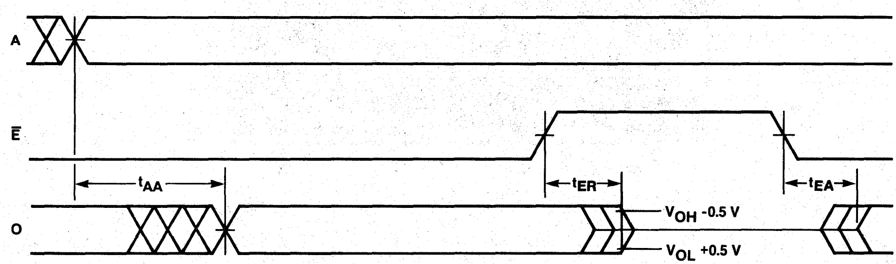
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE	NOT APPLICABLE

Definition of Waveforms



NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30 pF and measured at 1.5 V output level.
5. For open collector devices, TEA and TER are measured at the 1.5 output level with S_1 closed and C_L = 30 pF.
6. For three-state devices, TEA is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.

   TER is tested with C_L = 5 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} - 0.5 output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} + 0.5 output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION

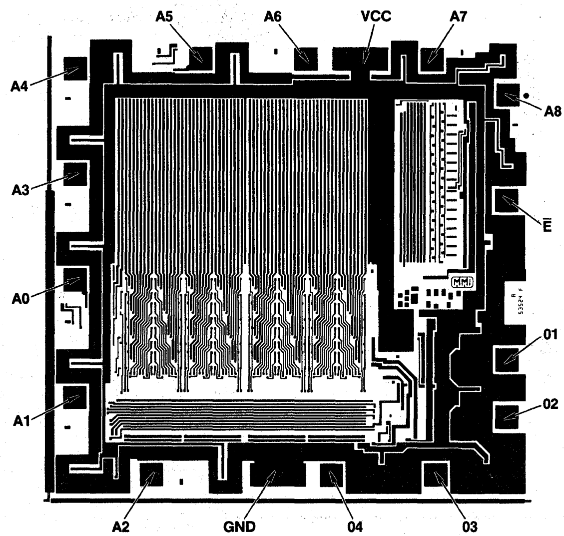
Data I/O Corp.
10525 Willows Rd. N.E.
Redmond, WA 98052

Kontron Electronics, Inc.
630 Price Ave.
Redwood City, CA 94036

Digelec Inc.
7335 E. Acoma Dr.
Suite 103
Scottsdale, AZ 85260

Stag Systems Inc.
1120 San Antonio Rd.
Palo Alto, CA 94303

Metal Mask Layout



High Performance 256x8 PROM TiW PROM Family

53/63S280 53/63S281 53/63S281A

Features/Benefits

- **28 ns maximum access time**
- **Reliable titanium-tungsten fuses (TiW) guarantees greater than 98% programming yields**
- **Low-voltage generic programming**
- **Pin-compatible with standard Schottky PROMs**
- **PNP inputs for low input current**
- **Open collector or three-state outputs**

Applications

- **Microprogram control store**
- **Microprocessor program store**
- **Look-up table**
- **Character generator**
- **Code converter**
- **Programmable Logic Element (PLE™) with 8 inputs, 8 outputs, and 256 product terms per output**

Description

The 53/63S280 and 53/63S281/A are 256x8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

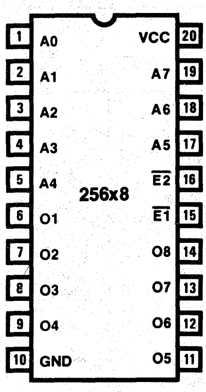
The 53/63S280 and 53/63S281/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

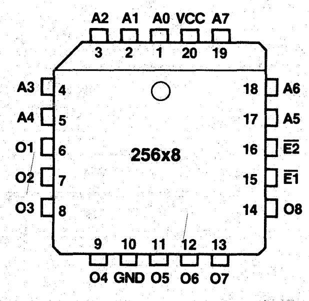
Selection Guide

MEMORY		PACKAGE		OUTPUT	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE			0°C to +75°C	−55°C to +125°C
2K	256x8	20	N,J NL,L*, W*	TS	Enhanced	63S281A	53S281A
				TS	Standard	63S281	53S281
				OC	Standard	63S280	53S280

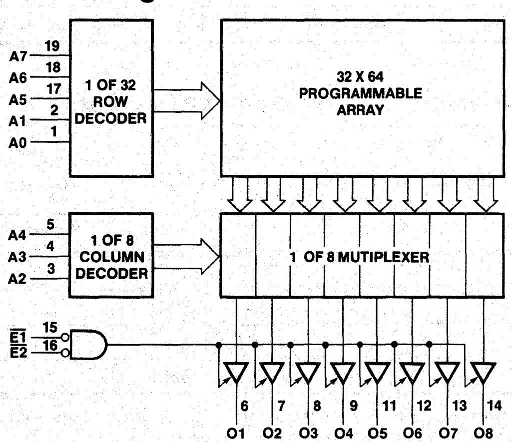
*Contact factory for package dimensions.

Pin Configurations





Block Diagram



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Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage	Guaranteed input logical low voltage for all inputs††					0.8	V
V_{IH}	High-level input voltage	Guaranteed input logical high voltage for all inputs††			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN	Com I_{OH} = −3.2 mA		2.4			V
			Mil I_{OH} = −2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				90	140	mA

Switching Characteristics Over Operating Conditions (See standard test load)

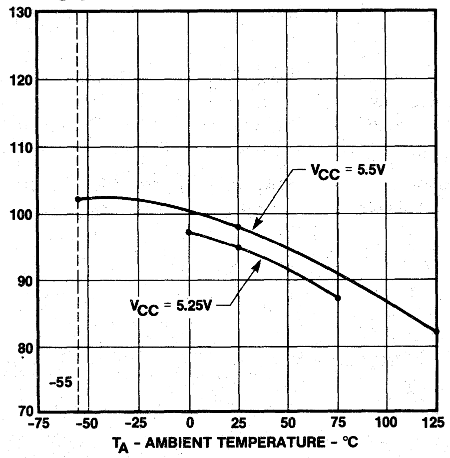
OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} MAX	UNIT
COMMERCIAL	63S281A	21	28	18	25	ns
	63S280, 63S281	21	45	18	25	
MILITARY	53S281A	21	40	18	30	
	53S280, 53S281	21	50	18	30	

* Three-state only. ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

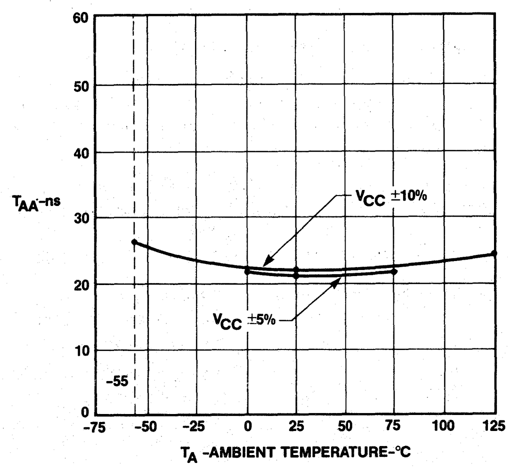
† Typicals at 5.0 V V_{CC} and 25°C T_A.

†† V_{IL} and V_{IH} limits are absolute values with respect to the device ground pin(s) and includes all overshoots due to test equipment noise.

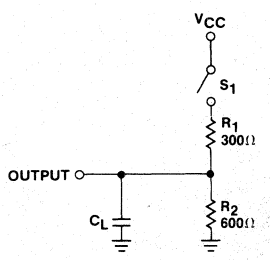
Typical I_{CC} vs Temperature



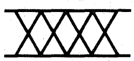
Typical T_{AA} vs Temperature



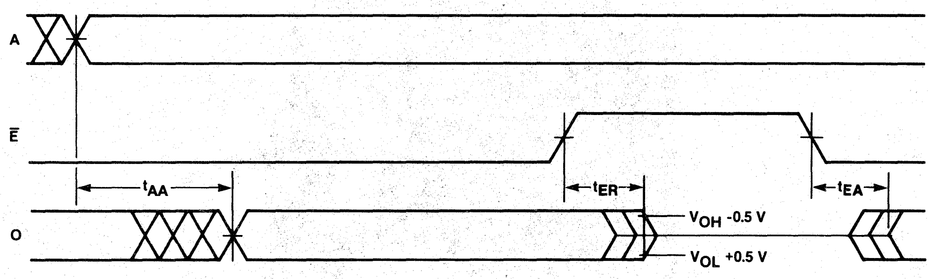
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30 pF and measured at 1.5 V output level.
5. For open collector devices, TEA and TER are measured at the 1.5 V output level with S_1 closed and C_L = 30 pF.
6. For three-state devices, TEA is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.
TER is tested with C_L = 5 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} +0.5 V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

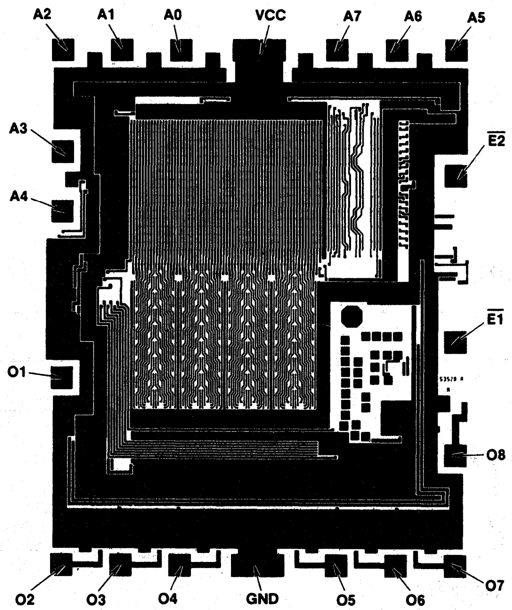
Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION	Data I/O Corp. 10525 Willows Rd. N.E. Redmond, WA 98073 Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94063	Digelec Inc. 586 Weddell Dr. Suite 1 Sunnyvale, CA 94089

Metal Mask Layout



High Performance 1024x4 PROM TiW PROM Family

53/63S440 53/63S441 53/63S441A

Features/Benefits

- 35 ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantees greater then 98% programming yields
- Low-voltage generic programming
- Pin-compatible with standard Schottky PROMs
- PNP inputs for low input current
- Open collector and three-state outputs

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable logic element (PLE™) 10 inputs, 4 outputs, 1024 product terms

Description

The 53/63S440 and 53/63S441/A are 1024x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping with open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

The 53/63S440 and 53/63S441/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

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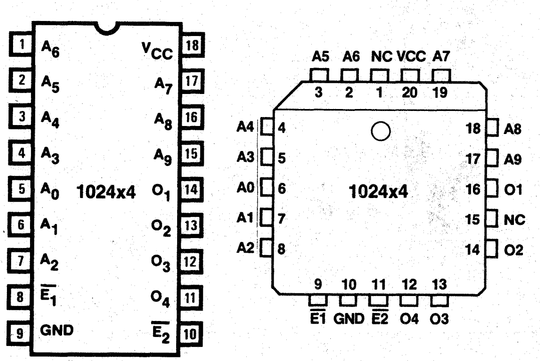
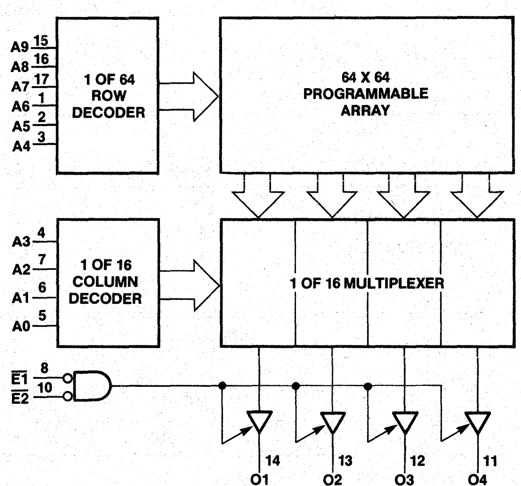
Selection Guide

MEMORY		PACKAGE		OUTPUT	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE			0°C to +75°C	-55°C to +125°C
4 K	1024x4	18 (20)	N,J,F,W, (NL),(L)	TS	Enhanced	63S441A	53S441A
				TS	Standard	63S441	53S441
				OC		63S440	53S440

Pin Configuration



Block Diagram



PLE™ is a trademark of Monolithic Memories.

TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage*	V_{CC} = MIN	MIL I_{OH} = −2 mA		2.4			V
			COM I_{OH} = −3.2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current***	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open.				95	140	mA

Switching Characteristics Over Operating Conditions (See standard test load)

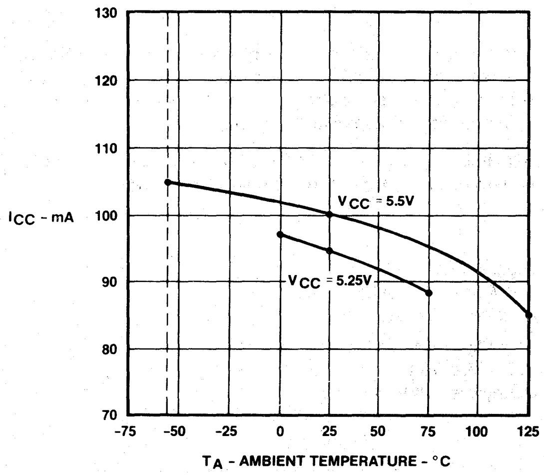
OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		UNIT
		TYP†	MAX	TYP†	MAX	
COMMERCIAL	63S441A	24	35	16	25	ns
	63S440, 63S441	24	45	16	25	
MILITARY	53S441A	24	50	16	30	
	53S440, 53S441	24	55	16	30	

* Three-state only.

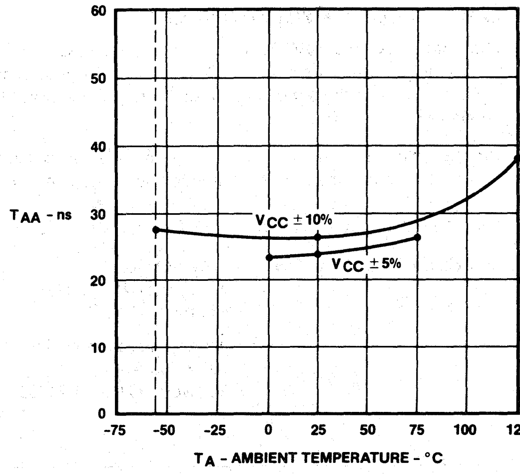
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

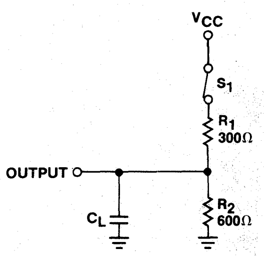
Typical I_{CC} vs Temperature



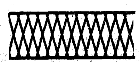
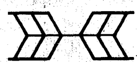
Typical T_{AA} vs Temperature



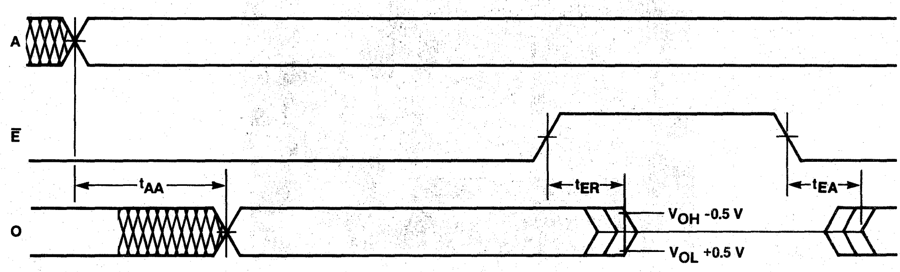
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} and t_{EA} are tested with switch S_1 closed, C_L = 30 pF and measured at 1.5 V output level.
5. t_{ER} is tested with C_L = 5 pF and S_1 closed. "1" to high-impedance test is measured at V_{OH} -0.5 V output level, "0" to high-impedance test is measured at V_{OL} + 0.5 V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

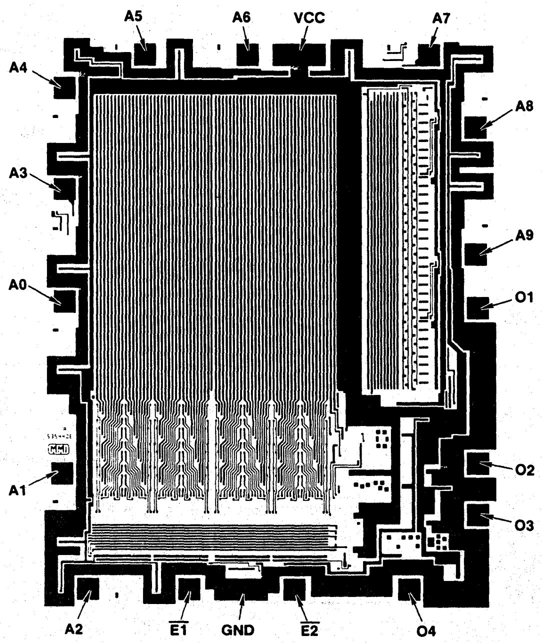
Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION		
	Data I/O Corp. 10525 Willows Rd. N.E. Redmond, WA 98073	Digelec Inc. 586 Weddell Dr. Suite 1 Sunnyvale, CA 94089
	Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94063	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale, CA 94089

Die Configuration



High Performance 512x8 PROM TiW PROM Family

53/63S480 53/63S481 53/63S481A

3

Features/Benefits

- **30 ns maximum access time**
- **Reliable titanium-tungsten fuses (TiW) guarantees greater than 98% programming yields**
- **Low voltage generic programming**
- **Pin-compatible with standard Schottky PROMs**
- **PNP inputs for low input current**
- **Open collector or three-state outputs**

Applications

- **Microprogram control store**
- **Microprocessor program store**
- **Look-up table**
- **Character generator**
- **Code converter**
- **Programmable Logic Element (PLE™) with 9 inputs, 8 outputs, and 512 product terms per output**

Description

The 53/63S480 and 53/63S481/A are 512x8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

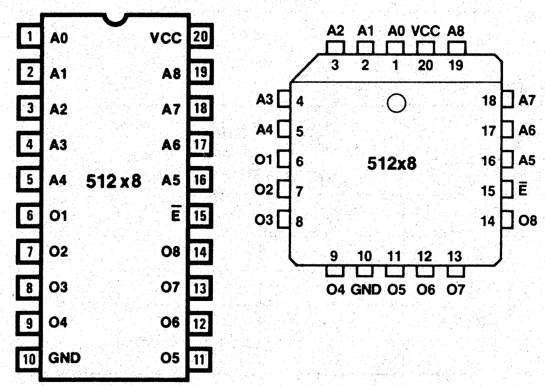
The 53/63S480 and 53/63S481/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

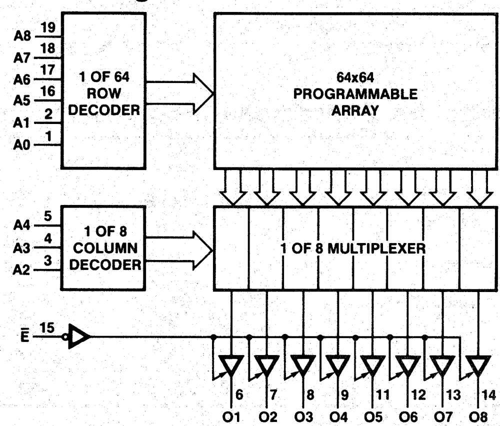
MEMORY		PACKAGE		OUTPUT	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE			0°C to +75°C	-55°C to +125°C
4K	512x8	20	N,J NL,L*, F*	TS	Enhanced	63S481A	53S481A
				TS	Standard	63S481	53S481
				OC	Standard	63S480	53S480

*Contact factory for package dimensions.

Pin Configurations



Block Diagram



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage	Guaranteed input logical low voltage for all inputs††					0.8	V
V_{IH}	High-level input voltage	Guaranteed input logical high voltage for all inputs††			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4			V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				104	155	mA

Switching Characteristics Over Operating Conditions (See standard test load)

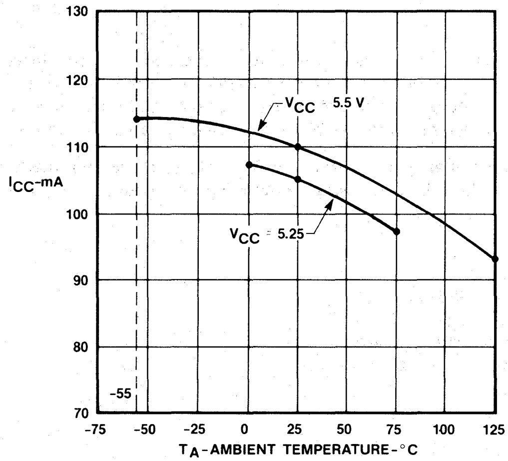
OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} MAX	UNIT
COMMERCIAL	63S481A	22	30	18	25	ns
	63S480, 63S481	22	45	18	25	
MILITARY	53S481A	22	40	18	30	
	53S480, 53S481	22	50	18	35	

* Three-state only. ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

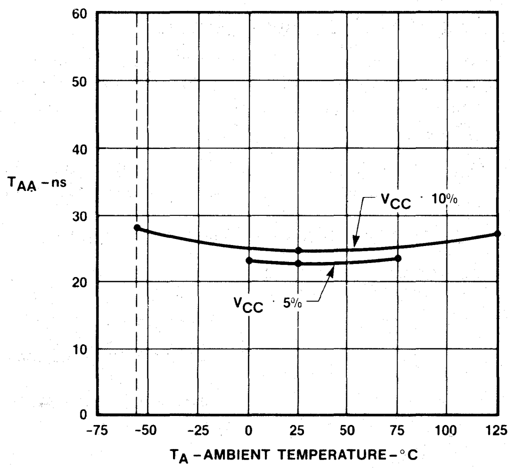
† Typicals at 5.0 V V_{CC} and 25°C T_A.

†† V_{IL} and V_{IH} limits are absolute values with respect to the device ground pin(s) and includes all overshoots due to test equipment noise.

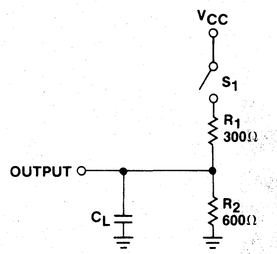
Typical I_{CC} vs Temperature



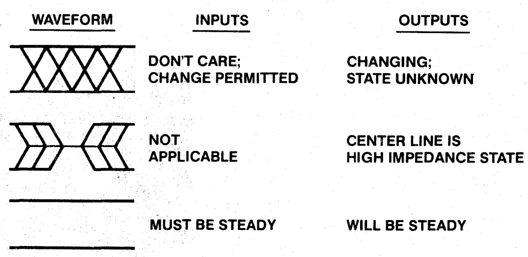
Typical T_{AA} vs Temperature



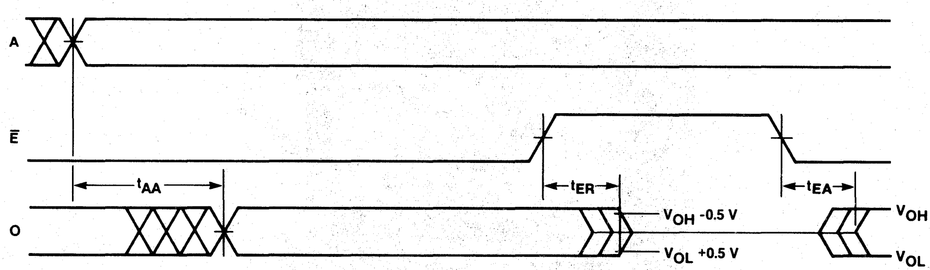
Switching Test Load



Definition of Timing Diagram



Definition of Waveforms



NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30 pF and measured at 1.5 V output level.
5. For open collector devices, TEA and TER are measured at the 1.5 V output level with S_1 closed and C_L = 30 pF.
6. For three-state devices, TEA is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.

TER is tested with C_L = 5 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} +0.5 V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

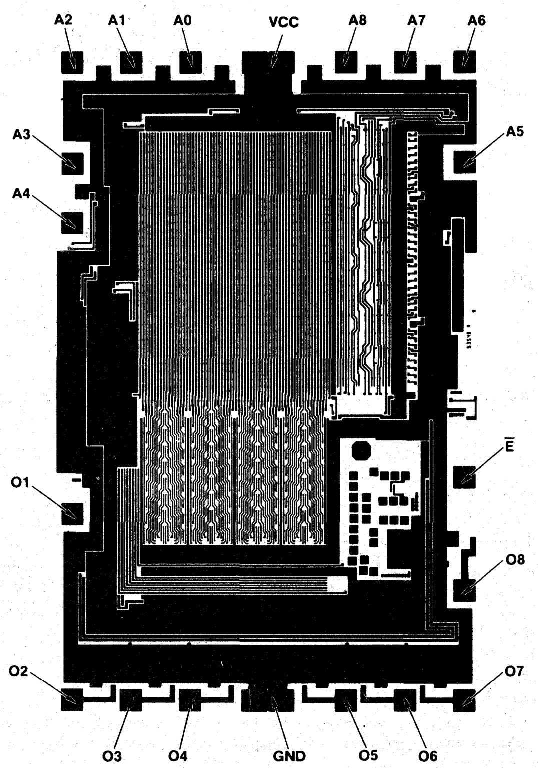
SOURCE AND LOCATION

Data I/O Corp.
10525 Willows Rd. N.E.
Redmond, WA 98073

Kontron Electronics, Inc.
630 Price Ave.
Redwood City, CA 94063

Digelec Inc.
586 Weddell Dr.
Suite 1
Sunnyvale, CA 94089

Metal Mask Layout



High Performance 2048x4 PROM TiW PROM Family

53/63S841 53/63S841A

3

Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantees greater than 98% programming yields
- Low voltage generic progamming
- Pin-compatible with standard Schottky PROMs
- PNP inputs for low input current

Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with eleven inputs, four outputs and 2048 product terms per output

Description

The 53/63S841 and 53/63S841A are 2048x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

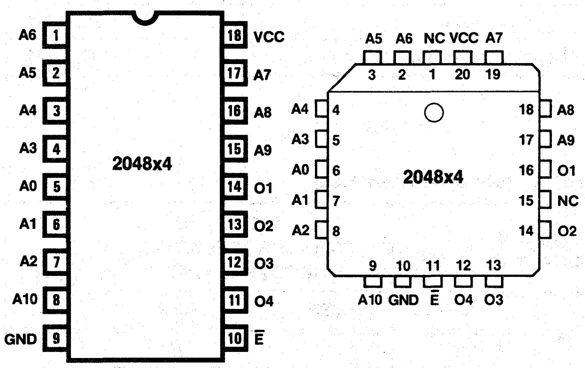
Programming

The 53/63S841 and 53/63S841A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs.

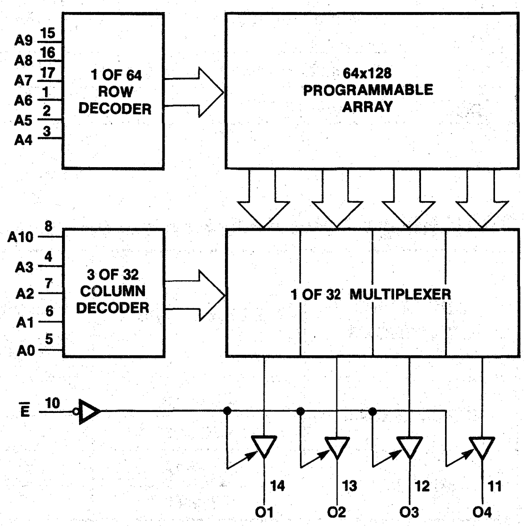
Selection Guide

MEMORY		PACKAGE		OUTPUT	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE			0°C to +75°C	-55°C to +125°C
8K	2048x4	18 (20)	N,J, (NL),(L), W,F	TS	Enhanced	63S841A	53S841A
					Standard	63S841	53S841

Pin Configurations



Block Diagram



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	COM			0.45	V
				MIL			0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	COM I_{OH} = −3.2 mA		2.4			V
			MIL I_{OH} = −2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.					150	mA

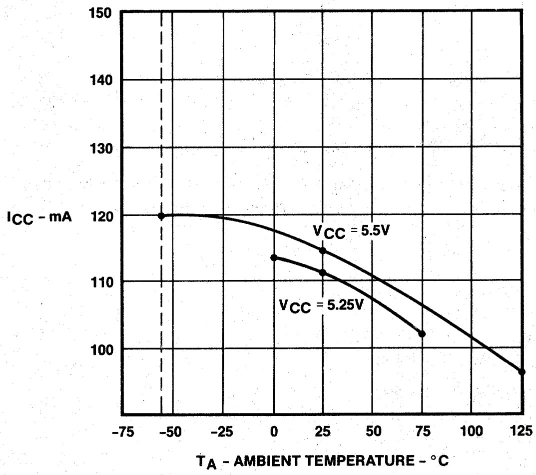
Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S841A		35		25	ns
	63S841		50		25	
MILITARY	53S841A		50		30	
	53S841		55		30	

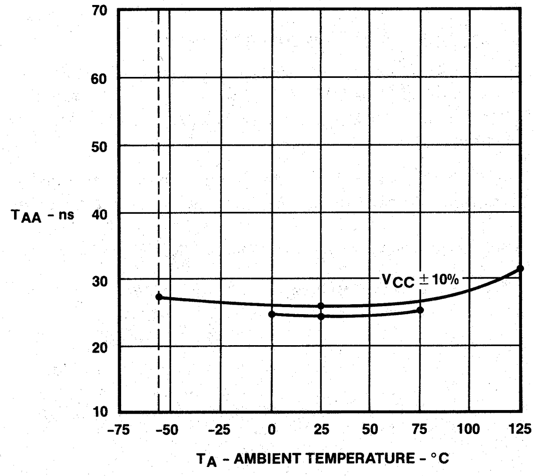
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

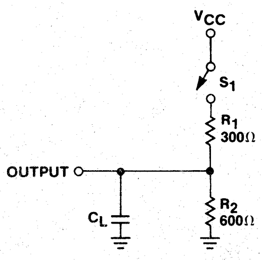
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature



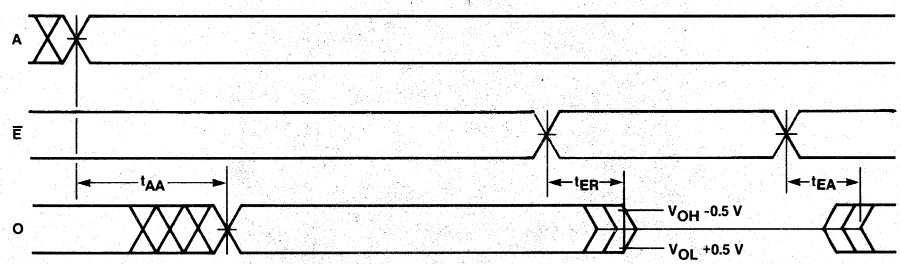
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V.

2. Input rise and fall times 2-5 ns from 0.8 V. to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30 pF and measured at 1.5 V output level.
5. TEA is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.

   TER is tested with C_L = 5 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} -0.5 V output level: S_1 is closed for "0" to high-impedance test measured at V_{OL} + 0.5 V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION

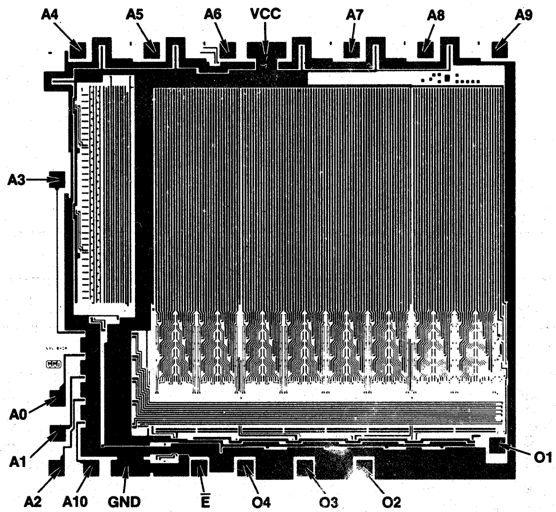
Data I/O Corp.
10525 Willows Rd. N.E.
Redmond, WA 98073

Kontron Electronics, Inc.
630 Price Ave.
Redwood City, CA 94063

Digelec Inc.
586 Weddell Dr.
Suite 1
Sunnyvale, CA 94089

Stag Microsystems Inc.
528-5 Weddell Dr.
Sunnyvale, CA 94089

Metal Mask Layout



High Performance 4096x4 PROM TiW PROM Family

53/63S1641 53/63S1641A

Features/Benefits

- **35 ns maximum access time**
- **Reliable titanium-tungsten fuses (TiW)**
- **Low-voltage generic programming**
- **Pin-compatible with standard Schottky PROMs**
- **PNP inputs for low input current**

Applications

- **Microprogram control stores**
- **Microprocessor program store**
- **Look-up table**
- **Character generator**
- **Code converter**
- **Programmable Logic Element (PLE™) 12 inputs, 4 outputs, 4096 product terms per output**

Description

The 53/63S1641 features low input current PNP inputs, full Schottky clamping and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide pre-programming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

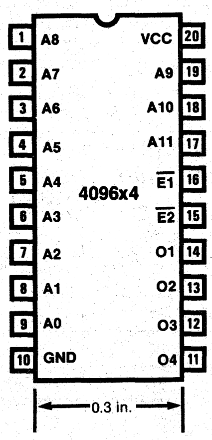
Programming

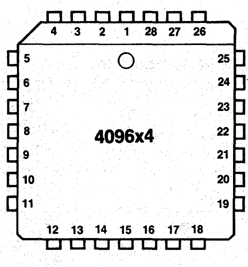
The 53/63S1641 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

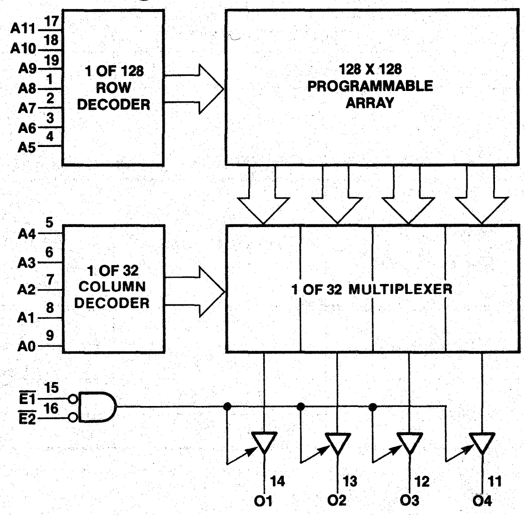
MEMORY			PACKAGE	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT			0°C to +75°C	-55°C to +125°C
16K	4Kx4	TS	N,J, NL	Standard	63S1641	53S1641
				Enhanced	63S1641A	53S1641A

Pin Configuration





Block Diagram



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Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5V to 7V	12V
Input voltage	-1.5V to 7V	7V
Input current	-30mA to +5mA	
Off-state output voltage	-0.5V to 5.5V	12V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = -2 mA		2.4			V
			COM I_{OH} = -3.2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				130	175	mA

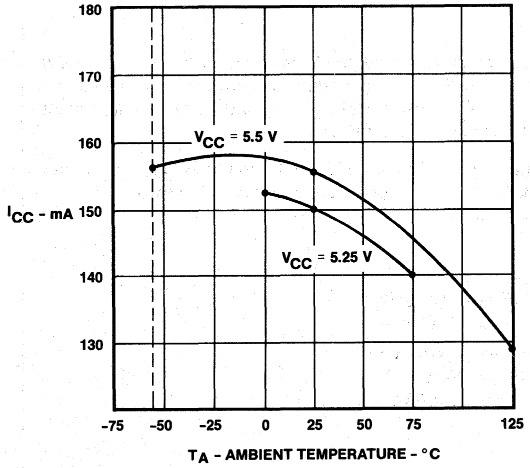
Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TIME	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		UNIT
		TYP†	MAX	TYP†	MAX	
COMMERCIAL	63S1641A	28	35	12	25	ns
	63S1641	28	50	12	25	
MILITARY	53S1641A	28	50	12	30	
	53S1641	28	65	12	30	

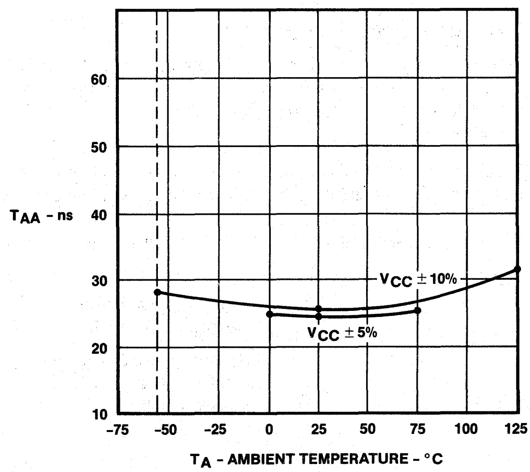
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25° C T_A.

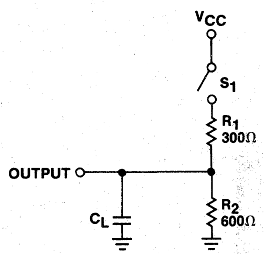
Typical I_{CC} vs Temperature



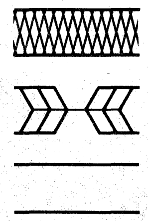
Typical T_{AA} vs Temperature



Switching Test Load

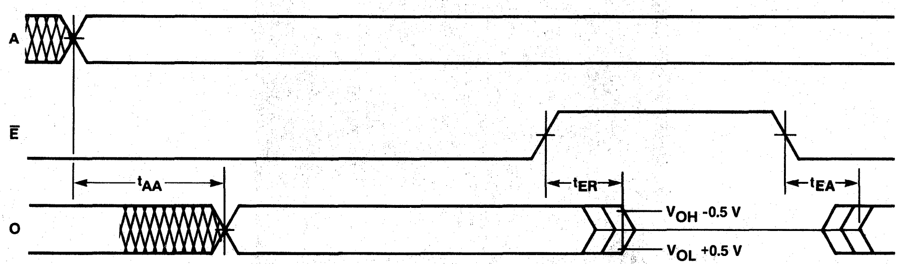


Definition of Timing Diagram



WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
5. t_{EA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

t_{ER} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5 output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5 V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION

Data I/O Corp.
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Digelec Inc.
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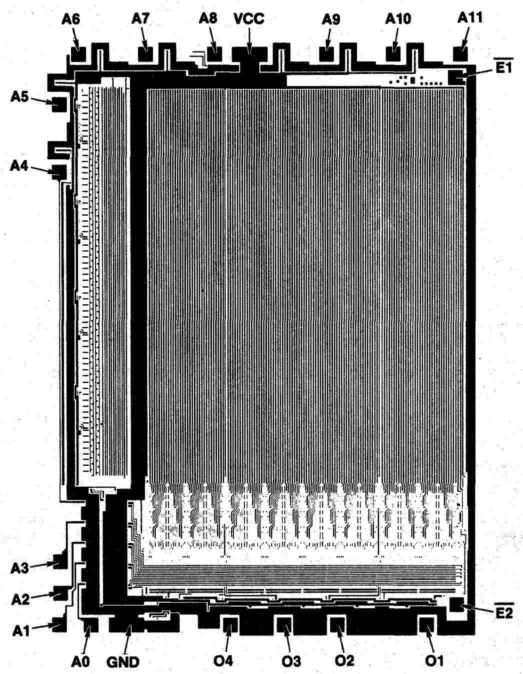
Sunnyvale, CA 94089

Stag Microsystems Inc.
528-5 Weddell Dr.
Sunnyvale, CA 94089

Metal Mask Layout



High Performance 2048x8 PROM TiW PROM Family

53/63S1681 53/63S1681A

Features/Benefits

- 35 ns maximum access time
- 16384-bit memory
- Reliable titanium-tungsten fuses (TiW)
- Pin-compatible with standard Schottky PROMs
- Available in space saving SKINNYDIP® package

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) 11 inputs, 8 outputs, 2048 product terms per output

Description

The 53/63S1681 is a high-speed 2Kx8 PROM which uses industry standard package and pin out. In addition, the device is available in the 24-pin (0.3 in.) SKINNYDIP®.

The family features low current PNP inputs, full Schottky clamping and three-state outputs. The Titanium-Tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

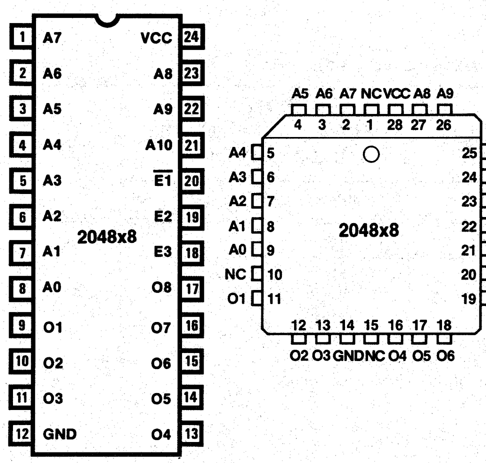
The 53/63S1681 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

3

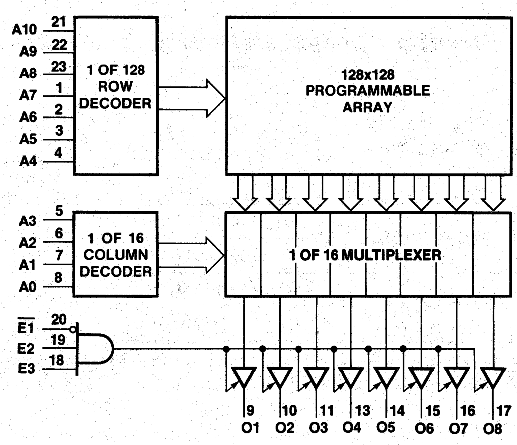
Selection Guide

MEMORY			PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	-55°C to +125°C
16K	2048x8	TS	24 (28)	N,NS, J,JS,W, (NL),(L)	Standard	63S1681	53S1681
					Enhanced	63S1681A	53S1681A

Pin Configurations



Block Diagram



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Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −2 mA		2.4			V
			COM I_{OH} = −3.2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL, all outputs open.				130	175	mA

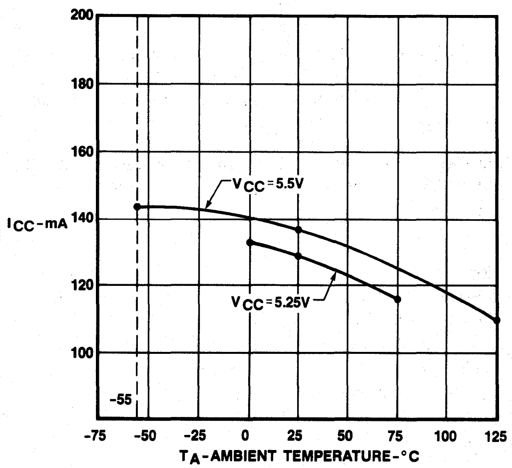
Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		UNIT
		TYP†	MAX	TYP†	MAX	
COMMERCIAL	63S1681A	27	35	18	25	ns
	63S1681	27	50	18	30	
MILITARY	53S1681A	27	45	18	35	
	53S1681	27	60	18	35	

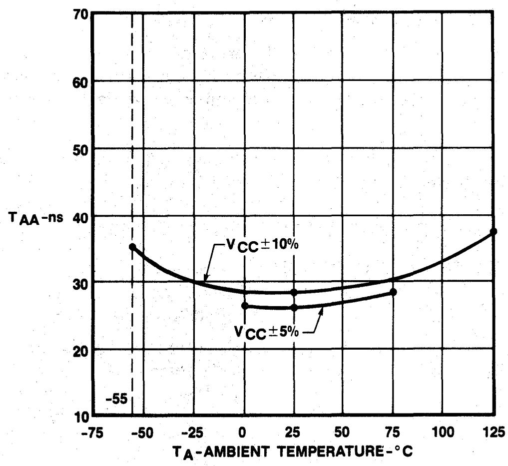
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25° C T_A.

Typical I_{CC} vs Temperature

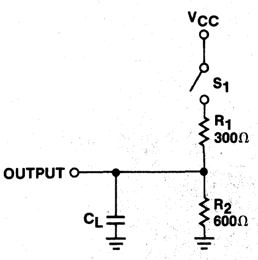


Typical T_{AA} vs Temperature

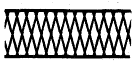
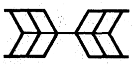


3

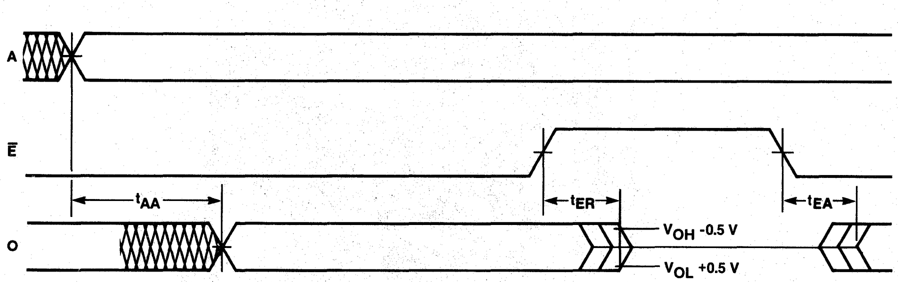
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
5. t_{EA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test. t_{ER} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} − 0.5 output level: S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5 V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

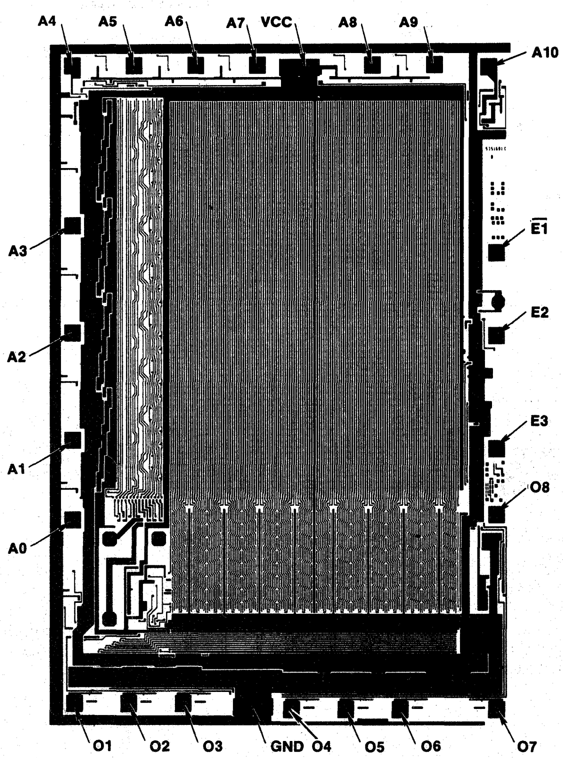
Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION	Data I/O Corp. 10525 Willows Rd. N.E. Redmond, WA 98073	Digelec Inc. 586 Weddell Dr. Suite 1 Sunnyvale, CA 94089
	Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94063	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale, CA 94089

Metal Mask Layout



High Performance 4096x8 PROM TiW PROM Family

53/63S3281 53/63S3281A

Features/Benefits

- 40 ns maximum access time
- 32768-bit memory
- Reliable titanium-tungsten fuses (TiW)
- Pin-compatible with standard Schottky PROMs
- PNP inputs for low input current

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) 12 inputs, 4096 product terms, 8 outputs

Description

The 53/63S3281 is a high-speed 4Kx8 PROM which uses industry standard pin out.

The family features low-current PNP inputs, full Schottky clamping and three-state outputs. The Titanium-Tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

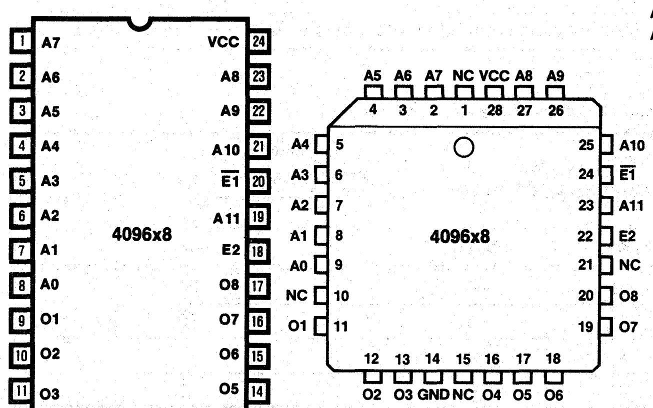
The 53/63S3281 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

3

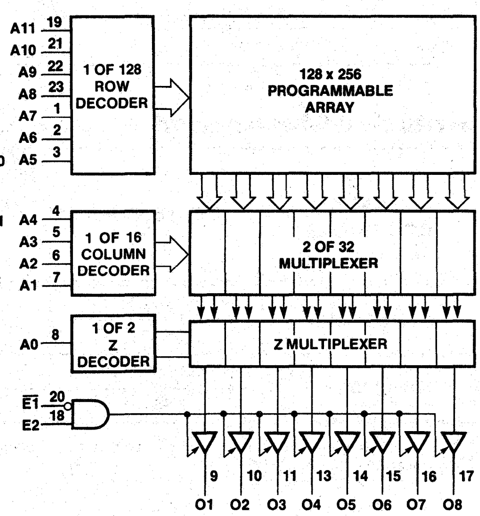
Selection Guide

MEMORY			PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	-55°C to +125°C
32K	4096x8	TS	24 (28)	N,J, (NL),(L), W	Standard	63S3281	53S3281
					Enhanced	63S3281A	53S3281A

Pin Configurations



Block Diagram



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Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −2 mA		2.4			V
			COM I_{OH} = −3.2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				150	190	mA

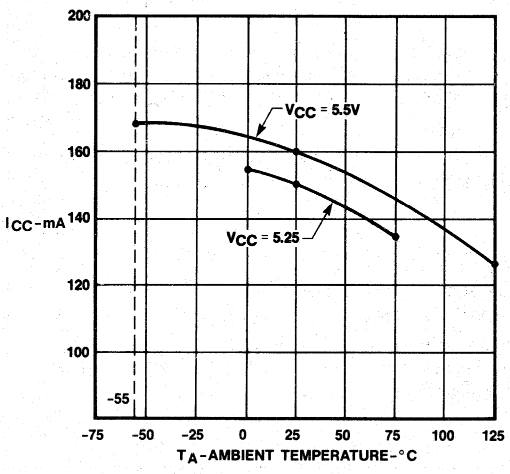
Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S3281A	31	40	18	20	ns
	63S3281	31	50	18	30	
MILITARY	53S3281A	31	50	18	35	
	53S3281	31	60	18	35	

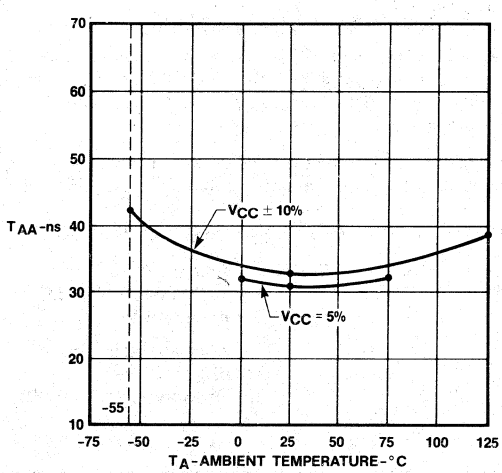
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC} and 25°C T_A.

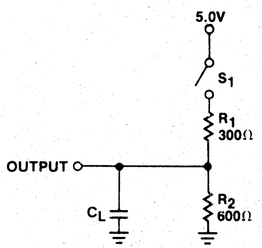
Typical I_{CC} vs Temperature



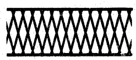
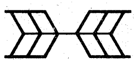
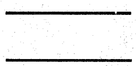
Typical T_{AA} vs Temperature



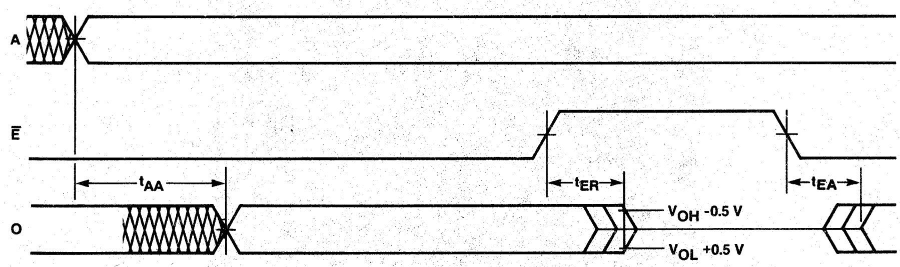
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5V output level.
5. t_{EA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test. t_{ER} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5 output level: S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

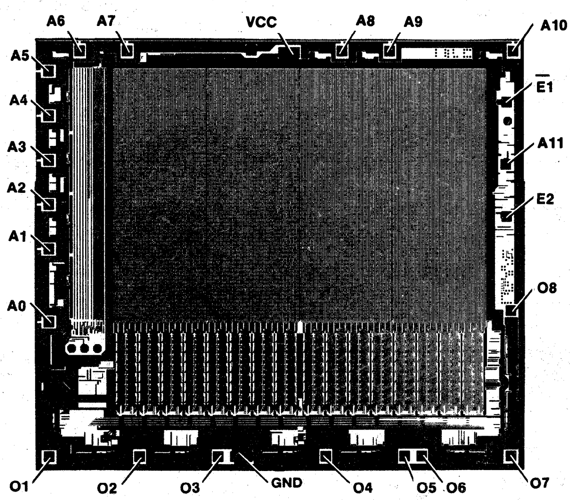
Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION		
	Data I/O Corp. 10525 Willows Rd. N.E. Redmond, WA 98073	Digelec Inc. 586 Weddell Dr. Suite 1 Sunnyvale, CA 94089
	Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94063	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale, CA 94089

Metal Mask Layout



High Performance 512x8 Registered PROM

53/63RA481 53/63RA481A

Features/Benefits

- **Versatile synchronous and asynchronous enables**
- **Asynchronous preset and clear**
- **Edge-triggered "D" registers**
- **8-bit-wide in 24-pin SKINNYDIP® for high board density**
- **On-chip register simplifies system timing**
- **Faster cycle times**
- **16 mA I_{OL} output drive capability**
- **Reliable titanium-tungsten fuses (Ti-W), with programming yields typically greater than 98%**

Applications

- **Microprogram control store**
- **State sequencers/state machines**
- **Next address generation**
- **Mapping PROM**

Description

The 53/63RA481 and 53/63RA481A are 512x8 Registered PROMs with on-chip "D" type registers, versatile output enable control through synchronous and asynchronous three-state enable inputs, and asynchronous preset and clear.

Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERFORMANCE	PINS	TYPE	MIL	COM
4K	Standard	24 (28)	NS,JS, (NL), (L)	53RA481	63RA481
	Enhanced			53RA481A	63RA481A

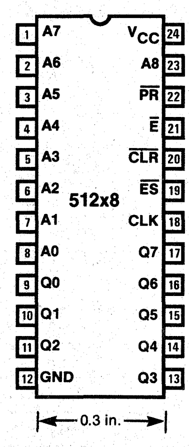
Flatpak — Contact the factory.

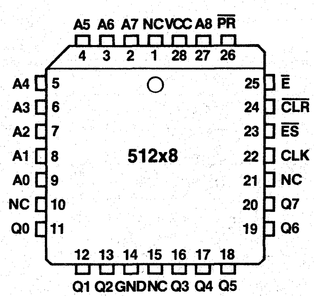
Data is transferred into the output registers on the rising edge of the clock. The data will appear at the outputs provided that both the asynchronous ($\overline{E}$) and synchronous ($\overline{ES}$) enables are Low. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made more flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting $\overline{E}$ to a High or if $\overline{ES}$ is High when the rising clock edge occurs. When V_{CC} power is first applied, the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high-impedance state.

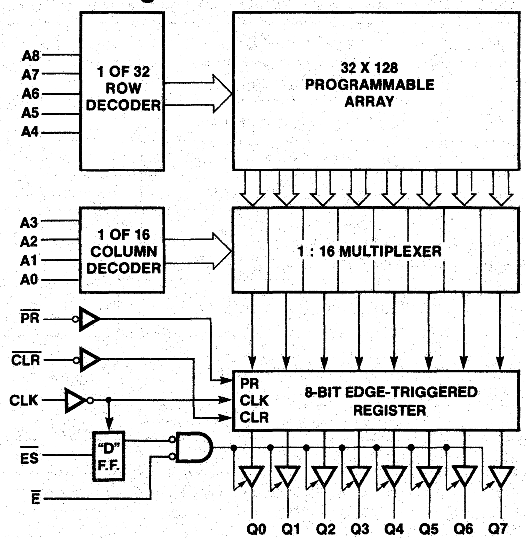
The output registers will be set to all Highs when preset is Low independent of the state of clock. The output registers will be reset to all Lows when clear is Low independent of the state of clock. Note that preset and clear are exclusive operations and cannot occur simultaneously.

Pin Configurations





Block Diagram



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	COMMERCIAL				MILITARY				UNIT
			63RA481A		63RA481		53RA481A		53RA481		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	5.0	4.75	5.25	4.75	5.25	4.5	5.5	4.5	5.5	V
T_A	Operating free-air temperature	25	0	75	0	75	-55	125	-55	125	°C
t_w	Width of clock (High or Low)	10	20		20		20		20		ns
t_{prw} / t_{clrw}	Width of preset or clear (Low) to Output (High or Low)	10	20		20		20		20		ns
t_{prr} / t_{clrr}	Recovery from preset or clear (Low) to clock High	11	20		20		25		25		ns
t_s (A)	Setup time from address to clock	22	30		35		35		45		ns
t_s ($\overline{ES}$)	Setup time from $\overline{ES}$ to clock	7	10		10		15		15		ns
t_h (A)	Hold time from address to clock	-5	0		0		0		0		ns
t_h ($\overline{ES}$)	Hold time from $\overline{ES}$ to clock	-3	5		5		5		5		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −2 mA COM I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-40	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V			40	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	-20		-90	mA
I_{CC}	Supply Current	V_{CC} = MAX	All inputs TTL; all outputs open.		130	180	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC} and 25° C T_A.

Switching Characteristics Over Operating Conditions and using Standard Test Load

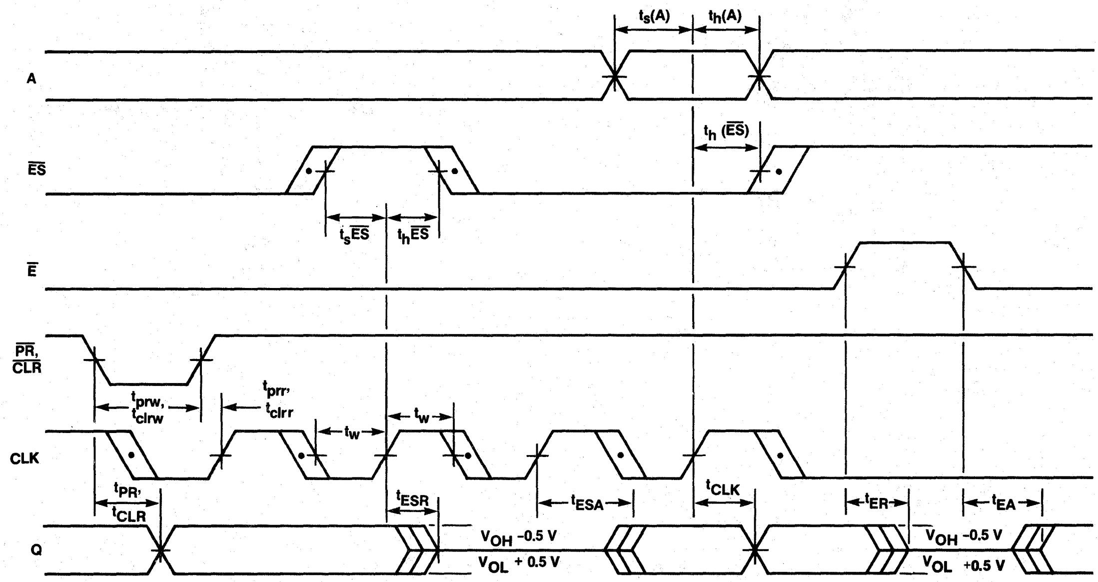
SYMBOL	PARAMETER	TYP†	COMMERCIAL 63RA481A MIN	COMMERCIAL 63RA481A MAX	COMMERCIAL 63RA481 MIN	COMMERCIAL 63RA481 MAX	MILITARY 53RA481A MIN	MILITARY 53RA481A MAX	MILITARY 53RA481 MIN	MILITARY 53RA481 MAX	UNIT
t_{CLK}	Clock to output Delay	11		15		20		20		25	ns
t_{ESA}	Clock to output access time ($\overline{ES}$)	14		25		30		30		35	ns
t_{ESR}	Clock to output recovery time ($\overline{ES}$)	14		25		30		30		35	ns
t_{EA}	Enable to output access time ($\overline{E}$)	10		20		30		25		35	ns
t_{ER}	Disable to output recovery time ($\overline{E}$)	10		20		30		25		35	ns
t_{PR}	Preset to output delay ($\overline{PR}$)	15		25		25		25		30	ns
t_{CLR}	Clear to output delay ($\overline{CLR}$)	18		25		30		35		40	ns

† Typical at 5.0 V V_{CC} and 25 °C T_A.

Function Table

$\overline{E}$	$\overline{ES}$	CLK	$\overline{PR}$	$\overline{CLR}$	A8-A0	Q7-Q0	Operation
H	X	X	X	X	X	Z	High-Impedance
X	H	↑	X	X	X	Z	High-Impedance
L	L	X	L	H	X	H	Preset
L	L	X	H	L	X	L	Clear
L	L	X	L	L	X		Illegal Operation
L	L	↑	H	H	A	Data	Memory Access

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V.

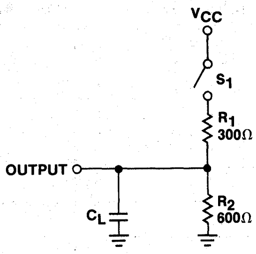
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.

3. Input access measured at the 1.5 V level.

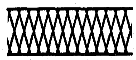
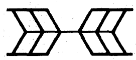
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V output level for all tests except t_{ESA} and t_{ESR}.

5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
t_{ER} and t_{ESR} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 output level: S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

Switching Test Load

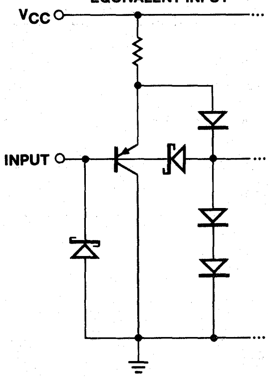


Definition of Timing Diagram

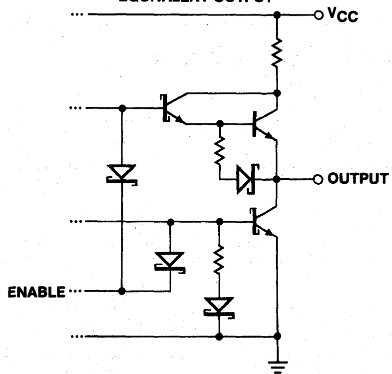
WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Schematic of Inputs and Outputs

EQUIVALENT INPUT



EQUIVALENT OUTPUT



Commercial Programmers

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Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

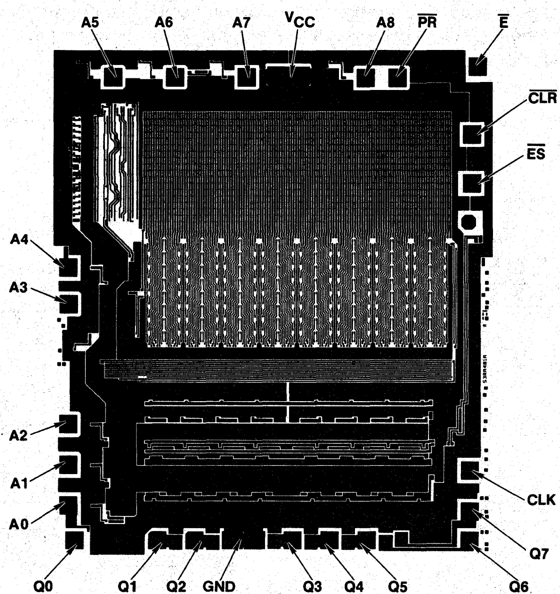
Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION		
	Data I/O Corp. 10525 Willows Rd. N.E. Redmond, WA 98073	Digelec Inc. 586 Weddell Dr. Suite 1 Sunnyvale, CA 94089
	Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94063	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale, CA 94089

3

Metal Mask Layout



High Performance 1024x8 Registered PROM

53/63RS881 53/63RS881A

Features/Benefits

- Edge triggered "D" registers
- Synchronous and asynchronous enables
- Versatile 1:16 initialization words
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM

Description

The 53/63RS881 and 53/63RS881A are 1Kx8 PROMs with on-chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ($\overline{E}$) and synchronous ($\overline{ES}$) enables are low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

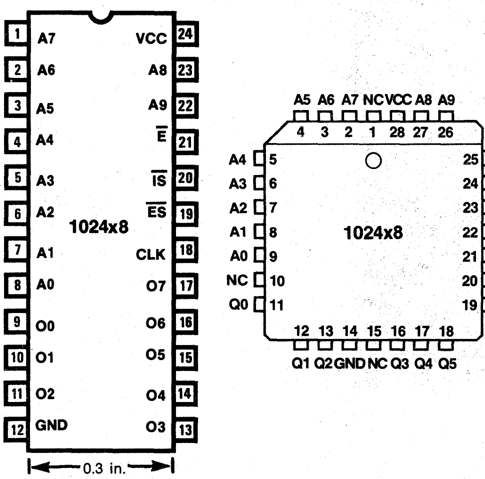
Memory expansion and data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting $\overline{E}$ to a high or if $\overline{ES}$ is high when the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{IS}$) pin low, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A9-A4). The unprogrammed state of $\overline{IS}$ words are low, presenting a CLEAR with $\overline{IS}$ pin low. With all $\overline{IS}$ column words (A3-A0) programmed to the same pattern, the $\overline{IS}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{IS}$ words programmed high a PRESET function is performed.

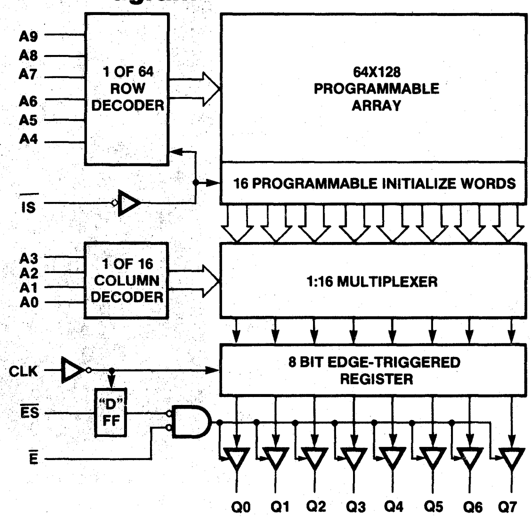
Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERFORMANCE	PINS	TYPE	MIL	COM
8K	Standard	24 (28)	NS,JS, (NL), (L),W	53RS881	63RS881
	Enhanced			53RS881A	63RS881A

Pin Configurations



Block Diagram



SKINNYDIP® is a registered trademark of Monolithic Memories

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

ings

	Operating	Programming
. . . .	−0.5 V to 7 V	12 V
. . . .	−1.5 V to 7 V	7 V
. . . .	−30 mA to +5 mA	
. . . .	−0.5 V to 5.5 V	12 V
. . . .	−65°C to +150°C	

METER	TYP†	MILITARY				COMMERCIAL				UNIT
		53RS881A		53RS881		63RS881A		63RS881		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
or low)	10	20		20		20		20		ns
ress to clock	25	40		45		30		35		ns
to clock	8	15		15		15		15		ns
o clock	20	30		35		25		30		ns
clock	−5	0		0		0		0		ns
	−3	5		5		5		5		ns
	−5	0		0		0		0		ns
	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
mperature	25	−55	125	−55	125	0	75	0	75	°C

CS Over Operating Conditions

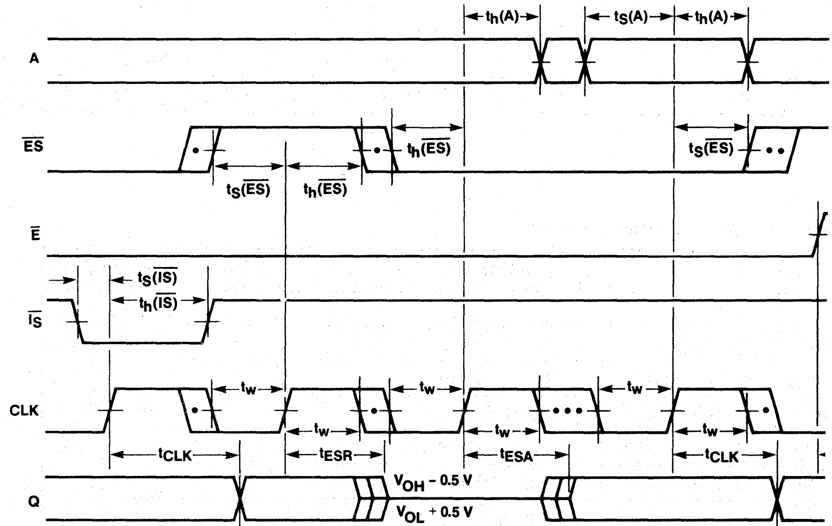
	TEST CONDITION		MIN	TYP†	MAX	UNIT
e					0.8	V
je			2			V
	V_{CC} = MIN	I_I = −18 mA			−1.2	V
t	V_{CC} = MAX	V_I = 0.4 V			−0.25	mA
nt	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
ge	V_{CC} = MIN	I_{OL} = 16 mA			0.5	V
ge	V_{CC} = MIN	MIL I_{OH} = −2 mA	2.4			V
		COM I_{OH} = −3.2 mA				
nt	V_{CC} = MAX	V_O = 0.4 V			−40	μA
		V_O = 2.4 V			40	
urrent*	V_{CC} = 5 V	V_O = 0 V	−20		−90	mA
	V_{CC} = MAX. All inputs TTL; all outputs open			130	180	mA

l at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions and using Standard Test L

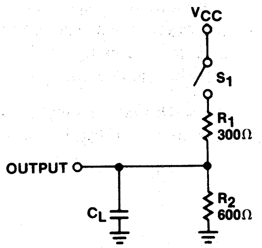
SYMBOL	PARAMETER	TYP	MILITARY			
			53RS881A		53RS881	
			MIN	MAX	MIN	MAX
t_{CLK}	Clock to output Delay	10		20		25
t_{ESA}	Clock to output access time ($\overline{ES}$)	18		30		35
t_{ESR}	Clock to output recovery time ($\overline{ES}$)	17		30		35
t_{EA}	Enable to output access time ($\overline{E}$)	18		30		35
t_{ER}	Disable to output recovery time ($\overline{E}$)	17		30		35

Definition of Waveforms

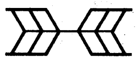


NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance impedance to "0" test.
t_{ER} and t_{EA} are measured. C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - high impedance test measured at V_{OL} + 0.5 V output level.

Switching Test Load

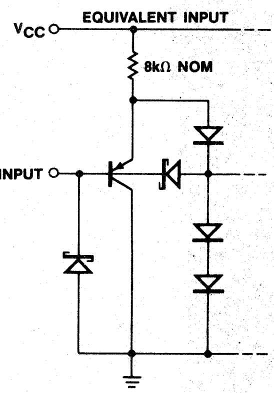


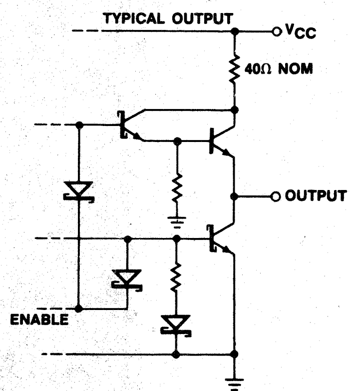
Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

3

Schematic of Inputs and Outputs





Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

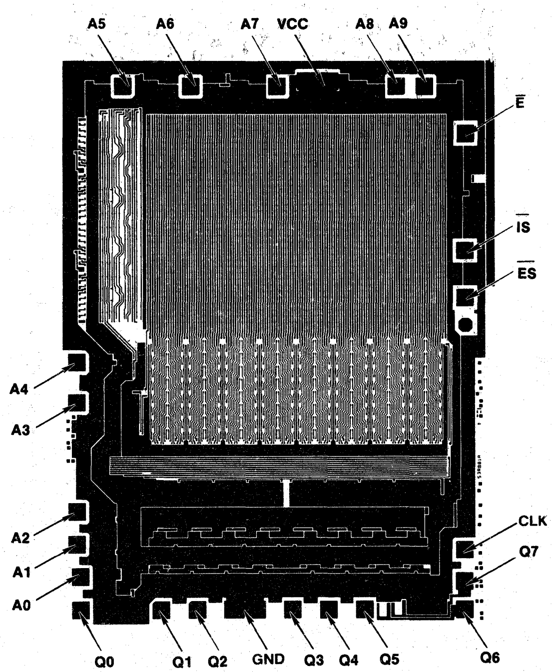
Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION	Data I/O Corp. 10525 Willows Rd. N.E. Redmond, WA 98073	Digelec Inc. 586 Weddell Dr. Suite 1 Sunnyvale, CA 94089
	Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94063	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale, CA 94089

Metal Mask Layout



2048x8 Registered PROM with Asynchronous Enable

53/63RA1681
53/63RA1681A

Features/Benefits

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM

Description

The 53/63RA1681 and 53/63RA1681A are 2Kx8 PROMs with on-chip "D"-type registers. Output enable control through an asynchronous enable input and flexible start up sequencing through programmable initialization words.

Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERFORMANCE	PINS	TYPE	MIL	COM
16K	Standard	24 (28)	NS, JS,W, (NL), (L)	53RA1681	63RA1681
	Enhanced			53RA1681A	63RA1681A

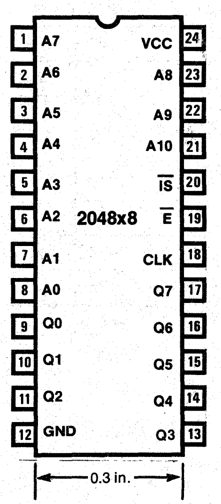
Flat-pack — contact the factory

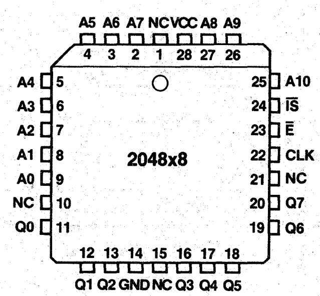
Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous enable ($\overline{E}$) is low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing.

Memory expansion and data control is made flexible with asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting $\overline{E}$ to a HIGH.

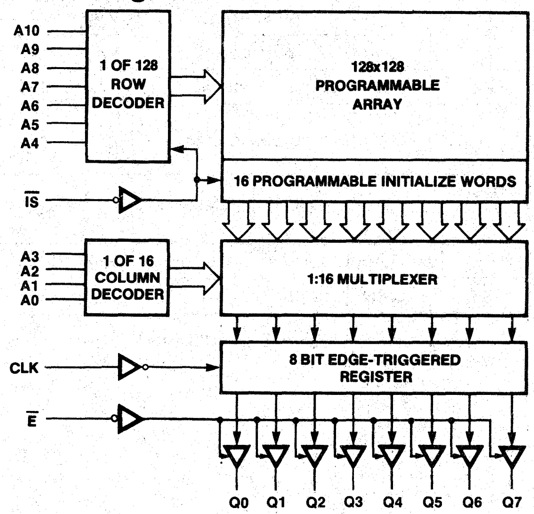
The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{IS}$) pin LOW, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A9-A4). With all $\overline{IS}$ column words (A3-A0) programmed to the same pattern, the $\overline{IS}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{IS}$ words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{IS}$ words are LOW, presenting a CLEAR with $\overline{IS}$ pin LOW.

Pin Configurations





Block Diagram



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RA1681A		53RA1681		63RA1681A		63RA1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{IS})}$	Setup time from $\overline{IS}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	−5	0		0		0		0		ns
$t_{h(\overline{IS})}$	Hold time ($\overline{IS}$)	−5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	−55	125	−55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −2 mA	2.4			V
			COM I_{OH} = −3.2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-40	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL; all outputs open			140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typical at 5.0 V V_{CC} and 25° C T_A.

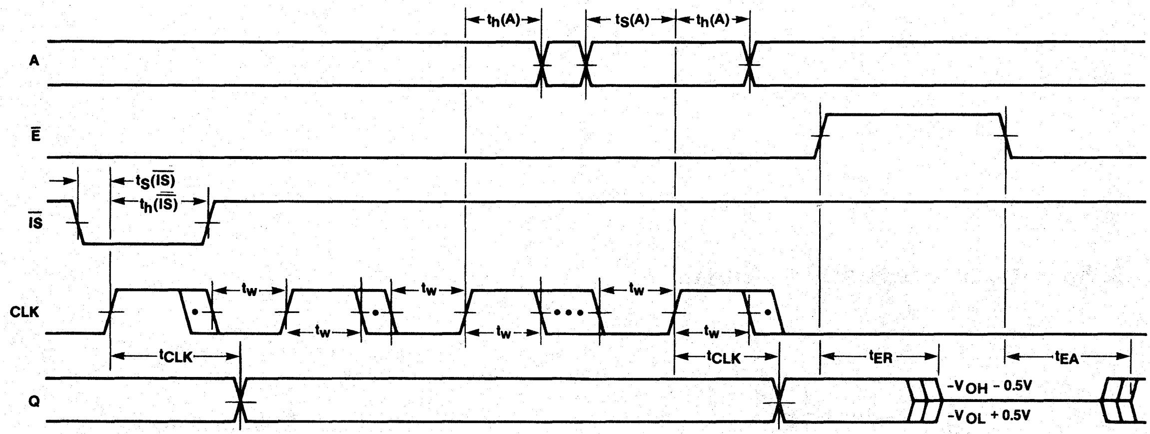
Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RA1681A		53RA1681		63RA1681A		63RA1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{EA}	Enable to output access time ($\overline{E}$)	15		30		35		25		30	ns
t_{ER}	Disable to output recovery time ($\overline{E}$)	15		30		35		25		30	ns

† Typical at 5.0 V V_{CC} and 25°C T_A.

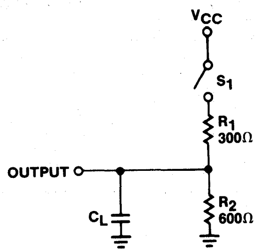
3

Definition of Waveforms

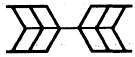


NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V output level for all tests except t_{EA} and t_{ER}.
5. t_{EA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.
t_{ER} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5 V output level.

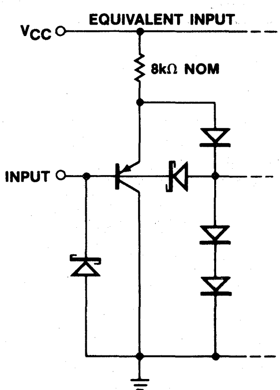
Switching Test Load

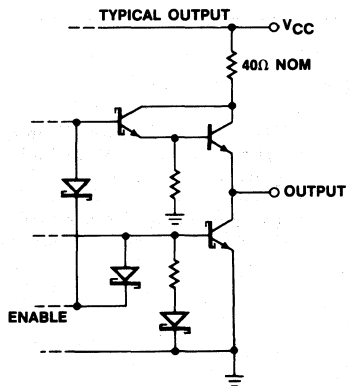


Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Schematic of Inputs and Outputs





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Remember — The best PROMs available can be made unreliable by improper programming techniques.

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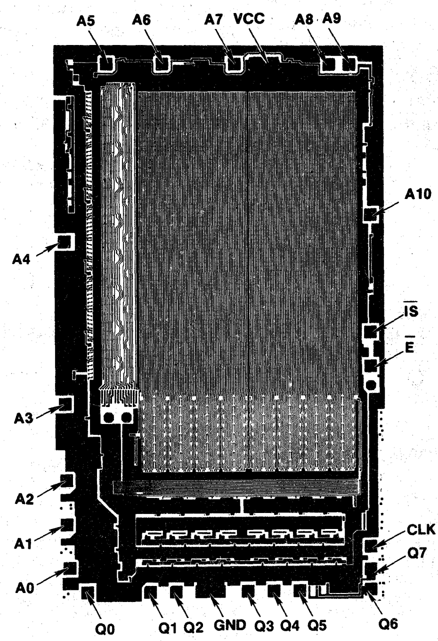
	Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94063	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale, CA 94089

3

Metal Mask Layout



2048x8 Registered PROM with Synchronous Enable

53/63RS1681 53/63RS1681A

Features/Benefits

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM

Description

The 53/63RS1681 and 53/63RS1681A are 2Kx8 PROMs with on-chip "D" type registers, versatile output enable control through synchronous enable inputs and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the synchronous ($\overline{ES}$) enable is LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous enable inputs. Outputs may be set to the high impedance state by setting $\overline{ES}$ HIGH before the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

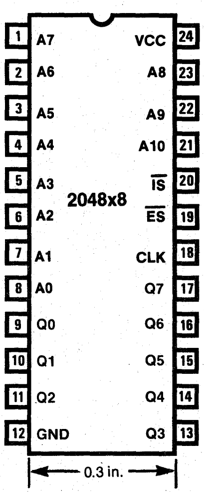
The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{IS}$) pin LOW, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A10-A4). With all $\overline{IS}$ column words (A3-A0) programmed to the same pattern, the $\overline{IS}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{IS}$ words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{IS}$ words are LOW, presenting a CLEAR with $\overline{IS}$ pin LOW.

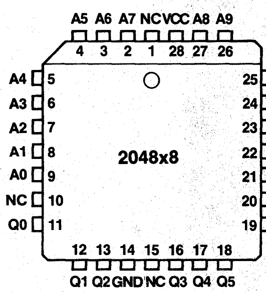
Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERFORMANCE	PINS	TYPE	MIL	COM
16K	Standard	24 (28)	NS, JS,W, (NL), (L)	53RS1681	63RS1681
	Enhanced			53RS1681A	63RS1681A

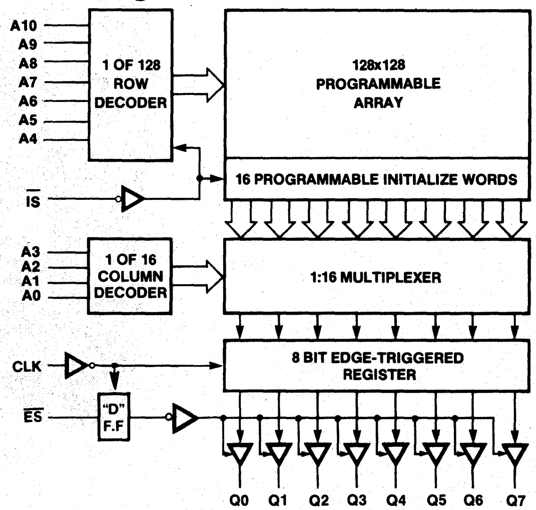
Flat-pack — contact the factory

Pin Configurations





Block Diagram



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374 Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{ES})}$	Setup time from $\overline{ES}$ to clock	7	15		15		15		15		ns
$t_{s(\overline{IS})}$	Setup time from $\overline{IS}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	−5	0		0		0		0		ns
$t_{h(\overline{ES})}$	Hold time $(\overline{ES})$	−3	5		5		5		5		ns
$t_{h(\overline{IS})}$	Hold time $(\overline{IS})$	−5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	−55	125	−55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	$V_I = V_{CC}$ MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −2 mA COM I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−40	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V			40	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL; all outputs open			140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

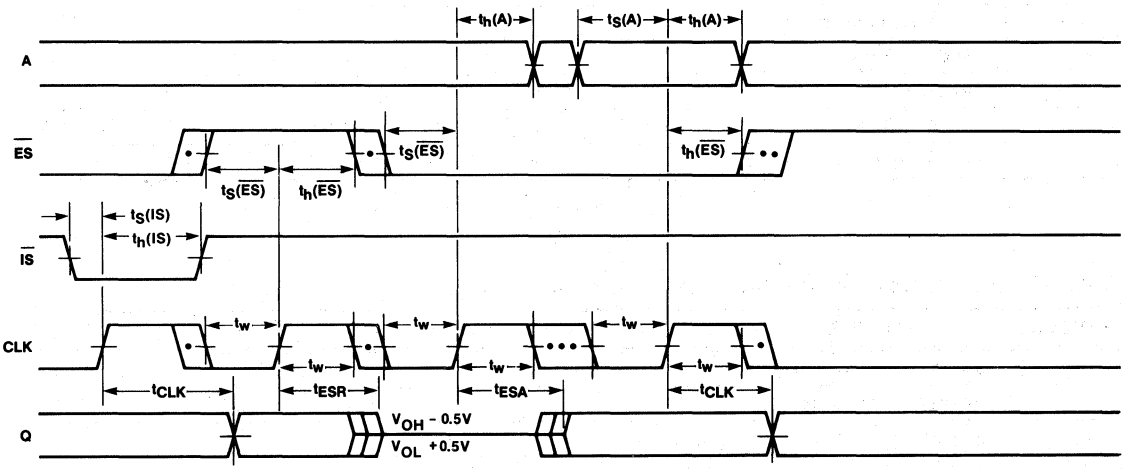
† Typical at 5.0 V V_{CC} and 25° C T_A.

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{ESA}	Clock to output access time ($\overline{ES}$)	15		30		35		25		30	ns
t_{ESR}	Clock to output recovery time ($\overline{ES}$)	15		30		35		25		30	ns

† Typical at 5.0 V V_{CC} and 25°C T_A.

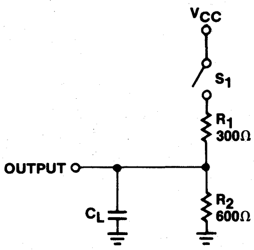
Definition of Waveforms



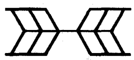
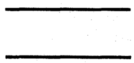
NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V output level for all tests except t_{ESA} and t_{ESR}.
5. t_{ESA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   t_{ESR} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5 V output level.

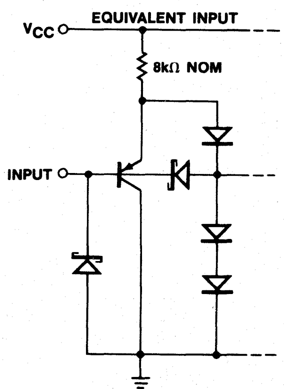
Switching Test Load

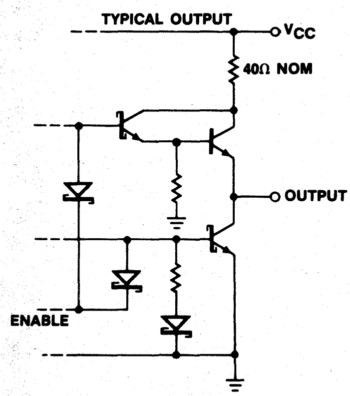


Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Schematic of Inputs and Outputs





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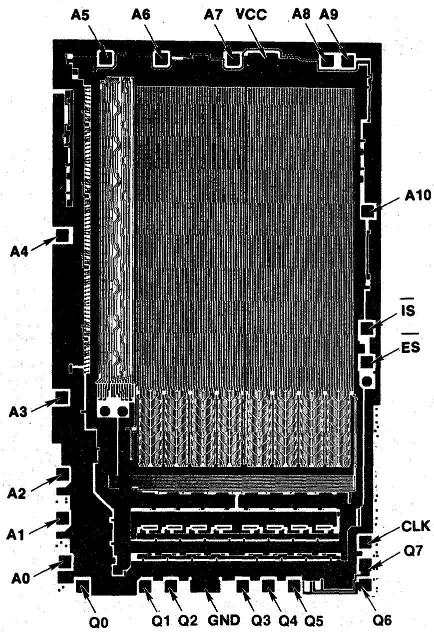
10525 Willows Rd. N.E.
Redmond, WA 98073

Kontron Electronics, Inc.
630 Price Ave.
Redwood City, CA 94063

Digelec Inc.
586 Weddell Dr. Suite 1
Sunnyvale, CA 94089

Stag Microsystems Inc.
528-5 Weddell Dr.
Sunnyvale, CA 94089

Metal Mask Layout



1024x4 Diagnostic Registered PROM

Enables and Output Initialization

53/63DA441
53/63DA442

Patent Pend.

Features/Benefits

- **Programmable asynchronous output initialization**
- **Three-state outputs with 2 enables**
- **Provides system diagnostic testing with system controllability and observability**
- **Shadow register eliminates shifting hazards**
- **Edge-triggered "D" registers simplifies system timing**
- **Cascadable for wide control words used in microprogramming**
- **24-pin SKINNYDIP® saves space**
- **24-mA output drive capability**
- **Replaces embedded diagnostic code**
- **Guaranteed programming yields of greater than 98%**

Applications

- **Microprogram control store with built-in system diagnostic testing**
- **Serial character generator**
- **Serial code converter**
- **Parallel in/serial out memory**
- **Cost-effective board testing**

Description

The 53/63DA441 and 53/63DA442 are 1Kx4 PROMs with registered outputs, programmable asynchronous initialization, 3-state outputs with 2 enables and a shadow register for diagnostic capabilities.

Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus.

During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

When exercised, the initialization input loads the output register with a user-programmable initialization word, independent of the state of CLK. This features is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt.

The distinguishing feature between the 53/63DA441 and 53/63DA442 is on the output enable structure. The 53/63DA441 has two asynchronous output enables, $\overline{E1}$ and $\overline{E2}$. Outputs will be enabled when both $\overline{E1}$ and $\overline{E2}$ are LOW. The 53/63DA442 has one asynchronous output enable $\overline{E}$ and one synchronous output enable $\overline{ES}$. Outputs will be enabled if $\overline{ES}$ is LOW during the last rising edge of CLK and $\overline{E}$ is LOW.

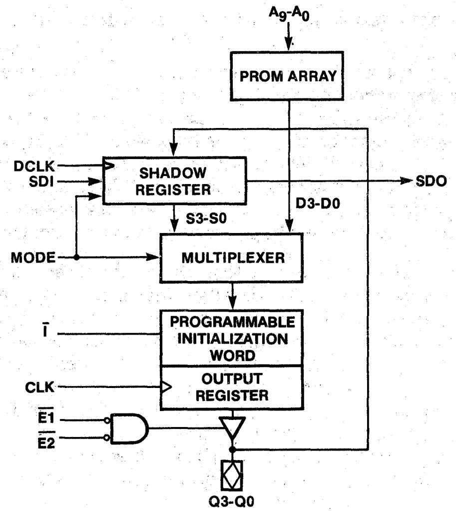
Selection Guide

MEMORY			PACKAGE		PART NUMBER	
SIZE	ORGANIZATION	OPTIONS	PINS	TYPE	MILITARY	COMMERCIAL
4 K	1024 x 4	Two asynchronous enables	24 (28)	NS,JS,W, (NL),(L)	53DA441	63DA441
		One synchronous enable, one asynchronous enable			53DA442	63DA442

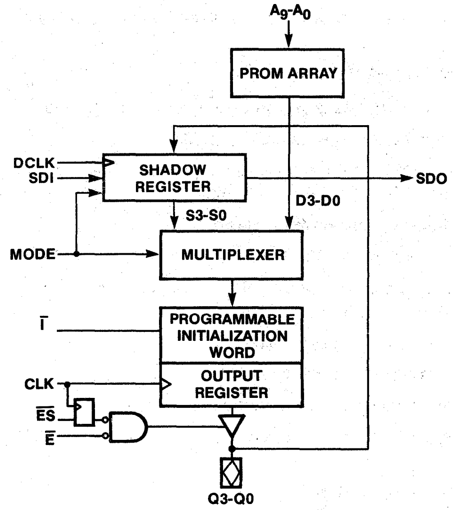
SKINNYDIP® is a registered trademark of Monolithic Memories

Block Diagrams

53/63DA441

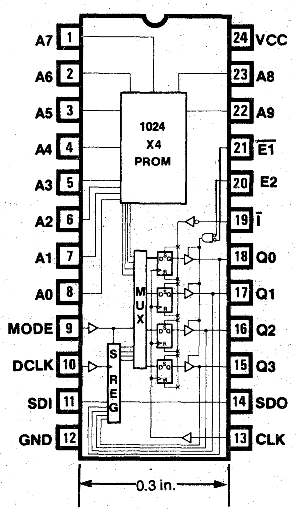


53/63DA442

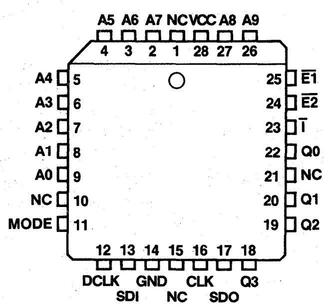


Logic Symbols

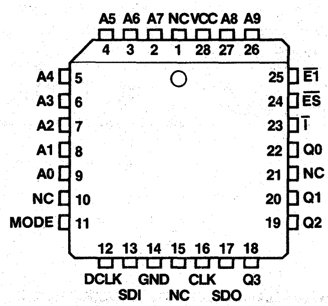
53/63DA441



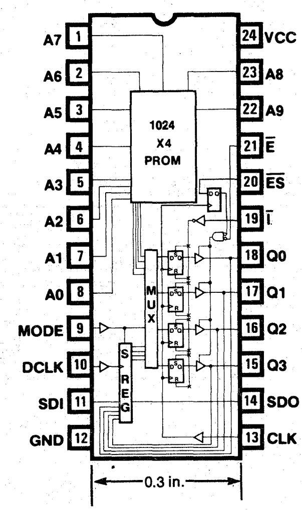
53/63DA441



53/63DA442



53/63DA442



Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation†

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Definition of Signals

MODE The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI The Serial Data In pin is the input to the least-significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK The clock pin loads the output register on the rising edge of CLK.

DCLK The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 Qn represents the data outputs of the output register. During a shadow register load with outputs enabled, these pins are the internal data inputs to the shadow register. With the outputs three-stated, these pins are external data inputs to the shadow register.

S3-S0 Sn represents the internal shadow register outputs.

A9-A0 An represents the address inputs to the PROM array.

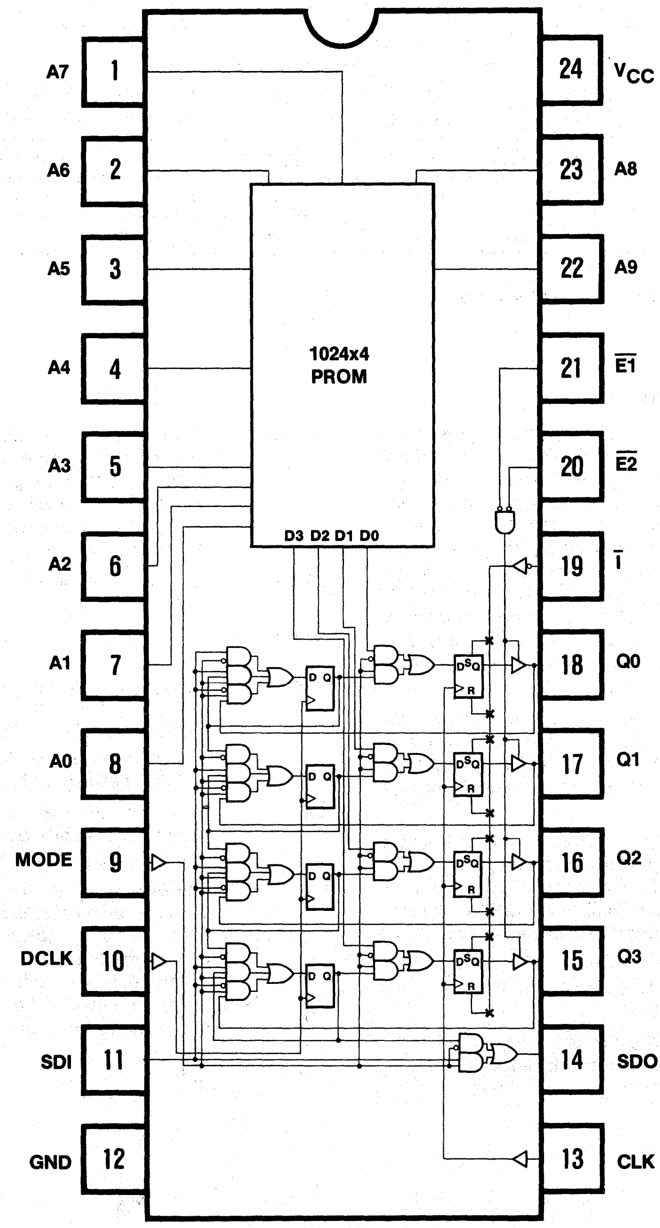
$\overline{E1}$, $\overline{E2}$, $\overline{E}$ These Output Enable pin(s) operate independent of CLK. For 'D441, outputs are enabled if, and only if, both $\overline{E1}$ and $\overline{E2}$ are LOW. For 'D442, outputs are enabled only when $\overline{ES}$ is LOW at the last rising edge of CLK and $\overline{E}$ is LOW.

$\overline{ES}$ Synchronous Output Enable for 'DA442 only. Outputs are enabled only when $\overline{ES}$ is LOW at the last rising edge of CLK and $\overline{E}$ is LOW.

$\overline{I}$ The asynchronous output register initialization input pin operates independent of CLK. When $\overline{I}$ is LOW, the output register is loaded with a user-programmable initialization word. Programmable initialization is a super set of preset and clear functions, and can be used to generate any microinstruction system reset or interrupt.

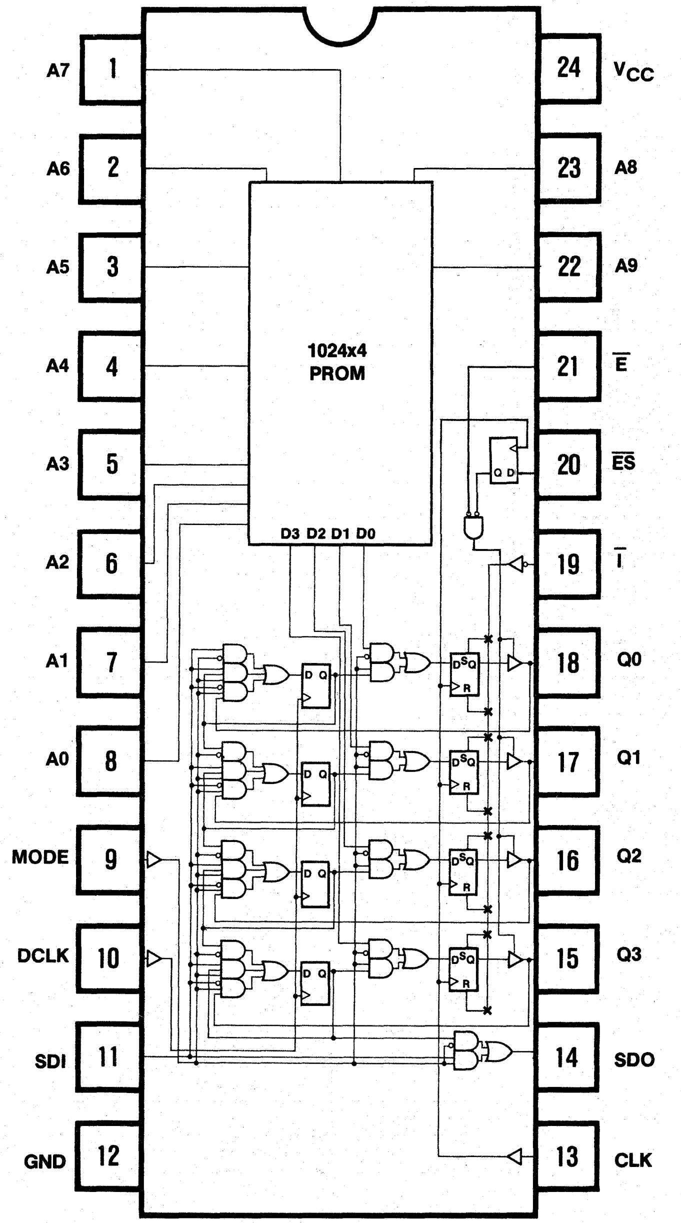
Logic Diagram

53/63DA441
1024x4 Diagnostic PROM with Asynchronous Initialization and Asynchronous Enables



Logic Diagram

53/63DA442
1024x4 Diagnostic PROM
with Asynchronous Initialization
and Both Asynchronous and Synchronous Enables



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150° C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Setup time from address to CLK	45	25		35	25		ns
t_h	Hold time for CLK	0	−15		0	−15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	35	15		25	15		ns
t_{sud}	Setup time from control inputs (SDI, MODE) to CLK, DCLK	50	20		40	20		ns
t_{hd}	Hold time for DCLK	0	−5		0	−5		ns
$t_s(\overline{ES})$	Setup time from $\overline{ES}$ to CLK ('DA442 only)	20	10		15	10		ns
$t_h(\overline{ES})$	Hold time ($\overline{ES}$) ('DA442 only)	5	0		5	0		ns
t_{iw}	Initialization pulse width (LOW)	25	10		20	10		ns
t_{ir}	Initialization recovery time	45	30		40	30		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL I_{OL} = 16 mA COM I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −2 mA COM I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V			40	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All outputs open. All inputs TTL.			130	180	mA

† Typical at 5.0 V V_{CC} and 25° C T_A.

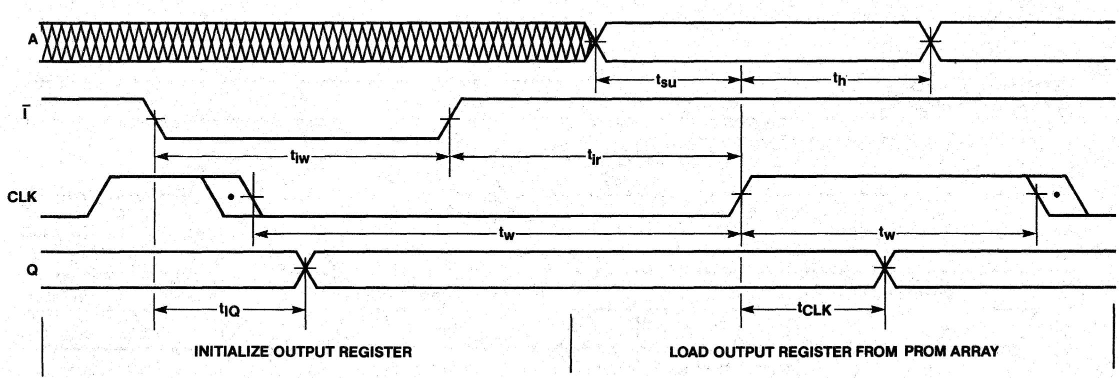
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

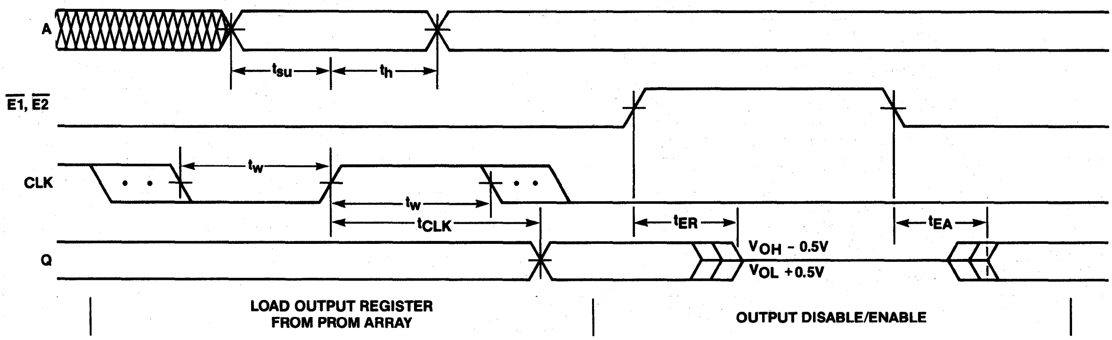
SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		11	25		11	18	ns
t_{ER}	Disable time		14	30		14	25	ns
t_{EA}	Enable time		16	30		16	25	ns
t_{MAXD}	Maximum diagnostic clock frequency	7	20		10	20		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		17	35		17	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns
t_{IQ}	Initialization to output delay		22	35		22	30	ns
t_{ESR}	CLK to output disable time ('DA442 only)		22	35		22	30	ns
t_{ESA}	CLK to output enable time ('DA442 only)		15	35		15	30	ns

† Typical at 5.0 V V_{CC} and 25° C T_A

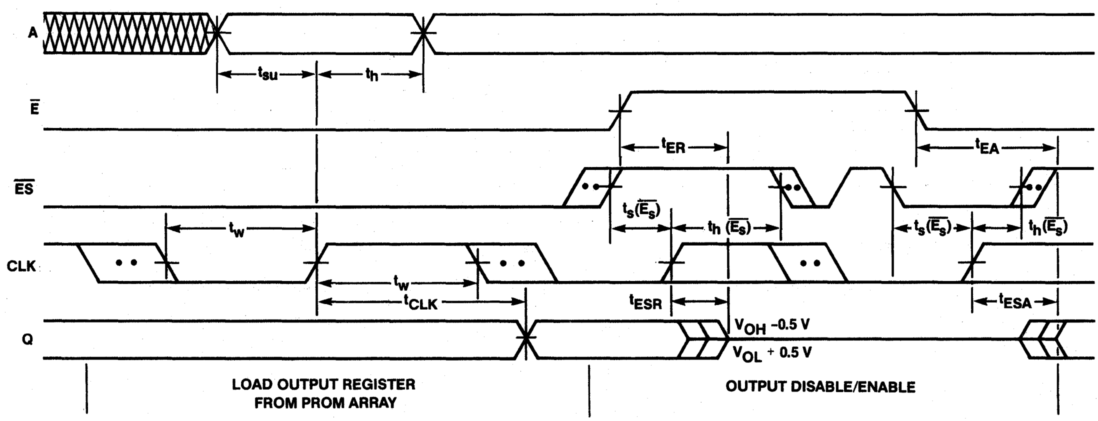
Definition of Waveforms



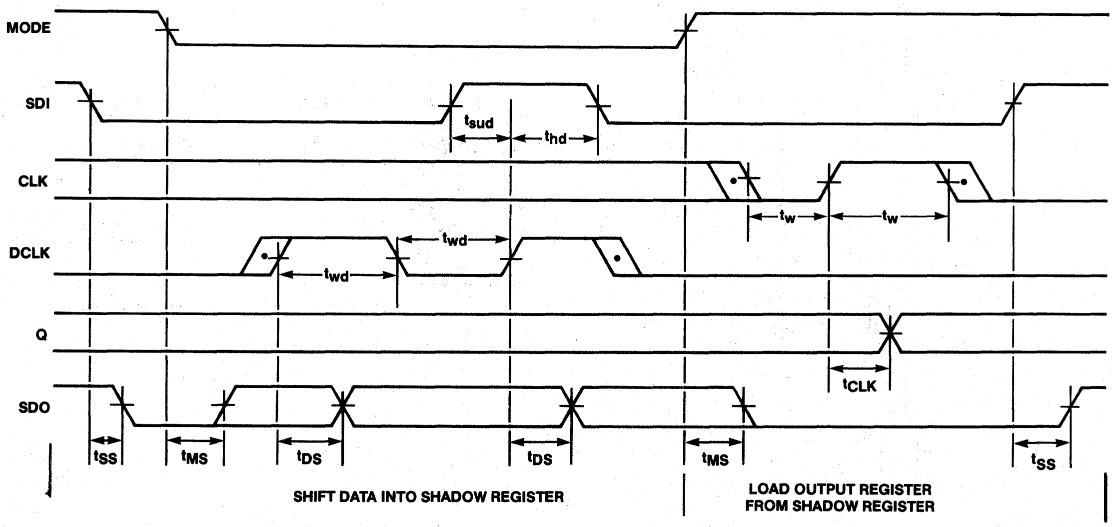
Normal PROM Operation (Mode = LOW)
(for both 53/63DA441 and 53/63DA442 with outputs enabled)



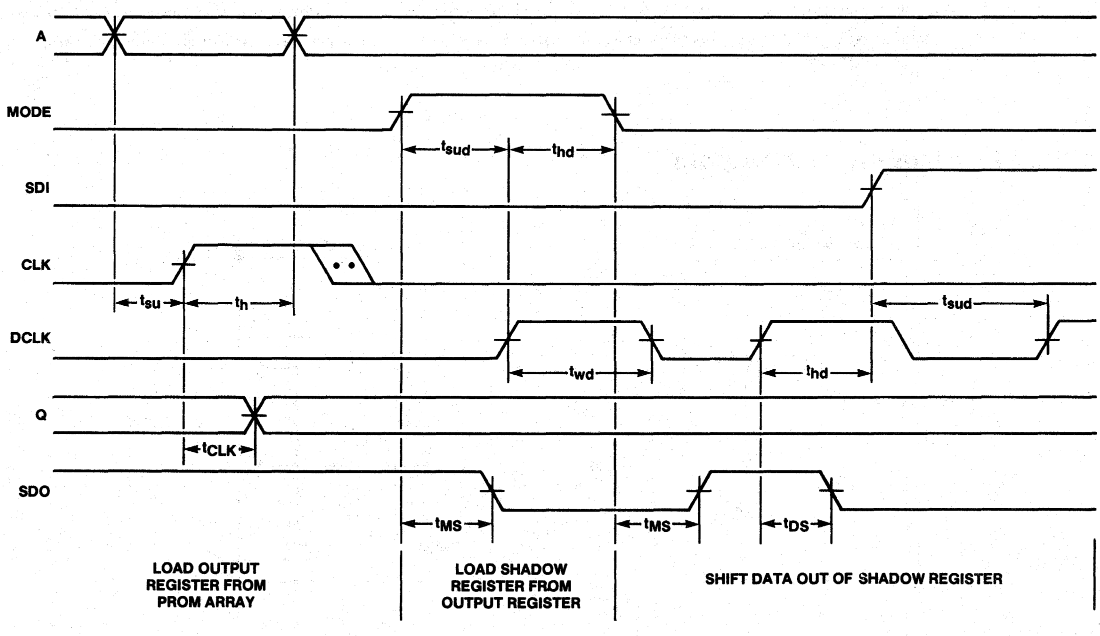
Normal PROM Operation (Mode = LOW)
(for 53/63DA441 only with $\overline{T}$ = HIGH)



Normal PROM Operation (Mode = LOW)
(for 53/63DA442 only with $\overline{T}$ = HIGH)

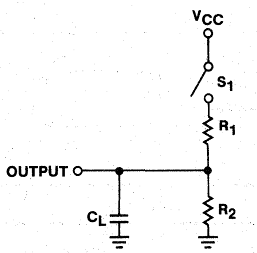


SYSTEM CONTROL

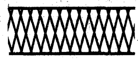
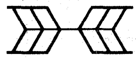
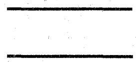


SYSTEM OBSERVATION

Switching Test Load



Definition of Timing Diagram

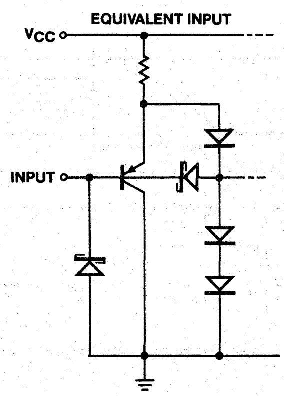
WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

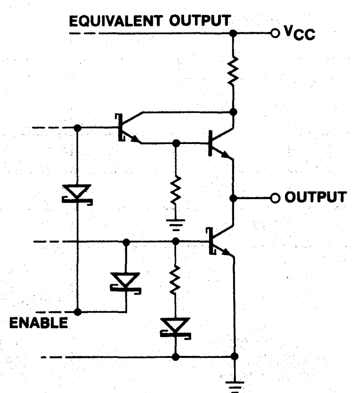
NOTES: 1. For commercial operating range $R_1 = 200\Omega$, $R_2 = 390\Omega$. For military operating range $R_1 = 300\Omega$, $R_2 = 600\Omega$.

2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
4. Input access measured at the 1.5 V level.
5. Data delay is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
6. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" to test and closed for high-impedance to "0" test.

   t_{ER} and t_{ESR} are measured C_L = 5 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} +0.5 V output level.

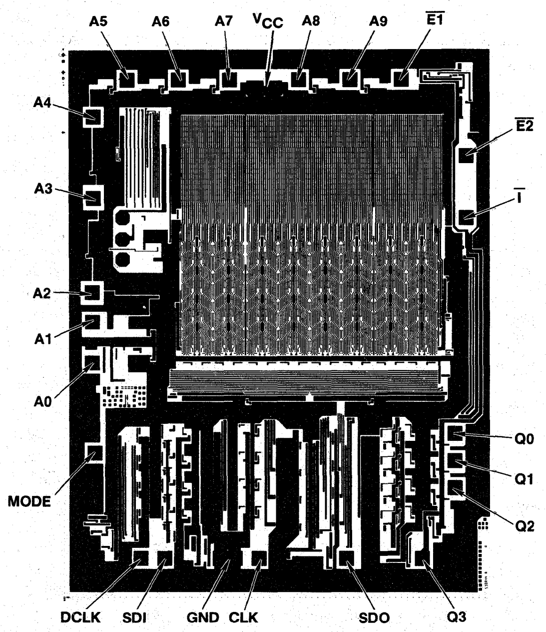
Schematic of Inputs and Outputs



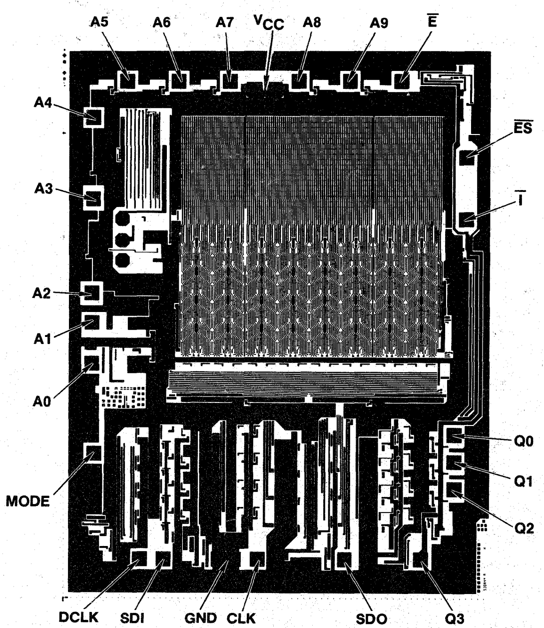


Die Configurations

53/63DA441



53/63DA442



3

Commercial Programmers

Monolithic Memories' PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION	Data I/O Corp. 10525 Willows Rd. N.E. C-46 Redmond, WA 98052	Digelec Inc. 7335 E. Acoma Dr. Suite 103 Scottsdale, AZ 85260
	Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94036	Stag Systems Inc. 1120 San Antonio Rd. Palo Alto, CA 94303

2048x4 Diagnostic Registered PROM

53DA841 63DA841

with Asynchronous Enable and Output Initialization

Patent Pend.

Features/Benefits

- **Asynchronous output enable**
- **Programmable asynchronous output initialization**
- **Provides system diagnostic testing with system controllability and observability**
- **Shadow register eliminates shifting hazards**
- **Edge-triggered "D" registers simplifies system timing**
- **Cascadable for wide control words used in microprogramming**
- **24-pin SKINNYDIP® saves space**
- **Ti-W fusible link technology guarantees greater than 98% programming yield**
- **24-mA output drive capability**
- **Replaces embedded diagnostic code**

Applications

- **Microprogram control store with built-in system diagnostic testing**
- **Serial character generator**
- **Serial code converter**
- **Parallel in/serial out memory**
- **Cost-effective board testing**

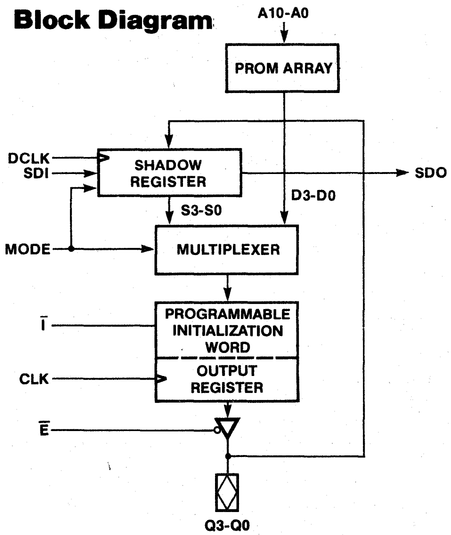
Description

The 53/63DA841 is a 2Kx4 PROM with registered three-state outputs, programmable asynchronous initialization and a shadow register for diagnostic capabilities. Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming. When exercised, the Initialization input loads the register with a user-programmable initialization word, independent of the state of CLK. This feature is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt.

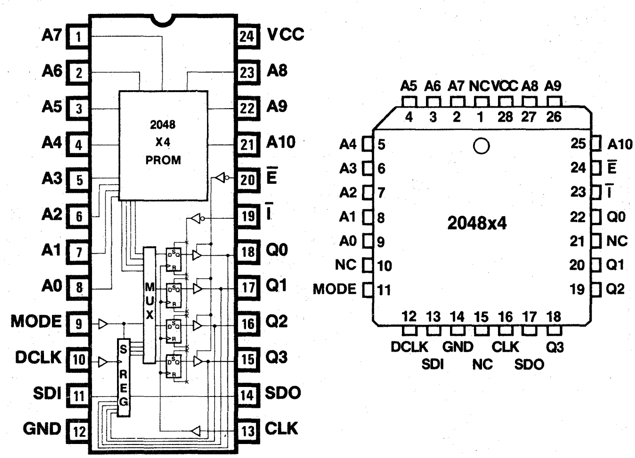
Ordering Information

MEMORY		TEMP.	PACKAGE		PART NO.
SIZE	ORG.		PINS	TYPE	
8K	2048x4	Com	24 (28)	NS,JS,W, (NL),(L)	63DA841
		Mil			53DA841

Block Diagram



Pin Configurations



Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation †

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Definition of Signals

MODE — The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output register. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI — The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO — The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK — The clock pin loads the output register on the rising edge of CLK.

DCLK — The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 — Qn represents the data outputs of the output register. During a shadow register load these pins are the internal data inputs to the shadow register.

S3-S0 — Sn represents the internal shadow register outputs.

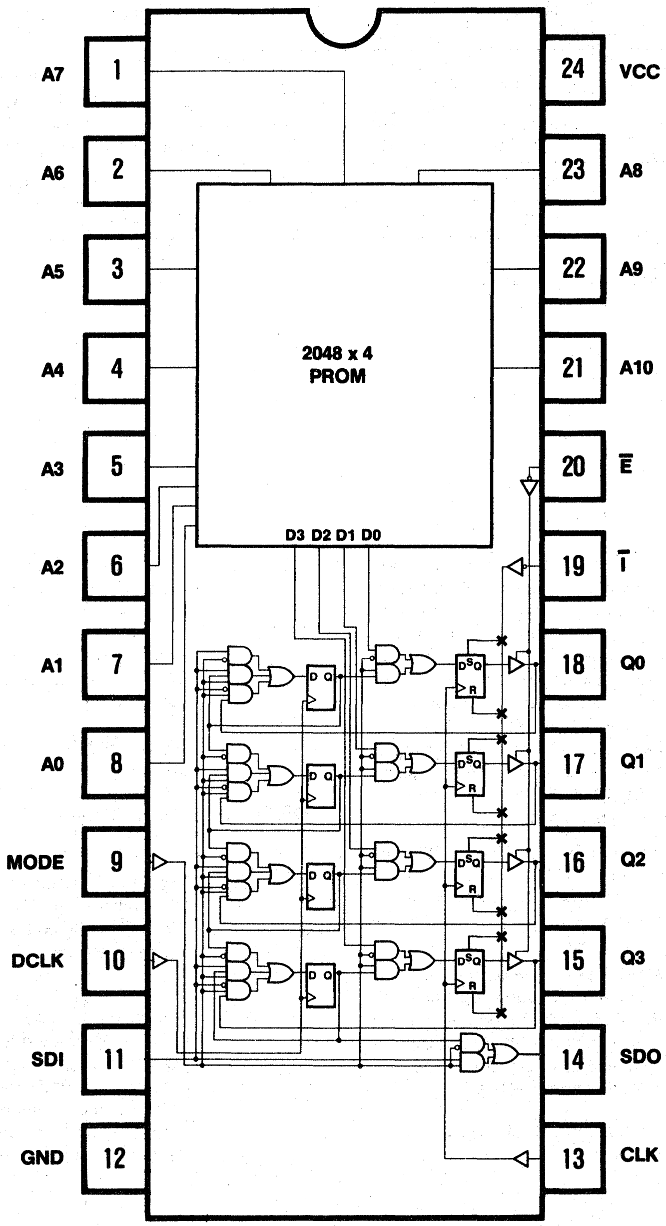
A10-A0 — An represents the address inputs to the PROM array.

$\overline{E}$ — The Output Enable pin operates independent of CLK. When $\overline{E}$ is LOW the outputs are enabled. When $\overline{E}$ is HIGH, the outputs are in the high-impedance state.

$\overline{I}$ — The asynchronous output register initialization input pin operates independent of CLK. When $\overline{I}$ is LOW, the output register is loaded with a user-programmable initialization word. Programmable initialization is a super-set of preset and clear functions, and can be used to generate any microinstruction for system reset or interrupt.

Logic Diagram

2048 x 4 Diagnostic PROM with Asynchronous Enable and Output Initialization



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	TYP†	MAX	COMMERCIAL MIN	TYP†	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Set up time from address to CLK	45	27		40	27		ns
t_h	Hold time for CLK	0	−15		0	−15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
t_{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20		45	20		ns
t_{hd}	Hold time for DCLK	0	−5		0	−5		ns
t_{iw}	Initialization pulse width (LOW)	25	10		20	10		ns
t_{ir}	Initialization recovery time	45	30		40	30		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	$V_I = V_{CC}$			40	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil I_{OL} = 16 mA Com I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil I_{OH} = −2 mA Com I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	µA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V			40	µA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V	−20		−90	mA
I_{CC}	Supply Current	V_{CC} = MAX. All inputs TTL. All outputs open			140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

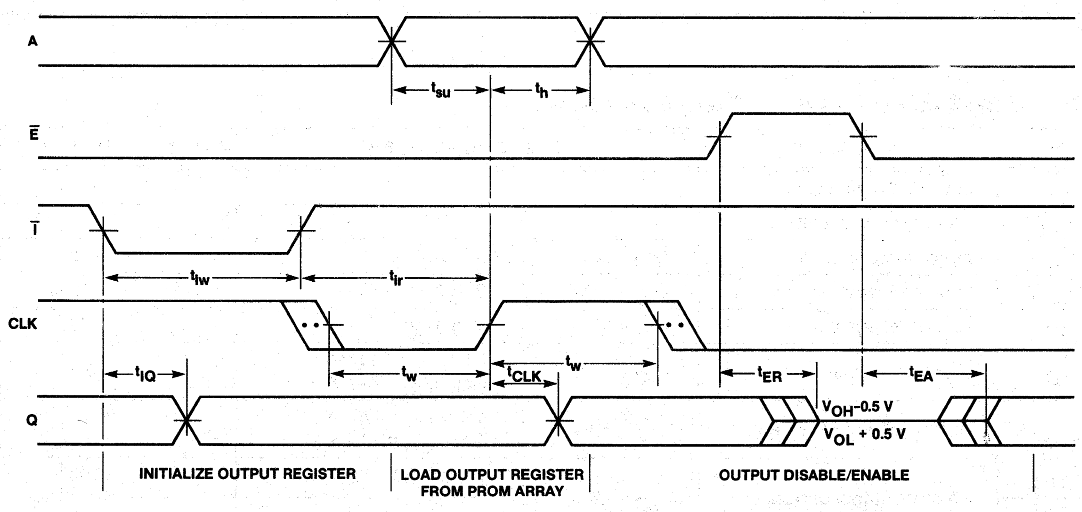
† Typical at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

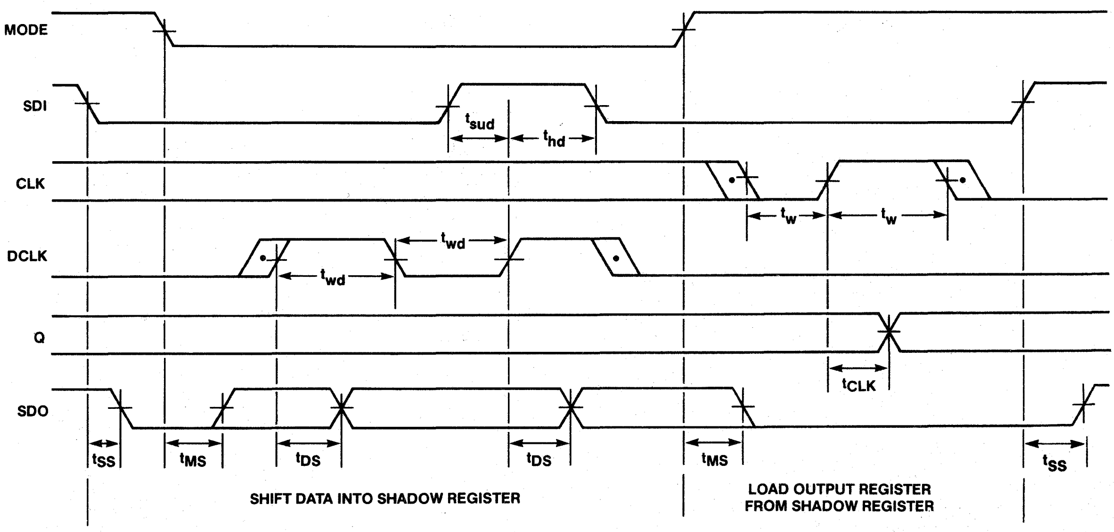
SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		13	25		13	20	ns
t_{ER}	Enable time		16	30		16	25	ns
t_{EA}	Disable time		16	30		16	25	ns
t_{IQ}	Initialization to output delay		23	40		23	35	ns
f_{MAXD}	Maximum diagnostic clock frequency	7	18		10	18		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		19	35		19	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns

† Typical at 5.0 V V_{CC} and 25°C T_A.

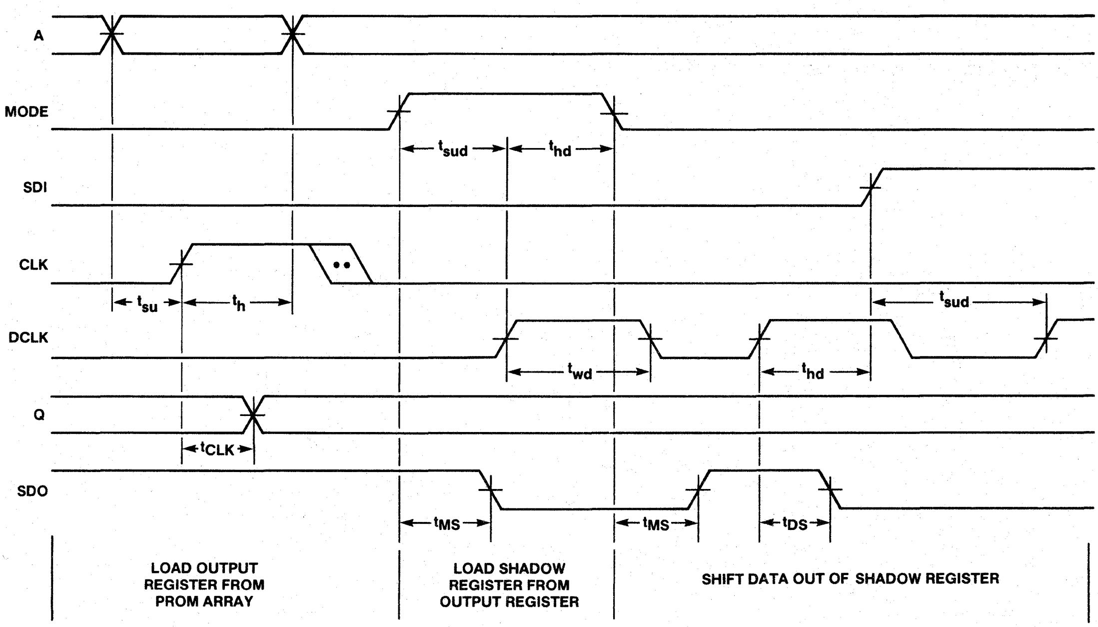
Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)

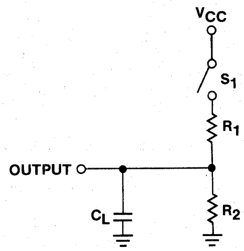


SYSTEM CONTROL

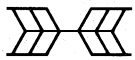
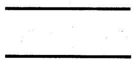


SYSTEM OBSERVATION

Switching Test Load

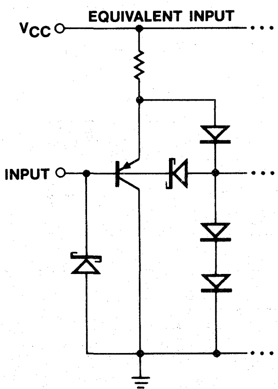


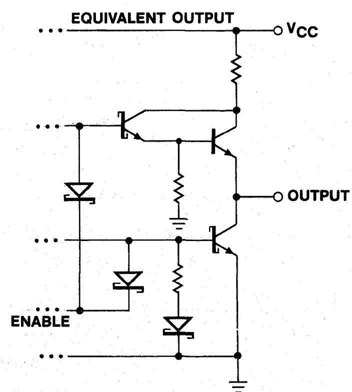
Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

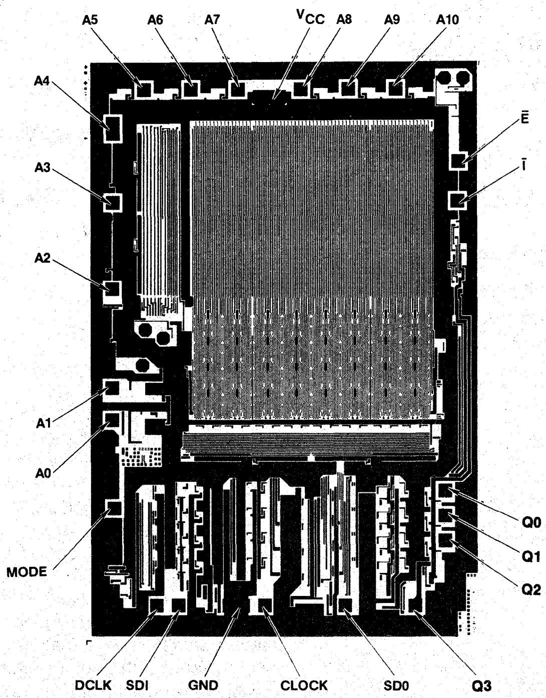
NOTES:
1. For commercial operating range $R_1 = 200\Omega$ $R_2 = 390\Omega$.
   For military operating range $R_1 = 300\Omega$ $R_2 = 600\Omega$.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
4. Input access measured at the 1.5 V level.
5. Data delay is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
6. t_{EA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.
   t_{ER} is measured C_L = 5pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} +0.5 V output level.

Schematic of Inputs and Outputs





Metal Mask Layout



3

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltage must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

MANUFACTURER	PROGRAMMER TYPE	PROGRAMMING MODULE	SOCKET CONFIGURATION
Data I/O*	Unipack Rev V07 Unipack 2 Rev V05	Family Code AA	Pinout Code AD

* Use socket adapter 351A-073 Rev. A.

4096x4 Diagnostic Registered PROM
Asynchronous Enable

53D1641
63D1641

Patent Pend.

Features/Benefits

- **Asynchronous output enable**
- **Provides system diagnostic testing for system controllability and observability**
- **Shadow register eliminates shifting hazards**
- **Edge-triggered "D" registers simplifies system timing**
- **Casadable for wide control words used in microprogramming**
- **24-pin SKINNYDIP® saves space**
- **24-mA output drive capability**
- **Replaces embedded diagnostic code**

Applications

- **Microprogram control store with built-in system diagnostic testing**
- **Serial character generator**
- **Serial code converter**
- **Parallel in/serial out memory**
- **Cost-effective board testing**

Description

The 53/63D1641 is a 4Kx4 PROM with registered three-state outputs and a shadow register for diagnostic capabilities.

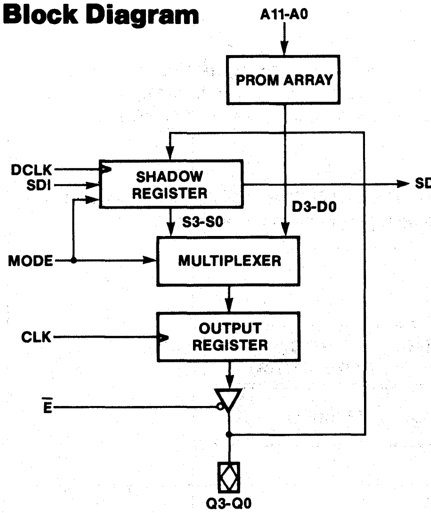
Ordering Information

MEMORY SIZE	MEMORY ORG.	TEMP.	PACKAGE PINS	PACKAGE TYPE	PART NO.
16K	4096x4	Mil	24 (28)	NS,JS,W, (NL),(L)	53D1641
		Com			63D1641

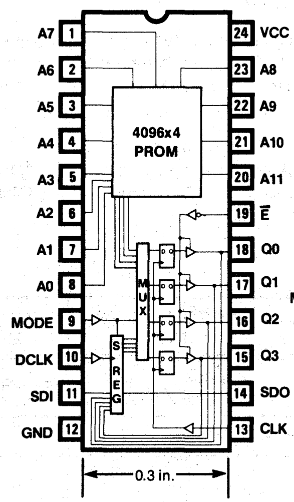
Flat-pack — contact the factory

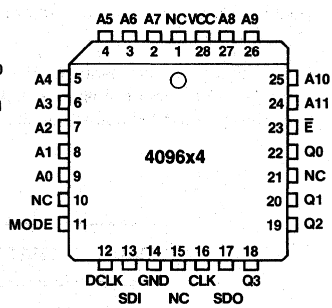
Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register, is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independent of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

Block Diagram



Pin Configurations





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Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation†

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Definition of Signals

MODE The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK The CLOCK pin loads the output register on the rising edge of CLK.

DCLK The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 Qn represents the data outputs of the output register. During a shadow register load with outputs enabled these pins are the internal data inputs to the shadow register. With the outputs three-stated these pins are external data inputs to the shadow register.

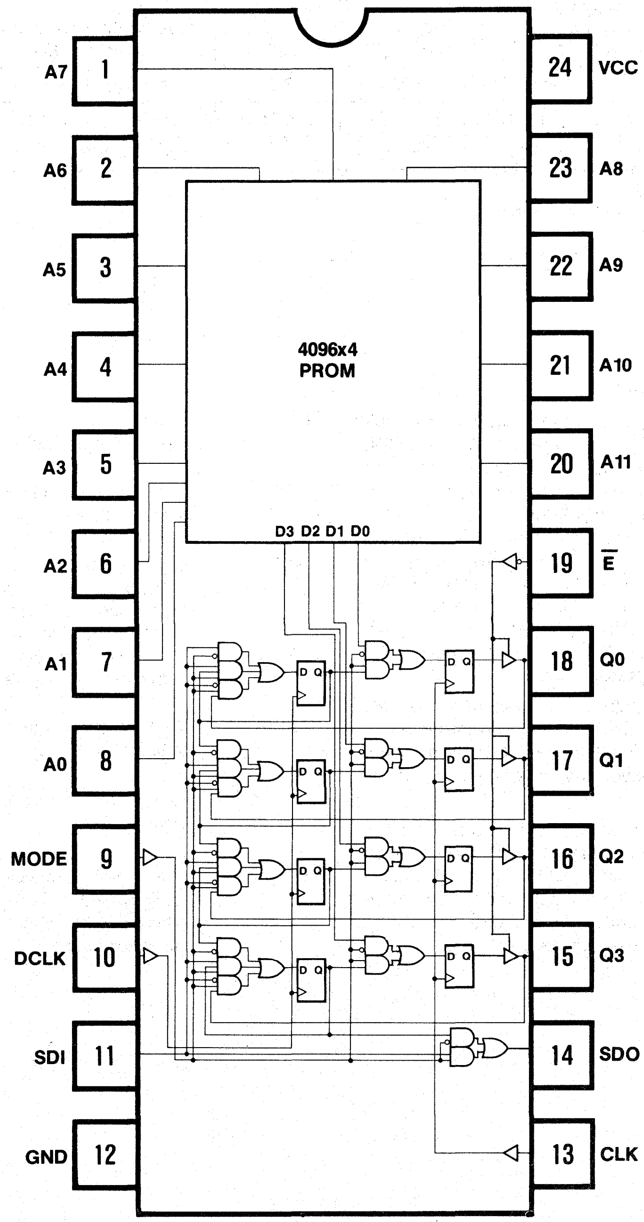
S3-S0 Sn represents the internal shadow register outputs.

A11-A0 An represents the address inputs to the PROM array.

$\overline{E}$ The Output Enable pin operates independent of CLK. When $\overline{E}$ is LOW the outputs are enabled. When $\overline{E}$ is HIGH, the outputs are in the high impedance state.

Logic Diagram

4096x4 Diagnostic PROM with Asynchronous Enable



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input Current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	-55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Set up time from address to CLK	45	25		40	25		ns
t_h	Hold time for CLK	0	-15		0	-15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
t_{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20		45	20		ns
t_{hd}	Hold time for DCLK	0	-5		0	-5		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL I_{OL} = 16 mA COM I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −2 mA COM I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-100	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V			40	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL; all outputs open			140	190	mA

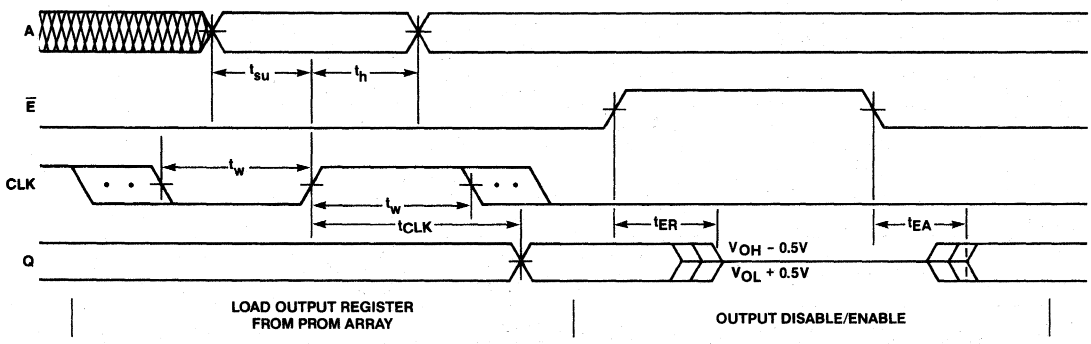
† Typical at 5.0 V V_{CC} and 25°C T_A.
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

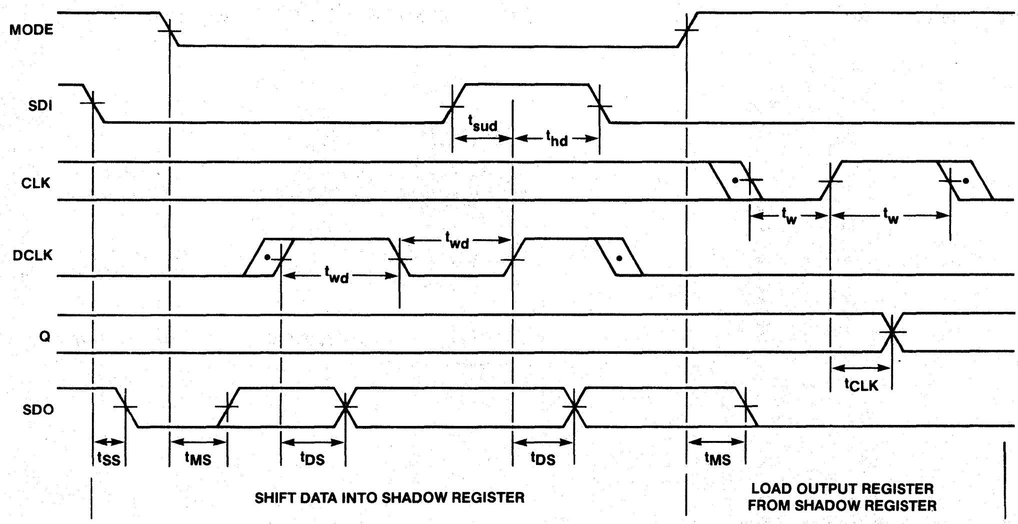
SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		11	25		11	20	ns
t_{ER}	Disable time		16	30		16	25	ns
t_{EA}	Enable time		16	30		16	25	ns
f_{MAXD}	Maximum diagnostic clock frequency	7	18		10	18		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		17	35		17	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns

† Typical at 5.0 V V_{CC} and 25° C T_A.

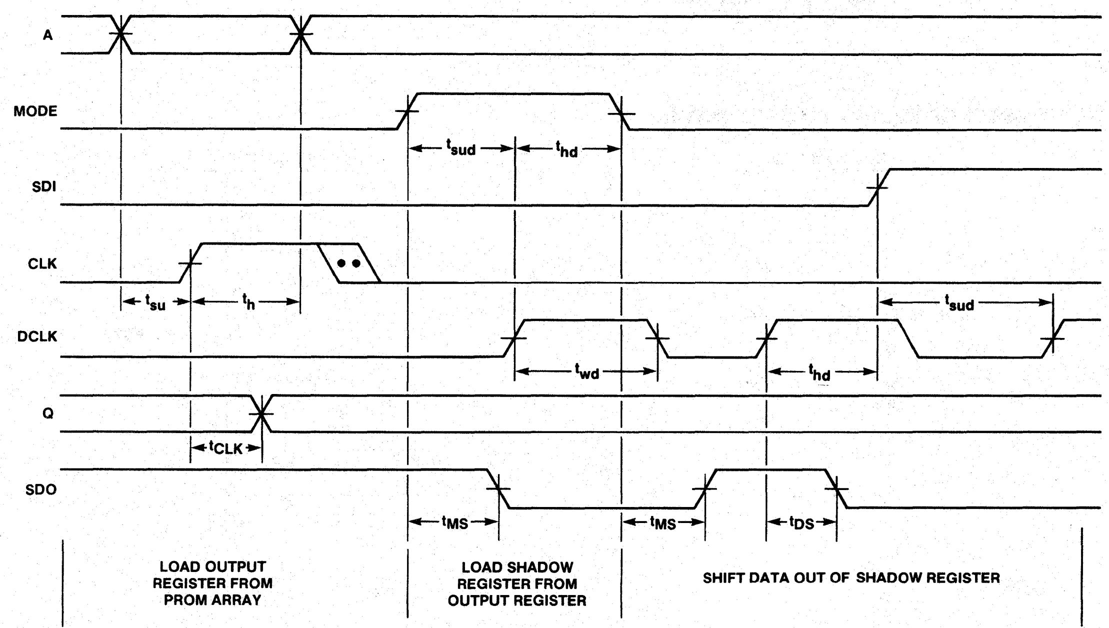
Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)

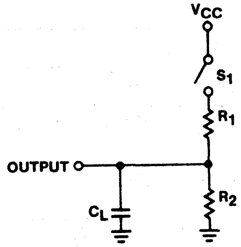


SYSTEM CONTROL

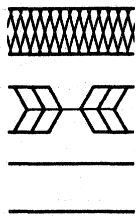


SYSTEM OBSERVATION

Switching Test Load



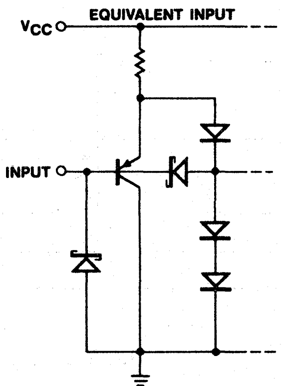
Definition of Timing Diagram

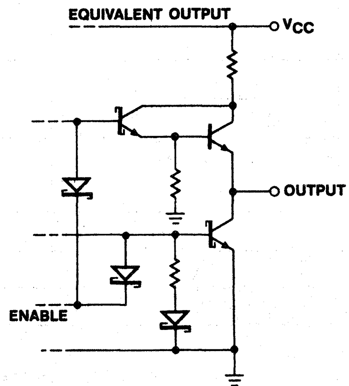


WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

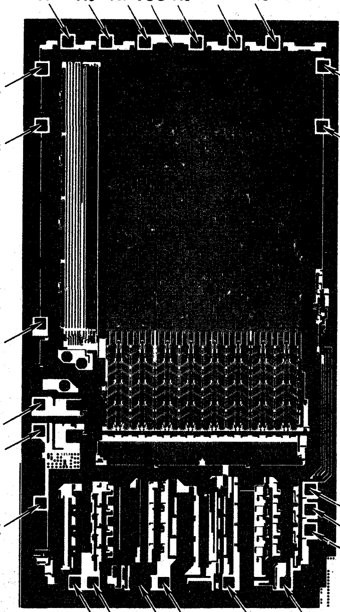
NOTES: 1. For commercial operating range $R_1 = 200\Omega$, $R_2 = 390\Omega$.
For military operating range $R_1 = 300\Omega$, $R_2 = 600\Omega$.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
4. Input access measured at the 1.5 V level.
5. Data delay is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
6. t_{EA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.
t_{ER} is measured with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5 V output level.

Schematic of Inputs and Outputs





Die Configuration



Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltage must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

MANUFACTURER	PROGRAMMER TYPE	PROGRAMMING MODULE	SOCKET CONFIGURATION
Data I/O	Unipack Rev-V07 Unipack2 Rev-V05	Family Code B2	Pinout Code 80

4096x4 Diagnostic Registered PROM

Output Initialization

53DA1643
63DA1643

Patent Pend.

Features/Benefits

- **Programmable asynchronous output initialization**
- **Provides system diagnostic testing with system controllability and observability**
- **Shadow register eliminates shifting hazards**
- **Edge-triggered "D" registers simplifies system timing**
- **Cascadable for wide control words used in microprogramming**
- **24-pin SKINNYDIP® saves space**
- **24-mA output drive capability**
- **Replaces embedded diagnostic code**

Applications

- **Microprogram control store with built-in system diagnostic testing**
- **Serial character generator**
- **Serial code converter**
- **Parallel in/serial out memory**
- **Cost-effective board testing**

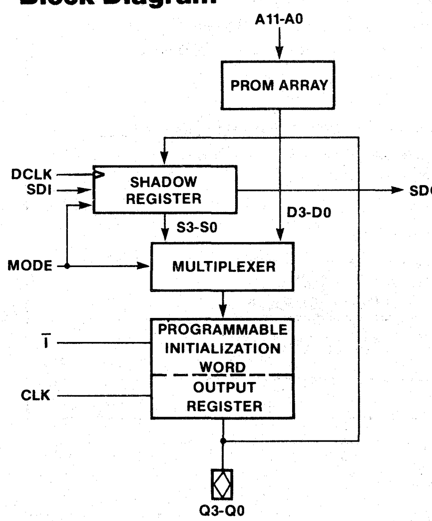
Description

The 53/63DA1643 is a 4Kx4 PROM with registered outputs, programmable asynchronous initialization, and a shadow register for diagnostic capabilities. Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming. When exercised, the Initialization input loads the output register with a user-programmable initialization word, independent of the state of CLK. This feature is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt

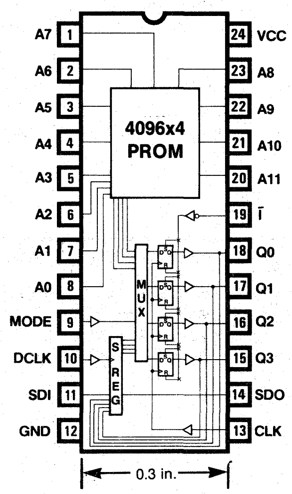
Ordering Information

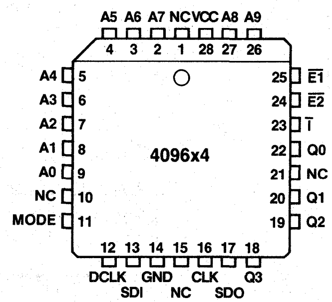
MEMORY		TEMP.	PACKAGE		PART NO.
SIZE	ORG.		PINS	TYPE	
16K	4096x4	Mil	24 (28)	NS,JS,W, (NL),(L)	53DA1643
		Com			63DA1643

Block Diagram



Pin Configurations





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Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation†

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Definition of Signals

MODE — The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output register. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI — The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO — The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK — The clock pin loads the output register on the rising edge of CLK.

DCLK — The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 — Qn represents the data outputs of the output register. During a shadow register load these pins are the internal data inputs to the shadow register.

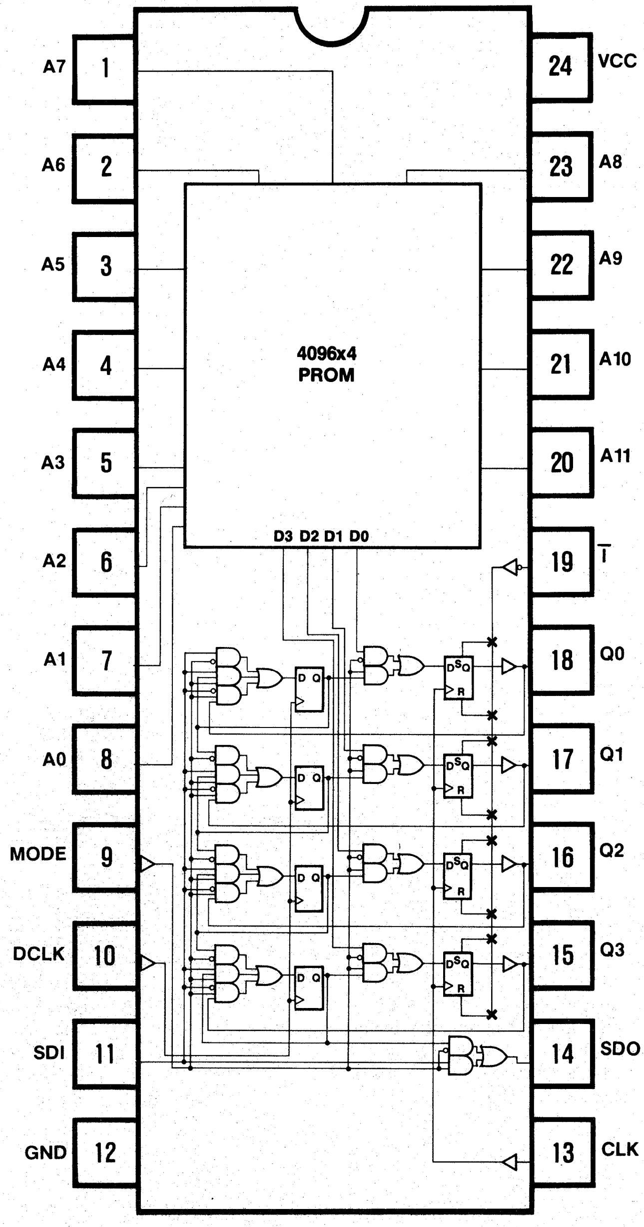
S3-S0 — Sn represents the internal shadow register outputs.

A11-A0 — An represents the address inputs to the PROM array.

$\overline{I}$ — The asynchronous output register initialization input pin operates independent of CLK. When $\overline{I}$ is LOW, the output register is loaded with a user programmable initialization word. Programmable initialization is a super set of preset and clear functions, and can be used to generate any microinstruction for system reset or interrupt.

Logic Diagram

4096x4 Diagnostic PROM with Asynchronous Initialization



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150° C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Set up time from address to CLK	45	25		40	25		ns
t_h	Hold time for CLK	0	-15		0	-15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
t_{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20		45	20		ns
t_{hd}	Hold time for DCLK	0	-5		0	-5		ns
t_{iw}	Initialization pulse width (LOW)	25	10		20	10		ns
t_{ir}	Initialization recovery time	45	25		40	25		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL I_{OL} = 16 mA COM I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −2 mA COM I_{OH} = −3.2 mA	2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL; all outputs open			140	190	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

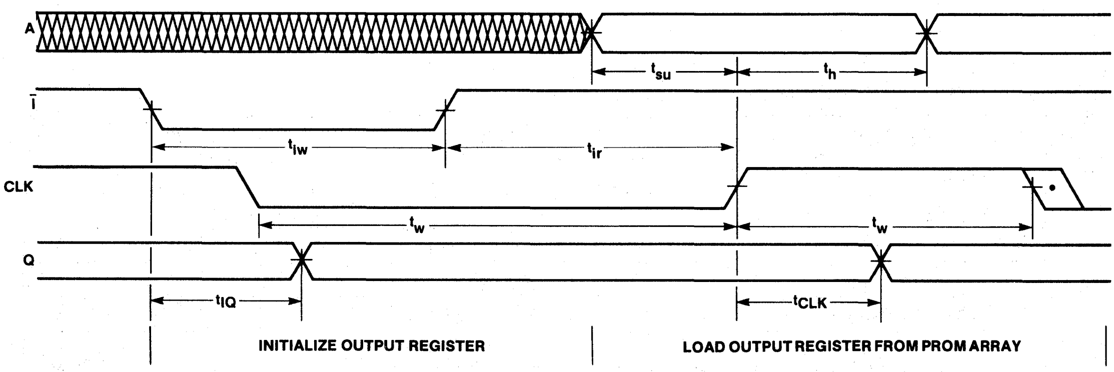
† Typical at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		11	25		11	20	ns
t_{IQ}	Initialization to output delay		23	40		23	35	ns
f_{MAXD}	Maximum diagnostic clock frequency	7	18		10	18		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		17	35		17	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns

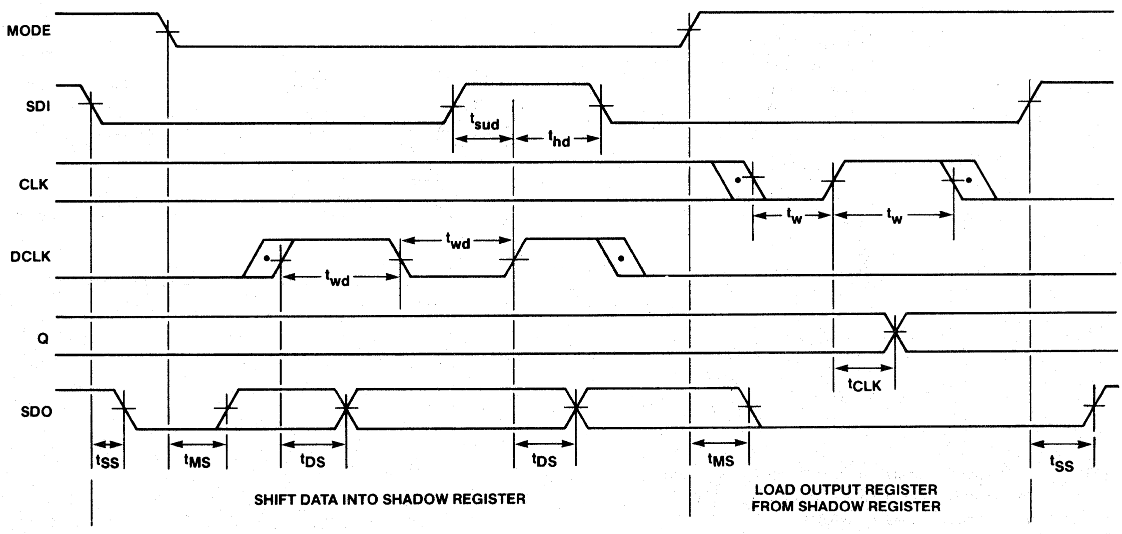
† Typical at 5.0 V V_{CC} and 25° C T_A.

Definition of Waveforms

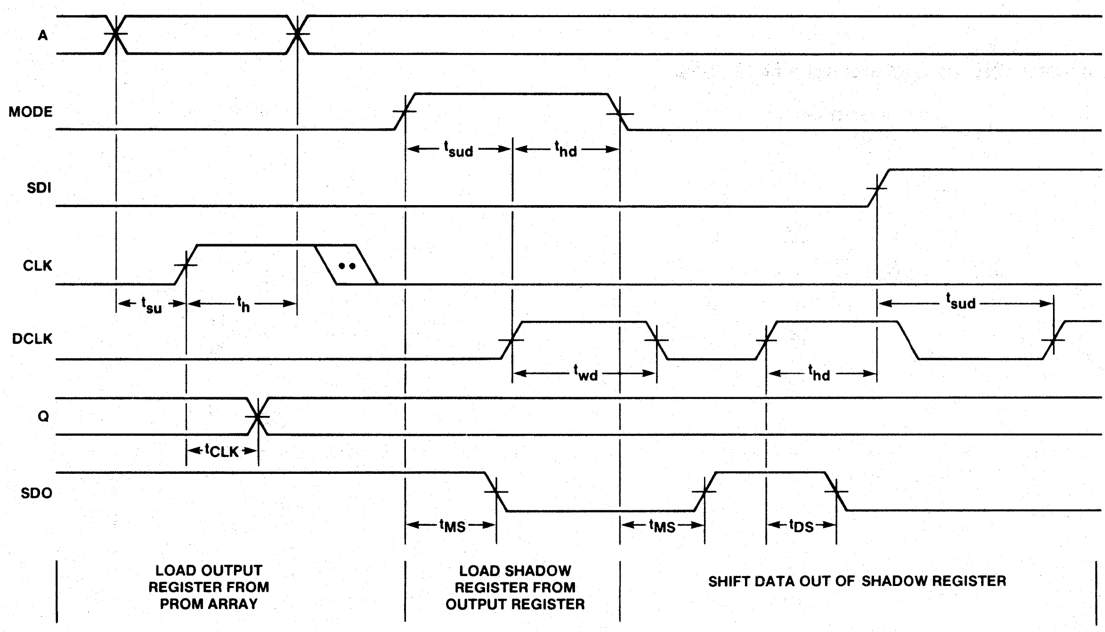


NORMAL PROM OPERATION (MODE = LOW)

Definition of Waveforms

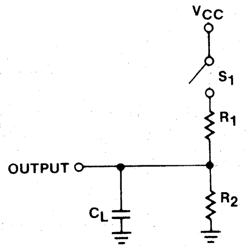


SYSTEM CONTROL

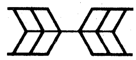


SYSTEM OBSERVATION

Switching Test Load

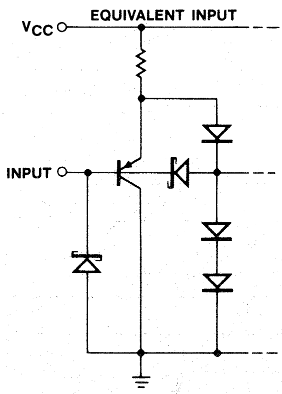


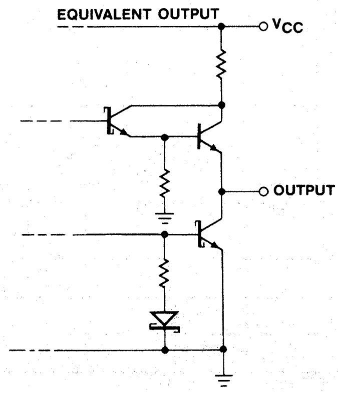
Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

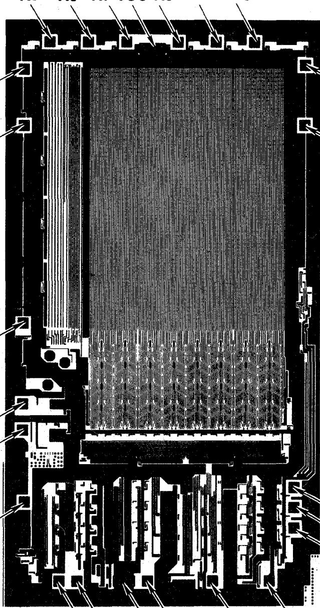
NOTES: 1. For commercial operating range R_1 = 200Ω, R_2 = 390Ω.
For military operating range R_1 = 300Ω, R_2 = 600Ω.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
4. Input access measured at the 1.5 V level.
5. Data delay is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.

Schematic of Inputs and Outputs





Die Configuration



3

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

MANUFACTURER	PROGRAMMER TYPE	PROGRAMMING MODULE	SOCKET CONFIGURATION
Data I/O	Unipack Rev-V07 Unipack2 Rev-V05	Family Code AA	Pinout Code 87

MONOLITHIC MEMORIES PROM PROGRAMMER REFERENCE CHART

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98073	Kontron Electronics 630 Price Ave. Redwood City, CA 94063	Stag Microsystems 528-5 Weddell Dr. Sunnyvale, CA 94089	Digelec 586-1 Weddell Dr. Sunnyvale, CA 94089	Varix 1210 E. Campbell Rd. Richardson, TX 75081
Programmer Model(s)	Model 19/29 Model 22	Model MPP-805	Model PPX Model PP17	UP803	OMNI
MMI Generic Bipolar PROM Personality Module	UniPak Rev 07 UniPak II Rev 05 (Not all PROMs are supported by earlier UniPak revisions	MOD16		FAM Mod. No. 12	
Socket Adapter(s) and Device Code					
63080/81	F18 P02 Model 22A - Adapter 351A-064	SA3	AM110-2 Code 21	DA No. 2 Pinout 1A Switch Pos. 0-7 (63S080) Switch Pos. 0-6 (63S081)	63S080 63S081
63S140/41	FD1 P01 Model 22A - Adapter 351A-064	SA4-2	AM130-2 Code 21	DA No. 7 Pinout 1B Switch Pos. 0-7 (63S140) Switch Pos. 0-6 (63S141)	63S140 63S141
63S240/41	F18 P03 Model 22A - Adapter 351A-064	SA4-1	AM130-3 Code 21	DA No. 4 Pinout 1D Switch Pos. 2-15 (63S240) Switch Pos. 2-14 (63S241)	63S240 63S241
63S280/81	F18 P08 Model 22A - Adapter 351A-064	†	†	†	63S280 63S281
63S440/41	F18 P05 Model 22A - Adapter 351A-064	SA4	AM140-2 Code 21	DA No. 3 Pinout 1E Switch Pos. 0-7 (63S440) Switch Pos. 0-6 (63S441)	63S440 63S441
63S480/81	F18 P09 Model 22A - Adapter 351A-064	†	†	†	63S480 63S481
63RA481	F18 P65† Model 22A - Adapter 351A-074	SA31-2	†	Pinout 1H† Switch Pos. 5-14	†
63DA441/42	FAA PAC Adapter 351A-073	†	†	†	†
63S841	F18 P06 Model 22A - Adapter 351A-064	SA4-4	AM 140-3 Code 21	DA No. Pinout 1L Switch Pos. 5-15 (63S840) Switch Pos. 5-14 (63S841)	63S840 63S841
63RS881	F18 P86 Model 22A - Adapter 351A-074 (300 mil pkg)	†	†	DA No. 64† Switch Pos. 0-12	†

† Contact manufacturer for availability and programming information.

MONOLITHIC MEMORIES PROM PROGRAMMER REFERENCE CHART

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98073	Kontron Electronics 630 Price Ave. Redwood City, CA 94063	Stag Microsystems 528-5 Weddell Dr. Sunnyvale, CA 94089	Digelec 586-1 Weddell Dr. Sunnyvale, CA 94089	Varix 1210 E. Campbell Rd. Richardson, TX 75081
Programmer Model(s)	Model 19/29 Model 22	Model MPP-805	Model PPX Model PP17	UP803	OMNI
MMI Generic Bipolar PROM Personality Module	UniPak Rev 07 UniPak II Rev 05 (Not all PROMs are supported by earlier UniPak revisions)	MOD16		FAM Mod. No. 12	
Socket Adapter(s) and Device Code					
63DA841	FAA PAD Adapter 351A-073	†	†	†	†
63S1641	F18 P53 Model 22A - Adapter 351A-064	SA20	AM 120-6 Code 21	DA No. 70† Switch Pos. 4-12	63S1641
63S1681	F18 P21	SA5-4	AM 100-5 Code 21	†	63S1681
63RA1681 **63RS1681**	F18 PA3	†	†	†	†
63D1641	FB2 P80 Adapter 351A-073	†	†	†	†
63D1643	FAA P87 Adapter 351A-073	†	†	†	†
63PL1681 **63PS1681**	F18 P21	SA5-4	AM 100-5 Code 21	†	†
63S3281	F18 P63	†	†	DA No. 64 Pinout 47 Switch Pos. 0-4	†

† Contact manufacturer for availability and programming information.

Generic
NiCR PROM Family
53/63XX-1 53/63XX-2

Features/Benefits

- **From 2048-bit to 8192-bit memory**
- **8-bit wide for byte-oriented applications**
- **-1 series for standard performance**
- **-2 series for enhanced performance**
- **Reliability-proven nichrome fusible links (qualified for MIL-M-38510)**
- **PNP inputs for low input current**
- **Compatible pin configurations for upward expansion**

Application

- **Microprogram store**
- **Microprocessor program store**
- **Look up table**
- **Character generator**
- **Random logic**
- **Code converter**

Description

The 53/63XX series generic PROM family offers a wide selection of size and organizations. The 8-bit wide PROMs range from 256x8 to 1024x8 in a wide selection of package sizes including the space-saving SKINNYDIP® 24-pin .300-inch wide package. All PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping, three-state and open-collector outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on-chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Generic PROM Selection Guide

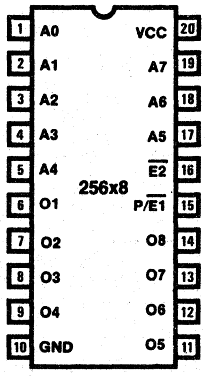
MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	COMMERCIAL	MILITARY
2K	256x8	OC TS	20	N,J	6308-1 6309-1	5308-1 5309-1
4K	512x8	OC TS	24 (28)	N, J, JS*, F, (L)	6340-1 6341-1, -2	5340-1 5341-1, -2
		OC TS	20	N, J	6348-1 6349-1, -2	5348-1 5349-1, -2
8K	1024x8	OC TS	24	N,J,JS*,F	6380-1, -2 6381-1, -2	5380-1, -2 5381-1, -2

* JS is the .300 inch wide SKINNYDIP package.

TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories MMI

Pin Configurations

53/6308-1
53/6309-1



53/6348-1
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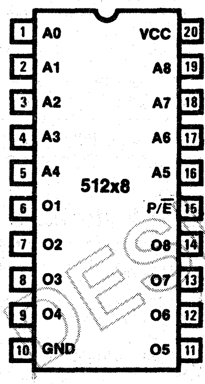
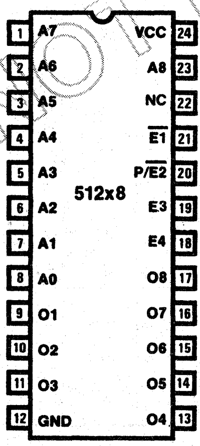
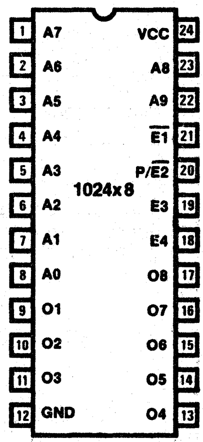


53/6340-1
53/6341-1, -2



53/6380-1, -2
53/6381-1, -2



Absolute Maximum Ratings

Supply voltage V_{CC} .... −0.5 V to 7 V
Input voltage .... −1.5 V to 7 V
Off-state output voltage .... −0.5 V to 5.5 V
Storage temperature .... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			-1 SERIES MIN	-1 SERIES MAX	-2 SERIES MIN	-2 SERIES MAX	UNIT
V_{IL}	Low-level input voltage					0.8		0.8	V
V_{IH}	High-level input voltage				2		2		V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.5		−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45 V			−0.25		−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 4.5 V (Program pin) V_I = V_{CC} MAX (Other pins)			40		40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8 V V_{IH} = 2 V	MIL I_{OL} = 12 mA			0.5		0.5	V
			COM I_{OL} = 16 mA						
V_{OH}	High-level output voltage*	V_{CC} = MIN V_{IL} = 0.8 V V_{IH} = 2 V	MIL I_{OH} = −2 mA		2.4		2.4		V
			COM I_{OH} = −3.2 mA						
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.5 V			−100		−40	μA
I_{OZH}			V_O = 2.4 V			100		40	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V			100		40	μA
			V_O = 5.5 V					100	
I_{OS}	Output short-circuit current*†	V_{CC} = 5 V	V_O = 0 V		−20	−90	−20	−90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All Outputs open	'08, '09			155		155	mA
			'40, '41, '48, '49	MIL		155		175	
				COM		155		155	
			'80, '81	MIL		175		175	
				COM		175		170	

* Three-state only.

† Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Commercial Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	R1 (Ω)	R2 (Ω)
6308-1, 6309-1	70	30	300	600
6340-1, 6341-1	70	30		
6341-2	55	30		
6348-1, 6349-1	70	30		
6349-2	55	30		
6380-1, 6381-1	90	40		
6380-2	70	30		
6381-2	55	30		

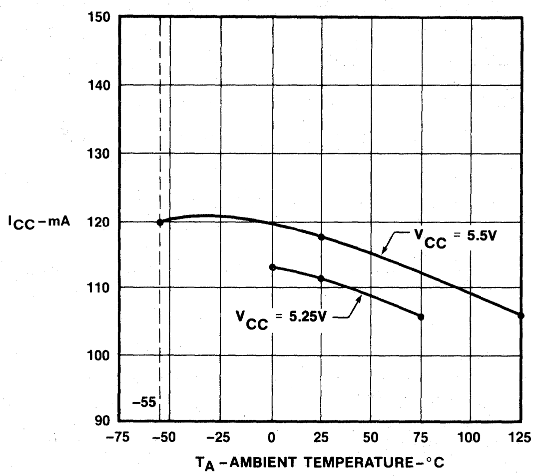
Switching Characteristics Over Military Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	R1 (Ω)	R2 (Ω)
5308-1, 5309-1	80	40	375	750
5340-1, 5341-1	80	40		
5341-2	70	40		
5348-1, 5349-1	80	40		
5349-2	70	40		
5380-1, 5381-1	125	40		
5380-2	90	40		
5381-2	70	40		

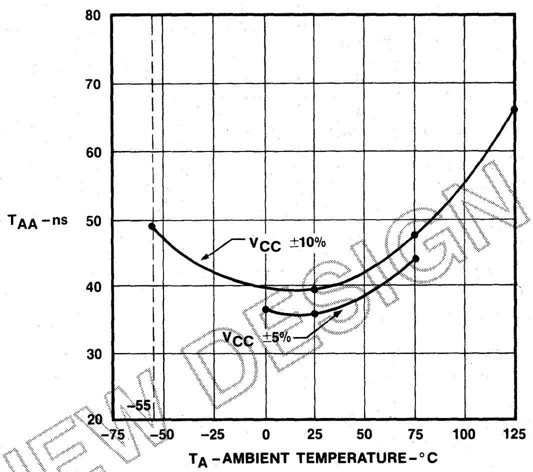
Typical Characteristics

53/6309

Typical I_{CC} vs Temperature

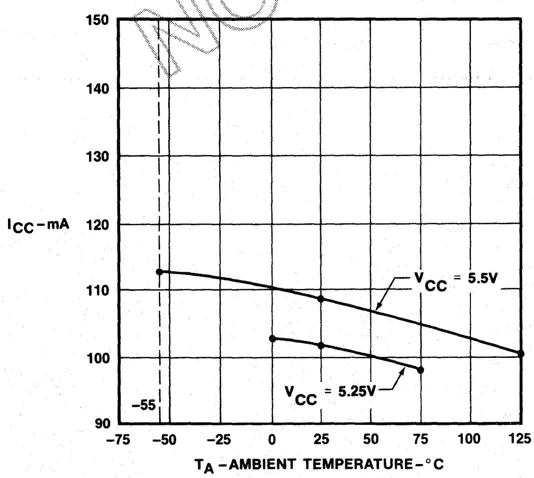


Typical T_{AA} vs Temperature

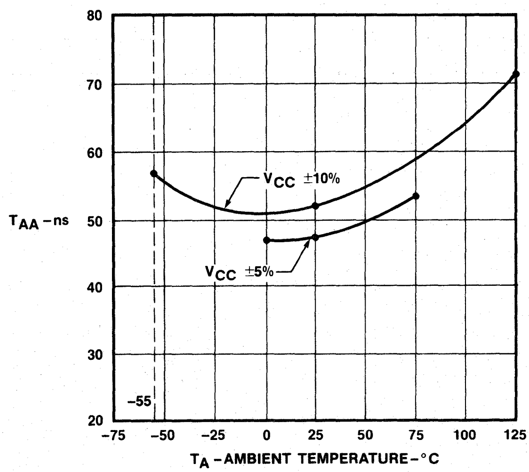


53/6341
53/6349

Typical I_{CC} vs Temperature



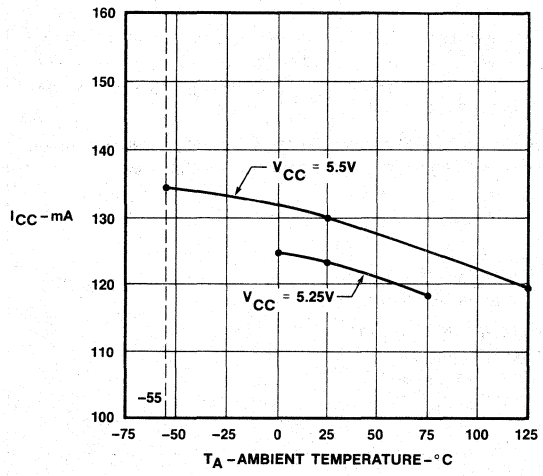
Typical T_{AA} vs Temperature



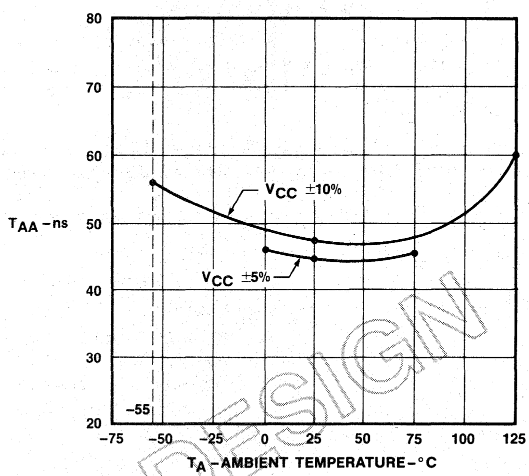
Typical Characteristics

53/6381

Typical I_{CC} vs Temperature

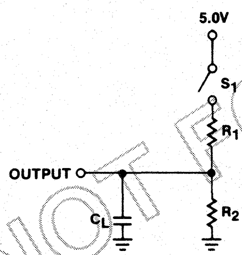


Typical T_{AA} vs Temperature

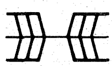
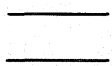


NOTE: Typical characteristic curves are for three-state devices. Equivalent open collector devices decrease in I_{CC} approximately 10 mA and increase in T_{AA} approximately 6 ns.

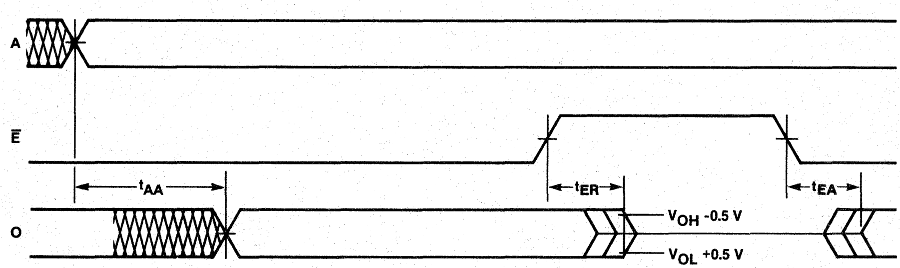
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 1.0 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed, C_1 = 30 pF and measured at 1.5 V output level.
5. For open collector devices, TEA and TER are measured at the 1.5 V output level with S_1 closed and C_L = 30 pF.
6. For three-state devices, TEA is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.

   TER is tested with C_L = 5 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} -0.5 output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} +0.5 V output level.

Commercial Programmers

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Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION

Data I/O Corp.
10525 Willows Rd. N.E.
Redmond, WA 98073

Kontron Electronics, Inc.
630 Price Ave.
Redwood City, CA 94063

Digelec Inc.
586 Weddell Dr. Suite 1
Sunnyvale, CA 94089

Stag Microsystems Inc.
528-5 Weddell Dr.
Sunnyvale, CA 94089

MONOLITHIC MEMORIES PROM PROGRAMMER REFERENCE CHART

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Programmer Model(s)	Model 19/29 Model 22	Model MPP-805	Model PPX Model PP17	UP803	OMNI
MMI Generic Bipolar PROM Personality Module	UniPak Rev 07 UniPak II Rev 05 (All NiCr PROMs should be programmed on these or later revisions)	MOD4		FAM Mod. No. 12	
Socket Adapter(s) and Device Code					
6308/09	FD1 P08 Model 22A - Adapter 351A-064	SA6-1	AM120-2 Code 20	DA No. 27 Pinout 2B Switch Pos. 5-15 (6308) Switch Pos. 5-14 (6309)	6308 6309
6340/41	FD1 P15 Model 22A - Adapter 351A-074 (300 mil pkg)	SA5-1	AM100-3 Code 20	DA No. 7 Pinout 1J Switch Pos. 4-13 (6340) Switch Pos. 4-12 (6341)	6340 6341
6348/49	FD1 P09 Model 22A - Adapter 531A-064	SA6	AM120-3 Code 20	DA No. 4 Pinout 1Q Switch Pos. 4-15 (6348) Switch Pos. 4-14 (6349)	6348 6349
6380/81	FD1 P16 Model 22A - Adapter 351A-074 (300 mil pkg)	SA5	AM100-4 Code 20	DA No. 7 Pinout 1K Switch Pos. 4-11 (6380) Switch Pos. 4-10 (6381)	6380 6381

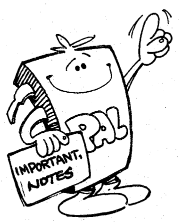

PAL
IMPORTANT NOTES

Table of Contents

PLE

PLE to PROM Cross Reference

TEMP. RANGE	PLE NUMBER	INPUTS	OUTPUTS	OUTPUT TYPE	MEMORY SIZE	PROM NUMBER	PACKAGE
Com.	PLE5P8C	5	8	Three-State	32 x 8	63S081	16N,J,(20),(NL)
	PLE5P8AC	5	8	Three-State	32 x 8	63S081A	16N,J,(20),(NL)
	PLE8P4C	8	4	Three-State	256 x 4	63S141A	16N,J,(20),(NL)
	PLE8P8C	8	8	Three-State	256 x 8	63S281A	20N,J,NL
	PLE9P4C	9	4	Three-State	512 x 8	63S241A	16N,J,(20),(NL)
	PLE9P8C	9	8	Three-State	512 x 8	63S481A	20N,J,NL
	PLE10P4C	10	4	Three-State	1024 x 4	63S841A	18N,J,(20),(NL)
	PLE10P8C	10	8	Three-State	1024 x 8	63S1881A	24NS,JS,(28),(NL)
	PLE11P4C	11	4	Three-State	2048 x 4	63S841A	18N,J,(28),(NL)
	PLE11P8C	11	8	Three-State	2048 x 8	63S1681A	24N,J,NS,JS,(28),(NL)
	PLE12P4C	12	4	Three-State	4096 x 4	63S1641A	20N,J,(28),(NL)
	PLE12P8C	12	8	Three-State	4096 x 8	63S3281A	24N,J,(28),(NL)
	PLE9R8C	9	8	Register	512 x 8	63RA481A	24NS,JS,(28),(NL)
	PLE10R8C	10	8	Register	1024 x 8	63RS881A	24NS,JS,(28),(NL)
	PLE11RA8C	11	8	Register	2048 x 8	63RA1681A	24NS,JS,(28),(NL)
	PLE11RS8C	11	8	Register	2048 x 8	63RS1681A	24NS,JS,(28),(NL)
Mil.	PLE5P8M	5	8	Three-State	32 x 8	53S081	16J,F,W,(20),(L)
	PLE8P4M	8	4	Three-State	256 x 4	53S141A	16J,F,W,(20),(L)
	PLE8P8M	8	8	Three-State	256 x 8	53S281A	20J,W,L
	PLE9P4M	9	4	Three-State	512 x 4	53S241A	16J,F,W,(20),(L)
	PLE9P8M	9	8	Three-State	512 x 8	53S481A	20J,L*
	PLE10P4M	10	4	Three-State	1024 x 4	53S441A	18J,F,W,(20),(L)
	PLE11P4M	11	4	Three-State	2048 x 4	53S841A	18J,F,W,(28),(L)
	PLE11P8M	11	8	Three-State	2048 x 8	53S1681A	24JS,J,W,(28),(L)
	PLE12P4M	12	4	Three-State	4096 x 4	53S1641A	20J
	PLE12P8M	12	8	Three-State	4096 x 8	53S3281A	24J,W,(28),(L)
	PLE9R8M	9	8	Register	512 x 8	53RA481A	24JS,(28),(L)*
	PLE10R8M	10	8	Register	1024 x 8	53RS881A	24JS,W,(28),(L)
	PLE11RA8M	11	8	Register	2048 x 8	53RA1681A	24JS,W,(28),(L)
	PLE11RS8M	11	8	Register	2048 x 8	53RS1681A	24JS,W,(28),(L)

* Contact Factory for Flat Pack.

Programmable Logic Element PLE™ Family

Features/Benefits

- Programmable replacement for conventional TTL logic
- Reduces IC inventories and simplifies their control
- Expedites and simplifies prototyping and board layout
- Saves space with .3 inch SKINNYDIP® packages
- Programmed on standard PROM programmers
- Test and simulation made simple with PLEASM software
- Low-current PNP inputs
- Three-state outputs
- Reliable Ti-W fuses guarantee >98% programming yield

Ordering Information

PLE5P8 A C N SHRP

- PROGRAMMABLE LOGIC ELEMENT
- NUMBER OF INPUTS
- OUTPUT TYPE
  - P = Non registered
  - R = Registered
  - RA = Registered asynchronous enable
  - RS = Registered synchronous enable
- NUMBER OF OUTPUTS
- PERFORMANCE
  - Blank = Standard
  - A = Enhanced
- OPTIONAL PROCESSING
  - SHRP = Reliability Enhanced
  - 883B = Mil-Std-883 Method 5004 and 5005 Level B
- PACKAGE
  - N = Plastic dip
  - NS = SKINNYDIP plastic
  - J = Ceramic dip
  - JS = SKINNYDIP ceramic
  - F = Flat Pack
  - L = Leadless chip carrier
  - NL = Plastic leaded chip carrier
  - W = Cerpak
- TEMPERATURE RANGE
  - C = 0°C to + 75°C
  - M = -55°C to + 125°C

4

PLE Selection Guide

PART NUMBER	INPUTS	OUTPUTS	PRODUCT TERMS	OUTPUT REGISTERS	t_{PD} (ns) MAX *
PLE5P8	5	8	32		25
PLE5P8A	5	8	32		15
PLE8P4	8	4	256		30
PLE8P8	8	8	256		28
PLE9P4	9	4	512		35
PLE9P8	9	8	512		30
PLE10P4	10	4	1024		35
PLE11P4	11	4	2048		35
PLE11P8	11	8	2048		35
PLE12P4	12	4	4096		35
PLE12P8	12	8	4096		40
PLE9R8	9	8	512	8	15
PLE10R8	10	8	1024	8	15
PLE11RA8	11	8	2048	8	15
PLE11RS8	11	8	2048	8	15

* Clock to output time for registered outputs.

NOTE: Commercial limits specified.

PLE™ is a trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

PLE means Programmable Logic Element

Joining the world of IdeaLogic™ is a new generation of high-speed PROMs which the designer can use as *Programmable Logic Elements.* The combination of PLEs as logic elements with PALs can greatly enhance system speed while providing almost unlimited design freedom.

Basically, PLEs are ideal when a large number of product terms is required. On the other hand, a PAL is best suited for situations when many inputs are needed.

The PLE transfer function is the familiar OR of products. Like the PAL, the PLE has a single array of fusible links. Unlike the PAL, the PLE circuits have a programmable OR array driven by a fixed AND array (the PAL is a programmed AND array driving a fixed OR array).

PRODUCT TERM AND INPUT LINES

	PLE	PAL
Product Terms	32 to 4096	2 to 16
Input Lines	5 to 12	10 to 20

The PLE family features common electrical parameters and programming algorithm, low-current PNP inputs, full Schottky clamping and three-state outputs.

The entire PLE family is programmed on conventional PROM programmers with the appropriate personality cards and socket adapters.

Registered PLEs

The registered PLEs have on-chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start-up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ($\overline{E}$) and synchronous ($\overline{ES}$) enables are Low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting $\overline{E}$ to a High or if $\overline{ES}$ is High when the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high-impedance state.

A flexible initialization feature allows start-up and time-out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{IS}$) pin Low, one of the 16 initialize words, addressed through pins 5,6,7 and 8 will be set in the output registers independent of all other input pins. The unprogrammed state of $\overline{IS}$ words are Low, presenting a CLEAR with $\overline{IS}$ pin Low. With all $\overline{IS}$ column words (A3-AO) programmed to the same pattern, the $\overline{IS}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{IS}$ words programmed High a PRESET function is performed.

The PLE9R8 has asynchronous PRESET and CLEAR functions. With the chip enabled, a Low on the $\overline{PR}$ input will cause all outputs to be set to the High state. When the $\overline{CLR}$ input is set Low the output registers are reset and all outputs will be set to the Low state. The $\overline{PR}$ and $\overline{CLR}$ functions are common to all output registers and independent of all other data input states.

	AND	OR	OUTPUT OPTIONS
PLE	Fixed	Prog	TS, Registered Outputs, Fusible Polarity
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	Prog	TS, OC, Fusible Polarity
FPLS	Prog	Prog	TS, Registered Feedback I/O
PAL	Prog	Fixed	TS, Registered Feedback I/O Fusible Polarity

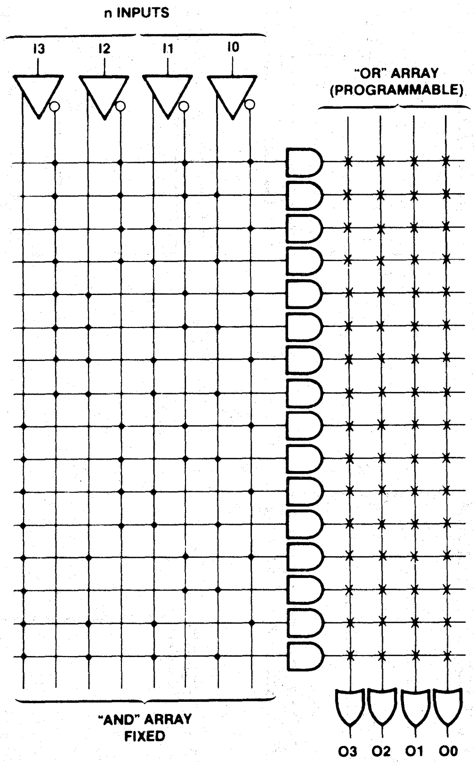
PLEASM™

Software that makes programmable logic easy.

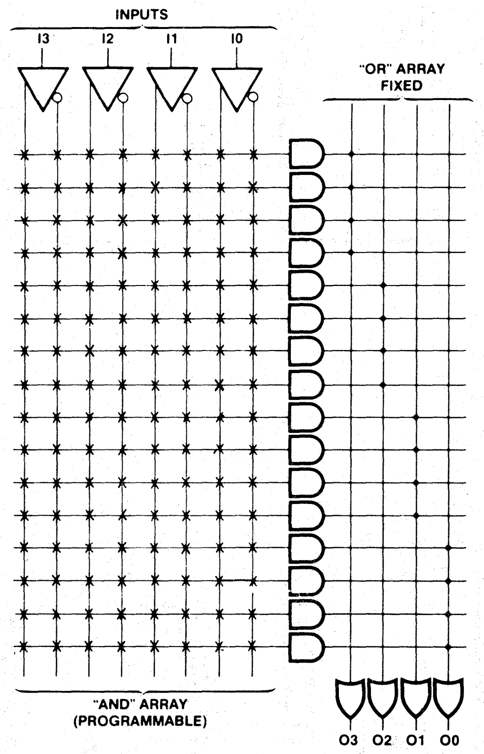
Monolithic Memories has developed a software tool to assist in designing and programming PROMs as PLEs. This package called "PLEASM" (PLE Assembler) is available for several computers including the VAX/VMS and IBM PC/DOS. PLEASM converts design equation (Boolean and arith-metic) into truth tables and formats compatible with PROM programmers. A simulator is also provided to test a design using a Function Table before actually programming the PLE.

PLEASM may be requested through the Monolithic Memories IdeaLogic Exchange.

PLE (PROM)



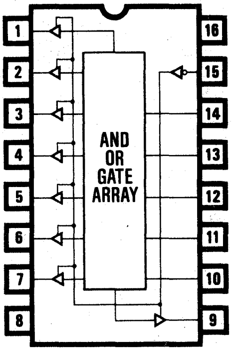
PAL



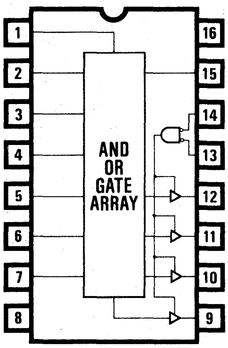
Note: • = Hardwired connection
X = Programmable fuse with a diode

Logic Symbols

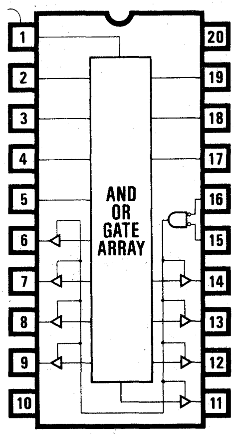
PLE5P8/A



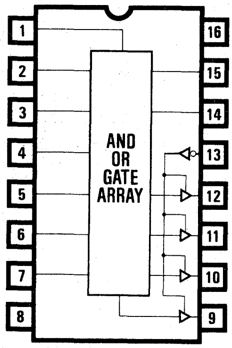
PLE8P4



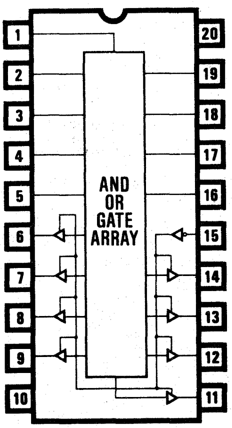
PLE8P8



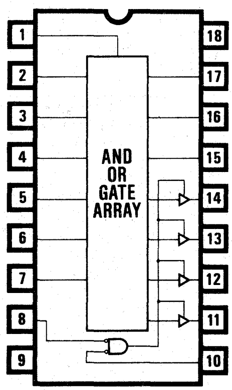
PLE9P4



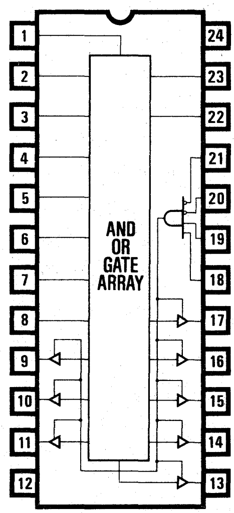
PLE9P8



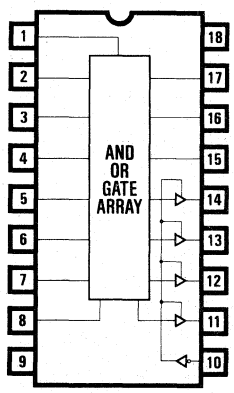
PLE10P4



PLE10P8

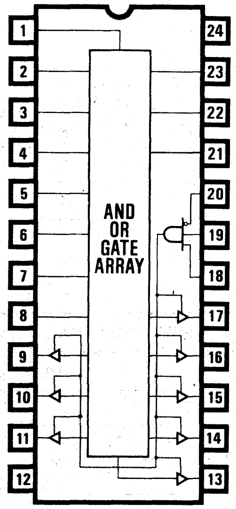


PLE11P4

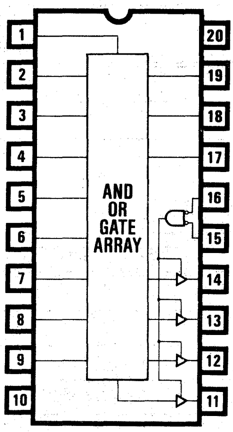


Logic Symbols

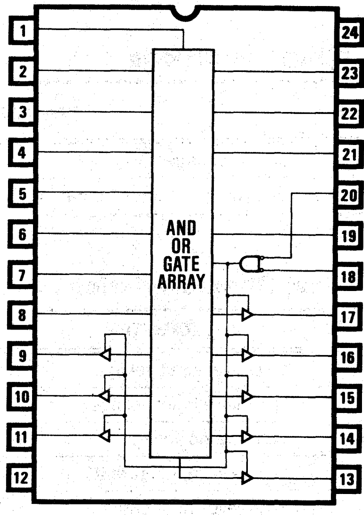
PLE11P8



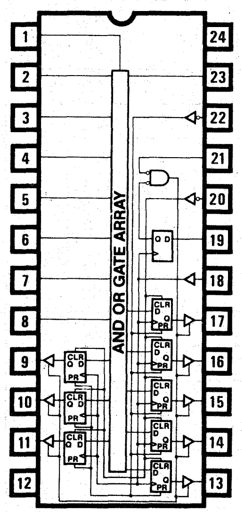
PLE12P4



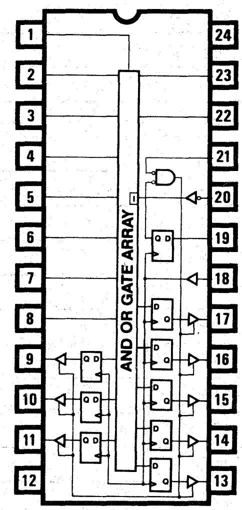
PLE12P8



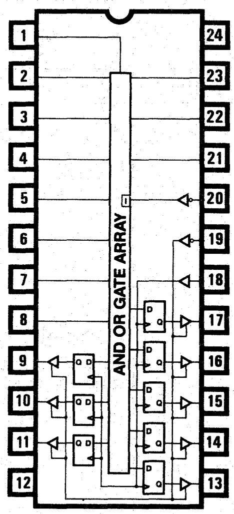
PLE9R8



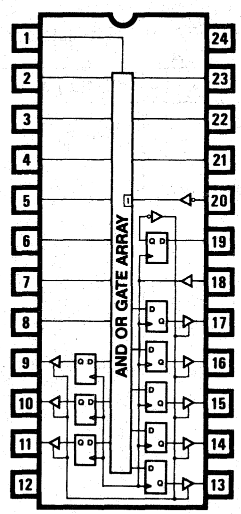
PLE10R8



PLE11RA8



PLE11RS8



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL			MILITARY			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	4.5	5	5.5	V
T_A	Operating free-air temperature	0	25	75	-55	25	125	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP*	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-0.8	-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.02	-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	$V_I = V_{CC}$				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com		0.3	.45	V
				Mil		0.3	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4	2.9		V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		-20	-50	-90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs TTL; all outputs open	5P8			90	125	mA
			5P8A			90	125	
			8P4			80	130	
			8P8			90	140	
			9P4			90	130	
			9P8			104	155	
			10P4			95	140	
			11P4			110	150	
			11P8			135	185	
			12P4			130	175	
			12P8			150	190	
			9R8			130	180	
			10R8			130	180	
			11RA8			140	185	
			11RS8			140	185	

* Typical at 5.0 V V_{CC} and 25° C T_A.

Switching Characteristics Over Military Operating Conditions

DEVICE TYPE	t_{PD} (ns) PROPAGATION DELAY MAX	t_{PZX} AND t_{PXZ} (ns) INPUT TO OUTPUT ENABLE/DISABLE TIME MAX
5P8AC	15	20
5P8C	25	20
8P4C	30	20
8P8C	28	25
9P4C	35	20
9P8C	30	25
10P4C	35	25
11P4C	35	25
11P8C	35	25
12P4C	35	25
12P8C	40	30

Switching Characteristics Over Commercial Operating Conditions

DEVICE TYPE	t_{PD} (ns) PROPAGATION DELAY MAX	t_{PZX} AND t_{PXZ} (ns) INPUT TO OUTPUT ENABLE/DISABLE TIME MAX
5P8M	35	30
8P4M	40	30
8P8M	40	30
9P4M	45	30
9P8M	40	30
10P4M	50	30
11P4M	50	30
11P8M	50	30
12P4M	50	30
12P8M	50	35

Operating Conditions

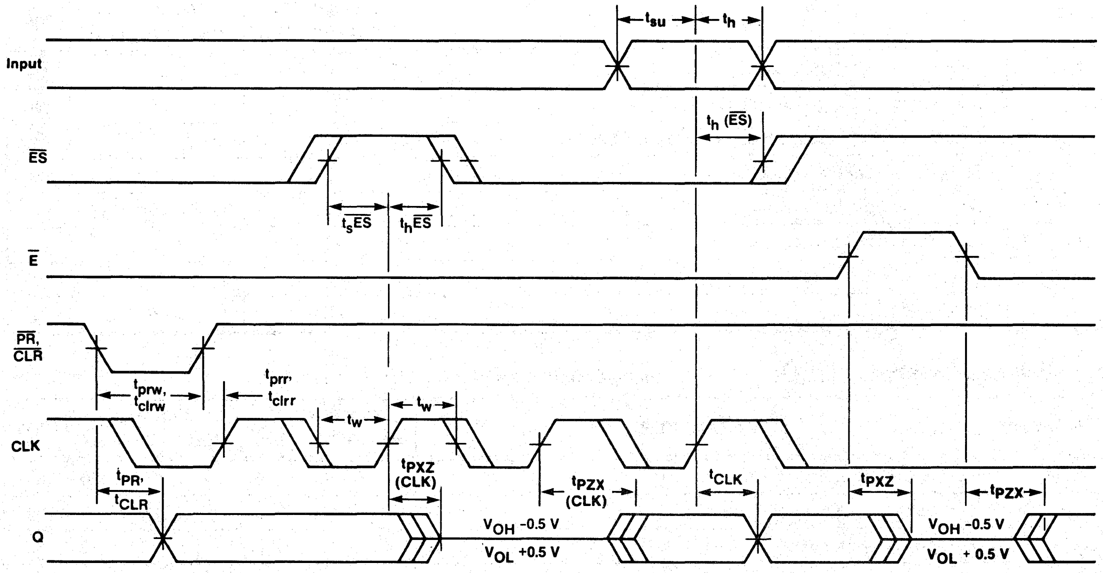
SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP*	COMMERCIAL MAX	MILITARY MIN	MILITARY TYP*	MILITARY MAX	UNIT
t_w	Width of clock (High or Low)	20	10		20	10		ns
t_{prw} t_{clrw}	Width of preset or clear (Low) to Output (High or Low)	20	10		20	10		ns
t_{prr} t_{clrr}	Recovery from preset or clear (Low) to clock High	20	11		25	11		ns
t_{su}	Setup time from input to clock	30	22		35	22		ns
$t_s(\overline{ES})$	Setup time from $\overline{ES}$ to clock	10	7		15	7		ns
t_h	Hold time from input to clock	0	-5		0	-5		ns
$t_h(\overline{ES})$	Hold time from $\overline{ES}$ to clock	5	-3		5	-3		ns

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP*	COMMERCIAL MAX	MILITARY MIN	MILITARY TYP*	MILITARY MAX	UNIT
t_{CLK}	Clock to output delay		11	15		11	20	ns
t_{PR}	Preset to output delay		15	25		15	25	ns
t_{CLR}	Clear to output delay		18	25		18	35	ns
t_{PZX} (CLK)	Clock to output enable time		14	25		14	30	ns
t_{PXZ} (CLK)	Clock to output disable time		14	25		14	30	ns
t_{PZX}	Input to output enable time		10	20		10	25	ns
t_{PXZ}	Input to output disable time		10	20		10	25	ns

* Typical at 5.0 V V_{CC} and 25° C T_A.

Definition of Waveforms



NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V level for all tests except t_{PXZ} and t_{PZX}.
5. t_{PZX} and $t_{PZX(CLK)}$ are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   t_{PXZ} and $t_{PXZ(CLK)}$ are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH}-0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL}+0.5 V output level.

Operating Conditions

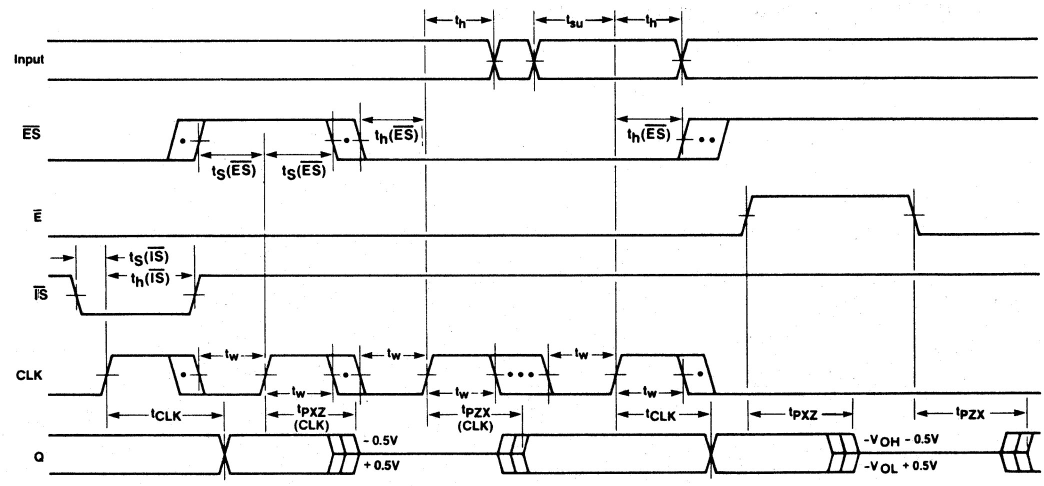
SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP*	COMMERCIAL MAX	MILITARY MIN	MILITARY TYP*	MILITARY MAX	UNIT
t_W	Width of clock (High or Low)	20	10		20	10		ns
t_{su}	Setup time from input to clock (10R8)	30	25		40	25		ns
t_{su}	Setup time from input to clock (11RA8, 11RS8)	35	28		40	28		ns
t_s ($\overline{ES}$)	Setup time from $\overline{ES}$ to clock	15	7		15	7		ns
t_s ($\overline{IS}$)	Setup time from $\overline{IS}$ to clock	25	20		30	20		ns
t_h	Hold time input to clock	0	-5		0	-5		ns
t_h ($\overline{ES}$)	Hold time ($\overline{ES}$)	5	-3		5	-3		ns
t_h ($\overline{IS}$)	Hold time ($\overline{IS}$)	0	-5		0	-5		ns

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP*	COMMERCIAL MAX	MILITARY MIN	MILITARY TYP*	MILITARY MAX	UNIT
t_{CLK}	Clock to output delay		10	15		10	20	ns
t_{PZX} (CLK)	Clock to output enable time		17	25		17	30	ns
t_{PXZ} (CLK)	Clock to output disable time		17	25		17	30	ns
t_{PZX}	Input to output enable time		17	25		17	30	ns
t_{PXZ}	Input to output disable time		17	25		17	30	ns

* Typical at 5.0 V V_{CC} and 25°C T_A.

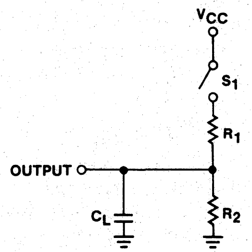
Definition of Waveforms



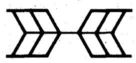
NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V level for all tests except t_{PZX} and t_{PXZ}.
5. t_{PZX} and $t_{PZX(CLK)}$ are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   t_{PXZ} and $t_{PXZ(CLK)}$ are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH}-0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL}+0.5 V output level.

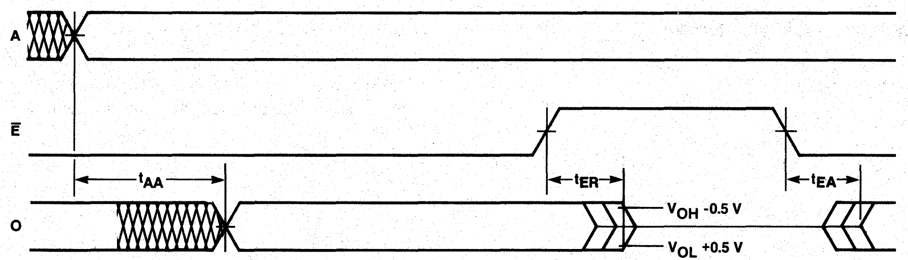
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: Apply to electrical and switching characteristics

Typical at 5.0 V V_{CC} and 25° C T_A.

Measurements are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise.

In all PLE devices unused inputs must be tied to either ground or V_{CC}. The series resistor required for unused inputs on standard TTL is NOT required for PLE devices, thus using less parts.

*Not more than on output should be shorted at a time and duration of the short-circuit should not exceed one second.

1. For commercial operating range R_1 = 200Ω, R_2 = 390Ω. For military operating range R_1 = 300Ω, R_2 = 600Ω.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2-5 ns from 0.8 to 2.0 V.
4. Input access measured at the 1.5 V level.
5. Data delay is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
6. t_{PZX} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test. t_{PXZ} is measured C_L = 5 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH}-0.5 V output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} + 0.5 V output level.

PLE™ Family Programming Instructions

Device Description

All of the members of the PLE family are manufactured with all outputs LOW in all storage locations. To produce a HIGH at a particular word, a Titanium-Tungsten Fusible-Link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To program a particular bit normal TTL levels are applied to all inputs. Programming occurs when:

1. V_{CC} is raised to an elevated level.
2. The output to be programmed is raised to an elevated level.
3. The device is enabled.

In order to avoid misprogramming the PLE only one output at a time is to be programmed. Outputs not being programmed should be connected to V_{CC} via 5 KΩ resistors.

Unless specified, Inputs should be at VIL.

Programming Sequence

The sequence of programming conditions is critical and must occur in the following order:

1. Select the appropriate address with chip disabled
2. Increase V_{CC} to programming voltage
3. Increase appropriate output voltage to programming voltage
4. Enable chip for programming pulse width
5. Decrease V_{OUT} and V_{CC} to normal levels

Programming Timing

In order to insure the proper sequence, a delay of 100 ns or greater must be allowed between steps. The enabling pulse must not occur less than 100 ns after the output voltage reaches programming level. The rise time of the voltage on V_{CC} and the output must be between 1 and 10 V/μs.

Verification

After each programming pulse verification of the programmed bit should be made with both low and high V_{CC}. The loading of the output is not critical and any loading within the DC specifications of the part is satisfactory.

Additional Pulses

Up to 10 programming pulses should be applied until verification indicates that the bit has programmed. Following verification, apply five additional programming pulses to the bit being programmed.

Programming Parameters Do not test these parameters or you may program the device

SYMBOL	PARAMETER	RECOMMENDED MIN	VALUE	MAX	UNIT
V_{CCP}	Required V_{CC} for programming	11.5	11.75	12.0	V
V_{OP}	Required output voltage for programming	10.5	11.0	11.5	V
t_R	Rise time of V_{CC} or V_{OUT}	1.0	5.0	10.0	V/μS
I_{CCP}	Current limit of V_{CCP} supply	800	1200		mA
I_{OP}	Current limit of V_{OP} supply	15	20		mA
t_{PW}	Programming pulse width (enabled)	9	10	11	μS
V_{CC}	Low V_{CC} for verification	4.2	4.3	4.4	V
V_{CC}	High V_{CC} for verification	5.8	6.0	6.2	V
MDC	Maximum duty cycle of V_{CCP}		25	25	%
t_D	Delay time between programming steps	100	120		ns
V_{IL}	Input low level	0	0	0.5	V
V_{IH}	Input high level	2.4	3.0	5.5	V

PLE™ is a trademark of Monolithic Memories.

Programming Equipment Suppliers

Monolithic Memories PLEs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PLEs available can be made unreliable by improper programming techniques.

SOURCE AND LOCATION

Data I/O Corp.
10525 Willows Rd. N.E.
Redmond, WA 98073

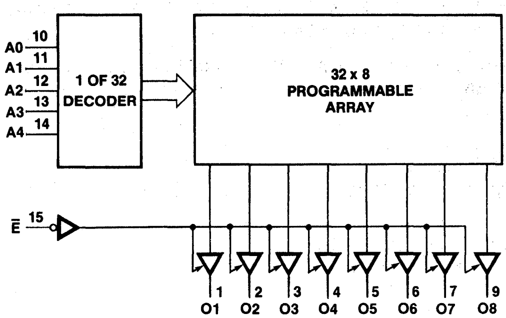
Kontron Electronics, Inc.
630 Price Ave.
Redwood City, CA 94063

Digelec Inc.
586 Weddell Dr. Suite 1
Sunnyvale, CA 94089

Varix Corp.
1210 E. Campbell Rd. Suite 100
Richardson, TX 75081

Block Diagrams

PLE5P8/A



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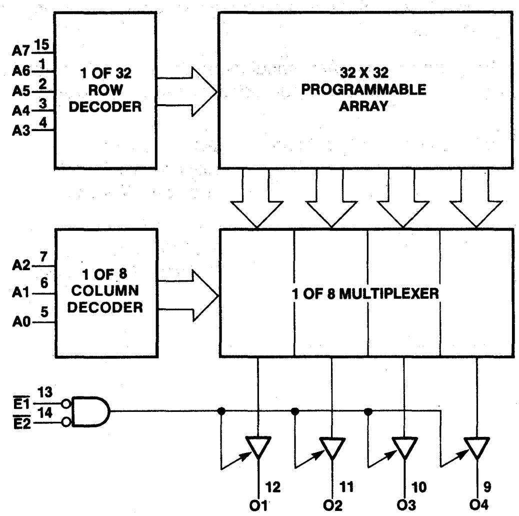

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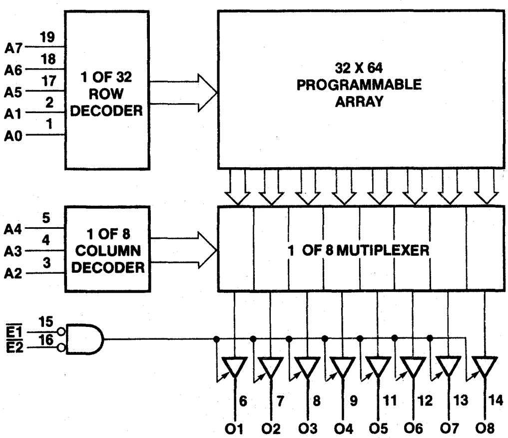

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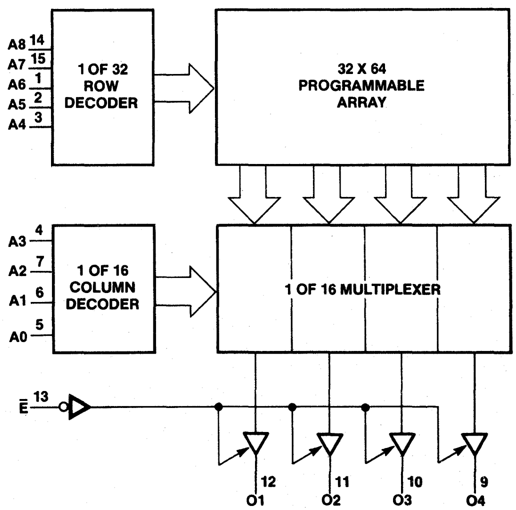

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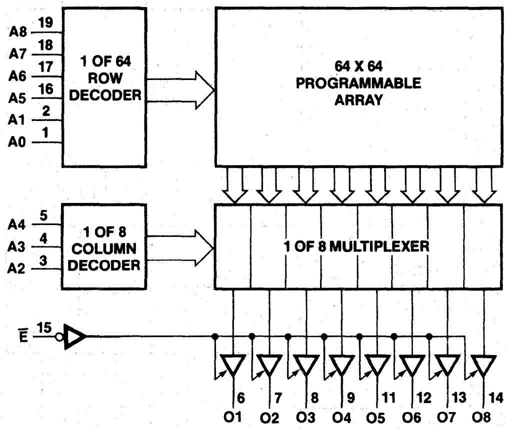

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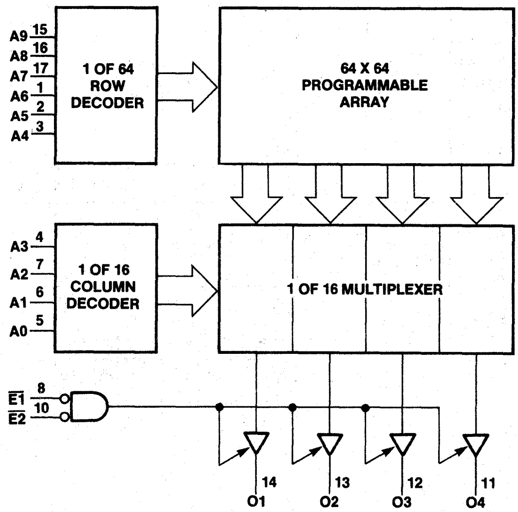

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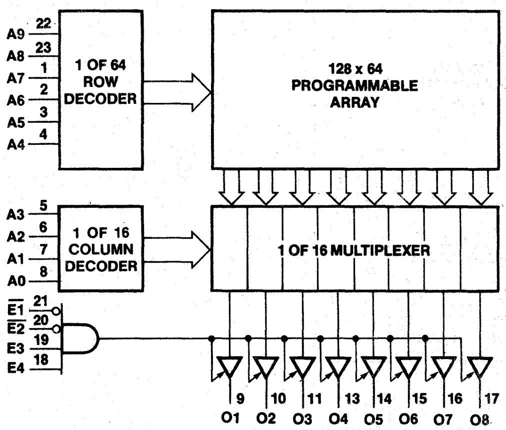

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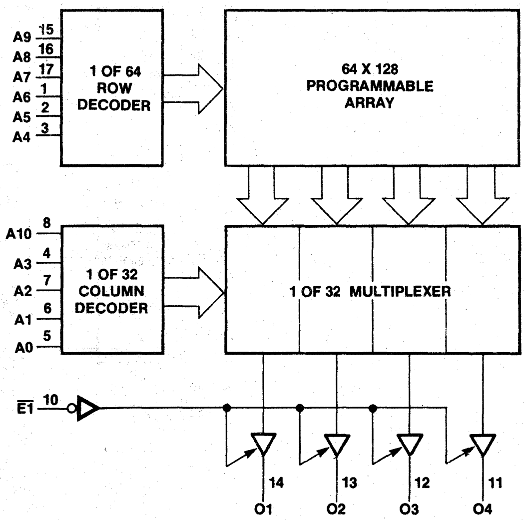

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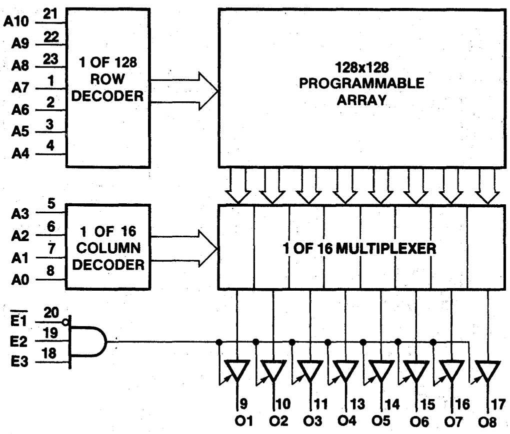

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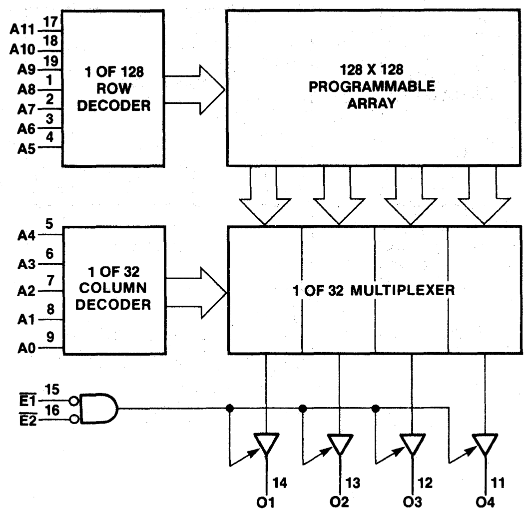

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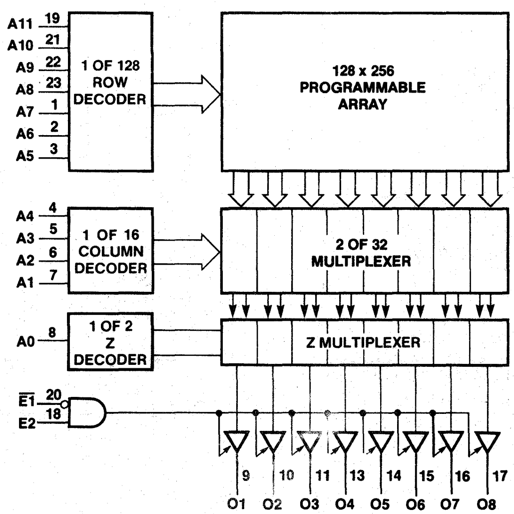
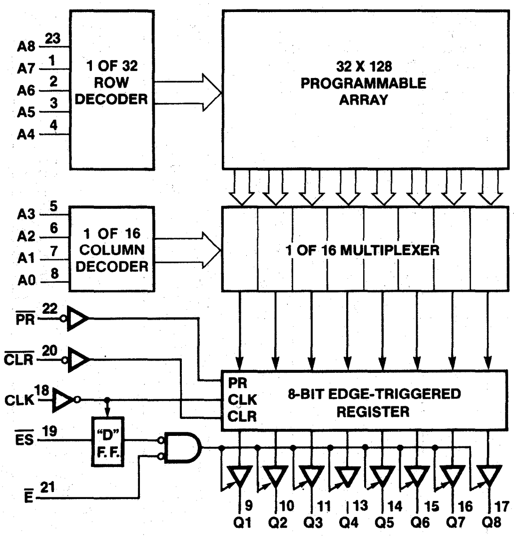


Block Diagrams

PLE9R8



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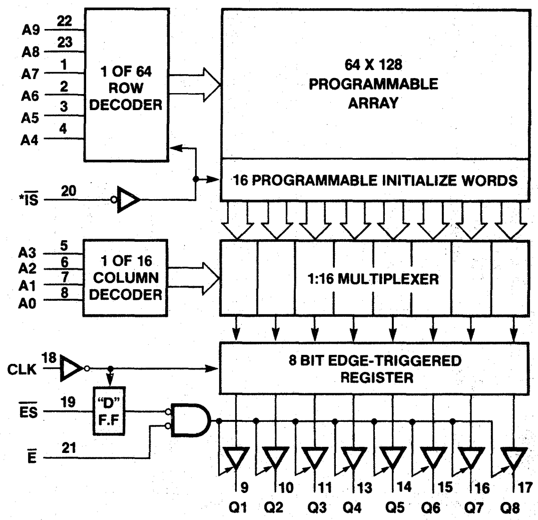

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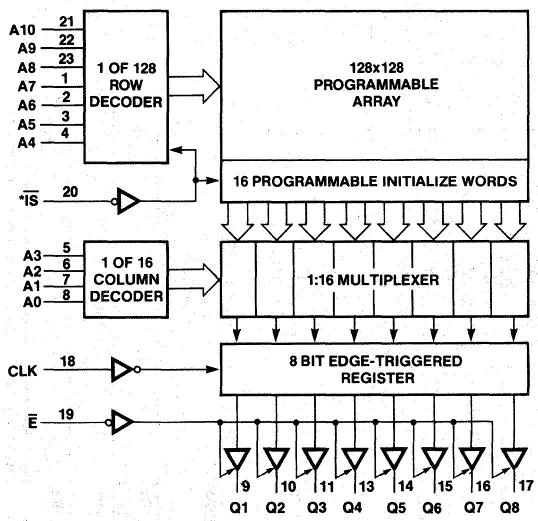

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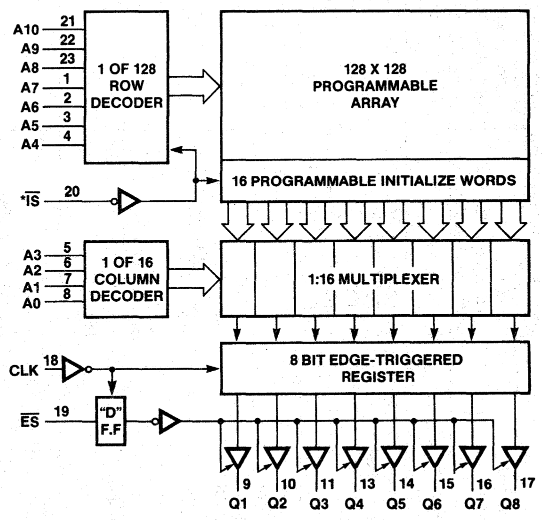

*IS selects 1:16 programmable initialization words.

MONOLITHIC MEMORIES PLE PROGRAMMER REFERENCE CHART

Source and Location	**Data I/O** **10525 Willows Rd. N.E.** **Redmond, WA 98073**	**Kontron Electronics** **630 Price Ave.** **Redwood City, CA 94063**	**Stag Microsystems** **528-5 Weddell Dr.** **Sunnyvale, CA 94089**	**Digelec** **586-1 Weddell Dr.** **Sunnyvale, CA 94089**	**Varix** **1210 E. Campbell Rd.** **Richardson, TX 75081**
Programmer Model(s)	Model 19/29 Model 22	Model MPP-805	Model PPX Model PP17	UP803	OMNI
MMI Generic Bipolar PLE Personality Module	UniPak Rev 07 UniPak II Rev 05 (Not all PLEs are supported by earlier UniPak revisions	MOD4		FAM Mod. No. 12	
Socket Adapter(s) and Device Code					
PLE5P8/ PLE5P8A	F18 P02 Model 22A- Adapter 351A-064	SA3	AM110-2 Code 21	DA No. 2 Pinout 1A Switch Pos. 0-6	63S081
PLE8P4	F18 P01 Model 22A- Adapter 351A-064	SA4-2	AM130-2 Code 21	DA No. 2 Pinout 1B Switch Pos. 0-6	63S141
PLE9P4	F18 P03 Model 22A- Adapter 351A-064	SA4-1	AM130-3 Code 21	DA No. 1 Pinout 1D Switch Pos. 2-14	63S241
PLE8P8	F18 P08 Model 22A- Adapter 351A-064	†	†	†	63S280 63S281
PLE10P4	F18 P05 Model 22A- Adapter 351A-064	SA4	AM140-2 Code 21	DA No. 3 Pinout 1E Switch Pos. 0-6	63S441
PLE9P8	F18 P08 Model 22A- Adapter 351A-064	†	†	†	63S480 63S481
PLE9R8	F18 P65† Model 22A- Adapter 351A-074	SA31-2	†	Pinout 1H † Switch Pos. 5-14	†
PLE11P4	F18 P06 Model 22A- Adapter 351A-064	SA4-4	AM140-3 Code 21	DA No. Pinout 1L Switch 5-14	63S841
PLE10R8	F18 P86† Model 22A- Adapter 351A-074 (300 mil pkg)		†	DA No. 64 † Switch Pos. 0-12	†
PLE12P4	F18 P53 Model 22A- Adapter 351A-064	SA20	AM120-6 Code 21	DA No. † Switch Pos. 4-12	63S1641
PLE11RA8 **PLE11RS8**	F18 PA3	†	†	†	†
PLE11P8	F18P21	SA5-4	AM100-5 Code 21	†	63S1681
PLE12P8	F18P63	†	†	DA No. 64 Pinout 47 Switch Pos. 0-4	†

† Contact manufacturer for availability and programming information.

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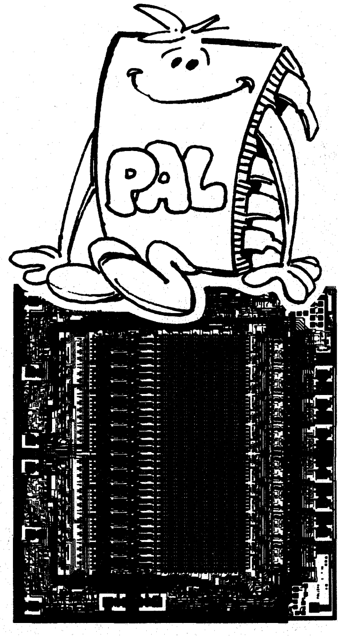
PAL®/HAL® CIRCUITS



The PAL® Concept

Monolithic Memories' family of PAL devices gives designers a powerful tool with unique capabilities for use in new and existing logic designs. The PAL saves time and money by solving many of the system partitioning and interface problems brought about by increases in semiconductor device technology.

Rapid advances in large scale integration technology have led to larger and larger standard logic functions; single I.C.s now perform functions that formerly required complete circuit cards. While LSI offers many advantages, advances have been made at the expense of device flexibility. Most LSI devices still require large numbers of SSI/MSI devices for interfacing with user systems. Designers are still forced to turn to random logic for many applications.

The designer is confronted with another problem when a product is designed. Often the function is well defined and could derive significant benefits from fabrication as an integrated circuit. However, the design cycle for a custom circuit is long and the costs can be very high. This makes the risk significant enough to deter most users. The technology to support maximum flexibility combined with fast turnaround on custom logic has simply not been available. Monolithic Memories offers the programmable solution.

The PAL family offers a fresh approach to using fuse programmable logic. PAL circuits are a conceptually unified group of devices which combine programmable flexibility with high speed and an extensive selection of interface options. PAL devices can lower inventory, cut design cycles and provide high complexity with maximum flexibility. These features, combined with lower package count and high reliability, truly make the PAL a circuit designer's best friend.

The PAL—Teaching Old PROMs New Tricks

MMI developed the modern PROM and introduced many of the architectures and techniques now regarded as industry standards. As the world's largest PROM manufacturer, MMI has the proven technology and high volume production capability required to manufacture and support the PAL.

The PAL is an extension of the fusible link technology pioneered by Monolithic Memories for use in bi-polar PROMs. The fusible link PROM first gave the digital systems designer the power to "write on silicon." In a few seconds he was able to transform a blank PROM from a general purpose device into one containing a custom algorithm, microprogram, or Boolean transfer function. This opened up new horizons for the use of PROMs in computer control stores, character generators, data storage tables and many other applications. The wide acceptance of this technology is clearly demonstrated by today's multi-million dollar PROM market.

The key to the PROM's success is that it allows the designer to quickly and easily customize the chip to fit his unique requirements. The PAL extends this programmable flexibility by utilizing proven fusible link technology to implement logic functions. Using PAL circuits the designer can quickly and effectively implement custom logic varying in complexity from random gates to complex arithmetic functions.

ANDs and ORs

The PAL implements the familiar sum of products logic by using a programmable AND array whose output terms feed a fixed OR array. Since the sum of products form can express any Boolean transfer function, the PAL circuit uses are only limited by the number of terms available in the AND - OR arrays. PAL devices come in different sizes to allow for effective logic optimization.

Figure 1 shows the basic PAL structure for a two input, one output logic segment. The general logic equation for this segment is

$$\text{Output} = (I_1+\overline{f_1})(\overline{I_1}+\overline{f_2})(I_2+\overline{f_3})(\overline{I_2}+\overline{f_4}) +$$
$$(I_1+\overline{f_5})(\overline{I_1}+\overline{f_6})(I_2+\overline{f_7})\ (\overline{I_2}+\overline{f_8})$$

where the "f" terms represent the state of the fusible links in the PAL AND array. An unblown link represents a logic 1. Thus,

fuse blown, f = 0

fuse intact, f = 1

An unprogrammed PAL has all fuses intact.

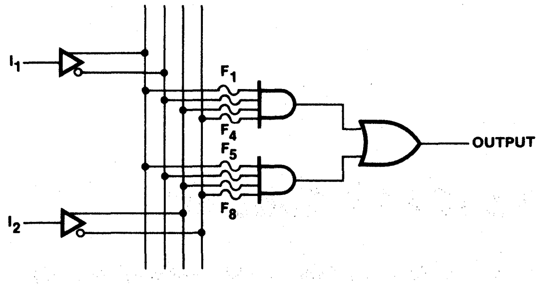


Figure 1

PAL Notation

Logic equations, while convenient for small functions, rapidly become cumbersome in large systems. To reduce possible confusion, complex logic networks are generally defined by logic diagrams and truth tables. Figure 2 shows the logic convention adopted to keep PAL logic easy to understand and use. In the figure, an "x" represents an intact fuse used to perform the logic AND function. (Note: the input terms on the common line with the x's are not connected together.) The logic symbology shown in Figure 2 has been informally adopted by integrated circuit manufacturers because it clearly establishes a one-to-one correspondence between the chip layout and the logic diagram. It also allows the logic diagram and truth table to be combined into a compact and easy to read form, thereby serving as a convenient shorthand for PAL circuits. The two input - one output example from Figure 1 redrawn using the new logic convention is shown in Figure 3.

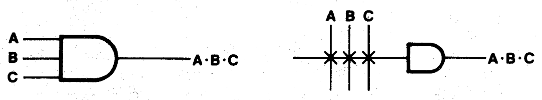


Figure 2

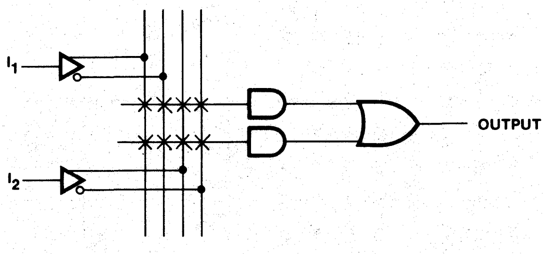


Figure 3

As a simple PAL example, consider the implementation of the transfer function:

Output $= I_1\bar{I}_2 + \bar{I}_1 I_2$

The normal combinatorial logic diagram for this function is shown in figure 4, with the PAL logic equivalent shown in figure 5.

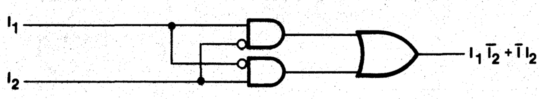


Figure 4

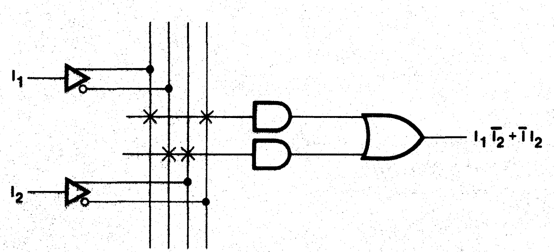


Figure 5

Using this logic convention it is now possible to compare the PAL structure to the structure of the more familiar PROM and PLA. The basic logic structure of a PROM consists of a fixed AND array whose outputs feed a programmable OR array (figure 6). PROMs are low-cost, easy to program, and available in a variety of sizes and organizations. They are most commonly used to store computer programs and data. In these applications the fixed input is a computer memory address; the output is the contents of that memory location.

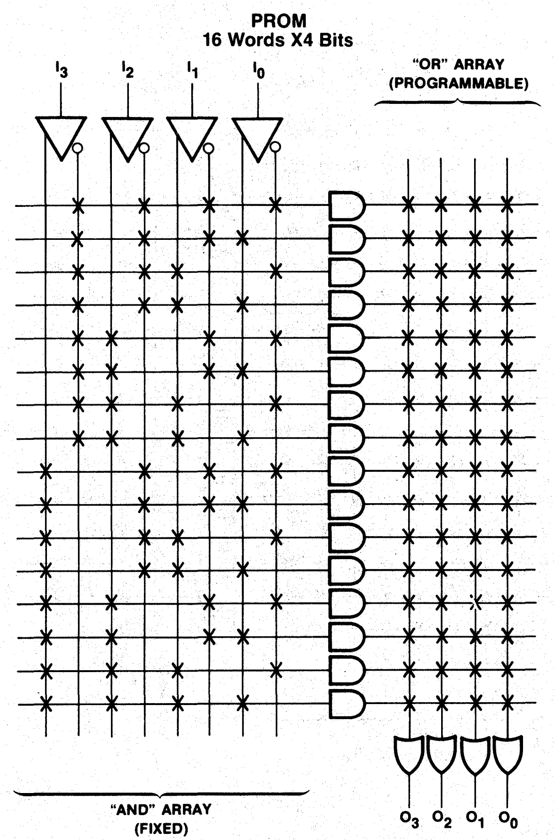


Figure 6

The basic logic structure of the PLA consists of a programmable AND array whose outputs feed a programmable OR array (Figure 7). Since the designer has complete control over all inputs and outputs, the PLA provides the ultimate flexibility for implementing logic functions. They are used in a wide variety of applications. However, this generality makes PLAs expensive, quite formidable to understand, and costly to program (they require special programmers).

The basic logic structure of the PAL, as mentioned earlier, consists of a programmable AND array whose outputs feed a fixed OR array (Figure 8). The PAL combines much of the flexibility of the PLA with the low cost and easy programmability of the PROM. Table 1 summarizes the characteristics of the PROM, PLA, and PAL logic families.

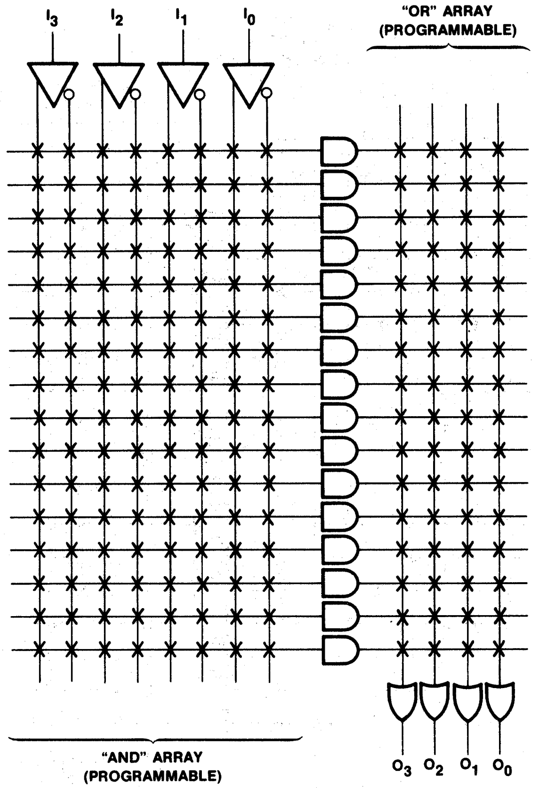


Figure 7

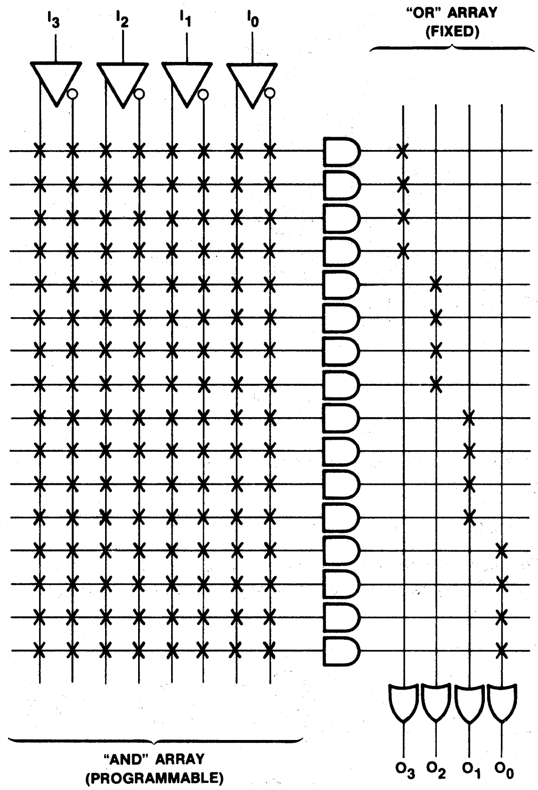


Figure 8

	AND	OR	OUTPUT OPTIONS
PROM	Fixed	Prog	TS, OC
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	None	TS, OC, Fusible Polarity
FPLS	Prog	Prog	TS, Registered Feedback, I/O
PAL	Prog	Fixed	TS, Registered Feedback, I/O

Table 1

PAL Input/Output/Function/Performance Chart

PART NO.	INPUT	OUTPUT	PROG. I/O'S	FEEDBACK REGISTER	OUTPUT POLARITY	FUNCTIONS	PERFORMANCE				
							STD	A	-2	A-2	A-4
10H8	10	8			AND-OR	AND-OR Gate Array	X		X		
12H6	12	6			AND-OR	AND-OR Gate Array	X		X		
14H4	14	4			AND-OR	AND-OR Gate Array	X		X		
16H2	16	2			AND-OR	AND-OR Gate Array	X		X		
16C1	16	2			BOTH[1]	AND-OR/NOR Gate Array	X		X		
10L8	10	8			AND-NOR	AND-OR Invert Gate Array	X		X		
12L6	12	6			AND-NOR	AND-OR Invert Gate Array	X		X		
14L4	14	4			AND-NOR	AND-OR Invert Gate Array	X		X		
16L2	16	2			AND-NOR	AND-OR Invert Gate Array	X		X		
12L10	12	10			AND-NOR	AND-OR Invert Gate Array	X				
14L8	14	8			AND-NOR	AND-OR Invert Gate Array	X				
16L6	16	6			AND-NOR	AND-OR Invert Gate Array	X				
18L4	18	4			AND-NOR	AND-OR Invert Gate Array	X				
20L2	20	2			AND-NOR	AND-OR Invert Gate Array	X				
20C1	20	2			BOTH[1]	AND-OR/NOR Gate Array	X				
16L8	10	2	6		AND-NOR	AND-OR Invert Gate Array		X		X	X
20L8	14	2	6		AND-NOR	AND-OR Invert Gate Array		X			
20L10	12	2	8		AND-NOR	AND-OR Invert Gate Array	X				
16R8	8	8		8	AND-NOR	AND-OR Invert Gate Array w/Regs		X		X	X
16R6	8	6	2	6	AND-NOR	AND-OR Invert Gate Array w/Regs		X		X	X
16R4	8	4	4	4	AND-NOR	AND-OR Invert Gate Array w/Regs		X		X	X
20R8	12	8		8	AND-NOR	AND-OR Invert w/Regs		X			
20R6	12	6	2	6	AND-NOR	AND-OR Invert w/Regs		X			
20R4	12	4	4	4	AND-NOR	AND-OR Invert w/Regs		X			
20X10	10	10		10	AND-NOR	AND-OR-XOR Invert w/Regs	X				
20X8	10	8	2	8	AND-NOR	AND-OR-XOR Invert w/Regs	X				
20X4	10	4	6	4	AND-NOR	AND-OR-XOR Invert w/Regs	X				
16X4	8	4	4	4	AND-NOR	AND-OR-XOR Invert w/Regs	X				
16A4	8	4	4	4	AND-NOR	AND-CARRY-OR-XOR Invert w/Regs	X				
16P8	10	2	6		PROG[2]	AND-OR Gate Array		X			
16RP8	8	8		8	PROG[2]	AND-OR Gate Array w/Regs		X			
16RP6	8	6	2	6	PROG[2]	AND-OR Gate Array w/Regs		X			
16RP4	8	4	4	4	PROG[2]	AND-OR Gate Array w/Regs		X			
20RA10	10		10[3]	10[3]	PROG[2]	Asynchronous Gate Array		X			
20RS10	10			10	PROG[2]	AND-OR Gate Array w/Regs		X			
20RS8	10		2	8	PROG[2]	AND-OR Gate Array w/Regs		X			
20RS4	10		6	4	PROG[2]	AND-OR Gate Array w/Regs		X			
20S10	10		10		PROG[2]	AND-OR Gate Array		X			
32R16	16	16[3]		16[3]	PROG[2]	AND-OR Gate Array w/Regs		X			
64R32	32	32[3]		32[3]	PROG[2]	AND-OR Gate Array w/Regs		X			

Table 2

[1] Simultaneous AND-OR and AND-NOR outputs

[2] Programmable active high or active low. i.e. AND-OR or AND-NOR

[3] Output can be registered or non-registered

PAL Circuits For Every Task

The members of the PAL family and their characteristics are summarized in Table 2. They are designed to cover the spectrum of logic functions at reduced cost and lower package count. This allows the designer to select the PAL that best fits his application. PAL units come in the following basic configurations:

Gate Arrays

PAL gate arrays are available in sizes from 12x10 (12 input terms, 10 output terms) to 20x2, with both active high and active low output configurations available (figure 9). This wide variety of input/output formats allows the PAL to replace many different sized blocks of combinatorial logic with single packages.

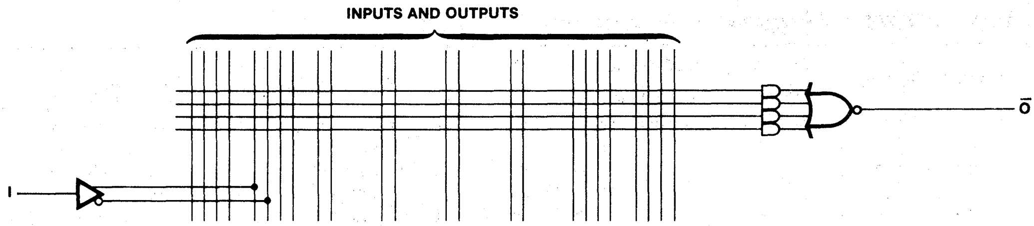


Figure 9

Programmable I/O

A feature of the high-end members of the PAL family is programmable input/output. This allows the product terms to directly control the outputs of the PAL (Figure 10). One product term is used to enable the three-state buffer, which in turn gates the summation term to the output pin. The output is also fed back into the PAL array as an input. Thus the PAL drives the I/O pin when the three-state gate is enabled; the I/O pin is an input to the PAL array when the three-state gate is disabled. This feature can be used to allocate available pins for I/O functions or to provide bi-directional output pins for operations such as shifting and rotating serial data.

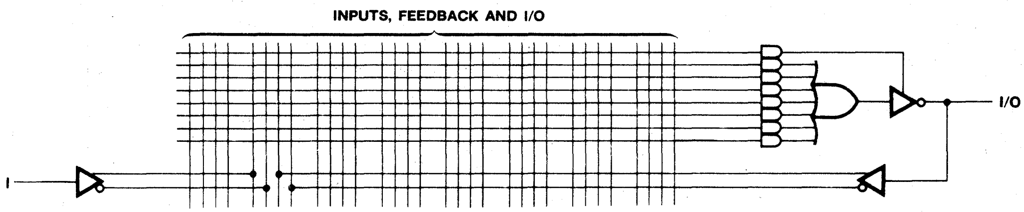


Figure 10

Registered Outputs with Feedback

Another feature of the high end members of the PAL family is registered data outputs with registered feedback. Each product term is stored into a D-type output flip-flop on the rising edge of the system clock (Figure 11). The Q output of the flip-flop can then be gated to the output pin by enabling the active low three-state buffer.

In addition to being available for transmission, the Q output is fed back into the PAL array as an input term. This feedback allows the PAL to "remember" the previous state, and it can alter its function based upon that state. This allows the designer to configure the PAL as a state sequencer which can be programmed to execute such elementary functions as count up, count down, skip, shift, and branch. These functions can be executed by the registered PAL at rates of up to 25 MHz.

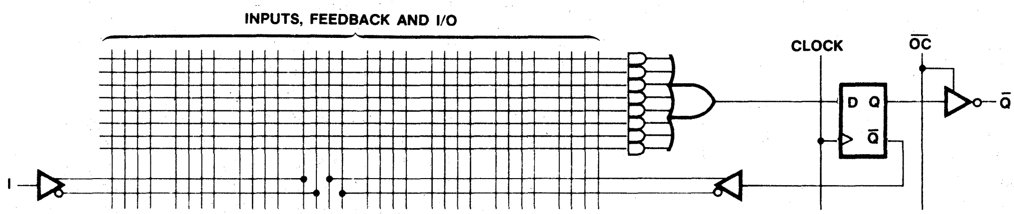


Figure 11

XOR PALs

These PAL devices feature an exclusive OR function. The sum of products is segmented into two sums which are then exclusive ORed (XOR) at the input of the D-type flip-flop (Figure 12). All of the features of the Registered PALs are included in the XOR PAL unit. The XOR function provides an easy implementation of the HOLD operation used in counters and other state sequencers.

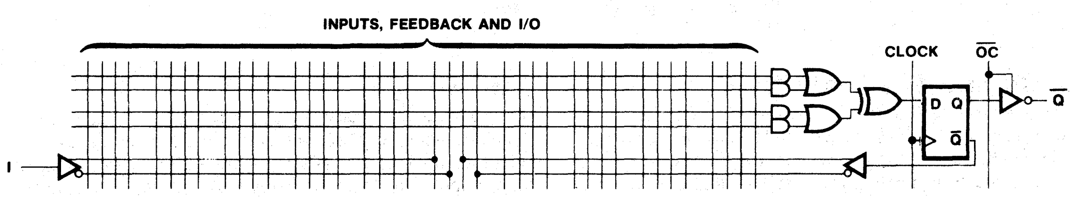


Figure 12

Arithmetic Gated Feedback

The arithmetic functions (add, subtract, greater than, and less than) are implemented by addition of gated feedback to the features of the XOR PAL device. The XOR at the input of the D-type flip-flop allows carrys from previous operations to be XORed with two variable sums generated by the PAL array. The flip-flop Q output is fed back to be gated with input terms A (Figure 13). This gated feedback provides any one of the 16 possible Boolean combinations which are mapped in the Karnaugh map (Figure 15). Figure 14 shows how the PAL array can be programmed to perform these 16 operations. These features provide for versatile operations on two variables and facilitate the parallel generation of carrys necessary for fast arithmetic operations.

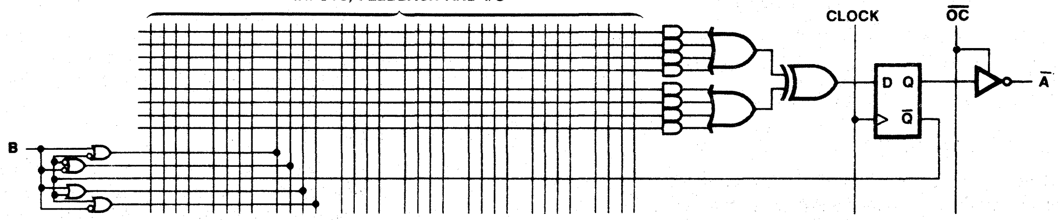


Figure 13

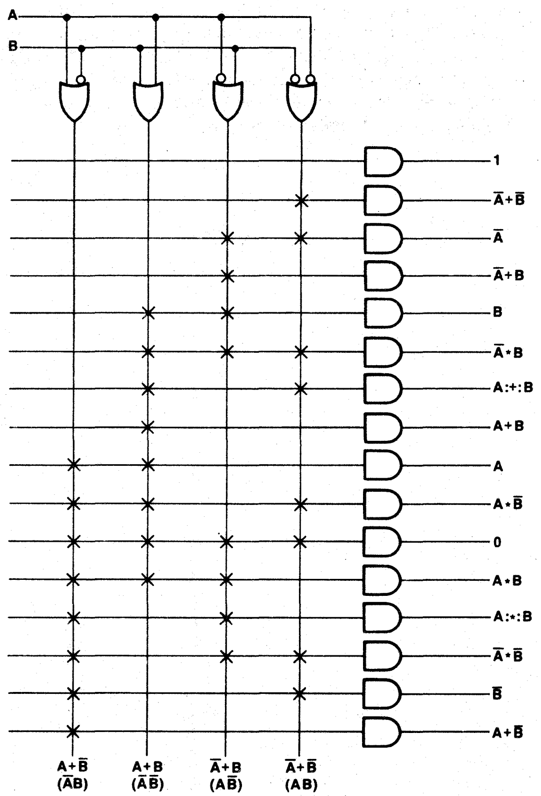


Figure 14

$(\overline{A}+B), (\overline{A}+\overline{B})$ / $(A+\overline{B}), (A+B)$	--	-x	xx	x-
--	1	$\overline{A}+\overline{B}$	$\overline{A}$	$\overline{A}+B$
-x	A+B	A:+:B	$\overline{A}\cdot B$	B
xx	A	$A\cdot\overline{B}$	0	$A\cdot B$
x-	$A+\overline{B}$	$\overline{B}$	$\overline{A}\cdot\overline{B}$	A:+:B

Figure 15

Advanced PAL Features

For 1985, a number of new features have been incorporated into the PAL family, including:

- Programmable output polarity for active high or active low operation
- Register preload which allows complete functional testing
- Product term sharing*, a feature making the number of product terms per output user-determinable
- Register bypass facilitating registered or combinatorial outputs
- Asynchronous clocks, sets, resets and output enables

A full description of each function is given on page 5-17.

PAL Programming

PAL devices can be programmed in most standard PROM programmers with the addition of a PAL personality card. The PAL appears to the programmer as a PROM. During programming half of the PAL outputs are selected for programming while the other outputs and the inputs are used for addressing. The outputs are then switched to program the other locations. Verification uses the same procedure with the programming lines held in a low state.

PALASM (PAL Assembler)

PALASM is the software used to define, simulate, build, and test PAL units. PALASM accepts the PAL Design Specification as an input file. It verifies the design against an optional function table and generates the fuse plot which is used to program the PAL devices. PALASM is available upon request for many computers and is documented in the PAL Design Concepts section.

HAL (Hard Array Logic)

The HAL family is the mask programmed version of a PAL. The HAL is to a PAL just as a ROM is to a PROM. A standard wafer is fabricated to the 6th mask. Then a custom metal mask is used to fabricate Aluminum links for a HAL instead of the programmable Ti-W fuse array used in a PAL.

The HAL is a cost-effective solution for large quantities and is unique in that it is a gate array with a programmable prototype.

PAL Technology

PAL circuits are manufactured using the proven TTL Schottky bipolar Ti-W fuse process to make fusible-link PROMs. An NPN emitter follower array forms the programmable AND array. PNP inputs provide high impedance inputs (0.25 mA max) to the array. All outputs are standard TTL drivers with internal active pull-up transistors. Typical PAL propagation delay time is less than 25 ns.

PAL Data Security

The circuitry used for programming and logic verification can be used at any time to determine the logic pattern stored in the PAL array. For security, the PAL has a "last fuse" which can be blown to disable the verification logic. This provides a significant deterrent to potential copiers, and it can be used to effectively protect proprietary designs.

* Patent pending

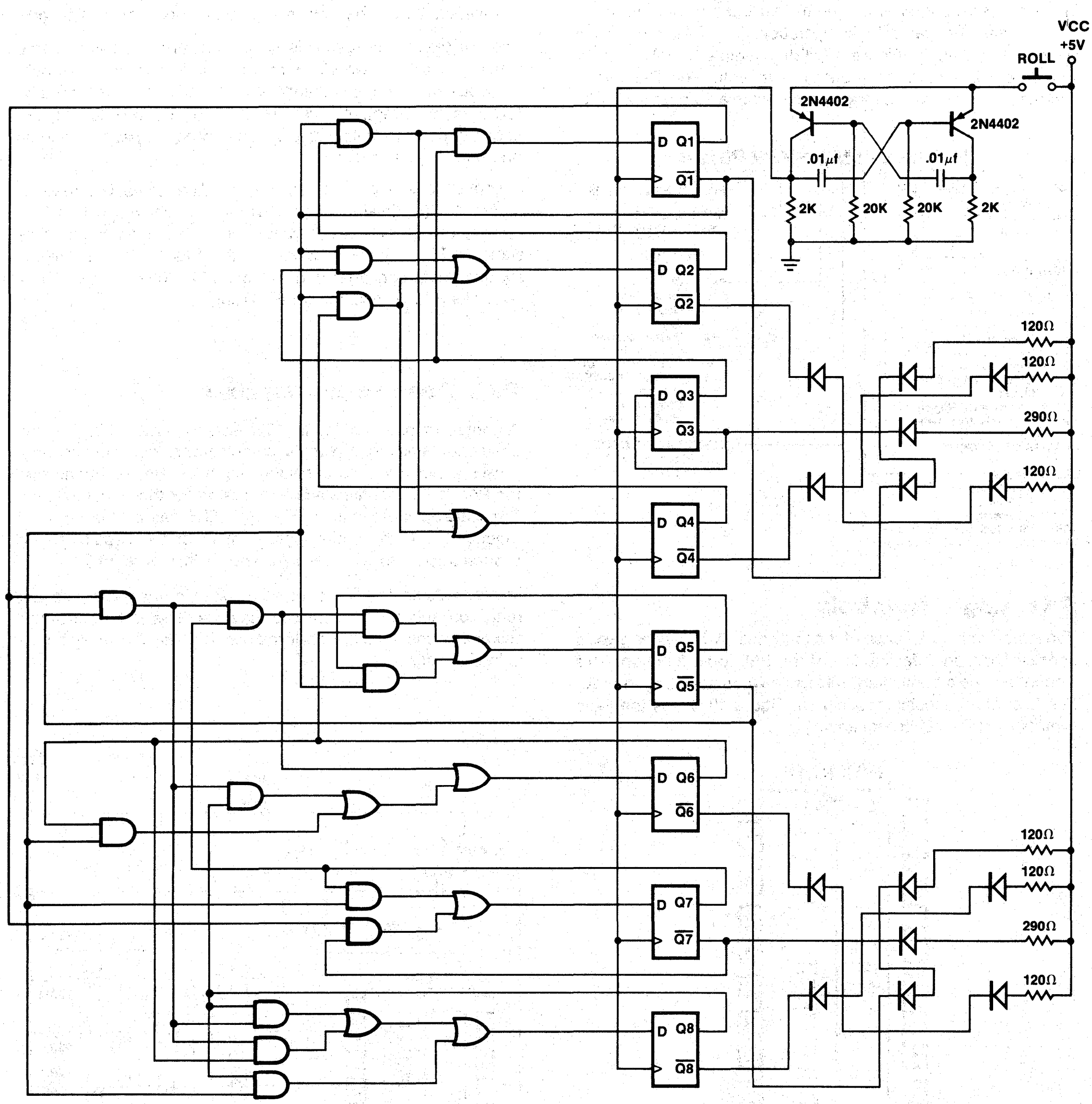
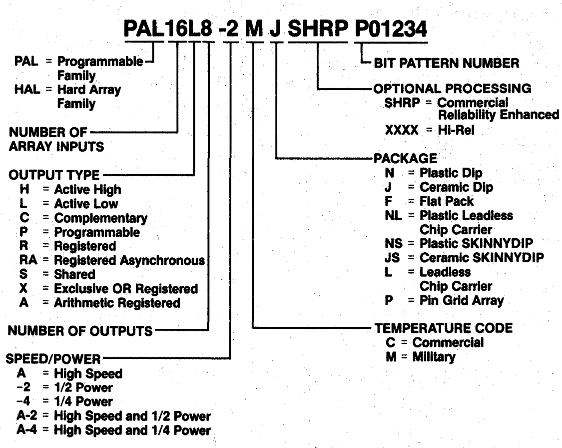

VCC
+5V
ROLL
2N4402
2N4402
.01μf
.01μf
2K
20K
20K
2K
D Q1
Q̅1
D Q2
Q̅2
D Q3
Q̅3
D Q4
Q̅4
D Q5
Q̅5
D Q6
Q̅6
D Q7
Q̅7
D Q8
Q̅8
120Ω
120Ω
290Ω
120Ω
120Ω
120Ω
290Ω
120Ω

Figure 16

PAL Part Numbers

The PAL part number is unique in that the part number code also defines the part's logic operation. The PAL parts code system is shown in Figure 17. For example, a PAL14L4CN would be a 14 input term, 4 output term, active-low PAL with a commercial temperature range packaged in a 20-pin plastic dip.



PAL Logic Symbols

The logic symbols for each of the individual PAL devices gives a concise functional description of the PAL logic function. This symbol makes a convenient reference when selecting the PAL that best fits a specific application. Figure 18 shows the logic symbol for a PAL10H8 gate array.

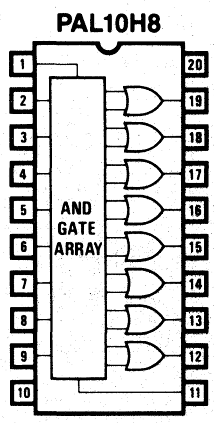


Figure 18

A PAL Example

As an example of how the PAL enables the designer to reduce costs and simplify logic design, consider the design of a simple, high-volume consumer product: an electronic dice game. This type of product will be produced in extremely high volume, so it is essential that every possible production cost be minimized.

The electronic dice game is simply constructed using a free running oscillator whose output is used to drive two asynchronous modulo six counters. When the user "rolls" the dice (presses a button), the current state of the counters is decoded and latched into a display resembling the pattern seen on an ordinary pair of dice.

A conventional logic diagram for the dice game is shown in Figure 16. (A detailed logic derivation is shown in the PAL applications section of this handbook). It is implemented using standard TTL, SSI and MSI parts, with a total I.C. count of eight: six quad gate packages and two quad D-latches. Looks like a nice, clean logic design, right? Wrong!!

PAL Goes to the Casino

A brief examination of Figure 16 reveals two basic facts: first, the circuit contains mostly simple, combinatorial logic, and second, it uses a clocked state transition sequence. Remembering that the PAL family contains ample provision for these features, the PAL catalog is consulted. The PAL16R8 has all the required functions, and the entire logic content of the circuit can be programmed into a single PAL shown in Figure 19.

In this example, the PAL effected an eight to one package count reduction and a significant cost savings. This is typical of the power and cost effective performance that the PAL family brings to logic design.

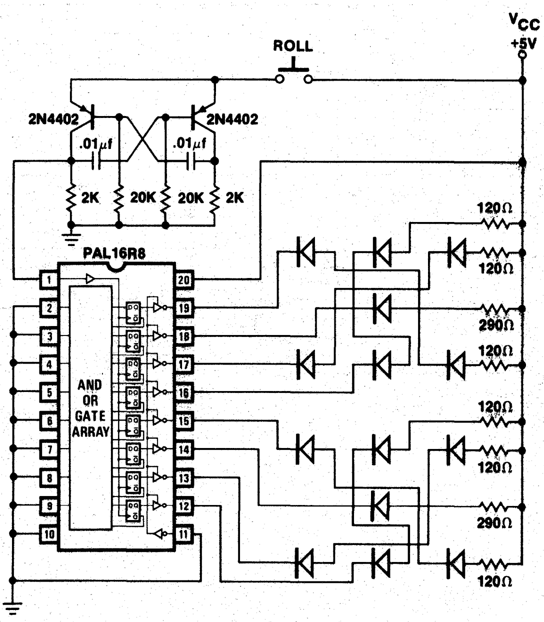
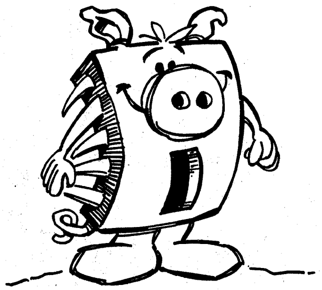


Figure 19

Advantages of Using PALs



The PAL has a unique place in the world of logic design. Not only does it offer many advantages over conventional logic, it also provides many features not found anywhere else. The PAL family:

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by at least 4 to 1.
- Expedites and simplifies prototyping and board layout.
- Saves space with 20-pin and 24-pin Skinny DIP packages.
- High speed: 15ns typical propagation delay.
- Programmed on standard PROM programmers.
- Programmable three-state outputs.
- Special feature eliminates possibility of copying by competitors.

All of these features combine together to lower product development costs and increase product cost effectiveness. The bottom line is that PAL units save money.

Direct Logic Replacement

In both new and existing designs the PAL can be used to replace various logic functions. This allows the designer to optimize a circuit in many ways never before possible. The PAL is particularly effective when used to provide interfaces required by many LSI functions. PAL flexibility combined with LSI function density makes a powerful team.

Design Flexibility

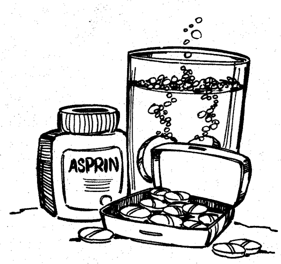
The PAL offers the systems logic designer a whole new world of options. Until now, the decision on logic system implementation was usually between SSI/MSI logic functions on one hand and microprocessors on the other. In many cases the function required is too awkward to implement the first way and too simple to justify the second. Now the PAL offers the designer high functional density, high speed, and low cost. Even better, PAL devices come in a variety of sizes and functions, thereby further increasing the designer's options.

Space Efficiency

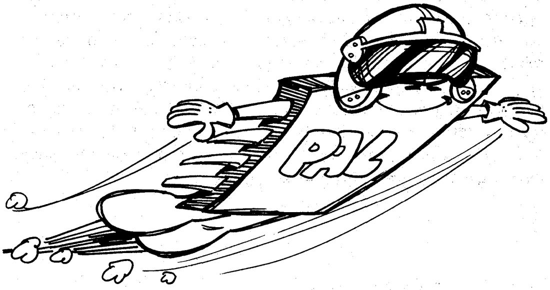
By allowing designers to replace many simple logic functions with single packages, the PAL allows more compact P.C. board layouts. The PAL space saving 20-pin and 24-pin "SKINNYDIP" helps to further reduce board area while simplifying board layout and fabrication. This means that many multi-card systems can now be reduced to one or two cards, and that can make the difference between a profitable success or an expensive disaster.

Smaller Inventory

The PAL family can be used to replace up to 90% of the conventional TTL family. This considerably lowers both shelving and inventory cataloging requirements. Even better, small custom modifications to the standard functions are easy for PAL users, not so easy for standard TTL users.



High Speed

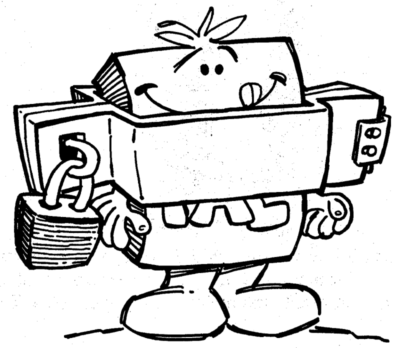


The PAL family runs faster or equal to the best of bipolar logic circuits. This makes the PAL the ideal choice for most logical operations or control sequence which requires a medium complexity and high speed. Also, in many microcomputer systems, the PAL can be used to handle high speed data interfaces that are not feasible for the microprocessor alone. This can be used to significantly extend the capabilities of the low-cost, low-speed NMOS microprocessors into areas formerly requiring high-cost bipolar microprocessors.

Easy Programming

The members of the PAL family can be quickly and easily programmed using standard PROM programmers. This allows designers to use PALs with a minimum investment in special equipment. Many types of programmable logic, such as the FPLA, require an expensive, dedicated programmer.

Secure Data

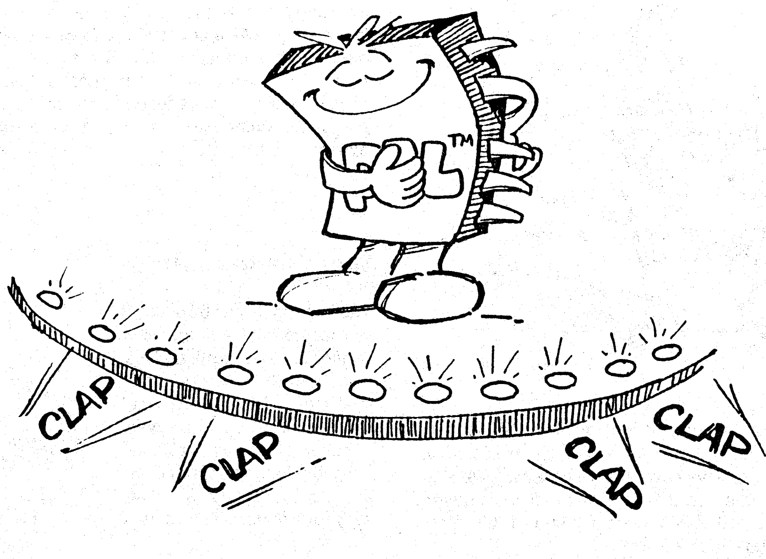


The PAL verification logic can be completely disabled by blowing out a special "last link." This prevents the unauthorized copying of valuable data, and makes the PAL perfect for use in any application where data integrity must be carefully guarded.

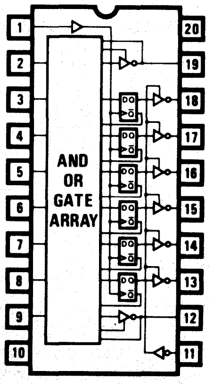
Summary

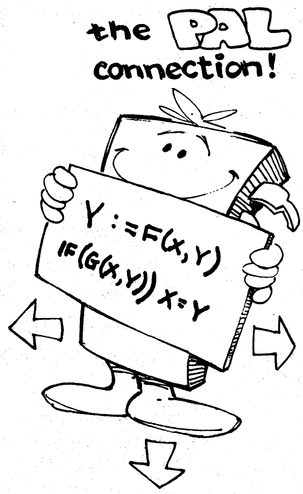
The PAL family of logic devices offers logic designers new options in the implementation of sequential and combinatorial logic designs. The family is fast, compact, flexible, and easy to use in both new and existing designs. It promises to reduce costs in most areas of design and production with a corresponding increase in product profitability.

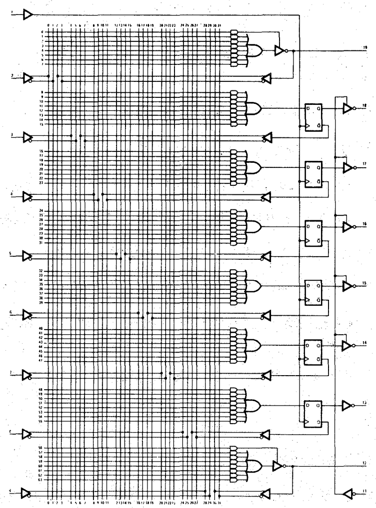
A Great Performer!



PAL16R6



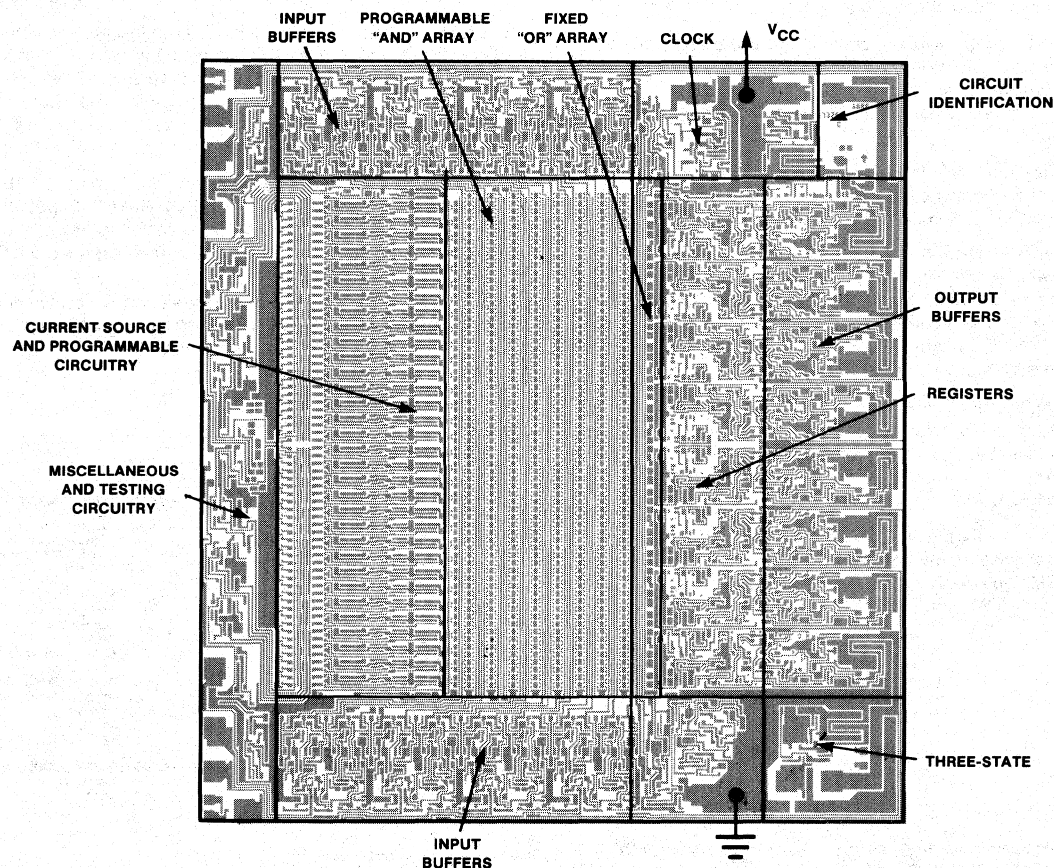




PAL16R6 Logic Symbols

PAL16R6 Logic Diagram

5



PAL 16R6 Metalization

PAL®-Programmable Array Logic
HAL®-Hard Array Logic

Features/Benefits

- **Reduces SSI/MSI chip count greater than 5 to 1**
- **Saves space with SKINNYDIP® packages**
- **Reduces IC inventories substantially**
- **Expedites and simplifies prototyping and board layout**
- **PALASM™ silicon compiler provides auto routing and test vectors**
- **Security fuse reduces possibility of copying by competitors**

Description

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The HAL family utilizes standard Low-Power Schottky TTL process and automated mask pattern generation directly from logic equations to provide a semi-custom gate array for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

There are four different speed/power families offered. Choose from either the standard, high speed, half power, or quarter power family to maximize design performance.

The PAL/HAL lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array).

The HAL transfer function is the familiar sum of products. Like the ROM, the HAL has a single array of selectable gates. Unlike the ROM, the HAL is a selectable AND array driving a fixed OR array (the ROM is a fixed AND array driving a selectable OR array).

PAL®, (Programmable Array Logic), PALASM®, HAL®, and SKINNYDIP® are registered trademarks and PMSI, and HMSI are trademarks of Monolithic Memories Inc.

In addition the PAL/HAL provides these options:

- **Variable input/output pin ratio**
- **Programmable three-state outputs**
- **Registers with feedback**
- **Arithmetic capability**
- **Exclusive-OR gates**
- **Other options identified on page 5-17**

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low-to-high transition of the clock. PAL/HAL Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets.

The entire PAL family is programmed using inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

To design a HAL, the user first programs and debugs a PAL using PALASM and the "PAL DESIGN SPECIFICATION" standard format. This specification is submitted to Monolithic Memories where it is computer processed and assigned a bit pattern number, e.g., P01234.

Monolithic Memories will provide a PAL sample for customer qualification. The user then submits a purchase order for a HAL of the specified bit pattern number, e.g., HAL18L4 P01234. See Ordering Information below.

Ordering Information

PAL16L8 -2 M J SHRP P01234

PAL = Programmable Family
HAL = Hard Array Family

NUMBER OF ARRAY INPUTS

OUTPUT TYPE
- H = Active High
- L = Active Low
- C = Complementary
- P = Programmable
- R = Registered
- RA = Registered Asynchronous
- S = Shared
- X = Exclusive OR Registered
- A = Arithmetic Registered

NUMBER OF OUTPUTS

SPEED/POWER
- A = High Speed
- -2 = 1/2 Power
- -4 = 1/4 Power
- A-2 = High Speed and 1/2 Power
- A-4 = High Speed and 1/4 Power

BIT PATTERN NUMBER

OPTIONAL PROCESSING
- SHRP = Commercial Reliability Enhanced
- XXXX = Hi-Rel

PACKAGE
- N = Plastic Dip
- J = Ceramic Dip
- F = Flat Pack
- NL = Plastic Leadless Chip Carrier
- NS = Plastic SKINNYDIP
- JS = Ceramic SKINNYDIP
- L = Leadless Chip Carrier
- P = Pin Grid Array

TEMPERATURE CODE
- C = Commercial
- M = Military

Register Bypass

Outputs within a bank must either be all registered or all combinatorial. Whether or not a bank of registers is bypassed depends on how the outputs are defined in the equations. A colon followed by an equal sign [:=] specifies a registered output with feedback which is updated after the low-to-high transition of the clock. An equal sign [=] defines a combinatorial output which bypasses the register. Registers are bypassed in banks of eight. Bypassing a bank of registers eliminates the feedback lines for those outputs.

Output Polarity

Output polarity is defined by comparison of the pin list and the equations. If the logic sense of a specific output in the pin list is different from the logic sense of that output as defined by its equation, the output is inverted or active low polarity. If the logic sense of a specific output in the pin list is the same as the logic sense of that output as defined by its equation, the output is active high polarity.

Product Term Sharing

The basic configuration is sixteen product terms shared between two output cells. For a typical output pair, each product term can be used by either output; but, since product term sharing is exclusive, a product term can be used by only one output, not both. If equations call for an output pair to use the same product term, two product terms are generated, one for each output. This should be taken into account when writing equations. PAL assemblers configure product terms automatically.

This example uses the 84-pin package. Four output equations are shown to demonstrate functionality. Pin names are arbitrary.

Product Term Editing

A unique feature of product term sharing is the ability to edit the design after the device has been programmed. Without this feature, a new PAL device had to be programmed if the user needed to change his design. Product term editing allows the user to delete an unwanted product term and reprogram a previously unused product term to the desired fuse pattern. This feature is made possible by the product term sharing architecture. Since each product term can be routed to either output in a given pair by selecting one of two steering fuses, it is possible to blow both of the steering fuses thereby completely disabling that product term. Once disabled, that product term is powered down, saving typically 0.25 mA. The desired change may now be programmed into one of the previously unused product terms corresponding to that output pair. Additional edits can be made as long as there are unused product terms for the output in question.

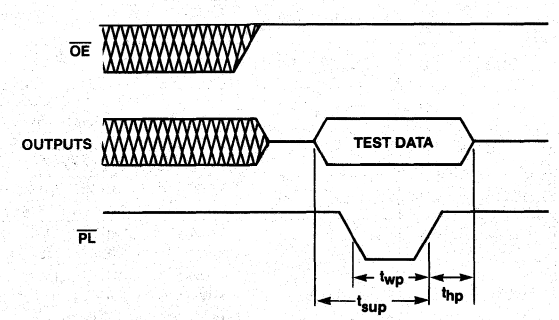
PRESET Feature (PAL64R32 only)

Register banks of eight may be PRESET to all highs on the outputs by setting the PRESET pin (PS) to a Low level. Note from the Logic Diagram that when the state of an output is High, the state of the register is Low due to the inverting tri-state buffer.

PAL Testability Features

Preload pins have been added to enable the testability of each state in state-machine design. Typically, for a modulo-n counter or a state machine there are many unreachable states for the registers. These states, and the logic which controls them are untestable without a way to "set-in" the desired starting state of the registers. In addition, long test sequences are sometimes needed to test a state machine simply to reach those starting states which are legal. Since complete logic verification is needed to ensure the proper exit from "illegal" or unused states, a way to enter these states must be provided. The ability to preload a given bank of registers is provided in this device.

To use the preload feature, several steps must be followed. First, a high level on an assertive-low output enable pin disables the outputs for that bank of registers. Next, the data to be loaded is presented at the output pins. This data is then loaded into the register by placing a low level on the PRELOAD pin. PRELOAD is asynchronous with respect to the clock.



Programmable Set and Reset (PAL20RA10 only)

In each SMAC, two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1. If the reset product line is high, the register output becomes a logic 0. The operation of the programmable set and reset overrides the clock.

Individually Programmable Register Bypass (PAL20RA10 only)

If both the set and reset product lines are high, the sum-of-products bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode.

Programmable Clock (PAL20RA10 only)

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others.

PAL Input/Output/Function/Performance Chart

GENERIC LOGIC	PINS	PACKAGE	DESCRIPTION	PART NUMBER			
				STANDARD	HIGH SPEED	1/2 POWER	1/4 POWER
10H8	20	N,J,F,L,NL	Octal 10 Input And-Or Gate Array	PAL10H8 HAL10H8		PAL10H8-2 HAL10H8-2	
12H6	20	N,J,F,L,NL	Hex 12 Input And-Or Gate Array	PAL12H6 HAL12H6		PAL12H6-2 HAL12H6-2	
14H4	20	N,J,F,L,NL	Quad 14 Input And-Or Gate Array	PAL14H4 HAL14H4		PAL14H4-2 HAL14H4-2	
16H2	20	N,J,F,L,NL	Dual 16 Input And-Or Gate Array	PAL16H2 HAL16H2		PAL16H2-2 HAL16H2-2	
16C1	20	N,J,F,L,NL	16 Input And-Or/Nor Gate Array	PAL16C1 HAL16C1		PAL16C1-2 HAL16C1-2	
10L8	20	N,J,F,L,NL	Octal 10 Input And-Or Invert Gate Array	PAL10L8 HAL10L8		PAL10L8-2 HAL10L8-2	
12L6	20	N,J,F,L,NL	Hex 12 Input And-Or-Invert Gate Array	PAL12L6 HAL12L6		PAL12L6-2 HAL12L6-2	
14L4	20	N,J,F,L,NL	Quad 14 Input And-Or-Invert Gate Array	PAL14L4 HAL14L4		PAL14L4-2 HAL14L4-2	
16L2	20	N,J,F,L,NL	Dual 16 Input And-Or-Invert Gate Array	PAL16L2 HAL16L2		PAL16L2-2 HAL16L2-2	
16L8	20	N,J,F,L,NL	Octal 16 Input And-Or-Invert Gate Array	PAL16L8 HAL16L8	PAL16L8A HAL16L8A	PAL16L8A-2 HAL16L8A-2	PAL16L8A-4 HAL16L8A-4
16R8	20	N,J,F,L,NL	Octal 16 Input Registered And-Or Invert Gate Array	PAL16R8 HAL16R8	PAL16R8A HAL16R8A	PAL16R8A-2 HAL16R8A-2	PAL16R8A-4 HAL16R8A-4
16R6	20	N,J,F,L,NL	Hex 16 Input Registered And-Or Invert Gate Array	PAL16R6 HAL16R6	PAL16R6A HAL16R6A	PAL16R6A-2 HAL16R6A-2	PAL16R6A-4 HAL16R6A-4
16R4	20	N,J,F,L,NL	Quad 16 Input Registered And-Or Invert Gate Array	PAL16R4 HAL16R4	PAL16R4A HAL16R4A	PAL16R4A-2 HAL16R4A-2	PAL16R4A-4 HAL16R4A-4
16X4	20	N,J,F,L,NL	Quad 16 Input Registered And-Or-Xor Invert Gate Array	PAL16X4 HAL16X4			
16A4	20	N,J,F,L,NL	Quad 16 Input Registered And-Carry-Or-Xor Invert Gate Array	PAL16A4 HAL16A4			
12L10	24 (28)	NS,JS,F,(L),(NL)	Deca 12 Input And-Or-Invert Gate Array	PAL12L10 HAL12L10			
14L8	24 (28)	NS,JS,F,(L),(NL)	Octal 14 Input And-Or-Invert Gate Array	PAL14L8 HAL14L8			
16L6	24 (28)	NS,JS,F,(L),(NL)	Hex 16 Input And-Or-Invert Gate Array	PAL16L6 HAL16L6			
18L4	24 (28)	NS,JS,F,(L),(NL)	Quad 18 Input And-Or-Invert Gate Array	PAL18L4 HAL18L4			
20L2	24 (28)	NS,JS,F,(L),(NL)	Dual 20 Input And-Or-Invert Gate Array	PAL20L2 HAL20L2			
20C1	24 (28)	NS,JS,F,(L),(NL)	20 Input And-Or/Nor Gate Array	PAL20C1 HAL20C1			
20L10	24 (28)	NS,JS,F,(L),(NL)	Deca 20 Input And-Or-Invert Gate Array	PAL20L10 HAL20L10			
20X10	24 (28)	NS,JS,F,(L),(NL)	Deca 20 Input Registered And-Or-Xor Invert Gate Array	PAL20X10 HAL20X10			
20X8	24 (28)	NS,JS,F,(L),(NL)	Octal 20 Input Registered And-Or-Xor Invert Gate Array	PAL20X8 HAL20X8			
20X4	24 (28)	NS,JS,F,(L),(NL)	Quad 20 Input Registered And-Or-Xor Invert Gate Array	PAL20X4 HAL20X4			
20L8	24 (28)	NS,JS,F,(L),(NL)	Octal 20 Input And-Or-Invert Gate Array		PAL20L8A HAL20L8A		
20R8	24 (28)	NS,JS,F,(L),(NL)	Octal 20 Input Registered And-Or Invert Gate Array		PAL20R8A HAL20R8A		
20R6	24 (28)	NS,JS,F,(L),(NL)	Hex 20 Input Registered And-Or Invert Gate Array		PAL20R6A HAL20R6A		
20R4	24 (28)	NS,JS,F,(L),(NL)	Quad 20 Input Registered And-Or Invert Gate Array		PAL20R4A HAL20R4A		

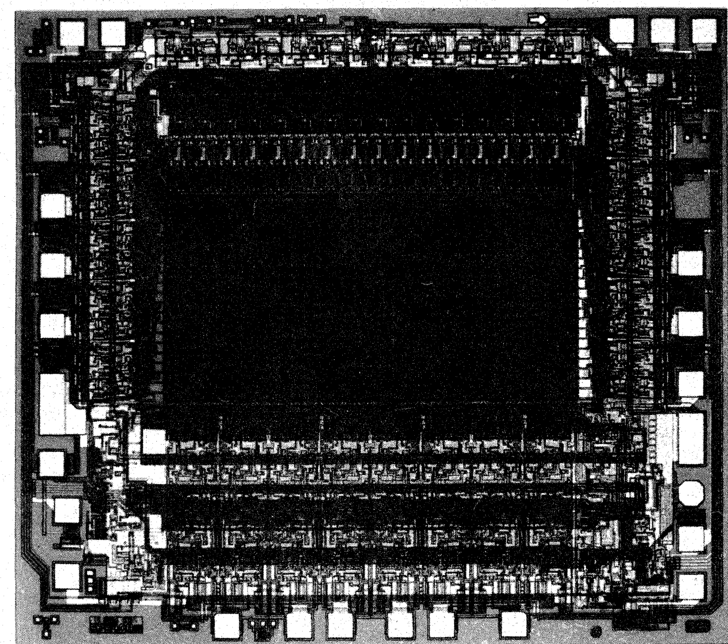
( ) = Military Product Standard.

PAL Input/Output/Function/Performance Chart

GENERIC LOGIC	PINS	PACKAGE	DESCRIPTION	PART NUMBER STANDARD	HIGH SPEED	1/2 POWER	1/4 POWER
*16P8	20	N,J,L,NL	Octal 16 Input And-Or Array w/Programmable Polarity		PAL16P8A HAL16P8A		
*16RP8	20	N,J,L,NL	Octal 16 Input Registered And-Or Array w/Programmable Polarity		PAL16RP8A HAL16RP8A		
*16RP6	20	N,J,L,NL	Hex 16 Input Registered And-Or Array w/Programmable Polarity		PAL16RP6A HAL16RP6A		
*16RP4	20	N,J,L,NL	Quad 16 Input Registered And-Or Array w/Programmable Polarity		PAL16RP4A HAL16RP4A		
20S10	24 (28)	N,J,W,(L),(NL)	Deca 20 Input And-Or Array w/Product Term Sharing		PAL20S10 HAL20S10		
20RS10	24 (28)	N,J,W,(L),(NL)	Deca 20 Input Registered And-Or Array w/Product Term Sharing		PAL20RS10 HAL20RS10		
20RS8	24 (28)	N,J,W,(L),(NL)	Octal 20 Input Registered And-Or Array w/Product Term Sharing		PAL20RS8 HAL20RS8		
20RS4	24 (28)	N,J,W,(L),(NL)	Quad 20 Input Registered And-Or Array w/Product Term Sharing		PAL20RS4 HAL20RS4		
20RA10	24 (28)	N,J,W,(L),(NL)	Deca 20 Input Registered Asynchronous And-Or Array		PAL20RA10 HAL20RA10		
32R16	40 (44)	N,J,(L),(NL)	16 Output, 32 Input Registered And-Or Gate Array		PAL32R16 HAL32R16		
64R32	84 (88)	L,(P)	32 Output, 64 Input Registered And-Or Gate Array		PAL64R32 HAL64R32		

* Contact Factory for Flat Pack

Die Configuration: PAL16L8

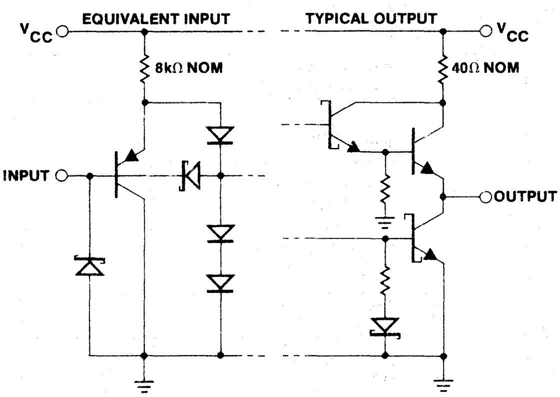


5

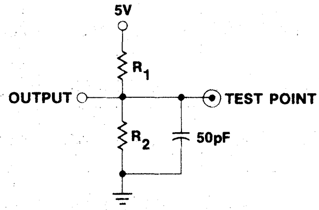
Absolute Maximum Ratings

	Operating	Programming
Supply Voltage, V_{CC}	−0.5V to 7.0V	−0.5V to 12.0V
Input Voltage	−1.5V to 5.5V	−1.0 to 22V
Off-state output Voltage	5.5V	12.0V
Storage temperature		−65° to +150°C

Schematic of Inputs and Outputs



Test Load



Other loads may be used.

Typical notes for all the following specifications (pages 5-21 — 5-39)

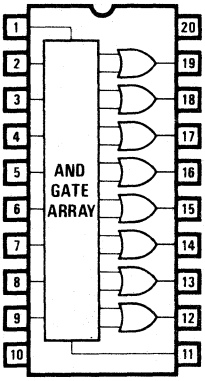
Notes: Apply to electrical and switching characteristics

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g., I_{IL} and I_{OZH}.

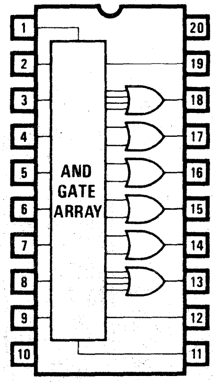
* These are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

** Only one output shorted at a time.

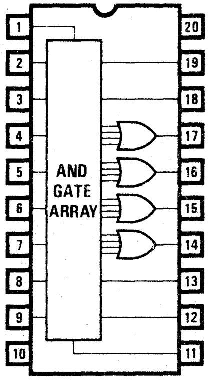
10H8



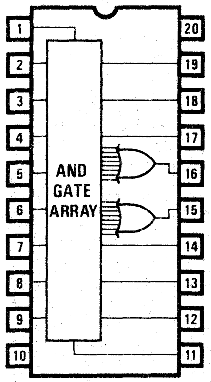
12H6



14H4



16H2



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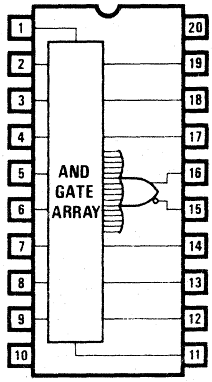
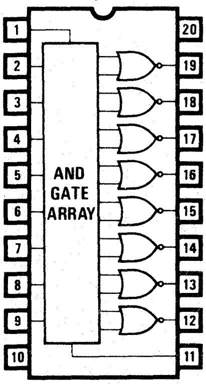


10L8



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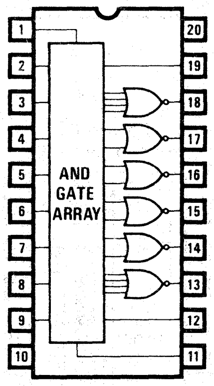

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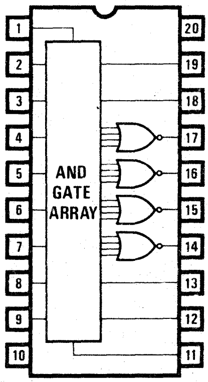

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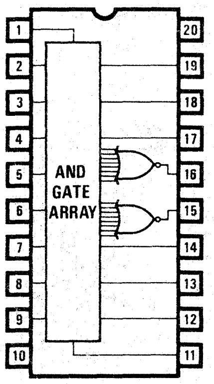

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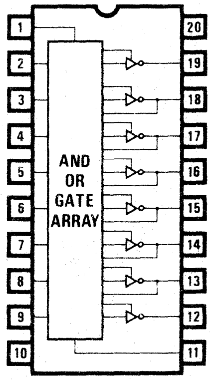

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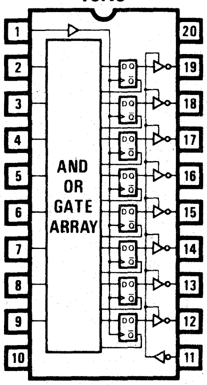

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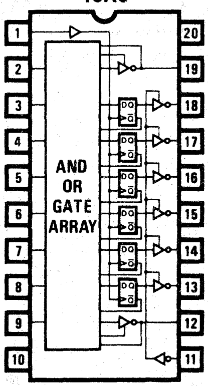

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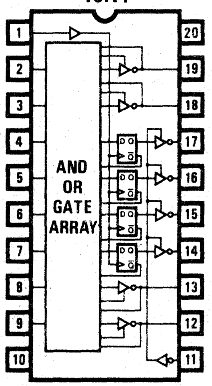

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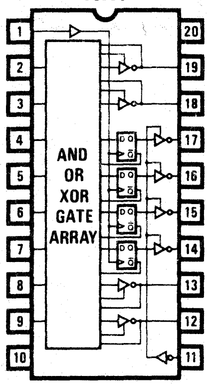

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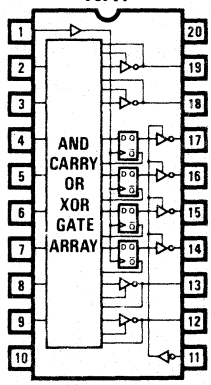
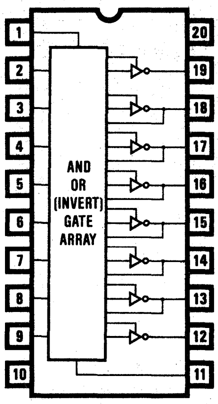
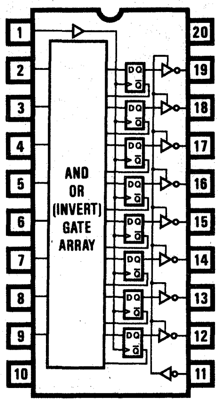


PAL16P8



PAL16RP8



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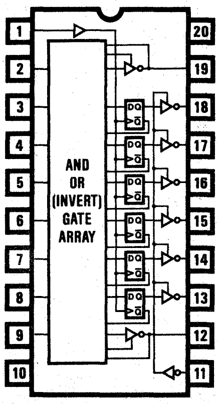

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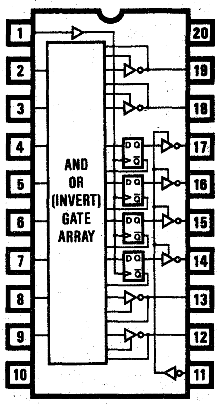
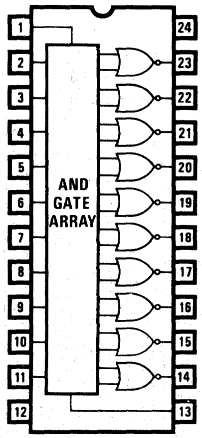


12L10



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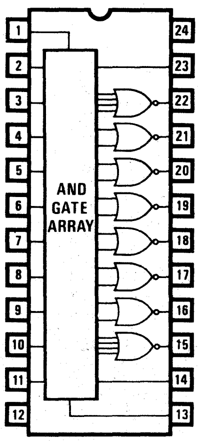

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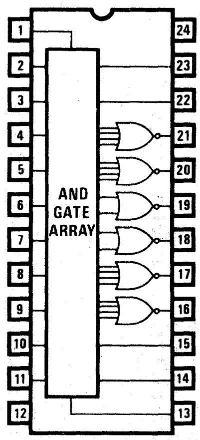

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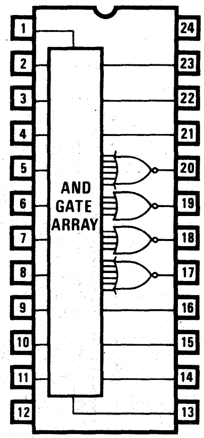

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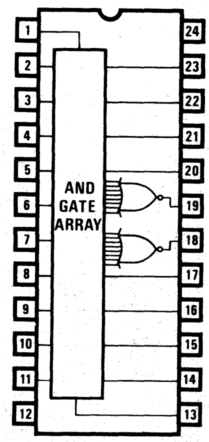

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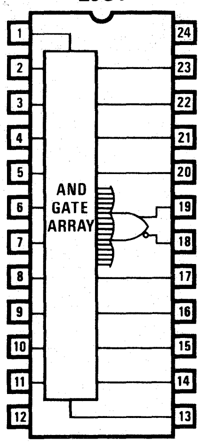

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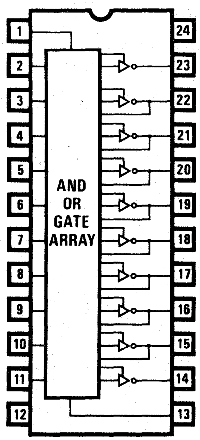

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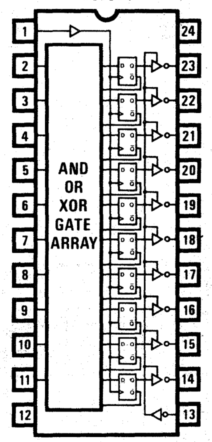

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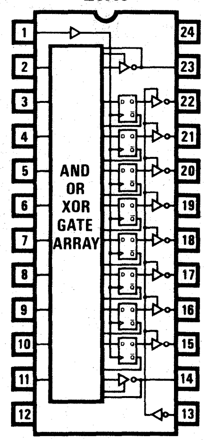

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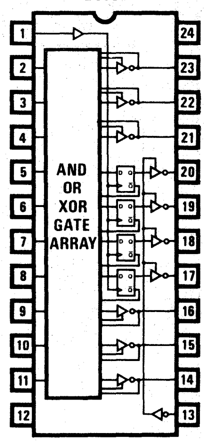

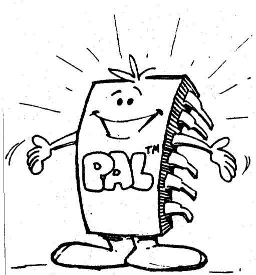

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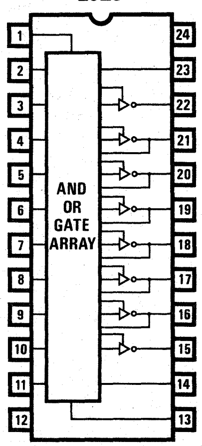

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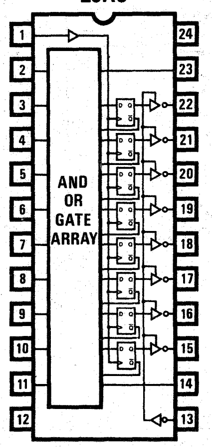

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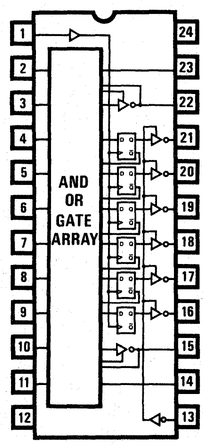

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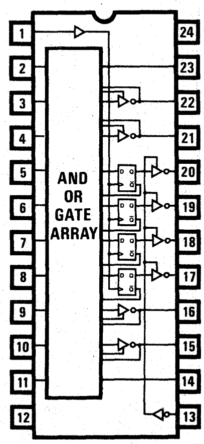

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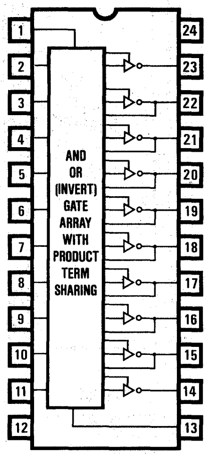

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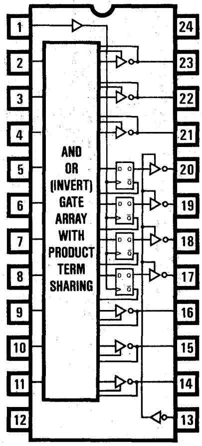

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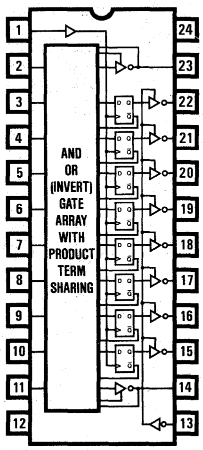

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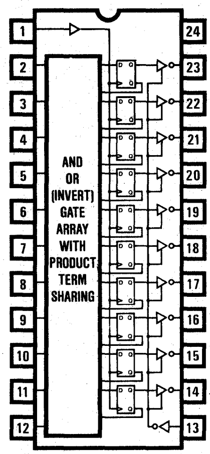

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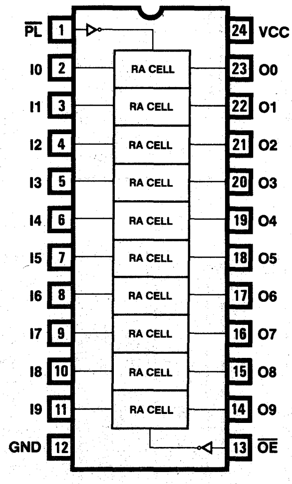
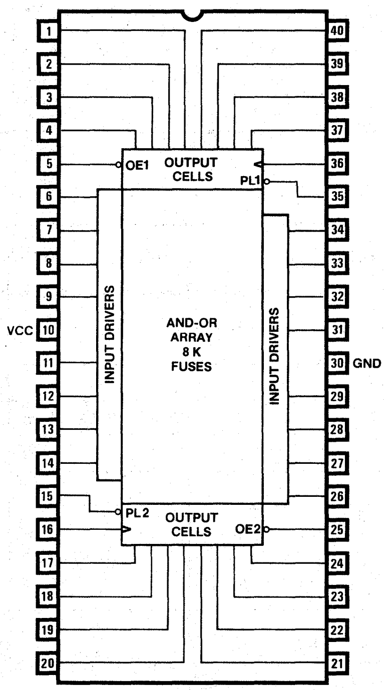
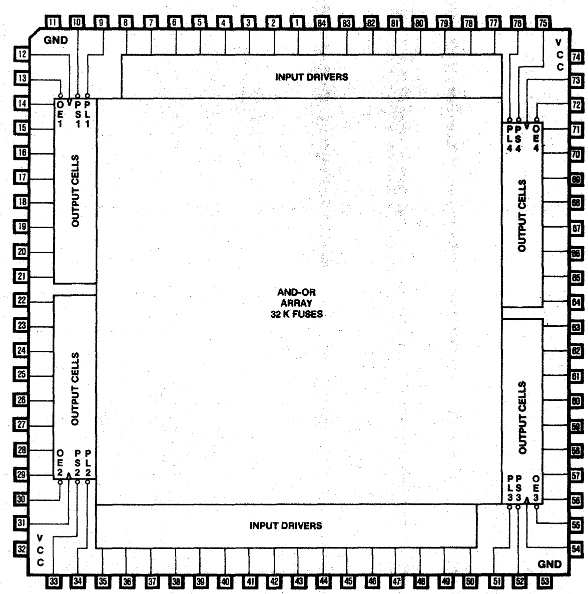


32R16



64R32



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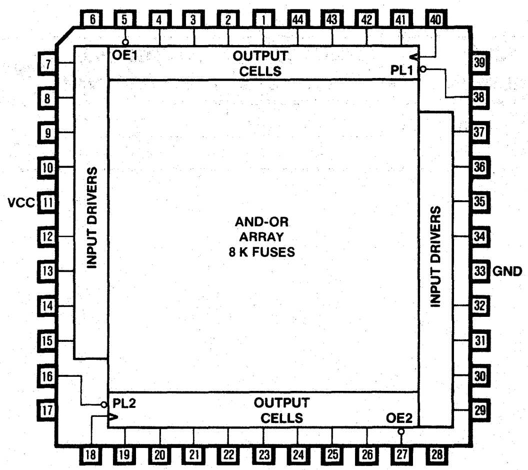
32R16



Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = –18mA		–0.8	–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V		–0.02	–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = –2mA	2.4	2.8		V
			COM	I_{OH} = –3.2mA				
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX				55	90	mA

Switching Characteristics

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	Except 16C1	R1 = 560Ω R2 = 1.1kΩ		25	45		25	35	ns
		16C1			25	45		25	40	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		-0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V		-0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	-30	-70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	R1 = 560Ω R2 = 1.1kΩ		25	45		25	40	ns

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback to clock	16R8 16R6 16R4	45	25		35	25		ns
		16X4 16A4	55	30		45	30		
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	16R4 16R6 16R8 16L8			120	180	mA
			16X4			160	225	
			16A4			170	240	

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	16R6 16R4 16L8	$R_1 = 200\Omega$ $R_2 = 390\Omega$		25	45		25	35	ns
		16X4 16A4			30	45		30	40	ns
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
t_{PZX}	Pin 11 to output enable except 16L8				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable except 16L8				15	25		15	25	ns
t_{PZX}	Input to output enable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	ns
t_{PXZ}	Input to output disable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	ns
f_{MAX}	Maximum frequency	16R8 16R6 16R4		14	25		16	25		MHz
		16X4 16A4		12	22		14	22		

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	40	20		35	20		ns
		High	30	10		25	10		ns
t_{su}	Set up time from input or feedback to clock		60	38		50	38		ns
t_h	Hold time		0	–15		0	–15		ns
T_A	Operating free-air temperature		–55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = –18mA		–0.8	–1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		–0.02	–0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = –2mA	2.4	2.8		V
			COM	I_{OH} = –3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			–100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX	20X10 20X8	20X4		120	180	mA
I_{CC}	Supply current	V_{CC} = MAX	20L10			90	165	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	$R_1 = 200\Omega$ $R_2 = 390\Omega$		35	60		35	50	ns
t_{CLK}	Clock to output or feedback			20	35		20	30	ns
$t_{PXZ/ZX}$	Pin 13 to output disable/enable except 20L10			20	45		20	35	ns
t_{PZX}	Input to output enable except 20X10			35	55		35	45	ns
t_{PXZ}	Input to output disable except 20X10			35	55		35	45	ns
f_{MAX}	Maximum frequency		10.5	16		12.5	16		MHz

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Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	10		15	10		ns
		High	20	10		15	10		ns
t_{su}	Set up time from input or feedback to clock	16R8A 16R6A 16R4A 16RP8A 16RP6A 16RP4A	30	15		25	15		ns
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	16R6A 16R4A 16L8A 16RP6A 16RP4A 16P8A	$R_1 = 200\Omega$ $R_2 = 390\Omega$		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 11 to output enable except 16L8A 16P8A				10	25		10	20	ns
t_{PXZ}	Pin 11 to output disable except 16L8A 16P8A				11	25		11	20	ns
t_{PZX}	Input to output enable	16R6A 16R4A 16L8A 16RP6A 16RP4A 16P8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	16R6A 16R4A 16L8A 16RP6A 16RP4A 16P8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	16R8A 16R6A 16R4A 16RP8A 16RP6A 16RP4A		20	40		28.5	40		MHz

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	7		15	7		ns
		High	20	7		15	7		ns
t_{su}	Set up time from input or feedback to clock	20R8A 20R6A 20R4A	30	15		25	15		ns
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V		V_O = 0V	−30	−90	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				160	210	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	20R6A 20R4A 20L8A	$R_1 = 200\Omega$ $R_2 = 390\Omega$		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 13 to output enable except 20L8A				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable except 20L8A				11	25		11	20	ns
t_{PZX}	Input to output enable	20R6A 20R4A 20L8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	20R6A 20R4A 20L8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	20R8A 20R6A 20R4A		20	40		28.5	40		MHz

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = –18mA		–0.8	–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V		–0.02	–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 4mA		0.3	0.5	V
			COM	I_{OL} = 4mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = –1mA	2.4	2.8		V
			COM	I_{OH} = –1mA				
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX				30	45	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	R1 = 1.12kΩ R2 = 2.2kΩ		45	80		45	60	ns

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback to clock	16R6A-2 16R4A-2 16R8A-2	50	25		35	25		ns
t_h	Hold time		0	–15		0	–15		ns
T_A	Operating free-air temperature		–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = –18mA		–0.8	–1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		–0.02	–0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = –2mA	2.4	2.8		V
			COM	I_{OH} = –3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			–100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V		V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	16L8A-2 16R6A-2 16R4A-2	R_1 = 200Ω R_2 = 390Ω		25	50		25	35	ns
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
$t_{PXZ/ZX}$	Pin 11 to output disable/enable except 16L8A-2				15	25		15	25	ns
t_{PZX}	Input to output enable	16L8A-2 16R6A-2 16R4A-2			25	45		25	35	ns
t_{PXZ}	Input to output disable	16R8A-2 16R6A-2 16R4A-2			25	45		25	35	ns
f_{MAX}	Maximum frequency	16R8A-2 16R6A-2 16R4A-2		14	25		16	25		MHz

Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	16R8A-4 16R6A-4 16R4A-4	Low	40	20		30	20		ns
			High	40	20		30	20		
t_{su}	Set up time from input or feedback to clock	16R8A-4 16R6A-4 16R4A-4		90	45		60	45		ns
t_h	Hold time			0	-15		0	-15		ns
T_A	Operating free-air temperature			-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		-0.8	-1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		-0.02	-0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 4mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −1mA	2.4	2.8		V
			COM	I_{OH} = −1 mA				
I_{OZL}	Off-state output current†	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX	16R4A-4 16R6A-4 16R8A-4 16L8A-4			30	50	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	16R6A-4 16R4A-4 16L8A-4	R_1 = 800Ω R_2 = 1.56kΩ		35	75		35	55	ns
t_{CLK}	Clock to output or feedback				20	45		20	35	ns
$t_{PXZ/ZX}$	Pin 11 to output disable/enable—except 16L8A-4				15	40		15	30	ns
t_{PZX}	Input to output enable	16R6A-4 16R4A-4 16L8A-4			30	65		30	50	ns
t_{PXZ}	Input to output disable	16R6A-4 16R4A-4 16L8A-4			30	65		30	50	ns
f_{MAX}	Maximum frequency	16R8A-4 16R6A-4 16R4A-4		8	18		11	18		MHz

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock		25	13		20	13		ns
t_{wp}	Preload pulse width		45	15		35	15		ns
t_{su}	Setup time for input or feedback to clock		25	10		20	10		ns
t_{sup}	Preload setup time		30	5		25	5		ns
t_h	Hold time	Polarity fuse intact	10	-2		10	-2		ns
		Polarity fuse blown	0	-6		0	-6		
t_{hp}	Preload hold time		30	5		25	5		ns
T_A	Operating free-air temperature		-55			0		75	°C
T_C	Operating case temperature				125				°C

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Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH}: Mil-2 mA Com-3.2 mA	2.4	2.8		V
I_{OZ}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V/V_O = 0.4 V	−100		100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			155	200	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	Polarity fuse intact	R_1 = 560 Ω R_2 = 1.1 KΩ		20	35		20	30	ns
		Polarity fuse blown			25	40		25	35	
t_{CLK}	Clock to output or feedback			10	17	35	10	17	30	ns
t_S	Input to asynchronous set				22	40		22	35	ns
t_R	Input to asynchronous reset				27	45		27	40	ns
t_{PZX}	Pin 13 to output enable				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable				10	25		10	20	ns
t_{PZX}	Input to output enable				18	35		18	30	ns
t_{PXZ}	Input to output disable				15	35		15	30	ns
f_{MAX}	Maximum frequency			16	35		20	35		MHz

Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low		20	10		15	10		ns
		High		20	10		15	10		
t_{su}	Setup time from input or feedback to clock	20RS10 20RS8 20RS4		40	25		35	25		ns
t_h	Hold time			0	−10		0	−10		ns
T_A	Operating free-air temperature			−55			0		75	°C
T_C	Operating case temperature					125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4 V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4 V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12 mA		0.3	0.5	V
			COM	I_{OL} = 24 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2 mA	2.4	2.8		V
			COM	I_{OH} = −3.2 mA				
I_{OZL}	Off-state output current†	V_{CC} = MAX		V_O = 0.4 V			−100	μA
I_{OZH}				V_{OL} = 2.4 mA			100	
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				175	240	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	20S10, 20RS8, 20RS4 Input or feedback to output	Polarity fuse intact	R_1 = 200 Ω R_2 = 390 KΩ		25	40		25	35	ns
		Polarity fuse blown			30	45		30	40	
t_{CLK}	Clock to output or feedback				12	20		12	17	ns
t_{PZX}	Pin 13 to output enable except 20S10				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable except 20S10				11	25		11	20	ns
t_{PZX}	Input to output enable	20S10, 20RS8, 20RS4			25	35		25	35	ns
t_{PXZ}	Input to output disable	20S10, 20RS8 20RP4			13	25		13	25	ns
f_{MAX}	20RS10, 20RS8, 20RS4 Maximum frequency			18	28		20	28		MHz

HAL PARAMETERS MAY DIFFER. CONTACT FACTORY FOR DETAILS.

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25			20			ns
		High	25			20			
t_{wp}	Preload pulse width		45			35			ns
t_{su}	Setup time for input to clock	Polarity fuse intact	50			40			ns
		Polarity fuse blown	50			40			
t_{sup}	Preload setup time		30			25			ns
t_h	Hold time		0	-10		0	-10		ns
t_{hp}	Preload hold time		10			5			ns
T_A	Operating free-air temperature		-55			0		75	°C
T_C	Operating case temperature				125				°C

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Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18 mA		-0.8	-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4 V		-0.02	-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8 mA		0.3	0.5	V
			COM	I_{OL} = 8 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2 mA	2.4	2.8		V
			COM	I_{OH} = −3.2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX		V_O = 0.4 V			-100	μA
I_{OZH}				V_O = 2.4 V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = MAX		V_O = 0 V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX				200	280	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output	Polarity fuse intact	R_1 = 560 Ω R_2 = 1.1 KΩ			50			40	ns
		Polarity fuse blown				55			45	
t_{CLK}	Clock to output or feedback					30			25	ns
t_{PZX}	Output enable					25			20	ns
t_{PXZ}	Output disable					25			20	ns
f_{MAX}	Maximum frequency			14			16			MHz

HAL PARAMETERS MAY DIFFER. CONTACT FACTORY FOR DETAILS.

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25			20			ns
		High							
t_{su}	Setup time for input to clock	Polarity fuse intact	50			40			ns
		Polarity fuse blown							
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL I_{OL} = 8 mA		0.3	0.5	V
			COM I_{OL} = 8 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −0.4 mA	2.4	2.8		V
			COM I_{OH} = −0.4 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}			V_O = 2.4 V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = MAX	V_O = 0 V	−10	−40	−60	mA
I_{CC}	Supply current	V_{CC} = MAX			400	640	mA

Switching Characteristics Over Operating Conditions

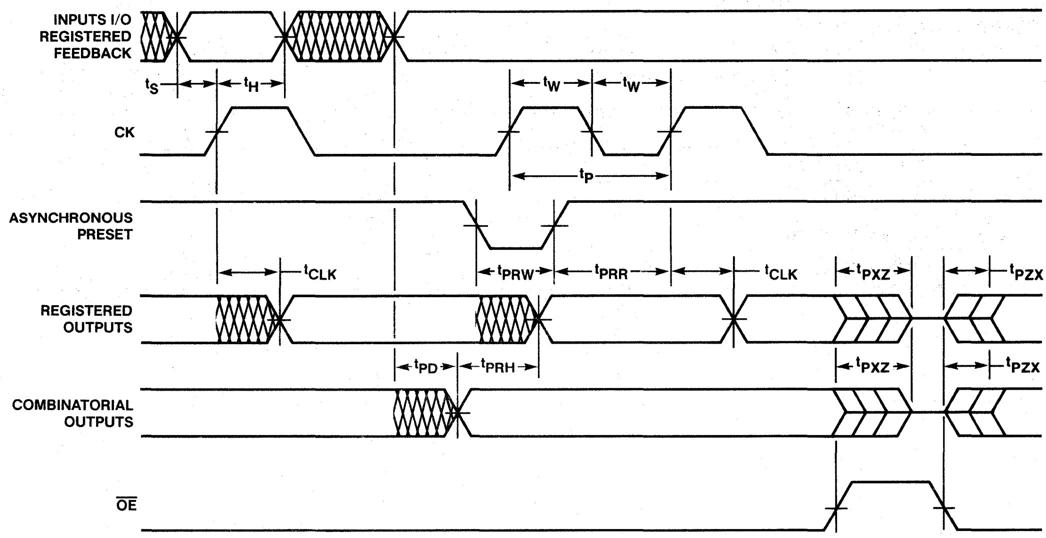
SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output	Polarity fuse intact	R_1 = 560Ω, R_2 = 1.1 KΩ			55			50	ns
		Polarity fuse blown				60			55	
t_{CLK}	Clock to output or feedback					30			22	ns
t_{PZX}	Output enable					35			30	ns
t_{PXZ}	Output disable					35			30	ns
t_{PRH}	Preset to output					40			35	ns
f_{MAX}	Maximum frequency			12.5			16	20		MHz

HAL PARAMETERS MAY DIFFER. CONTACT FACTORY FOR DETAILS.

Testing Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{wp}	Preload pulse width	45			35			ns
t_{sup}	Preload setup time	60			50			ns
t_{hp}	Preload hold time	10			5			ns
t_{PRW}	Preset pulse width	30			25			ns
t_{PRR}	Preset recovery time	40			35			ns

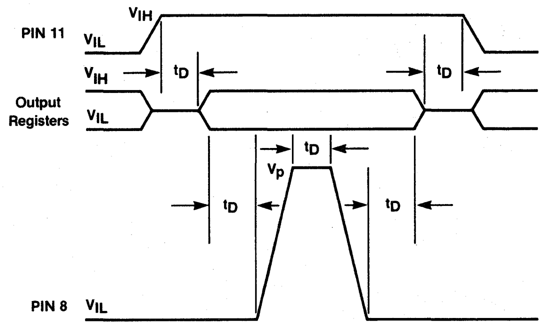
Switching Waveforms



Output Register PRELOAD Series 20AP

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing which would otherwise require a state sequencer for test coverage. The procedure for PRELOAD is as follows:

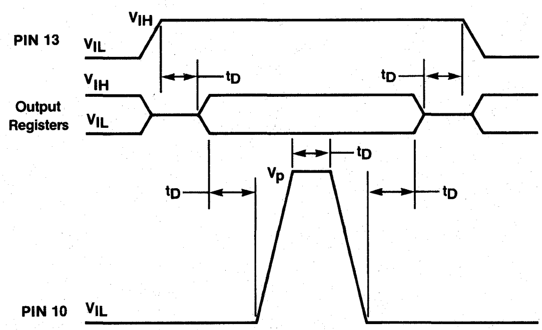
1 Raise V_{CC} to 4.5 V.
2 Disable output registers by setting pin 11 to V_{IH}.
3 Apply V_{IL}/V_{IH} to all output registers.
4 Pulse pin 8 to V_p. Then back to 0 V.
5 Remove V_{IL}/V_{IH} from all output registers.
6 Lower pin 11 to V_{IL} to enable the output registers.
7 Verify for V_{OL}/V_{OH} at all output registers.



Output Register PRELOAD Series 24RS

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing which would otherwise require a state sequencer for test coverage. The procedure for PRELOAD is as follows:

1 Raise V_{CC} to 4.5 V.
2 Disable output registers by setting pin 13 to V_{IH}.
3 Apply V_{IL}/V_{IH} to all output registers.
4 Pulse pin 10 to V_p. Then back to 0 V.
5 Remove V_{IL}/V_{IH} from all output registers.
6 Lower pin 13 to V_{IL} to enable the output registers.
7 Verify for V_{OL}/V_{OH} at all output registers.



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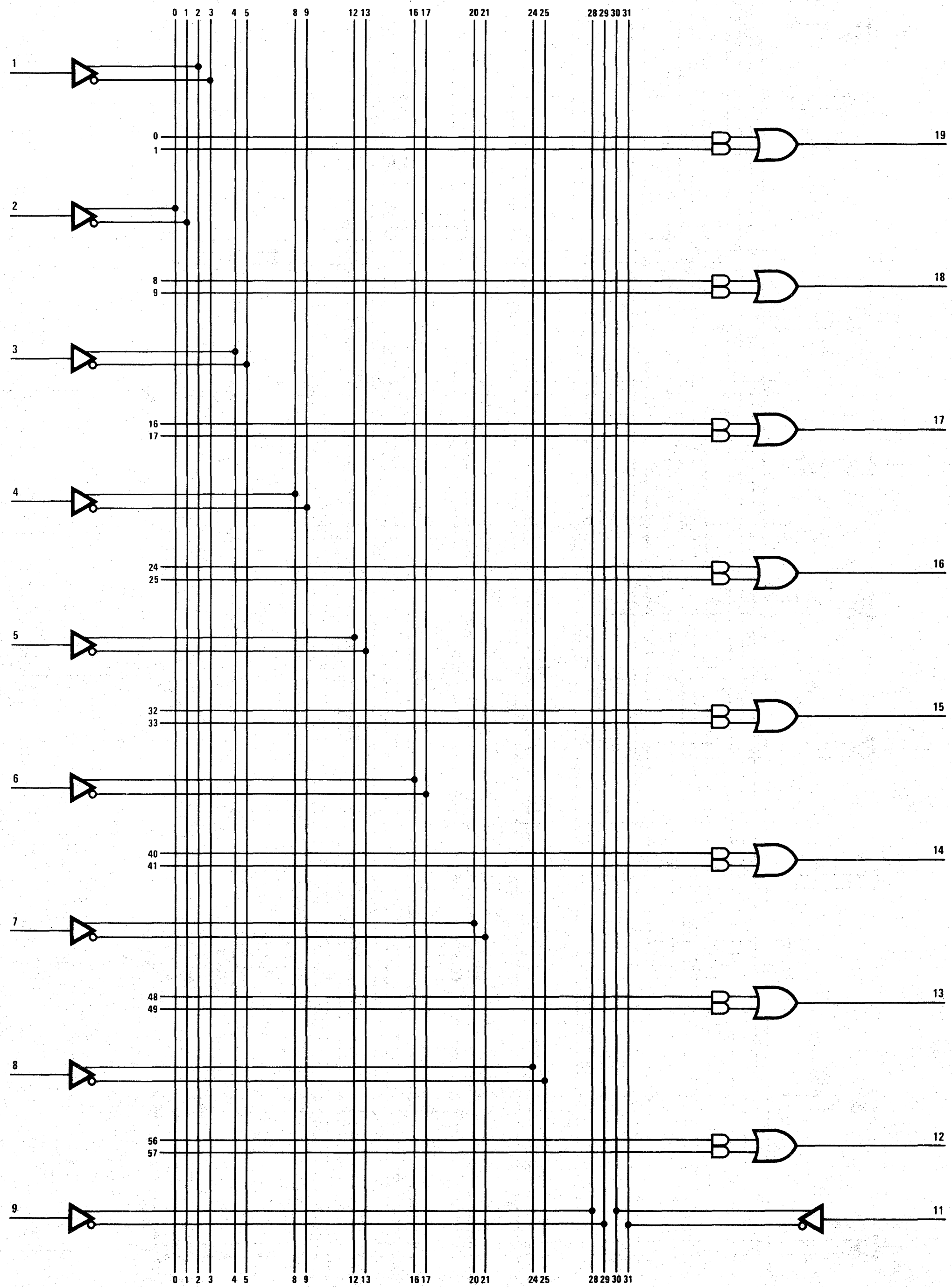
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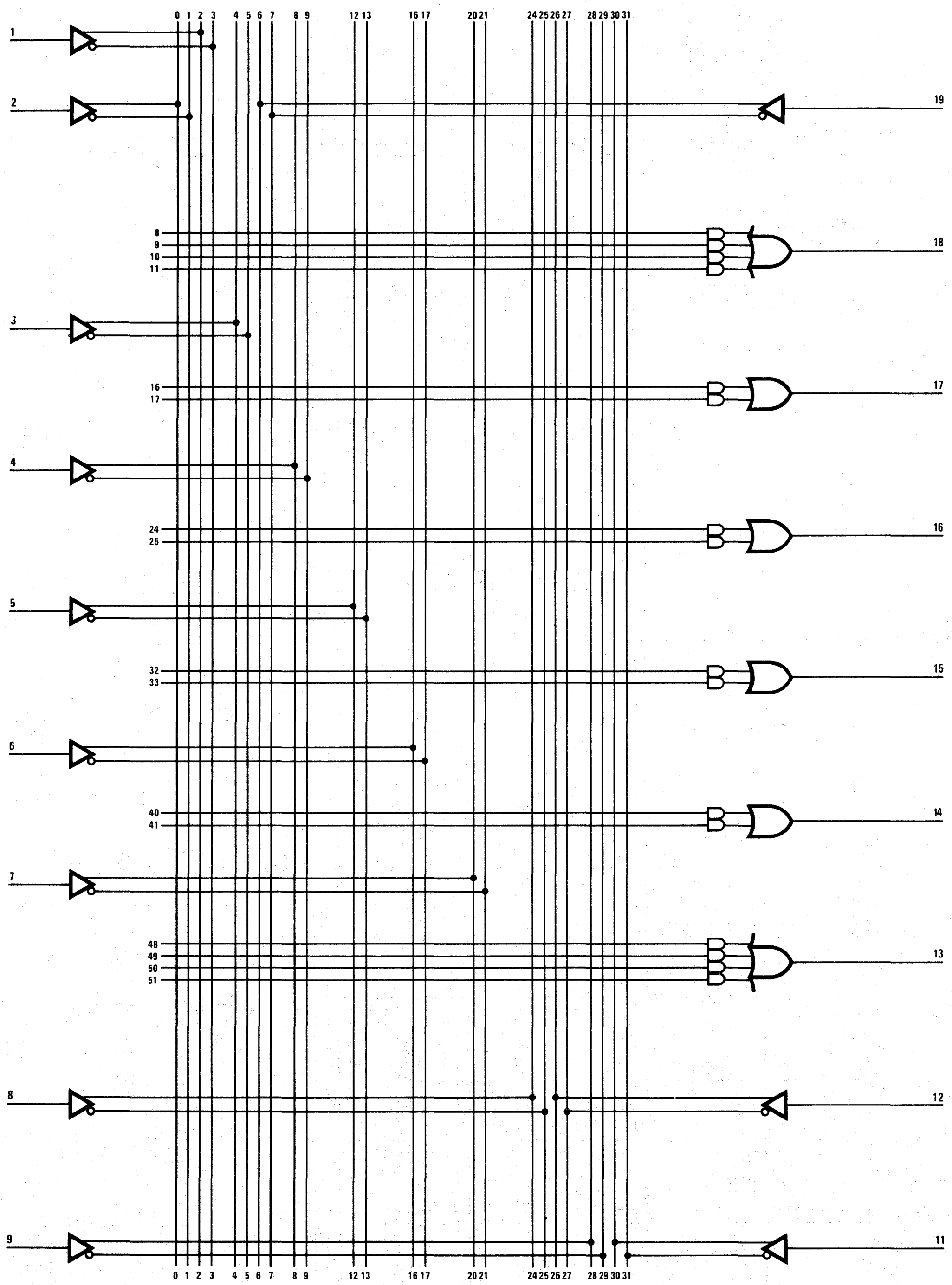

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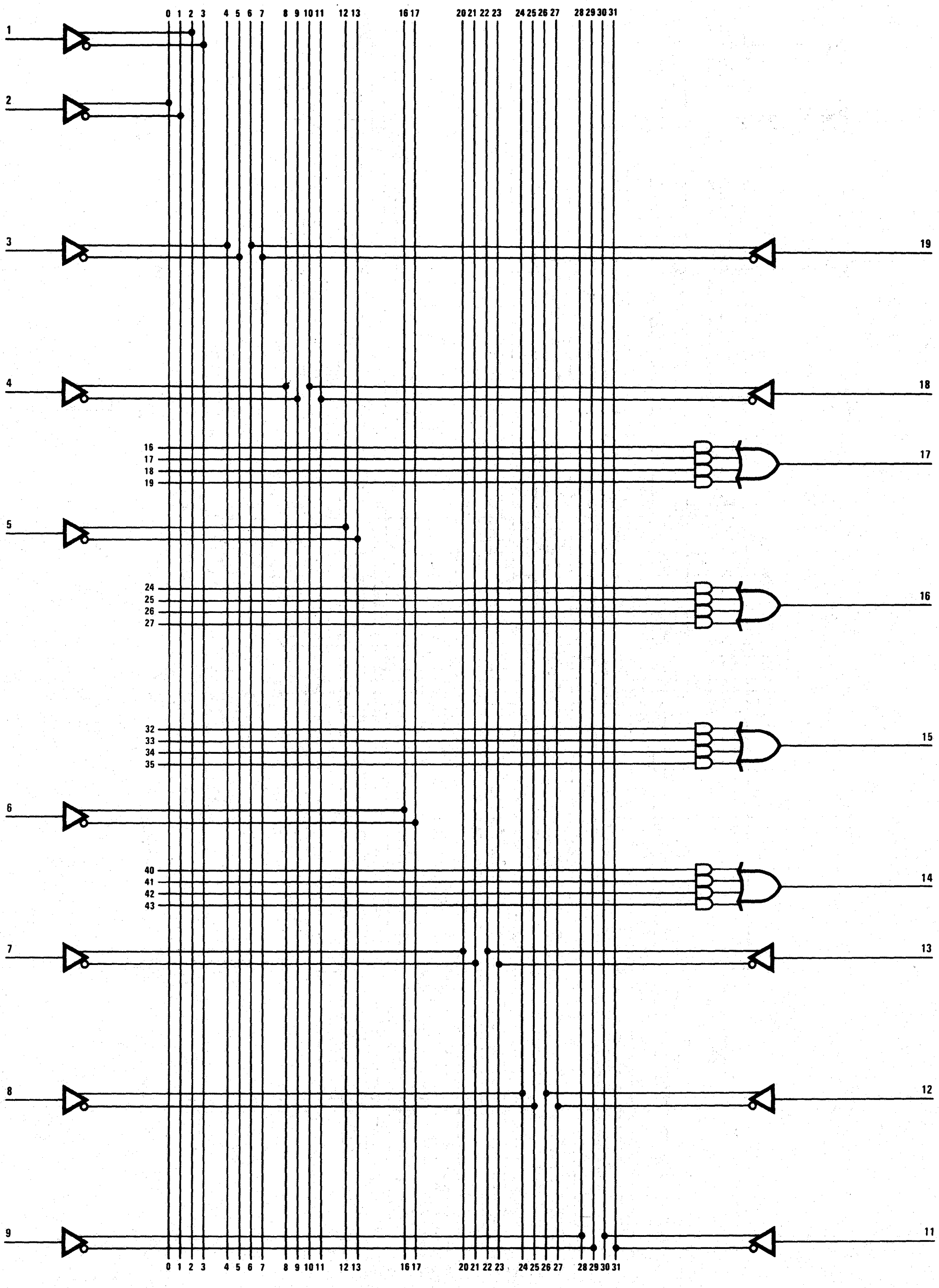
14H4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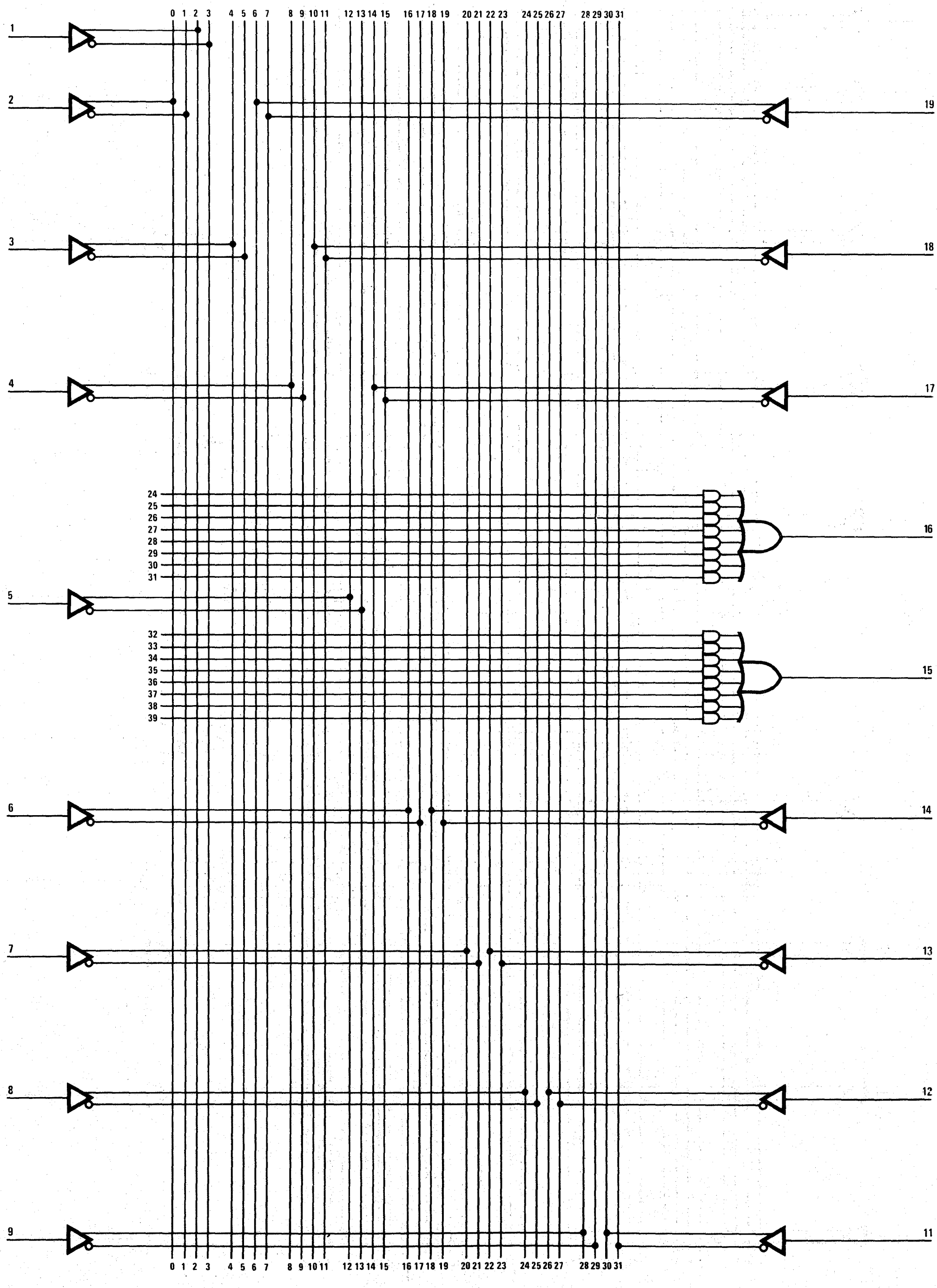
16H2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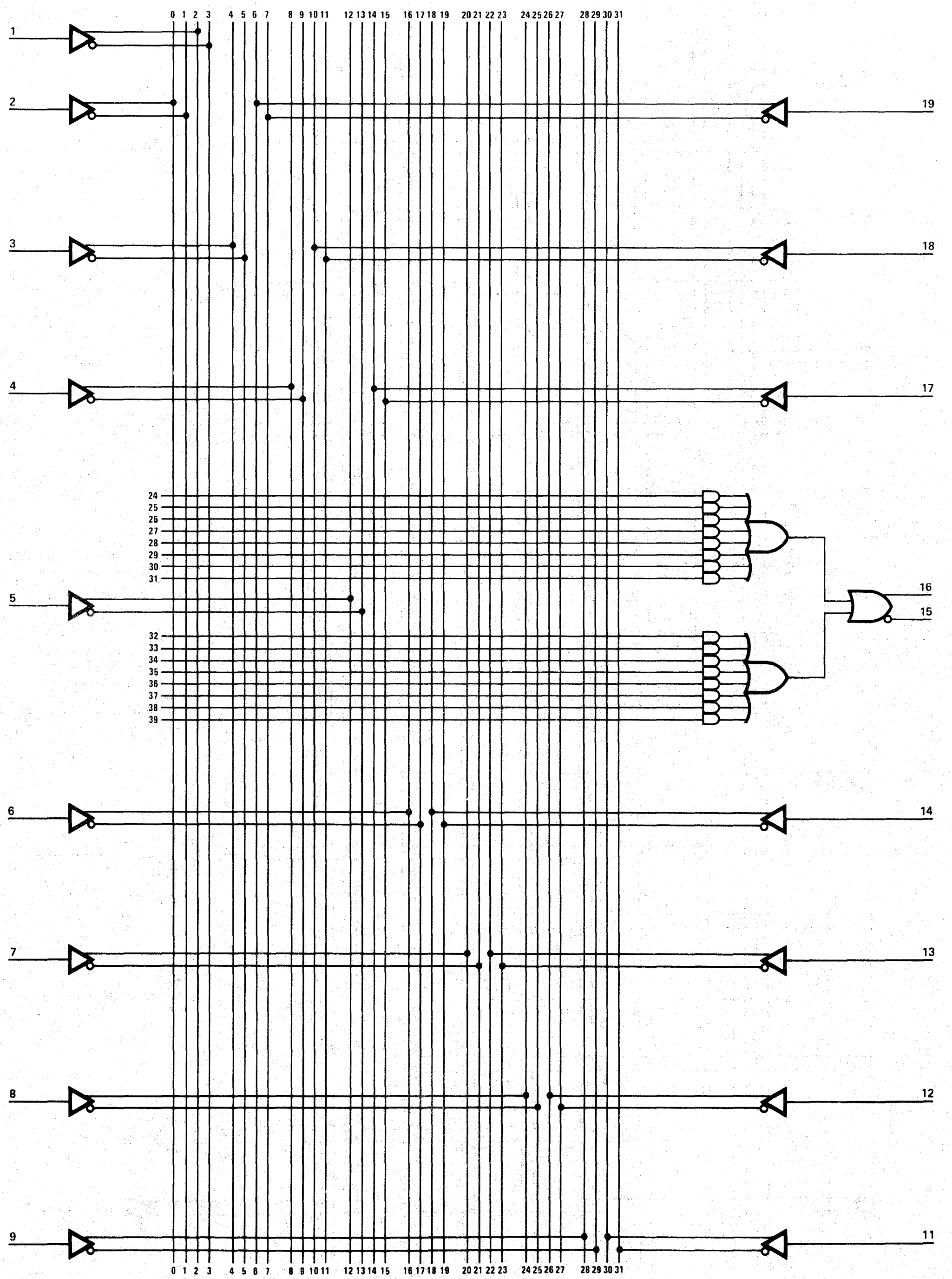
16C1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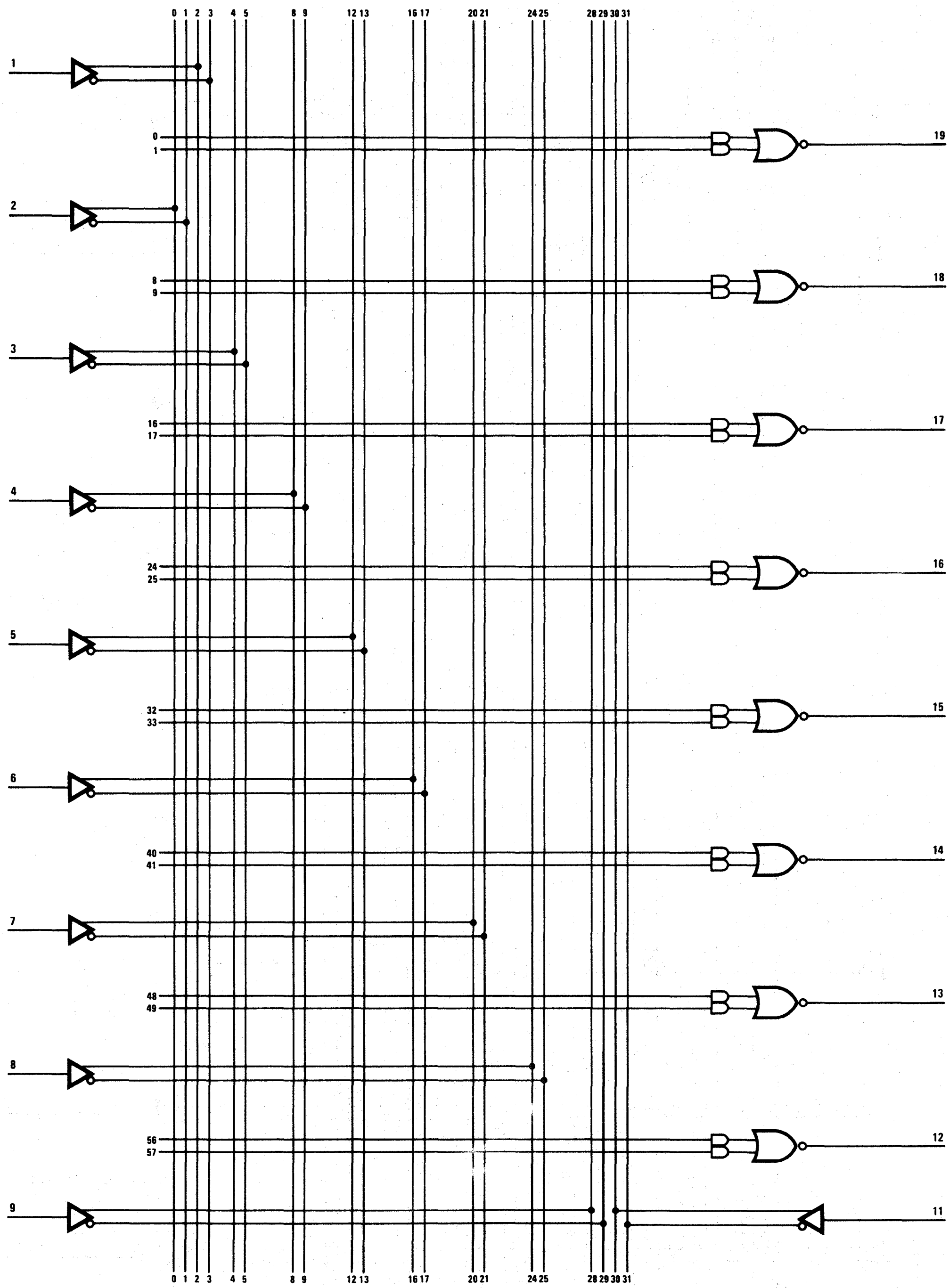
10L8



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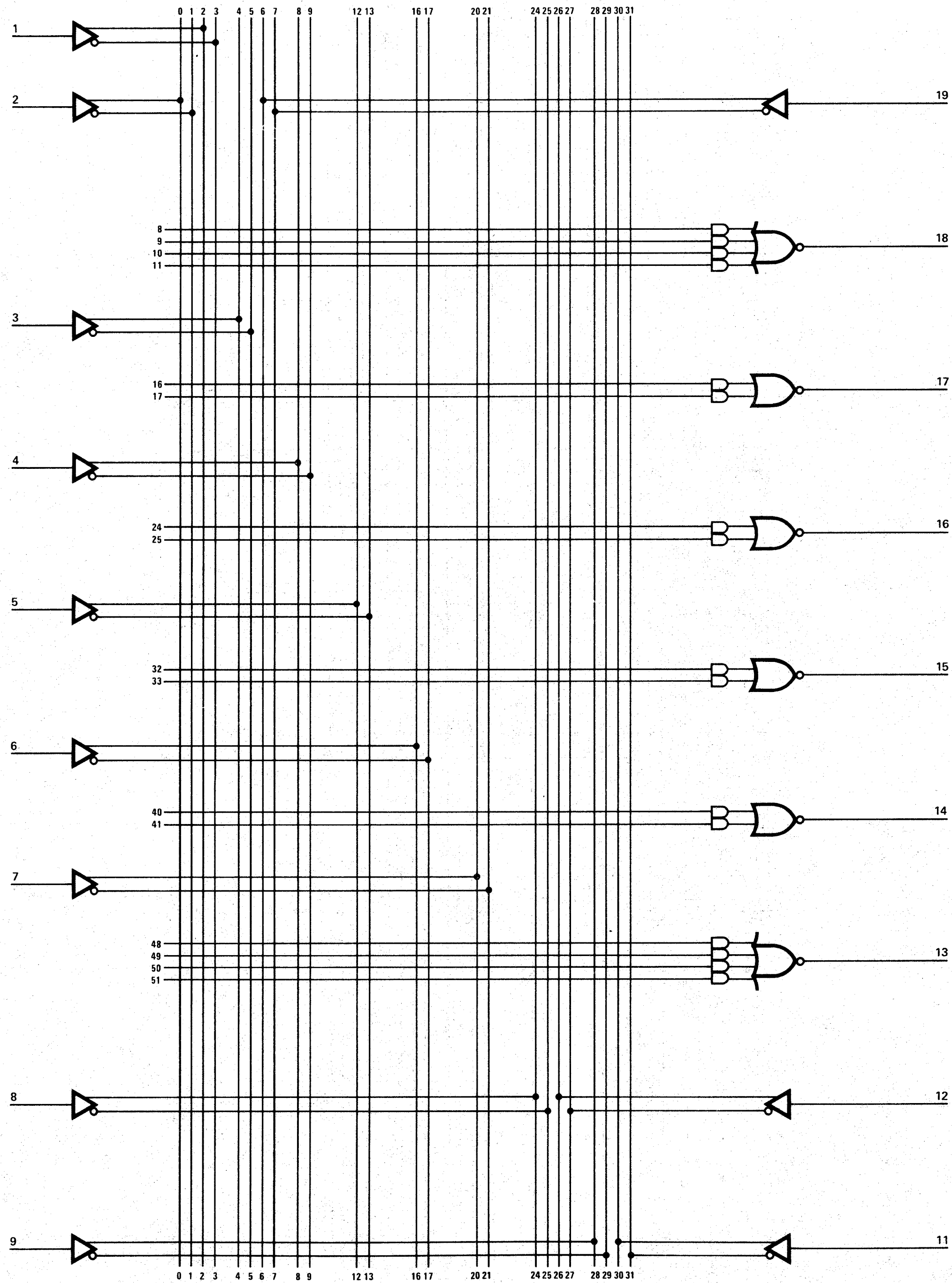
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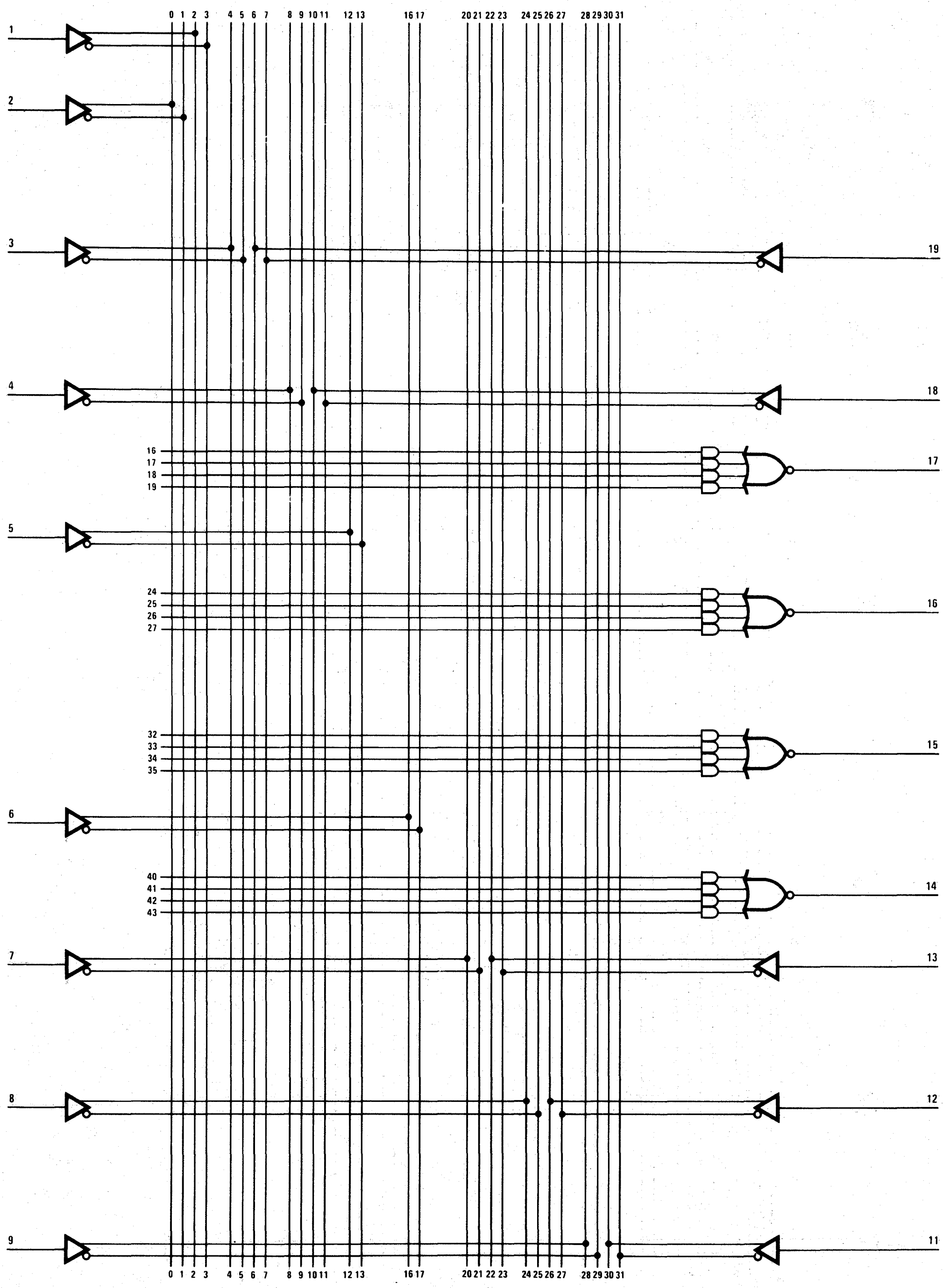
14L4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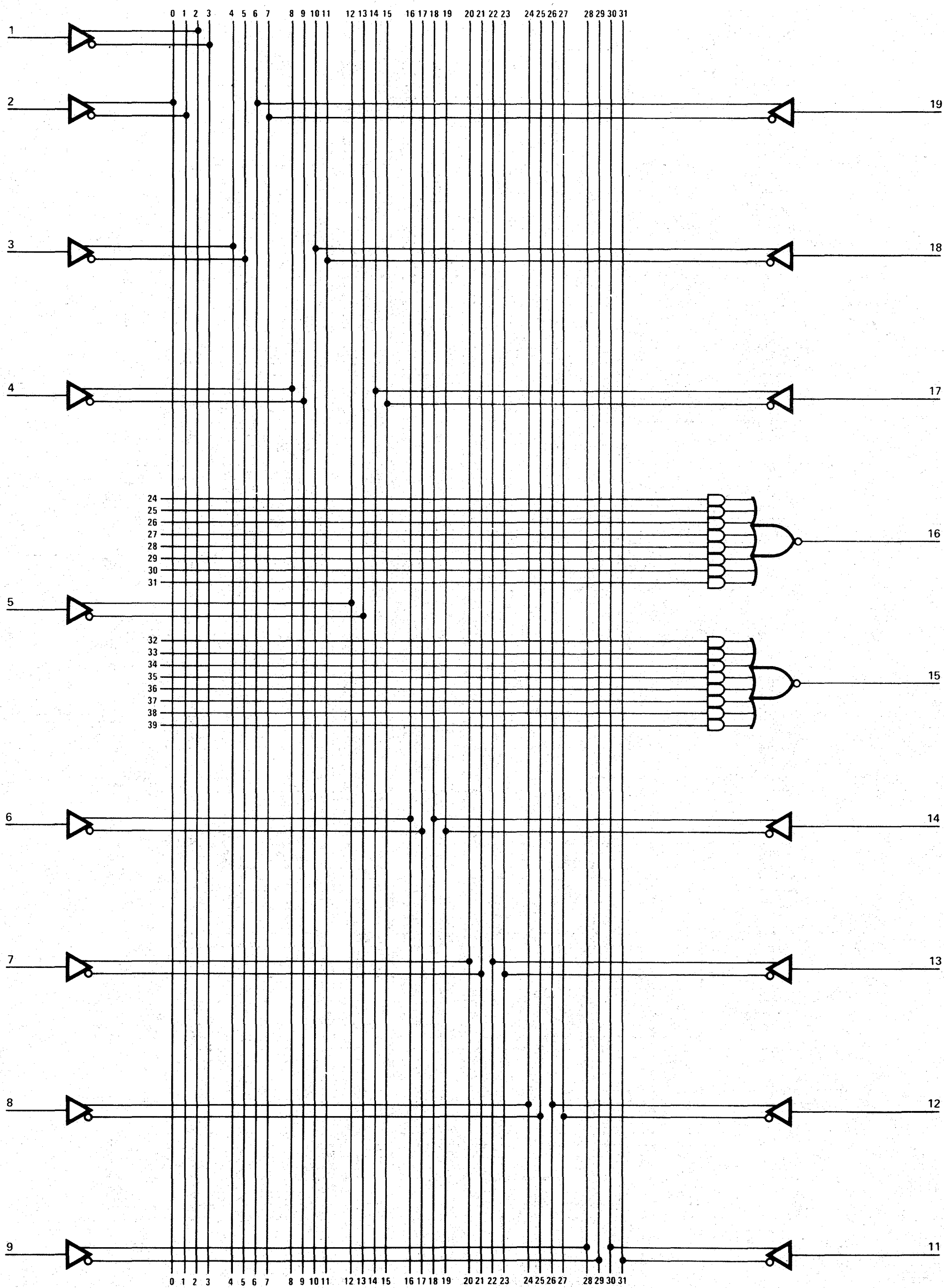
16L2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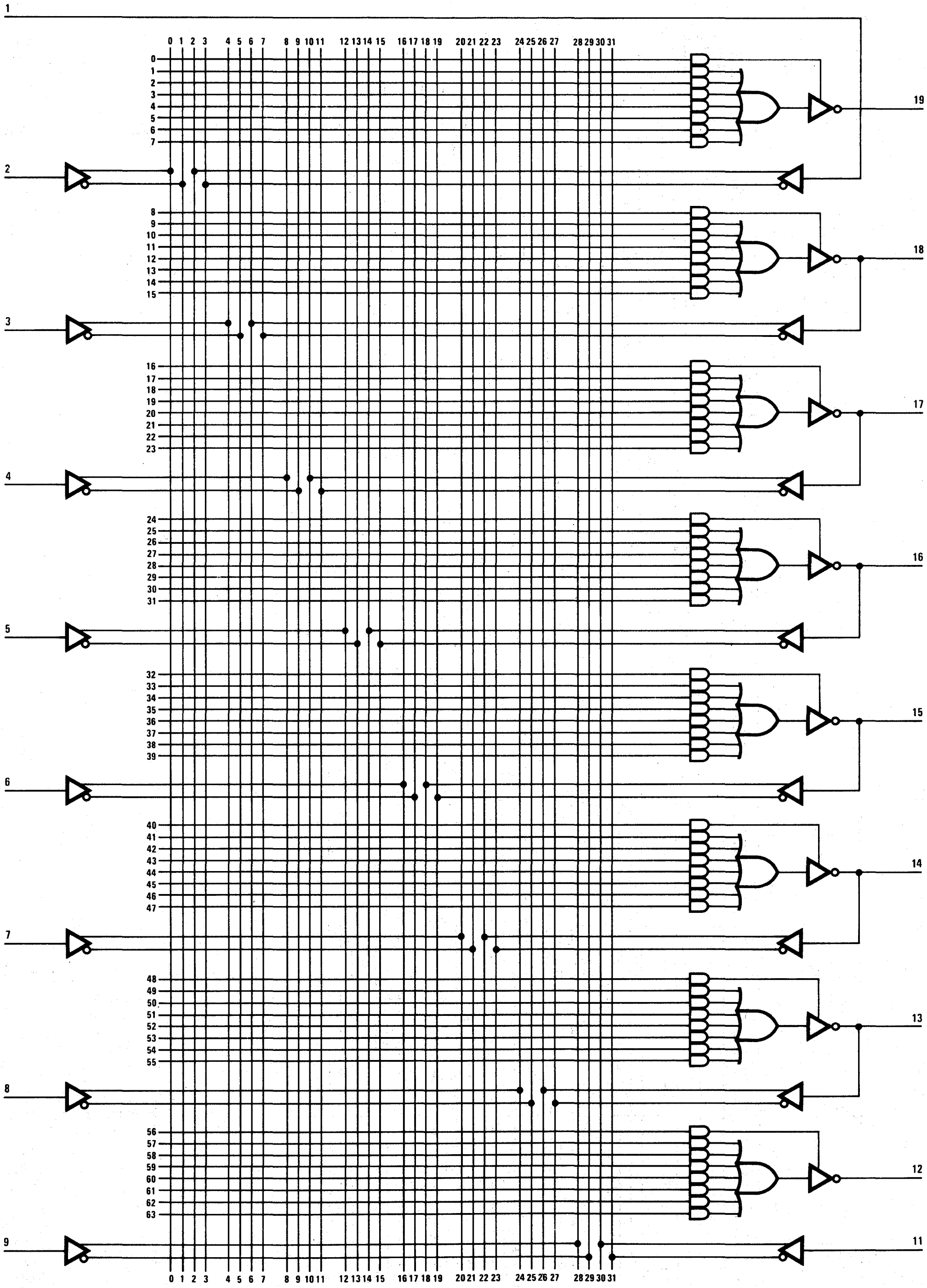
16L8



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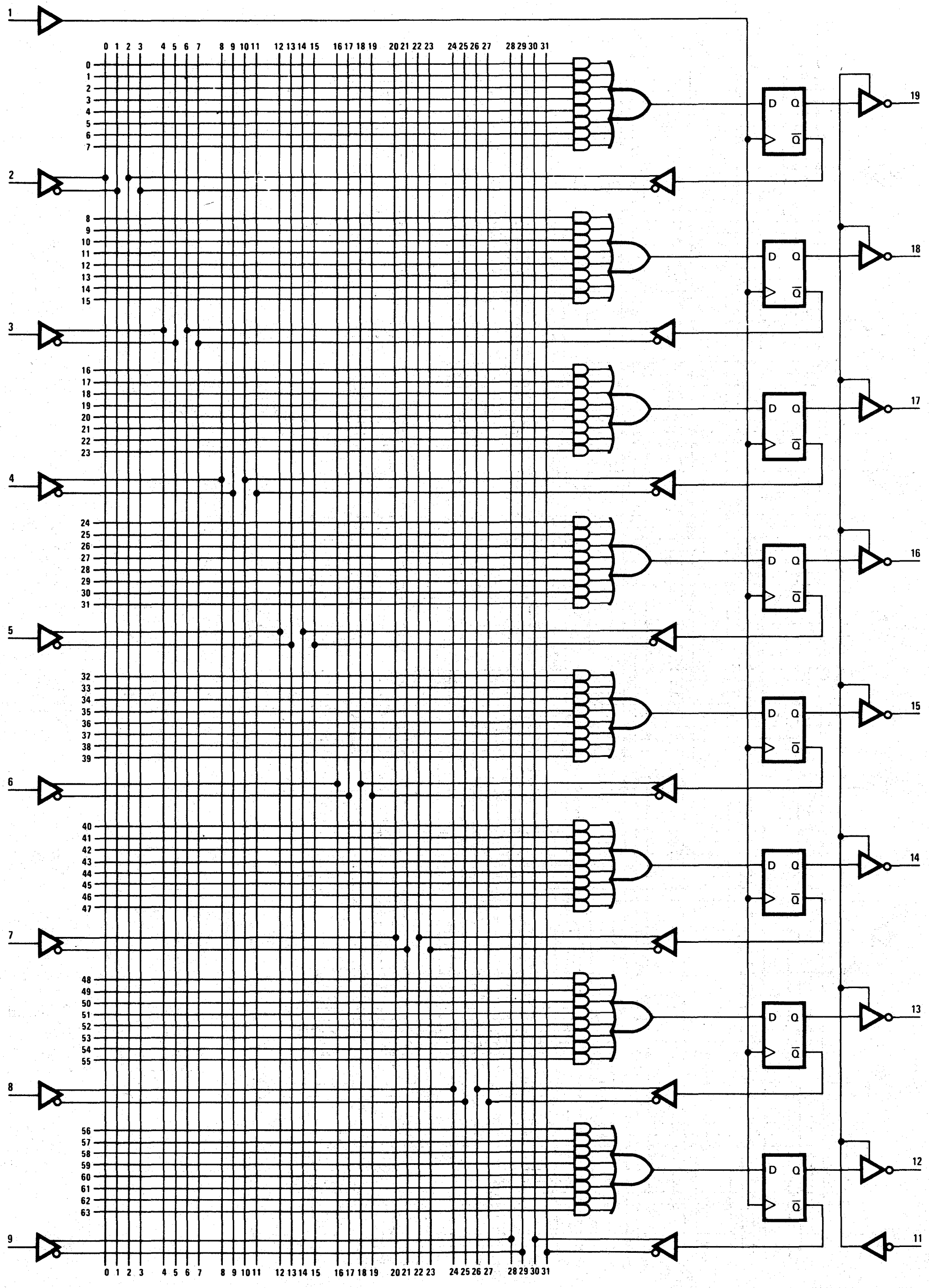
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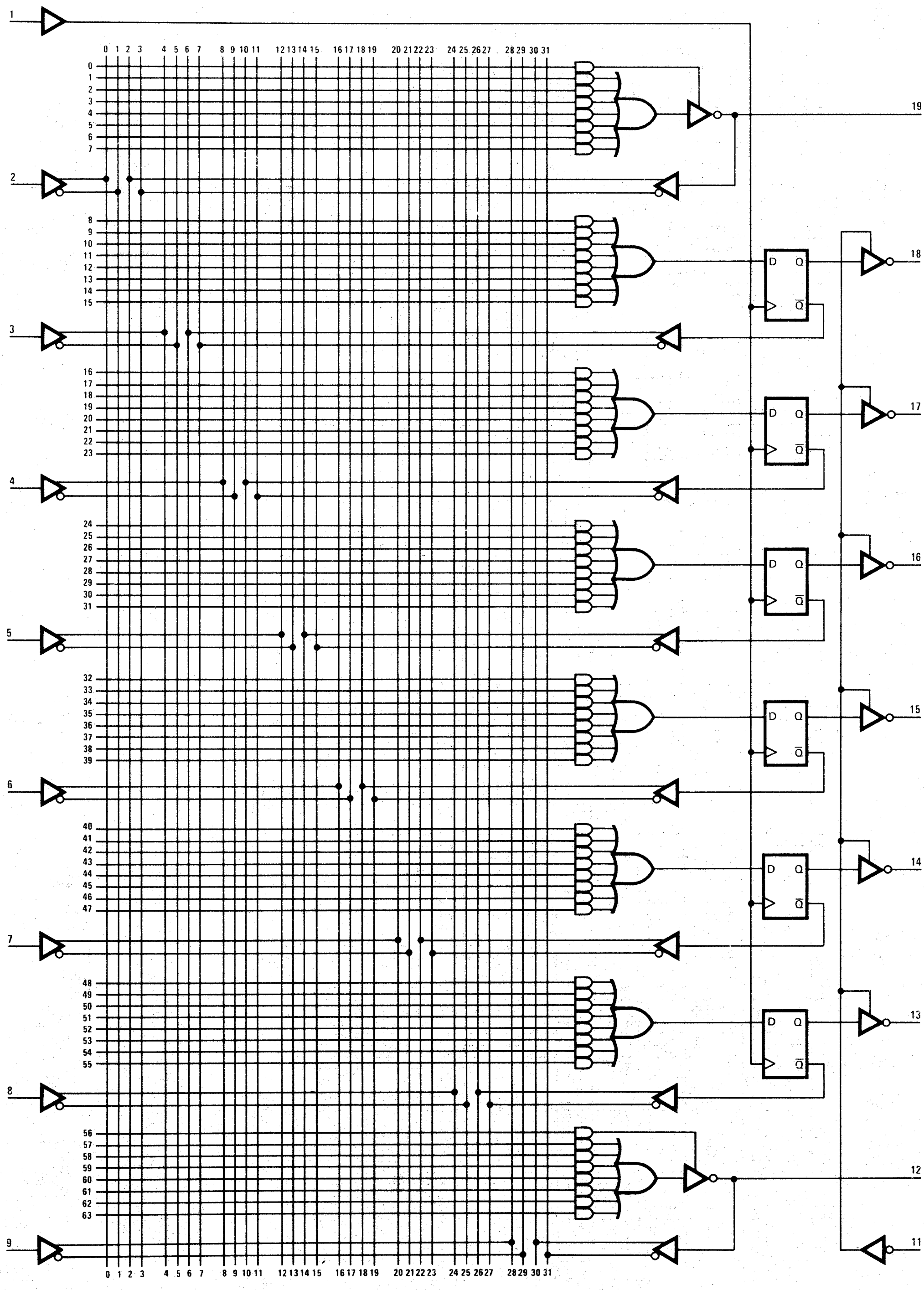
16R6



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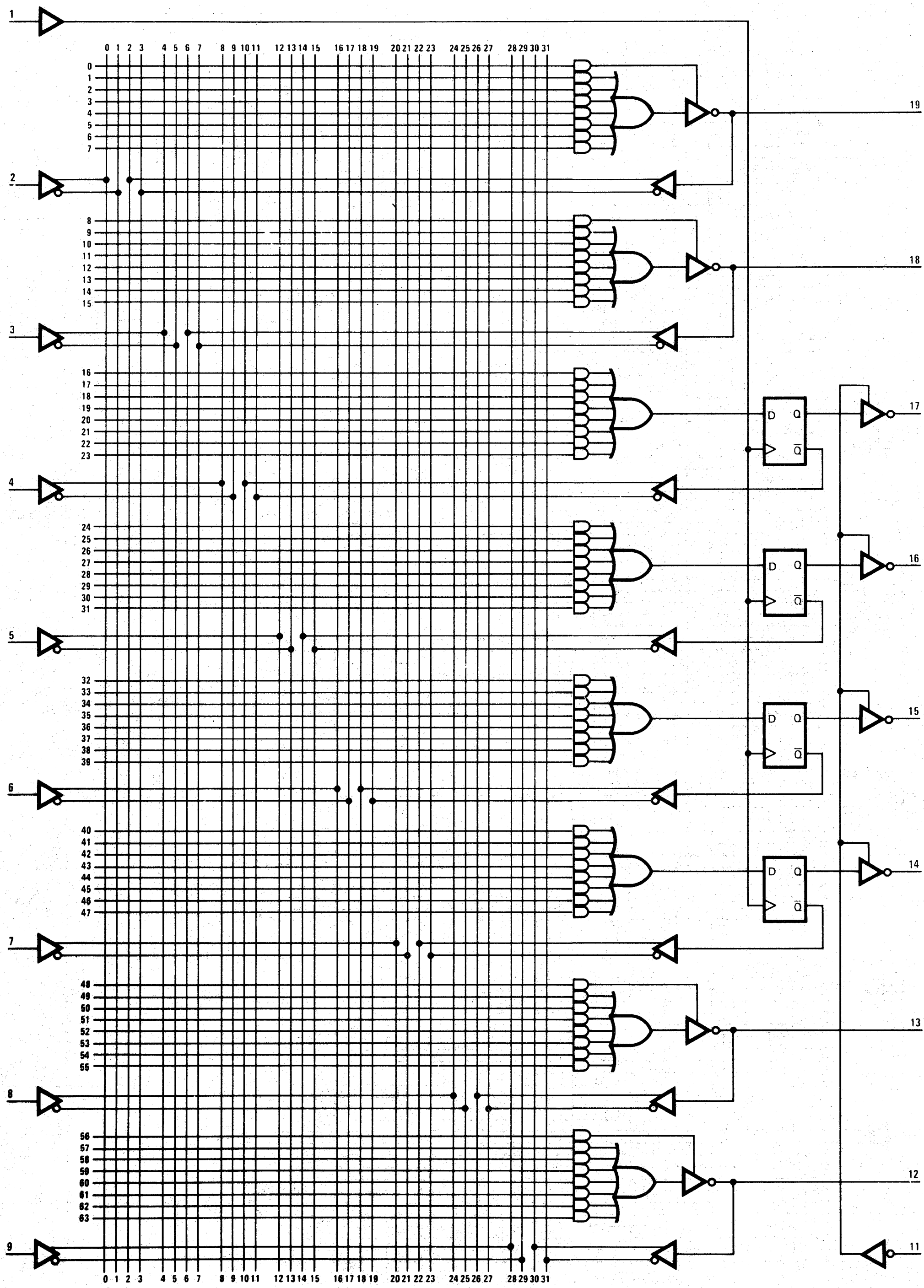
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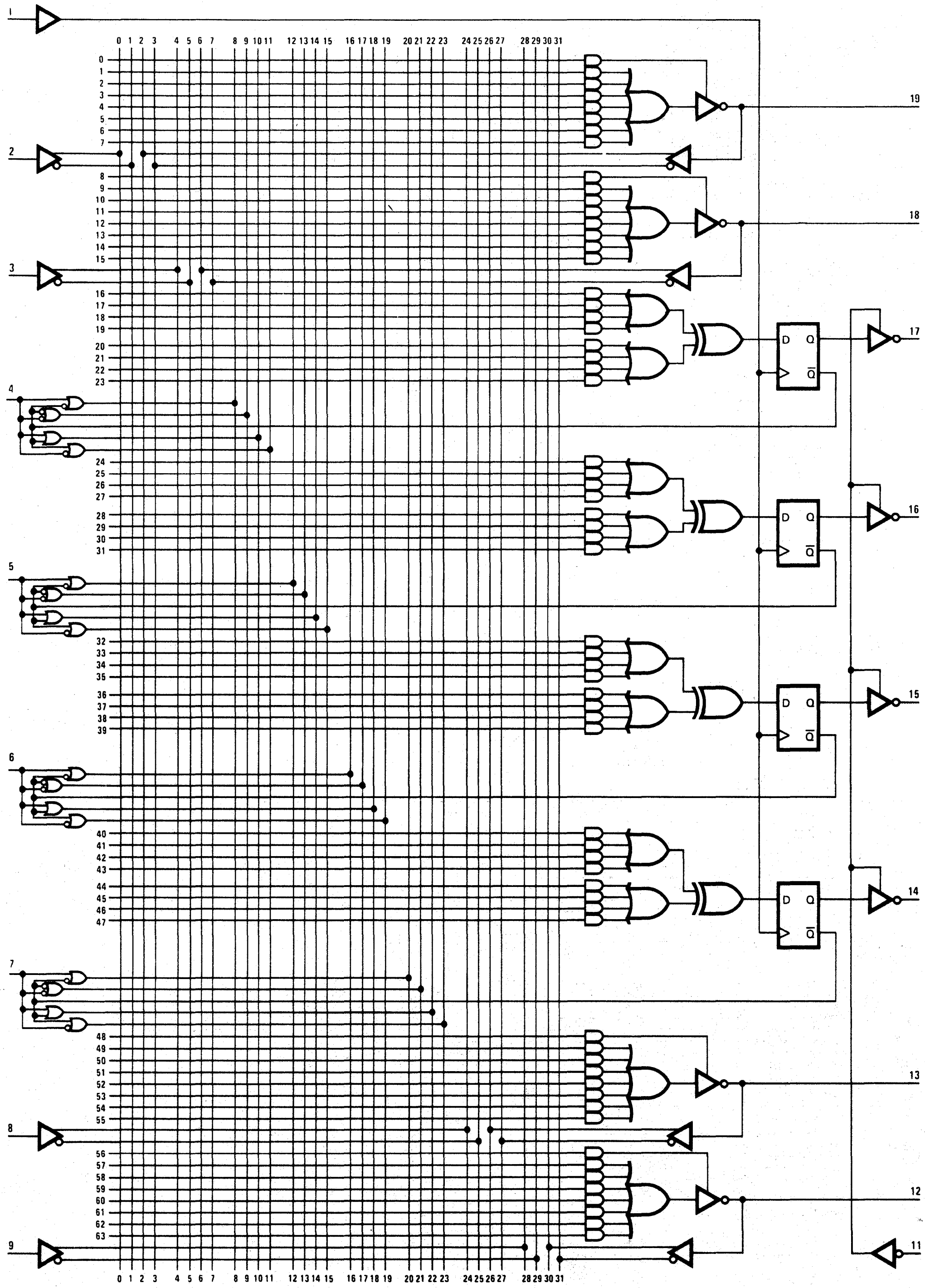
16X4



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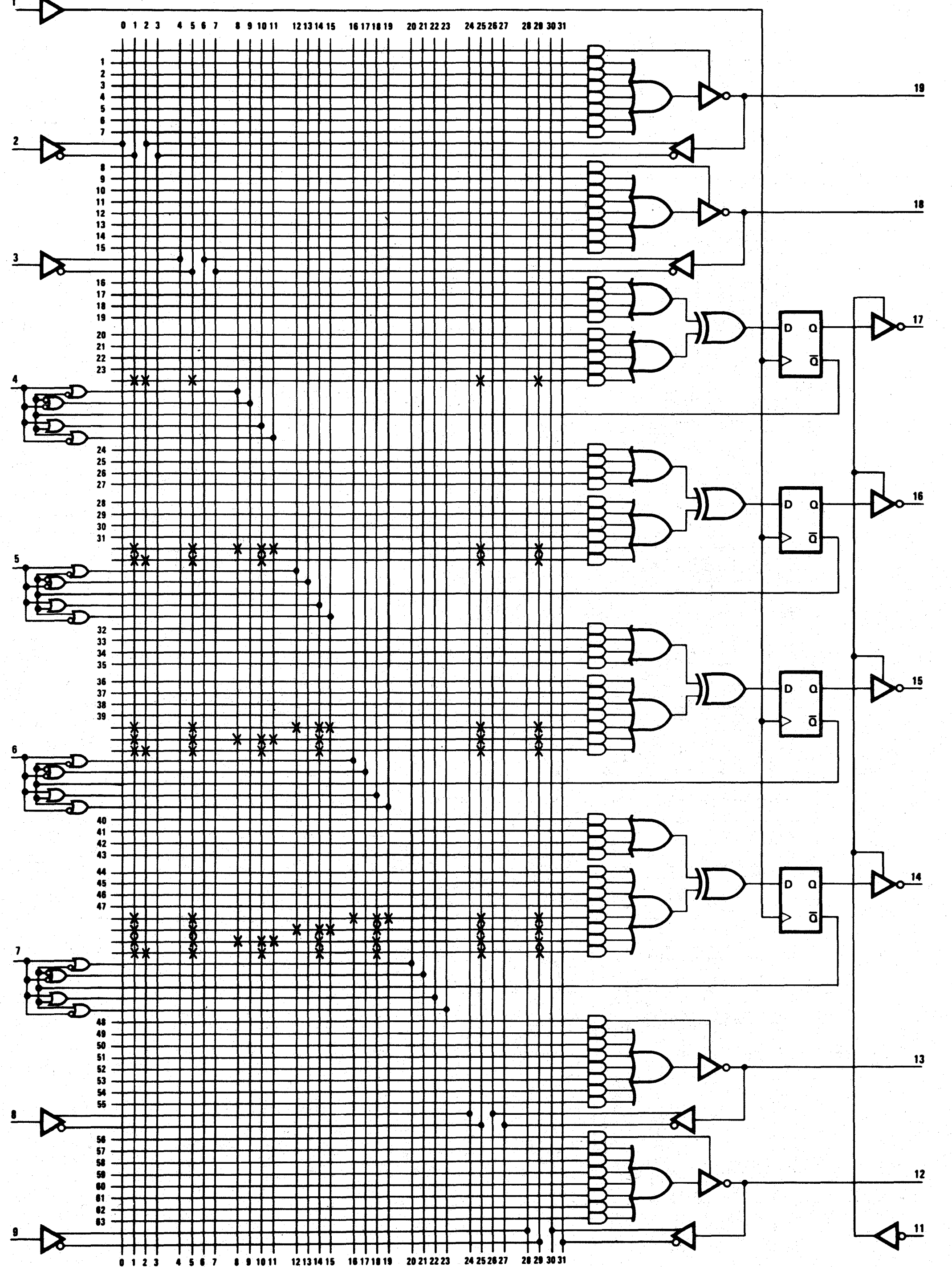

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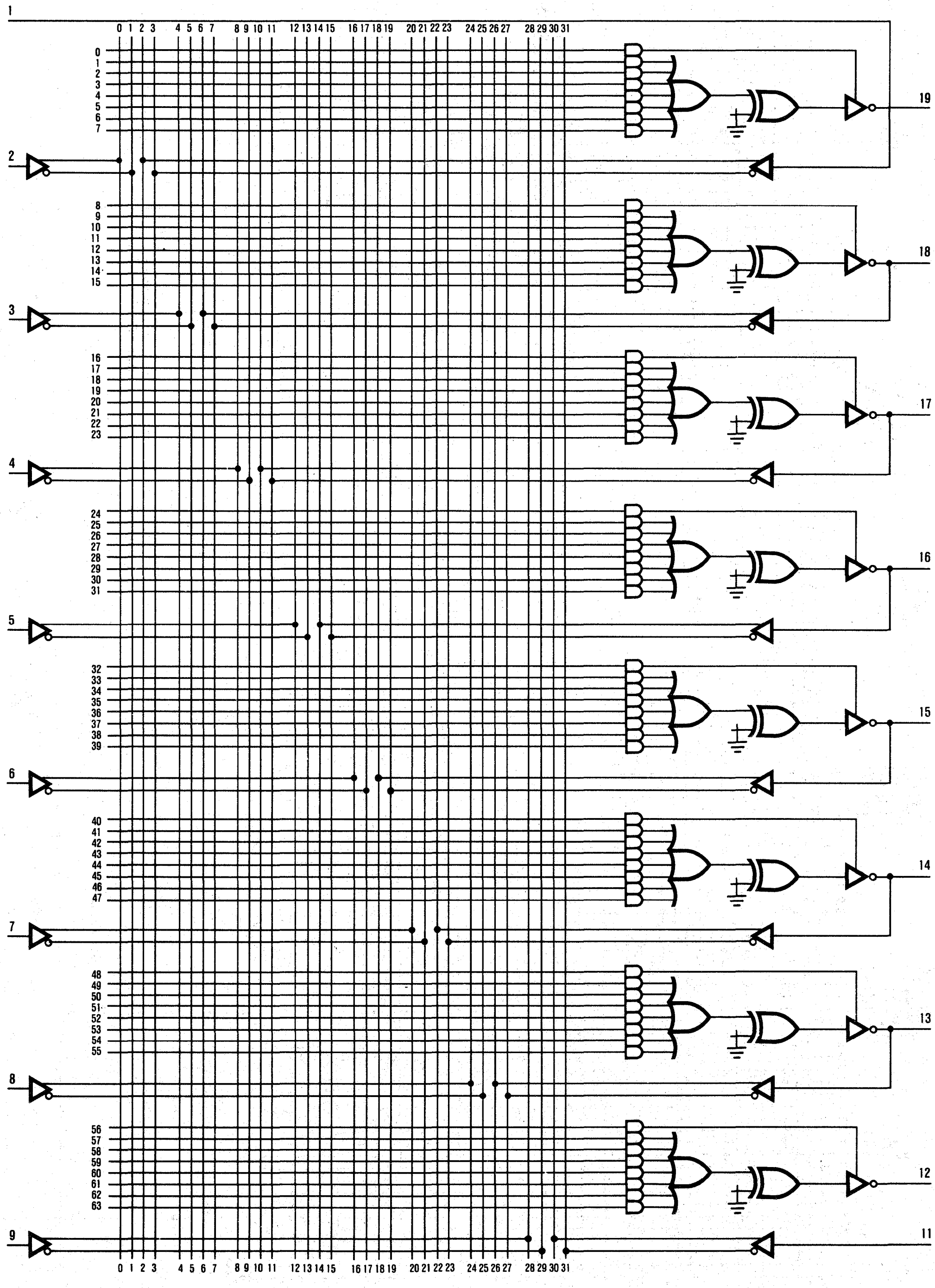

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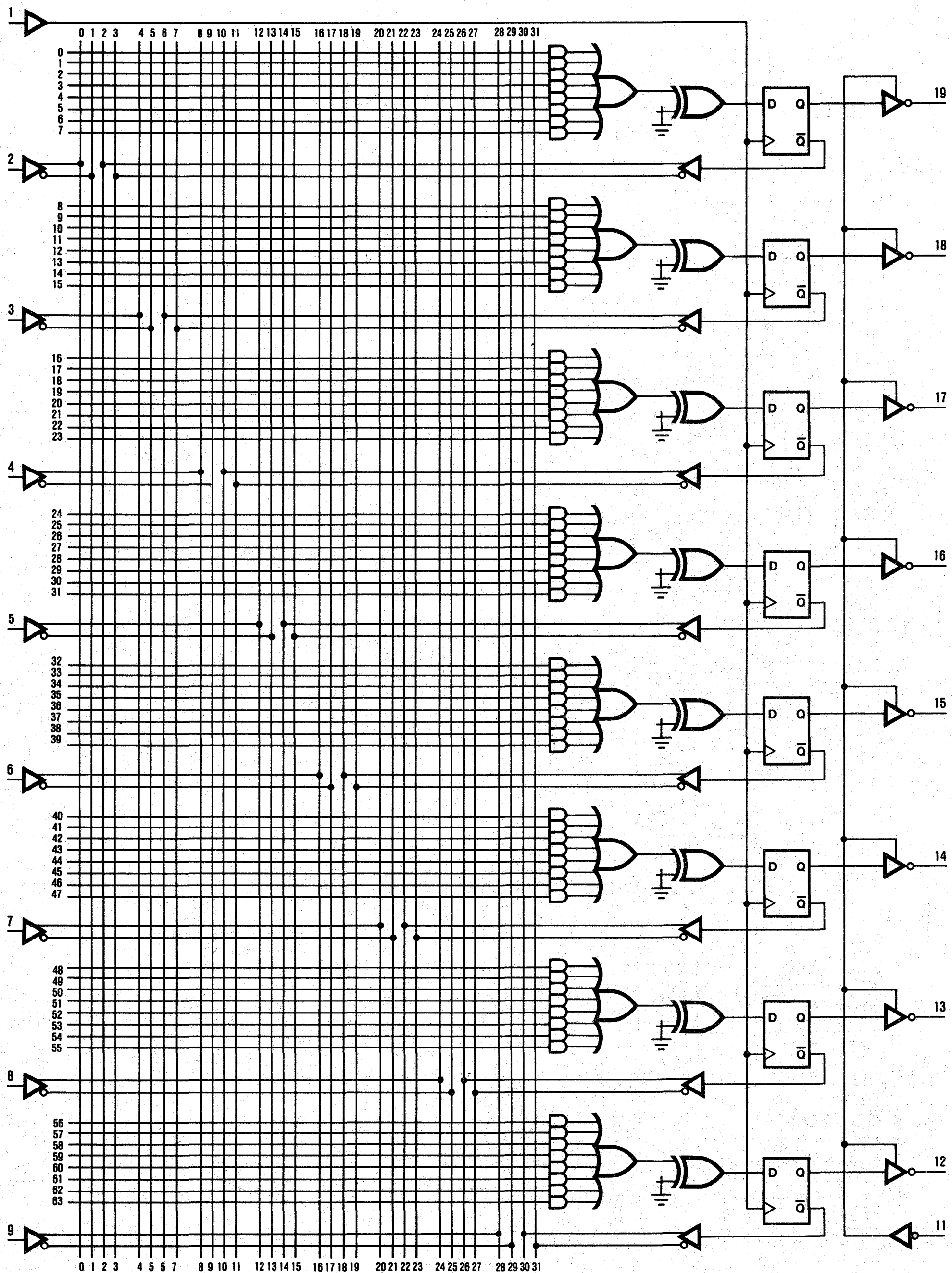
16RP8



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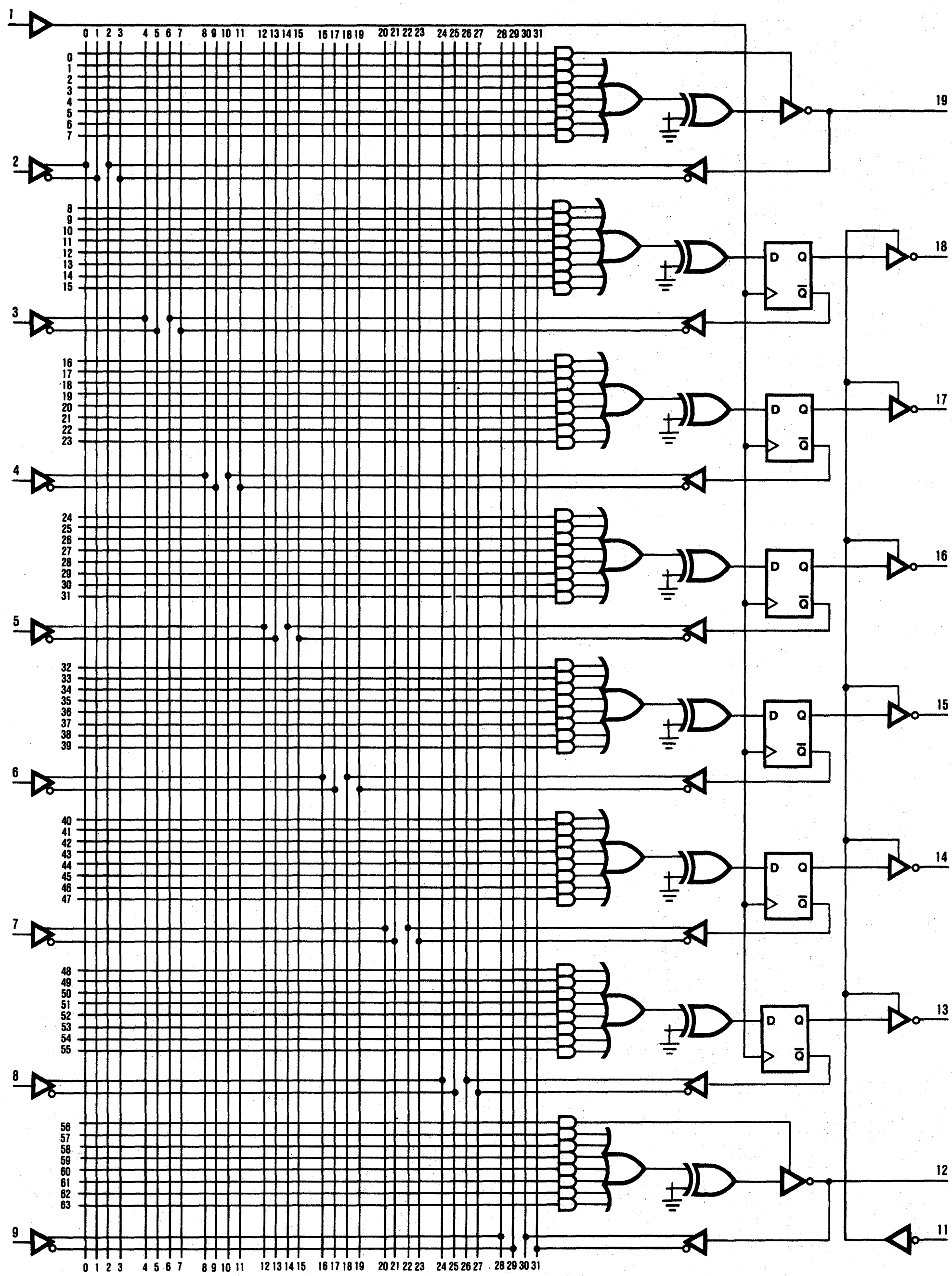
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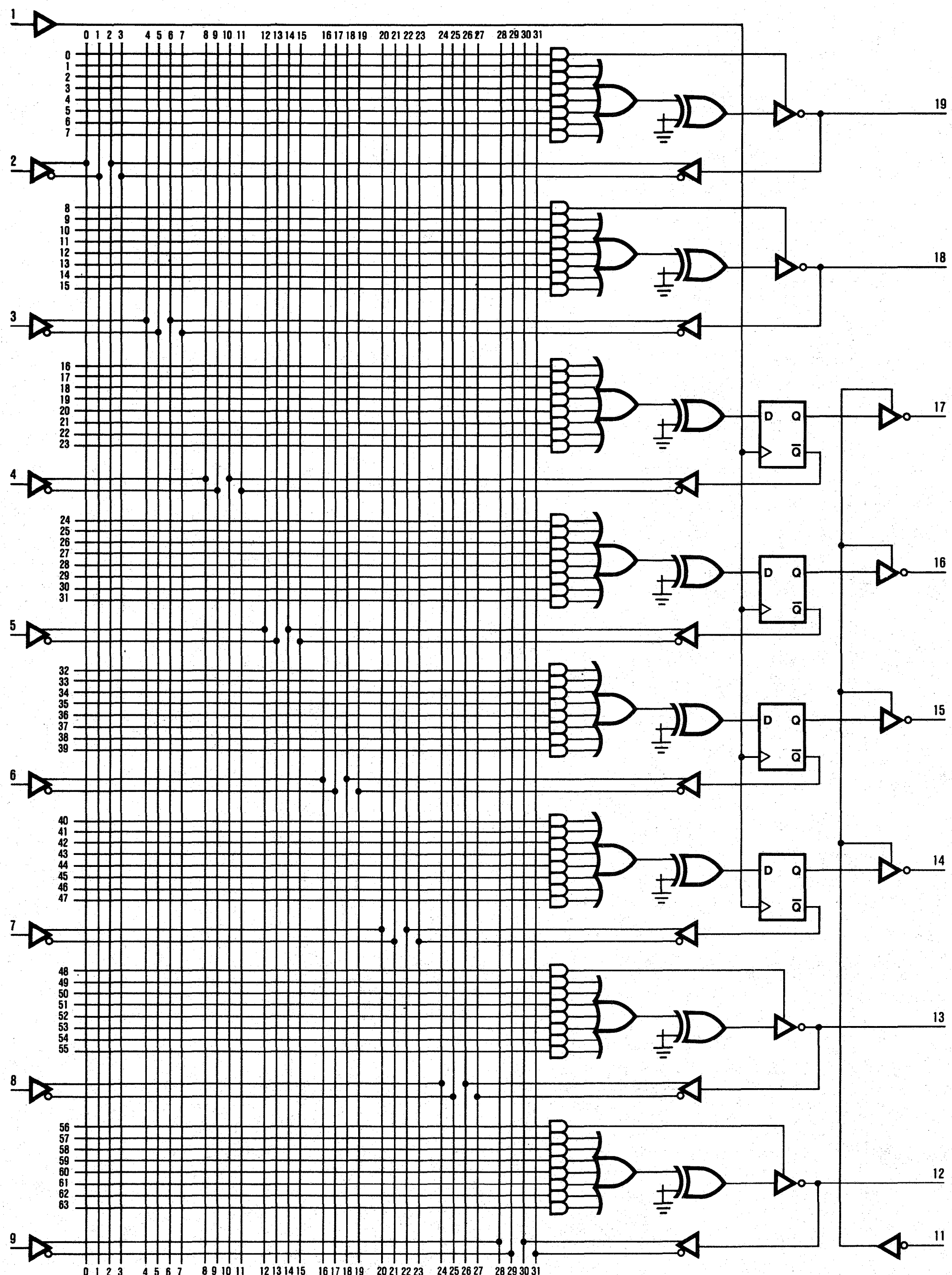
16RP4



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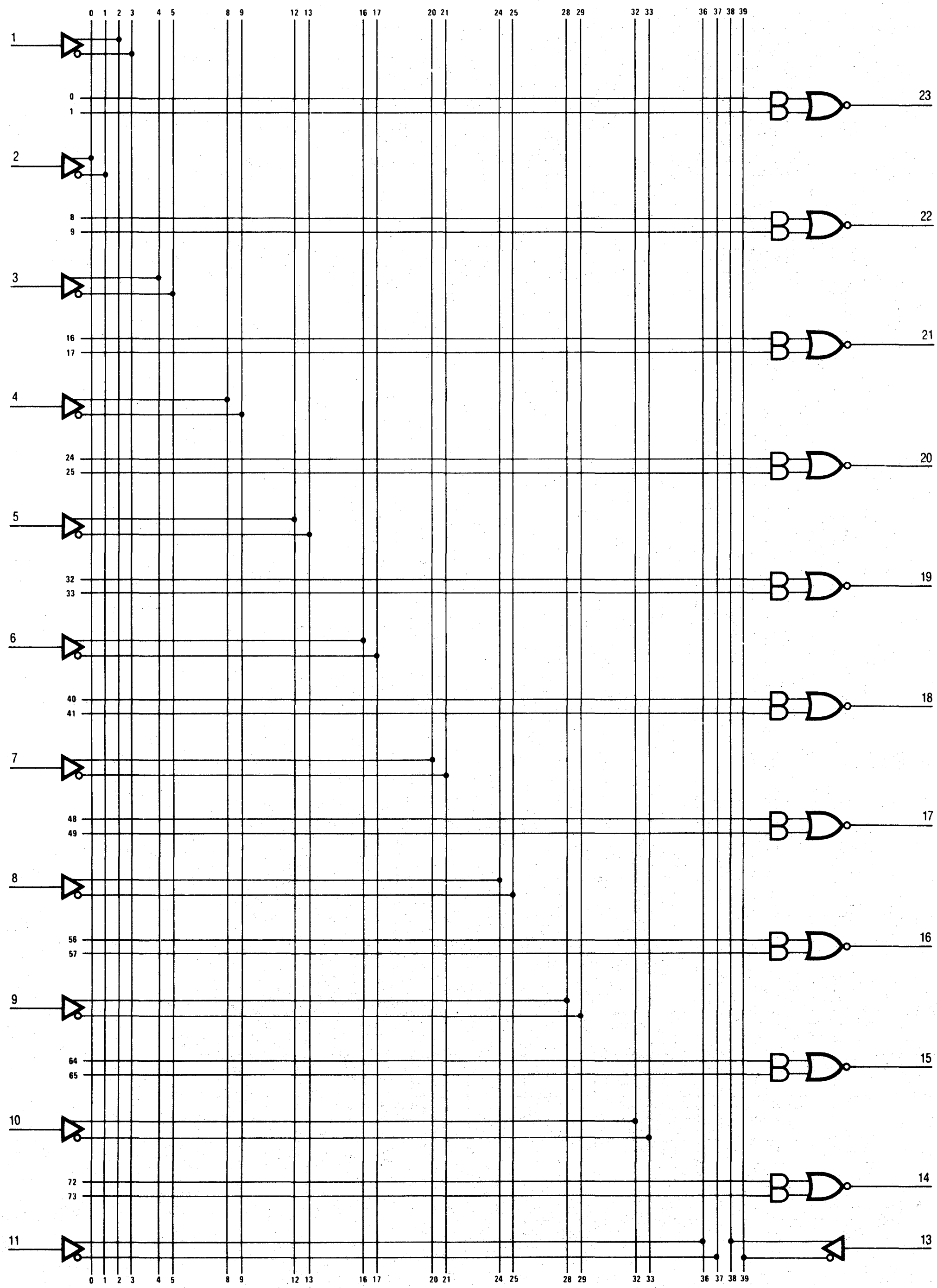
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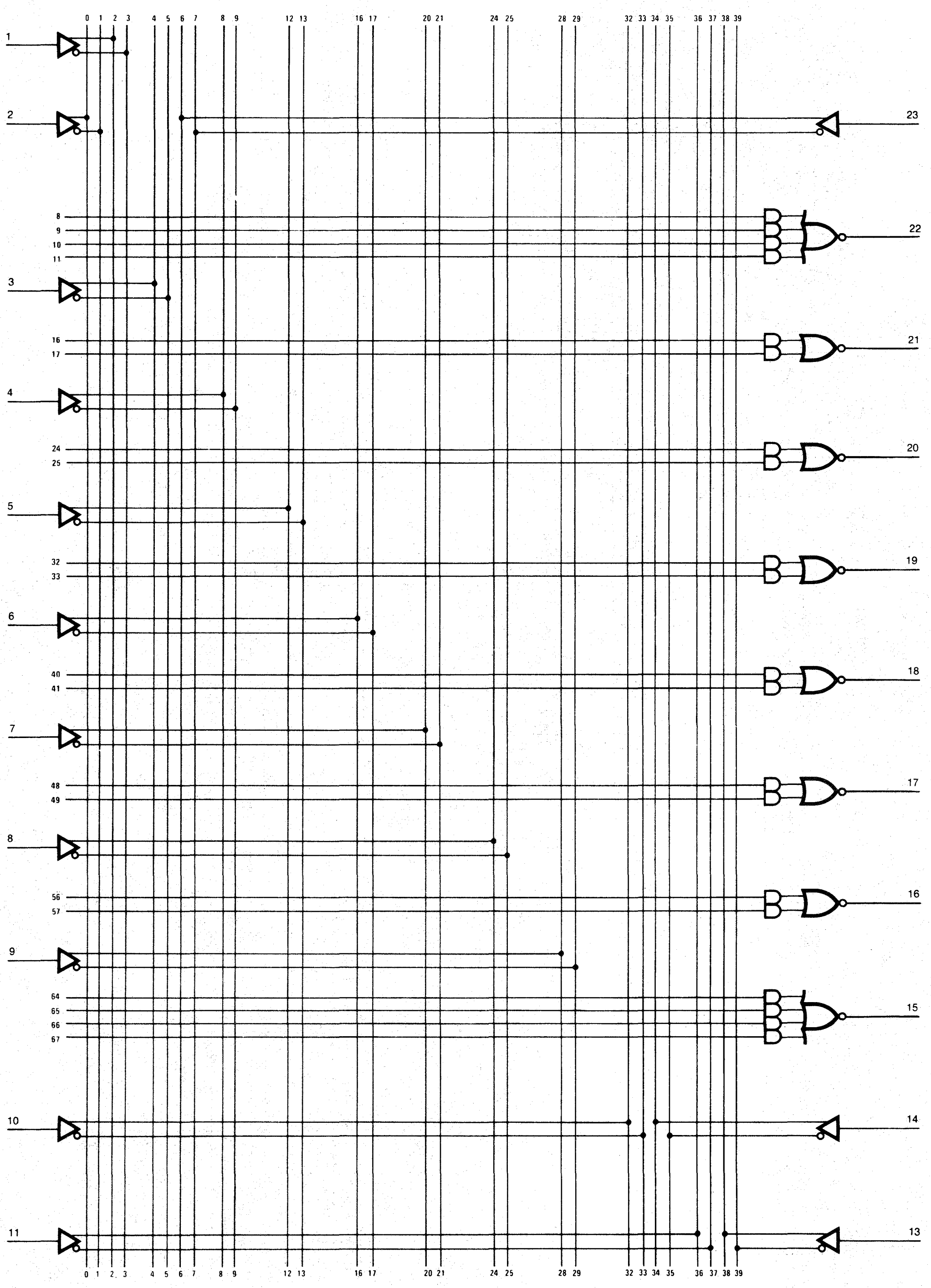
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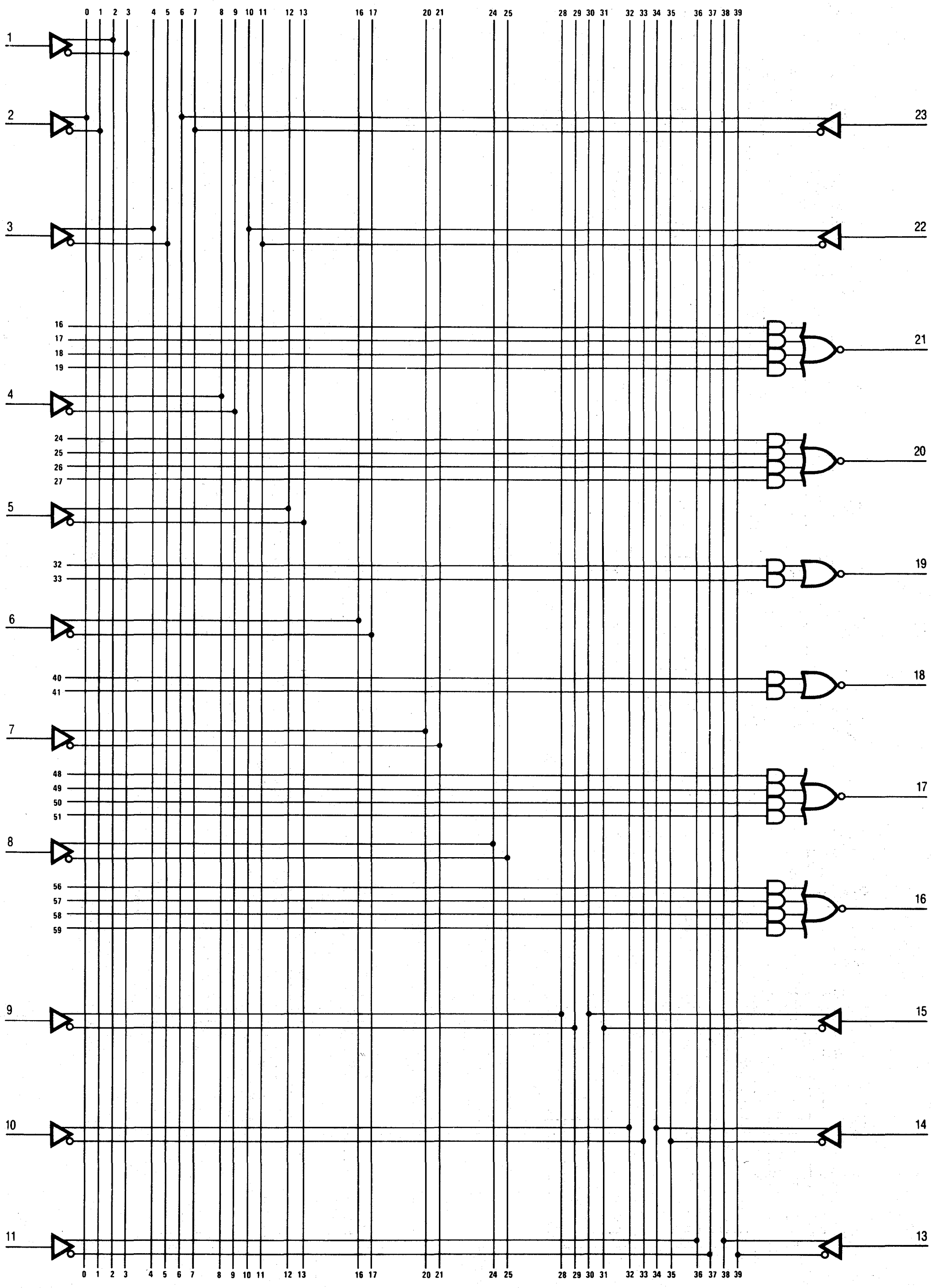
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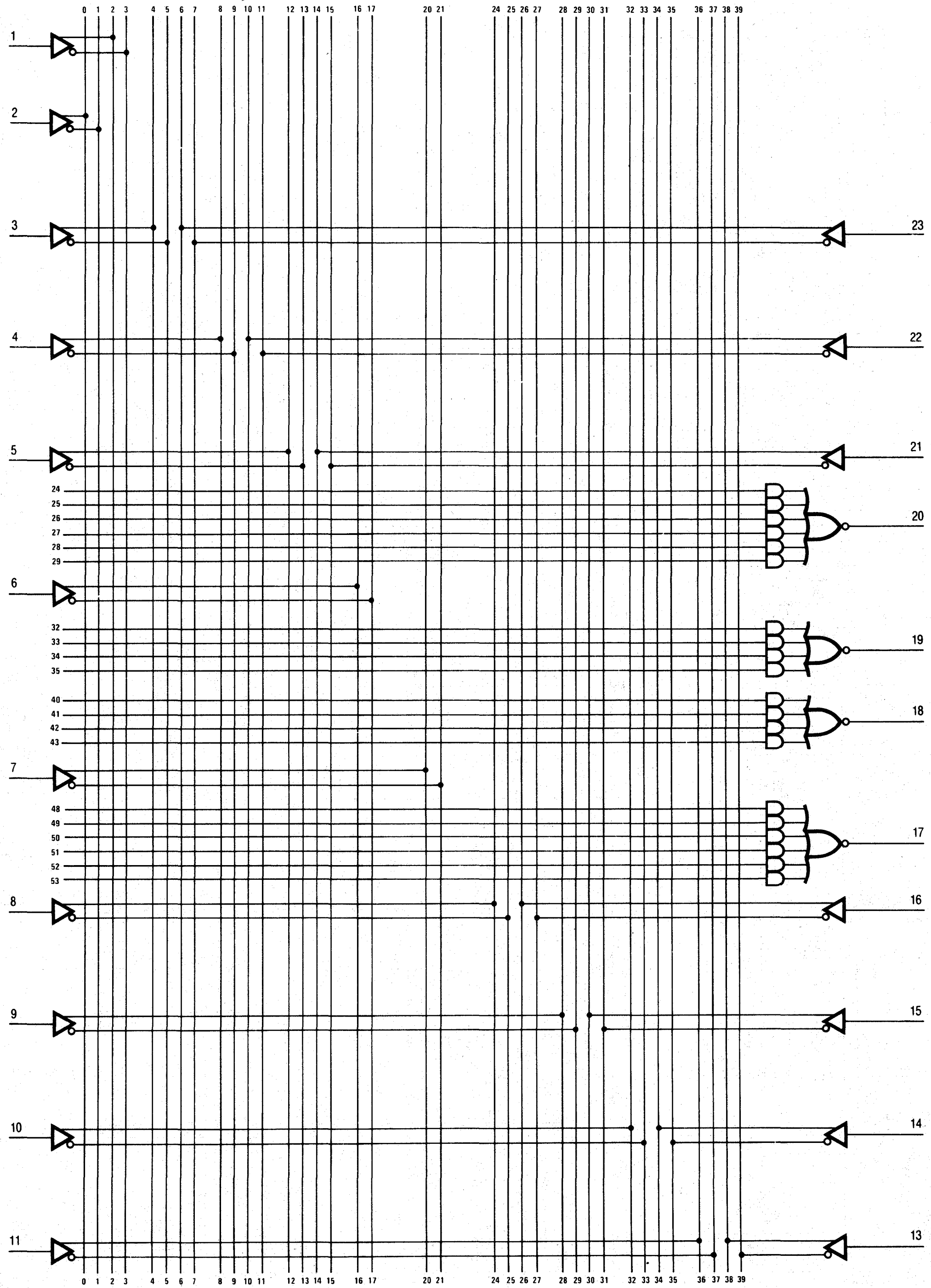
18L4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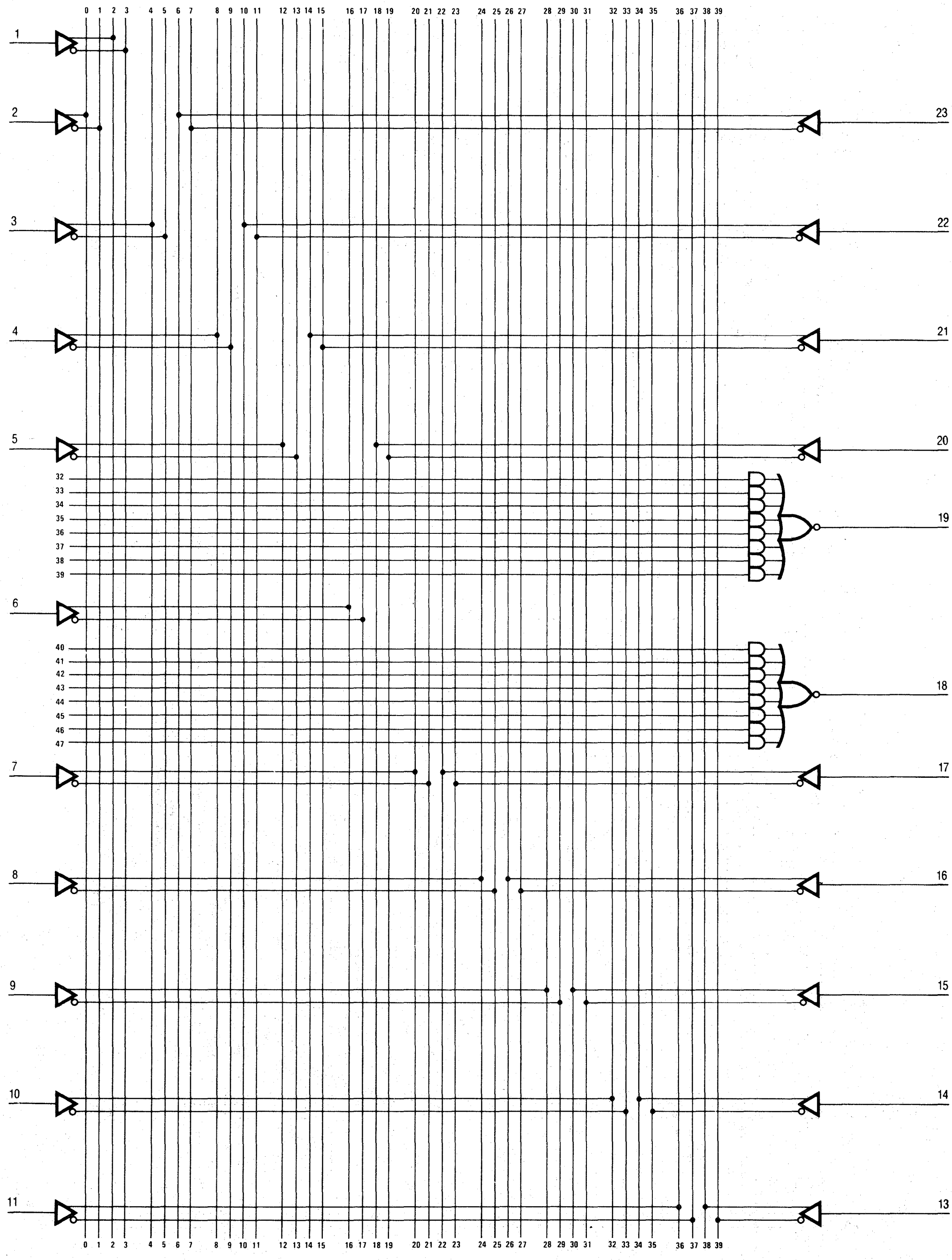
20L2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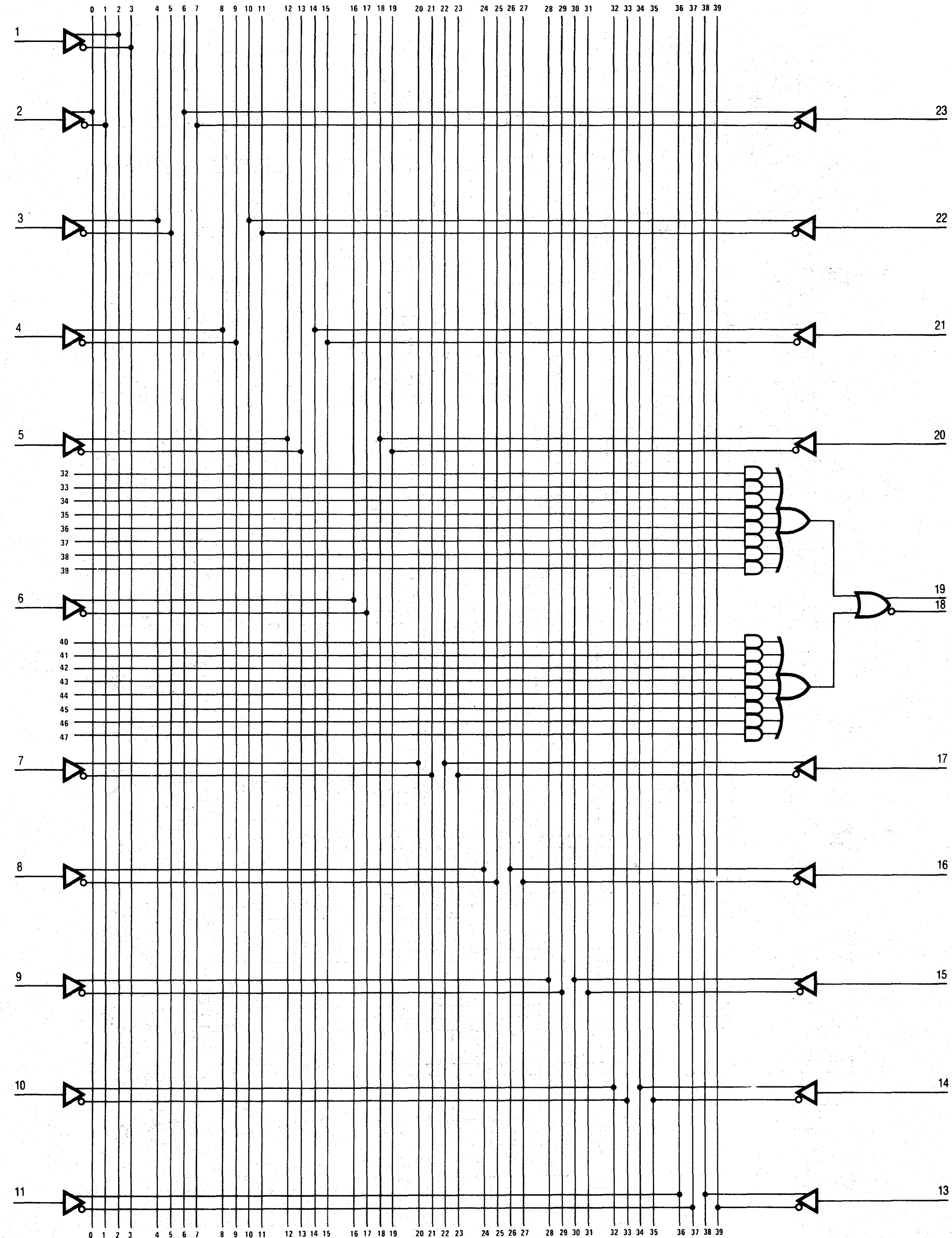

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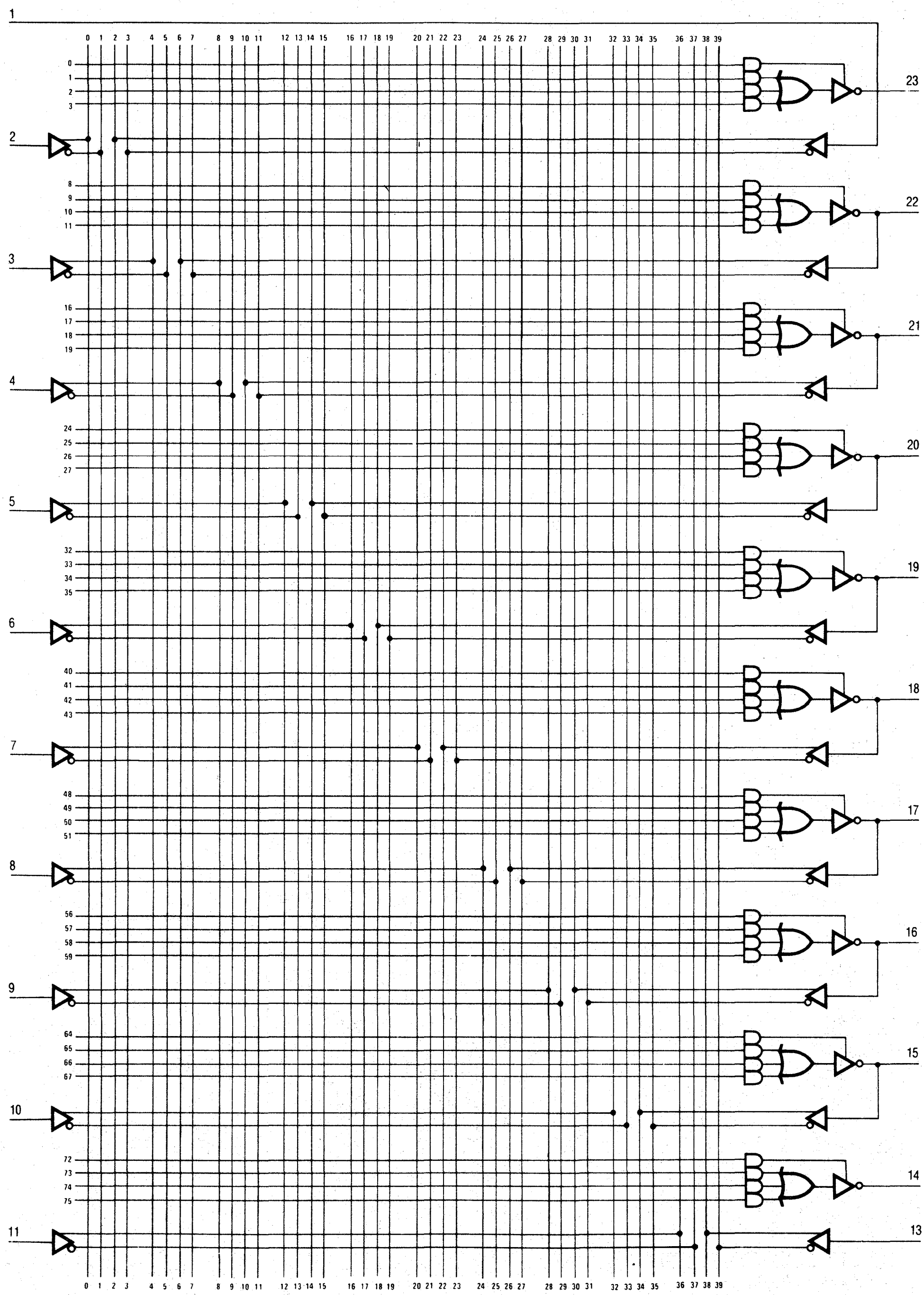

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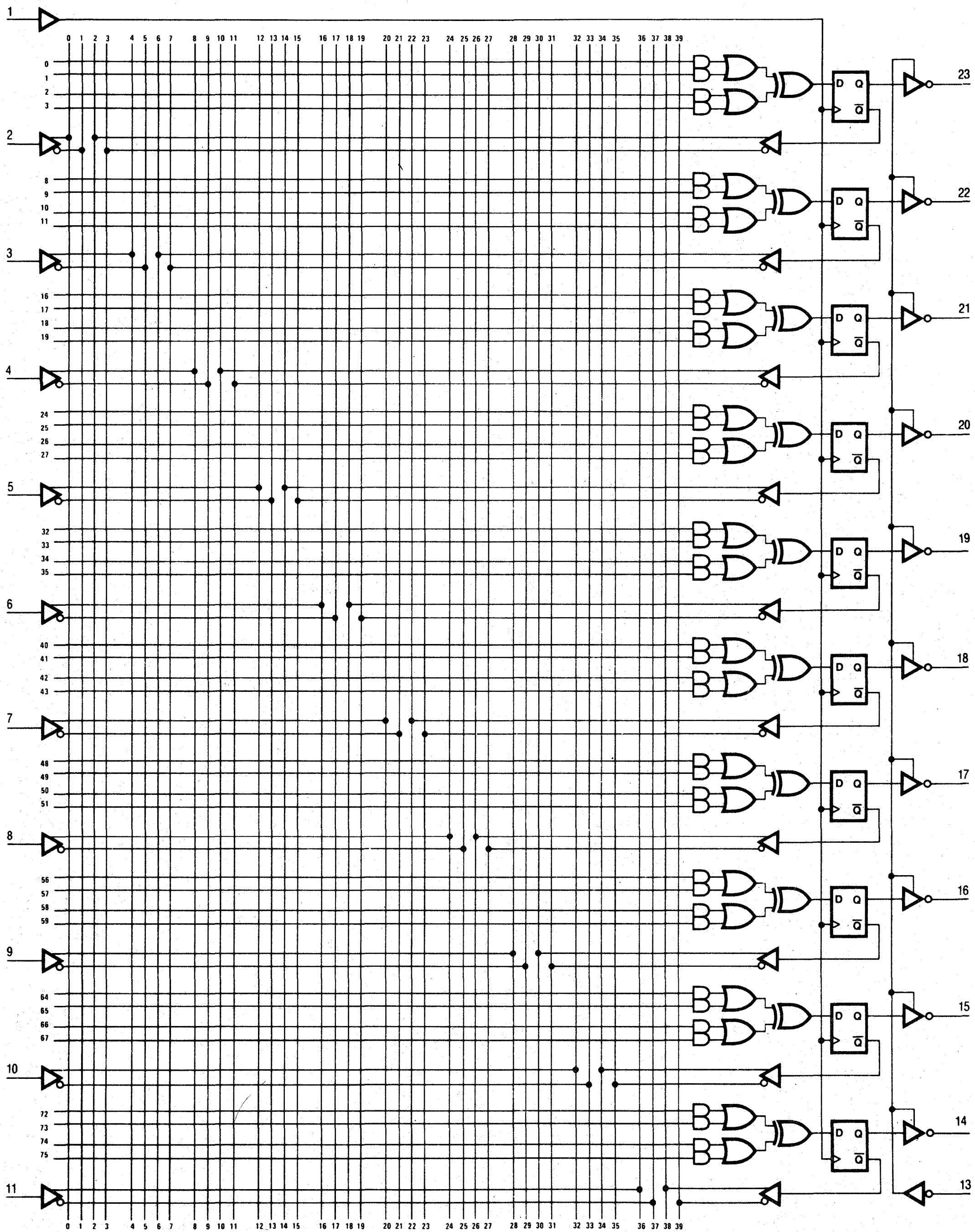

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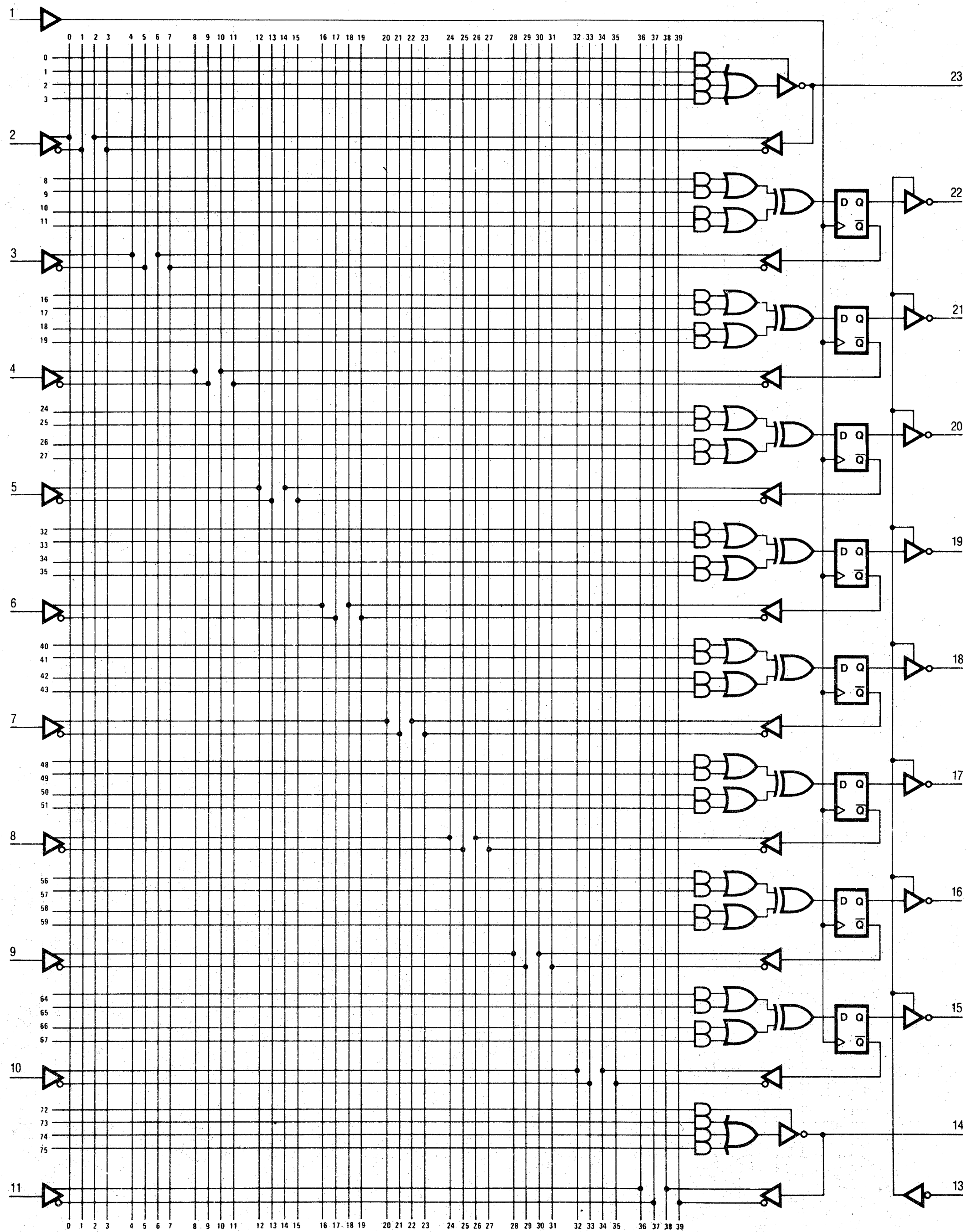

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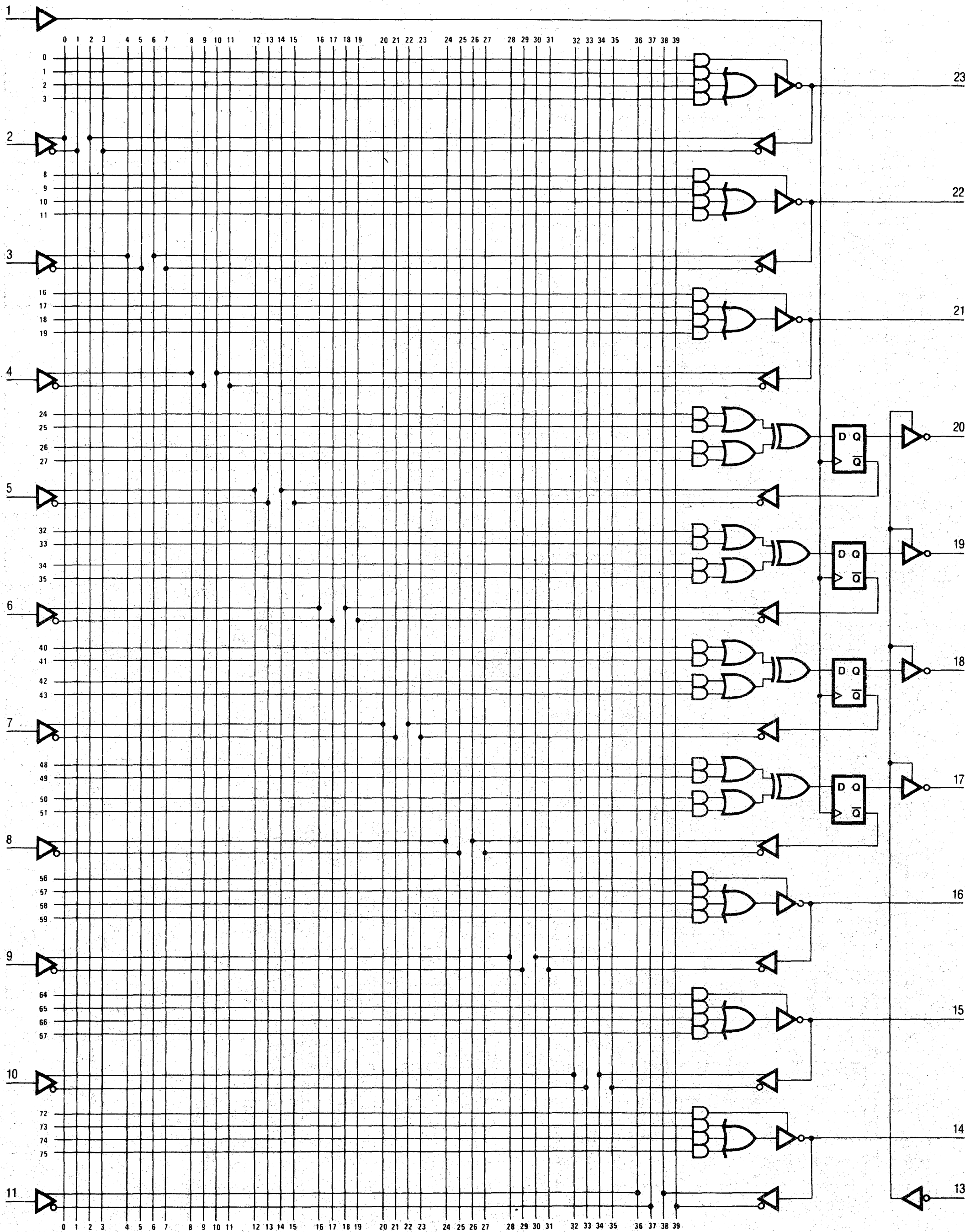

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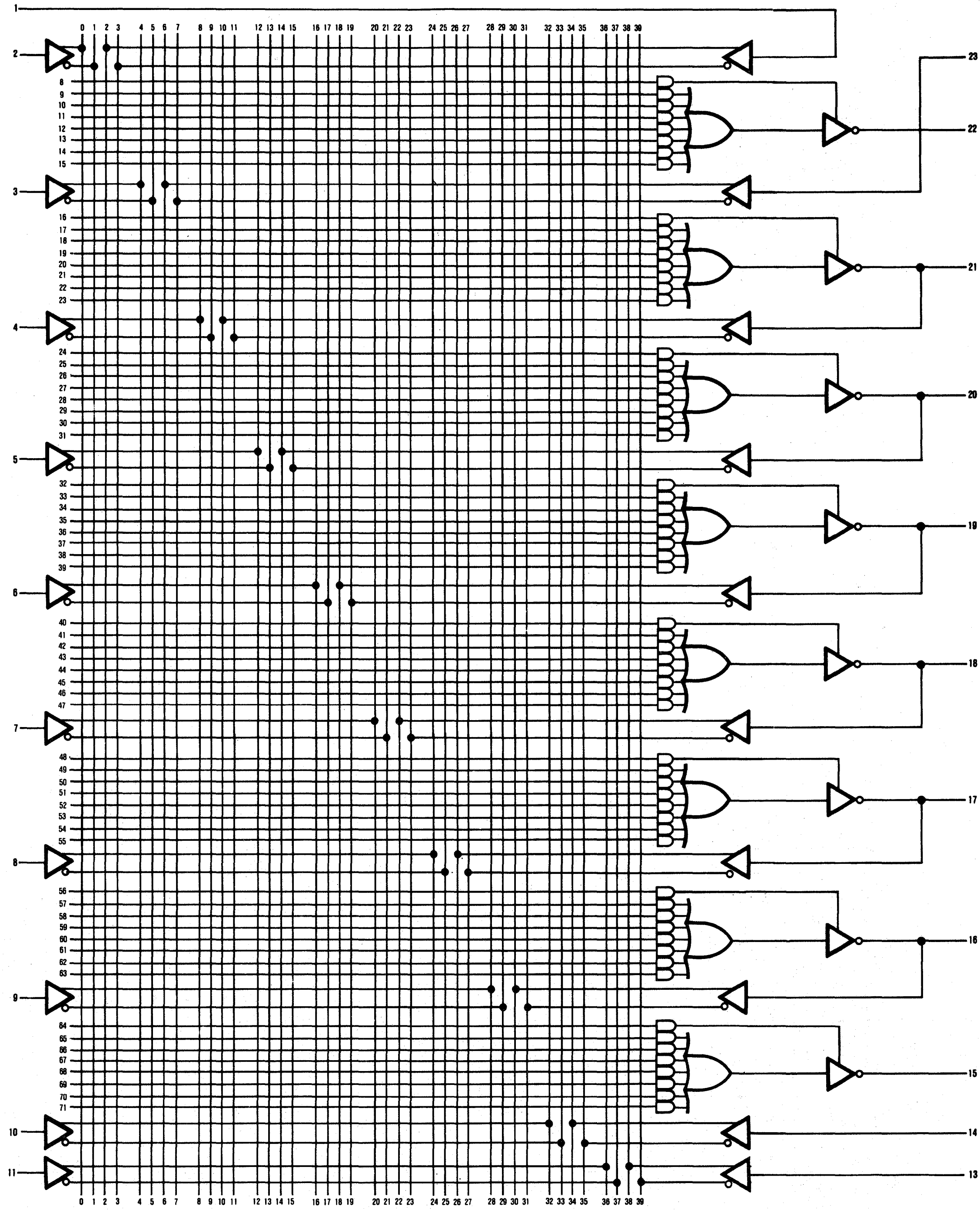
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0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
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24 25 26 27 28 29 30 31
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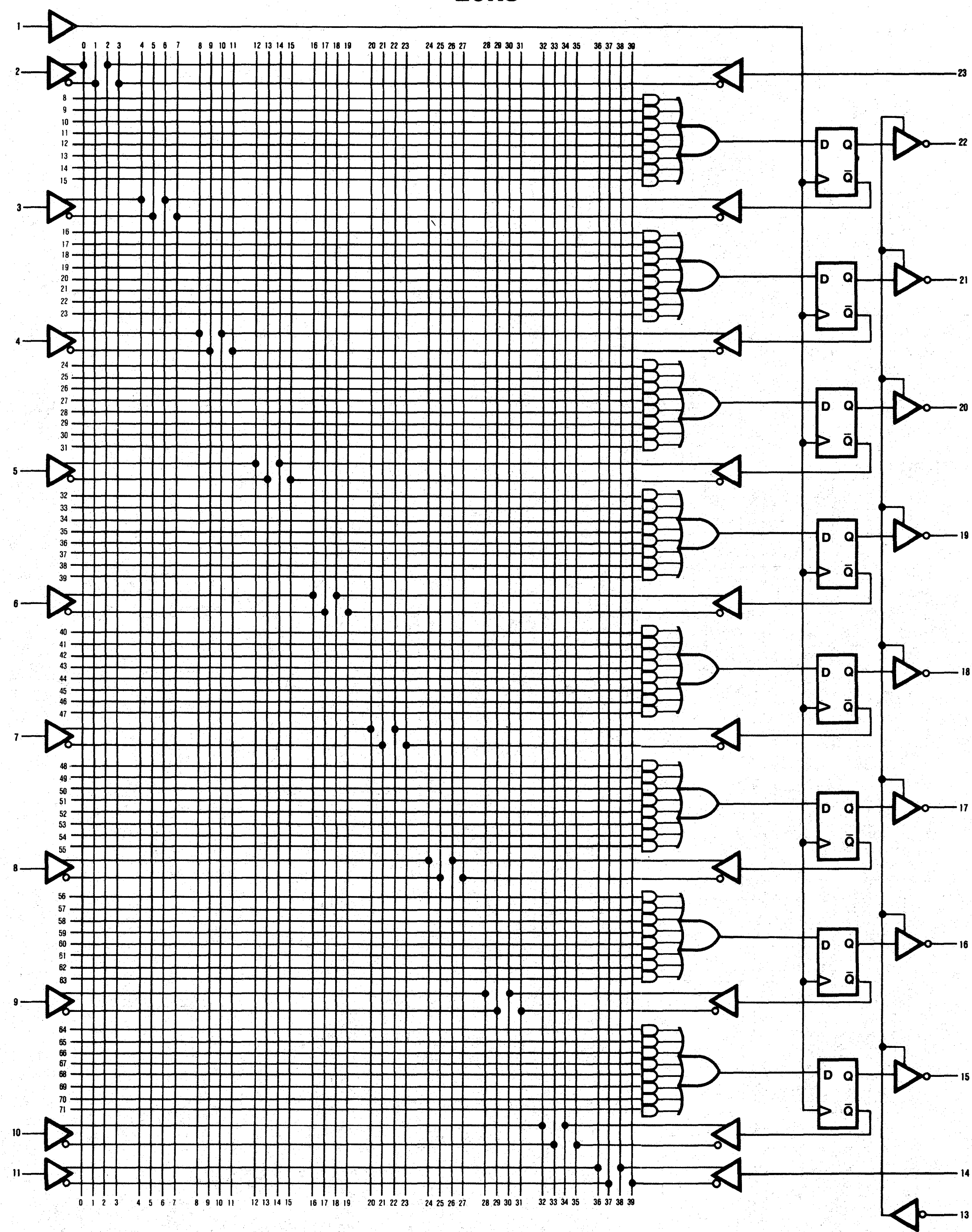
56 57 58 59 60 61 62 63
64 65 66 67 68 69 70 71

20R8



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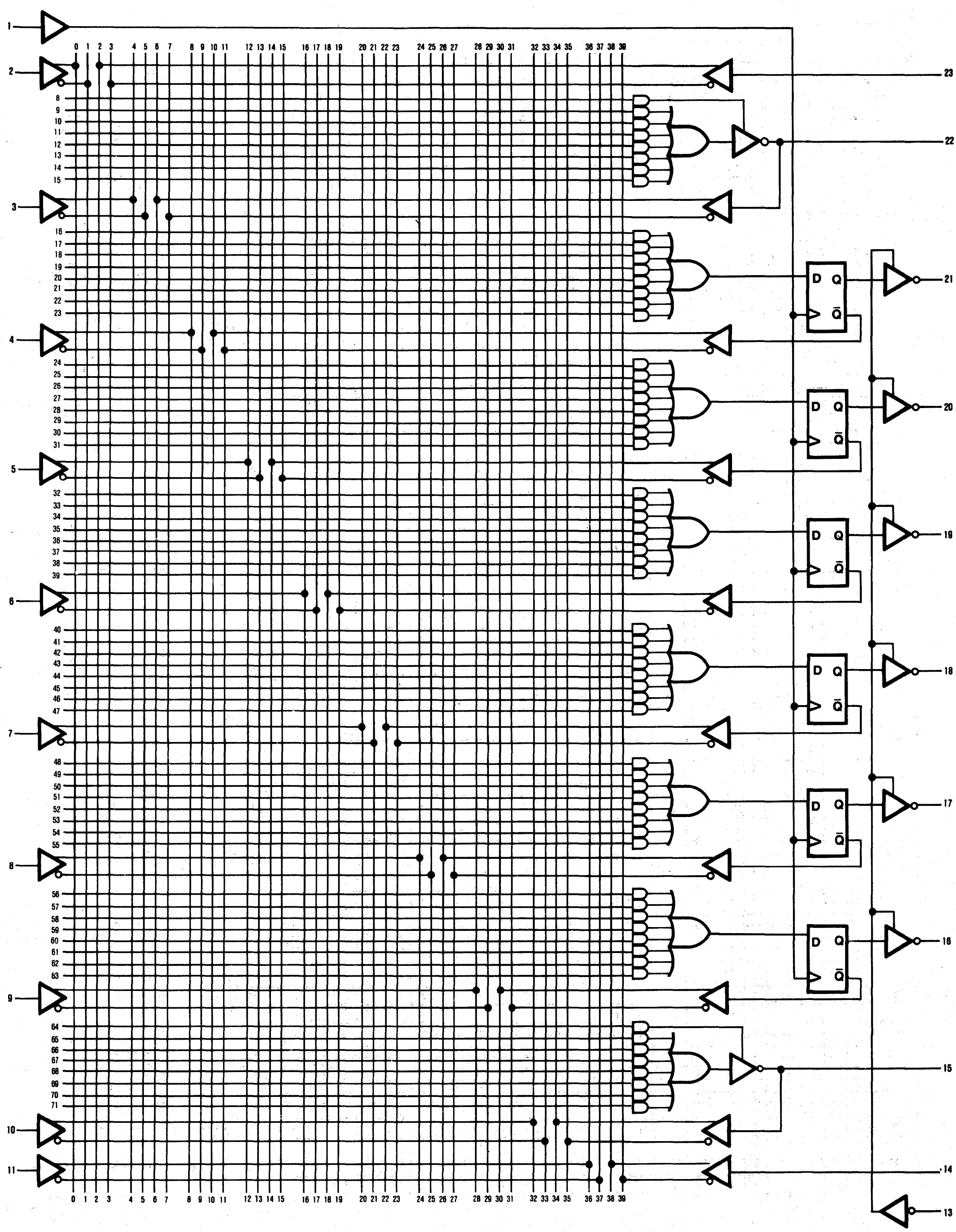
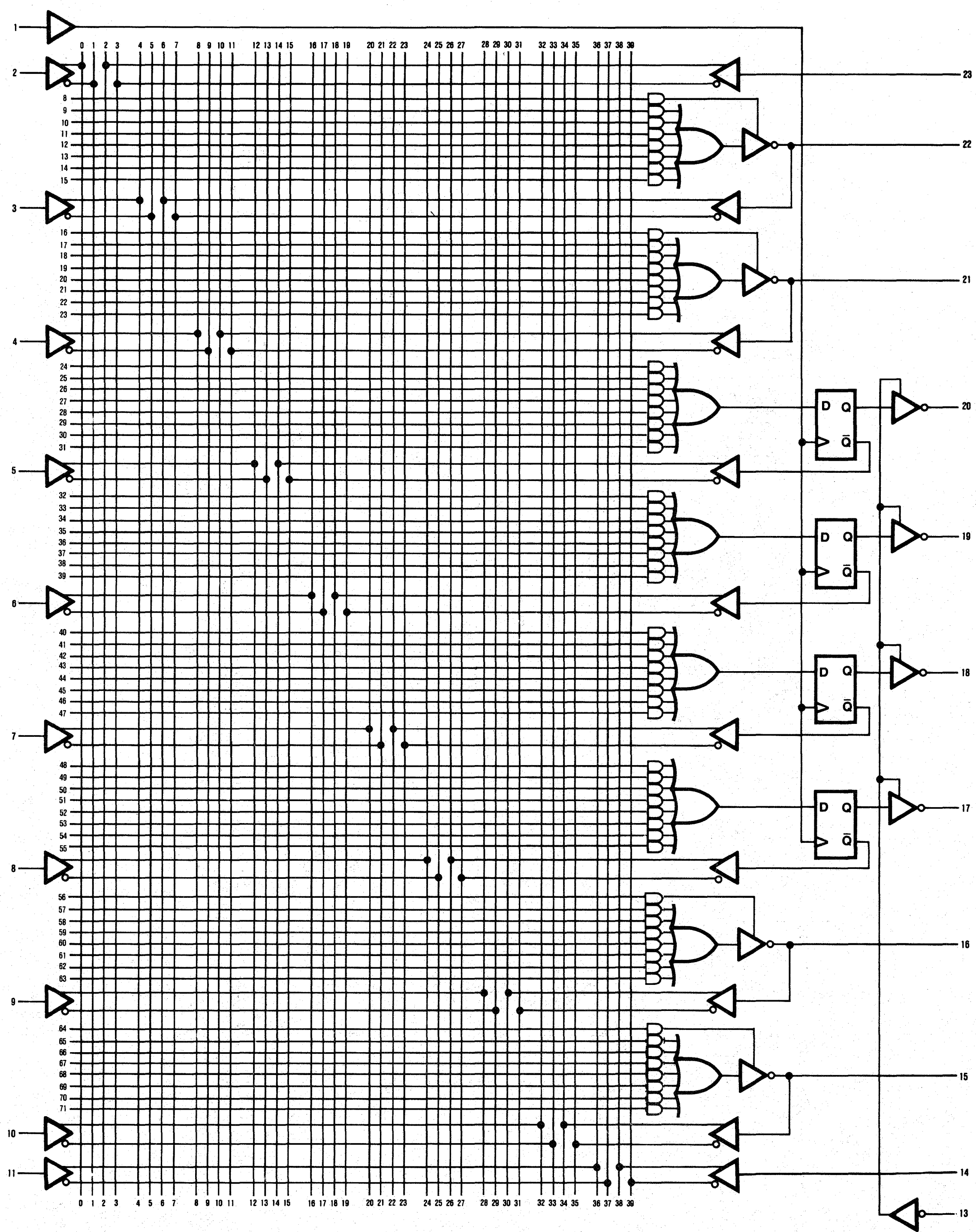


20R4



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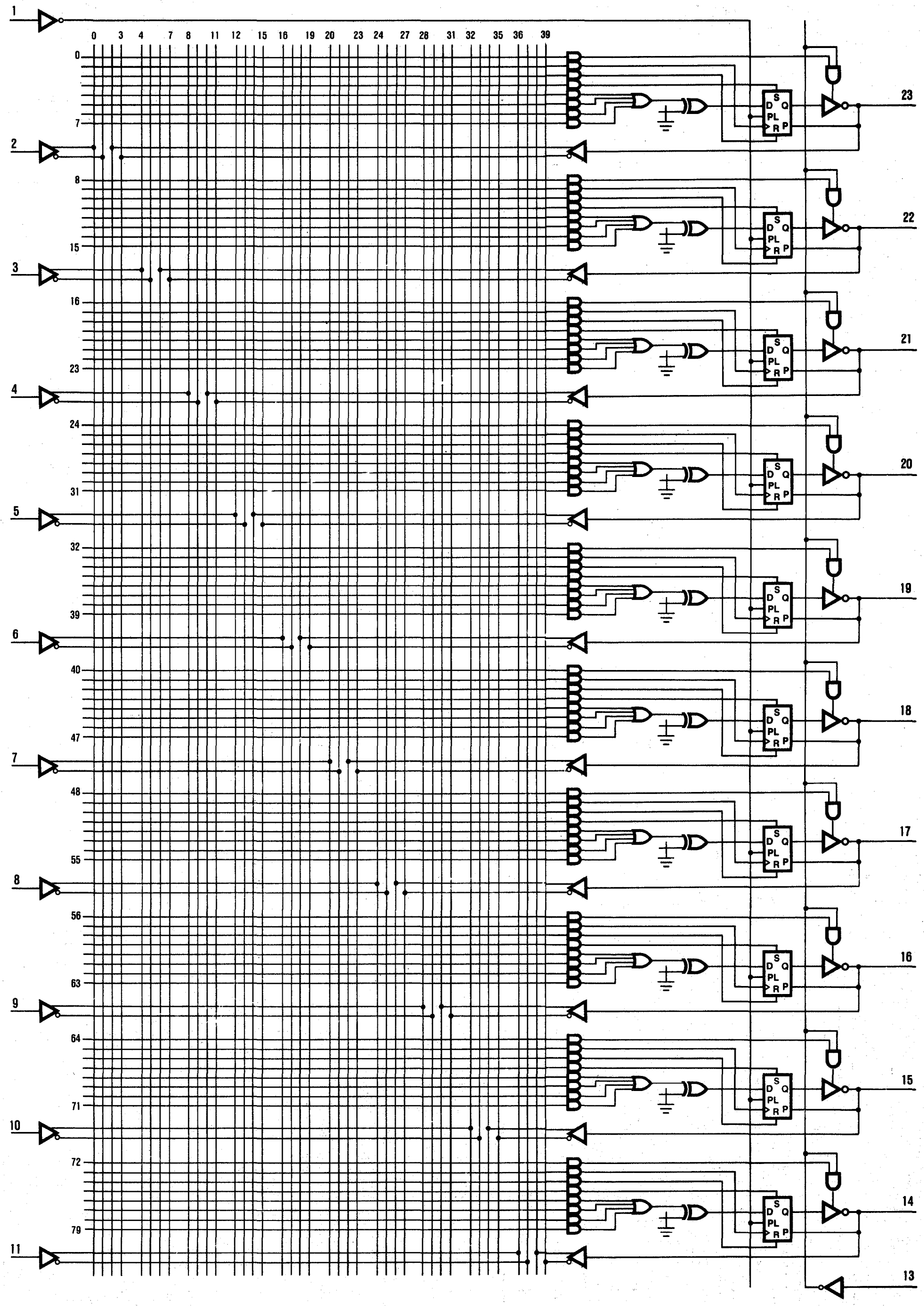
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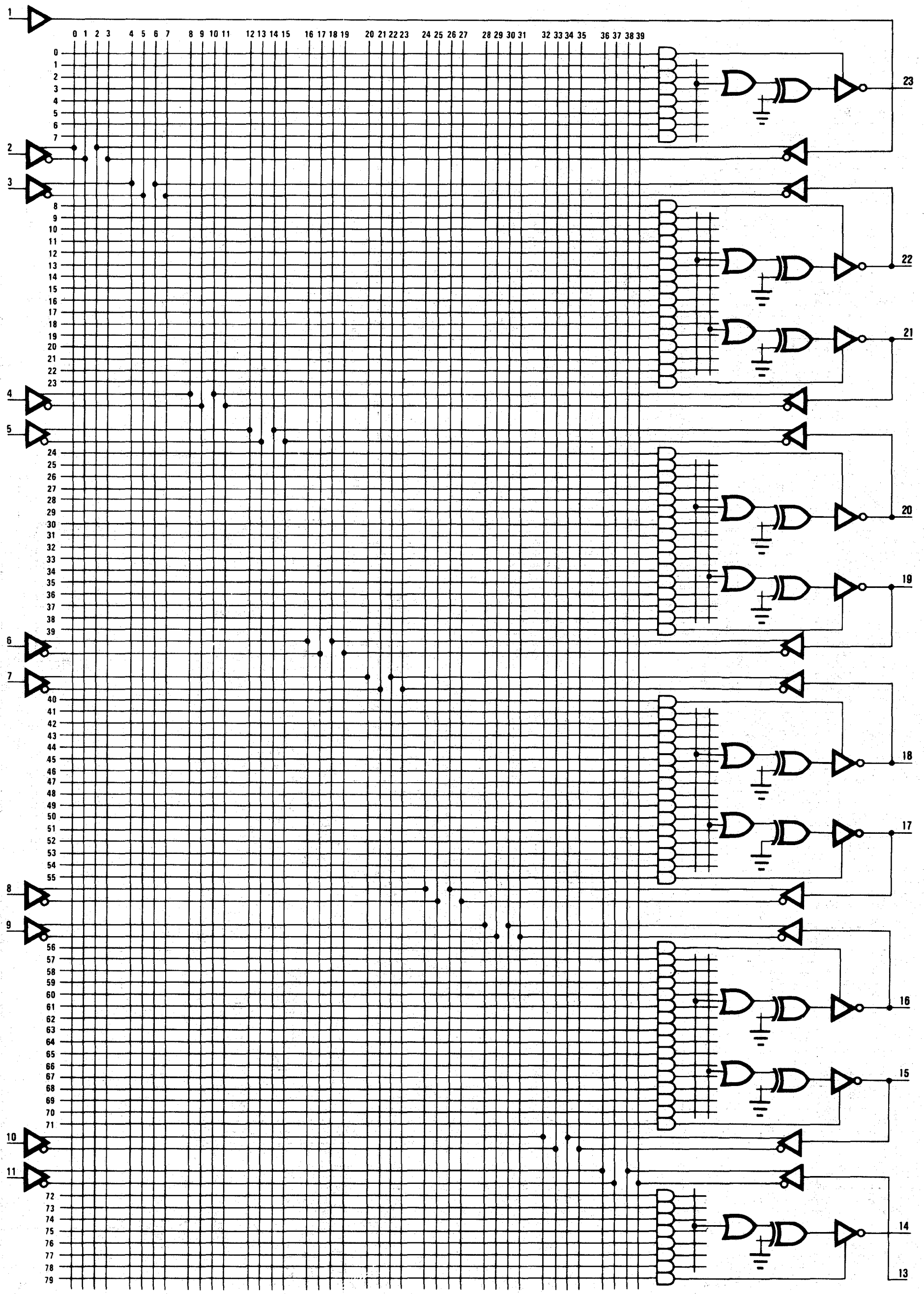
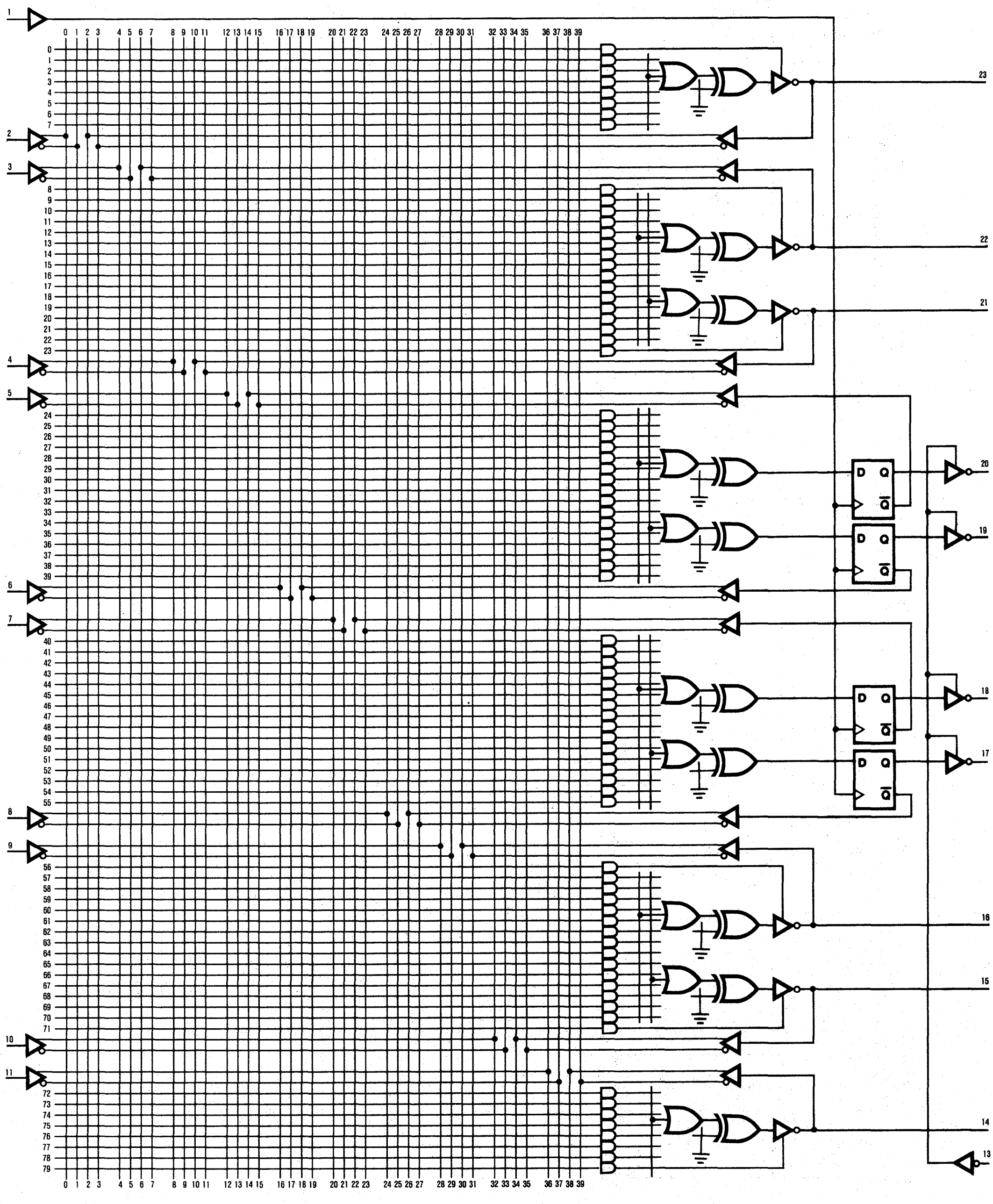
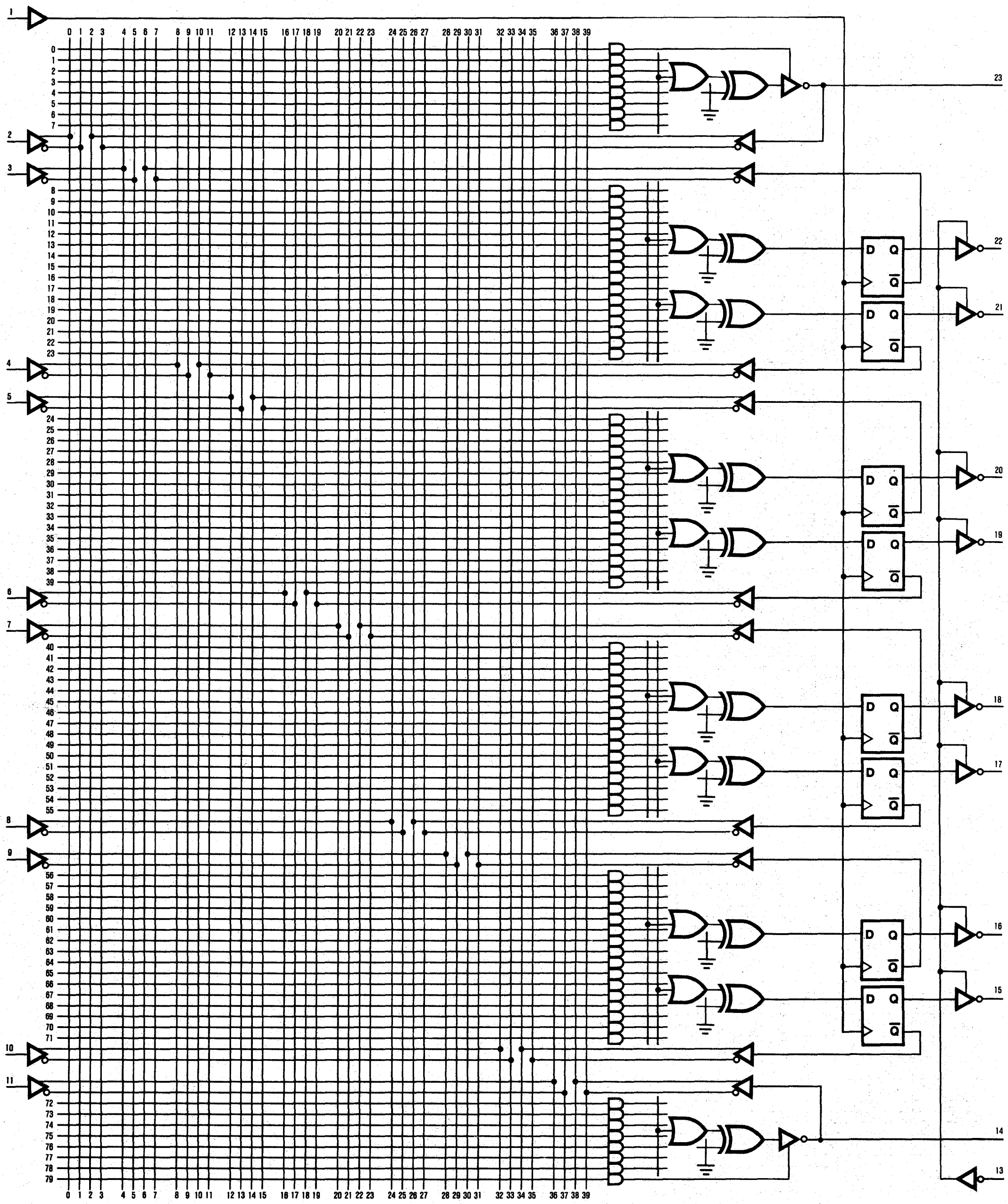
20S10



20RS4



20RS8



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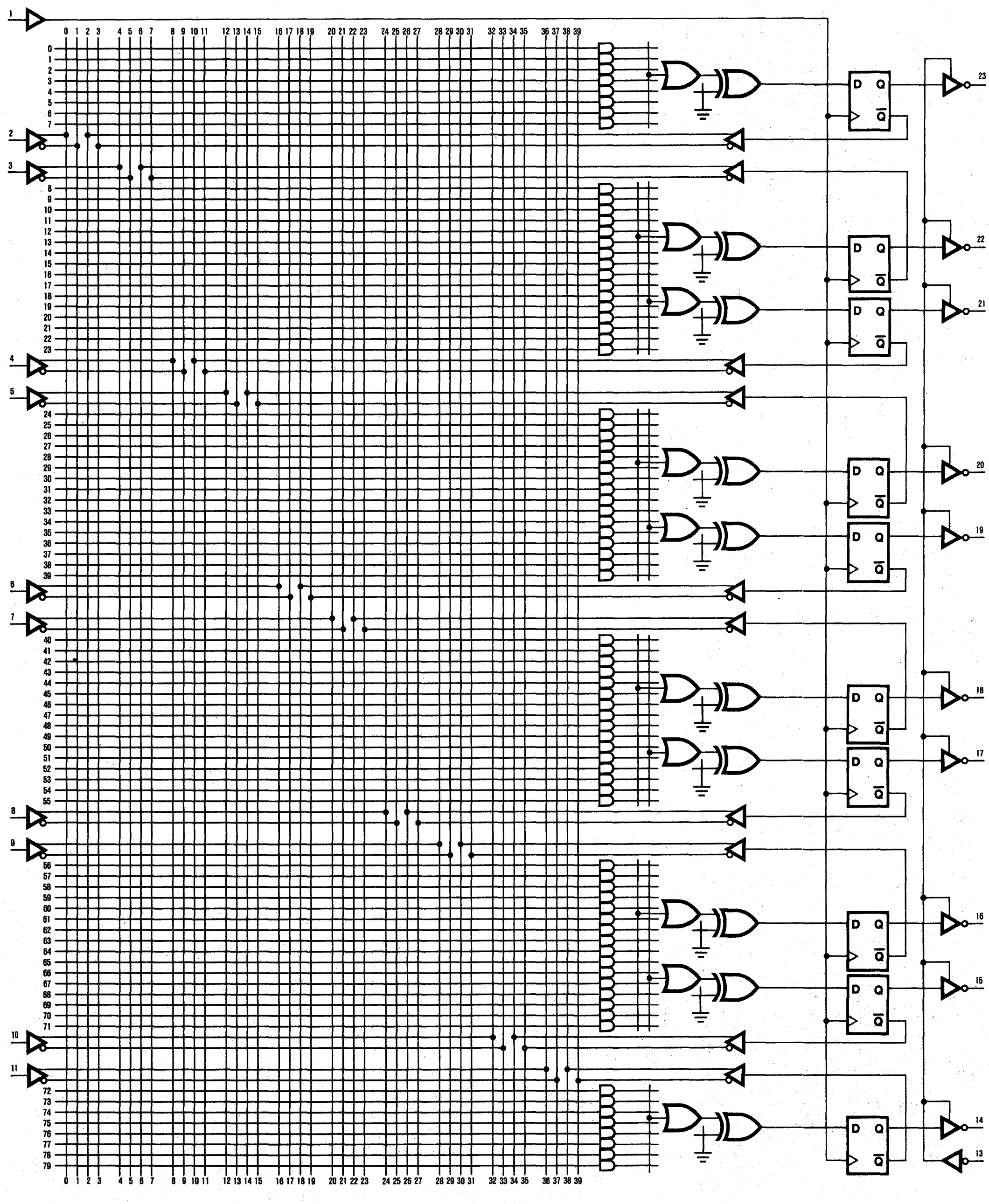
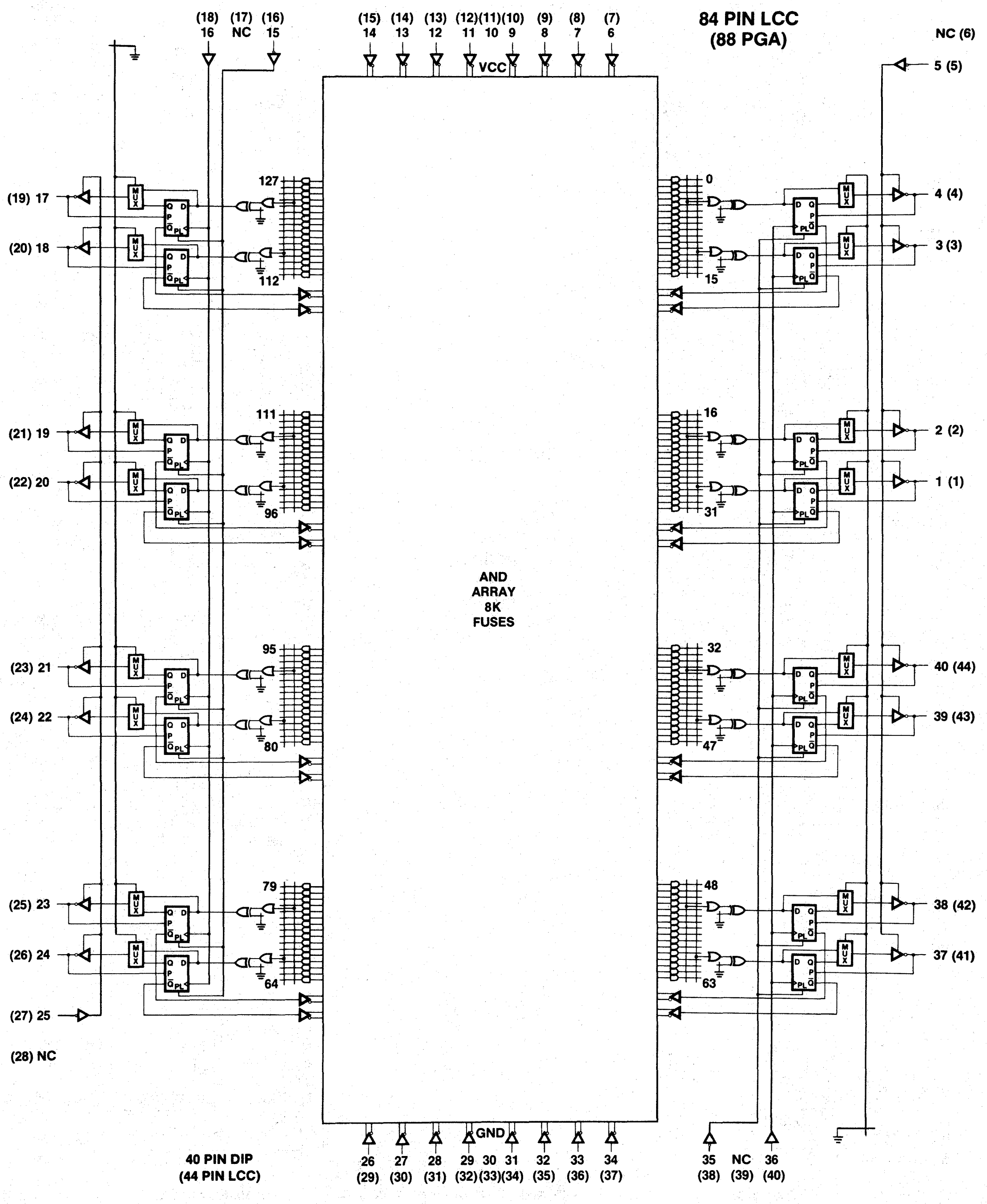


32R16


84 PIN LCC
(88 PGA)
(18) 16
(17) NC
(16) 15
(15) 14
(14) 13
(13) 12
(12) 11
(11) 10
(10) 9
(9) 8
(8) 7
(7) 6
VCC
NC (6)
5 (5)
(19) 17
(20) 18
(21) 19
(22) 20
(23) 21
(24) 22
(25) 23
(26) 24
(27) 25
(28) NC
4 (4)
3 (3)
2 (2)
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40 (44)
39 (43)
38 (42)
37 (41)
127
112
111
96
95
80
79
64
0
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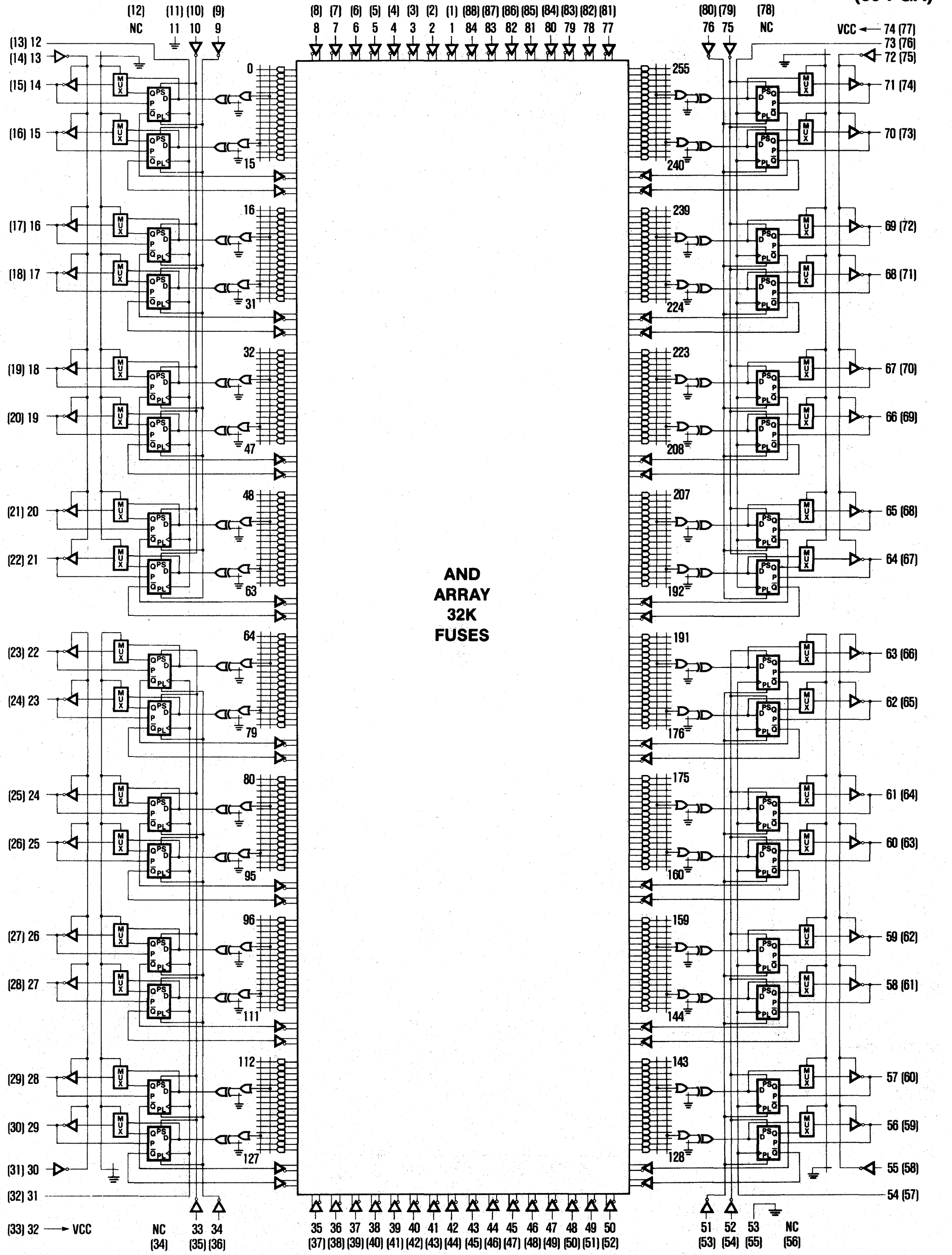
16
31
32
47
48
63
AND
ARRAY
8K
FUSES
GND
26 (29)
27 (30)
28 (31)
29 (32)
30 (33)
31 (34)
32 (35)
33 (36)
34 (37)
35 (38)
NC (39)
36 (40)
40 PIN DIP
(44 PIN LCC)

64R32

84 PIN LCC (88 PGA)



Programmer/Development System

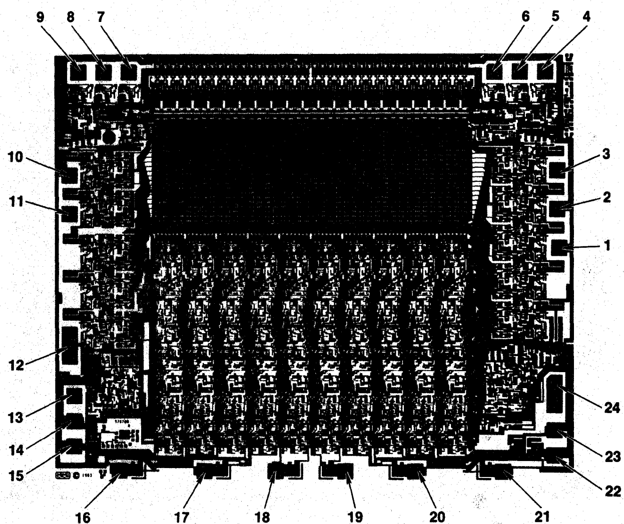
VENDOR	MegaPAL	PAL20RA10	PAL24RS	PAL20	PAL24	PAL24A
Data I/O	-Logic PAK (32R16 only)	-Logic PAK	-Logic PAK	-Logic PAK	-Logic PAK	-Logic PAK
Kontron	—	—	—	-EEP 80* PAL Adapter	-EEP 80 PAL Adapter	-EEP 80 PAL Adapter
Structured Design	—	—	—	-SD 1000	-SD 1000	-SD 1000
Stag	—	—	—	-ZL30	-ZL30	-ZL30
Varix	Omni Programmer	—	—	-Omni* Programmer	-Omni Programmer	-Omni Programmer
Valley Data Sciences	—	—	—	-Model 160	-Model 160	-Model 160
Storey Systems	—	—	—	-P240*	-P240	-P240
Digelec	—	—	—	-UP803*	-UP803	-UP803

* Except 16P8A, 16RP8A, 16RP6A, 16RP4A

The above chart represents those units which, at the time of printing, have been submitted to Monolithic Memories for evaluation and have demonstrated the capability to satisfactorily program the indicated devices.

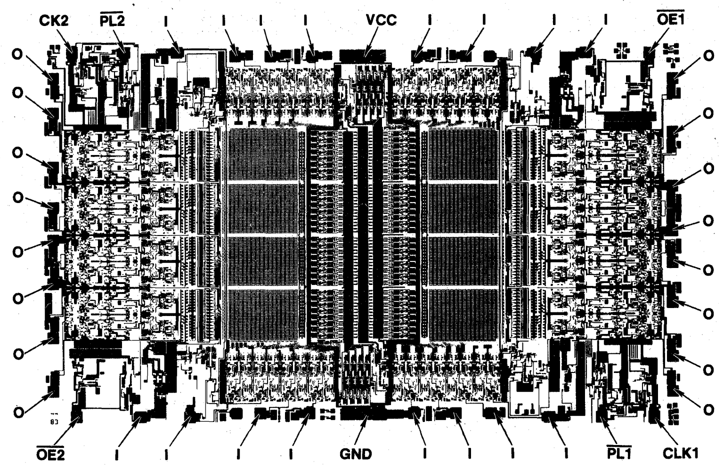
Die Configuration

PAL20RA10



Die Configurations

PAL32R16



PAL64R32

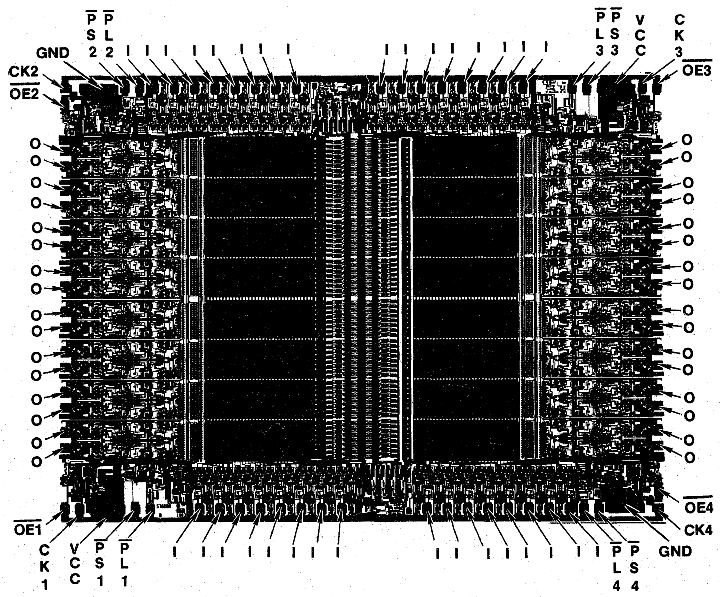


Table of Contents

SYSTEM BUILDING BLOCKS/HMSI™

System Building Blocks/HMSI Selection Guide

FUNCTION	PART NUMBER
8-Bit Counter	SN54/74LS461
8-Bit Up/Down Counter	SN54/74LS469
8-Bit Shift Register	SN54/74LS498
Multifunction 8-Bit Register	SN54/74LS380
10-Bit Counter	SN54/74LS491
16:1 Mux	SN54/74LS450
Dual 8:1 Mux	SN54/74LS451
Quad 4:1 Mux	SN54/74LS453
10-Bit Comparator	SN54/74LS460

8-Bit Counter
SN54/74LS461

Features/Benefits

- 8-bit counter for microprogram-counter, DMA-controller and general-purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading
- Expandable in 8-bit increments

Description

The 'LS461 is an 8-bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs (I0, I1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CO}$) is TRUE ($\overline{CO}$ = LOW) when the output register (Q_7-Q_0) is all HIGHs, otherwise FALSE ($\overline{CO}$ = HIGH).

The data output pins are enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more 'LS461 8-bit counters may be cascaded to provide larger counters. The operation codes were chosen such that when I1 is HIGH, I0 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

Function Table

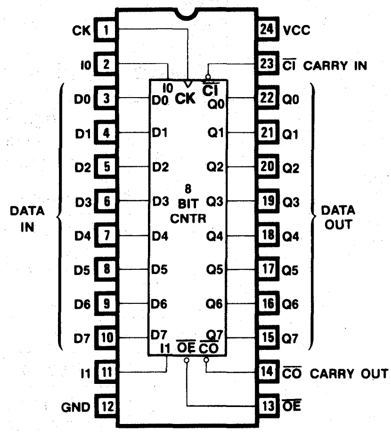
$\overline{OE}$	CK	I1	I0	$\overline{CI}$	D7-D0	Q7-Q0	OPERATION
H	*	*	*	*	*	Z	HI-Z*
L	↑	L	L	X	X	L	CLEAR
L	↑	L	H	X	X	Q	HOLD
L	↑	H	L	X	D	D	LOAD
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q plus 1	INCREMENT

* When $\overline{OE}$ is HIGH, the three-state outputs are disabled to the high-impedance states; however, sequential operation of the counter is not affected.

Ordering Information

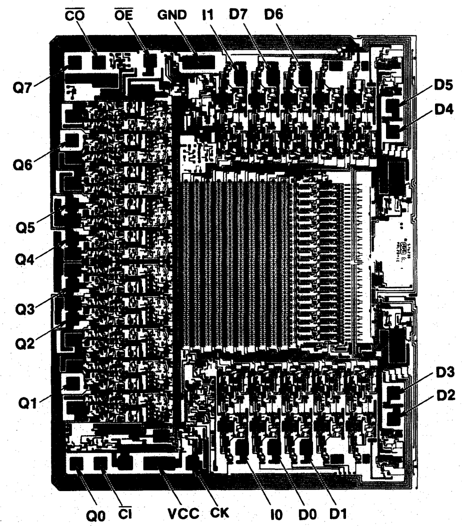
PART NUMBER	PACKAGE		TEMPERATURE
SN54LS461	JS, F	28L	MIL
SN74LS461	NS, JS		COM

Logic Symbol



Die Configuration

Die Size: 140x172 mil²



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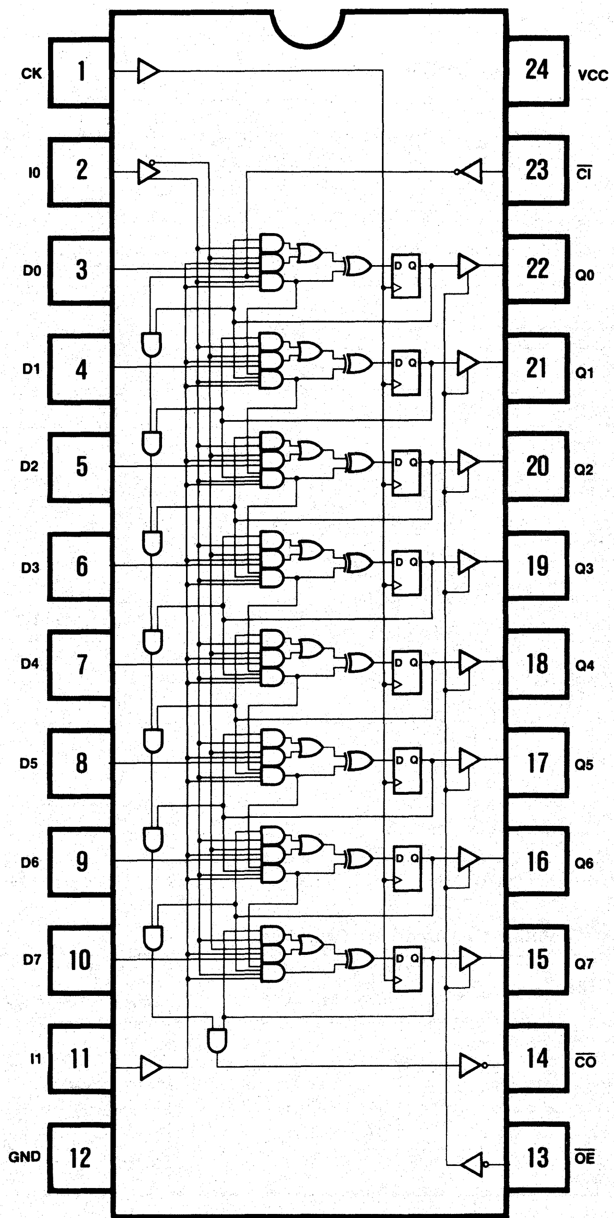
Monolithic Memories

Logic Diagram

8-Bit Counter



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		–55		125*	0		75	°C
t_w	Width of clock	Low	40			35			ns
		High	30			25			ns
t_{su}	Setup time		60			50			ns
t_h	Hold time		0	–15		0	–15		ns

* Case temperature

Electrical Characteristics Over Operating Conditions

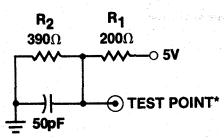
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	µA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 12mA COM I_{OL} = 24mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = –2mA COM I_{OH} = –3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX V_{IL} = 0.8V V_{IH} = 2V	V_O = 0.4V			–100	µA
I_{OZH}			V_O = 2.4V			100	µA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	–30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

* No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50 pF R_1 = 200Ω R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	$\overline{CI}$ to $\overline{CO}$ delay			35	60		35	50	ns
t_{CLK}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to $\overline{CO}$			55	95		55	80	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

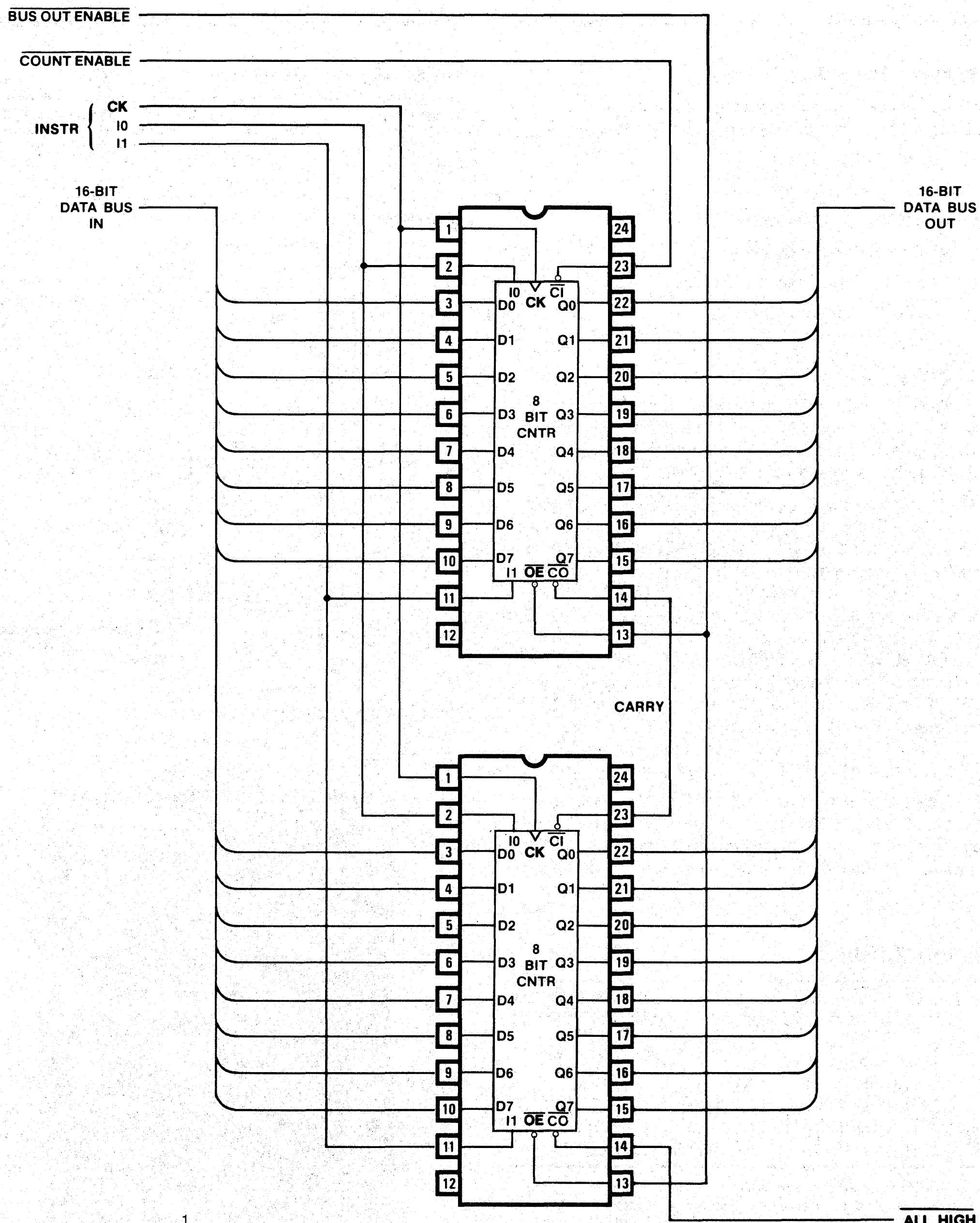
Test Load



* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Application

16-Bit Counter



NOTE: $f_{MAX} = \dfrac{1}{t_{PD\ CLK\ TO\ CO} + t_{SU}}$

8-Bit Up/Down Counter
SN54/74LS469

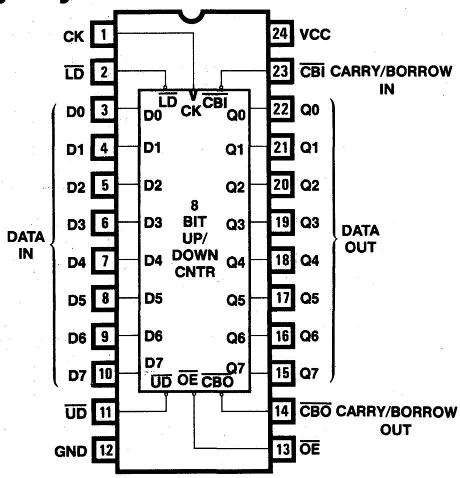
Features/Benefits

- 8-bit up/down counter for microprogram-counter, DMA-controller and general-purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading
- Expandable in 8-bit increments

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS469	JS, F	28L	MIL
SN74LS469	NS, JS		COM

Logic Symbol



Description

The 'LS469 is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs ($\overline{LD}$, $\overline{UD}$, $\overline{CBI}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CBI}$ = LOW), and the up/down control line ($\overline{UD}$) is LOW, otherwise the operation is a HOLD. The carry-out ($\overline{CBO}$) is TRUE ($\overline{CBO}$ = LOW) when the output register (Q7-Q0) is all HIGHs, otherwise FALSE ($\overline{CBO}$ = HIGH). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE ($\overline{CBI}$ = LOW), and the up/down control line ($\overline{UD}$) is HIGH, otherwise the operation is a HOLD. The borrow-out ($\overline{CBO}$) is TRUE ($\overline{CBO}$ = LOW) when the output register (Q7-Q0) is all LOWs, otherwise FALSE ($\overline{CBO}$ = HIGH).

The data output pins are enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469 8-bit up/down counters may be cascaded to provide larger counters.

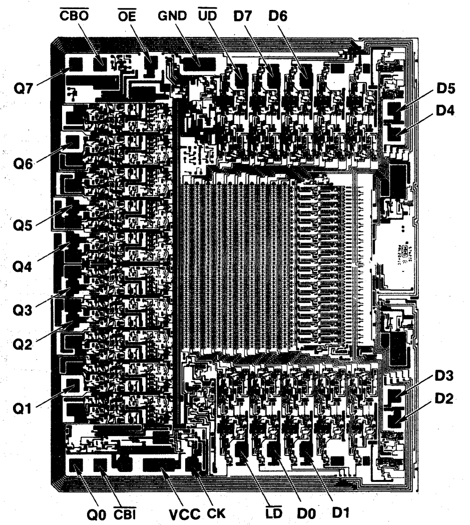
Function Table

$\overline{OE}$	CK	$\overline{LD}$	$\overline{UD}$	$\overline{CBI}$	D7-D0	Q7-Q0	OPERATION
H	*	*	*	*	*	Z	HI-Z*
L	↑	L	X	X	D	D	LOAD
L	↑	H	L	H	X	Q	HOLD
L	↑	H	L	L	X	Q plus 1	INCREMENT
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q minus 1	DECREMENT

* When $\overline{OE}$ is HIGH, the three-state outputs are disabled to the high-impedance state; however, sequential operation of the counter is not affected.

Die Configuration

Die Size: 140x172 mil^2



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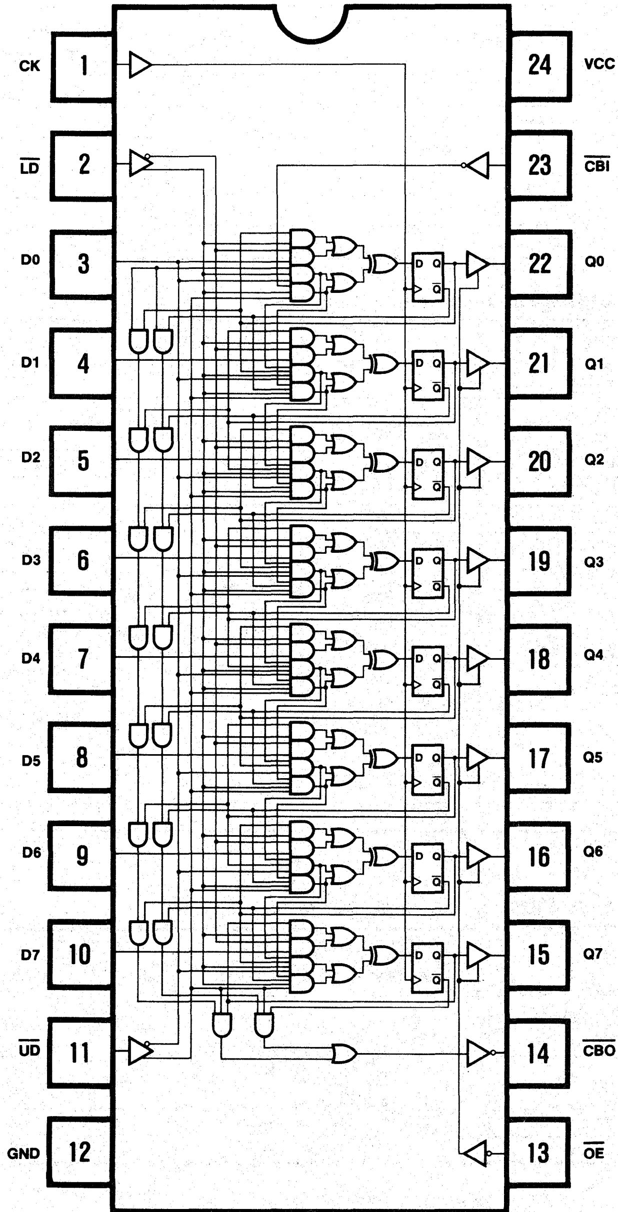
Monolithic Memories

Logic Diagram

8-Bit Up/Down Counter



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125*	0		75	°C
t_w	Width of clock	Low	40			35	10		ns
		High	30			25			ns
t_{su}	Setup time		60			50			ns
t_h	Hold time		0	−15		0	−15		ns

* Case temperature

Electrical Characteristics Over Operating Conditions

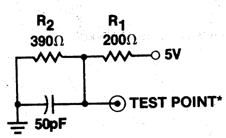
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OL} = 12mA			0.5	V
			COM I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = −2mA	2.4			V
			COM I_{OH} = −3.2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.4V			−100	μA
I_{OZH}			V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

* No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
† All typical values are V_{CC} = 5V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50 pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	$\overline{CBI}$ to $\overline{CBO}$ delay			35	60		35	50	ns
t_{CLK}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to $\overline{CBO}$			55	95		55	80	ns
t_{PZX}	Output enable delay			20	45		20	35	ns
t_{PXZ}	Output disable delay			20	45		20	35	ns

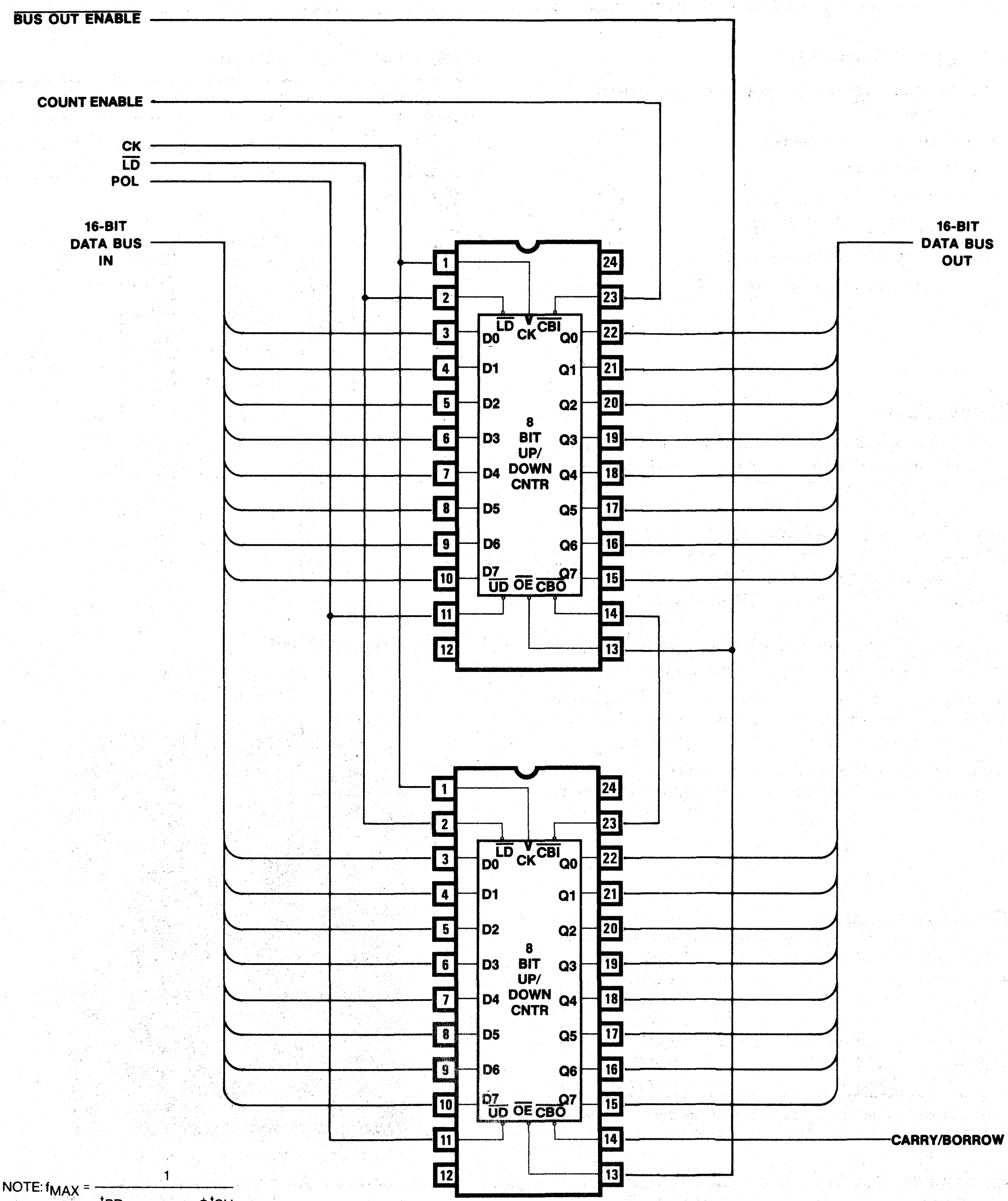
Test Load



* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Application

16-Bit Register



NOTE: $f_{MAX} = \frac{1}{t_{PD\ CLK\ TO\ CO} + t_{SU}}$

8-Bit Shift Register
SN54/74LS498

Features/Benefits
- 8-bit shift register for serial-to-parallel and parallel-to-serial applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading
- Expandable in 8-bit increments

Description
The 'LS498 is an 8-bit synchronous shift register with parallel load and hold capability. Two function select inputs (I0, I1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the input (D7-D0) into the output register (Q7-Q0). the HOLD operation holds the previous value regardless of clock transitions. The SHIFT LEFT operation shifts the output register, Q, one bit to the left; Q0 is replaced by LIRO. RILO outputs Q7.

The SHIFT right operation shifts the output register, Q, one bit to the right; Q7 is replaced by RILO. LIRO outputs Q0.

The data output pins are are enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more 'LS498 8-bit shift registers may be cascaded to provide larger shift registers as shown in the application section.

Function Table

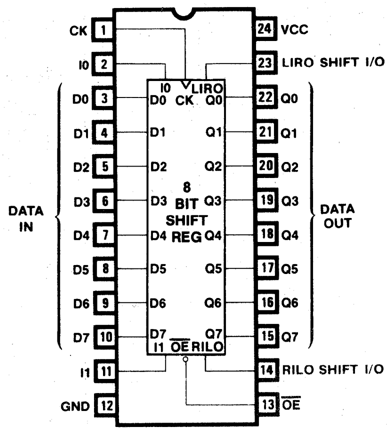
$\overline{OE}$	CK	I1	I0	D7-D0	Q7-Q0	OPERATION
H	*	*	*	*	Z	HI-Z*
L	↑	L	L	X	L	HOLD
L	↑	L	H	X	SR(Q)	SHIFT RIGHT
L	↑	H	L	X	SL(Q)	SHIFT LEFT
L	↑	H	H	D	D	LOAD

* When $\overline{OE}$ is HIGH, the three-state outputs are disabled to the high-impedance state; however, sequential operation of the register is not affected.

Ordering Information

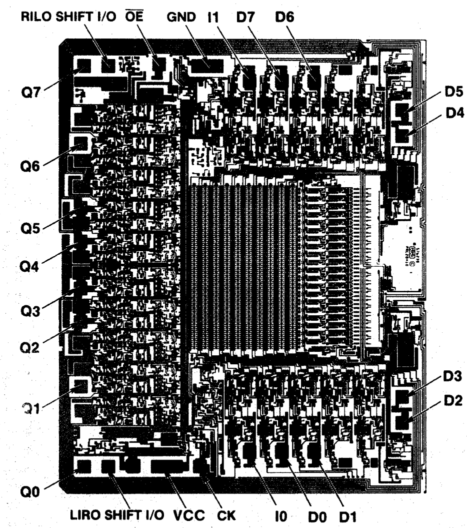
PART NUMBER	PACKAGE		TEMPERATURE
SN54LS498	JS, F	28L	MIL
SN74LS498	NS, JS		COM

Logic Symbol



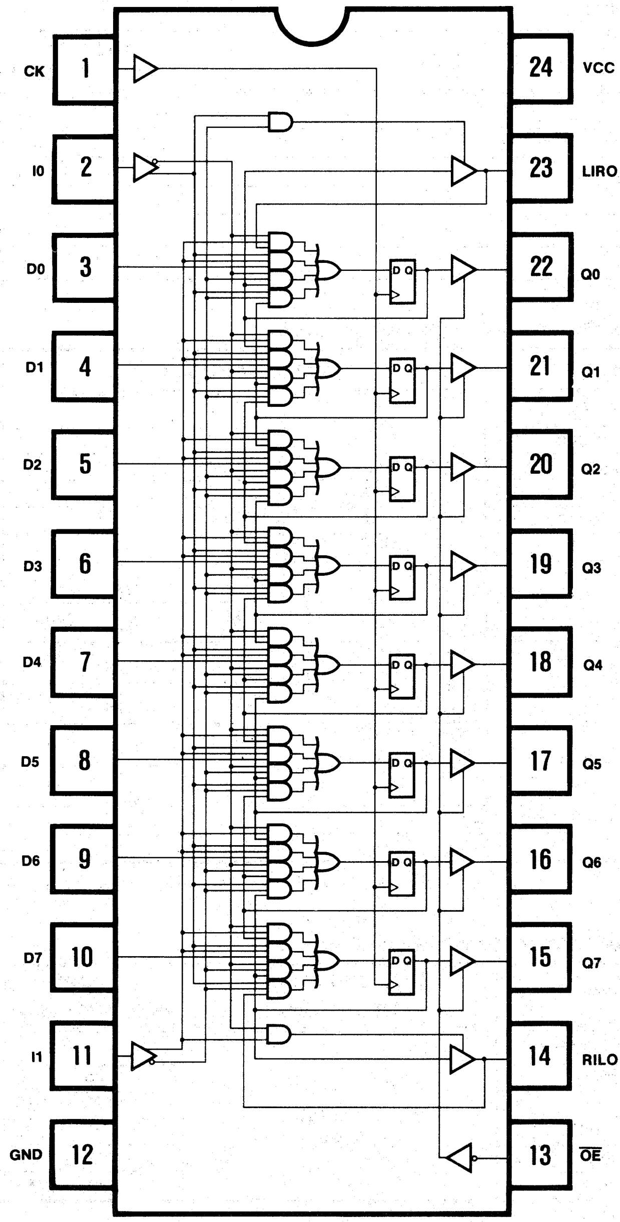
Die Configuration

Die Size: 140x172 mil^2



Logic Diagram

8-Bit Shift Register



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150° C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125*	0		75	°C
t_w	Width of clock	Low	40			35			ns
		High	30			25			ns
t_{su}	Setup time		60			50			ns
t_h	Hold time		0	−15		0	−15		ns

* Case temperature

Electrical Characteristics Over Operating Conditions

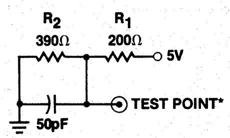
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OL} = 12mA; COM I_{OL} = 24mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = −2mA; COM I_{OH} = −3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.4V			−100	μA
I_{OZH}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

* No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50 pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	I0, I1 to LIRO, RILO			35	60		35	50	ns
t_{CLK}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to LIRO, RILO			55	95		55	80	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

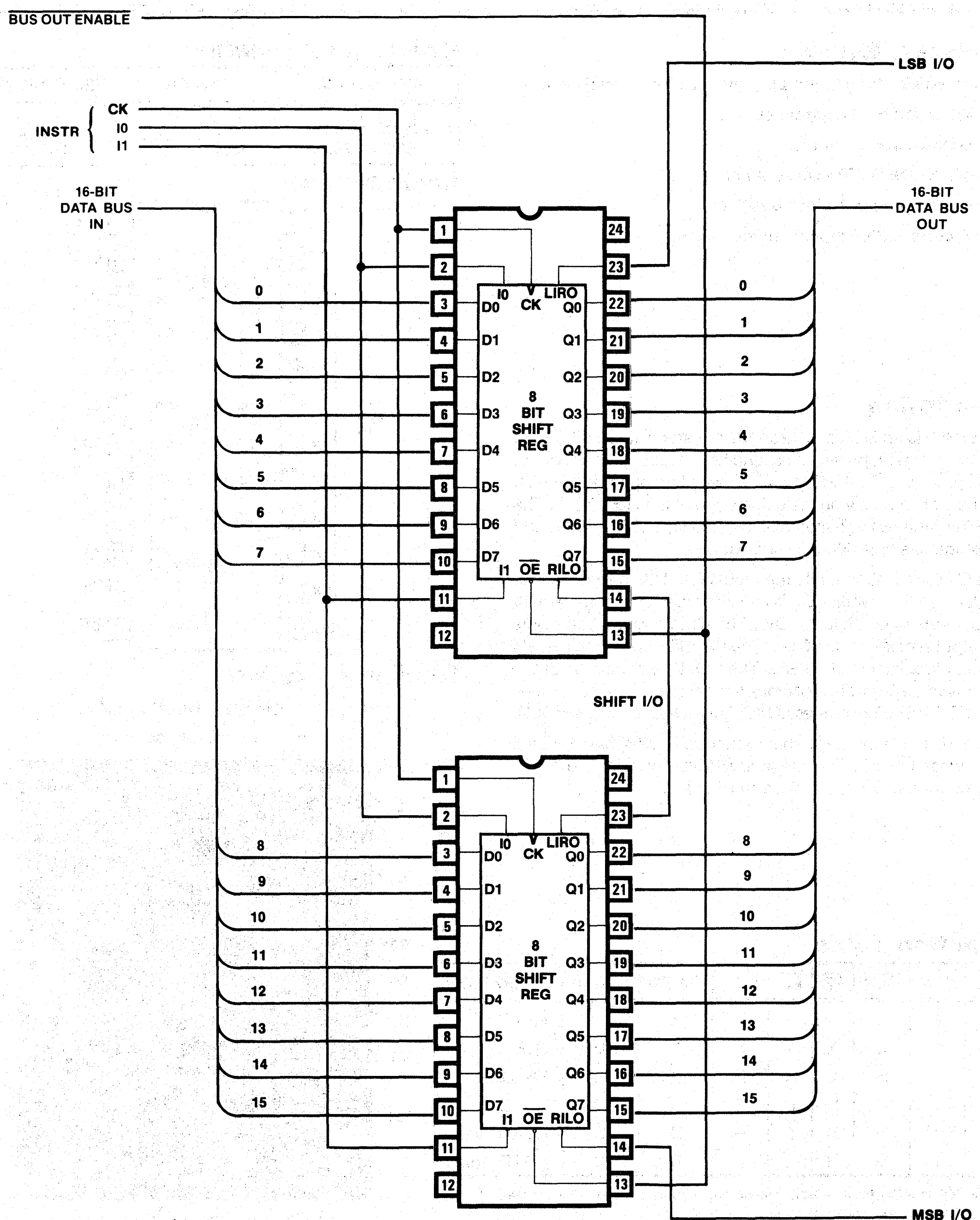
Test Load



* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Application

16-Bit Shift Register



NOTE: $f_{MAX} = \frac{1}{t_{PD\ CLK\ TO\ CO} + t_{SU}}$

* Assuming bit 15 is the MSB in the input stage

Multifunction 8-Bit Register
SN54/74LS380

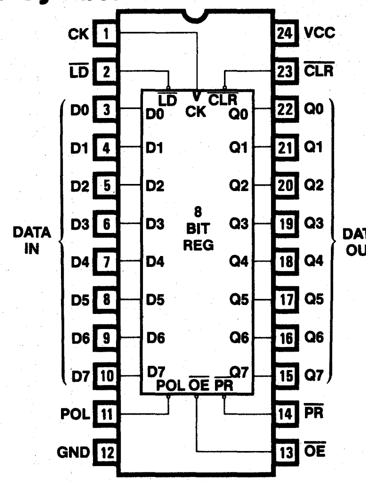
Features/Benefits

- 8-bit register for general-purpose interfacing applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS380	JS, F	28L	MIL
SN74LS380	NS, JS		COM

Logic Symbol



Description

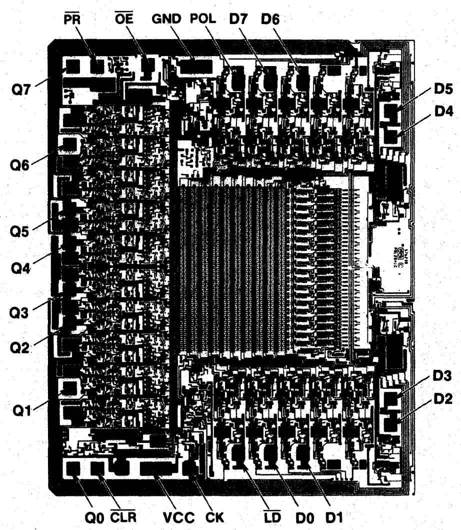
The 'LS380 is an 8-bit synchronous register with parallel load, load complement, preset, clear, and hold capacity. Four control inputs ($\overline{LD}$, POL, $\overline{CLR}$, $\overline{PR}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK). The 'LS380 combines the features of the 'LS374, 'LS377, 'LS273 and 'LS534 into a single 300-mil wide package.

The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0), when POL is HIGH, or loads the complement of the inputs when POL is LOW. The CLEAR operation resets the output register to all LOWs. The PRESET operation presets the output register to all HIGHs. The HOLD operation holds the previous value regardless of clock transitions. CLEAR overrides PRESET, PRESET overrides LOAD, and LOAD overrides HOLD.

The data output pins are enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Die Configuration

Die Size: 140x172 mil²



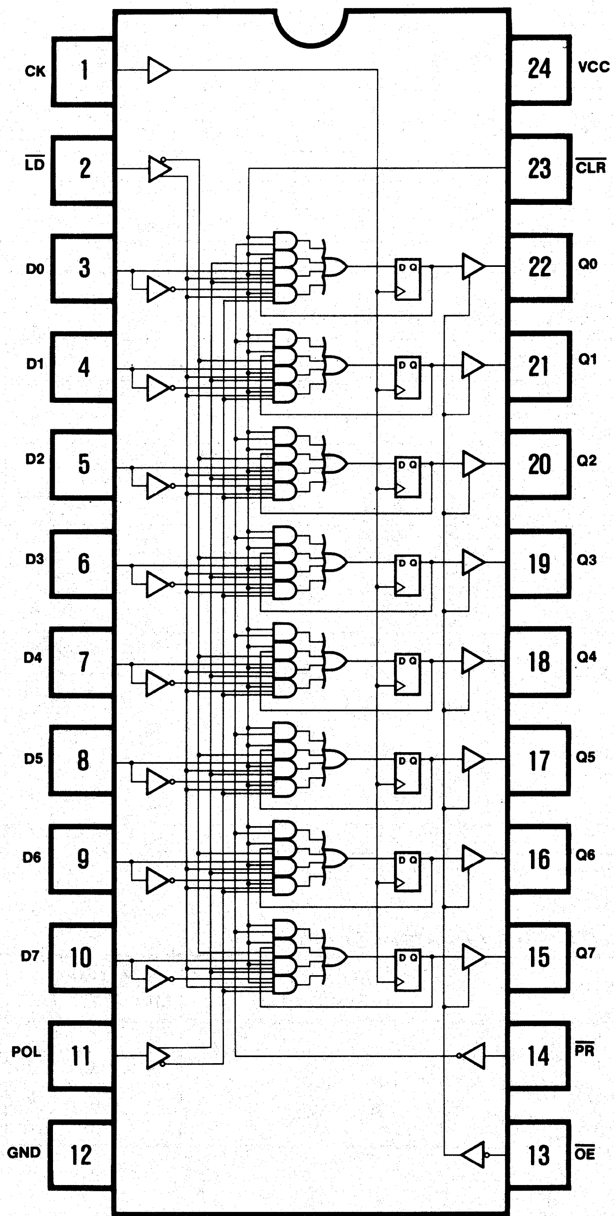
Function Table

$\overline{OE}$	CLK	$\overline{CLR}$	$\overline{PR}$	$\overline{LD}$	POL	D7-D0	Q7-Q0	OPERATION
H	*	*	*	*	*	*	Z	HI-Z*
L	↑	L	X	X	X	X	L	CLEAR
L	↑	H	L	X	X	X	H	PRESET
L	↑	H	H	H	X	X	Q	HOLD
L	↑	H	H	L	H	D	D	LOAD true
L	↑	H	H	L	L	D	$\overline{D}$	LOAD comp

* When $\overline{OE}$ is HIGH, the three-state outputs are disabled to the high-impedance state; however, sequential operation of the register is not affected.

Logic Diagram

8-Bit Register



Absolute Maximum Ratings

Supply voltage V_{CC}	7.0 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature	–65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		–55		125*	0		75	°C
t_w	Width of clock	High	40			40			ns
		Low	35			35			
t_{su}	Setup time		60			50			ns
t_h	Hold time		0	–15		0	–15		

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 12mA			0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = –2mA	2.4			V
			COM	I_{OH} = –3.2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V		V_O = 0.4V			–100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	–30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

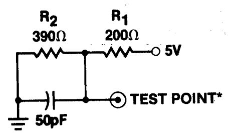
* No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{CLK}	Clock to Q			20	35		20	30	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

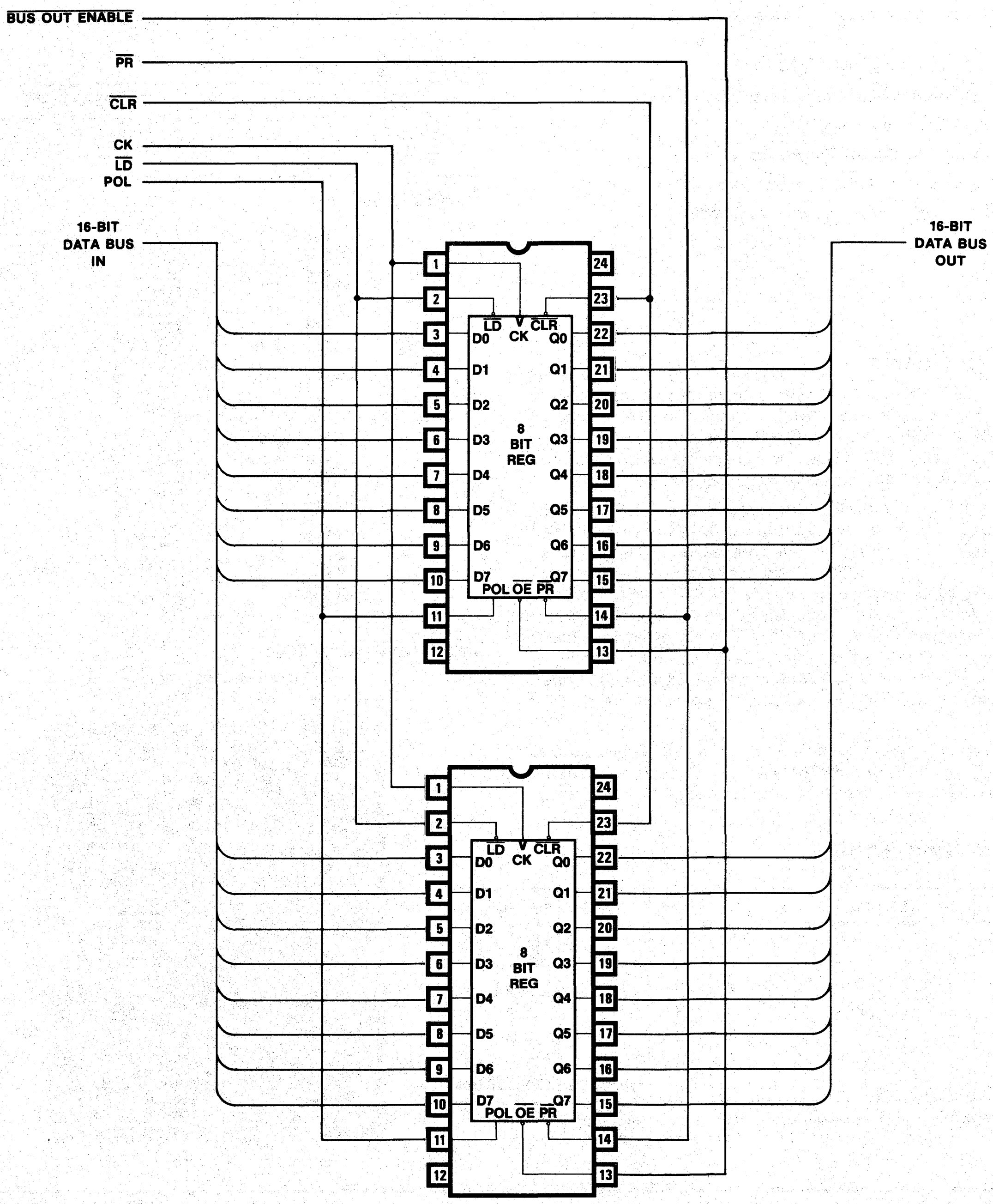
Test Load



* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Application

16-Bit Register



10-Bit Counter
SN54/74LS491

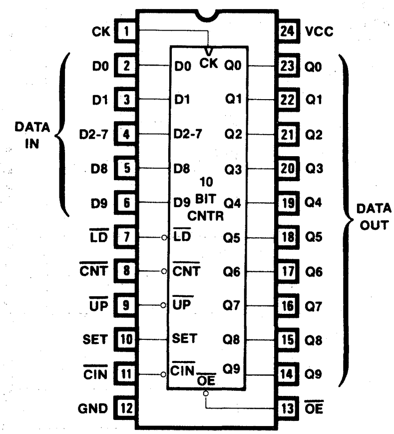
Features/Benefits

- CRT vertical and horizontal timing generation
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS491	JS, F	28L	MIL
SN74LS491	NS, JS		COM

Logic Symbol



Description

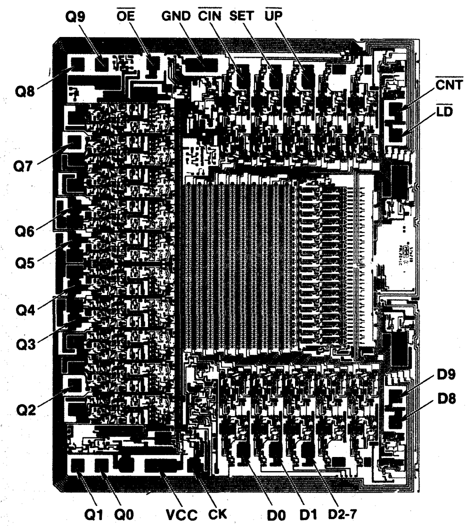
The 'LS491 is a 10-bit up/down counter with set, load and hold capabilities for two LSB, two MSB and six middle bits that are HIGH or LOW as a group. Five control inputs (SET, $\overline{LD}$, $\overline{CNT}$, $\overline{CIN}$ and $\overline{UP}$) provide one of five operations which occur synchronously on the rising edge of the clock (CK).

The SET operation sets the output register (Q9-Q0) to all HIGHs. The LOAD operation loads the inputs (D9-D0) into the register. When COUNT or CARRY IN are not asserted ($\overline{CNT}$ = HIGH or $\overline{CIN}$ = HIGH), the HOLD operation holds the previous value regardless of clock transitions. The COUNT UP operation adds one to the output of the register when the count up input is asserted ($\overline{UP}$ = LOW). The COUNT DOWN operation subtracts one from the output register when the count up input is not asserted ($\overline{UP}$ = HIGH). SET overrides both LOAD and COUNT, LOAD overrides COUNT, and COUNT is conditional on CARRY IN.

The data output pins are enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The 24 mA I_{OL} outputs are suitable for driving RAM/PROM address lines in video graphics systems.

Die Configuration

Die Size: 140x172 mil^2



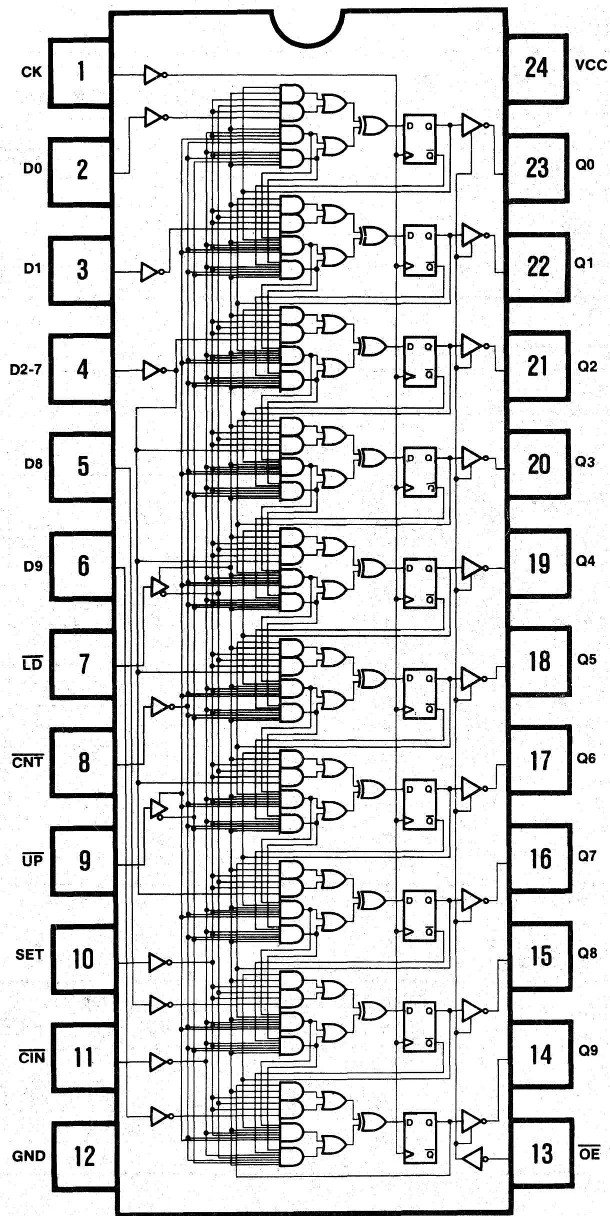
Function Table

$\overline{OE}$	CK	SET	$\overline{LD}$	$\overline{CNT}$	$\overline{CIN}$	$\overline{UP}$	D9-D0	Q9-Q0	OPERATION
H	*	*	*	*	*	*	*	Z	HI-Z*
L	↑	H	X	X	X	X	X	H	SET all HIGH
L	↑	L	L	X	X	X	D	D	LOAD D
L	↑	L	H	H	X	X	X	Q	HOLD
L	↑	L	H	L	H	X	X	Q	HOLD
L	↑	L	H	L	L	L	X	Q plus 1	COUNT UP
L	↑	L	H	L	L	H	X	Q minus 1	COUNT DN

* When $\overline{OE}$ is HIGH, the three-state outputs are disabled to the high-impedance states; however, sequential operation of the counter is not affected.

Logic Diagram

10-Bit Up/Down Counter



6

Absolute Maximum Ratings

Supply voltage V_{CC}	7.0 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature	–65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		–55		125*	0		75	°C
t_w	Width of clock	High	40			40			ns
		Low	35			35			
t_{su}	Setup time		60			50			ns
t_h	Hold time		0	–15		0	–15		

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OL} = 12mA COM I_{OL} = 24mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = –2mA COM I_{OH} = –3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.4V			–100	μA
I_{OZH}			V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	–30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

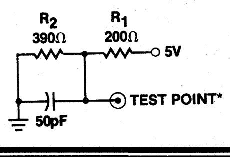
* No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{CLK}	Clock to Q			20	35		20	30	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

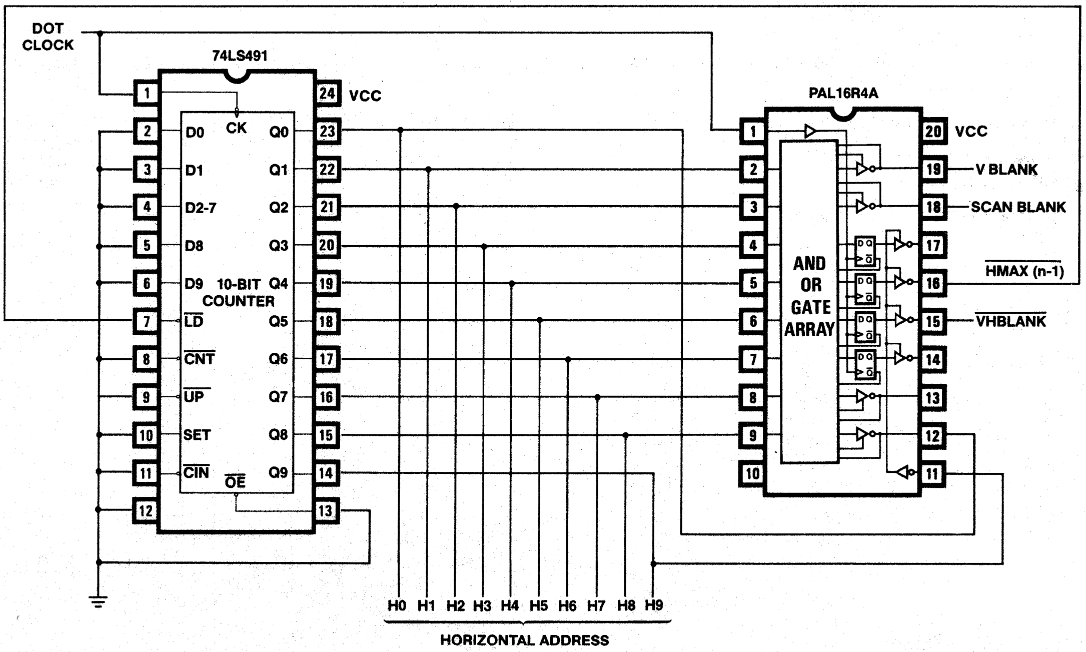
Test Load



* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Application

Video Horizontal Timing and Blanking



Timing Analysis:

Path 1 — Outputs of 74LS491 setting up at PAL16R4A inputs

$$t_{PD_{CK\text{-}Q/74LS491}} + t_{SU_{PAL16R4A}}$$

= 30 ns + 25 ns

= 55 ns

Path 2 — Outputs of PAL16R4A setting up at 74LS491 inputs

$$t_{PD_{CK\text{-}Q/PAL16A}} + t_{SU_{74LS491}}$$

= 25 ns + 50 ns

= 75 ns

Accordingly, the worst-case timing of the two paths is 75 ns, which results in a maximum video dot clock frequency of 13.33 MHz. Strict interpretation of the 60 Hz field rate NTSC Standard suggests that up to 52.1 μsec of time is available for active-raster-line duration. In practice however, most CRT monitors overscan the screen to correct horizontal sweep nonlinearities. As a consequence, the horizontal blanking time is increased, and the active video time decreased, typically to about 40 μsec. For the application circuit shown above, over 512 dots (pixels) for one line can be displayed:

$$\frac{40\ \mu\text{sec per line}}{75\ \text{ns per pixel per line}} \doteq 533\ \text{pixels}$$

Normally, at least a 10-bit counter is required to provide a video timing chain for such resolutions. The 74LS491, combined with a high-speed PAL (PAL16R4A) is capable of generating a complete set of video timing signals. Note that in the application circuit, the maximum horizontal count [H MAX (n-1)] is decoded one clock early, due to the 1-level pipelining used to obtain circuit speed.

16:1 Mux
SN54/74LS450

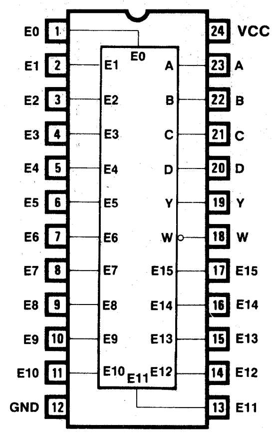
Features/Benefits

- 24-pin SKINNYDIP® saves space
- Similar to 74150 (Fat DIP)
- Low-current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS450	JS, F	28L	MIL
SN74LS450	NS, JS		COM

Logic Symbol



Description

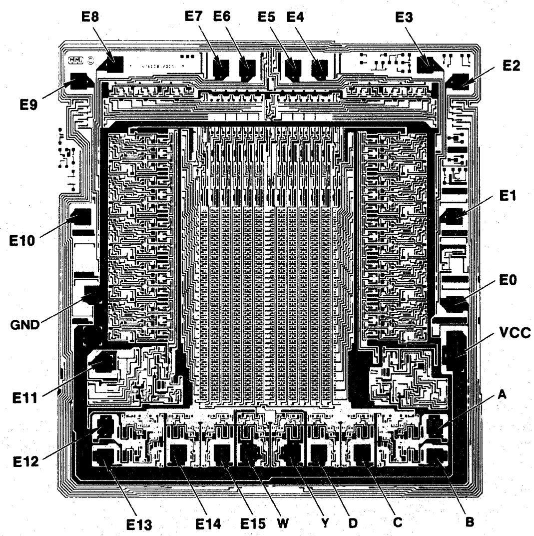
The 16:1 Mux selects one of sixteen inputs, E0 through E15, specified by four binary select inputs, A, B, C and D. The true data is output on Y and the inverted data on W. Propagation delays are the same for both inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem-pole drive standard.

Function Table

INPUT SELECT				OUTPUT	
D	C	B	A	W	Y
L	L	L	L	$\overline{E0}$	E0
L	L	L	H	$\overline{E1}$	E1
L	L	H	L	$\overline{E2}$	E2
L	L	H	H	$\overline{E3}$	E3
L	H	L	L	$\overline{E4}$	E4
L	H	L	H	$\overline{E5}$	E5
L	H	H	L	$\overline{E6}$	E6
L	H	H	H	$\overline{E7}$	E7
H	L	L	L	$\overline{E8}$	E8
H	L	L	H	$\overline{E9}$	E9
H	L	H	L	$\overline{E10}$	E10
H	L	H	H	$\overline{E11}$	E11
H	H	L	L	$\overline{E12}$	E12
H	H	L	H	$\overline{E13}$	E13
H	H	H	L	$\overline{E14}$	E14
H	H	H	H	$\overline{E15}$	E15

Die Configuration

Die Size: 140x131 mil^2



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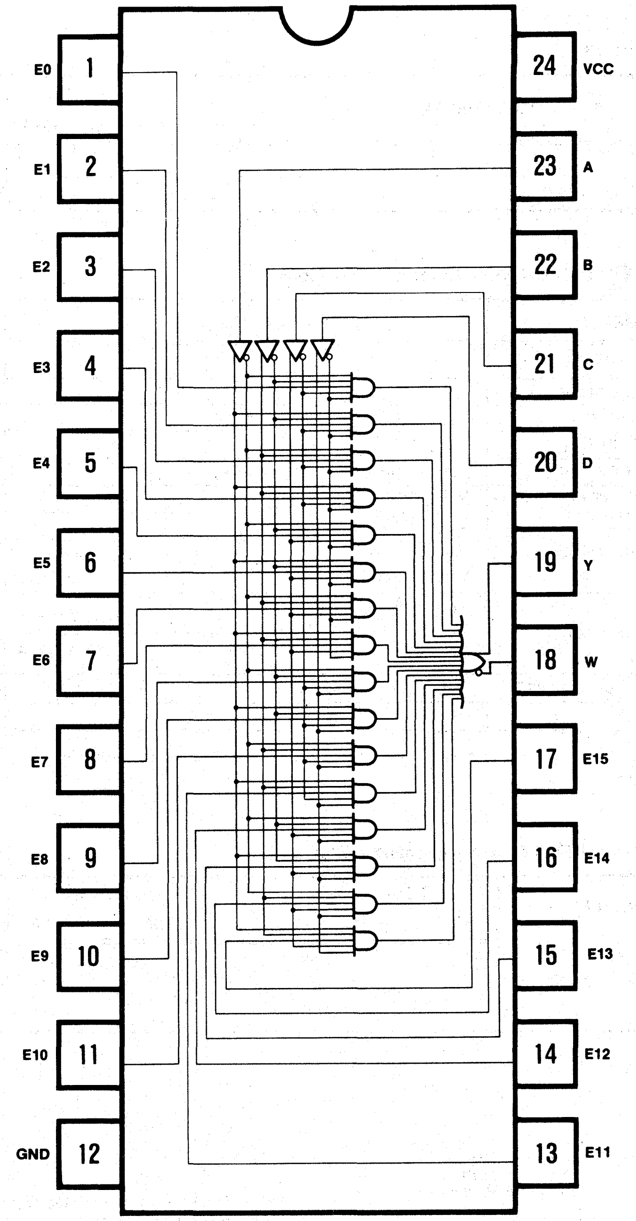
Logic Diagram

16:1 Mux



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125*	0		75	°C

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX, V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V; I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V; MIL I_{OH} = –2mA; COM I_{OH} = –3.2mA	2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V, V_O = 0V	–30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX		60	100	mA

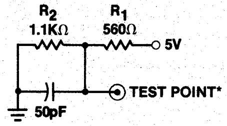
* No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Any input to Y or W	C_L = 50 pF, R_1 = 560Ω, R_2 = 1.1kΩ		25	45		25	40	ns

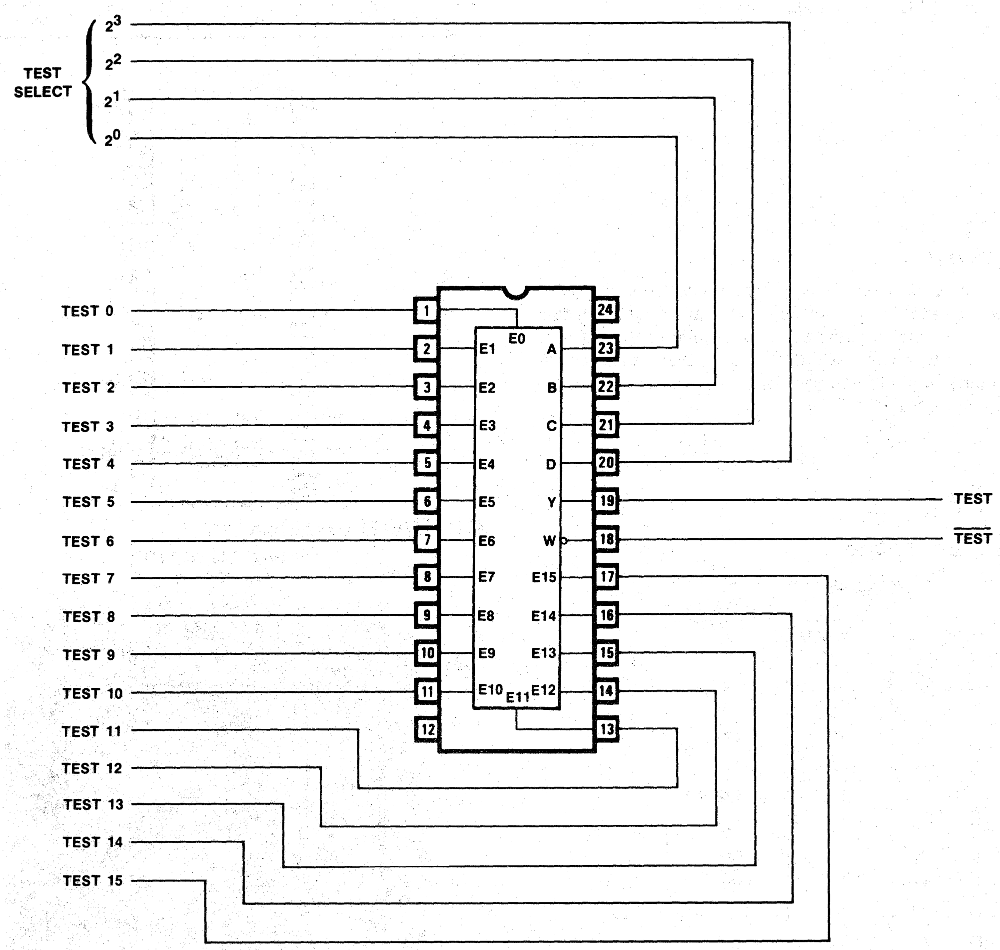
Test Load



* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Application

Test Condition Mux



Dual 8:1 Mux
SN54/74LS451

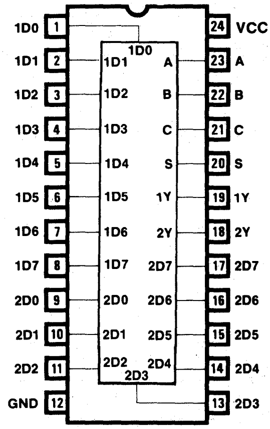
Features/Benefits

- 24-pin SKINNYDIP® saves space
- Twice the density of 74LS151
- Low-current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS451	JS, F	28L	MIL
SN74LS451	NS, JS		COM

Logic Symbol

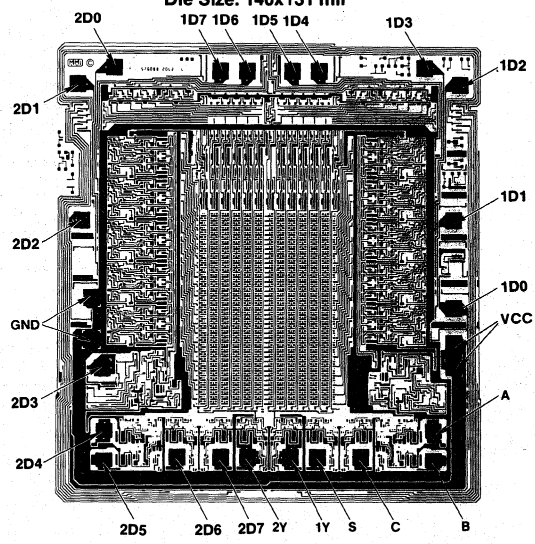


Description

The Dual 8:1 Mux selects one of eight inputs, D0 through D7, specified by three binary select inputs, A, B and C. The true data is output on Y when strobed by S. Propagation delays are the same for inputs, addresses and strobes and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem-pole drive standard.

Die Configuration

Die Size: 140x131 mil^2



Function Table

INPUTS				OUTPUTS
SELECT			STROBE	Y
C	B	A	S	
X	X	X	H	H
L	L	L	L	D0
L	L	H	L	D1
L	H	L	L	D2
L	H	H	L	D3
H	L	L	L	D4
H	L	H	L	D5
H	H	L	L	D6
H	H	H	L	D7

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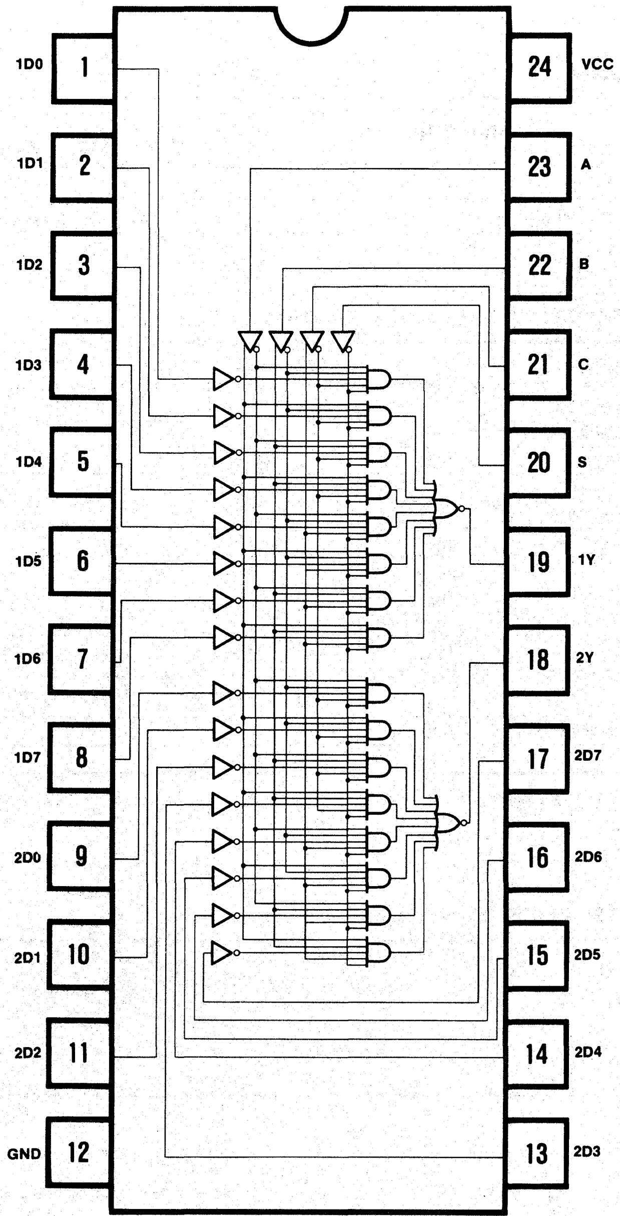
Monolithic Memories

Logic Diagram

Dual 8:1 Mux



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... –65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125*	0		75	°C

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	µA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = –2mA COM I_{OH} = –3.2mA	2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	–30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX			60	100	mA

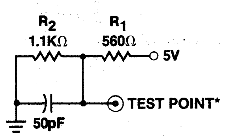
* No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Any input to Y	C_L = 50 pF R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns

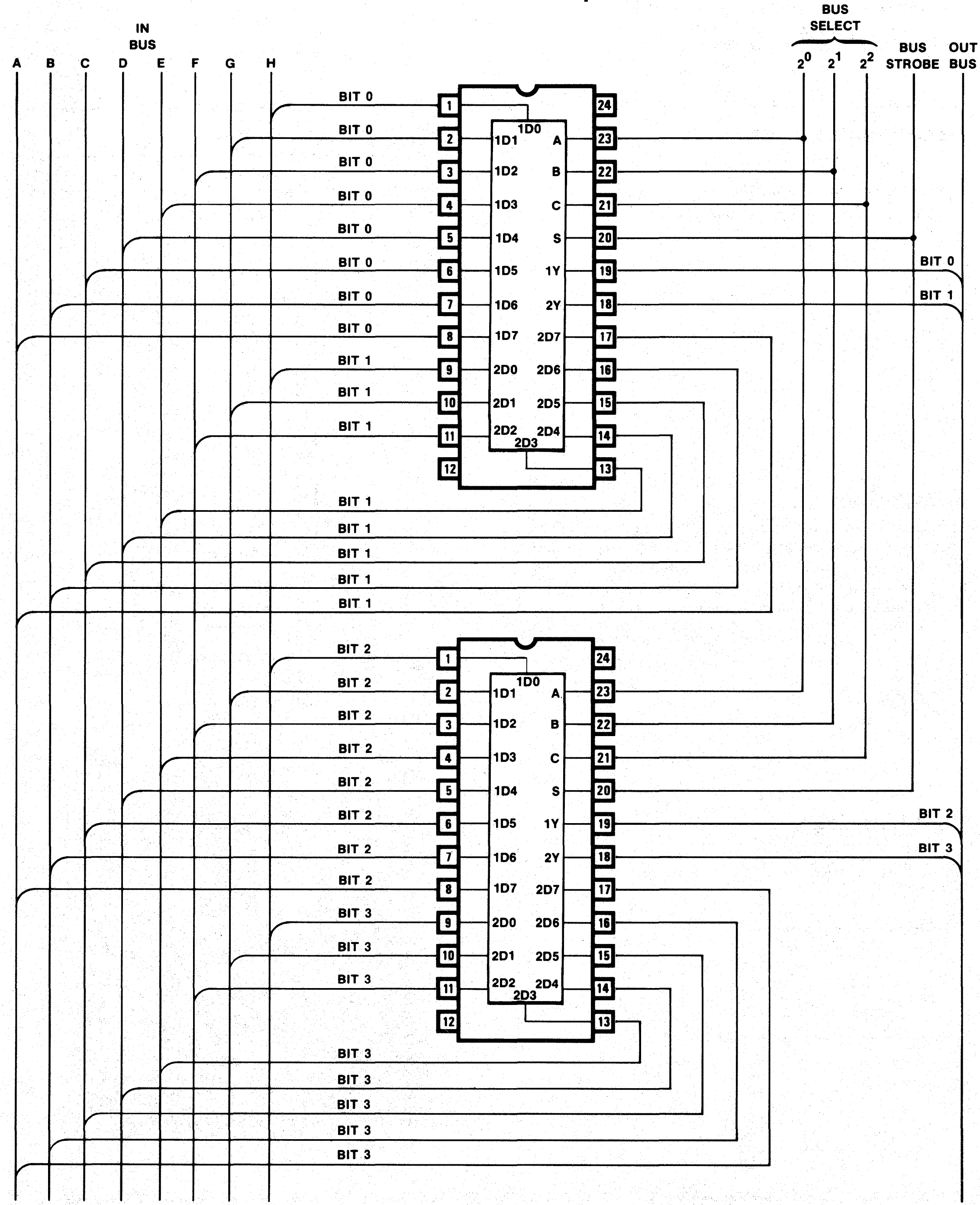
Test Load



* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Application

4-Bit Wide 8:1 Bus Multiplexer



6

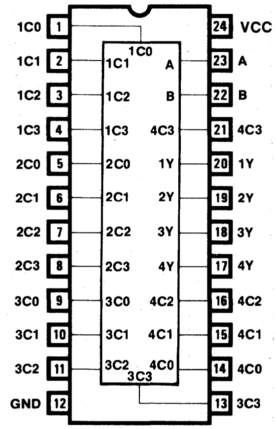
Quad 4:1 Mux
SN54/74LS453

Features/Benefits
- 24-pin SKINNYDIP® saves space
- Twice the density of 74LS153
- Low-current PNP inputs reduce loading

Ordering Information

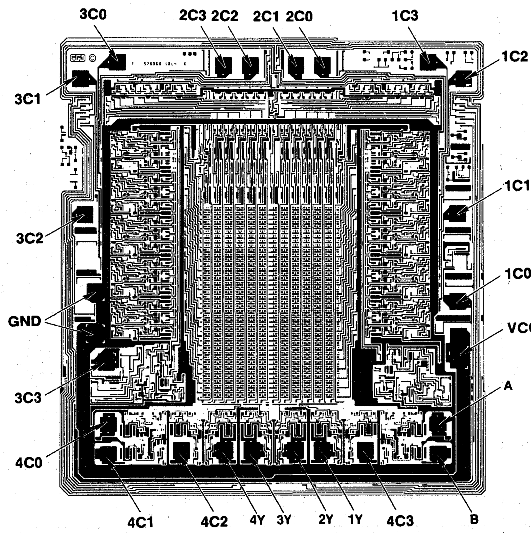
PART NUMBER	PACKAGE		TEMPERATURE
SN54LS453	JS, F	28L	MIL
SN74LS453	NS, JS		COM

Logic Symbol



Description
The Quad 4:1 Mux selects one of four inputs, C0 through C3, specified by two binary select inputs, A and B. The true data is output on Y. Propagation delays are the same for inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem-pole drive standard.

Die Configuration
Die Size: 140x131 mil^2

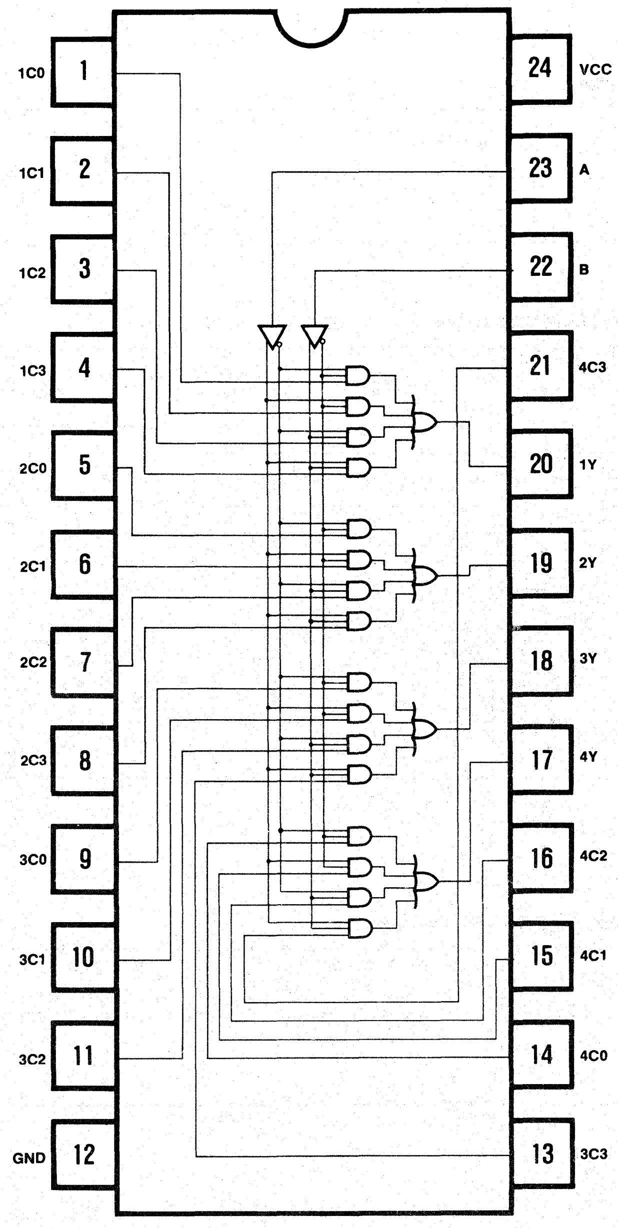


Function Table

INPUT SELECT		OUTPUTS Y
B	A	
L	L	C0
L	H	C1
H	L	C2
H	H	C3

Logic Diagram

Quad 4:1 Mux



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125*	0		75	°C

* Case temperature

Electrical Characteristics Over Operating Conditions

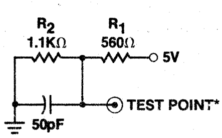
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = -18mA			-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V		I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = -2mA	2.4			V
			COM	I_{OH} = -3.2mA				
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	-30		-130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

* No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Any input to Y	C_L = 50 pF, R_1 = 560Ω, R_2 = 1.1kΩ		25	45		25	40	ns

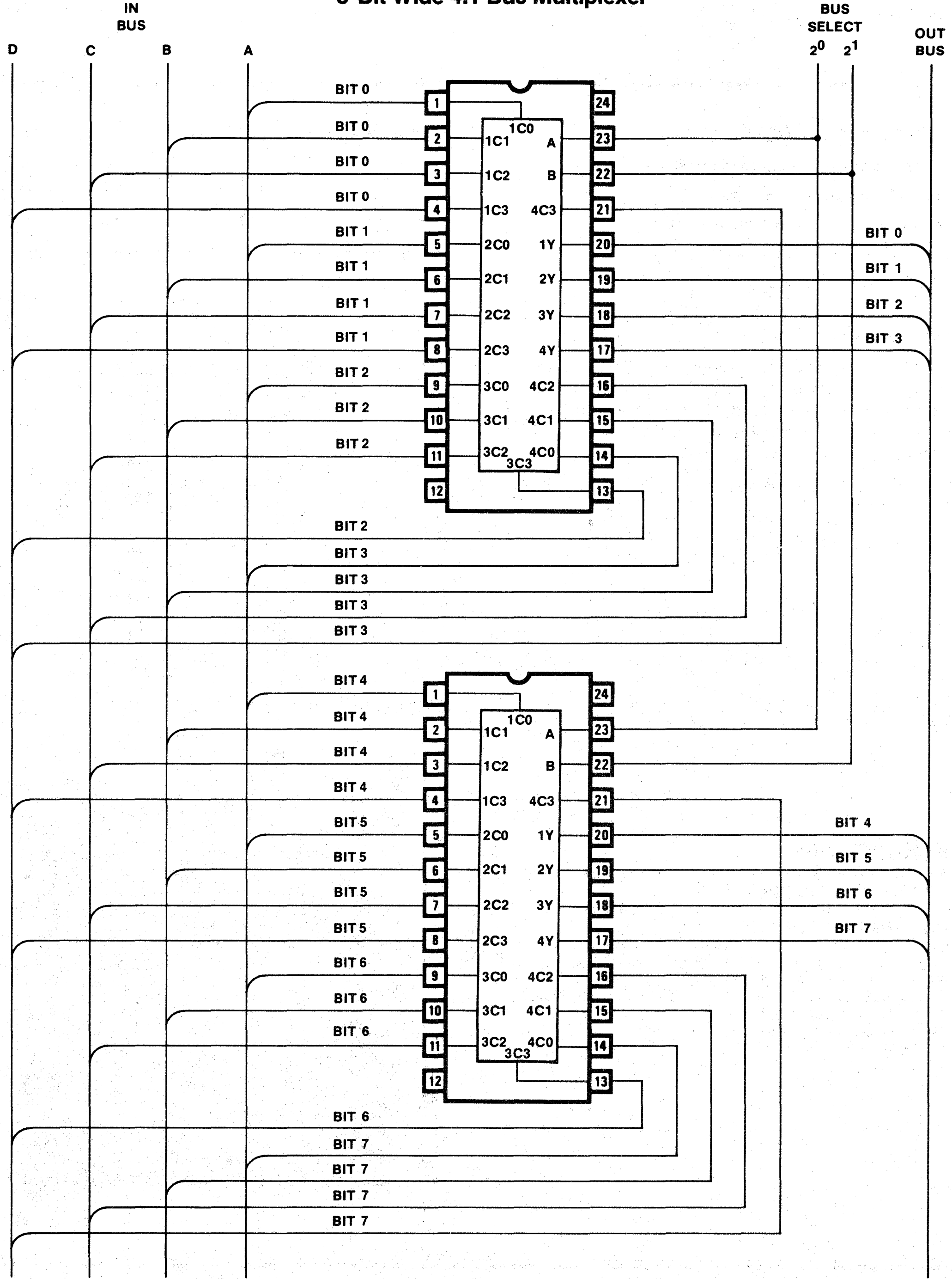
Test Load



* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Application

8-Bit Wide 4:1 Bus Multiplexer



6

10-Bit Comparator
SN54/74LS460

Features/Benefits

- True and complement comparison status outputs
- 24-pin SKINNYDIP® saves space
- Low-current PNP inputs reduce loading
- Expandable in 10-bit increments
- Useful for address decoding

Description

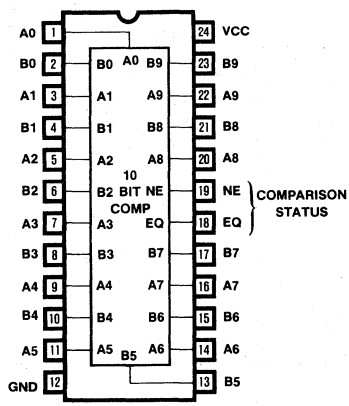
The 'LS460 is a 10-bit comparator with true and complement comparison status outputs. The device compares two 10-bit data strings (A9-A0 and B9-B0) to establish if this data is Equivalent (EQ = HIGH and NE = LOW) or Not Equivalent (EQ = LOW and NE = HIGH).

Outputs conform to the usual 8-mA LS totem-pole drive standard.

Ordering Information

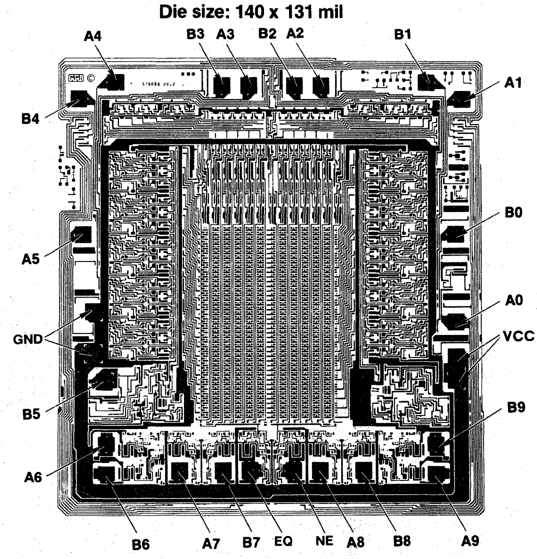
PART NUMBER	PACKAGE		TEMP
SN54LS460	JS, F	28L	MIL
SN74LS460	NS, JS		COM

Logic Symbol



Die Configuration

Die size: 140 x 131 mil



Function Table

INPUTS	OUTPUTS		OPERATION
(A9-A0)*,(B9-B0)*	EQ	NE	
(A9-A0) = (B9-B0)	1	0	Bit strings equivalent
(A9-A0) ≠ (B9-B0)	0	1	Bit strings not equivalent

* The parentheses (...) denote a 10-bit string from either Input A or B, as given by the symbols within the parentheses.

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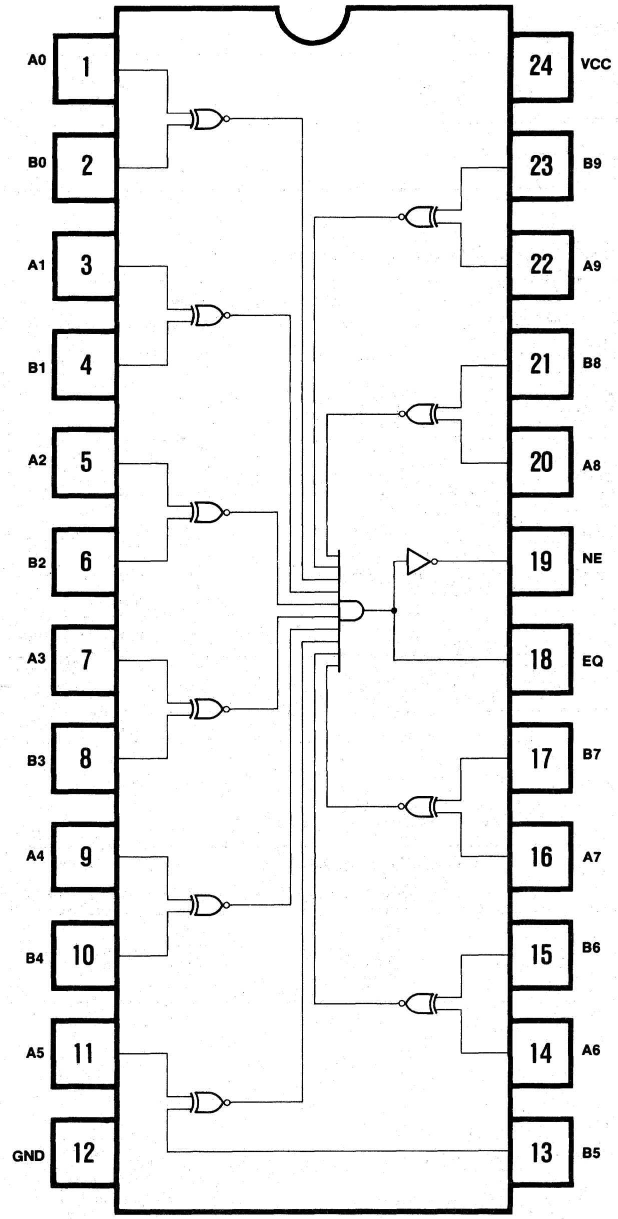
Monolithic Memories

Logic Diagram

10-Bit Comparator



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125*	0		75	°C

* Case temperature

Electrical Characteristics Over Operating Conditions

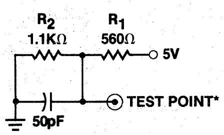
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = –2mA COM I_{OH} = –3.2mA	2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	–30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX			60	100	mA

* No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Any input to EQ or NE	C_L = 50 pF, R_1 = 560Ω, R_2 = 1.1kΩ		25	45		25	40	ns

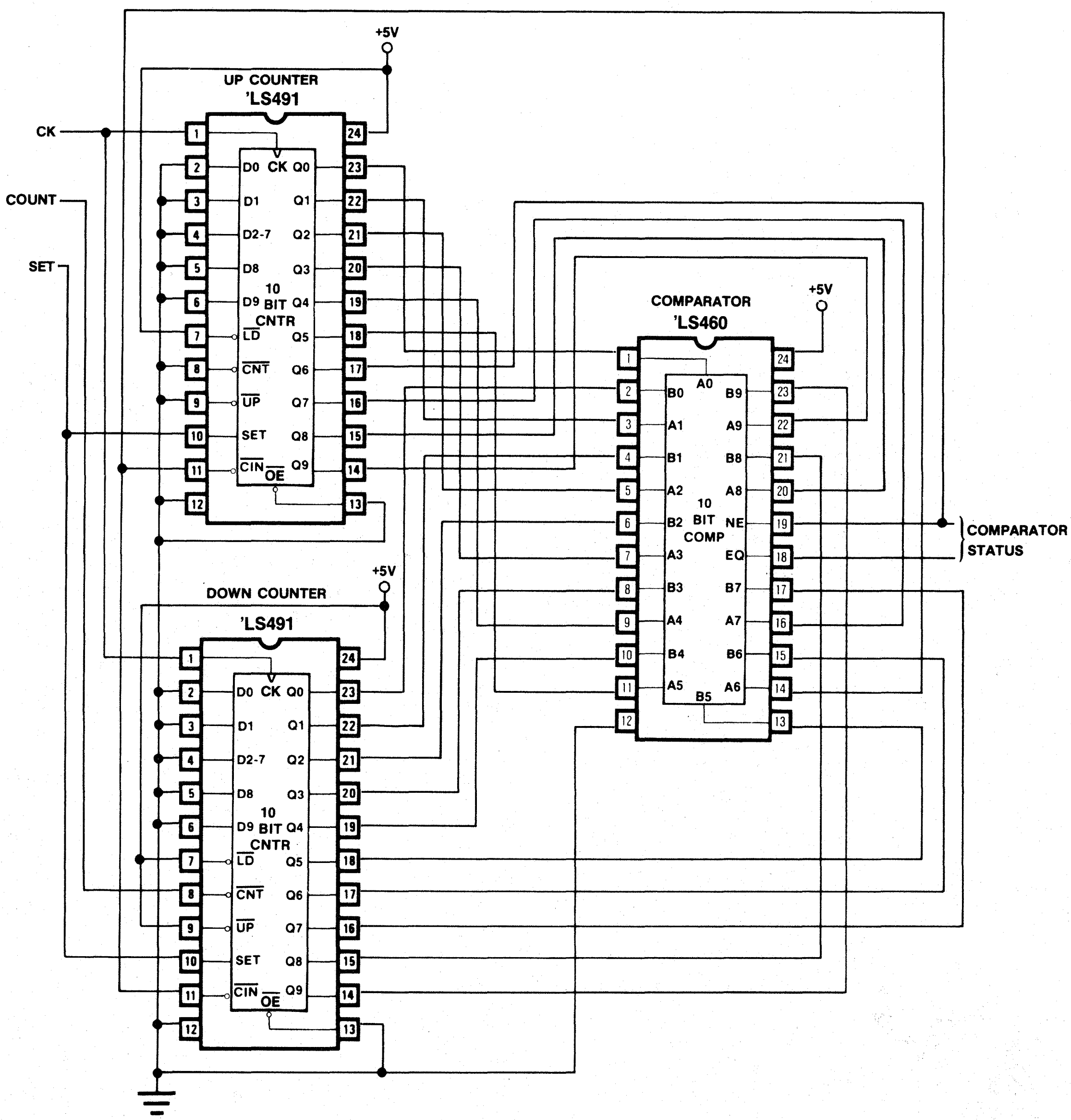
Test Load



* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Application

10-Bit Up Counter/Down Counter Comparator



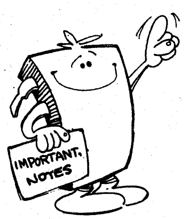

IMPORTANT
NOTES

Table of Contents

FIFO

First-In First-Out (FIFO) Selection Guide

ORGANIZATION/FEATURES	FREQUENCY	CASCADABLE	STANDALONE
Com 64x5 with flags Com 64x5 with flags	35 MHz 25 MHz		67413A 67413
Mil 64x5 with flags	25 MHz		57413A
Com 16x5 Com 16x5	20 MHz 10 MHz	74S225A 74S225	74S225A 74S225
Com 64x8/9 Serializing	28 MHz serial port 10 MHz parallel port	67417 on parallel port only	67417
Com 64x4 Com 64x5	16.7 MHz 16.7 MHz	C67401B C67402B	67401B 67402B
Com 64x4 Com 64x5	15 MHz 15 MHz	C67401A C67402A	67401A 67402A
Com 64x4 Com 64x5	10 MHz 10 MHz	C67401 C67402	67401 67402
Mil 64x4 Mil 64x5	10 MHz 10 MHz	C57401A C57402A	57401A 57402A
Mil 64x4 Mil 64x5	7 MHz 7 MHz	C57401 C57402	57401 57402
Com 64x4	5 MHz	67L401	67L401
Com 64x5	5 MHz	67L402	67L402

FIFOs: Rubber-Band Memories to Hold Your System Together

Chuck Hastings

Introduction

Data-rate matching problems are a very basic part of the life of a builder of digital systems. Some important electromechanical devices such as disk drives produce or absorb data at totally inflexible rates governed by media recording densities and by the speeds at which small electric motors are naturally willing to rotate. Other devices such as letter-quality printers have maximum data rates beyond which they cannot be hurried up, and which are relatively slow compared to the rates of other devices in the system.

Microprocessors and their associated main memories are generally faster and more flexible than other system components, but often operate with severly degraded efficiency if they must be diverted from their main tasks every few milliseconds to handle data-ready interrupts for individual dribs and drabs of data. While "one day at a time" may be a sound principle by which to live your life, "one bit at a time" or even "one byte at a time" is not a philosophy by which to make your microprocessor live if you want the best possible service from it.

Today there are components called "FIFOs" which let you keep your hardware design simple, and let each portion of your system see the data rate which it wants to see, and yet let you avoid hobbling the performance of your software by constantly interrupting your microprocessor, or even by intermittently halting it in order to let DMA (Direct Memory Access) circuits take over control of the main memory for a short time. FIFOs may be thought of as "elastic storage" devices — "logical rubber bands" between the different parts of your system, which stretch and go slack so that data rates between different subsystems do not need to match up on a short-term microsecond-by-microsecond basis, but only need to average out to be the same over a much longer period of time.

This tutorial paper both describes what FIFOs are in general, and introduces the 64x4 and 64x5 Monolithic Memories FIFOs in particular.

What is a FIFO?

FIFO is one of those made-up words, or *acronyms,* formed from the initials of a phrase — in this case, "*F*irst-*I*n, *F*irst-*O*ut." Originally, the phrase "First-In, First-Out" came from the field of operations research, where it describes a *queue discipline* which may be applied to the processing of the elements of any *queue* or waiting line. There is also a LIFO, or "Last-In, First-Out" queue discipline. The terms FIFO and LIFO have also been used for many years by accountants to describe formal procedures for allocating the costs of items withdrawn from an inventory, where these items have been bought over a period of time at varying prices.

You can probably think of some simple, everyday objects which in some manner behave according to the FIFO queue discipline. For instance, little two-seater cable-drawn boats are drawn through an amusement park tunnel of love one by one, and must emerge from the other end in the same order in which they entered the tunnel — "First-In, First-Out." The old-time coin dispensers used by the attendants at such amusement park features, or by city bus drivers, are "buffer storage" devices for coins which handle the coins in this same manner. (See Figure 1.)

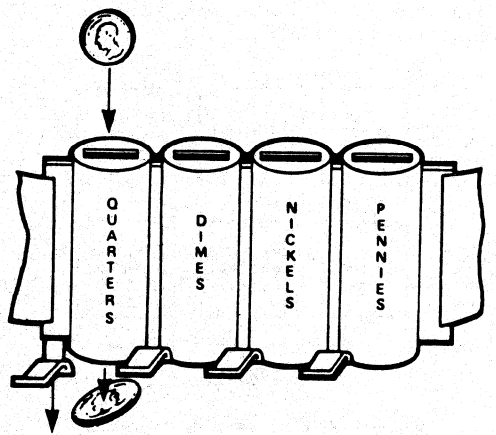


Figure 1. Primitive Mechanical FIFO Device

Notice also that the input of a coin into one of the tubes of such a coin dispenser through the slot at the top, and the output of a coin at the bottom of that tube when the lever for that tube is pushed, are completely independent events which do not have to be synchronized in any way, as long as the tube is neither totally empty nor totally full. However, if the tube fills up completely, a coin inserted into the slot will not go into the tube. Likewise, if the tube empties out completely, no coin is released from the tube at the bottom when the lever is pressed. The coin tube thus behaves as an *asynchronous* FIFO. Keep this homely example in mind.

In computer technology, both the FIFO queue discipline and the LIFO queue discipline are frequently used to control the insertion and withdrawal of information from a buffer memory, or from a dedicated buffer region of some larger memory. In input/output programming practice, a FIFO memory region is sometimes referred to as a *circular buffer,* and in programming for computer-controlled telephone systems it is called a *hopper.* A LIFO memory region is usually referred to as a *stack.*

Both FIFO and LIFO memories have frequently been implemented as special-purpose digital systems or subsystems, but as of the present time only FIFO memories are commonly implemented as individual, self-contained semiconductor devices.

Representative FIFOs

To give you the flavor of what these semiconductor devices are like, I'll describe the type 67401 64x4 FIFO and type 67402 64x5 FIFO which have been available for several years from Monolithic Memories. ("64x4" here means containing 64 words of 4 bits each.) These parts have a basic, easy-to-understand architecture and control philosophy. They also happen to be the fastest FIFOs available through normal commercial channels as of this writing, and they are in widespread use for applications ranging from microcomputers up to IBM-lookalike mainframes and large special-purpose military radar processors. A 67401 is internally organized as follows:

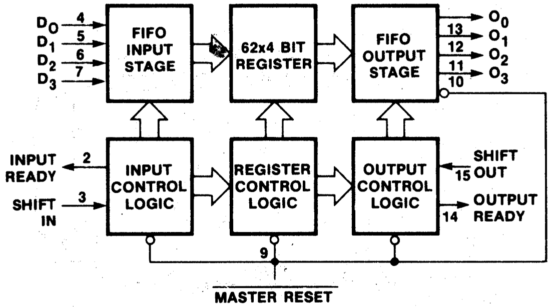


Figure 2. Architecture of the 67401 FIFO

The list of signals/pins for the 67401 is:

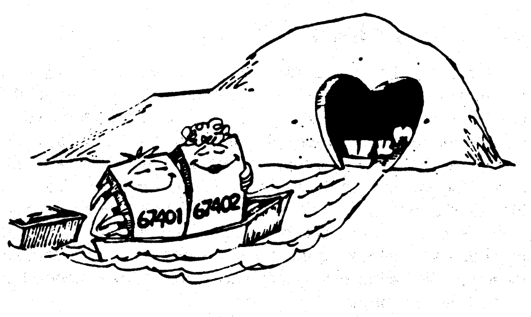
TYPE	HOW MANY	(CUM.)	I/O/V
Data In	4	4	I
Output	4	8	O
Control:			
Shift In	1	9	I
Shift Out	1	10	I
Master Reset	1	11	I
Status:			
Input Ready	1	12	O
Output Ready	1	13	O
Not Connected	1	14	—
Voltage:			
V_{CC} (+5V)	1	15	V
Ground	1	16	V

The corresponding list for the 67402 differs only in that there are five Data in lines rather than four, and five Output lines rather than four. The reason that there is an unused pin is that the 67401 was originally designed as a faster bipolar upgrade of a MOS part, the Fairchild 3341, which needs a second power-supply voltage (−12 V) as well as V_{CC}. Much of the description to be given here of the 67401 also applies to the 3341, except for data rate — the 67401 can operate at 5-35 MHz depending on the exact version, compared with approximately 1 MHz for the 3341. Pinouts are indicated in the data sheet.

The reason for having a 5-bit model as well as a 4-bit model of basically the same part is that if two 4-bit FIFOs are placed side-by-side they make only an 8-bit FIFO, and many people have FIFO applications which entail using a parity bit with each byte, and/or a frame-marker bit with the last byte of a frame or block, which means that they want 9-bit or 10-bit FIFOs. A 67402 next to a 67401 makes a 9-bit FIFO, and two 67402s make a 10-bit FIFO. But I'm getting ahead of myself.

A logic HIGH signal on the Input Ready line indicates that there is at least one vacant memory location within the FIFO into which a new data word may be inserted.Likewise, a logic HIGH on the Output Ready line indicates that there is at least one data word currently stored within the FIFO and available for reading at the outputs. The operation of the FIFO is such that, once a data word has been inserted at the Data In lines (the *top* of the FIFO, as it were), this word automatically *sinks all the way to the bottom* (assuming that the FIFO was previously empty) and forthwith appears at the Output lines. (Remember the synonym *hopper?*) in keeping with the FIFO queue discipline, the first word which was inserted is the first one available at the outputs, and additional words may be withdrawn *only* in the order in which they were originally inserted.

There is no provision for *random access* in these FIFOs, since their internal implementation uses one particular variation of shift-register technology. Each FIFO word consists of 4 (for the 67401) or 5 (for the 67402) data bits, plus a control or "presence" bit which indicates whether or not the word contains significant information. There are thus 4 or 5 data "tracks" and one presence "track" if you look at a FIFO *from a magnetic-tape* perspective. What the Master Reset input does is to clear all of the bits in the presence track, and in addition to clear the very last data word (at the "bottom") which controls the Output lines. The other 63 data words are not cleared, but it doesn't really matter; their status is like unto that of operating-system files whose Directory entries have been deleted, in that they can no longer be read out and will get written over as soon as new information comes in.



"'FIRST-IN, FIRST-OUT' ... DESCRIBES A QUEUE DISCIPLINE WHICH MAY BE APPLIED TO THE PROCESSING OF THE ELEMENTS OF ANY QUEUE ..."

We now return to what happens when a new data word gets inserted at the "top" of the FIFO. A mark (call it a "one") is made in the presence bit for word 00, the first word. Assume now that word 01 is vacant, so that there is a "zero" in its presence bit. The internal logic of the FIFO then operates so that the data from word 00 is automatically written into word 01, the presence bit for word 01 is automatically set to "one," and the presence bit for word 00 is automatically reset to "zero." If word 02 is likewise vacant, the process gets repeated, and so forth until the same piece of data has settled into the lowest vacant word in the FIFO — the next lower word, and all the rest, have "ones" in their presence bits, blocking further changes.

Conversely, now assume that at the moment no data word is being input, but that one has just been output. Then the bottom word in the FIFO — word 63 — has a "zero" in its presence bit, but there are a number of other words above it which have "ones" in their presence bits. The data in word 62 then moves into word 63 in the same manner described above, and the data in word 61 moves into word 62, and so forth, until there is no longer any word in the FIFO having a "one" in its presence bit which is above a word having a "zero" in its presence bit. The effect is that of empty locations bubbling up to the top of the FIFO. Or, in case you are one of those elite individuals who has been exposed to the concepts and jargon of modern semiconductor theory, you may prefer to think of the FIFO operation as one in which data ("electrons") flow from the top of the FIFO to the bottom, and vacancies ("holes") flow from the bottom of the FIFO to the top. In the general case, of course, new data words are being input at the top and old ones are being output at the bottom at random times, and there is a dynamic and continually changing situation within the FIFO as the new data words drop towards the bottom and the vacancies bubble up towards the top, and they intermix along the way.

An obvious consequences of this manner of operation in shift-register-technology FIFOs is that it takes quite a bit longer for a data word to pass all the way through the FIFO than the minimum time between successive input or output operations. There are various versions of the 67401 and 67402, rated at 5, 7, 10, 15, 16.7 or 35 MHz over commercial (0°C to +75°C) or military (-55°C to +125°C) temperature ranges. Thus, for instance, a 16.7-MHz FIFO can input data words at the top and/or output data words at the bottom at a sustained rate of a word every 60 nanoseconds. However, the "fall-through" time, t_{PT} for these same FIFOs is stated in the data sheet as 1.3 microseconds, which is a long enough time for 24 words to be input or 24 words to be output! There is in principle also a "bubble-through" time for a single vacancy to travel from word 63 all the way back to word 00, which should be identical to t_{PT}, and probably is although as *measured* on a semiconductor tester it may differ by as much as 50 nanoseconds, which is probably due to artifacts of measurement. By the way, the stated operating frequencies and the t_{PT} value are "worst-case" (guaranteed) numbers; the "typical" values observed in actual parts are necessarily somewhat better, since semiconductor manufacturers are obliged to take any parts back which customers can prove do not meet the worst-case numbers, and some margin of safety is always nice.

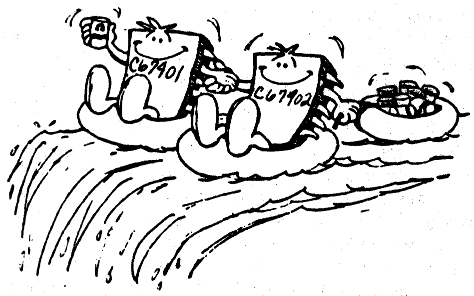
Besides Monolithic Memories, other manufacturers of high-speed FIFOs include Fairchild Semiconductor, Mostek, National Semiconductor, RCA, Texas Instruments, and TRW LSI Products. MOS (slow) FIFOs are available from Advanced Micro Devices, Fairchild Semiconductor, Texas Instruments, Western Digital, Zilog, and probably other firms. FIFOs in development or available at just about all of these vendors also offer new bells and whistles which I haven't discussed, such as three-state outputs, serial (one-bit-at-a-time) as well as parallel data ports, and additional status flags. For instance, Monolithic Memories now has the 67413 FIFO which has a "half-full" flag which tells when half of the FIFO's words contain data, and also a second flag which indicates that the FIFO is either "almost full" (within 8 words of full) or "almost empty" (within 8 words of empty), reminiscent of the "yellow warning interrupt" in Digital Equipment Corporation PDP-11 computers. This "almost-full/empty flag" can be used as an interrupt to a microprocessor to indicate that *some* action must be taken, and the microprocessor can then examine the "half-full flag" to see what it actually has to do.

There are also other design approaches to the insides of a FIFO besides the one based on shift-register technology which has been described here. For instance, a FIFO may be organized as a random-access memory ("RAM") with two counters capable of addressing the RAM right within the chip, an "in-pointer" and an "out-pointer." The counting sequences, of course, "wrap around" from the highest RAM address back to zero. The out-pointer chases the in-pointer, the region just traversed by the in-pointer but not yet by the out-pointer contains significant data, and the complementary region is logically "empty." This approach involves good news and bad news: the good news is that the long fall-through time goes away, but the bad news is that now reading and writing typically interfere with each other — unless the RAM is "two-port," they cannot be done simultaneously at all. Also, since this approach is more costly in "silicon area" than the shift-register approach, it would not result in as large FIFO capacities for the same size die or the same power consumption. In practice, this approach has only been used for MOS FIFOs which have turned out to be quite slow.

Another design approach is somewhat intermediate between the pure RAM approach as just described and the shift-register approach. It uses "ring counters" on the chip instead of full-blown binary counters. What this means in practice is that there are now *two* extra "tracks" along with the data tracks within the FIFO, plus also an input data bus and an output data bus. Single "one" bits move along the in-pointer track and the out-pointer track, and the out-pointer chases the in-pointer as before. The RAM is effectively two-port, and the two parallel buses both go to each and every word. Texas Instruments has announced some small (16x4) bipolar FIFOs based on this technical approach. Like the pure RAM approach, it gets rid of the fall-through time but needs proportionally more silicon area to store a given number of bits.

Designing with FIFOs

Returning now to the Monolithic Memories 67401 and 67402, if what you *really* need is a "deeper" FIFO, say 128x4 instead of just 64x4, these parts are designed to *cascade* using a simple "handshaking" procedure, without any external logic at all! If FIFO B follows FIFO A in the cascading sequence, the Shift In control input of FIFO B is connected to the Output Ready status output of FIFO A, and likewise the Shift Out control input of FIFO A is connected to the Input Ready status output of FIFO B, and the Master Reset control inputs are all tied together. (See Figure 3.) That's all there is to it. Any number of FIFOs may be cascaded in this manner.



"...THE MONOLITHIC MEMORIES C67401 AND C67402...ARE DESIGNED TO CASCADE USING A SIMPLE 'HANDSHAKING' PROCEDURE..."

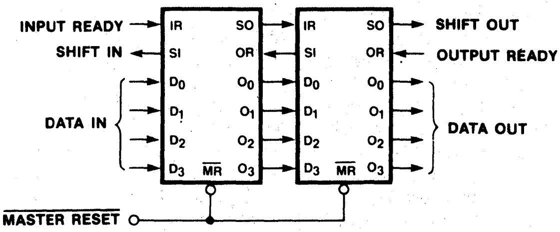


Figure 3. Cascading FIFOs to Form 128x4 FIFO

If what you *really* need is a "wider" FIFO, then you simply arrange 64x4 or 64x5 FIFOs side-by-side up to the required width. Then, you use an external AND gate such as a 74S08 or 74S11 to AND the Input Ready signals of the first rank of FIFOs if there is more than one rank, or of the only rank of FIFOs if there isn't. (See Figure 12 in the FIFO data sheet.) Likewise, a similar AND gate is also needed to AND the Output Ready signals of the last rank of FIFOs. If you didn't provide these AND gates and just took the Input Ready signal of one FIFO as representative of when the whole array was ready, you would be taking the rather large gamble that you had correctly chosen the slowest row in this array — and if you chose wrongly, 4-bit or 5-bit chunks of your input word might not get read correctly into the FIFO where they were supposed to go. Ditto on the output side. So like use the AND gates.

Although a humungus number of 67401s and 67402s are in use world-wide giving hassle-free service, it should be kept in mind that these devices are *asynchronous sequential circuits.* (One definition of "asynchronous sequential circuit" is "a fortuitous collection of race conditions," but that definition is unduly sardonic for very carefully designed parts such as these.) If your board is subject to noise, or if certain data sheet setup-time and hold-time conditions are occasionally not met, errors may occur. It is prudent system-design practice to every so often allow an array of FIFOs to empty out completely, and then issue a Master Reset. (I'm assuming, of course, to start with that you're not the kind of turkey who has to be *told* to issue a Master Reset as part of your power-up sequence.) In the event that you still get what appear to be occasional errors, very small (say from 22 to 68 picofarads) capacitors from both the Shift In control input and the Shift Out input of a FIFO to ground will often eliminate these. But by all means start with a *good* circuit board — these are high-speed-Schottky-technology circuits, and like to see a lot of ground-plane metal on the board, along with other reputable interconnection practices such as 0.1-microfarad disk capacitors between V_{CC} and ground for each chip to bypass switching noise.

The sequence of events which occurs during the operation of shifting a new data word into the "top" of a FIFO is shown in Figure 3 in the FIFO data sheet, and the corresponding sequence of events for shifting out the bottom word is shown in Figure 7 in the FIFO data sheet. In both of these figures, it has been assumed that the external logic — whether it be the rest of your system, or just another FIFO — refrains from raising the respective Shift line to HIGH until the respective Ready line has gone HIGH. If the Shift line is raised any earlier, it simply gets ignored.

When two FIFOs are cascaded as shown in Figure 3, the sequences of events shown in data-sheet Figures 3 and 7 are subject to the additional ground rule that the Output Ready line of the FIFO on the left in Figure 3 (call it "FIFO A") is identically the Shift In line of the FIFO on the right (call it "FIFO B"). And likewise, the Input Ready line of FIFO B is identically the Shift Out line of FIFO A. In the terminology we have been using. FIFO A is the "upper" FIFO and FIFO B is the "lower" FIFO. Although you do not normally need to be concerned about what happens when two FIFOs are hooked together for cascaded operation in this manner, since the "handshake" occurs quite automatically without the rest of your logic having to do anything to make it happen, it is an illuminating exercise to consider data-sheet Figures 3 and 7 together in this light and see why the cascading works.

In the general case, both FIFO A and FIFO B are neither completely full nor completely empty. Thus, from the description already given of FIFO internal operation, after some period of time there will be a significant piece of data in word 63 or FIFO A and a "one" in the presence bit for that word. Since the word-63 presence bit is what controls the Output Ready signal, the latter will at some point in time go HIGH and at that same point in time the data word in FIFO A word 63 is present at the output lines. Likewise, after some period of time there will be a vacancy in word 00 of FIFO B, and a "zero" in the presence bit for that word which in turn results in the Input Ready signal going HIGH. Remembering now that each of these Ready signals is in fact the respectively-opposite Shift signal for the other FIFO, it may be seen from data-sheet Figure 3 that the conditions for inputting a word into FIFO B have now been met, and from data-sheet Figure 7 that the conditions for outputting a word from FIFO A and allowing the next available piece of data from somewhere further "up" in FIFO A to enter FIFO A word 63 have also been met. The time delays shown in both data-sheet Figure 3 and data-sheet Figure 7 from the event at 2 to the event at 3, and from the event at 4 to the event at 5A, are asynchronous internal-logic-determined times of the order of four or five gate delays, where the gates in question are high-speed-Schottky LSI *internal* gates and have significantly less propagation delay than the SSI gates you can read about in data sheets.

Returning now to applying the timing analysis shown in data-sheet Figures 3 and 7 to the case of FIFO A and FIFO B operating in cascaded mode, notice that each movement (rising or falling) of the Ready signal for one FIFO is activated by the movement in the opposite sense (falling or rising, that is) for the Ready signal from the other part. The two signals, ORA/SIB (meaning "Output Ready A" which is the same signal as "Shift In B") and IRB/SOA, cannot both remain HIGH at the same time for more than a few nanoseconds, since if they are both HIGH a data word will pass between the two FIFOs as already described. So, at the point when *both* the sequence of events shown in data-sheet Figure 3 and the sequence of events shown in data-sheet Figure 7 have been completed, and consequently ORA/SIB and IRB/SOA have both gone HIGH again, another similar sequence of events occurs for both FIFOs and another word is passed, and so forth. This process continues apace until either ORA/SIB sticks LOW, which can happen if FIFO A gets completely emptied out of data words and has "zeroes" everywhere in its presence track; or until IRB/SOA sticks LOW, which can likewise happen if FIFO B gets completely filled and has "ones" everywhere in its presence track. When such a deadlock situation occurs, it lasts until a new data word has been input into FIFO A and has had time to "fall all the way through" and settle into FIFO A word 63, or until the data word in word 63 of FIFO B has been read out and the resulting vacancy has had time to "bubble all the way back up" into FIFO B word 00, as the case may be.

Various Uses for FIFOs

The classical FIFO application, as already mentioned at the beginning of this paper, is that of matching the instantaneous data rates of two digital systems in a simple, economical way. One of the two systems may, for reasons of design economics or even of utter necessity, want to emit or absorb data words in ultra-high-speed bursts, whereas the other one may prefer to operate at a slow-but-steady data rate or even at an erratic rate which varies between ultra-slow and slow or even between slow and fast. No matter — it's all the same to an asynchronous FIFO such as the 67401 or 67402, as long as the input rate and the output rate do match up over a long period of time so that it neither fills up nor empties out.

There are, however, some additional uses for FIFOs which arise from other, rather different circumstances. For instance, your digital system may simply need some extra buffer storage scattered around locally at different points on your block diagram, and you and your system may really just not care whether this storage is accessed on a random or on a queue basis. Under these circumstances, it is ordinarily less hassle to use a FIFO than to use a small RAM and come up with some extra logic to generate addresses and timing signals for it. Often the FIFO modus operandi is in fact the natural one for the application; as for instance when your system must accumulate a block of 64 characters and then run them by all at once in order to examine them for the presence of some control character, using some scanning logic — or perhaps even a microprocessor — which is otherwise occupied most of the time.

A less obvious but interesting application of FIFOs is as automatic "bus-watchers" for jump-history recording for hardware or even software diagnostic purposes. A FIFO whose inputs are connected to a minicomputer's program counter or microprogram counter, or to a microcomputer's main address bus, may be operated so as to record every new jump address generated by the program. This way, if at some point the hardware freaks out or the operating system crashes, a record exists of the last 64 jumps which were taken before the system was halted, assuming of course that you have provided some way for the system to sense that all is not well and halt itself. Such a record of jumps can be very valuable in tracing out what happened just before everything went haywire. FIFOs may be used in this way either as part of built-in self-monitoring features in digital systems, or as part of various kinds of external test equipment.

FIFOs may also be used as controllable delay elements for digital information which cannot be used immediately upon receipt — perhaps it must be matched against other information which is not yet available, or perhaps it must be synchronized with other streams of information which are out of phase by a varying amount. An example of the latter situation is deskewing several bit-streams off a parallel-format magnetic tape, which commonly has to be done when high recording densities are used. One FIFO *per bit-stream* is required — but the net resulting logic may still be the most reliable and economical way to get the job done, when compared with other possible digital designs. Another example is that of using FIFOs as data memories in digital correlators; the lag in an autocorrelation operation can be set simply by controlling how many words are in the FIFO at one time, and so forth. There are even some applications in which it is advantageous to operate a FIFO with all of its input and output cycles synchronized, so that absolutely all it does is to delay the data by some certain number of clock intervals.

References (1), (2), and (3) are formal applications notes available from Monolithic Memories, which discuss FIFOs from different viewpoints than this paper has taken. Each of them presents a more detailed explanation of one or more applications than there has been room for here. Reference (1) is mainly an overall applications survey, reference (2) emphasizes digital communications, and reference (3) emphasizes digital spectrum analyzers and also includes an overview of digital signal processing in general.

"A LESS OBVIOUS BUT INTERESTING APPLICATION OF FIFOS IS AS AUTOMATIC 'BUS-WATCHERS' . . ."

References

(1) "First In First Out Memories...Operations and Applications," applications note published March 1978 by Monolithic Memories Inc. and being reissued.

(2) "Understanding FIFO's," applications note published by Monolithic Memories Inc. The author, Alan Weissberger, has also gotten a modified version of this note published as a magazine article, "FIFOs Eliminate the Delay when Data Rates Differ," in *Electronic Design*, November 27, 1981. Despite the general title, the emphasis is on digital communications applications.

(3) "PROMs, PALs, FIFOs and Multipliers Team Up to Implement Single-Board High-Performance Audio Spectrum Analyzer," applications note published by Monolithic Memories Inc. The author, Richard Wm. Blasco, also got this note published in *Electronic Design* in two installments, in the issues of August 20 and September 3, 1981 under the titles "PAL Shrinks Audio Spectrum Analyzer" and "PAL Improves Spectrum Analyzer Performance" respectively.

Asynchronous First-In First-Out Memory (FIFO) 16x5
74S225/A

Features/Benefits

- DC to 20-MHz shift-in/shift-out rates
- Fully expandable by word width and depth
- Three-state outputs
- TTL-compatible inputs and outputs
- Functionally compatible with T.I. SN74S225
- Designed for extended testability

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
74S225	J, N	10 MHz Com
74S225A	J, N	20 MHz Com

Description

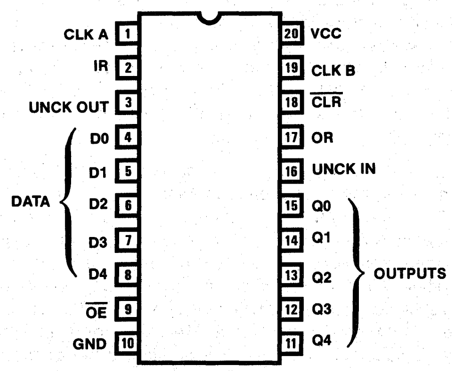
The 74S225/A is a Schottky-clamped transistor-transistor logic (STTL) 16x5 First-In-First-Out memory (FIFO) which operates from DC to 10/20 MHz. The data is loaded and emptied on a first-in-first-out basis through asynchronous input and output ports. These devices are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. Both word length and FIFO depth are expandable. Unload clock output (Pin 3) is designed for testability of V_{OL}.

Pin Names

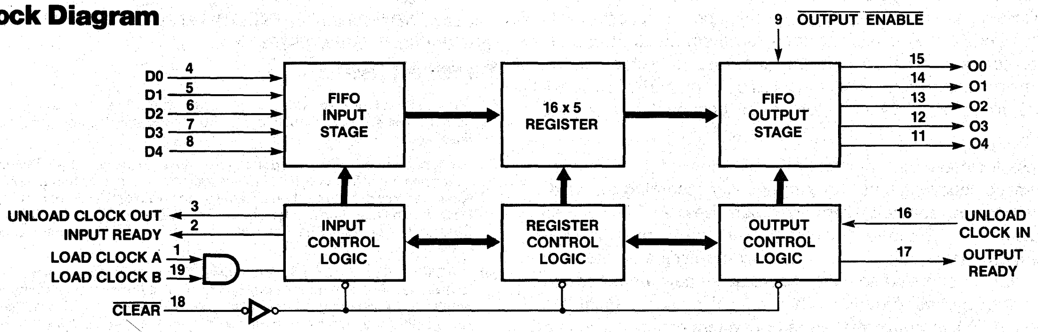
PIN #	PIN NAME	DESCRIPTION
1	CLK A	Load clock A
2	IR	Input ready
3	UNCK OUT	Unload clock output
4-8	D0-D4	Data inputs
9	$\overline{\text{OE}}$	Output enable
10	GND	Ground pin
11-15	Q4-Q0	Data outputs
16	UNCLK IN	Unload clock input
17	OR	Output ready
18	$\overline{\text{CLR}}$	Clear
19	CLK B	Load clock B
20	V_{CC}	Supply voltage

Pin Configuration

74S225/A . . J or N Package
(Top View)



Block Diagram



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Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC}	−0.5 V to 7 V
Input voltage	−1.5 V to 7 V
Off-state output voltage	−0.5 V to 5.5 V
Storage temperature	−65 to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225 MIN	74S225 TYP	74S225 MAX	74S225A MIN	74S225A TYP	74S225A MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	4.75		5.25	V
t_A	Operating free-air temperature		0		75	0		75	°C
t_{LCKH}	LOAD CLOCK pulse width, A or B, t_w (HIGH)	2	25			22		36	ns
t_{IDS}	Setup time, data to load clock	2	−20↑ *			−20↑ *			ns
t_{IDH}	Hold time, data from load clock	2	70↑			50↑			ns
t_{UCKL}	UNLOAD CLOCK INPUT pulse width, t_w (LOW)	4	7			7		36	ns
t_{CLW}	CLEAR pulse width, t_w (low)	2	40			20			ns
t_{CLCK}	Setup time, clear release to load clock, t_{su}	2	25↑			10			ns

* Data must be setup within 20 ns after valid Load Clock (A or B) pulse (positive transition).

↑ = Arrow indicates that it is referenced to the o-high transition.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		FIGURE	74S225 MIN	74S225 TYP	74S225 MAX	74S225A MIN	74S225A TYP	74S225A MAX	UNIT
f_{IN}	Load clock A or clock B	Cascade Mode** Standalone Mode	2	10	20		20	22		MHz
t_{LCIRL}	CLK A or CLK B to IR↓ **		2		55	75		43	55	ns
t_{LCCOL}	CLK A or CLK B to UNCK OUT↓		2		25	50		31	40	ns
f_{OUT}	Unload clock input	Cascade Mode*** Standalone Mode	4	10	20		20	22		MHz
t_{UCKORL}	UNCK IN ↑ to OR LOW		4		30	45		26	35	ns
t_{UCKORH}	UNCK IN ↑ to OR HIGH		4		40	60		32	45	ns
t_{ODH}	Output data hold, UNCK IN to output data		4		50	75	30	39		ns
t_{ODS}	Output data setup, UNCK IN to output data		4		50	75		41	55	ns
t_{RIP}	CLK A or CLK B to OR ↑		7		190	300		167	220	ns
t_{CLOL}	CLR to OR ↓		6		35	60		31	40	ns
t_{CLIH}	CLR to IR ↑		6		16	35		15	20	ns
t_{UCKOW}	Pulse width, UNCK OUT, t_w		2	7	14		7	11		ns
t_{ORD}	OR ↑ to output data		4		10	20		9	15	ns
t_{BUBI}	UNCK IN to IR ↑ (bubble-back time)		8		255	400		214	290	ns
t_{BUBC}	UNCK IN to UNCK OUT ↓ (bubble-back time)		8		270	400		226	290	ns

↓ Arrow indicates that it is referenced to the high-to-low transition.

** 16th word only

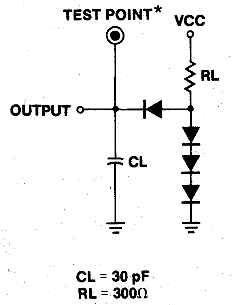
*** Devices connected to provide FIFO of greater than 16 word depth.

7

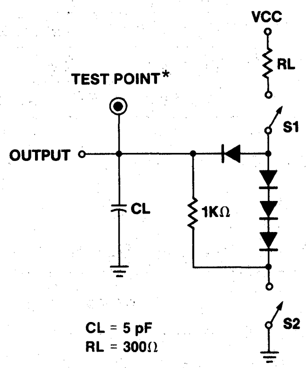
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225 MIN	74S225 TYP	74S225 MAX	74S225A MIN	74S225A TYP	74S225A MAX	UNIT
t_{PHZ}	Output disable delay, $\overline{OE}$ to Q_i, C_L = 5 pF	1		10	25		8	25	ns
t_{PLZ}							18	25	
t_{PZL}	Output enable delay, $\overline{OE}$ to Q_i, C_L = 5 pF	1		25	40		19	40	ns
t_{PZH}							23	40	

Test Load for Bi-State Output



Test Load for Three-State Output



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse Amplitude = 3.0 V
Input Rise and Fall Time (15%–90%) = 2.5 ns
Measurements made at 1.5 V

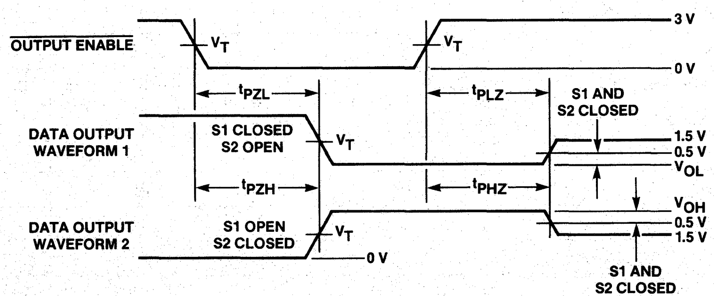


Figure 1. Enable and Disable

Waveform 1 is for an output with internal conditions such that the output is low except when disabled.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage							0.8	V
V_{IH}	High-level input voltage					2.0			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL1}	Low-level input current	D_0-D_4	V_{CC} = MAX	V_I = 0.5 V				−1	mA
I_{IL2}		All others						−.25	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V	Data inputs			40	μA
					Others			25	
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V				1	mA
V_{OL}	Low-level output voltage*		V_{CC} = MIN	I_{OL} = 16 mA (Data outputs)				0.5	V
				I_{OL} = 8 mA (All others)					
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −6.5 mA (Data outputs)		2.4			V
				I_{OH} = −3.2 mA (All others)					
I_{OS}	Output short-circuit current**		V_{CC} = MAX	V_O = 0 V		−30		−100	mA
I_{HZ}	Off-state output current		V_{CC} = MAX	V_O = 2.4 V				50	μA
I_{LZ}			V_{CC} = MAX	V_O = 0.5 V				−50	μA
I_{CC}	Supply current		V_{CC} = MAX	Inputs low, All outputs open	74S225		80	120	mA
					74S225A		80	125	

* To measure V_{OL} on Pin 3, force 10 V on Pin 9 (Extended Testability).

** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Functional Description

Data Input

After power up the CLEAR is pulsed low (Figure 5) to prepare the FIFO to accept data in the first location. Clear must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH, the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when both Load Clocks (CLK A and CLK B) are brought HIGH. The CLK A HIGH and CLK B HIGH signal causes the IR and UNCK OUT to pulse LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{RIP} defines the time required for the first data to travel from input to the output of a previously empty device. When the sixteenth word is clocked into the device, the memory is full (sixteen words) and IR remains low. The Unload Clock Output is provided chiefly for use in cascading devices to extend FIFO depth (Figure 9). When Input Ready is Low, do not attempt to shift-in new data.

Data Output

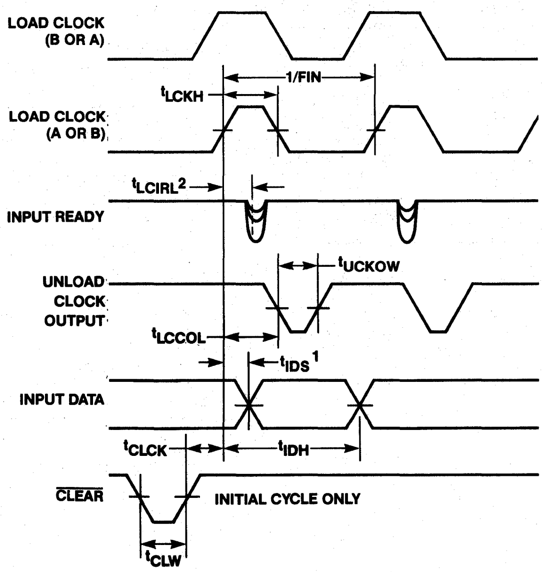
Data is read from the Q_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Unload Clock Input (UNCK IN) LOW. A LOW signal at UNCK IN causes the OR to go LOW. Valid data is maintained while the UNCK IN is LOW. When UNCK IN is brought HIGH the upstream data, provided that stage has valid data, is shifted to the output stage.

When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data remains valid for the last word.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{BUBI}) or completely empty (Output Ready stays LOW for at least t_{RIP}).

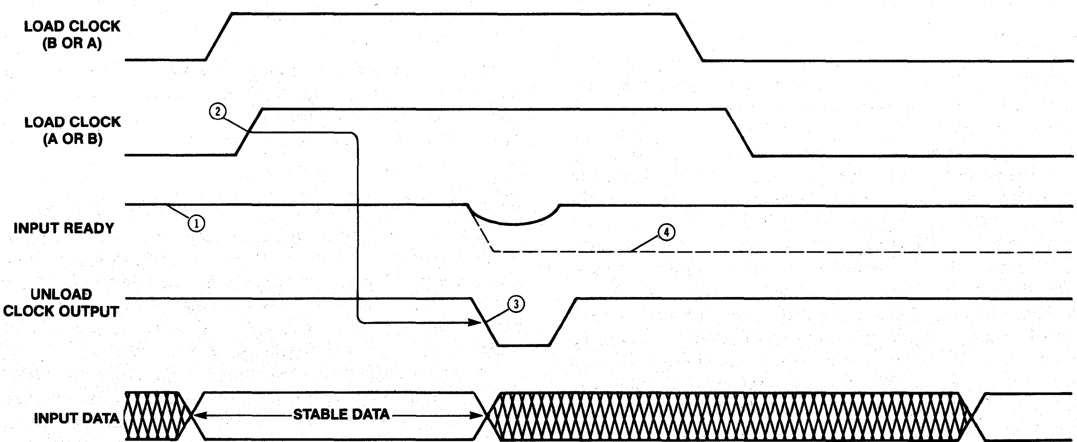
AC Test and High-Speed App. Notes

Since the FIFO is a high-speed device, care must be exercised in the design of the hardware and the timing utilized within the PC board design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Load Clocks (A, B) — Unload Clock Output-Input Ready combination, as well as the Unload Clock Input-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Load Clock pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or affected by ($\overline{CLR}$), the LOAD-CK activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (t_{IDH}) and the next activity of Input Ready (t_{LCIRL}) to be extended relative to Load Clock (A or B) going HIGH.



NOTES: 1. Permissible negative setup time for input data
2. Measure t_{LCIRL} for 16th input word only

Figure 2. Input Timing



NOTES: 1. Input Ready HIGH indicates space is available and a Load Clock (A and B) pulse may be applied.
2. Input Data is loaded into the first word.
3. Unload Clock Output pulses indicating the first word is full and the Data from the first word is released for "fall-through" to second word.
4. If the second word is already full, then the data remains at the first word. Since the FIFO is now full, Input Ready remains LOW.

Figure 3. The Mechanism of Clocking Data into the FIFO

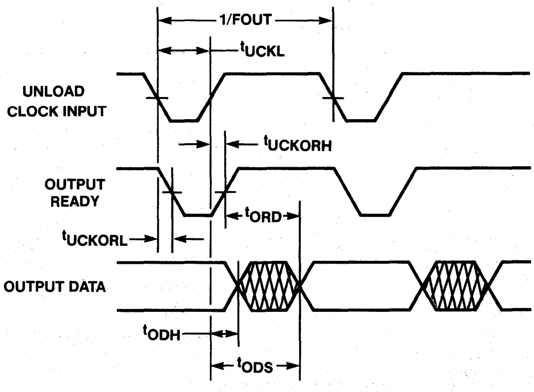
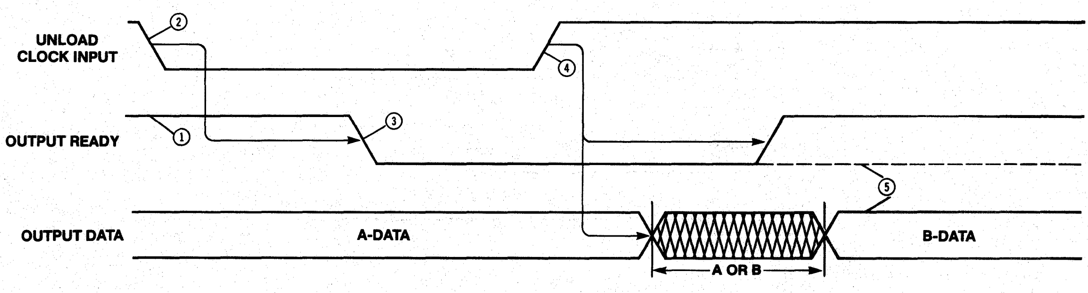


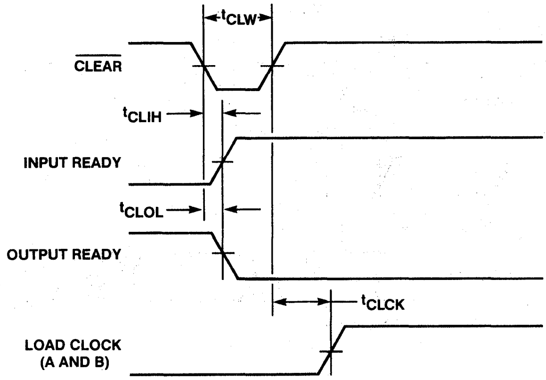
Figure 4. Output Timing



NOTES: 1. Output Ready HIGH indicates that data is available and an Unload Clock Input pulse may be applied.
2. Unload Clock Input goes LOW creating an empty position at word 16 for word 15 to "fall-through" to.
3. Output Ready goes LOW.
4. Unload Clock Input goes HIGH, causing Output Ready to go HIGH, indicating that new data (B) is now available at the FIFO outputs.
5. If the FIFO has only one word loaded (A-DATA), then Output Ready stays LOW and the A-DATA remains on the outputs.

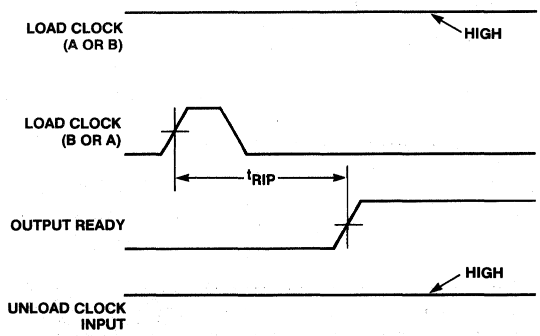
NOTE: Assume FIFO initially contains at least two words.

Figure 5. The Mechanism of Shifting Data Out of the FIFO



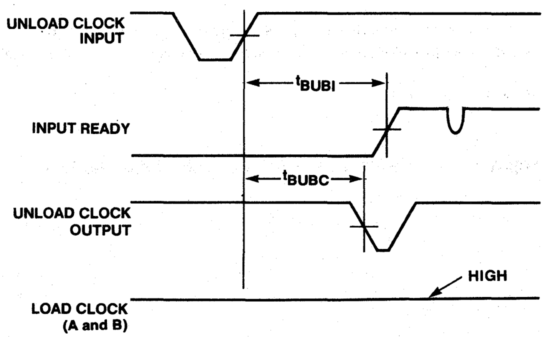
NOTE: Assume FIFO is full before $\overline{\text{CLEAR}}$ goes active.

Figure 6. Clear Timing



NOTES: 1. FIFO is initially empty.
2. Unload Clock Input and one Load Clock held HIGH throughout.

Figure 7. t_{RIP} Specifications



NOTES: 1. FIFO is initially full.
2. Load Clock (A and B) held HIGH throughout.

Figure 8. t_{BUBI}, t_{BUBC} Specifications

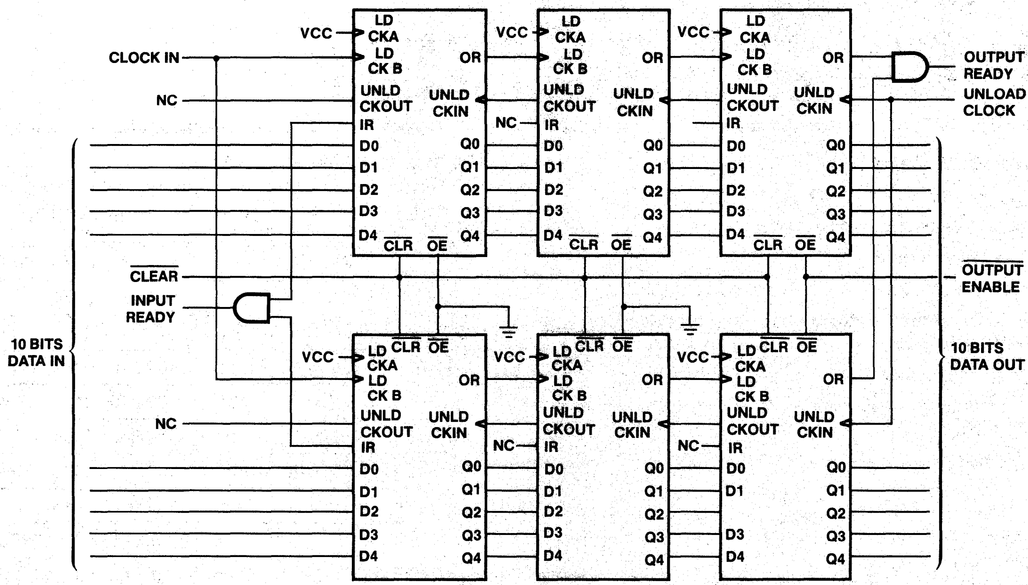
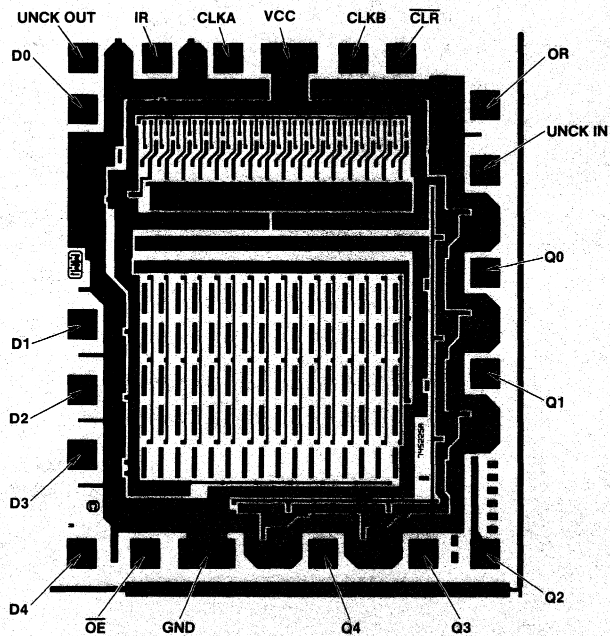


Figure 9. 48x10 FIFO with 54/74S225/A

7

Metal Mask Layout of the 74S225/A



Die Size: 78x93 mil^2

First-In First-Out (FIFO) 64x4 64x5 Cascadable Memory

C5/67401 C5/67401A C67401B
C5/67402 C5/67402A C67402B

Features/Benefits

- Choice of 16.7, 15 and 10 MHz shift-out/shift-in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in the word and bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times faster

Description

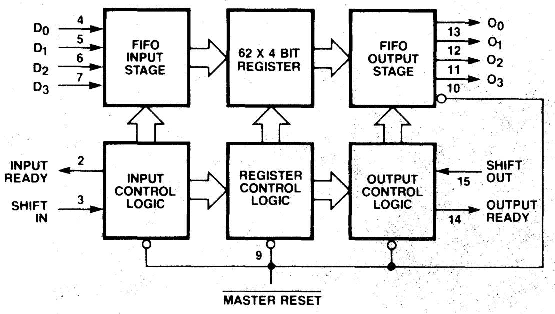
The C5/C67401B/2B/1A/2A/1/2 are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communications buffer applications. Both word length and FIFO depth are expandable.

Ordering Information

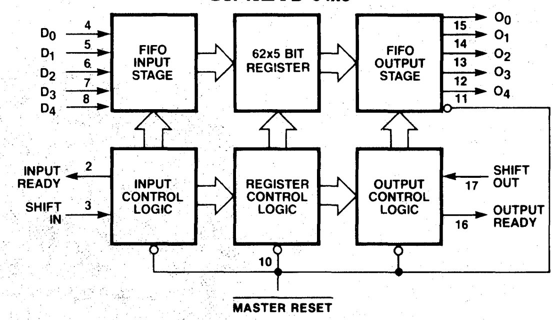
PART NUMBER	PKG	TEMP	DESCRIPTION
C57401	J,W(20)(L)	Mil	7 MHz 64x4 FIFO
C67401	J,N	Com	10 MHz 64x4 FIFO
C57402	J,W(20)(L)	Mil	7 MHz 64x5 FIFO
C67402	J,N	Com	10 MHz 64x5 FIFO
C57401A	J,W(20)(L)	Mil	10 MHz 64x4 FIFO
C67401A	J,N	Com	15 MHz 64x4 FIFO
C57402A	J,W(20)(L)	Mil	10 MHz 64x5 FIFO
C67402A	J,N	Com	15 MHz 64x5 FIFO
C67401B	J	Com	16.7 MHz 64x4 FIFO
C67402B	J	Com	16.7 MHz 64x5 FIFO

Block Diagrams

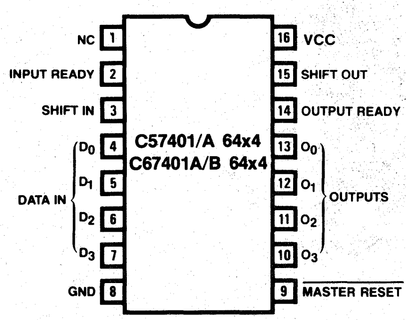
C57401/A 64x4
C67401A/B 64x4

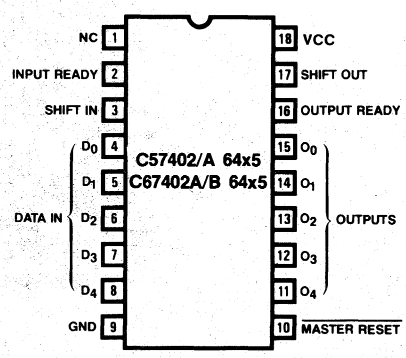


C57402/A 64x5
C67402A/B 64x5



Pin Configurations





Absolute Maximum Ratings

Supply voltage V_{CC} .... −0.5 V to 7 V
Input voltage .... −1.5 V to 7 V
Off-state output voltage .... −0.5 V to 5.5 V
Storage temperature .... −65° to +150° C

Operating Conditions C67401B/2B

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	18			ns
t_{SIL}	Shift in LOW time	1	18			ns
t_{IDS}	Input data setup	1	0			ns
t_{IDH}	Input data hold time	1	40			ns
t_{SOH}†	Shift Out HIGH time	5	18			ns
t_{SOL}	Shift Out LOW time	5	18			ns
t_{MRW}	Master Reset pulse	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

* Case temperature.

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Switching Characteristics C67401B/2B

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
f_{IN}	Shift in rate	1	16.7			MHz
t_{IRL}	Shift In to Input Ready LOW	1			35	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			37	ns
f_{OUT}	Shift Out rate	5	16.7			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			38	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			46	ns
t_{ODH}	Output Data Hold (previous word)	5	5			ns
t_{ODS}	Output Data Shift (next word)	5			44	ns
t_{PT}	Data throughput or "fall through"	4, 8			1.3	μs
t_{MRORL}	Master Reset to OR LOW	10			55	ns
t_{MRIRH}	Master Reset to IR HIGH	10			55	ns
t_{IPH}*	Input Ready pulse HIGH	4	20			ns
t_{OPH}*	Output Ready pulse HIGH	8	20			ns

†See AC test and High Speed application note.
*This parameter applies to FIFOs communicating with each other in a cascaded mode.

Absolute Maximum Ratings

Supply voltage V_{CC} .... -0.5 V to 7 V
Input voltage .... -1.5 V to 7 V
Off-state output voltage .... -0.5 V to 5.5 V
Storage temperature .... -65° to +150°C

Operating Conditions C5/C67401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		-55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	35			23			ns
t_{SIL}	Shift in LOW time	1	35			25			ns
t_{IDS}	Input data setup	1	0			0			ns
t_{IDH}	Input data hold time	1	45			40			ns
t_{SOH}†	Shift Out HIGH time	5	35			23			ns
t_{SOL}	Shift Out LOW time	5	35			25			ns
t_{MRW}	Master Reset pulse	10	40			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature.

Switching Characteristics C5/C67401A/2A

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	10			15			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			50			40	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			50			40	ns
f_{OUT}	Shift Out rate	5	10			15			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			45	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			65			50	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			60			45	ns
t_{PT}	Data throughput or "fall through"	4, 8			2.2			1.6	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}*	Input Ready pulse HIGH	4	30			30			ns
t_{OPH}*	Output Ready pulse HIGH	8	30			30			ns

† See AC test and High Speed application note.
* This parameter applies to FIFOs communicating with each other in a cascaded mode.

Absolute Maximum Ratings

Supply voltage V_{CC} .... −0.5 V to 7 V
Input voltage .... −1.5 V to 7 V
Off-state output voltage .... −0.5 V to 5.5 V
Storage temperature .... −65° to +150° C

Operating Conditions C5/C67401/2

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	45			35			ns
t_{SIL}	Shift in LOW time	1	45			35			ns
t_{IDS}	Input data setup	1	0			0			ns
t_{IDH}	Input data hold time	1	55			45			ns
t_{SOH}†	Shift Out HIGH time	5	45			35			ns
t_{SOL}	Shift Out LOW time	5	45			35			ns
t_{MRW}	Master Reset pulse	10	30			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature.

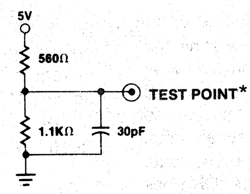
Switching Characteristics C5/C67401/2

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	7			10			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			60			45	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			60			45	ns
f_{OUT}	Shift Out rate	5	7			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			70			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			65			55	ns
t_{PT}	Data throughput or "fall through"	4, 8			4			3	µs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}*	Input Ready pulse HIGH	4	30			30			ns
t_{OPH}*	Output Ready pulse HIGH	8	30			30			ns

† See AC test and High Speed application note.
*This parameter applies to FIFOs communicating with each other in a cascaded mode.

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse 0 to 3V
Input Rise and Fall Time (10% − 90%)
2 − 5 ns.
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0–D_4, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_O = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX Inputs low, outputs open	C5/67401			160	mA
				C5/67402			180	
				C5/67401A			170	
				C5/67402A			190	
				C67401B			180	
				C67402B			200	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†There are absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty). Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e. rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High. This same type of problem is also related to t_{IRH}, t_{ORL} and t_{ORH} as related to Shift-Out.

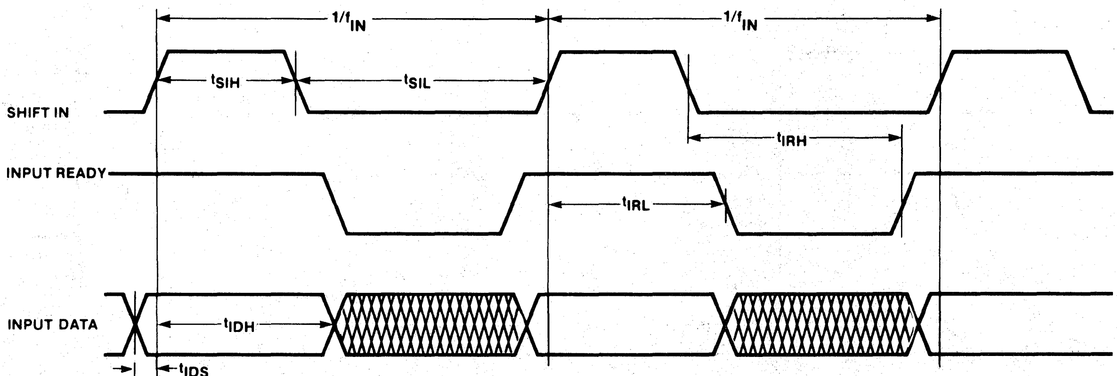


Figure 1. Input Timing

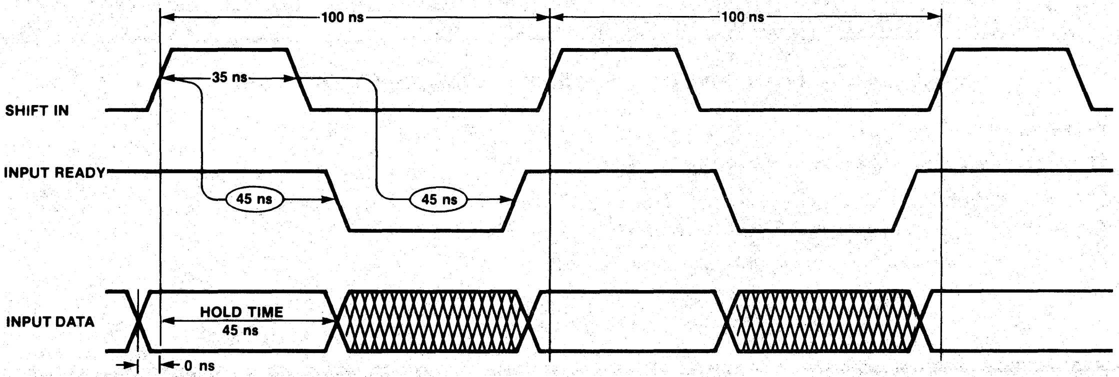


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate

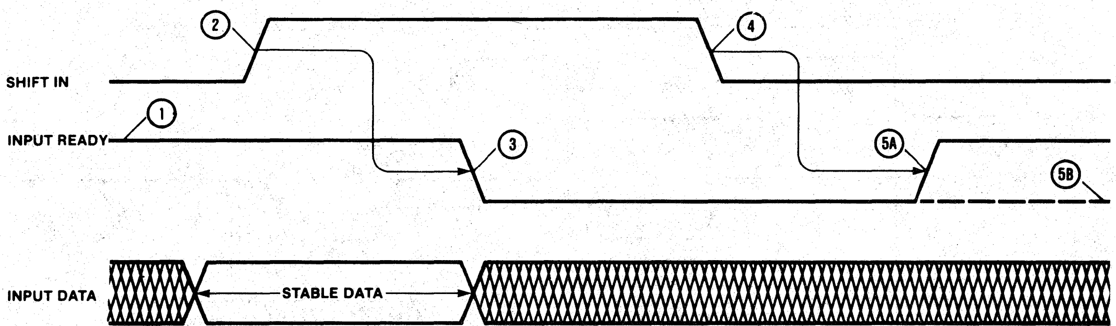


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 4).

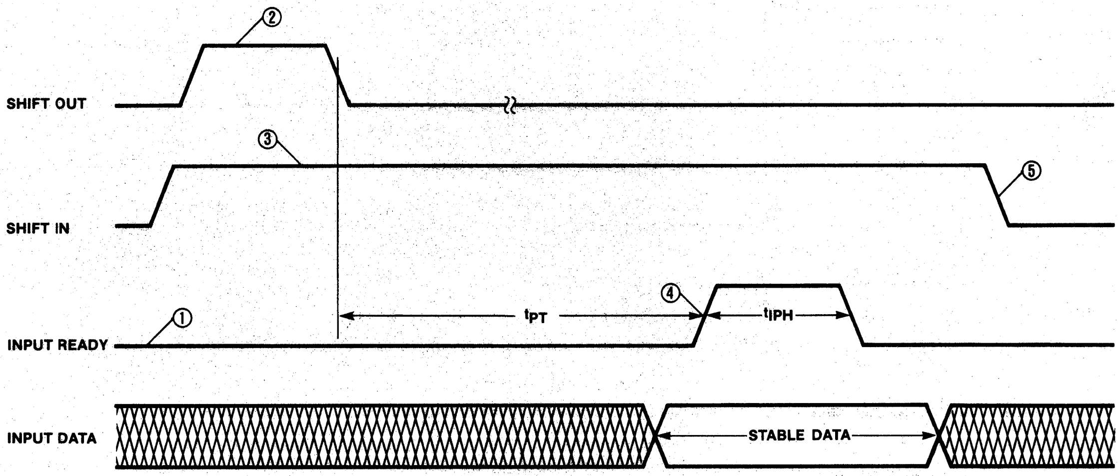
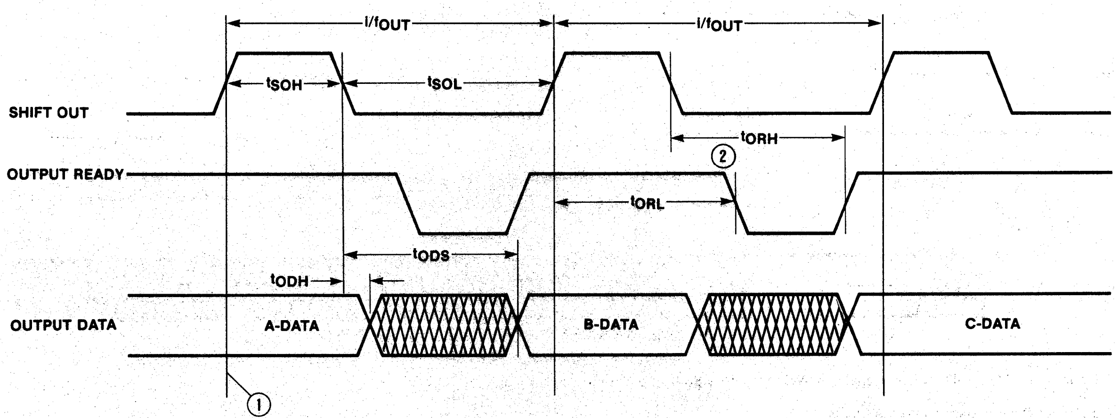


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

1. FIFO is initially full.
2. Shift Out pulse is applied. An empty location starts "bubbling" to the front.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
5. The Data from the first word is released for "fall through" to second word.



1. The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

Figure 5. Output Timing

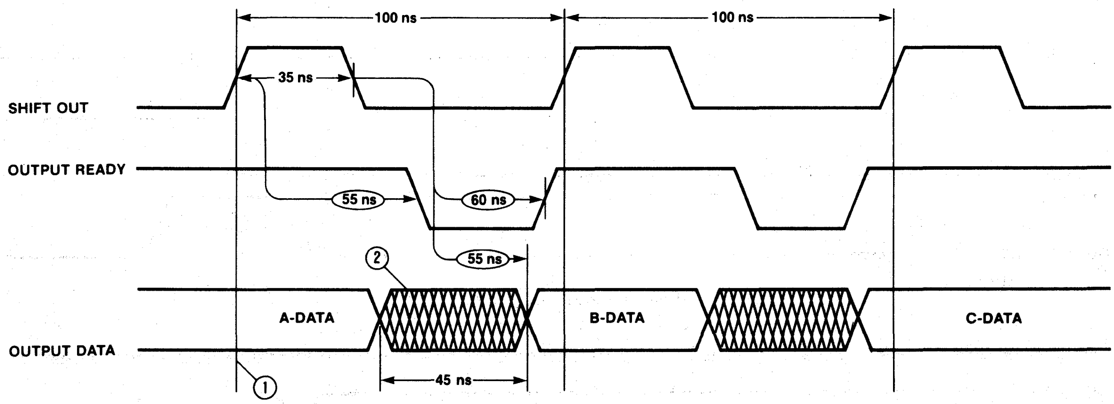


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

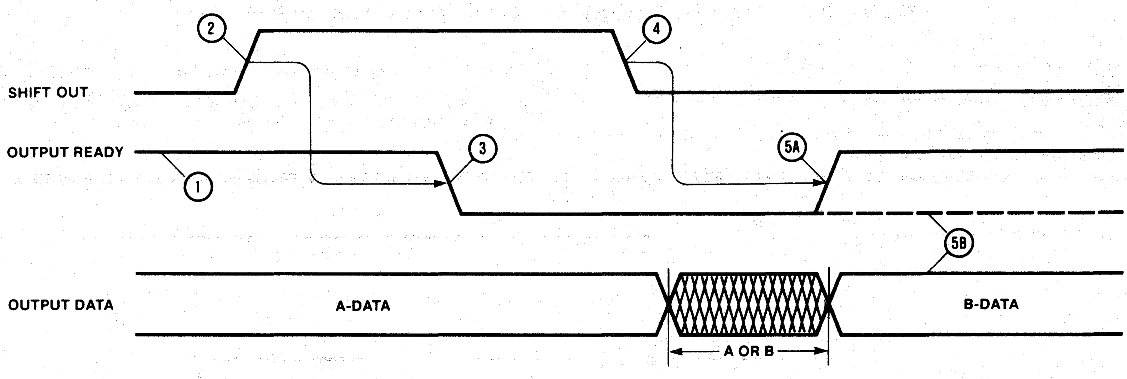


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

(2) Shift Out goes HIGH causing the next step.

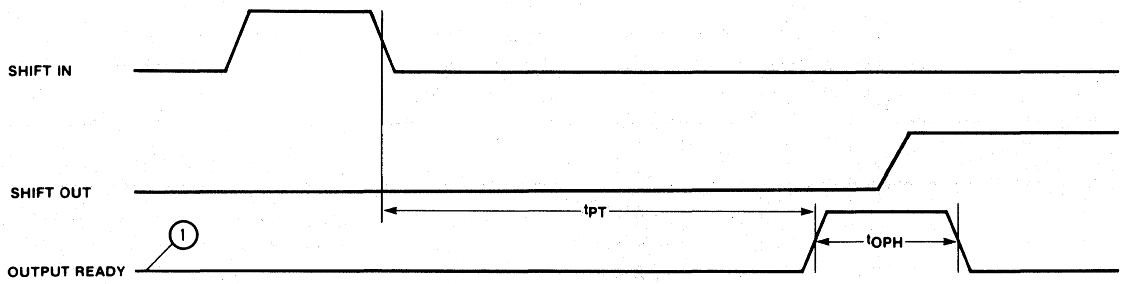
(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.



(1) FIFO initially empty.

Figure 8. t_{PT} and t_{OPH} Specification

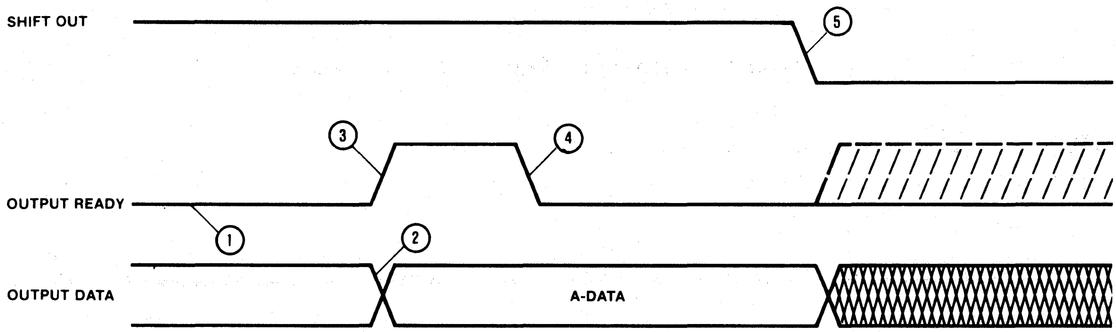


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

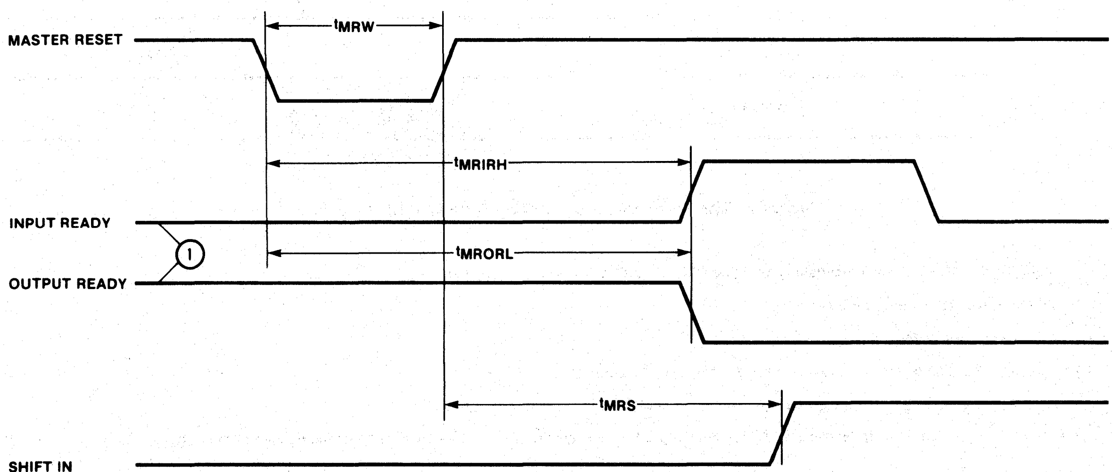
(1) Word 63 is empty.

(2) New data (A) arrives at the outputs (word 63).

(3) Output Ready goes HIGH indicating the arrival of the new data.

(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.

(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



(1) FIFO initially full.

Figure 10. Master Reset Timing

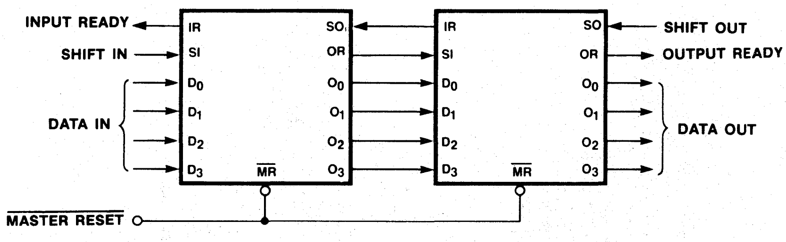


Figure 11. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

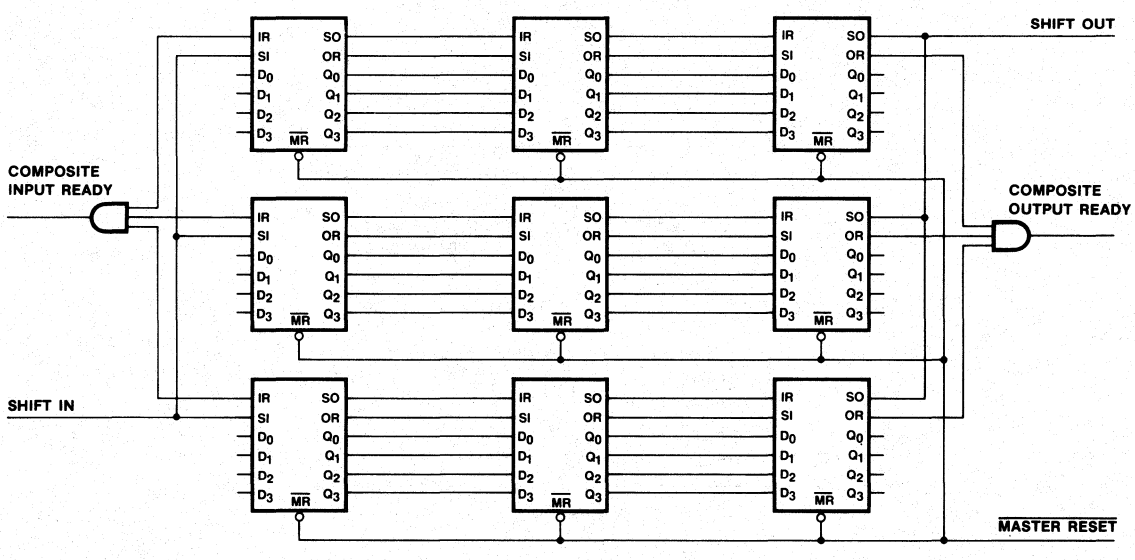
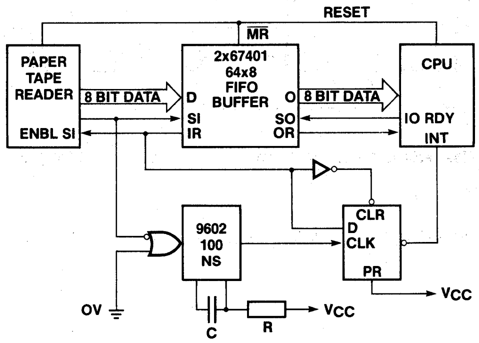


Figure 12. 192x12 FIFO with C5/C67401/1A/1B

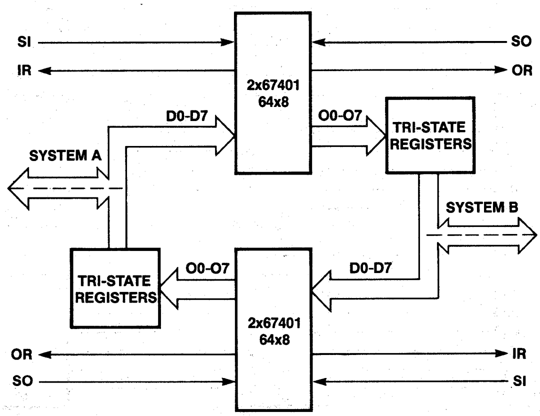
FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.

Applications



NOTE: The output of monostable holds off the "Buffer full" interrupt for 100ns. If 100ns after shift in, there has not been an input Ready to reset the "D Flip-flop" an interrupt is issued, as the FIFO is full. The CPU then empties the FIFO before the next character is output from the tape drive.

Figure 13. Slow Steady Rate to Fast "Blocked" Rate

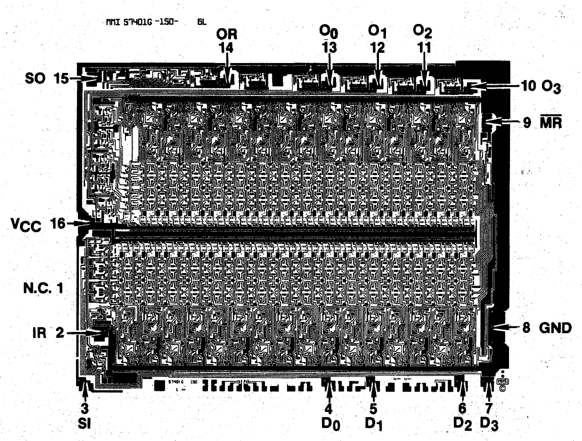


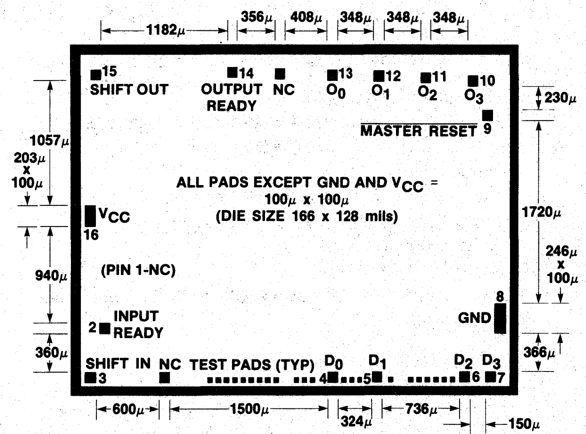
NOTE: Both depth and width expansion can be used in this mode. The IR and OR signals are the anded versions of the individual IR and OR signals.

Figure 14. Bidirectional FIFO Application

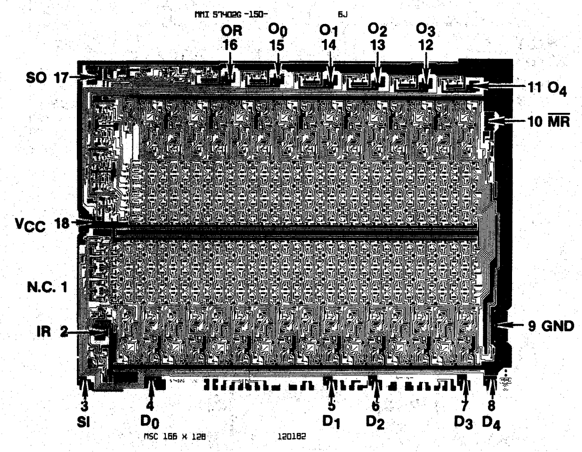
Die Configurations

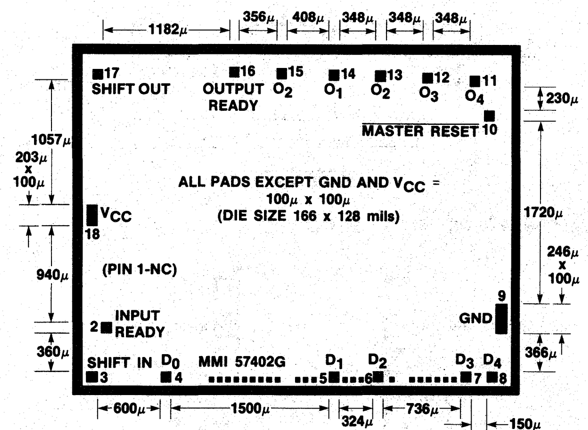
57401 Die Pattern
Step: G
Die Size: 128x166 mil²





57402 Die Pattern
Step: G
Die Size: 128x166 mil²





First-In First-Out (FIFO) 64x4 64x5
Standalone Memory

5/67401 5/67401A 67401B
5/67402 5/67402A 67402B

Features/Benefits

- Choice of 16.7, 15 and 10 MHz shift-out/shift-in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in the word dimension only
- Structured pin outs. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times as fast

Description

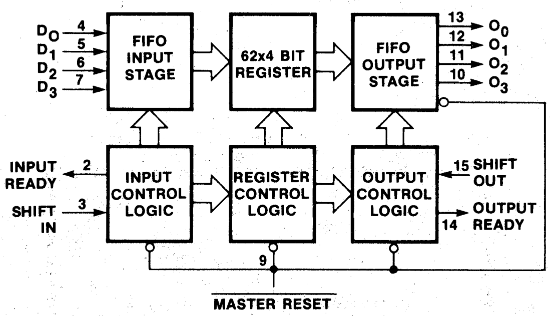
The 5/67401B/2B/1A/2A/1/2 are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4-bits and 64 words by 5-bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. Word length is expandable; FIFO depth is not expandable.

Ordering Information

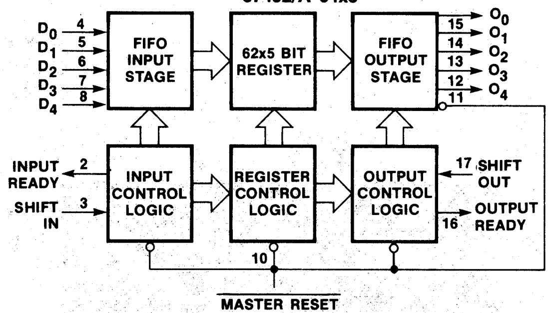
PART NUMBER	PKG	TEMP	DESCRIPTION
57401	J,W(20)(L)	Mil	7 MHz 64x4 FIFO
67401	J,N	Com	10 MHz 64x4 FIFO
57402	J,W(20)(L)	Mil	7MHz 64x5 FIFO
67402	J,N	Com	10 MHz 64x5 FIFO
57401A	J,W(20)(L)	Mil	10 MHz 64x4 FIFO
67401A	J	Com	15 MHz 64x4 FIFO
57402A	J,W(20)(L)	Mil	10 MHz 64x5 FIFO
67402A	J	Com	15 MHz 64x5 FIFO
67401B	J	Com	16.7 MHz 64x4 FIFO
67402B	J	Com	16.7 MHz 64x5 FIFO

Block Diagrams

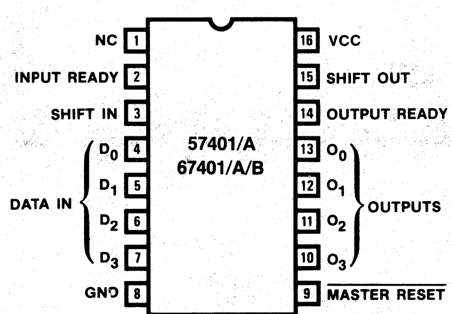
67401/A/B 64x4
57401/A 64x4

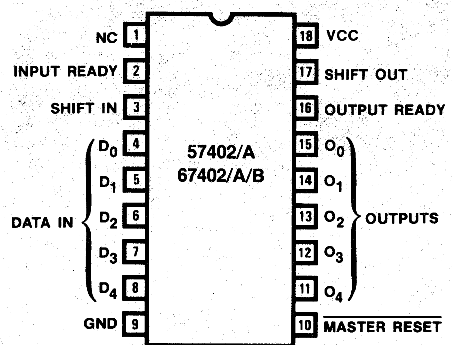


5/67402/A/B 64x5
57402/A 64x5



Pin Configurations





TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} .... −1.5 V to 7 V
Input voltage .... −1.5 V to 7 V
Off-state output voltage .... −0.5 V to 5.5 V
Storage temperature .... −65° to +150°C

Operating Conditions 67401B/2B

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH} †	Shift in HIGH time	1	18			ns
t_{SIL}	Shift in LOW time	1	18			ns
t_{IDS}	Input data setup	1	5			ns
t_{IDH}	Input data hold time	1	40			ns
t_{SOH} †	Shift Out HIGH time	5	18			ns
t_{SOL}	Shift Out LOW time	5	18			ns
t_{MRW}	Master Reset pulse	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

*Case temperature.

7

Switching Characteristics 67401B/2B

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
f_{IN}	Shift in rate	1	16.7			MHz
t_{IRL}	Shift In to input ready LOW	1			35	ns
t_{IRH}	Shift In to input ready HIGH	1			37	ns
f_{OUT}	Shift Out rate	5	16.7			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			38	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			44	ns
t_{ODH}	Output Data Hold (previous word)	5	5			ns
t_{ODS}	Output Data Shift (next word)	5			44	ns
t_{PT}	Data throughput or "fall through"	4,8			1.3	μs
t_{MRORL}	Master Reset to OR LOW	10			55	ns
t_{MRIRH}	Master Reset to IR HIGH	10			55	ns
t_{IPH}	Input Ready pulse HIGH	4	15			ns
t_{OPH}	Output Ready pulse HIGH	8	15			ns

†See A/C Test and High Speed Application Note.

Absolute Maximum Ratings

Supply voltage V_{CC} .... −0.5 V to 7 V
Input voltage .... −1.5 V to 7 V
Off-state output voltage .... −0.5 V to 5.5 V
Storage temperature .... −65° to +150°C

Operating Conditions 5/67401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	35			23		28†	ns
t_{SIL}	Shift in LOW time	1	35			25			ns
t_{IDS}	Input data setup	1	5			5			ns
t_{IDH}	Input data hold time	1	45			40			ns
t_{SOH}†	Shift Out HIGH time	5	35			23			ns
t_{SOL}	Shift Out LOW time	5	35			25			ns
t_{MRW}	Master Reset pulse	10	40			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature.

Switching Characteristics 5/67401A/2A

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	10			15			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			50			40	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			50			40	ns
f_{OUT}	Shift Out rate	5	10			15			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			45	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			65			50	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			60			45	ns
t_{PT}	Data throughput or "fall through"	4, 8			2.2			1.6	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}	Input Ready pulse HIGH	4	20			20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			20			ns

Absolute Maximum Ratings

Supply voltage V_{CC} .... −0.5 V to 7 V
Input voltage .... −1.5 V to 7 V
Off-state output voltage .... −0.5 V to 5.5 V
Storage temperature .... −65° to +150° C

Operating Conditions 5/67401/2

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	45			35			ns
t_{SIL}	Shift in LOW time	1	45			35			ns
t_{IDS}	Input data setup	1	10			5			ns
t_{IDH}	Input data hold time	1	55			45			ns
t_{SOH}†	Shift Out HIGH time	5	45			35			ns
t_{SOL}	Shift Out LOW time	5	45			35			ns
t_{MRW}	Master Reset pulse†	10	30			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature.

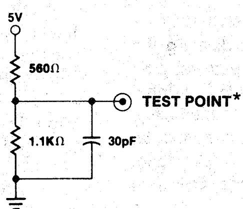
Switching Characteristics 5/67401/2

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	7			10			MHz
t_{IRL}†	Shift In to input ready LOW	1			60			45	ns
t_{IRH}†	Shift In to input ready HIGH	1			60			45	ns
f_{OUT}	Shift Out rate	5	7			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			70			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			65			55	ns
t_{PT}	Data throughput or "fall through"	4,8			4			3	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}	Input Ready pulse HIGH	4	20			20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			20			ns

†See AC test and high speed application note.

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse 0 to 3 V
Input Rise and Fall Time (10% to 90%) 2 – 5 ns.
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0–D_4, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_0 = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX Inputs low, outputs open.	5/67401			160	
				5/67402			180	
				5/67401A			170	
				5/67402A			190	
				67401B			180	
				67402B			200	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
†There are absolute voltages with respect to degree GND (PIN 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High.If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High. This same type of problem is also related to t_{IRH}, t_{ORL}, and t_{ORH} as related to Shift-Out.

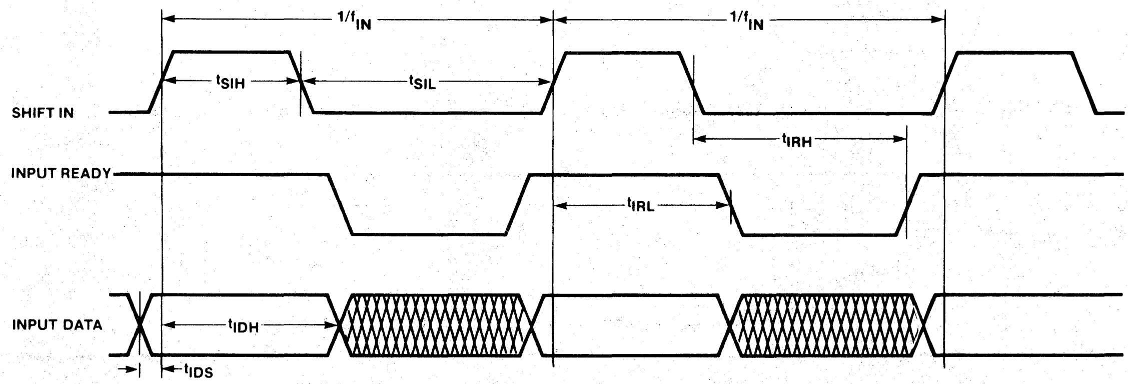


Figure 1. Input Timing

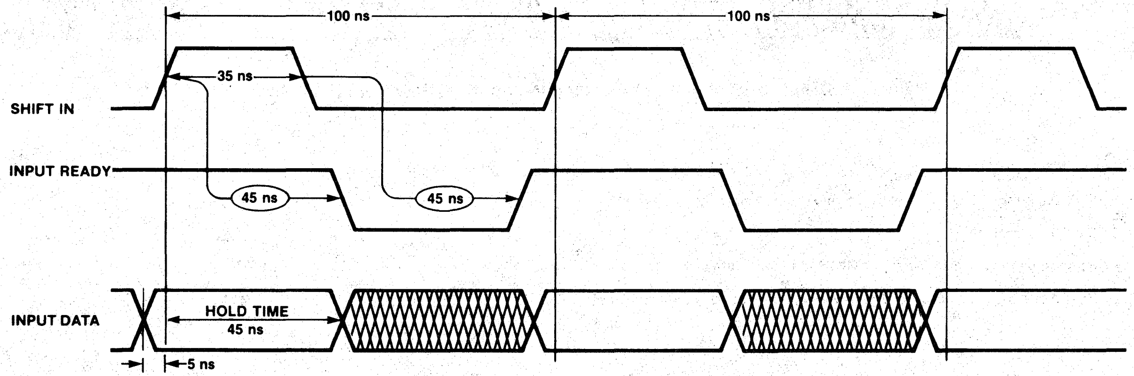


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate (67401/2)

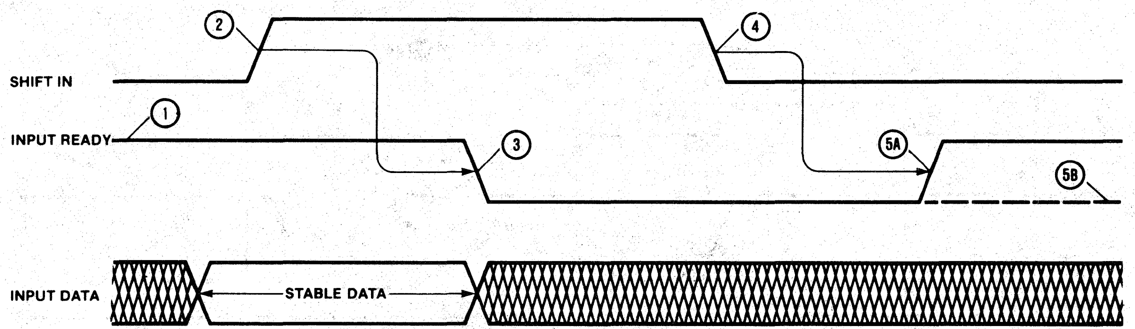


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored. (See Figure 4.)

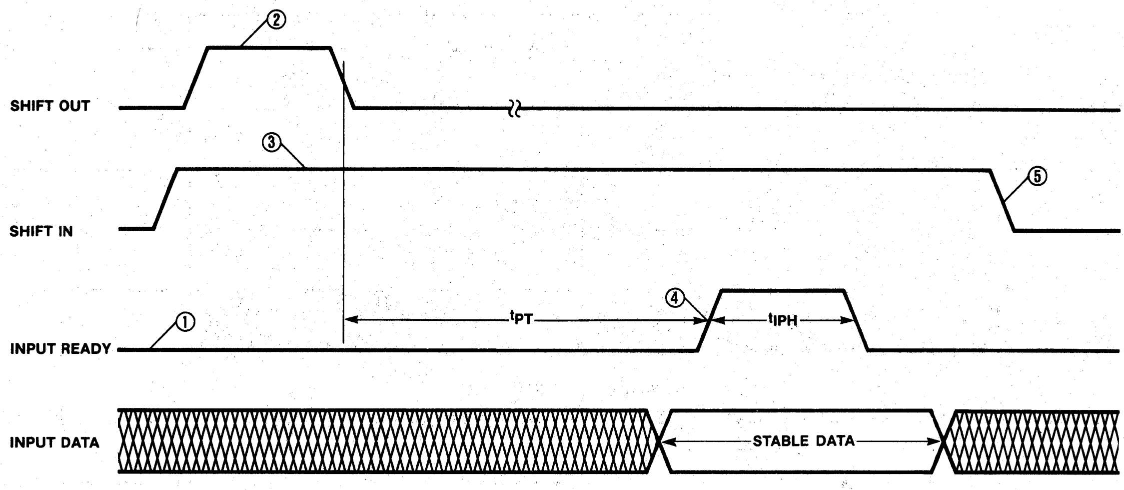


Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

1. FIFO is initially full.
2. Shift Out pulse is applied. An empty location starts "bubbling" to the front.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
5. The Data from the first word is released for "fall through" to second word.

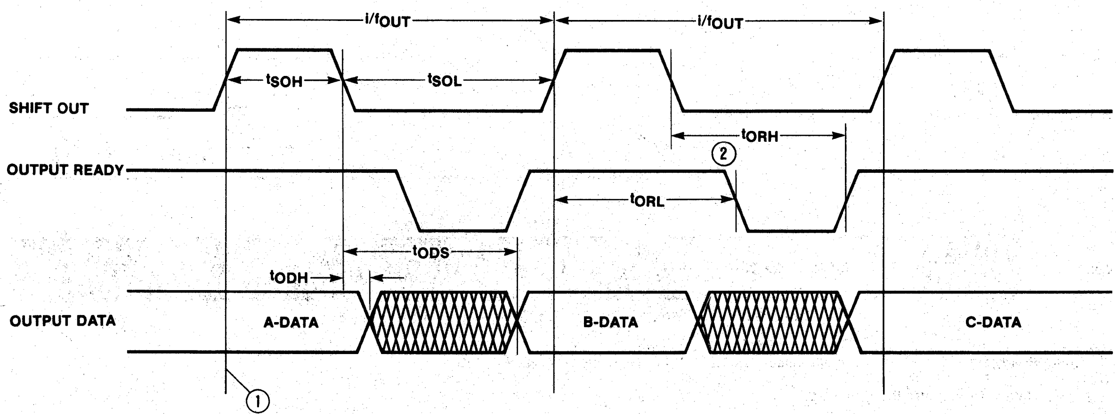


Figure 5. Output Timing

1. The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

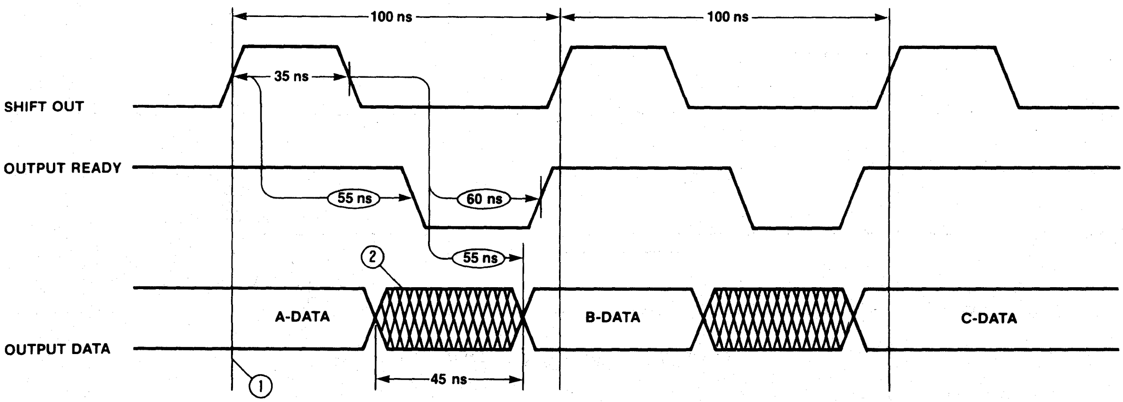


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate (67401/2)

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

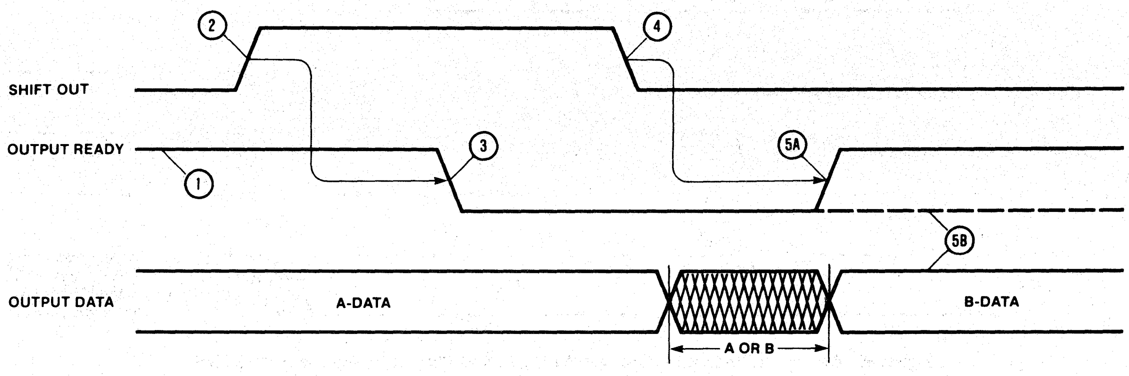


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.

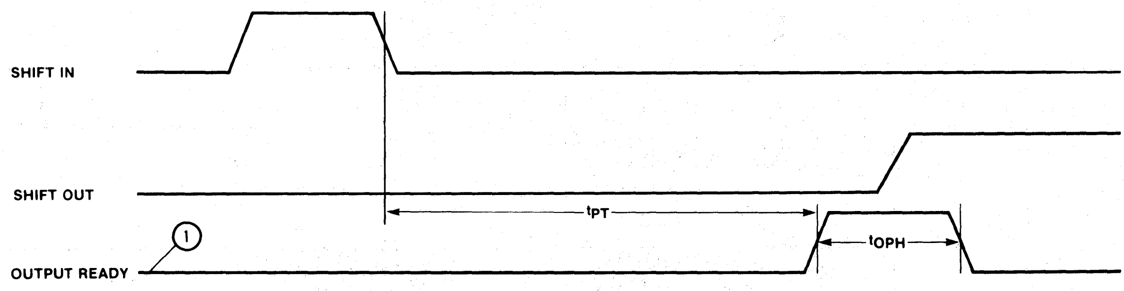


Figure 8. t_{PT} and t_{OPH} Specification

(1) FIFO initially empty.

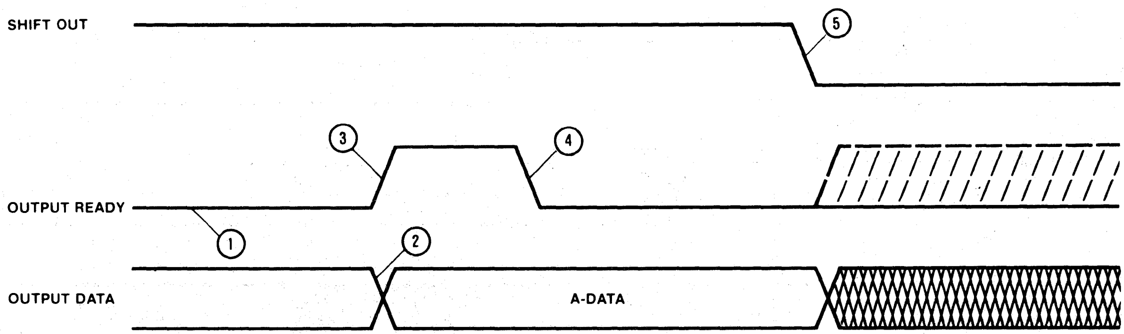


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

(1) Word 63 is empty.

(2) New data (A) arrives at the outputs (word 63).

(3) Output Ready goes HIGH indicating the arrival of the new data.

(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.

(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

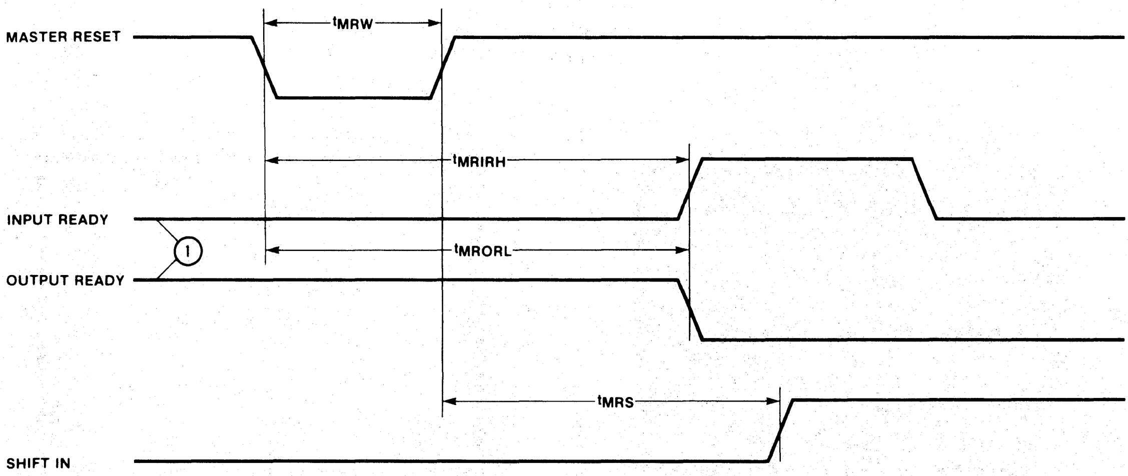


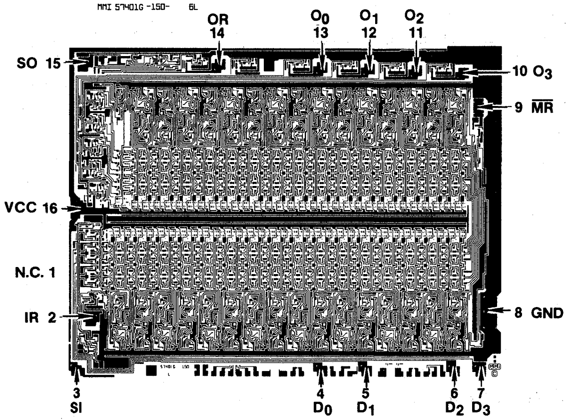
Figure 10. Master Reset Timing

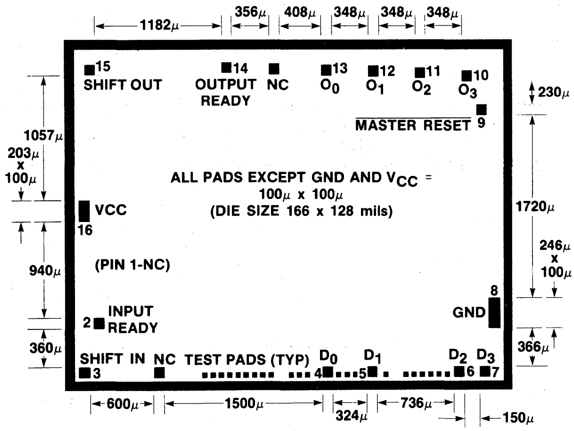
(1) FIFO initially full.

7

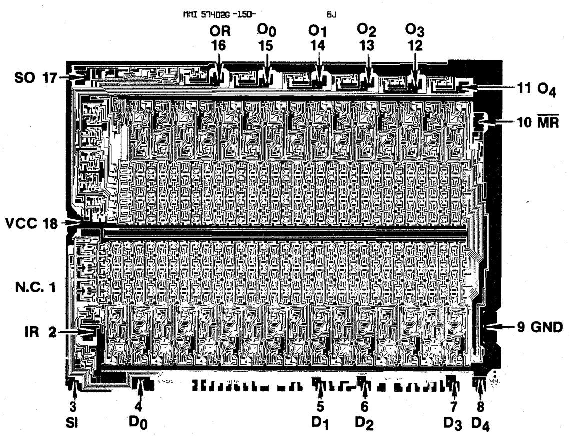
Die Configurations

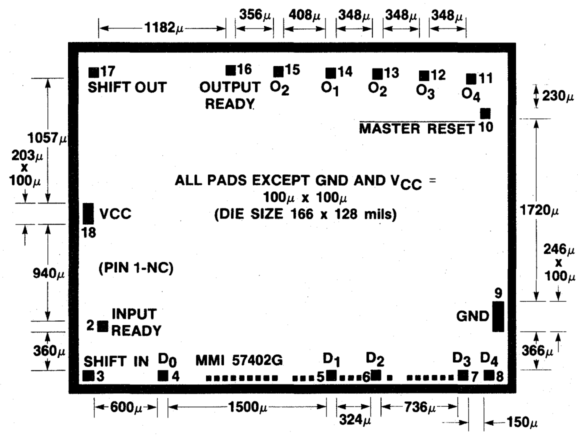
57401 Die Pattern
Step: G
Die Size: 128x166 mil^2





57402 Die Pattern
Step: G
Die Size: 128x166 mil^2





Low Power First-In First-Out (FIFO) 64x4 Cascadable Memory
67L401

Features/Benefits

- Guaranteed 5 MHz shift-out/shift-in rates
- Low Power Consumption
- TTL inputs and outputs
- Readily expandable in the word and bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and much faster

Description

The 67L401 is a low-power First In/First Out (FIFO) memory device with TTL speed. This device is organized in a 64x4-bit structure and easily cascadable with similar FIFOs to any depth or width. A 5MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. FIFOs can be cascaded to any depth in a handshake mode. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

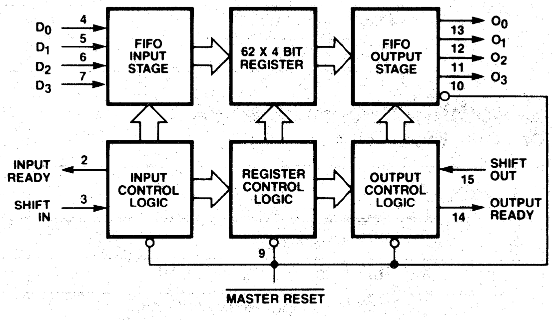
Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67L401 is particularly useful where low-power consumption is critical.

Ordering Information

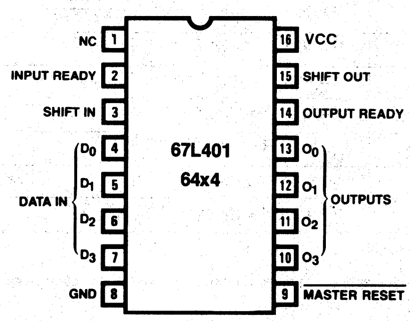
PART NUMBER	PKG	TEMP	DESCRIPTION
67L401	N	COM	5 MHz 64x4 FIFO
67L401	J	COM	5 MHz 64x4 FIFO

Block Diagram

67L401 64x4



Pin Configuration



7

Absolute Maximum Ratings

Supply voltage V_{CC} .... −0.5 V to 7 V
Input voltage .... −1.5 V to 7 V
Off-state output voltage .... −0.5 V to 5.5 V
Storage temperature .... −65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	55			ns
t_{SIL}	Shift in LOW time	1	55			ns
t_{IDS}	Input data setup	1	10			ns
t_{IDH}	Input data hold time	1	80			ns
t_{SOH}†	Shift Out HIGH time	5	55			ns
t_{SOL}	Shift Out LOW time	5	55			ns
t_{MRW}	Master Reset pulse	10	40			ns
t_{MRS}	Master Reset to SI	10	35			ns

Switching Characteristics

Over Operating Conditions

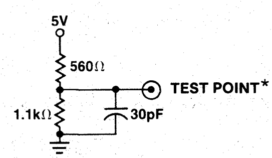
SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	5			MHz
t_{IRL}†	Shift in to Input Ready LOW	1			75	ns
t_{IRH}†	Shift in to Input Ready HIGH	1			75	ns
f_{OUT}	Shift Out rate	5	5			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			75	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			80	ns
t_{ODH}	Output Data Hold (previous word)	5	8			ns
t_{ODS}	Output Data Shift (next word)	5			70	ns
t_{PT}	Data throughput or "fall through"	4, 8			4	μs
t_{MRORL}	Master Reset to OR LOW	10			85	ns
t_{MRIRH}	Master Reset to IR HIGH	10			85	ns
t_{IPH}*	Input Ready pulse HIGH	4	20			ns
t_{OPH}*	Output Ready pulse HIGH	8	20			ns

† See AC test and application note.

* This parameter applies to FIFOs communicating with each other in a cascade mode.

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse = 3V
Input Rise and Fall Time (10% - 90%)
2 - 5 ns.
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level	D_0–D_3 MR	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}	input current	SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	−20		−90	mA
I_{CC}	Supply Current		V_{CC} = MAX	Inputs Low, Outputs Open		95	110	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† This is an absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment.

7

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and Application Note

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing. Though the external data rate is 5 MHz internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO will respond to very small glitches caused by long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in timing set up and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination, as well as the Shift Out-Output Ready Combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High.If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High.

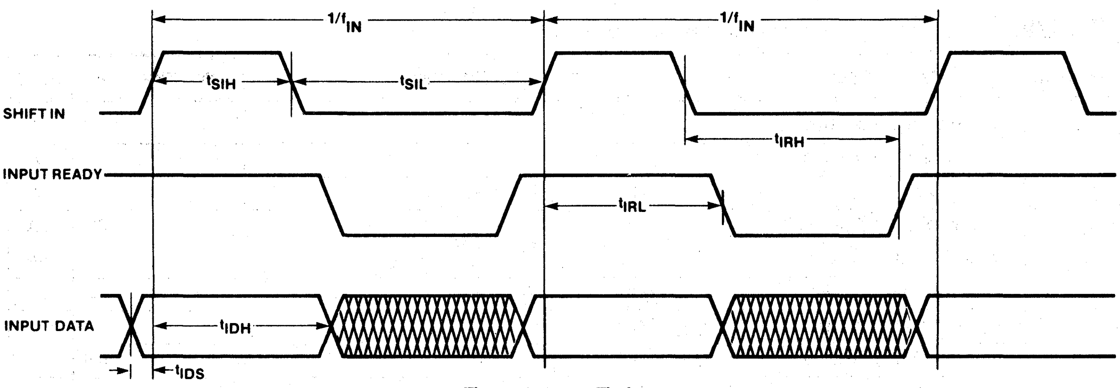


Figure 1. Input Timing

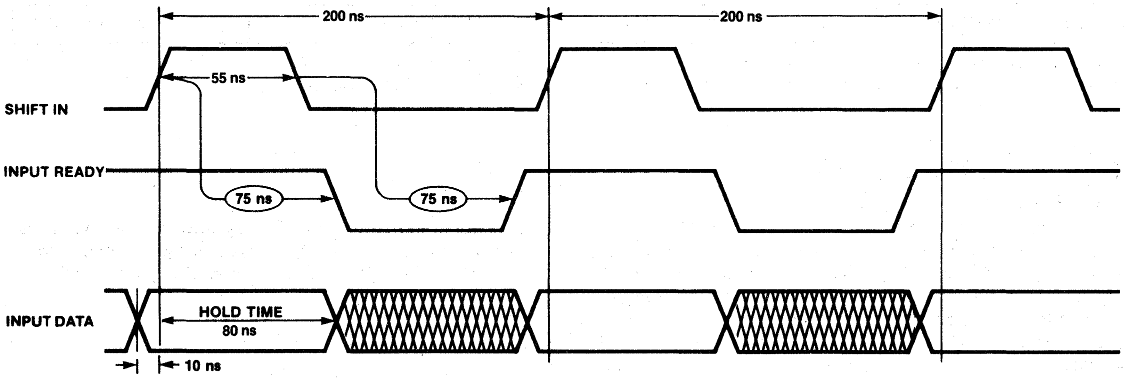


Figure 2. Typical Waveforms for 5 MHz Shift in Data Rate

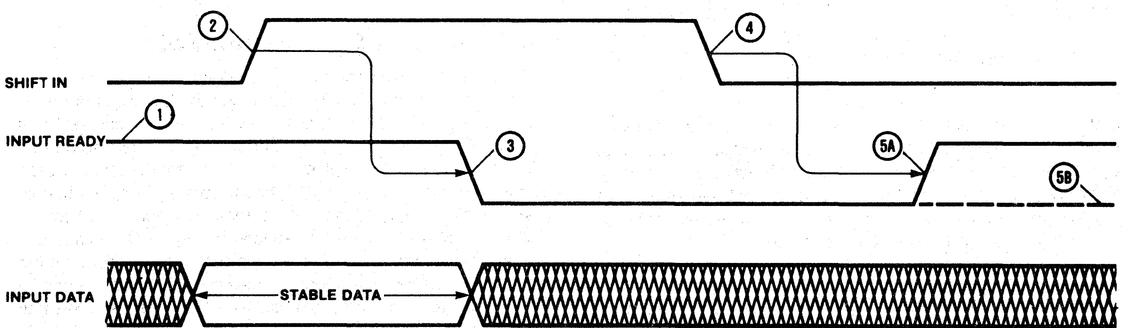


Figure 3. The Mechanism of Shifting Data into the FIFO

1 Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

2 Input Data is loaded into the first word.

3 Input Ready goes LOW indicating the first word is full.

4 The Data from the first word is released for "fall-through" to second word.

5A The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

5B If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

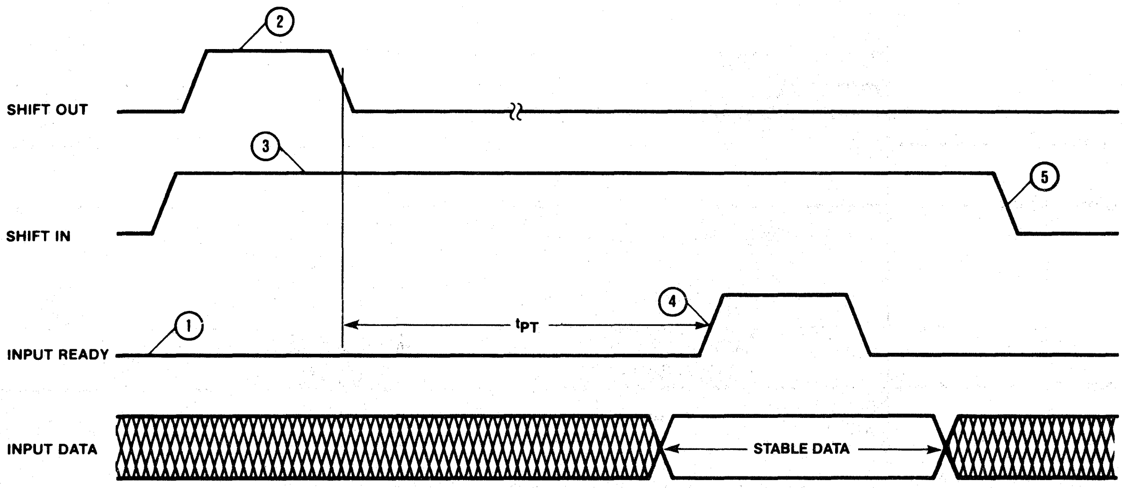


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

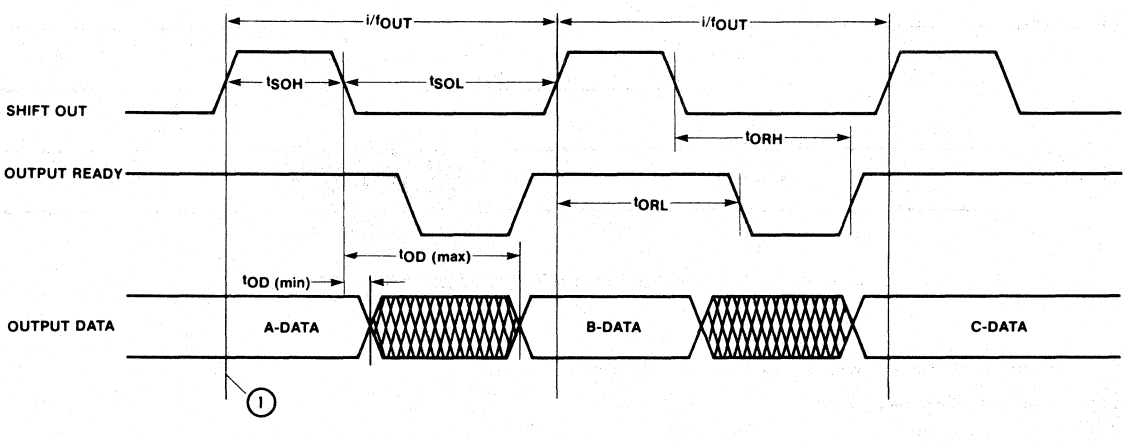
1 FIFO is initially full.

2 Shift Out pulse is applied. An empty location start "bubbling" to the front.

3 Shift In is held HIGH.

4 As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

5 The Data from the first word is released for "fall through" to second word.



1 The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

Figure 5. Output Timing

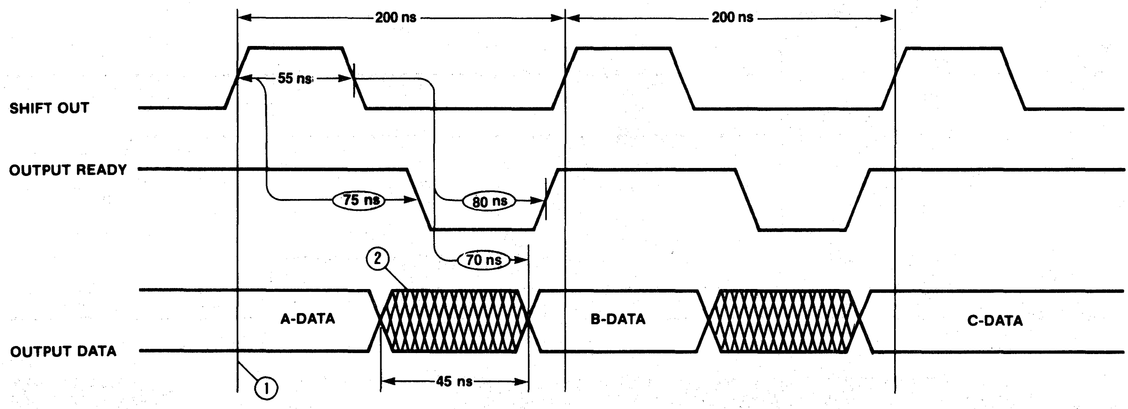


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

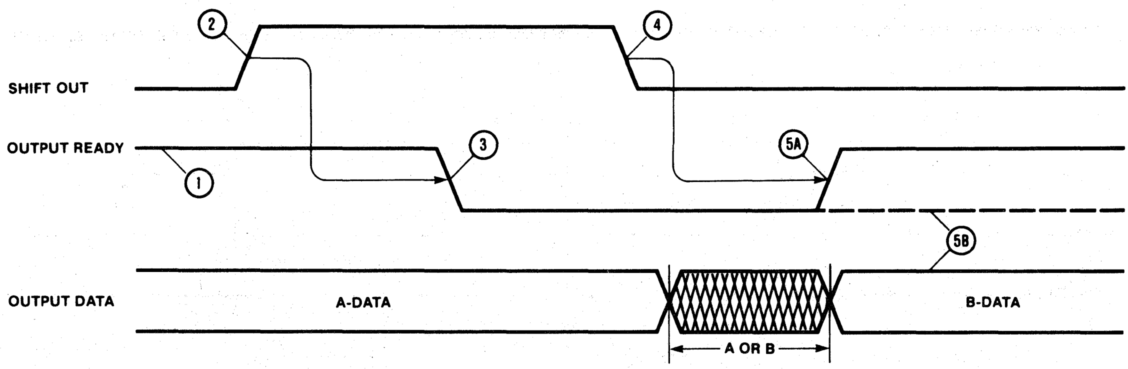


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

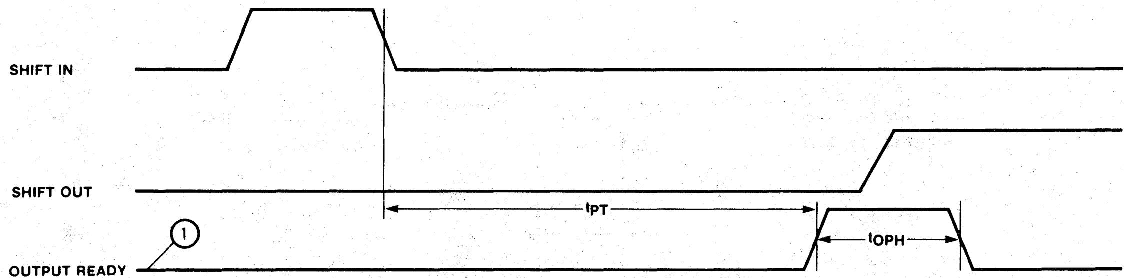
(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.



1 FIFO initially empty.

Figure 8. t_{PT} and t_{OPH} Specification

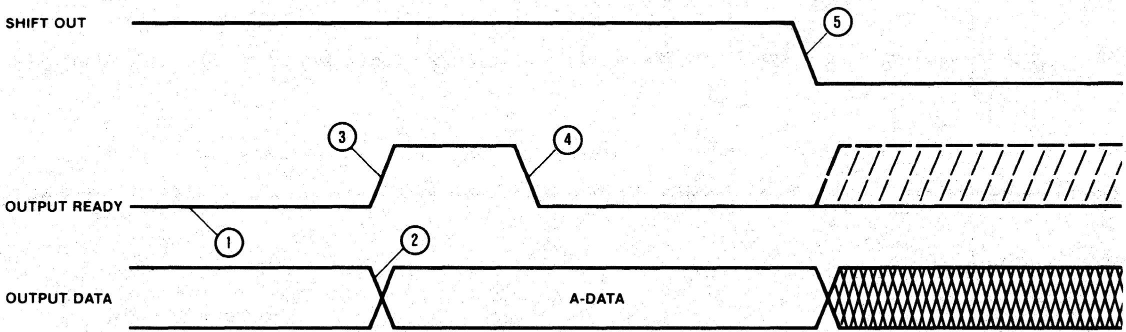


Figure 9. Data is ,Shifted Out Whenever Shift Out and Output Ready are Both HIGH

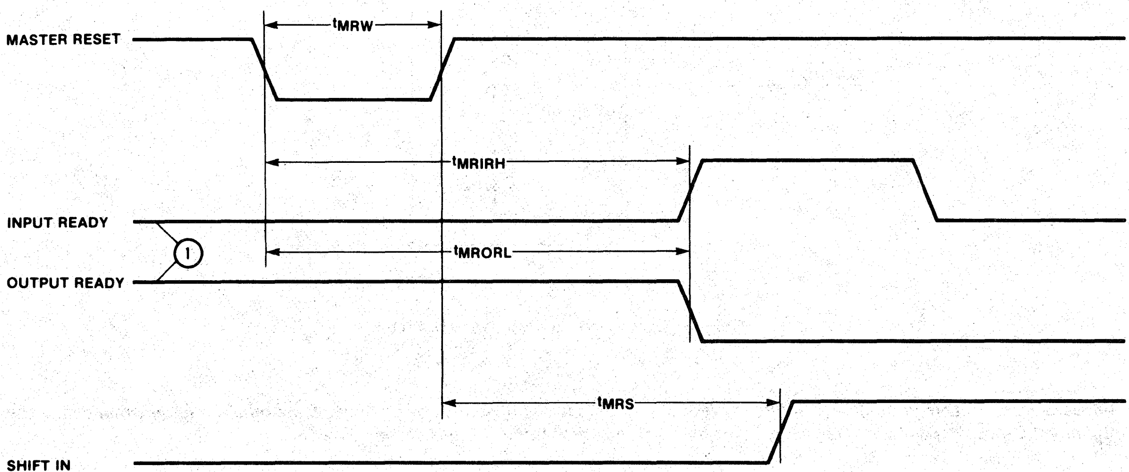
1 Word 63 is empty.

2 New data (A) arrives at the outputs (word 63).

3 Output Ready goes HIGH indicating the arrival of the new data.

4 Since Shift Out is held HIGH, Output Ready goes immediately LOW.

5 As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



1 FIFO initially full.

Figure 10. Master Reset Timing

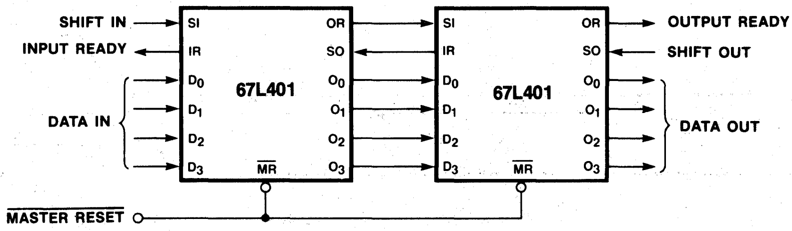


Figure 11. Cascading FIFOs to Form 128 x 4 FIFO with 67L401's

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

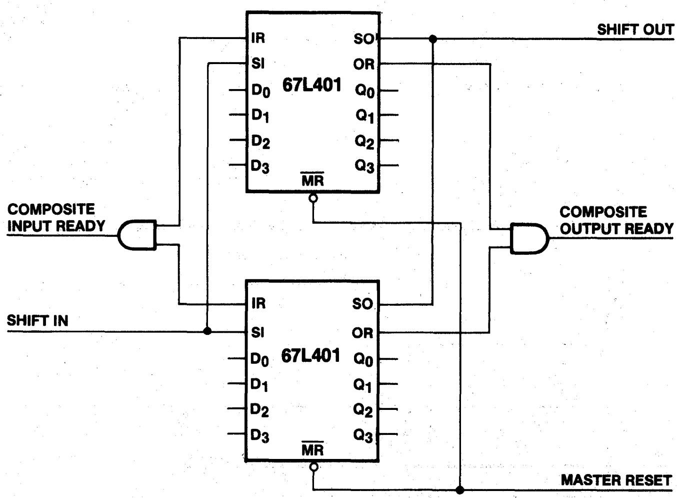


Figure 12. 64 x 8 FIFO with two 67L401's

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 13.

The 67L401 can also be used in a bidirectional operation as shown in Figure 14.

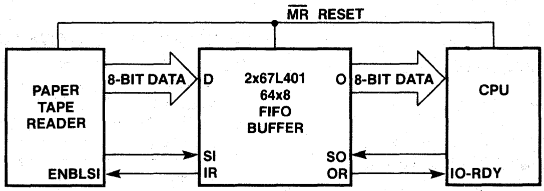
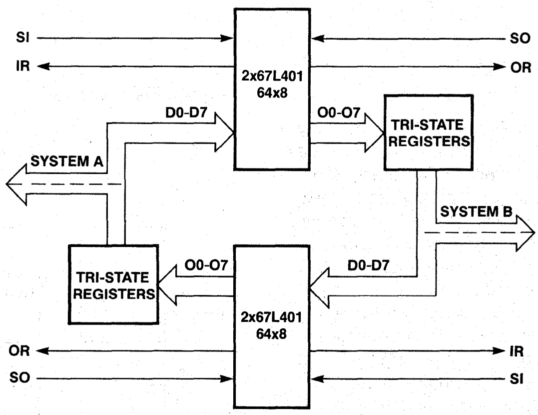


Figure 13. FIFO as data buffer between slow steady rate and fast 'burst' rate

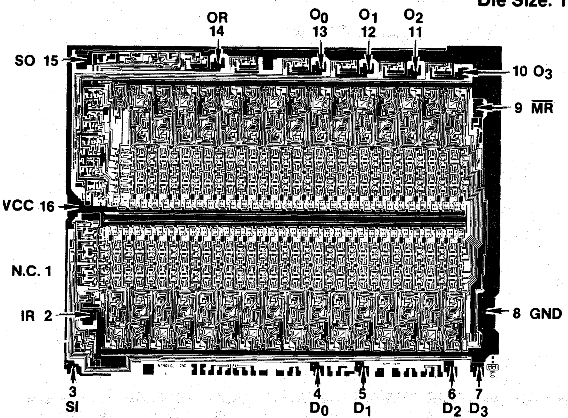


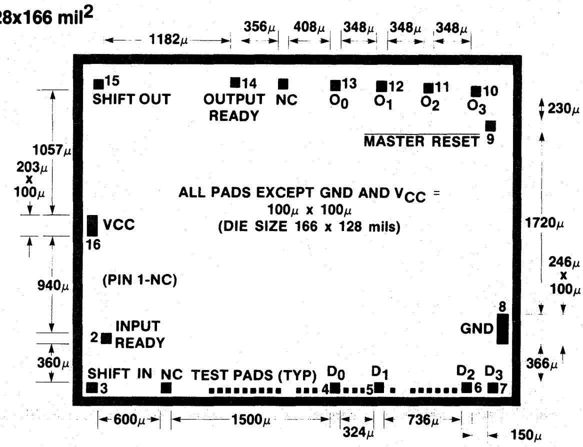
NOTE: Both depth and width expansion can be used in this mode.

Figure 14. Bidirectional FIFO application

Die Configurations

57401 Die Pattern
Step: G
Die Size: 128x166 mil^2





Low Power First-In First-Out (FIFO) 64x5 Cascadable Memory
67L402

Features/Benefits

- Guaranteed 5 MHz shift-out/shift-in rates
- Low power consumption
- TTL inputs and outputs
- Readily expandable in the word and bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation

Ordering Information

PART PACKAGE	PKG	TEMP	DESCRIPTION
67L402	N	COM	5 MHz 64x5 FIFO
67L402	J	COM	5 MHz 64x5 FIFO

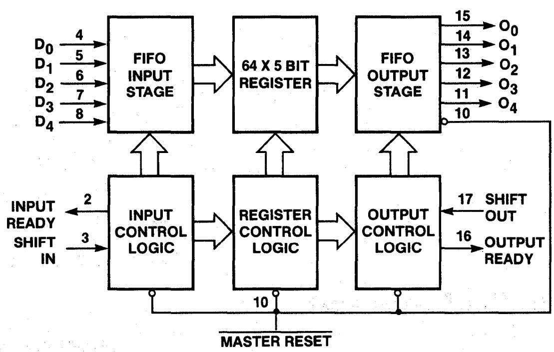
Description

The 67L402 is a low-power First-In First-Out (FIFO) memory device with TTL speed. This device is organized in a 64x5-bit structure and easily cascadable with similar FIFOs to any depth or width. A 5 MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. FIFOs can be cascaded to any depth in a handshake mode. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

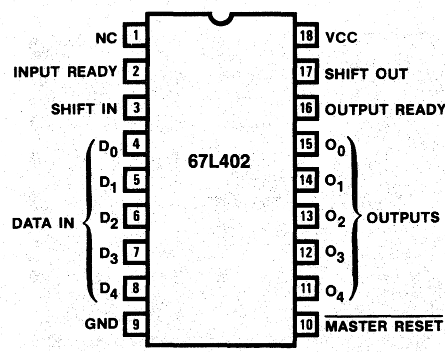
Generally. FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67L402 is particularly useful where low-power consumption is critical.

Block Diagram

67L402 64x5



Pin Configuration



Absolute Maximum Ratings

Supply voltage V_{CC} .... -0.5 V to 7 V
Input voltage .... -1.5 V to 7 V
Off-state output voltage .... -0.5 V to 5.5 V
Storage temperature .... -65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	55			ns
t_{SIL}	Shift in LOW time	1	55			ns
t_{IDS}	Input data setup	1	10			ns
t_{IDH}	Input data hold time	1	80			ns
t_{SOH}†	Shift Out HIGH time	5	55			ns
t_{SOL}	Shift Out LOW time	5	55			ns
t_{MRW}	Master Reset pulse	10	40			ns
t_{MRS}	Master Reset to SI	10	35			ns

Switching Characteristics

Over Operating Conditions

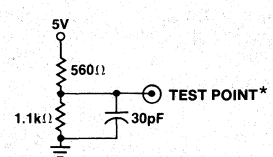
SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	5			MHz
t_{IRL}†	Shift in to Input Ready LOW	1			75	ns
t_{IRH}†	Shift in to Input Ready HIGH	1			75	ns
f_{OUT}	Shift Out rate	5	5			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			75	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			80	ns
t_{ODH}	Output Data Hold (previous word)	5	8			ns
t_{ODS}	Output Data Shift (next word)	5			70	ns
t_{PT}	Data throughput or "fall through"	4, 8			4	μs
t_{MRORL}	Master Reset to OR LOW	10			85	ns
t_{MRIRH}	Master Reset to IR HIGH	10			85	ns
t_{IPH}*	Input Ready pulse HIGH	4	20			ns
t_{OPH}*	Output Ready pulse HIGH	8	20			ns

† See AC test and application note.

* This parameter applies to FIFOs communicating with each other in a cascade mode.

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse = 3V
Input Rise and Fall Time (10% - 90%) 2 - 5 ns.
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0-D_3 MR	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_0 = 0V	−20		−90	mA
I_{CC}	Supply Current		V_{CC} = MAX	Inputs Low, Outputs Open		113	130	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† This is an absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and Application Note

Since the FIFO is a high-speed device, care must be exercised in design of the hardware and the timing. Though the external data rate is 5 MHz, internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO is sensitive to very small glitches caused by long reflective lines, high capacitances, and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with a very short lead length. In addition, care must be exercised in timing setup and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination as well as the Shift Out-Output Ready Combination, timing measurements may be misleading. i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High.

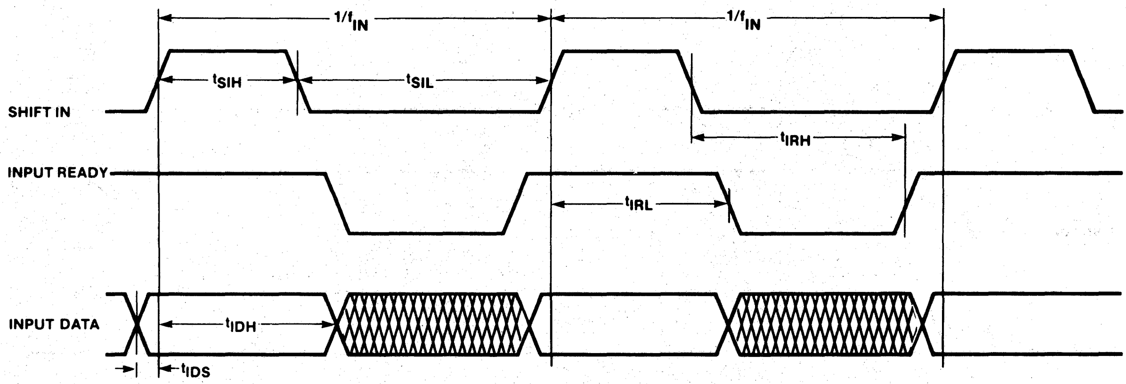


Figure 1. Input Timing

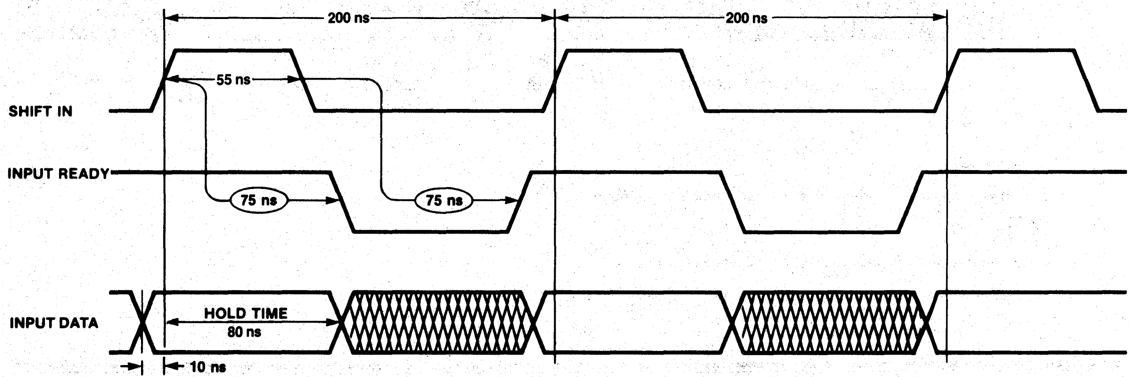


Figure 2. Typical Waveforms for 5 MHz Shift in Data Rate

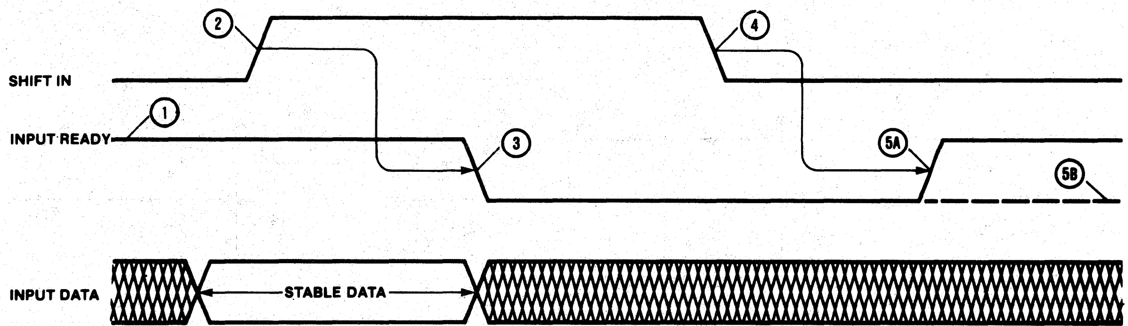


Figure 3. The Mechanism of Shifting Data into the FIFO

1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the first word.
3. Input Ready goes LOW indicating the first word is full.
4. The Data from the first word is released for "fall-through" to second word.

5A. The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

5B. If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

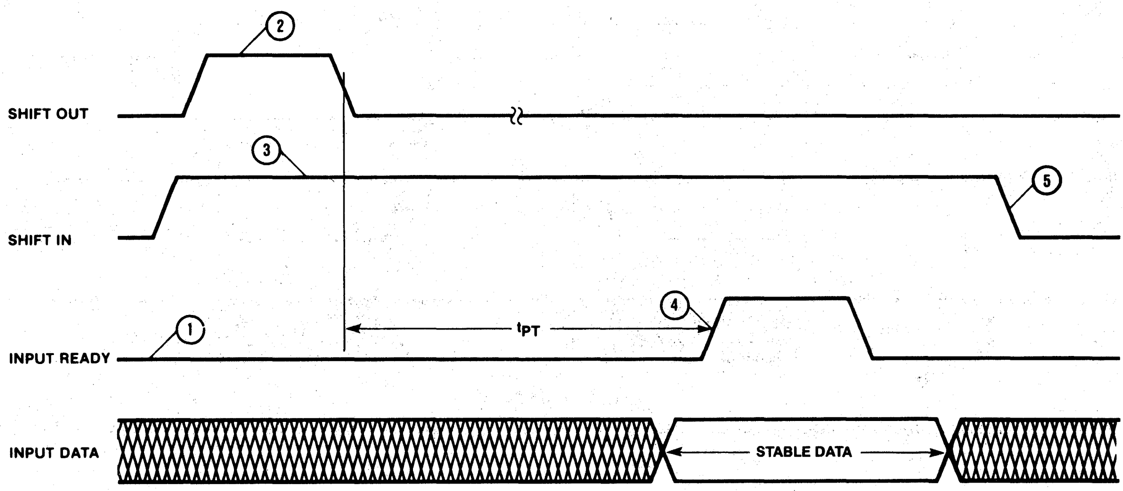


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

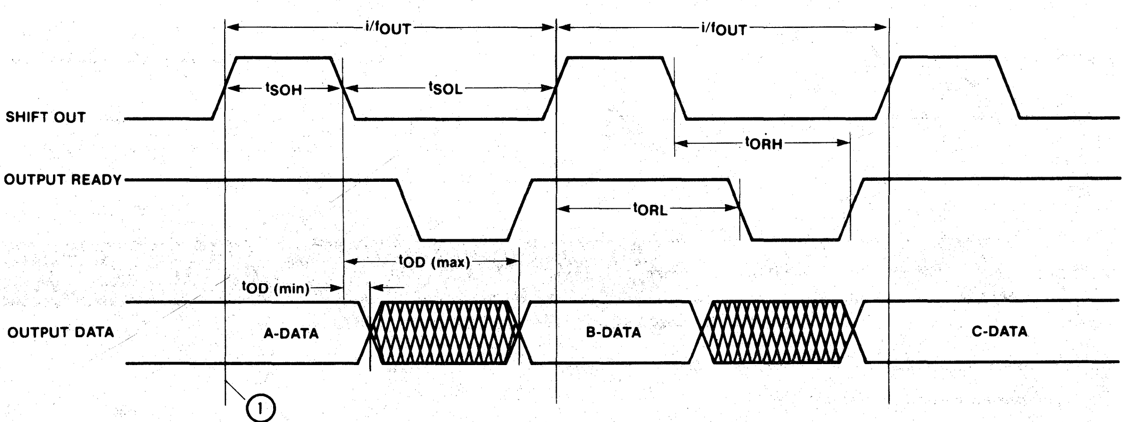
(1) FIFO is initially full.

(2) Shift Out pulse is applied. An empty location start "bubbling" to the front.

(3) Shift In is held HIGH.

(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

(5) The Data from the first word is released for "fall through" to second word.



(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

Figure 5. Output Timing

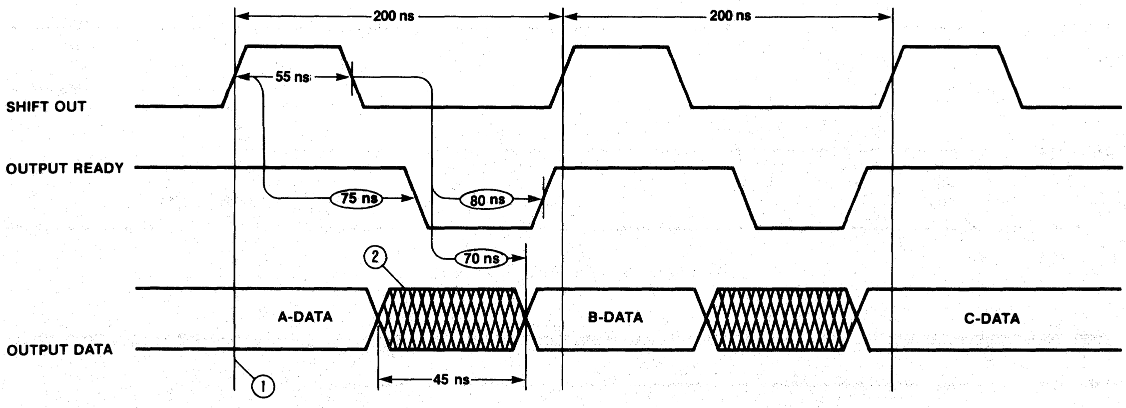


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

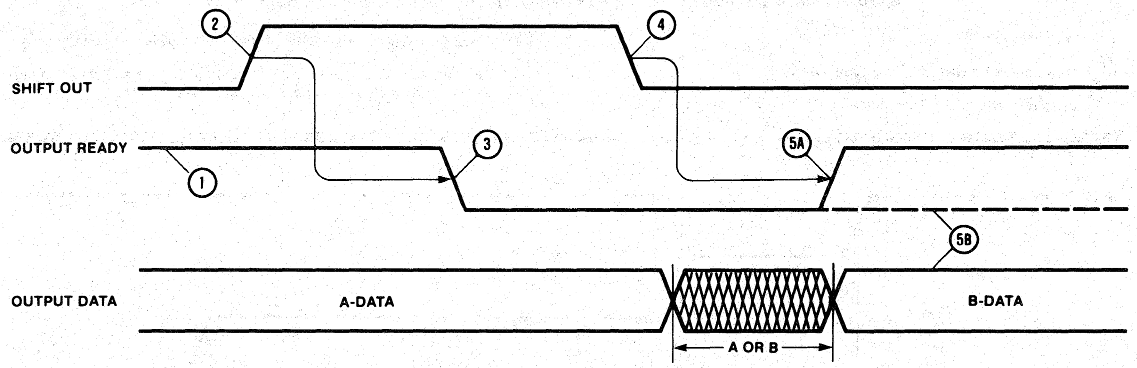


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

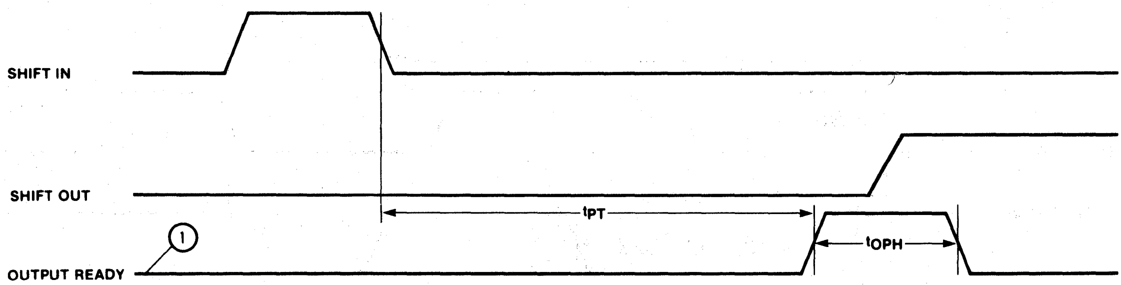
(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.



(1) FIFO initially empty.

Figure 8. t_{PT} and t_{OPH} Specification

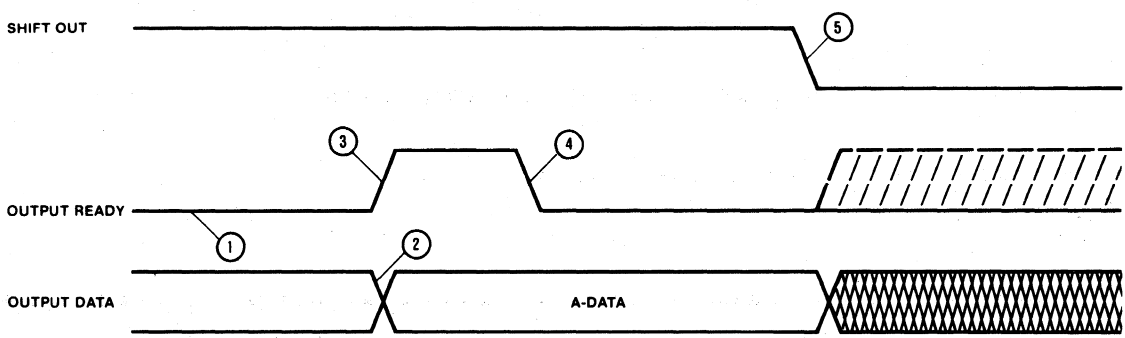


Figure 9. Data is ,Shifted Out Whenever Shift Out and Output Ready are Both HIGH

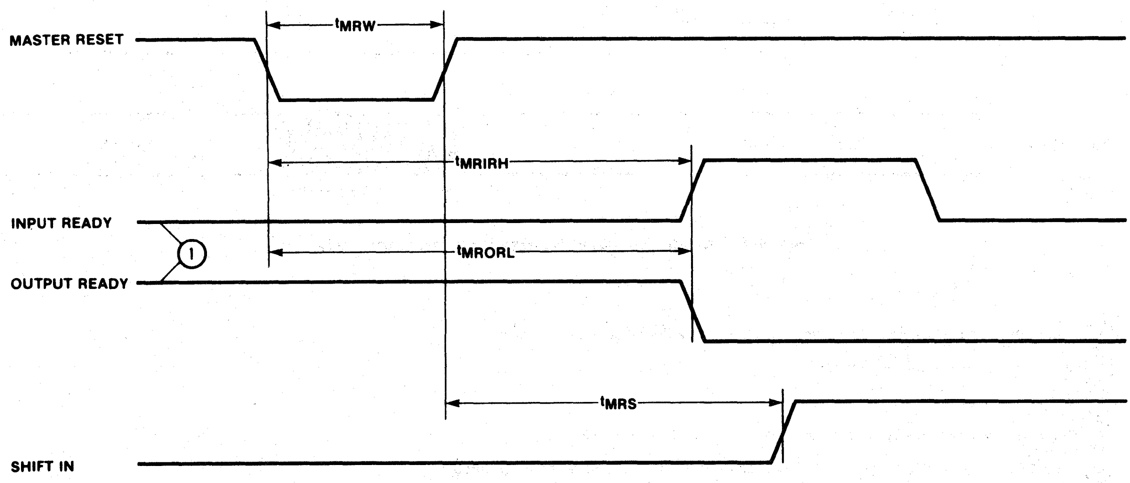
(1) Word 63 is empty.

(2) New data (A) arrives at the outputs (word 63).

(3) Output Ready goes HIGH indicating the arrival of the new data.

(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.

(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



(1) FIFO initially full.

Figure 10. Master Reset Timing

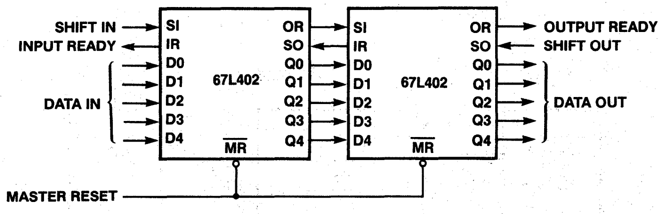


Figure 11. Cascading FIFOs to Form 128x4 FIFO with 67L402's

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

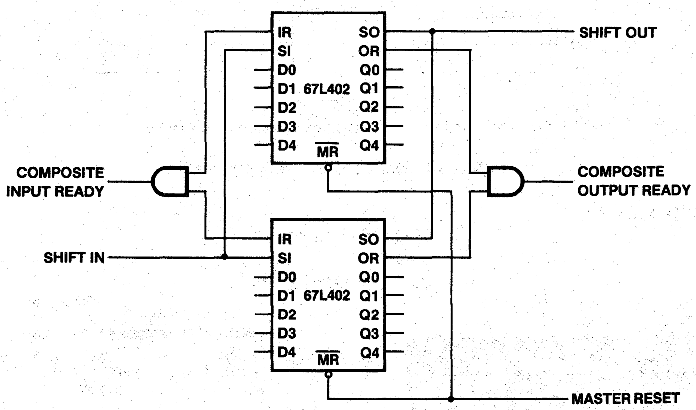


Figure 12. 64x8 FIFO with 67L402's

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 13.

The 67LS402 can also be used in a bidirectional operation as shown in Figure 14.

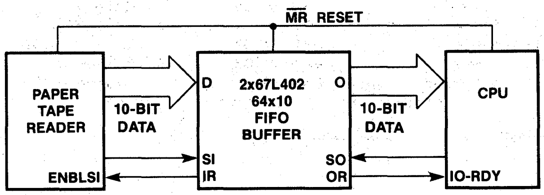
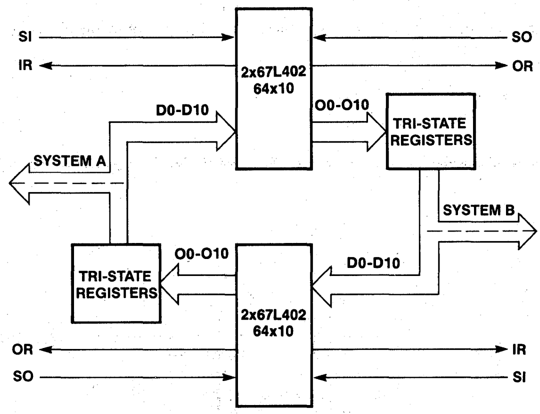


Figure 13. FIFO as Data Buffer Between Slow Steady Rate and Fast 'Burst' Rate

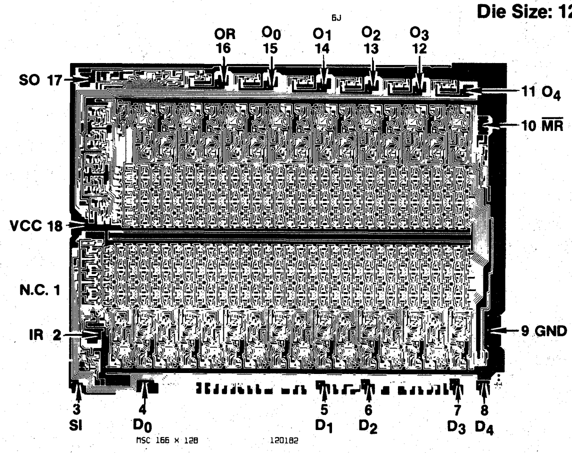


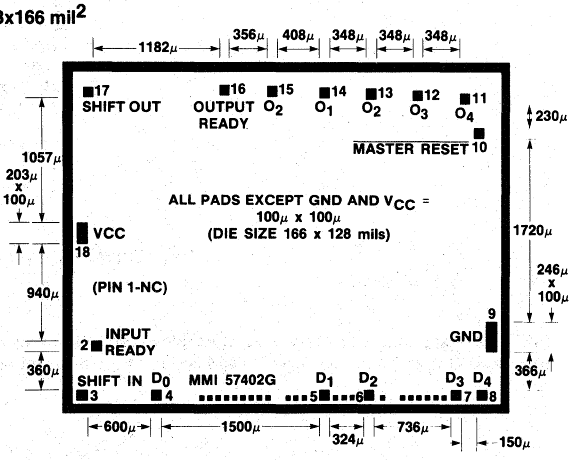
NOTE: Both depth and width expansion can be used in this mode.

Figure 14. Bidirectional FIFO application

Die Configurations

57402 Die Pattern
Step: G
Die Size: 128x166 mil²





First-In First-Out (FIFO) 64x5 Memory 35 MHz (Standalone)

57413A 67413A 67413

Features/Benefits

- **High-speed 35 MHz shift-in/shift-out rates**
- **High-drive capability**
- **Three-state outputs**
- **Half-full and Almost-full/Empty status flags**
- **Structured pinouts. Output pins directly opposite corresponding input pins.**
- **Asynchronous operation**
- **TTL-compatible inputs and outputs**

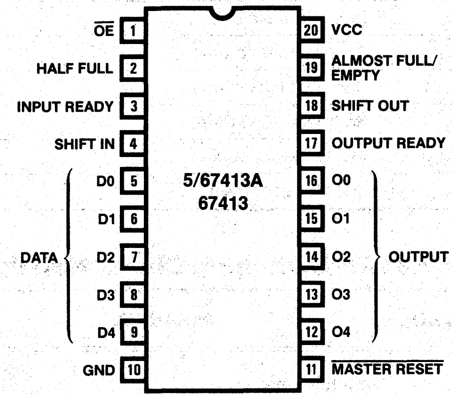
Description

The 5/67413A, 67413 are high-speed, 64x5 First-In-First-Out memories (FIFOs) which operate at 35-MHz input/output rates (67413 operates at 25-MHz in-out). The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive (I_{OL} = 24 mA) data outputs. These devices can be connected in parallel to give FIFOs of any word length. It has a Half-full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main applications of 5/67413A, 67413 are rate buffers; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

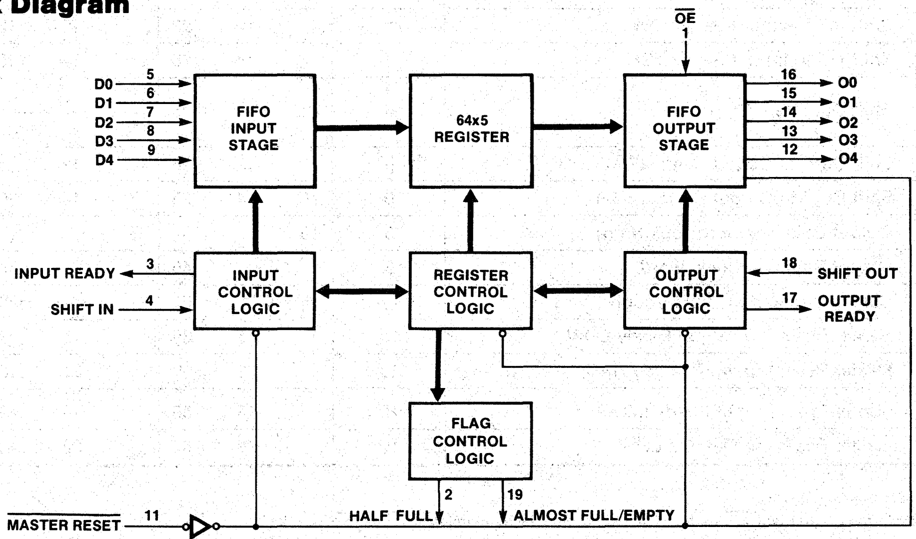
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
57413A	J,W(L28)	Mil	25 MHz-in/out
67413A	J	Com	35 MHz-in/out
57413	J	Com	25 MHz-in/out

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Supply voltage V_{CC} .... −0.5 V to 7 V
Input voltage .... −1.5 V to 7 V
Off-state output voltage .... −0.5 V to 5.5 V
Storage temperature .... −65° to +150°C

5/67413A Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	16			9			ns
t_{SIL}†	Shift in LOW time	1	20			17			ns
t_{IDS}	Input data set up	1	0			0			ns
t_{IDH}	Input data hold time	1	25			15			ns
t_{SOH}†	Shift Out HIGH time	5	16			9			ns
t_{SOL}	Shift Out LOW time	5	20			17			ns
t_{MRW}	Master Reset pulse †	10	35			30			ns
t_{MRS}	Master Reset to SI	10	35			35			ns

5/67413A Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	DC		25	DC DC		††30 †††35	MHz
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		12	28		12	18	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		14	25		14	20	ns
f_{OUT}	Shift Out rate	5	DC		25	DC DC		††30 †††35	MHz
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		12	28		12	18	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	5		14	25		14	20	ns
t_{ODH}†	Output Data Hold (previous word)	5	10			12			ns
t_{ODS}	Output Data Shift (next word)	5			40			34	ns
t_{PT}	Data throughput or "fall through"	4,8		510	750		510	650	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		18	30		18	28	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	10		21	30		21	28	ns
t_{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	30		18	28	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	10		32	55		32	45	ns

Note: Typical is measured 5 V, 25°C.
* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.
† See AC test and high-speed application note.
†† Tested
††† Guaranteed by design (see test load).

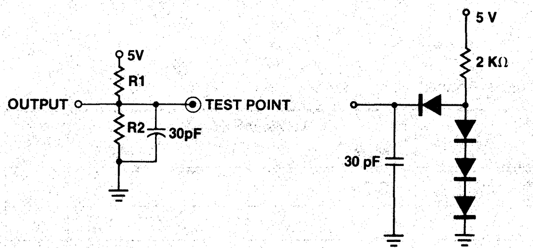
5/67413A Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{IPH}	Input ready pulse HIGH	4	5	12		5	12		ns
t_{OPH}	Output ready pulse HIGH	8	5	12		5	12		ns
t_{ORD}	Output ready ↑ HIGH to Data Valid	5			20			18	ns
t_{AEH}*	Shift Out ↑ to AF/E HIGH	11		100	145		100	135	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	11		450	650		450	600	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	12		450	650		450	600	ns
t_{AFH}*	Shift In ↑ to AF/E HIGH	12		100	145		100	135	ns
t_{HFH}*	Shift In ↑ to HF HIGH	13		280	380		280	360	ns
t_{HFL}*	Shift Out ↑ to HF LOW	13		280	380		280	360	s
t_{PHZ}	Output Disable Delay	A		14	30		14	25	ns
t_{PLZ}		A		14	30		14	25	ns
t_{PZL}	Output Enable Delay	A		14	30		14	25	ns
t_{PZH}		A		24	50		24	38	ns

Note: Input rise and fall time (10%-90%) = 2.5 ns. * See timing diagram for explanation of parameters.

5/67413A/67413

Standard Test Load



Input Pulse Amplitude = 3V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V

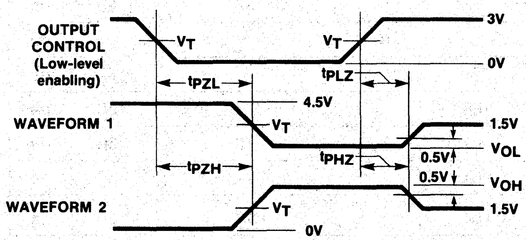


Figure A. Enable and Disable

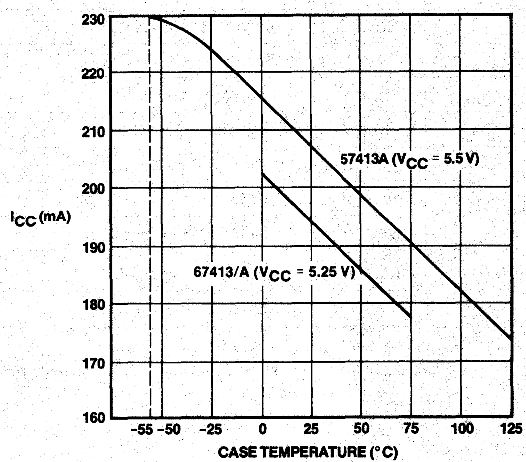
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Design Test Load

I_{OL}	R1	R2
24 mA	200Ω	300Ω
12 mA	390Ω	760Ω
8 mA	600Ω	1200Ω

Typical I_{CC} vs Temperature (V_{CC} = MAX)



Absolute Maximum Ratings

Supply voltage V_{CC}	−0.5 V to 7 V
Input voltage	−1.5 V to 7 V
Off-state output voltage	−0.5 V to 5.5 V
Storage temperature	−65° to +150° C

67413 Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	16			ns
t_{SIL}†	Shift in LOW time	1	20			ns
t_{IDS}	Input data set up	1	0			ns
t_{IDH}	Input data hold time	1	25			ns
t_{SOH}†	Shift Out HIGH time	5	16			ns
t_{SOL}	Shift Out LOW time	5	20			ns
t_{MRW}	Master Reset pulse †	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

67413 Switching Characteristics Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	DC		25	MHz
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		12	28	ns
t_{IRH}†	Shift In ↑ to Input Ready HIGH	1		14	25	ns
f_{OUT}	Shift Out rate	5	DC		25	MHz
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		12	28	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	5		14	25	ns
t_{ODH}†	Output Data Hold (previous word)	5	10			ns
t_{ODS}	Output Data Shift (next word)	5			40	ns
t_{PT}	Data throughput or "fall through"	4,8		510	750	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		18	30	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	10		21	30	ns
t_{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	30	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	10		32	55	ns

Note: Typical is measured at 5 V, 25° C.

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

† See AC test and high-speed application note.

67413 Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{IPH}	Input ready pulse HIGH	4	5	12		ns
t_{OPH}	Output ready pulse HIGH	8	5	12		ns
t_{ORD}	Output ready ↑ HIGH to Data Valid	5			20	ns
t_{AEH}*	Shift Out ↑ to AF/E HIGH	11		100	145	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	11		450	650	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	12		450	650	ns
t_{AFH}*	Shift In ↑ to AF/E HIGH	12		100	145	ns
t_{HFH}*	Shift In ↑ to HF HIGH	13		280	380	ns
t_{HFL}*	Shift Out ↑ to HF LOW	13		280	380	ns
t_{PHZ}	Output Disable Delay	A		14	30	ns
t_{PLZ}		A		14	30	ns
t_{PZL}	Output Enable Delay	A		14	30	ns
t_{PZH}		A		24	50	ns

Note: Input rise and fall time (10%-90%) = 2.5 ns.

* See timing diagram for explanation of parameters.

7

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage							0.8 †	V
V_{IH}	High-level input voltage					2 †			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA					−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45 V					−250	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V					50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V					1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} (Data outputs)	57413A	12 mA			0.5	V
				67413A	24 mA				
			I_{OL} (IR, OR)	5/67413A, 67413	8 mA††				
			I_{OL} (Flag outputs)	5/67413A, 67413	8 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} (Data outputs)	5/67413, 67413	−3.0 mA	2.4			V
			I_{OH} (IR,OR)		−0.9 mA				
			I_{OH} (Flag outputs)		−0.9 mA				
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V			−20		−90	mA
I_{HZ}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V					+20	μA
I_{LZ}		V_{CC} = MAX	V_O = 0.4 V					20	μA
I_{CC}	Supply current	V_{CC} = MAX. Inputs low, outputs open (5/67413A/67413)						**240	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

** See curve for I_{CC} vs. temp.

† There are absolute voltages with respect to GND (PIN 8 or 9) and includes all overshoots due to test equipment.

†† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a funcitonal standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-ingoing HIGH. This same type of problem is also related to T_{IRH}, T_{ORL} and T_{ORH} as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

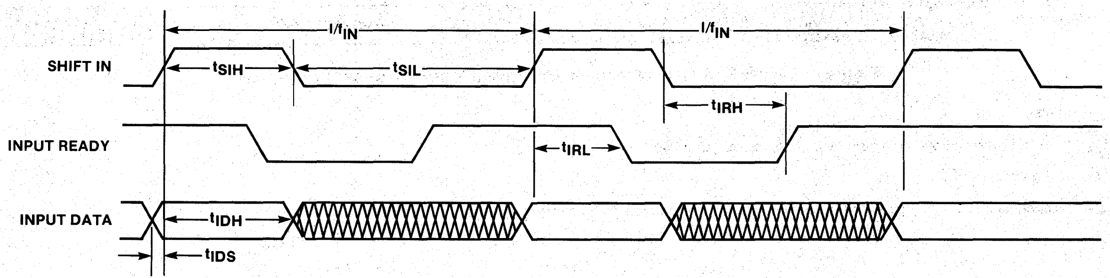


Figure 1. Input Timing

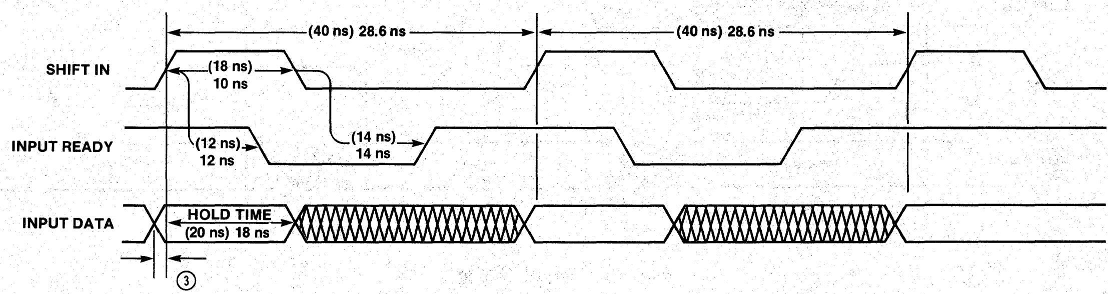


Figure 2. Typical Waveforms for (25) 35 MHz Shift-In Data Rate [(57413A) 67413A]

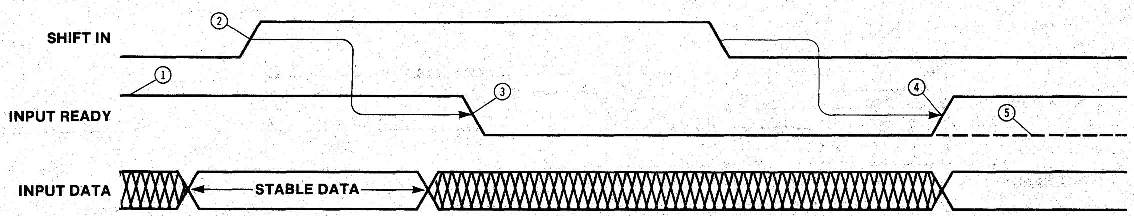


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
(5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

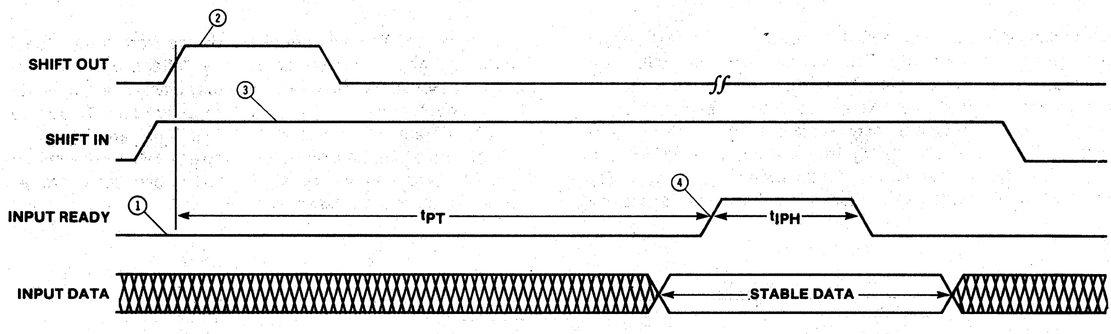


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.

(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.

(3) Shift In is held HIGH

(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

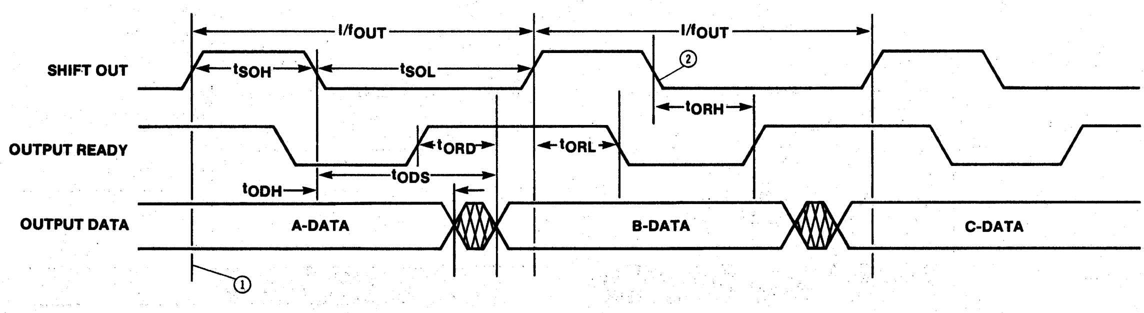


Figure 5. Output Timing

(1) The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

(2) Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

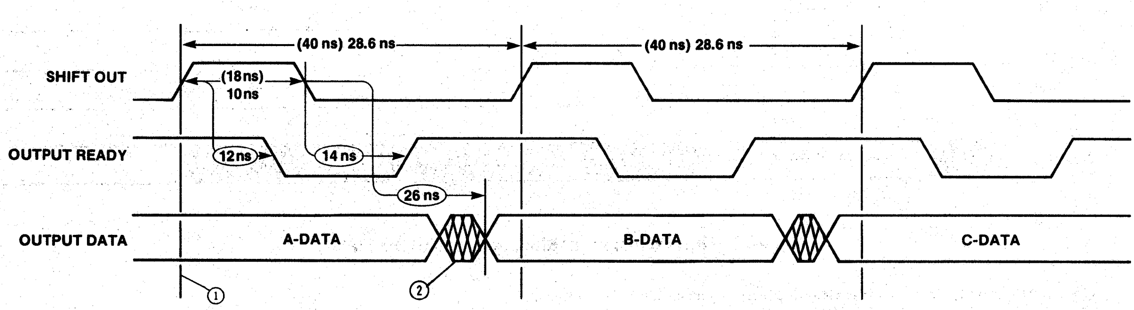


Figure 6. Typical Waveforms for (25) 35 MHz Shift-Out Data Rate (57413A) 67413A

(1) The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

(2) Data in the first crosshatched region may be A or B Data.

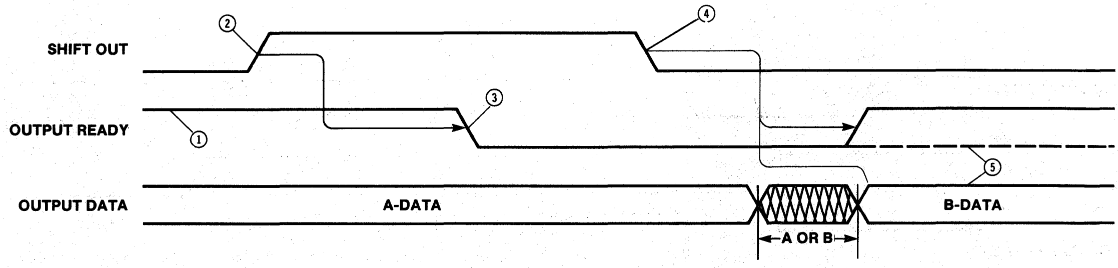


Figure 7. The Mechanism of Shifting Data Out of the FIFO

1. Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
2. Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
3. Output Ready goes LOW.
4. Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
5. If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

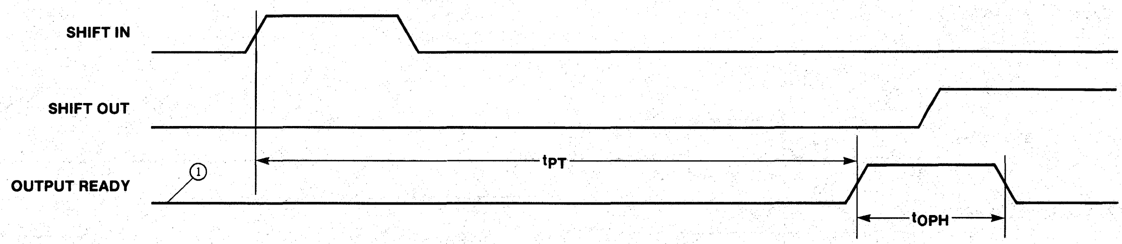


Figure 8. t_{PT} and t_{OPH} Specification

1. FIFO initially empty.

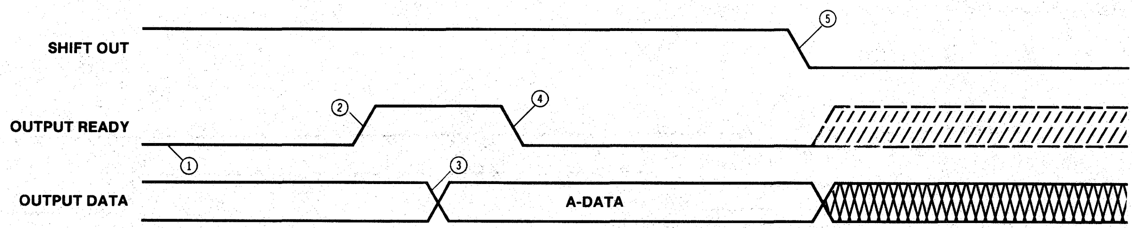


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

1. Word 63 is empty.
2. Output Ready goes HIGH indicating arrival of the new data.
3. New data (A) arrives at the outputs (word 63).
4. Since Shift Out is held HIGH, Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

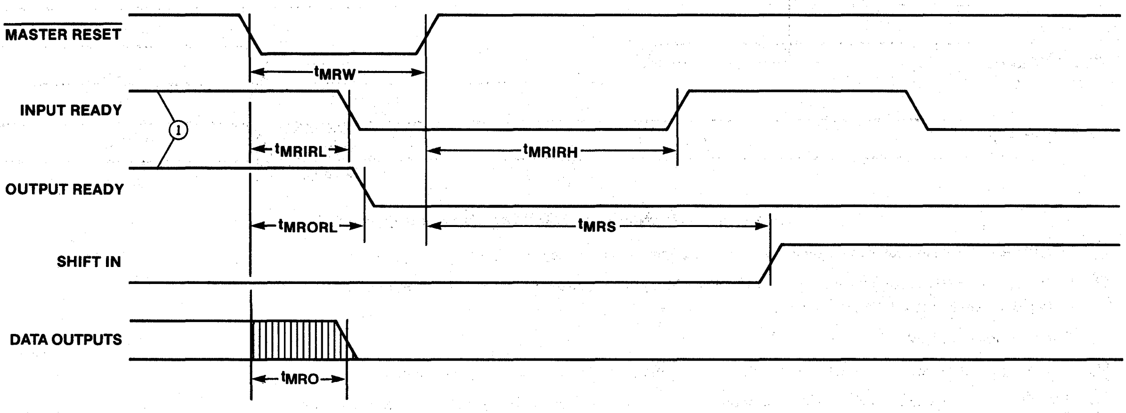


Figure 10. Master Reset Timing

(1) FIFO is partially full.

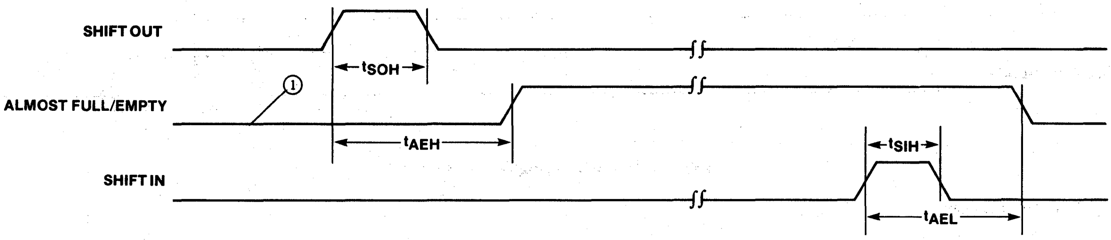


Figure 11. t_{AEH}, t_{AEL} Specifications

(1) FIFO contains 9 words (one more than almost empty).

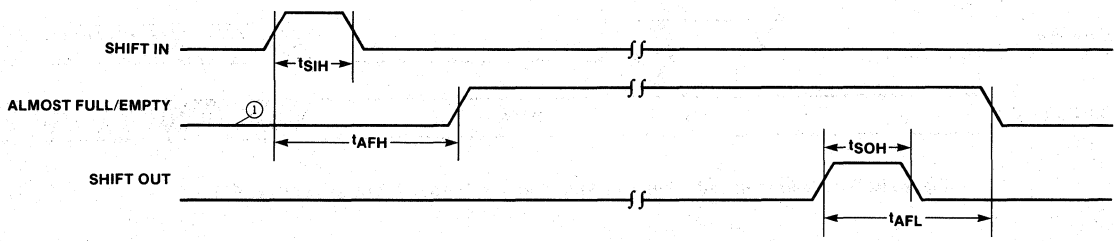


Figure 12. t_{AFH}, t_{AFL} Specifications

(1) FIFO contains 55 words (one short of almost full)

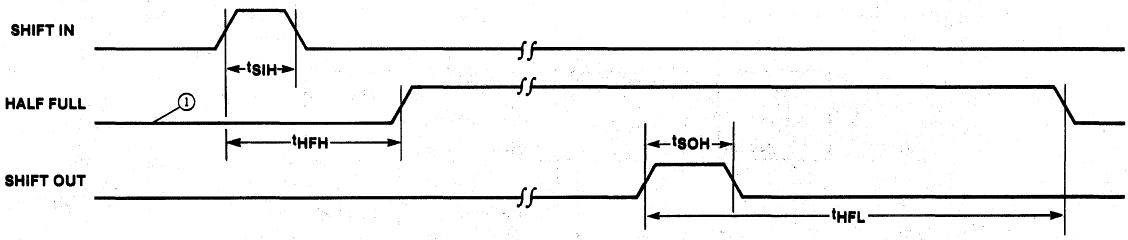


Figure 13. t_{HFL}, t_{HFH} Specifications

① FIFO contains 31 words (one short of half full).

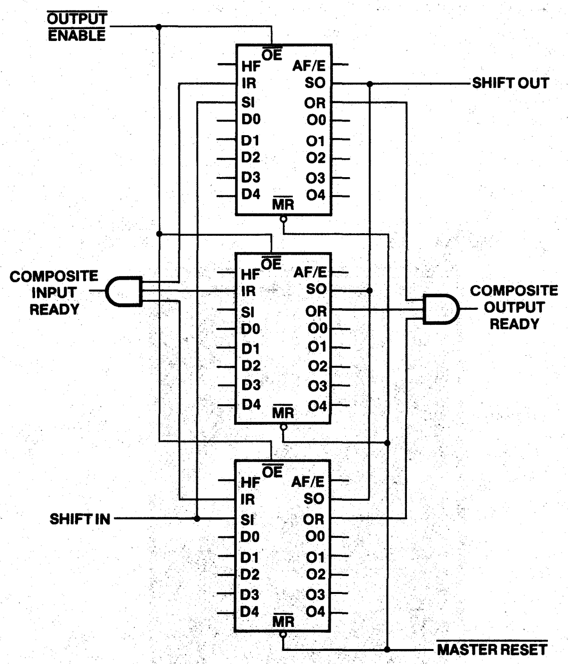


Figure 14. 64x15 FIFO with 5/67413A/67413

FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall through times of the FIFOs.

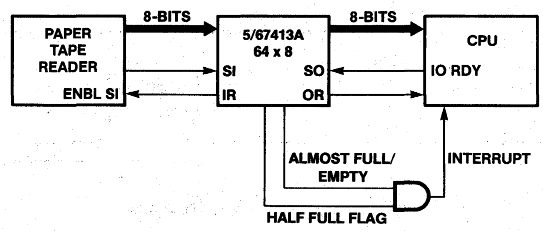
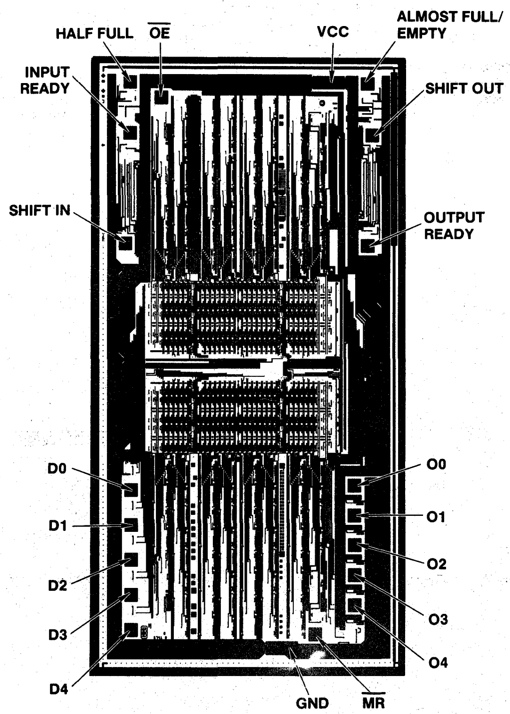


Figure 15. Application for 5/67413A "Slow and Steady Rate to Fast 'Blocked Rate' "

Note: Cascading the FIFO's in word width is done by ANDing the IR and OR as shown in Figure 14.

Die Configuration



Serializing First-In-First-Out (FIFO) 64x8/9 Memory
67417

Features/Benefits

- High-speed 28-MHz serial shift-in/shift-out rate
- 10-MHz parallel shift-in/shift-out rate
- Three-state outputs with Hi-current drive
- Cascadable at parallel port only
- Half-full flag (32 or more)
- Selectable 64x8 or 64x9 FIFO configuration thus providing "frame mark bit"

Typical Applications

- LAN equipment
- Data communication
- Office automation
- Microcomputers
- Minicomputers
- Disk/tape controllers

Description

The 67417 is a serializing/deserializing FIFO. This FIFO, the first one of its type in the industry, is organized 64 words x 8/9 bits wide. Like traditional Monolithic Memories' FIFOs it is cascadable, but only at the parallel port.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE	DESCRIPTION
67417	J	Com	64x9

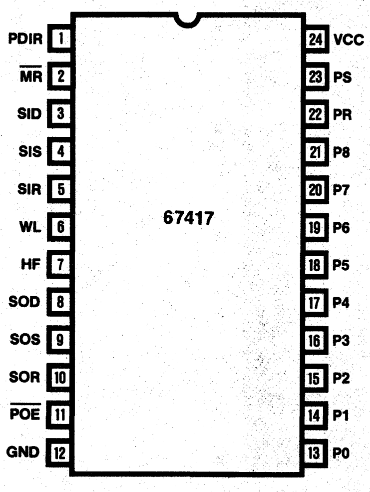
In addition, the device has the ability to connect directly to a system bus. These features make it a complete "sub-system on a chip."

The FIFO basically has three modes of operation;

1. Serial in to parallel out
2. Parallel in to serial out
3. Serial in to serial out (requires non-standard logic level on PDIR).

In the first mode, serial data can be accepted at up to 28 MHz and the FIFO outputs parallel data at up to 10 MHz. Similarly, in the alternate mode parallel data can be transformed into serial data. Please refer to appendix for detailed description.

Pin Configuration



Pin Names

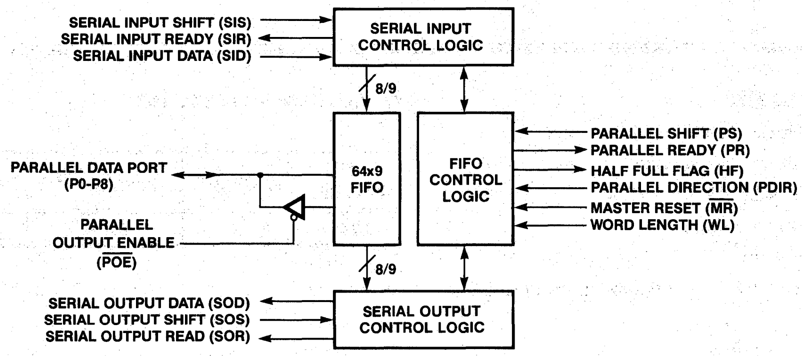
P0-P8	Parallel Data
PS	Parallel Shift In/Out
PR	Parallel Input/Output Ready
$\overline{POE}$	Parallel Output Enable
SID	Serial Input Data
SIS	Serial Input Shift
SIR	Serial Input Ready
SOD	Serial Output Data
SOS	Serial Output Shift
SOR	Serial Output Ready
PDIR	Parallel Port Direction
WL	Word Length
$\overline{MR}$	Master Reset
HF	Half Full Flag
VCC	VCC
GND	Ground

NOTE: Please call Monolithic Memories for introduction dates.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

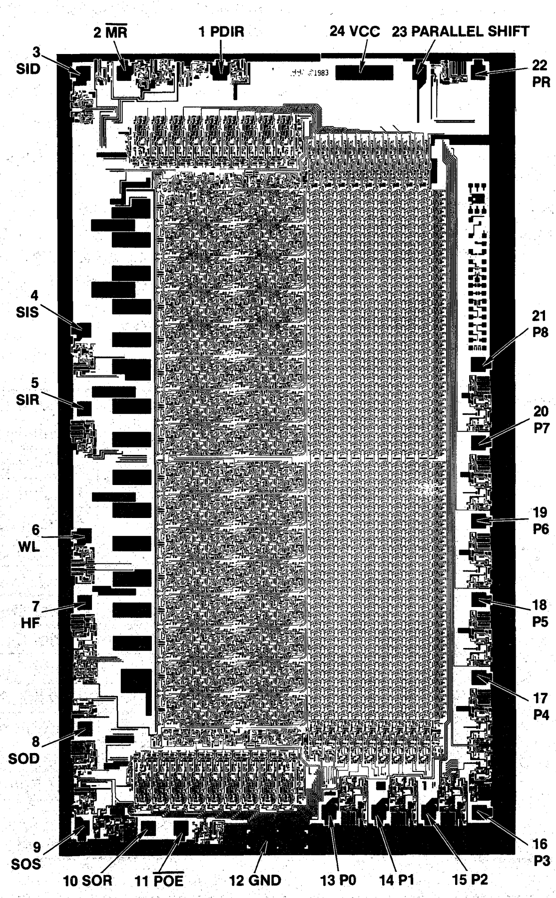
Monolithic Memories

Block Diagram



Die Configuration

Die size = 162x269 mils



Absolute Maximum Ratings

Supply voltage V_{CC} .... −0.5 V to 7 V
Input voltage .... −1.5 V to 7 V
Off-state output voltage .... −0.5 V to 5.5 V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
	SERIAL INPUT PARAMETERS					
f_{SIN}	Max. Serial Shift-In Rate	1			28	MHz
t_{SISH}	Serial Shift-In HIGH time	1	23			ns
t_{SISL}	Serial Shift-In LOW time	1	12			ns
t_{SIDS}	Serial Input Data Setup time	1	14			ns
t_{SIDH}	Serial Input Data Hold time	1	0			ns
t_{SIRHS}	Recovery Time Serial Input Ready ↑ to Serial Input Shift ↑	1	0			ns
	SERIAL OUTPUT PARAMETERS					
f_{SOUT}	Max. Serial Shift-Out Rate	1			28	MHz
t_{SOSH}	Serial Shift-Out HIGH time	3	15			ns
t_{SOSL}	Serial Shift-Out LOW time	3	15			ns
t_{ORHS}	Recovery time Serial Output Ready ↑ to Serial Output Shift ↑	3	5			ns
	WORD LENGTH PARAMETERS					
t_{SWL}	Setup SIS, SOS	1,3	18			ns
t_{HWL}	Hold SIS, SOS	1,3	3			ns
	PARALLEL PORT PARAMETERS					
f_P	Parallel shift-in/shift-out rate	8			10	MHz
t_{PSH}	Parallel Shift-In/Out HIGH time	5/8	30			ns
t_{PSL}	Parallel Shift-In/Out LOW time	5/8	30			ns
t_{PIDS}	Parallel Input Data Setup time	5	-5			ns
t_{PIDH}	Parallel Input Data hold time	5	35			ns
t_{PDIRSL}	Shift LOW to parallel direction transition	14	50			ns
t_{PDIRSH}	Parallel direction transition to Shift HIGH	14	50			ns
t_{PRHS}	Parallel Ready ↑ to Parallel Shift Low	10/11	30			ns
	MASTER RESET PARAMETER					
t_{MRW}	Master Reset LOW time	12/13	40			ns

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
	SERIAL INPUT PARAMETERS					
t_{SIRL}	Serial Input Shift ↑ to Serial Input Ready LOW	2			23	ns
t_{SIHFH}	Serial Input Shift ↑ to Half-Full Flag HIGH	7			1.3	μs
	SERIAL OUTPUT PARAMETERS					
t_{SORL}	Serial Output Shift ↑ to Serial Output Ready LOW	4			23	ns
t_{SOD}	Serial Output Shift ↑ to Serial Output data	3			23	ns
t_{ODRH}	Serial Output Data valid to Serial Output Ready HIGH	3	0	25		ns
t_{SOHFL}	Serial Output Shift ↑ to Half-Full LOW	7			1.3	μs
	PARALLEL INPUT/OUTPUT PARAMETERS					
t_{PSPRL}	Parallel Shift ↑ to Parallel Ready LOW	5/8			65	ns
t_{PSPRH}	Parallel Shift ↓ to Parallel Ready HIGH	5/8/10			80	ns
t_{PSHFH}	Parallel Shift-In ↓ to Half-Full HIGH	6			1.3	μs
t_{PSHFL}	Parallel Shift-Out ↓ to Half-Full LOW	9			1.3	μs
	PARALLEL OUTPUT PARAMETERS					
t_{PODH}	Minimum Parallel Shift ↓ to Ouput data	8	20			ns
t_{POD}	Maximum Parallel Shift ↓ to Output data	8			60	ns
t_{PODV}	Minimum Output data valid to parallel ready HIGH	8	0	15		ns
	OTHER PARAMETERS					
t_{PT}	Fall-through time	10/11/16/17			2.6	μs
t_{IPH}	Parallel Input Ready pulse HIGH	11	30			ns
t_{OPH}	Parallel Output Ready pulse HIGH	10	30			ns
t_{MRO}	$\overline{\text{Master Reset}}$ ↓ to Data Out LOW	12			65	ns
t_{MRSIRL}	$\overline{\text{Master Reset}}$ ↓ to Serial Input Ready LOW	12			40	ns
t_{MRSIRH}	$\overline{\text{Master Reset}}$ ↑ to Serial Input Ready HIGH	12			40	ns
t_{MRPRL}	$\overline{\text{Master Reset}}$ ↓ to Parallel Ready LOW	12/13			40	ns
t_{MRPRH}	$\overline{\text{Master Reset}}$ ↑ to Parallel Ready HIGH	13			30	ns
t_{MRSORL}	$\overline{\text{Master Reset}}$ ↓ to Serial Output Ready LOW	13			40	ns
t_{MRHFL}	Master Reset ↓ to Half-Full LOW	12/13			60	ns
t_{PDIROR}	Parallel Direction change to new Output Ready	14			60	ns
t_{PDIROD}	Parallel Direction change to Output data valid	14			60	ns
t_{PDIRPZ}	Parallel Direction change to Parallel Output data Hi-Z	14			35	ns
t_{PDIRSZ}	Parallel Direction changes to Serial Output-data Hi-Z	14			80	ns
t_{PZX}	Output enable time $\overline{\text{POE}}$ to P0-8	15			30	ns
t_{PXZ}	Output disable time $\overline{\text{POE}}$ to P0-8	15			35	ns

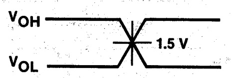
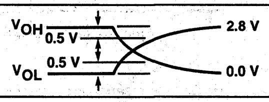
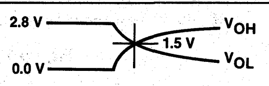
Electrical Characteristics Over Operating Conditions

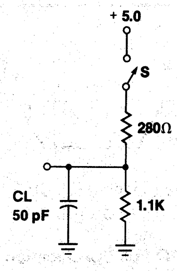
SYMBOL	PARAMETER	TEST CONDITIONS				COM MIN	COM TYP	COM MAX	UNIT
V_{IL}	Low-level input voltage							0.8†	V
V_{IH}	High-level input voltage					2†			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA					−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V					−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V					0.1	mA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V					0.4	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Data Outputs P0-P8, SOD	I_{OL} = 24 mA	0-80°C			0.58	V
					25°C			0.55	
				I_{OL} = 16 mA	0-80°C			0.5	
			All other outputs	I_{OL} = 8 mA				0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3 mA			2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V			−20		−90	mA
I_{LZ}	Off-state output current* SOD P0 to P8	V_{CC} = MAX	V_O = 0.4 V					−100	μA
I_{HZ}			V_O = 2.4 V					100	mA
I_{CC}	Supply current	V_{CC} = MAX						350	mA
O_V	PDIR non-standard over voltage	Serial-In, Serial-Out				10		16	V

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

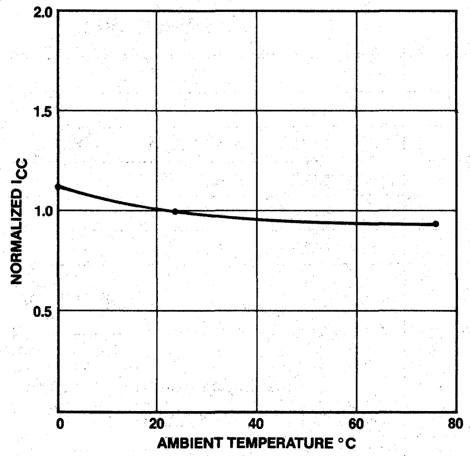
† This is an absolute voltage with respect to device GND (pin 12) and includes all overshoots due to test equipment.

Test Waveforms

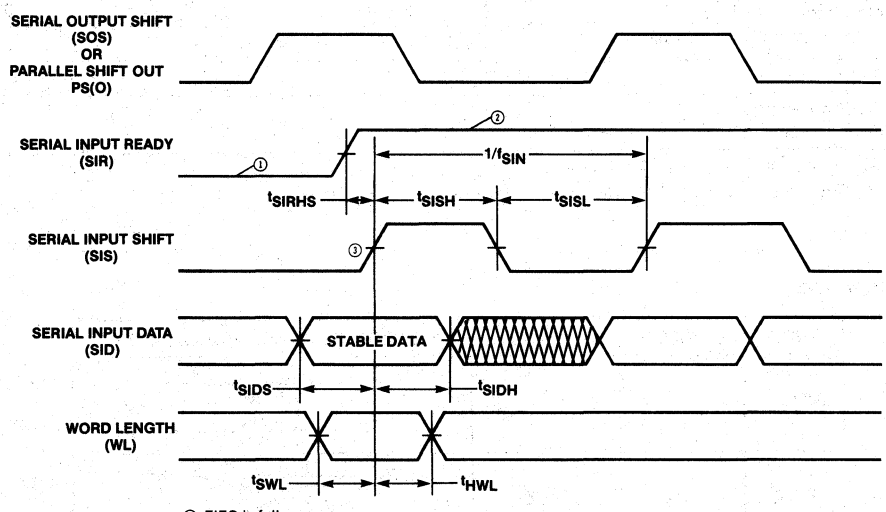
TEST	S = OPEN	S = CLOSED	OUTPUT WAVEFORM-MEAS-LEVEL
All t_{PD}		All t_{PD}	
t_{PXZ}	t_{PHZ}	t_{PLZ}	
t_{PZX}	t_{PZH}	t_{PZL}	



I_{CC} VS Temperature

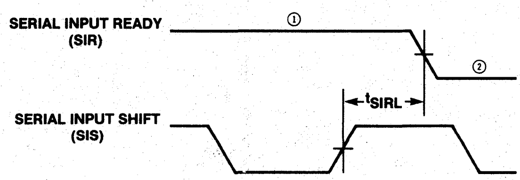


Definition of Waveforms



① FIFO is full.
② Shift-out (serial or parallel) is asserted, SIR goes High.
③ SIS can be asserted t_{SIRHS} after serial input ready changes from low-to-high.

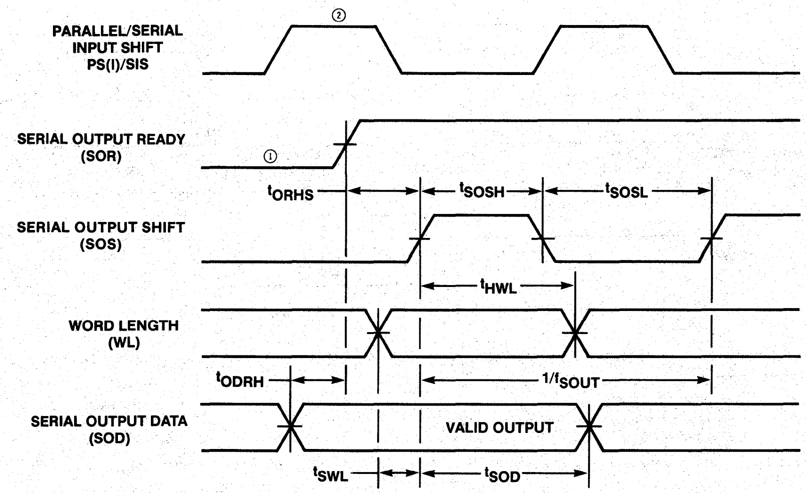
Figure 1. Serial Input Timing



① FIFO is not full.
② FIFO is full.

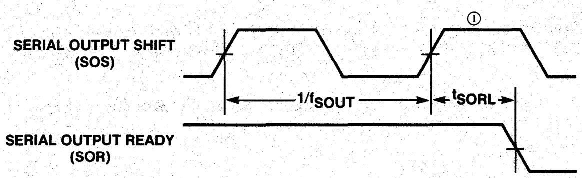
Figure 2. FIFO Full Specification (t_{SIRL})

Definition of Waveforms (cont'd)



① FIFO is empty, output ready remains Low and shift-out cannot be applied.
② After a word is shifted in, output ready goes High and shift-out can be applied.

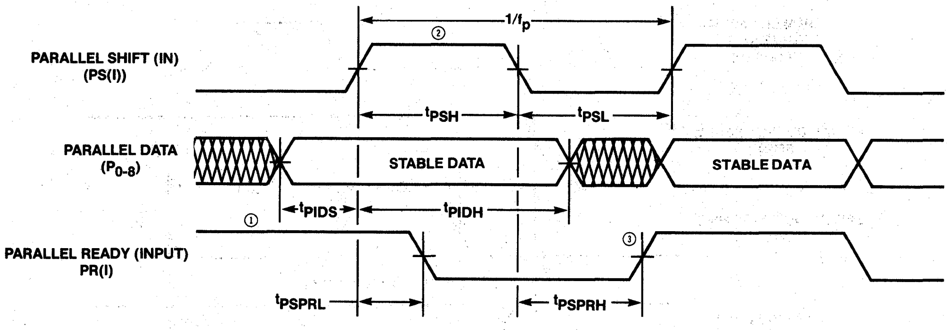
Figure 3. Serial Output Timing



① After the last shift-out, output ready goes Low indicating FIFO is empty.

Figure 4. FIFO Empty Specifications (t_{SORL})

Definition of Waveforms (cont'd)



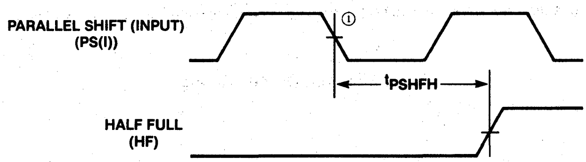
NOTE: P_{DIR} = High for the mode parallel-in to serial-out. Parallel ready is an output flag from the FIFO indicating that a word can be loaded into the FIFO.

① FIFO is not full and ready for input.

② PS (In) is asserted, shifting in parallel data P0-8.
PR (In) goes Low indicating parallel port is in use and no longer ready.
PR (In) will remain Low as long as PS (In) remains High.

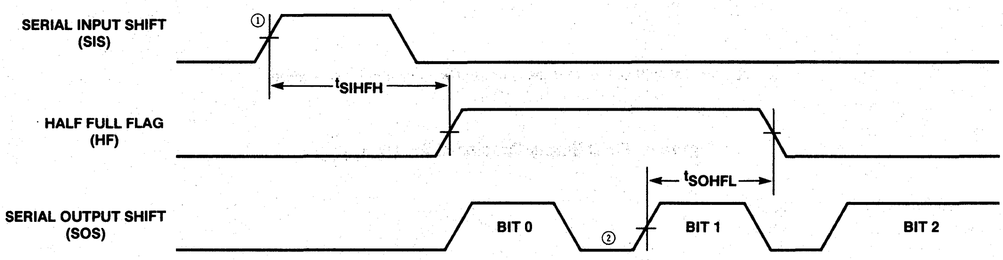
③ PS (In) has gone Low, allowing recent word to propagate through FIFO, PR (In) returns High when ready for more input.

Figure 5. Parallel Input Shift Timing



① for P_{DIR} = High, the direction is parallel-in to serial-out. After the 32nd shift-in, the half-full flag is set to High, and remains High, indicating the presence of 32 or more words.

Figure 6. Half-full Flag Specifications on Parallel (t_{PSHFH})

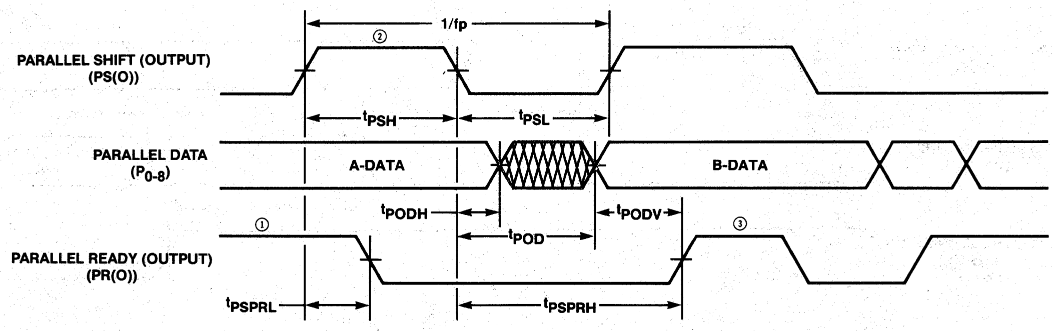


① When there are 31 words in the FIFO, the next shift-in on the 32nd word sets the half-full flag (HF) High indicating that there are 32 or more words.

② As soon as one word is partially shifted out, HF goes Low indicating there are less than 32 words.

Figure 7. Half-full Flag Specification on Serial Operation (t_{SIHFH}, t_{SOHFL})

Definition of Waveforms (cont'd)



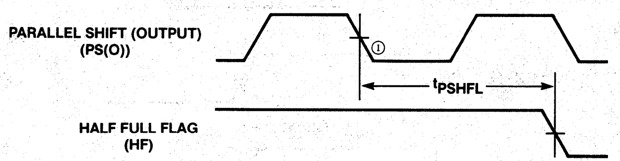
NOTE: For above conditions P_{DIR} = Low indicating that the direction is from serial-in to parallel-out. Thus parallel ready indicates the output status.

① FIFO is not empty and at least one word is valid and ready at P0-8 outputs.

② PS (Out) is asserted, shifting out parallel data. Data remains valid, but:
PR (Out) goes Low to indicate parallel port is in use and no longer ready.
PR (Out) will remain Low as long as PS (Out) remains High.

③ PS (Out) has gone Low, allowing data word to be shifted out. Next data word appears at output and PR (Out) is asserted to indicate valid data ready.

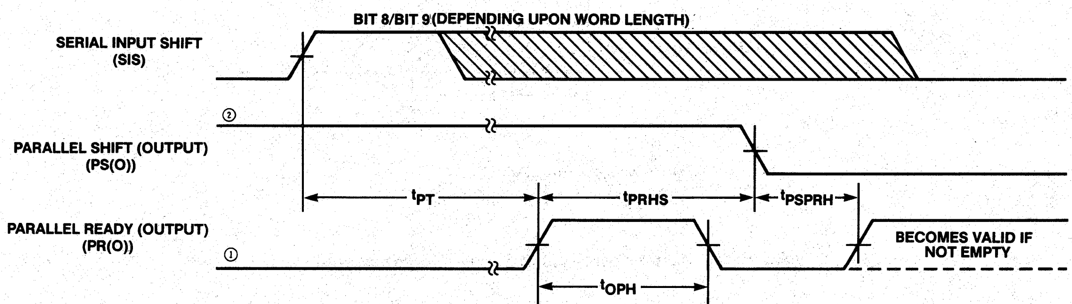
Figure 8. Serial-in to Parallel-out Specifications (t_{POD}, t_{PODH}, t_{ODV})



NOTE: For P_{DIR} = Low the direction is serial-in to parallel-out.

① When a word is shifted out and the half-full flag goes Low, 31 words or less are in the FIFO.

Figure 9. Half-full Flag Specification on Parallel Shift-out (t_{PSHFL})



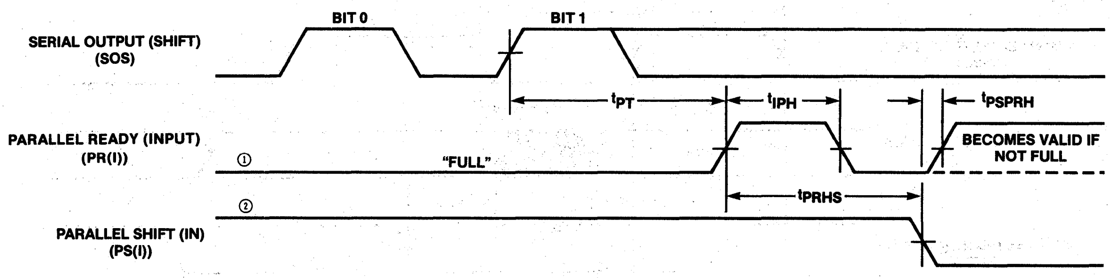
NOTE: P_{DIR} = Low indicating serial-in to parallel-out.

① FIFO initially empty.

② PS (Out) held High.

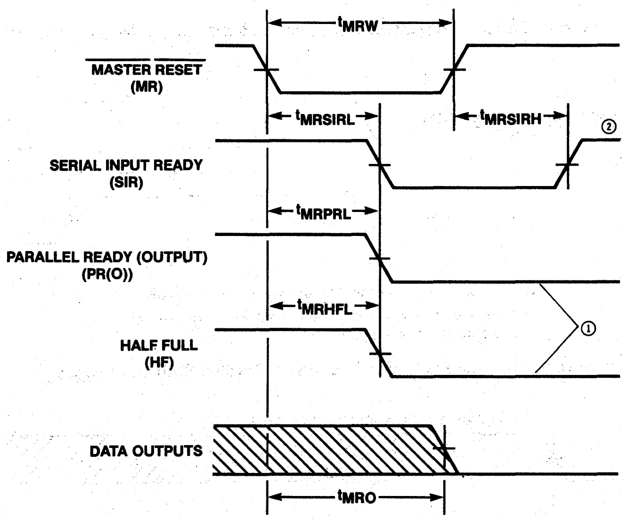
Figure 10. t_{PSPRH}, t_{PT}, t_{POH} Specifications (Serial Input Mode)

Definition of Waveforms (cont'd)



NOTE: P_{DIR} = High (parallel-in to serial-out).
① FIFO is full.
② PS (I) held High.

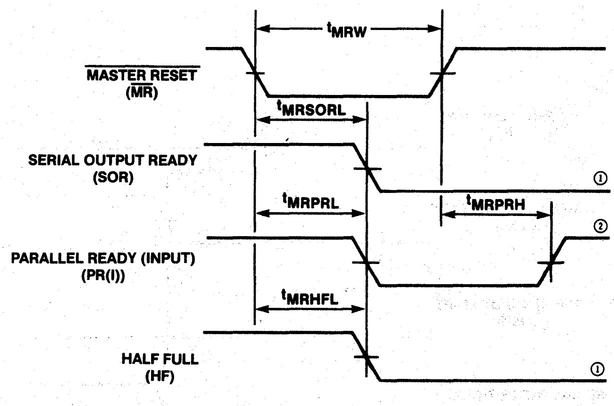
Figure 11. Fall-through Specifications



NOTE: P_{DIR} = Low.
① PR (O) and HF go Low.
② After $\overline{MR}$ goes High, SIR goes High.

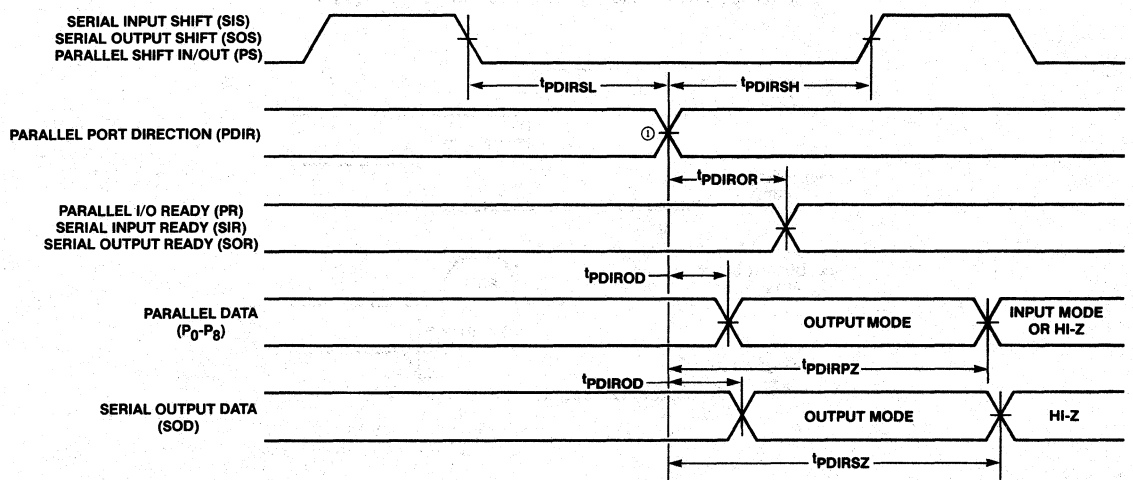
Figure 12. Master Reset Timing Serial-in to Parallel-out

Definition of Waveforms (cont'd)



NOTE: P_{DIR} = High.
① SOR and HF go Low.
② Affter $\overline{MR}$ goes High, PR(I) goes High.

Figure 13. Master Reset Timing (Parallel-in to Serial-out)



NOTE: When the FIFO is used as a stack, change the port direction before the FIFO is full; otherwise, data may be lost.

Figure 14. P_{DIR} Transition Parameters

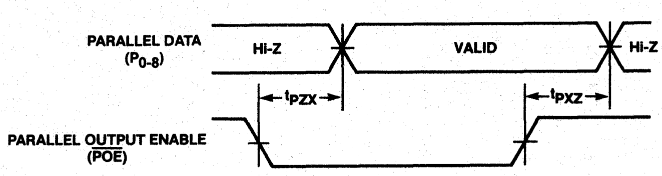


Figure 15. Parallel Port Enable and Disable Timing

Definition of Waveforms (cont'd)

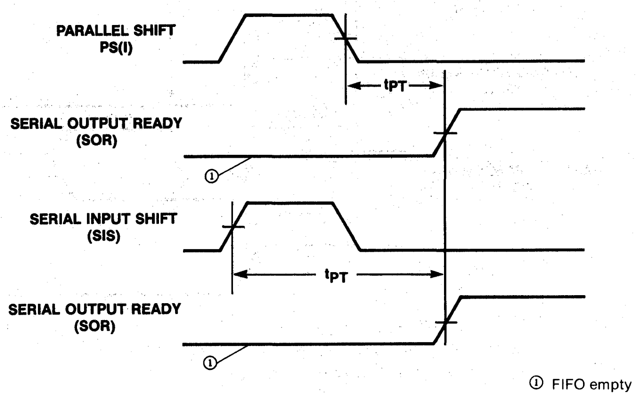


Figure 16. t_{PT} Specification (Shift-in to Serial Output Ready)

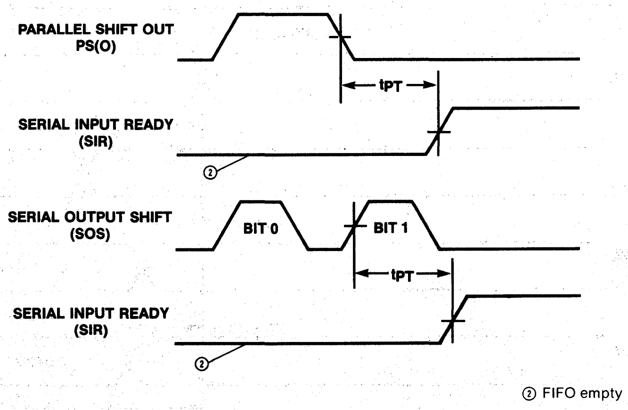


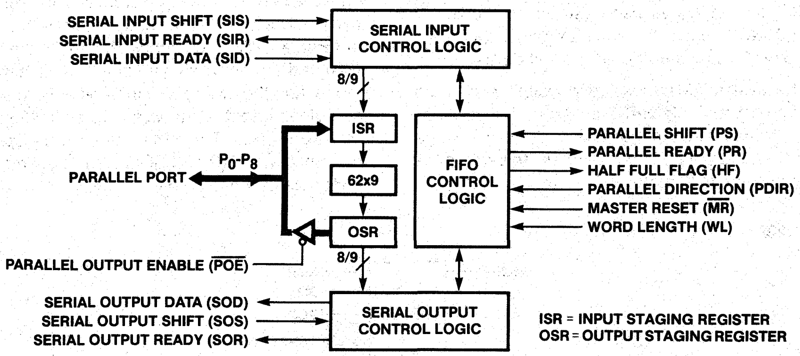
Figure 17. t_{PT} Specification (Shift-in to Serial Input Ready)

Appendix
Detailed Functional/Description for 67417

The 67417 is a serializing FIFO intended as a one-chip solution for data buffering and serializing/deserializing. It can be successfully used for interfacing parallel-format computing equipment to serial-format data communications and mass-memory equipment.

Parallel Port

This is a fully bidirectional port, and it operates at a more conservative data rate of 10 MHz. The input-staging register (ISR) internally controls the parallel input data port bus signals. Likewise the OSR internally controls the parallel output data port. The ISR data outputs drive the parallel data inputs to the cell array, and the OSR inputs are likewise driven by the final parallel data stage of the cell array



Basically the major internal subsystems of the 67417 are:

(i) The serial input port
(ii) The serial output port
(iii) The parallel port
(iv) The FIFO control logic and
(v) The cell array

Serial Port

The two serial ports (input and output) are entirely separate which allows a high-speed data rate of 28 MHz. These serial ports do not share data pins, control pins, or internal circuits. However, since the serial output data is a three-state output, the serial data ports could be connected together in the normal serial-parallel operation mode with separate SOR and SIR status signals.

The serial input port interface consists of the Serial Input Ready (SIR) output, Serial Input Data (SID) input, and the Serial Input Shift (SIS) clock input. Unlike the analogous SI and IR signals on the 67401/2, SIS and SIR do not accomplish a "handshake" with the rest of the logic of the system which incorporates the 67417; rather SIR is asserted whenever the 67417 is still capable of receiving at least one more bit. SIS is a positive edge-triggered input which sequences the serial input control logic. This logic in turn controls SIR and the 8/9-bit Input Staging Register (ISR).

The serial output port interface is the dual of the above, with a Serial Output Data (SOD) output, a Serial Output Shift (SOS) clock input, and a Serial Output Ready (SOR) status output. SOR is asserted whenever at least one more bit is available at the output. SOS is a positive edge-triggered input which sequences the 8/9-bit Output Staging Register (OSR). Serial Output Data is automatically three-stated whenever the serial output port is disabled (during Master Reset) and PDIR = Low. The parallel port is controlled by Parallel Shift (PS) input and Parallel Direction Input (PDIR). Parallel Ready (PR) is the handshake/status output. At the Parallel Port PS and PR *do* accomplish a handshake with the outside world as SI, IR, SO and OR on the 67401/2.

Modes of Operation

There are three modes in which the 67417 can operate

(i) Parallel-in to serial-out
(ii) Serial-in to parallel-out and
(iii) Serial-in to serial-out.

In the parallel-in to serial-out mode, PDIR = HIGH. Thus Parallel Shift (PS) acts as a Shift In (SI) and similarly, Parallel Ready (PR) as Input Ready (IR).

Similarly for serial-in to parallel-out mode, PDIR = LOW, and Parallel Shift (PS) acts as a Shift Out (SO) and Parallel Ready (PR) as Output Ready (OR).

If the direction mode for a particular application of the 67417 is not intended to change during system operation, the PDIR input should be strapped to a logic LOW or HIGH.

In the serial-in to serial-out mode, PDIR = 10 V minimum.

The parallel port does not function during this mode and is three-stated. The direction operating mode should not be changed if the FIFO is FULL otherwise stored data will be lost.

Cell Array

The 67417 cell array can function *either* as a 64x8 FIFO (with the 9th bit padded to a zero) or as a 64x9 FIFO, according to the setting of the word length (WL) control input. Like the PDIR control input, WL can be switched at electronic speeds during system operations; but if the word length of a particular 67417 is *never* to change during system operation, WL for that part can be strapped to ground or V_{CC}.

It is a permissible 67417 mode of operation to almost fill the FIFO (there should be at least two empty locations) with WL set to 8-bit operation, then switch WL to 9-bit operation (WL = HIGH) to load one more word plus a frame marker in the last bit, and then switch PDIR and unload the 67417 in a 9-bit mode. This sequence of operations has the effect of providing a "frame marker bit" in the ninth bit of the last word loaded. The corresponding 9th bits will have been zeroed by the 67417 internal logic for all the other words in the frame since they were loaded while the 67417 was operating as an 8-bit device.

It is, however, the system designer's responsibility to avoid changing PDIR inputs when only part of an 8- or 9-bit word has been received or transmitted. In general, if such a change occurs, the part in general will try to add zero bits to pad out the impacted word to assume full length.

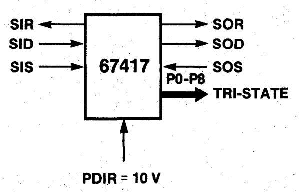
Half-Full Flag

This status output indicates when the 67417 statically contains 32 words or more. This provides an indication to send in more data if the device is operated in a mostly-empty mode or send out more data if the 67417 is operated in a mostly-full mode.

Cascading

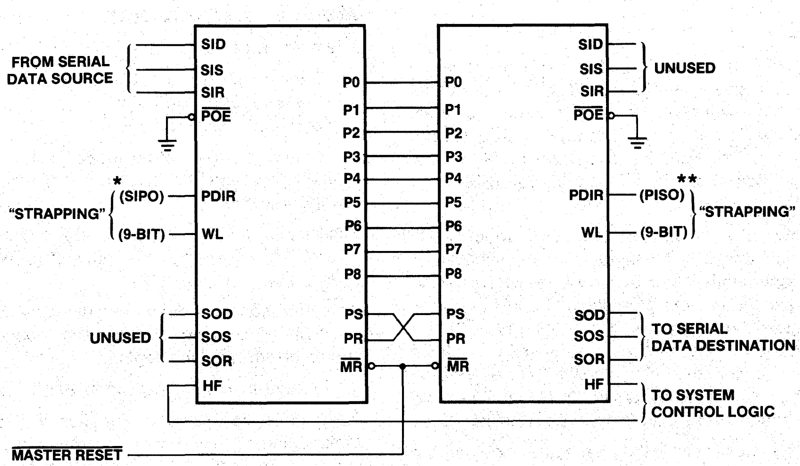
The 67417 is designed to be cascaded at the parallel port only, due to very high data transfer rates at the serial ports. Cascading two 67417's is accomplished by connecting Parallel Input/Output Ready (PR) of each part to control the Parallel Shift In/Out (PS) of the other part, with one FIFO in serial-in to parallel-out mode, and the other FIFO in parallel-in to serial-out mode. The combined effect of this is a reversible 128x8 or 128x9 serial-in serial-out FIFO. The 67417 can not be cascaded at the serial ports because SIR and SOR are not acknowledged signals but rather status signals only.

Applications



NOTE: It can shift in data serially in the multiples of 8- or 9-bit according to WL.

Figure 18. 512/576x1 Serial-in to Serial-out Mode



* SIPO = Serial-in to Parallel-out.
** PISO = Parallel-in to Serial-out.

Figure 19. Cascading of Two 'S417s for Serial-in to Serial-out Operation as a 128x9 (1152x1) FIFO

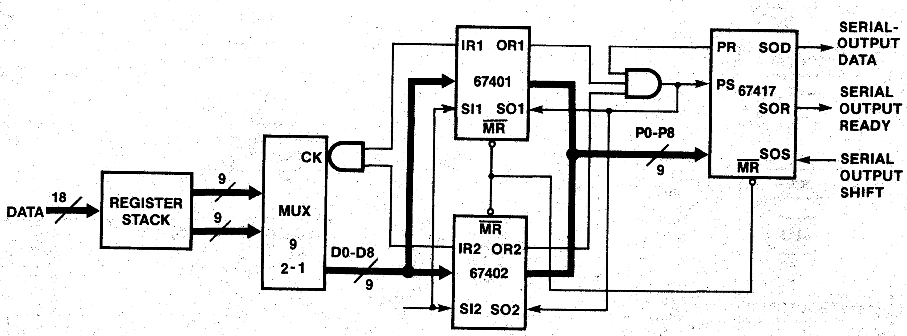


Figure 20. An Example of an Expansion Scheme for a 64x18 Parallel-to-Serial FIFO

An 18-bit data word is multiplexed into the two 67401/2 FIFOs. Since the 67417 FIFO is cascadable at the parallel port only, two 67401/2 FIFOs were used along with the 67417 to obtain the appropriate organization.

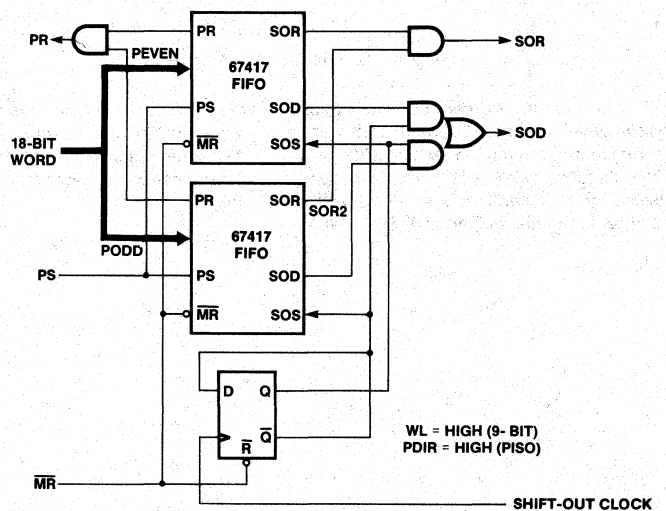


Figure 21. Another Example of an Expansion Scheme for a 64x18 Parallel-in to Serial-out FIFO Two 67417 FIFOs Are Used to Implement a 64x18 Parallel-in to Serial-out FIFO

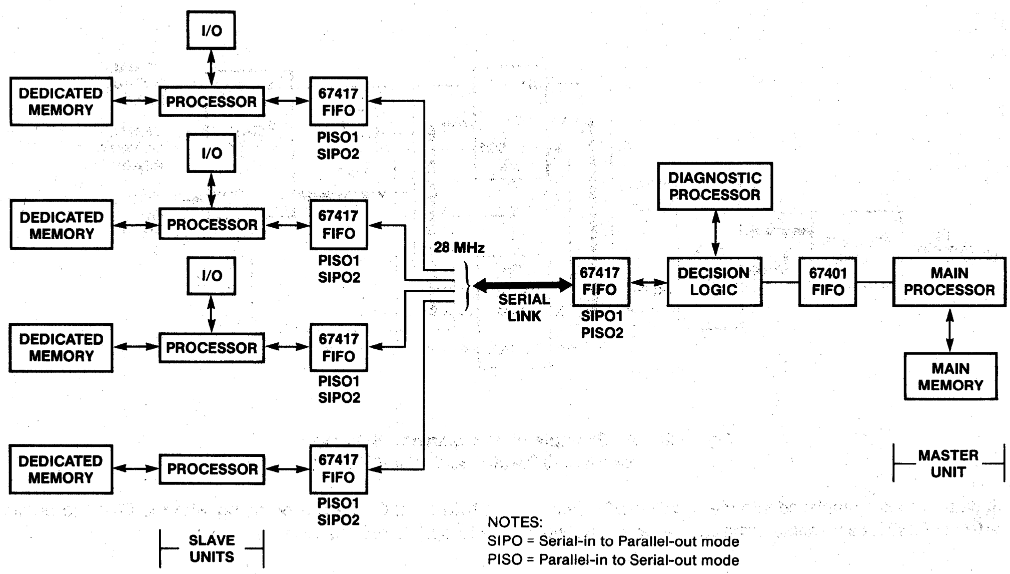


Figure 22. A Multiprocessing System

Each processor unit on the left has its own communication interface which consists of a serializing FIFO. The serial data link can operate in either direction 1 or direction 2 which is decided by the Decision logic. In direction 1 either of the slave units send the data to the master over the serial link, with its respective 67417 operating in parallel-in to serial-out mode (PISO1). While the 67417 for the master unit operates in serial-in to parallel-out mode (SIPO1). The direction 2 has the FIFOs (67417) operating in the reverse direction from the above case. Decision logic determines the priority of the slave processors to use the serial link.

Table of Contents
MEMORY SUPPORT

Memory Support Selection Guide

Dynamic RAM Controllers

DESCRIPTION	PART NUMBER	APPLICATIONS	PINS
Multi-mode DRAM Controller/Driver	SN74S408-3 SN74S408-2 SN74S408	16K, 64K DRAMs	48
Multi-mode DRAM Controller/Driver	SN74S409-3 SN74S409-2 SN74S409	16K, 64K, 256K DRAMs	48

8-Bit Dynamic-RAM Drivers

DESCRIPTION	PART NUMBER	APPLICATIONS	PINS
DRAM Drivers with complementary Enables	SN54/74S700/731-1	Pin-compatible with 'S210/241	20
DRAM Drivers with assertive Low Enables	SN54/74S730/734-1	Replaces Am2965/66; also pin compatible with 'S240/244	20

Power-Strobe Device

DESCRIPTION	PART NUMBER	APPLICATIONS	PINS
Quad Power/Logic Strobe	HD1-6600-8/HD1-16605-8 HD1-6600-5/HD1-6605-5 HD1-6600-2/HD1-6605-2	Useful to "power down" devices to reduce total system power	14

Improving Your Memory With 'S700-Family MOS Drivers

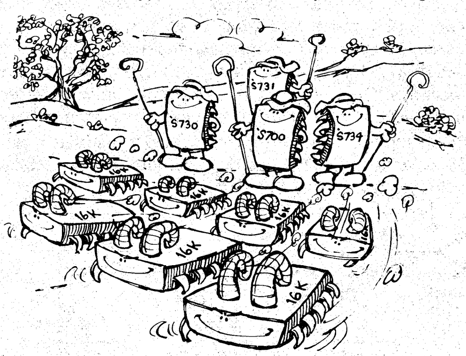
Chuck Hastings and Suneel Rajpal

Introduction

Today, fast-access-time high-density dynamic random-access-memory integrated circuits (DRAMs) are where it's at in the design of commercial computer memories of any size, from tabletop personal-computer memories to giant mainframe memories; magnetic cores are, now, "but a distant memory." As a computer-scene corollary to Parkinson's First Law[r1], "Work expands to fill the time available," it is observably *always* true that *"Computer software expands to fill the memory available."* Thus, the rapid advancements which have been made in the cost, density, availability, second-source standardization, and reliability of DRAMs have generally come just in the nick of time to keep up with the computer industry's insatiable demand for ever-larger main memories. To pick but one example, the Hewlett-Packard 3000-series minicomputer family was originally introduced with a maximum main-memory configuration of 131,072 bytes; today, the maximum configuration is 8,388,608 bytes, and plans for even larger configurations are already taking shape.

Unfortunately, the technological advancements in the *peripheral* integrated circuits needed to drive all of these DRAMs have, to say the least, been noticeably less rapid. The usual design practice has been to drive large DRAM arrays with high-current buffers such as 'S240s, coupled with external series resistors in the driven signal lines. Now, with the introduction of the Monolithic Memories 'S700/730/731/734 MOS drivers, the memory designer's task is greatly simplified.

The 'S700, 'S730, 'S731, and 'S734 are fast and powerful Schottky-technology TTL 8-bit buffers, specialized to drive large numbers of dynamic RAMs. Their internal design is particularly well adapted to driving signal lines with lots and lots of *distributed capacitance.* They are *drop-in, pin-compatible replacements* for the respective first-generation 'S240-family high-current drivers — 'S210, 'S240, 'S241, and 'S244, which excel for their intended high-current applications or even for lumped-capacitance applications but can be awkward to use in typical DRAM memory-board designs.



"...THE MONOLITHIC MEMORIES 'S700, 'S730, 'S731, AND 'S734 ARE...SPECIALIZED TO DRIVE LARGE NUMBERS OF DYNAMIC RAMS..."

So that you understand the essentials of what you need to know to design memory boards which work, we'll first take a quick glance at the electrical situation, complete with equations. Don't worry — we won't actually *derive* these equations here; derivations are readily available in the literature[r2, r3], and our purpose is simply to motivate some otherwise arbitrary-sounding statements as to what constitutes good layout practice. Following that, we'll present the rationale behind the various members of the family and their differing functional behavior or "architecture." Finally, we'll discuss some pragmatic design issues; how to avoid information loss due to glitches in battery-backup-protected memory systems during power failure, and when and where to use the 'S700 and 'S731 complementary-enable parts.

The Memory-Board Design Problem

The central problem facing the designer of a memory board is to drive a large number of highly-capacitative DRAM address, data, and control inputs just as fast as they can safely be driven, since memory speed (like memory size) is something which computer-system designers can never get quite enough of. Typically, a designer places *from 70 to 300 DRAMs on a single board.* Now, the address and data inputs of a DRAM have very non-negligible input capacitances — 3.5 picofarads (pf) typical, and 5 or even 7 pf worst-case; the control inputs may have as much as 10 pf worst-case. Assuming 5 pf, the total capacitance per address or data line per board must by simple multiplication fall between 350 pf and 1500 pf — even more when the capacitance of the printed-circuit-board (PCB) wiring traces is reckoned with. These numbers are not at all the sort of numbers you normally see on the data sheets for most of the industry-standard 8-bit buffers — those have for many years conventionally been specified by all vendors at 15 pf, 50 pf, etc. apparently according to the proposition that "small is beautiful," i.e., the logic delays and waveforms come out more agreeably at those numbers.

In keeping with motherhood and apple pie, the memory-board design obviously must be optimized for speed, reliability, physical area, and dollar cost; the *topology* (the physical organization and length of the wiring traces) and the number of drivers are chosen accordingly. Since contemporary DRAMs receive their complete addresses in *two* pieces, a "row address" and a "column address" (corresponding to the cell layout within the DRAM chip), the speed of the address-driving circuits is *particularly* critical since the bit pattern transmitted on the address lines must be changed *twice* during each complete memory read or write cycle. In DRAM "architecture," the row and column addresses are of equal length, say n bits, and the width of the data word within the DRAM is one bit in most contemporary parts. The first DRAMs with this architecture, in the mid-1970s, had n = 6, and thus were 2^{12}x1 = 4096x1 or "4K" DRAMs. By now, of course, such tiny DRAM sizes are

8

obsolete, and even 16K (16384x1) DRAMs are a super-low-cost commodity. Much commercial design today is being done with 64K (65536x1) DRAMs, and even larger DRAMs are coming soon; 256K (262144x1) DRAMs pin-compatible with the usual 64K types have been announced.

When all of these factors are taken into account, the practical upper limit to how many DRAM inputs can be hung on one trace is usually thought to be in the range of 80 to 100. This limit has some implications with respect to word length and word organization. The combined effect of the system word length as seen by the computer programmer, the number of check-code bits used for whatever checking scheme is employed, and the number of different words simultaneously accessed on one memory operation is to make certain odd-sounding total word lengths popular:

Organization	Total Word Length	Data Word Length	Check Bits/ Word	Checking Scheme
17x4	68	16	1	Simple parity
72x1	72	64	8	Hamming code
39x2	78	32	7	Hamming code
22x4	88	16	6	Hamming code

Table 1. Common DRAM Memory-Board Organizations

Assumptions and Equations

The key to good memory-board design is optimization of the layout and impedance of the wiring traces, and the choice of efficient RAM drivers. In prototype wirewrapped boards, the characteristic impedance of a wire which is at a varying distance from a ground plane as it crosses hill-and-dale over other wires may be difficult to control or predict, but is likely to be within the range of 100 to 120 ohms. In production memory boards, however, it is often a good approach to use *microstrips* to interconnect the array of DRAMs. A microstrip is simply a PCB wiring trace over a ground plane, separated from that ground plane by a thin layer of insulating medium such as fiberglass. A cross section of a microstrip is shown in Figure 1.

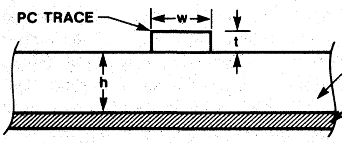


Figure 1. Microstrip Cross Section

The equations needed to design a memory board for a DRAM array interconnected by microstrips are listed below. Their rationale and derivation can be found in references on the application of electromagnetic field theory to circuit-board design[r2, r3].

Z_O = the characteristic trace impedance.

$$= \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \text{ohms}$$

T_d = the trace propagation velocity.

$$= 0.0848\sqrt{0.475e_r + 0.67} \text{ nsec/inch}$$

C_O = the trace capacitance.

$$= 1000\,(T_d/Z_O) \text{ pf/inch}$$

C_d = the equivalent trace capacitance associated with each DRAM. It takes 0.5 inches to interconnect one DRAM.

$$= 3.5 \text{ pf}/0.5 \text{ inch} = 7 \text{ pf/inch}$$

Z'_O = the modified trace impedance due to the capacitive loading of the DRAMs.

$$= \frac{Z_O}{\sqrt{1 + C_d/C_O}}$$

T'_d = the modified trace propagation time due to the capacitive loading of the DRAMs.

$$= T_d\sqrt{1 + C_d/C_O}$$

Where:
e_r = the relative dielectric constant of the PC board.
h = the distance from the trace to the ground plane.
w = the width of the trace.
t = the thickness of the trace.

Design Approaches and Their Consequences

Very well then, let's charge right in and see what these formidable-looking equations predict will happen when a memory board is laid out in an obvious, common-sense manner. To make the example specific, we choose the 39x2 organization, so that from a circuit point of view the word length on the memory board is 78 bits. Now, each wiring trace has a capacitance (C_{TRACE}) and an inductance (L_{TRACE}) per DRAM; assuming that the DRAMs are deployed at uniform intervals along the trace, these values are determinable easily from the values per-unit-length from the microstrip equations just presented, once the spacing in inches between DRAMs has been specified. (The value for L_{TRACE} has been buried in the equation for Z_O above and won't appear in any subsequent equations.) To be specific, we'll make the realistic assumption of one DRAM per 1/2 inch of trace. Each DRAM input also has a capacitance (C_{DRAM}) and an inductance (which we're justified in neglecting); we'll assume that these are uniform, although the most sophisticated designers consider *distributions* of DRAM capacitances. The electrical situation which results is shown in Figure 2:

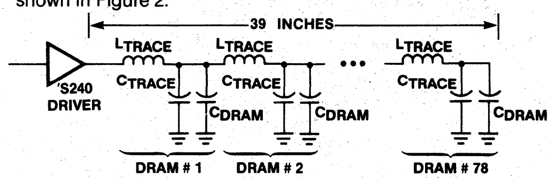


Figure 2. Transmission-Line Equivalent of a Single DRAM Wiring Trace

Typically, this trace has the following characteristics:

e_r = 5 (for G10 glass epoxy)
h = 30 mils
w = 15 mils
t = 3 mils

The following values can then be calculated using the appropriate equations:

Z_o = 85 ohms
T_d = 0.15 nsec/inch
C_o = 1.76 pf/inch
Z_o' = 38 ohms
T_d' = 0.35 nsec/inch

If we just string the DRAMs right down the trace like Christmas-tree lights, it will take 39 inches of trace to connect all 78 of them. So the actual propagation delay of the drive signal as it surges down this trace will be T_d' times 39 inches, or 0.35x39 = 13.7 nsec.

Notice that we are embarked on a design which is *specific* to the properties, including C_{DRAM}, of DRAMs which we are using; a final board design is inevitably, to some extent, "tuned" to a specific DRAM type. If C_{DRAM} changes, even in what might be considered the favorable direction (smaller, obviously!), the trace impedance gets changed and the design may no longer be "tuned." But we won't worry about that here.

Now, an 'S240 driver, such as we have assumed to be driving the trace, has a signal rise time or fall time of anywhere from 2 nsec to 10 nsec, depending on semiconductor manufacturing parameters. (The rise time is, to be precise, defined as the time it takes for the output voltage to go from 10% of full-scale to 90% of full-scale; the fall time is the obvious converse.) A good rule-of-thumb for circuit-board designers is that twice the propagation delay of the trace should be less than the rise time or fall time of the driver in order to avoid serious signal *reflections*, in which a "reflected" electromagnetic wave comes bouncing back from the other end of the trace. In other words, 2x13.7 nsec + 27.4 nsec must be less than 2-to-10 nsec, which it obviously isn't. Hence there *will* be reflections on this line, and *ringing* of the signal will occur, resulting in a waveform in the trace which looks like that of Figure 3 for a High-to-Low transition at the 'S240 output. The amplitude of the ringing voltage in real systems may be as much as 2v or even 2.5v.

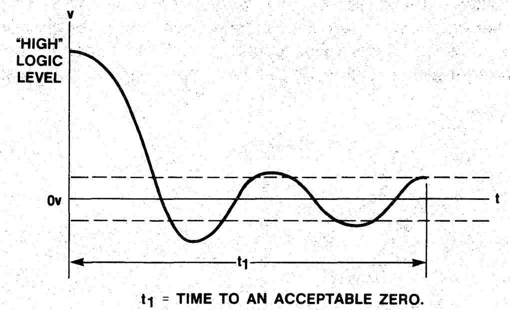


Figure 3. Line Ringing Due To Driver Mismatch

An 'S240 has a Schottky-driver output stage which may simplistically and approximately be represented as shown in Figure 4. When the 'S240 is driving to the logic High state, the switch S may be thought of as in position #1; when it is driving Low, S is in position #2. The effective output impedance of the 'S240 is thus about 30 ohms when driving from a previous Low state to High, but only about 10 ohms when driving from High to Low — a 3:1 difference. Thus, as the large lower transistor in the output "totem-pole" structure turns on very fast because of this low impedance, the fall time is *extremely* fast, and when ringing occurs the result may be *undershoot* — the voltage in the trace actually falls *below ground.*

An obvious consequence of ringing in the signal trace is that the system designer must allow much longer for the driver voltages, as seen by the DRAM inputs, to settle down after a transition since the ringing may be severe enough to repeatedly cross the switching threshold for the DRAMs. If this settling only had to happen once per memory access it would be bad enough, but it happens *twice* — remember that first the *row* address, and then the *column* address, gets transmitted over the address lines. Thus the allowances made for ringing cause memory performance, as measured by access time and/or cycle time, to significantly deteriorate.

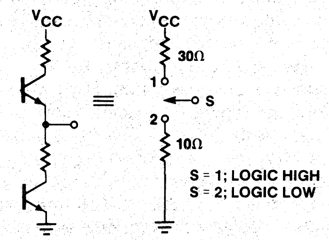


Figure 4. Typical Schottky-Driver Output Impedances

Even worse things can happen because of undershoot. First, if the voltage as seen by the DRAM inputs ever falls below -1.0v, that is, more than a volt below the steady-state PCB ground voltage at the DRAM ground pins, the contents of the "row-address registers" within the DRAMs can be altered. (*Some* DRAMs are supposed to be able to stand -2v for 20 nsec, but others just can't handle it.) Thus, if a write operation is in progress, the data word can get written helter-skelter into *different address locations in different DRAMs* (remember, each DRAM is just 1 bit wide!), so that the entire memory system very rapidly forgets everything it once knew. Second, the current surges resulting from severe undershoot may cause some 'S240-type drivers themselves to rather quickly self-destruct, which can be particularly annoying if they have been dip-soldered into place.

At this point it appears that our simple, common-sense first cut at memory-board layout is a naive recipe for disaster. So what can we do to improve on this naive approach and get the memory board to work?

First, we can *series terminate* the trace with a 10-ohm resistor to improve the impedance match. "Series termination" simply means that the resistor is located right *at* the 'S240 output, between it and the rest of the trace. 10 ohms is probably the minimum value for this resistor; other values of up to 33 ohms are also in use, according to the design context.

Second, much of our problem came about because of the sheer physical length of the trace, so we can modify the topology to cut that in half by having two "legs" rather than just

8

one off the driver output, which should essentially cut the propagation time for the trace in half.

Third, if need be, we could also vary the trace *width*, w, to change the trace impedance, Z_O, to a value more to our liking, in order to fine-tune the design, but we won't pursue that possibility here.

The result is the significantly-different layout of Figure 5, with all of the cute little capacitors and inductors omitted for clarity (or actually for sheer laziness):

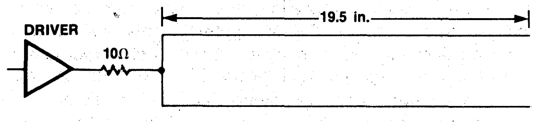


Figure 5. An Improved Layout

When the calculations are repeated, it turns out that the propagation delay down each leg of the trace is half as much, or 6.9 nsec; and the output impedances of the 'S240-plus-series-resistor are now 40 ohms when driving from Low to High, and 20 ohms when driving from High to Low, which is only a 2:1 difference. The trace impedance seen by this 'S240-plus-series-resistor is that of two 38-ohm legs in parallel, or 19 ohms, which is a very much better match to its effective output impedance. Also, the series resistor acts to slow down the exceedingly-rapid fall time of the 'S240, to the point where it may not be a great deal less than (or may even exceed) twice the trace propagation delay. So, obviously, we're a lot better off than we were.

Unfortunately, we're still not home free. We've also slowed down the *rise* time of the 'S240, i.e., the Low-to-High transition, which we weren't intending to do since it wasn't a problem. What we *really* would like is for the Low-to-High transition time and the High-to-Low transition time to become virtually the same, i.e., "symmetric." Now, DRAM addresses and data have a generally unpredictable salt-and-pepper mixture of ones and zeroes, and there is no way to take advantage under system conditions of a circuit design with one of these transition times much faster than the other. So computer-systems people, who have to be brutal realists rather than cockeyed optimists if their systems are to work reliably under real-world assumptions, normally just take whichever of these two transition times is "worse" (that is, longer) as the "logic delay" of the part as it operates within a system. Which is only reasonable! And thus it comes about that a deterioration in transition-time *symmetry* translates as a deterioration in net system *speed.*

So what do we do next? Well, we could try applying the same improvements a second time, by breaking the trace into *four* legs; however, physically interconnecting these four legs then will add more trace length, so that topology has to be traded off against interconnection efficiency. What would just get us out of this whole mess is if we could get *inside* the 'S240 and put the series resistor someplace where it will result in the effective output impedance of the driver being the same whether it is driving from Low-to-High or from High-to-Low. But we can't do *that.* Can we? Can we???

The 'S700-Family Drivers to the Rescue

Well, we can't exactly get *inside* an 'S240 and stick in a series resistor. We can, however, pull the 'S240 out of the socket it is occupying, and pop in an 'S730 — which is a *pin-compatible drop-in replacement,* and has the series resistor in exactly the right place. If we had been using a different 'S240-family driver, we could still have done the same thing — an 'S734 replaces an 'S244, an 'S700 replaces an 'S210, and an 'S731 replaces an 'S241; more on the various part types shortly.

When thus popped in as 'S240-type driver replacements, 'S700, 'S730, 'S731, and 'S734 drivers will generally speed up the total *effective* access and cycle times for most DRAM boards. This speed improvement is achieved by a sophisticated, rather than a brute-force, circuit-design approach. We've already let the cat out of the bag; they feature a new type of output stage, incorporating a *built-in* series limiting resistor, designed to efficiently drive highly-capacitative loads such as arrays of DRAM inputs interconnected by typical printed-circuit-board (PCB) wiring traces. This series resistor is located in the ideal place — between the collector of the lower output transistor in the totem-pole structure and the output pin. (See Figure 6.)

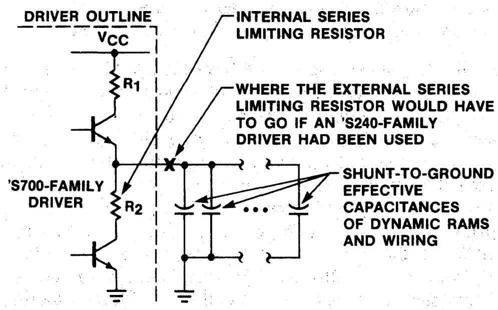


Figure 6. The Dynamic-RAM-Driver Circuit Output Stage

Now that the all-important resistor is safely inside the drive chip, its value is chosen as 20-25 ohms, so that the *in-system* Low-to-High and High-to-Low transition times of the resulting driver output stage remain symmetric, *with* the series resistor accounted for, under a wide range of circuit-loading conditions. The equivalent to Figure 4 for this new improved output stage is:

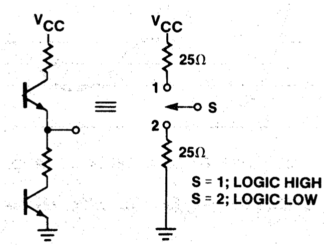
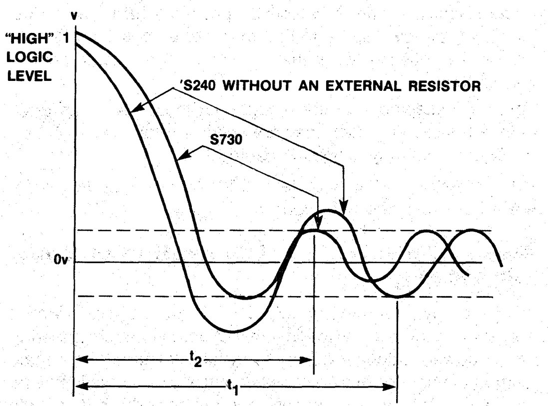


Figure 7. Driver Output Stage for 'S700-Series Buffers

What does that additional resistor in the transistor buy you? Plenty, when coupled with the other design features incorporated into the 'S700, 'S730, 'S731, and 'S734. First, there is a balanced impedance of about 25 ohms for either the Low-to-High transition or the High-to-Low transition. Since the effective impedance for the Low-to-High transition is now considerably higher than it was when using an 'S240, the undershoot problem goes away — the output voltage can never have an undershoot worse than 0.5v. Ringing *can* still occur; however, the time taken to reach an acceptable zero level is smaller than it was when using an 'S240, as shown in Figure 8.

Another advantage of the 'S700, 'S730, 'S731, and 'S734 is the high-state output voltage, now guaranteed to reach at least V_{CC}-1.15v. Certain MOS DRAM inputs are specified to require a minimum V_{IH} of 2.7 volts. More on this and other specification issues in just a minute.



t_1 = TIME TO ACCEPTABLE "LOW" LOGIC LEVEL FOR THE 'S240 WITHOUT AN EXTERNAL RESISTOR.

t_2 = TIME TO ACCEPTABLE "LOW" LOGIC LEVEL FOR THE 'S730.

Figure 8. Comparison of Undershoots; 'S240 and 'S730

Undershoot control, balanced High-state and Low-state output impedances, and appropriate voltage levels make the 'S700, 'S730, 'S731, and 'S734 very efficient RAM drivers. Consequently, although 'S240-family buffers may exhibit greater speed under light loading conditions and may even sink larger currents when operated in test jigs, 'S700-family buffers are likely to perform better under *realistic system conditions* when driving large capacitive loads is a major factor in the application. There may even be some *non-DRAM* bus-driving applications where such is the case!

And, as small added bonuses, the designer no longer has to find the physical space on his/her board for the external limiting resistors, and the resistors themselves no longer have to be paid for, and nobody has to be paid to stuff them into place on production copies of the board. All in all, an across-the-board "win-win" situation.

Keeping the Family Straight

Of the four new buffers in the 'S700 family, two — the 'S730 and 'S734 — are alternate-source versions of the Am2965 and Am2966 respectively. These two parts were originally introduced by AMD, which has also designated them alternatively as AmZ8165 and AmZ8166.

The other two buffers — the 'S700 and 'S731 — are *complementary-enable* versions of the 'S730 and 'S734 respectively, just as the 'S210 and 'S241 are complementary-enable versions of the 'S240 and 'S244. Complementary-enable parts excel in driving buses where the information to be placed on the bus can come from two different but physically adjacent origins, such as instruction addresses and data addresses in a bit-slice bipolar microcomputer system, or row-address fields and column-address fields on a DRAM memory board; more on this later.

These four new 'S700-family buffers may be grouped with Monolithic Memories' other buffers in a 2x2 matrix chart or "Karnaugh map," with the dimensions of this map chosen to be the assertiveness of the second-buffer-group enable input E_2 (here across the top, or X-axis) and the polarity of the data-buffer logical elements themselves (here down the side, or Y-axis). This chart is Table 2 of "Pick the Right 8-bit or 16-bit Interface Part for the Job," in section 13 of this databook.

The logic symbols for each of these four parts are shown on the first page of the data sheet, in part-number order. Except for the differences already noted in the assertiveness of signal E_2, and in the output polarity of the data buffers, these parts are all mutually pin-compatible.

You will have an easier time keeping these four parts straight once you notice that the part number for one particular "architecture" of 'S700-series buffer is always the part number of the corresponding high-current buffer, *plus 490.* Since hundreds of 54/74 part numbers have already been assigned, even though not all of the corresponding parts are yet in production, obtaining part numbers with even *this* much method in the madness was not exactly a piece of cake! Anyhow, if you want to easily remember what the part number should be when you replace an 'S240-family buffer with an 'S700-family buffer, you must add 490 to its part number: e.g., 'S241 + 490 = 'S731, and so forth.

Like other Monolithic Memories' 20-pin 8-bit interface circuits, the 'S700, 'S730, 'S731 and 'S734 come in the celebrated 300-mil SKINNYDIP® package. They *also* come in eutectic-seal-flatpack and leadless-chip-carrier packages.

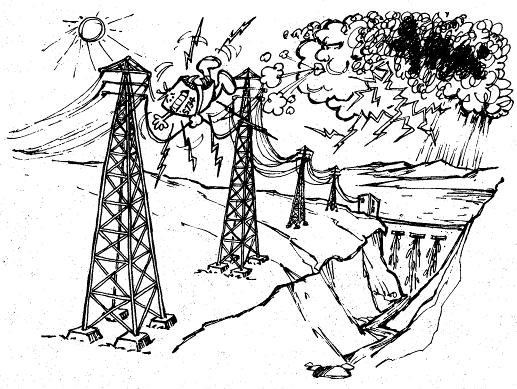
"... THE 'S700, 'S730, 'S731, AND 'S734 COME IN THE CELEBRATED 300-MIL 'SKINNYDIP™' PACKAGE..."

A Few Subtleties Regarding 'S700-Family Driver Specifications

If you are used to regular run-of-the-mill TTL data sheets, you should become sensitive to the fact that in several respects the Monolithic Memories 'S700-family data sheet (and, to be fair to a friendly competitor, AMD's Am2965/6 data sheet) represents a substantial departure from this norm.

First, since 'S700-family MOS drivers are obviously intended to mingle freely in the MOS world, they are specified to operate properly with as much as a ± 10% power-supply-level fluctuation over the entire commercial temperature range, instead of just the usual TTL ± 5%. The ± 10% standard is usual for MOS parts, but in the TTL world it is normally met only by selected military-version parts specified over the military temperature range. Thus, the V_{CC} seen by your commercial 'S700-series parts may fluctuate (even though you hope it won't) from 4.50v to 5.50v instead of only from 4.75v to 5.25v as for most commercial TTL.

Second, as already mentioned, an acceptable output logic High is considered to be V_{CC} -1.15v, or 3.85v assuming that your power supply really *is* under control after all. MOS parts are specified to think they're still seeing a Low up to 0.8v at an input, and to be seeing a High above either 2.4v or 2.7v; in between is, of course, the usual transitional or no-mans-land region. In keeping with the needs of the MOS world, 'S700-family Low-to-High logic propagation delays are measured from when the *input* crosses the usual TTL threshold somewhere in this no-mans-land (say 1.5v) to when the *output* crosses 2.7v — *not* merely to when the output crosses the TTL threshold. Likewise, 'S700-family High-to-Low logic propagation delays are measured from when the input crosses the TTL threshold to when the output crosses 0.8v. (See Figure 9).



"... S700 FAMILY MOS DRIVERS... ARE SPECIFIED TO OPERATE PROPERLY WITH AS MUCH AS A ±10% POWER-SUPPLY-LEVEL FLUCTUATION OVER THE ENTIRE COMMERCIAL TEMPERATURE RANGE, INSTEAD OF THE USUAL TTL ±5%..."

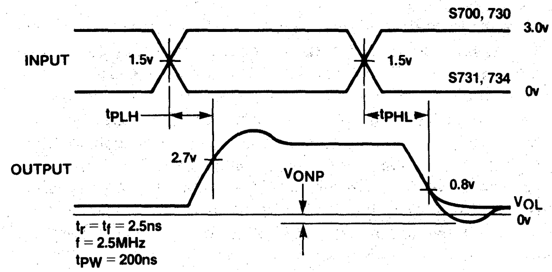


Figure 9. S700-Family Output-Voltage-Level Specification Conventions

Third, *both* minimum and maximum propagation delays are specified (at 25° C and 5v), so that you don't need to worry about any unwanted consequences in your system if your memory-access time for some bit positions turns out to be unexpectedly low relative to that for other bit positions. Worst-case skew between two buffer elements on the same chip is also specified.

Fourth, in keeping with the pledge that these parts can drive highly-capacitative lines, they are *specified* that way — at 500 pF loading, not only at 500 pF loading.

Fifth, unlike 'S240-family buffers, 'S700-family MOS drivers do **not** feature designed-in hysteresis.

Power-Failure-Proof Operation of Your DRAM Memory

It's generally nice if your computer, of whatever size, doesn't forget everything it was in the midst of doing and remembering if a-c power suddenly goes off. In fact, for large mainframe computers and for high-reliability control computers it may be downright critical. So, increasingly, memory designs include power-failure-protection logic, and DRAM "refresh" circuitry can run on battery-backup power. A typical design implementation is shown in Figure 10.

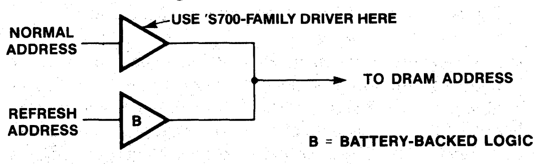


Figure 10. Battery Backup for Refresh-Address Logic

The refresh operations for the memory array must be *uninterrupted* during the transitions from a-c power to battery power and back, or else data will be lost; consequently, *all* of the logic associated with the DRAM refresh operations must be backed up. For economic reasons, other logic may *not* be backed up; hence, great care must be taken in the design at the DRAM interface, so that transients or oscillations are not introduced into the DRAM input lines by the non-backed-up logic thrashing around as a-c power goes down or comes back up.

Returning to Figure 10, note that it is the *normal* address path which is a potential source of DRAM input glitches, since the refresh-address-path buffer presumably never goes down. Again 'S700-family drivers can come riding to the rescue, since they are guaranteed to maintain glitch-free operation during either power-up or power-down.

Where to Use Complementary-Enable MOS Drivers

Driving a dynamic-MOS RAM address bus with a multiplexed row/column address can conveniently be done with an 'S700 as shown in Figure 9 of "Pick the Right 8-bit or 16-bit Interface Part for the Job," in Section 11 of this databook. This part is an inverting complementary-enable buffer with a series-resistor output structure, which is an ideal combination of characteristics here.

First of all, a TTL inverting buffer normally has one less transistor —and hence one less delay — in its internal data path than does an equivalent noninverting buffer, and hence is faster. And dynamic MOS RAMs really don't care if their addresses come in "true" or "complemented" form as long as that form *never* changes.

Second, a complementary-enable buffer can easily multiplex two different address sources to the same set of outputs without introducing extra switching delay, or allowing a momentary "bus fight" condition, if the same control signal (here CAS or "Column Address Strobe") is tied directly to both $\bar{E}_1$ and E_2, and the two 4-bit groups of outputs are tied together.

Like other three-state buffers, these parts operate in a "break-before-make" manner — it is faster to disable an output than to enable an output, by design. (The worst-case data-sheet a-c parameters don't always imply "break-before-make" operation, but the parts themselves **do** operate that way.) So, if two outputs are tied together and exchange control of the bus, they can't "fight," i.e., try simultaneously to drive the bus in opposite directions; at any given instant, one of the two will always be "floating" in the hi-Z state.

The 8 data input lines to *each* 'S700 must, of course, be parceled out with 4 lines coming from the row address and 4 lines coming from the column address.

These same advantages continue to accrue when an 'S700 is used, for example, to select between instruction addresses and data addresses in a minicomputer, or between next-microinstruction and branch addresses in a microengine, or between input and output addresses in a multiplexed input/output data channel, assuming that in each of these cases the address being produced is to go to the DRAMs without further ado. Notice that the 'S700s here are accomplishing *driving* (that is, power amplification and impedance matching) *and multiplexing simultaneously.* You could have used an MSI multiplexer part followed by an 'S730 to accomplish this very same thing, but with more logic delay.

If what you need in your application is a *non-inverting* driver, then everything we've just said above about the 'S700 continues to hold for the 'S731.

The Bottom Line

The 'S700, 'S730, 'S731, and 'S734, because of their unique output stage with an internal series resistor and balanced-impedance characteristics, can drive highly-capacitive loads of up to perhaps 100 dynamic-MOS RAM inputs. Since undershoot is limited to -0.5v already and so no *external* series limiting resistors are needed, the result is a net *system* speed gain, since Low-to-High and High-to-Low transition times remain symmetric. Otherwise, the logic delay would get degraded, since it must always be taken as the *worst* of these two transition times, and the use of an *external* series resistor greatly lengthens the Low-to-High transition time.

These second-generation MOS drivers also guarantee an output High voltage of V_{CC} -1.15v, and provide glitch-free operation during power-up and power-down. All of these features make them especially suitable for driving the address, data, and control lines of arrays of MOS DRAMs.

Credit Where Credit Is Due

A couple of years ago, many Monolithic Memories customers approached us with the emphatic suggestion that we should produce MOS drivers of this type, backed up by technical arguments which we have attempted herein to distil and present. In particular, the advice and assistance of Tak Watanabe of the Hewlett-Packard Computer Systems Division in Cupertino, California, has been utterly essential in the preparation of this application note.

Also, it was originally at Tak's suggestion that Monolithic Memories decided to produce the 'S700 and 'S731 complementary-enable drivers, as well as the 'S730 and 'S734 assertive-low-enable drivers. Tak's contributions, and those of other sage electronics-industry designers with whom we have spoken, are hereby gratefully acknowledged.

References

r1. *Parkinson's Law and Other Studies in Administration,* C. Northcote Parkinson, Houghton Mifflin Company, Boston, MA, 1957; also Ballantine Books, N.Y., 1964.

r2. *MECL System Design Handbook,* William R. Blood, Jr., Motorola Semiconductor Products Inc., Mesa, AZ, May 1983 (Fourth Edition); see in particular chapter 7.

r3. "Characteristics of Microstrip Transmission Lines," H. R. Kaupp, *IEEE Transactions on Electronic Computers,* April 1967 (Volume EC-16, Number 2); pages 185-193.

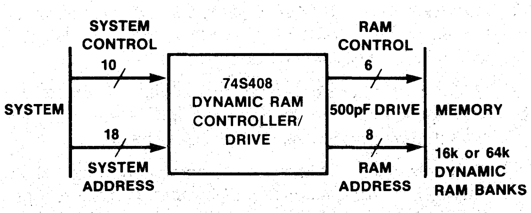
Dynamic RAM Controller/Driver

SN74S408/DP8408
SN74S408-2/DP8408-2
SN74S408-3/DP8408-3

Features/Benefits

- All DRAM drive functions on one chip have on-chip high-capacitance-load drivers (specified up to 88 DRAMs)
- Drives directly all 16K and 64K DRAMs: Capable of addressing up to 256K words
- Propagation delays of 25 nsec typical at 500-pF load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- Six operating modes support externally-controlled access and refresh, automatic access, as well as special memory initialization access
- On-chip 8-bit refresh counter with selectable End-of-Count (127 or 255)
- Direct replacement for National DP8408

MODE	MODE OF OPERATION
0,1,2	Externally-controlled refresh
3	Externally-controlled All-$\overline{\text{RAS}}$ write
4	Externally-controlled access
5	Auto access, slow t_{RAH}
6	Auto access, fast t_{RAH}
7	Set end of count

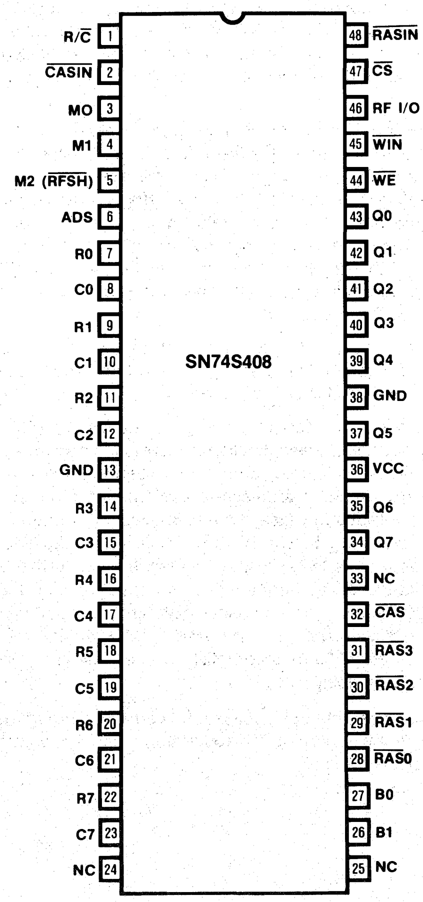


74S408 Interface Between System and DRAM Banks

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S408	N48, D48 (L52)	COM
SN74S408-2	N48, D48 (L52)	COM, SPEED OPTION
SN74S408-3	N48, D48 (L52)	COM, AC OPTION

Pin Configuration



NC = NO CONNECTION

Portions of this Data Sheet are reprinted courtesy of National Semiconductor Corporation.

Block Diagram

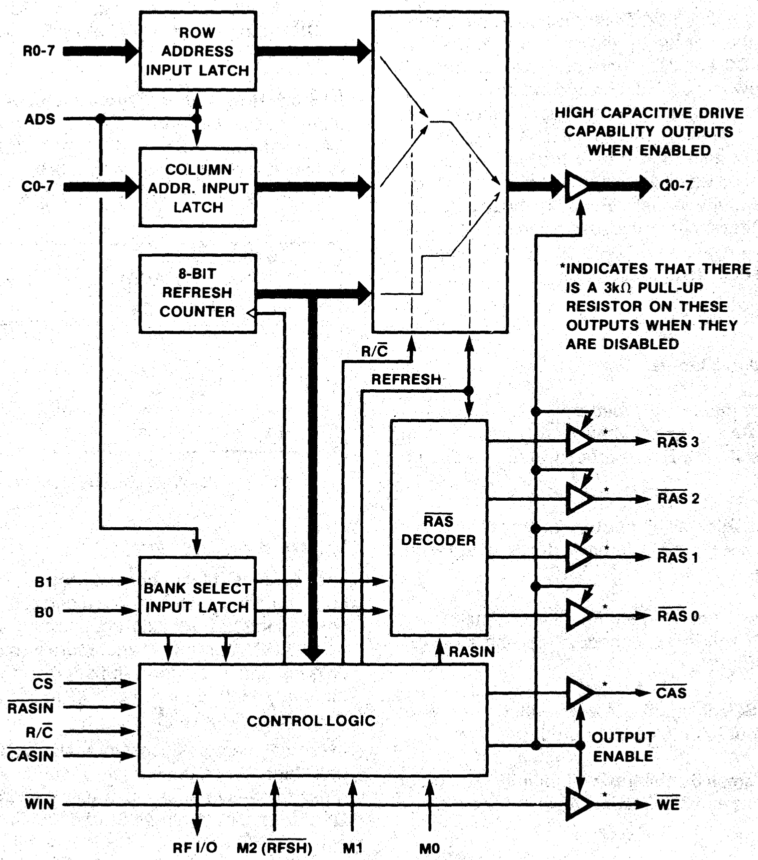


Figure 1. 74S408 Functional Block Diagram

Description

The 74S408 is a Multi-Mode Dynamic RAM Controller/Driver capable of driving directly up to 88 DRAMs. 18 address lines allow the 74S408 to drive all 16K and 64K DRAMs and addresses up to 256K words. Since the 74S408 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, and saves board space.

The 74S408's 6 operating modes offer externally-controlled or on-chip automatic access and externally-controlled refresh. An on-chip refresh counter makes refreshing less complicated; and automatic memory initialization is both simple and fast.

The 74S408 is a 48-pin DRAM Controller/Driver with 8 multiplexed address outputs and 6 control signals. It consists of two 8-bit address latches, an 8-bit refresh counter, and control logic. All address output drivers are capable of driving 500pf loads with propagation delays of 25nsec. The 74S408 timing parameters are specified driving the typical load capitance of 88 DRAMs, including trace capitance.

The 74S408 can drive up to 4 banks of DRAMs, with each bank comprised of 16Ks, or 64Ks. Control signal outputs $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are provided with the same driving capability. Each $\overline{RAS}$ output drives one bank of DRAMs so that the four $\overline{RAS}$ outputs are used to select the banks, while $\overline{CAS}$, $\overline{WE}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the nonselected banks in the standby mode (less than one tenth of the operating power) with the data output in three-state. Only the bank with its associated $\overline{RAS}$ low will be written to or read from, except in mode 3 where all $\overline{RAS}$ signals go low to allow fast memory initialization.

Pin Definitions

V_{CC} GND, GND—$V_{CC} = 5V \pm 5\%$. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 8 address bits change in the same direction simultaneously. Recommended solution would be a 1μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

R0-R7: Row Address Inputs.

C0-C7: Column Address Inputs.

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-of-Count (see table 3).

Q0-Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input—Enables selected $\overline{RAS_n}$ output when M2 ($\overline{RFSH}$) is high (modes 4-6), and all $\overline{RAS_n}$ outputs in modes 0, 1, 2 and 3.

R/$\overline{C}$: Row/Column Select Input—Selects either the row or column address input latch onto the output bus.

$\overline{CASIN}$: Column Address Strobe Input—Inhibits $\overline{CAS}$ output when high in Modes 4 and 3. In Mode 6 it can be used to prolong $\overline{CAS}$ output.

ADS: Address (Latch) Strobe Input—Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; latches on High-to-Low transition.

$\overline{CS}$: Chip Select Input—Three-state's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in mode 0, 1, 2). Enables all outputs when low.

M0, M1, M2 ($\overline{RFSH}$): Mode Control Inputs—These 3 control pins determine the 6 modes of operation of the 74S408 as depicted in Table 1.

RF I/O—The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active (low) when M2 = 0 (modes 0, 1, 2 or 3) and the End-of-Count output is at 127 or 255 (see Table 3).

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output—Buffered output from $\overline{WIN}$.

$\overline{CAS}$: Column Address Strobe Output—In Modes 5 and 6, $\overline{CAS}$ transitions low following valid column address. In Modes 3 and 4, it goes low after R/$\overline{C}$ goes low, or follows $\overline{CASIN}$ going low if R/$\overline{C}$ is already low. $\overline{CAS}$ is high during refresh.

$\overline{RAS}$ 0-3: Row Address Strobe Outputs—When M2($\overline{RFSH}$) is high (modes 4-7), the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When M2 ($\overline{RFSH}$) is low (modes 0-3) all $\overline{RAS_n}$ outputs go low together following $\overline{RASIN}$ going low.

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS_n}$
B1	B0	
0	0	$\overline{RAS_0}$
0	1	$\overline{RAS_1}$
1	0	$\overline{RAS_2}$
1	1	$\overline{RAS_3}$

Table 1. Memory Bank Decode

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{RASIN}$ and R/$\overline{C}$ are initially high. When the address inputs are enabled into the address latches (modes 4-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, (B0 and B1). If $\overline{CS}$ is low, all outputs are enabled. When $\overline{CS}$ is transitioned high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S408s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{CS}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The 74S408 has timing parameters that are specified with up to 600pF loads for $\overline{CAS}$, 500pF loads for Q_0-Q_7 and $\overline{WE}$, and 150 pF loads for $\overline{RAS_n}$ outputs. In a typical memory system this is equivalent to about 88 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 6). The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S408 Driving Any 16K, 64K or 256K DRAMs

The 74S408 can drive any 16K or 64K DRAMs. The on-chip 8-bit counter with selectable End-of-Count can support refresh of 128 or 512 rows, while the 8 address and 4 $\overline{RAS}_n$ outputs can address 4 banks of 16K or 64K DRAMs.

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and DATA at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

Power-Up Initialize

When V_{CC} is first applied to the 74S408, an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

74S408 Functional Mode Description

The 74S408 operates in 6 different functional modes. The operating mode is selected by signals M_0, M_1, M_2. Selecting M_2, M_1, M_0 = 0,0,0 or 0,0,1 or 0,1,0 will result at the same operating mode designated as mode 0,1,2 (see Table 2).

MODE	(RFSH) M2	M1	M0	MODE OF OPERATION	CONDITIONS
0,1,2	0 0 0	0 0 1	0 1 0	Externally-controlled refresh	RF I/O = EOC
3	0	1	1	Externally-controlled All-$\overline{RAS}$ write	All-$\overline{RAS}$ active
4	1	0	0	Externally-controlled access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto access, slow t_{RAH}	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto access, fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set end of count	See Table 3 for Mode 7

Table 2. 74S408 Mode Select Options

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74S408 Functional Mode Descriptions

Modes 0, 1, 2—Externally Controlled Refresh

In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled onto R_0-R_7 outputs, all $\overline{RAS}$ outputs are enabled following $\overline{RASIN}$, and $\overline{CAS}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{RASIN}$ or $M_2(\overline{RFSH})$ goes low-to-high while the other is low. RF I/O goes low when the count is 127 or 255 with $\overline{RASIN}$ and $\overline{RFSH}$ as set by End-of-Count (see Table 3), low. To reset the counter to all zeroes, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and $M_2(\overline{RFSH})$ can transition low simultaneously because the refresh counter becomes valid on the output but t_{RFLCT}. This means the counter address is valid on the Q outputs before $\overline{RAS}$ occurs on all $\overline{RAS}$ outputs, strobing the counter address into that row of all the DRAMS (see Figure 2). To perform externally controlled burst refresh $M_2(\overline{RFSH})$ initially can again have the same edge as $\overline{RASIN}$, but then can maintain a low state, since $\overline{RASIN}$ going low-to-high increments the counter (performing the burst refresh).

Mode 3—Externally Controlled All-$\overline{RAS}$ Write

This mode is useful at system initialization. The memory address is provided by the processor, which also perform the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S408 for the next write cycle.

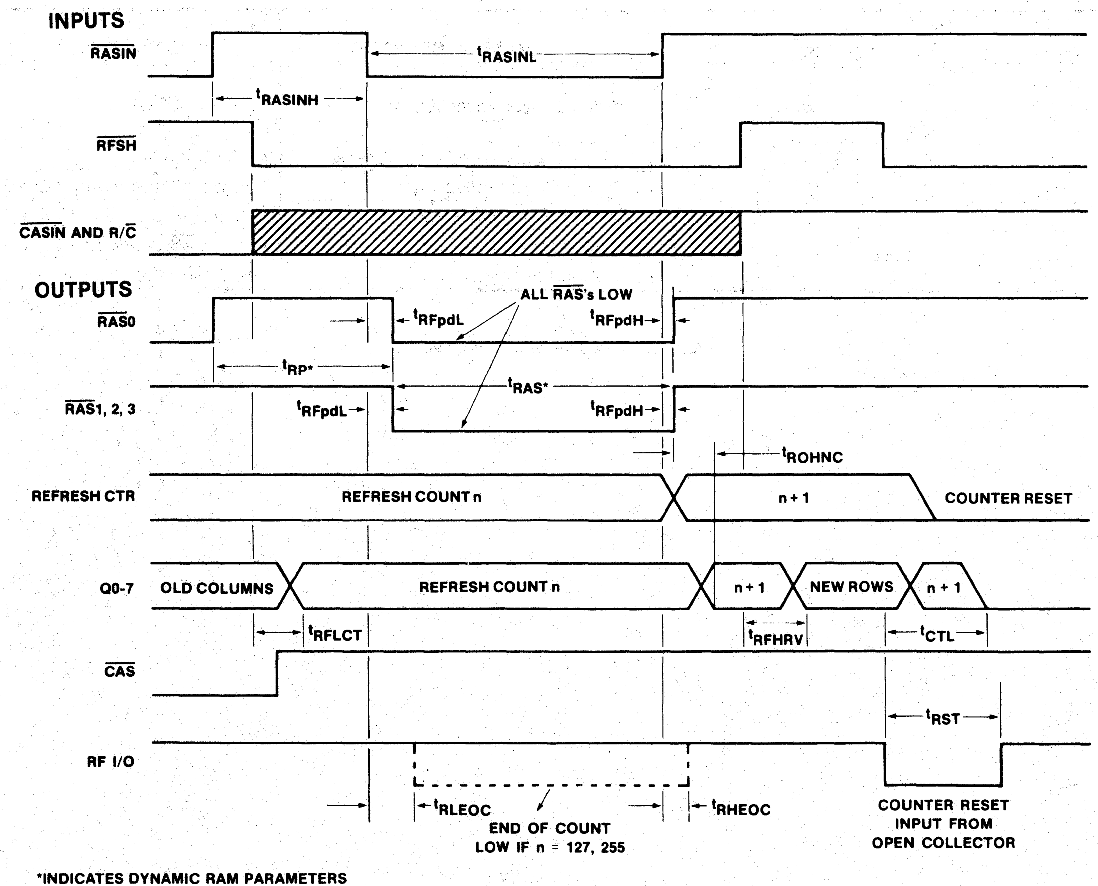


Figure 2. External Control Refresh Cycle (Modes 0, 1, 2)

Mode 4—Externally Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in Figure 3.

Output Address Selection

Refer to Figure 4a. With M2 ($\overline{\text{RFSH}}$) and R/$\overline{\text{C}}$ high, the row address latch contents are transferred to the multiplexed address bus output Q0-Q7, provided $\overline{\text{CS}}$ is set low. The column address latch contents are output after R/$\overline{\text{C}}$ goes low. $\overline{\text{RASIN}}$ can go low after the row addresses have been set up on Q0-Q7. This selects one of the $\overline{\text{RAS}}$ outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{\text{C}}$ can go low so that about 40 ns later column addresses appear on the Q outputs.

Automatic $\overline{\text{CAS}}$ Generation

In a normal memory access cycle $\overline{\text{CAS}}$ can be derived from inputs $\overline{\text{CASIN}}$ or R/C. If $\overline{\text{CASIN}}$ is high, then R/$\overline{\text{C}}$ going low switches the address output drivers from rows to columns. $\overline{\text{CASIN}}$ then going low causes $\overline{\text{CAS}}$ to go low approximately 40 ns later, allowing $\overline{\text{CAS}}$ to occur at a predictable time (see Figure 4b). For maximum system speed, $\overline{\text{CASIN}}$ can be kept low, since $\overline{\text{CAS}}$ will automatically occur approximately 20 ns after the column addresses are valid, or about 60 ns after R/$\overline{\text{C}}$ goes low (see Figure 4a). Most DRAMs have a column address set-up time before $\overline{\text{CAS}}$ (t_{ASC}) of 0 ns or −10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/$\overline{\text{C}}$ can go low a time delay (t_{RPDL} + t_{RAH} − t_{RHA}) after RASIN goes low, where t_{RAH} is the Row-Address hold-time of the DRAM.

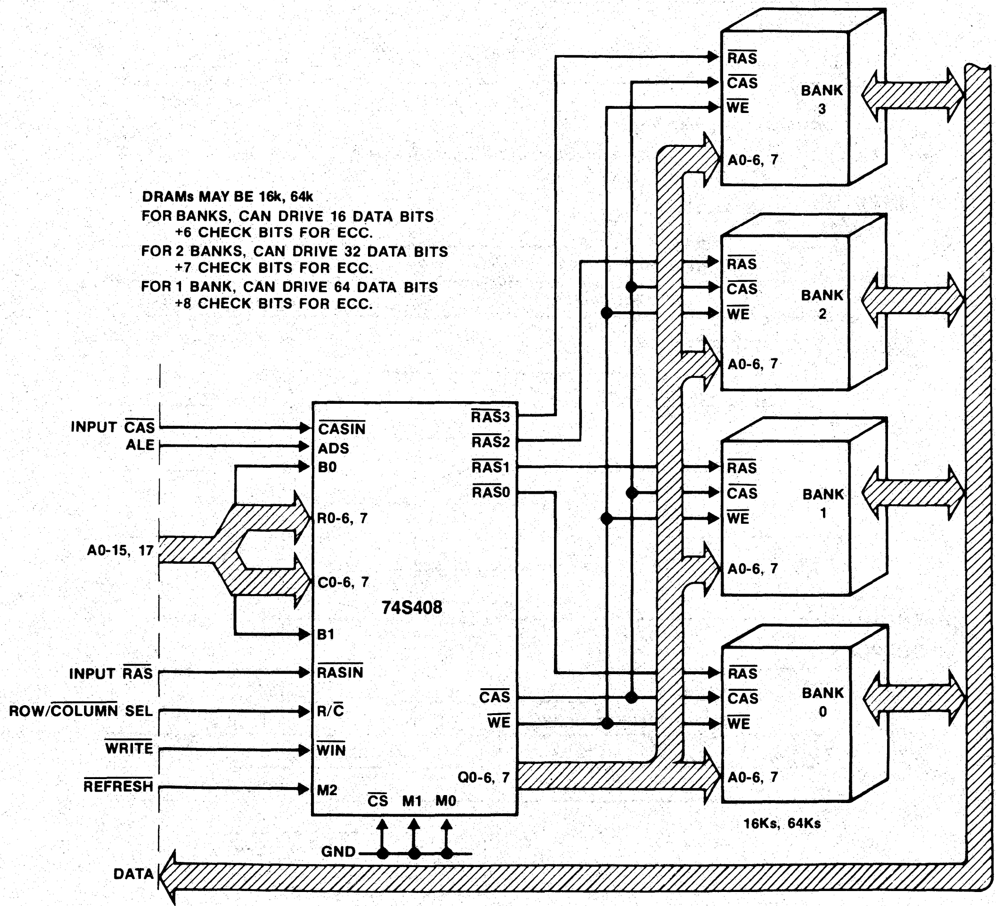
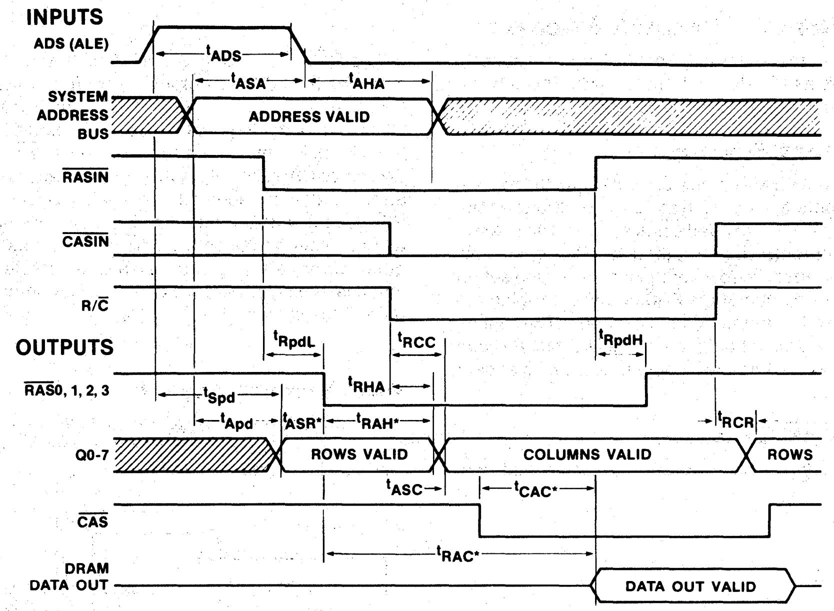
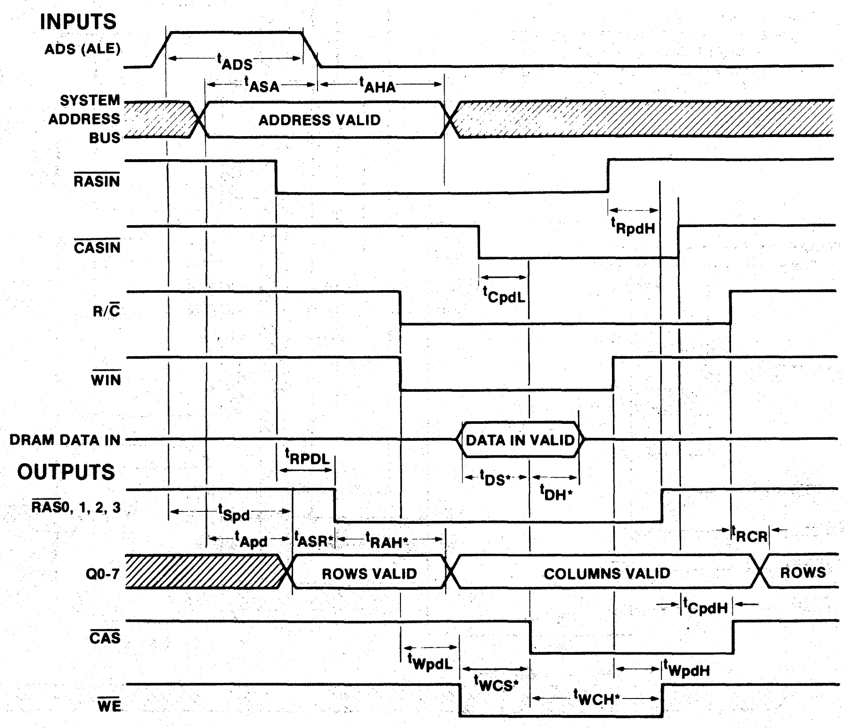


Figure 3. Typical Application of 74S408 Using Externally Controlled Access and Refresh in Modes 0 and 4



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4a. Read Cycle Timing (Mode 4)



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4b. Write Cycle Timing (Mode 4)

Mode 5—Automatic Access

In the Auto Access mode all outputs except WE are initiated from RASIN. Inputs R/C and CASIN are unnecessary and the output control signals are derived internally from one input signal (RASIN) minimizing timing-skew problems, thereby reducing memory-access time substantially and allowing the use of slower DRAMs.

Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a RAS must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then CAS occurs. This is all performed automatically by the 74S408 in this mode.

Provided the input address is valid as ADS goes low, RASIN can go low any time after ADS. This is because the selected RAS occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S408. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S408 in this mode (with ADS and RASIN edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 5a).

Next, the row address is disabled after t_{RAH} (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and t_{ASC} later, CAS occurs. The only other control input required is WIN. When a write cycle is required, WIN must go low at least 30 ns before CAS Is output low.

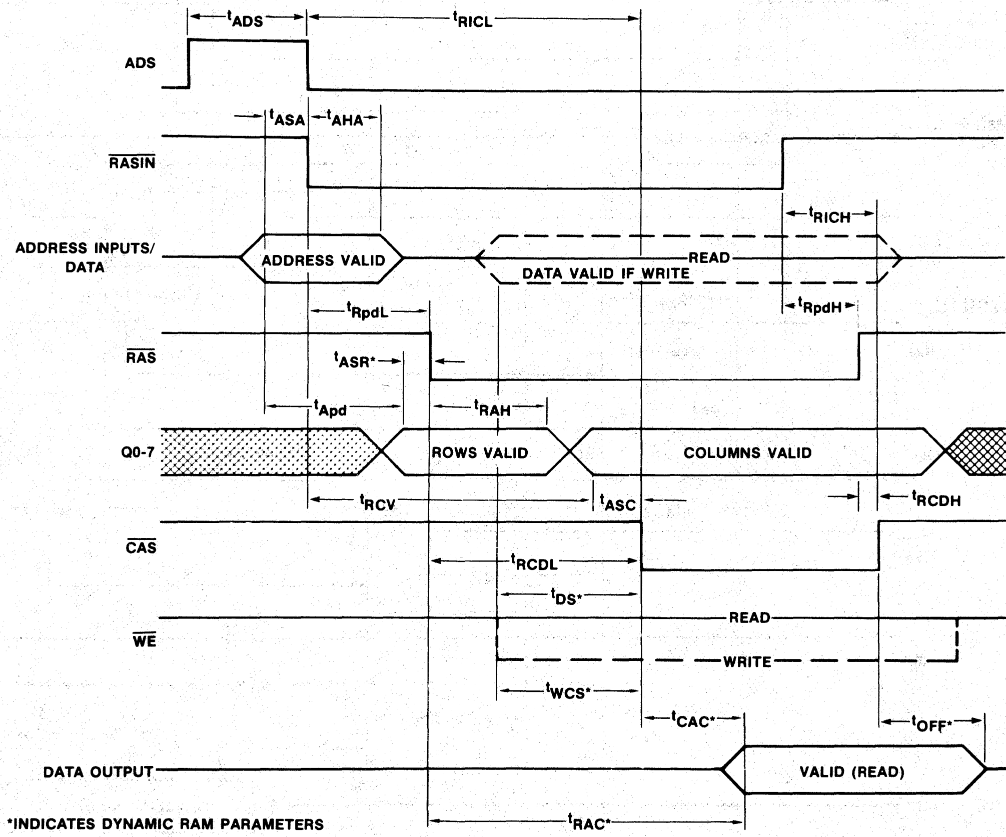


Figure 5a. Modes 5, 6 Timing (CASIN High in Mode 6)

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs. This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

Mode 6—Fast Automatic Access

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20 ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10 ns to 15 ns) in applications requiring fast access times; $\overline{RASIN}$ to $\overline{CAS}$ is typically 105 ns.

In this mode, the R/$\overline{C}$ pin is not used, but $\overline{CASIN}$ is used to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 5b. This is desirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by $\overline{CASIN}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{CASIN}$ subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, $\overline{CASIN}$ should be set high in Mode 6.

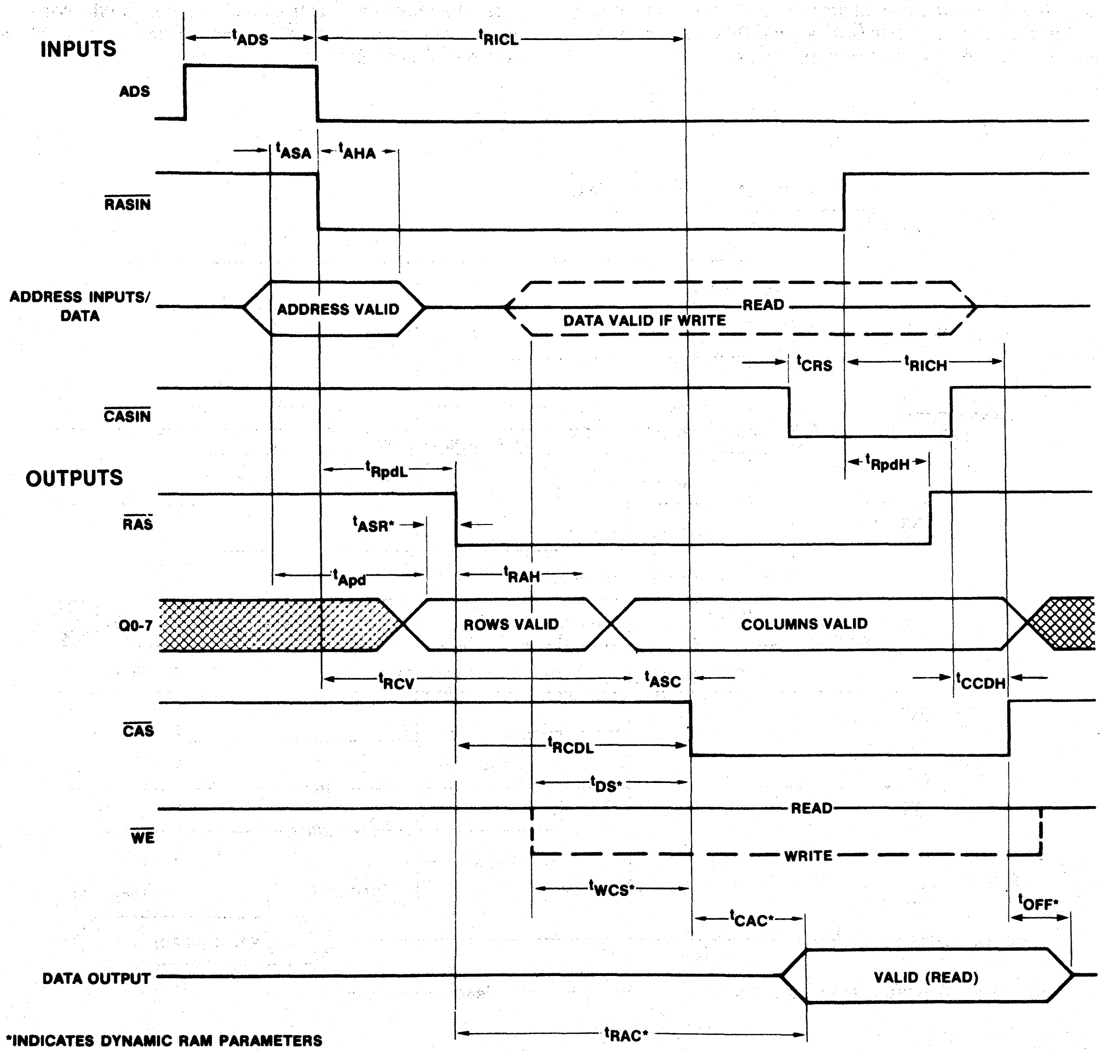


Figure 5b. Mode 6 Timing, Extended CAS

Mode 7—Set End-of-Count

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same EOC is 127; with B1 = 0 and B0 = 1, EOC is 255; and with B1 = 1 and B0 = 0, EOC is 127. This selected value of EOC will be used until the next Mode 7 selection. At power-up the EOC is automatically set to 127 (B1 and B0 set to 11).

BANK SELECT (STROBED BY ADS)		END OF COUNT SELECTED
B1	B0	
0	0	127
0	1	255
1	0	127
1	1	127

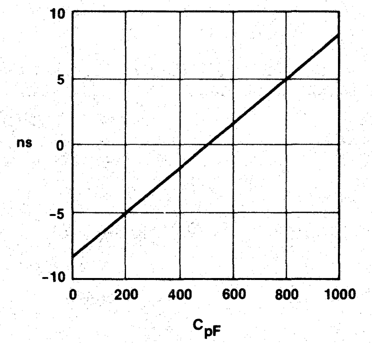


Figure 6. Change in Propagation Delay vs Loading Capacitance Relative to a 500pF Load

SN74S408/-2 Specifications:

Absolute Maximum Ratings (Note 1)

Supply voltage V_{CC} .... −0.5 V to 7.0 V
Storage temperature range .... −65° to +150°C
Input voltage .... −1.5 V to 5.5 V
Output current .... 150 mA
Lead temperature (soldering, 10 seconds) .... 300°C

NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S408			'S408-2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75		5.25	4.25		5.25	V
T_A	Operating free-air temperature		0		+75	0		+75	°C
t_{ASA}	Address setup time to ADS	Figures 4a,4b,5a,5b	15			15			ns
t_{AHA}	Address hold time from ADS	Figures 4a,4b,5a,5b	15			15			ns
t_{ADS}	Address strobe pulse width	Figures 4a,4b,5a,5b	30			30			ns
t_{RHA}	Row address held from column select	Figure 4a	10			10			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 2	50			50			ns
t_{RST}	counter reset pulse width	Figure 2	70			70			ns

Electrical Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C ≤ T_A ≤ 75°C Typicals are for V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS. R/$\overline{C}$ only.	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_{IRSI}	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mA
I_{ICTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselect		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS. R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0	V		
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	V_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_{1D}	Output high drive current except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{OD}	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	Three-state output current (address outputs)	0.4V ≤ V_{OUT} ≤ 2.7V, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		210	285	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

Switching Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C T_A 75°C See Figure 7 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408 MIN	'S408 TYP	'S408 MAX	'S408-2 MIN	'S408-2 TYP	'S408-2 MAX	UNIT
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	95	125	160	75	100	130	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	80	105	140	65	90	115	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	40	48	60	40	48	60	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	50	63	80	50	63	80	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		98	125		75	100	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b		78	105		65	85	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5a		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5b	40	54	70	40	54	70	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figure 5a		90	120		30	105	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figure 5a		75	105		70	90	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	20	27	35	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	15	23	32	15	23	32	ns
t_{APDL}	Address input to output low delay	Figures 4a,4b,5a,5b		25	40		25	40	ns
t_{APDH}	Address input to output high delay	Figures 4a,4b,5a,5b		25	40		25	40	ns
t_{SPDL}	Address strobe to address output low	Figure 4b,4a		40	60		40	60	ns
t_{SPDH}	Address strobe to address output high	Fibure 4b,4a		40	60		40	60	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	25	30	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	30	60	15	30	60	ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (RiC) low in Mode 4)	Figure 4b	32	41	58	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 4b	25	39	50	25	39	50	ns
t_{RCC}	Column select to column address valid	Figure 4a		40	58		40	58	ns
t_{RCR}	Row select to row address valid	Figure 4a,4b		40	58		40	58	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 2			100			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	35	50	70	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	30	40	55	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	CS = X , Figure 2		47	60		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figure 2		45	60		45	60	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figure 2		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	C_L = 50pF, Figure 2			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	C_L = 50pF, Figure 2			80			80	ns
t_{RAHI}	Row address hold time (Mode 5)	Figure 5a	30			20			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 5a,5b	20			12			ns
t_{ASC}	Column address setup time (Mode 5)	Figure 5a	8			3			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 5a,5b	6			3			ns
t_{RHA}	Row address held from column select	Figure 4a	10			10			ns
t_{CRS}	$\overline{Casin}$ setup time to $\overline{Rasin}$ high (Mode 6)	Figure 5b	35			35			ns

Switching Characteristics: (Cont.)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408 MIN	'S408 TYP	'S408 MAX	'S408-2 MIN	'S408-2 TYP	'S408-2 MAX	UNIT
	THREE-STATE PARAMETER								
t_{ZH}	$\overline{CS}$ low to address output high from HI—Z	Figure 7 R1 = 3.5k R2 = 1.5K		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15p, Figure 7 R2 = 1k, S1 open		20	40		20	40	ns
T_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figure 7 R1 = 3.5k R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figure 7 R1 = 1k, S2 open		25	50		25	50	ns
T_{HZH}	$\overline{CS}$ low to control output high from Hi-Z high	Figure 7 R2 = 750 Ω S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output Hi-Z high from high	C_L = 15pF Figure 7 R2 = 750Ω, S1 open		40	75		45	75	ns
t_{HZL}	$\overline{CS}$ low to control output low from Hi-Z high*	Figure 7, S1, S2 open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output Hi-Z high from low*	C_L = 15pF Figure 7 R2 = 750Ω S1 open		50	80		50	80	ms

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8, $\overline{WE}$ C_L = 500 pF; $\overline{RAS}$ C_L = 150 pF; $\overline{CAS}$ C_L = 600pF unless otherwise noted.

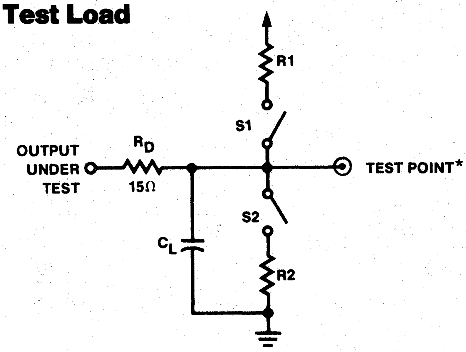
Note 2: All typical values are for T_A = 25° and V_C = 5.0V.

Note 3: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, t_R = t_F = 2.5 ns, f = 2.5 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

Test Load



R_1, R_2 = 4.7K Except as specified

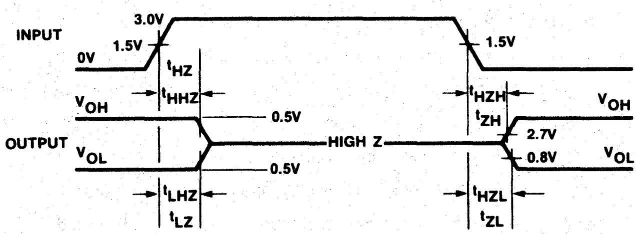


Figure 7. Waveform

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

SN74S408-3 Specifications:

Absolute Maximum Ratings (Note 1)

Supply voltage V_{CC} .... -0.5 V to 7.0 V
Storage temperature range .... -65° to +150° C
Input voltage .... -1.5 V to 5.5 V
Output current .... 150 mA
Lead temperature (soldering, 10 seconds) .... 300° C

NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S408-3 MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
T_A	Operating free-air temperature		0		+75	°C
t_{ASA}	Address setup time to ADS	Figures 4a,4b,5a,5b	15			ns
t_{AHA}	Address hold time from ADS	Figures 4a,4b,5a,5b	15			ns
t_{ADS}	Address strobe pulse width	Figures 4a,4b,5a,5b	30			ns
t_{RHA}	Row address held from column select	Figure 4a	10			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 2	50			ns
t_{RST}	counter reset pulse width	Figure 2	70			ns

Electrical Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C ≤ T_A ≤ 75°C Typicals are for V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS. R/$\overline{C}$ only.	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_{IRSI}	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mA
I_{ICTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselect		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS. R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0	V		
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	I_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_{1D}	Output high drive current except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{0D}	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	THREE-STATE output current (address outputs)	0.4V ≤ V_{OUT} ≤ 2.7V, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		210	285	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

** These are absolute voltages with respect to pins 13 or 38 on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

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Switching Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C T_A 75°C See Figure 7 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408-3 MIN	TYP	MAX	UNIT
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	95	125	185	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	80	105	160	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	40	48	70	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	50	63	95	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		98	145	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b		78	120	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5a		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5b	40	54	80	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figure 5a		90	140	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figure 5a		75	120	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	20	27	40	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	15	23	37	ns
t_{APDL}	Address input to output low delay	Figures 4a,4b,5a,5b		25	46	ns
t_{APDH}	Address input to output high delay	Figures 4a,4b,5a,5b		25	46	ns
t_{SPDL}	Address strobe to address output low	Figure 4b,4a		40	70	ns
t_{SPDH}	Address strobe to address output high	Figure 4b,4a		40	70	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	25	35	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	30	70	ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (RiC) low in Mode 4)	Figure 4b	32	41	67	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 4b	25	39	60	ns
t_{RCC}	Column select to column address valid	Figure 4a		40	67	ns
t_{RCR}	Row select to row address valid	Figure 4a,4b		40	67	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 2			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	35	50	80	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	30	40	65	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	CS = X , Figure 2		47	70	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figure 2		45	70	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figure 2		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	C_L = 50pF, Figure 2		80	ns	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	C_L = 50pF, Figure 2			80	ns
t_{RAHI}	Row address hold time (Mode 5)	Figure 5a	30			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 5a,5b	20			ns
t_{ASC}	Column address setup time (Mode 5)	Figure 5a	8			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 5a,5b	6			ns
t_{RHA}	Row address held from column select	Figure 4a	10			ns
t_{CRS}	$\overline{Casin}$ setup time to $\overline{Rasin}$ high (Mode 6)	Figure 5b	35			ns

Switching Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C T_A 75°C See Figure 7 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408-3 MIN	TYP	MAX	UNIT
	THREE-STATE PARAMETER					
t_{ZH}	$\overline{CS}$ low to address output high from HI—Z	Figure 8 R1 = 3.5k, R2 = 1.5K		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15p, Figure 8 R2 = 1k, S1 open		20	40	ns
T_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figure 8 R1 = 3.5k, R2 = 1.5k		35	50	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figure 8, R1 = 1k, S2 open		25	50	ns
T_{HZH}	$\overline{CS}$ low to control output high from Hi-Z high	Figure 8 R2 = 750 Ω, S1 open		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output Hi-Z high from high	C_L = 15pF, Figure 8, R2 = 750Ω, S1 open		40	75	ns
t_{HZL}	$\overline{CS}$ low to control output low from Hi-Z high*	Figure 8, S1, S2 open		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output Hi-Z high from low*	C_L = 15pF, Figure 8, R2 = 750Ω, S1 open		50	80	ns

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8, $\overline{WE}$ C_L = 500 pF; $\overline{RAS}$ C_L = 150 pF; $\overline{CAS}$ C_L = 600pF unless otherwise noted.

Note 2: All typical values are for T_A = 25° and V_C = 5.0V.

Note 3: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, t_R = t_F = 2.5 ns, f = 2.5 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

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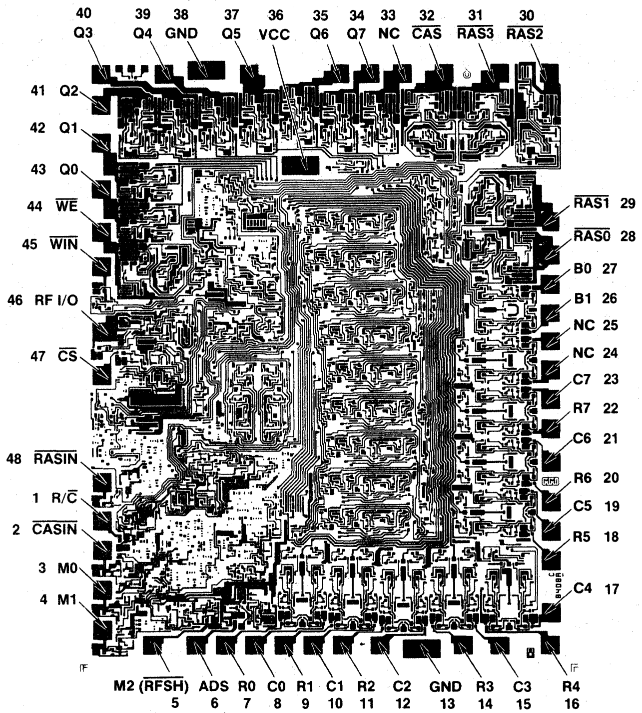
Die Configuration



Die Size: 161x129 mil^2

Multi-Mode Dynamic RAM Controller/Driver

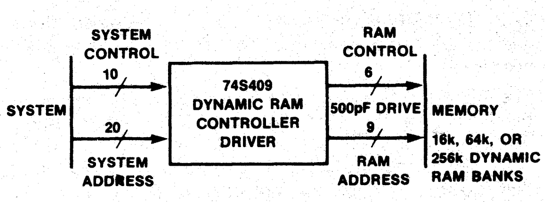
SN74S409/DP8409
SN74S409-2/DP8409-2
SN74S409-3/DP8409-3

Features/Benefits

- All DRAM drive functions on one chip have on-chip high-capacitance load drivers (specified up to 88 DRAMs)
- Drives directly all 16K, 64K and 256K DRAMs; capable of addressing up to 1M words
- Propagation delays of 25 nsec typical at 500 pF load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- Eight modes of operation support externally-controlled and automatic access and refresh, as well as special memory initialization access
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255 or 511)
- Direct replacement for National DP8409

Operating Modes

0	Externally-controlled fresh
1	Auto refresh — forced
2	Automatic burst refresh
3a	All-$\overline{RAS}$ auto write
3b	Externally-controlled All-$\overline{RAS}$ write
4	Externally-controlled access
5	Auto access, slow t_{RAH}, hidden refresh
6	Auto access, fast t_{RAH}
7	Set end of count

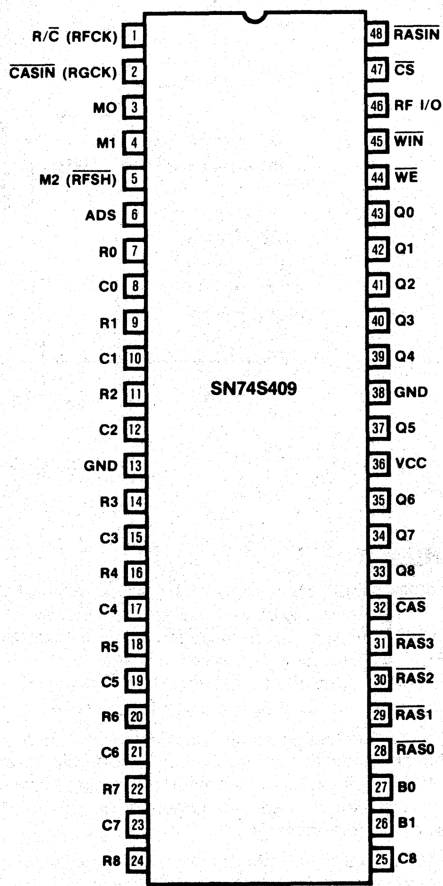


Interface Between System and DRAM Banks

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S409	N48, D48 (L52)	COM
SN74S409-2	N48, D48 (L52)	COM, SPEED OPTION
SN74S409-3	N48, D48 (L52)	COM, AC OPTION

Pin Configuration



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Block Diagram

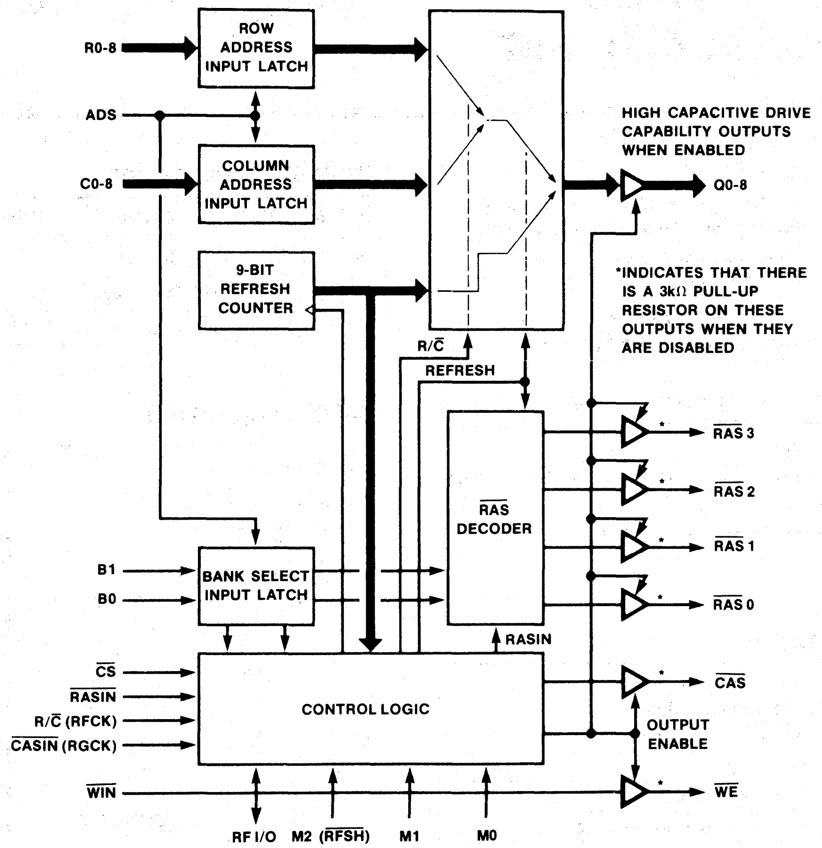

Figure 1. 74S409 Functional Block Diagram

Description

The 74S409 is a Multi-Mode Dynamic RAM Controller/Driver capable of directly driving up to 88 DRAMs. 20 address lines to the 74S409 allow it to address up to 1M words and it can drive 16K, 64K and 256K DRAMs. Since the 74S409 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, and saves board space.

The 74S409's 8 operating modes offer externally-controlled or on-chip automatic access and refresh. An on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The 74S409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. The 74S409 timing parameters are specified when driving the typical load capitance of 88 DRAMs, including trace capacitance.

The 74S409 can drive up to 4 banks of DRAMs, with each bank comprised of 16Ks, 64Ks or 256Ks. Control signal outputs $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are provided with the same driving capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the respective data outputs in three-state. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from, except in mode 3 where all $\overline{\text{RAS}}$ signals go low to allow fast memory initialization.

Pin Definitions

V_{CC} GND, GND—V_{CC} = 5V ± 5%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution is a 1-μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{\text{RAS}}_n$
B1	B0	
0	0	$\overline{\text{RAS}}_0$
0	1	$\overline{\text{RAS}}_1$
1	0	$\overline{\text{RAS}}_2$
1	1	$\overline{\text{RAS}}_3$

Table 1. Memory Bank Decode

R0-R8: Row Address Inputs.

C0-C8: Column Address Inputs.

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{\text{RAS}}$ outputs when $\overline{\text{RASIN}}$ goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-of-Count (see table 3), and select mode 3a or 3b.

Q0-Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

$\overline{\text{RASIN}}$: Row Address Strobe Input—Enables selected $\overline{\text{RAS}}_n$ output when M2 ($\overline{\text{RFSH}}$) is high (modes 4-6), and all $\overline{\text{RAS}}_n$ outputs in modes 0 and 3. $\overline{\text{RASIN}}$ input is disabled in modes 1 and 2.

R/$\overline{\text{C}}$ (RFCK)—In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/$\overline{\text{Column}}$ Select Input, selecting either the row or column address input latch onto the output bus.

$\overline{\text{CASIN}}$ (RGCK)—In modes 1, 2 and 3a, this pin is the $\overline{\text{RAS}}$ Generator Clock input. In all other modes it is $\overline{\text{CASIN}}$ (Column Address Strobe Input), which inhibits $\overline{\text{CAS}}$ output when high in Modes 3b and 4. In Mode 6 it can be used to prolong $\overline{\text{CAS}}$ output.

ADS: Address (Latch) Strobe Input—Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; latches on High-to-Low transition.

$\overline{\text{CS}}$: Chip Select Input—three-state's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.

M0, M1, M2 ($\overline{\text{RFSH}}$): Mode Control Inputs—These 3 control pins determine the 8 major modes of operation of the 74S409 as depicted in Table 2.

RF I/O $\overline{\text{RFRQ}}$ — This I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low in Modes 0, 2 and 3a when the End-of-Count output is at 127, 255, or 511 (see Table 3). In Auto-Refresh Mode (mode 5) it is the $\overline{\text{Refresh Request}}$ ($\overline{\text{RFRQ}}$) output.

$\overline{\text{WIN}}$: Write Enable Input.

$\overline{\text{WE}}$: Write Enable Output—Buffered output from $\overline{\text{WIN}}$.

$\overline{\text{CAS}}$: Column Address Strobe Output—In Modes 3a, 5, and 6, $\overline{\text{CAS}}$ transitions low following valid column address. In Modes 3b and 4, it goes low after R/$\overline{\text{C}}$ goes low, or follows $\overline{\text{CASIN}}$ going low if R/$\overline{\text{C}}$ is already low. $\overline{\text{CAS}}$ is high during refresh.

$\overline{\text{RAS}}$ 0-3: Row Address Strobe Outputs—When M2($\overline{\text{RFSH}}$) is high (modes 4-6), the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{\text{RASIN}}$ input. When M2 ($\overline{\text{RFSH}}$) is low (modes 0-3) all $\overline{\text{RAS}}_n$ outputs go low together following $\overline{\text{RASIN}}$ going low in modes 0 and 3 and automatically in modes 1 and 2.

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter.

The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid address until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the address is still valid.

In normal memory-access operation, $\overline{\text{RASIN}}$ and R/$\overline{\text{C}}$ are initially high. When the address inputs are enabled into the address latches (modes 3-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, (B0 and B1). If $\overline{\text{CS}}$ is low, all outputs are enabled. When $\overline{\text{CS}}$ goes high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S409s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{\text{CS}}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The 74S409 has timing parameters that are specified with up to 600pF loads for $\overline{CAS}$ and $\overline{WE}$, 500pF loads for Q_0-Q_8, and 150pF loads for $\overline{RAS}_n$ outputs. In a typical memory system this is equivalent to about 88 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 14. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S409 Driving Any 16K, 64K or 256K DRAMs

The 74S409 can drive any 16K, 64K, or 256K DRAMs. The on-chip 9-bit counter with selectable End-of-Count can support refresh of 128, 256 and 512 rows, while the 9 address and 4 $\overline{RAS}_n$ outputs can address 4 banks of 16K, 64K or 256K DRAMs.

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

Power-Up Initialize

When V_{CC} is first applied to the 74S409, an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

74S409 Functional Modes Description

The 74S409 operates in 8 different functional modes selected by signals M_0,M_1,M_2. Mode 3 splits further to modes 3a and 3b determined by signals B_0,B_1 in mode 7.

Mode 0 and mode 1 are generally used as Refresh modes for mode 4 and mode 5 respectively, and therefore will be described as mode-pairs 0,4 and 1,5.

Mode 6 is a fast access made for very fast DRAMs and mode 7 is used only to determine choice of mode 3a or 3b and for setting End-of-Count for the refresh modes.

MODE	(RFSH) M2	M1	M0	MODE OF OPERATION	CONDITIONS
0	0	0	0	Externally-controlled refresh	RF I/O = $\overline{EOC}$
1	0	0	1	Auto refresh—forced	RF I/O = Refresh request ($\overline{RFRQ}$)
2	0	1	0	Automatic burst refresh	RF I/O = $\overline{EOC}$
3a*	0	1	1	All-$\overline{RAS}$ auto write	RF I/O = $\overline{EOC}$; all $\overline{RAS}$ active
3b*	0	1	1	Externally-controlled All-$\overline{RAS}$ write	All-$\overline{RAS}$ active
4	1	0	0	Externally-controlled access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto access, slow t_{RAH}, hidden refresh	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto access, fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set end of count; determines mode 3a or 3b	See Table 3 for Mode 7

*Mode 3a is selected by setting B_0,B_1 to 01, 00, or 10 in mode 7.
*Mode 3b is selected by setting B_1,B_0 to 11 in mode 7.

Table 2. 74S409 Mode Select Options

Mode 0 — Externally-Controlled Refresh
Mode 4 — Externally-Controlled Access

Modes 0 and 4 facilitate external control of all timing parameters associated with the DRAMs. These modes are independent modes of operation though generally used together in the same application as shown in Figure 2.

Mode 0—Externally-Controlled Refresh

In this mode the input address latches are disabled from the address outputs and the refresh counter is enabled. All $\overline{RAS}$ outputs go low following $\overline{RASIN}$ and refresh the enabled row in all four banks. $\overline{CASIN}$ and R/$\overline{C}$ inputs are not used and $\overline{CAS}$ is inhibited. The refresh counter increments when either $\overline{RASIN}$ or M2 ($\overline{RFSH}$) switch high while the other is still low.

RF I/O goes low when the count equals End-of-Count (as set in mode 7), and $\overline{RASIN}$ is low. The 9-bit counter will always roll-over to zero at 512, regardless of End-of-Count. However, the counter can be reset at any time by driving RF I/O low through an external open-collector.

During refresh, $\overline{RASIN}$ and M2 ($\overline{RFSH}$) can transition low simultaneously because the refresh counter becomes valid on the output bus t_{RFLCT} after $\overline{RFSH}$ goes low, which is a shorter time than t_{RFPDL}. This means the counter address is valid on the Q outputs before $\overline{RAS}$ occurs on all $\overline{RAS}$ outputs, strobing the counter address into that row of all the DRAMs (see Figure 2.). To perform externally-controlled burst refresh, $\overline{RFSH}$ initially can again have the same edge as $\overline{RASIN}$, but then maintains a low state, since $\overline{RASIN}$ going low-to-high increments the counter (performing the burst refresh).

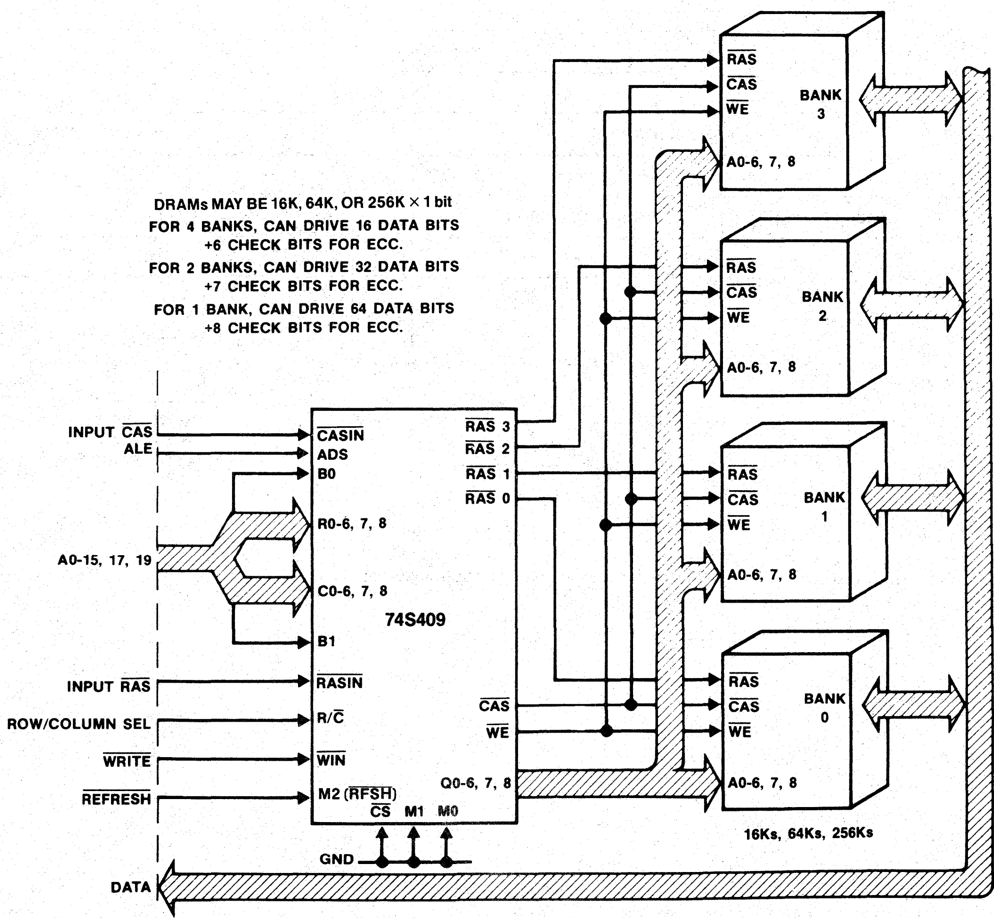

Figure 2. Typical Application of 74S409 Using Externally-Controlled Access and Refresh in Modes 0 and 4

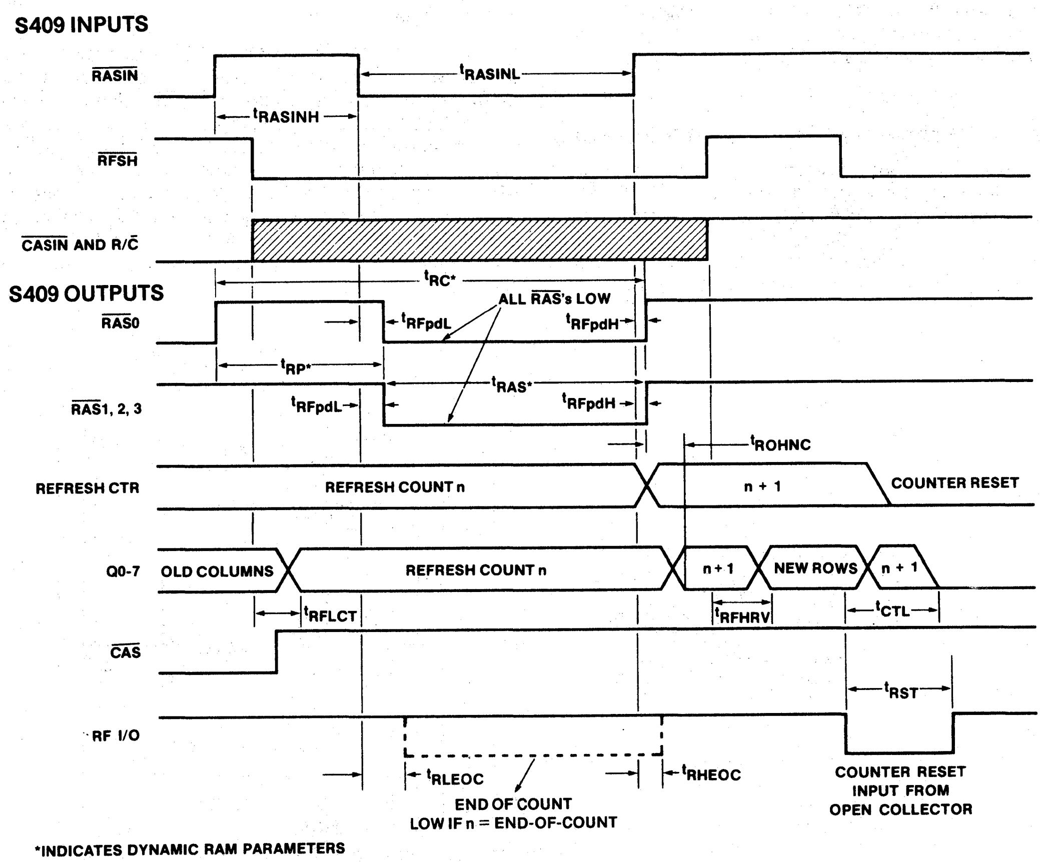

Figure 3. External Control Refresh Cycle (Mode 0)

Mode 4 — Externally-Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. Figures 4 and 5 show the timing for read and write cycles.

Output Address Selection

In this mode $\overline{CS}$ has to be low at least 50 nsec before the outputs will be valid. With R/$\overline{C}$ high, the row address latch contents are transfered to the multiplexed address bus output Q0-Q8. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0-Q8, and enables one $\overline{RAS}$ output selected by signals B0, B1 to strobe the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 nsec later, the column address appears on the Q output.

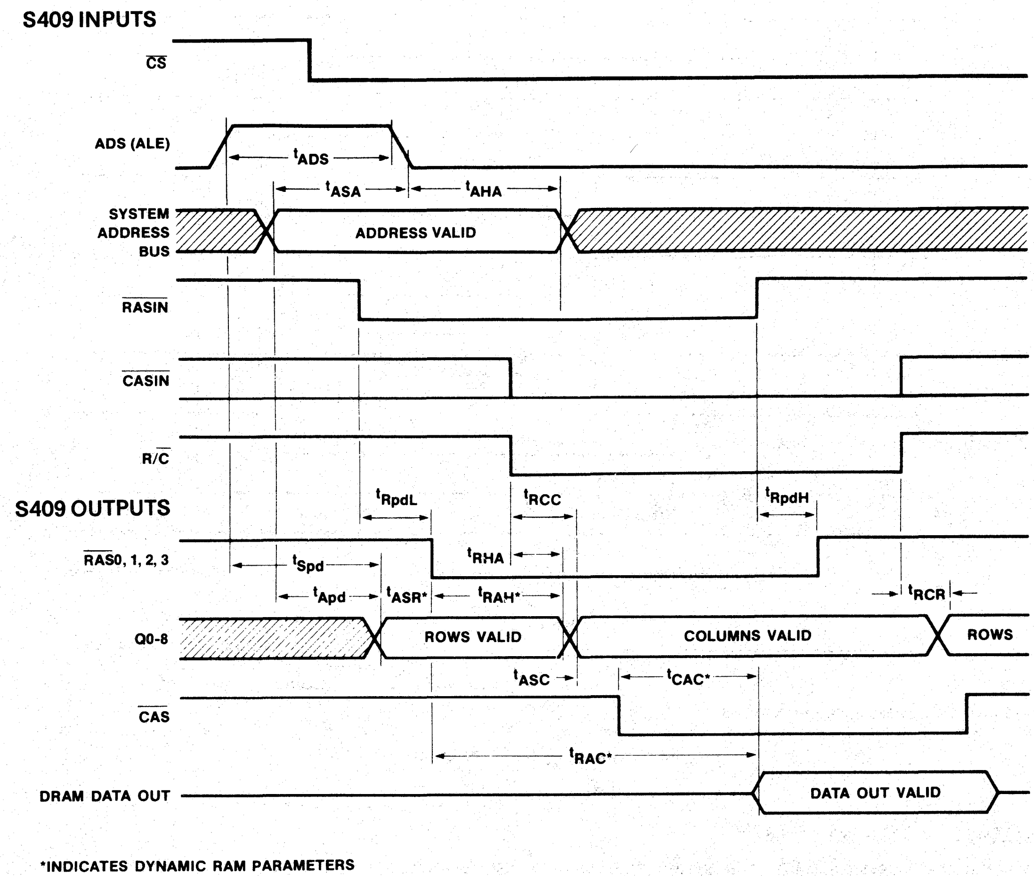

Figure 4. Read Cycle Timing (Mode 4)

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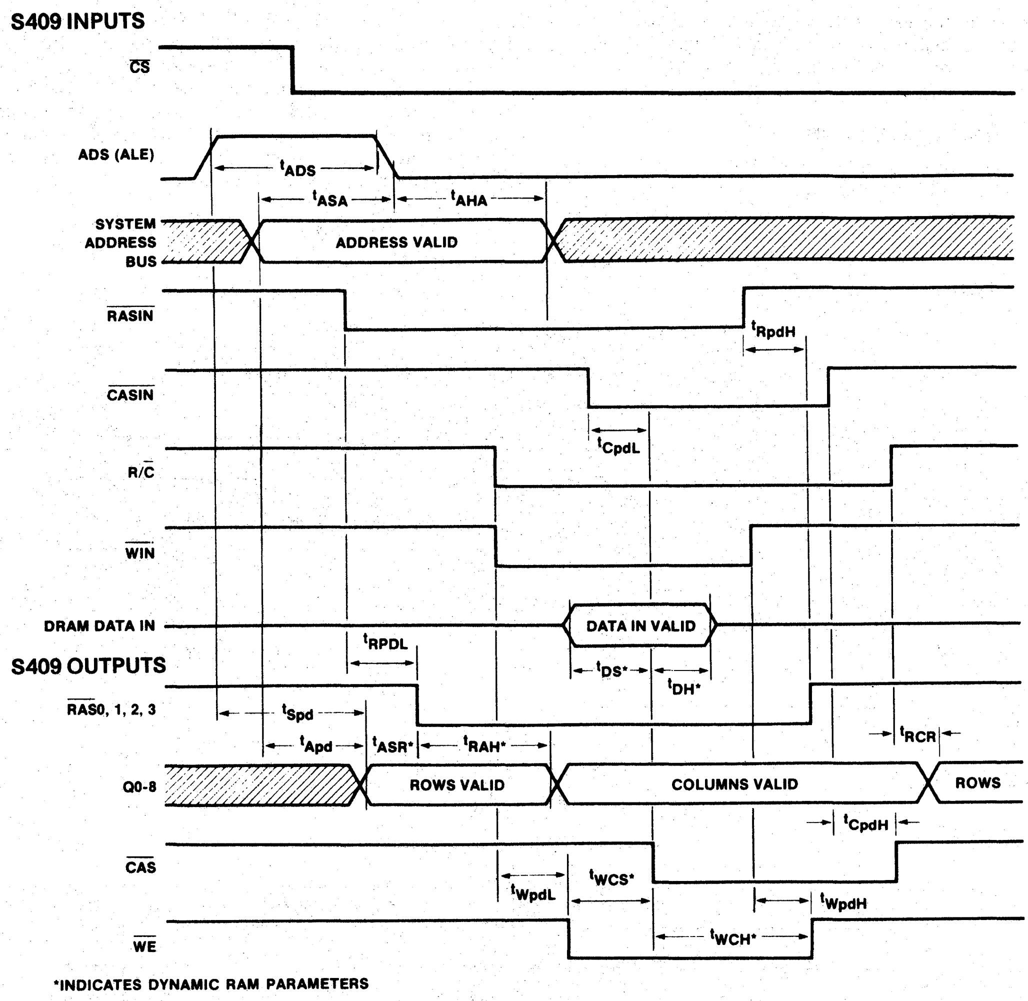


Figure 5. Write Cycle Timing (Mode 4)

Automatic $\overline{CAS}$ Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/$\overline{C}$. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see Figure 5). For maximum system speed, $\overline{CASIN}$ can be kept low, since $\overline{CAS}$ will automatically occur approximately 60 ns after R/$\overline{C}$ goes low (see Figure 4). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or −10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/$\overline{C}$ can go low a time delay ($t_{RPDL} + t_{RAH} - t_{RHA}$) after $\overline{RASIN}$ goes low, where t_{RAH} is the Row-Address hold-time of the DRAM, and $\overline{CASIN}$ can go low $t_{RCC} - t_{CPOL} + t_{ASC}$ (min.) after R/$\overline{C}$ goes low (see t_{DiF1}, t_{DiF2} switching characteristics).

Mode 1 — Automatic Forced Refresh
Mode 5 — Automatic Access with Hidden Refresh

Mode 1 and Mode 5 are generally used together incorporating the advantages of the "hidden refresh" performed in mode 5 with the possibiity to force a refresh by changing to mode 1. An advantage of the Automatic Access over the Externally-Controlled Access is the reduced memory access time, due to the fact that the output control signals are derived internally from one input signal ($\overline{\text{RASIN}}$).

Hidden and Forced Refresh

Hidden Refresh is a term describing memory refresh performed when the system does not access the portion of memory controlled by the 74S409 ($\overline{\text{CS}}$ = 1). A hidden refresh will occur once per Refresh Clock (RFCK) cycle provided $\overline{\text{CS}}$ went high and $\overline{\text{RASIN}}$ went low. If no hidden refresh occurred while RFCK was high, the RF I/O ($\overline{\text{RFRQ}}$) goes low immediately after RFCK goes low, indicating to the system when a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low by driving M2 ($\overline{\text{RFSH}}$) low, thereby changing mode of operation to Mode 1.

The Refresh Request on RF I/O ($\overline{\text{RFRQ}}$) is terminated as soon as $\overline{\text{RAS}}$ goes low, indicating to the system that the foced refresh has been done. The system should then drive M2 ($\overline{\text{RFSH}}$) high, changing the mode of operation back to Mode 5 (see Figure 6).

Mode 1 — Automatic Forced Refresh

In Mode 1, the R/$\overline{\text{C}}$ (RFCK) pin functions as RFCK (refresh cycle clock) instead of R/$\overline{\text{C}}$, and $\overline{\text{CAS}}$ remains high. If RFCK is kept permanently high then whenever M2 ($\overline{\text{RFSH}}$) goes low, an externally-controlled refresh will occur and all $\overline{\text{RAS}}$ outputs will follow $\overline{\text{RASIN}}$, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but can be set low externally through an open-collector driver, to reset the refresh counter.

If RFCK is an input clock, one and only one refresh cycle must take place every RFCK cycle. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O (Refresh Request) goes low immediately after RFCK goes low, indicating to the system that a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low The Refresh Request signal on RF I/O may be connected to a Hold or Bus Request input to the system. The system acknowledges the Hold or Bus Request when ready, and outputs Hold Acknowledge or Bus Request Acknowledge. If this is connected to the M2 ($\overline{\text{RFSH}}$) pin, a forced-refresh cycle will be initiated by the S409, and $\overline{\text{RAS}}$ will be internally generated on all four $\overline{\text{RAS}}$ outputs, strobing the refresh counter contents on the address ouputs into all the DRAMs. An external $\overline{\text{RAS}}$ Generator Clock (RGCK) is requred for this function. It is fed to the $\overline{\text{CASIN}}$ (RGCK) pin, and may be up to 10 MHz. Whenever M2 goes low (inducing a forced refresh), $\overline{\text{RAS}}$ remains high for one to two periods of RGCK, depending on when M2 goes low relative to the high-to-low triggering edge of RGCK; $\overline{\text{RAS}}$ then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to $\overline{\text{RAS}}$ going low, M2 should go low t_{RFSRG} before the next falling edge of RGCK. The Refresh Request on RF I/O is terminated as $\overline{\text{RAS}}$ begins, so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh $\overline{\text{RAS}}$ will have ended, and normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh $\overline{\text{RAS}}$ end in less than 2 periods of RGCK from the time $\overline{\text{RAS}}$ went low, then M2 may go high earlier than t_{FRQH} after RF I/O goes high and $\overline{\text{RAS}}$ will go high t_{RFRH} after M2.

Mode 5 – Automatic Access with Hidden Refresh

In this mode all address outputs, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are initiated from $\overline{\text{RASIN}}$ making the DRAM access appear similar to static RAM access. The hidden refresh feature enables DRAM refresh accomplished with no time-loss to the system.

Provided the input address is valid as ADS goes low, $\overline{\text{RASIN}}$ can go low any time after ADS. This is because the selected $\overline{\text{RAS}}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and $\overline{\text{RASIN}}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASR} before ADS went low (see Figure 7).

Next, the row address is disabled t_{RAH} after $\overline{\text{RAS}}$ goes low (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and (t_{ASC} later,) $\overline{\text{CAS}}$ occurs. The only other control input required is $\overline{\text{WIN}}$. When a write cycle is required, $\overline{\text{WIN}}$ must go low at least 30 ns before $\overline{\text{CAS}}$ is output low.

This gives a total typical delay from: input address valid to $\overline{\text{RASIN}}$ (15 ns); to $\overline{\text{RAS}}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{\text{CAS}}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{\text{RASIN}}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

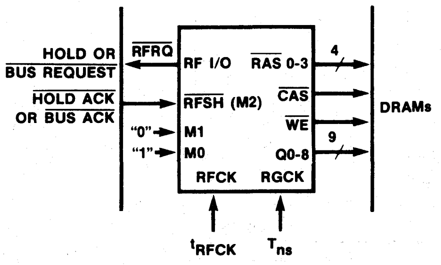
Refreshing

In this mode R/$\overline{\text{C}}$ (RFCK) functions as Refresh Clock and $\overline{\text{CASIN}}$ (RGCK) functions as $\overline{\text{RAS}}$ Generator Clock.

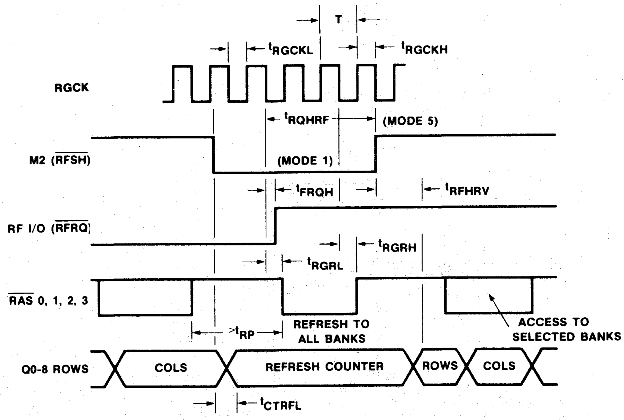
One refresh cycle must occur during each refresh clock period, and then the refresh address must be incremented before the next refresh cycle. As long as 128 rows are refreshed every 2 ms (one row every 16 μs), all 16K and 64K DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than 16 μs. RFCK going high sets an internal refresh-request flipflop. First the 74S409 will attempt to perform a hidden refresh so that the system thruput will not be affected. If, during the time RFCK is high, $\overline{\text{CS}}$ on the 74S409 goes high and $\overline{\text{RASIN}}$ occurs, a hidden refresh will occur. In this case, $\overline{\text{RASIN}}$ should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the 74S409 will perform a refresh. The refresh counter is enabled to the address outputs whenever $\overline{\text{CS}}$ goes high with RFCK high, and all $\overline{\text{RAS}}$ outputs follow $\overline{\text{RASIN}}$. If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flipflop is reset so on further refresh can occur until the next RFCK period starts with the positive-going edge of RFCK (see Figure 6). $\overline{\text{RASIN}}$ should go low at least 20 ns before RFCK goes low, to ensure occurrence of the hidden refresh.

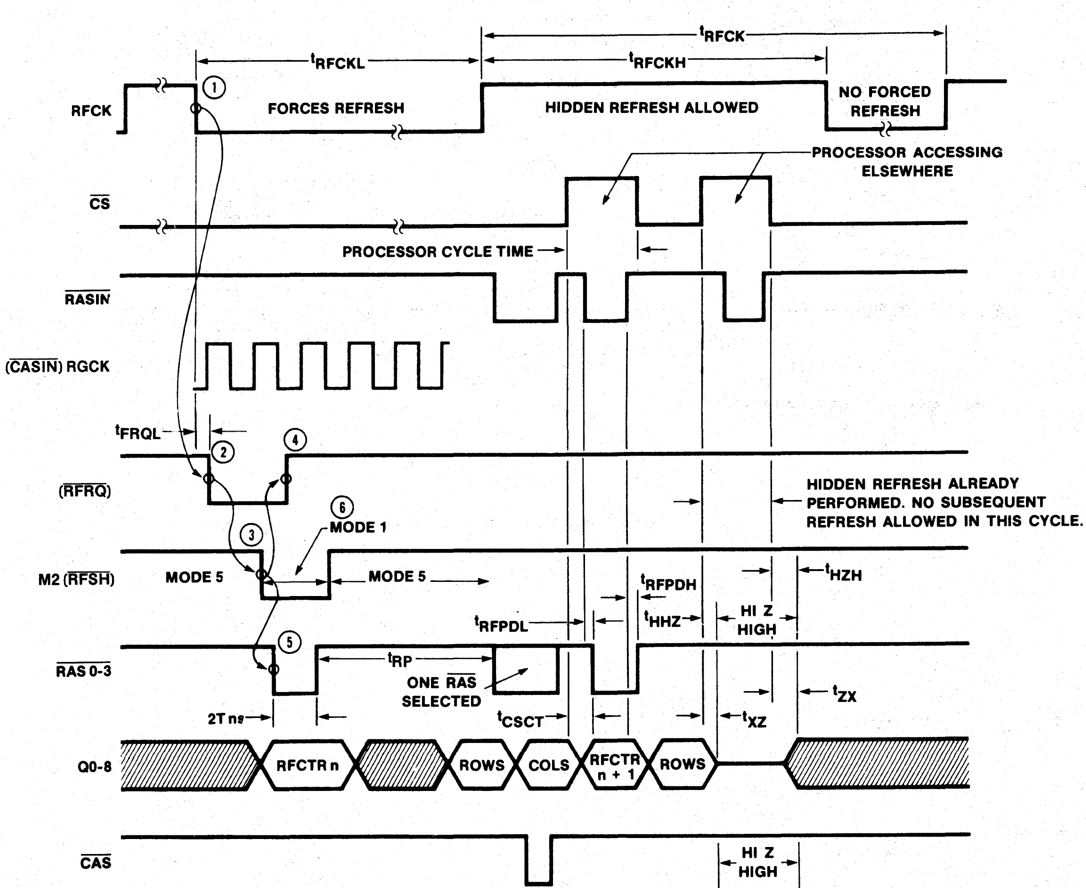
To determine the probability of a hidden refresh occurring, goes low, (and the internal-request flipflop has not been for 8μs, then the system has 20 chances to not select the 74S409. If during this time a hidden refresh did not occur, then the 74S409 forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After RFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 ($\overline{\text{RFSH}}$) low does the 74S409 initiate a forced refresh (which is performed automatically). Refer to Mode 1, and Figure 6. The internal refresh request flipflop is then reset.

Figure 6 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and $\overline{\text{CS}}$ again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic "1") and the address outputs go three-state until $\overline{\text{CS}}$ again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50 percent; in fact, the low-time should be designed to be a minimum. This is determined by the worst-case time (required by the system) to respond to the 74S409's forced-refresh request.



$t_{RFCK} \leq 2$ ms/128 = 15.6 μs





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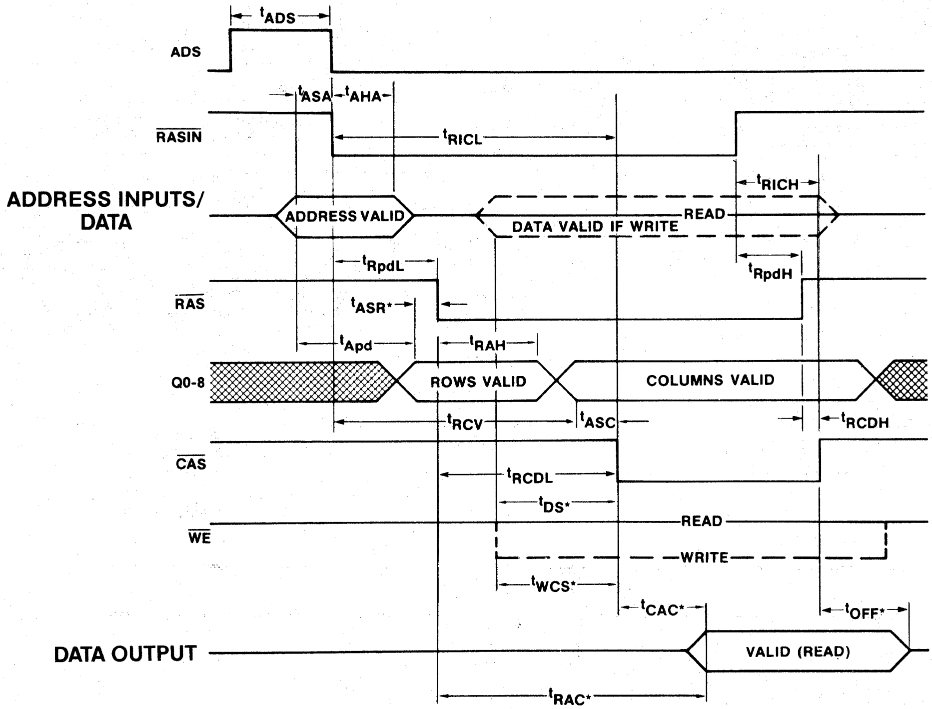
1. RFCK GOES LOW
2. RFRQ GOES LOW IN NO HIDDEN REFRESH OCCURRED WHILE RFCK WAS HIGH
3. M2 (RFSH) DRIVEN LOW EXTERNALLY
4. REFRESH REQUEST RELEASED
5. RAS 0-3 GO LOW TO PERFORM REFRESH
6. M2 (RFSH) RELEASED

Figure 6. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing



*INDICATES DYNAMIC RAM PARAMETERS

Figure 7. Mode 5 Timing

Mode 2 — Automatic Burst Refresh

This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2 ms (see Figure 8). When the 74S409 enters this mode, $\overline{\text{CASIN}}$ (RGCK) becomes the $\overline{\text{RAS}}$ Generator Clock (RGCK), and $\overline{\text{RASIN}}$ is disabled. $\overline{\text{CAS}}$ remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last $\overline{\text{RAS}}$ has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to indicate the End-of-Burst condition.

The signal on all four $\overline{\text{RAS}}$ outputs is just a divide-by-four of RGCK; in other words, if RGCK has a 100 ns period, $\overline{\text{RAS}}$ is high and low for 200 ns each cycle. The refresh counter increments at the end of each $\overline{\text{RAS}}$, starting from the count it contained when the mode was entered. If this was zero then for a RGCK with a 100 ns period with End-of Count set to 127, RF I/O will go low after 128 x 0.4μs, or 51.2μs. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins.

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the 74S409 (set to Mode 2), causing it to perform a complete burst refresh. When end-of-bust occurs (after 26 μs), power can then be removed from the 74S409 for 2 ms, consuming an average power of 1.3% of normal operating power. No control signal glitches occur when switching power to the 74S409.

Mode 3a — All-$\overline{\text{RAS}}$ Automatic Write

Mode 3a is useful at system initialization, when the memory is being cleared (i.e., with all-zeroes in the data field and the corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All $\overline{\text{RAS}}$ outputs are activated, as in refresh, and so are $\overline{\text{CAS}}$ and $\overline{\text{WE}}$. To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations. The refresh counter is used to address the rows, and $\overline{\text{RAS}}$ is low for two RGCK cycles and high for two cycles.

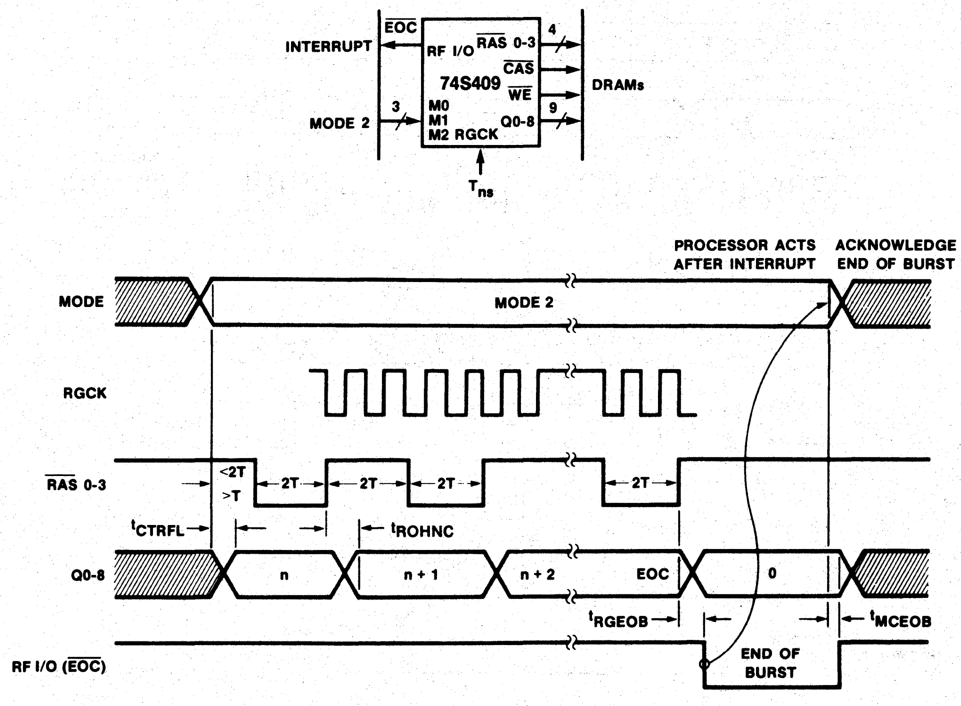
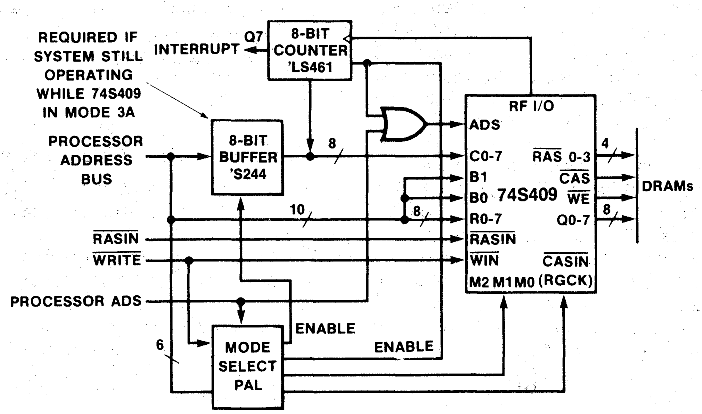


Figure 8. Auto-Burst Mode, Mode 2

8

To select this mode, B1 and B0 must have previously been set to 00, 01, or 10 in Mode 7, depending on the DRAM size. For example, for 16K DRAMs, B1 and B0 are 00. For 64K DRAMs, B1 and B0 are 01.

In this mode, R/$\overline{\text{C}}$ is disabled, $\overline{\text{WE}}$ is permanently enabled low, and $\overline{\text{CASIN}}$ (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127, 255, or 511 (as set by End-of-Count in Mode 7), and the $\overline{\text{RAS}}$ outputs are active.



74S409 Extra Circuitry Required for All-$\overline{\text{RAS}}$ Auto Write Mode, Mode 3a

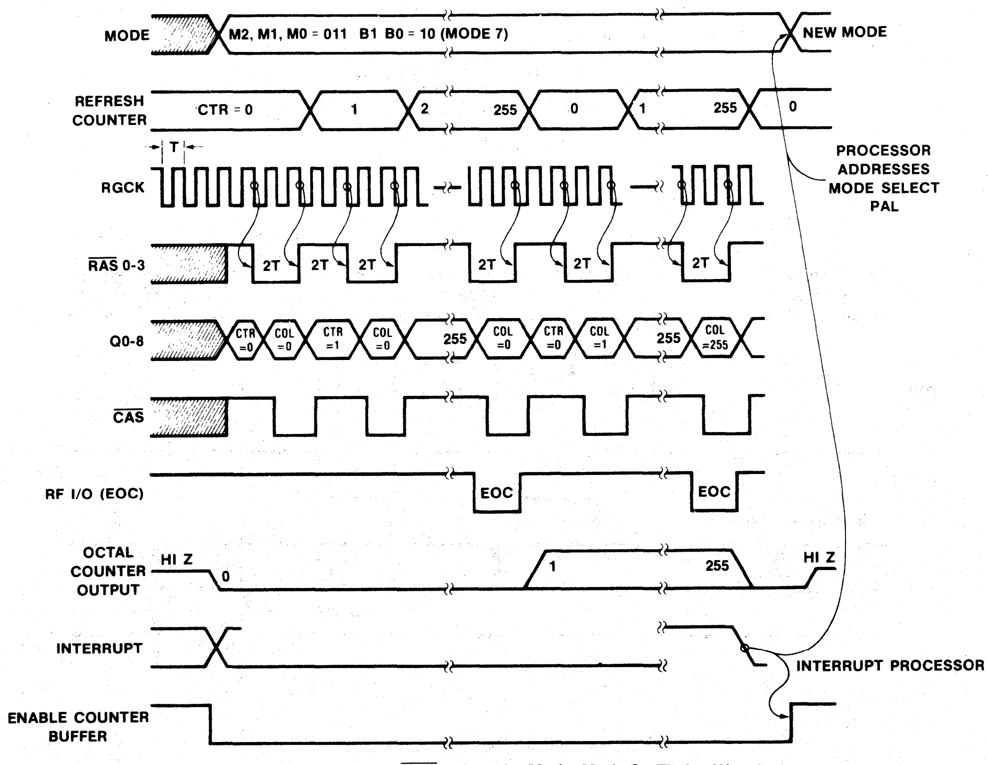


Figure 9. 74S409 All-$\overline{\text{RAS}}$ Auto Write Mode, Mode 3a, Timing Waveform

Mode 3b — Externally-Controlled All-$\overline{RAS}$ Write

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialization, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally-Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S409 for the next write cycle. This method is slower than Mode 3a, since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialization, and is not free for other initialization operations. However, initialization sequence timing is under system control, which may provide some system advantage.

Mode 4 — Externally-Controlled Access

Mode 4 is described in with mode 0 in section "Mode 0 and Mode 4."

Mode 5 — Automatic Access with Hidden Refresh

See description of mode 0 and mode 5.

Mode 6 — Fast Automatic Access

The Fast Automatic Access mode can only be used with fast DRAMs which have t_{RAH} of 10 nsec-15nsec. The typical $\overline{RASIN}$ to $\overline{CAS}$ delay is 105nsec. In this mode $\overline{CAS}$ can be extended after $\overline{RAS}$ goes high to extend the data output valid time. This feature is useful in applications with short cycles where $\overline{RAS}$ has to be terminated as soon as possible to meet the precharge (t_{RP}) requirements of the DRAM.

Mode 6 timing is illustrated in Figures 10 and 11. Provided that the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 10).

Next, the row address is disabled t_{RAH} after $\overline{RAS}$ goes low (20 ns minimum); the column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns): to rows valid (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

In this mode, the R/$\overline{C}$ (RFCK) pin is not used, but $\overline{CASIN}$ (RGCK) is used as $\overline{CASIN}$ to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 11.

Mode 7 — Set End-of-Count (3a, 3b select)

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same $\overline{EOC}$ is 127; with B1 = 0 and B0 = 1, $\overline{EOC}$ is 255; and with B1 = 1 and B0 = 0, $\overline{EOC}$ is 511. This selected value of $\overline{EOC}$ will be used until the next Mode 7 selection. At power-up the $\overline{EOC}$ is automatically set to 127 (B1 and B0 set to 11).

When B_1,B_2 are set to 11 in mode 7, mode 3b will be selected if mode 3 is selected (M_2, M_1, M_0 = 0, 1, 1). If B_1,B_2 is set to 00, 01 or 10 then mode 3a will be selected.

BANK SELECT (STROBED BY ADS)		END OF COUNT SELECTED
B1	B0	
0	0	127
0	1	255
1	0	511
1	1	127

Table 3. Mode 7

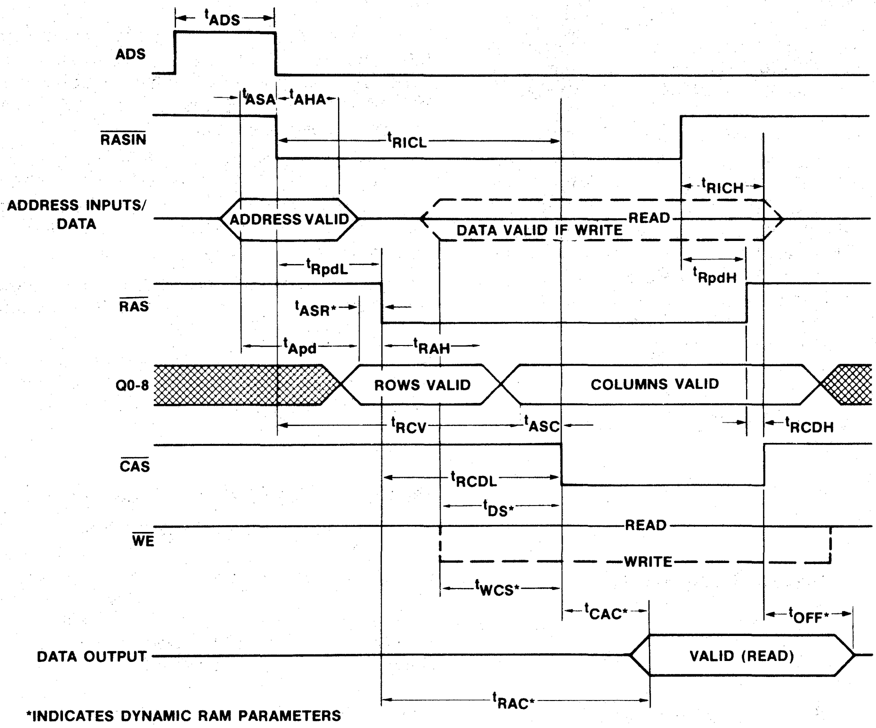


Figure 10. Mode 6 Timing ($\overline{\text{CASIN}}$ High)

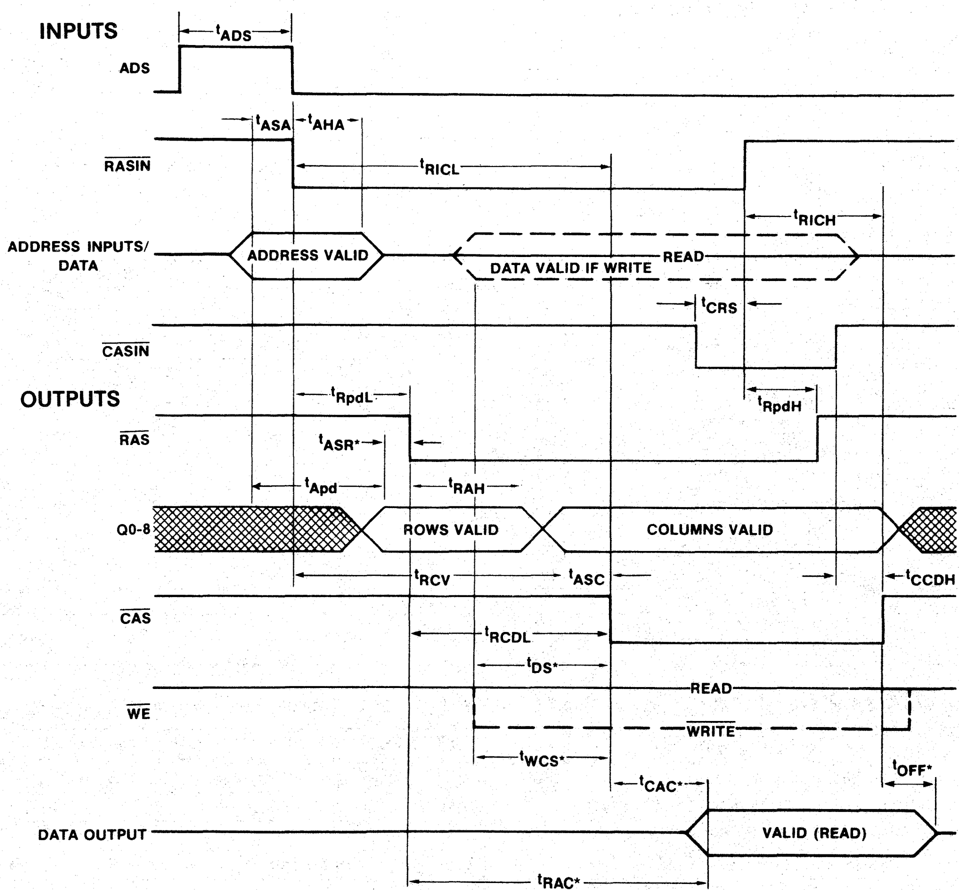


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Figure 11. Mode 6 Timing, Extended $\overline{CAS}$

SN74S409/-2 Specifications:

Absolute Maximum Ratings (Note 1)

Supply voltage V_{CC} .... −0.5 V to 7.0 V
Storage temperature range .... −65° to +150° C
Input voltage .... −1.5 V to 5.5 V
Output current .... 150 mA
Lead temperature (soldering, 10 seconds) .... 300° C

NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	4.75		5.25	V
T_A	Operating free-air temperature		0		75	0		75	°C
t_{ASA}	Address setup time to ADS	Figures 4, 5, 7, 10, 11	15			15			ns
t_{AHA}	Address hold time from ADS	Figures 4, 5, 7, 10, 11	15			15			ns
t_{ADS}	Address strobe pulse width	Figures 4, 5, 7, 10, 11	30			30			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 3	50			50			ns
t_{RST}	Counter reset pulse width	Figure 3	70			70			ns
$t_{RFCKL,H}$	Minimum pulse width of RFCK	Figure 6	100			100			ns
T	Period of $\overline{RAS}$ generator clock	Figure 6	100			100			ns
t_{RGCKL}	Minimum pulse width low of RGCK	Figure 6	35			35			ns
t_{RGCKH}	Minimum pulse width high of RGCK	Figure 6	35			35			ns
t_{CSRL}	$\overline{CS}$ low to access $\overline{RASIN}$ low	See Mode 5 description	10			10			ns
t_{RFSRG}	$\overline{RFSH}$ low set-up to RGCK low (Mode 1)	See Mode 1 description	35			35			ns
t_{RQHRF}	$\overline{RFSH}$ hold time from $\overline{RFRQ}$ (RF I/O)	Figure 6	2T			2T			ns

Electrical Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C ≤ T_A ≤ 75°C Typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS, R/C only	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_{IRSI}	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mAV
I_{ICTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselct		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS, R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0			V
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	I_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_{1D}	Output high drive current, except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{0D}	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	Three-state output current (address outputs)	0.4V ≤ V_{OUT} ≤ 2.7V, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		250	325	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

** These are absolute voltages with respect to pins 13 or 38 on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C ≤ T_A ≤ 75°C See Figure 12 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	FIGURE	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
t_{RHA}	Row address held from column select	Figure 4	10			10			ns
t_{RICL}	RASIN to CAS output delay (Mode 5)	Figures 7, 10	95	125	160	75	100	130	ns
t_{RICL}	RASIN to CAS output delay (Mode 6)	Figures 7, 10, 11	80	105	140	65	90	115	ns
t_{RICH}	RASIN to CAS output delay (Mode 5)	Figures 7, 10	40	48	60	40	48	60	ns
t_{RICH}	RASIN to CAS output delay (Mode 6)	Figures 7, 10, 11	50	63	80	50	63	80	ns
t_{RCDL}	RAS to CAS output delay (Mode 5)	Figures 7, 10		98	125		75	100	ns
t_{RCDL}	RAS to CAS output delay (Mode 6)	Figures 7, 10, 11		78	105		65	85	ns
t_{RCDH}	RAS to CAS output delay (Mode 5)	Figures 7, 10		27	40		27	40	ns
t_{RCDH}	RAS to CAS output delay (Mode 6)	Figures 7, 10		40	65		40	65	ns
t_{CCDH}	CASIN to CAS output delay Mode 6)	Figure 11	40	54	70	40	54	70	ns
t_{RCV}	RASIN to column address valid (Mode 5)	Figures 7, 10		90	120		80	105	ns
t_{RCV}	RASIN to column address valid (Mode 6)	Figures 7, 10, 11		75	105		70	90	ns
t_{RPDL}	RASIN to RAS delay	Figures 4, 5, 7, 10, 11	20	27	35	20	27	35	ns
t_{RPDH}	RASIN to RAS delay	Figures 4, 5, 7, 10, 11	15	23	32	15	23	32	ns
t_{APDL}	Address input to output low delay	Figures 4, 5, 7, 10, 11		25	40		25	40	ns
t_{APDH}	Address input to output high delay	Figures 4, 5, 7, 10, 11		25	40		25	40	ns
t_{SPDL}	Address strobe to address output low	Figures 4, 5		40	60		40	60	ns
t_{SPDH}	Address strobe to address output high	Figures 4, 5		40	60		40	60	ns
t_{WPDL}	WIN to WE output delay	Figure 5	15	25	30	15	25	30	ns
t_{WPDH}	WIN to WE output delay	Figure 5	15	30	60	15	30	60	ns
t_{CRS}	CASIN setup time to RASIN high (Mode 6)	Figure 11	35			35			ns
t_{CPDL}	CASIN to CAS delay (R/C low in Mode 4)	Figure 5	32	41	58	32	41	58	ns
t_{CPDH}	CASIN to CAS delay	Figure 5	25	39	50	25	39	50	ns
t_{RCC}	Column select to column address valid	Figure 4		40	58		40	58	ns
t_{RCR}	Row select to row address valid	Figures 4, 5		40	58		40	58	ns
t_{RAH}	Row address hold time (Mode 5)	Figures 7, 10	30			20			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 7, 10, 11	20			12			ns
t_{ASC}	Column address setup time (Mode 5)	Figures 7, 10	8			3			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 7, 10, 11	6			3			ns
t_{DiF1}	Maximum ($t_{RPDL} - t_{RHA}$) (Mode 4)				15			15	ns
t_{DiF2}	Maximum ($t_{RCC} - t_{CPDL}$) (Mode 4)				15			15	ns

SYMBOL	REFRESH PARAMETER	TEST CONDITIONS	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
t_{FRQL}	RFCK low to forced RFRQ low	C_L = 50 pF, Figure 6		20	30		20	30	ns
t_{FRQH}	RGCK low to force RFRQ high	C_L = 50pF, Figure 6		50	75		50	75	ns
t_{RGRL}	RGCK low to RAS low	Figure 6	50	65	95	50	65	95	ns
t_{RGRH}	RGCK low to RAS high	Figure 6	40	60	85	40	60	85	ns
t_{RFRH}	RFSH high to RAS high (encoding forced RFSH)	See Mode 1 description	55	80	110	55	80	110	ns
t_{CSCT}	CS high to RFSH counter valid	Figure 6		55	70		55	70	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 3			100			100	ns
t_{RFPDL}	RASIN to RAS delay during refresh	Figures 3, 6	35	50	70	35	50	70	ns
t_{RFPDH}	RASIN to RAS delay during refresh	Figures 3, 6	30	40	55	30	40	55	ns
t_{RFLCT}	RFSH low to counter address valid	CS = X, Figures 3, 6, 8		47	60		47	60	ns
t_{RFHRV}	RFSH high to row address valid	Figures 3, 6		45	60		45	60	ns
t_{ROHNC}	RAS high to new count valid	Figures 3, 8		30	55		30	55	ns
t_{RLEOC}	RASIN low to end-of-count low	C_L = 50pF, Figure 3			80			80	ns
t_{RHEOC}	RASIN high to end-of-count high	C_L = 50pF, Figure 3			80			80	ns
t_{RGEOB}	RGCK low to end-of-burst low	C_L = 50pF, Figure 8			95			95	ns
t_{MCEOB}	Mode change to end-of-burst high	C_L = 50pF, Figure 8			75			75	ns

Switching Characteristics: (Cont'd)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
	THREE-STATE PARAMETER								
t_{ZH}	$\overline{CS}$ low to address output high from Hi	Figures 6, 12 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15pF, Figures 6,12 R2 = 1k, S1 Open		20	40		20	40	ns
t_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figures 6, 12 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figures 6,13 R1 = 1k, S2 Open		25	50		25	50	ns
t_{HZH}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, $\overline{RASO-3}$) high from Hi-Z high	Figures 6,12 R2 = 750Ω, S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, $\overline{RASO-3}$) Hi-Z high from high	C_L = 15pF R2 = 750Ω, S1 open		40	75		40	75	ns
t_{HZL}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, $\overline{RASO-3}$) low from Hi-Z high	Figure 12 S1, S2 Open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, $\overline{RASO-3}$) Hi-Z high from low	C_L = 15pF, Figure 12 R2 = 750Ω, S1 open		50	80		50	80	ns

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8. C_L = 500pF; RAS0-RAS3, C_L = 150pF; CAS C_L = 600pF unless otherwise noted.

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F$ = 2.5 ns, f = 2.5 MHz. t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

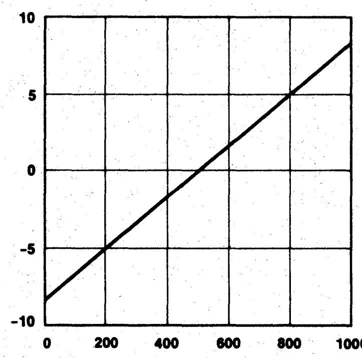
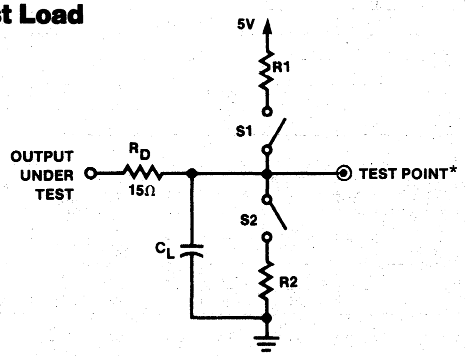


Figure 13. Change in Propagation Delay vs Loading Capacitance Relative to a 500 pF Load

Test Load



R1, R2 = 4.7K EXCEPT AS SPECIFIED.

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

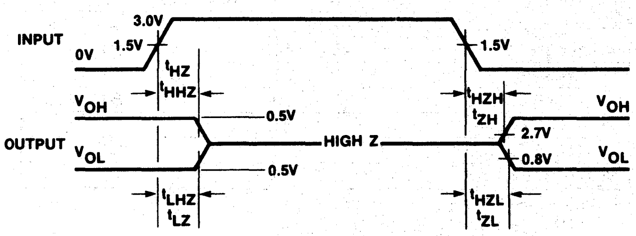


Figure 12. Waveform

SN74S409-3 Specifications:

Absolute Maximum Ratings (Note 1)

Supply voltage V_{CC} .... –0.5 V to 7.0 V
Storage temperature range .... –65° to +150° C
Input voltage .... –1.5 V to 5.5 V
Output current .... 150 mA
Lead temperature (soldering, 10 seconds) .... 300° C

NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S409-3 MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{ASA}	Address setup time to ADS	Figures 4, 5, 7, 10, 11	15			ns
t_{AHA}	Address hold time from ADS	Figures 4, 5, 7, 10, 11	15			ns
t_{ADS}	Address strobe pulse width	Figures 4, 5, 7, 10, 11	30			ns
$t_{RASINL,H}$	Pulse width of $\overline{\text{RASIN}}$ during refresh	Figure 3	50			ns
t_{RST}	Counter reset pulse width	Figure 3	70			ns
$t_{RFCKL,H}$	Minimum pulse width of RFCK	Figure 6	100			ns
T	Period of $\overline{\text{RAS}}$ generator clock	Figure 6	100			ns
t_{RGCKL}	Minimum pulse width low of RGCK	Figure 6	35			ns
t_{RGCKH}	Minimum pulse width high of RGCK	Figure 6	35			ns
t_{CSRL}	$\overline{\text{CS}}$ low to access $\overline{\text{RASIN}}$ low	See Mode 5 description	10			ns
t_{RFSRG}	$\overline{\text{RFSH}}$ low set-up to RGCK low (Mode 1)	See Mode 1 description	35			ns
t_{RQHRF}	$\overline{\text{RFSH}}$ hold time from $\overline{\text{RFRQ}}$ (RF I/O)	Figure 6	2T			ns

Electrical Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C ≤ T_A ≤ 75°C Typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS, R/C only	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_{IRSI}	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mAV
I_{ICTL}	Output load current for $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	V_{IN} = 0.5V, chip deselct		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS, R/$\overline{\text{C}}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0			V
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	I_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_{1D}	Output high drive current, except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{OD}	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	Three-state output current (address outputs)	0.4V ≤ V_{OUT} ≤ 2.7V, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		250	325	mA
C_{IN}	Input capacitance ADS, R/$\overline{\text{C}}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

** These are absolute voltages with respect to pins 13 or 38 on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C ≤ T_A ≤ 75°C See Figure 12 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	FIGURE	'S409-3 MIN	TYP	MAX	UNIT
t_{RHA}	Row address held from column select	Figure 4	10			ns
t_{RICL}	RASIN to CAS output delay (Mode 5)	Figures 7, 10	95	125	185	ns
t_{RICL}	RASIN to CAS output delay (Mode 6)	Figures 7, 10, 11	80	105	160	ns
t_{RICH}	RASIN to CAS output delay (Mode 5)	Figures 7, 10	40	48	70	ns
t_{RICH}	RASIN to CAS output delay (Mode 6)	Figures 7, 10, 11	50	63	95	ns
t_{RCDL}	RAS to CAS output delay (Mode 5)	Figures 7, 10		98	145	ns
t_{RCDL}	RAS to CAS output delay (Mode 6)	Figures 7, 10, 11		78	120	ns
t_{RCDH}	RAS to CAS output delay (Mode 5)	Figures 7, 10		27	40	ns
t_{RCDH}	RAS to CAS output delay (Mode 6)	Figures 7, 10		40	65	ns
t_{CCDH}	CASIN to CAS output delay Mode 6)	Figure 11	40	54	80	ns
t_{RCV}	RASIN to column address valid (Mode 5)	Figures 7, 10		90	140	ns
t_{RCV}	RASIN to column address valid (Mode 6)	Figures 7, 10, 11		75	120	ns
t_{RPDL}	RASIN to RAS delay	Figures 4, 5, 7, 10, 11	20	27	40	ns
t_{RPDH}	RASIN to RAS delay	Figures 4, 5, 7, 10, 11	15	23	37	ns
t_{APDL}	Address input to output low delay	Figures 4, 5, 7, 10, 11		25	46	ns
t_{APDH}	Address input to output high delay	Figures 4, 5, 7, 10, 11		25	46	ns
t_{SPDL}	Address strobe to address output low	Figures 4, 5		40	70	ns
t_{SPDH}	Address strobe to address output high	Figures 4, 5		40	70	ns
t_{WPDL}	WIN to WE output delay	Figure 5	15	25	35	ns
t_{WPDH}	WIN to WE output delay	Figure 5	15	30	70	ns
t_{CRS}	CASIN setup time to RASIN high (Mode 6)	Figure 11	35			ns
t_{CPDL}	CASIN to CAS delay (R/C low in Mode 4)	Figure 5	32	41	67	ns
t_{CPDH}	CASIN to CAS delay	Figure 5	25	39	60	ns
t_{RCC}	Column select to column address valid	Figure 4		40	67	ns
t_{RCR}	Row select to row address valid	Figures 4, 5		40	67	ns
t_{RAH}	Row address hold time (Mode 5)	Figures 7, 10	30			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 7, 10, 11	20			ns
t_{ASC}	Column address setup time (Mode 5)	Figures 7, 10	8			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 7, 10, 11	6			ns
t_{DiF1}	Maximum ($t_{RPDL} - t_{RHA}$) (Mode 4)				20	ns
t_{DiF2}	Maximum ($t_{RCC} - t_{CPDL}$) (Mode 4)				20	ns

SYMBOL	REFRESH PARAMETER	TEST CONDITIONS	'S409-3 MIN	TYP	MAX	UNIT
t_{FRQL}	RFCK low to forced RFRQ low	C_L = 50 pF, Figure 6		20	30	ns
t_{FRQH}	RGCK low to force RFRQ high	C_L = 50pF, Figure 6		50	75	ns
t_{RGRL}	RGCK low to RAS low	Figure 6	50	65	95	ns
t_{RGRH}	RGCK low to RAS high	Figure 6	40	60	85	ns
t_{RFRH}	RFSH high to RAS high (encoding forced RFSH)	See Mode 1 description	55	80	125	ns
t_{CSCT}	CS high to RFSH counter valid	Figure 6		55	75	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 3			100	ns
t_{RFPDL}	RASIN to RAS delay during refresh	Figures 3, 6	35	50	70	ns
t_{RFPDH}	RASIN to RAS delay during refresh	Figures 3, 6	30	40	55	ns
t_{RFLCT}	RFSH low to counter address valid	CS = X, Figures 3, 6, 8		47	70	ns
t_{RFHRV}	RFSH high to row address valid	Figures 3, 6		45	70	ns
t_{ROHNC}	RAS high to new count valid	Figures 3, 8		30	55	ns
t_{RLEOC}	RASIN low to end-of-count low	C_L = 50pF, Figure 3			80	ns
t_{RHEOC}	RASIN high to end-of-count high	C_L = 50pF, Figure 3			80	ns
t_{RGEOB}	RGCK low to end-of-burst low	C_L = 50pF, Figure 8			95	ns
t_{MCEOB}	Mode change to end-of-burst high	C_L = 50pF, Figure 8			75	ns

Switching Characteristics: (Cont'd)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S409-3 MIN	TYP	MAX	UNIT
	THREE-STATE PARAMETER					
t_{ZH}	$\overline{CS}$ low to address output high from Hi	Figures 6, 13 R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15pF, Figures 6, 13 R2 = 1k, S1 Open		20	40	ns
t_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figures 6, 13 R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figures 6, 14 R1 = 1k, S2 Open		25	50	ns
t_{HZH}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RASO-3}$) high from Hi-Z high	Figures 6, 13 R2 = 750Ω, S1 open		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RASO-3}$) Hi-Z high from high	C_L = 15pF R2 = 750Ω, S1 open		40	75	ns
t_{HZL}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RASO-3}$) low from Hi-Z high	Figure 13 S1, S2 Open		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RASO-3}$) Hi-Z high from low	C_L = 15pF, Figure 13, R2 = 750Ω, S1 open		50	80	ns

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8. C_L = 500pF; RAS0-RAS3, C_L = 150pF; CAS C_L = 600pF unless otherwise noted.

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F$ = 2.5 ns, f = 2.5 MHz. t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF/IO should not exceed 50 pF.

8

Applications

The 74S409 Dynamic RAM Controller provides all the address and control signals necessary to access and refresh dynamic RAMs. Since the 74S409 is not compatible with a specific bus or microprocessor, an interface is often necessary between the 74S409 and the system. A general application using PAL to implement the interface and two additional chips to provide refresh clock and chip select is shown in Figure 14.

The 74S409 operating modes may vary from application to application. For efficient refresh it is recommended to use mode 1 and mode 5 to take advantage of the hidden (transparent) refresh with forced refresh backup.

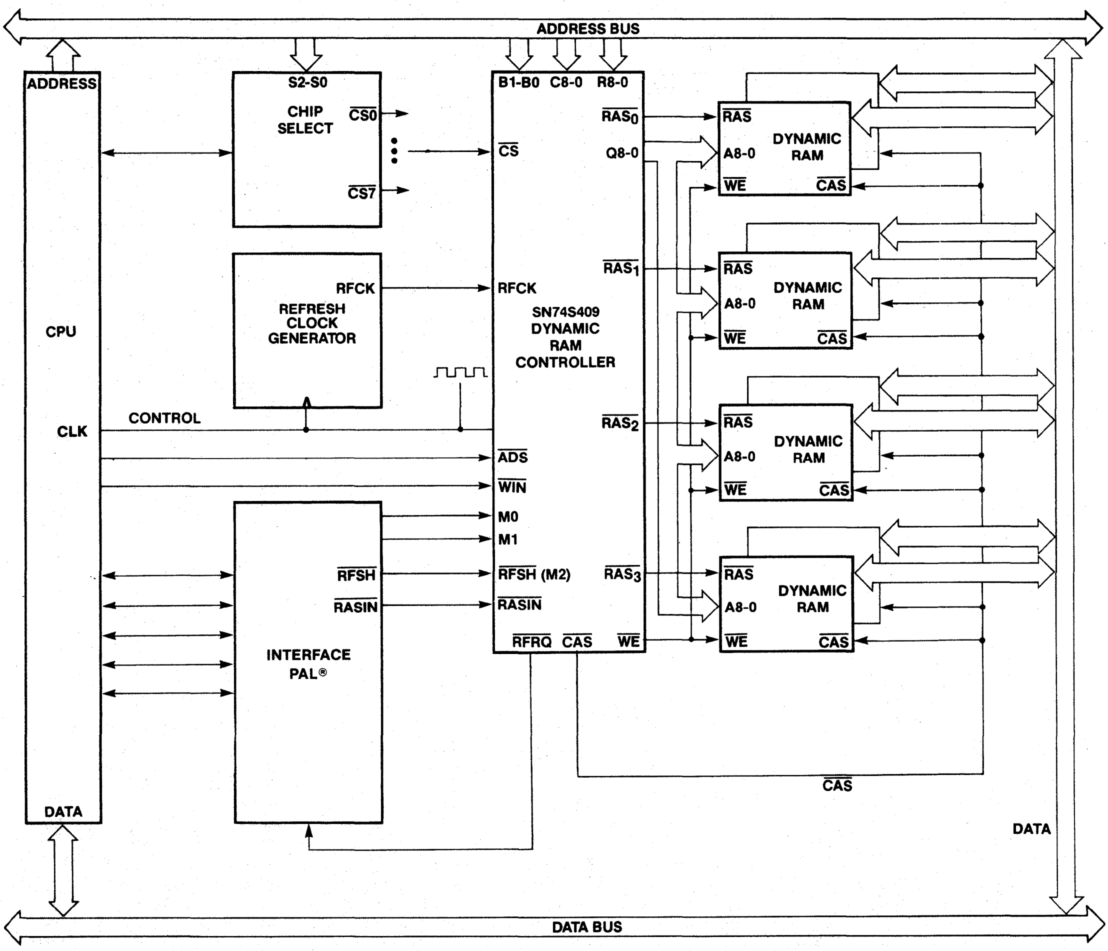


Figure 14. 74S409 in General Application

8-Bit Dynamic-RAM Driver with Three-state Outputs

SN54/74S700/-1 SN54/74S730/-1 SN54/74S731/-1 SN54/74S734/-1

Features/Benefits:

- **Provides MOS voltage levels for 16K and 64K DRAMs**
- **Undershoot of low-going output is less than -0.5 V**
- **Large capacitive drive capability**
- **Symmetric rise and fall times due to balanced output impedance**
- **Glitch-free outputs at power-up and power-down**
- **20-pin SKINNYDIP® saves space**
- **'S730/734 are exact replacement for the Am2965/66**
- **'S700/730/731/734 are pin-compatible with 'S210/240/241/244, and can replace them in many applications**
- **'S700-1/730-1/731-1/734-1 have a larger resistor in the output stage for better undershoot protection**
- **Commercial devices are specified at V_{CC} ±10%.**

Ordering Information

PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54S700/-1	J,W,L	Mil	High-Low	Invert	S
SN74S700/-1	N,J	Com			
SN54S730/-1	J,W,L	Mil	Low		
SN74S730/-1	N,J	Com			
SN54S731/-1	J,W,L	Mil	High-Low	Non-Invert	
SN74S731/-1	N,J	Com			
SN54S734/-1	J,W,L	Mil	Low		
SN74S734/-1	N,J	Com			

Description:

The 'S700, 'S730, 'S731, and 'S734 are buffers that can drive multiple address and control lines of MOS dynamic RAMs. The 'S700 and 'S730 are inverting drivers, and the 'S731 and 'S734 are non-inverting drivers. The 'S700/731 are pin-compatible with the 'S210/241 and have complementary enables. The 'S730 is pin-compatible with the 'S240 and an exact replacement for the Am2965. The 'S734 is pin-compatible with the 'S244 and an exact replacement for the Am2966.

These devices have been designed with an additional internal resistor in the lower output driver transistor circuit, unlike regular 8-bit buffers. This resistor serves two purposes: it causes a slower fall time for a high-to-low transition, and it limits the undershoot without the use of an external series resistor.

The 'S700, 'S730, 'S731, and 'S734 have been designed to drive the highly-capacitive input lines of dynamic RAMs. The drivers provide a guaranteed V_{OH} of V_{CC} - 1.15 volts, limit undershoot to 0.5V, and exhibit a rise time symmetrical to their fall time by having balanced outputs. These features enhance dynamic RAM performance.

For a better-controlled undershoot for lightly capacitive-loaded circuits the 'S700-1, 'S730-1, 'S731-1 and 'S734-1 provide a larger resistor in the lower output stage. Also an improved undershoot voltage of -0.3 V is provided in the 'S700-1 series.

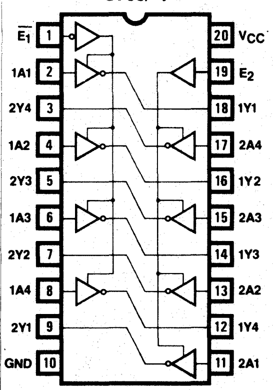
A typical fully-loaded-board dynamic-RAM array consists of 4 banks of dynamic-RAM memory. Each bank has its own $\overline{RAS}$ and $\overline{CAS}$, but has identical address lines. The $\overline{RAS}$ and $\overline{CAS}$ inputs to the array can come from one driver, reducing the skew between the $\overline{RAS}$ and $\overline{CAS}$ signals. Also, only one driver is needed to drive eight address lines of a dynamic RAM. The propagation delays are specified for 50pf and 500pf load capacitances, and the commercial-range specifications are extended to V_{CC} ± 10%.

All of the octal devices are packaged in the popular 20-pin SKINNYDIP™.

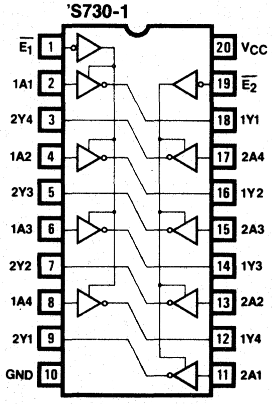
8

Logic Symbols

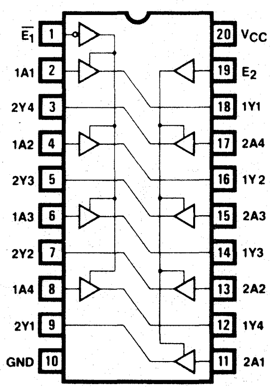
'S700/-1



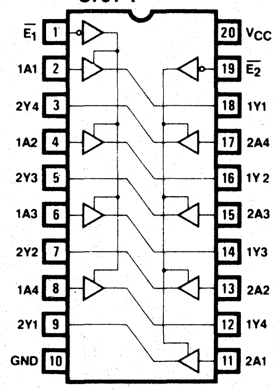
'S730 (Am2965)
'S730-1



'S731/-1



'S734 (Am2966)
'S734-1



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

Function Tables

'S700/-1

$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	H	Z
L	L	H	X	L	Z
L	H	L	L	H	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	H	L	L
H	H	X	L	Z	H
H	H	X	H	Z	L
H	L	X	X	Z	Z

'S730/-1

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	H	H
L	L	L	H	H	L
L	L	H	L	L	H
L	L	H	H	L	L
L	H	L	X	H	Z
L	H	H	X	L	Z
H	L	X	L	Z	H
H	L	X	H	Z	L
H	H	X	X	Z	Z

'S731/-1

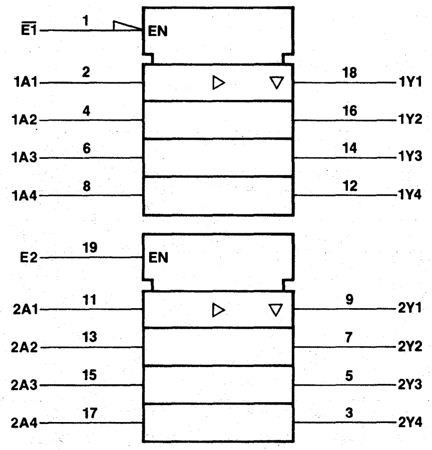
$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	L	Z
L	L	H	X	H	Z
L	H	L	L	L	L
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	H
H	H	X	L	Z	L
H	H	X	H	Z	H
H	L	X	X	Z	Z

'S734/-1

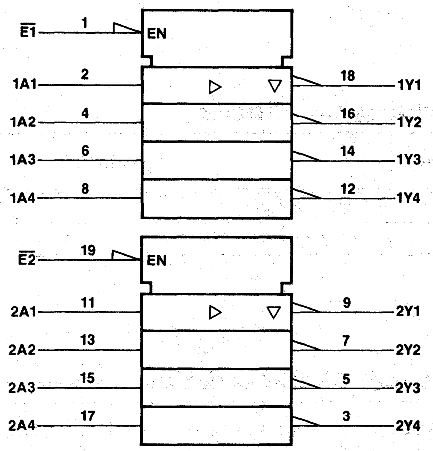
$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	L	L
L	L	L	H	L	H
L	L	H	L	H	L
L	L	H	H	H	H
L	H	L	X	L	Z
L	H	H	X	H	Z
H	L	X	L	Z	L
H	L	X	H	Z	H
H	H	X	X	Z	Z

IEEE Symbol

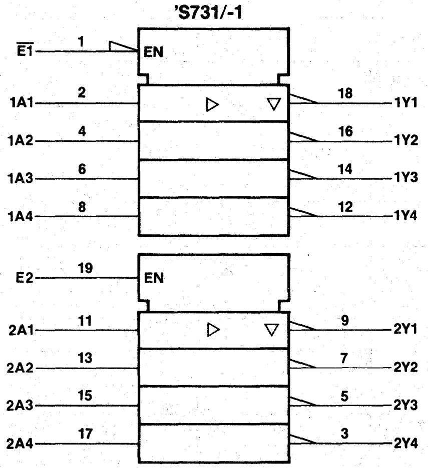
'S700/-1



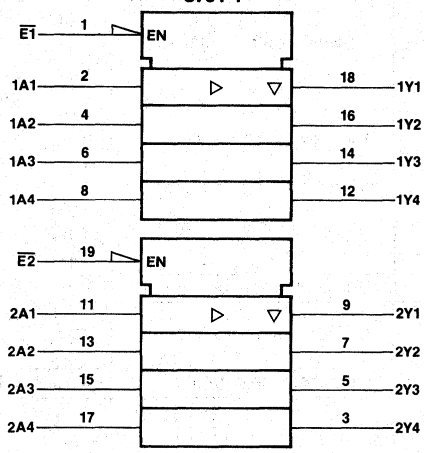
'S730-1



'S731/-1



'S734-1



Absolute Maximum Ratings

Supply voltage V_{CC} .... −0.5 V to 7.0 V
Input voltage .... −1.5 V to 7.0 V
Off-state output voltage .... −0.5 V to $+V_{CC}$ max
Storage temperature range .... −65° to +150°C
Output current .... 200 mA

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}*	Low-level input voltage						0.8			0.8	V
V_{IH}*	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	Any A	V_{CC} = MAX	V_I = 0.4V			−0.2			−0.2	mA
		Any E					−0.4			−0.4	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 1mA			0.5			0.5	V
				I_{OL} = 12mA			0.8			0.8	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −1mA	V_{CC} −1.15	V_{CC} −.7		V_{CC} −1.15	V_{CC} −.7		V
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.4V			−200			−200	μA
I_{OZH}				V_O = 2.7V			100			100	μA
I_{OS}	Output short-circuit current †		V_{CC} = MAX		−60		−200	−60		−200	mA
I_{OL}	Output sink current		V_{OL} = 2.0V	'S 7XX	50			50			mA
				'S 7XX-1	40			40			
I_{OH}	Output source current		V_{OH} = 2.0V		−35			−35			mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX Outputs open	S700/-1 S730/-1		24	50		24	50	mA
				S731/-1 S734/-1		53	75		53	75	
		Outputs Low		S700/-1 S730/-1		86	125		86	125	
				S731/-1 S734/-1		92	130		92	130	
		Outputs Disabled		S700/-1 S730/-1		86	125		86	125	
				S731/-1 S734/-1		116	150		116	150	

† Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

*These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or test noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C For the 'S700, 'S730, 'S731, 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	6	9	15	ns
			C_L = 500pf	18	22	30	
t_{PHL}			C_L = 50pf	5	7	15	
			C_L = 500pf	18	22	30	
t_{PZL}	Output enable delay	2 & 4	S = 1		12	20	ns
t_{PZH}			S = 2		12	20	
t_{PLZ}	Output disable delay	2 & 4	S = 1		11	20	ns
t_{PHZ}			S = 2		6.5	12	
t_{SKEW}	Output-to-output skew	1 & 3	C_L = 50pf		±0.5	±3.0	ns
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf		0	−0.5	V

*The SKEW timing specification is guaranteed by design, but not tested.

Switching Characteristics Over Operating Range** For the 'S700, 'S730, 'S731, 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MILITARY †† V_{CC} = 5.0V ±10%			COMMERCIAL V_{CC} = 5.0V ±10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	4		20	4		17	ns
			C_L = 500pf	18		40	18		35	
t_{PHL}			C_L = 50pf	4		20	4		17	
			C_L = 500pf	18		40	18		35	
t_{PZL}	Output enable delay	2 & 4	S = 1†			28			28	ns
t_{PZH}			S = 2†			28			28	
t_{PLZ}	Output disable delay	2 & 4	S = 1†			24			24	ns
t_{PHZ}			S = 2†			16			16	
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf			−0.5			−0.5	V

**AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.

†"S = 1" and "S = 2" refer to the switch setting in Figure 2.

††T_C = -55 to + 125°C for flatpack versions.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C For the 'S700-1, 'S730-1, 'S731-1, 'S734-1

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	6	9	15	ns
			C_L = 500pf	18	22	30	
t_{PHL}			C_L = 50pf	5	7	15	
			C_L = 500pf	18	22	40	
t_{PZL}	Output enable delay	2 & 4	S = 1		12	20	ns
t_{PZH}			S = 2		12	20	
t_{PLZ}	Output disable delay	2 & 4	S = 1		11	20	ns
t_{PHZ}			S = 2		6.5	12	
t_{SKEW}	Output-to-output skew	1 & 3	C_L = 50pf	*	±0.5	±3.0	ns
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf		0	−0.3	V

*The SKEW timing specification is guaranteed by design, but not tested.

Switching Characteristics Over Operating Range** For the 'S700-1, 'S730-1, 'S731-1, 'S734-1

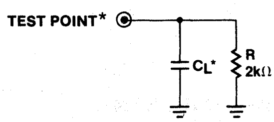
SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MILITARY †† V_{CC} = 5.0V ±10% MIN	TYP	MAX	COMMERCIAL V_{CC} = 5.0V ±10% MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	4		20	4		17	ns
			C_L = 500pf	18		40	18		35	
t_{PHL}			C_L = 50pf	4		20	4		17	
			C_L = 500pf	18		50	18		45	
t_{PZL}	Output enable delay	2 & 4	S = 1†			28			28	ns
t_{PZH}			S = 2†			28			28	
t_{PLZ}	Output disable delay	2 & 4	S = 1†			24			24	ns
t_{PHZ}			S = 2†			16			16	
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf			-0.3			-0.3	V

**AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.

†"S = 1" and "S = 2" refer to the switch setting in Figure 2.

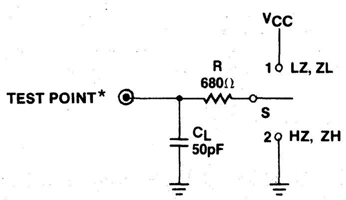
†† T_C = -55 to + 125° C for flatpack versions.

Test Loads



*t_{pd} specified at C_L = 50 and 500pF

Figure 1. Capacitive Load Switching



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Figure 2. Three-State Enable/Disable

Typical Switching Characteristics

VOLTAGE WAVEFORMS

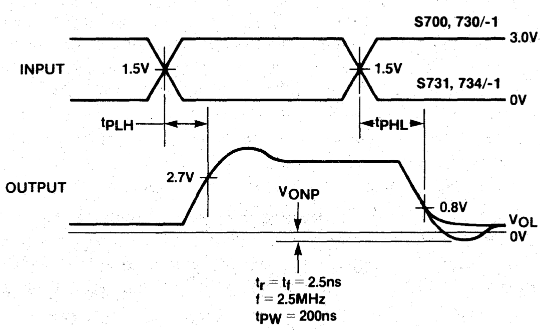


Figure 3. Output Voltage Levels

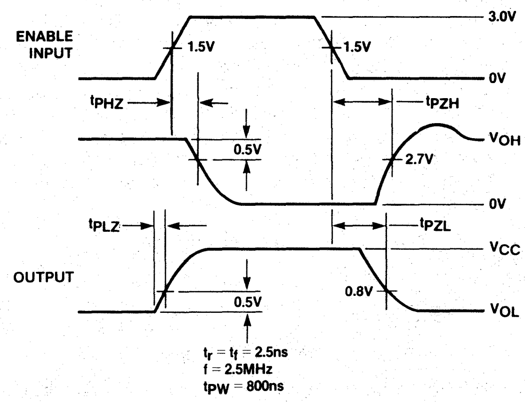
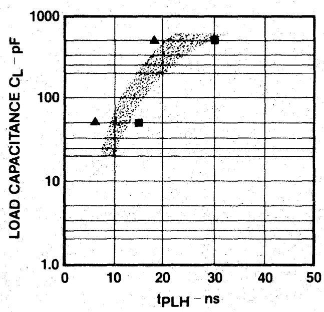
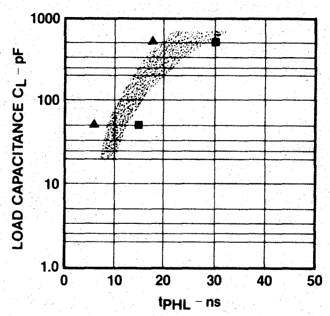


Figure 4. Three-State Control Levels

Typical Performance Characteristics:

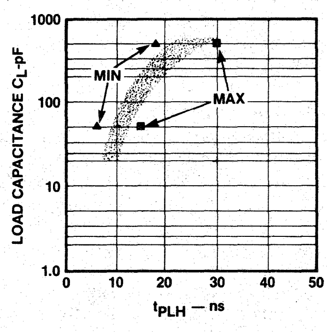


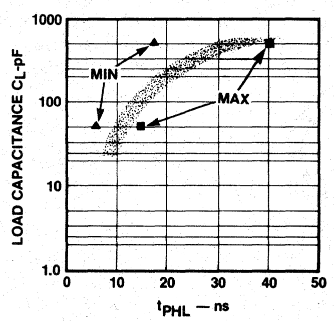


▲ INDICATE MINIMUM VALUES AT 25°C.
■ INDICATE MAXIMUM VALUE AT 25°C.

Figure 5a. t_{PLH} for V_{OH} = 2.7 V vs. C_L, for the 'S700 series

Figure 6a. t_{PHL} for V_{OL} = 0.8 V vs. C_L, for the 'S700 series





▲ INDICATE MINIMUM VALUES AT 25°C.
■ INDICATE MAXIMUM VALUE AT 25°C.

Figure 5b. t_{PLH} for V_{OH} = 2.7 V vs. C_L, for the 'S700-1 series

Figure 6b. t_{PHL} for V_{OL} = 0.8 V vs. C_L, for the 'S700-1 series

Applications

The'S700, 'S730, 'S731 and 'S734 are 8-bit bipolar dynamic RAM drivers and are pin-compatible with the 'S210, 'S240, 'S241 and 'S244 respectively.

The actual circuit conditions that arise for driving dynamic RAM memories are as follows: Typically, in dynamic RAM arrays address lines and control lines, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ have a fair amount of "daisy chaining." The daisy chaining causes an inductive effect due to the traces in the printed circuit board; the dominant factor in the RAM loading is input capacitance, and these two conditions contribute to the actual driver conditions shown in Figure 7. The result is a transmission line with distributed inductance and capacitance connected to the driver outputs.

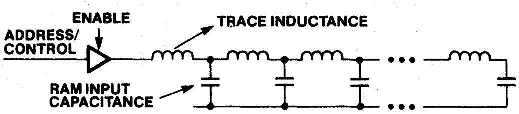


Figure 7. RAM Driver Output To Array

The transmission line effect can imply reflections, which in turn cause ringing, and it takes some time before the output settles from the low-to-high transition. On the high-to-low transition, along with ringing, a voltage undershoot can occur, and the circuit takes even longer to settle to an acceptable zero level. The main cause for the shorter high-to-low transition as compared to the low-to-high transition is the output impedance of typical Schottky drivers. Figure 8, shows a typical Schottky driver output stage and Figure 9 shows the output impedance for high and low output states.

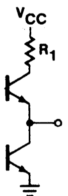


Figure 8. Typical Schottky Driver Output

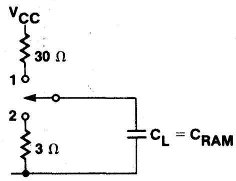


Figure 9. Driver Output Impedance

In Figure 9 when S=1, the output is high and the driver output impedance is approximately 30Ω. When S=2, the output is low and the driver output impedance is approximately 3Ω. There is a 10:1 ratio for the output impedances for the low and high states. The high-to-low transition causes a problem as the output transistor turns on fast due to the low impedance and undershoot results at the RAM inputs.

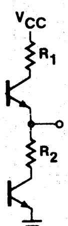


Figure 10. 'S700, 'S730, 'S731, and 'S734 Output Stage

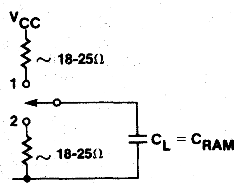


Figure 11. Driver Output Impedance For the 'S700, 'S730, 'S731, and 'S734

The 'S700, 'S730, 'S731, and 'S734 have a modification in their output stage, in that an internal resistor is added to the lower output stage as shown in Figure 10.

The 'S700-1, 'S730-1, 'S731-1 and 'S734-1 have a larger resistor, R2, comparted to the "non-dash" parts, which give better undershoot protection at a slightly slower switching performance.

The structure in Figure 10 provides a driver output impedance of approximately 18Ω to 25Ω in either high (S = 1) or low (S = 2) states as shown in Figure 11. In addition, this circuit limits undershoot to −0.5V, essentially eliminating that problem; provides a symmetrical rise and fall time; and guarantees output levels of V_{CC} −1.15V needed for MOS High levels. Also, when using the 'S700, 'S730, 'S731 and 'S734, no external resistors are needed. 'S240-series parts used with external resistors to provide drive capability, but the rise times and fall times are unsymmetrical due to higher impedance for low-to-high transitions.

Figure 12 shows the undershoot problem using a 'S240 without external resistors and the elimination of the problem by using the 'S730. Thus from a dynamic-RAM system-design viewpoint, the 'S700, 'S730, 'S731, and 'S734 are very effective RAM drivers.

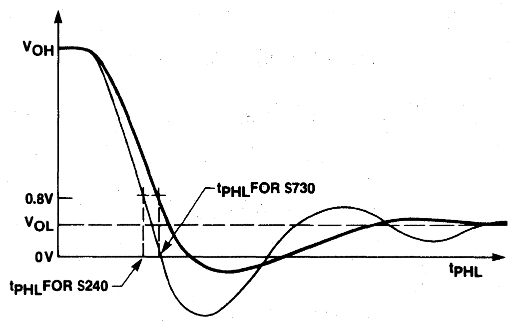


Figure 12. Comparison of Undershoots and t_{PHL}

An application using these 8-bit drivers to interface address and control lines (and data lines) to a dynamic RAM array using 64K DRAMs is discussed. The signals needed for the controls are $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. The address lines are A0–A7 and the data lines are shown as the high and low byte. The array is shown in Figure 13. It consists of four rows of DRAMs; each row has individual $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ lines. However, all four rows have common address lines A0–A7. The RAM capacitive loading for $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ is about 10 pf per input. The loading of the address lines is about 5 to 7 pf per input. The loading of the $\overline{RAS}_i$, $\overline{CAS}_i$ and $\overline{WE}_i$ inputs to each row of memories is 160 pf. Note that $\overline{RAS}_i$ and $\overline{CAS}_i$ come from the same driver, which reduces timings skews which might arise if they were output from separate drivers. The address lines are outputs from another driver, and the loading on each line is 320 pf (5 pf loading times 64 DRAMs). At this point it is worth noting that if a 320-pf loading affects performance unduly, then the address lines can be split between two drivers with each having a load of 160 pf, reducing overall signal delay.

If an error-detection-and-correction scheme is used, then typically the row size expands to 22 bits from the 16 bits shown in the example. The 'S700, 'S730, 'S731 and 'S734 drivers lend themselves to such expansion, as their propagation delays are specified at 50 pF and also at 500 pF.

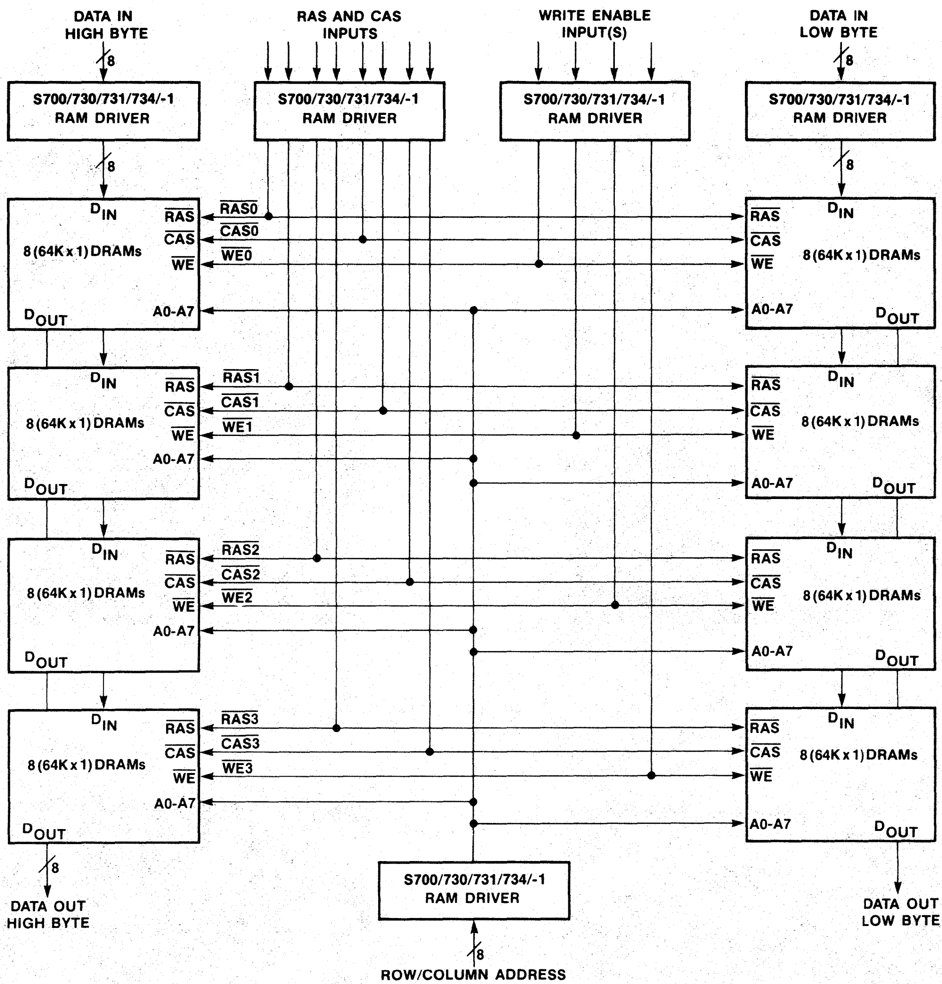
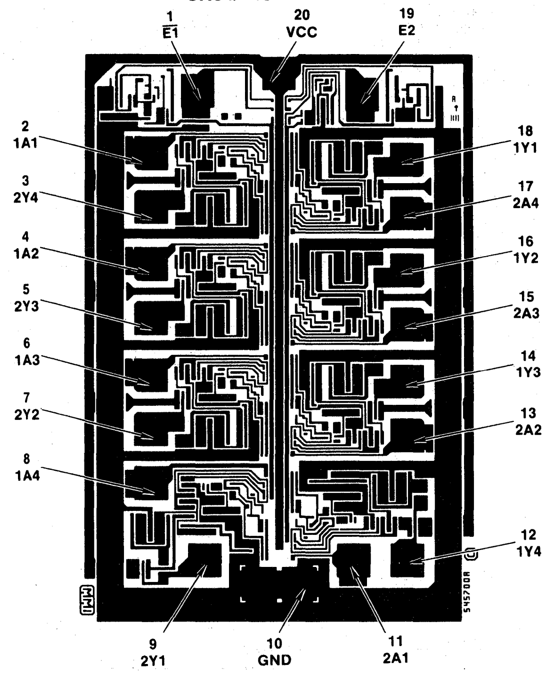


Figure 13. 256K X 16 Dynamic RAM Array with RAM Drivers

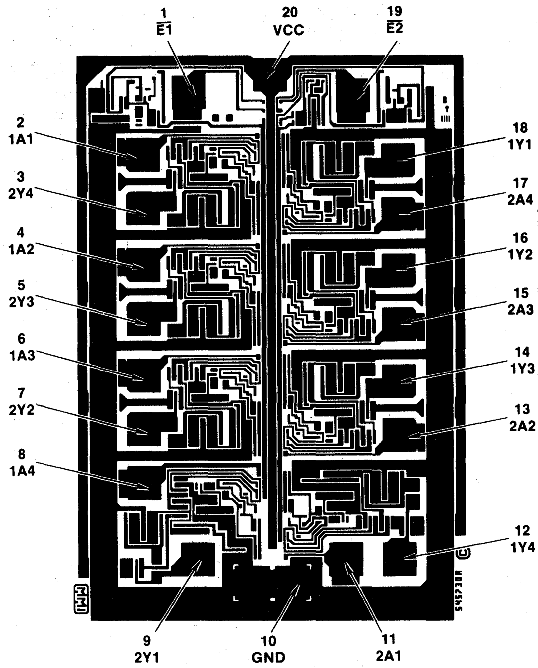
8

Die Configurations

SN54/74S700/-1

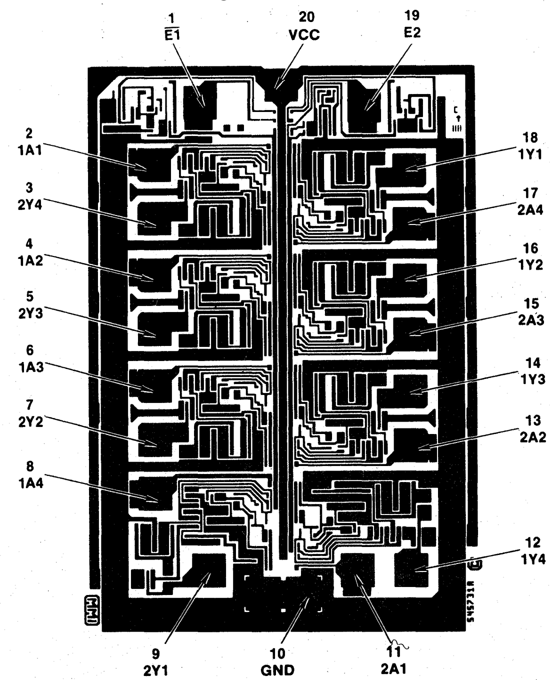


SN54/74S730/-1

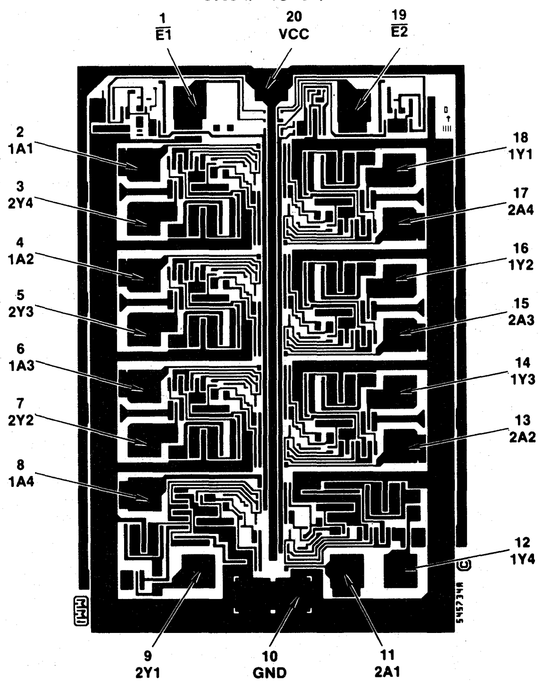


Die Size: 62x87 mil^2

SN54/74S731/-1



SN54/74S734/-1



Quad Power Strobe

HD1-6600-8
HD1-6600-5
HD1-6600-2

Features/Benefits

- High drive current—200 mA
- High speed—40 ns typical
- Low fan-in (250 μA Max), TTL-compatible
- Low power: Standby 30 mW/circuit
  Active 120 mW/circuit
- Several different power-supply levels

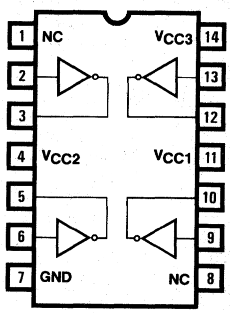
Ordering Information

PART NUMBER	PACKAGE	TYPE	TEMPERATURE RANGE
HD1-6600-5	J14	Power	0° to +75°C
HD1-6600-2	J14	Power	-55° to +125°C
HD1-6600-8*	J14	Power	-55° to +125°C

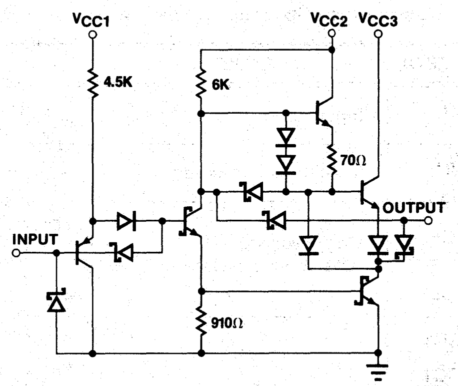
Description

The HD1-6600 quad power strobe are four high-current drivers used for power-down mode of ROM/PROM and other logic devices. V_{CC} can be removed from nonactive devices in order to reduce total system power.

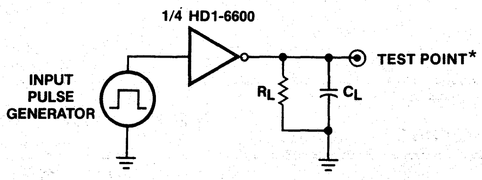
Pin Configuration



Block Diagram

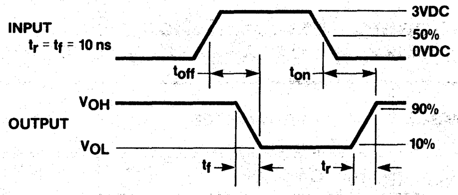


Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



*Note: Parts suffixed -8 are equivalent to parts suffixed -2 screened in accordance with MIL-STD 883 method 5004, Class B.

Absolute Maximum Ratings

Supply voltage, V_{CC1} .... +8 V
V_{CC2} .... +18 V (HD1-6600)
V_{CC3} .... +18 V (HD1-6600)
Input voltage .... −1.5 V to +5.5 V
Input current .... −25 mA to +5 mA
Output current .... −300 mA
Storage temperature range .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC1}	Supply voltage 1	4.5	5	5.5	4.5	5	5.5	V
V_{CC2}	Supply voltage 2	10	12	13.8	10	12	13.8	V
V_{CC3}	Supply voltage 3	4.5	5	5.5	4.75	5	5.5	V
I_{OH}	High-level output current		−150	−200		−150	−200	mA
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

Over Recommended Operating Free Air Temperature Range V_{CC2} = 12.0V V_{CC3} = 5.0V

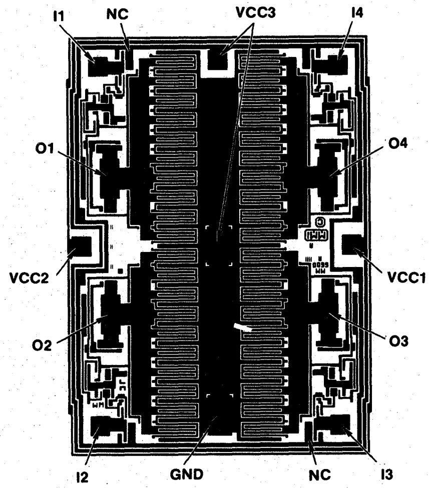
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IR} I_{IF}	Input current	V_{IN} = 2.4V V_{IN} = 0.4V	V_{CC1} = 5.5V		 −80	30 −250	μA
V_{IH} V_{IL}	Input threshold voltage	V_{CC1} = 4.5V		2.0		 0.8	V
V_{OH}	Output voltage (One strobe enabled)	V_{CC1} = 5.0V V_{IN} = 0.4V	I_{OH} = −150mA	4.75	4.85		V
V_{OL}		V_{CC1} = 5.0V V_{IN} = 2.4V	I_{OL} = 500μA		0.9	1.0	V
I_{CC1}	Supply current (All strobes enabled)	V_{CC1} = 5.5V	V_{IN} = 2.4V		4	6.0	mA
I_{CC1}		V_{CC1} = 5.5V	V_{IN} = 0.4V		4	6.4	mA
I_{CC2}		V_{CC1} = 5.5V V_{IN} = 0.4V	I_{OH} = −150mA		50	60	mA
I_{CC2}		V_{CC1} = 5.5V V_{IN} = 2.4V	I_{OL} = 0		10	12	mA

Switching Characteristics

V_{CC1} = 5.0V V_{CC2} = 12.0V V_{CC3} = 5.0V T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (SEE STANDARD TEST LOAD)	MIN	TYP	MAX	UNIT
t_{on}	Turn On delay	R_L = 31.6Ω C_L = 620pF		40	75	ns
t_{off}	Turn Off delay			40	75	ns
t_r	Rise time			35	65	ns
t_f	Fall time			35	65	ns

Die Configuration



Die Size: 90x67 mil^2

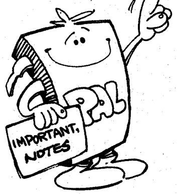

PAL
IMPORTANT,
NOTES

Table of Contents
ARITHMETIC ELEMENTS AND LOGIC

Arithmetic Elements and Logic Selection Guide

Arithmetic and Logic Elements

DESCRIPTION	PART NUMBER	MAX ADD TIME	MAX CARRY (OR GENERATE) TIME	PINS
4-bit ALU	5/74S381	27 ns	20 ns	20
4 Group carry-look-ahead generator	5/74S182		7 ns	16

Encoder Priority

DESCRIPTION	PART NUMBER	OUTPUT	MAX LOGIC DELAYS	PINS
High-Speed Schottky Priority Encoders	SN54/74S148 SN54/74S348	Totem-Pole 3-State	$\overline{D_i} \rightarrow \overline{A_i}$ = 13nsec $\overline{D_i}$ — $\overline{GS}$, $\overline{EO}$ = 15nsec	16

Arithmetic Logic Unit/ Function Generator
SN54S381 SN74S381

Features/Benefits

- A fully parallel 4-bit ALU
- Ideally suited for high-speed processors
- Generate and propagate outputs for full carry lookahead
- Three arithmetic functions
- Three logic functions
- Preset and clear functions
- Available in 20-pin SKINNYDIP®

Ordering Information

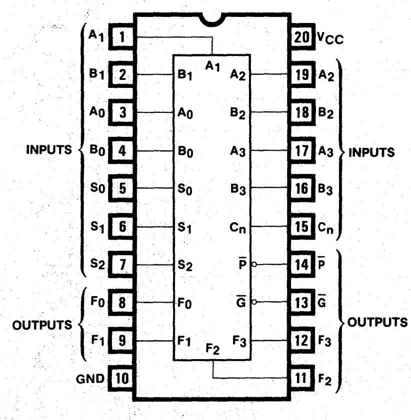
PART NUMBER	PACKAGE	TEMPERATURE
SN54S381	J,W,L	Military
SN74S381	N,J	Commercial

Description

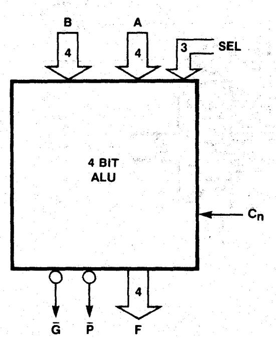
The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full lookahead carry circuit is provided for fast, simultaneous carry generation by means of two cascaded outputs (P and G) for the four bits in the package.

Pin Configuration

SN54S381, SN74S381



Logic Symbol

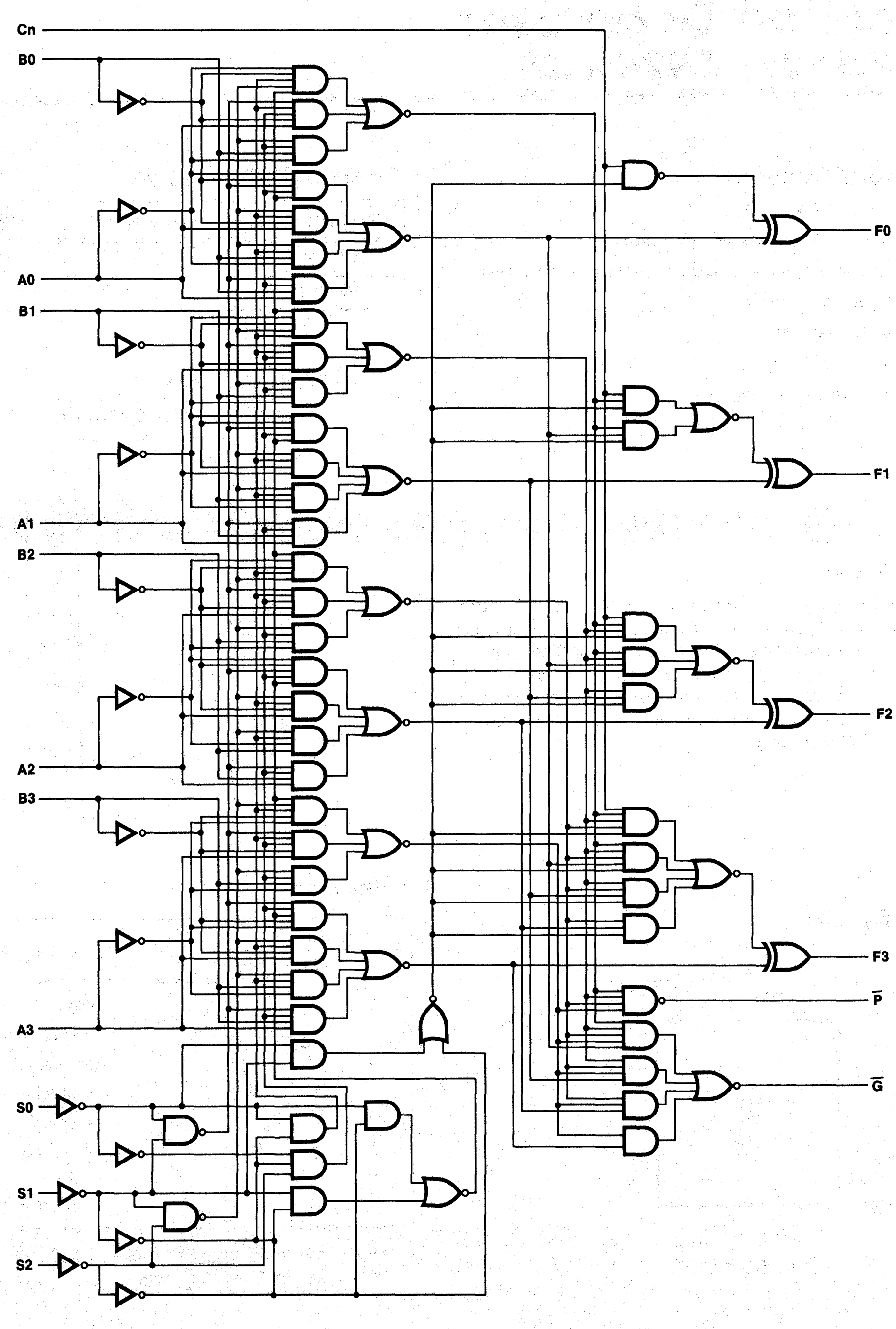


Function Table

SELECTION			ARITHMETIC/LOGIC OPERATION
S2	S1	S0	
L	L	L	Clear †
L	L	H	B minus A
L	H	L	A minus B
L	H	H	A plus B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	Preset ††

† Force all F outputs to be Lows.
†† Force all F outputs to be Highs.

Logic Diagram



Function Table

	INPUTS												OUTPUTS					
FUNCTION	S2	S1	S0	Cn	A3	A2	A1	A0	B3	B2	B1	B0	F3	F2	F1	F0	$\overline{G}$	$\overline{P}$
Clear	0	0	0	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0
B minus A (Inverse Subtraction)	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
				0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
				0	1	1	1	1	0	0	0	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
				1	0	0	0	0	1	1	1	1	1	1	1	1	0	0
				1	1	1	1	1	0	0	0	0	0	0	0	1	1	1
				1	1	1	1	1	1	1	1	1	0	0	0	0	1	0
A minus B (Subtract)	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
				0	0	0	0	0	1	1	1	1	0	0	0	0	1	1
				0	1	1	1	1	0	0	0	0	1	1	1	0	0	0
				0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
				1	0	0	0	0	1	1	1	1	0	0	0	1	1	1
				1	1	1	1	1	0	0	0	0	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1	0	0	0	0	1	0
A plus B (Add)	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
				0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
				0	1	1	1	1	0	0	0	0	1	1	1	1	1	0
				0	1	1	1	1	1	1	1	1	1	1	1	0	0	0
				1	0	0	0	0	0	0	0	0	0	0	0	1	1	1
				1	0	0	0	0	1	1	1	1	0	0	0	0	1	0
				1	1	1	1	1	0	0	0	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

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Function Table

	INPUTS												OUTPUTS			
FUNCTION	S2	S1	S0	Cn	A3	A2	A1	A0	B3	B2	B1	B0	F3	F2	F1	F0
$A \oplus B$ (OR)	1	0	0	X	0	0	0	0	0	0	0	0	0	0	0	0
				X	0	0	0	0	1	1	1	1	1	1	1	1
				X	1	1	1	1	0	0	0	0	1	1	1	1
				X	1	1	1	1	1	1	1	1	0	0	0	0
$A \oplus B$ (XOR)	1	0	1	X	0	0	0	0	0	0	0	0	0	0	0	0
				X	0	0	0	0	1	1	1	1	1	1	1	1
				X	1	1	1	1	0	0	0	0	1	1	1	1
				X	1	1	1	1	1	1	1	1	1	1	1	1
$A \bullet B$ (AND)	1	1	0	X	0	0	0	0	0	0	0	0	0	0	0	0
				X	0	0	0	0	1	1	1	1	0	0	0	0
				X	1	1	1	1	0	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	1	1	1	1	1
Preset	1	1	1	X	0	0	0	0	0	0	0	0	1	1	1	1
				X	0	0	0	0	1	1	1	1	1	1	1	1
				X	1	1	1	1	0	0	0	0	1	1	1	1
				X	1	1	1	1	1	1	1	1	1	1	1	1

1 = HIGH voltage level
0 = LOW voltage level
X = Don't care

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 5.5 V
Storage temperature range .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

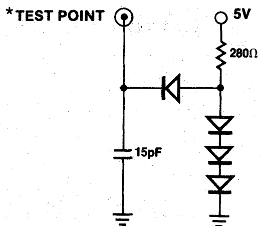
SYMBOL	PARAMETER	TEST CONDITIONS			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2						V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5 V	Any S input			−2			−2	mA
				Cn			−8			−8	
				All others			−6			−6	
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V	Any S input			50			50	μA
				Cn			250			250	
				All others			200			200	
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V				1			1	mA
V_{OL}	Low-Level output voltage	V_{CC} = MIN V_{IL} = 0.8 V	V_{IH} = 2 V I_{OL} = 20 mA				0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8 V	V_{IH} = 2 V I_{OH} = −1 mA		2.4	3.4		2.7	3.4		V
I_{OS}	Output short-circuit current*	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX				105	160		105	160	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

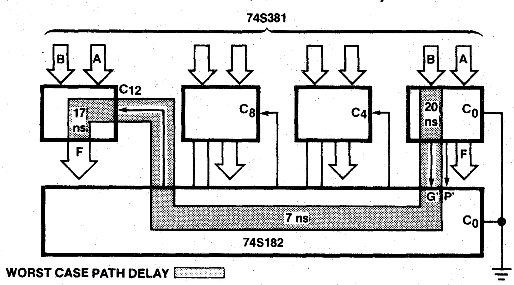
SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	FROM (INPUT)	TO (OUTPUT)	5/74S381 TYP	5/74S381 MAX	UNIT
t_P	Propagation delay time	C_L = 15 pF R_L = 280Ω	C	Any F	10	17	ns
t_P	Propagation delay time		Any A or B	$\overline{G}$	12	20	ns
t_P	Propagation delay time		Any A or B	$\overline{P}$	11	18	ns
t_{PLH}	Propagation delay, low-to-high		Any A or B	Any F	18	27	ns
t_{PHL}	Propagation delay, high-to-low		Any A or B	Any F	16	25	ns
t_P	Propagation delay time		Any S	Any F, $\overline{G}$, $\overline{P}$	18	30	ns

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

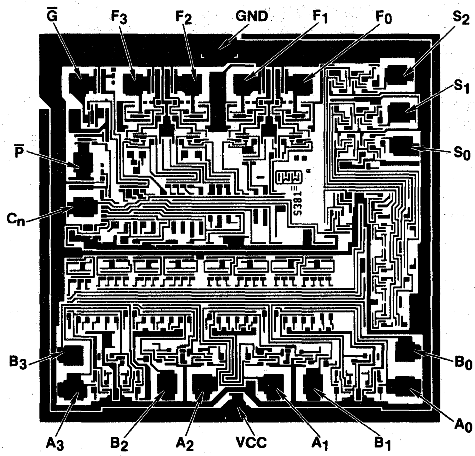
16-BIT ALU (USING 74S381)



MAXIMUM DELAY OF ADDITION/SUBTRACTION.

	74S381 + 74S182
1-4 bits	27ns
5-16 bits	44ns
17-64 bits	64ns

Die Configuration



Die Size: 83 x 86 mil^2

Look-Ahead Carry Generators

SN54S182 SN74S182

Features/Benefits

- Provides lookahead carry scross a group of four 'S381s
- Capable of multilevel lookahead carry for high-speed arithmetic operations over long wordlengths
- High-speed operation

Description

The SN54S182 and SN74S182 are high-speed, lookahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full lookahead across n-bit adders. Carry, carry-generate and carry-propagate functions are provided as enumerated in the pin designation table below.

When used in conjunction with 74S381, 74F381, 74S181 or 2901 arithmetic logic units (ALU), these generators provide high-speed carry lookahead capability for any word length. Each 'S182 generates the lookahead (anticipated carry) across a group of four ALUs and, in addition, other carry lookahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to any number of levels.

The carry functions (input, outputs, generate and propagate) of the carry lookahead generators are implemented in the compatible form for directed connection to the ALU. Logic equations for the 'S182 are:

$$Cn{+}x = G0 + P0\ Cn$$

$$Cn{+}y = G1 + P1\ G0 + P1\ P0\ Cn$$

$$Cn{+}z = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ Cn$$

$$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$$

$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

or

$$\overline{C}n{+}x = \overline{Y0\ (X0 + Cn)}$$

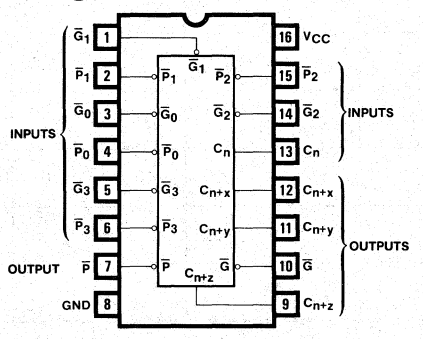
$$\overline{C}n{+}y = \overline{Y1\ [X1 + Y0\ (X0 + Cn)]}$$

$$\overline{C}n{+}z = \overline{Y2\ \{X2 + Y1\ [X1 + Y0\ (X0 + Cn)]\}}$$

$$Y = Y3\ (X3 + Y2)\ (X3 + X2 + Y1)\ (X3 + X2 + X1 + Y0)$$

$$X = X3 + X2 + X1 + X0$$

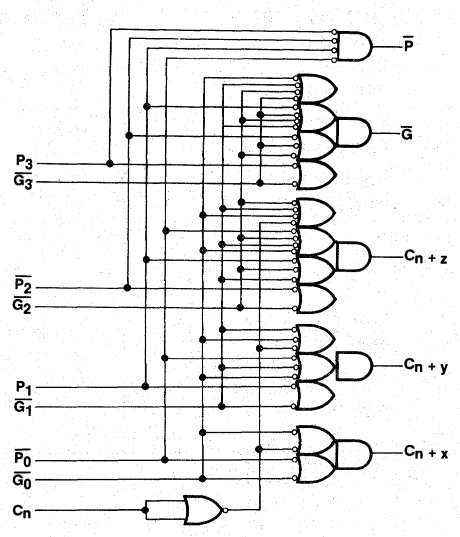
Pin Configuration



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S182	F,J,W,(20L)	Military
SN74S182	N,J	Commercial

Logic Diagram



Summarizing Tables

FUNCTION TABLE FOR C_{n+y} OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	Cn	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{C}_n$	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = High Level, L = Low Level, X = Irrelevant. Any inputs not shown in a given table are irrelevant with respect to that output.

TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 5.5 V
Storage temperature range .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2						V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5 V	Cn input			−2			−2	V
				$\overline{P3}$ input			−4			−4	mA
				$\overline{P2}$ input			−6			−6	mA
				$\overline{P0}$, $\overline{P1}$, or $\overline{G3}$ input			−8			−8	mA
				$\overline{G0}$ or $\overline{G2}$			−14			−14	mA
				$\overline{G1}$ input			−16			−16	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V	Cn input			50			50	µA
				$\overline{P3}$ input			100			100	µA
				$\overline{P2}$ input			150			150	µA
				$\overline{P0}$, $\overline{P1}$, or $\overline{G3}$ input			200			200	µA
				$\overline{G0}$ or $\overline{G2}$			350			350	µA
				$\overline{G1}$ input			400			400	µA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V				1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V, I_{OL} = 20 mA				0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V, I_{OH} = −1 mA		2.5	3.4		2.7	3.4		V
I_{OS}	Output short-circuit current*	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX	See Note 1			69	109		69	99	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = 5 V	See Note 2			35			35		mA

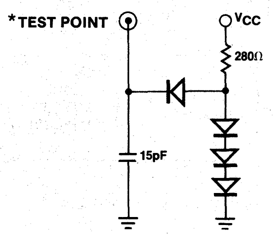
* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE: 1. I_{CCL} is measured with all outputs open, inputs $\overline{G0}$, $\overline{G1}$ and $\overline{G2}$ at 4.5 V, and all others inputs grounded.
2. I_{CCH} is measured with all outputs open, inputs $\overline{P3}$ and $\overline{G3}$ at 4.5 V, and all others inputs grounded.

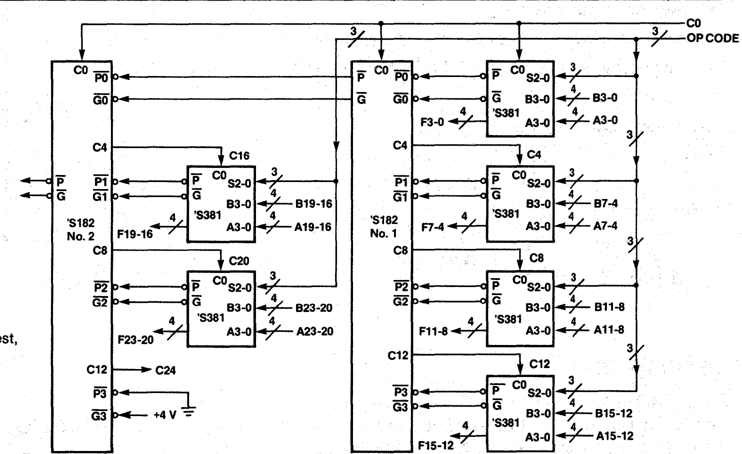
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	FROM (INPUT)	TO (OUTPUT)	5/74S182 TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high	C_L = 15 pF R_L = 280Ω	$\overline{G0}$,$\overline{G1}$,$\overline{G2}$,$\overline{G3}$	Cn + x, Cn + y or Cn + z	4.5	7	ns
t_{PHL}	Propagation delay time, high-to-low		$\overline{P0}$,$\overline{P1}$,$\overline{P2}$ or $\overline{P3}$		4.7	7	ns
t_{PLH}	Propagation delay time, low-to-high		$\overline{G0}$,$\overline{G1}$,$\overline{G2}$,$\overline{G3}$	$\overline{G}$	5	7.5	ns
t_{PHL}	Propagation delay time, high-to-low		$\overline{P1}$,$\overline{P2}$, or $\overline{P3}$		7	10.5	ns
t_{PLH}	Propagation delay, low-to-high		$\overline{P0}$,$\overline{P1}$,$\overline{P2}$ or $\overline{P3}$	$\overline{P}$	4.5	6.5	ns
t_{PHL}	Propagation delay, high-to-low				6.5	10	ns
t_{PLH}	Propagation delay, low-to-high		Cn	Cn + x, Cn + y or Cn + z	6.5	10	ns
t_{PHL}	Propagation delay high-to-low				7	10.5	ns

Standard Test Load

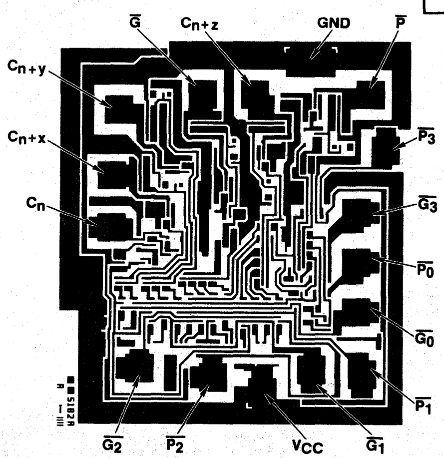


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



A 24-bit ALU made from 'S381s and 'S182s

Die Configuration



Die Size: 53x57 mil²

9

High-Speed Schottky Priority Encoders

SN54/74S148 (93S18)
SN54/74S348

Features/Benefits

- Second-generation Schottky designs feature VERY-High-Speed compared to other TTL priority encoders
- Totem-pole outputs on SN54/74S148
- Three-state outputs on SN54/74S348
- SN54/74S148 is speed upgrade for SN54/74148, SN54/74LS148, 9318, 93L18
- SN54/74S348 is speed upgrade for SN54/74LS348
- Encode eight data lines to 3-bit binary (octal) code
- Cascadable in several different ways
- Glitch on $\overline{GS}$ line in other TTL priority encoders has been designed out
- Applications include:
  - Interrupt/status scanning
  - Resource allocation in processors/peripherals
  - Normalization in floating-point arithmetic units
  - Bus arbitration
- Maximum Logic Delays:
  - $\overline{D_i}$ → $\overline{A_i}$ 13ns
  - $\overline{D_i}$ → $\overline{GS}$ 15ns
  - $\overline{D_i}$ → $\overline{EO}$ 15ns
    } 'S148 and 'S348
  - $t_{ZX}(E_i$ to $A_i)$ 18ns
  - $t_{XZ}(E_i$ to $A_i)$ 15ns
    } 'S348 Only

Description

The SN54/74S148 and SN54/74S348 high-speed Schottky TTL priority encoders scan 8 data-input lines, and output a 3-bit binary (that is, "octal") code which is the line number of the highest-priority data input being asserted. To allow expansion by cascading, in some cases without external logic, both devices provide three control signals: $\overline{EI}$ (Enable Input), $\overline{EO}$ (Enable Output), and $\overline{GS}$ (Group Select).

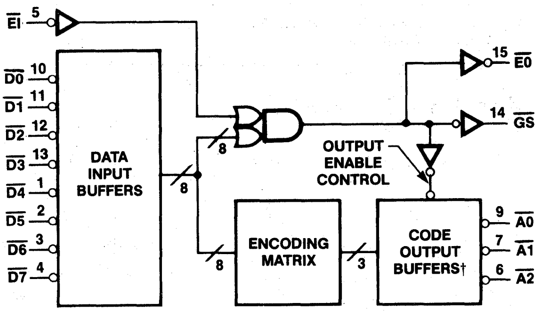
When $\overline{EI}$ is not being asserted, the code outputs are forced High in the 'S148 and into Hi-Z state in the 'S348. When $\overline{EI}$ is being asserted, these outputs are forced to the line-number code; see "Function Table." Also, when $\overline{EI}$ is being asserted, $\overline{EO}$ and $\overline{GS}$ are complementary; $\overline{EO}$ indicates that no data-input line is being asserted, whereas $\overline{GS}$ indicates that at least one of them is being asserted.

$\overline{EI}$ and $\overline{EO}$ may be used to link encoders together in a "daisy-chained" configuration. Also, in a two-level cascaded configuration, the $\overline{GS}$ signals from the first-level encoders are the data inputs for the second-level encoder(s); see "Applications."

Ordering Information

PART NUMBER	PKG	TEMP	OUTPUTS	POWER
SN54S148	J,F,W(20L)	Mil	Totem-pole	S
SN74S148	N,J	Com		
SN54S348	J,F,W(20L)	Mil	Three-state	
SN74S348	N,J	Com		

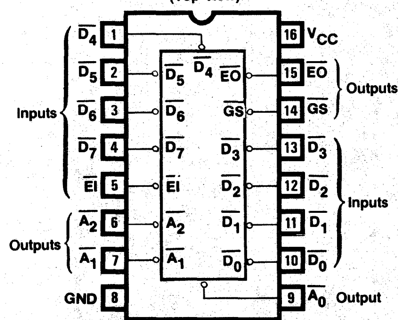
Block Diagram



† Disabled outputs are High for 54/74S148 and Hi-Z for 54/74S348.

Pin Configuration

SN54/74S148
SN54/74S348
(Top View)



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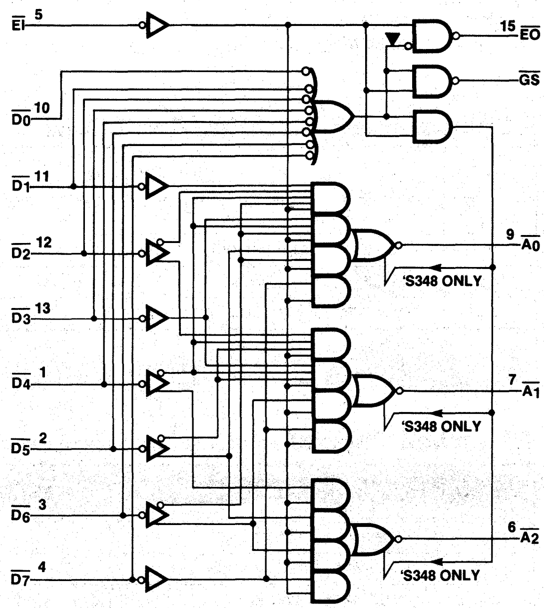
The line-number-code outputs ($\overline{A_2}$, $\overline{A_1}$, $\overline{A_0}$) are totem-pole in the 'S148 and are three-state in the 'S348. All inputs and outputs of both devices are TTL-compatible. Data inputs present *two* standard 54S/74S normalized loads; $\overline{EI}$, however, presents only a half of one such load.

The "Function Table" has been stated in terms of High (H) and Low (L) signal levels rather than in terms of "ones" and "zeroes." The most natural interpretation of the operation of these parts is that *all* signals, outputs as well as inputs, are *assertive-low* — that is, L is identified with "one" and H with "zero." Consequently, the highest-priority data input is named "D_7" and the output code it produces when asserted is LLL. In like manner, asserting the input D_4 produces the output code LHH if none of the higher-priority data-input lines D_7, D_6, or D_5 is being asserted; and so forth.

It is consistent with this interpretation that an 'S148 outputs a code of HHH either when it is disabled, or when it is enabled but none of its data inputs are being asserted. Under the same circumstances, the code outputs of an 'S348 go into Hi-Z state.

Logic Diagram



Function Table

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{D0}$	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$\overline{D4}$	$\overline{D5}$	$\overline{D6}$	$\overline{D7}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	$\overline{GS}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H/Z*	H/Z*	H/Z*	H	H
L	H	H	H	H	H	H	H	H	H/Z*	H/Z*	H/Z*	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

* NOTE: "H" for 'S148, "Z" for 'S348

Absolute Maximum Ratings

	Operating
Supply voltage V_{CC}	−0.5 V to 7 V
Input voltage	−1.5 V to 7 V
Off-state output voltage	−0.5 V to 5.5 V
Storage temperature range	−65° to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High level output current			−1			−1	mA
I_{OL}	Low level output current			20			20	mA
T_A	Operating free air temperature	−55		+125	0		+75	°C

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IH}	High-level input voltage		2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current, $\overline{EI}$ Input	V_{CC} = MAX V_I = 0.5V			−0.8			−0.8	mA
	Low-level input current, Any Input Except $\overline{EI}$				−3.2			−3.2	
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.7V			50			50	μA
I_I	Input current	V_{CC} = MAX V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V; I_{OL} = 20mA			.5			.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V; I_{OH} = −1.0mA	2.5	3.4		2.7	3.4		V
I_{OZL}	Off-state output current Low-level voltage applied ('S348 Only)	V_{CC} =MAX, V_{IL} = 0.8V, V_{IH} = 2V; V_O = 0.4V			−50			−50	μA
I_{OZH}	Off-state output current High-level voltage applied ('S348 Only)	V_{CC} =MAX, V_{IL} = 0.8V, V_{IH} = 2V; V_O = 2.7V			50			50	μA
I_{OS}	Short-circuit output current †	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current See note 1, 'S148	V_{CC} = MAX			115			110	mA
	'S348				125			120	

NOTE 1: I_{CC} is measured with inputs $\overline{D_7}$ and $\overline{EI}$ Low, other inputs High, and outputs open.

† Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	Low to High	$\overline{D_1}$ thru $\overline{D_7}$	$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$	C_L = 15pf, R_L = 280Ω		9	13	ns
t_{PHL}		High to Low					9	13	ns
t_{PLH}		Low to High	$\overline{D_0}$ thru $\overline{D_7}$	$\overline{GS}$			11	15	ns
t_{PHL}		High to Low					11	15	ns
t_{PLH}		Low to High		$\overline{EO}$			12	15	ns
t_{PHL}		High to Low					12	15	ns
t_{PLH}		Low to High	$\overline{EI}$	$\overline{GS}$			6	9	ns
t_{PHL}		High to Low					6	9	ns
SN54/74S148 ONLY									
t_{PLH}	Propagation delay	Low to High	$\overline{EI}$	$\overline{EO}$	C_L = 15pf, R_L = 280Ω		8	12	ns
t_{PHL}		High to Low					8	12	ns
t_{PLH}		Low to High		$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$			10	13	ns
t_{PHL}		High to Low					10	13	ns
SN54/74S348 ONLY									
t_{PLH}	Propagation delay	Low to High	$\overline{EI}$	$\overline{EO}$	C_L = 15pf		11	14	ns
t_{PHL}		High to Low			R_L = 280Ω		11	14	ns
t_{PZH}		Three-state to High		$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$	C_L = 50pf		12	18	ns
t_{PZL}		Three-state to Low			R_L = 280Ω		12	18	ns
t_{PHZ}		High to Three-state		$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$	C_L = 5pf		8	15	ns
t_{PLZ}		Low to Three-state			R_L = 280Ω		8	15	ns
t_{PZH}		Three-state to High	$\overline{D_0}$ thru $\overline{D_7}$*	$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$	N/A†		13		ns
t_{PZL}		Three-state to Low					13		ns
t_{PHZ}		High to Three-state		$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$			20		ns
t_{PLZ}		Low to Three-state					26		ns

* NOTE: Refer to second line of "Function Table".

† NOTE: These values are furnished for the purpose of estimating the logic delays of a combination such as shown in Fig. 1 and 2. They are design guidelines only and are not tested and therefore not guaranteed.

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Applications

The basic logic function performed by these priority encoders is to scan a parallel word of any length for the most-significant Low signal in a field of Highs. Although a single part has only 8 data inputs and hence can only scan a one-byte field, the architecture of these parts supports several different cascading schemes.

The Enable Input ($\overline{EI}$), when *not* being asserted, forces the code outputs ($\overline{A_2}$, $\overline{A_1}$, $\overline{A_0}$) High in an 'S148 or into Hi-Z (high-impedance) state in an 'S348. Since all input signals and all output signals for these parts are conventionally considered as assertive-low, the effect is to disable the code outputs in the manner appropriate for a totem-pole part ('S148) or a three-state part ('S348). When $\overline{EI}$ is asserted, the code outputs are forced to the code of the highest-priority data inputs being asserted; if no data input is being asserted, the code outputs remain as if the part were not enabled.

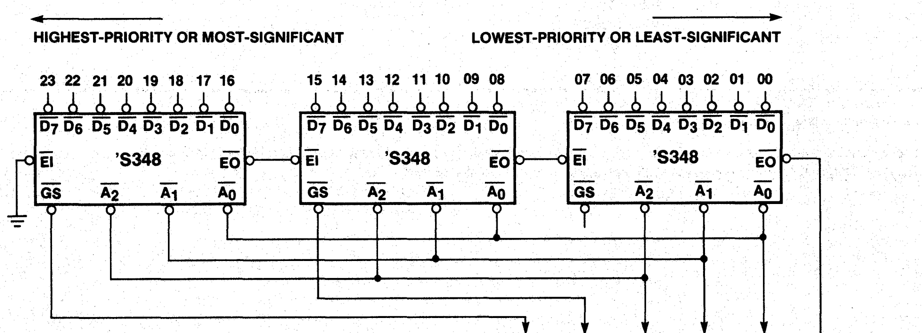
Also, when $\overline{EI}$ is being asserted, the $\overline{EO}$ and $\overline{GS}$ signals operate as complementary "presence" signals. When the encoder asserts $\overline{EO}$, this condition means that none of the data inputs for that encoder are being asserted, and that a lower-priority encoder should therefore be enabled to examine its data inputs. Thus, several encoders may be daisy-chained as in Figures 1 and 2, with $\overline{EO}$ from the highest-priority encoder controlling $\overline{EI}$ for the next-highest-priority encoder, and so forth. The highest-priority-encoder is always enabled. In such daisy-chain arrangements, code outputs may simply be bussed together if three-state encoders are being used, or combined using external assertive-low "OR" logic. Figure 1 illustrates a three-encoder daisy chain to scan 24 lines; a two-encoder daisy-chain may likewise be used to scan 16 lines. In each of these cases, no other components besides encoders are needed.

A slightly different approach is needed to scan more than 24 lines. Figure 2 shows a 64-line scanner which uses 9 'S348s and no other components. These encoders are on two "levels"; the $\overline{GS}$ outputs from the first-level encoders are the inputs for the second-level encoder, and indicate when asserted that the corresponding first-level encoders do indeed have inputs being asserted. The bussed first-level-encoder outputs form the least-significant octal digit of the 6-bit line-number code for the highest-priority data-input line being asserted; the outputs of the second-level encoder form the most-significant octal digit of this result. Figure 3 shows the highest-speed "totally-parallel" approach, which eliminates the potential delay due to daisy-chaining the enable signal through the first-level parts. The $\overline{EI}$ signals for all of the encoders are grounded, and an 8-way 3-bit multiplexer comprised of three 'S151s or three 'S251s is used to select the code outputs of the highest-priority first-level encoder which has any data-input lines being asserted. The address lines of these multiplexers are controlled by the code outputs of the second-level encoder.

Yet another cascading scheme, not shown, uses a single decoder such as an 'S138 instead of three multiplexers. The decoder's address-input lines are controlled by the second-level-encoder outputs as in Figure 3. Its outputs go to the $\overline{E1}$ inputs of the first-level encoders, so that *only* the highest-priority first-level encoder which has any data-input lines being asserted gets enabled. The first-level-encoder code outputs are bussed together as in Figure 2. This scheme is not quite as fast as that of Figure 3, but is faster than that of Figure 2 since the daisy-chaining delay is still eliminated.

The scheme of Figure 3 can be implemented with either totem-pole or three-state parts; the others require three-state parts. Additional schemes are possible. If more than 64 lines must be scanned, more than two levels of encoders can be used. Obviously, also, if only 48 or 56 lines must be scanned, a partially-populated version of one of the 64-bit schemes can do the job.

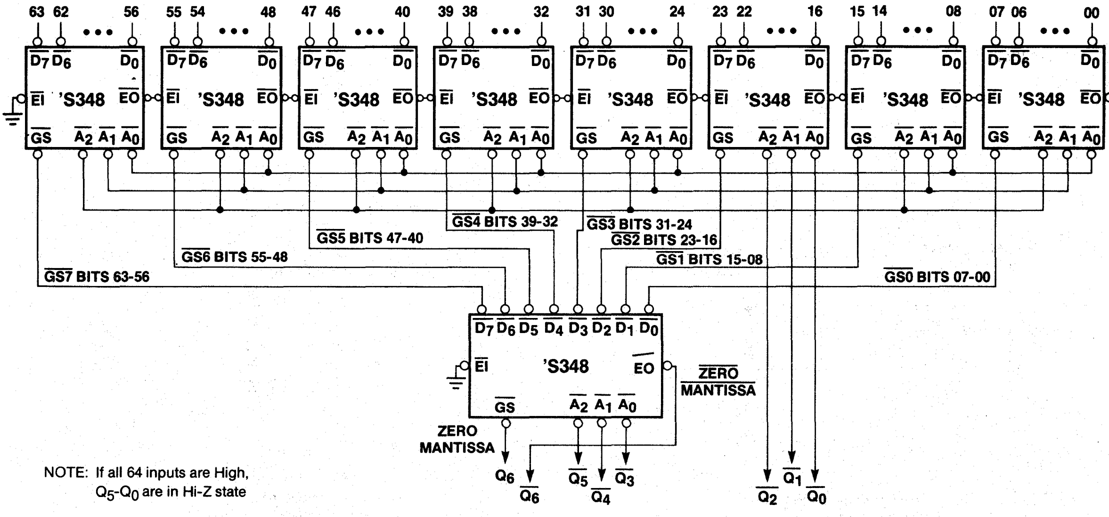
Although the original system purpose of priority encoders was to scan interrupt lines, they are also ideally suited for high-speed normalization scanning of the result of a floating-point adder/subtracter, in order to determine how many leading zeroes the result contains in order that the normalization shift may be performed in one operation by a "barrel shifter" or "matrix shifter." This result must be in "Negative Absolute Value" form because of the assertive-low behavior of the encoder. (See Monolithic Memories Application note AN-111, "Big, Fast, and Simple — Algorithms, Architecture, and Components for High-End-Superminis," by Ehud Gordon and Chuck Hastings, pages 7-8.) Another important application is "resource control" in computer systems having several semi-autonomous active units; for instance, a single encoder followed by a decoder can arbitrate requests on 8 bus-request lines and return a single bus-grant signal on one of 8 bus-grant lines.



NOTES: 1. The two 'S348s to the right form a 16-Bit Interrupt Scanner if $\overline{EI}$ for the middle one is grounded.

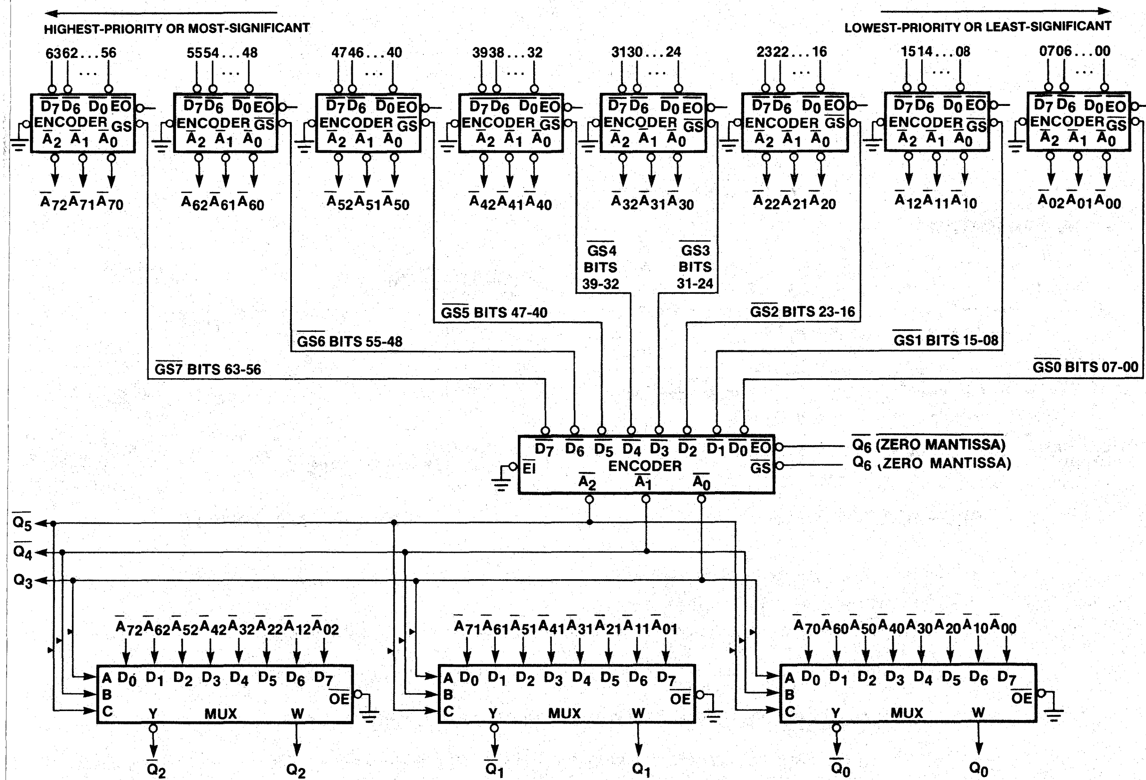
2. If all 24 inputs are High, $\overline{Q_2}$, $\overline{Q_1}$, and $\overline{Q_0}$ are in Hi-Z state; $\overline{Q_4}$ and $\overline{Q_3}$ are high.

Figure 1. 24-Bit Leading-Zeroes Detector or Interrupt Scanner Using 'S348s and No External Components



NOTE: If all 64 inputs are High, Q_5-Q_0 are in Hi-Z state

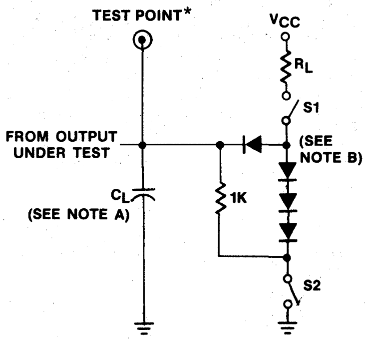
Figure 2. 64-Bit Leading-Zeroes Detector or Interrupt Scanner Using 'S348s and No External Components



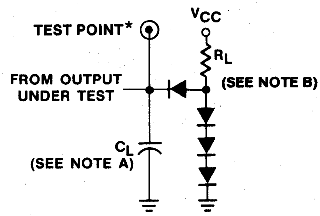
NOTE: Encoders here may be 'S148s or 'S348s; muxes may be 'S151s or 'S251s. If all 64 inputs are High, Q_5-Q_3 are in Hi-Z state, and Q_2-Q_0 are not meaningful.

Figure 3. Totally-Parallel 64-Bit Leading-Zeroes Detector or Interrupt Scanner

Test Loads



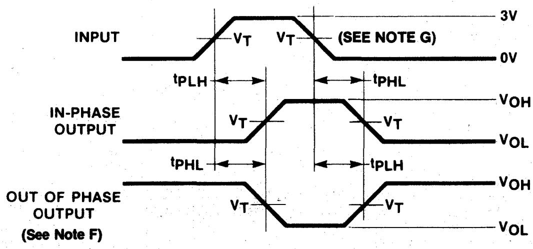
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



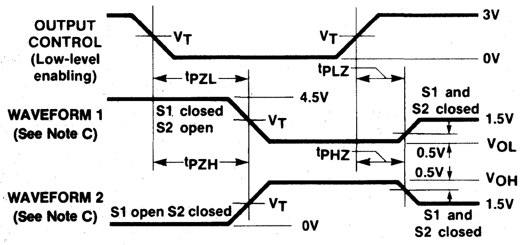
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



PROPAGATION DELAY

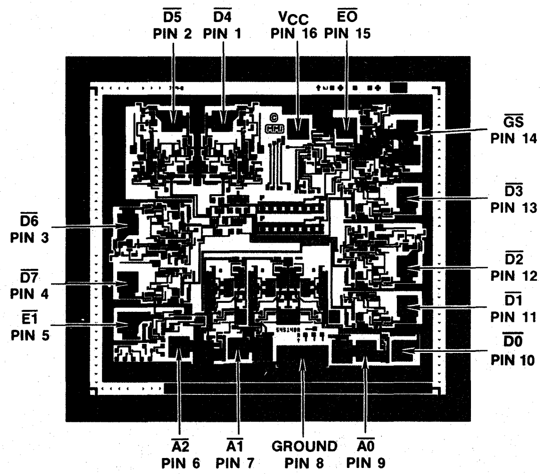


ENABLE AND DISABLE

NOTES:
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_{out} = 50Ω and:
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.
G. V_T = 1.5V

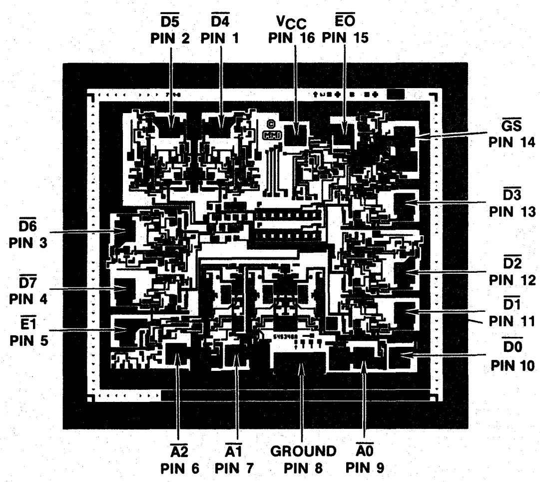
Die Configurations

SN54/74S148



Die Size: 81x70 mil^2

SN54/74S348



Die Size: 81x70 mil^2

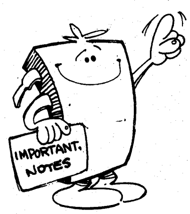

IMPORTANT
NOTES

Table of Contents
MULTIPLIERS/DIVIDERS

Multiplier/Divider Selection Guide

Co-Processor Multiplier/Divider with Accumulator

	PART NUMBER	MAX MULTIPLICATION TIME/ MAX DIVISION TIME	PINS
8 Bits	SN74S508 SN54S508	0.8 μs/2.2 μs	24
16 Bits	SN74S516	1.5 μs/3.5 μs	24

Cray Multipliers

DESCRIPTION	PART NUMBER	MAX DELAY	PINS
8x8 Multiplier (latched)	SN74S557	60 ns (X_i, Y_i, to S_{15})	40
8x8 Multiplier (latched)	SN54S557	60 ns	40
8x8 Multiplier (latched)	SN74S558	60 ns	40
8x8 Multiplier (latched)	SN54S557	60 ns	40
16x16 Multipliers	SN74S556	90 ns	84

Five New Ways to Go Forth and Multiply

Chuck Hastings

Our Multiplier Population Explosion

Recently it has seemed as if every time you turned around Monolithic Memories was announcing *another* new multiplier. Want to catch your breath, and find out where each of these fits into the overall scheme of things? Read on.

Actually, there have been five new multipliers in all within the last three years, plus two which had previously been available for several years. In time order of introduction, these are:

Parts No.	**Description**[A]
57/67558	150-nsec 8x8 Flow-Through Cray Multiplier[B]
57/67558-1	125-nsec 8x8 Flow-Through Cray Multiplier[B]
54/74S508	8-Bit Bus-Oriented Sequential Multiplier/Divider
54/74S558	60-nsec 8x8 Flow-Through Cray Multiplier
54/74S557	60-nsec 8x8 Flow-Through Cray Multiplier with Transparent Output Latches
54/74S516	16-Bit Bus-Oriented Sequential Multiplier/Divider
54/74S556	90-nsec 16x16 Flow-Through Cray Multiplier with Transparent Input and Output Latches

NOTES: A. Times are worst-case times for commercial-temperature-range parts.
B. Obsolete. 54/74S558 replaces these in both new and existing designs.

You will notice that the above parts fall into two categories: flow-through Cray multipliers, and bus-oriented sequential multiplier/dividers. Although all of these parts get referred to rather casually as "multipliers," there are major differences between the two general types; see Table 1 below.

The Cray Multipliers

The essential idea of a Cray multiplier, as originally put together by Seymour Cray in the late 1950s with discrete logic at Control Data Corporation, is to wire up an array of full adders in the form of a binary-arithmetic-multiplication pencil-and-paper example.[3] That is, everywhere that there is a "1" or a "0" in a longhand binary-multiplication example, the Cray type of multiplication uses a full adder. One may visualize a Cray multiplier functionally as a "diamond," as follows:

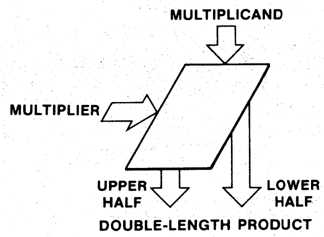


Figure 1. Pencil-and-Paper Analogy to Cray-Multiplier Operation

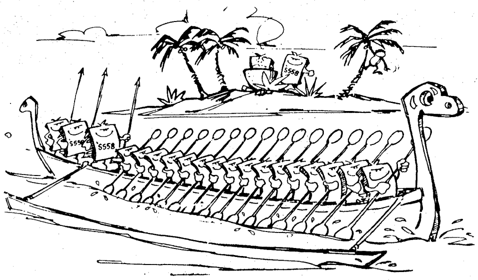
10

	Flow-Through Cray Multiplier	**Bus-Oriented Sequential Multiplier/Divider**
Role in System	*Building-block role* — as many as 34 parts used in one superminicomputer (NORD-500 from Norsk Data[1]).	*Co-processor role* — one, or occasionally two, parts used in one microcomputer[2].
Internal Operation	Static arithmetic-logic network; multiplies without being clocked[3] using eight bits of the multiplier at a time.	State machine; requires clocking to operate; contains edge-triggered registers; sequenced by a state counter; multiplies using two bits of the multiplier at a time[4].
External Control	Controlled by several mode-control input signals.	Controlled by sequences of micro-opcodes which come from a microprocessor, a registered PAL, or some other sequential-control device.
Package	40-pin DIP ('S557/8); 84-pin LCC or 88-pin PGA ('S556)	24-pin DIP.
Operations Performed	Can only perform multiplication.	Can perform multiplication, division, and multiplication-with-accumulation.
Storage Capabilities	Either no storage capabilities ('558 types), or optional storage for the double-length product only ('557 type), or full product and input storage ('556 type).	Four full-length registers; capable of storing both input operands and the double-length product.
Second Sources	8x8, Multiple-sourced (AMD, Fairchild, Monolithic Memories).	Sole-sourced; only bipolar *dividers* on the market.
Where Used	Initial usage has been in high-end minicomputers, array processors, and signal processors.	Initial usage has been in industrial-control microcomputers, digital modems, military avionics, CRT graphic systems, video games, and cartographic analysis systems.
Future Prospects	Potential large market today since these parts are now low-cost and multiple-sourced, and should be used in *all* new minicomputer designs!	Potential huge world-wide market for enhancement of microprocessor, bit-slice processor, and microcomputer capabilities, and for small-scale signal processing!

Table 1. A comparison of the two types of Monolithic Memories Multipliers

Our 57/67558, introduced in the mid-1970s, was the original *single-chip* Cray multiplier. To achieve what was for that time very high performance for a Schottky-TTL-technology part, the internal design of the 57/67558 also exploited other speed-freak multiplication techniques such as Booth multiplication[4] and Wallace-Tree addition[5]. All of these techniques achieve increased speed through extensive parallelism, and can be used at the system level as well as within LSI components. Subsequently, process improvements made it possible to offer a faster final-test option, the 57/67550-1, which attained a sales-volume level essentially equal to that of the original part.

About five years ago, AMD paid us the sincere compliment of second-sourcing these parts with the 75-nsec 25S558. Three years ago, we returned the compliment with the 60-nsec 54/74S558. All of these '558 parts, and the 70-nsec 54/74F558 announced by Fairchild, are fully compatible drop-in equivalents except for the variations in logic delay.



" ALL OF THESE TECHNIQUES ACHIEVE INCREASED SPEED THROUGH EXTENSIVE PARELLELISM."

When AMD introduced the 25S558, they introduced along with it the 80-nsec 25S557, a "metal option" of the same basic design with "transparent" output latches to hold the double-length product. "Transparent" means that the latches go away when you don't want them there; a latch-control line like that of the 54/74S373 controls whether these output latches store information, or simply behave as output buffers. Anyway, when we introduced our 54/74S558, we followed it within a few weeks with the 60-nsec 54/74S557, which is a much faster drop-in replacement for AMD's part. And subsequently, Fairchild has announced a 70-nsec 54/74F557.

Because AMD's 'S557 has the output latches implemented in TTL technology *after* the ECL-to-TTL converters, whereas our 'S557 has them implemented in ECL technology *before* the conversion, the latches operate much faster in ours. Our 'S557 is typically only about a nanosecond slower than our 'S558, whereas the logic-delay difference between AMD's two parts is considerably greater. Consequently, our margin of superiority over AMD for the 'S557 is even greater than for the 'S558.

More recently, we introduced the 90-nsec 'S556, which is a 16x16 direct size-upgrade of the 'S557/8 architecture, with the addition of input latches. In a "pipelined" mode, an 'S556 can produce a new 32-bit product every 75 nsec.

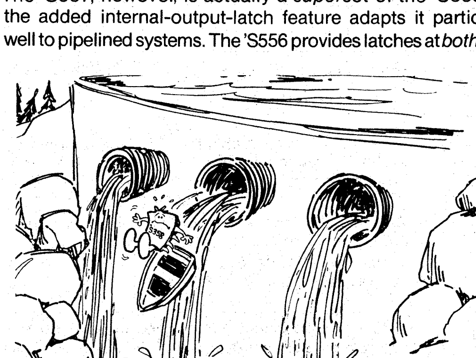
'S557/8 Cray multipliers come in a 40-pin dual-inline package, either ceramic or plastic. Worst-case power-supply current is 280 mA. The 'S556 comes in your choice of an 84-pin LCC (*L*eadless *C*hip *C*arrier) or an 88-pin PGA (*P*in-*G*rid *A*rray) package. Worst-case power-supply current is 800 mA (900 mA over military temperature range). The data-bus outputs can sink up to 8 mA I_{OL}, for all of these multipliers.

References 5 and 6 discuss technical approaches to using Cray multipliers in high-performance minicomputers. The 'S558, together with PROMs organized in a "Wallace-tree" configuration, can sail right along at the rate of four 56x56 multiplications every microsecond, on the basis of fixed-point arithmetic with no renormalization. (See table 7 on page 16 of reference 5; the multiplication time is 238 nsec for a "division step," which is a fixed-point multiplication, and 319 nsec for a floating-point multiplication where extra time is required for renormalization and correction of the exponent of the product.) 34 'S558s or 'S557s are required to perform this multiplication if the computer system architecture does not call for the computation of the least-significant half of the double-length product; 49 are required if it does.

"...THE 'S558, TOGETHER WITH PROMS ORGANIZED IN A "WALLACE-TREE" CONFIGURATION, CAN SAIL RIGHT ALONG AT THE RATE OF FOUR 56 x 56 MULTIPLICATIONS EVERY MICROSECOND... "

The "local" architecture of the multiplier section of a digital system can take two rather different forms. A minicomputer[5] which executes an unpredictable mixture of arithmetic and logical instructions one after the other, typically needs to be able to get the complete multiplication over and done with before going on to the next program step—which is probably not another multiplication. An array processor or digital correlator, however, tends to do very regular iterative computations; and the performance of such a system can often be greatly increased by a technique called "pipelining," in which the arithmetic unit consists of stages with registers or latches in between each stage, and partial computational results move from one stage to the next on each clock.

The "flow-through" architecture of the 'S558 works equally well in synchronous or asynchronous pipelined systems, but registers or latches must be provided externally. The 'S557, however, is actually a *superset* of the 'S558, and the added internal-output-latch feature adapts it particularly well to pipelined systems. The 'S556 provides latches at *both* ends.



"...THE 'FLOW-THROUGH' ARCHITECTURE OF THE 'S558 WORKS EQUALLY WELL IN SYNCHRONOUS OR ASYNCHRONOUS PIPELINED SYSTEMS... "

Even a smaller-scale system can make effective use of these parts. To return to the case of 56x56 multiplication, which corresponds to the word-length needed for multiplying mantissas in several popular floating-point-number formats, an iterative clocked scheme using just seven 8x8 multipliers, some adders, and an accumulator register can form the entire 112-bit double-length product in just seven multiply/add cycles. A number of mid-range minicomputers today multiply in this manner. The multipliers are configured as suggested by the following block diagram:

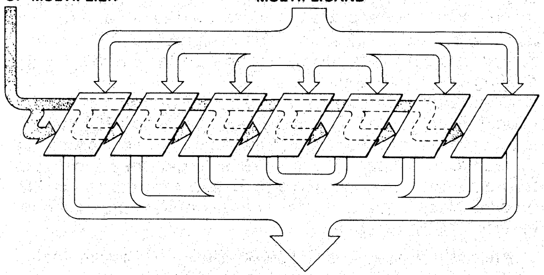


Figure 2. 8x56 Cray Multiplier In Diamond Representation

There is even an occasional 8-bit or 16-bit microprocessor-based system with a need for *very* fast multiplication, where 'S557/8s or 'S556s may get used as microprocessor peripherals[7,8]. Digital-video systems, in particular electronic games, with "vector graphic" capabilities are one example.

The world of 'S556/7/8 applications has turned out to include *all* sizes of minicomputers, digital video systems, and signal processors — FFT (Fast Fourier Transform) processors, voice recognition equipment, radar systems, digital correlators and filters, electronic seismographs, brain and body scanners, and so forth. And there are many unexpected off-beat applications, such as real-time data-rescaling circuits in instruments, altogether too numerous to list here. After all, an'S556 can multiply two 16-bit numbers together and output their entire 32-bit product in 90 nsec *worst case*...less time than it would take a speeding bullet to move the distance equal to the thickness of this piece of paper. How's that for Supermultiplier?

The Multiplier/Dividers

The Monolithic Memories 'S516 and 'S508 are state-of-the-art TTL-compatible intelligent peripherals for microprocessors, somewhere between arithmetic sequential circuits and specialized bipolar microprocessors. The 'S516 and 'S508 each can perform any of 28 different multiply and multiply-and-accumulate instructions, plus any of 13 different divide instructions, at bipolar speeds under the control of an internal state counter. (See Figure 2 of the 'S516 data sheet.) The state counter's sequence is in turn guided by 3-bit instruction codes which are external inputs to the 'S516/508. The 'S516 computes with 16-bit binary numbers, and the 'S508 computes with 8-bit binary numbers, as the part numbers none-too-subtly imply.

A 16-bit bi-directional data bus connects the 'S516 with the outside world for bringing in multipliers, multiplicands, dividends, and divisors; and returning products, quotients and remainders. It also has clock (CK) and run/wait ($\overline{GO}$) inputs, and an overflow indication (OVR) output.

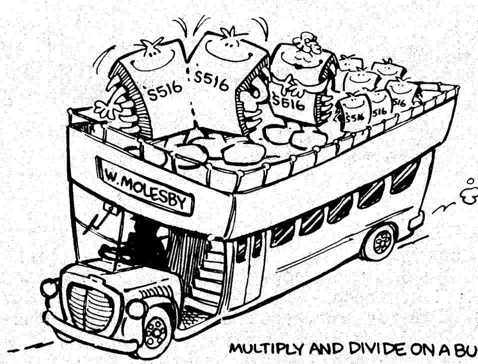
The 'S508 has all of the above inputs and outputs also, except that it has only an 8-bit bidirectional data bus. Since it comes in the same 24-pin package as the 'S516, it obviously has eight more pins available for other purposes. Four of these are used to bring out the internal-state-counter value; one each is used for a completion ($\overline{DONE}$) status output, an output-enable control (OE) input, and a master-reset ($\overline{MR}$) control input; and one is not used at all.

A simple, general interfacing scheme can be used to team a 'S516 with any of the currently popular 16-bit microprocessors,or an 'S508 with any 8-bit microprocessor. (See Figure 7 of the'S516 data sheet.) With a couple extra interface circuits, an'S516 can also be interfaced to an 8-bit microprocessor.Particularly if the system software is written in a highly-structured language such as PASCAL or FORTH, an'S516/508 can be retrofitted into an existing system with a large gain in performance and very little impact on either hardware or software — calls to the previous software-implemented one-step-at-a-time multiply and divide subroutines are simply rerouted to substitute a command from the microprocessor to the 'S516/508 to accept an operand and start its operation sequence.

The 'S516 and 'S508 are in fact two different "metal options" of one basic design; the 'S516 has twice as many data bits in each internal register. The 'S516 and 'S508 both have a worst-case clock rate of 6 MHz (commercial) or 5 MHz (military); the typical rate is 8 MHz. The simplest complete twos-complement 16x16 multiplication instruction can be performed in nine clock cycles by an 'S516, or in five by an 'S508, since 2-bits-at-a-time Booth multiplication is used;[4] thus, the worst-case time required by the 'S516 to multiply in this mode is 1.5 μsec for a commercial part, and for an 'S508 it is 833 nsec. On the same basis, 32/16 division can be done in 21 clock cycles, or 3.5 μsec worst-case, by an 'S516; and 16/8 division can be done in 13 clock cycles, or 2.2 μsec worst-case, by an 'S508.

An 'S516/508 can perform either positive or negative multiplication or multiply-accumulation, and many of the instructions provide for "chaining" of successive computations to eliminate extra operand transfers on the bus; these features further enhance the computational speed of the 'S516/508 in particular applications. Arithmetic can be either integer or fractional with respect to positioning of the results.

An 'S516 can powerfully enhance the capabilities of *any* present-day 16-bit or 8-bit microprocessor in a compute-bound application. In fact, it can be used in any digital system where there is a need to multiply and divide on a bus. An 'S508 can likewise enhance the capabilities of any 8-bit microprocessor.



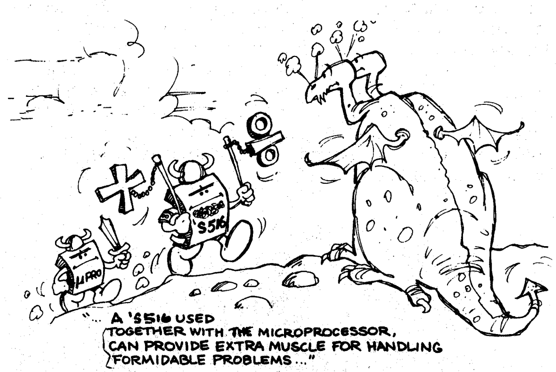
10

The 'S516 comes in an industry-standard 600-mil 24-pin dual-inline package, modified to include an integral aluminum heatsink which does not add appreciably to the package height. It requires only +5V and ground power connections, and draws a worst-case power-supply current of 450mA (commercial) or 500mA (military). Power consumption is greatest at cold temperatures, and decreases substantially as operating temperature increases. The 16 databus inputs require at most 0.25mA input current; the other inputs require at most 1mA. The 16 databus outputs can sink up to 8mA I_{OL}. The 'S508 also fits the above description, except that its worst-case power-supply current is 380mA (commercial) or 400mA (military), and it has only 8 databus inputs and outputs.

In describing applications of these parts, it is difficult to know where to start — they can be used in almost any design where a microprocessor can be used, and you know how many places that is today. So, perhaps a good starting point is to see what uses customers have thought up all by themselves. One customer even used *two* 'S516s in "pingpong" mode on a single 16-bit bus! So, rather than merely speculating as to what these parts *might* be good for, here's a list of what Monolithic Memories's customers have already *proven* they are good for:

- Real-time control of heavy machinery[9]
- Low-cost, high-performance digital modems
- CRT graphics, including video games
- Military avionics
- Cartographic analysis

As it happens, the above are 'S516 applications, except that digital modem designs have been done with both the 'S516 and the 'S508. Several of the 'S516 designs are already in production. In each of these applications, the microprocessor could have coped all right with the computational complexity, albeit at its own less-than-tremendous speed, but a 'S516 used together with the microprocessor can provide extra muscle for handling formidable problems.



Competition? Well, since there are no second sources for the 'S516, and no competitor at present has a similar fast part capable of performing division as well as multiplication, right now the 'S516 has no *direct* competition. Indirectly, there are some competing parts which perform *only* multiplication, and would have to perform division by Newton-Raphson iteration to be usable for any application where division is required. However, the 'S516 is (as far as we know) by far the lowest-priced *bipolar* 16-bit multiplier, and the other microprocessor peripheral chips which can perform division as well as multiplication are relatively-slow MOS devices. In one case, an 8-bit cascadable CMOS part requires a 50% reduction in clock rate to do 16-bit arithmetic. And considerable numerical-analysis and programming sophistication are required to implement Newton-Raphson division with *fixed-point* operands. (It's easier with floating-point operands.) In contrast, the 'S516/508 can be easily interfaced to almost any microprocessor using one or two PALs,® and can perform *either* multiplication or division on command.[2]

The 'S516 is so much faster than the competing MOS chips that it can even take them on for *floating-point* computations (which some of them are designed to do) and *win* . A conference paper[10] describes the design of an 'S516-based S-100-bus card capable of beating an Intel 8087 2:1 on floating-point arithmetic.

Some competing parts, in particular the AMI 2811 and Nippon Electric µPD7720, include an on-board ROM which must be mask-programmed at the factory, which makes life difficult for small companies (or even larger ones) which are trying to get a microprocessor-based product to market quickly. Also, some competing parts require sequencing by external TTL jellybeans.

And, as for using AMD/TRW 64-pin 16x16 Cray multiplier chips as microprocessor peripherals, these cost much more than the 'S516, occupy about three times the circuit-board space, multiply faster, don't divide at all except by Newton-Raphson iteration, and also require one or two "overhead" microprocessor instructions to interface for a given arithmetic operation. From a *system* viewpoint, when this overhead time is reckoned with, these chips provide little actual gain in multiply performance over the 'S516 at lots of extra cost, and an actual loss in divide performance: the 'S516 is *much more cost-effective overall.*

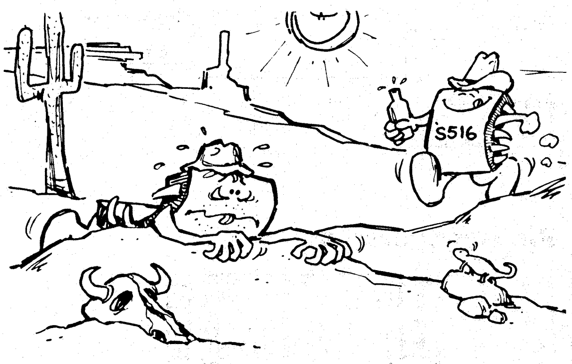
'S516s potentially fit into many, many places in commercial, industrial, and military electronics, particularly into small-scale real-time systems. The part is fast enough to enhance the performance of a 16-bit Motorola 68000, Zilog Z8000, or Intel 8086, as well as that of *any* 8-bit microprocessor. It is also fast enough to considerably improve the multiplication and division performance of 16-bit 2901-based "bit-slice" bipolar microcomputers, which are often used as processors in desktop graphics CRT terminals.

It is worth bringing the 'S516 to the attention of *any* designer who is developing:

- A personal computer or small business computer.
- A word processor, or a more grandiose "office automation system."
- A cruise missile, or any other "smart weapon."
- A digital modem.
- A small-scale speech-processing system. (These are *very* multiplication-intensive. We have one magazine article on the 'S516 in such an application.[11])
- A smart instrument, which does data conversion.
- An industrial control system, particularly one which must do many coordinate transformations.
- An all-digital studio-quality high-fidelity system.
- A cost-reduced computerized medical scanning system.
- A multiprocessor system for scientific computations.[12])

If an 'S516/508 is introduced into a system configured around an older microprocessor as a "co-processor" or helpmate for the microprocessor, and the application is arithmetic-intensive, the end effect can be a major upgrading of performance at the system level.[2-7] Consequently, a major reason for designing these parts in is *microprocessor life-cycle enhancement*. In particular, many MOS microprocessors have single-length and double-length add and subtract instructions: but either they have no multiply or divide instructions at all, or else they perform their multiply and divide instructions so slowly as to jeopardize the ability of the entire system to handle its computing load in real time.

So picture, if you will, the entrepreneur or chief engineer of a firm making a successful microprocessor-based widget which has been on the market for a few months, which uses an older 8-bit microprocessor such as a 6800 or 8085 or Z80. Just when his/her sales are really taking off, here comes a new start-up competitor with a similar system, using a Motorola 68000, with added features and faster performance made possible by the 68000's 16-bit word length and multiply/divide capabilities. The 'S516 can, in this instance, serve as a "great equalizer"—it can be retrofitted into the older system as previously described, and provides even higher-speed multiplication and division than the 68000. (Enough so, actually, that there are designers using the 'S516 *with* the 68000.) Thus, the 'S516 can dramatically extend the life cycle of existing microcomputer systems based on microprocessors which either don't have multiplication and division instructions, or perform these operations relatively slowly.



"... THE 'S516 CAN DRAMATICALLY EXTEND THE LIFE CYCLE OF EXISTING MICROCOMPUTER SYSTEMS BASED ON MICROPROCESSORS WHICH EITHER DON'T HAVE MULTIPLICATION AND DIVISION INSTRUCTIONS, OR PERFORM THESE OPERATIONS RELATIVELY SLOWLY..."

'S508s are somewhat easier to control from a logic-design viewpoint than 'S516s, purely because they have more control inputs and outputs. However, the shorter 'S508 word length makes the part naturally fit into smaller-scale systems than those which might use an 'S516. Essentially, the 'S508 is optimized for small-scale systems.

Now that you know what these parts are, can't you think of at least half a dozen prime uses for them right in your own back yard?

References (all available from Monolithic Memories)

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2. "SN54/74S516 Co-Processor Supercharges 68000 arithmetic," Richard Wm. Blasco, Vincent Coli, Chuck Hastings and Suneel Rajpal, Monolithic Memories Application Note AN-114.
3. "How to Design Superspeed Cray Multipliers with 558s," Chuck Hastings, included within the SN54/74S557/8 data sheet.
4. "Doing Your Own Thing in High-Speed Digital Arithmetic," Chuck Hastings, Monolithic Memories Conference Proceedings reprint CP-102.
5. "Big, Fast, and Simple — Algorithms, Architecture, and Components for High-End Superminis," Ehud Gordon and Chuck Hastings, Monolithic Memories Application Note AN-111.
6. "Fast 64x64 Multiplication using 16x16 Flow-Through Multipliers and Wallace Trees," Marvin Fox, Chuck Hastings and Suneel Rajpal, Monolithic Memories Conference Proceedings reprint CP-111.
7. "An 8x8 Multiplier and 8-bit μp Perform 16x16 Bit Multiplication," Shai Mor, *EDN,* November 5, 1979. Monolithic Memories Article Reprint AR-109.
8. "Using a 16x16 Cray Multiplier as a 16-Bit Microprocessor Peripheral to Perform 32-Bit Multiplication and Division," Chuck Hastings, Monolithic Memories Conference Proceedings reprint CP-140
9. "The Design and Application of a High-Speed Multiply/Divide Board for the STD Bus," Michael Linse, Gary Oliver, Kirk Bailey, and Michael Alan Baxter, Monolithic Memories Application Note AN-115.
10. "Minimum Chip-Count Number Cruncher Uses Bipolar Co-Processor," C. Hastings, E. Gordon, and R. Blasco. Monolithic Memories Conference Proceedings reprint CP-109.
11. "Medium-speed Multipliers Trim Cost, Shrink Band-width in Speed Transmission," Shlomo Waser and Allen Peterson, *Electronic Design,* February 1, 1979; pages 58-65. Monolithic Memories Article Reprint AR-107.
12. "A Synchronous Multi-Microprocessor System for Implementing Digital Signal Processing Algorithms," T.P. Barnwell, III and C.J.M. Hodges, *Southcon/82 Professional Program Session Record,* Session 21 reprint, paper 21/4.

8x8 Multiplier/Divider
SN54/74S508

Features/Benefits

- Co-processor for enhancing the arithmetic speed of all present 8-bit microprocessors
- Bus-oriented organization
- 24-pin package
- 8/8 or 16/8 division in less than 2.2 μsec
- 8x8 multiplication in less than .8 μsec
- 28 different multiplication instructions such as "fractional multiply and accumulate"
- 13 different divide instructions
- Self-contained and microprogrammable

Description

The SN54/74S508 ('S508) is a bus-organized 8x8 Multiplier/Divider. The device provides both multiplication and division of 2s-complement 8-bit numbers at high speed. There are 28 different multiply options, including: positive and negative multiply, positive and negative accumulation, multiplication by a constant, and both single-length and double-length addition in conjunction with multiplication. 13 different divide options allow single-length or double-length division, division of a previously-generated result, division by a constant, and continued division of a remainder or quotient.

The 'S508 is a time-sequenced device requiring a single clock. It loads operands from, and presents results to, a bidirectional 8-bit bus. Loading of the operands, reading of the results, and sequential control of the device is performed by a 3-bit instruction field.

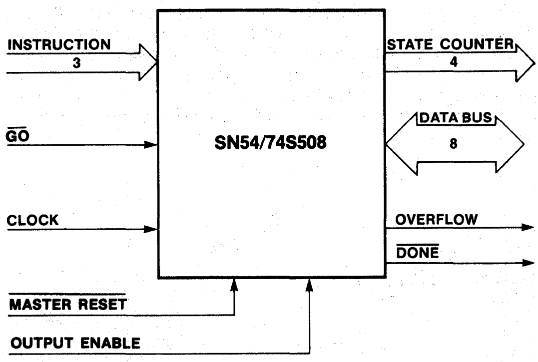
The 'S508 has the additional feature that operands and results can be either integers or fractions; when it deals with fractions, automatic scaling occurs. Results can be rounded if required, and an Overflow output indicates whenever a result is outside the normally-accepted number range.

For a simple multiplication of two operands and reading of the double-length result, the device takes five clock periods — one for initialization, and four for the actual multiplication. A typical clock period is 125 ns, which gives a multiplication time of 500 ns typical for 8x8 multiplication, plus 125 ns additionally for initialization, or 625 ns in all. More complex multiplications will take additional clock periods for loading the additional operands. A simple division operation requires 8 + 4 = 12 clock periods for a typical time of 1.5 μs (16 bits/8 bits), also plus 125 ns for initialization, or 1.625 μs in all.

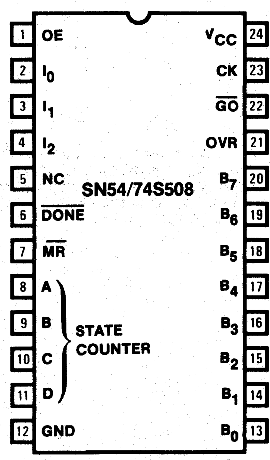
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S508	D24	Military
SN74S508	D24	Commercial

Logic Symbol



Pin Configuration



INSTRUCTION SEQUENCE				OPERATION	CLOCK CYCLES
ARITHMETIC OPERATIONS					
			0	$X1 \cdot Y$	5
			1	$-X1 \cdot Y$	5
			2	$X1 \cdot Y + K_Z, K_W$	5
			3	$-X1 \cdot Y + K_Z, K_W$	5
			4	$K_Z, K_W/X1$	13
		5/6	0	$X \cdot Y$	6
		5/6	1	$-X \cdot Y$	6
		5/6	2	$X \cdot Y + K_Z, K_W$	6
		5/6	3	$-X \cdot Y + K_Z, K_W$	6
		5/6	4	K_W/X	14
		5/6	5	K_Z/X	14
	5/6	6	0	$X \cdot Y + Z$	7
	5/6	6	1	$-X \cdot Y + Z$	7
	5/6	6	2	$X \cdot Y + K_Z \cdot 2^{-8}$	7
	5/6	6	3	$-X \cdot Y + K_Z \cdot 2^{-8}$	7
	5/6	6	4	Z, W/X	15
	5/6	6	5	Z/X	15
5/6	6	6	0	$X \cdot Y + Z, W$	8
5/6	6	6	1	$-X \cdot Y + Z, W$	8
5/6	6	6	2	$X \cdot Y + W_{sign}$	8
5/6	6	6	3	$-X \cdot Y + W_{sign}$	8
5/6	6	6	4	W/X	16
5/6	6	6	5	W_{sign}/X	16
5/6	6	6	6	(See Note 9 below)	—
5/6	5/6	6	7	Load X, Load Z, Load W, Clear Z	3
READING OPERATIONS					
			7	Read Z	1
		7	7	Read Z, W	2
	7	7	7	Read Z, W, Z	3
7	7	7	7	Read Z, W, Z, W	4
		5	7	Round, then Read Z	2
	5	7	7	Round, then Read Z, W	3

NOTES:
1. X,Y are input multiplier and multiplicand.
2. X1 is the previous contents of the first rank of the X register, (either the old X or a new X).
3. Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.
4. Z, W is a double-precision number. Z is the most significant half. Z, W represents addend upon input, and product (or accumulated sum) after multiplication.
5. K_Z, K_W represents previous accumulator contents. K_Z is the most-significant half.
6. W_{sign} is a single-length signed number, with sign extension.
7. Maximum clock cycle = 167 ns for a 6-MHz clock.
8. If n instruction codes are shown at the left under "instruction sequences," the number of clock cycles at the right is n+4 for multiplication and n+12 for division.
9. The code "5/6 6 6 6" represents an incomplete operation since it leaves the 'S508 in state 1 rather than in state 0, 8, or 10

Figure 1. 'S508 Instruction Set (Partial List)

SUMMARY OF SIGNALS/PINS	
B_7-B_0	Bidirectional data bus inputs/outputs
I_2-I_0	Instruction (sequential control) input
A, B, C, D	Internal-state-counter outputs
CK	Clock pulse input
$\overline{GO}$	Chip activation input
OE	Output enable input
$\overline{MR}$	Master reset input
OVR	Arithmetic overflow output
$\overline{DONE}$	Arithmetic-operation completion output

Description (continued)

The 'S508 device uses standard low-power Schottky technology, requires a single +5V power supply, and is fully TTL compatible. Bus inputs require at most 250 μA input current, and control and clock inputs require at most 1 mA input current. Bus outputs are three-state, and are capable of sinking 8 mA at the low logic level. The 'S508 is available in both commercial-temperature and military-temperature ranges, in a 600-mil 24-pin dual-in-line ceramic package.

Device Operation

The 'S508 contains four 8-bit working registers. Y is the multiplier register; X is the multiplicand and divisor register; W is the least-significant half of a double-length accumulator, and holds the least-significant half of the product after a multiplication operation, or the remainder after a division operation; and Z is the most-significant half of this same accumulator. In addition to these registers, there is a high-speed arithmetic unit which performs addition, subtraction, and shifting steps in order to accomplish the various arithmetic operations; a loading sequencer; and a PLA control network.

Operands are loaded into the working registers in time sequence at each clock period, under the control of this sequencer. The chip-activation signal $\overline{GO}$ must be LOW in order to begin the loading process and continue to the next step in the loading operation. If $\overline{GO}$ is continually held HIGH, the 'S508 remains in a wait state with its outputs held in their high-impedance states, so that the other devices attached to the bus may drive it. In this condition, the 'S508 does not respond to any codes on its instruction inputs; in effect, it does not "wake up" until $\overline{GO}$ goes LOW. Also, $\overline{GO}$ may change only when the clock input CK is HIGH. After all of the operands are loaded, the 'S508 jumps to the multiply routine, or to the divide routine, and performs the required operations as indicated in Figure 1. After 5 clock periods for a simple multiply or 13 clock periods for a simple divide, for example, the device is ready to place the result on the bus in time sequence.

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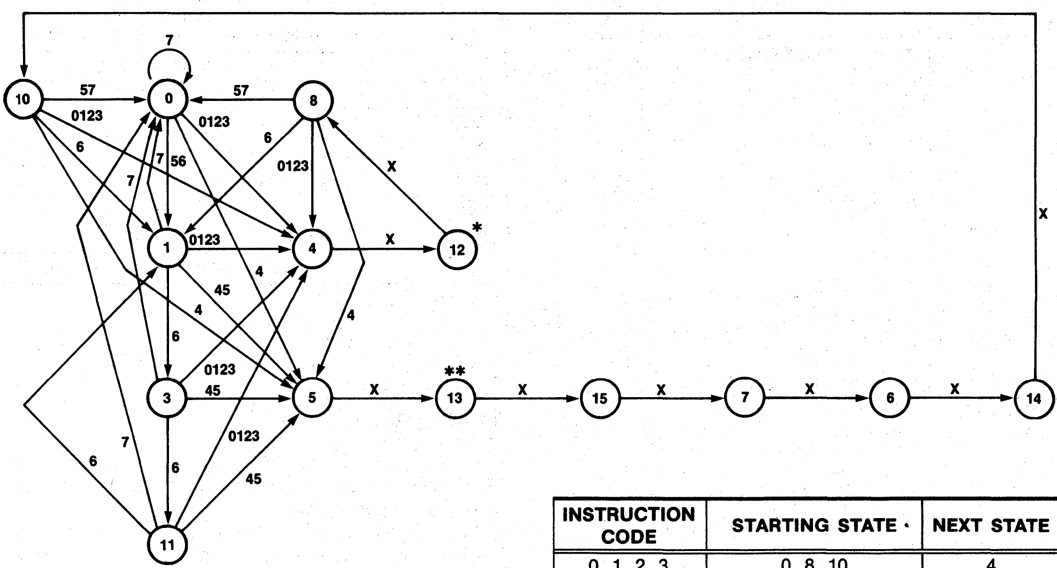


*Loop 3 times for multiplication.
**Loop 6 times for fractional division, or 7 times for integer division.

INSTRUCTION CODE	STARTING STATE ·	NEXT STATE
0, 1, 2, 3	0, 8, 10	4
4	0, 8, 10	5
5	0	1
5, 7	8, 10	0
6	0, 8, 10	1
7	0, 8, 10	0

KEY:

The numbers inside the circles indicate the *state* of the 'S508 multiplier/divider. These states are represented by a four-bit state counter, where A is the least-significant bit of this state counter and D is the most-significant bit. These four bits are available externally on the 'S508.

The next state of the 'S508 is a function of the present state and the instruction lines. For example if the 'S508 is at state 0 and the instruction is 0, 1, 2, or 3, then the next state is state 4 (multiply instruction); if the instruction is 4, the next state is state 5 (divide instruction); and so forth. The instructions which take the 'S508 from one state to another are indicated by the numbers written next to the state-transition path lines. "0123," for instance, implies that *any* of instructions 0, 1, 2, or 3 will take the 'S508 along the path marked "0123."

"X" next to a path implies that the path will be followed regardless of the value of the instruction inputs at that time. In other words, for the purpose of state transitions, X means "don't care." There are cases, however, where the particular instruction used may affect when the contents of the registers are available on the bus — see Figures 9 and 10 for contrasting examples of how this effect operates.

Figure 2. Transition Diagram for the 'S508 Multiplier/Divider

Three instruction inputs I_2, I_1, I_0, which may change only when the clock input CK is HIGH, select the required function and drive the sequencer from state to state. Thus, the action of the multiplier/divider at any clock period is a function of the machine state and the state of the control inputs. Figure 2 shows the multiply/divide state table, and all possible operations. After a Read or Round operation, the machine is driven back to state 0, and a new sequence of arithmetic operations is assumed. If a chain operation is being performed, such as accumulation of products, state 0 is bypassed, and loading of an operand or jumping to the next arithmetic operation occurs at the end of the previous arithmetic operation — at state 8 for a multiplication instruction, or at state 10 for a division instruction.

Register X is a dual-rank register, which allows the loading of an operand X during the multiplication or division process. If the machine enters the loading sequence and a new X operand has not been loaded, then the machine proceeds with the previously-loaded X, denoted in this text as "X1." This loading-while-processing capability allows a cycle to be saved during "chained" calculations, and also allows multiplication and division by a constant. (See Figure 13). (continued next page)

Figures 3 and 4 show the codes and durations for the 41 different possible arithmetic operations. These operations can be concatenated in strings to perform complicated 2s-complement arithmetic operations at high-speed. Rounding and reading of results can be performed after any operation. Figure 5 is a block diagram of the 'S508 8x8 Multiplier/Divider.

(continued page after next)

OPERATION		TIME-SLOT 1	2	3	4	5	6	7	8
$X1 \cdot Y$	INS CODE	0	MULTIPLY						
	BUS	Y							
$-X1 \cdot Y$	INS CODE	1	MULTIPLY						
	BUS	Y							
$X1 \cdot Y + K_Z, K_W$	INS CODE	2	MULTIPLY						
	BUS	Y							
$-X1 \cdot Y + K_Z, K_W$	INS CODE	3	MULTIPLY						
	BUS	Y							
$X \cdot Y$	INS CODE	5/6	0	MULTIPLY					
	BUS	X	Y						
$-X \cdot Y$	INS CODE	5/6	1	MULTIPLY					
	BUS	X	Y						
$X \cdot Y + K_Z, K_W$	INS CODE	5/6	2	MULTIPLY					
	BUS	X	Y						
$-X \cdot Y + K_Z, K_W$	INS CODE	5/6	3	MULTIPLY					
	BUS	X	Y						
$X \cdot Y + Z$	INS CODE	5/6	6	0	MULTIPLY				
	BUS	X	Z	Y					
$-X \cdot Y + Z$	INS CODE	5/6	6	1	MULTIPLY				
	BUS	X	Z	Y					
$X \cdot Y + K_Z \cdot 2^{-8}$	INS CODE	5/6	6	2	MULTIPLY				
	BUS	X	—	Y					
$-X \cdot Y + K_Z \cdot 2^{-8}$	INS CODE	5/6	6	3	MULTIPLY				
	BUS	X	—	Y					
$X \cdot Y + Z, W$	INS CODE	5/6	6	6	0	MULTIPLY			
	BUS	X	Z	W	Y				
$-X \cdot Y + Z, W$	INS CODE	5/6	6	6	1	MULTIPLY			
	BUS	X	Z	W	Y				
$X \cdot Y + W_{sign}$	INS CODE	5/6	6	6	2	MULTIPLY			
	BUS	X	—	W	Y				
$-X \cdot Y + W_{sign}$	INS CODE	5/6	6	6	3	MULTIPLY			
	BUS	X	—	W	Y				

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).
2) $K_Z \cdot 2^{-8}$ is a single-length signed number comprising the most-significant half of the previous double-length product and here gets added in at the least-significant end of the new result.
3) W_{sign} is a single-length signed number, with sign-extension as needed.
4) Fractional or integer arithmetic is specified by having the next-to-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.

Figure 3. Multiplication Codes and Times for 8x8 Multiplication in the 'S508

10

OPERATION		TIME-SLOT 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
K_Z, K_W/X_1	INS CODE	4	DIVIDE											1			
	BUS	—															
K_W/X	INS CODE	5/6	4	DIVIDE											1		
	BUS	X	—														
K_Z/X	INS CODE	5/6	5	DIVIDE											1		
	BUS	X	—														
Z, W/X	INS CODE	5/6	6	4	DIVIDE											1	
	BUS	X	Z	W													
Z/X	INS CODE	5/6	6	5	DIVIDE											1	
	BUS	X	Z	—													
W/X	INS CODE	5/6	6	6	4	DIVIDE											1
	BUS	X	—	W	—												
W_{sign}/X	INS CODE	5/6	6	6	5	DIVIDE											1
	BUS	X	0	W	—												

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).
2) Fractional division divides a 16-bit 2s-complement number in 1 clock period less than integer division.
3) W_{sign} is a single-length signed number, with sign-extension as needed.
4) Division operation W_{sign}/X requires that the Z register be initialized with all-zero contents at the time Z is loaded.
5) Fractional or integer arithmetic is specified by having the operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions, one of which does fractional arithmetic and one of which does integer arithmetic.

Figure 4. Division Codes and Time for 16/8 Division in 'S508

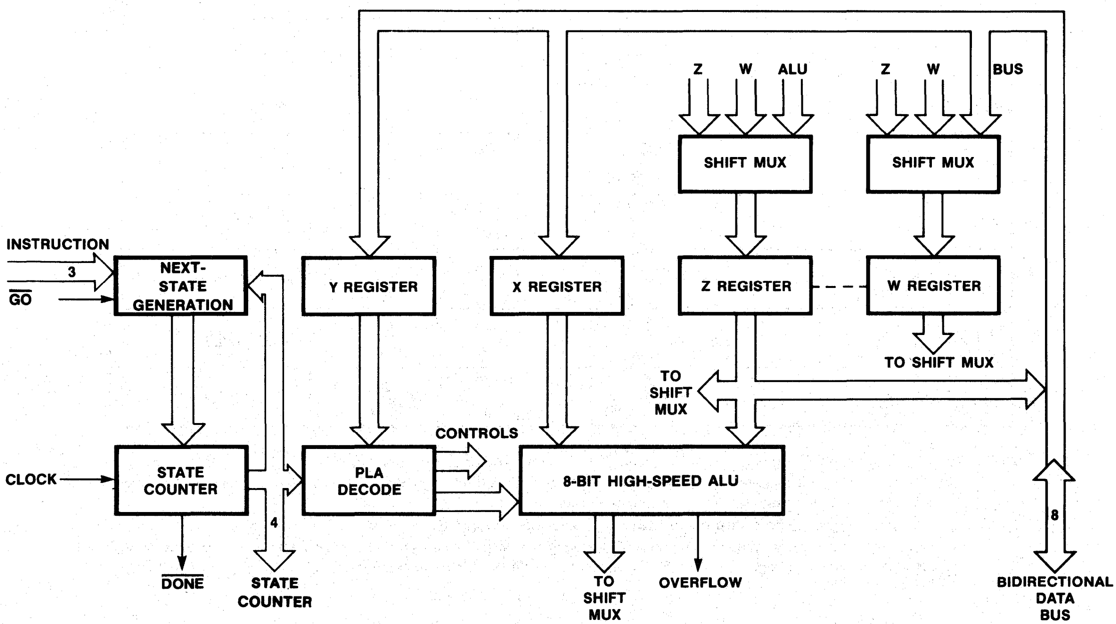


Figure 5. Internal Architecture of the 'S508

Multiplication

The 'S508 provides 2s-complement 8-bit multiplication, and can also accumulate previously-generated double-length products. No time penalty is incurred for accumulation, since the machine accumulates while the multiplication operation is proceeding. In addition to accumulation, the device can add into a product either a single-length or a double-length number. It can also use a previously-loaded operand as a constant, so that constant multiplication and accumulation is possible.

One key feature is the ability to perform both positive multiplications and negative multiplications, again without any speed penalty. This feature allows complex-arithmetic multiplications to be programmed with very little overhead. Another important feature is the ability to work with either fractions or integers.

Division

The 'S508 also provides a range of division operations. A double-length number in Z,W is divided by X; the result Q is stored in Z, and the remainder R in W. Again all numbers are in the 2s-complement number representation, with the most significant bit of an operand (whether single-length or double-length) having a negative weight. In order to facilitate repeated division, with the multiple-length quotient always keeping the same sign, the remainder is always the same sign as the dividend. Fractional or integer operation is possible, and division and multiplication operations can be concatenated. For example, the operations (AxB)/C, (A+B)/C can easily be performed. The dividend can be any previously-generated result — product, quotient, or remainder; or it may be a double-length or single-length signed operand.

Reading Results

The result of an arithmetic operation, or of a string of operations, can be read onto the 8-bit bus if the machine is at the end of an operation or at the start of a new sequence. The read operation requires that the $\overline{GO}$ signal be held LOW so that the information is read out onto the bidirectional bus, when code 7 is specified. (See Figure 6.) Since there is a double-length accumulator Z,W, reading can take two cycles. First, register Z is read. After another clock has been received, if code 7 is still present, the least-significant half of the product from the W register is placed on the bus, or likewise the remainder if a division operation had been performed.

If the 'S508 is instructed to perform a read operation during the loading sequence, then the sequence is broken and the machine is forced back to state 0 ready to start the sequence again. Continual read operations at state 0 just swap the contents of register Z and W.

The 'S508 has a direct master reset input $\overline{MR}$. Alternatively, initialization of the 'S508 can also easily be performed by continually presenting instruction code 7, which after a maximum of 13 clock periods forces the machine back to state 0.

Integer and Fractional Arithmetic

The 'S508 can work with either fractional or integer number representations. When working with integers, all numbers are scaled from the least-significant end and the least-significant bit is assumed to have a weight of 2^0. For integer multiplication, accumulation, and division, all numbers are scaled from this least-significant weight, and results are correct if interpreted in this manner. The double-length register Z,W can therefore hold numbers in the range -2^{15} to $+2^{15}-1$; the operands X and Y, and single-length results, are in the range -2^7 to $+2^7-1$.

When working with fractions, the machine automatically performs scaling so that input operands and results have a consistent format. All numbers in the fractional representation are scaled from the most significant end, which has a weight of -2^0 *(negative)*. The binary point is one place to the right of this most-significant bit, so that the next bit has a weight of 2^{-1}. The double-length register Z,W therefore holds numbers in the range -1 to $+1-2^{-15}$ and the operands X and Y and single-length results are in the range -1 to $+1-2^7$. Since automatic scaling occurs, the product of two numbers always has the least-significant bit as a 0, unless an accumulation is performed with the least-significant bit being a 1.

During a chain operation with the partial results not being read onto the bus, the 'S508 will stay in either the fractional or integer mode. At the start of a sequence of operations, fractional or integer operation is designated by loading operands using instruction code 5 or instruction code 6 respectively.

Mixed fractional and integer arithmetic is also possible, by redefining the weight of the least-significant or most-significant bits. However, care must be exercised, due to the automatic scaling feature, when fractional arithmetic is programmed.

Rounding

Rounding can be performed on the result of a multiplication or division. Generally rounding would only be called out during fractional operation, but nothing in the 'S508 precludes forming a rounded result during integer arithmetic.

Rounding for multiplication provides the best single-length most-significant half of the product. Rounding occurs at the end of a multiplication, and is performed instead of a Load or Read operation when a code 5 is specified, instead of a code 7, to get from state 8 or state 10 back to state 0. (See Figure 2; also, note that this mode of operation precludes "stealing" a cycle according to the method illustrated in Figure 9.) The 'S508 looks at the most-significant bit of the least-significant half of the product W_7, and adds 1 to the most-significant half of the product at the least-significant end if W_7 is a 1. After the operation, the 'S508 is in state 0, so that the rounded product can be read, and the W register is clear.

Rounding for division is performed by forcing the least-significant bit of the quotient in Z to a 1 unless the division is exact (remainder is zero). This method of rounding causes a slightly higher variance in the result than having an additional iterative division operation, but is considerably easier to perform. Again, after rounding the 'S508 goes to state 0, so that a read operation can be performed, and the W register is clear.

10

Overflow

The 'S508 has an overflow output OVR which is cleared prior to each operation, and is set during an operation if the product or quotient goes outside the normally-accepted range.

For multiplication, overflow can only occur if the most negative number in the operand range is used: $(-1)x(-1)=+1$, which cannot be held in the 'S508's internal registers. Overflow can more easily occur during either positive or negative accumulation of products. For fractional arithmetic, if the product or accumulation goes outside the range of -1 to $+1-2^{-15}$, then the overflow flipflop will be set.

Overflow may also occur during division if the quotient goes outside the generally-accepted number range of -1 to $+1-2^{-7}$ during fractional operation. This would occur if the divisor is less than the dividend, or equal to the dividend if a positive quotient is being generated. For integer arithmetic the numbers must be scaled by 2^7.

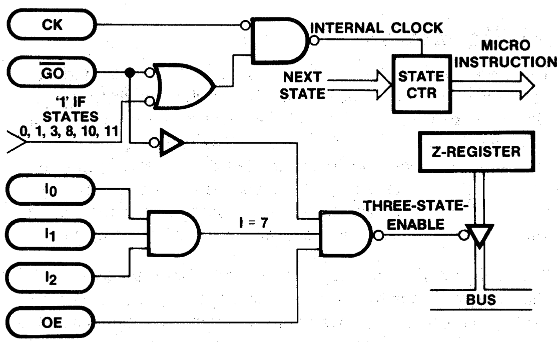


Figure 6. 'S508 Internal Circuitry of "$\overline{GO}$" Line and Three-State-Enable

During the states 0, 1, 2, 3, 8, 10 and 11 if the "GO" line ($\overline{GO}$) is held at logic HIGH then the machine will be in a wait state until $\overline{GO}$ goes to logic LOW.

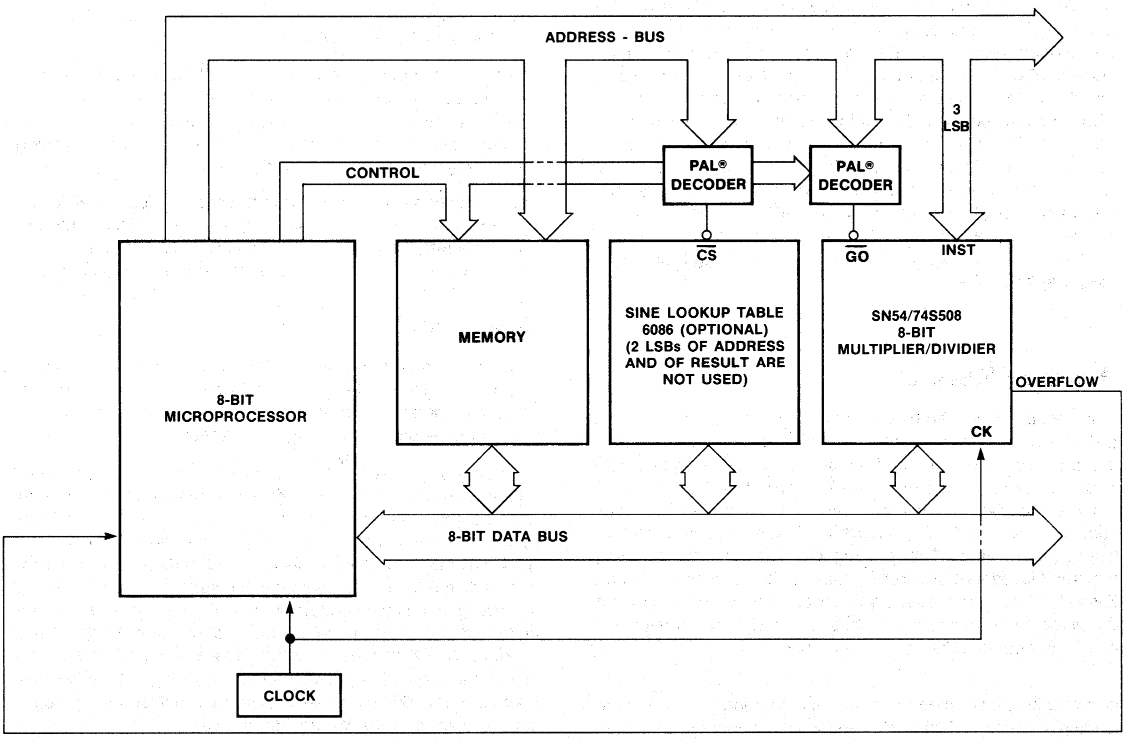


Figure 7. Interfacing the 'S508 to an 8-bit Microprocessor

Figure 7 shows the block diagram of a minimum 8-bit microprocessor system with its arithmetic capabilities enhanced by the use of a 'S508 8x8 multiplier/divider. The relatively small number of instruction lines (only 3) of the 'S508 provides a unique way to control the multiplier/divider. As may be seen from Figure 7, these three instruction lines are assigned to the three least-significant bits (LSBs) of the address bus, while the remaining address bits are decoded by a Programmable Array Logic (PAL®) circuit to determine when the multiplier/divider is selected. For example, suppose the 'S508 is assigned address 100; then any address in the range of 100-107 will enable the 'S508 (i.e., the $\overline{GO}$ line is LOW). Thus, if the address is 100 the 'S508 instruction is 0; if the address is 106 the 'S508 instruction is 6; and so forth.

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125†	0		75	°C
f_{MAX}	Clock frequency	8	5			6			MHz
t_{CWP}	Positive clock pulse width	8	90			70			ns
t_{CWN}	Negative clock pulse width	8	60			50			ns
t_{BS}	Bus setup time for inputting data *	8	60			50			ns
t_{BH}	Bus hold time for inputting data *	8	45			35			ns
t_{INSS}	Instruction, $\overline{GO}$ setup time	8	10			10			ns
t_{INSH}	Instruction, $\overline{GO}$ hold time	8	20			20			ns

* During operations when the bus is being used to input data.
†Case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.5V	B_7-B_0			−250	μA
			All other inputs			−1	mA
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.4V				250	μA
I_I	Maximum input current	V_{CC} = MAX V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN I_{OL} = 8mA			0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN I_{OH} = −2mA		2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = MAX V_O = 0V		−10		−90	mA
I_{CC}	Supply current	V_{CC} = MAX	SN54S508		300	400	mA
			SN74S508		300	380	

* Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

Switching Characteristics
Over Operating Conditions

SYMBOL	PARAMETER		FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{BO}	Bus output delay for outputting data*		8		70	120		70	95	ns
t_{PXZ}	Output disable delay	From I_2-I_0 to bus			40	70		40	65	ns
		From OE, $\overline{GO}$ to bus			20	50		20	40	
t_{PZX}	Output enable delay	From I_2-I_0 to bus			45	90		45	80	ns
		From OE, $\overline{GO}$ to bus			25	55		25	45	
t_{OVR}	Overflow output delay from CK		8		70	120		70	95	ns
t_{DN}	$\overline{DONE}$ output delay		8		30	90		30	70	ns

* During operations when the bus is being used to output data.

10

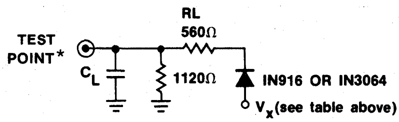
AC Test Conditions

Inputs 0 V_{LOW}, 3 V_{HIGH}. Rise and fall time 1-3 ns from 1 V to 2 V. Measurements are made from 1.5 V_{IN} to 1.5 V_{OUT}, except that t_{PXZ} is measured by a delta in the outputs of 0.5 V from V_{OL} or V_{OH} respectively.

Timing

Timing waveforms are shown in Figure 8. Specific instruction timing examples are shown in Figures 9 through 13.

Test Load

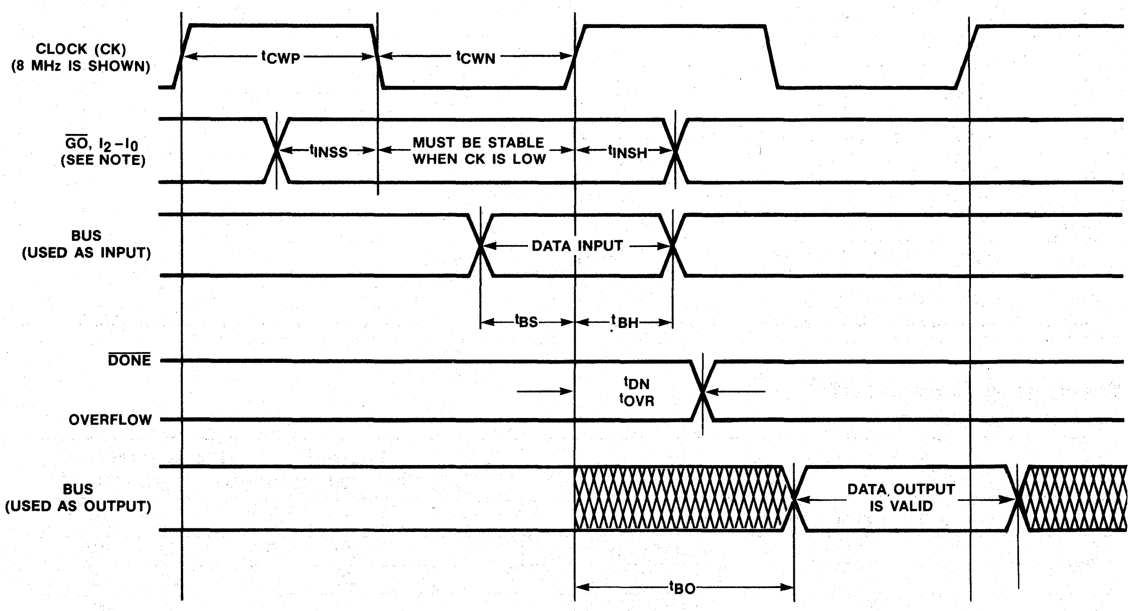


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms

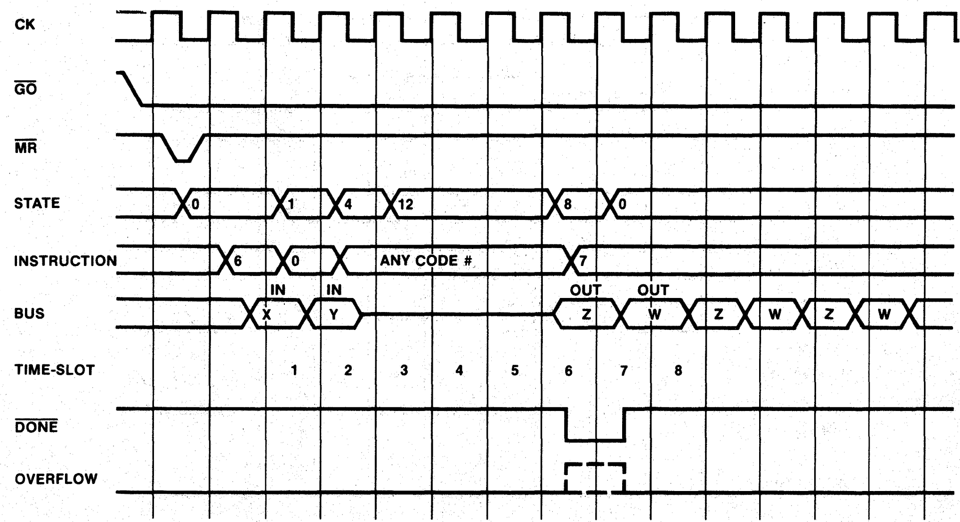
TEST	V_X*		OUTPUT WAVEFORM — MEAS. LEVEL
All t_{PD}	5.0V		V_{OH}, V_{OL}, 1.5V
t_{PXZ}	t_{PHZ}	t_{PLZ}	V_{OH}, V_{OL}, 0.5V, 0.5V, 2.8V, 0.0V
	0.0V	5.0V	
t_{PZX}	t_{PZH}	t_{PZL}	2.8V, 0.0V, 1.5V, V_{OH}, V_{OL}
	0.0V	5.0V	

* At diode: see "Test Load" figure at left.



NOTE: $\overline{GO}$ and I_2-I_0 can change only when CK is high.

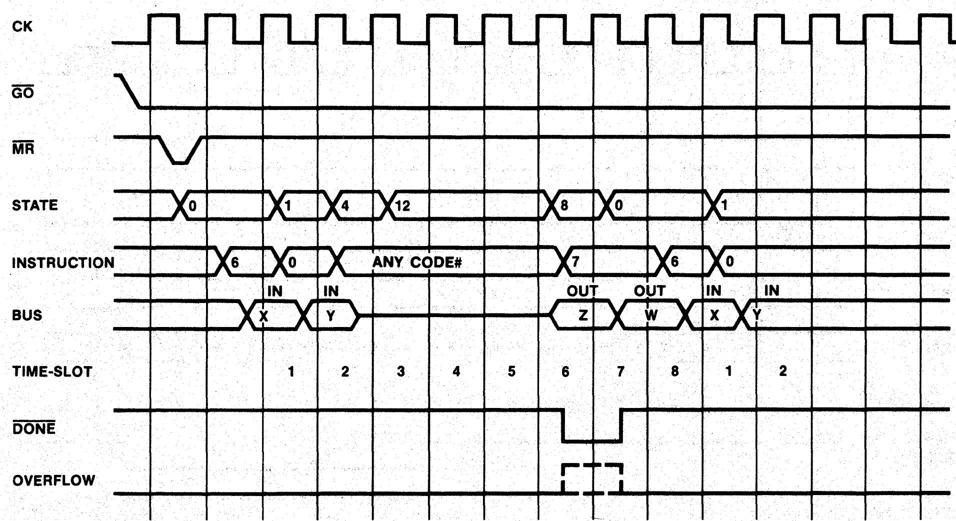
Figure 8. Timing Diagram of the 'S508



NOTES: Register Z is read at the same time that the "$\overline{\text{DONE}}$" signal is set. If the instruction remains at code 7 after time-slot 7, the contents of registers Z and W are swapped each cycle.

"Any code" means code 0 through 7. However code 6 will load a new value of X, and code 7 will cause the 'S508 to attempt to drive the data bus.

Figure 9. Instruction Timing Example No. 1: Load X, Load Y, Multiply, Read W. By Presenting Code 7 on the Instruction Lines During the Last Multiply Cycle (State 8), the Results May Be Read During Time Slots 6 and 7



NOTES: The instruction lines may be changed only when CK is high.

#"Any code" means code 0 through code 7.

Code 6 may be used here since a new X explicitly gets loaded for the next multiply operation. However, code 7 will cause the 'S508 to attempt to drive the data bus.

Figure 10. Instruction Timing Example No. 2: Repeat: "Load X, Load Y, Multiply, Read Z, Read W"

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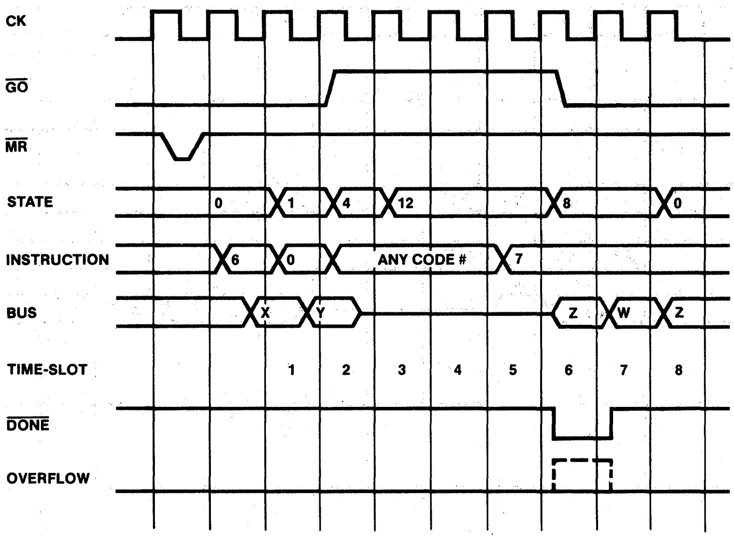
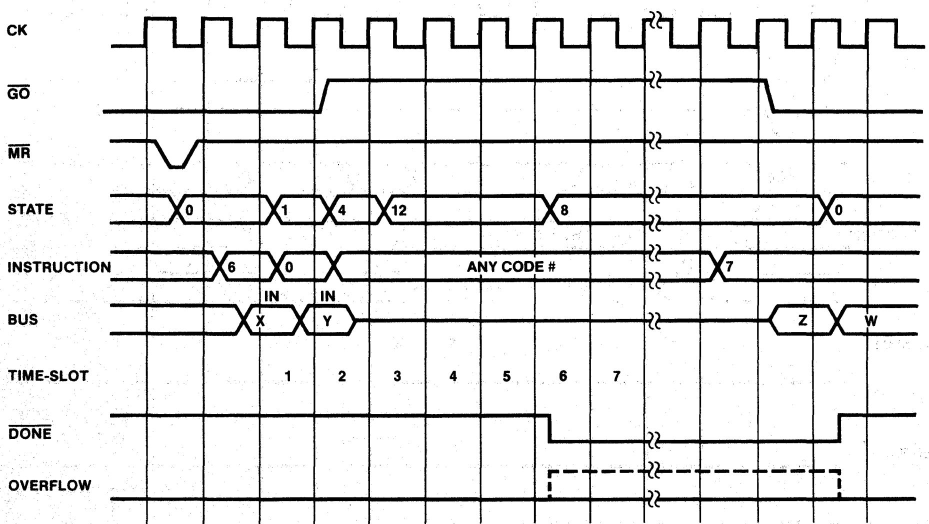


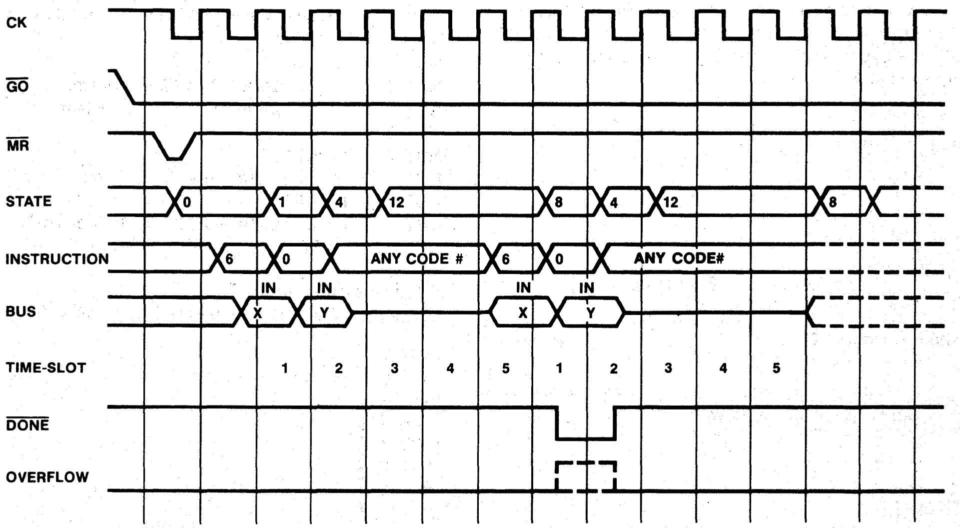
NOTE: If code 7 is given (instead of code 0 through 6), the first data that is read from the bus after the DONE signal is set (time-slot 7) is W and not Z. However, Z is read at time-slot 8.
#"Any code" means code 0 through code 7.

Figure 11. Instruction Timing Example No. 3: Load X, Load Y, Multiply, Read Z, Read W. This timing diagram corresponds to Table 1. Only after the DONE signal is set (after four clock pulses of the operation cycles), the result is read — Z during time-slot 7, and W during time-slot 8



NOTE:
"Any code" means code 0 through code 7. Code 6 or code 7 may be used here. Since GO is HIGH, no new X can be loaded and the 'S508 can not attempt to drive the bus.

Figure 12. Instruction Timing Example No. 4: Load X, Load Y, Multiply, Wait, Read Z, Read W



NOTES: This sequence of operations is suitable for use when reading is to be done only at the very end of the operation sequence. The new X value is loaded during the time that the previous multiplication is being performed. See Programming Example #3 for $\sum_{i=1}^{N} X_i \cdot Y_i$

#"Any code" means code 0 through code 7.
†Code 6 allows loading of a new X value in state 12 and it takes the 'S508 to state 8. In state 8, Y is loaded via instruction 2 and the multiply-accumulate operation is initiated.

Figure 13. Instruction Timing Example No. 5: Sum of Products

Programming Examples

In the following examples assume that each line with a separate instruction corresponds to one clock pulse. Instruction codes are 0, 1, 2, 3, 4, 5, 6, 7 and x according to the usage explained in the key to Figure 2.

Programming Example 1

Calculating X·Y (A·B)

INST 6 X ← A
INST 0 Y ← B
INST X MULT
INST X MULT
INST X MULT
INST 7 MULT and READ Z = 8 MSB OF (A·B)
INST 7 READ W = 8 LSB OF (A·B)

Programming Example 2

Calculating X1 · Y (A · C)

X1 is a previous multiplier value. It was previously loaded (in example 1) with A.

INST 0 Y ← C
INST X MULT
INST X MULT
INST X MULT
INST 7 MULT and READ Z = 8 MSB OF (A·C)
INST 7 READ W = 8 LSB OF (A·C)

Programming Example 3

Calculating $\sum_{i=1}^{N} X_i \cdot Y_i$ (A·B + C·D + E·F + . . .)

In this case we read only after N multiplications. A new X_{i+1} is loaded during the multiplication process for X_iY_i.
Assume N = 3.
The sequence of instructions and operations for calculating $\sum_{i=1}^{3} X_i \cdot Y_i$ is: (A·B + C·D + E·F)

N = 1
INST 6 X ← A
INST 0 Y ← B
INST X MULT
INST X MULT } Perform A·B
INST X MULT

N = 2
INST 6 MULT and LOAD X ← C
Z ← 8 MSB of (A·B)
W ← 8 LSB of (A·B)
INST 2 Y ← D
INST X MULT
INST X MULT } Perform C·D + (K_Z, K_W)
INST X MULT

N = 3
INST 6 MULT and LOAD X ← E
Z ← 8 MSB of (C·D + A·B)
W ← 8 LSB of (C·D + A·B)
INST 2 Y ← F
INST X MULT
INST X MULT } Perform E·F + (K_Z, K_W)
INST X MULT
READ Z INST 7 MULT and
READ Z = 8 MSB of (E·F + C·D + A·B)
READ W INST 7 READ W = 8 LSB of (E·F + C·D + A·B)

Programming Example 4

Multiplication plus a constant (A·B + Constant (16 bits))

Assume that the constant is a 16-bit 2s-complement number.

INST 6 X ← A
INST 6 Z ← C LOAD 8 MSB of constant
INST 6 W ← D LOAD 8 LSB of constant
INST 0 Y ← B
INST X MULT
INST X MULT } Perform A·B + (Z, W)
INST X MULT
INST 7 MULT and READ Z = 8 MSB of (A·B + (C, D))
INST 7 READ W = 8 LSB of (A·B + C, D)

Programming Example 5

Dividing a 16-bit number by an 8-bit number ((B, C)/A)

INST 6 X ← A
INST 6 Z ← B
INST 4 W ← C
INST X
INST X
INST X
INST X
INST X
INST X } Perform Division $\frac{(Z, W)}{X}$
INST X
INST X
INST X
INST X
INST X
INST 7 DIVIDE and READ the quotient Z = $\frac{(B, C)}{A}$
INST 7 READ the remainder W of $\frac{(B, C)}{A}$

16x16 Multiplier/Divider
SN74S516

Features/Benefits

- Co-processor for enhancing the arithmetic speed of all present 16-bit and 8-bit microprocessors
- Bus-oriented organization
- 24-pin package
- 16/16 or 32/16 division in less than 3.5 μsec
- 16x16 multiplication in less than 1.5 μsec
- 28 different multiplication instructions such as "fractional multiply and accumulate"
- 13 different divide instructions
- Self-contained and microprogrammable

Description

The SN74S516 ('S516) is a bus-organized 16x16 Multiplier/ Divider. The device provides both multiplication and division of 2s-complement 16-bit numbers at high speed. There are 28 different multiply options, including: positive and negative multiply, positive and negative accumulation, multiplication by a constant, and both single-length and double-length addition in conjunction with multiplication. 13 different divide options allow single-length or double-length division, division of a previously-generated result, division by a constant, and continued division of a remainder or quotient.

The 'S516 is a time-sequenced device requiring a single clock. It loads operands from, and presents results to, a bidirectional 16-bit bus. Loading of the operands, reading of the results, and sequential control of the device is performed by a 3-bit instruction field.

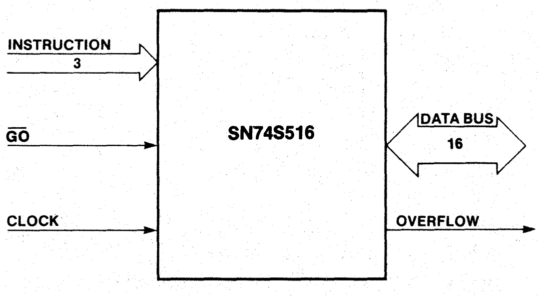
The 'S516 has the additional feature that operands and results can be either integers or fractions; when it deals with fractions, automatic scaling occurs. Results can be rounded if required, and an Overflow output indicates whenever a result is outside the normally-accepted number range.

For a simple multiplication of two operands the device takes nine clock periods — one for initialization, and eight for the actual multiplication. A realistic clock period is 167 ns, which gives a multiplication time of 1333 ns typical for 16x16 multiplication, plus 167 ns additionally for initialization, or 1500 ns in all. More complex multiplications will take additional clock periods for loading the additional operands. A simple division operation requires 16 + 4 = 20 clock periods for a typical time of 3.333 ns (32 bits/16 bits), also plus 167 ns for initialization, or 3500 ns in all.

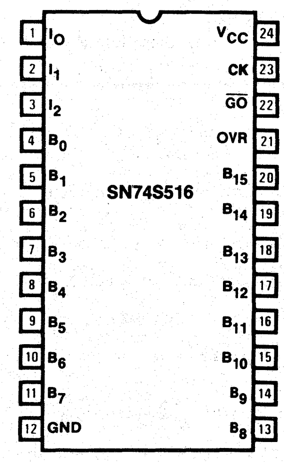
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S516	24T	Commercial

Logic Symbol



Pin Configuration



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Monolithic Memories

INSTRUCTION SEQUENCE				OPERATION	CLOCK CYCLES
ARITHMETIC OPERATIONS					
			0	X1 · Y	9
			1	-X1 · Y	9
			2	X1 · Y + K_z, K_w	9
			3	-X1 · Y + K_z, K_w	9
			4	K_z, K_w/X1	21
		5/6	0	X · Y	10
		5/6	1	-X · Y	10
		5/6	2	X · Y + K_z, K_w	10
		5/6	3	-X · Y + K_z, K_w	10
		5/6	4	K_w/X	22
		5/6	5	K_z/X	22
	5/6	6	0	X · Y + Z	11
	5/6	6	1	-X · Y + Z	11
	5/6	6	2	X · Y + $K_z \cdot 2^{-16}$	11
	5/6	6	3	-X · Y + $K_z \cdot 2^{-16}$	11
	5/6	6	4	Z, W/X	23
	5/6	6	5	Z/X	23
5/6	6	6	0	X · Y + Z, W	12
5/6	6	6	1	-X · Y + Z, W	12
5/6	6	6	2	X · Y + W_{sign}	12
5/6	6	6	3	-X · Y + W_{sign}	12
5/6	6	6	4	W/X	24
5/6	6	6	5	W_{sign}/X	24
5/6	6	6	6	(See Note 9 below.)	—
5/6	6	6	7	Load X, Load Z, Load W, Clear Z	4
	5/6	6	7	Load X, Load Z, Read Z	3
READING OPERATIONS					
			7	Read Z	1
		7	7	Read Z, W	2
	7	7	7	Read Z, W, Z	3
7	7	7	7	Read Z, W, Z, W	4
		5	7	Round, then Read Z	2
	5	7	7	Round, then Read Z, W	3

NOTES:
1. X,Y are input multiplier and multiplicand.
2. X1 is the previous contents of the first rank of the X register (either the old X or a new X).
3. Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.
4. Z, W is a double-precision number. Z is the most significant half. Z, W represents addend upon input, and product (or accumulated sum) after multiplication.
5. K_z, K_w represents previous accumulator contents. K_z is the most-significant half.
6. W_{sign} is a single-length signed number, with sign extension.
7. Maximum clock cycle = 167 ns for an 6-MHz clock.
8. If n instruction codes are shown at the left under "instruction sequences," the number of clock cycles at the right is n+8 for multiplication and n+20 for division.
9. The code "5/6 6 6 6" represents an incomplete operation since it leaves the 'S516 in state 1 rather than in state 0, 8, or 10.

Figure 1. 'S516 Instruction Set (Partial List)

SUMMARY OF SIGNALS/PINS	
B_{15}-B_0	Bidirectional data bus inputs/outputs
I_2-I_0	Instruction (sequential control) input
CK	Clock pulse input
$\overline{GO}$	Chip activation input
OVR	Arithmetic overflow output

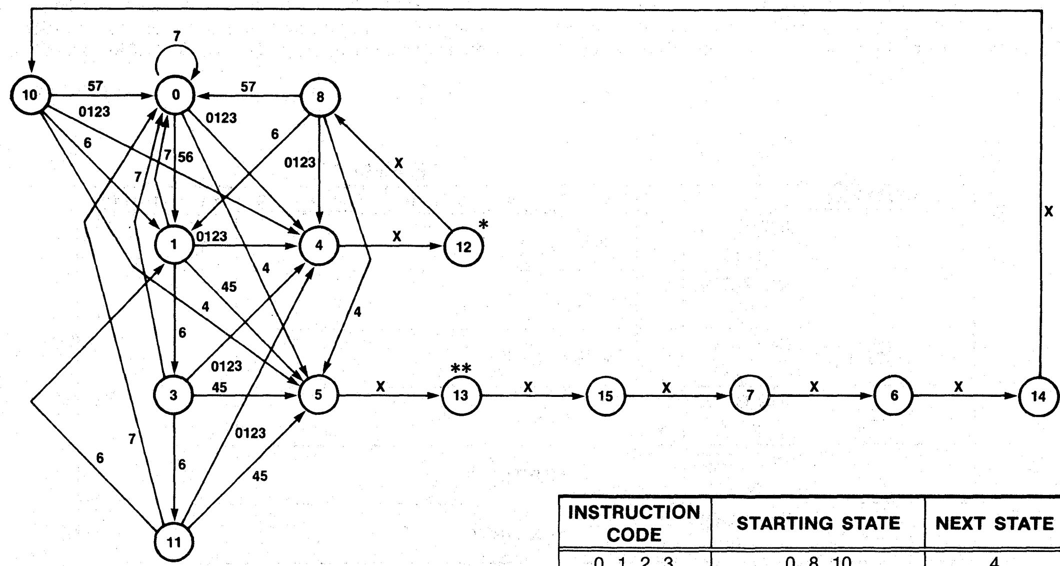
Description (continued)

The 'S516 device uses standard low-power Schottky technology, requires a single +5V power supply, and is fully TTL compatible. Bus inputs require at most 250 μA input current, and control and clock inputs require at most 1 mA input current. Bus outputs are three-state, and are capable of sinking 8 mA at the low logic level. The 'S516 is available in both commercial-temperature and military-temperature ranges, in a 600-mil 24-pin dual-in-line ceramic package.

Device Operation

The 'S516 contains four 16-bit working registers. Y is the multiplier register; X is the multiplicand and divisor register; W is the least-significant half of a double-length accumulator, and holds the least-significant half of the product after a multiplication operation, or the remainder after a division operation; and Z is the most-significant half of this same accumulator. In addition to these registers, there is a high-speed arithmetic unit which performs addition, subtraction, and shifting steps in order to accomplish the various arithmetic operations; a loading sequencer; and a PLA control network.

Operands are loaded into the working registers in time sequence at each clock period, under the control of this sequencer. The chip-activation signal $\overline{GO}$ must be LOW in order to begin the loading process and continue to the next step in the loading operation. If $\overline{GO}$ is continually held HIGH, the 'S516 remains in a wait state with its outputs held in their high-impedance states, so that the other devices attached to the bus may drive it. In this condition, the 'S516 does not respond to any codes on its instruction inputs; in effect, it does not "wake up" until $\overline{GO}$ goes LOW. Also, $\overline{GO}$ may change only when the clock input CK is HIGH. After all of the operands are loaded, the 'S516 jumps to the multiply routine, or to the divide routine, and performs the required operations as indicated in Figure 1. After 9 clock periods for a simple multiply or 21 clock periods for a simple divide, for example, the result is placed on the bus in time sequence.



*Loop 7 times for multiplication.
**Loop 14 times for fractional division, or 15 times for integer division.

INSTRUCTION CODE	STARTING STATE	NEXT STATE
0, 1, 2, 3	0, 8, 10	4
4	0, 8, 10	5
5	0	1
5, 7	8, 10	0
6	0, 8, 10	1
7	0, 8, 10	0

KEY:

The numbers inside the circles indicate the *state* of the 'S516 multiplier/divider. These states are represented by a four-bit state counter, where A is the least-significant bit of this state counter and D is the most-significant bit. (These four bits are not available externally on the 'S516.)

The next state of the 'S516 is a function of the present state and the instruction lines. For example if the 'S516 is at state 0 and the instruction is 0, 1, 2, or 3, then the next state is state 4 (multiply instruction); if the instruction is 4, the next state is state 5 (divide instruction); and so forth. The instructions which take the 'S516 from one state to another are indicated by the numbers written next to the state-transition path lines. "0123," for instance, implies that *any* of instructions 0, 1, 2, or 3 will take the 'S516 along the path marked "0123."

"X" next to a path implies that the path will be followed regardless of the value of the instruction inputs at that time. In other words, for the purpose of state transitions, X means "don't care." There are cases, however, where the particular instruction used may affect when the contents of the registers are available on the bus — see Figures 9 and 10 for contrasting examples of how this effect operates.

Figure 2. Transition Diagram for the 'S516 Multiplier/Divider

Three instruction inputs I_2, I_1, I_0, which may change only when the clock input CK is HIGH, select the required function and drive the sequencer from state to state. Thus, the action of the multiplier/divider at any clock period is a function of the machine state and the state of the control inputs. Figure 2 shows the multiply/divide state table, and all possible operations. After a Read or Round operation, the machine is driven back to state 0, and a new sequence of arithmetic operations is assumed. If a chain operation is being performed, such as accumulation of products, state 0 is bypassed, and loading of an operand or jumping to the next arithmetic operation occurs at the end of the previous arithmetic operation — at state 8 for a multiplication instruction, or at state 10 for a division instruction.

Register X is a dual-rank register, which allows the loading of an operand X during the multiplication or division process. If the machine enters the loading sequence and a new X operand has not been loaded, then the machine proceeds with the previously-loaded X, denoted in this text as "X1." This loading-while-processing capability allows a cycle to be saved during "chained" calculations, and also allows multiplication and division by a constant. (See Figure 13). (continued next page)

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Figures 3 and 4 show the codes and durations for the 41 different possible arithmetic operations. These operations can be concatenated in strings to perform complicated 2s-complement arithmetic operations at high-speed. Rounding and reading of results can be performed after any operation. Figure 5 is a block diagram of the 'S516 16x16 Multiplier/Divider.

(continued page after next)

OPERATION		TIME-SLOT 1	2	3	4	5	6	7	8	9	10	11	12
$X1 \cdot Y$	INS CODE	0	MULTIPLY										
	BUS	Y											
$-X1 \cdot Y$	INS CODE	1	MULTIPLY										
	BUS	Y											
$X1 \cdot Y + K_Z, K_W$	INS CODE	2	MULTIPLY										
	BUS	Y											
$-X1 \cdot Y + K_Z, K_W$	INS CODE	3	MULTIPLY										
	BUS	Y											
$X \cdot Y$	INS CODE	5/6	0	MULTIPLY									
	BUS	X	Y										
$-X \cdot Y$	INS CODE	5/6	1	MULTIPLY									
	BUS	X	Y										
$X \cdot Y + K_Z, K_W$	INS CODE	5/6	2	MULTIPLY									
	BUS	X	Y										
$-X \cdot Y + K_Z, K_W$	INS CODE	5/6	3	MULTIPLY									
	BUS	X	Y										
$X \cdot Y + Z$	INS CODE	5/6	6	0	MULTIPLY								
	BUS	X	Z	Y									
$-X \cdot Y + Z$	INS CODE	5/6	6	1	MULTIPLY								
	BUS	X	Z	Y									
$X \cdot Y + K_Z \cdot 2^{-16}$	INS CODE	5/6	6	2	MULTIPLY								
	BUS	X	—	Y									
$-X \cdot Y + K_Z \cdot 2^{-16}$	INS CODE	5/6	6	3	MULTIPLY								
	BUS	X	—	Y									
$X \cdot Y + Z, W$	INS CODE	5/6	6	6	0	MULTIPLY							
	BUS	X	Z	W	Y								
$-X \cdot Y + Z, W$	INS CODE	5/6	6	6	1	MULTIPLY							
	BUS	X	Z	W	Y								
$X \cdot Y + W_{sign}$	INS CODE	5/6	6	6	2	MULTIPLY							
	BUS	X	—	W	Y								
$-X \cdot Y + W_{sign}$	INS CODE	5/6	6	6	3	MULTIPLY							
	BUS	X	—	W	Y								

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).

2) $K_Z \cdot 2^{-16}$ is a single-length signed number comprising the most-significant half of the previous double-length product and here gets added in at the least-significant end of the new result.

3) W_{sign} is a single-length signed number, with sign-extension as needed.

4) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.

Figure 3. Multiplication Codes and Times for 16x16 Multiplication in the 'S516

<table>
<tr><th colspan="2"></th><th colspan="24">TIME-SLOT</th></tr>
<tr><th>OPERATION</th><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>10</th><th>11</th><th>12</th><th>13</th><th>14</th><th>15</th><th>16</th><th>17</th><th>18</th><th>19</th><th>20</th><th>21</th><th>22</th><th>23</th><th>24</th></tr>
<tr><td rowspan="2">$K_Z, K_W/X_1$</td><td>INS CODE</td><td>4</td><td colspan="19" rowspan="2">DIVIDE</td><td rowspan="2">1</td><td rowspan="2" colspan="3"></td></tr>
<tr><td>BUS</td><td>—</td></tr>
<tr><td rowspan="2">K_W/X</td><td>INS CODE</td><td>5/6</td><td>4</td><td colspan="19" rowspan="2">DIVIDE</td><td rowspan="2">1</td><td rowspan="2" colspan="2"></td></tr>
<tr><td>BUS</td><td>X</td><td>—</td></tr>
<tr><td rowspan="2">K_Z/X</td><td>INS CODE</td><td>5/6</td><td>5</td><td colspan="19" rowspan="2">DIVIDE</td><td rowspan="2">1</td><td rowspan="2" colspan="2"></td></tr>
<tr><td>BUS</td><td>X</td><td>—</td></tr>
<tr><td rowspan="2">Z, W/X</td><td>INS CODE</td><td>5/6</td><td>6</td><td>4</td><td colspan="19" rowspan="2">DIVIDE</td><td rowspan="2">1</td><td rowspan="2"></td></tr>
<tr><td>BUS</td><td>X</td><td>Z</td><td>W</td></tr>
<tr><td rowspan="2">Z/X</td><td>INS CODE</td><td>5/6</td><td>6</td><td>5</td><td colspan="19" rowspan="2">DIVIDE</td><td rowspan="2">1</td><td rowspan="2"></td></tr>
<tr><td>BUS</td><td>X</td><td>Z</td><td>—</td></tr>
<tr><td rowspan="2">W/X</td><td>INS CODE</td><td>5/6</td><td>6</td><td>6</td><td>4</td><td colspan="19" rowspan="2">DIVIDE</td><td rowspan="2">1</td></tr>
<tr><td>BUS</td><td>X</td><td>—</td><td>W</td><td>—</td></tr>
<tr><td rowspan="2">W_{sign}/X</td><td>INS CODE</td><td>5/6</td><td>6</td><td>6</td><td>5</td><td colspan="19" rowspan="2">DIVIDE</td><td rowspan="2">1</td></tr>
<tr><td>BUS</td><td>X</td><td>0</td><td>W</td><td>—</td></tr>
</table>

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).

2) Fractional division divides a 32-bit 2s-complement number in 1 clock period less than integer division.

3) W_{sign} is a single-length signed number, with sign-extension as needed.

4) Division operation W_{sign}/X requires that the Z register be initialized with all-zero contents at the time Z is loaded.

5) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions, one of which does fractional arithmetic and one of which does integer arithmetic.

Figure 4. Division Codes and Times for 32/16 Division in 'S516

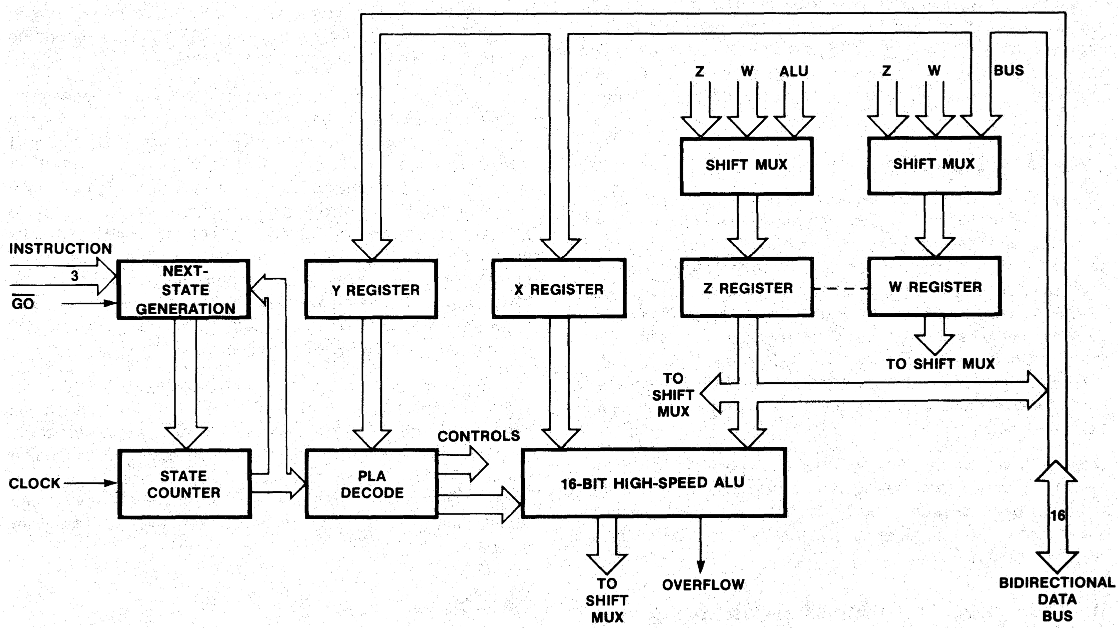

Figure 5. Internal Architecture of the 'S516

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Initialization

The 'S516 has no direct master reset input. However, initialization of the 'S516 can easily be performed by continually presenting instruction code 7, which after a maximum of 21 clock periods forces the machine back to state 0.

Multiplication

The 'S516 provides 2s-complement 16-bit multiplication, and can also accumulate previously-generated double-length products. No time penalty is incurred for accumulation, since the machine accumulates while the multiplication operation is proceeding. In addition to accumulation, the device can add into a product either a single-length or a double-length number. It can also use a previously-loaded operand as a constant, so that constant multiplication and accumulation is possible.

One key feature is the ability to perform both positive multiplications and negative multiplications, again without any speed penalty. This feature allows complex-arithmetic multiplications to be programmed with very little overhead. Another important feature is the ability to work with either fractions or integers.

Division

The 'S516 also provides a range of division operations. A double-length number in Z,W is divided by X; the result Q is stored in Z, and the remainder R in W. Again all numbers are in the 2s-complement number representation, with the most significant bit of an operand (whether single-length or double-length) having a negative weight. In order to facilitate repeated division, with the multiple-length quotient always keeping the same sign, the remainder is always the same sign as the dividend. Fractional or integer operation is possible, and division and multiplication operations can be concatenated. For example, the operations (AxB)/C, (A+B)/C can easily be performed. The dividend can be any previously-generated result — product, quotient, or remainder; or it may be a double-length or single-length signed operand.

Reading Results

The result of an arithmetic operation, or of a string of operations, can be read onto the 16-bit bus if the machine is at the end of an operation or at the start of a new sequence. The read operation requires that the $\overline{GO}$ signal be held LOW so that the information is read out onto the bidirectional bus, when code 7 is specified. (See Figure 6.) Since there is a double-length accumulator Z,W, reading can take two cycles. First, register Z is read. After another clock has been received, if code 7 is still present, the least-significant half of the product from the W register is placed on the bus, or likewise the remainder if a division operation had been performed.

If the 'S516 is instructed to perform a read operation during the loading sequence, then the sequence is broken and the machine is forced back to state 0 ready to start the sequence again. Control read operations at state 0 just swap the contents of register Z and W.

Integer and Fractional Arithmetic

The 'S516 can work with either fractional or integer number representations. When working with integers, all numbers are scaled from the least-significant end, and the least-significant bit is assumed to have a weight of 2^0. For integer multiplication, accumulation, and division, all numbers are scaled from this least-significant weight, and results are correct if interpreted in this manner. The double-length register Z,W can therefore hold numbers in the range -2^{31} to $+2^{31}-1$; the operands X and Y, and single-length results, are in the range -2^{15} to $+2^{15}-1$.

When working with fractions, the machine automatically performs scaling so that input operands and results have a consistent format. All numbers in the fractional representation are scaled from the most significant end, which has a weight of -2^0 *(negative)*. The binary point is one place to the right of this most-significant bit, so that the next bit has a weight of 2^{-1}. The double-length register Z,W therefore holds numbers in the range -1 to $+1-2^{-31}$ and the operands X and Y and single-length results are in the range -1 to $+1-2^{15}$. Since automatic scaling occurs, the product of two numbers always has the least-significant bit as a 0, unless an accumulation is performed with the least-significant bit being a 1.

During a chain operation with the partial results not being read onto the bus, the 'S516 will stay in either the fractional or integer mode. At the start of a sequence of operations, fractional or integer operation is designated by loading operands using instruction code 5 or instruction code 6 respectively.

Mixed fractional and integer arithmetic is also possible, by redefining the weight of the least-significant or most-significant bits. However, care must be exercised, due to the automatic scaling feature, when fractional arithmetic is programmed.

Rounding

Rounding can be performed on the result of a multiplication or division. Generally rounding would only be called out during fractional operation, but nothing in the 'S516 precludes forming a rounded result during integer arithmetic.

Rounding for multiplication provides the best single-length most-significant half of the product. Rounding occurs at the end of a multiplication, and is performed instead of a Load or Read operation when a code 5 is specified, instead of a code 7, to get from state 8 or state 10 back to state 0. (See Figure 2; also, note that this mode of operation precludes "stealing" a cycle according to the method illustrated in Figure 9.) The 'S516 looks at the most-significant bit of the least-significant half of the product W_{15}, and adds 1 to the most-significant half of the product at the least-significant end if W_{15} is a 1. After the operation, the 'S516 is in state 0, so that the rounded product can be read, and the W register is cleared.

Rounding for division is performed by forcing the least-significant bit of the quotient in Z to a 1 unless the division is exact (remainder is zero). This method of rounding causes a slightly higher variance in the result than having an additional iterative division operation, but is considerably easier to perform. Again, after rounding the 'S516 goes to state 0, so that a read operation can be performed, and the W register is cleared.

Overflow

The 'S516 has an overflow output OVR which is cleared prior to each operation, and is set during an operation if the product or quotient goes outside the normally-accepted range.

For multiplication, overflow can only occur if the most negative number in the operand range is used: (-1)x(-1)=+1, which cannot be held in the 'S516's internal registers. Overflow can more easily occur during either positive or negative accumulation of products. For fractional arithmetic, if the product or accumulation goes outside the range of -1 to $+1-2^{-31}$, then the overflow flipflop will be set.

The overflow flip-flop is enabled in state 8 for the multiply operation or in state 10 for a divide operation. It only gets reset when a transition to state 0 from states 0, 3, 8, 10 and 11, when instruction 7 is being presented to the 'S516.

Overflow may also occur during division if the quotient goes outside the generally-accepted number range of -1 to $+1-2^{-15}$ during fractional operation. This would occur if the divisor is less than the dividend, or equal to the dividend if a positive quotient is being generated. For integer arithmetic the numbers must be scaled by 2^{15}.

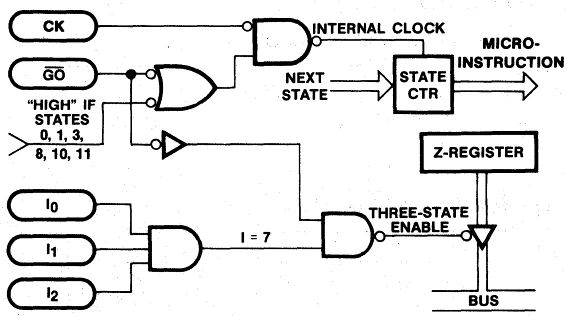


Figure 6. 'S516 Internal Circuitry of "$\overline{GO}$" Line and Three-State-Enable

During the states 0, 1, 3, 8, 10 and 11 if the "GO" line ($\overline{GO}$) is held at logic HIGH then the machine will be in a wait state until $\overline{GO}$ goes to logic LOW.

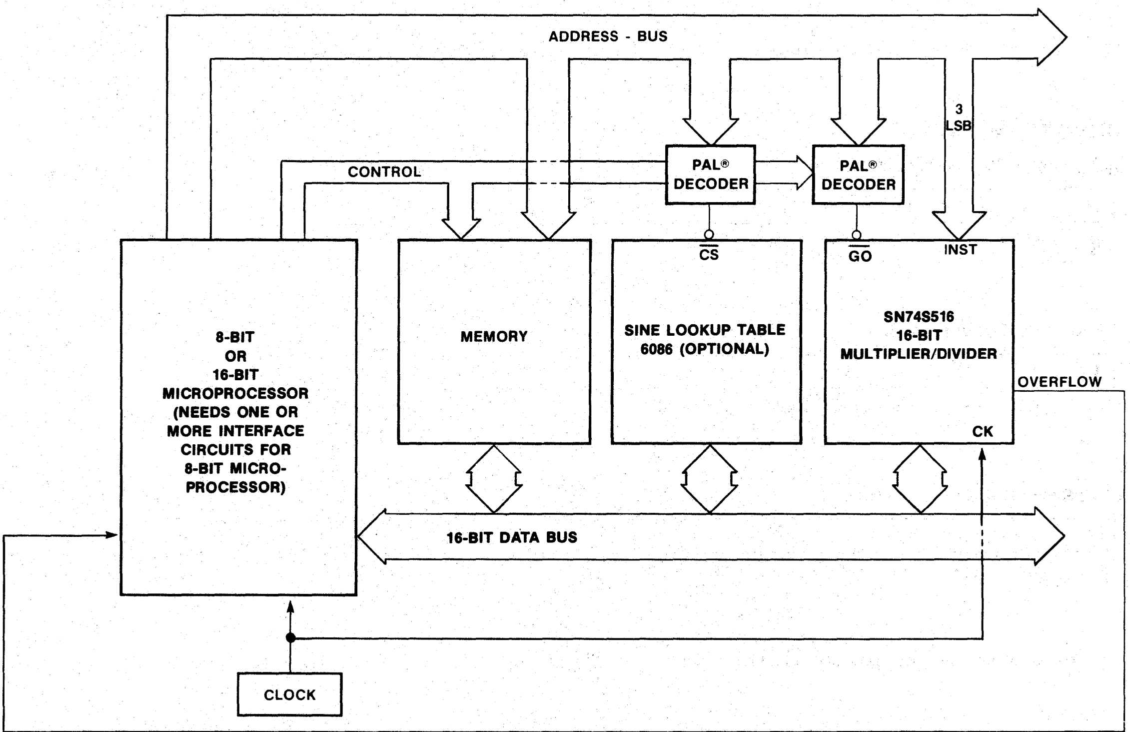


Figure 7. Interfacing the 'S516 to a Microprocessor

Figure 7 shows the block diagram of a microprocessor system with its arithmetic capabilities enhanced by the use of a 'S516 16x16 multiplier/divider. The relatively small number of instruction lines (only 3) of the 'S516 provides a unique way to control the multiplier/divider. As may be seen from Figure 7, these three instruction lines are assigned to the three least-significant bits (LSBs) of the address bus, while the remaining address bits are decoded by a Programmable Array Logic (PAL®) circuit to determine when the multiplier/divider is selected. For example, suppose the 'S516 is assigned address 100; then any address in the range of 100-107 will enable the 'S516 (i.e., the $\overline{GO}$ line is LOW). Thus, if the address is 100 the 'S516 instruction is 0; if the address is 106 the 'S516 instruction is 6; and so forth.

Data Formats

Fractional Multiply

X_i, Y_1 - Input, Multiplicand, Multipler

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Z_i - MS Half Output Product

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

W_i - LS Half Output Product*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	"0"

* The least significant bit of W_i is always a binary 0 due to normalization. Note that -1 x -1 yields an overflow in fractional multiply.

Integer Multiply

X_i, Y_1 - Input, Multiplicand, Multiplier

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Z_i - MS Half Output Product

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

W_i - LS Half Output Product**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

** The least significant bit of W_i is a valid data bit. Note that 2^{-15} x 2^{-15} yields $+2^{30}$ which can be represented in the output bits without overflowing.

Fractional Divide

Z_i - Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

X - Input Divisor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Z_i - Output Quotient

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

W - Output Partial Remainder †

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

† Note that the partial remainder $R = 2^{-15}$ (W)

Integer Divide Example (Z, W)/X

Z_i - MSB Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

W_i - LSB Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

X - Input Divisor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Z_i - Output Quotient

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

W_i - Output Partial Remainder

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETERS	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
f_{MAX}	Clock frequency	8	6			MHz
t_{CWP}	Positive clock pulse width	8	70			ns
t_{CWN}	Negative clock pulse width	8	50			ns
t_{BS}	Bus setup time for inputting data*	8	50			ns
t_{BH}	Bus hold time for inputting data*	8	35			ns
t_{INSS}	Instruction, GO setup time	8	10			ns
t_{INSH}	Instruction, GO hold time	8	30			ns

* During operations when the bus is being used to input data.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.5V	B_{15}-B_0			−250	μA
			All other inputs			−1	mA
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.4V				250	μA
I_I	Maximum input current	V_{CC} = MAX V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN I_{OL} = 8mA			0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN I_{OH} = −2mA		2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = MAX V_O = 0V		−10		−90	mA
I_{CC}	Supply current	V_{CC} = MAX			370	450†	mA

* Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

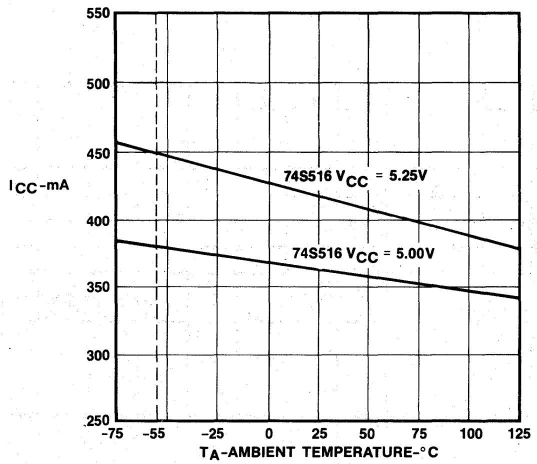
† At cold temperatures see the "I_{CC} vs Temperature" curves on the next page for more complete information. The typical values shown here are at 5.0 V.

Switching Characterictics Over Operating Conditions

SYMBOL	PARAMETER		FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{BO}	Bus output delay from CK for outputting data;* C_L = 30 pF		8		70	95	ns
t_{PXZ}	Output disable delay	FROM I_2-I_0 to bus			30	65	ns
		From GO to bus			20	40	
t_{PZX}	Output enable delay; C_L = 30 pF	FROM I_2-I_0 to bus			55	80	ns
		From GO to bus			25	45	
t_{OVR}	Overflow output delay from CK; C_L = 30 pF		8		60	95	ns

* During operations when the bus is being used to output data.

I_{CC} vs. Temperature

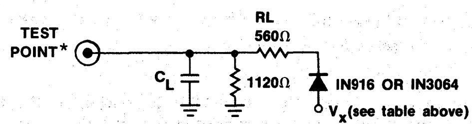


Test Waveforms

TEST	V_X*		OUTPUT WAVEFORM — MEAS. LEVEL
All t_{PD}	5.0V		V_{OH}, V_{OL}, 1.5V
t_{PXZ}	t_{PHZ}	t_{PLZ}	V_{OH}, 0.5V, 0.5V, V_{OL}, 2.8V, 0.0V
	0.0V	5.0V	
t_{PZX}	t_{PZH}	t_{PZL}	2.8V, 0.0V, 1.5V, V_{OH}, V_{OL}
	0.0V	5.0V	

*At diode; see "Test Circuit" figure below.

Test Load



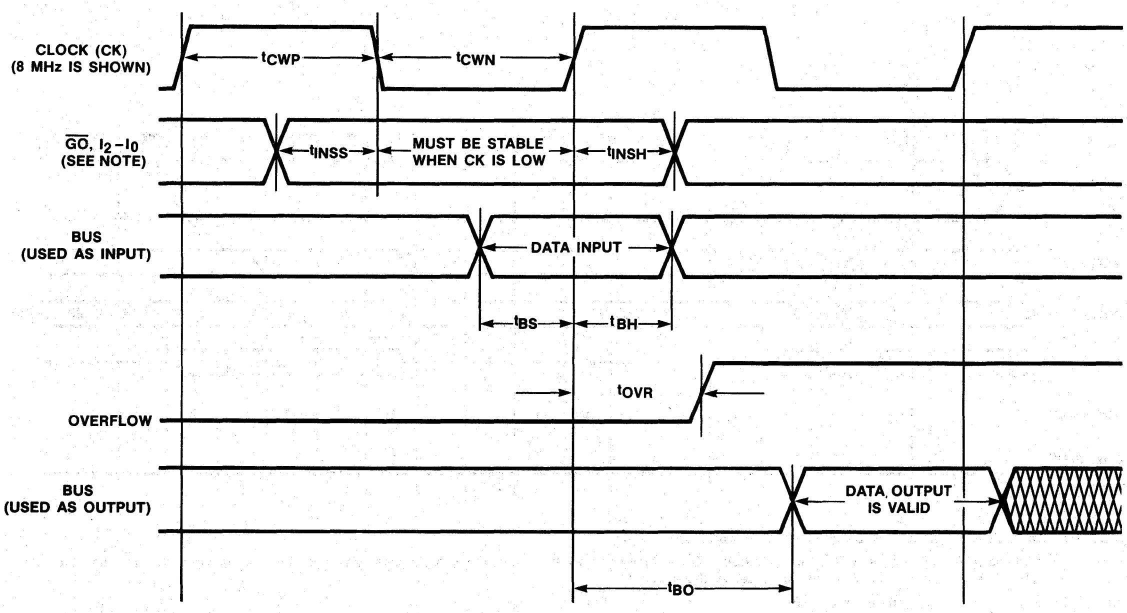
* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

AC Test Conditions

Inputs 0 V_{LOW}, 3 V_{HIGH}. Rise and fall time 1-3 ns from 1 V to 2 V. Measurements are made from 1.5 V_{IN} to 1.5 V_{OUT}, except that t_{PXZ} is measured by a delta in the outputs of 0.5 V from V_{OL} or V_{OH} respectively.

Timing

Timing waveforms are shown in Figure 8. Specific instruction timing examples are shown in Figures 9 through 13.



NOTE: $\overline{GO}$ and I_2-I_0 can change only when CK is high.

Figure 8. Timing Diagram of the 'S516

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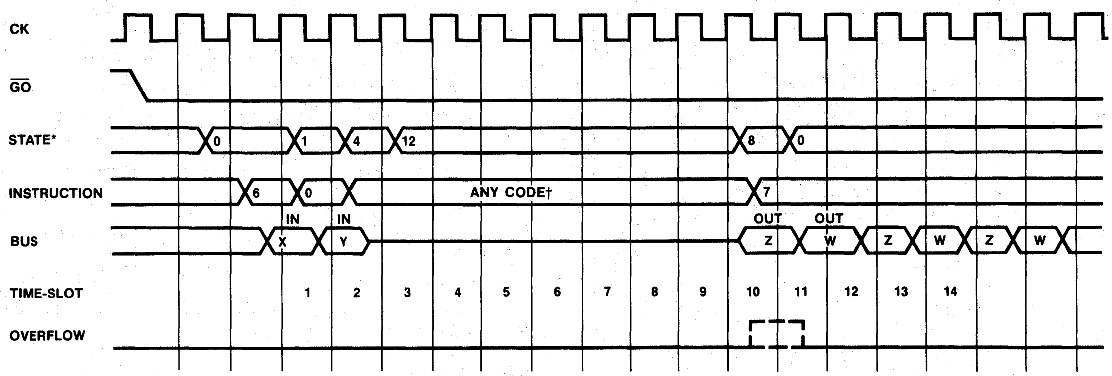
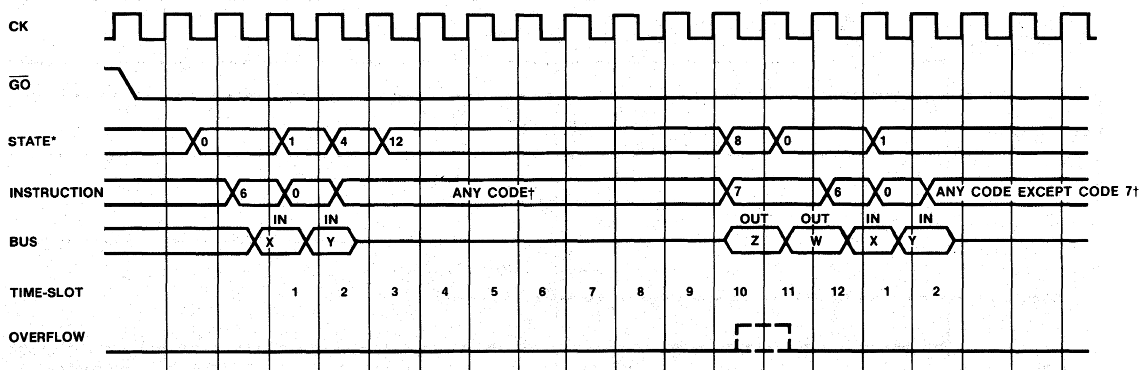


NOTES: Register Z is read at the same time that the overflow signal (if present) is set. If the instruction remains at code 7 after time-slot 11, the contents of registers Z and W are swapped each cycle.

†"Any code" means any of code 0 through code 7. However, code 6 will load a new value of X, and code 7 will cause the 'S516 to attempt to drive the data bus.

*Not available externally on the 'S516.

Figure 9. Instruction Timing Example No. 1: Load X, Load Y, Multiply, Read Z, Read W. By Presenting Code 7 on the Instruction Lines During the Last Multiply Cycle (State 8), the Results May Be Read During Time-Slots 10 and 11

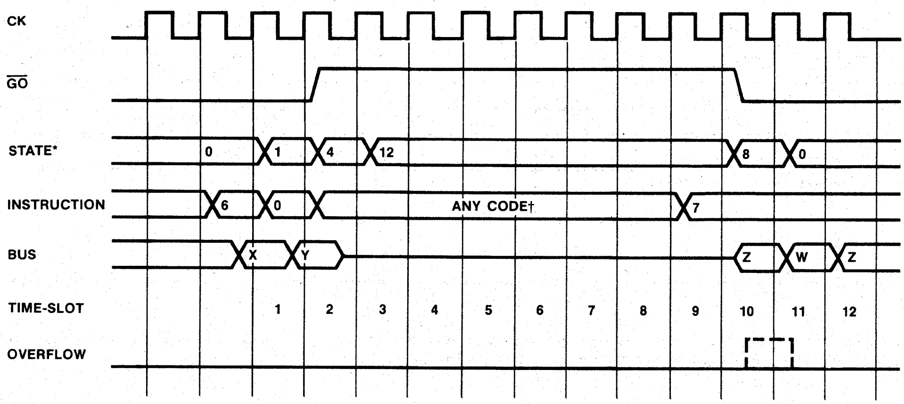


NOTES: The instruction lines may be changed only when CK is high.

†"Any code" means any of code 0 through code 7. Code 6 may be used here since a new X explicitly gets loaded for the next multiply operation. However, code 7 will cause the 'S516 to attempt to drive the data bus.

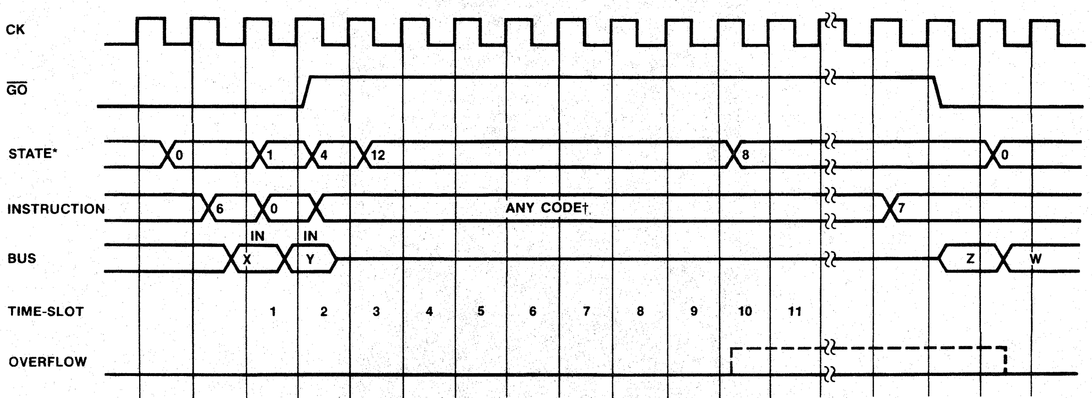
*Not available externally on the 'S516.

Figure 10. Instruction Timing Example No. 2: Repeat: "Load X, Load Y, Multiply, Read Z, Read W"



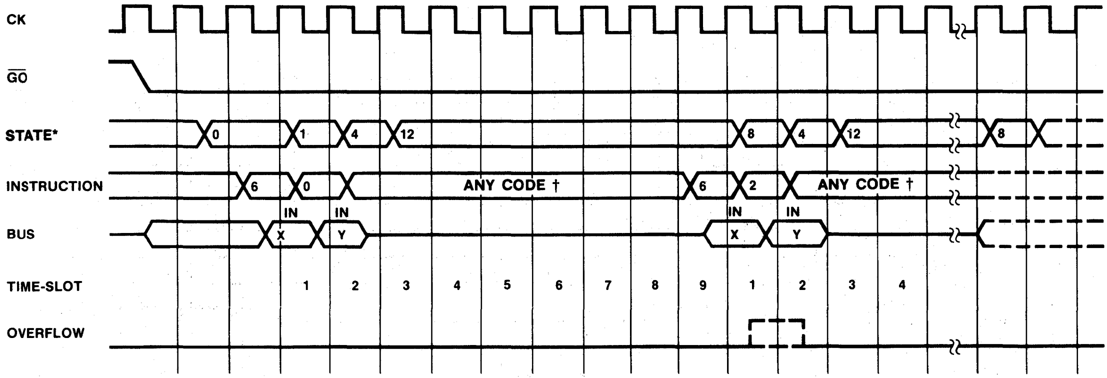
NOTES: Code 7 is given in time-slot 9, but has no effect until time-slot 10 since $\overline{GO}$ is HIGH. After $\overline{GO}$ goes LOW in time-slot 10, Z may be read.
†"Any code" means any of code 0 through code 7.
*Not available externally on the 'S516.

Figure 11. Instruction Timing Example No. 3: Load X, Load Y, Multiply, Read Z, Read W. This Timing Diagram Corresponds to Table 1. Only After Eight Clock Pulses of the Operation Cycle, the Result Is Read — Z During Time-Slot 10 and W During Time-Slot 11



NOTES: †"Any code" means any of code 0 through code 7. Code 6 or code 7 may be used here; since $\overline{GO}$ is HIGH, no new X can be loaded, and the 'S516 cannot attempt to drive the data bus.
*Not available externally on the 'S516.

Figure 12. Instruction Timing Example No. 4: Load X, Load Y, Multiply, Wait, Read Z, Read W



NOTES: This sequence of operations is suitable for use when reading is to be done only at the very end of the operation sequence. The new X value is loaded during the time that the previous multiplication is being performed. See Programming Example #3 for $\sum_{i=1}^{N} X_i \cdot Y_i$

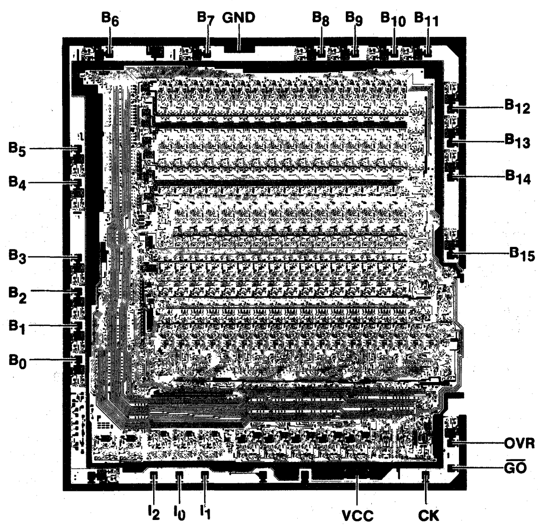
†"Any code" means any of code 0 through code 7. However, code 7 will cause the 'S516 to attempt to drive the data bus.

*Not available externally on the 'S516.

††Code 6 allows loading of a new X in State 12 and it takes the 'S516 State Counter to State 8. In State 8, Y is loaded via instruction 2 and the next multiply-accumulate cycle is initiated.

Figure 13. Instruction Timing Example No. 5: Sum of Products

Die Configuration



Die Size: 210x234 mil^2

Programming Examples

In the following examples assume that each line with a separate instruction corresponds to one clock pulse. Instruction codes are 0, 1, 2, 3, 4, 5, 6, 7 and x according to the usage explained in the key to Figure 2.

Programming Example 1

Calculating X · Y (A·B)

INST 6 X ← A
INST 0 Y ← B
INST X MULT
INST X MULT
INST X MULT
INST X MULT
INST X MULT
INST X MULT
INST X MULT
INST 7 MULT AND READ Z = 16 MSB OF (A·B)
INST 7 READ W = 16 LSB OF (A·B)

Programming Example 2

Calculating X1 · Y (A·C)

X1 is a previous multiplier value. It was previously loaded (in example 1) with A.

INST 0 Y ← C
INST X MULT
INST X MULT
INST X MULT
INST X MULT
INST X MULT
INST X MULT
INST X MULT
INST 7 MULT and READ Z = 16 MSB OF (A·C)
INST 7 READ W = 16 LSB OF (A·C)

Programming Example 3

Calculating $\sum_{i=1}^{N} X_i \cdot Y_i$ (A·B + C·D + E·F + . . .)

In this case we read only after N multiplications. A new X_{i+1} is loaded during the multiplication process for X_iY_i.
Assume N = 3.
The sequence of instructions and operations for calculating $\sum_{i=1}^{3} X_i \cdot Y_i$ is: (A·B + C·D + E·F)

INST 6 X ← A
INST 0 Y ← B
INST X MULT
INST X MULT
INST X MULT
N = 1 INST X MULT Perform A·B
INST X MULT
INST X MULT
INST X MULT
INST 6 MULT and LOAD X ← C
Z ← 16 MSB of (A·B)
W ← 16 LSB of (A·B)
INST 2 Y ← D
INST X MULT
INST X MULT
N = 2 INST X MULT
INST X MULT Perform C·D + (K_Z, K_W)
INST X MULT
INST X MULT
INST X MULT
INST 6 MULT and LOAD X ← E
Z ← 16 MSB of (C·D + A·B)
W ← 16 LSB of (C·D + A·B)
INST 2 Y ← F
INST X MULT
INST X MULT
N = 3 INST X MULT
INST X MULT Perform E·F + (K_Z, K_W)
INST X MULT
INST X MULT
INST X MULT
READ Z INST 7 MULT and
READ Z = 16 MSB of (E·F + C·D + A·B)
READ W INST 7 READ W = 16 LSB of (E·F + C·D + A·B)

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Programming Example 4

Multiplication plus a constant (A·B + Constant)

Assume that the constant is a 32-bit 2s-complement number.

INST 6	X ← A	
INST 6	Z ← C LOAD 16 MSB of constant	
INST 6	W ← D LOAD 16 LSB of constant	
INST 0	Y ← B	
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST X	MULT	Perform A·B + (Z, W)
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST 7	MULT and READ Z = 16 MSB of (A·B + (C, D))	
INST 7	READ W = 16 LSB of (A·B + (C, D))	

Programming Example 5

Dividing a 32-bit number by a 16-bit number ((B, C)/A)

INST 6	X ← A	
INST 6	Z ← B	
INST 4	W ← C	
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		Perform Division $\frac{(Z, W)}{X}$
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST 7	DIVIDE and READ the quotient $Z = \frac{(B, C)}{A}$	
INST 7	READ the remainder W of $\frac{(B, C)}{A}$	

16x16 Flow-Thru™ Multiplier Slice 54/74S556

Features/Benefits

- Twos-complement, unsigned, or mixed operands
- Full 32-bit product immediately available on each cycle
- High-speed 16x16 parallel multiplier
- Latched or transparent inputs/outputs
- Three-state output controls, independent for each half of the product
- Single +5 V supply (via multiple pins)
- Available in 84-terminal Leadless-Chip Carrier and 88-Pin-Grid-Array packages

Description

The 'S556 is a high-speed 16x16 combinatorial multiplier which can multiply two 16-bit unsigned or signed twos-complement numbers on every cycle. Each operand X and Y has an associated mode-control line, XM and YM respectively. When a mode-control line is at a LOW logic level, the operand is treated as an unsigned 16-bit number; when the mode-control line is at a HIGH logic level, the operand is treated as a 16-bit signed twos-complement number. Additional inputs RS and RU allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding. The entire 32-bit double-length product is available at the outputs at one time.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
54S556	P88, L84*	Military
74S556	P88, L84*	Commercial

P88 is an 88-Pin-Grid-Array Package.

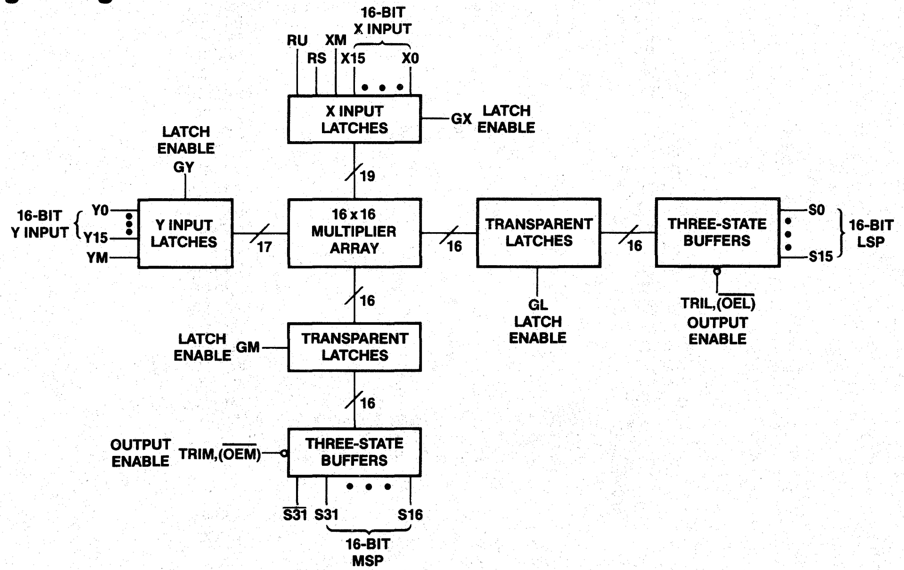
L84 is an 84-terminal Leadless-Chip Carrier Package.

* The 84-terminal leadless chip carrier, L84, and its socket, L84-2, are in development; contact the factory for further details.

The most-significant product bit, S31, is available in both true and complemented form to simplify longer-wordlength multiplications. The product outputs are three-state, controlled by assertive-low enables. The MSP outputs are controlled by the TRIM ($\overline{OEM}$) control input, while the LSP outputs are controlled by the TRIL ($\overline{OEL}$) control input. This allows one or more multipliers to be connected to a parallel bus or to be used in a pipelined system.

All inputs and outputs have transparent latches. The latches become transparent when the input to the corresponding gate control line GX, GY, GM, GL is HIGH. If latches are not required, these control inputs may be tied HIGH, leaving the multiplier fully transparent for combinatorial cascading. The device uses a single +5 V power supply, and is available both in an 84-terminal leadless chip carrier (LCC) package and in an 88-pin-grid-array package.

'S556 Logic Diagram



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Monolithic Memories

SUMMARY OF SIGNALS/PINS	
X_{15-0}	Multiplicand 16-bit data inputs
Y_{15-0}	Multiplier 16-bit data inputs
XM, YM	Mode-control inputs for each data word; LOW for unsigned data and HIGH for twos-complement data
S_{31-0}	Product 32-bit output
$\overline{S}_{31}$	Inverted MS product bit (for expansion)
RS, RU	Rounding inputs for signed and unsigned data, respectively
GX	Gate control for X_i, RS, RU
GY	Gate control for Y_i
GL	Gate control for least-significant half of product
GM	Gate control for most-significant half of product
TRIL $\overline{\text{OEL}}$	Three-state control for least-significant half of product
TRIM $\overline{\text{OEM}}$	Three-state control for most-significant half of products

Rounding Inputs

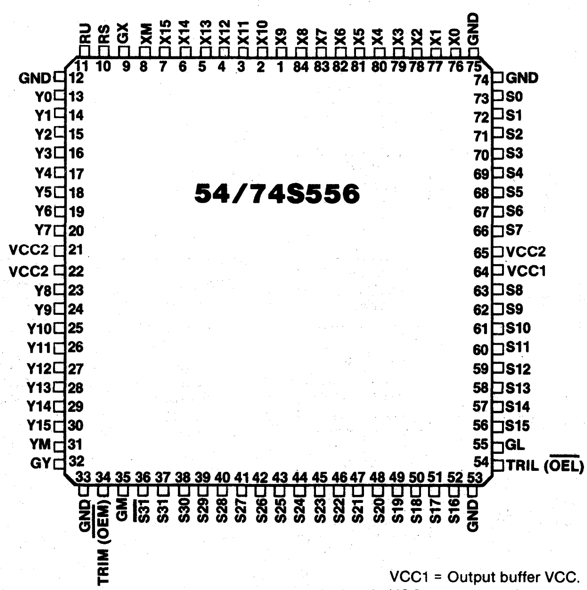
INPUTS		ADDS		USUALLY USED WITH	
RU	RS	2^{15}	2^{14}	XM	YM
L	L	NO	NO	X	X
L	H	NO	YES	H†	H†
H	L	YES	NO	L	L
H	H	YES	YES	*	*

† In mixed mode, one of these could be low but not both.
* Usually a nonsense operation.

Mode-Control Inputs

OPERATING MODE	INPUT DATA		MODE-CONTROL INPUTS	
	X_{15-0}	Y_{15-0}	XM	YM
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos-Comp.	L	H
	Twos-Comp.	Unsigned	H	L
Signed	Twos-Comp.	Twos-Comp.	H	H

84-Terminal Leadless Chip Carrier Pinout



VCC1 = Output buffer VCC.
VCC2 = Logic VCC.

All V_{CC} and GND pins must be connected to the respective V_{CC} and GND connections on the board and should not be used for daisychaining through the IC.

Operating Conditions

SYMBOL	PARAMETER		FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature			-55		*125	0		75	°C
t_{S1}	Setup time $(X_i, R_i)/Y_i$ to GX/GY		2a, 2b	12			10			ns
t_{S2}	Setup time X_i, Y_i, R_i to GM, GL	t_{S2L}	3a, 3b	65			60			ns
		t_{S2M}		82			74			
t_{S3}	Setup time GX, GY to GL, GM	t_{S3L}	4a, 4b, 4c, 4d, 4e, 4f	65			60			ns
		t_{S3M}		85			75			
t_{H1}	Hold time $(X_i, R_i)/Y_i$ to GX/GY		2a, 2b	8			8			ns
t_{H2}	Hold time X_i, Y_i, R_i to GM, GL	t_{H2L}, t_{H2M}	3a, 3b	3			3			ns
t_{H3}	Hold time GX, GY to GM, GL	t_{H3L}, t_{H3M}	4a, 4b, 4c, 4d, 4e, 4f	0			0			ns
t_W	Latch enable pulse width		6	14			12			ns

* Indicates case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage**					0.8	V
V_{IH}	High-level input voltage**			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			75	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5 V			-100	μA
I_{OZH}			V_O = 2.4 V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX	Commercial 74S556		600	800	mA
			Military 54S556		600	900	mA
I_{CC}	Supply current at hot temperature limit	V_{CC} = 5.25 V	T_A = 75°C			700	mA
		V_{CC} = 5.5 V	T_C = 125°C			800	mA

† Typical at 5.0 V and 25°C T_A.
* Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
** These are absolute voltages with respect to the ground pins and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	54S556 MILITARY			74S556 COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{DTL}	Transparent Multiply GX, GY, GM, GL = H	X_i, Y_i, R_i to S_{15-0} Figs. 1, 2c, 3b, 4c, 4f	CL = 30 pF RL = 560Ω See figure 7			84		50	76	ns
t_{DTM}		X_i, Y_i, R_i to $S_{31}, \overline{S}_{31-16}$ Figs. 1, 2c, 3b, 4c, 4f				100		60	90	ns
t_{D1L}	Transparent Output Multiply GM, GL = H	GX, GY to S_{15-0} Figs. 2a, 2b, 4d, 4e				88			80	ns
t_{D1M}		GX, GY, to $S_{31}, \overline{S}_{31-16}$ Figs. 2a, 2b, 4d, 4e				102			92	ns
t_{D2}	Transparent Input Multiply GX, GY = H	GM, GL to S_i Figs. 3a, 4a, 4b				40			35	ns
t_{PXZ}	Three-State Disable Timing	TRIL ($\overline{OEL}$), TRIM ($\overline{OEM}$) to S_i Fig. 5				40			30	ns
t_{PZX}	Three-State Enable Timing	TRIL ($\overline{OEL}$), TRIM ($\overline{OEM}$) to S_i Fig. 5				40			30	ns

Transparent Multiply — Flowthrough Operation

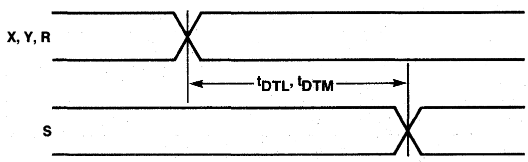
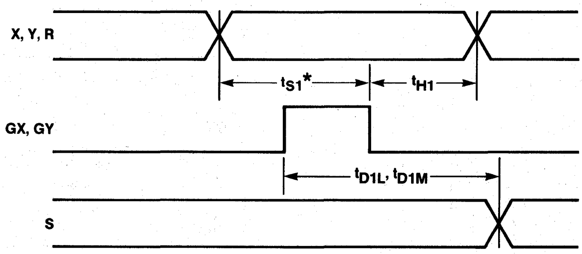


Figure 1.

The transparent multiply is a flowthrough operation of the 'S556. Both the input and output latches are made transparent by keeping GX, GY, GM, and GL at a HIGH level. The operands are presented to the X, Y, and R inputs; the results are available t_{DTL} and t_{DTM} later, for the least and most significant halves of the product respectively.

Transparent Output Multiply — Pipelined Input



* With this particular timing, set-up time t_{S1} will automatically be met.

Figure 2a.

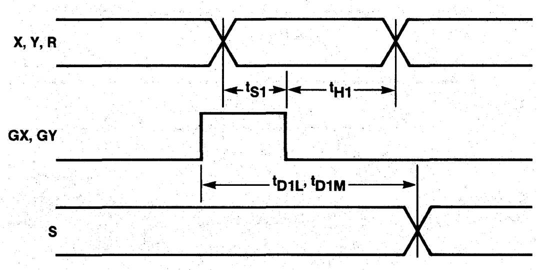


Figure 2b.

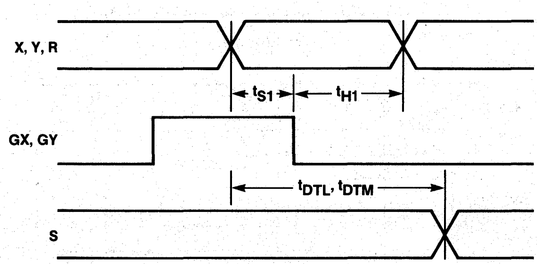


Figure 2c.

By tying the GL and GM lines HIGH, the 'S556 can perform transparent output (or pipelined input) multiplies. Data present is latched at the inputs using the GX and GY control signals. The time at which the result S is present at the outputs depends on when the rising edges of GX and GY occur. If the rising edges of GX and GY occur *after* the operand inputs change, then Figure 2a applies; the result will be available at the outputs t_{D1L} and t_{D1M}* after the rising edges of GX and GY. If the rising edges of GX and GY occur *less than* $(t_{W\,min} - t_{S1\,min})$ *before* the operand inputs change, then Figure 2b applies; in this case the result will also be available at the outputs t_{D1L} and t_{D1M}* after the rising edges of GX and GY. However, if the rising edges of GX and GY occur *more than* $(t_{W\,min} - t_{S1\,min})$ *before* the operand inputs change, then Figure 2c applies; the result will appear at the outputs t_{DTL} and t_{DTM}* after the operand inputs change.

* For the least and most significant halves of the product, respectively.

Transparent Input Multiply — Pipelined Output

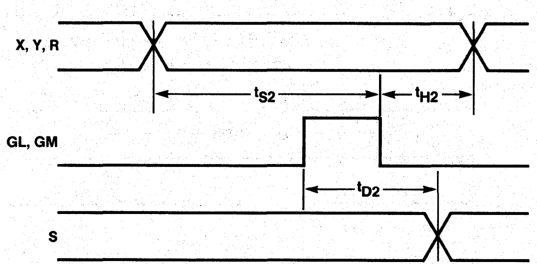


Figure 3a.

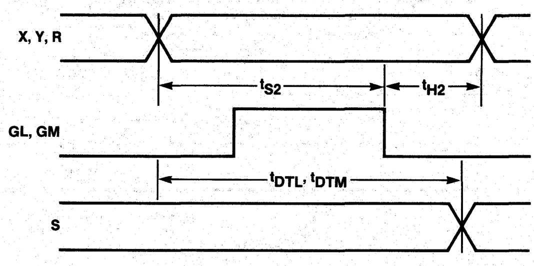


Figure 3b.

By tying the GX and GY lines HIGH, the 'S556 can perform transparent input (or pipelined output) multiplies. Data is presented at the inputs, and t_{S2} after X, Y and R change, the results can be latched. The time at which the result S is present at the outputs depends upon when the rising edges of GL and GM occur. If they occur *at or after* $(t_{S2\,min} - t_{W\,min})$ from the inputs changing, then Figure 3a applies; the result appears at the outputs t_{D2} after the rising edges of GL and GM. If the rising edges of GL and GM occur *before* $(t_{S2\,min} - t_{W\,min})$ from the inputs changing, then Figure 3b applies; the result appears at the outputs t_{DTL} and t_{DTM}* after the operand inputs change.

* For the least and most significant halves of the product, respectively.

Gated Multiply — Pipelined Input and Output

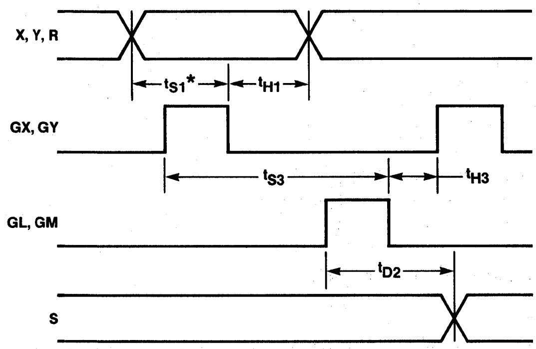


Figure 4a.

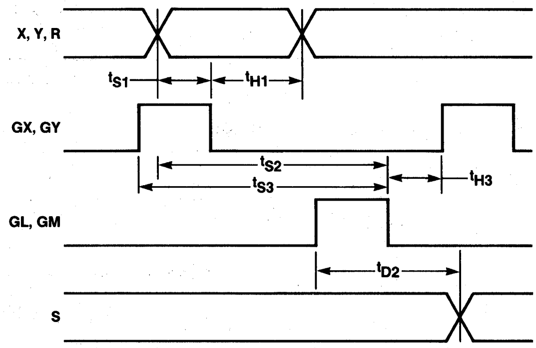


Figure 4b.

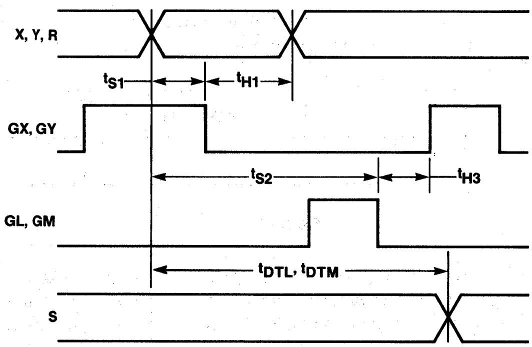


Figure 4c.

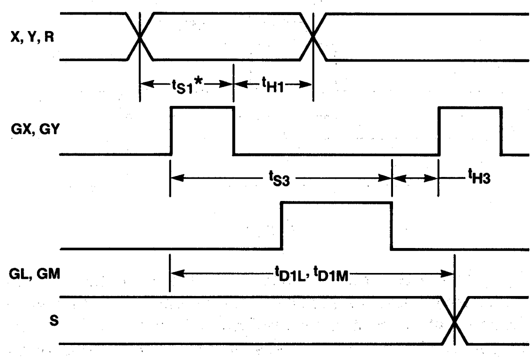
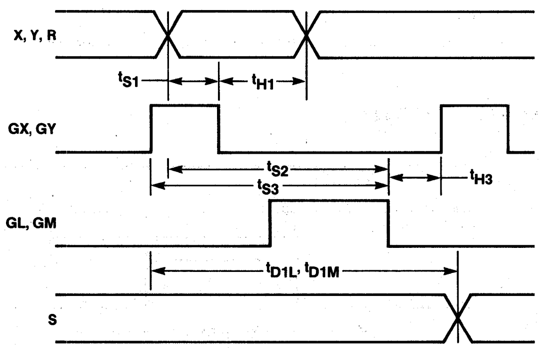
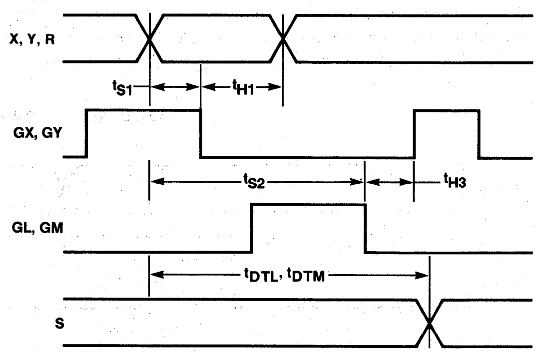


Figure 4d.





* With this particular timing setup time t_{S1} will be automatically met.

Figure 4e.

Figure 4f.

The gated multiply represents the pipelined input and output operation. The latch enable lines GX, GY, GL, GM are used to store incoming operands and outgoing results. The particular set-up times that must be met and the time the result takes to reach the outputs depends on two timing relationships. The first is when the rising edges of GX and GY occur with respect to the operand inputs changing, and the second is when the rising edges of GL and GM occur with respect to the rising edges of GX and GY. On the above timing diagrams, denote the absolute time that the operand inputs change as T_{XYR}, the absolute time that the rising edges of GX and GY occur as T_{GXY}, and the absolute time that the rising edges of GL and GM occur as T_{GLM}. Thus, the two delays of concern can be explicitly stated as (T_{GXY} - T_{XYR}) and (T_{GLM} - T_{GXY}). Notice that either of these quantities can be positive or negative depending on which event occurs first. Timing for gated multiplies can then be summarized in the following table:

$T_{GXY} - T_{XYR}$	$T_{GLM} - T_{GXY}$	FIGURE	WHICH SET-UP TIMES MUST BE MET	WHEN RESULT IS PRESENT AT OUTPUTS
$T_{GXY} - T_{XYR} \geq 0$	$T_{GLM}-T_{GXY} \geq t_{S3min}-t_{Wmin}$	4a	t_{S3}	$T_{GLM} + t_{D2}$
$0<T_{XYR}-T_{GXY} \leq t_{Wmin}-t_{S1min}$	$T_{GLM}-T_{GXY} \geq t_{S3min}-t_{Wmin}$	4b	t_{S1}, t_{S2}, t_{S3}	$T_{GLM} + t_{D2}$
$t_{Wmin} - t_{S1min} < T_{XYR} - T_{GXY}$	$T_{GLM}-T_{GXY} \geq t_{S3min}-t_{Wmin}$	4c	t_{S1}, t_{S2}	$T_{XYR} + (t_{DTL}, t_{DTM})^*$
$T_{GXY} - T_{XYR} \geq 0$	$T_{GLM}-T_{GXY} < t_{S3min}-t_{Wmin}$	4d	t_{S3}	$T_{GXY} + (t_{D1L}, t_{D1M})^*$
$0<T_{XYR}-T_{GXY} \leq t_{Wmin}-t_{S1min}$	$T_{GLM}-T_{GXY} < t_{S3min}-t_{Wmin}$	4e	t_{S1}, t_{S2}, t_{S3}	$T_{GXY} + (t_{D1L}, t_{D1M})^*$
$t_{Wmin} - t_{S1min} < T_{XYR} - T_{GXY}$	$T_{GLM}-T_{GXY} < t_{S3min}-t_{Wmin}$	4f	t_{S1}, t_{S2}	$T_{XYR} + (t_{DTL}, t_{DTM})^*$

* For the least and most significant halves of the product respectively.

NOTE: T_{XYR} represents the absolute time when the operand inputs change.
T_{GXY} and T_{GLM} represent the absolute times when the rising edges of the latch controls occur.

Three State Timing

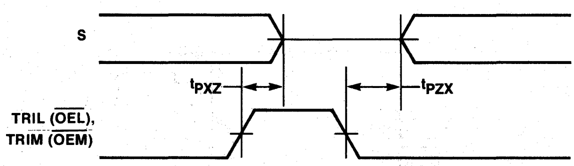


Figure 5.

Test Waveforms

TEST		V_X	OUTPUT WAVEFORM — MEAS. LEVEL
All t_{PD}		5.0V	V_{OH}, V_{OL}, 1.5V
t_{PXZ}	t_{PHZ}	0	V_{OH}, 0.5V, 0.5V, V_{OL}, 2.8V, 0.0V
	t_{PLZ}	5	
t_{PZX}	t_{PZH}	0	2.8V, 0.0V, 1.5V, V_{OH}, V_{OL}
	t_{PZL}	5	

Latch Enable Pulse Width (GL, GM, GX, GY)

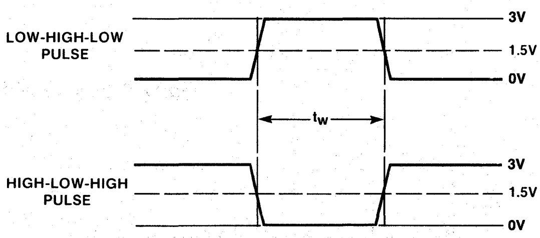


Figure 6.

Load Test Circuit

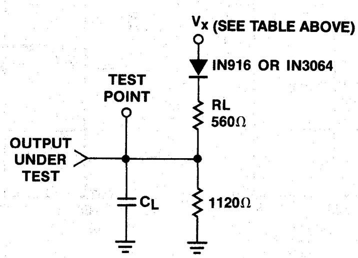


Figure 7.

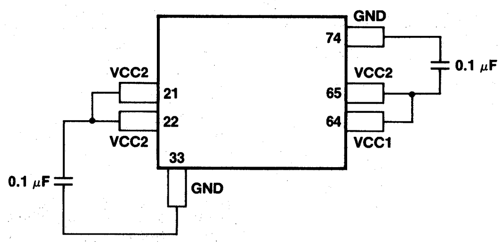
Recommended Bypass Capacitors

The switching currents when the outputs change can be fairly high, and bypass capacitors are recommended to adequately decouple the VCC and GND connections.

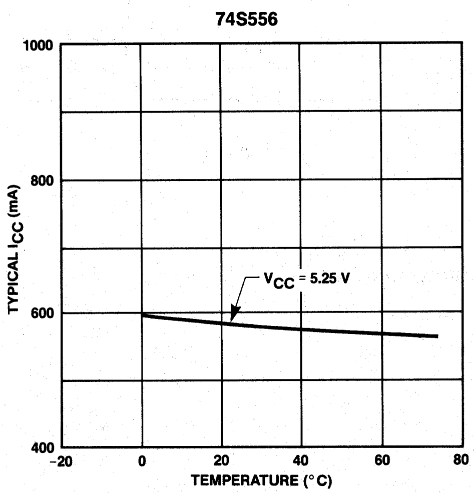
For example, on the 84-terminal LCC package, pins 21 and 22 are VCC2 supplies and should be decoupled with pin 33, a GND input, using a 0.1 μf monolithic ceramic disk capacitor. The capacitor must have good high-frequency characteristics. Also pins 64 and 65, VCC1 and VCC2, should be decoupled with pin 74, a GND input, with a similar capacitor arrangement.

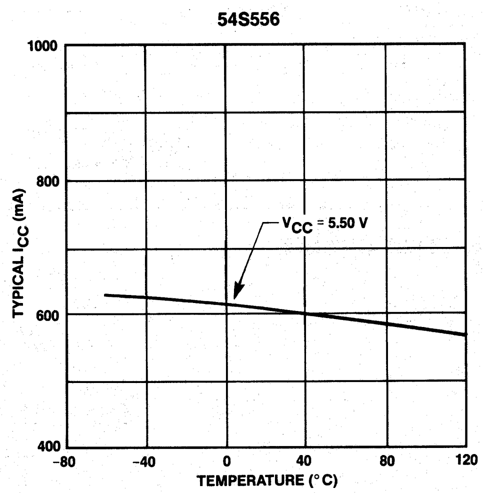
For the 88-pin-grid-array package pins 21 and 22 are VCC2 supplies and should be decoupled with pin 35, the GND pin. Pins 66 and 67, VCC1 and VCC2, should be decoupled with pin 77, the GND pin.

Decoupling Capacitors Shown with the 84-Terminal LCC Package



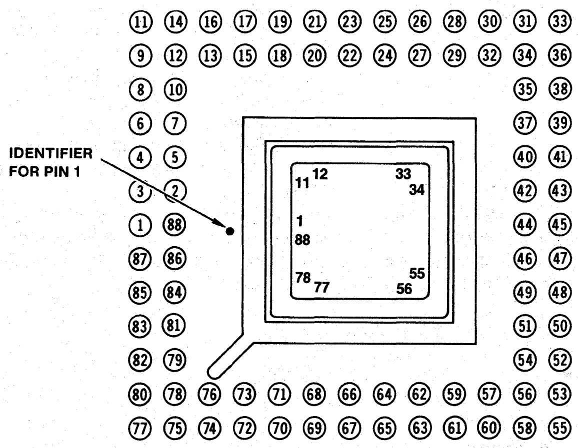
Typical Supply Current Over Temperature Range





88 Pin-Grid-Array

Pin Locations
Bottom View



Pin-Guide For Pin Grid Array

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	X9	23	N/C*	45	S25	67	VCC2†
2	X10	24	Y8	46	S24	68	N/C*
3	X11	25	Y9	47	S23	69	S7
4	X12	26	Y10	48	S22	70	S6
5	X13	27	Y11	49	S21	71	S5
6	X14	28	Y12	50	S20	72	S4
7	X15	29	Y13	51	S19	73	S3
8	XM	30	Y14	52	S18	74	S2
9	GX	31	Y15	53	S17	75	S1
10	RS	32	YM	54	S16	76	S0
11	RU	33	GY	55	GND	77	GND
12	GND	34	N/C*	56	TRIL ($\overline{\text{OEL}}$)	78	N/C*
13	Y0	35	GND	57	GL	79	GND
14	Y1	36	TRIM ($\overline{\text{OEM}}$)	58	S15	80	X0
15	Y2	37	GM	59	S14	81	X1
16	Y3	38	$\overline{\text{S31}}$	60	S13	82	X2
17	Y4	39	S31	61	S12	83	X3
18	Y5	40	S30	62	S11	84	X4
19	Y6	41	S29	63	S10	85	X5
20	Y7	42	S28	64	S9	86	X6
21	VCC2†	43	S27	65	S8	87	X7
22	VCC2†	44	S26	66	VCC1††	88	X8

* Not connected. † VCC2 = Logic VCC. †† VCC1 = Output buffer VCC.

Rounding

Multiplication of two n-bit operands results in a 2n-bit product†. Therefore, in a pure n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples illustrate the difference between the two conversion techniques in decimal arithmetic:

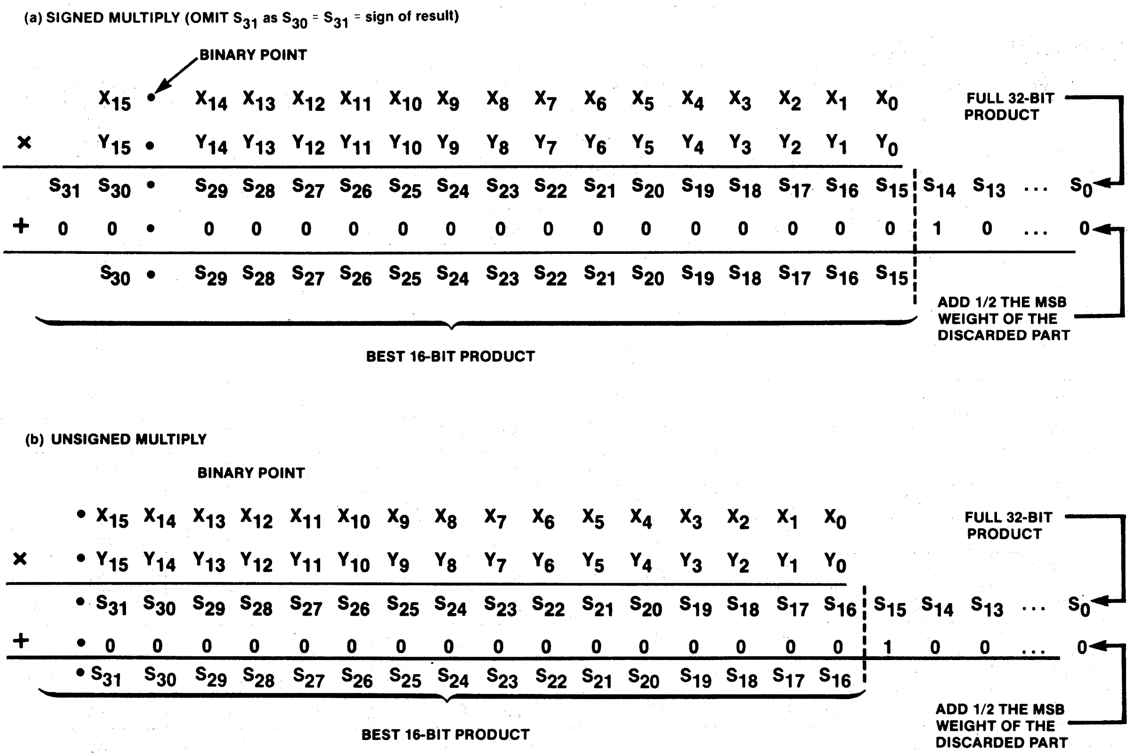
39.2 → 39 39.6 → 39	Truncating
39.2 + 0.5 = 39.7 → 39 39.6 + 0.5 = 40.1 → 40	Rounding

Obviously, rounding maintains more precision than truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single-length LSB to the MSB of the discarded part; e.g., in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding 0.05 to the number and truncating the LSB:

39.28 + 0.05 = 39.33 → 39.3

The situation in binary arithmetic is quite similar, but two cases need to be considered; signed and unsigned data representation. In signed multiplication, the two MSBs of the result are identical, except when both operands are −1; therefore, the best single-length product is shifted one position to the right with respect to the unsigned multiplications. Figure 8 illustrates these two cases for the 16x16 multiplier. In the signed case, adding one-half of the S_{15} weight is accomplished by adding 1 in bit position 14, and in the unsigned case by adding 1 in bit position 15. Therefore, the 'S556 multiplier has two rounding inputs. RS and RU. Thus, to get a rounded single-length result, the appropriate R input is tied to V_{CC} (logic High) and the other R input is grounded. If a double-length result is desired, both R inputs are grounded.

†In general multiplication of an M-bit operand by an N-bit operand results in an (M + N)-bit product.



NOTES:

(a) In signed (twos-complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best 16-bit product is from S_{30} through S_{15}, and rounding is performed by adding "1" to bit position S_{14}.

(b) In unsigned notation the best 16-bit product is the most significant half of the product and is corrected by adding "1" to bit position S_{15}.

Figure 8. Rounding the Result of Binary Fractional Multiplication.

Using the 'S556 in a Pipelined Positive-Edge Triggered Clock System

The 'S556 has internal latches which can be used affectively in systems where things happen on positive-going clock edges. This application is an extension of the gated multiply mode shown in Figure 1, in which a 32-bit product can be latched every t_{S3} nsec in the 'S556.

If the signals GX, GY, GM and GL can be derived from the system clock then the latches can almost have the same effect as having a register. The basic philosophy behind the recommended timing is that the input latches are closed when the output latches are open; the outputs are then closed (and have latched results) and new data is presented to the input latches, which are opened. This is shown by the relation between GX, GY and GL, GM in Figure 9. The set-up time t_{S3} is shown as one value but strictly speaking, it is split as t_{S3L} and t_{S3M} for the least significant and most significant half of the product respectively. The value of t_{S3L} is less than t_{S3M}, for applications requiring the least significant bits of the result as fast as possible.

One note of caution is that a design must always meet the set-up and hold times for X_i, R_i with respect to GX and for Y_i with respect to GY.

The result S_i is available t_{D2} after the rising edge of GM and GL.

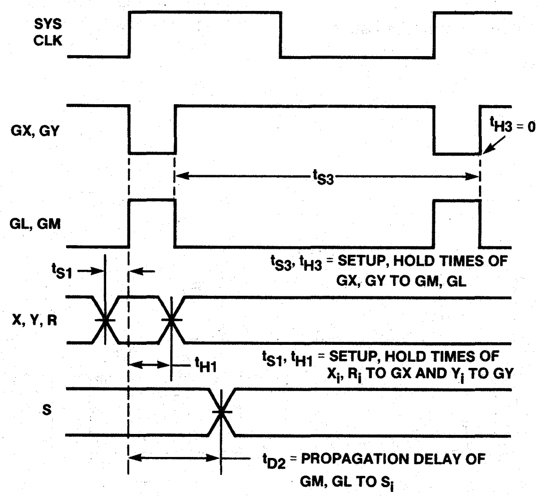


Figure 9.

Totally Parallel 32x32 Multiplier

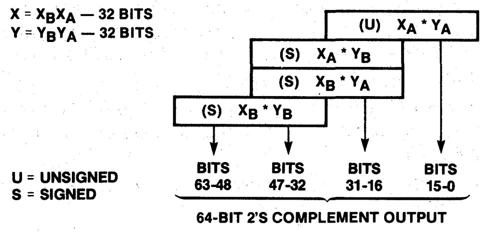
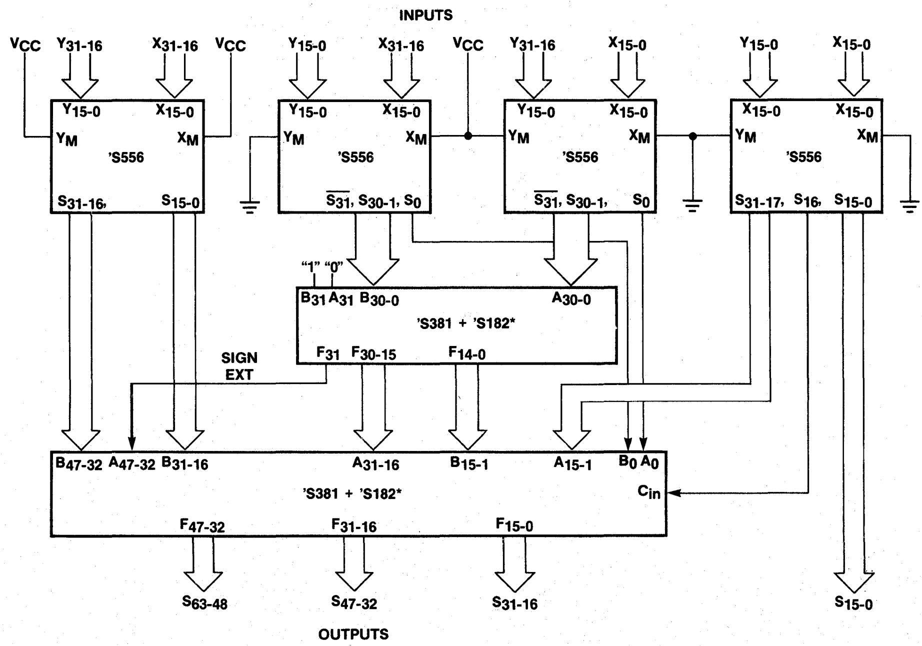


Figure 10. Partial Products for a 32x32 Multiplication

A twos-complement 32x32 multiplication can be performed within 220 nsec using 4 'S556s, 20 'S381s, and 7 'S182s. This 32x32 multiply operation involves adding up four partial products as shown in Figure 10. These four partial products are generated in four multipliers; the outputs are XA*YA, XA*YB, XB*YA, XB*YB, where X31-16 = XB, X15-0 = XA, Y31-16 = YB, Y15-0 = YA.

The implementation of this twos-complement 32x32 multiplier is shown in Figure 11. The outputs of the 16x16 multipliers are connected to two levels of adders to give a 64-bit product. The first level of adders is needed to add the two central partial products of Figure 10, XA*YB and XB*YA. Notice the technique which is used to generate the "sign extension", or the most-significant sum bit of the first level of adders. The 'S556 provides, as a direct output, the complement of the most-significant product bit; having this signal immediately speeds up the sign-extension computation, and reduces the external parts count.



* THESE ARE ADDER BLOCKS USING THE 'S381, A 4-BIT ALU FUNCTION GENERATOR, TO PERFORM A HIGH SPEED ADD OPERATION. THE 'S182 IS A LOOK-AHEAD CARRY GENERATOR WHICH REDUCES THE PROPAGATION DELAY. ALL THE ABOVE PARTS ARE AVAILABLE FROM MONOLITHIC MEMORIES INCORPORATED.

TOTAL MULTIPLY TIME = MULTIPLIER DELAY + ADDER LEVEL 1 DELAY + ADDER LEVEL 2 DELAY = 90 + 65 + 65 = 220 nsec

Figure 11. Implementation of the 32x32 Multiplier

For example, the inputs to the adder in the most significant position are the $\overline{S31}$ outputs from the two central multipliers. The sign extension of the addition of XA*YB and XB*YA is defined as

SIGN EXT = $\overline{A.\overline{B}. + \overline{A}.C. + \overline{B}.C.}$, where

A is the most-significant bit of the term XA*YB;
B is the most-significant bit of the term XB*YA; and
C is the carry-in to the most-significant bits of XA*YB and XB*YA, in the adder.

The sign extension can be computed as the negation of the carry-out term of three terms, $\overline{A}$, $\overline{B}$, and C. This term corresponds to the negative of the carry-out of the bit position just one place to the right of the most-significant bit position of the first level of adders. The negative of the carry-out can be generated by presenting a carry-out and a binary "one" to the most significant bit of the adder. The generated sum bit then corresponds to the negation of the carry-out of the previous stage, which is the sign extension required to be added to the 16 most-significant bits of the XB*YB partial product term.

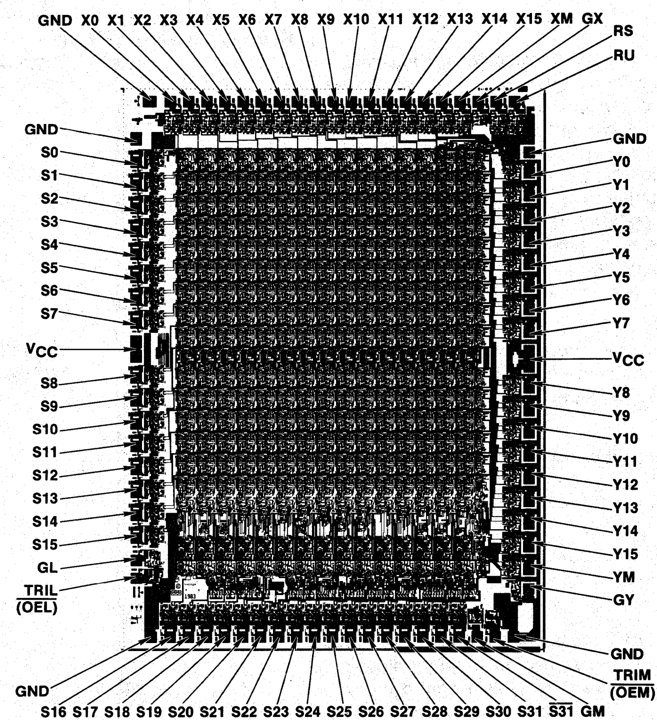
The second level of adders, which performs a 48-bit add function, is fairly straightforward. These adders can be implemented using 'S381 four-bit ALUs and 'S182 carry-bypasses ("carry-lookahead generators") which are available from Monolithic Memories Inc. and from other vendors.

Other configurations such as 48x48 and 64x64 multipliers can be designed using the same methodology, r1.

References

1. "Fast 64x64 Multiplication using 16x16 Flow-through Multiplier and Wallace Trees," Marvin Fox, Chuck Hastings, and Suneel Rajpal, *Monolithic Memories System Design Handbook*, pages 4-77 to 4-84.

Die Configuration



Die Size = 183x243 mil^2

8x8 High Speed Schottky Multipliers
SN54/74S557 SN54/74S558

Features/Benefits

- Industry-standard 8x8 multiplier
- Multiplies two 8-bit numbers; gives 16-bit result
- Cascadable; 56x56 fully-parallel multiplication uses only 34 multipliers for the most-significant half of the product
- Full 8x8 multiply in 60ns worst case
- Three-state outputs for bus operation
- Transparent 16-bit latch in 'S557
- Plug-in compatible with original Monolithic Memories' 67558

Description

The 'S557/'S558 is a high-speed 8x8 combinatorial multiplier which can multiply two eight-bit unsigned or signed twos-complement numbers and generate the sixteen-bit unsigned or signed product. Each input operand X and Y has an associated Mode control line, X_M and Y_M respectively. When a Mode control line is at a Low logic level, the operand is treated as an unsigned eight-bit number; whereas, if the Mode control is at a High logic level, the operand is treated as an eight-bit signed twos-complement number. Additional inputs, R_S and R_U, (R, in the 'S557) allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding signed or unsigned fractional numbers.

The 'S557 internally develops proper rounding for either signed or unsigned numbers by combining the rounding input R with X_M, Y_M, $\overline{X_M}$, and $\overline{Y_M}$ as follows:

$R_U = \overline{X_M} \cdot \overline{Y_M} \cdot R$ = Unsigned rounding input to 2^7 adder.

$R_S = (X_M + Y_M)\ R$ = Signed rounding input to 2^6 adder.

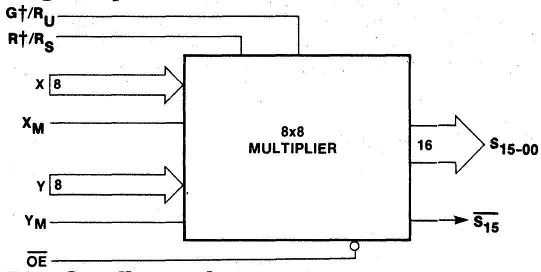
Since the 'S558 has no latches, it does not require the use of pin 11 for the latch enable input G, so R_S and R_U are brought out separately.

The most-significant product bit is available in both true and complemented form to assist in expansion to larger signed multipliers. The product outputs are three-state, controlled by an assertive-low Output Enable which allows several multipliers to be connected to a parallel bus or be used in a pipelined system. The device uses a single +5V power supply and is packaged in a standard 40-pin DIP.

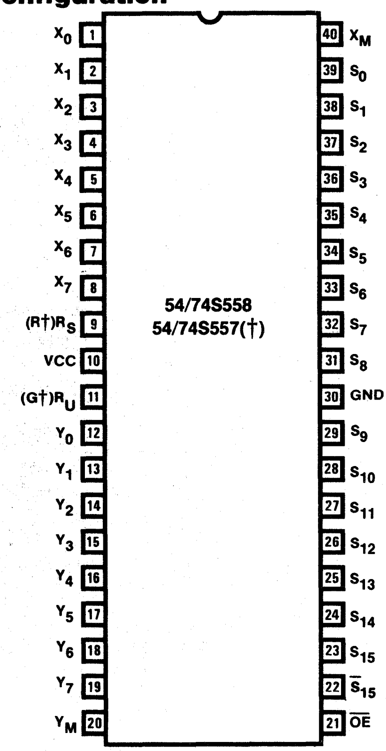
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
54S557, 54S558	J, (44), (L)	Military
74S557, 74S558	N,J,	Commercial

Logic Symbol

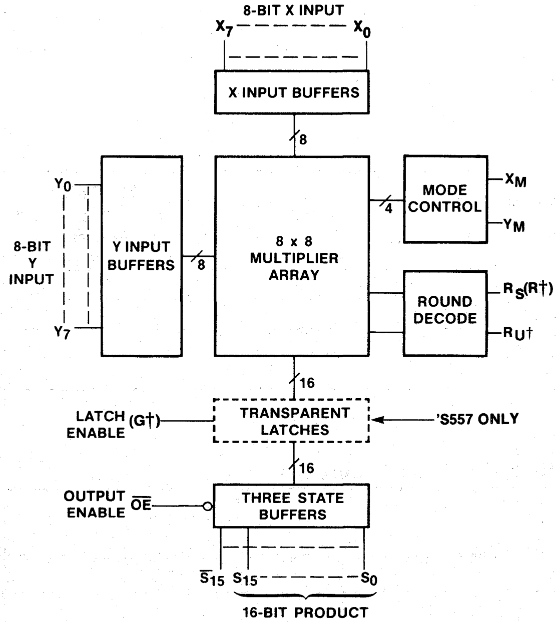


Pin Configuration



†For 54/74S557 Pin 9 is R and Pin 11 is G.

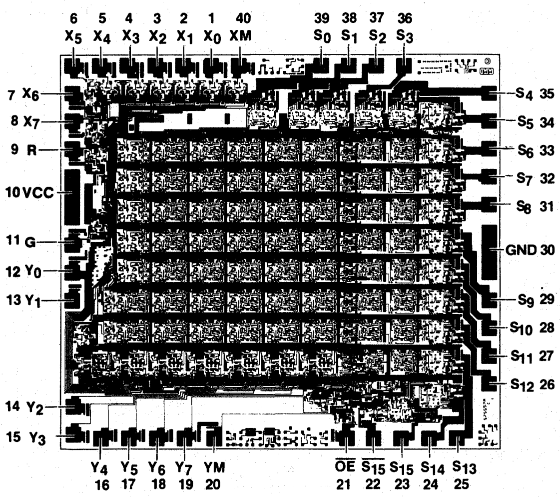
Logic Diagram



†For 54/74S557 Pin 9 is R and Pin 11 is G.

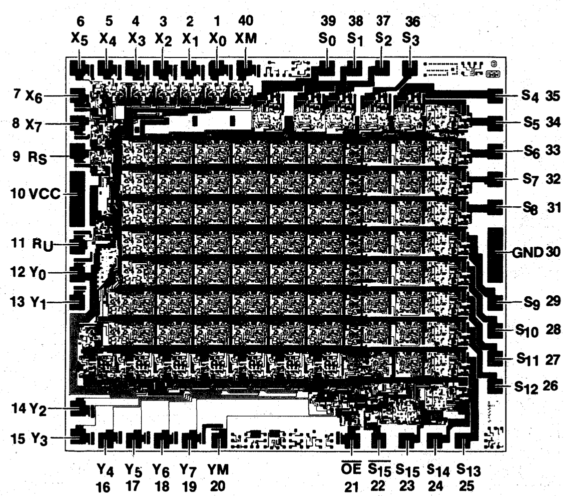
Die Configurations

'S557



Die Size: 144x130 mil^2

'S558



Die Size: 144x130 mil^2

10

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	DEVICE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNITS
V_{CC}	Supply voltage	all	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	all	-55		125*	0		75	°C
t_{su}	X_i, Y_i to G set	'S557	50			40			ns
t_h	X_i, Y_i to G hold time	'S557	0			0			ns
t_w	Latch enable pulse width	'S557	20			15			ns

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−1	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			100	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V			−100	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX			200	280	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

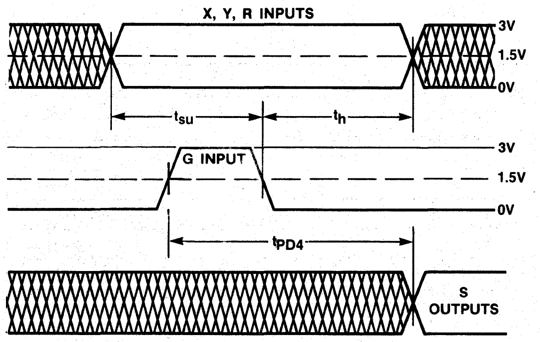
† Typicals at 5.0V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	DEVICE	TEST CONDITIONS	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{PD1}	X_i, Y_i to S_{7-0}	All	C_L = 30pF, R_L = 560Ω, see test figures		40	60		40	50	ns
t_{PD2}	X_i, Y_i to S_{15-8}	All			45	70		45	60	ns
t_{PD3}	X_i, Y_i to $\overline{S}_{15}$	All			50	75		50	65	ns
t_{PD4}	G to S_i	'S557			20	40		20	35	ns
t_{PXZ}	$\overline{OE}$ to S_i	All			20	40		20	30	ns
t_{PZX}	$\overline{OE}$ to S_i	All			15	40		15	30	ns

Timing Waveforms

Setup and Hold Times ('S557)

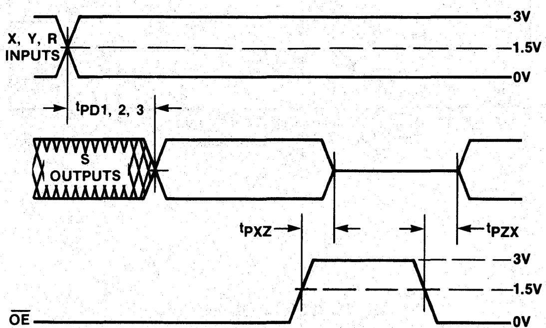


NOTE: If the rising edge of G occurs *before* ($t_{SU_{MIN}}$-$t_{W_{MIN}}$) from the inputs changing, then the applicable propagation delays are t_{PD}, t_{PD2} and t_{PD3}, (and not t_{PD4}). In this case the time at which the results arrive at the outputs depends on when the inputs change instead of when the rising edge of G occurs.

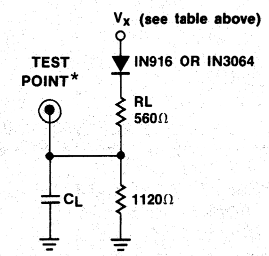
Test Waveforms

TEST	V_X		OUTPUT WAVEFORM — MEAS. LEVEL
All t_{PD}	5.0V		V_{OH}, V_{OL}, 1.5V
t_{PXZ}	for t_{PHZ}	for t_{PLZ}	V_{OH}, V_{OL}, 0.5V, 0.5V, 2.8V, 0.0V
	0.0V	5.0V	
t_{PZX}	for t_{PZH}	for t_{PZL}	2.8V, 0.0V, 1.5V, V_{OH}, V_{OL}
	0.0V	5.0V	

Propagation Delay

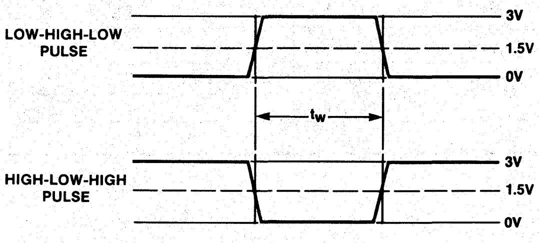


Test Load

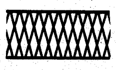
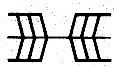


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Latch-Enable Pulse Width ('S557)



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

10

SUMMARY OF SIGNALS/PINS	
X_7-X_0	Multiplicand 8-bit data inputs
Y_7-Y_0	Multiplier 8-bit data inputs
X_M, Y_M	Mode control inputs for each data word; LOW for unsigned data and HIGH for twos-complement data
S_{15}-S_0	Product 16-bit output
$\overline{S}_{15}$	Inverted MSB for expansion
R_S, R_U	Rounding inputs for signed and unsigned data, respectively ('S558 only)
G	Transparent latch enable ('S557 only)
$\overline{OE}$	Three-state enable for S_{15}–S_0 and $\overline{S_{15}}$ outputs
R	Rounding input for signed or unsigned data; combined internally with X_M, Y_M ('S557 only)

ROUNDING INPUTS
'S557

INPUTS			ADDS	
X_M	Y_M	R	2^7	2^6
L	L	H	YES	NO
L	H	H	NO	YES
H	L	H	NO	YES
H	H	H	NO	YES
X	X	L	NO	NO

'S558

INPUTS		ADDS		USUALLY USED WITH	
R_U	R_S	2^7	2^6	X_M	Y_M
L	L	NO	NO	X	X
L	H	NO	YES	H†	H†
H	L	YES	NO	L	L
H	H	YES	YES	*	*

†In mixed mode, one of these could be Low but not both.
*Usually a nonsense operation. See applications section of data sheet.

74S557 FUNCTION TABLE

INPUTS		PRODUCT RESULT FROM ARRAY	LATCH CONTENTS (INTERNAL TO PART)	OUTPUTS	FUNCTION
$\overline{OE}$	G	T_i	Q_i	S_i	
L	L	X	L	L	Latched
L	L	X	H	H	
L	H	L	(L)*	L	Transparent
L	H	H	(H)*	H	
H	L	X	(L)	Z	Hi-Z; Latched Data not Changed
H	L	X	(H)	Z	
H	H	X	(X)*	Z	Hi-Z

*Identical with product result passing through latch.

MODE CONTROL INPUTS

OPERATING MODE	INPUT DATA		MODE CONTROL INPUTS	
	X_7-X_0	Y_7-Y_0	X_M	Y_M
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos-Comp.	L	H
	Twos-Comp.	Unsigned	H	L
Signed	Twos-Comp.	Twos-Comp.	H	H

Functional Description

The 'S557 and 'S558 multipliers are 8x8 full-adder Cray arrays capable of multiplying numbers in unsigned, signed, twos-complement, or mixed notation. Each 8-bit input operand X and Y has associated with it a mode control which determines whether the array treats this number as signed or unsigned. If the mode control is at High logic level, then the operand is treated as a twos-complement number with the most-significant bit having a negative weight; whereas, if the mode control is at a Low logic level, then the operand is treated as an unsigned number.

The multiplier provides all 16 product bits generated by the multiplication. For expansion during signed or mixed multiplication the most-significant product bit is available in both true and complemented form. This allows an adder to be used as a subtractor in many applications and eliminates the need for certain SSI circuits.

Two additional inputs to the array, R_S and R_U, allow the addition of a bit at the appropriate bit position so as to provide rounding to the best signed or unsigned fractional eight-bit result. These inputs can also be used for rounding in larger multipliers. In the 'S557, these two inputs are generated internally from the mode controls and a single R input.

The product outputs of the multiplier are controlled by an assertive-low $\overline{\text{Output Enable}}$ control. When this control is at a Low logic level the multiplier outputs are active, while if the control is at a High logic level then the outputs are placed in a high-impedance state. This three-state capability allows several multipliers to drive a common bus, and also allows pipelining of multiplication for higher-speed systems.

Rounding

Multiplication of two n-bit operands results in a 2n-bit product†. Therefore, in an n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples illustrate the difference between the two conversion techniques in decimal arithmetic:

$$\left.\begin{array}{l}39.2 \rightarrow 39\\ 39.6 \rightarrow 39\end{array}\right\}\ \text{Truncating}$$

$$\left.\begin{array}{l}39.2 + 0.5 = 39.7 \rightarrow 39\\ 39.6 + 0.5 = 40.1 \rightarrow 40\end{array}\right\}\ \text{Rounding}$$

Obviously, rounding maintains more precision than truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single-length LSB to the MSB of the discarded part; e.g., in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding 0.05 to the number and truncating the LSB:

$$39.28 + 0.05 = 39.33 \rightarrow 39.3$$

The situation in binary arithmetic is quite similar, but two cases need to be considered: signed and unsigned data representation. In signed multiplication, the two MSBs of the result are identical, except when both operands are −1; therefore, the best single-length product is shifted one position to the right with respect to the unsigned multiplications. Figure 1 illustrates these two cases for the 8x8 multiplier. In the signed case, adding one-half of the S_7 weight is accomplished by adding 1 in bit position 6, and in the unsigned case 1 is added to bit position 7. Therefore, the 'S558 multiplier has two rounding inputs, R_S and R_U. Thus, to get a rounded single-length result, the appropriate R input is tied to V_{CC} (logic High) and the other R input is grounded. If a double-length result is desired, both R inputs are grounded for the 'S558, and the single R input is grounded for the 'S557.

†In general: multiplication of an M-bit operand by an N-bit operand results in an (M + N)-bit product.

BINARY POINT

(a) SIGNED MULTIPLICATION

			X_7 •	X_6	X_5	X_4	X_3	X_2	X_1	X_0							
	X		Y_7 •	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0							
(a) SIGNED MULTIPLICATION		S_{15}	S_{14} •	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0 ← FULL 15-BIT PRODUCT
* OMIT S_{15} SINCE $S_{14} = S_{15}$	+		• 0	0	0	0	0	0	0	0	1	0	0	0	0	0	0 ← ADD 1/2 THE MSB WEIGHT OF THE DISCARDED PART
			* S_{14} •	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	S_7							

BEST 8-BIT PRODUCT

* OMIT S_{15} SINCE $S_{14} = S_{15}$

(b) UNSIGNED MULTIPLICATION

		• X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0								
	X	• Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0								
(b) UNSIGNED MULTIPLICATION		• S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0 ← FULL 16-BIT PRODUCT
	+	• 0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0 ← ADD 1/2 THE MSB WEIGHT OF THE DISCARDED PART
		• S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8								

BEST 8-BIT PRODUCT

NOTES:

(a) In signed (twos-complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best eight-bit product is from S_{14} through S_7, and rounding is performed by adding "1" to bit position S_6.

(b) In unsigned notation the best 8-bit product is the most significant half of the product and is corrected by adding "1" to bit position S_7.

Figure 1. Rounding the Result of Binary Fractional Multiplication

Signed Expansion

The most-significant product bit has both true and complement outputs available. When building larger signed multipliers, the partial products (except at the lower stages) are signed numbers. These unsigned and signed partial products must be added together to give the correct signed product. Having both the true and complemented form of the most-significant product bit available assists in this addition. For example, say that two signed partial products must be added and MSI adders are used; we then have the situation of adding together the carry from the previous adder stage plus the addition of the two negative most-significant partial-product bits. The result of adding these variables must be a positive sum and a negative carry (borrow). The equations for this are:

$S = A \oplus B \oplus C$

$C_{OUT} = AB + BC + CA$

where C is the carry-in and A and B are the sign bits of the two partial products.

Now an adder produces the equations:

$S = A \oplus B \oplus C$

$C_{OUT} = AB + BC + CA$

Examining these equations, it can be seen that, if the inversions of A and B are used, then the most significant sum bit of the adder is the sign extension bit.

$\text{Sign ext} = AB + B\bar{C} + \bar{C}A = \overline{\bar{A}\bar{B} + \bar{B}C + C\bar{A}}$,

and the sum remains the same.

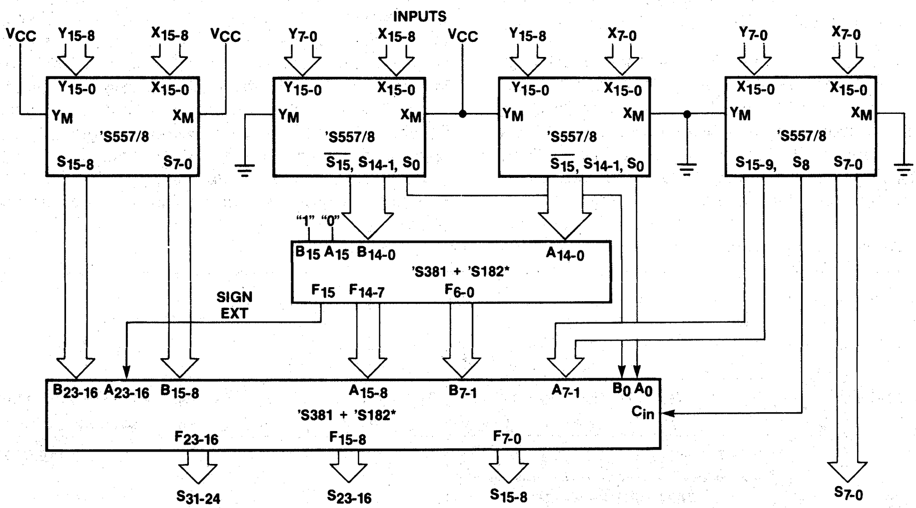
16x16 Twos-Complement Multiplication

The 16-bit X operand is broken into two 8-bit operands (X_7-X_0 and X_{15}-X_8), as is the Y operand. Since the situation is that of a cross-product, four partial products are generated as follows:

$$A = X_L * Y_L$$
$$B = X_L * Y_H$$
$$C = X_H * Y_L$$
$$D = X_H * Y_H$$

where the subscript L stands for bits 7-0, ("low or least-significant half), and the subscript H stands for bits 15-8.

Expanded twos-complement multiplication requires a sign extension of the B and C partial products. Thus, B_{15} and C_{15} need to be extended eight positions to the left (to align with D_{15}). In this approach two more adders are required. But the complement of the MSB ($\bar{S}_{15}$) on the 'S557/8 can be used to save these two adders. Figure 2 shows the implementation of 16x16 signed twos-complement multiplication in this manner.



* THESE ARE ADDER BLOCKS USING THE 'S381, A 4-BIT ALU FUNCTION GENERATOR, TO PERFORM A HIGH-SPEED ADD OPERATION. THE 'S182 IS A LOOKAHEAD CARRY GENERATOR AND REDUCES THE PROPAGATION DELAY. ALL OF THE ABOVE PARTS ARE AVAILABLE FROM MONOLITHIC MEMORIES INCORPORATED.

TOTAL MULTIPLY TIME = MULTIPLIER DELAY + ADDER LEVEL 1 DELAY + ADDER LEVEL 2 DELAY = 60+44+64 = 168 nsec

Figure 2. 16x16 Twos-Complement Signed Multiplication

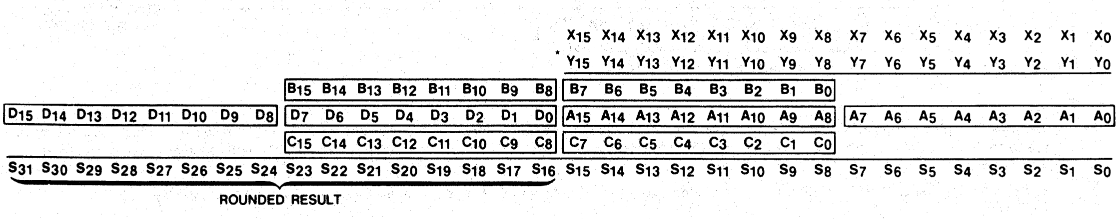


Figure 3. Unsigned Expansions of the 8x8 Multiplier to 16x16 Multiplication

Applications: How to Design Superspeed Cray Multipliers with '558s

by Chuck Hastings

Multiplication, as most of us think of it, is performed by repeated addition and shifting. When we multiply using pencil and paper, according to the familiar elementary-school method, we first write down the multiplicand, and then write down the multiplier immediately under it and underline the multiplier. Then we take the least-significant digit of the multiplier, multiply that digit by the entire multiplicand, and record the answer in the top row of our workspace, underneath the line. Then we repeat, using now the second-least-significant multiplier digit, and record that answer below the first one, pushed one digit position (that is, "shifted") to the left. This process continues until we run out of multiplier digits (or out of patience), at which point we add up the constants of the whole diamond-shaped workspace and record at the bottom an answer which consists of either m + n - 1 digits or m + n digits, where there are m digits in the multiplier and n digits in the multiplicand. An example, voila':

```
     125  (multiplicand)
    x107  (multiplier)
  ---------------------------------------------------
     875  (7 x 125)
    000   (0 x 125, shifted left one digit position)
   125    (1 x 125, shifted left two digit positions)
  ---------------------------------------------------
   13375  (sum of the above)
```

Figure 4. Decimal Multiplication

The decimal number system has no monopoly on truth — our ancestors simply happened to have ten fingers at the time when someone came up with the idea of counting. Binary numbers, as you know, are more copacetic than are decimal numbers with digital-logic elements, which like to settle comfortably into one voltage state ("High) or another ("Low"), rather than into one of ten different states. So we can repeat the above example using binary numbers, right? First, we convert our multiplicand and multiplier to binary:

$$125_{10} = 01111101_2$$
$$107_{10} = 01101011_2$$

The subscripts 10 and 2 refer to the "base" or "radix" of the number system, 10 for decimal and 2 for binary. (Remember your New Math?) For sneaky reasons to be revealed soon, I've used 8-bit binary numbers, which is one bit more than necessary for my example, and added a leading zero. So, we multiply:

```
         01111101₂ = 125₁₀
        x01101011₂ = 107₁₀
         --------
         01111101
        01111101
       00000000
      01111101
     00000000
    01111101
   01111101
  00000000
  ----------------
  0011010000111111 = 13375₁₀
```

Figure 5. Binary Multiplication

I've left off the remarks this time, but they're just like the remarks in the decimal example, at least in principle. Just in case you doubt this answer, I'll convert it back:

1	1	
1	2	
1	4	
1	8	
1	16	
1	32	
0	0	(64)
0	0	(128)
0	0	(256)
0	0	(512)
1	1024	
0	0	(2048)
1	4096	
1	8192	
0	0	(16384)
0	0	(32768)
	13375	

Figure 6. Binary-to-Decimal Conversion

Now look carefully at the diamond-shaped array of numbers in the workspace in Figure 5. Each row is either the multiplicand 01111101, or else all zeroes. The 01111101 rows correspond to "1" digits in the multiplier, and the all-zero rows to "0" digits in the multiplier. Life does get simpler in some ways when we switch to binary numbers: "multiplying a multiplier digit by the multiplicand" now means just gating a copy of the multiplicand into that position if the digit is "1," and not doing so if the digit is "0."

Seymour Cray, the master computer designer from Chippewa Falls, Wisconsin, whose career has spanned three companies (Univac, Control Data, and now Cray Research) and many inventions, first observed some time in the late 1950s that *computers* also could actually multiply this way, if one merely provided enough components. This last qualifying remark; in those days when even transistors, let alone integrated circuits, in computers were still a novelty was by no means a trivial one! To prove his point (and satisfy a government contract), Cray designed, and Control Data built, a 48x48 multiplier which operated in one microsecond, about 1960. This multiplier was part of a special-purpose array processor for a classified application, and was so big that a CDC 1604 (then considered a large-scale processor) served as its input/output controller. In principle, such a multiplier at that time would have had to consist of 48 48-bit full adders or "mills," each of which received one input 48-bit number from the outputs of the mill immediately above it in the array, and the other 48-bit number from a gate which either allowed the multiplicand to pass through, or else supplied an all-zero 48-bit number. Actually, these mills have to be somewhat *longer* than 48 bits. Anyway, that is at least 2304 full adders, and in 1960 a full-adder circuit normally occupied one small plug-in circuit card.

A later version of this multiplier, in the CDC 7600 supercomputer, could produce one 48x48 product out every 275 nanoseconds on a pipelined basis. The pipelining was asynchronous, and the entire humungous array of adders and gating logic could have up to three different products rippling down it at a given instant!

Back to the 1980s. Monolithic Memories has for several years produced an 8x8 Cray multiplier, the 57/67558, as a single 600-mil 40-pin DIP. After we invented this part, AMD second-sourced it, and by now it has become an industry standard. We now also have faster pin-compatible parts, the 54/74S558 and 54/74S557. Like other West Coast companies 2,000 miles from Wisconsin and Minnesota where Seymour Cray does his inventing, Monolithic Memories previously used the term "combinatorial multiplier" instead of "Cray multiplier" for this type of part. However, "combinatorial multiplier" has nine extra letters and five extra syllables, and also inadvertently implies that the technique involves combinatorial logic rather than arithmetic circuits. Some West Coast designs, including our 67558, use a modified internal array with only half as many full-adder circuits and slightly different interconnections, based on the two-bit "Booth-multiplication" algorithm (see reference 1), plus the "Wallace-tree" or "carry-save adder" technique (see references 2 and 3). Conceptually, however, the entire chip or system continues to operate as a Cray multiplier.

The '558, in particular can be thought of as a static logic network which fits exactly the binary multiplication example of Figure 5. (See now why I insisted on using 8-bit binary numbers?) There are no flipflops or latches whatever in the '558 — it is a "flow-through" device. Its 40 pins are used up as follows:

Use of Pins	Input, Output, or Voltage	Number of Pins
Multiplier	I	8
Multiplicand	I	8
Double-Length Product	O	16
Complement of Most-Significant Bit of Double-Length Product	O	1
3-State Output Enable	I	1
Number-Interpretation-Mode Control	I	2
Rounding Control for Product	I	2
Power and Ground	V	2
		40

Table 1. Use of Pins in the '558

The two number-interpretation-mode control pins, one for the multiplier and one for the multiplicand, allow the format for each of these two 8-bit input numbers to be chosen independently, as follows:

Control Input	Interpretation of 8-bit Input Number
L	8-bit unsigned
H	7-bit plus a sign bit

Table 2. Mode Control Input Encoding

The two rounding control pins allow either integer (right-justified) or fractional (left-justified) interpretation of the 14-bits-plus-sign double-length product of two 7-bits-plus-sign numbers for internal rounding of the double-length result to the most accurate 8-bit number. The control encoding is:

R_S Input	R_U Input	Effect
L	L	Disable Rounding
L	H	Round Unsigned
H	L	Round Signed
H	H	Nonsense (see below)

Table 3. Rounding Control Input Encoding

Rounding is normally disabled if the entire 16-bit double-length product output is to be used. If only an 8-bit subset of this product is to be used, this subset can be either bits 15-8 for unsigned rounding as shown in Figure 7, or bits 14-7 for signed rounding as shown in Figure 8. In either case, a "1" is forced into the '558's internal adder network at the bit position indicated by the arrow; adding a "1" into the bit position *below* the least-significant bit of the final answer has the effect of rounding, as you can see after a little thought. Obviously, forcing a "1" into *both* of these adder positions at the same time is a nonsense operation for most applications — it adds a "3" into the middle of the double-length result.

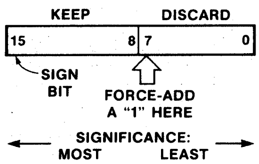


Figure 7. Unsigned Rounding

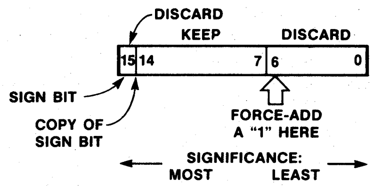


Figure 8. Signed Rounding

By now you probably have a fairly good idea of what a '558 is, and would like a few hints as to how to use it, right? First of all, there is an occasional application in things like video games for *very* fast multiplication, either 8x8 or 16x16, controlled by an 8-bit microprocessor, where there would be one '558 per system (see reference 4). More typically, however, the '558 is a building block, and several of them are used within one system; in fact, maybe more than several — "many." In the usual Silicon-Valley jargon, we can *cascade* a number of '558 (8x8) Cray-multiplier chips to create larger Cray multipliers at the systems level.

For the sake of concreteness, I'll discuss the case of 56x56 multipliers, which are appropriate in floating-point units which deal with "IBM-long-format" numbers which have a 56-bit mantissa. Any computer which emulates, or uses the same floating-point format as, any of the following computers can use such a multiplier:

IBM 360/370
Amdahl 470
Data General Eclipse
Gould/System Engineering SEL 32
Norsk Data 500 (different format)

There are two basic approaches: serial-parallel, and fully parallel. The serial-parallel approach uses seven '558s, and requires seven full multiply-and-add cycles. On the first cycle, the least-significant eight bits of the multiplier are multiplied by the entire multiplicand, and this partial product is saved. On the second cycle, the next-least significant eight bits of the multiplier are multiplied by the multiplicand, and that product (shifted eight bit positions to the left) is added into the first partial product to form the new partial product. And so forth, for five more cycles. It's almost like our decimal-multiplication example of Figure 1, except that instead of base-10 decimal digits we now have base-256 superdigits.

The fully-parallel approach totally applies Cray's usual design philosophy (sometimes characterized as "big, fast, and simple") at the systems level. It uses 49 '558s, in seven ranks; the 'i'th rank performs an operation corresponding to that done during the 'i'th cycle in the serial-parallel implementation. In principle, a complete mill is used to add the outputs of one rank of '558s to those of the rank above it. Or, alternatively, these mills can be laid out in a "tree" arrangement, such as:

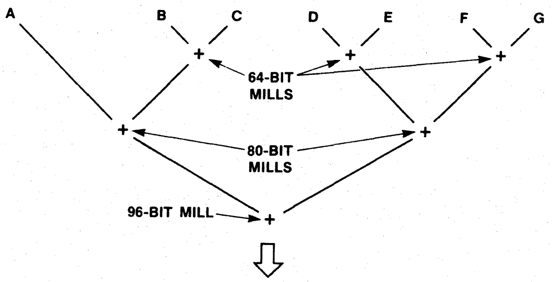


Figure 9. "Tree" Summing Arrangement of Mills for a 56x56 Cray Multiplier

Each letter stands for one rank of '558s, and each "+" stands for a mill of the indicated length. More involved "Wallace-tree" techniques are usually preferable. (See reference 3). If the least-significant half of the double-length product is *never* needed, only 34 'S558s are required. There is one subtlety which needs to be mentioned. If, conceptually, a '558 looks like a diamond —

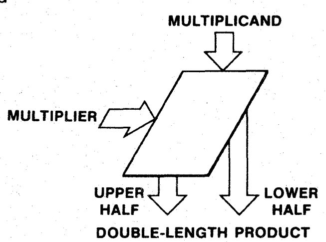


Figure 10. A Single '558 in "Diamond" Notation

then, the 8x56 multiplier for the serial-parallel configuration (which is also one rank of the fully-parallel configuration, which has seven such ranks) looks like this:

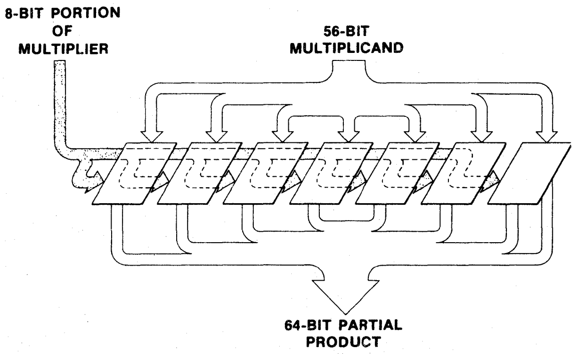


Figure 11. 8x56 Cray Multiplier in "Diamond" Notation

As you may discover after a moment's thought, *each* slanted double line in Figure 8 calls for addition of the outputs of *two* '558s — the eight most significant bits of one, and the eight least-significant bits of the next one to the left. There must also be an extra adder (or at least a "half adder") to propagate the carries from this addition all the way over to the left end of the result. The upshot is that an extra 56-bit mill is needed, in addition to the '558s. The eight least-significant bits of the least-significant '558 do not have to go through this mill, since they do not get added to anything else.

One final note: building up a large Cray-multiplier configuration out of '558s requires a *lot* of full adders, or else a lot of something else equivalent to them. Monolithic Memories also makes the 54/74S381 (a 4-bit "ALU" or "*A*rithmetic *L*ogic *U*nit") and the 54/74S182 (a carry-bypass circuit which works well with the '381); and two faster ALUs, the 54/74F381 and the 54/74F382 are in design. These ALUs and bypasses are excellent building blocks from which to assemble the mills used for summation within a rank of '558s, and also the mills used for tree-summation of the outputs of all ranks. For how to put together one of these mills using '381s, '382s, and '182s, see reference 1. For how to use PROMs as Wallace trees, see reference 3.

Now you can go ahead, design your Cray multiplier out of '558s, and start multiplying full-length numbers together in a fraction of a microsecond. Sound like fun?

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2. "Real-Time Processing Gains Ground with Fast Digital Multiplier," Shlomo Waser and Allen Peterson, *Electronics,* September 29, 1977.

3. "Big, Fast and Simple — Algorithms, Architecture, and Components for High-End Superminis," Ehud "Udi" Gordon and Chuck Hastings, 1982 *Southcon Professional Program,* Orlando, Florida, March 23-25, 1982, paper no. 21/3.

4. "An 8x8 Multiplier and 8-bit μP Perform 16x16-bit Multiplication," Shai Mor, EDN, November 5, 1979, Monolithic Memories Article Reprint AR-109.

NOTE: All of these references are available as application notes from Monolithic Memories Inc.

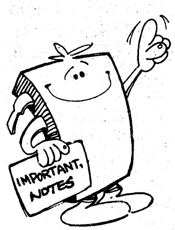

IMPORTANT, NOTES

Table of Contents
8-BIT INTERFACE

8-Bit Interface

PART NUMBER		FUNCTION	POWER	POLARITY	FEATURE
COMMERCIAL	MILITARY				
SN74LS241	SN54LS241	Buffer	LS	Noninvert	—
SN74LS244	SN54LS244				—
SN74LS341	SN54LS341				Schmitt Trigger
SN74LS344	SN54LS344				Schmitt Trigger
SN74LS210	SN54LS210			Invert	—
SN74LS240	SN54LS240				—
SN74LS310	SN54LS310				Schmitt Trigger
SN74LS340	SN54LS340				Schmitt Trigger
SN74S241	SN54LS241		S	Noninvert	—
SN74S244	SN54S244				—
SN74S341	SN54S341				Schmitt Trigger
SN74S344	SN54S344				Schmitt Trigger
SN74S731/-1	SN54S731/-1				MOS Driver
SN74S734/-1	SN54S734/-1				MOS Driver
SN74S210	SN54LS210			Invert	—
SN74S240	SN54S240				—
SN74S310	SN54S310				Schmitt Trigger
SN74S340	SN54S340				Schmitt Trigger
SN74S700/-1	SN54S700/-1				MOS Driver
SN74S730/-1	SN54S730/-1				MOS Driver
SN74LS245	SN54LS245	Buffer Transceiver	LS	Noninvert	—
SN74LS645	SN54LS645				—
SN74LS645-1	—				48 mA I_{OL}
SN74LS373	SN54LS373	Latch			—
SN74LS533	SN54LS533			Invert	—
SN74S373	SN54S373		S	Noninvert	—
SN74S531	—				32 mA I_{OL}
SN74S533	SN54S533			Invert	—
SN74S535	—				32 mA I_{OL}
SN74LS273	SN54LS273	Register	LS	Noninvert	Master Reset
SN74LS374	SN54LS374				—
SN74LS377	SN54LS377				Clock Enable
SN74LS534	SN54LS534			Invert	—
SN74S273	SN54S273		S	Noninvert	Master Reset
SN74S374	SN54S374				—
SN74S377	SN54S377				Clock Enable
SN74S383	SN54S383				Open Collector
SN74S532	—				32 mA I_{OL}
SN74S534	SN54S534			Invert	—
SN74S536	—				32 mA I_{OL}

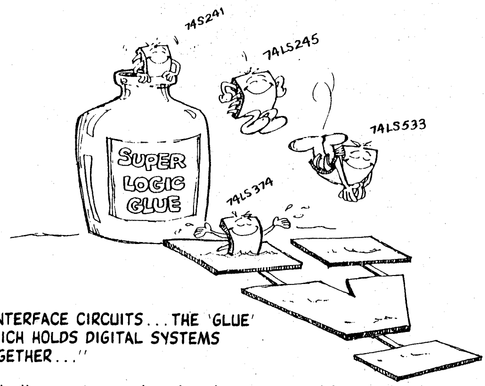
Pick the Right 8-Bit – or 16-Bit – Interface Part for the Job

Chuck Hastings and Bernard Brafman

Introduction

A few years ago, 20-pin 8-bit buffers, registers, latches, and transceivers came into existence as a rather haphazard upwards evolution from the MSI devices available in the mid-1970s. As time went on, usage of these parts increased until they became one of the fundamental computer-system building-block "primitives"—the "glue" which holds the entire system together. System designers demanded, and semiconductor manufacturers provided, many refinements such as inverting outputs to reduce parts count in assertive-low-bus systems, high-drive outputs to rescue designs with overloaded buses, Schmitt-trigger inputs to likewise rescue designs troubled with severe bus noise, high-voltage outputs specifically suited for driving MOS inputs, series-resistor outputs for driving highly-capacitive loads such as dynamic-MOS address buses, and so forth.

Today the demands are to reduce component costs and system board area. Reducing parts count achieves both of these objectives at one stroke. With the development of the 300-mil 24-pin SKINNYDIP™ package, it is now possible to effectively incorporate the equivalent of two 20-pin 8-bit interface parts into one 24-pin "16-bit interface" part. The approach is to look for common configurations of pairs of 8-bit parts, and implement the pair as a single chip. Common configurations include back-to-back "registered (or latched) transceivers," with the same options already available in the 20-pin 8-bit parts read back registers or latches, and pipelined registers or latches.



"INTERFACE CIRCUITS... THE 'GLUE' WHICH HOLDS DIGITAL SYSTEMS TOGETHER..."

Interface Basics

Where Do Interface Circuits Fit In?

Interface circuits appear as unglamorous bread-and-butter commodity items, as compared to many of the other more complex integrated circuits of today: their sales volume is very high, their average selling price is comparatively low, and essentially interchangeable parts are offered by several suppliers. They have the humble role of being the "glue" which holds digital systems together; they are *means* rather than ends in themselves.

When preliminary system block diagrams turn into detailed schematics, the *blocks* turn into complex circuits—microprocessors, multipliers/dividers, automatic dynamic-MOSRAM refresh controllers, high-speed FIFOs, programmable-logic circuits, arithmetic-logic units, and so forth. But then, however, the *lines* between those blocks turn into interface circuits, which must be there in the final design but never explicitly get noticed during the conceptual-design stage!

The term "interface" is actually a bit of a misnomer, since it implies that these parts always occur at a boundary between two somewhat different types of logic. That may have been true once, and it is still true that many of the circuits commonly called "interface" have inputs and/or outputs which are different electrically from those of, say, triple three-input NAND gates produced using the identical solid-state-circuit technologies. But a general working definition of "interface circuits" also has to cover some other parts which get used in similar system roles, but have normal inputs and normal totem-pole or three-state outputs. One such definition, current today at Monolithic Memories, is

"... ultra-high performance integrated circuits which do not lend themselves to higher levels of integration, due either to their parallel data structure or to the electrical properties of their inputs and/or outputs."

Interface circuits get used wherever data must be held, transmitted on demand, power-amplified, level-shifted, read from a noisy bus, inverted, or otherwise operated upon in some simple electrical way. If more complex transformations of the data are called for, of a predominantly mathematical rather than electrical nature, the designer will typically try to perform the required operations with readymade LSI or MSI circuits. Even here, of course, interface circuits often have the inconspicuous but crucial role of performing format conversion so that several LSI circuits can communicate with each other. Still, they are viewed as "overhead," which system designers try to minimize and semiconductor producers often rank well below their top level of corporate priorities.

But interface circuits are here to stay, at least for several more years. And the realization is growing among both users and producers of semiconductors that, since interface parts are not about to vanish soon, they need to be treated as something more than afterthoughts to the design process. Users who select interface circuits shrewdly are achieving real gains in system performance and reliability, and significant reductions in system size, weight, and power consumption. Producers who do a conscientious and professional job of developing and marketing these humble parts are finding increased demand for their wares, even during recessions.

Two major trends currently evident in the world of interface circuits are:

- **The emergence of an orderly, matrix-like approach to interface products, so that taken all together they form an *array* rather than simply a splendid jumble of assorted types.**
- **A strong emphasis on increasing the number of data bits which can be handled or accomodated by a single interface-circuit package.**

This paper will discuss each of these trends in some detail, and will then go on to present some realistic interface applications based on several actual designs.

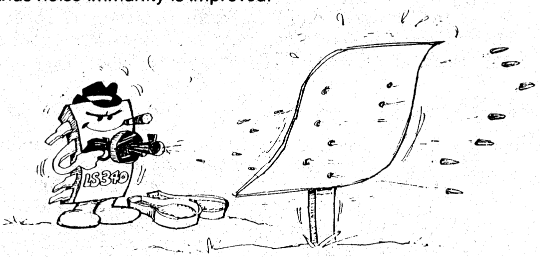
What Kinds of Interface Circuits Are There?

Commonly, the label "interface circuit" is applied to any of a diverse collection of miscellaneous devices which don't seem to fit into any other classification. As the term is used here, however, it means either one of three basic 8-bit types—buffers, latches, and registers—which are *simple* interface circuits, or else one of several 16-bit *compound* interface circuit types such as transceivers and pipelines.

Buffers merely "pass" or transmit information at increased power levels.Most contemporary buffer circuits, including 20-pin 8-bit buffers, also have an electronically-selectable electrical-isolation capability. Such a *three-state* buffer has a type of output which can be switched into a "hi-Z" (high-impedance) state in which it does not drive, nor appreciably load, the circuit node to which it is attached.

True or *noninverting* buffers pass the input information along with the same polarity (i.e., conventions in the representation of ones and zeroes by high and low voltages) that it had when it was received. *Inverting* buffers reverse the polarity of the input information from what was received, complementing all ones to zeroes and all zeroes to ones.

Most buffers feature standard PNP inputs. However, the 'S/'LS340/341/344/310 buffers feature Schmitt-trigger inputs, with a guaranteed 300/400-millivolt deadband (typically twice that) centered about the switching threshold voltage. (This notation is shorthand for "54/74S340, 54/74S341, 54/74S344, 54/74S310, 54/74LS340, 54/74LS341, 54/74LS344 and 54/74LS310," and will be used frequently hereafter.) These Schmitt-trigger buffers won't respond to input noise pulses which would make buffers with normal inputs start to switch, as long as the noise pulses do not completely cross the deadband; thus noise immunity is improved.



"...THE 'LS340/341/344/310 BUFFERS FEATURE SCHMITT-TRIGGER INPUTS, WITH A GUARANTEED... DEADBAND..."

Latches and *registers* have the same basic capability as buffers, but also have the additional capability that they retain stored information as long as power is supplied to them. Each of these circuit types requires an additional control signal in order to perform its system function.

More specifically, *latches* use an *enable* signal. When this signal is on, they store information, and their outputs do not change even if the information presented to their inputs changes. When their enable signal is off, latches act just like buffers. Turning on the enable signal in effect "freezes" in place whatever information was passing through the latch, so that the latch stores it.

Registers use a *clock* signal instead of an enable signal. When the clock signal goes through a transition from off to on, this "rising edge" causes the information present at the inputs to be stored in the register, and then to remain present at the register outputs until another rising edge occurs. When the clock is in a steady-state condition (a "level"), either on or off, or even when the clock goes through a transition from on to off (a "falling edge"), the outputs of the register do not change. Thus, unlike latches, registers lack a mode in which they act exactly like buffers and pass information directly from their inputs to their outputs. This lack is a consequence of the control signal being "edge-sensitive" rather than "level-sensitive."

Transceivers are bidirectional interface circuits capable of interconnecting two buses so that information can pass in either direction. Most of the transceiver parts in production today are *buffer transceivers*—they are like two cross-coupled buffer circuits within a single 20-pin package. A 16-bit buffer transceiver has eight A-bus data pins and eight B-bus data pins. Either the A-to-B buffers may be enabled, or the B-to-A buffers, or neither; if both sets of buffers were to be enabled, obviously there would be a race condition on each of the data lines, and so the control structure of some buffer transceivers specifically disallows that mode of operation. (Some other types do allow it.) Buffers which are not enabled are, of course, in the hi-Z state. Thus each buffer transceiver interface circuit consists of eight logical elements, and each of these logical elements consists of two simple-buffer elements cross-coupled back-to-back so that the input line for one is the output line for the other and conversely.

Latch transceivers and *register transceivers* are now positioned to become major factors in the marketplace; several semiconductor houses now offer such devices. In particular, Monolithic Memories now supplies several different families of these devices in the 24-pin 300-mil SKINNYDIP® package; some of these families are also supplied by Texas Instruments. A variety of speeds and architectures are available; see section 12 of this Databook for details.

Pipelines are unidirectional interface circuits having more than one full-width internal latch/register or "stage," but typically having just one set of parallel data inputs and one set of parallel data outputs. Two-stage latch pipelines, and both two-stage and four-stage register pipelines, are available. The four-stage devices can store twice as much information per package, but the two-stage devices can be reconfigured more flexibly and have a greater degree of separate control for each stage.

Understanding and Using Interface

How Designers Choose Interface Circuits

In the real world, a digital-logic designer doesn't set out deliberately to use some particular interface circuit whose properties he has carefully learned, in the same way that he might for instance set out to use a bit-slice registered ALU or a multiplier/divider. Rather, as we have said, it is much more likely that it all starts with some innocent-looking little line between two blocks on his preliminary system block diagram which, it turns out, can't really be just a simple little line after all.

Maybe the data which travels on that little line goes away at the source unless the little line is actually also capable of seizing it at the proper time and remembering it. Or maybe the end of the little line is an assertive-low system bus, with enough loads hanging off it to call for almost 30 milliamps of drive capability in whatever contemplates driving the bus, which doesn't quite jibe with the 2-milliamp drive capabilities and assertive-high outputs of the MOS LSI device from which the data is coming.

At this point the designer needs an interface circuit, and—wittingly or unwittingly—he must go through a several-stage decision process to determine what interface circuit he needs to actually implement that little line, before his block diagram can turn into a system. He must also fervently hope that, by the time he gets to the final twig on his decision tree, the interface part he needs will turn out to actually exist. Figure 1 is an example.

A top-down design approach, as illustrated in Figure 1, isn't always wise with integrated circuits, simply because the chances are fairly good that the desperately needed circuit actually *won't* exist[r1]. And there was a time, not all that long ago, when only a quasi-random subset of all of the obviously possible variations of the basic interface parts had reached full production status, so that they could be bought and plugged in. The hapless designer just had to memorize what that subset was, and do his design bottom-up from there.

Today, chaos is giving way to order, and enough of the possible interface parts which a designer might want do by now exist (or will exist shortly) that the kind of top-down thought process portrayed in Figure 1 really *will* work out all right when designing with interface. For instance, the line of interface parts now in production at Monolithic Memories is sufficiently orderly to be organizable into the matrix of the Interface Selection Guide on page 11-3 of this databook. Although this Guide is still somewhat irregular, it is at least recognizable as first-cousin to a logic-design Karnaugh map, and you can actually get your hands on any of the interface parts in the matrix.

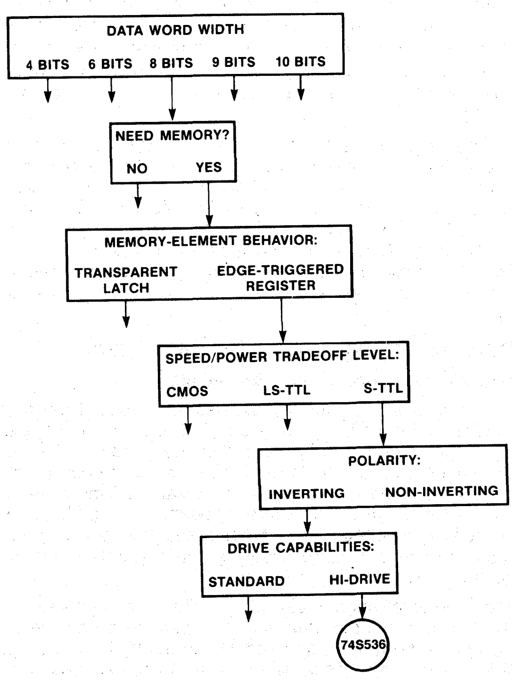


Figure 1. Interface-Circuit-Selection Decision Tree

The dimensions of variation for interface parts in any such Karnaugh map are, of course, two-valued "Boolean" variables. It is realistic from both logical and historical viewpoints to consider that all of the interface parts of the Interface Selection Guide have been derived from a very few basic types, by implementing those combinations which make sense of several two-valued properties of interface parts. These are:

- Commercial versus military temperature-range operation.
- High-speed Schottky (S-TTL) or low-power Schottky (LS-TTL) speed/power range.
- Noninverting or inverting outputs.
- No memory capabilities in the logical elements, so that they operate as buffers; or memory capabilities therein, further subdivided according to whether the logical elements operate as latches or registers.
- Compound 16-bit interface circuits or simple 8-bit interface circuits.
- Hi-drive or standard levels of current-sinking capability (I_{OL}) at the outputs.
- Schmitt-trigger or standard inputs.
- For non-three-state parts, master-reset or clock-enable control inputs.
- Series-resistor or standard outputs.

Obviously, not all imaginable combinations of the above properties actually exist as parts, or would even be useful if they did; and semiconductor houses cannot afford for long to offer 2^n interface-circuit part types for rapidly increasing n. Moreover, certain of the properties which in the past have had just two possible major choices (e.g., S-TTL and LS-TTL) today have more than two; for instance, Section 12 of this Databook includes some CMOS parts.

Nevertheless, by now the matrix approach has been fully-enough implemented to offer a very helpful perspective to the working designer.

Part numbers today allow some of the properties of interface circuits to be directly inferred, at least if the part number follows the conventions of the industry-standard "54/74" numbering series. 54/74 part numbers have a well-defined format VVE4TxxxP, with the following interpretation:

- VV — a prefix which varies somewhat from vendor to vendor.
- E4 — a temperature-range environmental specification. "54" implies the military temperature range (−55°C to +125°C), and "74" the commercial temperature range (0°C to +70°C for several vendors, and 0°C to +75°C for Monolithic Memories). In any case, interface circuits must run properly over a very wide temperature range.
- T — a solid-state-circuit technology. Upwards of a dozen of these have been promoted, with widely varying success, during the last decade. The earliest one, plain old gold-doped TTL, omitted using any special letter in part numbers. Today, the two dominant technologies are "S" (high-speed Schottky) and "LS" (Low-power Schottky). Others becoming quite important include "F" (for "FAST," a lower-power form of high-speed Schottky); "ALS" (advanced low-power Schottky); and "SC," "HCT" and "ACT" (isoplanar CMOS processed to be fully TTL-voltage-level compatible).
- xxx — a two-digit, three-digit, and today sometimes even four-digit number which uniquely specifies the *pin-out* of the part and its "functional behavior" (see the explanation which follows), independent of speed/power range.

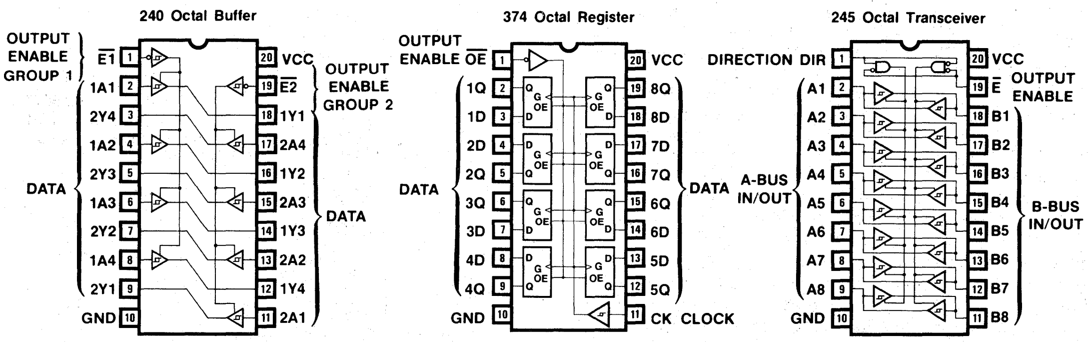
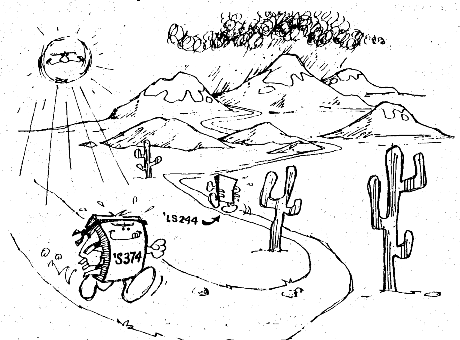


Figure 2. Pinouts for the Three Basic 20-Pin Interface Parts

- P — a package type: plastic, cerdip, flatpack, leadless chip carrier, sidebrazed ceramic, small-outline surface-mount, or whatever.

The functional behavior of a circuit can be defined somewhat circularly as **"what a designer needs to know about the circuit in order to construct designs which operate properly using parts from any supplier interchangeably."** This definition is akin to one classic definition of computer architecture as **"...the structure of the computer a programmer needs to know in order to be able to write any program that will correctly run on the computer."**[r2]



"... INTERFACE CIRCUITS MUST RUN PROPERLY OVER A VERY WIDE TEMPERATURE RANGE ..."

Two parts produced using different solid-state-circuit technologies may exhibit essentially the same functional behavior. If that is the case, and if either part will also satisfy system timing constraints (which is an issue quite separate from that of "functional behavior") and input/output voltage compatibility constraints, the designer does not need to care what kind of internal gates are used within the part—Schottky TTL, ECL, CMOS, NMOS, or water wheels. On the other hand, two parts produced using the same technology may have subtle, or even drastic, differences in their functional behavior; for example, one may have inverting outputs, or hi-drive outputs, or Schmitt-trigger inputs whereas the other does not.

The Matrix of Interface Part Types

The interface parts of the Interface Selection Guide mostly have one of just three different pinouts, shown in Figure 2, in their usual 20-pin plastic or cerdip SKINNYDIP form.

All of the buffers have the same pinout as the 'S240. They differ in speed/power range, in the polarity of the outputs, in the noise-rejection capabilities of the inputs (Schmitt-trigger or standard), and in enable structure (complementary or assertive-low) as shown in Figure 3, which really *is* unequivocally a Karnaugh map.

	COMPLEMENTARY ENABLES		ASSERTIVE-LOW ENABLES		
S-TTL	'S210	'S241	'S244	'S240	USUAL INPUTS
S-TTL	'S310	'S341	'S344	'S340	SCHMITT-TRIGGER INPUTS
LS-TTL	'LS310	'LS341	'LS344	'LS340	SCHMITT-TRIGGER INPUTS
LS-TTL	'LS210	'LS241	'LS244	'LS240	USUAL INPUTS
	INVERTING OUTPUTS	NON-INVERTING OUTPUTS	NON-INVERTING OUTPUTS	INVERTING OUTPUTS	

Figure 3. 8-Bit Three-State Buffers

Most of the latches and registers have the same pinout as the 'S374. They differ in whether the memory control line is level-sensitive (latch) or edge-sensitive (register), in speed/power range, in the polarity of the outputs, and in the I_{OL} (current-sinking drive) capability of the outputs as shown in the Karnaugh map of Figure 4.

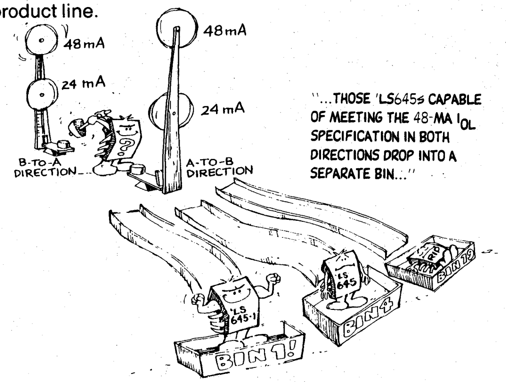
	LATCHES		REGISTERS		
S-TTL	'S533	'S373	'S374	'S534	USUAL (20-mA) OUTPUTS
S-TTL	'S535	'S531	'S532	'S536	HI-DRIVE (32-mA) OUTPUTS
LS-TTL	—	—	—	—	HI-DRIVE (32-mA) OUTPUTS
LS-TTL	'LS533	'LS373	'LS374	'LS534	USUAL (24-mA) OUTPUTS
	INVERTING OUTPUTS	NON-INVERTING OUTPUTS	NON-INVERTING OUTPUTS	INVERTING OUTPUTS	

Figure 4. 8-Bit Three-State Latches and Registers

11

The three transceivers of the Interface Selection Guide are more specifically *buffer transceivers*—compound 16-bit interface circuits like two 8-bit buffer circuits cross-coupled "back-to-back" within a single device. They differ in input-current and output-leakage-current specifications, which here are indistinguishable for test purposes since every data pin is both an input and an output; the 'LS245 specification is tighter. (The 'LS245-1 is *also* specified as faster, but that is *not* a difference in "functional behavior.") There is also a difference in I_{OL} capability; the 'LS645-1 is specified as higher. Actually, all three devices undergo identical fabrication, and are separated only at final testing; for instance, those 'LS645s capable of meeting the 48-mA I_{OL} specification in both directions drop into a separate bin.

Upcoming developments in interface parts will tend in many cases to follow the matrix approach, at least partially. Even where the new parts do not fit perfectly into the matrix of existing parts, some attention is likely to be paid to issues of balance and symmetry over the entire interface-circuit product line.

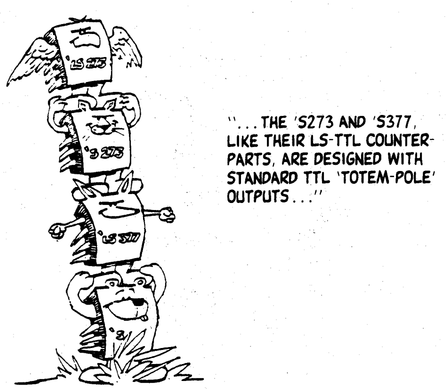


In some cases, new interface parts directly "fill in the holes" in the matrix. For instance, some recent additions to Monolithic Memories' line of interface parts are:

Function	Speed/ Power	Polarity	Feature	Part Number
Register	S	Noninv.	Master Reset	SN54/74S273
Register	S	Noninv.	Clock Enable	SN54/74S377 SN54/74S383@
Buffer	S	Noninv.	Series Output Resistor	SN54/74S734*
Buffer	S	Noninv.	Series Output Resistor	SN54/74S731
Buffer	S	Inv.	Series Output Resistor	SN54/74S730#
Buffer	S	Inv.	Series Output Resistor	SN54/74S700

NOTES: @—The 'S383 differs from the 'S377 only in having open-collector outputs rather than totem-pole outputs.
*—The 'S734 is a direct replacement for AMD's Am2966.
#—The 'S730 is a direct replacement for AMD's Am2965.

Table 1. Recent Additions to the Monolithic Memories Interface-Part-Type Matrix



The 'S273 and 'S377 bring to higher-performance TTL systems the same functional behavior which has long been available for medium-performance TTL systems, with the popular 'LS273 and 'LS377 parts. The 'S273 and 'S377, like their LS-TTL counterparts, are designed with standard TTL "totem-pole" outputs. Somehow, in the somewhat more chaotic early days of 8-bit interface, the need for high-speed Schottky versions of these parts got overlooked by most interface producers.

Since the 'S273 and 'S377 are totem-pole-output parts, the control pin which gets used on the 'S374 (whose pinout they otherwise follow) for "Output Enable" for the three-state outputs is available for something else. The 'S273 uses it as a "Master Reset" ($\overline{MR}$) input, capable of forcing all of the eight D-type flipflops on the chip into the off (low) state simultaneously, regardless of their previous state—*or* of the state of the clock line and/or the data-input lines. The 'S377, on the other hand, uses that same pin as a "Clock Enable" ($\overline{CK\ EN}$) input, which in effect either allows the clock signal to reach the eight D-type flipflops on the chip, or else cuts it off from reaching the flipflops so that they are not clocked and just sit there holding whatever information they contained previously. The 'S383 is a slight modification of the 'S377 to provide open-collector rather than totem-pole outputs.

The major applications for these parts are in situations where 'S374s would be difficult to control appropriately. Because of the 'S273's $\overline{MR}$ input, its forte is *control* applications—instruction registers, microinstruction registers, timing-pulse registers, and sequential circuits in general, and sometimes as eight *individual* separate D-type control flipflops in one package. In all of these applications, there *has* to be a way to force the system into some proper initial state, so that it "starts off on the right foot" and does not get into some unplanned-for, untestable, unpredictable machine-psycho condition on power-up. The 'S377, on the other hand, because of its $\overline{CK\ EN}$ input, is the optimum choice for the highest-performance TTL pipeline paths for data, instructions, microinstructions, and address parameters in "overlapped-architecture" machines such as array processors and high-performance minicomputers. Its open-collector counterpart, the 'S383, can be used to drive open-collector buses or to provide wired-OR or wired-AND logic functions.

The 'S700, 'S730, 'S731, and 'S734 feature a new type of output stage incorporating a series resistor, designed to efficiently drive highly-capacitative loads such as arrays of dynamic-MOSRAM inputs. Rise and fall times are more symmetric than with 'S240-type buffers, and the latter need an *external* series limiting resistor for their own protection when driving highly capacitative loads.

Consequently, although 'S240-type buffers may exhibit greater speed when tested under light loading conditions, 'S730-type buffers are likely to perform better under realistic system conditions when driving large distributed capacitative loads is a major factor in the application.

Of these four new buffers, two—the 'S730 and 'S734—are second-source versions of the Am2965 and Am2966 respectively, originally introduced by AMD. The other two—the 'S700 and 'S731—are complementary-enable versions of the 'S730 and 'S734 respectively, just as the 'S210 and 'S241 are complementary-enable versions of the 'S240 and 'S244 respectively. Complementary-enable buffers excel in driving buses with two multiplexed sources for the information, such as instruction addresses and data addresses in a bit-slice bipolar microcomputer system.

The four 'S730-type parts may be grouped with Monolithic Memories' line of conventional and Schmitt-trigger-input buffers in a 2x2 matrix chart or Karnaugh map, with the dimensions of this map chosen to be the polarity of the second-buffer-group enable input E_2 (here across the top) and the polarity of the data-buffer logical elements themselves (here down the side), thus:

		Polarity of E_2*	
		$\overline{E}_2$	E_2
Polarity of Data Buffers	Inverting	'LS240 'LS340 'S240 'S340 'S730	'LS210 'LS310 'S210 'S310 'S700
	Noninverting	'LS244 'LS344 'S244 'S344 'S734	'LS241 'LS341 'S241 'S341 'S731

* Since $\overline{E}_1$ is assertive-low for *all* of these parts, the parts with an assertive-low $\overline{E}_2$ are "assertive-low-enable" parts, whereas the parts with an assertive-high E_2 are "complementary-enable" parts.

Table 2. 8-Bit Buffers Grouped by Polarity and Enable Structure

By this time, many presently-unused SN54/74xxx part numbers have already been reserved for other potential new parts, even though not all of these parts are yet in production. Nevertheless, it was at least possible to part-number these four series-output-resistor buffers in such a way that the relationship among the four types remains the same as for 'S240-type buffers. To state this another way, one can add 490 to the last three digits of the usual buffer part number to get the part number for the corresponding series-output-resistor part, e.g., 'S241 + 490 = 'S731, etc.

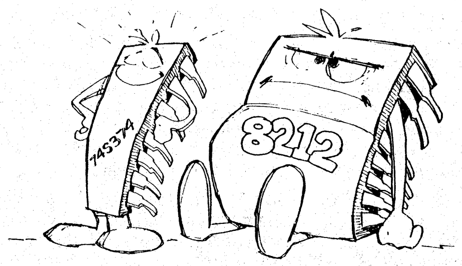
Directions In The Evolution of Interface Parts

More Bits per Package

Historically, the first interface parts were 16-pin TTL devices offered during the early 1970s, usually with four or six "logical elements" per package. One "logical element" handles one data bit; in simple interface parts, a logical element may be a buffer, a latch, or a register (with "register" here implying an edge-triggered flipflop).

As the digital-electronics industry shifted from MSI to LSI integrated circuits, and from the quaint and irregular old-time computer word lengths to word lengths which are multiples of eight bits (most often 8, 16, or 32), 8-bit interface devices became the only way to go for simple electrical data transformations—chip counts got intolerably high with 4-bit devices, and 6-bit devices were awkward misfits in most of the newer designs![3] And, to have eight input data lines, eight output data lines, power and ground, and two control signals, an integrated-circuit package has to have 20 pins.

To conserve board space, the width of this 20-pin package was chosen to be 300 mils (.300") like that of the overwhelming majority of the then-existing bipolar MSI and SSI devices. Hence, during the 1970s, the present 20-pin 300-mil SKINNYDIP package became the standard for interface circuits. One 20-pin SKINNYDIP takes up only about half as much board space as one of the older 600-mil 24-pin packages, which were then being used for a few early 8-bit interface parts such as the Intel 8212.



"...ONE 20-PIN SKINNYDIP™ TAKES UP ONLY ABOUT HALF AS MUCH BOARD SPACE AS ONE OF THE OLDER 600-MIL 24-PIN PACKAGES..."

24-pin interface parts were obviously the next major development to come. In the early 1980s, mechanical packaging problems which previously had inhibited the introduction of a 24-pin 300-mil SKINNYDIP were solved, and this package is now also in widespread use for PROMs, PAL programmable-logic circuits, and so forth. So what might one do with four additonal pins in an interface part?

One answer is to spend all four of them for additional *control* signals in order to achieve more flexible parts, such as the Monolithic Memories SN54/74LS380 "multifunction" 8-bit register. (See page 6-16 of this databook.) This part is actually implemented with "hard-array logic" technology, and has an internal structure like one form of PAL.

Another answer is to spend all four of them for additional *data* signals, equally for inputs and outputs. The result is 10-bit interface parts with functionality similar to that of existing 20-pin 8-bit parts.

A middle-of-the-road answer is to divide them equally between control signals and data signals. This approach leads to 9-bit interface parts with improved functionality.

16-bit "double-density" interface-circuits — dual 8-bit circuits in a single 24-pin SKINNYDIP — are a more far-reaching answer than the preceding ones. These circuits use the four extra pins to provide separate control inputs for *both* 8-bit internal groups, and also to provide improved functionality. The number of data pins is held at 16 by *multiplexing* the use of two 8-bit groups of input and/or output pins.

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The motivation for 16-bit interface parts is, first of all, to cut component counts by replacing two parts with one in as many situations as possible, in order to save board space and assembly costs. Particularly in high-performance computers and array processors, the packaging itself is expensive when it must be designed to provide a proper signal-transmission environment for ultra-fast logic. An almost-50% cut in the board area required for the interface parts—here, as always, the "glue" which holds the whole system together—may result in major indirect savings.

But there are other incentives besides sheer cost reduction which favor cramming as much logic as possible into a given board area. There usually is only one board size in a chassis (or even in a system), and any logic subsystem which cannot fit onto one such board immediately incurs a *speed* penalty attributable to board-to-board communications—extra buffers for noise-free signal transmission, extra signal-path length on each board over to the edge where the connectors are, more extra length in the backplane wiring, and lots of additional inductance and capacitance permeating all of the above.

So, saving board area is very likely to improve *both* system cost *and* system performance, by increasing the probability that a given logic subsystem will fit onto just one board.

Interface-part internal element density has for many years been increasing at a rate which is, to say the least, unspectacular. Going from four to six to eight to sixteen logical elements in an interface-circuit package doesn't seem like a whole lot, compared for instance to going from 1K to 4K to 16K to 64K to 256K bits in a single dynamic-MOSRAM package in roughly the same number of years.

But, consider what a *true* LSI interface circuit would have to look like—one with the same magnitude of "equivalent gate count" being bandied about for today's microprocessors, dynamic MOSRAMs, and so forth. First of all, it would need to have *several hundred data inputs* and *several hundred data outputs,* so that the most immediately-plausible mechanical design for a package would resemble a sea urchin! And, if it were implemented using any present-day TTL technology, the part would dissipate enough *watts* to need cooling fins like a Porsche cylinder head!

And so it has turned out that progress over time in increasing the logical-element density for interface parts has been more or less linear, while progress in increasing the level of integration for microprocessors and dynamic MOSRAMs has been more or less exponential. It is no accident that a basic phrase of the definition for "interface circuits" quoted earlier in this paper is **". . . which do not lend themslves to higher levels of integration . . ."** If these same density trends continue, digital electronic systems of the future may actually have a *higher* proportion of packages allocated to interface circuits than is typical today, which if it happens is likely to surprise quite a few people.

Structure of 16-Bit Interface Circuits

Common configurations of two 8-bit interface parts used together furnish a natural starting point for the definition of useful 16-bit interface parts. When the same configuration tends to occur over and over again, it is natural to "draw a boundary around it and put it all on one chip," unless of course the resulting compound chip turns out to need too many pins.

Figure 5 illustrates three such two-part configurations which are observably very common, and intuitively very plausible:

- "Back-to-back" or "cross-coupled." (Figure 5A).
- "Nose-to-tail" or "pipelined." (Figure 5B.)
- "Side-by-side" or "parallel." (Figure 5C.)

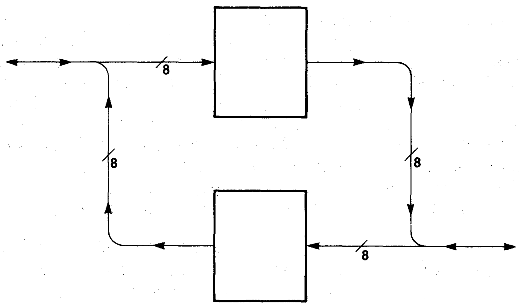

Figure 5A. Back-to-Back Configuration

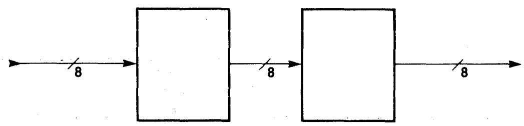

Figure 5B. Nose-to-Tail Configuration

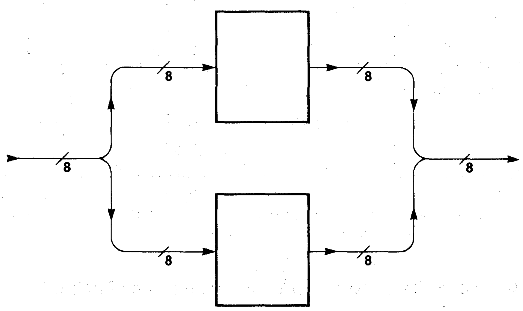

Figure 5C. Side-by-Side Configuration

Figure 5. Common Configurations of Two 8-Bit Interface Parts

The back-to-back configuration, when applied to simple 8-bit buffers, leads to buffer transceivers such as the 'LS245. The 'LS245 is, of course, still a 20-pin part; the choice was made to change its enable structure from that which would be strictly implied by placing two 'LS244s back-to-back, in order to hold the package size to 20 pins and to disallow having both directions simultaneously enabled. These same statements continue to hold for the 'LS645 and 'LS645-1. The 'LS640 and 'LS640-1 are inverting buffer transceivers, and the 'LS643 and 'LS643-1 incorporate an 8-bit inverting buffer back-to-back with an 8-bit noninverting buffer; there are also open-collector equivalents to these parts and the 'LS645 and 'LS645-1. The entire series features the same enable structure, with a master enable line $\overline{E}$ controlling *both* sets of buffers and a direction line DIR to allow just one direction to be enabled at a time.

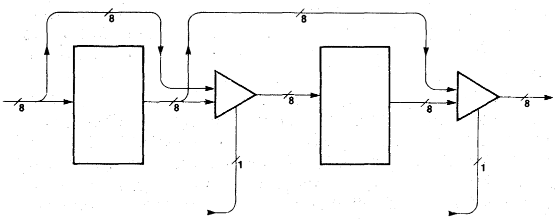

Figure 6. Two-Stage Pipeline Register Configuration

Applied to 'LS373 latches and 'LS374 registers, the back-to-back configuration leads to the 24-pin 'LS547 latch transceiver and the 'LS546 register transceiver respectively. These parts are just what one would expect them to be, with individual output-enable and clock control inputs for each 8-bit group, except that there are enough pins to also give each group clock-enable control inputs like the 'S377. The 'LS567 and 'LS566 are the corresponding inverting parts.

The nose-to-tail and side-by-side configurations do not lead to anything very interesting with buffers, at least as long as there are only enough pins for one 8-bit input data path and one 8-bit output data path. Latches and registers, however, are entirely another matter. It turns out to be attractive to *combine* these two configurations, even though at first glance they look quite dissimilar, into a single "two-stage pipeline" configuration as shown in Figure 6. Such a two-stage pipeline can operate in either a nose-to-tail mode or a side-by-side mode, according to the setting of the two internal multiplexers shown in Figure 6. Applied to 'LS373 latches and 'LS374 registers, this more powerful configuration leads to the 24-pin 'LS549 latch pipeline and the 'LS548 register pipeline. For these parts, the control inputs are a final-stage output enable, selects for each mux, a common clock (or latch-enable for the 'LS549) input for both stages, and individual clock-enable inputs for each stage.

To clarify the timing control of these parts, the 16-bit register parts ('LS546, 'LS566, and 'LS548) have individual clock-enable signals for each 8-bit group, and either individual clock signals ('LS546 and 'LS566) or a common clock signal ('LS548). The 16-bit latch parts ('LS547, 'LS567, and 'LS549), since the "clock" signal turns into a level-sensitive latch-enable signal, have two independent ways of enabling storage in each of the two stages. Thus, the 'LS547 and 'LS567 parts feature two separate and equivalent latch-enable control inputs for each 8-bit group, either one of which can cause the group to "latch up" and store information. The 'LS549 part has the same operating mode, except that each 8-bit group has one *separate* latch-enable control input and there is one more latch-enable input *common* to both groups.

Read-back latches and registers ('LS793 and 'LS794) also have a back-to-back structure; but their "return" element is a buffer (resembling, say, a '244), rather than another latch or register.

As with other TTL 8-bit latches and registers, the part-numbering scheme for all of the parts just mentioned assigns odd numbers to latches and even numbers to registers.

Front-loading latches are one other type of 16-bit interface part. The 'LS646 (noninverting) is to a first approximation an 'LS645 superimposed upon an 'LS546. (The numbering scheme wasn't *planned* to be that cute—it just happened.) The 'LS648 is a similar inverting part. To clarify what is meant, each of the eight logical elements of an 'LS646 consists of two back-to-back buffers and two back-to-back flipflops, with a parallelled buffer and flipflop pointing in the A-to-B direction and a similar buffer-flipflop pair pointing in the B-to-A direction. The 'LS646 and 'LS648 are three-state parts: the 'LS647 and 'LS649 are respectively the equivalent open-collector parts. The 'LS651 (inverting) and the 'LS652 (noninverting) are equivalent to the 'LS648 and 'LS646 respectively, but have a different control structure which allows independent enabling of either direction; the 'LS653 and 'LS654 are versions of the 'LS651 and 'LS652 respectively in which the A-direction output buffers are open-collector, and the B-direction buffers are still three-state.

32-bit interface parts are also visible on the horizon. Two four-stage pipelines, the Am29520 and Am29521, are offered by AMD as members of a series of signal-processing parts, and Monolithic Memories is introducing them also as the 'S720 and 'S721. As compared to the 'LS548 and 'LS549, they offer twice as many stored bits per square inch of board, but considerably less flexibility in accessing and controlling register contents.

The matrix approach to classifying various interface parts can be extended to encompass transceivers and pipelines, as is done in Table 3. The correspondence between the various 8-bit simple-interface parts and the 16-bit compound interface parts which are in a sense derived from them, is summarized in Table 4.

Configuration	Buffers	Latches	Registers	Front-Loading Latches
Simple	'210 '310 '240 '340 '241 '341 '244 '344	'373 '531 '533 '535	'374 '532 '534 '536	---
Back-to-Back	'245 '640 '640-1 '643 '643-1 '645 '645-1	'547 '567	'546 '566	'646 '647 '648 '649 '651 '652 '653 '654
Two-Stage Pipeline	---	'549	'548	---

Table 3. Matrix Classification Scheme for 8-Bit and 16-Bit Interface Parts

Simple Interface Type	Compound Interface Type	Number Of Pins	Buffer	Latch	Register
	Transceivers:				
'244	'245 '645 '645-1	20	X		
'240	'640 '640-1	20	X		
'240/'244	'643 '643-1	20	X		
'373	'547	24		X	
'374	'546	24			X
'533	'567	24		X	
'534	'566	24			X
	Pipelines:				
'373	'549	24		X	
'374	'548	24			X

Table 4. Equivalences Between Simple and Compound Interface Types

Various Applications of Interface Parts

Some Logic-Design Examples

Several illustrative designs using various interface parts may suggest some design insights and some creative ways to use interface. The designs presented have generally been excerpted from actual digital systems.

Reading a switch setting to establish an externally-defined system parameter, such as a device address, is a mundane but essential task in many microprocessor-based systems. Figure 7 illustrates how a group of eight switches may conveniently be read using a byte-wide buffer such as the 'LS244. Since the switches must be electrically isolated from the bus, the 'LS244's three-state outputs are disabled by control signals originated by the microprocessor until the time comes to read in the switch settings. Because the 'LS244 can supply up to 24 milliamps of I_{OL} to drive the bus, this simple scheme can be utilized even on heavily-loaded system data buses.

If still more drive capability is needed, an 'S244 in the same configuration can sink up to 64 milliamps. And, if the system is to be operated in an industrial environment and the switch signals entering the buffer inputs are subject to severe noise, the Schmitt-trigger 'LS344 type of buffer can also be substituted for the 'LS224 with no other change to the circuit.

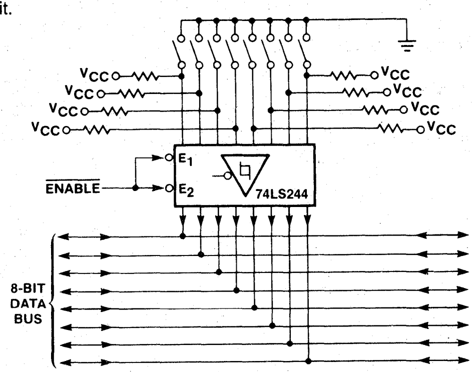

Figure 7. Switch-Setting Readin Circuit

Interfacing two separate buses is a very standard application for transceivers. Figure 8 shows an 'LS245, which has a control structure such that one control signal selects the *direction* of data transfer and the other one independently allows data transfer to be *enabled or disabled.* Thus, the two buses can be operated totally isolated from each other, or else either one may be made to follow the other. Depending on the drive-capability and polarity requirements of the application, any of the other buffer transceivers might be used here instead. Or, if memory as well as cross-coupling is required, a latch transceiver or register transceiver might also be used in a similar manner.

Driving a dynamic-MOSRAM address bus with a multiplexed row/column address can conveniently be done with an 'S700 as shown in Figure 9. This part is an inverting complementary-enable buffer with a series-resistor output structure, which is an ideal combination of characteristics here.

First of all, a TTL inverting buffer normally has one less transistor — and hence one less delay — in its internal data path than does an equivalent noninverting buffer, and hence is faster. And dynamic MOSRAMs really don't care if their addresses come in "true" or "complemented" form as long as that form *never* changes.

Second, a complementary-enable buffer can easily multiplex two different address sources to the same set of outputs without introducing extra switching delay, or allowing a momentary "bus fight" condition, if the same control signal (here $\overline{\text{CAS}}$ or "Column Address Strobe") is tied directly to both $\overline{E_1}$ and E_2 and the two 4-bit groups of outputs are tied together.

Finally, because of the internal series resistor in the'S700's output structure, this part (like the 'S730/1/4) can drive highly capacitative loads, of say up to 70 dynamic-MOSRAM inputs, without the need for external limiting resistors to control undershoot, resulting in a net system speed gain since signal rising and falling transition times remain symmetric. Otherwise, the effective logic delay of the buffer (which is simply the

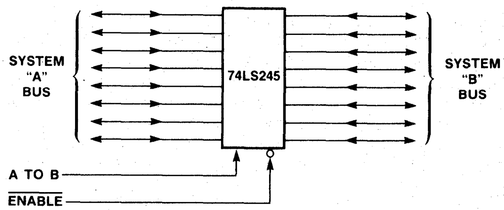

Figure 8. Interfacing Two Separate Buses

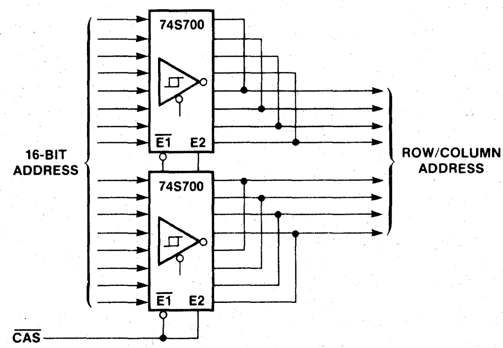

Figure 9. Multiplexed Row/Column Address Drivers

worse of the two transition times) would get degraded, since the use of an external series resistor would have greatly lengthened the low-to-high transition time.

Demultiplexing and holding address and data words for single-bus microprocessors is an application which takes advantage of the strong points of the 'S531 as shown in Figure 10. Since the 'S531 is a "transparent latch" and can operate as a buffer when necessary, the memory system designer can take advantage of the *full* time slots when the address and data signals are present on the microprocessor outputs. Because the address and data signals are then present for a longer period of time at the 'S531 outputs, it may be possible to use slower (and therefore less expensive!) memory devices than if edge-triggered registers had been used here instead. The three-state outputs of the 'S531 allow the designer to implement bidirectional data buses and DMA address schemes. Variations on this approach can use 'S373s if less drive capability is needed, or 'LS373s if less speed is needed as well; or 'S535s, 'S533s, or 'LS533s under the same respective circumstances if the address and data buses to be driven are assertive-low

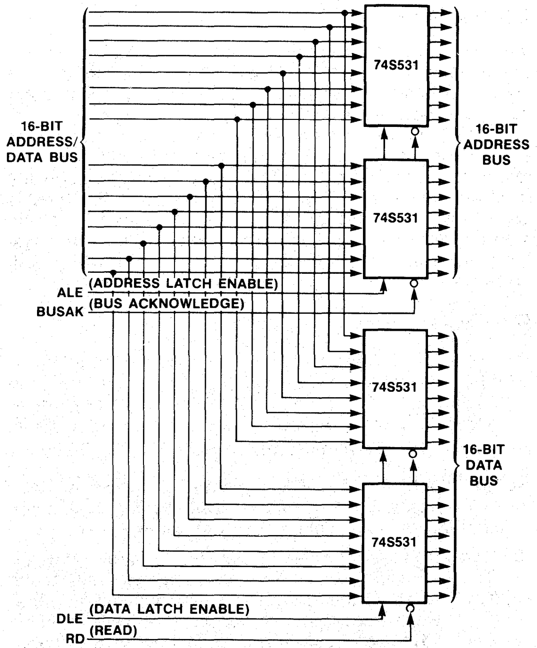

Figure 10. Address/Data Demultiplexer for Single-Bus Microprocessors

according to the system definition. If the data-bus interface needs to have latching capability also for data returning to the microprocessor, then 'LS547s are an excellent choice.

Synchronizing the state changes of a PROM-based control sequencer is easily performed using a register with a clock-enable feature, like the 'LS377 shown in Figure 11. In this simple sequencer, a 4-bit counter steps through the PROM addresses. The counter may be reset to address 0000, or loaded with any 4-bit address. The 32 × 8 PROM, with five address lines, allows for one external input as well as the four bits from the counter. The PROM outputs are pipelined using the 'LS377, which eliminates PROM output glitches, synchronizes the state changes of the sequencer with the system clock, and speeds up the effective cycle time. The availability of enable control inputs on both the counter and the 'LS377 allows forcing "wait" states, where both the counter and the register hold their current state for extended periods of time. If a higher-speed implementation of this design is needed, a 74S161 or 93S16 counter can replace the 74LS161, one of Monolithic Memories' new 63S081A ultra-speed 32x8 PROMs (15 nsec worst-case and 9 nsec typical for t_{AA}, instead of 50 and 37 nsec respectively) can replace the 6331-1, and an 'S377 can replace the 'LS377.

Saving Designs at the Last Minute, or Planning Ahead

Designs hanging out over the edge of unworkability can sometimes be salvaged without any redesign effort, by replacing standard interface parts with hi-drive, Schmitt-trigger-input, or even just inverting pin-compatible parts. Hi-drive parts such as the 'S532 or 'LS645-1 get dropped into 'S374 or 'LS645 sockets respectively late in the design cycle, when the designer suddenly discovers that he has hung several too many inputs on his main system bus. Schmitt-trigger-input parts such as the 'LS341 likewise get dropped into 'LS241 sockets shortly after the designer has recovered from his first observation of his actual bus waveforms on a good laboratory oscilloscope—it's that or back to the old drawing board. And, when he suddenly remembers after laying out a tightly packed board that "Oh, xxxx, that particular bus is assertive-*low*," it's nice to be able to simply substitute an 'S534 for an 'S374 in a few places rather than having to find room for several inverter packages. So a designer who has learned to think of interface parts in terms of the matrix approach will now and then find a particularly quick route to saving his skin.

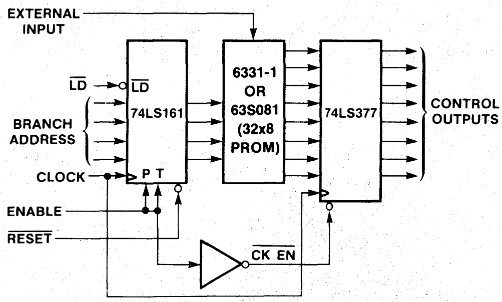

Figure 11. Synchronous PROM-Based Control Sequencer

However, an astute designer may use hi-drive, Schmitt-trigger-input, and inverting parts quite deliberately in order to gain speed, economy, drive capability, or noise immunity. A number of the industry-standard buses in the microcomputer world are assertive-low; and inverting buffers, latches, and registers are much more appropriate for connecting these to a microprocessor, or to a bit-slice arithmetic unit, than non-inverting parts with extra inverters in series just to make the polarity come out right. Similarly, Schmitt-trigger hex inverters whose only function in the data path is to provide noise immunity can be eliminated by using 'LS340-type buffers, which also provide significant drive capability and three-state outputs. The need to parallel three-state drivers and registers and split drive lines, just for extra drive capability, can be reduced or eliminated by using hi-drive parts. And, in an obvious but not trivial switch, substituting a high-speed Schottky part for a low-power Schottky equivalent part can beef up drive capability considerably.

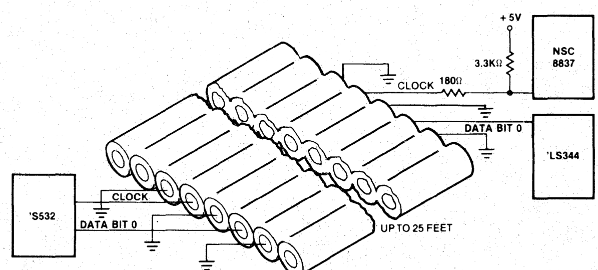

Figure 12. Flat-Cable Transmission Scheme Using Hi-Drive and Schmitt-Trigger-Input Interface Parts

Board-to-board signal transmission via flat cable is a particularly nice application for both hi-drive and Schmitt-trigger-input interface parts. The 32-milliamp outputs of, say, an 'S532 are better matched to the characteristic impedance of flat cable (usually 100 to 120 ohms) than 20-milliamp outputs would be. An adequate scheme, in many cases, for the

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transmission of *data* from board to board uses 3M or similar flat cable. Every second cable wire is grounded at both ends for shielding, so that signal wires alternate with ground wires ("signal-ground-signal-ground"), and there is at least one ground wire at each edge of the cable. Signal wires are driven by 32-mA hi-drive latches or registers, and the receivers are Schmitt-trigger-input buffers, and that's all there is to it—no resistors, capacitors, or black magic. For a strobe, clock, or control signal, a linear receiver such as a National Semiconductor 8837 is used together with a 180-ohm series resistor and a 3300-ohm shunt resistor to V_{CC}, as shown in Figure 12. This overall scheme is compatible with some Digital Equipment Corporation buses, and is good for transmission distances of up to 25 feet.

"...DESIGNS HANGING OUT OVER THE EDGE OF UNWORKABILITY CAN SOMETIMES BE SALVAGED..."

Conclusion

Interface parts seem primitive alongside of LSI microprocessors and dynamic MOSRAMs, but they are inescapable and smart designers today have learned how to use them astutely. A powerful aid in doing so is to think of the set of interface parts as an array, which fits into a matrix whose dimensions are various circuit properties. Even though the rate of progress seems slow, the bit-density and functionality of interface parts is steadily increasing, and the time is approaching for designers to learn to take the next logical step and use 16-bit interface parts extensively in their systems, in order both to save cost and to improve overall system performance.

References

r1. "Bottom-Up Design with LSI and MSI Components," Chuck Hastings, *Conference Proceedings of the Fourth West Coast Computer Faire.* 11-13 May 1979, pages 359-365. Available from the Computer Faire, Suite 110, 611 Veterans Boulevard, Redwood City, CA 94063.

r2. "Architecture of the IBM System/360," G. M. Amdahl, G. A. Blaauw, and F. P. Brooks, *IBM Journal of Research and Development,* Volume 8 (1964), pages 87-101.

r3. "The 20-Pin Octal Interface Family—Today's Computer-System Building Blocks," Chuck Hastings, applications note available from Monolithic Memories, Inc. A longer paper written when buffer transceivers were the only visible 16-bit parts, but with more detail on the 8-bit parts.

8-Bit Buffers

SN54/74LS210 SN54/74S210
SN54/74LS240 SN54/74S240
SN54/74LS241 SN54/74S241
SN54/74LS244 SN54/74S244

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '210 and '241 types combine multiplexer and driver functions

Description

These 8-bit buffers provide high speed and high current interface capability for bus organized digital systems. The three-state drivers will source a termination to ground (up to 133Ω) or sink a pull-up to V_{CC} as in the popular 220Ω/330Ω computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA I_{IL} on the low-power Schottky buffers and 0.4 mA I_{IL} on the Schottky buffers.

The '240 and '244 provide inverting and noninverting outputs respectively, with assertive low enables. The '210 and '241 also provide inverting and noninverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceive or multiplexer operation.

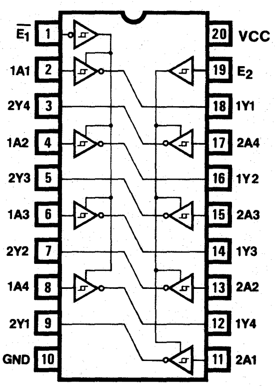
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Ordering Information

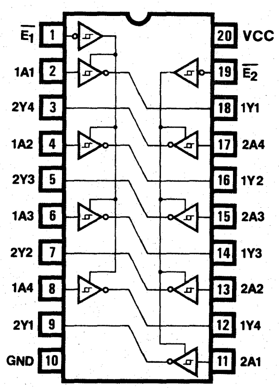
PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54LS210	J,L,W	Mil	High-Low	Invert	LS
SN74LS210	N,J	Com			
SN54LS240	J,L,W	Mil	Low		
SN74LS240	N,J	Com			
SN54LS241	J,L,W	Mil	High-Low	Non-Invert	
SN74LS241	N,J	Com			
SN54LS244	J,L,W	Mil	Low		
SN74LS244	N,J	Com			
SN54S210	J,L,W	Mil	High-Low	Invert	S
SN74S210	N,J	Com			
SN54S240	J,L,W	Mil	Low		
SN74S240	N,J	Com			
SN54S241	J,L,W	Mil	High-Low	Non-Invert	
SN74S241	N,J	Com			
SN54S244	J,L,W	Mil	Low		
SN74S244	N,J	Com			

Logic Symbols

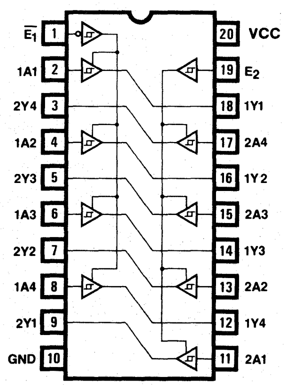
'210 8-Bit Buffer



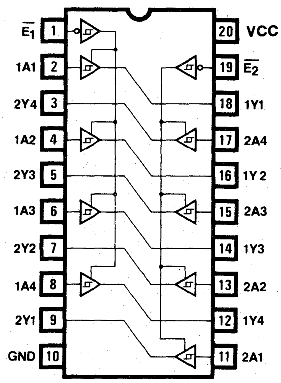
'240 8-Bit Buffer



'241 8-Bit Buffer



'244 8-Bit Buffer



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Monolithic Memories

Function Tables

'210

$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	H	Z
L	L	H	X	L	Z
L	H	L	L	H	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	H	L	L
H	H	X	L	Z	H
H	H	X	H	Z	L
H	L	X	X	Z	Z

'240

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	H	H
L	L	L	H	H	L
L	L	H	L	L	H
L	L	H	H	L	L
L	H	L	X	H	Z
L	H	H	X	L	Z
H	L	X	L	Z	H
H	L	X	H	Z	L
H	H	X	X	Z	Z

'241

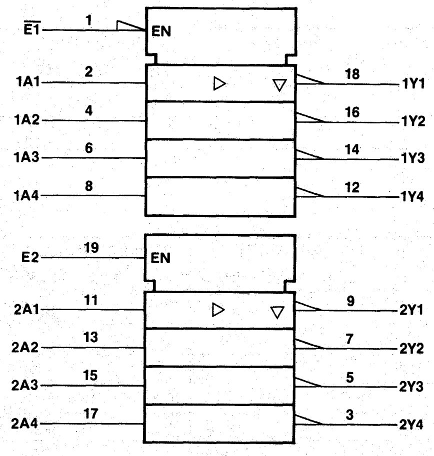
$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	L	Z
L	L	H	X	H	Z
L	H	L	L	L	L
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	H
H	H	X	L	Z	L
H	H	X	H	Z	H
H	L	X	X	Z	Z

'244

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	L	L
L	L	L	H	L	H
L	L	H	L	H	L
L	L	H	H	H	H
L	H	L	X	L	Z
L	H	H	X	H	Z
H	L	X	L	Z	L
H	L	X	H	Z	H
H	H	X	X	Z	Z

IEEE Symbols

'210



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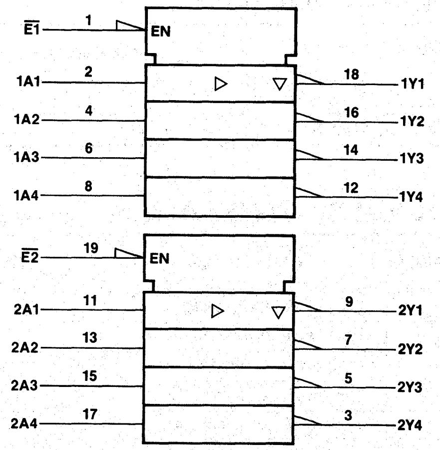

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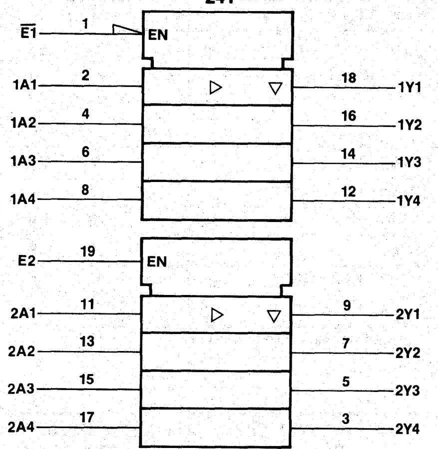

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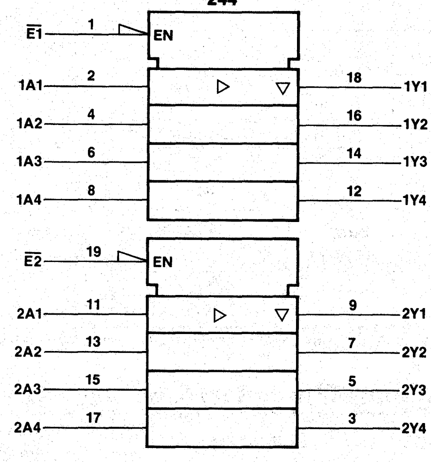

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Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 7 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN,	I_I = –18mA			–1.5			–1.5	V
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4V			–0.2			–0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7V			20			20	µA
I_I	Maximum input current		V_{CC} = MAX,	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA			0.4			0.4	V
				I_{OL} = 24mA						0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.5V, V_{IH} = 2V	I_{OH} = –3mA	2.4	3.4		2.4	3.4		V
				I_{OH} = –12mA	2						
				I_{OH} = –15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			–20			–20	µA
I_{OZH}				V_O = 2.7V			20			20	µA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		–40		–225	–40		–225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	LS210, LS240		17	27		17	27	mA
				LS241, LS244		17	27		17	27	
		Outputs Low		LS210, LS240		26	44		26	44	
				LS241, LS244		27	46		27	46	
		Outputs Disabled		LS210, LS240		29	50		29	50	
				LS241, LS244		32	54		32	54	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	LS210, LS240 MIN	LS210, LS240 TYP	LS210, LS240 MAX	LS241, LS244 MIN	LS241, LS244 TYP	LS241, LS244 MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}	Output Enable delay			20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				10	18		10	18	ns

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
ΔV_T	Hysteresis $(V_{T+} - V_{T-})$	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current, Any A	V_{CC} = MAX	V_I = 0.5V			−0.4			−0.4	mA
I_{IL}	Low-level input current, Any E	V_{CC} = MAX	V_I = 0.5V			−2			−2	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 48mA			0.55				V
			I_{OL} = 64mA						0.55	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −1mA				2.7			V
			I_{OH} = −3mA	2.4	3.4		2.4	3.4		
			I_{OH} = −12mA	2						
			I_{OH} = −15mA				2			
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50			−50	μA
I_{OZH}			V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current †	V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply Current, Outputs High	V_{CC} = MAX, Outputs open	S210,S240		80	123		80	135	mA
			S241,S244		95	147		95	160	
	Supply Current, Outputs Low		S210,S240		100	145		100	150	
			S241,S244		120	170		120	180	
	Supply Current, Outputs Disabled		S210,S240		100	145		100	150	
			S241,S244		120	170		120	180	

†Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	S210, S240 MIN	S210, S240 TYP	S210, S240 MAX	S241, S244 MIN	S241, S244 TYP	S241, S244 MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 50pF R_L = 90Ω		4.5	7		6	9	ns
t_{PHL}				4.5	7		6	9	ns
t_{PZL}	Output Enable delay			10	15		10	15	ns
t_{PZH}				6.5	10 *		8	12	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 90Ω		10	15		10	15	ns
t_{PHZ}				6	9		6	9	ns

* For the S210 add 2 ns for the E_2 (Pin 19) enable

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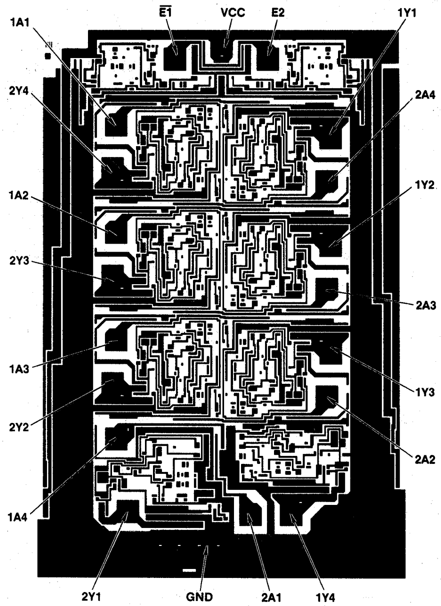
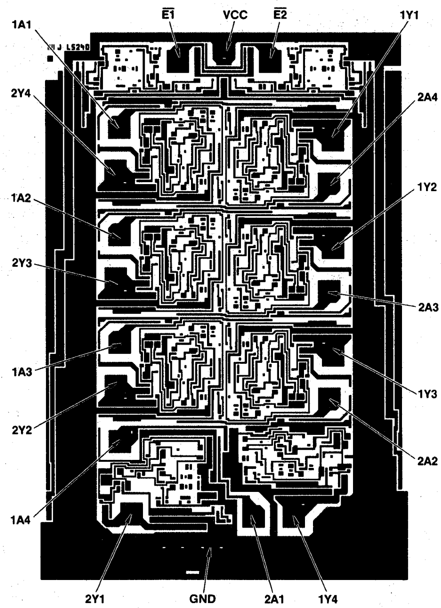
Die Configurations

'LS210

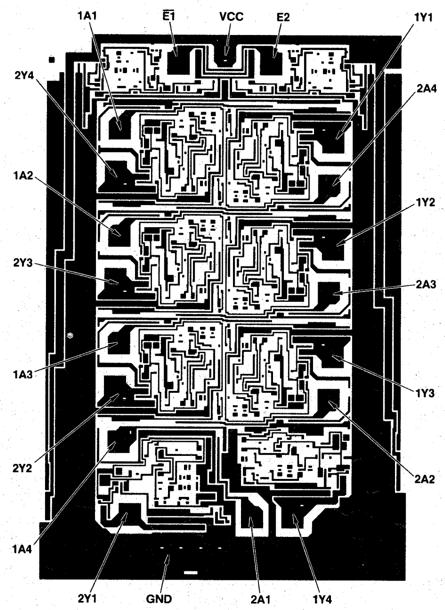


'LS240

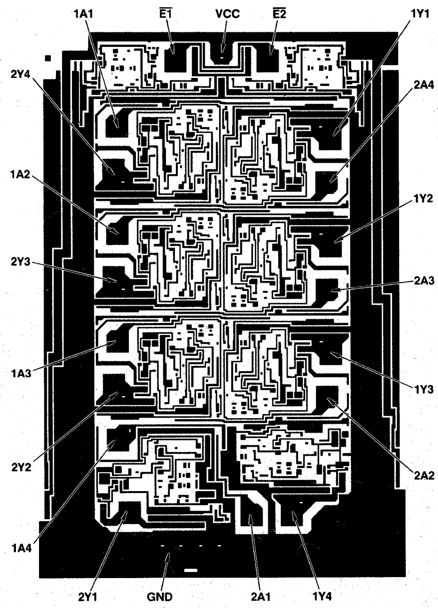


Die Size: 85x146 mil^2

'LS241

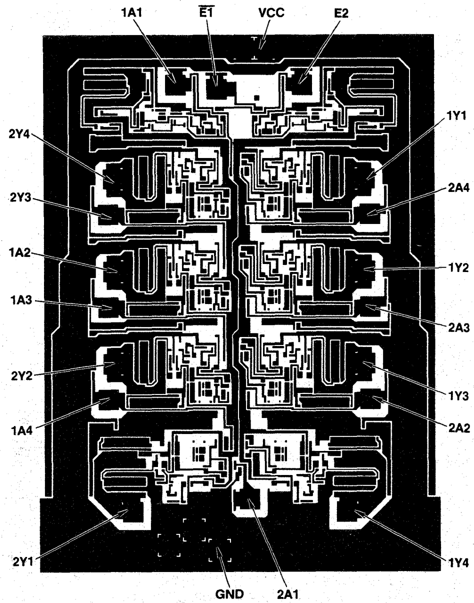


'LS244

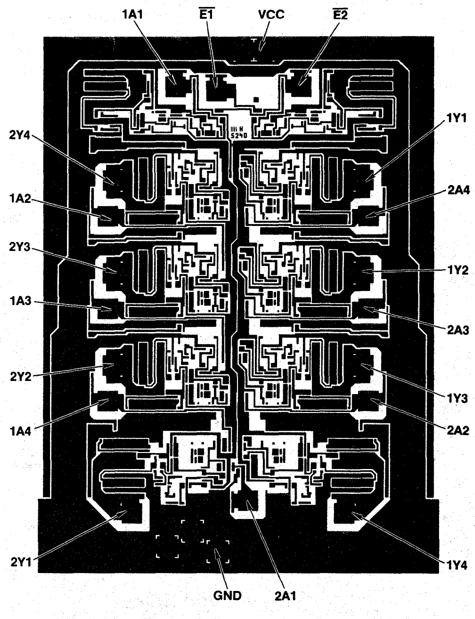


Die Configurations

'S210

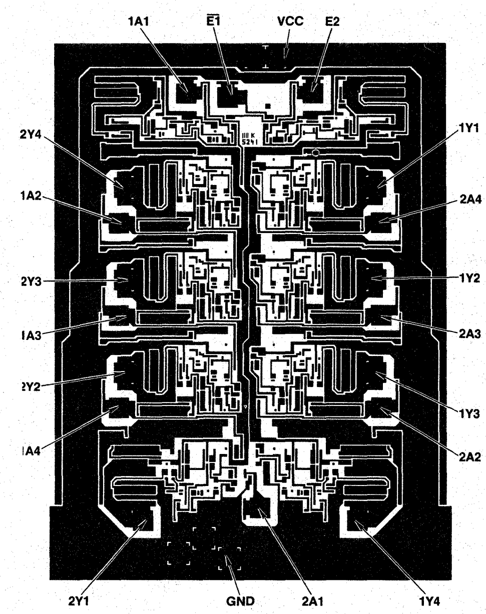


'S240

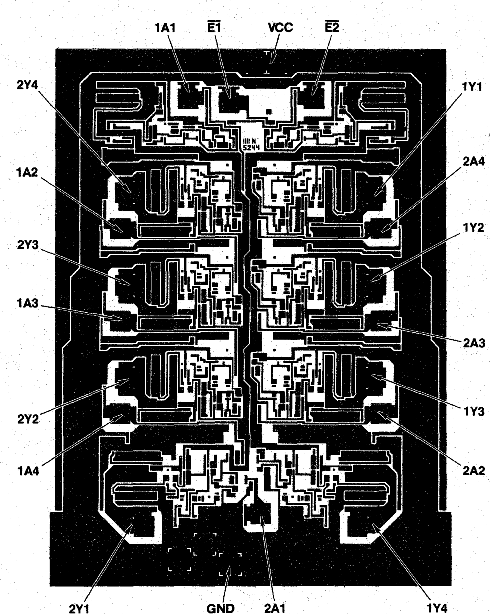


Die Size: 68x100 mil^2

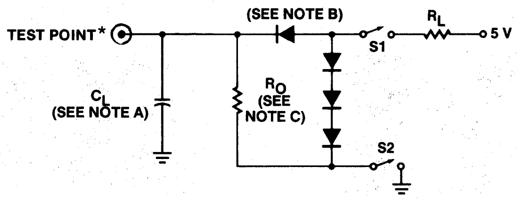
'S241



'S244

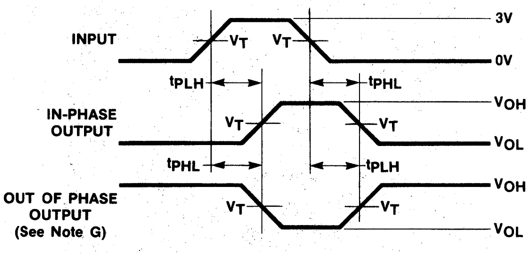


Test Load

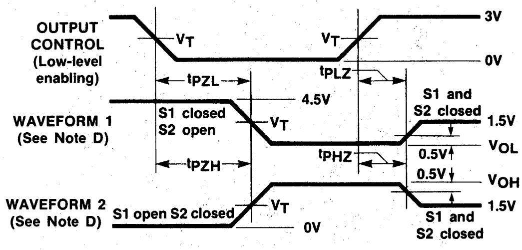


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay



Enable and Disable

NOTES:
- A. C_L includes probe and jig capacitance.
- B. All diodes are 1N916 or 1N3064.
- C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.
  For Series 54/74LS, R_O = 5K, V_T = 1.3 V.
- D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
  Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
  For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
  For Series 54/74LS and PALs, $t_R \leq 15$ ns. $t_F \leq 6$ ns.
- G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

8-Bit Buffers with Schmitt Trigger Inputs

SN54/74LS310 SN54/74S310
SN54/74LS340 SN54/74S340
SN54/74LS341 SN54/74S341
SN54/74LS344 SN54/74S344

Features

- Schmitt-trigger inputs guarantee high noise margin
- Three-state outputs drive bus lines
- Typical input and output capacitance ≤10 pf
- Low-current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '310 and '341 types combine multiplexer and driver functions
- Pin-compatible with SN54/74S210/240/1/4 and SN54/74LS210/240/1/4; can be direct replacement in systems with noise problems

Ordering Information

PART NUMBER	PKG*	TEMP	ENABLE	POLARITY	POWER
SN54LS310	J,F	mil	High-Low	Invert	LS
SN74LS310	N,J	com			
SN54LS340	J,F	mil	Low		
SN74LS340	N,J	com			
SN54LS341	J,F	mil	High-Low	Non-Invert	
SN74LS341	N,J	com			
SN54LS344	J,F	mil	Low		
SN74LS344	N,J	com			
SN54S310	J,F	mil	High-Low	Invert	S
SN74S310	N,J	com			
SN54S340	J,F	mil	Low		
SN74S340	N,J	com			
SN54S341	J,F	mil	High-Low	Non-Invert	
SN74S341	N,J	com			
SN54S344	J,F	mil	Low		
SN74S344	N,J	com			

Description

In addition to the standard Schottky and low-power Schottky 8-bit buffers, Monolithic Memories provides full hysteresis with a "true" Schmitt-trigger circuit. The improved performance characteristics are designed (1) for the low-power Schottky buffers, to be consistent with the SN54/74LS14 hex Schmitt-trigger inverter, and to guarantee a full 400 mV noise immunity; (2) for the Schottky buffers, to have low propagation delays, and to guarantee a full 500 mV noise immunity. The Schmitt-trigger operation makes these LS/S buffers ideal for bus receivers in a noisy environment.

These 8-bit buffers provide high-speed and high-current interface capability for bus-organized digital systems. The three-state drivers will source a termination to ground (up to 133Ω) or sink a pull-up to V_{CC} as in the popular 220Ω/330Ω computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA I_{IL} for the low-power Schottky buffers and 0.25 mA I_{IL} for the Schottky buffers.

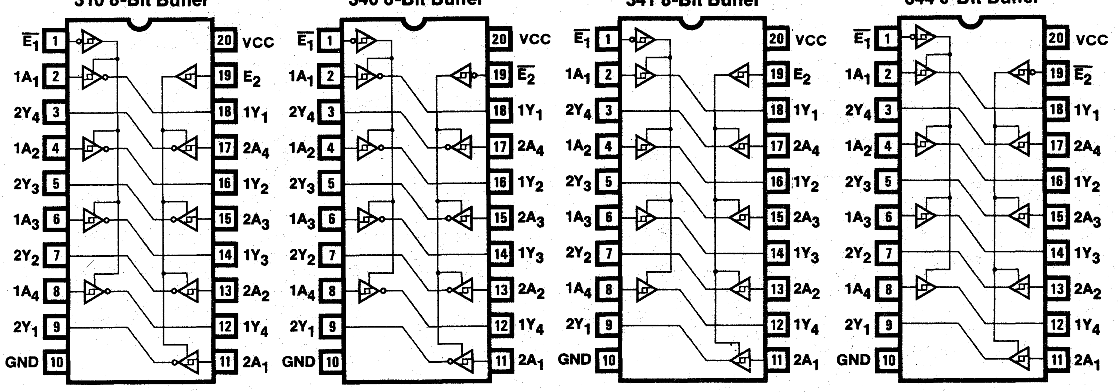
The '340 and '344 provide inverting and non-inverting outputs respectively, with assertive-low enables. The '310 and '341 also provide inverting and non-inverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceiver or multiplexer operation.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

11

Logic Symbols

'310 8-Bit Buffer   '340 8-Bit Buffer   '341 8-Bit Buffer   '344 8-Bit Buffer



*For other package types, please contact your local sales representative.

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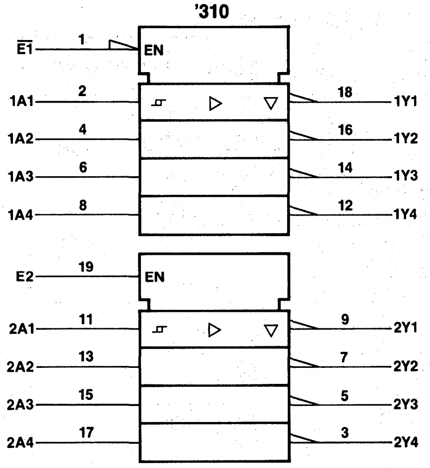
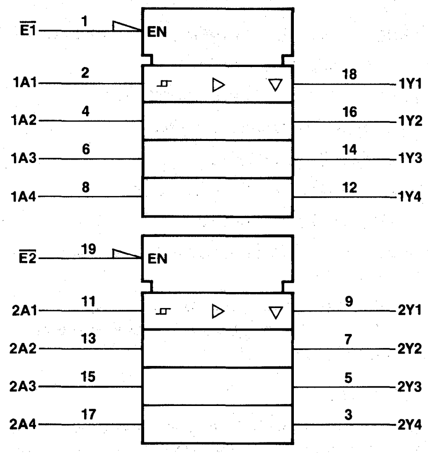
Monolithic Memories

IEEE Symbols

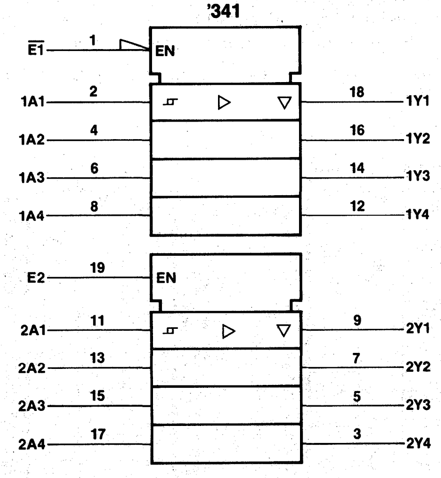
'310



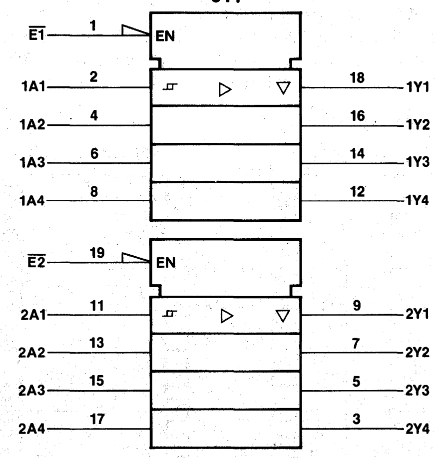
'340



'341



'344



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 7 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{T+}	Positive threshold voltage	Any A*		1.5	1.7	2.0	1.5	1.7	2.0	V
V_{T-}	Negative threshold voltage	Any A*		0.6	0.9	1.1	0.6	0.9	1.1	V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.5			-1.5	V
ΔV_T	Hysteresis (V_{T+}-V_{T-})	Any A*		0.4	0.8		0.4	0.8		V
ΔV_{DB}	Dead band voltage	Any A*		0.4			0.4			V
V_{IL}	Input low voltage	Any E*				0.8			0.8	V
V_{IH}	Input high voltage	Any E*		2.0			2.0			V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.2			-0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V			20				μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7 V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{T+} = 2 V, V_{T-} = 0.6 V	I_{OL} = 12 mA			0.4			0.4	V
			I_{OL} = 24 mA						0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{T+} = 2 V, V_{T-} = 0.6 V	I_{OH} = -3 mA	2.4	3.4		2.4	3.4		V
			I_{OH} = -12 mA	2						
			I_{OH} = -15 mA				2			
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{T+} = 2 V, V_{T-} = 0.6 V	V_O = 0.4 V			-20			-20	μA
I_{OZH}			V_O = 2.7 V			20			20	μA
I_{OS}	Output short-circuit current**	V_{CC} = MAX		-40		-225	-40		-225	mA
I_{CC}	Supply Current — Outputs High	V_{CC} = MAX, Outputs open	'LS310,'LS340		17	27		17	27	mA
			'LS341, 'LS344		18	35		18	35	
	Supply Current — Outputs Low		'LS310, 'LS340		26	44		26	44	
			'LS341, 'LS344		32	46		32	46	
	Supply Current — Outputs Disabled		'LS310, 'LS340		29	50		29	50	
			'LS341, 'LS344		34	54		34	54	

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

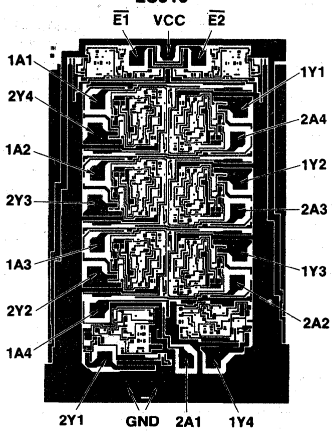
* "A" indicates data input, "E" indicates enable input.

Switching Characteristics $V_{CC} = 5\ V$, $T_A = 25°C$

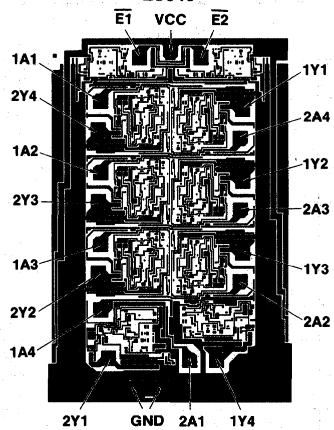
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)		'LS310, 'LS340 MIN	'LS310, 'LS340 TYP	'LS310, 'LS340 MAX	'LS341, 'LS344 MIN	'LS341, 'LS344 TYP	'LS341, 'LS344 MAX	UNIT
t_{PLH}	Data to Output delay	$C_L = 45\ pF$	$R_L = 667\ \Omega$		19	25		19	25	ns
t_{PHL}					19	25		19	25	ns
t_{PZL}	Output Enable delay				32	40		25	40	ns
t_{PZH}					23	35		24	35	ns
t_{PLZ}	Output Disable delay	$C_L = 5\ pF$	$R_L = 667\ \Omega$		18	30		21	30	ns
t_{PHZ}					15	25		18	25	ns

Die Configurations

'LS310

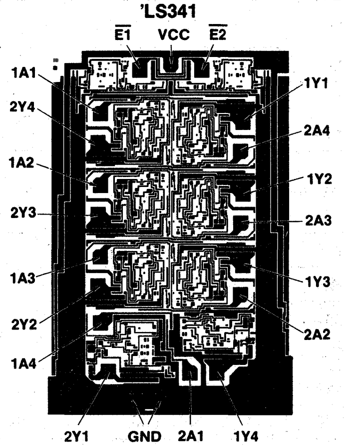


'LS340

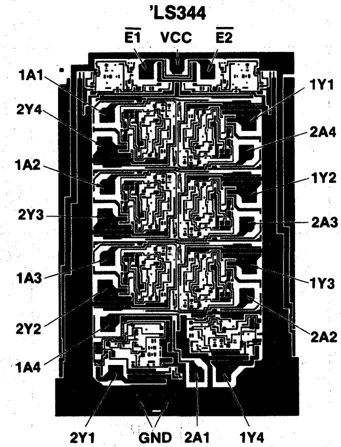


Die Size: 85x146 mil^2

'LS341



'LS344



Absolute Maximum Ratings

Supply voltage V_{CC}	7.0 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature	−65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{T+}	Positive threshold voltage	Any A*		1.5	1.8	2.05	1.6	1.8	2.0	V
V_{T-}	Negative threshold voltage	Any A*		0.8	1.1	1.35	0.8	1.1	1.3	V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.2			−1.2	V
ΔV_T	Hysteresis (V_{T+}−V_{T-})	Any A*		0.5	0.7		0.5	0.7		V
ΔV_{DB}	Dead band voltage	Any A*		0.15			0.3			V
V_{IL}	Input low voltage	Any E*				0.8			0.8	V
V_{IH}	Input high voltage	Any E*		2.0			2.0			V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5 V			−0.25			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{T+} = 2 V, V_{T-} = 0.8 V	I_{OL} = 48 mA			0.55				V
			I_{OL} = 64 mA						0.55	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{T+} = 2 V, V_{T-} = 0.8 V	I_{OH} = −1 mA				2.7			V
			I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
			I_{OH} = −12 mA	2						
			I_{OH} = −15 mA				2			
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IH} = 2.0 V, V_{IL} = 0.8 V	V_O = 0.5 V			−50			−50	μA
I_{OZH}			V_O = 2.7 V			50			50	μA
I_{OS}	Output short-circuit current**	V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply Current — Outputs High	V_{CC} = MAX, Outputs open	'S310,'S340		50	80		50	80	mA
			'S341, 'S344		80	130		80	130	
	Supply Current — Outputs Low		'S310, 'S340		110	155		100	155	
			'S341, 'S344		130	180		130	185	
	Supply Current — Outputs Disabled		'S310, 'S340		135	180		135	180	
			'S341, 'S344		155	180		150	200	

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

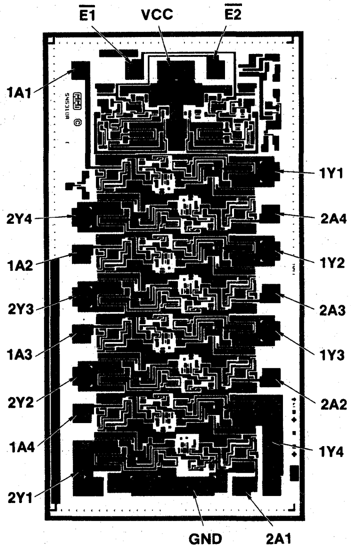
* "A" indicates data input, "E" indicates enable input.

Switching Characteristics $V_{CC} = 5\ V$, $T_A = 25°C$

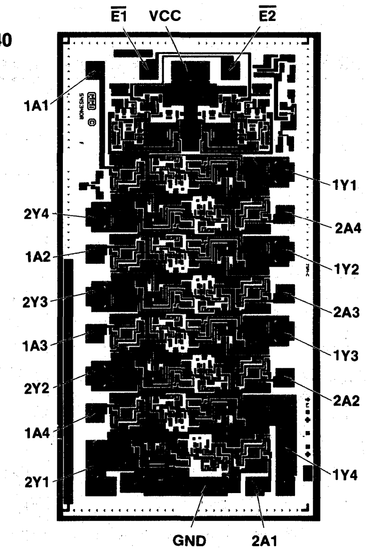
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S310, 'S340 MIN	'S310, 'S340 TYP	'S310, 'S340 MAX	'S341, 'S344 MIN	'S341, 'S344 TYP	'S341, 'S344 MAX	UNIT
t_{PLH}	Data to Output delay	$C_L = 50\ pF$ $R_L = 90\Omega$		11	15		16	22	ns
t_{PHL}				16	22		10	15	ns
t_{PZL}	Output Enable delay			8	15		10	15	ns
t_{PZH}				6	12		7	12	ns
t_{PLZ}	Output Disable delay	$C_L = 5\ pF$ $R_L = 90\Omega$		10	15		10	15	ns
t_{PHZ}				7	12		7	12	ns

Die Configurations

'S310

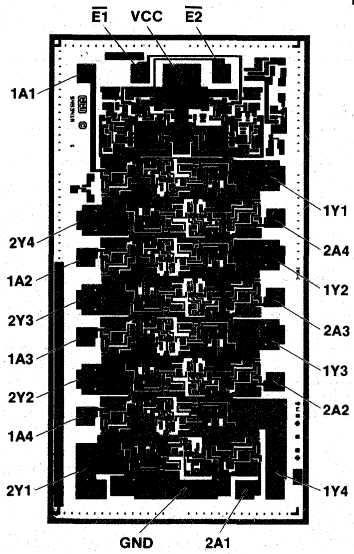


'S340

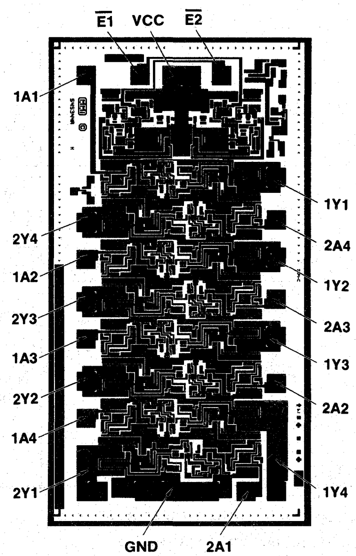


Die Size: 62x121 mil^2

'S341



'S344



Function Tables

'310

$\overline{E_1}$	E_2	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Enabled (Inverting)
H	L	Z	Z
L	H	Enabled (Inverting)	Enabled (Inverting)
L	L	Enabled (Inverting)	Z

'340

$\overline{E_1}$	$\overline{E_2}$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Z
H	L	Z	Enabled (Inverting)
L	H	Enabled (Inverting)	Z
L	L	Enabled (Inverting)	Enabled (Inverting)

'341

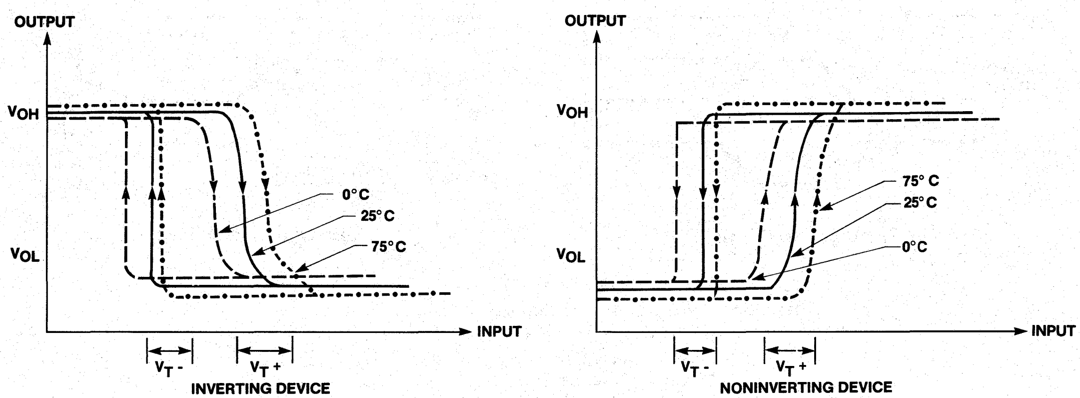
$\overline{E_1}$	E_2	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Enabled
H	L	Z	Z
L	H	Enabled	Enabled
L	L	Enabled	Z

'344

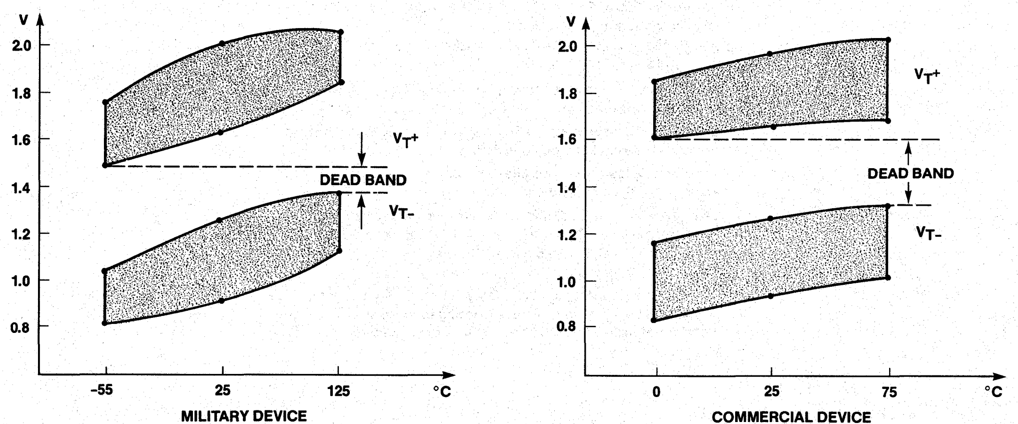
$\overline{E_1}$	$\overline{E_2}$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Z
H	L	Z	Enabled
L	H	Enabled	Z
L	L	Enabled	Enabled

Z ≡ High impedance (output off).

INPUT VS OUTPUT VOLTAGE TRANSFER CHARACTERISTIC

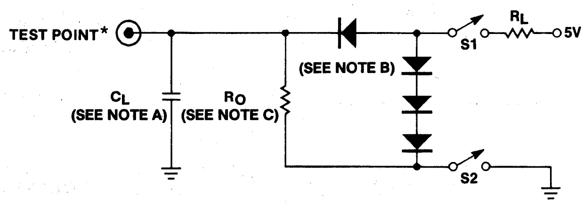


THRESHOLD VOLTAGE VS OPERATING TEMPERATURE



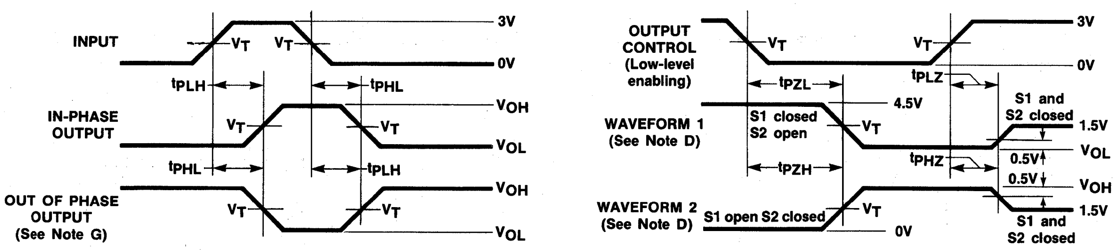
* Dead Band: The hysteresis is guaranteed at any operating temperature and voltage.

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay

Enable and Disable

NOTES:
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54/74S310/340/341/344 R_O = 5K, $V_T = V_{T+}$ = 1.8 V for low-to-high input transition.
For Series 54/74S310/340/341/344 R_O = 5K, $V_T = V_{T-}$ = 1.1 V for high-to-low input transition.
For Series 54/74LS310/340/341/344 R_O = 5K, $V_T = V_{T+}$ = 1.7 V for low-to-high input transition.
For Series 54/74L310/340/341/344 R_O = 5K, $V_T = V_{T-}$ = 0.9 V for high-to-low input transition.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{OUT} = 50\Omega$ and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ ns. $t_F \leq 6$ ns.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed. (Propagation delays are measured from the inputs crossing V_{T+}, V_{T-} to the outputs crossing V_T)

8-Bit Buffer Transceiver

SN54/74LS245

FOR MORE DETAIL SEE SECTION 12

Features/Benefits

- **Three-state outputs drive bus lines**
- **Low current PNP inputs reduce loading**
- **Symmetric -- equal driving capability in each direction**
- **20-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Ideal for microprocessor interface**
- **Pin-compatible with SN54/74LS645 -- improved speed, I_{IL} and I_{OZL} specifications**

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS245	J,L,W	Mil	Non-invert	LS
SN74LS245	N,J	Com		

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus, or from the B bus to the A bus depending upon the logic level at the direction control ($\overline{DIR}$) input. The enable input (E) can be used to disable the device, so that the buses are affectively isolated.

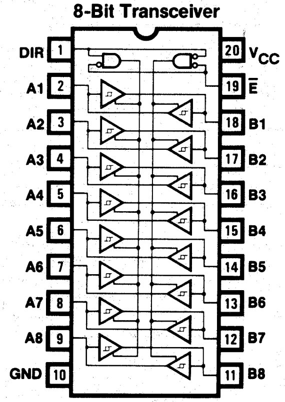
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

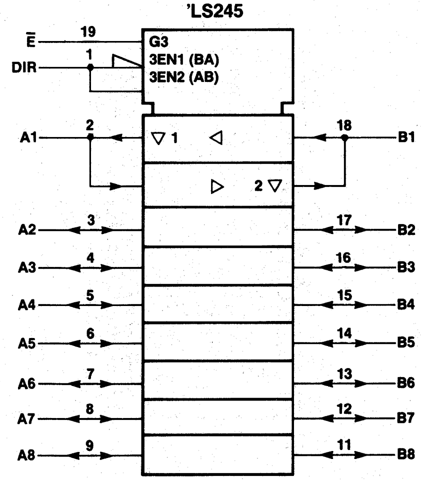
Logic Symbol

8-Bit Transceiver



IEEE Symbol

'LS245



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Monolithic Memories

8-Bit Buffer Transceiver
SN54/74LS645 SN74LS645-1

FOR MORE DETAIL SEE SECTION 12

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric — equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- SN74LS645-1 rated at I_{OL} = 48 mA

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS645	J,L,W	Mil	Non-invert	LS
SN74LS645	N,J	Com		
SN74LS645-1	J	Com		

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\bar{E}$) can be used to disable the device so that the buses are effectively isolated.

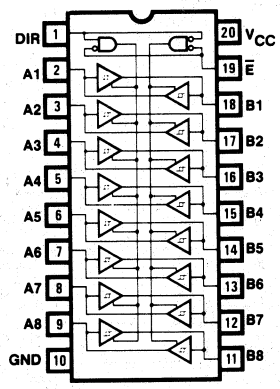
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Table

ENABLE $\bar{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

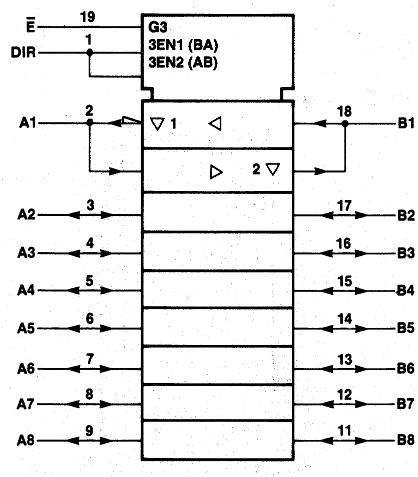
Logic Symbol

8-Bit Transceiver



IEEE Symbol

'LS645/645-1



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Monolithic Memories

8-Bit Registers with Master Reset or Clock Enable

SN54/74LS273 SN54/74LS377
SN54/74S273 SN54/74S377

Features/Benefits

- 20-Pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprogram instruction registers
- Ideal for microprogram interface
- Suitable for pipeline data registers
- Useful in timing, sequencing, and control circuits
- Three '273s may replace four '174s
- Three '377s may replace four '378s/Am25S07s

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	CONTROL OPTION	POWER
SN54LS273 SN74LS273	J,F,L,W N,J,L	Mil Com	Non-invert	Master Reset	LS
SN54LS377 SN74LS377	J,F,L,W N,J,L	Mil Com		Clock Enable	
SN54S273 SN74S273	J,F,L,W N,J,L	Mil Com	Non-invert	Master Reset	S
SN54S377 SN74S377	J,F,L,W N,J,L	Mil Com		Clock Enable	

Description

These 8-bit registers contain eight D-type flip-flops, they feature very low I_{CC} (17 mA typical) on the low-power Schottky devices and very-high-speed operation on the Schottky devices. The '273 register is loaded on the rising edge of the clock (CK) and asynchronously cleared whenever the master reset line, $\overline{MR}$, is low. The '377 register is loaded on the rising edge of the clock provided that the clock enable line, $\overline{CK\ EN}$, is low.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Table '273

INPUTS			OUTPUT
$\overline{MR}$	CLOCK	DATA	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L or H or ↓	X	Q_0

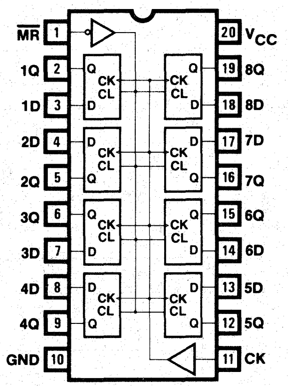
Function Table '377

INPUTS			OUTPUT
$\overline{CK\ EN}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L or H or ↓	X	Q_0

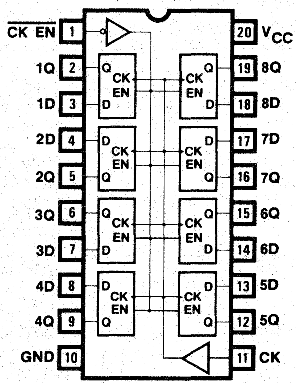
11

Logic Symbols

8-Bit Register
with Master Reset
'273



8-Bit Register
with Clock Enable
'377



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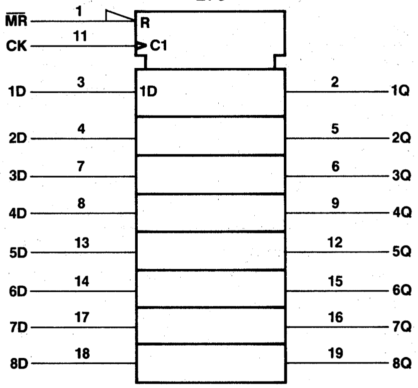
Monolithic Memories

Absolute Maximum Ratings

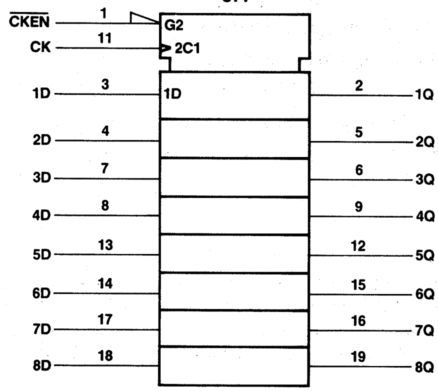
Supply voltage V_{CC} .... 7 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature range .... -65° C to + 150° C

IEEE Symbols

'273



'377



Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface, Test Load/Waveforms)	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature			-55		125	0		75	°C
t_W	Width of clock	High-t_{WH}	1	20			20			ns
		Low-t_{WL}								
t_{WMR}	Width of Master Reset ('LS273 only)	Low-t_{WMRL}	2	20			20			ns
t_{rec}		$\overline{MR}$ to CK ('S273 only)	2	25 ↑			25 ↑			ns
t_{su}	Setup time	Data input to CK	3	20 ↑			20 ↑			ns
		Low $\overline{CK\ EN}$ to CK ('LS377 only)	4	25 ↑			25 ↑			
		High $\overline{CK\ EN}$ to CK ('LS377 only)		10 ↑			10 ↑			
t_h	Hold time	Data input	3	5 ↑			5 ↑			ns
		Low $\overline{CK\ EN}$ to CK ('LS377 only)	4	5 ↑			5 ↑			
		High $\overline{CK\ EN}$ to CK ('LS377 only)		5 ↑			5 ↑			

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition. ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7 V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −400μA	2.5	3.4		2.7	3.4		V
I_{OS}	Output short-circuit current*	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current †	V_{CC} = MAX	LS273		17	27		17	27	mA
		Outputs open	LS377		17	28		17	28	

* Note more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

† I_{CC} is measured after first a momentary ground, and then 4.5 V is applied to clock, while the following other input conditions are held:
(a) for the 'LS273 — 4.5 V on all data and master-reset inputs.
(b) for the 'LS377 — ground on all data and clock-enable inputs.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	LS273 MIN	LS273 TYP	LS273 MAX	LS377 MIN	LS377 TYP	LS377 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15 pF R_L = 2KΩ	30	40		35	40		MHz
t_{PLH}	Clock to Output delay				27			27	ns
t_{PHL}					27			27	ns
t_{PHL}	Master Reset to output delay ('LS273 only)				27				ns

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Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature range .... -65° C to + 150° C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface, Test Load/Waveforms)	FIGURE	MILITARY MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
V_{CC}	Supply voltage			4.5 5 5.5	4.75 5 5.25	V
T_A	Operating free-air temperature			-55 125	0 75	°C
t_W	Width of clock	High-t_{WH} Low-t_{WL}	1	7	7	ns
t_{WMR}	Width of Master Reset ('S273 only)	Low-t_{WMRL}	2	10	10	ns
t_{rec}		$\overline{MR}$ to CK ('S273 only)	2	7↑	7↑	ns
t_{su}	Setup time	Data input to CK	3	5↑	5↑	ns
		Low $\overline{CK\ EN}$ to CK ('S377 only)	4	9↑	9↑	
		High $\overline{CK\ EN}$ to CK ('S377 only)	4	9↑	9↑	
t_h	Hold time	Data input	3	3↑	3↑	ns ns
		Low $\overline{CK\ EN}$ to CK ('S377 only)	4	3↑	3↑	
		High $\overline{CK\ EN}$ to CK ('S377 only)		0↑	0↑	

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
V_{IL}	Low-level input voltage			0.8	0.8	V
V_{IH}	High-level input voltage			2	2	V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA	-1.2	-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5 V	-250	-250	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V	50	50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V	1	1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = 2 V	I_{OL} = 20 mA	0.5	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = 2 V	I_{OH} = -1mA	2.5 3.4	2.7 3.4	V
I_{OS}	Output short-circuit current*	V_{CC} = MAX		-40 -100	-40 -100	mA
I_{CC}	Supply current †	V_{CC} = MAX	'S273	150	150	mA
		Outputs open	'S377	160	160	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S273 MIN	'S273 TYP	'S273 MAX	'S377 MIN	'S377 TYP	'S377 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15 pF R_L = 280Ω	75	110		75	110		MHz
t_{PLH}	Clock to Output delay			6	15		6	15	ns
t_{PHL}				9	15		9	15	ns
t_{PHL}	Master Reset to output delay ('S273 only)			13	22				ns

11

CLOCK PULSE WIDTH AND CLOCK TO OUTPUT DELAYS

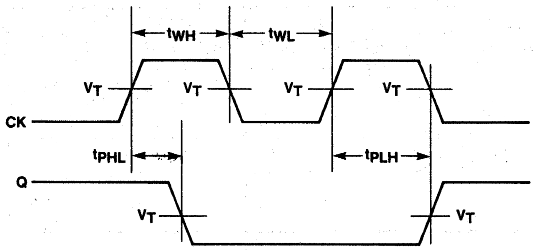


Figure 1

DATA SET-UP AND HOLD TIMES

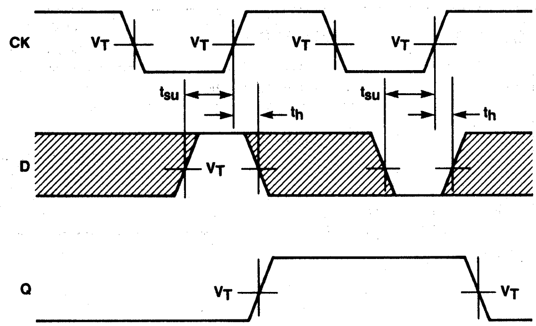


Figure 3

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME FOR 'S273

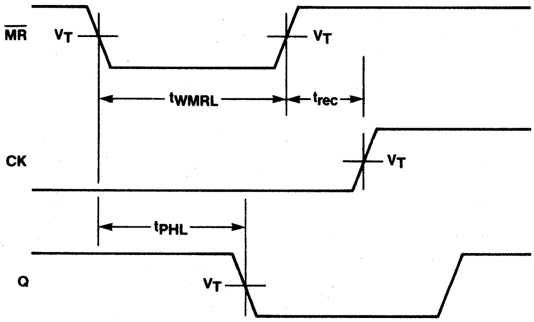


Figure 2

CLOCK ENABLE SETUP AND HOLD TIMES FOR 'S377

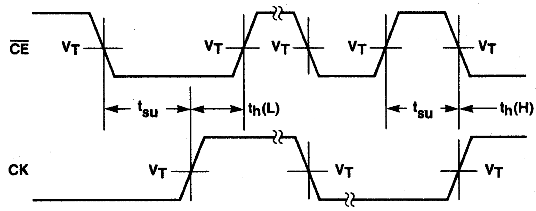
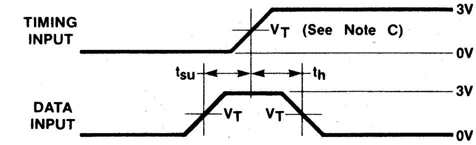
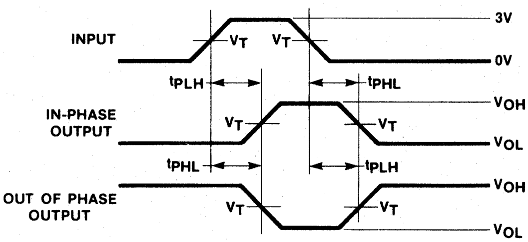


Figure 4

Test Waveforms

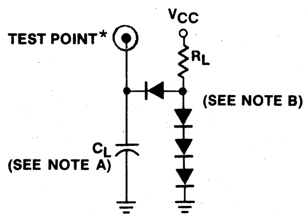


SETUP AND HOLD



PROPAGATION DELAY

Test Load



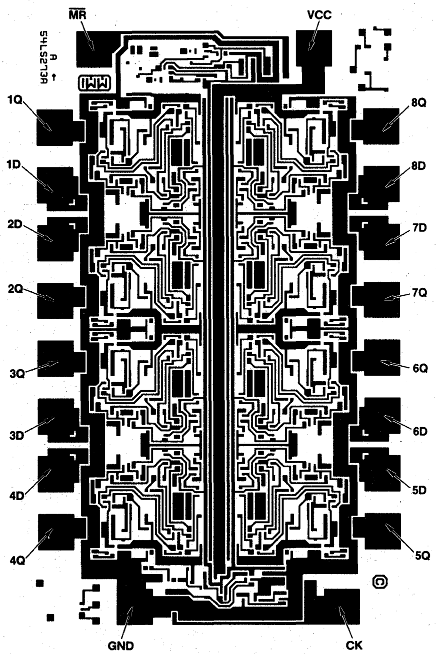
* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

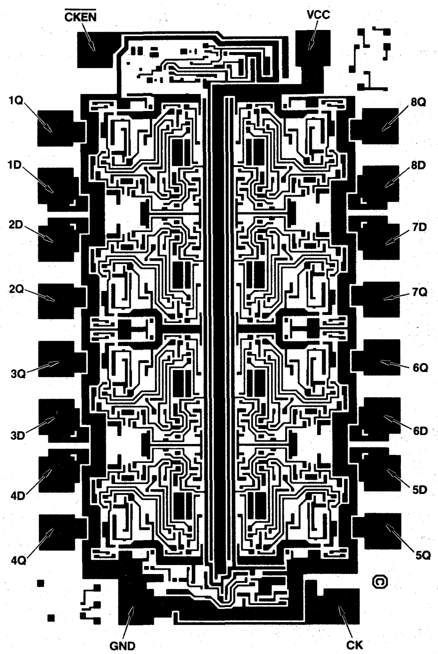
NOTES:
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54/74S, V_T = 1.5 V.
For Series 54/74LS, V_T = 1.3 V.
D. In the examples above the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.

Die Configurations

'LS273

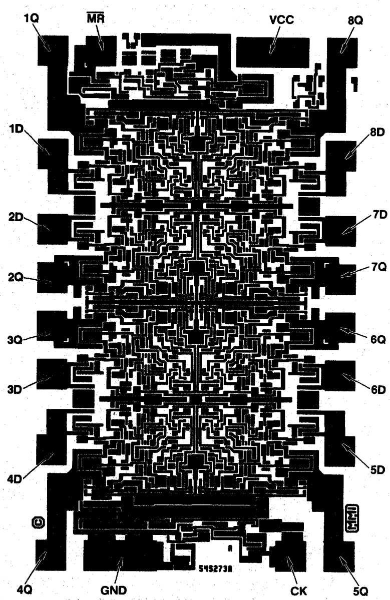


'LS377

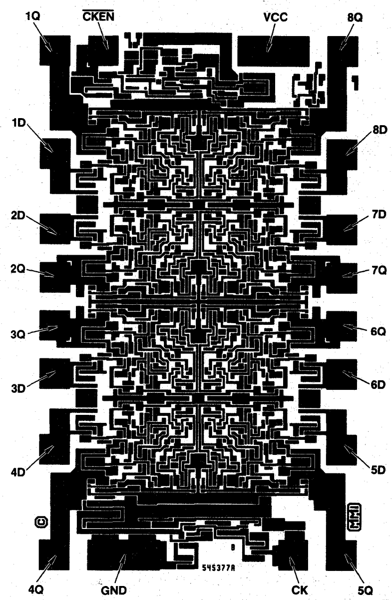


Die Size: 58x93 mil^2

'S273



'S377



Die Size: 56x87 mil^2

8-Bit Latches, 8-Bit Registers

SN54/74LS373 SN54/74S373
SN54/74LS374 SN54/74S374

Features/Benefits

- **Three-state outputs drive bus lines**
- **20-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Hysteresis improves noise margin**
- **Low current PNP inputs reduce loading**
- **Ideal for microprocessor interface**

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS373	J,L,W	Mil	Non-invert	Latch	LS
SN74LS373	N,J	Com			
SN54LS374	J,L,W	Mil		Register	
SN74LS374	N,J	Com			
SN54S373	J,L,W	Mil		Latch	S
SN74S373	N,J	Com			
SN54S374	J,L,W	Mil		Register	
SN74S374	N,J	Com			

Description

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Tables

'373 8-Bit Latch

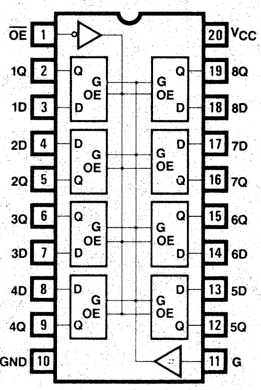
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'374 8-Bit Register

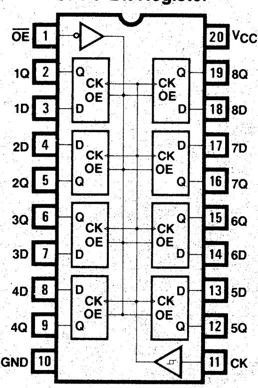
$\overline{OE}$	CK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L or H or $\downarrow$	X	Q_0
H	X	X	Z

Logic Symbols

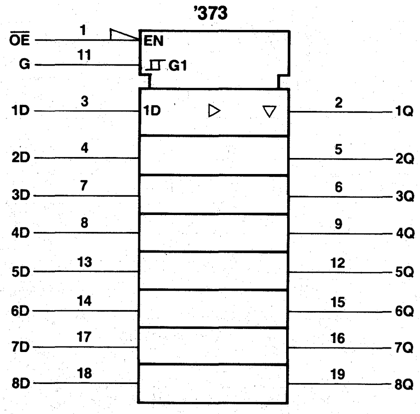
'373 8-Bit Latch

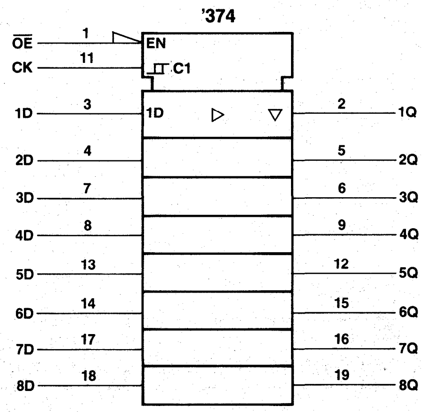


'374 8-Bit Register



IEEE Symbols





11

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 7 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150° C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		-55		125	0		75	°C
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{su}	Setup time	LS373	5↓			5↓			ns
		LS374	20↑			20↑			
t_h	Hold time	LS373	20↓			20↓			ns
		LS374	0↑			0↑			

↑↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-1.5			-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			-0.4			-0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = -1mA	2.4	3.4					V
			I_{OH} = -2.6mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			-20			-20	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		-30		-130	-30		-130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	LS373		24	40		24	40	mA
			LS374		27	40		27	40	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Charcteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	LS373 MIN	LS373 TYP	LS373 MAX	LS374 MIN	LS374 TYP	LS374 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 45pF R_L = 667Ω				35	50		MHz
t_{PLH}	Data to Output delay			12	18				ns
t_{PHL}				12	18				ns
t_{PLH}	Clock/Gate to output delay			20	30		15	28	ns
t_{PHL}				18	30		19	28	ns
t_{PZL}	Output Enable delay			25	36		21	28	ns
t_{PZH}				15	28		20	28	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		14	25	ns
t_{PHZ}				12	20		12	20	ns

Absolute Maximum Ratings

Supply voltage V_{CC}	7.0 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature	−65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125	0		75	°C
t_w	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Setup time	S373	0↓			0↓			ns
		S374	5↑			5↑			
t_h	Hold time	S373	10↓			10↓			ns
		S374	2↑			2↑			

↑↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−0.25			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2mA	2.4	3.4					V
			I_{OH} = −6.5mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50			−50	μA
I_{OZH}			V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S373		105	160		105	160	mA
			S374		90	140		90	140	

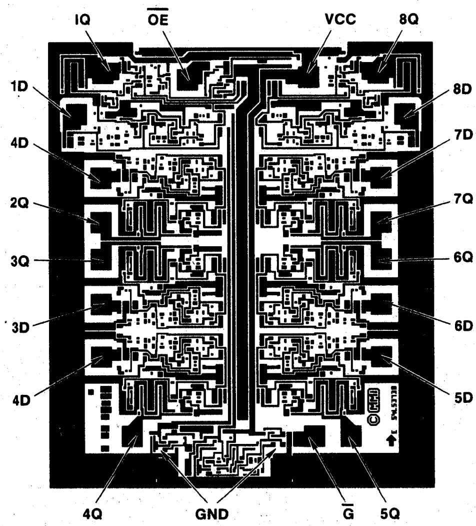
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

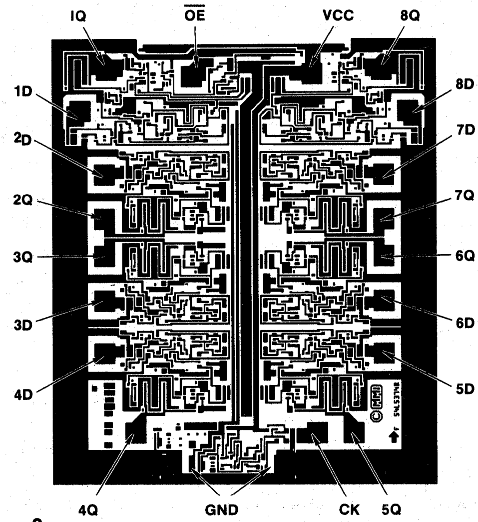
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	S373 MIN	S373 TYP	S373 MAX	S374 MIN	S374 TYP	S374 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			7	12				ns
t_{PHL}				7	12				ns
t_{PLH}	Clock/Gate to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output Enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns

Die Configurations

'LS373

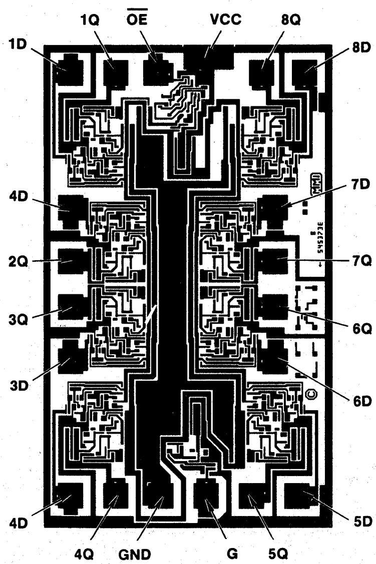


'LS374

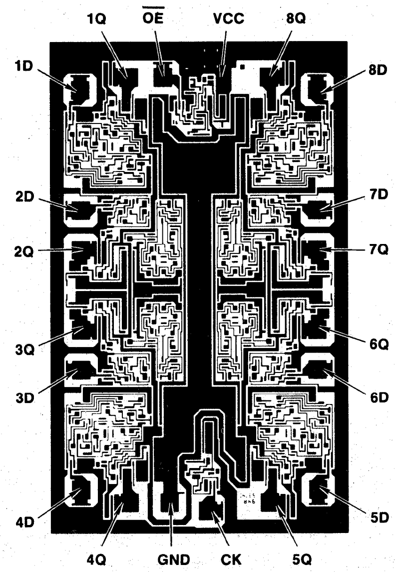


Die Size: 76x87 mil^2

'S533

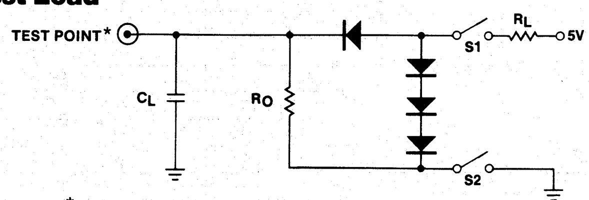


'S534



Die Size: 63x100 mil^2

Test Load

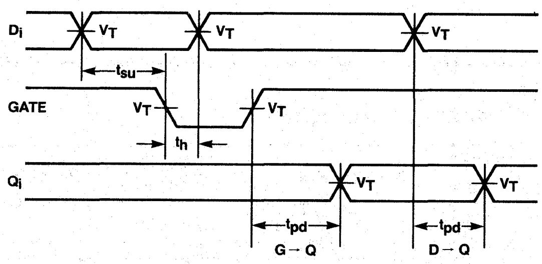


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

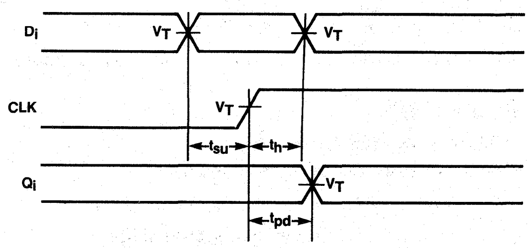
FOR THE LS373/374
R_O = 5KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

FOR THE LS373/374
R_O = 1KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

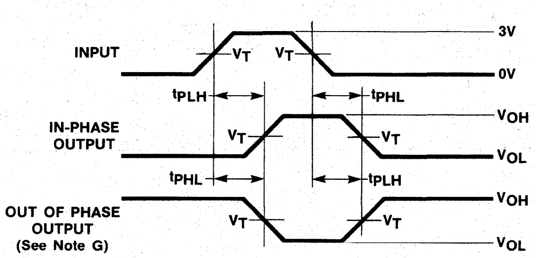
'373 Timing Diagrams



'374 Timing Diagrams

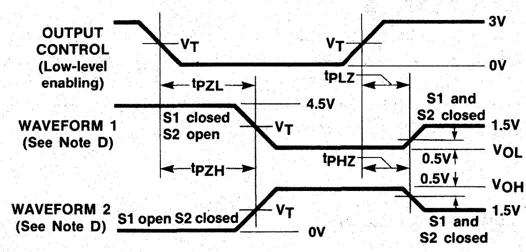


Test Waveforms



V_T = 1.5 V

Propagation Delay



Enable and Disable

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.
For Series 54/74LS, R_O = 5K, V_T = 1.3 V.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, $t_R \leq$ 2.5 ns, $t_F \leq$ 2.5 ns.
For Series 54/74LS and PALs, $t_R \leq$ 15 ns. $t_F \leq$ 6 ns.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

11

8-Bit Register With Clock Enable and Open-Collector Outputs
SN54/74S383

Features

- 20-Pin SKINNYDIP® Saves Space
- 8-bit data path matches byte boundaries
- Only available TTL open-collector-output register
- Ideal for certain microprocessor system buses
- Suitable for pipeline data registers
- Excellent for multiple, physically-separated connections to buses in microprocessor-based systems
- Wired-OR or wired-AND logic with outputs

Description

This 8-bit register contains 8 D-type flip-flops and features very fast switching. The 'S383 register is loaded on the rising edge of the clock provided that the clock enable line, $\overline{\text{CK EN}}$, is low. Like other 8-bit interface devices, the 'S383 is packaged in the popular 20-pin SKINNYDIP.

Ordering Information

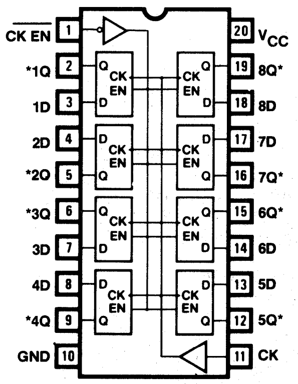
PART NUMBER	PKG	TEMP	POLAR-ITY	CONTROL OPTIONS	POWER
SN54S383	J,L,W	Mil	Non-	Clock	S
SN74S383	N,J	Com	invert	Enable	

Function Table 'S383

INPUTS			OUTPUT
$\overline{\text{CK EN}}$	CLOCK	DATA	Q
H	X	X	Q_0
L	$\uparrow$	H	H
L	$\uparrow$	L	L
X	L or H or $\downarrow$	X	Q_0

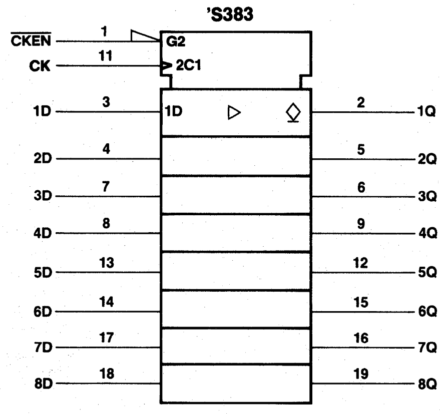
Logic Symbol

8-Bit Register with Clock Enable and Open-Collector Outputs
'S383



*Indicates Open-Collector Output

IEEE Symbol



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface, Test Load/Waveforms)	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature			−55		125	0		75	V
t_W	Width of clock	High-t_{WH}	1	7			7			ns
		Low-t_{WL}								
t_{su}	Setup time	Data input to CK	2	5↑			5↑			ns
		Low $\overline{\text{CK EN}}$ to CK		9↑			9↑			
		High $\overline{\text{CK EN}}$ to CK		9↑			9↑			
t_h	Hold time	Data input	2	3↑			3↑			ns
		Low $\overline{\text{CK EN}}$ to CK		3↑			3↑			
		High $\overline{\text{CK EN}}$ to CK		0↑			0↑			

↑↓ The arrow indicates the transition of the clock/enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			-250			-250	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = 2V	I_{OL} = 24mA			0.5			0.5	V
I_{OH}	High-level output current	V_{CC} = MIN V_{IL} = MAX V_{IH} = 2V	V_{OH} = 5.5 V			250			250	μA
I_{CC}	Supply current	V_{CC} = MAX Outputs open	Outputs HIGH			160			160	mA
			Outputs LOW			160			160	

Switching Characteristics V_{CC} = 5 V, T_A = 25° C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S383 MIN	'S383 TYP	'S383 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15 pF R_L = 280Ω	75	110		MHz
t_{PLH}	Clock to output delay			10	17	ns
t_{PHL}				14	22	ns

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Test Waveforms

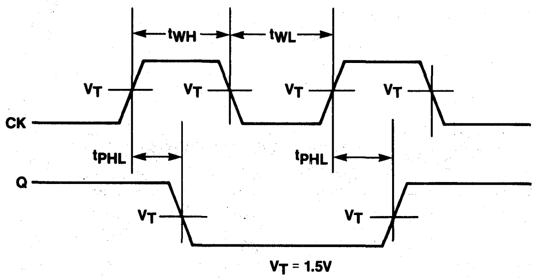


Figure 1

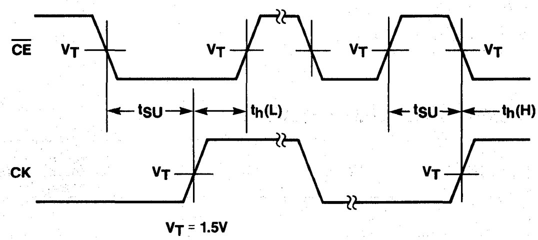
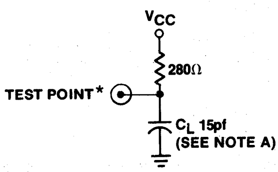


Figure 2

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

A. Includes probe and jig capacitance.

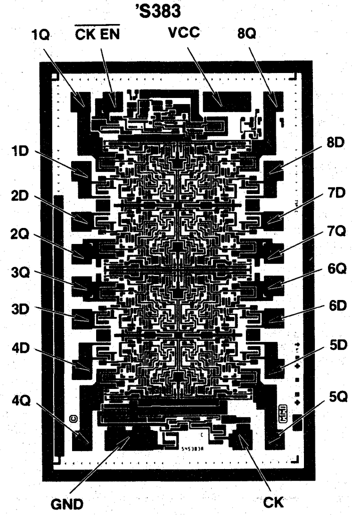
B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

C. All input pulses are aupplied by generators having the following characteristics: PRR
$\leq$1 MHz, Z_{out} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.

Die Configuration

Die Size: 58x93 mil^2

'S383

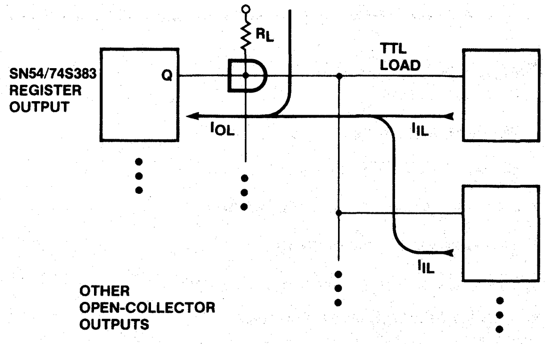


Open Collector Bus Application Information For Determination of R_L For Wired-And Applications

1. **CALCULATE R_L(Min):**

$$R_L(\text{Min}) = \frac{V_{CC} - V_{OL}(\text{Max})}{I_{OL} - (\text{TOTAL } I_{IL})}$$

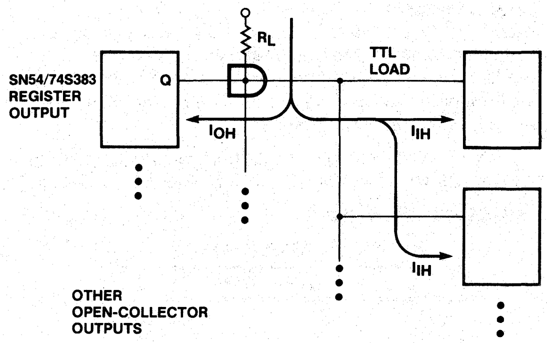
where I_{OL} = 24 mA at
V_{OL}(Max) = 0.5 V



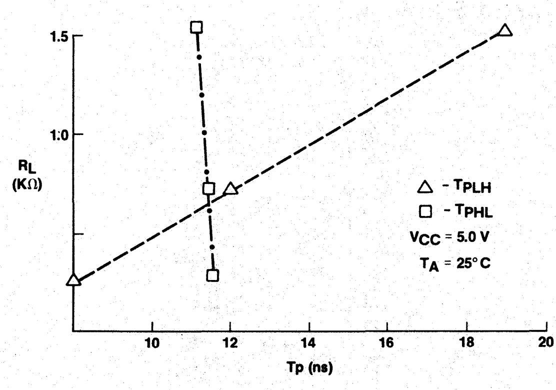
2. **CALCULATE R_L(Max):**

$$R_L(\text{Max}) = \frac{V_{CC} - V_{OH}(\text{Min})}{(\text{TOTAL } I_{OH} + \text{TOTAL } I_{IH})}$$

where I_{OH} = 250 μA at
V_{OH}(Min) = 2.5V



3. **SELECT** a value for R_L in the range of R_L(Min) to R_L(Max), based on power consumption and speed requirements:



R_L vs. Tp FOR SN54/74S383

8-Bit Latches, 8-Bit Registers with Inverting Outputs

SN54/74LS533 SN54/74S533
SN54/74LS534 SN54/74S534

Features/Benefits

- Inverting outputs
- Three-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN54/74LS373/4 or SN54/74S373/4 — can be direct replacement when bus polarity must be changed

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
54LS533 74LS533	J,W,L N,J	Mil Com	Invert	Latch	LS
54LS534 74LS534	J,W,L N,J	Mil Com		Register	
54S533 74S533	J,W,L N,J	Mil Com		Latch	S
54S534 74S534	J,W,L N,J	Mil Com		Register	

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides inverting outputs instead of non-inverting outputs. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-bit slice to an assertive-low bus.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Tables

'533 8-Bit Latch (Inverting)

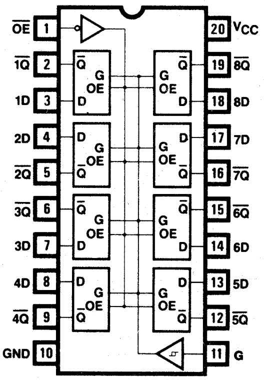
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'534 8-Bit Register (Inverting)

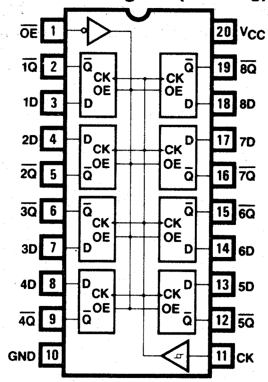
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	H
L	↑	L	L
L	L or H or ↓	X	Q_0
H	X	X	Z

Logic Symbols

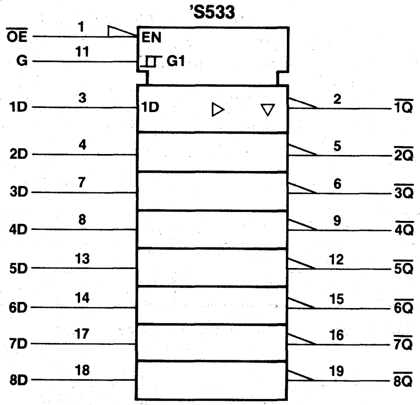
'533 8-Bit Latch (Inverting)

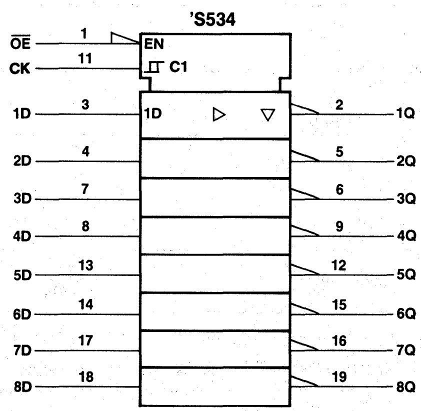


'533 8-Bit Register (Inverting)



IEEE Symbols





Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 7 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125	0		75	°C
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{su}	Setup time	LS533	3↓			3↓			ns
		LS534	20↑			20↑			
t_h	Hold time	LS533	10↓			10↓			ns
		LS534	0↑			0↑			

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1mA	2.4	3.4					V
			I_{OH} = −2.6mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V						−20	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	LS533		36	48		36	48	mA
			LS534		27	48		27	48	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	LS533 MIN	LS533 TYP	LS533 MAX	LS534 MIN	LS534 TYP	LS534 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 45pF R_L = 667Ω				35	50		MHz
t_{PLH}	Data to Output delay			17	25				ns
t_{PHL}				12	25				ns
t_{PLH}	Clock/Gate to output delay			20	35		19	30	ns
t_{PHL}				18	35		15	30	ns
t_{PZL}	Output Enable delay			25	36		21	30	ns
t_{PZH}				17	30		20	30	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		18	29		18	29	ns
t_{PHZ}				16	24		16	24	ns

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		-55		125	0		75	°C
t_w	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Setup time	S533	0↓			0↓			ns
		S534	5↑			5↑			
t_h	Hold time	S533	10↓			10↓			ns
		S534	5↑			5↑			

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA			-1.2			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			-0.25			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = -2mA	2.4	3.4					V
			I_{OH} = -6.5mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			-50			-50	μA
I_{OZH}			V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		-40		-100	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S533		105	160		105	160	mA
			S534		90	140		90	140	

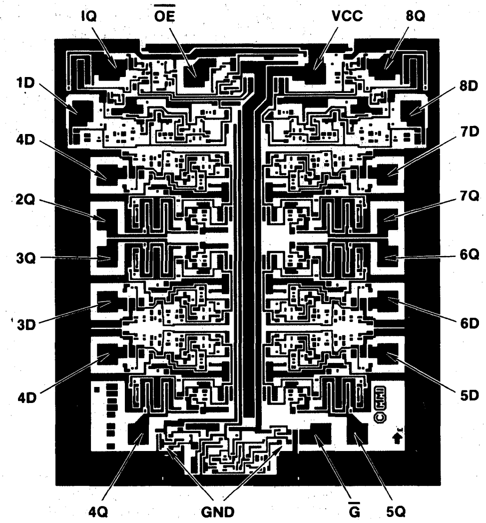
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

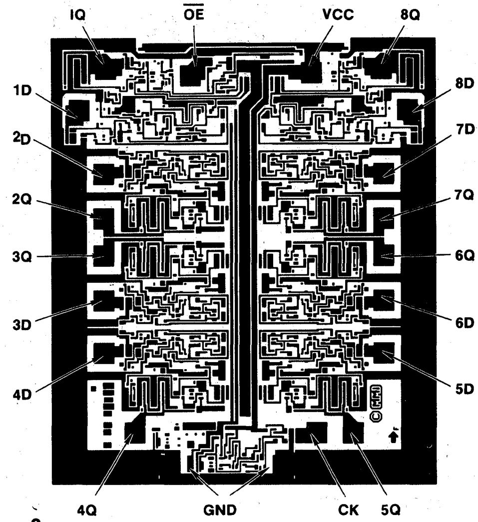
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	S533 MIN	S533 TYP	S533 MAX	S534 MIN	S534 TYP	S534 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Gate to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns

Die Configurations

'LS533

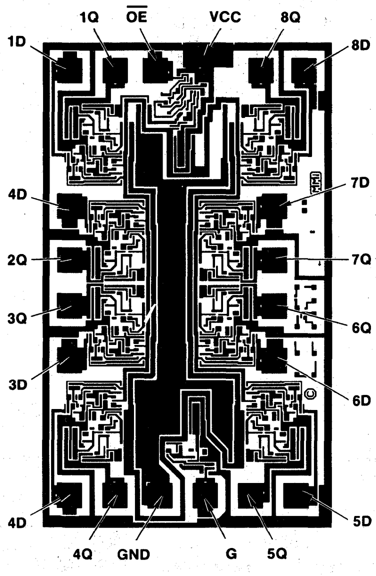


'LS534

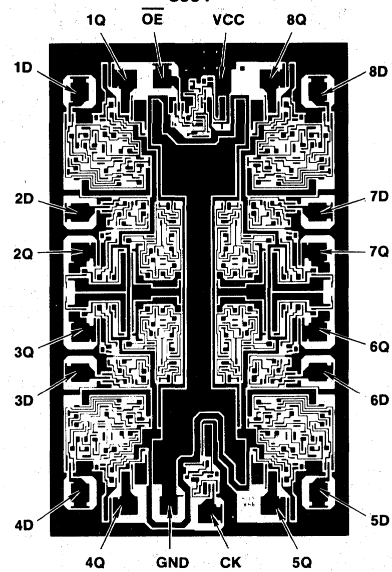


Die Size: 76x87 mil^2

'S533

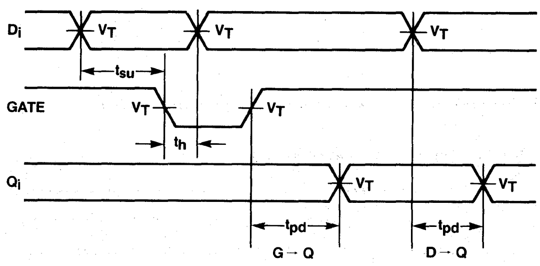


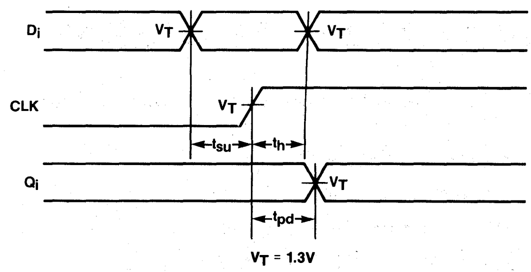
'S534

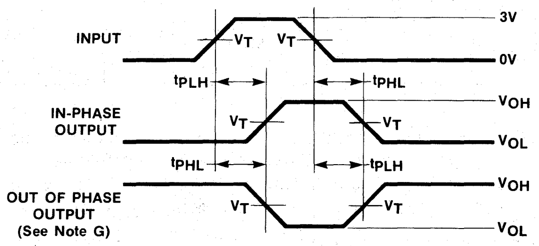


Die Size: 63x100 mil^2

Test Waveforms

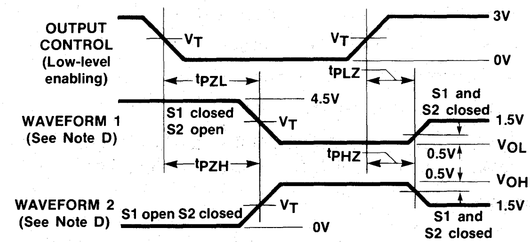






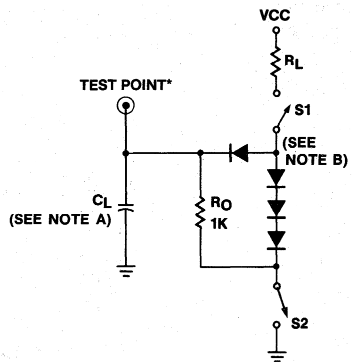
Propagation Delay

VT = 1.3 V



Enable and Disable

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

NOTES:
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.
For Series 54/74LS, R_O = 5K, V_T = 1.3 V.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ ns. $t_F \leq 6$ ns.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

8-Bit Latch, 8-Bit Register with 32 mA Outputs

SN74S531 SN74S532

Features/Benefits

- High drive capability (I_{OL} = 32 mA)
- Three-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN74S373/4 — can be a direct replacement when high drive capability is required

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32-mA requirements with the SN54/74365A/366A/367A/368A hex buffers.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S531	N,J	com	Non-invert	Latch	S
SN74S532	N,J	com		Register	

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the rising edge of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Function Tables

'S531 8-Bit Latch

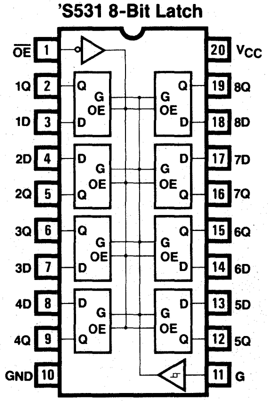
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'S532 8-Bit Register

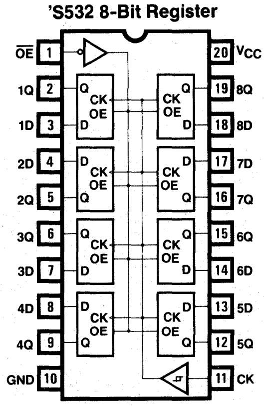
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L or H or ↓	X	Q_0
H	X	X	Z

Logic Symbols

'S531 8-Bit Latch

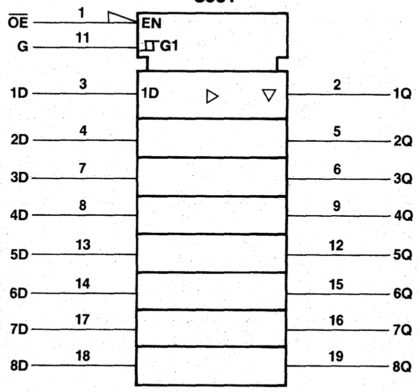


'S532 8-Bit Register

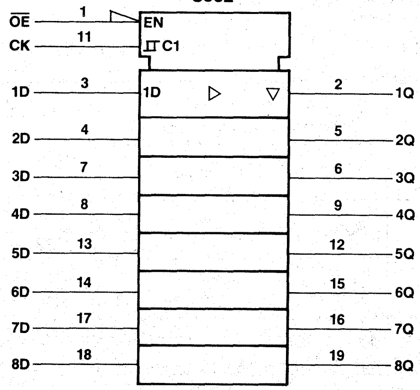


IEEE Symbols

'S531

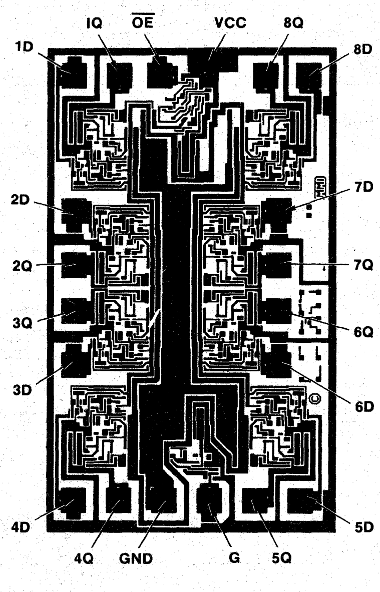


'S532



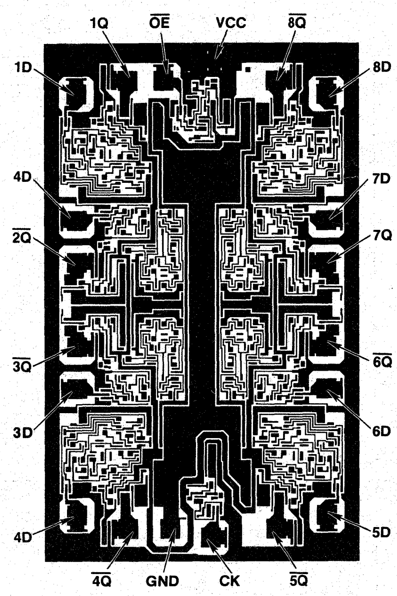
Die Configurations

'S531



Die Size: 63x100 mil^2

'S532



Die Size: 66x106 mil^2

11

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... –65° to +150° C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Width of Clock/Enable	High	6	6		ns
		Low	7.3	7.3		
t_{su}	Setup time	S531	0↓	0↓		ns
		S532	5↑	5↑		
t_h	Hold time	S531	10↓	10↓		ns
		S532	2↑	2↑		

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

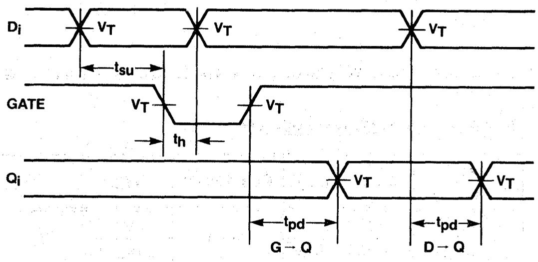
SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = –18mA			–1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = –6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			–50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX,		–40		–100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S531		105	160	mA
			S532		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

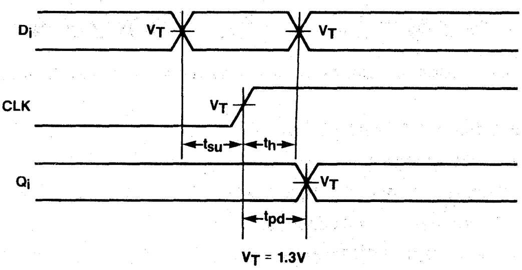
Switching Characteristics V_{CC} = 5 V, T_A = 25° C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	S531 MIN	S531 TYP	S531 MAX	S532 MIN	S532 TYP	S532 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			7	12				ns
t_{PHL}				7	12				ns
t_{PLH}	Clock/Gate to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output Enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns

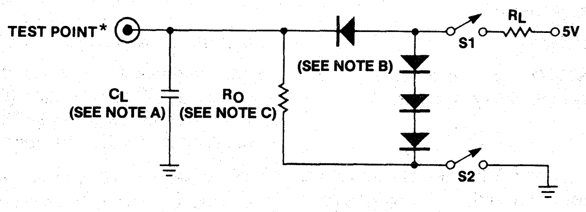
'S531 Timing Diagrams



'S532 Timing Diagrams

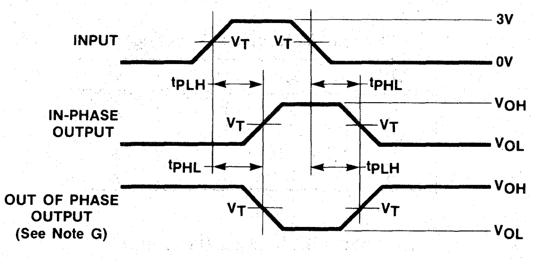


Test Load



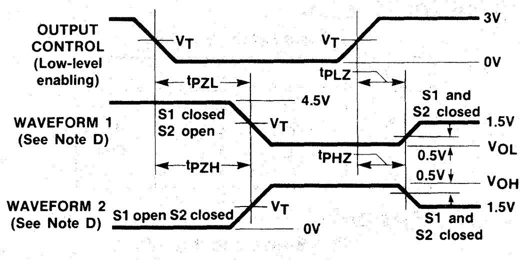
* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay

$V_T = 1.3\ V$



Enable and Disable

NOTES:
- A. C_L includes probe and jig capacitance.
- B. All diodes are 1N916 or 1N3064.
- C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.
- D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

  Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- F. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_{OUT} = 50Ω and:
  For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
  For Series 54/74LS and PALs, $t_R \leq 15$ ns. $t_F \leq 6$ ns.
- G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

11

8-Bit Latch, 8-Bit Register with Inverting, 32 mA Outputs

SN74S535 SN74S536

Features/Benefits

- **Inverting outputs**
- **High-drive capability (I_{OL} = 32 mA)**
- **Three-state outputs drive bus lines**
- **20-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Hysteresis improves noise margin**
- **Low current PNP inputs reduce loading**
- **Ideal for microprocessor interface**
- **Pin-compatible with SN74S533/4 — can be a direct replacement when high-drive capability is required**

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA; also, inverting outputs instead of the standard noninverting outputs.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32-mA requirements with the SN54/74365/366/367/368 hex buffers. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-bit slice to an assertive low.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the rising edge of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S535	N,J	Com	Invert	Latch	S
SN74S536	N,J	Com		Register	

Function Tables

'S535 8-Bit Latch (Inverting)

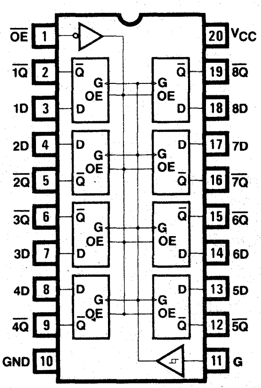
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'S536 8-Bit Register (Inverting)

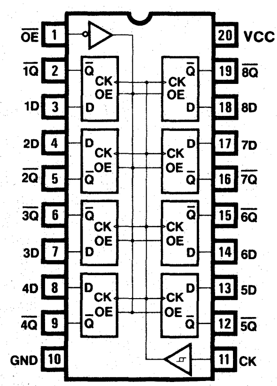
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L or H or ↓	X	Q_0
H	X	X	Z

Logic Symbols

'S535 8-Bit Latch (Inverting)



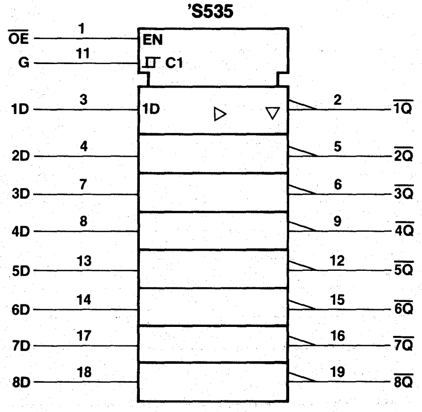
'S536 8-Bit Register (Inverting)



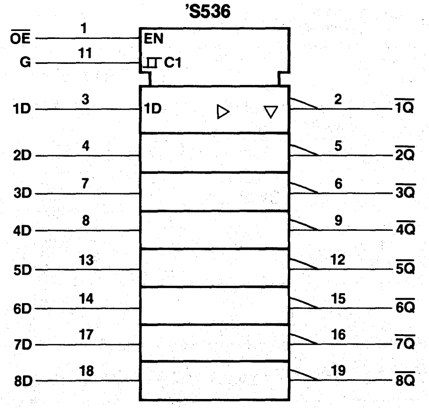
TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

IEEE Symbols

'S535

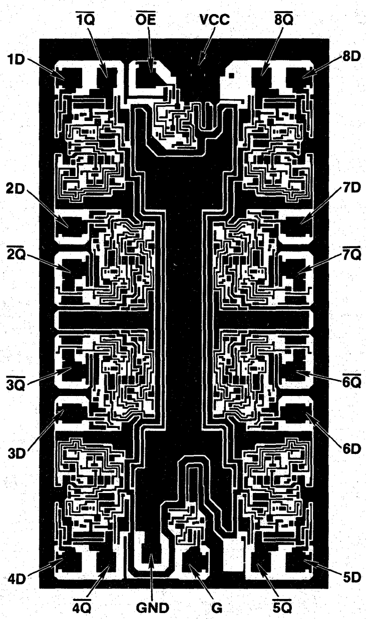


'S536



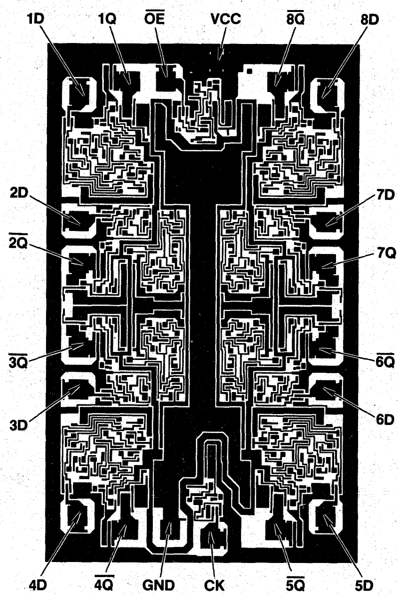
Die Configurations

'S535



Die Size: 61x112 mil^2

'S536



Die Size: 66x106 mil^2

11

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Width of Clock/Enable	High	6	6		ns
		Low	7.3	7.3		
t_{su}	Setup time	S535	0↓	0↓		ns
		S536	5↑	5↑		
t_h	Hold time	S535	10↓	10↓		ns
		S536	5↑	2↑		

Electrical Maximum Ratings Over Operating Conditions

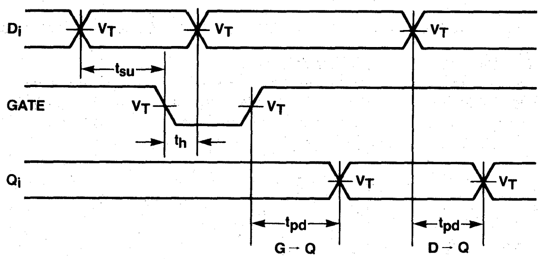
SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MAX V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	V_O = 0.5V			−50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current *	V_{CC}		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX Outputs open	S535		105	160	mA
			S536		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

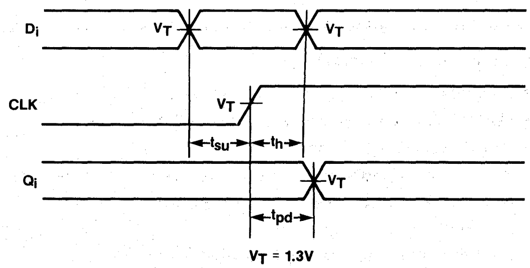
Switching Charcteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	S535 MIN	S535 TYP	S535 MAX	S536 MIN	S536 TYP	S536 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Enable to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns

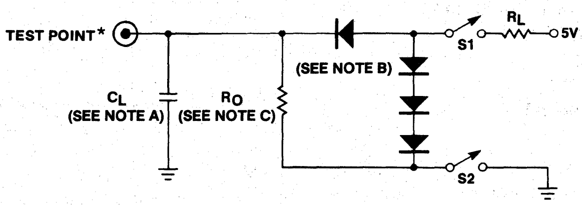
'S535 Timing Diagrams



'S536 Timing Diagrams

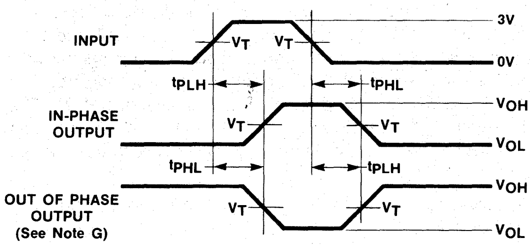


Test Load

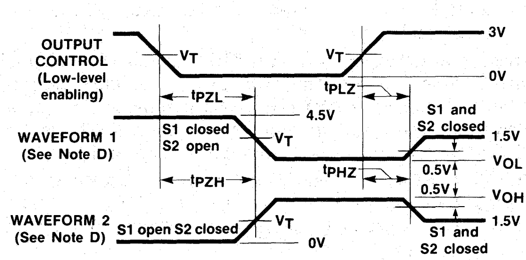


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay



Enable and Disable

V_T = 1.3 V

NOTES:

A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ ns. $t_F \leq 6$ ns.

G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

8-Bit Dynamic-RAM Drivers with Three-State Outputs

FOR MORE DETAIL SEE SECTION 8

SN54/74S700/-1 SN54/74S730/-1
SN54/74S731/-1 SN54/74S734/-1

Features/Benefits:

- **Provides MOS voltage levels for 16 K and 64 K D-RAMs**
- **Undershoot of low-going output is less than -0.5 V**
- **Large capacitive drive capability**
- **Symmetric rise and fall times due to balanced output impedance**
- **Glitch-free outputs at power-up and power-down**
- **20-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **'S730/734 are exact replacement for the Am2965/66**
- **'S700/730/731/734 are pin-compatible with 'S210/240/241/244, and can replace them in many applications**
- **'S700-1/730-1/731-1/734-1 have a larger resistor in the output stage for better undershoot protection**
- **Commercial devices are specified at V_{CC} ±10%.**

Ordering Information

PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54S700/-1	J,W,L	Mil	High-Low	Invert	S
SN74S700/-1	N,J	Com			
SN54S730/-1	J,W,L	Mil	Low		
SN74S730/-1	N,J	Com			
SN54S731/-1	J,W,L	Mil	High-Low	Non-Invert	
SN74S731/-1	N,J	Com			
SN54S734/-1	J,W,L	Mil	Low		
SN74S734/-1	N,J	Com			

Description:

The 'S700, 'S730, 'S731, and 'S734 are buffers that can drive multiple address and control lines of MOS dynamic RAMs. The 'S700 and 'S730 are inverting drivers and the 'S731 and 'S734 are non-inverting drivers. The 'S700/731 are pin-compatible with the 'S210/241 and have complementary enables. The 'S730 is pin-compatible with the 'S240 and an exact replacement for the Am2965. The 'S734 is pin-compatible with the 'S244 and an exact replacement for the Am2966.

These devices have been designed with an additional internal resistor in the lower output driver transistor circuit, unlike regular 8-bit buffers. This resistor serves two purposes: it causes a slower fall time for a high-to-low transition, and it limits the undershoot without the use of an external series resistor.

The 'S700, 'S730, 'S731, and 'S734 have been designed to drive the highly-capacitive input lines of dynamic RAMs. The drivers provide a guaranteed V_{OH} of V_{CC} - 1.15 volts, limit undershoot to 0.5V, and exhibit a rise time symmetrical to their fall time by having balanced outputs. These features enhance dynamic RAM performance.

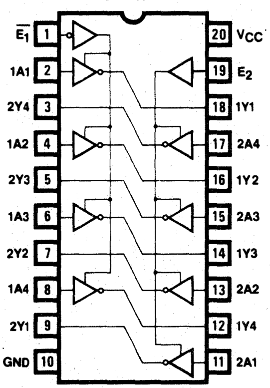
For a better-controlled undershoot for lightly capacitive-loaded circuits the 'S700-1, 'S730-1, 'S731-1 and 'S734-1 provide a larger resistor in the lower output stage. Also an improved undershoot volatge of -0.3 V is provided in the 'S700-1 series.

A typical fully-loaded-board dynamic-RAM array consists of 4 banks of dynamic-RAM memory. Each bank has its own $\overline{RAS}$ and $\overline{CAS}$, but has identical address lines. The $\overline{RAS}$ and $\overline{CAS}$ inputs to the array can come from one driver, reducing the skew between the $\overline{RAS}$ and $\overline{CAS}$ signals. Also, only one driver is needed to drive eight address lines of a dynamic RAM. The propagation delays are specified for 50pf and 500pf load capacitances, and the commercial-range specifications are extended to V_{CC} ± 10%.

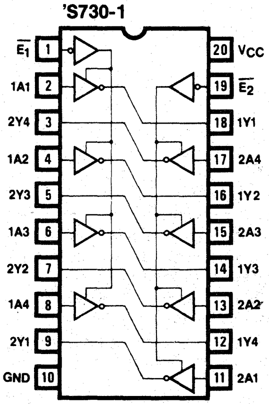
All of the octal devices are packaged in the popular 20-pin SKINNYDIP™.

Logic Symbols

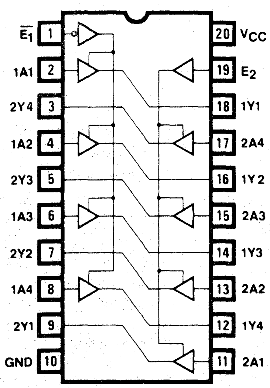
'S700/-1



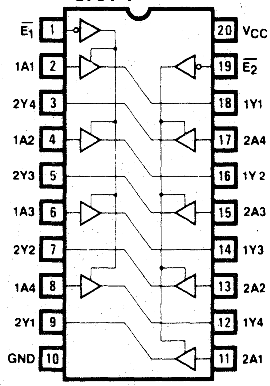
'S730 (Am2965)
'S730-1



'S731/-1



'S734 (Am2966)
'S734-1



TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

8-Bit Diagnostic Register SN54/74S818

FOR MORE DETAIL SEE SECTION 12

Features/Benefits

- High-drive capability: I_{OL} = 32 mA (Com), 24 mA (Mil)
- Assists on-line and off-line system diagnostic testing
- Swaps the content of shadow register and output register
- Shadow register for diagnostic testing
- Edge-triggered "D" registers
- Cascadable for wide control words for use in microprogramming
- Features RAM write-back for writable control store initialization
- PNP inputs for low-input current
- 24-pin SKINNYDIP® saves space

Applications

- Register for microprogram control store
- Status register
- Data register
- Instruction register
- Address register
- Interrupt mask register
- Pipeline register
- General purpose register
- Parallel-serial/Serial-parallel converter

Description

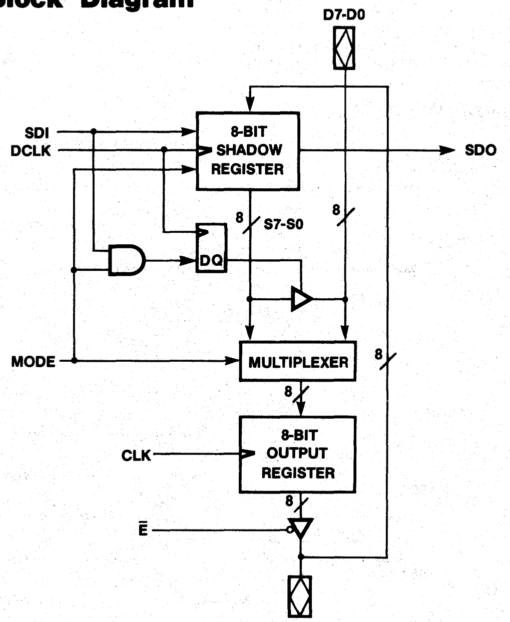
The SN54/74S818 is an 8-bit register with diagnostic features. There is a shadow register in each diagnostic register. Diagnostic data is shifted in serially into the shadow register (S7-S0), while the output register is loaded with either the content of the shadow register or the input data (D7-D0). Moreover, D7-D0 can also be used as the outputs from the shadow register to the data bus, while the outputs (B7-B0) can also be converted to inputs when disabled.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S818	JS,F,L	Mil
SN74S818	NS,JS	Com

NOTE: L package here is L28. The other packages are 24-pin.

Block Diagram



Function Table

INPUTS				OUTPUTS			OPERATION	SEE FIG.
MODE	SDI	CLK	DCLK	B7-B0	S7-S0	SDO		
L	X	↑	*	Bn ← Dn	HOLD	S7	Load output register from input bus	1
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S7	Shift shadow register data	2
L	X	↑	↑	Bn ← Dn	Sn ← Sn-1 S0 ← SDI	S7	Load output register from input bus while shifting shadow register data	1 & 2
H	X	↑	*	Bn ← Sn	HOLD	SDI	Load output register from shadow register	2,3,4
H	L	*	↑	HOLD	Sn ← Bn	SDI	Load shadow register from output bus	3
H	L	↑	↑	Bn ← Sn	Sn ← Bn	SDI	Swap shadow register and output register	
H	H	*	↑	HOLD	HOLD	SDI	Enable D7-D0 as outputs for RAM write-back	4

* Clock must be steady or falling.

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TWX: 910-338-2376
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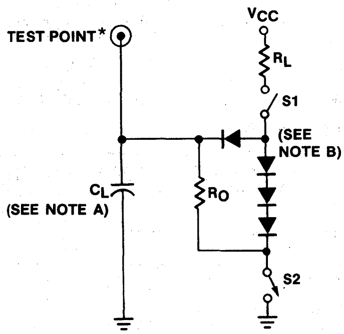
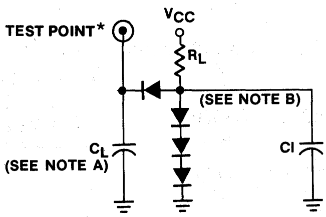
Monolithic Memories

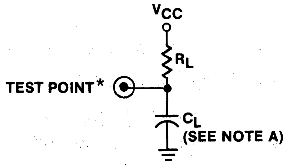
Test Load



LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



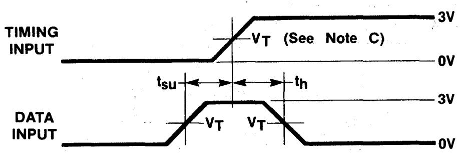
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



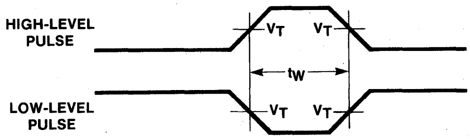
* The "TEST POINT" is driven by the output under test and observed by instrumentation.

LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

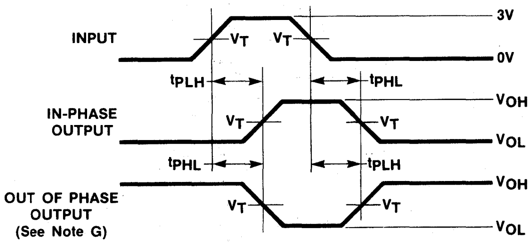
Test Waveforms



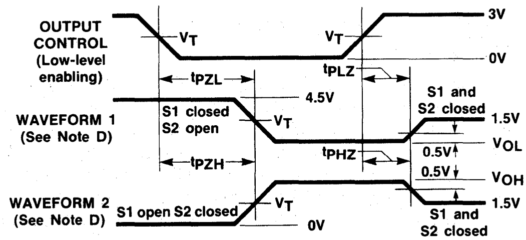
SETUP AND HOLD



PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE

NOTES:
A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54/74S, R_O = 1K, V_T = 1.5V.
For Series 54/74LS, R_O = 5K, V_T = 1.3V excepting 54/74LS310, 340, 341, 344.
For Series 54/74LS310/340/341/344 R_O = 5K, $V_T = V_{T+}$ = 1.7 V for low-to-high input transition.
For Series 54/74LS310/340/341/344 R_O = 5K, $V_T = V_{T-}$ = 0.9 V for low-to-high input transition.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_{out} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ns, $t_F \leq 6$ ns.

G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

Table of Contents

DOUBLE-DENSITY PLUS™ INTERFACE

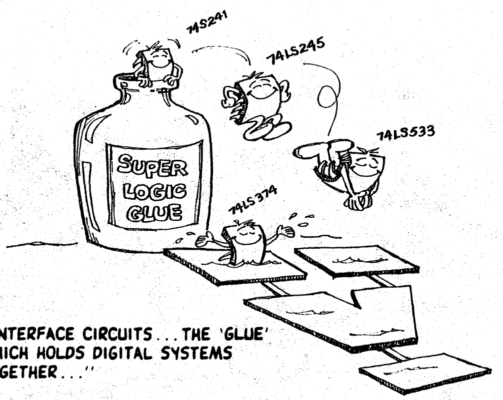
Double-Density PLUS™ Selection Guide

PART NUMBER		PART DESCRIPTION			POWER	POLARITY	OUTPUT	$I_{OL(COM)}$
COMMERCIAL	MILITARY	ARCHITECTURE	FUNCTION	FEATURE				
74LS245	54LS245	Transceiver	Buffer	Direction control	LS	Noninvert	Three-state	24 mA
74LS645	54LS645							
74LS645-1	—							48 mA
74LS546	54LS546		Register	Independent enable controls				32 mA
74LS566	54LS566					Invert		
74LS547	54LS547		Latch			Noninvert		
74LS567	54LS567					Invert		
74LS646	54LS646		Front-loading latch	Direction control		Noninvert		24 mA
74LS647	54LS647						Open-collector	
74LS648	54LS648					Invert	Three-state	
74LS649	54LS649						Open-collector	
74LS651	54LS651			Independent enable controls			Three-state	
74LS652	54LS652					Noninvert		
74LS653	54LS653					Invert	A: Open-collector B: Three-state	
74LS654	54LS654					Noninvert		
74ACT646	54ACT646			Direction control	CMOS		Three-state	12 mA
74ACT648	54ACT648					Invert		
74ACT651	54ACT651			Independent enable controls				
74ACT652	54ACT652					Noninvert		
74LS793	54LS793	Readback	Latch	Readback enable control	LS			24 mA
74LS794	54LS794		Register					
74LS548	54LS548	Two-stage pipeline		Input, Output individual select controls				32 mA
74LS549	54LS549		Latch					
74S818	54S818	Diagnostic	Register	Mode controls	S			

Small But Mighty; New Components Give You More Logic in Less Chips*

Chuck Hastings and Suneel Rajpal

Interface circuits are generally thought of as unglamorous bread-and-butter items. They have the humble role of being the "glue" which holds digital systems together. Contemporary custom-LSI wizards often claim to be on the point of getting rid of all these bothersome little low-complexity circuits, and yet *more* interface circuits are sold with each passing year. According to recent estimates, during 1983 the personal computer industry *alone* consumed one-fourth as many interface circuits as *all* users consumed during 1982. Figure 1 graphically portrays a realistic scenario for interface for the next few years—everything else will shrink, so interface will grab an *increasing* share of board area in the future!



"INTERFACE CIRCUITS... THE 'GLUE' WHICH HOLDS DIGITAL SYSTEMS TOGETHER..."

What this means to you is that, if interface does its part and does some shrinking too, you'll get some *major* shrinkage in your overall system. Interface is low-complexity stuff to start with, and over the years it has stubbornly resisted being shrunk. Nonetheless, today Monolithic Memories offers a broad line of interface parts which arose from commonly-encountered circumstances, and which — where they fit your design — shrink parts count by a factor of 2:1. Unsurprisingly, they are called "Double-Density PLUS Interface." Actually, under optimal conditions certain of these parts can shrink your parts count by as much as 4:1.

Double-Density PLUS™ Interface can do wonders to compress the physical size of your logic. Consider, for example, a simple sychronous cross-connection between two 8-bit microprocessor buses, capable of transferring information in either direction one byte at time. This cross-connection can be implemented using two 'LS374 8-bit noninverting registers, connected "back-to-back" — that is, each 'LS374 has all of its eight outputs tied respectively to the eight inputs of the other one. Together, these two parts total 40 pins and 2 (0.6*1.1) = 2 (0.66) = 1.32 square inches, allowing for 100 mils end clearance and 300 mils side clearance as is common practice in board layout.

"... DOUBLE-DENSITY PLUS™ INTERFACE CAN DO WONDERS TO COMPRESS THE PHYSICAL SIZE OF YOUR LOGIC... "

You may notice that, when these two parts are considered as a functional block, far fewer than 40 pins go to the outside world; there are only the 16 data pins corresponding to the two 8-bit buses, two clock pins, two output-enable pins, and power and ground. Now, since Monolithic Memories also noticed back-to-back 'LS374s as an attractive low-pin-count combination a couple of years ago, today you have the option of replacing both of these 'LS374's with a single 24-pin, 300-mil "SKINNYDIP®" 'LS546, which takes up only (0.6*1.3) = 0.78 square inches of your board — slightly more than half as much board area as the two 'LS374s. To summarize:

DESIGN SOLUTION	BOARD AREA		WIRE ENDS	
	Sq. In.	Normalized	Pin Count	Normalized
Two 'LS374s	1.32	1.00	40	1.00
One 'LS546	0.78	0.59	24	0.60

Table 1. Board Area and Wire Savings Using 'LS546

*Note: This article is a portion of Monolithic Memories Conference Paper CP-112, which may be found in its entirety in the second edition of the *Systems Design Handbook.*

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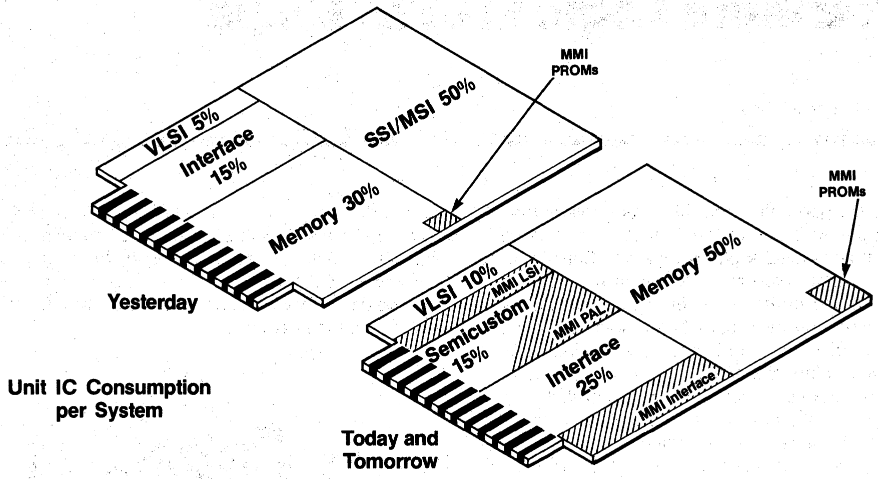


Figure 1. Logic Distribution on a Typical Board

You also pick up some other benefits along the way making this swap. The two registers within the 'LS546 are appreciably faster than the 'LS374s, and also have a higher output drive — 32 mA sinking current instead of 24 mA. The 'LS546 and 'LS566 have clock enables which operate independently for each register. The 'LS546 also has a cleaned-up "structured" pinout with the 8 pins for each data bus together, each bus having its own side of the 24-pin dual-inline package.

The 'LS546 is comprised of two non-inverting edge-triggered registers. If you are dealing with assertive-low buses and need inverting registers, use an 'LS566. If you prefer latches to registers, use either an 'LS547 (non-inverting) or an 'LS567 (inverting). All of these parts have a common "back-to-back" internal architecture, as shown in Figure 2.

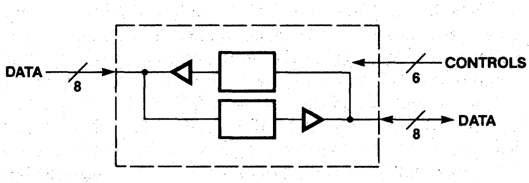
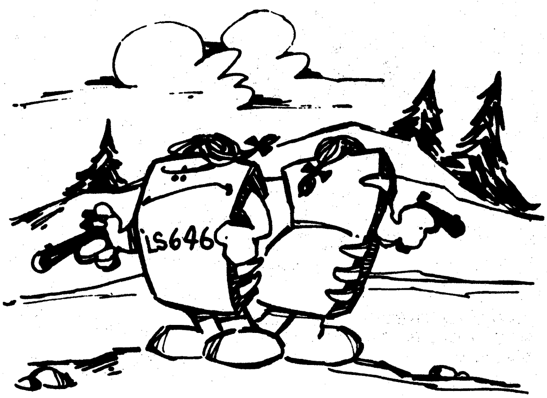


Figure 2. The 546/547/566/567 Block Diagram

Two more families of back-to-back parts also come in the same pinout: the 'LS646/7/8/9 family, and the 'LS651/2/3/4 family. These differ from each other in enable structure; the 'LS646 et. al. have a "direction-control line" so that you can't perform certain operations on both sides of the part simultaneously, whereas the 'LS651 et. al. have generally independent operations on both sides. In each of these families there are two non-inverting parts and two inverting parts; in each case, there is a three-state part and an open-collector part. All of the parts from both families are comprised of "front-loading-latch" individual elements (see



BACK-TO-BACK CONFIGURATION

Figure 3); a front-loading latch is an edge-triggered flipflop in parallel with a buffer, so that the data can be piped through the buffer to reach the output rapidly and then can be *subsequently* recorded in the flipflop. It is also possible, in a front-loading-latch structure, to pipe data temporarily around the flipflop to the output without *ever* recording it in the flipflop. The 'LS646/7/8/9 feature hysteresis on their data inputs as well as on their control inputs, which makes them function well in high-noise environments. The 'LS653/4 are open-collector in one direction, but three-state in the other direction.

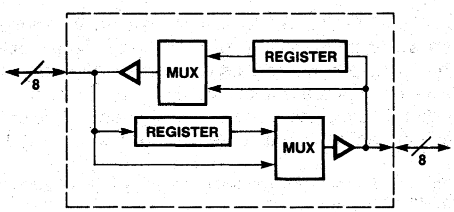


Figure 3. The '646-Series/'651-Series Block Diagram

Then there are two "readback" parts, which consists of a latch or register back-to-back with a buffer: the 'LS793 readback latch, and the 'LS794 readback register. Both of these are just 20-pin, and hence offer a full 2:1 saving in board area as well as in parts count. They have structured pinouts compatible with those of the 'LS573 and 'LS574, but a very different internal architecture; each of the 8 elements (latch or flipflop) has 2 outputs, one of which is totem-pole and goes to the presumed "output pin" of that element, and the other of which is three-state and goes back to the "input pin" for the element (see Figure 4). Thus, it is possible to read the contents of an 'LS793 or 'LS794 from its *input* lines by enabling its three-state outputs.

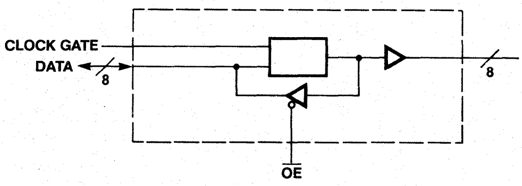


Figure 4. The '793/'794 Block Diagram

The 'LS793 and 'LS794 are intended for use in decentralized systems, for instance industrial-control systems in which a large number of slowly-changing setpoints and displays are under the control of a central microprocessor. The readback feature permits reading one of these, updating it, and replacing it. Without the readback feature, the system would have to keep a *redundant* copy of the setpoint or display value in main memory, which could cause additional system overhead due to the time-slicing of the microprocessor's activities, or even due to virtual-memory page-faulting in larger systems. Moreover, there is the reliability issue of whether the alleged redundant copy always agrees exactly with the real thing out there in the register controlling the actuator or the display, and what happens whenever it doesn't.

CONFIGURATION	BUFFERS	LATCHES	REGISTERS
Back-to-Back B/L/R	'245(244) '645/-1('244)	'547('373) '567('533)	'546('374) '566('534)
Back-to-Back Front-Loading Latches			'646/7('374) '648/9('534) '652/4('374 '651/3('534)
Readback B/L/R		'793('373)	'794('374)

Table 2. The Back-to-Back and Other Double-Density PLUS Interface Products from Monolithic Memories

Note that the bracketed part numbers represent the element *inside* the Double-Density PLUS Interface. For example, a '245 can replace two '244s, a '547 can replace two '533s, and a '546 can replace two '374s. The same holds true for the '646 and '651 series. However the '793/'794 are the equivalent of a '373/'374 and a readback buffer such as a '244.

Although they are not brand-new parts, it should also be mentioned that the 'LS245 and 'LS640/1/2/3/4/5 (and their "−1" high-drive options) are likewise in principle Double-Density PLUS™ Interface parts with a back-to-back architecture.

Table 2 is a summary of the back-to-back Double-Density PLUS™ Interface presently available from Monolithic Memories.

Two other common and intuitively-plausible combinations of a couple of 8-bit latches or registers are "nose-to-tail" (one after the other), and "side-by-side" (alternate). If two registers are used in a nose-to-tail combination, for instance, data from the inputs enters the first register when it is clocked, and the outputs of the first register are the inputs of the second register, and thus the same data finally reach the outputs of the combination when the second register is subsequently clocked. And, if two registers are used in a side-by-side combination, their inputs come from the same input bus, and their outputs go to the same output bus, but they can be controlled separately and the output bus can be driven from either one.

Although the nose-to-tail configuration and the side-by-side configuration seem quite different, with the provision of some internal multiplexing the same Double-Density PLUS™ Interface part can satisfy both requirements. Such a part is called a pipeline — register or latch, as the case may be. The internal architecture of a two-level pipeline is shown in Figure 5.

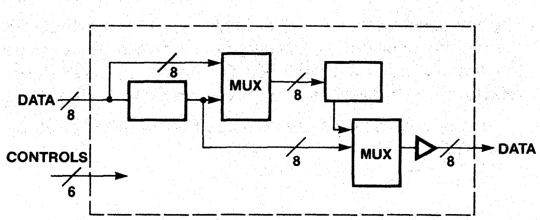


Figure 5. The '548/9 Block Diagram

The 'LS548, with the edge-triggered registers, and the 'LS549, with latches, follow the Figure 5 block diagram exactly. Their pinouts resemble those of 'LS546, 'LS646, and 'LS651 families. Their speeds are similar, and they also feature 32-mA-I_{OL} outputs.

Typical applications for Double-Density PLUS Interface include computer peripherals, minicomputers, and microcomputers. Applications for the open-collector parts are in the telecommunication and games areas. The drive of these parts enables them to drive heavily-loaded buses, and flat cables.

12

8-Bit Buffer Transceiver

SN54/74LS245

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric — equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Pin-compatible with SN54/74LS645 — improved speed, I_{IL} and I_{OZL} specifications

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS245	J,L,W	Mil	Non-invert	LS
SN74LS245	N,J	Com		

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device so that the buses are effectively isolated.

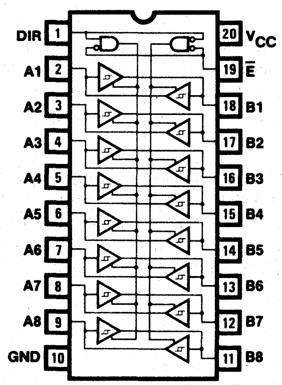
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

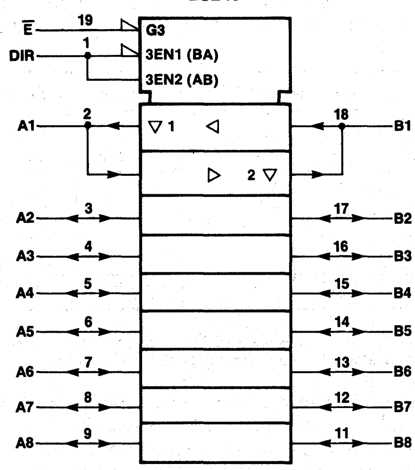
Logic Symbol

'LS245



IEEE Symbol

'LS245



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = –18mA			–1.5			–1.5	V
ΔV_T	Hysteresis $(V_{T+} - V_{T-})$ A or B	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			–0.2			–0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_I	Maximum input current — A or B	V_{CC} = MAX,	V_I = 5.5V			0.1			0.1	mA
	Maximum input current — DIR or $\bar{E}$		V_I = 7.0V							
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = –3mA	2.4	3.4		2.4	3.4		V
			I_{OH} = –12mA	2			2			
			I_{OH} = –15mA				2			
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			–200			–200	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		–40		–225	–40		–225	mA
I_{CC}	Supply Current — Outputs High	V_{CC} = MAX, Outputs open			48	70		48	70	mA
	Supply Current — Outputs Low				62	90		62	90	
	Supply Current — Outputs Disabled				64	95		64	95	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	A to B DIRECTION MIN	A to B TYP	A to B MAX	B to A DIRECTION MIN	B to A TYP	B to A MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		8	12		8	12	ns
t_{PHL}				8	12		8	12	ns
t_{PZL}	Output Enable delay			27	40		27	40	ns
t_{PZH}				25	40		25	40	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				15	25		15	25	ns

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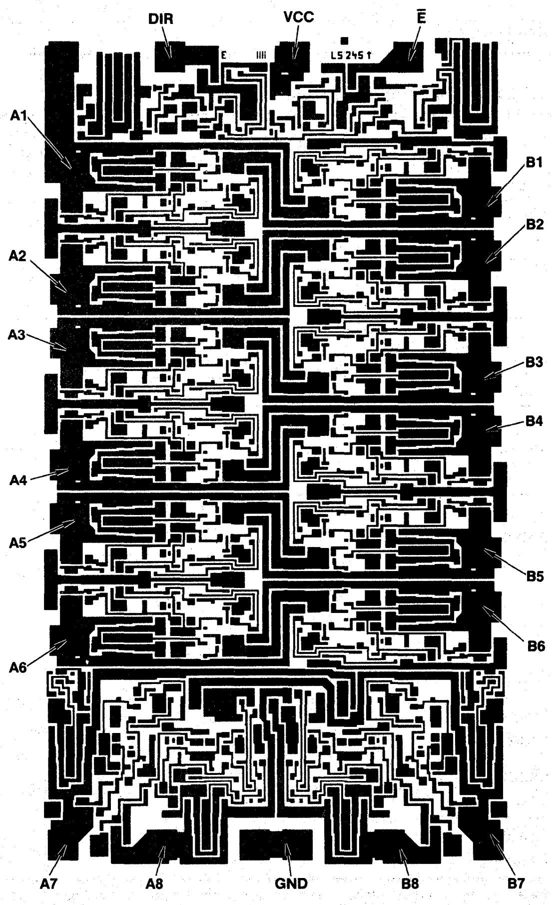
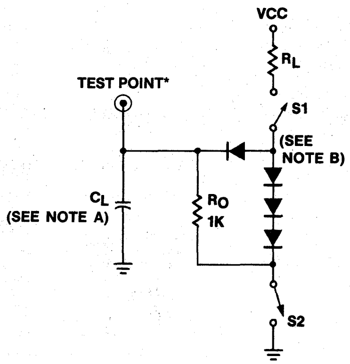
Die Configuration

'LS245



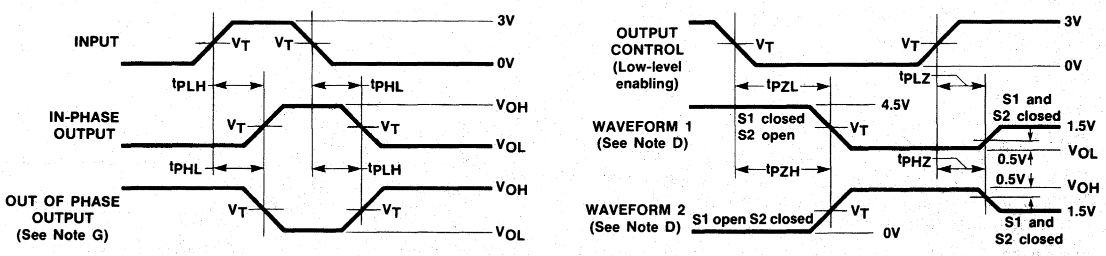
Die Size: 65x111 mil^2

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54/74LS, R_O = 5K, V_T = 1.3 V.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, t_R ≤ 2.5 ns, t_F ≤ 2.5 ns.
For Series 54/74LS and PALs, t_R ≤ 15 ns. t_F ≤ 6 ns.

G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

12

8-Bit Buffer Transceivers

SN54/74LS645 SN74LS645-1

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric — equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- SN74LS645-1 rated at I_{OL} = 48 mA

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS645	J,L,W	Mil	Non-invert	LS
SN74LS645	N,J	Com		
SN74LS645-1	J	Com		

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device so that the buses are effectively isolated.

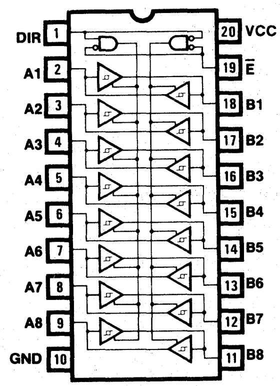
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

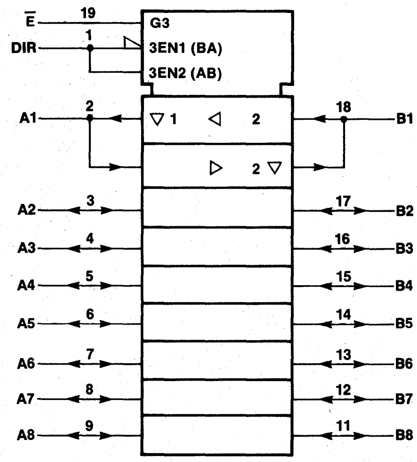
Logic Symbol

'LS645/645-1



IEEE Symbol

'LS645/645-1



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.5			0.6	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
	Hysteresis ($V_{T+}-V_{T-}$) A or B	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			20			20	µA
I_I	Maximum input current A or B	V_{CC} = MAX	V_I = 5.5V			0.1			0.1	mA
	Maximum input current DIR or $\overline{E}$		V_I = 7V							
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
		V_{IL} = MAX,	I_{OL} = 24mA					0.35	0.5	
		V_{IH} = 2V	I_{OL} = 48mA†					0.4	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
		V_{IL} = MAX,	I_{OH} = −12mA	2						
		V_{IH} = 2V	I_{OH} = −15mA				2			
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−400			−400	µA
I_{OZH}			V_O = 2.7V			20			20	µA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current — Outputs High	V_{CC} = MAX, Outputs open			48	70		48	70	mA
	Supply Current — Outputs Low				62	90		62	90	
	Supply Current — Outputs Disabled				64	95		64	95	

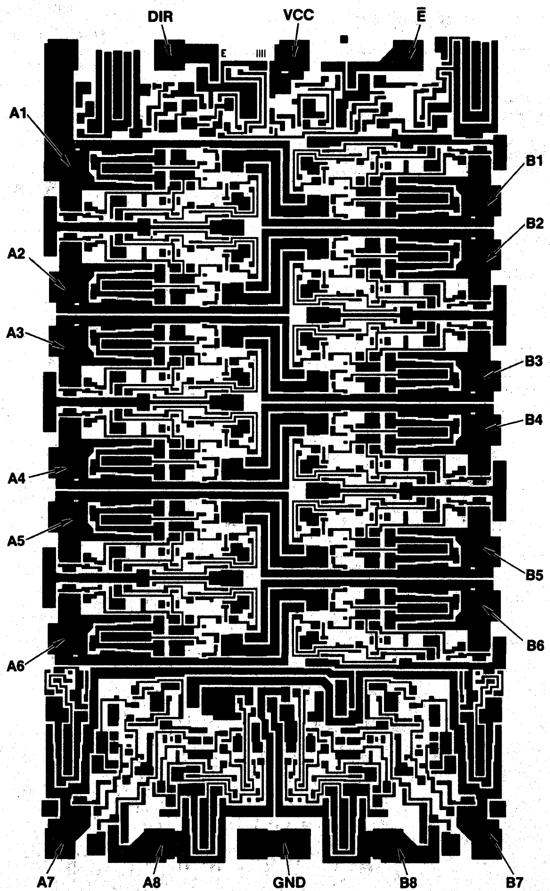
*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†This specification applies only to the SN74LS645-1.

Switching Characteristics V_{CC} = 5 V, T_A = 25° C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	A TO B DIRECTION MIN	A TO B DIRECTION TYP	A TO B DIRECTION MAX	B TO A DIRECTION MIN	B TO A DIRECTION TYP	B TO A DIRECTION MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		8	15		8	15	ns
t_{PHL}				11	15		11	15	ns
t_{PZL}	Output Enable delay			31	40		31	40	ns
t_{PZH}				26	40		26	40	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				15	25		15	25	ns

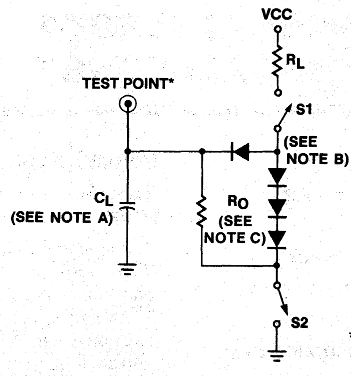
Die Configuration

'LS645, 'LS645-1



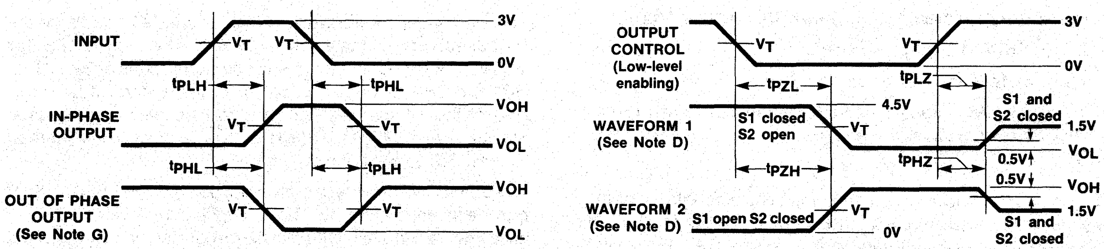
Die Size: 65x111 mil^2

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay $V_T = 1.3$ V **Enable and Disable**

NOTES:
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54/74LS, R_O = 5K, V_T = 1.3 V.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, $t_R \le 2.5$ ns, $t_F \le 2.5$ ns.
For Series 54/74LS and PALs, $t_R \le 15$ ns. $t_F \le 6$ ns.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

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8-Bit Bus Register Transceivers and Latch Transceivers

SN54/74LS546 SN54/74LS547
SN54/74LS566 SN54/74LS567

Features/Benefits

- **Bidirectional transceivers utilizing registers or latches**
- **Faster than other LS-TTL registers/latches**
- **Independent registers/latches for A bus and B bus**
- **Data can be swapped between internal registers/latches**
- **8-bit data paths match byte boundaries**
- **'LS546/547/566/567 can replace two 'LS374/373/534/533 devices**
- **Independent clock/gate enables for rank A and rank B**
- **High drive capability: I_{OL} = 32 mA (COM), 24 mA (MIL)**
- **24-pin SKINNYDIP® saves space**
- **Three-state outputs drive bus lines**
- **The clock, clock-enable, and latch-enable inputs typically have 300 mV hysteresis**

There are independent clock and clock enable controls for the two directions namely CKA, CKB, CKEA, CKEB for 'LS546/'LS566, and independent gate enable control GA1, GA2, GB1 and $\overline{GB2}$ for 'LS547/'LS567. The CKA/B and $\overline{CKEA/B}$ can control the internal registers A/B to load data or hold data. Similarly, the GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ can govern the internal latches, A/B to pass or hold data.

Description

These devices are comprised of a pair of 8-bit registers ('LS546, 'LS566), or a pair of 8-bit latches ('LS547, 'LS567).

The direction of operation is controlled by $\overline{OEAB}$ and $\overline{OEBA}$. When $\overline{OEAB}$ is Low and $\overline{OEBA}$ is High, the operation of the registers/latches is A-to-B direction; when $\overline{OEAB}$ is High and $\overline{OEBA}$ is low, the operation of the registers/latches is B-to-A direction; when $\overline{OEAB}$ and $\overline{OEBA}$ both are High, the A, B buses both are inputs, data will be stored into registers/latches; when $\overline{OEAB}$ and $\overline{OEBA}$ both are Low, the A, B buses both are outputs, data will transfer from internal registers/latches to A, B buses.

There are independent clock and clock enable controls for the two directions: namely CKA, CKB, $\overline{CKEA}$ and $\overline{CKEB}$ for 'LS546/'LS566, and independent gate enable control GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ for 'LS547/'LS567. The CKA/B and $\overline{CKEA/B}$ can control the internal registers A/B to load data or hold data. Similarly, the GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ govern the internal latches, A/B to pass or hold data.

The 'LS546/'547 provide non-inverting polarity; the 'LS566/'LS567 provide inverting polarity. The 'LS546/'LS547/'LS566/'LS567 all have 3-state outputs, and have 32-mA output drive I_{OL} (COM) over the commercial temperature range and 24-mA output drive I_{OL} (MIL), over the military temperature range.

All of the devices are packaged in the popular 24-pin SKINNYDIP package.

Ordering Information

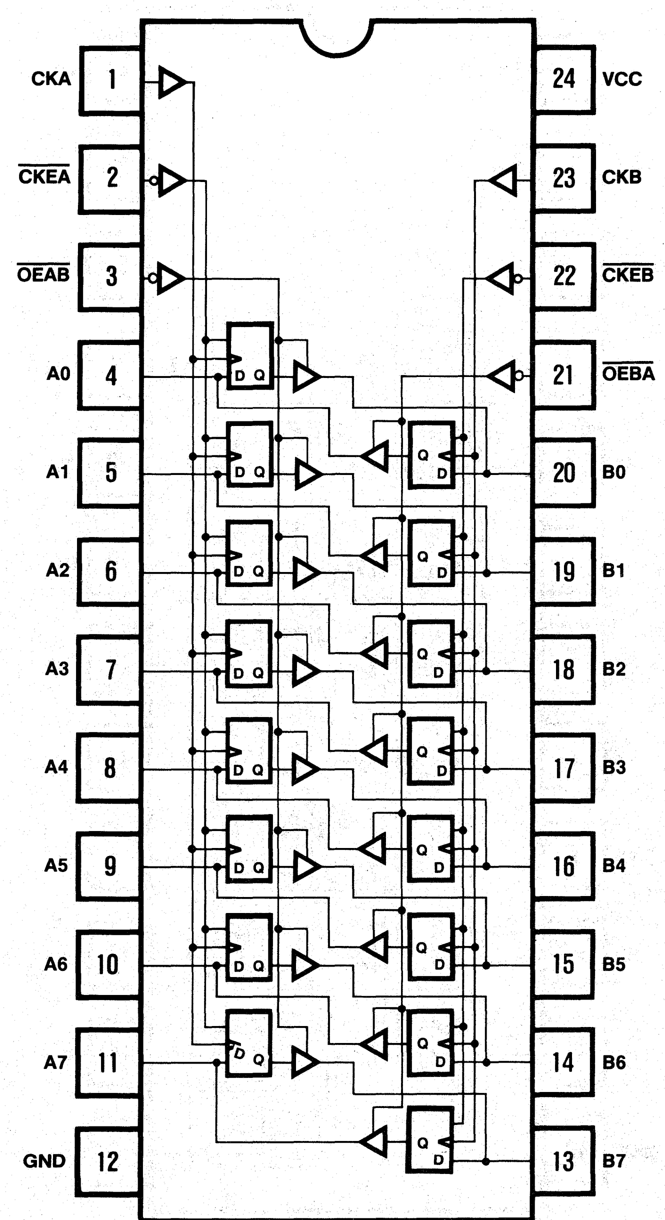
PART NUMBER	PACKAGE	TEMPERATURE	POLARITY	TYPE	POWER
SN54LS546	JS, W, L	Mil	Non-invert	Register	LS
SN74LS546	NS, JS	Com			
SN54LS547	JS, W, L	Mil		Latch	
SN74LS547	NS, JS	Com			
SN54LS566	JS, W, L	Mil	Invert	Register	
SN74LS566	NS, JS	Com			
SN54LS567	JS, W, L	Mil		Latch	
SN74LS567	NS, JS	Com			

NOTE: L package here is L28. The other packages are 24-pin.

TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

Logic Diagram

SN54/74LS546
REGISTER TRANSCEIVER
NON-INVERTING OUTPUTS



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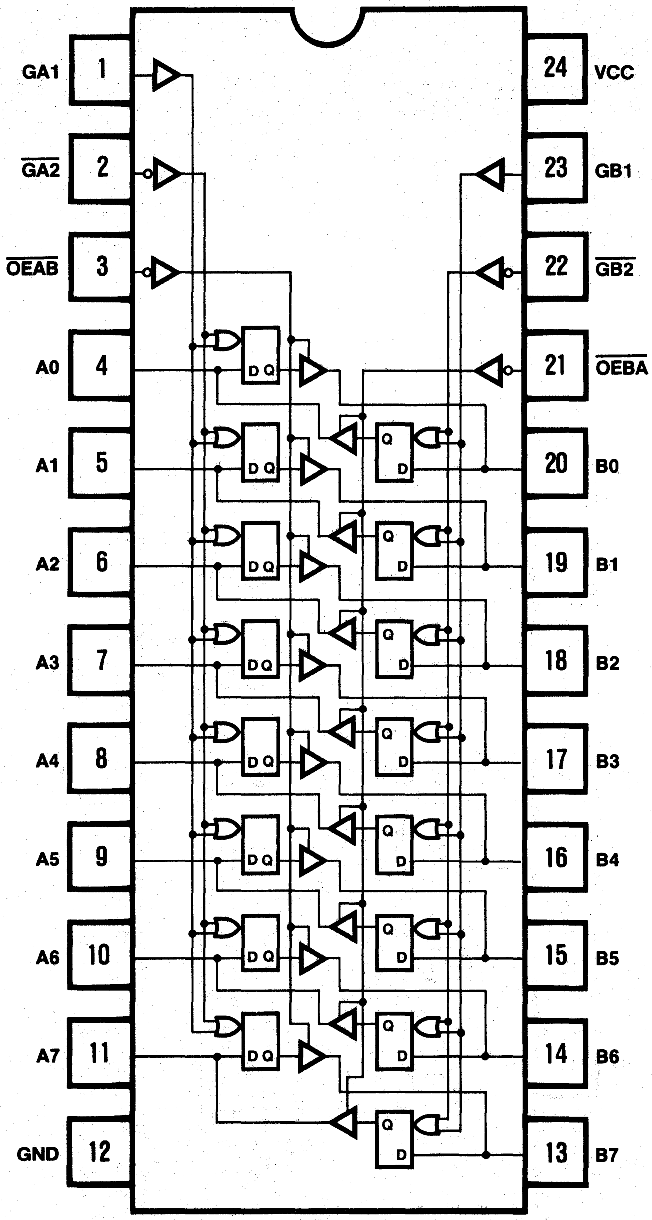
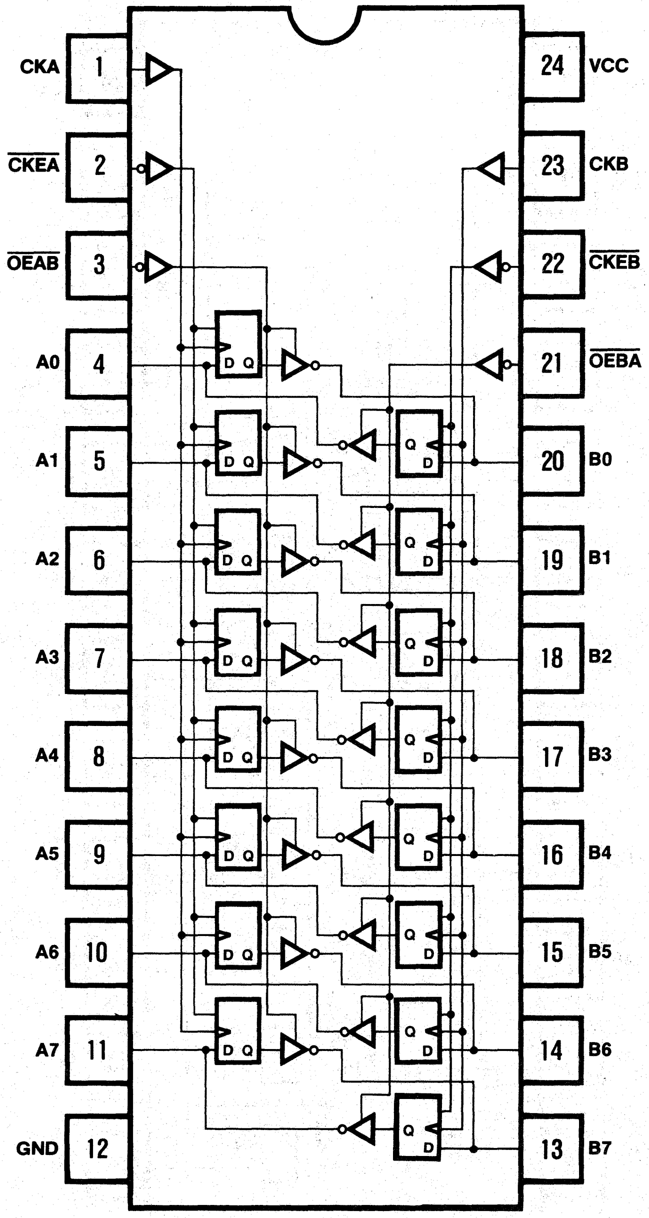
Logic Diagram

SN54/74LS547
LATCH TRANSCEIVER
NON-INVERTING OUTPUTS



Logic Diagram

SN54/74LS566
REGISTER TRANSCEIVER
INVERTING OUTPUTS



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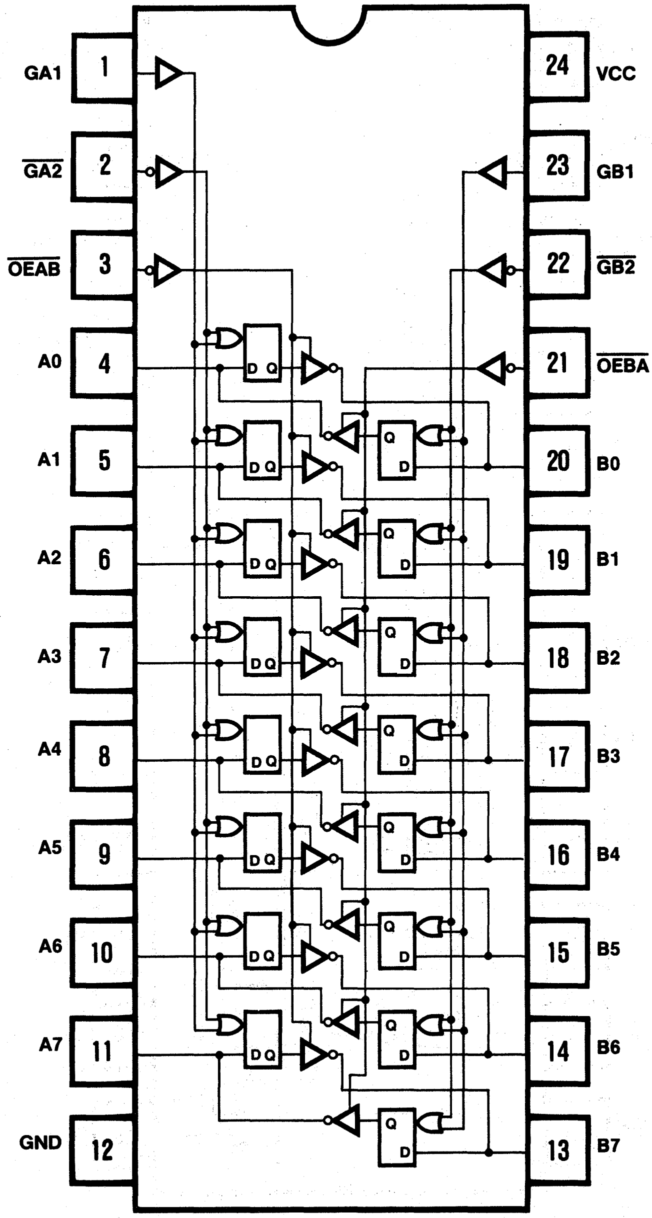
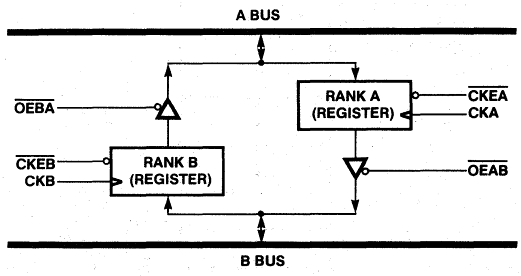
Logic Diagram

SN54/74LS567
LATCH TRANSCEIVER
INVERTING OUTPUTS

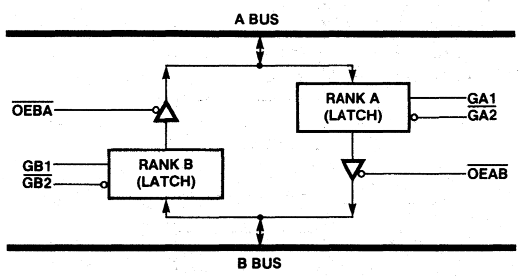


Block Diagrams

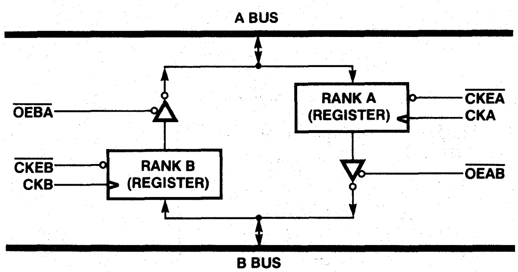
'LS546 (Non-inverting)



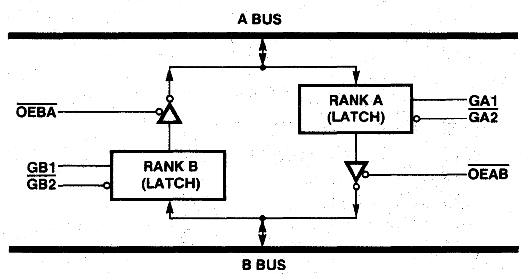
'LS547 (Non-inverting)



'LS566 (Inverting)



'LS567 (Inverting)



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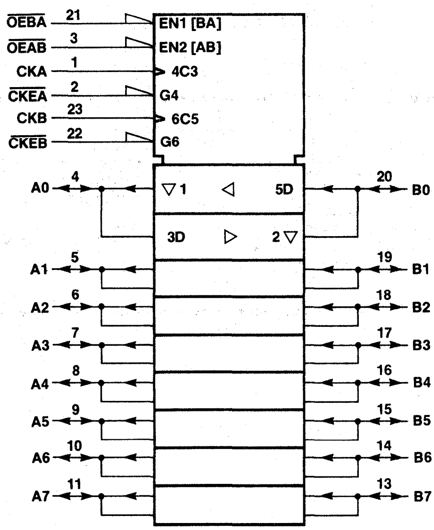
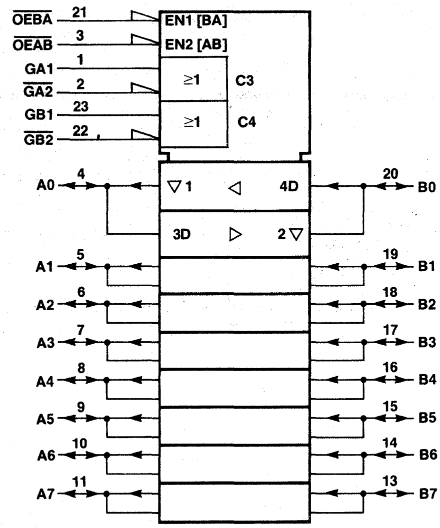
IEEE Symbols

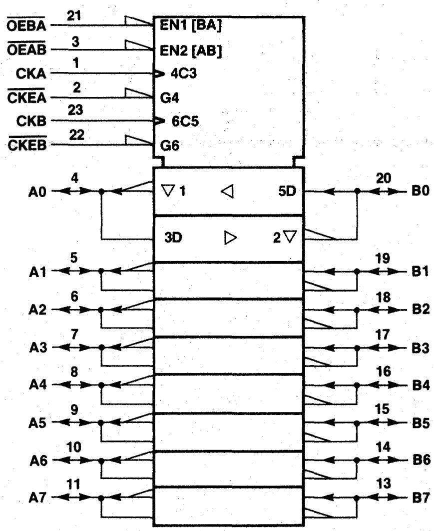
'LS546



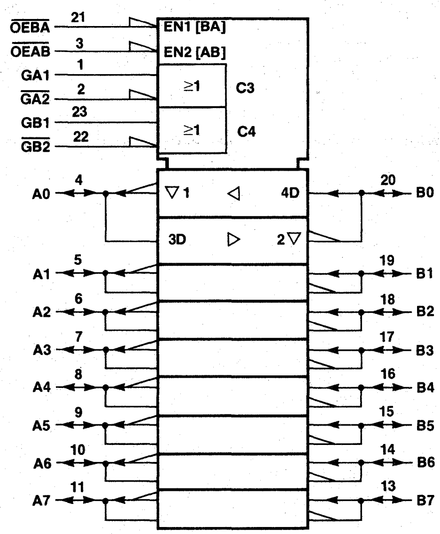
'LS547



'LS566



'LS567



Function Table Nomenclature Description

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

X: H or L state irrelevant ("Don't Care" conditions).

GA1/$\overline{\text{GA2}}$: Gate enables for rank A of 'LS547/'LS567.

GB1/$\overline{\text{GB2}}$: Gate enables for rank B of 'LS547/'LS567.

QoA/QoB: Previous data of the internal rank A/B.

GA1	$\overline{\text{GA2}}$	RANK A	GB1	$\overline{\text{GB2}}$	RANK B
L	L	Enabled (Flush)	L	L	Enabled (Flush)
L	L	Enabled (Flush)	L	H	Disabled (Freeze)
L	L	Enabled (Flush)	H	X	Enabled (Flush)
L	H	Disabled (Freeze)	H	X	Enabled (Flush)
L	H	Disabled (Freeze)	L	L	Enabled (Flush)
L	H	Disabled (Freeze)	L	H	Disabled (Freeze)
H	X	Enabled (Flush)	L	L	Enabled (Flush)
H	X	Enabled (Flush)	L	H	Disabled (Freeze)
H	X	Enabled (Flush)	H	X	Enabled (Flush)

$\overline{\text{CKEA}}$/$\overline{\text{CKEB}}$: Clock enable for rank A/B of 'LS546/'LS566.

CKA/CKB: Clock for rank A/B of 'LS546/'LS566.

UC: H or L or $\downarrow$ case (nonclocked operation).

$\uparrow$: Positive edge of CK causes clocking, if clock enable is asserted.

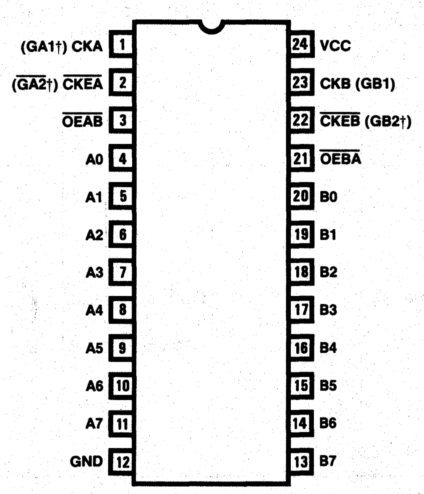
CKA	$\overline{\text{CKEA}}$	RANK A	CKB	$\overline{\text{CKEB}}$	RANK B
UC	X	Disabled	UC	X	Disabled
$\uparrow$	L	Enabled	$\uparrow$	L	Enabled
$\uparrow$	L	Enabled	$\uparrow$	H	Disabled
$\uparrow$	H	Disabled	$\uparrow$	L	Enabled
$\uparrow$	H	Disabled	$\uparrow$	H	Disabled

$\overline{\text{OEAB}}$: To enable the A-to-B operation.

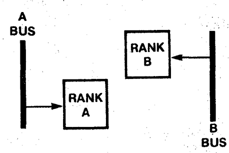
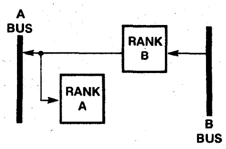
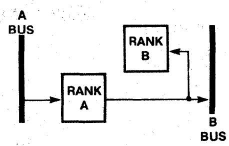
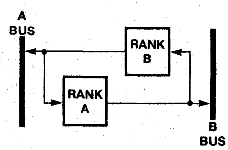
$\overline{\text{OEBA}}$: To enable the B-to-A operation.

$\overline{\text{OEAB}}$	$\overline{\text{OEBA}}$	OPERATION DIRECTION
L	L	A, B buses both are outputs (Transfer stored data to bus stored)
L	H	A-to-B
H	L	B-to-A
H	H	A, B buses both are inputs (storage)

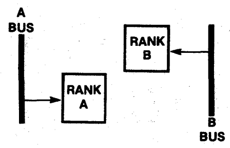
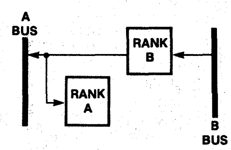
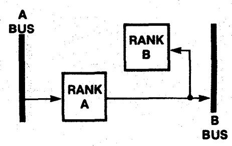
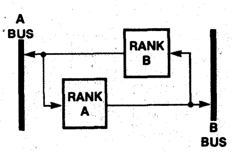
Pin Configuration



Bus Operation For 'LS546

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	GATE ENABLE (A)		RANK A	GATE ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		CKA	$\overline{CKEA}$		CKB	$\overline{CKEB}$	
Storage	H	H	Input	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	B bus
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
B-to-A Operation	H	L	Output of Rank B	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	Rank B	UC	X	QoB
						↑	L	Rank B	↑	L	B bus
						↑	L	Rank B	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
A-to-B Operation	L	H	Input	Output of Rank A		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	Rank A
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	Rank A
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	Rank A
						↑	H	QoA	↑	H	QoB
Transfer Stored Data	L	L	Output of Rank B	Output of Rank A		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	Rank A
						UC	X	QoA	↑	H	QoB
						↑	L	Rank B	UC	X	QoB
						↑	L	Rank B	↑	L	Rank A
						↑	L	Rank B	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	Rank A
						↑	H	QoA	↑	H	QoB

Bus Operation For 'LS547

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	GATE ENABLE (A)		RANK A	GATE ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		GA1	$\overline{GA2}$		GB1	$\overline{GB2}$	
Storage	H	H	Input	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	B bus
						H	X	A bus	X	L	B bus
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	B bus
						X	L	A bus	X	L	B bus
B-to-A Operation	H	L	Output of Rank B	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	Rank B	L	H	QoB
						H	X	Rank B	H	X	B bus
						H	X	Rank B	X	L	B bus
						X	L	Rank B	L	H	QoB
						X	L	Rank B	H	X	B bus
						X	L	Rank B	X	L	B bus
A-to-B Operation	L	H	Input	Output of Rank A		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	Rank A
						L	H	QoA	X	L	Rank A
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	Rank A
						H	X	A bus	X	L	Rank A
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	Rank A
						X	L	A bus	X	L	Rank A
Transfer Stored Data	L	L	Output of Rank B	Output of Rank A		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	Rank A
						L	H	QoA	X	L	Rank A
						H	X	Rank B	L	H	QoB
						H*	X	Rank B	H	X	Rank A
						H*	X	Rank B	X	L	Rank A
						X	L	Rank B	L	H	QoB
						X*	L	Rank B	H	X	Rank A
						X*	L	Rank B	X	L	Rank A

* NOTE: These controls for $\overline{OEAB}$, $\overline{OEBA}$, GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ can cause race conditions.

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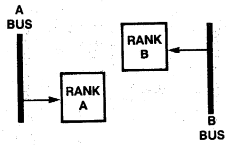
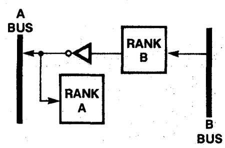
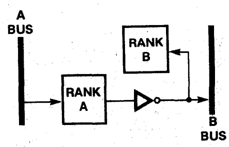
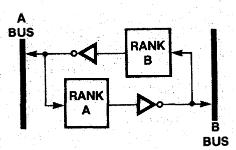
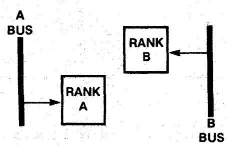
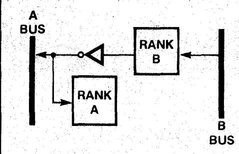
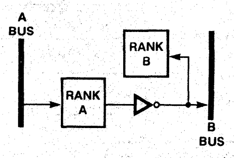
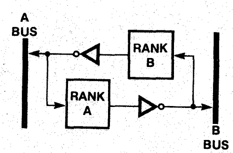
Bus Operation For 'LS566

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE (A)		RANK A	CLOCK ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		CKA	$\overline{CKEA}$		CKB	$\overline{CKEB}$	
Storage	H	H	Input	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	B bus
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
B-to-A Operation	H	L	Output of $\overline{\text{Rank B}}$	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	$\overline{\text{Rank B}}$	UC	X	QoB
						↑	L	$\overline{\text{Rank B}}$	↑	L	B bus
						↑	L	$\overline{\text{Rank B}}$	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
A-to-B Operation	L	H	Input	Output of $\overline{\text{Rank A}}$		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	$\overline{\text{Rank A}}$
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	$\overline{\text{Rank A}}$
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	$\overline{\text{Rank A}}$
						↑	H	QoA	↑	H	QoB
Transfer Stored Data	L	L	Output of $\overline{\text{Rank B}}$	Output of $\overline{\text{Rank A}}$		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	$\overline{\text{Rank A}}$
						UC	X	QoA	↑	H	QoB
						↑	L	$\overline{\text{Rank B}}$	UC	X	QoB
						↑	L	$\overline{\text{Rank B}}$	↑	L	$\overline{\text{Rank A}}$
						↑	L	$\overline{\text{Rank B}}$	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	$\overline{\text{Rank A}}$
						↑	H	QoA	↑	H	QoB

Bus Operation For 'LS567

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	GATE ENABLE (A)		RANK A	GATE ENABLE (B)		RANK B
	$\overline{\text{OEAB}}$	$\overline{\text{OEBA}}$	A0-A7	B0-B7		GA1	$\overline{\text{GA2}}$		GB1	$\overline{\text{GB2}}$	
Storage	H	H	Input	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	B bus
						H	X	A bus	X	L	B bus
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	B bus
						X	L	A bus	X	L	B bus
B-to-A Operation	H	L	Output of Rank B	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	$\overline{\text{Rank B}}$	L	H	QoB
						H	X	$\overline{\text{Rank B}}$	H	X	B bus
						H	X	$\overline{\text{Rank B}}$	X	L	B bus
						X	L	$\overline{\text{Rank B}}$	L	H	QoB
						X	L	$\overline{\text{Rank B}}$	H	X	B bus
						X	L	$\overline{\text{Rank B}}$	X	L	B bus
A-to-B Operation	L	H	Input	Output of Rank A		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	$\overline{\text{Rank A}}$
						L	H	QoA	X	L	$\overline{\text{Rank A}}$
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	$\overline{\text{Rank A}}$
						H	X	A bus	X	L	$\overline{\text{Rank A}}$
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	$\overline{\text{Rank A}}$
						X	L	A bus	X	L	$\overline{\text{Rank A}}$
Transfer Stored Data	L	L	Output of Rank B	Output of Rank A		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	$\overline{\text{Rank A}}$
						L	H	QoA	X	L	$\overline{\text{Rank A}}$
						H	X	$\overline{\text{Rank B}}$	L	H	QoB
						H*	X	$\overline{\text{Rank B}}$	H	X	$\overline{\text{Rank A}}$
						H*	X	$\overline{\text{Rank B}}$	X	L	$\overline{\text{Rank A}}$
						X	L	$\overline{\text{Rank B}}$	L	H	QoB
						X*	L	$\overline{\text{Rank B}}$	H	X	$\overline{\text{Rank A}}$
						X*	L	$\overline{\text{Rank B}}$	X	L	$\overline{\text{Rank A}}$

* NOTE: These controls for $\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$, GA1, $\overline{\text{GA2}}$, GB1 and $\overline{\text{GB2}}$ can cause race conditions.

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Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER				MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage				4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature				−55		125	0		75	°C
T_W	Width of clock/gate	'LS546, 'LS566	High	CK	11			8			ns
			Low		19			15			
		'LS547, 'LS567	High	GA1,GB1	10			8			
			Low	$\overline{GA2}$,$\overline{GB2}$	18			16			
T_{su}	Setup time	'LS546	CKA, CKB		14↑			11↑			ns
		'LS547	GA1, GB1		5↓			5↓			
			$\overline{GA2}$, $\overline{GB2}$		15↑			15↑			
		'LS566	CKA, CKB		14↑			11↑			
		'LS567	GA1, GB1		13↓			13↓			
			$\overline{GA2}$, $\overline{GB2}$		22↑			22↑			
T_h	Hold time	'LS546	CKA, CKB		0↑			0↑			ns
		'LS547	GA1, GB1		13↓			13↓			
			$\overline{GA2}$, $\overline{GB2}$		5↑			5↑			
		'LS566	CKA, CKB		0↑			0↑			
		'LS567	GA1, GB1		11↓			11↓			
			$\overline{GA2}$, $\overline{GB2}$		5↑			5↑			
T_{suce}	Setup time for $\overline{CKEA}$, $\overline{CKEB}$, ('LS546, 'LS566 only)				15↑			11↑			ns
T_{hce}	Hold time for $\overline{CKEA}$, $\overline{CKEB}$ ('LS546, 'LS566 only)				5↑			4↑			ns

↑ ↓ the arrow indicates the transition of the clock/gate input used for reference:
↑ for the low-to-high transitions.
↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX V_I = 0.4 V	A or B			−250			−250	μA
				All others			−400			−400	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7.0 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = 2V	I_{OL} = 24 mA			0.5				V
				I_{OL} = 32 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IL} = MAX V_{IH} = 2V	I_{OH} = −1 mA	2.4	3.4					V
				I_{OH} = −2.6 mA				2.4	3.1		
I_{OZL}	Off-state output current		V_{CC} = MAX	V_O = 0.4 V			−250			−250	μA
I_{OZH}				V_O = 2.4 V			20			20	
I_{OS}	Output short-circuit current*		V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current		V_{CC} = MAX Outputs open	'LS546			180			180	mA
				'LS547			180			180	
				'LS566			180			180	
				'LS567			180			180	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

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Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY 'LS546 MIN	MILITARY 'LS546 MAX	MILITARY 'LS547 MIN	MILITARY 'LS547 MAX	COMMERCIAL 'LS546 MIN	COMMERCIAL 'LS546 MAX	COMMERCIAL 'LS547 MIN	COMMERCIAL 'LS547 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω, $\overline{OE}$ = L		33				43			MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS546 only)			26				21			ns
t_{PLH}/t_{PHL}	GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS547 only)					27				24	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS547 only)					23				18	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω		25		25		21		21	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω		22		22		19		19	ns

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	'LS546 MIN	'LS546 MAX	'LS547 MIN	'LS547 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω, $\overline{OE}$ = L		50			MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS546 only)			19			ns
t_{PLH}/t_{PHL}	GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS547 only)					23	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS547 only)					17	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω		19		19	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω		17		17	ns

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY				COMMERCIAL				UNIT
			'LS566		'LS567		'LS566		'LS567		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω $\overline{OE}$ = L		33				43			MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS566 only)			26				21			ns
t_{PLH}/t_{PHL}	GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS567 only)					26				24	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS567 only)					29				23	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω		25		25		21		21	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω		22		22		19		19	ns

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

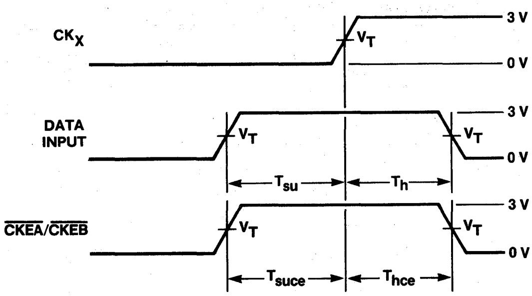
SYMBOL	PARAMETER	TEST CONDITIONS	'LS566		'LS567		UNIT
			MIN	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω $\overline{OE}$ = L		50			MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS566 only)			19			ns
t_{PLH}/t_{PHL}	GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS567 only)					21	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS567 only)					19	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω		19		19	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω		17		17	ns

12

Definition of Waveforms

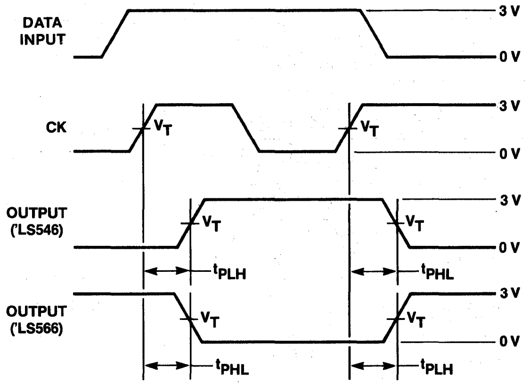
'LS546/566

Setup and Hold



$V_T = 1.3\ V$

Clock CK to Output Delay

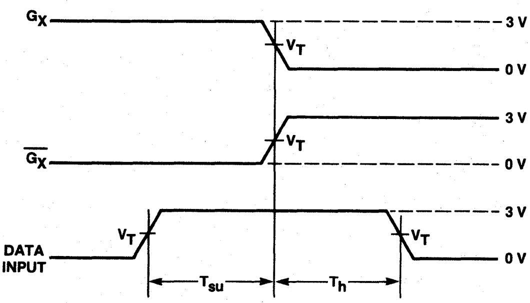


$V_T = 1.3\ V$

Definition of Waveforms

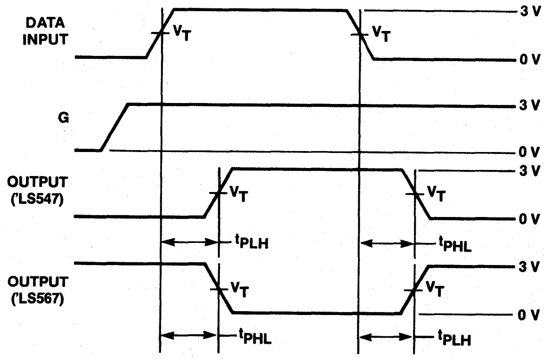
'LS547/567

Setup and Hold



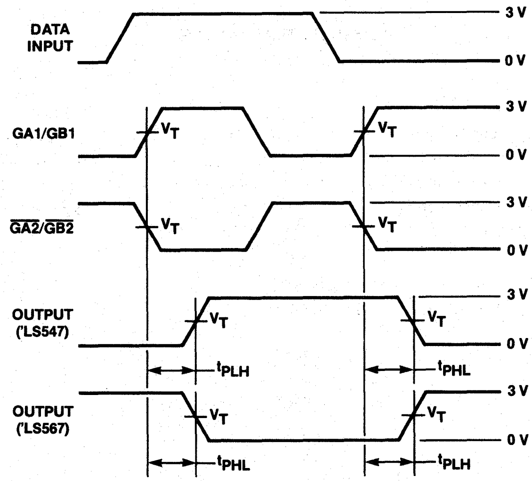
V_T = 1.3 V

Data D to Output Delay



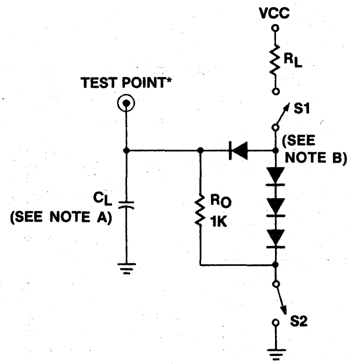
V_T = 1.3 V

GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to Output Delay

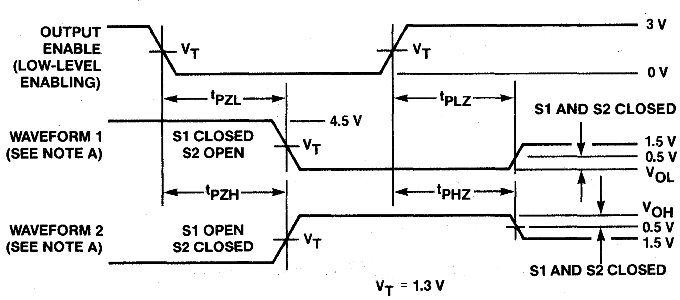


V_T = 1.3 V

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

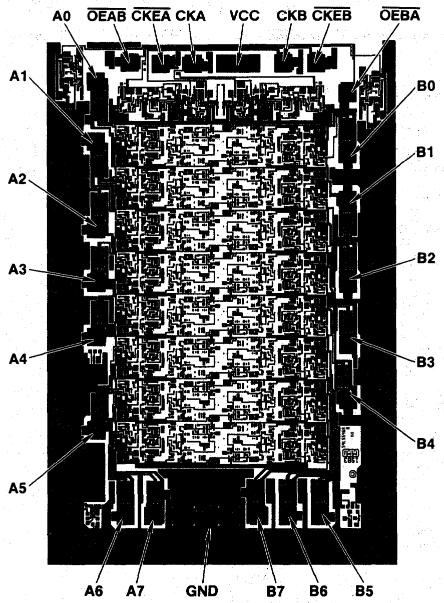


ENABLE AND DISABLE

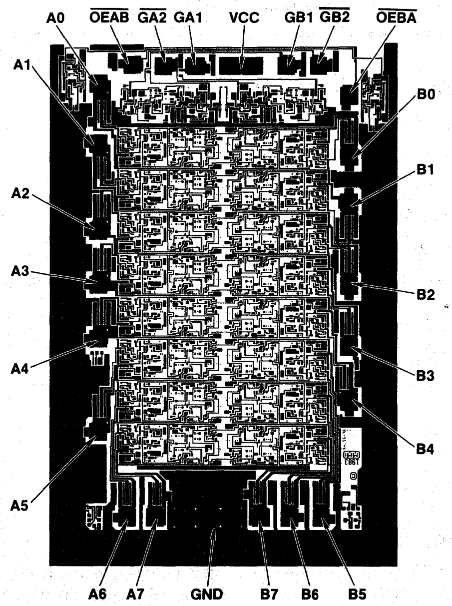
NOTES:
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50Ω and t_R ≤ 15 ns t_F ≤ 6 ns.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

Die Configurations

'LS546

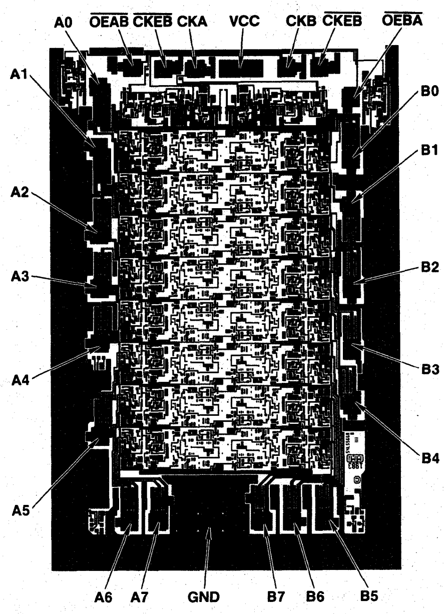


'LS547

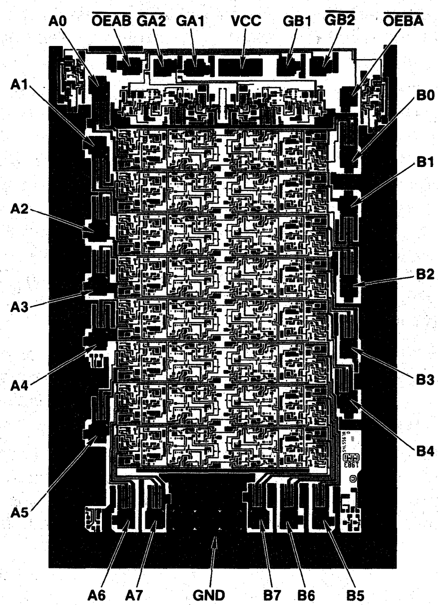


Die Size: 100x147 mil^2

'LS566



'LS567



12

8-Bit Bus Front-Loading-Latch Transceivers

SN54/74LS646 SN54/74LS647
SN54/74LS648 SN54/74LS649

Features/Benefits

- Bidirectional bus transceivers and registers
- Independent registers for A and B buses
- Real-time data transfer or stored data transfer
- 24-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Three-state or open-collector outputs drive bus lines

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	O/P	POWER
SN54LS646	JS,W,L	Mil	Non-invert	3-state	LS
SN74LS646	NS,JS	Com			
SN54LS647	JS,W,L	Mil		Open-collector	
SN74LS647	NS,JS	Com			
SN54LS648	JS,W,L	Mil	Invert	3-state	
SN74LS648	NS,JS	Com			
SN54LS649	JS,W,L	Mil		Open-collector	
SN74LS649	NS,JS	Com			

NOTE: L package here is L28. The other packages are 24-pin.

Description

The 8-bit bus transceivers with 3-state ('LS646, 'LS648) or open-collector ('LS647, 'LS649) outputs have 16 D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS646/647 and 'LS648/649 are given in their respective Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path or "feed-through" into a two-way mux, is sometimes called a "front-loading latch."

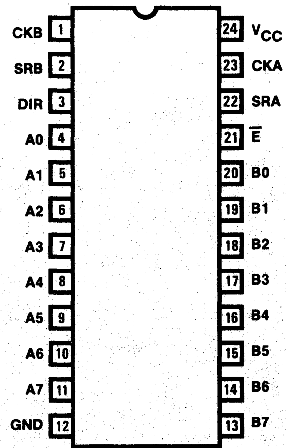
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by enable line $\overline{E}$, and direction line DIR.

When $\overline{E}$ is High data from the buses can be stored into register A and B. When $\overline{E}$ is Low and DIR is High, the direction of operation is from A to B; when $\overline{E}$ and DIR are LOW, the direction of operation is from B to A.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

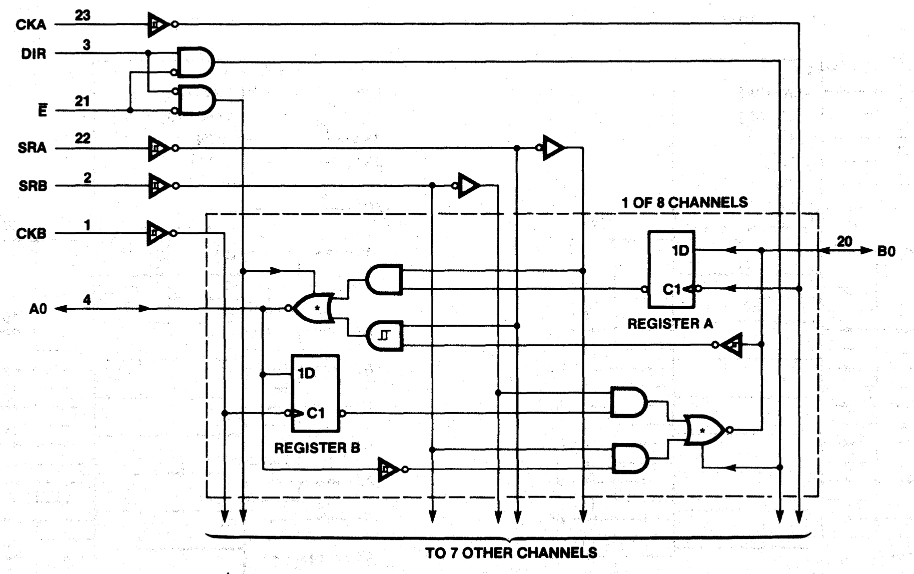
Pin Configuration

'LS646/647/648/649
8-Bit Bus Front-Loading-Latch Transceivers



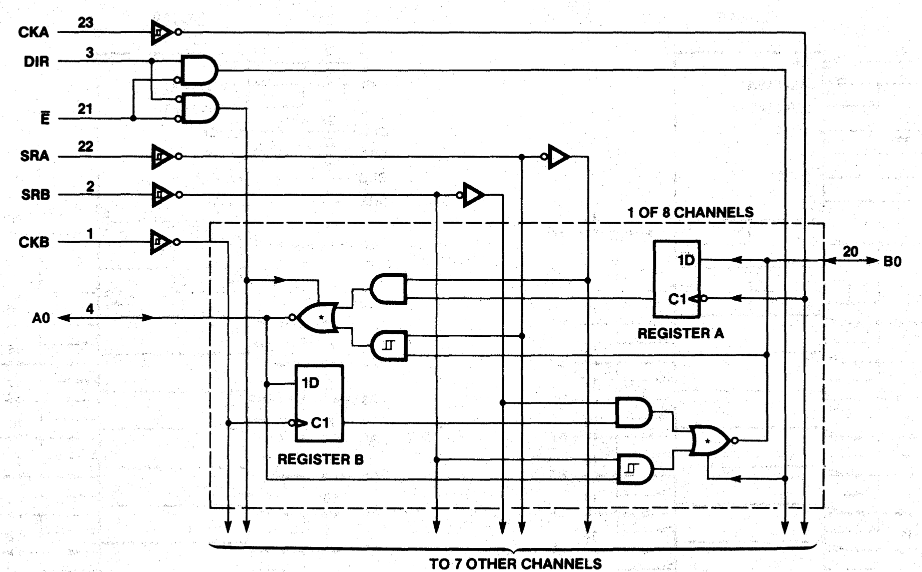
Logic Diagrams

'LS646/647 (Non-Inverting)



* For the 'LS646 devices, the A and B bus outputs are 3-state.
For the 'LS647 devices, the A and B bus outputs are open-collector.

'LS648/649 (Inverting)



* For the 'LS648 devices, the A and B bus outputs are 3-state.
For the 'LS649 devices, the A and B bus outputs are open-collector.

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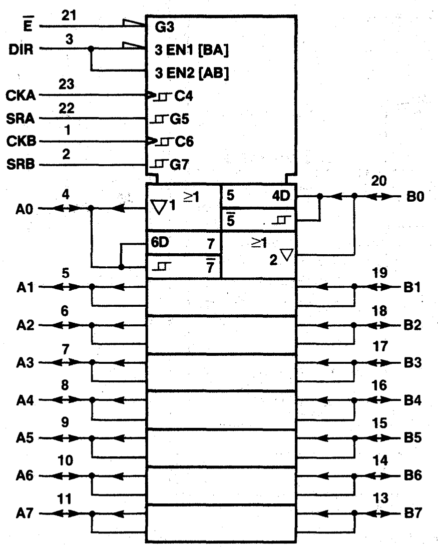
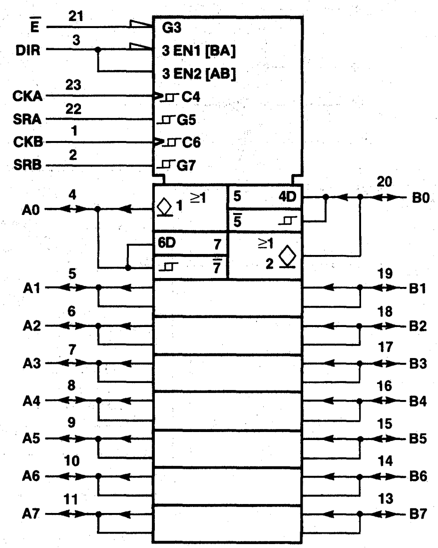
IEEE Symbols

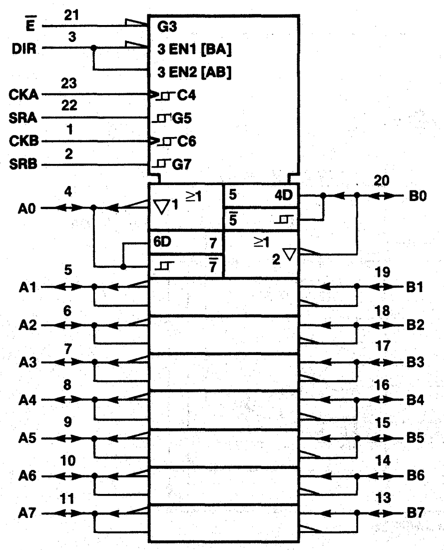
'LS646



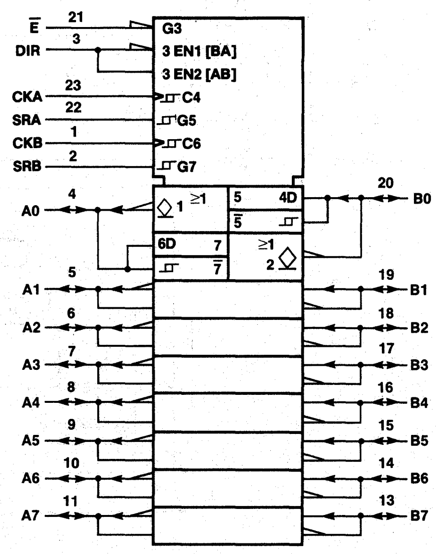
'LS647



'LS648

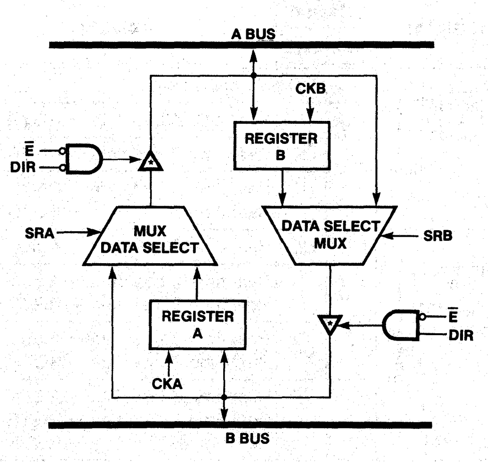


'LS649

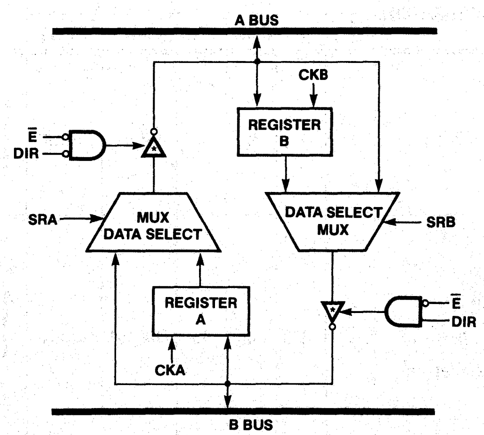


Block Diagrams

'LS646/647 (Non-Inverting)



'LS648/649 (Inverting)



* For the 'LS646/648 devices, the A and B bus outputs are 3-state.
For the 'LS647/649 devices, the A and B bus outputs are open-collector.

Function Table Nomenclature Description

Ē: To enable the A-to-B or B-to-A operation.

DIR: To select the direction of operation.

Ē	DIR	OPERATION DIRECTION
L	L	B-to-A
L	H	A-to-B
H	X	A and B buses both are inputs (storage)

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is a High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for Register A/B.

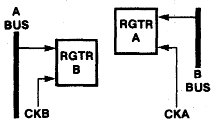
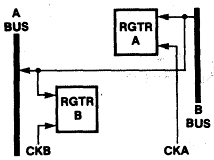
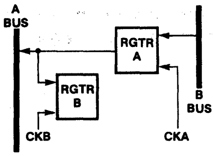
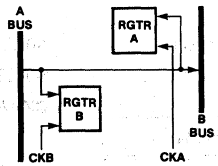
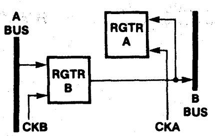
X: H or L state irrelevant ("Don't Care" conditions).

↑: Positive edge of CK causes clocking, if clock enable is asserted.

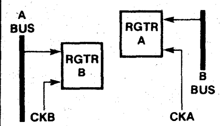
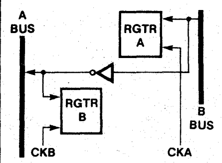
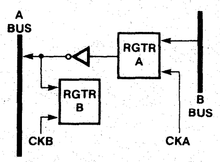
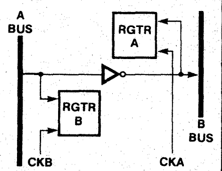
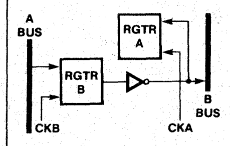
UC: H or L or ↓ case (nonclocked operation).

RGTR: Register.

Bus Operation for 'LS646/647

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS646/647
	$\overline{E}$	DIR	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	H	X	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time B bus data → A bus
								UC	↑	Real time B bus data → A bus Real time B bus data → RGTR B
								↑	UC	Real time B bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR A data → A bus
								UC	↑	RGTR A data → A bus RGTR A data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR A data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
Real time A-to-B Operation	L	H	X	L	Input	Output		UC	UC	Real time A bus data → B bus
								UC	↑	Real time A bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time A bus data → B bus Real time A bus data → RGTR A
								↑	↑	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	L	H	X	H	Input	Output		UC	UC	RGTR B data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR B data → B bus
								↑	UC	RGTR B data → B bus RGTR B data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A

Bus Operation for 'LS648/649

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS648/649
	$\overline{E}$	DIR	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	H	X	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time $\overline{B}$ bus data → A bus
								UC	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR B
								↑	UC	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A Real time $\overline{B}$ bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR $\overline{A}$ data → A bus
								UC	↑	RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
Real time A-to-B Operation	L	H	X	L	Input	Output		UC	UC	Real time $\overline{A}$ bus data → B bus
								UC	↑	Real time $\overline{A}$ bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A
								↑	↑	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	L	H	X	H	Input	Output		UC	UC	RGTR $\overline{B}$ data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus
								↑	UC	RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A

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Absolute Maximum Ratings

Supply voltage, V_{CC} .... 7.0 V
Input voltage, ... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		−55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS646	20 ↑			20 ↑			ns
		'LS648	20 ↑			20 ↑			
t_h	Hold time	'LS646	0 ↑			0 ↑			ns
		'LS648	0 ↑			0 ↑			
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
ΔV_T	Hysteresis (V_{T+}-V_{T-})		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			−0.4			−0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			−400			−400	μA
I_{OZH}				V_O = 2.7 V			20			20	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current		V_{CC} = MAX, 'LS-646	Outputs High			145			145	mA
				Outputs Low			165			165	
				Outputs Disabled			165			165	
			V_{CC} = MAX, 'LS-648	Outputs High			145			145	
				Outputs Low			165			165	
				Outputs Disabled			165			165	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics $V_{CC} = 5\,V$, $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS646 MIN	'LS646 MAX	'LS648 MIN	'LS648 MAX	UNIT
t_{PLH}	Data to output delay	$C_L = 45pF$ $R_L = 667\Omega$		18		18	ns
t_{PHL}				20		25	ns
t_{PLH}	Clock to output delay			25		25	ns
t_{PHL}				35		40	ns
t_{PLH}	Select to output delay (data input High)			40		55	ns
t_{PHL}				35		40	ns
t_{PLH}	Select to output delay (data input Low)			50		40	ns
t_{PHL}				25		40	ns
t_{PZL}	Output enable delay			65		55	ns
t_{PZH}				55		50	ns
t_{PLZ}	Output disable delay	$C_L = 5pF$ $R_L = 667\Omega$		35		35	ns
t_{PHZ}				35		45	ns
t_{PZL}	Direction enable delay	$C_L = 45pF$ $R_L = 667\Omega$		60		45	ns
t_{PZH}				45		40	ns
t_{PLZ}	Direction disable delay	$C_L = 5pF$ $R_L = 667\Omega$		30		30	ns
t_{PHZ}				30		35	ns

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIL				COM				UNIT
			'LS646		'LS648		'LS646		'LS648		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Data to output delay	$C_L = 45pF$ $R_L = 667\Omega$		25		18		25		18	ns
t_{PHL}				25		25		25		25	ns
t_{PLH}	Clock to output delay			28		25		28		25	ns
t_{PHL}				35		40		35		40	ns
t_{PLH}	Select to output delay † (data input High)			40		55		40		55	ns
t_{PHL}				35		40		35		40	ns
t_{PLH}	Select to output delay † (data input Low)			50		40		50		40	ns
t_{PHL}				30		40		30		40	ns
t_{PZL}	Output enable delay			65		55		65		55	ns
t_{PZH}				55		50		55		50	ns
t_{PLZ}	Output disable delay	$C_L = 5pF$ $R_L = 667\Omega$		45		35		45		35	ns
t_{PHZ}				45		50		45		50	ns
t_{PZL}	Direction enable delay	$C_L = 45pF$ $R_L = 667\Omega$		60		45		60		45	ns
t_{PZH}				45		40		45		40	ns
t_{PLZ}	Direction disable delay	$C_L = 5pF$ $R_L = 667\Omega$		40		30		40		30	ns
t_{PHZ}				45		45		45		45	ns

† See Figure 4.

Absolute Maximum Ratings

Supply voltage, V_{CC} .... 7.0 V
Input voltage, ... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150° C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		-55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			ns
t_{su}	Setup time	'LS647	20↑			20↑			ns
		'LS649	20↑			20↑			ns
t_h	Hold time	'LS647	0↑			0↑			ns
		'LS649	0↑			0↑			ns
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IH}	High-level input voltage					2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN		I_I = -18 mA			-1.5			-1.5	V
ΔV_T	Hysteresis (V_{T+}-V_{T-})		V_{CC} = MIN			0.1	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX		V_I = 0.4 V			-0.4			-0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX		V_I = 2.7 V			20			20	µA
I_I	Maximum input current	A or B	V_{CC} = MAX		V_I = 5.5 V			0.1			0.1	mA
		All others			V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V		I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 24 mA					0.35	0.5	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V		V_{OH} = 5.5 V			100			100	µA
I_{CC}	Supply current		V_{CC}= MAX	'LS-647	Outputs High			130			130	mA
					Outputs Low			150			150	
					Outputs Disabled			150			150	
				'LS-649	Outputs High			130			130	
					Outputs Low			150			150	
					Outputs Disabled			150			150	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics $V_{CC} = 5$ V, $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS647 MIN	'LS647 MAX	'LS649 MIN	'LS649 MAX	UNIT
t_{PLH}	Data to output delay	$C_L = 45pF$ $R_L = 667\Omega$		26		25	ns
t_{PHL}				27		30	ns
t_{PLH}	Clock to output delay			35		30	ns
t_{PHL}				45		45	ns
t_{PLH}	Select to output delay† (data input High)			50		55	ns
t_{PHL}				45		45	ns
t_{PLH}	Select to output delay† (data input Low)			60		45	ns
t_{PHL}				30		40	ns
t_{PLH}	Output enable delay			40		40	ns
t_{PHL}				50		50	ns
t_{PLH}	Direction enable delay			35		30	ns
t_{PHL}				40		45	ns

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIL 'LS647 MIN	MIL 'LS647 MAX	MIL 'LS649 MIN	MIL 'LS649 MAX	COM 'LS647 MIN	COM 'LS647 MAX	COM 'LS649 MIN	COM 'LS649 MAX	UNIT
t_{PLH}	Data to output delay	$C_L = 45pF$ $R_L = 667\Omega$		32		35		32		35	ns
t_{PHL}				27		30		27		30	ns
t_{PLH}	Clock to output delay			35		40		35		40	ns
t_{PHL}				45		45		45		45	ns
t_{PLH}	Select to output delay† (data input High)			50		55		50		55	ns
t_{PHL}				45		45		45		45	ns
t_{PLH}	Select to output delay† (data input Low)			60		50		60		50	ns
t_{PHL}				30		40		30		40	ns
t_{PLH}	Output enable delay			40		45		40		45	ns
t_{PHL}				50		50		50		50	ns
t_{PLH}	Direction enable delay			40		45		40		45	ns
t_{PHL}				40		45		40		45	ns

† See Figure 4.

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Test Waveforms

Setup Time/Hold Time

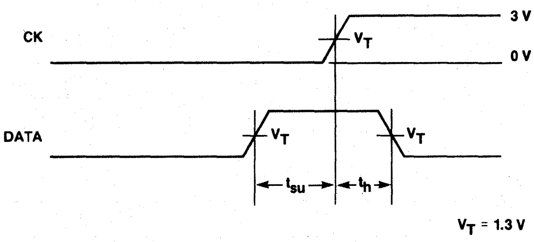


Figure 1.

Bus Data To Bus Output Delay

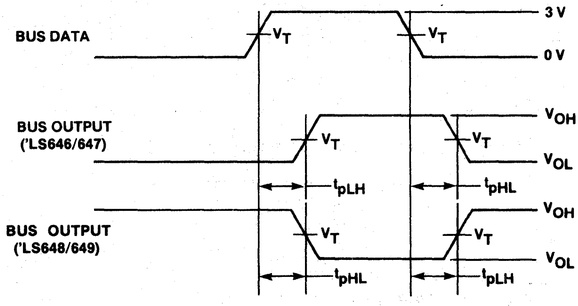


Figure 2. V_T = 1.3 V

CK To Bus Output Propagation Delay Time

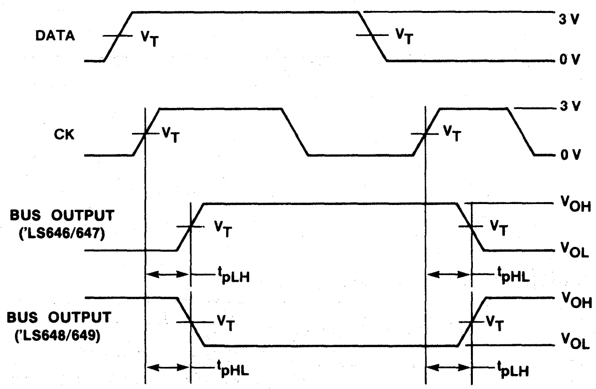


Figure 3 V_T = 1.3 V

Select To Output Delay

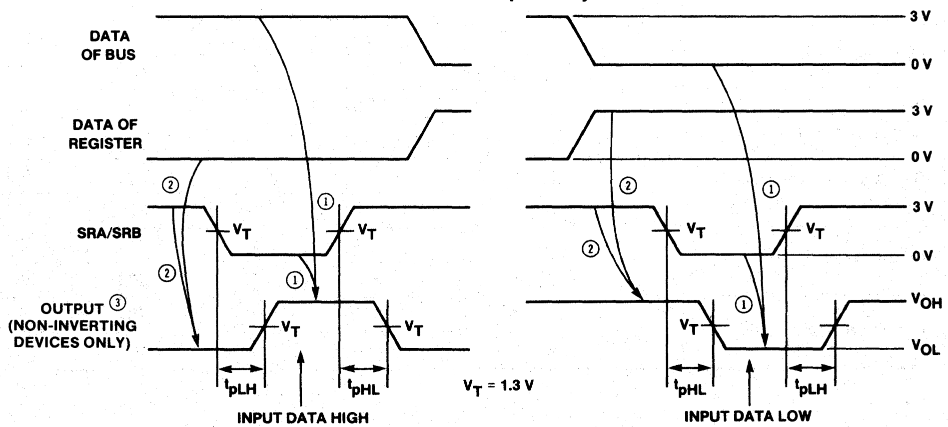


Figure 4

NOTES:
1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Enable/Disable/Direction-Change Delay

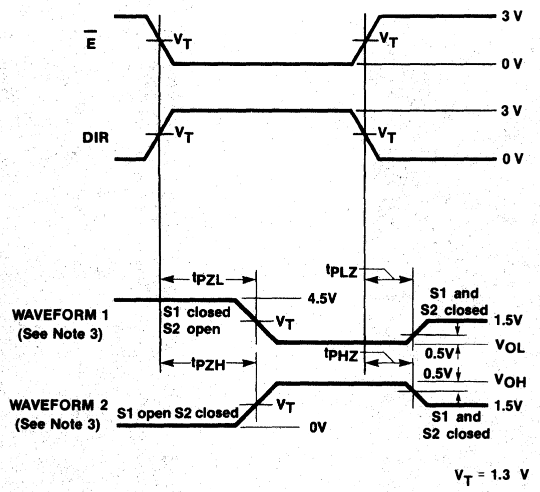
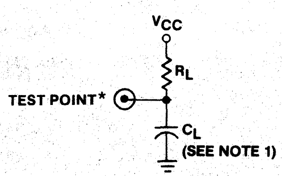
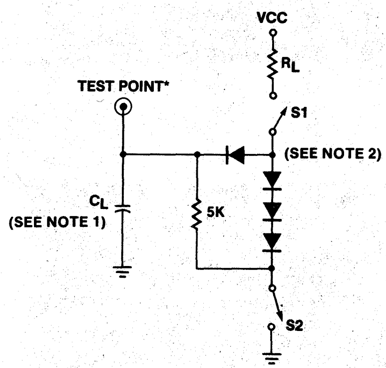


Figure 5

Test Loads



Load Circuit For Open-Collector Outputs



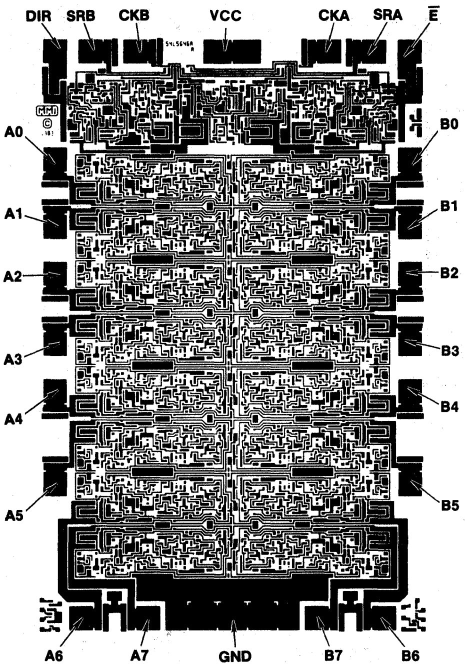
Load Circuit For Three-State Outputs

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

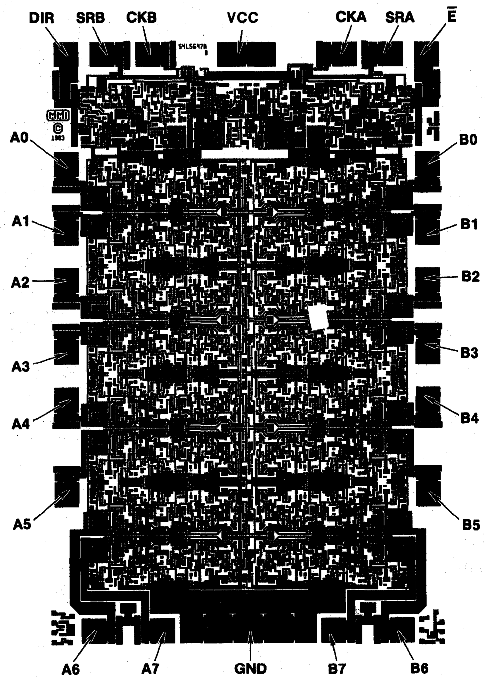
NOTES:
1. C_L includes probe and jig capacitance.
2. All diodes are 1N916 or 1N3064.
3. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. In the examples above the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz $Z_{out} = 50\Omega$ and $t_R = 15$ ns $t_F \leq 6$ ns
6. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

Die Configurations

'LS646

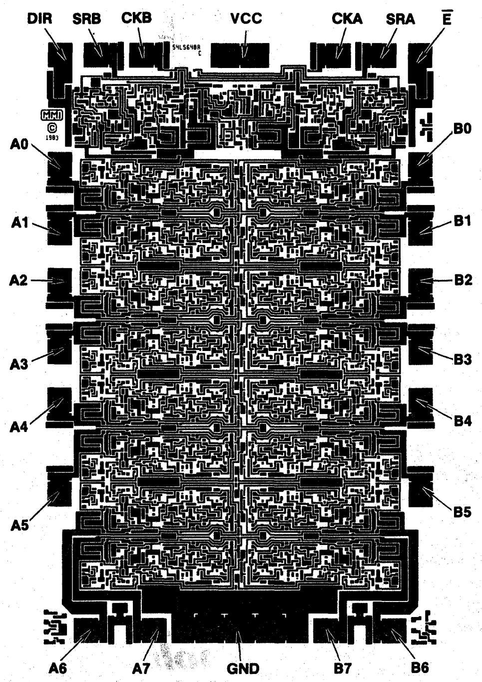


'LS647

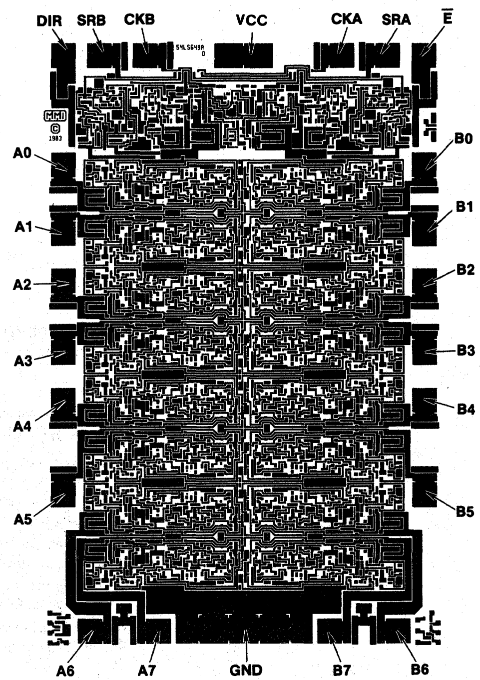


Die Size: 93x127 mil^2

'LS648



'LS649



8-Bit Bus Front-Loading-Latch Transceivers

SN54/74LS651 SN54/74LS652
SN54/74LS653 SN54/74LS654

Features/Benefits

- **Bidirectional bus transceivers and registers**
- **Independent registers for A and B buses**
- **Real-time data transfer or stored data transfer**
- **Simultaneous outputs on both buses**
- **24-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Three-state or open-collector outputs drive bus lines**
- **'LS653/4 are open-collector in A direction, three-state in B direction**

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	OUTPUTS	POWER
SN54LS651	JS,F,L	Mil	Invert	3-state	LS
SN74LS651	NS,JS	Com			
SN54LS652	JS,F,L	Mil	Non-invert		
SN74LS652	NS,JS	Com			
SN54LS653	JS,F,L	Mil	Invert	A bus open-collector; B bus three-state	
SN74LS653	NS,JS	Com			
SN54LS654	JS,F,L	Mil	Non-invert		
SN74LS654	NS,JS	Com			

NOTE: L package here is L28. The other packages are 24-pin.

Description

These 8-bit bus transceivers with 3-state ('LS651, 'LS652) or open-collector ('LS653, 'LS654) outputs have 16 D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS651/653 and 'LS652/654 are given in their respective Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a by-passing path or "feed-through" into a two-way mux, is sometimes called a "front-loading latch."

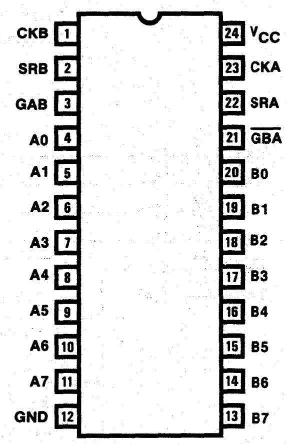
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by two enable lines, GAB and $\overline{\text{GBA}}$.

When GAB is Low and $\overline{\text{GBA}}$ is High, data from the buses can be loaded into registers A and B. When $\overline{\text{GBA}}$ is Low, the A bus is configured for output. When GAB is High, the B bus is configured for output. The A and B buses can be enabled at the same time, to operate as outputs simultaneously.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

Pin Configuration

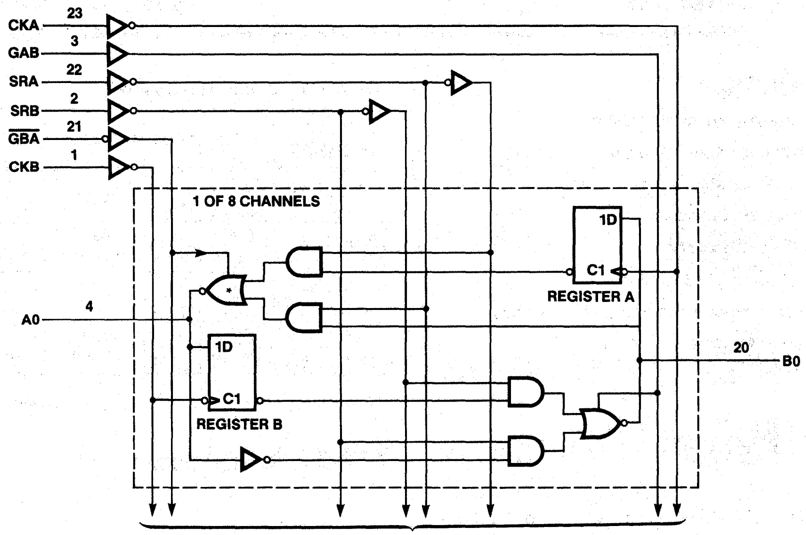
'LS651/652/653/654
8-Bit Bus Front-Loading-Latch Transceivers



TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

Logic Diagrams

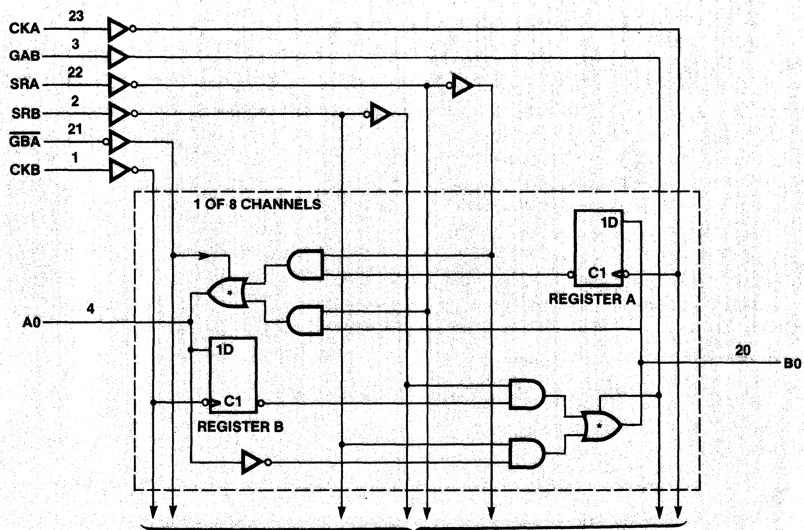
'LS652/654 (Non-Inverting)



TO 7 OTHER CHANNELS

* For the 'LS652 devices, the A bus outputs are 3-state.
For the 'LS654 devices, the A bus outputs are open-collector.
The B bus outputs are 3-state for both devices.

'LS651/653 (Inverting)

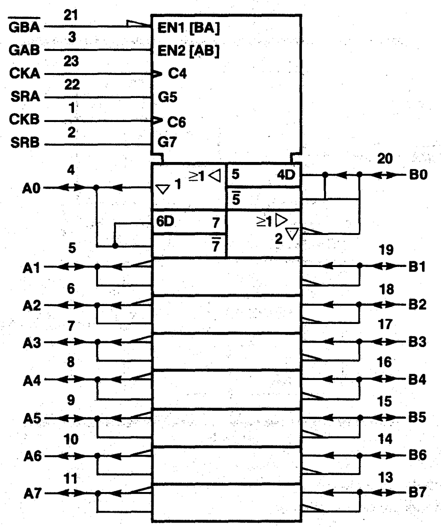


TO 7 OTHER CHANNELS

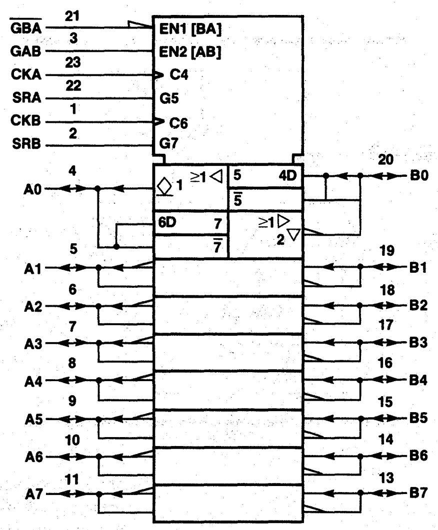
* For the 'LS651 devices, the A bus outputs are 3-state.
For the 'LS653 devices, the A bus outputs are open-collector.
The B bus outputs are 3-state for both devices.

IEEE Symbols

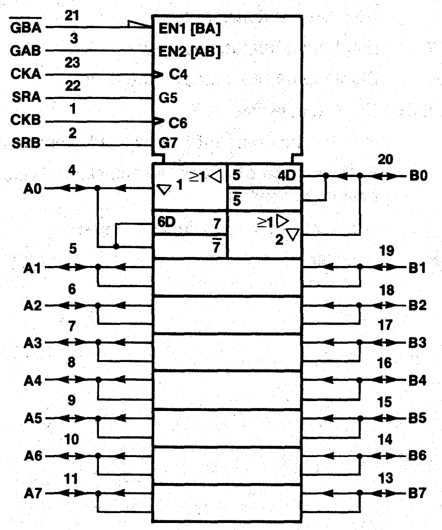
'LS651



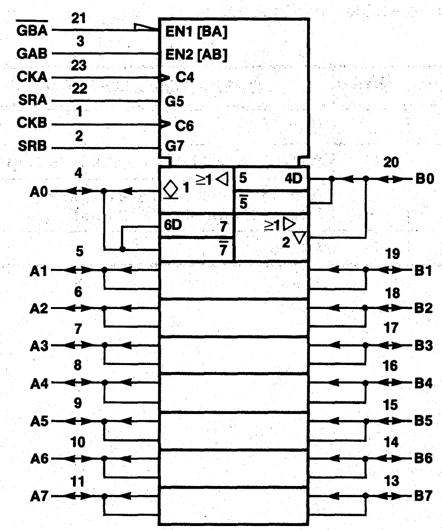
'LS653



'LS652



'LS654



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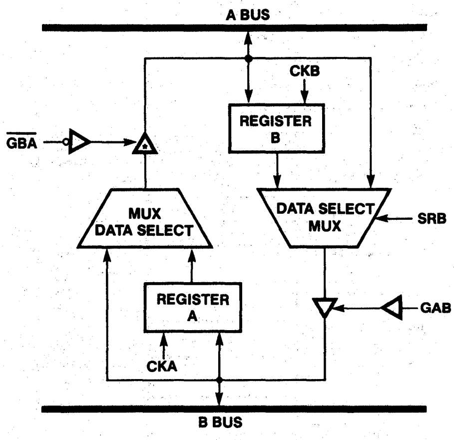
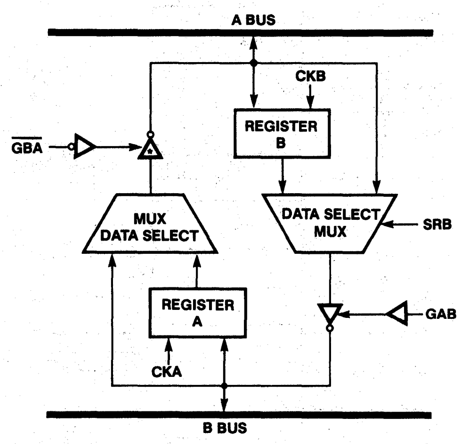
Block Diagrams

'LS652/654 (Non-Inverting)



'LS651/653 (Inverting)



* For the 'LS651/652 devices, the A bus outputs are 3-state.
For the 'LS653/654 devices, the A bus outputs are open-collector.
The B bus outputs are 3-state for both devices.

Function Table Nomenclature Description

GAB: To enable the A-to-B operation.

$\overline{\text{GBA}}$: To enable the B-to-A operation.

GAB	$\overline{\text{GBA}}$	OPERATION DIRECTION
L	L	B to A
L	H	A and B buses both are inputs (storage)
H	L	A and B buses both are outputs (Transfer stored data to bus)
H	H	A to B

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for Register A/B.

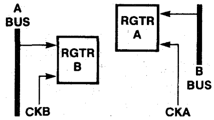
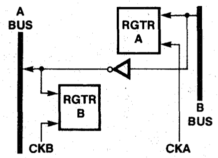
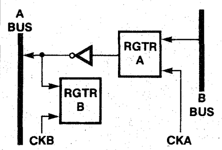
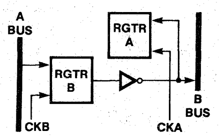
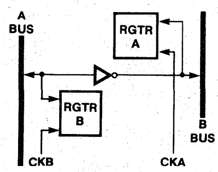
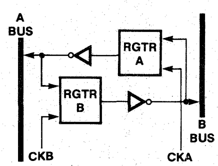
X: H or L state irrelevant ("Don't Care" conditions).

↑: Positive edge of CK causes clocking, if clocking enable is asserted.

UC: H or L or ↓ case (nonclocked operation).

RGTR: Register.

Bus Operation for 'LS651/653

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS651/653
	GAB	$\overline{GBA}$	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	L	H	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time $\overline{B}$ bus data → A bus
								UC	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR B
								↑	UC	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A Real time $\overline{B}$ bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR $\overline{A}$ data → A bus
								UC	↑	RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
Real time A-to-B Operation	H	H	X	L	Input	Output		UC	UC	Real time $\overline{A}$ bus data → B bus
								UC	↑	Real time $\overline{A}$ bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A
								↑	↑	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	H	H	X	H	Input	Output		UC	UC	RGTR $\overline{B}$ data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus
								↑	UC	RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
Transfer Stored Data	H	L	H	H	Output	Output		UC	UC	RGTR $\overline{A}/\overline{B}$ data → A/B bus
								UC	↑	RGTR $\overline{A}/\overline{B}$ data → A/B bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	RGTR $\overline{A}/\overline{B}$ data → A/B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	RGTR $\overline{A}/\overline{B}$ data → A/B bus RGTR $\overline{A}$ data → RGTR B RGTR $\overline{B}$ data → RGTR A

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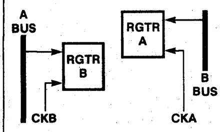
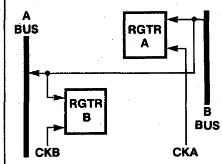
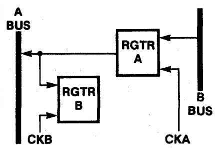
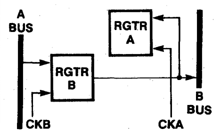
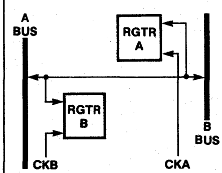
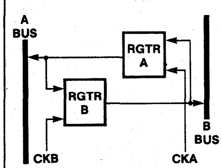
Bus Operation for 'LS652/654

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS652/654
	GAB	$\overline{GBA}$	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	L	H	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time B bus data → A bus
								UC	↑	Real time B bus data → A bus Real time B bus data → RGTR B
								↑	UC	Real time B bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR A data → A bus
								UC	↑	RGTR A data → A bus RGTR A data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR A data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
Real time A-to-B Operation	H	H	X	L	Input	Output		UC	UC	Real time A bus data → B bus
								UC	↑	Real time A bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time A bus data → B bus Real time A bus data → RGTR A
								↑	↑	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	H	H	X	H	Input	Output		UC	UC	RGTR B data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR B data → B bus
								↑	UC	RGTR B data → B bus RGTR B data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A
Transfer Stored Data	H	L	H	H	Output	Output		UC	UC	RGTR A/B data → A/B bus
								UC	↑	RGTR A/B data → A/B bus RGTR A data → RGTR B
								↑	UC	RGTR A/B data → A/B bus RGTR B data → RGTR A
								↑	↑	RGTR A/B data → A/B bus RGTR A data → RGTR B RGTR B data → RGTR A

Absolute Maximum Ratings

Supply voltage, V_{CC} .... 7.0 V
Input voltage, ... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		-55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS651	20 ↑			20 ↑			ns
		'LS652	20 ↑			20 ↑			
t_h	Hold time	'LS651	0 ↑			0 ↑			ns
		'LS652	0 ↑			0 ↑			
I_{OH}	High-level output current				-12			-15	mA
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5			-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			-0.4			-0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-400			-400	μA
I_{OZH}				V_O = 2.7 V			20			20	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		-40		-225	-40		-225	mA
I_{CC}	Supply current	'LS-651	V_{CC} = MAX	Outputs High			145			145	mA
				Outputs Low			165			165	
				Outputs disabled			165			165	
		'LS-652		Outputs High			145			145	
				Outputs Low			165			165	
				Outputs disabled			165			165	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

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Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS651 MIN	'LS651 MAX	'LS652 MIN	'LS652 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		15		15	ns
t_{PHL}				15		20	ns
t_{PLH}	Clock to output delay			20		20	ns
t_{PHL}				30		30	ns
t_{PLH}	Select to output delay † (data input High)			35		35	ns
t_{PHL}				20		25	ns
t_{PLH}	Select to output delay † (data input Low)			35		35	ns
t_{PHL}				30		20	ns
t_{PZL}	$\overline{GBA}$ to A bus output enable delay			25		25	ns
t_{PZH}				20		20	ns
t_{PLZ}	$\overline{GBA}$ to A bus output disable delay	C_L = 5pF R_L = 667Ω		25		25	ns
t_{PHZ}				35		35	ns
t_{PZL}	GAB to B bus output enable delay	C_L = 45pF R_L = 667Ω		30		30	ns
t_{PZH}				25		25	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω		25		25	ns
t_{PHZ}				35		35	ns

† See Figure 4.

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIL 'LS651 MIN	MIL 'LS651 MAX	MIL 'LS652 MIN	MIL 'LS652 MAX	COM 'LS651 MIN	COM 'LS651 MAX	COM 'LS652 MIN	COM 'LS652 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		20		20		15		20	ns
t_{PHL}				20		25		17		22	ns
t_{PLH}	Clock to output delay			25		25		22		22	ns
t_{PHL}				35		35		30		30	ns
t_{PLH}	Select to output delay † (data input High)			40		40		35		35	ns
t_{PHL}				25		30		25		28	ns
t_{PLH}	Select to output delay † (data input Low)			40		40		35		35	ns
t_{PHL}				35		25		30		22	ns
t_{PZL}	$\overline{GBA}$ to A bus output enable delay			30		30		25		25	ns
t_{PZH}				25		25		20		20	ns
t_{PLZ}	$\overline{GBA}$ to A bus output disable delay	C_L = 5pF R_L = 667Ω		35		30		30		28	ns
t_{PHZ}				40		45		40		40	ns
t_{PZL}	GAB to B bus output enable delay	C_L = 45pF R_L = 667Ω		35		35		30		32	ns
t_{PZH}				30		30		25		25	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω		35		35		30		30	ns
t_{PHZ}				40		45		35		40	ns

† See Figure 4.

Absolute Maximum Ratings

Supply voltage, V_{CC} .... 7.0 V
Input voltage, ... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		-55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS653	20↑			20↑			ns
		'LS654	20↑			20↑			
t_h	Hold time	'LS653	0↑			0↑			ns
		'LS654	0↑			0↑			
V_{OH}	High-level output voltage (A bus only)				5.5			5.5	V
I_{OH}	High-level output current (B bus only)				-12			-15	mA
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions, ↓ for the high-to-low transitions.

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Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current: A or B All others	V_{CC} = MAX	V_I = 5.5 V V_I = 7 V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage (B bus only)	V_{CC} = MIN V_{IL} = MAX V_{IH} = 2 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
			I_{OH} = MAX	2			2			
I_{OH}	High-level output current (A bus only)	V_{CC} = MIN V_{IL} = MAX V_{IH} = 2 V	V_{OH} = 5.5 V			100			100	μA
I_{OZL}	Off-state output current (B bus only)	V_{CC} = MAX V_{IL} = MAX V_{IH} = 2 V	V_O = 0.4 V			−400			−400	μA
I_{OZH}			V_O = 2.7 V (B bus only)			20			20	μA
I_{OS}	Output short-circuit current* (B bus only)	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	V_{CC} = MAX, 'LS-653	Outputs High			145			145	mA
			Outputs Low			165			165	
			Outputs disabled			165			165	
		V_{CC} = MAX, 'LS-654	Outputs High			145			145	
			Outputs Low			165			165	
			Outputs disabled			165			165	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS* (See Test Load/Waveforms)	'LS653 MIN	'LS653 MAX	'LS654 MIN	'LS654 MAX	UNIT
t_{PLH}	Data to A bus output delay	C_L = 45pF R_L = 667Ω		25		25	ns
t_{PHL}				20		25	ns
t_{PLH}	Data to B bus output delay			15		15	ns
t_{PHL}				15		20	ns
t_{PLH}	Clock to A bus output delay			30		30	ns
t_{PHL}				30		30	ns
t_{PLH}	Clock to B bus output delay			20		20	ns
t_{PHL}				30		30	ns
t_{PLH}	Select to A bus † output delay (data input High)			45		45	ns
t_{PHL}				25		30	ns
t_{PLH}	Select to A bus † output delay (data input Low)			40		45	ns
t_{PHL}				30		25	ns
t_{PLH}	Select to B bus † output delay (data input High)			35		35	ns
t_{PHL}				25		25	ns
t_{PLH}	Select to B bus † output delay (data input Low)			35		35	ns
t_{PHL}				30		20	ns
t_{PLH}	$\overline{GBA}$ to A bus output enable delay			35		35	ns
t_{PHL}				25		30	ns
t_{PZL}	GAB to B bus output enable delay			30		30	ns
t_{PZH}				25		25	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω		25		25	ns
t_{PHZ}				35		35	ns

* For A bus, the test load will refer to the open-collector test load. See Figure 6.
For B bus, the test load will refer to the three-state test load. See Figure 7.

† See Figure 4.

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS* (See Test Load/Waveforms)	MIL 'LS653 MIN	MIL 'LS653 MAX	MIL 'LS654 MIN	MIL 'LS654 MAX	COM 'LS653 MIN	COM 'LS653 MAX	COM 'LS654 MIN	COM 'LS654 MAX	UNIT
t_{PLH}	Data to A bus output delay	C_L = 45pF R_L = 667Ω		30		30		28		30	ns
t_{PHL}				25		30		23		28	ns
t_{PLH}	Data to B bus output delay			20		20		18		18	ns
t_{PHL}				20		25		18		20	ns
t_{PLH}	Clock to A bus output delay			40		40		35		35	ns
t_{PHL}				40		40		35		35	ns
t_{PLH}	Clock to B bus output delay			25		25		23		23	ns
t_{PHL}				35		35		30		30	ns
t_{PLH}	Select to A bus output † delay (data input High)			50		50		45		48	ns
t_{PHL}				30		40		25		35	ns
t_{PLH}	Select to A bus output † delay (data input Low)			45		55		43		50	ns
t_{PHL}				35		30		30		28	ns
t_{PLH}	Select to B bus output † delay (data input High)			40		35		35		35	ns
t_{PHL}				25		35		25		30	ns
t_{PLH}	Select to B bus output † delay (data input Low)			40		45		35		40	ns
t_{PHL}				35		25		30		23	ns
t_{PLH}	$\overline{GBA}$ to A bus output enable delay			40		35		35		35	ns
t_{PHL}				30		40		28		35	ns
t_{PZL}	GAB to B bus output enable delay			35		35		30		33	ns
t_{PZH}				30		30		25		28	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω		35		35		30		30	ns
t_{PHZ}				40		45		38		40	ns

* For A bus, the test load will refer to the open-collector test load. See Figure 6.
For B bus, the test load will refer to the three-state test load. See Figure 7.

† See Figure 4.

Test Waveforms

Setup Time/Hold Time

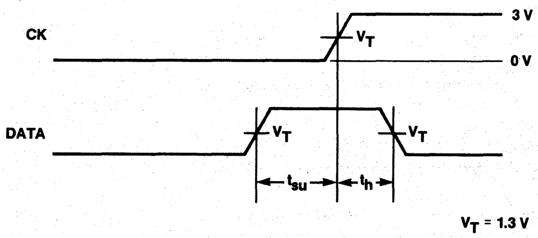


Figure 1.

Bus Data To Bus Output Delay

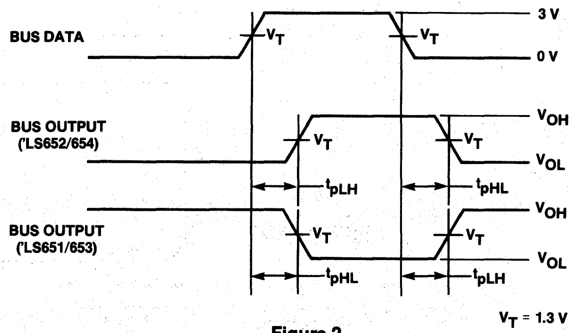


Figure 2.

CK To Bus Output Propagation Delay Time

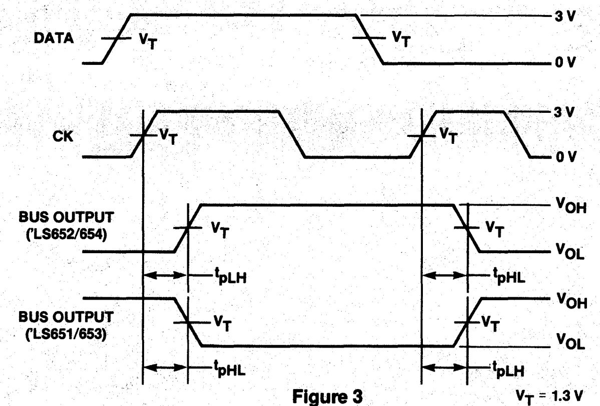


Figure 3

Select To Output Delay

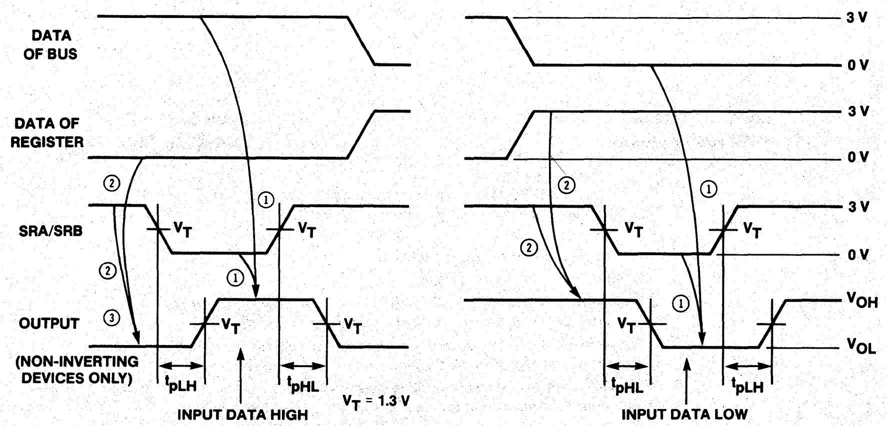


Figure 4

NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Enable/Disable Delay

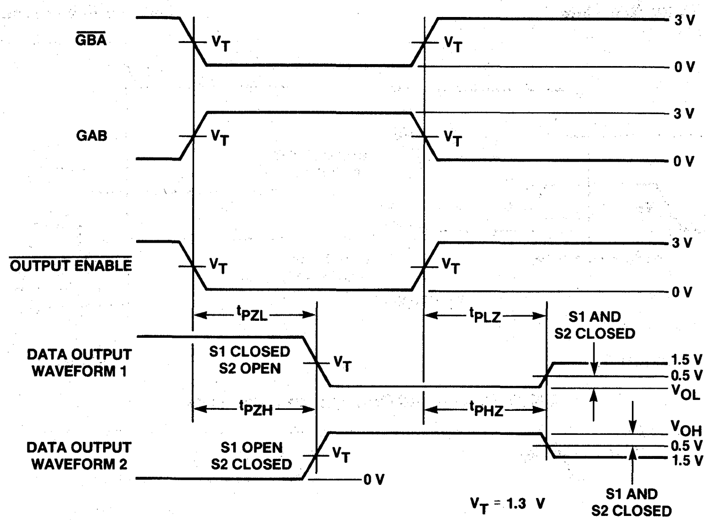
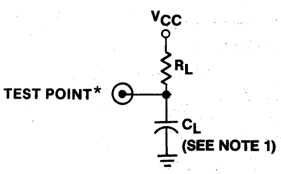
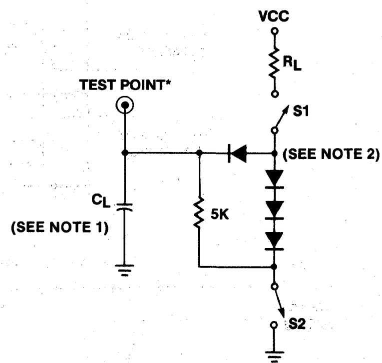


Figure 5

Test Loads



Load Circuit For Open-Collector Outputs



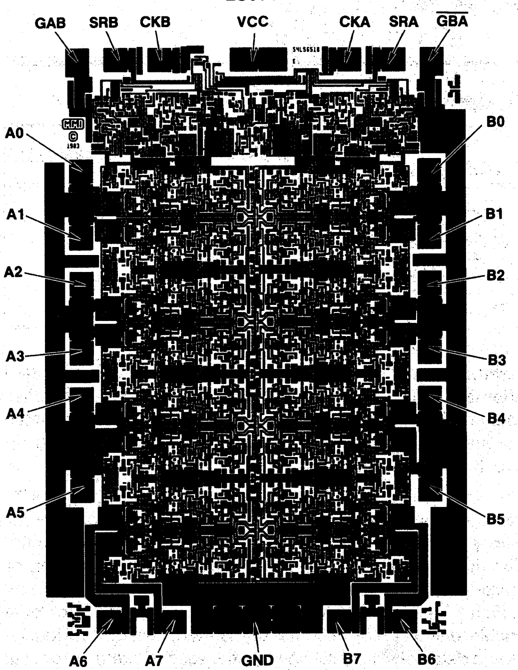
Load Circuit For Three-State Outputs

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

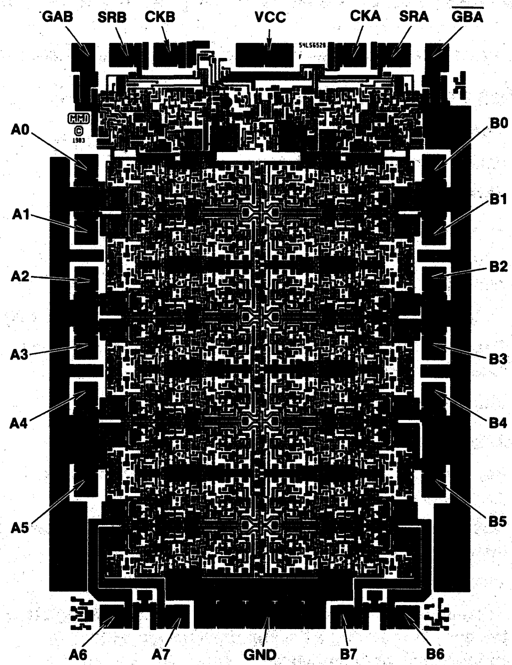
NOTES:
1. C_L includes probe and jig capacitance.
2. All diodes are 1N916 or 1N3064.
3. Waveform 1 is for an output with internal conditions such that output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that output is high except when disabled by the output control.
4. In the examples above the phase relationships between input and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the follow characteristics: PRR ≤ 1 MHZ $t_R \leq 15$ ns $t_F \leq 6$ ns $Z_{out} = 50\Omega$
6. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

Die Configurations

'LS651

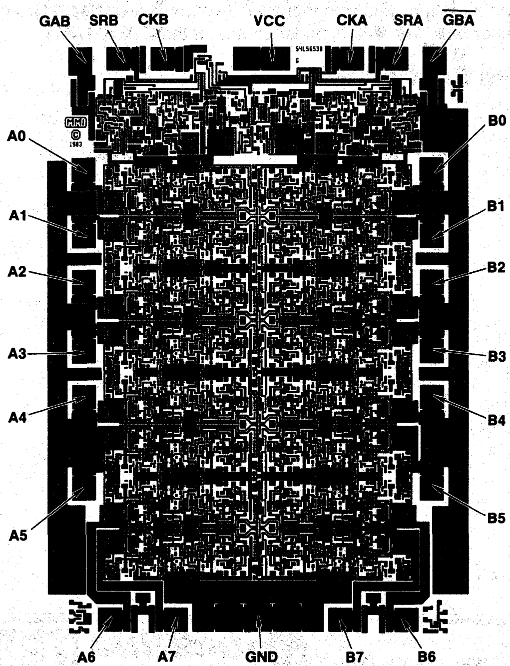


'LS652

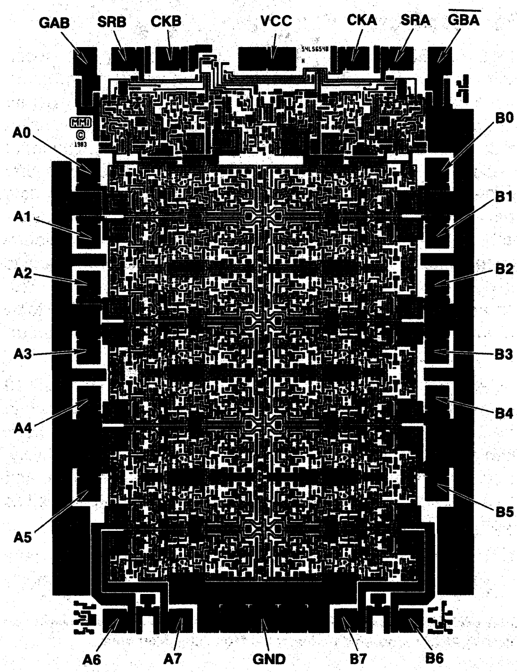


Die Size: 93x127 mil^2

'LS653



'LS654



8-Bit Two-Stage Pipelined Register/Latch

SN54/74LS548 SN54/74LS549

Feature/Benefits

- Two 8-bit high-speed registers/latches
- Faster than other LS-TTL registers/latches
- Three-state outputs drive bus lines
- 24-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Multiplexer selects either rank at input/output
- Output can drive bus directly: I_{OL} 32 mA (com), 24 mA (mil)
- Registers/latches configurable for nose-to-tail or side-by-side operation
- Individual clock/gate enables for each rank

Applications

- Registers for pipelined arithmetic units or digital signal processors
- Bus monitor for popular 8-bit microprocessors to restart instructions upon virtual memory page fault
- Video display character/attribute pipelined registers
- Sequence/state generator for systems: dual-rank registers/latches allow storing a backup previous state for redundancy, or diagnostics
- Two-stage buffer for pipelined interfacing input/output

Description

The 54/74LS548 and 54/74LS549 contain a pair of high-speed 8-bit registers ('LS548) or latches ('LS549) which perform various pipeline storage functions. Two control pins govern a pair of internal multiplexers, as shown in the block diagrams; using these, several useful data paths can be configured. The input selection multiplexer determines the source of data to the second register/latch, as controlled by the INSEL line. In this way, data from either the D7-D0 inputs, or the outputs of the first register/latch, are stored in the second register/latch. The output selection multiplexer determines the source of data that will be sent to the outputs Y7-Y0. This multiplexer is controlled by the OUTSEL line, and allows either the first or second register/latch data to be output. The outputs are fully buffered, provide high-drive current, and allow three-state control through the $\overline{OE}$ line.

The arrangement of registers/latches within the 'LS548/'LS549 can be thought of a two 8-bit storage ranks, rank 1 and rank 2. The 'LS548 has a common clock line CK, and separate clock enables $\overline{CKE1}$ and $\overline{CKE2}$ for rank 1 and rank 2 respectively. In contrast, the 'LS549 operates as a flow-through latch, and has separate latch enables $\overline{G1}$ and $\overline{G2}$ for each rank, as well as a common latch-enable input G.

In the 'LS548, data present at the D7-D0 inputs are stored in rank 1 on the positive edge of CK, if $\overline{CKE1}$ has been previously

Ordering Information

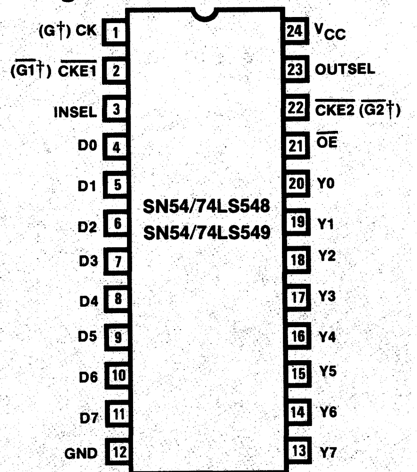
PART NUMBER	PKG	TEMP	TYPE	POWER
SN54LS548	JS,F,L	Mil	Register	LS
SN74LS548	NS,JS	Com		
SN54LS549	JS,F,L	Mil	Latch	
SN74LS549	NS,JS	Com		

* NOTE: L package here is L28. The other packages are 24-pin.

asserted. Data for rank 2 are stored similarly, if $\overline{CKE2}$ is asserted prior to the clock. In the 'LS549, data pass through the latches when the latch controls ($\overline{G1}$ or $\overline{G2}$) for either rank are enabled simultaneously with the common latch enable G. Data remain in a rank when the latch controls are disabled, or 'unasserted'.

The clock/gate control lines are used with the INSEL and OUTSEL controls for flexible data storage and movement operations. Two representative examples are shown in Figure 1 (a) and 1 (b). The first example is a classical 2-stage pipelined register, or 'nose-to-tail' configuration. Data at D7-D0 are first stored in rank 1, then stored in rank 2 on the next clock/gate. If the clock/gate enable for either rank becomes unasserted, then the previously-stored data are simply retained. In the second example, data at D7-D0 are stored in either or both ranks if the respective clock/gate enable signals are asserted. In this 'side-by-side' configuration, data sent to the Y7-Y0 outputs are selected from either rank 1 or rank 2, under control of the OUTSEL line.

Pin Configuration



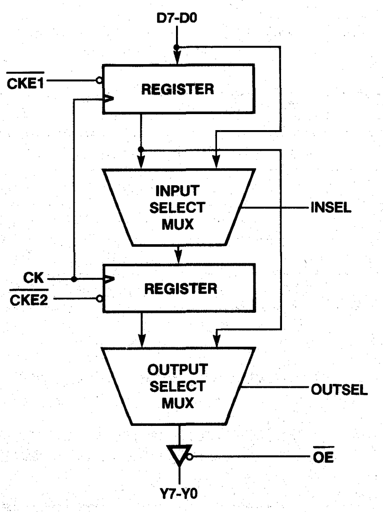
† For SN54/74LS549.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

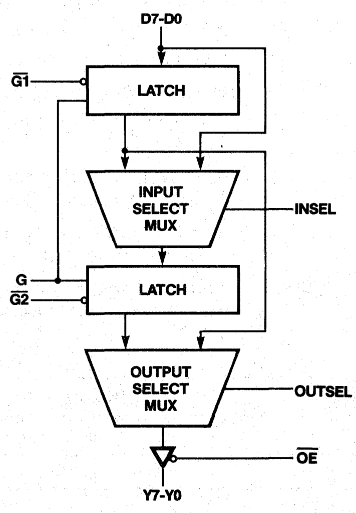
Monolithic Memories

Block Diagrams

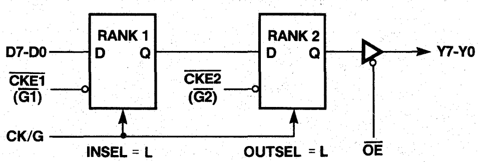
'LS548



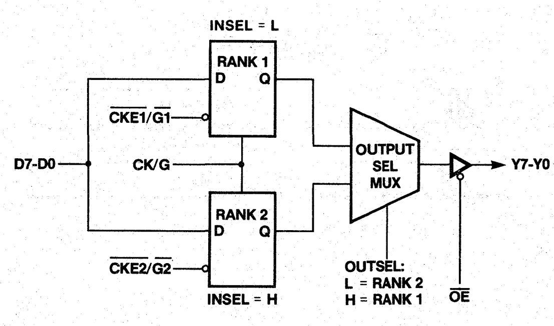
'LS549



Typical Configurations



(a) Nose-to-Tail



(b) Side-by-Side

Figure 1

Function Table Nomenclature Description

Rank 1-Q or Rank 2-Q = Data available at the internal flip-flop/latch outputs for the 8 rank 1 or rank 2 registers/latches respectively.

D = Data at the D0-D7 input pins.

Y = Data at the Y0-Y7 output pins.

X = H or L state irrelevant ("don't care" conditions)

Q_0 = Previous states of the internal register/latch data are retained.

Z = Indicates that the Y0-Y7 outputs are in high-impedance state.

INSEL = Input select mux control pin; determines the source of input data for rank 2.

INSEL	RANK 2 INPUT
L	Rank 1
H	D

OUTSEL = Output select mux control pin; selects either rank 1 or rank 2 for output.

OUTSEL	OUTPUT
L	Rank 2
H	Rank 1

$\overline{OE}$ = Output enable pin.

$\overline{OE}$	OUTPUT
L	Rank 1 or Rank 2
H	Hi-Z

↑ = Positive edge of CK causes clocking, if clocking is enabled.

CK = The common clock line for the 54/74LS548.

$\overline{CKE1}$/$\overline{CKE2}$ = Clock enable line for the rank 1/rank 2 register in the 54/74LS548.

CK	$\overline{CKE1}$	$\overline{CKE2}$	RANK 1	RANK 2
L or H or ↓	X	X	Disabled	Disabled
↑	L	L	Enabled	Enabled
↑	L	H	Enabled	Disabled
↑	H	L	Disabled	Enabled
X	H	H	Disabled	Disabled

G = The common latch control line for the 54/74LS549.

$\overline{G1}$/$\overline{G2}$ = Latch enable line for the rank 1/rank 2 latch in the 54/74LS549.

G	$\overline{G1}$	$\overline{G2}$	RANK 1	RANK 2
L	L	L	Enabled (Flush)	Enabled (Flush)
L	L	H	Enabled (Flush)	Disabled (Freeze)
L	H	L	Disabled (Freeze)	Enabled (Flush)
L	H	H	Disabled (Freeze)	Disabled (Freeze)
H	X	X	Enabled (Flush)	Enabled (Flush)

'LS548 Function Table

CK	$\overline{CKE1}$	RANK 1	$\overline{CKE2}$	INSEL	RANK 2
L or H or ↓	X	Q0	X	X	Q0
↑	H	Q0	H	X	Q0
↑	L	D	H	X	Q0
↑	L	D	L	L	Rank 1-Q
↑	L	D	L	H	D
↑	H	Q0	L	L	Rank 1-Q
↑	H	Q0	L	H	D

'LS549 Function Table

G	$\overline{G1}$	RANK 1	$\overline{G2}$	INSEL	RANK 2
L	L	D	L	L	Rank 1-Q
L	L	D	L	H	D
L	L	D	H	X	Q0
L	H	Q0	L	L	Rank 1-Q
L	H	Q0	L	H	D
L	H	Q0	H	X	Q0
H	X	D	X	X	D

'LS548/549 Output Function Table

OUTSEL	$\overline{OE}$	Y
L	L	Rank 2-Q
H	L	Rank 1-Q
X	H	Hi-Z

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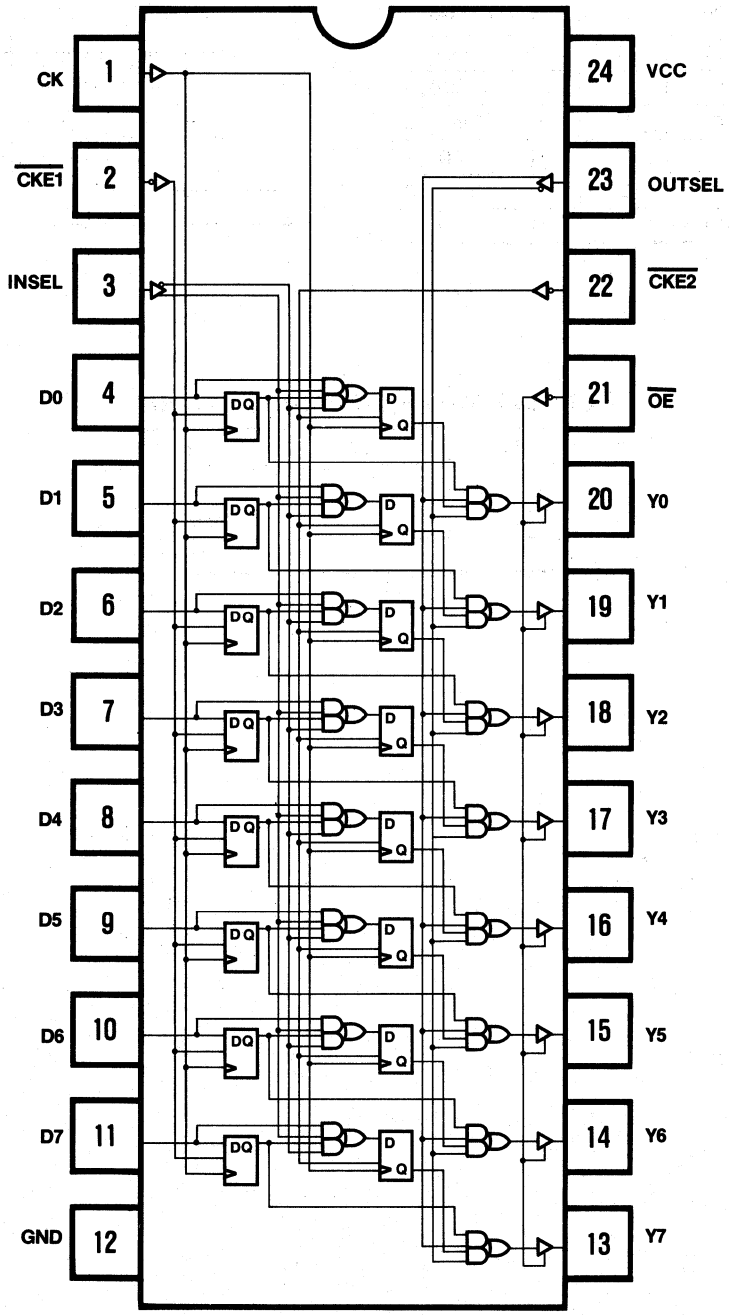
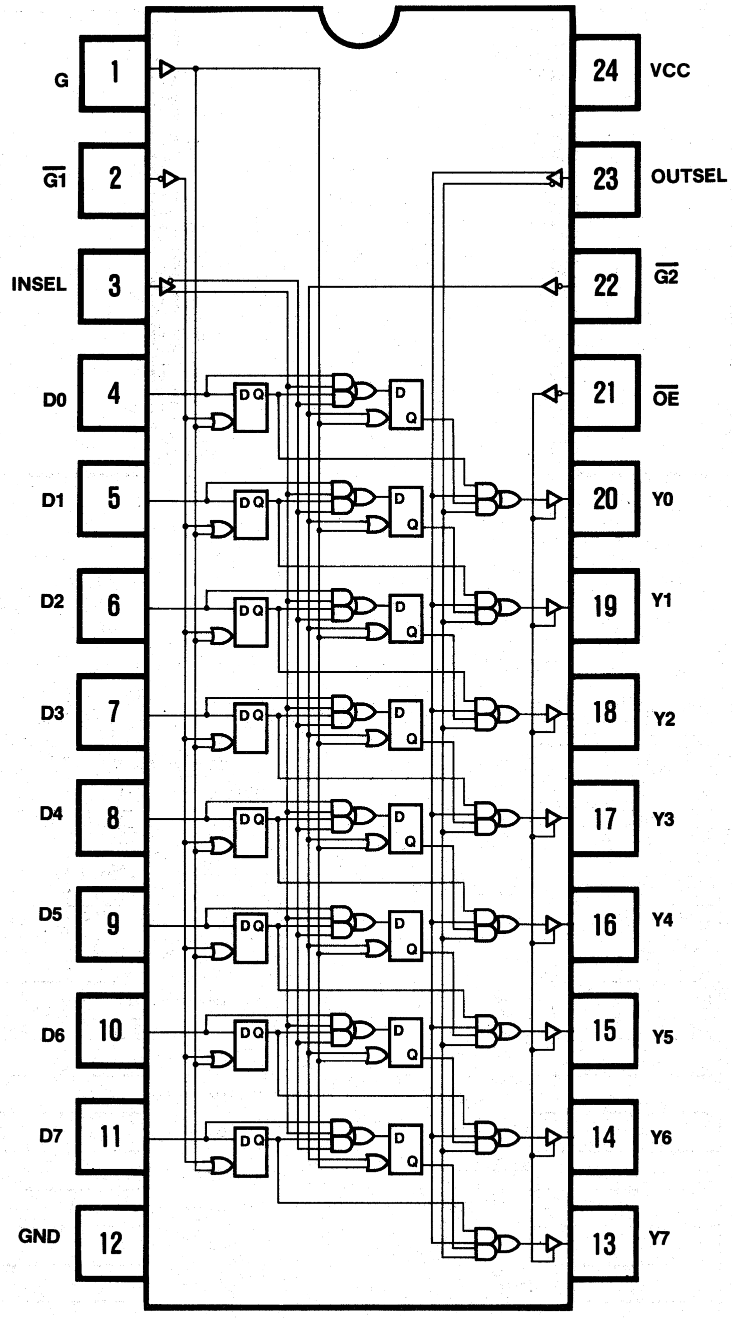
Logic Diagram

54/74LS548 Pipelined Register



Logic Diagram

54/74LS549 Pipelined Latch



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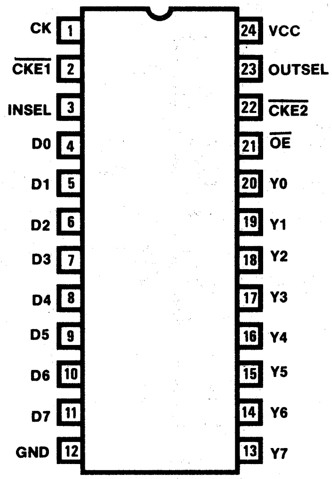
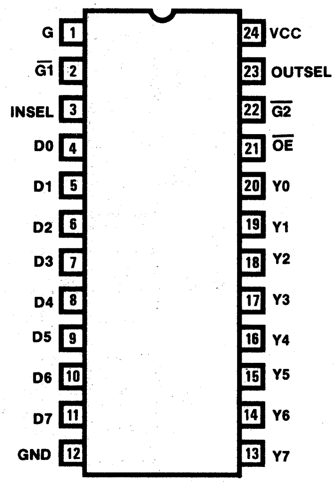
Pin Configurations

'LS548

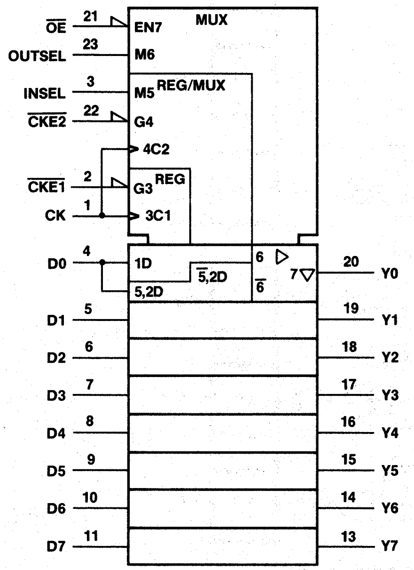


'LS549

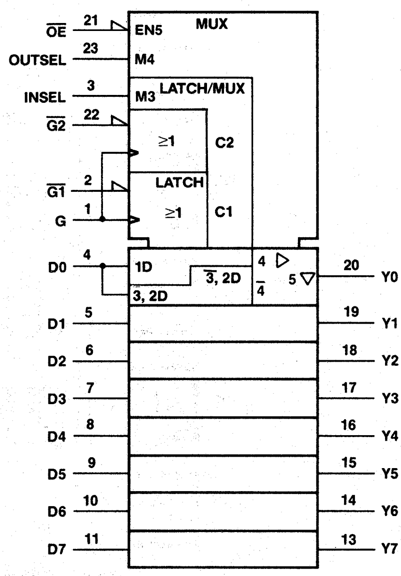


IEEE Symbols

'LS548



'LS549



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER				MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage				4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature				−55		125	0		75	°C
t_w	Width of CK, G, $\overline{G1}$, $\overline{G2}$	High	'LS548	CK	15			11			ns
			'LS549	G							
		Low	'LS548	CK	15			11			ns
			'LS549	$\overline{G1}$, $\overline{G2}$	18			16			
t_{su}	Setup time for D, G, $\overline{GX}$		'LS548	CK	20↑			15↑			ns
			'LS549	G	10↓			6↓			
				$\overline{G1}$, $\overline{G2}$	17↑			4↑			
t_h	Hold time for D, G, $\overline{GX}$		'LS548	CK	0↑			0↑			ns
			'LS549	G	12↓			10↓			
				$\overline{G1}$, $\overline{G2}$	5↑			5			
$t_{su\text{-}CKEX}$	Setup time for clock enables $\overline{CKE1}$, $\overline{CKE2}$ ('LS548 only)				15↑			10↑			ns
$t_{h\text{-}CKEX}$	Hold time for clock enable $\overline{CKE1}$, $\overline{CKE2}$, ('LS548 only)				8↑			5↑			ns
$t_{su\text{-}INSEL}$	Setup time for INSEL[1]				30			25			ns
$t_{h\text{-}INSEL}$	Hold time for INSEL[2]				0			0			ns

NOTES: 1. This is the minimum setup time needed for INSEL prior to the rising edge of the clock/$\overline{GX}$, and to the falling edge of the G, to ensure data transfer to rank 2.
2. This is the minimum hold time needed for INSEL after the rising edge of the clock/$\overline{GX}$, and to the falling edge of the G, to ensure data transfer to rank 2.
↑↓ the arrow indicates the transition of the clock/gate input used for reference:
↑ for the low-to-high transitions,
↓ for the high-to-low transitions.

12

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18 mA			–1.5			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	D or Y			–250			–250	µA
			All others			–400			–400	
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V			20			20	µA
I_I	Maximum input current: D or Y	V_{CC} = MIN	V_I = 5.5 V			0.1			0.1	mA
	Maximum input current: All others		V_I = 7 V							
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 32 mA					0.35	0.5	V
			I_{OL} = 24 mA			0.5				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = –1 mA	2.4	3.4					V
			I_{OH} = –2.6 mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			–20			–20	µA
I_{OZH}			V_O = 2.7 V							
I_{OS}	Output short-circuit current*	V_{CC} = MAX		–30		–130	–30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	'LS548			150			150	mA
			'LS549			160			160	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS548 MIN	'LS548 MAX	'LS549 MIN	'LS549 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF, R_L = 280Ω, $\overline{OE}$ = L	50				MHz
t_{PLH}/t_{PHL}	CK, $\overline{G1}$, or $\overline{G2}$ to output delay			18		22	ns
t_{PLH}/t_{PHL}	G to output delay ('LS549)					23	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS549)					16	ns
t_{PLH}/t_{PHL}	Output multiplexer control OUTSEL to output delay			20		20	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF, R_L = 280Ω		18		18	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF, R_L = 280Ω		15		15	ns

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIL 'LS548 MIN	MIL 'LS548 MAX	MIL 'LS549 MIN	MIL 'LS549 MAX	COM 'LS548 MIN	COM 'LS548 MAX	COM 'LS549 MIN	COM 'LS549 MAX	UNIT
f_{MAX}	Maximum clock frequency		33				45				MHz
t_{PLH}/t_{PHL}	CK, $\overline{G1}$ or $\overline{G2}$ to output delay	C_L = 45 pF, R_L = 280Ω, $\overline{OE}$ = L		25		26		20		24	ns
t_{PLH}/t_{PHL}	G to output delay ('LS549)					28				25	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS549)					24				18	ns
t_{PLH}/t_{PHL}	Output multiplexer control OUTSEL to output delay			27		27		22		22	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF, R_L = 280Ω		23		23		20		20	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF, R_L = 280Ω		20		20		17		17	ns

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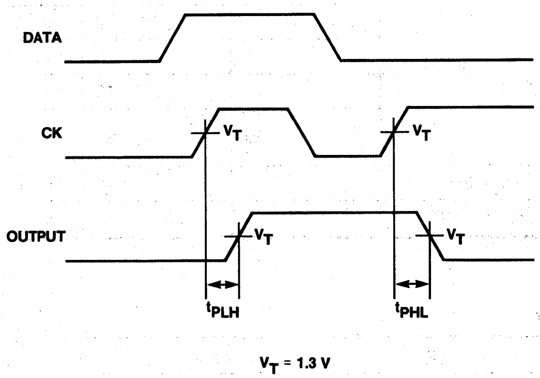
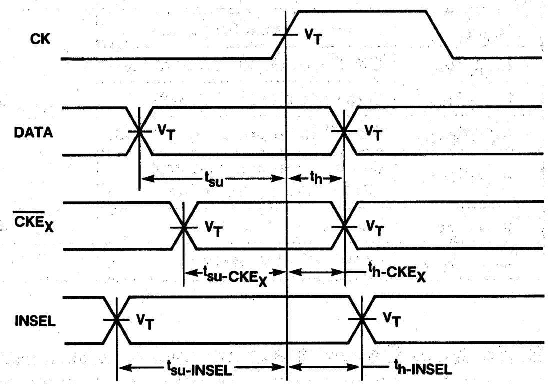
Test Waveforms

'LS548

CK to Output Delay

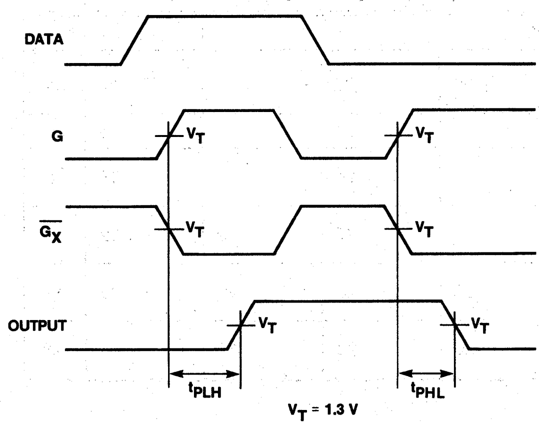


Setup and Hold

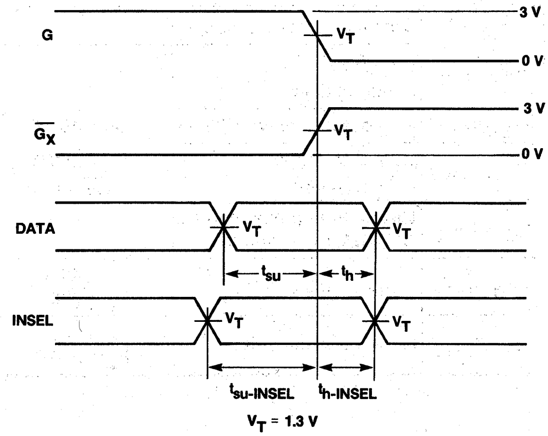


'LS549

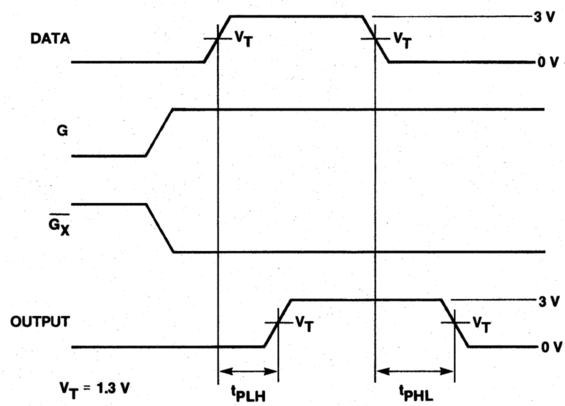
G to Output Delay



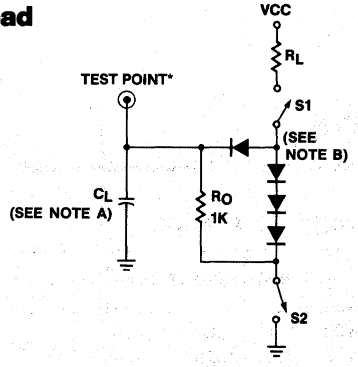
Setup and Hold



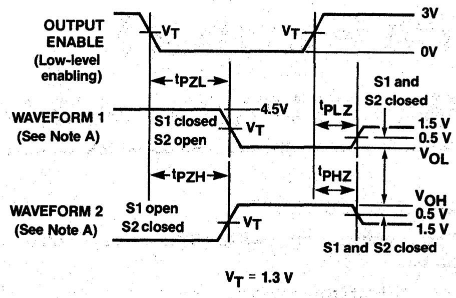
Data D to Output Delay



Test Load



Load Circuit for Three-state Outputs



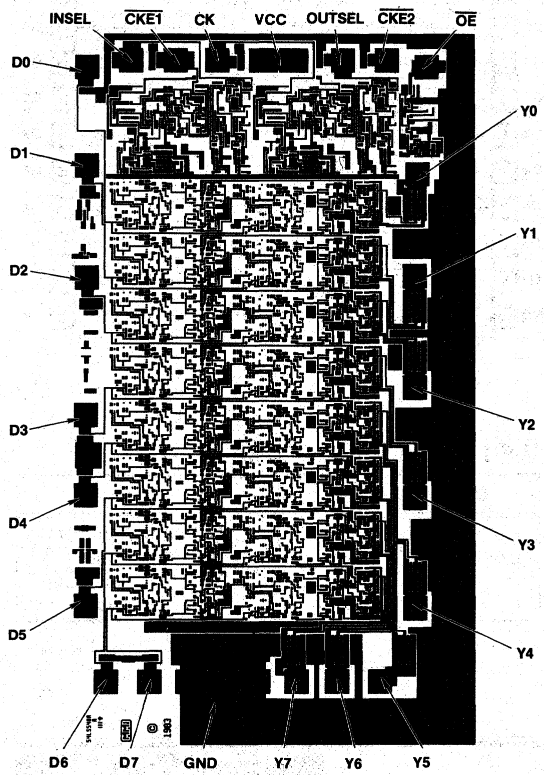
'LS548/549 Enable and Disable

* The "TEST POINT" is drived by the output under test, and observed by instrumentation.

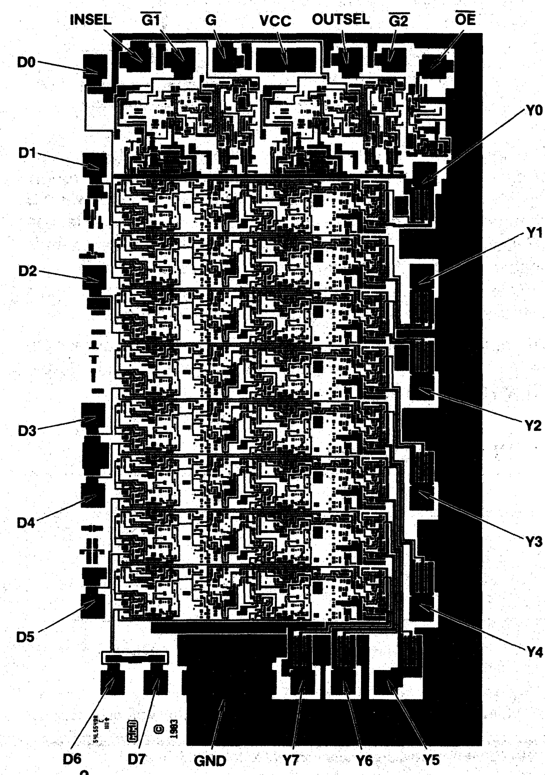
NOTES:
- A. C_L includes probe and Jig capacitance.
- B. All diodes are 1N916 or 1N3064.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
  Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω and:
- F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

Die Configurations

SN54/74LS548



SN54/74LS549



Die Size: 89x150 mil^2

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8-Bit Latch/Register with Readback

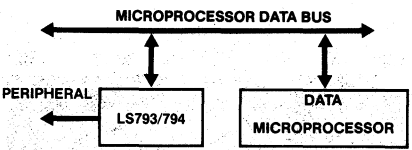
SN54/74LS793 SN54/74LS794

Features/Benefits

- I/O port configuration enables output data back onto input bus
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface

Description

These 8-bit latches/registers are useful for I/O operations on a microprocessor bus. An image of the output data can be read back by the CPU. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in an 'LS793/4, for verification and/or updating.



The data is loaded in the registers on the low-to-high transition of the clock (CK), for the 'LS794. The data is passed through the 'LS793 when the gate, (G), is High, and it is "latched" when G changes to Low. The output enable, $\overline{OE}$ is used to enable data on D7-D0. When $\overline{OE}$ is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When $\overline{OE}$ is High, D7-D0 are inputs to the latches/registers configuring D as an input bus.

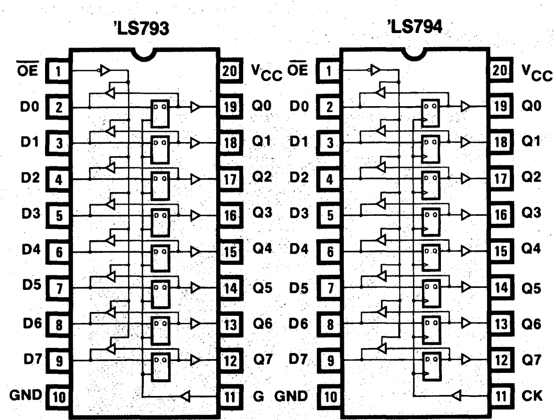
The output drive of these commercial parts for any output pin is I_{OL} = 24 mA. They are available in the popular 20-pin SKINNYDIP® package.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS793	J,W,L	Mil	Non-invert	Latch	LS
SN74LS793	N,J	Com			
SN54LS794	J,W,L	Mil		Register	
SN74LS794	N,J	Com			

* W (Cerpak), D (Side-brazed ceramic dual-in-line) packages are also available for both parts.

Logic Symbols



'LS793 Function Table

G	$\overline{OE}$	Q	D
L	L	Q_0**	Output, Q
L	H	Q_0**	Input
H†	L	D*	Output, Q*
H	H	D	Input

* In this case the output of the latch feeds the input, and a "race" condition results.

** Q_0 represents the previous "latched" state.

† This transition is not a normal mode of operation and may produce hazards.

'LS794 Function Table

CK	$\overline{OE}$	Q	D
L or H or ↓	L	Q_0	Output, Q
L or H or ↓	H	Q_0	Input
↑	L	Q_0	Output, Q*
↑	H	D	Input

* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_0.

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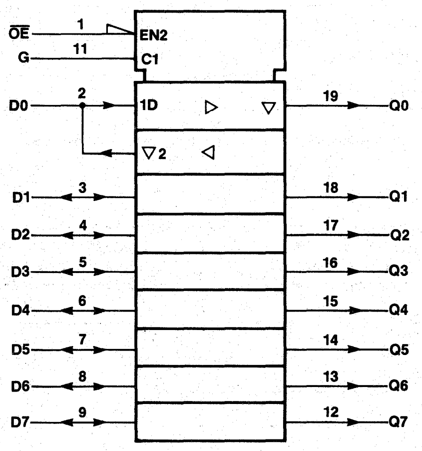
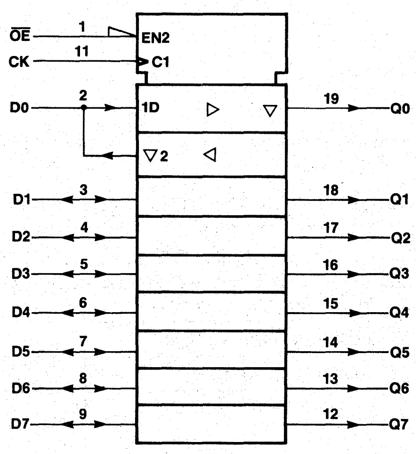
IEEE Symbols

'LS793



'LS794



Absolute Maximum Ratings

Supply voltage V_{CC} .... 7.0 V
Input voltage .... 7.0 V
Off-state output voltage .... 5.5 V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature			-55		125	0		75	°C
t_w	Width of Clock/Gate	High		15			15			ns
		Low ('LS794 only)		15			15			
t_{su}	Setup time		'LS793	15↓			10↓			ns
			'LS794	15↑			15↑			
t_h	Hold time		'LS793	10↓			10↓			
			'LS794	0↑			0↑			

↑ ↓ The arrow indicates the transition of the clock/gate input used for reference. ↑ for the low-to-high transitions, ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5			-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			-2.50			-2.50	μA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			40			40	μA
I_I	Maximum input current	D or Q	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -1 mA	2.4	3.4					V
				I_{OH} = -2.6 mA				2.4	3.1		
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-250			-250	μA
I_{OZH}				V_O = 2.7 V			40			40	
I_{OS}	Output short-circuit current*		V_{CC} = MAX		-30		-130	-30		-130	mA
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	'LS793			120			120	mA
				'LS794			120			120	

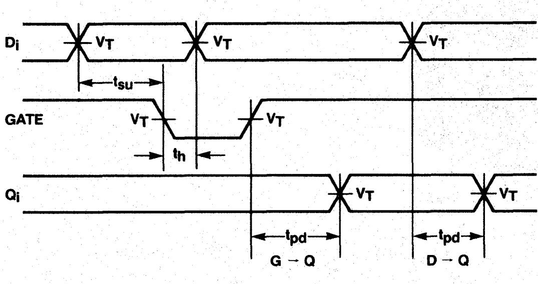
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

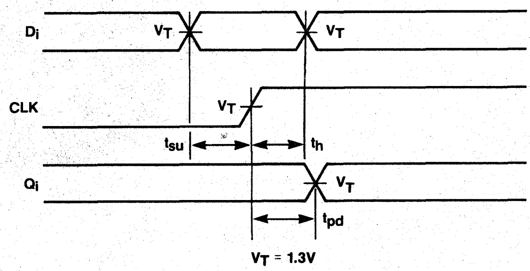
SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	'LS793 MIN	'LS793 TYP	'LS793 MAX	'LS794 MIN	'LS794 TYP	'LS794 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45pF R_L = 280 Ω				35	50		MHz
t_{PLH}	Data to output delay			12	18				ns
t_{PHL}				12	18				ns
t_{PLH}	Clock/gate to output delay			17	25		9	20	ns
t_{PHL}				12	25		14	20	ns
t_{PZL}	Output enable delay†			15	20		15	20	ns
t_{PZH}				11	20		11	20	ns
t_{PLZ}	Output disable delay†	C_L = 5pF R_L = 280 Ω		8	20		8	20	ns
t_{PHZ}				9	20		9	20	ns

† For the 'LS793, G should remain LOW during these tests.

'LS793 Timing Diagrams



'LS794 Timing Diagrams

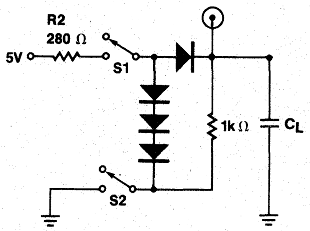


The case when gate is HIGH and data flows through the part is specified as Data to Output delay in the Switching Characteristics table. (V_T = 1.3V).

Test Loads

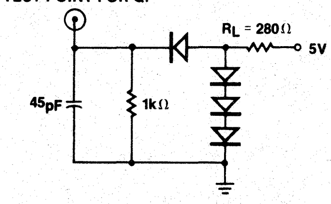
FOR D OUTPUTS-ENABLE AND DISABLE

TEST POINT FOR Di*



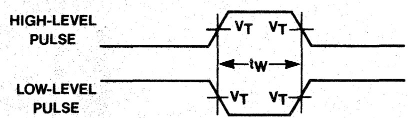
FOR Q OUTPUTS

TEST POINT FOR Qi*

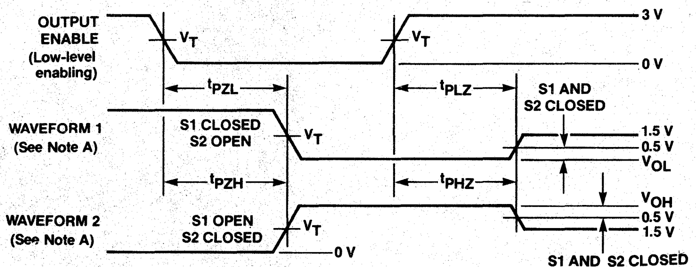


* The "TEST POINT" is drived by the output under test, and observed by instrumentation.

PULSE WIDTH



ENABLE AND DISABLE WAVEFORMS

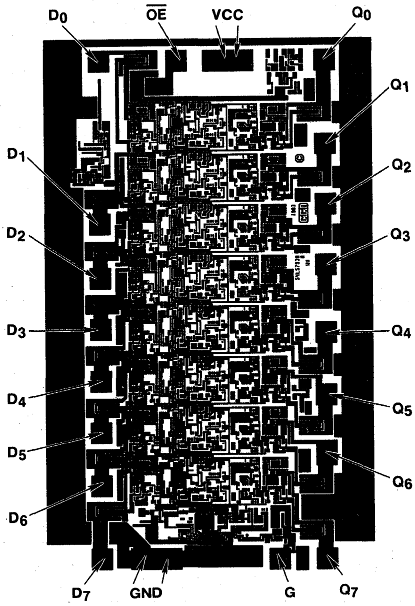


For the 'LS793, the latch control "G" should be low while testing the enable and disable times, so that the output (Q) does not change. (V_T = 1.3V).

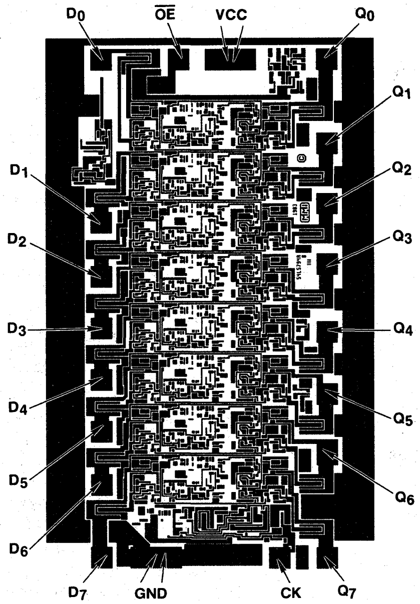
NOTES: A. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Die Configurations

'LS793



'LS794



Die Size: 79x127 mil^2

8-Bit Diagnostic Register SN74S818

Features/Benefits

- High drive capability: I_{OL} = 32 mA (Com), 24 mA (Mil)
- Assists on-line and off-line system diagnostic testing
- Swaps the content of shadow register and output register
- Shadow register for diagnostic testing
- Edge-triggered "D" registers
- Cascadable for wide control words as used in microprogramming
- Features RAM write-back for writable control store initialization
- PNP inputs for low-input current
- 24-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries

Applications

- Register for microprogram control store
- Status register
- Data register
- Instruction register
- Address register
- Interrupt mask register
- Pipeline register
- General purpose register
- Parallel-serial/serial-parallel converter

Description

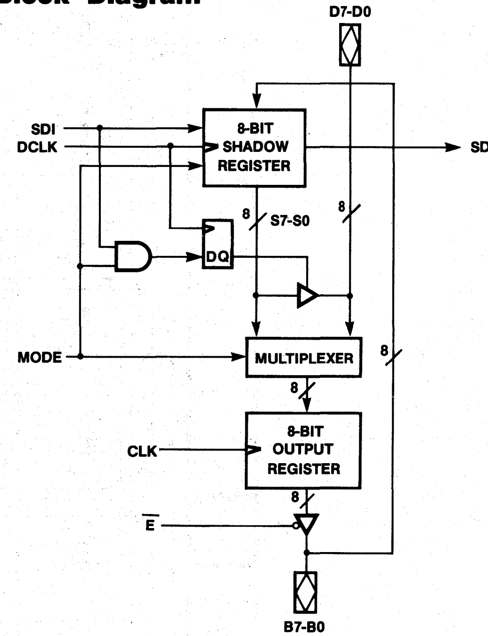
The SN74S818 is an 8-bit register with diagnostic features. There is a shadow register in each diagnostic register. Diagnostic data is shifted in serially into the shadow register (S7-S0), while the output register is loaded with either the content of the shadow register or the input data (D7-D0). Moreover, D7-D0 can also be used as the outputs from the shadow register to the data bus, while the outputs (B7-B0) can also be converted to inputs when disabled.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S818*	NS, JS	Com

* Contact the factory for miliatry version.

Block Diagram



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Function Table

INPUTS				OUTPUTS			OPERATION	SEE FIG.
MODE	SDI	CLK	DCLK	B7-B0	S7-S0	SDO		
L	X	↑	*	Bn ← Dn	HOLD	S7	Load output register from input bus	1
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S7	Shift shadow register data	2
L	X	↑	↑	Bn ← Dn	Sn ← Sn-1 S0 ← SDI	S7	Load output register from input bus while shifting shadow register data	1 & 2
H	X	↑	*	Bn ← Sn	HOLD	SDI	Load output register from shadow register	2,3,4
H	L	*	↑	HOLD	Sn ← Bn	SDI	Load shadow register from output bus	3
H	L	↑	↑	Bn ← Sn	Sn ← Bn	SDI	Swap shadow register and output register	
H	H	*	↑	HOLD	HOLD	SDI	Enable D7-D0 as outputs for RAM write-back	4

* Clock must be steady or falling.

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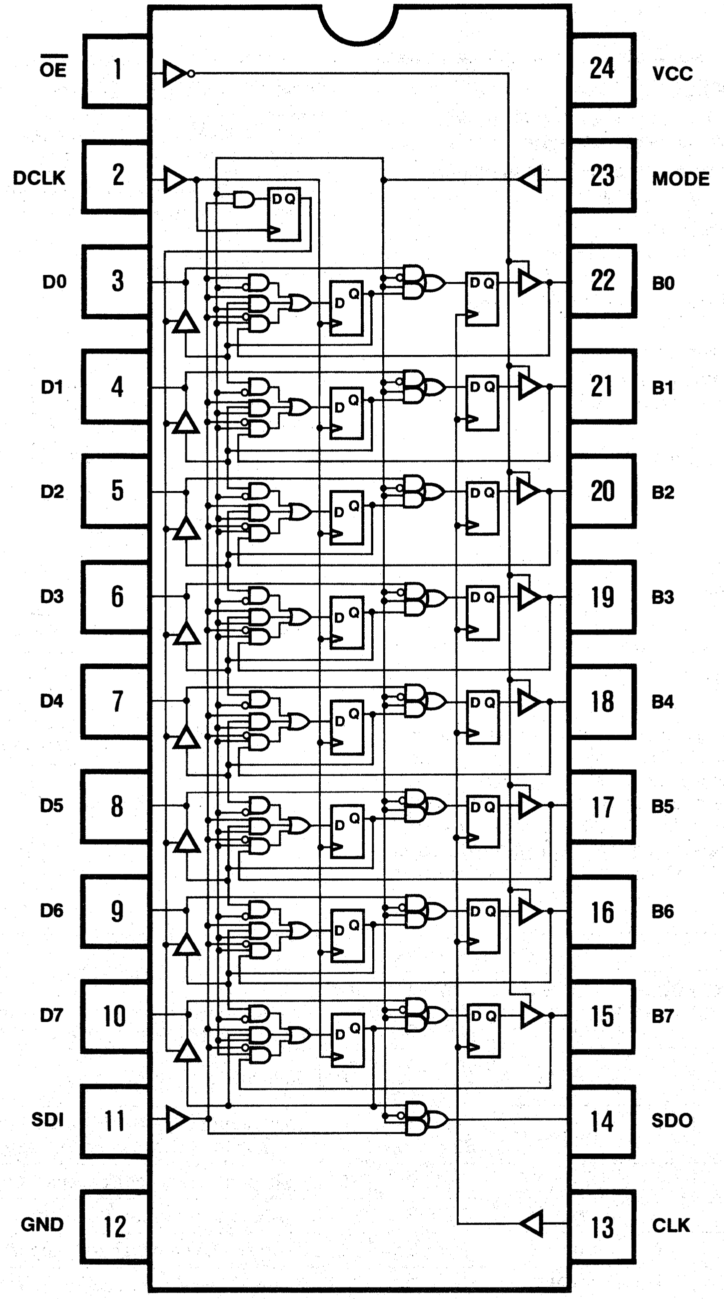
Logic Diagram



Absolute Maximum Ratings

	Operating
Supply voltage V_{CC}	7.0 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature	–65 to +150° C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_w	Width of CLK	High	12			ns
		Low	13			ns
t_{wd}	Width of DCLK	High	20			ns
		Low	20			ns
t_{suc}	Setup time from MODE to CLK		17 ↑			ns
t_{hc}	Hold time from CLK to MODE		0 ↑			ns
t_{sud}	Setup time from data to CLK		14 ↑			ns
t_{hd}	Hold time from CLK to data		0 ↑			ns
t_{sudc}	Setup time from SDI, MODE to DCLK		20 ↑			ns
t_{hdc}	Hold time from DCLK to SDI, MODE		0 ↑			ns
t_{sudq}	Setup time from output to DCLK		18 ↑			ns
t_{hdq}	Hold time from DLCK to output		0 ↑			ns

↑ ↓ The arrow indicates the transition of the clock/gate input used for reference: ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

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Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.2	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.5 V			−0.25	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			50	μA
I_I	Maximum input current	D or B	V_{CC} = MAX	V_I = 5.5 V			1	mA
		All others		V_I = 7 V				
V_{OL}	Low-level output voltage	B7-B0	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 32 mA			0.5	V
				I_{OL} = 24 mA				
		SDO D7-D0		I_{OL} = 8 mA			0.5	
				I_{OL} = 4 mA				
V_{OH}	High-level output voltage	B7-B0	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = 6.5 mA	2.4			V
		SDO D7-D0		I_{OH} = −2 mA				
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.5 V			−250	μA
I_{OZH}				V_O = 2.4 V			50	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX. Outputs open			115	145	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics $V_{CC} = 5$ V, $T_A = 25°C$

SYMBOL	PARAMETER		TEST CONDITIONS (See Test Load/Waveforms)	MIN	MAX	UNIT
f_{MAX}	Maximum output clock frequency		$C_L = 50$ pF $R_L = 280\Omega$ $\overline{OE} = L$	40		MHz
f_{MAXD}	Maximum diagnostic clock frequency	Cascaded	$C_L = 50$ pF $R_L = 2$ KΩ	20		MHz
		Uncascaded		25		
t_{CLK}	CLK to output delay		$C_L = 50$ pF $R_L = 280\Omega$ $\overline{OE} = L$		14	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		$C_L = 50$ pF $R_L = 2$ KΩ		12	ns
t_{MS}	MODE to SDO delay				17	ns
t_{DS}	DCLK to SDO delay (MODE = LOW)				28	ns
t_{DEZL}	DCLK to D7-D0 enable delay		$C_L = 50$ pF $R_L = 2$ KΩ		25	ns
t_{DEZH}					20	ns
t_{DDLZ}	DCLK to D7-D0 disable delay		$C_L = 5$ pF $R_L = 2$ KΩ		36	ns
t_{DDHZ}					60	ns
t_{DC}	DCLK to CLK separation		$C_L = 50$ pF $R_L = 280\Omega$ $\overline{OE} = L$	22		ns
t_{CD}	CLK to DCLK separation			35		ns
t_{PZL}	Output enable delay		$C_L = 50$ pF $R_L = 280\Omega$		19	ns
t_{PZH}					13	ns
t_{PLZ}	Output disable delay		$C_L = 5$ pF $R_L = 280\Omega$		12	ns
t_{PHZ}					22	ns

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER		TEST CONDITIONS (See Test Load/Waveforms)	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum output clock frequency		$C_L = 50$ pF $R_L = 280\Omega$ OE = L	40		MHz
f_{MAXD}	Maximum diagnostic clock frequency	Cascaded	$C_L = 50$ pF $R_L = 2$ KΩ	20		MHz
		Uncascaded		25		
t_{CLK}	CLK to output delay		$C_L = 50$ pF $R_L = 280\Omega$ OE = L		14	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		$C_L = 50$ pF $R_L = 2$ KΩ		15	ns
t_{MS}	MODE to SDO delay				18	ns
t_{DS}	DCLK to SDO delay (MODE = LOW)				30	ns
t_{DEZL}	DCLK to D7-D0 enable delay		$C_L = 50$ pF $R_L = 2$ KΩ		25	ns
t_{DEZH}					25	ns
t_{DDLZ}	DCLK to D7-D0 disable delay		$C_L = 5$ pF $R_L = 2$ KΩ		45	ns
t_{DDHZ}					80	ns
t_{DC}	DCLK to CLK separation		$C_L = 50$ pF $R_L = 280\Omega$ OE = L	30		ns
t_{CD}	CLK to DCLK separation			40		ns
t_{PZL}	Output enable delay		$C_L = 50$ pF $R_L = 280\Omega$		20	ns
t_{PZH}					15	ns
t_{PLZ}	Output disable delay		$C_L = 5$ pF $R_L = 280\Omega$		15	ns
t_{PHZ}					25	ns

Timing Waveforms

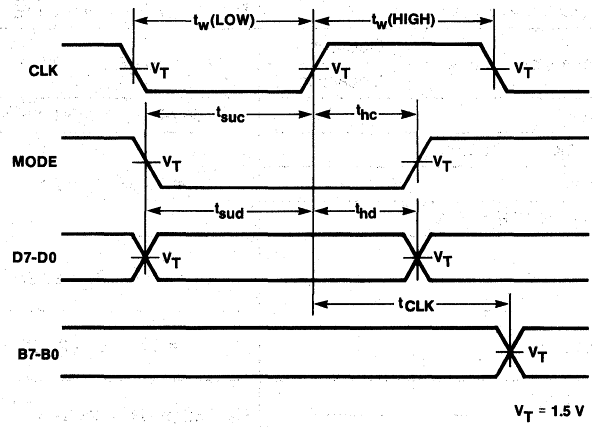

Figure 1. Switching waveforms for typical register applications ($\overline{OE}$ = L)

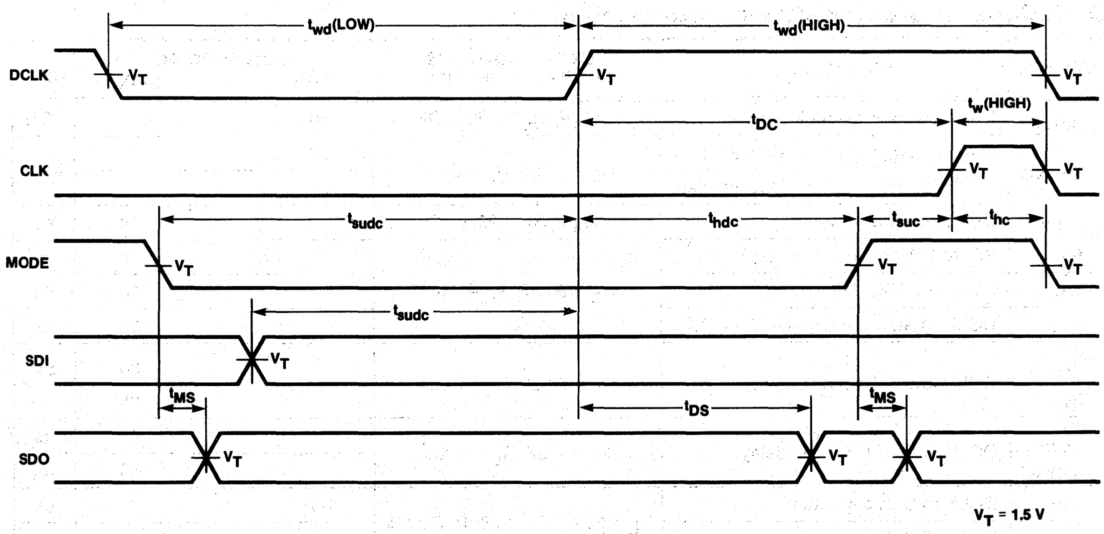

Figure 2. Switching waveforms for shift-in followed by diagnostic load

Timing Waveforms

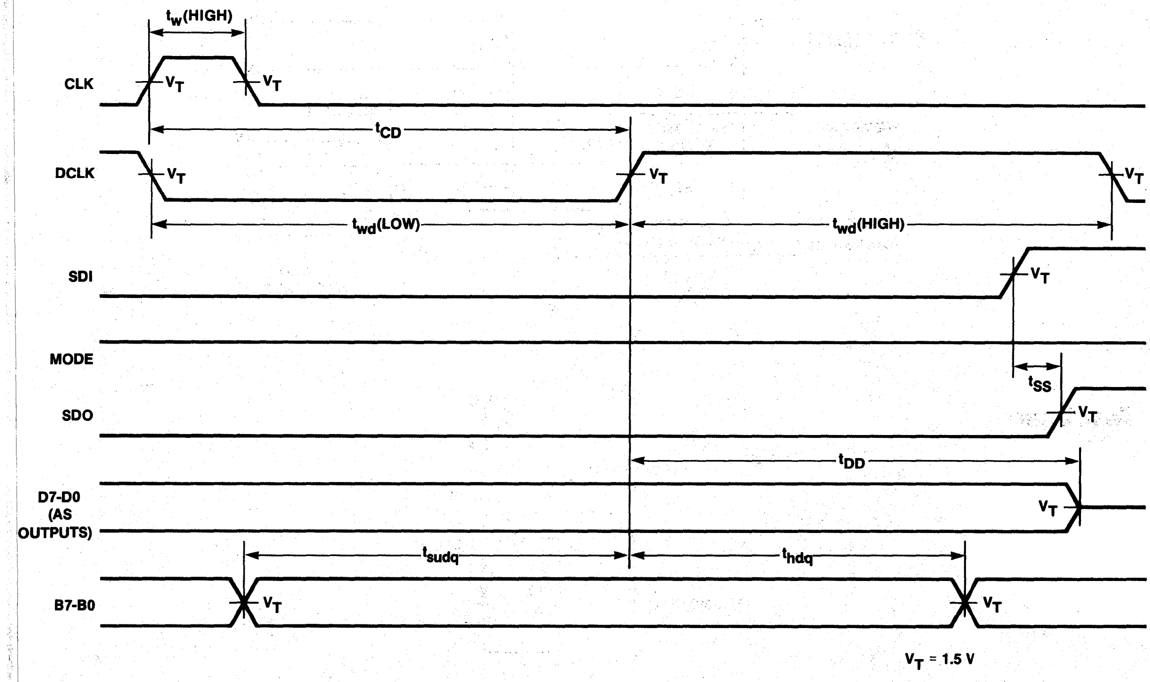

Figure 3. Switching waveforms for data bus (D7-D0) disabling

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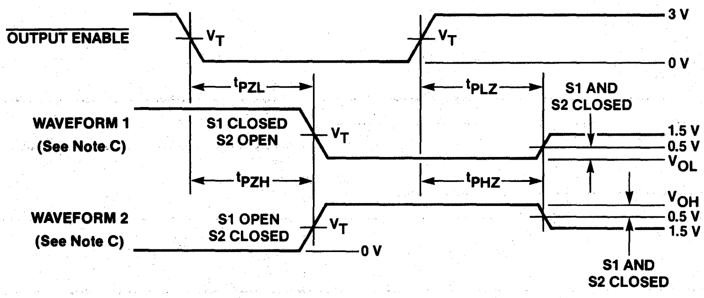
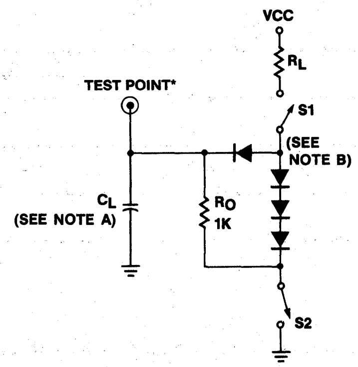
Enable/Disable Delay



Test Load



* The "TEST POINT" is drived by the output under test, and observed by instrumentation.

NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz Z_{out} = 50Ω and for series 54/74S t_R = 2.5 ns $t_F \leq$ 2.5 ns.

F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

G.

	B7-B0	D7-D0, SDO
R_O	1 KΩ	5 KΩ

Basics of Diagnostics

The basic theory of diagnostics is to insert test data to the inputs of a typical system and sample the test results from certain nodes of the circuits. For a combinatorial circuit, testing is very easy since the circuit has no memory of the previous states. But for a sequential circuit, the data to be sampled at a node depends not only on the inputs, but also on the current state it is in. If the previous state contains some error, it will possibly perform an illegal jump. In that case, depending on which state the system is currently in, the next state may be different. After several illegal jumps, it will be quite impossible to keep track of the jumps which it performs.

A way to solve the problem is by converting a sequential circuit to a combinatorial one. A sequential circuit can often be viewed as a network with a clock and a number of inputs and outputs, with some outputs being routed back to the inputs (see Figure 5a). If the loop is broken and inputs which are fed back from the outputs are instead fed in from some external sources (see Figure 5b), the system can be viewed as combinatorial and system testing will be easier. The "shadow register" concept involves shifting in serial data to the hidden register (the shadow register) and then loading test data to the output register. Together with other system inputs, the test results will appear on the output end of the network and can be sampled and analyzed. and analysed.

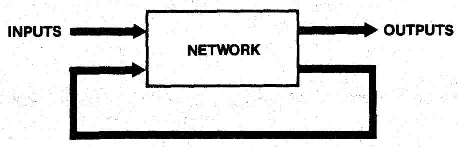


Figure 5a. A typical digital system

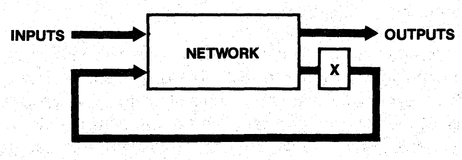


Figure 5b. The feedback of figure 5a is broken to convert the system to a non-sequential one

Diagnostic On-Chip™ (DOC™) Using Shadow Register

The diagnostic register is an 8-bit register with two levels of registers—a shadow register and an output register. A shadow register is basically a buried register with shift capability. There is also an output register whose outputs appear to the rest of the system. There is an output flipflop to each shadow flipflop. An output flipflop drives a three-state output buffer before going to the output pin. If the output is disabled, the output pin may be converted to an input pin. This feature is very important if the output is driving a bus and sampling of data on the bus is desired.

The input to a bit of the shadow register is a multiplexer which can select from one of the following nodes:

a) Output of the preceding bit of the shadow register (or SDI for the least significant bit).
b) Output of the same bit of the shadow register.
c) Data on the output pin of the same bit. This data may be the output of the corresponding bit of the output register if there is no output enable pin and the output is enabled, or the input to that pin if there is an output enable pin and output is disabled. Refer to Figure 6 for some general information on a typical diagnostic functional part with output enable ($\overline{OE}$).

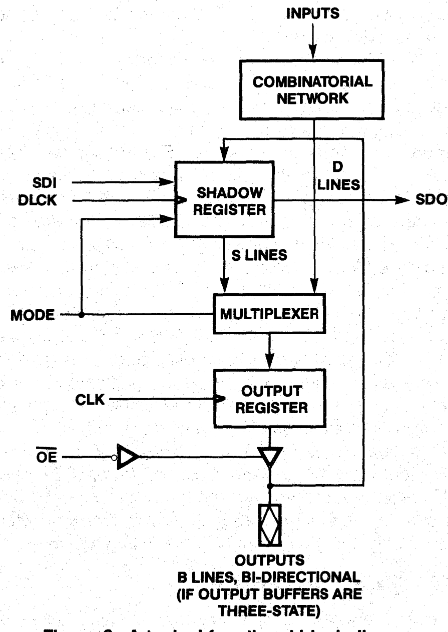


Figure 6. A typical functional block diagram for a diagnostic part

The input to any bit of the output register is also selected from one of the following nodes:
a) Corresponding input bit.
b) Corresponding output bit of the shadow register.

The reasons why a shadow register is preferred, as compared to shifting in diagnostic data directly to the output register, are:
a) The output register contains control signals for the system. Certain bits of this register may control different ports which are driving the same bus. As diagnostic data is shifted in, these bits become random and the ports they are controlling may drive a bus simultaneously. Invalid data may appear and worst of all, with a low-impedance path between the power supply, severe damage may be done to these ports.
b) As a diagnostic word is shifted in, the system is performing different tasks from what it is supposed to do. For example, when an ALU is performing an addition, diagnostic data is shifted in. The ALU then performs some other functions. The status of the system keeps changing. In some cases, illegal states may appear which produces unpredictable test results; for example, a flag may appear unpredictably.
c) The shadow register enables diagnostic data to be shifted in as background data without holding up the processor operation.

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The diagnostic register is one part in a series of diagnostic products which follows a new standard for diagnostics. The basic standard is described in Figure 6 and the table on page one. This standard implies that all diagnostic parts in this series are cascadable.

Diagnostic Pins

There are several pins in the diagnostic register in addition to the regular 8-bit inputs and outputs:

1) Diagnostic Clock (DCLK)—The diagnostic clock is used to clock the shadow register.

2) MODE—This pin is used in selecting the data to the registers. For the output register, MODE = LOW indicates that the output register is being used as a normal register; MODE = HIGH means that the next state of the output register will be obtained from the shadow register. For the shadow register, MODE = LOW indicates serial data from SDI (see below) is shifted in every diagnostic clock; MODE = HIGH switches SDI from a data input to a control input. See below for details.

3) Serial Data In (SDI)—When MODE = LOW, this pin is for shifting serial data in. When MODE = HIGH, SDI serves as a control pin. If MODE = HIGH and SDI = LOW, data from the output pins will be loaded to the shadow register on the next DCLK. MODE = HIGH and SDI = HIGH indicate a reserved operation. The data from the diagnostic clock is held the same. This reserved operation will be very significant when more operations than what is described are needed. The diagnostic register gives an example of how it can be used.

4) Serial Data Out (SDO)—When MODE = LOW, this pin carries the shift-out bit of the shadow register. When MODE = HIGH, the SDI becomes a control pin and the control signal should be passed along if several diagnostic parts are connected together serially. So SDO should carry SDI along in this case.

Write-Back to RAMs

Due to the applications of a diagnostic register in a writable microprogram control store, this part also includes an additional feature to initialize the control RAMs; when necessary, the input data pins to the register can be operated as output pins. In short, a diagnostic register is an 'asymmetric register transceiver' with shift capability. The term 'asymmetric register transceiver' means that there are two bidirectional registered ports on a chip, and these ports are enabled with different methodologies and have different timings. One port is still primarily for inputs (D7-D0), while the other is primarily for outputs (B7-B0).

When MODE and SDI are both HIGHs, the D7-D0 will be converted to an output port on the rising edge of the next DCLK by enabling the three-state buffers driving the D7-D0. The input for the three-state buffers is from the outputs of the shadow register (S7-S0).

Applications

This part can be used as a: microprogram control store register, data register, status register, address register, instruction register, interrupt mask register, interrupt vector, program counter, stack pointer, and for other general purposes.

If the diagnostic registers are used in a system using microprogram control words, status registers, and instruction registers, etc., one way to connect them together is shown in Figure 7. There is only one data input and one data output to the diagnostic parts. When serial data is shifted in or shifted out, data has to be passed from one diagnostic chip to another. Since SDI must be passed from chip-to-chip if it is used for control, it is necessary for logic designers to make sure the fall-through time of SDI to the last chip and the setup time from SDI to DCLK are satisfied.

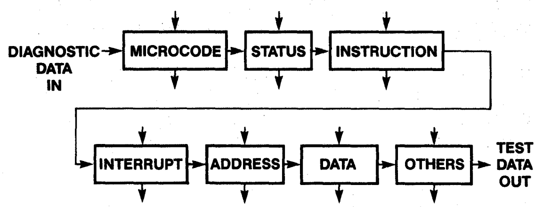

Figure 7. One way diagnostic registers can be linked together

The diagnostic registers are basically used for diagnostic purposes, although they may also function as parallel-to-serial and serial-to-parallel converters.

Two examples of how the diagnostic parts can be built into a system are shown in Figures 8, 9. The diagnostic registers are used to substitute the instruction register, memory data registers, status register, memory address registers, and the registers for a non-writable (Figure 8) or a writable (Figure 9) microprogram control store. The only additional block to a typical system without diagnostic features is the diagnostics controller. The diagnostics controller should be able to supply the system with signals like MODE, SDI, DCLK, and the register clock (CLK). In order words, the diagnostics controller in itself is a supercontroller of the processing unit. It should also be noted that all sequential paths, except for the register files, should be converted to combinatorial paths if all the diagnostic parts are to break the sequential loops.

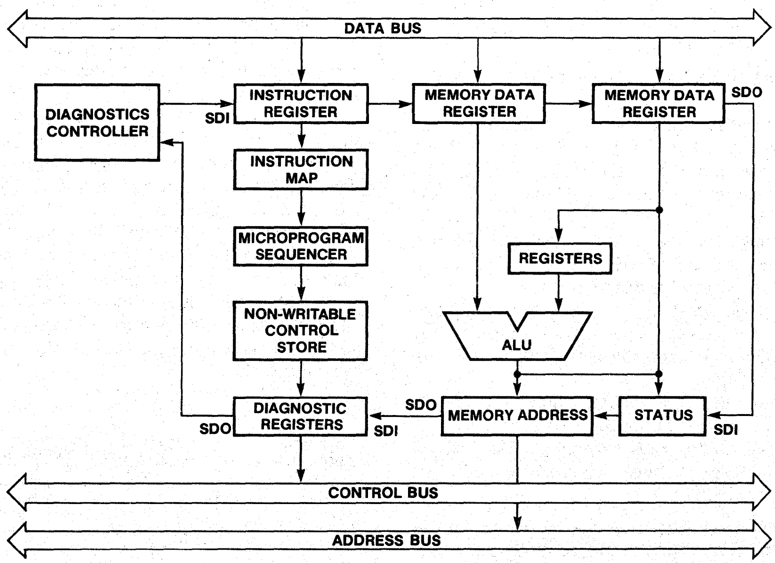

Figure 8. An application example of using diagnostic registers in a CPU using non-writable control store

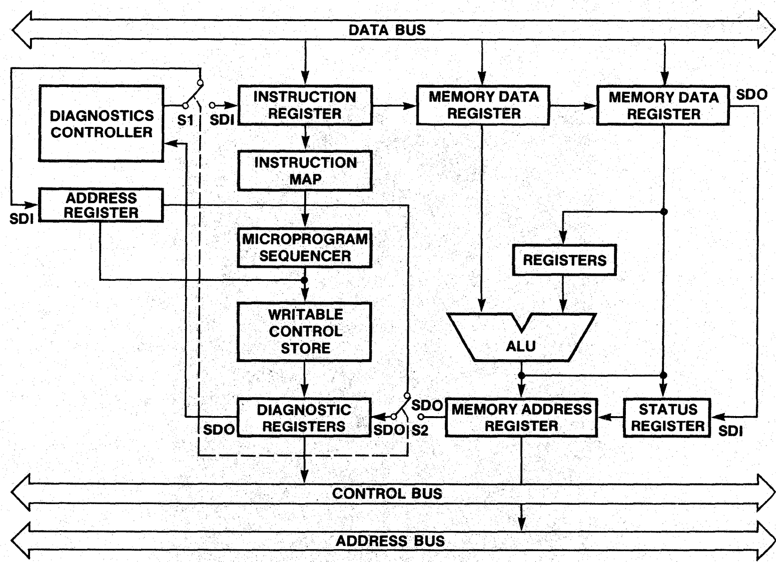

Figure 9. An application example of using diagnostic registers in a CPU using writable control store

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In normal operation, the diagnostic controller will make the diagnostic feature inactive by setting MODE = LOW and disabling DCLK and have the CLK free running.

When diagnostics are needed, the following sequence is performed:

1) Shift in diagnostic test data bit-by-bit. In order to perform this operation, CLK is disabled; MODE remains LOW; SDI contains the bit to be shifted in, and the diagnostic clock is enabled. This will continue until a full test vector is shifted into the shadow register.
2) MODE switches to HIGH. Then DCLK is disabled and CLK is enabled. The contents of the shadow register, which is the test vector, will be loaded into the output register.
3) The test result is set up at the inputs of the diagnostic registers. MODE switches to LOW again. DCLK is still disabled and CLK is still enabled. The test result will be clocked into the output register.
4) With MODE HIGH and DCLK enabled and CLK disabled, the test result will be clocked to the shadow register.
5) With MODE held LOW and DCLK still enabled and CLK still disabled, the test result can be shifted out and analyzed while another test vector is shifted in.

A block diagram of such a diagnostics controller is shown in Figure 10. The central control unit of this controller may be a disk-based unit or even a diagnostic PROM. Note that, in normal operation, MODE remains LOW and only CLK is active.

Figure 9 is an example with writable programmable control store where initialization of the control RAMs is necessary. This can be done by loading in a sequence of data and address through the diagnostics controller. What this controller must be able to do, in addition to what is described above (see Figure 10), is to disable the outputs from the microprogram sequencer and feed in the address through another diagnostic register. There is a switch, S1, which switches the SDI to the registers of the writable control store from some other register (in Figure 9, it is the memory address register) to the diagnostic 'control store address' register. The initialization data is shifted into the shadow register by resetting MODE to LOW and enabling DCLK. After all data is shifted into the shadow register, MODE and SDI are set HIGH and then followed by a CLK, a DCLK, and a write to control store. The CLK loads the present control store address in the output registers of the 'control store address' register, and the MODE = HIGH and SDI = HIGH will enable the inputs to the diagnostic register as outputs, so that the data in the shadow register can be written back to the control store.

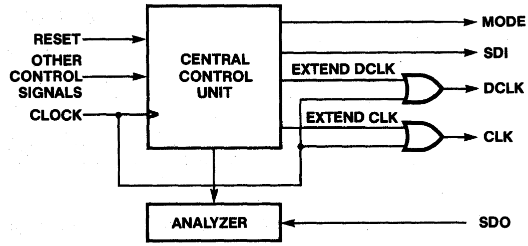
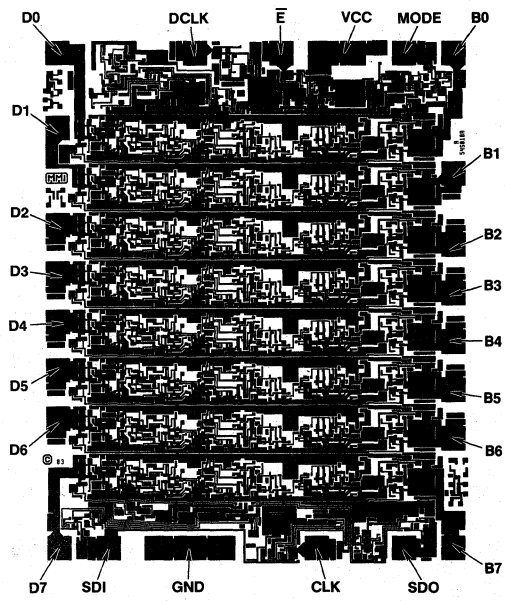


Figure 10. A diagnostic controller unit

Die Configuration



Die Size: 92x112 mil^2

8-Bit Bus Front-Loading Latch Transceivers — Advanced CMOS-TTL Compatible

54/74ACT646 54/74ACT648

Features/Benefits

- Bidirectional bus transceiver and register
- Independent registers for A and B buses
- Real-time data transfer or stored data transfer
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low quiescent supply current of <10 μA (typical)
- Active supply current at about 20% LS equivalent
- Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to +85°C

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	OUTPUT	TECH
54ACT646	JS,W, L28	Mil	Non-invert	3-state	CMOS
74ACT646	NS,JS	Com			
54ACT648	JS,W, L28	Mil	Invert		
74ACT648	NS,JS	Com			

Description

This 8-bit bus transceiver with three-state outputs has sixteen D-type flip-flops and multiplexers. The bus-oriented pinout of the part is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'ACT646/648 are given in the Logic Diagram. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path, or "feed-through", into a two-way multiplexer is sometimes called a "front-loading latch."

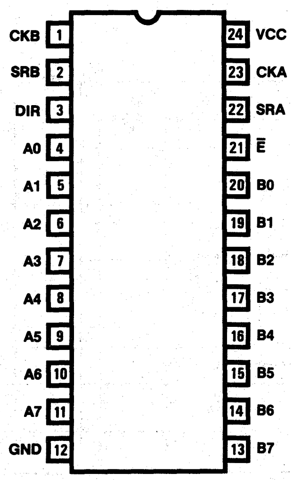
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by enable line $\overline{E}$, and direction line DIR.

When $\overline{E}$ is High, data from the buses can be stored into register A and B. When $\overline{E}$ is Low and DIR is High, the direction of operation is from A to B, when $\overline{E}$ and DIR are Low, the direction of operation is from B to A.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

Pin Configuration

'ACT646/648
8-Bit Bus Front-Loading Latch Transceiver



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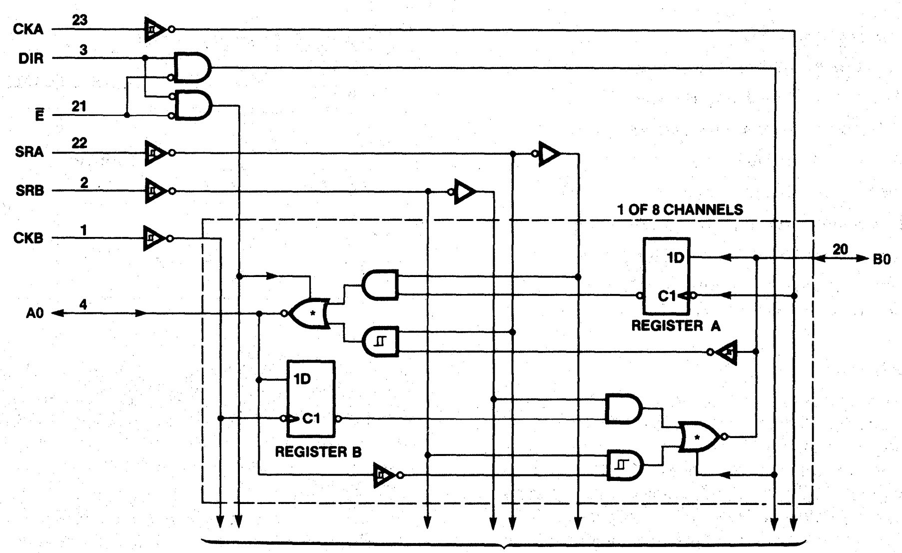
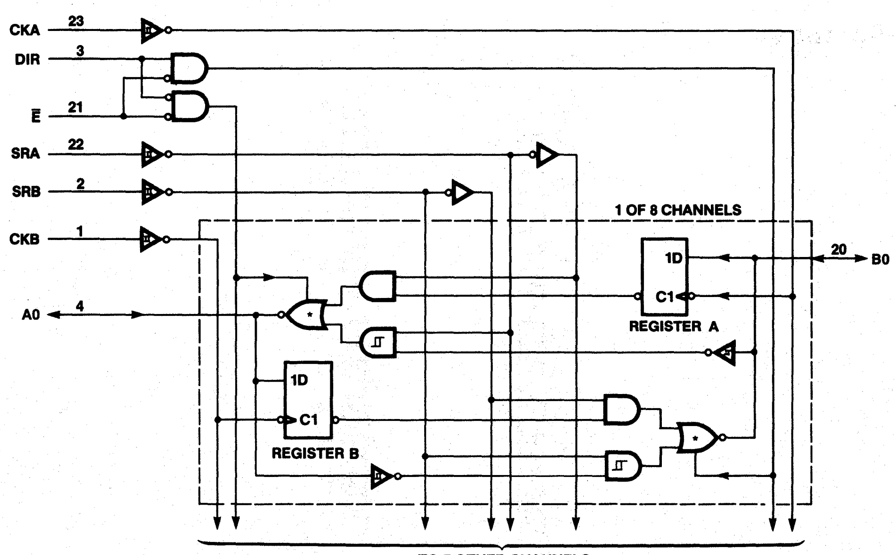
Monolithic Memories

Logic Diagrams

'ACT646 (Non-Inverting)

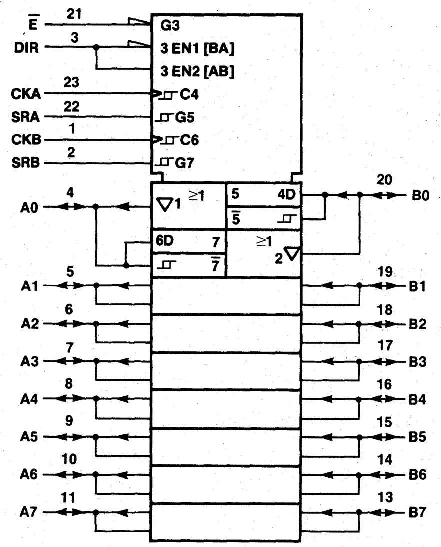


'ACT648 (Inverting)

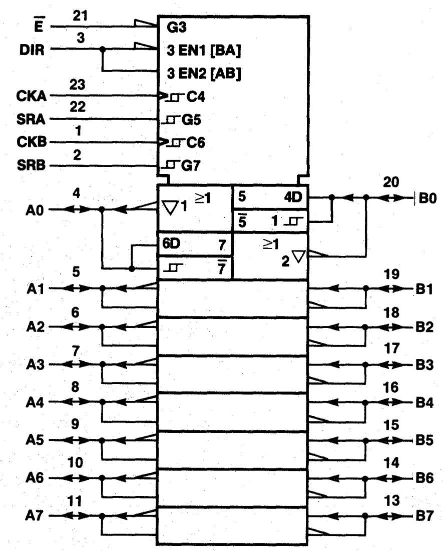


IEEE Symbols

'ACT646

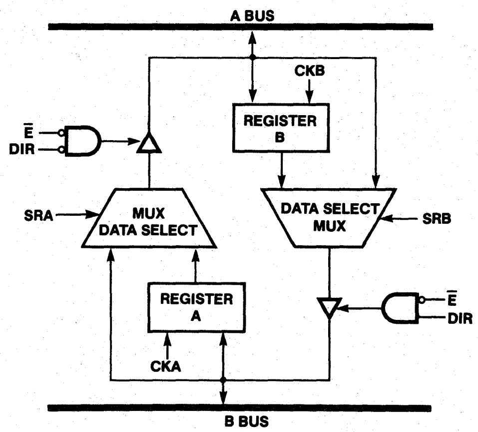


'ACT648

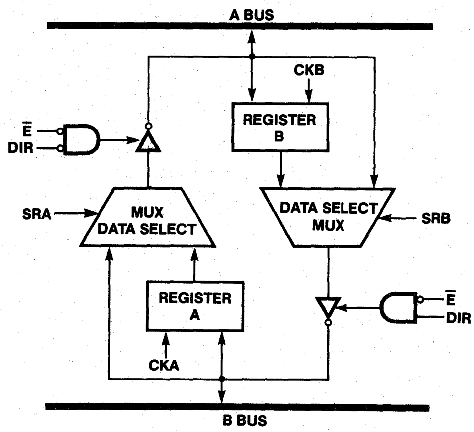


Block Diagrams

'ACT646 (Non-inverting)



'ACT648 (Inverting)



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Function Table Nomenclature Description

$\overline{E}$: To enable A-to-B or B-to-A operation.

DIR: To select the direction of operation.

$\overline{E}$	DIR	OPERATION DIRECTION
L	L	B-to-A
L	H	A-to-B
H	X	A and B buses both are inputs (Storage)

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is a High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for Register A/B.

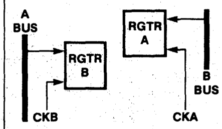
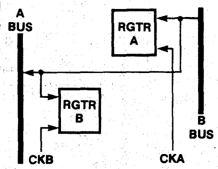
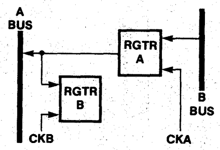
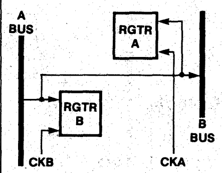
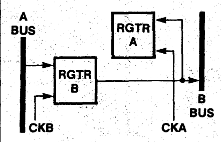
X: H or L state irrelevant ("Don't Care" condition).

↑: Positive edge of clock causes clocking, if clock enable is asserted.

UC: H or L or ↓ case (nonclocked operation).

RGTR: Register.

Bus Operation for 'ACT646

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'ACT646
	$\overline{E}$	DIR	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	H	X	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time B bus data → A bus
								UC	↑	Real time B bus data → A bus Real time B bus data → RGTR B
								↑	UC	Real time B bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR A data → A bus
								UC	↑	RGTR A data → A bus RGTR A data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR A data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
Real time A-to-B Operation	L	H	X	L	Input	Output		UC	UC	Real time A bus data → B bus
								UC	↑	Real time A bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time A bus data → B bus Real time A bus data → RGTR A
								↑	↑	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	L	H	X	H	Input	Output		UC	UC	RGTR B data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR B data → B bus
								↑	UC	RGTR B data → B bus RGTR B data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A

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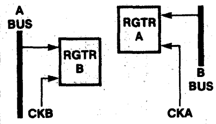
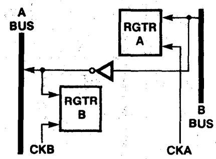
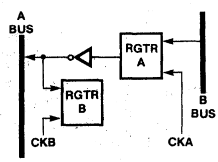
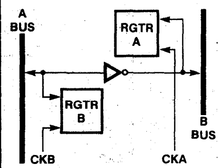
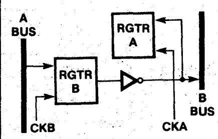
Bus Operation for 'ACT648

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'ACT648
	$\overline{E}$	DIR	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	H	X	X	X	Input	Input	 	UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input	 	UC	UC	Real time $\overline{B}$ bus data → A bus
								UC	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR B
								↑	UC	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A Real time $\overline{B}$ bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input	 	UC	UC	RGTR $\overline{A}$ data → A bus
								UC	↑	RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
Real time A-to-B Operation	L	H	X	L	Input	Output	 	UC	UC	Real time $\overline{A}$ bus data → B bus
								UC	↑	Real time $\overline{A}$ bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A
								↑	↑	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	L	H	X	H	Input	Output	 	UC	UC	RGTR $\overline{B}$ data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus
								↑	UC	RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A

Absolute Maximum Ratings

Supply voltage, V_{CC} .... -0.5 V to 7.0 V
DC input voltage, V_I .... -0.5 V to V_{CC} +0.5 V
DC output voltage, V_O .... -0.5 V to V_{CC}+0.5 V
DC output source/sink current per output pin, I_O .... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} .... ±100 mA
Input diode current, I_{IK}:
V_I <0 .... -20 mA
V_I >V_{CC} .... +20 mA
Output diode current, I_{OK}:
V_O <0 .... -20 mA
V_O >V_{CC} .... +20 mA
Storage temperature .... -65 to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
T_A	Operating free-air temperature		-55		125	-40		85	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Set up time		30↑			25↑			ns
t_h	Hold time		0↑			0↑			ns
t_r	Input rise time at V_I = 4.5 V		0		500	0		500	ns
t_f	Input fall time at V_I = 4.5 V		0		500	0		500	ns
I_{OH}	High-level output current				-6			-6	mA
I_{OL}	Low-level output current				12			12	mA

↑ The arrow indicates the Low-to-High transition of the clock input used as reference.

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Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		25°C MIN TYP MAX	MILITARY MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
V_{IL}	Low-level input voltage			0.8	0.7	0.8	V
V_{IH}	High-level input voltage			2	2	2	V
I_{IN}	Input Current	V_{CC} = MAX	$V_I = V_{CC}$ or GND	±1.0	±1.0	±1.0	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = 20 μA	0.1	0.1	0.1	V
			I_{OL} = 6 mA	0.32	0.4	0.37	
			I_{OL} = 12 mA	0.4	0.4	0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = −20 μA	3.4	3.4	3.4	V
			I_{OH} = −6 mA	2.4	2.4	2.4	
I_{OZ}	Off-state output current	V_{CC} = MAX	$V_O = V_{CC}$ or GND	±10	±50	±30	μA
I_{CC}	Quiescent supply current	V_{CC} = MAX	$V_I = V_{CC}$ or GND	10	80	40	μA
I_C	Maximum quiescent supply current	V_{CC} = MAX	Only one input at 2.4 V	1.5	2.0	1.9	mA
		V_I = 2.4 V or 0.5 V	All inputs at 2.4 V	25	35	33	

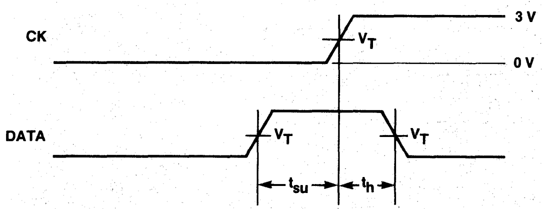
Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	COM/MIL T_A = 25°C MIN MAX	MILITARY MIN MAX	COMMERCIAL MIN MAX	UNIT
t_{PLH}	Data to output delay	C_L = 50 pF	35	55	45	ns
t_{PHL}			35	55	45	
t_{PLH}	Clock to output delay		30	44	38	ns
t_{PHL}			30	44	38	
t_{PLH}	Select to output delay* (data input high)		28	40	35	ns
t_{PHL}			28	40	35	
t_{PLH}	Select to output delay* (data input low)		28	40	35	ns
t_{PHL}			28	40	35	
t_{PZL}	Output enable delay	R_L = 1KΩ C_L = 50 pF	40	50	45	ns
t_{PZH}			40	50	45	
t_{PLZ}	Output disable delay		35	45	40	ns
t_{PHZ}			35	45	40	
t_{PZL}	Direction enable delay		40	50	45	ns
t_{PZH}			35	45	40	
t_{PLZ}	Direction disable delay		30	40	35	ns
t_{PHZ}			30	40	35	

* See Figure 4.

Test Waveforms

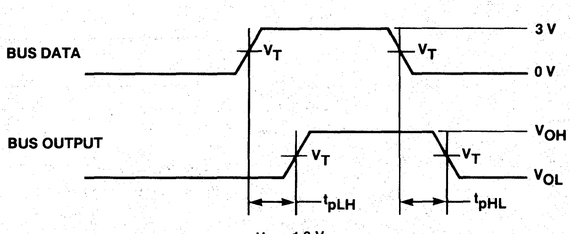
Setup Time/Hold Time



$V_T = 1.3$ V

Figure 1.

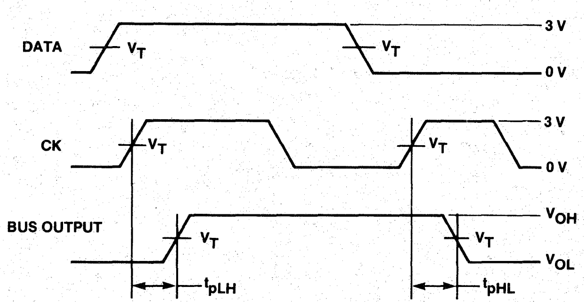
Bus Data To Bus Output Delay



$V_T = 1.3$ V

Figure 2.

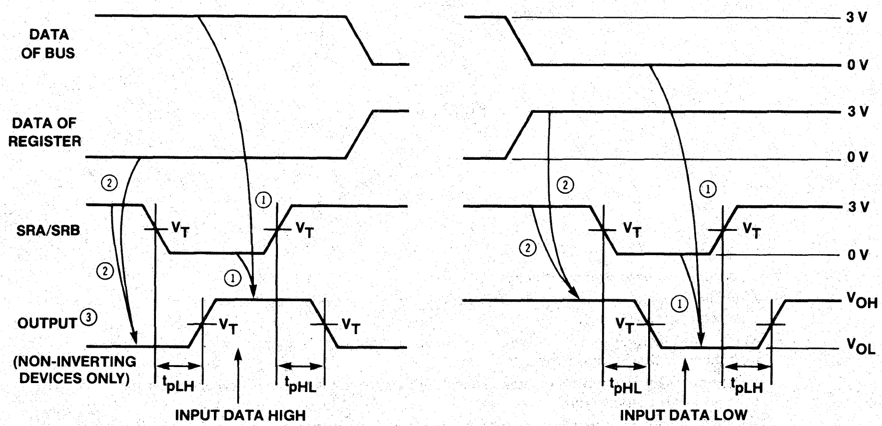
CK To Bus Output Propagation Delay Time



$V_T = 1.3$ V

Figure 3.

Select To Output Delay



$V_T = 1.3$ V

NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Figure 4.

Enable/Disable/Direction-Change Delay

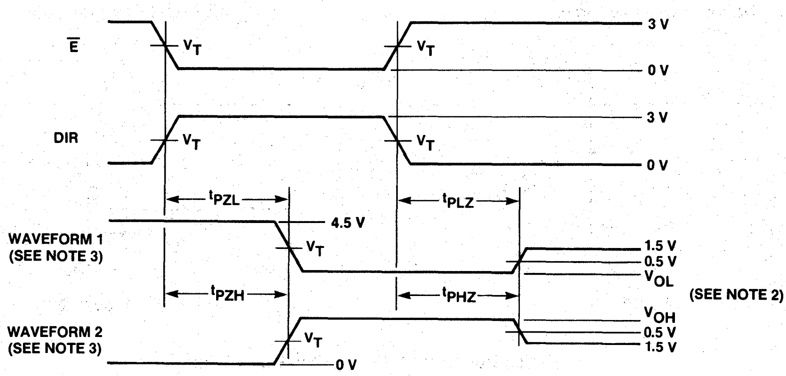


Figure 5.

Test Load

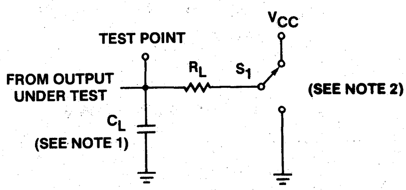


Figure 6.

NOTES

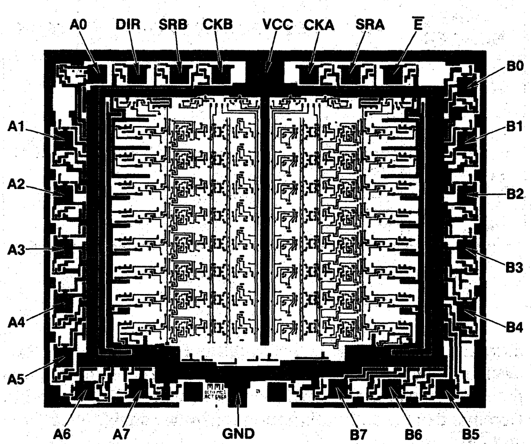
1. C_L includes probe and jig capacitance.
2. When measuring t_{PLZ} and t_{PZL}, S_1 is tied to V_{CC}. When measuring t_{PHZ} and t_{PZH}, S_1 is tied to ground.

   When measuring propagation delay times of three-state outputs, S_1 is open, i.e., not connected to V_{CC} or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.

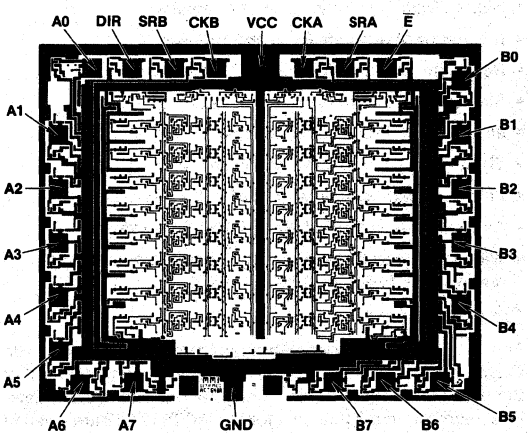
   Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: PRR ≤1 MHz, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

Die Configurations

54/74ACT646



54/74ACT648



Die size: 87x107 mil^2

8-Bit Bus Front-Loading Latch Transceivers — Advanced CMOS-TTL Compatible

54/74ACT651 54/74ACT652

Features/Benefits

- **Bidirectional bus transceiver and register**
- **Independent registers for A and B buses**
- **Real-time data transfer or stored data transfer**
- **Simultaneous outputs on both buses**
- **24-pin SKINNYDIP® saves space**
- **Three-state outputs drive bus lines**
- **Low quiescent supply current of <10 μA (typical)**
- **Active supply current at about 20% LS equivalent**
- **Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to +85°C**

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	OUTPUT	TECH
54ACT651	JS,W, L28	Mil	Invert	3-state	CMOS
74ACT651	NS,JS	Com			
54ACT652	JS,W, L28	Mil	Non-invert		
74ACT652	NS,JS	Com			

Description

This 8-bit bus transceiver with three-state outputs has sixteen D-type flip-flops and multiplexers. The bus-oriented pinout of the part is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'ACT651/652 are given in the Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path, or "feed-through", into a two-way multiplexer is sometimes called a "front-loading latch."

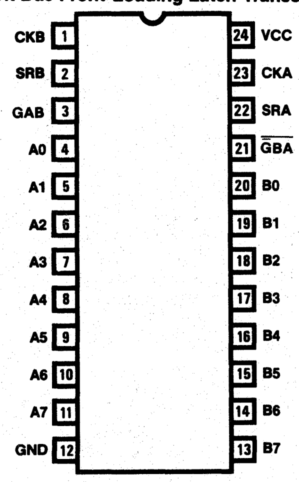
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by two enable lines, GAB and $\overline{\text{GBA}}$.

When GAB is low and $\overline{\text{GBA}}$ is high, data from the buses can be loaded into registers A and B. When $\overline{\text{GBA}}$ is low, the A bus is configured for output. When GAB is high, the B bus is configured for output. The A and B buses can be enabled at the same time, to operate as outputs simultaneously.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

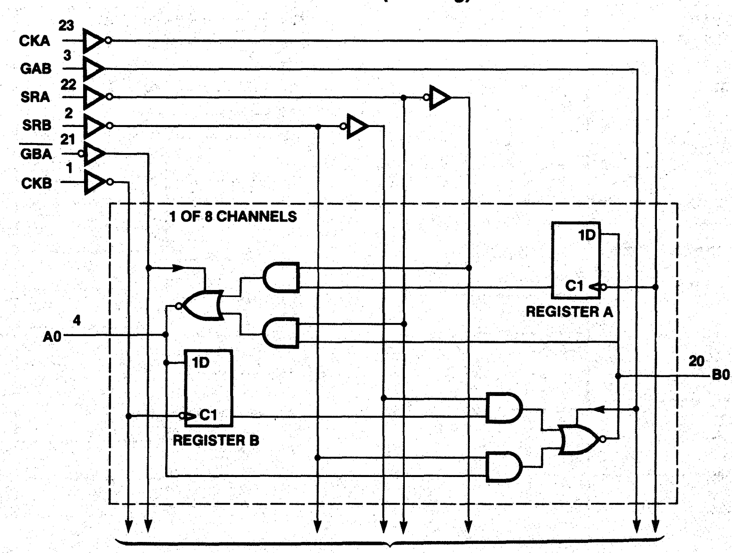
Pin Configuration

'ACT651/652
8-Bit Bus Front-Loading Latch Transceiver

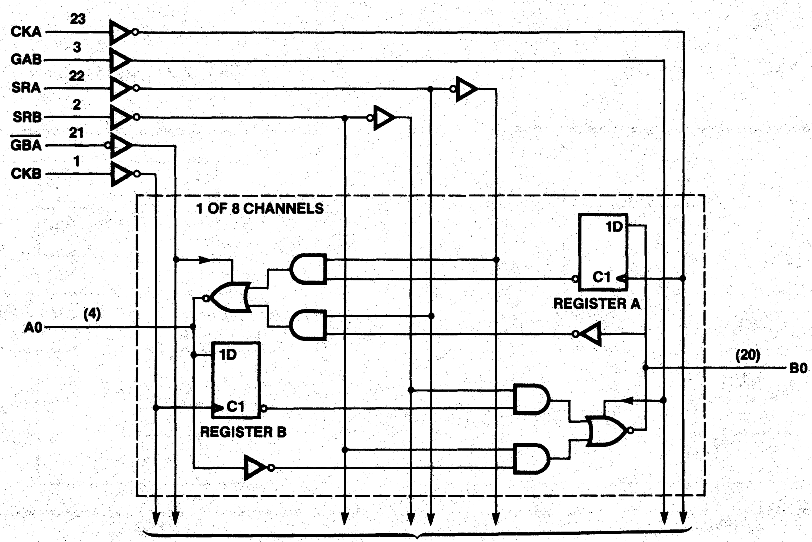


Logic Diagrams

'ACT651 (Inverting)



'ACT652 (Non-Inverting)



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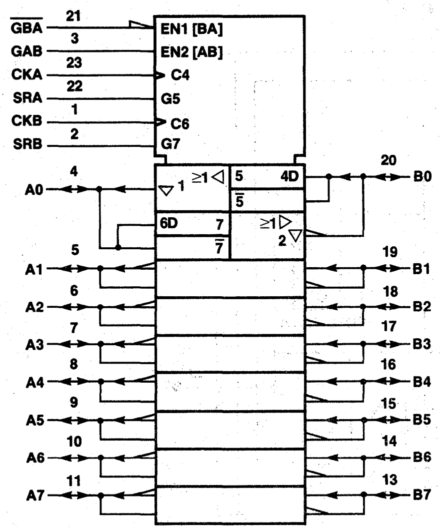
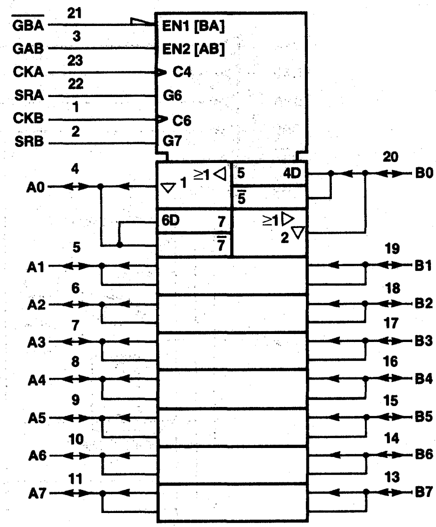
IEEE Symbols

'ACT651

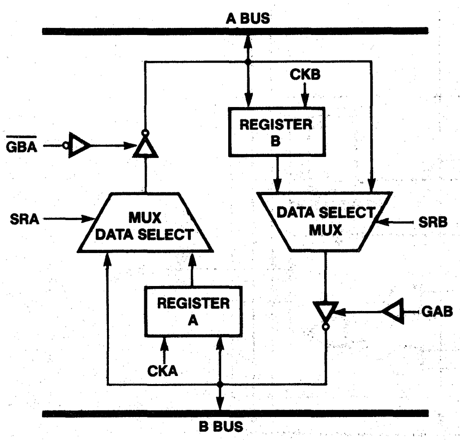


'ACT652

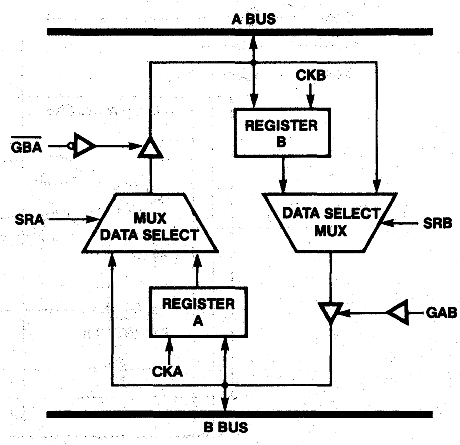


Block Diagrams

'ACT651 (Inverting)



'ACT652 (Non-inverting)



Function Table Nomenclature Description

GAB: To enable A-to-B operation.

$\overline{\text{GBA}}$: To enable B-to-A operation.

GAB	$\overline{\text{GBA}}$	OPERATION DIRECTION
L	L	B-to-A
L	H	A and B buses both are inputs (Storage)
H	L	A and B buses both are outputs (Transfer stored data to bus)
H	H	A-to-B

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is a High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for register A/B.

X: H or L state irrelevant ("Don't Care" condition).

↑: Positive edge of CK causes clocking, if clock enable is asserted.

UC: H or L or ↓ case (nonclocked operation).

RGTR: Register.

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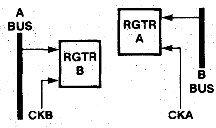
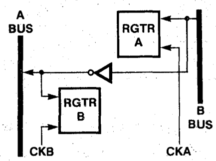
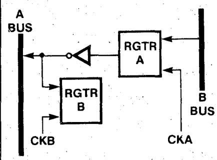
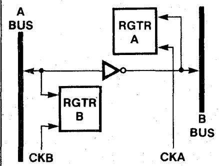
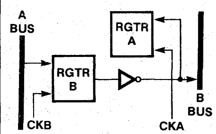
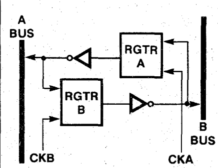
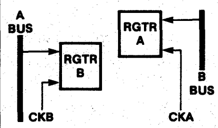
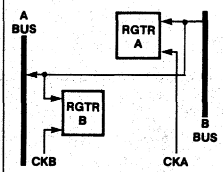
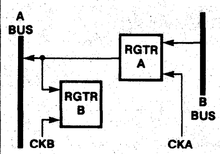
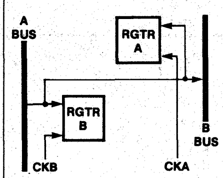
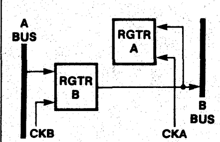
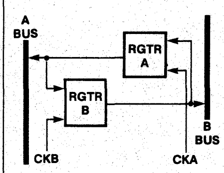
Bus Operation for 'ACT651

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'ACT651
	GAB	$\overline{GBA}$	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	L	H	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time $\overline{B}$ bus data → A bus
								UC	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR B
								↑	UC	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A Real time $\overline{B}$ bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR $\overline{A}$ data → A bus
								UC	↑	RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
Real time A-to-B Operation	H	H	X	L	Input	Output		UC	UC	Real time $\overline{A}$ bus data → B bus
								UC	↑	Real time $\overline{A}$ bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A
								↑	↑	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	H	H	X	H	Input	Output		UC	UC	RGTR $\overline{B}$ data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus
								↑	UC	RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
Transfer Stored Data	H	L	H	H	Output	Output		UC	UC	RGTR $\overline{A}/\overline{B}$ data → A/B bus
								UC	↑	RGTR $\overline{A}/\overline{B}$ data → A/B bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	RGTR $\overline{A}/\overline{B}$ data → A/B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	RGTR $\overline{A}/\overline{B}$ data → A/B bus RGTR $\overline{A}$ data → RGTR B RGTR $\overline{B}$ data → RGTR A

Bus Operation for 'ACT652

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'ACT652
	GAB	$\overline{GBA}$	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	L	H	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time B bus data → A bus
								UC	↑	Real time B bus data → A bus Real time B bus data → RGTR B
								↑	UC	Real time B bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR A data → A bus
								UC	↑	RGTR A data → A bus RGTR A data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR A data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
Real time A-to-B Operation	H	H	X	L	Input	Output		UC	UC	Real time A bus data → B bus
								UC	↑	Real time A bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time A bus data → B bus Real time A bus data → RGTR A
								↑	↑	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	H	H	X	H	Input	Output		UC	UC	RGTR B data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR B data → B bus
								↑	UC	RGTR B data → B bus RGTR B data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A
Transfer Stored Data	H	L	H	H	Output	Output		UC	UC	RGTR A/B data → A/B bus
								UC	↑	RGTR A/B data → A/B bus RGTR A data → RGTR B
								↑	UC	RGTR A/B data → A/B bus RGTR B data → RGTR A
								↑	↑	RGTR A/B data → A/B bus RGTR A data → RGTR B RGTR B data → RGTR A

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Absolute Maximum Ratings

Supply voltage, V_{CC} .... −0.5 V to 7.0 V
DC input voltage, V_I .... −0.5 V to V_{CC} +0.5 V
DC output voltage, V_O .... −0.5 V to V_{CC}+0.5 V
DC output source/sink current per output pin, I_O .... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} .... ±100 mA
Input diode current, I_{IK}:
V_I <0 .... −20 mA
V_I >V_{CC} .... +20 mA
Output diode current, I_{OK}:
V_O <0 .... −20 mA
V_O >V_{CC} .... +20 mA
Storage temperature .... −65 to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
T_A	Operating free-air temperature		−55		125	−40		85	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Set up time		30↑			25↑			ns
t_h	Hold time		0↑			0↑			ns
t_r	Input rise time at V_I = 4.5 V		0		500	0		500	ns
t_f	Input fall time at V_I = 4.5 V		0		500	0		500	ns
I_{OH}	High-level output current				−6			−6	mA
I_{OL}	Low-level output current				12			12	mA

↑ The arrow indicates the Low-to-High transition of the clock input used as reference.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		25°C MIN	25°C TYP	25°C MAX	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.7			0.8	V
V_{IH}	High-level input voltage			2			2			2			V
I_{IN}	Input Current	V_{CC} = MAX	V_I = V_{CC} or GND			±1.0			±1.0			±1.0	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20 μA			0.1			0.1			0.1	V
			I_{OL} = 6 mA			0.32			0.4			0.37	
			I_{OL} = 12 mA			0.4			0.4			0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −20 μA	3.4			3.4			3.4			V
			I_{OH} = −6 mA	2.4			2.4			2.4			
I_{OZ}	Off-state output current	V_{CC} = MAX	V_O = V_{CC} or GND			±10			±50			±30	μA
I_{CC}	Quiescent supply current	V_{CC} = MAX	V_I = V_{CC} or GND			10			80			40	μA
I_C	Maximum quiescent supply current	V_{CC} = MAX	Only one input at 2.4 V			1.5			2.0			1.9	mA
		V_I = 2.4 V or 0.5 V	All inputs at 2.4 V			25			35			33	

Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	COM/MIL T_A = 25°C MIN	COM/MIL T_A = 25°C MAX	MILITARY MIN	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{PLH}	Data to output delay	C_L = 50 pF		39		53		48	ns
t_{PHL}				30		48		42	
t_{PLH}	Clock to output delay			35		50		44	ns
t_{PHL}				30		44		40	
t_{PLH}	Select to output delay* (data input high)			32		44		40	ns
t_{PHL}				32		44		40	
t_{PLH}	Select to output delay* (data input low)			35		50		44	ns
t_{PHL}				30		40		36	
t_{PZL}	$\overline{GBA}$ to A bus output enable delay	R_L = 1KΩ, C_L = 50 pF		25		35		32	ns
t_{PZH}				25		35		32	
t_{PLZ}	$\overline{GBA}$ to A bus output disable delay			25		35		32	ns
t_{PHZ}				35		40		38	
t_{PZL}	GAB to B bus output enable delay			30		35		33	ns
t_{PZH}				25		35		32	
t_{PLZ}	GAB to B bus output disable delay			25		35		32	ns
t_{PHZ}				35		40		38	

* See Figure 4.

Test Waveforms

Setup Time/Hold Time

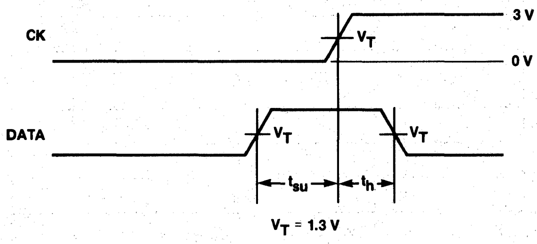


Figure 1

Bus Data To Bus Output Delay

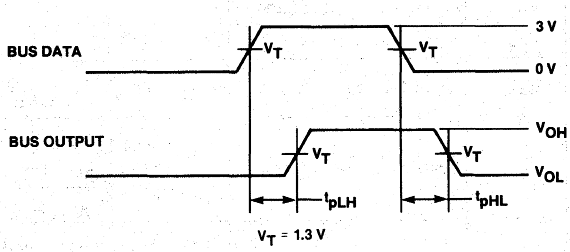


Figure 2

CK To Bus Output Propagation Delay Time

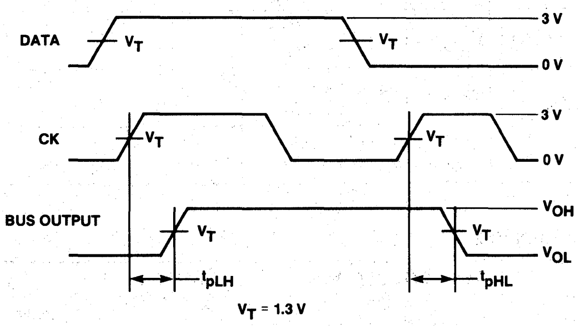
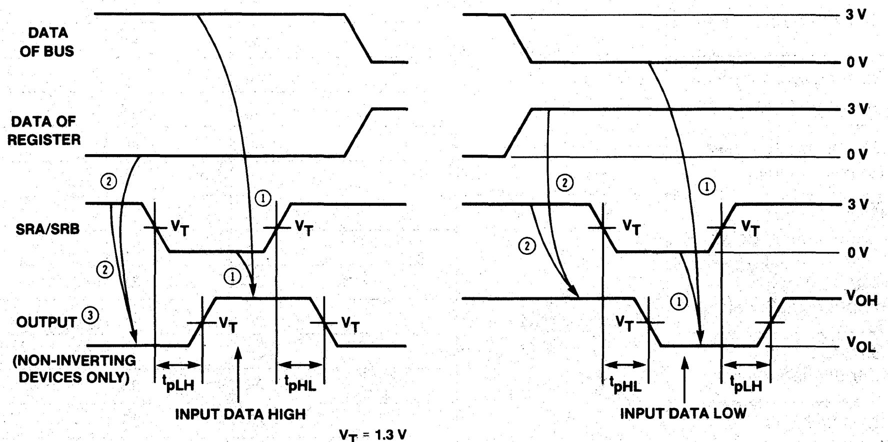


Figure 3

Select To Output Delay



NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Figure 4

Enable/Disable/Direction-Change Delay

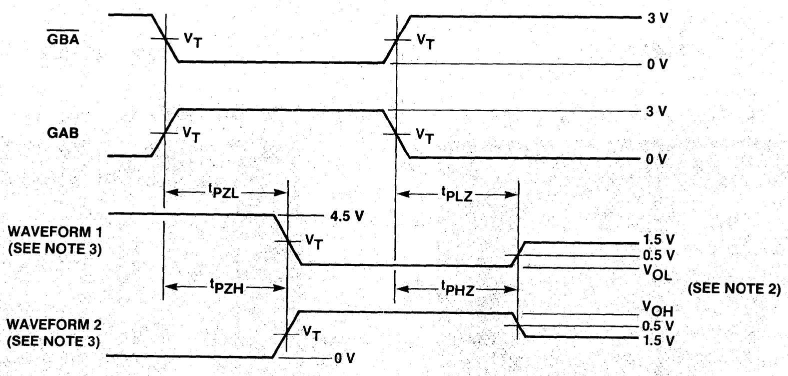


Figure 5

Test Load

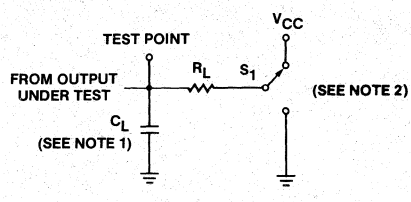


Figure 6

NOTES
1. C_L includes probe and jig capacitance.
2. When measuring t_{PLZ} and t_{PZL}, S_1 is tied to V_{CC}. When measuring t_{PHZ} and t_{PZH}, S_1 is tied to ground.

   When measuring propagation delay times of three-state outputs, S_1 is open, i.e., not connected to V_{CC} or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.

   Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: PRR $\leq$1 MHz, $t_r \leq$6 ns, $t_f \leq$6 ns, Z_{out} = 50 Ω.

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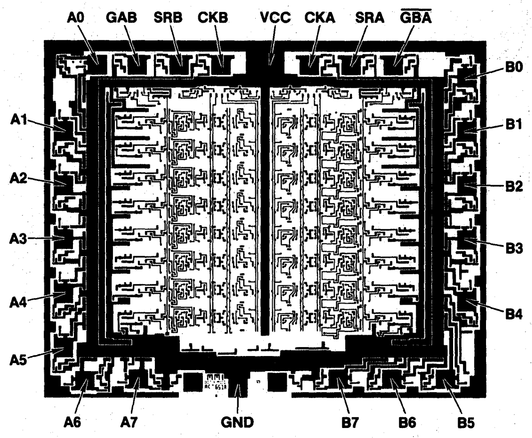
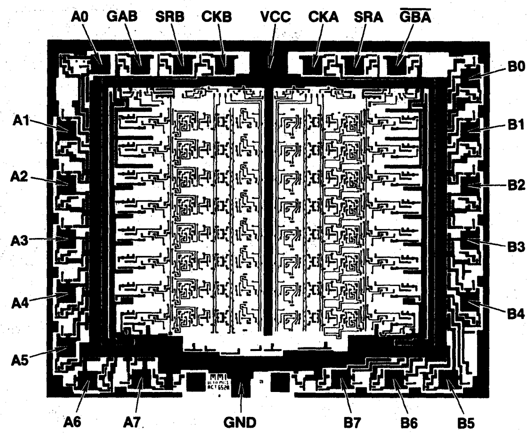
Die Configurations

54/74ACT651



54/74ACT652



Die Size: 87x107 mil^2

Table of Contents
ECL10KH

ECL10KH Selection Guide

DEVICE	FUNCTION	PACKAGE	PINS
	NOR Gate		
MC10H102	Quad 2-Input		
MC10H211	Dual 3-Input, 3-Output		
	OR Gate		
MC10H103	Quad 2-Input		
MC10H210	Dual 3-Input, 3-Output		
	AND Gates		
MC10H104	Quad AND		
	Complex Gates		
MC10H101	Quad OR/NOR		
MC10H105	Triple 2-3-2 Input OR/NOR	J, N	16
MC10H107	Triple Exclusive OR/NOR		
	Flip-Flop Latches		
MC10H130	Dual Latch		
MC10H131	Dual D Master Slave Flip-Flop		
	Data Selector Multiplexer		
MC10H158	Quad 2-Input Multiplexers (Non-inverting)		
MC10H159	Quad 2-Input Multiplexers (Inverting)		
MC10H173	Quad 2-Input Multiplexer Latch		
	Special Function		
MC10H141	Universal Shift Register		

ECL10KH for High Performance System Design.

The designer of high-performance digital systems now has new alternatives with the introduction of Monolithic Memories' ECL 10KH family of Logic. Monolithic Memories' ECL 10KH devices are completely equivalent to Motorola's MECL 10KH. This means that the system designer can take advantage of the high performance of ECL 10KH logic, and eliminate the woe of having a sole-sourced logic family.

ECL logic is used in a broad range of applications that demand high speed and a stable system environment. ECL 10KH represents a particular optimization of semiconductor technology towards ease of use in systems. A summary of the advantages of ECL 10KH may be of use to the system designer.

ECL 10KH, in general, is compatible with 10K ECL logic, but it is faster, offers better noise margin, and operates at equal power as compared to MECL 10K logic. Propagation delays, and clock speeds are 100% better, and noise immunity is improved 75% over the MECL 10K series. The basic power dissipation of 25 mW/Gate is comparable to MECL 10K.

To obtain better circuit speeds, new semiconductor processing is used with ECL 10KH. Smaller transistors result from this processing, allowing greater speed. Other design changes are employed in ECL 10KH, over the basic MECL 10K gate structure, which yield better DC performance as well. ECL 10KH is a voltage-compensated logic family, allowing guaranteed DC and AC parameters over a ±5% power supply range. Voltage-compensation allows for smaller semiconductor die sizes for a given function as compared with ECL devices employing both voltage compensation and temperature compensation. Smaller die sizes translate into a lower production cost, which in turn means a lower cost to the end user.

ECL10KH High-Speed Emitter-Coupled Logic Family
MC10H101
Quad OR/NOR Gate

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- **Propagation delay, 1 ns typical**
- **Power dissipation 25 mW/gate**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible.**

Ordering Information

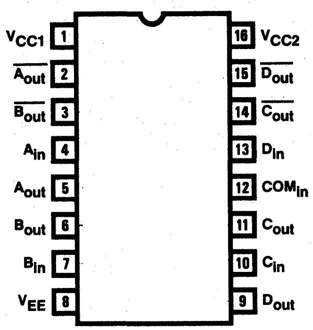
PART NUMBER	PACKAGE	TEMPERATURE
MC10H101	J, N	COM

Description

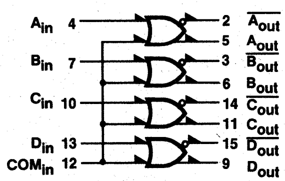
The MC10H101 is a member of Monolithic Memories' ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

MC10H101
Quad OR/NOR Gate



MC10H101



Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) .... -8.0 to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) .... 0 V_{dc} to V_{EE}
Output Current:
  Continuous .... 50 mA
  Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ± 5% (See note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	29	—	26	—	29	mA
I_{inH}	Input current high	MC10H101	—	425	—	265	—	265	μA
		MC10H101 (Pin 12 only)	—	850	—	535	—	535	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

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Switching Characteristics V_{EE} = -5.2 V ± 5% (See note)

SYMBOL	PARAMETER	0°C MIN	0°C MAX	25°C MIN	25°C MAX	75°C MIN	75°C MAX	UNIT
t_{pd}	Propagation delay	0.7	1.6	0.7	1.5	0.7	1.7	ns
t_r	Rise time (20%-80%)	0.7	2.2	0.7	2.0	0.7	2.2	ns
t_f	Fall time (80%-20%)	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H103 Quad 2-Input OR Gate

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

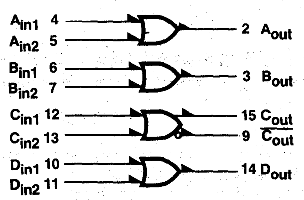
Features/Benefits

- Propagation delay, 1.0 ns typical
- Power dissipation 25 mW/gate
- Noise margin 150 mV
- Voltage compensated
- ECL 10K compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H103	J,N	Com

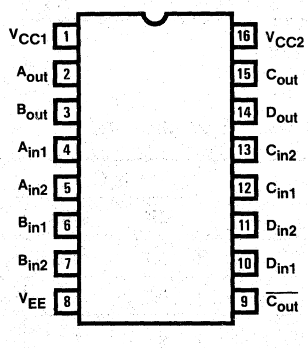
Logic Diagram



Description

The MC10H103 is a member of Monolithic Memories' ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration



Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) .... −8.0 V to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) .... 0 V_{dc} to V_{EE}
Output Current:
Continuous .... 50 mA
Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current	—	29	—	26	—	29	mA
I_{inH}	Input current HIGH	—	425	—	265	—	265	μA
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2V ± 5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	0.7	1.6	0.7	1.5	0.7	1.7	ns
t_r	Rise time (20%-80%)	0.7	2.2	0.7	2.0	0.7	2.2	ns
t_f	Fall time (80%-20%)	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

MC10H102/Quad 2-Input NOR Gate
MC10H105/Triple 2-3-2 Input OR/NOR Gate

Features/Benefits

- **Propagation delay, 1 ns typical**
- **Power dissipation 25 mW/gate**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K compatible.**

Ordering Information

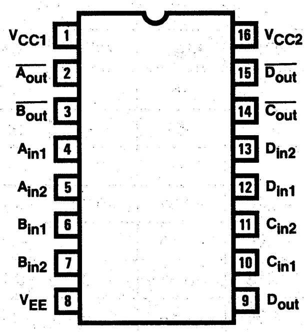
PART NUMBER	PACKAGE	TEMPERATURE
MC10H102	J,N	COM
MC10H105		

Description

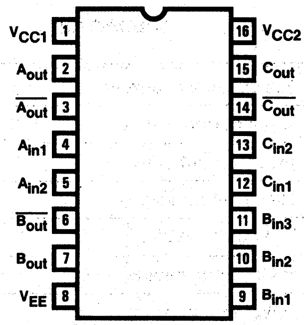
The MC10H102 and MC10H105 are members of Monolithic Memories new ECL family.These ECL 10KH parts are functional/pinout duplications of the standard ECL 10K family parts, with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configurations

MC10H102
Quad 2-Input NOR Gate

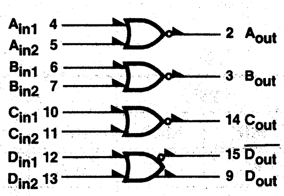


MC10H105
Triple 2-3-2 Input OR/NOR Gate



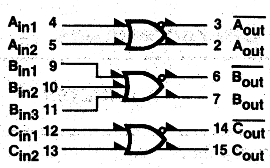
Logic Diagrams

MC10H102



Quad 2-Input NOR Gate

MC10H105



Triple 2-3-2 input OR/NOR Gate

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) .... −8.0 V to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) .... 0 V_{dc} to V_{EE}
Output Current:
Continuous .... 50 mA
Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2V ± 5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current	MC10H102	—	29	—	26	—	29	mA
		MC10H105	—	23	—	21	—	23	
I_{inH}	Input current HIGH		—	425	—	265	—	265	μA
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

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Switching Characteristics V_{EE} = -5.2V ± 5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	0.7	1.6	0.7	1.5	0.7	1.7	ns
t_r	Rise time (20%-80%)	0.7	2.2	0.7	2.0	0.7	2.2	ns
t_f	Fall time (80%-20%)	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE: Each ECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H104/MC10H107 Quad 2-Input AND Gate/Triple 2-Input Exclusive OR/NOR Gate

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation 35 mW/gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

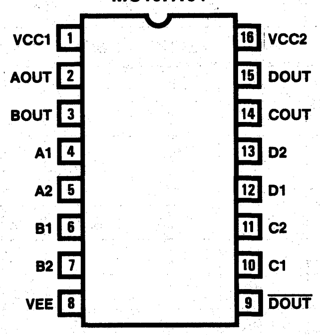
PART NUMBER	PACKAGE	TEMPERATURE
MC10H104 MC10H107	J,N	Com

Description

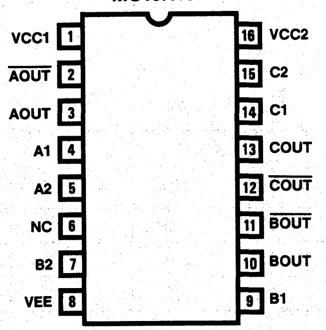
The MC10H104 and MC10H107 are members of Monolithic Memories' new ECL family. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10K family parts with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configurations

MC10H104

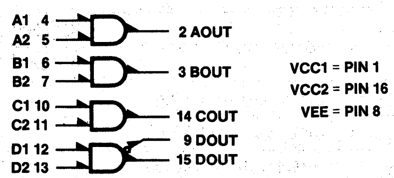


MC10H107



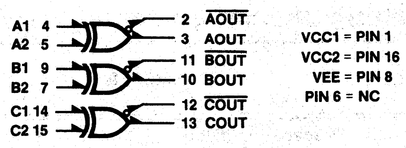
Logic Diagrams

MC10H104



Quad 2-Input AND Gate

MC10H107



Triple 2-Input Exclusive OR/NOR Gate

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Absolute Maximum Ratings

Power supply V_{EE} (V_{CC} = 0) .... −8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) .... 0 Vdc to V_{EE}
Output current:
Continuous .... 50 mA
Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{EE}	Supply Voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		+75	°C
T_{stg}	Storage temperature range	Plastic	-55		+150	°C
		Ceramic	-55		+165	

Electrical Characteristics V_{EE} = −5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current	MC10H104 MC10H107	– –	39 31	– –	35 28	– –	39 31	mA
I_{inH}	Input current HIGH		–	425	–	265	–	265	μA
I_{inL}	Input current LOW		0.5	–	0.5	–	0.3	–	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = −5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	MC10H104 MC10H107	0.7 0.7	2.2 2.0	0.7 0.7	2.0 1.9	0.7 0.7	2.2 2.0	ns
t_r	Rise time		0.7	2.2	0.7	2.0	0.7	2.2	ns
t_f	Fall time		0.7	2.2	0.7	2.0	0.7	2.2	ns

ECL 10KH High-Speed Emitter-Coupled Logic Family Dual Latch MC10H130

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation, 155 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H130 is a dual latch which has two different mechanisms to retain data through latch control signals. Each latch can be operated separately by holding the common latch control signal ($\overline{C}$) LOW, then switching an individual latch control signal ($\overline{CE1}$/$\overline{CE2}$) from LOW to HIGH to cause retention of data in the relevant latch. If simultaneous operation of both latches is required, $\overline{CE1}$ and $\overline{CE2}$ are held LOW and the common latch control C is switched from LOW to HIGH.

For either latch, data present at the inputs (D1/D2) will be seen at the outputs (Q1/$\overline{Q1}$ and Q2/$\overline{Q2}$) when both latch control signals are LOW. This condition allows data to be setup within the latch, after which time causing a positive transition to the HIGH state on either or both latch control signals causes data retention. After either or both of these signals are HIGH, subsequent changes in data at an input are ignored by the latch, provided the hold time requirement is met.

An alternative means to load data in the latches is to use the direct set and reset (S1/S2 and R1/R2, respectively) lines. These inputs do not override the latch controls, or the D inputs. Instead, set or reset are only effective when either $\overline{C}$, $\overline{CE1}$/$\overline{CE2}$ or both, are HIGH. Note that this relationship is different than the case for a similar part, the MC10H131, which is a Dual Master-Slave D-type Flip-Flop.

Function Table

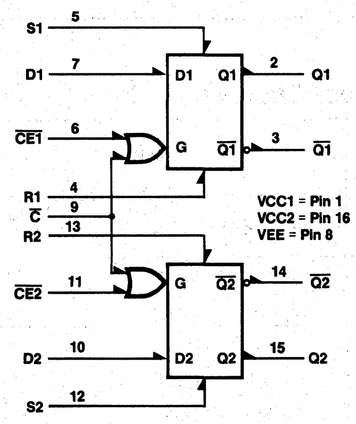
D	$\overline{C}$	$\overline{CE1}$/$\overline{CE2}$	R	S	$Q_{n=1}$
L	L	L	X	X	L
H	L	L	X	X	H
X	H	X	L	L	Q_n
X	H	X	L	H	H
X	H	X	H	L	L
X	H	X	H	H	N.D.
X	X	H	L	L	Q_n
X	X	H	L	H	H
X	X	H	H	L	L
X	X	H	H	H	N.D.

X = Don't Care
N.D. = Not Defined

Ordering Information

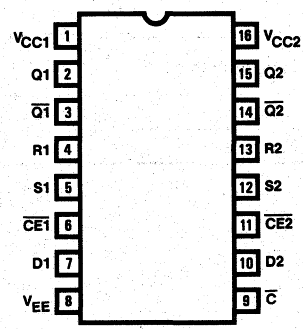
PART NUMBER	PACKAGE	TEMPERATURE
MC10H130	J,N	Com.

Logic Diagram



Pin Configuration

MC10H130
Dual Latch



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Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) .... -8.0 V to $0V_{dc}$
Input voltage V_I (V_{CC} = 0) .... $0V_{dc}$ to V_{EE}
Output Current:
Continuous .... 50 mA
Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_{stg}	Storage temperature	Plastic	-55		+150	°C
		Ceramic	-55		+165	
T_A	Operating temperature range		0		+75	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	38	—	35	—	38	mA
I_{inH}	Input current HIGH	Pins 6, 11	—	468	—	275	—	275	μA
		Pins 7, 9, 10	—	545	—	320	—	320	
		Pins 4, 5, 12, 13	—	434	—	255	—	255	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2V, ±5% (See note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Clock	0.7	2.2	0.7	2.1	0.7	2.2	ns
		Data, Set, Reset	0.7	2.0	0.7	1.8	0.7	2.0	
t_r	Rise time (20%-80%)		0.7	2.2	0.7	2.0	0.7	2.2	ns
t_f	Fall time (80%-20%)		0.7	2.2	0.7	2.0	0.7	2.2	ns
t_{set}	Setup time		2.2	—	2.2	—	2.2	—	ns
t_{hold}	Hold time		0.7	—	0.7	—	0.7	—	ns

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

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ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H131 Dual Master-Slave Type D Flip-Flop

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- **Propagation delay, 1 ns typical**
- **Power dissipation, 235 mW typical**
- **Noise margin of 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

The MC10H131 is a member of Monolithic Memories' ECL family. The MC10H131 is a dual master-slave D-type flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking fuction. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the controlling input(s). A change in the information present at the data (D) input will not affect the data output at any other time due to master slave construction.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power supply current.

Function Tables

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined.

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H↑	L	L
H↑	H	H

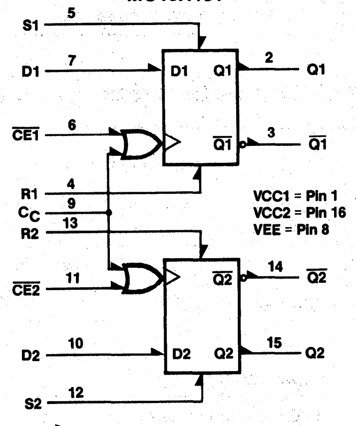
X = Don't Care.
C = $\overline{CE}$ + C_C.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H131	J,N	Com.

Logic Diagram

MC10H131

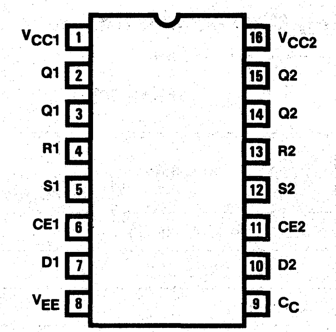


> : denotes edge triggered clock

Pin Configuration

MC10H131

Dual Master-Slave Type D Flip-Flop



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Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) .... –8.0 to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) .... 0 V_{dc} to V_{EE}
Output Current:
Continuous .... 50 mA
Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{EE}	Supply voltage		–5.46	–5.2	–4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	62	—	56	—	62	mA
I_{inH}	Input current HIGH	Pins 6, 11	—	530	—	310	—	310	µA
		Pin 9	—	660	—	390	—	390	
		Pins 7, 10	—	485	—	285	—	285	
		Pins 4, 5, 12, 13	—	790	—	465	—	465	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

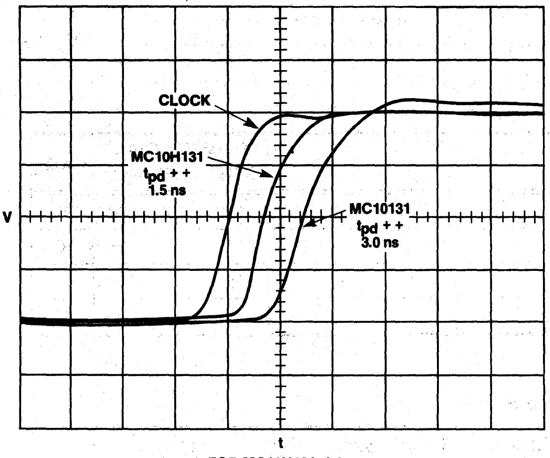
Switching Characteristics V_{EE} = -5.2 V ±5% (See note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Clock to Q	0.7	2.0	0.7	2.0	0.7	2.1	ns
		Set, Reset to Q	0.7	2.0	0.7	2.0	0.7	2.1	
t_r	Rise time (20%–80%)		0.7	2.3	0.7	2.3	0.7	2.5	ns
t_f	Fall time (80%–20%)		0.7	2.3	0.7	2.3	0.7	2.5	ns
t_{set}	Setup time		0.7	—	0.7	—	0.7	—	ns
t_{hold}	Hold time		0.7	—	0.7	—	0.7	—	ns
f_{tog}	Toggle frequency		250	—	250	—	250	—	MHz

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

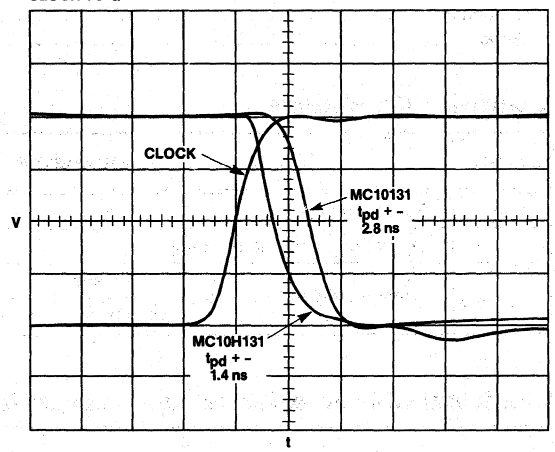
Switching Time Comparison ECL 10KH versus ECL 10K

CLOCK TO Q



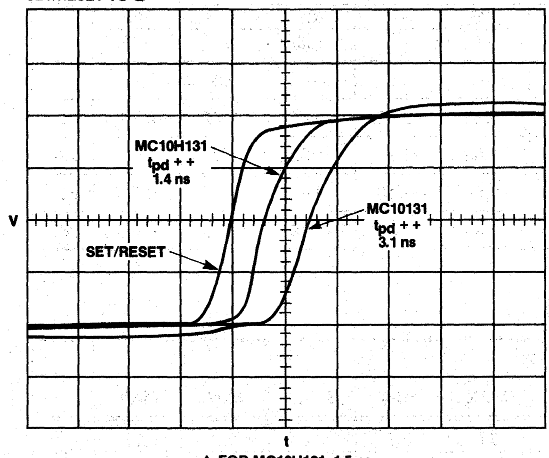
t_r FOR MC10H131: 1.4 ns
t_r FOR MC10131: 2.0 ns

CLOCK TO $\overline{Q}$



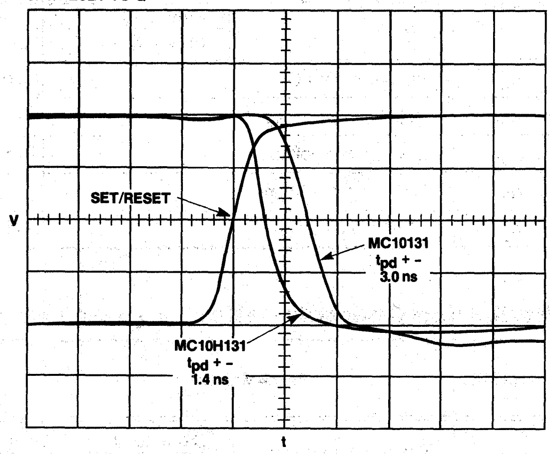
t_f FOR MC10H131: 1.2 ns
t_f FOR MC10131: 1.4 ns

SET/RESET TO Q



t_r FOR MC10H131: 1.5 ns
t_r FOR MC10131: 2.1 ns

SET/RESET TO $\overline{Q}$



t_f FOR MC10H131: 1.2 ns
t_f FOR MC10131: 1.5 ns

NOTE: t_r and t_f measured from the 20% to the 80% level of the output signal swing.
t_{pd} is measured from the 50% level of the input to the 50% level of the output.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H141
Four-Bit Universal Shift Register

PRELIMINARY INFORMATION
This document contains specifications and information which are subject to change.

Features/Benefits
- Shift frequency, 250 MHz min
- Power dissipation, 425 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description
The MC10H141 is a four-bit universal shift register which performs shift-left, or shift-right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control

(See following page)

Function Table

SELECT		OUTPUTS				OPERATION
S1	S2	$Q0_{n-1}$	$Q1_{n-1}$	$Q2_{n-1}$	$Q3_{n-1}$	
L	L	D0	D1	D2	D3	Parallel entry
L	H	$Q1_n$	$Q2_n$	$Q3_n$	DR	Shift right*
H	L	DL	$Q0_n$	$Q1_n$	$Q2_n$	Shift left*
H	L	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$	Stop shift

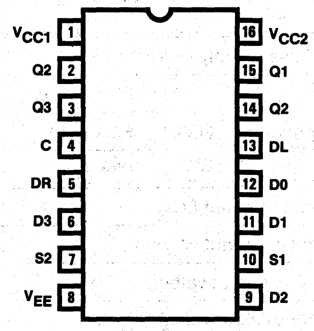
* Outputs as exist after pulse appears at "C" input with input conditions as shown (Pulse Positive transition of clock input).

Ordering Information

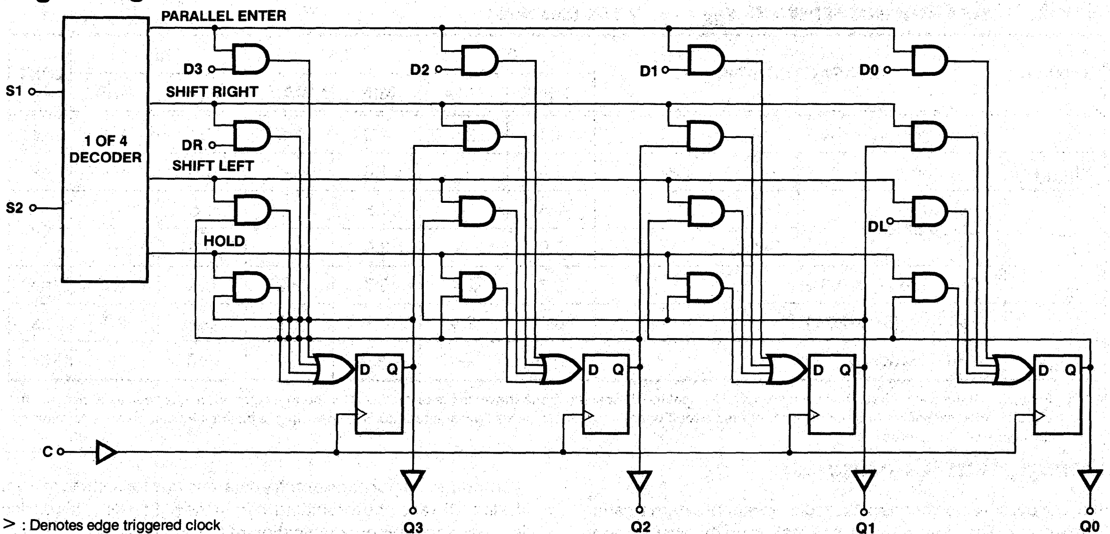
PART NUMBER	PACKAGE	TEMPERATURE
MC10H141	J, N	Com

Pin Configuration

MC10H141
Four-Bit Universal Shift Register



Logic Diagram



> : Denotes edge triggered clock

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Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{EE} (V_{CC} = 0) .... -8.0 V to 0 V_{dc}
Input voltage, V_I (V_{CC} = 0) .... 0 V_{dc} to V_{EE}
Output Current:
Continuous .... 50 mA
Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating free-air temperature		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current		—	112	—	102	—	112	mA
I_{inH}	Input current HIGH	Pins 5, 6, 9, 11, 12, 13	—	405	—	255	—	255	μA
		Pins 7, 10	—	416	—	260	—	260	
		Pins 4,	—	510	—	320	—	320	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-0.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	CHARACTERISTIC		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay		1.1	2.0	1.0	1.9	1.1	2.1	ns
t_{hold}	Hold time		1.0	—	1.0	—	1.0	—	ns
t_{set}	Setup time	Data	1.5	—	1.5	—	1.5	—	ns
		Select	3.0	—	3.0	—	3.0	—	
t_r	Rise time (20%-80%)		0.7	2.4	0.7	2.2	0.7	2.4	ns
t_f	Fall time (80%-20%)		0.7	2.4	0.7	2.2	0.7	2.4	ns
f_{shift}	Shift frequency		250	—	250	—	250	—	MHz

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

Description (Continued)

the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift-left, shift-right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR). This device is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay and operation frequency and no increase in power supply current.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H158 QUAD 2-Input Multiplexer

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- **Propagation delay, 1.5 ns typical**
- **Power dissipation, 197 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-Compatible**

Description

The MC10H158 is a member of Monolithic Memories' ECL Family. The MC10H158 is a quad 2-input multiplexer. When the select line (SELECT) is LOW D_1 data appear at the outputs (Q3-Q0). Conversely, when the select input is HIGH, D_0 data appear at the outputs. This ECL part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

MC10H158 Function Table

SELECT	D_0*	D_1*	Q
L	X	L	L
L	X	H	H
H	L	X	L
H	H	X	H

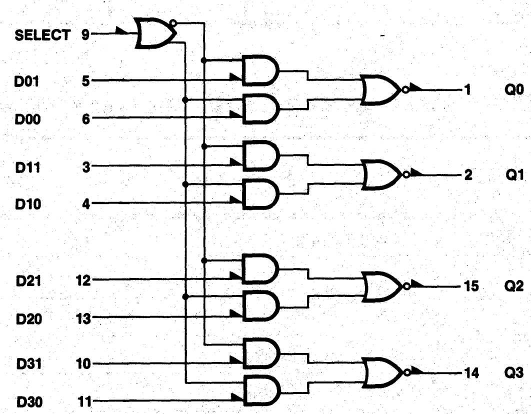
* D_0/D_1 indicate each of four bit positions for the "zero" or "one" inputs, as controlled by the select line.

X = Don't care.

Ordering Information

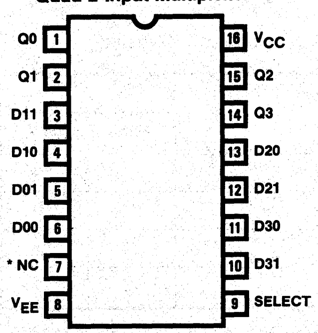
PART NUMBER	PACKAGE	TEMPERATURE
MC10H158	J, N	COM

Logic Diagram



V_{EE} Pin 8
V_{CC} Pin 16

Pin Configuration



* NC-No connection

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Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{EE} (V_{CC} = 0) .... –8.0 to 0 V_{dc}
Input voltage, V_I (V_{CC} = 0) .... 0 V_{dc} to V_{EE}
Output Current:
Continuous .... 50 mA
Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply Voltage		–5.46	–5.2	–4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	–55		150	°C
		Ceramic	–55		165	

Electrical Characteristics V_{EE} = –5.2 V ±5% (See note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	53	—	48	—	53	mA
I_{inH}	Input current HIGH	Pin 9	—	475	—	295	—	295	μA
		Pins 3-6 and 10-13	—	515	—	320	—	320	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	LOW output voltage		–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	HIGH input voltage		–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	LOW input voltage		–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

Switching Characteristics V_{EE} = 5.2 V ±5% (See note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data	1.0	1.9	1.0	1.8	1.0	2.0	ns
		Select	1.0	2.9	1.0	2.7	1.0	2.9	
t_r	Rise time (20%-80%)		0.7	2.2	0.7	2.0	0.7	2.2	ns
t_f	Fall time (80%-20%)		0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTES: Each ECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H159 Quad 2-Input Inverting Multiplexer with Enable

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- Propagation delay, 1.5 ns typical
- Power dissipation, 218 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

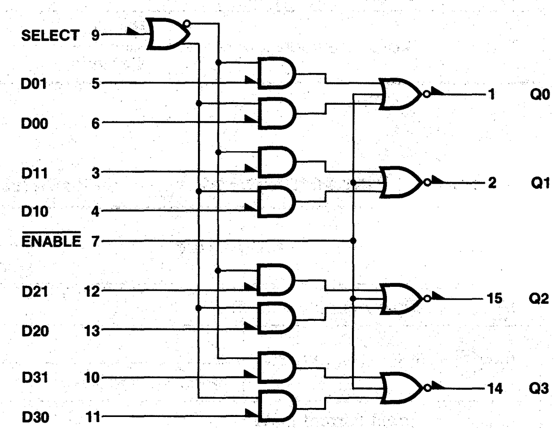
PART NUMBER	PACKAGE	TEMPERATURE
MC10H159	J, N	COM

Description

The MC10H159 is a member of Monolithic Memories' ECL family. The MC10H159 is a quad 2-input inverting multiplexer with enable. A HIGH level on the enable input (ENABLE) overrides the select input (SELECT) and forces all of the outputs (Q3-Q0) to the LOW level. A LOW level on the enable input allows multiplexer action, which is controlled by the select input. When the select input is LOW, D_1 data appear at the outputs. Conversely, when the select input is HIGH, D_0 data appear at the outputs.

Logic Diagram

MC10H159



V_{EE} Pin 8
V_{CC} Pin 16

MC10H159 Function Table

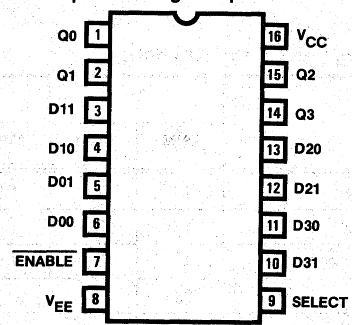
ENABLE	SELECT	D0	D1	Q
L	L	X	L	H
L	L	X	H	L
L	H	L	X	H
L	H	H	X	L
H	X	X	X	L

* D_0/D_1 indicate each of 4 bit positions for the "zero" or "one" inputs, as controlled by the select line.

X = Don't care.

Pin Configuration

MC10H159
Quad 2-Input Inverting Multiplexer with Enable



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Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) .... –8.0 to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) .... 0 V_{dc} to V_{EE}
Output Current:
  Continuous .... 50 mA
  Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN TYP MAX	UNIT
V_{EE}	Supply voltage		–5.46 –5.2 –4.94	V
T_A	Operating temperature range		0 75	°C
T_{stg}	Storage temperature range	Plastic	–55 150	°C
		Ceramic	–55 165	

Electrical Characteristics V_{EE} = –5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current		—	58	—	53	—	58	mA
I_{inH}	Input current HIGH	Pin 9	—	475	—	295	—	295	µA
		Pins 3-7 and 10-13		515	—	320	—	320	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.75	-1.45	Vdc

Switching Characteristics V_{EE} = –5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	Data	1.0	2.2	1.0	2.0	1.0	2.2	ns
		Select	1.0	3.2	1.0	3.0	1.0	3.2	
		Enable	1.0	3.2	1.0	3.0	1.0	3.2	
t_r	Rise time (20%-80%)		0.7	2.2	0.7	2.0	0.7	2.2	ns
t_f	Fall time (80%-20%)		0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H173 QUAD 2-Input Multiplexer With Latch

PRELIMINARY INFORMATION
This document contains specifications and information which are subject to change.

Features/Benefits

- **Propagation delay, 1.5 ns typical**
- **Power dissipation, 275 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Ordering Information

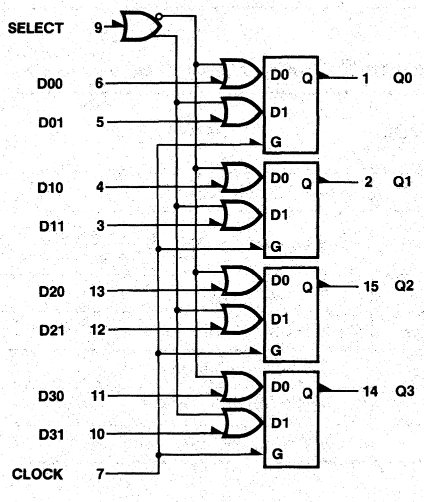
PART NUMBER	PACKAGE	TEMPERATURE
MC10H173	J, N	Com

Description

The MC10H173 is a quad 2-input multiplexer with latch. This device is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay and no increase in power-supply current.

It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the data outputs.

Logic Diagram

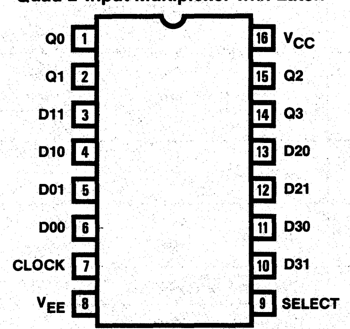


MC10H173 Function Table

SELECT	CLOCK	$Q_n = 1$
H	L	D00
L	L	D01
X	H	$Q0_n$

X = Don't care.

Pin Configuration



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Absolute Maximum Ratings

Supply voltage, V_{EE} (V_{CC} = 0) .... -8.0 to 0 V_{dc}
Input voltage, V_I (V_{CC} = 0) .... 0 V_{dc} to V_{EE}
Output Current:
Continuous .... 50 mA
Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current		—	73	—	66	—	73	mA
I_{inH}	Input current HIGH	Pins 3-7 and 10-13	—	510	—	320	—	320	μA
		Pin 9	—	475	—	300	—	300	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = 5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	Data	0.7	2.3	0.7	2.1	0.7	2.3	ns
		Clock	1.0	3.7	1.0	3.5	1.0	3.7	
		Select	1.0	3.6	1.0	3.4	1.0	3.6	
t_{set}	Setup time	Data	0.7	—	0.7	—	0.7	—	ns
		Select	1.0	—	1.0	—	1.0	—	
t_{hold}	Hold time	Data	0.7	—	0.7	—	0.7	—	ns
		Select	1.0	—	1.0	—	1.0	—	
t_r	Rise time (20%-80%)		0.7	2.4	0.7	2.1	0.7	2.4	ns
t_f	Fall time (80%-20%)		0.7	2.4	0.7	2.1	0.7	2.4	ns

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

ECL 10 KH High-Speed Emitter-Coupled Logic Family MC10H210/MC10H211 3-Input, 3-Output OR/NOR Gates

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- Propagation delay, 1.0 ns typical
- Power dissipation, 160 mW typical
- Noise margin 150 mV (over operating voltage and temperature range)
- Voltage compensated
- ECL 10K-compatible

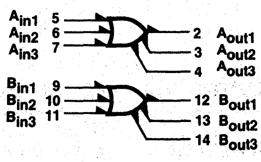
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H210	J	Com
MC10H211	N	

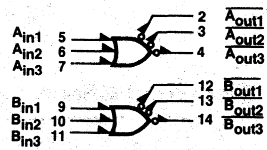
Description

The MC10H210 and MC10H211 are members of Monolithic Memories' ECL family. These devices are dual 3-input, 3-output "OR" and "NOR" gates respectively. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10KH family parts, with 100% improvement in propagation delay and no increase in power supply current.

MC10H210

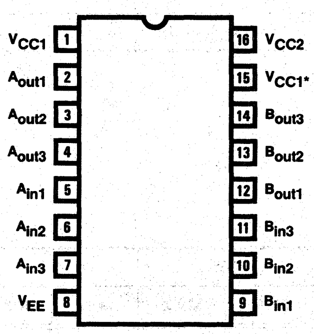


MC10H211



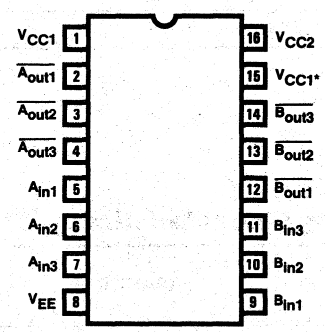
Pin Configurations

MC10H210
3-INPUT 3-OUTPUT OR GATE



* Pins 1 and 15 internally connected

MC10H211
3-INPUT 3-OUTPUT NOR GATE



* Pins 1 and 15 internally connected

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Absolute Maximum Ratings

Supply voltage, V_{EE} (V_{CC} = 0) .... -8.0 V to 0 V_{dc}
Input voltage, V_I (V_{CC} = 0) .... 0 V_{dc} to V_{EE}
Output Current:
Continuous .... 50 mA
Surge .... 100 mA

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL MIN TYP MAX	UNIT
V_{EE}	Supply voltage	-5.46 -5.2 -4.94	V
T_A	Operating free-air temperature	0 75	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current	—	42	—	38	—	42	mA
I_{inH}	Input current HIGH	—	720	—	450	—	450	μA
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} -5.2 V, ± 5%,

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	0.7	1.6	0.7	1.5	0.7	1.7	ns
t_r	Rise time (20%-80%)	0.7	2.2	0.7	2.0	0.7	2.2	ns
t_f	Fall time (80%-20%)	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTES: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

Setup Time

Setup time, t_{su}

The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IC}

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Negative-going threshold voltage, V_{T}

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

Positive-going threshold voltage, V_{T+}

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

Truth Table Explanations

H	=	high level (steady-state)
L	=	low level (steady-state)
↑	=	transition from low to high level
↓	=	transition from high to low level
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a..h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output.

Clock Frequency

Maximum clock frequency, f_{max}

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, I_{IH}

The current into * an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}

The current into * an output with input conditions applied that according to the product specification will establish a high level at the output.

High-level output current, I_{CEX}

The high-level leakage current of an open collector output.

Low-level input current, I_{IL}

The current into * an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}

The current into * an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}

The current into * an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}

The current into * an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}

The current into * the V_{CC} supply terminal of an integrated circuit.

*Current out of a terminal is given as a negative value.

Hold Time

Hold time, t_h

The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, t_{PXZ}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

t_{EA} is the output enable access time of memory devices.
t_{ER} is the output disable (enable recovery) time of memory devices.

Propagation Time

Propagation delay time, t_{PD}

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{AA} is the address (to output) access time of memory devices.

Pulse Width

Pulse width, t_w

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

AVAILABLE LITERATURE

Military Products Division Brochure
Monolithic Memories Inc. Annual Report
PROM Cross-Reference Guide
SHRP—Super High Reliability Products Brochure
PROM/Programmer's Reference Guide
Leadless Brochure

BOOKS

LSI Data Book
PAL Handbook
System Design Handbook
PLE Handbook

APPLICATION NOTES
(Standalone)

AN-100
PROMs, PALs, FIFOs, AND MULTIPLIERS TEAM UP TO IMPLEMENT SINGLE-BOARD HIGH-PERFORMANCE AUDIO SPECTRUM ANALYZER
(System Handbook, Section 1)

The teamwork of a logic device (PAL), a memory device (PROM), a buffer (FIFO), and multiplier chips makes cost-effective and efficient digital signal processing (DSP). This idea is illustrated through the audio spectrum analyzer, but is not limited to that use. Creative designers will soon develop low cost/high performance architectures that can perform as well as the example given.

AN-115
THE DESIGN AND APPLICATION OF A HIGH-SPEED MULTIPLY/DIVIDE BOARD FOR THE STD BUS.
Northcon/82 Session 15
(System Design Handbook, Section 5)

A fundamental limitation in most microcomputer systems is high-speed arithmetic computing speed, especially when multiplications or divisions are required. A hardware multiply/divide board designed to work efficiently with a STD BUS microcomputer in an industrial control system is presented.

The described includes the simultaneous calculation of several digitally-controlled servo loops which allow control of machinery to within the resolution of servo position sensors at a bandwidth that software alone cannot accomplish.

AN-118
PSEUDO RANDOM NUMBER GENERATOR (A DISGUISED PAL)
(System Design Handbook, Section 9)

Due to their interesting properties, Pseudo Random Numbers (PRN) are useful across a wide spectrum of applications, including secure communication, test pattern generation, scramblers, and radar ranging systems. For the requirements of a given application, a "customized" PRN generator is readily implemented using PALs.

AN-123
SHADOW REGISTER ARCHITECTURE SIMPLIFIES DIGITAL DIAGNOSIS
(System Design Handbook, Section 2)

A series of new devices including register and PROMs with diagnostics now make it easier for system designers to include diagnostic circuitry in microprogrammed systems. When in the diagnostic mode, these devices allow for complete system controllability and observability with a minimum of additional hardware. Other schemes such as embedding diagnostic code in a digital system and LSSD (Level-Sensitive Scan Design) have been used in the pass but these techniques have their drawbacks. This new series of products as well as microprogrammed architectures using these products will be explored in this paper.

AN-126
PROMs AND PLEs: AN APPLICATION PERSPECTIVE

Programmable Read Only Memories are widely used in digital systems, both as a memory device, as well as a Programmable Logic Element (PLE™). This document describes the use of PROMs and PLEs in many practical applications ranging from Diagnostic Microsequencers, to M-Bit Parallel CRC. The concept of testability and built-in Diagnostics in the PROMs is also illustrated.

AN-127
DIAGNOSTIC DEVICES AND ALGORITHMS FOR TESTING DIGITAL SYSTEMS

A new concept called Diagnostics On Chip™ (DOC™) was introduced in the industry recently. A series of new products with shadow register diagnostic capability is coming. These new products use this new concept and will provide a cost-effective solution to the issue of testability for digital systems.

AN-128
THE THIRD WAVE HITS SILICON VALLEY

High-technology products and industries are not exempt from the effects of major long-term social trends. Some of today's trends are customization or "de-massification," decentralization, self-help, user-friendliness or "high touch," and appropriate scale. These trends are already affecting the ways in which semiconductors are designed and used, and such human-factors issues will be crucially important in the near future.

AN-129
HIGH-SPEED PROMS WITH ON-Chip REGISTERS AND DIAGNOSTICS

A family of High-Speed Registered and Diagnostic PROMs offer new savings for system designers. The Registered PROM family features on-chip "D"-type output registers which are useful in pipelined systems and state machines. In addition to output registers, the Diagnostic PROMs feature a Shadow Register which makes it easier for system designers to include diagnostics in microprogrammed systems. Architectures and applications for these devices are discussed in this paper.

AN-130
NEXT GENERATION PROGRAMMABLE LOGIC

Programmable logic devices have evolved from simple combinatorial arrays to devices with features and densities that rival gate arrays. This paper opens with a description of second generation PALs; specifically, MegaPALs and Registered-Asynchronous PALs. Then a new concept in programmable logic, called PLE, is introduced. A discussion of design methodology for programmable logic devices follows. The paper closes with a description of present and next generation software tools, PALASM2 and PLEASM, including several application examples using these software tools.

AN-131
NEW PAL® ARCHITECTURE PROVIDES SYNCHRONOUS AND ASYNCHRONOUS FEATURES IN A SINGLE PACKAGE

The new PAL20RA10 is the ultimate general purpose tool for integrating random logic system "glue" and asynchronous control/handshake circuitry. Both synchronous and asynchronous circuits may be integrated within the same PAL, with a considerable reduction of package count.

AN-132
ARITHMETIC COMPUTING FOR INDUSTRIAL CONTROL

The availability of various new multiplier/divider integrated circuits has enabled inexpensive microprocessor systems to perform real-time control tasks that previously required high-performance minicomputers. By joining the speed of a multiplier with the versatility of a microprocessor, real-time control tasks can be implemented with reasonable cost and good performance. Such real-time applications include motion-control, tool positioning and other related servo-loop control functions.

This paper describes a hypothetical control system for an industrial process that currently exists. The concept of an arithmetic-aided microprocessor is presented mindful of this real application, and the subject is developed tutorially. By reviewing the various issues of a real system and the benefits provided by the composite of math IC and microprocessor in this manner, new applications should become evident.

AN-134
DYNAMIC RAM CONTROLLER AND PAL®
SIMPLIFY MC6809E TO 64K DRAM INTERFACE

Most microprocessor systems use dynamic RAM for data and program storage because it is still the most effective way of realizing large memory array configurations with a relatively small total component cost. Compared with static RAM, dynamic RAM requires more complex interface and refresh control circuitry, representing an increase in chip count on dynamic RAM boards. Fortunately, this problem of interface and refresh has been reduced by the availability of a number of dedicated LSI dynamic RAM controller chips. Also, with the application of PAL Programmable Array Logic, microprocessor and DRAM controller interface may be simplified.

CONFERENCE PROCEEDINGS

CP-113
SERIALIZING FIFO AND BURST ERROR PROCESSOR TEAM UP TO ENHANCE SERIAL DATA RELIABILITY

In high-speed serial data transmission, as in state-of-the-art disk drives and data communication there is a growing need for data reliability.

The Single Burst Error Recovery chip, SiBER, can correct 5, 8, or 11-bit bursts of error or detect double burst errors in high-speed serial data bit streams. This paper describes serial-data error detection and correction in host independent and peripheral-independent environments. The SiBER implements the standard CCITT CRC polynomial and a computer generated polynomial in one 24-pin bipolar LSI chip.

CP-114
A DSP ARCHITECTURE FOR A 4800BPS MODEM

This paper describes a hardware configuration of a multiplier chip, the 74S516 and an 8-bit microprocessor, the 8051, and together with other IC's they form a digital signal processor.

This DSP is used to build a modem where the main task is to convert the received signal into a 48-bits/second serial stream.

CP-115
MEMORY ALIASING TO IMPROVE
MATH PROCESSOR PERFORMANCE*

During the past few years, microprocessors have found applications in almost every field. However, those areas requiring high-speed mathematical operations have been limited by the relatively slow multiply and divide operations. The recent introduction of high-speed multipliers and multiplier/dividers has helped to alleviate this problem. In many cases, more time is now spent getting data to and from these devices than is used for the actual computation. This paper presents a method called "Memory Aliasing" that reduces the data flow time to half of the nominal value. A discussion of what constitutes memory aliasing and how to use it is provided. A case study illustrates the performance improvements using a Z8002B microprocessor and a Monolithic Memories' 74S516 multiplier/divider.

CP-116
SYSTEM SOLUTIONS FOR A HIGH-SPEED PROCESSOR USING INNOVATIVE ICs

The need for high-speed building blocks for pipelined processors is prevalent. The following article is a description of the elements of a high speed processor design that uses an instruction lookahead unit, control store unit and floating point adders, subtracters and multiplier.

CP-117
LSI CONTROL AND ERROR
CORRECTION FOR DYNAMIC RAMS

Dynamic Random Access Memories (DRAMs) take a leading place as a semiconductor volatile storage medium. Formerly used strictly for moderate-performance low-cost applications, dynamic memories today are more attractive for high-end applications due to greater density and better AC performance, and they draw more designers to cope with the more complicated access and refresh schemes needed for the dynamic RAMs.

The purpose of this paper is to present several LSI solutions for DRAM control and Error Detection and Correction (EDC) along with examples to show their place in a system.

CP-118 *(Will be available soon.)*
THE A B C OF DYNAMIC RAMS

Dynamic Random Access Memories (DRAMs), being dense and cost effective, take a leading place as semiconductor volatile storage medium. Formerly used strictly for moderate-performance low-cost applications, dynamic RAMS today get faster and become more attractive for high end applications as well. In order to take advantage of the cost efficiency of the dynamic RAMs, more designers are willing to cope with the more complicated access and refresh schemes.

The purpose of this paper is to introduce the dynamic RAMs to the designer unfamiliar with this form of memory. A short comparison between static and dynamic RAMs is followed by descriptions of access and refresh cycles for the dynamic RAMs. Several refresh strategies are discussed and a system solution is presented.

CP-119 *(Will be available soon.)*
The A-TO-Z OF HIGH-SPEED PRIORITY ENCODERS: ARBITRATION TO ZERO DETECTION

Priority encoders are classical "Medium-Scale Integration" (MSI) logic-operator devices. They were originally developed for parallel scanning of interrupts and status signals. Subsequently, they have been used for normalization scanning in hgh-performance floating-point adders/subtractors, for control of digital-system buses and other centralized resources, and for other specialized applications which assume the same basic logical form.

Today very-high-speed TTL-compatible priority encoders are finally available, in both totem-pole-output and three-state-output forms. The cascadable architecture of these parts allows for economical and convenient scanning of any number of inputs.

CP-120 *(Will be available soon.)*
LSI CONTROL AND ERROR CORRECTION FOR DYNAMIC RAMS

Dynamic Random Access Memories (DRAM), take a leading place as semiconductor volatile storage medium. Formerly used strictly for moderate-performance low-cost applications, dynamic memories today are more attractive for high-end applications due to the greater density and better AC performance, and draw more designers to cope with the more complicated access and refresh schemes needed for the dynamic RAMs.

The purpose of this paper is to present several LSI solutions for DRAM control and Error Detection and Correction (EDC) along with examples to show their place in a system.

CP-122
HIGH-PERFORMANCE DIGITAL MUSIC SYNTHESIS

The goal of presenting the digital synthesizer in this paper is to demonstrate a more unified system for a variety of situations. The synthesizer is useful for many artistic explorations besides traditional musical concerts. This design is aimed at new application areas where the interface requirements preclude effective use of present machines. It maintains the broad capabilities at a low cost.

Part of the development of this project is research into sound generation methods. The primary signal processing technique for the system is CORDIC. The CORDIC algorithm is introduced in this paper along with a short history.

An expanding bibliography is included for the benefit of new research. We hope that new applications will result from some of the information.

CP-123
MULTIPROCESSING ARCHITECTURES: A NEW FRONTIER FOR VLSI APPLICATIONS

Except for special application areas, computer performance has generally been enhanced and achieved by the requirements of Von Neumann's basic concepts. Advances in semiconductor components have had more influence on computer performance than any other single factor.

Over the last few decades, the major thrust in computer technology has been to increase the raw computing power of large machines. For complex applications, high-speed number crunching, and new innovative applications, there is a demand for multiple microprocessor systems to provide additional computing power.

In this paper we will discuss the architecture of a typical system which has a main microprocessor doing decision jobs and number crunching, etc., while being helped by four other I/O processors. In other words, this paper deals with hardware building blocks for a multiprocessing system.

ARTICLE REPRINTS

AR-100
PAL SHRINKS AUDIO SPECTRUM ANALYZER (PART 1 OF 2)

Using an audio spectrum analyzer as the example, the author demonstrates how PALs can reduce board space, maximize performance, save money, and improve quality for DSP. Specific diagrams offer ways a designer can build versatility into the microprogram to create other applications.

AR-101
PAL SPECTRUM ANALYZER IMPROVES PERFORMANCE (PART 2 OF 2)

Continuing the idea from the first part of this two part paper (AR-100), the author adds ideas from the reality of high performance to the use of PALs in DSP architecture. Control logic is the key to success since PALs have flexibility coding. Simplified tables and diagrams round out the author's illustration.

AR-108
STATE-OF-THE-ART IN HIGH SPEED ARITHMETIC INTEGRATED CIRCUITS

Use of bipolar technology to construct arithmetic ICs has resulted in devices with increasing switching speed and gate density and low power dissipation. Future technological advances should have an even greater impact on product performance through larger wafer diameters and sharper pattern fabrication.

AR-109
AN 8 x 8 MULTIPLIER AND 8-BIT MICROPROCESSOR PERFORM 16 x 16 BIT MULTIPLICATION

A special algorithm implemented in software doubles an 8 x 8-bit multiplier's usual capabilities, permitting efficient 16 x 16 multiplications of signed, unsigned or mixed two's-complement numbers. The article presents this requisite multiplication algorithm as it is implemented on a Z80 μP utilizing the SN74S558.

AR-110
REAL-TIME PROCESSING GAINS GROUND WITH FAST DIGITAL MULTIPLICATION

Refinements in algorithm and hardware have improved the speed and power of single-chip multipliers. These chips can speed the complex operations needed for digital treatment which previously could be carried out off line using large computers. Functions like autocorrelation and fast Fourier transforms necessary for digital filtering and compression, for example, can now be done in real time using these new multipliers. Algorithms and specific applications for these new multiplers are given in this paper.

AR-116
ON-CHIP CIRCUITRY REVEALS SYSTEM'S LOGIC STATES

As computer and data processing systems grow in size and complexity, designers must continue to refine the methods needed to test them. One method, based on serial scan diagnostics, affords a systematic diagnostic technique for pinpointing hardware failures in a digital system. The diagnostic capability is implemented in a system by adding special hardware that enables key test points to be sampled and important control signals to be stimulated. Systems containing the diagnostic hardware are simple to test and are usually more reliable. This diagnostic technique and the two families of devices whch incorporate this diagnostic hardware (Diagnostic PROMs and 8-Bit Register) are the subject of this paper.

AR-117
SINGLE-CHIP CONTROLLERS COVER RAMS

As dynamic RAMs become widely used, demand is growing for automatic sequencing of RAM access signals and refresh controls. NSC's DP8408 and DP8409 are single-chip dynamic RAM controllers available also from Monolithic Memories as the 74S408/9 series.

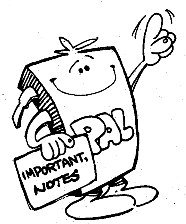
A short description of dynamic RAM operation is provided and both devices are described in several applications.

AR-118
PROGRAMMING CHIPS ON PERSONAL COMPUTERS

Programmable Array Logic chips are fast becoming an economical alternative to custom integrated circuits. Personal computers can assist in the design of programmable arrays, further reducing the cost of developing custom electronic logic. PALASM, the CAD tool for PALs, which was previously available only for mainframes and minicomputers, is now available for many popular personal computers. This article outlines the design process for PALs using PALASM and personal computers.

AR-119
BIPOLAR ARITHMETIC CHIP SPEEDS 68000's MATH THROUGHPUT

Although no 68000-family coprocessor is yet available to help the 16-bit processor perform double-precision and floating-point operations, a general-purpose multiplier/divider can, without significantly boosting the system cost.


PAL
IMPORTANT,
NOTES

Advanced Information Section

Products listed in this section were due for imminent release at the time of printing. Please contact Monolithic Memories for current availability and full parametric specifications.

Table of Contents

ADVANCED INFORMATION

ADVANCE INFORMATION

Features/Benefits

- 8192-bit memory
- Reliable titanium-tungsten fuses (Ti-W) guarantees greater than 98% programming yields
- Low voltage generic programming
- Pin-compatible with standard Schottky PROMs
- PNP inputs for low input current
- Open collector and three-state outputs
- 24-pin SKINNYDIP® package and 28-pin plastic chip carrier for high board density

Description

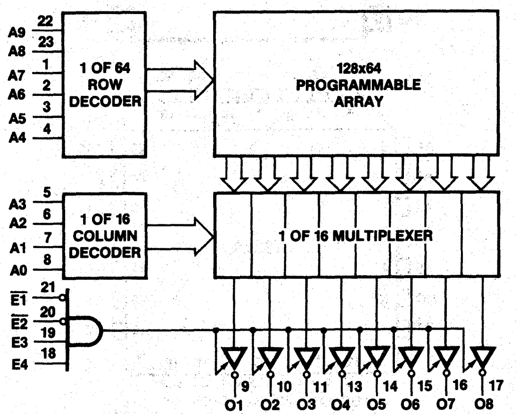
The 53/63S880 and 53/63S881/A are 1Kx8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping with open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

The 53/63S880 and 53/63S881/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic Ti-W PROMs. For details refer to Monolithic Memories' LSI Data Book.

Block Diagram



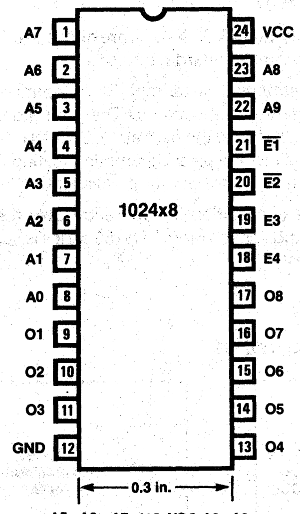
Applications

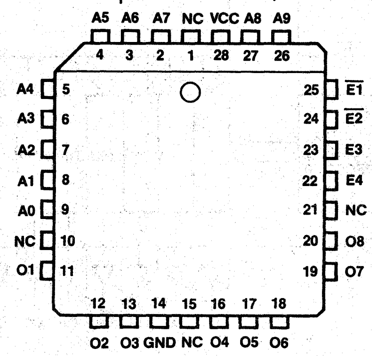
- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with ten inputs, eight outputs and 1024 product terms per output

Preliminary Data

t_{AA} = 35 ns
t_{EA}/t_{ER} = 25 ns
I_{CC} = 175 mA

Pin Configurations





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Monolithic Memories

High Performance 8192x8 PROM

53/63S6481
53/63S6481A
PLE 13P8

ADVANCE INFORMATION

Features/Benefits

- 65536-bit memory
- Greater than 99% programming yields
- Low voltage generic programming
- Pin-compatible with standard Schottky PROMs
- PNP inputs for low input current
- Three-state output enable
- 8-bit wide output
- 24-pin standard DIP package and 28-pin plastic chip carrier for high board density

Typical Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with thirteen inputs, eight outputs and 8192 product terms per output

Preliminary Data

t_{AA} = 45 ns
t_{EA}/t_{ER} = 25 ns
I_{CC} = 190 mA

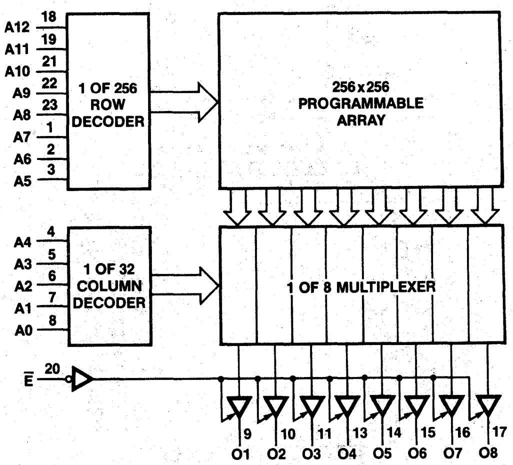
Description

The 53/63S6481 and 53/63S6481A are high-speed 8Kx8 PROMs which use industry standard pinouts.

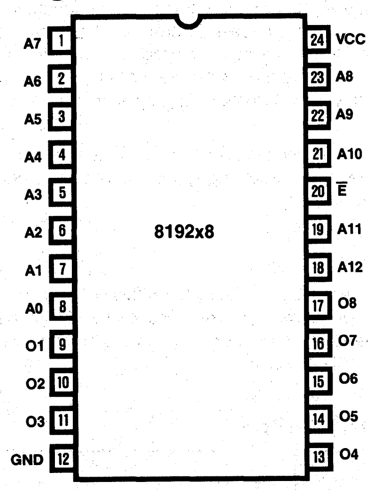
The family features low-current PNP inputs, full Schottky clamping, and three-state outputs. The fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

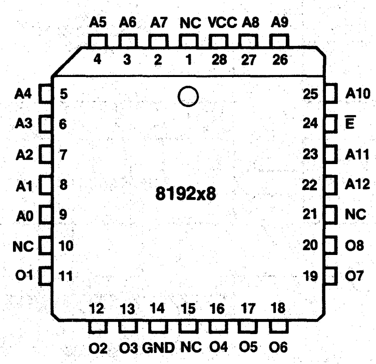
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Block Diagram



Pin Configurations





PLE™ is a trademark of Monolithic Memories.

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Monolithic Memories

ADVANCE INFORMATION

Features/Benefits

- High speed
- Deep FIFOs — 16 addresses for SRAM
- Arbitration read/write
- Control signals for data latching
- Full, half-full, empty and almost-full flags for any buffer size from 512 to 64K
- Expandable
- Three-state outputs

Typical Applications

- LAN equipment
- Data communication
- Disk/tape controllers
- Host to Dedicated Processor interface

Pin Configuration

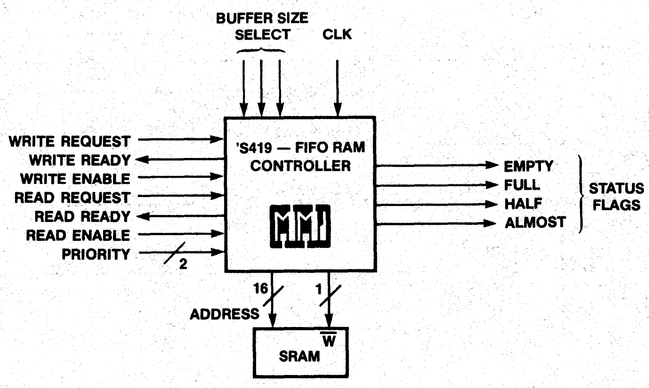
Signal	Pin	Pin	Signal
CLK	1	40	GND
BF0	2	39	$\overline{W}$
BF1	3	38	A0
BF2	4	37	A1
$\overline{MR}$	5	36	A2
WRDY	6	35	A3
RRDY	7	34	A4
WCLK	8	33	A5
RCLK	9	32	A6
VCC	10	31	A7
PW	11	30	GND
PR	12	29	A8
FULL	13	28	A9
EMPTY	14	27	A10
1/2 FULL	15	26	A11
ALMOST	16	25	A12
WREQ	17	24	A13
WEN	18	23	A14
REN	19	22	A15
RREQ	20	21	TEST

Description

The 54/74S419 FIFO Ram Controller provides addressing, control, status and arbitration for a shared SRAM used as a First-In-First-Out buffer. The 16 address lines can address up to 64K deep SRAM. Control signals include the $\overline{W}$ for SRAM, handshake signals for READ/WRITE ports, and strokes for external data latching.

The 'S419 allows single port SRAM to resolve read and write request conflicts according to a simple priority rule. If priority is selected on either read or write port, the operation requested is serviced with no delay. For no priority mode, read and write operations are alternated.

Block Diagram



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ADVANCE INFORMATION

Features/Benefits

- Bipolar S TTL technology allows fast data rate
- Selectable CRC or ECC polynomials
- Standard 16-bit CRC-CCITT polynomial detects errors
- Computer-generated 32-bit ECC polynomial exceeds the performance of Fire code polynomials
- Double-burst error detection and single-burst error correction with ECC polynomial
- Programmable correction span of five, eight, or eleven bits
- Hardware or software correction modes
- Hardware correction provides a user friendly correction cycle which can be implemented without having to learn how to decode the syndrome.
- Separate receiver and transmitter ports
- HOLD pin for idle operation
- Maximum of 1024 bytes of data
- Selective inversion of checkbits and initialization of registers to a high state improves reliability
- 24-pin package

Typical Applications

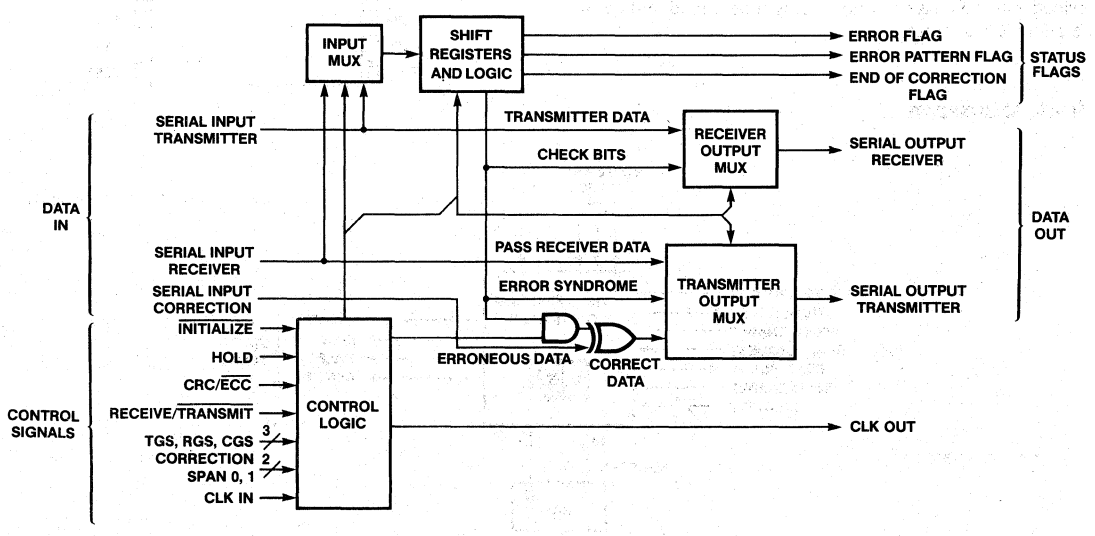
- Disk drives
- Data communication
- High speed serial data transmission

Description

SiBER (Single Burst Error Recovery) is a LSI error-detection-and-correction circuit which may be used to insure data integrity between two serial ports. SiBER implements the standard 16-bit CRC-CCITT polynomial ($x^{16} + x^{12} + x^5 + 1$), and also one of Neal Glover's computer generated polynomials ($x^{32} + x^{28} + x^{26} + x^{19} + x^{17} + x^{10} + x^6 + x^2 + 1$).

The 16-bit CRC-CCITT polynomial can be used only to generate the checkbits, while the 32-bit ECC polynomial can be used to both generate and correct. The 32-bit ECC polynomial can be used to correct 5-, 8-, or 11-bit bursts of erroneous data, or to detect double-burst errors in a data stream of up to 1024 bytes of data.

The SiBER has four modes of operation: transmit, receive, correct and search, which enables correction by software, software/hardware, or hardware. In addition, a HOLD pin is provided for "idle" operation.



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Monolithic Memories

Monolithic MMI Memories

Programmable Array Logic Very High Speed PAL®20B Series

ADVANCE INFORMATION

Features/Benefits

- 15 ns maximum propagation delay
- F_{max} = 40 MHz
- 12 ns maximum from clock input to data output
- Advanced shallow-junction technology
- Instant prototyping and board layout
- Zero NRE charge
- Reduces chip count by greater than four to one
- Programmable replacement for TTL logic
- Programmed on standard PAL programmer
- Programmable three-state outputs
- Security fuse prevents duplication by competitors

Ordering Information

PART NUMBER	PKG	GATE ARRAY DESCRIPTION
PAL16L8B	N,J,L,NL	Octal 16 input And-Or
PAL16R8B	N,J,L,NL	Octal 16 input Registered And-Or
PAL16R6B	N,J,L,NL	Hex 16 input Registered And-Or
PAL16R4B	N,J,L,NL	Quad 16 input Registered And-Or

The PAL transfer function is the familiar sum of products. The PAL is a programmable AND array driving a fixed OR array. In addition, the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D-type flip-flops which are loaded on the low-to-high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets.

The entire PAL family is programmed on conventional PAL programmers with appropriate personality and socket adapter modules. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Description

The PAL20B series, employing Monolithic Memories' advanced shallow-junction technology is an enhanced version of the PAL20A series. With 15 ns maximum propagation delay time, the PAL20B series provides the highest speed performance in the existing PAL family. The advanced shallow-junction technology offers an impressive speed improvement for applications where speed is critical. The PAL20B series contains the PAL16L8B, 16R8B, 16R6B and 16R4B which are pin-compatible with the PAL20 and 20A series.

General Description

The PAL20B series utilizes Monolithic Memories' advanced shallow-junction bipolar process and the bipolar fusible-link technology to provide user-programmable logic for replacement conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his or her own chip" by blowing fusible links to configure AND and OR gates to perform his or her desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from the PC board and are placed on silicon where they can be easily modified during prototype check-out or production.

Typical Application

- DMA control
- State machine control
- High-speed video control
- Standard logic replacement

Preliminary Data

- Propagation delay = 15 ns max
- Clock to output delay = 12 ns max
- Maximum frequency = 40 MHz min
- I_{CC} = 180 mA max

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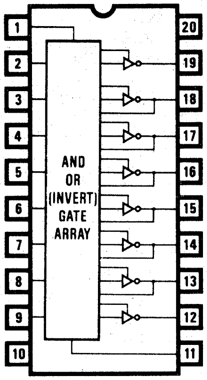
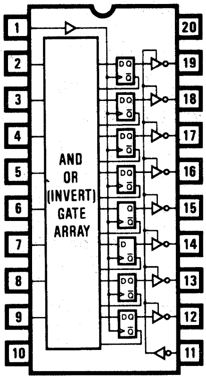
Monolithic MMI Memories

Pin Configuration

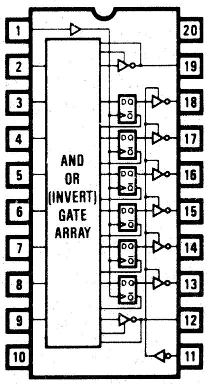
PAL16L8B



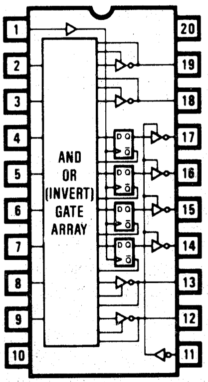
PAL16R8B



PAL16R6B



PAL16R4B



Monolithic MMI Memories

Programmable Array Logic Family PAL® Series 20 AP With Programmable Output Polarity

ADVANCE INFORMATION

Features/Benefits

- **25 ns maximum propagation delay**
- **Programmable output polarity**
- **Programmable replacement for TTL logic**
- **Expedites prototyping and board layout**
- **Programmed on standard PAL programmers**
- **Last fuse prevents duplication**

Functional Description

The PAL series 20 AP represents an enhancement of existing PAL architectures which provides greater design flexibility and higher speed. The PAL series 20 AP comes with programmable output polarity and is pin-for-pin compatible with the standard PAL 20 series.

The programmable output polarity feature allows the user to program individual outputs either active high or active low. This feature eliminates any possible need for inversion of signals outside the device.

General Description

The PAL series utilizes Monolithic Memories' advanced self-aligned washed-emitter high-speed bipolar process and the bipolar fusible-link technology to provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the system engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform the desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from the PC board and are placed on silicon where they can be easily modified during prototype check-out or production.

Product Description

PART NUMBER	PKG	GATE ARRAY DESCRIPTION
PAL10P8A	J, N, L, NL	Octal 10-input And-Or
PAL12P6A	J, N, L, NL	Hex 12-input And-Or
PAL14P4A	J, N, L, NL	Quad 14-input And-Or
PAL16P2A	J, N, L, NL	Dual 16-input And-Or
PAL16C1A	J, N, L, NL	16-input And-Or

The PAL transfer function is the familiar sum of products. The PAL has a single array of fusible links which is a programmable AND array driving a fixed OR array.

Unused inputs are tied directly to VCC or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state.

The entire PAL family is programmed on inexpensive conventional PAL programmers with appropriate personality and socket adapter modules. Once the PAL is programmed and verified two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Preliminary Data

- T_{PD} (max) = 25 ns propagation delay
- I_{CC} (max) = 90 mA

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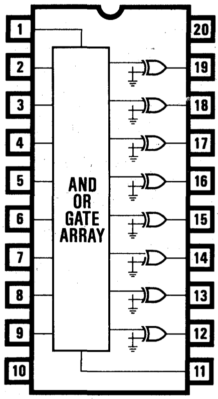
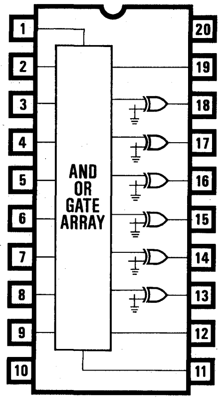
Monolithic Memories MMI

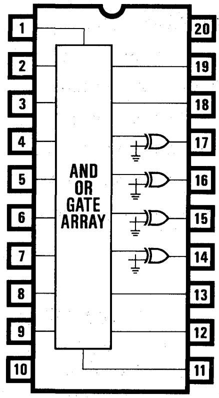
PAL10P8A



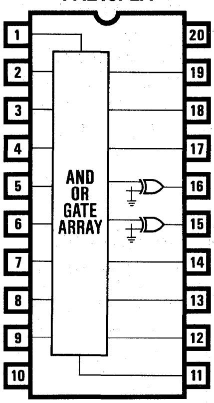
PAL12P6A



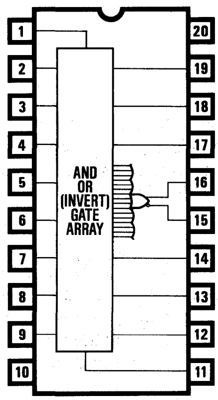
PAL14P4A



PAL16P2A



PAL16C1A



Programmable Array Logic Family PAL® Series 24 AP With Programmable Output Polarity

/ ADVANCE INFORMATION

Features/Benefits

- **25 ns maximum propagation delay**
- **Programmable output polarity**
- **Programmable replacement for TTL logic**
- **Expedites prototyping and board layout**
- **Programmed on standard PAL programmers**
- **Last fuse prevents duplication**

Functional Description

The PAL series 24 AP represents an enhancement of existing PAL architectures which provides greater design flexibility and higher speed. The PAL series 24 AP comes with programmable output polarity and is pin-for-pin compatible with the standard PAL 24 series.

The programmable output polarity feature allows the user to program individual outputs either active high or active low. This feature eliminates any possible need for inversion of signals outside the device.

General Description

The PAL series utilizes Monolithic Memories' advanced self-aligned washed-emitter high-speed bipolar process and the bipolar fusible-link technology to provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the system engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform the desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from the PC board and are placed on silicon where they can be easily modified during prototype check-out or production.

Product Description

PART NUMBER	PKG	GATE ARRAY DESCRIPTION
PAL12P10A	JS, NS, (L), (NL)	Deca 12-input And-Or
PAL14P8A	JS, NS, (L), (NL)	Octal 14-input And-Or
PAL16P6A	JS, NS, (L), (NL)	Hex 16-input And-Or
PAL18P4A	JS, NS, (L), (NL)	Quad 18-input And-Or
PAL20P2A	JS, NS, (L), (NL)	Dual 20-input And-Or
PAL20C1A	JS, NS, (L), (NL)	20-input And-Or

NOTE: L and NL options are 28-pin chip carriers.

The PAL transfer function is the familiar sum of products. The PAL has a single array of fusible links which is a programmable AND array driving a fixed OR array.

Unused inputs are tied directly to VCC or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state.

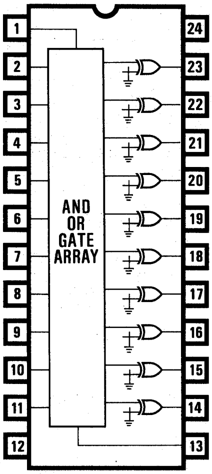
The entire PAL family is programmed on inexpensive conventional PAL programmers with appropriate personality and socket adapter modules. Once the PAL is programmed and verified two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Preliminary Data

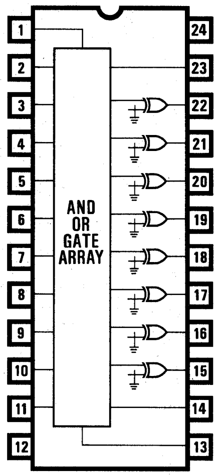
- T_{PD} (max) = 25 ns propagation delay
- I_{CC} (max) = 100 mA

15

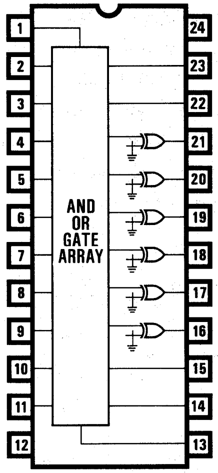
PAL12P10A



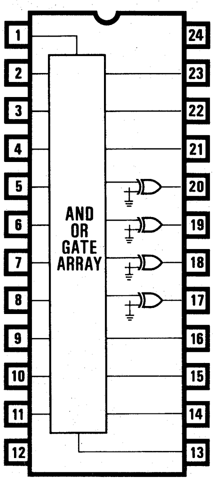
PAL14P8A



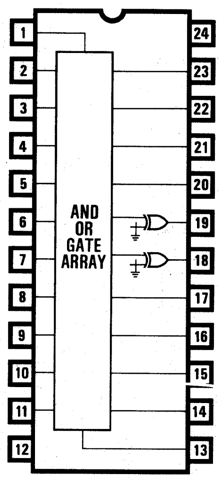
PAL16P6A



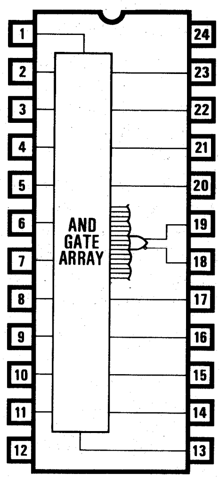
PAL18P4A



PAL20P2A



PAL20C1A



Features/Benefits

- 20 inputs; 12 external, 8 feedback
- 6 ns max. propagation delay
- 32 product terms
- Product term sharing
- Programmable output polarity
- 10KH ECL compatible
- 24-pin SKINNYDIP®
- 50Ω termination drive
- Input pull-down resistors
- Voltage compensated
- Compatible with TTL programmers

Description

This ECL PAL® device has a 20P8 architecture, is ECL 10KH compatible, and has a simple programming algorithm. The 10HPAL20P8 is a 20-input, 8-output PAL part. Outputs have a polarity fuse and can drive a 50 Ω termination to -2.0 V.

Product term sharing allows the choice of one of two outputs for the given product term. Product terms are grouped in multiples of eight per output pair allowing up to eight product terms to be associated with any output term.

Features

The following description explains some of the features of the 10HPAL20P8. Features to be programmed into the PAL device are completely specified by the Boolean equations and automatically configured by the PAL assembler (PALASM)™.

Product Term Sharing

The basic configuration is eight product terms shared between two output cells. For each output a product term can be used by either output, but since the product term sharing is exclusive, a product term can be used by only one output, not both. If the same product term is needed by the same output pair, then two product terms are generated, one for each output.

Programmable Polarity

Output polarity is defined by comparison of the pin list and the equations. If the logic sense of a specific output is different from the logic sense of that output as defined by its equation, the output is inverted. If the logic sense of a specific output is the same as the logic sense of that output as defined by its equation, the output is active high polarity.

Preliminary Data

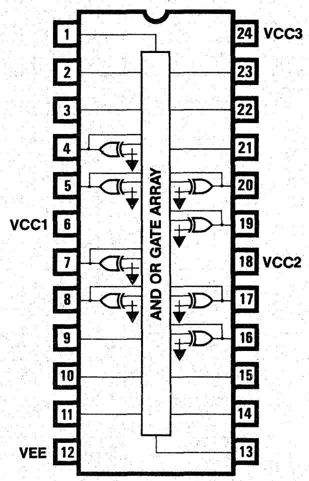
- 6 ns maximum propagation delay
- ~230 mA maximum I_{EE} current

Areas of Application

- High-performance communication equipment
- High-speed test instrumentation
- Mainframes or Super-minis
- Computer-aided graphics

Pin Configuration

10HPAL20P8



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* Patent pending.

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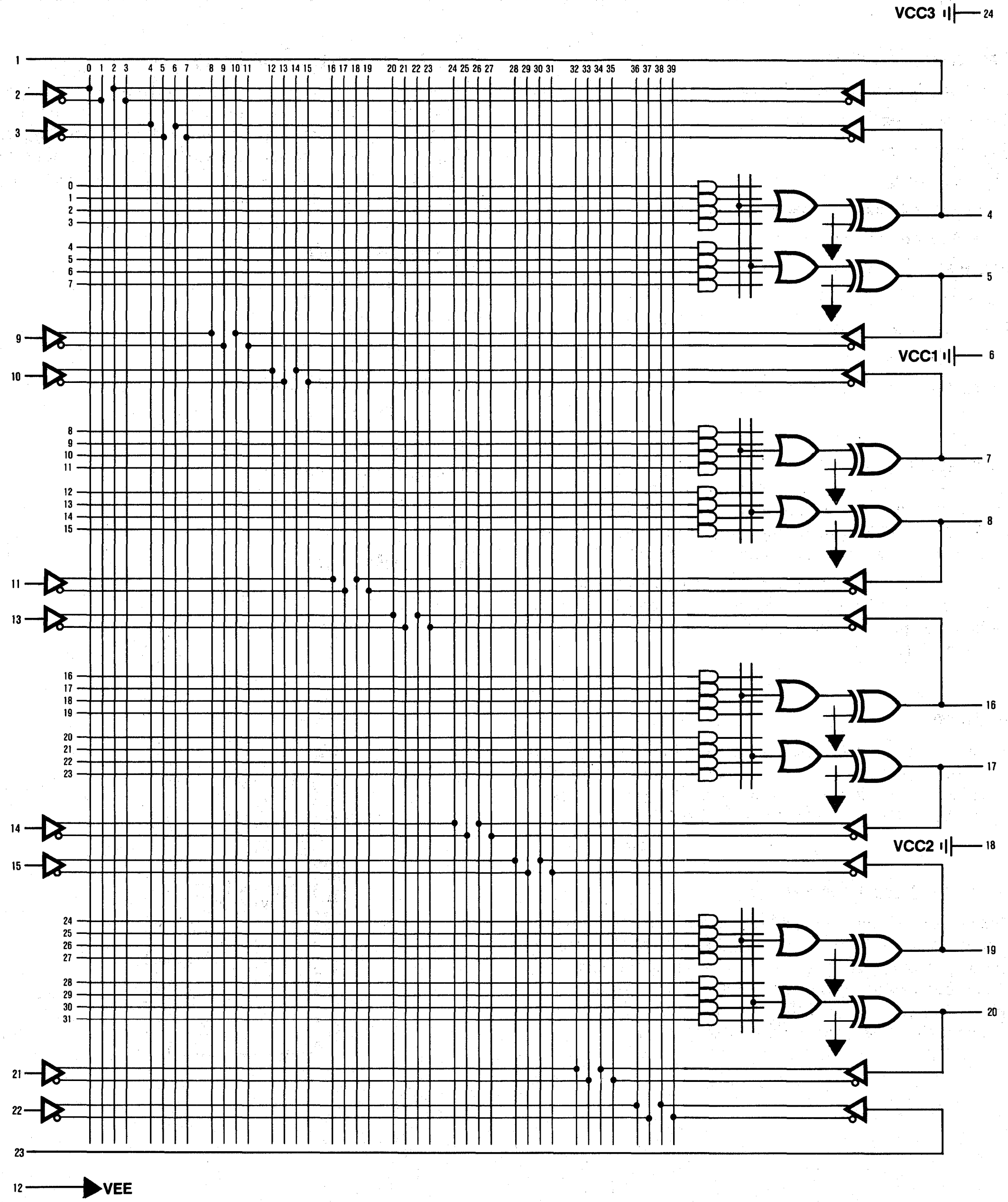
Logic Diagram

10HPAL20P8



ZHAL™ 20 CMOS Hard Array Logic Devices

ADVANCE INFORMATION

Features/Benefits

- Zero standby power
- High speed, CMOS technology
- Low cost alternative for Small and Medium 20 Pin PAL® series
- Fully CMOS/TTL level compatible

Description

The Medium 20 Pin ZHAL represents a new concept in HAL technology which offers the benefits of virtually zero standby power consumption and high speed operation. These benefits are achieved as a result of Monolithic Memories' advanced 3 micron CMOS technology.

The ZHAL architecture is optimized for low cost and ease of implementation in CMOS. It also provides a high degree of flexibility which allows it to address 80-85% of all Medium 20 Pin PAL applications and all the applications of the Small 20 Pin PAL series.

General Description

To design a ZHAL, the user first programs and debugs a PAL using PALASM and the "PAL DESIGN SPECIFICATION" standard format. This specification is submitted to Monolithic Memories where it is computer processed and assigned a bit pattern number, e.g. P01234.

Monolithic Memories will provide a PAL sample for customer qualification. The user then submits a purchase order for a ZHAL of the specified bit pattern number, e.g. ZHAL16L8 P01234.

Areas of Application

- Portable computers
- Battery-operated instrumentation
- Low-power industrial or military equipment
- Standard CMOS/TTL logic replacement

Preliminary Data

I_{CC} (Standby) = 100μA (Max)

I_{CC} @(F_{MAX}) = 90mA

V_{OL} = .4V

V_{OH} = 3.5V (HCT COMPATIBLE)

V_{OH} = 2.4V (TTL)

I_{OL} = 8mA

I_{OH} = −6mA (HCT COMPATIBLE)

I_{OH} = −4mA (TTL)

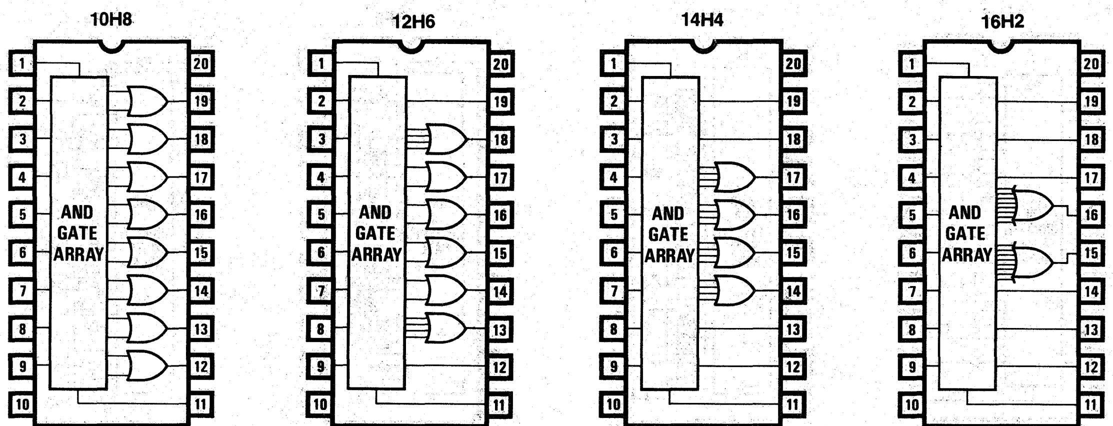
Propagation delay = 35ns max

Setup time = 30ns min

Clock to out time = 25ns max

F_{MAX} = 18MHz

MMI's New Zero Power Hard Array Logic (ZHAL) is Pin for Pin Compatible and May Replace Most Patterns of The Following PALs:



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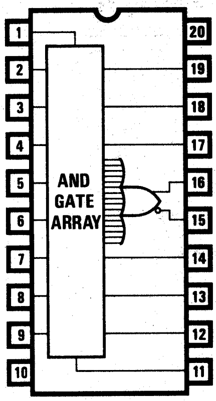
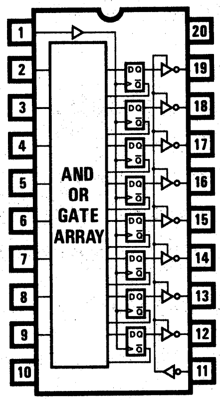
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories MMI

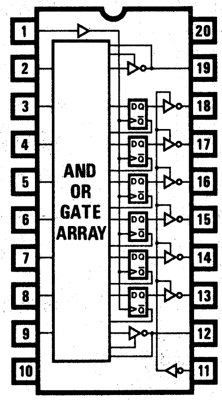
16C1



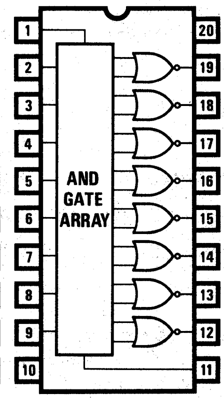
16R8



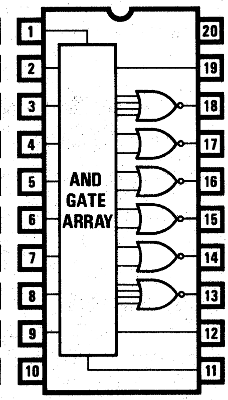
16R6



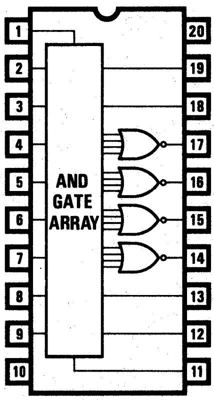
10L8



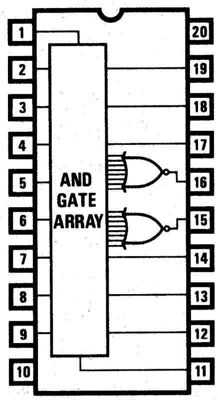
12L6



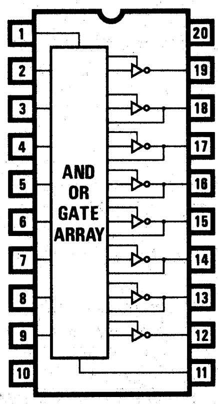
14L4



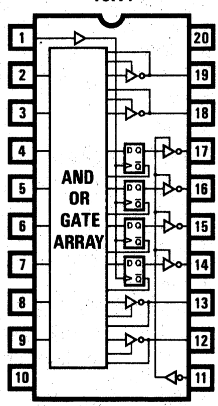
16L2



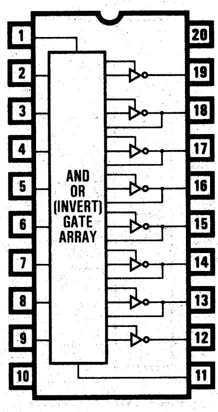
16L8



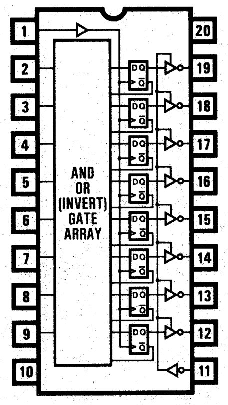
16R4



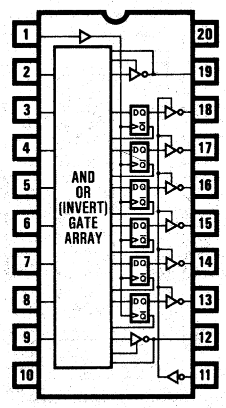
16P8



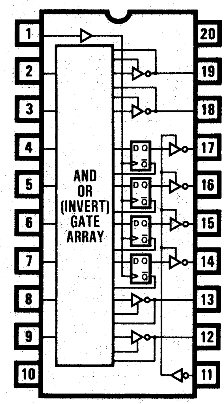
16RP8



16RP6



16RP4



NOTE: Please contact your local MMI field application engineer for assistance in evaluating whether this ZHAL device can be used.

Table of Contents
PACKAGE DRAWINGS

Leads/Finish

Monolithic Memories Incorporated provides high strength nickel iron steel (Alloy 42) leads on all flat pack and side braze packaged devices. In addition, the user is offered a choice of two finishes, standard gold plate and solder dip over gold plate.

***Alloy 42**

Composition (Nominal)	Nickel	42.0%
	Manganese	.50%
	Cobalt	.19%
	Silicon	.07%
	Chromium	.06%
	Aluminum	.024%
	Carbon	.012%
	Phosphorous	.006%
	Sulfur	.001%
	Iron	Balance

***Physical Properties**

Melting Point	1,427°C
Curie Temperature	380°C
Density (g/cc)	8.11
Coefficient of Thermal Expansion cm/cm°C(21 - 343°C)	5.4×10^{-6}
Thermal Conductivity cal-cm/sq cm-sec°C	.03
Electrical Resistivity (micro ohm-cm at 20°C)	71
Modulus of Elasticity (psi)	21.1×10^{6}
Tensile Strength (ksi)	97
Elongation	10%
Vickers Hardness	208

* Stamping Technology Data Sheet
CarTech Data Sheet

Lids

Monolithic Memories Incorporated utilizes high durability KOVAR lids on all Flatpack, chip carriers and sidebrazed packages.

***Composition**

Nickel	29.0%
Cobalt	17.0%
Manganese	.30%
Silicon	.20%
Carbon	.02% Maximum
Iron	balance
Lid Finish — Gold plating	
Melting Point	1,450°C
Curie Temperature	435°C
Density (g/cc)	8.36
Thermal Conductivity (cal-cm/sq cm-sec°C)	.05
Electrical Resistivity (micro ohm-cm at 20°C)	49

*CarTech Data Sheet

Package Body

Monolithic Memories Incorporated utilizes high reliability multilayer ceramics in the body of all side brazed packages. The body ceramic is comprised of a mixture of 90% alumina (AL_2O_3) with other ceramics such as silica (SiO_2), MgO and CaO.

***Physical Properties (nominal)**

Bulk Density	3.6 grams/cc
Water Absorption	~0%
Vickers Hardness	1,300
Flexural Strength	40,000 psi
Young's Modulus	39×10^{6} psi
Coefficient of Linear Expansion	6.5×10^{-6} (40°C–00°C)
Thermal Conductivity	.04 Cal/cm · Sec · °C
Specific Heat	.20 Cal/g°C
Dielectric Strength	10 kv/mm
Volume Resistivity	10^{14} ohm · cm (20°C)
Volume Resistivity	10^{9} ohm · cm (300°C)

* Kyocera International Data Sheet

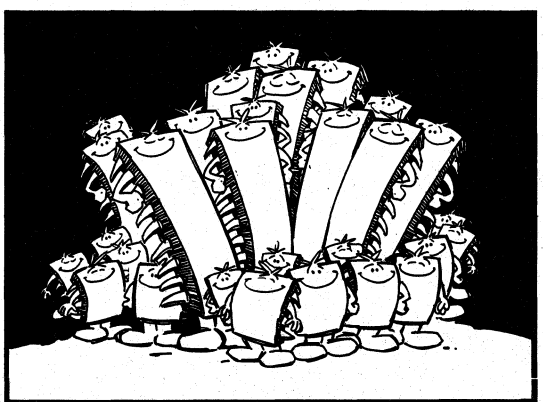
Aluminum Bonding Wire

Monolithic Memories Incorporated uses 1.25 mil aluminum wire to connect I.C. chips to all hermetic packages. The same high reliability wire is used in side brazed packages, flat packs, cerpacks, chip carriers, cerdip packages, and pin grid arrays.

***Physical Properties**

Composition	Aluminum	99%
	Silicon	.85% to 1.15%
	Other	.009% maximum
Tensile Strength	17 to 21 grams	
Elongation	1% to 4%	
Resistance (ohms/inch)	.94 to 1.1	
Weight (mg/foot)	.61 - .68	

* Secon Metals Corp., Data Sheet, 1975



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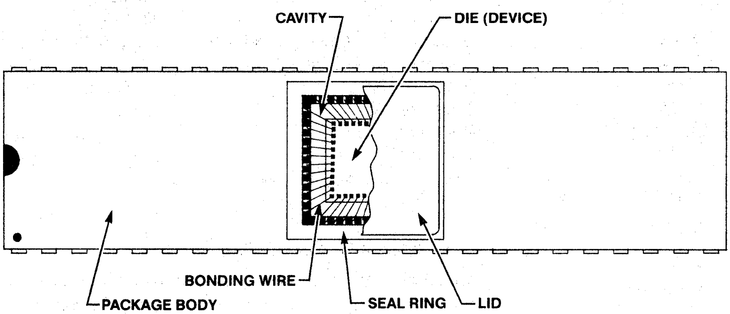
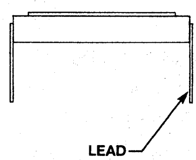
Package Drawing

Side Brazed Package





PACKAGE BODY
Alumina
(Standard Dark)

BONDING WIRE
1.25 Mil Aluminum

LID
Gold Plated Kovar With
Nickel Underplating

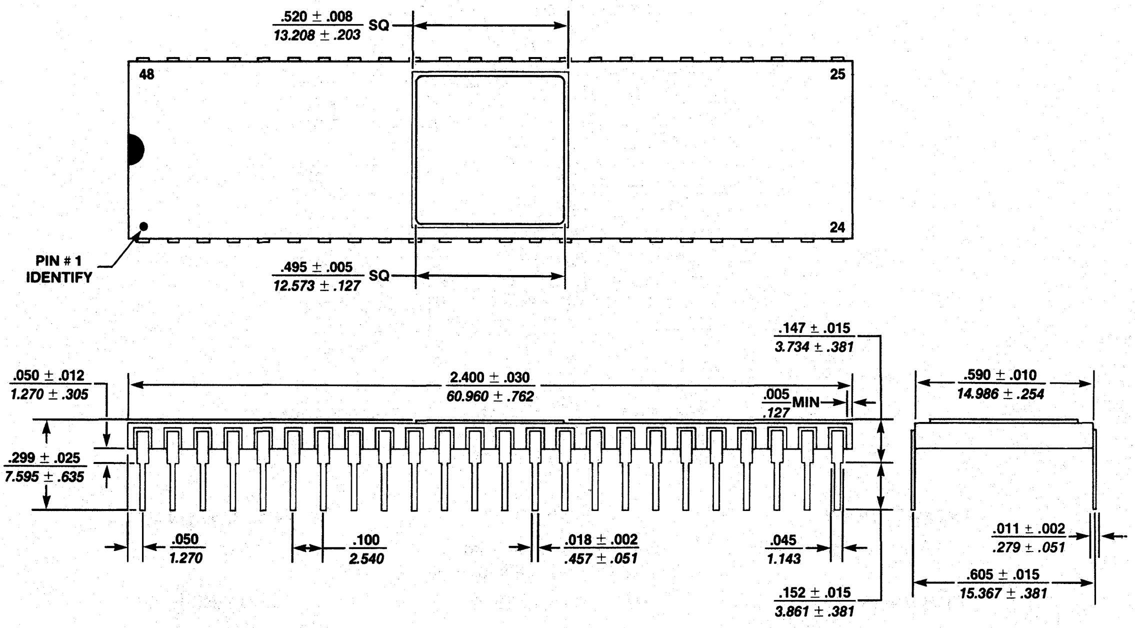
CAVITY/SEAL RING
Gold Over Nickel
Over Tungsten

LEAD MATERIAL
Alloy 42

LEAD FINISHES
Gold Plate (Standard)
Solder Dip Over Gold Plate

Package Drawing

48D Side Brazed Ceramic Dip
(1/2"x2 7/16")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

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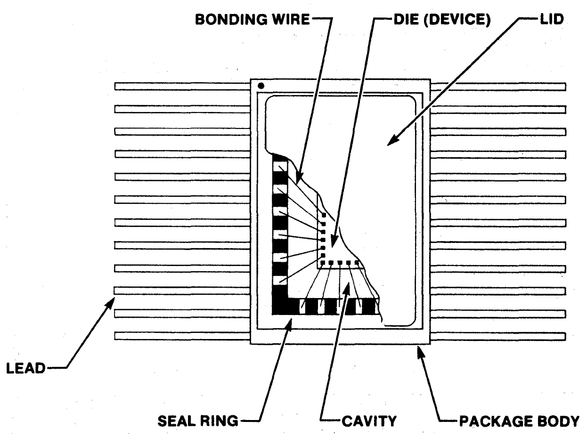
Package Drawing

Flat Pack



PACKAGE BODY
Alumina

BONDING WIRE
1.25 Mil Aluminum

LID
Gold Plated Kovar With Nickel Underplating

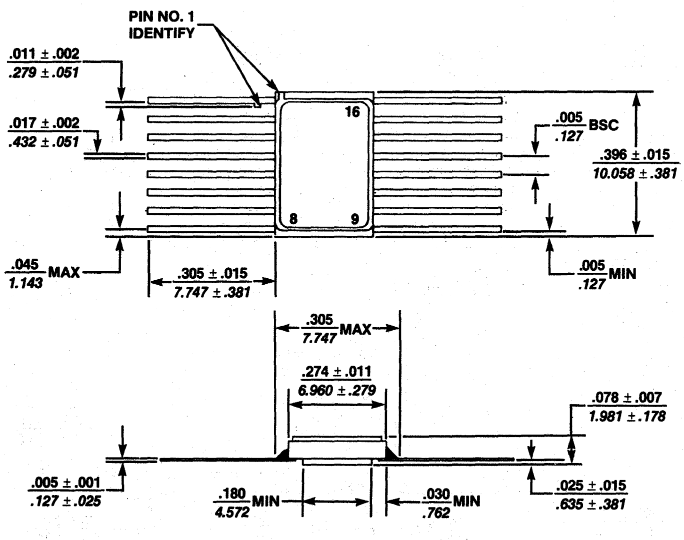
CAVITY/SEAL RING
Gold Over Nickel Over Tungsten

LEAD MATERIAL
Alloy 42

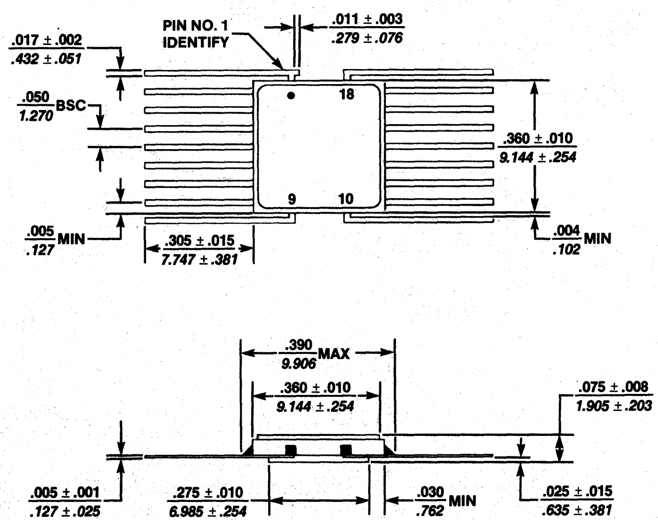
LEAD FINISHES
Gold Plate (Standard)
Solder Dip Over Gold Plate

Package Drawings

16F-4/5 Flat Pack
(1/4"x3/8")



18F-2/3 Flat Pack
(3/8"x3/8")

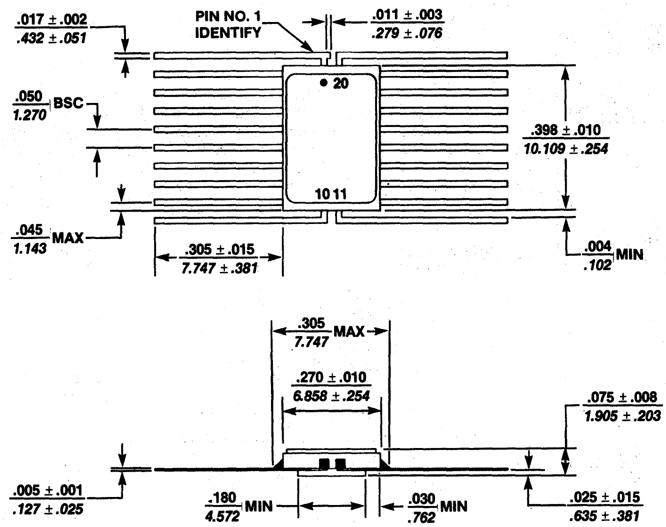


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

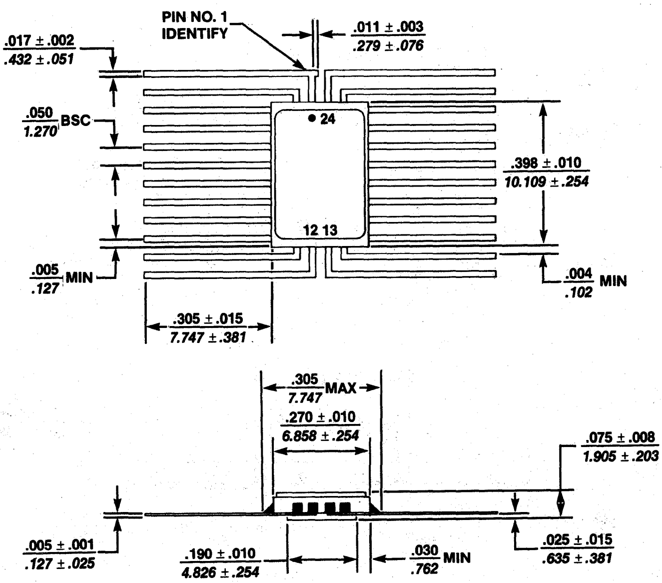
16

Package Drawings

20F-3 Flat Pack
(1/4"x3/8")



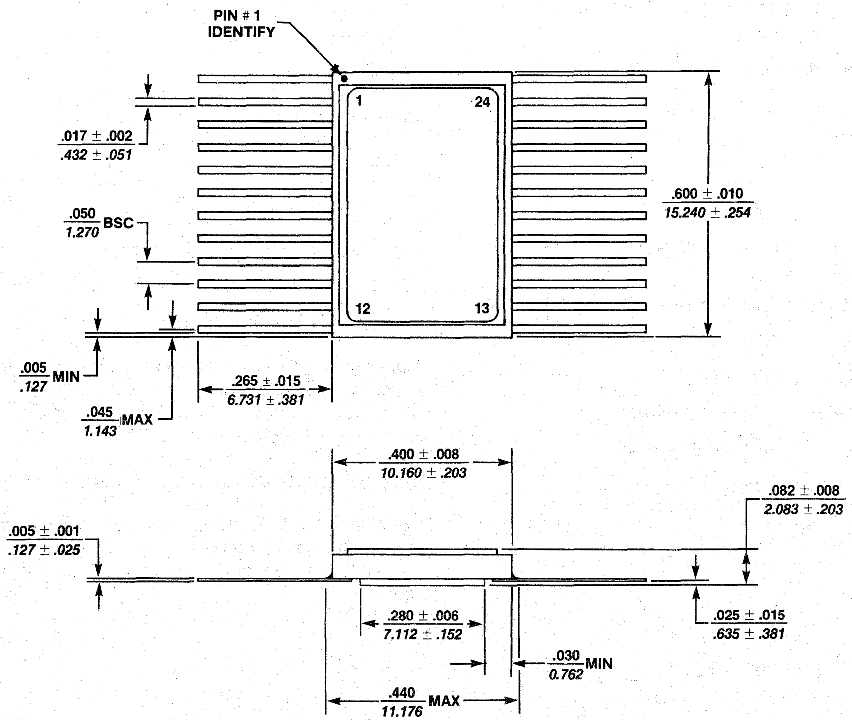
24F-3 Flat Pack
(1/4"x3/8")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawing

24F-4/6 Flat Pack
(3/8"x5/8")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

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Cerdip Package

Caps and Bases

Caps and bases consist of two sections, pressed alumina body and LS-0113 glass seal ring.

***Properties of pressed Alumina (Nominal)**

Alumina Content	91%
Water Absorption	~0%
Specific Gravity	3.80
Moh's Hardness	9.0
Coefficient of Linear Expansion	7.1×10^{-6} °C(40°C – 500°C)
Thermal Conductivity	.05 cal/cm·sec· °C
Flexural Strength	38,497 psi
Dielectric Strength	10 kv/mm
Volume Resistivity	10^{12} $\Omega \cdot$ cm (25°C)
Volume Resistivity	10^{8} $\Omega \cdot$ cm (300°C)

***Physical Properties of LS-0113 Seal Glass**

Coefficient of Thermal Expansion (30 - 250°C)	6.4×10^{-6}/°C
Specific Gravity	6.85
Transition Point	320°C
Softening Point	400° C
Seal Temperature	450° C
Dielectric Loss Tangent (1MHz·25° C)	33.0
Dielectric Constant	85.0
Volume Resistivity 250° C · Ω cm)	2.5×10^{9}
Thermal Conductivity @ 25° C, Kcal/m, hr° C)	.78
$\propto$ Particle Emission CPH/cm^2	22

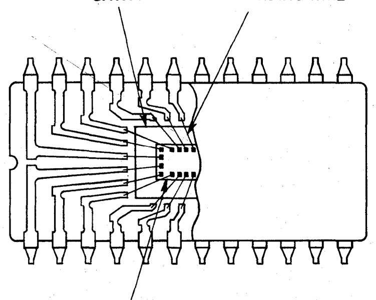
* Narumi Technical Ceramics Datasheet

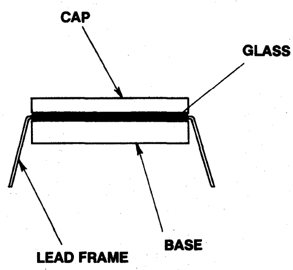
Cavity/Die Attach

Monolithic Memories Incorporated utilizes high strength eutectic die attach in CerDip packages. CerDip bases have a gold lined cavity and attachment of die occurs through the formation of a silicon/gold eutectic at elevated temperatures.

Leadframe Material/Lead Finish

Monolithic Memories Incorporated uses Alloy 42 as a leadframe material for Cerdip packages. Standard lead finish is tin plate (300 - 600 μ). Solder dip is used to conform to 38510 lead finish spec.

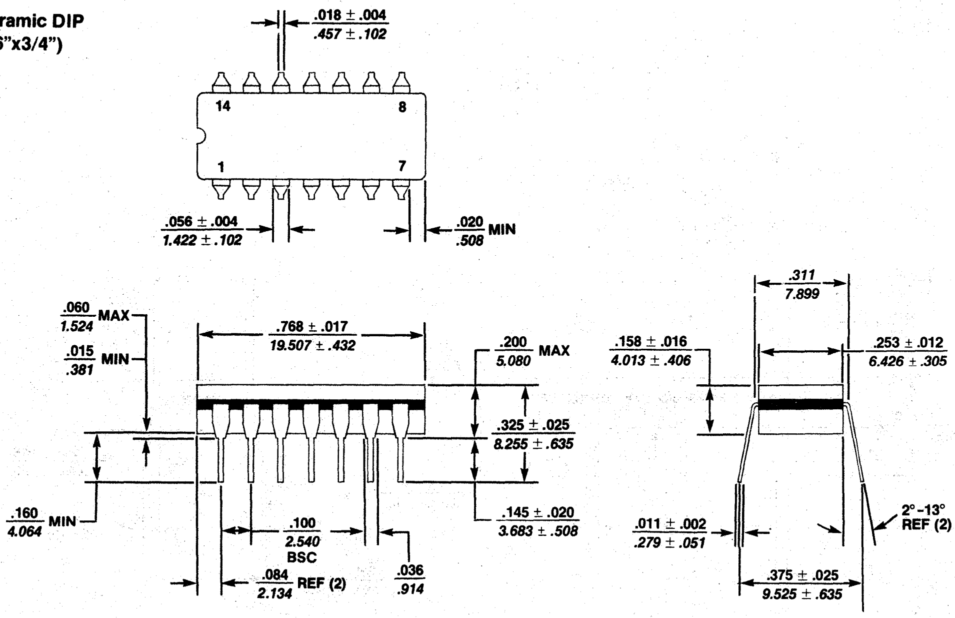




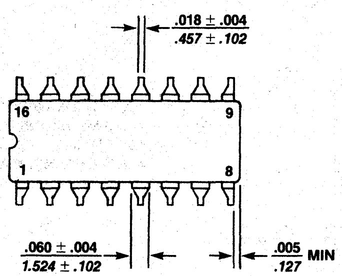
LEAD FRAME	BONDING WIRE	CAP AND BASE
Alloy 42	1.25 Mil Aluminum	Pressed Alumina
GLASS	**CAVITY**	**LEAD FINISHES**
LS-0113	Gold Over Alumina For Eutectic Die Attach	Tin Plate Solder Dip

Package Drawings

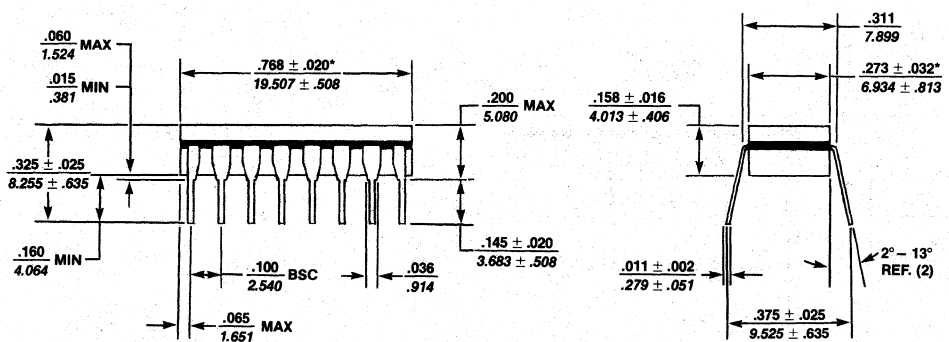
14J Ceramic DIP
(5/16"x3/4")



16J Ceramic DIP
(5/16"x3/4")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES



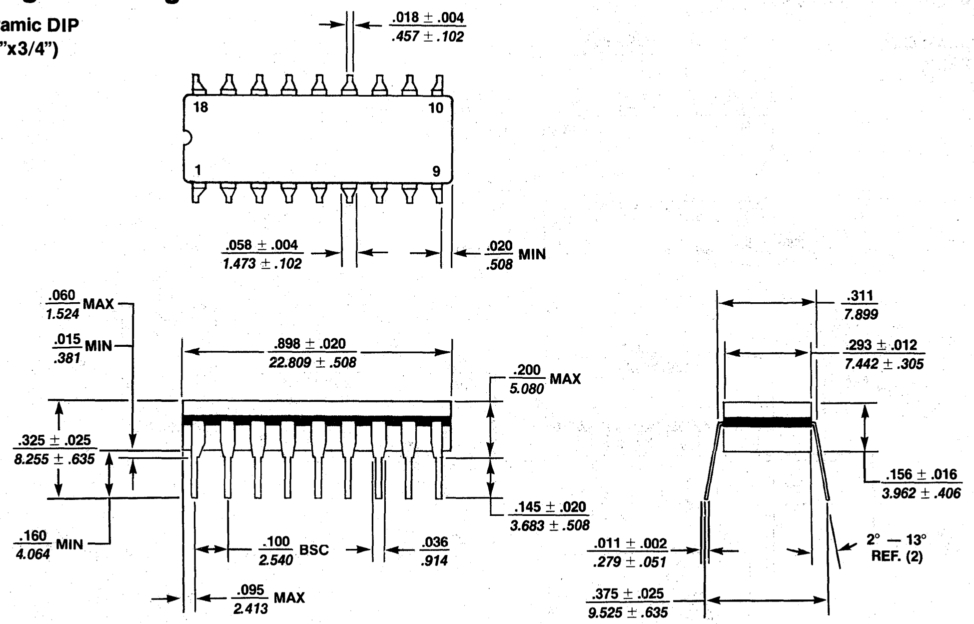
Notes:

1. Specified body dimensions allow for differences between SSI, MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

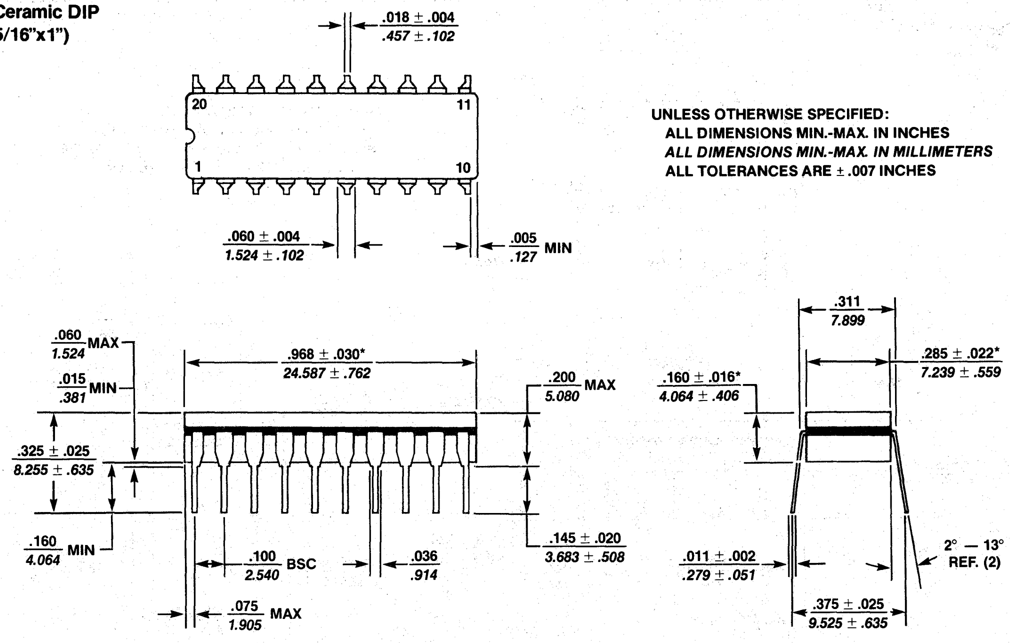
16

Package Drawings

18J Ceramic DIP
(5/16"x3/4")



20J Ceramic DIP
(5/16"x1")



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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
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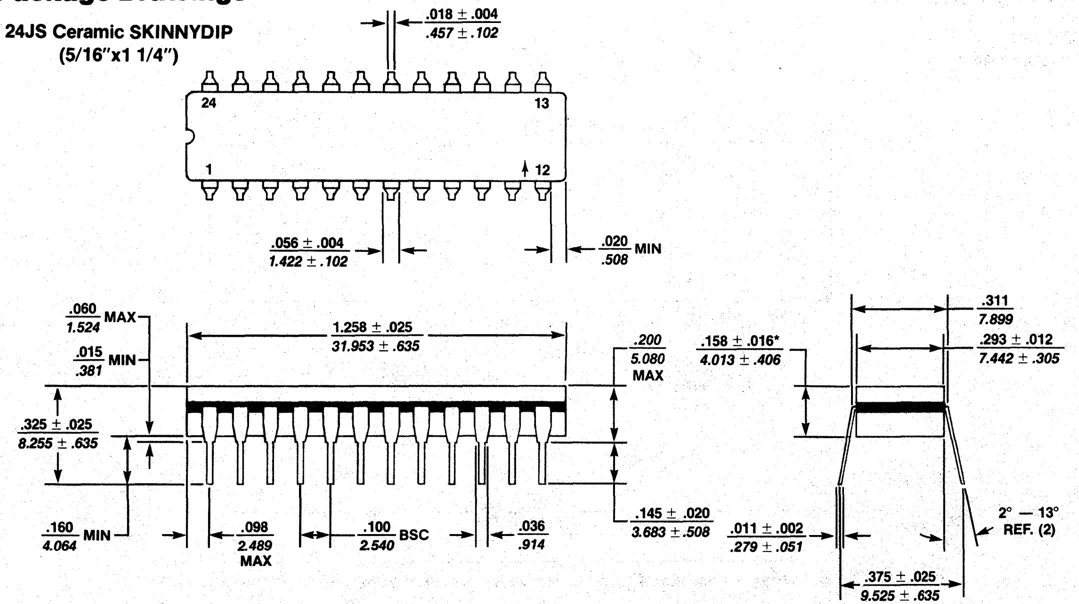
Notes:

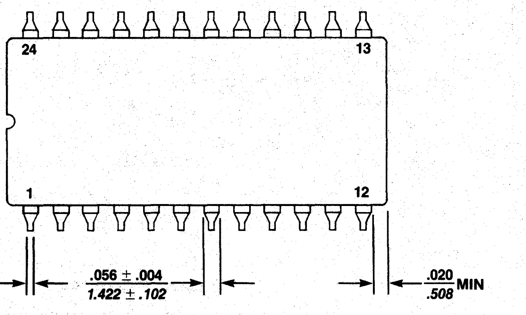
1. Specified body dimensions allow for differences between SSI, MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

Package Drawings

24JS Ceramic SKINNYDIP
(5/16"x1 1/4")



24J Ceramic DIP
(1/2"x1 1/4")



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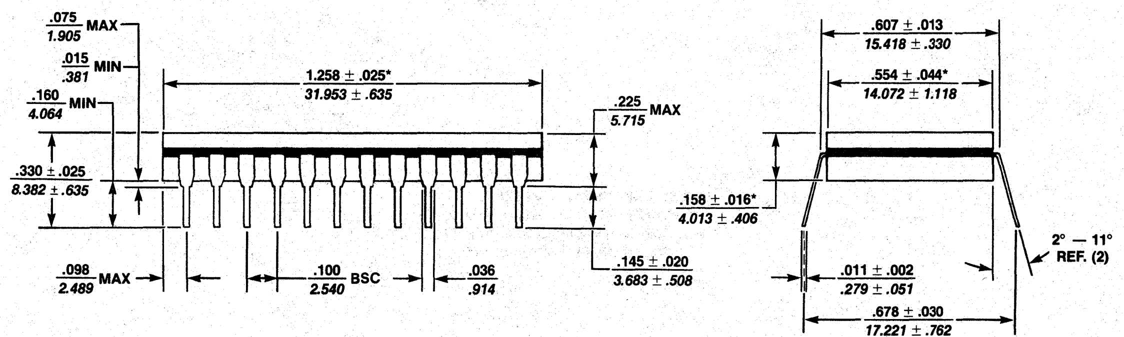
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES



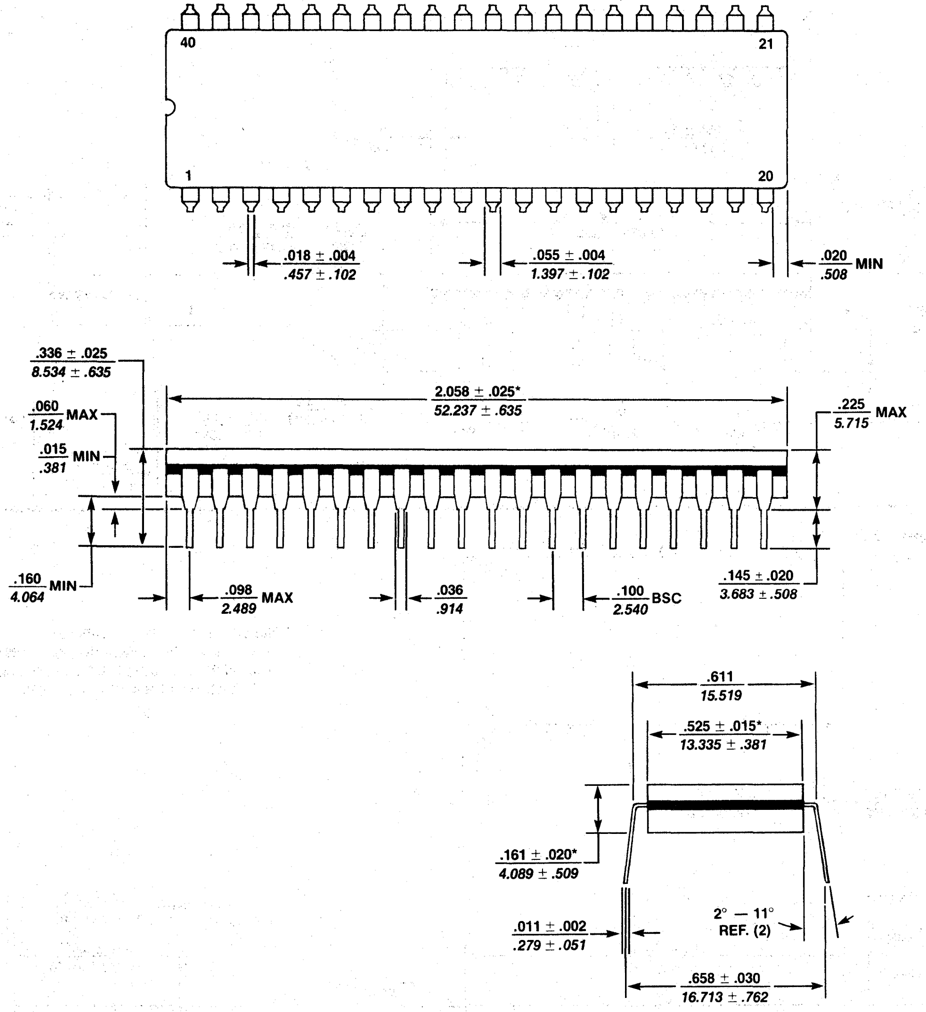
Notes:

1. Specified body dimensions allow for differences between MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

16

Package Drawings

40J Ceramic DIP
(9/16"x2 1/16")



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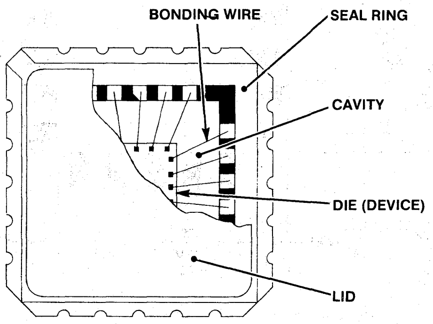
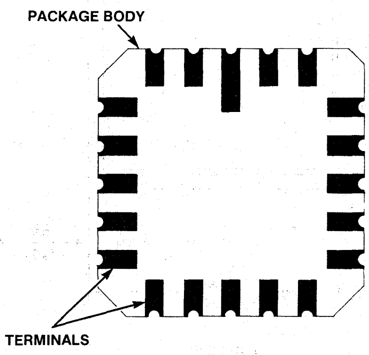
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

1. Specified body dimensions allow for differences between MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

Leadless Chip Carrier





PACKAGE BODY

Alumina
(Standard Dark)

BONDING WIRE

1.25 Mil Aluminum

LID

Gold Plated Kovar With
Nickel Underplating

CAVITY/SEAL RING

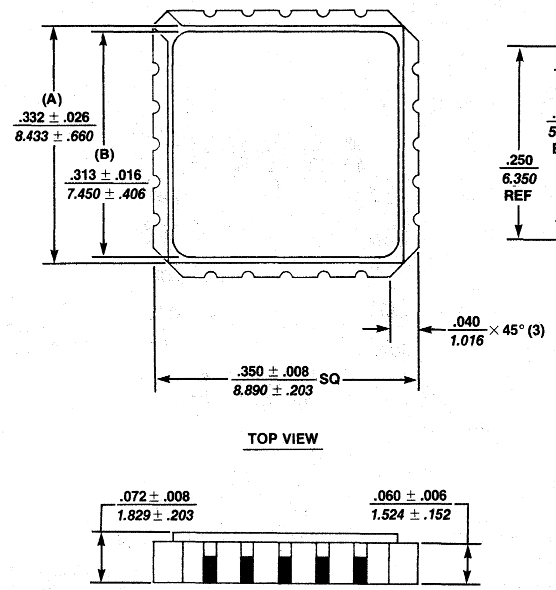
Gold Over Nickel
Over Tungsten

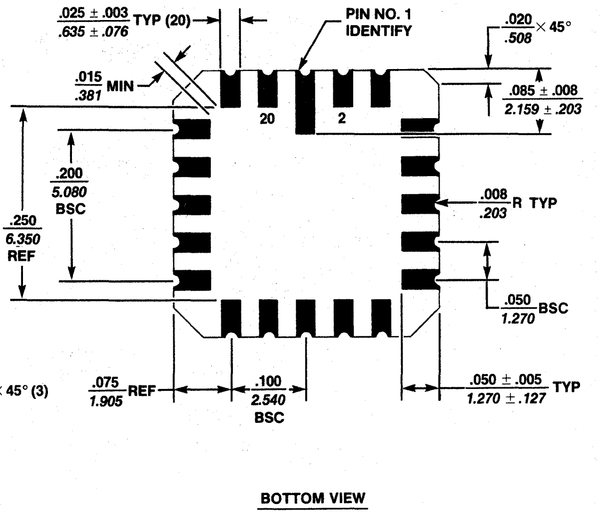
TERMINALS

Gold Plating Over Tungsten

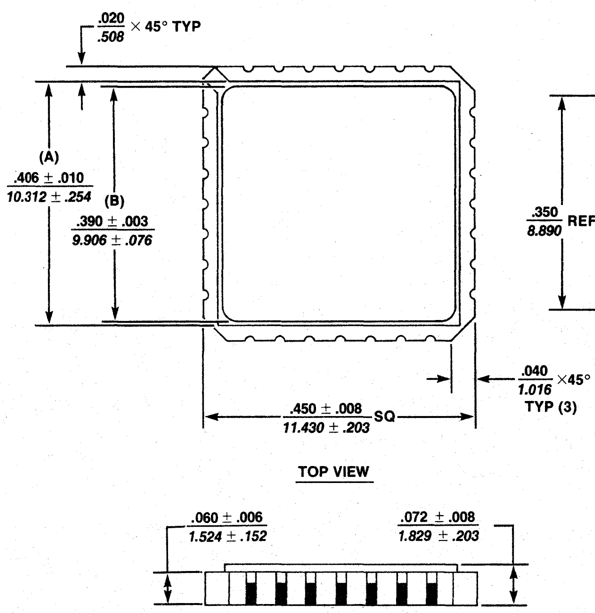
Package Drawings

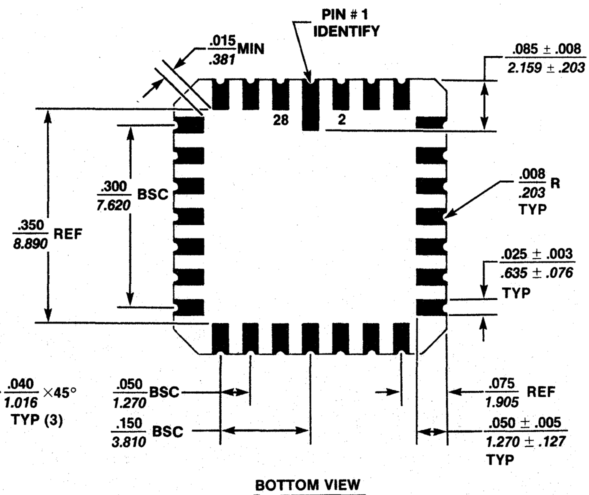
20L Leadless Chip Carrier
(.350"x.350")





28L Leadless Chip Carrier
(.450"x.450")





UNLESS OTHERWISE SPECIFIED:
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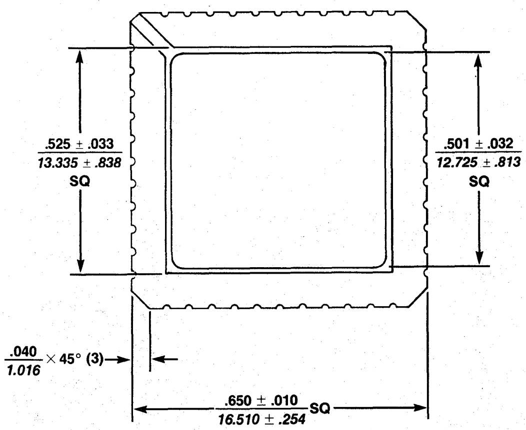
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

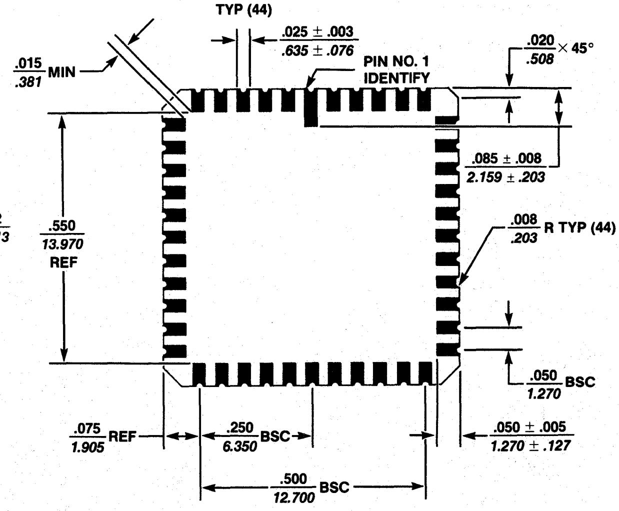
1. Solder fillets on lid edges not shown.

Package Drawings

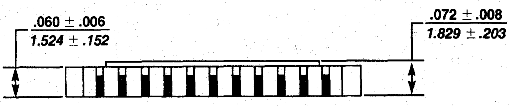
44L Leadless Chip Carrier
(.650"x.650")



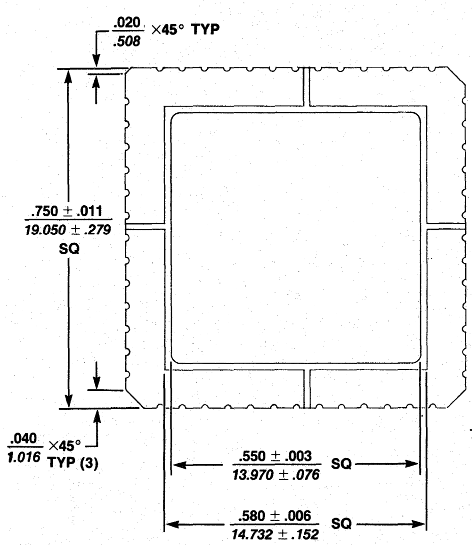
TOP VIEW



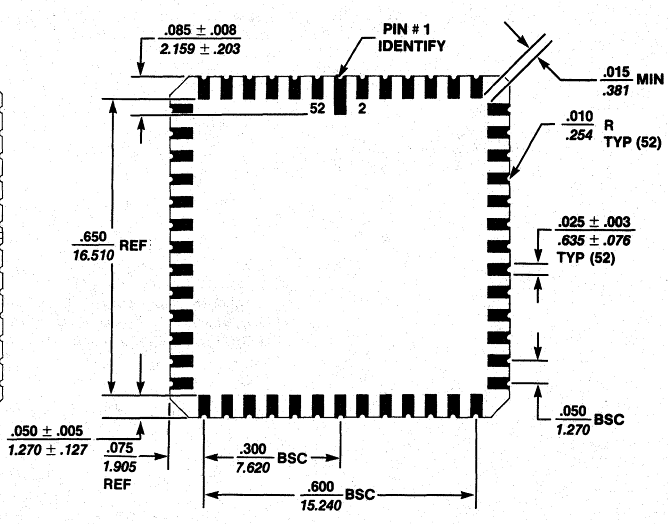
BOTTOM VIEW



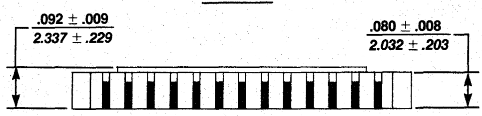
52L Leadless Chip Carrier
(.750"x.750")



TOP VIEW



BOTTOM VIEW



UNLESS OTHERWISE SPECIFIED:
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

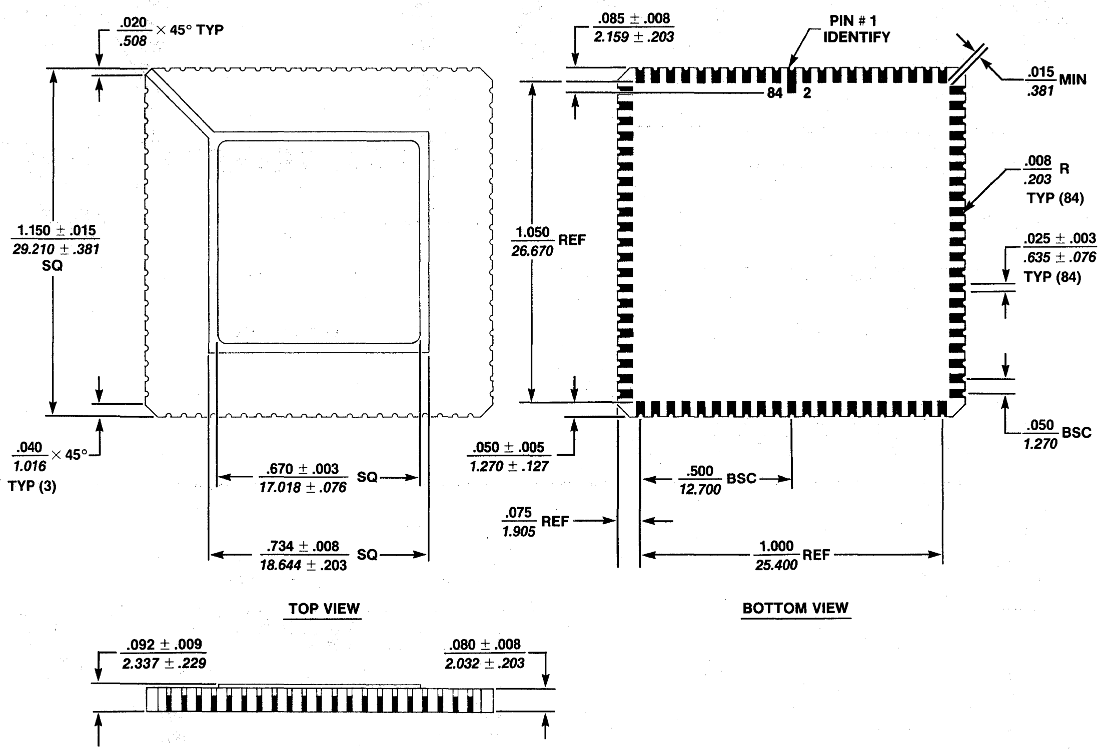
Notes:

1. Solder fillets on lid edges not shown.

16

Package Drawings

84L-1 Leadless Chip Carrier (Cavity Up)
(1.150"x1.150")



UNLESS OTHERWISE SPECIFIED:
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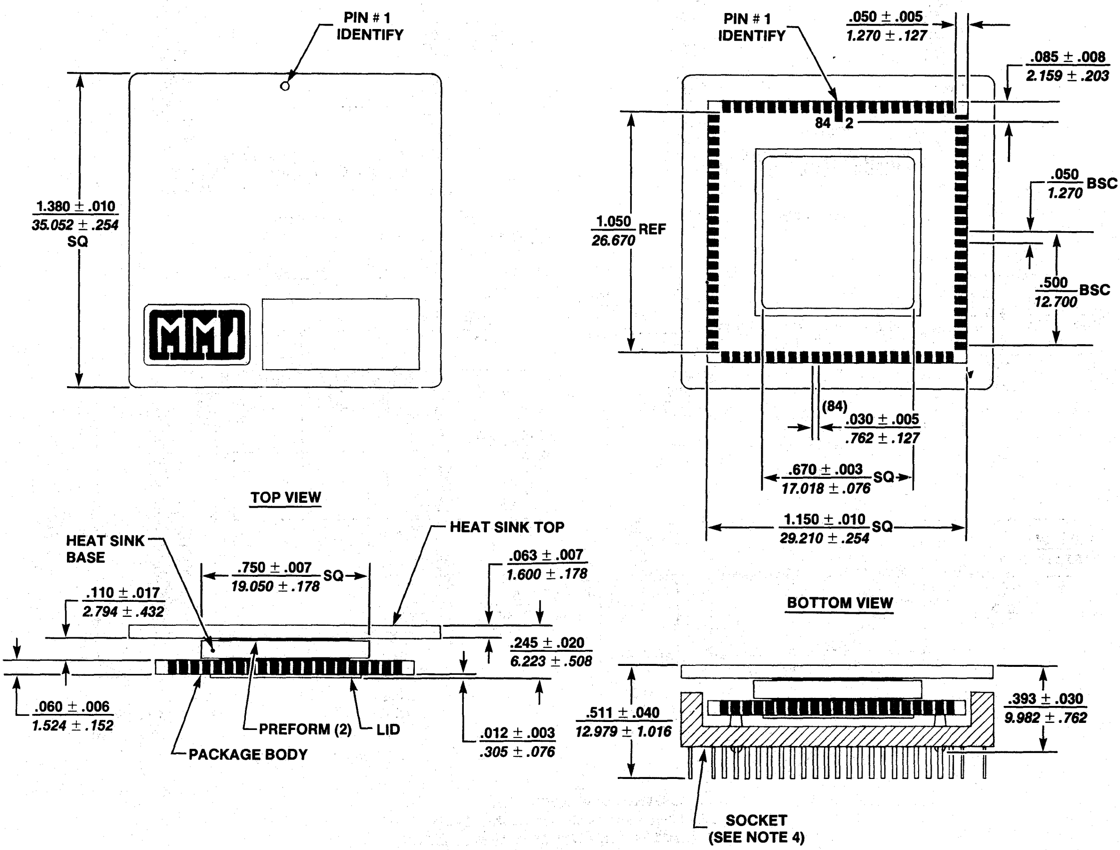
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

Notes:

1. Solder fillets on lid edges not shown.

Package Drawings

84L-2 Leadless Chip Carrier (Cavity Down)
(1.380"x1.380")



UNLESS OTHERWISE SPECIFIED:
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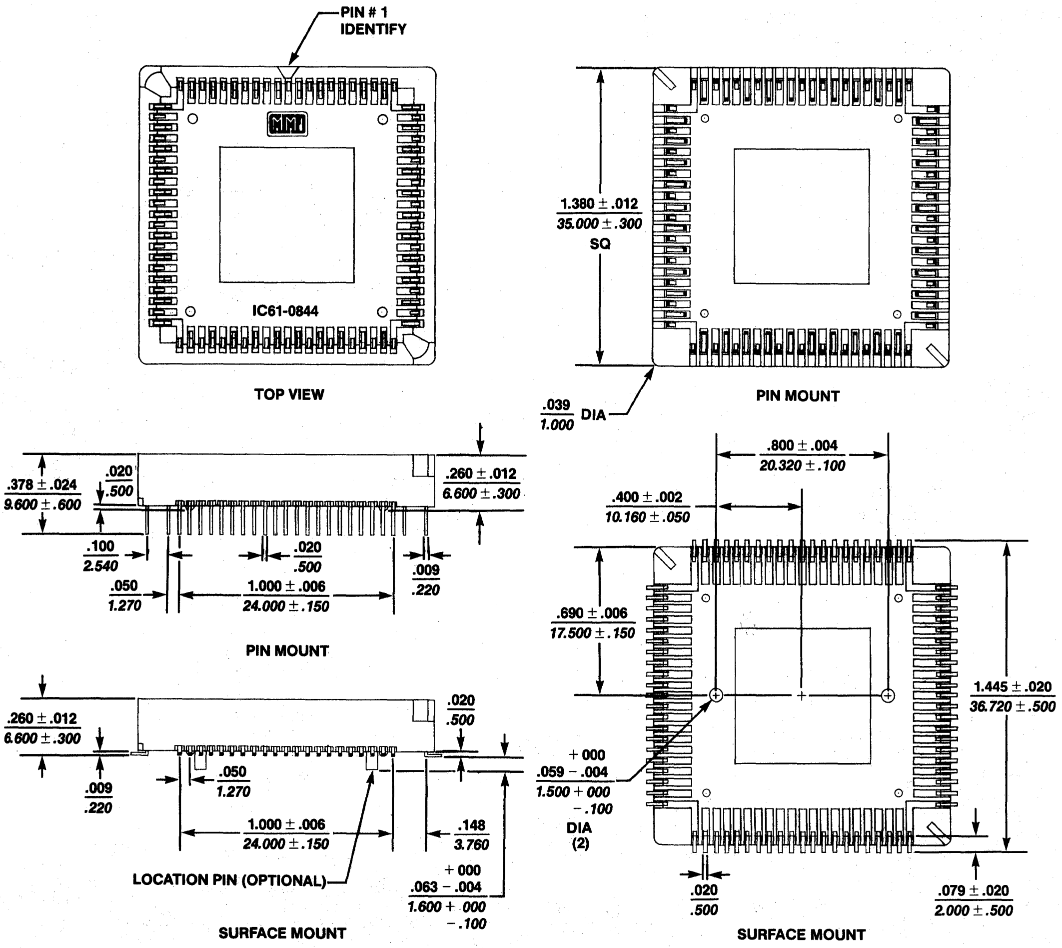
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

1. Solder fillets on lid edges not shown.

16

84L-2 Socket



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ALL TOLERANCES ARE ±.007 INCHES

Socket Specifications (all values from Yamaichi/Nepenthe data sheet):

1. Insulation Resistance .... 1,000 MΩ minimum at 500 V DC
2. Dielectric Withstanding Voltage .... 700 V AC RMS for one (1) minute
3. Contact Resistance .... 20 MΩ maximum at 10 mA, 20 mV
4. Rated Current Per Contact .... 1 A maximum
5. Operating Temperature .... −55 to +100°C
6. Contact Force .... 85 grams min for each contact

Molded Packages

Leadframe

Monolithic Memories Incorporated utilizes the latest high-strength, high-conductivity copper leadframes for assembling devices in molded plastic packages. Depending on availability, all copper leadframes will be stamped from either ALLOY 195 or TAMAC 5.

Listed below are the physical parameters of these two equivalent alloys:

Nominal Composition	(1) Alloy 195	(2) Tamac 5
Copper	97.0%	98.0%
Iron	1.5%	.75%
Tin	.6%	1.25%
Phosphorous	.1%	.03%
Cobalt	.8%	
Zinc	.2% max.	
Aluminum	.02% max.	
Lead	.02% max.	
Melting Point	1,090°C	1,075°C
Density (G/cc)	8.92	8.8
Coefficient of Thermal Expansion (20–300°C) cm/cm/°C	1.69×10^{-5}	1.67×10^{-5}
Thermal Conductivity at 20°C cal - cm/sq cm - sec - °C	.47	.33
Electrical Resistivity (microhm - cm @ 20°C)	3.94	4.93
Modulus of Elasticity (psi)	1.73×10^{7}	1.71×10^{7}
Tensile Strength (ksi)	75/85	69/79
Elongation	2 - 5%	4 - 7%
Vickers Hardness	157 - 175	150 -

Mechanical Criteria

All leadframes are sufficiently strong so that leads in the finished package will survive two 90° bends (bend is complete cycle 0° to 90° to 0°) without fracturing.

(1) OLIN Brass data sheet, 1971
(2) TAMAGAWA data sheet, 1980

Gold Bonding Wire

Monolithic Memories chips are connected to package leads using 1.0 mil, 1.25 mil, or 1.30 gold wire, depending on assembly and device requirements. In some cases, the impurities of the gold wire will vary to accommodate particular devices. Listed below are typical parameters.

Composition

Gold	99.9990		
Silver	.0001	-	.001
Calcium	.0001	-	.001
Copper	.00001	-	.0002
Iron	.0001	-	.001
Beryllium	.0001	-	.001
Magnesium	.0001	-	.001
Others	.001	-	.001

Diameter	Elongation	Tensile Strength (g)	*Resistance ohms per in.	Weight mg per ft
.00100	3 - 6%	8 - 12	1.13 - 1.20	2.83 - 3.20
.00125	3 - 6%	10 - 14	.72 - .77	4.42 - 5.00
.00130	3 - 6%	14 - 18	.67 - .71	4.78 - 5.41

* Secon Metal data sheet

Package Body

Monolithic Memories utilizes a low-chlorine thermosetting epoxy resin for all molded assembly. This moisture-resistant thermally-conductive plastic provides high-reliability protection in a commercial environment.

[1]Thermoset Plastic

Thermal Expansion	2.5×10^{-5}°C max.
Thermal Conductivity	1.6×10^{-3} cal/sec cm °C min.
Glass Transition Temperature	150°C min.
Heat Deflection Temperature	200°C min.
Water Absorption After Boiling for 24 hrs.	.5% max.
Specific Gravity	1.80 - 1.86
Volume Resistivity (Room Temperature)	$10^{15}\ \Omega$ - cm
Volume Resistivity (150°C)	$10^{13}\ \Omega$ - cm
Dielectric Constant (1MHz)	4.5 max.
Flexural Strength	19,000 psi
Impact Strength	2.5 kgf • cm/mm^2
Fre Na^+	5 ppm max.
Free Cl^-	5 ppm max.
Hydrolyzable Chlorine	300 ppm max.

[1]Sumitomo Bakelite Company data sheet

Lead Finish

Monolithic Memories molded devices come standard with 300 - 600 microinches of tin plating on all exposed leads. This finish provides the user with a solderable surface for PC board attachment.

In addition to tin plating, Monolithic Memories offers a solder dip finish. This finish puts a coating of solder on all exposed metal and results in excellent solderability of the finished package.

Die Attach Pad/Bonding

Monolithic Memories utilizes high-strength conductive epoxy to attach die to P-Dip leadframes. The leadframe is plated with 150 microinches of silver in the die attach area to enhance the strength and reliability of the bond.

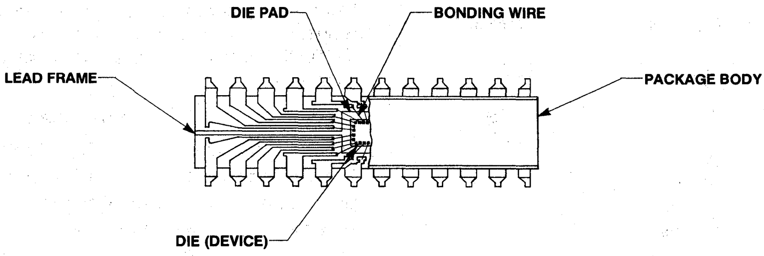
***Epoxy Characteristics (typical)**

Specific Gravity	2.31
Shore "D" Hardness (ASTM-D-1706)	84
Coefficient of Thermal Expansion (cm/cm° C)	2.5×10^{-5}
Tensile Strength (ASTM-D-1002)	
Measured at 25° C	2,100 psi
Measured at 85° C	1,500 psi
Volume Resistivity (ohm - cm, 25° C - 155° C)	.001
Resistivity After 200 hrs. Aging at 180°C	.0001

* Amicon Corporation data sheet

16

Molded DIP



LEAD FRAME

Copper Alloy 195.
Copper Alloy Tamac 5.

BONDING WIRE

1.25 Mil Gold Wire.

PACKAGE BODY

Thermoset Plastic.

LEAD FINISH

Tin Plating.
Solder Dip.

DIE PAD

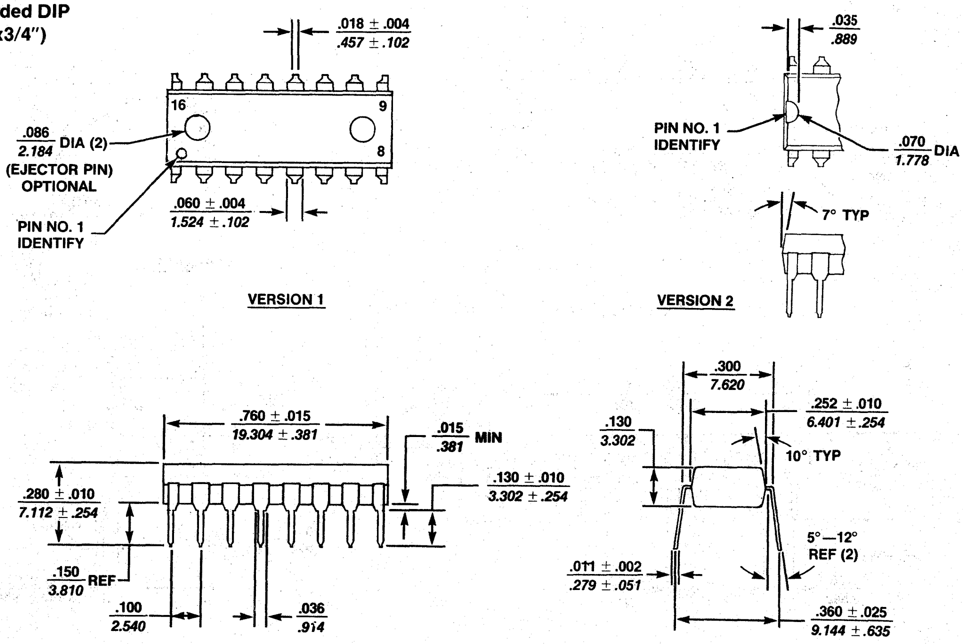
Spot Silver Plating
(150 Microinches).

DIE BOND

Silver Filled Epoxy.

Package Drawings

16N Molded DIP
(1/4"x3/4")



18N Molded DIP
(1/4"x7/8")

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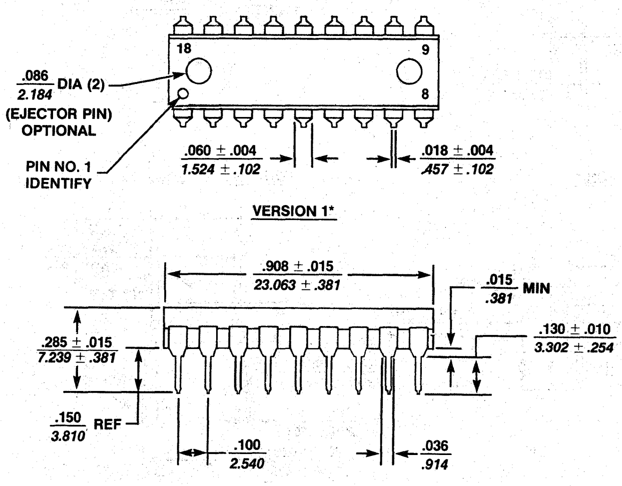
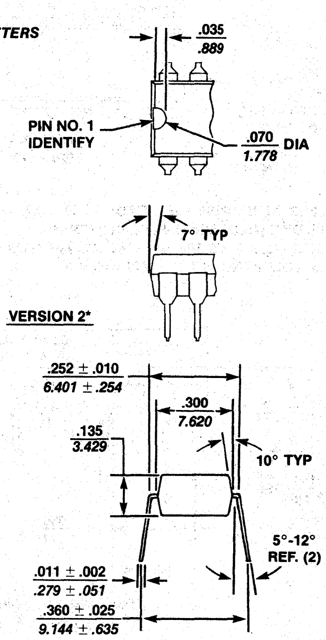




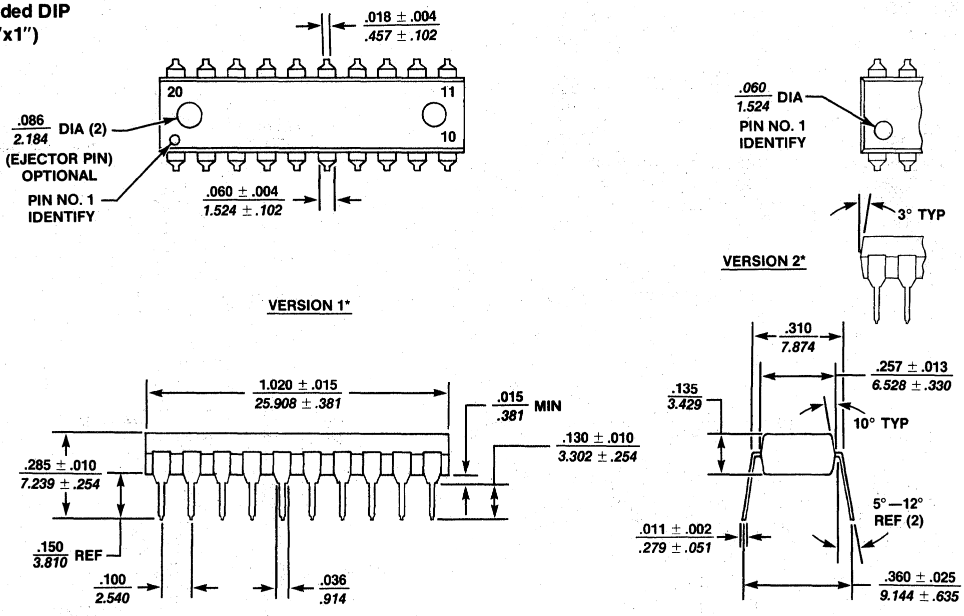
Notes:

1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both version 1 and version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on version 1 are optional.

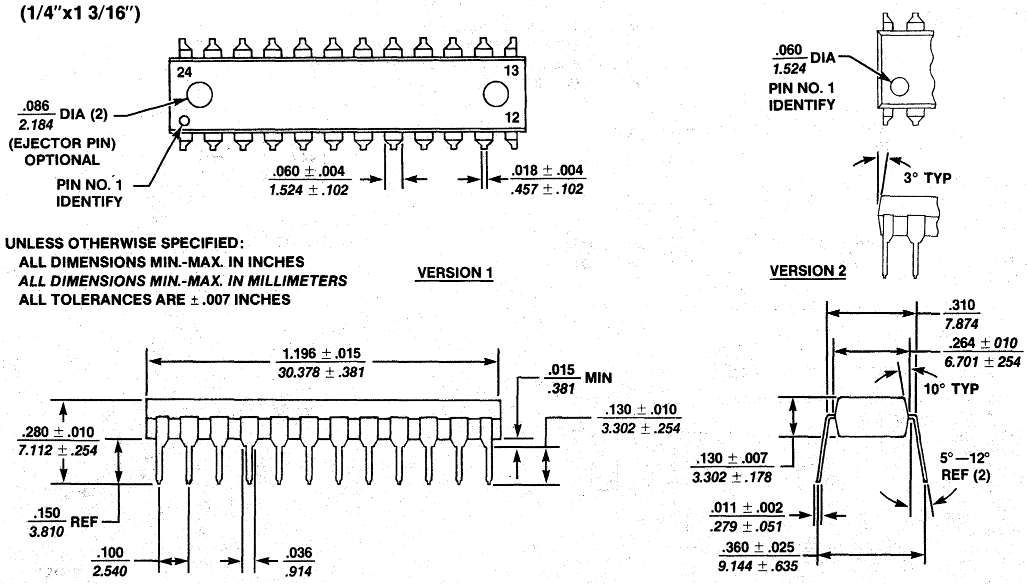
10MAR85

Package Drawings

20N Molded DIP
(1/4"x1")



24NS Molded SKINNYDIP
(1/4"x1 3/16")



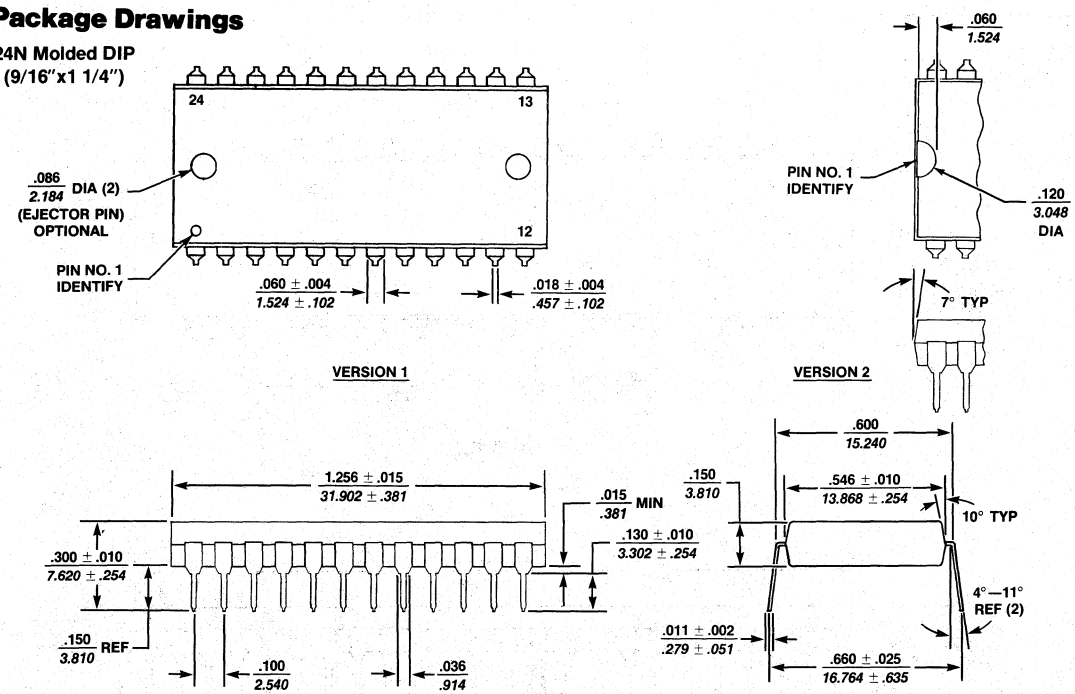
Notes:

1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both version 1 and version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on version 1 are optional.

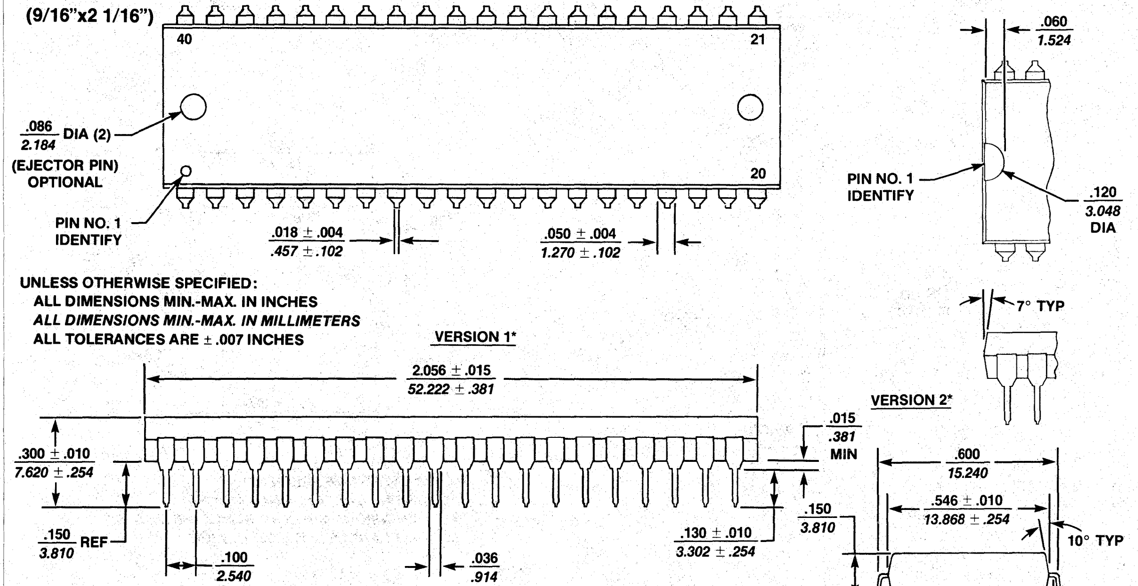
10MAR85

Package Drawings

24N Molded DIP
(9/16"x1 1/4")



40N Molded DIP
(9/16"x2 1/16")



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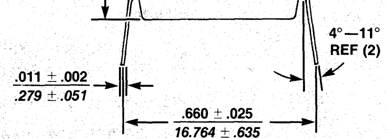


Notes:

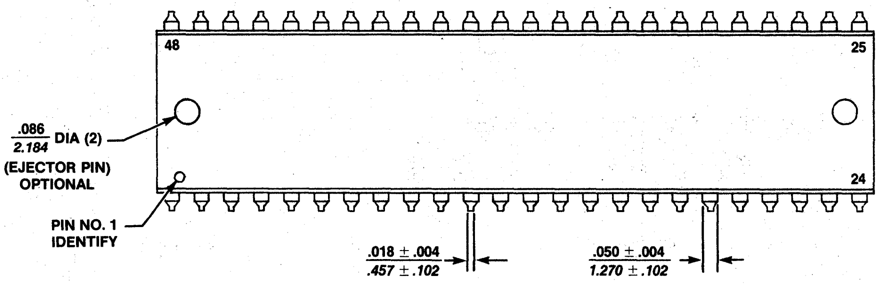
1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both version 1 and version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on version 1 are optional.

10MAR85

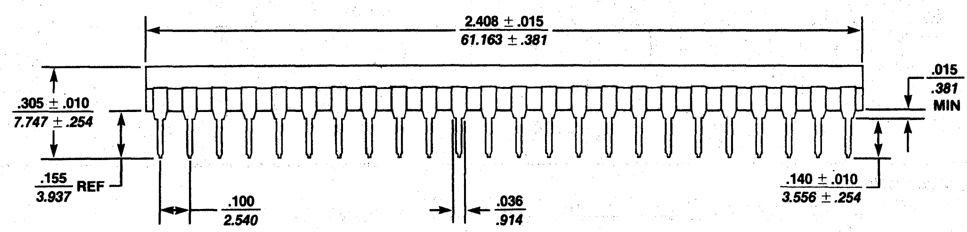
16

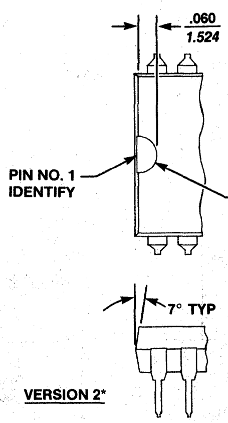
Package Drawings

48N Molded DIP
(9/16"x2 13/32")

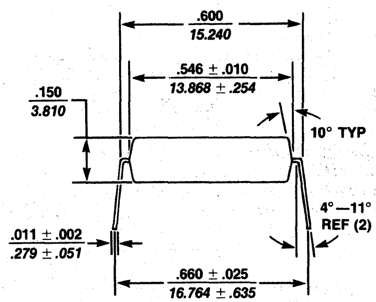


VERSION 1*





VERSION 2*



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Notes:

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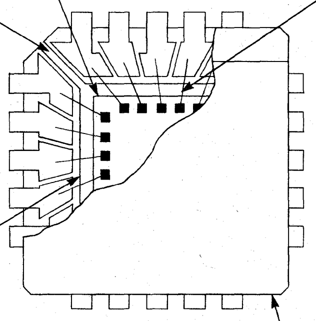
2. Both version 1 and version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on version 1 are optional.

10MAR85

Molded Chip Carrier

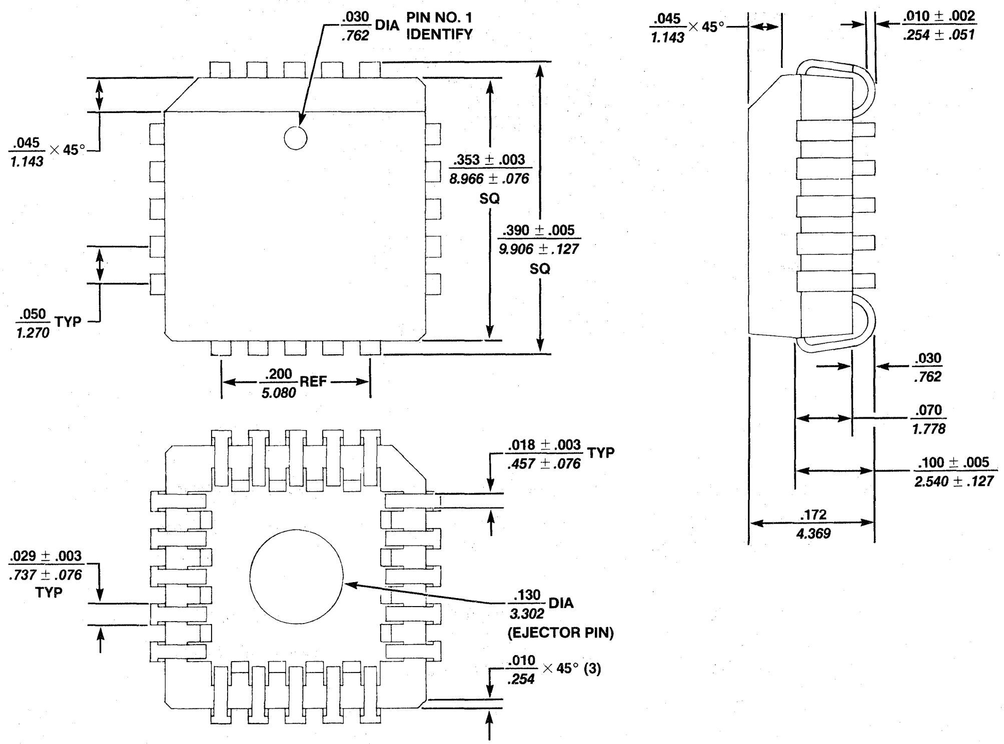


LEAD FRAME	BONDING WIRE	PACKAGE BODY
Copper Alloy 195. Copper Alloy Tamac 5.	1.25 Mil Gold Wire	Thermoset Plastic.
LEAD FINISH	**DIE PAD**	**DIE BOND**
Tin Plating. Solder Dip.	Spot Silver Plating (150 Microinches).	Silver Filled Epoxy.

16

Package Drawing

20NL Molded Chip Carrier
(.351"x.351")



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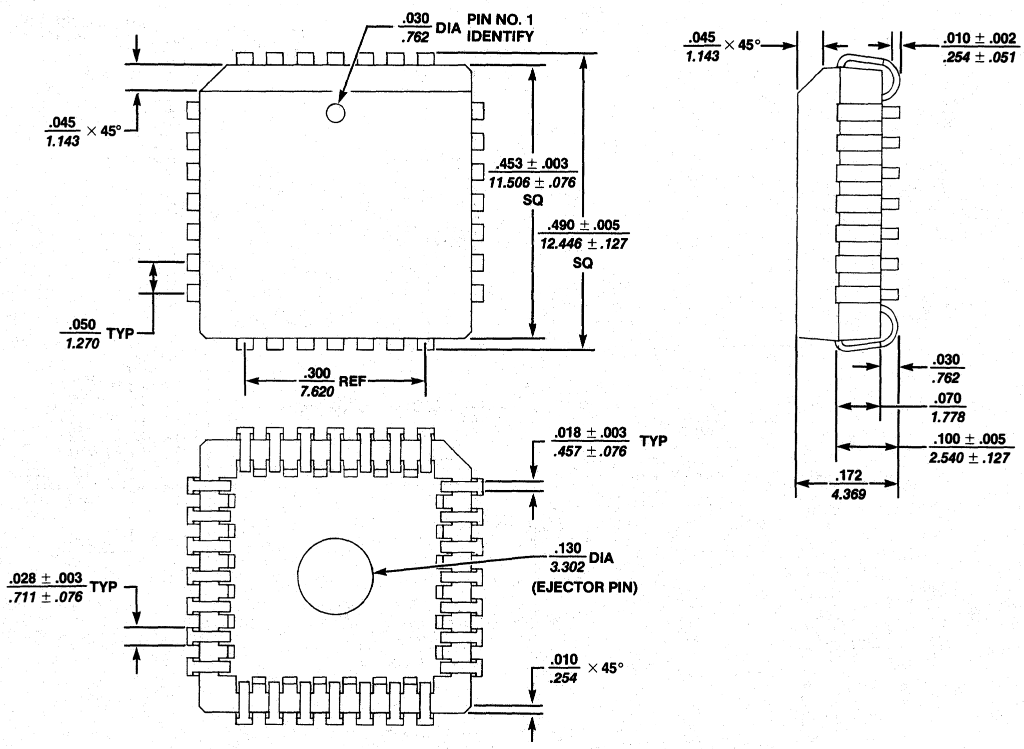
ALL TOLERANCES ARE ±.007 INCHES

Package Drawing

28NL Molded Chip
(.451"x.451")

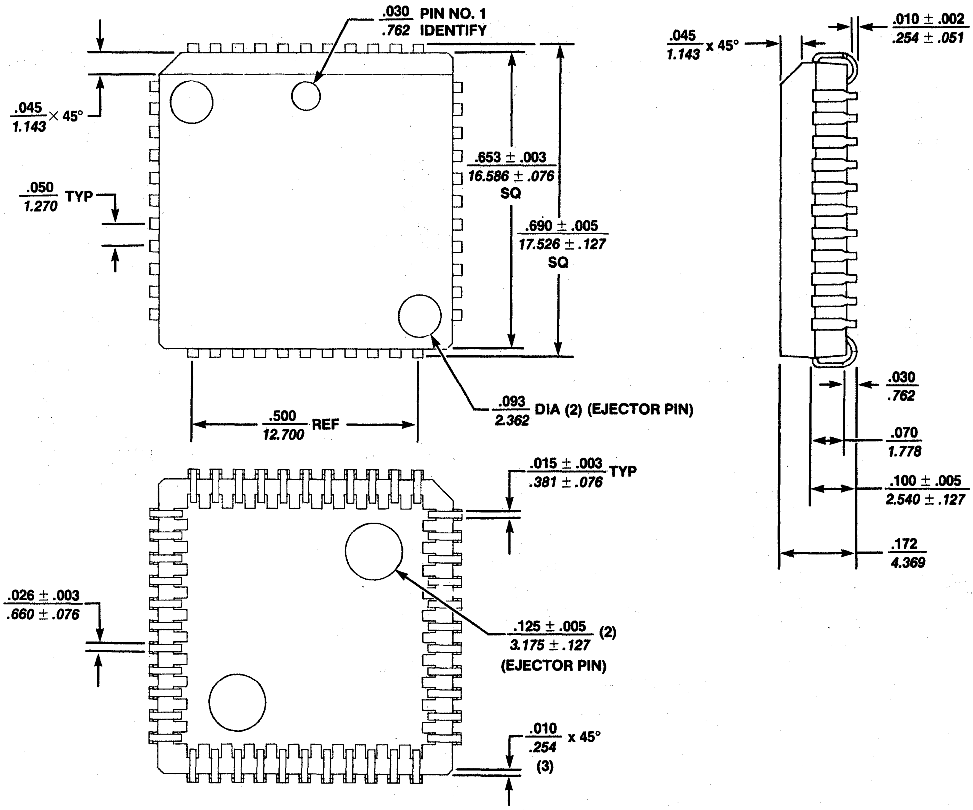


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

16

Package Drawing

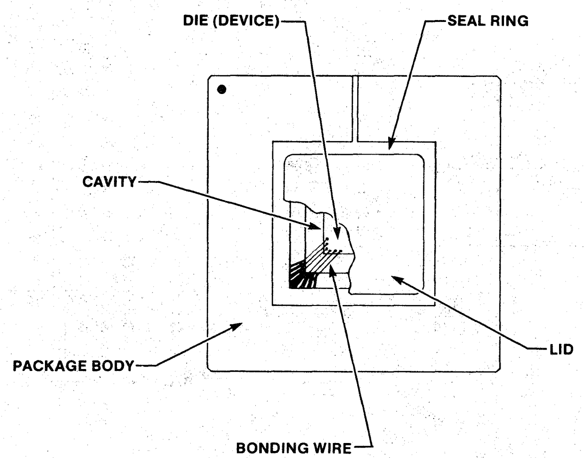
44NL Molded Chip Carrier
(.650"x.650")

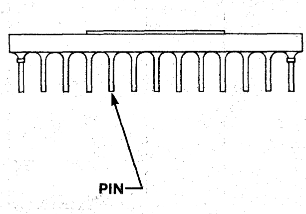


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawing

Pin Grid Array



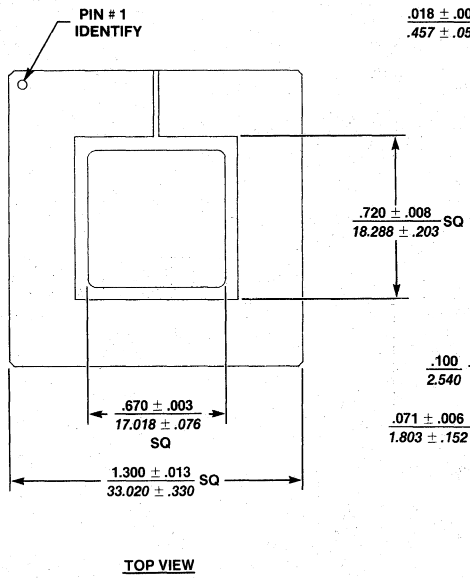


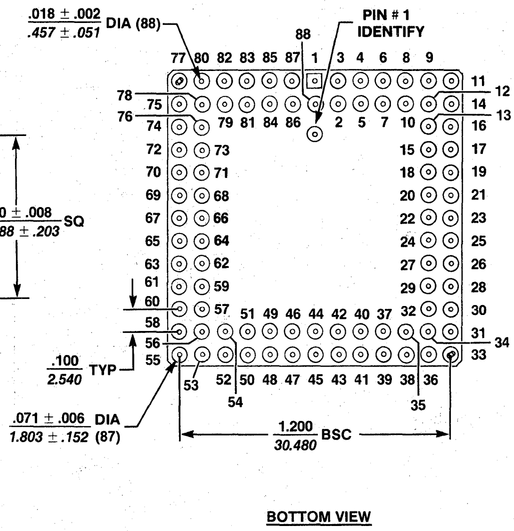
PACKAGE BODY	LID	PIN MATERIAL
Alumina (Standard Dark)	Gold Plated Kovar With Nickel Underplating	Gold Plated Kovar
BONDING WIRE	**CAVITY/SEAL RING**	
1.25 Mil Aluminum	Gold Over Tungsten	

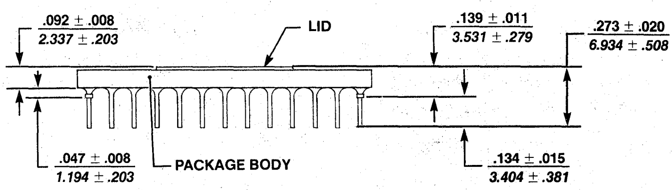
16

Package Drawing

**88P-1 Pin Grid Array (Cavity Up)
(1.300"x1.300")**







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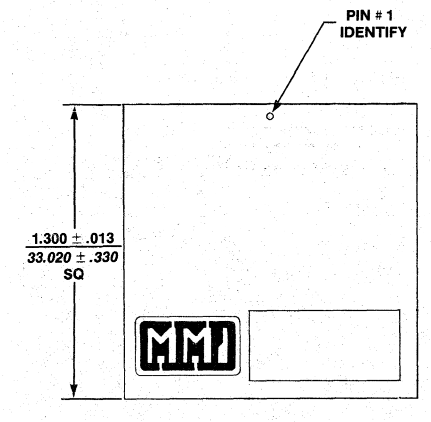
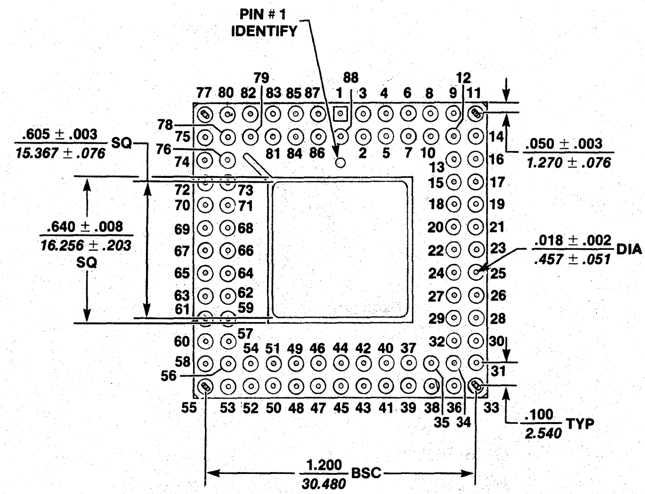
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawing

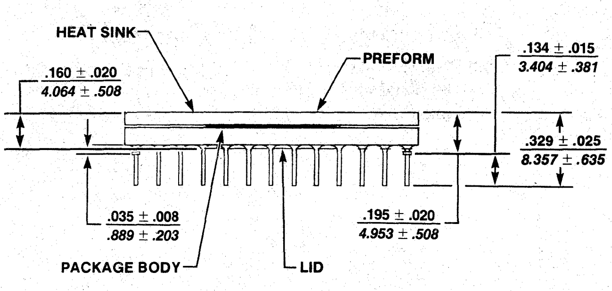
88P-2 Pin Grid Array (Cavity Down)
(1.300"x1.300")



TOP VIEW



BOTTOM VIEW



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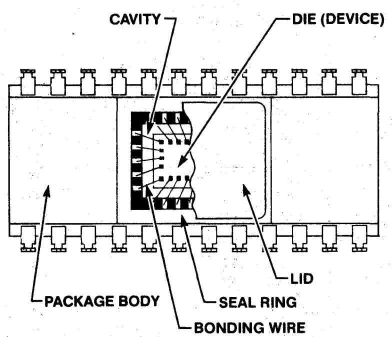
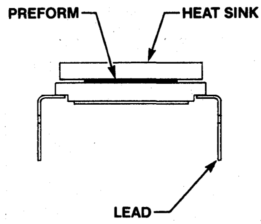
Package Drawing

Top Brazed

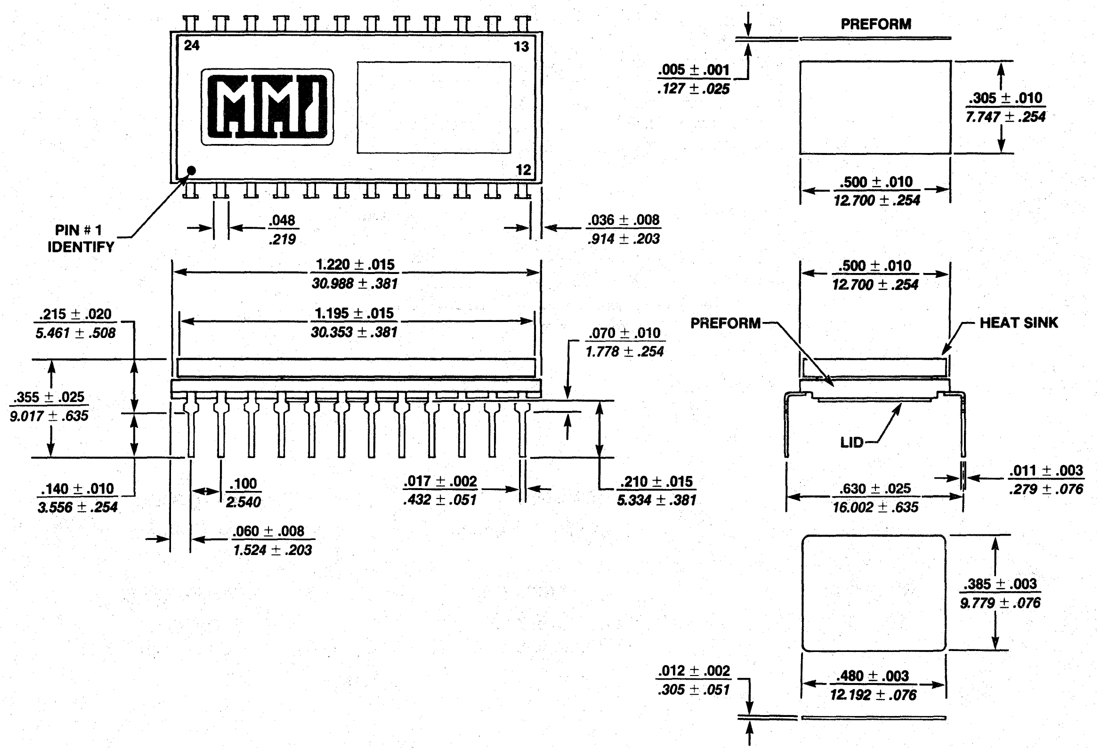




PACKAGE BODY	**LID**	**LEAD MATERIAL**	**HEAT SINK**
Alumina	Gold Plated Kovar With Nickel Underplating	Alloy 42	Blue Anodized Aluminum
BONDING WIRE	**CAVITY/SEAL RING**	**LEAD FINISHES**	**PREFORM**
1.25 Mil Aluminum	Gold Over Tungsten	Gold Plate (Standard) Solder Dip Over Gold Plate	Conductive Epoxy

Package Drawing

24T Top Brazed Ceramic Dip (With Heat Sink) (1/2"x1 1/4")



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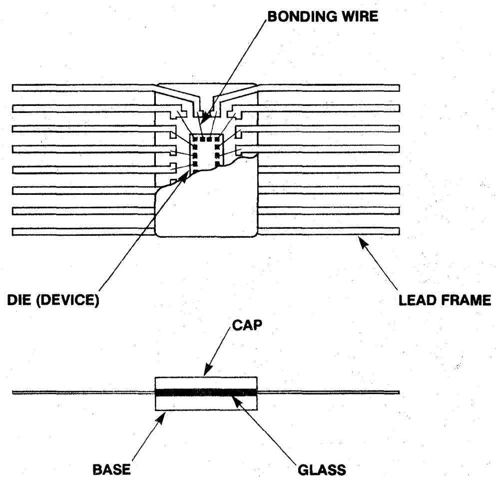
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

16

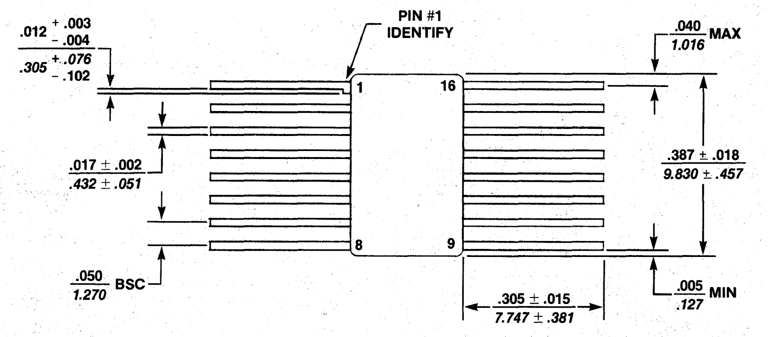
Cerpack

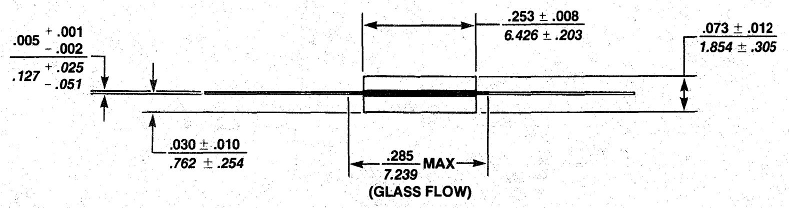


LEAD FRAME	BONDING WIRE	CAP AND BASE
Alloy 42	1.25 Mil Aluminum	Pressed Alumina
GLASS	**CAVITY**	**LEAD FINISHES**
LS-0113	Gold Over Alumina For Eutectic Die Attach	Tin Plate Solder Dip

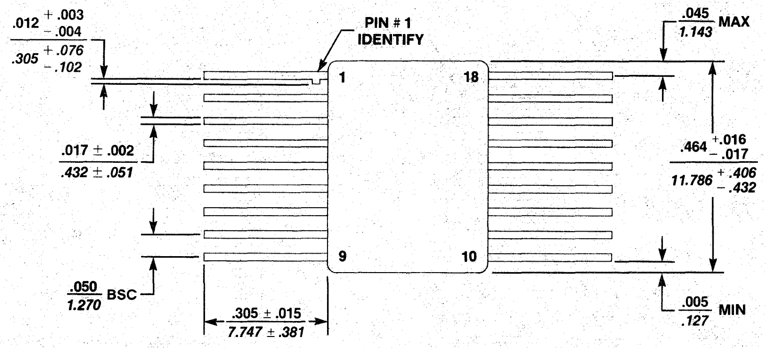
Package Drawings

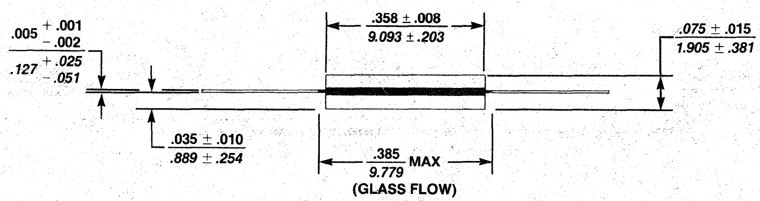
16W-3 Cerpack
(1/4"x3/8")





18W-1 Cerpack
(11/32"x15/32")





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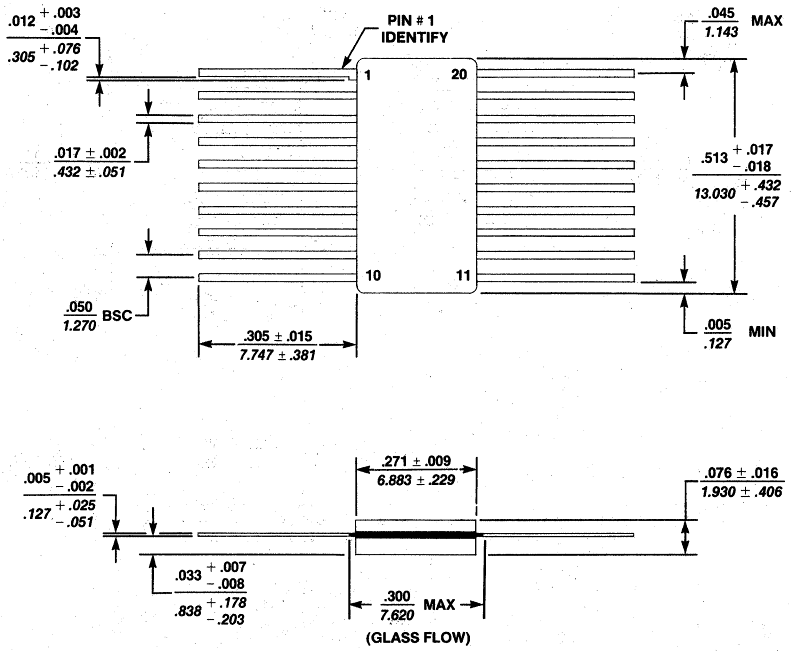
ALL TOLERANCES ARE ± .007 INCHES

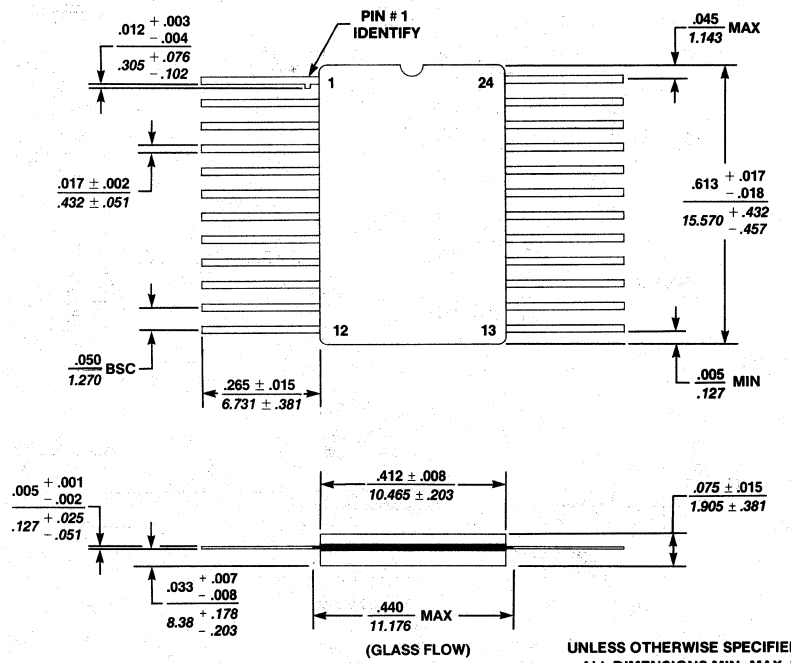
16

Package Drawings

20W-2 Cerpack (1/4"x1/2")



24W-2 Cerpack (3/8"x5/8")



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Power Dissipation Determination

Introduction

Thermal resistance for a packaged integrated circuit determines the operating temperature, and hence the performance and lifetime of the semiconductor device. For this reason, it is of interest to know the thermal impedance of the package configurations commonly in use and the effect of external factors such as air circulation and board-mounting conditions on the device temperature. To accomplish this end, measurement techniques and standards have been established providing certain conventions for data aquisition. Monolithic Memories has chosen to conform to these conventions in measurement and provides standard data for thermal impedance in the form of θ_{JC}, θ_{CA}, and a provision for obtaining θ_{JA} (resistance from junction to ambient) as a function of air movement over the package or package/board combination.

Use of Monolithic Memories data

In this publication data is presented for a variety of packages and ambient conditions. In order to simplify the data presentation, graphs of θ_{CA} vs. airflow are provided for packages in common use. These include socket-mounted dual-in-line packages such as p-dip, cerdip, and side-brazed packages, board mounted cerpacks and flatpacks, and free-standing leadless-chip carriers. Since θ_{CA} is a package geometry related function, the user need only look up the package type for the air-flow used. With this number, and knowledge of the die attach type, the total thermal resistance may be determined from the semiconductor junction to the ambient. Since the θ_{JC} is largely dependent on the package type and die attach type, a table has been constructed for easy use. (Although θ_{JC} is a die-size dependent variable for eutectic die attach, the effect of θ_{JC} on θ_{JA} is small enough that a constant may be used in most cases. For other die-attach methods, the thermal resistance was only slightly dependent on die size). After obtaining θ_{JC} and θ_{CA} as described above, the total thermal resistance, θ_{JA}, may be found by the addition of θ_{JC} to θ_{CA} as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

Notes on the tabulated data

1. All side-brazed, cerdip-sealed, and molded dual-in-line packages were mounted in zero insertion force sockets and placed transverse to the airstream. Thermocouples were mounted directly to the bottom of the package.
2. All cerpacks and flatpacks were board mounted in direct contact with a double-sided fiberglass-epoxy composite printed circuit board. The thermocouple was placed directly between the package and the board and fastened to the package.
3. All L_{CC} packages except the 84 PIN L_{CC} were freestanding, suspended by 28 GA. tinned copper wire soldered to pads corresponding to V_{CC} and GND. The 84 PIN L_{CC} was mounted in a single insertion socket. Thermocouples were attached directly to the bottom of the parts.

Thermal Impedance Measurement Procedure

Definition

Thermal impedance of a device is defined as the rise in the junction temperature against some reference point per unit of power dissipation or it may be described by the formula:

$$\frac{\Delta\, Tj\ (°C)}{Pd\ (Watts)}$$

Tj = temperature of junction
Pd = power dissipation

Theory

The principle of measuring the Thermal Impedance of a device is based on measuring the temperature of the hottest junction on the die under power dissipation. This is done by using the substrate diode to monitor the chip temperature. By reverse biasing and forcing a small forward current (500 μA) through the device under test (between + V_{CC} and ground), a large number of substrate diodes become forward-biased. By doing this, the hottest substrate diode junction is automatically detected, since it has the lowest voltage drop during this forward-biased condition. The forward voltage drop across the substrate diode is quite linear over a range of 25°C to 100°C. The hottest substrate diode is used as a "thermometer" to monitor the chip under power.

Procedure

A block diagram of the Thermal Impedance setup is shown in Figure 1. The substrate diode is forward biased by the Constant Current Source (-500 μA). The V_{CC} is supplied by the Power Supply, which is gated at 48.8 cycles/second, with a duty cycle of ≃ 99.5%. The V_F of the substrate diode is 'sampled' by the Sample/Hold circuit, which is gated synchronously with the V_{CC} supply, sampling is done for 40 μS, during each 100 μS window when the V_{CC} power supply is OFF. In addition to the V_F readings, the case temperature (closest to die attach point) and the Ambient temperature are monitored. The power dissipated (Pd) by the device is measured by DVM and calculated:

$$Pd = I_{CC} \times V_{CC}.$$

The device is mounted in a socket within a Wind Tunnel. The air speed within the wind tunnel is monitored with an Air Velocity meter. The air speed is adjustable from 0 to 1000 feet/min. The use of a wind tunnel allows us to graph the temperature of the die, in relation to the cooling air speed. The worst case θ_{JA} is at 0 air speed (STATIC).

Summary

The Thermal Impedance measurement can be summarized as follows:

1). Calibration of the ΔV_F/°C of the D.U.T. This is done by measuring the V_F at two different temperatures with the V_{CC} power supply OFF, and dividing the ΔV_F by the Δ°C.

2). Measurement of ΔV_F under operating conditions, under different air flow rates (0, 100, 500, 1000 ft/min.), while measuring °C case, °C ambient, I_{CC} and V_{CC}. The readings are recorded when the change in the case (°C case) temperature is less than 2% (of Δ °C case - °C amb) over a time of 30 seconds.

3). Calculation of Thermal Impedance

Symbol of Definitions

$V_{F1} = V_F$ @ low temp. cal. point (V_{CC} OFF)
$V_{F2} = V_F$ @ high temp. cal. point (V_{CC}OFF)
$°C_1$ = Case °C @ low temp. cal. point (V_{CC} OFF)
$°C_2$ = Case °C @ high temp. cal. point (V_{CC} OFF)
$V_{F3} = V_F$ under power, stablized
$°C_3$ = Case °C under power, stabilized
$°C_A$ = Ambient °C
$Pd = I_{CC} \times V_{CC}$

a) θ_{JC} (Junction to case)

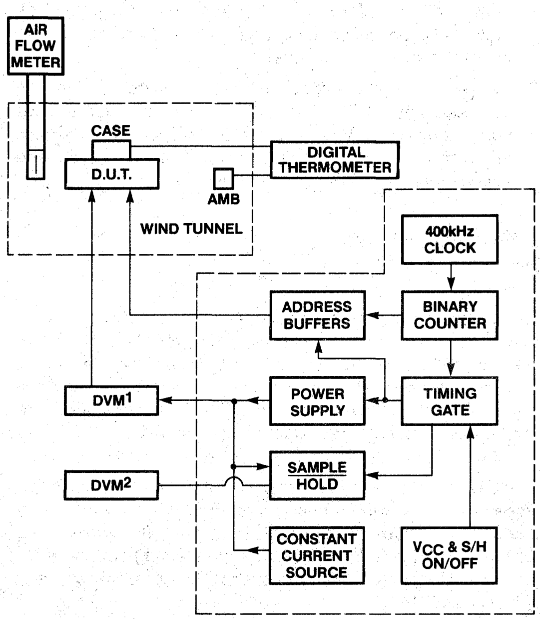
$$\theta_{JC} = \frac{\left[\left(\dfrac{(V_{F1} - V_{F3})}{\dfrac{V_{F1} - V_{F2}}{°C_2 - °C_1}}\right) + (°C_1 - °C_3)\right]}{Pd} = \underline{\hspace{3em}}\ °C/W$$

b) $$\theta_{CA} = \frac{(°C_3 - °C_A)}{Pd}$$

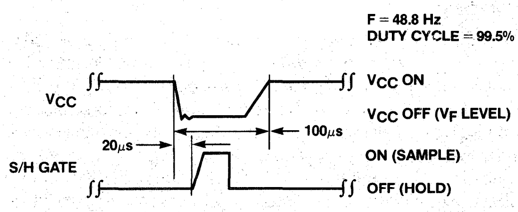
c) θ_{JA} (Junction to ambient)

$$\theta_{JA} = \theta_{CA} + \theta_{JC} = \underline{\hspace{3em}}\ °C/W$$

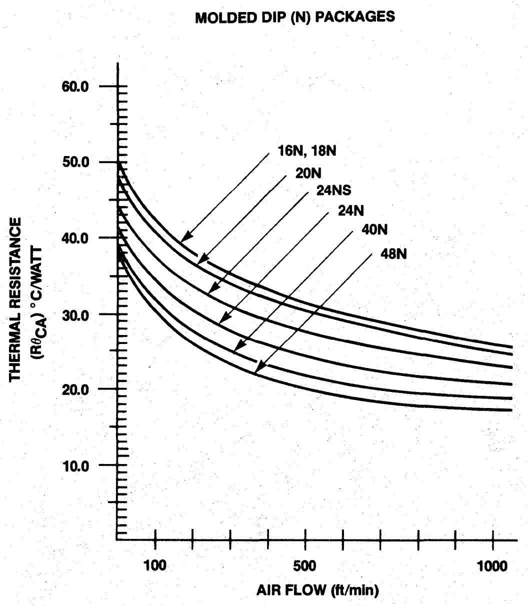
Block Diagram

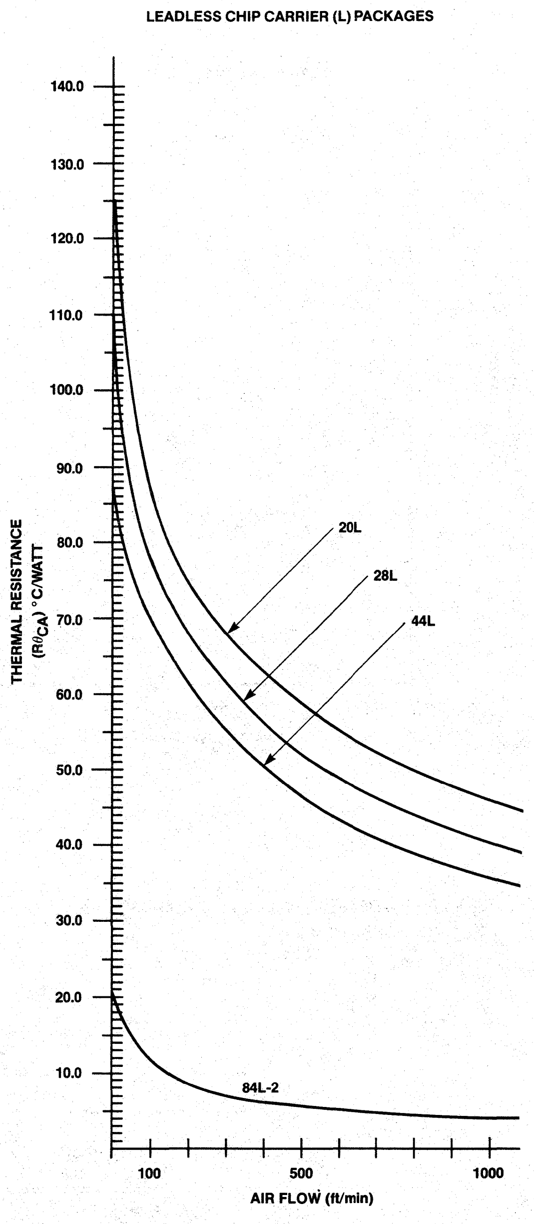


1). Digital Thermometer measures °C case and °C ambient
2). DVM:1 measures V_{CC} and I_{CC}
3). DVM^2 measures V_F of the substrate diode
4). BINARY counter creates A_0 thru A_{11};
A_θ = 100 kHz, A_1 = 50 kHz,
A_2 = 25 kHz etc. synchronious.
5). Timing gate switches the power supply, address buffers, and sample/hold circuits.
6). Constant current source provides –500 μA to the V_{CC} pin for the V_F measurement.
7). The airflow meter measures the air velocity for air-flow measurements.



Package Drawings





$R\theta_{JC}$ (°C/WATT) VALUES*		
DIE ATTACH	PACKAGE TYPE	
	L	N
Au/Si Eutectic	<4	N/A
Epoxy	N/A	15

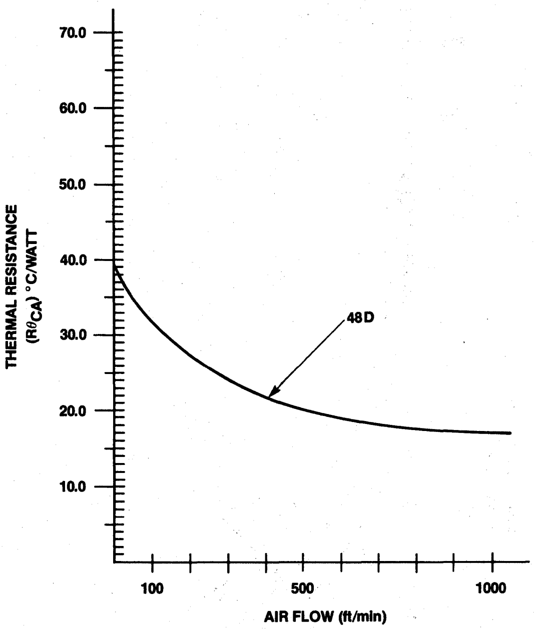
* These are typical values for die of 8,000 mils^2.
Most Monolithic Memories' products will be slightly lower.
$R\theta_{JA} + R\theta_{JC} + R\theta_{CA}$

NOTES:

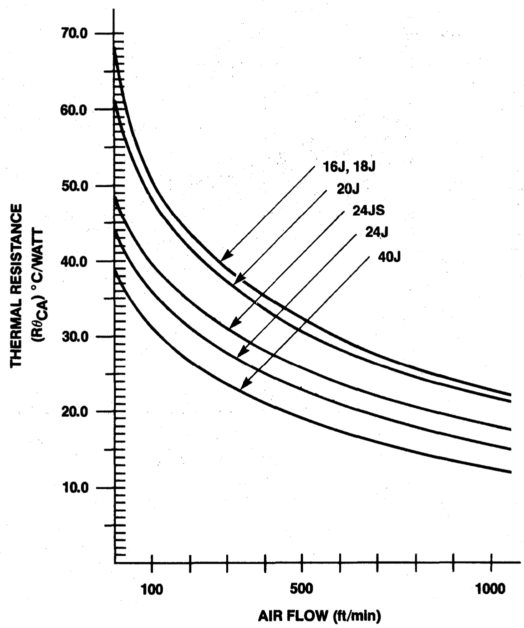
To determine $R\theta_{JA}$; first locate curve of $R\theta_{CA}$ vs air flow for the desired package. Read value of $R\theta_{CA}$ from this curve and add $R\theta_{JC}$ from the table below.

Package Drawings

SIDE BRAZED (D) PACKAGES



CERDIP (J) PACKAGES



NOTES:

To determine $R\theta_{JA}$; first locate curve of $R\theta_{CA}$ vs air flow for the desired package. Read value of $R\theta_{CA}$ from this curve and add $R\theta_{JC}$ from the table below.

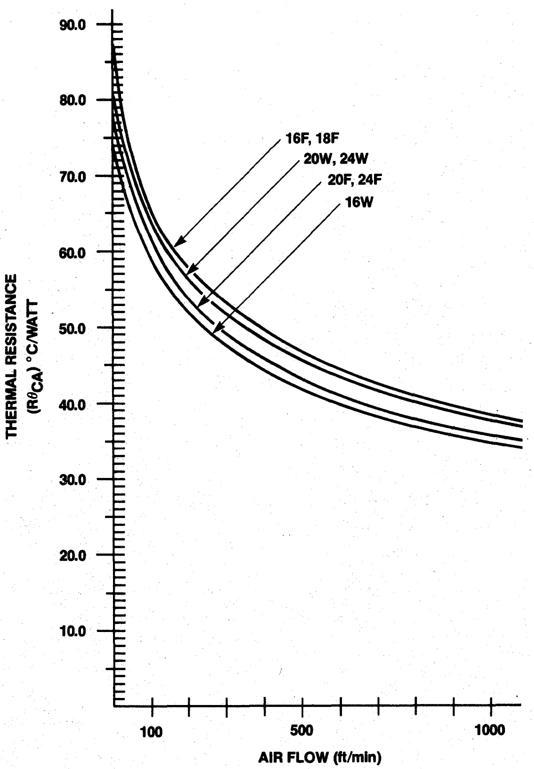
$R\theta_{JC}$ (° C/WATT) VALUES*		
DIE ATTACH	PACKAGE TYPE	
	D	J
Au/Si Eutectic	<4	<5
Epoxy	N/A	N/A

* These are typical values for die of 8,000 mils^2.
Most Monolithic Memories' products will be slightly lower.

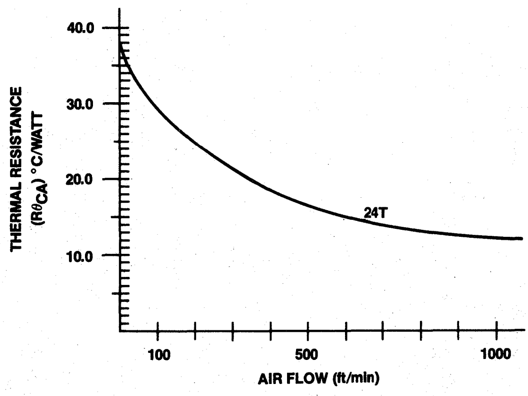
$R\theta_{JA} + R\theta_{JC} + R\theta_{CA}$

Package Drawings

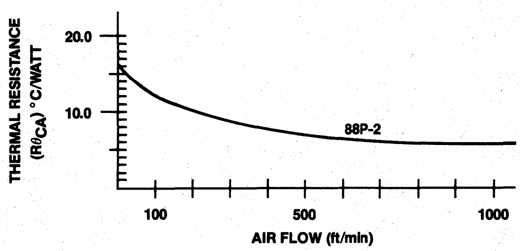
FLAT PACK (F), CERPACK (W) PACKAGES



TOP BRAZED CERAMIC PACKAGE



PIN GRID ARRAY (P) PACKAGE

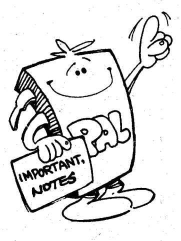


NOTES:

To determine $R\theta_{JA}$; first locate curve of $R\theta_{CA}$ vs air flow for the desired package. Read value of $R\theta_{CA}$ from this curve and add $R\theta_{JC}$ from the table below.

$R\theta_{JC}$ (° C/WATT) VALUES*				
DIE ATTACH	PACKAGE TYPE			
	F	P	T	W
Au/Si Eutectic	<4	<4	<4	<4
Epoxy	N/A	N/A	N/A	N/A

* These are typical values for die of 8,000 mils^2.
Most Monolithic Memories' products will be slightly lower.
$R\theta_{JA} + R\theta_{JC} + R\theta_{CA}$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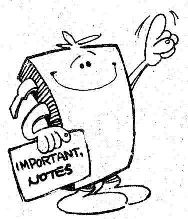
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