DESIGNING DIFFUSED INTEGRATED CIRCUIT RESISTORS

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ELECTRONIC INDUSTRIES

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Certain problems arise when both passive and active circuit elements are constructed in a solid crystal of semiconductor material. A method is shown here for obtaining resistors by diffusing a thin layer of p- or n- type impurity into a substrate of the opposite type material.

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In integrated circuits, when the active and passive circuit elements are constructed in a solid crystal of semiconductor material, conventional methods of obtaining circuit resistance are not always possible or practical.

One method of obtaining a compatible resistor is by diffusion. The resistor is obtained by diffusing a thin layer of p- or n-type impurity into a substrate of the opposite type material. The resistance of this layer will depend on the concentration profile of the impurity in the diffused material, the depth of diffusion, and the length-to-width ratio of the diffused area. For uniformly doped bulk semiconductor material, the end-to-end resistance R is given by

$$R = \frac{\rho l}{t w}$$

where

ρ = the resistivity of the material (ohm-cm)
l = length of the material (cm)
w = width of material (cm)
t = thickness of material (cm).

With diffused resistors used in integrated circuits, the diffusion depth is extremely small and is relatively constant. The resistance value of the diffused area can be stated in terms of the sheet resistance (R_S) of the material, measured in ohms/sq, and the l/w ratio of the diffused area as:

$$R = \left(\frac{\rho}{t}\right)\frac{l}{w} = \left(R_S\right)\frac{l}{w}$$

When silicon is used, we can take advantage of the protective coating of silicon dioxide (SiO_2) which may be grown on the surface of the crystal. This dioxide coating acts as both a mask against impurity diffusion and as an insulating and passivating coating for the junctions. Fig. 1 illustrates the construction of a typical unit. As shown in Fig. 1a, an area, the length and width of which partially determines the value of the resistor, is etched through the silicon dioxide. The unit is then placed in a furnace for a boron diffusion to form a p-type layer, several microns deep, as shown in Fig. 1b. The silicon

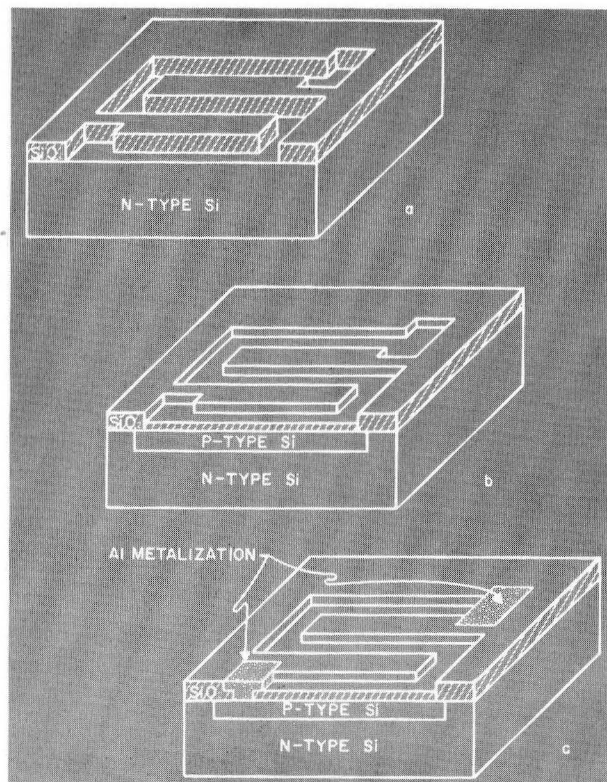


Fig. 1: Construction of a typical unit.

linear current voltage relationship. Measurements indicate that the maximum power dissipation, for units mounted in a standard TO18 can, is on the order of 3 mw per square mil of diffused area.

V-I Characteristics

Fig. 6 illustrates the V-I characteristics at high power levels. The maximum voltage drop across the unit is limited by the reverse voltage breakdown of the p-n junction in the substrate. This value is normally in the range of 30-80 volts, as shown in Fig. 7, depending only upon the impurity concentration of substrate material. Because of the small cross-section of the diffused area, there is also a limitation on the maximum current due to current limiting effects. However, this effect is usually hidden by the heating action at high currents.

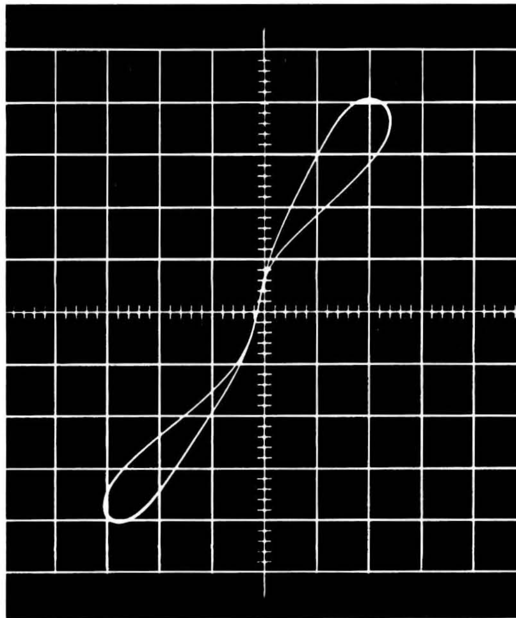


Fig. 6 (l): The V-I characteristics at high power levels. (20 ma/div.—vert., 10 v./div.—horiz.)

Typical applications of these devices usually fall into two general categories: applications such as load and bias resistors or applications involving the use of the substrate connection, such as R-C filters and "speed-up" resistors in logic circuits.

When used as a single independent element, these devices may be connected as any standard resistor, within the rated values. However, when included in fully integrated circuits in conjunction with other elements, the proper bias voltage must be maintained between the resistance element and the substrate material.

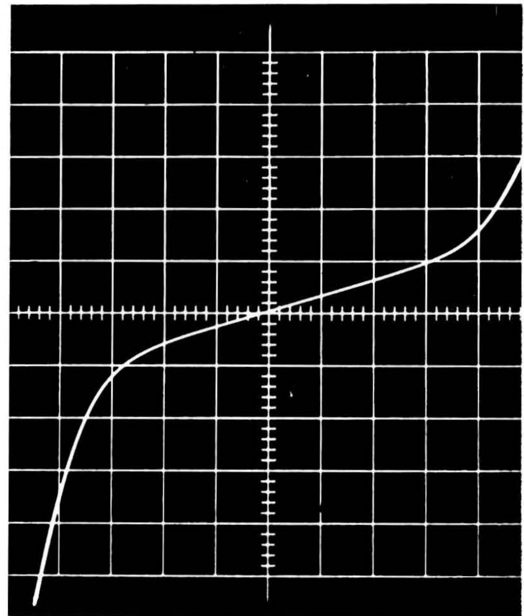


Fig. 7 (r): Reverse voltage breakdown is normally in the range of 30-80 v., depending on the impurity concentration of substrate material.

As shown in the example in Fig. 8, a p-type diffusion may be used for the emitter resistor directly on the n-type collector region. In this example, the substrate potential is always greater than the potential of any portion of the resistance element, and thus the p-n junction remains reverse biased. In the example of Fig. 9, the p-type diffusion is always at a higher potential than the remainder of the circuit, and thus the resistor substrate must be electrically isolated from the remaining circuit elements. In this example, the isolation is accomplished by n- and p-type regions forming back-to-back diodes between the circuit elements.

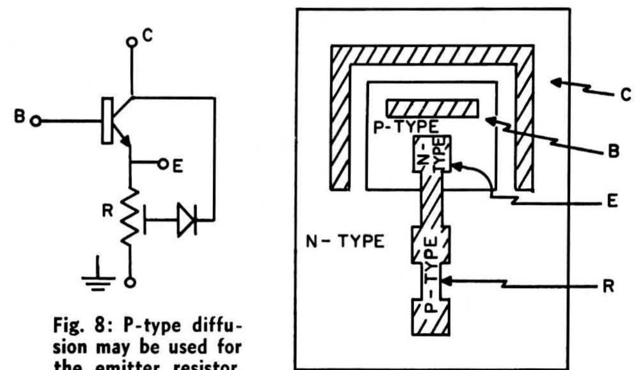


Fig. 8: P-type diffusion may be used for the emitter resistor.

dioxide forms again during the diffusion and is then etched again to form holes for the ohmic contact areas as shown in Fig. 1c. Aluminum or gold is deposited into the holes to form the ohmic contact to the p-type layer. Wire leads may be bonded to the metalized areas by standard techniques. Fig. 2 is a photograph of a group of diffused resistors used for test purposes. Typical values of resistance obtained by this method may range from 10 ohms to 100K ohms. Tolerances may be controlled to $\pm 10\%$ in the diffusion process. When two or more resistors are diffused into the same substrate, the resistance values will vary slightly, even for identical pattern configurations, due to the properties of the substrate. Normally, however, these variations can be held to within $\pm 3\%$.

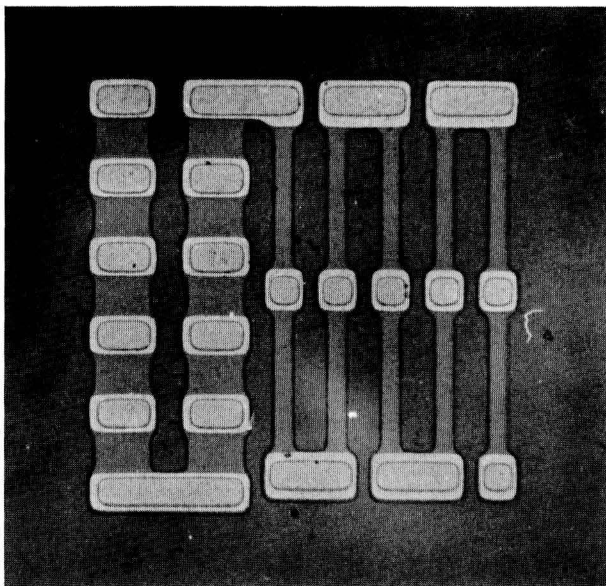


Fig. 2: Diffused resistors used for test purposes. Typical values from 10Ω to 100 KΩ.

Equivalent Circuit

The equivalent circuit of a diffused resistor is shown in Fig. 3. A diode and the distributed capacitance of the p-n junction is available when a contact is made to the substrate material. Some of the values of these parameters which are indicated in Fig. 3 are as follows:

$$BV_f \approx 0.5 \text{ volt}$$
$$BV_r \approx 50 \text{ volts}$$
$$I_{co} \approx 10 \text{ nanoamps}$$

where

BV_f = forward voltage drop across the junction

BV_r = reverse breakdown voltage of junction

I_{co} = leakage current of junction

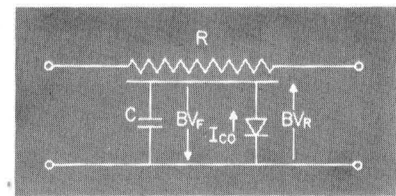


Fig. 3. Equivalent circuit for a diffused resistor.

The value and variation of the capacitance will be discussed later. These parasitics must be taken into account, as shown later, when the substrate becomes part of an integrated circuit.

The following parameters are usually considered, in addition to the above values, to describe a diffused resistor: (1) frequency effects, (2) parasitic capacitance, (3) temperature coefficients, and (4) maximum ratings.

Fig. 4 illustrates, in terms of "h" parameters, some of the characteristics of a diffused 5K ohm resistor as a function of frequency. These results were obtained with the substrate as the common ground and with the resistor terminals as the input and output. The plot of

$$h_{21} = i_2/i_1$$

where

i_1 = input current

i_2 = output current

illustrates the transfer characteristics while the plot of

$$h_{11} = v_1/i_1$$

where

v_1 = input voltage

illustrates the actual values of resistance as a function of frequency. As shown, these measurements indicate useful resistor action up to nearly 10 MC. However, by isolating the substrate, the parasitic capacitance effect is reduced and the frequency range is extended.

For resistors of this type, the distributed junction capacitance is a function of both the impurity concentration of the substrate and the voltage across the p-n junction. As an example, a diffused resistor of 100 ohms per square, diffused 3 microns deep into 0.5 ohm-cm silicon, will have approximately 0.13 pf/mil^2 at 1 v. reverse bias. The value of this capacitance also closely follows the theoretical form for a reverse biased graded junction of

$$C = KV^{-1/3}$$

where

$K = 18 \times 10^{-12}$.

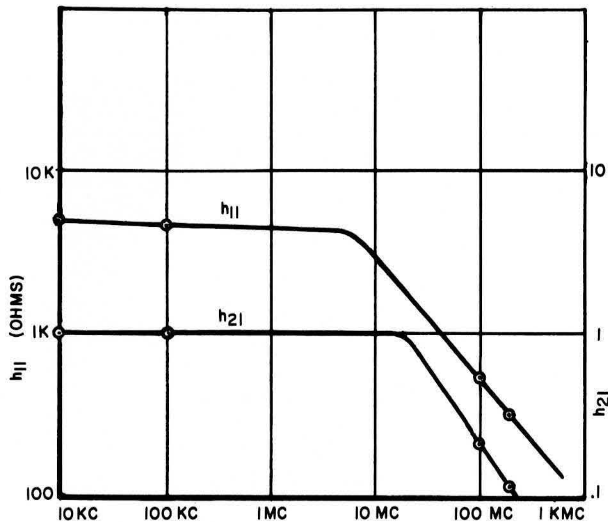


Fig. 4: Characteristics of diffused 5K resistor as a function of frequency.

Thus the effective junction capacitance may be governed by a reverse bias voltage placed on the resistor substrate.

The temperature coefficient is another variable which should be considered in the application of these devices to integrated circuits. One of the most critical parameters affecting the value of the temperature coefficient is the surface impurity concentration of the diffused area. The total resistance R of the units is determined primarily by ρ as given by

$$R = \frac{\rho_{ave} l}{A}$$

where

l = the length of the diffused area
area A = the width times depth of the junction
ρ_{ave} = an average value of the resistivity in the diffused area.

From semiconductor theory, in a highly concentrated p-type layer, ρ is given by

$$\rho = \frac{1}{q \mu_p p}$$

where

q = the electron charge
p = the hole concentration
μ_p = the hole mobility.

Thus, in the normal temperature range, μ_p is the primary temperature dependent parameter in the determination of R. Gartner[1] shows how the temperature variation of hole mobility is a function of the impurity concentration, becoming less temperature dependent with the higher concentrations. The mobility normally decreases with temperature, thus giving a positive temperature coefficient for the total resistance of the unit. However, for high impurity concentrations (10^{19} to 10^{20} atoms per cc) of both n- or p-type, the mobility remains relatively constant over the normal temperature range.

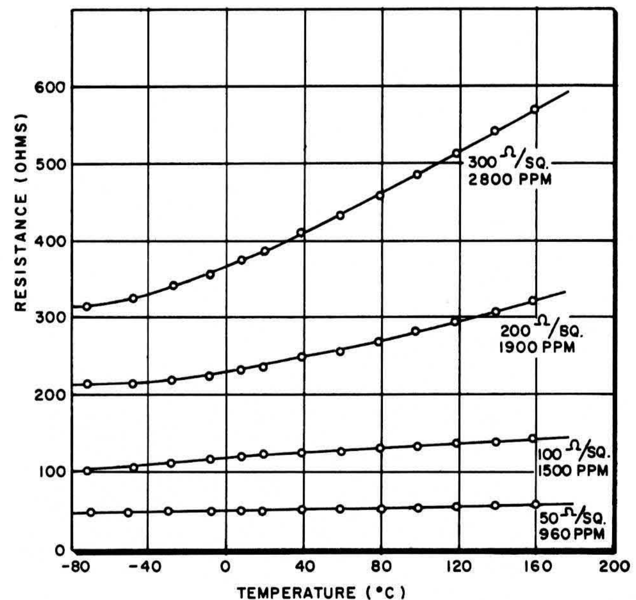
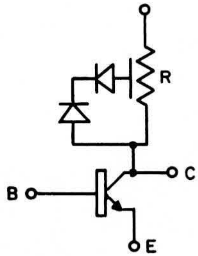


Fig. 5: Various resistor values plotted as a function of temperature.

This effect is shown in Fig. 5 where various resistor values are plotted as a function of temperature. The top curve illustrates the effect of a low value of impurity concentration (approximately 10^{18} atoms per cc), while the lower curves show the effect of higher concentrations. At 100 ohms per square, diffused approximately 3 microns deep, the temperature coefficient is approximately 1500 parts per million per degree Centigrade. Thus the temperature coefficient of the diffused resistor may be controlled to a great extent by the initial surface impurity concentration of the diffused area.

There are some inherent low frequency limitations in the application of these devices, mainly power dissipation and maximum voltage ratings. The amount of power dissipation in the resistor is limited primarily by the heating effects on the material of the diffused layer. Excessive heating will result in a non-



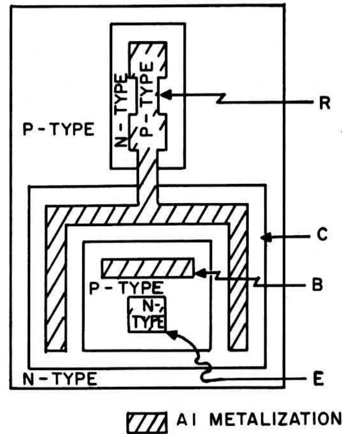
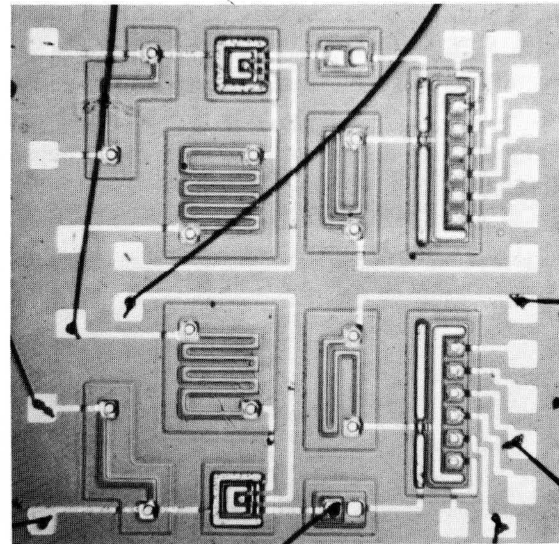


Fig. 9: Resistor substrate here must be electrically isolated.

Other Applications

In other applications, the inherent parasitic junction capacitance of the device may be used to an advantage. In some applications, such as the coupling resistor of a flip-flop circuit, a small speed-up capacitor is usually placed in parallel with the resistor. By connecting the isolated substrate to one terminal of the diffused area, part of the junction capacitance will appear across the resistor. Hurley[2] has shown that for a resistor with a distributed capacitance, approximately 1/2.7 of the total junction capacitance will appear in parallel when connected in this manner. Thus for some applications, a diffused resistor is capable of performing a dual function. Fig. 10 illustrates an actual application of diffused resistors in an integrated circuit.

Fig. 10: Application in an integrated circuit.



Acknowledgments

1. Gartner, W. W., *Transistors.* Princeton, New Jersey: D. Van Nostrand Company, Inc., 1960.

2. Hurley, R. B., "Approximations to Distributed Speed-Up Capacitance," *Electronic Equipment Engineering,* December, 1961.

3. Much of this work was done under Air Force Contract #AF33-(616)8276 on Compatible Techniques for Integrated Circuits.

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