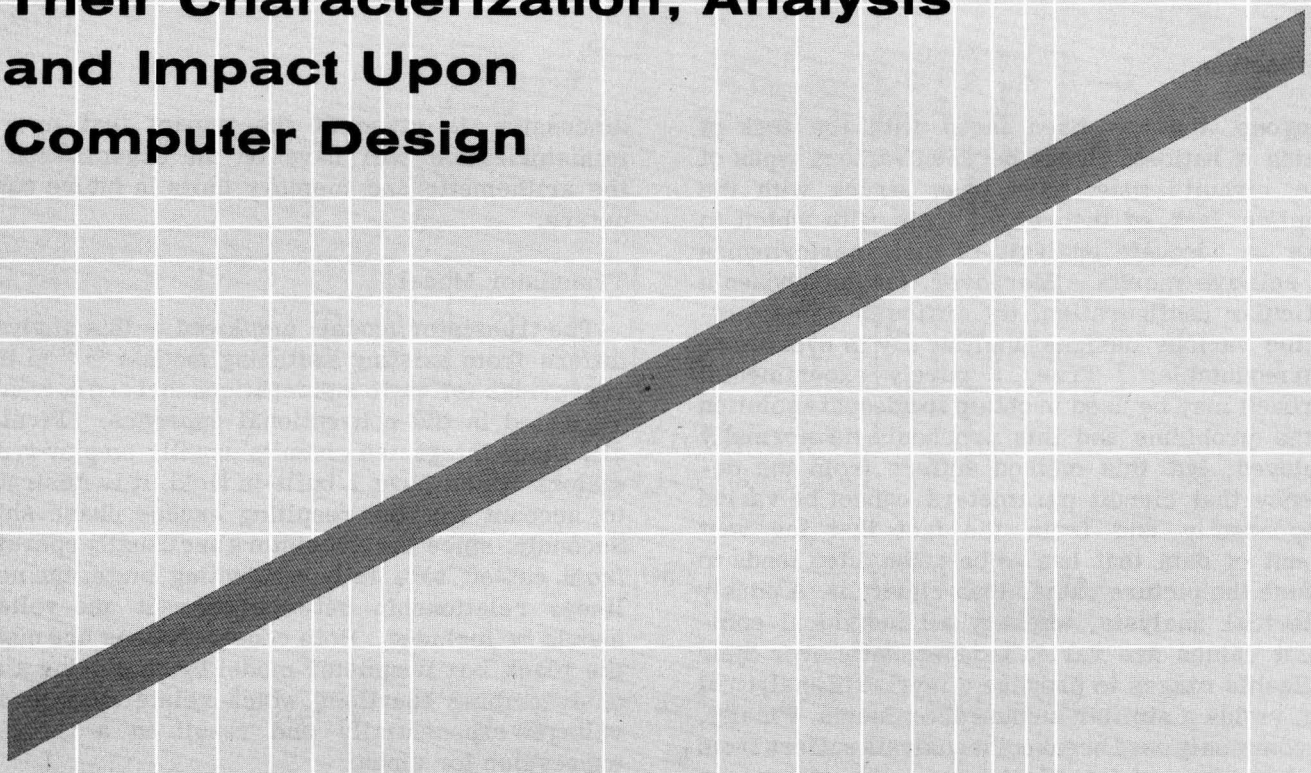
Microminiaturized Logic Circuits: Their Characterization, Analysis and Impact Upon Computer Design



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Introduction

Anyone who has been faced with the task of making a rational choice between various types of logic circuits must have been struck with the complete lack of theoretical tools with which to make an adequate analysis of their performance and relative merits. Moreover, having chosen a particular configuration, the difficulty of optimizing the various designs analytically is even more insurmountable. True, a purely experimental approach may be used to obtain an adequate solution to the problems and this procedure is normally employed; but this method suffers from the deficiency that circuit parameters cannot be varied independently and from the fact that the vast amount of data that has to be taken often tends to confuse the picture rather than clarify it. A purely numerical analysis, whereby all individual component values are varied independently over their applicable ranges to produce a myriad of analytical data, yields a similar amount of confusion. Finally, the commonly used breakpoint analysis suffers from the deficiency of introducing too many extraneous parameters that are not essential to the solution of the problem. Also, breakpoint analysis sometimes leads one into traps causing erroneous solutions because of the simplifying assumptions made. Hence, there exists a great need for nonlinear analysis techniques in combination with a more quantitative understanding of applicable approximations and their validity.

This paper does by no means claim to solve all the problems involved, but merely to indicate a possible approach. With the advent of microminiaturization of logic circuits, there will be a greater need for synthesizing system functions directly from the device properties without resorting to the side step of analyzing circuits consisting of separate components. Before the synthesis problem can be tackled, however, methods of analysis must first be developed.

To demonstrate this approach an attempt is made to characterize a logic circuit in terms of non-linear black box characteristics and to show how these characteristics can be derived from the fundamental device equations. Finally, a brief discussion is given of the impact that microminiaturization will have on the organization of the arithemetic and memory units in future computers.

Transistor Model

The transistor model[1] employed in this analysis differs from existing switching models [2, 3] in that it provides for two considerations that are normally neglected in the conventional approach. First of all, since integrated circuits usually employ transistors which have a built-in field, it is desirable to account for the resulting excess phase shift. Secondly, since the transistors are usually operated from cut-off to a fully conducting state, the nonlinear relationship between current and voltage should be included. Both considerations are met in the black box transistor model by employing a set of describing equations which relate current and voltage exponentially and result in a two-pole expression for alpha.

The formal derivation of the black box model has been performed for both the diffusion (no base field) and the drift (constant base field) transistors. The procedure starts with the diffusion equation and employs the Laplace Transform to obtain a solution for the minority carrier density in terms of hyperbolic functions. A linear relationship between the terminal currents and the minority carrier density is obtained through the use of a power-series-approximation for the hyperbolic functions. By interpreting the results in the time domain and employing the junction relationship between minority carrier density and voltage, the following set of describing equations is obtained:

$$i_e = a_{11}(1+\tau_{11}s)\left(e^{\frac{q\phi_e}{KT}}-1\right) - \frac{a_{12}}{1+\tau_{12}s}\left(e^{\frac{q\phi_c}{KT}}-1\right) \quad (1)$$

$$i_c = -\frac{a_{21}}{1+\tau_{21}s}\left(e^{\frac{q\phi_e}{KT}}-1\right) + a_{22}(1+\tau_{22}s)\left(e^{\frac{q\phi_c}{KT}}-1\right) \quad (2)$$

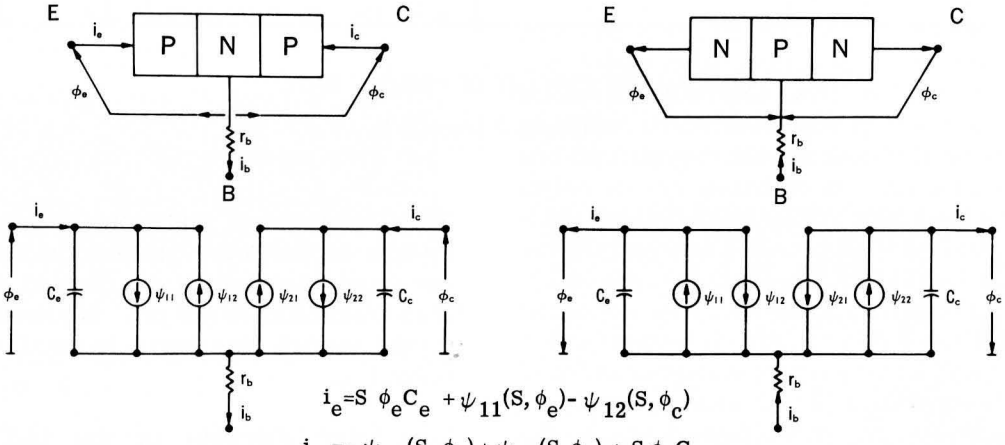
where $s = \frac{d}{dt}$

ϕ_e, ϕ_c = emitter and collector junction voltages (defined as the potential of the p material with respect to the n material)

i_e, i_c = emitter and collector currents (positive sense defined as flowing from the p material to the n)

The definition of current sources ($\psi 11, \psi 12, \psi 21$ and $\psi 22$) from the describing equations, and the addition of base resistance and collector and emitter depletion layer capacitance results in the transistor model illustrated in Figure 1.

TRANSISTOR MODEL



$$i_e = S\,\phi_e C_e + \psi_{11}(S, \phi_e) - \psi_{12}(S, \phi_c)$$

$$i_c = -\psi_{21}(S, \phi_e) + \psi_{22}(S, \phi_c) + S\,\phi_c C_c$$

$$\psi_{11} = a_{11}(1+\tau_{11}S)(e^{\frac{q\phi_e}{KT}} - 1) = a_{11}(1+\tau_{11}S)f(\phi_e), \quad \psi_{12} = \frac{a_{12}}{1+\tau_{12}S}(e^{\frac{q\phi_c}{KT}} - 1) = \frac{a_{12}}{1+\tau_{12}S} f(\phi_c)$$

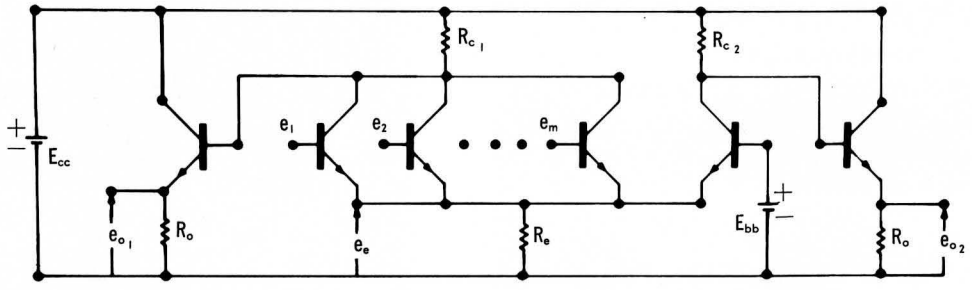
$$\psi_{21} = \frac{a_{21}}{1+\tau_{21}S}(e^{\frac{q\phi_e}{KT}} - 1) = \frac{a_{21}}{1+\tau_{21}S} f(\phi_e), \quad \psi_{22} = a_{22}(1+\tau_{22}S)(e^{\frac{q\phi_c}{KT}} - 1) = a_{22}(1+\tau_{22}S)f(\phi_c)$$

$$S = \frac{d}{dt}$$

FIGURE 1-

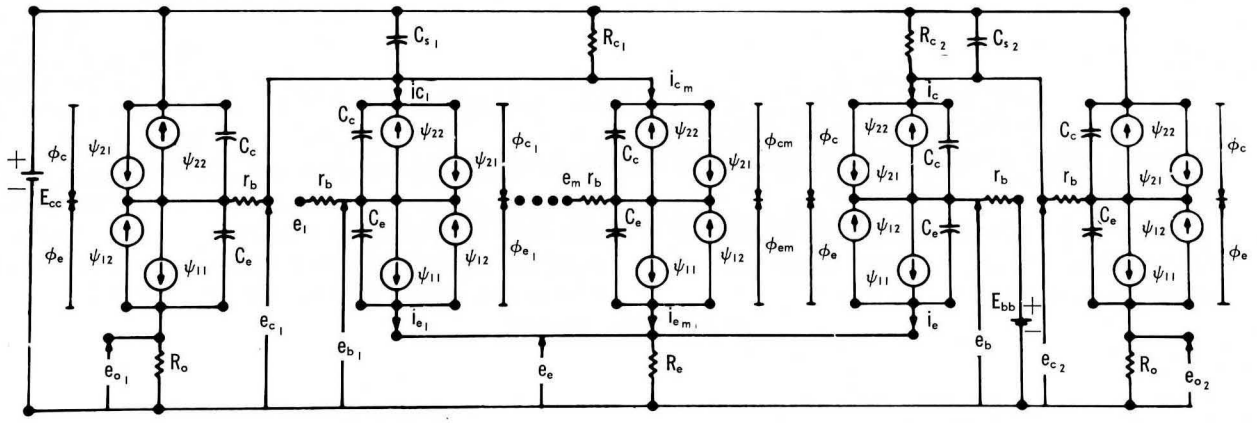
D.C. Considerations

The D.C. characteristics of a logic gate may be presented in black box form and the black box parameters may be related to the basic parameters of the active and passive components of the integrated circuit. As a vehicle for this demonstration we will use the MECL logic gate shown in Figure 2a. The gate is assumed to have a fan-in of m and the two outputs perform respectively the OR and NOR logic functions of the inputs when the logical one is defined as a high potential. Using the large-signal model for the transistor described in the previous section, the complete equivalent circuit for the MECL case is as shown in Figure 2b. Assuming the inverse alpha (α_i) to be much smaller than the forward alpha (α_f), the current through the common emitter resistor R_e may be written:



THE "MECL" LOGIC GATE

FIGURE 2-a



EQUIVALENT CIRCUIT OF "MECL" GATE

FIGURE 2 (cont.)- b

$$I_e = \sum_{r=1}^{m} a_{11_r}\left(e^{\frac{q}{KT}(e_{br}-e_e)}-1\right) + a_{11}\left(e^{\frac{q}{KT}(E_{bb}-e_e)}-1\right) = \frac{e_e}{R_e} \tag{3}$$

Solving for e_e and taking into account the incremental increase of I_e when any of the input transistors are conducting, we obtain:

$$e_e = E_{bb} + \frac{KT}{q}\ln\left(1+\sum_{r=1}^{m}\frac{a_{11r}}{a_{11}}e^{\frac{q}{KT}(e_{br}-E_{bb})}\right) - E_{eb} \tag{4}$$

In the case where all transistors are identical and if a given number (r) of the m transistors are being turned on, this expression reduces to:

$$e_e = E_{bb} - E_{eb} + \frac{KT}{q}\ln\left(1+re^{\frac{q}{KT}(e_{b1}-E_{bb})}\right) \tag{5}$$

where E_{eb} is the offset voltage between base and emitter:

$$E_{eb} = \frac{KT}{q}\ln\left(1+m+\frac{I_{e'}}{a_{11}}\right) \tag{6}$$

$$I_e = I_{eo} + \frac{e_{b1}-E_{bb}}{R_e\left[1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}\right]} \approx I_{eo} \tag{7}$$

The last term in equation (7) represents the increase in the total current through R_e when r of the input transistors are turned on and the fixed bias transistor is cut off. In practical realizations of the circuit this term is small compared to the term I_{eo}.

The total currents in the two collectors are respectively:

$$i_{c1} = \sum_{r=1}^{m}\left[a_{21_r}\left(e^{\frac{q}{KT}(e_{br}-e_e)}-1\right) - a_{22_r}\left(e^{\frac{q}{KT}(e_{br}-e_{c1})}-1\right)\right] \tag{8}$$

and

$$i_c = a_{21}\left(e^{\frac{q}{KT}(E_{bb}-e_e)}-1\right) - a_{22}\left(e^{\frac{q}{KT}(E_{bb}-e_{c2})}-1\right) \tag{9}$$

Substituting for e_e from equation (5) and assuming, again, identical transistors:

$$i_{c1} = \frac{\alpha_f}{1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}} \times \left[I_{eo} + \frac{e_{b1}-E_{bb}}{R_e\left(1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}\right)}\right] - \frac{e_{b1}-e^s_{b1}}{R_{c1}+\frac{R_e}{\alpha_f}e^{\frac{q}{KT}(e^s_{b1}-e_{b1})}} \tag{10}$$

$$i_c = \frac{\alpha_f}{1+re^{\frac{q}{KT}(e_{b1}-E_{bb})}}\left[I_{eo}+\frac{e_{b1}-E_{bb}}{R_e\left(1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}\right)}\right] \tag{11}$$

The quantity e_{b1}^s represents the base voltage at which the input transistors go into saturation and is related to the other parameters of the circuits by the following relationship:

$$e_{b1}^s = \frac{E_{cc}+\alpha_f\frac{R_{c1}}{R_e}E_{eb}+\frac{KT}{q}\ln\frac{KT}{q}\frac{\alpha_f}{rR_e a_{22}}}{1+\alpha_f\frac{R_{c1}}{R_e}} \tag{12}$$

In terms of the collector currents, the collector voltages are given as:

$$e_{c1}=E_{cc}-i_{c1}R_{c1} \qquad e_{c2}=E_{cc}-i_c R_{c2} \tag{13}$$

and, since under D.C. conditions the emitter followers act only as D.C. level translators, the output from the emitter followers is related to the collector voltages of the gate by the following expression:

$$e_o=e_c-\frac{KT}{q}\ln\left(1+\frac{I_o}{a_{11}}\right)=e_c-E_T \tag{14}$$

where E_T represents the base emitter offset voltage and I_o the emitter current of the emitter followers.

Substituting for the collector currents from equations 10 and 11, we obtain the desired expressions for the output voltages:

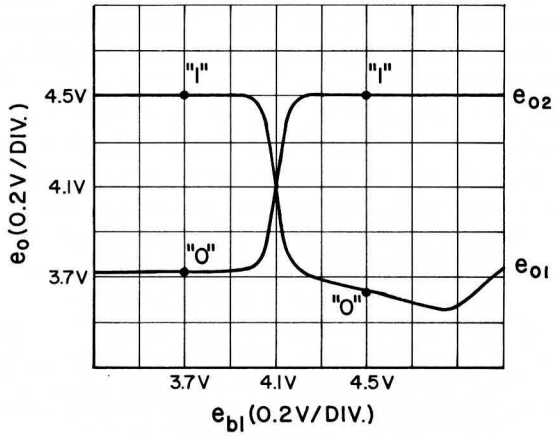
$$e_{o1}=E_{cc}-E_T-\frac{\alpha_f R_{c1}}{1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}}\times\left[I_{eo}+\frac{e_{b1}-E_{bb}}{R_e\left(1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}\right)}\right]+\frac{e_{b1}-e_{b1}^s}{1+\frac{R_e}{\alpha_f R_{c1}}e^{\frac{q}{KT}(e_{b1}^s-e_{b1})}} \tag{15}$$

$$e_{o2}=E_{cc}-E_T-\frac{\alpha_f R_{c2}}{1+re^{\frac{q}{KT}(e_{b1}-E_{bb})}}\times\left[I_{eo}+\frac{e_{b1}-E_{bb}}{R_e\left(1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}\right)}\right] \tag{16}$$

The above equations for e_{o1} and e_{o2} represent the non-linear relationship between output voltage and input voltage and will be referred to as the transfer characteristics of the gate. Figures 3a and 3b compare the theoretical transfer characteristics as computed from equations (15) and (16), with the experimentally obtained transfer characteristics using identical values of the parameters. It is seen that the experimental and theoretical transfer characteristics agree in every respect within less than 5%, and that the characteristics have a very narrow transition region. Defining the transition width as the change in base voltage necessary to make the collector voltage execute 10 - 90% of the logic swing, the expression for transition width becomes:

$$\Delta e=\frac{KT}{q}\ln 81\approx 4.4\frac{KT}{q} \tag{17}$$

INPUT-OUTPUT TRANSFER CHARACTERISTICS

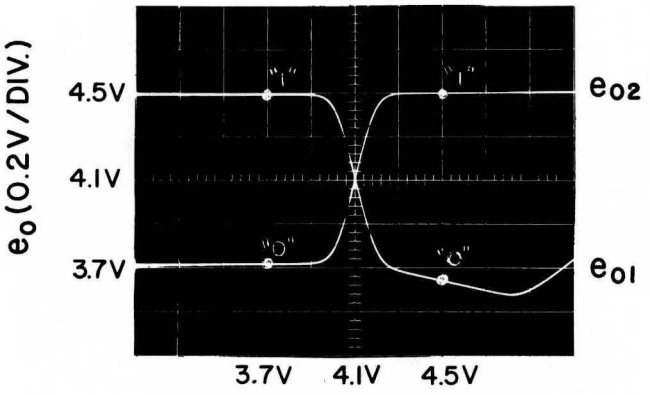


$$e_{o1}=E_{cc}-E_T-\frac{\alpha_f R_{c1}I_e}{1+e^{\frac{q}{KT}(e_b-e_{b1})}}+\frac{e_{b1}-e_{b1}^s}{1+\frac{R_e}{\alpha_f R_{c1}}e^{\frac{q}{KT}(e_{b1}^s-e_{b1})}}$$

$$e_{o2}=E_{cc}-E_T-\frac{\alpha_f R_{c2}I_e}{1+e^{\frac{q}{KT}(e_{b1}-e_b)}} \qquad I_e=I_{eo}+\frac{e_{b1}-e_b}{R_e\left[1+e^{\frac{q}{KT}(e_b-e_{b1})}\right]}$$

$e_b = E_{bb}$
$r = 1$

FIGURE 3-a



OBSERVED CHARACTERISTICS

FIGURE 3 (cont.)-b

It is a remarkable fact that the transition width is not dependent on any of the circuit characteristics but only upon two physical constants and upon the temperature. At room temperature, 25°C, the transition width computes out to about 115mV.

Since the output of a logic circuit must be compatible with its input, the transfer characteristic also determines the location of the operating points corresponding to logical zero's and one's. These points are indicated in Figure 3 showing that the logical one in this particular example corresponds to 4.5V and a logical zero to an output voltage of 3.7 volts. This means that the logic swing is about .8V, or about 7 times the transition width.

The transfer characteristic is also very useful in determining the noise immunity of the circuit. Defining the noise immunity as the ratio between the noise voltage that will just cause a logical one to be misinterpreted as a logical zero (or vice versa) and the logic swing, we see that the permissible noise voltage that can be applied to the gate is equal to the distance between the mid-point of the transfer characteristic and any of the operating points. The noise immunity may be expressed mathematically as:

$$N^0 = \frac{1}{2} - \frac{KT}{qe_1} \ln r \qquad N^1 = \frac{1}{2} + \frac{KT}{qe_1} \ln r \tag{18}$$

where N^0 and N^1 are the noise immunities when a logical zero and a logical one are applied to r of the inputs of the gate respectively and where e_1 is the logic swing. Since the operating points are nearly symmetrical with repect to the mid-point of the transfer characteristics, the noise immunity is approximately 400 mV or 50% of the logic swing.

TRANSFER CHARACTERISTICS AS A FUNCTION OF FAN-IN AND TEMPERATURE

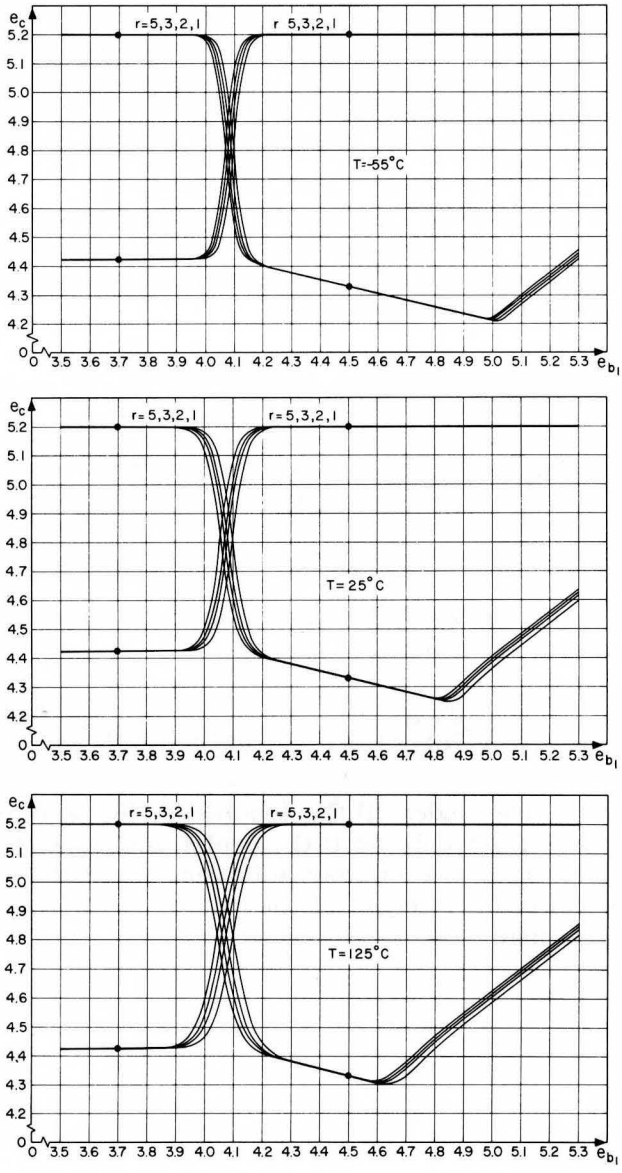


FIGURE 4-

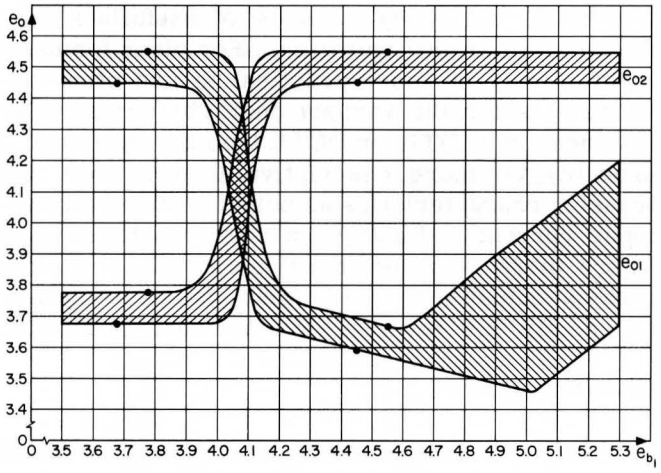
Finally, the transfer characteristic is a valuable tool for the purpose of determining "worst case" design. Figures 4a, 4b and 4c show how the transfer characteristics vary with fan-in at temperatures of -55°C, 25°C and 125°C. As expected from equation (17) the transition width of the characteristic widens as temperature is increased. Also, it should be noted that the crossover point between the OR and NOR characteristic moves to the left as fan-in is increased.

It is seen from equations (15) and (16) that the crossover point is given by:

$$e_{b1}^{0.5} = E_{bb} - \frac{KT}{q} \ln r \tag{19}$$

This shows that the horizontal movement of the crossover point varies logarithmically with fan-in.

Moreover, it should be noted that the logic swing remains independent of temperature changes since the logic swing is essentially only dependent on the ratio between the collector resistors and the common emitter resistance. In other words, to insure a certain nimimum logic swing, tolerances must be imposed only upon the ratio of the resistors and not upon their absolute values. In integrated circuits this is indeed very fortunate since diffused resistors cannot be made to a tolerance of better than ± 20% while ratios between resistors can be easily kept within 1%. Using the relationships of transfer characteristics with fan-in and temperature, as obtained from Figure 4, and also assuming certain tolerance limits on the offset voltage E_T and the power supply, the upper and lower limits for the transfer characteristics may be computed from equations 15 and 16. The result is shown in Figure 5, from which it can be seen that this essentially defines a band of transfer characteristics under all kinds of conditions. Operating points are also indicated on these curves from which "Worst Case" conditions can be determined.



TOLERANCE VARIATION of TRANSFER CHARACTERISTICS
FIGURE 5-

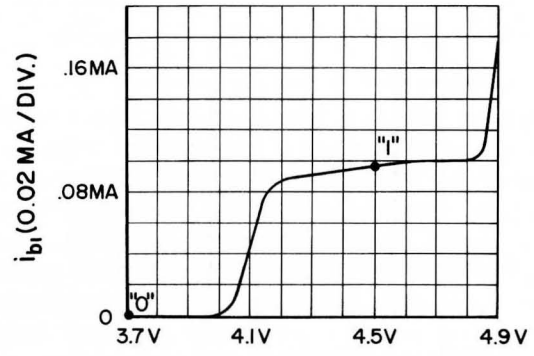
It is interesting to note that the part of the curve representing saturating conditions exhibits the widest variations which are, incidentally, mainly due to the temperature sensitivity of e_{b1}^s; that is, the point at which the circuit goes into saturation. However, since the circuit never becomes saturated, as indicated by the location of the operating points in Figure 5, the circuit operation is not affected by the large variation of the transfer characteristic in the saturation region.

An expression for the input characteristics of the gate (the non-linear equivalent of the linear Y_{11} parameter) may be derived in the same manner as the expressions for the transfer characteristics. The input characteristic is essentially a plot of base current versus base voltage and, as shown in Figure 6, good agreement between theoretical and experimental curves is achieved. It is seen that the small signal input resistance of the gate is nearly infinite near a logic zero; approximately 2.5K Ω in the transition region; and about 40K Ω at the logical one operating point. However, for practical purposes the average input resistance in going from a logical zero to a logical one is more useful than the various incremental resistances. From the expressions for the input characteristics it is easily shown that the average input resistance is:

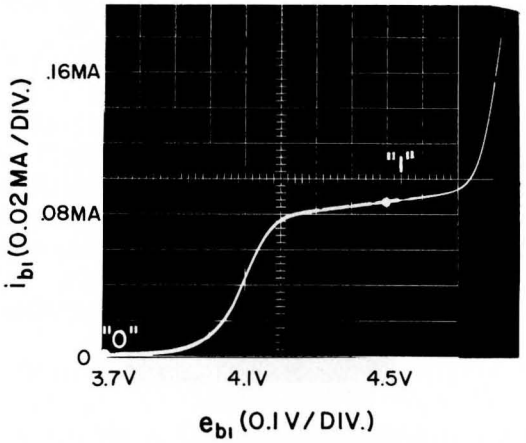
$$\bar{R}_i \approx \beta R_{c1} \qquad (20)$$

which, in this case, turns out to be about 10K. The initial assumption that r_b can be neglected, therefore, is justifiable.

INPUT CHARACTERISTICS



$$i_{b1} = \frac{I_e(1-\alpha_f)}{1+e^{\frac{q}{KT}(e_b-e_{b1})}} + \frac{1}{R_{C1}}\left[\frac{(e_{b1}-e_{b1}^s)(1-\alpha_i)}{1+\frac{R_e}{\alpha_f R_{C1}}e^{\frac{q}{KT}(e_{b1}^s-e_{b1})}}\right]$$



OBSERVED CHARACTERISTICS
FIGURE 6-

The output characteristic, which is the output current versus the output voltage, may easily be derived from the transistor model for the emitter followers. The expression for this characteristic is simply:

$$i_o = I_o e^{\frac{q}{KT}(e_c - e_o - E_T)} - \frac{e_o}{R_o} \qquad (21)$$

where E_T is the base-emitter off-set voltage for the emitter followers given by:

$$E_T = \frac{KT}{q} \ln \frac{I_o}{a_{11}} \qquad (22)$$

and where I_o is the current through the emitter follower with a logical zero output. This characteristic, representing the non-linear equivalent of the small signal parameter Y_{22}, is shown in Figure 7 together with its experimental counterpart.

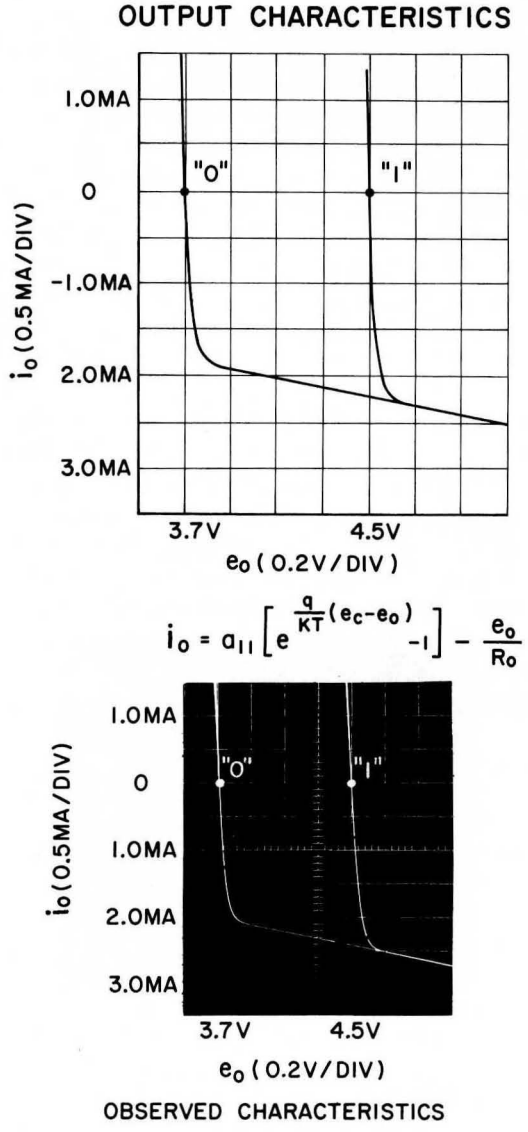


FIGURE 7-

Again, it should be observed that there is perfect agreement between theoretical and experimental characteristics. Together with the input characteristics, the output curves are useful in estimating loading effects and D.C. fan-out capability of the gates. Since the output impedance of the gate is on the order of 22 Ω, fan-outs up to 25 can be tolerated without excessive reduction in logic swing. In other words, the fan-out capability of this gate is limited by restrictions on transient response rather than D. C. considerations.

To complete the "black box" specifications of the gate one should also include the effect of output voltage upon the input voltage; that is, the inverse transfer characteristics. However, since this gate is for all practical purposes perfectly unilateral, these characteristics are identically equal to zero over the entire operating range.

In the example used here to demonstrate black box characterization of logic circuits, the input current-versus-input voltage has been selected for the input characteristics, the output voltage-versus-input voltage describes the transfer characteristics, and the output current-versus-output voltage describes the output characteristics. This choice was made solely by reasons of usefullness for this particular configuration. For other forms of logic it may be more practical to use other relationships for the various characteristics. For instance, in a DTL or DCTL type circuit it would probably be more descriptive to represent the transfer characteristics as output voltage-versus-input current. Finally, in logic configurations where there is a considerable amount of coupling between output and input, it may also be necessary to specify the inverse transfer characteristics.

Input Capacitance

In a logic circuit the input capacitance would also, in general, be a highly non-linear function of the input voltage. There are two reasons for this. The first and least significant reason is the fact that the junction capacitance in diodes and transistors is a function of the voltage across the junction; the usual relationship being that the capacitance is inversely proportional to between the 1/3 and 1/2 power of the junction voltage depending upon whether the junction is graded or is step-like in nature. However, the variation in capacitance due to this effect is usually small as the logic swing of the gate varies from a logical zero to a logical one. This variation may therefore be neglected without excessive error.

The predominant cause of variation in capacitance is the variation of incremental gain of the logic circuit as the circuit traverses from a logic zero

to a logical one. For example, in the MECL gate it is very easily shown that the input capacitance varies approximately with input voltage as follows:

$$C_{in} \approx \frac{C_e}{1+re^{\frac{q}{KT}(e_{b1}-E_{bb})}} + C_c\left[1+\frac{\frac{1}{r}\frac{qe_1}{KT}e^{\frac{q}{KT}(E_{bb}-e_{b1})}}{(1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})})^2}\right] \quad (23)$$

where C_e and C_c represent the depletion capacitances of the emitter and collector junctions respectively.

Figure 8 shows typical variation of input capacitance with input voltage, from which it can be seen that the input capacitance goes through a sharp peak as the input voltage traverses from a logical zero to a logical one.

INPUT CAPACITANCE vs INPUT VOLTAGE

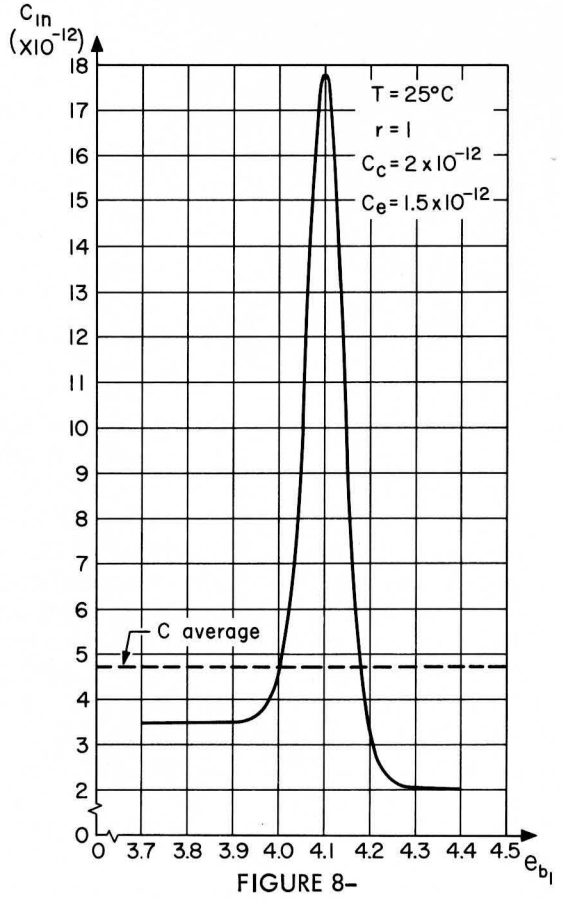


FIGURE 8-

In general it is very difficult to obtain a reasonable, simple and tractable analytical expression for the transient response of a logic gate when the exact behavior of capacitance is taken into account. One way to simplify this problem is to use the average value of the input capacitance as the input voltage traverses between a logical zero and a logical one, defined as follows:

$$\overline{C}_b = \frac{1}{e_{b1}^1 - e_{b1}^o}\int_{e_{b1}^o}^{e_{b1}^1}\left[\frac{d(e_{b1}-e_e)C_e(e_{b1}-e_e)}{de_{b1}} + \frac{d(e_{b1}-e_{c1})C_c(e_{b1}-e_{c1})}{de_{b1}}\right]de_{b1} \approx \frac{C_e}{2} + 2Cc \quad (24)$$

where e_{b1}^o and e_{b1}^1 refer to the magnitudes of the input voltage for a logical zero and one, respectively. This definition may, at first glance, seem somewhat arbitrary; however, there are two good reasons for this choice. First, it may be shown that the transient response of a circuit consisting of non-linear elements is not dependent upon detailed behavior of these non-linearities, but rather on the average value of the function over the entire operating range.[4] Second, the above definition is convenient because it represents the equivalent constant capacitance that accumulates same amount of charge as the non-linear capacitance when the gate traverses from a logical zero to a logical one. The average capacitance in this particular case is indicated by the dashed line in Figure 8.

Transient Response

The transient response of the gate, illustrated in Figure 2, is determined by the differential equations governing the charging and discharging of the input capacitance (or the so called base response), the equations governing the response of the collector voltage, and the effect of load capacity at the output terminals.

Base Response

If we adopt the idea of an average input capacitance and take into account the fact that the input resistance to the gate is very large, the equation

governing the base response is linear and of the first order. The solution to this equation is simply:

$$e_{b1}(t)=E_{bb}-\frac{e_1}{2}+e_1(1-e^{\frac{-t}{\tau_{b1}}}) \tag{25}$$

where e_1 represents the logic swing and where τ_{b1} is defined as:

$$\tau_{b1}=r_b\bar{C}_b=r_b(\bar{C}_{e1}+\bar{C}_{c1})\cong r_b\left(\frac{C_e}{2}+2C_c\right) \tag{26}$$

The delay and rise time associated with the base response is therefore;

$$T_D^b=0.7\,\tau_{b1} \tag{27}$$

and

$$T_R^b=2.2\tau_{b1} \tag{28}$$

Collector Response

Utilizing the equivalent circuit of the MECL gate shown in Figure 2b, it can be shown that the differential equation governing the transient response of the collector voltage on the Nor side is as follows:

$$\begin{aligned}&\tau_{21}\,\tau_{11}\,\tau_{c1}\frac{d^3e_{c1}}{dt^3}+\\&(\tau_{21}\,\tau_{11}+\tau_{21}\,\tau_{c1}+\tau_{11}\,\tau_{c1})\frac{d^2e_{c1}}{dt^2}+\\&(\tau_{21}+\tau_{11}+\tau_{c1})\frac{de_{c1}}{dt}+e_{c1}\\&=E_{cc}-\frac{\alpha_f I_{eo}R_{c1}}{1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}}+\\&\tau_{cb}\left[\tau_{21}\,\tau_{11}\frac{d^3e_{b1}}{dt^3}+(\tau_{21}+\tau_{11})\frac{d^2e_{b1}}{dt^2}+\frac{de_{b1}}{dt}\right]\end{aligned} \tag{29}$$

where we have simplified the expression for the transfer function to:

$$e_{c1}=E_{cc}-\frac{\alpha_f I_{eo}R_{c1}}{1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}}=E_{cc}-\frac{e_1}{1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}} \tag{30}$$

and where τ_{c1} and τ_{cb} are defined as:

$$\tau_{c1}=R_{c1}C_1=R_{c1}\left[r\bar{C}_{c1}+(m-r)\bar{C}_{cm}+C_{s1}\right] \tag{31}$$

$$\tau_{cb}=rR_{c1}\bar{C}_{c1} \tag{32}$$

C_{s1} being here the collector to substrate capacitance. Changing variables and by appropriate use of the convolution integral it is easily shown that the solution to this differential equation is:

$$\begin{aligned}e_{c1}(t)=&E_{cc}+\frac{\tau_{cb}}{\tau_{c1}-\tau_{b1}}\left(e^{\frac{-t}{\tau_{c1}}}-e^{\frac{-t}{\tau_{b1}}}\right)e_1\\&-\left\{\frac{\tau_{c1}^2e^{\frac{-t}{\tau_{c1}}}}{(\tau_{c1}-\tau_{11})(\tau_{c1}-\tau_{21})}\left[E_{cc}-e_{c1}(0)+\int_{E_{bb}-\frac{e_1}{2}}^{e_{b1}}\frac{de_{b1}}{\left[1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}\right]\left[\frac{1}{2}+\frac{E_{bb}-e_{b1}}{e_1}\right]^{1+\frac{\tau_{b1}}{\tau_{c1}}}}\right]\right.\\&\left.-\frac{\tau_{11}^2e^{\frac{-t}{\tau_{11}}}}{(\tau_{c1}-\tau_{11})(\tau_{11}-\tau_{21})}\left[E_{cc}-e_{c1}(0)+\int_{E_{bb}-\frac{e_1}{2}}^{e_{b1}}\frac{de_{b1}}{\left[1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}\right]\left[\frac{1}{2}+\frac{E_{bb}-e_{b1}}{e_1}\right]^{1+\frac{\tau_{b1}}{\tau_{11}}}}\right]\right\}\end{aligned} \tag{33}$$

(33) (cont.)

$$+\frac{\tau_{21}^2 e^{\frac{-t}{\tau_{21}}}}{(\tau_{c1}-\tau_{21})(\tau_{11}-\tau_{21})}\left[E_{cc}-e_{c1}(0)+\frac{\tau_{b1}}{\tau_{21}}\int_{E_{bb}-\frac{e_1}{2}}^{e_{b1}}\frac{de_{b1}}{\left[1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}\right]\left[\frac{1}{2}+\frac{E_{bb}-e_{b1}}{e_1}\right]^{1+\frac{\tau_{b1}}{\tau_{21}}}}\right]$$

where $e_{c1}(0)$ represents the initial value of the collector voltage and where it is assumed that the initial value of the first and second derivatives of the collector voltage are equal to "zero". In order to reduce the power consumed by a logic circuit the circuit should be designed such that it is circuit limited rather than device limited. In other words, one should select the time constant τ_{c1} considerably larger than τ_{11} and τ_{21}. Moreover, τ_{cb} is usually very small, so that the second term in the above equation may be neglected. Hence, the above equation simplifies to:

$$e_{c1}(t)=E_{cc}-e^{\frac{-t}{\tau_{c1}}}\left[E_{cc}-e_{c1}(0)+\frac{\tau_{b1}}{\tau_{c1}}\int_{E_{bb}-\frac{e_1}{2}}^{e_{b1}}\frac{de_{b1}}{\left[1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}\right]\left[\frac{1}{2}+\frac{E_{bb}-e_{b1}}{e_1}\right]^{1+\frac{\tau_{b1}}{\tau_{c1}}}}\right] \quad (34)$$

The expression for e_{c2} (t) may be derived in the same manner and the result is almost identical to that of e_{c1} (t).

Figure 9 shows the transient response of the normalized collector voltage as a function of normalized time for various values of the normalized logic swing of the driving gate $(\frac{qe_1^*}{KT})$. It is very interesting to observe that, as the logical swing is increased, the rise time of the gate decreases rapidly, approaching asymptotically the rise time of the step function response of an RC network with time constant τ_{c1}. This is a very desirable feature of this circuit since slow pulses appearing at its input terminals tend to be reshaped by the gate, and the need for extraneous shaping networks in the computer is eliminated. Another interesting feature that can be deduced from Figure 9 is the fact that below a certain critical value of the logic swing the rise time of the collector response is larger than the rise time of the signal applied to the base. On the other hand, if the logic swing is greater than this critical value, the rise time in the collector is less than that of the base. Thus, if the logic swing is less than this critical value, the rise time will continue to deteriorate if a signal is passed through a number of cascaded gates while above this critical value the signal becomes reshaped. The asymptotical value of the rise time, after a signal has passed through a large number of stages, is about equal to the step function response of the gates which may be therefore regarded as the typical rise time of the gates.

Finally, it should be noted that the delay time does not change appreciably with logic swing and is essentially equal to the sum of the base and collector delay times. The delay and rise times of the collector response may therefore be written as:

$$T_D^c = T_D^b + 0.7\ \tau_{c1} \quad (35)$$

$$T_R^c = 2.2\ \tau_{c1} \quad (36)$$

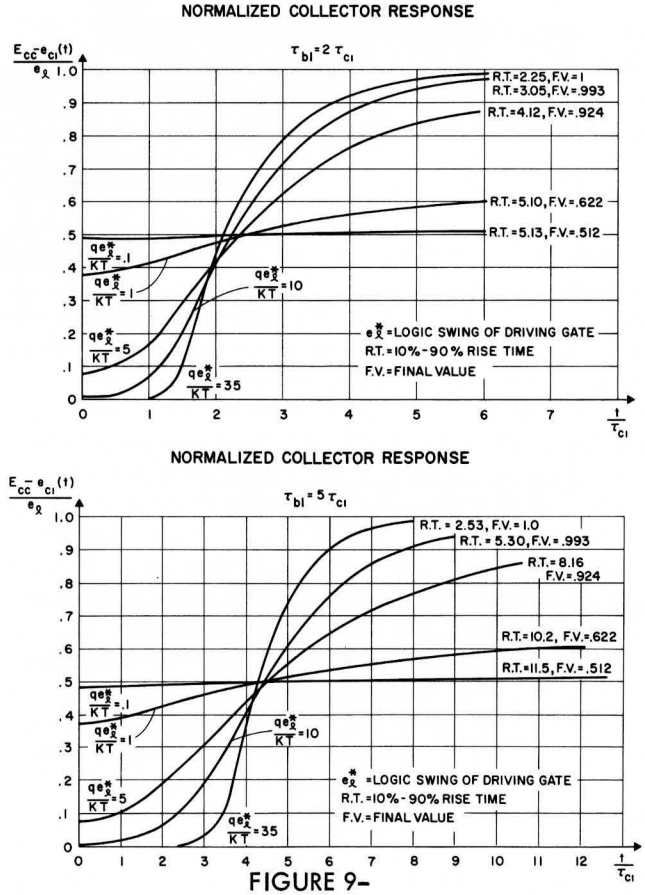


FIGURE 9-

Emitter Follower Response

By following essentially a procedure similar to that of the gate it is easily shown that the rise time, fall time, and delay time of the emitter followers are approximately given by:

$$T_R^e \approx \left[\frac{KT}{qI_o} + 2.2(1-\alpha_f)(r_b+R_c)\right] C_o \qquad (37)$$

and

$$T_F^e = \frac{R_o C_o}{\frac{E_{bb}+1}{e_1}\frac{}{2}} \qquad (38)$$

and

$$T_D^e \approx \left[\frac{KT}{2I_o q} + 0.7(1-\alpha_f)(r_b+R_{c1}) + \frac{R_o}{\frac{E_{bb}}{e_1}+\frac{1}{2}}\right] C_o \qquad (39)$$

where C_o represents the load capacitance. The total delay time, rise time and fall time of the gate may therefore be written as:

$$T_D = T_D^c + T_D^e \qquad (40)$$

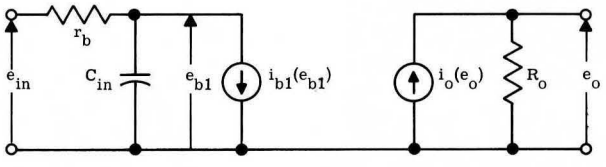
and

$$T_R = \sqrt{(T_R^g)^2 + (T_R^e)^2} \qquad (41)$$

and

$$T_F = \sqrt{(T_F^g)^2 + (T_F^e)^2} \qquad (42)$$

Based upon these results the black box equivalent circuit for the gate is as depicted in Figure 10.



$$i_{b1} = (1-\alpha_f)\frac{e^{\frac{q}{KT}(e_{b1}-E_{bb})}}{1+e^{\frac{q}{KT}(e_{b1}-E_{bb})}+(r-1)e^{\frac{q}{KT}(e_{b1}-E_{bb})}} I_e$$

$$C_{in} \approx \frac{C_e}{1+re^{\frac{q}{KT}(e_{b1}-E_{bb})}} + C_c\left[1+\alpha_f I_e R_{c1}\frac{\frac{q}{KT}\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}}{(1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})})^2}\right]$$

$$i_o(e_o) = I_o e^{\frac{q}{KT}(e_c-e_o-E_T)} - \frac{e_o}{R_o}$$

$$e_{c1}(t) = E_{cc} - e^{\frac{t}{\tau_{c1}}}\left[E_{cc}-e_{c1}(o)+\frac{\tau_{b1}}{\tau_{c1}}\int_{E_{bb}-\frac{e_1}{2}}^{e_{b1}}\frac{de_{b1}}{\left[1+\frac{1}{r}e^{\frac{q}{KT}(E_{bb}-e_{b1})}\right]\left[\frac{1}{2}+\frac{E_{bb}-e_{b1}}{e_1}\right]}\right]^{1+\frac{\tau_{b1}}{\tau_{c1}}}$$

$$e_{c2}(t) = E_{cc} - e^{\frac{-t}{\tau_{c2}}}\left[E_{cc}-e_{c2}(o)+\frac{\tau_{b1}}{\tau_{c2}}\int_{E_{bb}-\frac{e_1}{2}}^{e_{b1}}\frac{de_{b1}}{\left[1+re^{\frac{q}{KT}(e_{b1}-E_{bb})}\right]\left[\frac{1}{2}+\frac{E_{bb}-e_{b1}}{e_1}\right]}\right]^{1+\frac{\tau_{b1}}{\tau_{c2}}}$$

FIGURE 10-

Power-Time Relationship for the Collector Response

The power consumed by the gate, excluding the emitter followers is:

$$P = E_{cc}\frac{e_1}{R_{c1}} + \frac{E_{bb}e_1}{\beta R_{c1}} = \frac{e_1}{R_{c1}}\left[E_{bb} + E_{eb} + \frac{e_1}{2} + \frac{E_{bb}}{\beta}\right] \quad (43)$$

As mentioned earlier, there are two inherent quantities, - transition width and E_{eb} - in the expression for the transfer characteristics that are imposed upon us by "Mother Nature". Since these quantities vary with temperature, they may produce erroneous operation if the circuit is not designed properly. To minimize the effects of the variation of these two quantities and also to achieve a certain margin of safety in the circuit design, the logic swing should be selected much larger than the transition width, and the bias E_{bb} should be much larger than E_{eb}. This, necessarily, results in a higher power consumption. To reflect the compromise that must be made between power consumption and these safety margins, substitute:

$$\eta = \frac{e_1}{\Delta e} \quad , \quad \gamma = \frac{E_{bb}}{E_{eb}} \quad (44)$$

where η and γ represent the ratios between logic swing and transition width and E_{bb} to E_{eb} respectively. The expression for power then becomes:

$$P = \frac{\eta \Delta e}{R_{c1}}\left[(\gamma + 1)E_{eb} + \frac{\eta \Delta e}{2} + \frac{\gamma}{\beta}E_{eb}\right]$$

It is interesting to note here that the power goes up as the square of η and as the product of η and γ. Finally, substituting R_{c1} from the expression for the rise time and delay time of the collector response, we obtain:

$$P(T_D^c - T_D^b) = 0.7C_1\left[(\gamma+1)E_{eb} + \eta\frac{\Delta e}{2} + \frac{\gamma}{\beta}E_{eb}\right]\eta\Delta e \quad (46)$$

and

$$PT_R^c = 2.2C_1\left[(\gamma+1)E_{eb} + \eta\frac{\Delta e}{2} + \frac{\gamma}{\beta}E_{eb}\right]\eta\Delta e \quad (47)$$

In the design of a logic circuit this equation is extremely useful because it shows in one neat package the trade-off between power, speed, noise immunity and the amount of temperature independence desired. Also, it shows that power and time are related hyperbolically, a fact that has been known experimentally for a long time.

Computer Organization

Hardware realization of advanced computer system concepts involving, for example, multi-processing adaptive or learning organizations vastly increase the number of circuit elements required and are becoming more difficult to justify economically. This economic barrier is in part due to the continual application of the basic logic building block philosophy wherein utilization is made of soldered or welded assemblies of discrete active and passive components. Due to ever-increasing demands for reduction in size and increased performance, the simple double-sided printed circuit cards have been supplemented by a more complex arrangement of sub-modules usually consisting of one or more inter-connected logic circuits which are mounted and inter-connected with other sub-modules usually via a multi-layered printed circuit board.

The advent of integrated circuits, while compatatible with the present packaging state of the art, offers some significant additional advantages. The increased logic capability as required in the sub-modules can be achieved with a significant size reduction over the discrete circuit counterpart. In addition, the economics of building more logic complexity in one integrated circuit module is much more favorable. For example, the cost of building two discrete logic gates in one sub-module package would be approximately twice the component cost and somewhere between one and two times the assembly cost of a single gate. Factors determining the cost differential between an integrated dual gate and a single integrated gate at the present time are more complex. Manufacturing yield, the number of components, the amount of material used and the build-up of parameter tolerances as the logic complexity of the circuit increases all affect the final cost of the integrated circuit. While exact comparison figures are not available at the present time, it is estimated that the cost of an integrated circuit is quite competitive with discrete counterparts. As technology improves the governing cost factor will be based primarily on electrical specifications with logic complexity, number of components and the amount of material used playing a much less significant cost determining role.

Increasing the logic complexity of the basic sub-module usually minimizes the topological interconnection problem. The half adder function is a typical example of the maximum logic complexity presently available with integrated circuits. Within a year it is reasonable to predict technological advances wherein integrated logic complexity equivalent to one bit of a parallel adder can be economically built. The maximum future logic complexity will probably be determined primarily by tooling costs in addition to electrical specifications.

As the complexity of integrated logic circuits and machine organizations increase in the future, the need for the prevention of circuit failure in sensitive circuit arrangements either by use of redundancy or adaptive organizations will become a paramount factor in design.

In the area of memory it is anticipated that integrated circuit memory bits having identical transfer characteristics to that of the integrated logic portion of the computer will find wider application. Memory has been the main stumbling block in achieving the ultra-high performance capability of semiconductor logic circuits. A significant portion of this problem can be attributed to the interface circuitry which is necessitated when dissimilar device technlogies are employed in implementing the memory and the processing portion of a computer.

Higher order of complexity in integrated circuit memory systems, as typified by associative memory organizations, are forecast. In Figure 11 is shown a simplified logic block diagram of 4 bits of an associative memory system. This entire system can be implemented with the basic MECL half adder configuration; that is, by proper interconnections one half adder circuit implements either the register flip-flop, AND-OR gate clusters, storage elements, exclusive OR and the detector function. Since a single basic circuit is repeated in an array configuration over the face of a wafer of semiconductor material in the manufacturing process, small associative memory arrays appear to be feasible within the present state of the art. It also appears that with advanced photo mask techniques and device technologies, a larger practical sized memory array will become feasible.

With reference to Figure 11 it should be noted that in addition to the exclusive OR function, the AND and OR function is required for implementing the "read" operation. Also, each exclusive OR and AND-OR circuit has a memory register bit associated with it. Hence, we have between two memory words the required logic for performing binary addition. If a suitable compatible cross point switching arrangement can be devised, the logic power of memory could be increased; possibly to the point where memory and the processing section become inseparable.

Conclusions

This paper has attempted to point out a possible approach to the characterization and analysis of integrated logic circuits and to discuss some of the fundamental problems involved; however, since a specific example had to be resorted to in order to clarify some of the important aspects of such an analysis, and since special tricks in some of the approximations had to be used in order to achieve a solution, it is fairly evident that the analysis techniques available today are far from adequate. The field of non-linear circuit analysis is only in its infancy and much homework remains to be done in order to achieve general methods of attack for the analysis and synthesis of integrated switching circuits. As is often true in engineering, technology is presently far ahead of theory. However, only through a better understanding of the analysis of logic circuits can we expect to take full advantage of this new field of integrated circuits in the future.

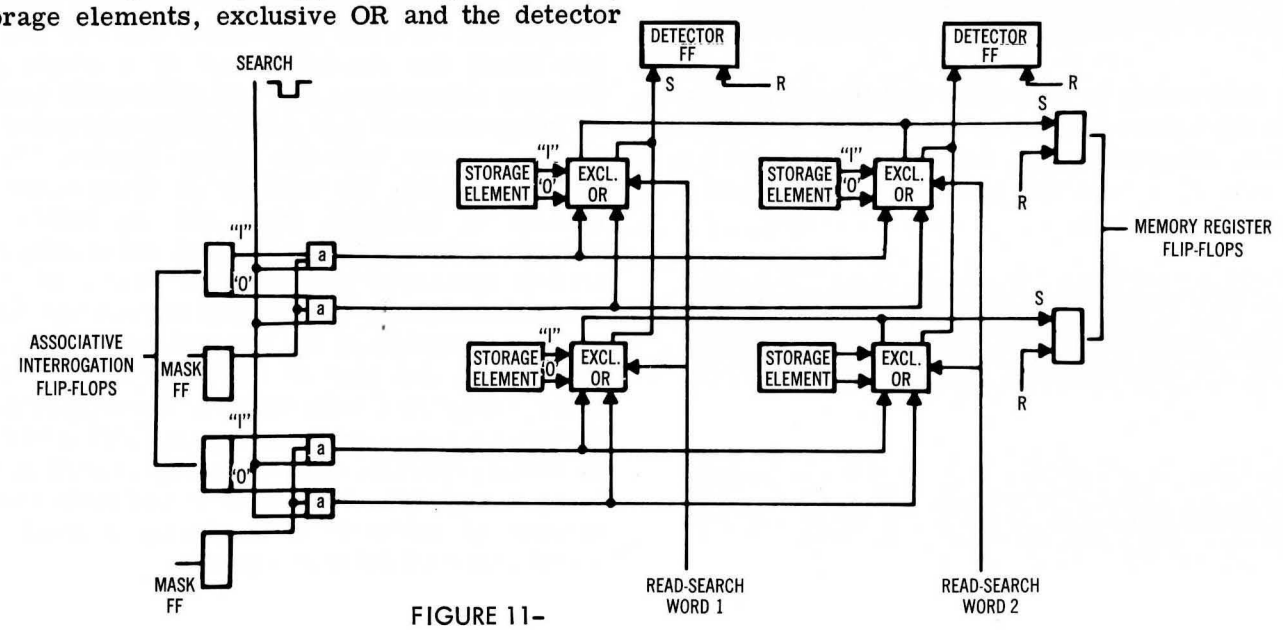


FIGURE 11-

Acknowledgments

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