MDTL

INTEGRATED CIRCUITS
MC930/MC830 SERIES

MDTL

INTEGRATED CIRCUITS

INDEX

NUMERICAL INDEX

(Functions and Characteristics)

V_{CC} = 5.0 Vdc, T_A = 25°C

Function	Type ① 0 to +75°C	Case	Type ① −55 to +125°C	Case	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Page No.
Expandable Dual 4-Input NAND Gate	MC830	83,93	MC930	83	8	30	22	5-12
Expandable Dual 3-2 Input NAND Gate	MC830	96A	MC930	96A	8	30	22	5-12
Clocked Flip-Flop	MC831	83,93,96A	MC931	83,96A	7	40	55	5-28
Expandable Dual 4-Input Buffer	MC832	83,93	MC932	83	25	35	85	5-24
Expandable Dual 3-2 Input Buffer	MC832	96A	MC932	96A	25	35	85	5-24
Dual 4-Input Expander	MC833	83,93	MC933	83	–	–	–	5-52
Dual 4-3 Input Expander	MC833	96A	MC933	96A	–	–	–	5-52
Hex Inverter	MC834	83,93	MC934	83	8	30	66	5-18
Hex Inverter	MC836	83,93	MC936	83	8	30	66	5-20
Hex Inverter	MC837	83,93	MC937	83	7	25	90	5-20
Decade Counter	MC838	83,93	MC938	83	8	30 MHz ③	150	5-44
Divide-by-Sixteen Counter	MC839	83,93	MC939	83	8	30 MHz ③	150	5-48
4-Input AND Driver with NOR Strobe	MC843	96A	MC943	96A	250 mA	80	50	5-26
Expandable Dual 4-Input Power Gate	MC844	83,93	MC944	83	27	30	65	5-22
Expandable Dual 3-2 Input Power Gate	MC844	96A	MC944	96A	27	30	65	5-22
Clocked Flip-Flop	MC845	83,93,96A	MC945	83,96A	12/10 ②	40	60	5-31
Quad 2-Input NAND Gate	MC846	83,93	MC946	83	8	30	44	5-16
Quad Inverter	MC846	96A	MC946	96A	8	30	44	5-16
Clocked Flip-Flop	MC848	83,93,96A	MC948	83,96A	11/9 ②	40	70	5-31
Quad 2-Input NAND Gate (2 kΩ pullup resistor)	MC849	83,93	MC949	83	7	25	66	5-16
Quad Inverter (2 kΩ pullup resistor)	MC849	96A	MC949	96A	7	25	60	5-16
Pulse Triggered Binary	MC850	83,93,96A	MC950	83,96A	10/8 ②	15	50	5-39
Monostable Multivibrator	MC851	83,93,96A	MC951	83,96A	10	40	30	5-42
Dual J-K Flip-Flop (common clock and C_D, separate S_D)	MC852	83,93	MC952	83	12/10 ②	40	120	5-34
Dual J-K Flip-Flop (separate clock and S_D, no C_D)	MC853	83,93	MC953	83	12/10 ②	40	120	5-34
Dual J-K Flip-Flop (common clock and C_D, separate S_D, 2 kΩ pullup resistor)	MC855	83,93	MC955	83	11/9 ②	40	140	5-34
Dual J-K Flip-Flop (separate clock and S_D, no C_D, 2 kΩ pullup resistor)	MC856	83,93	MC956	83	11/9 ②	40	140	5-34
Expandable Dual 4-Input NAND Gate (2 k pullup resistor)	MC861	83,93	MC961	83	7	25	33	5-12
Expandable Dual 3-2 Input NAND Gate (2 k pullup resistor)	MC861	96A	MC961	96A	7	25	33	5-12
Triple 3-Input NAND Gate	MC862	83,93	MC962	83	8	30	33	5-14
Dual 2-Input NAND Gate plus Inverter	MC862	96A	MC962	96A	8	30	30	5-14
Triple 3-Input NAND Gate (2 kΩ pullup resistor)	MC863	83,93	MC963	83	7	25	50	5-14
Dual 2-Input NAND Gate plus Inverter (2 kΩ pullup resistor)	MC863	96A	MC963	96A	7	25	45	5-14

① G suffix denoted Metal Can, F suffix denotes Flat Package, P suffix denotes Plastic Package. (i.e., MC830G = Metal Can, MC830F = Flat Package, MC830 P = Plastic Package)

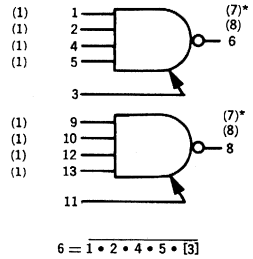
② Fan-out for MC830 series type / Fan-out for MC930 series type.

③ Maximum Counting Frequency

Numbers at ends of terminals represent pin numbers. Numbers in parenthesis indicate loading.
"G" Package: V_{CC} = pin 10, Gnd = pin 5 unless otherwise noted.
"F" and "P" Packages: V_{CC} = pin 14, Gnd = pin 7 unless otherwise noted.

GATES

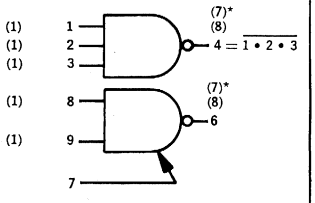
MC830F, MC830P, MC930F MC861F, MC861P, MC961F Expandable Dual 4-Input Gate



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

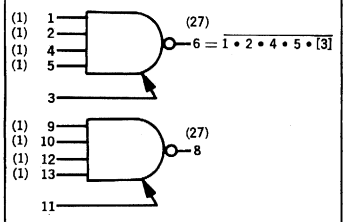
*APPLIES TO MC861F, MC861P, MC961F

MC830G, MC930G MC861G, MC961G Expandable Dual 3-2 Input Gate

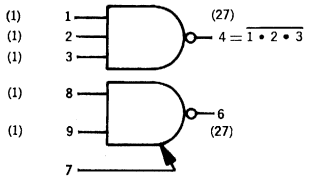


*APPLIES TO MC861G, MC961G

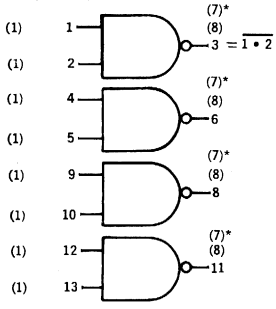
MC844F, MC844P, MC944F Expandable Dual 4-Input Power Gate



MC844G, MC944G Expandable Dual 3-2 Input Power Gate

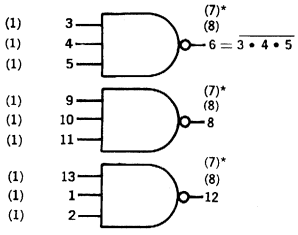


MC846F, MC846P, MC946F MC849F, MC849P, MC949F Quad 2-Input Gate



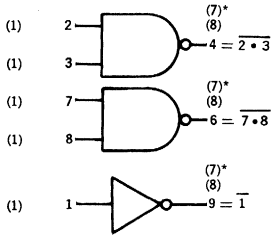
*APPLIES TO MC849F, MC849P, MC949F

MC862F, MC862P, MC962F MC863F, MC863P, MC963F Triple 3-Input Gate



*APPLIES TO MC863F, MC863P, MC963F

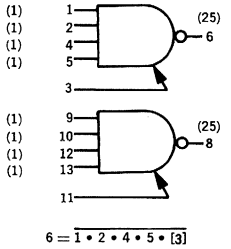
MC862G, MC962G MC863G, MC963G Dual 2-Input Gate Plus Inverter



*APPLIES TO MC863G, MC963G

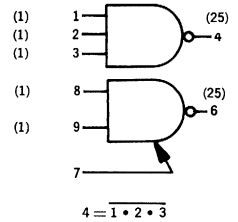
BUFFERS

MC832F, MC832P, MC932F Expandable Dual 4-Input Buffer



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

MC832G, MC932G Expandable Dual 3-2 Input Buffer

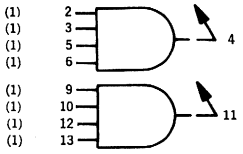


$4 = \overline{1 \cdot 2 \cdot 3}$

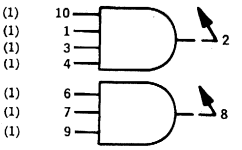
LOADING DIAGRAMS (continued)

EXPANDERS

MC833F, MC833P, MC933F
Dual 4-Input Expander

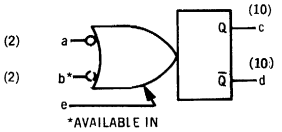


MC833G, MC933G
Dual 4-3 Input Expander



MULTIVIBRATOR

MC851F, MC851G, MC851P
MC951F, MC951G
Monostable Multivibrator



*AVAILABLE IN
"F" & "P" Pkgs. ONLY

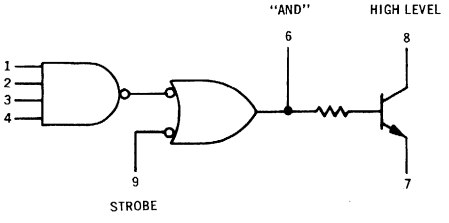
"F" & "P" Pkgs.: Vcc = pin 14, Gnd = pin 7
"G" Pkg.: Vcc = pin 6, Gnd = pin 1

Pin Connections

Letter	a	b	c	d	e
"F" & "P" Pkgs.	3	4	6	1	2
"G" Pkg.	9	—	10	7	8

DRIVERS

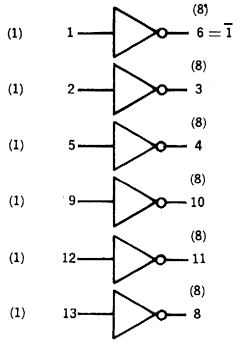
MC843G, MC943G
4-Input AND Driver with NOR Strobe



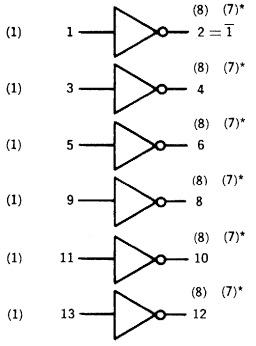
$\overline{8} = 1 \cdot 2 \cdot 3 \cdot 4 + \overline{9}$

INVERTERS

MC834F, MC834P, MC934F
Hex Inverter

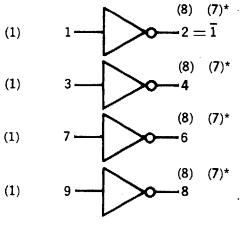


MC836F, MC836P, MC936F
MC837F, MC837P, MC937F
Hex Inverter



*APPLIES TO MC837F, MC837P, MC937F

MC846G, MC946G
MC849G, MC949G
Quad Inverter



*APPLIES TO MC849G, MC949G

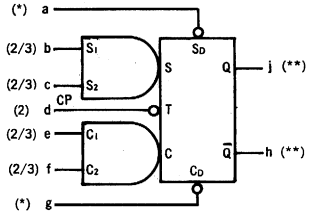
FLIP-FLOPS

MC831F, MC831G, MC831P
MC931F, MC931G

MC845F, MC845G, MC845P
MC945F, MC945G

MC848F, MC848G, MC848P
MC948F, MC948G

Clocked Flip-Flop



*SD and CD loading factor: ¾ for MC831/MC931 types
2 for other clocked flip-flops

**Q and Q̄ loading factor: 7 for MC831/MC931 types
12 for MC845 types
10 for MC945 types
11 for MC848 types
9 for MC948 types

Pin Connections

Letter	a	b	c	d	e	f	g	h	j
"F" & "P" Pkgs.	10	3	4	2	12	11	5	9	6
"G" Pkg.	7	2	3	1	9	8	—	6	4

SYNCHRONOUS TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

0 — Low State (more negative)
1 — High State (more positive)
X — State of the input does not affect the state of the circuit.
U — Indeterminate State

J-K TRUTH TABLE
(Connect S_2 to $\bar{Q}$, C_2 to Q)

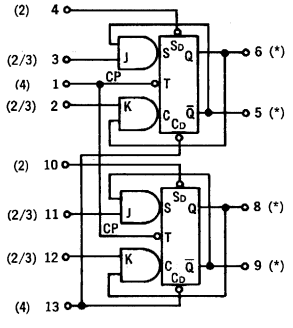
t_n		t_{n+1}
S_1	C_1	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

ASYNCHRONOUS TRUTH TABLE

S_D	C_D	Q	$\bar{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs.

MC852F, MC852P, MC952F
MC855F, MC855P, MC955F
Dual J-K Flip-Flop



*Q and Q̄ loading factor:

12 — MC852
10 — MC952
11 — MC855
9 — MC955

ASYNCHRONOUS TRUTH TABLE
MC952/MC852 and MC955/MC855

S_D	C_D	Q	$\bar{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

ASYNCHRONOUS TRUTH TABLE
MC953/MC853 and MC956/MC856

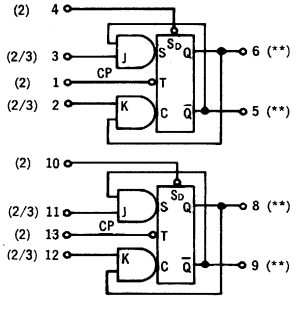
S_D	Q	$\bar{Q}$
1	NC	NC
0	1	0

J-K TRUTH TABLE
All Types

t_n		t_{n+1}
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs: they are independent of all other inputs.

MC853F, MC853P, MC953F
MC856F, MC856P, MC956F
Dual J-K Flip-Flop



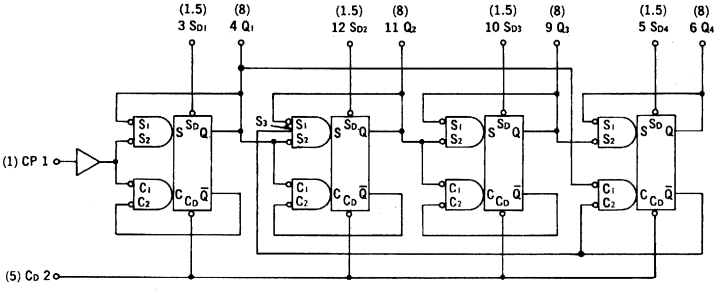
**Q and Q̄ loading factor:

12 — MC853
10 — MC953
11 — MC856
9 — MC956

LOADING DIAGRAMS (continued)

COUNTERS

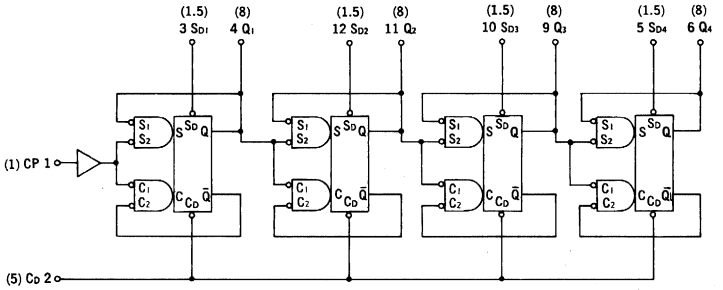
MC838F, MC838P, MC938F
Decade Counter



DECODING LOGIC

0	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
1	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
2	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	
3	Q_1	Q_2	$\bar{Q}_3$	
4	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	
5	Q_1	$\bar{Q}_2$	Q_3	
6	$\bar{Q}_1$	Q_2	Q_3	
7	Q_1	Q_2	Q_3	
8	$\bar{Q}_1$	Q_4		
9	Q_1	Q_4		

MC839F, MC839P, MC939F
Divide-by-Sixteen Counter

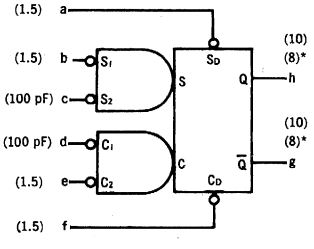


DECODING LOGIC

0	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
1	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
2	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	$\bar{Q}_4$
3	Q_1	Q_2	$\bar{Q}_3$	$\bar{Q}_4$
4	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	$\bar{Q}_4$
5	Q_1	$\bar{Q}_2$	Q_3	$\bar{Q}_4$
6	$\bar{Q}_1$	Q_2	Q_3	$\bar{Q}_4$
7	Q_1	Q_2	Q_3	$\bar{Q}_4$
8	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	Q_4
9	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	Q_4
10	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	Q_4
11	Q_1	Q_2	$\bar{Q}_3$	Q_4
12	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	Q_4
13	Q_1	$\bar{Q}_2$	Q_3	Q_4
14	$\bar{Q}_1$	Q_2	Q_3	Q_4
15	Q_1	Q_2	Q_3	Q_4

PULSE TRIGGERED BINARY

MC850F, MC850G, MC850P, MC950F, MC950G
Pulse Triggered Binary



* APPLIES TO MC950F, MC950G

SYNCHRONOUS TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	0	0	0	U
1	X	1	X	Q_n
X	1	X	1	Q_n
0	1	1	0	Q_n
0	0	X	1	1
0	0	1	X	1
1	X	0	0	0
X	1	0	0	0

ASYNCHRONOUS TRUTH TABLE

S_D	C_D	Q	$\bar{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

SINGLE TRIGGER TRUTH TABLE
(Pins S_2 and C_1 tied together)

t_n		t_{n+1}
S_1	C_2	Q
0	0	U
1	0	0
0	1	1
1	1	Q_n

0 = low state (more negative) 1 = high state (more positive)

X = don't care U = indeterminate state NC = no change

Pin Connections

Letter	a	b	c	d	e	f	g	h
"F" & "P" Pkgs.	13	4	5	6	10	1	11	3
"G" Pkg.	9	3	4	5	7	1	8	2

MDTL

GENERAL INFORMATION SECTION

INTRODUCTION

The MDTL line of diode transistor logic is a general purpose logic family offering moderate speed, good noise immunity, low noise generation, a high degree of logic flexibility, and economy.

GATE FUNCTIONS

The MDTL family offers positive-logic NAND gates with the capability of tying together the outputs of two or more elements. This not only allows greater logic flexibility, but also reduces required inventory stocking levels since AND-OR-INVERT functions (Wired OR) are readily obtained without special gates.

Buffer elements and power gates are available for driving large capacitive loads and/or where fan-out requirements are high. The buffer has an active pullup configuration, therefore the AND-OR-INVERT function can not be implemented with the buffer. Outputs of two or more buffer elements (or multiple buffer and power gate arrays) may be paralleled to achieve higher fan-out providing the inputs are also paralleled.

PROPAGATION DELAY

The typical propagation delay through an MDTL gate is 30 ns with nominal loading, providing the gate utilizes 6.0 k ohm pullup resistors. (Gates with 2.0 k ohm pullup resistors, approximately 25% faster, are also available.) The propagation delay is asymmetrical; t_{pd+} (propagation delay with the output transistor turning off) is normally double the value of t_{pd-} (propagation delay with the output transistor turning on). It will also be found that the value of t_{pd-} is affected very little by output loading, while t_{pd+} is quite dependent on the capacitive load seen by the output.

FLIP-FLOP OPERATING CHARACTERISTICS

There are two generic types of flip-flops within the MDTL family- - an ac binary and master-slave configuration. The ac binary is useful in high-speed systems (it will toggle at a rate typically greater than 40 MHz) and is also useful in control sections where its unique truth table is often advantageous.

FLIP-FLOP TRUTH TABLES

The synchronous truth tables, specified for the single clocked flip-flops (MC931/831, MC945/845, MC948/848) and the dual J-K flip-flops, relate the state the output will attain after a negative transition of the toggle input to the state of the output and the steering inputs (J-K or S-C) during the period when the toggle input is high. The complete truth table is valid only when the steering inputs are not allowed to change while the toggle input is high.

For applications which require changing the steering inputs while the clock input is high, a determination of the divergence from the truth table may be obtained from Figure 1. Note that the first four states do not affect the master section while the remaining five may. A general rule for this type of flip-flop (MC931/831, MC945/845, MC948/848 operated in the synchronous R-S mode) is that if one or more conditions that affect the master section are present while the clock is high, the flip-flop will respond to the last condition present prior to the negative transition of the clock.

Figure 2 shows a next-state table for J-K flip-flops, useful in determining the response of J-K flip-flops to a negative clock transition under conditions that involve changing the steering inputs while the clock input is high. Simply stated, satisfying either of the last two conditions in the table at any time while the clock input is high will cause the flip-flop to toggle when the clock goes low. The above discussion and next-state table apply to the MC931/831, MC945/845, and MC948/848 when operated in the J-K mode as well as to the dual J-K devices in the MDTL family.

FIGURE 1 – SINGLE CLOCKED FLIP-FLOP TRUTH TABLE

t_n				t_{n+1}	
S_1	S_2	C_1	C_2	Q	
0	x	0	x	Q_n	These Conditions Have No Effect On Master Section
0	x	x	0	Q_n	
x	0	0	x	Q_n	
x	0	x	0	Q_n	
0	x	1	1	0	These Conditions May Affect The Master Section
x	0	1	1	0	
1	1	0	x	1	
1	1	x	0	1	
1	1	1	1	U	

0 – Low State (more negative)
1 – High State (more positive)
x – State of the input does not affect the state of the circuit.
U – Indeterminate State

FIGURE 2 – J-K NEXT-STATE TABLE

J	K	Q_n	Q_{n+1}
0	x	0	Q_n
x	0	1	Q_n
1	x	0	$\overline{Q}_n$
x	1	1	$\overline{Q}_n$

POWER SUPPLY REQUIREMENTS

Normal operating voltage for the MDTL series is 5.0 volts ±10%. Typical power dissipation is given for each circuit, assuming a supply voltage of 5.0 volts. Also specified is a maximum worst-case current drain at the operating voltage. It should be noted that the specification of maximum current at 8.0 volt supply is primarily to guarantee reliability of the product under adverse conditions. It is not meant to infer that 8.0 volts is a normal operating condition.

Since power dissipation of an MDTL gate or flip-flop changes little with changes in the output state, bypassing of the power supply leads is not critical; however, a 1.0 μF capacitor where the supply connections enter the board is recommended. This is generally sufficient if the system is composed of gates and flip-flops with passive pullup elements, but smaller capacitors (approximately 0.01 μF) should be distributed on the board with a ratio of one capacitor for each eight packages if the board has a high density of circuits with active pullup elements (i.e., buffers, ac-coupled binaries, decade counters, etc.). It is also advisable to bypass the supply with a single 0.01 μF capacitor in close proximity to any MC951/851 used in the system.

MAXIMUM RATINGS

Characteristic	Rating	Unit
Supply Voltage — Continuous Pulsed, < 1 second	8.0 12	Vdc
Output Current (into outputs) — MC932/832, MC944/844 — Continuous Pulsed, < 30 ms MC951/851, MC950/850 — Continuous MC950/850 — Pulsed, < 30 ms All other types	 150 300 50 100 30	mAdc
Input Forward Current	−10	mAdc
Input Reverse Current — MC932/832, MC944/844, MC950/850 All other types	 5.0 1.0	mAdc
Operating Temperature Range — MC930 Series MC830 Series	 −55 to +125 0 to + 75	°C
Storage Temperature Range — Metal Can and Flat Package Plastic Package	 −65 to +150 −55 to +125	°C

GENERAL RULES

- The number of load circuits that may be driven from an output is determinated by the input loading factor. The summation of input loading should not exceed the drive capability of the output.
- With the exception of the buffer elements, the outputs of all MDTL gates and inverters may be tied together to form the Wired-OR function. For each added gate which has a 6 k ohm pullup resistor, subtract 0.83 unit load. The addition of a gate with a 2 k ohm pullup resistor reduces the available fan-out by 2.5 unit loads. No reduction in fan-out is required when wiring collectors of gates or inverters which have no internal pullup resistor.
- The outputs of the Dual Buffer may not be tied together.
- The outputs of the Dual Power Gate may be tied together to perform the Wired-OR function.
- An external load resistor should be utilized with the Dual Power Gate. At V_{CC} = 5.0 ± 0.5 V, subtract the following output loads:

  R
  2kΩ — 2 loads
  1kΩ — 4 loads
  510Ω — 8 loads

- For increased current capability, the inputs and outputs of ½ MC932 and ½ MC944 can be paralleled (up to and including 4 common outputs). The combined output will equal 100 loads while each combined input will equal 4 loads.

DEFINITIONS

C_P Clock pulse

f_C Counting frequency

I_{CE} Test current for measuring LV_{CE}

I_{CEX} Collector-to-emitter leakage of the output transistor

I_F Forward current of input diodes for unit input load. Also shown are 0.5 I_F, 2/3 I_F, 2 I_F, etc., which indicate input loading factor times I_F.

I_2, I_{12} Forward current of pins 2 and 12 of the pulse triggered binary

I_9 Forward current of pin 9 of the monostable multivibrator

I_{FCP} Forward current of clock input diodes. Shown as 2 I_{FCP} for inputs with loading factor of 2.

I_{FD} Forward current of dual expander diodes

I_{FS} Forward current of SET and CLEAR input diodes. Shown as 2 I_{FS} for inputs with loading factor of 2.

I_{max} Maximum rated power supply current with V_{max} applied

I_{OH} Output high current

I_{OL} Output low current

I_{OLB} Output low current of buffer stage of 4-Input AND Driver

I_{PDH} Power supply drain with the inputs high

I_{PDL} Power supply drain with the inputs low

I_R Reverse current of input diodes with V_R applied. Also shown are 2 I_R, 4 I_R, 5 I_R, etc., which indicate input loading factor times I_R.

I_{RCP} Reverse current of clock input diodes. Shown as 2 I_{RCP} for inputs with loading factor of 2.

I_{SC} Short circuit current obtained from device output when one or more inputs are low

LV_{CE} Output latch voltage

PW Pulse Width

t_f Fall time

t_r Rise time

t_{pd+} Propagation delay time with the output transistor turning off

t_{pd-} Propagation delay time with the output transistor turning on

TP_{in} Test point at input of unit under test

TP_{out} Test point at output of unit under test

V_{CC} Power supply voltage

V_{CCH} High power supply voltage

V_{CCL} Low power supply voltage

V_{CEX} Output transistor collector-to-emitter voltage

V_{CPTH} Clock threshold voltage

V_F Forward voltage test condition when testing forward current of input diodes

V_{FD} Forward voltage drop limit for expander diodes

V_{IH} Voltage for high input voltage state

V_{IL} Voltage for low input voltage state

V_{max} Maximum rated power supply voltage (V_{CC})

V_{OH} Output high voltage with I_{OH} flowing out of pin

V_{OHB} Output high voltage of buffer stage of 4-Input AND Driver

V_{OL} Output low voltage with I_{OL} flowing into pin

V_{OLB} Output low voltage of buffer stage of 4-Input AND Driver

V_{OX} Output voltage test condition when testing I_{CEX} for 4-Input AND Driver

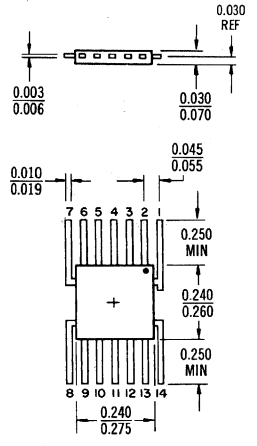
V_R Reverse voltage for input diode leakage test

V_X Low voltage utilized in testing expander inputs

PACKAGING

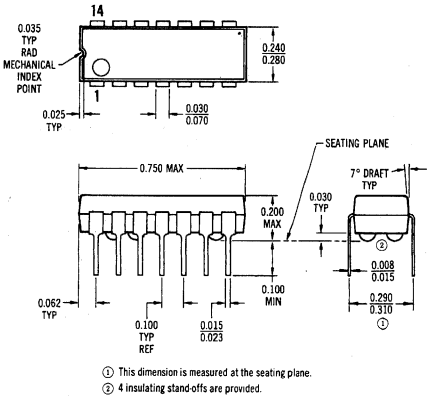
Devices with "F" suffix to the type number are in the TO-86 flat package (case 83); those with "G" suffix are in the TO-100 metal can (case 96A); those with "P" suffix are in the dual in-line plastic package (case 93).

CASE 83 (TO-86)

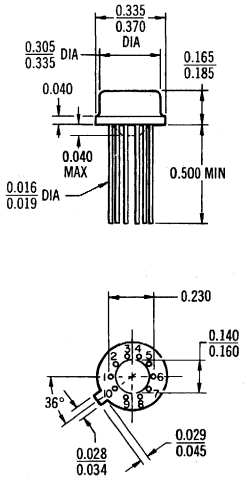


Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

CASE 93 (TO-116)



CASE 96A (TO-100)



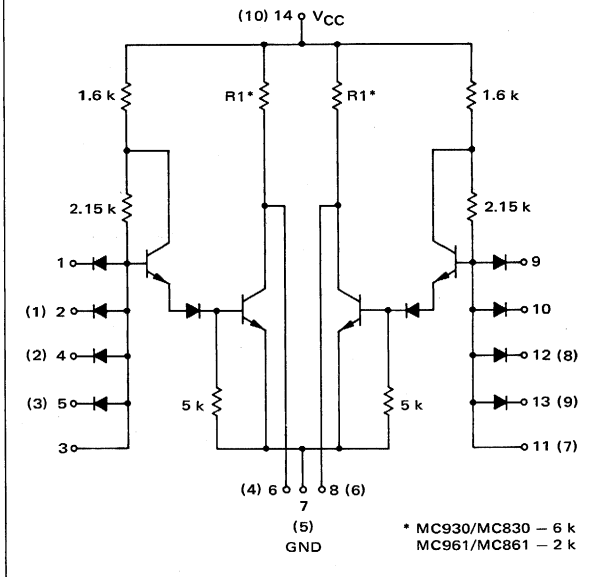
EXPANDABLE DUAL 4-INPUT GATES

MC930F · MC830F, P
MC961F · MC861F, P

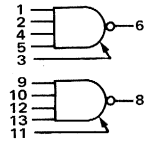
EXPANDABLE DUAL 3-2 INPUT GATES

MC930G · MC830G
MC961G · MC861G

This gate element, in the 14-pin flat and dual in-line packages, consists of two expandable 4-input NAND gate circuits. Since the metal can (G suffix) has only 10 pins, that circuit consists of one 3-input and one 2-input expandable gate. The elements may be cross-coupled to form a bistable multivibrator, or the outputs may be connected in parallel to perform the logic "OR" function.



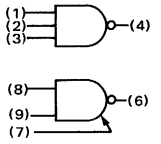
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC930F/MC830F, P
MC961F/MC861F, P

Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

Negative Logic: $6 = \overline{1 + 2 + 4 + 5 + [3]}$



MC930G/MC830G
MC961G/MC861G

Positive Logic: $4 = \overline{1 \cdot 2 \cdot 3}$

Negative Logic: $4 = \overline{1 + 2 + 3}$

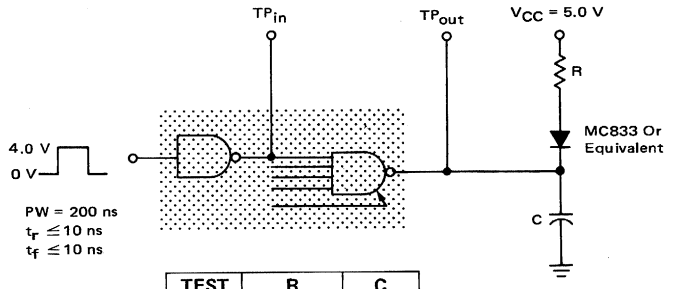
Input Loading Factor = 1

Output Loading Factor:
MC930/MC830 = 8
MC961/MC861 = 7

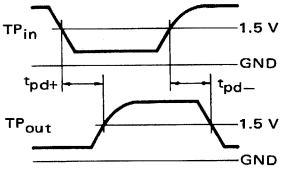
Total Power Dissipation:
MC930/MC830 = 22 mW typ/pkg
MC961/MC861 = 33 mW typ/pkg

Propagation Delay Time
MC930/MC830 = 30 ns typ
MC961/MC861 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

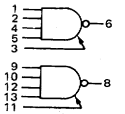


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER													
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	–	1	–	2	3	4	5	6	–	–	7	8	9	10



	@ Test Temperature	I_{OL} mA MC930	I_{OL} mA MC961	I_{OH} mA MC930	I_{OH} mA MC961	V_{IL} Volts	V_{IH} Volts	V_X Volts	V_F Volts	V_R Volts	V_{CEX} Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts	V_{max} Volts
MC930, MC961	−55°C	11.4	10.4	-0.12	-0.5	1.40	2.10	-	0	4.00	-	-	4.50	5.50	-
	+25°C	12.0	11.0	-0.12	-0.5	1.10	2.00	1.80	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	10.8	9.8	-0.12	-0.5	0.80	2.00	-	0	4.00	-	-	4.50	5.50	-
		MC830	MC861	MC830	MC861										
MC830, MC861	0°C	12.0	11.0	-0.12	-0.5	1.20	2.00	-	0.45	4.00	-	-	5.00	5.00	-
	+25°C	12.0	11.0	-0.12	-0.5	1.10	1.90	1.80	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	11.4	10.4	-0.12	-0.5	0.95	1.80	-	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC930, MC961 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC830, MC861 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_X	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	1,2,4,5	-	-	-	-	-	14	-	-	7
	V_{OH}	6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	1	-	-	-	-	-	-		-	-	
				-		-		-			-		-		-		-		2	-	-	-	-	-	-		-	-	
				-		-		-			-		-		-		-		4	-	-	-	-	-	-		-	-	
				-		-		-			-		-		-		-		5	-	-	-	-	-	-		-	-	
				-		-		-			-		-		-		-		-	-	3	-	-	-	-		-	-	
Short-Circuit Current MC930/MC830	I_{SC}	6	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	1,6,7
MC961/MC861		6	-	-4.00	-	-4.00	-	-3.90	mAdc	-	-3.90	-	-3.90	-	-3.75	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	1,6,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	-	1	-	-	-	14	-	2,4,5,7
		2	-		-		-			-		-		-			-	-	-	-	-	-	2	-	-	-		-	1,4,5,7
		4	-		-		-			-		-		-			-	-	-	-	-	-	4	-	-	-		-	1,2,5,7
		5	-		-		-			-		-		-			-	-	-	-	-	-	5	-	-	-		-	1,2,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	-	6,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	-	-	1	2,4,5	-	-	14	-	7
		2	-		-		-			-		-		-			-	-	-	-	-	-	2	1,4,5	-	-		-	
		4	-		-		-			-		-		-			-	-	-	-	-	-	4	1,2,5	-	-		-	
		5	-		-		-			-		-		-			-	-	-	-	-	-	5	1,2,4	-	-		-	
Power Drain Current (Total Device) MC930/MC830	I_{PDH}	14	-	-	-	6.5	-	-	mAdc	-	-	-	8.0	-	-	mAdc	-	-	-	-	-	-	-	-	14	-	-	-	7
MC961/MC861	I_{PDH}	14	-	-	-	10.7	-	-		-	-	-	13.1	-	-		-	-	-	-	-	-	-	-	14	-	-	-	7
All Types	I_{max}	14	-	-	-	5.5	-	-		-	-	-	8.0	-	-		-	-	-	-	-	-	-	-	-	-	-	14	1,7,9
Switching Times																	Pulse In	Pulse Out											
MC930/MC830	t_{pd+}	1,6	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,6	-	-	10	30	-	-		-	-	10	30	-	-				-	-	-	-	-	-		-	-	-	
MC961/MC861	t_{pd+}	1,6	-	-	15	60	-	-		-	-	15	60	-	-				-	-	-	-	-	-		-	-	-	
	t_{pd-}	1,6	-	-	10	30	-	-		-	-	10	30	-	-				-	-	-	-	-	-		-	-	-	

Pins not listed are left open.

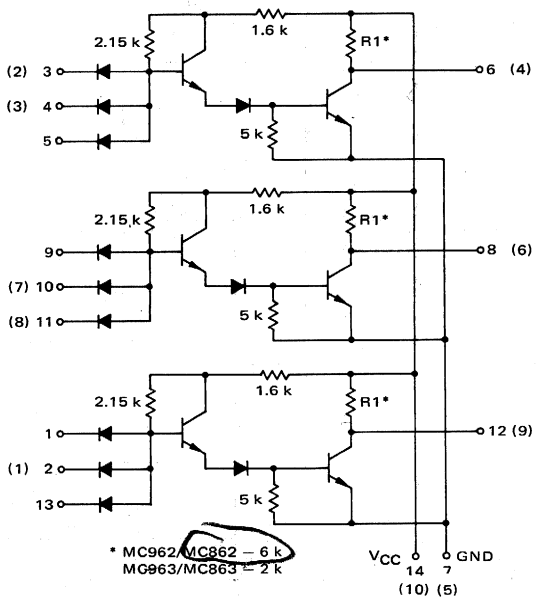
TRIPLE 3-INPUT GATES

MC962F · MC862F, P
MC963F · MC863F, P

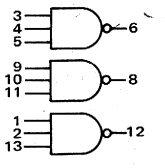
DUAL 2-INPUT GATES PLUS INVERTER

MC962G · MC862G
MC963G · MC863G

This gate element, in the 14-pin flat and dual in-line packages, consists of three 3-input NAND gate circuits. Since the metal can (G suffix) has only 10 pins, that circuit consists of two 2-input gates and one inverter.



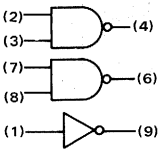
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC962F/MC862F,P
MC963F/MC863F,P

Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Negative Logic: $6 = \overline{3 + 4 + 5}$



MC962G/MC862G
MC963G/MC863G

Positive Logic: $4 = \overline{2 \cdot 3}$

Negative Logic: $4 = \overline{2 + 3}$

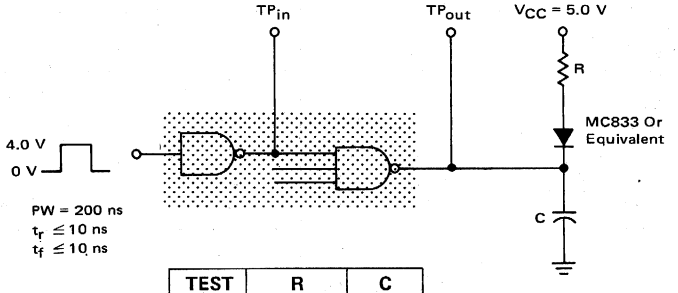
Input Loading Factor = 1

Output Loading Factor:
- MC962/MC862 = 8
- MC963/MC863 = 7

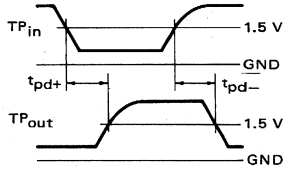
Total Power Dissipation:
- MC962F/MC862F, P = 33 mW typ/pkg
- MC962G/MC862G = 30 mW typ/pkg
- MC963F/MC863F,P = 50 mW typ/pkg
- MC963G/MC863G = 45 mW typ/pkg

Propagation Delay Time
- MC962/MC862 = 30 ns typ
- MC963/MC863 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

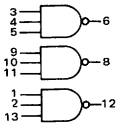


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	–	1	2	3	–	4	5	6	–	7	8	9	–	10



@ Test Temperature		TEST CURRENT / VOLTAGE VALUES													
		mA				Volts									
		I_{OL}		I_{OH}		V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
		MC962	MC963	MC962	MC963									
MC962, MC963	−55°C	11.4	10.4	-0.12	-0.5	1.40	2.10	0	4.00	-	-	4.50	5.50	-
	+25°C	12.0	11.0	-0.12	-0.5	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	10.8	9.8	-0.12	-0.5	0.80	2.00	0	4.00	-	-	4.50	5.50	-
		MC862	MC863	MC862	MC863									
MC862, MC863	0°C	12.0	11.0	-0.12	-0.5	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-
	+25°C	12.0	11.0	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	11.4	10.4	-0.12	-0.5	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC962, MC963 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC862, MC863 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	3,4,5	-	-	-	-	14	-	-	7
	V_{OH}	6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	3	-	-	-	-	-		-	-	
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	↓	4	-	-	-	-	-	↓	-	-	↓
				-		-		-			-		-		-		-		5	-	-	-	-	-		-	-	
Short-Circuit Current																												
MC962/MC862	I_{SC}	6	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	14	-	3,6,7
MC963/MC863		6	-	-4.00	-	-4.00	-	-3.90	mAdc	-	-3.90	-	-3.90	-	-3.75	mAdc	-	-	-	-	-	-	-	-	-	14	-	3,6,7
Reverse Current	I_R	3	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	3	-	-	-	14	-	4,5,7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	-	↓	-	3,5,7
		5	-		-		-			-		-		-			-	-	-	-	-	5	-	-	-		-	3,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	6,14	-	-	-	-	3,7
Forward Current	I_F	3	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	3	4,5	-	-	-	14	-	7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	4	3,5	-	-	-	↓	-	↓
		5	-		-		-			-		-		-			-	-	-	-	5	3,4	-	-	-		-	
Power Drain Current (Total Device)																												
MC962/MC862	I_{PDH}	14	-	-	-	9.75	-	-	mAdc	-	-	-	12	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	7
MC963/MC863	I_{PDH}	14	-	-	-	16	-	-	↓	-	-	-	19.6	-	-	↓	-	-	-	-	-	-	-	14	-	-	-	7
All Types	I_{max}	14	-	-	-	8.25	-	-	↓	-	-	-	12	-	-	↓	-	-	-	-	-	-	-	-	-	-	14	3,7,9,13
Switching Times																	Pulse In	Pulse Out										
MC962/MC862	t_{pd+}	3,6	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	3	6	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	3,6	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓
MC963/MC863	t_{pd+}	3,6	-	-	15	60	-	-		-	-	15	60	-	-				-	-	-	-	-		-	-	-	
	t_{pd-}	3,6	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓

Pins not listed are left open.

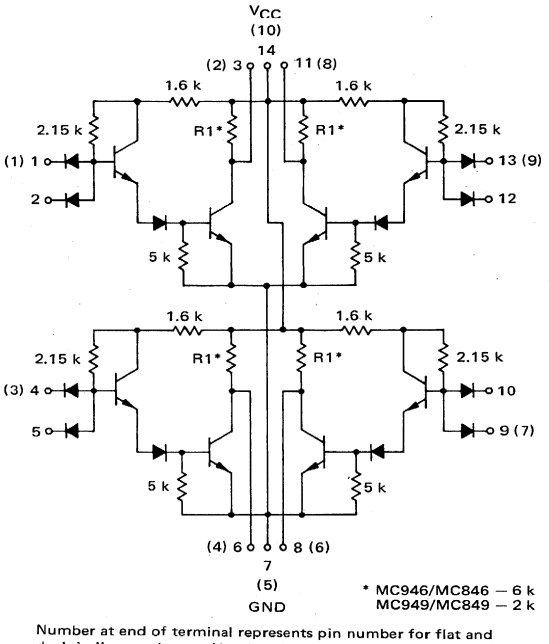
QUAD 2-INPUT GATES

MC946F · MC846F, P
MC949F · MC849F, P

QUAD INVERTERS

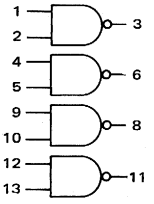
MC946G · MC846G
MC949G · MC849G

This gate element, in the 14-pin flat and dual in-line packages, consists of four 2-input NAND gate circuits. This circuit can be used as a dual 2-input non-inverting gate, or as two bistable circuits when two dual 2-input gates are cross-coupled. Since the metal can (G suffix) has only 10 pins, that circuit consists of four inverters.



* MC946/MC846 — 6 k
MC949/MC849 — 2 k

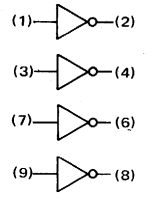
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC946F/MC846F, P
MC949F/MC849F, P

Positive Logic: $3 = \overline{1 \cdot 2}$

Negative Logic: $3 = \overline{1 + 2}$



MC946G/MC846G
MC949G/MC849G

Positive Logic: $2 = \overline{1}$

Negative Logic: $2 = \overline{1}$

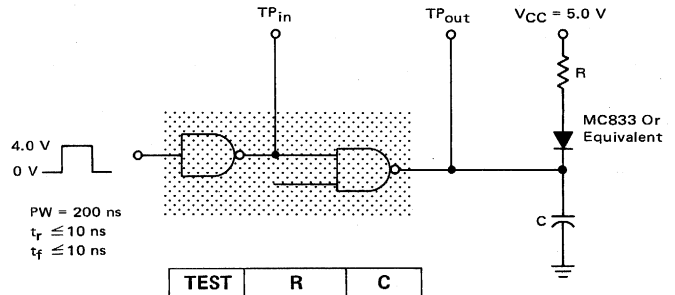
Input Loading Factor = 1

Output Loading Factor:
MC946/MC846 = 8
MC949/MC849 = 7

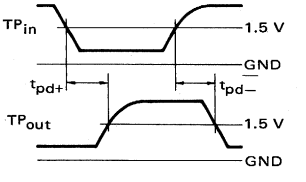
Total Power Dissipation:
MC946/MC846 = 44 mW typ/pkg
MC949F/MC849F, P = 66 mW typ/pkg
MC949G/MC849G = 60 mW typ/pkg

Propagation Delay Time:
MC946/MC846 = 30 ns typ
MC949/MC849 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

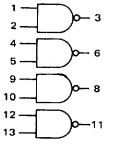


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	1	–	2	3	–	4	5	6	7	–	8	–	9	10

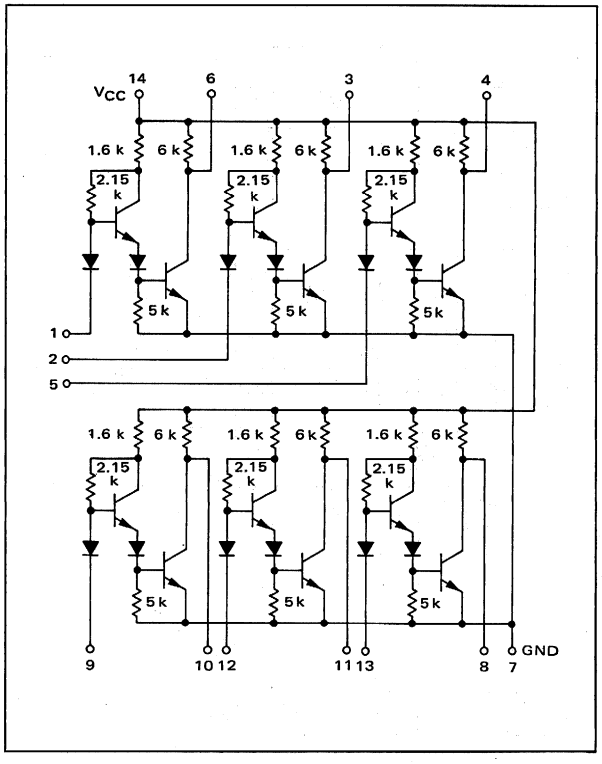


	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES													
		mA				Volts									
		I_{OL}		I_{OH}											
		MC946	MC949	MC946	MC949	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	
MC946, MC949	−55°C	11.4	10.4	-0.12	-0.5	1.40	2.10	0	4.00	-	-	4.50	5.50	-	
	+25°C	12.0	11.0	-0.12	-0.5	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00	
	+125°C	10.8	9.8	-0.12	-0.5	0.80	2.00	0	4.00	-	-	4.50	5.50	-	
		MC846	MC849	MC846	MC849										
MC846, MC849	0°C	12.0	11.0	-0.12	-0.5	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-	
	+25°C	12.0	11.0	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	11.4	10.4	-0.12	-0.5	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-	

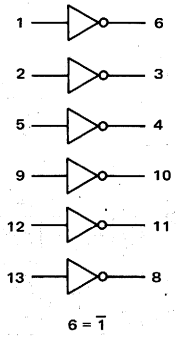
Characteristic	Symbol	Pin Under Test	MC946, MC949 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC846, MC849 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	3	-	-	1,2	-	-	-	-	14	-	-	7
	V_{OH}	3	2.50	-	2.60	-	2.50	-	↓	2.60	-	2.60	-	2.50	-	↓	-	3	1	-	-	-	-	-	↓	-	-	↓
		3	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	3	2	-	-	-	-	-		-	-	
Short-Circuit Current																												
MC946/MC846	I_{SC}	3	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,3,7
MC949/MC849		3	-	-4.00	-	-4.00	-	-3.90	mAdc	-	-3.90	-	-3.90	-	-3.75	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,3,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	1	-	-	-	14	-	2,7
		2	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	2	-	-	-	14	-	1,7
Output Leakage Current	I_{CEX}	3	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	3,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	1	2	-	-	-	14	-	7
		2	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	2	1	-	-	-	14	-	7
Power Drain Current (Total Device)																												
MC946/MC846	I_{PDH}	14	-	-	-	13	-	-	mAdc	-	-	-	16	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	7
MC949/MC849	I_{PDH}	14	-	-	-	21.4	-	-	↓	-	-	-	26.2	-	-	↓	-	-	-	-	-	-	-	14	-	-	-	7
All Types	I_{max}	14	-	-	-	11	-	-		-	-	-	16	-	-		-	-	-	-	-	-	-	-	-	-	14	1,4,7,9,12
Switching Times																	Pulse In	Pulse Out										
MC946/MC846	t_{pd+}	1,3	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	3	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,3	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓
MC949/MC849	t_{pd+}	1,3	-	-	15	60	-	-		-	-	15	60	-	-				-	-	-	-	-		-	-	-	
	t_{pd-}	1,3	-	-	10	30	-	-		-	-	10	30	-	-				-	-	-	-	-		-	-	-	

Pins not listed are left open.

MC934F · MC834F, P

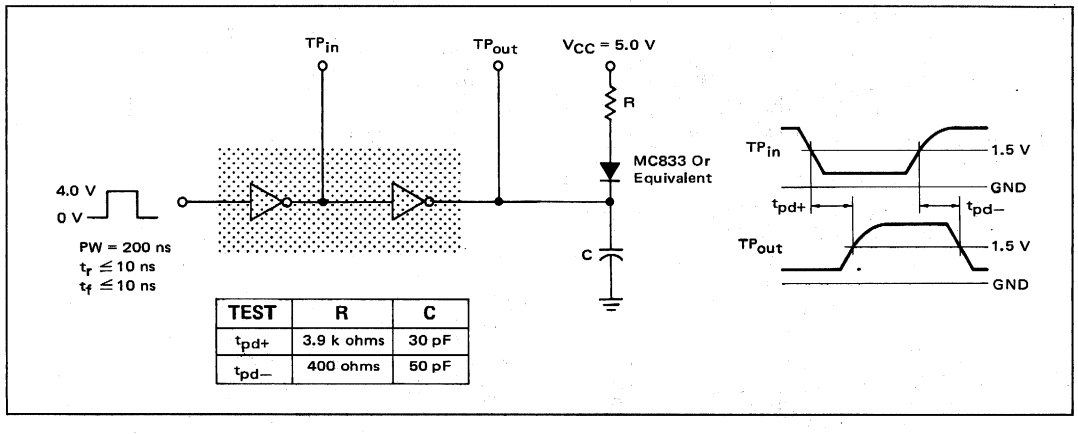


This element consists of six inverter circuits.



Input Loading Factor = 1
Output Loading Factor = 8
Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 30 ns typ

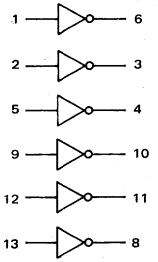
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

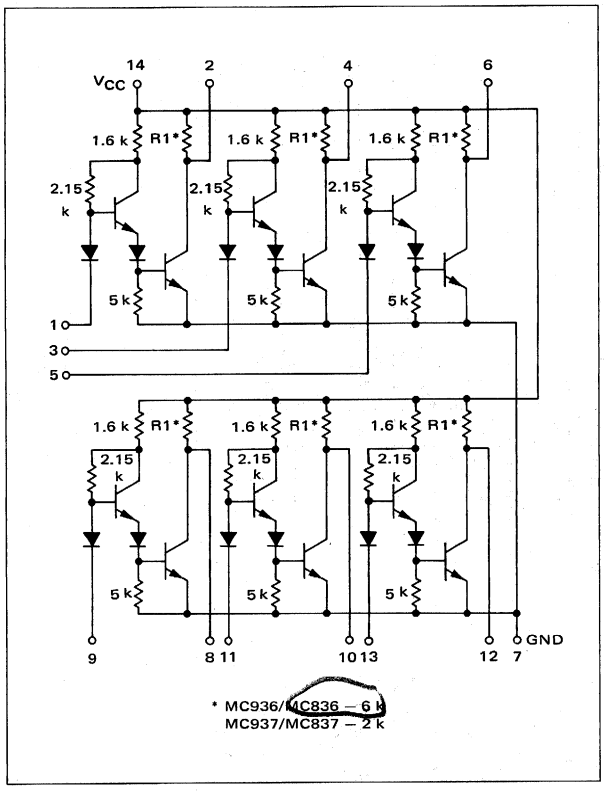


@ Test Temperature		TEST CURRENT / VOLTAGE VALUES											
		mA		Volts									
		I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	
MC934	−55°C	11.4	-0.12	1.40	2.10	0	4.00	-	-	4.50	5.50	-	
	+25°C	12.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00	
	+125°C	10.8	-0.12	0.80	2.00	0	4.00	-	-	4.50	5.50	-	
MC834	0°C	12.0	-0.12	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-	
	+25°C	12.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	11.4	-0.12	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-	

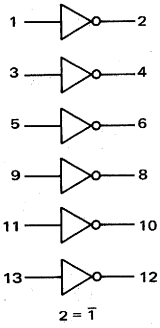
Characteristic	Symbol	Pin Under Test	MC934 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC834 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	1	-	-	-	-	14	-	-	7
	V_{OH}	6	2.50	-	2.60	-	2.50	-	Vdc	2.60	-	2.60	-	2.50	-	Vdc	-	6	1	-	-	-	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,6,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	1	-	-	-	14	-	7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	6,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	1	-	-	-	-	14	-	7
Power Drain Current (Total Device)	I_{PDH}	14	-	-	-	19.5	-	-	mAdc	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	16.5	-	-	mAdc	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,2,5,7, 9,12,13
Switching Times																	Pulse In	Pulse Out										
	t_{pd+}	1,6	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	6	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,6	-	-	10	30	-	-	ns	-	-	10	30	-	-	ns	1	6	-	-	-	-	-	14	-	-	-	7

Pins not listed are left open.

MC936F · MC836F, P
MC937F · MC837F, P



This element consists of six inverter circuits.



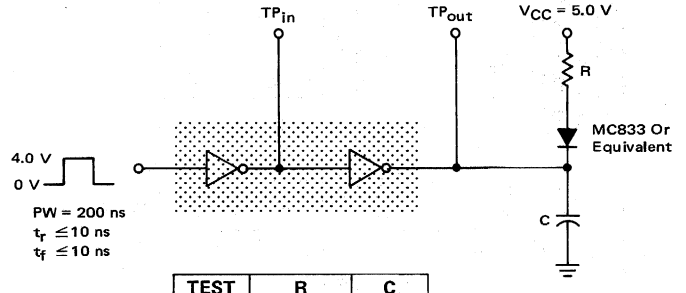
Input Loading Factor = 1

Output Loading Factor:
MC936/MC836 = 8
MC937/MC837 = 7

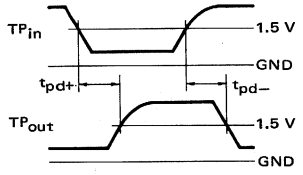
Total Power Dissipation
MC936/MC836 = 66 mW typ/pkg
MC937/MC837 = 90 mW typ/pkg

Propagation Delay Time
MC936/MC836 = 30 ns typ
MC937/MC837 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

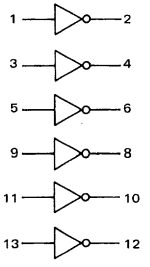


TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



@ Test Temperature		TEST CURRENT / VOLTAGE VALUES												
		mA				Volts								
		I_{OL}		I_{OH}										
		MC936	MC937	MC936	MC937	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC936, MC937	−55°C	11.4	10.4	-0.12	-0.5	1.40	2.10	0	4.00	-	-	4.50	5.50	-
	+25°C	12.0	11.0	-0.12	-0.5	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	10.8	9.8	-0.12	-0.5	0.80	2.00	0	4.00	-	-	4.50	5.50	-
		MC836	MC837	MC836	MC837									
MC836, MC837	0°C	12.0	11.0	-0.12	-0.5	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-
	+25°C	12.0	11.0	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	11.4	10.4	-0.12	-0.5	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC936, MC937 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC836, MC837 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	2	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	2	-	-	1	-	-	-	-	14	-	-	7
	V_{OH}	2	2.50	-	2.60	-	2.50	-	Vdc	2.60	-	2.60	-	2.50	-	Vdc	-	2	1	-	-	-	-	-	14	-	-	7
Short-Circuit Current																												
MC936/MC836	I_{SC}	2	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,2,7
MC937/MC837		2	-	-4.00	-	-4.00	-	-3.90	mAdc	-	-3.90	-	-3.90	-	-3.75	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,2,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	1	-	-	-	14	-	7
Output Leakage Current	I_{CEX}	2	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	2,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	1	-	-	-	-	14	-	7
Power Drain Current (Total Device)																												
MC936/MC836	I_{PDH}	14	-	-	-	19.5	-	-	mAdc	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	7
MC937/MC837	I_{PDH}	14	-	-	-	32.0	-	-	↓	-	-	-	39	-	-	↓	-	-	-	-	-	-	-	14	-	-	-	7
All Types	I_{max}	14	-	-	-	16.5	-	-	↓	-	-	-	24	-	-	↓	-	-	-	-	-	-	-	-	-	-	14	1,3,5,7, 9,11,13
Switching Times																	Pulse In	Pulse Out										
MC936/MC836	t_{pd+}	1,2	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	2	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,2	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓
MC937/MC837	t_{pd+}	1,2	-	-	15	60	-	-	↓	-	-	15	60	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓
	t_{pd-}	1,2	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓

Pins not listed are left open.

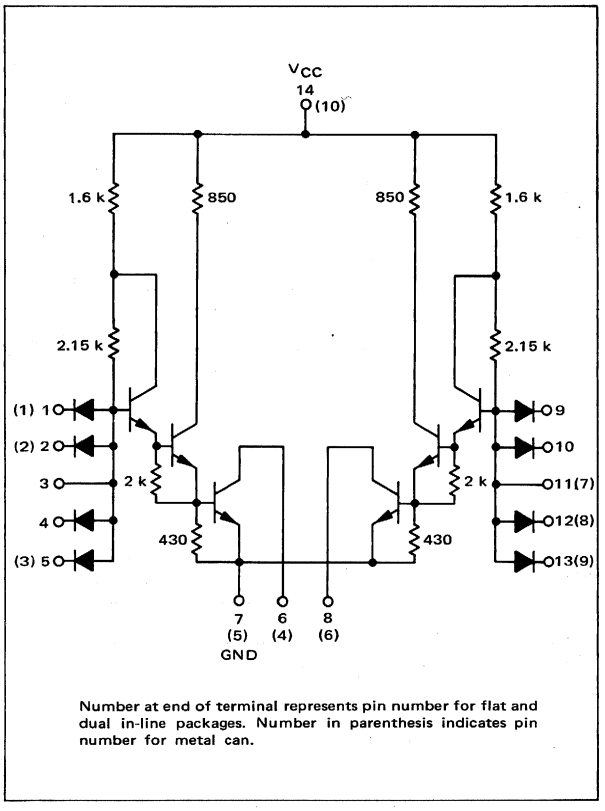
EXPANDABLE DUAL 4-INPUT POWER GATES

MC944F • MC844F, P

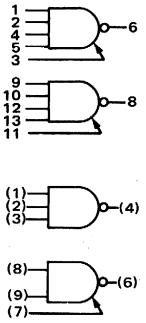
EXPANDABLE DUAL 3-2 INPUT POWER GATES

MC944G • MC844G

The MC944/MC844 is a dual NAND power gate with an output transistor capable of sinking more current than standard gate elements. It is useful as a high fan-out gate (with an external pull-up resistor), and as a line, relay, or lamp driver. Each output of the MC944/MC844 is capable of sinking up to 100 mA individually (90 mA if both outputs are conducting simultaneously) provided that temperature extremes are limited to 0°C to +100°C for MC944, and +15°C to +55°C for MC844. The typical breakdown voltage of the output transistor is greater than 12 V.



Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC944F/MC844F, P

Positive Logic:

$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

Negative Logic:

$6 = \overline{1 + 2 + 4 + 5 + [3]}$

MC944G/MC844G

Positive Logic: $4 = \overline{1 \cdot 2 \cdot 3}$

Negative Logic: $4 = \overline{1 + 2 + 3}$

Input Loading Factor = 1
Output Loading Factor = 27
Total Power Dissipation = 65 mW typ/pkg
Propagation Delay Time = 30 ns typ

OPERATING RULES

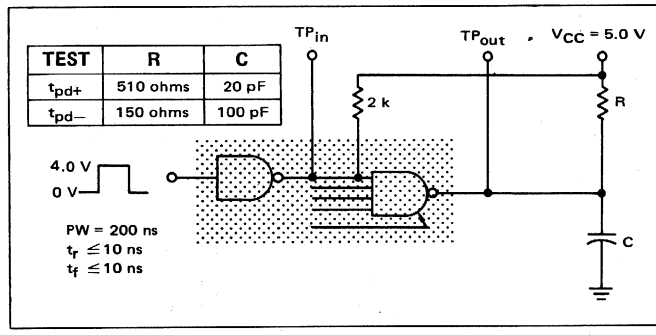
- The outputs of the Dual Power Gate may be tied together to perform the wired-collector OR function.
- An external load resistor should be utilized with the Dual Power Gate. At V_{CC} = 5.0 ±0.5 V, subtract the following output loads:

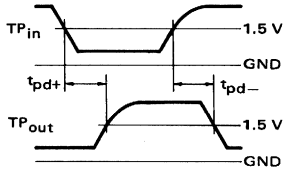
  R
  2 kΩ – 2 loads
  1 kΩ – 4 loads
  510Ω – 8 loads

- For increased current capability, the inputs and outputs of ½MC944 and ½MC932 can be paralleled (up to and including 4 common outputs). The combined output will equal 100 loads while each combined input will equal 4 loads.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

TEST	R	C
t_{pd+}	510 ohms	20 pF
t_{pd-}	150 ohms	100 pF



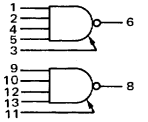


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gate is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	1	2	-	-	3	4	5	6	-	-	7	8	9	10



@ Test Temperature		I_{OL} (mA)	I_{CE} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_X (Volts)	V_F (Volts)	V_R (Volts)	V_{CEX} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	V_{max} (Volts)
MC944	−55°C	36	-	-	2.10	-	0	4.00	-	-	4.50	5.50	-
	+25°C	40	5.00	1.10	2.00	1.80	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	36	-	-	2.00	-	0	4.00	-	-	4.50	5.50	-
MC844	0°C	40	-	-	2.00	-	0.45	4.00	-	-	5.00	5.00	-
	+25°C	40	5.00	1.10	1.90	1.80	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	36	-	-	1.80	-	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC944 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC844 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{CE} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_X (Volts)	V_F (Volts)	V_R (Volts)	V_{CEX} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	V_{max} (Volts)	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	1,2,4,5	-	-	-	-	-	14	-	-	7
Output Breakdown Voltage	LV_{CE}	6	-	-	6.0	-	-	-	Vdc	-	-	6.0	-	-	-	Vdc	-	6	-	-	-	-	-	-	-	-	14	-	1,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	µAdc	-	5.0	-	5.0	-	10	µAdc	-	-	-	-	-	-	1	-	-	-	14	-	2,4,5,7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	2	-	-	-	↓	-	1,4,5,7
		4	-		-		-			-		-		-			-	-	-	-	-	-	4	-	-	-		-	1,2,5,7
		5	-		-		-			-		-		-			-	-	-	-	-	-	5	-	-	-		-	1,2,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	µAdc	-	-	-	100	-	-	µAdc	-	-	1	-	-	-	-	6	-	-	14	-	7
			-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	-	-	2	-	-	-	-	↓	-	-	↓	-	↓
			-	-	-		-	-		-	-	-		-	-		-	-	4	-	-	-	-		-	-		-	
			-	-	-		-	-		-	-	-		-	-		-	-	5	-	-	-	-		-	-		-	
			-	-	-		-	-		-	-	-		-	-		-	-	-	-	3	-	-		-	-		-	
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	-	1	2,4,5	-	-	-	14	-	7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	2	1,4,5	-	-	-	↓	-	↓
		4	-		-		-			-		-		-			-	-	-	-	-	4	1,2,5	-	-	-		-	
		5	-		-		-			-		-		-			-	-	-	-	-	5	1,2,4	-	-	-		-	
Power Drain Current (Total Device)	I_{PDH}	14	-	-	-	20	-	-	mAdc	-	-	-	22.5	-	-	mAdc	-	-	-	-	-	-	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	6.0	-	-	mAdc	-	-	-	8.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,7,9
Switching Times																	Pulse In	Pulse Out											
	t_{pd+}	1,6	-	-	15	50	-	-	ns	-	-	15	50	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,6	-	-	10	35	-	-	ns	-	-	10	35	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7

Pins not listed are left open.

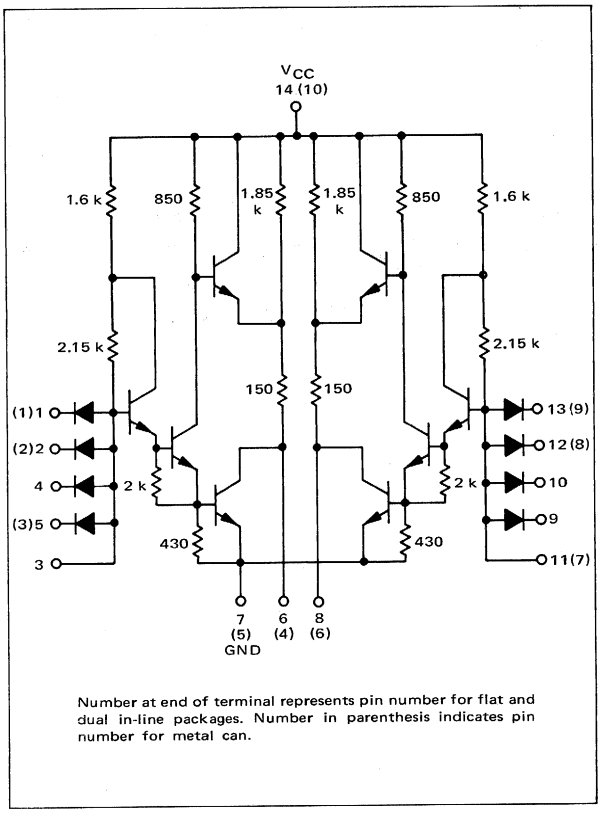
EXPANDABLE DUAL 4-INPUT BUFFERS

MC932F • MC832F, P

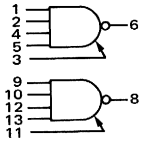
EXPANDABLE DUAL 3-2 INPUT BUFFERS

MC932G • MC832G

This buffer element, in the 14-pin flat and dual in-line packages, consists of two expandable 4-input inverting drivers. Since the metal can (G suffix) has only 10 pins, this circuit consists of one 3-input and one 2-input expandable inverting driver. These units are designed especially for driving large capacitive loads at high speeds. An output emitter follower in series with a 150-ohm resistor drives the output to the high voltage level. A low saturation resistance transistor is turned on, pulling the output down to the low voltage level, and providing rapid discharge of capacitive loads.



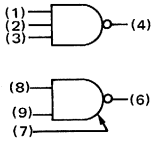
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC932F/MC832F, P

Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

Negative Logic: $6 = \overline{1 + 2 + 4 + 5 + [3]}$



MC932G/MC832G

Positive Logic: $4 = \overline{1 \cdot 2 \cdot 3}$

Negative Logic: $4 = \overline{1 + 2 + 3}$

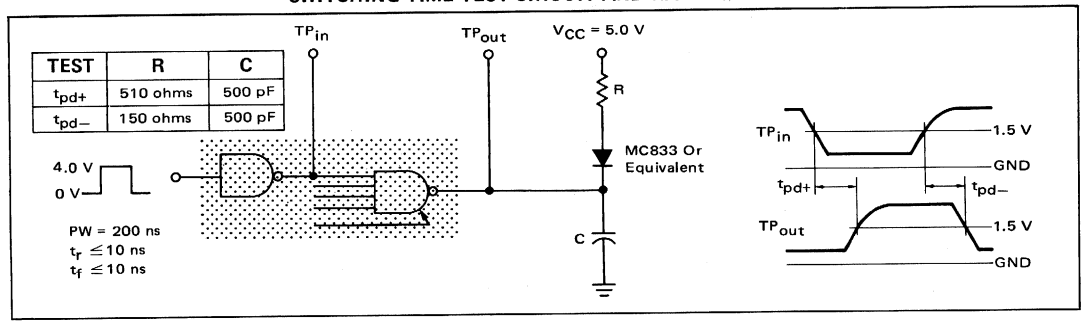
Input Loading Factor = 1
Output Loading Factor = 25
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 35 ns typ

OPERATING RULES

- The outputs of the Dual Buffer may not be tied together.
- For increased current capability, the inputs and outputs of ½MC932 and ½MC944 can be paralleled (up to and including 4 common outputs). The combined output will equal 100 loads while each combined input will equal 4 loads.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

TEST	R	C
t_{pd+}	510 ohms	500 pF
t_{pd-}	150 ohms	500 pF

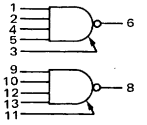


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	1	2	–	–	3	4	5	6	–	–	7	8	9	10

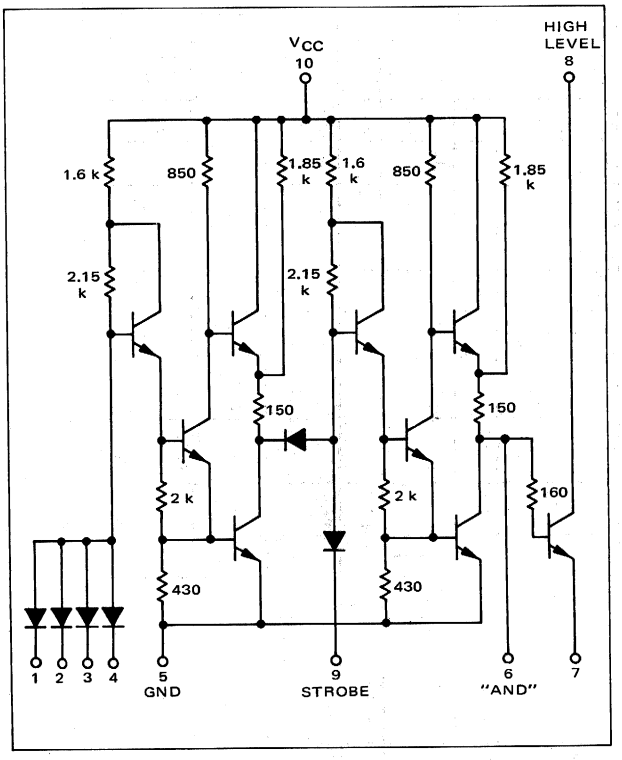


	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES												
		mA		Volts										
		I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_X	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	
MC932	−55°C	34	-2.00	1.40	2.10	-	0	4.00	-	-	4.50	5.50	-	
	+25°C	36	-2.50	1.10	2.00	1.80	0	4.00	4.50	5.00	4.50	5.50	8.00	
	+125°C	32	-4.00	0.80	2.00	-	0	4.00	-	-	4.50	5.50	-	
MC832	0°C	36	-2.00	1.20	2.00	-	0.45	4.00	-	-	5.00	5.00	-	
	+25°C	36	-2.50	1.10	1.90	1.80	0.45	4.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	34	-3.00	0.95	1.80	-	0.50	4.00	-	-	5.00	5.00	-	

Characteristic	Symbol	Pin Under Test	MC932 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC832 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_X	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	1,2,4,5	-	-	-	-	-	14	-	-	7
	V_{OH}	6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	1	-	-	-	-	-	-	-	-	-	
				-		-		-			-		-		-		-		2	-	-	-	-	-	-	-	-	-	
				-		-		-			-		-		-		-		4	-	-	-	-	-	-	-	-	-	
				-		-		-			-		-		-		-		5	-	-	-	-	-	-	-	-	-	
				-		-		-			-		-		-		-		-	-	3	-	-	-	-	-	-	-	
Short-Circuit Current	I_{SC}	6	-16	-	-18	-	-16	-	mAdc	-15	-	-16	-	-14	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	1,6,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	-	1	-	-	-	14	-	2,4,5,7
		2	-		-		-			-		-		-			-	-	-	-	-	-	2	-	-	-		-	1,4,5,7
		4	-		-		-			-		-		-			-	-	-	-	-	-	4	-	-	-		-	1,2,5,7
		5	-		-		-			-		-		-			-	-	-	-	-	-	5	-	-	-		-	1,2,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	-	6,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	-	1	2,4,5	-	-	-	14	-	7
		2	-		-		-			-		-		-			-	-	-	-	-	2	1,4,5	-	-	-		-	
		4	-		-		-			-		-		-			-	-	-	-	-	4	1,2,5	-	-	-		-	
		5	-		-		-			-		-		-			-	-	-	-	-	5	1,2,4	-	-	-		-	
Power Drain Current (Total Device)	I_{PDH}	14	-	-	-	26.6	-	-	mAdc	-	-	-	30	-	-	mAdc	-	-	-	-	-	-	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	6.0	-	-	mAdc	-	-	-	8.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,7,9
Switching Times																	Pulse In	Pulse Out											
	t_{pd+}	1,6	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,6	-	-	15	40	-	-	ns	-	-	15	40	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7

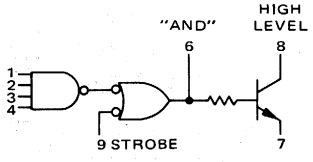
Pins not listed are left open.

MC943G • MC843G



Maximum permissible voltage applied to Pin 8 = 40 Vdc.

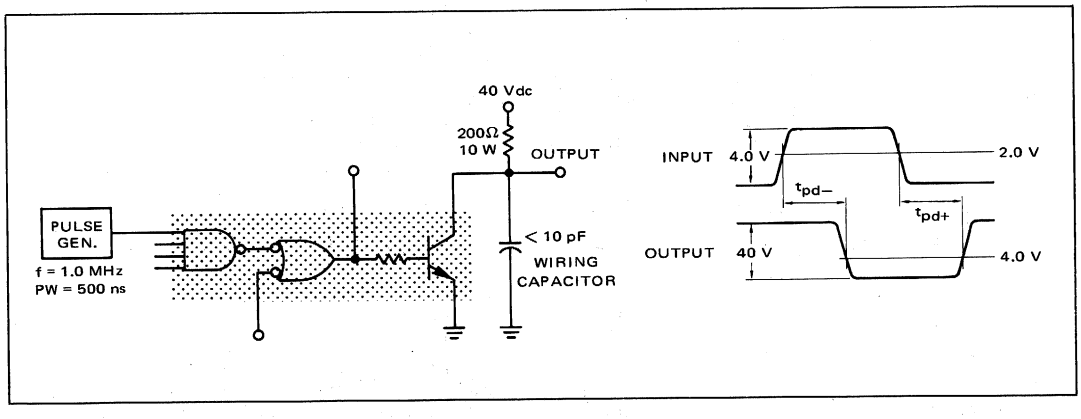
This device is a monolithic dual buffer element in a hybrid configuration with a high performance NPN silicon transistor to allow the output stage to operate to 40 volts with sink current capability of 250 mA. The device may also be used in conjunction with other saturated logic forms.



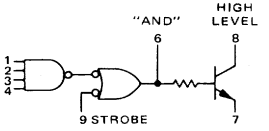
Positive Logic: $\overline{8} = 1 \cdot 2 \cdot 3 \cdot 4 + \overline{9}$
Negative Logic: $\overline{8} = (1 + 2 + 3 + 4)\overline{9}$

Total Power Dissipation = 50 mW typ/pkg
Propagation Delay Time = 80 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

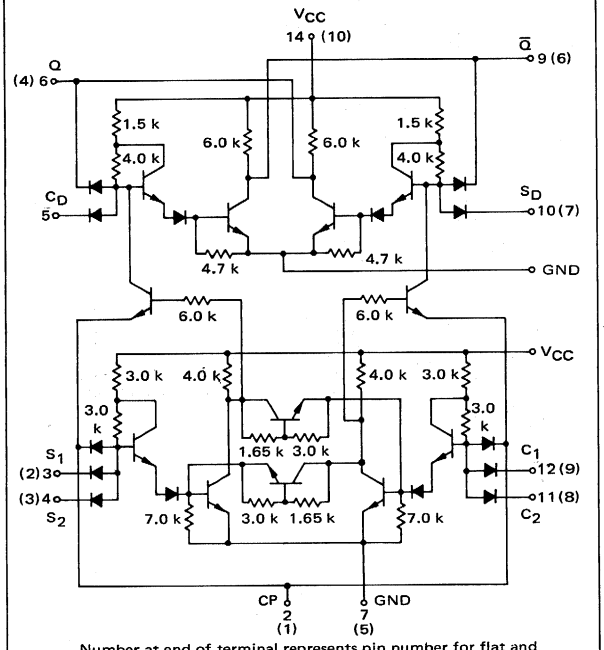


	@ Test Temperature	I_{OL} (mA)	I_{OLB} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_{OX} (Volts)	V_F (Volts)	V_R (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	V_{max} (Volts)
MC943	−55°C	250	34	1.40	2.10	40	0	4.00	-	5.00	5.50	-
MC943	+25°C	250	36	1.10	2.00	40	0	4.00	5.00	5.00	5.50	8.00
MC943	+125°C	250	32	0.80	2.00	40	0	4.00	-	5.00	5.50	-
MC843	0°C	250	36	1.20	2.00	40	0.45	4.00	-	5.00	5.00	-
MC843	+25°C	250	36	1.10	.90	40	0.45	4.00	5.00	5.00	5.00	8.00
MC843	+75°C	250	34	0.95	1.80	40	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC943 Test Limits −55°C Min	MC943 Test Limits −55°C Max	MC943 Test Limits +25°C Min	MC943 Test Limits +25°C Max	MC943 Test Limits +125°C Min	MC943 Test Limits +125°C Max	Unit	MC843 Test Limits 0°C Min	MC843 Test Limits 0°C Max	MC843 Test Limits +25°C Min	MC843 Test Limits +25°C Max	MC843 Test Limits +75°C Min	MC843 Test Limits +75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{OLB} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_{OX} (Volts)	V_F (Volts)	V_R (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	V_{max} (Volts)	Gnd
Output Voltage	V_{OL}	8	-	0.50	-	0.50	-	0.50	Vdc	-	0.50	-	0.50	-	0.50	Vdc	8	-	-	1,2,3,4	-	-	-	-	10	-	-	5,7
		8	-	0.50	-	0.50	-	0.50		-	0.50	-	0.50	-	0.50		8	-	1,2,3,4,9	-	-	-	-	-		-	-	
	V_{OLB}	6	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		-	6	1	-	-	-	-	-		-	-	
			-		-		-			-		-		-			-		2	-	-	-	-	-		-	-	
			-		-		-			-		-		-			-		3	-	-	-	-	-		-	-	
			-		-		-			-		-		-			-		4	-	-	-	-	-		-	-	
	V_{OHB}	6	2.20	-	2.00	-	1.80	-		2.00	-	2.00	-	1.90	-		-	-	-	1,2,3,4	-	-	-	-		-	-	
		6	2.20	-	2.00	-	1.80	-		2.00	-	2.00	-	1.90	-		-	-	1,2,3,4,9	-	-	-	-	-		-	-	
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	-	1	-	-	10	-	2,3,4,5,7
		2	-		-		-			-		-		-			-	-	-	-	-	-	2	-	-		-	1,3,4,5,7
		3	-		-		-			-		-		-			-	-	-	-	-	-	3	-	-		-	1,2,4,5,7
		4	-		-		-			-		-		-			-	-	-	-	-	-	4	-	-		-	1,2,3,5,7
		9	-		-		-			-		-		-			-	-	-	-	-	-	9	-	-		-	5,7
Output Leakage Current	I_{CEX}	8	-	5.0	-	5.0	-	200	μAdc	-	10	-	10	-	200	μAdc	-	-	-	-	8	-	-	-	10	-	-	1,5,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	-	1	2,3,4	-	-	10	-	5,7
		2	-		-		-			-		-		-			-	-	-	-	-	2	1,3,4	-	-		-	
		3	-		-		-			-		-		-			-	-	-	-	-	3	1,2,4	-	-		-	
		4	-		-		-			-		-		-			-	-	-	-	-	4	1,2,3	-	-		-	
		9	-		-		-			-		-		-			-	-	-	-	-	9	-	-	-		-	
Power Drain Current	I_{PDH}	10	-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc	-	-	-	-	-	-	-	10	-	-	-	5,7
	I_{max}	10	-	-	-	6.0	-	-	mAdc	-	-	-	8.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	10	1,5,9
Switching Times																	Pulse In	Pulse Out										
	t_{pd-}	1, 8	-	-	-	100	-	-	ns	-	-	-	140	-	-	ns	1	8	-	-	-	-	-	10	-	-	-	5,7
	t_{pd+}	1, 8	-	-	-	150	-	-	ns	-	-	-	230	-	-	ns	1	8	-	-	-	-	-	10	-	-	-	5,7

Pins not listed are left open.

MC931F, G · MC831F, P, G

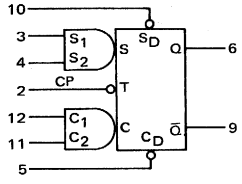


Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

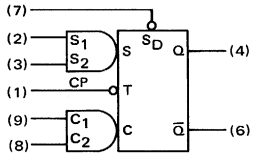
This clocked flip-flop consists of two directly coupled flip-flops, operating on the "master-slave" principle. Operation depends only on voltage levels, and the shape of the input clock becomes unimportant in determining the state of this flip-flop. The input information is stored in the "master" flip-flop when the clock voltage is high, and is transferred to the "slave" when the clock voltage is low.

This clocked flip-flop can be operated in either the R-S or J-K mode. For J-K operation the Q output is connected to a clear input, and the $\overline{Q}$ output is connected to a set input. Direct set (S_D) and direct clear (C_D) inputs are available.

MC931F/MC831F, P



MC931G/MC831G



SYNCHRONOUS TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

0 – Low State (more negative)

1 – High State (more positive)

X – State of the input does not affect the state of the circuit.

U – Indeterminate State

J-K TRUTH TABLE

(Connect S_2 to $\overline{Q}$, C_2 to Q)

t_n		t_{n+1}
S_1	C_1	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

ASYNCHRONOUS TRUTH TABLE

S_D	C_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs.

Input Loading Factor:
S and C = 2/3
S_D and C_D = 3/4
T = 2

Output Loading Factor = 7

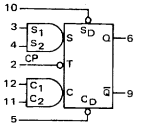
Total Power Dissipation = 55 mW typ/pkg

Propagation Delay Time = 40 ns typ

ELECTRICAL CHARACTERISTICS

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBERS												
Flat/Dual In-Line	–	2	3	4	5	6	7	–	9	10	11	12	–	14
Metal Can	–	1	2	3	–	4	5	–	6	7	8	9	–	10



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_{max}
MC931	−55°C	10.0	-0.12	1.40	2.10	0	4.00	-	4.50	5.50	-
	+25°C	10.6	-0.12	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	9.5	-0.12	0.80	2.00	0	4.00	-	4.50	5.50	-
MC831	0°C	10.5	-0.12	1.20	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	10.5	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	10.2	-0.12	0.95	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC931 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC831 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	CP_a§	CP_b§	CP_c§	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	-	-	-	-	14	-	-	-	2	-	3,7,9‡
		9	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		9	-	-	-	-	-	-		-	-	-	2	-	6‡,7,12
	V_{OH}	6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6†	11	3,4	-	-	-		-	-	2	-	-	7
				-		-		-			-		-		-		-	6†	12	3,4	-	-	-		-	-		-	-	7
				-		-		-			-		-		-		-	6	10	5	-	-	-		-	-		-	-	3,4,7
		9		-		-		-			-		-		-		-	9†	3	11,12	-	-	-		-	-		-	-	7
				-		-		-			-		-		-		-	9†	4	11,12	-	-	-		-	-		-	-	7
				-		-		-			-		-		-		-	9	5	10	-	-	-		-	-		-	-	7,11,12
Reverse Current	I_R	3	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	3	-	-	14	-	-	-	-	2,7
		4	-		-		-			-		-		-			-	-	-	-	-	4	-	-		-	-	-	-	2,7
		5	-		-		-			-		-		-			-	-	-	-	-	5	-	-		-	2	-	-	3,4,7
		10	-		-		-			-		-		-			-	-	-	-	-	10	-	-		-	2	-	-	7,11,12
		11	-		-		-			-		-		-			-	-	-	-	-	11	-	-		-	-	-	-	2,7
		12	-		-		-			-		-		-			-	-	-	-	-	12	-	-		-	-	-	-	2,7
	I_{RCP}	2	-	20	-	20	-	30		-	30	-	30	-	40		-	-	-	-	-	2	-	-		-	-	-	-	3,4,7,11,12
Forward Current	2/3 I_F	3	-	-1.07	-	-1.07	-	-1.00	mAdc	-	-0.95	-	-0.95	-	-0.90	mAdc	-	-	-	-	-	3	-	-	14	-	-	-	-	7
		4	-		-		-			-		-		-			-	-	-	-	-	4	-	-		-	-	-	-	
		11	-		-		-			-		-		-			-	-	-	-	-	11	-	-		-	-	-	-	
		12	-		-		-			-		-		-			-	-	-	-	-	12	-	-		-	-	-	-	
	I_{FCP}	2	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	4	-	-	-	-	-		-	-	-	2	
	I_{FCP}	2	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	11	-	-	-	-	-		-	-	-	2	
	I_{FS}	5	-	-1.20	-	-1.20	-	-1.10		-	-1.05	-	-1.05	-	-1.00		-	-	-	-	5	-	-	-		-	-	-	-	4,7,9,10
	I_{FS}	10	-	-1.20	-	-1.20	-	-1.10		-	-1.05	-	-1.05	-	-1.00		-	-	-	-	10	-	-	-		-	-	-	-	5,6,7,11
Power Drain Current	I_{PDH}	14	-	-	-	11	-	-	mAdc	-	-	-	14	-	-	mAdc	-	-	-	-	-	-	14	-	-	-	-	-	-	7
	I_{max}	14	-	-	-	14.5	-	-	mAdc	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	2,3,4,7, 11,12
Switching Times																	Pulse In	Pulse Out												
	t_{pd+}	2, 6	-	-	25	75	-	-	ns	-	-	25	75	-	-	ns	2	6	-	-	-	-	14	-	-	-	-	-	-	7
	t_{pd-}	2, 6	-	-	35	75	-	-	ns	-	-	35	75	-	-	ns	2	6	-	-	-	-	14	-	-	-	-	-	-	7

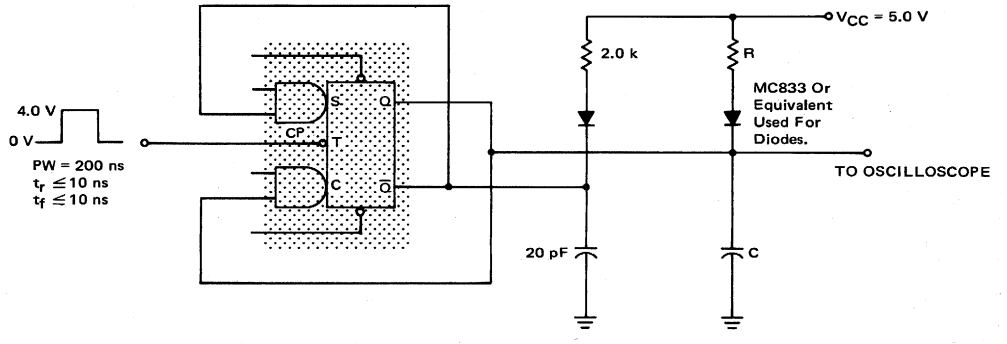
Pins not listed are left open.

§ CP_a = Clock Pulse a
CP_b = Clock Pulse b
CP_c = Clock Pulse c
} See Clock Pulse Waveforms.

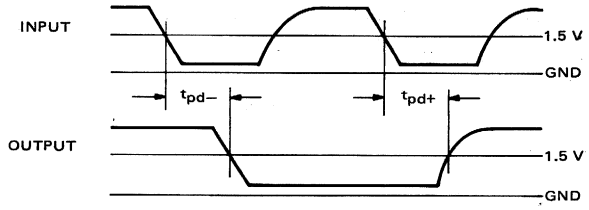
† Momentarily ground this terminal before applying -0.12 mA.

‡ Momentarily ground this terminal before applying I_{OL} to complementary terminal, i.e., terminal of opposite function.

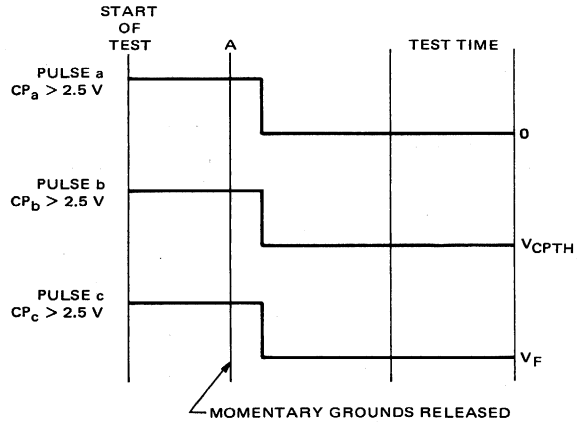
PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	30 pF



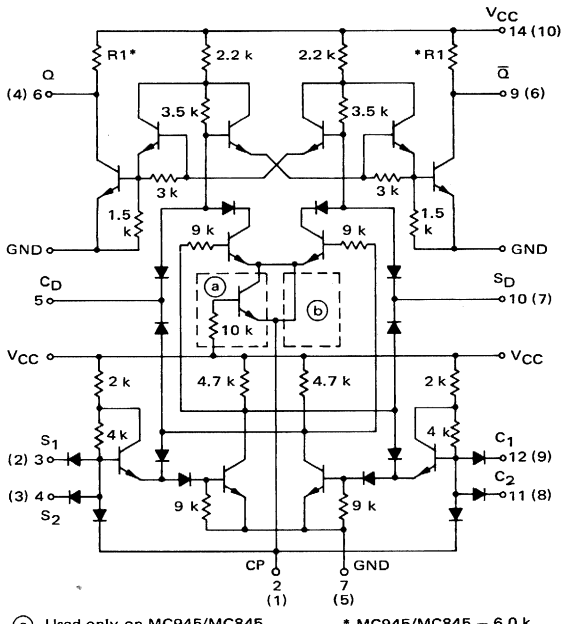
CLOCK PULSE WAVEFORMS
($t_f < 1.0\ \mu s$)



TEST CONDITIONS

	V_{CPTH}
	MC931
−55°C	1.10 V
+25°C	0.95 V
+125°C	0.75 V
	MC831
0°C	1.00 V
+25°C	0.95 V
+75°C	0.85 V

MC945F, G · MC845F, P, G
MC948F, G · MC848F, P, G



(a) Used only on MC945/MC845

(b) Used only on MC948/MC848

* MC945/MC845 – 6.0 k
MC948/MC848 – 2.0 k

Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

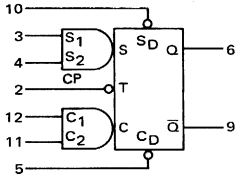
These clocked flip-flops consist of two directly coupled flip-flops, operating on the "master-slave" principle. The input information is stored in the "master" flip-flop when the clock voltage is high, and is transferred to the "slave" when the clock voltage is low.

This clocked flip-flop can be operated in either the R-S or J-K mode. For J-K operation the Q output is connected to a clear input, and the $\overline{Q}$ output is connected to a set input. Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs. No matter what other inputs are applied to the flip-flop, the direct set and clear inputs prevail.

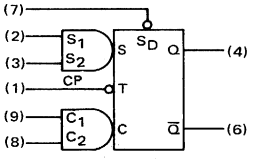
The outputs are buffered, thereby reducing the possibility of circuit disturbance from external line noise.

The output pull-up resistor of the MC948/MC848 has been changed from that utilized in the MC945/MC845 in order to improve the propagation delay-versus-capacitance characteristics.

MC945F/MC845F, P
MC948F/MC848F, P



MC945G/MC845G
MC948G/MC848G



Input Loading Factor:
S and C = 2/3
S_D, C_D, T = 2

Output Loading Factor:
MC945 = 10
MC845 = 12
MC948 = 9
MC848 = 11

Total Power Dissipation:
MC945/MC845 = 60 mW typ/pkg
MC948/MC848 = 70 mW typ/pkg

Propagation Delay Time = 40 ns typ

SYNCHRONOUS TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

0 – Low State (more negative)

1 – High State (more positive)

X – State of the input does not affect the state of the circuit.

U – Indeterminate State

J-K TRUTH TABLE
(Connect S_2 to $\overline{Q}$, C_2 to Q)

t_n		t_{n+1}
S_1	C_1	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

ASYNCHRONOUS TRUTH TABLE

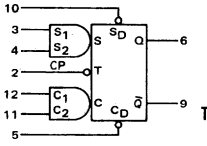
S_D	C_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs.

ELECTRICAL CHARACTERISTICS

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	–	2	3	4	5	6	7	–	9	10	11	12	–	14
Metal Can	–	1	2	3	–	4	5	–	6	7	8	9	–	10



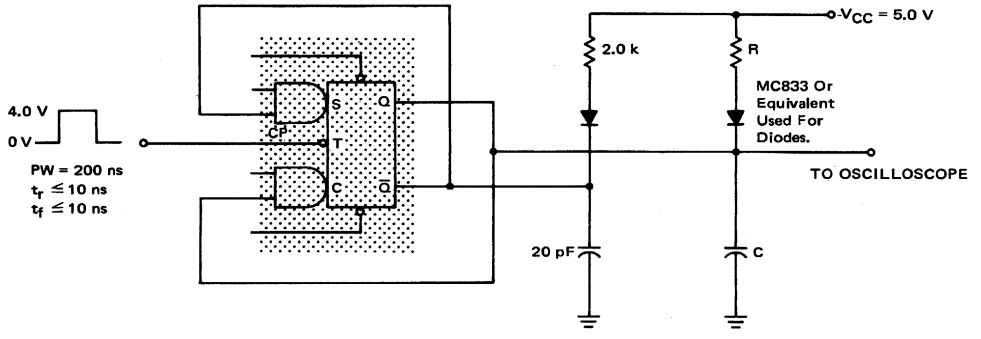
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES												
	mA				Volts								
	I_{OL}		I_{OH}		V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	
	MC945	MC948	MC945	MC948									
MC945, MC948 −55°C	14.6	13.0	-0.12	-0.5	1.40	2.10	0	4.00	-	4.50	5.50	-	
MC945, MC948 +25°C	15.2	13.6	-0.12	-0.5	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00	
MC945, MC948 +125°C	13.8	12.3	-0.12	-0.5	0.80	2.00	0	4.00	-	4.50	5.50	-	
	MC845	MC848	MC845	MC848									
MC845, MC848 0°C	16.8	15.4	-0.12	-0.5	1.20	2.00	0.45	4.00	-	5.00	5.00	-	
MC845, MC848 +25°C	16.8	15.4	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00	
MC845, MC848 +75°C	16.0	14.6	-0.12	-0.5	0.95	1.80	0.50	4.00	-	5.00	5.00	-	

Characteristic	Symbol	Pin Under Test	MC945, MC948 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC845, MC848 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	CP_a§	CP_b§	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	-	-	-	-	14	-	-	-	2	3,7
		9	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		9	-	-	-	-	-	-		-	-	-	2	7,12
	V_{OH}	6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	11	3,4	-	-	-		-	-	2	-	7
		↓		-		-		-			-		-		-		-	↓	12	3,4	-	-	-		-	-		-	7
				-		-		-			-		-		-		-		10	5	-	-	-		-	-		-	3,4,7
		9		-		-		-			-		-		-		-	9	3	11,12	-	-	-		-	-		-	7
		↓		-		-		-			-		-		-		-	↓	4	11,12	-	-	-		-	-		-	7
				-		-		-			-		-		-		-		5	10	-	-	-		-	-		-	7,11,12
Reverse Current	I_R	3	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	3	-	-	14	-	-	-	2,7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	↓	-	-	-	2,7
		5	-		-		-			-		-		-			-	-	-	-	-	5	-	-		-	2	-	3,4,7
		10	-		-		-			-		-		-			-	-	-	-	-	10	-	-		-	2	-	7,11,12
		11	-		-		-			-		-		-			-	-	-	-	-	11	-	-		-	-	-	2,7
		12	-		-		-			-		-		-			-	-	-	-	-	12	-	-		-	-	-	2,7
	I_{RCP}	2	-	20	-	20	-	30		-	30	-	30	-	40		-	-	-	-	-	2	-	-		-	-	-	3,4,7,11,12
Forward Current	2/3 I_F	3	-	-1.07	-	-1.07	-	-1.00	mAdc	-	-0.95	-	-0.95	-	-0.90	mAdc	-	-	-	-	3	-	-	-	14	-	-	-	7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	4	-	-	-	↓	-	-	-	↓
		11	-		-		-			-		-		-			-	-	-	-	11	-	-	-		-	-	-	
		12	-		-		-			-		-		-			-	-	-	-	12	-	-	-		-	-	-	
	I_{FCP}	2	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	5	-	2	-	-	-		-	-	-	7
	I_{FCP}	2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	10	-	2	-	-	-		-	-	-	7
	I_{FS}	5	-		-		-			-		-		-			-	-	-	-	5	-	-	-		-	-	-	3,7,10,12
	I_{FS}	10	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	10	-	-	-	↓	-	-	-	4,5,7,11
Power Drain Current																													
MC945/MC845	I_{PDH}	14	-	-	-	11	-	-	mAdc	-	-	-	14	-	-	mAdc	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	14.5	-	-	↓	-	-	-	18	-	-	↓	-	-	-	-	-	-	-	-	-	14	-	-	2,3,4,7,11,12
MC948/MC848	I_{PDH}	14	-	-	-	13.5	-	-		-	-	-	17	-	-		-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	19	-	-	↓	-	-	-	22.5	-	-	↓	-	-	-	-	-	-	-	-	-	14	-	-	2,3,4,7,11,12
Switching Times																	Pulse In	Pulse Out											
MC945/MC845	t_{pd+}	2,6	-	-	25	100	-	-	ns	-	-	25	100	-	-	ns	2	6	-	-	-	-	14	-	-	-	-	-	7
	t_{pd-}	2,6	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓	↓	↓	-	-	-	-	↓	-	-	-	-	-	↓
MC948/MC848	t_{pd+}	2,6	-	-	25	75	-	-		-	-	25	75	-	-				-	-	-	-		-	-	-	-	-	
	t_{pd-}	2,6	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓			-	-	-	-	↓	-	-	-	-	-	↓

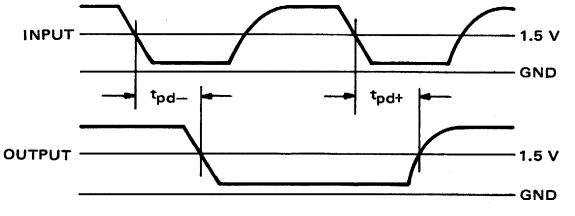
Pins not listed are left open.

§ CP_a = Clock Pulse a
CP_b = Clock Pulse b
} See Clock Pulse Waveforms.

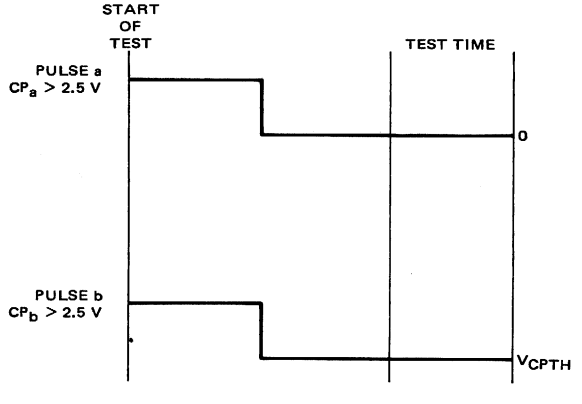
PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	30 pF



CLOCK PULSE WAVEFORMS
($t_f < 1.0\ \mu s$)



TEST CONDITIONS

	V_{CPTH}	
	MC945	MC948
−55°C	1.15 V	1.30 V
+25°C	0.95 V	1.15 V
+125°C	0.65 V	0.85 V
	MC845	MC848
0°C	1.00 V	1.20 V
+25°C	0.95 V	1.15 V
+75°C	0.65 V	0.85 V

MC952F · MC852F, P
MC953F · MC853F, P
MC955F · MC855F, P
MC956F · MC856F, P

Each section of the monolithic MC952/MC852 and MC953/MC853 dual J-K clocked flip-flops consists of two directly-coupled flip-flops operating on the "master-slave" principle. Operation depends only on voltage levels, so the rise and fall times of the input clock are unimportant in determining the state of the flip-flop. Input information is stored in the "master" flip-flop when the clock voltage is high and is transferred to the "slave" when the clock voltage goes low.

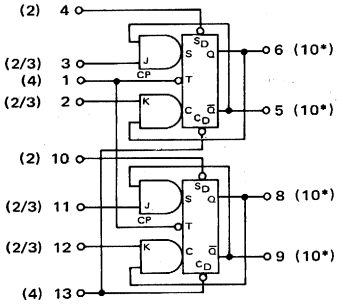
The MC952/MC852 has a common clock input which makes this device suitable for clocked counters and shift register applications. A common direct clear (C_D) and separate direct sets (S_D) are available. The direct inputs override all synchronous inputs.

The MC953/MC853 has separate clock inputs to each flip-flop, which makes the device suitable for ripple counter applications. Separate direct set inputs which override the synchronous inputs are also provided.

The outputs of the flip-flops are buffered, thereby reducing the possibility of circuit disturbance from external line noise.

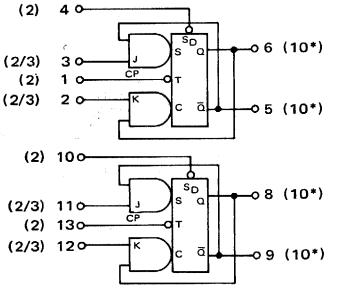
Total Power Dissipation
MC952/MC852, MC953/MC853
= 120 mW typ/pkg
MC955/MC855, MC956/MC856
= 140 mW typ/pkg
Propagation Delay Time = 40 ns typ

MC952/MC852



* 12 for MC852

MC953/MC853



* 12 for MC853

Number in parenthesis indicates loading.

ASYNCHRONOUS TRUTH TABLE
MC952/MC852 and MC955/MC855

S_D	C_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

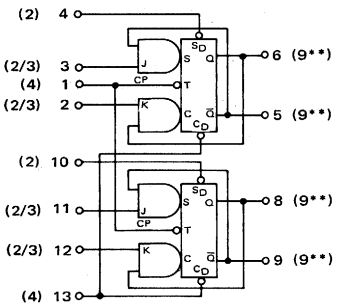
Each section of the monolithic MC955/MC855 and MC956/MC856 dual J-K clocked flip-flops consists of two directly-coupled flip-flops operating on the "master-slave" principle. Input information is stored in the "master" flip-flop when the clock voltage is high and is transferred to the "slave" when the clock voltage goes low.

The MC955/MC855 has a common clock input which makes this device suitable for clocked counters and shift register applications. A common direct clear (C_D) and separate direct sets (S_D) are available. The direct inputs override all synchronous inputs.

The MC956/MC856 has separate clock inputs to each flip-flop, which makes the device suitable for ripple counter applications. Separate direct set inputs which override the synchronous inputs are also provided.

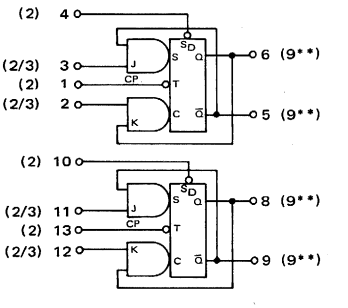
The outputs of the flip-flops are buffered, thereby reducing the possibility of circuit disturbance from external line noise. The output pull-up resistor has been changed from that utilized in the MC952/MC852 and MC953/MC853 in order to improve the propagation delay versus capacitance characteristics.

MC955/MC855



** 11 for MC855

MC956/MC856



** 11 for MC856

Number in parenthesis indicates loading.

ASYNCHRONOUS TRUTH TABLE
MC953/MC853 and MC956/MC856

S_D	Q	$\overline{Q}$
1	NC	NC
0	1	0

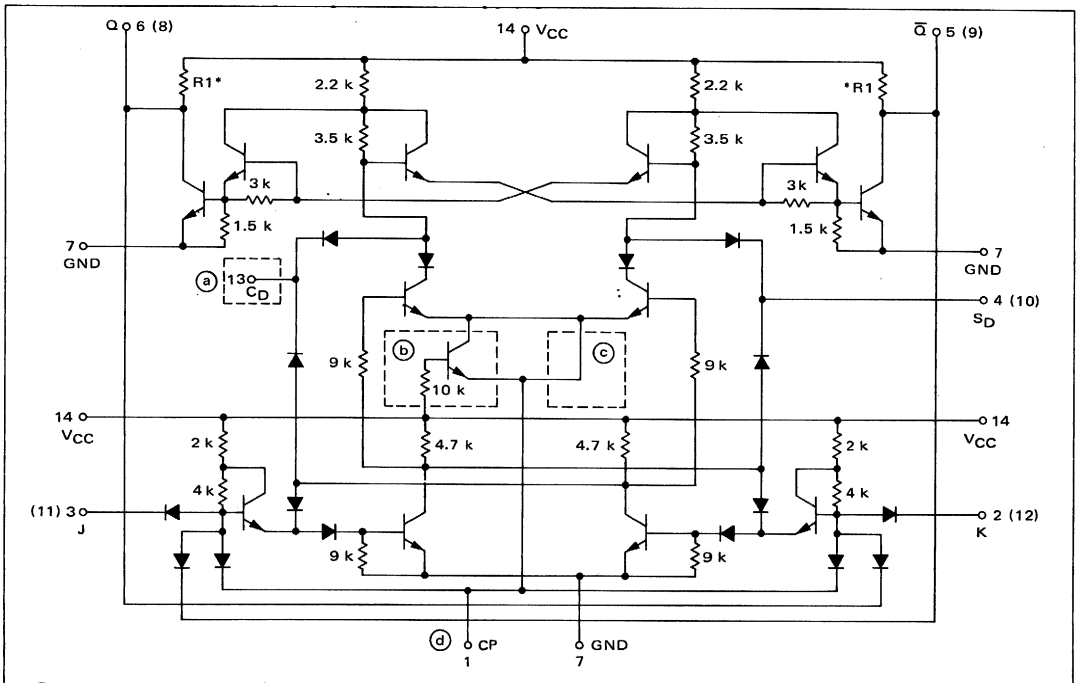
J-K TRUTH TABLE — All Types †

t_n		t_{n+1}
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs.

†Valid only when J and K inputs remain unchanged during period while CP is high.

CIRCUIT SCHEMATIC (½ of circuit shown)

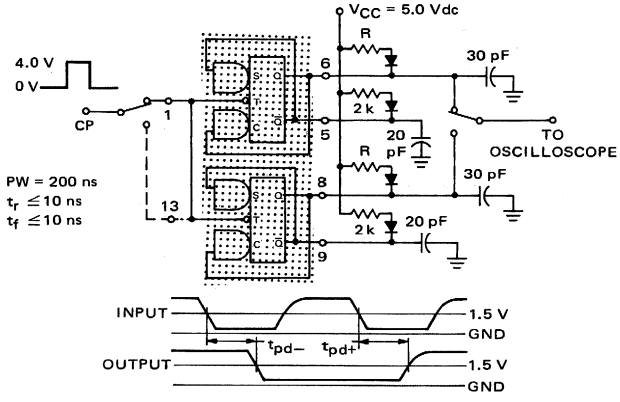


(a) Used only on MC952/MC852 and MC955/MC855
(b) Used only on MC952/MC852 and MC953/MC853
(c) Used only on MC955/MC855 and MC956/MC856
(d) Pin 13 used for other side of MC953/MC853 and MC956/MC856

NOTE: Number in parenthesis indicates pin number for other half of the schematic. Ground and V_{CC} pins are common to both sides.

* MC952/MC852 and MC953/MC853 — 6 k
MC955/MC855 and MC956/MC856 — 2 k

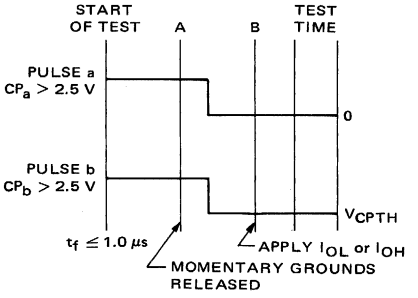
PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



Test circuit shown for MC952/MC852 and MC955/MC855.
Use dotted-line connection for MC953/MC853 and MC956/MC856, which have separate toggle inputs.
Ground pin 7. Only connected inputs are shown. All others are open.
MC833 or equivalent used for diodes.

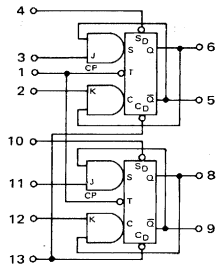
TEST	R
t_{pd+}	3.9 k ohms
t_{pd-}	400 ohms

CLOCK PULSE WAVEFORMS



TEST CONDITIONS

T_A	V_{CPTH}	
	MC952, MC953	MC955, MC956
−55°C	1.15 V	1.30 V
+25°C	0.95 V	1.15 V
+125°C	0.65 V	0.85 V
	MC852, MC853	MC855, MC856
0°C	1.00 V	1.20 V
+25°C	0.95 V	1.15 V
+75°C	0.65 V	0.85 V



MC952/MC852
MC955/MC855
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC952, MC955 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC852, MC855 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Output Voltage	V_{OL}	5	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc
		6	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	
		8	-		-		-			-		-		-		
		9	-		-		-			-		-		-		
	V_{OH}	5	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-	
		5		-		-		-			-		-		-	
		6		-		-		-			-		-		-	
		6		-		-		-			-		-		-	
		8		-		-		-			-		-		-	
		8		-		-		-			-		-		-	
		9		-		-		-			-		-		-	
		9		↓		↓		↓			↓		↓		↓	
Short-Circuit Current MC952/MC852	I_{SC}	5	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc
		6		↓		↓		↓			↓		↓		↓	
		8														
		9														
MC955/MC855		5	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10		-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	
		6		↓		↓		↓			↓		↓		↓	
		8														
		9														
Reverse Current All Types	I_R	2	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc
		3	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	
		4	-		-		-			-		-		-		
		10	-		-		-			-		-		-		
		11	-		-		-			-		-		-		
		12	-		-		-			-		-		-		
All Types	$2\,I_R$	13	-	4.0	-	4.0	-	10		-	10	-	10	-	20	
MC952/MC852	$2\,I_{RCP}$	1	-	20	-	20	-	40		-	40	-	40	-	60	
MC955/MC855	$2\,I_{RCP}$	1	-	20	-	20	-	40		-	40	-	40	-	60	
Forward Current	$2/3\,I_F$	2	-	-1.07	-	-1.07	-	-1.00	mAdc	-	-0.95	-	-0.95	-	-0.90	mAdc
		3	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	
		11	-		-		-			-		-		-		
		12	-		-		-			-		-		-		
	$2\,I_{FCP}$	1	-	-6.40	-	-6.40	-	-6.00		-	-5.60	-	-5.60	-	-5.34	
		1	-	-6.40	-	-6.40	-	-6.00		-	-5.60	-	-5.60	-	-5.34	
	I_{FS}	4	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67	
		10	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67	
	$2\,I_{FS}$	13	-	-6.40	-	-6.40	-	-6.00		-	-5.60	-	-5.60	-	-5.34	
Power Drain Current																
MC952/MC852	I_{PDH}	14	-	-	-	22	-	-	mAdc	-	-	-	28	-	-	mAdc
	I_{max}	14	-	-	-	32	-	-		-	-	-	36	-	-	
MC955/MC855	I_{PDH}	14	-	-	-	27	-	-		-	-	-	34	-	-	
	I_{max}	14	-	-	-	38	-	-		-	-	-	45	-	-	
Switching Times																
MC952/MC852	t_{pd+}	1, 6	-	-	25	100	-	-	ns	-	-	25	100	-	-	ns
	t_{pd-}	1, 6	-	-	15	55	-	-		-	-	15	55	-	-	
	t_{pd+}	1, 8	-	-	25	100	-	-		-	-	25	100	-	-	
	t_{pd-}	1, 8	-	-	15	55	-	-		-	-	15	55	-	-	
MC955/MC855	t_{pd+}	1, 6	-	-	25	75	-	-		-	-	25	75	-	-	
	t_{pd-}	1, 6	-	-	15	55	-	-		-	-	15	55	-	-	
	t_{pd+}	1, 8	-	-	25	75	-	-		-	-	25	75	-	-	
	t_{pd-}	1, 8	-	-	15	55	-	-		-	-	15	55	-	-	

Pins not listed are left open.

§ CP_a = Clock Pulse a, CP_b = Clock Pulse b } See Clock Pulse Waveforms.

† Applied after Clock Pulse.

‡ Momentary Ground.

@ Test Temperature		I_{OL} mA		I_{OH} mA		V_{IL} Volts	V_{IH} Volts	V_F Volts	V_R Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts	V_{max} Volts
		MC952	MC955	MC952	MC955								
MC952, MC955	−55°C	14.6	13.0	-0.12	-0.5	1.40	2.10	0	4.00	-	4.50	5.50	-
	+25°C	15.2	13.6	-0.12	-0.5	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	13.8	12.3	-0.12	-0.5	0.80	2.00	0	4.00	-	4.50	5.50	-
		MC852	MC855	MC852	MC855								
MC852, MC855	0°C	16.8	15.4	-0.12	-0.5	1.20	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	16.8	15.4	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	16.0	14.6	-0.12	-0.5	0.95	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	CP_a§	CP_b§	Gnd
Output Voltage	V_{OL}	5	5†	-	2	-	-	-	-	14	-	-	-	1	7,13‡
		6	6†	-	3	-	-	-	-		-	-	-		4‡,7
		8	8†	-	11	-	-	-	-		-	-	-		7,10‡
		9	9†	-	12	-	-	-	-		-	-	-		7,13†
	V_{OH}	5		5†	3	2	-	-	-		-	-	1	-	4‡,7
		5		5	2,13	4	-	-	-		-	-		-	7
		6		6†	2	3	-	-	-		-	-		-	7,13‡
		6		6	3,4	13	-	-	-		-	-		-	7
		8		8†	12	11	-	-	-		-	-		-	7,13‡
		8		8	10,11	13	-	-	-		-	-		-	7
		9		9†	11	12	-	-	-		-	-		-	7,10‡
		9		9	12,13	10	-	-	-		-	-		-	7
Short-Circuit Current MC952/MC852	I_{SC}	5	-	-	-	-	-	-	-	-	14	-	-	1	5,7
		6	-	-	-	-	-	-	-	-		-	-		6,7
		8	-	-	-	-	-	-	-	-		-	-		7,8
		9	-	-	-	-	-	-	-	-		-	-		7,9
MC955/MC855		5	-	-	-	-	-	-	-	-		-	-		5,7
		6	-	-	-	-	-	-	-	-		-	-		6,7
		8	-	-	-	-	-	-	-	-		-	-		7,8
		9	-	-	-	-	-	-	-	-		-	-		7,9
Reverse Current All Types	I_R	2	-	-	-	-	-	2	-	-	14	-	-	-	1,7
		3	-	-	-	-	-	3	-	-		-	-		1,7
		4	-	-	-	-	-	4	-	-		-	1	-	2,6,7
		10	-	-	-	-	-	10	-	-		-	1	-	7,8,12
		11	-	-	-	-	-	11	-	-		-	-	-	1,7
		12	-	-	-	-	-	12	-	-		-	-	-	1,7
All Types	$2\,I_R$	13	-	-	-	-	-	13	-	-		-	1	-	3,5,7,9,11
MC952/MC852	$2\,I_{RCP}$	1	-	-	-	-	-	1,14	-	-	-	-	-	-	2,3,5,6,7,8, 9,11,12
MC955/MC855	$2\,I_{RCP}$	1	-	-	-	-	-	1	-	-	14	-	-	-	2,3,5,6,7,8, 9,11,12
Forward Current	$2/3\,I_F$	2	-	-	-	-	2	-	-	-	14	-	-	1	7
		3	-	-	-	-	3	-	-	-		-	-		
		11	-	-	-	-	11	-	-	-		-	-		
		12	-	-	-	-	12	-	-	-		-	-		
	$2\,I_{FCP}$	1	-	-	4,10	-	1	-	-	-		-	-	-	
		1	-	-	13	-	1	-	-	-		-	-	-	
	I_{FS}	4	-	-	-	-	4	-	-	-		-	-	-	2,3,7,13
		10	-	-	-	-	10	-	-	-		-	-	-	7,11,12,13
	$2\,I_{FS}$	13	-	-	-	-	13	-	-	-		-	-	-	2,3,4,7, 10,11,12
Power Drain Current															
MC952/MC852	I_{PDH}	14	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7, 10,11,12
MC955/MC855	I_{PDH}	14	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7, 10,11,12
Switching Times			Pulse In	Pulse Out											
MC952/MC852	t_{pd+}	1,6	1	6	-	-	-	-	14	-	-	-	-	-	7
	t_{pd-}	1,6		6	-	-	-	-		-	-	-	-	-	
	t_{pd+}	1,8		8	-	-	-	-		-	-	-	-	-	
	t_{pd-}	1,8		8	-	-	-	-		-	-	-	-	-	
MC955/MC855	t_{pd+}	1,6		6	-	-	-	-		-	-	-	-	-	
	t_{pd-}	1,6		6	-	-	-	-		-	-	-	-	-	
	t_{pd+}	1,8		8	-	-	-	-		-	-	-	-	-	
	t_{pd-}	1,8		8	-	-	-	-		-	-	-	-	-	

Pins not listed are left open.

§ CP_a = Clock Pulse a, CP_b = Clock Pulse b } See Clock Pulse Waveforms.

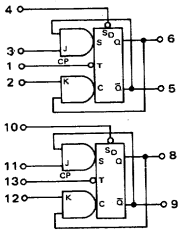
† Applied after Clock Pulse.

‡ Momentary Ground.

MC953/MC853
MC956/MC856

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



@ Test Temperature		I_{OL} mA MC953	I_{OL} mA MC956	I_{OH} mA MC953	I_{OH} mA MC956	V_{IL} Volts	V_{IH} Volts	V_F Volts	V_R Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts	V_{max} Volts
MC953, MC956	−55°C	14.6	13.0	-0.12	-0.5	1.40	2.10	0	4.00	-	4.50	5.50	-
	+25°C	15.2	13.6	-0.12	-0.5	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	13.8	12.3	-0.12	-0.5	0.80	2.00	0	4.00	-	4.50	5.50	-
		MC853	MC856	MC853	MC856								
MC853, MC856	0°C	16.8	15.4	-0.12	-0.5	1.20	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	16.8	15.4	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	16.0	14.6	-0.12	-0.5	0.95	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC953, MC956 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC853, MC856 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	CP_a§	CP_b§	Gnd
Output Voltage	V_{OL}	5	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	5	-	4	-	-	-	-	14	-	-	-	-	7
		6	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		6†	-	3	-	-	-	-		-	-	-	1.	4‡ 7
	V_{OH}	5	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	5†	3	2	-	-	-		-	-	1	-	4‡,7
		6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	3,4	-	-	-	-		-	-	1	-	7
Short-Circuit Current MC953/MC853	I_{SC}	5	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc	-	-	-	-	-	-	-	-	14	-	-	1	5,7
		6	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00		-1.25	-2.50	-1.15	-2.30	-1.05	-2.15		-	-	-	-	-	-	-	-		-	-		6,7
MC956/MC856		5	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10		-2.60	-5.20	-2.35	-4.75	-2.20	-4.40		-	-	-	-	-	-	-	-		-	-	-	5,7
		6	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10		-2.60	-5.20	-2.35	-4.75	-2.20	-4.40		-	-	-	-	-	-	-	-		-	-		6,7
Reverse Current All Types	I_R	2	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	2	-	-	14	-	-	-	1,7
		3	-		-		-			-		-		-			-	-	-	-	-	3	-	-		-	-	-	1,7
		4	-		-		-			-		-		-			-	-	-	-	-	4	-	-		-	-	-	2,6,7
MC953/MC853	I_{RCP}	1	-	10	-	10	-	20		-	20	-	20	-	30		-	-	-	-	-	1,14	-	-	-	-	-	-	2,3,5,6,7
MC956/MC856	I_{RCP}	1	-	10	-	10	-	20		-	20	-	20	-	30		-	-	-	-	-	1	-	-	14	-	-	-	2,3,5,6,7
Forward Current	$2/3\ I_F$	2	-	-1.07	-	-1.07	-	-1.00	mAdc	-	-0.95	-	-0.95	-	-0.90	mAdc	-	-	-	-	2	-	-	-	14	-	-	1	7
	$2/3\ I_F$	3	-	-1.07	-	-1.07	-	-1.00		-	-0.95	-	-0.95	-	-0.90		-	-	-	-	3	-	-	-		-	-	1	
	I_{FCP}	1	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	4	-	1	-	-	-		-	-	-	
	I_{FS}	4	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	-	-	4	-	-	-		-	-	-	3,7
Power Drain Current (Total Device) MC953/MC853	I_{PDH}	14	-	-	-	22	-	-	mAdc	-	-	-	28	-	-	mAdc	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	32	-	-		-	-	-	36	-	-		-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7,10, 11,12,13
MC956/MC856	I_{PDH}	14	-	-	-	27	-	-		-	-	-	34	-	-		-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	38	-	-		-	-	-	45	-	-		-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7,10, 11,12,13
Switching Times																	Pulse In	Pulse Out											
MC953/MC853	t_{pd+}	1,6	-	-	25	100	-	-	ns	-	-	25	100	-	-	ns	1	6	-	-	-	-	14	-	-	-	-	-	7
	t_{pd-}	1,6	-	-	15	55	-	-		-	-	15	55	-	-				-	-	-	-		-	-	-	-	-	
MC956/MC856	t_{pd+}	1,6	-	-	25	75	-	-		-	-	25	75	-	-				-	-	-	-		-	-	-	-	-	
	t_{pd-}	1,6	-	-	15	55	-	-		-	-	15	55	-	-				-	-	-	-		-	-	-	-	-	

Pins not listed are left open.

§ CP_a = Clock Pulse a
CP_b = Clock Pulse b
} See Clock Pulse Waveforms.

† Applied after Clock Pulse.
‡ Momentary ground.

MC950F, G • MC850F, P, G

The MC950/MC850 high-speed gated flip-flop utilizes capacitive coupling of the pulse-triggered set and clear inputs. Directly coupled set and clear inputs are available as well as direct set and clear inputs that respond to dc levels and override the clocked inputs. Separate clock signals may be applied to the capacitively coupled inputs or they may be tied together to obtain single-channel triggering operation. Maximum toggle frequency is typically 40 MHz at 25°C with power dissipation on the order of 30 mW.

Typical applications include binary ripple counters, shift registers, and similar applications. It may be used to advantage in high-speed portions of digital systems that are presently using MDTL circuitry.

SYNCHRONOUS TRUTH TABLE

t_n				$t_n + 1$
S_1	S_2	C_1	C_2	Q
0	0	0	0	U
1	X	1	X	Q_n
X	1	X	1	Q_n
0	1	1	0	Q_n
0	0	X	1	1
0	0	1	X	1
1	X	0	0	0
X	1	0	0	0

SINGLE TRIGGER TRUTH TABLE

(Pins S_2 and C_1 tied together)

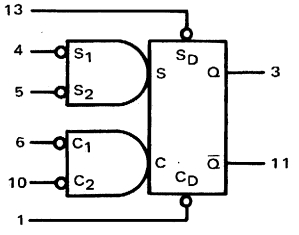
t_n		$t_n + 1$
S_1	C_2	Q
0	0	U
1	0	0
0	1	1
1	1	Q_n

ASYNCHRONOUS TRUTH TABLE

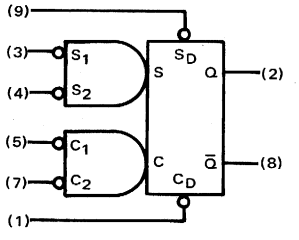
S_D	C_D	Q	$\bar{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

0 = low state (more negative)
1 = high state (more positive)
X = don't care
U = indeterminate state
NC = no change

MC950F/MC850F, P



MC950G/MC850G

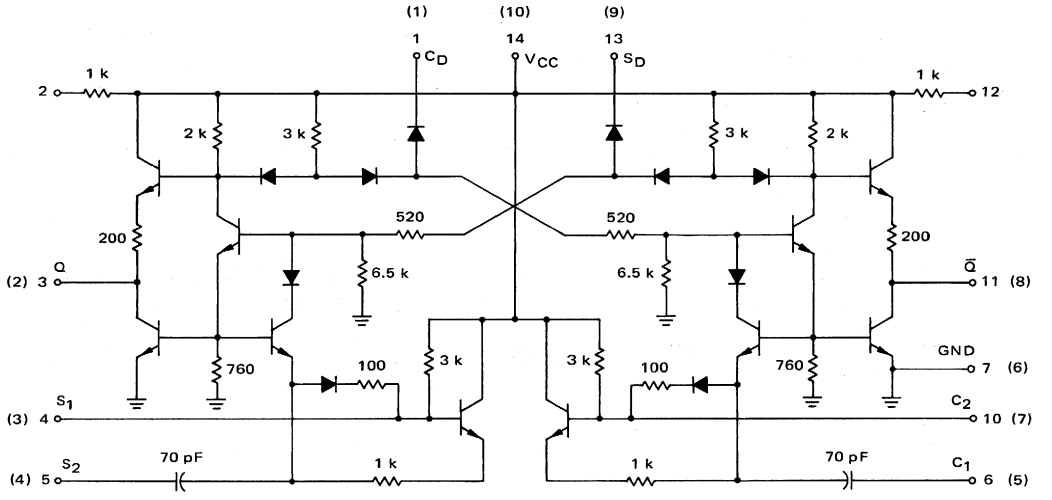


Input Loading Factor
S_D, S_1, C_D, C_2 = 1.5
S_2, C_1 = 100 pF

Output Loading Factor
MC950 = 8
MC850 = 10

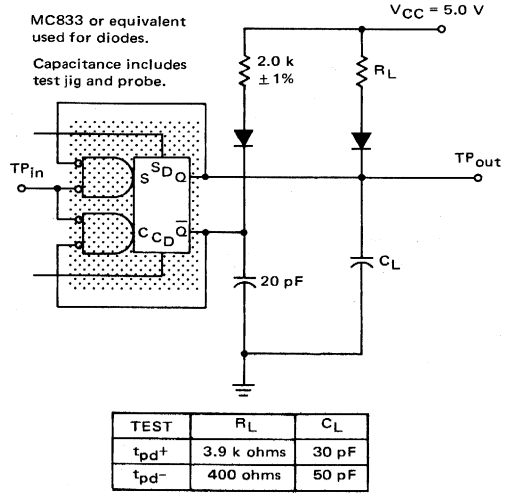
Total Power Dissipation = 50 mW typ/pkg
Propagation Delay Time = 15 ns typ

CIRCUIT SCHEMATIC

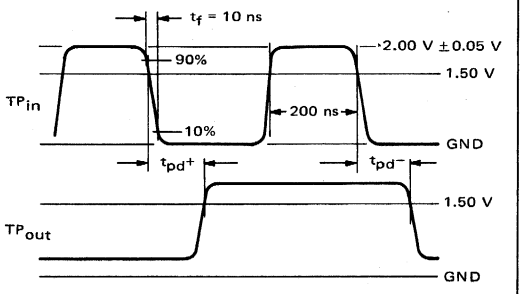


Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



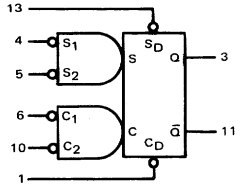
TEST	R_L	C_L
t_{pd^+}	3.9 k ohms	30 pF
t_{pd^-}	400 ohms	50 pF



ELECTRICAL CHARACTERISTICS

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	-	-	10	11	12	13	14
Metal Can	1	-	2	3	4	5	6	-	-	7	8	-	9	10

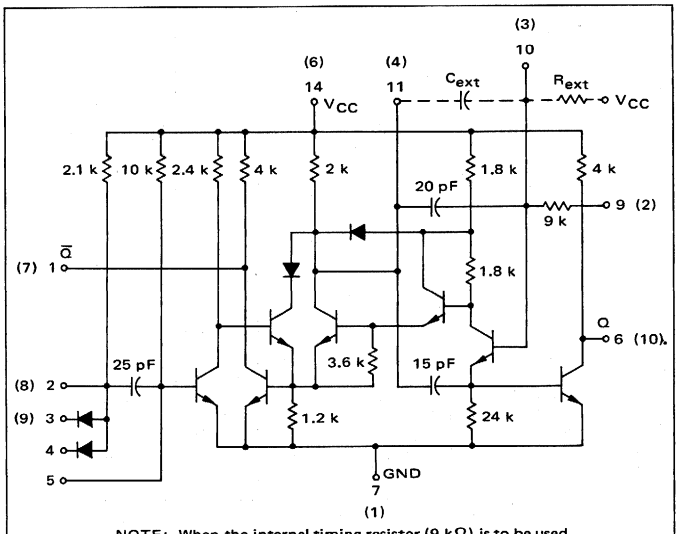


@ Test Temperature		TEST CURRENT / VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_F	Volts V_R	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_{max}
MC950	−55°C	11.4	-1.50	0	4.00	-	-	4.50	5.50	-
	+25°C	12.0	-1.50	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	10.8	-1.50	0	4.00	-	-	4.50	5.50	-
MC850	0°C	14.0	-1.50	0.45	4.00	-	-	5.00	5.00	-
	+25°C	14.0	-1.50	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	13.3	-1.50	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC950 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC850 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	3	-	-	-	-	-	14	-	-	1,7
		11	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		11	-	-	-	-	-		-	-	7,13
	V_{OH}	3	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	3	-	-	-	-		-	-	7,13*
		11	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	11	-	-	-	-		-	-	1*, 7
Short-Circuit Current	I_{SC}	3	-11.5	-	-14.0	-	-13.0	-	mAdc	-12.6	-	-13.7	-	-12.6	-	mAdc	-	-	-	-	-	-	-	14	-	3,7,13
		11	-11.5	-	-14.0	-	-13.0	-	mAdc	-12.6	-	-13.7	-	-12.6	-	mAdc	-	-	-	-	-	-	-	14	-	1,7,11
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	1	-	-	-	14	-	7
		13	-	2.0	-	2.0	-	5.0		-	5.0	-	5.0	-	10		-	-	-	13	-	-	-		-	7
	I_{RCP}	5	-	20	-	20	-	30		-	30	-	30	-	40		-	-	-	5	-	-	-		-	4,7,10
		6	-	20	-	20	-	30		-	30	-	30	-	40		-	-	-	6	-	-	-		-	4,7,10
Output Leakage Current	I_{CEX}	3	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	3,14	-	-	-	-	7,13*
		11	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	11,14	-	-	-	-	1*,7
Forward Current	$1.5\ I_F$	1	-	-2.40	-	-2.40	-	-2.25	mAdc	-	-2.20	-	-2.20	-	-2.10	mAdc	-	-	1	13	-	-	-	14	-	7
		4	-		-		-			-		-		-			-	-	4	10	-	-	-		-	
		10	-		-		-			-		-		-			-	-	10	4	-	-	-		-	
		13	-		-		-			-		-		-			-	-	13	1	-	-	-		-	
	I_2	2	-	-	-4.60	-6.90	-	-		-	-	-3.85	-7.15	-	-		-	-	-	-	-	-	-		-	2,7
	I_{12}	12	-	-	-4.60	-6.90	-	-		-	-	-3.85	-7.15	-	-		-	-	-	-	-	-	-		-	7,12
Power Drain Current	I_{PDH}	14	-	-	-	9.0	-	-	mAdc	-	-	-	10	-	-	mAdc	-	-	-	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	14	-	-	mAdc	-	-	-	16	-	-	mAdc	-	-	-	-	-	-	-	-	14	1,7,13
Switching Times																	Pulse In	Pulse Out								
	t_{pd}^+	5, 6, 3	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	5, 6	3	-	-	-	14	-	-	-	7
	t_{pd}^-	5, 6, 3	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	5, 6	3	-	-	-	14	-	-	-	7

Pins not listed are left open.
*Momentarily ground this terminal before taking measurement.

MC951F, G • MC851F, P, G



NOTE: When the internal timing resistor (9 kΩ) is to be used, connect Pin 9 to Pin 14 (flat and dual in-line packages) or pins 2 and 6 (can). DO NOT MAKE THIS CONNECTION IF USING THE EXTERNAL CAPACITOR AND RESISTOR.

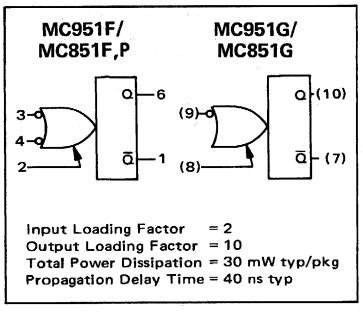
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

Maximum permissible current into Pin 9 (2) = 10 mAdc.

The MC951/MC851 is a monolithic monostable multivibrator circuit which gives complementary output pulses upon the dynamic zero transition of the input waveform. The output pulse width is determined by an R-C timing circuit and, due to differentiation of the input, is essentially independent of the input pulse width. With internal components, nominal pulse width is 100 ns.

Provisions are available to increase the pulse width by adding external capacitance and to increase pulse width stability by utilizing a precision external resistor in place of the internal charging resistor.

Typical applications include analog comparators, elimination of transients on pulse waveforms, and provision for delays to insure the proper sequence of digital operations in computer applications.



Input Loading Factor = 2
Output Loading Factor = 10
Total Power Dissipation = 30 mW typ/pkg
Propagation Delay Time = 40 ns typ

APPLICATIONS INFORMATION

OUTPUT PULSE WIDTH

EXTERNAL COMPONENTS USED	INTERNAL RESISTOR CONNECTION	PULSE WIDTH ns (APPROX)
None	Pin 9 to V_{CC}	100
C_{ext} (between Pins 10 & 11)	Pin 9 to V_{CC}	4.5 (C_{ext} + 20)
R_{ext} (between Pin 10 & V_{CC}) (9 kΩ min, 15 kΩ max)	Pin 9 open	0.5 R_{ext} (C_{ext} + 20)

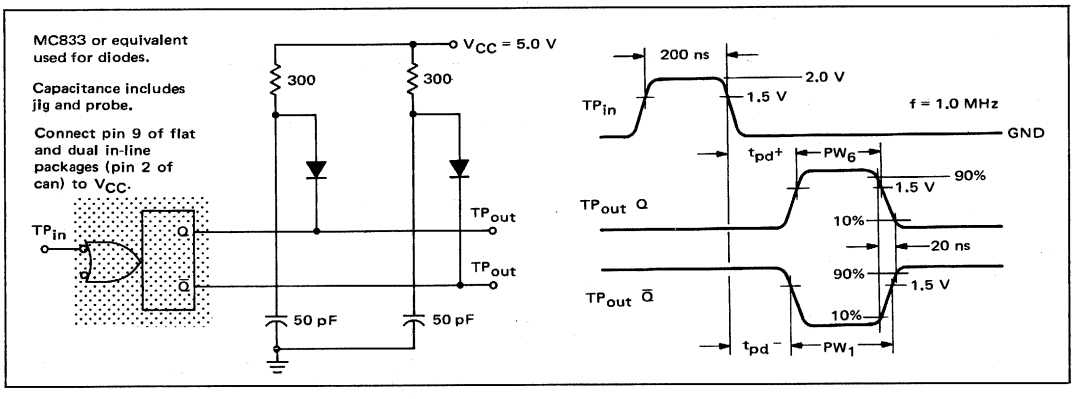
Capacitance values in pF, Resistance values in kΩ
Pin numbers shown for devices in flat and dual in-line packages.

MAXIMUM INPUT FALL TIME TO TRIGGER

t_f ns	VOLTAGE SWING VOLTS
25	1.0
50	2.0
100	4.0

Output duty cycle ≤ 40%. Higher duty cycles obtainable at a possible decrease of performance.

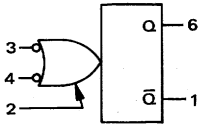
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	–	9	10	11	–	–	14
Metal Can	7	8	9	–	–	10	1	–	2	3	4	–	–	6



	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_F	Volts V_R	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_{max}
MC951	−55°C	15.0	-0.18	0	4.00	–	4.50	5.50	–
	+25°C	15.0	-0.18	0	4.00	5.00	4.50	5.50	8.00
	+125°C	14.0	-0.18	0	4.00	–	4.50	5.50	–
MC851	0°C	15.0	-0.18	0.45	4.00	–	5.00	5.00	–
	+25°C	15.0	-0.18	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	14.0	-0.18	0.50	4.00	–	5.00	5.00	–

Characteristic	Symbol	Pin Under Test	MC951 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC851 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	1	–	0.40	–	0.40	–	0.45	Vdc	–	0.45	–	0.45	–	0.50	Vdc	1	–	–	–	–	14	–	–	7,10
		1	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	1	–	–	–	–	14	–	–	5,7
		6	–		–		–			–		–		–			6	–	–	–	–	9,14	–	–	7
	V_{OH}	1	2.50	–	2.60	–	2.50	–		2.60	–	2.60	–	2.50	–		–	1	–	–	–	9,14	–	–	7
		6	2.50	–	2.60	–	2.50	–	↓	2.60	–	2.60	–	2.50	–	↓	–	6	–	–	–	14	–	–	7,10
Reverse Current	I_R	3	–	2.0	–	2.0	–	5.0	μAdc	–	5.0	–	5.0	–	10	μAdc	–	–	–	3	–	–	14	–	2,7
		4	–	2.0	–	2.0	–	5.0	μAdc	–	5.0	–	5.0	–	10	μAdc	–	–	–	4	–	–	14	–	2,7
Forward Current	$0.5\ I_F$	2	-0.80	–	-0.80	–	-0.75	–	mAdc	-0.70	–	-0.70	–	-0.67	–	mAdc	–	–	2	–	–	–	14	–	7
		11	-0.80	–	-0.80	–	-0.75	–		-0.70	–	-0.70	–	-0.67	–		–	–	10	–	–	–	↓	–	↓
	$0.5I_F/2I_F$	3	-0.80	-3.20	-0.80	-3.20	-0.75	-3.00		-0.70	-2.80	-0.70	-2.80	-0.67	-2.67		–	–	3	4	–	–		–	
		4	-0.80	-3.20	-0.80	-3.20	-0.75	-3.00		-0.70	-2.80	-0.70	-2.80	-0.67	-2.67		–	–	4	3	–	–	↓	–	↓
	I_9	9	–	–	0.50	0.75	–	–	↓	–	–	0.40	0.80	–	–	↓	–	–	–	–	–	–	9,14	–	7,10
Power Drain Current	I_{PDL}	9,14†	–	–	–	9.0	–	–	mAdc	–	–	–	12	–	–	mAdc	–	–	–	–	9,14	–	–	–	3,4,7
	I_{max}	14	–	–	–	22	–	–	mAdc	–	–	–	25	–	–	mAdc	–	–	–	–	–	–	–	14	3,4,7
Switching Times																	Pulse In	Pulse Out							
	t_{pd+}	3,6	–	–	–	50	–	–	ns	–	–	–	50	–	–	ns	3	6	–	–	9,14	–	–	–	7
	t_{pd-}	3,1	–	–	–	50	–	–		–	–	–	50	–	–			1	–	–		–	–	–	
	PW_1	3,1	–	–	90	220	–	–		–	–	90	220	–	–			1	–	–		–	–	–	
	PW_6	3,6	–	–	70	160	–	–	↓	–	–	70	160	–	–	↓		6	–	–	↓	–	–	–	↓

Pins not listed are left open.
†I_{PDL} is measured at pins 9 and 14 simultaneously.

MC938F · MC838F, P

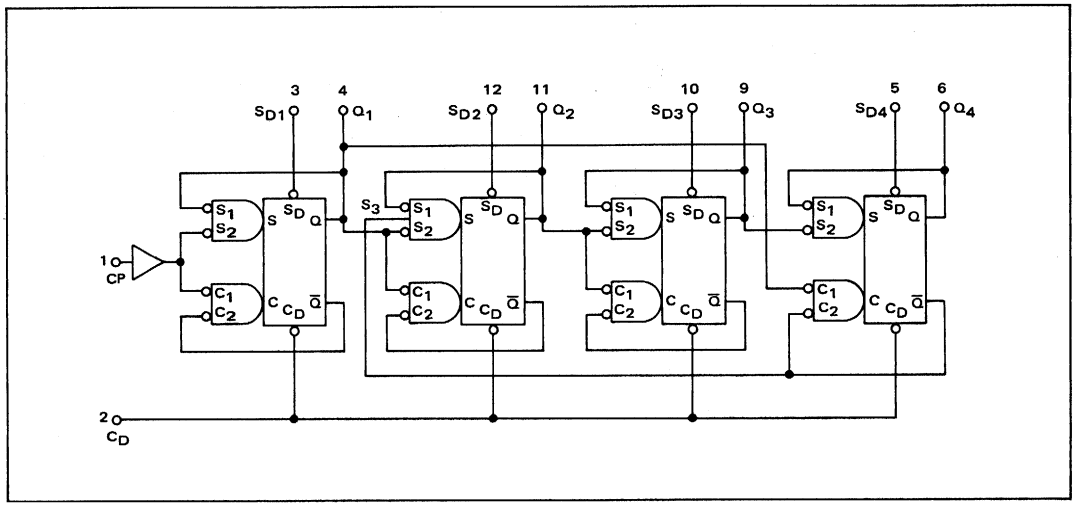
This monolithic ripple counter is designed to operate at ±20% of the nominal 5.0 volt power supply voltage and is guaranteed to 20 MHz. It has standard MDTL inputs, and uses active pull-up devices in the outputs to increase capacitive drive capabilities. The outputs correspond to a standard 8-4-2-1 BCD with individual direct sets and a common direct clear available to preset the counter to any desired condition. Typical noise margin is 1.0 volt.

Input Loading Factor
S_D = 1.5
C_D = 5
CP = 1

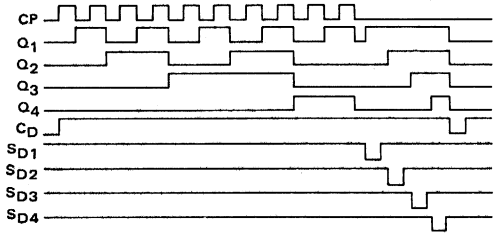
Output Loading Factor = 8

Total Power Dissipation = 150 mW typ/pkg

Maximum Counting Frequency = 30 MHz typ



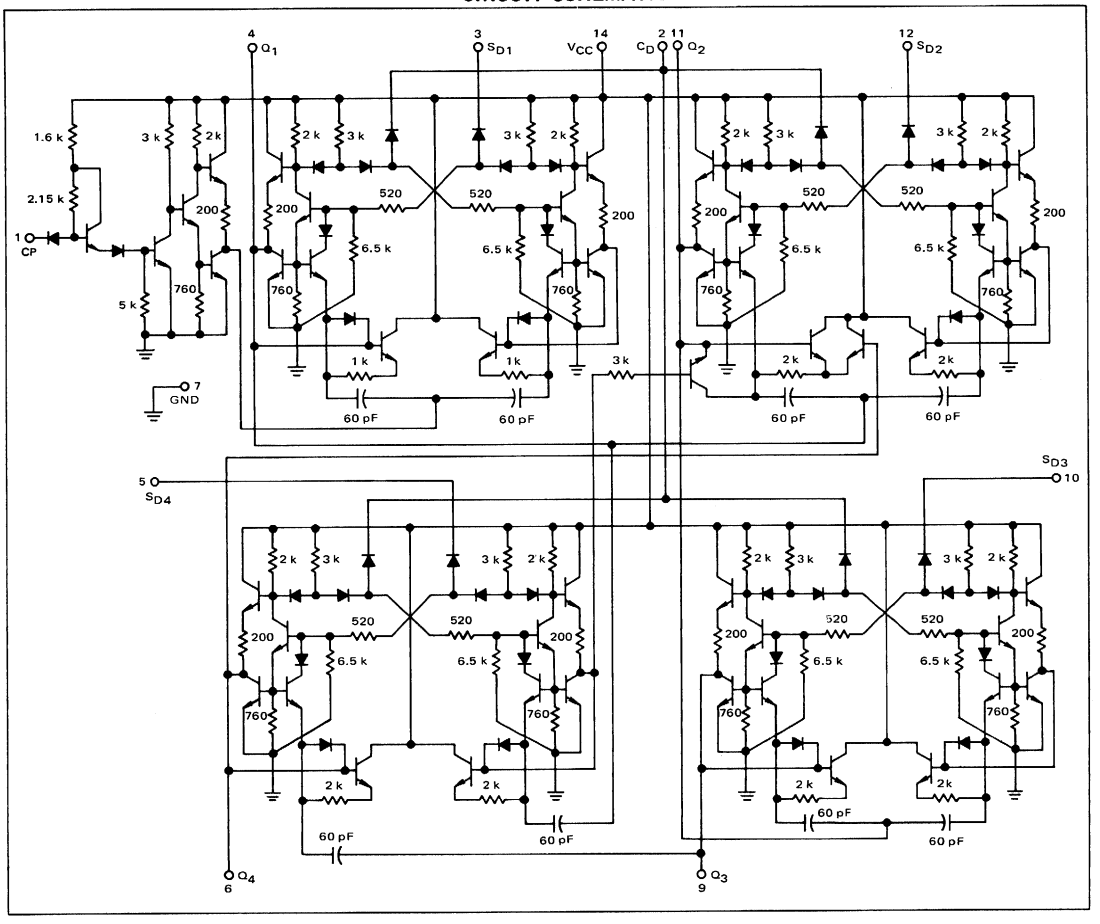
COUNTER SEQUENCE



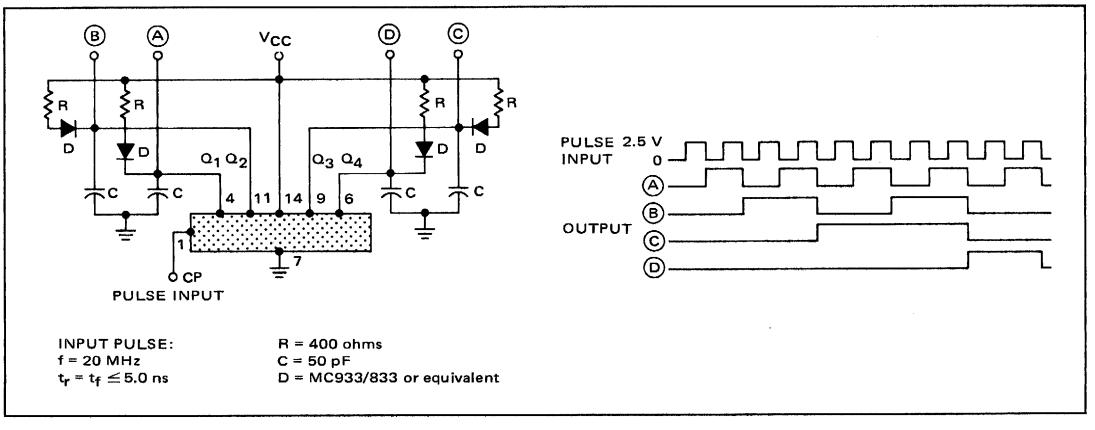
DECODING LOGIC

0	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
1	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
2	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	
3	Q_1	Q_2	$\bar{Q}_3$	
4	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	
5	Q_1	$\bar{Q}_2$	Q_3	
6	$\bar{Q}_1$	Q_2	Q_3	
7	Q_1	Q_2	Q_3	
8	$\bar{Q}_1$	Q_4		
9	Q_1	Q_4		

CIRCUIT SCHEMATIC



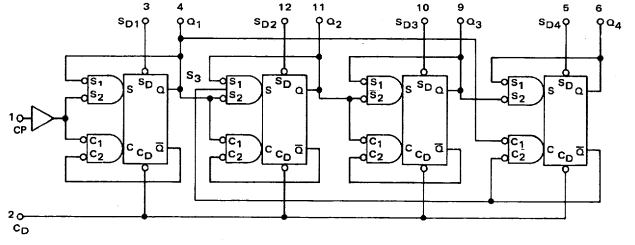
COUNTING FREQUENCY TEST CIRCUIT AND WAVEFORMS



INPUT PULSE:
f = 20 MHz
$t_r = t_f \leq 5.0$ ns

R = 400 ohms
C = 50 pF
D = MC933/833 or equivalent

ELECTRICAL CHARACTERISTICS



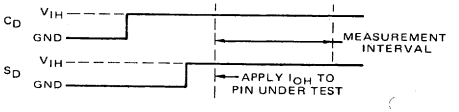
@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC938	−55°C	11.4	-0.12	2.10	0	4.00	-	4.50	5.50	-
MC938	+25°C	12.0	-0.12	2.00	0	4.00	5.00	4.50	5.50	8.00
MC938	+125°C	10.8	-0.12	2.00	0	4.00	-	4.50	5.50	-
MC838	0°C	12.0	-0.12	2.00	0.45	4.00	-	5.00	5.00	-
MC838	+25°C	12.0	-0.12	1.90	0.45	4.00	5.00	5.00	5.00	8.00
MC838	+75°C	11.4	-0.12	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC938 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC838 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	4	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	4	-	3,5,10,12	-	-	-	14	-	-	1,2,7
		6	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6	-	↓	-	-	-	↓	-	-	↓
		9	-		-		-			-		-		-			9	-		-	-	-		-	-	
		11	-		-		-			-		-		-			11	-		-	-	-		-	-	
	V_{OH}	4	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	4*	2*,3*,5, 10,12	-	-	-		-	-	1,7
		6		-		-		-			-		-		-		-	6*	2*,3,5*, 10,12	-	-	-		-	-	↓
		9		-		-		-			-		-		-		-	9*	2*,3,5, 10*,12	-	-	-		-	-	
		11		-		-		-			-		-		-		-	11*	2*,3,5, 10,12*	-	-	-		-	-	
Short-Circuit Current	I_{SC}	4	-9.0	-	-12.0	-	-10.0	-	mAdc	-9.0	-	-10.0	-	-9.0	-	mAdc	-	-	2,5,10,12	-	-	-	-	14	-	1,3,4,7
		6	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	2,3,10,12	-	-	-	-	↓	-	1,5,6,7
		9		-		-		-			-		-		-		-	-	2,3,5,12	-	-	-	-		-	1,7,9,10
		11		-		-		-			-		-		-		-	-	2,3,5,10	-	-	-	-		-	1,7,11,12

Pins not listed are left open.

† Momentarily ground this terminal before applying test condition.

* Inputs to C_D (pin 2) and appropriate S_D (pins 3, 5, 10, or 12) as shown:



ELECTRICAL CHARACTERISTICS (continued)

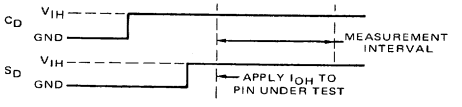
@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH}	Volts V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC938	−55°C	11.4	-0.12	2.10	0	4.00	-	4.50	5.50	-
	+25°C	12.0	-0.12	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	10.8	-0.12	2.00	0	4.00	-	4.50	5.50	-
MC838	0°C	12.0	-0.12	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	12.0	-0.12	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	11.4	-0.12	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC938 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC838 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	µAdc	-	5.0	-	5.0	-	10	µAdc	-	-	-	-	1	-	-	14	-	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	3†	-	-	↓	-	↓
		5	-		-		-			-		-		-			-	-	-	-	5†	-	-		-	
		10	-		-		-			-		-		-			-	-	-	-	10†	-	-		-	
		12	-		-		-			-		-		-			-	-	-	-	12†	-	-		-	
	$4 I_R$	2	-	8.0	-	8.0	-	20		-	20	-	20	-	40		-	-	-	-	2†	-	-		-	
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	1	-	-	-	14	-	7
	$1.5 I_F$	3	-	-2.40	-	-2.40	-	-2.25	↓	-	-2.10	-	-2.10	-	-2.00	↓	-	-	-	3	-	-	-	↓	-	↓
		5	-		-		-			-		-		-			-	-	-	5	-	-	-		-	
		10	-		-		-			-		-		-			-	-	-	10	-	-	-		-	
		12	-		-		-			-		-		-			-	-	-	12	-	-	-		-	
	$5 I_F$	2	-	-8.00	-	-8.00	-	-7.50		-	-7.00	-	-7.00	-	-6.65		-	-	-	2	-	-	-		-	
Power Drain Current	I_{PDH}	14	-	-	-	40	-	-	mAdc	-	-	-	43.5	-	-	mAdc	-	-	10*	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	28	-	-	mAdc	-	-	-	32	-	-	mAdc	-	-	-	-	-	-	-	-	14	2,3,5,7, 10,12
																	Pulse In	Pulse Out								
Counting Frequency	f_C	1,4,6, 9,11	-	-	-	20	-	-	MHz	-	-	-	20	-	-	MHz	1	4,6,9,11	-	-	-	14	-	-	-	7

Pins not listed are left open.

† Momentarily ground this terminal before applying test condition.

* Inputs to C_D (pin 2) and appropriate S_D (pins 3, 5, 10, or 12) as shown:



MC939F · MC839F, P

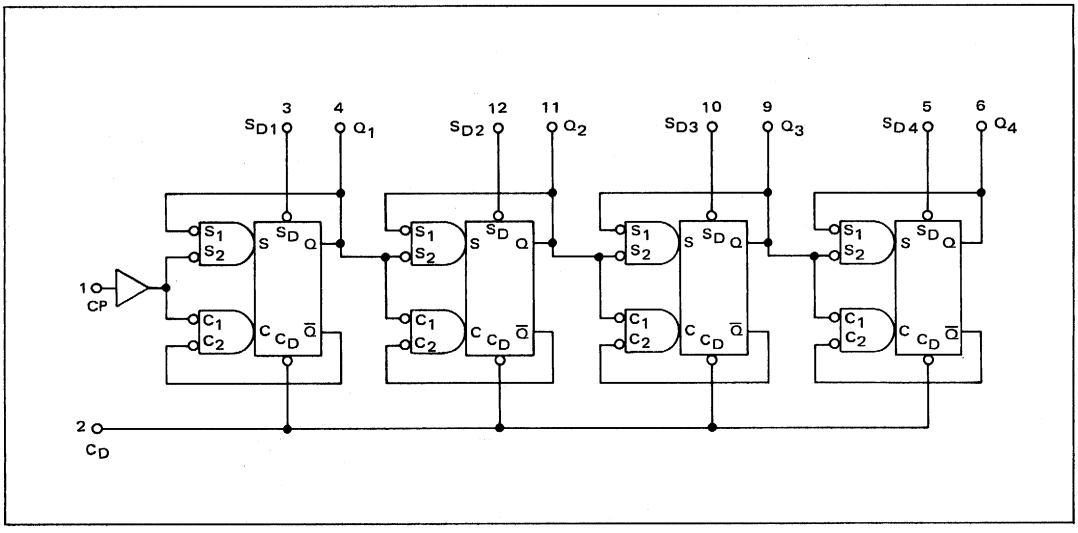
This monolithic ripple counter is designed to operate at ±20% of the nominal 5.0 volt power supply voltage and is guaranteed to 20 MHz. It has standard MDTL inputs, and uses active pull-up devices in the outputs to increase capacitive drive capabilities. The outputs correspond to a standard 8-4-2-1 binary code with individual direct sets and a common direct clear available to preset the counter to any desired condition. Typical noise margin in 1.0 volt.

Input Loading Factor:
- S_D = 1.5
- C_D = 5
- CP = 1

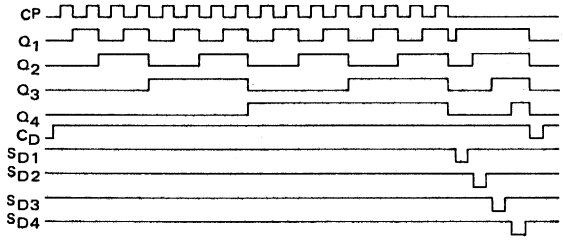
Output Loading Factor = 8

Total Power Dissipation = 150 mW typ/pkg

Maximum Counting Frequency = 30 MHz typ



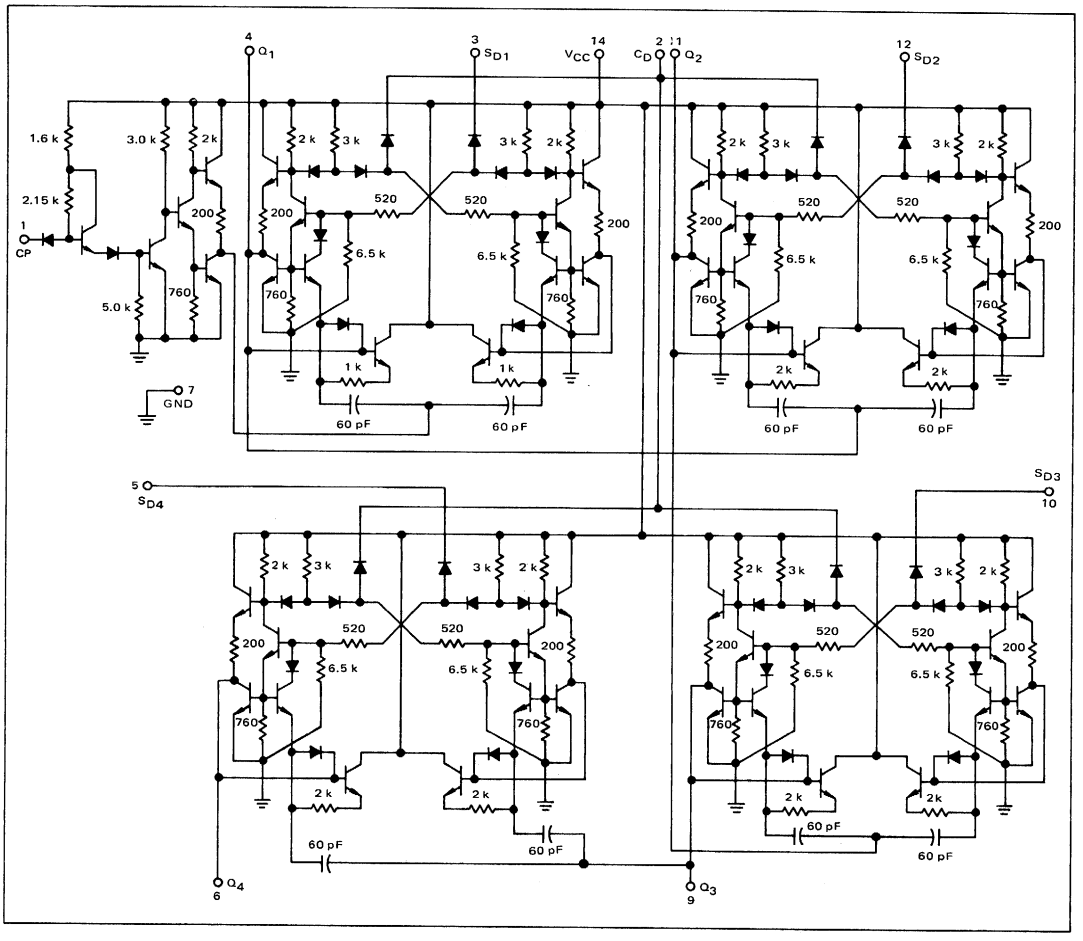
COUNTER SEQUENCE



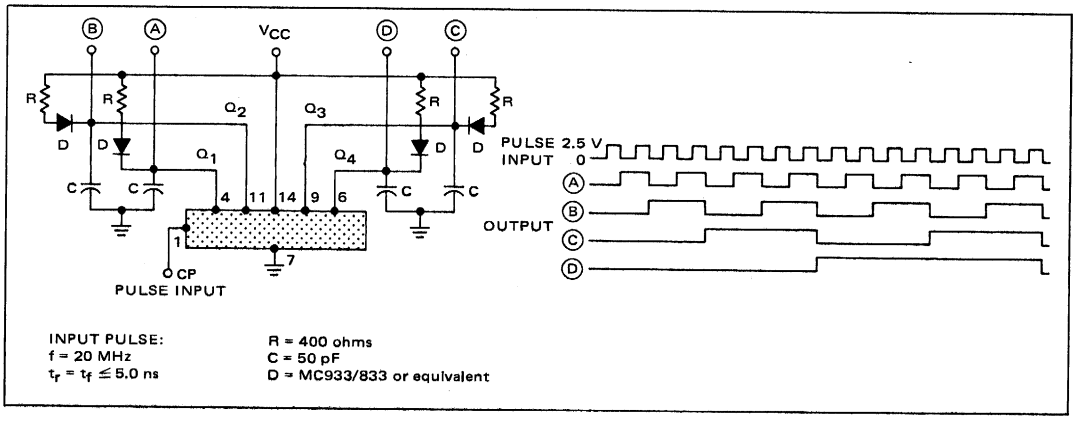
DECODING LOGIC

0	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$
1	Q_1	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$
2	$\overline{Q}_1$	Q_2	$\overline{Q}_3$	$\overline{Q}_4$
3	Q_1	Q_2	$\overline{Q}_3$	$\overline{Q}_4$
4	$\overline{Q}_1$	$\overline{Q}_2$	Q_3	$\overline{Q}_4$
5	Q_1	$\overline{Q}_2$	Q_3	$\overline{Q}_4$
6	$\overline{Q}_1$	Q_2	Q_3	$\overline{Q}_4$
7	$\overline{Q}_1$	Q_2	Q_3	$\overline{Q}_4$
8	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	Q_4
9	Q_1	$\overline{Q}_2$	$\overline{Q}_3$	Q_4
10	$\overline{Q}_1$	Q_2	$\overline{Q}_3$	Q_4
11	Q_1	Q_2	$\overline{Q}_3$	Q_4
12	$\overline{Q}_1$	$\overline{Q}_2$	Q_3	Q_4
13	Q_1	$\overline{Q}_2$	Q_3	Q_4
14	$\overline{Q}_1$	Q_2	Q_3	Q_4
15	Q_1	Q_2	Q_3	Q_4

CIRCUIT SCHEMATIC



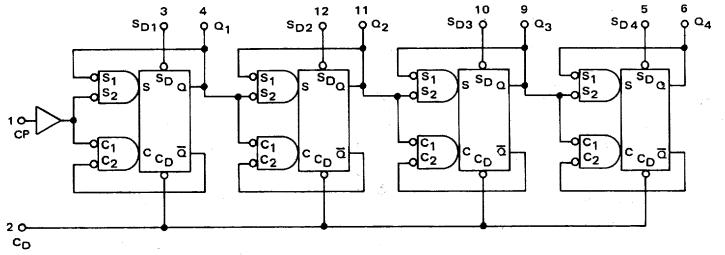
COUNTING FREQUENCY TEST CIRCUIT AND WAVEFORMS



INPUT PULSE:
f = 20 MHz
$t_r = t_f \leq 5.0$ ns

R = 400 ohms
C = 50 pF
D = MC933/833 or equivalent

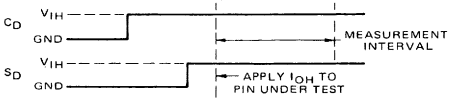
ELECTRICAL CHARACTERISTICS



@ Test Temperature		TEST CURRENT / VOLTAGE VALUES mA I_{OL}	I_{OH}	Volts V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC939	−55°C	11.4	-0.12	2.10	0	4.00	-	4.50	5.50	-
	+25°C	12.0	-0.12	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	10.8	-0.12	2.00	0	4.00	-	4.50	5.50	-
MC839	0°C	12.0	-0.12	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	12.0	-0.12	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	11.4	-0.12	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC939 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC839 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	4	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	4	-	3,5,10,12	-	-	-	14	-	-	1,2,7
		6	-		-		-			-		-		-			6	-		-	-	-		-	-	
		9	-		-		-			-		-		-			9	-		-	-	-		-	-	
		11	-		-		-			-		-		-			11	-		-	-	-		-	-	
	V_{OH}	4	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	4*	2*,3*, 5,10,12	-	-	-		-	-	1,7
		6		-		-		-			-		-		-		-	6*	2*,3,5*, 10,12	-	-	-		-	-	
		9		-		-		-			-		-		-		-	9*	2*,3,5, 10*,12	-	-	-		-	-	
		11		-		-		-			-		-		-		-	11*	2*,3,5, 10,12*	-	-	-		-	-	
Short-Circuit Current	I_{SC}	4	-9.0	-	-12.0	-	-10.0	-	mAdc	-9.0	-	-10.0	-	-9.0	-	mAdc	-	-	2,5,10,12	-	-	-	-	14	-	1,3,4,7
		6		-		-		-			-		-		-		-	-	2,3,10,12	-	-	-	-		-	1,5,6,7
		9		-		-		-			-		-		-		-	-	2,3,5,12	-	-	-	-		-	1,7,9,10
		11		-		-		-			-		-		-		-	-	2,3,5,10	-	-	-	-		-	1,7,11,12

Pins not listed are left open.
† Momentarily ground this terminal before applying test condition.
* Inputs to C_D (pin 2) and appropriate S_D (pins 3, 5, 10, or 12) as shown:

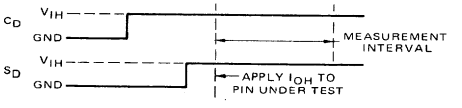


ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature		TEST CURRENT / VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_{max}
MC939	−55°C	11.4	-0.12	2.10	0	4.00	-	4.50	5.50	-
	+25°C	12.0	-0.12	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	10.8	-0.12	2.00	0	4.00	-	4.50	5.50	-
MC839	0°C	12.0	-0.12	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	12.0	-0.12	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	11.4	-0.12	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC939 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC839 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	1	-	-	14	-	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	3†	-	-	↓	-	↓
		5	-		-		-			-		-		-			-	-	-	-	5†	-	-		-	
		10	-		-		-			-		-		-			-	-	-	-	10†	-	-		-	
		12	-		-		-			-		-		-			-	-	-	-	12†	-	-		-	
	4 I_R	2	-	8.0	-	8.0	-	20		-	20	-	20	-	40		-	-	-	-	2†	-	-		-	
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	1	-	-	-	14	-	7
	1.5 I_F	3	-	-2.40	-	-2.40	-	-2.25	↓	-	-2.10	-	-2.10	-	-2.00	↓	-	-	-	3	-	-	-	↓	-	↓
		5	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	-	5	-	-	-		-	
		10	-		-		-			-		-		-			-	-	-	10	-	-	-		-	
		12	-		-		-			-		-		-			-	-	-	12	-	-	-		-	
	5 I_F	2	-	-8.00	-	-8.00	-	-7.50		-	-7.00	-	-7.00	-	-6.65		-	-	-	2	-	-	-	↓	-	↓
Power Drain Current	I_{PDH}	14	-	-	-	40	-	-	mAdc	-	-	-	43.5	-	-	mAdc	-	-	2†	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	28	-	-	mAdc	-	-	-	32	-	-	mAdc	-	-	-	-	-	-	-	-	14	2,3,5,7, 10,12
																	Pulse In	Pulse Out								
Counting Frequency	f_C	1, 4, 6, 9,11	-	-	-	20	-	-	MHz	-	-	-	20	-	-	MHz	1	4,6,9,11	-	-	-	14	-	-	-	7

Pins not listed are left open.
† Momentarily ground this terminal before applying test condition.
* Inputs to C_D (pin 2) and appropriate S_D (pins 3, 5, 10, or 12) as shown:



DUAL 4-INPUT EXPANDERS

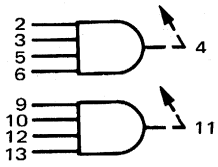
MC933F • MC833F, P

DUAL 4-3 INPUT EXPANDERS

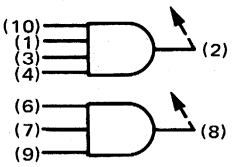
MC933G • MC833G

This dual expander consists of two independent diode networks with characteristics matched to the input diodes of the gate and buffer elements in this logic family. Its use increases the fan-in capability of other MDTL devices to a maximum of 20 while only slightly affecting performance.

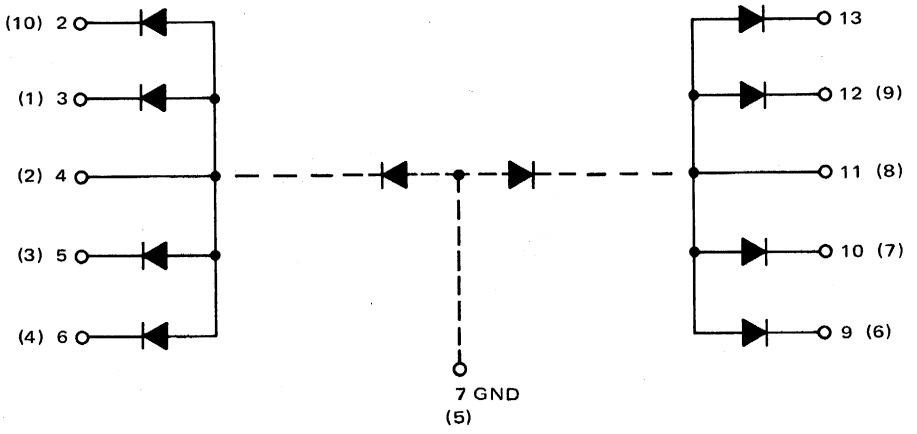
MC933F/MC833F, P



MC933G/MC833G



Input Loading Factor = 1



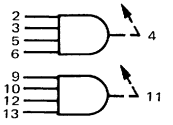
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	–	2	3	4	5	6	7	–	9	10	11	12	13	–
Metal Can	–	10	1	2	3	4	5	–	6	7	8	9	–	–



Characteristic	Symbol	Pin Under Test	MC933 Test Limits −55°C Min	MC933 Test Limits −55°C Max	MC933 Test Limits +25°C Min	MC933 Test Limits +25°C Max	MC933 Test Limits +125°C Min	MC933 Test Limits +125°C Max	MC933 Unit	MC833 Test Limits 0°C Min	MC833 Test Limits 0°C Max	MC833 Test Limits +25°C Min	MC833 Test Limits +25°C Max	MC833 Test Limits +75°C Min	MC833 Test Limits +75°C Max	MC833 Unit	TEST CURRENT / VOLTAGE VALUES (All Temperatures) mA I_{FD}	TEST CURRENT / VOLTAGE VALUES (All Temperatures) Volts V_R	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{FD}	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: V_R	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: Gnd
																	2.00	4.00			
Forward Voltage	V_{FD}	4	–	0.98	–	0.82	–	0.65	Vdc	–	0.90	–	0.82	–	0.75	Vdc	4	–			2,7
			–		–		–			–		–		–				–			3,7
			–		–		–			–		–		–				–			5,7
			–		–		–			–		–		–				–			6,7
			0.85	–	0.70	–	0.50	–		0.75	–	0.68	–	0.60	–			–			2,3,5,6,7
Reverse Current	I_R	2	–	2.0	–	2.0	–	5.0	μAdc	–	5.0	–	5.0	–	10	μAdc	–	2			3,5,6,7
		3	–		–		–			–		–		–			–	3			2,5,6,7
		5	–		–		–			–		–		–			–	5			2,3,6,7
		6	–		–		–			–		–		–			–	6			2,3,5,7
	$5\ I_R$	4	–	10	–	10	–	25		–	–	–	–	–	–		–	4			7
	$2\ I_R$	4	–	–	–	–	–	–		–	–	–	10	–	–		–	4			7

Pins not listed are left open.

DTL

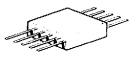
INTEGRATED CIRCUITS

MC200/250 SERIES

MC200 series (−55 to +125°C)
MC250 series (0 to 75°C)

The DTL family of integrated logic circuits is characterized by moderate speed and low power dissipation.

CASE 71A



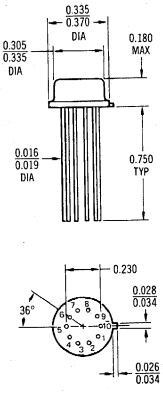
CASE 72
(TO-91)

FUNCTIONS AND CHARACTERISTICS ($V+ = 4$ V, $V- = -2$ V, $T_A = 25°C$)

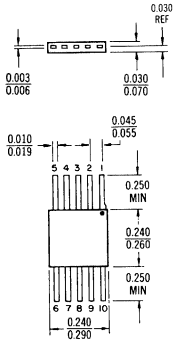
FUNCTION	TYPE①		FAN-OUT		Propagation Delay	Power Dissipation	CASE
	−55 to +125°C	0 to +75°C	MC200 SERIES	MC250 SERIES	t_{pd} ns typ	mW typ	
4-Input Gate NAND/NOR	MC201	MC251	5	4	30	6	71A, 72
3-Input Gate NAND/NOR	MC202	MC252	5	4	30	6	71A, 72
3-Input Power Gate NAND/NOR	MC204	MC254	20	12	40	30	71A, 72
Line Driver	MC205	MC255	20	12	55	50	71A, 72
Dual 2-Input Gate NAND/NOR	MC206	MC256	5	4	30	12	71A, 72
Dual 3-2 Input Gate NAND/NOR	MC207	MC257	5	4	30	12	71A, 72
Dual 3-2 Input Gate NAND/NOR	MC208	MC258	4	3	30	30	71A, 72
Clocked R-S Flip-Flop	MC209	MC259	8	6	60	16	71A, 72
Clocked R-S Flip-Flop (Pulse Triggered Binary)	MC210	MC260	8	6	60	16	71A, 72
Dual 3-Input Gate NAND/NOR	MC212	MC262	5	4	30	12	71A, 72
Dual 3-Input Gate NAND/NOR	MC213	MC263	4	3	30	30	71A, 72
			V_R (Volts)		t_{rr} (ns)		
6-Input Gate AND (Expander)	MC203	MC253	8	8	4	—	71A, 72
Dual 3-Input Gate AND (Expander)	MC215	MC265	8	8	4	—	71A, 72
Dual 3-Input Diode Array	MC217	MC267	8	8	4	—	71A, 72

① G suffix denotes Metal Can, F suffix denotes Flat Package. (i.e., MC201G = Metal Can, MC201F = Flat Package.)

OUTLINE DIMENSIONS



CASE 71A



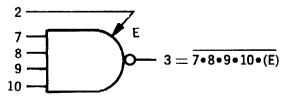
CASE 72
(TO-91)

Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

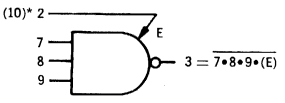
Numbers at ends of terminals represent pin numbers.
Inputs have a fan-in of 1 unless otherwise noted. For fan-out capability, see Functions and Characteristics table.
(V^+ = pin 6, V^- = pin 5 unless otherwise noted. Gnd = 1.)

GATES

MC201, MC251
4-Input Gate NAND/NOR

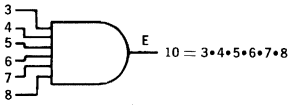


MC202, MC252
MC204, MC254
3-Input Gate NAND/NOR



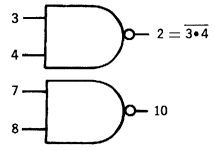
*MC204, MC254
Fan-in = 2 for MC204, MC254

MC203, MC253
6-Input Gate AND
(Expander)

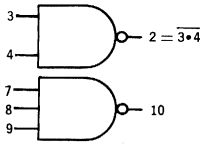


Note: No power supply connection.

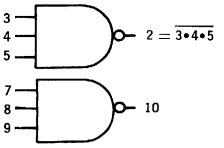
MC206, MC256
Dual 2-Input Gate NAND/NOR



MC207, MC257
MC208, MC258
Dual 3-2 Input Gate NAND/NOR

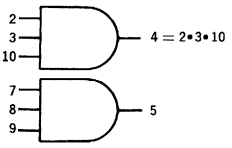


MC212, MC262
MC213, MC263
Dual 3-Input Gate NAND/NOR



Note: No V- connection.

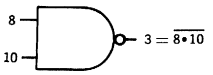
MC215, MC265
Dual 3-Input Gate AND
(Expander)



Note: No power supply connection.

DRIVERS

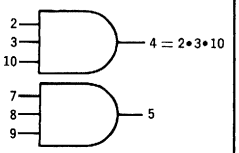
MC205, MC255
Line Driver



Fan-in = 2

DIODE ARRAYS

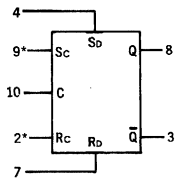
MC217, MC267
Dual Diode Array



Note: No power supply connection.

FLIP-FLOPS

MC209, MC259
Clocked R-S Flip-Flop



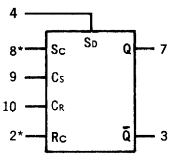
CLOCKED SET-RESET		
Sc	Rc	Q
0	0	?
0	1	1
1	0	0
1	1	No Change

DIRECT SET-RESET		
SD	RD	Q
0	0	‡
0	1	1
1	0	0
1	1	No Change

*Fan-in = 0.75 for MC209, 1 for MC259

‡Both Q and $\overline{Q}$ in 1 state until either SD or CD rises.

MC210, MC260 Clocked R-S Flip-Flop (Pulse Triggered Binary)



*Fan-in = 0.7

Sc	CS	CR	Rc	Q	$\overline{Q}$
1	X	1	X	NC	NC
X	1	X	1	NC	NC
1	X	X	1	NC	NC
0	0	X	1	1	0
0	0	1	X	1	0
1	X	0	0	0	1
X	1	0	0	0	1
0	0	0	0	U	U

Low level on SD overrides other inputs and results in high level on Q.
0 on pins CS or CR means transition to low level.
X = don't care.
NC = no change.
U = indeterminate state.