MEDIUM-POWER
MRTL
INTEGRATED CIRCUITS
MC900/MC800 SERIES

MEDIUM-POWER
MRTL
INTEGRATED CIRCUITS

INDEX

Medium-power MRTL logic circuits are specified over two different temperature ranges. Typical gate speed is 12 ns, with power dissipation averages of 19 mW (input high) and 5.0 mW (inputs low) per logic node.

INDEX

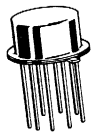
NUMERICAL INDEX

(Functions and Characteristics)

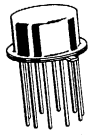
V_{CC} = 3.0 V ± 10%, T_A = 25°C

Function	Type ①		Case	Output Loading Factor each output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Page No.
	-55 to +125°C	0 to +100°C					
Buffer	MC900	MC800	72, 96	25	20	16/45 ②	6-31
Counter Adapter	MC901	MC801	96	5	22	55	6-76
R-S Flip-Flop	MC902	MC803	96	4	14	22	6-38
3-Input NOR Gate	MC903	MC803	72, 96	5	12	19/5.0 ②	6-12
Half Adder	MC904	MC804	72, 96	5	14	45	6-66
Half-Shift Register	MC905	MC805	72, 96	4	22	53	6-57
Half-Shift Register (w/o Inverter)	MC906	MC806	72, 96	4	22	36	6-60
4-Input NOR Gate	MC907	MC807	72, 96	5	12	19/5.0 ②	6-15
Dual 2-Input NOR Gate	MC914	MC814	72, 96	5	12	38/10 ②	6-19
Dual 3-Input NOR Gate	MC915	MC815	72, 96A	5	12	38/10 ②	6-21
J-K Flip-Flop	MC916	MC816	72, 96	3	35	62/54 ③	6-40
Quad 2-Input NOR Gate	MC924	MC824	83	5	12	76/20 ②	6-27
Dual 4-Input NOR Gate	MC925	MC825	83	5	12	38/10 ②	6-23
J-K Flip-Flop	MC926	MC826	72, 96A	5	35	130/65 ③	6-44
Quad Inverter	MC927	MC827	72, 96A	5	12	76/20 ②	6-78
5-Input NOR Gate	MC929	MC829	72, 96	5	12	19/5.0 ②	6-17
Quad Exclusive OR Gate	MC971	MC871	83	5	12	72	6-29
J-K Flip-Flop	MC974	MC874	96	5	35	130/65 ③	6-47
Dual Half Adder	MC975	MC875	83	5	20	90	6-68
Dual Half-Shift Register	MC983	MC883	83	4	22	110	6-62
Dual Half-Shift Register w/Inverter	MC984	MC884	83	4	22	75	6-64
Quad 2-Input Expander	MC985	MC885	83	–	12	17/– ②	6-84
Dual 4-Input Expander	MC986	MC886	83	–	12	17/– ②	6-82
Dual 3-Input Buffer, non inverting	MC988	MC888	83	25	24	128/42 ②	6-36
Hex Inverter	MC989	MC889	83	5	12	76/20 ②	6-80
Dual J-K Flip-Flop	MC990	MC890	83	3	35	124/108 ③	6-50
Dual J-K Flip-Flop	MC991	MC891	83	5	40	155/130 ③	6-54
Triple 3-Input NOR Gate	MC992	MC892	83	5	12	57/15 ②	6-25
Dual Full Adder	MC996	MC896	83	4	60	70	6-70
Dual Full Subtractor	MC997	MC897	83	4	60	70	6-73
Dual Buffer	MC999	MC899	72, 96A	25	20	32/90 ②	6-34
Hex Expander	MC9919	MC9819	83	–	12	13/– ②	6-86

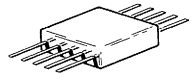
① G Suffix denotes Metal Can, F suffix denotes Flat Package; i.e., MC900G = Metal Can, MC900F = Flat Package.
② Inputs High/Inputs Low
③ Only Clock Input High/Inputs Low



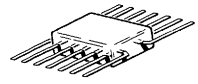
TO-99



TO-100



TO-91



TO-86

MAXIMUM RATINGS
($T_A = 25°C$)

Characteristic		Symbol	Rating	Unit
Input Voltage		—	±4	Vdc
Power Supply Voltage (Pulsed ≤ 1 s)		—	+12	Vdc
Operating Temperature Range	MC900 Series MC800 Series	T_A	-55 to +125 0 to +100	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TEST CONDITION TOLERANCES

$V_{BOT} = \pm 10$ mV $V_{CC} = \pm 10$ mV $V_{in} = \pm 2$ mV $V_{on} = \pm 2$ mV $V_{off} = \pm 2$ mV

DEFINITIONS

I_{A3}, I_{A4}, I_{A5} — Minimum available output current from a device with an output loading of 3, 4, or 5. Output voltage not to fall below the value of V_{in}.

I_{AB} — Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.

I_{CEX} — Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

I_{in} — Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

2 I_{in}, 3 I_{in} — Maximum input current drawn by one input of a device with 2 or 3 bases internally tied together.

V_{BOT} — A high-value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} — Supply voltage.

$V_{CE(sat)}$ — Maximum saturation voltage with V_{BOT} applied to the input.

V_{in} — Minimum high-level voltage applied to the input of a device.

V_{off} — The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} — The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} — The maximum output voltage with V_{on} applied to the input.

V_R — Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

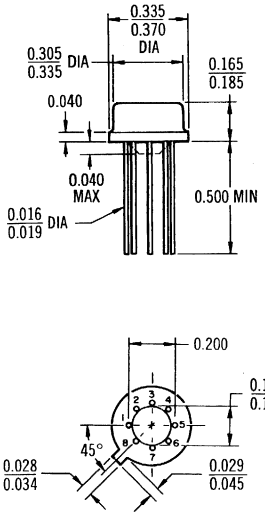
Release Time — The time that the J or K input data must be held after the negative-going clock input transition in order to propagate correct data.

Set-up Time — The time that the J or K input data must be present prior to the negative-going clock input transition in order to propagate correct data.

GENERAL RULES

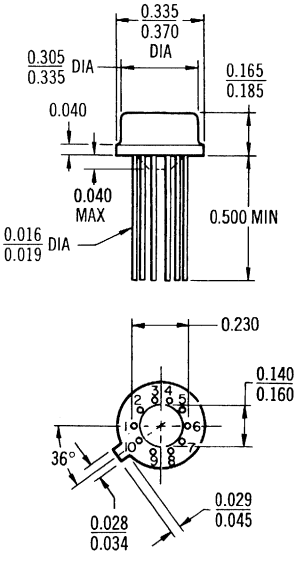
- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- A gate output connected in parallel with another output reduces the drive capability by ½ load. (Paralleling gate circuits requires a V_{CC} connection to only one of the gates.)
- Any number of gates may be paralleled if the input loading is increased by ¼ load, if only one gate is connected to V_{CC}.
- If the counter adapter is paralleled with another circuit, the output drive capability must be reduced by 2 loads. The reason for this drive reduction is the 1280-ohm resistance that connects the output terminals on the counter adapter.
- All unused inputs should be returned to ground.
- When paralleling gates with V_{CC} connected, a maximum of 4 outputs may be paralleled where the input loading factor is increased by 2.33.

OUTLINE DIMENSIONS



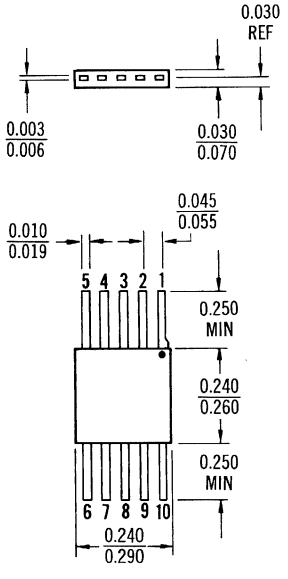
Pin 4 connected to case.

TO-99



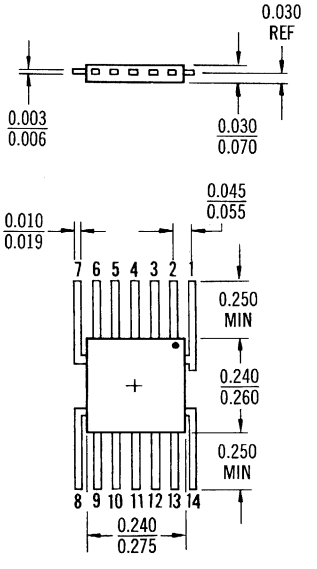
Pin 5 connected to case.

TO-100



Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

TO-91



Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

TO-86

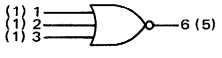
MRTL DEVICES AVAILABLE IN METAL CANS

The logic diagrams on these two pages describe the MC900/MC800 MRTL integrated circuits available in metal cans, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of –55 to +125°C for the MC900 Series, and 0 to +100°C for the MC800 Series, with V_{CC} = 3.0 V ±10%. For the TO-99 metal can, V_{CC} is applied to pin 8, with ground connected to pin 4. For the TO-100 metal can, V_{CC} is applied to pin 10, with ground connected to pin 5.

GATES

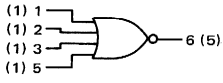
MC903G • MC803G
3-Input Gate



$6 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

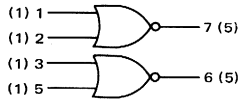
MC907G • MC807G
4-Input Gate



$6 = \overline{1 + 2 + 3 + 5}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

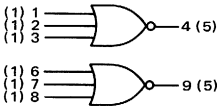
MC914G • MC814G
Dual 2-Input Gate



$7 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

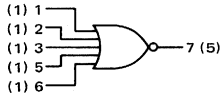
MC915G • MC815G
Dual 3-Input Gate



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

MC929G • MC829G
5-Input Gate

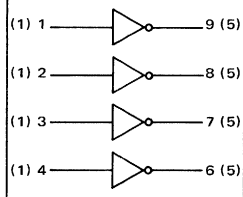


$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

INVERTERS

MC927G • MC827G
Quad Inverter

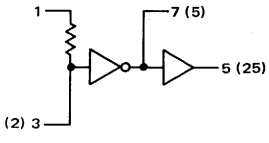


$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

BUFFERS

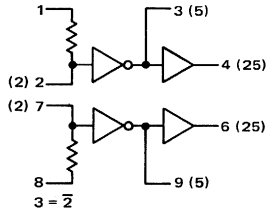
MC900G • MC800G
Buffer



$7 = \overline{3}$
$5 = \overline{3}$

t_{pd} = 20 ns
P_D = 16 mW (Input High)
45 mW (Inputs Low)

MC999G • MC899G
Dual Buffer

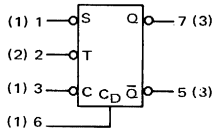


$3 = \overline{2}$
$4 = \overline{2}$

t_{pd} = 20 ns
P_D = 32 mW (Input High)
90 mW (Inputs Low)

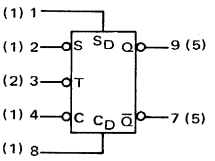
FLIP-FLOPS

MC916G • MC816G
J-K Flip-Flop



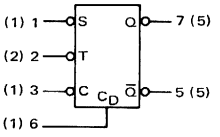
t_{pd} = 30 ns
P_D = 62 mW (Only Clock Input High)
54 mW (Inputs Low)

MC926G • MC826G
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Input High)
65 mW (Inputs Low)

MC974G • MC874G
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Input High)
65 mW (Inputs Low)

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC926 and MC826 only

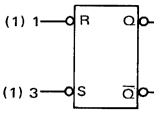
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC902G • MC802G
R-S Flip-Flop

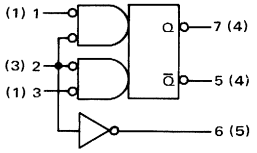


t_{pd} = 14 ns
P_D = 22 mW

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	0

HALF-SHIFT REGISTERS

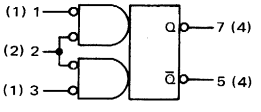
MC905G • MC805G
Half-Shift Register



t_{pd} = 22 ns
P_D = 53 mW

$7 = \overline{5}\,(1 + 2)$
$5 = \overline{7}\,(2 + 3)$
$6 = \overline{2}$

MC906G • MC806G
Half-Shift Register
(Without Inverter)

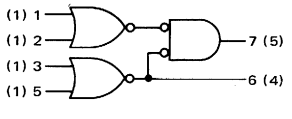


t_{pd} = 22 ns
P_D = 36 mW

$7 = \overline{5}\,(1 + 2)$
$5 = \overline{7}\,(2 + 3)$

HALF ADDERS

MC904G • MC804G
Half Adder

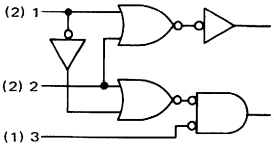


$7 = (1 + 2)\,(3 + 5)$
$6 = \overline{3 + 5}$
t_{pd} = 14
P_D = 45

IF: $3 = \overline{1}$, & $5 = \overline{2}$
THEN: $6 = 1 \cdot 2$
$7 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

COUNTER ADAPTERS

MC901G • MC801G
Counter Adapter



t_{pd} = 22 ns
P_D = 55 mW

$7 = 1 + 2$
$5 = (\overline{1} + 2)\,\overline{3}$

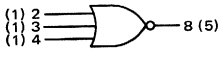
MRTL DEVICES AVAILABLE IN FLAT PACKAGES

The logic diagrams on these four pages describe the MC900/MC800 MRTL integrated circuits available in flat packages, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability — fan-out — (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of −55 to +125°C for the MC900 Series, and 0 to +100°C for the MC800 Series, with V_{CC} = 3.0 V ±10%. For the TO-91 flat package, V_{CC} is applied to pin 10, with ground connected to pin 5. For the TO-86 flat package, V_{CC} is applied to pin 14, with ground connected to pin 7.

GATES

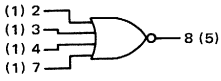
MC903F • MC803F
3-Input Gate



$8 = \overline{2 + 3 + 4}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

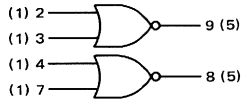
MC907F • MC807F
4-Input Gate



$8 = \overline{2 + 3 + 4 + 7}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

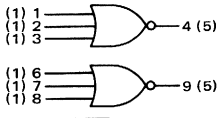
MC914F • MC814F
Dual 2-Input Gate



$9 = \overline{2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

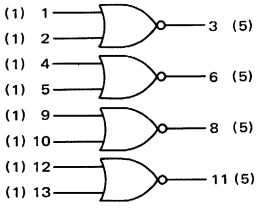
MC915F • MC815F
Dual 3-Input Gate



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

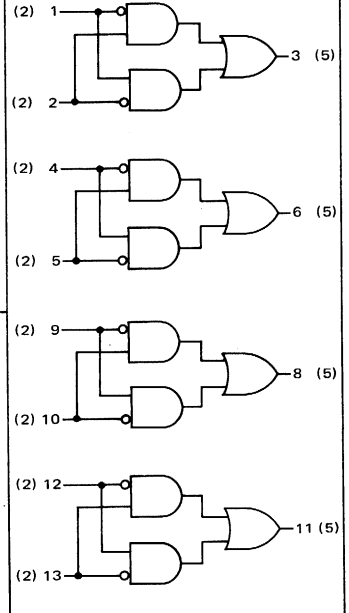
MC924F • MC824F
Quad 2-Input Gate



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

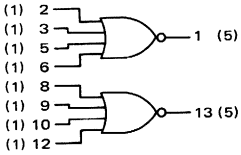
MC971F • MC871F
Quad Exclusive "OR" Gate



$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns
P_D = 72 mW

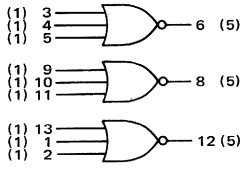
MC925F • MC825F
Dual 4-Input Gate



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

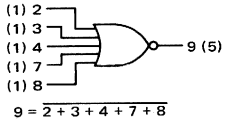
MC992F • MC892F
Triple 3-Input Gate



$6 = \overline{3 + 4 + 5}$

t_{pd} = 12 ns
P_D = 57 mW (Input High)
15 mW (Inputs Low)

MC929F • MC829F
5-Input Gate

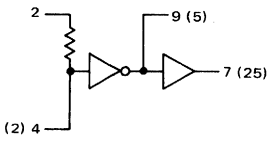


$9 = \overline{2 + 3 + 4 + 7 + 8}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

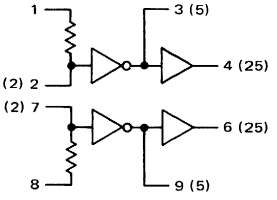
BUFFERS

MC900F • MC800F
Buffer



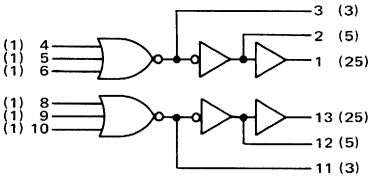
$9 = \overline{4}$
$7 = \overline{4}$
t_{pd} = 15 ns
P_D = 16 mW (Input High)
45 mW (Inputs Low)

MC999F • MC899F
Dual Buffer



$3 = \overline{2}$
$4 = \overline{2}$
t_{pd} = 15 ns
P_D = 32 mW (Input High)
90 mW (Inputs Low)

MC988F • MC888F
Dual 3-Input Buffer
(Non-Inverting)



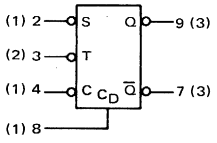
t_{pd} = 24 ns
P_D = 128 mW (Input High)
42 mW (Inputs Low)

$3 = \overline{4 + 5 + 6}$
$2 = 4 + 5 + 6$
$1 = 4 + 5 + 6$

Outputs 1, 2, or 3 may not be used simultaneously.
Outputs 11, 12, or 13 may not be used simultaneously.

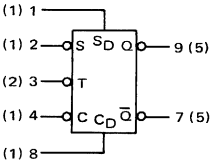
FLIP-FLOPS

MC916F • MC816F
J-K Flip-Flop



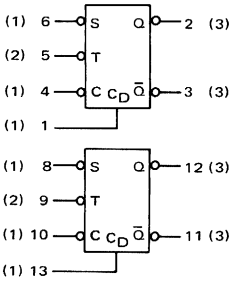
t_{pd} = 35 ns
P_D = 62 mW (Only Clock Inputs High)
54 mW (Inputs Low)

MC926F • MC826F
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Inputs High)
65 mW (inputs Low)

MC990F • MC890F
Dual J-K Flip-Flop



t_{pd} = 35 ns
P_D = 124 mW (Only Clock Inputs High)
108 Mw (Inputs Low)

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

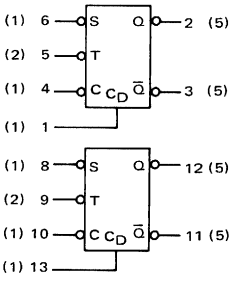
CLOCKED INPUT OPERATION ③
all types

t_n ④		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

J-K FLIP-FLOP TRUTH TABLES

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

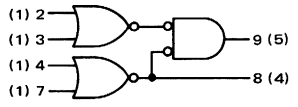
MC991F • MC891F
Dual J-K Flip-Flop



t_{pd} = 40 ns
P_D = 155 mW (Only Clock Input High)
130 mW (Inputs Low)

HALF ADDERS

MC904F • MC804F
Half Adder



$9 = (2 + 3)(4 + 7)$

$8 = \overline{4 + 7}$

t_{pd} = 14 ns

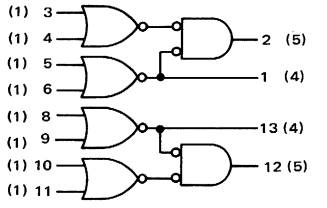
P_D = 45 mW

IF: $4 = \overline{2}$, & $7 = \overline{3}$

THEN: $8 = 2 \cdot 3$

$9 = 2 \cdot \overline{3} + \overline{2} \cdot 3$

MC975F • MC875F
Dual Half Adder



t_{pd} = 20 ns

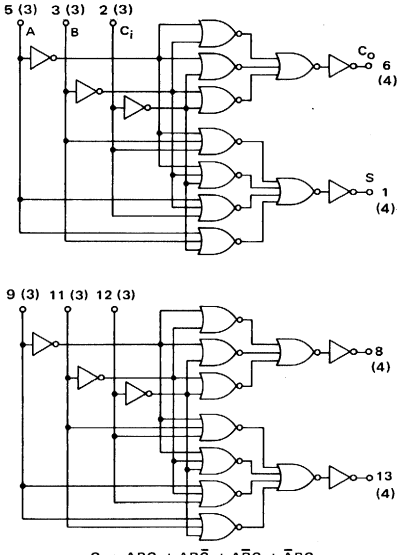
P_D = 120 mW

$2 = (3 + 4)(5 + 6)$

$1 = \overline{5 + 6}$

FULL ADDER

MC996F • MC896F
Dual Full Adder



$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

$S = ABC_i + A\overline{B}\overline{C_i} + \overline{A}\overline{B}C_i + \overline{A}B\overline{C_i}$

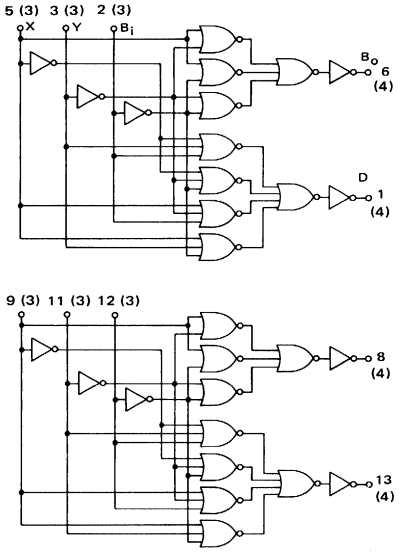
t_{pd} = 60 ns

P_D = 84 mW

TRUTH TABLE				
Input Logic Level			Output Logic Level	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

MC997F • MC897F
Dual Full Subtractor



$D = YXB_i + Y\overline{X}\overline{B_i} + \overline{Y}X\overline{B_i} + \overline{Y}\overline{X}B_i$

$B_o = \overline{Y}\overline{X}B_i + Y\overline{X}\overline{B_i} + Y\overline{X}B_i + YXB_i$

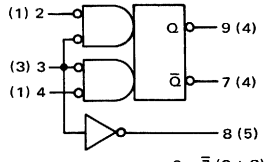
t_{pd} = 60 ns

P_D = 84 mW

TRUTH TABLE				
Input Logic Level			Output Logic Level	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

HALF-SHIFT REGISTERS

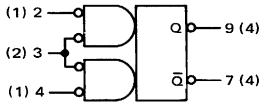
MC905F • MC805F
Half-Shift Register



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$
$8 = \overline{3}$

t_{pd} = 22 ns
P_D = 53 mW

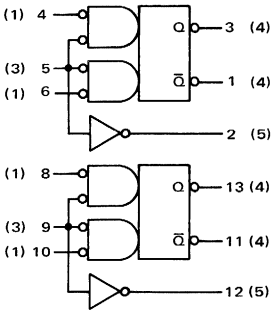
MC906F • MC806F
Half-Shift Register
(Without Inverter)



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$

t_{pd} = 22 ns
P_D = 36 mW

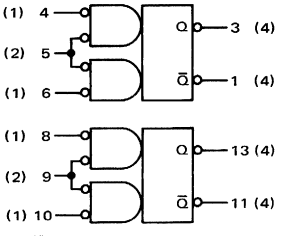
MC983F • MC883F
Dual Half-Shift Register



$1 = \overline{3}\ (6 + 5)$
$3 = \overline{1}\ (5 + 4)$
$2 = \overline{5}$

t_{pd} = 22 ns
P_D = 140 mW

MC984F • MC884F
Dual Half-Shift Register
(Without Inverter)

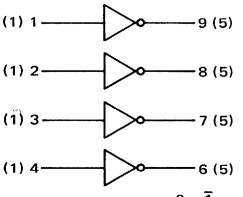


$3 = \overline{1}\ (4 + 5)$
$1 = \overline{3}\ (6 + 5)$

t_{pd} = 22 ns
P_D = 120 mW

INVERTERS

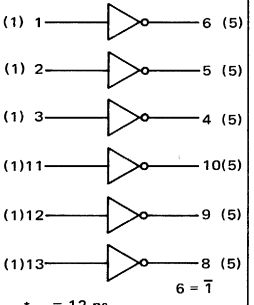
MC927F • MC827F
Quad Inverter



$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

MC989F • MC889F
Hex Inverter

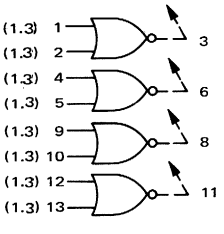


$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

EXPANDERS

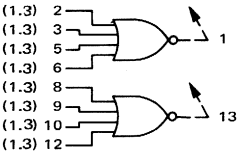
MC985F • MC885F
Quad 2-Input Expander



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 17 mW (input High)
Negligible (Inputs Low)

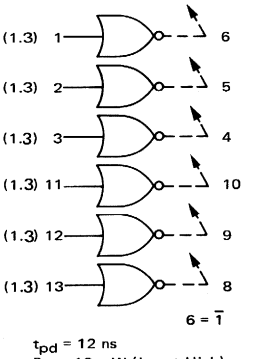
MC986F • MC886F
Dual 4-Input Expander



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 17 mW (Input High)
Negligible (Inputs Low)

MC9919F • MC9819F
Hex Expander



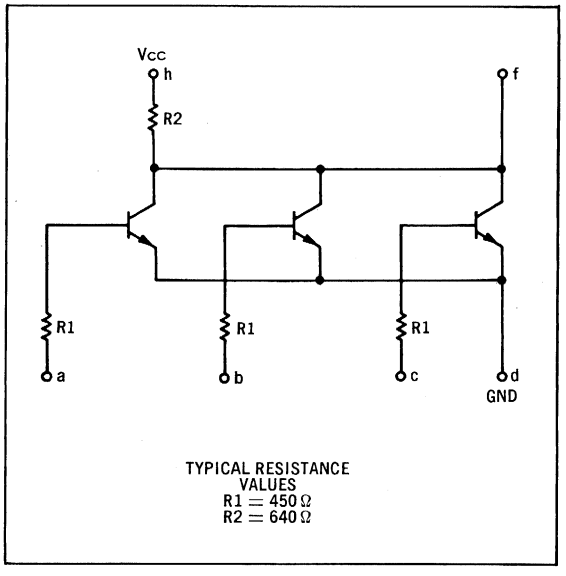
$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 13 mW (Input High)
Negligible (Inputs Low)

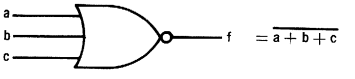
MC903 • MC803

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Provides the positive logic NOR function. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules)



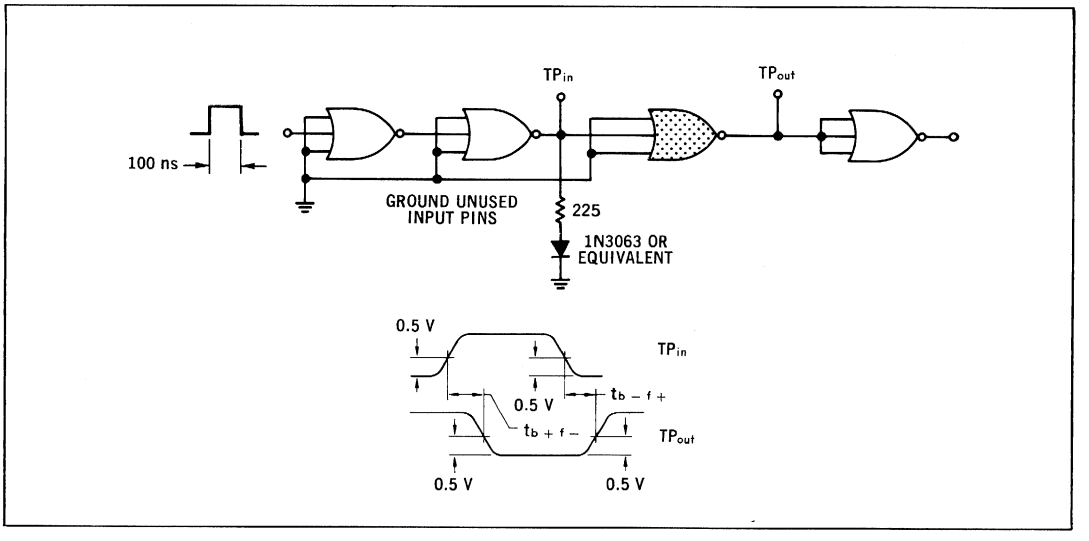
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω



PIN CONNECTIONS

SCHEMATIC	a	b	c	d	—	f	—	h
G PACKAGE (TO-99)	1	2	3	4	—	6	—	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC903	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC803	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

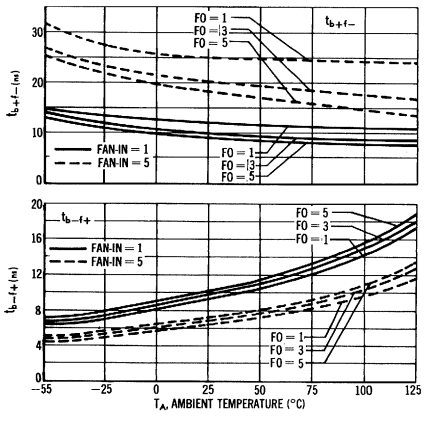
Characteristic	Symbol	Pin Under Test	MC903 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC803 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a b c	- - -	495 ↓ ↓	- - -	435 ↓ ↓	- - -	470 ↓ ↓	µAdc ↓	- - -	504 ↓ ↓	- - -	450 ↓ ↓	- - -	450 ↓ ↓	µAdc ↓	a b c	- - -	b, c a, c a, b	- - -	h ↓ ↓	d ↓
Output Current	I_{A5}	f	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	f	-	a, b, c	h	d
Output Leakage Current	I_{CEX}	f	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	f	-	-	a, b, c	-	d
Output Voltage	V_{out}	f ↓	- - -	710 ↓ ↓	- - -	300 ↓ ↓	- - -	320 ↓ ↓	mVdc ↓	- - -	574 ↓ ↓	- - -	400 ↓ ↓	- - -	370 ↓ ↓	mVdc ↓	- - -	a b c	- - -	- - -	h ↓ ↓	d ↓
Saturation Voltage	$V_{CE(sat)}$	f ↓	- - -	200 ↓ ↓	- - -	210 ↓ ↓	- - -	280 ↓ ↓	mVdc ↓	- - -	290 ↓ ↓	- - -	260 ↓ ↓	- - -	340 ↓ ↓	mVdc ↓	- - -	- - -	a b c	- - -	h ↓ ↓	d ↓
Switching Time	t	b+f- b-f+	- -	- -	- -	20 28	- -	- -	ns ns	- -	- -	- -	20 28	- -	- -	ns ns	Pulse In b b	Pulse Out f f	- -	- -	h h	d d

Pins not listed are left open

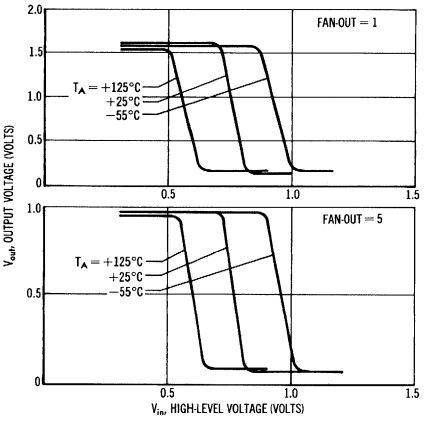
Pins e and g omitted

TYPICAL CURVES

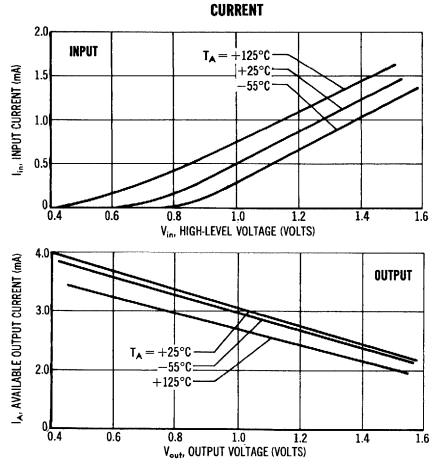
SWITCHING CHARACTERISTICS



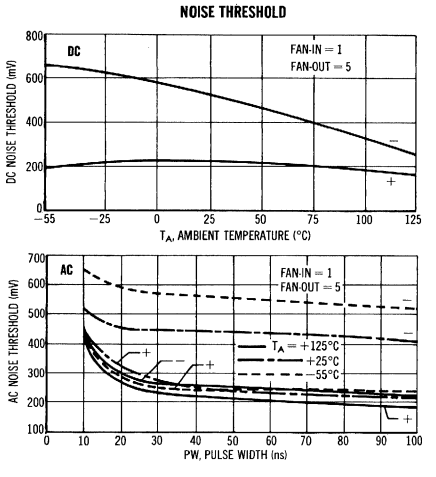
OUTPUT VOLTAGE



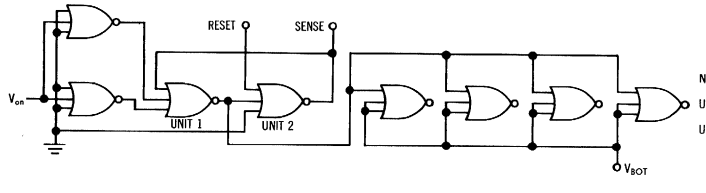
CURRENT



NOISE THRESHOLD



TEST CIRCUIT FOR NOISE THRESHOLD MEASUREMENTS

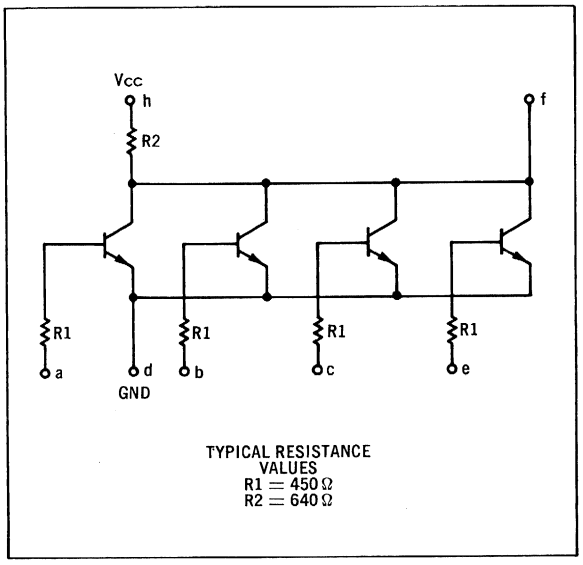


NOTE: V_{CC} and ground connections made to all devices.
UNIT 1 — Negative dc voltage with respect to ground applied to pin d.
UNIT 2 — Positive dc voltage with respect to ground applied to pin d.

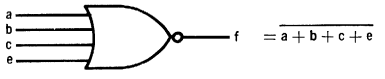
MC907 • MC807

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Provides positive logic NOR function. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules).



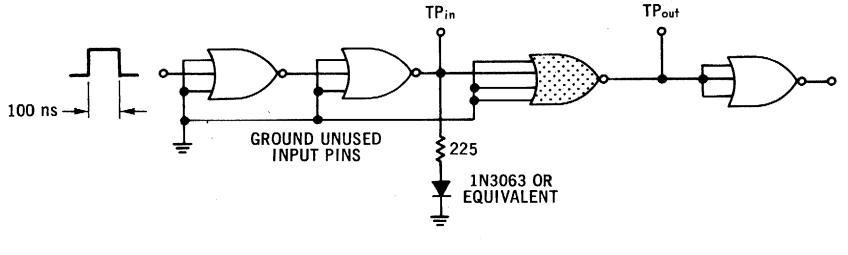
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

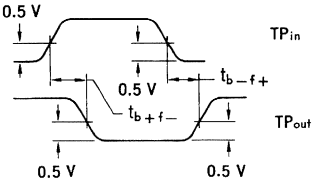


PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	—	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC907	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC807	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

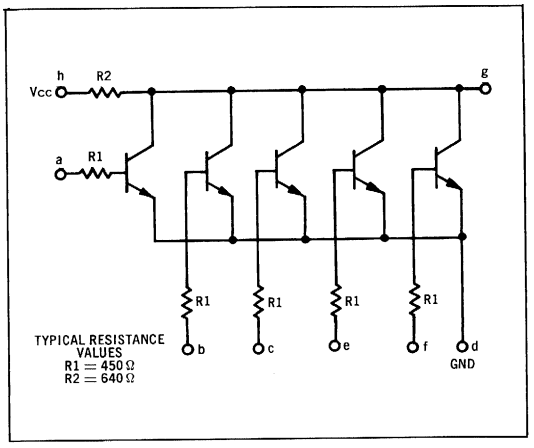
Characteristic	Symbol	Pin Under Test	MC907 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC807 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	a	-	b, c, e	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c, e	-	↓	↓
		c	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	c	-	a, b, e	-	↓	↓
		e	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	e	-	a, b, c	-	↓	↓
Output Current	I_{A5}	f	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	f	-	a, b, c, e	h	d
Output Leakage Current	I_{CEX}	f	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	f	-	-	a, b, c, e	-	d
Output Voltage	V_{out}	f	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	↓
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	c	-	-	↓	↓
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	e	-	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	f	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	b	-	↓	↓
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	c	-	↓	↓
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	e	-	↓	↓
																	Pulse In	Pulse Out				
Switching Time	t	b+f-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	b	f	-	-	h	d
		b-f+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	b	f	-	-	h	d

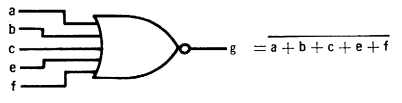
Pins not listed are left open.

MC929 • MC829

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Provides positive logic NOR function. Individual gates may be paralleled with other logic elements for increasing the number of inputs (subject to loading rules).

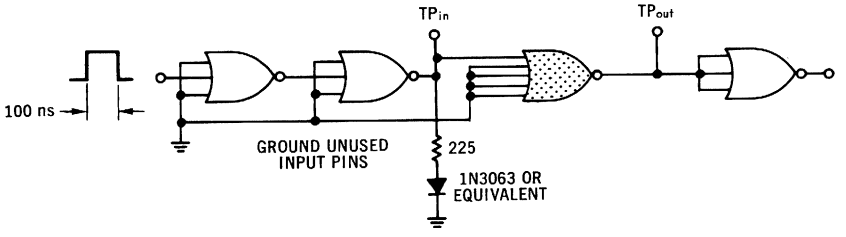


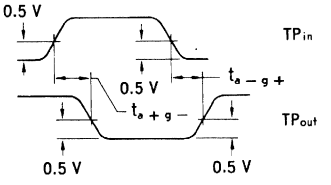


PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC929	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC829	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

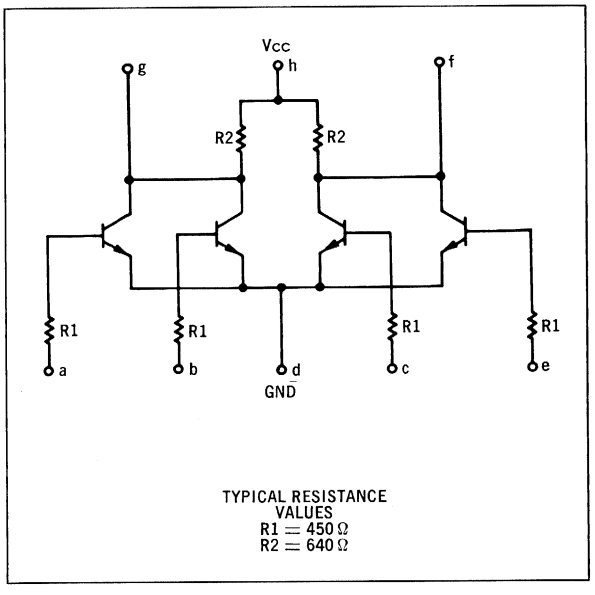
Characteristic	Symbol	Pin Under Test	MC929 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC829 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	a	-	b, c, e, f	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c, e, f	-	↓	↓
		c	-		-		-			-		-		-			c	-	a, b, e, f	-		
		e	-		-		-			-		-		-			e	-	a, b, c, f	-		
		f	-		-		-			-		-		-			f	-	a, b, c, e	-		
Output Current	I_{A5}	g	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	g	-	a,b,c,e,f	h	d
Output Leakage Current	I_{CEX}	g	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	g	-	-	a,b,c,e,f	-	d
Output Voltage	V_{out}	g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	↓
			-		-		-			-		-		-			-	c	-	-		
			-		-		-			-		-		-			-	e	-	-		
			-		-		-			-		-		-			-	f	-	-		
Saturation Voltage	$V_{CE(sat)}$	g	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	b	-	↓	↓
			-		-		-			-		-		-			-	-	c	-		
			-		-		-			-		-		-			-	-	e	-		
			-		-		-			-		-		-			-	-	f	-		
																	Pulse In	Pulse Out				
Switching Time	t	a+g-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	a	g	-	-	h	b,c,d,e,f
		a-g+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	a	g	-	-	h	b,c,d,e,f

Pins not listed are left open.

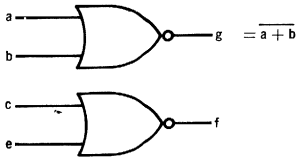
MC914 • MC814

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Two 2-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.



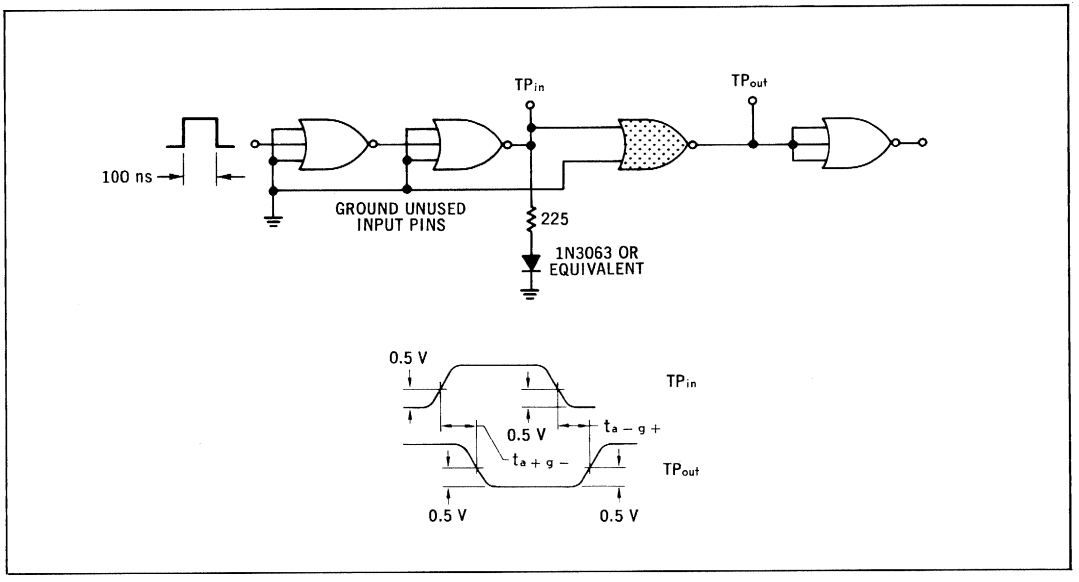
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω



PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC914	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC814	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

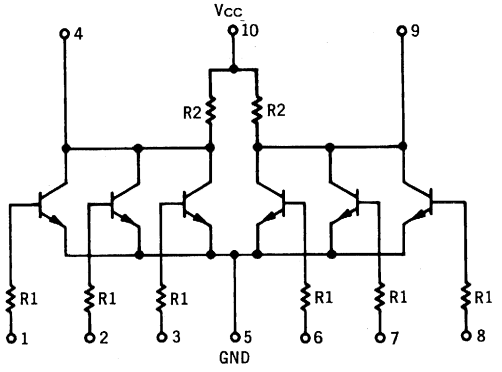
Characteristic	Symbol	Pin Under Test	MC914 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC814 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b	-	h	d
		b	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	b	-	a	-	h	d
Output Current	I_{A5}	g	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	g	-	a, b	h	d
Output Leakage Current	I_{CEX}	g	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	g	-	-	a, b	-	d
Output Voltage	V_{out}	g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
		g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	b	-	-	h	d
Saturation Voltage	$V_{CE(sat)}$	g	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
		g	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	b	-	h	d
																	Pulse In	Pulse Out				
Switching Time	t	a+g-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	a	g	-	-	h	d
		a-g+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	a	g	-	-	h	d

Ground inputs of gate not under test. Other pins not listed are left open.

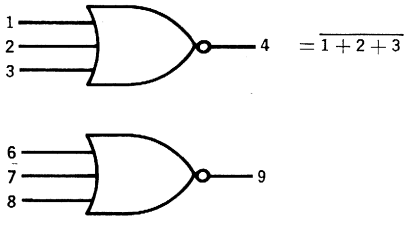
MC915 • MC815

Available in TO-100 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Two 3-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

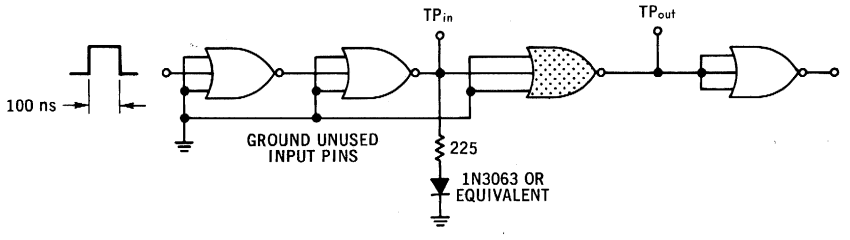


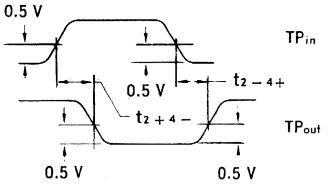
TYPICAL RESISTANCE VALUES
R1 = 450Ω
R2 = 640Ω



"F" PACKAGE AND "G" PACKAGE PIN-OUTS ARE THE SAME

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC915	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC815	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

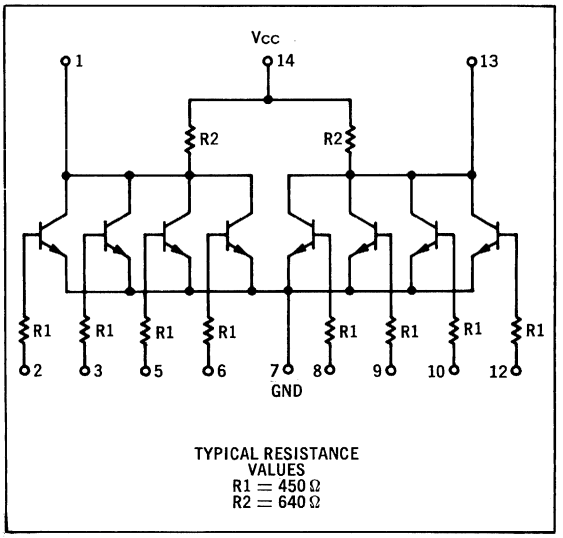
Characteristic	Symbol	Pin Under Test	MC915 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC815 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	2,3	-	10	5
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1,3	-	↓	↓
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	1,2	-	↓	↓
Output Current	I_{A5}	4	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	4	-	1,2,3	10	5
Output Leakage Current	I_{CEX}	4	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	4	-	-	1,2,3	-	5
Output Voltage	V_{out}	4	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	10	5
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	↓
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	4	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	10	5
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2	-	↓	↓
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	↓
																	Pulse In	Pulse Out				
Switching Time	t	2+4-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	2	4	-	-	10	5
		2-4+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	2	4	-	-	10	5

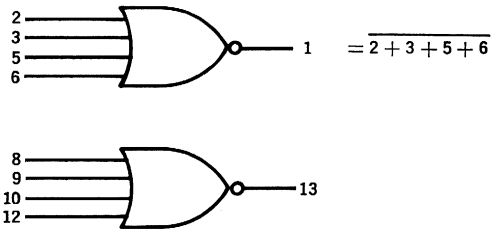
Ground inputs of gate not under test. Other pins not listed are left open.

MC925 • MC825

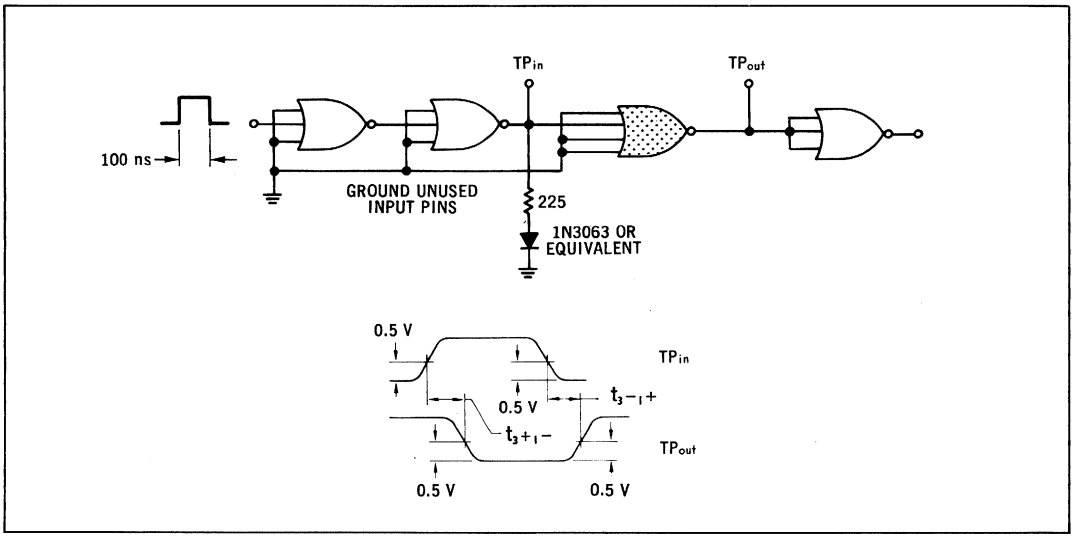
Available in TO-86 Flat Package, Add "F" Suffix.

Two 4-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.





SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC925	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC825	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

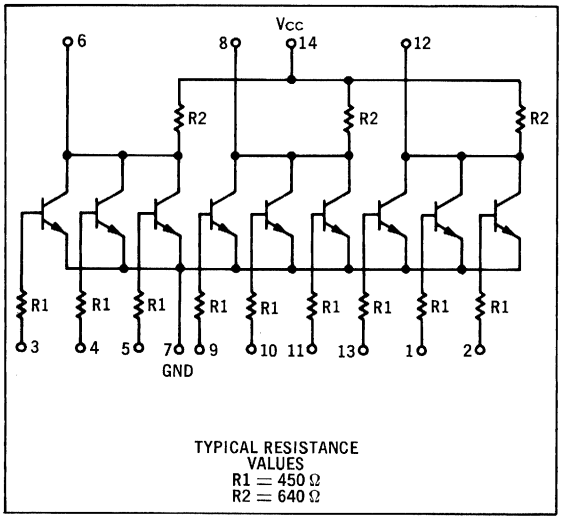
Characteristic	Symbol	Pin Under Test	MC925 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC825 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	2	-	3,5,6	-	14	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,5,6	-	↓	↓
		5	-		-		-			-		-		-			5	-	2,3,6	-		
		6	-		-		-			-		-		-			6	-	2,3,5	-		
Output Current	I_{A5}	1	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	1	-	2,3,5,6	14	7
Output Leakage Current	I_{CEX}	1	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	1	-	-	2,3,5,6	-	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	3,5,6,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	2,5,6,7
			-		-		-			-		-		-			-	5	-	-		2,3,6,7
			-		-		-			-		-		-			-	6	-	-		2,3,5,7
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	3,5,6,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	2,5,6,7
			-		-		-			-		-		-			-	-	5	-		2,3,6,7
			-		-		-			-		-		-			-	-	6	-		2,3,5,7
																	Pulse In	Pulse Out				
Switching Time	t	3+1-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	3	1	-	-	14	2,5,6,7
		3-1+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	3	1	-	-	14	2,5,6,7

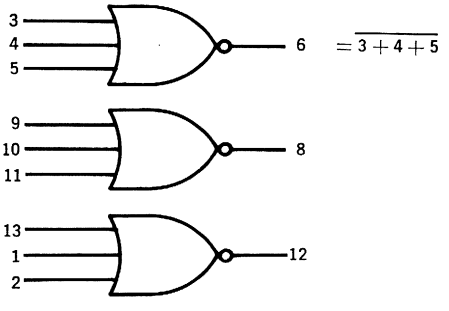
Ground inputs of gate not under test. Other pins not listed are left open.

MC992 • MC892

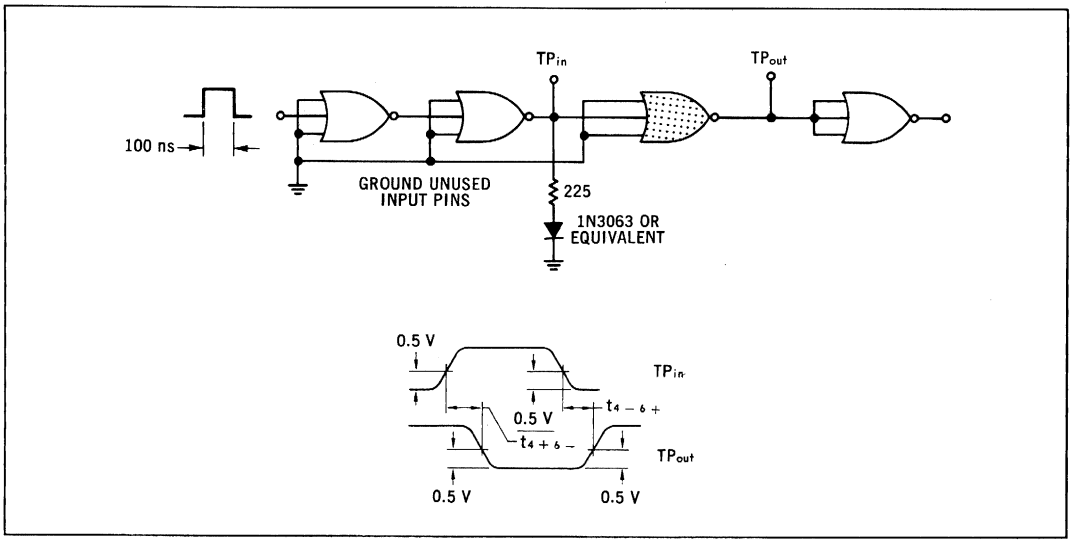
Available in TO-86 Flat Package, Add "F" Suffix.

Three 3-input positive logic NOR gates in a single package may be used independently, paralleled for increased number of inputs (subject to loading rules), or cross coupled to form bistable elements.





SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC992	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC892	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

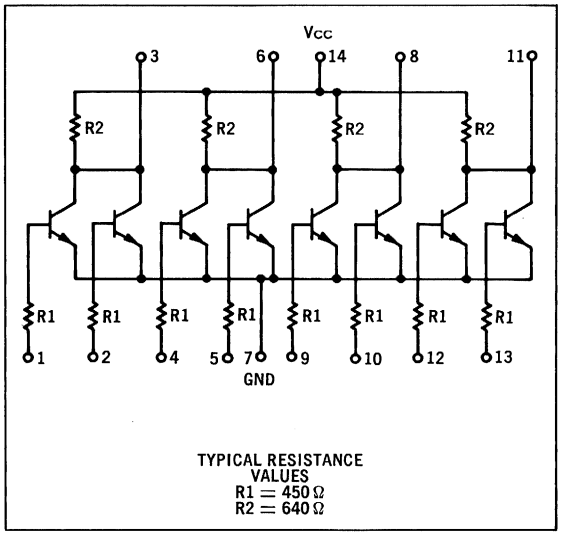
Characteristic	Symbol	Pin Under Test	MC992 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC892 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	3	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	3	-	4,5	-	14	7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	4	-	3,5	-	↓	↓
		5	-		-		-			-		-		-			5	-	3,4	-		
Output Current	I_{A5}	6	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	6	-	3,4,5	14	7
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	6	-	-	3,4,5	-	7
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	-	-	14	4,5,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	4	-	-	↓	3,5,7
			-		-		-			-		-		-			-	5	-	-		3,4,7
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	3	-	14	4,5,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	4	-	↓	3,5,7
			-		-		-			-		-		-			-	-	5	-		3,4,7
																	Pulse In	Pulse Out				
Switching Time	t	4+6-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	4	6	-	-	14	3,5,7
		4-6+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	4	6	-	-	14	3,5,7

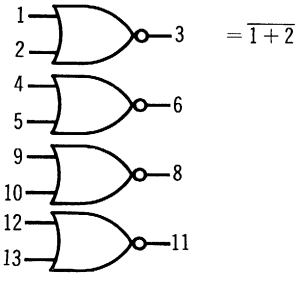
Ground inputs of gates not under test. Other pins not listed are left open.

MC924 • MC824

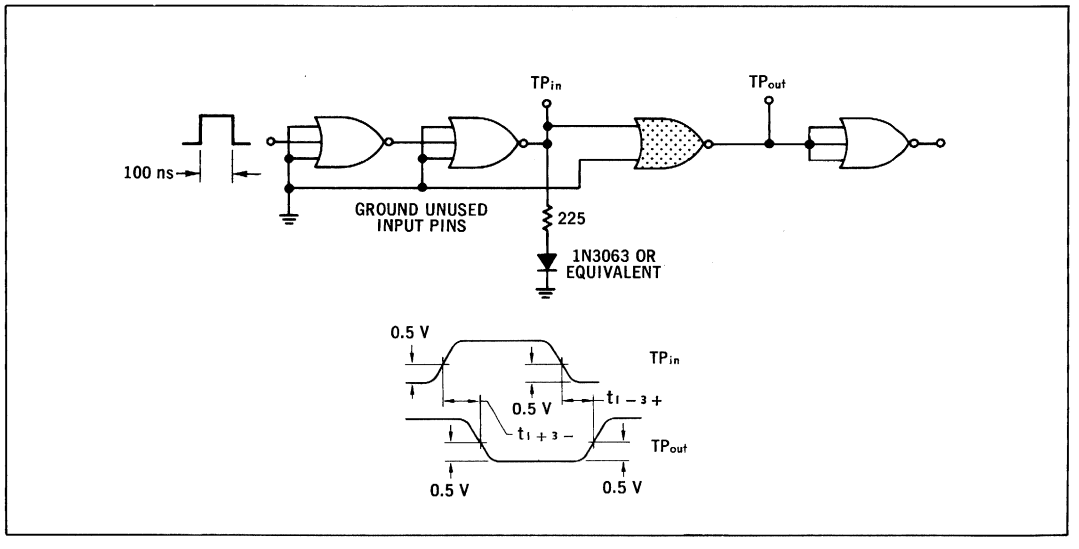
Available in TO-86 Flat Package, Add "F" Suffix.

This gate element consists of four 2-input positive logic NOR gate circuits in a single package. The gate circuits may be used independently, or connected together to form flip-flops or non-inverting gates.





SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC924	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC824	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

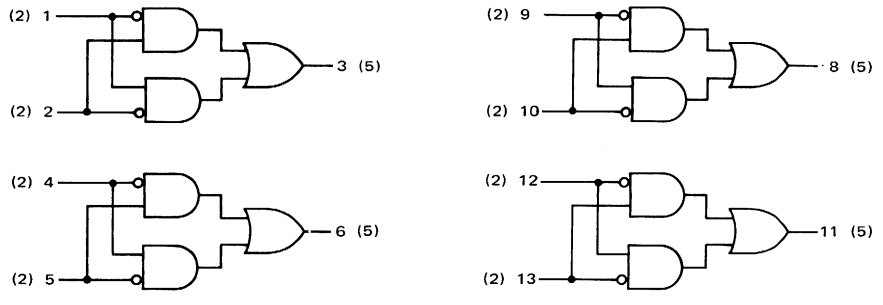
Characteristic	Symbol	Pin Under Test	MC924 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC824 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	1	-	2	-	14	7
		2	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	2	-	1	-	14	7
Output Current	I_{A5}	3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	3	-	-	1,2	14	7
Output Leakage Current	I_{CEX}	3	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	-	3	-	1,2	-	7
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	2,7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	1,7
Saturation Voltage	$V_{CE(sat)}$	3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	2,7
		3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	1,7
																	Pulse In	Pulse Out				
Switching Time	t	1+3-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	1	3	-	-	14	2,7
		1-3+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	1	3	-	-	14	2,7

Ground inputs of gates not under test. Other pins not listed are left open.

MC971 • MC871

Available in TO-86 flat package, add "F" suffix

Four gate arrays designed to provide the Exclusive OR function. The output is high only if one input is high and all other inputs are low.



POSITIVE LOGIC
$3 = 1\cdot\bar{2} + \bar{1}\cdot 2$

t_{pd} = 12 ns typ
P_D = 72 mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR

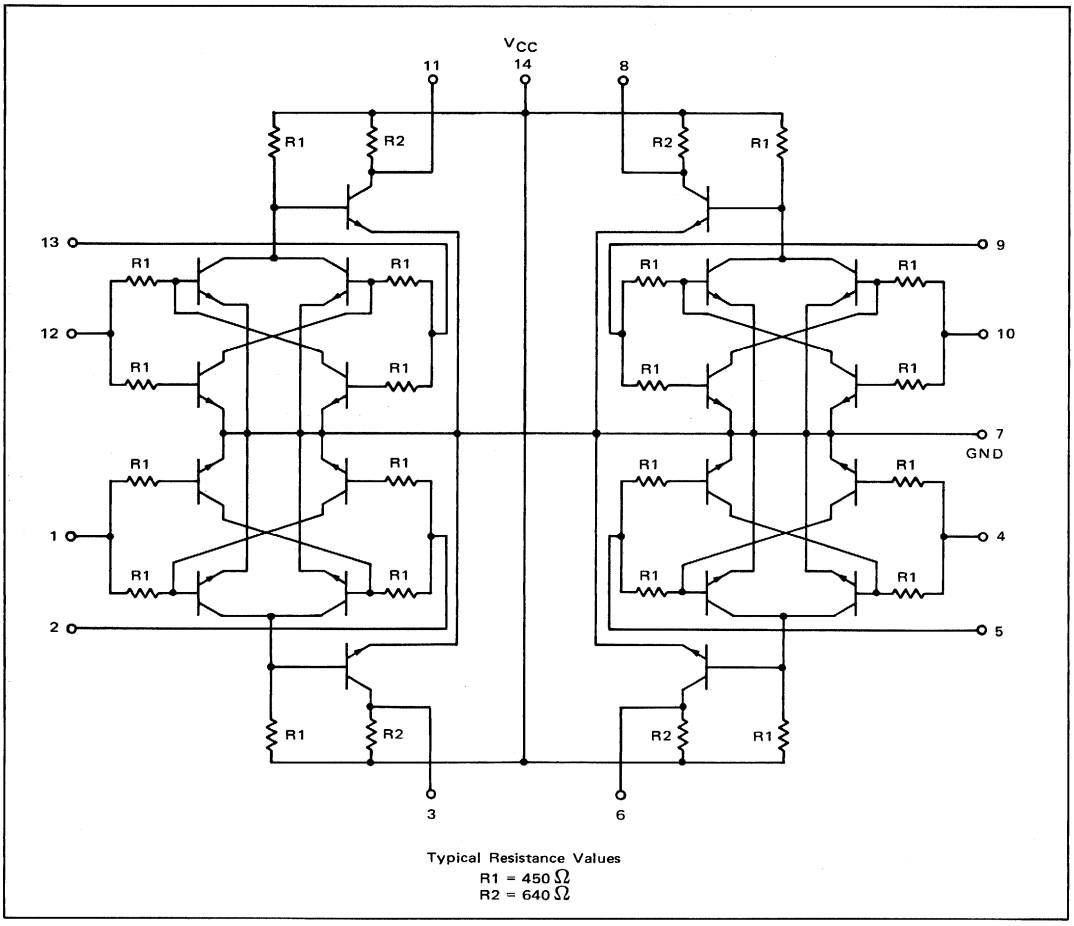
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

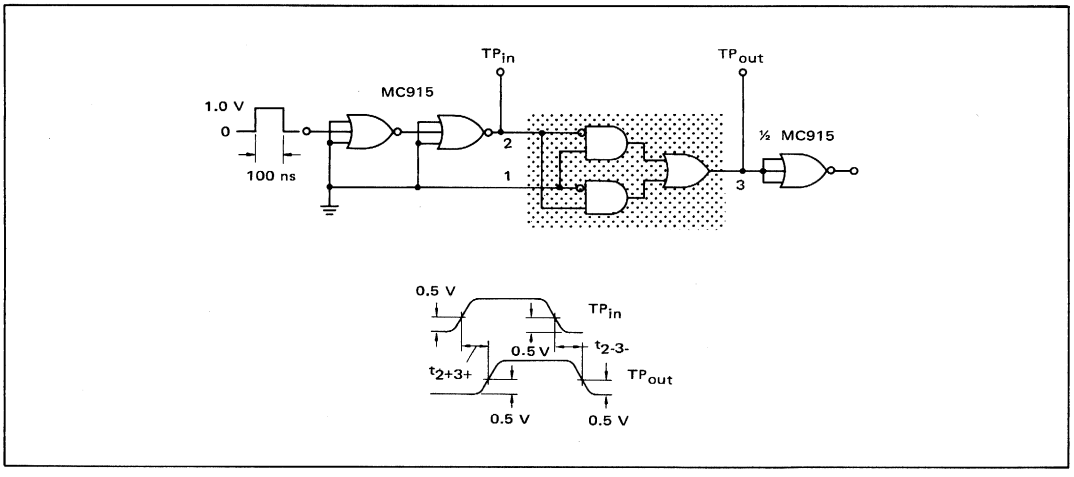
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC971	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC871	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC971 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC871 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	1	-	990	-	870	-	940	μAdc	-	1008	-	900	-	900	μAdc	1	-	-	2	14	7
		2	-	990	-	870	-	940	μAdc	-	1008	-	900	-	900	μAdc	2	-	-	1	14	7
Output Current	I_{A5}	3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	1,3	-	2	14	7
		3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	2,3	-	1	14	7
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	-	-	1,2	14	7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1,2	-	-	14	7
Switching Time																	Pulse In		Pulse Out			
	t	1+3-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	2	3	-	14	7
		1-3+	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	1	2	↓	-	↓	↓
		2+3+	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	2	-	↓	1	↓	↓
		2-3-	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	2	-	↓	1	↓	↓

Ground inputs of gates not under test. Other pins not listed are left open.



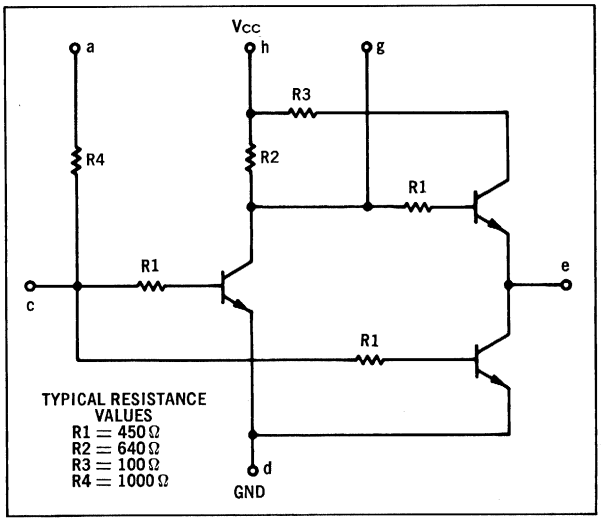
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

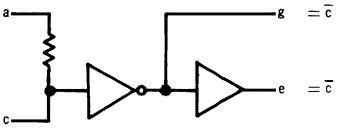


MC900 • MC800

Available in TO-99 metal can, add "G" suffix.
Available in TO-91 flat package, add "F" suffix.

The buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input, the differentiation of input waveforms, and various multivibrator applications.



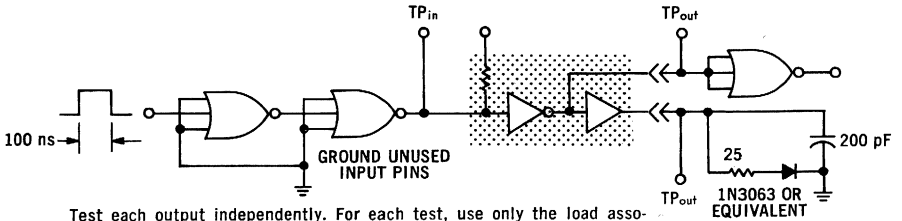


Outputs e and g may not be used simultaneously

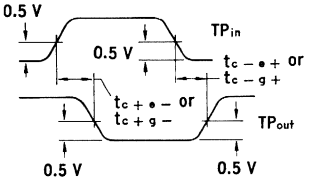
PIN CONNECTIONS

SCHEMATIC	a	—	c	d	e	—	g	h
G PACKAGE (TO-99)	1	—	3	4	5	—	7	8
F PACKAGE (TO-91)	.2	3	4	5	7	8	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test. Output not under test should be left open.



ELECTRICAL CHARACTERISTICS

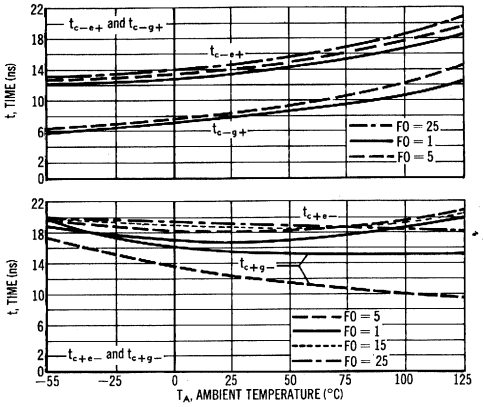
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC900	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC800	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC900 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC800 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2\,I_{in}$	c	-	990	-	870	-	940	μAdc	-	1010	-	900	-	900	μAdc	c	-	-	-	h	-	d
Output Current	I_{AB}	e	12.4	-	12.7	-	11.8	-	mAdc	12.6	-	11.9	-	11.25	-	mAdc	-	e	-	c	h	-	d
	I_{A5}	g	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	g	-	c	h	-	d
Output Voltage	V_{out}	e	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	c	-	-	h	e	d
		g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	c	-	-	h	-	d
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	c	-	h	e	d
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	c	-	h	-	↓
		g	-		-		-			-		-		-			-	-	-	-	a, h	-	
Switching Time	t	c+e-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	Pulse In: c	Pulse Out: e	-	-	h	-	d
		c-e+	-	-	-	45	-	-	↓	-	-	-	45	-	-	↓	↓	e	-	-	↓	-	↓
		c+g-	-	-	-	28	-	-		-	-	-	28	-	-			g	-	-		-	
		c-g+	-	-	-	32	-	-		-	-	-	32	-	-			g	-	-		-	

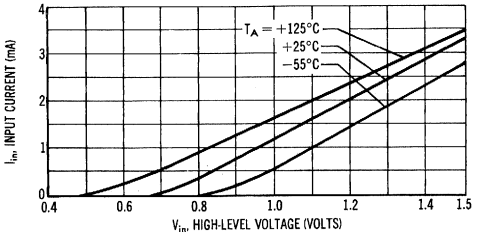
Pins not listed are left open.

* Resistor Value to V_{CC}

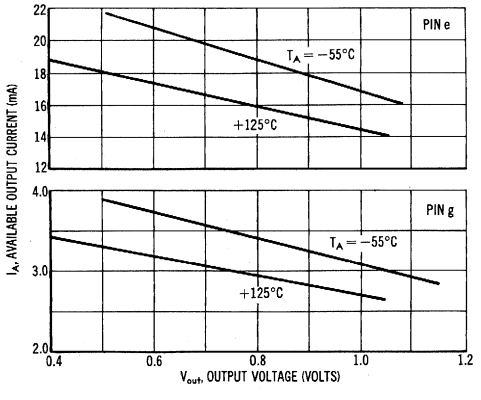
SWITCHING CHARACTERISTICS



INPUT CURRENT

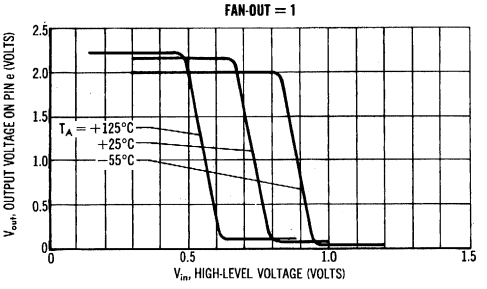


AVAILABLE OUTPUT CURRENT

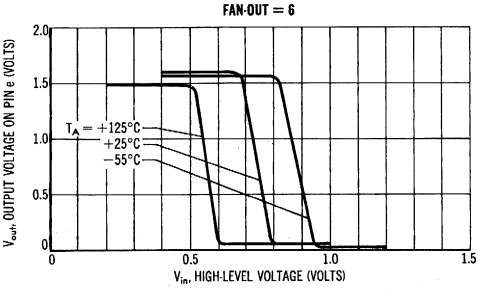


OUTPUT VOLTAGE

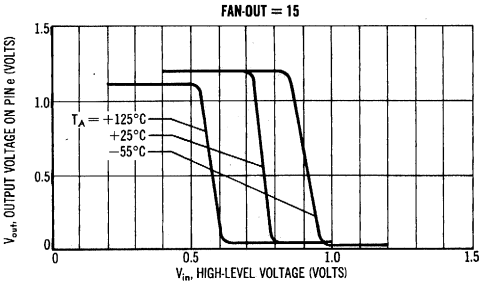
FAN-OUT = 1



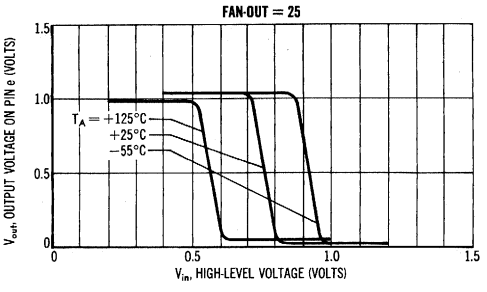
FAN-OUT = 6



FAN-OUT = 15



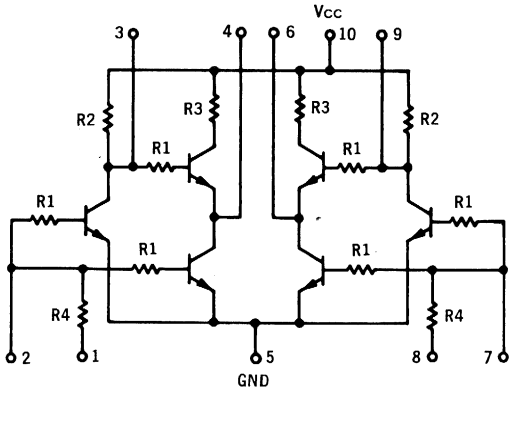
FAN-OUT = 25



MC999 • MC899

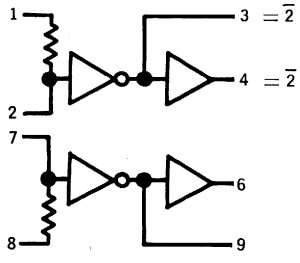
Available in TO-100 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

The dual buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input, the differentiation of input waveforms and various multivibrator applications.



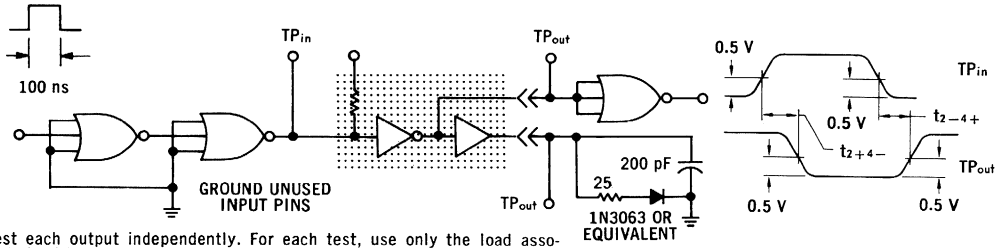
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω
R4 = 1.0 kΩ

"F" PACKAGE AND "G" PACKAGE PIN-OUTS ARE THE SAME



Outputs 3 and 4 may not be used simultaneously
Outputs 9 and 6 may not be used simultaneously

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test. Output not under test should be left open.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC999	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC899	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

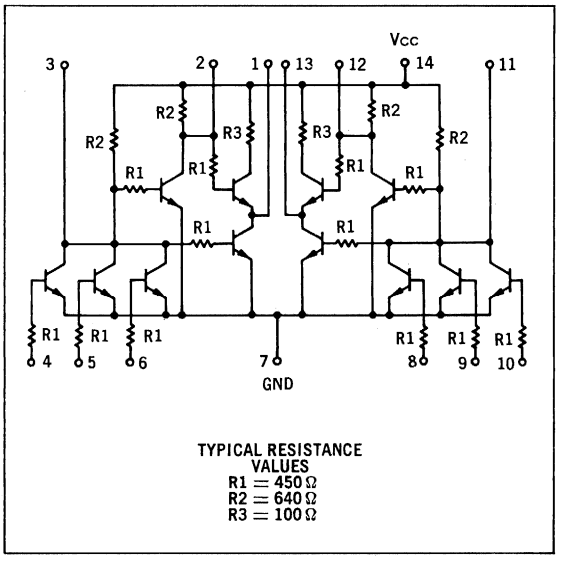
Characteristic	Symbol	Pin Under Test	MC999 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC899 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Grd
Input Current	$2\,I_{in}$	2	-	990	-	870	-	940	μAdc	-	1010	-	900	-	900	μAdc	2	-	-	-	10	-	5
Output Current	I_{A5}	3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	3	-	2	10	-	5
	I_{AB}	4	12.4	-	12.7	-	11.8	-	mAdc	12.6	-	11.9	-	11.25	-	mAdc	-	4	-	2	10	-	5
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	10	-	5
		4	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	10	4	5
Saturation Voltage	$V_{CE(sat)}$	3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	10	-	5
		3	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	-	-	1,10	-	↓
		4	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	2	-	10	4	↓
Switching Time	t	2+3-	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	Pulse In: 2	Pulse Out: 3	-	-	10	-	5
		2-3+	-	-	-	32	-	-		-	-	-	32	-	-		↓	3	-	-	↓	-	↓
		2+4-	-	-	-	30	-	-		-	-	-	30	-	-			4	-	-		-	
		2-4+	-	-	-	45	-	-		-	-	-	45	-	-		↓	4	-	-	↓	-	↓

Ground inputs of buffer not under test. Other pins not listed are left open.

* Resistor value to V_{CC}

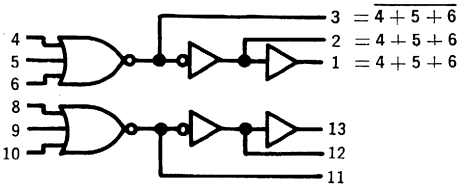
MC988 • MC888

Available in TO-86 Flat Package, Add "F" Suffix.



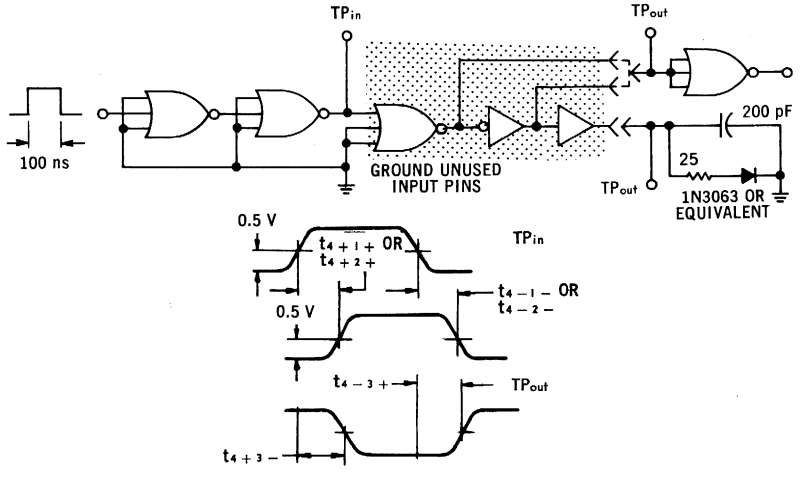
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω

Two 3-input positive logic NOR gates, each followed by an inverting and a non-inverting high fan-out amplifier, are provided in a single package. For each section, the output from each stage is available. If more than one output is used, however, the full loading factors cannot be employed since each output provides the drive for the succeeding stage.



Outputs 1, 2, or 3 may not be used simultaneously.
Outputs 11, 12, or 13 may not be used simultaneously.

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



Test each output independently. For each test, use only the load associated with the output under test (pin 2 test uses the same load as pin 3 test). Outputs not under test should be left open.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC988	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC888	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

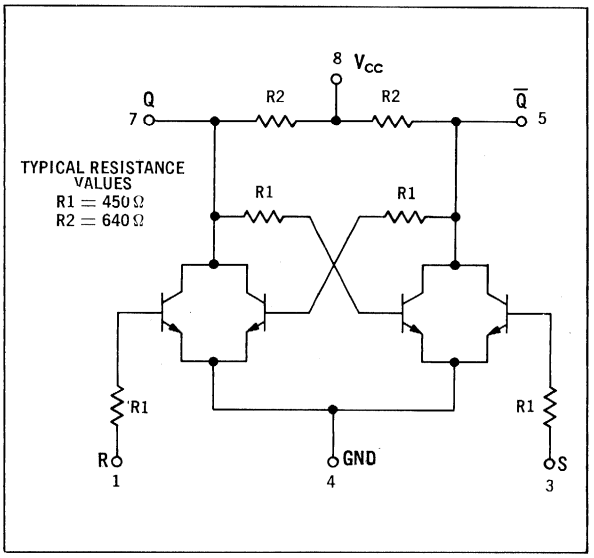
Characteristic	Symbol	Pin Under Test	MC988 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC888 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	4	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	4	-	5,6	-	14	-	7
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	5	-	4,6	-	↓	-	↓
		6	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6	-	4,5	-	↓	-	↓
Output Current	I_{AB}	1	12.4	-	12.7	-	11.8	-	mAdc	12.6	-	11.9	-	11.25	-	mAdc	-	1	-	3	14	-	7,11
	I_{A5}	2	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	2	-	3	↓	-	7,11
	I_{A3}	3	1.48	-	1.52	-	1.41	-	↓	1.51	-	1.43	-	1.35	-	↓	-	3	-	4,5,6	↓	-	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	-	-	14	1	4,5,6,7,11
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	-	4,5,6,7,11
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	6	-	-	↓	-	4,5,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	-	-	↓	-	4,6,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	4	-	-	↓	-	5,6,7
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	3	-	14	1	4,5,6,7,11
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	-	4,5,6,7,11
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	6	-	↓	-	4,5,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	5	-	↓	-	4,6,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	4	-	↓	-	5,6,7
																	Pulse In	Pulse Out					
Switching Time	t	4+1+	-	-	-	65	-	-	ns	-	-	-	65	-	-	ns	4	1	-	-	14	-	5,6,7
		4-1-	-	-	-	58	-	-	↓	-	-	-	58	-	-	↓	4	1	-	-	↓	-	↓
		4+2+	-	-	-	42.5	-	-	↓	-	-	-	42.5	-	-	↓	4	2	-	-	↓	-	↓
		4-2-	-	-	-	42.5	-	-	↓	-	-	-	42.5	-	-	↓	4	2	-	-	↓	-	↓
		4+3-	-	-	-	20	-	-	↓	-	-	-	20	-	-	↓	4	3	-	-	↓	-	↓
		4-3+	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	4	3	-	-	↓	-	↓

Ground inputs of buffer not under test. Other pins not listed are left open.

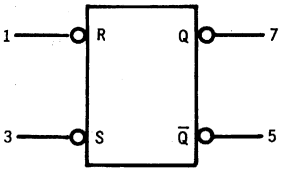
* Resistor Value to V_{CC}.

MC902 • MC802

Available in TO-99 Metal Can, Add "G" Suffix

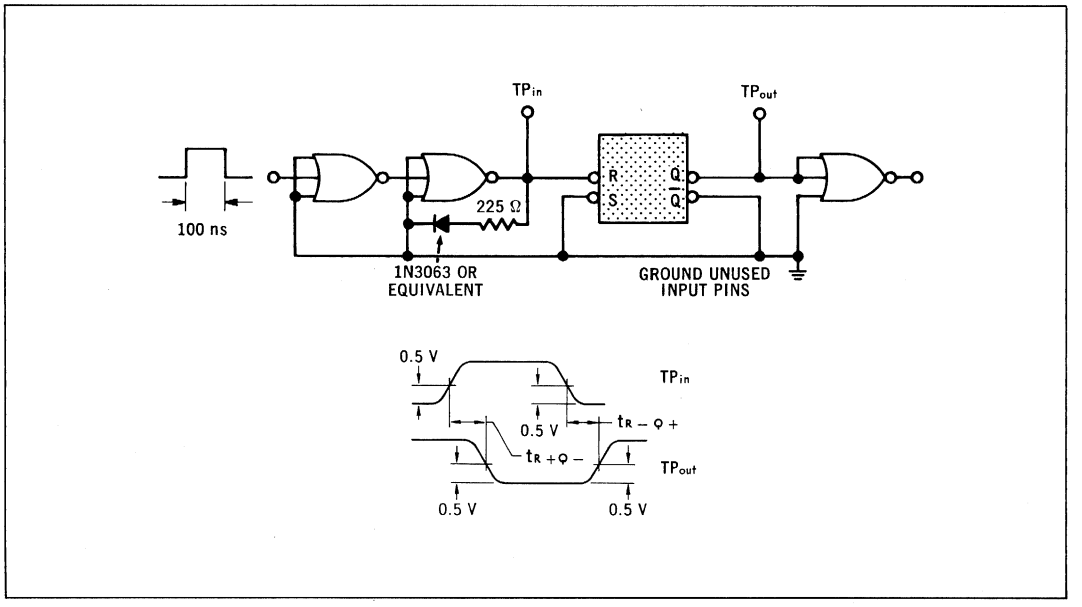


This flip-flop is formed by internally cross-coupling two basic RTL NOR gates.



R	S	Q^{n+1}
0	0	Q^n
0	1	1
1	0	0
1	1	0

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



ELECTRICAL CHARACTERISTICS

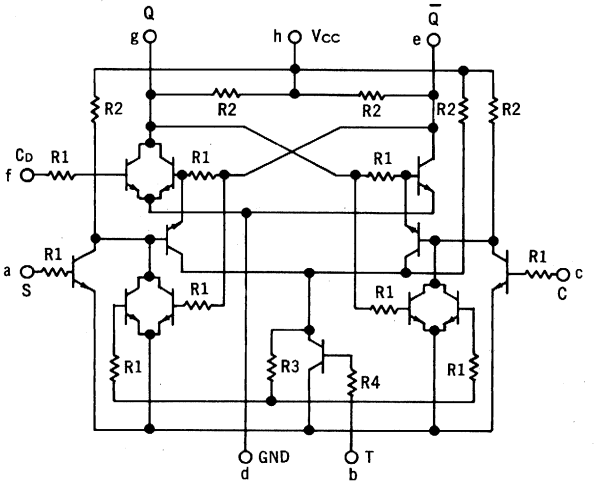
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC902	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC802	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC902 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC802 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	5	-	8	4
		3	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	3	-	7	-	8	4
Output Current	I_{A4}	5	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	5	1	3	8	4
	I_{A4}	7	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	7	3	1	8	4
Output Voltage	V_{out}	5	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	1	-	8	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	7	-	-	↓	↓
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	3	-	↓	↓
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	-	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	5	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1,3	-	8	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1	↓	4,5 †
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1,3	-	↓	4
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	3	↓	4,7 †
																	Pulse In	Pulse Out				
Switching Time	t	1+7-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	1	7	-	-	8	4
		1-7+	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	1	7	-	-	8	4

Pins 2 and 6 omitted. Other pins not listed are left open. † Silicon Diode to Ground

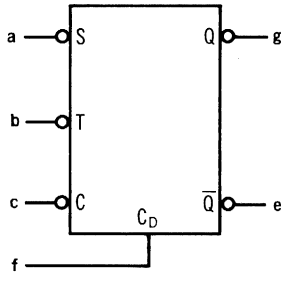
MC916 • MC816

Available in TO-99 Metal Can, Add "G" Suffix
Available in TO-91 Flat Package, Add "F" Suffix



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω

J-K flip-flop with a direct clear input in addition to the clocked input.



CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

① Direct input (C_D) must be low.
② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transistion is denoted t_{n+1}.
③ Q_n is the state of the Q output in the time period t_n.

PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC916	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC816	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC916 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC816 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	e	-	h	d
	$2\,I_{in}$	b	-	990	-	870	-	940	↓	-	1010	-	900	-	900	↓	b	-	a, c, g	-	↓	↓
	I_{in}	c	-	495	-	435	-	470		-	504	-	450	-	450		c	-	g	-		
		f	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	f	-	e	-	↓	↓
Output Current	I_{A3}	e	1.48	-	1.52	-	1.41	-	mAdc	1.51	-	1.43	-	1.35	-	mAdc	-	e	a, f	-	h	d
		e	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	e, f	a	-	↓	d
		g		-		-		-			-		-		-		-	g	c	f		d, e †
Output Voltage	V_{out}	g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	f	-	-	h	
		g‡#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	a, c	-	-		
		g‡	-		-		-			-		-		-			-	c	-	a		d, e
		g‡§	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	-	a, c	↓	d, f
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	-	f	h	d, e †
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	f	-	↓	d, e
		g	-		-		-			-		-		-			-	-	-	-		d, g †
Turn-On Voltage	V_{on}	g‡§	1014	-	815	-	674	-	mVdc	909	-	844	-	710	-	mVdc	-	a, c	-	-	h	d, f
		g‡	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	a	-	c	↓	
		g‡#*		-		-		-			-		-		-		-	-	-	a, c		

† Silicon Diode to Ground

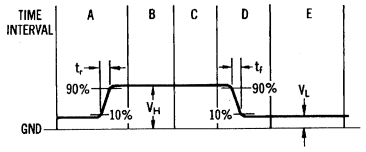
* MC916 pin g loaded by: 1.52 mAdc (+25°C), 1.48 mAdc (−55°C), 1.41 mAdc (+125°C); MC816 pin g loaded by: 1.42 mAdc (+25°C), 1.51 mAdc (0°C), 1.35 mAdc (+100°C)

Pins not listed are left open.

‡ Pin b = Clock pulse to pin b (see Figure 1).

§ Pin e = LOW, # Pin g = LOW } Set by a momentary ground prior to the application of the negative-going Clock Pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.

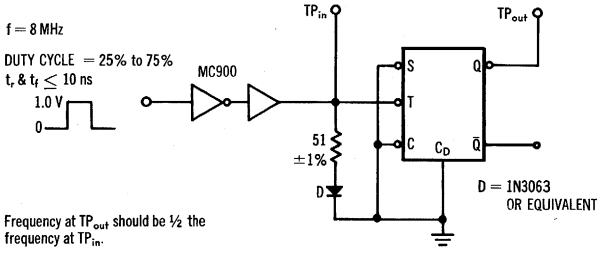
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.

E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



Frequency at TP_{out} should be ½ the frequency at TP_{in}.

MC816		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC916		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.724 V

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

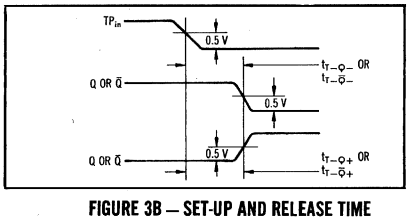


FIGURE 3B — SET-UP AND RELEASE TIME

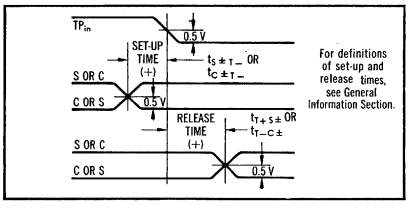
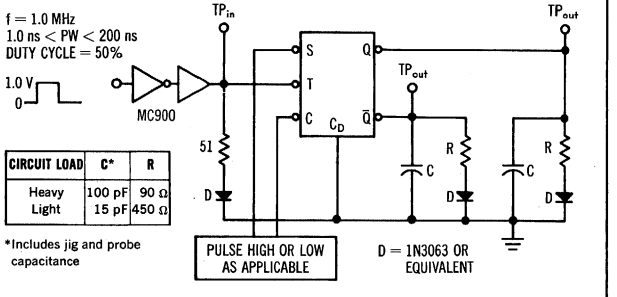


FIGURE 3C — TEST CIRCUIT



CIRCUIT LOAD	C*	R
Heavy	100 pF	90 Ω
Light	15 pF	450 Ω

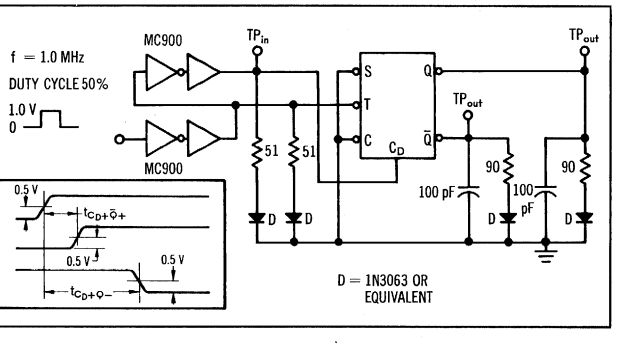
*Includes jig and probe capacitance

SWITCHING TIMES

Test	Figure No.	Maximum Over Full Temperature Range (ns)
t_{T-Q-}	3A, 3C	60
$t_{T-\bar{Q}-}$	3A, 3C	60
t_{T-Q+}	3A, 3C	100
$t_{T-\bar{Q}+}$	3A, 3C	100
$t_{S\pm T-}$	3B, 3C	50
$t_{C\pm T-}$	3B, 3C	50
$t_{T-S\pm}$	3B, 3C	50
$t_{T-C\pm}$	3B, 3C	50
t_{CD+Q-}	4	50
$t_{CD+\bar{Q}+}$	4	90

1. Change of state occurs on trailing edge of clock pulse.
2. With a high level on C_D, and with the proper SET and CLEAR inputs for a low level at $\bar{Q}$, $\bar{Q}$ will be high except for a short period after the negative-going edge of a clock pulse. $\bar{Q}$ will go low for up to 50 ns, and then return to a high level within 100 ns after a negative clock transition.

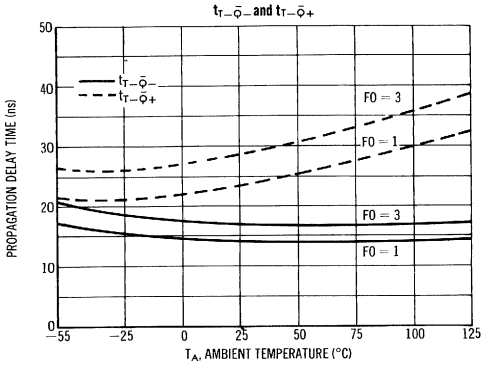
FIGURE 4 — DIRECT CLEAR PROPAGATION DELAY TIME



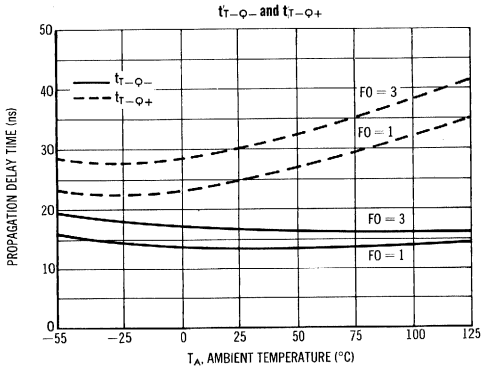
TYPICAL CURVES

TYPICAL PROPAGATION DELAY TIME

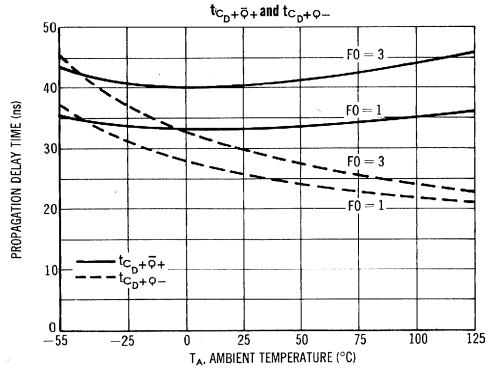
$t_{T-\bar{Q}-}$ and $t_{T-\bar{Q}+}$



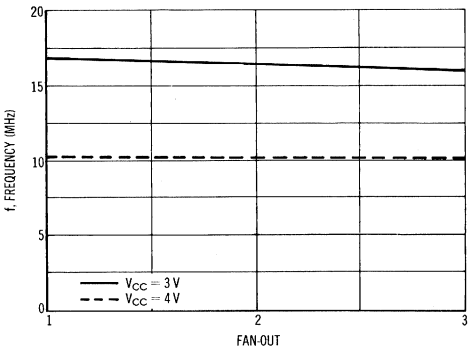
t_{T-Q-} and t_{T-Q+}



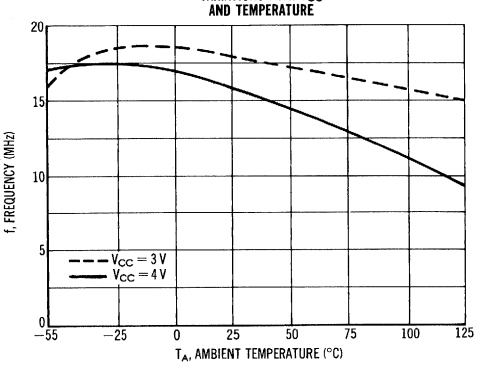
$t_{C_D+\bar{Q}+}$ and t_{C_D+Q-}



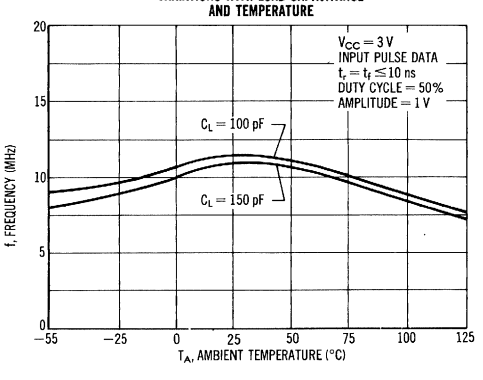
TOGGLE FREQUENCY
VARIATIONS WITH FAN-OUT AND V_{CC}



VARIATIONS WITH V_{CC} AND TEMPERATURE



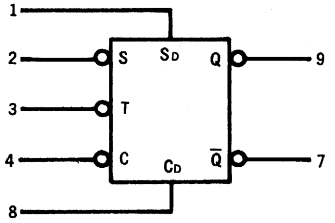
VARIATIONS WITH LOAD CAPACITANCE AND TEMPERATURE



MC926 • MC826

Available in TO-100 Metal Can, Add "G" Suffix
Available in TO-91 Flat Package, Add "F" Suffix

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



t_{pd} = 35 ns typ
P_D = 130 mW typ (Only Clock Input High)
65 mW typ (Inputs Low)

DIRECT INPUT OPERATION①

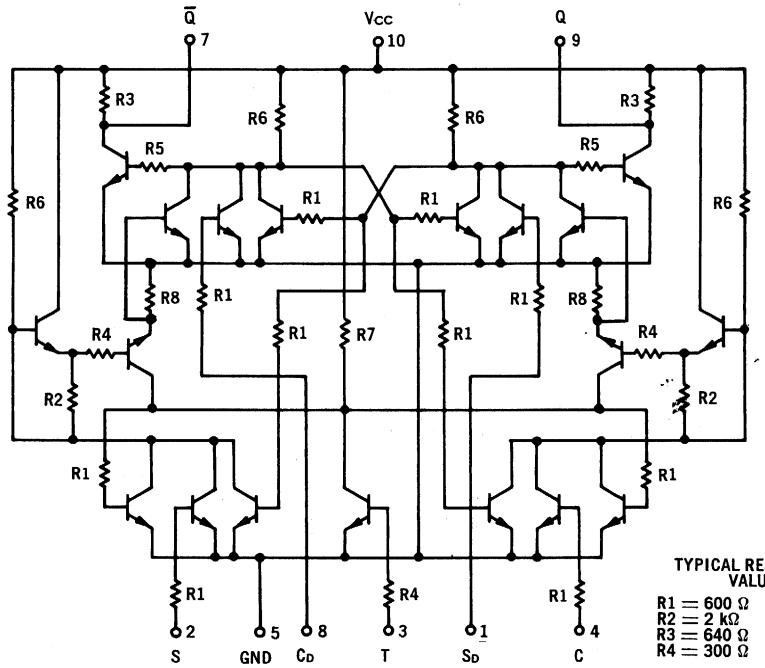
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION③

t_n④		t_{n+1}④	
S	C	Q	$\overline{Q}$
1	1	Q_n⑤	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

① Clock (T) to remain unchanged.
② The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
③ Direct inputs (C_D and S_D) must be low.
④ The time period prior to the negative transistor of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
⑤ Q_n is the state of the Q output in the time period t_n.

"F" PACKAGE AND "G" PACKAGE
PIN-OUTS ARE THE SAME.



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 550 Ω
R2 = 2 kΩ	R6 = 900 Ω
R3 = 640 Ω	R7 = 700 Ω
R4 = 300 Ω	R8 = 3 kΩ

ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC926	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC826	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

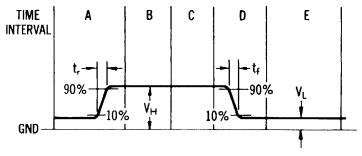
Characteristic	Symbol	Pin Under Test	MC926 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC826 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	-	-	10	5
	I_{in}	2	-	495	-	435	-	470		-	504	-	450	-	450		2	-	8	-		
	$2\ I_{in}$	3	-	990	-	870	-	940		-	1010	-	900	-	900		3	-	2,4	-		
	I_{in}	4	-	495	-	435	-	470		-	504	-	450	-	450		4	-	1	-		
	I_{in}	8	-	495	-	435	-	470		-	504	-	450	-	450		8	-	-	-		
Output Current	I_{A5}	7	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	7,8	1	-	10	5
		9	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	1,9	8	-	10	5
Saturation Voltage	$V_{CE(sat)}$	7	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	1	-	8	10	5
		7#‡	-		-		-			-		-		-			-	2	-	4		
		7#‡	-		-		-			-		-		-			-	-	-	2,4		
		7§‡	-		-		-			-		-		-			-	2,4	-	-		
		9	-		-		-			-		-		-			-	8	-	1		
		9§‡	-		-		-			-		-		-			-	4	-	2		
		9#‡	-		-		-			-		-		-			-	2,4	-	-		
		9§‡	-		-		-			-		-		-			-	-	-	2,4		

§ Pin 1 = High
# Pin 8 = High
Set by momentary application of V_{BOT} prior to the application of the negative going clock pulse.

‡ Pin 3 = ⌐└

Pins not listed are left open.

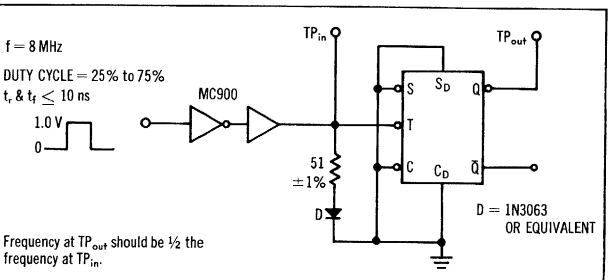
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC826		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC926		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.724 V

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

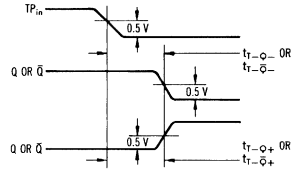
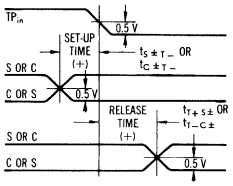
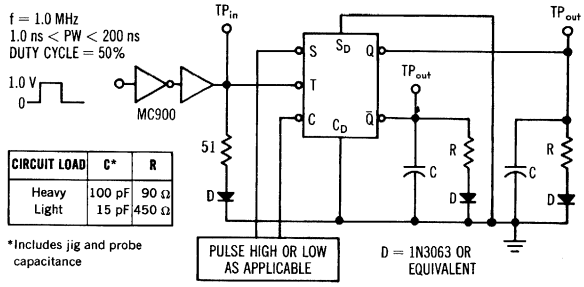


FIGURE 3B — SET-UP AND RELEASE TIME



For definitions of set-up and release times, see General Information Section.

FIGURE 3C — TEST CIRCUIT



CIRCUIT LOAD	C*	R
Heavy	100 pF	90 Ω
Light	15 pF	450 Ω

*Includes jig and probe capacitance

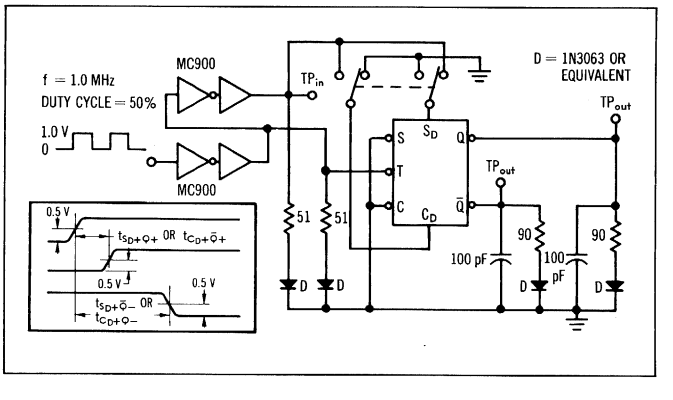
SWITCHING TIMES

Test	Figure No.	Minimum Over Full Temperature Range (ns)	Maximum Over Full Temperature Range (ns)
t_{T-Q-}	3A, 3C	25#	90
$t_{T-\bar{Q}-}$	3A, 3C	25#	90
t_{T-Q+}	3A, 3C	25#	90
$t_{T-\bar{Q}+}$	3A, 3C	25#	90
t_{S+T-}	3B, 3C	—	50
t_{S-T-}	3B, 3C	—	30
t_{C+T-}	3B, 3C	—	50
t_{C-T-}	3B, 3C	—	30
t_{T-S+}	3B, 3C	—	0*
t_{T-S-}	3B, 3C	—	+5*
t_{T-C+}	3B, 3C	—	0*
t_{T-C-}	3B, 3C	—	+5*
t_{C_D+} or t_{S_D+} to output −	4	—	90
t_{C_D+} or t_{S_D+} to output +	4	—	70

Lightly loaded

* Negative switching time means the inputs can momentarily change before the clock pulse transition.

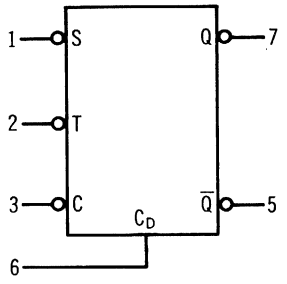
FIGURE 4 — DIRECT CLEAR PROPAGATION DELAY TIME



MC974 • MC874

Available in TO-99 metal can, add "G" suffix.

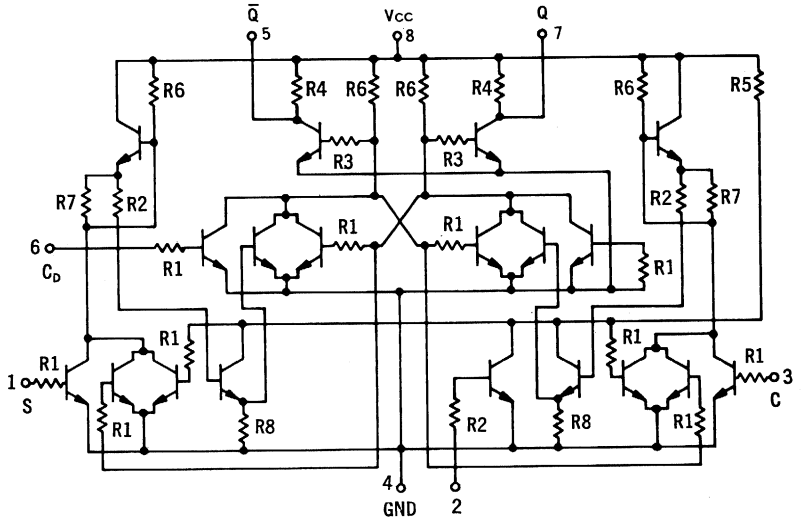
J-K flip-flop with a direct clear input in addition to the clocked inputs.



CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

① Direct input (C_D) must be low.
② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
③ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 700 Ω
R2 = 300 Ω	R6 = 900 Ω
R3 = 550 Ω	R7 = 2k Ω
R4 = 640 Ω	R8 = 3k Ω

ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC974	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC874	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC974 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC874 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	6	-	8	4
	$2\ I_{in}$*	2	-	990	-	870	-	940		-	1008	-	900	-	900		2	-	1,3	-		
	I_{in}	3 Δ	-	495	-	435	-	470		-	504	-	450	-	450		3	-	-	-		
	I_{in}	6	-	495	-	435	-	470		-	504	-	450	-	450		6	-	-	-		
Output Current	I_{A5}	5	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	5,6	-	-	8	4
		7 Δ	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	7	-	-	8	4
Saturation Voltage	$V_{CE(sat)}$	5‡§	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	1	-	3	8	4
		5‡§	-		-		-			-		-		-			-	-	-	1,3		
		5Δ§	-		-		-			-		-		-			-	1,3	-	-		
		7Δ	-		-		-			-		-		-			-	6	-	-		
		7‡§	-		-		-			-		-		-			-	1,3	-	-		
		7Δ§	-		-		-			-		-		-			-	3	-	1		
		7Δ§	-		-		-			-		-		-			-	-	-	1,3		

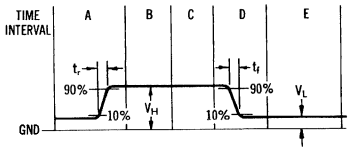
Pins not listed are left open.

Δ Preset the flip-flop by the following procedure:
(1) Momentarily apply V_{BOT} to pin 6 to preclear flip-flop.
(2) After V_{BOT} is removed from pin 6, ground pins 1 and 3.
(3) Apply a negative-going clock pulse to pin 2 (see note §) while pins 1 and 3 are still grounded. This changes the state of the flip-flop to the SET condition.
(4) Remove the grounds from pins 1 and 3, and proceed with the test.

‡ Momentarily apply V_{BOT} to pin 6 prior to the arrival of the negative-going clock pulse to effect a change of state.

§ Clock Pulse to pin 2:

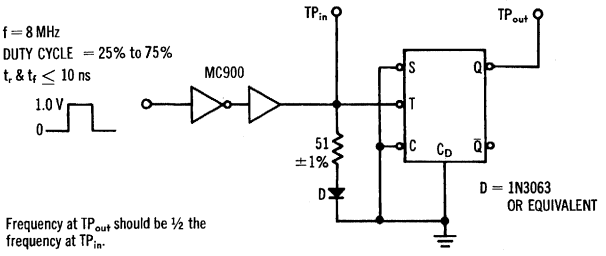
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC874		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC974		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.724 V

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

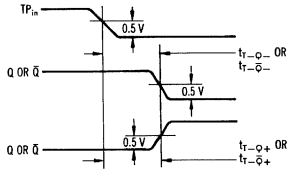
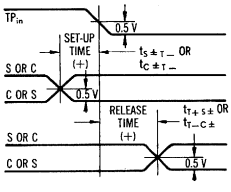
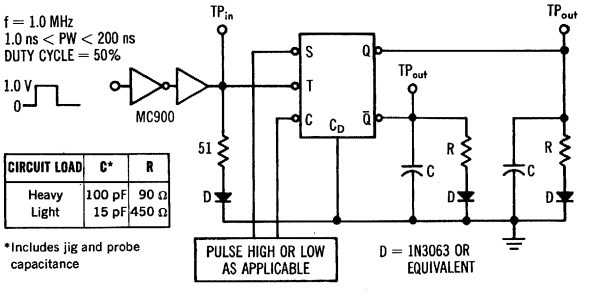


FIGURE 3B — SET-UP AND RELEASE TIME



For definitions of set-up and release times, see General Information Section.

FIGURE 3C — TEST CIRCUIT



CIRCUIT LOAD	C*	R
Heavy	100 pF	90 Ω
Light	15 pF	450 Ω

*Includes jig and probe capacitance

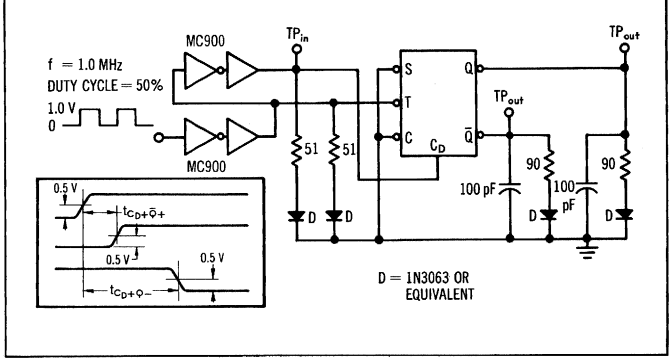
SWITCHING TIMES

Test	Figure No.	Minimum Over Full Temperature Range (ns)	Maximum Over Full Temperature Range (ns)
t_{T-Q-}	3A, 3C	25#	90
$t_{T-\bar{Q}-}$	3A, 3C	25#	90
t_{T-Q+}	3A, 3C	25#	90
$t_{T-\bar{Q}+}$	3A, 3C	25#	90
t_{S+T-}	3B, 3C	—	50
t_{S-T-}	3B, 3C	—	30
t_{C+T-}	3B, 3C	—	50
t_{C-T-}	3B, 3C	—	30
t_{T-S+}	3B, 3C	—	0*
t_{T-S-}	3B, 3C	—	+5*
t_{T-C+}	3B, 3C	—	0*
t_{T-C-}	3B, 3C	—	+5*
t_{CD+Q-}	4	—	90
$t_{CD+\bar{Q}+}$	4	—	70

Lightly loaded

* Negative switching time means the inputs can momentarily change before the clock pulse transition.

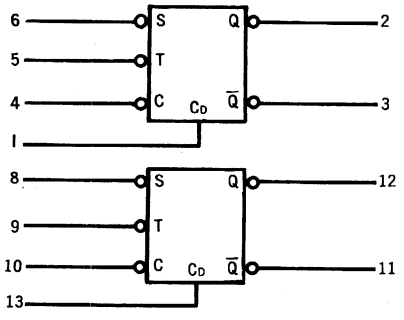
FIGURE 4 — DIRECT CLEAR PROPAGATION DELAY TIME



MC990 • MC890

Available in TO-86 flat package, add "F" suffix.

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



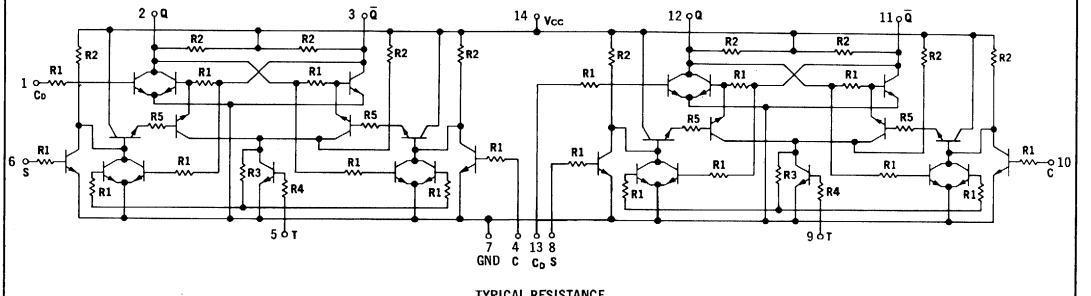
CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

① Direct input (C_D) must be low

② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

③ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω
R5 = 300 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC990	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC890	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC990 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC890 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	3	-	14	4,5,6,7
	I_{in}	4	-	495	-	435	-	470		-	504	-	450	-	450		4	-	2	-		1,5,6,7
	$2\ I_{in}$	5	-	990	-	870	-	940		-	1010	-	900	-	900		5	-	4,6	-		1,7
	I_{in}	6	-	495	-	435	-	470		-	504	-	450	-	450		6	-	3	-		1,4,5,7
Output Current	I_{A3}	2#	1.48	-	1.52	-	1.41	-	mAdc	1.51	-	1.43	-	1.35	-	mAdc	-	2	4	1	14	5,6,7
		3		-		-		-			-		-		-		-	3	1,6	-		4,5,7
		3		-		-		-			-		-		-		-	1,3	6	-		4,5,7
Output Voltage	V_{out}	2	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	3,4,5,6,7
		2Δ§	-		-		-			-		-		-			-	4,6	-	-		1,7
		2#§	-		-		-			-		-		-			-	4	-	6		1,7
		2#§	-		-		-			-		-		-			-	-	-	4,6		1,7
		2†	-		-		-			-		-		-			-	-	-	-		1,6,7
		2*	-		-		-			-		-		-			-	-	-	-		1,6,7
		3#§	-	710	-		-	320		-	574	-		-	370		-	4,6	-	-		1,7
		3Δ§	-		-		-			-		-		-			-	6	-	4		
		3Δ§	-		-		-			-		-		-			-	-	-	4,6		
Saturation Voltage	$V_{CE(sat)}$	2	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	3,4,5,6,7
		2Δ	-		-		-			-		-		-			-	-	-	-		1,4,5,6,7
		3#	-		-		-			-		-		-			-	-	-	1		4,5,6,7
Turn On Voltage	V_{on}	2‡	-	-	0.815	-	-	-	Vdc	-	-	0.844	-	-	-	Vdc	-	-	-	-	14	1,4,7
		2**	-	-	0.815	-	-	-	Vdc	-	-	0.844	-	-	-	Vdc	-	-	-	-	14	1,4,7

Ground inputs of flip-flop not under test. Pins not listed are left open.

\# Pin 3 = LOW } Set by a momentary ground prior to the application of
Δ Pin 2 = LOW } the negative-going clock pulse.

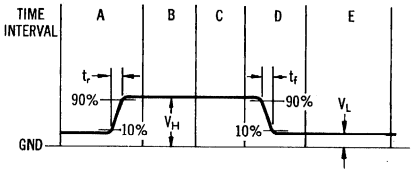
§ Clock Pulse to Pin 5 (See Figure 1)

† Clock Pulse on Pin 5, data pulse on Pin 4 (See Figure 2)
‡ Clock Pulse on Pin 5, data pulse on Pin 6 (See Figure 2)

* Clock Pulse on Pin 5, data pulse on Pin 4, momentary ground on Pin 2 (See Figure 3)
** Clock Pulse on Pin 5, data pulse on Pin 6, momentary ground on Pin 3 (See Figure 3)

CLOCK PULSE DEFINITIONS

FIGURE 1



SEQUENCE OF EVENTS:

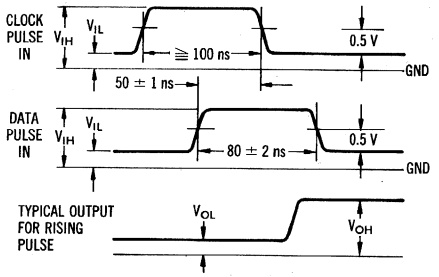
A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC890		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC990		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.674 V

FIGURE 2

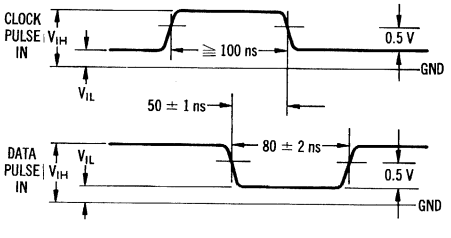


INPUT PULSE REQUIREMENTS:

V_{IL} = 0.200 V max
V_{IH} = 0.894 V min, 1.500 V max
$t_r \leqq$ 10 ns
$t_f \leqq$ 10 ns
f = 1.0 MHz typ

NOTE:
Measurements for output voltages should be taken at least 100 ns after pulses have occurred.

FIGURE 3



INPUT PULSE REQUIREMENTS:

V_{IL} = 0.200 V max
V_{IH} = 0.894 V min, 1.500 V max
$t_r \leqq$ 10 ns
$t_f \leqq$ 10 ns
f = 1.0 MHz typ

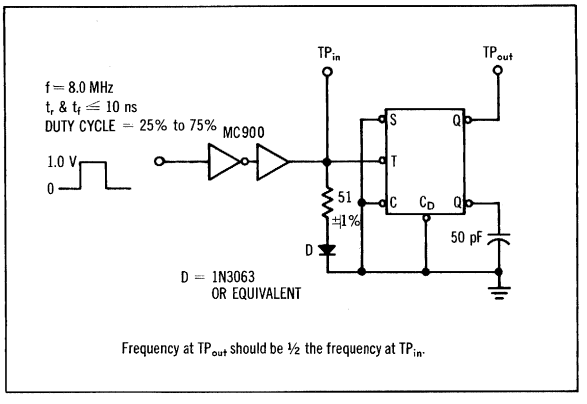
SEQUENCE OF EVENTS:

A. Apply all dc biases required.
B. Apply momentary ground to pin indicated. This sets the flip-flop. Momentary ground must occur before the pulses shown above every time, or the flip-flop will toggle to the wrong condition every alternate pulse.
C. After momentary ground has been released, apply pulses marked above.
D. Measure voltage of designated output after the pulse. Measurements for output voltages should be taken at least 100 ns after pulses have occurred.

SWITCHING TIMES

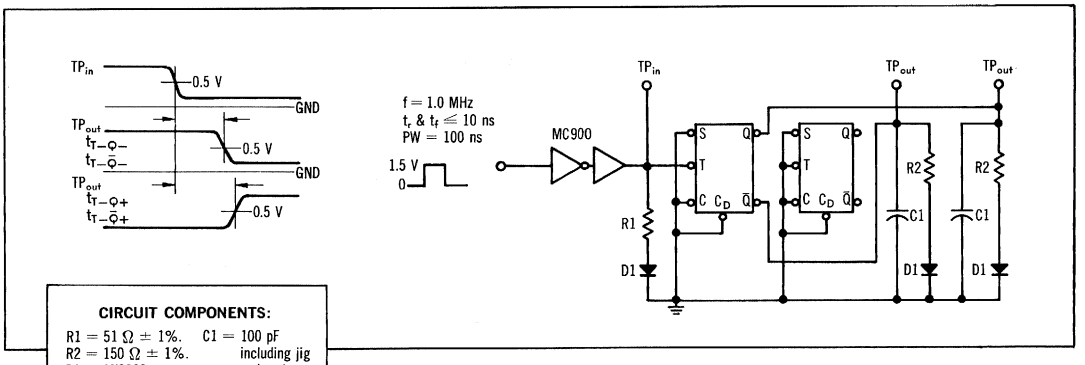
Test	Figure No.	Maximum (ns) @ 25°C Only	Maximum (ns) Over Full Temperature Range
t_{T-Q-}	5	40	60
t_{T-Q+}	5	80	100
$t_{T-\bar{Q}-}$	5	40	60
$t_{T-\bar{Q}+}$	5	80	100
t_{C_D+Q-}	6	—	50
$t_{C_D+\bar{Q}+}$	6	—	90

FIGURE 4 — TOGGLE MODE TEST CIRCUIT



SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 5

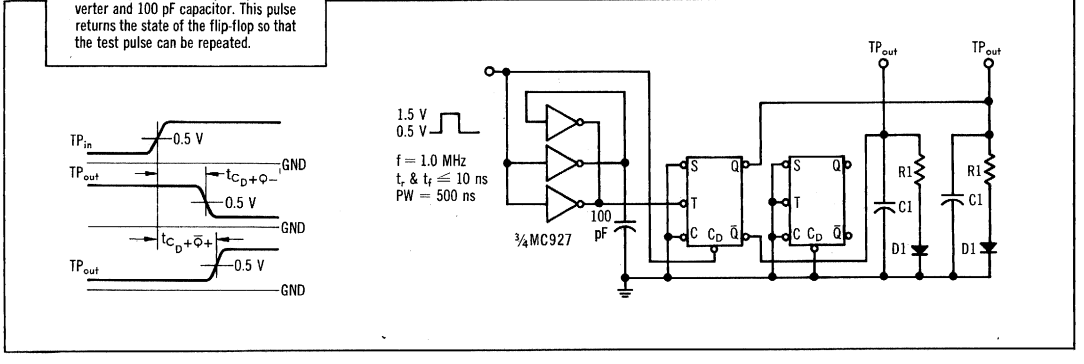


CIRCUIT COMPONENTS:

R1 = 51 Ω ± 1%. C1 = 100 pF including jig and probe.
R2 = 150 Ω ± 1%.
D1 = 1N3063 or equivalent.

NOTE:
The TOG pulse is developed by the inverter and 100 pF capacitor. This pulse returns the state of the flip-flop so that the test pulse can be repeated.

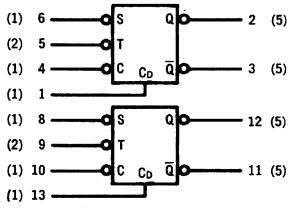
FIGURE 6



MC991 • MC891

Available in TO-86 flat package, add "F" suffix.

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



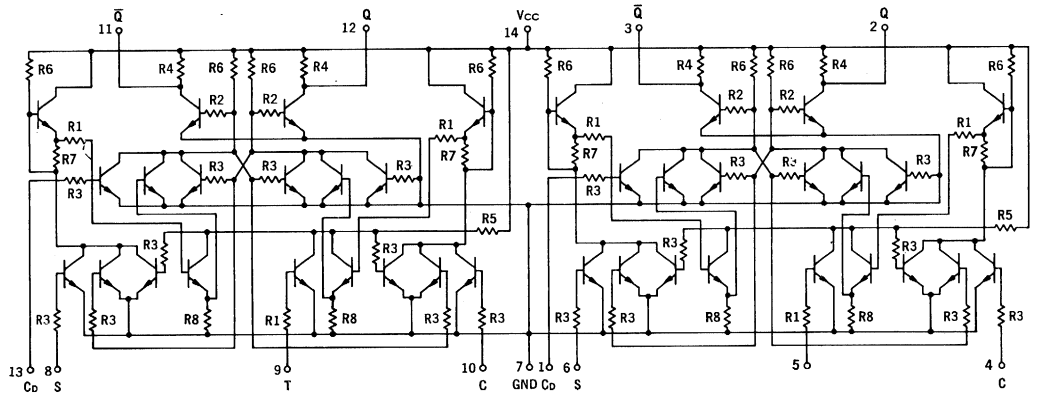
CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

t_{pd} = 40 ns typ
f_{TOG} = 4.0 MHz max
P_D = 155 mW typ (Only Clock Input High)
130 mW typ (Inputs Low)

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.



TYPICAL RESISTANCE VALUES
R1 = 300 Ω R4 = 640 Ω R7 = 2.0 k
R2 = 550 Ω R5 = 700 Ω R8 = 3.0 k
R3 = 600 Ω R6 = 900 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC991	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC891	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC991 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC891 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	4§	-	495	-	435	-	470	μAdc	-	600	-	600	-	570	μAdc	4	-	-	-	14	7
	$2I_{in}$	5	-	990	-	870	-	940		-	1200	-	1200	-	1140		5	-	4, 6	-		
	I_{in}	6	-	495	-	435	-	470		-	600	-	600	-	570		6	-	1	-		
	I_{in}	1	-	495	-	435	-	470		-	600	-	600	-	570		1	-	-	-		
Output Current	I_{A5}	2§	2.47	-	2.54	-	2.35	-	mAdc	3.0	-	3.0	-	2.85	-	mAdc	-	2	-	-	14	7
		3	2.47	-	2.54	-	2.35	-	mAdc	3.0	-	3.0	-	2.85	-	mAdc	-	1, 3	-	-	14	7
Output Voltage	V_{out}	2†⑤	-	710	-	300	-	320	mVdc	-	500	-	400	-	400	mVdc	-	4	-	-	14	1, 7
		2‡④	-		-		-			-		-		-			-	-	-	6		
		2†⑥	-		-		-			-		-		-			-	4	-	-		
		2‡⑦	-		-		-			-		-		-			-	-	-	6		
		3†④	-		-		-			-		-		-			-	-	-	4		
		3‡⑤	-		-		-			-		-		-			-	6	-	-		
		3†⑦	-		-		-			-		-		-			-	-	-	4		
		3‡⑥	-		-		-			-		-		-			-	6	-	-		
Saturation Voltage	$V_{CE(sat)}$	2§	-	200	-	210	-	280	mVdc	-	400	-	300	-	350	mVdc	-	1	-	-	14	7
		2* #	-		-		-			-		-		-			-	4, 6	-	-		
		2*§	-		-		-			-		-		-			-	4	-	6		
		2*§	-		-		-			-		-		-			-	-	-	4, 6		
		3* #	-		-		-			-		-		-			-	6	-	4		
		3* #	-		-		-			-		-		-			-	-	-	4, 6		
		3*§	-		-		-			-		-		-			-	4, 6	-	-		

Ground input pins of flip-flop not under test. Other pins not listed are left open.

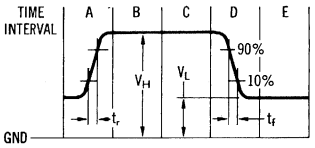
§ Preset the flip-flop by the following procedure:
(1) Momentarily apply V_{BOT} to pin 1 to preclear the flip-flop.
(2) After V_{BOT} is removed from pin 1, ground pins 4 and 6.
(3) Apply a negative-going clock pulse to pin 5 (see note *) while pins 4 and 6 are still grounded. This changes the state of the flip-flop to the SET condition.
(4) Remove the grounds from pins 4 and 6 and proceed with the test.

* Clock pulse to pin 5, see Figure 1.
\# Pin 1 = HIGH, set by a momentary application of V_{BOT} prior to the application of the negative-going clock.

† Clock pulse to pin 5, data pulse to pin 6.
‡ Clock pulse to pin 5, data pulse to pin 4.

④ = See Figure 4.
⑤ = See Figure 5.
⑥ = See Figure 6.
⑦ = See Figure 7.

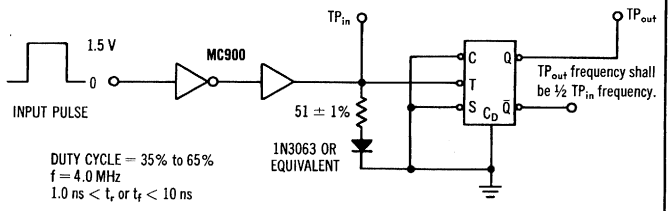
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be < 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC991

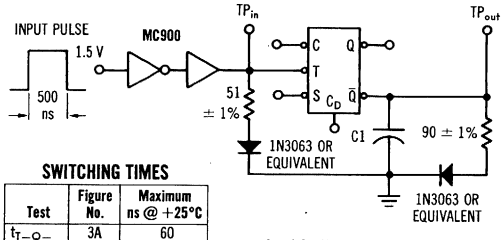
T_A	V_L	V_H
+25°C	+0.565 V ± 10 mV	+0.844 V ± 10 mV
−55°C	+0.710 V ± 10 mV	+1.014 V ± 10 mV
+125°C	+0.320 V ± 10 mV	+0.674 V ± 10 mV

MC891

T_A	V_L	V_H
+25°C	+0.554 V ± 10 mV	+1.430 V ± 10 mV
0°C	+0.574 V ± 10 mV	+1.310 V ± 10 mV
+100°C	+0.370 V ± 10 mV	+1.190 V ± 10 mV

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

FIGURE 3 — SWITCHING TIMES TEST CIRCUIT



SWITCHING TIMES

Test	Figure No.	Maximum ns @ +25°C
t_{T-Q-}	3A	60
t_{T-Q+}	3A	60
$t_{T-\bar{Q}-}$	3A	60
$t_{T-\bar{Q}+}$	3A	60
t_{CD+Q-}	3B	90
$t_{CD+\bar{Q}+}$	3B	70

f = 1.0 MHz
1.0 ns < t_r or t_f < 10 ns

C1 = 100 pF INCLUDING PROBE & JIG CAPACITANCE

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

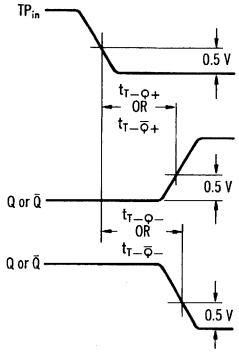
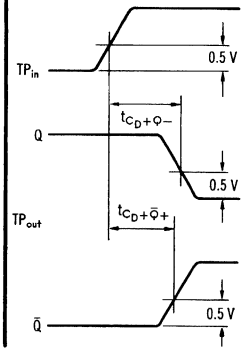
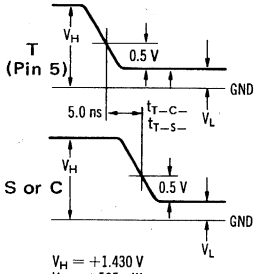


FIGURE 3B — DIRECT CLEAR PROPAGATION DELAY TIME



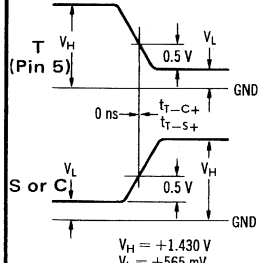
TEST WAVEFORMS FOR V_{out} TESTS

FIGURE 4



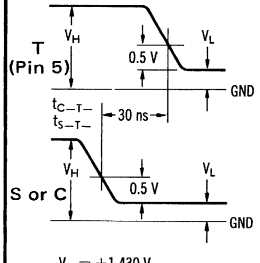
V_H = +1.430 V
V_L = +565 mW
1.0 ns < t_f < 10 ns

FIGURE 5



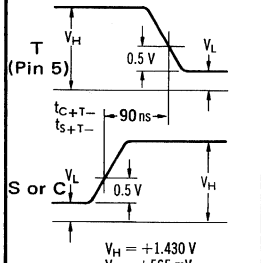
V_H = +1.430 V
V_L = +565 mW
1.0 ns < t_f < 10 ns
1.0 ns < t_r < 10 ns

FIGURE 6



V_H = +1.430 V
V_L = +565 mW
1.0 ns < t_f < 10 ns

FIGURE 7

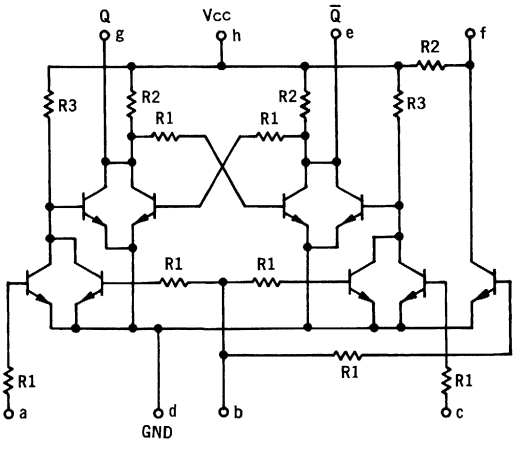


V_H = +1.430 V
V_L = +565 mW
1.0 ns < t_f < 10 ns
1.0 ns < t_r < 10 ns

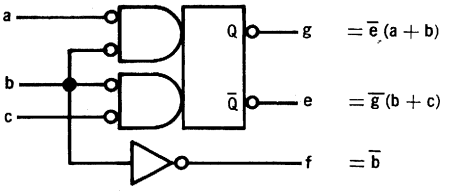
MC905 • MC805

Available in TO-99 metal can, add "G" suffix.
Available in TO-91 flat package, add "F" suffix.

This half-shift register is a bistable storage element with a built-in inverter for the gating signal. Information coming in on pins a and c will be transferred to pins g and e when the gating signal, pin b, goes low. If all three inputs, a, b, and c, are low, the outputs, g and e, will both be low.



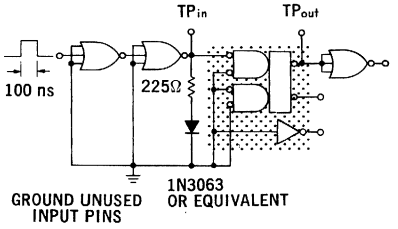
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

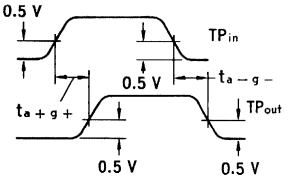


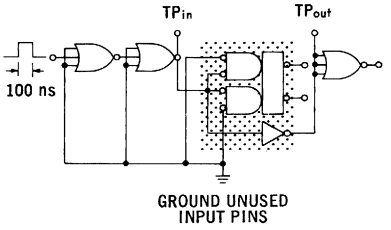
PIN CONNECTIONS

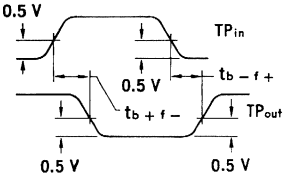
SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS









ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC905	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC805	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

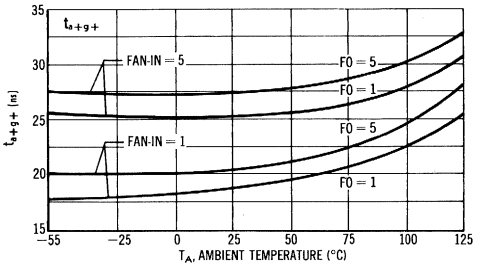
Characteristic	Symbol	Pin Under Test	MC905 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC805 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	a	-	b	-	h	d
	$3\ I_{in}$	b	-	1480	-	1300	-	1410	↓	-	1510	-	1350	-	1350	↓	b	-	a, c	-	↓	↓
	I_{in}	c	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	c	-	b	-	↓	↓
Output Current	I_{A4}	e	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	b, e	-	-	h	d, g †
	I_{A4}	e	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	c, e	-	-	↓	d
	I_{A5}	f	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	f	-	b	↓	d
	I_{A4}	g	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	b, g	-	-	↓	d, e †
	I_{A4}	g	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	a, g	-	-	↓	d
Output Voltage	V_{out}	e	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	g	b, c	-	h	d
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	↓
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	e	a, b	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a, b, c	-	h	d, e †
		e	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	b, c	↓	d, g
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	b	-	↓	d
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	a, b, c	-	↓	d, g †
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	a, b	↓	d, e
																	Pulse In	Pulse Out				
Switching Time	t	a+g+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	a	g	-	-	h	d, e
		a-g-	-	-	-	40	-	-	↓	-	-	-	40	-	-	↓	a	g	-	-	↓	d, e
		b+f-	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	b	f	-	-	↓	d
		b-f+	-	-	-	24	-	-	↓	-	-	-	24	-	-	↓	b	f	-	-	↓	d

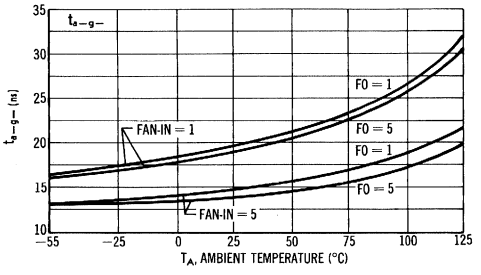
† Silicon Diode to Ground

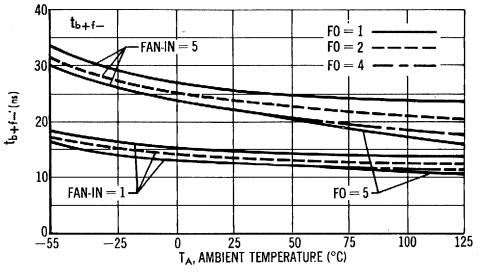
Pins not listed are left open.

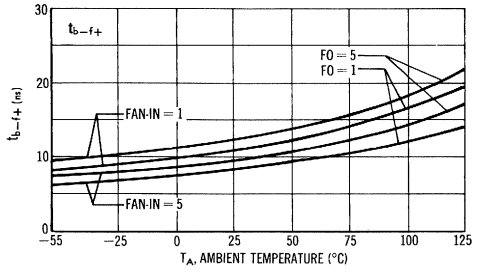
TYPICAL CURVES

SWITCHING CHARACTERISTICS

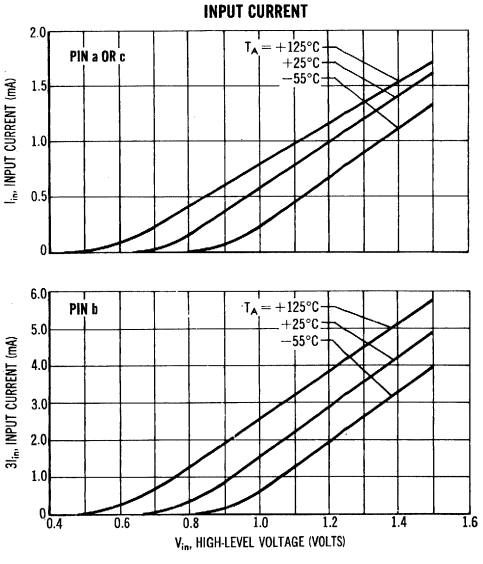




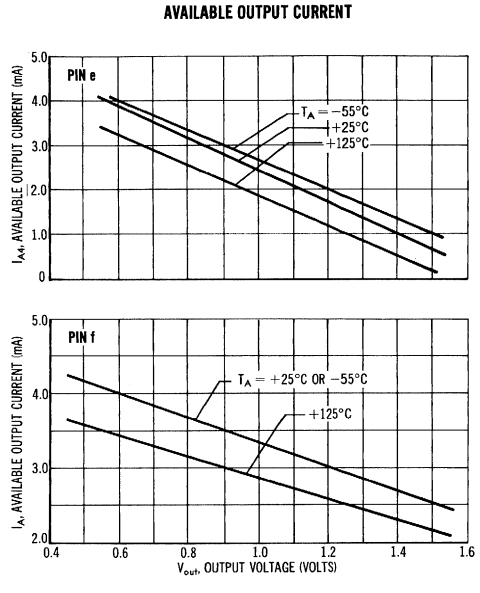




INPUT CURRENT



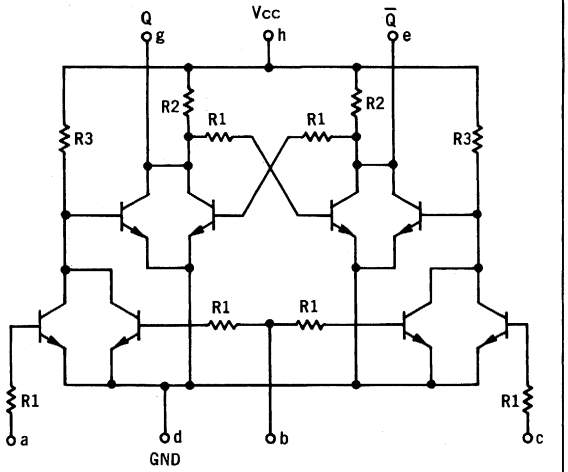
AVAILABLE OUTPUT CURRENT



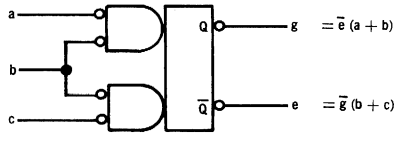
MC906 • MC806

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

This half-shift register is a bistable storage element. Information coming in on pins a and c will be transferred to pins g and e when the gating signal, pin b, goes low. If all three inputs, a, b, and c, are low, the outputs, g and e, will both be low.



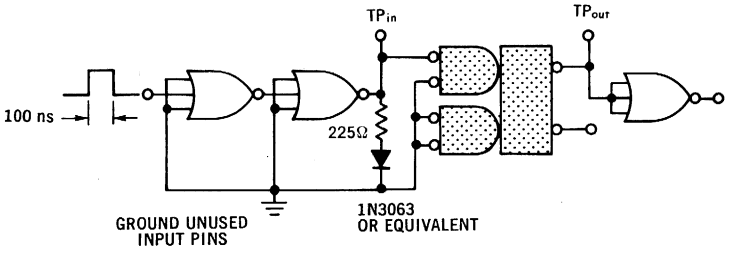
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

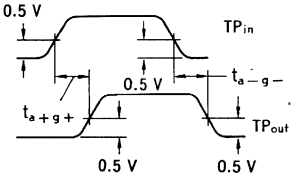


PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	—	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC906	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC806	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC906 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC806 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b	-	h	d
	$2\,I_{in}$	b	-	990	-	870	-	940	↓	-	1010	-	900	-	900	↓	b	-	a, c	-	↓	↓
	I_{in}	c	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	c	-	b	-	↓	↓
Output Current	I_{A4}	e	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	b, e	-	-	h	d, g †
		e	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	c, e	-	-	↓	d
		g	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	b, g	-	-	↓	d, e †
		g	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	a, g	-	-	↓	d
Output Voltage	V_{out}	e	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	g	b, c	-	h	d
		g		710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	e	a, b	-	h	d
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a, b, c	-	h	d, e †
		e	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	b, c	↓	d, g
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	a, b, c	-	↓	d, g †
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	a, b	↓	d, e
																	Pulse In	Pulse Out				
Switching Time	t	a+g+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	a	g	-	-	h	d, e
		a−g−	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	a	g	-	-	h	d, e

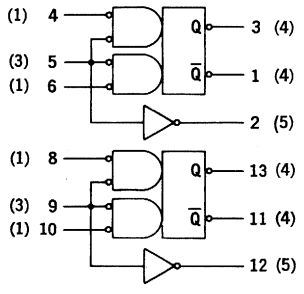
† Silicon Diode to Ground

Pins not listed are left open.

MC983 • MC883

Available in TO-86 flat package, add "F" suffix.

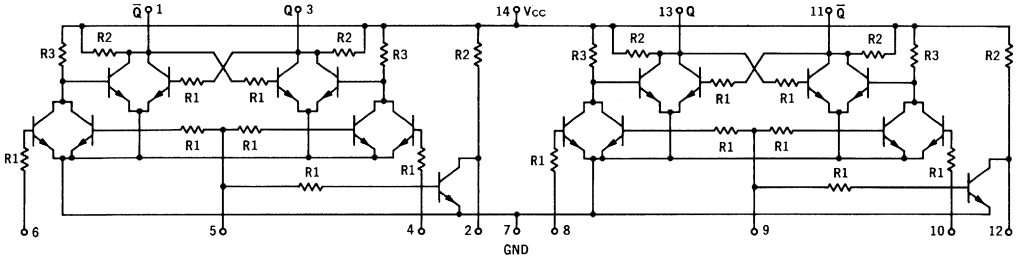
Two half-shift registers in a single package, each having a built-in inverter for the gating signal. For example, information coming in on pins 4 and 6 will be transferred to pins 3 and 1 when the gating signal, pin 5, goes low. If all three inputs, 4, 5, and 6, are low, the outputs, 1 and 3, will both be low.



$1 = \overline{3}\,(6 + 5)$
$3 = \overline{1}\,(5 + 4)$
$2 = \overline{5}$

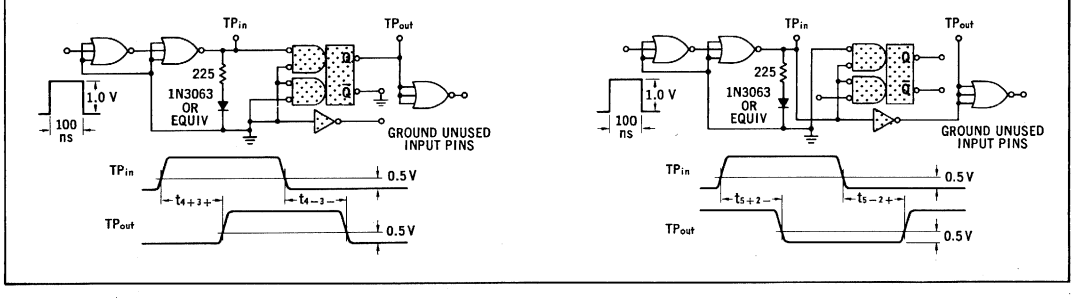
$t_{pd} = 22$ ns typ
$P_D = 110$ mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-shift register only.
The other half-shift register is tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC983 −55°C	1.014	1.014	1.50	0.710	3.00
MC983 +25°C	0.844	0.815	1.50	0.565	3.00
MC983 +125°C	0.674	0.674	1.50	0.320	3.00
MC883 0°C	0.909	0.909	1.50	0.574	3.00
MC883 +25°C	0.844	0.844	1.50	0.554	3.00
MC883 +100°C	0.710	0.710	1.50	0.370	3.00

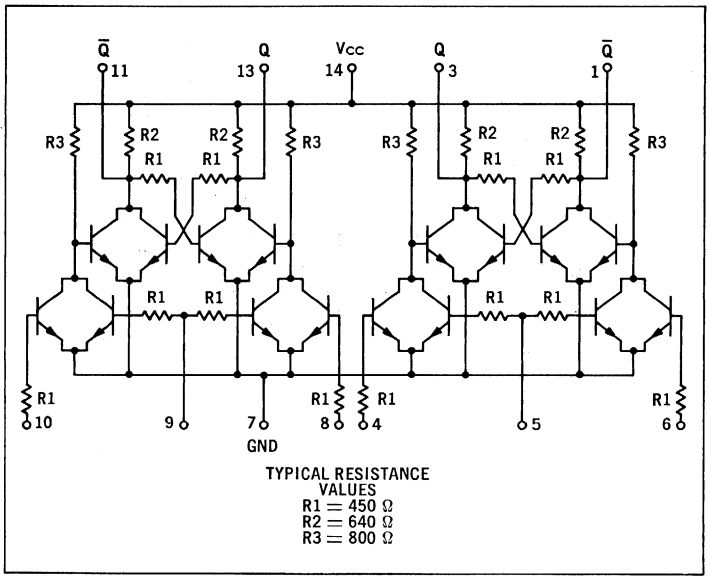
Characteristic	Symbol	Pin Under Test	MC983 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC883 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	4	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	4	-	5	-	14	7
	$3I_{in}$	5	-	1485	-	1305	-	1410	↓	-	1512	-	1350	-	1350	↓	5	-	4,6	-	↓	↓
	I_{in}	6	-	495	-	435	-	470		-	504	-	450	-	450		6	-	5	-		
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1,5	-	-	14	3*,7
	I_{A4}	1	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	1,6	-	-	↓	7
	I_{A5}	2	2.47	-	2.54	-	2.35	-		2.52	-	2.38	-	2.25	-		-	2	-	5		7
	I_{A4}	3	1.98	-	2.19	-	1.88	-		2.02	-	2.05	-	1.80	-		-	3,5	-	-		1*,7
	I_{A4}	3	1.98	-	2.19	-	1.88	-		2.02	-	2.05	-	1.80	-		-	3,4	-	-		7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	5,6	-	14	7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	-	-	↓	↓
		3	-		-		-			-		-		-			-	1	4,5	-		
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	4,5,6	-	14	1*,7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	5,6	↓	2,7
		2	-		-		-			-		-		-			-	-	5	-		7
		3	-		-		-			-		-		-			-	-	4,5,6	-		3*,7
		3	-		-		-			-		-		-			-	-	-	5,6		1,7
Switching Time	t	4+3+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In: 4	Pulse Out: 3	-	-	14	1,7
		4-3-	-	-	-	40	-	-	↓	-	-	-	40	-	-	↓	4	3	-	-	↓	1,7
		5+2-	-	-	-	28	-	-		-	-	-	28	-	-		5	2	-	-		7
		5-2+	-	-	-	24	-	-		-	-	-	24	-	-		5	2	-	-		7

Ground input pins of half-shift register not under test. Other pins not listed are left open. *Momentary ground.

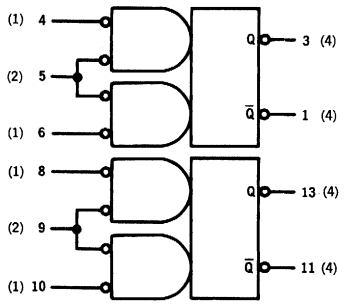
MC984 • MC884

Available in TO-86 flat package, add "F" suffix.

This bistable storage element consists of two half-shift registers in a single package. For example, information coming in on pins 4 and 6 will be transferred to pins 3 and 1 when the gating signal, pin 5, goes low. If all three inputs, 4, 5, and 6, are low, the outputs, 3 and 1, will both be low.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

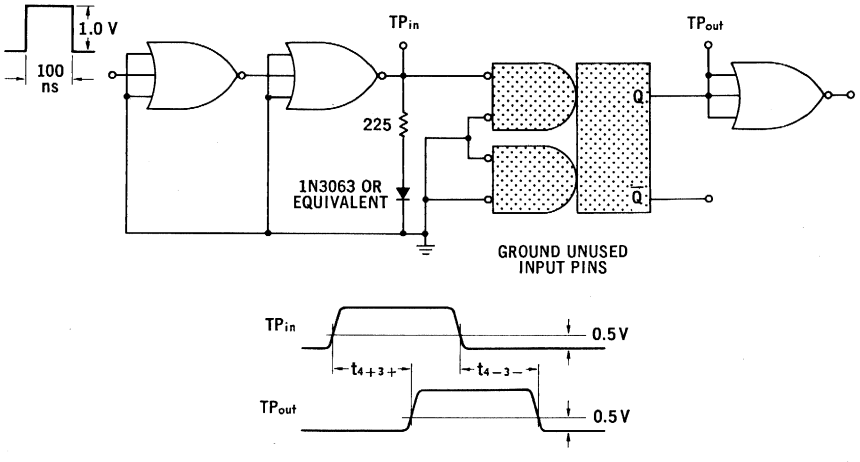


$3 = \overline{1}\,(4 + 5)$
$1 = \overline{3}\,(6 + 5)$

t_{pd} = 22 ns typ
P_D = 75 mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures shown are for one half-shift register only.
The other half-shift register is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC984	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC884	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

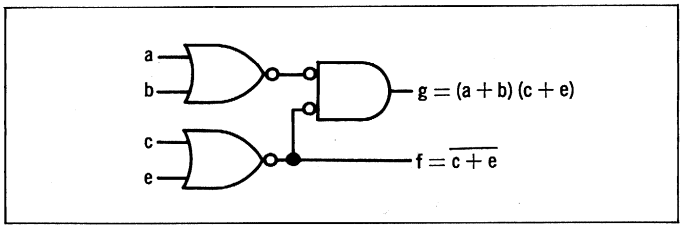
Characteristic	Symbol	Pin Under Test	MC984 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC884 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	4	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	4	-	5	-	14	7
	$2I_{in}$	5	-	990	-	870	-	940	↓	-	1008	-	900	-	900	↓	5	-	4, 6	-	↓	↓
	I_{in}	6	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	6	-	5	-	↓	↓
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1, 5	-	-	14	3*, 7
		1	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	1, 6	-	-	↓	7
		3	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3, 5	-	-	↓	1*, 7
		3	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3, 4	-	-	↓	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	5, 6	-	14	7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	4, 5	-	14	7
Saturation Voltage	V_{CE}	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	4, 5, 6	-	14	1*, 7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	5, 6	↓	3, 7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	4, 5, 6	↓	3*, 7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	4, 5	↓	1, 7
																	Pulse In	Pulse Out				
Switching Time	t	4+3+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	4	3	-	-	14	1, 7
		4-3-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	4	3	-	-	14	1, 7

Ground input pins of half-shift register not under test. Other pins not listed are left open. *Momentary ground.

MC904 • MC804

Available in TO-99 metal can, add "G" suffix.
Available in TO-91 flat package, add "F" suffix.

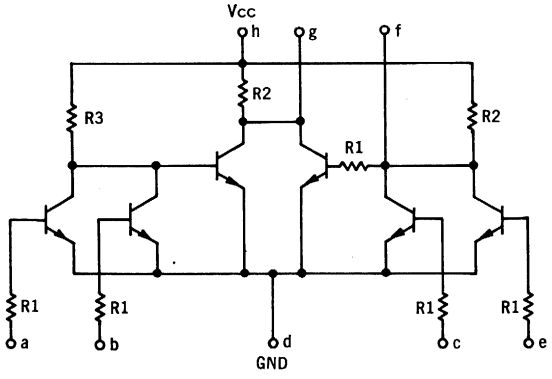
This half-adder device can be used to supply the SUM and CARRY operations on two input signals. If the inputs are applied to pins a and b, and their complements to pins c and e, the SUM of the inputs appears on pin g while the CARRY appears on pin f.



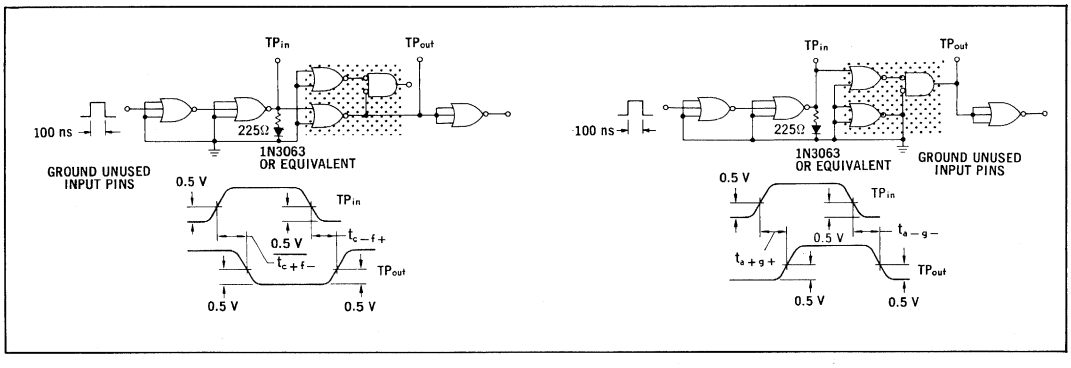
PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω



SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC904	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC804	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

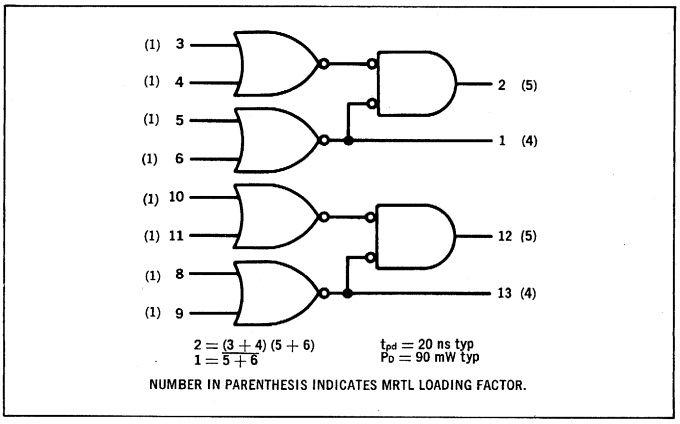
Characteristic	Symbol	Pin Under Test	MC904 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC804 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a	-	↓	↓
		c	-		--		-			-		-		-			c	-	e	-		
		e	-		-		-			-		-		-			e	-	c	-		
Output Current	I_{A4}	f	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	f	-	c, e	h	d
	I_{A5}	g	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	a, c, g	-	-	↓	↓
	I_{A5}	g	2.47	-	2.54	-	2.35	-		2.52	-	2.38	-	2.25	-		-	b, e, g	-	-		
Output Voltage	V_{out}	f	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	c	-	-	h	d
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	e	-	-	↓	↓
		g	-		-		-			-		-		-			-	f	a, b	-		
Saturation Voltage	$V_{CE(sat)}$	f	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	c	-	h	d
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	e	-	↓	↓
		g	-		-		-			-		-		-			-	-	a, b	c, e		
		g	-		-		-			-		-		-			-	-	c, e	a, b		
																	Pulse In	Pulse Out				
Switching Time	t	a+g+	-	-	-	36	-	-	ns	-	-	-	36	-	-	ns	a	g	-	-	h	d
		a-g-	-	-	-	36	-	-	↓	-	-	-	36	-	-	↓	a	g	-	-	↓	↓
		c+f-	-	-	-	20	-	-		-	-	-	20	-	-		c	f	-	-		
		c-f+	-	-	-	30	-	-		-	-	-	30	-	-		c	f	-	-		

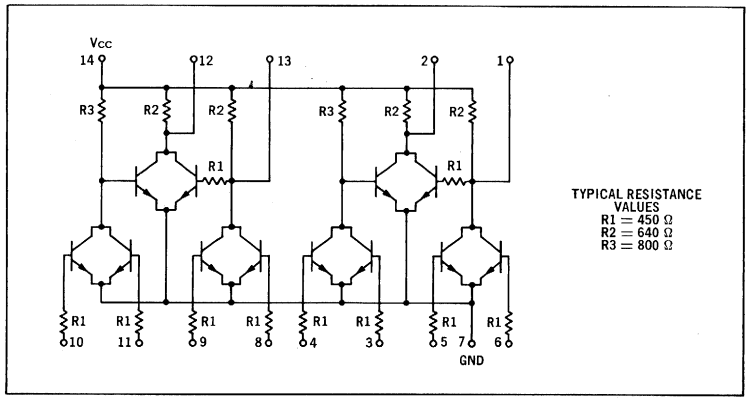
Pins not listed are left open.

MC975 • MC875

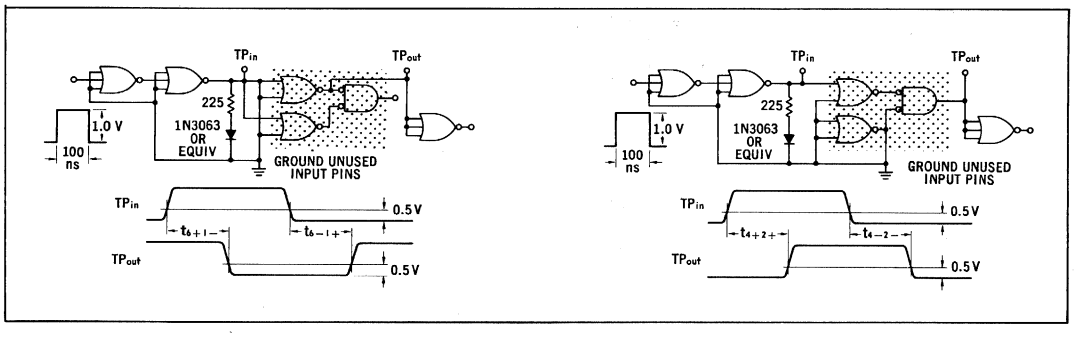
Available in TO-86 flat package, add "F" suffix.

A dual half-adder device contained in a single package. Each can be used to supply the SUM and CARRY operations on two input signals. For example, if the inputs are applied to pins 3 and 4, and their complements to pins 5 and 6, the SUM of the inputs appears on pin 2 while the CARRY appears on pin 1.





SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-adder only.
The other half-adder is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC975	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC875	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

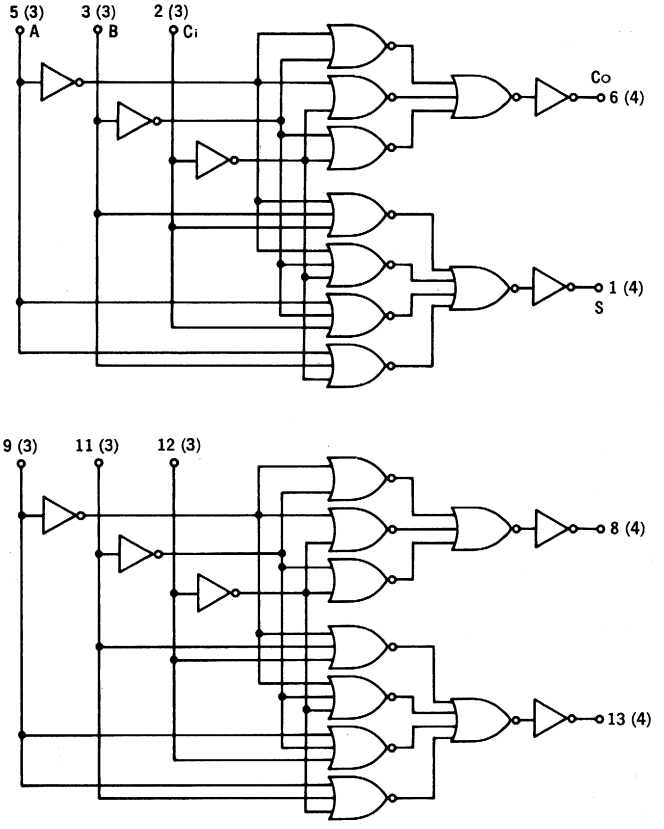
Characteristic	Symbol	Pin Under Test	MC975 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC875 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	3	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	3	-	4	-	14	7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	4	-	3	-	↓	↓
		5	-	-	-	-	-	-		-	-	-	-	-	-		5	-	6	-		
		6	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		6	-	5	-		
Output Current	IA4	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1	-	5, 6	14	7
	IA5	2	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	2, 3, 5	-	-	↓	↓
	IA5	2	2.47	-	2.54	-	2.35	-		2.52	-	2.38	-	2.25	-		-	2, 4, 6	-	-		
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	5	-	-	14	7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	6	-	-	↓	↓
		2	-	-	-	-	-	-		-	-	-	-	-	-		-	1	3, 4	-		
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	5	-	14	7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	6	-	↓	↓
		2	-	-	-	-	-	-		-	-	-	-	-	-		-	-	3, 4	5, 6		
		2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	5, 6	3, 4	↓	
																	Pulse In	Pulse Out				
Switching Time	t	6+1-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	6	1	-	-	14	7
		6-1+	-	-	-	30	-	-	↓	-	-	-	30	-	-	↓	6	1	-	-	↓	7
		4+2+	-	-	-	36	-	-		-	-	-	36	-	-		4	2	-	-		1, 7
		4-2-	-	-	-	36	-	-		-	-	-	36	-	-		4	2	-	-		1, 7

Ground input pins of half-adder not under test. Other pins not listed are left open.

MC996 • MC896

Available in TO-86 flat package, add "F" suffix.

Provides the SUM and CARRY functions while requiring only AUGEND (A) and ADDEND (B) inputs with CARRY IN.



TRUTH TABLE				
INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

POSITIVE LOGIC

$Co = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

$S = ABC_i + AB\overline{C_i} + A\overline{B}\overline{C_i} + \overline{A}\overline{B}C_i$

$t_{pd} = 60$ ns typ

$P_D = 70$ mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR

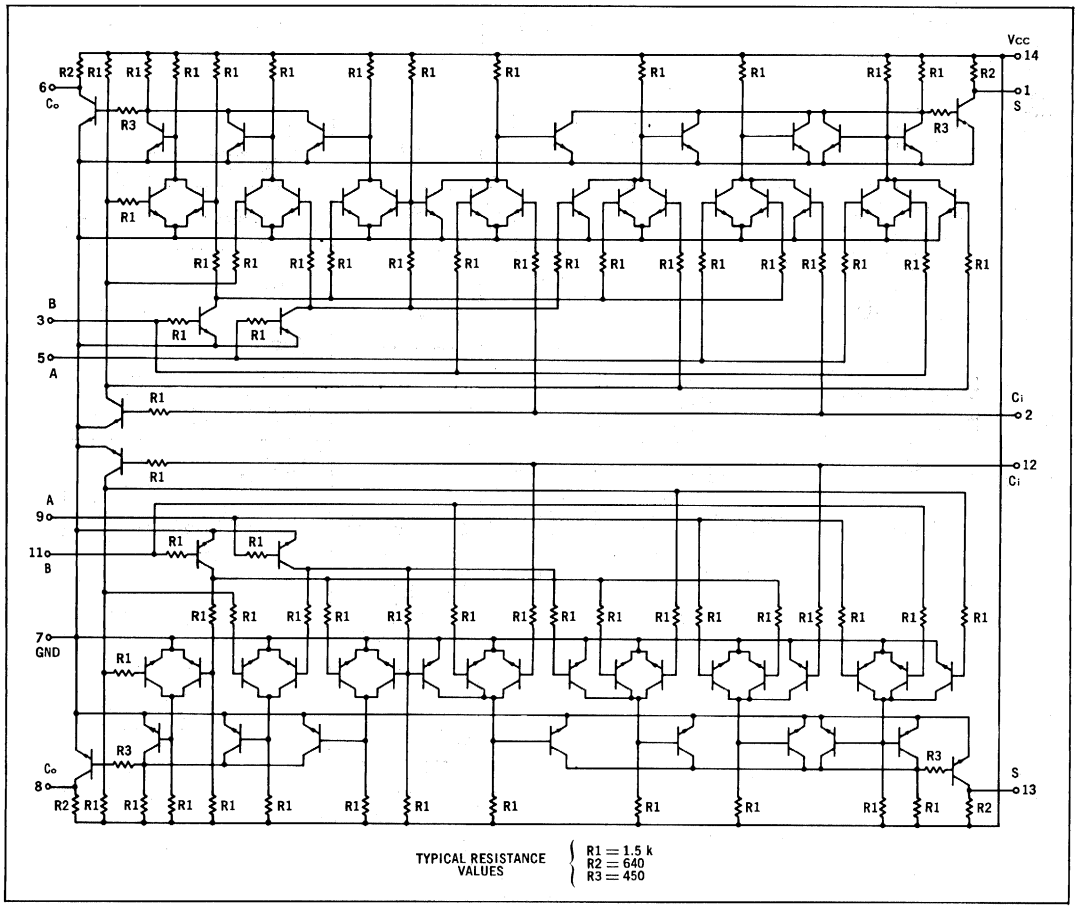
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one adder.
The other adder is tested in the same manner.

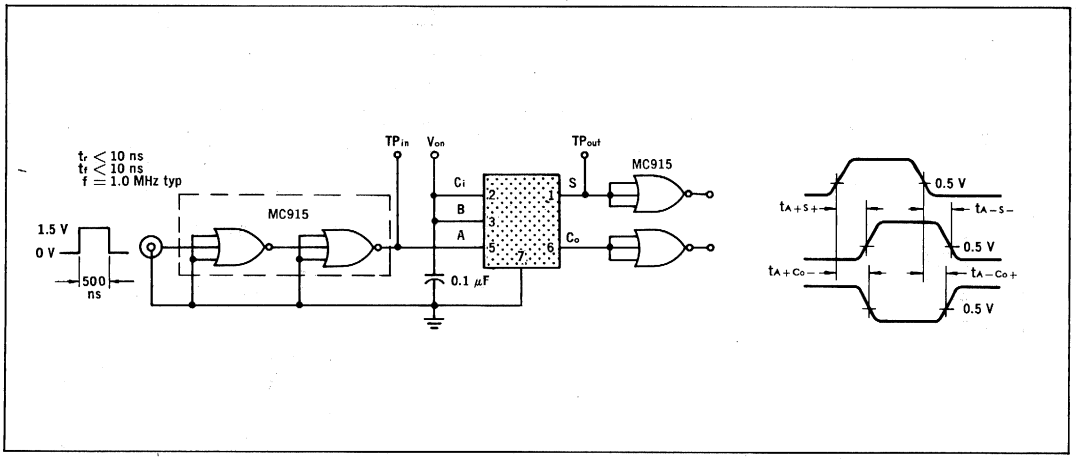
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC996	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC896	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC996 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC896 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$3I_{in}$	2	-	1485	-	1305	-	1410	μAdc	-	1512	-	1350	-	1350	μAdc	2	-	-	-	14	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	-	-	↓	↓
		5	-		-		-			-		-		-			5	-	-	-		
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1,2	-	3,5	14	7
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	1,3	-	2,5	↓	↓
				-		-		-			-		-		-		-	1,5	-	2,3		
				-		-		-			-		-		-		-	1,2,3,5	-	-		
		6		-		-		-			-		-		-		-	2,3,6	-	5		
		↓		-		-		-			-		-		-		-	2,5,6	-	3		
				-		-		-			-		-		-		-	3,5,6	-	2		
				-		-		-			-		-		-		-	2,3,5,6	-	-		
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	-	-	2,3,5	14	7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2,3	-	5	↓	↓
			-		-		-			-		-		-			-	3,5	-	2		
			-		-		-			-		-		-			-	2,5	-	3		
		6	-		-		-			-		-		-			-	-	-	2,3,5		
		↓	-		-		-			-		-		-			-	2	-	3,5		
			-		-		-			-		-		-			-	3	-	2,5		
			-		-		-			-		-		-			-	5	-	2,3		
																	Pulse In		Pulse Out			
Switching Time	t	5+1+	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	5	2,3	1	-	14	7
		5-1-	-	-	-	75	-	-		-	-	-	75	-	-		↓	2,3	1	-	↓	↓
		5+6+	-	-	-	85	-	-		-	-	-	85	-	-			2	6	3		
		5-6-	-	-	-	65	-	-		-	-	-	65	-	-			2	6	3		
		3+1+	-	-	-	75	-	-		-	-	-	75	-	-		3	-	1	2,5		
		3-1-	-	-	-	75	-	-		-	-	-	75	-	-		↓	-	1	2,5		
		3+6+	-	-	-	85	-	-		-	-	-	85	-	-			2	6	5		
		3-6-	-	-	-	65	-	-		-	-	-	65	-	-			2	6	↓		
		2+1-	-	-	-	70	-	-		-	-	-	70	-	-		2	3	1			
		2-1+	-	-	-	80	-	-		-	-	-	80	-	-		↓	↓	1			
		2+6+	-	-	-	70	-	-		-	-	-	70	-	-				6			
		2-6-	-	-	-	80	-	-	↓	-	-	-	80	-	-	↓			6	↓		

Ground input pins of adder not under test.
Other pins not listed are left open.



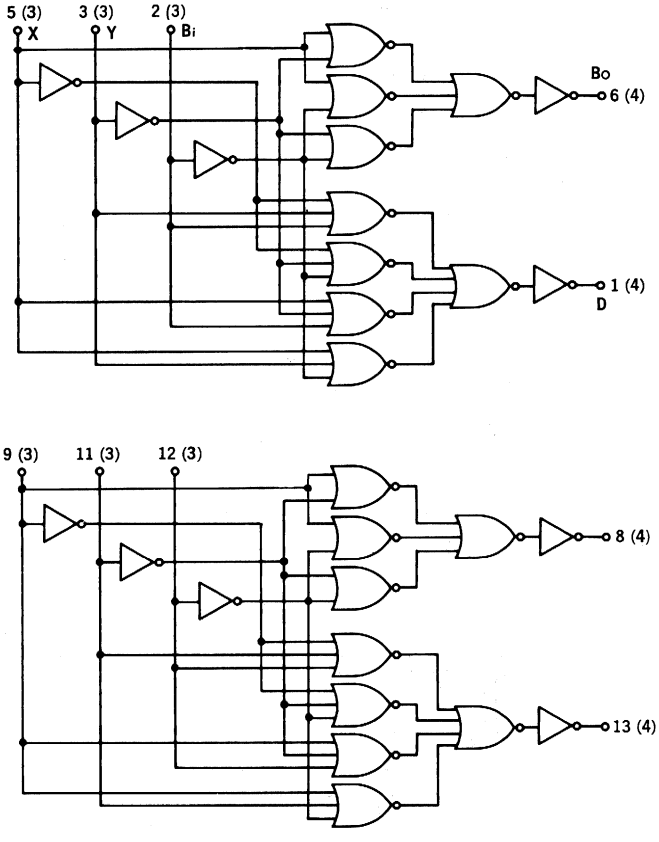
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



MC997 • MC897

Available in TO-86 flat package, add "F" suffix.

Provides the DIFFERENCE and BORROW functions while requiring only MINUEND (X) and SUBTRAHEND (Y) inputs with BORROW IN.



TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

POSITIVE LOGIC

$D = Y\bar{X}B_i + Y\bar{X}\bar{B}_i + \bar{Y}X\bar{B}_i + \bar{Y}\bar{X}B_i$

$B_o = \bar{Y}\bar{X}B_i + Y\bar{X}\bar{B}_i + \bar{Y}XB_i + YXB_i$

$t_{pd} = 60$ ns typ

$P_D = 70$ mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR

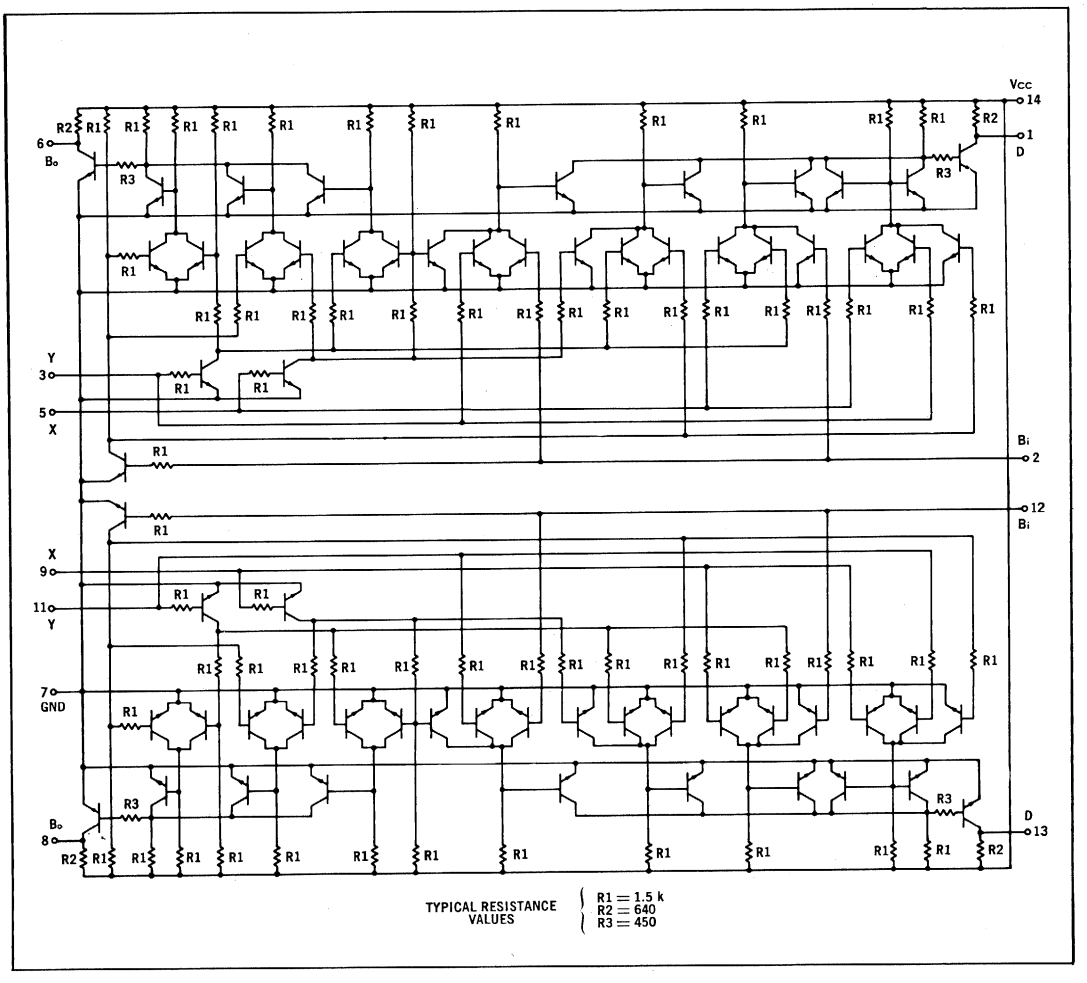
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one subtractor.
The other subtractor is tested in the same manner.

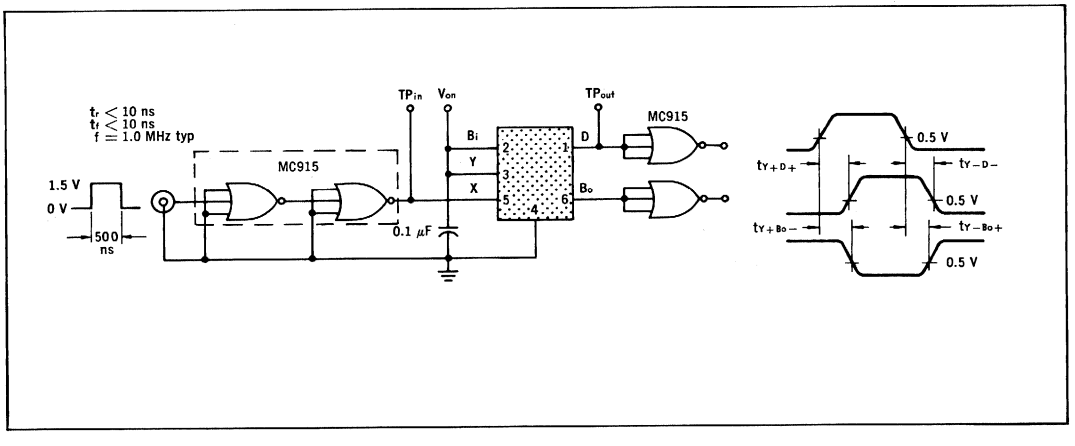
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC997	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC897	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC997 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC897 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$3\ I_{in}$	2	-	1485	-	1305	-	1410	μAdc	-	1512	-	1350	-	1350	μAdc	2	-	-	-	14	7
		3	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	3	-	-	-		
		5	-		-		-			-		-		-			5	-	-	-	↓	↓
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1,2	-	3,5	14	7
		↓		-		-		-			-		-		-		-	1,3	-	2,5		
				-		-		-			-		-		-		-	1,5	-	2,3		
				-		-		-			-		-		-		-	1,2,3,5	-	-		
		6		-		-		-			-		-		-		-	2,3,5,6	-	-		
		↓		-		-		-			-		-		-		-	2,6	-	3,5		
				-		-		-			-		-		-		-	3,6	-	2,5		
				-		-		-			-		-		-		-	2,3,6	-	5	↓	↓
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	-	-	2,3,5	7	14
		↓	-		-		-			-		-		-			-	2,3	-	5		
			-		-		-			-		-		-			-	3,5	-	2		
			-		-		-			-		-		-			-	2,5	-	3		
		6	-		-		-			-		-		-			-	2,5	-	3		
		↓	-		-		-			-		-		-			-	3,5	-	2		
			-		-		-			-		-		-			-	-	-	2,3,5		
			-		-		-			-		-		-			-	5	-	2,3	↓	↓
Switching Time																	Pulse In		Pulse Out			
	t	5+1+	-	-	-	60	-	-	ns	-	-	-	60	-	-	ns	5	2,3	1	-	14	7
		5-1-	-	-	-	60	-	-		-	-	-	60	-	-		↓	↓	1	-		
		5+6+	-	-	-	65	-	-		-	-	-	65	-	-				6	-		
		5-6-	-	-	-	60	-	-		-	-	-	60	-	-				6	-		
		3+1+	-	-	-	↓	-	-		-	-	-	↓	-	-		3	-	1	2,5		
		3-1-	-	-	-		-	-		-	-	-		-	-			-	1	2,5		
		3+6-	-	-	-	65	-	-		-	-	-	65	-	-			2	6	5		
		3-6+	-	-	-	60	-	-		-	-	-	60	-	-			2	6			
		2+1-	-	-	-		-	-		-	-	-		-	-		2	3	1	↓		
		2-1+	-	-	-		-	-		-	-	-		-	-			3	1			
		2+6+	-	-	-		-	-		-	-	-		-	-			3,5	6	-		
		2-6-	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	↓	3,5	6	-	↓	↓

Ground input pins of subtractor not under test.
Other pins not listed are left open.



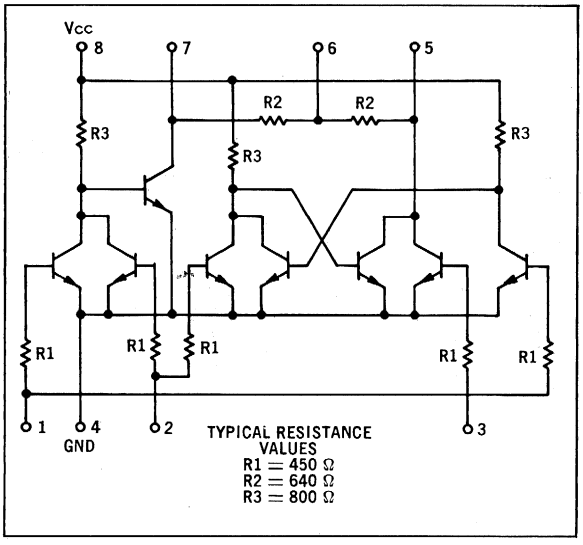
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

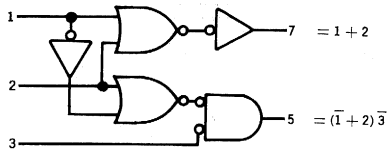


MC901 • MC801

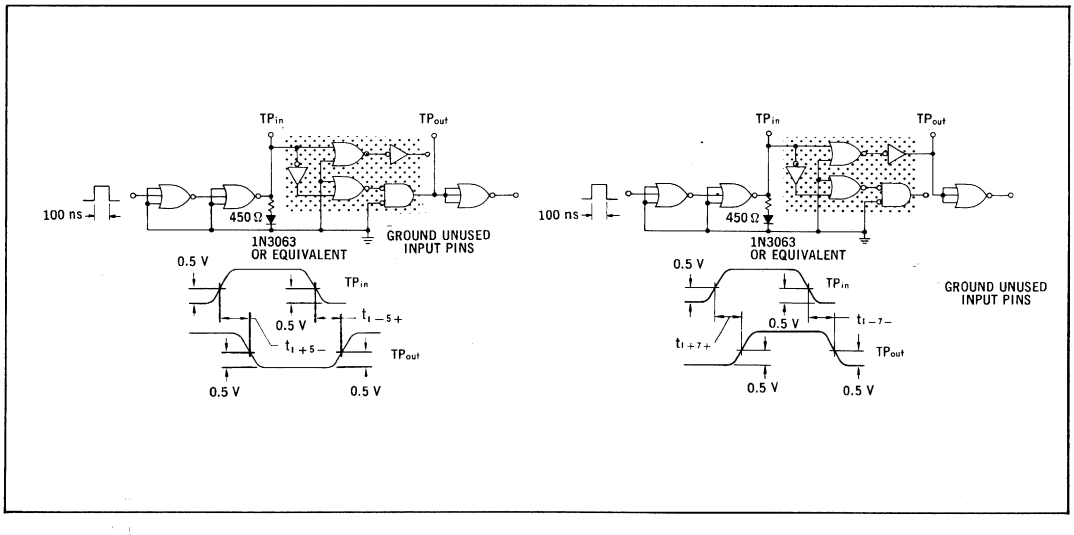
Available in TO-99 metal can, add "G" suffix.

This device provides the true output at pin 7 and the complement output at pin 5 for an input applied to pin 1. A positive gating signal may be applied to pin 2 to inhibit both outputs. A positive signal applied to pin 3 will hold output pin 5 at near-ground potential. The output nodes are returned separately to the power supply so that the outputs might be paralleled with other circuits.





SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC901	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC801	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

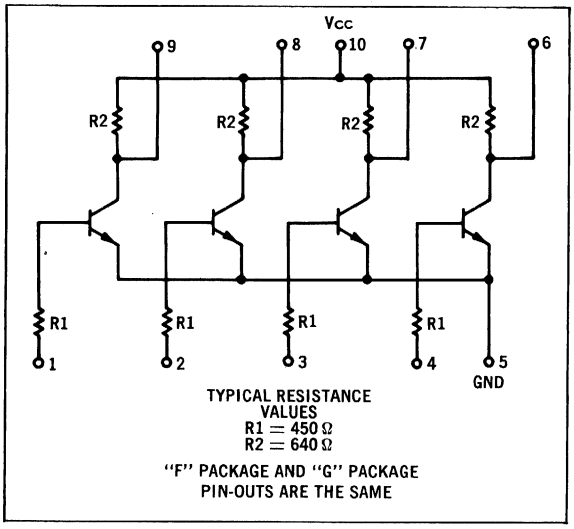
Characteristic	Symbol	Pin Under Test	MC901 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC801 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2\ I_{in}$	1	-	990	-	870	-	940	µAdc	-	1010	-	900	-	900	µAdc	1	-	2	-	6,8	4
	$2\ I_{in}$	2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1	-	↓	↓
	$2\ I_{in}$	2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	-	-	↓	↓
	I_{in}	3	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	3	-	1	-	↓	↓
Output Current	I_{A5}	5	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	5	-	1,3	6,8	4
		5	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	2,5	1	3	↓	↓
		7	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	1,7	-	-	↓	↓
		7	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	2,7	-	-	↓	↓
Output Voltage	V_{out}	5	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	2	-	6,8	4
Saturation Voltage	$V_{CE(sat)}$	5	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	1	-	2	6,8	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2,3	-	↓	↓
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1,2	↓	↓
																	Pulse In	Pulse Out				
Switching Time	t	1+5-	-	-	-	42	-	-	ns	-	-	-	42	-	-	ns	1	5	-	-	6,8	4
		1-5+	-	-	-	42	-	-	↓	-	-	-	42	-	-	↓	↓	5	-	-	↓	↓
		1+7+	-	-	-	38	-	-	↓	-	-	-	38	-	-	↓	↓	7	-	-	↓	↓
		1-7-	-	-	-	36	-	-	↓	-	-	-	36	-	-	↓	↓	7	-	-	↓	↓

Pins not listed are left open.

MC927 • MC827

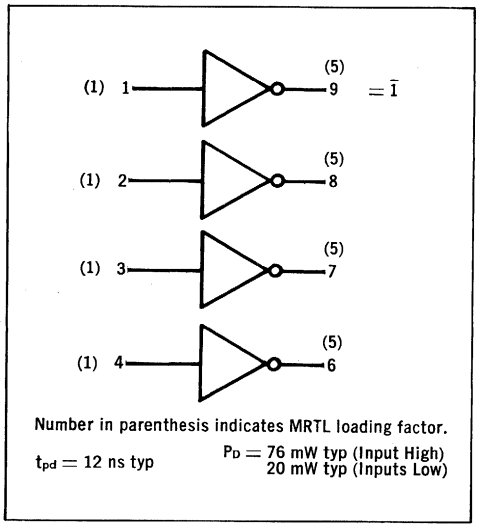
Available in TO-100 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Four individual circuits each perform the simple inversion function.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

"F" PACKAGE AND "G" PACKAGE PIN-OUTS ARE THE SAME

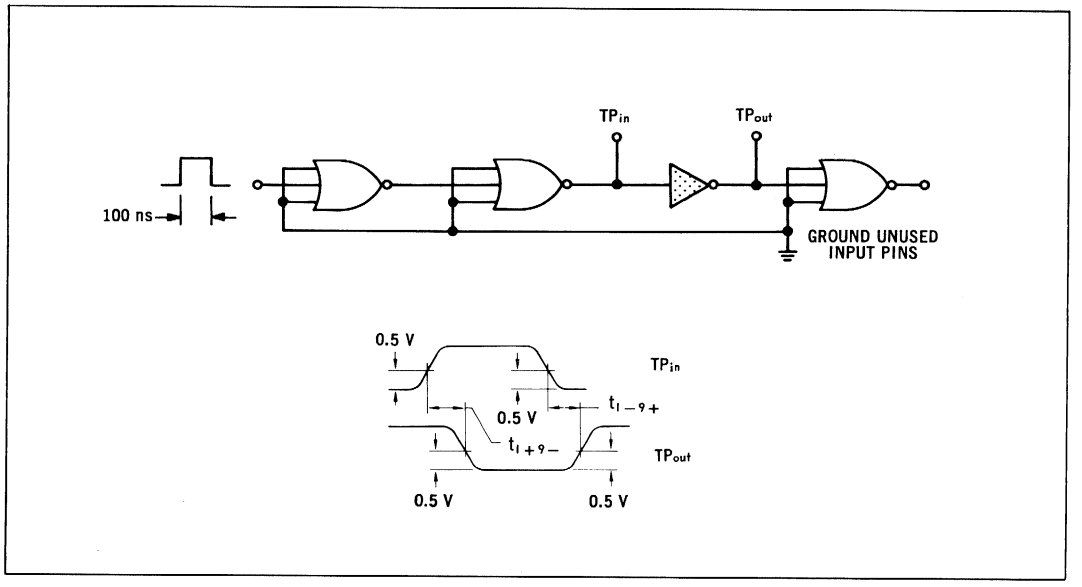


Number in parenthesis indicates MRTL loading factor.

t_{pd} = 12 ns typ

P_D = 76 mW typ (Input High)
20 mW typ (Inputs Low)

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.
Other inverters are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC927	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC827	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC927 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC827 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	1*	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	*	-	10	5
Output Current	I_{A5}	6	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	6	-	4	10	5
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	6	-	-	4	-	5
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	4	1, 2, 3	-	10	5
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1, 2, 3, 4	-	10	5
																	Pulse In	Pulse Out				
Switching Time	t	1+9- 1-9+	- -	- -	- -	20 28	- -	- -	ns ns	- -	- -	- -	20 28	- -	- -	ns ns	1 1	9 9	-	-	10 10	5 5

* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V_{BOT}.

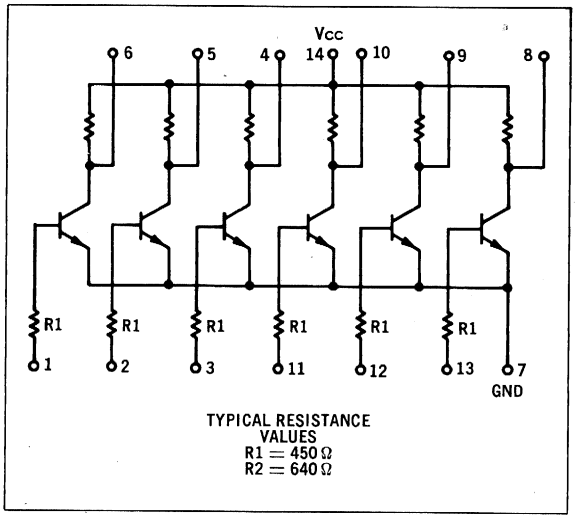
Ground inputs of inverters not used in test.

Other pins not listed are left open.

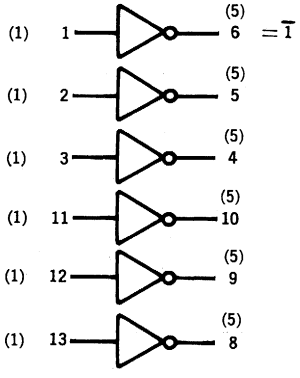
MC989 • MC889

Available in TO-86 flat package, add "F" suffix.

Six individual circuits are contained in a package. Each provides the simple inversion function.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

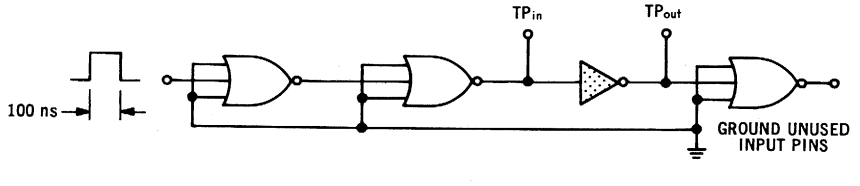


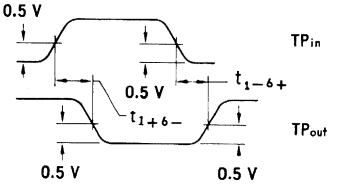
Number in parenthesis indicates MRTL loading factor.

t_{pd} = 12 ns typ

P_D = 76 mW typ (Input High)
20 mW typ (Inputs Low)

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.
Other inverters are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC989	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC889	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test.	MC989 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC889 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1*	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	1	-	-	-	14	7
Output Current	I_{A5}	6	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	6	-	1	14	7
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	6	-	-	1	-	7
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	7
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	7
																	Pulse In	Pulse Out				
Switching Time	t	1+6-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	1	6	-	-	14	7
		1-6+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	1	6	-	-	14	7

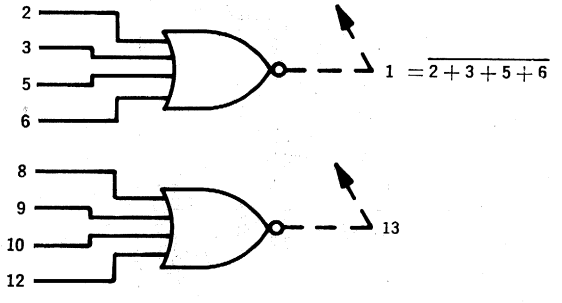
Ground inputs of inverters not used in test. Other pins not listed are left open.

* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V_{BOT}.

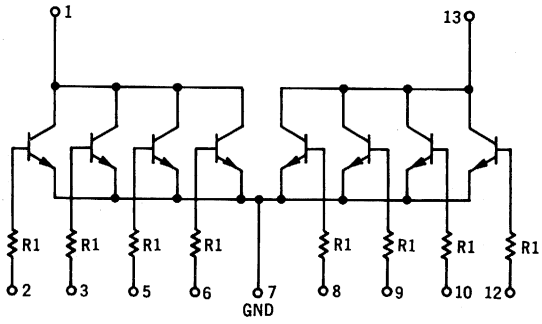
MC986 • MC886

Available in TO-86 flat package, add "F" suffix.

Two 4-input gate expanders housed in a single package may be used independently or combined. Each of these expanders increases the input capability of a standard MRTL gate by four.



When an expander is added to a gate, subtract 0.4 load unit from the output of the gate for each expander circuit added.



V_{CC} connection to pin 14 not shown.

TYPICAL RESISTANCE VALUE
R1 = 450Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expander is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC986	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC886	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC986 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC886 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	2	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	2	-	3, 5, 6	-	14	1	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2, 5, 6	-	↓	↓	↓
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	5	-	2, 3, 6	-	↓	↓	↓
		6	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6	-	2, 3, 5	-	↓	↓	↓
Output Leakage Current	I_{CEX}	1	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	1	-	-	2, 3, 5, 6	14	-	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	1	3, 5, 6, 7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓	2, 5, 6, 7
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	-	-	↓	↓	2, 3, 6, 7
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	6	-	-	↓	↓	2, 3, 5, 7
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	1	3, 5, 6, 7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	↓	2, 5, 6, 7
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	5	-	↓	↓	2, 3, 6, 7
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	6	-	↓	↓	2, 3, 5, 7

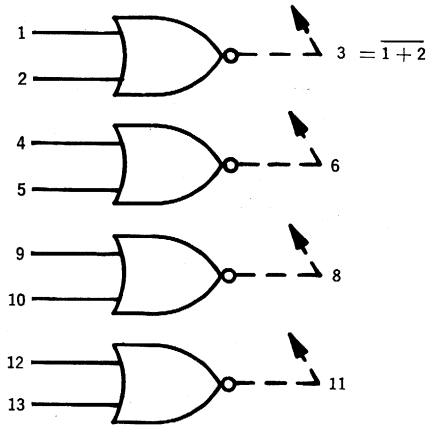
Ground inputs of expander not under test. Other pins not listed are left open.

* Resistor Value to V_{CC}.

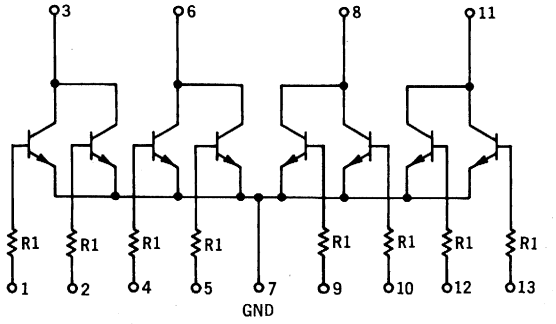
MC985 • MC885

Available in TO-86 flat package, add "F" suffix.

Four 2-input expanders housed in a single package increase the input capability of MRTL gates.



When an expander is added to a gate, subtract 0.4 load unit from the output of the gate for each expander circuit added.



V_{CC} connection to pin 14 not shown.

TYPICAL RESISTANCE VALUE
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
Other expanders are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC985	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC885	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC985 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC885 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	2	-	14	3	7
		2	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	2	-	1	-	14	3	7
Output Leakage Current	I_{CEX}	3	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	3	-	-	1,2	14	-	7
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	3	2,7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	3	1,7
Saturation Voltage	$V_{CE(sat)}$	3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	3	2,7
		3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	3	1,7

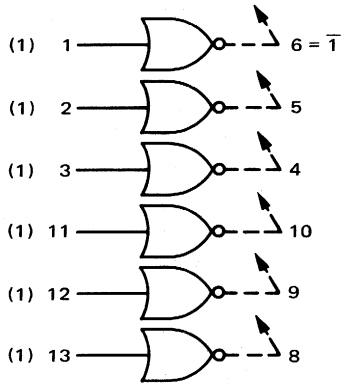
Ground inputs of expanders not under test. Other pins not listed are left open.

* Resistor Value to V_{CC}.

MC9919 • MC9819

Available in TO-86 flat package, add "F" suffix.

Six individual expanders are contained in a single package providing increased input capability for MRTL gates.

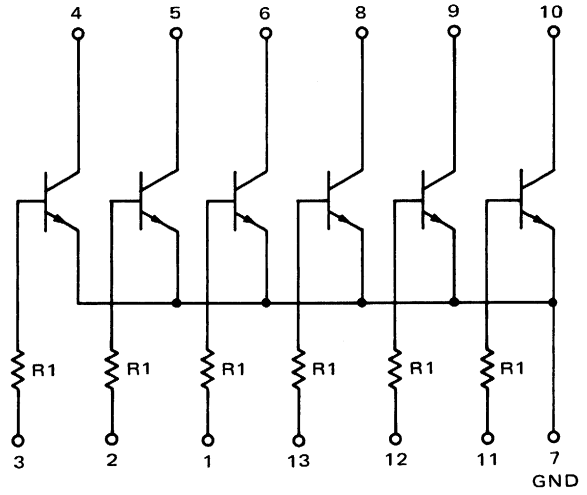


t_{pd} = 12 ns

P_D = 13 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.

When an expander is added to a gate, subtract 0.4 load from the output of the gate for each expander circuit added. The input loading factor of the expanded gate is 1.3. Pin 14 of the expander must be connected to V_{CC}.



V_{CC} connection to pin 14 not shown.

Typical Resistance Values
R1 = 450Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC9919	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC9819	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC9919 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC9819 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	-	-	14	6	7
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	6	-	-	1	14	-	7
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	6	7
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	6	7

Ground inputs of expanders not used in test. Other pins not listed are left open.

* Resistor value to V_{CC}.

LOW-POWER
mW MRTL
INTEGRATED CIRCUITS
MC908/MC808 SERIES

LOW POWER

mW MRTL

INTEGRATED CIRCUITS

Low-power mW MRTL circuits are designed for use where minimal system power consumption is desired. Typical gate speed is 27 ns, with typical power dissipation of 6.5 mW (input high), and 0.5 mW (inputs low) per logic node.

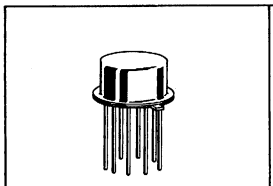
INDEX

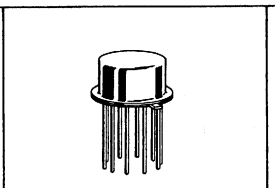
NUMERICAL INDEX
(Functions and Characteristics)

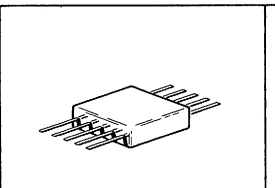
V_{CC} = 3.0 V ±10% for MC908 Series, 3.6 V ±10% for MC808 Series; T_A = 25°C

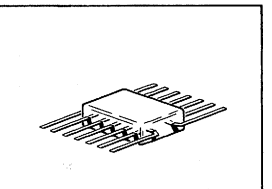
Function	Type ①		Case	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation ② mW typ/pkg		Page No.
	0 to +75°C	−55 to +125°C				MC808 Series	MC908 Series	
Half Adder	MC808	MC908	72,96	4	60	19/12.5	14/8.5	6-141
2-Input Buffer	MC809	MC909	72,96	30	57	7.0/23	5.5/16	6-115
Dual 2-Input NOR Gate	MC810	MC910	72,96	4	27	10/2.5	8.0/1.0	6-104
Dual 4-Input OR/NOR Gate	MC811	MC911	72,96	4	60	8.0/5.5	6.0/3.5	6-100
Half Adder	MC812	MC912	72,96	4	66	15.5/10.5	11.5/5.5	6-143
Type D Flip-Flop	MC813	MC913	72,96	3	75	24/17.5 ③	17.5/13 ③	6-122
Quad 2-Input NOR Gate	MC817	MC917	83	4	27	20/5.0	16/2.5	6-113
Dual 3-Input NOR Gate	MC818	MC918	72,96A	4	27	12/2.5	9.5/1.0	6-107
Dual 4-Input NOR Gate	MC819	MC919	83	4	27	13/2.5	11/1.0	6-109
J-K Flip-Flop	MC820	MC920	72,96	2	50	20.5/14.5 ④	15.5/10 ④	6-126
Dual 2-Input Gate Expander	MC821	MC921	72,96	–	27	3.0/ –	3.0/ –	6-146
J-K Flip-Flop	MC822	MC922	72,96A	4	70	24/20 ④	17.5/13 ④	6-129
5-Input NOR Gate	MC828	MC928	72,96	4	27	7.5/1.0	6.5/0.5	6-102
Dual J-K Flip-Flop	MC876	MC976	83	2	50	41/29 ④	31/20 ④	6-138
Dual Type D Flip-Flop	MC878	MC978	83	3	60	48/35 ③	35/26 ③	6-135
Dual Buffer	MC881	MC981	96	30	57	14/46	11/32	6-118
J-K Flip-Flop	MC882	MC982	96	2	80	23/21 ④	15/13 ④	6-132
Triple 3-Input NOR Gate	MC893	MC993	83	4	27	18/3.5	14/2.0	6-111
Dual 2-Input Buffer	MC898	MC998	83	30	57	14/46	11/32	6-120
Quad 2-Input Expander	MC9821	MC9921	83	–	27	20/ –	20/ –	6-148

① G suffix denotes Metal Can, F suffix denotes Flat Package; i.e., MC818G = Metal Can, MC818F = Flat Package.
② Input High/Inputs Low unless otherwise noted.
③ Direct Set and Direct Clear Low, All Other Inputs High/All Inputs Low
④ Only Clock Input High/All Inputs Low


TO-99


TO-100


TO-91


TO-86

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	–	+4.0	Vdc
Power Supply Voltage (Pulsed ≤ 1.0 s)	–	+12	Vdc
Operating Temperature Range MC908 Series MC808 Series	T_A	−55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TEST CONDITION TOLERANCES

V_{BOT} = ±10 mV V_{CC} = ±10 mV V_{in} = ±2 mV V_{on} = ±2 mV V_{off} = ±2 mV

DEFINITIONS

I_{A2}, I_{A3}, I_{A4} — Minimum available output current from a device with an output loading of 2, 3, or 4.

I_{AB} — Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.

I_{AM} — The maximum available current from the output of a Dual Gate.

I_{CEX} — Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

$0.8\ I_{in}$ — The current drawn from the V_{in} supply by an inverter transistor for a fan-in of 1.

I_{in} — Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

$1.8\ I_{in}$ — Current drawn from the V_{in} supply by the Toggle pin of the Flip-Flop.

$2\ I_{in}$ — Maximum input current drawn by one input of a device with 2 bases internally tied together.

I_L — Isolation leakage current.

V_{BOT} — A high-value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} — Supply voltage.

$V_{CE(sat)}$ — Maximum saturation voltage with V_{BOT} applied into the input.

V_{in} — Minimum high-level voltage applied to the input of a device.

V_{LL} — A supply voltage low enough to allow flow of leakage currents only.

V_{off} — The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} — The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} — The maximum output voltage with V_{on} applied to the input.

V_R — Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

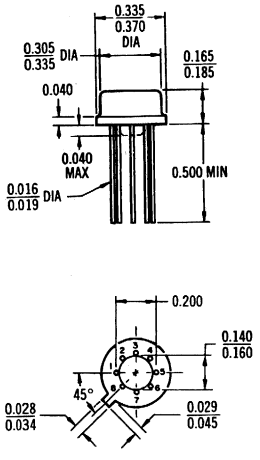
Release Time — The time that the J or K input data must be held after the negative-going clock input transition in order to propagate correct data.

Set-Up Time — The time that the J or K input data must be present prior to the negative-going clock input transition in order to propagate correct data.

GENERAL RULES

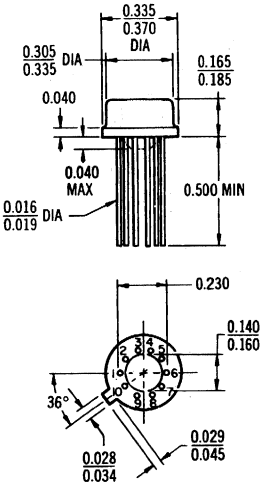
- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- A gate output connected in parallel with another output reduces the drive capability by ½ load. (Paralleling gate circuits requires a V_{CC} connection to only one of the gates.)
- Any number of gates may be paralleled if the input loading is increased by ¼ load.
- All unused inputs should be returned to ground.

OUTLINE DIMENSIONS



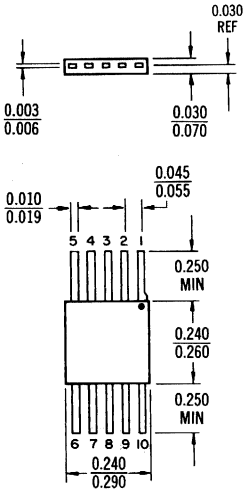
Pin 4 connected to case.

TO-99



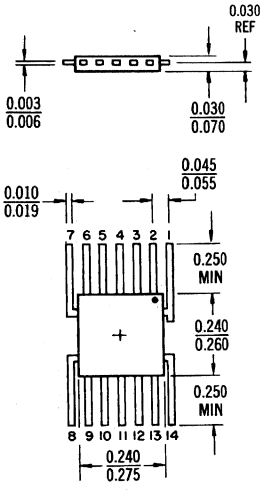
Pin 5 connected to case.

TO-100



Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

TO-91



Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

TO-86

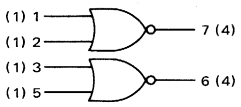
mW MRTL DEVICES AVAILABLE IN METAL CANS

The logic diagrams on these two pages describe the MC908 /MC808 MRTL integrated circuits available in metal cans, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of –55 to +125°C with V_{CC} = 3.0 V ±10% for the MC908 Series, and 0 to +75°C with V_{CC} = 3.6 V ±10% for the MC808 Series. For the TO-99 metal can, V_{CC} is applied to pin 8, with ground connected to pin 4. For the TO-100 metal can, V_{CC} is applied to pin 10, with ground connected to pin 5.

GATES

MC910G • MC810G
Dual 2-Input Gate

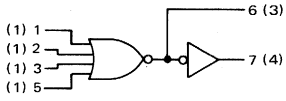


$7 = \overline{1 + 2}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC910G	MC810G
Input High	8.0	10
Inputs Low	1.0	2.5

MC911G • MC811G
4-Input Gate



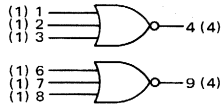
$6 = \overline{1 + 2 + 3 + 5}$

$7 = 1 + 2 + 3 + 5$

t_{pd} = 60 ns typical

Total Power Dissipation mW typ		
	MC911G	MC811G
Input High	6.0	8.0
Inputs Low	3.5	5.5

MC918G • MC818G
Dual 3-Input Gate

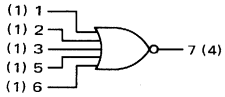


$4 = \overline{1 + 2 + 3}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC918G	MC818G
Input High	9.5	12
Inputs Low	1.0	2.5

MC928G • MC828G
5-Input Gate



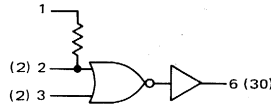
$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC928G	MC828G
Input High	6.5	7.5
Inputs Low	0.5	1.0

BUFFERS

MC909G • MC809G
Buffer

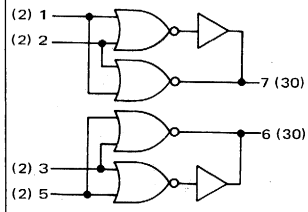


$6 = \overline{2 + 3}$

t_{pd} = 57 ns typical

Total Power Dissipation mW typ		
	MC909G	MC809G
Input High	5.5	7.0
Inputs Low	16	23

MC981G • MC881G
Dual Buffer



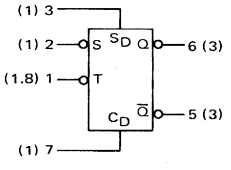
$7 = \overline{1 + 2}$

t_{pd} = 57 ns typical

Total Power Dissipation mW typ		
	MC981G	MC881G
Input High	11	14
Inputs Low	32	46

FLIP-FLOPS

MC913G • MC813G
Type D Flip-Flop



t_{pd} = 75 ns typical

Total Power Dissipation mW typ		
	MC913G	MC813G
Direct Set and Direct Clear Inputs Low, All other Inputs High	17.5	24
Inputs Low	13	17.5

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

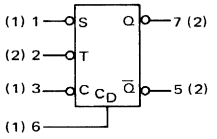
CLOCKED INPUT OPERATION ③

t_n		t_{n+1}	
S		Q	$\overline{Q}$
1		1	0
0		0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

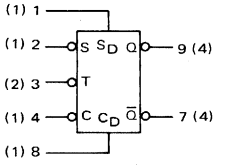
MC920G • MC820G
J-K Flip Flop



t_{pd} = 50 ns typical

Total Power Dissipation mW typ		
	MC920G	MC820G
Only Clock Input High	15.5	20.5
Inputs Low	10	14.5

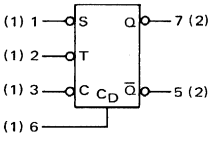
MC922G • MC822G
J-K Flip-Flop



t_{pd} = 70 ns typical

Total Power Dissipation mW typ		
	MC922G	MC822G
Only Clock Input High	17.5	24
Inputs Low	13	20

MC982G • MC882G
J-K Flip-Flop



t_{pd} = 80 ns typical

Total Power Dissipation mW typ		
	MC982G	MC882G
Only Clock Input High	15	23
Inputs Low	13	21

DIRECT INPUT OPERATION ① MC922 and MC822 only

S_D	C_D	Q	$\overline{Q}$
0	0	②	③
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

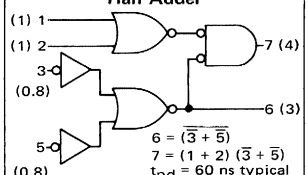
t_n		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

HALF ADDERS

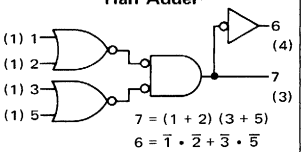
MC908G • MC808G
Half Adder



$6 = (\overline{\overline{3} + \overline{5}})$
$7 = (1 + 2)(\overline{3} + \overline{5})$
t_{pd} = 60 ns typical

Total Power Dissipation mW typ		
	MC908G	MC808G
Input High	14	19
Inputs Low	8.5	12.5

MC912G • MC812G
Half Adder

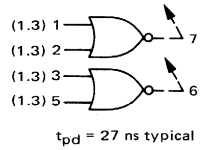


$7 = (1 + 2)(3 + 5)$
$6 = \overline{1} \cdot \overline{2} + \overline{3} \cdot \overline{5}$
t_{pd} = 66 ns typical

Total Power Dissipation mW typ		
	MC912G	MC812G
Input High	11.5	15.5
Inputs Low	5.5	10.5

EXPANDER

MC921G • MC821G
Dual 2-Input Expander



t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC921G	MC821G
Input High	3.0	3.0
Inputs Low	--	--

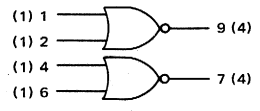
mW MRTL DEVICES AVAILABLE IN FLAT PACKAGES

The logic diagrams on these three pages describe the MC908/MC808 MRTL integrated circuits available in flat packages, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of −55 to +125°C with V_{CC} = 3.0 V ±10% for the MC908 Series, and 0 to +75°C with V_{CC} = 3.6 V ±10% for the MC808 Series. For the TO-91 flat package, V_{CC} is applied to pin 10, with ground connected to pin 5. For the TO-86 flat package, V_{CC} is applied to pin 14, with ground connected to pin 7.

GATES

MC910F • MC810F
Dual 2-Input Gate

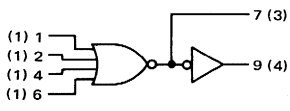


$9 = \overline{1 + 2}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC910F	MC810F
Input High	8.0	10
Inputs Low	1.0	2.5

MC911F • MC811F
4-Input Gate



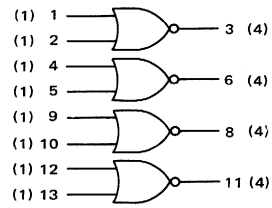
$7 = \overline{1 + 2 + 4 + 6}$

$9 = 1 + 2 + 4 + 6$

t_{pd} = 60 ns typical

Total Power Dissipation mW typ		
	MC911F	MC811F
Input High	6.0	8.0
Inputs Low	3.5	5.5

MC917F • MC817F
Quad 2-Input Gate

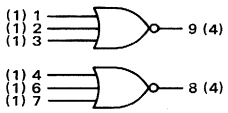


$3 = \overline{1 + 2}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC917F	MC817F
Input High	16	20
Inputs Low	2.5	5.0

MC918F • MC818F
Dual 3-Input Gate

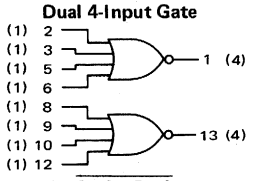


$9 = \overline{1 + 2 + 3}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC918F	MC818F
Input High	9.5	12
Inputs Low	1.0	2.5

MC919F • MC819F
Dual 4-Input Gate

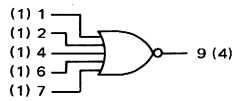


$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC919F	MC819F
Input High	11	1.3
Inputs Low	1.0	2.5

MC928F • MC828F
5-Input Gate

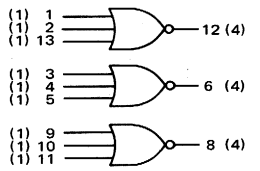


$9 = \overline{1 + 2 + 4 + 6 + 7}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC928F	MC828F
Input High	6.5	7.5
Inputs Low	0.5	1.0

MC993F • MC893F
Triple 3-Input Gate



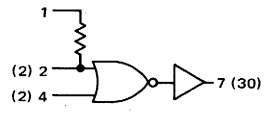
$12 = \overline{1 + 2 + 13}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC993F	MC893F
Input High	14	18
Inputs Low	2.0	3.5

BUFFERS

MC909F • MC809F
Buffer

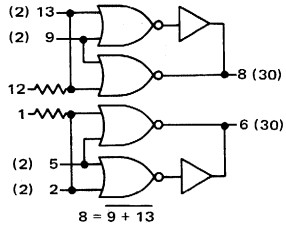


$7 = \overline{2 + 4}$

t_{pd} = 57 ns typical

Total Power Dissipation mW typ		
	MC909F	MC809F
Input High	5.5	7.0
Inputs Low	16	23

MC998F • MC898F
Dual 2-Input Buffer



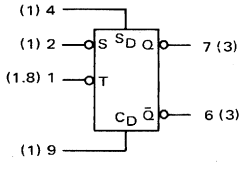
$8 = \overline{9 + 13}$

t_{pd} = 57 ns typical

Total Power Dissipation mW typ		
	MC998F	MC898F
Input High	11	14
Inputs Low	32	46

FLIP-FLOPS

MC913F • MC813F
Type D Flip-Flop



t_{pd} = 75 ns typical

Total Power Dissipation mW typ		
	MC913F	MC813F
Direct Set and Direct Clear Inputs Low, All other Inputs High	17.5	24
Inputs Low	13	17.5

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

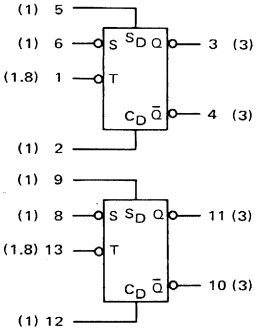
t_n	t_{n+1}	
S	Q	$\bar{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of pulse
t_{n+1} = time period subsequent to negative transition of clock pulse

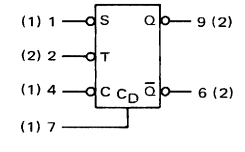
Total Power Dissipation mW typ		
	MC978F	MC878F
Direct Set and Direct Clear Inputs Low, All other Inputs High	35	48
Inputs Low	26	35

MC978F • MC878F
Dual Type D Flip-Flop



t_{pd} = 60 ns typical

MC920F • MC820F
J-K Flip-Flop



t_{pd} = 50 ns typical

Total Power Dissipation mW typ		
	MC920F	MC820F
Only Clock Input High	15.5	20.5
Inputs Low	10	14.5

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC920 and MC820 only

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

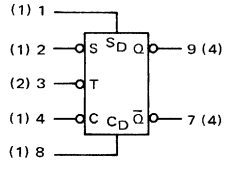
CLOCKED INPUT OPERATION ③ all types

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

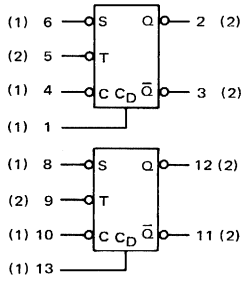
MC922F • MC822F
J-K Flip-Flop



t_{pd} = 70 ns typical

Total Power Dissipation mW typ		
	MC922F	MC822F
Only Clock Input High	17.5	24
Inputs Low	13	20

MC976F • MC876F
Dual J-K Flip-Flop

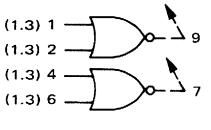


t_{pd} = 50 ns typical

Total Power Dissipation mW typ		
	MC976F	MC876F
Only Clock Input High	31	41
Inputs Low	20	29

EXPANDERS

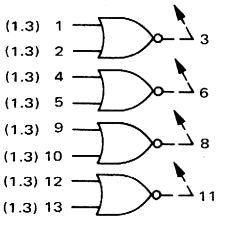
MC921F • MC821F
Dual 2-Input Expander



t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC921F	MC821F
Input High	3.0	3.0
Inputs Low	--	--

MC9921F • MC9821F
Quad 2-Input Expander



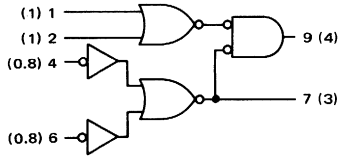
$3 = \overline{1 + 2}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC9921F	MC9821F
Input High	20	20
Inputs Low	–	–

HALF ADDERS

MC908F • MC808F
Half Adder



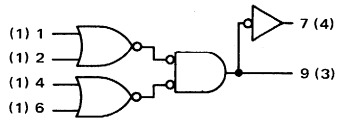
$9 = (1 + 2)(\overline{4} + \overline{6})$

$7 = (\overline{4} + \overline{6})$

t_{pd} = 60 ns typical

Total Power Dissipation mW typ		
	MC908F	MC808F
Input High	14	19
Inputs Low	8.5	12.5

MC912F • MC812F
Half Adder



$7 = \overline{1} \cdot \overline{2} + \overline{4} \cdot \overline{6}$

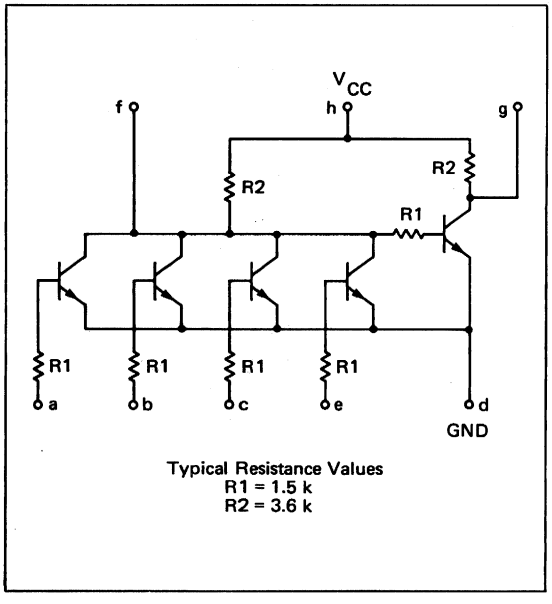
$9 = (1 + 2)(4 + 6)$

t_{pd} = 66 ns typical

Total Power Dissipation mW typ		
	MC912F	MC812F
Input High	11.5	15.5
Inputs Low	5.5	10.5

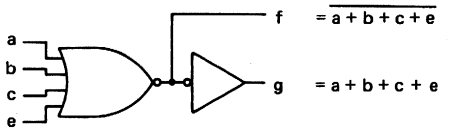
MC911 • MC811

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



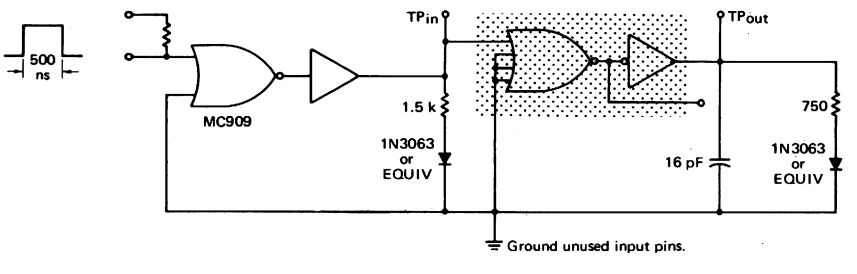
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

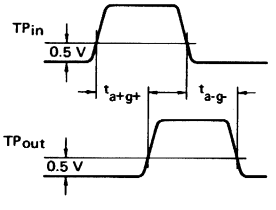
Provides the positive logic NOR function and its complement through an inverter. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules).



PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC911	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC811	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

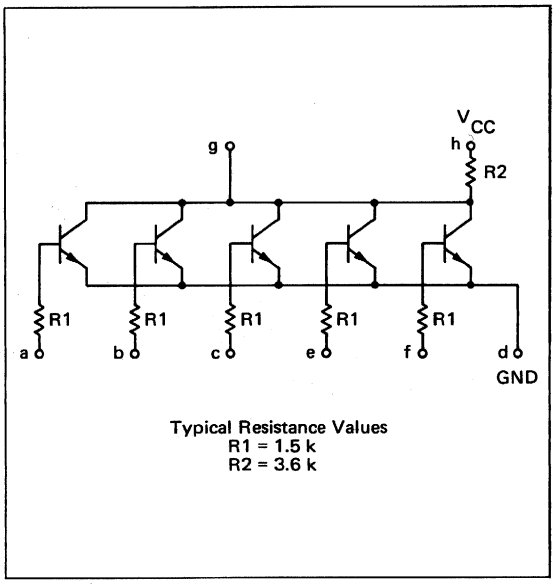
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC911 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC811 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b, c, e	-	h	-	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c, e	-	↓	-	↓
		c	-		-		-			-		-		-			c	-	a, b, e	-		-	
		e	-		-		-			-		-		-			e	-	a, b, c	-		-	
Output Current	I_{A3}	f	350	-	364	-	308	-	μAdc	420	-	430	-	395	-	μAdc	f	-	-	a,b, c, e	h	-	d
	I_{A4}	g	475	-	494	-	418	-		570	-	570	-	535	-	μAdc	g	-	-	f	↓	-	a,b,c,d,e
	I_{AM}	g	-	730	-	815	-	830	↓	-	-	-	-	-	-	-	g	-	-	f		-	a,b,c,d,e
Output Voltage	V_{out}	f	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	a	-	-	h	-	b, c, d, e
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	-	a, c, d, e
		f	-		-		-			-		-		-			-	c	-	-		-	a, b, d, e
		f	-		-		-			-		-		-			-	e	-	-		-	a, b, c, d
		g	-		-		-			-		-		-			-	f	-	-		-	a,b,c,d,e
Saturation Voltage	$V_{CE(sat)}$	f	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	a	-	-	-	h	-	b, c, d, e
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	-	-	↓	-	a, c, d, e
		f	-		-		-			-		-		-			c	-	-	-		-	a, b, d, e
		f	-		-		-			-		-		-			e	-	-	-		-	a, b, c, d
		g	-		-		-			-		-		-			f	-	-	-		-	a,b,c,d,e
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	h	a,b,c,d,e
																	Pulse In	Pulse Out					
Switching Time	t	a+g+	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	a	g	-	-	h	-	b, c, d, e
		a-g-	-	-	-	70	-	-	ns	-	-	-	70	-	-	ns	a	g	-	-	h	-	b, c, d, e

Pins not listed are left open.

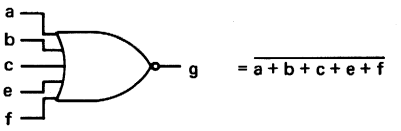
MC928 • MC828

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



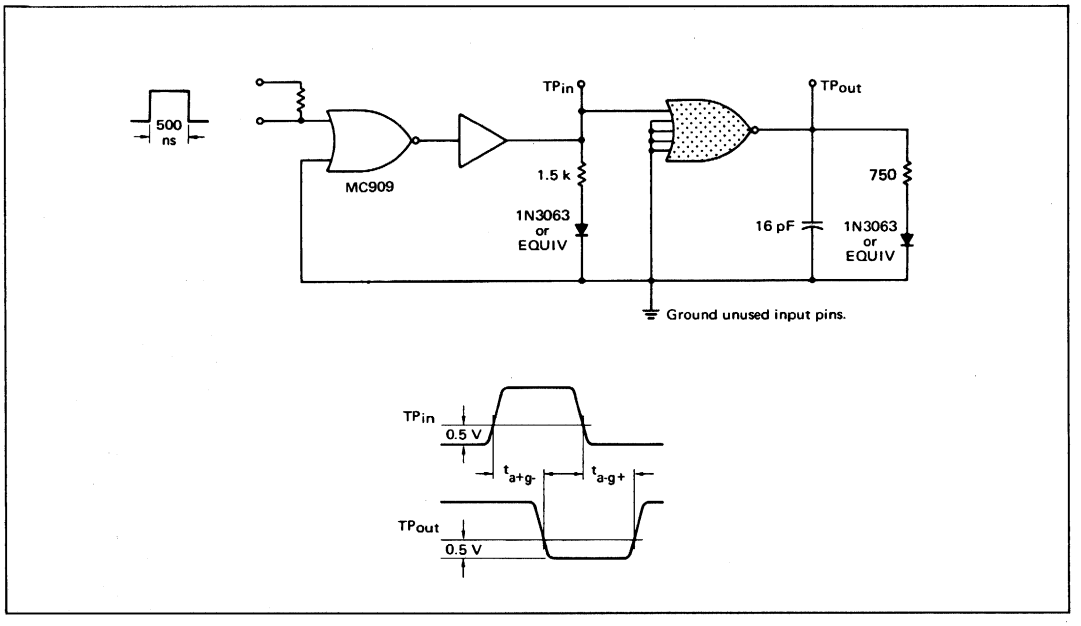
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

Provides the positive logic NOR function. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules).



PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC928	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC828	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

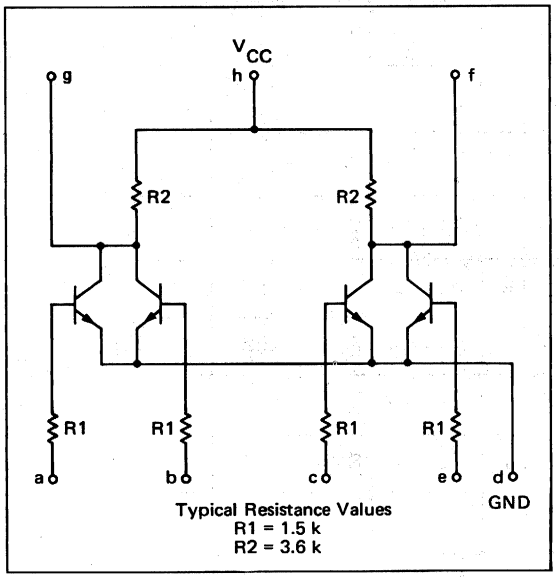
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC928 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC828 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b, c, e, f	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c, e, f	-	↓	↓
		c	-		-		-			-		-		-			c	-	a, b, e, f	-		
		e	-		-		-			-		-		-			e	-	a, b, c, f	-		
		f	-		-		-			-		-		-			f	-	a, b, c, e	-		
Output Current	I_{A4}	g	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	g	-	-	a,b,c,e,f	h	d
Output Voltage	V_{out}	g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	a	-	-	h	b,c,d,e,f
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	a,c,d,e,f
		g	-		-		-			-		-		-			-	c	-	-		a,b,d,e,f
		g	-		-		-			-		-		-			-	e	-	-		a,b,c,d,f
		g	-		-		-			-		-		-			-	f	-	-		a,b,c,d,e
Saturation Voltage	$V_{CE(sat)}$	g	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	a	-	-	-	h	b,c,d,e,f
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	-	-	↓	a,c,d,e,f
		g	-		-		-			-		-		-			c	-	-	-		a,b,d,e,f
		g	-		-		-			-		-		-			e	-	-	-		a,b,c,d,f
		g	-		-		-			-		-		-			f	-	-	-		a,b,c,d,e
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	h	a,b,c,d,e,f
																	Pulse In	Pulse Out				
Switching time	t	a+g-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	a	g	-	-	h	b,c,d,e,f
		a-g+	-	-	-	60	-	-	ns	-	-	-	60	-	-	ns	a	g	-	-	h	b,c,d,e,f

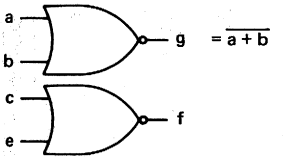
Pins not listed are left open.

MC910 • MC810

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.

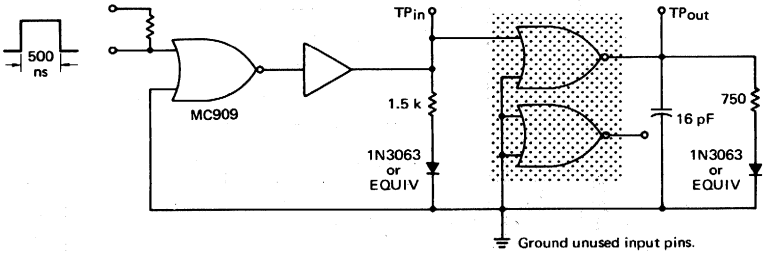


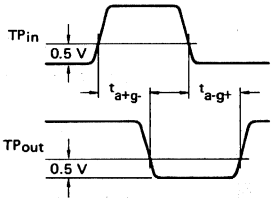
Two 2-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.



PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

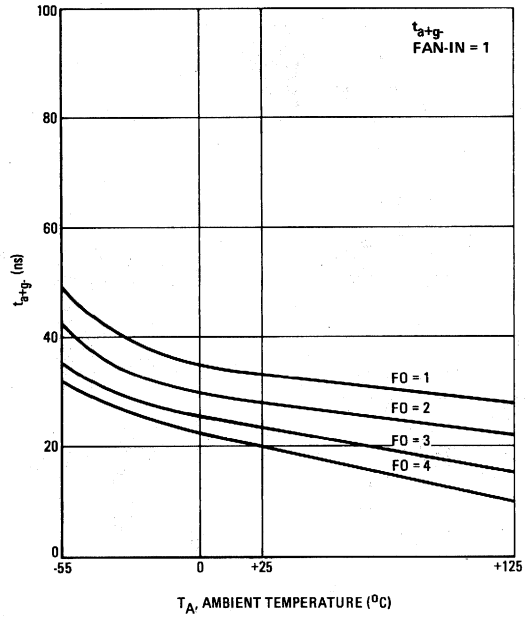
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

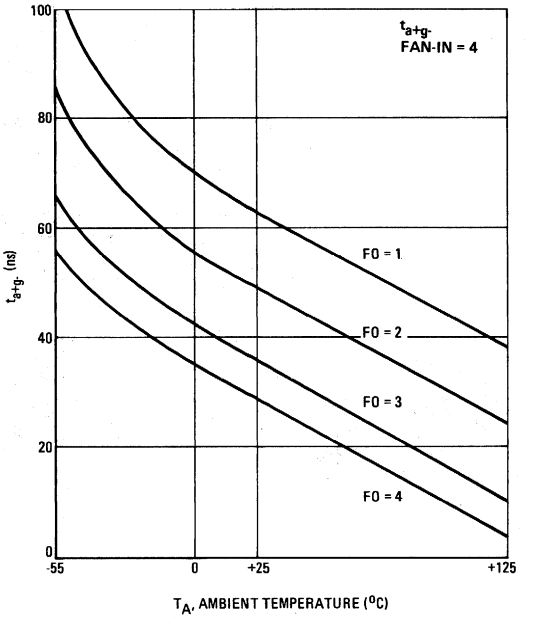
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC910	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC810	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

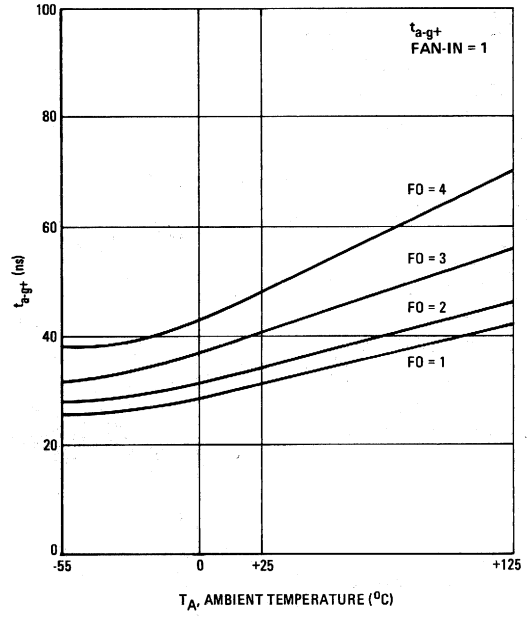
Characteristic	Symbol	Pin Under Test	MC910 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC810 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	µAdc	-	150	-	140	-	140	µAdc	a	-	b	-	h	d
		b	-	125	-	130	-	110	µAdc	-	150	-	140	-	140	µAdc	b	-	a	-	h	d
Output Current	I_{A4}	g	475	-	494	-	418	-	µAdc	570	-	570	-	535	-	µAdc	g	-	c	a, b	h	d
	I_{AM}	g	-	730	-	815	-	830	µAdc	-	-	-	-	-	-	-	g	-	c	a, b	h	d
Output Voltage	V_{out}	g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	a	-	-	h	b, d
		g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	b	-	-	h	a, d
Saturation Voltage	$V_{CE(sat)}$	g	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	a	-	-	-	h	b, d
		g	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	b	-	-	-	h	a, d
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	µAdc	-	100	-	100	-	100	µAdc	-	-	-	-	h	a, b, d
																	Pulse In	Pulse Out				
Switching Time	t	a+g-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	a	g	-	-	h	d
		a-g+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	a	g	-	-	h	d

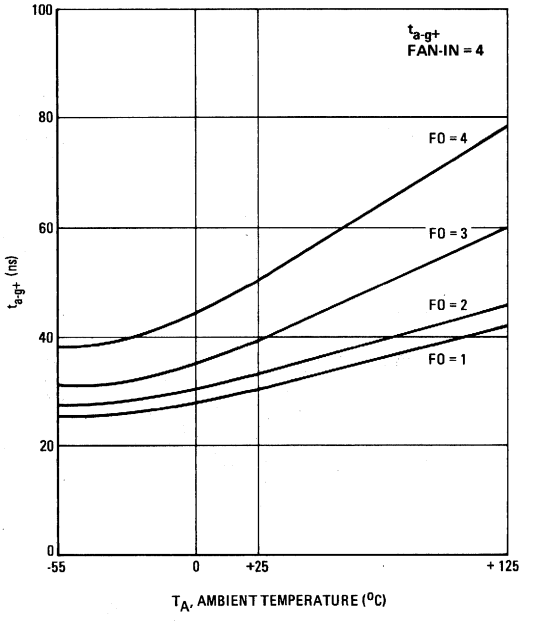
Ground input pins of gate not under test. Other pins not listed are left open.

SWITCHING CHARACTERISTICS



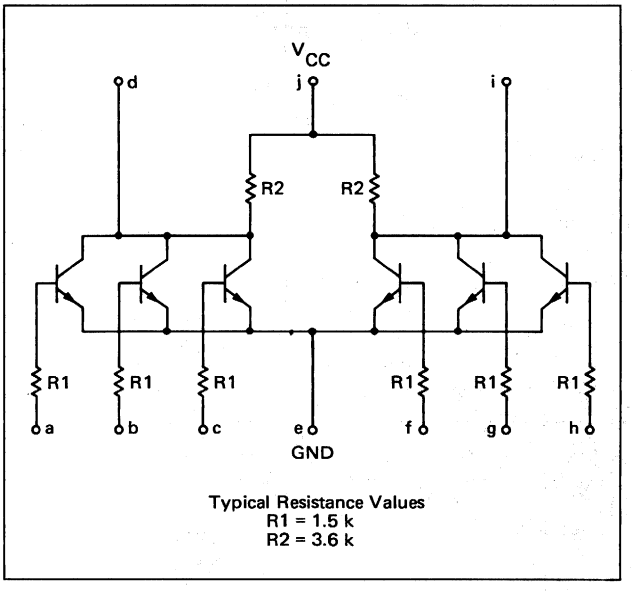






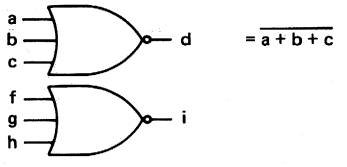
MC918 • MC818

Available in TO-100 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



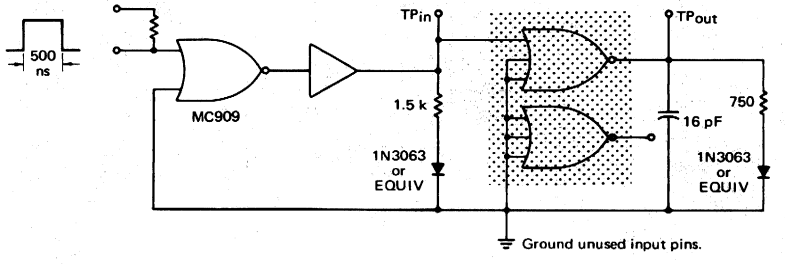
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

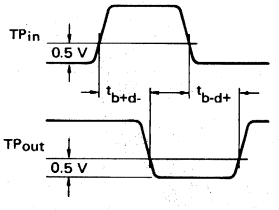
Two 3-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.



PIN CONNECTIONS										
Schematic	a	b	c	d	e	f	g	h	i	j
G Package (TO-100)	1	2	3	4	5	6	7	8	9	10
F Package (TO-91)	1	2	3	9	5	4	6	7	8	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
Other gates are tested in the same manner.

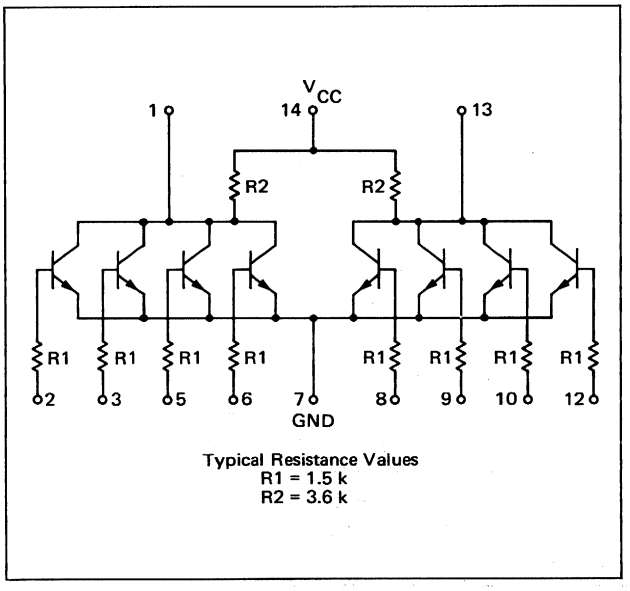
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC918	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC818	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

Characteristic	Symbol	Pin Under Test	MC918 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC818 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b, c	-	j	e
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c	-	↓	↓
		c	-		-		-			-		-		-			c	-	a, b	-		
Output Current	I_{A4}	d	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	d	-	g	a, b, c	j	e
	I_{AM}	d	-	730	-	815	-	830	μAdc	-	-	-	-	-	-	-	d	-	g	a, b, c	j	e
Output Voltage	V_{out}	d	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	a	-	-	j	b, c, e
		d	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	a, c, e
		d	-		-		-			-		-		-			-	c	-	-		a, b, e
Saturation Voltage	$V_{CE(sat)}$	d	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	a	-	-	-	j	b, c, e
		d	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	-	-	↓	a, c, e
		d	-		-		-			-		-		-			c	-	-	-		a, b, e
Isolation Leakage Current	I_L	j	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	j	a, b, c, e
																	Pulse In	Pulse Out				
Switching Time	t	b+d-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	b	d	-	-	j	a, c, e
		b-d+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	b	d	-	-	j	a, c, e

Ground input pins of gates not under test. Other pins not listed are left open.

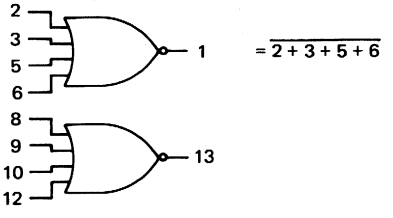
MC919 • MC819

Available in TO-86 Flat Package, Add F Suffix.



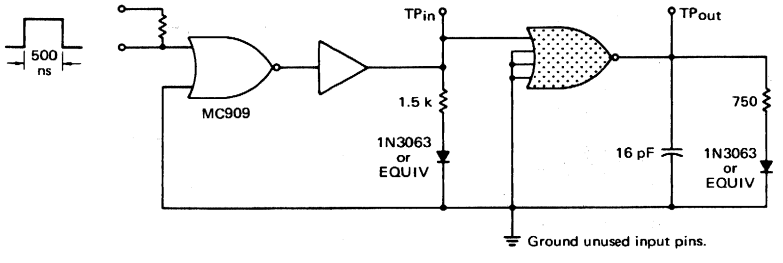
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

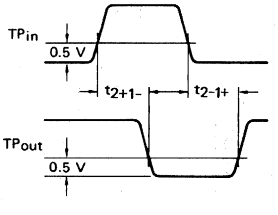
Two 4-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.



$= \overline{2+3+5+6}$

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
Other gates are tested in the same manner.

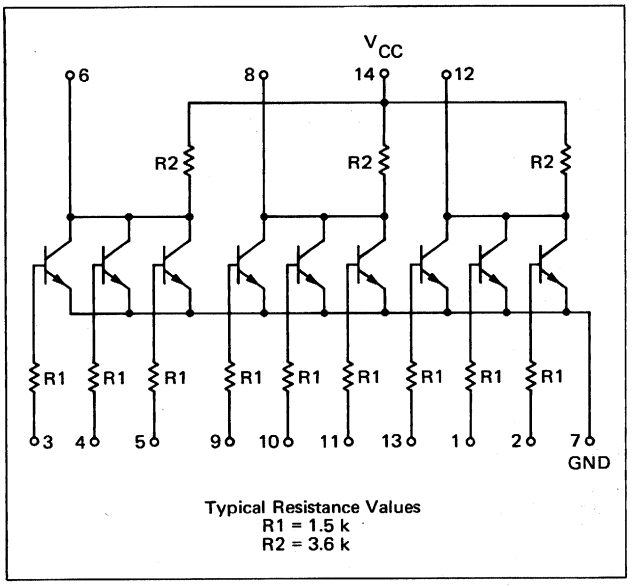
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC919	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC819	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.880	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

Characteristic	Symbol	Pin Under Test	MC919 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC819 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	2	-	3, 5, 6	-	14	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2, 5, 6	-	↓	↓
		5	-		-		-			-		-		-			5	-	2, 3, 6	-		
		6	-		-		-			-		-		-			6	-	2, 3, 5	-		
Output Current	I_{A4}	1	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	1	-	8	2, 3, 5, 6	14	7
	I_{AM}	1	-	730	-	815	-	830	μAdc	-	-	-	-	-	-	-	1	-	8	2, 3, 5, 6	14	7
Output Voltage	V_{out}	1	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	-	-	14	3, 5, 6, 7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	2, 5, 6, 7
		1	-		-		-			-		-		-			-	5	-	-		2, 3, 6, 7
		1	-		-		-			-		-		-			-	6	-	-		2, 3, 5, 7
Saturation Voltage	$V_{CE(sat)}$	1	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	2	-	-	-	14	3, 5, 6, 7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	-	-	↓	2, 5, 6, 7
		1	-		-		-			-		-		-			5	-	-	-		2, 3, 6, 7
		1	-		-		-			-		-		-			6	-	-	-		2, 3, 5, 7
Isolation Leakage Current	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	14	2,3,5,6,7
																	Pulse In	Pulse Out				
Switching Time	t	2+1-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	2	1	-	-	14	5, 6, 7
		2-1+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	2	1	-	-	14	5, 6, 7

Ground input pins of gates not under test. Other pins not listed are left open.

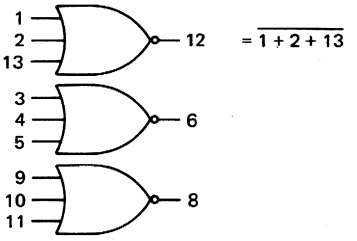
MC993 • MC893

Available in TO-86 Flat Package, Add F Suffix.

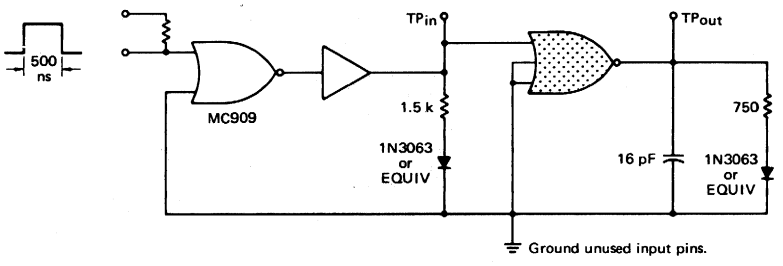


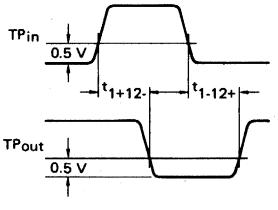
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

Three 3-input positive logic NOR gates in a single package may be used independently, paralleled for increased number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
Other gates are tested in the same manner.

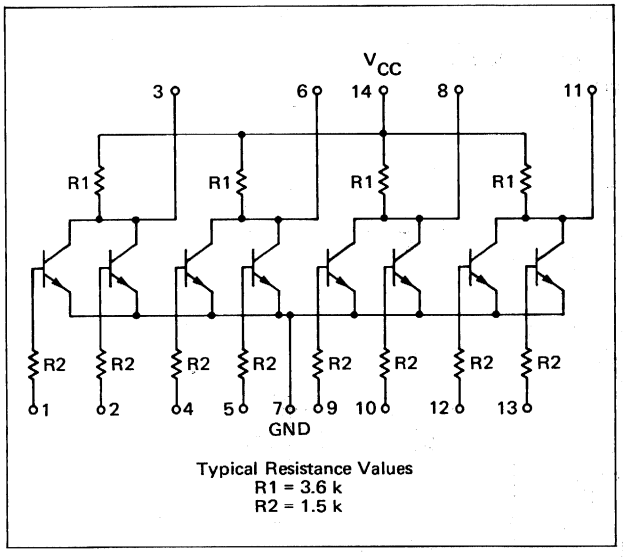
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC993	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC893	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

Characteristic	Symbol	Pin Under Test	MC993 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC893 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	1	-	2, 13	-	14	7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1, 13	-	↓	↓
		13	-		-		-			-		-		-			13	-	1, 2	-		
Output Current	I_{A4}	12	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	12	-	3, 9	1, 2, 13	14	7
	I_{AM}	12	-	730	-	815	-	830	μAdc	-	-	-	-	-	-	-	12	-	3, 9	1, 2, 13	14	7
Output Voltage	V_{out}	12	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	13	-	-	14	1, 2, 7
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	2, 7, 13
		12	-		-		-			-		-		-			-	2	-	-		1, 7, 13
Saturation Voltage	$V_{CE(sat)}$	12	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	13	-	-	-	14	1, 2, 7
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	1	-	-	-	↓	2, 7, 13
		12	-		-		-			-		-		-			2	-	-	-		1, 7, 13
Isolation Leakage Current	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	14	1,2,7,13
																	Pulse In	Pulse Out				
Switching Time	t	1+12-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	1	12	-	-	14	2, 7, 13
		1-12+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	12	-	-	14	2, 7, 13

Ground input pins of gates not under test. Other pins not listed are left open.

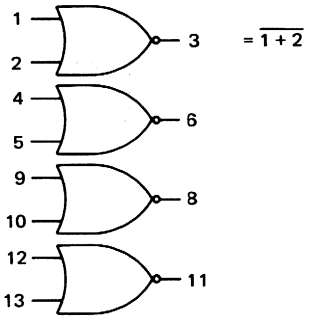
MC917 • MC817

Available in TO-86 Flat Package, Add F Suffix.

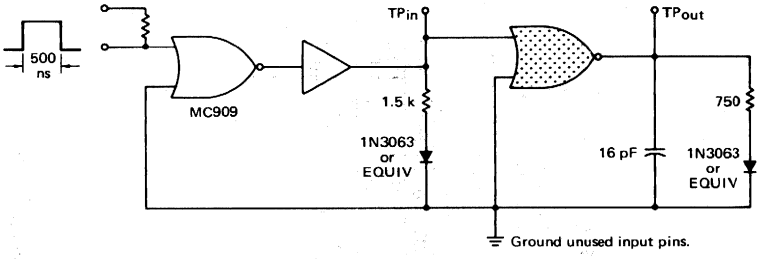


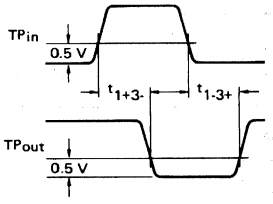
Typical Resistance Values
R1 = 3.6 k
R2 = 1.5 k

This gate element consists of four 2-input positive logic NOR gate circuits in a single package. Each may be used independently or connected together to form non-inverting gates or flip-flops.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
Other gates are tested in the same manner.

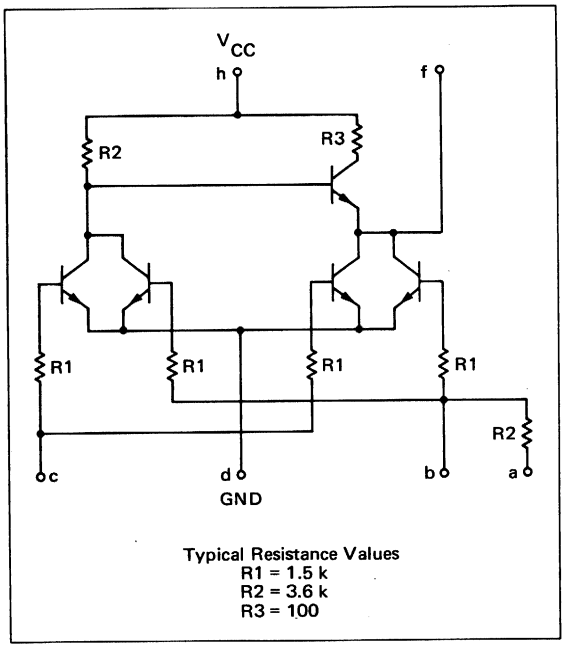
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC917	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC817	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

Characteristic	Symbol	Pin Under Test	MC917 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC817 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	1	-	2	-	14	7
		2	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	2	-	1	-	14	7
Output Current	I_{A4}	3	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	3	-	4, 9, 12	1, 2	14	7
	I_{AM}	3	-	730	-	815	-	830	μAdc	-	-	-	-	-	-	-	3	-	4, 9, 12	1, 2	14	7
Output Voltage	V_{out}	3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	1	-	-	14	2, 7
		3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc		2	-	-	14	1, 7
Saturation Voltage	$V_{CE(sat)}$	3	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	1	-	-	-	14	2, 7
		3	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	2	-	-	-	14	1, 7
Isolation Leakage Current	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	14	1, 2, 7
																	Pulse In	Pulse Out				
Switching Time	t	1+3-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	1	3	-	-	14	2, 7
		1-3+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	3	-	-	14	2, 7

Ground input pins of gates not under test. Other pins not listed are left open.

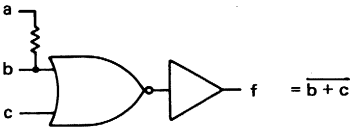
MC909 • MC809

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



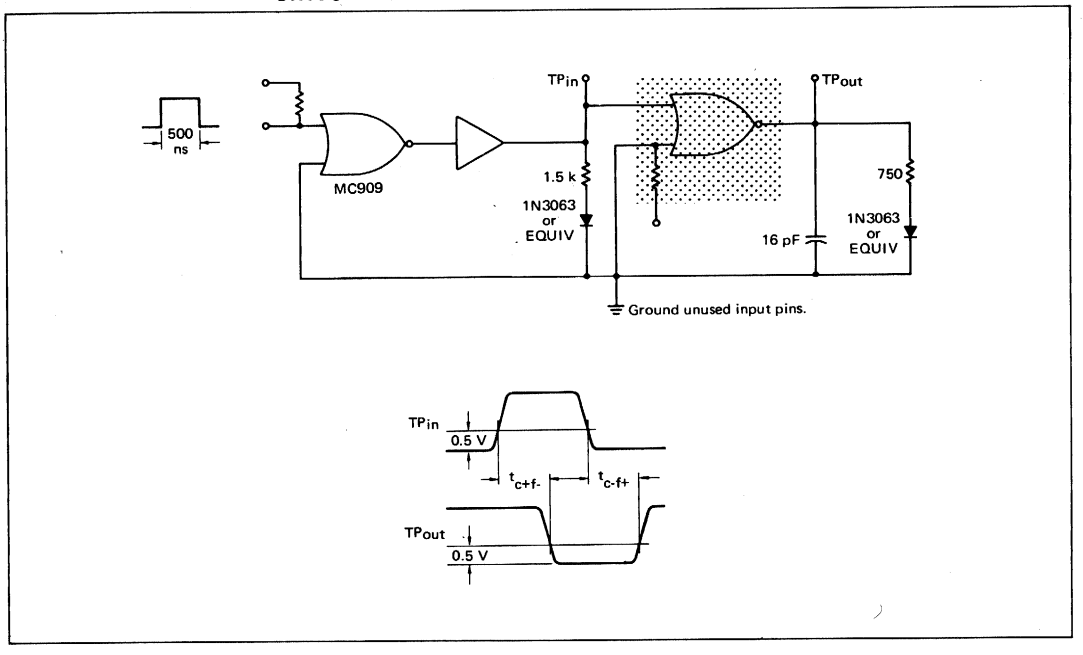
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 100

This buffer is designed to drive a greater number of loads than the basic Resistor Transistor Logic circuit. Returning an input resistor to V_{CC} allows for capacitive coupling in multivibrator and differentiator applications.



PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	–	6	–	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



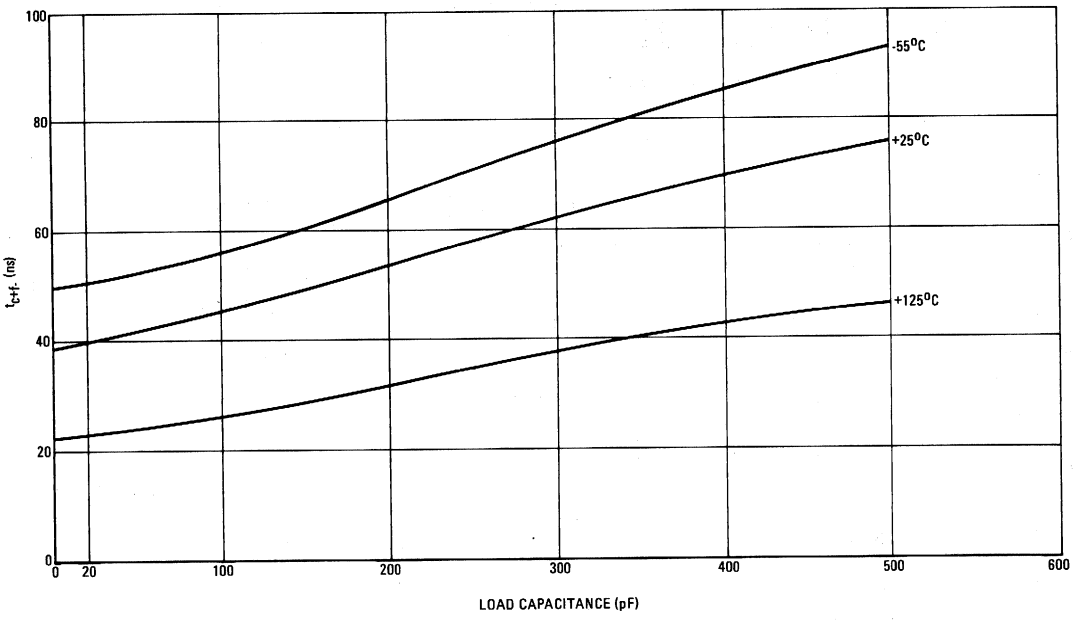
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(kΩ)
MC909	−55°C	0.970	0.935	1.80	0.650	3.00	4.27
	+25°C	0.805	0.750	1.80	0.450	3.00	4.3
	+125°C	0.590	0.555	1.80	0.260	3.00	5.0
MC809	0°C	0.880	0.850	1.80	0.500	3.60	4.3
	+25°C	0.830	0.800	1.80	0.460	3.60	4.3
	+75°C	0.740	0.710	1.80	0.400	3.60	4.7

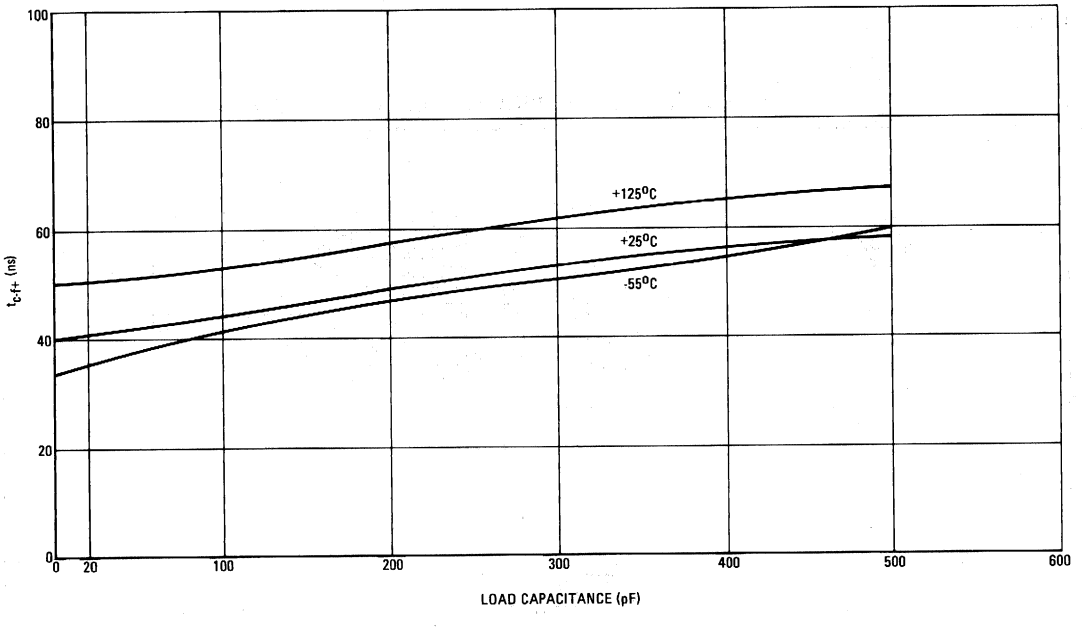
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC909 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC809 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{RH}*	Gnd
Input Current	$2I_{in}$	b	-	250	-	260	-	220	μAdc	-	300	-	280	-	280	μAdc	b	-	c	-	h	-	d
		c	-	250	-	260	-	220	μAdc	-	300	-	280	-	280	μAdc	c	-	b	-	h	-	d
Output Current	I_{AB}	f	3.75	-	4.0	-	3.3	-	mAdc	4.5	-	4.5	-	4.5	-	mAdc	f	-	-	b, c	h	-	d
Output Voltage	V_{out}	f	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	b	-	-	h	f	c, d
		f	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	c	-	-	h	f	b, d
Saturation Voltage	$V_{CE(sat)}$	f	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	b	-	-	-	h	f	c, d
		f	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	c	-	-	-	h	f	b, d
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	h	-	b, c, d
Switching Time	t	c+f-	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In: c	Pulse Out: f	-	-	h	-	b, d
		c-f+	-	-	-	70	-	-	ns	-	-	-	70	-	-	ns	c	f	-	-	h	-	b, d

Pins not listed are left open. *Resistor value to V_{CC}

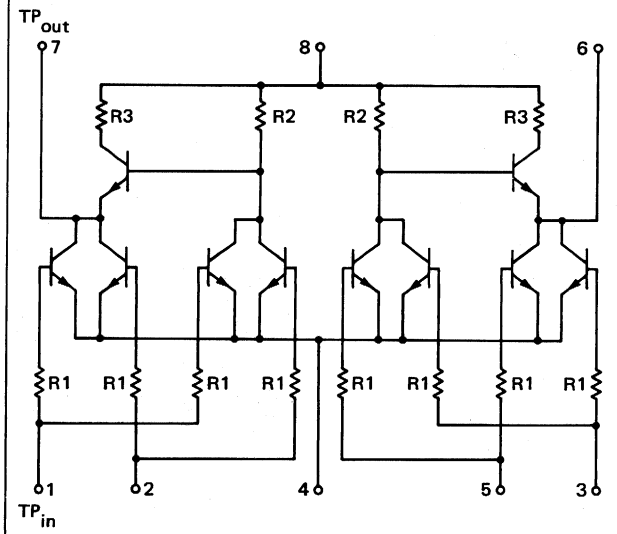
PROPAGATION DELAY versus TEMPERATURE





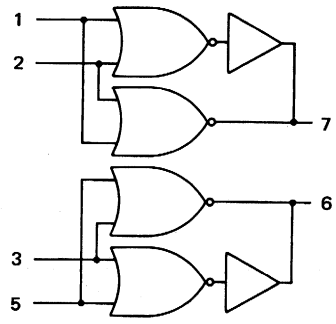
MC981 • MC881

Available in TO-99 Metal Can, Add G Suffix.



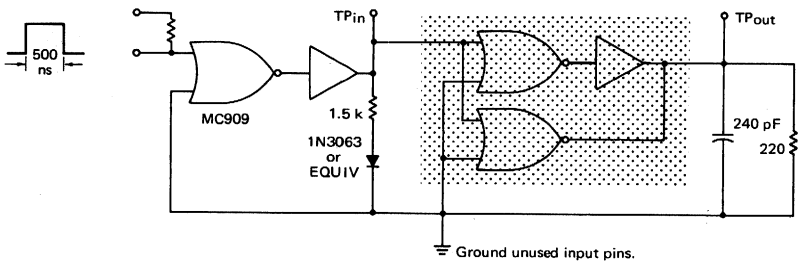
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 100

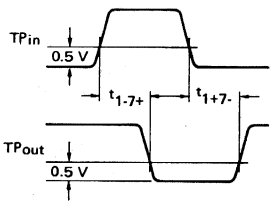
These Buffers are designed to drive a greater number of loads than the basic Resistor Transistor Logic circuit.



$7 = \overline{1+2}$

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one buffer only.
The other buffer is tested in the same manner.

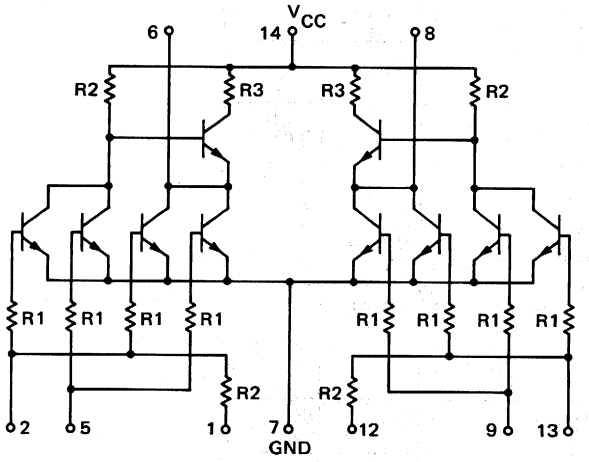
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(kΩ)
MC981	−55°C	0.970	0.935	1.80	0.650	3.00	4.27
	+25°C	0.805	0.750	1.80	0.450	3.00	4.3
	+125°C	0.590	0.555	1.80	0.260	3.00	5.0
MC881	0°C	0.880	0.850	1.80	0.500	3.60	4.3
	+25°C	0.830	0.800	1.80	0.460	3.60	4.3
	+75°C	0.740	0.710	1.80	0.400	3.60	4.7

Characteristic	Symbol	Pin Under Test	MC981 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC881 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{RH}*	Gnd
Input Current	$2I_{in}$	1	-	250	-	260	-	220	μAdc	-	300	-	280	-	280	μAdc	1	-	2	-	8	-	4
		2	-	250	-	260	-	220	μAdc	-	300	-	280	-	280	μAdc	2	-	1	-	8	-	4
Output Current	I_{AB}	7	3.75	-	4.0	-	3.3	-	mAdc	4.5	-	4.5	-	4.5	-	mAdc	7	-	-	1,2	8	-	4
Output Voltage	V_{out}	7	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	1	-	-	8	7	2,4
		7	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	-	-	8	7	1,4
Saturation Voltage	$V_{CE(sat)}$	7	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	1	-	-	-	8	7	2,4
		7	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	2	-	-	-	8	7	1,4
Isolation Leakage Current	I_L	8	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	8	-	1,2,3,4,5
																	Pulse In	Pulse Out					
Switching Time	t	1+7-	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	1	7	-	-	8	-	2,4
		1-7+	-	-	-	70	-	-	ns	-	-	-	70	-	-	ns	1	7	-	-	8	-	2,4

Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

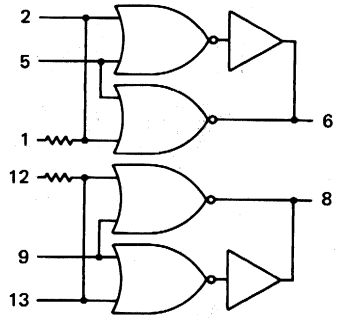
MC998 • MC898

Available in TO-86 Flat Package, Add F Suffix.



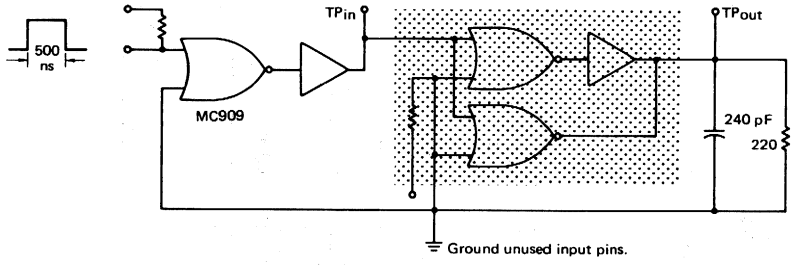
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 100

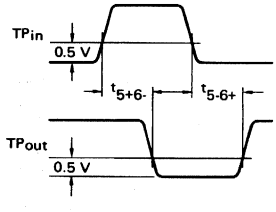
These Buffers are designed to drive a greater number of loads than the basic Resistor Transistor Logic Circuit. Returning an input resistor to V_{CC} allows for capacitive coupling in multivibrator and differentiator applications.



$6 = \overline{2 + 5} = \overline{2} \cdot \overline{5}$

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one buffer only.
The other buffer is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	(kΩ)
MC998	−55°C	0.970	0.935	1.80	0.650	3.00	0.500	4.27
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400	4.3
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300	5.0
MC898	0°C	0.880	0.850	1.80	0.500	3.60	0.450	4.3
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400	4.3
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350	4.7

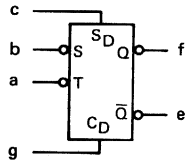
Characteristic	Symbol	Pin Under Test	MC998 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC898 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	V_{RH}*	Gnd
Input Current	$2I_{in}$	2	-	250	-	260	-	220	μAdc	-	300	-	280	-	280	μAdc	2	-	5	-	14	-	-	7
		5	-	250	-	260	-	220	μAdc	-	300	-	280	-	280	μAdc	5	-	2	-	14	-	-	7
Output Current	I_{AB}	6	3.75	-	4.0	-	3.3	-	mAdc	4.5	-	4.5	-	4.5	-	mAdc	6	-	-	2,5	14	-	-	7
Output Voltage	V_{out}	6	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	-	-	14	-	6	5,7
		6	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	5	-	-	14	-	6	2,7
Saturation Voltage	$V_{CE(sat)}$	6	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	-	2	-	14	-	6	5,7
		6	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	-	5	-	14	-	6	2,7
Isolation Leakage Current	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	-	2,5,7
																	Pulse In	Pulse Out						
Switching Time	t	5+6-	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	5	6	-	-	14	-	-	2,7
		5-6+	-	-	-	70	-	-	ns	-	-	-	70	-	-	ns	5	6	-	-	14	-	-	2,7

Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

MC913 • MC813

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.

The MC913/MC813 RTL Type D Flip-Flop is a storage element that stores the state of pin b during negative transitions of pin a. The flip-flop is not affected by changes of pin b during either the low or high state of the clock. Using pins c and g as inputs produces a standard R-S flip-flop.



DIRECT INPUT OPERATION ①

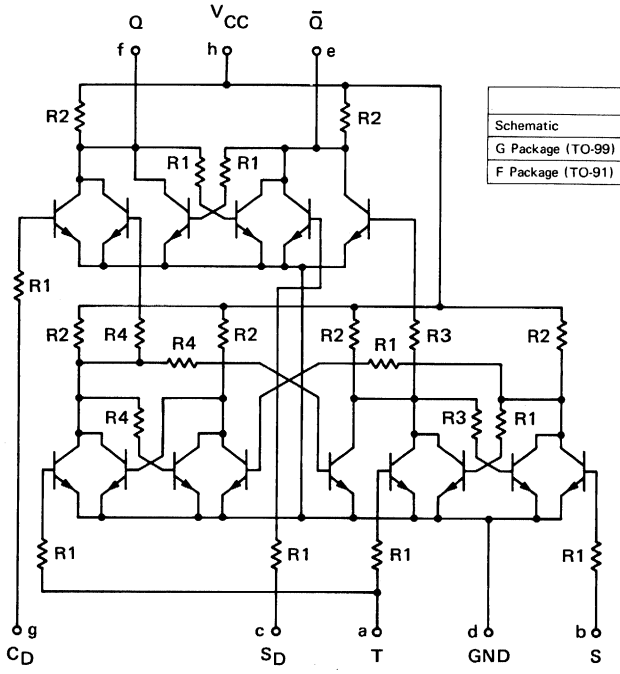
S_D	C_D	Q	$\bar{Q}$
0	0	⑤	⑤
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n	$t_n + 1$	
S	Q	$\bar{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
$t_n + 1$ = time period subsequent to negative transition of clock pulse



PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 180
R4 = 480

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC913	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC813	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC913 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC813 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	$1.8\ I_{in}$	a	-	225	-	234	-	198	μAdc	-	270	-	252	-	252	μAdc	a	-	-	-	h	-	b, c, d, g
	$1.8\ I_{in}$	a	-	225	-	234	-	198		-	270	-	252	-	252		a	-	b	-		-	c, d, g
	I_{in}	b*	-	125	-	130	-	110		-	150	-	140	-	140		b	-	-	a		-	c, d, g
		c*	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		c	-	b	↓		-	d, g
		g*	-		-		-			-		-		-			g	-	-			-	b, c, d
Output Current	I_{A3}	e	350	-	364	-	308	-	μAdc	420	-	430	-	395	-	μAdc	e	a	b, g	c	h	-	d
		e*		-		-		-			-		-		-		e	-	g	a, c		-	b, d
		f		-		-		-			-		-		-		-	g	a, c	-		-	b, d
		f*	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	f	b	c	a, g	↓	-	d
Output Voltage	V_{out}	e	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	c	a, g	-	h	-	b, d
		e	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	f	a	-		-	b, c, d, g
		f	-		-		-			-		-		-			-	g	a, c	-		-	b, d
		f	-		-		-			-		-		-			-	e	a	-		-	b, c, d, g
Saturation Voltage	$V_{CE\,(sat)}$	e	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	c	-	a, g	-	h	-	b, d
		e	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	f	-	a	-		-	b, c, d, g
		e*	-		-		-			-		-		-			-	b	g	a		-	c, d
		f	-		-		-			-		-		-			g	-	a, c	-		-	b, d
		f	-		-		-			-		-		-			e	-	a	-		-	b, c, d, g
		f*	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	c	a, b	↓	-	d, g
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	h	a, b, c, d, g

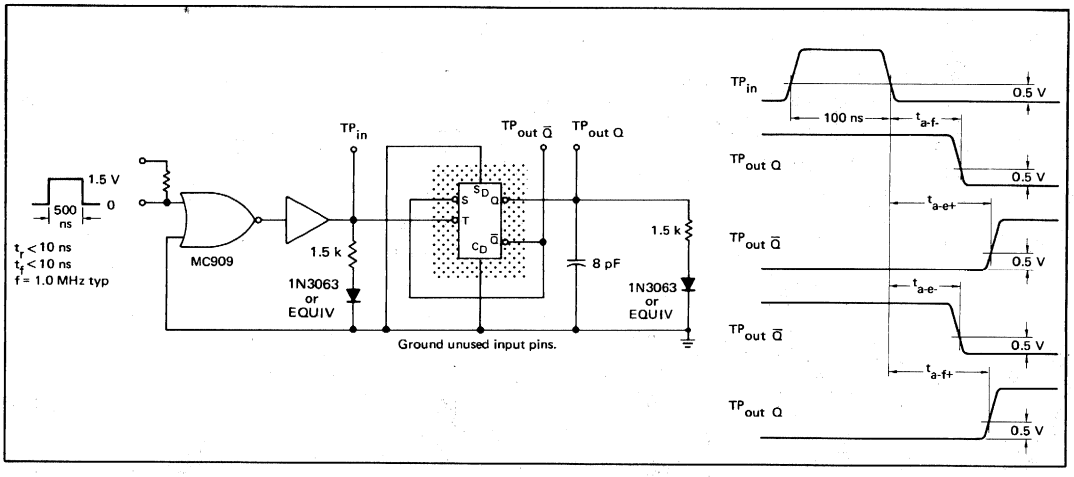
Pins not listed are left open.

*The voltage applied to pin a must change from V_{RL} to V_{off} prior to making measurements.

V_{RL} = Resistance value to V_{CC}; V_{RL} = 2.8 k ohms @ −55°C, @ 0°C; V_{RL} = 2.7 k ohms @ +25°C, V_{RL} = 3.0 k ohms @ +125°C @ +75°C

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

FIGURE 1



SET-UP AND RELEASE TIMES TEST CIRCUIT AND WAVEFORMS

FIGURE 2A

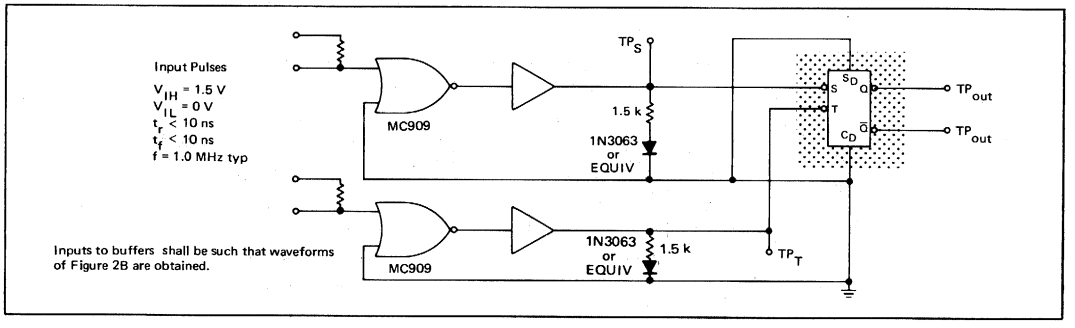
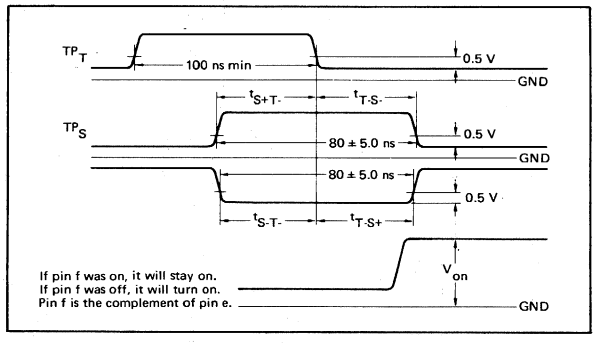


FIGURE 2B

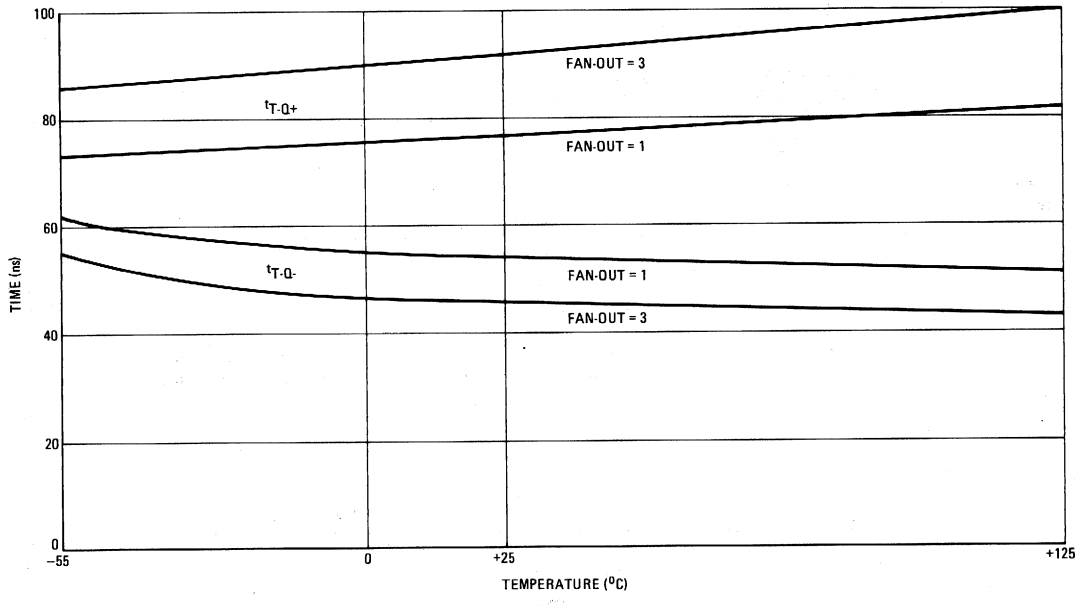


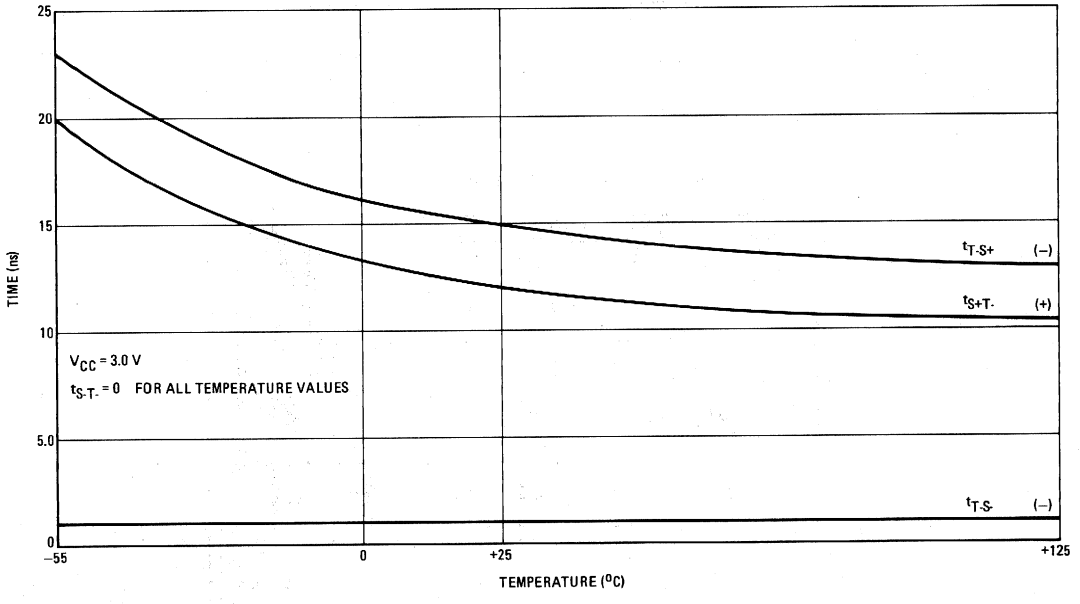
SWITCHING TIMES

Test	Fig. No.	ns @ 25°C	
		min	max
$t_{T-\bar{Q}-}$*	1	--	80
$t_{T-\bar{Q}+}$*	1	--	120
t_{T-Q-}*	1	--	80
t_{T-Q+}*	1	--	120
t_{S+T-}	2	60	--
t_{T-S-}	2	30	--
t_{S-T-}	2	60	--
t_{T-S+}	2	30	--

*Tie pin b to pin e

SWITCHING TIMES versus TEMPERATURE

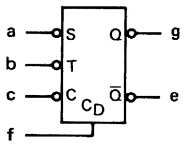




MC920 • MC820

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.

J-K Flip-Flop with a direct clear input in addition to the clocked inputs.

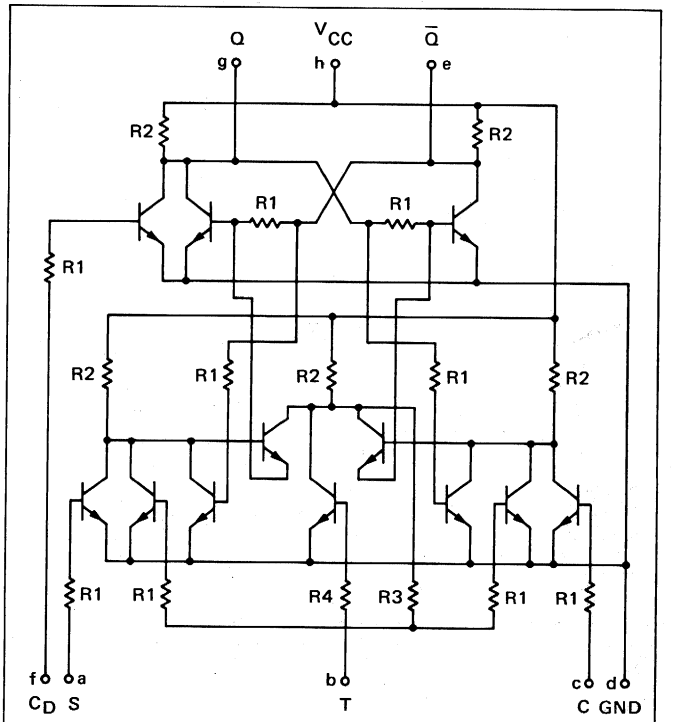


Direct Input (C_D) must be low.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse.
Q_n = state of Q output in time period t_n.

CLOCKED INPUT OPERATION

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 3.0 k
R4 = 750

ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_{LL}
MC920	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC820	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

Characteristic	Symbol	Pin Under Test	MC920 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC820 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	e	-	h	-	d
	$2I_{in}$	b	-	250	-	260	-	220		-	300	-	280	-	280		b	-	a, c	-		-	
	I_{in}	c	-	125	-	130	-	110		-	150	-	140	-	140		c	-	g	-		-	
	I_{in}	f	-	125	-	130	-	110		-	150	-	140	-	140		f	-	e	-		-	
Output Current	I_{A2}	e	238	-	247	-	209	-	μAdc	270	-	290	-	255	-	μAdc	-	e	a, f	-	h	-	d
		e		-		-		-			-		-		-		-	e, f	a	-		-	
		g#		-		-		-			-		-		-		-	g	c	f		-	
Output Voltage	V_{out}	e#	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	g	-	-	h	-	d
		e*#	-		-		-			-		-		-			-	a, c	-	-		-	d, f
		e*§	-		-		-			-		-		-			-	a	-	c		-	
		e*§	-		-		-			-		-		-			-	-	-	a, c		-	
		g	-		-		-			-		-		-			-	f	-	-		-	d, e
		g§	-		-		-			-		-		-			-	e	-	-		-	d
		g*§	-		-		-			-		-		-			-	a, c	-	-		-	d, f
		g*#	-		-		-			-		-		-			-	c	-	a		-	
		g*#	-		-		-			-		-		-			-	-	-	a, c		-	
Saturation Voltage	$V_{CE(sat)}$	e#	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	-	-	f	h	-	d
		g	-		-		-			-		-		-			-	-	f	-		-	d, e
		g§	-		-		-			-		-		-			-	-	-	-		-	d
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	h	d

Pins not listed are left open.

Pin e = LOW
§ Pin g = LOW
} Set by a momentary ground prior to the application of the negative-going clock pulse.

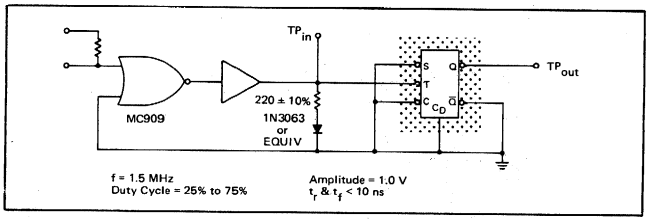
* = Clock Pulse to Pin b. (see Fig. 4)

SWITCHING TIMES

Test	Fig. No.	Over-All Temperature Range		Unit
		min	max	
T-$\bar{Q}$-	2	20	80	ns
T-Q+	2	--	120	ns
C_D+Q-	3	--	60	ns
C_D+$\bar{Q}$+	3	--	120	ns

NOTE: Waveform at the output test point should be ½ the frequency of the waveform at the input test point.

FIGURE 1 - TOGGLE MODE TEST CIRCUIT



SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 2

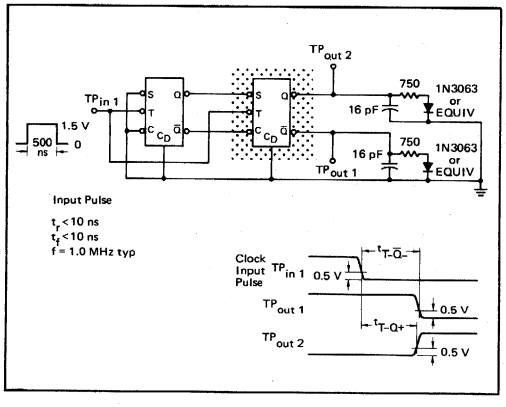


FIGURE 3

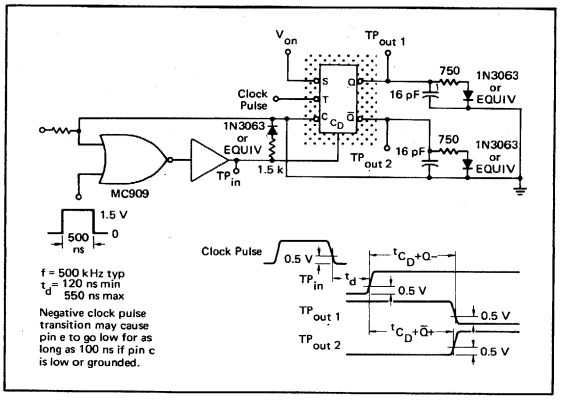
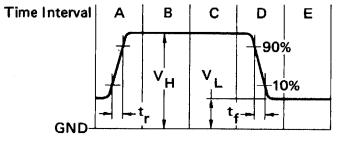


FIGURE 4



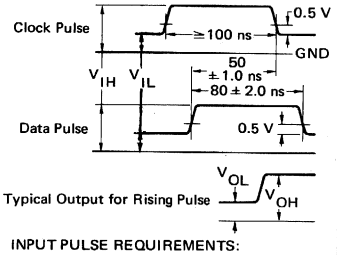
SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $<1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC820

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+850 ± 2.0 mVdc
0°C	+500 ± 2.0 mVdc	+900 ± 2.0 mVdc
+75°C	+400 ± 2.0 mVdc	+760 ± 2.0 mVdc

FIGURE 5



INPUT PULSE REQUIREMENTS:

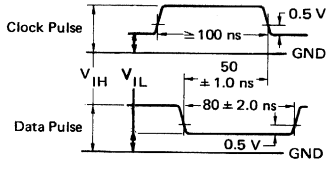
V_{IL} = 0.200 V max
V_{IH} = 0.894 V min. 1.500 V max
t ≤ 10 ns
t ≤ 10 ns
f = 1.0 MHz typ

NOTE:
Measurements for output voltages should be taken at least 100 ns after pulses have occurred.

MC920

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+800 ± 2.0 mVdc
−55°C	+650 ± 2.0 mVdc	+985 ± 2.0 mVdc
+125°C	+260 ± 2.0 mVdc	+605 ± 2.0 mVdc

FIGURE 6



INPUT PULSE REQUIREMENTS:

V_{IL} = 0.200 V max
V_{IH} = 0.894 V min, 1.500 V max
t ≤ 10 ns
t ≤ 10 ns
f = 1.0 MHz typ

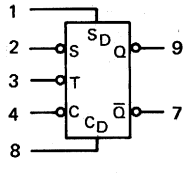
SEQUENCE OF EVENTS:

A. Apply all dc biases required.
B. Apply momentary ground to pin indicated. This sets the flip-flop. Momentary ground must occur before the pulses shown above every time, or the flip-flop will toggle to the wrong condition every alternate pulse.
C. After momentary ground has been released, apply pulses marked above.
D. Measure voltage of designated output after the pulse measurements for output voltages should be taken at least 100 ns after pulses have occurred.

MC922 • MC822

Available in TO-100 Metal Can, Add G Suffix
Available in TO-91 Flat Package, Add F Suffix

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



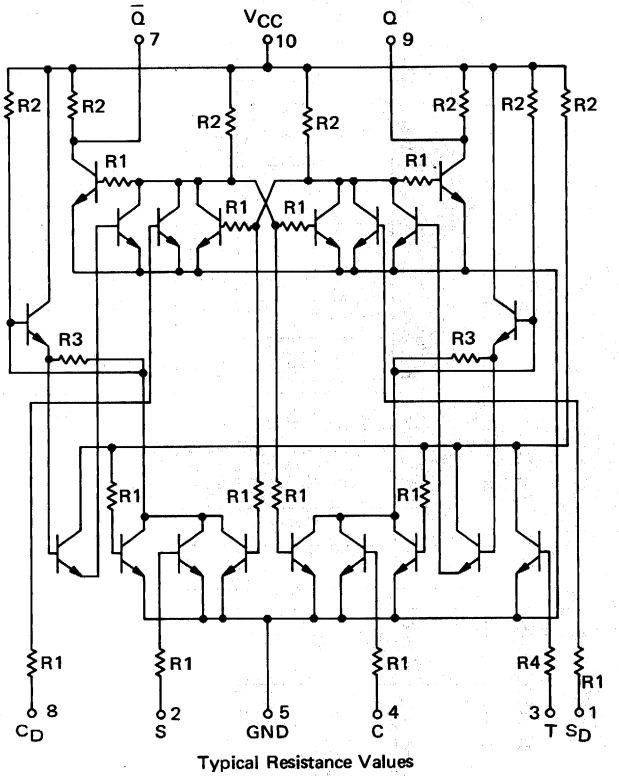
CLOCKED INPUT OPERATION

t_n		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	③	③
1	0	1	0
0	1	0	1
1	1	0	0

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n, and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.



Typical Resistance Values

R1 = 1.5 k R3 = 2.0 k
R2 = 3.6 k R4 = 750

F Package And G Package Pin-Outs Are The Same

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC922	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC822	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

ELECTRICAL CHARACTERISTICS

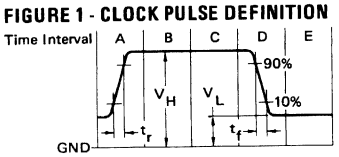
Characteristic	Symbol	Pin Under Test	MC922 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC822 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	1	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	1	-	-	-	10	5
	I_{in}	2	-	125	-	130	-	110		-	150	-	140	-	140		2	-	8	-		
	$2\ I_{in}$	3	-	250	-	260	-	220		-	300	-	280	-	280		3	-	2, 4	-		
	I_{in}	4	-	125	-	130	-	110		-	150	-	140	-	140		4	-	1	-		
	I_{in}	8	-	125	-	130	-	110		-	150	-	140	-	140		8	-	-	-		
Output Current	I_{A4}	7	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	-	7, 1	8	-	10	5
		9	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	-	8, 9	1	-	10	5
Saturation Voltage	$V_{CE(sat)}$	7	-	220	-	222	-	220	mVdc	-	250	-	250	-	250	mVdc	-	1	-	8	10	5
		7*#	-		-		-			-		-		-			-	2	-	4		
		7*#	-		-		-			-		-		-			-	-	-	2, 4		
		7§*	-		-		-			-		-		-			-	2, 4	-	-		
		9	-		-		-			-		-		-			-	8	-	1		
		9§*	-		-		-			-		-		-			-	4	-	2		
		9*#	-		-		-			-		-		-			-	2, 4	-	-		
		9§*	-		-		-			-		-		-			-	-	-	2, 4		

§ Pin 1 = High
# Pin 8 = High
} Set by momentary application of V_{BOT} prior to the negative going clock pulse.

* Pin 3 = Clock pulse to pin 3 (see Figure 1).

Pins not listed are left open.

FIGURE 1 - CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $<1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

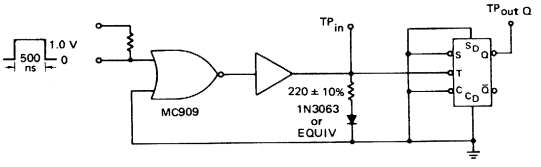
MC822

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+850 ± 2.0 mVdc
0°C	+500 ± 2.0 mVdc	+900 ± 2.0 mVdc
+75°C	+400 ± 2.0 mVdc	+760 ± 2.0 mVdc

MC922

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+800 ± 2.0 mVdc
−55°C	+650 ± 2.0 mVdc	+985 ± 2.0 mVdc
+125°C	+260 ± 2.0 mVdc	+605 ± 2.0 mVdc

FIGURE 2 - TOGGLE MODE TEST CIRCUIT



f = 4.0 MHz
Duty Cycle = 25% to 75%
t_r & t_f < 10 ns

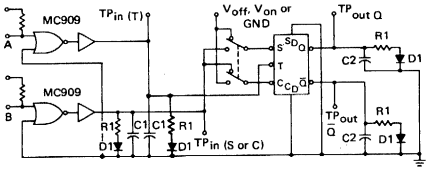
NOTE:
Waveform at the output test point should be ½ the frequency of the waveform at the input test point.

SWITCHING TIMES

Test	Figure No. 3	Maximum (ns)
t_{T-Q-}	3B	150
$t_{T-\bar{Q}-}$	3B	150
t_{T-Q+}	3B	100
$t_{T-\bar{Q}+}$	3B	100
t_{S+T-}	3C	50
t_{S-T-}	3C	30
t_{C+T-}	3C	50
t_{C-T-}	3C	30
t_{T-S+}	3C	0
t_{T-S-}	3C	+5
t_{T-C+}	3C	0
t_{T-C-}	3C	+5
$t_{C_D+\bar{Q}-}$	4	140
$t_{C_D+\bar{Q}+}$	4	70
$t_{S_D+\bar{Q}+}$	4	140
t_{S_D+Q-}	4	70

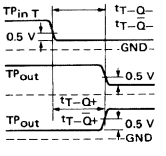
SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS

FIGURE 3A - SET-UP, RELEASE AND SWITCHING TIMES TEST CIRCUIT



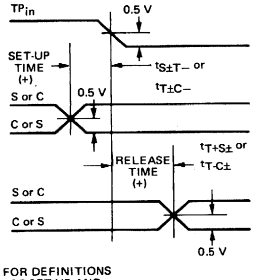
C1 = 20 pF Including Jig and Probe
C2 = 8.0 pF Including Jig and Probe
R1 = 1.5 k ohms ± 1.0%
D1 = 1N3063 or Equivalent

FIGURE 3B - SWITCHING TIME WAVEFORMS



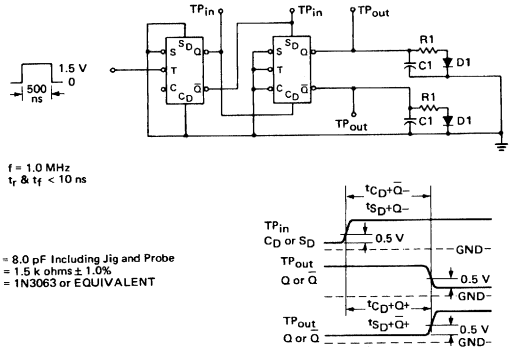
NOTE: Whichever input pin (S or C) is tied to MC909 Buffer on input pin B is at virtual ground when the input is tied to V_{BOT}.

FIGURE 3C - SET-UP AND RELEASE TIME



FOR DEFINITIONS OF SET-UP AND RELEASE TIMES, SEE GENERAL INFORMATION SECTION.

FIGURE 4 - DIRECT SET AND DIRECT CLEAR PROPAGATION DELAY TIME



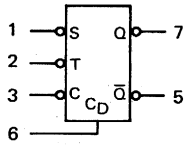
f = 1.0 MHz
t_r & t_f < 10 ns

C1 = 8.0 pF Including Jig and Probe
R1 = 1.5 k ohms ± 1.0%
D1 = 1N3063 or EQUIVALENT

MC982 • MC882

Available in TO-99 Metal Can, Add G Suffix.

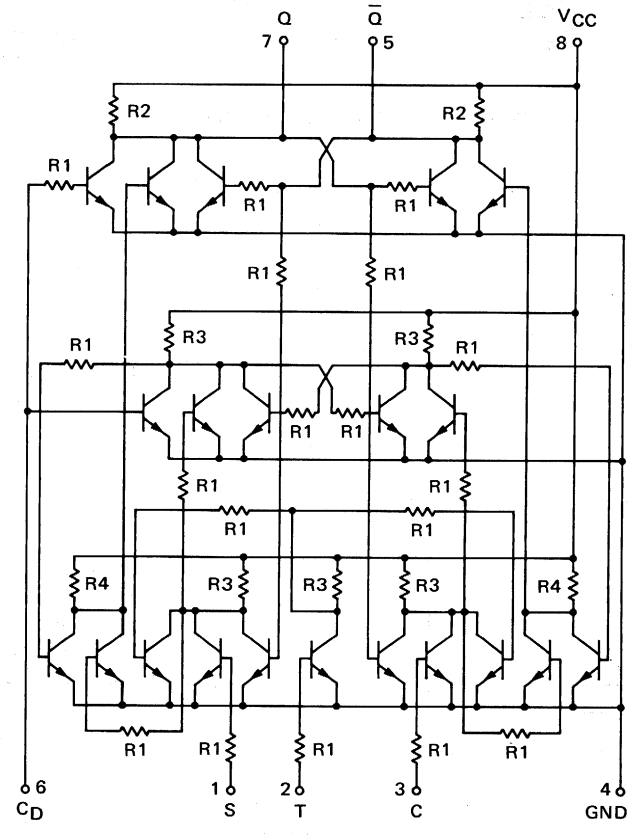
J-K Flip-Flop with a direct clear input in addition to the clocked inputs.



CLOCKED INPUT OPERATION ①

t_n ③		t_{n+1} ②	
S	C	Q	$\overline{Q}$
1	1	Q_n ③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n ④

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 4.5 k
R4 = 7.2 k

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC982	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC882	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC982 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC882 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	1#*	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	-	-	3	-	8	4,6
		2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	2	-	3	-	↓	1,3,4,6
		3*§	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	-	1	-	↓	4,6
	$2\ I_{in}$	6	-	250	-	260	-	220	↓	-	300	-	280	-	280	↓	6	-	2,3,5	-	↓	4
Output Current	I_{A2}	5*†	238	-	247	-	209	-	μAdc	270	-	290	-	255	-	μAdc	-	-	3	-	8	1,4,6
		7*‡	238	-	247	-	209	-	μAdc	270	-	290	-	255	-	μAdc	-	-	1	-	8	3,4,6
Saturation Voltage	$V_{CE(sat)}$	5**Δ	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	1	-	3	8	4,6
		5**Δ	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	-	-	1,3	↓	4,6
		7	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	6	1,2	-	↓	3,4,5
		7**◇	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	1,3	-	-	↓	4
		7**ΔΔ	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	3	-	1	↓	4,6
		7**ΔΔ	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1,3	↓	4,6

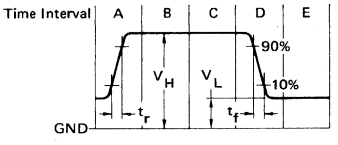
Pins not listed are left open.

* = Pin 2 Clock Pulse a
** = Pin 2 Clock Pulse c
\# = Pin 1 Clock Pulse b
§ = Pin 3 Clock Pulse b
† = Pin 5 Clock Pulse b
‡ = Pin 7 Clock Pulse b (See Figure 4.)

Δ Pin 5 = } Momentary ground prior to negative transition of Clock Pulse c.
ΔΔ Pin 7 = }

◇ Pin 6 = Momentary V_{BOT} prior to negative transition of Clock Pulse c.

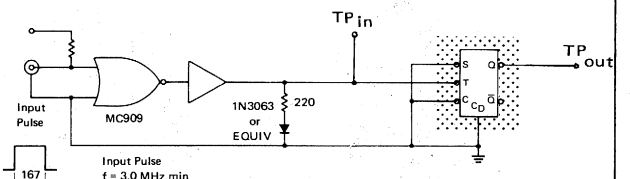
FIGURE 1 - CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be <1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 - TOGGLE MODE TEST CIRCUIT



MC882

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+0.850 ±2.0mVdc
0°C	+500 ± 2.0 mVdc	+0.900 ±2.0mVdc
+75°C	+400 ± 2.0 mVdc	+0.760 ±2.0mVdc

MC982

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+0.800 ±2.0mVdc
−55°C	+650 ± 2.0 mVdc	+0.985 ±2.0mVdc
+125°C	+260 ± 2.0 mVdc	+0.605 ±2.0mVdc

SWITCHING TIME TEST CIRCUITS AND WAVE FORMS

FIGURE 3A

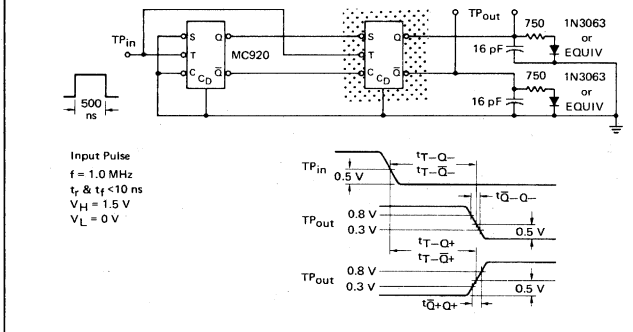
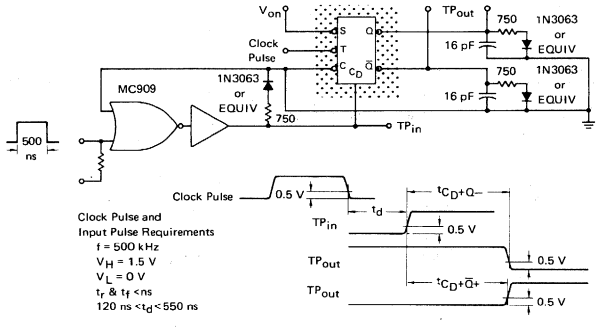


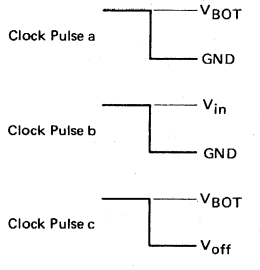
FIGURE 3B



SWITCHING TIMES

Test	Fig. No.	ns @ +25°C min	max
t_{T-Q-}	3A	40	140
t_{T-Q+}	3A	70	195
$t_{T-\overline{Q}-}$	3A	40	140
$t_{T-\overline{Q}+}$	3A	70	195
$t_{\overline{Q}+Q+}$	3A	30	100
$t_{\overline{Q}-Q-}$	3A	5	40
t_{C_D+Q-}	3B	55	--
$t_{C_D+\overline{Q}+}$	3B	5	--

FIGURE 4 - CORRELATION OF CLOCK PULSE a, b, & c

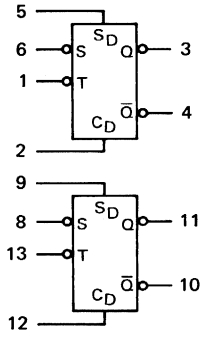


The negative transition of Clock Pulse a must precede the negative transition of Clock Pulse b.

MC978 • MC878

Available in TO-86 Flat Package, Add F Suffix.

The type "D" Flip-Flop is a storage element that stores the state of the S input during negative transitions of the T input. The flip-flop state is not affected by changes in the S input during either the low or the high state of the T input. S_D and C_D inputs may be used for asynchronous operation.



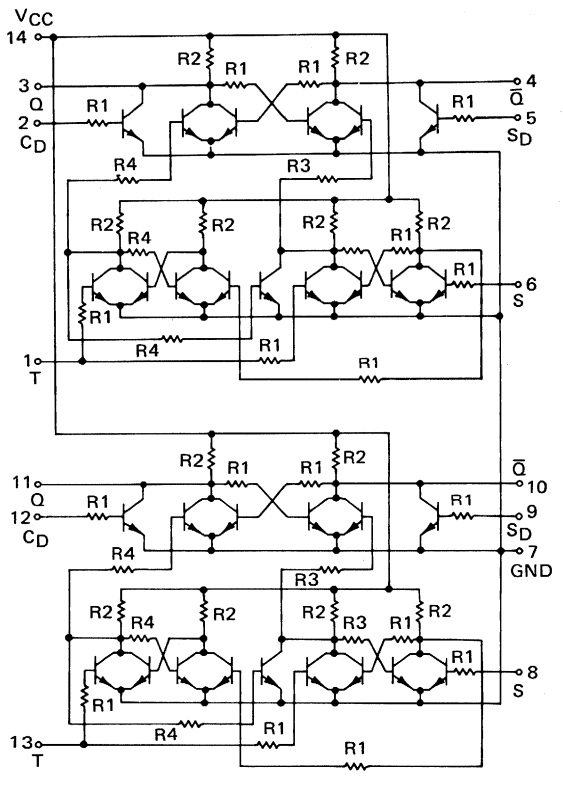
DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	④	④
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ⑤

t_n ③	t_{n+1} ①	
S	Q	$\overline{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_C = C_C = 0$. The output state cannot be predetermined in the case when the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 180
R4 = 480

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

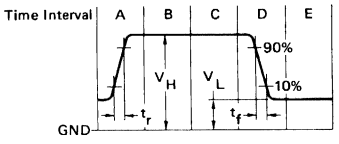
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC978	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC878	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

Characteristic	Symbol	Pin Under Test	MC978 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC878 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Grd
Input Current	$1.8\ I_{in}$	1	-	225	-	234	-	198	μAdc	-	270	-	252	-	252	μAdc	1	-	6	-	14	-	2, 5, 7
	$1.8\ I_{in}$	1	-	225	-	234	-	198		-	270	-	252	-	252		1	-	-	-		-	2, 5, 6, 7
	I_{in}	2#	-	125	-	130	-	110		-	150	-	140	-	140		2	-	-	-		-	5, 6, 7
		5#	-		-		-			-		-		-			5	-	6	-		-	2, 7
		6#	-		-		-			-		-		-			6	-	-	-		-	2, 5, 7
Output Current	I_{A3}	3	350	-	364		308	-	μAdc	420	-	430	-	395	-	μAdc	3	1	5	2	14	-	6, 7
		3#		-		-		-					-		-		3	6	5	2		-	7
		4		-		-		-			-		-		-		4	1	2, 6	5		-	
		4#		-		-		-			-		-		-		4	-	2	5, 6		-	
Output Voltage	V_{out}	3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	1, 5	-	14	-	6, 7
		3	-		-		-			-		-		-			-	4	1	-		-	2, 5, 6, 7
		4	-		-		-			-		-		-			-	5	1, 2	-		-	6, 7
		4	-		-		-			-		-		-			-	3	1	-		-	2, 5, 6, 7
Saturation Voltage	$V_{CE(sat)}$	3	-	220	-	220	-	220	mVdc	-	450	-	400	-	350	mVdc	2	-	1, 5	-	14	-	6, 7
		3	-		-		-			-		-		-			4	-	1	-		-	2, 5, 6, 7
		3*	-		-		-			-		-		-			-	-	1	5		-	6, 7
		3§†	-		-		-			-		-		-			-	-	-	6		-	2, 7
		3#‡	-		-		-			-		-		-			-		5	-		-	2, 7
		4	-		-		-			-		-		-			5	-	1, 2	-		-	6, 7
		4	-		-		-			-		-		-			3	-	1	-		-	2, 5, 6, 7
		4†	-		-		-			-		-		-			-	-	1	2		-	6, 7
		4§*	-		-		-			-		-		-			-	6	-	-		-	5, 7
		4#**	-		-		-			-		-		-			-	-	2	-		-	5, 7
Current Leakage	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	1,2,5,6,7

\# = Pin 1 Clock Pulse a
§ = Pin 1 Clock Pulse b
* = Pin 2 Data Pulse a
** = Pin 6 Data Pulse a
† = Pin 5 Data Pulse a
‡ = Pin 6 Data Pulse b
See Figure 4

Ground inputs of flip-flop not under test. Other pins not listed are left open.

FIGURE 1 - CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\,\mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

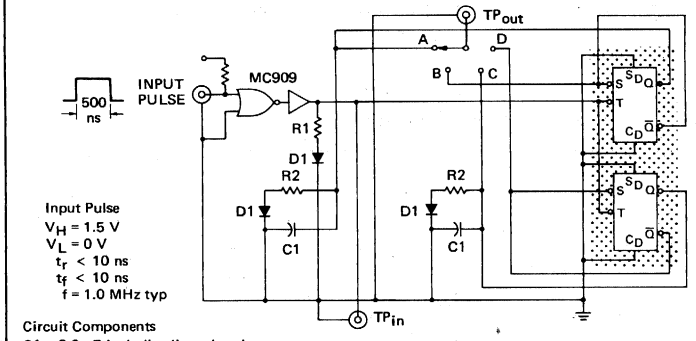
MC878

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+0.850±2.0mVdc
0°C	+500 ± 2.0 mVdc	+0.900±2.0mVdc
+75°C	+400 ± 2.0 mVdc	+0.760±2.0mVdc

MC978

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+0.800 ±2.0 mVdc
−55°C	+650 ± 2.0 mVdc	+0.985 ±2.0 mVdc
+125°C	+260 ± 2.0 mVdc	+0.605 ±2.0 mVdc

FIGURE 2 - SWITCHING TIMES TEST AND WAVEFORMS



Input Pulse
V_H = 1.5 V
V_L = 0 V
t_r < 10 ns
t_f < 10 ns
f = 1.0 MHz typ

Circuit Components
C1 = 8.0 pF including jig and probe
R1 = 220 ohms ± 1.0%
R2 = 1.5 k ohms ± 1.0%
D1 = 1N3063 or equivalent

SWITCHING TIMES

TEST	SWITCH	MAXIMUM (ns @ 25°C)
t_{T-Q+}	A	120
t_{T-Q-}	A	80
$t_{T-\overline{Q}+}$	B	120
$t_{T-\overline{Q}-}$	B	80
$t_{T-\overline{Q}+}$	D	120
$t_{T-\overline{Q}-}$	D	80
t_{T-Q+}	C	120
t_{T-Q-}	C	80

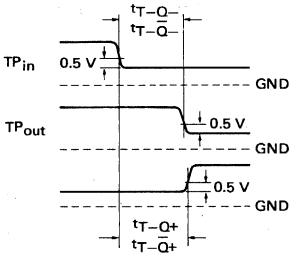
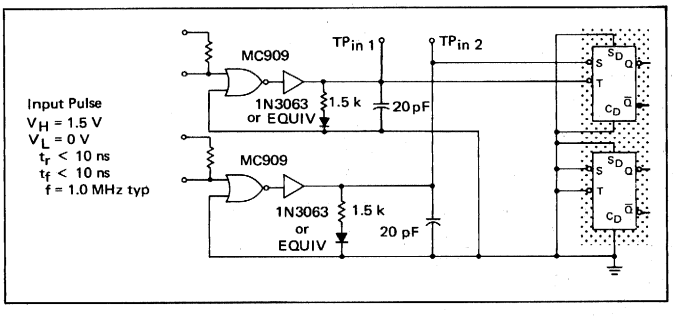


FIGURE 3A - SET UP AND RELEASE TIMES TEST CIRCUIT



Input Pulse
V_H = 1.5 V
V_L = 0 V
t_r < 10 ns
t_f < 10 ns
f = 1.0 MHz typ

FIGURE 3B - INPUT PULSE WIDTHS FOR SET UP AND RELEASE TIMES

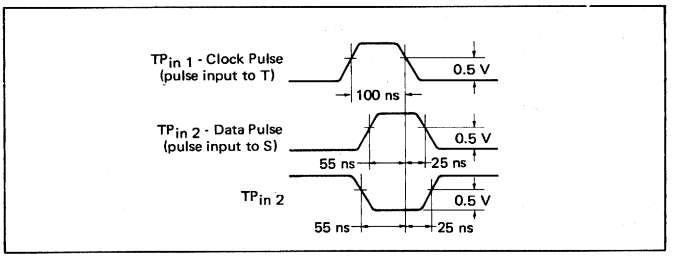
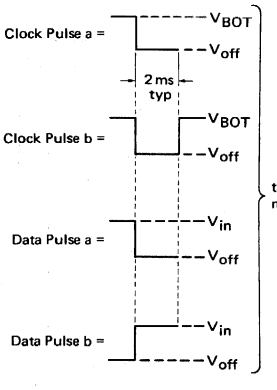


FIGURE 4 - CORRELATION OF CLOCK PULSE a & b AND DATA PULSE a & b

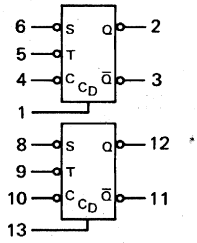


When applicable, the negative transition of Clock Pulse a must precede the transition of Data Pulse a and Data Pulse b. The negative and positive transitions of Clock Pulse b must follow the negative transition of Data Pulse a.

MC976 • MC876

Available in TO-86 Flat Package, Add F Suffix.

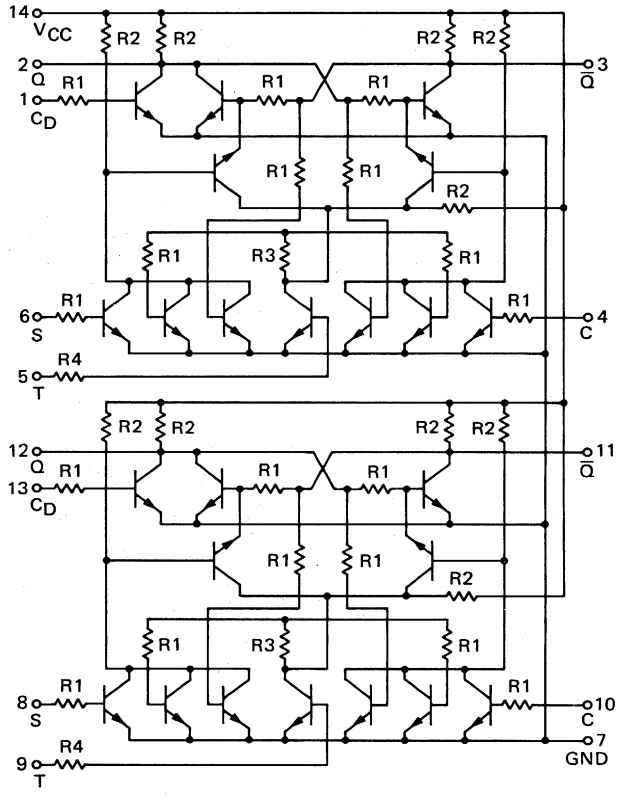
Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



CLOCKED INPUT OPERATION①

t_n ③		t_{n+1} ②	
S	C	Q	$\bar{Q}$
1	1	Q_n ⑤	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ⑥

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.



Typical Resistance Values

R1 = 1.5 k R3 = 3.0 k

R2 = 3.6 k R4 = 750

ELECTRICAL CHARACTERISTICS

Test procedures shown are for one flip-flop only.
The other flip-flop is tested in the same manner.

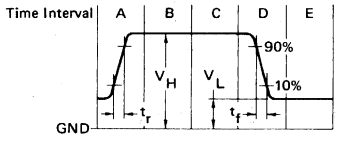
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC976	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC876	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

Characteristic	Symbol	Pin Under Test	MC976 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC876 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	I_{in}	1	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	1	-	3	-	14	-	7
	I_{in}	4	-	125	-	130	-	110	↓	-	150	-	140	-	140	↓	4	-	2	-	↓	-	↓
	$2\ I_{in}$	5	-	250	-	260	-	220	↓	-	300	-	280	-	280	↓	5	-	4, 6	-	↓	-	↓
	I_{in}	6	-	125	-	130	-	110	↓	-	150	-	140	-	140	↓	6	-	3	-	↓	-	↓
Output Current	I_{A2}	2*	270	-	280	-	240	-	μAdc	320	-	320	-	300	-	μAdc	-	2	4	1	14	-	7
		3	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3	1, 6	-	↓	-	↓
		3		-		-		-			-		-		-		-	1, 3	6	-		-	
Output Voltage	V_{out}	2	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	1	-	-	14	-	3, 7
		2**	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	-	7
		2*#	-		-		-			-		-		-			-	4, 6	-	-		-	1, 7
		2*#	-		-		-			-		-		-			-	4	-	6		-	↓
		2*#	-		-		-			-		-		-			-	-	-	4, 6		-	
		3*	-		-		-			-		-		-			-	2	-	-		-	7
		3*#	-		-		-			-		-		-			-	4, 6	-	-		-	1, 7
		3**#	-		-		-			-		-		-			-	6	-	4		-	
		3**#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	4, 6	↓	-	↓
Saturation Voltage	$V_{CE(sat)}$	2	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	-	1	-	14	-	3, 7
		2**	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	-	7
		3*	-		-		-			-		-		-			-	-	-	1		-	7
Current Leakage	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	1,4,5,6,7

\# = Clock Pulse to Pin 5, see Figure 1.
* = Pin 3 Low
** = Pin 2 Low
Set by a momentary ground prior to the application of the negative-going clock pulse.

Ground inputs of flip-flop not under test. Other pins not listed are left open.

FIGURE 1 - CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be < 1.0 µs
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

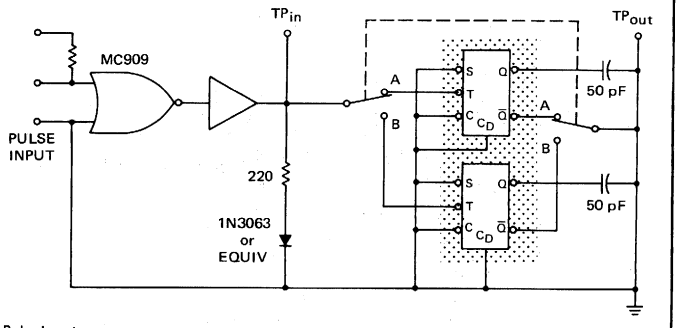
MC876

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+0.850 ±2.0mVdc
0°C	+500 ± 2.0 mVdc	+0.900 ±2.0mVdc
+75°C	+400 ± 2.0 mVdc	+0.760 ±2.0mVdc

MC976

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+0.800±2.0mVdc
−55°C	+650 ± 2.0 mVdc	+0.985 ±2.0mVdc
+125°C	+260 ± 2.0 mVdc	+0.605±2.0mVdc

FIGURE 2 - TOGGLE MODE TEST CIRCUIT



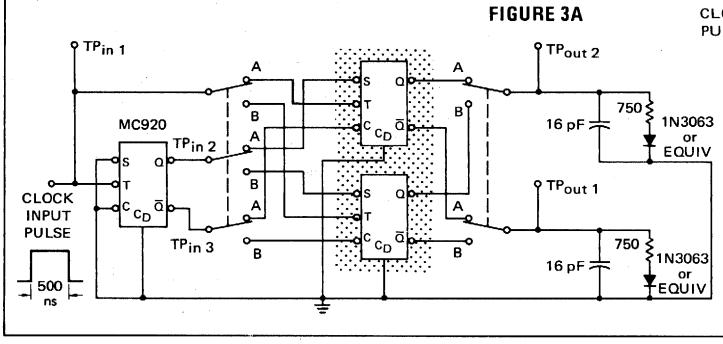
Pulse Input
f = 3.0 MHz
Duty Cycle = 35% to 65%

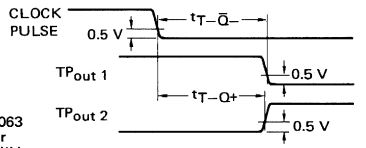
t_r & t_f < 10 ns
V_H = 1.0 V
V_L = 0 V

The circuit should toggle with an output pulse frequency of 1.5 MHz when the duty cycle varies between 35% and 65%.

SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS

FIGURE 3A





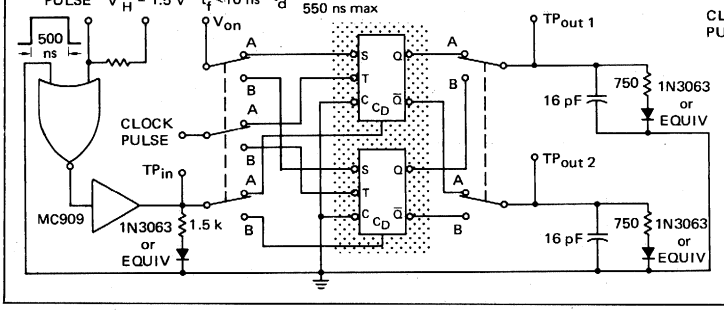
Clock Input Pulse
f = 1.0 MHz
V_H = 1.5 Vdc
V_L = 0 Vdc
t_r < 10 ns
t_f < 10 ns

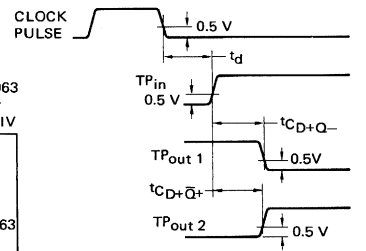
SWITCHING TIMES

TEST	MAXIMUM (ns @+25°C)
$t_{T-\bar{Q}-}$	85
t_{T-Q+}	125
t_{CD+Q-}	65
$t_{CD+\bar{Q}+}$	125

FIGURE 3B

INPUT PULSE V_L = 0 V, V_H = 1.5 V; t_r < 10 ns, t_f < 10 ns; f = 500 kHz typ; t_d = 120 ns min, 550 ns max

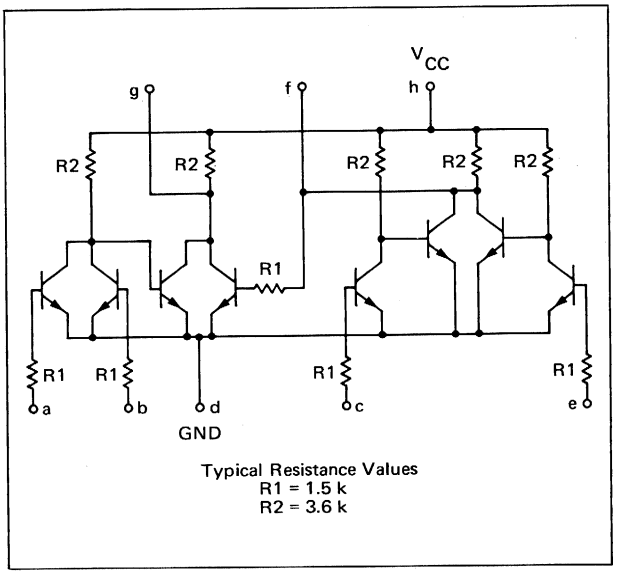




Negative clock pulse transition may cause $\bar{Q}$ to go low for as long as 100 ns.

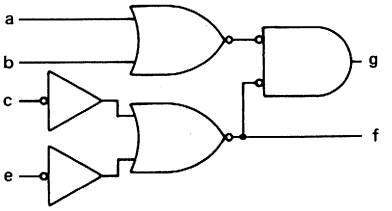
MC908 • MC808

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

The MC908/MC808 is an RTL half-adder. The binary half-adder function can be performed by connecting pin a to pin c and pin b to pin e. The "SUM" is available on pin g while the "CARRY" is available on pin f. The device is also used as a data selector by connecting pin a to pin c and using pins b and e as data inputs. A full adder can be devised by utilizing two MC908/MC808s and one MC911/MC811.

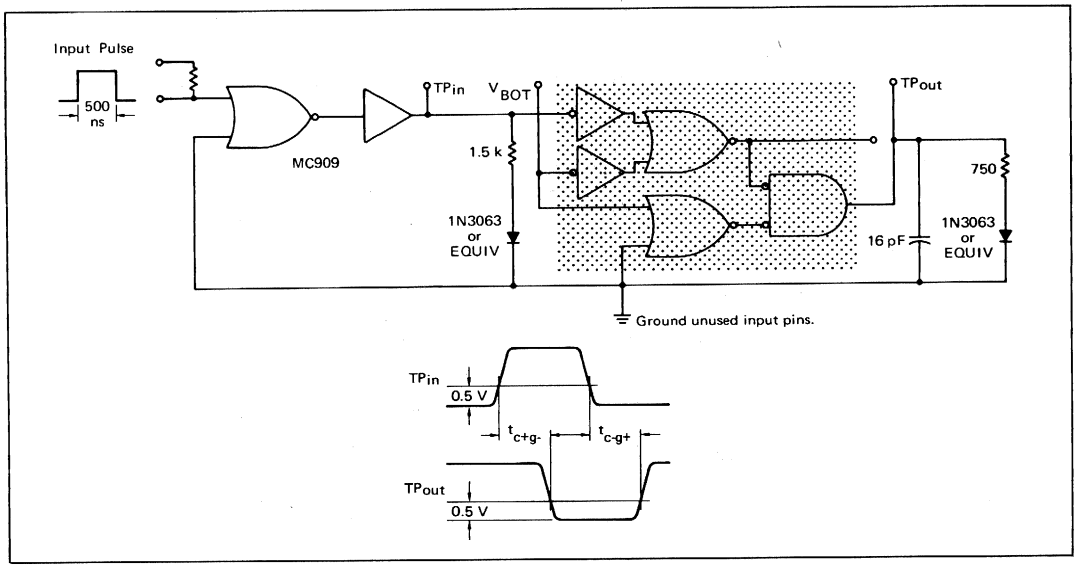


$g = (a + b)(\overline{c} + \overline{e})$

$f = \overline{\overline{c} + \overline{e}}$

PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC908	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC808	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

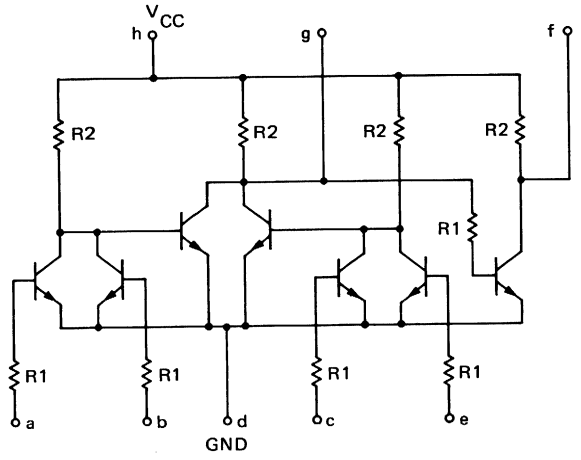
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC908 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC808 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b	-	h	-	c, d, e
		b	-	125	-	130	-	110	↓	-	150	-	140	-	140	↓	b	-	a	-	↓	-	c, d, e
	0.8 I_{in}	c	-	100	-	104	-	88		-	120	-	112	-	112		c	-	-	-		-	a, b, d, e
		e	-	100	-	104	-	88		-	120	-	112	-	112		e	-	-	-			a, b, c, d
Output Current	I_{A3}	f	350	-	364	-	308	-	μAdc	420	-	430	-	395	-	μAdc	f	c, e	-	-	h	-	a, b, d
	I_{A4}	g	475	-	494	-	418	-	↓	570	-	570	-	535	-	↓	g	a	-	c, e	↓	-	b, d
		g	475	-	494	-	418	-		570	-	570	-	535	-		g	b	-	c, e		-	a, d
Output Voltage	V_{out}	g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	f	a, b, c, e	-	h	-	d
Saturation Voltage	$V_{CE(sat)}$	f	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	-	c	e	h	-	a, b, d
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	e	c	↓	-	a, b, d
		g	-		-		-			-		-		-			-	-	-	a, b		-	c, d, e
		g	-		-		-			-		-		-			f	-	a, b, c, e	-		-	d
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	h	a, b, c, d, e
																	Pulse In	Pulse Out					
Switching Time	t	c-g+	-	-	-	80	-	-	ns	-	-	-	80	-	-	ns	c	g	b, e	-	h	-	a, d
		c+g-	-	-	-	100	-	-	ns	-	-	-	100	-	-	ns	c	g	b, e	-	h	-	a, d

Input pins not listed are left open.

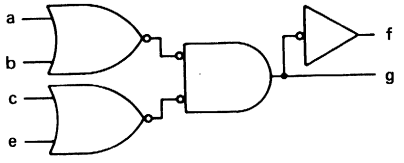
MC912 • MC812

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

The MC912/MC812 is an RTL Half-Adder. By applying the complement of pins a and b to pins c and e, the "SUM" and "NOT SUM" functions of a binary half-adder are produced on pin g and f respectively.

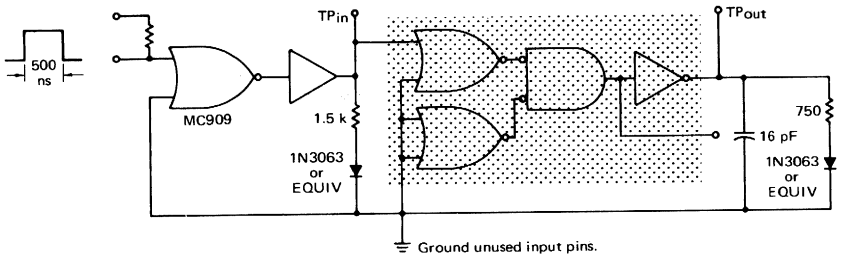


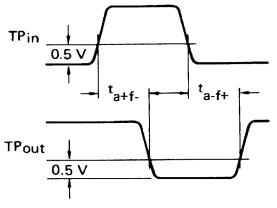
$f = \overline{a} \cdot \overline{b} + \overline{c} \cdot \overline{e}$

$g = (a + b)\,(c + e)$

PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





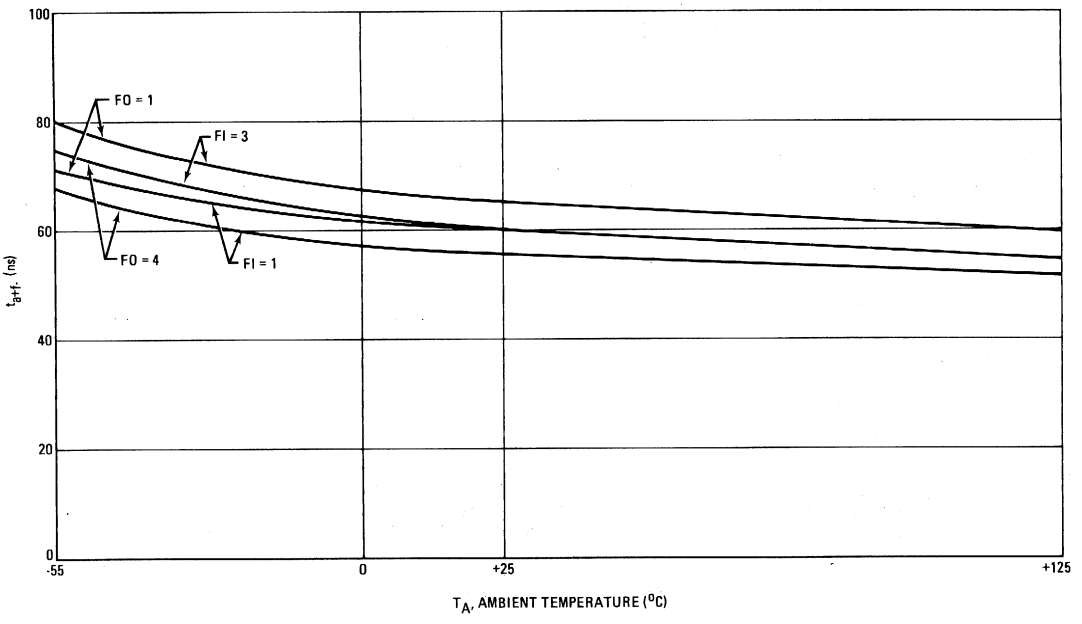
ELECTRICAL CHARACTERISTICS

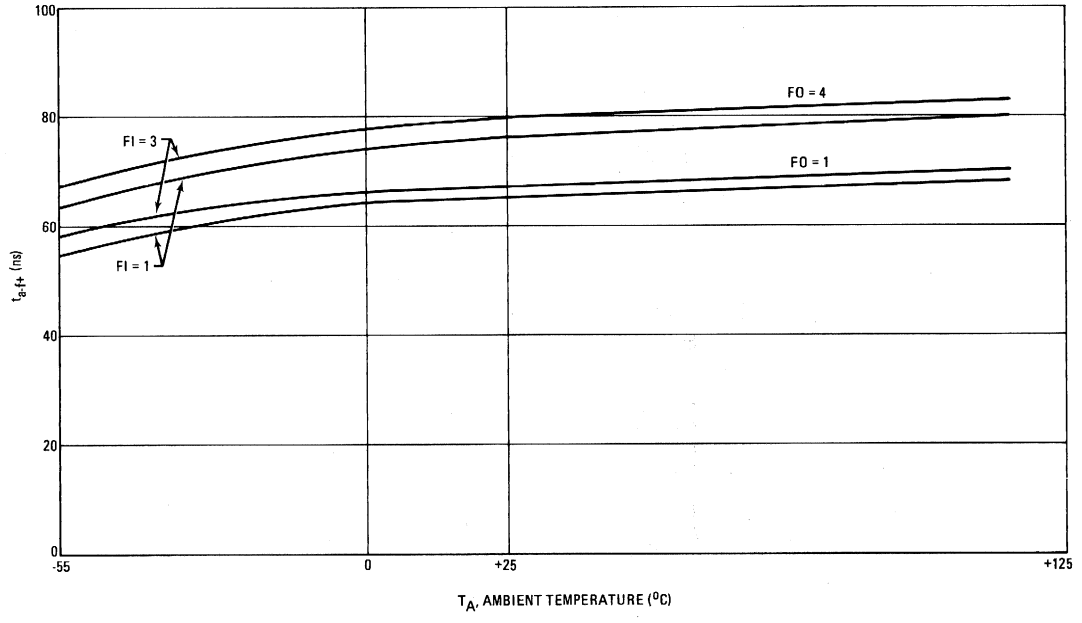
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC912	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC812	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

Characteristic	Symbol	Pin Under Test	MC912 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC812 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b	-	h	-	c, d, e
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a	-	↓	-	c, d, e
		c	-		-		-			-		-		-			c	-	e	-		-	a, b, d
		e	-		-		-			-		-		-			e	-	c	-		-	a, b, d
Output Current	I_{A3}	g	350	-	364	-	308	-	μAdc	420	-	430	-	395	-	μAdc	g	a, c	-	-	h	-	b, d, e
	I_{A3}	g	350	-	364	-	308	-	↓	420	-	430	-	395	-	↓	g	b, e	-	-	↓	-	a, c, d
	I_{A4}	f	475	-	494	-	418	-		570	-	570	-	535	-		f	-	-	-		-	a, b, c, d, e
Output Voltage	V_{out}	f	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	g	a, b, c, e	-	h	-	d
Saturation Voltage	$V_{CE(sat)}$	f	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	g	-	a, b, c, e	-	h	-	d
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	c, e	a, b	↓	-	
		g	-		-		-			-		-		-			-	-	a, b	c, e		-	↓
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	h	a, b, c, d, e
																	Pulse In	Pulse Out					
Switching Time	t	a+f-	-	-	-	100	-	-	ns	-	-	-	100	-	-	ns	a	f	e	-	h	-	b, c, d
		a-f+	-	-	-	80	-	-	ns	-	-	-	80	-	-	ns	a	f	e	-	h	-	b, c, d

Input pins not listed are left open.

PROPAGATION DELAY versus TEMPERATURE

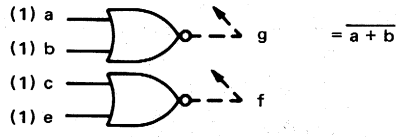




MC921 • MC821

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.

This gate expander is designed to increase the fan-in capability of the gates in the mW MRTL line.



$= \overline{a + b}$

t_{pd} = 27 ns typ

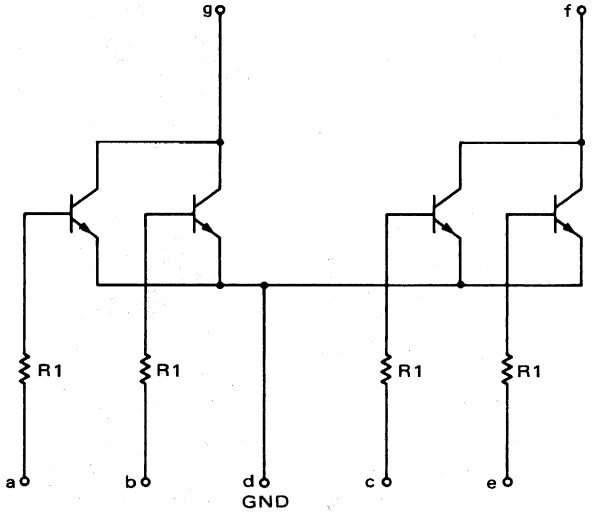
P_D = 3.0 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES mW MRTL LOADING FACTOR

NOTES ON USE OF THE MC921/MC821

1. The input loading factor of the expanded gate is 1.33.
2. Pin h of the expander must be connected to V_{CC}.
3. The output loading factor of the expanded gate is decreased 0.5 load for every added node.

PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10



Typical Resistance Value
R1 = 1.5 k

ELECTRICAL CHARACTERISTICS

Test procedures shown are for one expander only.
Other expanders are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(k ohms) V_{RH}*	V_{RL}*
MC921	−55°C	0.970	0.935	1.80	0.650	3.00	4.27	2.8
	+25°C	0.805	0.750	1.80	0.450	3.00	4.3	2.7
	+125°C	0.590	0.555	1.80	0.260	3.00	5.0	3.0
MC821	0°C	0.880	0.850	1.80	0.500	3.60	4.3	2.7
	+25°C	0.830	0.800	1.80	0.460	3.60	4.3	2.7
	+75°C	0.740	0.710	1.80	0.400	3.60	4.7	2.8

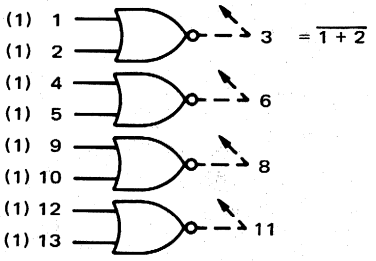
Characteristic	Symbol	Pin Under Test	MC921 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC821 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{RH}*	V_{RL}*	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b	-	h	g	-	d
		b	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	b	-	a	-	h	g	-	d
Output Leakage Current	I_{CEX}	g	-	5.0	-	5.0	-	40	μAdc	-	20	-	20	-	20	μAdc	g	-	-	a, b	h	-	-	d
Output Voltage	$V_{CE(sat)}$	g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	a	-	-	h	-	g	b, d
		g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	b	-	-	h	-	g	a, d
Saturation Voltage	$V_{CE(sat)}$	g	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	a	-	-	-	h	-	g	b, d
		g	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	b	-	-	-	h	-	g	a, d
Isolation Leakage Current	I_L	g	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	g	-	-	a, b, d
		h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	h	-	-	a, b, d

Ground input pins of expander not under test.
Other pins not listed are left open.
*Resistor value to V_{CC}.

MC9921 • MC9821

Available in TO-86 Flat Package, Add F Suffix.

This element consists of four 2-input expanders in a single package to increase the input capability of mW MRTL gates.



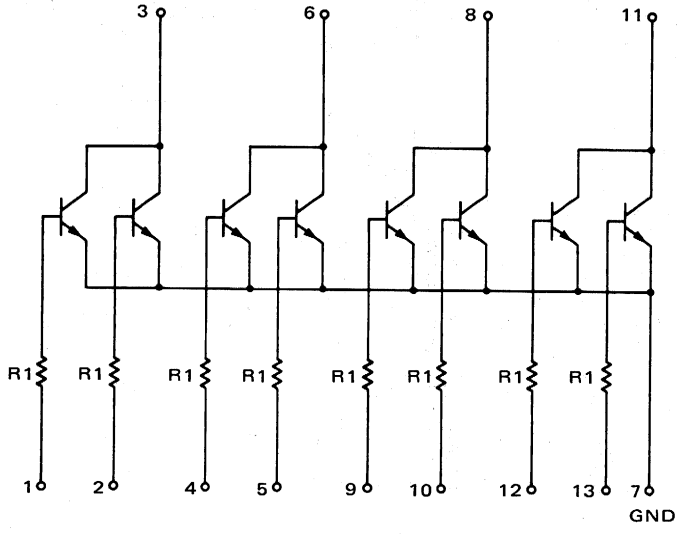
t_{pd} = 27 ns typ

P_D = 20 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES mW MRTL LOADING FACTOR

NOTES ON THE USE OF THE MC9921/MC9821

1. The input loading factor of the expanded gate is 1.33.
2. Pin 14 of the expander must be connected to V_{CC}.
3. The output loading factor of the expanded gate is decreased 0.5 load for every added node.



V_{CC} connection to pin 14 not shown
Typical Resistance Value
R1 = 1.5 k

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(kΩ) V_R*
MC9921	−55°C	0.970	0.935	1.80	0.650	3.00	3.6
	+25°C	0.805	0.750	1.80	0.450	3.00	3.6
	+125°C	0.590	0.555	1.80	0.260	3.00	4.0
MC9821	0°C	0.880	0.850	1.80	0.500	3.60	3.6
	+25°C	0.830	0.800	1.80	0.460	3.60	3.6
	+75°C	0.740	0.710	1.80	0.400	3.60	3.6

ELECTRICAL CHARACTERISTICS

Test procedures shown are for one expander only.
Other expanders are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC9921 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC9821 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	1	-	2	-	14	3	7
		2	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	2	-	1	-	14	3	7
Output Leakage Current	I_{CEX}	3	-	25	-	25	-	30	μAdc	-	40	-	40	-	50	μAdc	3	-	-	1,2	14	-	7
Output Voltage	V_{out}	3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	1	-	-	14	3	2,7
		3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	-	-	14	3	1,7
Saturation Voltage	$V_{CE(sat)}$	3	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	1	-	-	-	14	3	2,7
		3	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	2	-	-	-	14	3	1,7

Ground input pins of expanders not under test.
Other pins not listed are left open.
*Resistor value to V_{CC}.

PLASTIC
MRTL
INTEGRATED CIRCUITS
LOW-POWER
AND
MEDIUM-POWER
MC700P/MC800P SERIES

MILLIWATT AND MEDIUM-POWER
PLASTIC MRTL
INTEGRATED CIRCUITS

This series of MRTL logic circuits is packaged in the molded plastic package to provide exceptional economy. This group contains devices from both the medium-power and low-power groups; the medium-power devices have loading factors normalized for ease of mixing the two power levels in a system.

INDEX

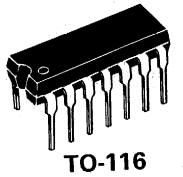
NUMERICAL INDEX
(Functions and Characteristics)

V_{CC} = 3.6 V ± 10%, T_A = 25°C, Case 93

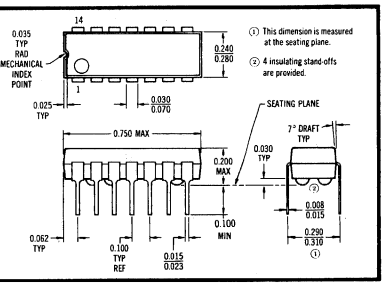
Function	Type		Output Loading Factor each output		Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg ①	Page No.
	+15 to +55°C	0 to +75°C	MC700 Series	MC800 Series			
MRTL							
Dual 3-Input NOR Gate	MC715P	MC815P	16	5	12	55/15	6-174
J-K Flip-Flop		MC816P	–	3	35	91/79 ②	6-202
J-K Flip-Flop	MC723P		10	–	35	91/79 ②	6-202
Quad 2-Input NOR Gate	MC724P	MC824P	16	5	12	100/30	6-180
Dual 4-Input NOR Gate	MC725P	MC825P	16	5	12	60/15	6-176
J-K Flip-Flop	MC726P	MC826P	16	5	35	100/86 ②	6-205
Quad Exclusive OR Gate	MC771P	MC871P	16	5	12	87	6-182
Dual Half Adder	MC775P	MC875P	16	5	20	120	6-227
1 J-K Flip-Flop, 1 Expander, 2 Buffers	MC779P	MC879P	–	–	–	166/169 ③	6-221
Dual Half-Shift Register	MC783P	MC883P	13	4	22	140	6-237
Dual Half-Shift Register w/Inverter	MC784P	MC884P	13	4	22	100	6-235
Quad 2-Input Expander	MC785P	MC885P	–	–	12	20/–	6-215
Dual 4-Input Expander	MC786P	MC886P	–	–	12	20/–	6-213
1 J-K Flip-Flop, 1 Inverter, 2 Buffers	MC787P	MC887P	–	–	–	163/177 ③	6-224
Dual 3-Input Buffer, non inverting	MC788P	MC888P	80	25	24	145/56	6-188
Hex Inverter	MC789P	MC889P	16	5	12	130/15	6-211
Dual J-K Flip-Flop	MC790P	MC890P	10	3	35	182/158 ②	6-208
Dual J-K Flip-Flop	MC791P	MC891P	16	5	40	190/160 ②	6-199
Triple 3-Input NOR Gate	MC792P	MC892P	16	5	12	82/24	6-178
Dual Full Adder	MC796P	MC896P	13	4	60	84	6-229
Dual Full Subtractor	MC797P	MC897P	13	4	60	84	6-232
Dual Buffer	MC799P	MC899P	80	25	20	50/100	6-186
Hex Expander	MC9719P	MC9819P	–	–	12	13/–	6-219
mW MRTL			All Series				
Quad 2-Input NOR Gate	MC717P	MC817P	4		27	20/5.0	6-172
Dual 3-Input NOR Gate	MC718P	MC818P	4		27	12/2.5	6-166
Dual 4-Input NOR Gate	MC719P	MC819P	4		27	13/2.5	6-168
J-K Flip-Flop	MC722P	MC822P	4		70	24/20 ②	6-196
Dual J-K Flip-Flop	MC776P	MC876P	2		50	41/29 ②	6-190
Dual Type D Flip-Flop	MC778P	MC878P	3		60	48/35 ④	6-193
Triple 3-Input NOR Gate	MC793P	MC893P	4		27	18/3.5	6-170
Dual 2-Input Buffer	MC798P	MC898P	30		57	14/46	6-184
Quad 2-Input Expander	MC9721P	MC9821P	–		27	20/–	6-217

① Inputs High/Inputs Low unless otherwise noted.
② Only Clock Input High/Inputs Low
③ Only Clock Input High on flip-flop, other element Inputs High/Inputs Low
④ Direct Set and Direct Clear Low, All Other Inputs High/All Inputs Low

UNIBLOC* PLASTIC PACKAGE CASE 93 TO-116



TO-116



*TRADEMARK OF MOTOROLA INC.

MAXIMUM RATINGS $T_A = 25°C$

Rating	Symbol	Value	Unit
Input Voltage	—	±4.0	Vdc
Power Supply Voltage (Pulsed ≦ 1.0 s)	—	+12	Vdc
Operating Temperature Range MC700P Series MC800P Series	T_A	 +15 to +55 0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

TEST CONDITION TOLERANCES $V_{BOT} = \pm10$ mV $V_{CC} = \pm10$ mV $V_{in} = \pm2$ mV $V_R = \pm1\%$ $V_{on} = \pm2$ mV $V_{off} = \pm2$ mV $V_{LL} = \pm2$ mV

DEFINITIONS

I_{A2}, I_{A3}, I_{A4}, I_{A5}, I_{A10}, I_{A13}, I_{A16} — Minimum available output current from a device with an output loading factor of 2, 3, 4, 5, 10, 13, and 16 respectively. Output voltage not to fall below the value of V_{in}.

I_{AB} — Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.

I_{AM} — The maximum available current from the output of a Dual Gate.

I_{CEX} — Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

I_{in} — Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

1.8 I_{in} — Current drawn from the V_{in} supply by the Toggle pin of the Flip-Flop.

2 I_{in} — Maximum input current drawn by one input of a device with 2 bases internally tied together.

I_L — Isolation leakage current.

I_o — Output load current.

V_{BOT} — A high value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} — Supply voltage.

$V_{CE(sat)}$ — Maximum saturation voltage with V_{BOT} applied to the input.

V_{in} — Minimum high level voltage applied to the input of a device.

V_{LL} — A supply voltage low enough to allow flow of leakage currents only.

V_{off} — The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} — The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} — The maximum output voltage with V_{on} applied to the input.

V_R — Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

GENERAL RULES

- EXPANDER RULES:
  1. The MC785P/885P, MC786P/886P and MC9719P/9819P MRTL expanders can be used to expand medium-power MRTL output nodes only. The MC9721P/9821P expander can be used to expand mW MRTL output nodes only.
  2. mW MRTL and MC800 MRTL Series: When using the MC885P, MC886P, MC9819P or MC9721/9821 subtract 0.5 from the output loading factor of the expanded gate for each expander node that is connected; also increase the input loading factor of the expanded gate by a factor of 1.33.
  3. MC700 MRTL Series: When using the MC785P, MC786P or MC9719P subtract 2.0 from the output loading factor of the medium-power MRTL expanded gate for each expander node that is connected; also increase the input loading factor of the medium-power expanded gate by a factor of 3.75.
- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- When mixing MRTL and mWMRTL in the same system, the loading factors must be normalized in accordance with the input current of the units being driven.
- All unused inputs should be returned to ground.

LOW POWER mW MRTL DEVICES

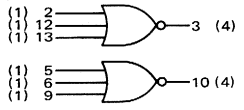
The logic diagrams shown describe the MC700P/MC800P Series of low-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (if on the circuit input terminal) or load driving ability – fan-out – (if on the circuit output terminal).

Using the indicated loading factors, these low-power mW MRTL circuits are compatible with the medium-power MRTL circuits shown on page 6-162. The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C for the MC700P Series, and 0 to +75°C for the MC800P Series, with V_{CC} = 3.6 V ±10%.

All elements in the MC700P/MC800P Series operate with V_{CC} applied to pin 11 and ground connected to pin 4.

GATES

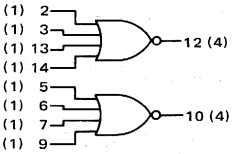
MC718P • MC818P
Dual 3-Input Gate



$3 = \overline{2 + 12 + 13}$

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5 mW (Inputs Low)

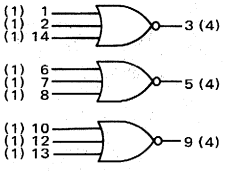
MC719P • MC819P
Dual 4-Input Gate



$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 27 ns
P_D = 13 mW (Input High)
2.5 mW (Inputs Low)

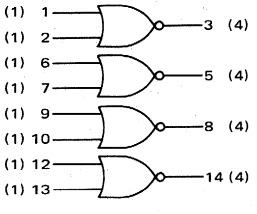
MC793P • MC893P
Triple 3-Input Gate



$3 = \overline{1 + 2 + 14}$

t_{pd} = 27 ns
P_D = 18 mW (Input High)
3.5 mW (Inputs Low)

MC717P • MC817P
Quad 2-Input Gate

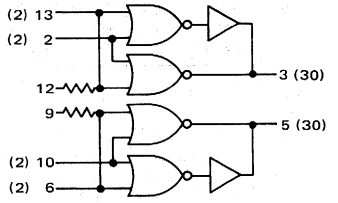


$3 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 20 mW (Input High)
5.0 mW (Inputs Low)

BUFFERS

MC798P • MC898P
Dual 2-Input Buffer

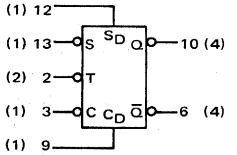


$3 = \overline{2 + 13}$

t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 mW (Inputs Low)

FLIP-FLOPS

MC722P • MC822P
J-K Flip-Flop



f_{Tog} = 1 MHz
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

DIRECT INPUT OPERATION ①

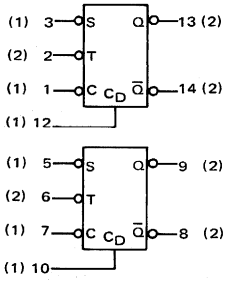
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n ④		t_{n+1} ④	
S	C	Q	$\overline{Q}$
1	1	Q_n ⑤	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n ⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.
6. Clock pulse fall time must be < 100 ns.

MC776P • MC876P
Dual J-K Flip-Flop



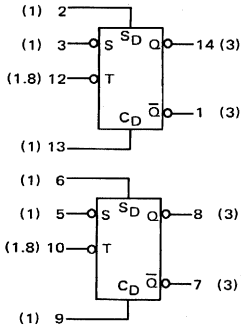
f_{Tog} = 3 MHz
P_D = 41 mW (Only Clock Input High)
29 mW (Inputs Low)

CLOCKED INPUT OPERATION

t_n		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

MC778P • MC878P
Dual Type D Flip-Flop



f_{Tog} = 1 MHz
P_D = 48 mW (Direct Set (S_D) and Direct Clear (C_D) Low; all other Inputs High)
35 mW (All Inputs Low)

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

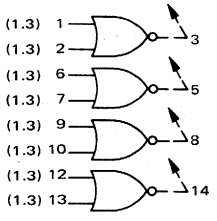
CLOCKED INPUT OPERATION ③

t_n ④	t_{n+1} ④	
S	Q	$\overline{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

EXPANDERS

MC9721P • MC9821P Quad 2-Input Expander



$3 = \overline{1 + 2}$

t_{pd} = 27 ns

P_D = 20 mW (Input High)
Negligible (Inputs Low)

MEDIUM-POWER MRTL DEVICES

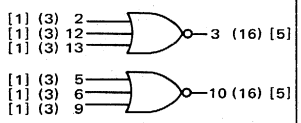
The logic diagrams shown describe the MC700P/MC800P Series of medium-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis or brackets indicates the input loading factor (if on the circuit input terminal) or load driving ability – fan-out – (if on the circuit output terminal). The bracketed number is the loading factor when working with other medium-power devices; e.g., [1] is the MRTL load factor defined as 1 times the MRTL basic gate input current (600 μAdc @ +25°C). The number in parenthesis is the loading factor when working with mW MRTL devices; e.g., (3) is the MRTL load factor defined as 3 times the mW MRTL basic gate input current (140 μAdc @ +25°C.

Using the parenthetic loading factors, these medium-power MRTL circuits are compatible with the low-power mW MRTL circuits shown on page 6-159. The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C for the MC700P Series, and 0 to +75°C for the MC800P Series, with V_{CC} = 3.6 V ±10%.

All elements in the MC700P/800P Series operate with V_{CC} applied to pin 11 and ground connected to pin 4.

GATES

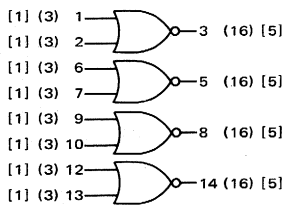
MC715P • MC815P
Dual 3-Input Gate



$3 = \overline{2 + 12 + 13}$

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

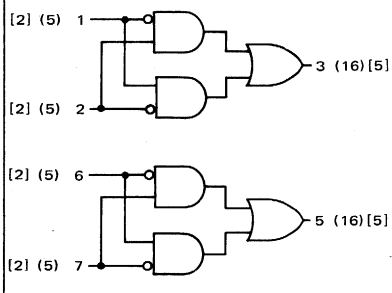
MC724P • MC824P
Quad 2-Input Gate



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 100 mW (Input High)
30 mW (Inputs Low)

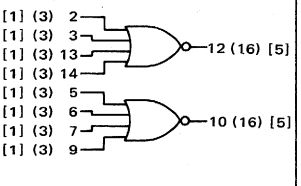
MC771P • MC871P
Quad Exclusive "OR" Gate



$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns
P_D = 87 mW

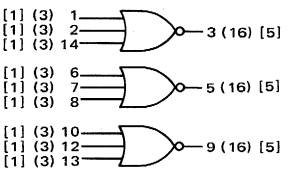
MC725P • MC825P
Dual 4-Input Gate



$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 12 ns
P_D = 60 mW (Input High)
15 mW (Inputs Low)

MC792P • MC892P
Triple 3-Input Gate

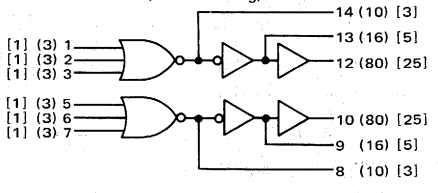


$3 = \overline{1 + 2 + 14}$

t_{pd} = 12 ns
P_D = 82 mW (Input High)
24 mW (Inputs Low)

BUFFERS

MC788P • MC888P Dual 3-Input Buffer
(Non-Inverting)

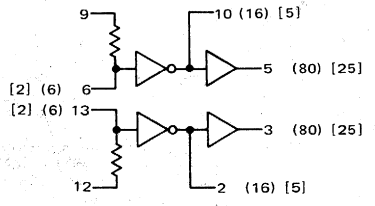


t_{pd} = 24 ns
P_D = 145 mW (Input High)
56 mW (Inputs Low)

$14 = \overline{1 + 2 + 3}$
$13 = 1 + 2 + 3$
$12 = 1 + 2 + 3$

Outputs 12, 13, or 14 may not be used simultaneously.
Outputs 8, 9, or 10 may not be used simultaneously.

MC799P • MC899P Dual Buffer



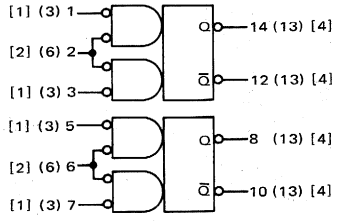
t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

$10 = \overline{6}$
$5 = \overline{6}$

Outputs 2 and 3 may not be used simultaneously.
Outputs 5 and 10 may not be used simultaneously.

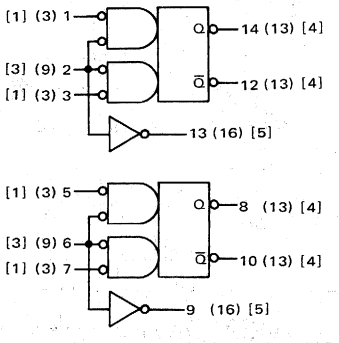
HALF-SHIFT REGISTERS

MC784P • MC884P
Dual Half-Shift Register
(Without Inverter)



$14 = \overline{12}\ (1 + 2)$
$12 = \overline{14}\ (3 + 2)$
t_{pd} = 22 ns
P_D = 100 mW

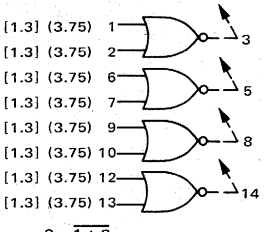
MC783P • MC883P
Half-Shift Register



$14 = \overline{12}\ (1 + 2)$
$12 = \overline{14}\ (3 + 2)$
t_{pd} = 22 ns
P_D = 140 mW

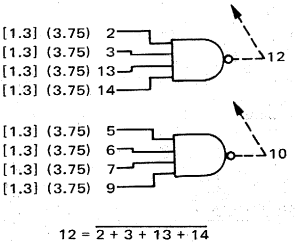
EXPANDERS

MC785P • MC885P
Quad 2-Input Expander



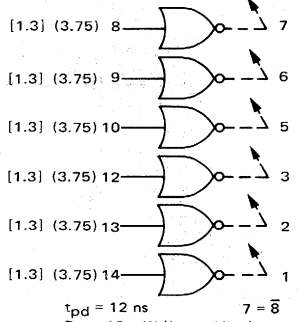
$3 = \overline{1 + 2}$
t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

MC786P • MC886P
Dual 4-Input Expander



$12 = \overline{2 + 3 + 13 + 14}$
t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

MC9719P • MC9819P
Hex Expander



t_{pd} = 12 ns
P_D = 13 mW (Input High)
Negligible (Inputs Low)

$7 = \overline{8}$

FLIP-FLOPS

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

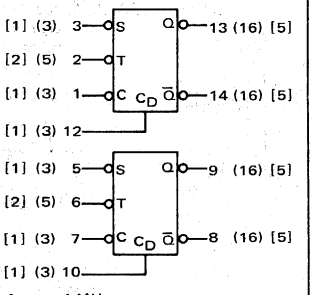
CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1} ④	
S	C	Q	$\bar{Q}$
1	1	Q_n⑤	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n⑤

J-K FLIP-FLOP TRUTH TABLES

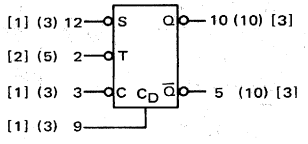
1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.
6. Clock pulse fall time must be < 100 ns.

MC791P • MC891P
Dual J-K Flip-Flop



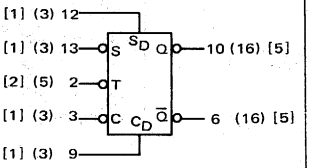
f_{Tog} = 4 MHz
P_D = 190 mW (Only Clock Input High)
160 mW (Inputs Low)

MC723P • MC816P
J-K Flip-Flop



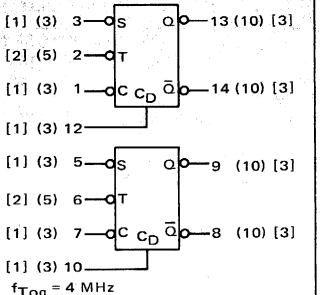
f_{Tog} = 4 MHz
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

MC726P • MC826P
J-K Flip-Flop



f_{Tog} = 4 MHz
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

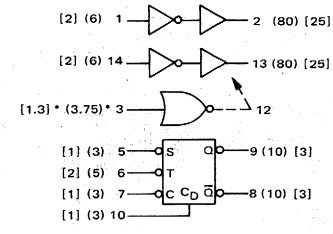
MC790P • MC890P
Dual J-K Flip-Flop



f_{Tog} = 4 MHz
P_D = 182 mW (Only Clock Input High)
158 mW (Inputs Low)

MULTIFUNCTION DEVICES

MC779P • MC879P
Multifunction
(1 J-K FLIP-FLOP, 1 EXPANDER, 2 BUFFERS)

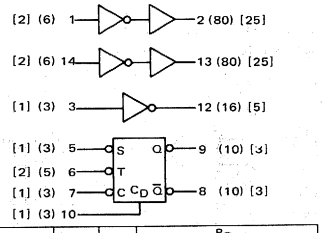


	f_{Tog} MHz	t_{pd} ns	P_D mW (Input High)	P_D mW (Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
EXPANDER	—	12	2.5	Negligible

‡Only Clock Input High

*Input loading factor is 3 for mW MRTL, or 1 for MRTL, if pin 12 is tied to pin 8 or 9 on the same package.

MC787P • MC887P
Multifunction
(1 J-K FLIP-FLOP, 1 INVERTER, 2 BUFFERS)

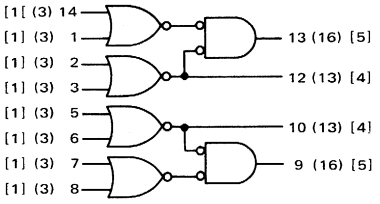


	f_{Tog} MHz	t_{pd} ns	P_D mW (Input High)	P_D mW (Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
INVERTER	—	12	22	8

‡Only Clock Input High

HALF ADDERS

MC775P • MC875P
Dual Half Adder



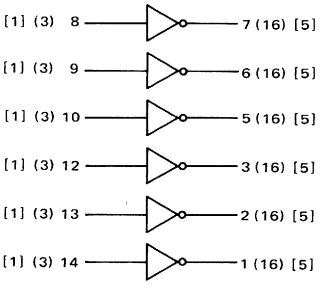
$13 = (14 + 1)(2 + 3)$

$12 = \overline{2 + 3}$

t_{pd} = 20 ns
P_D = 120 mW typ

INVERTER

MC789P • MC889P
Hex Inverter

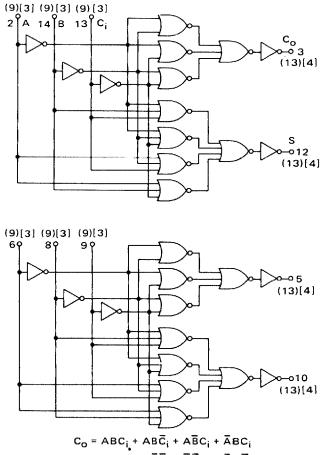


t_{pd} = 12 ns
P_D = 130 mW (Input High)
15 mW (Inputs Low)

$1 = \overline{14}$

FULL ADDER

MC796P • MC896P
Dual Full Adder



$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

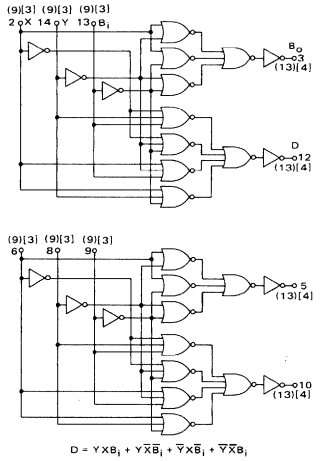
$S = ABC_i + A\overline{B}\,\overline{C_i} + \overline{A}B\overline{C_i} + \overline{A}\overline{B}C_i$

t_{pd} = 60 ns typical
P_D = 84 mW typical

TRUTH TABLE				
Input Logic Level			Output Logic Level	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

MC797P • MC897P
Dual Full Subtractor



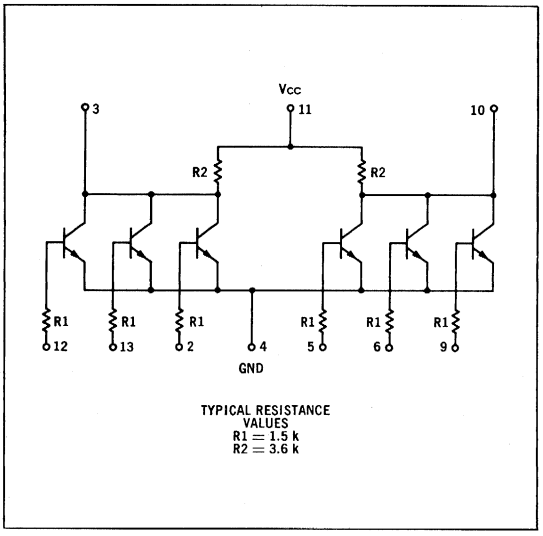
$D = YXB_i + Y\overline{X}\,\overline{B_i} + \overline{Y}X\overline{B_i} + \overline{Y}\,\overline{X}B_i$

$B_o = \overline{Y}\,\overline{X}B_i + Y\overline{X}\,\overline{B_i} + \overline{Y}X\overline{B_i} + YXB_i$

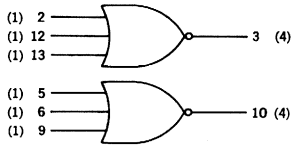
t_{pd} = 60 ns typical
P_D = 84 mW typical

TRUTH TABLE				
Input Logic Level			Output Logic Level	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

MC718P • MC818P



Two 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

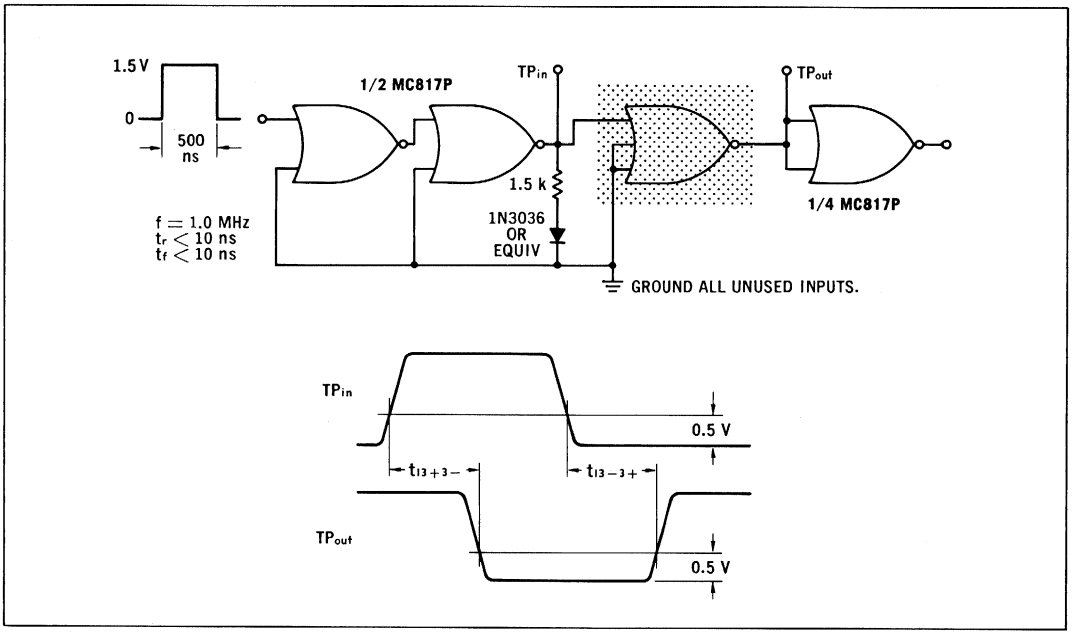


$3 = \overline{2 + 12 + 13}$

NUMBER IN PARENTHESIS INDICATES MC718P, MC818P LOADING FACTOR

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

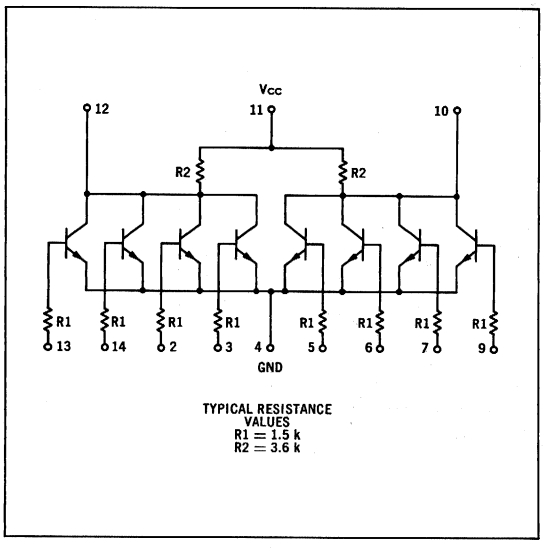
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC818P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC718P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC818P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC718P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	12, 13	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	12	-	2, 13	-	↓	↓
		13	-		-		-			-		-					13	-	2, 12	-		
Output Current	I_{A4}	3	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	3	-	-	2,12,13	11	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	-	↓	2,4,13
		3	-		-		-			-		-		-			-	2	-	-		4,12,13
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	12	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	13	-	↓	2,4,12
		3	-		-		-			-		-		-			-	-	2	-		4,12,13
Switching Time	$t_{on} + t_{off}$	3, 13	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 13	Pulse Out 3	-	-	11	2,4,12

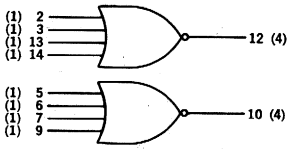
Ground unused input pins. Other pins not listed are left open.

MC719P • MC819P



TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k

Two 4-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

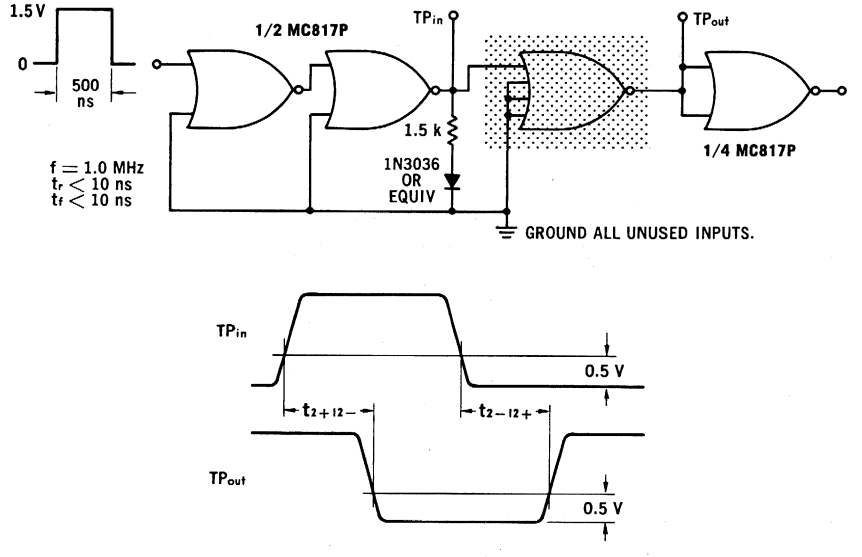


$12 = \overline{2 + 3 + 13 + 14}$

NUMBER IN PARENTHESIS INDICATES MC719P, MC819P LOADING FACTOR

t_{pd} = 27 ns
P_D = 13 mW (Input High)
2.5 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

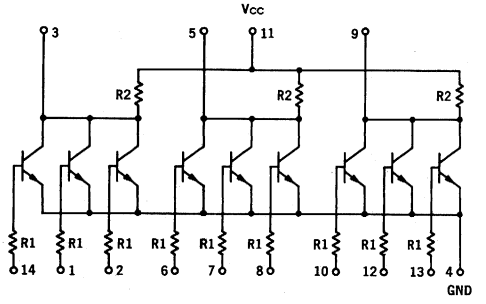
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC819P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC719P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC819P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC719P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	150	-	140	-	140	µAdc	-	150	-	150	-	150	µAdc	2	-	3,13,14	-	11	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,13,14	-	↓	↓
		13	-		-		-			-		-		-			13	-	2, 3, 14	-		
		14	-		-		-			-		-		-			14	-	2, 3, 13	-		
Output Current	I_{A4}	12	570	-	570	-	535	-	µAdc	570	-	570	-	570	-	µAdc	-	12	-	2,3,13, 14	11	4
Output Voltage	V_{out}	12	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	2	-	-		3,4,13,14
		12	-		-		-			-		-		-			-	3	-	-		2,4,13,14
Saturation Voltage	$V_{CE(sat)}$	12	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	13	-	11	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	-	2	-		3,4,13,14
		12	-		-		-			-		-		-			-		3	-		2,4,13,14
Switching Time	$t_{on} + t_{off}$	2, 12	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 2	Pulse Out 12	-	-	11	3,4,13,14

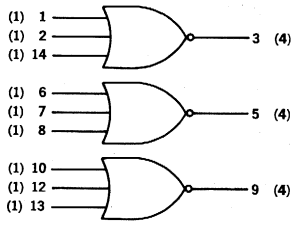
Ground inputs of gate not under test. Other pins not listed are left open.

MC793P • MC893P



TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k

Three 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.

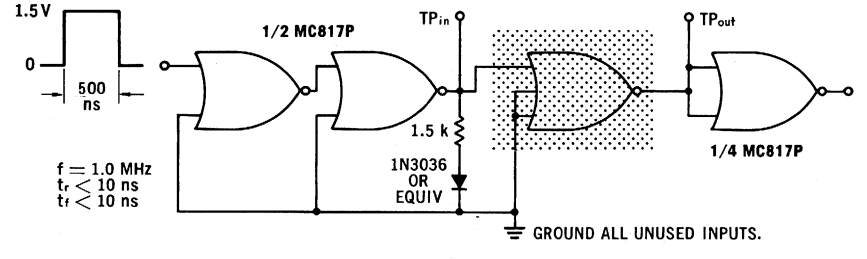


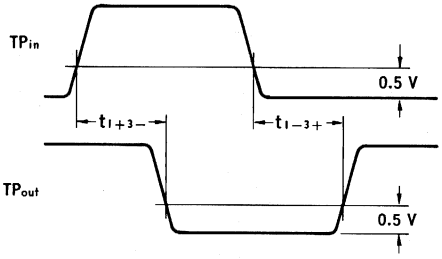
$3 = \overline{1 + 2 + 14}$

NUMBER IN PARENTHESIS INDICATES MC793P, MC893P LOADING FACTOR

t_{pd} = 27 ns
P_D = 18 mW (Input High)
3.5 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

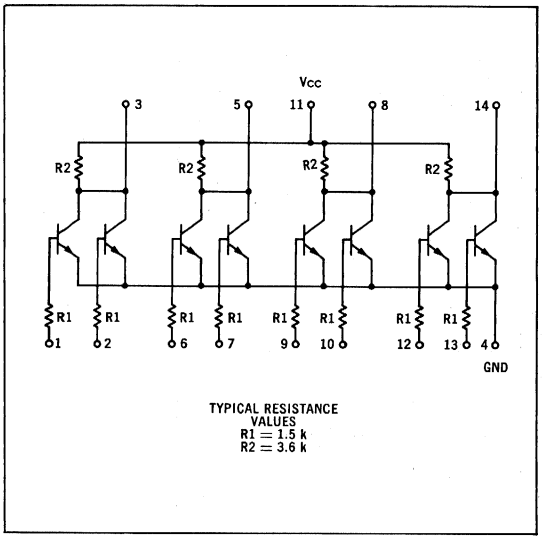
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC893P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC793P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

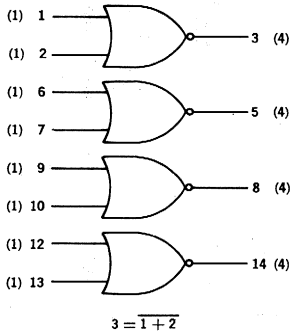
Characteristic	Symbol	Pin Under Test	MC893P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC793P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	2,14	-	11	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1,14	-	↓	↓
		14	-		-		-			-		-		-			14	-	1,2	-		
Output Current	I_{A4}	3	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	-	3	-	1,2,14	11	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	2,4,14
		3	-		-		-			-		-		-			-	2	-	-		1,4,14
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	14	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1	-	↓	2,4,14
		3	-		-		-			-		-		-			-	-	2	-		1,4,14
Switching Time	$t_{on} + t_{off}$	1, 3	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In: 1	Pulse Out: 3	-	-	11	2,4,14

Ground input pins of gates not under test. Other pins not listed are left open.

MC717P • MC817P



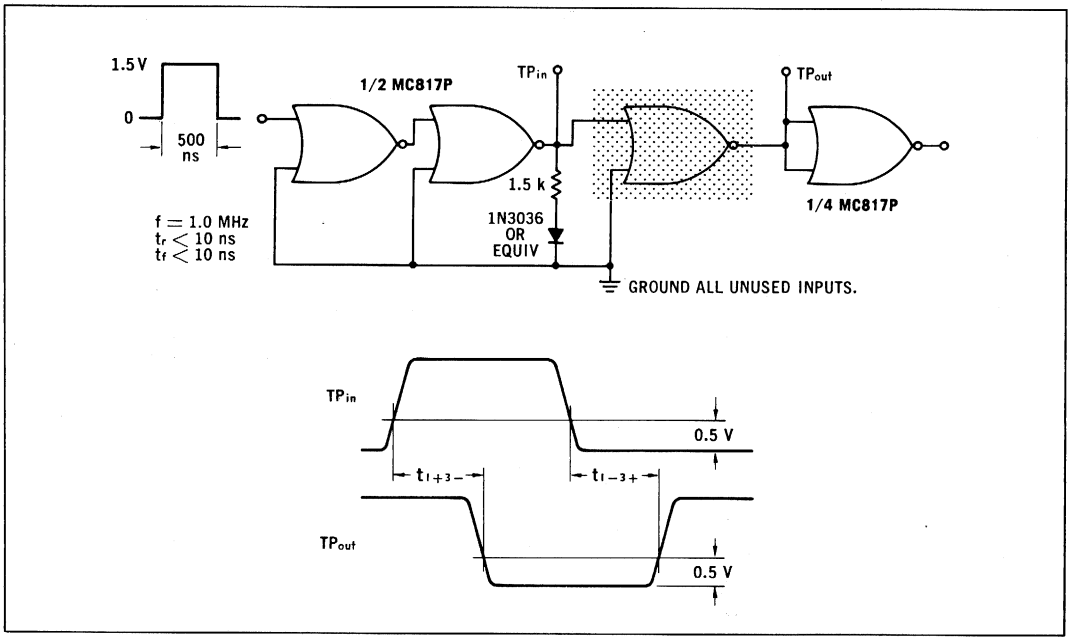
Four 2-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



NUMBER IN PARENTHESIS INDICATES MC717P, MC817P LOADING FACTOR

t_{pd} = 27 ns
P_D = 20 mW (Input High)
5.0 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

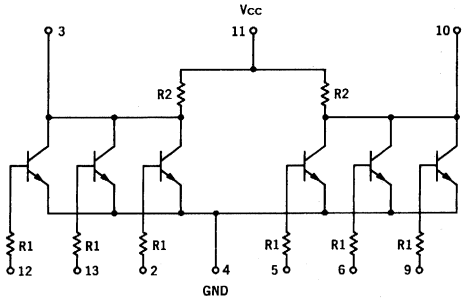
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC817P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC717P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC817P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC717P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	2	-	11	4
		2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	1	-	11	4
Output Current	I_{A4}	3	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	-	3	-	1,2	11	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2,4
		3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	1,4
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	1	-	11	2,4
		3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	-	11	1,4
Switching Time	$t_{on} + t_{off}$	1,3	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 1	Pulse Out 3	-	-	11	2,4

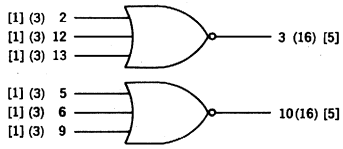
Ground input pins of gates not under test. Other pins not listed are left open.

MC715P • MC815P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

Two 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



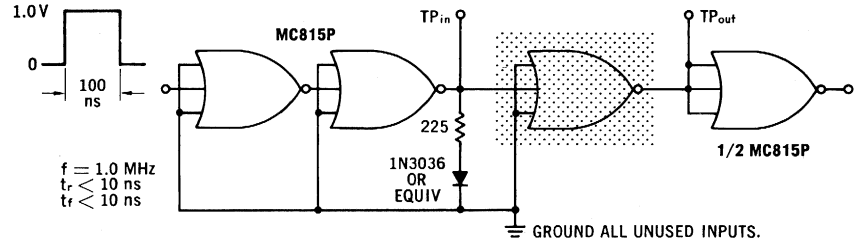
$3 = \overline{2 + 12 + 13}$

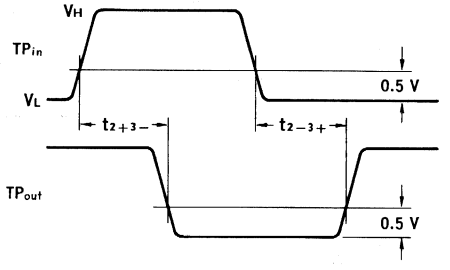
NUMBER IN PARENTHESIS INDICATES MC715P LOADING FACTOR

NUMBER IN BRACKETS INDICATES MC815P LOADING FACTOR

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

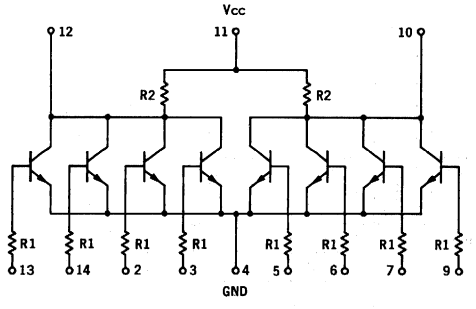
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC815P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC715P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC815P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC715P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	12, 13	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	12	-	2, 13	-	↓	↓
		13	-		-		-			-		-		-			13	-	2, 12	-		
Output Current	I_{A5}*	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	2,12,13	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	-	↓	2,4,12
		3	-		-		-			-		-		-			-	2	-	-		4,12,13
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	12	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	13	-	↓	2,4,12
		3	-		-		-			-		-		-			-	-	2	-		4,12,13
Switching Time	$t_{on} + t_{off}$	3,13	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In 13	Pulse Out 3	-	-	11	2,4,12

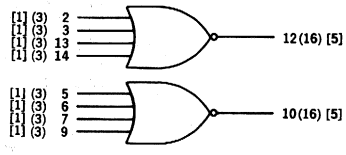
Ground input pins of gate not under test. Other pins not listed are left open. *Symbol is I_{A16} for MC715P.

MC725P • MC825P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

Two 4-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



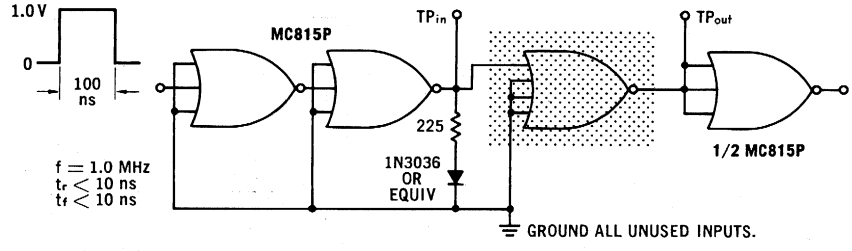
$12 = \overline{2 + 3 + 13 + 14}$

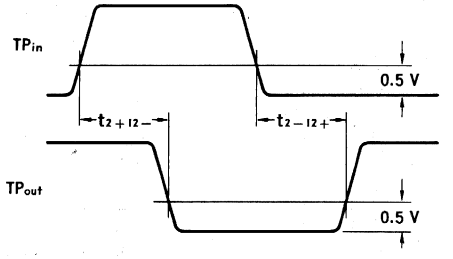
NUMBER IN PARENTHESIS INDICATES MC725P LOADING FACTOR

NUMBER IN BRACKETS INDICATES MC825P LOADING FACTOR

t_{pd} = 12 ns
P_D = 60 mW (Input High)
15 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

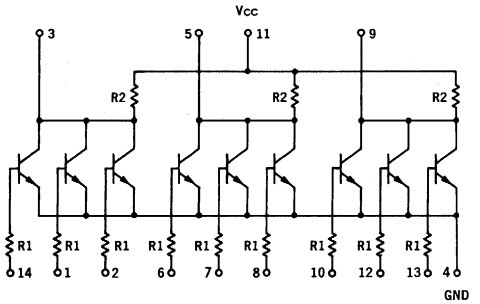
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC825P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC725P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC825P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC725P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	3,13,14	-	11	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,13,14	-	↓	↓
		13	-		-		-			-		-		-			13	-	2,3,14	-		
		14	-		-		-			-		-		-			14	-	2,3,13	-		
Output Current	I_{A5}*	12	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	12	-	2,3,13,14	11	4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-		2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	2	-	-		3,4,13,14
		12	-		-		-			-		-		-			-	3	-	-		2,4,13,14
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	13	-	11	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	-	2	-		3,4,13,14
		12	-		-		-			-		-		-			-	-	3	-		2,4,13,14
Switching Time	$t_{on} + t_{off}$	2, 12	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In 2	Pulse Out 12	-	-	11	3,4,13,14

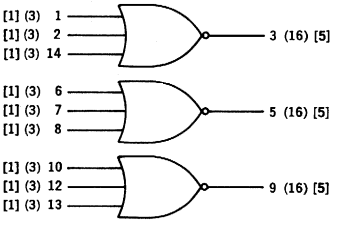
Ground input pins of gate not under test. Other pins not listed are left open. *Symbol is I_{A16} for MC725P.

MC792P • MC892P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

Three 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



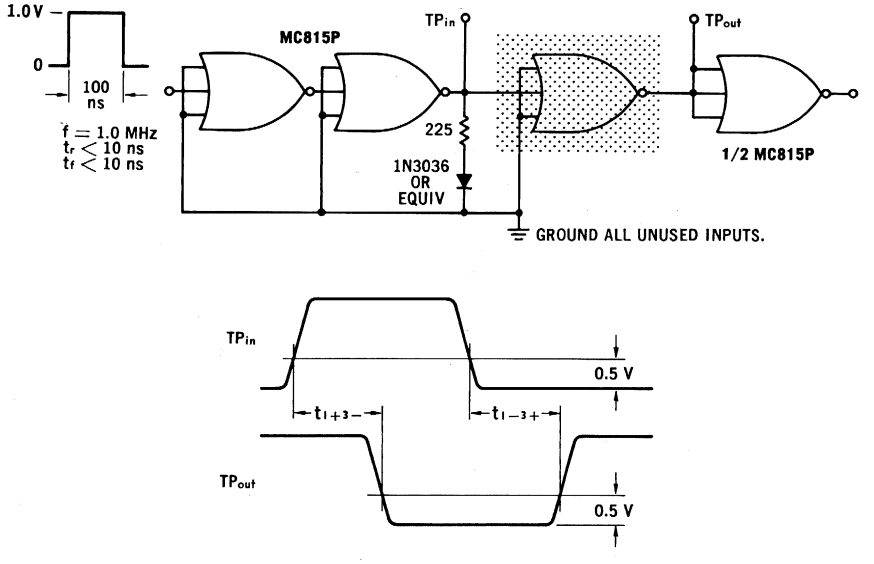
$3 = \overline{1 + 2 + 14}$

NUMBER IN PARENTHESIS INDICATES MC792P LOADING FACTOR.

NUMBER IN BRACKETS INDICATES MC892P LOADING FACTOR.

t_{pd} = 12 ns
P_D = 82 mW (Input High)
24 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

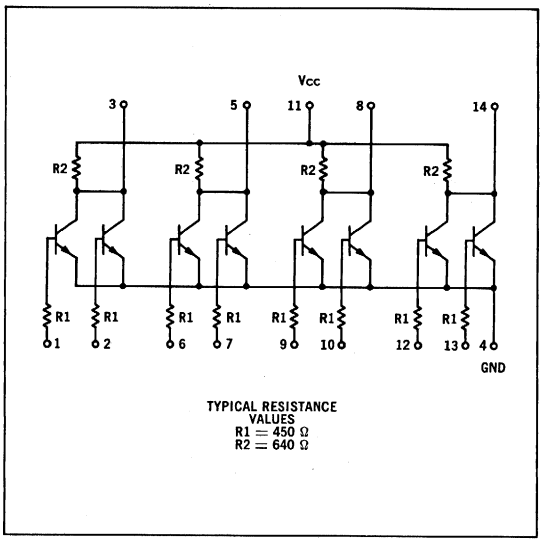
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC892P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC792P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

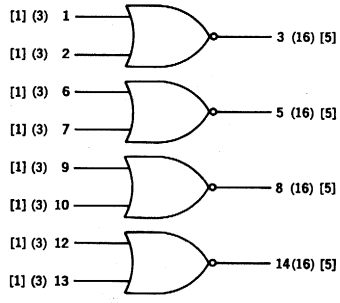
Characteristic	Symbol	Pin Under Test	MC892P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC792P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2,14	-	11	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1,14	-	↓	↓
		14	-		-		-			-		-		-			14	-	1,2	-		
Output Current	I_{A5}*	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	1,2,14	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	2,4,14
		3	-		-		-			-		-		-			-	2	-	-		1,4,14
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1	-	↓	2,4,14
		3	-		-		-			-		-		-			-	-	2	-		1,4,14
Switching Time	$t_{on} + t_{off}$	1,3	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In 1	Pulse Out 3	-	-	11	2,4,14

Ground input pins of gates not under test. Other pins not listed are left open. *I_{A16} is symbol for MC792P.

MC724P • MC824P



Four 2-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.

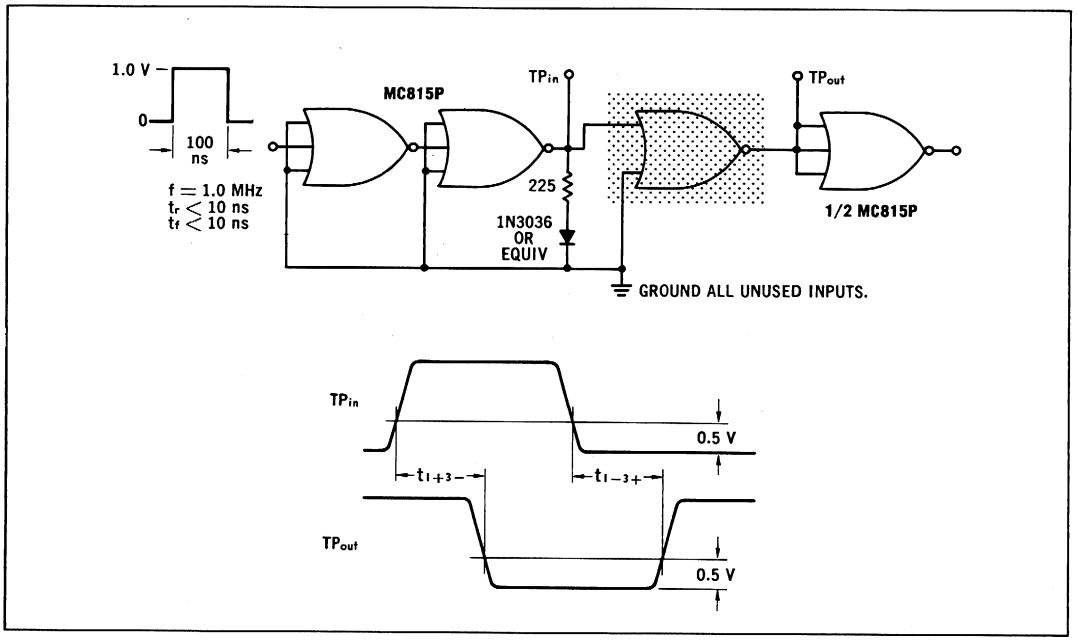


$3 = \overline{1 + 2}$

NUMBER IN PARENTHESIS INDICATES MC724P LOADING FACTOR
NUMBER IN BRACKETS INDICATES MC824P LOADING FACTOR

t_{pd} = 12 ns
P_D = 100 mW (Input High)
30 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

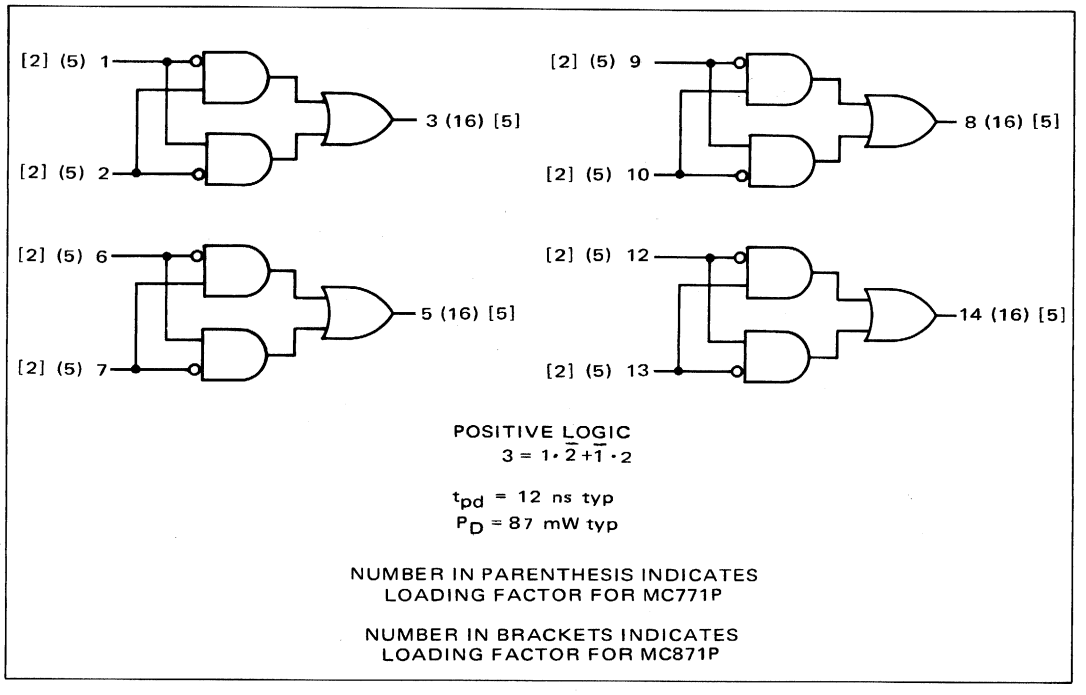
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC824P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC724P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC824P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC724P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	4
		2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	1	-	11	4
Output Current	I_{A5}*	3	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	1,2	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2,4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	1,4
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	2,4
		3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	2	-	11	1,4
Switching Time	$t_{on} + t_{off}$	1,3	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In: 1	Pulse Out: 3	-	-	11	2,4

Ground input pins of gates not under test. Other pins not listed are left open. *I_{A16} is symbol for MC724P.

MC771P · MC871P

Four gate arrays designed to provide the Exclusive OR function. The output is high only if one input is high and all other inputs are low.



POSITIVE LOGIC

$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns typ

P_D = 87 mW typ

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC771P

NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC871P

ELECTRICAL CHARACTERISTICS

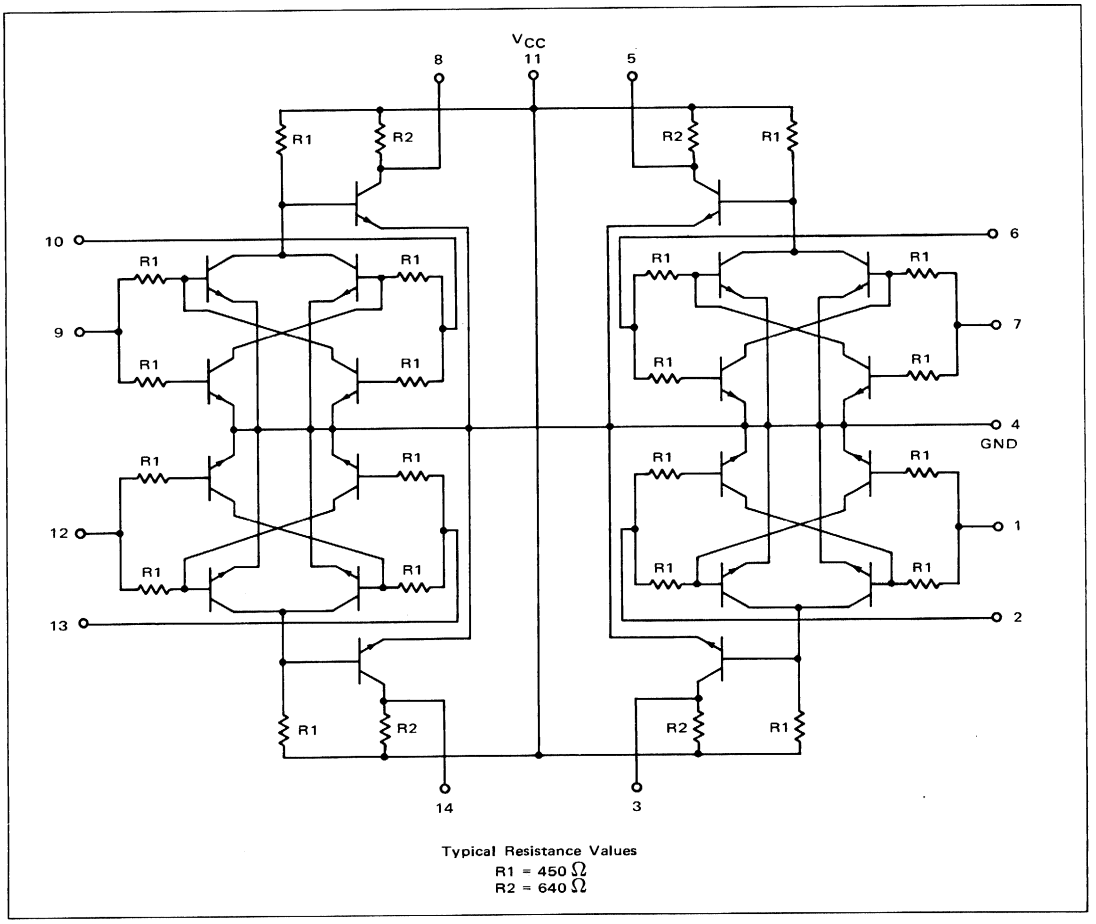
Test procedures are shown for one gate only. The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC871P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC771P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

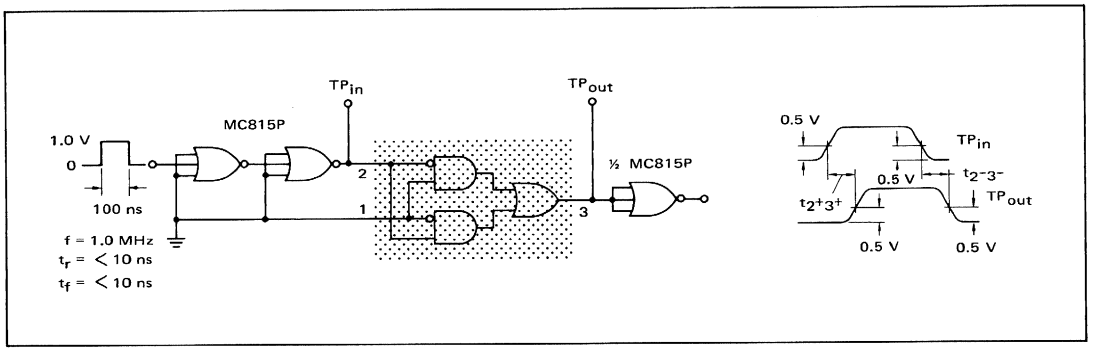
Characteristic	Symbol	Pin Under Test	MC871P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC771P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	1	-	1.2	-	1.2	-	1.1	mAdc	-	1.00	-	1.00	-	0.94	mAdc	1	-	-	2	11	4
		2	-	1.2	-	1.2	-	1.1	mAdc	-	1.00	-	1.00	-	0.94	mAdc	2	-	-	1	11	4
Output Current	I_{A5}*	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	1,3	-	2	11	4
		3	3.00	-	3.00	-	3.00	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	2,3	-	1	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	-	1,2	11	4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1,2	-	-	11	4
Switching Time	t	1+3-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In 1	2	Pulse Out 3	-	11	4
		1-3+	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	1	2	↓	-	↓	↓
		2+3+	-	-	-		-	-		-	-	-		-	-		2	-		1		
		2-3-	-	-	-		-	-		-	-	-		-	-		2	-		1		

Ground inputs of gates not under test. Other pins not listed are left open.

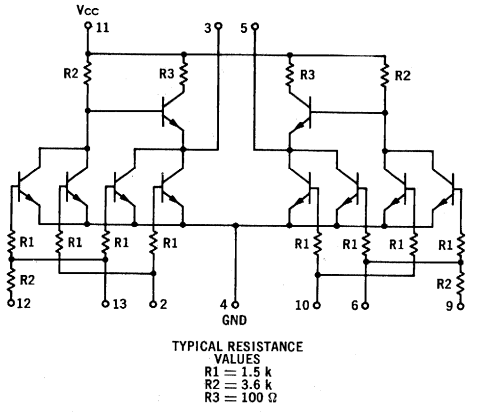
* Symbol is I_{A16} for MC771P.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

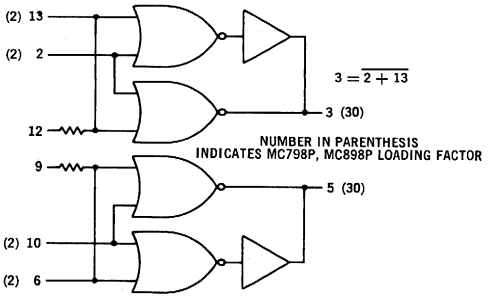


MC798P • MC898P



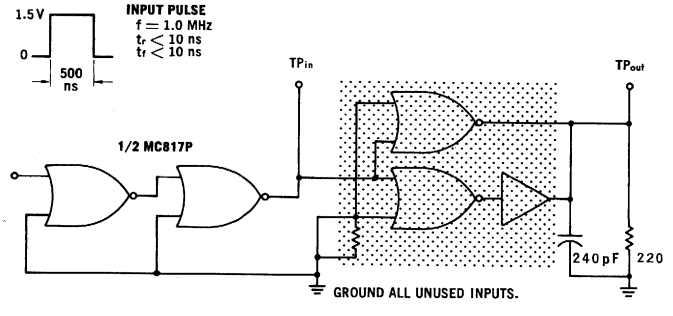
TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k
R3 = 100 Ω

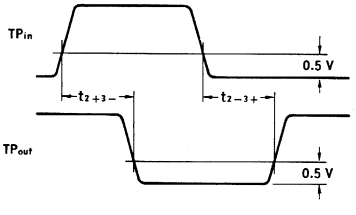
Dual 2-input buffers designed to drive a greater number of loads than the basic Resistor Transistor Logic circuit. Returning an input resistor to V_{CC} allows for capacitive coupling in multivibrator and differentiator applications.



t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

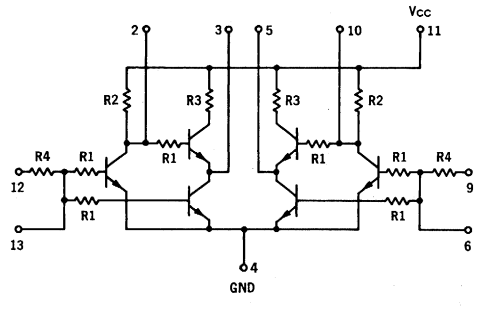
Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(k Ohms) V_R*
MC898P	0°C	0.880	0.850	1.80	0.500	3.60	4.6
	+25°C	0.830	0.800	1.80	0.460	3.60	4.8
	+75°C	0.740	0.710	1.80	0.400	3.60	5.0
MC798P	+15°C	0.865	0.865	1.80	0.475	3.60	4.6
	+25°C	0.850	0.850	1.80	0.460	3.60	4.8
	+55°C	0.800	0.800	1.80	0.430	3.60	5.0

Characteristic	Symbol	Pin Under Test	MC898P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC798P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2\ I_{in}$	2	-	300	-	280	-	280	μAdc	-	300	-	300	-	300	μAdc	2	-	13	-	11	-	4
Output Current	I_{AB}	3	4.5	-	4.5	-	4.5	-	mAdc	5.0	-	5.0	-	5.0	-	mAdc	-	3	-	2,13	11	-	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	3	2,4
		3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	3	4,13
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	13	-	11	3	2,4
		3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	-	11	3	4,13
Switching Time	$t_{on} + t_{off}$	2,3	-	-	-	160	-	-	ns	-	-	-	160	-	-	ns	Pulse In 2	Pulse Out 3	-	-	11	-	4,13

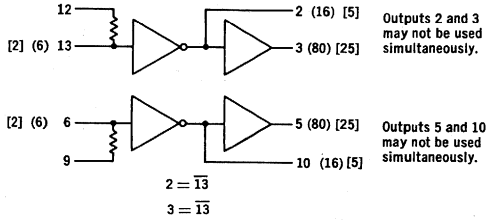
Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

MC799P • MC899P



TYPICAL RESISTANCE VALUES
R1 = 450Ω R3 = 100Ω
R2 = 640Ω R4 = 1.0 k

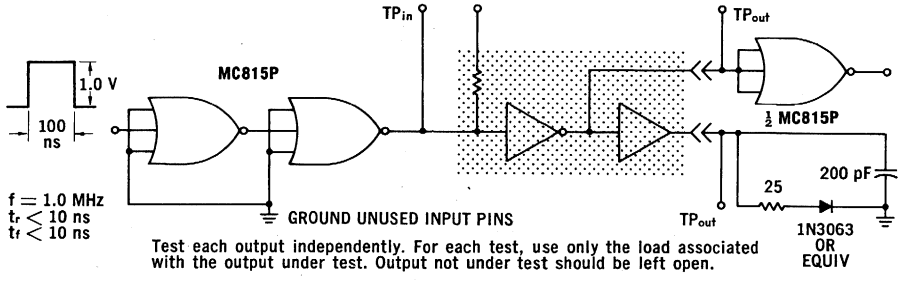
The dual buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input, the differentiation of input waveforms and various multivibrator applications.



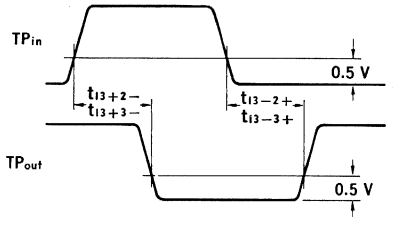
NUMBER IN PARENTHESIS INDICATES MC799P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC899P LOADING FACTOR

t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test. Output not under test should be left open.



ELECTRICAL CHARACTERISTICS

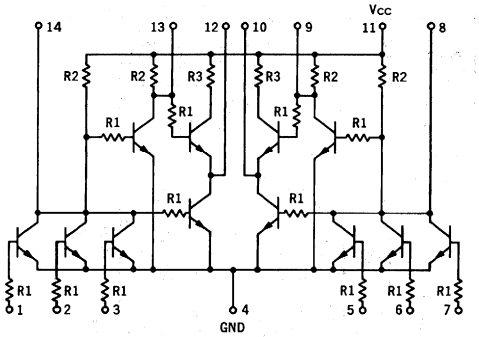
Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC899P	0°C	0.960	0.930	1.80	0.570	3.60	640
MC899P	+25°C	0.910	0.800	1.80	0.500	3.60	640
MC899P	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC799P	+15°C	0.865	0.865	1.80	0.475	3.60	640
MC799P	+25°C	0.850	0.850	1.80	0.460	3.60	640
MC799P	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC899P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC799P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2I_{in}$	13	-	1.2	-	1.2	-	1.1	mAdc	-	1.0	-	1.0	-	0.94	mAdc	13	-	-	-	11	-	4
Output Current	I_{A5}**	2	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	2	-	13	11	-	4
	I_{AB}	3	15.0	-	15.0	-	14.25	-	mAdc	13.75	-	13.75	-	12.50	-	mAdc	-	3	-	13	11	-	4
Output Voltage	V_{out}	2	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	-	4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	3	4
Saturation Voltage	$V_{CE(sat)}$	2	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	13	-	11	-	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	11, 12	-	↓
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	13	-	11	3	↓
																	Pulse In	Pulse Out					
Switching Time	t	13+3-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	13	3	-	-	11	-	4
		13-3+	-	-	-	45	-	-	↓	-	-	-	45	-	-	↓	13	3	-	-	↓	-	↓
		13+2-	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	13	2	-	-	↓	-	↓
		13-2+	-	-	-	32	-	-	↓	-	-	-	32	-	-	↓	13	2	-	-	↓	-	↓

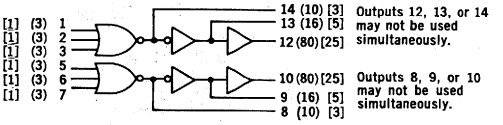
Ground all unused input pins. Other pins not listed are left open. * Resistor Value to V_{CC}. ** Symbol is I_{A16} for MC799P.

MC788P • MC888P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω

Two 3-input positive logic NOR gates, each followed by an inverting and non-inverting high fan-out amplifier, are provided in a single package. For each section, the output from each stage is available. If more than one output is used, the full loading factors cannot be employed since each output provides the drive for the succeeding stage.

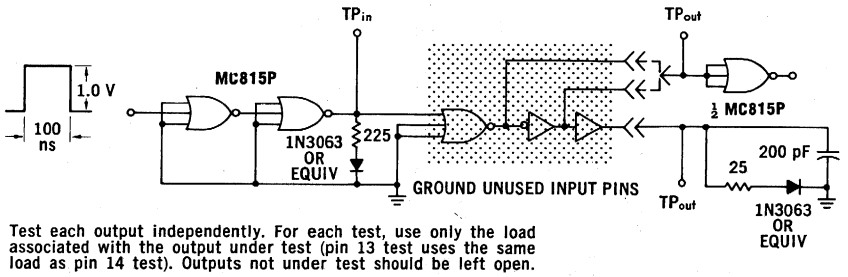


$14 = \overline{1+2+3}$ $13 = 1+2+3$ $12 = 1+2+3$

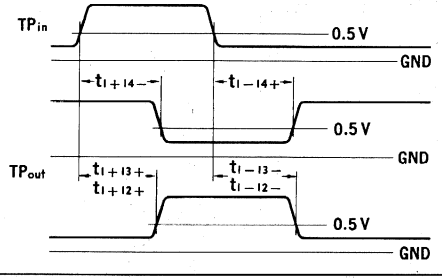
NUMBER IN PARENTHESIS INDICATES MC788P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC888P LOADING FACTOR.

t_{pd} = 24 ns
P_D = 145 mW (Input Low)
56 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test (pin 13 test uses the same load as pin 14 test). Outputs not under test should be left open.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC888P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC788P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

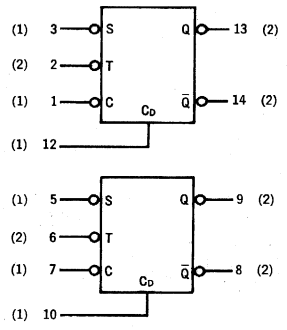
Characteristic	Symbol	Pin Under Test	MC888P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC788P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2, 3	-	11	-	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1, 3	-	↓	-	↓
		3	-		-		-			-		-		-			3	-	1, 2	-		-	
Output Current	I_{AB} †	12	15.0	-	15.0	-	14.25	-	mAdc	13.50	-	13.75	-	12.50	-	mAdc	-	12	-	14	11	-	4
	I_{A5} #	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.50	-	mAdc	-	13	-	14	↓	-	↓
	I_{A3} ‡	14	1.8	-	1.8	-	1.71	-		-	-	-	-	-	-	-	-	14	-	1, 2, 3		-	
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	12	1,2,3,4
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	-	1,2,3,4
		14	-		-		-			-		-		-			-	1	-	-		-	2,3,4
		14	-		-		-			-		-		-			-	2	-	-		-	1,3,4
		14	-		-		-			-		-		-			-	3	-	-		-	1,2,4
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	12	1,2,3,4
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	-	1,2,3,4
		14	-		—		-			-		-		-			-	-	1	-		-	2,3,4
		14	-		-		-			-		-		-			-	-	2	-		-	1,3,4
		14	-		-		-			-		-		-			-	-	3	-		-	1,2,4
																	Pulse In	Pulse Out					
Switching Time	t	1+12+	-	-	-	65	-	-	-	-	-	-	65	-	-	-	1	12	-	-	11	-	2,3,4
		1-12-	-	-	-	58	-	-	-	-	-	-	58	-	-	-	1	12	-	-	↓	-	
		1+13+	-	-	-	42.5	-	-	-	-	-	-	42.5	-	-	-	1	13	-	-		-	
		1-13-	-	-	-	42.5	-	-	-	-	-	-	42.5	-	-	-	1	13	-	-		-	
		1+14-	-	-	-	20	-	-	-	-	-	-	20	-	-	-	1	14	-	-		-	
		1-14+	-	-	-	28	-	-	-	-	-	-	28	-	-	-	1	14	-	-	↓	-	↓

Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

†I_{A80} is symbol for MC788P. #I_{A16} is symbol for MC788P. ‡I_{A5} is symbol for MC788P.

MC776P • MC876P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



fTOG = 3 MHz min
PD = 41 mW (Only Clock Input High)
29 mW (All Inputs Low)

NUMBER IN PARENTHESIS
INDICATES MC776P, MC876P LOADING FACTOR

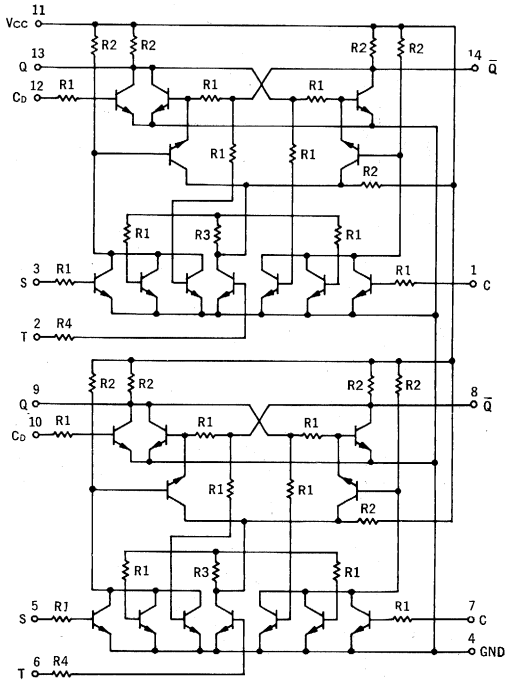
CLOCKED INPUT OPERATION①

t_n②		t_{n+1} ②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

① Direct input (C_D) must be low.

② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

③ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 1.5k R3 = 3.0k
R2 = 3.6k R4 = 750Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

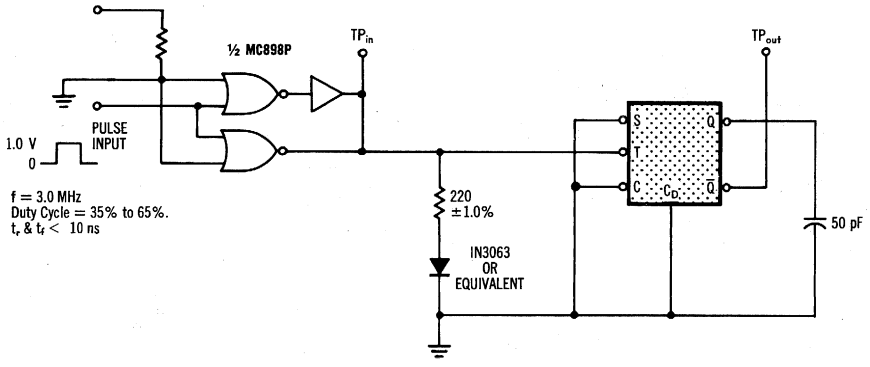
	@ Test Temperature	TEST VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	TEST VALUES (μA) I_O
MC876P	0°C	0.880	0.850	1.80	0.500	3.60	270
	+25°C	0.830	0.800	1.80	0.460	3.60	290
	+75°C	0.740	0.710	1.80	0.400	3.60	255
MC776P	+15°C	0.865	0.865	1.80	0.475	3.60	270
	+25°C	0.850	0.850	1.80	0.460	3.60	270
	+ 55°C	0.800	0.800	1.80	0.430	3.60	270

Characteristic	Symbol	Pin Under Test	MC876P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC776P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VALUES APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	I_O	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	µAdc	-	150	-	150	-	150	µAdc	1	-	13	-	11	-	4
	$2\ I_{in}$	2	-	300	-	280	-	280	↓	-	300	-	300	-	300	↓	2	-	1, 3	-	↓	-	↓
	I_{in}	3	-	150	-	140	-	140	↓	-	150	-	150	-	150	↓	3	-	14	-	↓	-	↓
	I_{in}	12	-	150	-	140	-	140	↓	-	150	-	150	-	150	↓	12	-	14	-	↓	-	↓
Output Current	I_{A2}	13	320	-	320	-	300	-	µAdc	320	-	320	-	320	-	µAdc	-	13	1	12	11	-	4, 14 §
		14	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	14	3, 12	-	↓	-	↓
		14	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	12, 14	3	-	↓	-	↓
Output Voltage	V_{out}	13	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	↓	-	4, 14
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	-	4, 13 §
		13*†	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	14	4, 12
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	3	↓	↓	↓
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 3	↓	↓	↓
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	-	↓	-	14 §
Saturation Voltage	$V_{CE(sat)}$	13	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	12	-	11	-	4, 14
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	-	4, 13 §
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	12	↓	-	4, 14 §
Turn On Voltage	V_{on}	13*#	850	-	800	-	710	-	mVdc	865	-	850	-	800	-	mVdc	-	1, 3	-	-	11	13	4, 12
		13*†	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3	-	1	↓	↓	↓
		13*†	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	-	1, 3	↓	↓	↓

* Clock Pulse to pin 2
† Pin 13 = LOW } Set by a momentary ground prior to the
# Pin 14 = LOW } application of the negative-going clock.

§ ground thru diode (cathode to ground).
Ground inputs of flip-flop not under test.
Other pins not listed are left open.

TOGGLE MODE TEST CIRCUIT



1. Set up the circuit with the Input Pulse as given.
2. The circuit should toggle with an output (TP_{out}) sense frequency of 1.5 MHz as the duty cycle is varied between 35% and 65%.

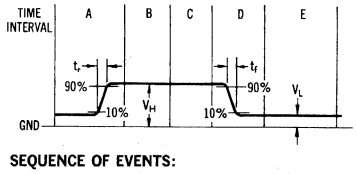
CLOCK PULSE

MC776P		
T_A	V_L	V_H
15°C	0.475 V	0.915 V
25°C	0.460 V	0.900 V
55°C	0.430 V	0.850 V

MC876P		
T_A	V_L	V_H
0°C	0.50 V	0.900 V
25°C	0.46 V	0.850 V
75°C	0.40 V	0.760 V

All values are ± 2.0mV

CLOCK PULSE DEFINITION

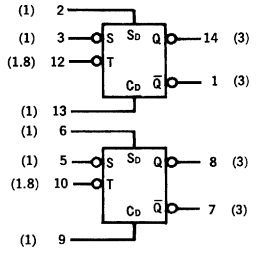


SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, but should be < 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC778P • MC878P

The type "D" Flip-Flop is a storage element that stores the state of the S input during negative transitions of the T input. The flip-flop state is not affected by changes in the S input during either the low or the high state of the T input. S_D and C_D inputs may be used for asynchronous operation.



DIRECT INPUT OPERATION①

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION③

t_n④		t_{n+1}④	
S		Q	$\bar{Q}$
1		1	0
0		0	1

NUMBER IN PARENTHESIS INDICATES MC778P, MC878P LOADING FACTOR

P_D = 48 mW (Direct Set, S_D, and Direct Clear, C_D, Low; all other inputs high)
35 mW (All Inputs Low)

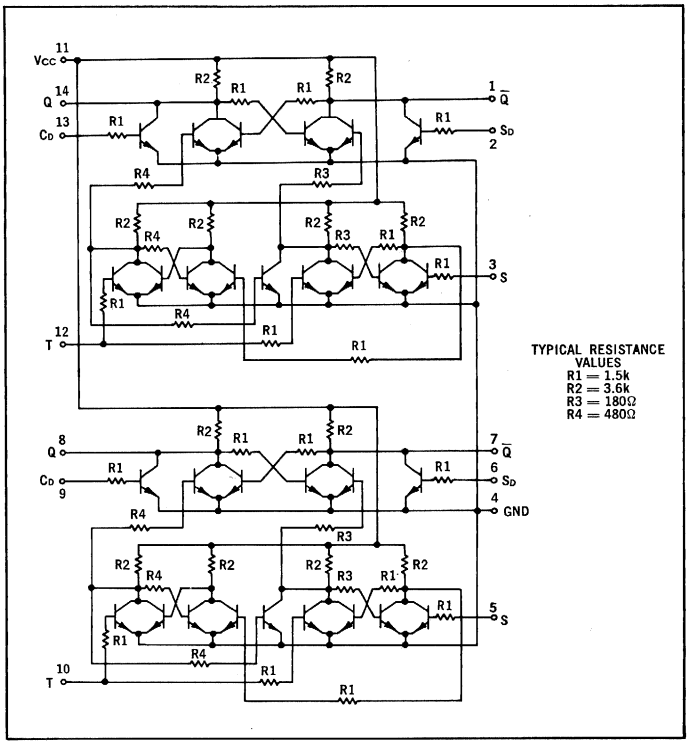
frog = 1 MHz

① Clock (T input) must be high.

② The output state will not change when the input state goes from $S_D = C_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.

③ Direct inputs (S_D and C_D) must be low.

④ The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.



TYPICAL RESISTANCE VALUES
R1 = 1.5k
R2 = 3.6k
R3 = 180Ω
R4 = 480Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

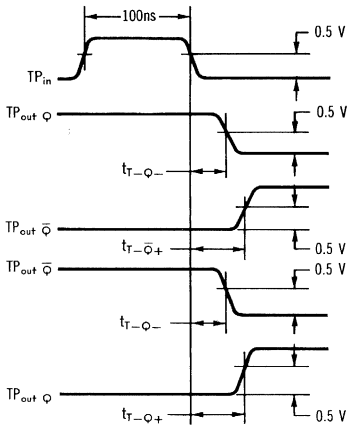
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	KΩ±1% V_R*
MC878P	0°C	0.880	0.850	1.80	0.500	3.60	0.45	4.3
	+25°C	0.830	0.800	1.80	0.460	3.60	0.40	4.3
	+75°C	0.740	0.710	1.80	0.400	3.60	0.35	4.7
MC778P	+15°C	0.865	0.865	1.80	0.475	3.60	-	4.6
	+25°C	0.850	0.850	1.80	0.460	3.60	-	4.8
	+55°C	0.800	0.800	1.80	0.430	3.60	-	5.0

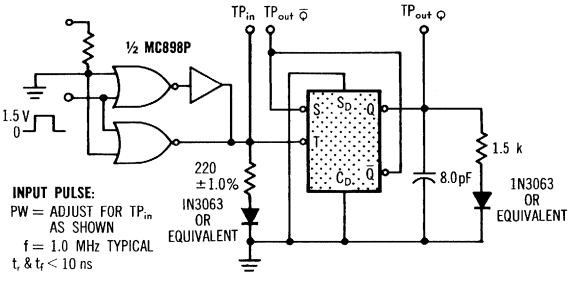
Characteristic	Symbol	Pin Under Test	MC878P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC778P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	V_R*	Gnd
Input Current	I_{in}	2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	3	12	11	-	12	4, 13
	I_{in}	3	-	150	-	140	-	140		-	150	-	150	-	150		3	-	-	12		-	12	2, 4, 13
	1.8 I_{in}	12	-	270	-	250	-	250		-	270	-	270	-	270		12	-	-	-		-	-	2, 3, 4, 13
	1.8 I_{in}	12	-	270	-	250	-	250		-	270	-	270	-	270		12	-	3	-		-	-	2, 4, 13
	I_{in}	13	-	150	-	140	-	140		-	150	-	150	-	150		13	-	-	12		-	12	2, 3, 4
Output Current	I_{A3}	1	420	-	430	-	395	-	μAdc	420	-	420	-	420	-	μAdc	1	12	3, 13	2	11	-	-	4
		1		-		-		-			-		-		-		1	-	13	2, 12		-	12	3, 4
		14		-		-		-			-		-		-		14	12	2	13		-	-	3, 4
		14		-		-		-			-		-		-		14	3	2	12, 13		-	12	4
Output Voltage	V_{out}	1	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	12, 13	-	11	-	-	3, 4
		1	-		-		-			-		-		-			-	14	12	-		-	-	2, 3, 4, 13
		14	-		-		-			-		-		-			-	13	2, 12	-		-	-	3, 4
		14	-		-		-			-		-		-			-	1	12	-		-	-	2, 3, 4, 13
Saturation Voltage	$V_{CE(sat)}$	1	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	3	13	12	11	-	12	2, 4
		14	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	3, 12	11	-	12	4, 13
Leakage Current	I_L	11	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	μAdc	-	-	-	-	-	11	-	2, 3, 4, 12, 13

* Apply to V_{CC} thru resistor prior to applying V_{off}. Ground inputs of flip-flop not under test. Other pins not listed are left open.

SWITCHING TIMES
TEST CIRCUIT AND WAVEFORMS

FIGURE 1

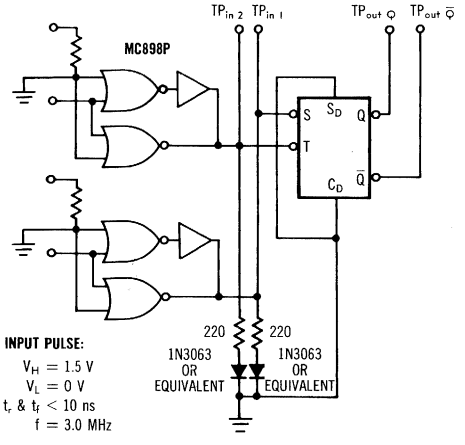




TEST	MAXIMUM (ns @ 25°C)
t_{T-Q+}	120
$t_{T-\overline{Q}-}$	80
t_{T-Q-}	80
$t_{T-\overline{Q}+}$	120

SWITCHING TIMES

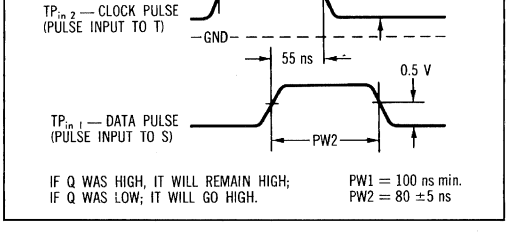
FIGURE 2A — SET-UP AND RELEASE TIMES TEST CIRCUIT



INPUT PULSES ARE ADJUSTED TO PRODUCE TP$_{in\ 1}$ AND TP$_{in\ 2}$ SHOWN IN FIGURES 2B AND 2C.

TP$_{in\ 1}$ is defined as the data pulse
TP$_{in\ 2}$ is defined as the clock pulse

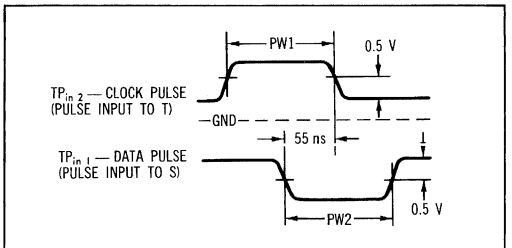
FIGURE 2B — SET-UP TIME WAVEFORMS



IF Q WAS HIGH, IT WILL REMAIN HIGH;
IF Q WAS LOW; IT WILL GO HIGH.

PW1 = 100 ns min.
PW2 = 80 ±5 ns

FIGURE 2C — RELEASE TIME WAVEFORMS

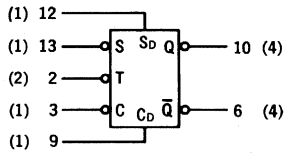


IF Q WAS LOW, IT WILL REMAIN LOW;
IF Q WAS HIGH, IT WILL GO LOW.

PW1 = 100 ns min.
PW2 = 80 ±5 ns

MC722P • MC822P

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



NUMBER IN PARENTHESIS
INDICATES MC722P, MC822P LOADING FACTOR

f_{TOG} = 1.0 MHz
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The ouput state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.

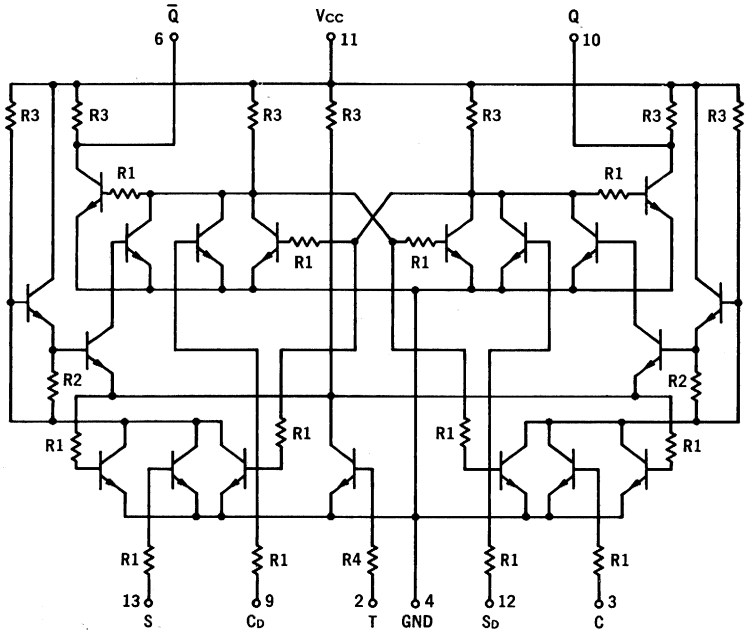
0 = low state

1 = high state

t_n = time period prior to negative transition of clock pulse

t_{n+1} = time period subsequent to negative transition of clock pulse

Q_n = state of Q output in time period t_n



TYPICAL RESISTANCE VALUES
R1 = 1.5 k R3 = 3.6 k
R2 = 2.0 k R4 = 750 Ω

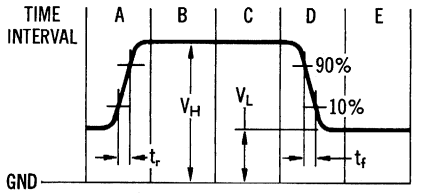
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC822P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC722P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC822P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC722P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	2	-	300	-	280	-	280	µAdc	-	300	-	300	-	300	µAdc	2	-	3, 13	-	11	4
	I_{in}	3	-	150	-	140	-	140		-	150	-	150	-	150		3	-	12	-		
		9	-		-		-			-		-		-			9	-	-	-		
		12	-		-		-			-		-		-			12	-	-	-		
		13	-		-		-			-		-		-			13	-	9	-		
Output Current	I_{A4}	6	570	-	570	-	535	-	mAdc	570	-	570	-	570	-	µAdc	6	9	12	-	11	4
		10	570	-	570	-	535	-	mAdc	570	-	570	-	570	-	µAdc	10	12	9	-	11	4
Saturation Voltage	$V_{CE(sat)}$	6	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	12	-	9	11	4
		6*#	-		-		-			-		-		-			-	13	-	3		
		6*#	-		-		-			-		-		-			-	-	-	3, 13		
		6*##	-		-		-			-		-		-			-	3, 13	-	-		
		10	-		-		-			-		-		-			-	9	-	12		
		10*##	-		-		-			-		-		-			-	3	-	13		
		10*#	-		-		-			-		-		-			-	3, 13	-	-		
		10*##	-		-		-			-		-		-			-	-	-	3, 13		

Pins not listed are left open.
* = Clock Pulse to pin 2, see Figure 1.
# = Pin 9 HIGH, ## = Pin 12 HIGH } Set by a momentary application of V_{BOT} prior to the application of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

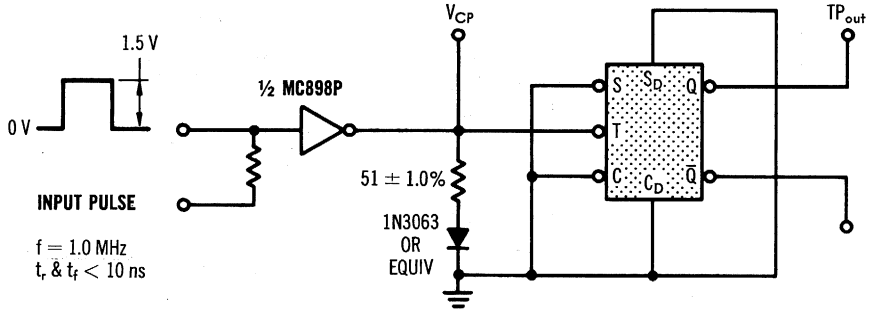
MC822P

T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+ 0.850 V ± 2.0 mV
0°C	+ 0.500 V ± 2.0 mV	+ 0.900 V ± 2.0 mV
+ 75°C	+ 0.400 V ± 2.0 mV	+ 0.760 V ± 2.0 mV

MC722P

T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+ 0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+ 0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+ 0.850 V ± 2.0 mV

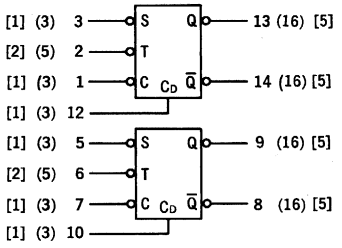
FIGURE 2 — TOGGLE MODE TEST CIRCUIT



THE SENSE FREQUENCY AT TP_{out} (0.5 MHz) SHOULD BE ½ THE FREQUENCY AT V_{CP} WHEN THE DUTY CYCLE IS VARIED BETWEEN 25% AND 75%.

MC791P • MC891P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



f_{tog} = 4 MHz
t_{pd} = 40 ns typ

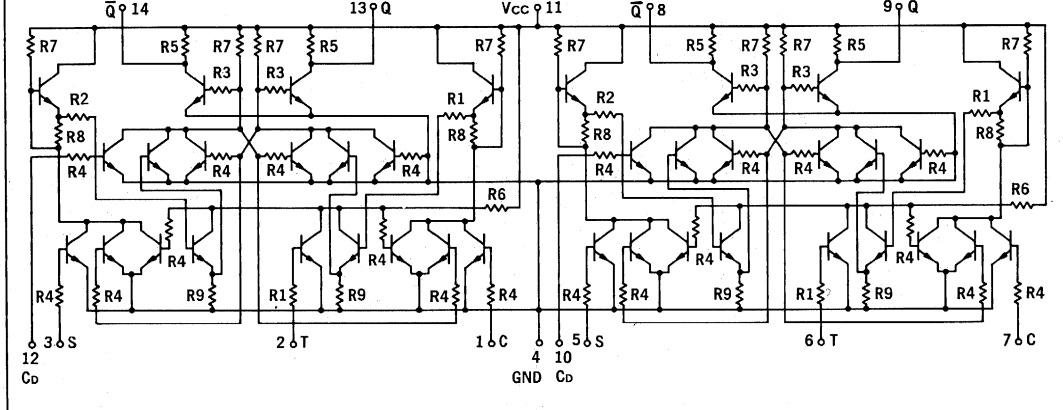
P_D = 190 mW typ (Only Clock Input High)
160 mW typ (Inputs Low)

CLOCKED INPUT OPERATION ①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC791P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC891P



TYPICAL RESISTANCE VALUES
R1 = 300 Ω R4 = 600 Ω R7 = 900 Ω
R2 = 500 Ω R5 = 640 Ω R8 = 2.0 k
R3 = 550 Ω R6 = 700 Ω R9 = 3.0 k

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC891P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC791P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC891P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC791P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1†	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	-	-	11	4
	$2I_{in}$	2	-	1200	-	1200	-	1140	↓	-	1000	-	1000	-	940	↓	2	-	1, 3	-	↓	↓
	I_{in}	3	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	3	-	12	-	↓	↓
	I_{in}	12	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	12	-	-	-	↓	↓
Output Current	I_{A5}‡	13†	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	13	-	-	11	-
		14	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	12, 14	-	-	11	4
Output Voltage	V_{out}	13 § ⑤	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	4, 12
		13§§④	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	3	↓	↓
		13 § ⑥	-		-		-			-		-		-			-	1	-	-		
		13§§⑦	-		-		-			-		-		-			-	-	-	3		
		14 § ④	-		-		-			-		-		-			-	-	-	1		
		14§§⑤	-		-		-			-		-		-			-	3	-	-		
		14 § ⑦	-		-		-			-		-		-			-	-	-	1		
		14§§⑥	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	13†	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	12	-	-	11	4
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	↓
		13†*	-		-		-			-		-		-			-	1	-	3		
		13†*	-		-		-			-		-		-			-	-	-	1, 3		
		14*#	-		-		-			-		-		-			-	3	-	1		
		14*#	-		-		-			-		-		-			-	-	-	1, 3		
		14†*	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	↓

Ground inputs of flip-flop not under test. Other pins not listed are left open.

† Preset the flip-flop by the following procedure:
(1) Momentarily apply V_{BOT} to pin 12 to preclear flip-flop.
(2) After V_{BOT} is removed from pin 12, ground pins 1 and 3.
(3) Apply a negative-going clock pulse to pin 2 (see note*) while pins 1 and 3 are still grounded. This changes the state of the flip-flop to the SET condition.
(4) Remove grounds from pins 1 and 3, and proceed with the test.

‡ Symbol is I_{A16} for MC791P.

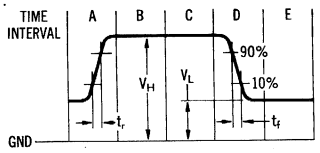
* Clock pulse to pin 2, see Figure 1.

Pin 12 = HIGH — Set by momentary application of V_{BOT} prior to the application of the negative-going clock pulse.

§ = Clock pulse to pin 2, data pulse to pin 3.
§§ = Clock pulse to pin 2, data pulse to pin 1.

④ = See Figure 4.
⑤ = See Figure 5.
⑥ = See Figure 6.
⑦ = See Figure 7.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC891P

T_A	V_L	V_H
+ 25°C	+ 0.500 V ± 2.0 mV	+ 0.930 V ± 2.0 mV
0°C	+ 0.570 V ± 2.0 mV	+ 0.980 V ± 2.0 mV
+ 75°C	+ 0.450 V ± 2.0 mV	+ 0.790 V ± 2.0 mV

MC791P

T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+ 0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+ 0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+ 0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT

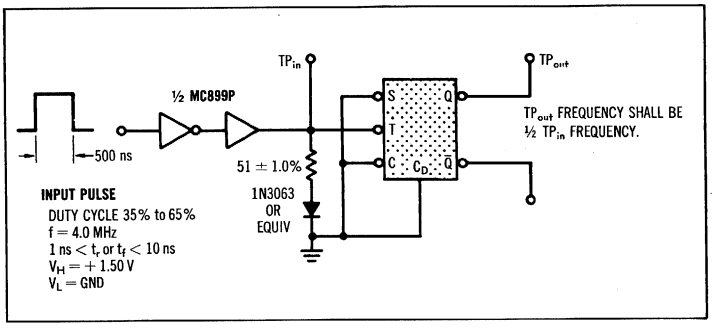


FIGURE 3 — TEST CIRCUIT

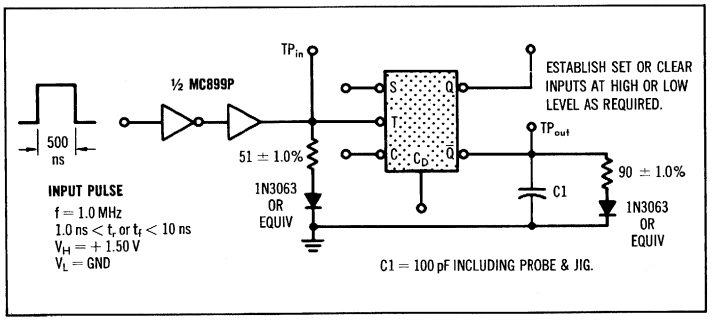


FIGURE 4 — TEST WAVEFORMS

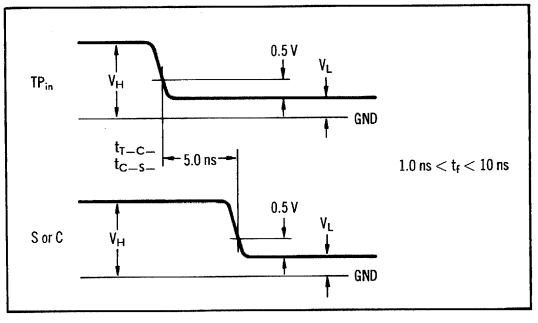


FIGURE 5 — TEST WAVEFORMS

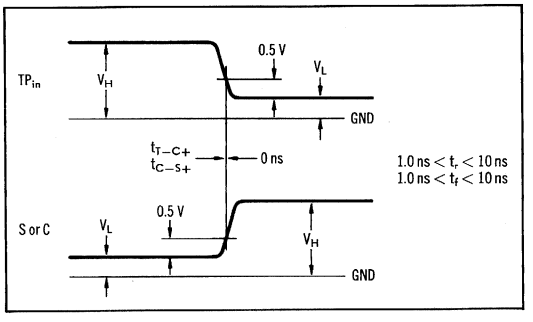


FIGURE 6 — TEST WAVEFORMS

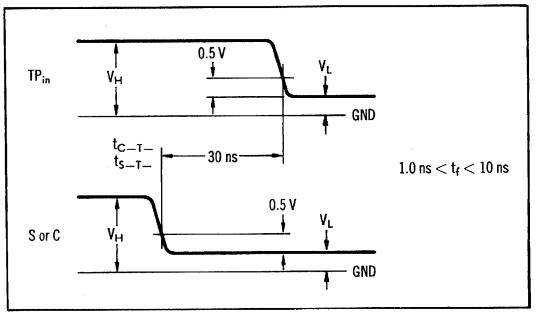
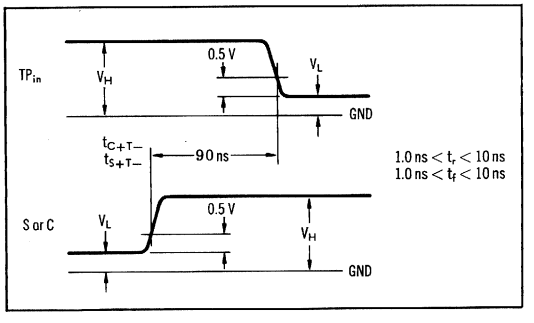
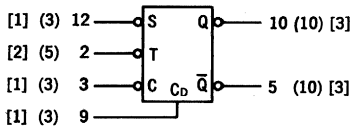


FIGURE 7 — TEST WAVEFORMS



MC723P • MC816P

J-K flip-flop with a direct clear input in addition to the clocked inputs.



f_{tog} = 4 MHz

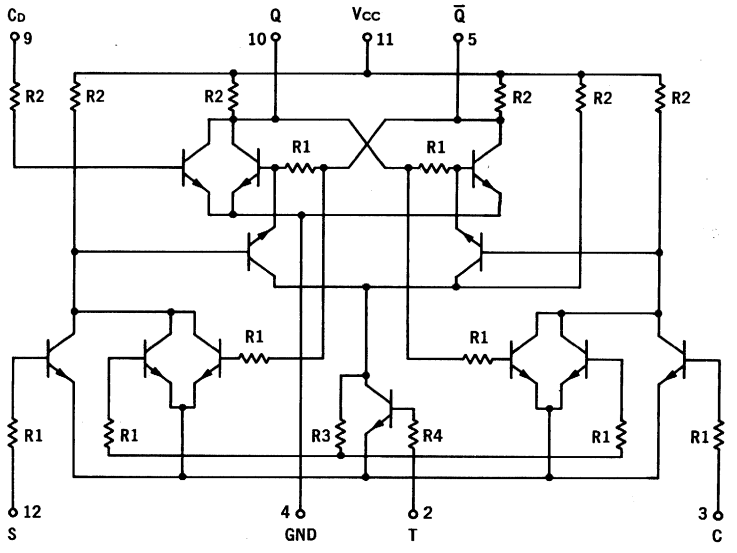
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

CLOCKED INPUT OPERATION ①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC723P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC816P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC816P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC723P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC816P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC723P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	2	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	2	-	3, 12	-	11	4
	I_{in}	3	-	600	-	600	-	570		-		-		-			3	-	10	-		
		9	-		-		-			-		-		-			9	-	5	-		
		12	-		-		-			-		-		-			12	-	5	-		
Output Current	I_{A3}†	5	1.80	-	1.80	-	1.71	-	mAdc	1.65	-	1.65	-	1.56	-	mAdc	-	5	9, 12	-	11	4
		5		-		-		-			-		-		-		-	5, 9	12	-		4
		10		-		-		-			-		-		-		-	10	3	9		4, 5§
Output Voltage	V_{out}	10	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	9	-	-	11	4, 5
		10*##	-		-		-			-		-		-			-	3, 12	-	-		4, 9
		10*	-		-		-			-		-		-			-	3	-	12		
		10*##	-		-		-			-		-		-			-	-	-	3, 12		
Saturation Voltage	$V_{CE(sat)}$	5	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	-	9	11	4, 5
		10	-		-		-			-		-		-			-	-	9	-		4, 5
		10	-		-		-			-		-		-			-	-	-	-		4, 10§
Turn-On Voltage	V_{on}	10*##Δ	930	-	880	-	790	-	mVdc	865	-	850	-	800	-	mVdc	-	3, 12	-	-	11	4, 9
		10*Δ		-		-		-			-		-		-		-	12	-	3		
		10*#Δ		-		-		-			-		-		-		-	-	-	3, 12		

Pins not listed are left open.

† = I_{A10} is symbol for MC723P

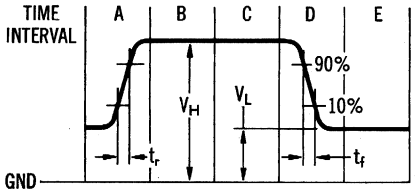
§ = Silicon diode to ground.

* = Clock Pulse to pin 2, See Figure 1.

= Pin 10 LOW
= Pin 5 LOW
} Set by a momentary ground prior to the application of the negative-going Clock pulse.

Δ = MC816P pin 10 loaded by: 1.56 mAdc (0°C and +75°C)
1.65 mAdc (+25°C)
MC723P pin 10 loaded by: 1.56 mAdc (+15°C and +55°C)
1.65 mAdc (+25°C)

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

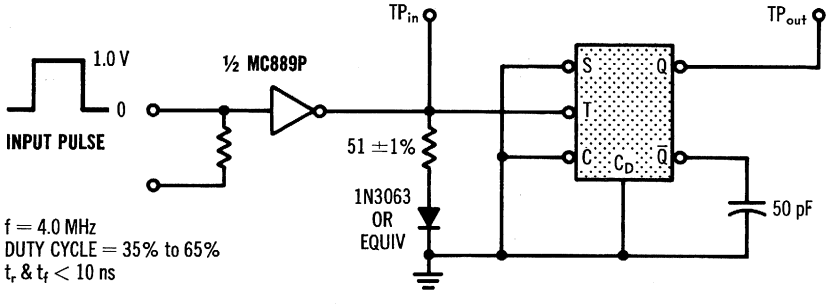
MC816P

T_A	V_L	V_H
+25°C	+0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+75°C	+0.450 V ± 2.0 mV	+0.840 V ± 2.0 mV

MC723P

T_A	V_L	V_H
+25°C	+0.460 V ± 2.0 mV	+0.900 V ± 2.0 mV
+15°C	+0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+55°C	+0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

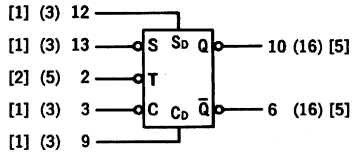
FIGURE 2 — TOGGLE MODE TEST CIRCUIT



FREQUENCY AT TP_{out} SHOULD BE ½ THE FREQUENCY AT TP_{in}

MC726P • MC826P

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



f_{TOG} = 4 MHz

P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

CLOCKED INPUT OPERATION ①

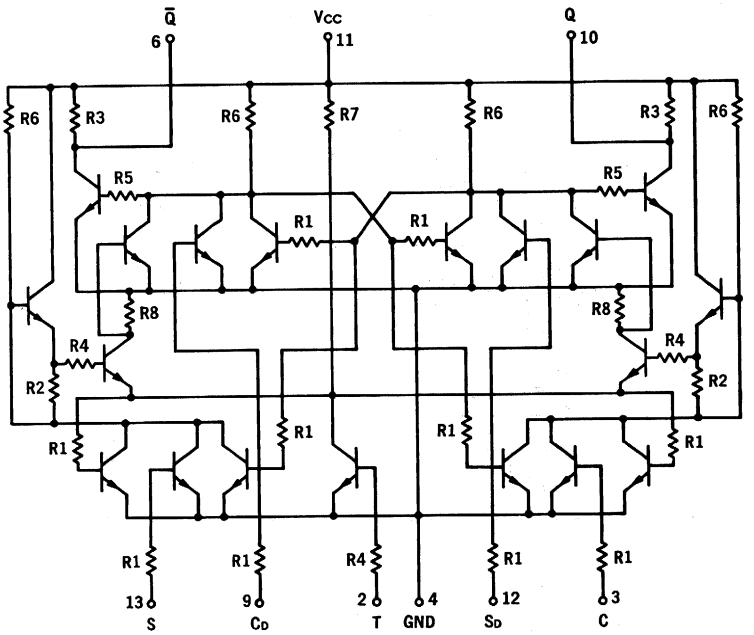
t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

DIRECT INPUT OPERATION ④

S_D	C_D	Q	$\bar{Q}$
0	0	⑤	⑤
1	0	1	0
0	1	0	1
1	1	0	0

1. Direct inputs (C_D and S_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock (T) to remain unchanged.
5. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
6. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC726P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC826P



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 550 Ω
R2 = 2 k	R6 = 900 Ω
R3 = 640 Ω	R7 = 700 Ω
R4 = 300 Ω	R8 = 3 k

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
		TEST VOLTAGE VALUES (Volts)				
MC826P	0°C	0.960	0.930	1.80	0.570	3.60
MC826P	+25°C	0.910	0.880	1.80	0.500	3.60
MC826P	+75°C	0.820	0.790	1.80	0.450	3.60
MC726P	+15°C	0.865	0.865	1.80	0.475	3.60
MC726P	+25°C	0.850	0.850	1.80	0.460	3.60
MC726P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC826P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC726P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	2	-	1200	-	1200	-	1140	µAdc	-	1000	-	1000	-	940	µAdc	2	-	3, 13	-	11	4
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	12	-		
		9	-		-		-			-		-		-			9	-	-	-		
		12	-		-		-			-		-		-			12	-	-	-		
		13	-		-		-			-		-		-			13	-	9	-		
Output Current	I_{A5} §	6	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	-	6, 12	9	-	11	4
		10	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	-	10, 9	12	-	11	4
Saturation Voltage	$V_{CE(sat)}$	6	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	12	-	9	11	4
		6*#	-		-		-			-		-		-			-	13	-	3		
		6*#	-		-		-			-		-		-			-	-	-	3, 13		
		6*##	-		-		-			-		-		-			-	3, 13	-	-		
		10	-		-		-			-		-		-			-	9	-	12		
		10*##	-		-		-			-		-		-			-	3	-	13		
		10*#	-		-		-			-		-		-			-	3, 13	-	-		
		10*##	-		-		-			-		-		-			-	-	-	3, 13		

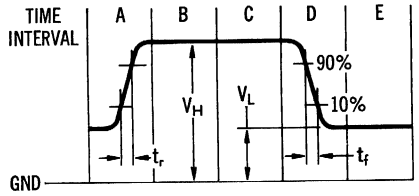
Pins not listed are left open.

* Clock Pulse to pin 2, see Figure 1.

§ I_{A16} is symbol for MC726P.

\# Pin 9 HIGH
Pin 12 HIGH
} Set by momentary application of V_{BOT} prior to the application of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

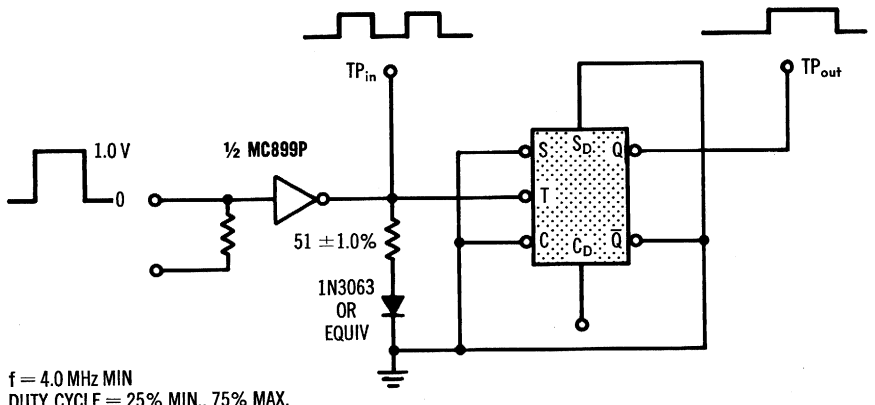
MC826P

T_A	V_L	V_H
+ 25°C	+0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+ 75°C	+0.450 V ± 2.0 mV	+0.840 V ± 2.0 mV

MC726P

T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT

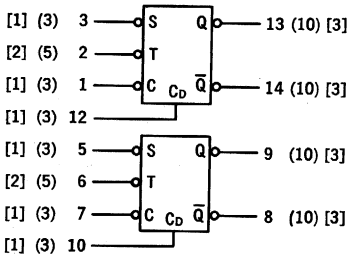


f = 4.0 MHz MIN
DUTY CYCLE = 25% MIN., 75% MAX.
t_r & $t_f < 10$ ns

OUTPUT FREQUENCY SHALL BE ½ OF TP_{in} FREQUENCY.

MC790P • MC890P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



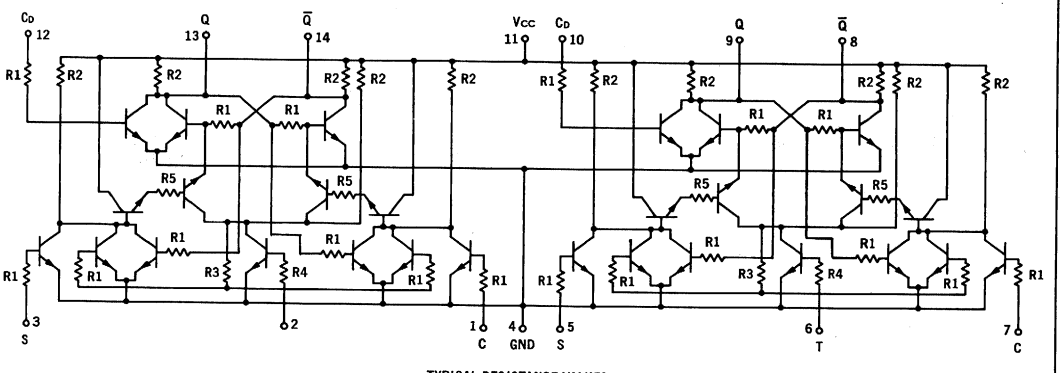
f_{Tog} = 4 MHz
P_D = 182 mW (Only Clock Input High)
158 (Inputs Low)

CLOCKED INPUT OPERATION ①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC790P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC890P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω R3 = 510 Ω
R2 = 640 Ω R4 = 225 Ω
R5 = 300 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC890P	0°C	0.960	0.930	1.80	0.570	3.60
MC890P	+25°C	0.910	0.880	1.80	0.500	3.60
MC890P	+75°C	0.820	0.790	1.80	0.450	3.60
MC790P	+15°C	0.865	0.865	1.80	0.475	3.60
MC790P	+25°C	0.850	0.850	1.80	0.460	3.60
MC790P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC890P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC790P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	13	-	11	2, 3, 4, 12
	$2I_{in}$	2	-	1200	-	1200	-	1140	↓	-	1000	-	1000	-	940	↓	2	-	1, 3	-	↓	4, 12
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	14	-		1, 2, 4, 12
	I_{in}	12	-	600	-	600	-	570		-	500	-	500	-	470		12	-	14	-		1, 2, 3, 4
Output Current	I_{A3} §	13	1.80	-	1.80	-	1.71	-	mAdc	1.65	-	1.65	-	1.56	-	mAdc	-	13	1	12	11	2, 3, 4
		14	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	14	3, 12	-	↓	1, 2, 4
		14		-		-		-			-		-		-		-	12, 14	3	-		1, 2, 4
Output Voltage	V_{out}	13	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	11	1,2,3,4,14
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	4, 12
		13*##	-		-		-			-		-		-			-	1	-	3		↓
		13*##	-		-		-			-		-		-			-	-	-	1, 3		
		14*##	-		-		-			-		-		-			-	1, 3	-	-		
		14*#	-		-		-			-		-		-			-	3	-	1		
		14*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 3	↓	
Saturation Voltage	$V_{CE(sat)}$	13	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	12	-	11	1,2,3,4,14
		13#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	1,2,3,4,12
		14##	-		-		-			-		-		-			-	-	12	-		1,2,3,4

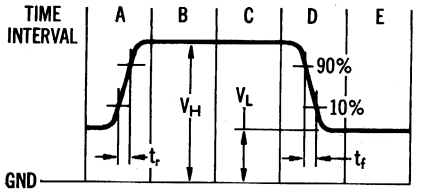
Ground unused input pins. Other pins not listed are left open.

* Clock pulse to pin 2, see Figure 1,

§ I_{A10} is symbol for MC790P.

Pin 13 = LOW
Pin 14 = LOW
} Set by a momentary ground prior to the application of the negative-going Clock Pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

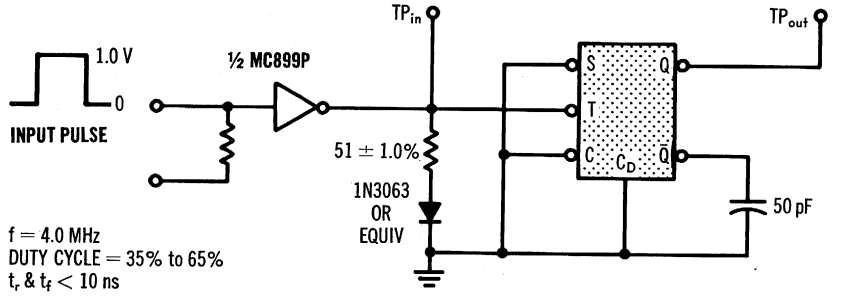
MC890P

T_A	V_L	V_H
+ 25°C	+0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+ 75°C	+0.450 V ± 2.0 mV	+0.840 V ± 2.0 mV

MC790P

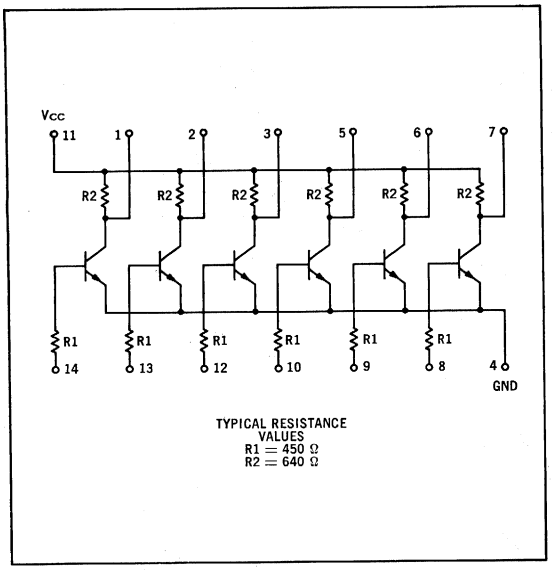
T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



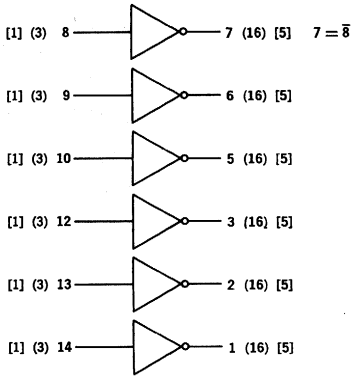
FREQUENCY AT TP_{out} SHOULD BE ½ THE FREQUENCY AT TP_{in}

MC789P • MC889P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

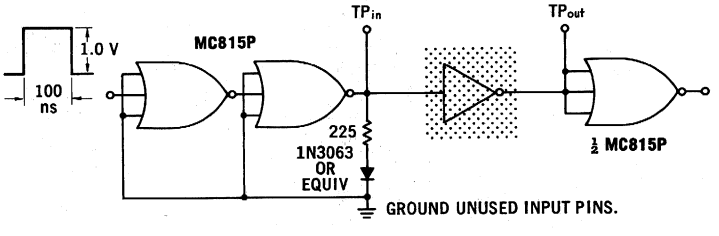
Six individual circuits are contained in a single package. Each provides the simple inversion function.

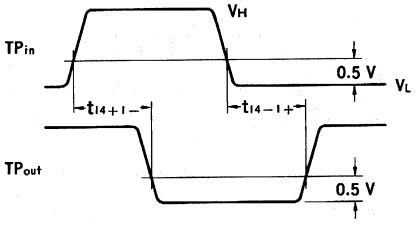


NUMBER IN PARENTHESIS INDICATES MC789P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC889P LOADING FACTOR.

t_{pd} = 12 ns
P_D = 130 mW (Input High)
15 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.
The other inverters are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC889P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC789P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

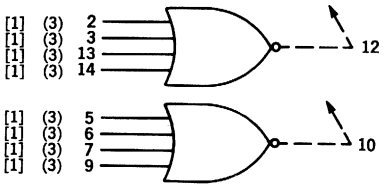
Characteristic	Symbol	Pin Under Test	MC889P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC789P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	14*	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	14	-	*	-	11	4
Output Current	I_{A5}	1	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	1	-	-	14	11	4
Output Voltage	V_{out}	1	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	4
Saturation Voltage	$V_{CE(sat)}$	1	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	4
Switching Time	$t_{on} + t_{off}$	1, 14	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In: 14	Pulse Out: 1	-	-	11	4

Ground inputs of inverters not under test. Other pins not listed are left open

* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V_{BOT}.

MC786P • MC886P

Two 4-input gate expanders housed in a single package. Each may be used independently or combined. Each expander increases the input capability of a standard MRTL gate by four.

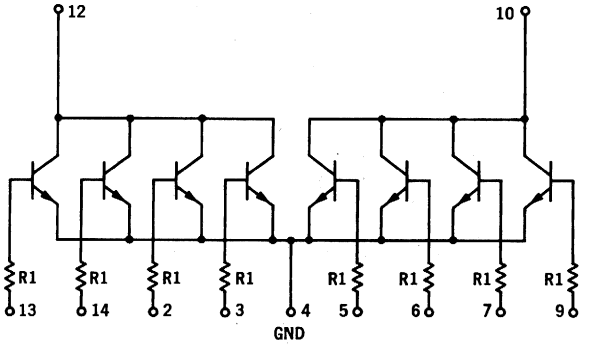


$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MC786P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC886P LOADING FACTOR.
SEE SHEET 6-158 FOR EXPANDER RULES

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



V_{CC} CONNECTION TO PIN 11 NOT SHOWN

TYPICAL RESISTANCE VALUES
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expander is tested in the same manner.

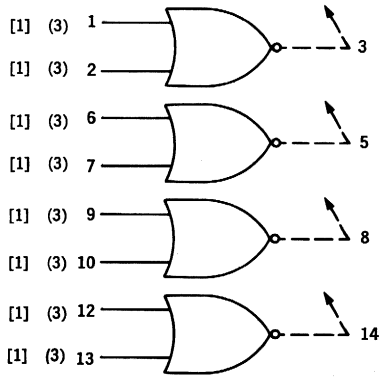
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC886P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC786P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC886P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC786P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	3,13,14	-	11	12	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,13,14	-	↓	↓	↓
		13	-		-		-			-		-		-			13	-	2,3,14	-			
		14	-		-		-			-		-		-			14	-	2,3,13	-			
Output Leakage Current	I_{CEX}	12	-	200	-	200	-	250	μAdc	-	225	-	225	-	250	μAdc	12	-	-	2, 3, 13, 14	11	-	4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	12	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	↓	2,3,4,13
		12	-		-		-			-		-		-			-	2	-	-			3,4,13,14
		12	-		-		-			-		-		-			-	3	-	-			2,4,13,14
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	13	-	11	12	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	↓	2,3,4,13
		12	-		-		-			-		-		-			-	-	2	-			3,4,13,14
		12	-		-		-			-		-		-			-	-	3	-			2,4,13,14

Ground unused input pins. Other pins not listed are left open.

MC785P • MC885P

Four 2-input expanders housed in a single package increase the input capability of MRTL gates.

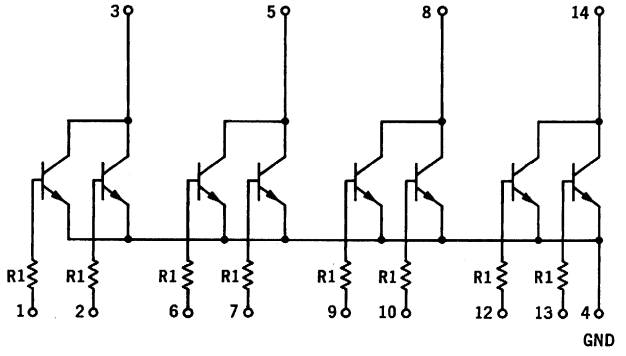


$3 = \overline{1 + 2}$

$t_{pd} = 12$ ns
$P_D = 20$ mW (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MC785P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC885P LOADING FACTOR.
SEE SHEET 6-158 FOR EXPANDER RULES

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



V_{CC} CONNECTION TO PIN 11 IS NOT SHOWN

TYPICAL RESISTANCE VALUES
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

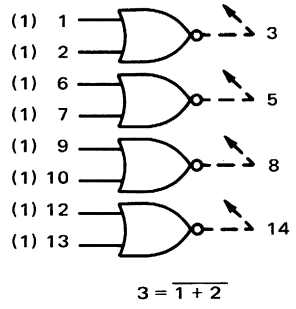
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC885P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC785P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC885P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC785P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	3	4
		2	-	600	—	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	1	-	11	3	4
Output Leakage Current	I_{CEX}	3	-	200	-	200	-	250	μAdc	-	225	-	225	-	250	μAdc	3	-	-	1, 2	11	-	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	3	2, 4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	3	1, 4
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	3	2, 4
		3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	2	-	11	3	1, 4

Ground unused input pins. Other pins not listed are left open. * Resistor value to V_{CC}.

MC9721P • MC9821P

Four 2-input expanders housed in a single package increase the input capability of mW MRTL gates.



$3 = \overline{1 + 2}$

t_{pd} = 27 ns

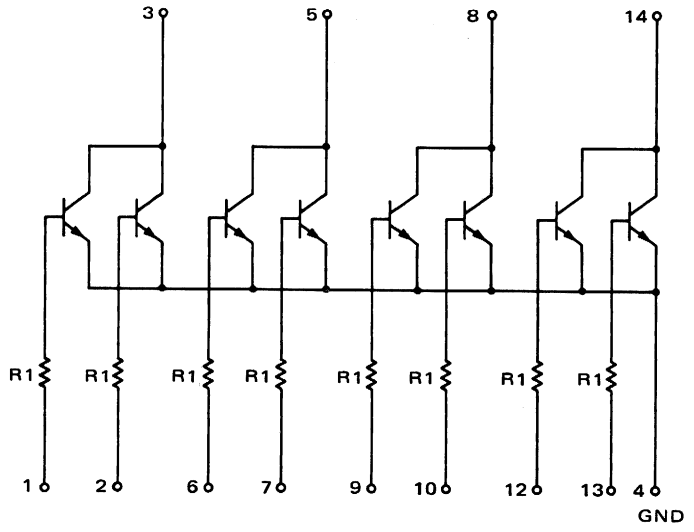
P_D = 20 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MC9721P, MC9821P LOADING FACTOR

NOTES ON THE USE OF THE MC9721/MC9821

1. The input loading factor of the expanded gate is 1.33.
2. Pin 11 of the expander must be connected to V_{CC}.
3. The output loading factor of the expanded gate is decreased 0.5 load for every added node.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



V_{CC} connection to pin 11 is not shown
Typical Resistance Values
R1 = 1.5 k

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(kΩ) V_R*
MC9821P	0°C	0.880	0.850	1.80	0.500	3.60	3.6
	+25°C	0.830	0.800	1.80	0.460	3.60	3.6
	+75°C	0.740	0.710	1.80	0.400	3.60	4.0
MC9721P	+15°C	0.865	0.865	1.80	0.475	3.60	3.6
	+25°C	0.850	0.850	1.80	0.460	3.60	3.6
	+55°C	0.800	0.800	1.80	0.430	3.60	3.6

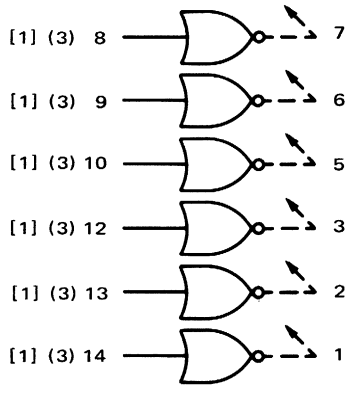
Characteristic	Symbol	Pin Under Test	MC9821P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9721P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	2	-	11	3	4
		2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	1	-	11	3	4
Output Leakage Current	I_{CEX}	3	-	25	-	25	-	30	μAdc	-	40	-	40	-	50	μAdc	3	-	-	1,2	11	-	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	3	2,4
		3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	3	1,4
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	1	-	11	3	2,4
		3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	-	11	3	1,4

Ground unused input pins. Other pins not listed are left open.

* Resistor value to V_{CC}.

MC9719P • MC9819P

Six individual expanders are contained in a single package to increase the input capability of MRTL gates.



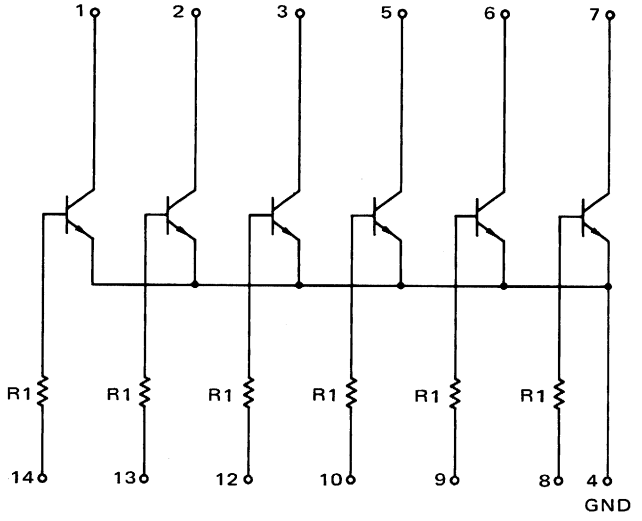
t_{pd} = 12 ns
P_D = 13 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES
MC9719P LOADING FACTOR

NUMBER IN BRACKETS INDICATES
MC9819P LOADING FACTOR

When an expander is added to a gate, subtract 0.4 load from the output of the gate for each expander circuit added.

SEE SHEET 6-158 FOR EXPANDER RULES



V_{CC} connection to pin 11 is not shown
Typical Resistance Value
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC9819P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC9719P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC9819P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9719P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	14	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	14	-	-	-	11	1	4
Output Leakage Current	I_{CEX}	1	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	1	-	-	14	11	-	4
Output Voltage	V_{out}	1	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1	4
Saturation Voltage	$V_{CE(sat)}$	1	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	1	4

Ground inputs of expanders not under test. Other pins not listed are left open.

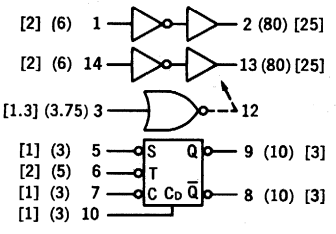
* Resistor value to V_{CC}.

MULTIFUNCTION DEVICES

(1 J-K Flip-Flop, 1 Expander, 2 Buffers)

MC779P • MC879P

A medium-power monolithic device consisting of one J-K flip-flop, one expander, and two buffer circuits in a single package. This J-K flip-flop can be operated in the toggling mode. Simultaneous logic ONE pulses applied to the SET and CLEAR terminals cause the output state to reverse. A direct clear input allows asynchronous entry for preclearing counters, inserting parallel data into registers, and other similar applications. The MRTL expander is designed to increase the fan-in capability of gates with expander inputs, and the buffers are high fan-out gates with single inputs.



$2 = \overline{1}$

$12 = \overline{3}$

CLOCKED INPUT OPERATION ①

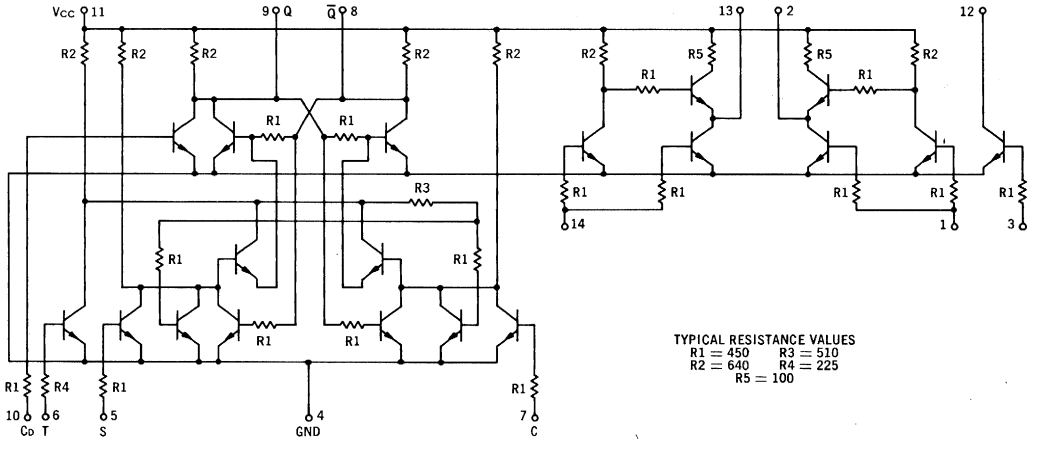
t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

	f_{Tog} MHz	t_{pd}	P_D(mW)	
			(Inputs High)	(Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
EXPANDER	—	12	2.5	Negligible

‡Only Clock Input High

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC779P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC879P



TYPICAL RESISTANCE VALUES
R1 = 450 R3 = 510
R2 = 640 R4 = 225
R5 = 100

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC879P	0°C	0.960	0.930	1.80	0.570	3.60	640
MC879P	+25°C	0.910	0.880	1.80	0.500	3.60	640
MC879P	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC779P	+15°C	0.865	0.865	1.80	0.475	3.60	640
MC779P	+25°C	0.850	0.850	1.80	0.460	3.60	640
MC779P	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC879P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC779P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2I_{in}$	1	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	1	-	-	-	11	2	3,4,5,6,7,10,14
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	-	-		12	1,4,5,6,7,10,14
	I_{in}	5	-	600	-	600	-	570		-	500	-	500	-	470		5	-	8	-		-	1,3,4,14
	$2I_{in}$	6	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		6	-	5, 7	-		-	
	I_{in}	7	-	600	-	600	-	570		-	500	-	500	-	470		7	-	9	-		-	
	I_{in}	10	-	600	-	600	-	570		-	500	-	500	-	470		10	-	8	-		-	
	$2I_{in}$	14	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		14	-	-	-		13	1,3,4,5,6,7,10
Output Current	I_{AB}†	2	15.0	-	15.0	-	14.25	-	mAdc	13.50	-	13.75	-	12.50	-	mAdc	-	2	-	1	11	-	3,4,5,6,7,10,14
	I_{A3}‡	8	1.8	-	1.8	-	1.71	-		1.65	-	1.65	-	1.56	-		-	8	5, 10	-		-	1,3,4,14
	I_{A3}‡	8		-		-		-			-		-		-		-	8, 10	5	-		-	
	I_{A3}‡	9##		-		-		-			-		-		-		-	9	7	10		-	
	I_{A5}#	12	3.0	-	3.0	-	2.85	-		2.65	-	2.65	-	2.50	-		-	12	-	3		12	1,4,5,6,7,10,14
	I_{AB}†	13	15.0	-	15.0	-	14.25	-		13.50	-	13.75	-	12.50	-		-	13	-	14		-	1,3,4,5,6,7,10
Output Voltage	V_{out}	2	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2	3,4,5,6,7,10,14
		8Δ##	-		-		-			-		-		-			-	5, 7	-	-		-	1,3,4,10,14
		8Δ**	-		-		-			-		-		-			-	5	-	7		-	
		8Δ**	-		-		-			-		-		-			-	-	-	5, 7		-	
		9	-		-		-			-		-		-			-	10	-	-		-	1,3,4,8,14
		9Δ**	-		-		-			-		-		-			-	5, 7	-	-		-	1,3,4,10,14
		9Δ##	-		-		-			-		-		-			-	7	-	5		-	
		9Δ##	-		-		-			-		-		-			-	-	-	5, 7		-	
		12	-		-		-			-		-		-			-	3	-	-		12	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	14	-	-		13	1,3,4,5,6,7,10
Saturation Voltage	$V_{CE(sat)}$	2	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	2	3,4,5,6,7,10,14
		8##	-		-		-			-		-		-			-	-	-	10		-	1,3,4,14
		9	-		-		-			-		-		-			-	-	10	-		-	1,3,4,8,14
		9**	-		-		-			-		-		-			-	-	-	-		-	1,3,4,14
		12	-		-		-			-		-		-			-	-	3	-		12	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	-	14	-		13	1,3,4,5,6,7,10
																	Pulse In	Pulse Out					
Switching Time	t	1+2-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	1	2	-	-	11	-	3,4,14
		1-2+	-	-	-	45	-	-		-	-	-	45	-	-		1	2	-	-		-	3,4,14
		14+13-	-	-	-	30	-	-		-	-	-	30	-	-		14	13	-	-		-	1,3,4
		14-13+	-	-	-	45	-	-		-	-	-	45	-	-		14	13	-	-		-	1,3,4

Pins not listed are left open.

Δ = Clock Pulse to pin 6, see Figure 1.

* = Resistor value to V_{CC}.

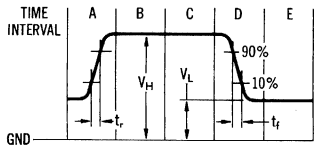
† = I_{A80} is symbol for MC779P

‡ = I_{A10} is symbol for MC779P

\# = I_{A16} is symbol for MC779P

Pin 8 = LOW
** Pin 9 = LOW
} Set by a momentary ground prior to the application of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

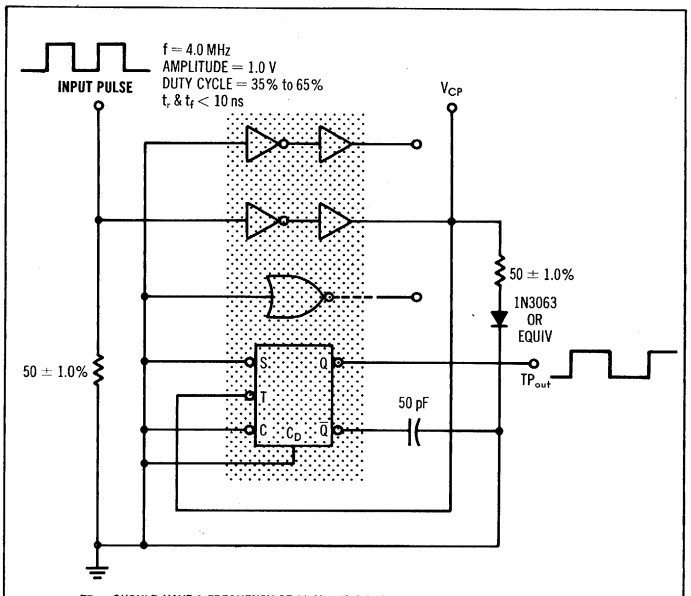
MC879P

T_A	V_L	V_H
+ 25°C	+ 0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+ 0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+ 75°C	+ 0.450 V ± 2.0 mV	+0.790 V ± 2.0 mV

MC779P

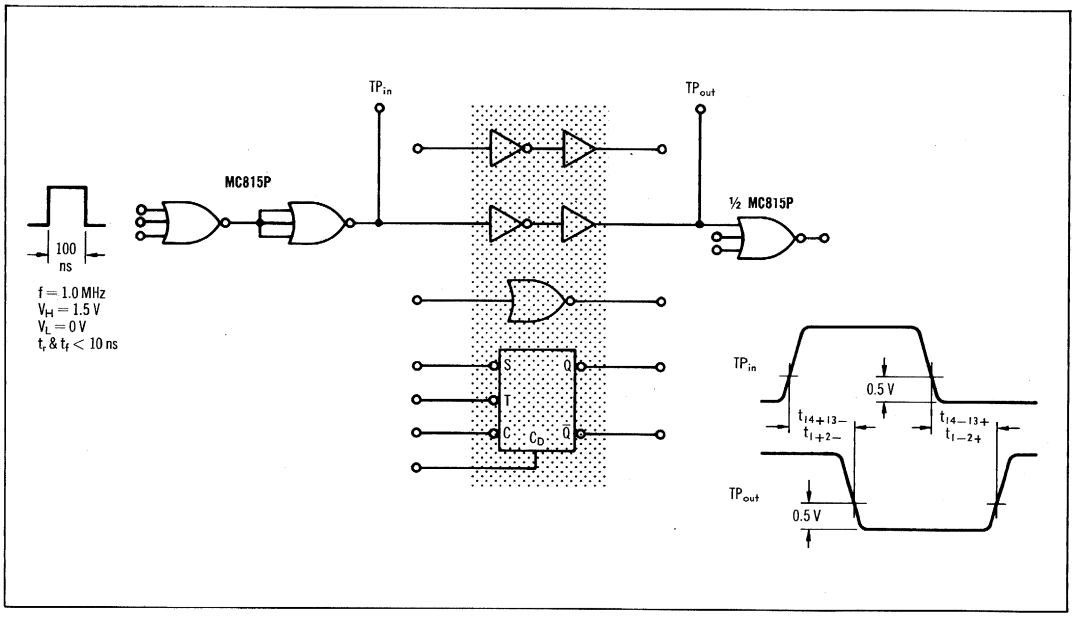
T_A	V_L	V_H
+ 25°C	−0.460 V ± 2.0 mV	−0.900 V ± 2.0 mV
+ 15°C	+0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+ 55°C	+0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



TP_{out} SHOULD HAVE A FREQUENCY OF ½ V_{CP} (2.0 MHz) WHEN THE DUTY CYCLE IS VARIED FROM 35% to 65%.

FIGURE 3 — SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

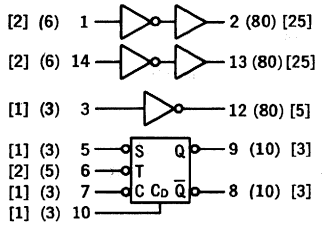


MULTIFUNCTION DEVICES

(1 J-K Flip-Flop, 1 Inverter, 2 Buffers)

MC787P • MC887P

A medium-power monolithic device consisting of one J-K flip-flop, one inverter, and two buffer circuits in a single package. This J-K flip-flop can be operated in the toggling mode. Simultaneous logic ONE pulses applied to the SET and CLEAR terminals cause the output state to reverse. A direct clear input allows asynchronous entry for pre-clearing counters, inserting parallel data into registers, and other similar applications. The inverter is a basic MRTL gate and the buffers are high fan-out gates with single inputs.



$2 = \overline{1}$

$12 = \overline{3}$

CLOCKED INPUT OPERATION ①

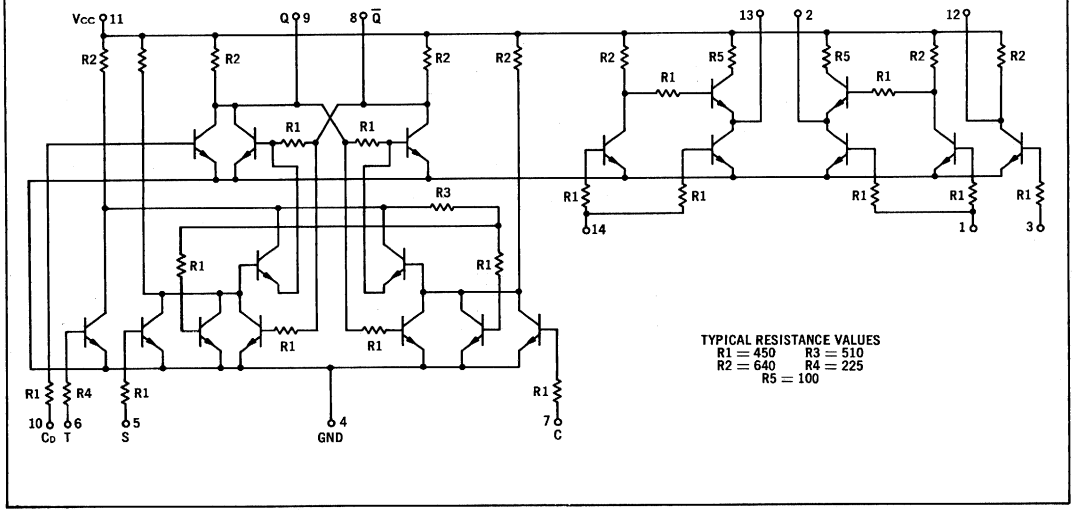
t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

	f_{tog} MHz	t_{pd} ns	P_D (mW) (Input High)	P_D (mW) (Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
INVERTER	—	12	22	8

‡Only Clock Input High

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC787P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC887P



TYPICAL RESISTANCE VALUES
R1 = 450 R3 = 510
R2 = 640 R4 = 225
R5 = 100

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC887P	0°C	0.960	0.930	1.80	0.570	3.60	640
MC887P	+25°C	0.910	0.880	1.80	0.500	3.60	640
MC887P	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC787P	+15°C	0.865	0.865	1.80	0.475	3.60	640
MC787P	+25°C	0.850	0.850	1.80	0.460	3.60	640
MC787P	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC887P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC787P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2I_{in}$	1	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	1	-	-	-	11	2	3,4,5,6,7,10,14
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	-	-		-	1,4,5,6,7,10,14
	I_{in}	5	-	600	-	600	-	570		-	500	-	500	-	470		5	-	8	-		-	1,3,4,14
	$2I_{in}$	6	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		6	-	5,7	-		-	
	I_{in}	7	-	600	-	600	-	570		-	500	-	500	-	470		7	-	9	-		-	
	I_{in}	10	-	600	-	600	-	570		-	500	-	500	-	470		10	-	8	-		-	
	$2I_{in}$	14	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		14	-	-	-		13	1,3,4,5,6,7,10
Output Current	I_{AB}†	2	15.0	-	15.0	-	14.25	-	mAdc	13.50	-	13.75	-	12.50	-	mAdc	-	2	-	1	11	-	3,4,5,6,7,10,14
	I_{A3}‡	8	1.8	-	1.8	-	1.71	-		1.65	-	1.65	-	1.56	-		-	8	5,10	-		-	1,3,4,14
	I_{A3}‡	8		-		-		-			-		-		-		-	8,10	5	-		-	
	I_{A3}‡	9##		-		-		-			-		-		-		-	9	7	10		-	
	I_{A5}#	12	3.0	-	3.0	-	2.85	-		2.65	-	2.65	-	2.50	-		-	12	-	3		-	1,4,5,6,7,10,14
	I_{AB}†	13	15.0	-	15.0	-	14.25	-		13.50	-	13.75	-	12.50	-		-	13	-	14		-	1,3,4,5,6,7,10
Output Voltage	V_{out}	2	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2	3,4,5,6,7,10,14
		8Δ##	-		-		-			-		-		-			-	5,7	-	-		-	1,3,4,10,14
		8Δ**	-		-		-			-		-		-			-	5	-	7		-	
		8Δ**	-		-		-			-		-		-			-	-	-	5,7		-	
		9	-		-		-			-		-		-			-	10	-	-		-	1,3,4,8,14
		9Δ**	-		-		-			-		-		-			-	5,7	-	-		-	1,3,4,10,14
		9Δ##	-		-		-			-		-		-			-	7	-	5		-	
		9Δ##	-		-		-			-		-		-			-	-	-	5,7		-	
		12	-		-		-			-		-		-			-	3	-	-		-	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	14	-	-		13	1,3,4,5,6,7,10
Saturation Voltage	$V_{CE(sat)}$	2	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	2	3,4,5,6,7,10,14
		8##	-		-		-			-		-		-			-	-	-	10		-	1,3,4,14
		9	-		-		-			-		-		-			-	-	10	-		-	1,3,4,8,14
		9**	-		-		-			-		-		-			-	-	-	-		-	1,3,4,14
		12	-		-		-			-		-		-			-	—	3	-		-	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	-	14	-		13	1,3,4,5,6,7,10
																	Pulse In	Pulse Out					
Switching Time	t	1+2-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	1	2	-	-	11	-	3,4,14
		1-2+	-	-	-	45	-	-		-	-	-	45	-	-		1	2	-	-		-	3,4,14
		14+13-	-	-	-	30	-	-		-	-	-	30	-	-		14	13	-	-		-	1,3,4
		14-13+	-	-	-	45	-	-		-	-	-	45	-	-		14	13	-	-		-	1,3,4

Pins not listed are left open.

Δ = Clock Pulse to pin 6, see Figure 1.

* Resistor value to V_{CC}.

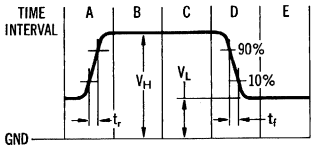
† = I_{A80} is symbol for MC787P

‡ = I_{A10} is symbol for MC787P

\# = I_{A16} is symbol for MC787P

Pin 8 = LOW } Set by a momentary ground prior to the application of the negative-going clock pulse.
** Pin 9 = LOW }

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

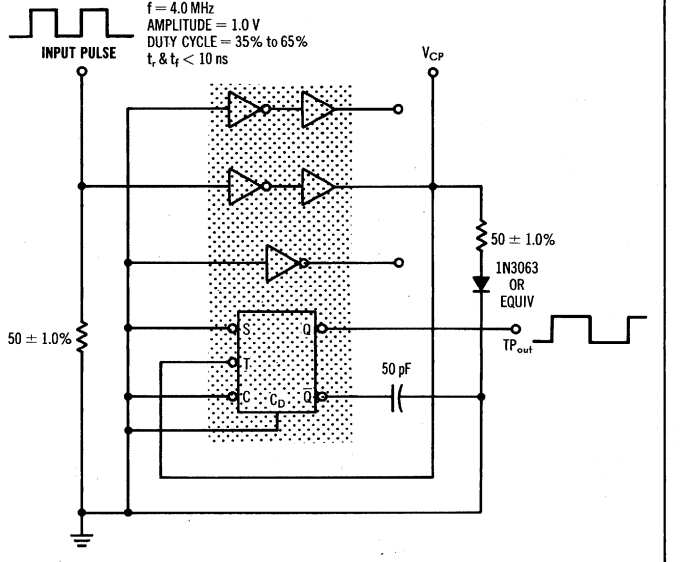
MC887P

T_A	V_L	V_H
+ 25°C	+ 0.500 V ± 2.0 mV	+ 0.930 V ± 2.0 mV
0°C	+ 0.570 V ± 2.0 mV	+ 0.980 V ± 2.0 mV
+ 75°C	+ 0.450 V ± 2.0 mV	+ 0.790 V ± 2.0 mV

MC787P

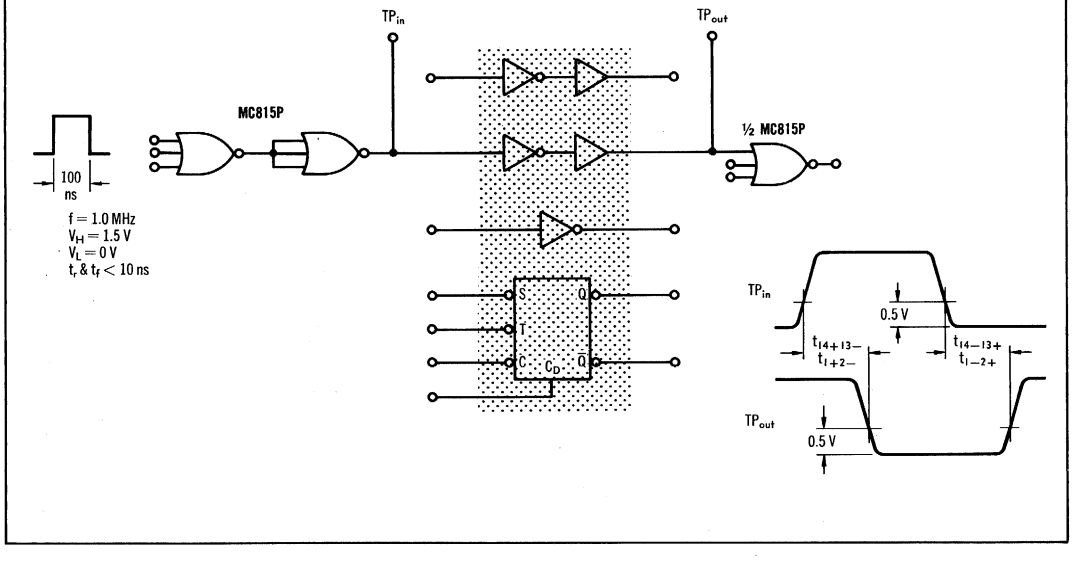
T_A	V_L	V_H
+ 25°C	−0.460 V ± 2.0 mV	−0.900 V ± 2.0 mV
+ 15°C	+0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+ 55°C	+0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT

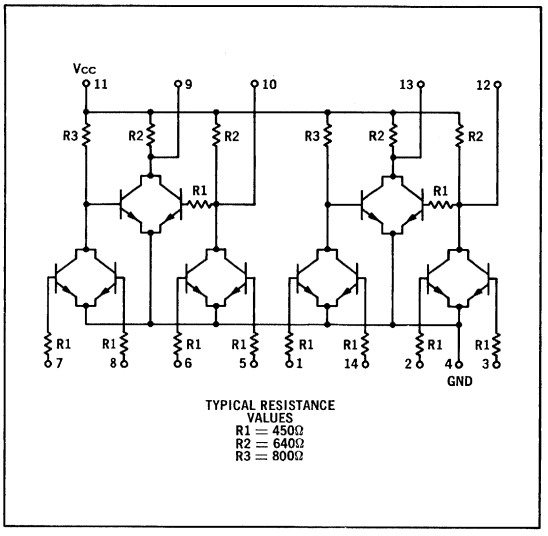


TP_{out} SHOULD HAVE A FREQUENCY OF ½ V_{CP} (2.0 MHz) WHEN THE DUTY CYCLE IS VARIED FROM 35% to 65%.

FIGURE 3 — SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

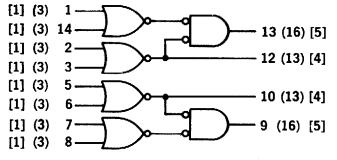


MC775P • MC875P



TYPICAL RESISTANCE VALUES
R1 = 450Ω
R2 = 640Ω
R3 = 800Ω

Two half-adder devices in a single package. Each device can be used to supply the SUM and CARRY operations on two input signals. E g.,if the inputs are applied to pins 1 and 14, and their complements to pins 2 and 3, the SUM of the inputs appears on pin 13 while the CARRY appears on pin 12.

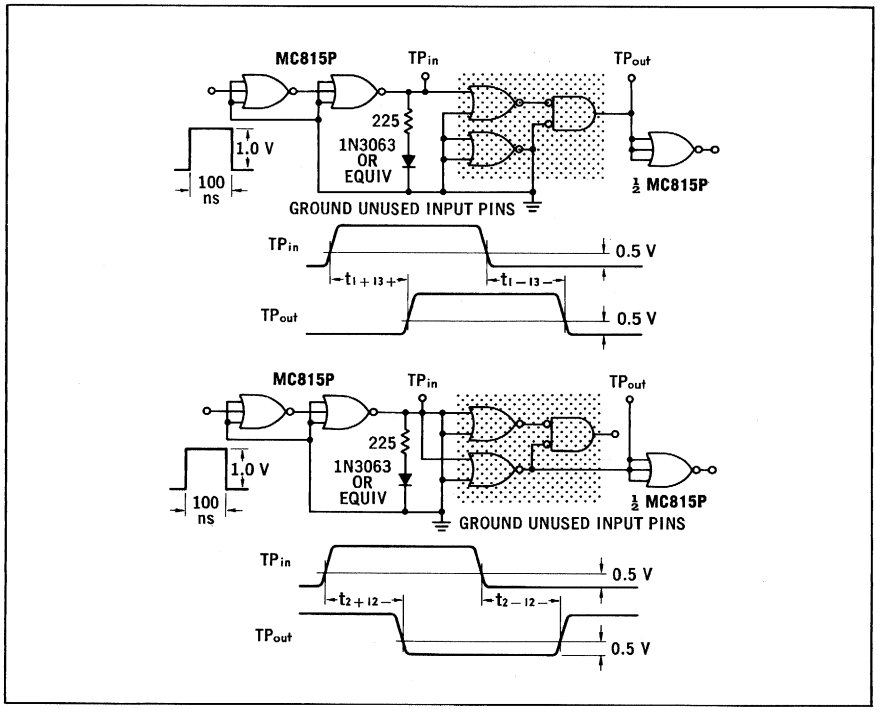


IF: $2 = \overline{1}$, & $3 = \overline{14}$
THEN: $12 = 1 \cdot 14$, & $13 = 1 \cdot \overline{14} + \overline{1} \cdot 14$

t_{pd} = 20 ns typ
P_D = 120 mW typ

NUMBER IN PARENTHESIS INDICATES MC775P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC875P LOADING FACTOR.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-adder only.
The other half-adder is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC875P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC775P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC875P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC775P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	14	-	11	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	3	-	↓	↓
		3	-		-		-			-		-		-			3	-	2	-		
		14	-		-		-			-		-		-			14	-	14	-		
Output Current	I_{A4}*	12	2.4	-	2.4	-	2.28	-	mAdc	-	-	-	-	-	-	-	-	12	-	2, 3	11	4
	I_{A5}†	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.5	-	mAdc	-	1, 2, 13	-	-	↓	↓
	I_{A5}†	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.5	-	mAdc	-	3,13,14	-	-		
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓
		13	-		-		-			-		-		-			-	12	1, 13	-		
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	2	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	↓
		13	-		-		-			-		-		-			-	-	1, 14	2, 3		
		13	-		-		-			-		-		-			-	-	2, 3	1, 14		
Switching Time	t																Pulse In	Pulse Out				
		2+12-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	2	12	-	-	11	4
		2-12+	-	-	-	30	-	-	↓	-	-	-	30	-	-	↓	2	12	-	-	↓	4
		1+13+	-	-	-	36	-	-		-	-	-	36	-	-		1	13	-	-		4, 12
		1-13-	-	-	-	36	-	-		-	-	-	36	-	-		1	13	-	-		4, 12

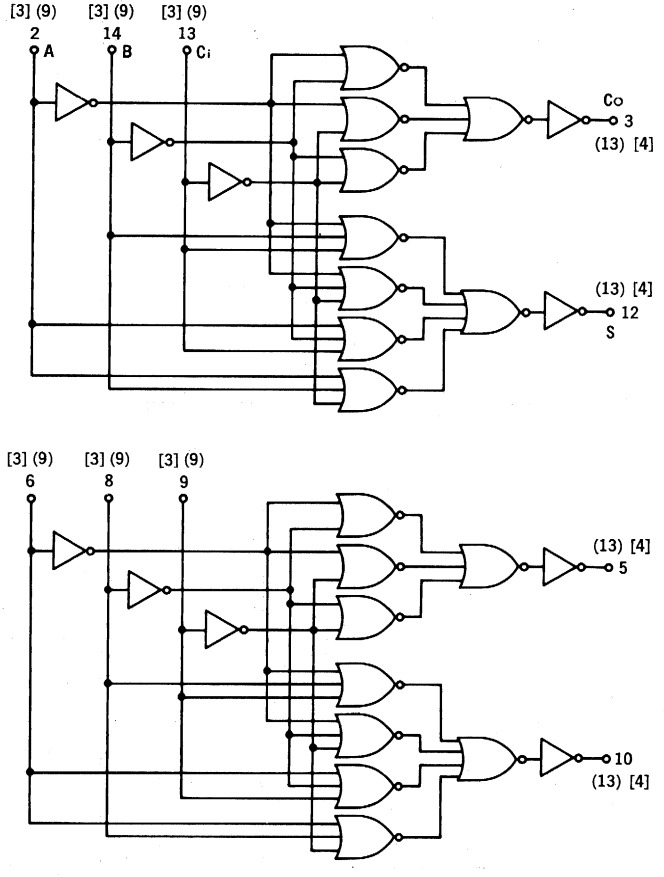
Ground inputs of half-adder not under test. Other pins not listed are left open.

* I_{AB} is symbol for MC775

† I_{A16} is symbol for MC775

MC796P • MC896P

Provides the SUM and CARRY functions while requiring only the AUGEND (A) and ADDEND (B) inputs with CARRY IN.



TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

POSITIVE LOGIC

$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

$S = ABC_i + A\overline{B}\overline{C_i} + \overline{A}\overline{B}C_i + \overline{A}B\overline{C_i}$

$t_{pd} = 60$ ns typ

$P_D = 84$ mW typ

NUMBER IN PARENTHESIS INDICATES M796P LOADING FACTOR.

NUMBER IN BRACKETS INDICATES MC896P LOADING FACTOR.

ELECTRICAL CHARACTERISTICS

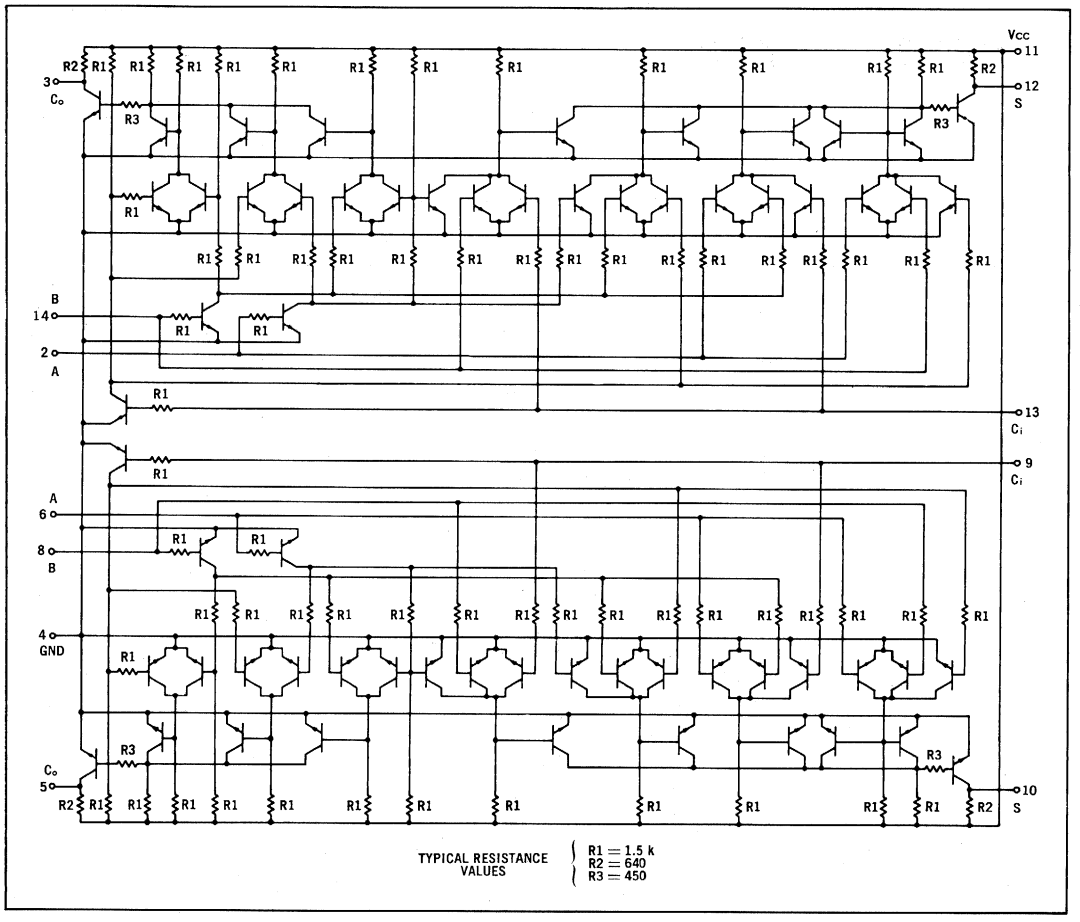
Test procedures are shown for one full adder only.
The other full adder is tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC896P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.800	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC796P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

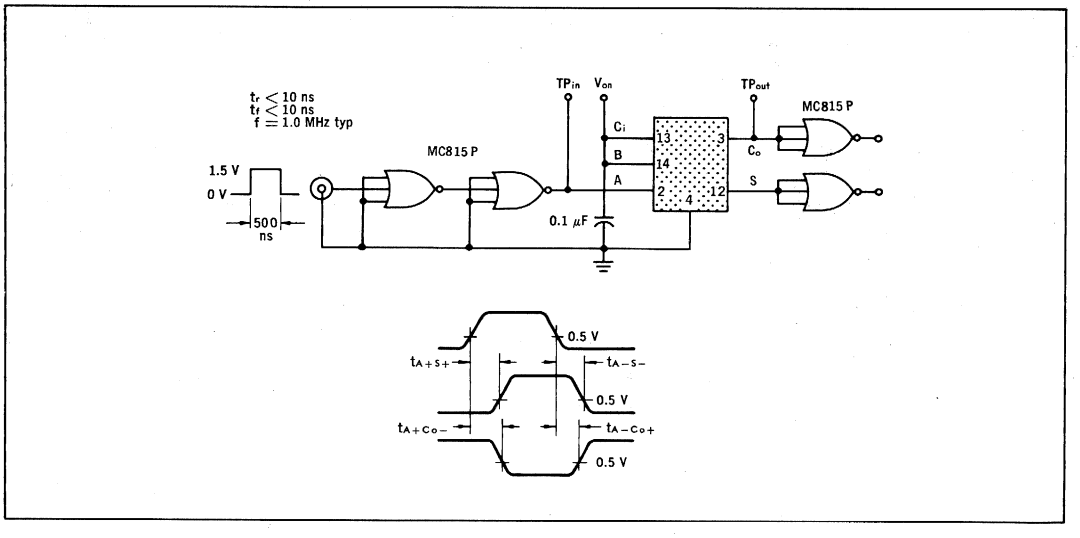
Characteristic	Symbol	Pin Under Test	MC896P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC796P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$3\ I_{in}$	2	-	1800	-	1800	-	1710	μAdc	-	1500	-	1500	-	1410	μAdc	2	-	-	-	11	4
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	13	-	-	-	↓	↓
		14	-		-		-			-		-		-			14	-	-	-		
Output Current	I_{A4}*	3	2.40	-	2.40	-	2.28	-	mAdc	2.15	-	2.15	-	2.03	-	mAdc	-	3,13,14	-	2	11	4
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	2,3,13	-	14	↓	↓
				-		-		-			-		-		-		-	2,3,14	-	13		
				-		-		-			-		-		-		-	(2,3,) (13,14)	-	-		
		12		-		-		-			-		-		-		-	12,13	-	2,14		
		↓		-		-		-			-		-		-		-	12,14	-	2,13		
				-		-		-			-		-		-		-	2,12	-	13,14		
				-		-		-			-		-		-		-	(2,12,) (13,14)	-	-		
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	-	2,13,14	11	4
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	2,14	↓	↓
			-		-		-			-		-		-			-	14	-	2,13		
			-		-		-			-		-		-			-	2	-	13,14		
		12	-		-		-			-		-		-			-	-	-	2,13,14		
		↓	-		-		-			-		-		-			-	13,14	-	2		
			-		-		-			-		-		-			-	2,14	-	13		
			-		-		-			-		-		-			-	2,14	-	13		
Switching Time																	Pulse In		Pulse Out			
	t	2+12+	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	2	13,14	12	-	11	4
		2-12-	-	-	-	75	-	-		-	-	-	75	-	-			-	12	-	↓	↓
		2+3+	-	-	-	85	-	-		-	-	-	85	-	-			13	3	14		
		2-3-	-	-	-	65	-	-		-	-	-	65	-	-		↓	13	3	14		
		14+12+	-	-	-	75	-	-		-	-	-	75	-	-		14	-	12	2,13		
		14-12-	-	-	-	75	-	-		-	-	-	75	-	-			-	12	2,13		
		14+3+	-	-	-	85	-	-		-	-	-	85	-	-		↓	13	3	2		
		14-3-	-	-	-	65	-	-		-	-	-	65	-	-			13	3			
		13+12-	-	-	-	70	-	-		-	-	-	70	-	-		13	14	12			
		13-12+	-	-	-	80	-	-		-	-	-	80	-	-			↓	12			
		13+3+	-	-	-	70	-	-		-	-	-	70	-	-				3			
		13-3-	-	-	-	80	-	-	↓	-	-	-	80	-	-	↓	↓	↓	3	↓	↓	↓

* Symbol is I_{A13} for MC796P.

Ground inputs of full adder not under test.
Other pins not listed are left open.

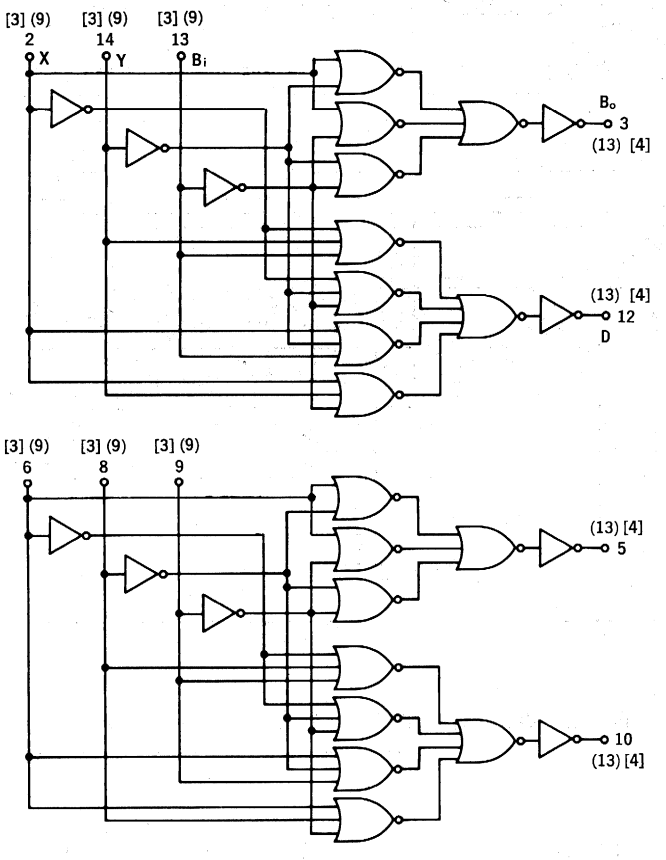


SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



MC797P • MC897P

Provides the DIFFERENCE and BORROW functions while requiring only MINUEND (X) and SUBTRAHEND (Y) inputs with BORROW IN.



TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

POSITIVE LOGIC

$D = YX\overline{B}_i + Y\overline{X}\overline{B}_i + \overline{Y}X\overline{B}_i + \overline{Y}\overline{X}B_i$

$B_o = \overline{Y}\overline{X}B_i + Y\overline{X}\overline{B}_i + Y\overline{X}B_i + YXB_i$

$t_{pd} = 60$ ns typ

$P_D = 84$ mW typ

NUMBER IN PARENTHESIS INDICATES MC797P LOADING FACTOR.

NUMBER IN BRACKETS INDICATES MC897P LOADING FACTOR.

ELECTRICAL CHARACTERISTICS

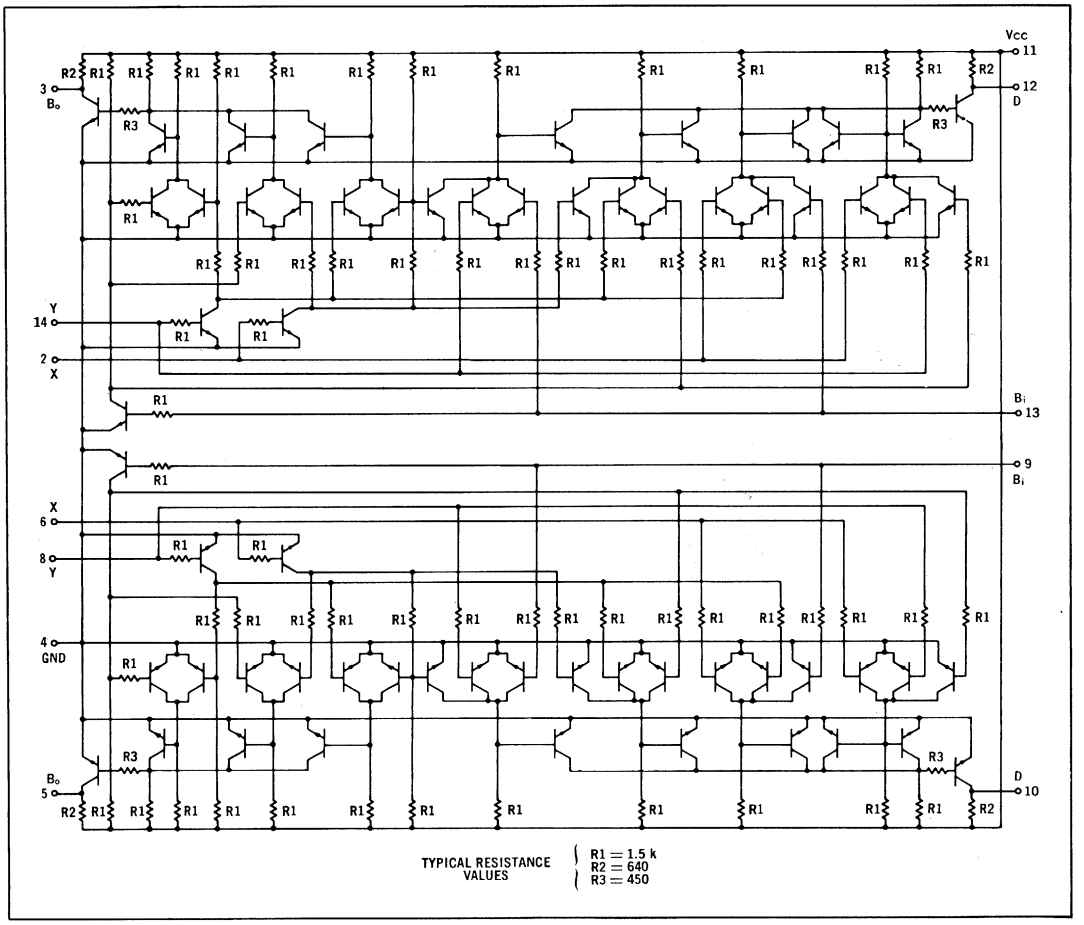
Test procedures are given for only one subtractor.
The other subtractor is tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC897P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.800	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC797P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

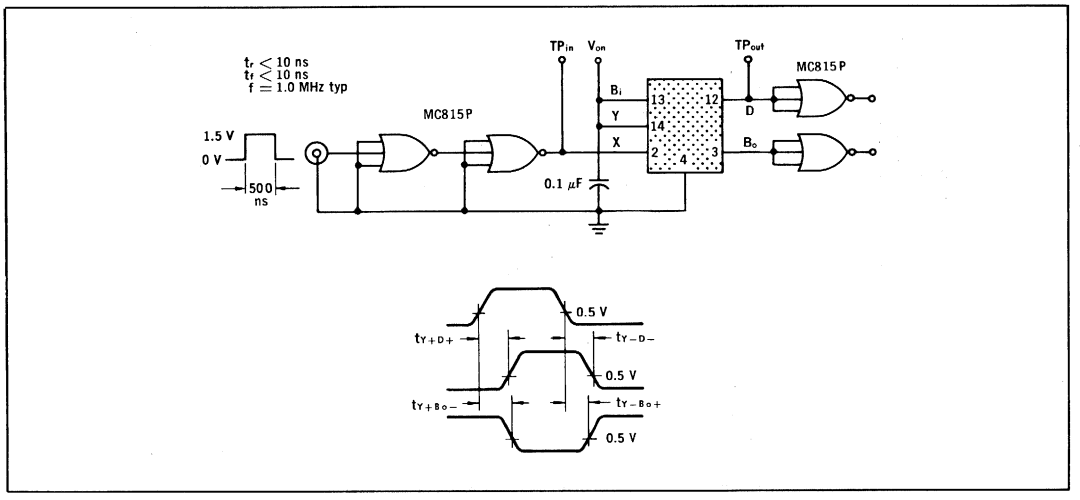
Characteristic	Symbol	Pin Under Test	MC897P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC797P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$3\ I_{in}$	2	-	1800	-	1800	-	1710	μAdc	-	1500	-	1500	-	1410	μAdc	2	-	-	-	11	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	13	-	-	-	↓	↓
		14	-		-		-			-		-		-			14	-	-	-		
Output Current	I_{A4}*	3	2.40	-	2.40	-	2.28	-	mAdc	2.15	-	2.15	-	2.03	-	mAdc	-	{2,3,13,14}	-	-	11	4
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3,13	-	2,14	↓	↓
				-		-		-			-		-		-		-	3,14	-	2,13		
		12		-		-		-			-		-		-		-	12,13	-	2,14		
		↓		-		-		-			-		-		-		-	12,14	-	2,13		
				-		-		-			-		-		-		-	2,12	-	13,14		
				-		-		-			-		-		-		-	{2,12,13,14}	-	-		
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2,13	-	14	11	4
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2,14	-	13	↓	↓
			-		-		-			-		-		-			-	-	-	2,13,14		
		12	-		-		-			-		-		-			-	-	-	2,13,14		
		↓	-		-		-			-		-		-			-	13,14	-	2		
			-		-		-			-		-		-			-	2,14	-	13		
			-		-		-			-		-		-			-	2,13	-	14		
Switching Time																	Pulse In		Pulse Out			
	t	2+12+	-	-	-	60	-	-	ns	-	-	-	60	-	-	ns	2	13,14	12	-	11	4
		2-12-	-	-	-	60	-	-		-	-	-	60	-	-		↓	↓	12	-	↓	↓
		2+3+	-	-	-	65	-	-		-	-	-	65	-	-				3	-		
		2-3-	-	-	-	60	-	-		-	-	-	60	-	-				3	-		
		14+12+	-	-	-	↓	-	-		-	-	-	↓	-	-		14	-	12	2,13		
		14-12-	-	-	-		-	-		-	-	-		-	-		↓	-	12	2,13		
		14+3-	-	-	-	65	-	-		-	-	-	65	-	-			13	3	2		
		14-3+	-	-	-	60	-	-		-	-	-	60	-	-		↓	↓	3	↓		
		13+12-	-	-	-	↓	-	-		-	-	-	↓	-	-		13		12			
		13-12+	-	-	-		-	-		-	-	-		-	-		↓	↓	12			
		13+3+	-	-	-		-	-		-	-	-		-	-			2,14	3	-		
		13-3-	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	↓	2,14	3	-	↓	↓

* Symbol for MC797P is I_{A13}.

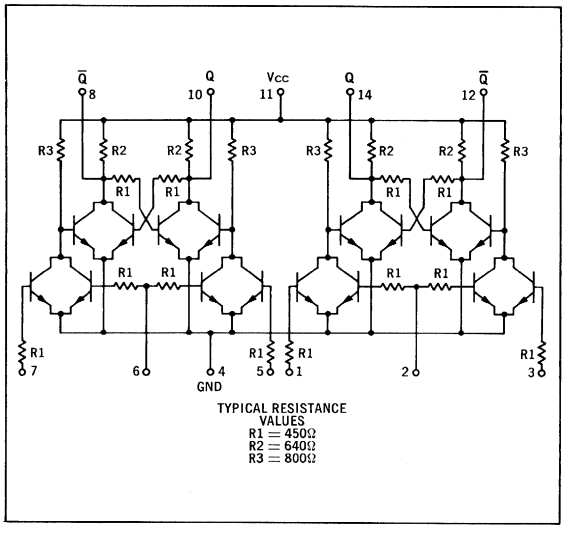
Ground input pins of subtractor not under test.
Other pins not listed are left open.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

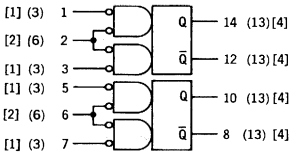


MC784P • MC884P



TYPICAL RESISTANCE VALUES
R1 = 450Ω
R2 = 640Ω
R3 = 800Ω

Two half-shift registers in a single package. Each is a bistable storage element. Eg., information coming in on pins 1 and 3 will be transferred to pins 14 and 12 when the gating signal, pin 2, goes low. If all three inputs, 1, 2, and 3, are low, the outputs, 14 and 12, will both be low.

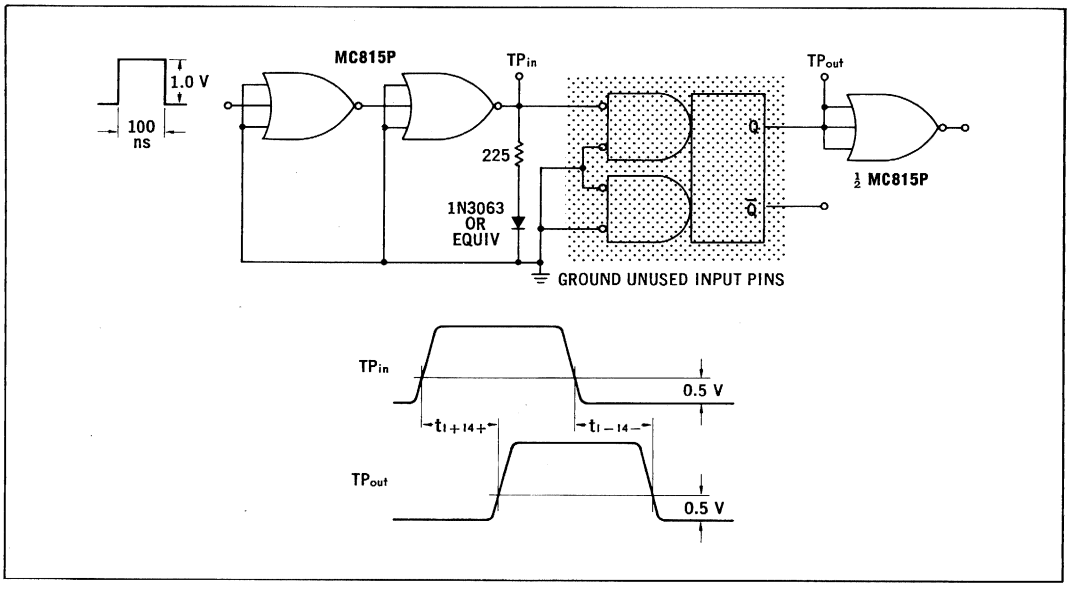


NUMBER IN PARENTHESIS INDICATES MC784P LOADING FACTOR

NUMBER IN BRACKETS INDICATES MC884P LOADING FACTOR

t_{pd} = 22 ns typ
P_D = 120 mW typ

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-shift register only.
The other half-shift register is tested in the same manner.

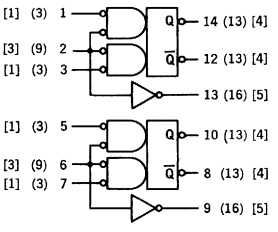
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC884P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC784P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC884P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC784P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	4
	$2I_{in}$	2	-	1200	-	1200	-	1140	↓	-	1000	-	1000	-	940	↓	2	-	1, 3	-	↓	↓
	I_{in}	3	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	3	-	2	-	↓	↓
Output Current	I_{A4}*	12	2.4	-	2.4	-	2.28	-	mAdc	2.15	-	2.15	-	2.03	-	mAdc	-	2, 12	-	-	11	4, 14†
		12	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3, 12	-	-	↓	4
		14		-		-		-			-		-		-		-	2, 14	-	-		4, 12†
		14		-		-		-			-		-		-		-	1, 14	-	-		4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	2, 3	-	11	4
		14	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	12	1, 2	-	11	4
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1, 2, 3	-	11	4, 12†
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	2, 3	↓	4, 14
		14	-		-		-			-		-		-			-	-	1, 2, 3	-		4, 14†
		14	-		-		-			-		-		-			-	-	-	1, 2		4
Switching Time	t	1+14+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In 1	Pulse Out 14	-	-	11	4, 12
		1-14-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	14	-	-	11	4, 12

Ground input pins of half-register not under test. Other pins not listed are left open. † Silicon diode to ground. * Symbol is I_{A13} for the MC784P.

MC783P • MC883P

Dual half-shift registers each with built-in inverter, in a single package. Information coming in on pins 1 and 2 will be transferred to pins 14 and 12 when the gating signal, pin 2, goes low. If all three inputs, 1, 2, and 3, are low, the outputs, 12 and 14, will both be low.

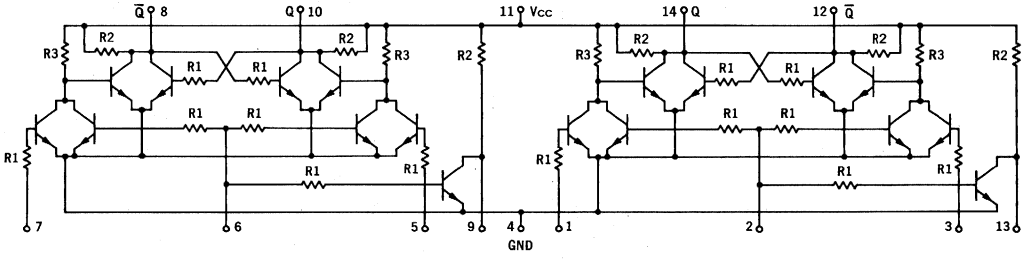


$14 = \overline{12}\ (1 + 2)$
$12 = \overline{14}\ (3 + 2)$

t_{pd} = 22 ns typ
P_D = 140 mW typ

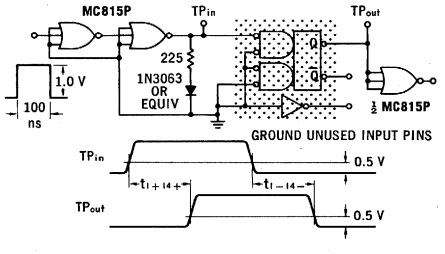
NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC783P

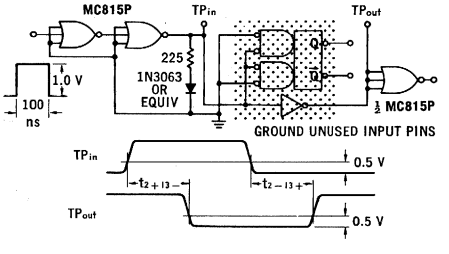
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC883P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-shift register only.
The other half-shift register is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC883P	0°C	0.960	0.930	1.80	0.570	3.60
MC883P	+25°C	0.910	0.880	1.80	0.500	3.60
MC883P	+75°C	0.820	0.790	1.80	0.450	3.60
MC783P	+15°C	0.865	0.865	1.80	0.475	3.60
MC783P	+25°C	0.850	0.850	1.80	0.460	3.60
MC783P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC883P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC783P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	4
	$3I_{in}$	2	-	1800	-	1800	-	1710	↓	-	1500	-	1500	-	1410	↓	2	-	1, 3	-	↓	↓
	I_{in}	3	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	3	-	2	-	↓	↓
Output Current	I_{A4}*	12	2.4	-	2.4	-	2.28	-	mAdc	2.15	-	2.15	-	2.03	-	mAdc	-	2, 12	-	-	11	4, 14†
	I_{A4}*	12	2.4	-	2.4	-	2.28	-	↓	2.15	-	2.15	-	2.03	-	↓	-	3, 12	-	-	↓	4
	I_{A5}**	13	3.0	—	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.5	-	↓	-	13	-	2	↓	4
	I_{A4}*	14	2.4	-	2.4	-	2.28	-	↓	2.15	-	2.15	-	2.03	-	↓	-	2, 14	-	-	↓	4, 12†
	I_{A4}*	14	2.4	-	2.4	-	2.28	-	↓	2.15	-	2.15	-	2.03	-	↓	-	1, 14	-	-	↓	4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	2, 3	-	11	4
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	↓
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	12	1, 2	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1, 2, 3	-	11	4, 12†
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	2, 3	↓	4, 14
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2	-	↓	4
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1, 2, 3	-	↓	4, 14†
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 2	↓	4, 12
Switching Time	t	2+13-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In 2	Pulse Out 13	-	-	11	4
		2-13+	-	-	-	40	-	-	↓	-	-	-	40	-	-	↓	2	13	-	-	↓	4
		1+14+	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	1	14	-	-	↓	4, 12
		1-14-	-	-	-	24	-	-	↓	-	-	-	24	-	-	↓	1	14	-	-	↓	4, 12

Ground input pins of half-shift register not under test. Other pins not listed are left open. * Symbol is I_{A13} for MC783P. ** Symbol is I_{A16} for MC783P †Silicon diode to ground.

COMMERCIAL

MRTL

INTEGRATED CIRCUITS

LOW-POWER
AND
MEDIUM-POWER

MC700 SERIES

MILLIWATT AND MEDIUM-POWER

COMMERCIAL MRTL

INTEGRATED CIRCUITS

INDEX

In this series of MRTL logic circuits, medium and low-power devices are combined and specified for compatible application in commercial usages. Medium-power devices have loading factors normalized for compatibility with low-power for ease of mixing the two power levels in a system.

INDEX

DEVICE		POWER	PACKAGE
GATES			
MC703	3-Input Gates	MRTL	F, G
MC707	4-Input Gates	MRTL	F, G
MC711	4-Input Gates	mW MRTL	F, G
MC728	5-Input Gates	mW MRTL	F, G
MC729	5-Input Gates	MRTL	F, G
MC710	Dual 2-Input Gates	mW MRTL	F, G
MC714	Dual 2-Input Gates	MRTL	F, G
MC715	Dual 3-Input Gates	MRTL	F, G
MC718	Dual 3-Input Gates	mW MRTL	F, G
MC719	Dual 4-Input Gate	mW MRTL	F
MC725	Dual 4-Input Gate	MRTL	F
MC792	Triple 3-Input Gate	MRTL	F
MC793	Triple 3-Input Gate	mW MRTL	F
MC717	Quad 2-Input Gate	mW MRTL	F
MC724	Quad 2-Input Gate	MRTL	F
BUFFERS			
MC700	Buffers	MRTL	F, G
MC709	Buffers	mW MRTL	F, G
MC781	Dual Buffer	mW MRTL	G
MC799	Dual Buffers	MRTL	F, G
MC798	Dual 2-Input Buffer	mW MRTL	F
MC788	Dual 3-Input Buffer	MRTL	F
INVERTERS			
MC727	Quad Inverters	MRTL	F, G
MC789	Hex Inverter	MRTL	F
EXPANDERS			
MC721	Dual 2-Input Expanders	mW MRTL	F, G
MC786	Dual 4-Input Expander	MRTL	F
MC785	Quad 2-Input Expander	MRTL	F

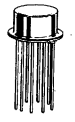
DEVICE		POWER	PACKAGE
COUNTER ADAPTERS			
MC701	Counter Adapter	MRTL	G
ADDERS			
MC704	Half Adders	MRTL	F, G
MC708	Half Adders	mW MRTL	F, G
MC712	Half Adders	mW MRTL	F, G
MC775	Dual Half Adder	MRTL	F
HALF-SHIFT REGISTERS			
MC705	Half-Shift Registers with Inverter	MRTL	F, G
MC706	Half-Shift Registers without Inverter	MRTL	F, G
MC783	Dual Half-Shift Register with Inverter	MRTL	F
MC784	Dual Half-Shift Register without Inverter	MRTL	F
FLIP-FLOPS			
MC702	R-S Flip-Flop	MRTL	G
MC720	J-K Flip-Flops	mW MRTL	F, G
MC722	J-K Flip-Flops	mW MRTL	F, G
MC723	J-K Flip-Flops	MRTL	F, G
MC726	J-K Flip-Flops	MRTL	F, G
MC774	J-K Flip-Flop	MRTL	G
MC782	J-K Flip-Flop	mW MRTL	G
MC776	Dual J-K Flip-Flop	mW MRTL	F
MC790	Dual J-K Flip-Flop	MRTL	F
MC791	Dual J-K Flip-Flop	MRTL	F
MC713	Type D Flip-Flops	mW MRTL	F, G
MC778	Dual Type D Flip-Flop	mW MRTL	F

NUMERICAL INDEX
(Functions and Characteristics)

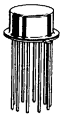
V_{CC} = 3.6 V ±10%, T_A = 25°C

Function	Type ① +15 to +55°C	Case	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg
MRTL					
Buffer	MC700	72,96	80	20	25/50 ②
Counter Adapter	MC701	96	16	22	80
R-S Flip-Flop	MC702	96	13	14	32
3-Input NOR Gate	MC703	72,96	16	12	28/7.5 ②
Half Adder	MC704	72,96	16	14	65
Half-Shift Register	MC705	72,96	13	22	75
Half-Shift Register (w/o Inverter)	MC706	72,96	13	22	52
4-Input NOR Gate	MC707	72,96	16	12	30/7.5 ②
Dual 2-Input NOR Gate	MC714	72,96	16	12	50/15 ②
Dual 3-Input NOR Gate	MC715	72,96A	16	12	55/15 ②
J-K Flip-Flop	MC723	72,96	10	35	91/79 ④
Quad 2-Input NOR Gate	MC724	83	16	12	100/30 ②
Dual 4-Input NOR Gate	MC725	83	16	12	60/15 ②
J-K Flip-Flop	MC726	72,96A	16	35	100/86 ④
Quad Inverter	MC727	72,96A	16	12	87/30 ②
5-Input NOR Gate	MC729	72,96	16	12	33/7.5 ②
Quad Exclusive OR Gate	MC771	83	16	12	87
J-K Flip-Flop	MC774	96	16	35	100/86 ④
Dual Half Adder	MC775	83	16	20	120
Dual Half Shift Register	MC783	83	13	22	140
Dual Half Shift Register w/Inverter	MC784	83	13	22	100
Quad 2-Input Expander	MC785	83	–	12	20/ – ②
Dual 4-Input Expander	MC786	83	–	12	20/ – ②
Dual 3-Input Buffer, non-inverting	MC788	83	80	24	145/56 ②
Hex Inverter	MC789	83	16	12	130/15 ②
Dual J-K Flip-Flop	MC790	83	10	35	182/158 ④
Dual J-K Flip-Flop	MC791	83	16	40	190/160 ④
Triple 3-Input NOR Gate	MC792	83	16	12	82/24 ②
Dual Full Adder	MC796	83	13	60	84
Dual Full Subtractor	MC797	83	13	60	84
Dual Buffer	MC799	72,96A	80	20	50/100 ②
Hex Expander	MC9719	83	–	12	13/ – ②
mW MRTL					
Half Adder	MC708	72,96	4	60	19/12.5 ②
2-Input Buffer	MC709	72,96	30	57	7.0/23 ②
Dual 2-Input NOR Gate	MC710	72,96	4	27	10/2.5 ②
Dual 4-Input OR/NOR Gate	MC711	72,96	4	60	8.0/5.5 ②
Half Adder	MC712	72,96	4	66	15.5/10.5 ②
Type D Flip-Flop	MC713	72,96	3	75	24/17.5 ③
Quad 2-Input NOR Gate	MC717	83	4	27	20/5.0 ②
Dual 3-Input NOR Gate	MC718	72,96A	4	27	12/2.5 ②
Dual 4-Input NOR Gate	MC719	83	4	27	13/2.5 ②
J-K Flip-Flop	MC720	72,96	2	50	20.5/14.5 ④
Dual 2-Input Gate Expander	MC721	72,96	–	27	3.0/ – ②
J-K Flip-Flop	MC722	72,96A	4	70	24/20 ④
5-Input NOR Gate	MC728	72,96	4	27	7.5/1.0 ②
Dual J-K Flip-Flop	MC776	83	2	50	41/29 ④
Dual Type D Flip-Flop	MC778	83	3	60	48/35 ③
Dual Buffer	MC781	96	30	57	14/46 ②
J-K Flip-Flop	MC782	96	2	80	23/21 ④
Triple 3-Input NOR Gate	MC793	83	4	27	18/3.5 ②
Dual 2-Input Buffer	MC798	83	30	57	14/46 ②
Quad 2-Input Expander	MC9721	83	–	27	20/ – ②

① G suffix denotes Metal Can, F suffix denotes Flat Package; i.e., MC718G = Metal Can, MC718F = Flat Package.
② Inputs High/Inputs Low.
③ Direct Set and Direct Clear Low, All Other Inputs High/All Inputs Low
④ Only Clock Input High/Inputs Low

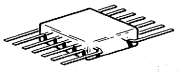


TO-99



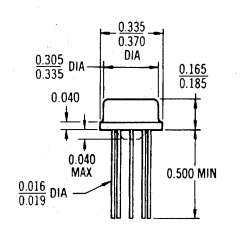
TO-100

TO-91

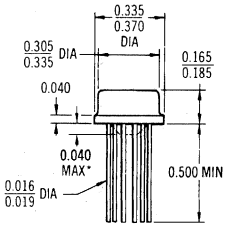


TO-86

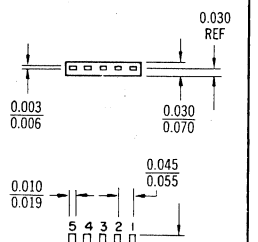
OUTLINE DIMENSIONS



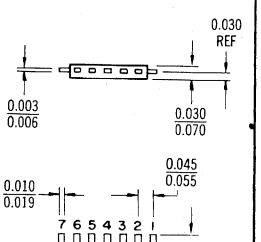
Pin 4 connected to case.



Pin 5 connected to case.



Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.



Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

TEST CONDITION TOLERANCES $V_{BOT} = \pm 10$ mV $V_{CC} = \pm 10$ mV $V_{in} = \pm 2$ mV $V_R = \pm 1\%$ $V_{on} = \pm 2$ mV $V_{off} = \pm 2$ mV

GENERAL RULES

- Testing tables shown in the MC900/800 MRTL and the MC908/808 mW MRTL sections of this volume may be utilized for testing MC700F and G commercial series devices. Pin number configurations are the same. MC700 series forcing functions and test limits are shown on page 6-247.
- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- For ease of mixing MRTL and mW MRTL in the same system, the loading factors are normalized in accordance with the input currents being driven.
- Any number of gates may be paralleled; the input loading is increased by 1/4 load if only one gate is connected to V_{CC}.
- When paralleling gates with V_{CC} connected, a maximum of 4 outputs may be paralleled, increasing the input loading factor by 2.33.
- If the counter adapter is paralleled with another circuit, the output drive capability must be reduced by two loads. The reason for this drive reduction is the 1280-ohm resistance that connects the output terminals on the counter adapter.
- All unused input pins should be returned to ground.
- EXPANDER RULES:
  1. The MC785F, MC786F and MC9719F MRTL expanders can be used to expand medium-power MRTL output nodes only.
  2. When using the MC785F, MC786F or MC9719F subtract 0.5 from the output loading factor of the medium-power MRTL expanded gate for each expander node that is connected; also increase the input loading factor of the medium-power expanded gate by a factor of 1.33.

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Logic Input Voltage		±4.0	Vdc
Power Supply Voltage (Pulsed ≤ 1 second)		+12	Vdc
Operating Temperature Range MC700G/F Series	T_A	+15 to +55	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Milliwatt MRTL			MRTL			Unit
	+15°C	+25°C	+55°C	+15°C	+25°C	+55°C	
I_{A3}	0.420	0.420	0.420	–	–	–	mAdc min
I_{A4}	0.570	0.570	0.570	–	–	–	mAdc min
I_{A10}	–	–	–	1.65	1.65	1.65	mAdc min
I_{A13}	–	–	–	2.15	2.15	2.03	mAdc min
I_{A16}	–	–	–	2.65	2.65	2.5	mAdc min
I_{AB}	5.0	5.0	5.0	13.5	13.75	12.5	mAdc min
I_{CEX}	50	50	100	225	225	250	μAdc max
I_{in}	0.150	0.150	0.150	0.500	0.500	0.470	mAdc max
2 I_{in}	0.300	0.300	0.300	1.0	1.0	0.94	mAdc max
V_{out}	0.400	0.300	0.320	0.400	0.300	0.320	Vdc max
V_{CE}	0.220	0.230	0.320	0.300	0.290	0.320	Vdc max
TEST CONDITIONS							
V_{BOT}	1.8	1.8	1.8	1.8	1.8	1.8	Vdc
V_{CC}	3.6	3.6	3.6	3.6	3.6	3.6	Vdc
V_{in}	0.865	0.850	0.800	0.865	0.850	0.800	Vdc
V_{off}	0.475	0.460	0.430	0.475	0.460	0.430	Vdc
V_{on}	0.865	0.850	0.800	0.865	0.850	0.800	Vdc
V_R*	4600	4800	5000	640	640	640	Ohms

*Resistor value to V_{CC}

DEFINITIONS

I_{A2}, I_{A3}, I_{A4}, I_{A5}, I_{A10}, I_{A13}, I_{A16} Minimum available output current from a device with an output loading factor of 2, 3, 4, 5, 10, 13, and 16 respectively. Output voltage not to fall below the value of V_{on}.

I_{AB} Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.

I_{AM} The maximum available current from the output of a Dual Gate.

I_{CEX} Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

I_{in} Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

1.8 I_{in} Current drawn from the V_{in} supply by the Toggle pin of the Flip-Flop.

2 I_{in} Maximum input current drawn by one input of a device with 2 bases internally tied together.

I_L Isolation leakage current.

I_O Output load current.

V_{BOT} A high value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} Supply voltage.

$V_{CE(sat)}$ Maximum saturation voltage with V_{BOT} applied to the input.

V_{in} Minimum high level voltage applied to the input of a device.

V_{LL} A supply voltage low enough to allow flow of leakage currents only.

V_{off} The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} The maximum output voltage with V_{on} applied to the input.

V_R Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

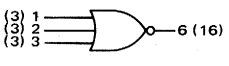
COMMERCIAL MRTL DEVICES AVAILABLE IN METAL CANS

The logic diagrams on these pages describe the MC700 Series Commercial MRTL integrated circuits available in metal cans, and permit quick selection of those circuits required for the implementation of a commercial system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal). Medium-power devices have loading factors normalized for compatability with the low-power devices for ease of mixing the two power levels in a system.

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the unit. Loading data are valid over the temperature range of +15 to +55°C, with V_{CC} = 3.6 V ±10%. For the TO-99 metal can, V_{CC} is applied to pin 8, with ground connected to pin 4. For the TO-100 metal can, V_{CC} is applied to pin 10, with ground connected to pin 5.

GATES

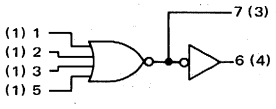
MC703G 3-Input Gate
(medium-power)



$6 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 28 mW (Input High)
7.5 mW (Inputs Low)

MC711G 4-Input Gate
(milliwatt)

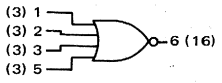


$7 = \overline{1 + 2 + 3 + 5}$

$6 = 1 + 2 + 3 + 5$

t_{pd} = 60 ns
P_D = 8.0 mW (Input High)
5.5 mW (Inputs Low)

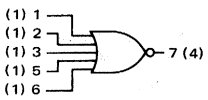
MC707G 4-Input Gate
(medium-power)



$6 = \overline{1 + 2 + 3 + 5}$

t_{pd} = 12 ns
P_D = 30 mW (Input High)
7.5 mW (Inputs Low)

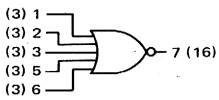
MC728G 5-Input Gate
(milliwatt)



$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 27 ns
P_D = 7.5 mW (Input High)
1.0 mW (Inputs Low)

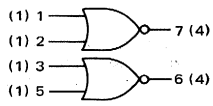
MC729G 5-Input Gate
(medium-power)



$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 33 mW (Input High)
7.5 mW (Inputs Low)

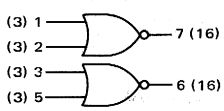
MC710G Dual 2-Input Gate
(milliwatt)



$7 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 10 mW (Input High)
2.5 mW (Inputs Low)

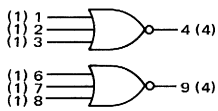
MC714G Dual 2-Input Gate
(medium-power)



$7 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 50 mW (Input High)
15 mW (Inputs Low)

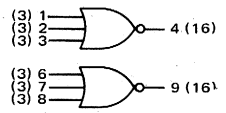
MC718G Dual 3-Input Gate
(milliwatt)



$4 = \overline{1 + 2 + 3}$

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5 mW (Inputs Low)

MC715G Dual 3-Input Gate
(medium-power)

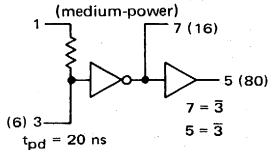


$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

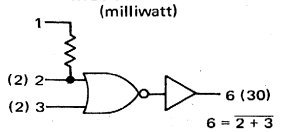
BUFFERS

MC700G Buffer
(medium-power)



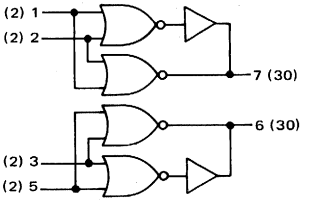
$7 = \overline{3}$
$5 = \overline{3}$
t_{pd} = 20 ns
P_D = 25 mW (Input High)
50 mW (Inputs Low)

MC709G Buffer
(milliwatt)



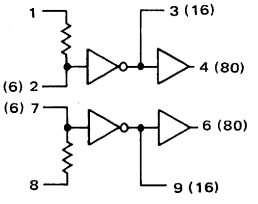
$6 = \overline{2 + 3}$
t_{pd} = 57 ns
P_D = 7.0 mW (Input High)
23 mW (Inputs Low)

MC781G Dual Buffer
(milliwatt)



$7 = \overline{1 + 2}$
t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 mW (Inputs Low)

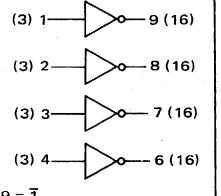
MC799G Dual Buffer
(medium-power)



$3 = \overline{2}$
$4 = \overline{2}$
t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

INVERTER

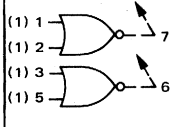
MC727G Quad Inverter
(medium-power)



$9 = \overline{1}$
t_{pd} = 12 ns
P_D = 87 mW (Input High)
30 mW (Inputs Low)

EXPANDER

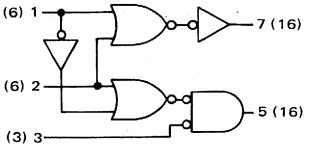
MC721G
Dual 2-Input Expander
(milliwatt)



t_{pd} = 27 ns
P_D = 3.0 mW (Input High)

COUNTER ADAPTER

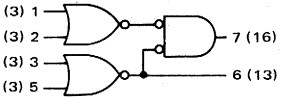
MC701G Counter Adapter
(medium-power)



$7 = 1 + 2$
$5 = (\overline{1} + 2)\,\overline{3}$
t_{pd} = 22 ns
P_D = 80 mW

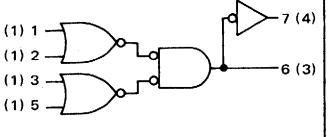
HALF ADDERS

MC704G Half Adder
(medium-power)



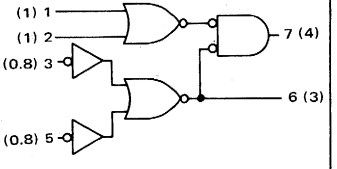
IF: $3 = \overline{1}$, & $5 = \overline{2}$
THEN: $6 = 1 \cdot 2$
$7 = 1 \cdot \overline{2} + \overline{1} \cdot 2$
$7 = (1 + 2)\,(3 + 5)$
$6 = \overline{3 + 5}$
t_{pd} = 14 ns
P_D = 65 mW

MC712G Half Adder
(milliwatt)



$7 = (1 + 2)\,(3 + 5)$
$6 = \overline{1} \cdot \overline{2} + \overline{3} \cdot \overline{5}$
t_{pd} = 66 ns
P_D = 15.5 mW (Input High)
10.5 mW (Inputs Low)

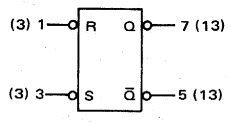
MC708G Half Adder
(milliwatt)



$7 = (\overline{\overline{3} + \overline{5}})$
$6 = (1 + 2)\,(\overline{3} + \overline{5})$
t_{pd} = 60 ns
P_D = 19 mW (Input High)
12.5 mW (Inputs Low)

FLIP-FLOPS

MC702G R-S Flip-Flop
(medium-power)



t_{pd} = 14 ns
P_D = 32 mW

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC722 and MC726 only

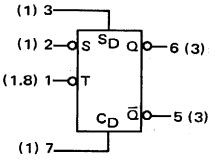
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC713G Type D Flip-Flop
(milliwatt)



t_{pd} = 75 ns
P_D = 24 mW (Direct Set and Direct Clear Inputs Low, All other Inputs High)
17.5 mW (All Inputs Low)

DIRECT INPUT OPERATION ①

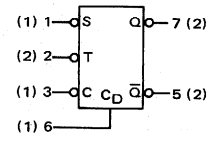
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n		t_{n+1}	
S		Q	$\bar{Q}$
1		1	0
0		0	1

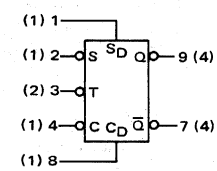
1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
   0 = low state
   1 = high state
   t_n = time period prior to negative transition of pulse
   t_{n+1} = time period subsequent to negative transition of clock pulse

MC720G J-K Flip-Flop
(milliwatt)



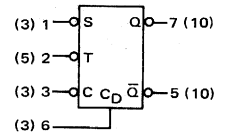
t_{pd} = 50 ns
P_D = 20.5 mW (Only Clock Input High)
14.5 mW (Inputs Low)

MC722G J-K Flip-Flop
(milliwatt)



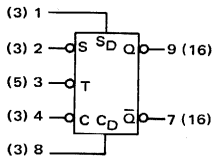
t_{pd} = 70 ns
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

MC723G J-K Flip-Flop
(medium-power)



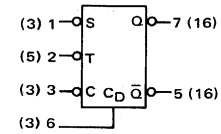
f_{Tog} = 4.0 MHz
t_{pd} = 30 ns
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

MC726G J-K Flip-Flop
(medium-power)



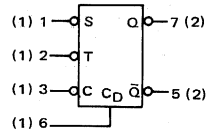
f_{Tog} = 4.0 MHz
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

MC774G J-K Flip-Flop
(medium-power)



t_{pd} = 35 ns
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

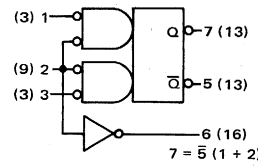
MC782G J-K Flip-Flop
(milliwatt)



t_{pd} = 80 ns
P_D = 23 mW (Only Clock Input High)
21 mW (Inputs Low)

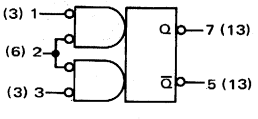
HALF-SHIFT REGISTERS

MC705G Half-Shift Register
(medium-power)



7 = $\bar{5}$ (1 + 2)
5 = $\bar{7}$ (2 + 3)
6 = $\bar{2}$
t_{pd} = 22 ns
P_D = 75 mW

MC706G Half-Shift Register
(without inverter—medium-power)



7 = $\bar{5}$ (1 + 2)
5 = $\bar{7}$ (2 + 3)
t_{pd} = 22 ns
P_D = 52 mW

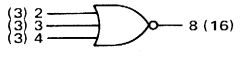
COMMERCIAL MRTL DEVICES AVAILABLE IN FLAT PACKAGES

The logic diagrams shown on these pages describe the MC700 Series Commercial MRTL integrated circuits available in flat packages, and permit quick selection of those circuits required for implementation of a commercial system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal). Medium-power devices have loading factors normalized for compatability with the low-power devices for ease of mixing the two power levels in a system.

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the unit. Loading data are valid over the temperature range of +15 to +55°C, with V_{CC} = 3.6 V ±10%. For the TO-91 flat package, V_{CC} is applied to pin 10, with ground connected to pin 5. For the TO-86 flat package, V_{CC} is applied to pin 14, with ground connected to pin 7.

GATES

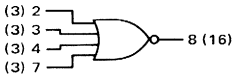
MC703F 3-Input Gate
(medium-power)



$8 = \overline{2 + 3 + 4}$

t_{pd} = 12 ns
P_D = 28 mW (Input High)
7.5 mW (Inputs Low)

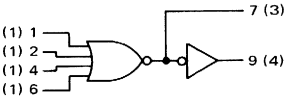
MC707F 4-Input Gate
(medium-power)



$8 = \overline{2 + 3 + 4 + 7}$

t_{pd} = 12 ns
P_D = 30 mW (Input High)
7.5 mW (Inputs Low)

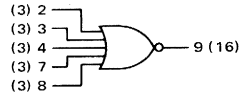
MC711F 4-Input Gate
(milliwatt)



$7 = \overline{1 + 2 + 4 + 6}$
$9 = 1 + 2 + 4 + 6$

t_{pd} = 60 ns
P_D = 8.0 mW (Input High)
5.5 mW (Inputs Low)

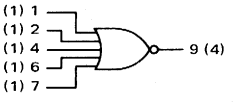
MC729F 5-Input Gate
(medium-power)



$9 = \overline{2 + 3 + 4 + 7 + 8}$

t_{pd} = 12 ns
P_D = 33 mW (Input High)
7.5 mW (Inputs Low)

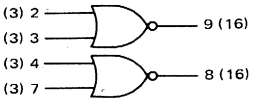
MC728F 5-Input Gate
(milliwatt)



$9 = \overline{1 + 2 + 4 + 6 + 7}$

t_{pd} = 27 ns
P_D = 7.5 mW (Input High)
1.0 mW (Inputs Low)

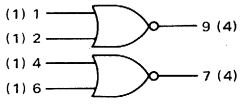
MC714F Dual 2-Input Gate
(medium-power)



$9 = \overline{2 + 3}$

t_{pd} = 12 ns
P_D = 50 mW (Input High)
15 mW (Inputs Low)

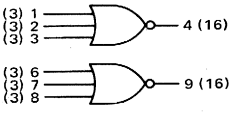
MC710F Dual 2-Input Gate
(milliwatt)



$9 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 10 mW (Input High)
2.5 mW (Inputs Low)

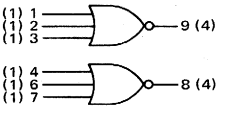
MC715F Dual 3-Input Gate
(medium-power)



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

MC718F Dual 3-Input Gate
(milliwatt)



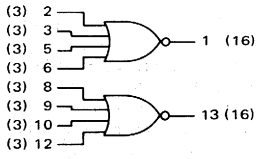
$9 = \overline{1 + 2 + 3}$

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5 mW (Inputs Low)

(continued)

GATES (continued)

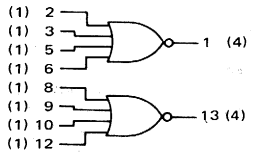
MC725F Dual 4-Input Gate
(medium-power)



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 60 mW (Input High)
15 mW (Inputs Low)

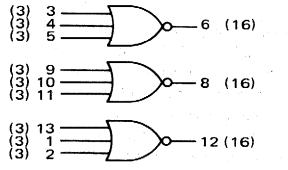
MC719F Dual 4-Input Gate
(milliwatt)



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 27 ns
P_D = 13 mW (Input High)
2.5 mW (Inputs Low)

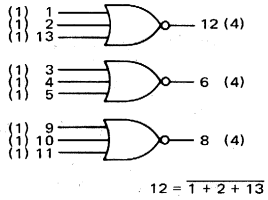
MC792F Triple 3-Input Gate
(medium-power)



$6 = \overline{3 + 4 + 5}$

t_{pd} = 12 ns
P_D = 82 mW (Input High)
24 mW (Inputs Low)

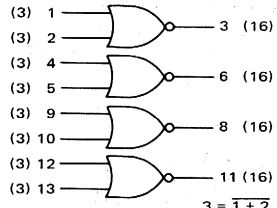
MC793F Triple 3-Input Gate
(milliwatt)



$12 = \overline{1 + 2 + 13}$

t_{pd} = 27 ns
P_D = 18 mW (Inputs High)
3.5 mW (Inputs Low)

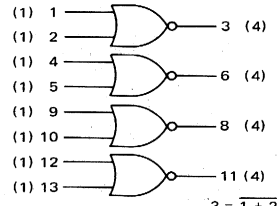
MC724F Quad 2-Input Gate
(medium-power)



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 100 mW (Input High)
30 mW (Inputs Low)

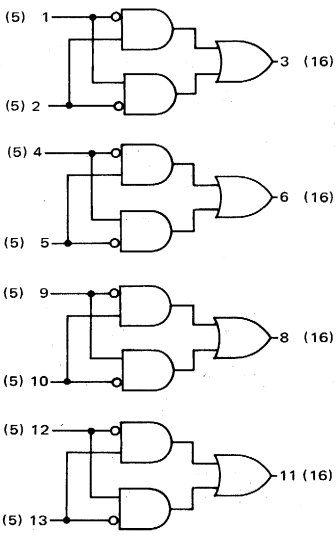
MC717F Quad 2-Input Gate
(milliwatt)



$3 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 20 mW (Input High)
5.0 mW (Inputs Low)

MC771F Quad Exclusive "OR" Gate
(medium-power)

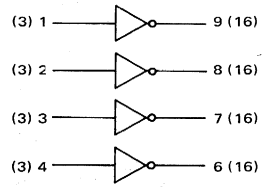


$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns
P_D = 87 mW

INVERTERS

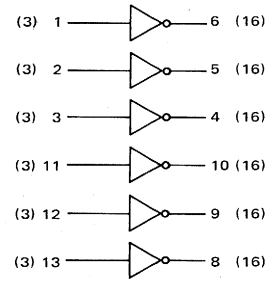
MC727F Quad Inverter
(medium-power)



$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 87 mW (Input High)
30 mW (Inputs Low)

MC789F Hex Inverter
(medium-power)

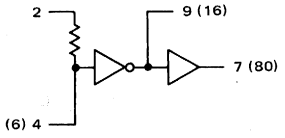


$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 130 mW (Input High)
15 mW (Inputs Low)

BUFFERS

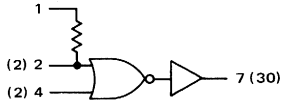
MC700F Buffer
(medium-power)



$9 = \overline{4}$
$7 = \overline{4}$

t_{pd} = 20 ns
P_D = 25 mW (Input High)
50 mW (Inputs Low)

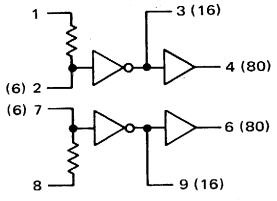
MC709F BUFFER
(milliwatt)



$7 = \overline{2 + 4}$

t_{pd} = 57 ns
P_D = 7.0 mW (Input High)
23 mW (Inputs Low)

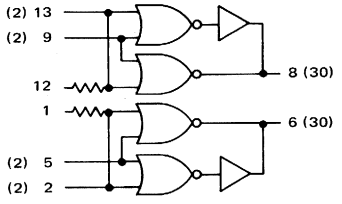
MC799F Dual Buffer
(medium-power)



$3 = \overline{2}$
$4 = \overline{2}$

t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

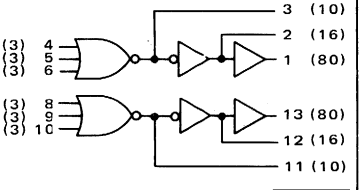
MC798F Dual 2-Input Buffer
(milliwatt)



$8 = \overline{9 + 13}$

t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 mW (Inputs Low)

MC788F Dual 3-Input Buffer
(non-inverting—medium-power)



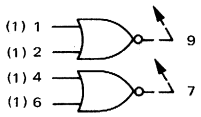
t_{pd} = 24 ns
P_D = 145 mW (Input High)
56 mW (Inputs Low)

$3 = \overline{4 + 5 + 6}$
$2 = 4 + 5 + 6$
$1 = 4 + 5 + 6$

Outputs 1, 2 or 3 may not be used simultaneously.
Outputs 11, 12, or 13 may not be used simultaneously.

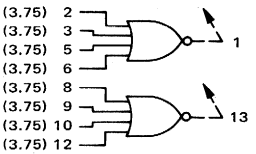
EXPANDERS

MC721F Dual 2-Input Expander
(milliwatt)



t_{pd} = 27 ns
P_D = 3.0 mW (Input High)

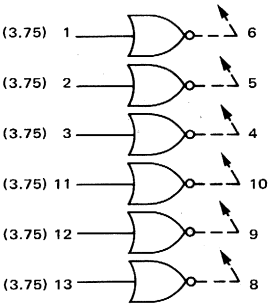
MC786F Dual 4-Input Expander
(medium-power)



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

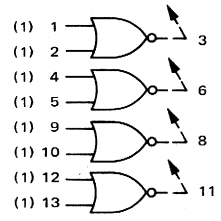
MC9719F Hex Expanders
(medium-power)



$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 13 mW (Input High)
Negligible (Inputs Low)

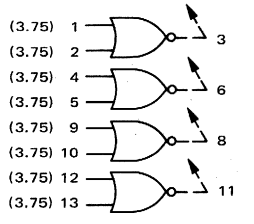
MC9721F Quad 2-Input Expander
(milliwatt)



$3 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

MC785F Quad 2-Input Expander
(medium-power)

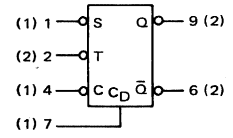


$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

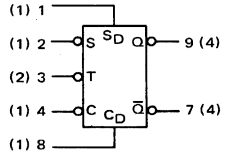
FLIP-FLOPS

MC720F J-K Flip-Flop
(milliwatt)



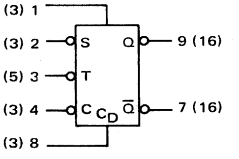
t_{pd} = 50 ns
P_D = 20.5 mW (Only Clock Input High)
14.5 mW (Inputs Low)

MC722F J-K Flip-Flop
(milliwatt)



t_{pd} = 70 ns
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

MC726F J-K Flip-Flop
(medium-power)



f_{Tog} = 4.0 MHz
t_{pd} = 35 ns
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC722 and MC726 only

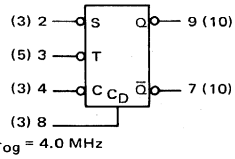
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1} ④	
S	C	Q	$\overline{Q}$
1	1	Q_n ⑤	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n ⑤

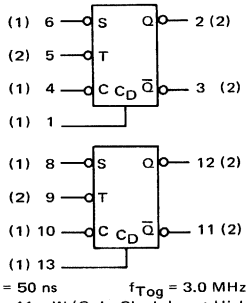
1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC723F J-K Flip-Flop
(medium-power)



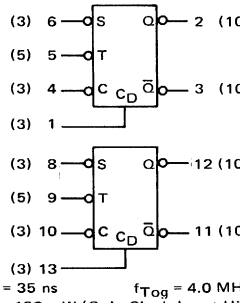
f_{Tog} = 4.0 MHz
t_{pd} = 35 ns
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

MC776F Dual J-K Flip-Flop
(milliwatt)



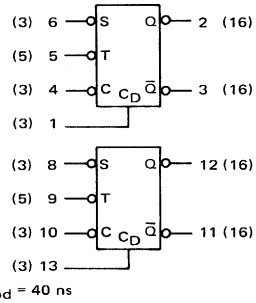
t_{pd} = 50 ns f_{Tog} = 3.0 MHz min
P_D = 41 mW (Only Clock Input High)
29 mW (Inputs Low)

MC790F Dual J-K Flip-Flop
(medium-power)



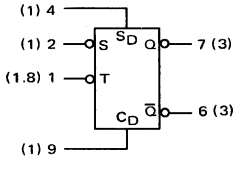
t_{pd} = 35 ns f_{Tog} = 4.0 MHz
P_D = 182 mW (Only Clock Input High)
158 mW (Inputs Low)

MC791F Dual J-K Flip-Flop
(medium-power)



t_{pd} = 40 ns
P_D = 190 mW (Only Clock Input High)
160 mW (Inputs Low)

MC713F Type D Flip-Flop
(milliwatt)



t_{pd} = 75 ns
P_D = 24 mW (Direct Set and Direct Clear Inputs Low, All other Inputs High)
17.5 mW (All Inputs Low)

DIRECT INPUT OPERATION ①

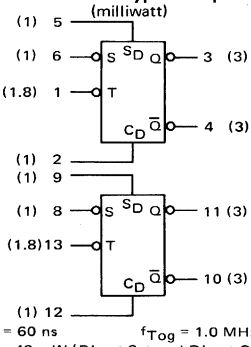
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n	t_{n+1}	
S	Q	$\overline{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
   0 = low state
   1 = high state
   t_n = time period prior to negative transition of pulse
   t_{n+1} = time period subsequent to negative transition of clock pulse

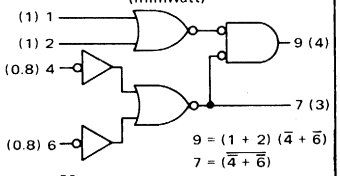
MC778F Dual Type D Flip-Flop
(milliwatt)



t_{pd} = 60 ns f_{Tog} = 1.0 MHz
P_D = 48 mW (Direct Set and Direct Clear Inputs Low, All other Inputs High)
35 mW (All Inputs Low)

HALF ADDERS

MC708F Half-Adder
(milliwatt)

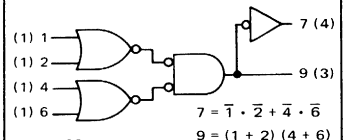


$9 = (1 + 2)(\overline{4} + \overline{6})$

$7 = \overline{(\overline{4} + \overline{6})}$

t_{pd} = 60 ns
P_D = 19 mW (Input High)
12.5 mW (Inputs Low)

MC712F Half-Adder
(milliwatt)

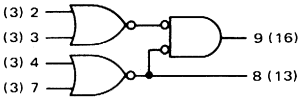


$7 = \overline{1} \cdot \overline{2} + \overline{4} \cdot \overline{6}$

$9 = (1 + 2)(4 + 6)$

t_{pd} = 66 ns
P_D = 15.5 mW (Input High)
10.5 mW (Inputs Low)

MC704F Half Adder
(medium-power)



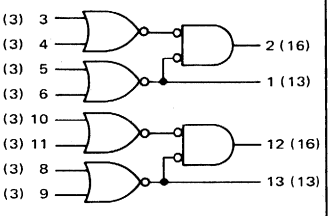
$9 = (2+3)(4 + 7)$

$8 = \overline{4 + 7}$

IF: $4 = \overline{2}$, & $7 = \overline{3}$
THEN: $8 = 2 \cdot 3$
$9 = 2 \cdot \overline{3} + \overline{2} \cdot 3$

t_{pd} = 14 ns
P_D = 65 mW

MC775F Dual Half Adder
(medium-power)



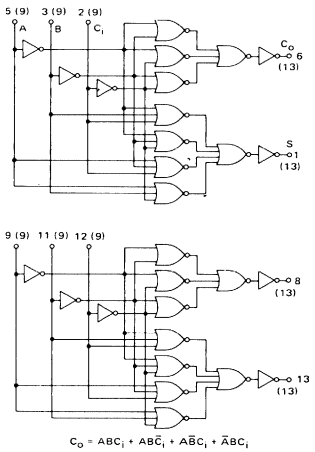
$2 = (3 + 4)(5 + 6)$

$1 = \overline{5 + 6}$

t_{pd} = 20 ns
P_D = 120 mW

FULL ADDER

MC796F Dual Full Adder



$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

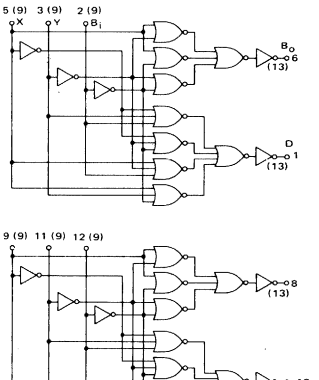
$S = ABC_i + AB\overline{C_i} + A\overline{B}\overline{C_i} + \overline{A}B\overline{C_i}$

t_{pd} = 60 ns
P_D = 84 mW

TRUTH TABLE				
Input Logic Level			Output Logic Level	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

MC797F Dual Full Subtractor



$D = YXB_i + Y\overline{X}\overline{B_i} + \overline{Y}X\overline{B_i} + \overline{Y}\overline{X}B_i$

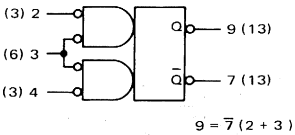
$B_o = \overline{Y}\overline{X}B_i + Y\overline{X}\overline{B_i} + Y\overline{X}B_i + YXB_i$

t_{pd} = 60 ns
P_D = 84 mW

TRUTH TABLE				
Input Logic Level			Output Logic Level	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

HALF-SHIFT REGISTERS

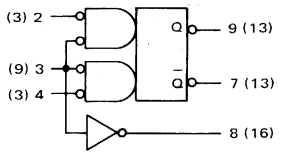
MC706F Half-Shift Register
(without inverter—medium-power)



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$

t_{pd} = 22 ns
P_D = 52 mW

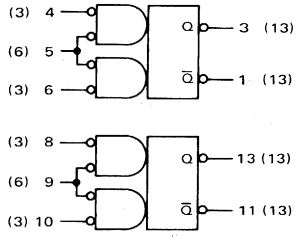
MC705F Half-Shift Register
(with inverter—medium-power)



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$
$8 = \overline{3}$

t_{pd} = 22 ns
P_D = 75 mW

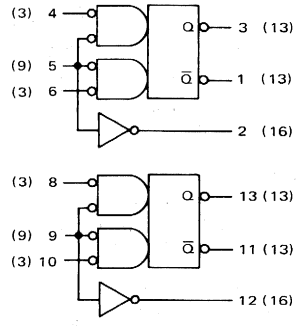
MC784F Dual Half-Shift Register
(without inverter—medium-power)



$3 = \overline{1}\ (4 + 5)$
$1 = \overline{3}\ (6 + 5)$

t_{pd} = 22 ns
P_D = 100 mW

MC783F Dual Half-Shift Register
(with inverter—medium-power)



$3 = \overline{1}\ (4 + 5)$
$1 = \overline{3}\ (6 + 5)$

t_{pd} = 22 ns
P_D = 140 mW