MEDIUM-POWER

MRTL

INTEGRATED CIRCUITS
MC900/MC800 SERIES

MEDIUM-POWER
MRTL
INTEGRATED CIRCUITS

INDEX

DEVICE SPECIFICATIONS

FUNCTIONS AND CHARACTERISTICS

V_{CC} = 3.0 V ±10%, T_A = 25°C

Function	Type ① -55 to +125°C	0 to +100°C	Case	Output Loading Factor each output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg
GATES						
3-Input NOR Gate	MC903	MC803	601, 606	5	12	19/5.0 ②
4-Input NOR Gate	MC907	MC807	601, 606	5	12	19/5.0 ②
Dual 2-Input NOR Gate	MC914	MC814	601, 606	5	12	38/10 ②
Dual 3-Input NOR Gate	MC915	MC815	603, 606	5	12	38/10 ②
Quad 2-Input NOR Gate	MC924	MC824	607	5	12	76/20 ②
Dual 4-Input NOR Gate	MC925	MC825	607	5	12	38/10 ②
5-Input NOR Gate	MC929	MC829	601, 606	5	12	19/5.0 ②
Quad Exclusive OR Gate	MC971	MC871	607	5	12	72
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Buffer	MC900	MC800	601, 606	25	20	16/45 ②
Dual 3-Input Buffer, non inverting	MC988	MC888	607	25	24	128/42 ②
Dual Buffer	MC999	MC899	603, 606	25	20	32/90 ②
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J-K Flip-Flop	MC916	MC816	601, 606	3	30	62/54 ③
J-K Flip-Flop	MC926	MC826	603, 606	5	35	130/65 ③
J-K Flip-Flop	MC974	MC874	601	5	35	130/65 ③
Dual J-K Flip-Flop	MC990	MC890	607	3	35	124/108 ③
Dual J-K Flip-Flop	MC991	MC891	607	5	40	155/130 ③
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Dual Half Adder	MC975	MC875	607	5	20	90
Dual Full Adder	MC996	MC896	607	5	60	190
Dual Full Subtractor	MC997	MC897	607	5	60	190
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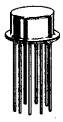
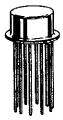
Hex Inverter	MC989	MC889	607	5	12	76/20 ②
EXPANDERS						
Quad 2-Input Expander	MC985	MC885	607	–	12	17/– ②
Dual 4-Input Expander	MC986	MC886	607	–	12	17/– ②
Hex Expander	MC9919	MC9819	607	–	12	13/– ②

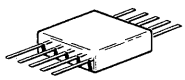
① G Suffix denotes Metal Can, F suffix denotes Flat Package; i.e., MC900G = Metal Can, MC900F = Flat Package.
② Inputs High/Inputs Low
③ Only Clock Input High/Inputs Low



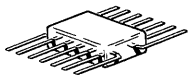
G SUFFIX
METAL PACKAGE
CASE 601
TO-99



G SUFFIX
METAL PACKAGE
CASE 603
TO-100



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

MAXIMUM RATINGS
($T_A = 25°C$)

Rating	Symbol	Value	Unit
Input Voltage	—	±4	Vdc
Power Supply Voltage (Pulsed ≤ 1 s)	—	+12	Vdc
Operating Temperature Range MC900 Series MC800 Series	T_A	-55 to +125 0 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TEST CONDITION TOLERANCES

$V_{BOT} = \pm 10$ mV $V_{CC} = \pm 10$ mV $V_{in} = \pm 2$ mV $V_{on} = \pm 2$ mV $V_{off} = \pm 2$ mV

DEFINITIONS

I_{A3}, I_{A4}, I_{A5} — Minimum available output current from a device with an output loading of 3, 4, or 5. Output voltage not to fall below the value of V_{in}.

I_{AB} — Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.

I_{CEX} — Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

I_{in} — Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

2 I_{in}, 3 I_{in} — Maximum input current drawn by one input of a device with 2 or 3 bases internally tied together.

V_{BOT} — A high-value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} — Supply voltage.

$V_{CE(sat)}$ — Maximum saturation voltage with V_{BOT} applied to the input.

V_{in} — Minimum high-level voltage applied to the input of a device.

V_{off} — The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} — The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} — The maximum output voltage with V_{on} applied to the input.

V_R — Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

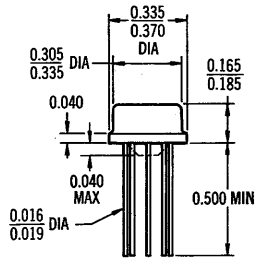
Release Time — The time that the J or K input data must be held after the negative-going clock input transition in order to propagate correct data.

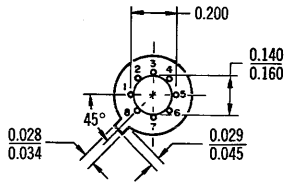
Set-up Time — The time that the J or K input data must be present prior to the negative-going clock input transition in order to propagate correct data.

GENERAL RULES

- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- A gate output connected in parallel with another output reduces the drive capability by ½ load. (Paralleling gate circuits requires a V_{CC} connection to only one of the gates.)
- Any number of gates may be paralleled if the input loading is increased by ¼ load, if only one gate is connected to V_{CC}.
- If the counter adapter is paralleled with another circuit, the output drive capability must be reduced by 2 loads. The reason for this drive reduction is the 1280-ohm resistance that connects the output terminals on the counter adapter.
- All unused inputs should be returned to ground.
- When paralleling gates with V_{CC} connected, a maximum of 4 outputs may be paralleled where the input loading factor is increased by 2.33.

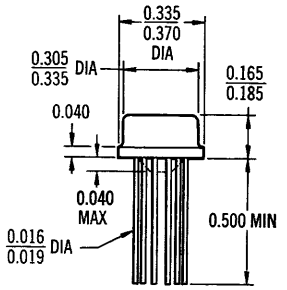
OUTLINE DIMENSIONS

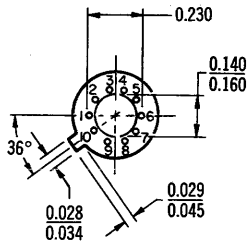




Pin 4 connected to case.

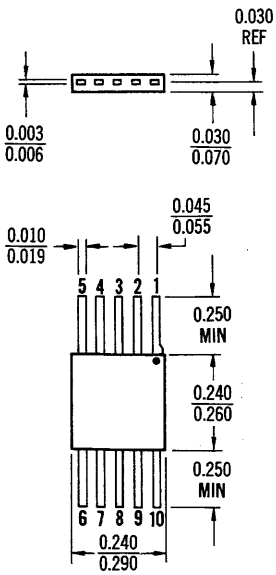
G SUFFIX
METAL PACKAGE
CASE 601
TO-99





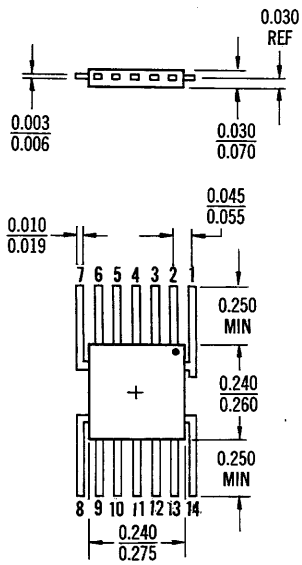
Pin 5 connected to case.

G SUFFIX
METAL PACKAGE
CASE 603
TO-100



Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

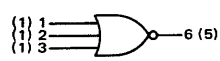
MRTL DEVICES AVAILABLE IN METAL CANS

The logic diagrams on these two pages describe the MC900/MC800 MRTL integrated circuits available in metal cans, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of –55 to +125°C for the MC900 Series, and 0 to +100°C for the MC800 Series, with V_{CC} = 3.0 V ±10%. For the TO-99 metal can, V_{CC} is applied to pin 8, with ground connected to pin 4. For the TO-100 metal can, V_{CC} is applied to pin 10, with ground connected to pin 5.

GATES

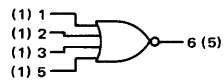
MC903G • MC803G
3-Input Gate



$6 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

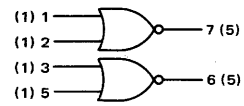
MC907G • MC807G
4-Input Gate



$6 = \overline{1 + 2 + 3 + 5}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

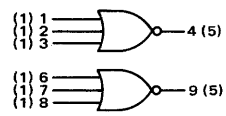
MC914G • MC814G
Dual 2-Input Gate



$7 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

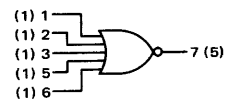
MC915G • MC815G
Dual 3-Input Gate



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

MC929G • MC829G
5-Input Gate

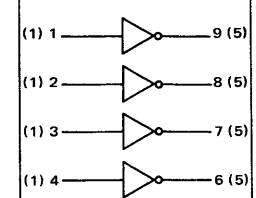


$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

INVERTERS

MC927G • MC827G
Quad Inverter

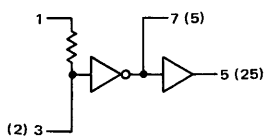


$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

BUFFERS

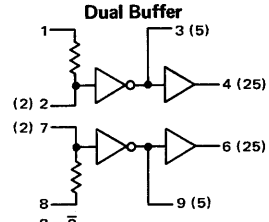
MC900G • MC800G
Buffer



$7 = \overline{3}$
$5 = \overline{3}$

t_{pd} = 20 ns
P_D = 16 mW (Input High)
45 mW (Inputs Low)

MC999G • MC899G
Dual Buffer

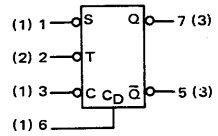


$3 = \overline{2}$
$4 = \overline{2}$

t_{pd} = 20 ns
P_D = 32 mW (Input High)
90 mW (Inputs Low)

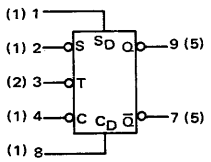
FLIP-FLOPS

MC916G • MC816G
J-K Flip-Flop



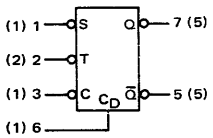
t_{pd} = 30 ns
P_D = 62 mW (Only Clock Input High)
54 mW (Inputs Low)

MC926G • MC826G
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Input High)
65 mW (Inputs Low)

MC974G • MC874G
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Input High)
65 mW (Inputs Low)

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC926 and MC826 only

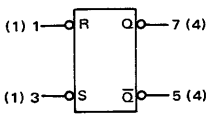
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC902G • MC802G
R-S Flip-Flop

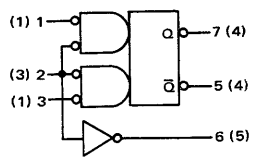


t_{pd} = 14 ns
P_D = 22 mW

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	0

HALF-SHIFT REGISTERS

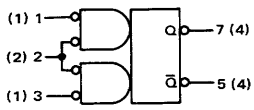
MC905G • MC805G
Half-Shift Register



t_{pd} = 22 ns
P_D = 53 mW

$7 = \overline{5}\,(1 + 2)$
$5 = \overline{7}\,(2 + 3)$
$6 = \overline{2}$

MC906G • MC806G
Half-Shift Register
(Without Inverter)

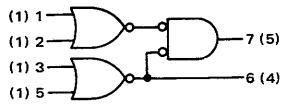


t_{pd} = 22 ns
P_D = 36 mW

$7 = \overline{5}\,(1 + 2)$
$5 = \overline{7}\,(2 + 3)$

HALF ADDERS

MC904G • MC804G
Half Adder



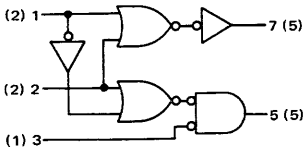
$7 = (1 + 2)\,(3 + 5)$
$6 = \overline{3 + 5}$

t_{pd} = 14
P_D = 45

IF: $3 = \overline{1}$, & $5 = \overline{2}$
THEN: $6 = 1 \cdot 2$
$7 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

COUNTER ADAPTERS

MC901G • MC801G
Counter Adapter



t_{pd} = 22 ns
P_D = 55 mW

$7 = 1 + 2$
$5 = (\overline{1} + 2)\,\overline{3}$

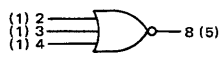
MRTL DEVICES AVAILABLE IN FLAT PACKAGES

The logic diagrams on these four pages describe the MC900/MC800 MRTL integrated circuits available in flat packages, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of –55 to +125°C for the MC900 Series, and 0 to +100°C for the MC800 Series, with V_{CC} = 3.0 V ±10%. For the TO-91 flat package, V_{CC} is applied to pin 10, with ground connected to pin 5. For the TO-86 flat package, V_{CC} is applied to pin 14, with ground connected to pin 7.

GATES

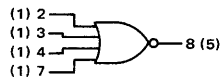
MC903F • MC803F
3-Input Gate



$8 = \overline{2 + 3 + 4}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

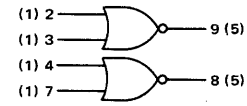
MC907F • MC807F
4-Input Gate



$8 = \overline{2 + 3 + 4 + 7}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

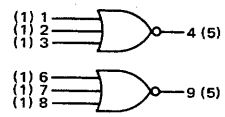
MC914F • MC814F
Dual 2-Input Gate



$9 = \overline{2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

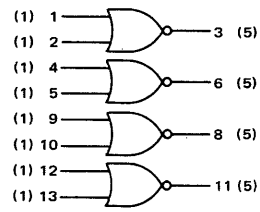
MC915F • MC815F
Dual 3-Input Gate



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

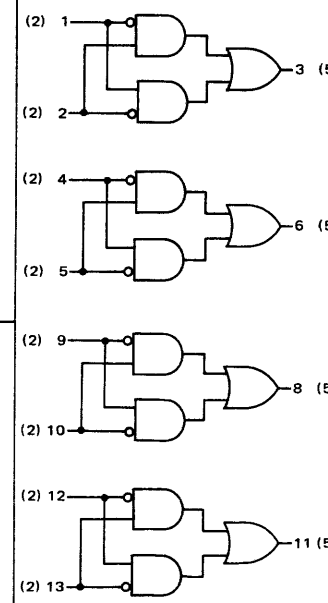
MC924F • MC824F
Quad 2-Input Gate



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

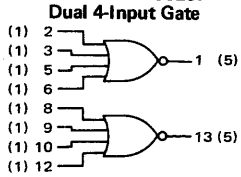
MC971F • MC871F
Quad Exclusive "OR" Gate



$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns
P_D = 72 mW

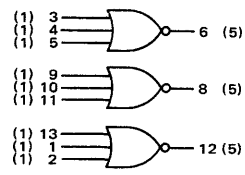
MC925F • MC825F
Dual 4-Input Gate



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

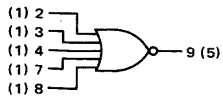
MC992F • MC892F
Triple 3-Input Gate



$6 = \overline{3 + 4 + 5}$

t_{pd} = 12 ns
P_D = 57 mW (Input High)
15 mW (Inputs Low)

MC929F • MC829F
5-Input Gate

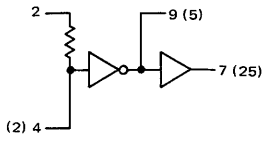


$9 = \overline{2 + 3 + 4 + 7 + 8}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

BUFFERS

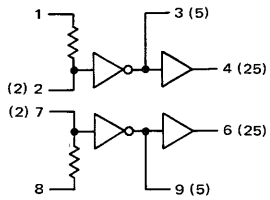
MC900F • MC800F
Buffer



$9 = \overline{4}$
$7 = \overline{4}$

t_{pd} = 15 ns
P_D = 16 mW (Input High)
45 mW (Inputs Low)

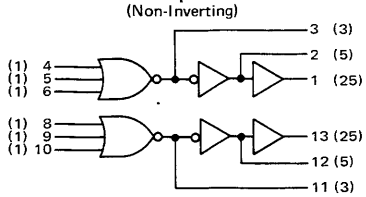
MC999F • MC899F
Dual Buffer



$3 = \overline{2}$
$4 = \overline{2}$

t_{pd} = 15 ns
P_D = 32 mW (Input High)
90 mW (Inputs Low)

MC988F • MC888F
Dual 3-Input Buffer
(Non-Inverting)



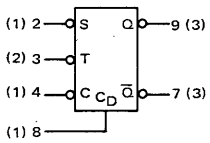
t_{pd} = 24 ns
P_D = 128 mW (Input High)
42 mW (Inputs Low)

$3 = \overline{4 + 5 + 6}$
$2 = 4 + 5 + 6$
$1 = 4 + 5 + 6$

Outputs 1, 2, or 3 may not be used simultaneously.
Outputs 11, 12, or 13 may not be used simultaneously.

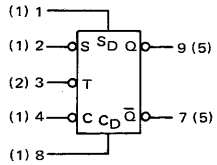
FLIP-FLOPS

MC916F • MC816F
J-K Flip-Flop



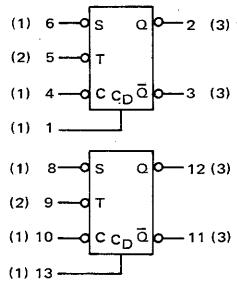
t_{pd} = 30 ns
P_D = 62 mW (Only Clock Inputs High)
54 mW (Inputs Low)

MC926F • MC826F
J-K Flip-Flop



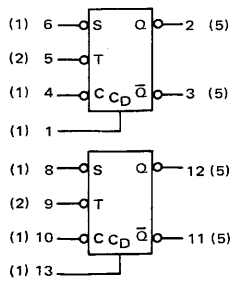
t_{pd} = 35 ns
P_D = 130 mW (Only Clock Inputs High)
65 mW (inputs Low)

MC990F • MC890F
Dual J-K Flip-Flop



t_{pd} = 35 ns
P_D = 124 mW (Only Clock Inputs High)
108 Mw (Inputs Low)

MC991F • MC891F
Dual J-K Flip-Flop



t_{pd} = 40 ns
P_D = 155 mW (Only Clock Input High)
130 mW (Inputs Low)

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

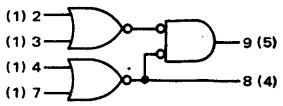
t_n ④		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

J-K FLIP-FLOP TRUTH TABLES

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

HALF ADDERS

MC904F • MC804F
Half Adder



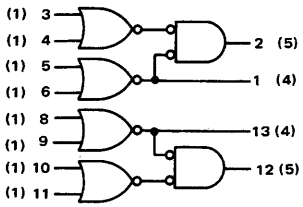
$9 = (2 + 3)(4 + 7)$

$8 = \overline{4 + 7}$

t_{pd} = 14 ns
P_D = 45 mW

IF: $4 = \overline{2}$, & $7 = \overline{3}$
THEN: $8 = 2 \cdot 3$
$9 = 2 \cdot \overline{3} + \overline{2} \cdot 3$

MC975F • MC875F
Dual Half Adder

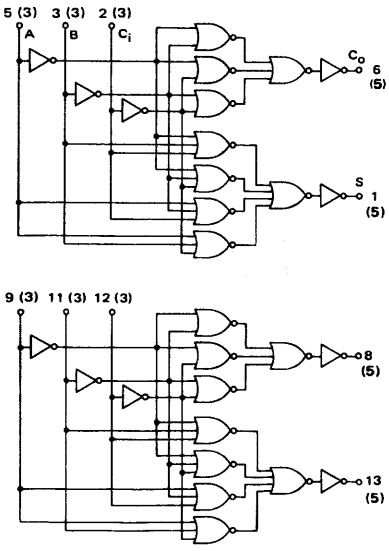


t_{pd} = 20 ns
P_D = 120 mW

$2 = (3 + 4)(5 + 6)$
$1 = \overline{5 + 6}$

FULL ADDER

MC996F • MC896F
Dual Full Adder



$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

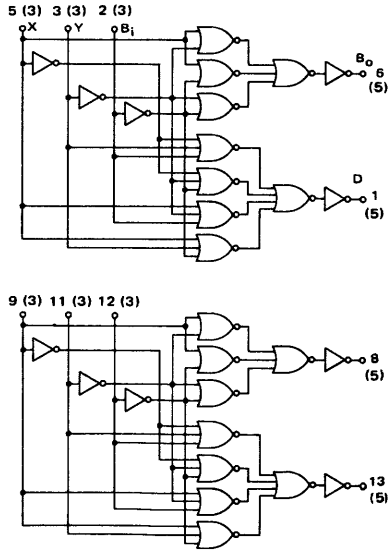
$S = ABC_i + A\overline{B}\overline{C_i} + \overline{A}\overline{B}C_i + \overline{A}B\overline{C_i}$

t_{pd} = 60 ns
P_D = 190 mW

TRUTH TABLE				
Input Logic Level			Output Logic Level	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

MC997F • MC897F
Dual Full Subtractor



$D = YXB_i + Y\overline{X}\overline{B_i} + \overline{Y}X\overline{B_i} + \overline{Y}\overline{X}B_i$

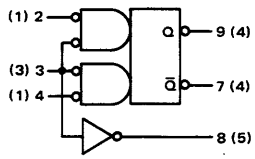
$B_o = \overline{Y}\overline{X}B_i + Y\overline{X}\overline{B_i} + Y\overline{X}B_i + YXB_i$

t_{pd} = 60 ns
P_D = 190 mW

TRUTH TABLE				
Input Logic Level			Output Logic Level	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

HALF-SHIFT REGISTERS

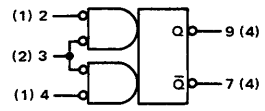
MC905F • MC805F
Half-Shift Register



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$
$8 = \overline{3}$

t_{pd} = 22 ns
P_D = 53 mW

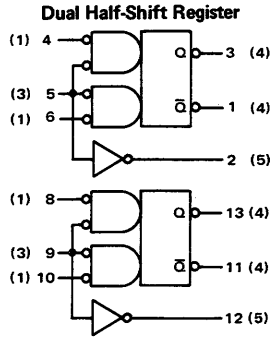
MC906F • MC806F
Half-Shift Register
(Without Inverter)



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$

t_{pd} = 22 ns
P_D = 36 mW

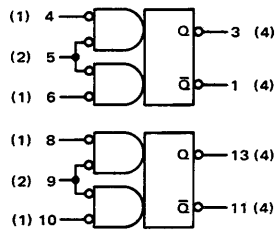
MC983F • MC883F
Dual Half-Shift Register



$1 = \overline{3}\ (6 + 5)$
$3 = \overline{1}\ (5 + 4)$
$2 = \overline{5}$

t_{pd} = 22 ns
P_D = 110 mW

MC984F • MC884F
Dual Half-Shift Register
(Without Inverter)

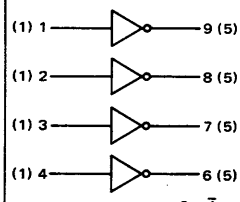


$3 = \overline{1}\ (4 + 5)$
$1 = \overline{3}\ (6 + 5)$

t_{pd} = 22 ns
P_D = 75 mW

INVERTERS

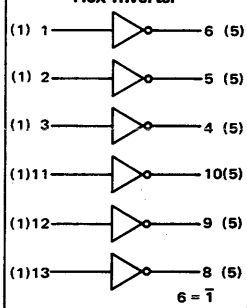
MC927F • MC827F
Quad Inverter



$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

MC989F • MC889F
Hex Inverter

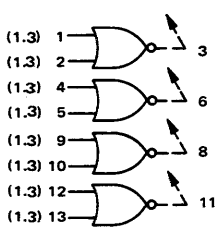


$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

EXPANDERS

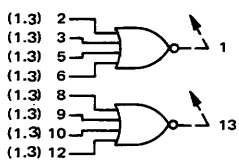
MC985F • MC885F
Quad 2-Input Expander



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 17 mW (input High)
Negligible (Inputs Low)

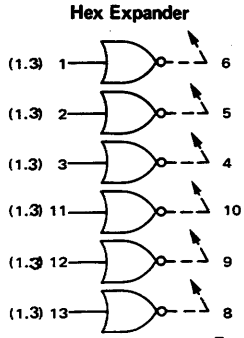
MC986F • MC886F
Dual 4-Input Expander



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 17 mW (Input High)
Negligible (Inputs Low)

MC9919F • MC9819F
Hex Expander



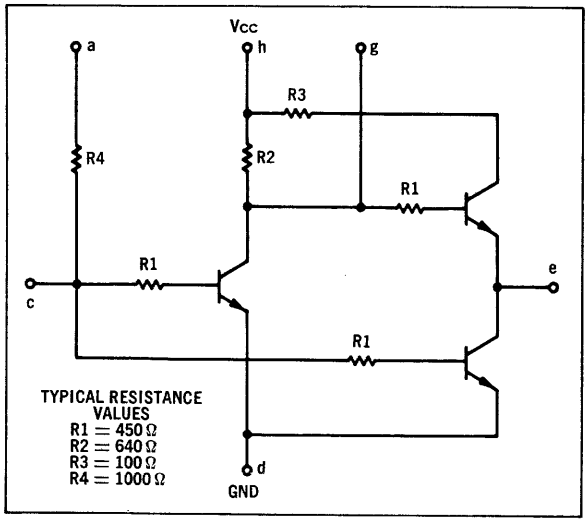
$6 = \overline{1}$

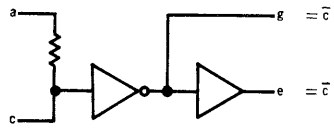
t_{pd} = 12 ns
P_D = 13 mW (Input High)
Negligible (Inputs Low)

MC900 • MC800

Available in TO-99 metal can, add "G" suffix.
Available in TO-91 flat package, add "F" suffix.

The buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input, the differentiation of input waveforms, and various multivibrator applications.



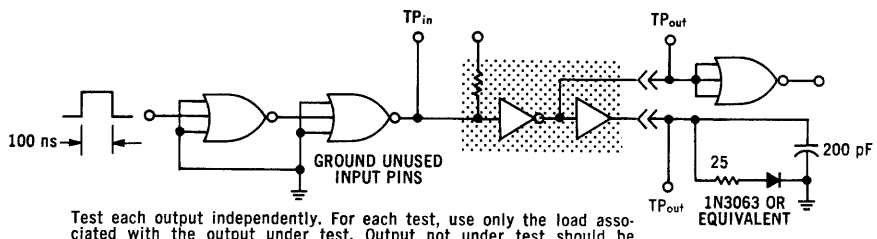


Outputs e and g may not be used simultaneously

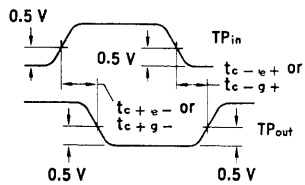
PIN CONNECTIONS

SCHEMATIC	a	—	c	d	e	—	g	h
G PACKAGE (TO-99)	1	—	3	4	5	—	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test. Output not under test should be left open.



ELECTRICAL CHARACTERISTICS

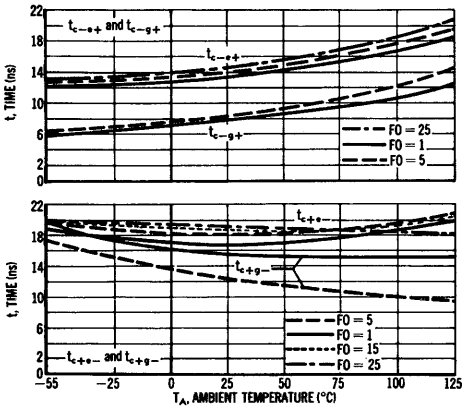
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC900	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC800	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC900 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC800 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2\,I_{in}$	c	-	990	-	870	-	940	μAdc	-	1010	-	900	-	900	μAdc	c	-	-	-	h	-	d
Output Current	I_{AB}	e	12.4	-	12.7	-	11.8	-	mAdc	12.6	-	11.9	-	11.25	-	mAdc	-	e	-	c	h	-	d
	I_{A5}	g	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	g	-	c	h	-	d
Output Voltage	V_{out}	e	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	c	-	-	h	e	d
		g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	c	-	-	h	-	d
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	c	-	h	e	d
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	c	-	h	-	↓
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	a,h	-	↓
Switching Time	t	c+e-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	Pulse In: c	Pulse Out: e	-	-	h	-	d
		c-e+	-	-	-	45	-	-	↓	-	-	-	45	-	-	↓	↓	e	-	-	↓	-	↓
		c+g-	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	↓	g	-	-	↓	-	↓
		c-g+	-	-	-	32	-	-	↓	-	-	-	32	-	-	↓	↓	g	-	-	↓	-	↓

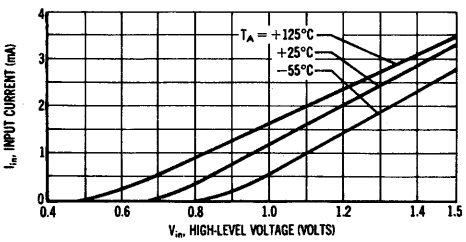
Pins not listed are left open.

* Resistor Value to V_{CC}

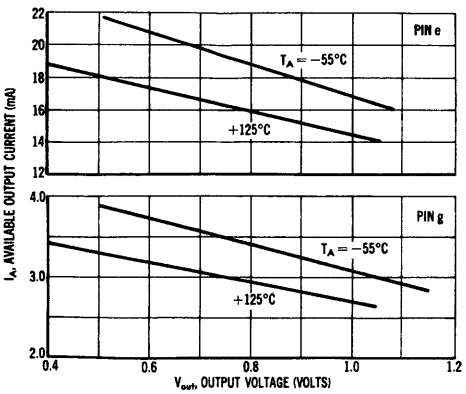
SWITCHING CHARACTERISTICS



INPUT CURRENT

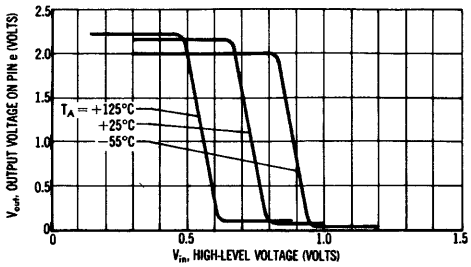


AVAILABLE OUTPUT CURRENT

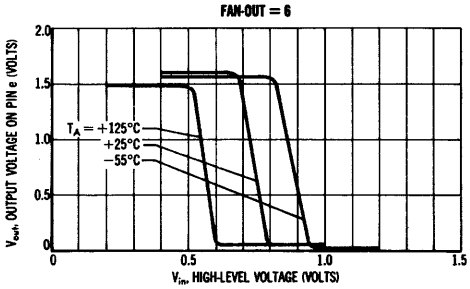


OUTPUT VOLTAGE

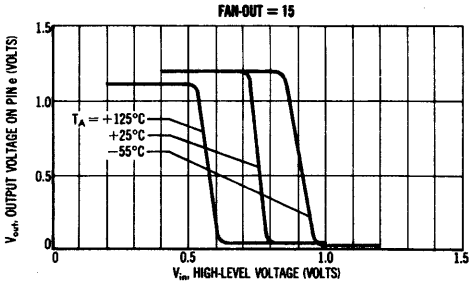
FAN-OUT = 1



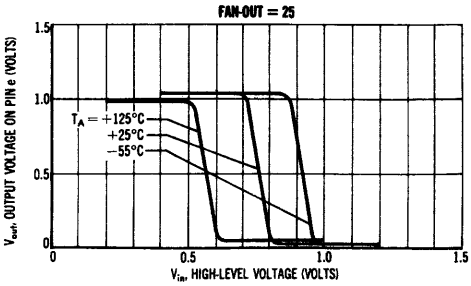
FAN-OUT = 6



FAN-OUT = 15



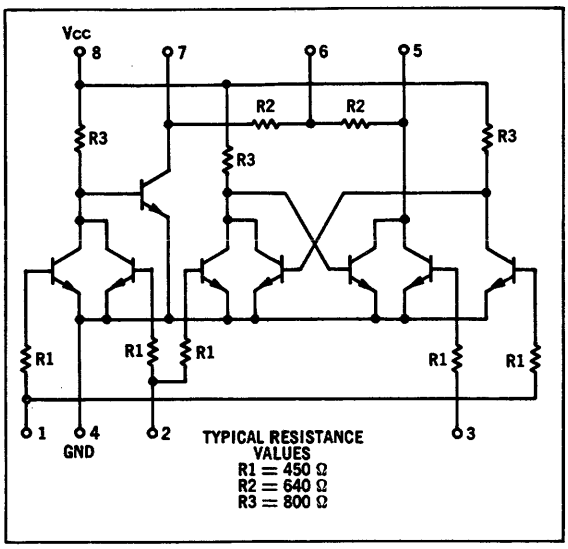
FAN-OUT = 25

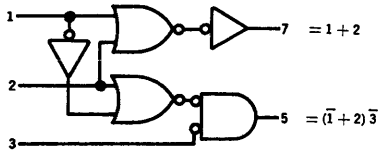


MC901 • MC801

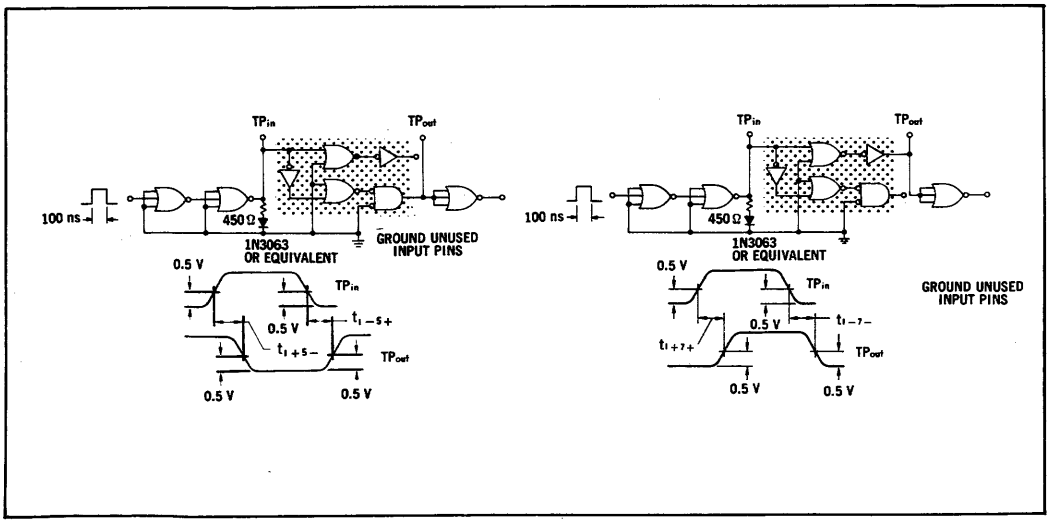
Available in TO-99 metal can, add "G" suffix.

This device provides the true output at pin 7 and the complement output at pin 5 for an input applied to pin 1. A positive gating signal may be applied to pin 2 to inhibit both outputs. A positive signal applied to pin 3 will hold output pin 5 at near-ground potential. The output nodes are returned separately to the power supply so that the outputs might be paralleled with other circuits.





SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

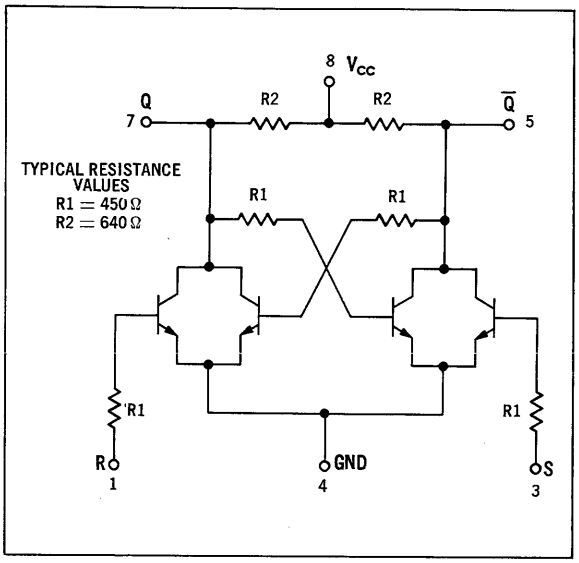
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC901	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC801	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC901 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC801 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2\ I_{in}$	1	-	990	-	870	-	940	µAdc	-	1010	-	900	-	900	µAdc	1	-	2	-	6,8	4
	$2\ I_{in}$	2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1	-	↓	↓
	$2\ I_{in}$	2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	-	-	↓	↓
	I_{in}	3	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	3	-	1	-	↓	↓
Output Current	I_{A5}	5	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	5	-	1,3	6,8	4
		5	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	2,5	1	3	↓	↓
		7		-		-		-			-		-		-		-	1,7	-	-		
		7		-		-		-			-		-		-		-	2,7	-	-		
Output Voltage	V_{out}	5	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	2	-	6,8	4
Saturation Voltage	$V_{CE(sat)}$	5	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	1	-	2	6,8	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2,3	-	↓	↓
		7	-		-		-			-		-		-			-	-	-	1,2		
																	Pulse In	Pulse Out				
Switching Time	t	1+5-	-	-	-	42	-	-	ns	-	-	-	42	-	-	ns	1	5	-	-	6,8	4
		1-5+	-	-	-	42	-	-		-	-	-	42	-	-		↓	5	-	-	↓	↓
		1+7+	-	-	-	38	-	-		-	-	-	38	-	-			7	-	-		
		1-7-	-	-	-	36	-	-	↓	-	-	-	36	-	-	↓		7	-	-		

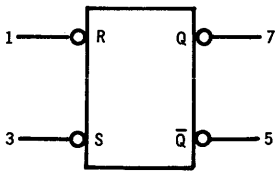
Pins not listed are left open.

MC902 • MC802

Available in TO-99 Metal Can, Add "G" Suffix

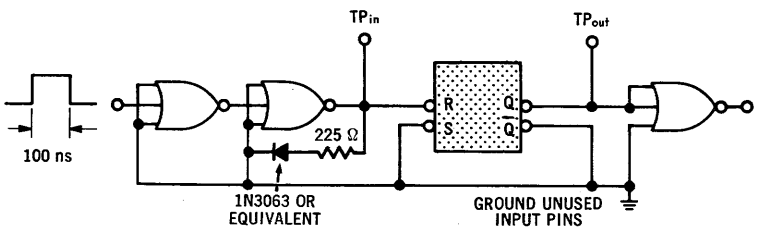


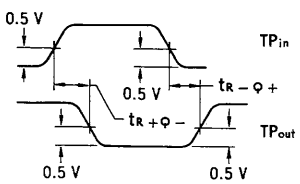
This flip-flop is formed by internally cross-coupling two basic RTL NOR gates.



R	S	Q^{n+1}
0	0	Q^n
0	1	1
1	0	0
1	1	0

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC902	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC802	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

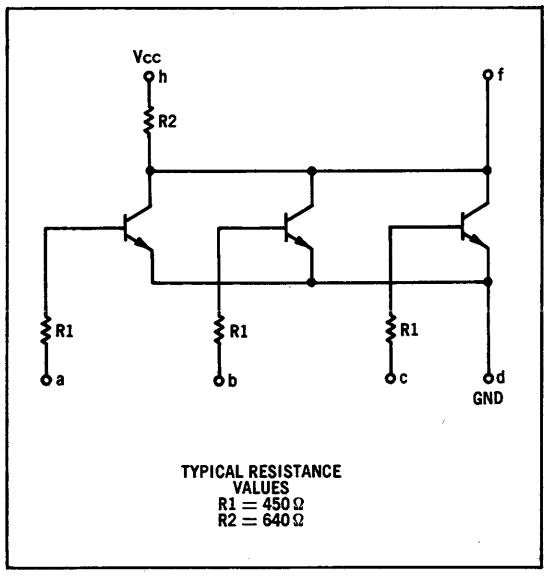
Characteristic	Symbol	Pin Under Test	MC902 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC802 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	5	-	8	4
		3	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	3	-	7	-	8	4
Output Current	I_{A4}	5	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	5	1	3	8	4
	I_{A4}	7	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	7	3	1	8	4
Output Voltage	V_{out}	5	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	1	-	8	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	7	-	-	↓	↓
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	3	-	↓	↓
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	-	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	5	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1,3	-	8	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1	↓	4,5 †
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1,3	-	↓	4
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	3	↓	4,7 †
																	Pulse In	Pulse Out				
Switching Time	t	1+7-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	1	7	-	-	8	4
		1-7+	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	1	7	-	-	8	4

Pins 2 and 6 omitted. Other pins not listed are left open. † Silicon Diode to Ground

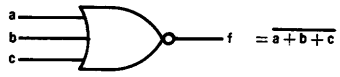
MC903 • MC803

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Provides the positive logic NOR function. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules).



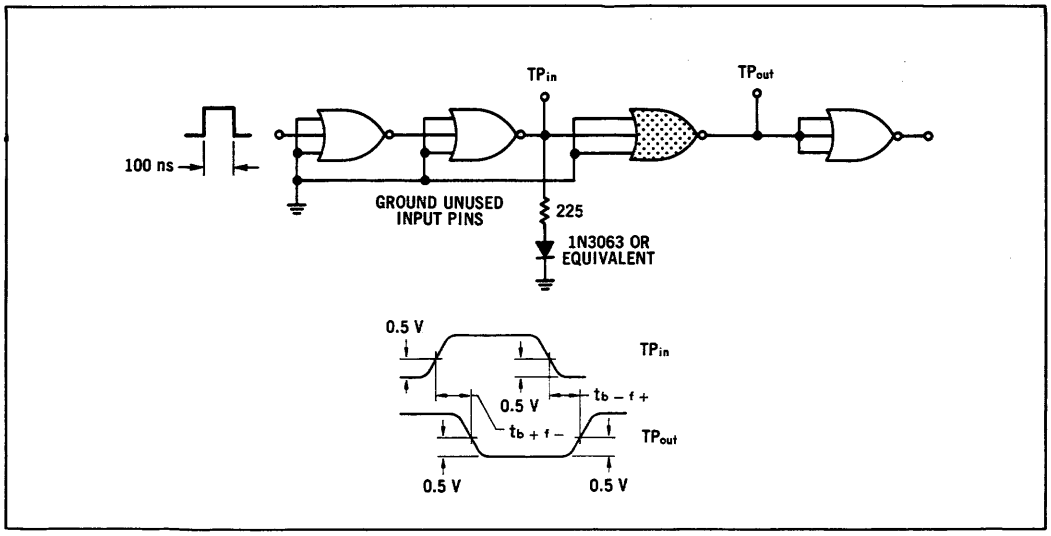
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω



PIN CONNECTIONS

SCHEMATIC	a	b	c	d	—	f	—	h
G PACKAGE (TO-99)	1	2	3	4	—	6	—	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC903	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC803	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

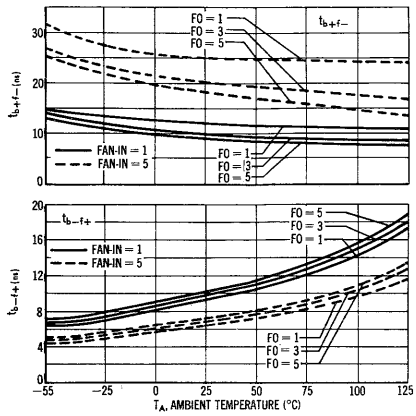
Characteristic	Symbol	Pin Under Test	MC903 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC803 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b, c	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c	-	↓	↓
		c	-		-		-			-		-		-			c	-	a, b	-		
Output Current	I_{A5}	f	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	f	-	a, b, c	h	d
Output Leakage Current	I_{CEX}	f	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	f	-	-	a, b, c	-	d
Output Voltage	V_{out}	f	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	↓
			-		-		-			-		-		-			-	c	-	-		
Saturation Voltage	$V_{CE(sat)}$	f	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	b	-	↓	↓
			-		-		-			-		-		-			-	-	c	-		
																	Pulse In	Pulse Out				
Switching Time	t	b+f-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	b	f	-	-	h	d
		b-f+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	b	f	-	-	h	d

Pins not listed are left open

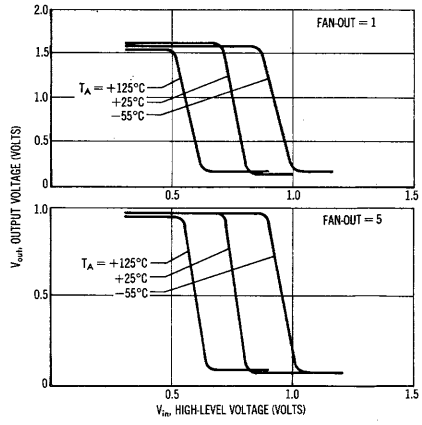
Pins e and g omitted

TYPICAL CURVES

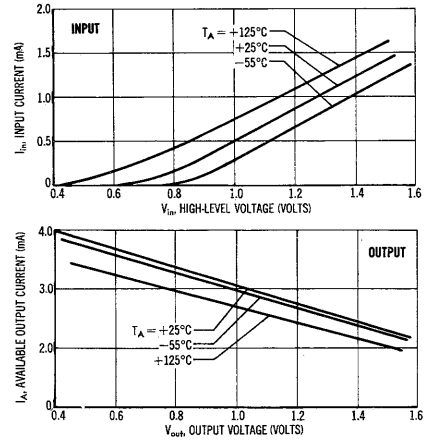
SWITCHING CHARACTERISTICS



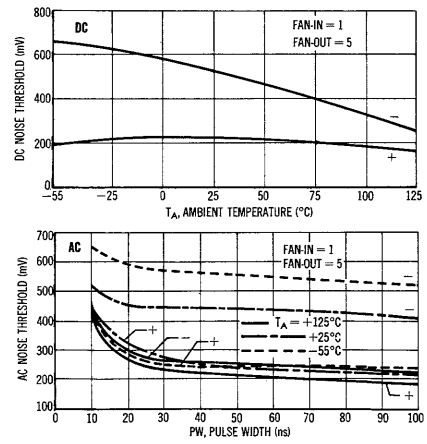
OUTPUT VOLTAGE



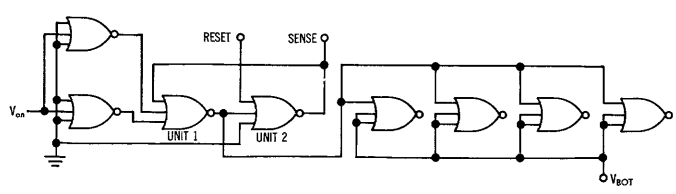
CURRENT



NOISE THRESHOLD



TEST CIRCUIT FOR NOISE THRESHOLD MEASUREMENTS

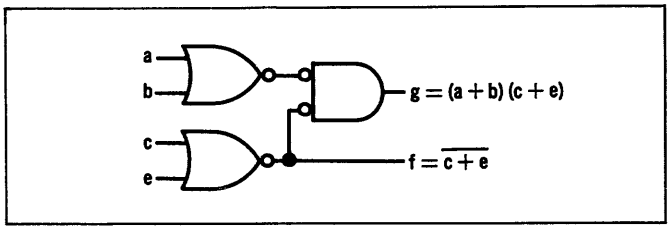


NOTE: V_{CC} and ground connections made to all devices.
UNIT 1 — Negative dc voltage with respect to ground applied to pin d.
UNIT 2 — Positive dc voltage with respect to ground applied to pin d.

MC904 • MC804

Available in TO-99 metal can, add "G" suffix.
Available in TO-91 flat package, add "F" suffix.

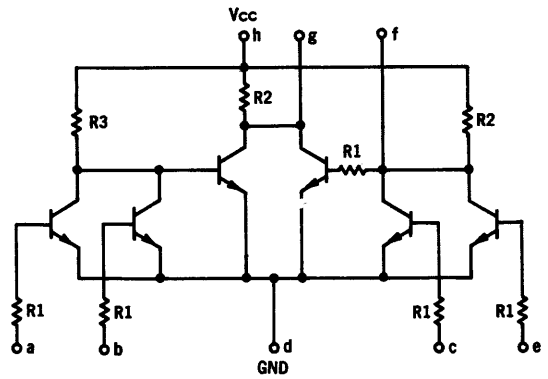
This half-adder device can be used to supply the SUM and CARRY operations on two input signals. If the inputs are applied to pins a and b, and their complements to pins c and e, the SUM of the inputs appears on pin g while the CARRY appears on pin f.



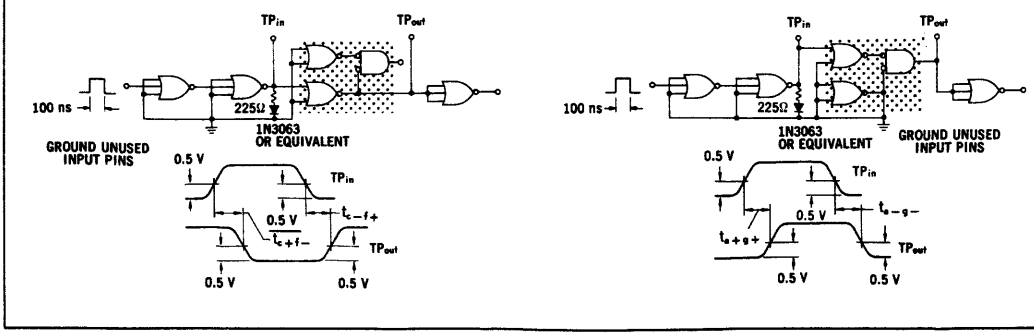
PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω



SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC904	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC804	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

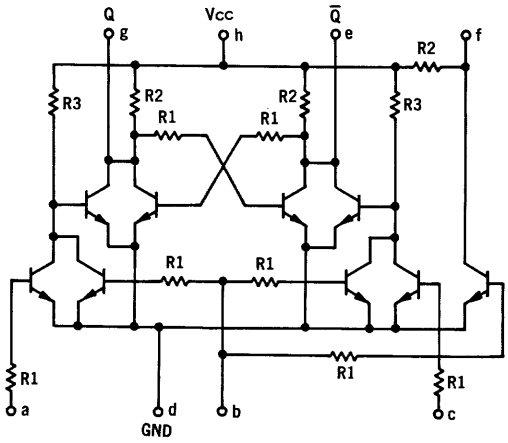
Characteristic	Symbol	Pin Under Test	MC904 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC804 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a	-	↓	↓
		c	-		--		-			-		-		-			c	-	e	-		
		e	-		-		-			-		-		-			e	-	c	-		
Output Current	I_{A4}	f	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	f	-	c, e	h	d
	I_{A5}	g	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	a, c, g	-	-	↓	↓
	I_{A5}	g	2.47	-	2.54	-	2.35	-		2.52	-	2.38	-	2.25	-		-	b, e, g	-	-		
Output Voltage	V_{out}	f	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	c	-	-	h	d
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	e	-	-	↓	↓
		g	-		-		-			-		-		-			-	f	a, b	-		
Saturation Voltage	$V_{CE(sat)}$	f	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	c	-	h	d
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	e	-	↓	↓
		g	-		-		-			-		-		-			-	-	a, b	c, e		
		g	-		-		-			-		-		-			-	-	c, e	a, b		
Switching Time	t	a+g+	-	-	-	36	-	-	ns	-	-	-	36	-	-	ns	Pulse In: a	Pulse Out: g	-	-	h	d
		a-g-	-	-	-	36	-	-	↓	-	-	-	36	-	-	↓	a	g	-	-	↓	↓
		c+f-	-	-	-	20	-	-		-	-	-	20	-	-		c	f	-	-		
		c-f+	-	-	-	30	-	-		-	-	-	30	-	-		c	f	-	-		

Pins not listed are left open.

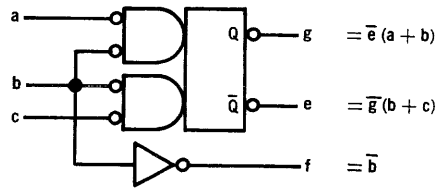
MC905 • MC805

Available in TO-99 metal can, add "G" suffix.
Available in TO-91 flat package, add "F" suffix.

This half-shift register is a bistable storage element with a built-in inverter for the gating signal. Information coming in on pins a and c will be transferred to pins g and e when the gating signal, pin b, goes low. If all three inputs, a, b, and c, are low, the outputs, g and e, will both be low.



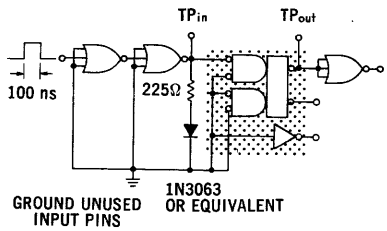
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

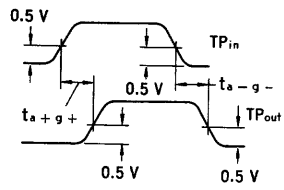


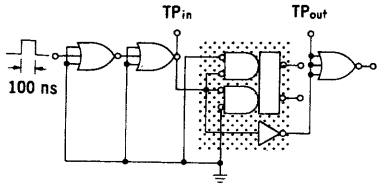
PIN CONNECTIONS

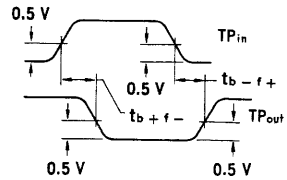
SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS









ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC905	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC805	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

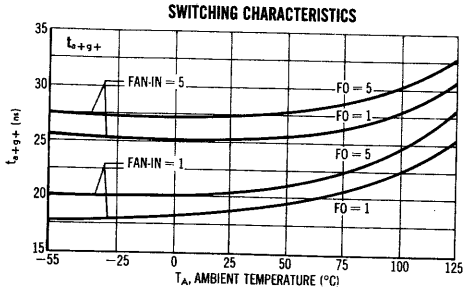
Characteristic	Symbol	Pin Under Test	MC905 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC805 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	a	-	b	-	h	d
	$3\ I_{in}$	b	-	1480	-	1300	-	1410		-	1510	-	1350	-	1350		b	-	a, c	-		
	I_{in}	c	-	495	-	435	-	470		-	504	-	450	-	450		c	-	b	-		
Output Current	I_{A4}	e	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	b, e	-	-	h	d, g †
	I_{A4}	e	1.98	-	2.19	-	1.88	-		2.02	-	2.05	-	1.80	-		-	c, e	-	-		d
	I_{A5}	f	2.47	-	2.54	-	2.35	-		2.52	-	2.38	-	2.25	-		-	f	-	b		d
	I_{A4}	g	1.98	-	2.19	-	1.88	-		2.02	-	2.05	-	1.80	-		-	b, g	-	-		d, e †
	I_{A4}	g	1.98	-	2.19	-	1.88	-		2.02	-	2.05	-	1.80	-		-	a, g	-	-		d
Output Voltage	V_{out}	e	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	g	b, c	-	h	d
		f	-		-		-			-		-		-			-	b	-	-		
		g	-		-		-			-		-		-			-	e	a, b	-		
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a, b, c	-	h	d, e †
		e	-		-		-			-		-		-			-	-	-	b, c		d, g
		f	-		-		-			-		-		-			-	-	b	-		d
		g	-		-		-			-		-		-			-	-	a, b, c	-		d, g †
		g	-		-		-			-		-		-			-	-	-	a, b		d, e
Switching Time	t	a+g+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In: a	Pulse Out: g	-	-	h	d, e
		a-g-	-	-	-	40	-	-		-	-	-	40	-	-		a	g	-	-		d, e
		b+f-	-	-	-	28	-	-		-	-	-	28	-	-		b	f	-	-		d
		b-f+	-	-	-	24	-	-		-	-	-	24	-	-		b	f	-	-		d

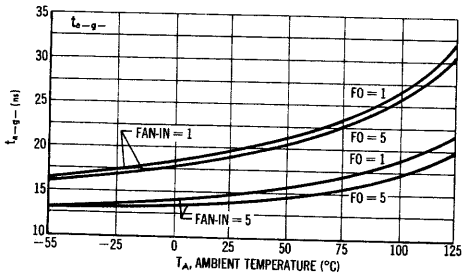
† Silicon Diode to Ground

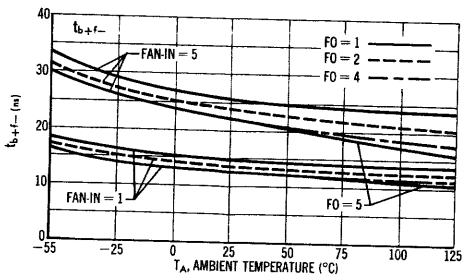
Pins not listed are left open.

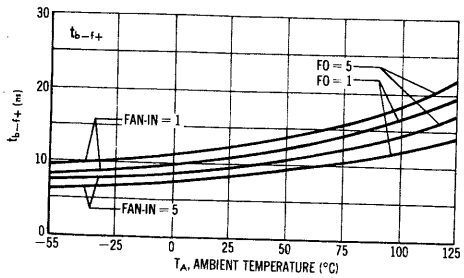
TYPICAL CURVES

SWITCHING CHARACTERISTICS

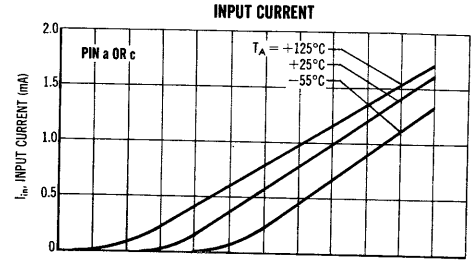


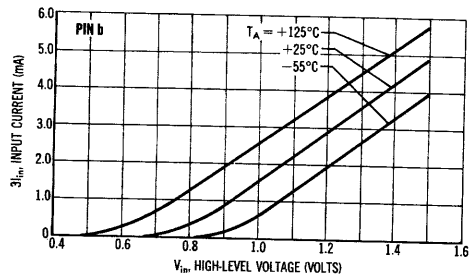




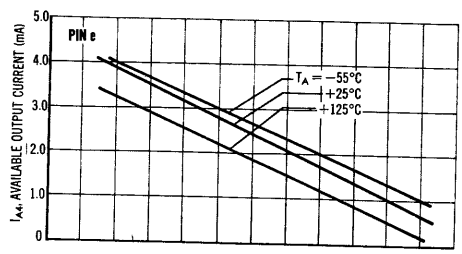


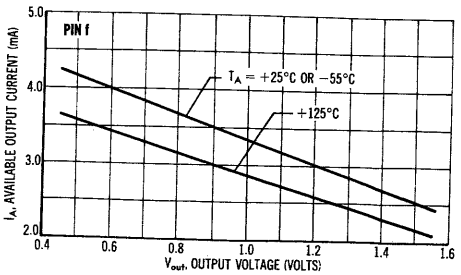
INPUT CURRENT





AVAILABLE OUTPUT CURRENT

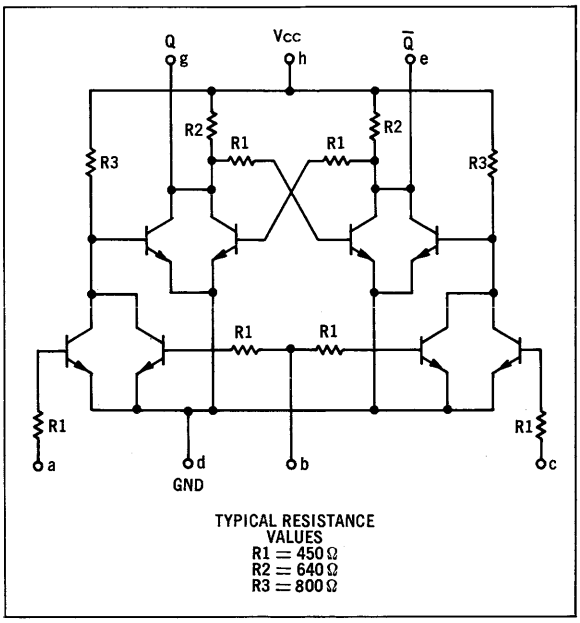




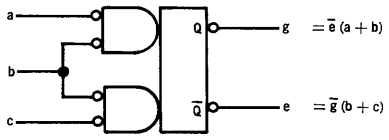
MC906 • MC806

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

This half-shift register is a bistable storage element. Information coming in on pins a and c will be transferred to pins g and e when the gating signal, pin b, goes low. If all three inputs, a, b, and c, are low, the outputs, g and e, will both be low.



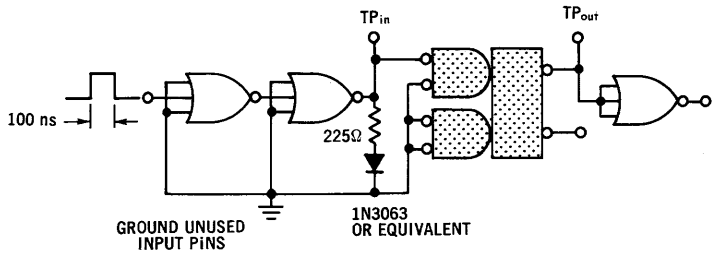
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

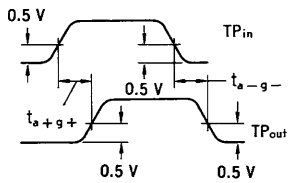


PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	—	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC906	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC806	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC906 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC806 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b	-	h	d
	$2\ I_{in}$	b	-	990	-	870	-	940	↓	-	1010	-	900	-	900	↓	b	-	a, c	-	↓	↓
	I_{in}	c	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	c	-	b	-	↓	↓
Output Current	I_{A4}	e	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	b, e	-	-	h	d, g †
		e	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	c, e	-	-	↓	d
		g		-		-		-			-		-		-		-	b, g	-	-		d, e †
		g		-		-		-			-		-		-		-	a, g	-	-		d
Output Voltage	V_{out}	e	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	g	b, c	-	h	d
		g		710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	e	a, b	-	h	d
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a, b, c	-	h	d, e †
		e	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	b, c	↓	d, g
		g	-		-		-			-		-		-			-	-	a, b, c	-		d, g †
		g	-		-		-			-		-		-			-	-	-	a, b		d, e
Switching Time	t	a+g+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In: a	Pulse Out: g	-	-	h	d, e
		a-g-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	a	g	-	-	h	d, e

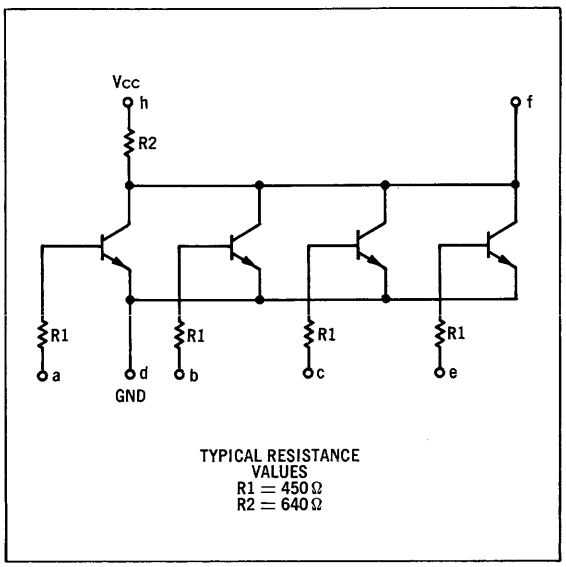
† Silicon Diode to Ground

Pins not listed are left open.

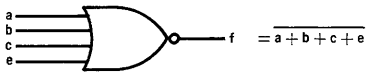
MC907 • MC807

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Provides positive logic NOR function. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules).



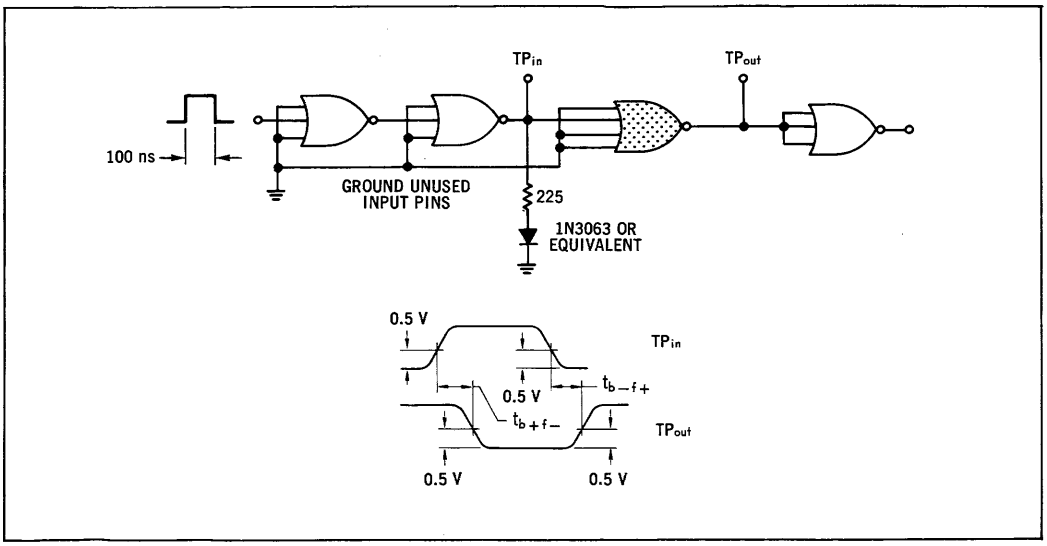
TYPICAL RESISTANCE VALUES
R1 = 450Ω
R2 = 640Ω



PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	—	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC907	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC807	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

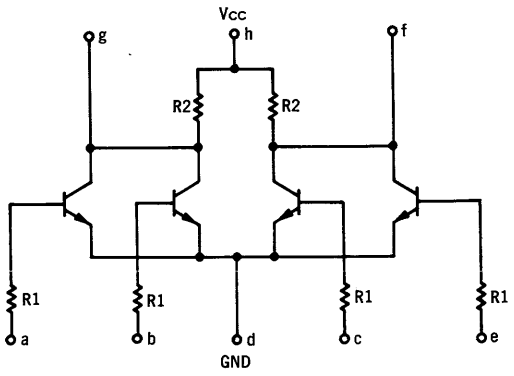
Characteristic	Symbol	Pin Under Test	MC907 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC807 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	a	-	b, c, e	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c, e	-	↓	↓
		c	-		-		-			-		-		-			c	-	a, b, e	-		
		e	-		-		-			-		-		-			e	-	a, b, c	-		
Output Current	I_{A5}	f	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	f	-	a, b, c, e	h	d
Output Leakage Current	I_{CEX}	f	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	f	-	-	a, b, c, e	-	d
Output Voltage	V_{out}	f	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	↓
			-		-		-			-		-		-			-	c	-	-		
			-		-		-			-		-		-			-	e	-	-		
Saturation Voltage	$V_{CE(sat)}$	f	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	b	-	↓	↓
			-		-		-			-		-		-			-	-	c	-		
			-		-		-			-		-		-			-	-	e	-		
																	Pulse In	Pulse Out				
Switching Time	t	b+f-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	b	f	-	-	h	d
		b-f+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	b	f	-	-	h	d

Pins not listed are left open.

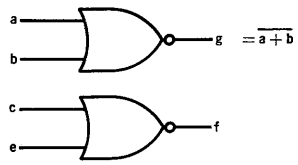
MC914 • MC814

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Two 2-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.



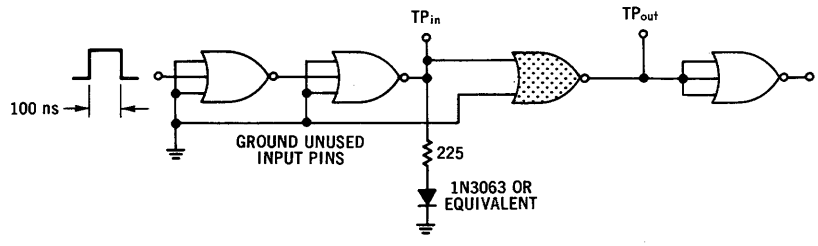
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

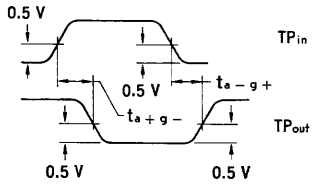


PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC914	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC814	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

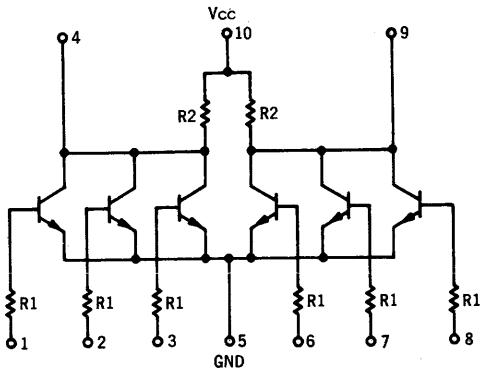
Characteristic	Symbol	Pin Under Test	MC914 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC814 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b	-	h	d
		b	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	b	-	a	-	h	d
Output Current	I_{A5}	g	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	g	-	a, b	h	d
Output Leakage Current	I_{CEX}	g	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	g	-	-	a, b	-	d
Output Voltage	V_{out}	g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
		g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	b	-	-	h	d
Saturation Voltage	$V_{CE(sat)}$	g	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
		g	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	b	-	h	d
																	Pulse In	Pulse Out				
Switching Time	t	a+g-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	a	g	-	-	h	d
		a-g+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	a	g	-	-	h	d

Ground inputs of gate not under test. Other pins not listed are left open.

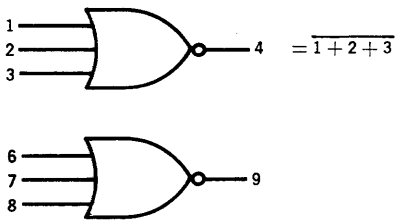
MC915 • MC815

Available in TO-100 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Two 3-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

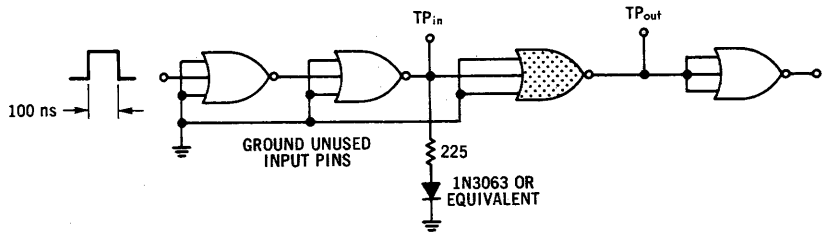


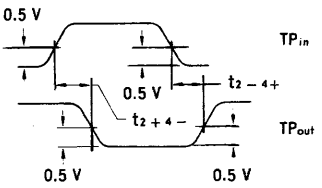
TYPICAL RESISTANCE VALUES
R1 = 450Ω
R2 = 640Ω



"F" PACKAGE AND "G" PACKAGE PIN-OUTS ARE THE SAME

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

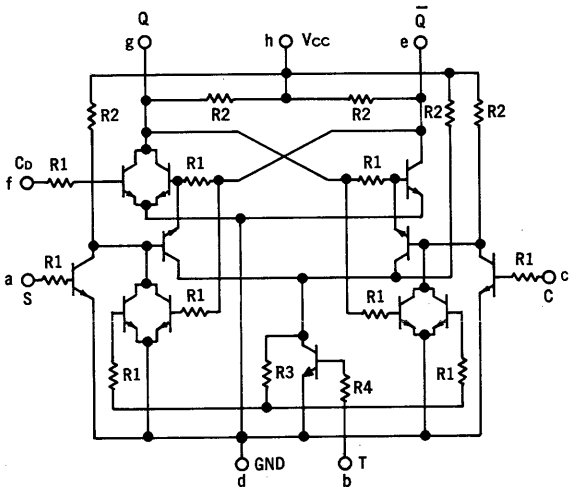
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC915	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC815	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC915 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC815 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	1	-	2, 3	-	10	5
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1, 3	-	↓	↓
		3	-		-		-			-		-		-			3	-	1, 2	-		
Output Current	I_{A5}	4	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	4	-	1, 2, 3	10	5
Output Leakage Current	I_{CEX}	4	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	4	-	-	1, 2, 3	-	5
Output Voltage	V_{out}	4	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	10	5
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	↓
			-		-		-			-		-		-			-	3	-	-		
Saturation Voltage	$V_{CE(sat)}$	4	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	10	5
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2	-	↓	↓
			-		-		-			-		-		-			-	-	3	-		
																	Pulse In	Pulse Out				
Switching Time	t	2+4-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	2	4	-	-	10	5
		2-4+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	2	4	-	-	10	5

Ground inputs of gate not under test. Other pins not listed are left open.

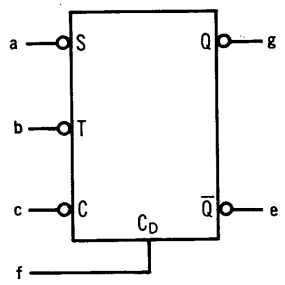
MC916 • MC816

Available in TO-99 Metal Can, Add "G" Suffix
Available in TO-91 Flat Package, Add "F" Suffix



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω

J-K flip-flop with a direct clear input in addition to the clocked input.



CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

① Direct input (C_D) must be low.
② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transistion is denoted t_{n+1}.
③ Q_n is the state of the Q output in the time period t_n.

PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC916	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC816	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC916 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC816 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	a	-	e	-	h	d
	$2\ I_{in}$	b	-	990	-	870	-	940		-	1010	-	900	-	900		b	-	a, c, g	-		
	I_{in}	c	-	495	-	435	-	470		-	504	-	450	-	450		c	-	g	-		
		f	-	495	-	435	-	470		-	504	-	450	-	450		f	-	e	-		
Output Current	I_{A3}	e	1.48	-	1.52	-	1.41	-	mAdc	1.51	-	1.43	-	1.35	-	mAdc	-	e	a, f	-	h	d
		e		-		-		-			-		-		-		-	e, f	a	-		d
		g		-		-		-			-		-		-		-	g	c	f		d, e †
Output Voltage	V_{out}	g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	f	-	-	h	
		g‡#	-		-		-			-		-		-			-	a, c	-	-		
		g‡	-		-		-			-		-		-			-	c	-	a		d, e
		g‡§	-		-		-			-		-		-			-	-	-	a, c		d, f
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	-	f	h	d, e †
		g	-		-		-			-		-		-			-	-	f	-		d, e
		g	-		-		-			-		-		-			-	-	-	-		d, g †
Turn-On Voltage	V_{on}	g‡§	1014	-	815	-	674	-	mVdc	909	-	844	-	710	-	mVdc	-	a, c	-	-	h	d, f
		g‡		-		-		-			-		-		-		-	a	-	c		
		g‡#*		-		-		-			-		-		-		-	-	-	a, c		

† Silicon Diode to Ground

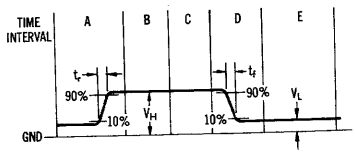
* MC916 pin g loaded by: 1.52 mAdc (+25°C), 1.48 mAdc (-55°C), 1.41 mAdc (+125°C); MC816 pin g loaded by: 1.42 mAdc (+25°C), 1.51 mAdc (0°C), 1.35 mAdc (+100°C)

Pins not listed are left open.

‡ Pin b = Clock pulse to pin b (see Figure 1).

§ Pin e = LOW
# Pin g = LOW
} Set by a momentary ground prior to the application of the negative-going Clock Pulse.

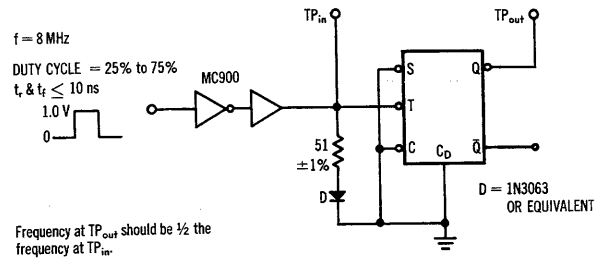
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



Frequency at TP_{out} should be ½ the frequency at TP_{in}.

MC816		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC916		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.724 V

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

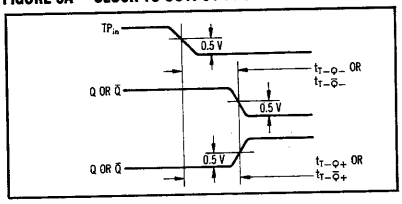


FIGURE 3B — SET-UP AND RELEASE TIME

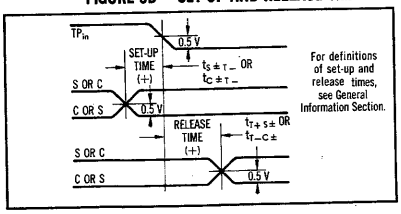
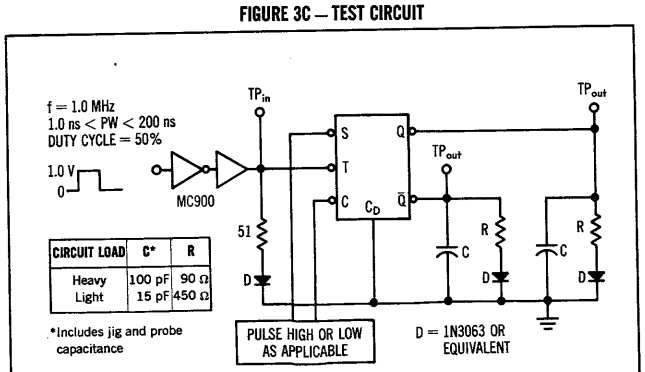


FIGURE 3C — TEST CIRCUIT



CIRCUIT LOAD	C*	R
Heavy	100 pF	90 Ω
Light	15 pF	450 Ω

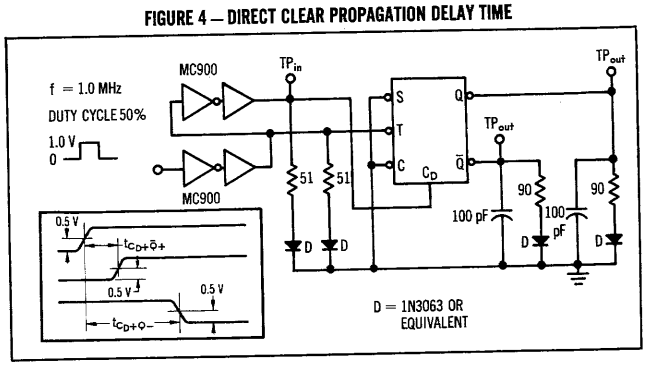
*Includes jig and probe capacitance

SWITCHING TIMES

Test	Figure No.	Maximum Over Full Temperature Range (ns)
t_{T-Q-}	3A, 3C	60
$t_{T-\bar{Q}-}$	3A, 3C	60
t_{T-Q+}	3A, 3C	100
$t_{T-\bar{Q}+}$	3A, 3C	100
$t_{S\pm T-}$	3B, 3C	50
$t_{C\pm T-}$	3B, 3C	50
$t_{T-S\pm}$	3B, 3C	50
$t_{T-C\pm}$	3B, 3C	50
t_{CD+Q-}	4	50
$t_{CD+\bar{Q}-}$	4	90

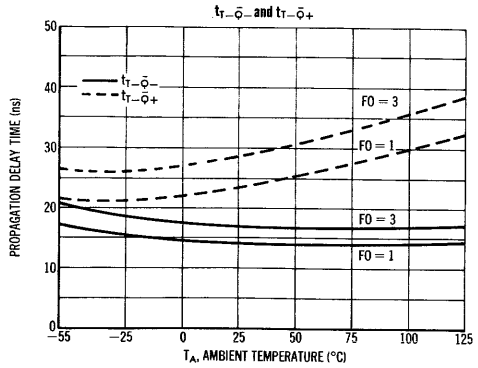
1. Change of state occurs on trailing edge of clock pulse.
2. With a high level on C_D, and with the proper SET and CLEAR inputs for a low level at $\bar{Q}$, $\bar{Q}$ will be high except for a short period after the negative-going edge of a clock pulse. $\bar{Q}$ will go low for up to 50 ns, and then return to a high level within 100 ns after a negative clock transition.

FIGURE 4 — DIRECT CLEAR PROPAGATION DELAY TIME

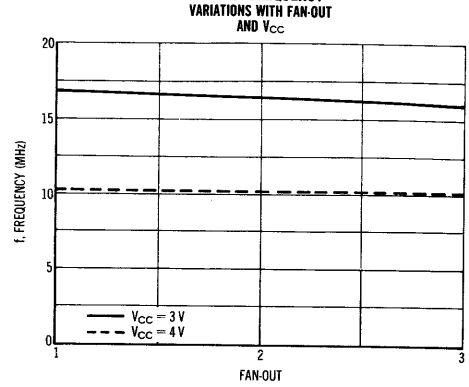


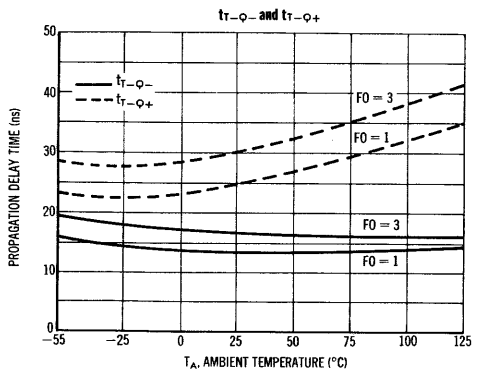
TYPICAL CURVES

TYPICAL PROPAGATION DELAY TIME

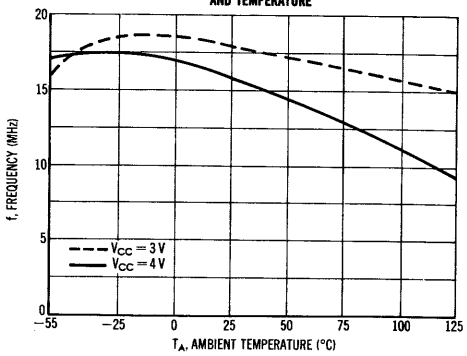


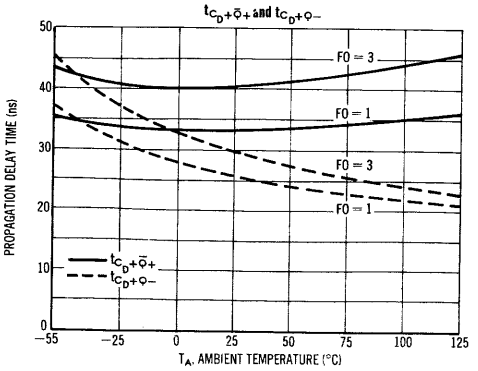
TOGGLE FREQUENCY VARIATIONS WITH FAN-OUT AND V_{CC}



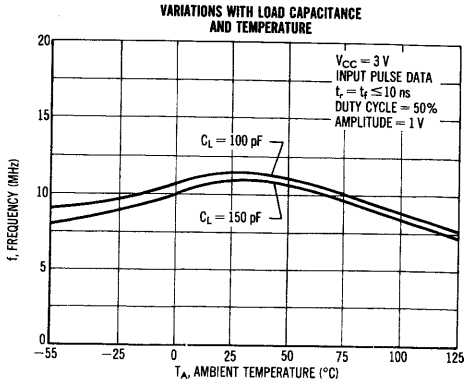


VARIATIONS WITH V_{CC} AND TEMPERATURE





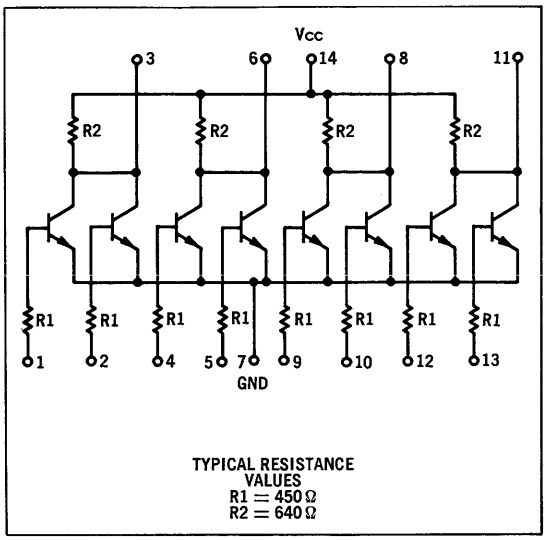
VARIATIONS WITH LOAD CAPACITANCE AND TEMPERATURE

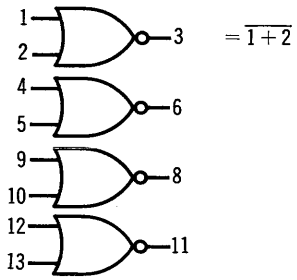


MC924 • MC824

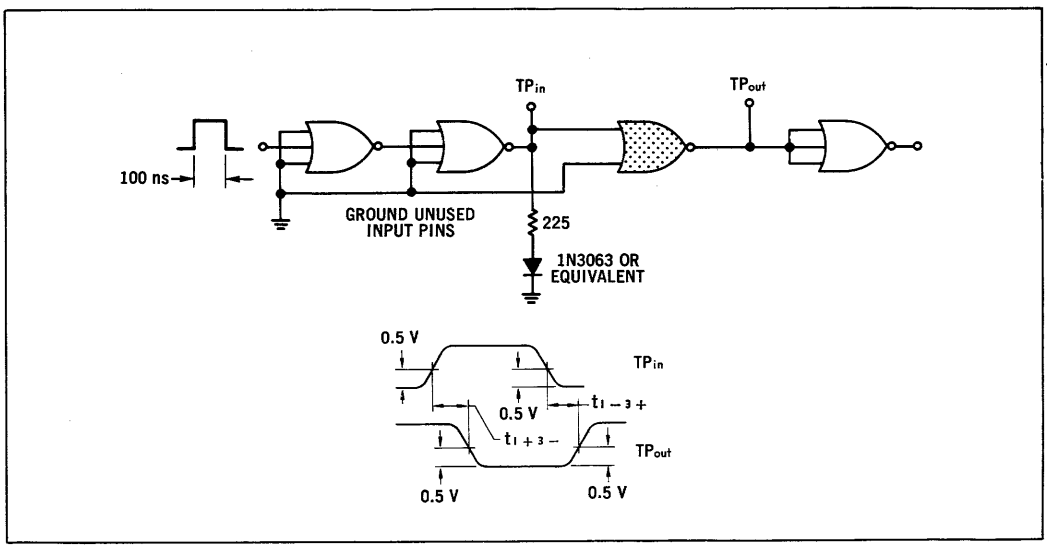
Available in TO-86 Flat Package, Add "F" Suffix.

This gate element consists of four 2-input positive logic NOR gate circuits in a single package. The gate circuits may be used independently, or connected together to form flip-flops or non-inverting gates.





SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC924	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC824	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

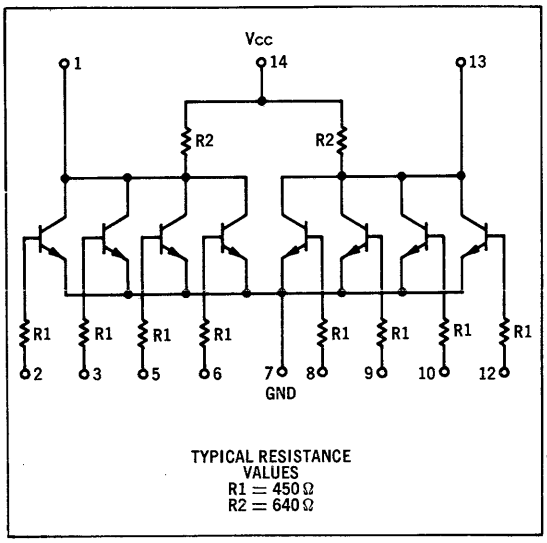
Characteristic	Symbol	Pin Under Test	MC924 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC824 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	1	-	2	-	14	7
		2	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	2	-	1	-	14	7
Output Current	I_{A5}	3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	3	-	-	1,2	14	7
Output Leakage Current	I_{CEX}	3	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	-	3	-	1,2	-	7
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	2,7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	1,7
Saturation Voltage	$V_{CE(sat)}$	3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	2,7
		3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	1,7
																	Pulse In	Pulse Out				
Switching Time	t	1+3-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	1	3	-	-	14	2,7
		1-3+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	1	3	-	-	14	2,7

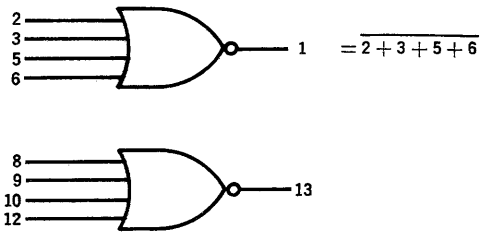
Ground inputs of gates not under test. Other pins not listed are left open.

MC925 • MC825

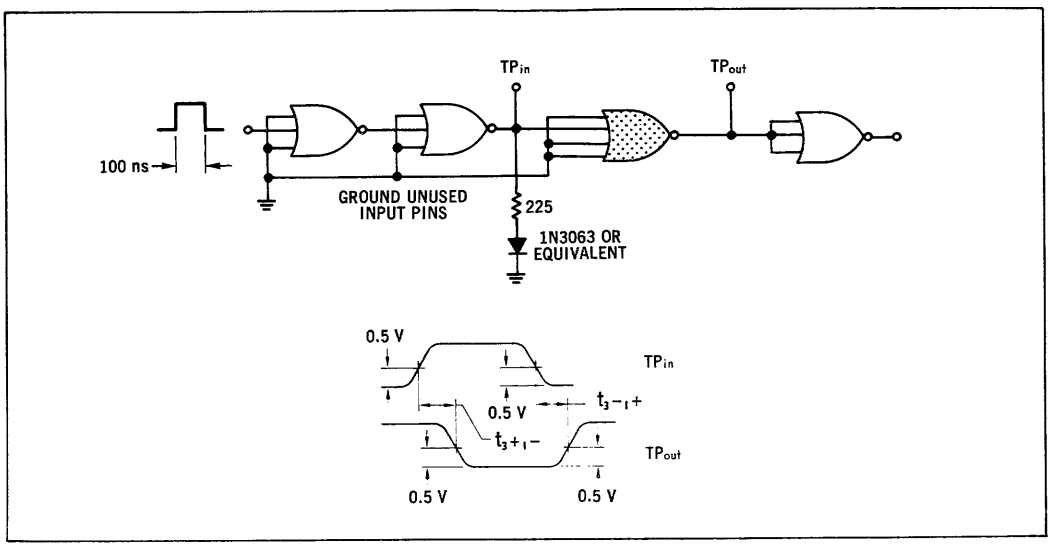
Available in TO-86 Flat Package, Add "F" Suffix.

Two 4-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.





SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC925	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC825	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

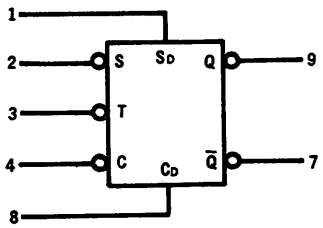
Characteristic	Symbol	Pin Under Test	MC925 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC825 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	2	-	3,5,6	-	14	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,5,6	-	↓	↓
		5	-		-		-			-		-		-			5	-	2,3,6	-		
		6	-		-		-			-		-		-			6	-	2,3,5	-		
Output Current	I_{A5}	1	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	1	-	2,3,5,6	14	7
Output Leakage Current	I_{CEX}	1	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	1	-	-	2,3,5,6	-	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	3,5,6,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	2,5,6,7
			-		-		-			-		-		-			-	5	-	-		2,3,6,7
			-		-		-			-		-		-			-	6	-	-		2,3,5,7
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	3,5,6,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	2,5,6,7
			-		-		-			-		-		-			-	-	5	-		2,3,6,7
			-		-		-			-		-		-			-	-	6	-		2,3,5,7
																	Pulse In	Pulse Out				
Switching Time	t	3+1-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	3	1	-	-	14	2,5,6,7
		3-1+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	3	1	-	-	14	2,5,6,7

Ground inputs of gate not under test. Other pins not listed are left open.

MC926 • MC826

Available in TO-100 Metal Can, Add "G" Suffix
Available in TO-91 Flat Package, Add "F" Suffix

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



t_{pd} = 35 ns typ
P_D = 130 mW typ (Only Clock Input High)
65 mW typ (Inputs Low)

DIRECT INPUT OPERATION①

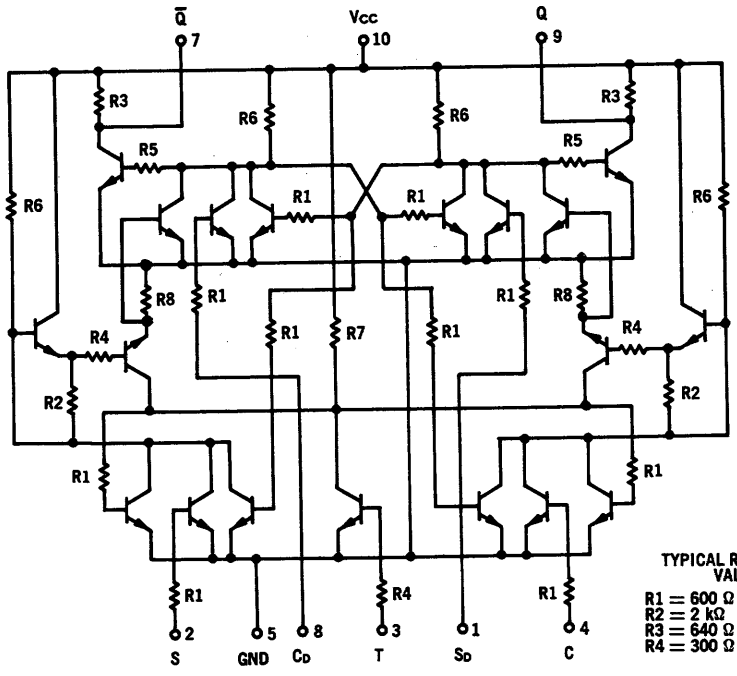
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION③

t_n④		t_{n+1}④	
S	C	Q	$\overline{Q}$
1	1	Q_n⑤	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

① Clock (T) to remain unchanged.
② The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
③ Direct inputs (C_D and S_D) must be low.
④ The time period prior to the negative transistor of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
⑤ Q_n is the state of the Q output in the time period t_n.

"F" PACKAGE AND "G" PACKAGE PIN-OUTS ARE THE SAME.



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 550 Ω
R2 = 2 kΩ	R6 = 900 Ω
R3 = 640 Ω	R7 = 700 Ω
R4 = 300 Ω	R8 = 3 kΩ

ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC926	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC826	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

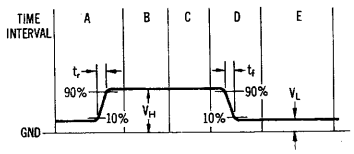
Characteristic	Symbol	Pin Under Test	MC926 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC826 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	-	-	10	5
	I_{in}	2	-	495	-	435	-	470		-	504	-	450	-	450		2	-	8	-		
	$2\,I_{in}$	3	-	990	-	870	-	940		-	1010	-	900	-	900		3	-	2, 4	-		
	I_{in}	4	-	495	-	435	-	470		-	504	-	450	-	450		4	-	1	-		
	I_{in}	8	-	495	-	435	-	470		-	504	-	450	-	450		8	-	-	-		
Output Current	I_{A5}	7	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	7, 8	1	-	10	5
		9	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	1, 9	8	-	10	5
Saturation Voltage	$V_{CE(sat)}$	7	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	1	-	8	10	5
		7#‡	-		-		-			-		-		-			-	2	-	4		
		7#‡	-		-		-			-		-		-			-	-	-	2, 4		
		7§‡	-		-		-			-		-		-			-	2, 4	-	-		
		9	-		-		-			-		-		-			-	8	-	1		
		9§‡	-		-		-			-		-		-			-	4	-	2		
		9#‡	-		-		-			-		-		-			-	2, 4	-	-		
		9§‡	-		-		-			-		-		-			-	-	-	2, 4		

§ Pin 1 = High, # Pin 8 = High } Set by momentary application of V_{BOT} prior to the application of the negative going clock pulse.

‡ Pin 3 = ⌐└

Pins not listed are left open.

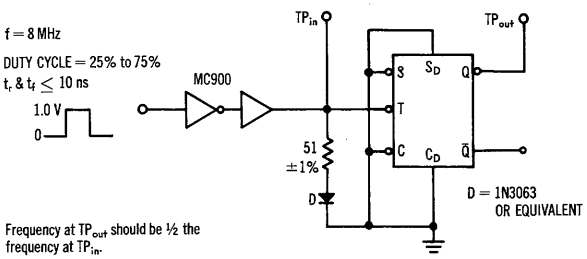
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC826		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC926		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.724 V

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

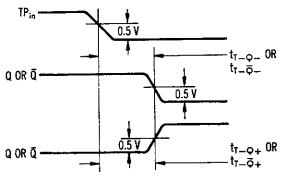
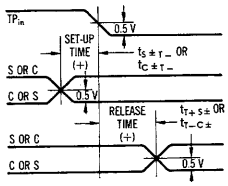
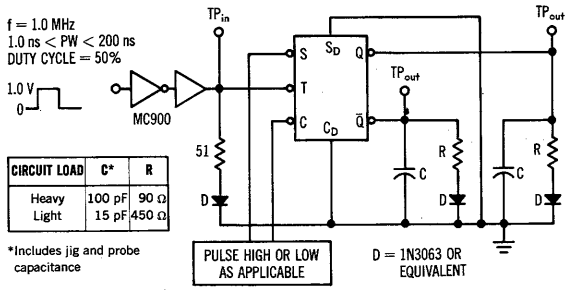


FIGURE 3B — SET-UP AND RELEASE TIME



For definitions of set-up and release times, see General Information Section.

FIGURE 3C — TEST CIRCUIT



CIRCUIT LOAD	C*	R
Heavy	100 pF	90 Ω
Light	15 pF	450 Ω

*Includes jig and probe capacitance

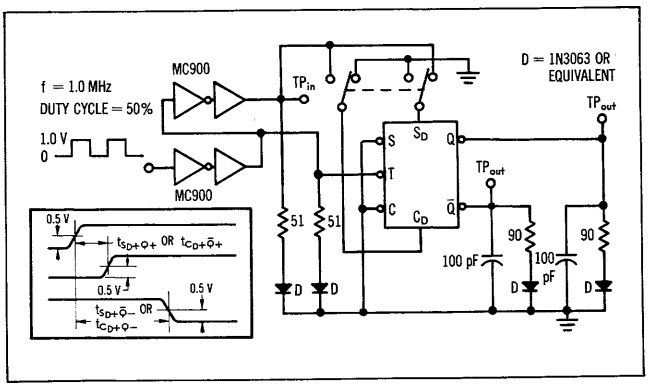
SWITCHING TIMES

Test	Figure No.	Minimum Over Full Temperature Range (ns)	Maximum Over Full Temperature Range (ns)
t_{T-Q-}	3A, 3C	25#	90
$t_{T-\bar{Q}-}$	3A, 3C	25#	90
t_{T-Q+}	3A, 3C	25#	90
$t_{T-\bar{Q}+}$	3A, 3C	25#	90
t_{S+T-}	3B, 3C	—	50
t_{S-T-}	3B, 3C	—	30
t_{C+T-}	3B, 3C	—	50
t_{C-T-}	3B, 3C	—	30
t_{T-S+}	3B, 3C	—	0*
t_{T-S-}	3B, 3C	—	+5*
t_{T-C+}	3B, 3C	—	0*
t_{T-C-}	3B, 3C	—	+5*
t_{C_D+} or t_{S_D-} to output −	4	—	90
t_{C_D+} or t_{S_D+} to output +	4	—	70

Lightly loaded

* Negative switching time means the inputs can momentarily change before the clock pulse transition.

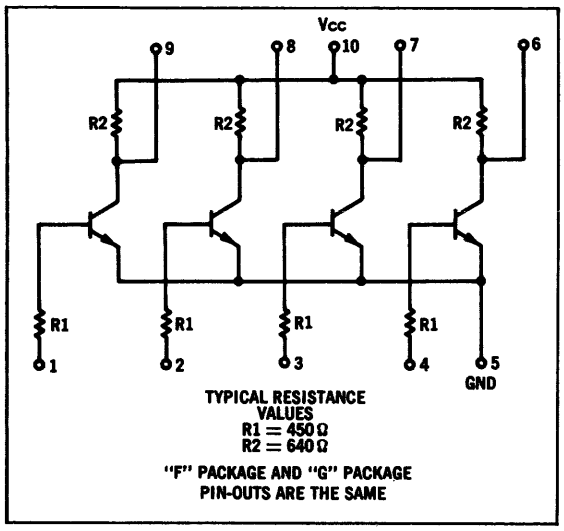
FIGURE 4 — DIRECT CLEAR PROPAGATION DELAY TIME



MC927 • MC827

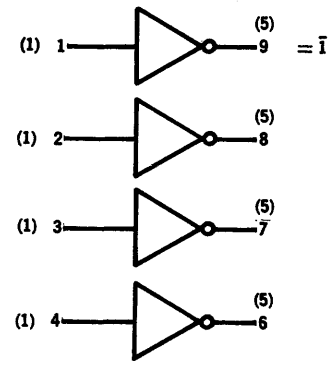
Available in TO-100 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Four individual circuits each perform the simple inversion function.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

"F" PACKAGE AND "G" PACKAGE PIN-OUTS ARE THE SAME

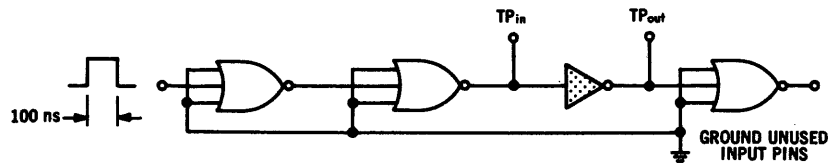


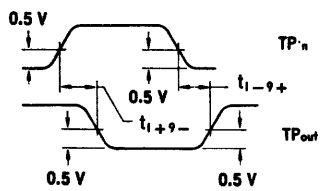
Number in parenthesis indicates MRTL loading factor.

t_{pd} = 12 ns typ

P_D = 76 mW typ (Input High)
20 mW typ (Inputs Low)

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.
Other inverters are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC927	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC827	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC927 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC827 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	1*	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	*	-	10	5
Output Current	I_{A5}	6	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	6	-	4	10	5
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	6	-	-	4	-	5
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	4	1, 2, 3	-	10	5
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1, 2, 3, 4	-	10	5
																	Pulse In	Pulse Out				
Switching Time	t	1+9- 1-9+	- -	- -	- -	20 28	- -	- -	ns ns	- -	- -	- -	20 28	- -	- -	ns ns	1 1	9 9	- -	- -	10 10	5 5

* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V_{BOT}.

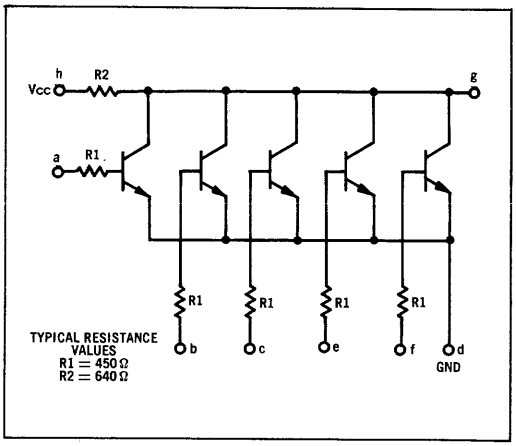
Ground inputs of inverters not used in test.

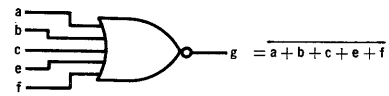
Other pins not listed are left open

MC929 • MC829

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Provides positive logic NOR function. Individual gates may be paralleled with other logic elements for increasing the number of inputs (subject to loading rules).

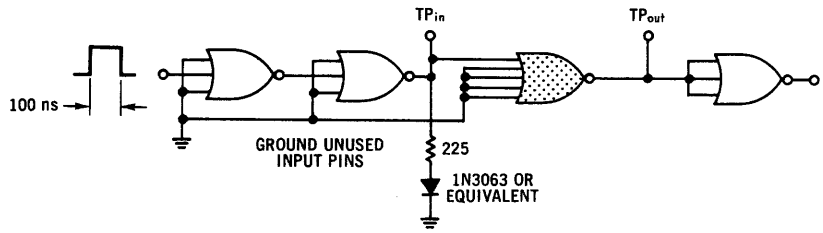


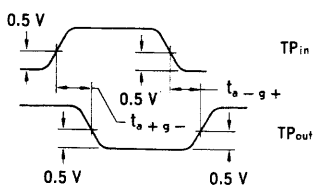


PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC929	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC829	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

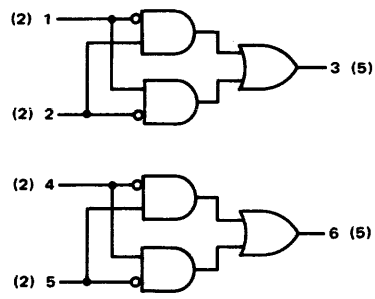
Characteristic	Symbol	Pin Under Test	MC929 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC829 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	a	-	b, c, e, f	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c, e, f	-	↓	↓
		c	-		-		-			-		-		-			c	-	a, b, e, f	-		
		e	-		-		-			-		-		-			e	-	a, b, c, f	-		
		f	-		-		-			-		-		-			f	-	a, b, c, e	-		
Output Current	I_{A5}	g	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	g	-	a,b,c,e,f	h	d
Output Leakage Current	I_{CEX}	g	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	g	-	-	a,b,c,e,f	-	d
Output Voltage	V_{out}	g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	↓
			-		-		-			-		-		-			-	c	-	-		
			-		-		-			-		-		-			-	e	-	-		
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	f	-	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	g	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	b	-	↓	↓
			-		-		-			-		-		-			-	-	c	-		
			-		-		-			-		-		-			-	-	e	-		
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	f	-	↓	↓
																	Pulse In	Pulse Out				
Switching Time	t	a+g-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	a	g	-	-	h	b,c,d,e,f
		a-g+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	a	g	-	-	h	b,c,d,e,f

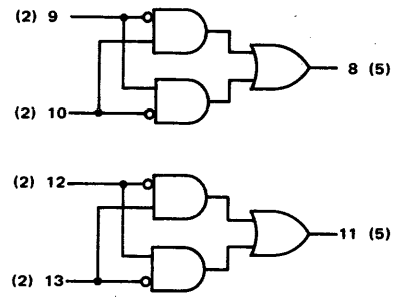
Pins not listed are left open.

MC971 • MC871

Available in TO-86 flat package, add "F" suffix

Four gate arrays designed to provide the Exclusive OR function. The output is high only if one input is high and all other inputs are low.





POSITIVE LOGIC
$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns typ
P_D = 72 mW typ

NUMBER IN PARENTHESIS INDICATES
MRTL LOADING FACTOR

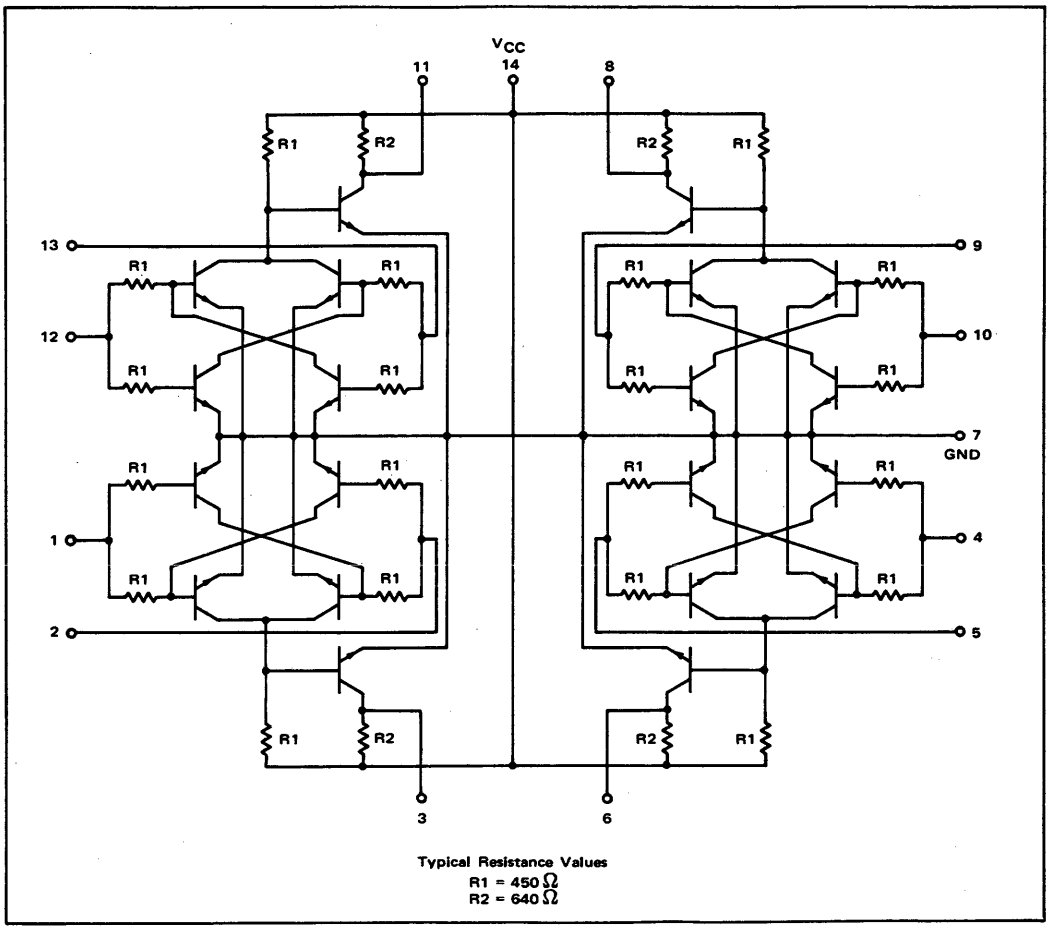
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gates are tested in the same manner.

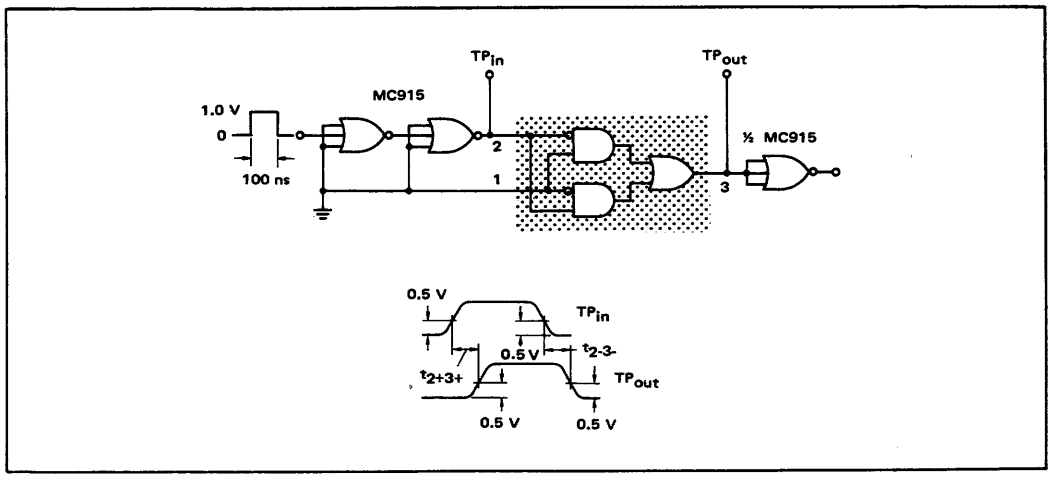
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC971	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC871	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC971 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC871 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	1	-	990	-	870	-	940	μAdc	-	1008	-	900	-	900	μAdc	1	-	2	-	14	7
		2	-	990	-	870	-	940	μAdc	-	1008	-	900	-	900	μAdc	2	-	1	-	14	7
Output Current	I_{A5}	3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	1,3	-	2	14	7
		3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	2,3	-	1	14	7
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	-	-	1,2	14	7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1,2	-	-	14	7
Switching Time	t																Pulse In		Pulse Out			
		1-3-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	2	3	-	14	7
		1-3+	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	1	2	↓	-	↓	↓
		2-3+	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	2	-	↓	1	↓	↓
		2-3-	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	2	-	↓	1	↓	↓

Ground inputs of gates not under test. Other pins not listed are left open.



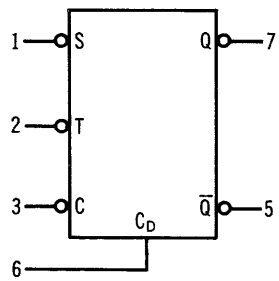
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



MC974 • MC874

Available in TO-99 metal can, add "G" suffix.

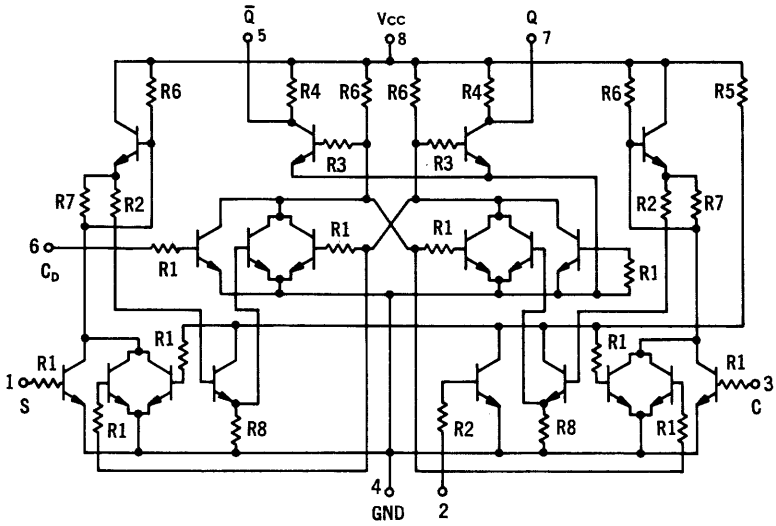
J-K flip-flop with a direct clear input
in addition to the clocked inputs.



CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

① Direct input (C_D) must be low.
② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
③ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 700 Ω
R2 = 300 Ω	R6 = 900 Ω
R3 = 550 Ω	R7 = 2k Ω
R4 = 640 Ω	R8 = 3k Ω

ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC974	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC874	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC974 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC874 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	6	-	8	4
	$2\ I_{in}$*	2	-	990	-	870	-	940		-	1008	-	900	-	900		2	-	1,3	-		
	I_{in}	3 Δ	-	495	-	435	-	470		-	504	-	450	-	450		3	-	-	-		
	I_{in}	6	-	495	-	435	-	470		-	504	-	450	-	450		6	-	-	-		
Output Current	I_{A5}	5	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	5,6	-	-	8	4
		7 Δ	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	7	-	-	8	4
Saturation Voltage	$V_{CE(sat)}$	5‡§	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	1	-	3	8	4
		5‡§	-		-		-			-		-		-			-	-	-	1,3		
		5Δ§	-		-		-			-		-		-			-	1,3	-	-		
		7Δ	-		-		-			-		-		-			-	6	-	-		
		7‡§	-		-		-			-		-		-			-	1,3	-	-		
		7Δ§	-		-		-			-		-		-			-	3	-	1		
		7Δ§	-		-		-			-		-		-			-	-	-	1,3		

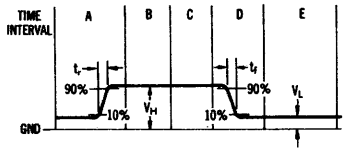
Pins not listed are left open.

Δ Preset the flip-flop by the following procedure:
(1) Momentarily apply V_{BOT} to pin 6 to preclear flip-flop.
(2) After V_{BOT} is removed from pin 6, ground pins 1 and 3.
(3) Apply a negative-going clock pulse to pin 2 (see note §) while pins 1 and 3 are still grounded. This changes the state of the flip-flop to the SET condition.
(4) Remove the grounds from pins 1 and 3, and proceed with the test.

‡ Momentarily apply V_{BOT} to pin 6 prior to the arrival of the negative-going clock pulse to effect a change of state.

§ Clock Pulse to pin 2.

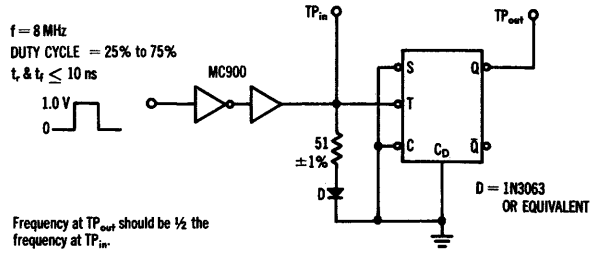
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



Frequency at TP_{out} should be ½ the frequency at TP_{in}.

MC874		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

MC974		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	1.064 V

All voltages ±10 mV

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

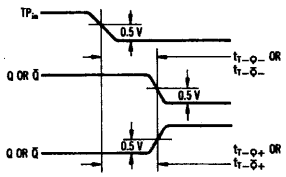
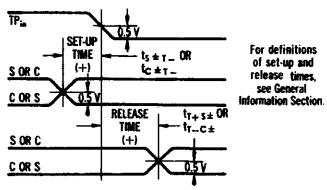
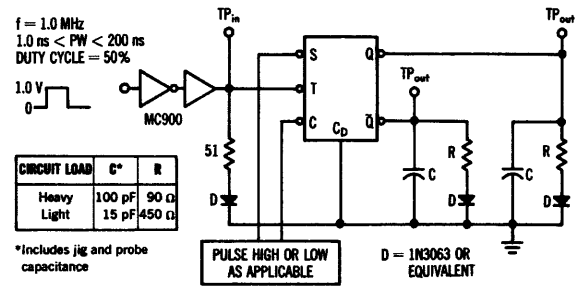


FIGURE 3B — SET-UP AND RELEASE TIME



For definitions of set-up and release times, see General Information Section.

FIGURE 3C — TEST CIRCUIT



CIRCUIT LOAD	C*	R
Heavy	100 pF	90 Ω
Light	15 pF	450 Ω

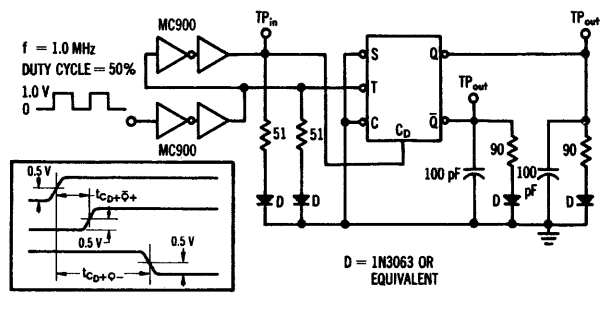
*Includes jig and probe capacitance

SWITCHING TIMES

Test	Figure No.	Minimum Over Full Temperature Range (ns)	Maximum Over Full Temperature Range (ns)
t_{T-Q-}	3A, 3C	25#	90
$t_{T-\bar{Q}-}$	3A, 3C	25#	90
t_{T-Q+}	3A, 3C	25#	90
$t_{T-\bar{Q}+}$	3A, 3C	25#	90
t_{S+T-}	3B, 3C	—	50
t_{S-T-}	3B, 3C	—	30
t_{C+T-}	3B, 3C	—	50
t_{C-T-}	3B, 3C	—	30
t_{T-S+}	3B, 3C	—	0*
t_{T-S-}	3B, 3C	—	+5*
t_{T-C+}	3B, 3C	—	0*
t_{T-C-}	3B, 3C	—	+5*
t_{C_D+Q-}	4	—	90
$t_{C_D+\bar{Q}+}$	4	—	70

Lightly loaded * Negative switching time means the inputs can momentarily change before the clock pulse transition.

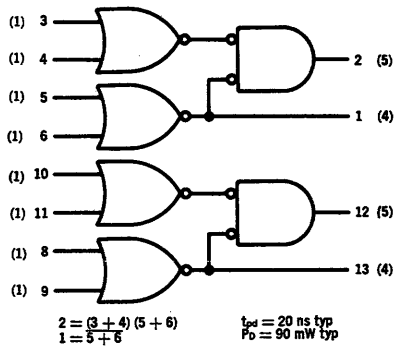
FIGURE 4 — DIRECT CLEAR PROPAGATION DELAY TIME



MC975 • MC875

Available in TO-86 flat package, add "F" suffix.

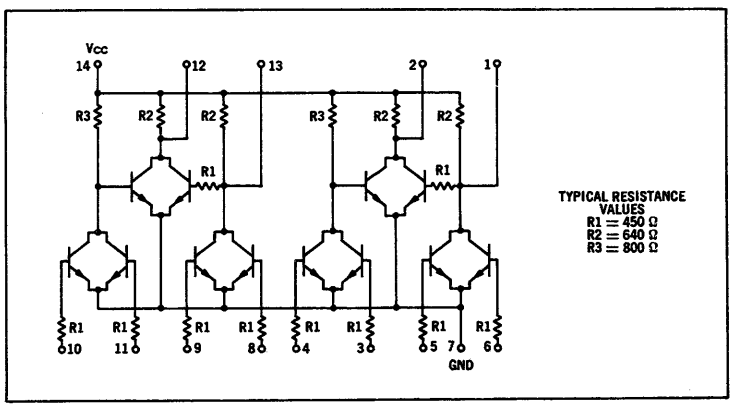
A dual half-adder device contained in a single package. Each can be used to supply the SUM and CARRY operations on two input signals. For example, if the inputs are applied to pins 3 and 4, and their complements to pins 5 and 6, the SUM of the inputs appears on pin 2 while the CARRY appears on pin 1.



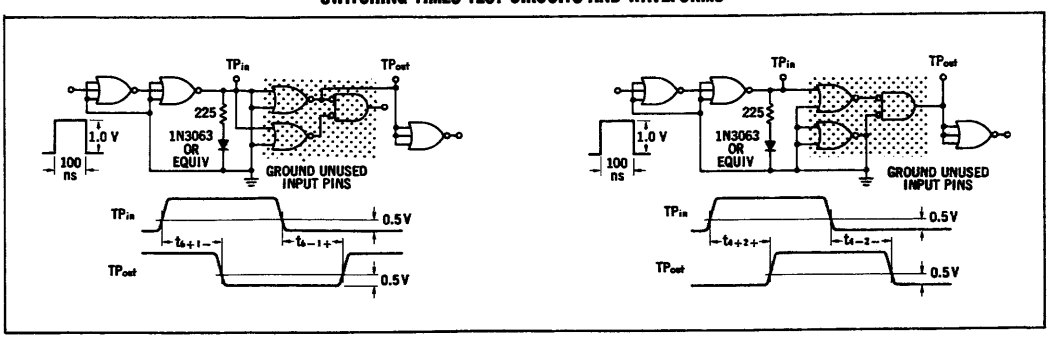
$2 = \overline{(3+4)\,(5+6)}$ $\quad 1 = \overline{5+6}$

$t_{pd} = 20$ ns typ
$P_D = 90$ mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.



SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-adder only.
The other half-adder is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC975	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC875	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

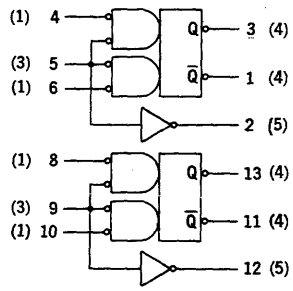
Characteristic	Symbol	Pin Under Test	MC975 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC875 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	3	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	3	-	4	-	14	7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	4	-	3	-	↓	↓
		5	-		-		-			-		-		-			5	-	6	-		
		6	-		-		-			-		-		-			6	-	5	-		
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1	-	5, 6	14	7
	I_{A5}	2	2.47	-	2.54	-	2.35	-		2.52	-	2.38	-	2.25	-		-	2, 3, 5	-	-	↓	↓
	I_{A5}	2	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	2, 4, 6	-	-		
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	5	-	-	14	7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	6	-	-	↓	↓
		2	-		-		-			-		-		-			-	1	3, 4	-		
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	5	-	14	7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	6	-	↓	↓
		2	-		-		-			-		-		-			-	-	3, 4	5, 6		
		2	-		-		-			-		-		-			-	-	5, 6	3, 4		
																	Pulse In	Pulse Out				
Switching Time	t	6+1-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	6	1	-	-	14	7
		6-1+	-	-	-	30	-	-		-	-	-	30	-	-		6	1	-	-		7
		4+2+	-	-	-	36	-	-		-	-	-	36	-	-		4	2	-	-		1, 7
		4-2-	-	-	-	36	-	-	↓	-	-	-	36	-	-	↓	4	2	-	-	↓	1, 7

Ground input pins of half-adder not under test. Other pins not listed are left open.

MC983 • MC883

Available in TO-86 flat package, add "F" suffix.

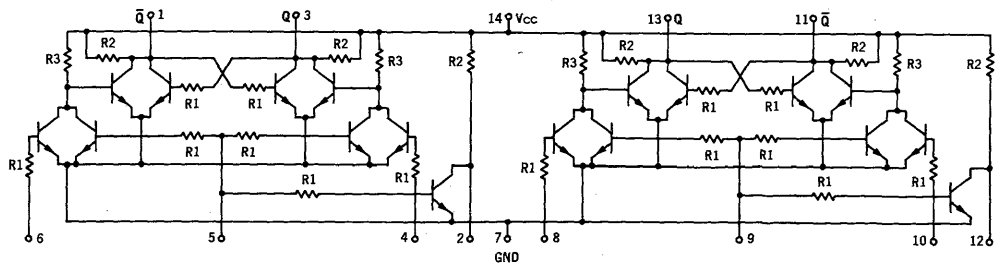
Two half-shift registers in a single package, each having a built-in inverter for the gating signal. For example, information coming in on pins 4 and 6 will be transferred to pins 3 and 1 when the gating signal, pin 5, goes low. If all three inputs, 4, 5, and 6, are low, the outputs, 1 and 3, will both be low.



$1 = \overline{3}\,(6 + 5)$
$3 = \overline{1}\,(5 + 4)$
$2 = \overline{5}$

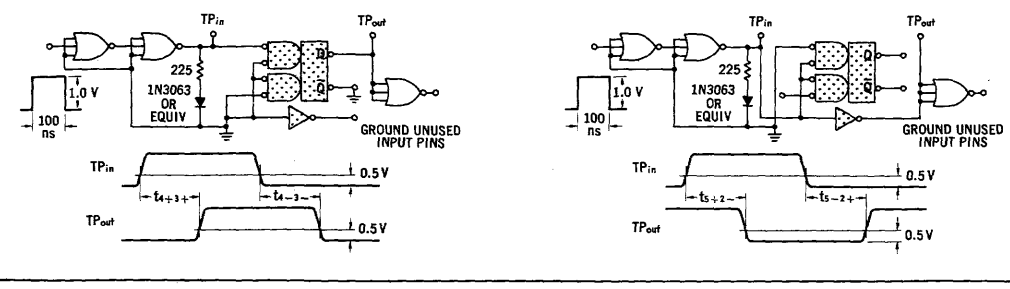
$t_{pd} = 22$ ns typ
$P_D = 110$ mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-shift register only.
The other half-shift register is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC983	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC883	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

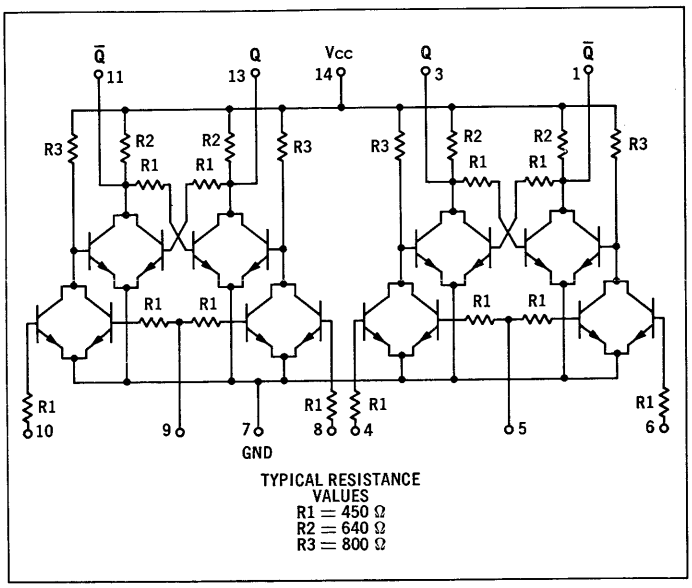
Characteristic	Symbol	Pin Under Test	MC983 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC883 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	4	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	4	-	5	-	14	7
	$3I_{in}$	5	-	1485	-	1305	-	1410	↓	-	1512	-	1350	-	1350	↓	5	-	4, 6	-	↓	↓
	I_{in}	6	-	495	-	435	-	470		-	504	-	450	-	450		6	-	5	-		
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1, 5	-	-	14	3*, 7
	I_{A4}	1	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	1, 6	-	-	↓	7
	I_{A5}	2	2.47	-	2.54	-	2.35	-		2.52	-	2.38	-	2.25	-		-	2	-	5		7
	I_{A4}	3	1.98	-	2.19	-	1.88	-		2.02	-	2.05	-	1.80	-		-	3, 5	-	-		1*, 7
	I_{A4}	3	1.98	-	2.19	-	1.88	-		2.02	-	2.05	-	1.80	-		-	3, 4	-	-		7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	5, 6	-	14	7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	-	-	↓	↓
		3	-		-		-			-		-		-			-	1	4, 5	-		
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	4, 5, 6	-	14	1*, 7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	5, 6	↓	2, 7
		2	-		-		-			-		-		-			-	-	5	-		7
		3	-		-		-			-		-		-			-	-	4, 5, 6	-		3*, 7
		3	-		-		-			-		-		-			-	-	-	5, 6		1, 7
Switching Time	t	4+3+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In 4	Pulse Out 3	-	-	14	1, 7
		4-3-	-	-	-	40	-	-	↓	-	-	-	40	-	-	↓	4	3	-	-	↓	1, 7
		5+2-	-	-	-	28	-	-		-	-	-	28	-	-		5	2	-	-		7
		5-2+	-	-	-	24	-	-		-	-	-	24	-	-		5	2	-	-		7

Ground input pins of half-shift register not under test. Other pins not listed are left open. *Momentary ground.

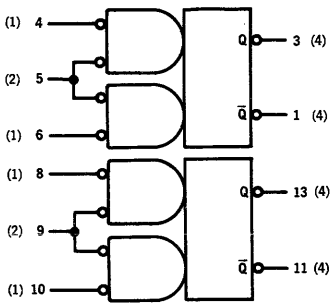
MC984 • MC884

Available in TO-86 flat package, add "F" suffix.

This bistable storage element consists of two half-shift registers in a single package. For example, information coming in on pins 4 and 6 will be transferred to pins 3 and 1 when the gating signal, pin 5, goes low. If all three inputs, 4, 5, and 6, are low, the outputs, 3 and 1, will both be low.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

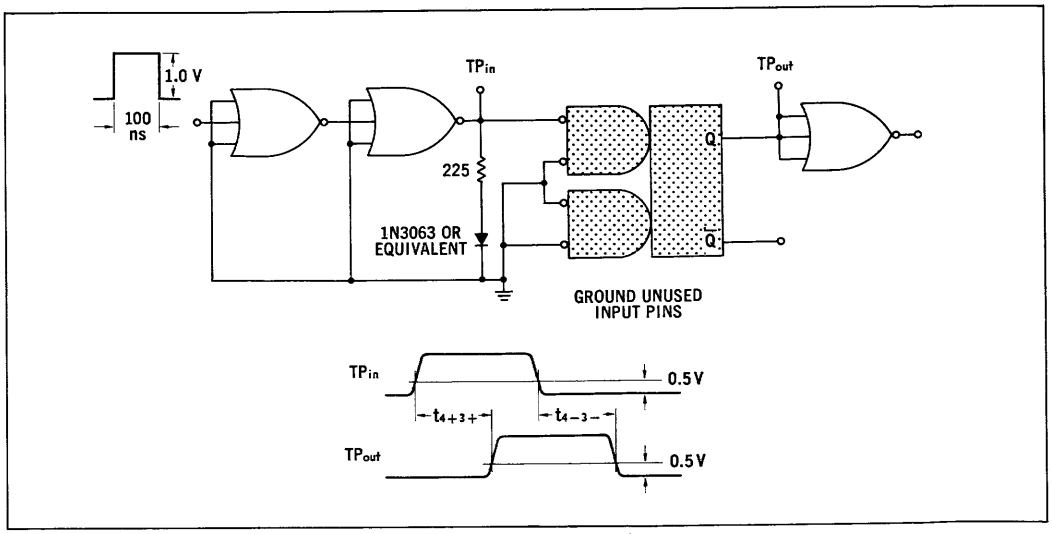


$3 = \overline{1}\,(4 + 5)$
$1 = \overline{3}\,(6 + 5)$

t_{pd} = 22 ns typ
P_D = 75 mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures shown are for one half-shift register only.
The other half-shift register is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC984	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC884	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

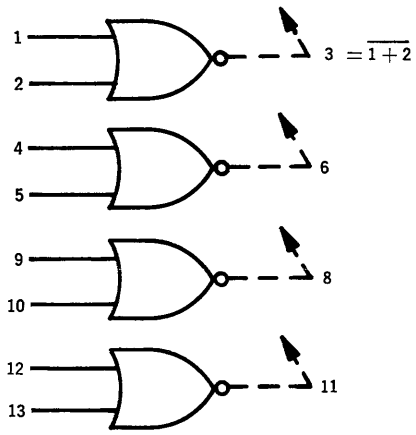
Characteristic	Symbol	Pin Under Test	MC984 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC884 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	4	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	4	-	5	-	14	7
	$2I_{in}$	5	-	990	-	870	-	940	↓	-	1008	-	900	-	900	↓	5	-	4, 6	-	↓	↓
	I_{in}	6	-	495	-	435	-	470		-	504	-	450	-	450		6	-	5	-		
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1, 5	-	-	14	3*, 7
		1	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	1, 6	-	-		7
		3		-		-		-			-		-		-		-	3, 5	-	-		1*, 7
		3		-		-		-			-		-		-		-	3, 4	-	-	↓	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	5, 6	-	14	7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	4, 5	-	14	7
Saturation Voltage	V_{CE}	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	4, 5, 6	-	14	1*, 7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	5, 6	↓	3, 7
		3	-		-		-			-		-		-			-	-	-	4, 5, 6		3*, 7
		3	-		-		-			-		-		-			-	-	-	4, 5		1, 7
Switching Time	t	4+3+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In 4	Pulse Out 3	-	-	14	1, 7
		4-3-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	4	3	-	-	14	1, 7

Ground input pins of half-shift register not under test. Other pins not listed are left open. *Momentary ground.

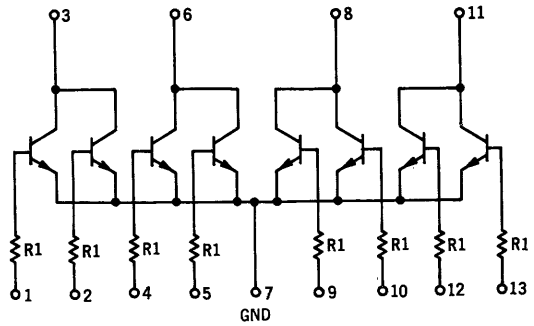
MC985 • MC885

Available in TO-86 flat package, add "F" suffix.

Four 2-input expanders housed in a single package increase the input capability of MRTL gates.



When an expander is added to a gate, subtract 0.4 load unit from the output of the gate for each expander circuit added.



V_{CC} connection to pin 14 not shown.

TYPICAL RESISTANCE VALUE
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
Other expanders are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC985	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC885	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC985 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC885 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	2	-	14	3	7
		2	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	2	-	1	-	14	3	7
Output Leakage Current	I_{CEX}	3	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	3	-	-	1,2	14	-	7
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	3	2,7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	3	1,7
Saturation Voltage	$V_{CE(sat)}$	3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	3	2,7
		3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	3	1,7

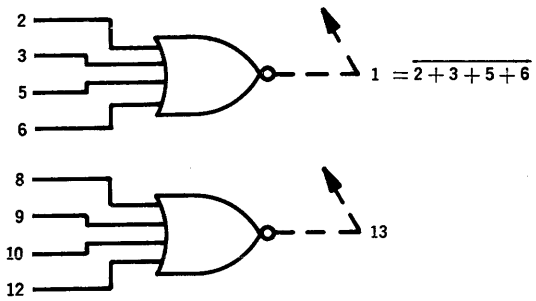
Ground inputs of expanders not under test. Other pins not listed are left open.

* Resistor Value to V_{CC}

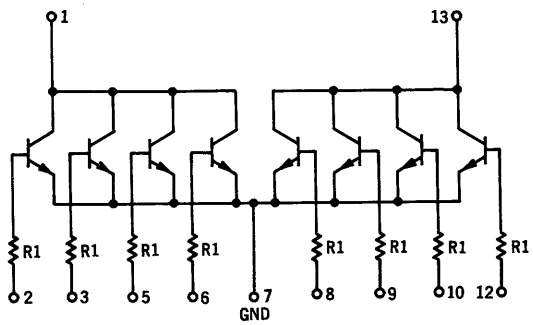
MC986 • MC886

Available in TO-86 flat package, add "F" suffix.

Two 4-input gate expanders housed in a single package may be used independently or combined. Each of these expanders increases the input capability of a standard MRTL gate by four.



When an expander is added to a gate, subtract 0.4 load unit from the output of the gate for each expander circuit added.



V_{CC} connection to pin 14 not shown.

TYPICAL RESISTANCE VALUE
R1 = 450Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expander is tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC986	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC886	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

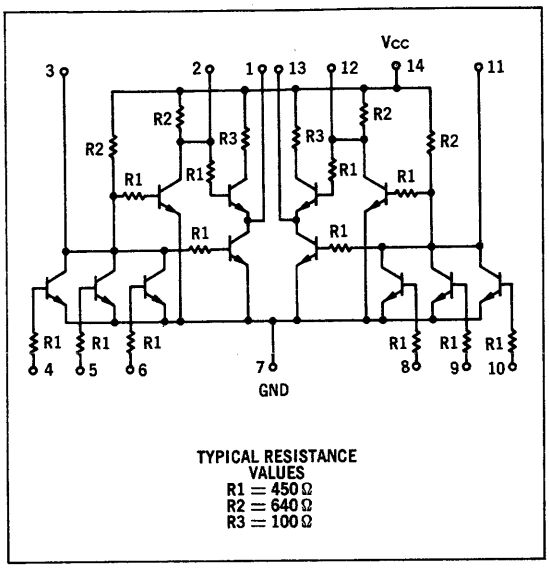
Characteristic	Symbol	Pin Under Test	MC986 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC886 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	2	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	2	-	3,5,6	-	14	1	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,5,6	-	↓	↓	↓
		5	-		-		-			-		-		-			5	-	2,3,6	-			
		6	-		-		-			-		-		-			6	-	2,3,5	-			
Output Leakage Current	I_{CEX}	1	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	1	-	-	2,3,5,6	14	-	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	1	3,5,6,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓	2,5,6,7
			-		-		-			-		-		-			-	5	-	-			2,3,6,7
			-		-		-			-		-		-			-	6	-	-			2,3,5,7
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	1	3,5,6,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	↓	2,5,6,7
			-		-		-			-		-		-			-	-	5	-			2,3,6,7
			-		-		-			-		-		-			-	-	6	-			2,3,5,7

Ground inputs of expander not under test. Other pins not listed are left open.

* Resistor Value to V_{CC}.

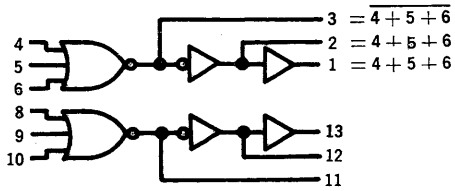
MC988 • MC888

Available in TO-86 Flat Package, Add "F" Suffix.



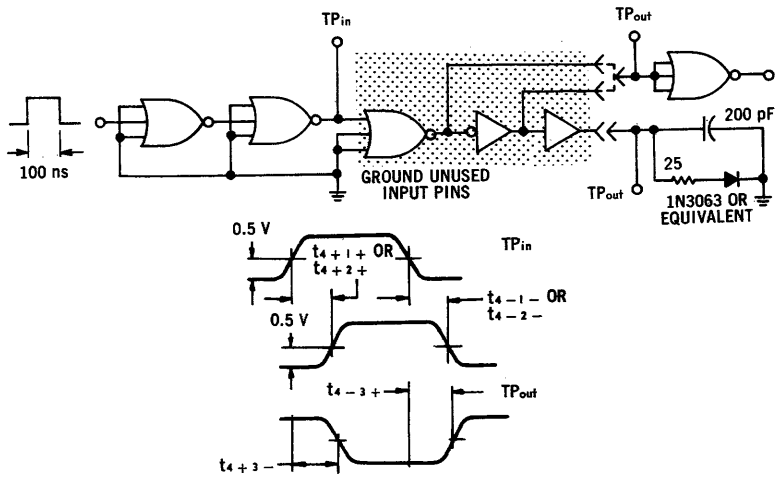
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω

Two 3-input positive logic NOR gates, each followed by an inverting and a non-inverting high fan-out amplifier, are provided in a single package. For each section, the output from each stage is available. If more than one output is used, however, the full loading factors cannot be employed since each output provides the drive for the succeeding stage.



Outputs 1, 2, or 3 may not be used simultaneously.
Outputs 11, 12, or 13 may not be used simultaneously.

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



Test each output independently. For each test, use only the load associated with the output under test (pin 2 test uses the same load as pin 3 test). Outputs not under test should be left open.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC988	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC888	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC988 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC888 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	4	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	4	-	5,6	-	14	-	7
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	5	-	4,6	-	↓	-	↓
		6	-		-		-			-		-		-			6	-	4,5	-		-	
Output Current	I_{AB}	1	12.4	-	12.7	-	11.8	-	mAdc	12.6	-	11.9	-	11.25	-	mAdc	-	1	-	3	14	-	7,11
	I_{A5}	2	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	2	-	3	↓	-	7,11
	I_{A3}	3	1.48	-	1.52	-	1.41	-		1.51	-	1.43	-	1.35	-		-	3	-	4,5,6		-	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	-	-	14	1	4,5,6,7,11
		2	-		-		-			-		-		-			-	3	-	-		-	4,5,6,7,11
		3	-		-		-			-		-		-			-	6	-	-		-	4,5,7
		3	-		-		-			-		-		-			-	5	-	-		-	4,6,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	4	-	-	↓	-	5,6,7
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	3	-	14	1	4,5,6,7,11
		2	-		-		-			-		-		-			-	-	3	-		-	4,5,6,7,11
		3	-		-		-			-		-		-			-	-	6	-		-	4,5,7
		3	-		-		-			-		-		-			-	-	5	-		-	4,6,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	4	-	↓	-	5,6,7
																	Pulse In	Pulse Out					
Switching Time	t	4+1+	-	-	-	65	-	-	ns	-	-	-	65	-	-	ns	4	1	-	-	14	-	5,6,7
		4-1-	-	-	-	58	-	-	↓	-	-	-	58	-	-	↓	4	1	-	-	↓	-	↓
		4+2+	-	-	-	42.5	-	-		-	-	-	42.5	-	-		4	2	-	-		-	
		4-2-	-	-	-	42.5	-	-		-	-	-	42.5	-	-		4	2	-	-		-	
		4+3-	-	-	-	20	-	-		-	-	-	20	-	-		4	3	-	-		-	
		4-3+	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	4	3	-	-	↓	-	↓

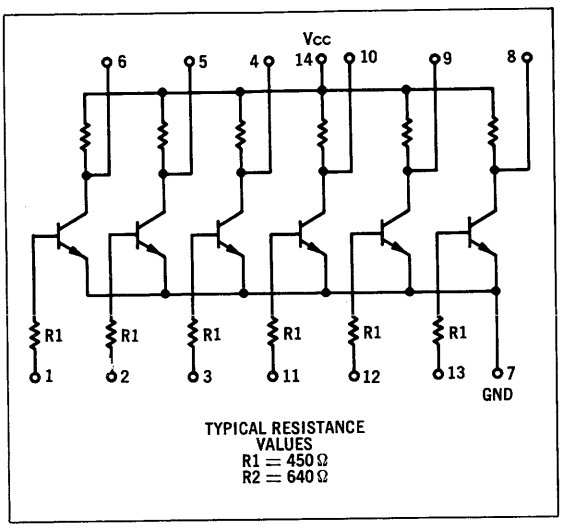
Ground inputs of buffer not under test. Other pins not listed are left open.

* Resistor Value to V_{CC}.

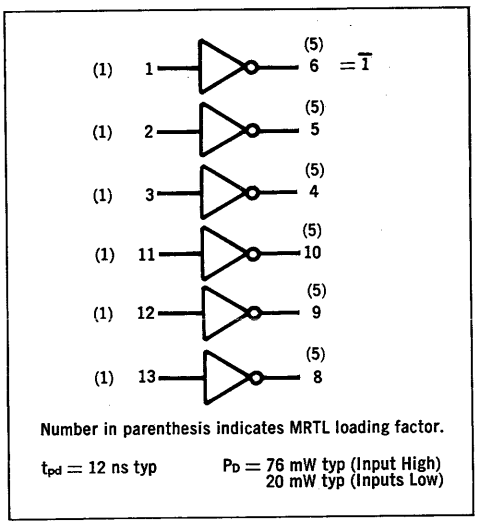
MC989 • MC889

Available in TO-86 flat package, add "F" suffix.

Six individual circuits are contained in a package. Each provides the simple inversion function.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

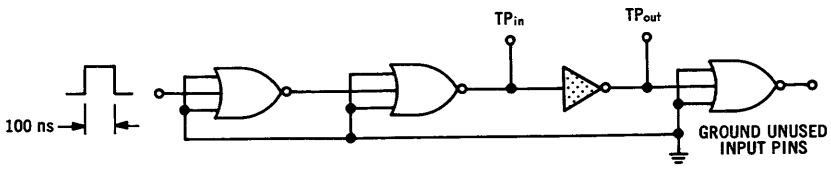


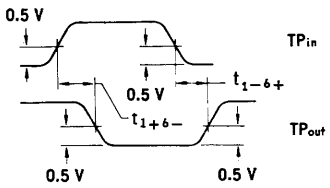
Number in parenthesis indicates MRTL loading factor.

t_{pd} = 12 ns typ

P_D = 76 mW typ (Input High)
20 mW typ (Inputs Low)

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.
Other inverters are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC989	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC889	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC989 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC889 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1 *	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	1	-	-	-	14	7
Output Current	I_{A5}	6	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	6	-	1	14	7
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	6	-	-	1	-	7
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	7
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	7
																	Pulse In	Pulse Out				
Switching Time	t	1+6-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	1	6	-	-	14	7
		1-6+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	1	6	-	-	14	7

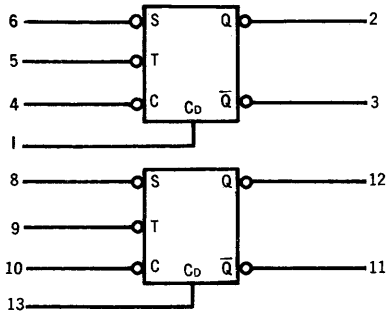
Ground inputs of inverters not used in test. Other pins not listed are left open.

* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V_{BOT}.

MC990 • MC890

Available in TO-86 flat package, add "F" suffix.

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



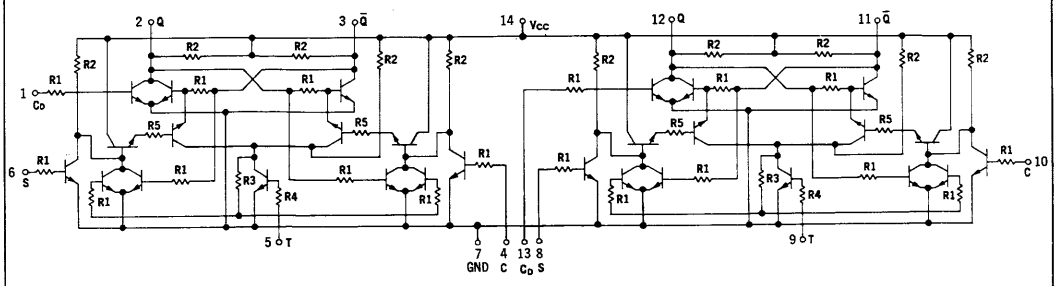
CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

① Direct input (C_D) must be low

② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

③ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω
R5 = 300 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only. The other flip-flop is tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC990	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC890	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC990 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC890 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	3	-	14	4, 5, 6, 7
	I_{in}	4	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	4	-	2	-	↓	1, 5, 6, 7
	2 I_{in}	5	-	990	-	870	-	940	↓	-	1010	-	900	-	900	↓	5	-	4, 6	-	↓	1, 7
	I_{in}	6	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	6	-	3	-	↓	1, 4, 5, 7
Output Current	I_{A3}	2#	1.48	-	1.52	-	1.41	-	mAdc	1.51	-	1.43	-	1.35	-	mAdc	-	2	4	1	14	5, 6, 7
		3	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3	1, 6	-	↓	4, 5, 7
		3	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	1, 3	6	-	↓	4, 5, 7
Output Voltage	V_{out}	2	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	3, 4, 5, 6, 7
		2Δ§	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	4, 6	-	-	↓	1, 7
		2#§	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	4	-	6	↓	1, 7
		2#§	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	4, 6	↓	1, 7
		2†	-	-	-	-	-	-	↓	-	-	-	-	-	-	↓	-	-	-	-	↓	1, 6, 7
		2*	-	-	-	-	-	-	↓	-	-	-	-	-	-	↓	-	-	-	-	↓	1, 6, 7
		3#§	-	710	-	↓	-	320	↓	-	574	-	↓	-	370	↓	-	4, 6	-	-	↓	1, 7
		3Δ§	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	6	-	4	↓	
		3Δ§	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	4, 6	↓	
Saturation Voltage	$V_{CE(sat)}$	2	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	3, 4, 5, 6, 7
		2Δ	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	1, 4, 5, 6, 7
		3#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1	↓	4, 5, 6, 7
Turn On Voltage	V_{on}	2‡	-	-	0.815	-	-	-	Vdc	-	-	0.844	-	-	-	Vdc	-	-	-	-	14	1, 4, 7
		2**	-	-	0.815	-	-	-	Vdc	-	-	0.844	-	-	-	Vdc	-	-	-	-	14	1, 4, 7

Ground inputs of flip-flop not under test. Pins not listed are left open.

\# Pin 3 = LOW } Set by a momentary ground prior to the application of
Δ Pin 2 = LOW } the negative-going clock pulse.

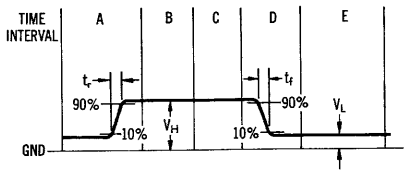
§ Clock Pulse to Pin 5 (See Figure 1)

† Clock Pulse on Pin 5, data pulse on Pin 4 (See Figure 2)
‡ Clock Pulse on Pin 5, data pulse on Pin 6 (See Figure 2)

* Clock Pulse on Pin 5, data pulse on Pin 4, momentary ground on Pin 2 (See Figure 3)
** Clock Pulse on Pin 5, data pulse on Pin 6, momentary ground on Pin 3 (See Figure 3)

CLOCK PULSE DEFINITIONS

FIGURE 1



SEQUENCE OF EVENTS:

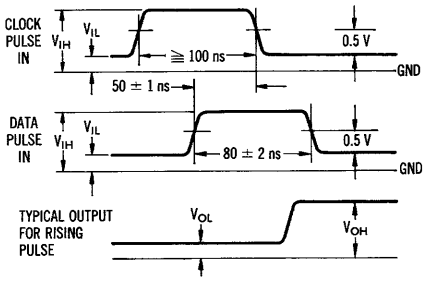
A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC890		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC990		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.674 V

FIGURE 2

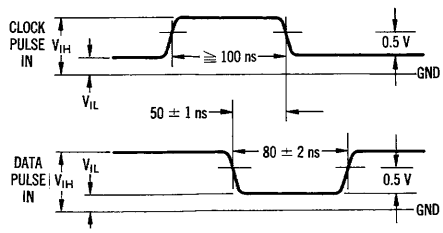


INPUT PULSE REQUIREMENTS:

V_{IL} = 0.200 V max
V_{IH} = 0.894 V min, 1.500 V max
t_r ≦ 10 ns
t_f ≦ 10 ns
f = 1.0 MHz typ

NOTE:
Measurements for output voltages should be taken at least 100 ns after pulses have occurred.

FIGURE 3



INPUT PULSE REQUIREMENTS:

V_{IL} = 0.200 V max
V_{IH} = 0.894 V min, 1.500 V max
t_r ≦ 10 ns
t_f ≦ 10 ns
f = 1.0 MHz typ

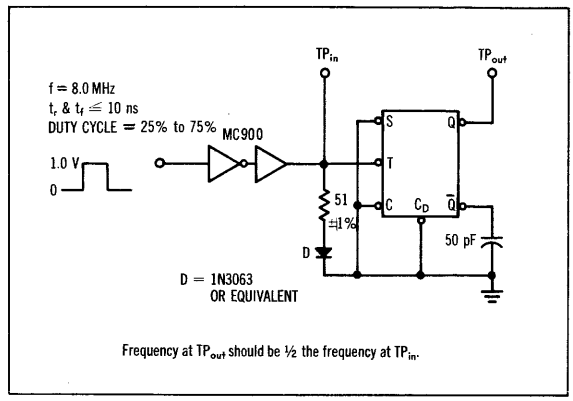
SEQUENCE OF EVENTS:

A. Apply all dc biases required.
B. Apply momentary ground to pin indicated. This sets the flip-flop. Momentary ground must occur before the pulses shown above every time, or the flip-flop will toggle to the wrong condition every alternate pulse.
C. After momentary ground has been released, apply pulses marked above.
D. Measure voltage of designated output after the pulse. Measurements for output voltages should be taken at least 100 ns after pulses have occurred.

SWITCHING TIMES

Test	Figure No.	Maximum (ns) @ 25°C Only	Maximum (ns) Over Full Temperature Range
t_{T-Q-}	5	40	60
t_{T-Q+}	5	80	100
$t_{T-\bar{Q}-}$	5	40	60
$t_{T-\bar{Q}+}$	5	80	100
t_{C_D+Q-}	6	—	50
$t_{C_D-\bar{Q}+}$	6	—	90

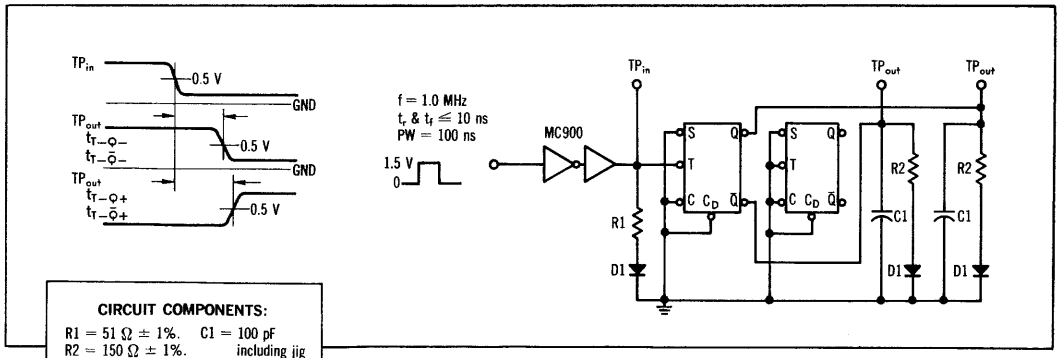
FIGURE 4 — TOGGLE MODE TEST CIRCUIT



Frequency at TP_{out} should be ½ the frequency at TP_{in}.

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 5

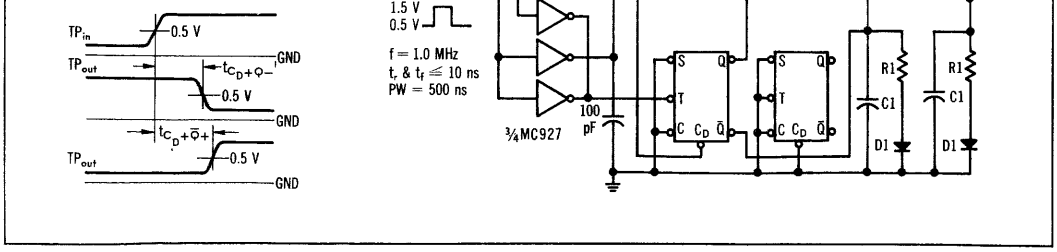


CIRCUIT COMPONENTS:

R1 = 51 Ω ± 1%. C1 = 100 pF including jig and probe.
R2 = 150 Ω ± 1%.
D1 = 1N3063 or equivalent.

NOTE:
The TOG pulse is developed by the inverter and 100 pF capacitor. This pulse returns the state of the flip-flop so that the test pulse can be repeated.

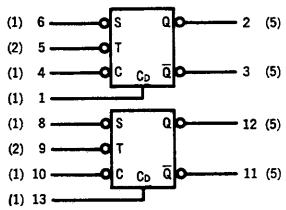
FIGURE 6



MC991 • MC891

Available in TO-86 flat package, add "F" suffix.

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



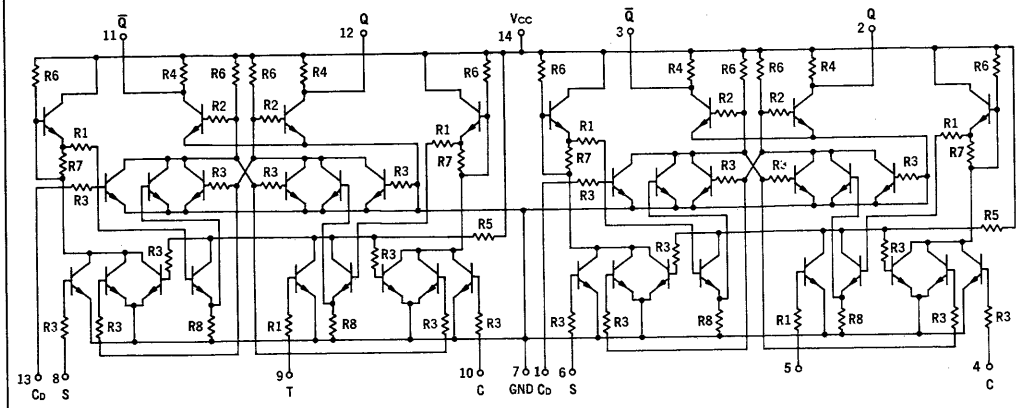
t_{pd} = 40 ns typ
f_{tog} = 4.0 MHz max
P_D = 155 mW typ (Only Clock Input High)
130 mW typ (Inputs Low)

CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.



TYPICAL RESISTANCE VALUES

R1 = 300 Ω R4 = 640 Ω R7 = 2.0 k
R2 = 550 Ω R5 = 700 Ω R8 = 3.0 k
R3 = 600 Ω R6 = 900 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only. The other flip-flop is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC991	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC891	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC991 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC891 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{1n}	4 §	-	495	-	435	-	470	μAdc	-	600	-	600	-	570	μAdc	4	-	-	-	14	7
	$2I_{in}$	5	-	990	-	870	-	940		-	1200	-	1200	-	1140		5	-	4, 6	-		
	I_{in}	6	-	495	-	435	-	470		-	600	-	600	-	570		6	-	1	-		
	I_{in}	1	-	495	-	435	-	470		-	600	-	600	-	570		1	-	-	-		
Output Current	I_{A5}	2 §	2.47	-	2.54	-	2.35	-	mAdc	3.0	-	3.0	-	2.85	-	mAdc	-	2	-	-	14	7
		3	2.47	-	2.54	-	2.35	-	mAdc	3.0	-	3.0	-	2.85	-	mAdc	-	1, 3	-	-	14	7
Output Voltage	V_{out}	2†⑤	-	710	-	300	-	320	mVdc	-	500	-	400	-	400	mVdc	-	4	-	-	14	1, 7
		2‡④	-		-		-			-		-		-			-	-	-	6		
		2†⑥	-		-		-			-		-		-			-	4	-	-		
		2‡⑦	-		-		-			-		-		-			-	-	-	6		
		3†④	-		-		-			-		-		-			-	-	-	4		
		3‡⑤	-		-		-			-		-		-			-	6	-	-		
		3†⑦	-		-		-			-		-		-			-	-	-	4		
		3‡⑥	-		-		-			-		-		-			-	6	-	-		
Saturation Voltage	$V_{CE(sat)}$	2§	-	200	-	210	-	280	mVdc	-	400	-	300	-	350	mVdc	-	1	-	-	14	7
		2* #	-		-		-			-		-		-			-	4, 6	-	-		
		2*§	-		-		-			-		-		-			-	4	-	6		
		2*§	-		-		-			-		-		-			-	-	-	4, 6		
		3* #	-		-		-			-		-		-			-	6	-	4		
		3* #	-		-		-			-		-		-			-	-	-	4, 6		
		3*§	-		-		-			-		-		-			-	4, 6	-	-		

Ground input pins of flip-flop not under test. Other pins not listed are left open.

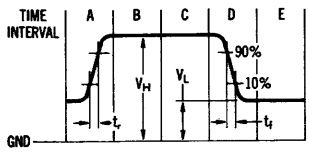
§ Preset the flip-flop by the following procedure:
(1) Momentarily apply V_{BOT} to pin 1 to preclear the flip-flop.
(2) After V_{BOT} is removed from pin 1, ground pins 4 and 6.
(3) Apply a negative-going clock pulse to pin 5 (see note *) while pins 4 and 6 are still grounded. This changes the state of the flip-flop to the SET condition.
(4) Remove the grounds from pins 4 and 6 and proceed with the test.

* Clock pulse to pin 5, see Figure 1.
\# Pin 1 = HIGH, set by a momentary application of V_{BOT} prior to the application of the negative-going clock.

† Clock pulse to pin 5, data pulse to pin 6.
‡ Clock pulse to pin 5, data pulse to pin 4.

④ = See Figure 4.
⑤ = See Figure 5.
⑥ = See Figure 6.
⑦ = See Figure 7.

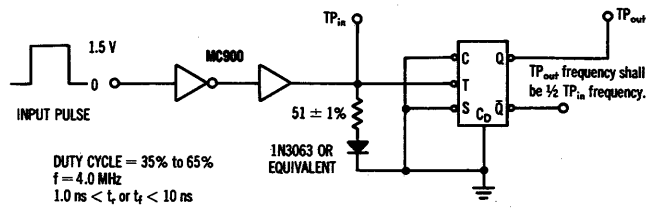
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC991

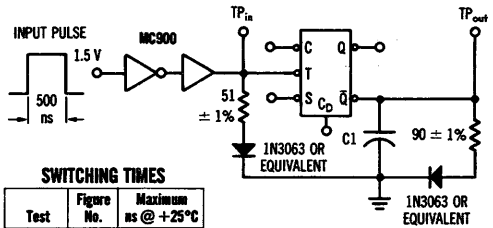
T_A	V_L	V_H
+25°C	+0.565 V ± 10 mV	+0.844 V ± 10 mV
−55°C	+0.710 V ± 10 mV	+1.014 V ± 10 mV
+125°C	+0.320 V ± 10 mV	+0.674 V ± 10 mV

MC891

T_A	V_L	V_H
+25°C	+0.554 V ± 10 mV	+1.430 V ± 10 mV
0°C	+0.574 V ± 10 mV	+1.310 V ± 10 mV
+100°C	+0.370 V ± 10 mV	+1.190 V ± 10 mV

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

FIGURE 3 — SWITCHING TIMES TEST CIRCUIT



SWITCHING TIMES

Test	Figure No.	Maximum ns @ +25°C
t_{T-Q-}	3A	60
t_{T-Q+}	3A	60
$t_{T-\bar{Q}-}$	3A	60
$t_{T-\bar{Q}+}$	3A	60
t_{CD+Q-}	3B	90
$t_{CD+\bar{Q}+}$	3B	70

f = 1.0 MHz
1.0 ns < t_r or t_f < 10 ns

C1 = 100 pF INCLUDING PROBE & JIG CAPACITANCE

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

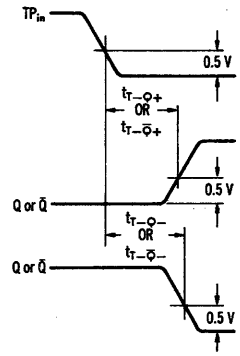
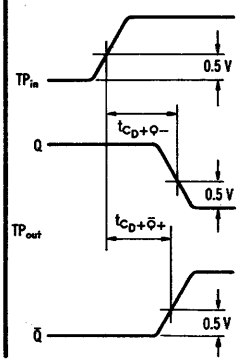
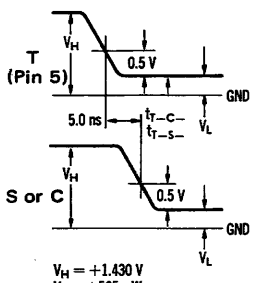


FIGURE 3B — DIRECT CLEAR PROPAGATION DELAY TIME



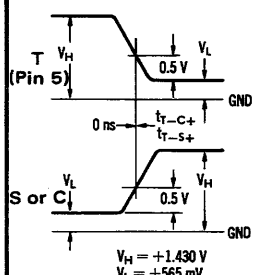
TEST WAVEFORMS FOR V_{out} TESTS

FIGURE 4



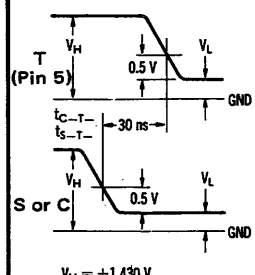
V_H = +1.430 V
V_L = +565 mW
1.0 ns < t_f < 10 ns

FIGURE 5



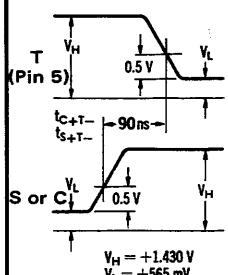
V_H = +1.430 V
V_L = +565 mV
1.0 ns < t_f < 10 ns
1.0 ns < t_r < 10 ns

FIGURE 6



V_H = +1.430 V
V_L = +565 mW
1.0 ns < t_f < 10 ns

FIGURE 7

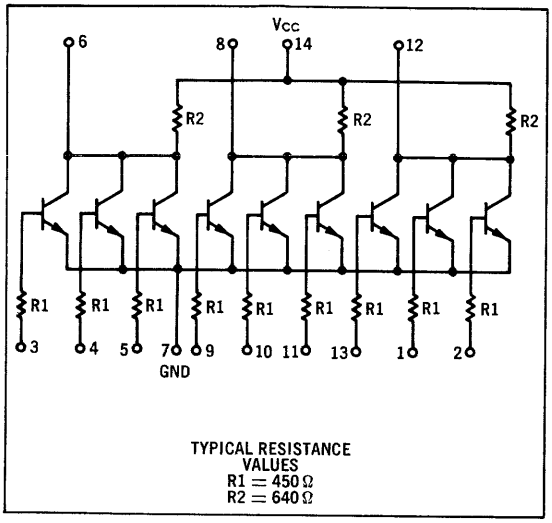


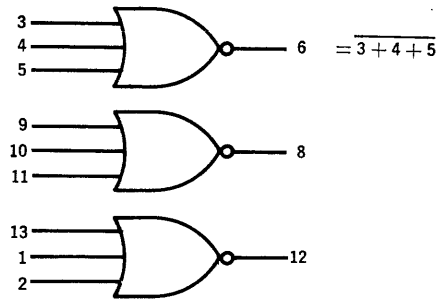
V_H = +1.430 V
V_L = +565 mV
1.0 ns < t_f < 10 ns
1.0 ns < t_r < 10 ns

MC992 • MC892

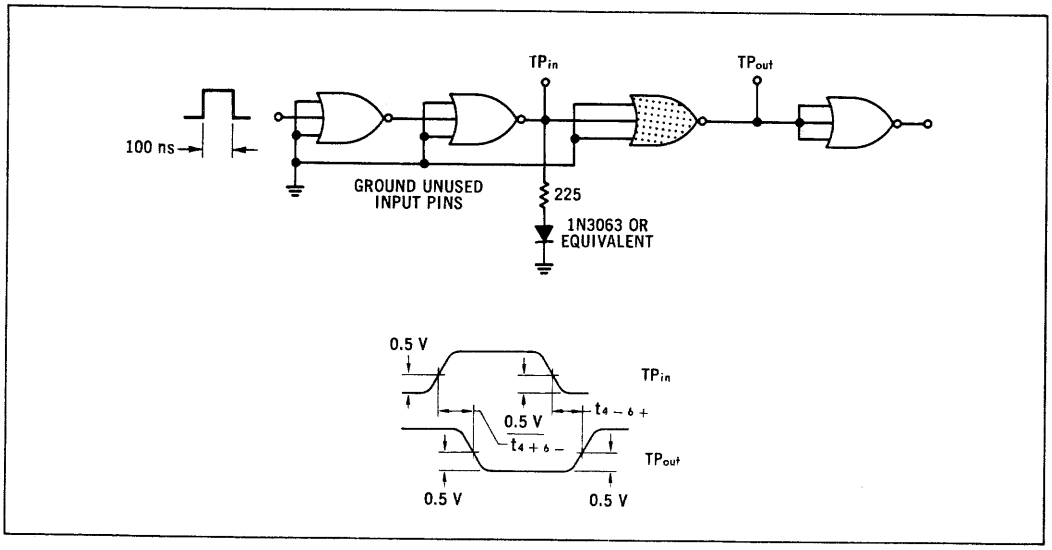
Available in TO-86 Flat Package, Add "F" Suffix.

Three 3-input positive logic NOR gates in a single package may be used independently, paralleled for increased number of inputs (subject to loading rules), or cross coupled to form bistable elements.





SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC992	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC892	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

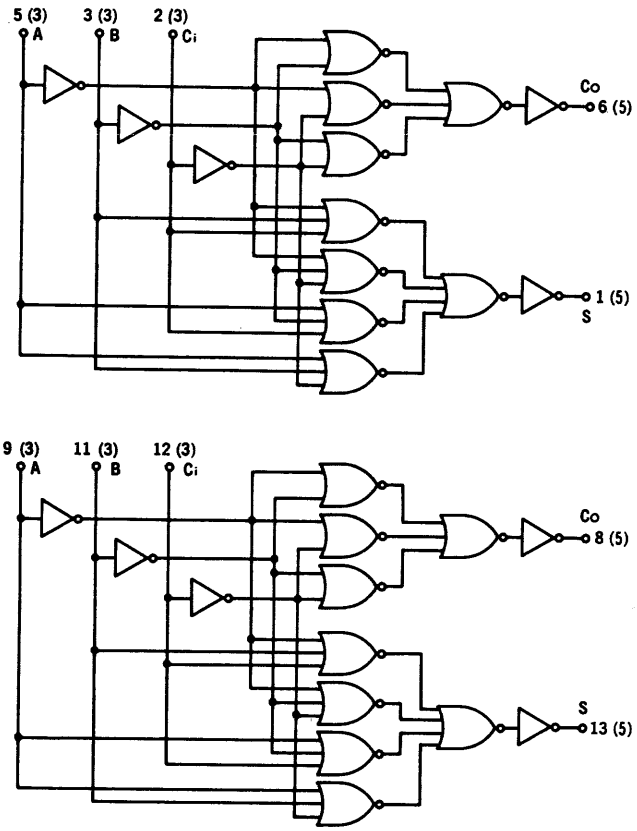
Characteristic	Symbol	Pin Under Test	MC992 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC892 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	3	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	3	-	4,5	-	14	7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	4	-	3,5	-	↓	↓
		5	-		-		-			-		-		-			5	-	3,4	-		
Output Current	I_{A5}	6	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	6	-	3,4,5	14	7
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	6	-	-	3,4,5	-	7
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	-	-	14	4,5,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	4	-	-	↓	3,5,7
			-		-		-			-		-		-			-	5	-	-		3,4,7
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	3	-	14	4,5,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	4	-	↓	3,5,7
			-		-		-			-		-		-			-	-	5	-		3,4,7
Switching Time	t	4+6-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	Pulse In: 4	Pulse Out: 6	-	-	14	3,5,7
		4-6+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	4	6	-	-	14	3,5,7

Ground inputs of gates not under test. Other pins not listed are left open.

MC996 • MC896

Available in TO-86 flat package, add "F" suffix.

Provides the SUM and CARRY functions while requiring only AUGEND (A) and ADDEND (B) inputs with CARRY IN.



TRUTH TABLE				
INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
A	B	C_i	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

POSITIVE LOGIC

$Co = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

$S = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}B\overline{C_i}$

$t_{pd} = 60$ ns typ

$P_D = 190$ mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR

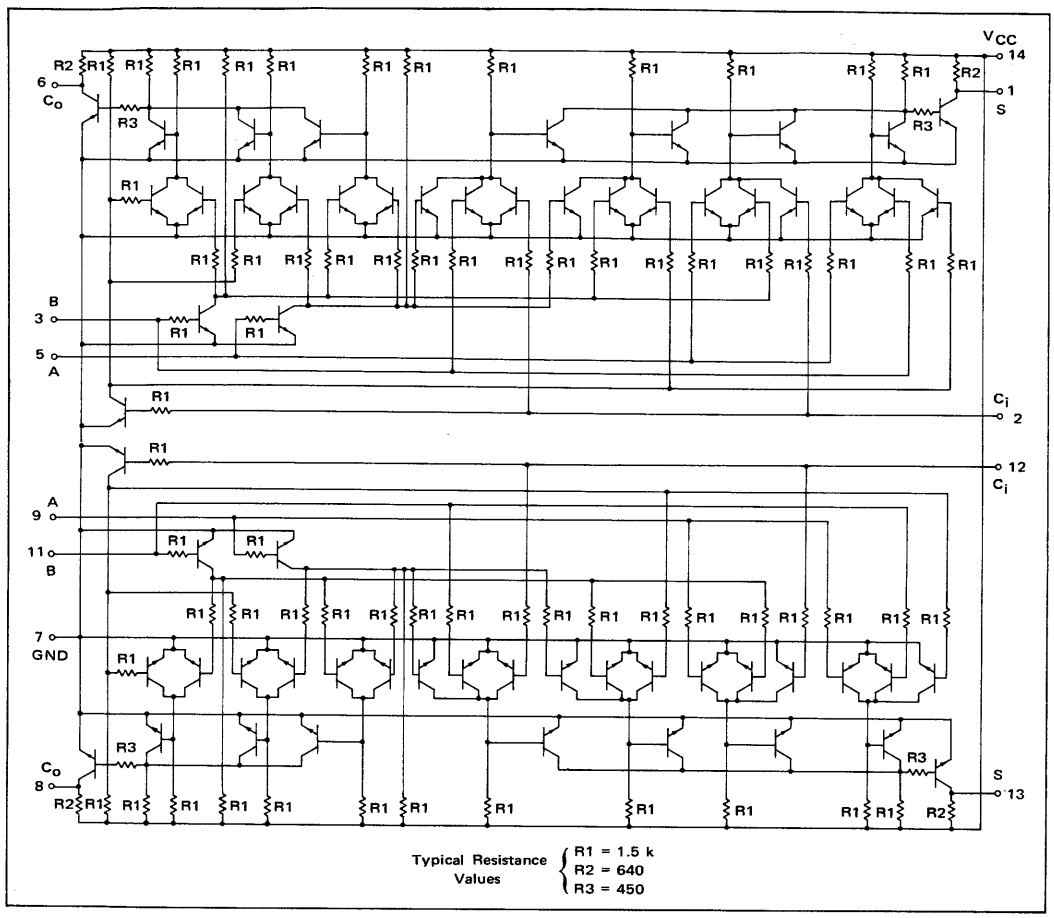
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one adder.
The other adder is tested in the same manner.

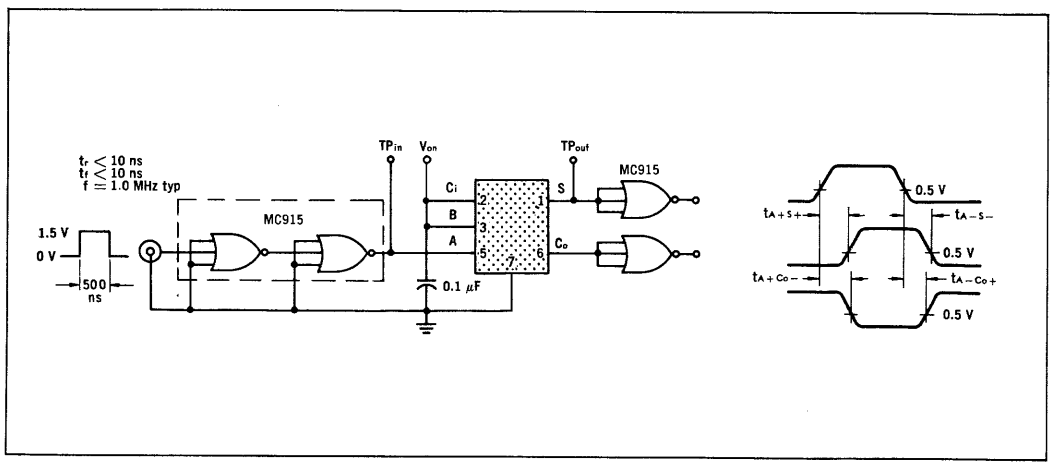
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC996	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC896	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC996 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC896 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$3I_{in}$	2	-	1485	-	1305	-	1410	μAdc	-	1512	-	1350	-	1350	μAdc	2	-	-	-	14	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	-	-	↓	↓
		5	-		-		-			-		-		-			5	-	-	-		
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1,2	-	3,5	14	7
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	1,3	-	2,5	↓	↓
				-		-		-			-		-		-		-	1,5	-	2,3		
				-		-		-			-		-		-		-	1,2,3,5	-	-		
		6		-		-		-			-		-		-		-	2,3,6	-	5		
		↓		-		-		-			-		-		-		-	2,5,6	-	3		
				-		-		-			-		-		-		-	3,5,6	-	2		
				-		-		-			-		-		-		-	2,3,5,6	-	-		
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	-	-	2,3,5	14	7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2,3	-	5	↓	↓
			-		-		-			-		-		-			-	3,5	-	2		
			-		-		-			-		-		-			-	2,5	-	3		
		6	-		-		-			-		-		-			-	-	-	2,3,5		
		↓	-		-		-			-		-		-			-	2	-	3,5		
			-		-		-			-		-		-			-	3	-	2,5		
			-		-		-			-		-		-			-	5	-	2,3		
																	Pulse In		Pulse Out			
Switching Time	t	5+1+	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	5	2,3	1	-	14	7
		5-1-	-	-	-	75	-	-		-	-	-	75	-	-		↓	2,3	1	-	↓	↓
		5+6+	-	-	-	85	-	-		-	-	-	85	-	-			2	6	3		
		5-6-	-	-	-	65	-	-		-	-	-	65	-	-			2	6	3		
		3+1+	-	-	-	75	-	-		-	-	-	75	-	-		3	-	1	2,5		
		3-1-	-	-	-	75	-	-		-	-	-	75	-	-		↓	-	1	2,5		
		3+6+	-	-	-	85	-	-		-	-	-	85	-	-			2	6	5		
		3-6-	-	-	-	65	-	-		-	-	-	65	-	-			2	6	↓		
		2+1-	-	-	-	70	-	-		-	-	-	70	-	-		2	3	1			
		2-1+	-	-	-	80	-	-		-	-	-	80	-	-		↓	↓	1			
		2+6+	-	-	-	70	-	-		-	-	-	70	-	-				6			
		2-6-	-	-	-	80	-	-		-	-	-	80	-	-				6			

Ground input pins of adder not under test.
Other pins not listed are left open.



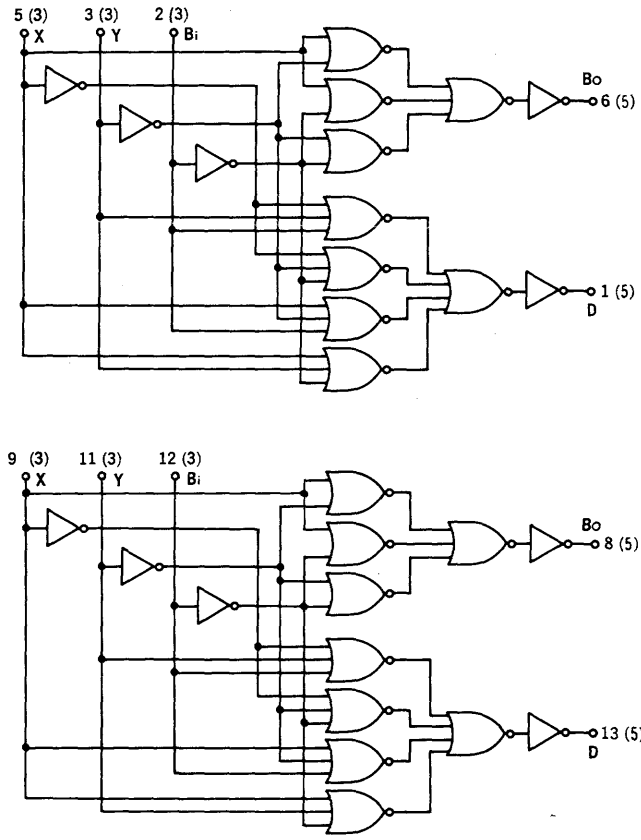
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



MC997 • MC897

Available in TO-86 flat package, add "F" suffix.

Provides the DIFFERENCE and BORROW functions while requiring only MINUEND (X) and SUBTRAHEND (Y) inputs with BORROW IN.



TRUTH TABLE				
INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

POSITIVE LOGIC

$D = YXB_i + Y\bar{X}\bar{B}_i + \bar{Y}X\bar{B}_i + \bar{Y}\bar{X}B_i$

$B_o = \bar{Y}\bar{X}B_i + Y\bar{X}\bar{B}_i + Y\bar{X}B_i + YXB_i$

$t_{pd} = 60$ ns typ

$P_D = 190$ mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR

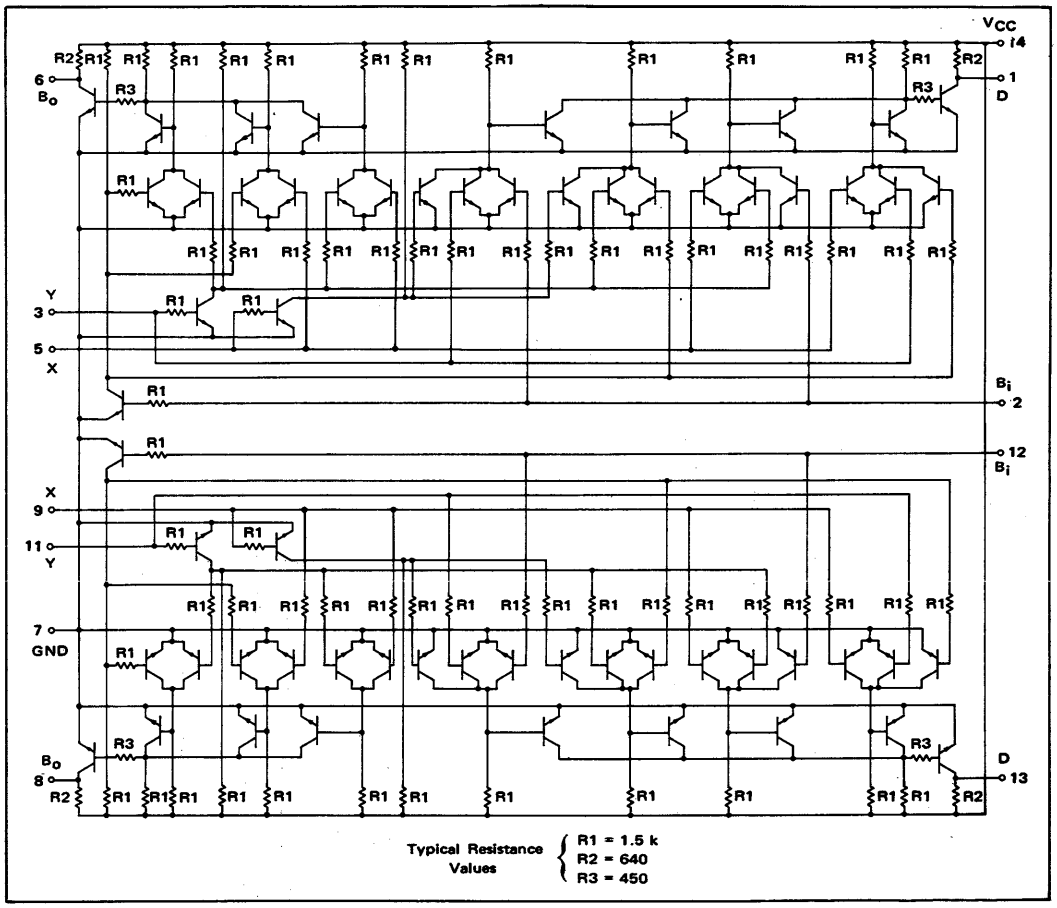
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one subtractor.
The other subtractor is tested in the same manner.

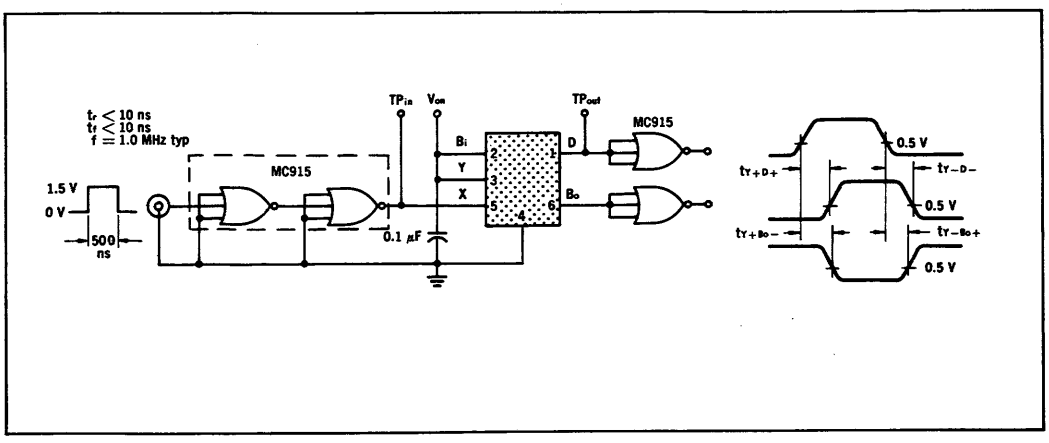
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC997	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC897	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC997 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC897 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$3\,I_{in}$	2	-	1485	-	1305	-	1410	μAdc	-	1512	-	1350	-	1350	μAdc	2	-	-	-	14	7
		3	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	3	-	-	-	↓	↓
		5	-		-		-			-		-		-			5	-	-	-		
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1, 2	-	3, 5	14	7
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	1, 3	-	2, 5	↓	↓
				-		-		-			-		-		-		-	1, 5	-	2, 3		
				-		-		-			-		-		-		-	1, 2, 3, 5	-	-		
		6		-		-		-			-		-		-		-	2, 3, 5, 6	-	-		
		↓		-		-		-			-		-		-		-	2, 6	-	3, 5		
				-		-		-			-		-		-		-	3, 6	-	2, 5		
				-		-		-			-		-		-		-	2, 3, 6	-	5		
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	-	-	2, 3, 5	7	14
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2, 3	-	5	↓	↓
			-		-		-			-		-		-			-	3, 5	-	2		
			-		-		-			-		-		-			-	2, 5	-	3		
		6	-		-		-			-		-		-			-	2, 5	-	3		
		↓	-		-		-			-		-		-			-	3, 5	-	2		
			-		-		-			-		-		-			-	-	-	2, 3, 5		
			-		-		-			-		-		-			-	5	-	2, 3		
Switching Time																	Pulse In		Pulse Out			
	t	5+1+	-	-	-	60	-	-	ns	-	-	-	60	-	-	ns	5	2, 3	1	-	14	7
		5-1-	-	-	-	60	-	-		-	-	-	60	-	-		↓	↓	1	-	↓	↓
		5+6+	-	-	-	65	-	-		-	-	-	65	-	-				6	-		
		5-6-	-	-	-	60	-	-		-	-	-	60	-	-				6	-		
		3+1+	-	-	-	↓	-	-		-	-	-	↓	-	-		3	-	1	2, 5		
		3-1-	-	-	-		-	-		-	-	-		-	-		↓	-	1	2, 5		
		3+6-	-	-	-	65	-	-		-	-	-	65	-	-			2	6	5		
		3-6+	-	-	-	60	-	-		-	-	-	60	-	-			2	6	↓		
		2+1-	-	-	-	↓	-	-		-	-	-	↓	-	-		2	3	1			
		2-1+	-	-	-		-	-		-	-	-		-	-		↓	3	1	↓		
		2+6+	-	-	-		-	-		-	-	-		-	-			3, 5	6	-		
		2-6-	-	-	-	↓	-	-		-	-	-	↓	-	-			3, 5	6	-	↓	↓

Ground input pins of subtractor not under test.
Other pins not listed are left open.



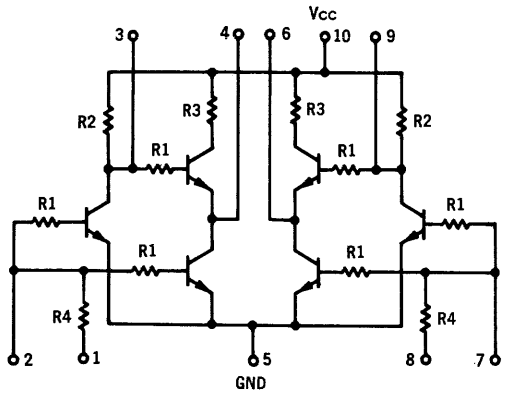
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



MC999 • MC899

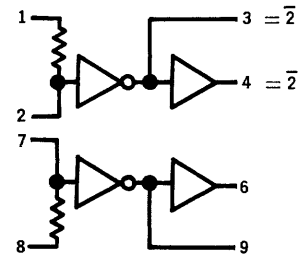
Available in TO-100 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

The dual buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input, the differentiation of input waveforms and various multivibrator applications.



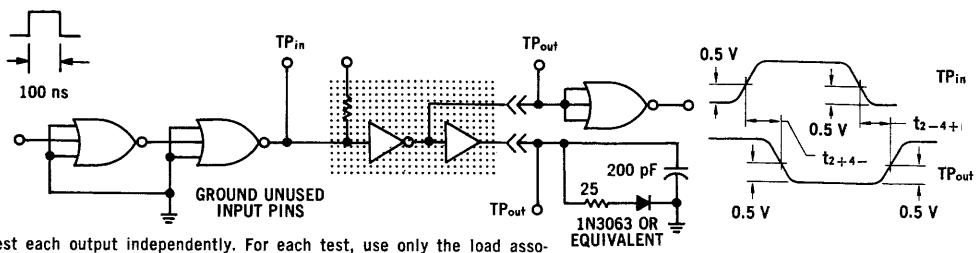
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω
R4 = 1.0 kΩ

"F" PACKAGE AND "G" PACKAGE PIN-OUTS ARE THE SAME



Outputs 3 and 4 may not be used simultaneously
Outputs 9 and 6 may not be used simultaneously

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test. Output not under test should be left open.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC999	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC899	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC999 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC899 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Grd
Input Current	$2\ I_{in}$	2	-	990	-	870	-	940	μAdc	-	1010	-	900	-	900	μAdc	2	-	-	-	10	-	5
Output Current	I_{A5}	3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	3	-	2	10	-	5
	I_{AB}	4	12.4	-	12.7	-	11.8	-	mAdc	12.6	-	11.9	-	11.25	-	mAdc	-	4	-	2	10	-	5
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	10	-	5
		4	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	10	4	5
Saturation Voltage	$V_{CE(sat)}$	3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	10	-	5
		3	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	-	-	1, 10	-	↓
		4	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	2	-	10	4	↓
Switching Time	t	2+3-	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	Pulse In: 2	Pulse Out: 3	-	-	10	-	5
		2-3+	-	-	-	32	-	-		-	-	-	32	-	-		↓	3	-	-	↓	-	↓
		2+4-	-	-	-	30	-	-		-	-	-	30	-	-			4	-	-		-	
		2-4+	-	-	-	45	-	-		-	-	-	45	-	-		↓	4	-	-	↓	-	↓

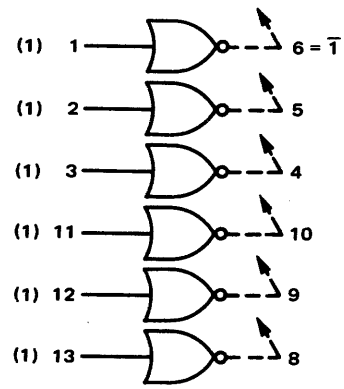
Ground inputs of buffer not under test. Other pins not listed are left open.

* Resistor value to V_{CC}

MC9919 • MC9819

Available in TO-86 flat package, add "F" suffix.

Six individual expanders are contained in a single package providing increased input capability for MRTL gates.

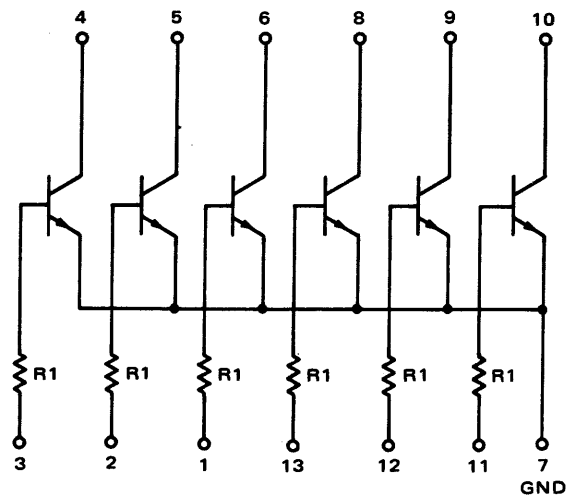


t_{pd} = 12 ns

P_D = 13 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.

When an expander is added to a gate, subtract 0.4 load from the output of the gate for each expander circuit added. The input loading factor of the expanded gate is 1.3. Pin 14 of the expander must be connected to V_{CC}.



V_{CC} connection to pin 14 not shown.

Typical Resistance Values
R1 = 450Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC9919 −55°C	1.014	1.014	1.50	0.710	3.00	680
MC9919 +25°C	0.844	0.815	1.50	0.565	3.00	680
MC9919 +125°C	0.674	0.674	1.50	0.320	3.00	680
MC9819 0°C	0.909	0.909	1.50	0.574	3.00	680
MC9819 +25°C	0.844	0.844	1.50	0.554	3.00	680
MC9819 +100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC9919 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC9819 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	-	-	14	6	7
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	6	-	-	1	14	-	7
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	6	7
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	6	7

Ground inputs of expanders not used in test. Other pins not listed are left open.

* Resistor value to V_{CC}.