PLASTIC

MRTL

INTEGRATED CIRCUITS

LOW-POWER
AND
MEDIUM-POWER

MC700P/MC800P SERIES

MILLIWATT AND MEDIUM-POWER

PLASTIC MRTL

INTEGRATED CIRCUITS

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MC718P, MC818P	Dual 3-Input Gates	mW MRTL
MC719P, MC819P	Dual 4-Input Gates	mW MRTL
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MC786P, MC886P	Dual 4-Input Expanders	MRTL
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MC792P, MC892P	Triple 3-Input Gates	MRTL
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MC9722P, MC9822P	Dual J-K Flip-Flop	mW MRTL
MC9760P, MC9860P	BCD-to-Decimal Decoder Driver	MRTL

FUNCTIONS AND CHARACTERISTICS
MRTL

V_{CC} = 3.6 V ± 10%, T_A = 25°C

Function	Type +15 to +55°C	Type 0 to +75°C	Case	Output Loading Factor Each Output mW MRTL	Output Loading Factor Each Output MRTL	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg
GATES							
Dual 3-Input Gates	MC715P	MC815P	605	16	5	12	55/15 ②
Quad 2-Input Gates	MC724P	MC824P	605	16	5	12	100/30 ②
Dual 4-Input Gates	MC725P	MC825P	605	16	5	12	60/15 ②
Quad Exclusive OR Gates	MC771P	MC871P	605	16	5	12	87
Triple 3-Input Gates	MC792P	MC892P	605	16	5	12	82/24 ②
Quad 2-Input AND Gate	MC9713P	MC9813P	605	16	5	28	100
Quad 2-Input NAND Gate	MC9714P	MC9814P	605	16	5	14 ⑤	145
Quad 2-Input OR Gate	MC9715P	MC9815P	605	16	5	14 ⑤	28/100 ②
BUFFERS							
Dual Buffers, Non-Inverting	MC788P	MC888P	605	80	25	24	145/56 ②
Dual Buffers, Inverting	MC799P	MC899P	605	80	25	20	50/100 ②
FLIP-FLOPS							
J-K Flip-Flops	–	MC816P	605	–	3	35	91/79 ③
J-K Flip-Flops	MC723P	–	605	10	–	35	91/79 ③
J-K Flip-Flops	MC726P	MC826P	605	16	5	35	100/86 ③
Dual J-K Flip-Flops	MC790P	MC890P	605	10	3	35	182/158 ③
Dual J-K Flip-Flops	MC791P	MC891P	605	16	5	40	190/160 ③
INVERTER							
Hex Inverters	MC789P	MC899P	605	16	5	12	130/15 ②
EXPANDERS							
Quad 2-Input Expanders	MC785P	MC885P	605	–	–	12	20/– ②
Dual 4-Input Expanders	MC786P	MC886P	605	–	–	12	20/– ②
Hex Expanders	MC9719P	MC9819P	605	–	–	12	13/– ②
MULTI-FUNCTION DEVICES							
1 J-K Flip-Flop, 1 Expander, 2 Buffers	MC779P	MC879P	605	–	–	–	141/124 ④
1 J-K Flip-Flop, 1 Inverter, 2 Buffers	MC787P	MC887P	605	–	–	–	138/132 ④
ADDERS AND SUBTRACTORS							
Dual Half-Adders	MC775P	MC875P	605	16	5	20	120
Dual Full Adders	MC796P	MC896P	605	16	5	60	225
Dual Full Subtractors	MC797P	MC897P	605	16	5	60	225
4-Bit Parallel Full Adder	MC9704P	MC9804P	612	6	2	125	265
SHIFT REGISTERS							
Dual Half-Shift Registers With Inverter	MC783P	MC883P	605	13	4	22	140
Dual Half-Shift Registers	MC784P	MC884P	605	13	4	22	100
Serial-Parallel Shift Register	MC794P	MC894P	605	16	5	55	225
COUNTERS							
Binary Up Counter	MC777P	MC877P	605	10	3	–	180
Decade Up Counter	MC780P	MC880P	605	10	3	–	250
DATA ROUTING FUNCTION							
Dual 4-Channel Data Selector	MC9701P	MC9801P	612	16	5	25	100
Dual 4-Channel Data Distributor	MC9707P	MC9807P	612	16	5	25	150
SCHMITT TRIGGER							
Quad Schmitt Trigger	MC9709P	MC9809P	605	16	5	30	95
DECODER/DRIVER							
BCD-to-Decimal Decoder Driver	MC9760P	MC9860P	612	–	–	–	115

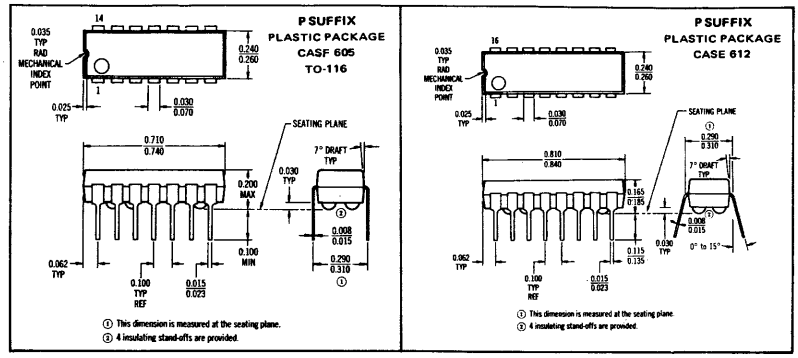
FUNCTIONS AND CHARACTERISTICS (continued)
mW MRTL

Function	Type +15 to +55°C	Type 0 to +75°C	Case	Output Loading Factor Each Output — Medium and Low Power	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg
GATES						
Quad 2-Input Gates	MC717P	MC817P	605	4	27	20/5.0 ②
Dual 3-Input Gates	MC718P	MC818P	605	4	27	12/2.5 ②
Dual 4-Input Gates	MC719P	MC819P	605	4	27	13/2.5 ②
Dual Exclusive OR-NOR Gate	MC764P	MC864P	605	3,4	35,65	25
Triple 3-Input Gates	MC793P	MC893P	605	4	27	18/3.5 ②
FLIP-FLOPS						
J-K Flip-Flops	MC722P	MC822P	605	4	70	24/20 ③
Quad Latch	MC767P	MC867P	612	9	50	110
Dual J-K Flip-Flops	MC776P	MC876P	605	2	50	41/29 ③
Dual Type D Flip-Flops	MC778P	MC878P	605	3	60	48/35 ①
Dual J-K Flip-Flop	MC9722P	MC9822P	605	4	75	24/– ③
BUFFER						
Dual Buffers	MC798P	MC898P	605	30	57	14/46 ②
INVERTERS						
Hex Inverter	MC9718P	MC9818P	605	4	27	7.0/3.0 ②
EXPANDERS						
Hex Expander	MC9720P	MC9820P	605	–	12	30/– ②
Quad 2-Input Expanders	MC9721P	MC9821P	605	–	27	20/– ②
DECODER						
BCD-to-Decimal Decoder	MC770P	MC870P	612	7	36	100/– ②

① Direct Set and Direct Clear Low, All other Inputs High/All Inputs Low.
② Inputs High/Inputs Low
③ Only Clock Inputs High/Inputs Low
④ Only Clock Input high on flip-flop, other element Inputs High/Inputs Low
⑤ Operating frequency (MHz)

PACKAGING

Plastic MRTL 14-lead devices are in Case 605 (TO–116); 16-lead devices are in Case 612.



MAXIMUM RATINGS $T_A = 25°C$

Rating	Symbol	Value	Unit
Input Voltage	—	±4.0	Vdc
Power Supply Voltage (Pulsed ≦ 1.0 s)	—	+12	Vdc
Operating Temperature Range MC700P Series MC800P Series	T_A	 +15 to +55 0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

TEST CONDITION TOLERANCES

$V_{BOT} = \pm 10$ mV $V_{CC} = \pm 10$ mV $V_{in} = \pm 2$ mV $V_R = \pm 1\%$ $V_{on} = \pm 2$ mV $V_{off} = \pm 2$ mV $V_{LL} = \pm 2$ mV

DEFINITIONS

I_{A2}, I_{A3}, I_{A4}, I_{A5}, I_{A10}, I_{A13}, I_{A16} — Minimum available output current from a device with an output loading factor of 2, 3, 4, 5, 10, 13, and 16 respectively. Output voltage not to fall below the value of V_{in}.

I_{AB} — Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.

I_{AM} — The maximum available current from the output of a Dual Gate.

I_{CEX} — Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

I_{in} — Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

$1.8\ I_{in}$ — Current drawn from the V_{in} supply by the Toggle pin of the Flip-Flop.

$2\ I_{in}$ — Maximum input current drawn by one input of a device with 2 bases internally tied together.

I_L — Isolation leakage current.

I_O — Output load current.

V_{BOT} — A high value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} — Supply voltage.

$V_{CE(sat)}$ — Maximum saturation voltage with V_{BOT} applied to the input.

V_{in} — Minimum high level voltage applied to the input of a device.

V_{LL} — A supply voltage low enough to allow flow of leakage currents only.

V_{off} — The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} — The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} — The maximum output voltage with V_{on} applied to the input.

V_R — Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

GENERAL RULES

- EXPANDER RULES:
  1. The MC785P/885P, MC786P/886P and MC9719P/9819P MRTL expanders can be used to expand medium-power MRTL output nodes only. The MC9721P/9821P expander can be used to expand mW MRTL output nodes only.
  2. mW MRTL and MC800 MRTL Series: When using the MC885P, MC886P, MC9819P or MC9721/9821 subtract 0.5 from the output loading factor of the expanded gate for each expander node that is connected; also increase the input loading factor of the expanded gate by a factor of 1.33.
  3. MC700 MRTL Series: When using the MC785P, MC786P or MC9719P subtract 2.0 from the output loading factor of the medium-power MRTL expanded gate for each expander node that is connected; also increase the input loading factor of the medium-power expanded gate by a factor of 3.75.
- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- When mixing MRTL and mWMRTL in the same system, the loading factors must be normalized in accordance with the input current of the units being driven.
- All unused inputs should be returned to ground.

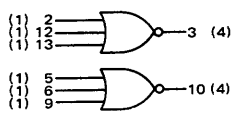
LOW-POWER mW MRTL DEVICES

The logic diagrams shown describe the MC700P/MC800P Series of low-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (if on the circuit input terminal) or load driving ability – fan-out – (if on the circuit output terminal).

Using the indicated loading factors, these low-power mW MRTL circuits are compatible with the medium-power MRTL circuits shown in this section. The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C for the MC700P Series, and 0 to +75°C for the MC800P Series, with V_{CC} = 3.6 V ±10%.

GATES

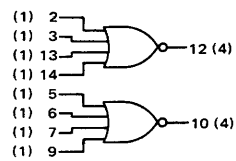
MC718P • MC818P
Dual 3-Input Gate



$3 = \overline{2 + 12 + 13}$

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5 mW (Inputs Low)

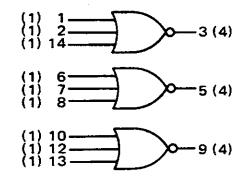
MC719P • MC819P
Dual 4-Input Gate



$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 27 ns
P_D = 13 mW (Input High)
2.5 mW (Inputs Low)

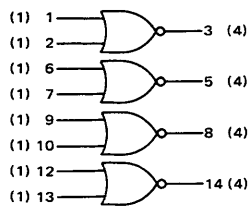
MC793P • MC893P
Triple 3-Input Gate



$3 = \overline{1 + 2 + 14}$

t_{pd} = 27 ns
P_D = 18 mW (Input High)
3.5 mW (Inputs Low)

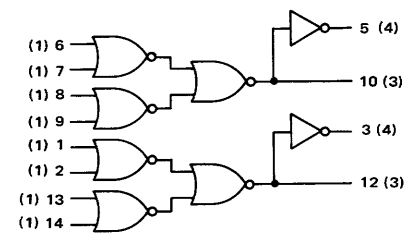
MC717P • MC817P
Quad 2-Input Gate



$3 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 20 mW (Input High)
5.0 mW (Inputs Low)

MC764P • MC864P
Dual Exclusive OR-NOR Gate

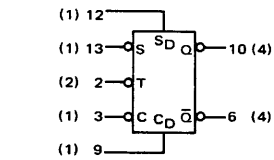


$12 = (1 + 2) \cdot (13 + 14)$
$3 = \overline{1} \cdot \overline{2} + \overline{13} \cdot \overline{14}$

t_{pd} = 65 ns (Pins 5 and 3)
t_{pd} = 35 ns (Pins 10 and 12)
P_D = 25 mW

FLIP-FLOPS

MC722P • MC822P
J-K Flip-Flop



f_{Tog} = 1 MHz
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

DIRECT INPUT OPERATION ①

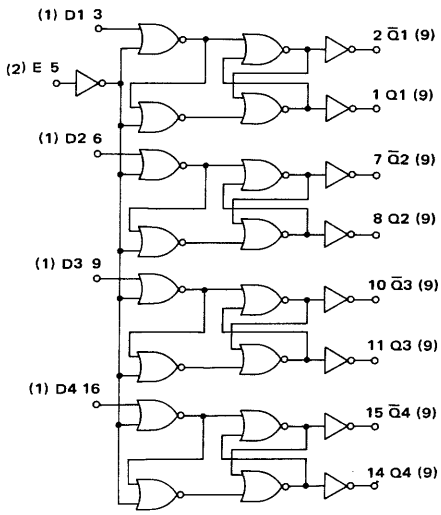
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n ④		t_{n+1} ④	
S	C	Q	$\bar{Q}$
1	1	Q_n ⑤	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.
6. Clock pulse fall time must be < 100 ns.

MC767P • MC867P
Quad Latch



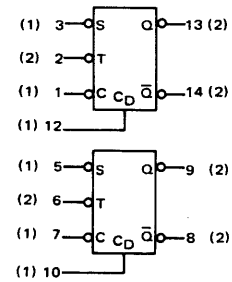
$t_{pd(avg)}$* = 50 ns typ
P_D = 110 mW typ

*Avg $t_{pd} = \frac{t_{on} + t_{off}}{2}$

TRUTH TABLE

E	D	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	Q_n	$\bar{Q}_n$
0	1	Q_n	$\bar{Q}_n$
1	0	0	1
1	1	1	0

MC776P • MC876P
Dual J-K Flip-Flop



f_{Tog} = 3 MHz
P_D = 41 mW (Only Clock Input High)
29 mW (Inputs Low)

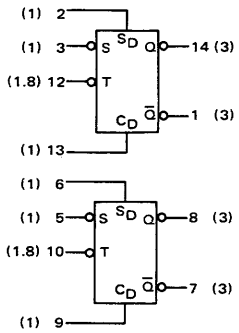
CLOCKED INPUT OPERATION

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

FLIP-FLOPS (continued)

MC778P • MC878P
Dual Type D Flip-Flop



f_{Tog} = 1 MHz

P_D = 48 mW (Direct Set (S_D) and Direct Clear (C_D) Low; all other Inputs High)
35 mW (All Inputs Low)

DIRECT INPUT OPERATION ①

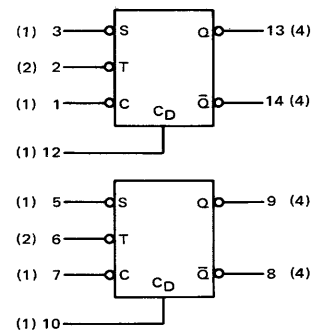
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n④		t_{n+1}④	
S		Q	$\bar{Q}$
1	1	1	0
0	0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

MC9722P • MC9822P
Dual J-K Flip-Flop



CLOCKED INPUT OPERATION ①

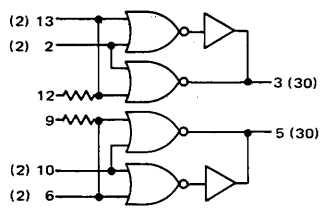
t_n②		t_{n+1} ②	
S	C	Q	$\bar{Q}$
1	1	Q_n ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ③

f_{Tog} = 4.0 MHz
t_{pd} = 75 ns typ
P_D = 24 mW typ (Only Clock Input High)

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

BUFFER

MC798P • MC898P
Dual 2-Input Buffer

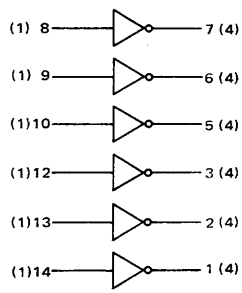


$3 = \overline{2 + 13}$

t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 mW (Inputs Low)

INVERTER

MC9718P • MC9818P
Hex Inverter

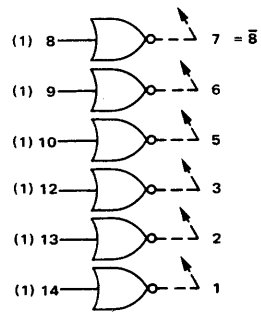


$7 = \bar{8}$

t_{pd} = 27 ns
P_D = 7.0 mW (Input High)
3.0 mW (Input Low)

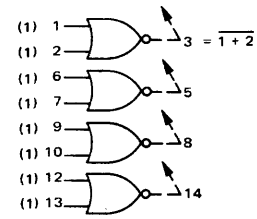
EXPANDERS

MC9720P • MC9820P
Hex Expander



t_{pd} = 12 ns
P_D = 30 mW (Inputs High)
Negligible (Inputs Low)

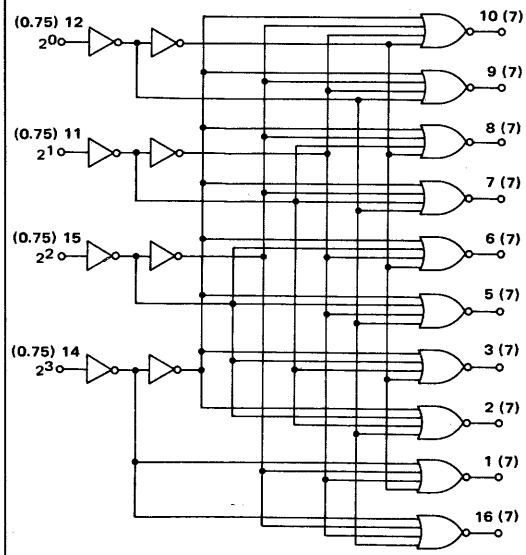
MC9721P • MC9821P
Quad 2-Input Expander



t_{pd} = 27 ns
P_D = 20 mW typ (Input High)
Negligible (Inputs Low)

DECODER

MC770P • MC870P
BCD-to-Decimal Decoder



TRUTH TABLE

INPUT (BCD)				OUTPUT (DECIMAL)									
2^3	2^2	2^1	2^0	0	1	2	3	4	5	6	7	8	9
14	15	11	12	10	9	8	7	6	5	3	2	1	16
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

t_{pd} = 36 ns
P_D = 100 mW typ (All inputs high)

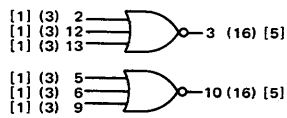
MEDIUM-POWER MRTL DEVICES

The logic diagrams shown describe the MC700P/MC800P Series of medium-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis or brackets indicates the input loading factor (if on the circuit input terminal) or load driving ability – fan-out – (if on the circuit output terminal). The bracketed number is the loading factor when working with other medium-power devices; e.g., [1] is the MRTL load factor defined as 1 times the MRTL basic gate input current (600 μAdc @ +25°C). The number in parenthesis is the loading factor when working with mW MRTL devices; e.g., (3) is the MRTL load factor defined as 3 times the mW MRTL basic gate input current (140 μAdc @ +25°C).

Using the parenthetic loading factors, these medium-power MRTL circuits are compatible with the low-power mW MRTL circuits shown in this section. The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C for the MC700P Series, and 0 to +75°C for the MC800P Series, with V_{CC} = 3.6 V ±10%.

GATES

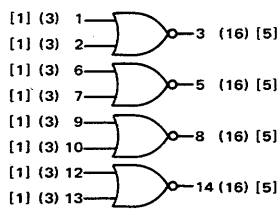
MC715P • MC815P
Dual 3-Input Gate



$3 = \overline{2 + 12 + 13}$

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

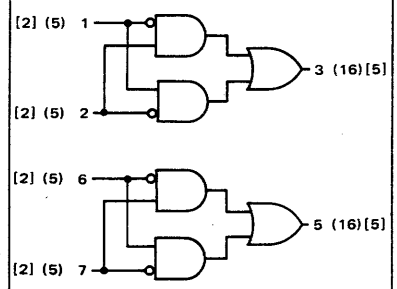
MC724P • MC824P
Quad 2-Input Gate

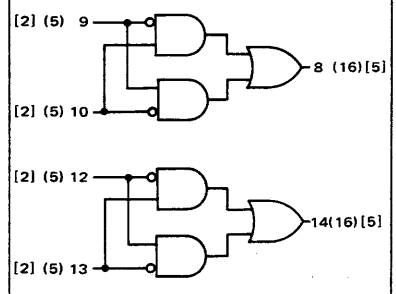


$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 100 mW (Input High)
30 mW (Inputs Low)

MC771P • MC871P
Quad Exclusive "OR" Gate

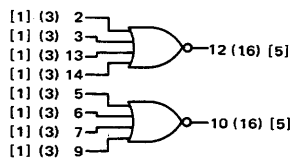




$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns
P_D = 87 mW

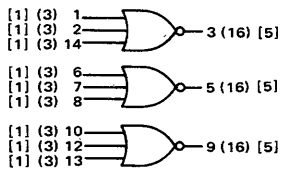
MC725P • MC825P
Dual 4-Input Gate



$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 12 ns
P_D = 60 mW (Input High)
15 mW (Inputs Low)

MC792P • MC892P
Triple 3-Input Gate

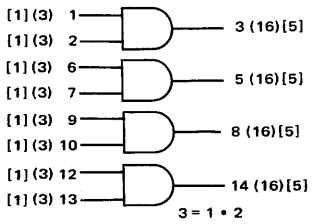


$3 = \overline{1 + 2 + 14}$

t_{pd} = 12 ns
P_D = 82 mW (Input High)
24 mW (Inputs Low)

GATES (continued)

MC9713P • MC9813P
Quad 2-Input AND Gate



$3 = 1 \cdot 2$

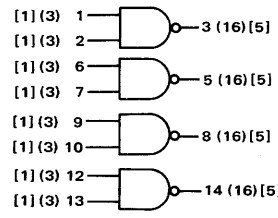
$A_{vg}\ t_{pd}^{*} = 28$ ns typ

$P_D = 100$ mW typ

Operating f = 14 MHz typ

$^{*}A_{yg}\ t_{pd} = \frac{t_{on} + t_{off}}{2}$

MC9714P • MC9814P
Quad 2-Input NAND Gate

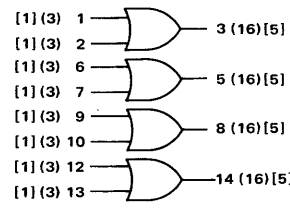


$3 = \overline{1 \cdot 2}$

$P_D = 145$ mW typ

Operating f = 14 MHz typ

MC9715P • MC9815P
Quad 2-Input OR Gate



$3 = 1 + 2$

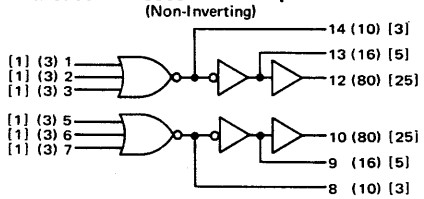
$P_D = 100$ mW typ (Inputs Low)

= 28 mW typ (Inputs High)

Operating f = 14 MHz typ

BUFFERS

MC788P • MC888P Dual 3-Input Buffer
(Non-Inverting)



t_{pd} = 24 ns

P_D = 145 mW (Input High)

56 mW (Inputs Low)

$14 = \overline{1 + 2 + 3}$

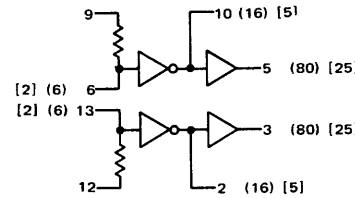
$13 = 1 + 2 + 3$

$12 = 1 + 2 + 3$

Outputs 12, 13, or 14 may not be used simultaneously.

Outputs 8, 9, or 10 may not be used simultaneously.

MC799P • MC899P Dual Buffer



t_{pd} = 20 ns

P_D = 50 mW (Input High)

100 mW (Inputs Low)

$10 = \overline{6}$

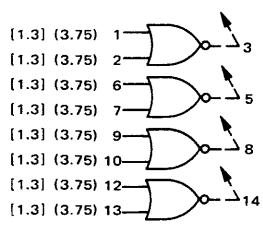
$5 = \overline{6}$

Outputs 2 and 3 may not be used simultaneously.

Outputs 5 and 10 may not be used simultaneously.

EXPANDERS

MC785P • MC885P
Quad 2-Input Expander



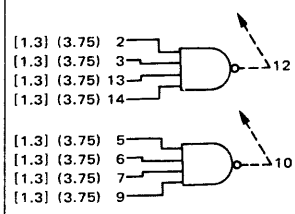
$3 = \overline{1 + 2}$

t_{pd} = 12 ns

P_D = 20 mW (Input High)

Negligible (Inputs Low)

MC786P • MC886P
Dual 4-Input Expander



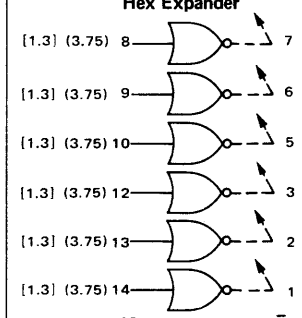
$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 12 ns

P_D = 20 mW (Input High)

Negligible (Inputs Low)

MC9719P • MC9819P
Hex Expander



t_{pd} = 12 ns

P_D = 13 mW (Input High)

Negligible (Inputs Low)

$7 = \overline{8}$

FLIP-FLOPS

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ①

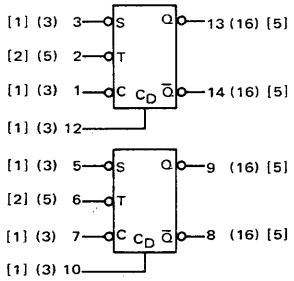
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1} ④	
S	C	Q	$\overline{Q}$
1	1	Q_n⑤	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

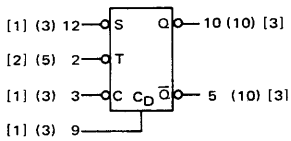
1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.
6. Clock pulse fall time must be < 100 ns.

MC791P • MC891P
Dual J-K Flip-Flop



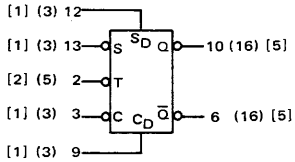
f_{Tog} = 4 MHz
P_D = 190 mW (Only Clock Input High)
160 mW (Inputs Low)

MC723P • MC816P
J-K Flip-Flop



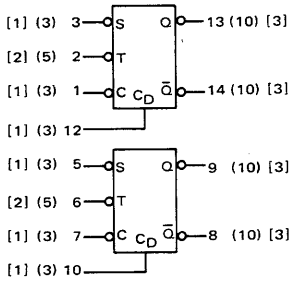
f_{Tog} = 4 MHz
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

MC726P • MC826P
J-K Flip-Flop



f_{Tog} = 4 MHz
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

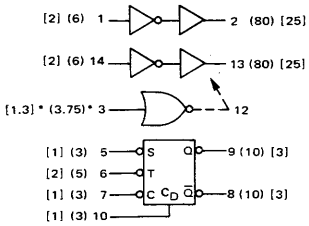
MC790P • MC890P
Dual J-K Flip-Flop



f_{Tog} = 4 MHz
P_D = 182 mW (Only Clock Input High)
158 mW (Inputs Low)

MULTIFUNCTION DEVICES

MC779P • MC879P
Multifunction
(1 J-K FLIP-FLOP, 1 EXPANDER, 2 BUFFERS)

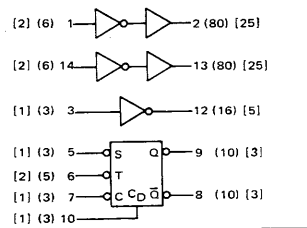


	f_{Tog} MHz	t_{pd} ns	P_D mW (Input High)	P_D mW (Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
EXPANDER	—	12	25	Negligible

‡Only Clock Input High

*Input loading factor is 3 for mW MRTL, or 1 for MRTL, if pin 12 is tied to pin 8 or 9 on the same package.

MC787P • MC887P
Multifunction
(1 J-K FLIP-FLOP, 1 INVERTER, 2 BUFFERS)

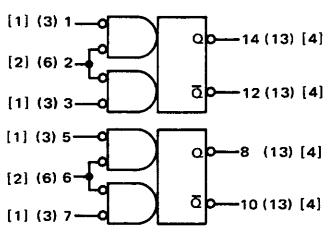


	f_{Tog} MHz	t_{pd} ns	P_D mW (Input High)	P_D mW (Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
INVERTER	—	12	22	8

‡Only Clock Input High

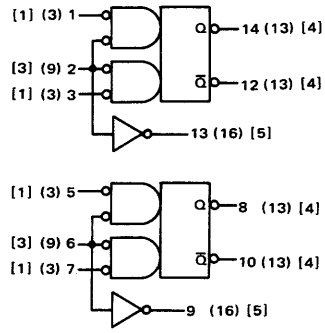
SHIFT REGISTERS

MC784P • MC884P
Dual Half-Shift Register
(Without Inverter)



$14 = \overline{12}\ (1 + 2)$
$12 = \overline{14}\ (3 + 2)$
t_{pd} = 22 ns
P_D = 100 mW

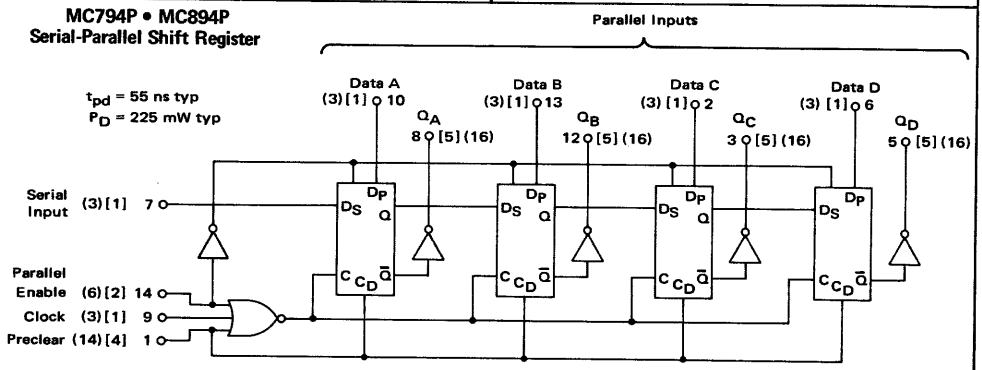
MC783P • MC883P
Half-Shift Register



$14 = \overline{12}\ (1 + 2)$
$12 = \overline{14}\ (3 + 2)$
t_{pd} = 22 ns
P_D = 140 mW

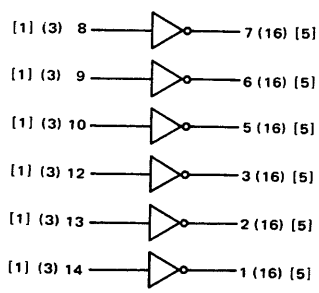
MC794P • MC894P
Serial-Parallel Shift Register

t_{pd} = 55 ns typ
P_D = 225 mW typ



INVERTER

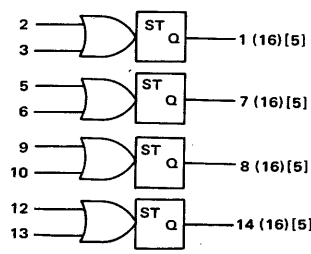
MC789P • MC889P
Hex Inverter



t_{pd} = 12 ns
P_D = 130 mW (Input High)
15 mW (Inputs Low)
$1 = \overline{14}$

SCHMITT TRIGGER

MC9709P • MC9809P
Quad Schmitt Trigger

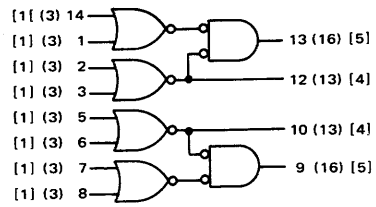


$t_r = t_f$ = 20 ns typ
Avg. t_{pd} = 30 ns typ, Avg. = $\frac{t_{on} + t_{off}}{2}$
f = 18 MHz typ
P_D = 95 mW typ

Upper Trigger Voltage = 1.40 V typ
Lower Trigger Voltage = 0.75 V typ

HALF ADDER

MC775P • MC875P
Dual Half Adder



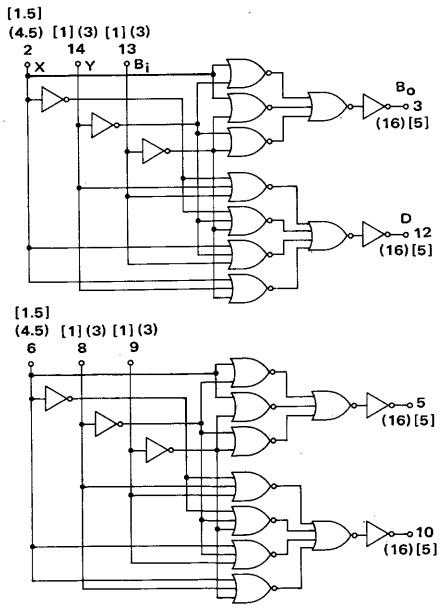
$13 = (14 + 1)(2 + 3)$

$12 = \overline{2 + 3}$

t_{pd} = 20 ns
P_D = 120 mW typ

FULL SUBTRACTOR

MC797P • MC897P
Dual Full Subtractor



$D = YXB_i + \bar{Y}X\bar{B}_i + \bar{Y}\bar{X}B_i + \bar{Y}\bar{X}\bar{B}_i$

$B_o = \bar{Y}\bar{X}B_i + Y\bar{X}\bar{B}_i + Y\bar{X}B_i + YXB_i$

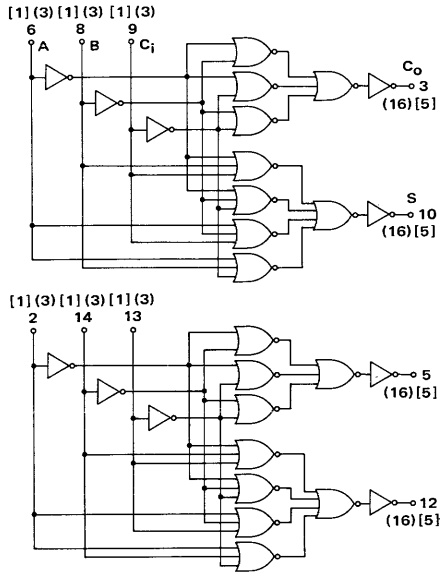
t_{pd} = 60 ns typ
P_D = 225 mW typ

TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

FULL ADDERS

MC796P • MC896P
Dual Full Adder



$C_o = ABC_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$

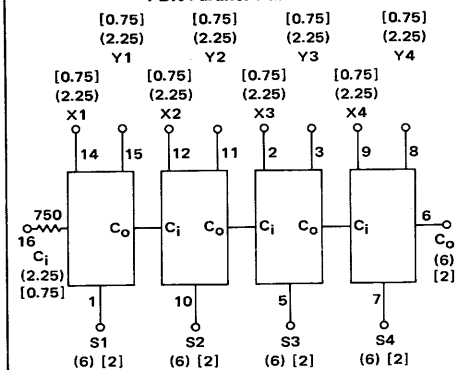
$S = ABC_i + A\bar{B}\bar{C}_i + \bar{A}\bar{B}C_i + \bar{A}B\bar{C}_i$

t_{pd} = 60 ns typ
P_D = 225 mW typ

TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

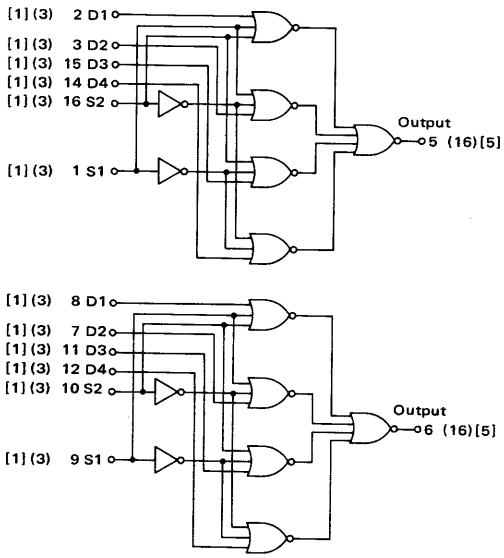
MC9704P • MC9804P
4-Bit Parallel Full Adder



C_o t_{pd} = 125 ns typ
P_D = 265 mW typ
Operating Frequency = 8.0 MHz

DATA ROUTING FUNCTIONS

MC9701P • MC9801P
Dual 4-Channel Data Selector



TRUTH TABLE

Input Select		Data Line
S1	S2	Selected
0	0	D1
0	1	D2
1	0	D3
1	1	D4

$$\text{Output} = \overline{S1}\,\overline{S2}\,D1 + \overline{S1}\,S2\,D2 + S1\,\overline{S2}\,D3 + S1\,S2\,D4$$

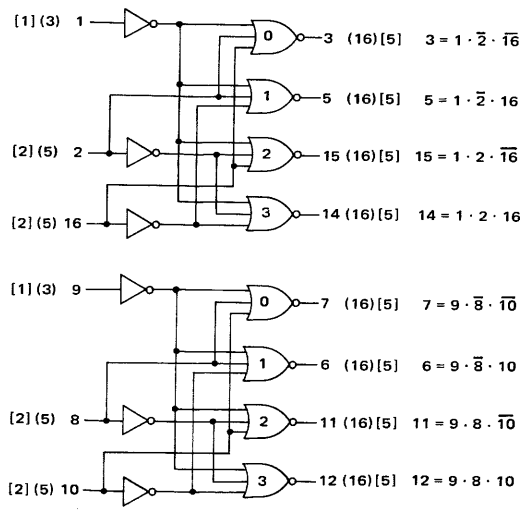
Avg. t_{pd} = 25 ns typ Avg. $t_{pd} = \frac{t_{+-} + t_{-+}}{2}$

P_D = 100 mW typ

Operating Frequency = 18 MHz typ

(Both Selector Inputs and Data Inputs High)

MC9707P • MC9807P
Dual 4-Channel Date Distributor



TRUTH TABLE

	INPUTS			OUTPUTS			
	D	S1	S2	0	1	2	3
Pin	1	2	16	3	5	15	14
Numbers	9	8	10	7	6	11	12
Level	0	*	*	0	0	0	0
	1	0	0	1	0	0	0
	1	0	1	0	1	0	0
	1	1	0	0	0	1	0
	1	1	1	0	0	0	1

*Either state.

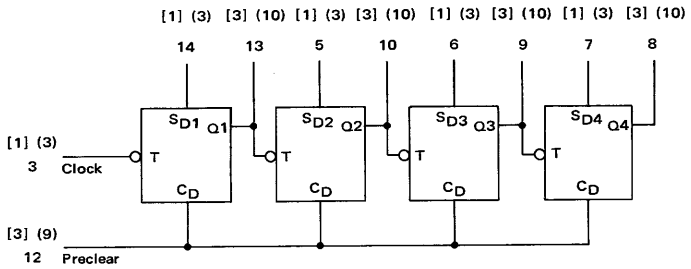
A_{vg}* t_{pd} = 25 ns typ

P_D = 150 mW typ

*A_{vg} $t_{pd} = \frac{t_{on} + t_{off}}{2}$

COUNTERS

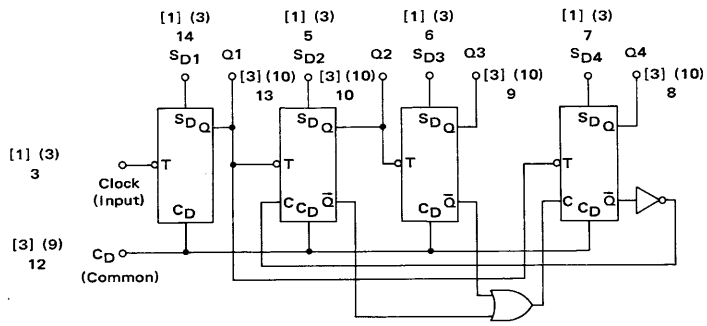
MC777P • MC877P
Binary Up Counter



f_{Tog} = 4.0 MHz
P_D = 180 mW typ

DECODING LOGIC	
0	$\bar{A}\,\bar{B}\,\bar{C}\,\bar{D}$
1	$A\,\bar{B}\,\bar{C}\,\bar{D}$
2	$\bar{A}\,B\,\bar{C}\,\bar{D}$
3	$A\,B\,\bar{C}\,\bar{D}$
4	$\bar{A}\,\bar{B}\,C\,\bar{D}$
5	$A\,\bar{B}\,C\,\bar{D}$
6	$\bar{A}\,B\,C\,\bar{D}$
7	$A\,B\,C\,\bar{D}$
8	$\bar{A}\,\bar{B}\,\bar{C}\,D$
9	$A\,\bar{B}\,\bar{C}\,D$
10	$\bar{A}\,B\,\bar{C}\,D$
11	$A\,B\,\bar{C}\,D$
12	$\bar{A}\,\bar{B}\,C\,D$
13	$A\,\bar{B}\,C\,D$
14	$\bar{A}\,B\,C\,D$
15	$A\,B\,C\,D$

MC780P • MC880P
Decade Up Counter



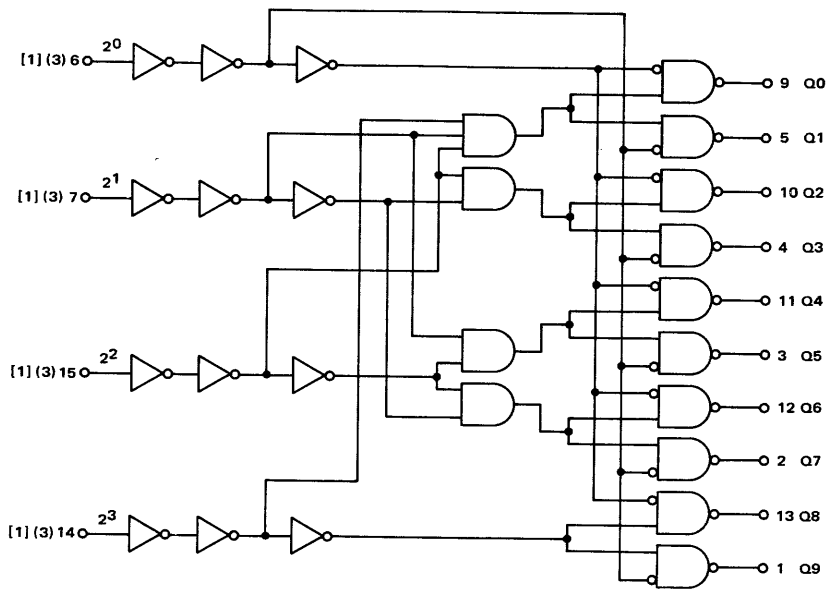
DECODING LOGIC

0	$\bar{A}$	$\bar{B}$	$\bar{C}$	$\bar{D}$
1	A	$\bar{B}$	$\bar{C}$	$\bar{D}$
2	$\bar{A}$	B	$\bar{C}$	$\bar{D}$
3	A	B	$\bar{C}$	$\bar{D}$
4	$\bar{A}$	$\bar{B}$	C	$\bar{D}$
5	A	$\bar{B}$	C	$\bar{D}$
6	$\bar{A}$	B	C	$\bar{D}$
7	A	B	C	$\bar{D}$
8	$\bar{A}$	$\bar{B}$	$\bar{C}$	D
9	A	$\bar{B}$	$\bar{C}$	D

P_D = 250 mW typ
f = 4.0 MHz
Counting Frequency

DECODER/DRIVER

MC9760P • MC9860P
BCD-to-Decimal Decoder/Driver



P_D = 115 mW typ

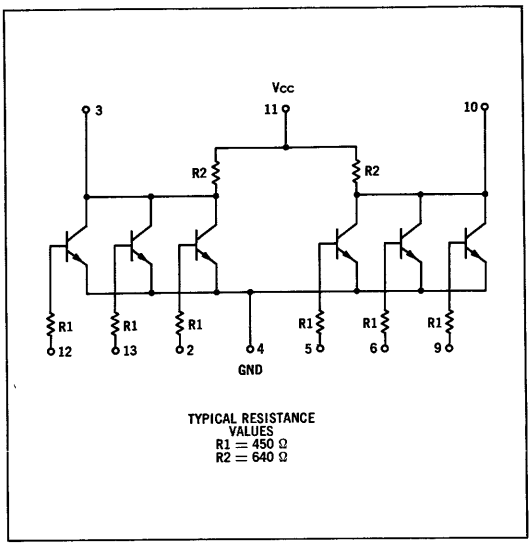
TRUTH TABLE

	INPUT* (BCD)				OUTPUT (DECIMAL)									
Value	2^0	2^1	2^2	2^3	0	1	2	3	4	5	6	7	8	9
Pin No.	6	7	15	14	9	5	10	4	11	3	12	2	13	1
Logic Levels	1	1	1	1	0	1	1	1	1	1	1	1	1	1
	0	1	1	1	1	0	1	1	1	1	1	1	1	1
	1	0	1	1	1	1	0	1	1	1	1	1	1	1
	0	0	1	1	1	1	1	0	1	1	1	1	1	1
	1	1	0	1	1	1	1	1	0	1	1	1	1	1
	0	1	0	1	1	1	1	1	1	0	1	1	1	1
	1	0	0	1	1	1	1	1	1	1	0	1	1	1
	0	0	0	1	1	1	1	1	1	1	1	0	1	1
	1	1	1	0	1	1	1	1	1	1	1	1	0	1
	0	1	1	0	1	1	1	1	1	1	1	1	1	0

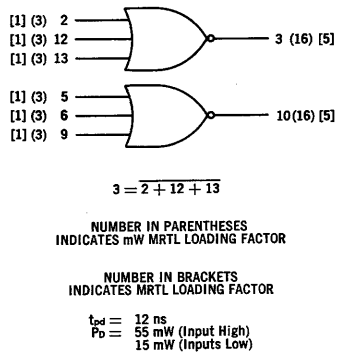
Logic "0" ≤ 1.5 Vdc @ 6.0 mA
Logic "1" ≥65 Vdc (MC9760)
Logic "1" ≥70 Vdc (MC9860)

*Any input configuration not shown results in an indeterminate state at the outputs.

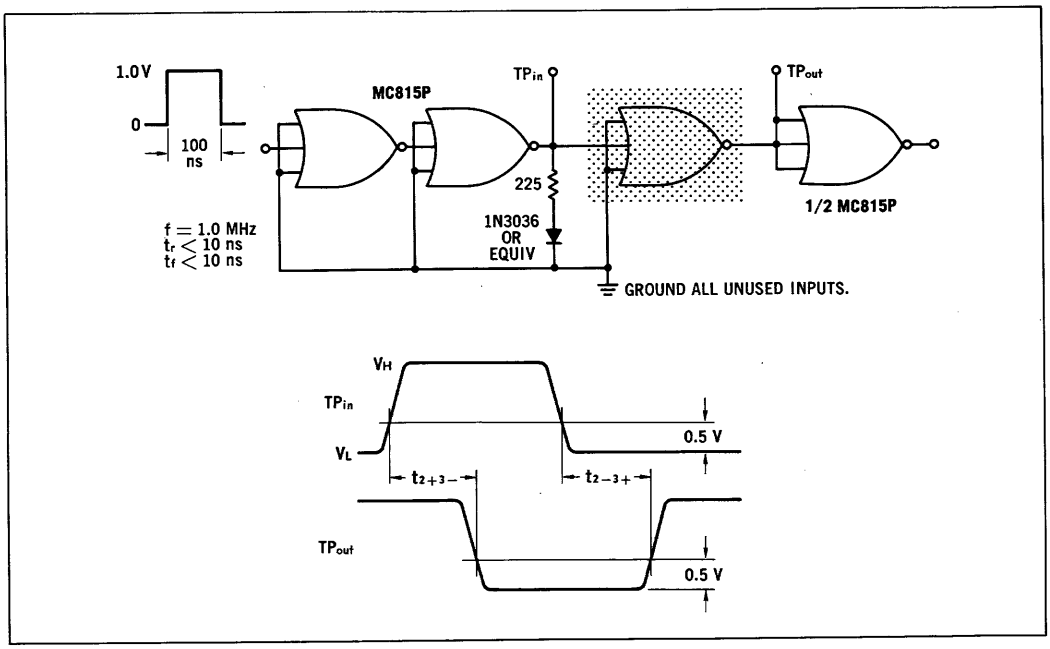
MC715P • MC815P



Two 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

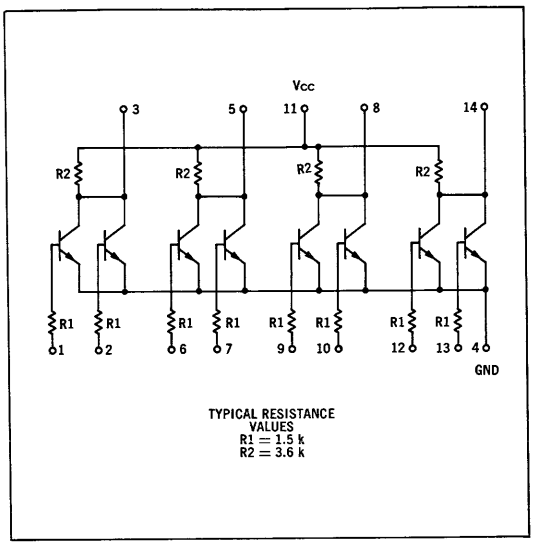
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC815P	0°C	0.960	0.930	1.80	0.570	3.60
MC815P	+25°C	0.910	0.880	1.80	0.500	3.60
MC815P	+75°C	0.820	0.790	1.80	0.450	3.60
MC715P	+15°C	0.865	0.865	1.80	0.475	3.60
MC715P	+25°C	0.850	0.850	1.80	0.460	3.60
MC715P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC815P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC715P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	12, 13	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	12	-	2, 13	-	↓	↓
		13	-		-		-			-		-		-			13	-	2, 12	-		
Output Current	I_{A5}	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	2,12,13	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	-	↓	2,4,12
		3	-		-		-			-		-		-			-	2	-	-		4,12,13
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	12	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	13	-	↓	2,4,12
		3	-		-		-			-		-		-			-	-	2	-		4,12,13
Switching Time	$t_{on} + t_{off}$	3, 13	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In 13	Pulse Out 3	-	-	11	2,4,12

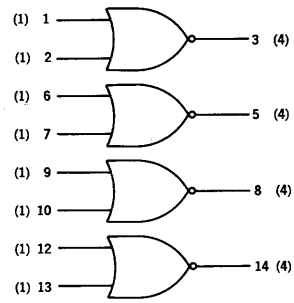
Ground input pins of gate not under test. Other pins not listed are left open.

MC717P • MC817P



TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k

Four 2-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.

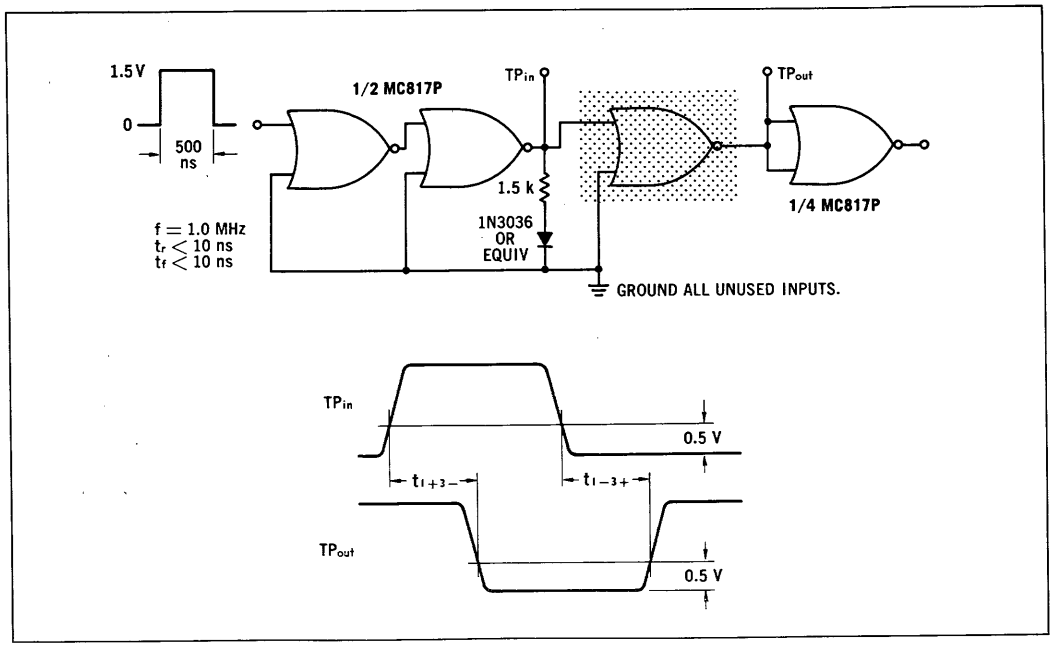


$3 = \overline{1 + 2}$

NUMBER IN PARENTHESES INDICATES LOADING FACTOR

t_{pd} = 27 ns
P_D = 20 mW (Input High)
5.0 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

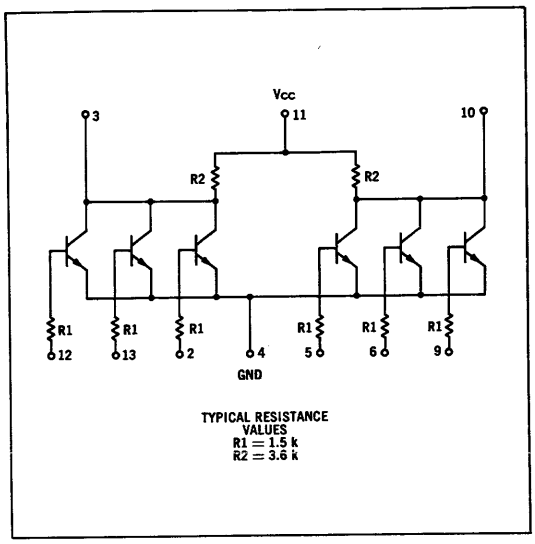
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC817P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC717P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC817P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC717P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	2	-	11	4
		2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	1	-	11	4
Output Current	I_{A4}	3	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	-	3	-	1,2	11	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2,4
		3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	1,4
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	1	-	11	2,4
		3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	-	11	1,4
Switching Time	$t_{on} + t_{off}$	1,3	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In: 1	Pulse Out: 3	-	-	11	2,4

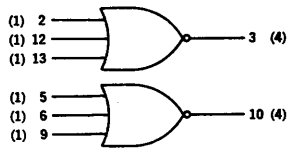
Ground input pins of gates not under test. Other pins not listed are left open.

MC718P • MC818P



TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k

Two 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

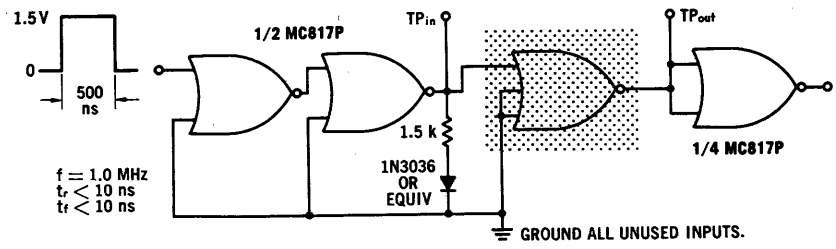


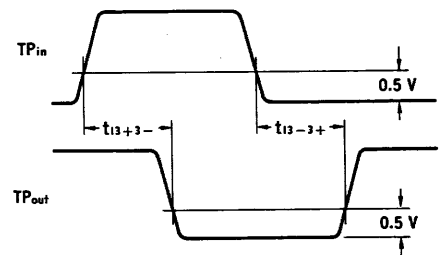
$3 = \overline{2 + 12 + 13}$

NUMBER IN PARENTHESES INDICATES LOADING FACTOR

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

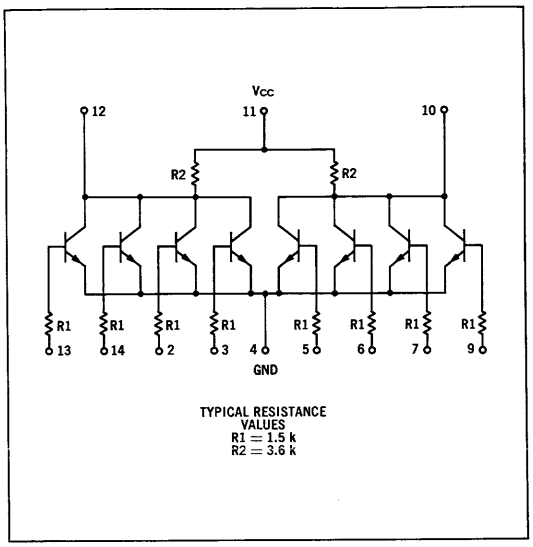
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC818P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC718P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC818P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC718P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	12, 13	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	12	-	2, 13	-	↓	↓
		13	-		-		-			-		-					13	-	2, 12	-		
Output Current	I_{A4}	3	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	3	-	-	2,12,13	11	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	-	↓	2,4,13
		3	-		-		-			-		-		-			-	2	-	-		4,12,13
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	12	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	13	-	↓	2,4,12
		3	-		-		-			-		-		-			-	-	2	-		4,12,13
Switching Time	$t_{on} + t_{off}$	3, 13	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 13	Pulse Out 3	-	-	11	2,4,12

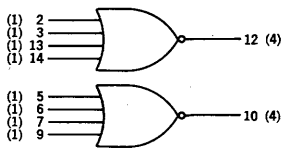
Ground unused input pins. Other pins not listed are left open.

MC719P • MC819P



TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k

Two 4-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

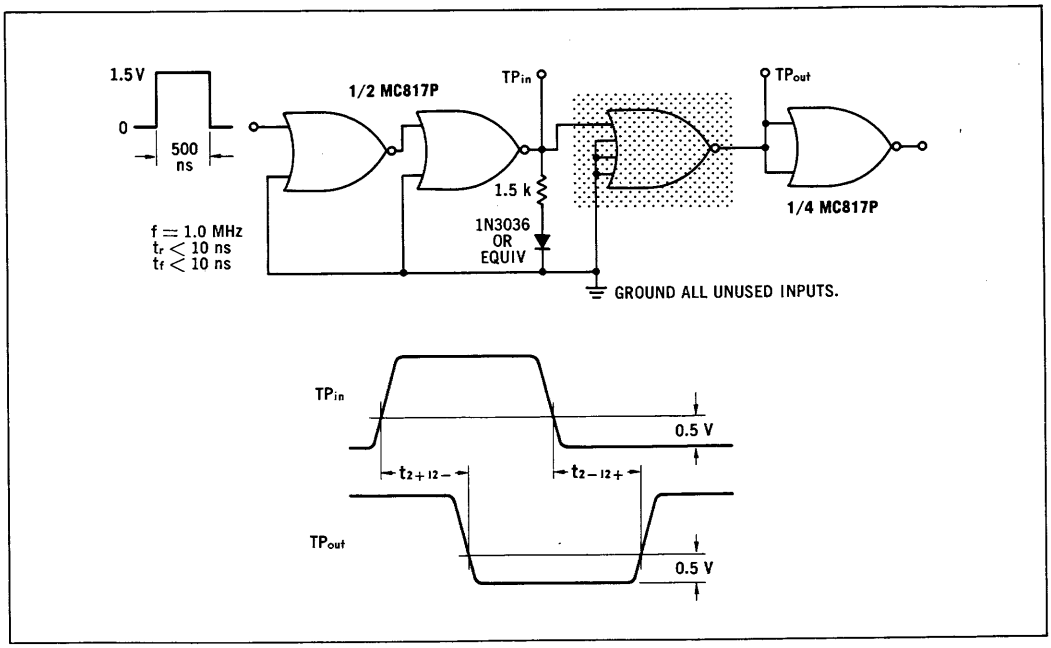


$12 = \overline{2 + 3 + 13 + 14}$

NUMBER IN PARENTHESES INDICATES LOADING FACTOR

t_{pd} = 27 ns
P_D = 13 mW (Input High)
2.5 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gate is tested in the same manner.

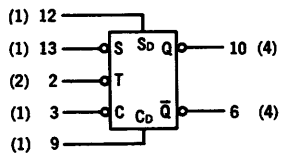
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC819P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC719P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC819P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC719P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	3,13,14	-	11	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,13,14	-	↓	↓
		13	-		-		-			-		-		-			13	-	2,3,14	-		
		14	-		-		-			-		-		-			14	-	2,3,13	-		
Output Current	I_{A4}	12	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	-	12	-	2,3,13, 14	11	4
Output Voltage	V_{out}	12	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	2	-	-		3,4,13,14
		12	-		-		-			-		-		-			-	3	-	-		2,4,13,14
Saturation Voltage	$V_{CE(sat)}$	12	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	13	-	11	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	-	2	-		3,4,13,14
		12	-		-		-			-		-		-			-		3	-		2,4,13,14
Switching Time	$t_{on} + t_{off}$	2, 12	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In: 2	Pulse Out: 12	-	-	11	3,4,13,14

Ground inputs of gate not under test. Other pins not listed are left open.

MC722P • MC822P

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



NUMBER IN PARENTHESES INDICATES LOADING FACTOR

f_{Tog} = 1.0 MHz
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\bar{Q}$
0	0	③	③
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The ouput state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.

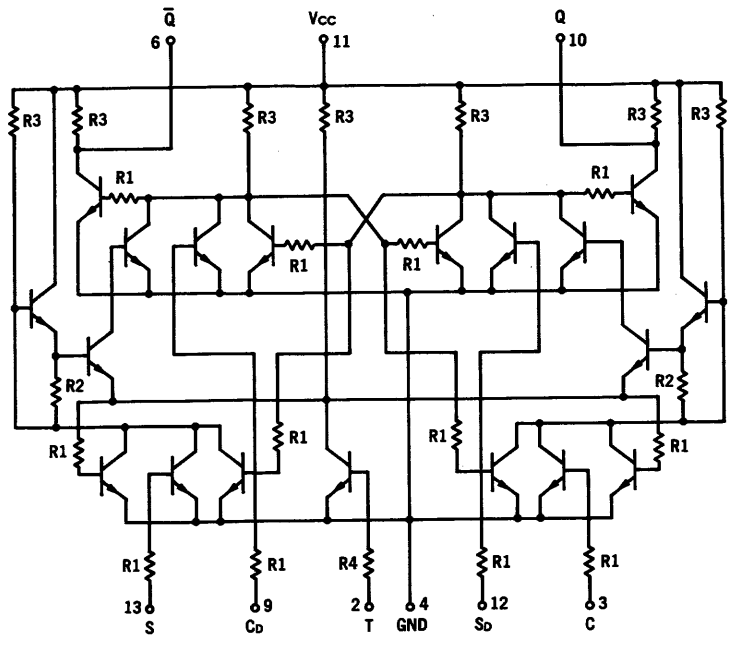
0 = low state

1 = high state

t_n = time period prior to negative transition of clock pulse

t_{n+1} = time period subsequent to negative transition of clock pulse

Q_n = state of Q output in time period t_n



TYPICAL RESISTANCE VALUES
R1 = 1.5 k R3 = 3.6 k
R2 = 2.0 k R4 = 750 Ω

ELECTRICAL CHARACTERISTICS

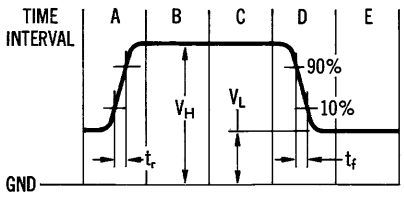
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC822P	0°C	0.880	0.850	1.80	0.500	3.60
MC822P	+25°C	0.830	0.800	1.80	0.460	3.60
MC822P	+75°C	0.740	0.710	1.80	0.400	3.60
MC722P	+15°C	0.865	0.865	1.80	0.475	3.60
MC722P	+25°C	0.850	0.850	1.80	0.460	3.60
MC722P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC822P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC722P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	2	-	300	-	280	-	280	μAdc	-	300	-	300	-	300	μAdc	2	-	3, 13	-	11	4
	I_{in}	3	-	150	-	140	-	140		-	150	-	150	-	150		3	-	12	-		
		9	-		-		-			-		-		-			9	-	-	-		
		12	-		-		-			-		-		-			12	-	-	-		
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	13	-	9	-	↓	↓
Output Current	I_{A4}	6	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	6	9	12	-	11	4
		10	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	10	12	9	-	11	4
Saturation Voltage	$V_{CE(sat)}$	6	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	12	-	9	11	4
		6*#	-		-		-			-		-		-			-	13	-	3		
		6*#	-		-		-			-		-		-			-	-	-	3, 13		
		6*##	-		-		-			-		-		-			-	3, 13	-	-		
		10	-		-		-			-		-		-			-	9	-	12		
		10*##	-		-		-			-		-		-			-	3	-	13		
		10*#	-		-		-			-		-		-			-	3, 13	-	-		
		10*##	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	3, 13	↓	↓

Pins not listed are left open.
* = Clock Pulse to pin 2, see Figure 1.

= Pin 9 HIGH
= Pin 12 HIGH
} Set by a momentary application of V_{BOT} prior to the application of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

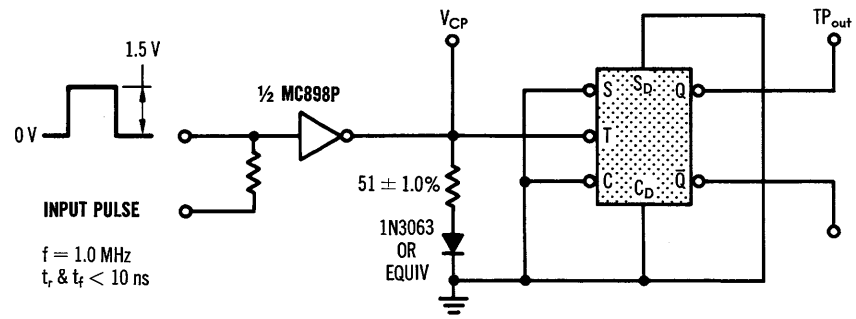
MC822P

T_A	V_L	V_H
+25°C	+0.460 V ± 2.0 mV	+0.850 V ± 2.0 mV
0°C	+0.500 V ± 2.0 mV	+0.900 V ± 2.0 mV
+75°C	+0.400 V ± 2.0 mV	+0.760 V ± 2.0 mV

MC722P

T_A	V_L	V_H
+25°C	+0.460 V ± 2.0 mV	+0.900 V ± 2.0 mV
+15°C	+0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+55°C	+0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

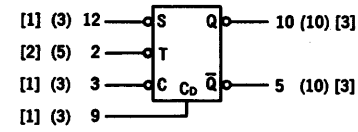
FIGURE 2 — TOGGLE MODE TEST CIRCUIT



THE SENSE FREQUENCY AT TP_{out} (0.5 MHz) SHOULD BE ½ THE FREQUENCY AT V_{CP} WHEN THE DUTY CYCLE IS VARIED BETWEEN 25% AND 75%.

MC723P • MC816P

J-K flip-flop with a direct clear input in addition to the clocked inputs.



$f_{tog} = 4$ MHz

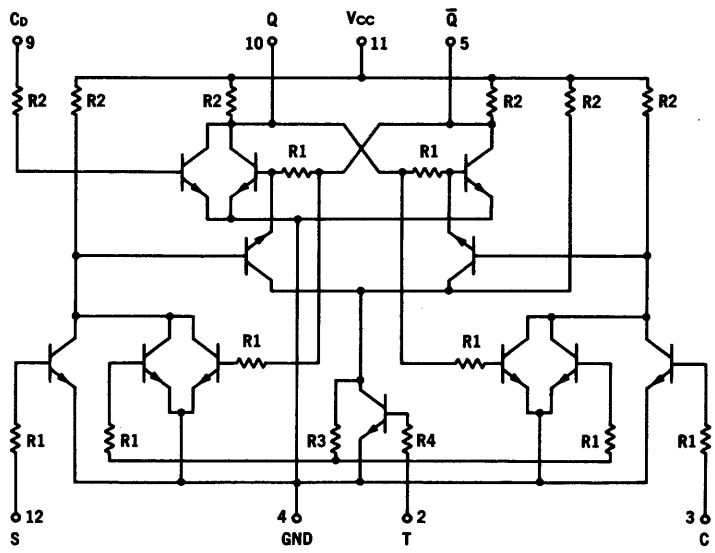
$P_D = 91$ mW (Only Clock Input High)
79 mW (Inputs Low)

CLOCKED INPUT OPERATION ①

t_n ③		t_{n+1} ③	
S	C	Q	$\overline{Q}$
1	1	Q_n ④	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n ④

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC816P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC723P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC816P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC723P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	2	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	2	-	3, 12	-	11	4
	I_{in}	3	-	600	-	600	-	570		-		-		-			3	-	10	-		
		9	-		-		-			-		-		-			9	-	5	-		
		12	-		-		-			-		-		-			12	-	5	-		
Output Current	I_{A3}	5	1.80	-	1.80	-	1.71	-	mAdc	1.65	-	1.65	-	1.56	-	mAdc	-	5	9, 12	-	11	4
		5		-		-		-			-		-		-		-	5, 9	12	-		4
		10		-		-		-			-		-		-		-	10	3	9		4, 5 §
Output Voltage	V_{out}	10	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	9	-	-	11	4, 5
		10*##	-		-		-			-		-		-			-	3, 12	-	-		4, 9
		10*	-		-		-			-		-		-			-	3	-	12		
		10*##	-		-		-			-		-		-			-	-	-	3, 12		
Saturation Voltage	$V_{CE(sat)}$	5	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	-	9	11	4, 5
		10	-		-		-			-		-		-			-	-	9	-		4, 5
		10	-		-		-			-		-		-			-	-	-	-		4, 10 §
Turn-On Voltage	V_{on}	10*##Δ	930	-	880	-	790	-	mVdc	865	-	850	-	800	-	mVdc	-	3, 12	-	-	11	4, 9
		10*Δ		-		-		-			-		-		-		-	12	-	3		
		10*#Δ		-		-		-			-		-		-		-	-	-	3, 12		

Pins not listed are left open.

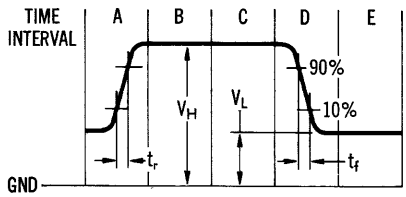
§ = Silicon diode to ground.

* = Clock Pulse to pin 2, See Figure 1.

= Pin 10 LOW
= Pin 5 LOW
} Set by a momentary ground prior to the application of the negative-going Clock pulse.

Δ = MC816P pin 10 loaded by: 1.56 mAdc (0°C and +75°C)
1.65 mAdc (+25°C)
MC723P pin 10 loaded by: 1.56 mAdc (+15°C and +55°C)
1.65 mAdc (+25°C)

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

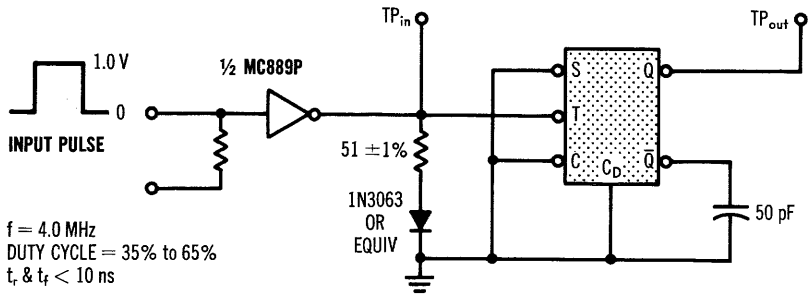
MC816P

T_A	V_L	V_H
+ 25°C	+0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+ 75°C	+0.450 V ± 2.0 mV	+0.840 V ± 2.0 mV

MC723P

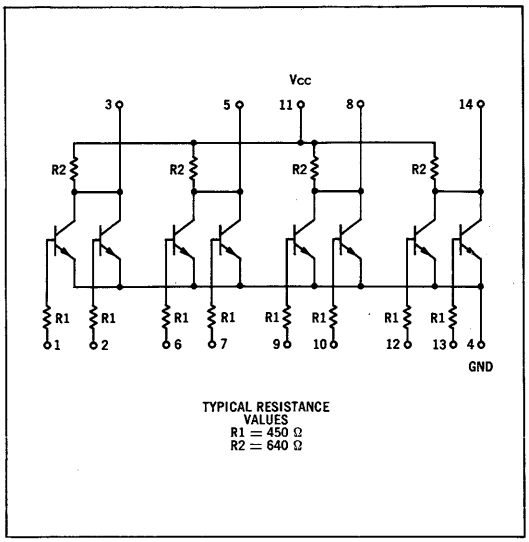
T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



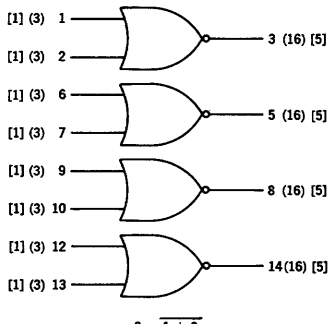
FREQUENCY AT TP_{out} SHOULD BE ½ THE FREQUENCY AT TP_{in}

MC724P • MC824P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

Four 2-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.

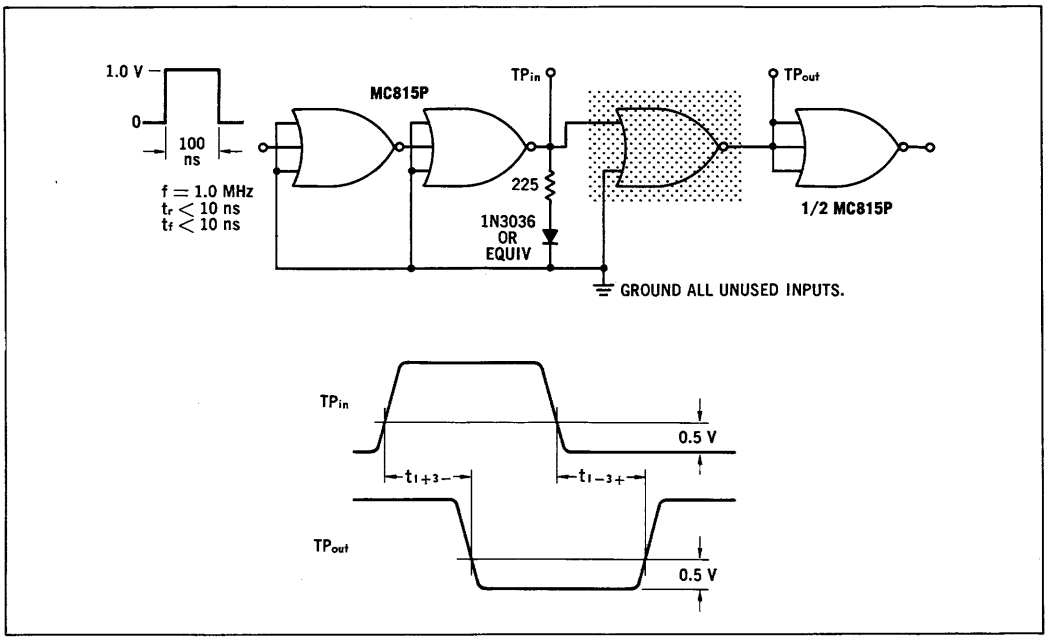


$3 = \overline{1 + 2}$

NUMBER IN PARENTHESIS INDICATES mW MRTL LOADING FACTOR
NUMBER IN BRACKETS INDICATES MRTL LOADING FACTOR

t_{pd} = 12 ns
P_D = 100 mW (Input High)
30 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

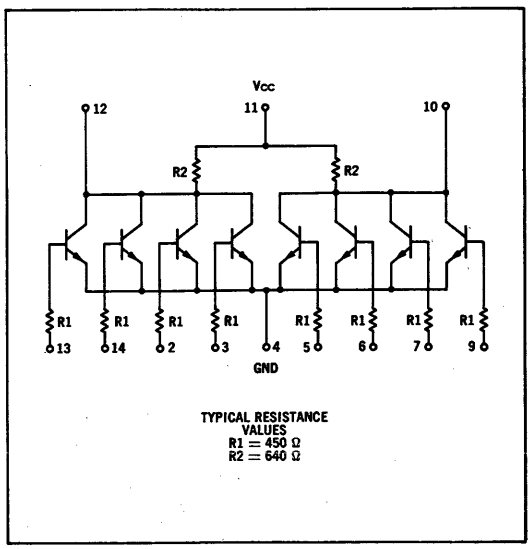
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC824P	0°C	0.960	0.930	1.80	0.570	3.60
MC824P	+25°C	0.910	0.880	1.80	0.500	3.60
MC824P	+75°C	0.820	0.790	1.80	0.450	3.60
MC724P	+15°C	0.865	0.865	1.80	0.475	3.60
MC724P	+25°C	0.850	0.850	1.80	0.460	3.60
MC724P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC824P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC724P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	4
		2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	1	-	11	4
Output Current	I_{A5}	3	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	1,2	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2,4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	1,4
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	2,4
		3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	2	-	11	1,4
Switching Time	$t_{on} + t_{off}$	1,3	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In: 1	Pulse Out: 3	-	-	11	2,4

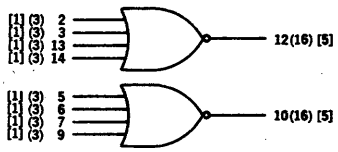
Ground input pins of gates not under test. Other pins not listed are left open.

MC725P • MC825P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

Two 4-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



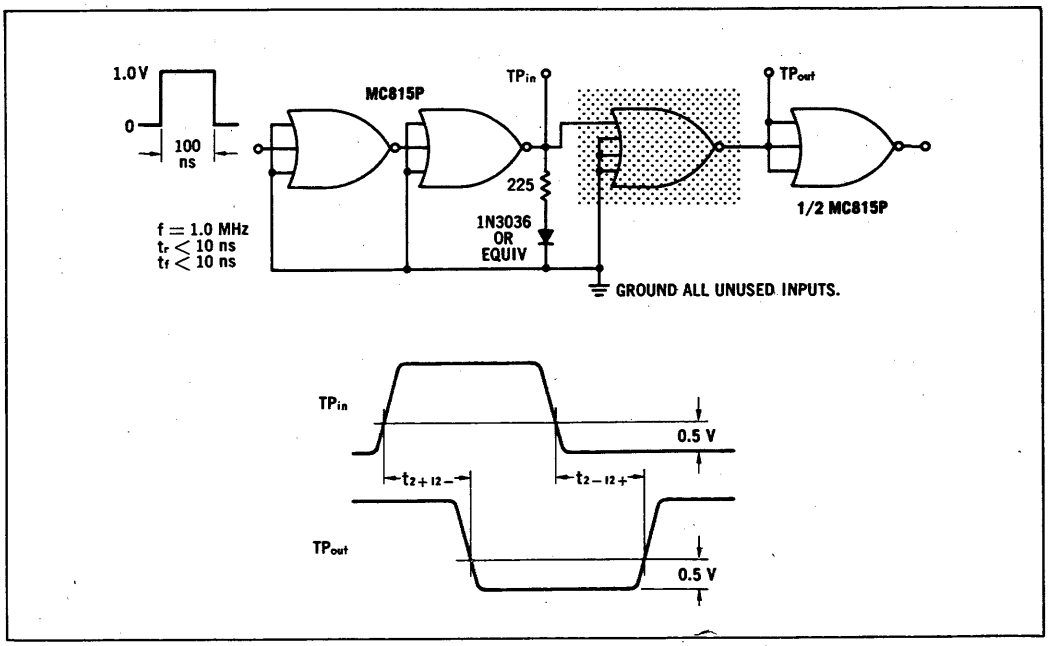
$12 = \overline{2 + 3 + 13 + 14}$

NUMBER IN PARENTHESES INDICATES mW MRTL LOADING FACTOR

NUMBER IN BRACKETS INDICATES MRTL LOADING FACTOR

t_{pd} = 12 ns
P_D = 60 mW (Input High)
15 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gate is tested in the same manner.

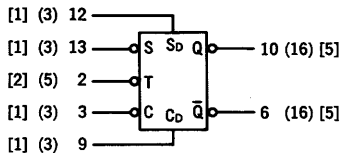
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC825P	0°C	0.960	0.930	1.80	0.570	3.60
MC825P	+25°C	0.910	0.880	1.80	0.500	3.60
MC825P	+75°C	0.820	0.790	1.80	0.450	3.60
MC725P	+15°C	0.865	0.865	1.80	0.475	3.60
MC725P	+25°C	0.850	0.850	1.80	0.460	3.60
MC725P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC825P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC725P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	3,13,14	-	11	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,13,14	-	↓	↓
		13	-		-		-			-		-		-			13	-	2,3,14	-		
		14	-		-		-			-		-		-			14	-	2,3,13	-		
Output Current	I_{A5}	12	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	12	-	2,3,13,14	11	4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-		2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓		↓	-	↓	↓	-	14	-	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	2	-	-		3,4,13,14
		12	-		-		-			-		-		-			-	3	-	-		2,4,13,14
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	13	-	11	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	-	2	-		3,4,13,14
		12	-		-		-			-		-		-			-	-	3	-		2,4,13,14
Switching Time	$t_{on} + t_{off}$	2, 12	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In 2	Pulse Out 12	-	-	11	3,4,13,14

Ground input pins of gate not under test. Other pins not listed are left open.

MC726P • MC826P

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



$f_{max} = 4$ MHz

$P_D = 100$ mW (Only Clock Input High)
86 mW (Inputs Low)

CLOCKED INPUT OPERATION ①

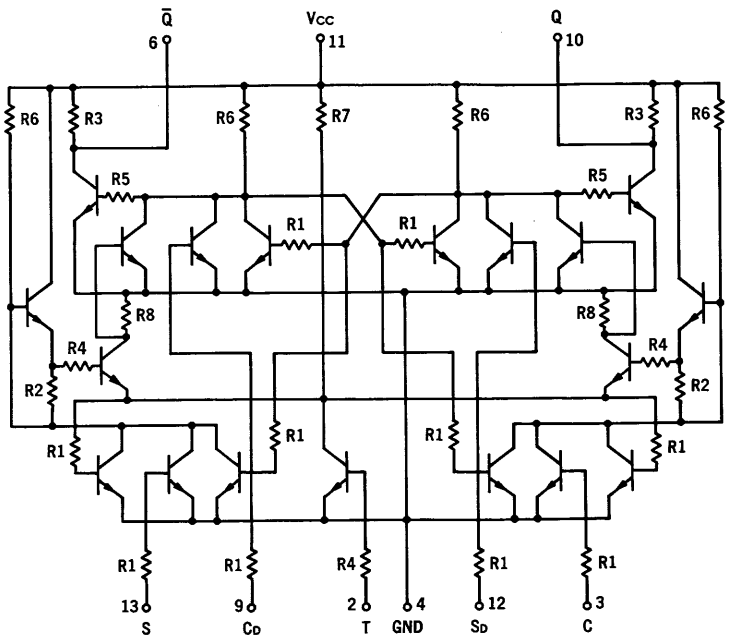
t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

DIRECT INPUT OPERATION ④

S_D	C_D	Q	$\bar{Q}$
0	0	⑤	⑤
1	0	1	0
0	1	0	1
1	1	0	0

1. Direct inputs (C_D and S_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock (T) to remain unchanged.
5. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
6. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 550 Ω
R2 = 2 k	R6 = 900 Ω
R3 = 640 Ω	R7 = 700 Ω
R4 = 300 Ω	R8 = 3 k

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC826P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC726P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

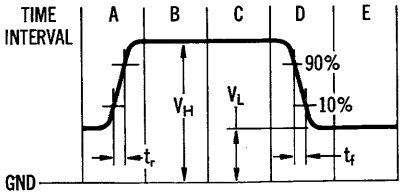
Characteristic	Symbol	Pin Under Test	MC826P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC726P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	2	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	2	-	3, 13	-	11	4
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	12	-		
		9	-		-		-			-		-		-			9	-	-	-		
		12	-		-		-			-		-		-			12	-	-	-		
		13	-		-		-			-		-		-			13	-	9	-		
Output Current	I_{A5}	6	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	-	6, 12	9	-	11	4
		10	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	-	9, 10	12	-	11	4
Saturation Voltage	$V_{CE(sat)}$	6	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	12	-	9	11	4
		6*#	-		-		-			-		-		-			-	13	-	3		
		6*#	-		-		-			-		-		-			-	-	-	3, 13		
		6*##	-		-		-			-		-		-			-	3, 13	-	-		
		10	-		-		-			-		-		-			-	9	-	12		
		10*##	-		-		-			-		-		-			-	3	-	13		
		10*#	-		-		-			-		-		-			-	3, 13	-	-		
		10*##	-		-		-			-		-		-			-	-	-	3, 13		

Pins not listed are left open.

* Clock Pulse to pin 2, see Figure 1.

\# Pin 9 HIGH
\#\# Pin 12 HIGH
} Set by momentary application of V_{BOT} prior to the application of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

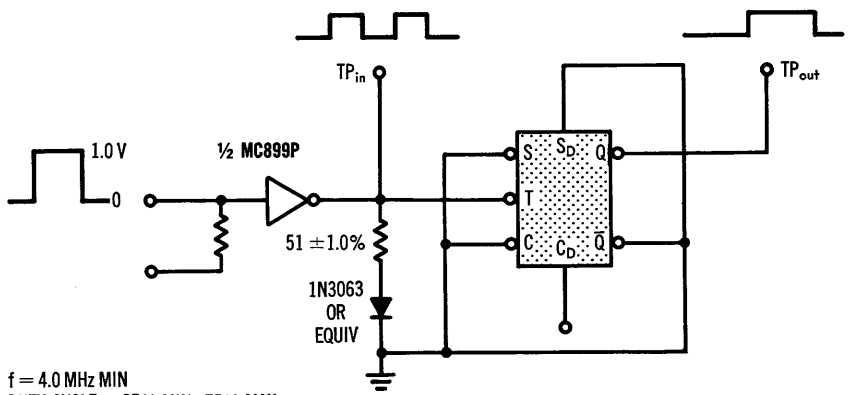
MC826P

T_A	V_L	V_H
+25°C	+0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+75°C	+0.450 V ± 2.0 mV	+0.840 V ± 2.0 mV

MC726P

T_A	V_L	V_H
+25°C	+0.460 V ± 2.0 mV	+0.900 V ± 2.0 mV
+15°C	+0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+55°C	+0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

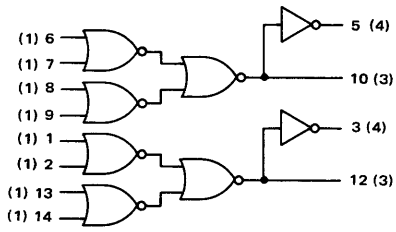
FIGURE 2 — TOGGLE MODE TEST CIRCUIT



f = 4.0 MHz MIN
DUTY CYCLE = 25% MIN., 75% MAX.
t_r & $t_f < 10$ ns

OUTPUT FREQUENCY SHALL BE ½ OF TP_{in} FREQUENCY.

MC764P • MC864P



$12 = (1 + 2) \cdot (13 + 14)$

$3 = \overline{1} \cdot \overline{2} + \overline{13} \cdot \overline{14}$

t_{pd} = 65 ns (Pins 5 and 3)
t_{pd} = 35 ns (Pins 10 and 12)
P_D = 25 mW

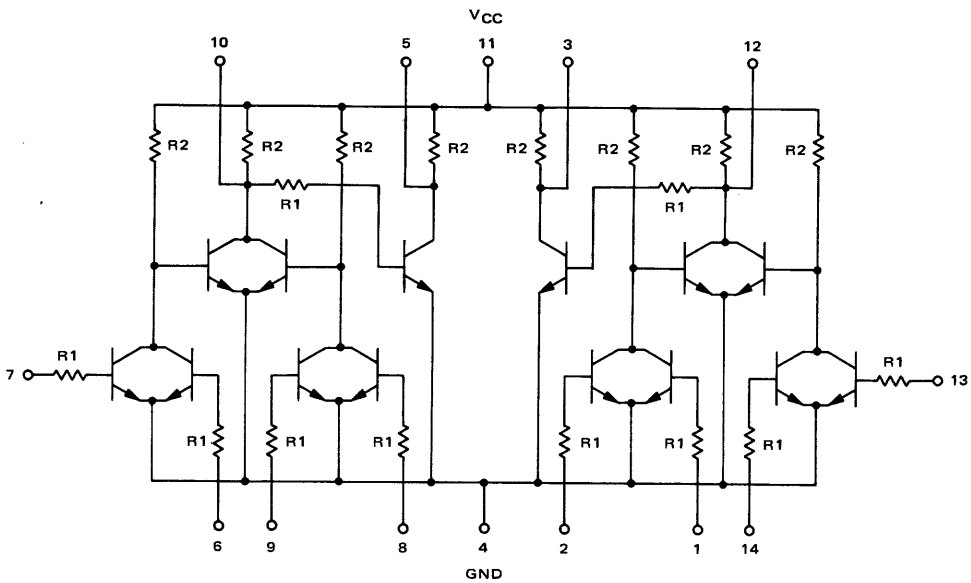
Number in Parenthesis Indicates Loading Factor.

MC764P/864P is a dual multi-purpose device. Types of recommended utilization include:

Dual Exclusive OR-NOR Gate, when $6 = \overline{8}$ and $7 = \overline{9}$, then $10 = 6 \cdot \overline{7} + \overline{6} \cdot 7$ (This equals the sum when used as a Half-Adder) and $5 = 6 \cdot 7 + \overline{6} \cdot \overline{7}$.

Dual Data Distributor, with data on 6 and 9, control on 7 and control on 8 so that $10 = 9 \cdot 7 + 6 \cdot \overline{7}$ and $5 = \overline{9} \cdot 7 + \overline{6} \cdot \overline{7}$.

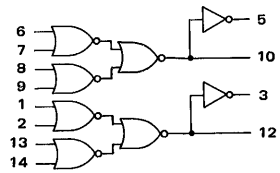
Dual Gated R-S Flip-Flop, by connecting the non-inverted output back to an input. When pin 10 is connected to pin 9 then $\overline{10} = 5 = \overline{6} \cdot \overline{7}$ and $\overline{5} = 10 = 8 \cdot (6 + 7)$. Pin 10 will remain in its previous state ($10^{n+1} = 10^n$) whenever the input configuration is $\overline{8} \cdot (6 + 7)$. Another name for the flip-flop, then, is a $\overline{R1}\ \overline{R2}$–S flip-flop.



TYPICAL RESISTANCE VALUES
R1 = 1.5 kΩ
R2 = 3.6 kΩ

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner.

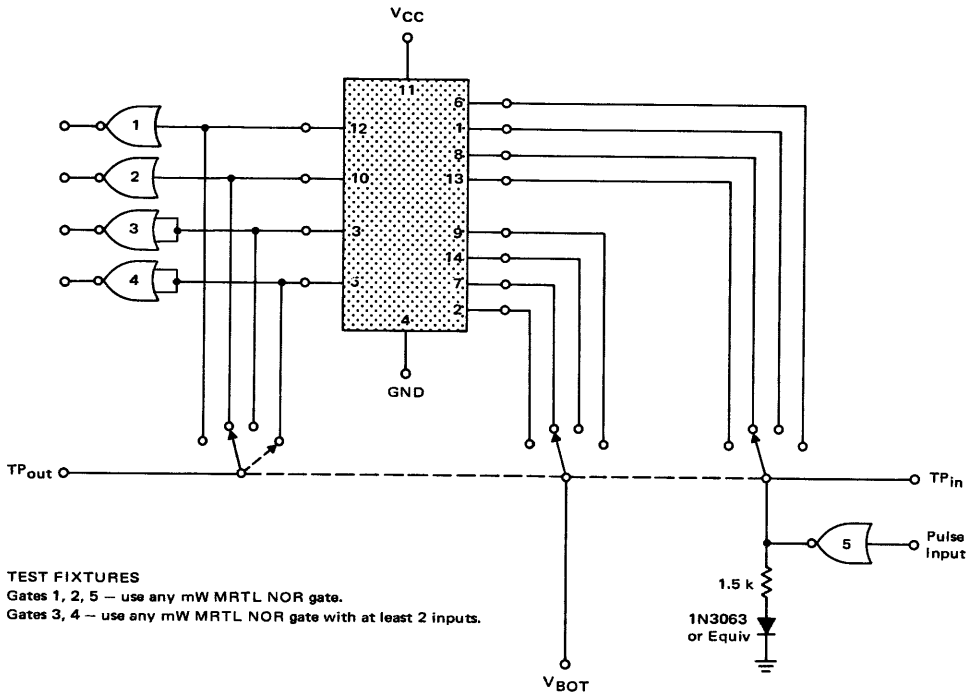


@ Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC864P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC764P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

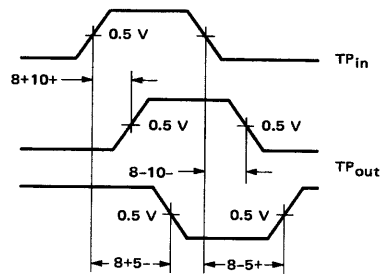
Characteristic	Symbol	Pin Under Test	MC864P TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC764P TEST LIMITS +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	6	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	6	-	7	-	11	4
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	7	-	6	-	↓	↓
		8	-		-		-			-		-		-			8	-	9	-		
		9	-		-		-			-		-		-			9	-	8	-		
Output Current	I_{A4}	5	640	-	640	-	600	-	μAdc	640	-	640	-	640	-	μAdc	-	5	-	6,7,8,9	11	4
	I_{A3}	10	↓	-	↓	-	↓	-	↓	480	-	480	-	480	-	↓	-	7,8,10	-	-	↓	↓
		10		-		-		-		480	-	480	-	480	-		-	6,9,10	-	-		
Output Voltage	V_{out}	5	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	6,7,8,9	-	-	11	4
		10	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	8,9	-	6,7	↓	↓
		10	-		-		-			-		-		-			-	6,7	-	8,9		
		10	-		-		-			-		-		-			-	-	-	6,7,8,9		
																	Pulse In	Pulse Out				
Switching Times	t_{8+5-}	5	-	-	-	80	-	-	ns	-	-	-	80	-	-	ns	8	5	9	-	11	4
	t_{8-5+}	5	-	-	-	60	-	-	↓	-	-	-	60	-	-	↓	↓	5	9	-	↓	↓
	t_{8+10+}	10	-	-	-	65	-	-		-	-	-	65	-	-			10	7	-		
	t_{8-10-}	10	-	-	-	35	-	-		-	-	-	35	-	-		↓	10	7	-		

Ground unused input pins. Other pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

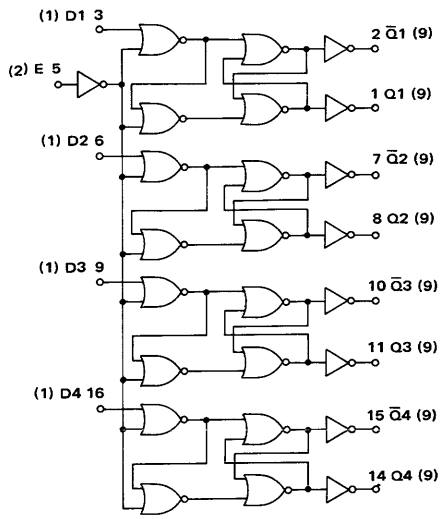


TEST FIXTURES
Gates 1, 2, 5 – use any mW MRTL NOR gate.
Gates 3, 4 – use any mW MRTL NOR gate with at least 2 inputs.



INPUT PULSE
f = 4.0 MHz
PW = 100 ns
PH = 1.5 V
$t_r = t_f \leq 10$ ns

MC767P • MC867P



Number in Parenthesis Indicates Loading Factor.

The MC767P/867P Quad Latch is designed for use in any application requiring temporary storage. A common enable line allows only the desired information to be "clocked in." When the level of the enable line is high, the output of each latch will be synonymous with the data input to that latch. When the enable line level goes low, the output will remain at the previous level, independent of any changes at the input. The MC767P/867P is available in a 16-pin dual in line plastic package.

TRUTH TABLE

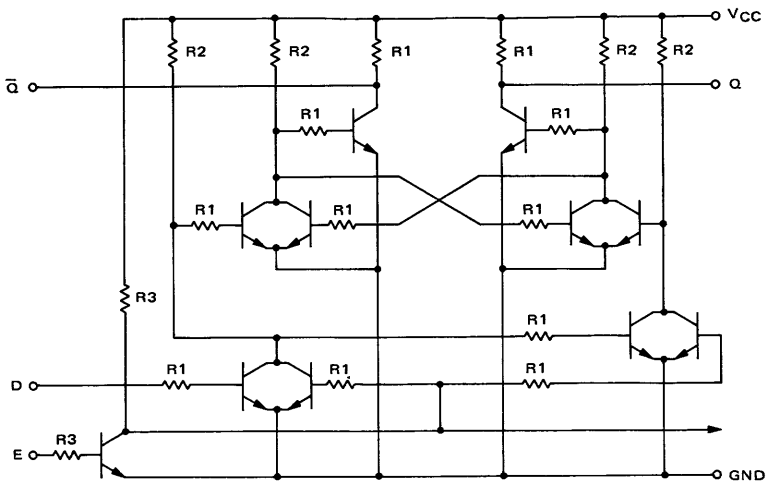
E	D	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	Q_n	$\bar{Q}_n$
0	1	Q_n	$\bar{Q}_n$
1	0	0	1
1	1	1	0

$t_{pd(avg)}$* = 50 ns typ

P_D = 110 mW typ

*Avg $t_{pd} = \frac{t_{on} + t_{off}}{2}$

1/4 OF CIRCUIT SHOWN



TYPICAL RESISTANCE VALUES

R1 = 1.5 k R3 = 750 Ω

R2 = 3.6 k

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one latch. The other latches are tested in the same manner.

@ Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC867P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC767P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

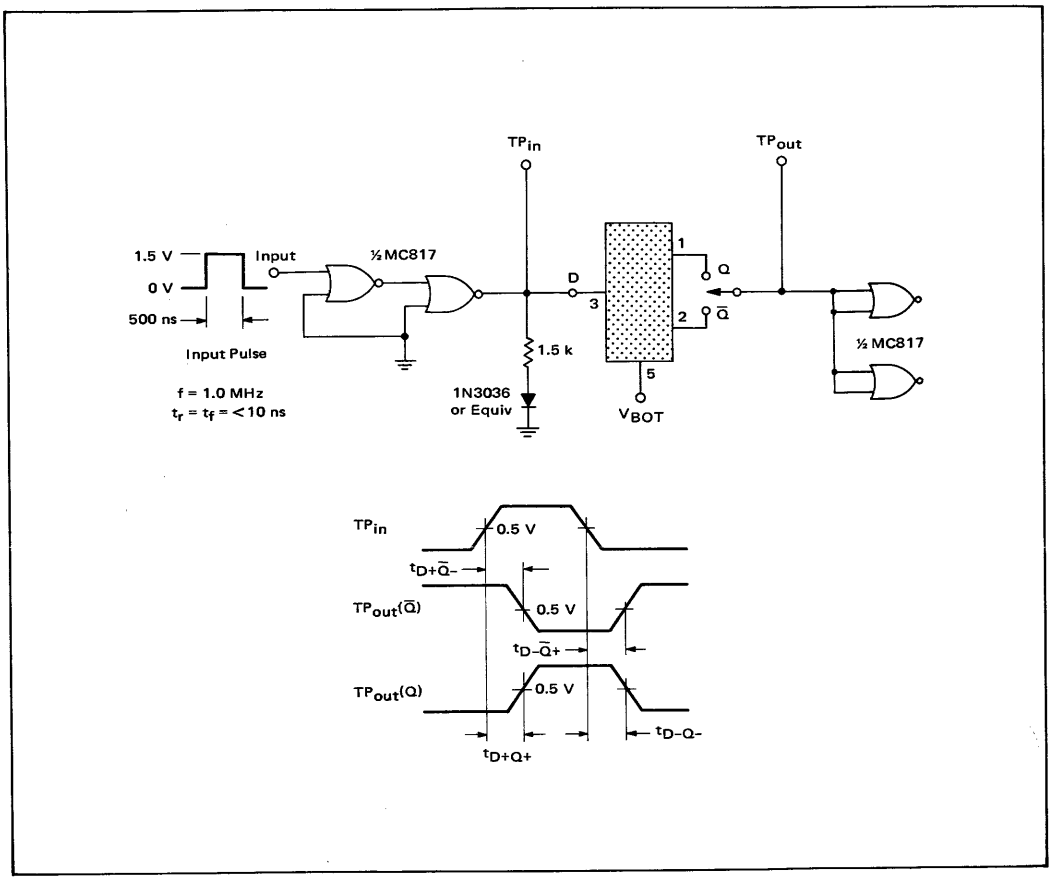
Characteristic	Symbol	Pin Under Test	MC867P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC767P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	3	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	3	-	-	-	13	4,5
	$2\ I_{in}$	5	-	300	-	280	-	280	μAdc	-	300	-	300	-	300	μAdc	5	-	-	-	13	4
Output Current	I_{A9}	1	-1.28	-	-1.28	-	-1.20	-	mAdc	-1.28	-	-1.28	-	-1.28	-	mAdc	3,5	1	-	-	13	4
		2	-1.28	-	-1.28	-	-1.20	-	mAdc	-1.28	-	-1.28	-	-1.28	-	mAdc	5	2	-	-	13	3,4
Saturation Voltage	$V_{CE(sat)}$	1	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	5	-	-	-	13	3,4
		2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	3,5	-	-	-	↓	4
		1	-		-		-			-		-		-			3,5*	-	-	-		3,4,5*
		2	-		-		-			-		-		-			3,5**	-	-	-		3,4,5**
Power Supply Drain Current	I_{PD}	13	-	-	-	35	-	-	mAdc	-	-	-	35	-	-	mAdc	-	-	-	-	13	4,5
Switching Times																	Pulse In	Pulse Out				
	t_{3+1+}	1	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	3	1	5	-	13	4
	t_{3-1-}	1	-	-	-	70	-	-	↓	-	-	-	70	-	-	↓	↓	1	↓	-	↓	↓
	t_{3+2-}	2	-	-	-	90	-	-		-	-	-	90	-	-			2		-		
	t_{3-2+}	2	-	-	-	60	-	-		-	-	-	60	-	-		↓	2		-	↓	↓

Ground inputs of latches not under test. Other pins not listed are left open.

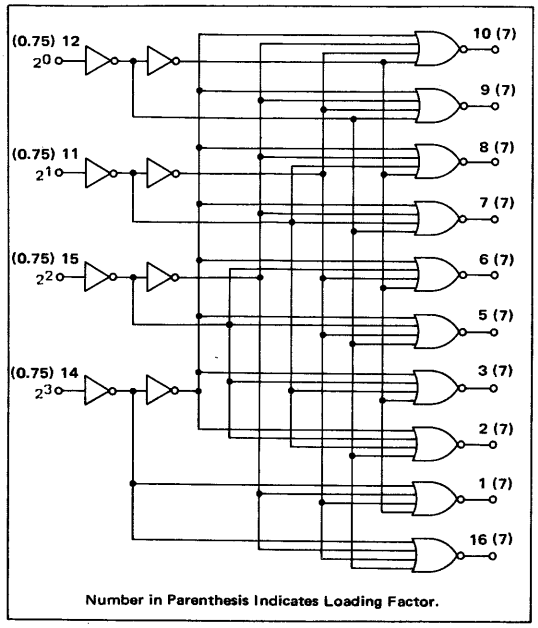
*A negative pulse from V_{in} to ground is applied to pin 5, then 2.0 ms later a positive pulse from ground to V_{in} is applied to pin 3 for measurement of V_{CE} on pin 1.

**A negative pulse from V_{in} to ground is applied to pin 5, then 2.0 ms later a positive pulse from V_{in} to ground is applied to pin 3 for measurement of V_{CE} on pin 2.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



MC770P • MC870P*



Number in Parenthesis Indicates Loading Factor.

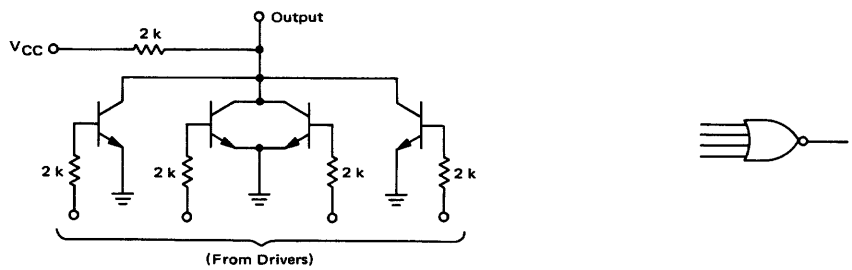
The MC770P/870P is a monolithic BCD to decimal decoder consisting of eight inverters and ten 4-input NOR gates which are utilized to convert binary coded decimal (8-4-2-1) input to an output, via the appropriate one of ten output lines.

TRUTH TABLE

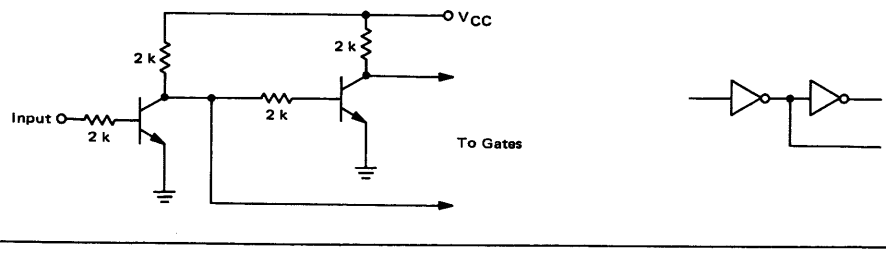
	INPUT (BCD)				OUTPUT (DECIMAL)									
Value	2^3	2^2	2^1	2^0	0	1	2	3	4	5	6	7	8	9
Pin No.	14	15	11	12	10	9	8	7	6	5	3	2	1	16
Logic Level	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	0	0	0	1	0	1	0	0	0	0	0	0	0	0
	0	0	1	0	0	0	1	0	0	0	0	0	0	0
	0	0	1	1	0	0	0	1	0	0	0	0	0	0
	0	1	0	0	0	0	0	0	1	0	0	0	0	0
	0	1	0	1	0	0	0	0	0	1	0	0	0	0
	0	1	1	0	0	0	0	0	0	0	1	0	0	0
	0	1	1	1	0	0	0	0	0	0	0	1	0	0
	1	0	0	0	0	0	0	0	0	0	0	0	1	0
	1	0	0	1	0	0	0	0	0	0	0	0	0	1
	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	0	0	0	0	0	0	0	0	0	0

t_{pd} = 36 ns
P_D = 100 mW typ (All inputs high)

4-INPUT "NOR" GATE (1-OF-10)



DUAL SERIES INVERTING DRIVER (1-OF-4)



*P suffix = 16 pin dual-in-line plastic package, Case 612.

ELECTRICAL CHARACTERISTICS

@ Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC870P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC770P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

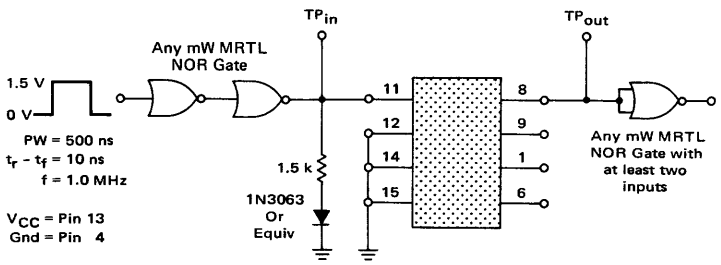
Characteristic	Symbol	Pin Under Test	MC870P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC770P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$0.75\ I_{in}$	11	-	113	-	105	-	105	μAdc	-	113	-	113	-	113	μAdc	11	-	-	-	13	4,12,14,15
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	12	-	-	-	↓	4,11,14,15
		14	-		-		-			-		-		-			14	-	-	-		4,11,12,15
		15	-		-		-			-		-		-			15	-	-	-		4,11,12,14
Output Current	I_{A7}*	10	-1.05	-	-0.98	-	-0.98	-	mAdc	-1.05	-	-1.05	-	-1.05	-	mAdc	-	10*	-	*	13	4
Output Voltage	V_{out}	1**	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	**	-	**	13	4
Power Supply Current Drain	I_{PD}	13	-	-	-	42	-	-	mAdc	-	-	-	42	-	-	mAdc	11,12,14,15	-	-	-	13	4
Switching Times																	Pulse In	Pulse Out				
	t_{14+1+}	1	-	-	-	65	-	-	ns	-	-	-	65	-	-	ns	14	1	-	-	13	4,11,12,15
	t_{14-1-}	1	-	-	-	50	-	-	↓	-	-	-	50	-	-	↓	14	1	-	-	↓	4,11,12,15
	t_{15+6+}	6	-	-	-	65	-	-		-	-	-	65	-	-		15	6	-	-		4,11,12,14
	t_{15-6-}	6	-	-	-	50	-	-		-	-	-	50	-	-		15	6	-	-		4,11,12,14
	t_{11+8+}	8	-	-	-	65	-	-		-	-	-	65	-	-		11	8	-	-		4,12,14,15
	t_{11-8-}	8	-	-	-	50	-	-		-	-	-	50	-	-		11	8	-	-		4,12,14,15
	t_{12+9+}	9	-	-	-	65	-	-		-	-	-	65	-	-		12	9	-	-		4,11,14,15
	t_{12-9-}	9	-	-	-	50	-	-		-	-	-	50	-	-		12	9	-	-		4,11,14,15

Pins not listed are left open.

*Test is shown for one output only. The other outputs are tested in the same manner. Inputs must have V_{on} and V_{off} applied in accordance with the truth table for the output under test.

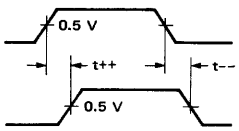
**Test shown is for one output only. All nine outputs, excepting the one which is "ON" according to the truth table, are to be tested for all usable input configurations shown in the truth table — a total of 90 tests.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



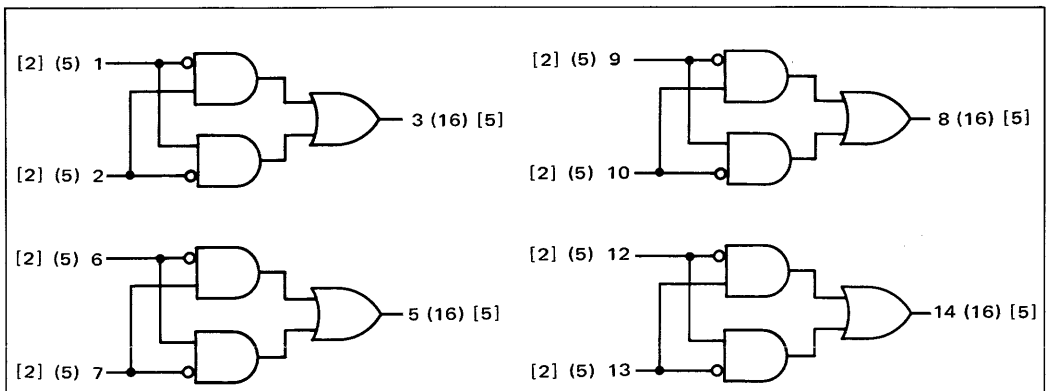
Switching Circuit indicates one input and one output. Other input and output combinations are tested in a similar manner.

Load and driving gates must be of same series as unit under test.



MC771P · MC871P

Four gate arrays designed to provide the Exclusive OR function. The output is high only if one input is high and all other inputs are low.



POSITIVE LOGIC

$3 = 1 \cdot \bar{2} + \bar{1} \cdot 2$

t_{pd} = 12 ns typ
P_D = 87 mW typ

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR mW MRTL

NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

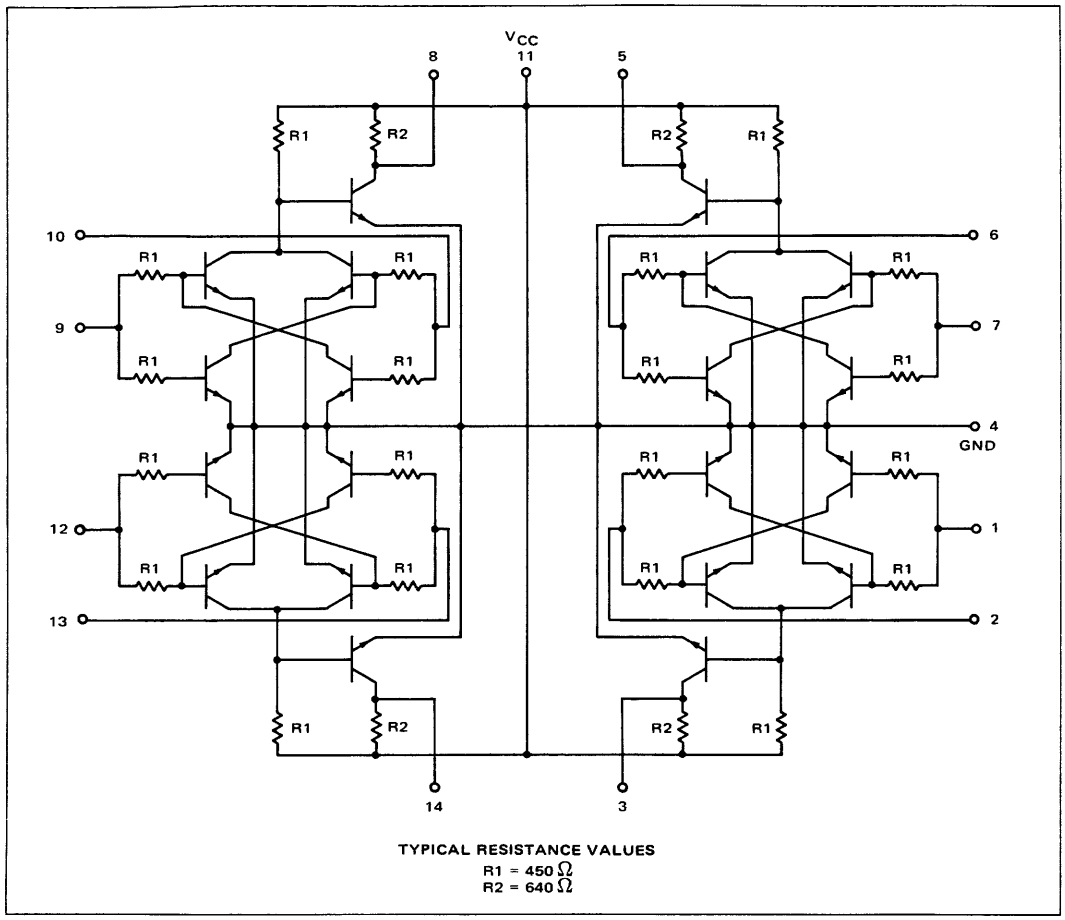
ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

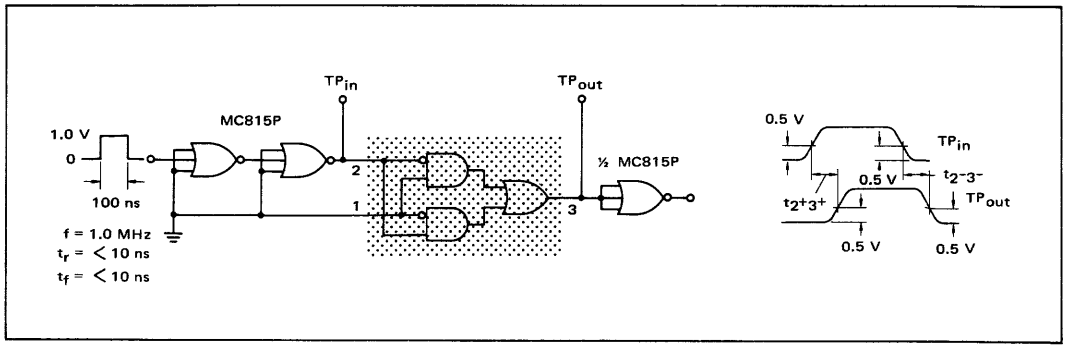
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC871P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC771P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC871P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC771P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	1	-	1.2	-	1.2	-	1.1	mAdc	-	1.00	-	1.00	-	0.94	mAdc	1	-	2	-	11	4
		2	-	1.2	-	1.2	-	1.1	mAdc	-	1.00	-	1.00	-	0.94	mAdc	2	-	1	-	11	4
Output Current	I_{A5}	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	1,3	-	2	11	4
		3	3.00	-	3.00	-	3.00	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	2,3	-	1	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	-	1,2	11	4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1,2	-	-	11	4
Switching Time	t	1→3-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In 1	2	Pulse Out 3	-	11	4
		1-3+	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	1	2	↓	-	↓	↓
		2→3+	-	-	-		-	-		-	-	-		-	-		2	-		1		
		2-3-	-	-	-		-	-		-	-	-		-	-		2	-		1		

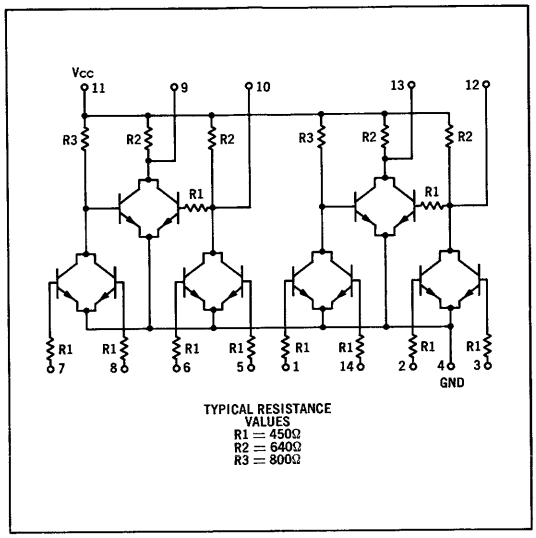
Ground inputs of gates not under test. Other pins not listed are left open.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

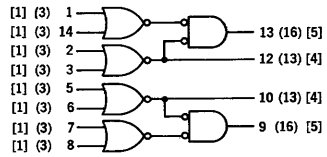


MC775P • MC875P



TYPICAL RESISTANCE VALUES
R1 = 450Ω
R2 = 640Ω
R3 = 800Ω

Two half-adder devices in a single package. Each device can be used to supply the SUM and CARRY operations on two input signals. E g.,if the inputs are applied to pins 1 and 14, and their complements to pins 2 and 3, the SUM of the inputs appears on pin 13 while the CARRY appears on pin 12.

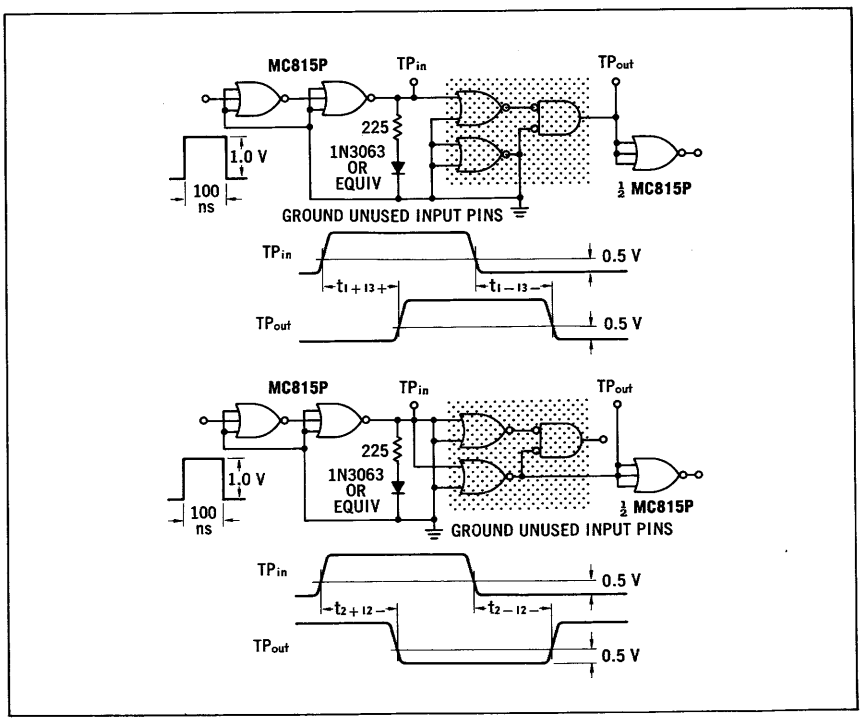


IF: $2 = \overline{1}$, & $3 = \overline{14}$
THEN: $12 = 1 \cdot 14$, & $13 = 1 \cdot \overline{14} + \overline{1} \cdot 14$

t_{pd} = 20 ns typ
P_D = 120 mW typ

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-adder only.
The other half-adder is tested in the same manner.

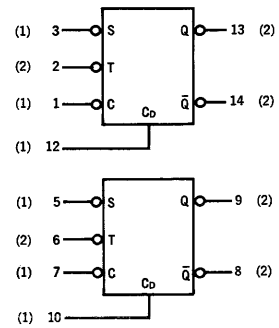
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC875P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC775P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC875P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC775P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	14	-	11	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	3	-	↓	↓
		3	-		-		-			-		-		-			3	-	2	-		
		14	-		-		-			-		-		-			14	-	14	-		
Output Current	I_{A4}	12	2.4	-	2.4	-	2.28	-	mAdc	-	-	-	-	-	-	-	-	12	-	2, 3	11	4
	I_{A5}	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.5	-	mAdc	-	1, 2, 13	-	-	↓	↓
	I_{A5}	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.5	-	mAdc	-	3, 13, 14	-	-	↓	↓
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓
		13	-		-		-			-		-		-			-	12	1, 13	-		
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	2	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	↓
		13	-		-		-			-		-		-			-	-	1, 14	2, 3		
		13	-		-		-			-		-		-			-	-	2, 3	1, 14		
Switching Time	t	2+12-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	Pulse In 2	Pulse Out 12	-	-	11	4
		2-12+	-	-	-	30	-	-	↓	-	-	-	30	-	-	↓	2	12	-	-	↓	4
		1+13+	-	-	-	36	-	-		-	-	-	36	-	-		1	13	-	-		4, 12
		1-13-	-	-	-	36	-	-		-	-	-	36	-	-		1	13	-	-		4, 12

Ground inputs of half-adder not under test. Other pins not listed are left open.

MC776P • MC876P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



f_{TOG} = 3 MHz min
P_D = 41 mW (Only Clock Input High)
29 mW (All Inputs Low)

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR

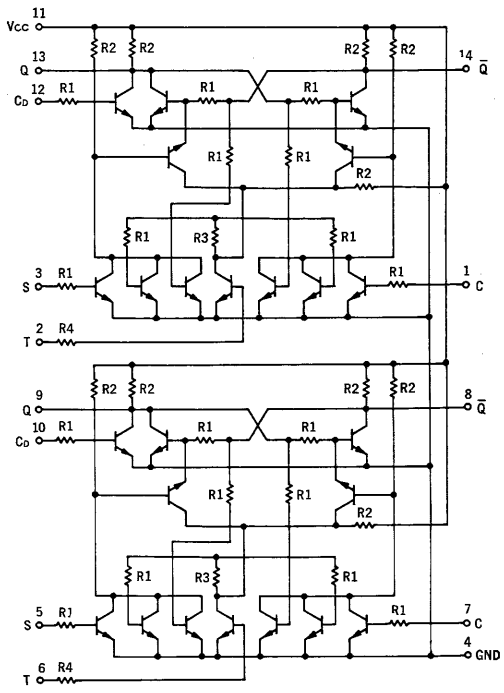
CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	Q̄
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

① Direct input (C_D) must be low.

② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

③ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 1.5k R3 = 3.0k
R2 = 3.6k R4 = 750Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

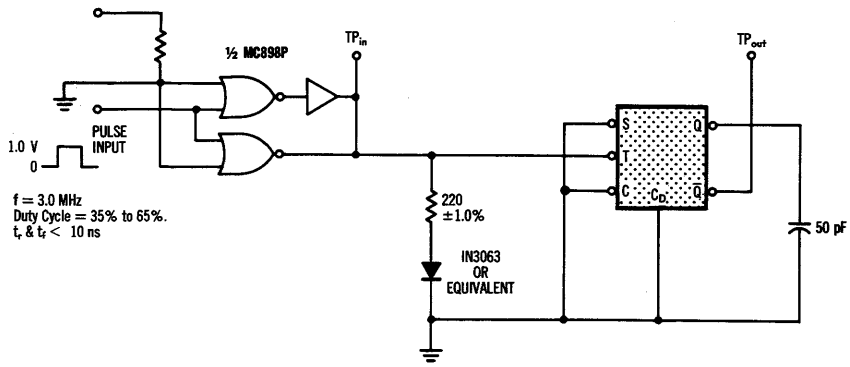
	@ Test Temperature	TEST VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	TEST VALUES (μA) I_0
MC876P	0°C	0.880	0.850	1.80	0.500	3.60	270
MC876P	+25°C	0.830	0.800	1.80	0.460	3.60	290
MC876P	+75°C	0.740	0.710	1.80	0.400	3.60	255
MC776P	+15°C	0.865	0.865	1.80	0.475	3.60	270
MC776P	+25°C	0.850	0.850	1.80	0.460	3.60	270
MC776P	+ 55°C	0.800	0.800	1.80	0.430	3.60	270

Characteristic	Symbol	Pin Under Test	MC876P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC776P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VALUES APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	I_0	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	13	-	11	-	4
	$2\ I_{in}$	2	-	300	-	280	-	280		-	300	-	300	-	300		2	-	1, 3	-		-	
	I_{in}	3	-	150	-	140	-	140		-	150	-	150	-	150		3	-	14	-		-	
	I_{in}	12	-	150	-	140	-	140		-	150	-	150	-	150		12	-	14	-		-	
Output Current	I_{A2}	13	320	-	320	-	300	-	μAdc	320	-	320	-	320	-	μAdc	-	13	1	12	11	-	4, 14 §
		14		-		-		-			-		-		-		-	14	3, 12	-		-	
		14		-		-		-			-		-		-		-	12, 14	3	-		-	
Output Voltage	V_{out}	13	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-		-	4, 14
		13	-		-		-			-		-		-			-	14	-	-		-	4, 13 §
		13*†	-		-		-			-		-		-			-	1, 3	-	-		14	4, 12
		13*#	-		-		-			-		-		-			-	1	-	3			
		13*#	-		-		-			-		-		-			-	-	-	1, 3			
		14	-		-		-			-		-		-			-	13	-	-		-	14 §
Saturation Voltage	$V_{CE(sat)}$	13	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	12	-	11	-	4, 14
		13	-		-		-			-		-		-			-	-	-	-		-	4, 13 §
		14	-		-		-			-		-		-			-	-	-	12		-	4, 14 §
Turn On Voltage	V_{on}	13*#	850	-	800	-	710	-	mVdc	865	-	850	-	800	-	mVdc	-	1, 3	-	-	11	13	4, 12
		13*†		-		-		-			-		-		-		-	3	-	1			
		13*†		-		-		-			-		-		-		-	-	-	1, 3			

* Clock Pulse to pin 2
† Pin 13 = LOW } Set by a momentary ground prior to the
# Pin 14 = LOW } application of the negative-going clock.

§ ground thru diode (cathode to ground).
Ground inputs of flip-flop not under test.
Other pins not listed are left open.

TOGGLE MODE TEST CIRCUIT



1. Set up the circuit with the Input Pulse as given.
2. The circuit should toggle with an output (TP_{out}) sense frequency of 1.5 MHz as the duty cycle is varied between 35% and 65%.

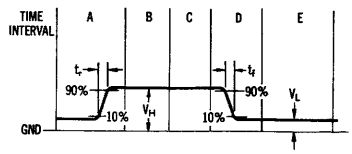
CLOCK PULSE

MC776P		
T_A	V_L	V_H
15°C	0.475 V	0.915 V
25°C	0.460 V	0.900 V
55°C	0.430 V	0.850 V

MC876P		
T_A	V_L	V_H
0°C	0.50 V	0.900 V
25°C	0.46 V	0.850 V
75°C	0.40 V	0.760 V

All values are ± 2.0mV

CLOCK PULSE DEFINITION

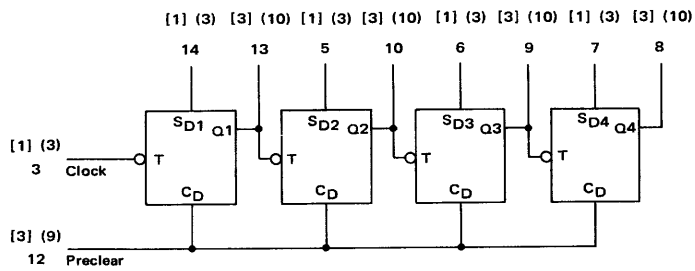


SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, but should be < 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC777P • MC877P

This monolithic binary counter has outputs corresponding to a standard 8-4-2-1 binary code, with individual presets and a common preclear input.

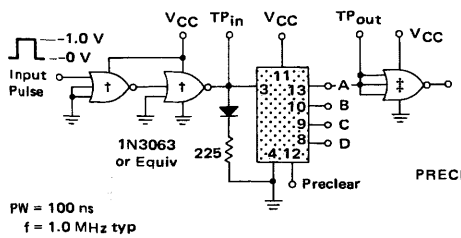


DECODING LOGIC	
0	$\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$
1	$A\,\overline{B}\,\overline{C}\,\overline{D}$
2	$\overline{A}\,B\,\overline{C}\,\overline{D}$
3	$A\,B\,\overline{C}\,\overline{D}$
4	$\overline{A}\,\overline{B}\,C\,\overline{D}$
5	$A\,\overline{B}\,C\,\overline{D}$
6	$\overline{A}\,B\,C\,\overline{D}$
7	$A\,B\,C\,\overline{D}$
8	$\overline{A}\,\overline{B}\,\overline{C}\,D$
9	$A\,\overline{B}\,\overline{C}\,D$
10	$\overline{A}\,B\,\overline{C}\,D$
11	$A\,B\,\overline{C}\,D$
12	$\overline{A}\,\overline{B}\,C\,D$
13	$A\,\overline{B}\,C\,D$
14	$\overline{A}\,B\,C\,D$
15	$A\,B\,C\,D$

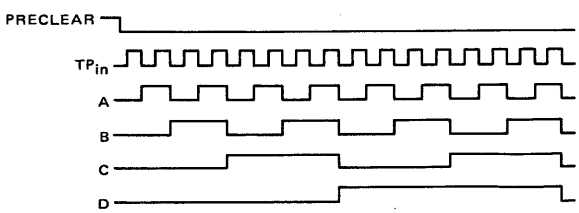
Numbers in Brackets Indicate MRTL Loading Factor.
Numbers in Parenthesis Indicate mW MRTL Loading Factor.

f_{Tog} = 4.0 MHz
P_D = 180 mW typ

TOGGLE TEST CIRCUIT AND WAVEFORMS



† = Any MRTL NOR gate.
‡ = Any MRTL 3-input NOR gate.



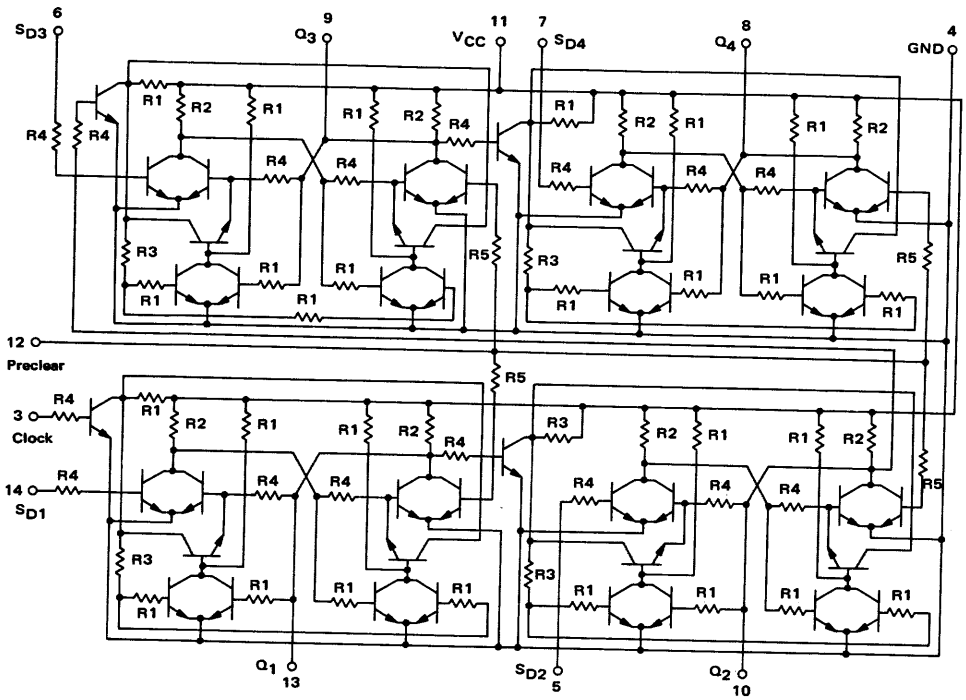
ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only. The other flip-flops are tested in the same manner.

@ Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC877P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC777P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC877P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC777P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	3	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	3	-	-	-	11	4
	I_{in}	5	-	600	-	600	-	570		-	500	-	500	-	470		5	-	-	-		
	$3\ I_{in}$	12	-	1800	-	1800	-	1710		-	1500	-	1500	-	1410		12	-	-	-		
Output Current	I_{A3}	10	-1.80	-	-1.80	-	-1.71	-	mAdc	-1.65	-	-1.65	-	-1.56	-	mAdc	10	-	5	-	11	4
Output Voltage	V_{out}	10	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	-	-	11	4.10*
Saturation Voltage	$V_{CE(sat)}$	10	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	-	-	11	4
Power Supply Current Drain	I_{PD}	11	-	-	-	80	-	-	mAdc	-	-	-	80	-	-	mAdc	-	-	12	-	11	4
																	Pulse In	Pulse Out				
Switching Times	t_{3-8+}	8	-	-	-	100	-	-	ns	-	-	-	100	-	-	ns	3	8	-	-	11	4
	t_{3-8-}	8	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	3	8	-	-	11	4

*Apply a momentary ground to pin 10 prior to measurement.
Ground input pins of flip-flops not under test. Other pins not listed are left open.



TYPICAL RESISTANCE VALUES

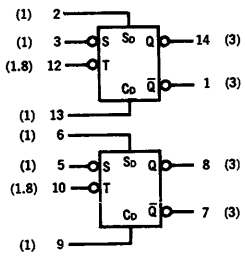
R1 = 1.5 k R3 = 750 Ω

R2 = 640 Ω R4 = 450 Ω

R5 = 600 Ω

MC778P • MC878P

The type "D" Flip-Flop is a storage element that stores the state of the S input during negative transitions of the T input. The flip-flop state is not affected by changes in the S input during either the low or the high state of the T input. S_D and C_D inputs may be used for asynchronous operation.



DIRECT INPUT OPERATION①

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION③

t_n④	t_{n+1}④	
S	Q	$\bar{Q}$
1	1	0
0	0	1

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR

P_D = 48 mW (Direct Set, S_D, and Direct Clear, C_D, Low; all other inputs high)
35 mW (All Inputs Low)

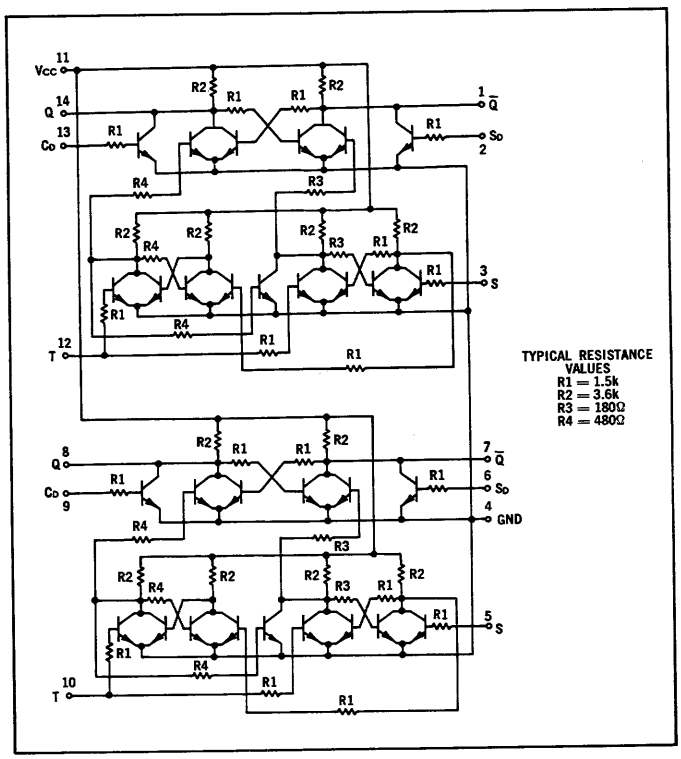
frog = 1 MHz

① Clock (T input) must be high.

② The output state will not change when the input state goes from $S_D = C_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.

③ Direct inputs (S_D and C_D) must be low.

④ The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.



TYPICAL RESISTANCE VALUES
R1 = 1.5k
R2 = 3.6k
R3 = 180Ω
R4 = 480Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

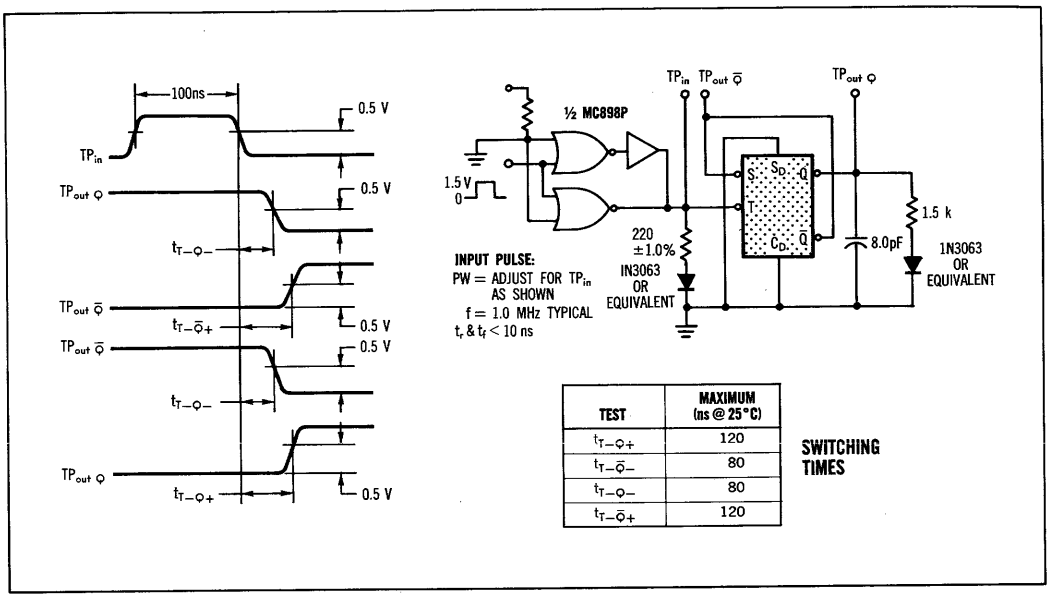
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	KΩ ±1% V_R*
MC878P	0°C	0.880	0.850	1.80	0.500	3.60	0.45	4.3
	+25°C	0.830	0.800	1.80	0.460	3.60	0.40	4.3
	+75°C	0.740	0.710	1.80	0.400	3.60	0.35	4.7
MC778P	+15°C	0.865	0.865	1.80	0.475	3.60	-	4.6
	+25°C	0.850	0.850	1.80	0.460	3.60	-	4.8
	+55°C	0.800	0.800	1.80	0.430	3.60	-	5.0

Characteristic	Symbol	Pin Under Test	MC878P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC778P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	V_R*	Gnd
Input Current	I_{in}	2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	3	12	11	-	12	4, 13
	I_{in}	3	-	150	-	140	-	140		-	150	-	150	-	150		3	-	-	12		-	12	2, 4, 13
	1.8 I_{in}	12	-	270	-	250	-	250		-	270	-	270	-	270		12	-	-	-		-	-	2, 3, 4, 13
	1.8 I_{in}	12	-	270	-	250	-	250		-	270	-	270	-	270		12	-	3	-		-	-	2, 4, 13
	I_{in}	13	-	150	-	140	-	140		-	150	-	150	-	150		13	-	-	12		-	12	2, 3, 4
Output Current	I_{A3}	1	420	-	430	-	395	-	μAdc	420	-	420	-	420	-	μAdc	1	12	3, 13	2	11	-	-	4
		1		-		-		-			-		-		-		1	-	13	2, 12		-	12	3, 4
		14		-		-		-			-		-		-		14	12	2	13		-	-	3, 4
		14		-		-		-			-		-		-		14	3	2	12, 13		-	12	4
Output Voltage	V_{out}	1	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	12, 13	-	11	-	-	3, 4
		1	-		-		-			-		-		-			-	14	12	-		-	-	2, 3, 4, 13
		14	-		-		-			-		-		-			-	13	2, 12	-		-	-	3, 4
		14	-		-		-			-		-		-			-	1	12	-		-	-	2, 3, 4, 13
Saturation Voltage	$V_{CE(sat)}$	1	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	3	13	12	11	-	12	2, 4
		14	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	3, 12	11	-	12	4, 13
Leakage Current	I_L	11	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	μAdc	-	-	-	-	-	11	-	2, 3, 4, 12, 13

* Apply to V_{CC} thru resistor prior to applying V_{off}. Ground inputs of flip-flop not under test. Other pins not listed are left open.

SWITCHING TIMES
TEST CIRCUIT AND WAVEFORMS

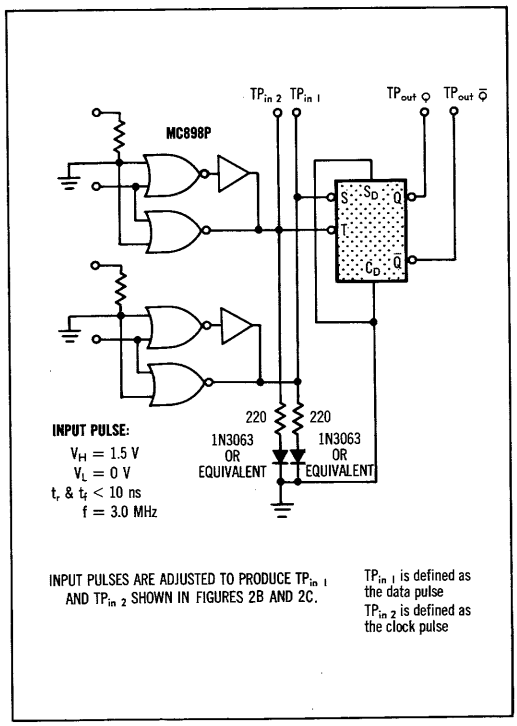
FIGURE 1



TEST	MAXIMUM (ns @ 25°C)
t_{T-Q+}	120
$t_{T-\overline{Q}-}$	80
t_{T-Q-}	80
$t_{T-\overline{Q}+}$	120

SWITCHING TIMES

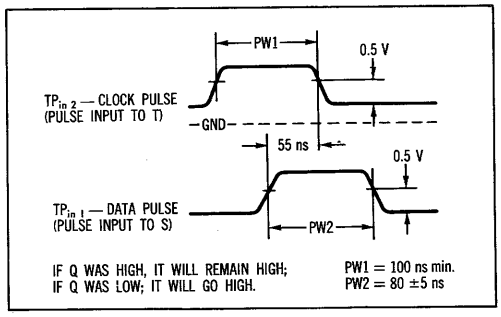
FIGURE 2A — SET-UP AND RELEASE TIMES TEST CIRCUIT



INPUT PULSES ARE ADJUSTED TO PRODUCE TP$_{in\ 1}$ AND TP$_{in\ 2}$ SHOWN IN FIGURES 2B AND 2C.

TP$_{in\ 1}$ is defined as the data pulse
TP$_{in\ 2}$ is defined as the clock pulse

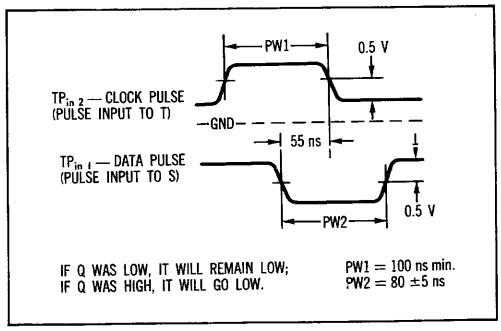
FIGURE 2B — SET-UP TIME WAVEFORMS



IF Q WAS HIGH, IT WILL REMAIN HIGH;
IF Q WAS LOW; IT WILL GO HIGH.

PW1 = 100 ns min.
PW2 = 80 ±5 ns

FIGURE 2C — RELEASE TIME WAVEFORMS



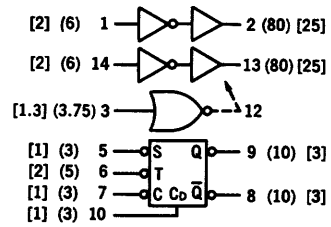
IF Q WAS LOW, IT WILL REMAIN LOW;
IF Q WAS HIGH, IT WILL GO LOW.

PW1 = 100 ns min.
PW2 = 80 ±5 ns

(1 J-K Flip-Flop, 1 Expander, 2 Buffers)

MC779P • MC879P

A medium-power monolithic device consisting of one J-K flip-flop, one expander, and two buffer circuits in a single package. This J-K flip-flop can be operated in the toggling mode. Simultaneous logic ONE pulses applied to the SET and CLEAR terminals cause the output state to reverse. A direct clear input allows asynchronous entry for preclearing counters, inserting parallel data into registers, and other similar applications. The MRTL expander is designed to increase the fan-in capability of gates with expander inputs, and the buffers are high fan-out gates with single inputs.



$2 = \overline{1}$

$12 = \overline{3}$

	f_{Tog} MHz	t_{pd}	P_D(mW) (Inputs High)	P_D(mW) (Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
EXPANDER	—	12	25	Negligible

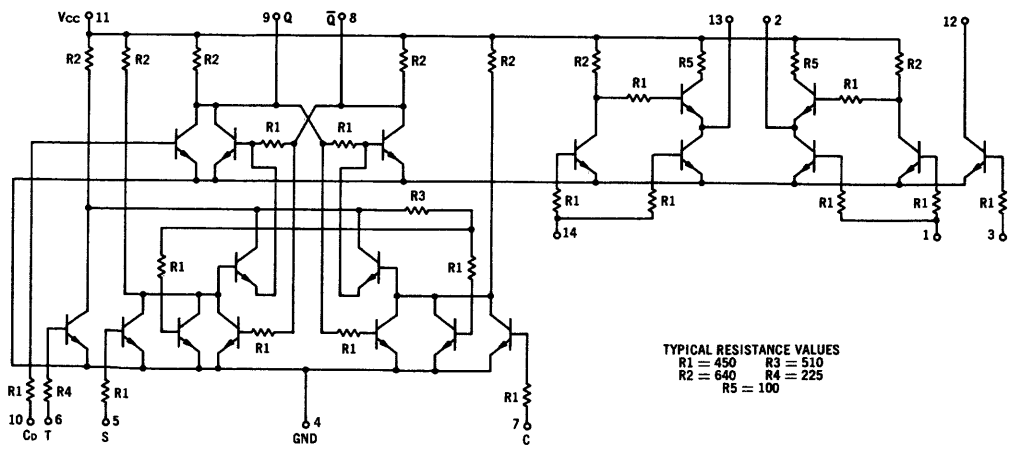
‡Only Clock Input High

CLOCKED INPUT OPERATION ①

t_n ③		t_{n+1} ③	
S	C	Q	$\overline{Q}$
1	1	Q_n ③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n ③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



TYPICAL RESISTANCE VALUES
R1 = 450 R3 = 510
R2 = 640 R4 = 225
R5 = 100

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC879P	0°C	0.960	0.930	1.80	0.570	3.60	640
MC879P	+25°C	0.910	0.880	1.80	0.500	3.60	640
MC879P	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC779P	+15°C	0.865	0.865	1.80	0.475	3.60	640
MC779P	+25°C	0.850	0.850	1.80	0.460	3.60	640
MC779P	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC879P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC779P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2I_{in}$	1	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	1	-	-	-	11	2	3,4,5,6,7,10,14
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	-	-		12	1,4,5,6,7,10,14
	I_{in}	5	-	600	-	600	-	570		-	500	-	500	-	470		5	-	8	-		-	1,3,4,14
	$2I_{in}$	6	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		6	-	5,7	-		-	
	I_{in}	7	-	600	-	600	-	570		-	500	-	500	-	470		7	-	9	-		-	
	I_{in}	10	-	600	-	600	-	570		-	500	-	500	-	470		10	-	8	-		-	
	$2I_{in}$	14	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		14	-	-	-		13	1,3,4,5,6,7,10
Output Current	I_{AB}	2	15.0	-	15.0	-	14.25	-	mAdc	13.50	-	13.75	-	12.50	-	mAdc	-	2	-	1	11	-	3,4,5,6,7,10,14
	I_{A3}	8	1.8	-	1.8	-	1.71	-		1.65	-	1.65	-	1.56	-		-	8	5,10	-		-	1,3,4,14
	I_{A3}	8		-		-		-			-		-		-		-	8,10	5	-		-	
	I_{A3}	9##		-		-		-			-		-		-		-	9	7	10		-	
	I_{A5}	12	3.0	-	3.0	-	2.85	-		2.65	-	2.65	-	2.50	-		-	12	-	3		12	1,4,5,6,7,10,14
	I_{AB}	13	15.0	-	15.0	-	14.25	-		13.50	-	13.75	-	12.50	-		-	13	-	14		-	1,3,4,5,6,7,10
Output Voltage	V_{out}	2	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2	3,4,5,6,7,10,14
		8Δ##	-		-		-			-		-		-			-	5,7	-	-		-	1,3,4,10,14
		8Δ**	-		-		-			-		-		-			-	5	-	7		-	
		8Δ**	-		-		-			-		-		-			-	-	-	5,7		-	
		9	-		-		-			-		-		-			-	10	-	-		-	1,3,4,8,14
		9Δ**	-		-		-			-		-		-			-	5,7	-	-		-	1,3,4,10,14
		9Δ##	-		-		-			-		-		-			-	7	-	5		-	
		9Δ##	-		-		-			-		-		-			-	-	-	5,7		-	
		12	-		-		-			-		-		-			-	3	-	-		12	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	14	-	-		13	1,3,4,5,6,7,10
Saturation Voltage	$V_{CE(sat)}$	2	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	2	3,4,5,6,7,10,14
		8##	-		-		-			-		-		-			-	-	-	10		-	1,3,4,14
		9	-		-		-			-		-		-			-	-	10	-		-	1,3,4,8,14
		9**	-		-		-			-		-		-			-	-	-	-		-	1,3,4,14
		12	-		-		-			-		-		-			-	-	3	-		12	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	-	14	-		13	1,3,4,5,6,7,10
																	Pulse In	Pulse Out					
Switching Time	t	1+2-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	1	2	-	-	11	-	3,4,14
		1-2+	-	-	-	45	-	-		-	-	-	45	-	-		1	2	-	-		-	3,4,14
		14+13-	-	-	-	30	-	-		-	-	-	30	-	-		14	13	-	-		-	1,3,4
		14-13+	-	-	-	45	-	-		-	-	-	45	-	-		14	13	-	-		-	1,3,4

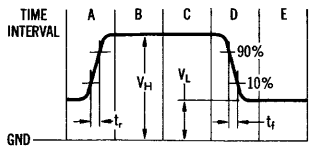
Pins not listed are left open.

Δ = Clock Pulse to pin 6, see Figure 1.

* = Resistor value to V_{CC}.

Pin 8 = LOW
** Pin 9 = LOW
} Set by a momentary ground prior to the application of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

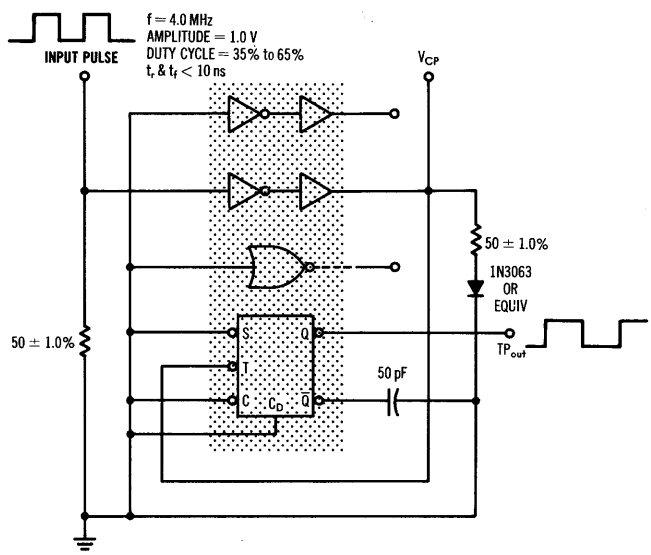
MC879P

T_A	V_L	V_H
+25°C	+0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+75°C	+0.450 V ± 2.0 mV	+0.790 V ± 2.0 mV

MC779P

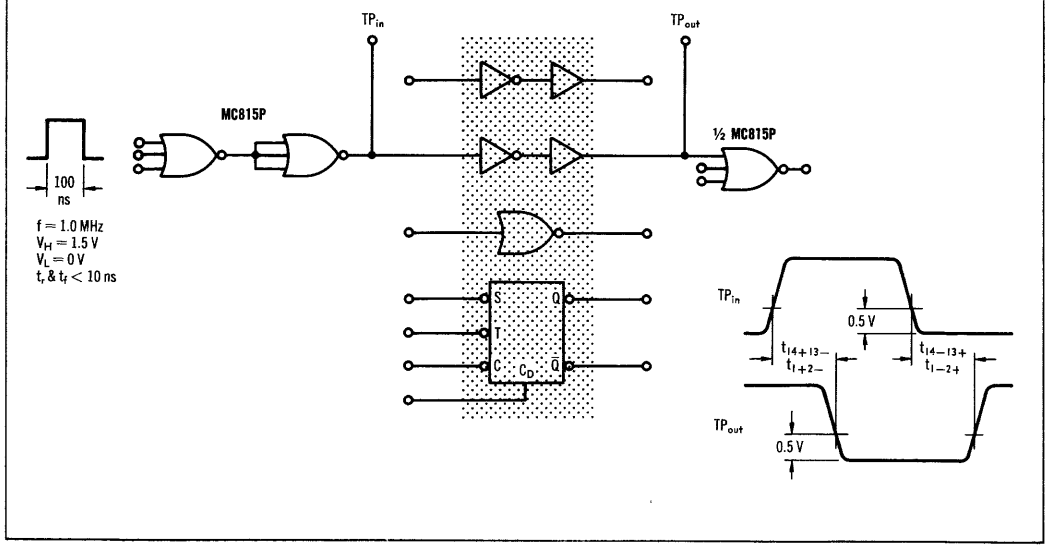
T_A	V_L	V_H
+25°C	−0.460 V ± 2.0 mV	−0.900 V ± 2.0 mV
+15°C	+0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+55°C	+0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



TP_{out} SHOULD HAVE A FREQUENCY OF ½ V_{CP} (2.0 MHz) WHEN THE DUTY CYCLE IS VARIED FROM 35% to 65%.

FIGURE 3 — SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



DECADE UP COUNTER

MC780P • MC880P

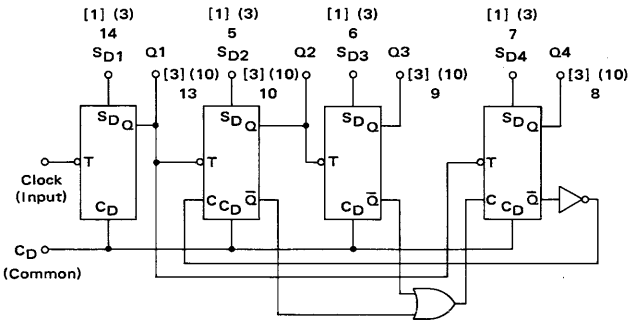
DECODING LOGIC

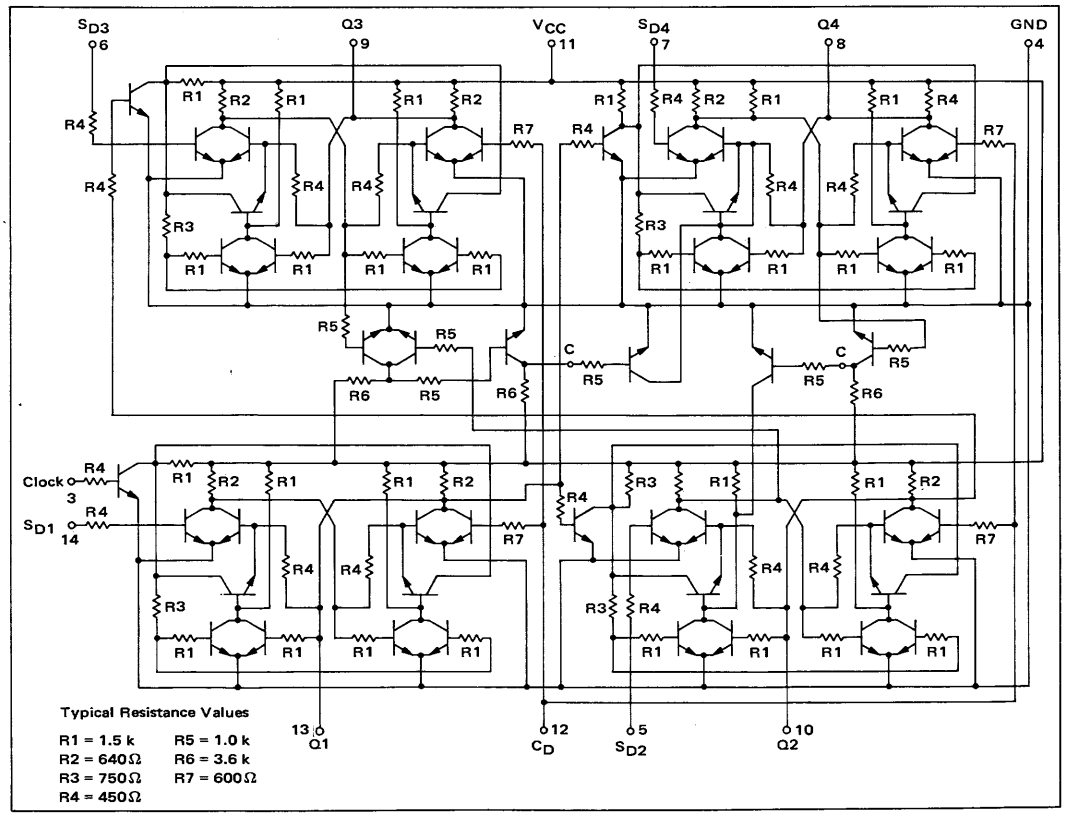
0	$\bar{A}$	$\bar{B}$	$\bar{C}$	$\bar{D}$
1	A	$\bar{B}$	$\bar{C}$	$\bar{D}$
2	$\bar{A}$	B	$\bar{C}$	$\bar{D}$
3	A	B	$\bar{C}$	$\bar{D}$
4	$\bar{A}$	$\bar{B}$	C	$\bar{D}$
5	A	$\bar{B}$	C	$\bar{D}$
6	$\bar{A}$	B	C	$\bar{D}$
7	A	B	C	$\bar{D}$
8	$\bar{A}$	$\bar{B}$	$\bar{C}$	D
9	A	$\bar{B}$	$\bar{C}$	D

P_D = 250 mW typ
f = 4.0 MHz
Counting Frequency

The MC780P/MC880P is a monolithic decade up counter consisting of four flip-flops internally interconnected. A common direct clear is provided to return all outputs to the logical zero level. Individual direct set inputs are provided to set the counter to any specific count.

Number in parenthesis indicates loading factor for mW MRTL.
Number in brackets indicates loading factor for MRTL.





Typical Resistance Values

R1 = 1.5 k	R5 = 1.0 k
R2 = 640Ω	R6 = 3.6 k
R3 = 750Ω	R7 = 600Ω
R4 = 450Ω	

ELECTRICAL CHARACTERISTICS

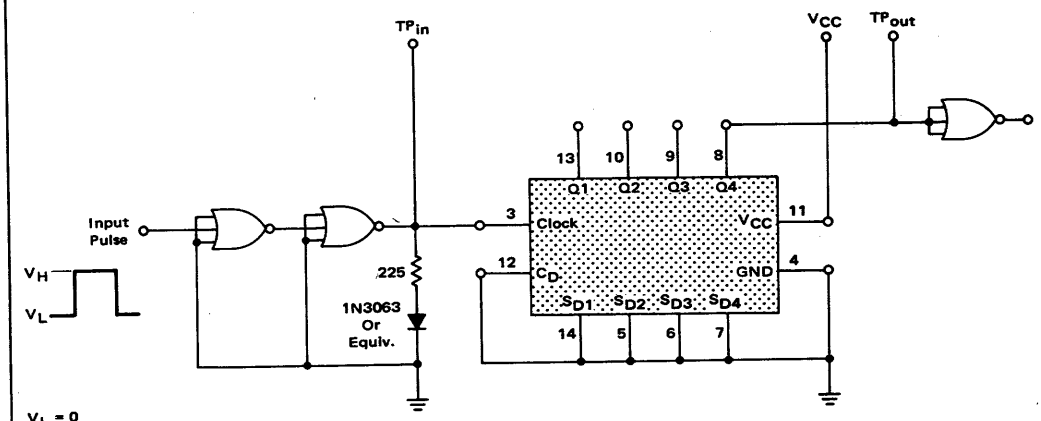
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC880P	0°C	0.960	0.930	1.80	0.570	3.60
MC880P	+25°C	0.910	0.880	1.80	0.500	3.60
MC880P	+75°C	0.820	0.790	1.80	0.450	3.60
MC780P	+15°C	0.865	0.865	1.80	0.475	3.60
MC780P	+25°C	0.850	0.850	1.80	0.460	3.60
MC780P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC880P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC780P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	3	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	3	-	-	-	11	4
		5	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	5	-	-	-	↓	↓
		6	-		-		-			-		-		-			6	-	-	-		
		7	-		-		-			-		-		-			7	-	-	-		
		14	-		-		-			-		-		-			14	-	-	-		
	$3\ I_{in}$	12	-	1800	-	1800	-	710	↓	-	1500	-	1500	-	1410	↓	12	-	-	-	↓	↓
Output Current	I_{A3}	8	-1.80	-	-1.80	-	-1.71	-	mAdc	-1.65	-	-1.65	-	-1.56	-	mAdc	-	8	7	-	11	4
		9	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	9	6	-	↓	↓
		10		-		-		-			-		-		-		-	10	5	-		
		13		-		-		-			-		-		-		-	13	14	-		
Output Voltage	V_{out}*	8	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	-	-	11	4
		9	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	↓
		10	-		-		-			-		-		-			-	-	-	-		
		13	-		-		-			-		-		-			-	-	-	-		
Saturation Voltage	$V_{CE(sat)}$	8	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	12	-	11	4
		9	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	↓	-	↓	↓
		10	-		-		-			-		-		-			-	-		-		
		13	-		-		-			-		-		-			-	-		-		
Power Supply Current Drain	I_{PD}	11	-	-	-	75	-	-	mAdc	-	-	-	75	-	-	mAdc	-	-	-	-	11	4
Switching Times																	Pulse In	Pulse Out				
Propagation Delay	t_{3-8+}	8	-	-	-	100	-	-	ns	-	-	-	100	-	-	ns	3	8	-	-	11	4
	t_{3-8-}	8	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	3	8	-	-	11	4

Pins not listed are left open.

*Apply momentary ground to pin under test prior to measurement of V_{out} on that pin.

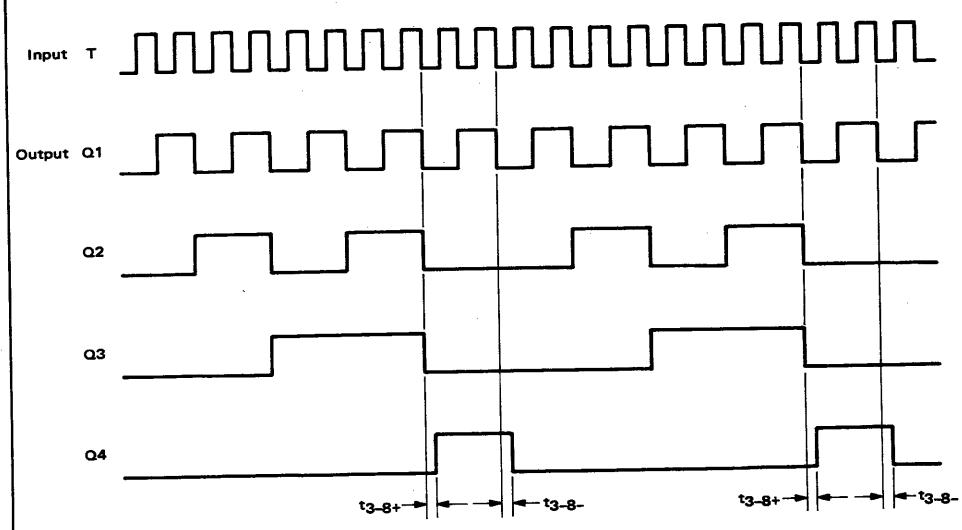
SWITCHING TIME TEST CIRCUIT



V_L = 0
V_H = 1.0 V
Pulse Width = 100 ns
PRF = 1.0 MHz Typ

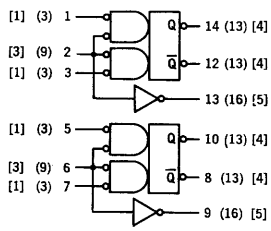
Any MRTL 3-input gates may be used as load and driving gates.

VOLTAGE WAVEFORMS AND DEFINITIONS



MC783P • MC883P

Dual half-shift registers each with built-in inverter, in a single package. Information coming in on pins 1 and 2 will be transferred to pins 14 and 12 when the gating signal, pin 2, goes low. If all three inputs, 1, 2, and 3, are low, the outputs, 12 and 14, will both be low.

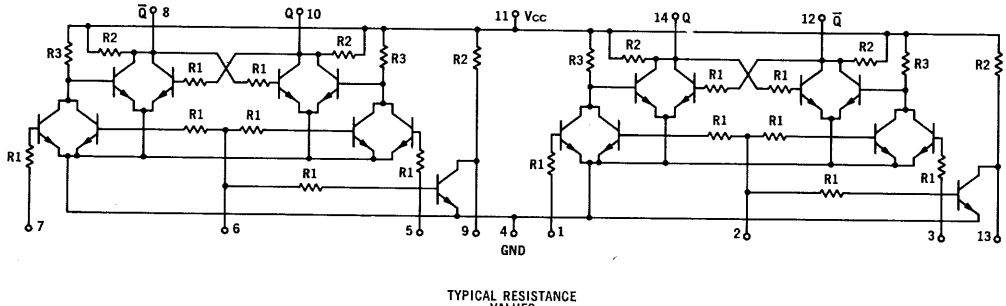


$14 = \overline{12}\,(1 + 2)$
$12 = \overline{14}\,(3 + 2)$

t_{pd} = 22 ns typ
P_D = 140 mW typ

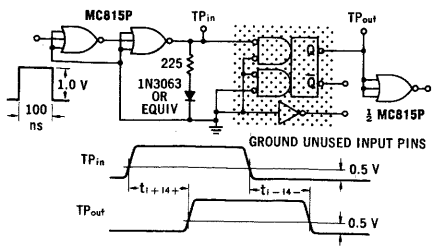
NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL

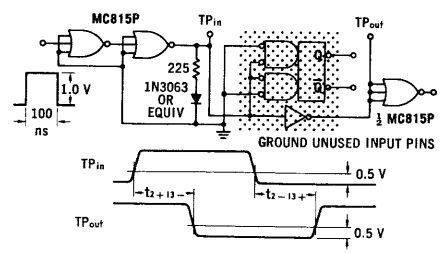
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



TYPICAL RESTRICTION VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-shift register only.
The other half-shift register is tested in the same manner.

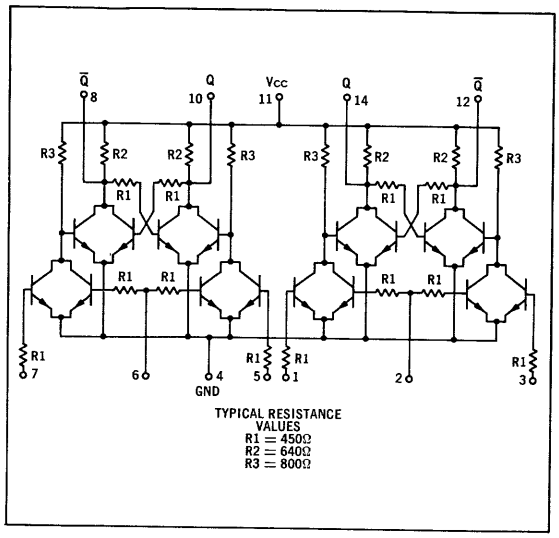
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC883P	0°C	0.960	0.930	1.80	0.570	3.60
MC883P	+25°C	0.910	0.880	1.80	0.500	3.60
MC883P	+75°C	0.820	0.790	1.80	0.450	3.60
MC783P	+15°C	0.865	0.865	1.80	0.475	3.60
MC783P	+25°C	0.850	0.850	1.80	0.460	3.60
MC783P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC883P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC783P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	4
	$3I_{in}$	2	-	1800	-	1800	-	1710		-	1500	-	1500	-	1410		2	-	1, 3	-		
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	2	-		
Output Current	I_{A4}	12	2.4	-	2.4	-	2.28	-	mAdc	2.15	-	2.15	-	2.03	-	mAdc	-	2, 12	-	-	11	4, 14†
	I_{A4}	12	2.4	-	2.4	-	2.28	-		2.15	-	2.15	-	2.03	-		-	3, 12	-	-		4
	I_{A5}	13	3.0	—	3.0	-	2.85	-		2.65	-	2.65	-	2.5	-		-	13	-	2		4
	I_{A4}	14	2.4	-	2.4	-	2.28	-		2.15	-	2.15	-	2.03	-		-	2, 14	-	-		4, 12†
	I_{A4}	14	2.4	-	2.4	-	2.28	-		2.15	-	2.15	-	2.03	-		-	1, 14	-	-		4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	2, 3	-	11	4
		13	-		-		-			-		-		-			-	2	-	-		
		14	-		-		-			-		-		-			-	12	1, 2	-		
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1, 2, 3	-	11	4, 12†
		12	-		-		-			-		-		-			-	-	-	2, 3		4, 14
		13	-		-		-			-		-		-			-	-	2	-		4
		14	-		-		-			-		-		-			-	-	1, 2, 3	-		4, 14†
		14	-		-		-			-		-		-			-	-	-	1, 2		4, 12
Switching Time	t	2+13-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In 2	Pulse Out 13	-	-	11	4
		2-13+	-	-	-	40	-	-		-	-	-	40	-	-		2	13	-	-		4
		1+14+	-	-	-	28	-	-		-	-	-	28	-	-		1	14	-	-		4, 12
		1-14-	-	-	-	24	-	-		-	-	-	24	-	-		1	14	-	-		4, 12

Ground input pins of half-shift register not under test. Other pins not listed are left open.

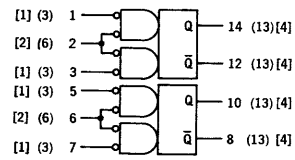
†Silicon diode to ground.

MC784P • MC884P



TYPICAL RESISTANCE VALUES
R1 = 450Ω
R2 = 640Ω
R3 = 800Ω

Two half-shift registers in a single package. Each is a bistable storage element. E.g., information coming in on pins 1 and 3 will be transferred to pins 14 and 12 when the gating signal, pin 2, goes low. If all three inputs, 1, 2, and 3, are low, the outputs, 14 and 12, will both be low.

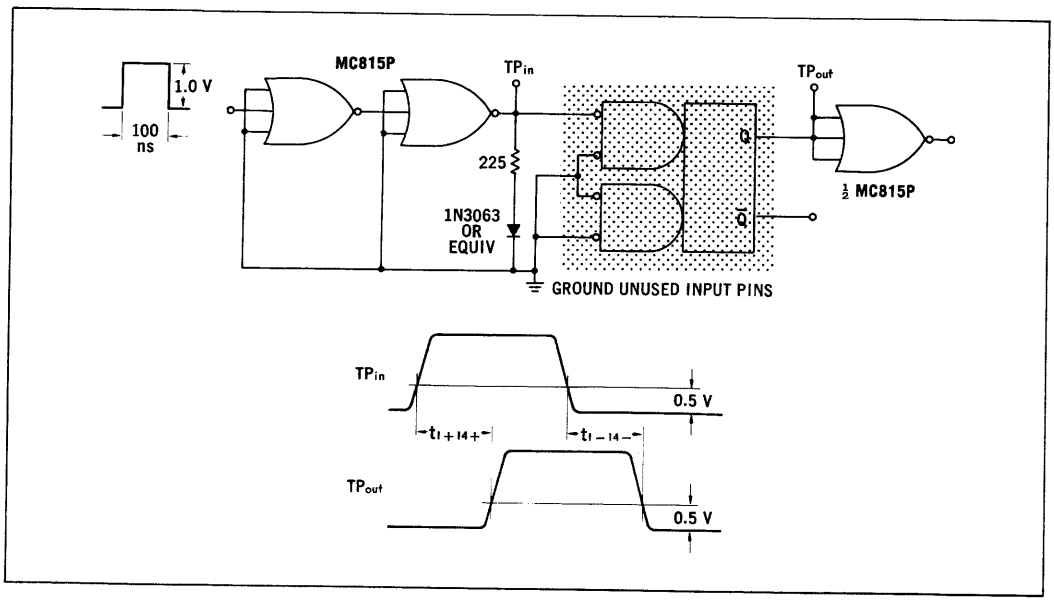


NUMBER IN PARENTHESIS INDICATES mW MRTL LOADING FACTOR

NUMBER IN BRACKETS INDICATES MRTL LOADING FACTOR

t_{pd} = 22 ns typ
P_D = 120 mW typ

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-shift register only.
The other half-shift register is tested in the same manner.

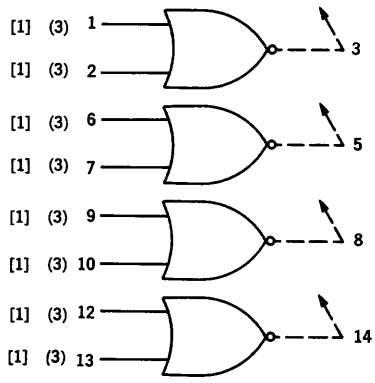
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC884P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC784P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC884P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC784P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	4
	$2I_{in}$	2	-	1200	-	1200	-	1140	↓	-	1000	-	1000	-	940	↓	2	-	1, 3	-	↓	↓
	I_{in}	3	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	3	-	2	-	↓	↓
Output Current	I_{A4}	12	2.4	-	2.4	-	2.28	-	mAdc	2.15	-	2.15	-	2.03	-	mAdc	-	2, 12	-	-	11	4, 14†
		12	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3, 12	-	-	↓	4
		14		-		-		-			-		-		-		-	2, 14	-	-		4, 12†
		14		-		-		-			-		-		-		-	1, 14	-	-		4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	2, 3	-	11	4
		14	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	12	1, 2	-	11	4
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1, 2, 3	-	11	4, 12†
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	2, 3	↓	4, 14
		14	-		-		-			-		-		-			-	-	1, 2, 3	-		4, 14†
		14	-		-		-			-		-		-			-	-	-	1, 2		4
Switching Time	t	1+14+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In 1	Pulse Out 14	-	-	11	4, 12
		1-14-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	14	-	-	11	4, 12

Ground input pins of half-register not under test. Other pins not listed are left open. †Silicon diode to ground.

MC785P • MC885P

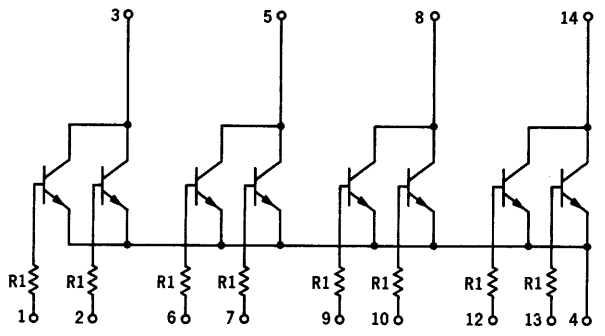
Four 2-input expanders housed in a single package increase the input capability of MRTL gates.



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL
SEE GENERAL INFORMATION SECTION FOR EXPANDER RULES



V_{CC} CONNECTION TO PIN 11 IS NOT SHOWN

TYPICAL RESISTANCE VALUES
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

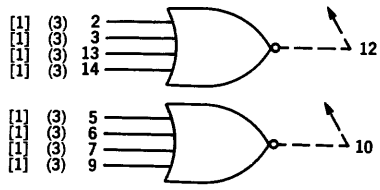
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC885P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC785P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC885P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC785P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	3	4
		2	-	600	—	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	1	-	11	3	4
Output Leakage Current	I_{CEX}	3	-	200	-	200	-	250	μAdc	-	225	-	225	-	250	μAdc	3	-	-	1, 2	11	-	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	3	2, 4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	3	1, 4
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	3	2, 4
		3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	2	-	11	3	1, 4

Ground unused input pins. Other pins not listed are left open. * Resistor value to V_{CC}

MC786P • MC886P

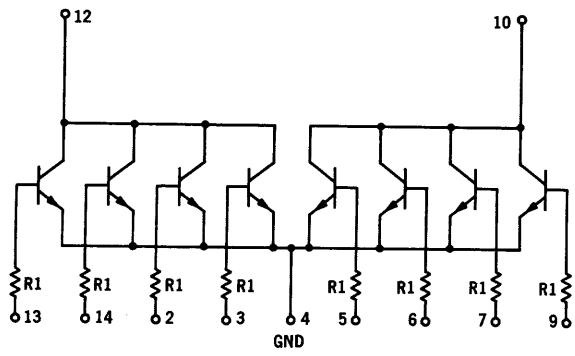
Two 4-input gate expanders housed in a single package. Each may be used independently or combined. Each expander increases the input capability of a standard MRTL gate by four.



$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL
SEE GENERAL INFORMATION SECTION FOR EXPANDER RULES



V_{CC} CONNECTION TO PIN 11 NOT SHOWN

TYPICAL RESISTANCE VALUES
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expander is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC886P	0°C	0.960	0.930	1.80	0.570	3.60	640
MC886P	+25°C	0.910	0.880	1.80	0.500	3.60	640
MC886P	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC786P	+15°C	0.865	0.865	1.80	0.475	3.60	640
MC786P	+25°C	0.850	0.850	1.80	0.460	3.60	640
MC786P	+55°C	0.800	0.800	1.80	0.430	3.60	640

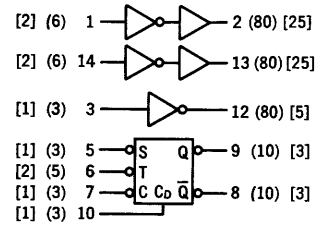
Characteristic	Symbol	Pin Under Test	MC886P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC786P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	3,13,14	-	11	12	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,13,14	-	↓	↓	↓
		13	-		-		-			-		-		-			13	-	2,3,14	-			
		14	-		-		-			-		-		-			14	-	2,3,13	-			
Output Leakage Current	I_{CEX}	12	-	200	-	200	-	250	μAdc	-	225	-	225	-	250	μAdc	12	-	-	2, 3, 13, 14	11	-	4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	12	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	↓	2,3,4,13
		12	-		-		-			-		-		-			-	2	-	-			3,4,13,14
		12	-		-		-			-		-		-			-	3	-	-			2,4,13,14
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	13	-	11	12	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	↓	2,3,4,13
		12	-		-		-			-		-		-			-	-	2	-			3,4,13,14
		12	-		-		-			-		-		-			-	-	3	-			2,4,13,14

Ground unused input pins. Other pins not listed are left open.

(1 J-K Flip-Flop, 1 Inverter, 2 Buffers)

MC787P • MC887P

A medium-power monolithic device consisting of one J-K flip-flop, one inverter, and two buffer circuits in a single package. This J-K flip-flop can be operated in the toggling mode. Simultaneous logic ONE pulses applied to the SET and CLEAR terminals cause the output state to reverse. A direct clear input allows asynchronous entry for pre-clearing counters, inserting parallel data into registers, and other similar applications. The inverter is a basic MRTL gate and the buffers are high fan-out gates with single inputs.



$2 = \overline{1}$

$12 = \overline{3}$

CLOCKED INPUT OPERATION ①

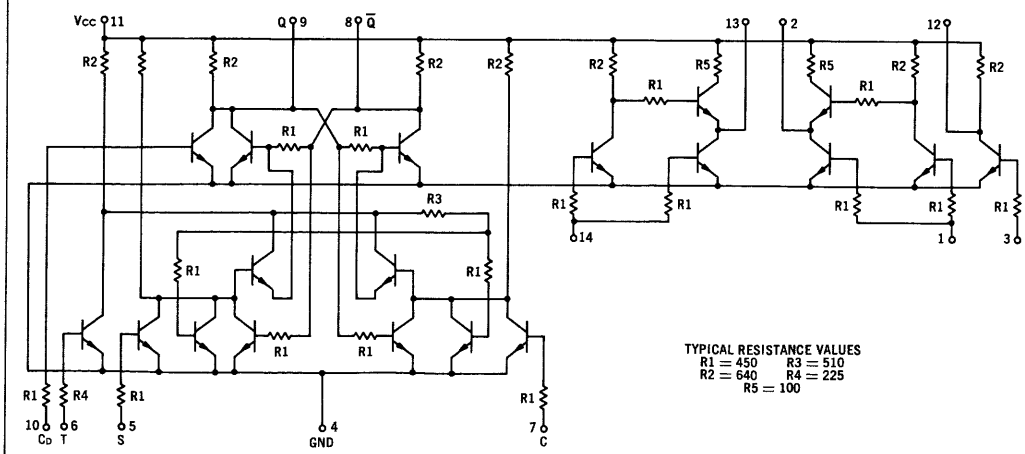
t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

	f_{Toq} MHz	t_{pd} ns	P_D (mW) (Input High)	P_D (mW) (Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
INVERTER	—	12	22	8

‡Only Clock Input High

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESES INDICATES mW MRTL LOADING FACTOR
NUMBER IN BRACKETS INDICATES MRTL LOADING FACTOR



TYPICAL RESISTANCE VALUES
R1 = 450 R3 = 510
R2 = 640 R4 = 225
R5 = 100

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC887P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC787P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC887P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC787P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2I_{in}$	1	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	1	-	-	-	11	2	3,4,5,6,7,10,14
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	-	-		-	1,4,5,6,7,10,14
	I_{in}	5	-	600	-	600	-	570		-	500	-	500	-	470		5	-	8	-		-	1,3,4,14
	$2I_{in}$	6	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		6	-	5,7	-		-	
	I_{in}	7	-	600	-	600	-	570		-	500	-	500	-	470		7	-	9	-		-	
	I_{in}	10	-	600	-	600	-	570		-	500	-	500	-	470		10	-	8	-		-	
	$2I_{in}$	14	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		14	-	-	-		13	1,3,4,5,6,7,10
Output Current	I_{AB}	2	15.0	-	15.0	-	14.25	-	mAdc	13.50	-	13.75	-	12.50	-	mAdc	-	2	-	1	11	-	3,4,5,6,7,10,14
	I_{A3}	8	1.8	-	1.8	-	1.71	-		1.65	-	1.65	-	1.56	-		-	8	5,10	-		-	1,3,4,14
	I_{A3}	8		-		-		-			-		-		-		-	8,10	5	-		-	
	I_{A3}	9##		-		-		-			-		-		-		-	9	7	10		-	
	I_{A5}	12	3.0	-	3.0	-	2.85	-		2.65	-	2.65	-	2.50	-		-	12	-	3		-	1,4,5,6,7,10,14
	I_{AB}	13	15.0	-	15.0	-	14.25	-		13.50	-	13.75	-	12.50	-		-	13	-	14		-	1,3,4,5,6,7,10
Output Voltage	V_{out}	2	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2	3,4,5,6,7,10,14
		8Δ##	-		-		-			-		-		-			-	5,7	-	-		-	1,3,4,10,14
		8Δ**	-		-		-			-		-		-			-	5	-	7		-	
		8Δ**	-		-		-			-		-		-			-	-	-	5,7		-	
		9	-		-		-			-		-		-			-	10	-	-		-	1,3,4,8,14
		9Δ**	-		-		-			-		-		-			-	5,7	-	-		-	1,3,4,10,14
		9Δ##	-		-		-			-		-		-			-	7	-	5		-	
		9Δ##	-		-		-			-		-		-			-	-	-	5,7		-	
		12	-		-		-			-		-		-			-	3	-	-		-	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	14	-	-		13	1,3,4,5,6,7,10
Saturation Voltage	$V_{CE(sat)}$	2	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	2	3,4,5,6,7,10,14
		8##	-		-		-			-		-		-			-	-	-	10		-	1,3,4,14
		9	-		-		-			-		-		-			-	-	10	-		-	1,3,4,8,14
		9**	-		-		-			-		-		-			-	-	-	-		-	1,3,4,14
		12	-		-		-			-		-		-			-	-	3	-		-	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	-	14	-		13	1,3,4,5,6,7,10
																	Pulse In	Pulse Out					
Switching Time	t	1+2-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	1	2	-	-	11	-	3,4,14
		1-2+	-	-	-	45	-	-		-	-	-	45	-	-		1	2	-	-		-	3,4,14
		14+13-	-	-	-	30	-	-		-	-	-	30	-	-		14	13	-	-		-	1,3,4
		14-13+	-	-	-	45	-	-		-	-	-	45	-	-		14	13	-	-		-	1,3,4

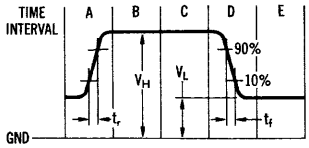
Pins not listed are left open.

Δ = Clock Pulse to pin 6, see Figure 1.

* Resistor value to V_{CC}

Pin 8 = LOW
** Pin 9 = LOW
} Set by a momentary ground prior to the application of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

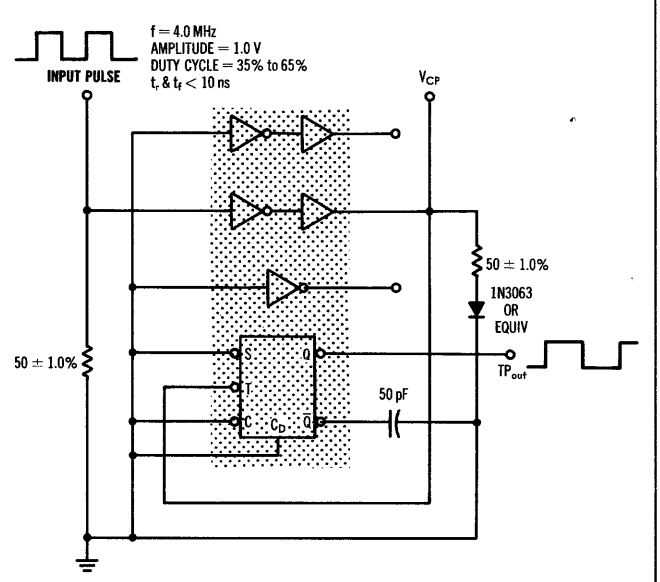
MC887P

T_A	V_L	V_H
+ 25°C	+ 0.500 V ± 2.0 mV	+ 0.930 V ± 2.0 mV
0°C	+ 0.570 V ± 2.0 mV	+ 0.980 V ± 2.0 mV
+ 75°C	+ 0.450 V ± 2.0 mV	+ 0.790 V ± 2.0 mV

MC787P

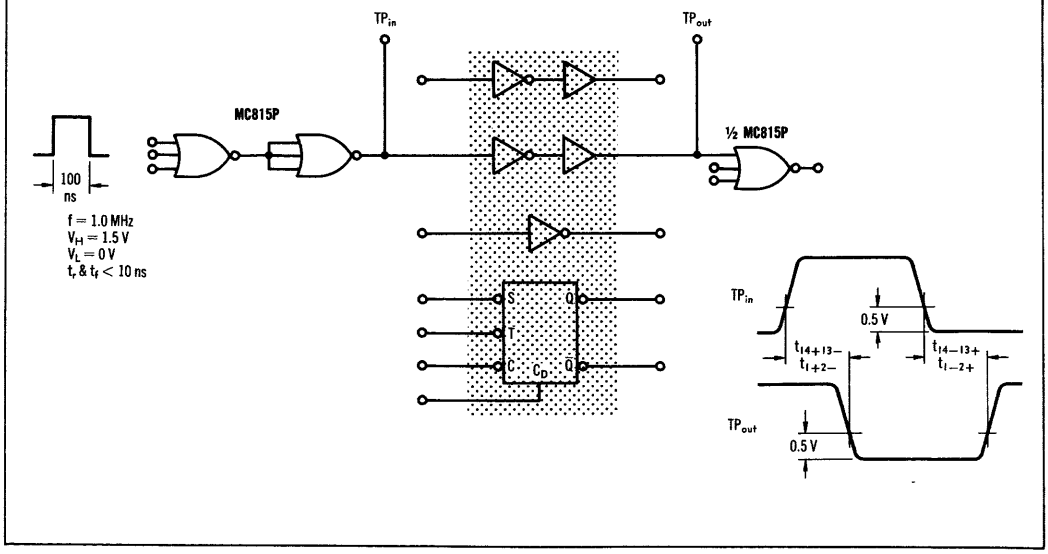
T_A	V_L	V_H
+ 25°C	−0.460 V ± 2.0 mV	−0.900 V ± 2.0 mV
+ 15°C	+0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+ 55°C	+0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT

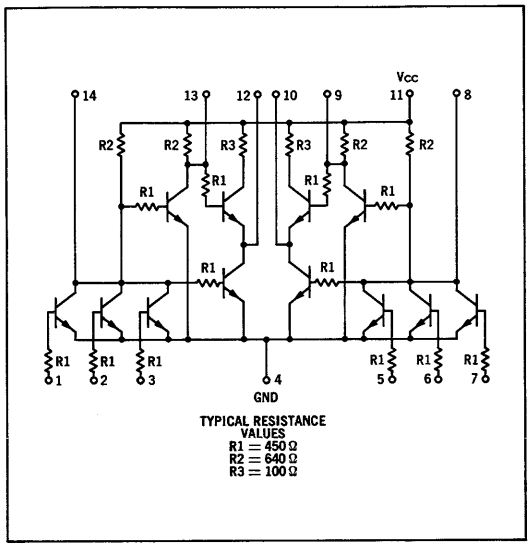


TP_{out} SHOULD HAVE A FREQUENCY OF ½ V_{CP} (2.0 MHz) WHEN THE DUTY CYCLE IS VARIED FROM 35% to 65%.

FIGURE 3 — SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

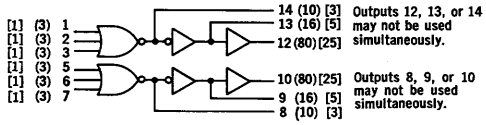


MC788P • MC888P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω

Two 3-input positive logic NOR gates, each followed by an inverting and non-inverting high fan-out amplifier, are provided in a single package. For each section, the output from each stage is available. If more than one output is used, the full loading factors cannot be employed since each output provides the drive for the succeeding stage.

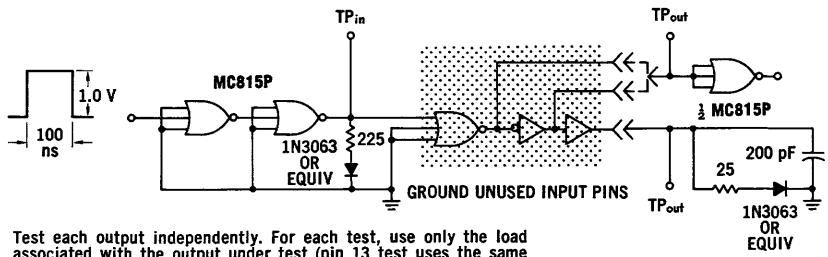


$14 = \overline{1+2+3}$ $\quad 13 = 1+2+3$ $\quad 12 = 1+2+3$

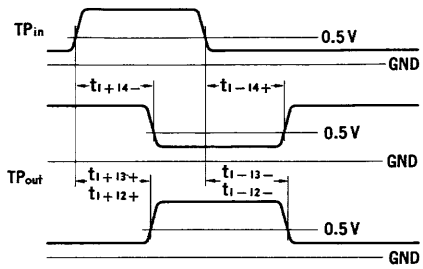
NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

t_{pd} = 24 ns
P_D = 145 mW (Input Low)
56 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test (pin 13 test uses the same load as pin 14 test). Outputs not under test should be left open.



ELECTRICAL CHARACTERISTICS

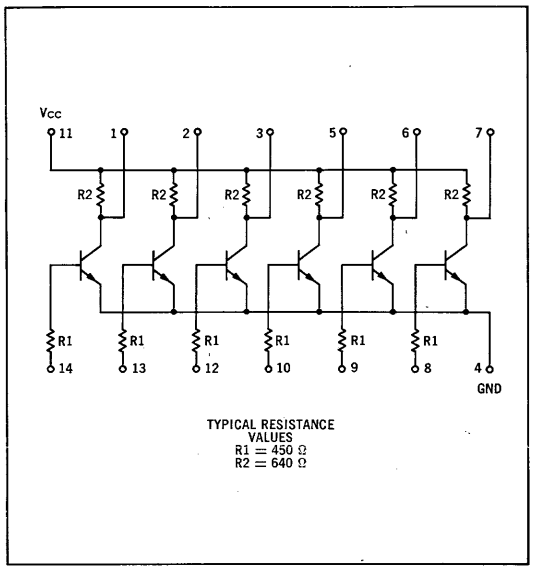
Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC888P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC788P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC888P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC788P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2, 3	-	11	-	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1, 3	-	↓	-	↓
		3	-		-		-			-		-		-			3	-	1, 2	-		-	
Output Current	I_{AB}	12	15.0	-	15.0	-	14.25	-	mAdc	13.50	-	13.75	-	12.50	-	mAdc	-	12	-	14	11	-	4
	I_{A5}	13	3.0	-	3.0	-	2.85	-		2.65	-	2.65	-	2.50	-	mAdc	-	13	-	14	↓	-	↓
	I_{A3}	14	1.8	-	1.8	-	1.71	-	↓	-	-	-	-	-	-	-	-	14	-	1, 2, 3		-	
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	12	1,2,3,4
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	-	1,2,3,4
		14	-		-		-			-		-		-			-	1	-	-		-	2,3,4
		14	-		-		-			-		-		-			-	2	-	-		-	1,3,4
		14	-		-		-			-		-		-			-	3	-	-		-	1,2,4
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	12	1,2,3,4
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	-	1,2,3,4
		14	-		—		-			-		-		-			-	-	1	-		-	2,3,4
		14	-		-		-			-		-		-			-	-	2	-		-	1,3,4
		14	-		-		-			-		-		-			-	-	3	-		-	1,2,4
																	Pulse In	Pulse Out					
Switching Time	t	1+12+	-	-	-	65	-	-	-	-	-	-	65	-	-	-	1	12	-	-	11	-	2,3,4
		1-12-	-	-	-	58	-	-	-	-	-	-	58	-	-	-	1	12	-	-	↓	-	↓
		1+13+	-	-	-	42.5	-	-	-	-	-	-	42.5	-	-	-	1	13	-	-		-	
		1-13-	-	-	-	42.5	-	-	-	-	-	-	42.5	-	-	-	1	13	-	-		-	
		1+14-	-	-	-	20	-	-	-	-	-	-	20	-	-	-	1	14	-	-		-	
		1-14+	-	-	-	28	-	-	-	-	-	-	28	-	-	-	1	14	-	-	↓	-	↓

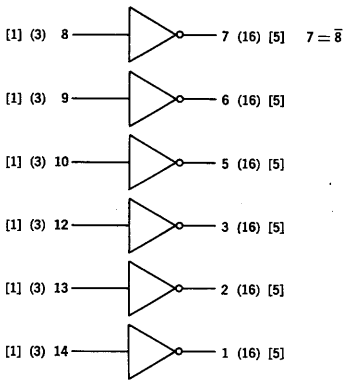
Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

MC789P • MC889P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

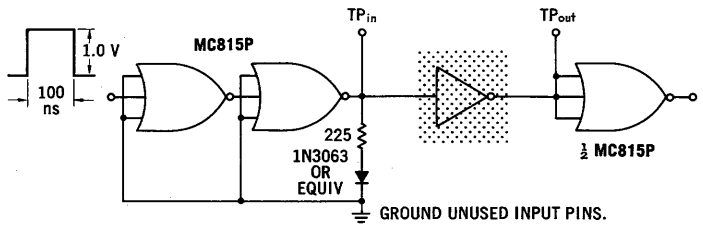
Six individual circuits are contained in a single package. Each provides the simple inversion function.

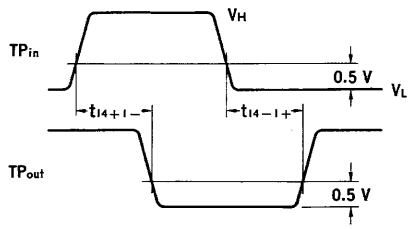


NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

t_{pd} = 12 ns
P_D = 130 mW (Input High)
15 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.
The other inverters are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC889P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC789P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

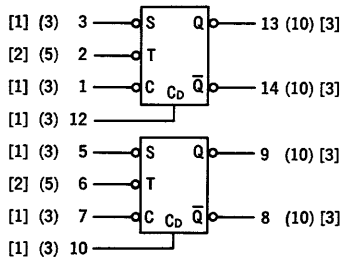
Characteristic	Symbol	Pin Under Test	MC889P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC789P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	14*	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	14	-	*	-	11	4
Output Current	I_{A5}	1	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	1	-	-	14	11	4
Output Voltage	V_{out}	1	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	4
Saturation Voltage	$V_{CE(sat)}$	1	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	4
Switching Time	$t_{on} + t_{off}$	1, 14	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In: 14	Pulse Out: 1	-	-	11	4

Ground inputs of inverters not under test. Other pins not listed are left open

* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V_{BOT}.

MC790P • MC890P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



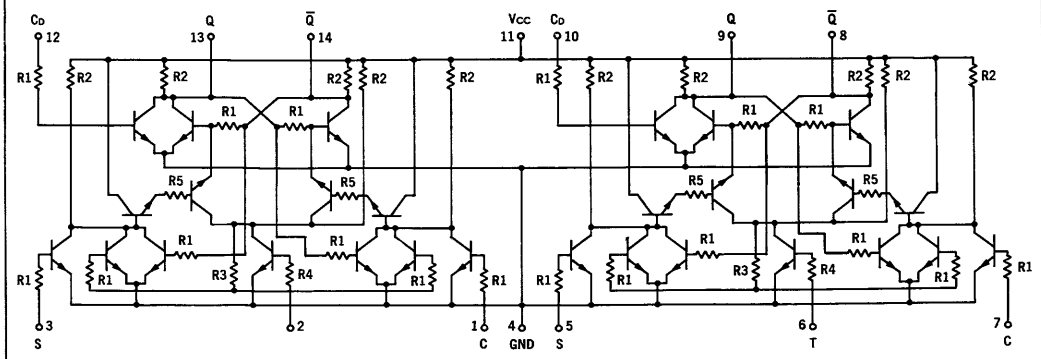
f_{Tog} = 4 MHz
P_D = 182 mW (Only Clock Input High)
158 (Inputs Low)

CLOCKED INPUT OPERATION ①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



TYPICAL RESISTANCE VALUES
R1 = 450 Ω R3 = 510 Ω
R2 = 640 Ω R4 = 225 Ω
R5 = 300 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC890P	0°C	0.960	0.930	1.80	0.570	3.60
MC890P	+25°C	0.910	0.880	1.80	0.500	3.60
MC890P	+75°C	0.820	0.790	1.80	0.450	3.60
MC790P	+15°C	0.865	0.865	1.80	0.475	3.60
MC790P	+25°C	0.850	0.850	1.80	0.460	3.60
MC790P	+55°C	0.800	0.800	1.80	0.430	3.60

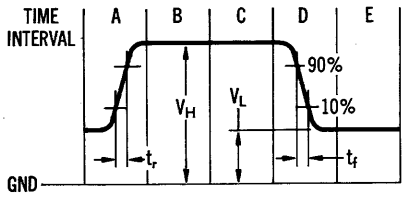
Characteristic	Symbol	Pin Under Test	MC890P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC790P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	13	-	11	2, 3, 4, 12
	$2I_{in}$	2	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		2	-	1, 3	-		4, 12
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	14	-		1, 2, 4, 12
	I_{in}	12	-	600	-	600	-	570		-	500	-	500	-	470		12	-	14	-		1, 2, 3, 4
Output Current	I_{A3}	13	1.80	-	1.80	-	1.71	-	mAdc	1.65	-	1.65	-	1.56	-	mAdc	-	13	1	12	11	2, 3, 4
		14		-		-		-			-		-		-		-	14	3, 12	-		1, 2, 4
		14		-		-		-			-		-		-		-	12, 14	3	-		1, 2, 4
Output Voltage	V_{out}	13	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	11	1,2,3,4,14
		13*#	-		-		-			-		-		-			-	1, 3	-	-		4, 12
		13*##	-		-		-			-		-		-			-	1	-	3		
		13*##	-		-		-			-		-		-			-	-	-	1, 3		
		14*##	-		-		-			-		-		-			-	1, 3	-	-		
		14*#	-		-		-			-		-		-			-	3	-	1		
		14*#	-		-		-			-		-		-			-	-	-	1, 3		
Saturation Voltage	$V_{CE(sat)}$	13	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	12	-	11	1,2,3,4,14
		13#	-		-		-			-		-		-			-	-	-	-		1,2,3,4,12
		14##	-		-		-			-		-		-			-	-	12	-		1,2,3,4

Ground unused input pins. Other pins not listed are left open.

* Clock pulse to pin 2, see Figure 1,

Pin 13 = LOW
Pin 14 = LOW
} Set by a momentary ground prior to the application of the negative-going Clock Pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

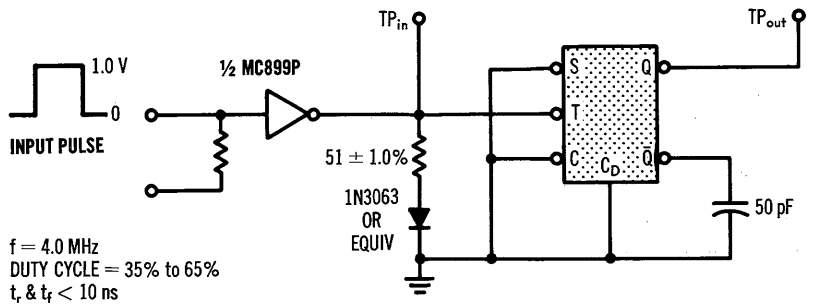
MC890P

T_A	V_L	V_H
+ 25°C	+0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+ 75°C	+0.450 V ± 2.0 mV	+0.840 V ± 2.0 mV

MC790P

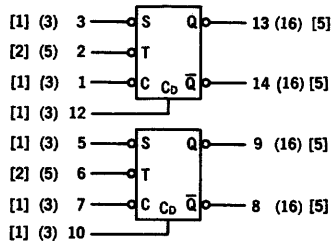
T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC791P • MC891P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



$f_{Tog} = 4$ MHz
$t_{pd} = 40$ ns typ

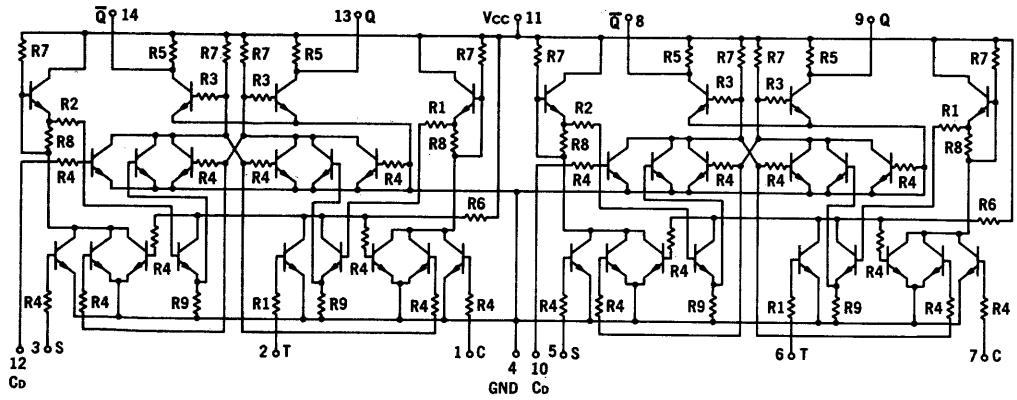
$P_D = 190$ mW typ (Only Clock Input High)
160 mW typ (Inputs Low)

CLOCKED INPUT OPERATION ①

t_n ②		t_{n+1} ③	
S	C	Q	$\overline{Q}$
1	1	Q_n ③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n ③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



TYPICAL RESISTANCE VALUES
R1 = 300 Ω R4 = 600 Ω R7 = 900 Ω
R2 = 500 Ω R5 = 640 Ω R8 = 2.0 k
R3 = 550 Ω R6 = 700 Ω R9 = 3.0 k

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC891P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC791P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC891P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC791P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1†	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	-	-	11	4
	$2I_{in}$	2	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		2	-	1, 3	-		
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	12	-		
	I_{in}	12	-	600	-	600	-	570		-	500	-	500	-	470		12	-	-	-		
Output Current	I_{A5}	13†	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	13	-	-	11	-
		14	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	12, 14	-	-	11	4
Output Voltage	V_{out}	13 § ⑤	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	4, 12
		13§§④	-		-		-			-		-		-			-	-	-	3		
		13 § ⑥	-		-		-			-		-		-			-	1	-	-		
		13§§⑦	-		-		-			-		-		-			-	-	-	3		
		14 § ④	-		-		-			-		-		-			-	-	-	1		
		14§§⑤	-		-		-			-		-		-			-	3	-	-		
		14 § ⑦	-		-		-			-		-		-			-	-	-	1		
		14§§⑥	-		-		-			-		-		-			-	3	-	-		
Saturation Voltage	$V_{CE(sat)}$	13†	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	12	-	-	11	4
		13*#	-		-		-			-		-		-			-	1, 3	-	-		
		13†*	-		-		-			-		-		-			-	1	-	3		
		13†*	-		-		-			-		-		-			-	-	-	1, 3		
		14*#	-		-		-			-		-		-			-	3	-	1		
		14*#	-		-		-			-		-		-			-	-	-	1, 3		
		14†*	-		-		-			-		-		-			-	1, 3	-	-		

Ground inputs of flip-flop not under test. Other pins not listed are left open.

† Preset the flip-flop by the following procedure:
(1) Momentarily apply V_{BOT} to pin 12 to preclear flip-flop.
(2) After V_{BOT} is removed from pin 12, ground pins 1 and 3.
(3) Apply a negative-going clock pulse to pin 2 (see note*) while pins 1 and 3 are still grounded. This changes the state of the flip-flop to the SET condition.
(4) Remove grounds from pins 1 and 3, and proceed with the test.

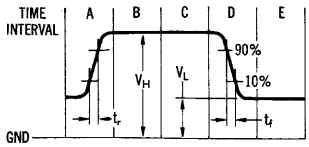
* Clock pulse to pin 2, see Figure 1.

Pin 12 = HIGH — Set by momentary application of V_{BOT} prior to the application of the negative-going clock pulse.

§ = Clock pulse to pin 2, data pulse to pin 3.
§§ = Clock pulse to pin 2, data pulse to pin 1.

④ = See Figure 4.
⑤ = See Figure 5.
⑥ = See Figure 6.
⑦ = See Figure 7.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC891P

T_A	V_L	V_H
+ 25°C	+ 0.500 V ± 2.0 mV	+ 0.930 V ± 2.0 mV
0°C	+ 0.570 V ± 2.0 mV	+ 0.980 V ± 2.0 mV
+ 75°C	+ 0.450 V ± 2.0 mV	+ 0.790 V ± 2.0 mV

MC791P

T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+ 0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+ 0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+ 0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT

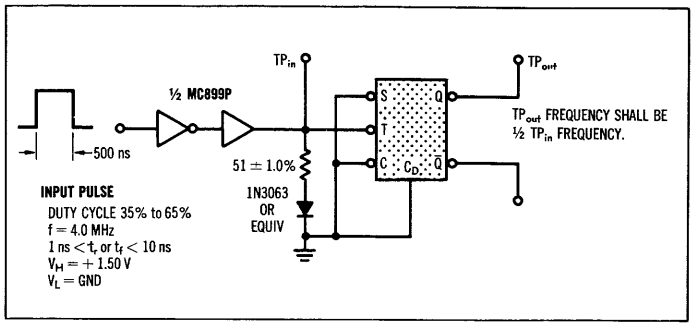


FIGURE 3 — TEST CIRCUIT

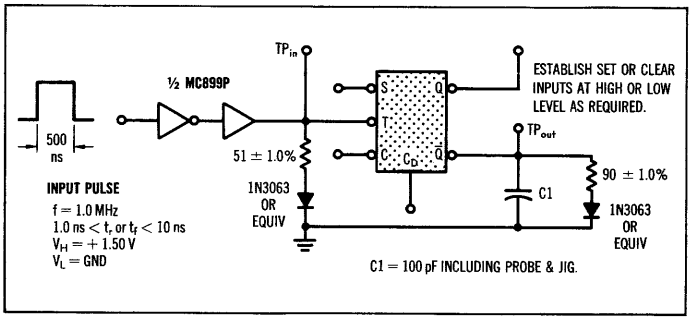


FIGURE 4 — TEST WAVEFORMS

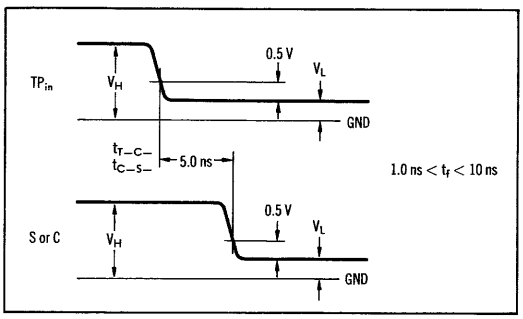


FIGURE 5 — TEST WAVEFORMS

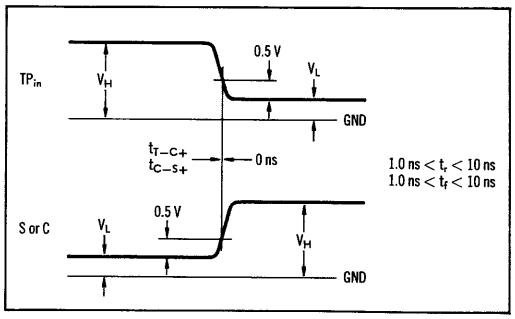


FIGURE 6 — TEST WAVEFORMS

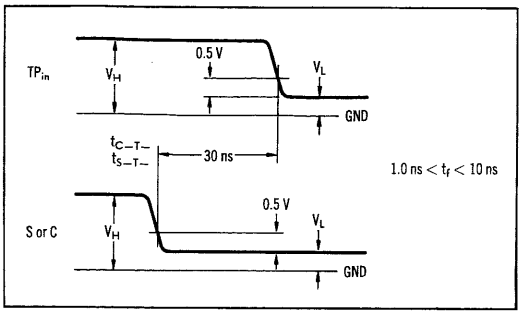
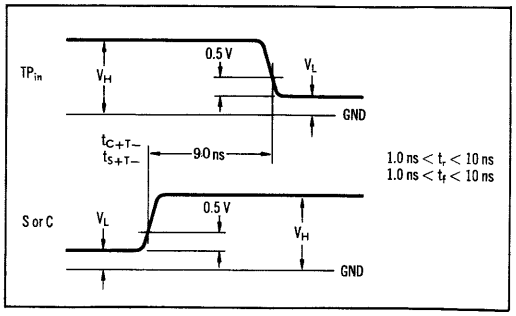
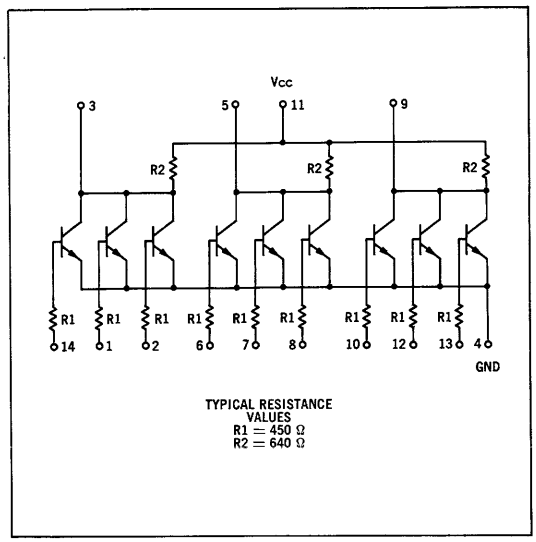


FIGURE 7 — TEST WAVEFORMS

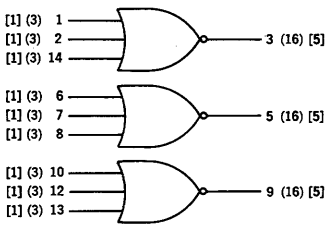


MC792P • MC892P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

Three 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



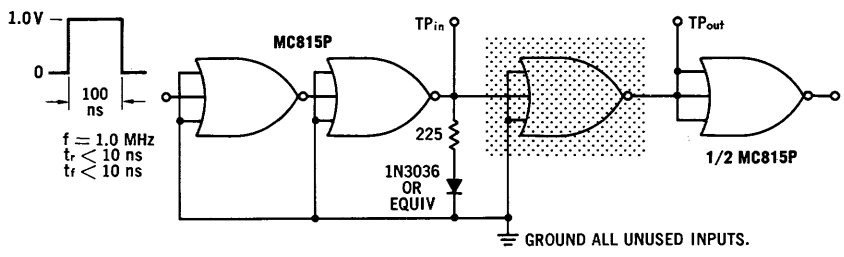
$3 = \overline{1 + 2 + 14}$

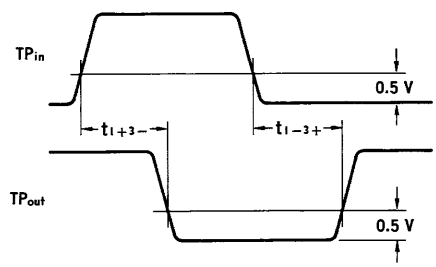
NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL

NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

t_{pd} = 12 ns
P_D = 82 mW (Input High)
24 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

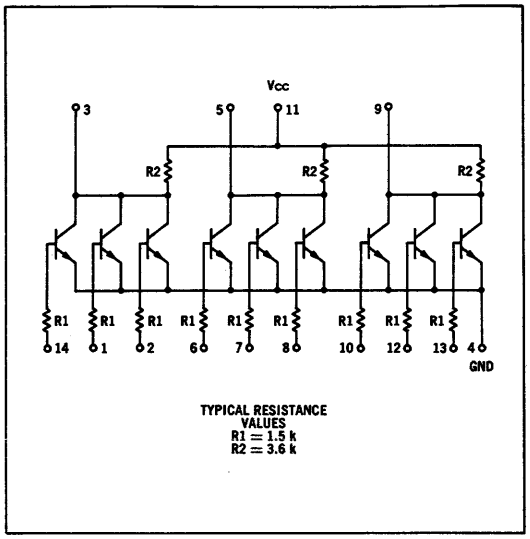
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC892P	0°C	0.960	0.930	1.80	0.570	3.60
MC892P	+25°C	0.910	0.880	1.80	0.500	3.60
MC892P	+75°C	0.820	0.790	1.80	0.450	3.60
MC792P	+15°C	0.865	0.865	1.80	0.475	3.60
MC792P	+25°C	0.850	0.850	1.80	0.460	3.60
MC792P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC892P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC792P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2, 14	-	11	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1, 14	-	↓	↓
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	14	-	1, 2	-	↓	↓
Output Current	I_{A5}	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	1, 2, 14	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	2,4,14
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	1,4,14
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1	-	↓	2,4,14
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2	-	↓	1,4,14
Switching Time	$t_{on} + t_{off}$	1, 3	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In: 1	Pulse Out: 3	-	- -	11	2,4,14

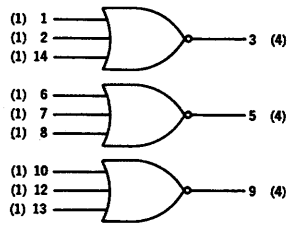
Ground input pins of gates not under test. Other pins not listed are left open.

MC793P • MC893P



TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k

Three 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.

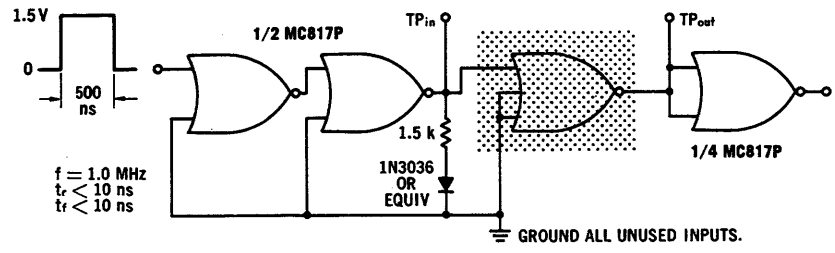


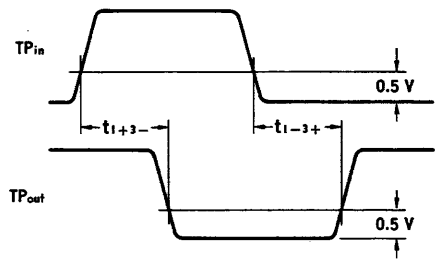
$3 = \overline{1 + 2 + 14}$

NUMBER IN PARENTHESES INDICATES LOADING FACTOR

t_{pd} = 27 ns
P_D = 18 mW (Input High)
3.5 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC893P	0°C	0.880	0.850	1.80	0.500	3.60
MC893P	+25°C	0.830	0.800	1.80	0.460	3.60
MC893P	+75°C	0.740	0.710	1.80	0.400	3.60
MC793P	+15°C	0.865	0.865	1.80	0.475	3.60
MC793P	+25°C	0.850	0.850	1.80	0.460	3.60
MC793P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC893P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC793P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	2,14	-	11	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1,14	-	↓	↓
		14	-		-		-			-		-		-			14	-	1,2	-		
Output Current	I_{A4}	3	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	-	3	-	1,2,14	11	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-		2,4,14
		3	-		-		-			-		-		-			-	2	-	-	↓	1,4,14
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	14	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1	-		2,4,14
		3	-		-		-			-		-		-			-	-	2	-	↓	1,4,14
Switching Time	$t_{on} + t_{off}$	1,3	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 1	Pulse Out 3	-	-	11	2,4,14

Ground input pins of gates not under test. Other pins not listed are left open.

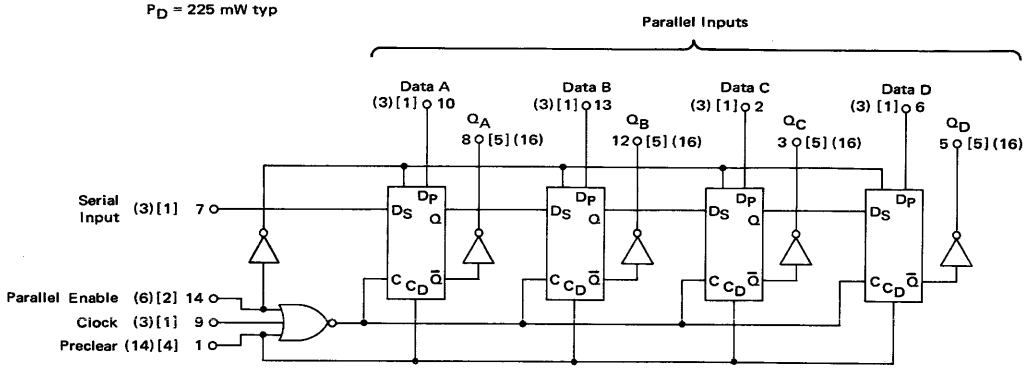
SERIAL-PARALLEL
SHIFT REGISTER

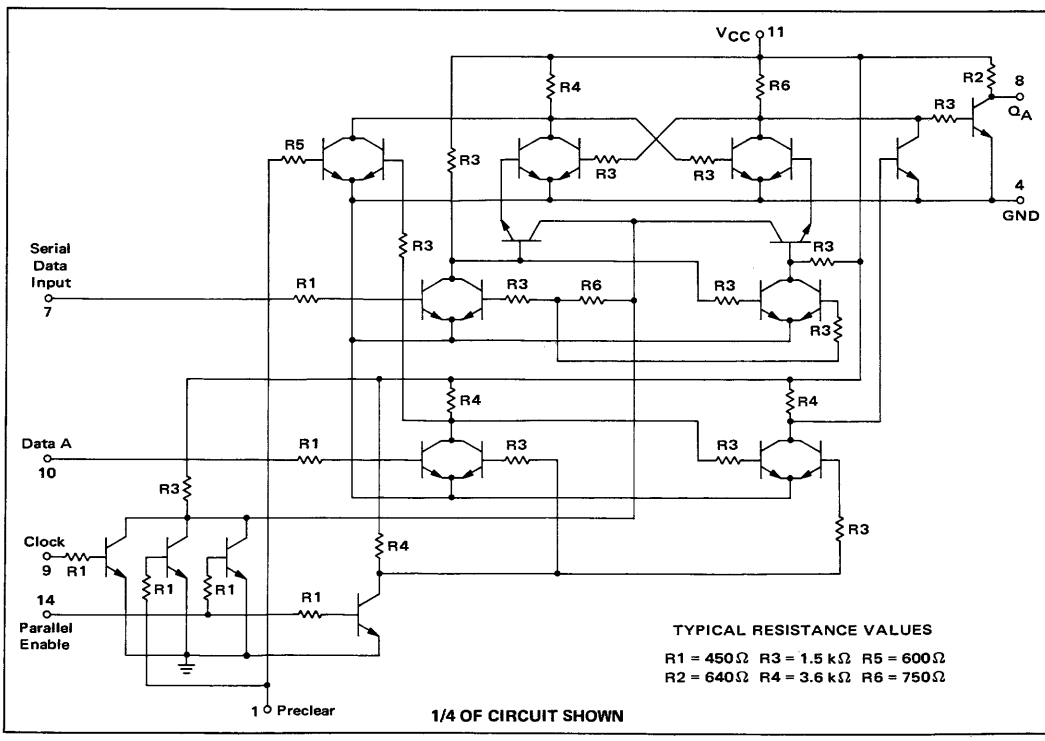
MC794P • MC894P*

Number in parenthesis indicates mW MRTL loading factor. Number in brackets indicates MRTL loading factor.

The MC794P/MC894P is a highly versatile 4-bit Shift Register with both Serial and Parallel entry capability. It can be utilized as an accumulator, buffer register, serial to parallel/parallel to serial converter, and is fully compatible with the other MRTL functions. The clock fall time must be ≤100 ns.

t_{pd} = 55 ns typ
P_D = 225 mW typ





TYPICAL RESISTANCE VALUES

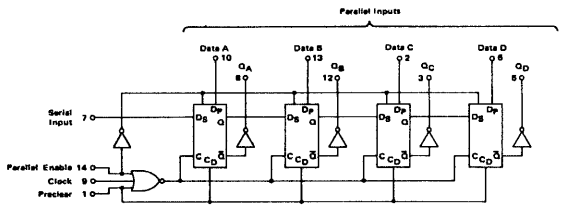
R1 = 450Ω R3 = 1.5 kΩ R5 = 600Ω
R2 = 640Ω R4 = 3.6 kΩ R6 = 750Ω

1/4 OF CIRCUIT SHOWN

*See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures for Inputs B, C, and D are the same as given for Input A (pin 10) in the table below.

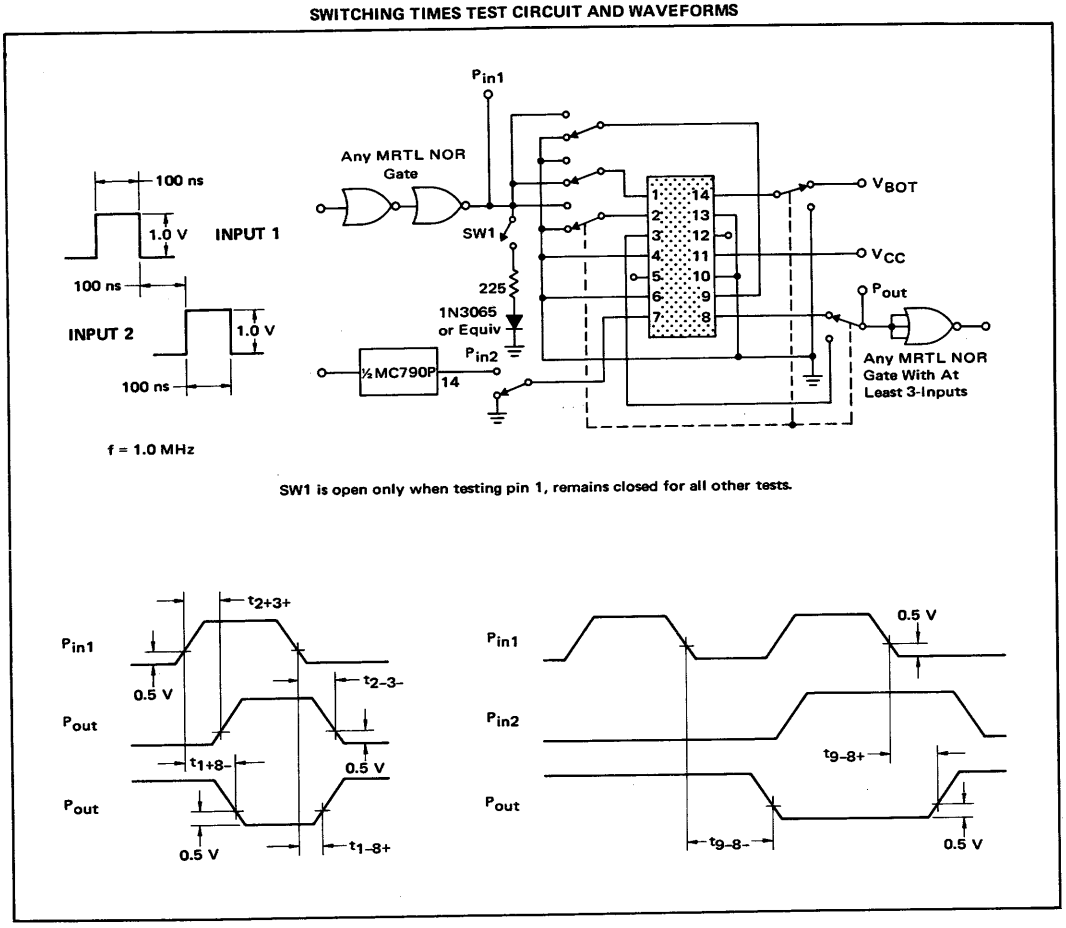


@ Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC894P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC794P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

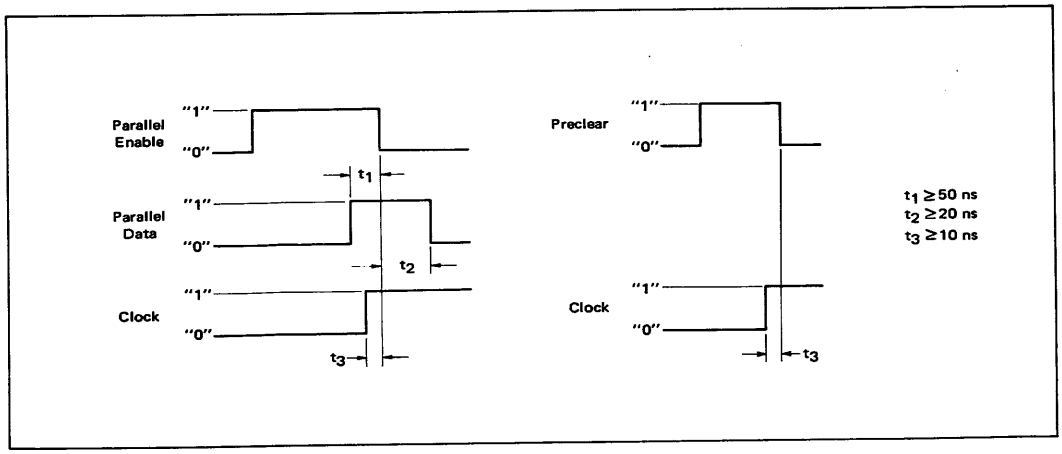
Characteristic	Symbol	Pin Under Test	MC894P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC794P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$4I_{in}$	1	-	2400	-	2400	-	2280	µAdc	-	2000	-	2000	-	1880	µAdc	1,14	-	-	-	11	2,4,6,10,13
	I_{in}	2	-	600	-	600	-	570		-	500	-	500	-	470		2	-	-	-		4,14
		6	-		-		-			-		-		-			6	-	-	-		4,14
		7	-		-		-			-		-		-			7	-	-	-		1,4,9,14
		9	-		-		-			-		-		-			9	-	1,14	-		4
		10	-		-		-			-		-		-			10	-	-	-		4,14
		13	-		-		-			-		-		-			13	-	-	-		4,14
	$2I_{in}$	14	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		14	-	-	-		4
Output Current	I_{A5}	3	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	2,3,14	-	-	11	4
		5		-		-		-			-		-		-		-	5,6,14	-	-		
		8		-		-		-			-		-		-		-	8,10,14	-	-		
		12		-		-		-			-		-		-			12,13,14	-	-		
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	4,14
		3	-		-		-			-		-		-			-	14	-	2		4
		5	-		-		-			-		-		-			-	1	-	-		4,14
		5	-		-		-			-		-		-			-	14	-	6		4
		8	-		-		-			-		-		-			-	1	-	-		4,14
		8	-		-		-			-		-		-			-	14	-	10		4
		12	-		-		-			-		-		-			-	1	-	-		4,14
		12	-		-		-			-		-		-			-	14	-	13		4
Power Supply Drain Current	I_{PD}	11	-	-	-	75	-	-	mAdc	-	-	-	75	-	-	mAdc	-	-	1	-	11	4
Switching Times																	P_{in1}*	P_{in2}*		P_{out}		
	t_{2-3-}	3	-	-	-	70	-	-	ns	-	-	-	70	-	-	ns	2	-	14	3	11	1,4,6,7,9,10,13
	t_{2+3+}	3	-	-	-	68	-	-		-	-	-	68	-	-		2	-	14	3		1,4,6,7,9,10,13
	t_{1+8-}	8	-	-	-	85	-	-		-	-	-	85	-	-		1	-	-	8		2,4,6,7,9,10,13,14
	t_{1-8+}	8	-	-	-	50	-	-		-	-	-	50	-	-		1	-	-	8		2,4,6,7,9,10,13,14
	t_{9-8-}	8	-	-	-	63	-	-		-	-	-	63	-	-		9	7	-	8		1,2,4,6,10,13,14
	t_{9-8+}	8	-	-	-	66	-	-		-	-	-	66	-	-		9	7	-	8		1,2,4,6,10,13,14

Ground all unused input pins. Other pins not listed are left open.
*See "Switching Times Test Circuit and Waveforms".

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



PARALLEL ENABLE MODE



MC796P • MC896P

TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Provides the SUM and CARRY functions while requiring only the AUGEND (A) and ADDEND (B) inputs with CARRY IN.

POSITIVE LOGIC

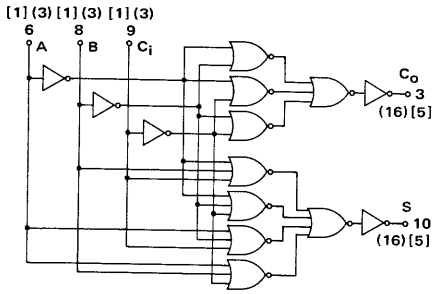
$C_o = ABC_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$

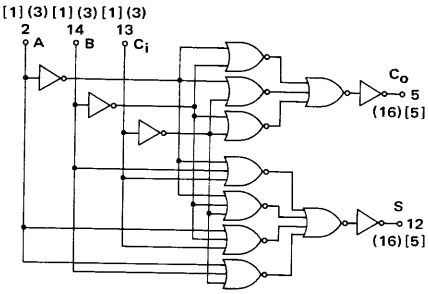
$S = ABC_i + AB\bar{C}_i + \bar{A}\bar{B}C_i + \bar{A}B\bar{C}_i$

t_{pd} = 60 ns typ

P_D = 225 mW typ

Number in Parenthesis Indicates mWMRTL Loading Factor.
Number in Brackets Indicates MRTL Loading Factor.





ELECTRICAL CHARACTERISTICS

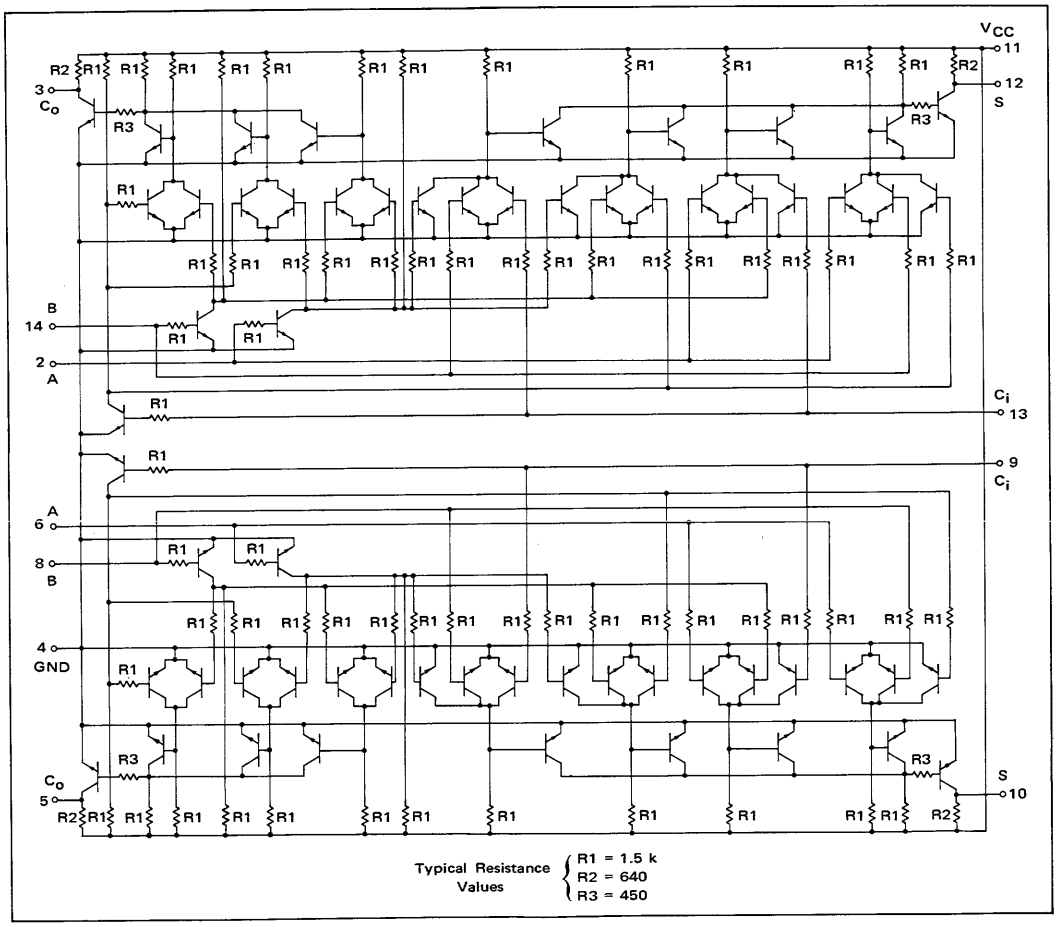
Test procedures are shown for one full adder only. The other full adder is tested in the same manner.

@Test Temperature		V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC896P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.800	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC796P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

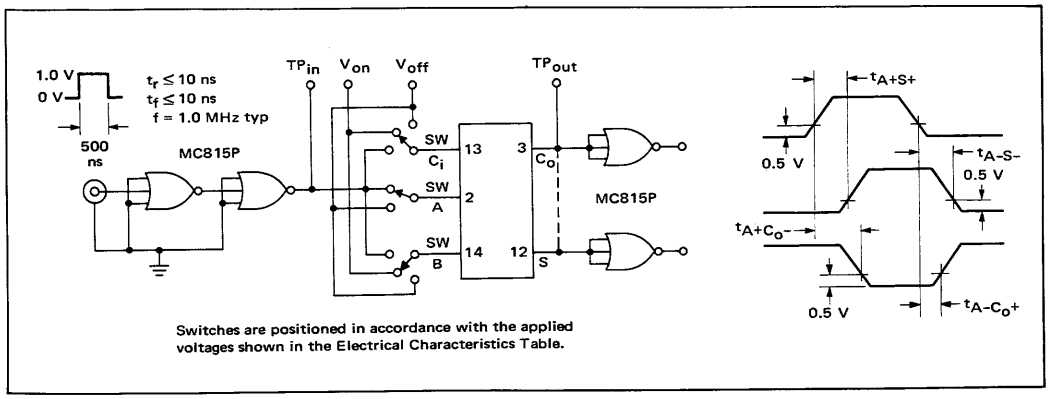
TEST VOLTAGE VALUES (Volts)

Characteristic	Symbol	Pin Under Test	MC896P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC796P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2 13 14	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2 13 14	-	-	-	11	4
Output Current	I_{AS}	3 12	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	- - - - - - - -	3,13,14 2,3,13 2,3,14 (2,3,) (13,14) 12,13 12,14 2,12 (2,12,) (13,14)	- - - - - - - -	2 14 13 - 2,14 2,13 13,14 -	11	4
Output Voltage	V_{out}	3 12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	- - - - - - - -	- 13 14 2 - 13,14 2,14 2,14	- - - - - - - -	2,13,14 2,14 2,13 13,14 2,13,14 2 13 13	11	4
Switching Time																	Pulse In		Pulse Out			
	t_{2+12+}	12	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	2	13,14	12	-	11	4
	t_{2-12-}	12	-	-	-	75	-	-		-	-	-	75	-	-				-	12	-		
	t_{2+3+}	3	-	-	-	85	-	-		-	-	-	85	-	-				13	3	14		
	t_{2-3-}	3	-	-	-	65	-	-		-	-	-	65	-	-				13	3	14		
	t_{14+12+}	12	-	-	-	75	-	-		-	-	-	75	-	-		14	-	12	2,13		
	t_{14-12-}	12	-	-	-	75	-	-		-	-	-	75	-	-				12	2,13		
	t_{14+3+}	3	-	-	-	85	-	-		-	-	-	85	-	-				13	3	2	
	t_{14-3-}	3	-	-	-	65	-	-		-	-	-	65	-	-				13	3		
	t_{13+12-}	12	-	-	-	70	-	-		-	-	-	70	-	-		13	14	12			
	t_{13-12+}	12	-	-	-	80	-	-		-	-	-	80	-	-				12			
	t_{13+3+}	3	-	-	-	70	-	-		-	-	-	70	-	-				3			
	t_{13-3-}	3	-	-	-	80	-	-		-	-	-	80	-	-				3			

Ground inputs of full adder not under test. Other pins not listed are left open.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Switches are positioned in accordance with the applied voltages shown in the Electrical Characteristics Table.

MC797P • MC897P

TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Provides the DIFFERENCE and BORROW functions while requiring only MINUEND (X) and SUBTRAHEND BORROW IN.

POSITIVE LOGIC

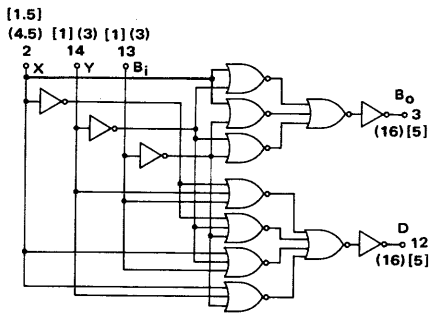
$D = YX\bar{B}_i + \bar{Y}X\bar{B}_i + \bar{Y}\bar{X}B_i + \bar{Y}\bar{X}B_i$

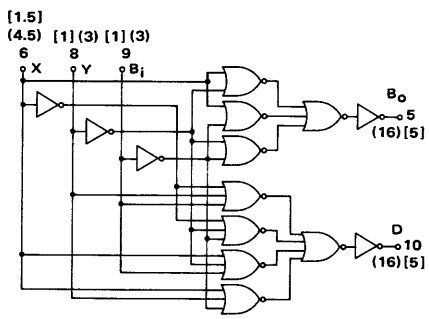
$B_o = \bar{Y}\bar{X}B_i + Y\bar{X}\bar{B}_i + Y\bar{X}B_i + YXB_i$

t_{pd} = 60 ns typ

P_D = 225 mW typ

Number in Parenthesis Indicates mW MRTL Loading Factor.
Number in Brackets Indicates MRTL Loading Factor.





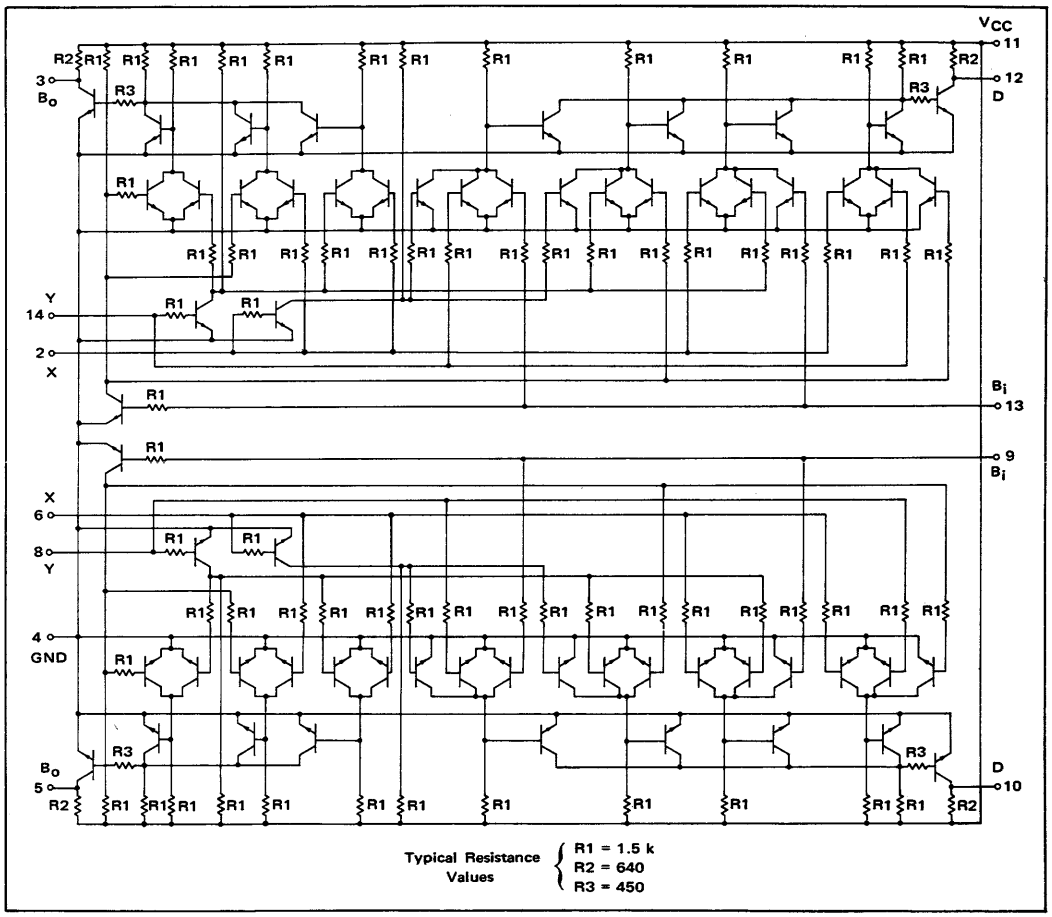
ELECTRICAL CHARACTERISTICS

Test procedures are given for only one subtractor. The other subtractor is tested in the same manner.

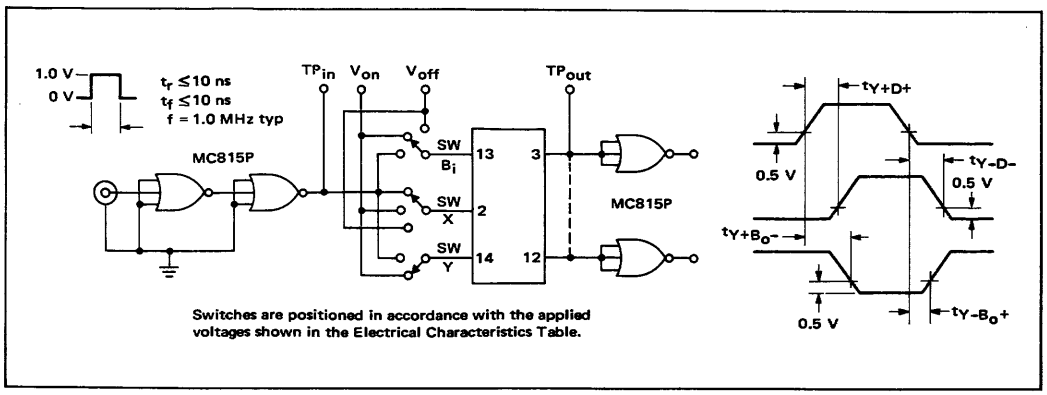
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC897P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.800	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC797P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC897P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC797P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	1.5 I_{in}	2	-	900	-	900	-	855	μAdc	-	750	-	750	-	705	μAdc	2	-	-	-	11	4
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		13	-	-	-		
	I_{in}	14	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	14	-	-	-	↓	↓
Output Current	I_{A5}	3	3.00	-	3.00	-	2.85	-	mAdc	2.85	-	2.85	-	2.50	-	mAdc	-	2,3, (13,14)	-	-	11	4
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3,13	-	2,14	↓	↓
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3,14	-	2,13	↓	↓
		12	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	12,13	-	2,14	↓	↓
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	12,14	-	2,13	↓	↓
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	2,12	-	13,14	↓	↓
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	(2,12, 13,14)	-	-	↓	↓
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2,13	-	14	11	4
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2,14	-	13	↓	↓
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	2,13,14	↓	↓
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	2,13,14	↓	↓
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13,14	-	2	↓	↓
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2,14	-	13	↓	↓
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2,13	-	14	↓	↓
Switching Time																	Pulse In		Pulse Out			
	t_{2+12+}	12	-	-	-	60	-	-	ns	-	-	-	60	-	-	ns	2	13,14	12	-	11	4
	t_{2-12-}	12	-	-	-	60	-	-	↓	-	-	-	60	-	-	↓	↓	↓	12	-	↓	↓
	t_{2+3+}	3	-	-	-	65	-	-	↓	-	-	-	65	-	-	↓	↓	↓	3	-	↓	↓
	t_{2-3-}	3	-	-	-	60	-	-	↓	-	-	-	60	-	-	↓	↓	↓	3	-	↓	↓
	t_{14+12+}	12	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	14	-	12	2,13	↓	↓
	t_{14-12-}	12	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	↓	-	12	2,13	↓	↓
	t_{14+3-}	3	-	-	-	65	-	-	↓	-	-	-	65	-	-	↓	↓	13	3	2	↓	↓
	t_{14-3+}	3	-	-	-	60	-	-	↓	-	-	-	60	-	-	↓	↓	↓	3	↓	↓	↓
	t_{13+12-}	12	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	13	↓	12	↓	↓	↓
	t_{13-12+}	12	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	↓	↓	12	↓	↓	↓
	t_{13+3+}	3	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	↓	2,14	3	-	↓	↓
	t_{13-3-}	3	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	↓	2,14	3	-	↓	↓

Ground input pins of subtractor not under test. Other pins not listed are left open.

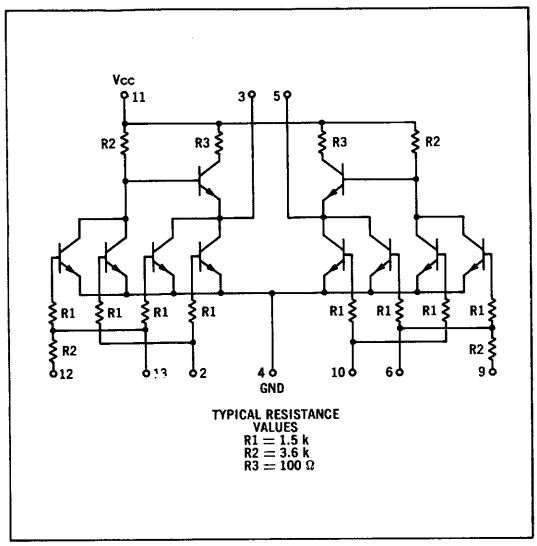


SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



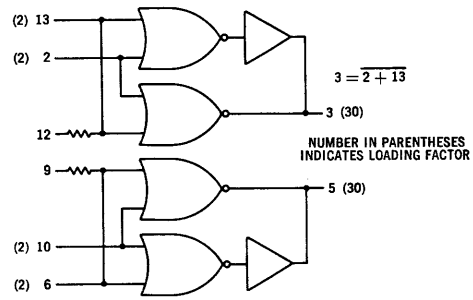
Switches are positioned in accordance with the applied voltages shown in the Electrical Characteristics Table.

MC798P • MC898P



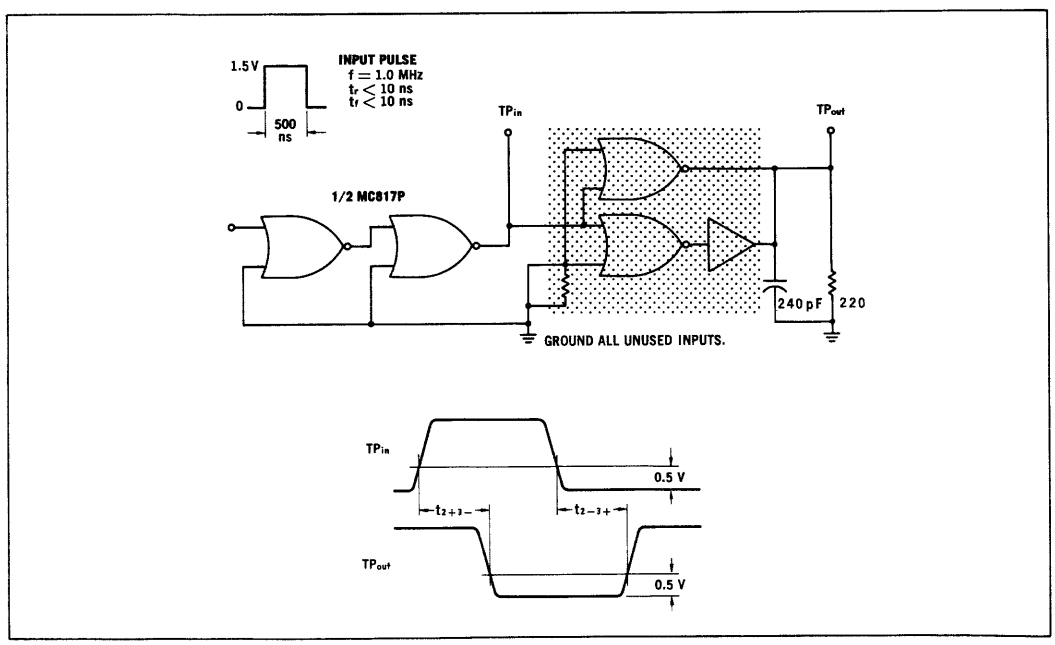
TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k
R3 = 100 Ω

Dual 2-input buffers designed to drive a greater number of loads than the basic Resistor Transistor Logic circuit. Returning an input resistor to V_{CC} allows for capacitive coupling in multivibrator and differentiator applications.



t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

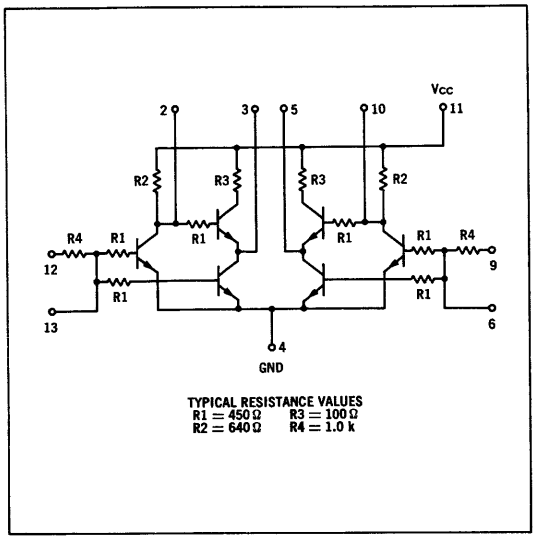
Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(k Ohms) V_R*
MC898P	0°C	0.880	0.850	1.80	0.500	3.60	4.6
	+25°C	0.830	0.800	1.80	0.460	3.60	4.8
	+75°C	0.740	0.710	1.80	0.400	3.60	5.0
MC798P	+15°C	0.865	0.865	1.80	0.475	3.60	4.6
	+25°C	0.850	0.850	1.80	0.460	3.60	4.8
	+55°C	0.800	0.800	1.80	0.430	3.60	5.0

Characteristic	Symbol	Pin Under Test	MC898P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC798P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2\ I_{in}$	2	-	300	-	280	-	280	μAdc	-	300	-	300	-	300	μAdc	2	-	13	-	11	-	4
Output Current	I_{AB}	3	4.5	-	4.5	-	4.5	-	mAdc	5.0	-	5.0	-	5.0	-	mAdc	-	3	-	2, 13	11	-	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	3	2, 4
		3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	3	4, 13
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	13	-	11	3	2, 4
		3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	-	11	3	4, 13
Switching Time	$t_{on} + t_{off}$	2, 3	-	-	-	160	-	-	ns	-	-	-	160	-	-	ns	Pulse In: 2	Pulse Out: 3	-	-	11	-	4, 13

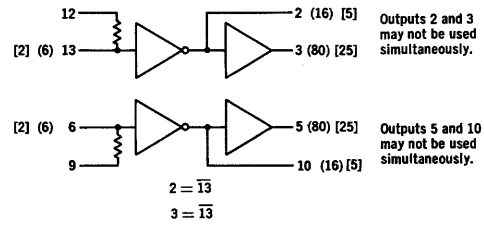
Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

MC799P • MC899P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω R3 = 100 Ω
R2 = 640 Ω R4 = 1.0 k

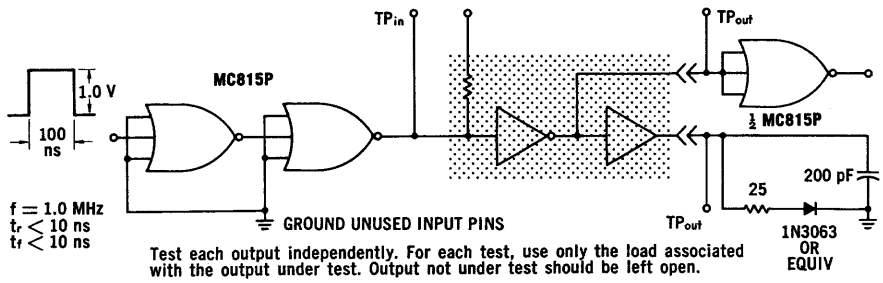
The dual buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input, the differentiation of input waveforms and various multivibrator applications.



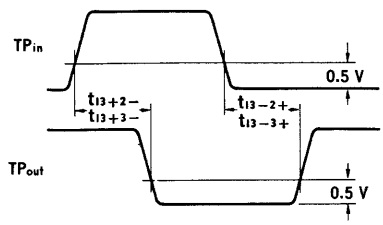
NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test. Output not under test should be left open.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

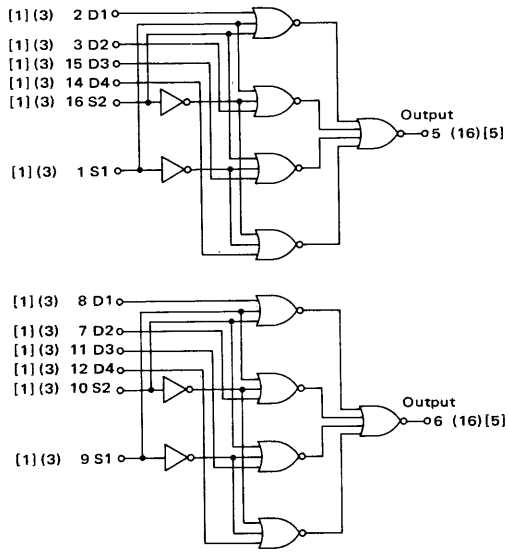
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC899P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.800	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC799P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC899P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC799P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2I_{in}$	13	-	1.2	-	1.2	-	1.1	mAdc	-	1.0	-	1.0	-	0.94	mAdc	13	-	-	-	11	-	4
Output Current	I_{A5}	2	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	2	-	13	11	-	4
	I_{AB}	3	15.0	-	15.0	-	14.25	-	mAdc	13.75	-	13.75	-	12.50	-	mAdc	-	3	-	13	11	-	4
Output Voltage	V_{out}	2	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	-	4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	3	4
Saturation Voltage	$V_{CE(sat)}$	2	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	13	-	11	-	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	11, 12	-	
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	13	-	11	3	↓
Switching Time	t	13+3-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	Pulse In 13	Pulse Out 3	-	-	11	-	4
		13-3+	-	-	-	45	-	-	↓	-	-	-	45	-	-	↓	13	3	-	-	↓	-	↓
		13+2-	-	-	-	28	-	-		-	-	-	28	-	-		13	2	-	-		-	
		13-2+	-	-	-	32	-	-		-	-	-	32	-	-		13	2	-	-		-	

Ground all unused input pins. Other pins not listed are left open. * Resistor Value to V_{CC}.

MC9701P • MC9801P

A dual electronic four-position switch that enables selection of any one of four data input lines selected by a binary coded select input.



Number in Parenthesis Indicates mW MRTL Loading Factor.
Number in Brackets Indicates MRTL Loading Factor.

TRUTH TABLE

Input Select		Data Line
S1	S2	Selected
0	0	D1
0	1	D2
1	0	D3
1	1	D4

$$\text{Output} = \overline{S1}\,\overline{S2}\,D1 + \overline{S1}\,S2\,D2 + S1\,\overline{S2}\,D3 + S1\,S2\,D4$$

Avg. t_{pd} = 25 ns typ

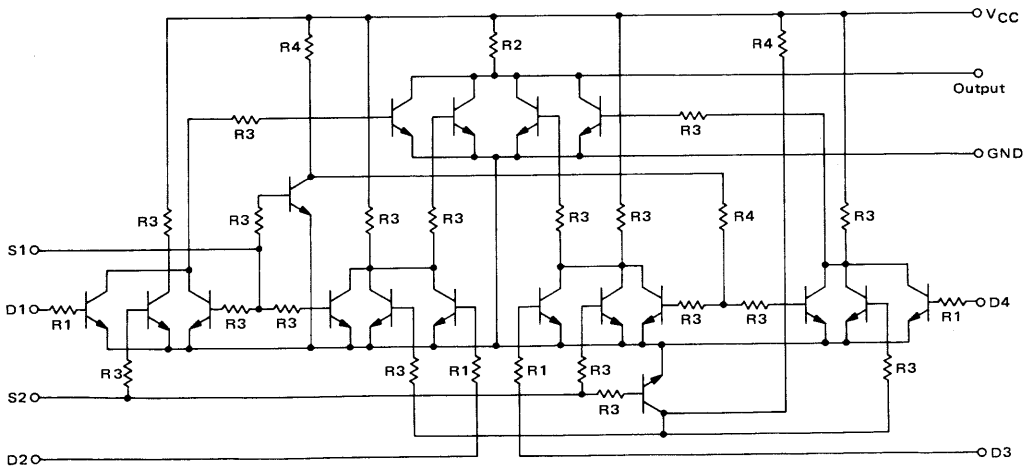
Avg. $t_{pd} = \frac{t_{+-} + t_{-+}}{2}$

P_D = 100 mW typ

Operating Frequency = 18 MHz typ

(Both Selector Inputs and Data Inputs High)

(1/2 OF CIRCUIT SHOWN)



TYPICAL RESISTANCE VALUES

R1 = 450Ω R3 = 1.5 k

R2 = 640Ω R4 = 3.6 k

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one data selector only. The other data selector is tested in the same manner.

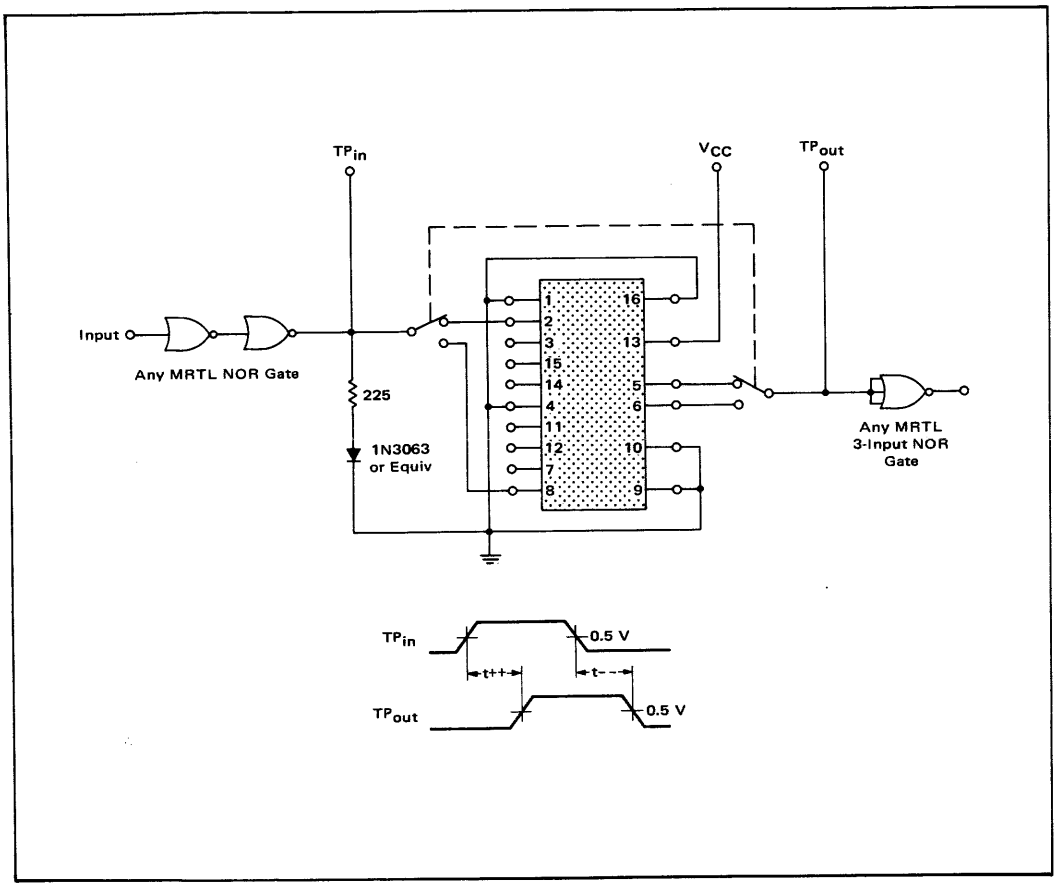
	@ Test Temperature	V_{in}	V_{on}	V_{off}	V_{CC}
MC9801P	0°C	0.960	0.930	0.570	3.60
	+25°C	0.910	0.880	0.500	3.60
	+75°C	0.820	0.790	0.450	3.60
MC9701P	+15°C	0.865	0.865	0.475	3.60
	+25°C	0.850	0.850	0.460	3.60
	+55°C	0.800	0.800	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC9801P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9701P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	-	13	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	-	↓	↓
		3	-		-		-			-		-		-			3	-	-		
		14	-		-		-			-		-		-			14	-	-		
		15	-		-		-			-		-		-			15	-	-		
		16	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	16	-	-	↓	↓
Output Current	I_{A5}	5	-3.0	-	-3.0	-	-2.85	-	mAdc	-2.65	-	-2.65	-	-2.5	-	mAdc	-	2,5	1,16	13	4
		5	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3,5,16	1	↓	↓
		5		-		-		-			-		-		-		-	1,5,14,16	-		
		5		-		-		-			-		-		-		-	1,5,15	16		
Saturation Voltage	$V_{CE(sat)}$	5	-	400	-	400	-	400	mVdc	-	300	-	300	-	320	mVdc	-	-	1,2,16	13	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	16	1,3	↓	↓
		5	-		-		-			-		-		-			-	1	15,16		
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1,16	14	↓	↓
Power Supply Current Drain	I_{PD}*	13	-	-	-	37	-	-	mAdc	-	-	-	37	-	-	mAdc	1,9,10,16	-	-	-	-
																	Pulse In	Pulse Out			
Switching Times	t_{2+5+}	5	-	-	-	32	-	-	ns	-	-	-	32	-	-	ns	2	5	-	13	1,4,16
	t_{2-5-}	5	-	-	-	26	-	-	ns	-	-	-	26	-	-	ns	2	5	-	13	1,4,16

*I_{PD} test is for both halves of the dual selector.

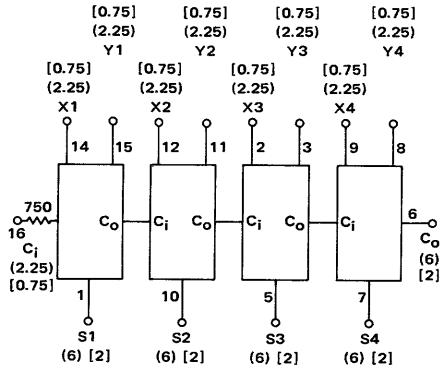
Ground inputs of dual selector not under test. Other pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



MC9704P • MC9804P

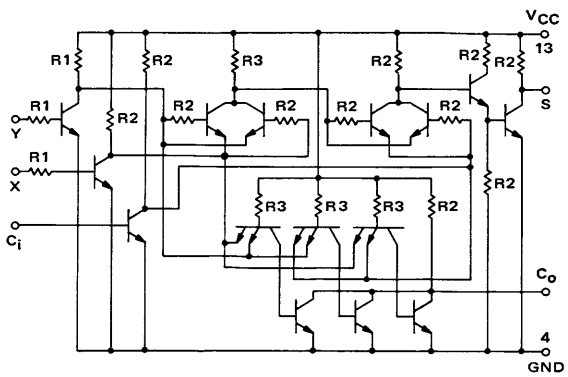
MC9704P/9804P is a four-bit full adder with ripple-through carry.



C_o t_{pd} = 125 ns typ
P_D = 265 mW typ
Operating Frequency = 8.0 MHz

Number in Parenthesis Indicates Loading Factor for mW MRTL. Number in Brackets Indicates Loading Factor for MRTL.

(1/4 OF CIRCUIT SHOWN)



TYPICAL RESISTANCE VALUES
R1 = 750Ω
R2 = 1.5 k
R3 = 3.6 k

ELECTRICAL CHARACTERISTICS

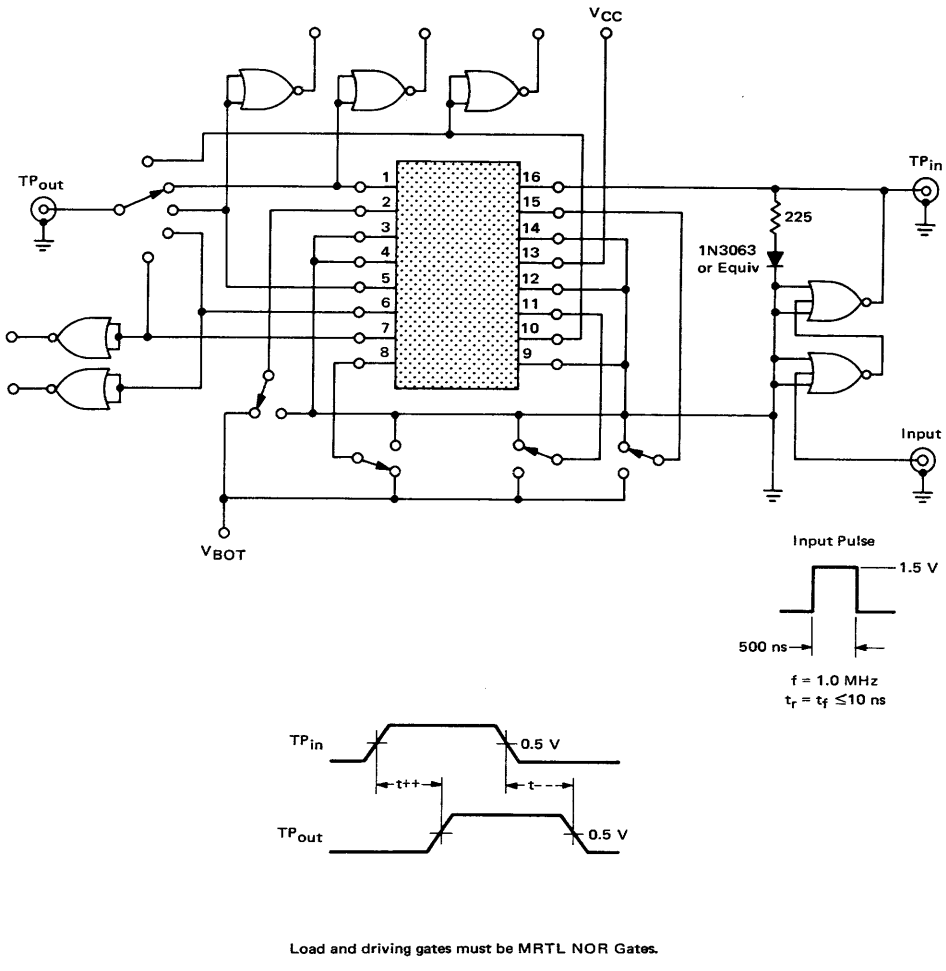
Test procedures are shown for one adder only. The other adders are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC9804P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC9704P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC9804P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9704P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$0.75\ I_{in}$	14	-	450	-	450	-	427	μAdc	-	375	-	375	-	353	μAdc	14	-	15,16	-	13	4
		15	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	15	-	14,16	-	↓	↓
		16	-		-		-			-		-		-			16	-	14,15	-		
Output Current	I_{A2}	1	-1.20	-	-1.20	-	-1.14	-	mAdc	-1.00	-	-1.00	-	-0.94	-	mAdc	-	1,15	-	14,16	13	4
		5	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3,5	-	2,11,12,14,15,16	↓	↓
		6		-		-		-			-		-		-		-	6,8,9	-	2,3,14,15,16		
		7		-		-		-			-		-		-		-	7,9	-	2,3,8,14,15,16		
		10		-		-		-			-		-		-		-	10,11	-	12,14,15,16		
Output Voltage	V_{out}	1	-	0.500	-	0.400	-	0.400	Vdc	-	0.400	-	0.300	-	0.320	Vdc	-	-	-	14,15,16	13	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	2,3,11,12,14,15,16	↓	↓
		6	-		-		-			-		-		-			-	-	-	2,3,8,9,11,12,14,15,16		
		7	-		-		-			-		-		-			-	-	-	2,3,8,9,11,12,14,15,16		
		10	-		-		-			-		-		-			-	-	-	11,12,14,15,16		
Power Supply Current Drain	I_{PD}	13	-	-	-	80	-	-	mAdc	-	-	-	80	-	-	mAdc	-	-	-	-	13	4
Switching Times Propagation Delay																	Pulse In	Pulse Out				
	t_{16+6+}	6	-	-	-	135	-	-	ns	-	-	-	135	-	-	ns	16	6	2,8,11,15	-	13	3,4,9,12,14
	t_{16-6-}	6	-	-	-	110	-	-	↓	-	-	-	110	-	-	↓	↓	6	2,8,11,15	-	↓	3,4,9,12,14
	t_{16+1+}	1	-	-	-	90	-	-		-	-	-	90	-	-			1	-	-		2,3,4,8,9,11,12,14,15
	t_{16-1-}	1	-	-	-	50	-	-		-	-	-	50	-	-			1	-	-		2,3,4,8,9,11,12,14,15
	t_{16+10+}	10	-	-	-	105	-	-		-	-	-	105	-	-			10	15	-		2,3,4,8,9,11,12,14
	t_{16-10-}	10	-	-	-	70	-	-		-	-	-	70	-	-			10	15	-		2,3,4,8,9,11,12,14
	t_{16+5+}	5	-	-	-	120	-	-		-	-	-	120	-	-			5	11,15	-		2,3,4,8,9,12,14
	t_{16-5-}	5	-	-	-	90	-	-		-	-	-	90	-	-			5	11,15	-		2,3,4,8,9,12,14
	t_{16+7+}	7	-	-	-	135	-	-		-	-	-	135	-	-			7	2,11,15	-		3,4,8,9,12,14
	t_{16-7-}	7	-	-	-	110	-	-	↓	-	-	-	110	-	-	↓	↓	7	2,11,15	-	↓	3,4,8,9,12,14

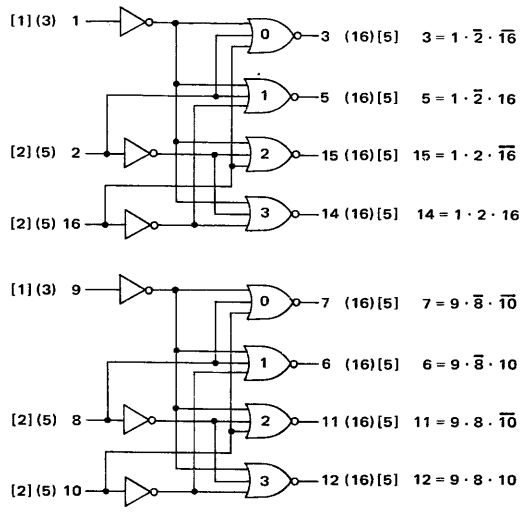
Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Load and driving gates must be MRTL NOR Gates.

MC9707P • MC9807P †



Number in parenthesis indicates loading factor for mW MRTL.
Number in brackets indicates loading factor for MRTL.

MC9707P/MC9807P consists of two electronic, one-pole, four-position switches which route one-bit of binary data to one of four output lines. Switching is accomplished by means of a pair of BCD coded select lines.

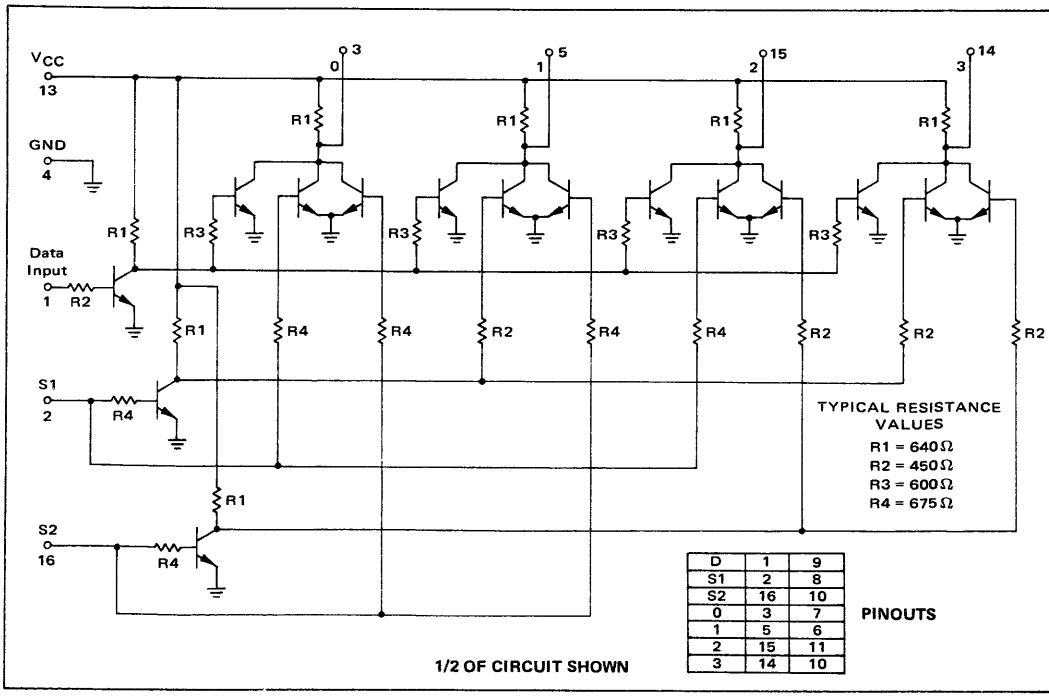
TRUTH TABLE

	INPUTS			OUTPUTS			
	D	S1	S2	0	1	2	3
Pin Numbers	1	2	16	3	5	15	14
	9	8	10	7	6	11	12
Level	0	*	*	0	0	0	0
	1	0	0	1	0	0	0
	1	0	1	0	1	0	0
	1	1	0	0	0	1	0
	1	1	1	0	0	0	1

*Either state.

A_{vg}* t_{pd} = 25 ns typ
P_D = 150 mW typ

$$*A_{vg}\ t_{pd} = \frac{t_{on} + t_{off}}{2}$$



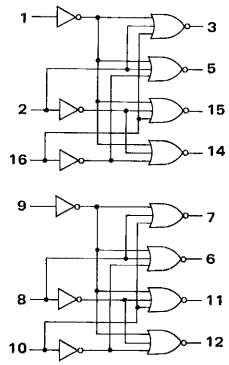
D	1	9
S1	2	8
S2	16	10
0	3	7
1	5	6
2	15	11
3	14	10

PINOUTS

†See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are given for only one of the Dual Data Distributors. The other Data Distributor is tested in the same manner.

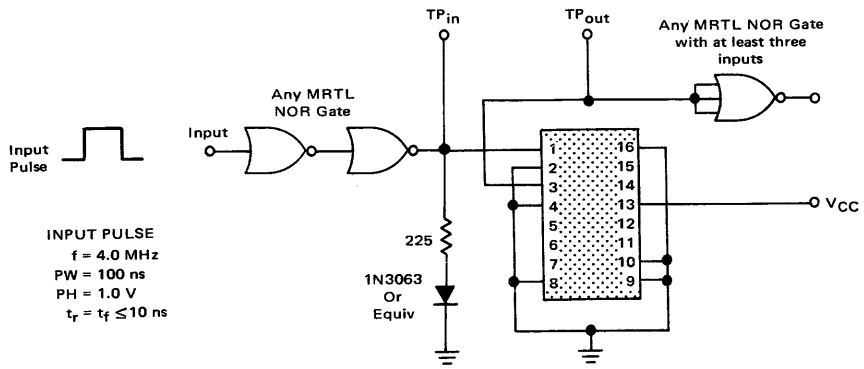


@ Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC9807P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC9707P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

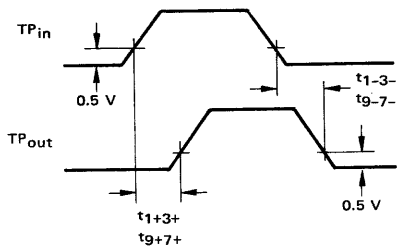
Characteristic	Symbol	Pin Under Test	MC9807P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9707P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	-	-	13	4
	$^2_{in}$	2	-	1200	-	1200	-	1140	↓	-	1000	-	1000	-	940	↓	2	-	16	-	↓	↓
		16	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		16	-	1	-		
Output Current	I_{A5}	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	1,3	-	2,16	13	4
		5	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	1,5,16	-	2	↓	↓
		14		-		-		-			-		-		-		-	1,2,14,16	-	-		
		15		-		-		-			-		-		-		-	1,2,15	-	16		
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2	1	-	13	4,16
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	1,16	-	↓	4
		14	-		-		-			-		-		-			-	-	2,16	1		↓
		15	-		-		-			-		-		-			-	16	1,2	-		
Power Supply Drain Current	I_{PD}	13	-	-	-	68	-	-	mAdc	-	-	-	68	-	-	mAdc	-	-	2,8,10,16	-	13	1,4,9
Switching Times																	Pulse In	Pulse Out				
	t_{1+3+}	1	-	-	-	36	-	-	ns	-	-	-	36	-	-	ns	1	3	-	-	13	2,16
	t_{1-3-}	1	-	-	-	26	-	-	ns	-	-	-	26	-	-	ns	1	3	-	-	13	2,16

Ground input pins of data distributor not under test.
Other pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

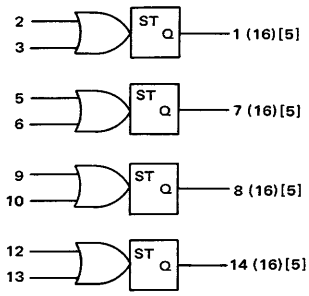


To measure t_{g+7+} and t_{g-7-}, connect input to pin 9, output to pin 7, and ground pin 1. The remainder of the test configuration is unchanged.



MC9709P • MC9809P

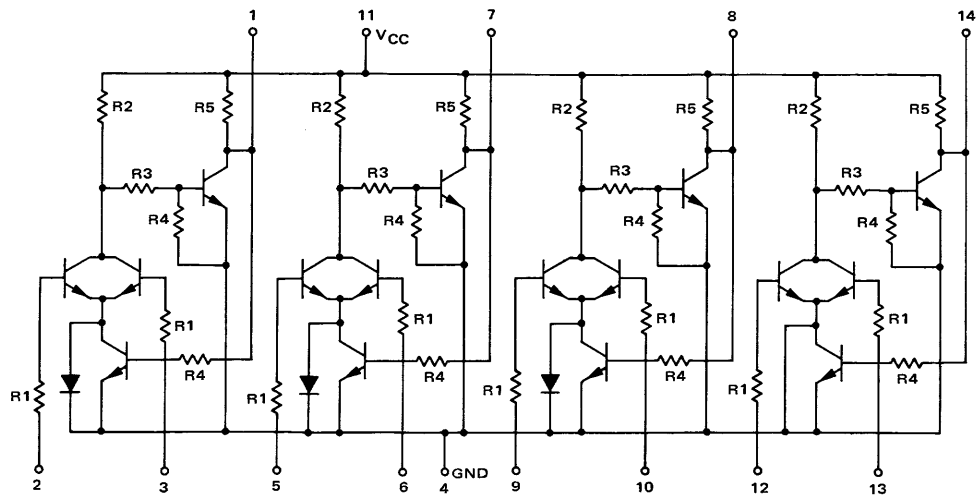
The MC9709P/9809P device consists of four Schmitt Triggers in a single 14-pin dual in-line plastic package. It provides a square-wave output from a slow-rise-time input with 650 mV internal hysteresis.



$t_r = t_f = 20$ ns typ
Avg. $t_{pd} = 30$ ns typ, Avg. $= \frac{t_{on} + t_{off}}{2}$
f = 18 MHz typ
$P_D = 95$ mW typ

Upper Trigger Voltage = 1.40 V typ
Lower Trigger Voltage = 0.75 V typ

Number in Parenthesis Indicates mW MRTL Loading Factor.
Number in Brackets Indicates MRTL Loading Factor.



TYPICAL RESISTANCE VALUES

R1 = 450 Ω	R4 = 1.5 k
R2 = 2.0 k	R5 = 640 Ω
R3 = 500 Ω	

ELECTRICAL CHARACTERISTICS

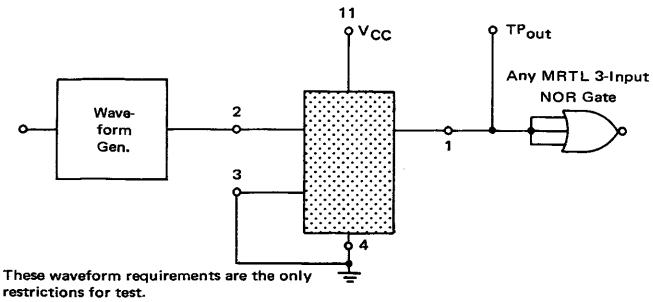
Test procedures are shown for one Schmitt Trigger only. The other Schmitt triggers are tested in the same manner.

	@ Test Temperature	V_{on}	V_{BOT}	V_{off}	V_{CC}
		TEST VOLTAGE VALUES (Volts)			
MC9809P	0°C	0.930	1.80	0.570	3.60
MC9809P	+25°C	0.880	1.80	0.500	3.60
MC9809P	+75°C	0.790	1.80	0.450	3.60
MC9709P	+15°C	0.865	1.80	0.475	3.60
MC9709P	+25°C	0.850	1.80	0.460	3.60
MC9709P	+55°C	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC9809P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9709P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Output Current	I_{A5}	1	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	1	2	-	11	4
		1	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	1	3	-	11	4
Output Voltage	V_{out}	1	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	2,3	11	4
Power Supply Drain Current (Total Device)	I_{PD}	11	-	-	-	32	-	-	mAdc	-	-	-	32	-	-	mAdc	-	-	-	11	4
																	Pulse Out	Input			
Output Pulse	t_{1+}	1	-	100	-	100	-	100	ns	-	100	-	100	-	100	ns	1	2	-	11	4
Rise and Fall Times	t_{1-}	1	-	100	-	100	-	100	ns	-	100	-	100	-	100	ns	1	2	-	11	4

Ground unused input pins. Other pins not listed are left open.

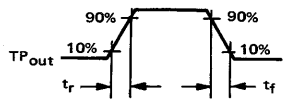
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



These waveform requirements are the only restrictions for test.

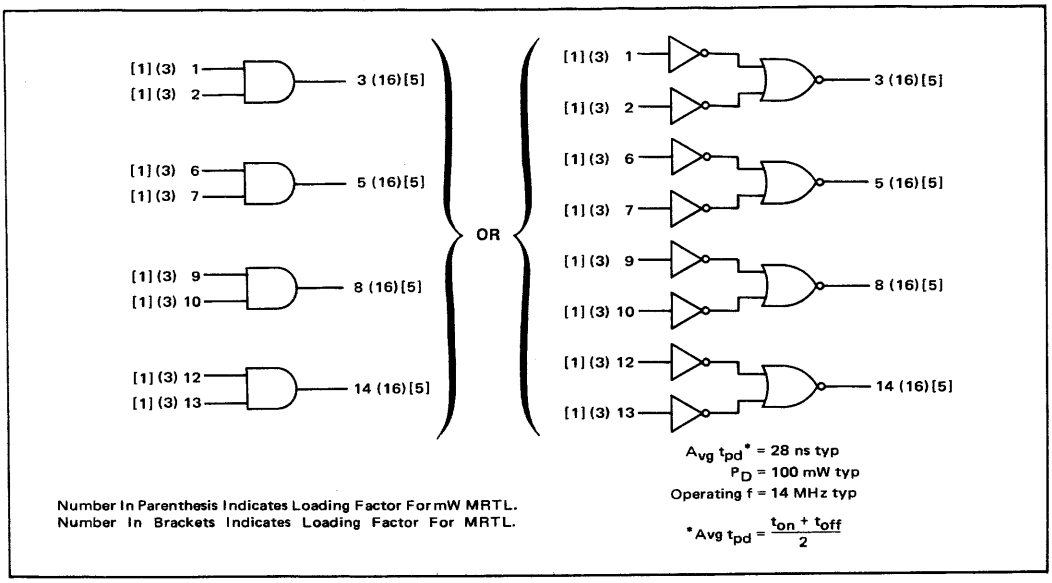
$f \geq 60$ Hz

$PA^* = 2.0$ V *Do not exceed ± 4.0 volts.



MC9713P • MC9813P

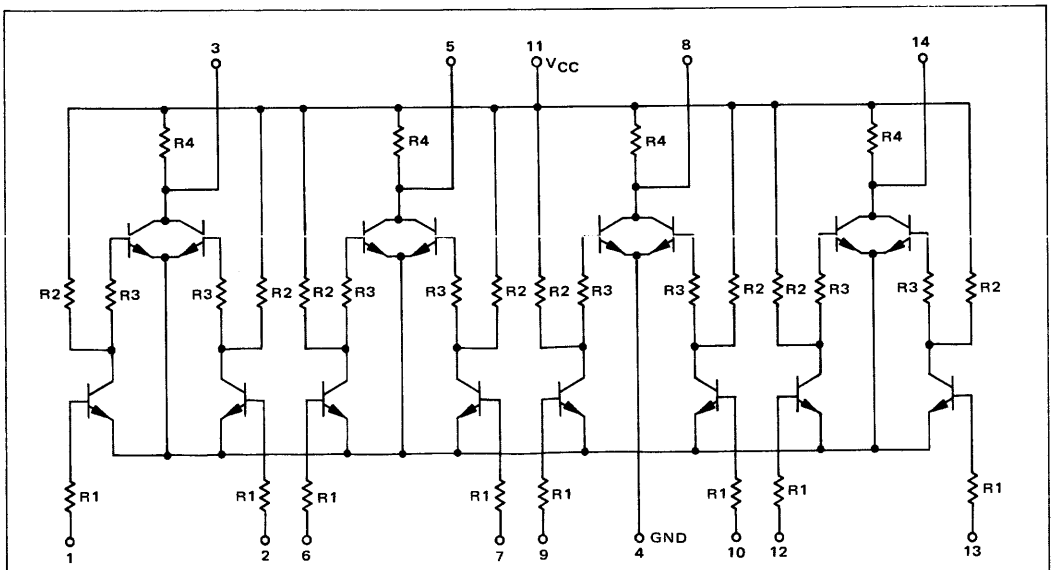
Increased logic flexibility is provided by MC9713P/9813P, quad 2-input AND gates in a single 14-pin dual in-line plastic package.



Number In Parenthesis Indicates Loading Factor For mW MRTL.
Number In Brackets Indicates Loading Factor For MRTL.

$A_{vg}\ t_{pd}{}^{*} = 28$ ns typ
$P_D = 100$ mW typ
Operating f = 14 MHz typ

$^{*}A_{vg}\ t_{pd} = \frac{t_{on} + t_{off}}{2}$



TYPICAL RESISTANCE VALUES

R1 = 450Ω
R2 = 1.8 k
R3 = 1.5 k
R4 = 640 Ω

ELECTRICAL CHARACTERISTICS

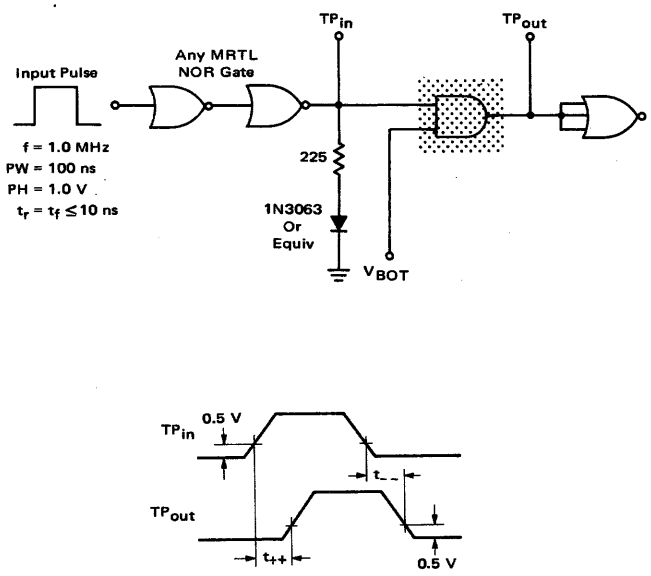
Test procedures are shown for one gate only. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC9813P 0°C	0.960	0.930	1.80	0.570	3.60
MC9813P +25°C	0.910	0.880	1.80	0.500	3.60
MC9813P +75°C	0.820	0.790	1.80	0.450	3.60
MC9713P +15°C	0.865	0.865	1.80	0.475	3.60
MC9713P +25°C	0.850	0.850	1.80	0.460	3.60
MC9713P +55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC9813P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9713P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	-	-	11	4
		2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	-	-	11	4
Output Current	I_{A5}	3	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	1,2,3	-	-	11	4
Output Voltage	V_{out}	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	2	-	1	11	4
		3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	1	-	2	11	4
Power Supply Drain Current	I_{PD}	11	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc	-	-	2,7,10,13	-	11	1,4,6,9,12
Switching Times																	Pulse In	Pulse Out				
	t_{1+3+}	3	-	-	-	42	-	-	ns	-	-	-	42	-	-	ns	1	3	2	-	11	4
	t_{1-3-}		-	-	-	26	-	-		-	-	-	26	-	-		1		2	-		
	t_{2+3+}		-	-	-	42	-	-		-	-	-	42	-	-		2		1	-		
	t_{2-3-}		-	-	-	26	-	-		-	-	-	26	-	-		2		1	-		

Ground inputs of gates not under test. Other pins not listed are left open.

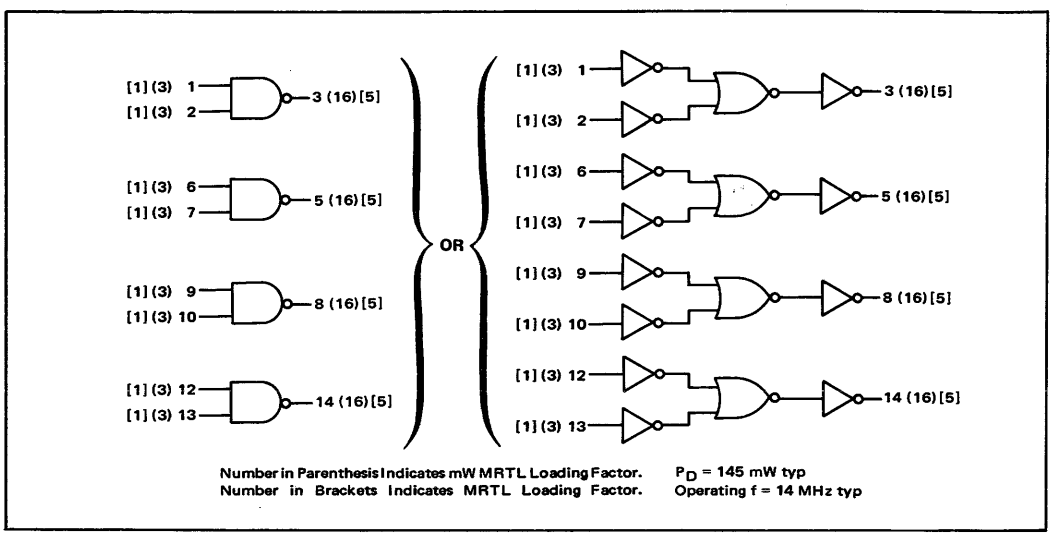
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



QUAD 2-INPUT
"NAND" GATE

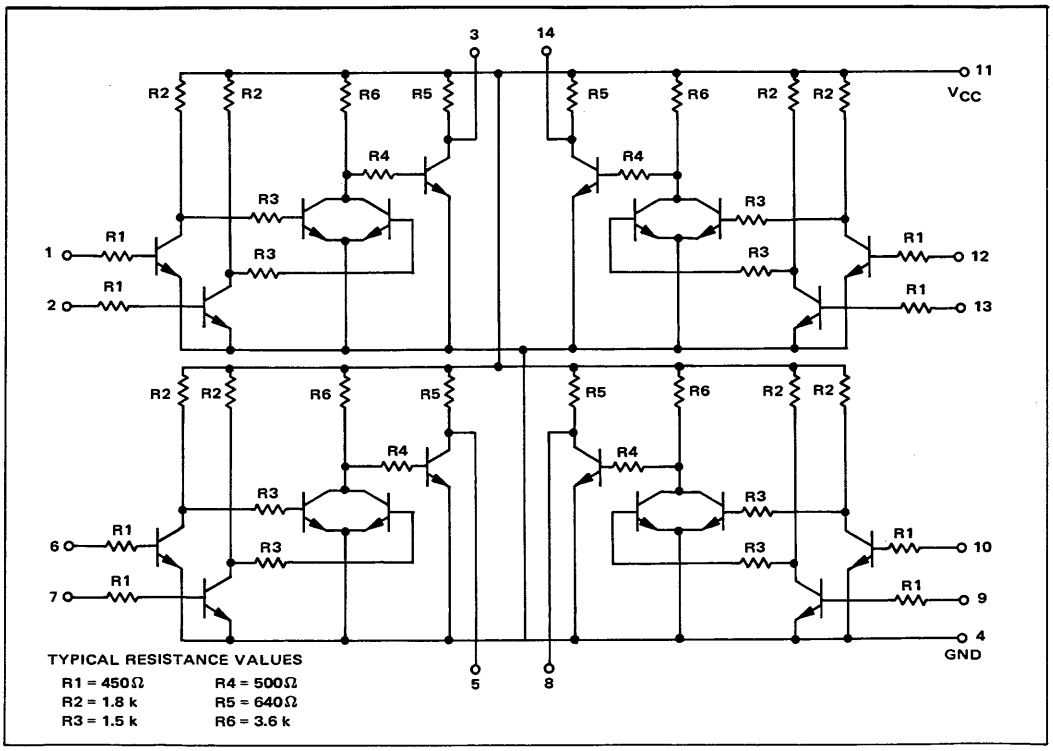
MC9714P • MC9814P

Increased logic flexibility is provided by MC9714P/9814P, quad 2-input positive logic NAND gates in a single 14-pin dual in-line plastic package.



Number in Parenthesis Indicates mW MRTL Loading Factor.
Number in Brackets Indicates MRTL Loading Factor.

P_D = 145 mW typ
Operating f = 14 MHz typ



TYPICAL RESISTANCE VALUES

R1 = 450Ω	R4 = 500Ω
R2 = 1.8 k	R5 = 640Ω
R3 = 1.5 k	R6 = 3.6 k

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only. The other gates are tested in the same manner.

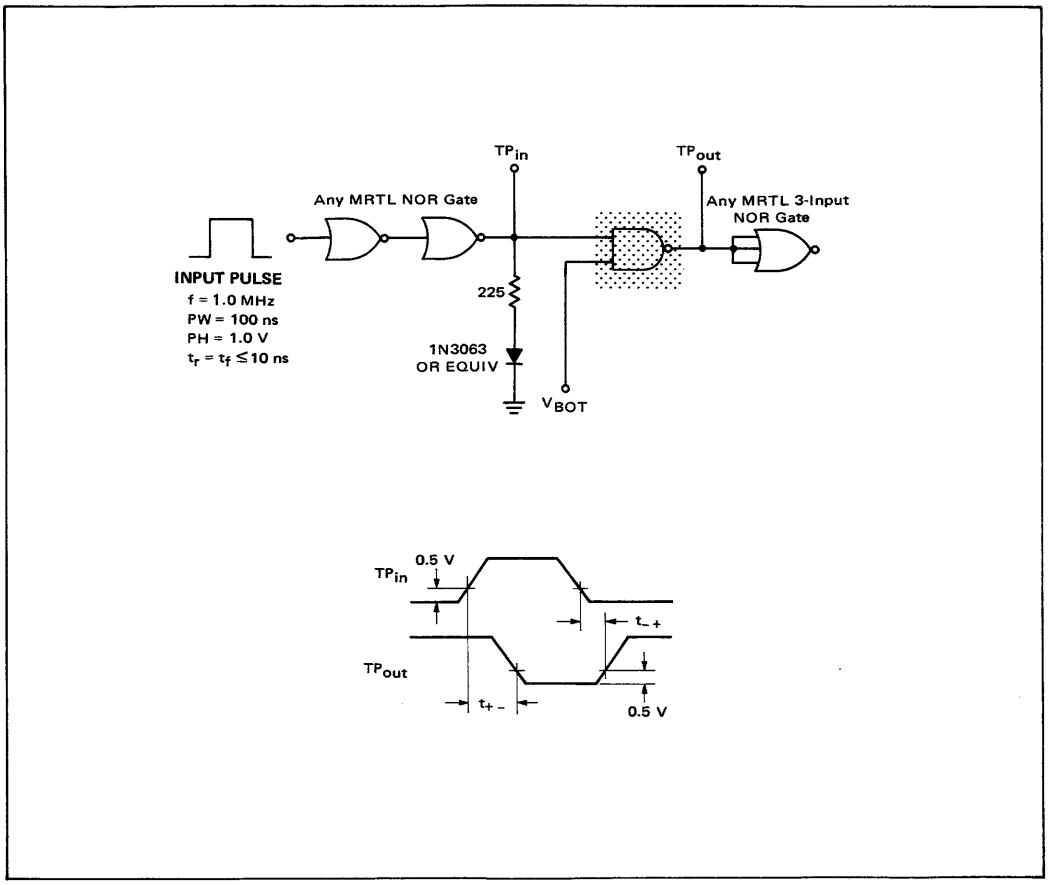
@ Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC9814P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC9714P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC9814P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9714P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	-	-	11	4
		2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	-	-	11	4
Output Current	I_{A5}	3	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	2,3	-	1	11	4
		3	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	1,3	-	2	11	4
Output Voltage	V_{out}	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	1,2	-	-	11	4
Power Supply Drain Current	I_{PD}*	11	-	-	-	52	-	-	mAdc	-	-	-	52	-	-	mAdc	-	-	1,2,6,7,9, 10,12,13	-	11	4
Switching Times																	Pulse In	Pulse Out				
	t_{1+3-}	3	-	-	-	57	-	-	ns	-	-	-	57	-	-	ns	1	3	2	-	11	4
	t_{1-3+}	↓	-	-	-	38	-	-	↓	-	-	-	38	-	-	↓	1	3	2	-	↓	↓
	t_{2+3-}	↓	-	-	-	57	-	-	↓	-	-	-	57	-	-	↓	2	3	1	-	↓	↓
	t_{2-3+}	↓	-	-	-	38	-	-	↓	-	-	-	38	-	-	↓	2	3	1	-	↓	↓

Ground inputs of gates not under test. Pins not listed are left open.

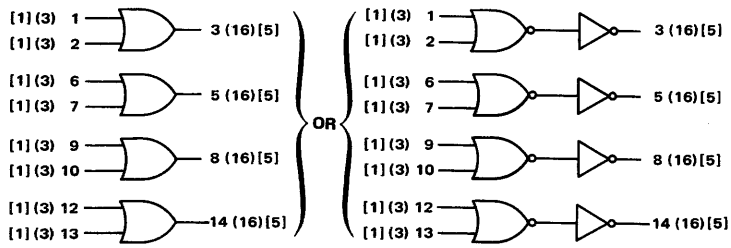
*This test includes all gates (13 mAdc per gate).

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



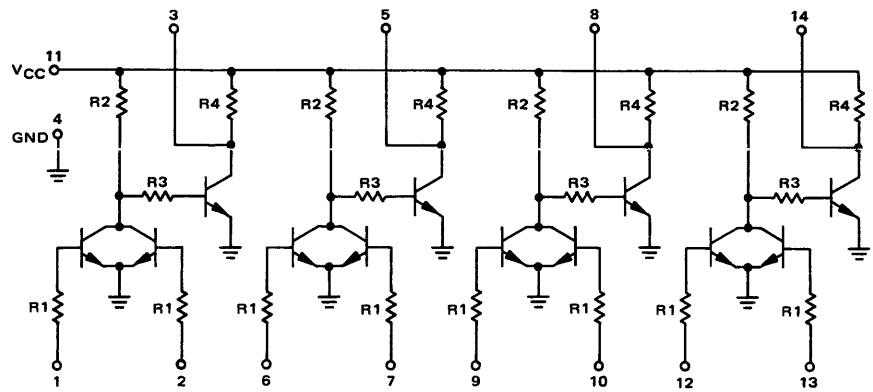
MC9715P • MC9815P

MC9715P/9815P provides increased logic flexibility, quad 2-input OR gates housed in a single 14-pin dual in-line plastic package.



P_D = 100 mW typ (Inputs Low)
= 28 mW typ (Inputs High)
Operating f = 14 MHz typ

Number In Parenthesis Indicates mW MRTL Loading Factor.
Number In Brackets Indicates MRTL Loading Factor.



TYPICAL RESISTANCE VALUES

R1 = 450 Ω	R3 = 500 Ω
R2 = 1.8 k	R4 = 640 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC9815P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC9715P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

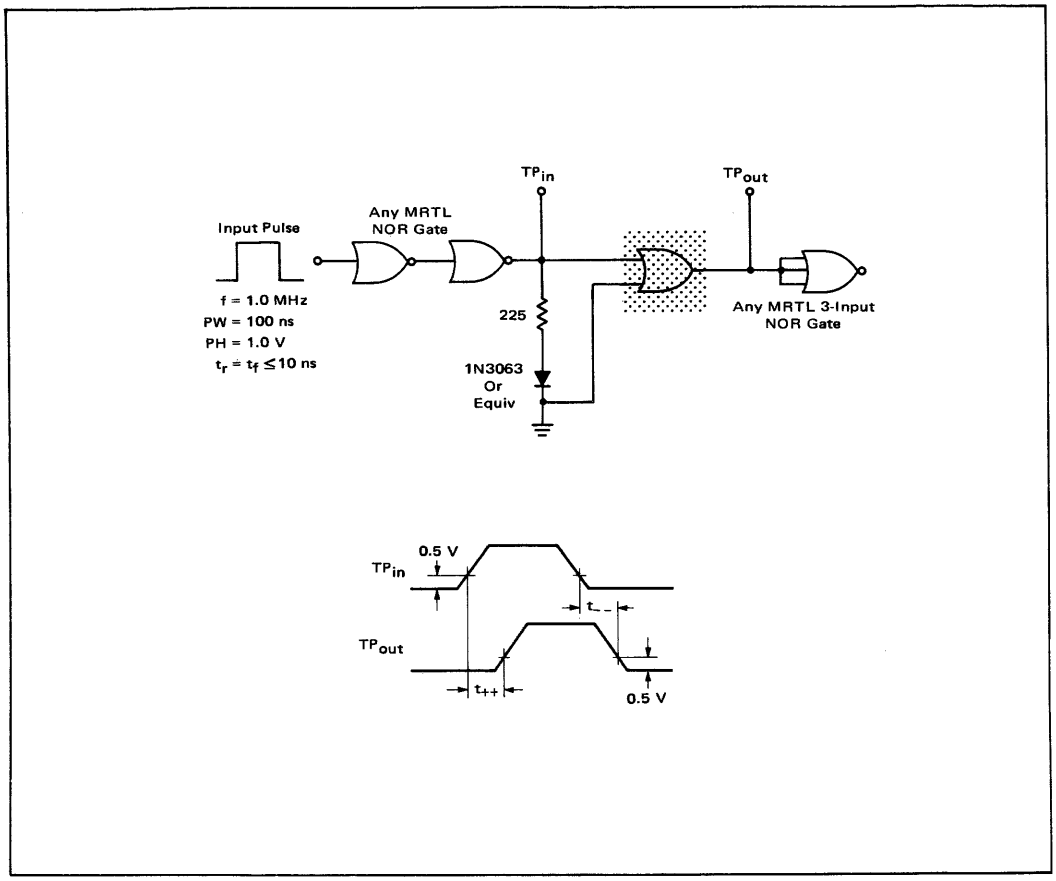
Characteristic	Symbol	Pin Under Test	MC9815P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9715P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	4
		2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	1	-	11	4
Output Current	I_{A5}	3	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	1,3	-	-	11	4
Output Voltage	V_{out}	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	-	1,2	11	4
Power Supply Drain Current	I_{PD1}	11	-	-	-	9.5	-	-	mAdc	-	-	-	9.5	-	-	mAdc	-	-	*	-	11	4
	I_{PD2}	11	-	-	-	33	-	-	mAdc	-	-	-	33	-	-	mAdc	-	-	-	-	11	4**
Switching Times																	Pulse In	Pulse Out				
	t_{1+3+}	3	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	1	3	-	-	11	2,4
	t_{1-3-}	↓	-	-	-	45	-	-	↓	-	-	-	45	-	-	↓	1	↓	-	-	↓	2,4
	t_{2+3+}		-	-	-	50	-	-		-	-	-	50	-	-		2		-	-		1,4
	t_{2-3-}		-	-	-	45	-	-		-	-	-	45	-	-		2		-	-		1,4

Ground unused input pins. Other pins not listed are left open.

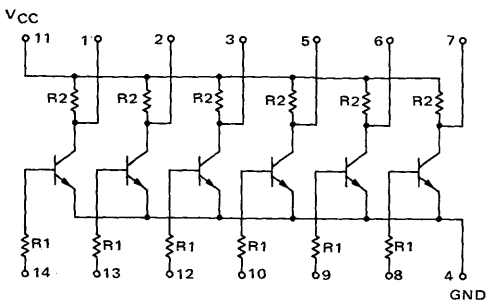
*All inputs at V_{BOT} (inputs 1, 2, 6, 7, 9, 10, 12, 13).

**All inputs at ground (inputs 1, 2, 6, 7, 9, 10, 12, 13).

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



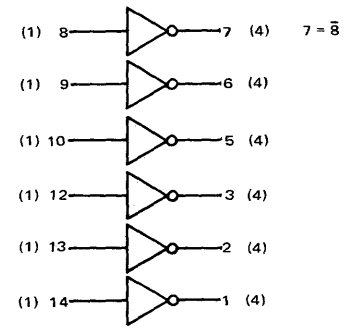
MC9718P • MC9818P



TYPICAL RESISTANCE VALUES

R1 = 1.5 k
R2 = 3.6 k

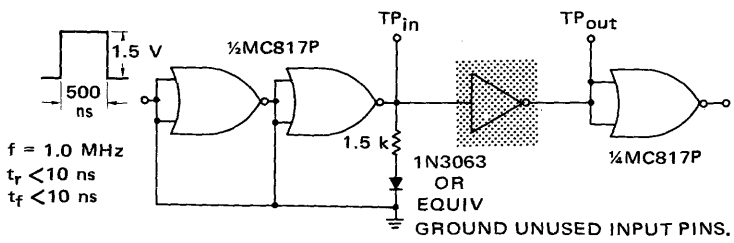
Six individual circuits are contained in a single package. Each provides the simple inversion function.

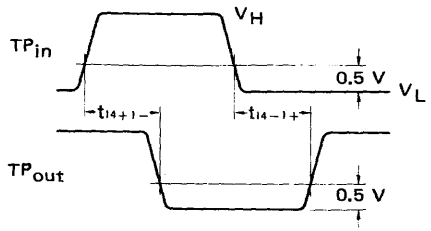


t_{pd} = 27 ns
P_D = 7.0 mW (Input High)
3.0 mW (Input Low)

Number In Parenthesis Indicates Loading Factor

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.
The other inverters are tested in the same manner.

	@ Test Temperature	V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
		TEST VOLTAGE VALUES (Volts)				
MC9818P	0°C	0.880	0.850	1.80	0.500	3.60
MC9818P	+25°C	0.830	0.800	1.80	0.460	3.60
MC9818P	+75°C	0.740	0.710	1.80	0.400	3.60
MC9718P	+15°C	0.865	0.865	1.80	0.475	3.60
MC9718P	+25°C	0.850	0.850	1.80	0.460	3.60
MC9718P	+55°C	0.800	0.800	1.80	0.430	3.60

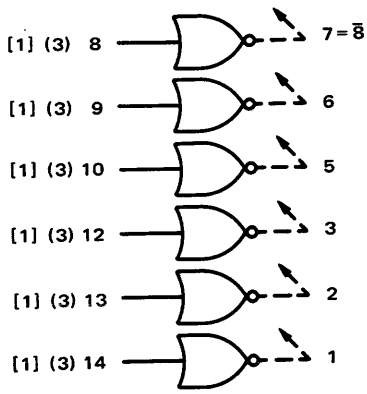
Characteristic	Symbol	Pin Under Test	MC9818P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9718P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	14*	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	14	-	*	-	11	4
Output Current	I_{A4}	1	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	1	-	-	14	11	4
Output Voltage	V_{out}	1	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	4
Saturation Voltage	$V_{CE(sat)}$	1	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	14	-	11	4
Switching Time	$t_{on} + t_{off}$	1, 14	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 14	Pulse Out 1	-	-	11	4

Ground inputs of inverters not under test. Other pins not listed are left open

* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V_{BOT}.

MC9719P • MC9819P

Six individual expanders are contained in a single package to increase the input capability of MRTL gates.

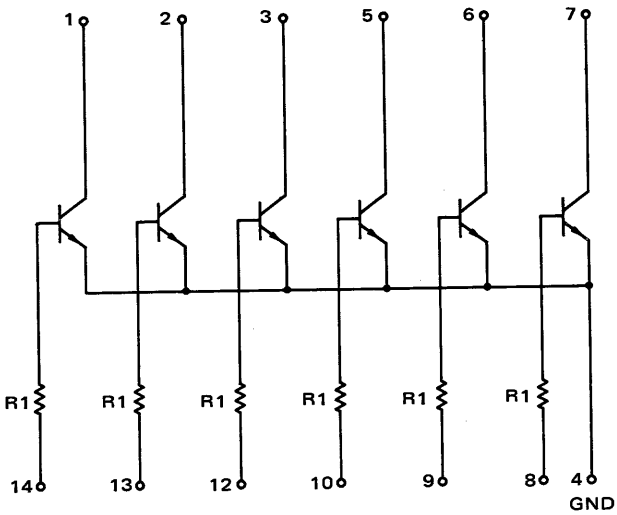


t_{pd} = 12 ns
P_D = 13 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESES
INDICATES mW MRTL LOADING FACTOR

NUMBER IN BRACKETS
INDICATES MRTL LOADING FACTOR

When an expander is added to a gate, subtract 0.4 load from the output of the gate for each expander circuit added.
SEE GENERAL INFORMATION SECTION FOR EXPANDER RULES



V_{CC} connection to pin 11 is not shown
Typical Resistance Value
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC9819P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC9719P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

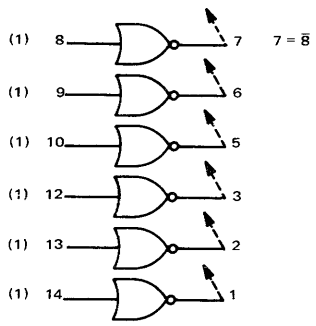
Characteristic	Symbol	Pin Under Test	MC9819P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9719P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	14	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	14	-	-	-	11	1	4
Output Leakage Current	I_{CEX}	1	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	1	-	-	14	11	-	4
Output Voltage	V_{out}	1	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1	4
Saturation Voltage	$V_{CE(sat)}$	1	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	1	4

Ground inputs of expanders not under test. Other pins not listed are left open.

* Resistor value to V_{CC}

MC9720P • MC9820P

Six individual expanders are contained in a single package to increase the input capability of the mW MRTL gates.

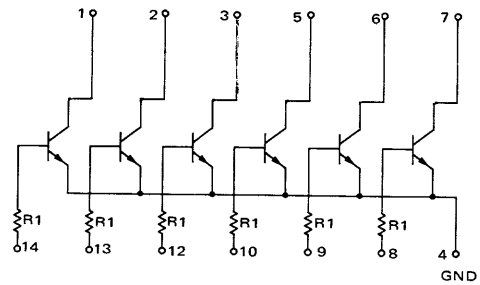


t_{pd} = 12 ns
P_D = 30 mW (Inputs High)
Negligible (Inputs Low)

Number In Parenthesis Indicates Loading Factor.

NOTES ON THE USE OF THE MC9720/9820

1. The input loading factor of the expanded gate is 1.33.
2. Pin 11 of the expander must be connected to V_{CC}.
3. The output loading factor of the expander gate is decreased 0.5 load for every added node.



CONNECTION TO V_{CC} NOT SHOWN
TYPICAL RESISTANCE VALUES
R1 = 1.5 kΩ

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

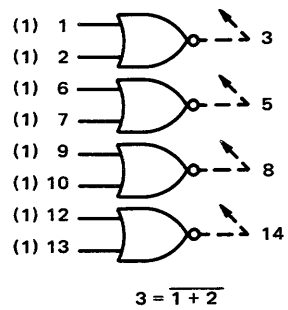
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(k Ohms) V_R*
MC9820P	0°C	0.880	0.850	1.80	0.500	3.60	3.6
	+25°C	0.830	0.800	1.80	0.460	3.60	3.6
	+75°C	0.740	0.710	1.80	0.400	3.60	4.0
MC9720P	+15°C	0.865	0.865	1.80	0.475	3.60	3.6
	+25°C	0.850	0.850	1.80	0.460	3.60	3.6
	+55°C	0.800	0.800	1.80	0.430	3.60	3.6

Characteristic	Symbol	Pin Under Test	MC9820P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9720P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	14	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	14	-	-	-	11	1	4
Output Leakage Current	I_{CEX}	1	-	25	-	25	-	30	μAdc	-	40	-	40	-	50	μAdc	1	-	-	14	11	-	4
Output Voltage	V_{out}	1	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1	4
Saturation Voltage	$V_{CE(sat)}$	1	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	14	-	11	1	4

Ground unused input pins. Other pins not listed are left open. *Resistor value to V_{CC}.

MC9721P • MC9821P

Four 2-input expanders housed in a single package increase the input capability of mW MRTL gates.



$3 = \overline{1 + 2}$

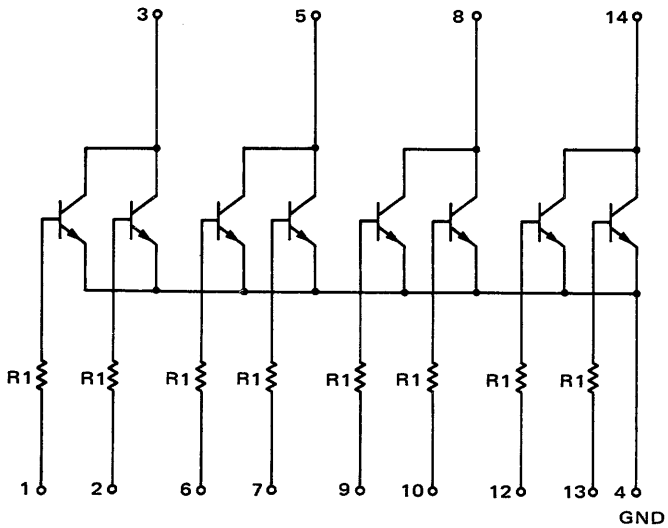
t_{pd} = 27 ns

P_D = 20 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR

NOTES ON THE USE OF THE MC9721/MC9821

1. The input loading factor of the expanded gate is 1.33.
2. Pin 11 of the expander must be connected to V_{CC}.
3. The output loading factor of the expanded gate is decreased 0.5 load for every added node.



V_{CC} connection to pin 11 is not shown
Typical Resistance Values
R1 = 1.5 k

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(kΩ) V_R*
MC9821P	0°C	0.880	0.850	1.80	0.500	3.60	3.6
	+25°C	0.830	0.800	1.80	0.460	3.60	3.6
	+75°C	0.740	0.710	1.80	0.400	3.60	4.0
MC9721P	+15°C	0.865	0.865	1.80	0.475	3.60	3.6
	+25°C	0.850	0.850	1.80	0.460	3.60	3.6
	+55°C	0.800	0.800	1.80	0.430	3.60	3.6

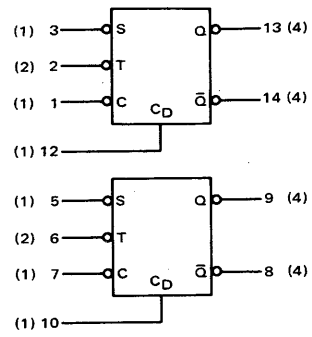
Characteristic	Symbol	Fin Under Test	MC9821P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9721P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	2	-	11	3	4
		2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	1	-	11	3	4
Output Leakage Current	I_{CEX}	3	-	25	-	25	-	30	μAdc	-	40	-	40	-	50	μAdc	3	-	-	1,2	11	-	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	3	2,4
		3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	3	1,4
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	1	-	11	3	2,4
		3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	-	11	3	1,4

Ground unused input pins. Other pins not listed are left open.

* Resistor value to V_{CC}.

MC9722P • MC9822P

MC9722P/9822P consists of two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



NUMBER IN PARENTHESIS INDICATES LOADING FACTOR

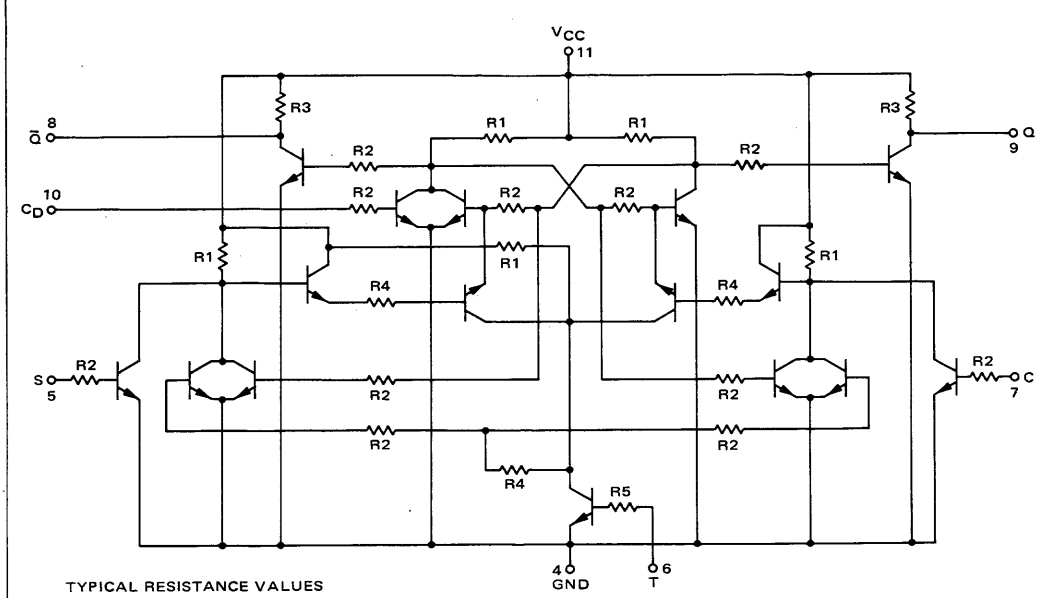
CLOCKED INPUT OPERATION ①

t_n ②		t_{n+1} ②	
S	C	Q	$\bar{Q}$
1	1	Q_n ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ③

f_{Tog} = 4.0 MHz
t_{pd} = 75 ns typ
P_D = 24 mW typ (Only Clock Input High)

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

1/2 OF CIRCUIT SHOWN

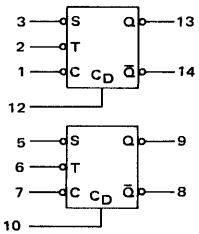


TYPICAL RESISTANCE VALUES

R1 = 4.5 k
R2 = 1.5 k
R3 = 3.6 k
R4 = 2.0 k
R5 = 750Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only. The other flip-flop is tested in the same manner.



@ Test Temperature		TEST VOLTAGE VALUES: Volts V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Pulse C_P
MC9822P	0°C	0.880	0.850	1.80	0.500	3.60	V_{in} to V_{off}
	+25°C	0.830	0.800	1.80	0.460	3.60	V_{in} to V_{off}
	+75°C	0.740	0.710	1.80	0.400	3.60	V_{in} to V_{off}
MC9722P	+15°C	0.865	0.865	1.80	0.475	3.60	V_{in} to V_{off}
	+25°C	0.850	0.850	1.80	0.460	3.60	V_{in} to V_{off}
	+55°C	0.800	0.800	1.80	0.430	3.60	V_{in} to V_{off}

Characteristic	Symbol	Pin Under Test	MC9822P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9722P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	C_P	Gnd
Input Current	I_{in}	5	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	5	-	10	-	11	-	4
		7	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	7	-	-	-	↓	-	↓
		10	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		10	-	-	-		-	
	2_{in}	6	-	300	-	280	-	280	↓	-	300	-	300	-	300	↓	6	-	5,7	-	↓	-	↓
Output Current	I_{A4}	8	-570	-	-570	-	-535	-	μAdc	-570	-	-570	-	-570	-	μAdc	-	8,10	-	-	11	-	4
		9*	-570	-	-570	-	-535	-	μAdc	-570	-	-570	-	-570	-	μAdc	-	9	-	-	11	-	4
																	P_{in} 1		P_{in} 2			P_{in} 3	
Output Voltage	V_{out}	8④	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	5	-	6	7	11	-	4,10
		9⑤	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	5	7	↓	-	↓	-	↓
		9④	-		-		-			-		-		-			-	-		5		7	
		8⑤	-		-		-			-		-		-			-	5		-		7	
		9⑥	-		-		-			-		-		-			5	7		-		-	
		8⑦	-		-		-			-		-		-			5	-		7		-	
		8⑥	-		-		-			-		-		-			-	5		-		7	
		9⑦	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	↓	5	↓	7	↓

Ground inputs of flip-flop not under test. Other pins not listed are left open.

*Preset the device as follows: a. Momentarily apply V_{BOT} to pin 10, this preclears the flip-flop.
b. Remove V_{BOT}, ground pins 5 and 7.
c. Apply negative-going clock pulse (C_P) to pin 6 while pins 5 and 7 are still grounded. (This changes the state of the flip-flop to a set condition.)
d. Remove ground from pins 5 and 7.

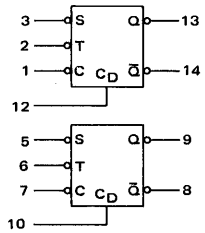
**Apply V_{BOT} momentarily prior to arrival of clock pulse (C_P) to change the state of the flip-flop.

④ See Figure 4
⑤ See Figure 5
⑥ See Figure 6
⑦ See Figure 7

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for one flip-flop only. The other flip-flop is tested in the same manner.



@ Test Temperature		TEST VOLTAGE VALUES: Volts V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Pulse C_P
MC9822P	0°C	0.880	0.850	1.80	0.500	3.60	V_{in} to V_{off}
	+25°C	0.830	0.800	1.80	0.460	3.60	V_{in} to V_{off}
	+75°C	0.740	0.710	1.80	0.400	3.60	V_{in} to V_{off}
MC9722P	+15°C	0.865	0.865	1.80	0.475	3.60	V_{in} to V_{off}
	+25°C	0.850	0.850	1.80	0.460	3.60	V_{in} to V_{off}
	+55°C	0.800	0.800	1.80	0.430	3.60	V_{in} to V_{off}

Characteristic	Symbol	Pin Under Test	MC9822P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9722P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	C_P	Gnd
Saturation Voltage	$V_{CE(sat)}$	8	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	5	10**	7	11	6	4
		9*	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	10	-	-	↓	*	↓
		8	-		-		-			-		-		-			-	-	10**	5,7		6	
		9	-		-		-			-		-		-			-	5,7	10**	-		↓	
		8*	-		-		-			-		-		-			-	5,7	-	-			
		9*	-		-		-			-		-		-			-	7	-	5			
		9*	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	5,7	↓	↓	↓
																	Pulse In	Pulse Out					
Toggle Frequency	f_{tog}	9	-	-	-	4.0	-	-	MHz	-	-	-	4.0	-	-	MHz	6	9	-	-	11	-	4,7,10

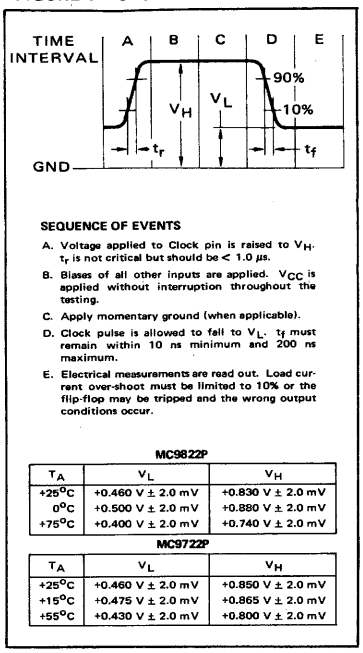
Ground inputs of flip-flop not under test. Other pins not listed are left open.

*Preset the device as follows: a. Momentarily apply V_{BOT} to pin 10, this preclears the flip-flop.
b. Remove V_{BOT}, ground pins 5 and 7.
c. Apply negative-going clock pulse (C_P) to pin 6 while pins 5 and 7 are still grounded. (This changes the state of the flip-flop to a set condition.)
d. Remove ground from pins 5 and 7.

**Apply V_{BOT} momentarily prior to arrival of clock pulse (C_P) to change the state of the flip-flop.

④ See Figure 4
⑤ See Figure 5
⑥ See Figure 6
⑦ See Figure 7

FIGURE 1 – CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be < 1.0 µs.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC9822P

T_A	V_L	V_H
+25°C	+0.460 V ± 2.0 mV	+0.830 V ± 2.0 mV
0°C	+0.500 V ± 2.0 mV	+0.880 V ± 2.0 mV
+75°C	+0.400 V ± 2.0 mV	+0.740 V ± 2.0 mV

MC9722P

T_A	V_L	V_H
+25°C	+0.460 V ± 2.0 mV	+0.850 V ± 2.0 mV
+15°C	+0.475 V ± 2.0 mV	+0.865 V ± 2.0 mV
+55°C	+0.430 V ± 2.0 mV	+0.800 V ± 2.0 mV

FIGURE 2 – TOGGLE MODE TEST CIRCUIT

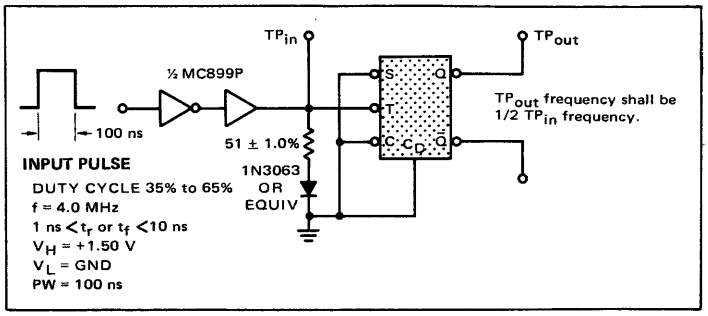


FIGURE 3 – TEST CIRCUIT

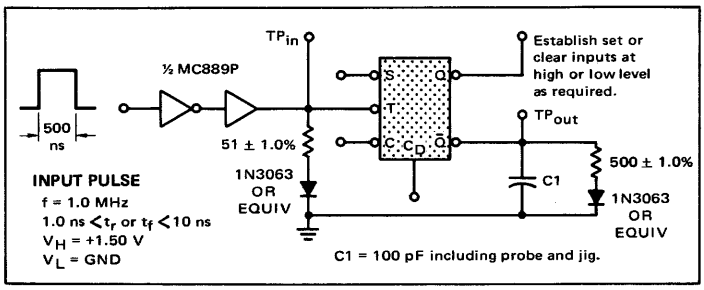


FIGURE 4 – TEST WAVEFORMS

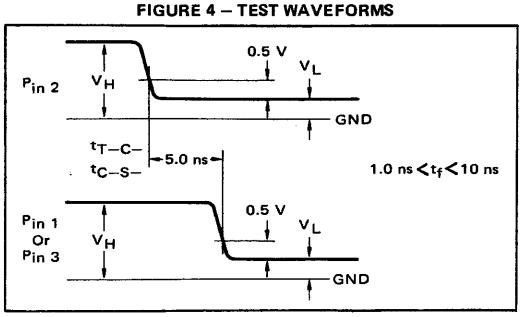


FIGURE 5 – TEST WAVEFORMS

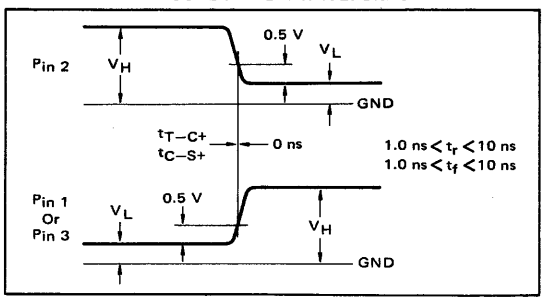


FIGURE 6 – TEST WAVEFORMS

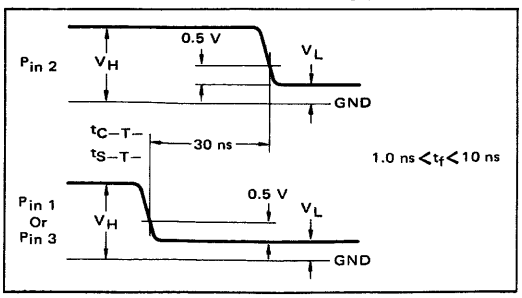
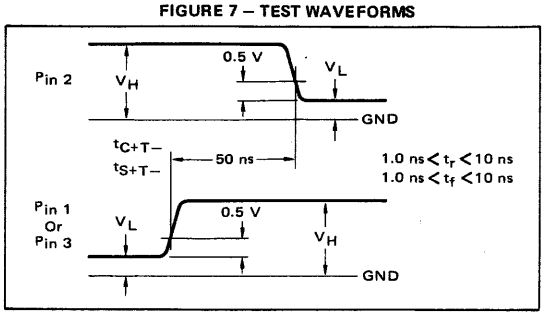


FIGURE 7 – TEST WAVEFORMS



BCD-TO-DECIMAL
DECODER-DRIVER

MC9760P • MC9860P†

The MC9760P/MC9860P monolithic BCD-to-Decimal Decoder/Driver is designed for use with high-voltage neon indicating tubes. The high-voltage output transistors can withstand 70-volts (MC9860P), and 65-volts (MC9760P), insuring direct operation of the indicator tubes without background glow. The inputs are compatible with MRTL logic functions.

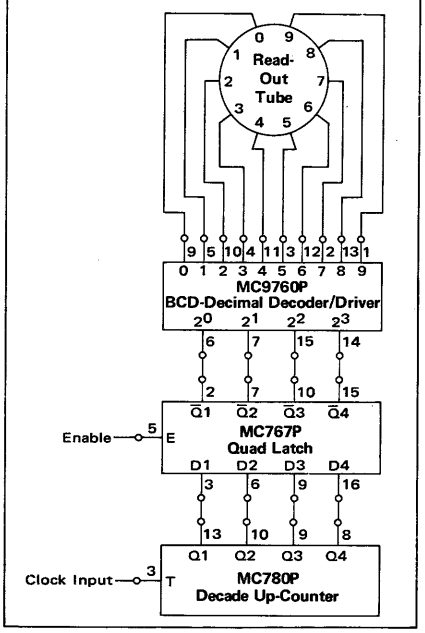
TRUTH TABLE

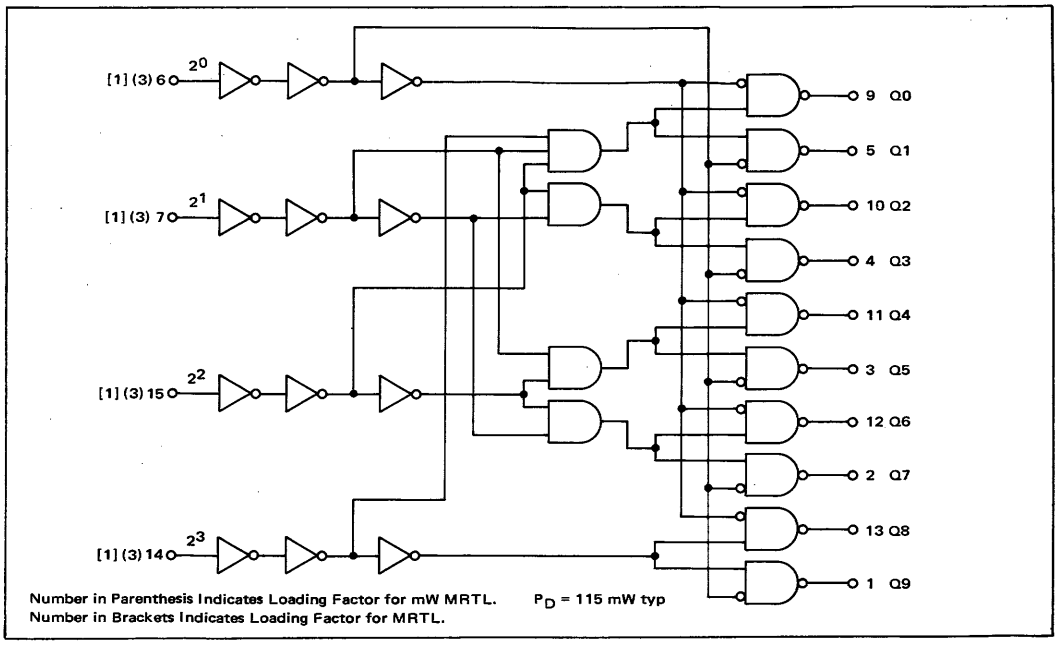
	INPUT* (BCD)				OUTPUT (DECIMAL)								
Value	2^0	2^1	2^2	2^3	0	1	2	3	4	5	6	7	8	9
Pin No.	6	7	15	14	9	5	10	4	11	3	12	2	13	1
Logic Levels	1	1	1	1	0	1	1	1	1	1	1	1	1	1
	0	1	1	1	1	0	1	1	1	1	1	1	1	1
	1	0	1	1	1	1	0	1	1	1	1	1	1	1
	0	0	1	1	1	1	1	0	1	1	1	1	1	1
	1	1	0	1	1	1	1	1	0	1	1	1	1	1
	0	1	0	1	1	1	1	1	1	0	1	1	1	1
	1	0	0	1	1	1	1	1	1	1	0	1	1	1
	0	0	0	1	1	1	1	1	1	1	1	0	1	1
	1	1	1	0	1	1	1	1	1	1	1	1	0	1
	0	1	1	0	1	1	1	1	1	1	1	1	1	0

Logic "0" ≤1.5 Vdc @ 6.0 mA
Logic "1" ≥65 Vdc (MC9760)
Logic "1" ≥70 Vdc (MC9860)

*Any input configuration not shown results in an indeterminate state at the outputs.

TYPICAL INTERCONNECTION DIAGRAM

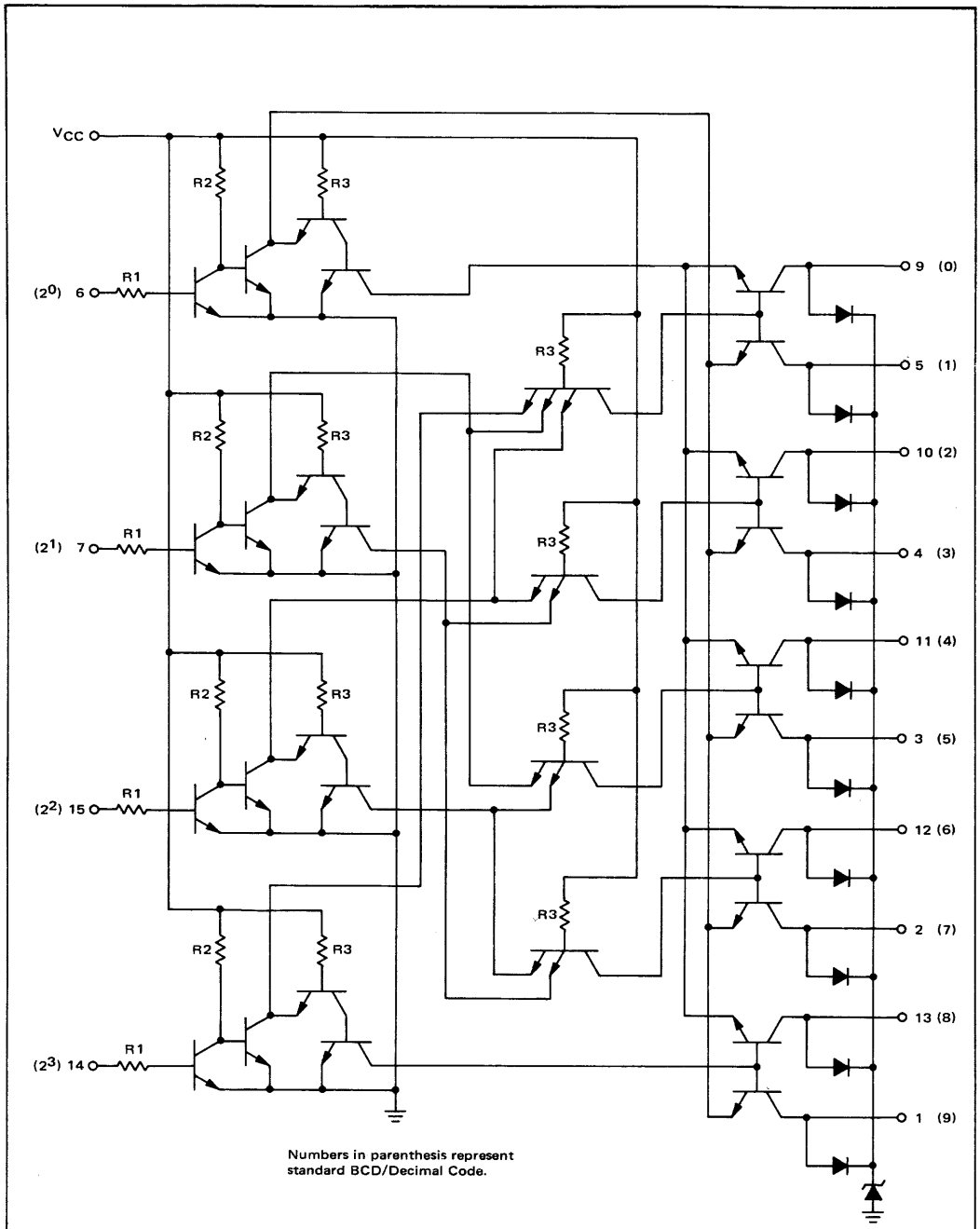




Number in Parenthesis Indicates Loading Factor for mW MRTL.
Number in Brackets Indicates Loading Factor for MRTL.

P_D = 115 mW typ

†See General Information section for packaging.



Numbers in parenthesis represent standard BCD/Decimal Code.

TYPICAL RESISTANCE VALUES

R1 = 450Ω
R2 = 640Ω
R3 = 3.75 k

ELECTRICAL CHARACTERISTICS

@ Test Temperature		V_{in}	V_{on}	V_{CEX}	I_A	I_L	V_{CC}
MC9860P	0°C	0.960	0.930	40	6.0	5.0	3.6
	+25°C	0.910	0.880	40	6.0	5.0	3.6
	+75°C	0.820	0.790	40	6.0	5.0	3.6
MC9760P	+15°C	1.05	1.05	40	6.0	5.0	3.6
	+25°C	1.00	1.00	40	6.0	5.0	3.6
	+55°C	0.95	0.95	40	6.0	5.0	3.6

TEST VOLTAGE/CURRENT VALUES (Vdc/mAdc)

Characteristic	Symbol	Pin Under Test	MC9860P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9760P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW V_{in}	V_{on}	V_{CEX}	I_A	I_L	V_{CC}	Gnd
Input Current	I_{in}	6	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	6	-	-	-	-	16	8
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	7	-	-	-	-	↓	↓
		14	-		-		-			-		-		-			14	-	-	-	-		
		15	-	▼	-	▼	-	▼	▼	-	▼	-	▼	-	▼	▼	15	-	-	-	-	▼	▼
Output Voltage	V_{out}	1	-	1.5	-	1.5	-	1.5	Vdc	-	1.5	-	1.5	-	1.5	Vdc	-	*	-	1	-	16	8*
Output Leakage Current	I_{CEX}	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc	-	**	1	-	-	16	8**
Output Breakdown Voltage	BV_{CEX}	1	70	-	70	-	70	-	Vdc	65	-	65	-	65	-	Vdc	-	6,7,14,15	-	-	1	16	8
		2		-		-		-			-		-		-		-	↓	-	-	2	↓	↓
		3		-		-		-			-		-		-		-		-	-	3		
		4		-		-		-			-		-		-		-		-	-	4		
		5		-		-		-			-		-		-		-	▼	-	-	5		▼
		9		-		-		-			-		-		-		-	14,15	-	-	9		6,7,8
		10		-		-		-			-		-		-		-	↓	-	-	10		↓
		11		-		-		-			-		-		-		-		-	-	11		
		12		-		-		-			-		-		-		-		-	-	12		
		13	▼	-	▼	-	▼	-	▼	▼	-	▼	-	▼	-	▼	-	▼	-	-	13	▼	▼
Power Supply Current Drain	I_{PD}	16	-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc	-	6,7,14,15	-	-	-	16	8

*I_A is applied to pin under test – V_{on} and gnd are applied to inputs in accordance with truth table for "on" condition of pin under test (1 test for each output).

**V_{CEX} is applied to pin under test – V_{on} and gnd are applied to inputs in accordance with truth table for "off" conditions of pin under test (9 tests for each output).

Other pins not listed are left open.