MOTOROLA Semiconductor Products Inc.

TTL
INTEGRATED CIRCUITS
DATA BOOK

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This book presents technical data for a broad line of TTL integrated circuits. Complete specifications for the individual monolithic circuits in the most popular TTL families are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of any manufacturer.

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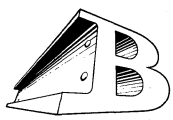


TTL

CROSS REFERENCE

The following listings of TTL devices indicate the Motorola replacement for most TTL devices available. Devices are referenced to the prime source only – not to any manfuacturer who may be a second source.

In some cases a Motorola suggested alternate is given. These parts have pinout and/or specification differences and therefore are not exact replacements. The alternate will generally vary by pinouts, function, or specifications. In many cases the alternate offers improved performance.

FAMILIES REFERENCED

Manufacturer	Series Number
Texas Instruments	SN54/74 SN54H/74H
Fairchild	9000/9300
Signetics	8200/7200 8800 8H00
National	8200 8500 8600 8800
Sylvania	SUHL I & II

SERIES 54/74 TTL

TEXAS INSTRUMENTS TO MOTOROLA

TEMPERATURE RANGE CROSS REFERENCE

Temperature Range	T.I.	Motorola
0°C to +70°C	SN74xx	MC74xx
−55°C to +125°C	SN54xx	MC54xx

PACKAGE CROSS REFERENCE

Package	T.I.	Motorola	Comments
Flat Ceramic (1/4" x 1/8", 1/2" leads)	F	Special	
Dual In-Line Ceramic	J	L	
Dual In-Line Plastic	N	P	
Flat Ceramic (1/4" x 1/8", 1" leads)	S	F	Motorola Package is 1/4" x 1/4"

DEVICE CROSS REFERENCE

Type	Function	Direct Replacement	Suggested Alternate	Comments
SN7400	Quad 2-Input NAND Gate	MC7400	—	
SN7401	Quad 2-Input NAND Gate (Open Collector)	MC7401	—	
SN7402	Quad 2-Input NOR Gate	MC7402	—	
SN7403	Quad 2-Input NOR Gate (Open Collector)	MC7403	—	
SN7404	Hex Inverter	MC7404	—	
SN7405	Hex Inverter (Open Collector)	MC7405	—	
SN7406	Hex Inverter Buffer/Driver (Open Collector)	MC7406*	—	
SN7407	Hex Buffer/Driver (Open Collector)	MC7407*	—	
SN7408	Quad 2-Input AND Gate	MC7408*	—	
SN7410	Triple 3-Input NAND Gate	MC7410	—	
SN7412	Triple 3-Input NAND Gate (Open Collector)	—	MC3007	
SN7413	Dual 4-Input NAND Schmitt Trigger	—	—	
SN7416	Hex Inverter Buffer/Driver (Open Collector)	MC7416*	—	
SN7417	Hex Buffer/Driver (Open Collector)	MC7417*	—	
SN7420	Dual 4-Input NAND Gate	MC7420	—	
SN7423	Expandable Dual 4-Input NOR Gate with Enable	—	—	
SN7425	Dual 4-Input NOR Gate with Enable	—	—	
SN7426	Quad 2-Input High-Voltage Interface NAND Gate	MC7426	—	Both devices have output breakdown voltage = 30V
SN7427	Triple 3-Input NOR Gate	—	—	
SN7430	8-Input NAND Gate	MC7430	—	
SN7432	Quad 2-Input OR Gate	—	MC3003	
SN7437	Quad 2-Input NAND Buffer	—	—	
SN7438	Quad 2-Input NAND Buffer (Open Collector)	—	—	
SN7440	Dual 4-Input NAND Buffer	MC7440	—	
SN7441A	BCD-to-Decimal Decoder/Driver	MC7441A	—	MC7441A has zener clamped outputs, Nixie® display driver. V_{out} = 55 V
SN7442	BCD-to-Decimal Decoder	MC7442	—	
SN7443	Excess 3-to-Decimal Decoder	MC7443	—	
SN7444	Excess 3 Gray-to-Decimal Decoder	MC7444	—	
SN7445	BCD-to-Decimal Decoder/Driver	MC7445	—	
SN7446	BCD-to-Seven Segment Decoder/Driver	MC7446	MC8317B*	V_{out} = 30 V, I_{out} = 20 mA } MC7446 V_{out} = 40 V, I_{out} = 20 mA } MC8317B

*To be introduced

SERIES 54/74 TTL DEVICE CROSS REFERENCE (cont)

Type	Function	Direct Replacement	Suggested Alternate	Comments
SN7447	BCD-to-Seven Segment Decoder/Driver	MC7447	MC8317D* MC4039	V_{out} = 15 V, I_{out} = 20 mA } MC7447 V_{out} = 20 V, I_{out} = 20 mA } MC8317D
SN7448	BCD-to-Seven Segment Decoder	MC7448	MC8307*	
SN7449	BCD-to-Seven Segment Decoder	MC7449	—	
SN7450	Expandable Dual 2-Wide 2-Input AOI Gate	MC7450	—	
SN7451	Dual 2-Wide 2-Input AOI Gate	MC7451	—	
SN7453	Expandable 4-Wide 2-Input AOI Gate	MC7453	—	
SN7454	4-Wide 2-Input AOI Gate	MC7454	—	
SN7460	Dual 4-Input Expander	MC7460	—	
SN7470	J-K Flip-Flop	MC7470	MC3052	
SN7472	J-K Flip-Flop	MC7472	MC3050	MC3050 is edge triggered
SN7473	Dual J-K Flip-Flop	MC7473	MC3061	MC3061 f_{Tog} = 40 MHz, edge triggered
SN7474	Dual Type D Flip-Flop	MC7479	—	MC7479 has buffered outputs, Set-Reset override clock.
SN7475	Quad Latch	MC7475	MC4015	MC4015 is quad edge-triggered flip-flop
SN7476	Dual J-K Flip-Flop	MC7476	—	
SN7477	Quad Latch	MC7477	—	14-pin flat pack only
SN7480	Gated Full Adder	MC7480	—	
SN7481	16-Bit Memory	MC4004	MC4005	MC4005 I_{out} = 20 mA
SN7482	2-Bit Adder	MC17482	MC27482	MC17482 faster, slightly different loading. MC27482 has exclusive OR outputs for look-ahead carry schemes.
SN7483	4-Bit Adder	MC7483	MC8260	MC8260 has greater functional capability.
SN7484	Gated-Input 16-Bit Memory	MC7484	—	
SN7485	4-Bit Comparator	—	MC4022	
SN7486	Quad Exclusive OR Gate	—	MC3021	MC3021 is pin compatible, I_F = 3.0 mA; 7486 I_F = 1.6 mA
SN7488	256-Bit Read Only Memory	—	—	
SN7489	64-Bit Random Access Memory	—	MCM4064	
SN7490	Decade Counter	MC7490	MC4023	MC4023 f_{Tog} = 30 MHz, multicount capability
SN7491A	8-Bit Shift Register	MC7491A	—	
SN7492	Divide-by-12 Counter	MC7492	MC4023	MC4023 f_{Tog} = 30 MHz, multicount capability
SN7493	4-Bit Binary Counter	MC7493	—	
SN7494	4-Bit Shift Register	MC7494*	MC4015	MC4015 higher speed, lower power
SN7495	4-Bit Universal Shift Register	MC7495	MC4012	MC4012 f_{Tog} = 30 MHz, P_D = 180 mW
SN7496	5-Bit Shift Register	MC7496	—	
SN74100	8-Bit Bistable Latch	MC74100*	—	
SN74104	J-K Flip-Flop	—	—	
SN74105	J-K Flip-Flop	—	—	
SN74107	Dual J-K Flip-Flop	MC74107	MC7474	MC7474 has V_{CC} on Pin 14, Gnd on Pin 7
SN74110	J-K Flip-Flop	—	—	
SN74111	J-K Flip-Flop	—	—	
SN74121	Monostable Multivibrator	MC74121		
SN74122	Retriggerable Monostable Multivibrator	—	MC8601	
SN74123	Dual Retriggerable Monostable Multivibrator	—	MC8602*	
SN74141	BCD-to-Decimal Decoder	—	—	

*To be introduced

SERIES 54/74 TTL DEVICE CROSS REFERENCE (cont)

Type	Function	Direct Replacement	Suggested Alternate	Comments
SN74145	BCD-to-Decimal Decoder/Driver	MC74145	—	
SN74150	16-Bit Data Selector	MC74150*	—	
SN74151	8-Bit Data Selector	MC74151*	MC8312	
SN74152	8-Bit Data Selector	MC74152*	MC8312	
SN74153	Dual 4-Bit Data Selector	MC74153*	MC4000	MC4000 t_{pd} = 18 ns, P_D = 150 mW
SN74154	One-of-16 Decoder	MC8311	—	
SN74155	Dual One-of-Four Line Decoder	MC74155*	MC4007	MC4007 t_{pd} = 14 ns, P_D = 125 mW
SN74156	Dual Two-to-Four Line Decoder (Open Collector)	MC74156*	—	
SN74160	BCD Counter	MC9310	—	
SN74161	Synchronous 4-Bit Binary Counter	MC9316	—	
SN74162	Synchronous 4-Bit Decade Counter	—	—	
SN74163	Synchronous 4-Bit Binary Counter	—	—	
SN74164	8-Bit Serial-In/Parallel-Out Shift Register	MC74164*	—	
SN74165	8-Bit Parallel-In/Serial-Out Shift Register	MC74165*	—	
SN74166	Synchronous 8-Bit Shift Register	—	—	
SN74170	4-by-4 Register File	—	—	
SN74180	8-Bit Parity Generator	MC74180*	—	
SN74181	Arithmetic Logic Unit	MC74181*	MC7260*	
SN74182	Carry Generator	MC74182*	MC7261*	
SN74185	Binary-to-BCD Converter	—	MC4001	MC4001 expandable to any number of bits. Converts BCD to Binary or Binary to BCD
SN74190	Synchronous Decade Up/Down Counter	—	—	
SN74191	Synchronous 4-Bit Binary Up/Down Counter	—	—	
SN74192	Synchronous Decade Counter	MC74192*	—	
SN74193	Synchronous Binary Counter	MC74193*	—	
SN74196	50-MHz BCD Counter	—	MC8280*	
SN74197	50-MHz Presettable Binary Counter	—	MC8316 MC8291*	
SN74198	8-Bit Parallel In-Out Left-Right Shift Register	—	—	
SN74199	8-Bit Parallel In-Out J-K Input Shift Register	—	—	

*To be introduced

SERIES 54H/74H (MC3000) TTL

TEXAS INSTRUMENTS TO MOTOROLA

TEMPERATURE RANGE CROSS REFERENCE

Temperature Range	T.I.	Motorola
0°C to +70°C	74Hxx	MC30xx
−55°C to +125°C	54Hxx	MC31xx

PACKAGE CROSS REFERENCE

Package	T.I.	Motorola	Comments
Flat Ceramic (1/4" x 1/8", 1/2" leads)	F	Special	
Dual In-Line Ceramic	J	L	
Dual In-Line Plastic	N	P	
Flat Ceramic (1/4" x 1/8", 1" leads)	S	F	Motorola Package is 1/4" x 1/4"

DEVICE CROSS REFERENCE

Type	Function	Direct Replacement	Suggested Alternate
SN74H00	Quad 2-Input NAND Gate	MC3000	—
SN74H01	Quad 2-Input NAND Gate (Open Collector)	MC3004	—
SN74H04	Hex Inverter	MC3008	—
SN74H05	Hex Inverter (Open Collector)	MC3009	—
SN74H08	Quad 2-Input AND Gate	MC3001	—
SN74H10	Triple 3-Input NAND Gate	MC3005	—
SN74H11	Triple 3-Input AND Gate	MC3006	—
SN74H20	Dual 4-Input NAND Gate	MC3010	—
SN74H21	Dual 4-Input AND Gate	MC3011	—
SN74H22	Dual 4 Input NAND Gate (Open Collector)	MC3012	—
SN74H30	8-Input NAND Gate	MC3016	—
SN74H40	Dual 4-Input NAND Buffer	MC3024	—
SN74H50	Expandable Dual 2-Wide 2-Input AOI Gate	MC3020	—
SN74H51	Dual 2-Wide 2-Input AOI Gate	MC3023	—
SN74H52	Expandable 4-Wide 2-2-2-3 Input AND-OR Gate	MC3031	—
SN74H53	Expandable 4-Wide 2-2-2-3 Input AOI Gate	MC3032	—
SN74H54	4-Wide 2-2-2-3 Input AOI Gate	MC3033	—
SN74H55	Expandable 2-Wide 4-Input AOI Gate	MC3034	—
SN74H60	Dual 4-Input Expander	MC3030	—
SN74H61	Triple 3-Input Expander	MC3019	—
SN74H62	4-Wide 3-2-2-3 Input Expander	MC3018	—
SN74H71	J-K Flip-Flop	MC3054	—
SN74H72	J-K Flip-Flop	MC3055	—
SN74H73	Dual J-K Flip-Flop	MC3063	—
SN74H74	Dual Type D Flip-Flop	—	MC3060
SN74H76	Dual J-K Flip-Flop	—	MC3062, MC3063
SN74H78	Dual J-K Flip-Flop	—	MC3061
SN74H101	J-K Flip-Flop	—	MC3054
SN74H102	J-K Flip-Flop	—	MC3055
SN74H103	Dual J-K Flip-Flop	—	MC3063
SN74H106	Dual J-K Flip-Flop	—	MC3062, MC3063
SN74H108	Dual J-K Flip-Flop	—	MC3061

9000/9300 SERIES TTL

FAIRCHILD TO MOTOROLA

PACKAGE AND TEMPERATURE RANGE CROSS REFERENCE

Package	Temperature Range	Fairchild	Motorola
14-Pin Flat Ceramic (1/4" x 1/4")	0°C to +75°C	U3I9xxx59x	MC8xxxF
14-Pin Flat Ceramic (1/4" x 1/4")	−55°C to +125°C	U3I9xxx51x	MC9xxxF
16-Pin Flat Ceramic (1/4" x 3/8")	0°C to +75°C	U4L9xxx59x	MC8xxxF
16-Pin Flat Ceramic (1/4" x 3/8")	−55°C to +125°C	U4L9xxx51x	MC9xxxF
14-Pin Dual In-Line Ceramic	0°C to +75°C	U6A9xxx59x	MC8xxxL
14-Pin Dual In-Line Ceramic	−55°C to +125°C	U6A9xxx51X	MC9xxxL
16-Pin Dual In-Line Ceramic	0°C to +75°C	U6B9xxx59x	MC8xxxL
16-Pin Dual In-Line Ceramic	−55°C to +125°C	U6B9xxx51x	MC9xxxL

DEVICE CROSS REFERENCE

Type	Function	Direct Replacement	Suggested Alternate	Comments
9000	J-K Flip Flop	—	MC3051	MC3051 is edge triggered
9001	J-$\overline{K}$ Flip Flop	MC3052†	—	
9002	Quad 2-Input NAND Gate	MC7400#†	MC3000	MC3000 has superior characteristics
9003	Triple 3-Input NAND Gate	MC7410#†	MC3005	Active bypass
9004	Dual 4-Input NAND Gate	MC7420#†	MC3010	Improved power vs. frequency characteristic
9005	Dual Expandable AOI Gate	MC7450#†	MC3020	Direct pin replacement for DIL and flat pack
9006	Dual Expander	MC7460#†	MC3030	
9007	8-Input NAND Gate	—	MC3015	MC3015 pin compatible with 9007
9008	4-Wide Expandable AOI Gate	—	MC7453#/	MC7453 is 2-2-2-2 Input 9008 is 2-2-2-3 Input
9009	Dual 4-Input Buffer	MC7440#†	MC3024	
9014	Quad Exclusive OR Gate	—	MC3021	
9015	Quad NOR Gate	—	MC3002	
9016	Hex Inverter	MC7404†	MC3024	
9017	Hex Inverter (Open Collector)	—	MC7405, MC3009	
9020	Dual J-K Flip Flop	—	MC3061	Edge triggered
9022	Dual J-K Flip Flop	—	MC3062	High speed (50 MHz)
9024	Dual J-K Flip Flop	—	MC3060	
9033	16-Bit Memory	—	MC4004	MC4004: V_{CC} = Pin 4 Gnd = Pin 10
9034	256-Bit Read Only Memory	MCM4002	—	Optional pullup resistors to facilitate wire OR outputs (custom metalization)
9035	64-Bit Memory	—	MCM4064	
9300	4-Bit Shift Register	MC9300	MC4012	MC4012 P_D = 180 mW, f_{Tog} = 30 MHz
9301	BCD-to-Decimal Decoder	MC9301	—	
9304	Dual Full Adder	MC9304	—	
9306	Up/Down BCD Counter	MC9306*	MC74192	
9307	Seven-Segment Decoder	MC9307*	MC7448	Active high outputs, MC7448 is pin replacement
9308	Dual 4-Bit Latch	MC9308	—	
9309	Dual 4-Input Multiplexer	MC9309	MC4000	
9310	Programmable BCD Up Counter	MC9310	MC4016	MC4016 programs in binary code, counts down
9311	One-of-16 Decoder	MC9311	—	
9312	8-Input Multiplexer	MC9312	—	
9314	4-Bit Latch	MC9314*	MC4015	MC4015 Quad Type D Flip-Flop

† These devices are pinout replacements but may vary in electrical specifications
* To be introduced
#Dual in-line package only

9000/9300 SERIES TTL DEVICE CROSS REFERENCE (cont)

Type	Function	Direct Replacement	Suggested Alternate	Comments
9315	BCD-to-Decimal Decoder/Driver	MC7441A	—	Nixie® driver capability
9316	Programmable Binary Up Counter	MC9316*	MC4018	MC4018 programs in binary code, counts down
9317	Seven-Segment Decoder	MC9317*	MC7446/7	MC7446/7 pin replacements
9318	8-Input Priority Encoder	MC9318*	—	
9321	Dual One-of-Four Decoder	—	MC4007	MC4007 P_D = 125 mW, t_{pd} = 14 ns.
9322	Quad 2-Input Multiplexer	—	MC8266*	
9324	5-Bit Comparator	—	MC4022	
9325	BCD-to-Decimal Decoder/Driver	MC74141	—	
9327	Seven-Segment Decoder	—	MC7446	
9328	Dual 8-Bit Shift Register	MC9328	—	
9334	8-Bit Addressable Latch	—	—	
9337	Seven-Segment Decoder	—	—	
9338	8-Bit Multiple Register	—	—	
9340	Arithmetic Logic Unit	—	MC7260*	
9341	4-Bit Arithmetic Ligic Unit	MC74181*		
9342	Carry Extender	MC74182*	MC7261*	
9348	12-Bit Parity Tree	—	MC4008, MC4010	MC4008, 4010 expandable to any size words
9350	Decade Up Counter	—	MC4023	
9352	BCD-to-Decimal Decoder	MC7442	—	
9353	Excess 3-to-Decimal Decoder	MC7443	—	
9354	Excess 3 Gray-to-Decimal Decoder	MC7444	—	
9356	4-Bit Binary Counter	—	MC7493	
9357A	BCD-to-Seven Segment Decoder/Driver	MC7446	—	
9357B	BCD-to-Seven Segment Decoder/Driver	MC7447	—	
9358	BCD-to-Seven Segment Decoder	MC7448	—	
9359	BCD-to-Seven Segment Decoder	MC7449	—	
9360	Decade Up/Down Counter	MC74192*	—	
9366	Binary Up/Down Counter	MC74193*	—	
9375	4-Bit Latch	MC7475	—	
9377	4-Bit Latch	MC7477	—	
9380	Full Adder	MC7480	—	
9382	2-Bit Full Adder	MC7482	—	
9383	4-Bit Full Adder	MC7483	—	
9390	Decade Counter	MC7490	—	
9391	8-Bit Shift Register	MC7491	—	
9392	Divide-by-12 Counter	MC7492	—	
9393	Binary Counter	MC7493	—	
9394	4-Bit Shift Register	MC7494*	—	
9395	4-Bit Universal Shift Register	MC7495	—	
9396	5-Bit Shift Register	MC7496	—	

† These devices are pinout replacements but may vary in electrical specifications
* To be introduced
#Dual in-line package only

DCL. . . TTL

SIGNETICS TO MOTOROLA

TEMPERATURE RANGE CROSS REFERENCE (8200 SERIES ONLY)

Temperature Range	Signetics	Motorola
0°C to +75°C	N82xx	MC72xx
−55°C to +125°C	S82xx	MC82xx

PACKAGE CROSS REFERENCE

Package	Signetics	Motorola	Comments
14-Pin Dual In-Line Plastic	A	P	
16-Pin Dual In-Line Plastic	B	P	
16-Pin Dual In-Line Ceramic	E	L	
14-Pin Dual In-Line Ceramic	F	L	
14-Pin Flat Glass	J	F	Motorola package is ceramic
24-Pin Flat Ceramic	P	F	
14-Pin Flat Ceramic	Q	F	
16-Pin Flat Ceramic	R	F	
24-Pin Dual In-Line Ceramic	Y	L	

DEVICE CROSS REFERENCE

Type	Function	Direct Replacement	Suggested Alternate	Comments
N8200	Dual 5-Bit Register	—	MC4015	MC4015 Quad Flip Flop, has direct Set, Reset, 30-MHz data rate
N8202	10-Bit Register	—	MC4015	MC4015 Quad Flip Flop, has direct Set, Reset, 30-MHz data rate
N8230	8-Input Data Selector	—	MC8312, MC74151*	
N8241	Quad Exclusive OR Gate	MC7241	MC3021	
N8242	4-Bit Comparator	MC7242	MC3022	
N8250	Binary-to-Octal Decoder	MC7250*	MC4006	
N8251	BCD-to-Decimal Decoder	MC7251*	MC8301	
N8260	Arithmetic Logic Element	MC7260*	—	
N8261	Fast Carry Extender	MC7261*	—	
N8266	4-Bit 2-Input Data Selector	MC7266*	—	
N8267	4-Bit 2-Input Data Selector (Open Collector)	MC7267*	—	
N8268	Gated Full Adder	—	MC7480	
N8270	4-Bit Universal Shift Register	MC7270*	MC4012	
N8271	4-Bit Universal Shift Register	MC7271*	MC8300	
N8275	Quad Latch	—	MC7475	
N8276	8-Bit Shift Register	—	MC7491A	
N8280	Presettable Decade Counter	MC7280*	MC4016	MC4016 fully programmable
N8281	Presettable Binary Counter	MC7281*	MC4018	MC4018 fully programmable
N8284	Synchronous Binary Up/Down Counter	MC7284*	—	
N8285	Synchronous Decade Up/Down Counter	MC7285*	—	
N8288	Presettable Divide-by-12 Counter	MC7288*	MC7492	

* To be introduced
** Direct replacement can be supplied as a special.
\# Motorola flat-pack device direct replacement for Signetics flat-pack device.
\## Motorola device direct replacement in dual-in-line packages (P, L). Can supply F package as special.

DCL. . .TTL DEVICE CROSS REFERENCE (cont)

Type	Function	Direct Replacement	Suggested Alternate	Comments
N8806	Dual Expander	MC7460	—	
N8808	8-Input NAND Gate	MC7430	—	
N8816	Dual 4-Input NAND Gate	—	MC7420**#	
N8822	Dual J-K Flip Flop	—	MC7473#	
N8825	J-K Flip Flop	—	MC3051	
N8826	Dual J-K Flip Flop	—	MC3061	
N8827	Dual J-K Flip Flop	—	MC3062	
N8828	Dual Type D Flip Flop	MC7479	—	MC7479 has buffered outputs
N8829	J-K Flip Flop	MC7472	MC3051	
N8840	Dual AOI Gate	MC7450	—	
N8848	4-Wide AOI Gate	MC7453	—	
N8855	Dual 4-Input Power Gate	—	MC7440**	
N8870	Triple 3-Input NAND Gate	—	MC7410#	
N8880	Quad 2-Input NAND Gate	—	MC7400**#	
N8881	Quad 2-Input NAND Gate (Open Collector)	MC7401	—	
N8885	Quad 2-Input NOR Gate	—	MC7402	
N8H16	Dual 4-Input NAND Gate	—	MC3010##	
N8H20	Dual J-K Flip Flop	—	MC3061	MC3000 series has active bypass, improved power vs. frequency characteristic, improved t_{pd} vs. temperature.
N8H21	Dual J-K Flip Flop	—	MC3062	
N8H22	Dual J-K Flip Flop	—	—	
N8H70	Triple 3-Input NAND Gate	—	MC3005##	
N8H80	Quad 2-Input NAND Gate	—	MC3000##	
N8H90	Hex Inverter	—	MC3008##	

* To be introduced

** Direct replacement can be supplied as a special.

Motorola flat-pack device direct replacement for Signetics flat-pack device.

Motorola device direct replacement in dual-in-line packages (P, L). Can supply F package as special.

DM7000/8000 SERIES TTL

NATIONAL TO MOTOROLA

TEMPERATURE RANGE CROSS REFERENCE

Temperature Range	National	Motorola
0°C to +70°C	DM8xxx	MC74xx
−55°C to +125°C	DM7xxx	MC54xx

PACKAGE CROSS REFERENCE

Package	National	Motorola
Dual In-Line Ceramic	D	L
Flat Ceramic (1/4" x 1/4")	F	F
Dual In-Line Plastic	N	P

DEVICE CROSS REFERENCE

Type	Function	Direct Replacement	Suggested Alternate	Comments
DM8200	4-Bit Digital Comparator	—	—	
DM8210	8-Channel Digital Switch	—	—	
DM8211	8-Channel Multiplexer with Strobe	—	—	
DM8213	4-to-16 Line Decoder	MC8311	—	
DM8220	Parity Checker/Generator	—	MC4008	
DM8283	4-Bit Full Adder	MC7483	MC7260*	
DM8520	Modulo N Divider	—	MC4016/18	MC4016/18 program directly in binary/BCD code
DM8530	Decade Counter	MC7490	MC7280*	MC7280 is presettable
DM8532	Divide-by-12 Counter	MC7492	MC7288*	MC7288 is presettable
DM8533	Divide-by-16 Counter	MC7493	MC7281*	MC7281 is presettable
DM8550	Quad Latch	MC7475	MC4015	MC4015 is Quad D Flip Flop
DM8551	Buss ORable Quad D	—	—	
DM8560	Decade Up/Down Counter	MC74192*	—	
DM8563	Binary Up/Down Counter	MC74193*	—	
DM8570	Serial In-Parallel Out 8-Bit Shift Register	MC74164*	MC7495	Two MC7495's can perform parallel or serial in, parallel or serial out function
DM8580	4-Bit Universal Shift Register	MC7495	MC4012	MC4012 P_D = 180 mW, f_{Tog} = 30 MHz
DM8590	Parallel In Serial Out 8-Bit Shift Register	MC74165*	MC7495	Two MC7495's can perform 8 bit parallel or serial in, parallel or serial out function
DM8600	4-Bit Universal Shift Register	MC8300	—	
DM8680	Presettable Decade Counter	—	—	
DM8681	Presettable Binary Counter	—	—	
DM8688	Presettable Divide-by-12 Counter	—	—	
DM8810	Quad 2-Input TTL-to-MOS Gate	—	—	
DM8811	Quad 2-Input TTL-to-MOS Gate	—	—	
DM8812	14-volt Hex Inverter (Open Collector)	—	—	
DM8820	Line Receiver	—	MC1584	
DM8822	EIA RS-232C Line Receiver	—	MC1488	MC1488 is quad
DM8830	Line Driver	—	MC1582	
DM8840	BCD-to-Decimal Decoder/Driver	MC7441A	—	
DM8842	BCD-to-Decimal Decoder	MC7442	—	
DM8846	BCD-to-Seven Segment Decoder/Driver	MC7446	—	Active low, V_{out} = 30 Volts, I_{out} = 20 mA
DM8847	BCD-to-Seven Segment Decoder/Driver	MC7447	—	Active low, V_{out} = 35 Volts, I_{out} = 20mA
DM8848	BCD-to-Seven Segment Decoder/Driver	MC7448	—	Active High
DM8850	Retriggerable Monostable Multivibrator	MC9601	—	

*To be introduced

SUHL TTL

SYLVANIA TO MOTOROLA

TEMPERATURE RANGE CROSS REFERENCE

Temperature Range	Sylvania	Motorola
SF and SG Series (Example: SG40)		
−55°C to +125°C, High Fan-Out	SG40 (Base Number)	MC500
−55°C to +125°C, Low Fan-Out	SG41	MC550
0°C to +75°C, High Fan-Out	SG42	MC400
0°C to +75°C, Low Fan-Out	SG43	MC450
SM Series (Example: SM10 — applies only to Direct Replacement)		
−55°C to +125°C, High Fan-Out	SM10 (Base Number)	MC4326
−55°C to +125°C, Low Fan-Out	SM11	MC4327
0°C to +75°C, High Fan-Out	SM12	MC4026
0°C to +75°C, Low Fan-Out	SM13	MC4027

PACKAGE CROSS REFERENCE

Package	Sylvania	Motorola	Comments
Dual In-Line Ceramic (Black)	01	L	
Flat Ceramic	02	F	Motorola package is 1/4" x 1/4"
Dual In-Line Ceramic	03	L	
Dual In-Line Plastic		P	Motorola only

DEVICE CROSS REFERENCE

Type	Function	Direct Replacement	Suggested Alternate
SF10	R-S Flip-Flop	MC513	—
SF11	R-S Flip-Flop	MC563	—
SF12	R-S Flip-Flop	MC413	—
SF13	R-S Flip-Flop	MC463	—
SF20	Gated R-S Flip-Flop	MC514	—
SF21	Gated R-S Flip-Flop	MC564	—
SF22	Gated R-S Flip-Flop	MC414	—
SF23	Gated R-S Flip-Flop	MC464	—
SF30	AC Coupled R-S Flip-Flop	MC521	—
SF31	AC Coupled R-S Flip-Flop	MC571	—
SF32	AC Coupled R-S Flip-Flop	MC421	—
SF33	AC Coupled R-S Flip-Flop	MC471	—
SF50	AND J-K Flip-Flop	MC515	—
SF51	AND J-K Flip-Flop	MC565	—
SF52	AND J-K Flip-Flop	MC415	—
SF53	AND J-K Flip-Flop	MC465	—
SF60	OR J-K Flip-Flop	MC516	MC2126
SF61	OR J-K Flip-Flop	MC566	MC2176
SF62	OR J-K Flip-Flop	MC416	MC2026
SF63	OR J-K Flip-Flop	MC466	MC2076
SF80	Dual Type D Flip-Flop	MC522	MC3160
SF81	Dual Type D Flip-Flop	MC572	MC3160
SF82	Dual Type D Flip-Flop	MC422	MC3060
SF83	Dual Type D Flip-Flop	MC472	MC3060
SF91	Dual Type D Flip-Flop	MC572	MC3160
SF93	Dual Type D Flip-Flop	MC472	MC3060
SF100	Dual J-K Flip-Flop (Separate Clock, 35 MHz)	MC523	MC3162 MC2123
SF101	Dual J-K Flip-Flop	MC573	MC3162 MC2173
SF102	Dual J-K Flip-Flop	MC423	MC3062 MC2023

SUHL TTL DEVICE CROSS REFERENCE (cont)

Type	Function	Direct Replacement	Suggested Alternate
SF103	Dual J-K Flip-Flop	MC473	MC3062 MC2073
SF110	Dual J-K Flip-Flop (Common Clock, 35 MHz)	MC524	MC3161 MC2124
SF111	Dual J-K Flip-Flop	MC574	MC3161 MC2174
SF112	Dual J-K Flip-Flop	MC424	MC3061 MC2024
SF113	Dual J-K Flip-Flop	MC474	MC3061 MC2074
SF120	Dual J-K Flip-Flop (Separate Clock, 50 MHz)	MC2123	MC3162
SF121	Dual J-K Flip-Flop	MC2173	MC3162
SF122	Dual J-K Flip-Flop	MC2023	MC3062
SF123	Dual J-K Flip-Flop	MC2073	MC3062
SF130	Dual J-K Flip-Flop (Common Clock, 50 MHz)	MC2124	MC3161
SF131	Dual J-K Flip-Flop	MC2174	MC3161
SF132	Dual J-K Flip-Flop	MC2024	MC3061
SF133	Dual J-K Flip-Flop	MC2074	MC3061
SF200	AND J-K Flip-Flop (50 MHz)	MC2125	MC3151
SF201	AND J-K Flip-Flop	MC2175	MC3151
SF202	AND J-K Flip-Flop	MC2025	MC3051
SF203	AND J-K Flip-Flop	MC2075	MC3051
SF210	OR J-K Flip-Flop (50 MHz)	MC2126	MC3154
SF211	OR J-K Flip-Flop	MC2176	MC3154
SF212	OR J-K Flip-Flop	MC2026	MC3054
SF213	OR J-K Flip-Flop	MC2076	MC3054
SF250	AND J-K Flip-Flop (30 MHz)	—	MC3151 MC2125
SF251	AND J-K Flip-Flop	—	MC3151 MC2175
SF252	AND J-K Flip-Flop	—	MC3051 MC2025
SF253	AND J-K Flip-Flop	—	MC3051 MC2075
SF260	OR J-K Flip-Flop (30 MHz)	—	MC3154 MC2126
SF261	OR J-K Flip-Flop	—	MC3154 MC2176
SF262	OR J-K Flip-Flop	—	MC3054 MC2026
SF263	OR J-K Flip-Flop	—	MC3054 MC2076
SG40	Dual 4-Input NAND Gate	MC500	—
SG41	Dual 4-Input NAND Gate	MC550	—
SG42	Dual 4-Input NAND Gate	MC400	—
SG43	Dual 4-Input NAND Gate	MC450	—
SG50	Expandable 4-Wide 2-2-2-3 Input AOI Gate	MC501	—
SG51	Expandable 4-Wide 2-2-2-3 Input AOI Gate	MC551	—
SG52	Expandable 4-Wide 2-2-2-3 Input AOI Gate	MC401	—
SG53	Expandable 4-Wide 2-2-2-3 Input AOI Gate	MC451	—
SG60	8-Input NAND Gate	MC502	—
SG61	8-Input NAND Gate	MC552	—
SG62	8-Input NAND Gate	MC402	—
SG63	8-Input NAND Gate	MC452	—
SG70	Expandable Dual 2-Wide 2-Input AOI Gate	MC520	—
SG71	Expandable Dual 2-Wide 2-Input AOI Gate	MC570	—
SG72	Expandable Dual 2-Wide 2-Input AOI Gate	MC420	—
SG73	Expandable Dual 2-Wide 2-Input AOI Gate	MC470	—
SG80	Dual Pulse Shaper/Delay AND Gate	MC526	—
SG81	Dual Pulse Shaper/Delay AND Gate	MC576	—
SG82	Dual Pulse Shaper/Delay AND Gate	MC426	—
SG83	Dual Pulse Shaper/Delay AND Gate	MC476	—

SUHL TTL DEVICE CROSS REFERENCE (cont)

Type	Function	Direct Replacement	Suggested Alternate
SG90	2-Wide 3-Input AOI Gate with Gated Complement	MC503	–
SG91	2-Wide 3-Input AOI Gate with Gated Complement	MC553	–
SG92	2-Wide 3-Input AOI Gate with Gated Complement	MC403	–
SG93	2-Wide 3-Input AOI Gate with Gated Complement	MC453	–
SG100	Expandable 3-Wide 3-Input AOI Gate	MC504	MC2112
SG101	Expandable 3-Wide 3-Input AOI Gate	MC554	MC2162
SG102	Expandable 3-Wide 3-Input AOI Gate	MC404	MC2012
SG103	Expandable 3-Wide 3-Input AOI Gate	MC454	MC2062
SG110	Expandable 2-Wide 4-Input AOI Gate	MC505	–
SG111	Expandable 2-Wide 4-Input AOI Gate	MC555	–
SG112	Expandable 2-Wide 4-Input AOI Gate	MC405	–
SG113	Expandable 2-Wide 4-Input AOI Gate	MC455	–
SG120	Expandable 8-Input NAND Gate	MC506	MC2111
SG121	Expandable 8-Input NAND Gate	MC556	MC2161
SG122	Expandable 8-Input NAND Gate	MC406	MC2011
SG123	Expandable 8-Input NAND Gate	MC456	MC2061
SG130	Dual 4-Input Line Driver	MC507	–
SG131	Dual 4-Input Line Driver	MC557	–
SG132	Dual 4-Input Line Driver	MC407	–
SG133	Dual 4-Input Line Driver	MC457	–
SG140	Quad 2-Input NAND Gate	MC508	MC2101 MC3100
SG141	Quad 2-Input NAND Gate	MC558	MC2151 MC3100
SG142	Quad 2-Input NAND Gate	MC408	MC2001 MC3000
SG143	Quad 2-Input NAND Gate	MC458	MC2051 MC3000
SG150	4-Wide 3-2-2-3 Input Expander for AOI Gates	MC509	–
SG151	4-Wide 3-2-2-3 Input Expander for AOI Gates	MC559	–
SG152	4-Wide 3-2-2-3 Input Expander for AOI Gates	MC409	–
SG153	4-Wide 3-2-2-3 Input Expander for AOI Gates	MC459	–
SG160	Triple 2-Input Buss Driver	MC519	–
SG161	Triple 2-Input Buss Driver	MC569	MC3107
SG162	Triple 2-Input Buss Driver	MC419	–
SG163	Triple 2-Input Buss Driver	MC469	MC3007
SG170	Dual 4-Input Expander for AOI Gates	MC510	–
SG171	Dual 4-Input Expander for AOI Gates	MC560	–
SG172	Dual 4-Input Expander for AOI Gates	MC410	–
SG173	Dual 4-Input Expander for AOI Gates	MC460	–
SG180	Dual 4-Input Expander for NAND Gates	MC511	–
SG181	Dual 4-Input Expander for NAND Gates	MC561	–
SG182	Dual 4-Input Expander for NAND Gates	MC411	–
SG183	Dual 4-Input Expander for NAND Gates	MC461	–
SG190	Triple 3-Input NAND Gate	MC512	MC3105
SG191	Triple 3-Input NAND Gate	MC562	MC3105
SG192	Triple 3-Input NAND Gate	MC412	MC3005
SG193	Triple 3-Input NAND Gate	MC462	MC3005
SG200	Expandable 8-Input NAND Gate	MC2111	–
SG201	Expandable 8-Input NAND Gate	MC2161	–
SG202	Expandable 8-Input NAND Gate	MC2011	–
SG203	Expandable 8-Input NAND Gate	MC2061	–
SG210	Expandable 2-Wide 4-Input AOI Gate	MC2100	–
SG211	Expandable 2-Wide 4-Input AOI Gate	MC2150	–
SG212	Expandable 2-Wide 4-Input AOI Gate	MC2000	–
SG213	Expandable 2-Wide 4-Input AOI Gate	MC2050	–
SG220	Quad 2-Input NAND Gate	MC2101	MC3100
SG221	Quad 2-Input NAND Gate	MC2151	MC3100
SG222	Quad 2-Input NAND Gate	MC2001	MC3000
SG223	Quad 2-Input NAND Gate	MC2051	MC3000
SG230	4-Wide 3-2-2-3 Input Expander for AOI Gates	MC2102	–
SG231	4-Wide 3-2-2-3 Input Expander for AOI Gates	MC2152	–
SG232	4-Wide 3-2-2-3 Input Expander for AOI Gates	MC2002	–
SG233	4-Wide 3-2-2-3 Input Expander for AOI Gates	MC2052	–

SUHL TTL DEVICE CROSS REFERENCE (cont)

Type	Function	Direct Replacement	Suggested Alternate
SG240	Dual 4-Input NAND Gate	MC2103	MC3110
SG241	Dual 4-Input NAND Gate	MC2153	MC3110
SG242	Dual 4-Input NAND Gate	MC2003	MC3010
SG243	Dual 4-Input NAND Gate	MC2053	MC3010
SG250	Expandable 4-Wide 2-2-2-3 Input AOI Gate	MC2104	MC5453
SG251	Expandable 4-Wide 2-2-2-3 Input AOI Gate	MC2154	MC5453
SG252	Expandable 4-Wide 2-2-2-3 Input AOI Gate	MC2004	MC7453
SG253	Expandable 4-Wide 2-2-2-3 Input AOI Gate	MC2054	MC7453
SG260	8-Input NAND Gate	MC2105	MC3115
SG261	8-Input NAND Gate	MC2155	MC3115
SG262	8-Input NAND Gate	MC2005	MC3015
SG263	8-Input NAND Gate	MC2055	MC3015
SG270	Dual 4-Input Expander for AOI Gates	MC2106	MC3130
SG271	Dual 4-Input Expander for AOI Gates	MC2156	MC3130
SG272	Dual 4-Input Expander for AOI Gates	MC2006	MC3030
SG273	Dual 4-Input Expander for AOI Gates	MC2056	MC3030
SG280	Dual 4-Input AND Gate	MC527	—
SG281	Dual 4-Input AND Gate	MC577	—
SG282	Dual 4-Input AND Gate	MC427	—
SG283	Dual 4-Input AND Gate	MC477	—
SG290	Dual 2-Wide 2-3 Input OR Expander	MC528	—
SG291	Dual 2-Wide 2-3 Input OR Expander	MC578	—
SG292	Dual 2-Wide 2-3 Input OR Expander	MC428	—
SG293	Dual 2-Wide 2-3 Input OR Expander	MC478	—
SG300	Expandable 3-Wide 3-Input AOI Gate	MC2112	—
SG301	Expandable 3-Wide 3-Input AOI Gate	MC2162	—
SG302	Expandable 3-Wide 3-Input AOI Gate	MC2012	—
SG303	Expandable 3-Wide 3-Input AOI Gate	MC2062	—
SG310	Expandable Dual 2-Wide 2-Input AOI Gate	MC2113	MC3120
SG311	Expandable Dual 2-Wide 2-Input AOI Gate	MC2163	MC3120
SG312	Expandable Dual 2-Wide 2-Input AOI Gate	MC2013	MC3020
SG313	Expandable Dual 2-Wide 2-Input AOI Gate	MC2063	MC3020
SG320	Triple 3-Input NAND Gate	MC2107	MC3105
SG321	Triple 3-Input NAND Gate	MC2157	MC3105
SG322	Triple 3-Input NAND Gate	MC2007	MC3005
SG323	Triple 3-Input NAND Gate	MC2057	MC3005
SG330	Quad 2-Input NOR Gate	—	MC3102
SG331	Quad 2-Input NOR Gate	—	MC3102
SG332	Quad 2-Input NOR Gate	—	MC3002
SG333	Quad 2-Input NOR Gate	—	MC3002
SG340	Quad 2-Input NOR Gate	—	MC3102
SG341	Quad 2-Input NOR Gate	—	MC3102
SG342	Quad 2-Input NOR Gate	—	MC3002
SG343	Quad 2-Input NOR Gate	—	MC3002
SG351	Quad 2-Input Lamp Driver	MC2165	—
SG353	Quad 2-Input Lamp Driver	MC2065	—
SG370	Hex Inverter	MC529	MC5404
SG371	Hex Inverter	MC579	MC5404
SG372	Hex Inverter	MC429	MC7404
SG373	Hex Inverter	MC479	MC7404
SG380	Hex Inverter	MC2116	MC3108
SG381	Hex Inverter	MC2166	MC3108
SG382	Hex Inverter	MC2016	MC3008
SG383	Hex Inverter	MC2066	MC3008
SM10	Full Adder	MC4326	MC5480
SM11	Full Adder	MC4327	MC5480
SM12	Full Adder	MC4026	MC7480
SM13	Full Adder	MC4027	MC7480
SM20	Dependent Carry Fast Adder	MC4328	—
SM21	Dependent Carry Fast Adder	MC4329	—
SM22	Dependent Carry Fast Adder	MC4028	—
SM23	Dependent Carry Fast Adder	MC4029	—
SM30	Independent Carry Fast Adder	MC4330	—
SM31	Independent Carry Fast Adder	MC4331	—

SUHL TTL DEVICE CROSS REFERENCE (cont)

Type	Function	Direct Replacement	Suggested Alternate
SM32	Independent Carry Fast Adder	MC4030	—
SM33	Independent Carry Fast Adder	MC4031	—
SM41	Carry Decoder	MC4332	—
SM43	Carry Decoder	MC4032	—
SM61	Quad Latch (Open Collector)	MC4335	—
SM63	Quad Latch (Open Collector)	MC4035	—
SM71	Quad Latch	MC4337	—
SM73	Quad Latch	MC4037	—
SM81	16-Bit Scratch Pad Memory	MC4304	—
SM82	16-Bit Scratch Pad Memory	MC4304	—
SM83	16-Bit Scratch Pad Memory	MC4004	—
SM90	Decade Counter	MC5090**	MC5490
SM91	Decade Counter	MC5091**	MC5490
SM92	Decade Counter	MC5092**	MC7490
SM93	Decade Counter	MC5093**	MC7490
SM111	4-Bit Shift Register	MC5111**	MC4312, MC5495
SM113	4-Bit Shift Register	MC5113**	MC4012, MC7495
SM121	8-Bit Parity Tree	MC5121**	MC4308
SM123	8-Bit Parity Tree	MC5123**	MC4008
SM131	4-Bit Comparator	MC5131**	MC4322
SM133	4-Bit Comparator	MC5133**	MC4022
SM141	Programmable Binary Divider	MC5141**	MC4318
SM143	Programmable Binary Divider	MC5143**	MC4018
SM151	Programmable Decade Divider	MC5151**	MC4316
SM153	Programmable Decade Divider	MC5153**	MC4016
SM163	Binary Counter	MC5163**	MC7493
SM173	Decade Counter	MC5173**	MC7490
SM181	Binary Up/Down Counter	MC5181**	MC54193*
SM183	Binary Up/Down Counter	MC5183**	MC74193*
SM191	Decade Up/Down Counter	MC5191**	MC54192*
SM193	Decade Up/Down Counter	MC5193**	MC74192*, MC8306
SM203	BCD-to-Seven Segment Decoder	—	MC8307*, MC7448, MC4039
SM211	Dual 4-Bit Multiplexer	MC4300	—
SM213	Dual 4-Bit Multiplexer	MC4000	—
SM221	Demultiplexer	MC4302	—
SM223	Demultiplexer	MC4002	—

* To be introduced
** Available on special order only

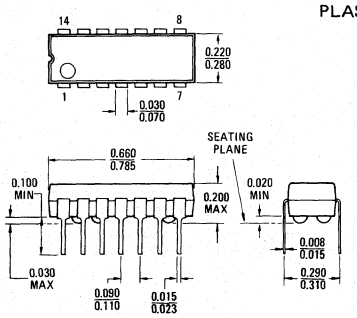
PACKAGING INFORMATION

The packaging used for each device type is indicated on the individual data sheet unless packaging is the same for all devices in a given MC-number series. In this case, the packaging description is in the General Information section for that series.

Package type is denoted by a suffix to the part number as follows:

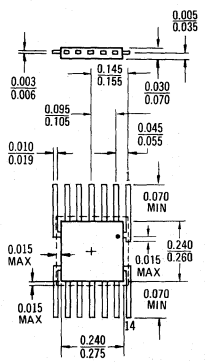
Suffix	Description
F	Ceramic Flat
L	Ceramic Dual In-Line
P	Plastic Dual In-Line

P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



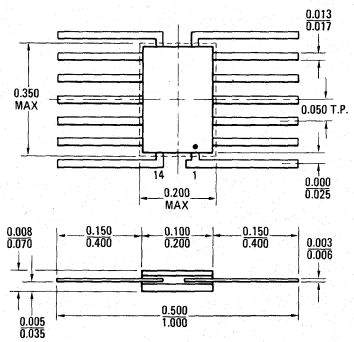
Four insulating stand-offs are provided
To convert inches to millimeters multiply by 25.4
All JEDEC dimensions and notes apply

F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86



Lead 1 identified by color dot or by elbow on lead.
To convert inches to millimeters multiply by 25.4
All JEDEC dimensions and notes apply

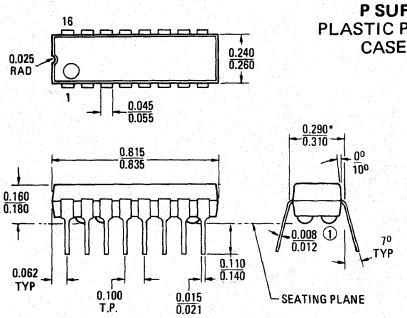
F SUFFIX
CERAMIC PACKAGE
CASE 609
TO-85



Lead 1 identified by color dot or by elbow on lead.
To convert inches to millimeters multiply by 25.4
All JEDEC dimensions and notes apply

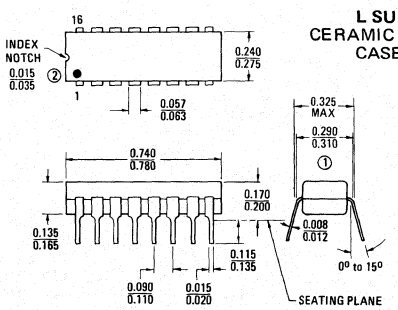
Devices formerly using Case 609 are now being manufactured in Case 607. Either package may be shipped during the transition.

P SUFFIX
PLASTIC PACKAGE
CASE 612



*Dimension is to lead centerline when formed parallel.
① 4 insulating stand-offs are provided.
To convert inches to millimeters multiply by 25.4

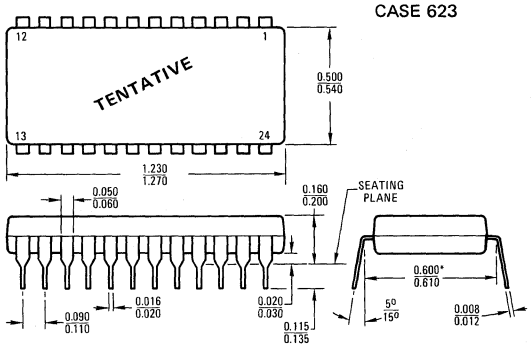
L SUFFIX
CERAMIC PACKAGE
CASE 620



① This dimension is measured from the lead centers at the seating plane with leads vertical.
② Lead 1 identified by color dot, notch in lead, or notch in ceramic.
To convert inches to millimeters multiply by 25.4

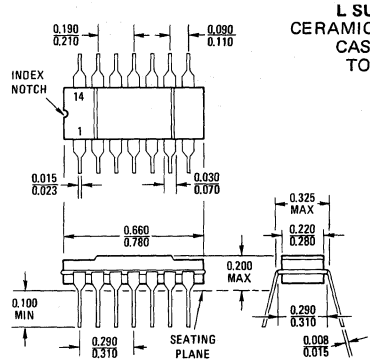
PACKAGING INFORMATION (continued)

L SUFFIX
CERAMIC PACKAGE
CASE 623



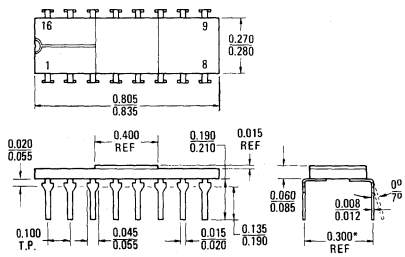
To convert inches to millimeters multiply by 25.4
*Dimension is to lead centerline when formed parallel.

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



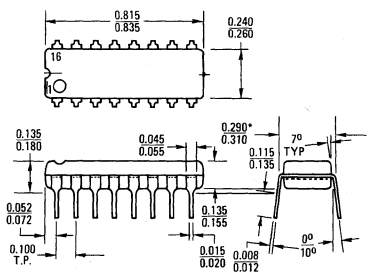
To convert inches to millimeters multiply by 25.4.
All JEDEC TO-116 dimensions and notes apply.

L SUFFIX
CERAMIC PACKAGE
CASE 638



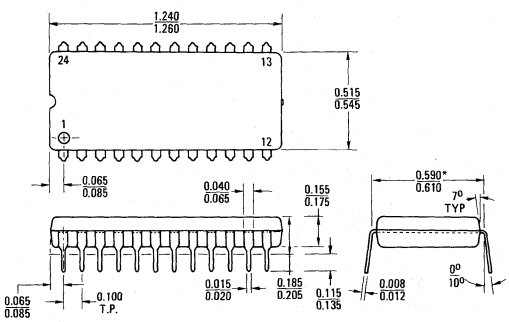
To convert inches to millimeters multiply by 25.4
*Dimension is to lead centerline when formed parallel.

P SUFFIX
PLASTIC PACKAGE
CASE 648

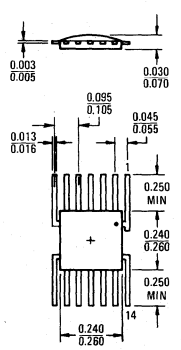


To convert inches to millimeters multiply by 25.4
*Dimension is to lead centerline when formed parallel.

P SUFFIX
PLASTIC PACKAGE
CASE 649



*Dimension to lead centerline when formed parallel.
To convert inches to millimeters multiply by 25.4



F SUFFIX
CERAMIC PACKAGE
CASE 651

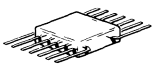
Lead 1 identified by color dot or by elbow on lead.
Top Cover made of silastic material.

To convert inches to millimeters multiply by 25.4

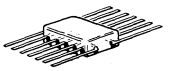
INTEGRATED CIRCUITS

The MTTL complex functions are designed for digital applications in the medium to high-speed range.

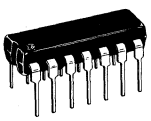
These MTTL devices provide significant reduction in package count and increased logic per function over devices in the basic MTTL and MDTL families.



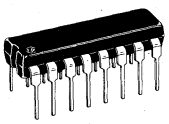
F SUFFIX
CERAMIC PACKAGE
CASE 607♦
TO-86



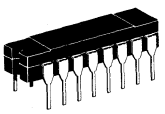
F SUFFIX
CERAMIC PACKAGE
CASE 609♦
TO-85



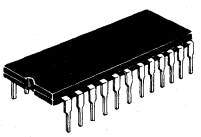
P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



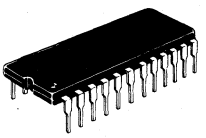
P SUFFIX
PLASTIC PACKAGE
CASE 612



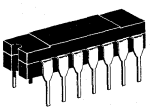
L SUFFIX
CERAMIC PACKAGE
CASE 620



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

All devices shown can be used with all MTTL and MDTL devices; however, the loading factors shown reflect use with other devices in the same MC-number series unless otherwise noted.

Function	Type ① -55 to +125°C	Case	Type ① 0 to +75°C	Case	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation P_D mW typ/pkg
Dual 4-Channel Data Selector	MC4300F	607,632	MC4000F,L,P	607,632,605	10	Control Line = 18 Data Line = 11	150
BCD-to-Binary/Binary-to-BCD Number Converter	–	–	MC4001L,P	620,612	Open Collector I_{OL} = 16 mA	Address Time <45 ns	300
Dual Data Distributor	–	–	MC4002F,L,P	607,632,605	10	10.5	175
16-Bit Scratch Pad Memory Cell	MC4304F,L	607,632	MC4004F,L,P	607,632,605	I_{OL} = 40 mA Open Collector	Write mode: 25 Sense mode: 15	250
16-Bit Scratch Pad Memory Cell	MC4305F,L	607,632	MC4005F,L,P	607,632,605	I_{OL} = 20 mA	Write mode: 25 Sense mode: 15	250
Binary to One-of-Eight Line Decoder	MC4306F,L	607,632	MC4006F,L,P	607,632,605	10	14	100
Dual Binary to One-of-Four Line Decoder	–	–	MC4007L,P	620,612	10	14	125
8-Bit Parity Tree	MC4308F,L	607,632	MC4008F,L,P	607,632,605	10	15 to 30	150
Dual 4-Bit Parity Tree	–	–	MC4010F,L,P	607,632,605	10	9.5 to 22	125
4-Bit Shift Register	–	–	MC4012F,L,P	607,632,605	10	22/bit	180
Quad Type D Flip-Flop	–	–	MC4015L,P	620,612	10	16	190
Programmable Modulo-N Decade Counter	MC4316L	620	MC4016L,P	620,612	8	Clock to Q3 = 50 Clock to Buss = 35	250
Programmable Modulo-N Hexadecimal Counter	MC4318L	620	MC4018L,P	620,612	8	Clock to Q3 = 50 Clock to Buss = 35	250
Dual 4-Bit Comparator (Open Collector)	–	–	MC4021P	612	10	20	250
Dual 4-Bit Comparator	–	–	MC4022P	612	10	20	250
4-Bit Universal Counter	–	–	MC4023F,L,P	607,632,605	10	16/bit	200
Dual Voltage Controlled Multivibrator	MC4324F,L	607,632	MC4024F,L,P	607,632,605	7	f_{max} = 25 MHz	150
Full Adder	MC4326F,L	607,632	MC4026F,L,P	607,632,605	15/12••	25/13#	90
Full Adder	MC4327F,L	607,632	MC4027F,L,P	607,632,605	7/6••	25/13#	90
Adder (Dependent Carry)	MC4328F,L	607,632	MC4028F,L,P	607,632,605	15/12••	25/13#	125
Adder (Dependent Carry)	MC4329F,L	607,632	MC4029F,L,P	607,632,605	7/6••	25/13#	125
Adder (Independent Carry)	MC4330F,L	607,632	MC4030F,L,P	607,632,605	15/12••	25/13#	125
Adder (Independent Carry)	MC4331F,L	607,632	MC4031F,L,P	607,632,605	7/6••	25/13#	125
Carry Decoder	MC4332F,L	607,632	MC4032F,L,P	607,632,605	–	Δt_{pd} = 4.0/decoder	20
Quad Latch (Open Collector)	MC4335F,L	607,632	MC4035F,L,P	607,632,605	7	25	140
Quad Latch	MC4337F,L	607,632	MC4037F,L,P	607,632,605	10	25	150
Inverting/Non-Inverting One-of-Eight Decoder	–	–	MC4038P	612	Open Collector I_{OL} = 20 mA	Address Time <45 ns	240
Seven-Segment Character Generator	–	–	MC4039P	612			240
Binary to Two-of-Eight Decoder	–	–	MC4040P	612			200
Single-Error Hamming Code Detector and Generator	–	–	MC4041P	612			250
Quad Predriver	–	–	MC4042F,L,P	607,632,605	I_{OL} = 50 mA Open Collector	15	120
Dual Line Selector	–	–	MC4043F,L,P	607,632,605	I_{OL} = 400 mA Pulsed	20	70

① F suffix denotes ceramic flat package, L suffix denotes ceramic dual in-line package, P suffix denotes plastic dual in-line package.

♦Devices formerly using Case 609 (TO-85) are now being manufactured in Case 607 (TO-86). Either package may be shipped during the transition.

••MC4300 Series/MC4000 Series; loading specified for use with MTTL I devices.

#Add delay/Carry delay †High/Low

MTTL COMPLEX LOGIC FUNCTIONS

FUNCTIONS AND CHARACTERISTICS (continued)

Function	Type ① -55 to +125°C	Case	Type ① 0 to +75°C	Case	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation P_D mW typ/pkg
Phase-Frequency Detector	MC4344F,L	607,632	MC4044F,L,P	607,632,605	10	9.0	85
Non-Inverting One-of-Eight Decoder	–	–	MC4048P	612	Open Collector I_{OL} = 16 mA	Address Time <50 ns	240
Counter-Latch-Decoder	MC4350L	620	MC4050L,P	620,612	Open Collector I_{OL} = 40 mA	f_{Tog} = 35 MHz	450
Counter-Latch-Decoder	–	–	MC4051P	612	Open Emitter 40 mA Sourcing Capability @ 10% Duty Cycle	f_{Tog} = 35 MHz	450
Dual Majority Logic Gate	–	–	MC4062P	605	–	$\overline{Z}$ = 20 $\overline{\overline{Z}}$ = 11	75
			0 to +70°C				
BCD-to-Decimal Decoder and High-Level Driver	–	–	MC7441AL,P	620,612	–	–	105
BCD-to-Decimal Decoder	MC5442L	620	MC7442L,P	620,612	10	2 Logic Levels = 22 3 Logic Levels = 23	140
Excess Three-to-Decimal Decoder	MC5443L	620	MC7443L,P	620,612	10	2 Logic Levels = 22 3 Logic Levels = 23	140
Excess Three Gray-to-Decimal Decoder	MC5444L	620	MC7444L,P	620,612	10	2 Logic Levels = 22 3 Logic Levels = 23	140
BCD to One-of-Ten Decoder/Driver	MC5445L	620	MC7445L,P	620,612	–	50 max	215
BCD-to-Seven Segment Decoder/Driver	MC5446L	620	MC7446L,P	620,612	BI/RBO = 5	–	265
BCD-to-Seven Segment Decoder/Driver	MC5447L	620	MC7447L,P	620,612	BI/RBO = 5	–	265
BCD-to-Seven Segment Decoder/Driver	MC5448L	620	MC7448L,P	620,612	BI/RBO = 5 a thru g = 4	–	265
BCD-to-Seven Segment Decoder/Driver	MC5449F	607	MC7449F	607	6	–	165
Quad Latch			MC7475P	612	10	30	160
Gated Full Adder	MC5480L	632	MC7480L,P	632,605	S, $\overline{S}$ = 10 $\overline{C}_{out}$ = 5 A*, B* = 3	10/55#	105
2-Bit Full Adder	MC15482F,L	607,632	MC17482F,L,P	607,632,605	10	15/12#	165
2-Bit Full Adder	MC25482F,L	607,632	MC27482F,L,P	607,632,605	10	15/12#	165
4-Bit Binary Full Adder	MC5483L	620	MC7483L,P	620,612	S = 10 C_{out} = 5	35	390
16-Bit Scratch Pad Memory Cell With Gated Inputs	MC5484L	620	–	–	I_{OL} = 40 mA Open Collector I_{OL} = 20 mA	Write Mode: 25 Sense Mode: 15	250
	–	–	MC7484L,P	620,612			
Decade Counter	MC5490F,L	607,632	MC7490F,L,P	607,632,605	10	20/bit	160
8-Bit Shift Register	MC5491AL	632	MC7491AL,P	632,605	10	25	175
Divide-by-Twelve Counter	MC5492F,L	607,632	MC7492F,L,P	607,632,605	10	60	160
4-Bit Binary Counter	MC5493L	632	MC7493L,P	632,605	10	20/bit	160
4-Bit Shift Register	*MC5494L	620	*MC7494P	612	–	25	175
4-Bit Shift Register	MC5495F,L	607,632	MC7495F,L,P	607,632,605	10	25	250
5-Bit Shift Register	MC5496L	620	MC7496L,P	620,612	–	25	240
Monostable Multivibrator	MC54121F,L	607,632	MC7412IF,L,P	607,632,605	10	t_{pd+}, B to Q = 35	90
BCD to One-of-Ten Decoder/Driver	MC54145L	620	MC74145L,P	620,612	–	50 max	215
16-Channel Data Selector	*MC54150L	623	*MC74150P	649	–	8.5 to 35	200
8-Channel Data Selector	*MC54151L	620	*MC74151P	612	–	8.5 to 35	145
			0 to +75°C				
Quad Exclusive OR Gate	MC8241F,L	607,632	MC7241F,L,P	607,632,605	10	10	225
Quad Exclusive NOR Gate (Open Collector)	MC8242F,L	607,632	MC7242F,L,P	607,632,605	10	18	170
Universal 4-Bit Shift Register	MC9300L	620	MC8300L,P	620,612	6	25	300
BCD-to-Decimal Decoder	MC9301L	620	MC8301L,P	620,612	10	22	125
Dual Full Adder	MC9304L	620	MC8304L,P	620,612	$\overline{C}_{o1}$, $\overline{C}_{o2}$ = 7 S1, $\overline{S}$2 = 10 $\overline{S}$1, S2 = 9	8.0 to 28	110
Dual 4-Bit Latch	–	–	MC8308P	649	9	E to Q = 25	325
Dual 4-Channel Data Selector	MC9309L	620	MC8309L,P	620,612	Z, W = 10 $\overline{Z}$, $\overline{W}$ = 9	9.0 to 24	150
Presettable Decade Counter	MC9310L	620	MC8310L,P	620,612	6	14 to 35	300
One-of-16 Decoder	–	–	MC8311P	649	10	$\overline{E}$ to Q = 26 max	175
8-Channel Data Selector	MC9312L	620	MC8312L,P	620,612	Z = 20/10† $\overline{Z}$ = 18/9†	9.0 to 24	135
Presettable 4-Bit Binary Counter	MC9316L	620	MC8316L,P	620,612	6	14 to 35	300
Dual 8-Bit Shift Register	MC9328L	620	MC8328L,P	620,612	6	C to Q = 22 (t_{pd-}) 13 (t_{pd+}) $\overline{MR}$ to Q = 35	250
Retriggerable Monostable Multivibrator	MC9601F,L	607,632	MC8601F,L,P	607,632,605	MC9601 = 6 MC8601 = 8	25	75

① F suffix denotes ceramic flat package, L suffix denotes ceramic dual in-line package, P suffix denotes plastic dual in-line package.

**MC4300 Series/MC4000 Series; loading specified for use with MTTL I devices. *To be announced

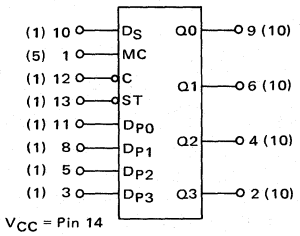
#Add delay/Carry delay †High/Low

LOGIC DIAGRAMS

Numbers at ends of pin terminals represent pin numbers. Numbers in parenthesis indicate loading. Loading factors reflect use with other devices in the same MC-number series unless otherwise noted.

SHIFT REGISTERS

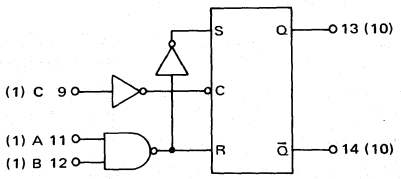
MC4012
4-Bit Shift Register



V_{CC} = Pin 14
Gnd = Pin 7

t_{pd} = 22 ns typ/bit
P_D = 180 mW typ/pkg

MC5491A/MC7491A
8-Bit Shift Register



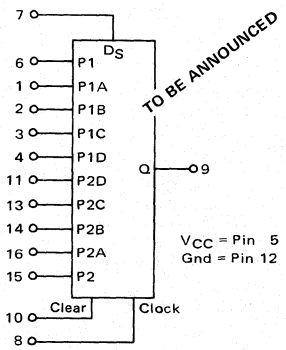
TRUTH TABLE
Synchronous Inputs

t_n		t_{n+8}	
A	B	Q	Q̄
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

V_{CC} = Pin 5
Gnd = Pin 10

t_{pd} = 25 ns typ
P_D = 175 mW typ/pkg
f = 18 MHz typ

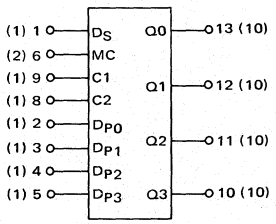
MC5494/MC7494
4-Bit Shift Register



V_{CC} = Pin 5
Gnd = Pin 12

t_{pd}, Clock to Q = 25 ns typ
P_D = 175 mW typ/pkg
f_{Tog} = 10 MHz

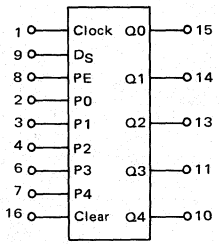
MC5495/MC7495
4-Bit Shift Register



V_{CC} = Pin 14
Gnd = Pin 7

t_{pd} = 25 ns typ
P_D = 250 mW typ/pkg
f = 31 MHz typ

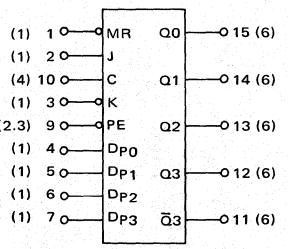
MC5496/MC7496
5-Bit Shift Register



V_{CC} = Pin 5
Gnd = Pin 12

t_{pd}, Clock to Q4 = 25 ns typ
P_D = 240 mW typ/pkg
f_{Tog} = 10 MHz

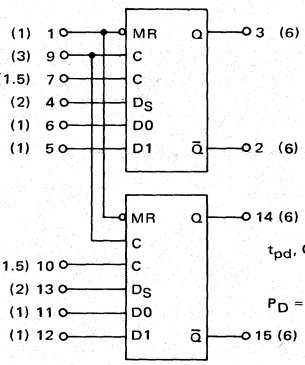
MC8300/MC9300
Universal 4-Bit Shift Register



V_{CC} = Pin 16
Gnd = Pin 8

t_{pd} = 25 ns typ
P_D = 300 mW typ/pkg

MC8328/MC9328
Dual 8-Bit Shift Register



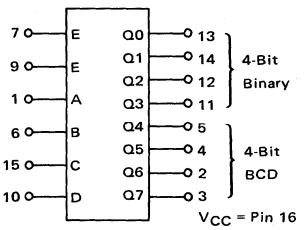
V_{CC} = Pin 16
Gnd = Pin 8

t_{pd}, Clock to Output = 22 ns typ (t_{pd-})
= 13 ns typ (t_{pd+})
$\overline{MR}$ to Output = 35 ns typ (t_{pd-} or t_{pd+})
P_D = 250 mW typ/pkg

2

DECODERS

MC4001
BCD-to-Binary/Binary-to-BCD Number Converter



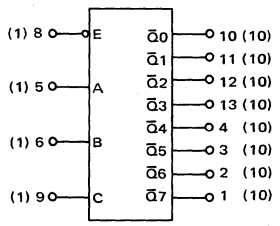
V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
				Binary to BCD				BCD to Binary			
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	0	0	1	0	1
0	1	1	0	1	0	0	1	0	1	1	0
0	1	1	1	1	0	1	0	0	1	1	1
1	0	0	0	1	0	1	1	0	1	0	1
1	0	0	1	1	1	0	0	0	1	1	0
1	0	1	0	1	0	0	0	0	1	1	1
1	0	1	1	1	0	0	1	1	0	0	0
1	1	0	0	1	1	1	0	1	0	0	1
1	1	0	1	1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1	0	0	1	0
1	1	1	1	0	1	0	0	0	0	0	0

P_D = 300 mW typ/pkg

MC4006/MC4306
Binary to 1-of-8 Line Decoder

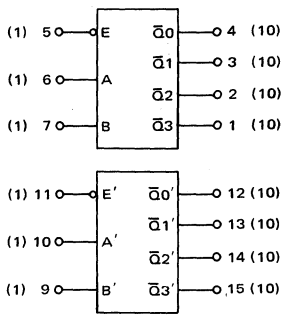


V_{CC} = Pin 14
Gnd = Pin 7

INPUT			OUTPUT							
C	B	A	7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

t_{pd} = 14 ns typ
P_D = 100 mW typ/pkg

MC4007
Dual Binary to 1-of-4 Line Decoder



INPUT		OUTPUT			
B	A	3	2	1	0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

V_{CC} = Pin 16
Gnd = Pin 8

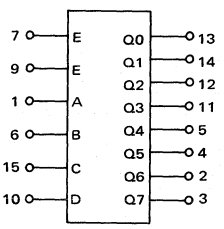
t_{pd} = 14 ns typ
P_D = 125 mW typ/pkg

MC4038
Inverting/Non-Inverting 1-of-8 Decoder

MC4040
Binary to 2-of-8 Decoder

MC4041
Single-Error Hamming Code Detector and Generator

MC4048
Non-Inverting 1-of-8 Decoder

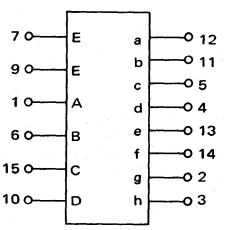


V_{CC} = Pin 16
Gnd = Pin 8

ALL TYPES INPUT				MC4038 OUTPUT								MC4040 OUTPUT								MC4041 OUTPUT								MC4048 OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	0	1	0	1	1	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0
0	1	0	1	1	1	1	1	1	0	1	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0
0	1	1	0	1	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0	1	1	1	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	0	1	0	0	0	0	0	0	1	0	1	1	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
1	0	1	0	0	0	1	0	0	0	0	0	1	0	1	1	1	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
1	0	1	1	0	0	0	1	0	0	0	0	1	0	1	1	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
1	1	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

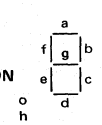
P_D = 240 mW typ/pkg — MC4038, MC4041, MC4048
= 200 mW typ/pkg — MC4040

MC4039
7-Segment Character Generator



V_{CC} = Pin 16
Gnd = Pin 8

SEGMENT IDENTIFICATION



P_D = 240 mW typ/pkg

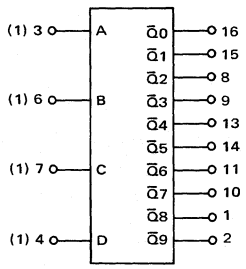
DIGIT	SEGMENTS ILLUMINATED	INPUT 3	2	1	0	OUTPUT a	b	c	d	e	f	g	h
0	a,b,c,d,e,f	0	0	0	0	0	0	0	0	0	0	1	1
1	b,c	0	0	0	1	1	0	0	1	1	1	1	1
2	a,b,d,e,g	0	0	1	0	0	0	1	0	0	1	0	1
3	a,b,c,d,g	0	0	1	1	0	0	0	0	1	1	0	1
4	b,c,f,g	0	1	0	0	1	0	0	1	1	0	0	1
5	a,c,d,f,g	0	1	0	1	0	1	0	0	1	0	0	1
6	c,d,e,f,g	0	1	1	0	1	1	0	0	0	0	0	1
7	a,b,c	0	1	1	1	0	0	0	1	1	1	1	1
8	a,b,c,d,e,f,g	1	0	0	0	0	0	0	0	0	0	0	1
9	a,b,c,f,g	1	0	0	1	0	0	0	1	1	0	0	1
NONE		1	0	1	0	1	1	1	1	1	1	1	1
●	h (Ext.)	1	0	1	1	1	1	1	1	1	1	1	0
–	g	1	1	0	0	1	1	1	1	1	1	0	1
NONE		1	1	0	1	1	1	1	1	1	1	1	1
NONE		1	1	1	0	1	1	1	1	1	1	1	1
NONE		1	1	1	1	1	1	1	1	1	1	1	1

(continued)

LOGIC DIAGRAMS (continued)

DECODERS (continued)

MC7441A
BCD-to-Decimal Decoder and High-Level Driver

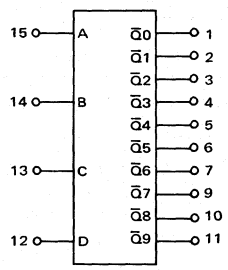


V_{CC} = Pin 5
Gnd = Pin 12

INPUT				OUTPUT									
D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1

P_D = 105 mW typ/pkg

MC5445/MC7445
MC54145/MC74145
BCD to 1-of-10 Decoder/Driver



V_{CC} = Pin 16
Gnd = Pin 8

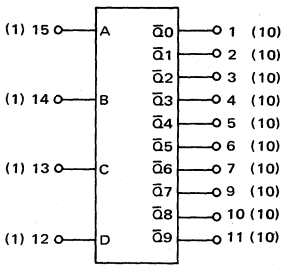
INPUT				OUTPUT									
D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

t_{pd} = 50 ns max
P_D = 215 mW typ/pkg

MC5442/MC7442
BCD-to-Decimal Decoder

MC5443/MC7443
Excess Three-to-Decimal Decoder

MC5444/MC7444
Excess Three Gray-to-Decimal Decoder

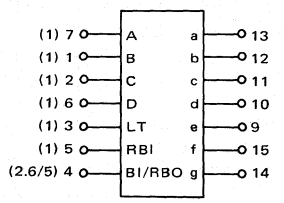


V_{CC} = Pin 16
Gnd = Pin 8

t_{pd}, 2 Logic Levels = 22 ns typ
3 Logic Levels = 23 ns typ
P_D = 140 mW typ/pkg

MC5442/MC7442 BCD INPUT				MC5443/MC7443 EXCESS 3 INPUT				MC5444/MC7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	0	1	0	1	0	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	0	0	0	0	1	1	0	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	0	0	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	1	1	1	0	1	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	0	1	1	1	1	0	1	1	1	1	1
1	0	0	1	1	1	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	0	1	0	0	1	0	1	1	1	1	1	0	1	1	1	1
1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	1	1	0	1	1	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

MC5446/MC7446
MC5447/MC7447
MC5448/MC7448
BCD-to-Seven Segment Decoder/Drivers



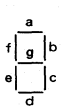
V_{CC} = Pin 16
Gnd = Pin 8

P_D = 265 mW typ/pkg

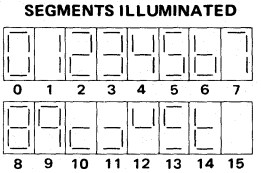
DIGIT OR FUNCTION	ALL TYPES							MC5446/MC7446 MC5447/MC7447 OUTPUT							MC5448/MC7448 OUTPUT						
	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	a	b	c	d	e	f	g
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0
1	1	X	0	0	0	1	1	1	0	0	1	1	1	1	0	1	1	0	0	0	0
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0	1	1	0	1	1	0	1
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0	1	1	1	1	0	0	1
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0	1	0	1	1	0	1	1
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0	1	1	1	0	0	1	1
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0	0	0	0	1	1	0	1
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1	0	0	1
12	1	X	1	1	0	0	1	1	0	1	1	1	0	0	0	1	1	1	1	0	1
13	1	X	1	1	0	1	1	0	1	1	0	1	0	0	1	0	0	1	0	1	1
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
BI	X	X	X	X	X	X	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0
LT	0	X	X	X	X	X	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1

X = Don't care

SEGMENT IDENTIFICATION



SEGMENTS ILLUMINATED

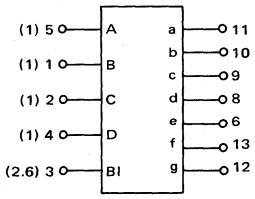


LOGIC DIAGRAMS (continued)

2

DECODERS (continued)

MC5449/MC7449
BCD-to-Seven Segment Decoder/Driver



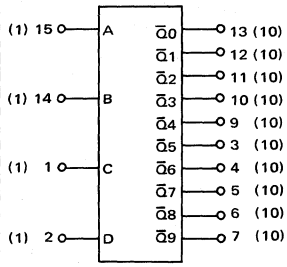
V_{CC} = Pin 16
Gnd = Pin 8

P_D = 165 mW typ/pkg

DIGIT OR FUNCTION	INPUT D	C	B	A	BI	OUTPUT a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	1	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	1	0	0	1
4	0	1	0	0	1	0	1	1	0	0	1	1
5	0	1	0	1	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	0	1	1
10	1	0	1	0	1	0	0	0	1	1	0	1
11	1	0	1	1	1	0	0	1	1	0	0	1
12	1	1	0	0	1	0	1	0	0	0	1	1
13	1	1	0	1	1	1	0	0	1	0	1	1
14	1	1	1	0	1	0	0	0	1	1	1	1
15	1	1	1	1	1	0	0	0	0	0	0	0
BI	X	X	X	X	0	0	0	0	0	0	0	0

X = Don't care

MC8301/MC9301
BCD-to-Decimal Decoder

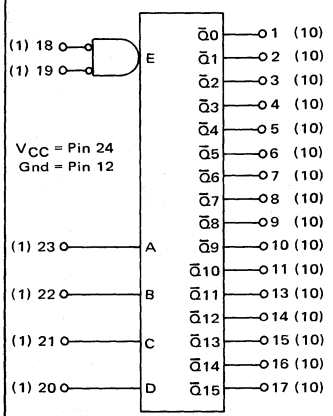


V_{CC} = Pin 16
Gnd = Pin 8

INPUT D	C	B	A	OUTPUT 9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

t_{pd} = 22 ns typ
P_D = 125 mW typ/pkg

MC8311
1-of-16 Decoder



V_{CC} = Pin 24
Gnd = Pin 12

INPUT $\overline{E0}$	$\overline{E1}$	D	C	B	A	OUTPUT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

X = Don't care

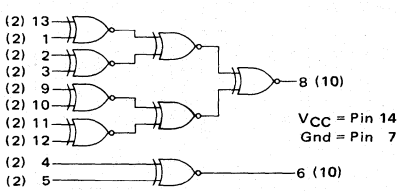
t_{pd} ($\overline{E}$ to Q) = 26 ns typ
P_D = 175 mW typ/pkg

MC54145/MC74145
BCD to 1-of-10 Decoder/Driver

See MC5445/MC7445

PARITY TREES

MC4008/MC4308
8-Bit Parity Tree

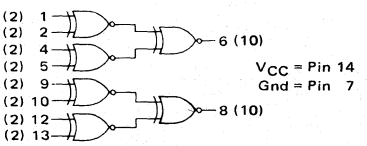


V_{CC} = Pin 14
Gnd = Pin 7

$8 = 1 \odot 2 \odot 3 \odot 9 \odot 10 \odot 11 \odot 12 \odot 13$
$6 = 4 \odot 5$
where $X \odot Y = \overline{X} \cdot \overline{Y} + X \cdot Y$

t_{pd} = 15-30 ns typ
P_D = 150 mW typ/pkg

MC4010
Dual 4-Bit Parity Tree



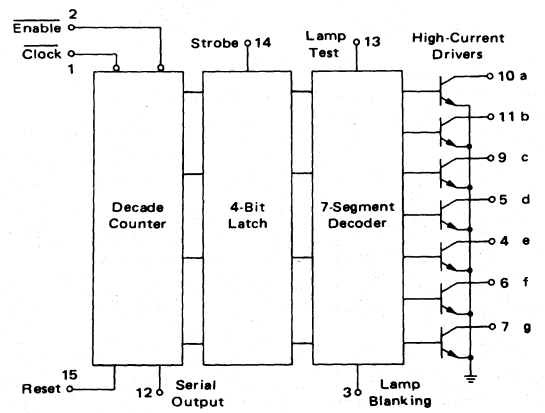
V_{CC} = Pin 14
Gnd = Pin 7

$6 = 1 \odot 2 \odot 4 \odot 5$
where $X \odot Y = \overline{X} \cdot \overline{Y} + X \cdot Y$

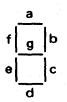
t_{pd} = 9.5-22 ns typ
P_D = 125 mW typ/pkg

LOGIC DIAGRAMS (continued)

COUNTER-LATCH-DECODER



MC4050/MC4350
Monolithic Counter-Latch-Decoder

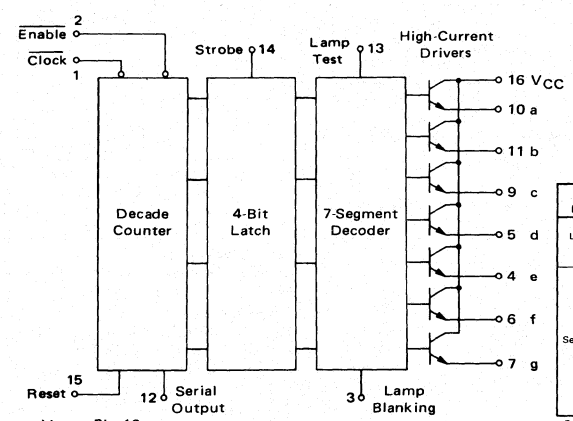


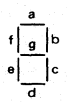
SEGMENT IDENTIFICATION

FUNCTION	INPUT $\overline{C}$	$\overline{E}$	R	S	LT	LB	OUTPUT S_{out}	a	b	c	d	e	f	g
Lamp Test	X	X	X	X	1	X	–	0	0	0	0	0	0	0
Lamp Blanking	X	X	X	X	0	1	–	1	1	1	1	1	1	1
Reset	X	X	1	1	0	0	0	1	1	1	1	1	1	1
Enable	P	1	0	1	0	0	0	1	1	1	1	1	1	1
State Sequence 1	P1	0	0	1	0	0	0	1	0	0	1	1	1	1
2	P2	0	0	1	0	0	0	0	0	1	0	0	1	0
3	P3	0	0	1	0	0	0	0	0	0	0	1	1	0
4	P4	0	0	1	0	0	0	1	0	0	1	1	0	0
5	P5	0	0	1	0	0	0	0	1	0	0	1	0	0
6	P6	0	0	1	0	0	0	0	1	0	0	0	0	0
7	P7	0	0	1	0	0	0	0	0	0	1	1	1	1
8	P8	0	0	1	0	0	0	0	0	0	0	0	0	0
9	P9	0	0	1	0	0	1	0	0	0	0	1	0	0
0	P10	0	0	1	0	0	0	0	0	0	0	0	0	1
1	P11	0	0	1	0	0	0	1	0	0	1	1	1	1
Latch	P	0	0	0	0	0	0	1	0	0	1	1	1	1

P = any number of pulses may be applied
P_n = n pulses on the Clock input
X = Don't care

MC4051
Monolithic Counter-Latch-Decoder





SEGMENT IDENTIFICATION

FUNCTION	INPUT $\overline{C}$	$\overline{E}$	R	S	LT	LB	OUTPUT S_{out}	a	b	c	d	e	f	g
Lamp Test	X	X	X	X	1	X	–	1	1	1	1	1	1	1
Lamp Blanking	X	X	X	X	0	1	–	0	0	0	0	0	0	0
Reset	X	X	1	1	0	0	0	0	0	0	0	0	0	0
Enable	P	1	0	1	0	0	0	0	0	0	0	0	0	0
State Sequence 1	P1	0	0	1	0	0	0	0	1	1	0	0	0	0
2	P2	0	0	1	0	0	0	1	1	0	1	1	0	1
3	P3	0	0	1	0	0	0	1	1	1	1	0	0	1
4	P4	0	0	1	0	0	0	0	0	1	1	0	0	1
5	P5	0	0	1	0	0	0	1	0	1	1	0	1	1
6	P6	0	0	1	0	0	0	1	0	1	1	1	1	1
7	P7	0	0	1	0	0	0	1	1	1	0	0	0	0
8	P8	0	0	1	0	0	0	1	1	1	1	1	1	1
9	P9	0	0	1	0	0	0	1	1	1	1	0	1	1
0	P10	0	0	1	0	0	0	1	1	1	1	1	1	0
1	P11	0	0	1	0	0	0	0	0	1	1	0	0	0
Latch	P	0	0	0	0	0	0	0	0	1	1	0	0	0

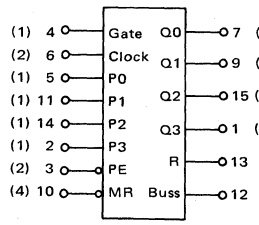
P = any number of pulses may be applied
P_n = n pulses on the Clock input
X = Don't care

LOGIC DIAGRAMS (continued)

COUNTERS

MC4016/MC4316
Programmable Modulo-N Decade Counter

MC4018/MC4318
Programmable Modulo-N Hexadecimal Counter



V_{CC} = Pin 16
Gnd = Pin 8

t_{pd}, Clock to Q3 = 50 ns typ
Clock to Buss = 35 ns typ
P_D = 250 mW typ/pkg

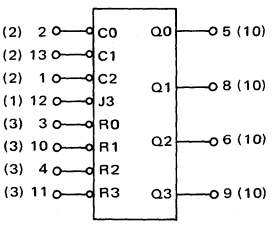
MC4016/MC4316

COUNT	OUTPUT Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC4018/MC4318

COUNT	OUTPUT Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

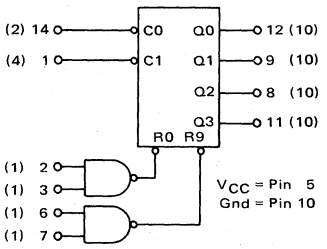
MC4023
4-Bit Universal Counter



V_{CC} = Pin 14
Gnd = Pin 7

t_{pd} = 16 ns typ/bit
P_D = 200 mW typ/pkg
f = 30 MHz typ

MC5490/MC7490
Decade Counter



V_{CC} = Pin 5
Gnd = Pin 10

RESET/COUNT TRUTH TABLE

R0 Pin 2	R0 Pin 3	R9 Pin 6	R9 Pin 7	OUTPUT Q3	Q2	Q1	Q0
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	0	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

X = Don't care.

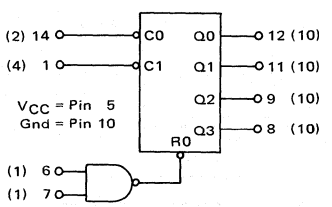
t_{pd} = 20 ns typ/bit
P_D = 160 mW typ/pkg

COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Q0 connected to $\overline{C1}$

MC5492/MC7492
Divide-by-Twelve Counter



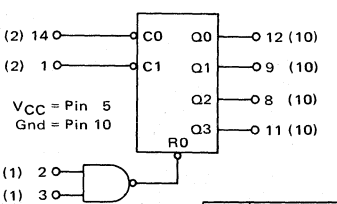
V_{CC} = Pin 5
Gnd = Pin 10

t_{pd} = 60 ns typ
P_D = 160 mW typ/pkg

COUNT	OUTPUT Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

Q0 connected to $\overline{C1}$

MC5493/MC7493
4-Bit Binary Counter



V_{CC} = Pin 5
Gnd = Pin 10

t_{pd} = 20 ns typ/bit
P_D = 160 mW typ/pkg

COUNT	OUTPUT Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

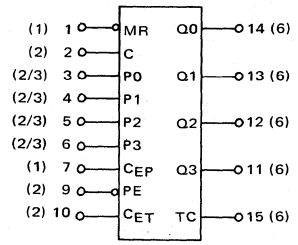
Q0 connected to $\overline{C1}$

(continued)

COUNTERS (continued)

MC8310/MC9310
Presettable Decade Counter

MC8316/MC9316
4-Bit Binary Counter



V_{CC} = Pin 16
Gnd = Pin 8

MC8310/MC9310

COUNT	OUTPUT Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

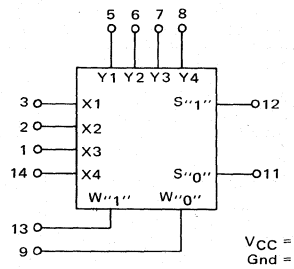
MC8316/MC9316

COUNT	OUTPUT Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

t_{pd} = 14 to 35 ns typ
f_{Tog} = 28 MHz typ
P_D = 300 mW typ/pkg

MEMORIES AND MAGNETIC MEMORY DRIVERS

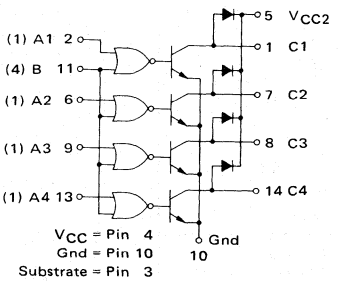
MC4004, MC4005, MC4304, MC4305
16-Bit Scratch Pad Memory Cell



V_{CC} = Pin 4
Gnd = Pin 10

t_{pd}: Write Mode = 25 ns typ
Read Mode = 15 ns typ
P_D = 250 mW typ/pkg

MC4042
Quad Predriver



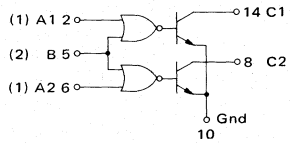
V_{CC} = Pin 4
Gnd = Pin 10
Substrate = Pin 3

TRUTH TABLE
(One gate only)

A1	B	C1
0	0	0
0	1	1
1	0	1
1	1	1

t_{pd} = 15 ns typ
P_D = 120 mW typ/pkg

MC4043
Dual Line Selector



V_{CC} = Pin 4
Gnd = Pin 10
Substrate = Pin 3

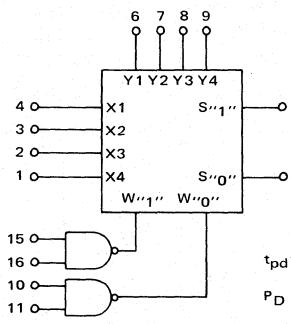
Collectors of Output Transistors:
Gate 1 = Pin 1
Gate 2 = Pin 7

TRUTH TABLE
(One gate only)

A1	B	C1
0	0	0
0	1	1
1	0	1
1	1	1

t_{pd} = 20 ns typ
P_D = 70 mW typ/pkg

MC5484/MC7484
16-Bit Scratch Pad Memory Cell With Gated Inputs



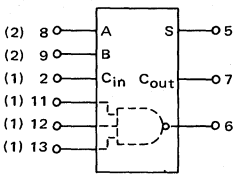
V_{CC} = Pin 5
Gnd = Pin 12

t_{pd}: Write Mode = 25 ns typ
Read Mode = 15 ns typ
P_D = 250 mW typ/pkg

2

ADDERS

MC4026/MC4326
MC4027/MC4327
Full Adder



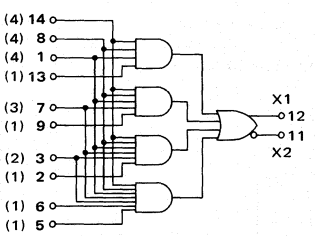
V_{CC} = Pin 4
Gnd = Pin 10

Output Loading Factor:
MC4326 = 15 MTTL I Loads
MC4327 = 7 MTTL I Loads
MC4026 = 12 MTTL I Loads
MC4027 = 6 MTTL I Loads

INPUT			OUTPUT	
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

t_{pd} = (Add Delay) = 25 ns typ
t_{pd} (Carry Delay) = 13 ns typ
P_D = 90 mW typ/pkg

MC4032/MC4332
Carry Decoder



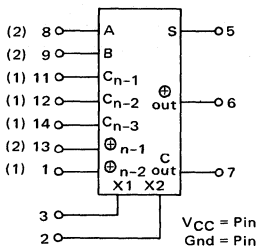
V_{CC} = Pin 4
Gnd = Pin 10

Δt_{pd} = 4.0 ns typ/decoder
1.0 ns typ/pF at expander nodes
P_D = 20 mW typ/pkg

MC4028/MC4328
MC4029/MC4329
Dependent-Carry Fast Adder

MC4030/MC4330
MC4031/MC4331
Independent-Carry Fast Adder

t_{pd} = (Add Delay) = 25 ns typ
t_{pd} (Carry Delay) = 13 ns typ
P_D = 125 mW typ/pkg



V_{CC} = Pin 4
Gnd = Pin 10

Output Loading Factor:
MC4328, MC4330 = 15 MTTL I Loads
MC4329, MC4331 = 7 MTTL I Loads
MC4028, MC4030 = 12 MTTL I Loads
MC4029, MC4031 = 6 MTTL I Loads

CONDENSED TRUTH TABLE FOR THE Nth STAGE

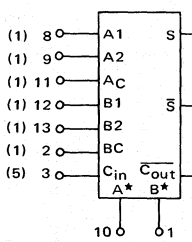
Pin Numbers									
8	9	11	12,13	13, 14, 1	5	6	7		
A	B	C_{n-1}	Note 1	Note 2	S	$\oplus_{out}$	MC4330/4030 MC4331/4031 C_{out}	MC4328/4028 MC4329/4029 C_{out}	Comment Note 3
0	0	0	0	0	0	0	0	0	–
0	0	0	0	1	1	0	0	0	–
0	0	0	1	0	1	0	0	0	–
0	0	0	1	1	1	0	0	0	ϕ
0	0	1	0	0	1	0	0	0	–
0	0	1	0	1	1	0	0	0	ϕ
0	0	1	1	0	1	0	0	0	ϕ
0	0	1	1	1	1	0	0	0	ϕ
0	1	0	0	0	1	1	0	0	–
0	1	0	0	1	0	1	0	1	–
0	1	0	1	0	0	1	0	1	–
0	1	0	1	1	0	1	0	1	ϕ
0	1	1	0	0	0	1	0	1	–
0	1	1	0	1	0	1	0	1	ϕ
0	1	1	1	0	0	1	0	1	ϕ
0	1	1	1	1	0	1	0	1	ϕ
1	0	0	0	0	1	1	0	0	–
1	0	0	0	1	0	1	0	1	–
1	0	0	1	0	0	1	0	1	–
1	0	0	1	1	0	1	0	1	ϕ
1	0	1	0	0	0	1	0	1	–
1	0	1	0	1	0	1	0	1	ϕ
1	0	1	1	0	0	1	0	1	ϕ
1	0	1	1	1	0	1	0	1	ϕ
1	1	0	0	0	0	0	1	1	–
1	1	0	0	1	1	0	1	1	–
1	1	0	1	0	1	0	1	1	–
1	1	0	1	1	1	0	1	1	ϕ
1	1	1	0	0	1	0	1	1	–
1	1	1	0	1	1	0	1	1	ϕ
1	1	1	1	0	1	0	1	1	ϕ
1	1	1	1	1	1	0	1	1	ϕ

Note 1. This column represents the AND function whose inputs are pins 13 and 12, and is defined by the expression $(A_{n-1} \oplus B_{n-1})(C_{n-2})$.

Note 2. This column represents the AND function whose inputs are pins 13, 14, and 1, and is defined by the expression $(A_{n-1} \oplus B_{n-1})(A_{n-2} \oplus B_{n-2})(C_{n-3})$.

Note 3. ϕ = Don't Care. The "Don't Care" occurs for the MC4330-31/4030-31 only, because the C_n and the $\oplus_n$ from any one previous stage entering a given subsequent stage cannot be simultaneously at logic "1".

MC5480/MC7480
Gated Full Adder



V_{CC} = Pin 7
Gnd = Pin 14

(Input = 1.625) (Input = 1.625)
(Output = 3) (Output = 3)

t_{pd} (Add Delay) = 55 ns typ
t_{pd} (Carry Delay = 10 ns typ
P_D = 105 mW typ/pkg

C_{in}	B	A	$\overline{C_{out}}$	$\bar{S}$	S
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

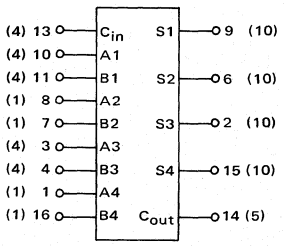
1. $A = \overline{A^* \cdot A_C}$, $B = \overline{B^* \cdot B_C}$
where $A^* = \overline{A_1 \cdot A_2}$
$B^* = \overline{B_1 \cdot B_2}$
2. When A^* (or B^*) is used as an input, A1 and A2 (or B1 and B2) must be connected to ground.
3. When A1 and A2 (or B1 and B2) are used as inputs, A^* (or B^*) must be open, or used to perform wired-OR logic.

(continued)

LOGIC DIAGRAMS (continued)

ADDERS (continued)

MC5483/MC7483
4-Bit Binary Adder



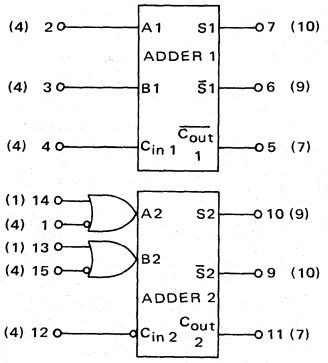
V_{CC} = Pin 5
Gnd = Pin 12

INPUT				OUTPUT							
				When C_{in} = 0			When C_{in} = 1				
						When C2 = 0				When C2 = 1	
A1 / A3	B1 / B3	A2 / A4	B2 / B4	S1 / S3	S2 / S4	C2 / C_o	S1 / S3	S2 / S4	C2 / C_o
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	1	0	1	1	0
1	0	1	1	1	1	0	0	0	1
0	1	1	1	1	1	0	0	0	1
1	1	1	1	0	1	1	1	1	1

Input conditions at A1, A2, B1, B2, and C_{in} are used to determine outputs S1 and S2, and the value of the internal carry, C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs S3, S4, and C_{out}.

t_{pd} = 35 ns typ
P_D = 390 mW typ/pkg

MC8304/MC9304
Dual Full Adder



V_{CC} = Pin 16
Gnd = Pin 8

ADDER 1

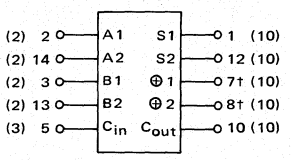
INPUT			OUTPUT		
C_{in} 1	B1	A1	$\overline{C_o}$ 1	$\overline{S1}$	S1
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

ADDER 2

INPUT					OUTPUT		
$\overline{C_{in}}$ 2	B2	A2	$\overline{B2}$	$\overline{A2}$	C_o 2	S2	$\overline{S2}$
0	0	0	0	0	1	1	0
0	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	1	1	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	0	1
0	0	1	1	1	0	1	0
0	1	0	0	0	1	1	0
0	1	0	0	1	1	1	0
0	1	0	1	0	1	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0
0	1	1	0	1	1	1	0
0	1	1	1	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	0	1	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	1	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	1	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	1
1	1	0	0	1	0	1	0
1	1	0	1	0	0	1	0
1	1	0	1	1	0	1	0
1	1	1	0	0	1	0	1
1	1	1	0	1	1	0	1
1	1	1	1	0	1	0	1
1	1	1	1	1	1	0	1

t_{pd} = 8.0 to 28 ns typ
P_D = 110 mW typ/pkg

MC15482/MC17482
MC25482/MC27482
2-Bit Full Adder



V_{CC} = Pin 4
Gnd = Pin 11

t_{pd} (Add Delay) = 15 ns
t_{pd} (Carry Delay) = 12 ns
P_D = 165 mW typ/pkg

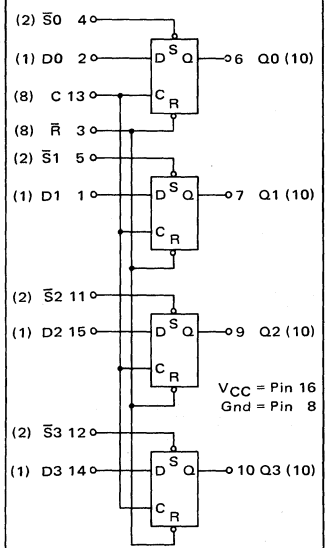
INPUT				OUTPUT							
				C_{in} = 0			C_{in} = 1				
A1	B1	A2	B2	S1	S2	C_o	S1	S2	C_o	⊕1†	⊕2†
0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	1	0	1	0
0	1	0	0	1	0	0	0	1	0	1	0
1	1	0	0	0	1	0	1	1	0	0	0
0	0	1	0	0	1	0	1	1	0	0	1
1	0	1	0	1	1	0	0	0	1	1	1
0	1	1	0	1	1	0	0	0	1	1	1
1	1	1	0	0	0	1	1	0	1	0	1
0	0	0	1	0	1	0	1	1	0	0	1
1	0	0	1	1	1	0	0	0	1	1	1
0	1	0	1	1	1	0	0	0	1	1	1
1	1	0	1	0	0	1	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	0	0
1	0	1	1	1	0	1	0	1	1	1	0
0	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	0	1	1	1	1	0	0	0

†Available only on MC25482/27482

LOGIC DIAGRAMS (continued)

FLIP-FLOPS

MC4015
Quad Type D Flip-Flop

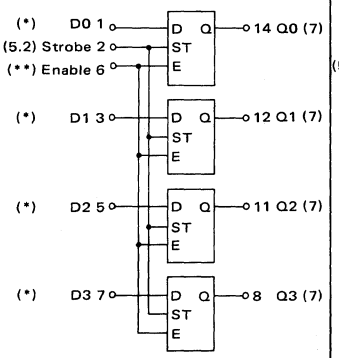


D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse
Q_n = time period following clock pulse

t_{pd} = 16 ns typ
P_D = 190 mW typ/pkg

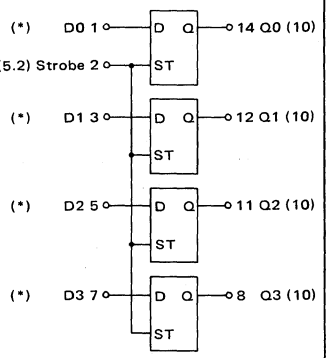
MC4035/MC4335
Quad Latch
(Open Collector)



Two 5.0 kilohm pullup resistors are internally connected to V_{CC} and brought out on pins 9 and 13.

t_{pd} = 25 ns typ
P_D = 140 mW typ/pkg

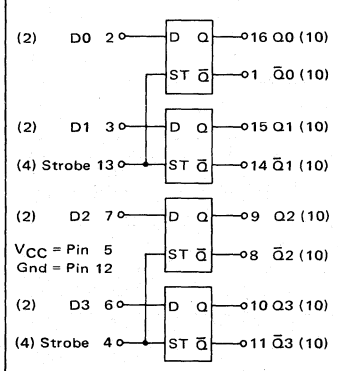
MC4037/MC4337
Quad Latch



t_{pd} = 25 ns typ
P_D = 150 mW typ/pkg

All loading factors are for MTTL I loads.
*MC4035, MC4037 = 4.0; MC4335, MC4337 = 4.2 (Strobe High)
MC4035, MC4037 = 0.9; MC4335, MC4337 = 1.1 (Strobe Low)
**MC4035 = 3.6, MC4335 = 4.0

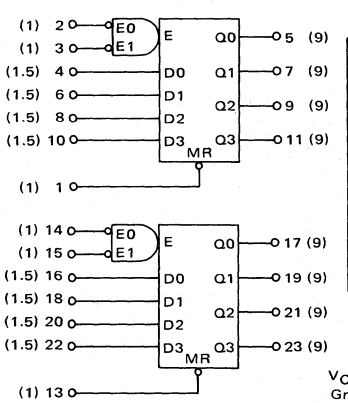
MC7475
Quad Latch



t_n	t_{n+1}	
D	Q	Q̄
1	1	0
0	0	1

t_{pd} = 30 ns typ
P_D = 160 mW typ/pkg

MC8308
Dual 4-Bit Latch



INPUTS							OUTPUTS			
$\overline{MR}$	$\overline{E}0$	$\overline{E}1$	D3	D2	D1	D0	Q3	Q2	Q1	Q0
1	0	0	0	0	0	1	0	0	0	1
1	0	0	0	0	1	0	0	0	1	0
1	0	0	0	1	0	0	0	1	0	0
1	0	0	0	1	0	1	0	0	1	1
1	0	0	0	1	1	0	0	1	0	0
1	0	0	0	1	1	1	0	1	1	1
1	0	0	1	0	0	0	1	0	0	0
1	0	0	1	0	0	1	1	0	0	1
1	0	0	1	0	1	0	1	0	1	0
1	0	0	1	0	1	1	1	0	1	1
1	0	0	1	1	0	0	1	1	0	0
1	0	0	1	1	0	1	1	1	0	1
1	0	0	1	1	1	0	1	1	1	0
1	0	0	1	1	1	1	1	1	1	1
1	0	1	X	X	X	X	LATCHED			
1	1	0	X	X	X	X	LATCHED			
1	1	1	X	X	X	X	LATCHED			
0	X	X	X	X	X	X	0	0	0	0

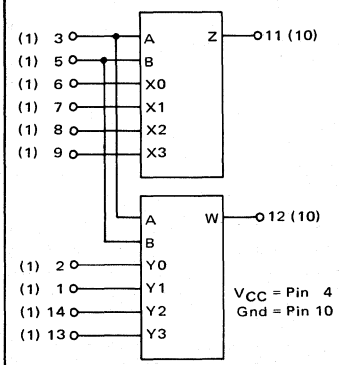
X = Don't Care

t_{pd} (E to Q) = 25 ns typ
P_D = 325 mW typ/pkg

LOGIC DIAGRAMS (continued)

DATA ROUTING FUNCTIONS

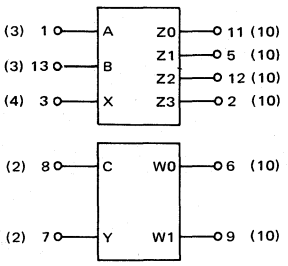
MC4000/MC4300
Dual 4-Channel Data Selector



$Z = ABX0 + A\overline{B}X1 + \overline{A}BX2 + \overline{A}\overline{B}X3$
$W = ABY0 + A\overline{B}Y1 + \overline{A}BY2 + \overline{A}\overline{B}Y3$

t_{pd} = 11 ns typ
P_D = 150 mW typ/pkg

MC4002
Dual Data Distributor

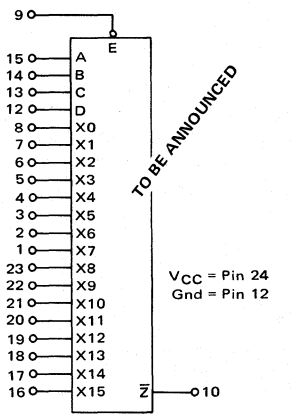


$Z0 = ABX$
$Z1 = A\overline{B}X$
$Z2 = \overline{A}BX$
$Z3 = \overline{A}\overline{B}X$
$W0 = \overline{C}Y$
$W1 = CY$

V_{CC} = Pin 4
Gnd = Pin 10

t_{pd} = 10.5 ns typ
P_D = 175 mW typ/pkg

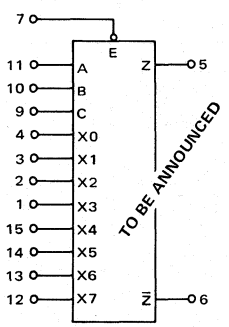
MC54150/MC74150
16-Channel Data Selector



$Z = E \bullet (\overline{A}\overline{B}\overline{C}\overline{D}\ X0 + A\overline{B}\overline{C}\overline{D}\ X1 + \overline{A}B\overline{C}\overline{D}\ X2 + AB\overline{C}\overline{D}\ X3 + \overline{A}\overline{B}C\overline{D}\ X4 + A\overline{B}C\overline{D}\ X5 + \ldots + ABCD\ X15)$

t_{pd} = 8.5 to 35 ns typ
P_D = 200 mW typ/pkg

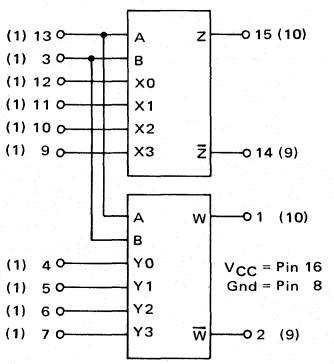
MC54151/MC74151
8-Channel Data Selector



$Z = E \bullet (\overline{A}\overline{B}\overline{C}X0 + A\overline{B}\overline{C}X1 + \overline{A}B\overline{C}X2 + AB\overline{C}X3 + \overline{A}\overline{B}CX4 + A\overline{B}CX5 + \overline{A}BCX6 + ABCX7)$

t_{pd} = 8.5 to 35 ns typ
P_D = 145 mW typ/pkg

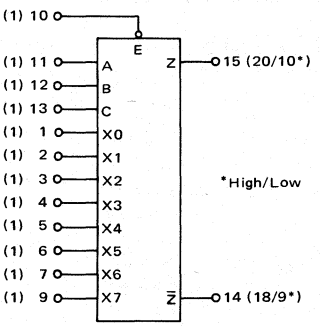
MC8309/MC9309
Dual 4-Channel Data Selector



$Z = \overline{A}\overline{B}X0 + A\overline{B}X1 + \overline{A}BX2 + ABX3$
$\overline{Z} = \overline{A}\overline{B}\overline{X0} + A\overline{B}\overline{X1} + \overline{A}B\overline{X2} + AB\overline{X3}$
$W = \overline{A}\overline{B}Y0 + A\overline{B}Y1 + \overline{A}BY2 + ABY3$
$\overline{W} = \overline{A}\overline{B}\overline{Y0} + A\overline{B}\overline{Y1} + \overline{A}B\overline{Y2} + AB\overline{Y3}$

t_{pd} = 9.0 to 24 ns typ
P_D = 150 mW typ/pkg

MC8312/MC9312
8-Channel Data Selector



VCC = Pin 16
Gnd = Pin 8

$Z = E \bullet (\overline{A}\overline{B}\overline{C}X0 + A\overline{B}\overline{C}X1 + \overline{A}B\overline{C}X2 + AB\overline{C}X3 + \overline{A}\overline{B}CX4 + A\overline{B}CX5 + \overline{A}BCX6 + ABCX7)$

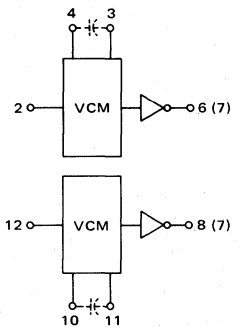
$\overline{Z} = E \bullet (\overline{A}\overline{B}\overline{C}\overline{X0} + A\overline{B}\overline{C}\overline{X1} + \overline{A}B\overline{C}\overline{X2} + AB\overline{C}\overline{X3} + \overline{A}\overline{B}C\overline{X4} + A\overline{B}C\overline{X5} + \overline{A}BC\overline{X6} + ABC\overline{X7})$

t_{pd} = 9.0 to 24 ns typ
P_D = 135 mW typ/pkg

2

MULTIVIBRATORS

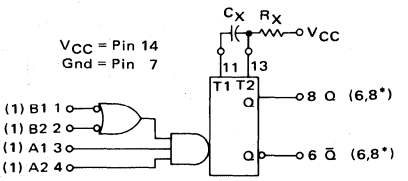
MC4024/MC4324
Dual Voltage-Controlled Multivibrator



V_{CC}: VCM = 1, 13
Output Buffer = 14
Gnd: VCM = 5, 9
Output Buffer = 7
External Capacitor for Frequency Range Determination

P_D = 150 mW typ/pkg
f = 30 MHz typ

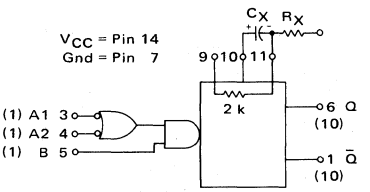
MC8601/MC9601
Retriggerable Monostable Multivibrator



*MC9601, MC8601

t_{pd} = 25 ns typ
P_D = 75 mW typ/pkg

MC54121/MC74121
Monostable Multivibrator



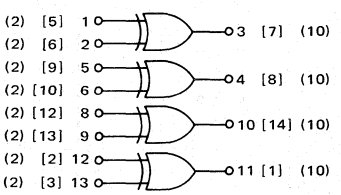
t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	Triggering
X	0	0	X	0	1	Triggering
1	1	1	X	0	1	Triggering
1	1	1	0	X	1	Triggering
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

X = Don't care
t_n = Time period prior to input transition
t_{n+1} = Time period following input transition

t_{pd}, B to Q = 35 ns typ
P_D = 90 mW typ/pkg (50% duty cycle)

EXCLUSIVE GATES

MC7241/MC8241
Quad Exclusive OR Gate



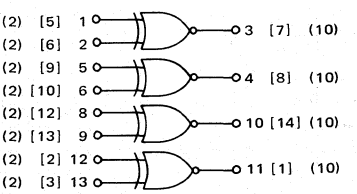
V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 10 ns typ
P_D = 225 mW typ/pkg

Numbers at ends of terminals represent pin numbers for devices in the dual in-line package.
Numbers in brackets represent pin numbers for devices in the flat package.

MC7242/MC8242
Quad Exclusive NOR Gate (Open Collector)



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

$3 = \overline{1} \cdot \overline{2} + 1 \cdot 2$

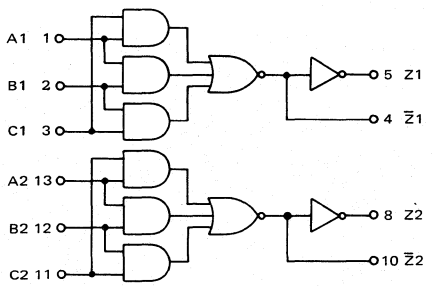
t_{pd} = 18 ns typ
P_D = 170 mW typ/pkg

Numbers at ends of terminals represent pin numbers for devices in the dual in-line package.
Numbers in brackets represent pin numbers for devices in the flat package.

LOGIC DIAGRAMS (continued)

MAJORITY LOGIC GATE

MC4062
Dual Majority Logic Gate



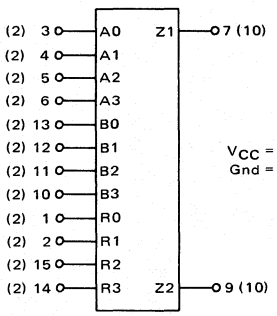
V_{CC} = Pin 14
Gnd = Pin 7

INPUT			OUTPUT	
A	B	C	Z	$\overline{Z}$
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

t_{pd} = 20 ns typ ($\overline{Z}$ Output)
11 ns typ (Z Output)
P_D = 75 mW typ/pkg

COMPARATORS

MC4021, MC4022
Dual 4-Bit Comparator



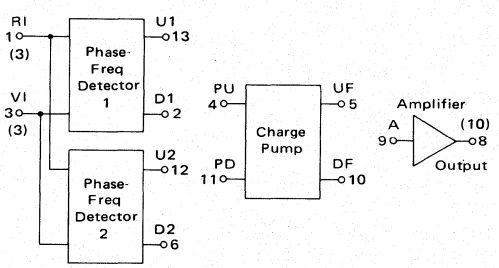
V_{CC} = Pin 16
Gnd = Pin 8

A0	A1	A2	A3	B0	B1	B2	B3	R0	R1	R2	R3	Z1	Z2
0	0	0	0	0	0	1	1	0	0	0	1	1	0
0	0	0	0	0	0	1	1	0	0	0	1	0	0
0	0	0	0	0	0	1	1	0	0	0	1	0	1
0	1	1	0	0	1	0	1	0	1	1	0	0	0
0	1	1	1	0	1	0	0	0	1	1	0	0	1
0	1	1	1	0	1	0	0	0	1	1	0	0	0
1	0	0	1	1	0	0	0	0	0	0	1	1	0
1	0	0	0	1	0	0	0	0	0	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	1	1	1	1	0	0	1

t_{pd} = 20 ns typ
P_D = 250 mW typ/pkg

PHASE-FREQUENCY DETECTOR

MC4044/MC4344
Phase-Frequency Detector



V_{CC} = Pin 14
Gnd = Pin 7

t_{pd} (thru phase detector) = 9.0 ns typ
P_D = 85 mW typ/pkg

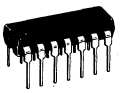
MTTL

MC5400/MC7400 SERIES INTEGRATED CIRCUITS

MTTL

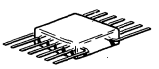
MC5400 Series (–55 to +125°C)
MC7400 Series (0 to +70°C)

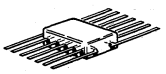
MC5400/MC7400 series integrated circuits comprise a family of transistor-transistor logic designed for general purpose digital applications. The family has a medium operating speed (15-30 MHz clock rate), good external noise immunity, high fan out, and the capability of driving capacitive loads of up to 600 pF.



P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116

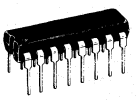
F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

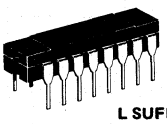




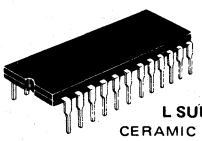
F SUFFIX
CERAMIC PACKAGE
CASE 609
TO-85

P SUFFIX
PLASTIC PACKAGE
CASE 612

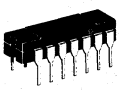




L SUFFIX
CERAMIC PACKAGE
CASE 620

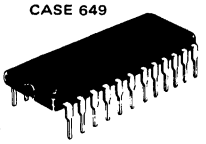


L SUFFIX
CERAMIC PACKAGE
CASE 623



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 649



MAXIMUM RATINGS

Rating		Value	Unit
Power Supply Voltage		7.0	Vdc
Input Voltage		5.5	Vdc
Operating Temperature Range	MC5400 MC7400	–55 to +125 0 to +70	°C
Storage Temperature Range – Ceramic Plastic		–65 to +150 –55 to +125	°C

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Function	Type ①				Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg
	–55 to +125°C	Case ②	0 to +70°C	Case ②			
Quad 2-Input NAND Gate	MC5400F,L	607, 632	MC7400F,L,P	607,632,605	10	10	40
Quad 2-Input NAND Gate (Open Collector Output)	MC5401F,L	607, 632	MC7401F,L,P	607,632,605	10	35	40
Quad 2-Input NOR Gate	MC5402F,L	607, 632	MC7402F,L,P	607,632,605	10	10	40
Quad 2-Input NAND Gate (With Open Collector)	MC5403L	632	MC7403L,P	605, 632	10	35	40
Hex Inverter	MC5404F,L	607, 632	MC7404F,L,P	607,632,605	10	13	60
Hex Inverter	MC5405L	632	MC7405L,P	632, 605	10	35	60
Triple 3-Input NAND Gate	MC5410F,L	607, 632	MC7410F,L,P	607,632,605	10	10	30
Dual 4-Input NAND Gate	MC5420F,L	607, 632	MC7420F,L,P	607,632,605	10	10	20
Quad 2-Input Interface NAND Gate	MC5426L	632	MC7426L,P	632, 605	10	17	40
8-Input NAND Gate	MC5430F,L	607, 632	MC7430F,L,P	607,632,605	10	10	10
Dual 4-Input NAND Buffer	MC5440F,L	607, 632	MC7440F,L,P	607,632,605	30	13	50
BCD-to-Decimal Decoder and High-Level Driver	–	–	MC7441AL,P	620, 612	–	–	105
BCD-to-Decimal Decoder	MC5442L	620	MC7442L,P	620, 612	10	22/23#	140
Excess Three-to-Decimal Decoder	MC5443L	620	MC7443L,P	620, 612	10	22/23#	140
Excess Three Gray-to-Decimal Decoder	MC5444L	620	MC7444L,P	620, 612	10	22/23#	140

① F suffix denotes Flat Package. L suffix denotes Dual In-Line Ceramic Package. P suffix denotes Dual In-Line Plastic Package.

② Devices formerly using Case 609 (TO-85) are now being manufactured in Case 607 (TO-86). Either package may be shipped during the transition.

(continued)

*Add delay/Carry delay. # 2 Logic Levels/3 Logic Levels.

FUNCTIONS AND CHARACTERISTICS (continued)

Function	Type ①				Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg
	-55 to +125°C	Case ②	0 to +70°C	Case ②			
BCD to One-of-Ten Decoder/Driver	MC5445L	620	MC7445L,P	620, 612	–	50 max	215
BCD-to-Seven Segment Decoder/Driver	MC5446L	620	MC7446L,P	620, 612	BI/RBO 5	–	265
BCD-to-Seven Segment Decoder/Driver	MC5447L	620	MC7447L,P	620, 612	BI/RBO 5	–	265
BCD-to-Seven Segment Decoder/Driver	MC5448L	620	MC7448L,P	620, 612	BI/RBO = 5 a thru g = 4	–	265
BCD-to-Seven Segment Decoder/Driver	MC5449F	607	MC7449F	607	6	–	165
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC5450F,L	607, 632	MC7450F,L,P	607,632,605	10	13	28
Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC5451F,L	607, 632	MC7451F,L,P	607,632,605	10	13	28
Expandable 4-Wide 2-Input AND-OR-INVERT Gate	MC5453F,L	607, 632	MC7453F,L,P	607,632,605	10	13	22
4-Wide 2-Input AND-OR-INVERT Gate	MC5454F,L	607, 632	MC7454F,L,P	607,632,605	10	13	22
Dual 4-Input Expander for AND-OR-INVERT Gates	MC5460F,L	607, 632	MC7460F,L,P	607,632,605	–	5.0	8.0
J-K Flip-Flop	MC5470L	632	MC7470L,P	632, 605	10	30	65
J-K Flip-Flop	MC5472F,L	607, 632	MC7472F,L,P	607,632,605	10	30	40
Dual J-K Flip-Flop	MC5473F,L	607, 632	MC7473F,L,P	607,632,605	10	30	80
Quad Latch	–	–	MC7475P	612	10	30	160
Dual J-K Flip-Flop	–	–	MC7476P	612	10	30	80
Dual Type D Flip-Flop	MC5479F,L	607, 632	MC7479F,L,P	607,632,605	10	16	84
Gated Full Adder	MC5480L	632	MC7480L,P	632, 605	$S,\overline{S}$ = 10 $\overline{C}_{out}$ = 5 A★,B★, = 3	10/55*	105
2-Bit Full Adder	MC15482F,L	607, 632	MC17482F,L,P	607,632,605	10	15/12*	165
2-Bit Full Adder	MC25482F,L	607, 632	MC27482F,L,P	607,632,605	10	25/12*	165
4-Bit Binary Full Adder	MC5483L	620	MC7483L,P	620, 612	S = 10 C_{out} = 5	35	390
16-Bit Scratch Pad Memory Cell With Gated Inputs	MC5484L	620	–	–	I_{OL} = 40 mA Open Collector I_{OL} = 20 mA	Write Mode: 25 Sense Mode: 15	250
	–	–	MC7484L,P	620, 612			
Decade Counter	MC5490F,L	607, 632	MC7490F,L,P	607,632,605	10	20/bit	160
8-Bit Shift Register	MC5491AL	632	MC7491AL,P	632, 605	10	25	175
Divide-by-Twelve Counter	MC5492F,L	607, 632	MC7492F,L,P	607,632,605	10	60	160
4-Bit Binary Counter	MC5493L	632	MC7493L,P	632, 605	10	20/bit	160
4-Bit Shift Register	†MC5494L	620	†MC7494P	612	–	25	175
4-Bit Shift Register	MC5495F,L	607, 632	MC7495F,L,P	607,632,605	10	25	250
5-Bit Shift Register	MC5496L	620	MC7496P	612	–	25	240
Dual J-K Flip-Flop	MC54107L	632	MC74107L,P	632, 605	10	30	80
Monostable Multivibrator	MC54121F,L	607, 632	MC74121F,L,P	607,632,605	10	t_{pd+}, B to Q = 35	90
BCD to One-of-Ten Decoder/Driver	MC54145L	620	MC74145L,P	620, 612	–	50 max	215
16-Channel Data Selector	†MC54150L	623	†MC74150P	649	–	8.5 to 35	200
8-Channel Data Selector	†MC54151L	620	†MC74151P	612	–	8.5 to 35	145

① F suffix denotes Flat Package. L suffix denotes Dual In-Line Ceramic Package. P suffix denotes Dual In-Line Plastic Package.

② Devices formerly using Case 609 (TO-85) are now being manufactured in Case 607 (TO-86). Either package may be shipped during the transition.

*Add delay/Carry delay. # 2 Logic Levels/3 Logic Levels. †To be announced.

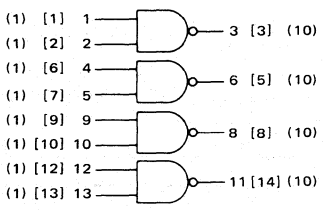
LOGIC DIAGRAMS (continued)

Numbers at ends of terminals represent pin numbers for devices in the dual in-line package.
Numbers in brackets represent pin numbers for devices in the flat package.
Numbers in parenthesis indicate loading.
Logic equations are for devices in the dual in-line package.

GATES

Flat Package: V_{CC} = Pin 4, Gnd = Pin 11. Dual In-Line Package: V_{CC} = Pin 14, Gnd = Pin 7 unless otherwise noted.

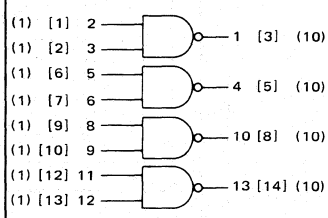
MC5400/MC7400
Quad 2-Input NAND Gate



$3 = \overline{1 \cdot 2}$

t_{pd} = 10 ns typ
P_D = 40 mW typ/pkg

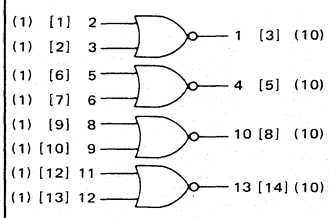
MC5401/MC7401
Quad 2-Input NAND Gate
(Open Collector Output)



$1 = \overline{2 \cdot 3}$

t_{pd} = 35 ns typ
P_D = 40 mW typ/pkg

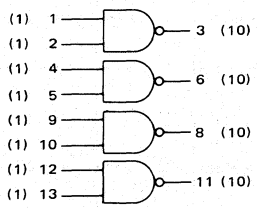
MC5402/MC7402
Quad 2-Input NOR Gate



$1 = \overline{2 + 3}$

t_{pd} = 10 ns typ
P_D = 40 mW typ/pkg

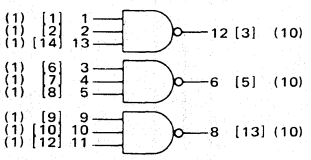
MC5403/MC7403
Quad 2-Input NAND Gate
(Open Collector Output)



$3 = \overline{1 \cdot 2}$

t_{pd} = 35 ns typ
P_D = 40 mW typ/pkg

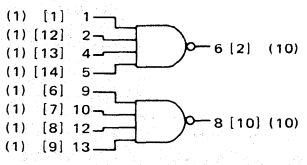
MC5410/MC7410
Triple 3-Input NAND Gate



$12 = \overline{1 \cdot 2 \cdot 13}$

t_{pd} = 10 ns typ
P_D = 30 mW typ/pkg

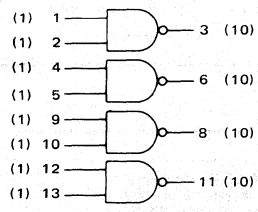
MC5420/MC7420
Dual 4-Input NAND Gate



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

t_{pd} = 10 ns typ
P_D = 20 mW typ/pkg

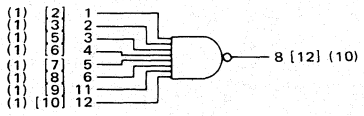
MC5426/MC7426
Quad 2-Input Interface NAND Gate



$3 = \overline{1 \cdot 2}$

t_{pd} = 17 ns typ
P_D = 40 mW typ/pkg

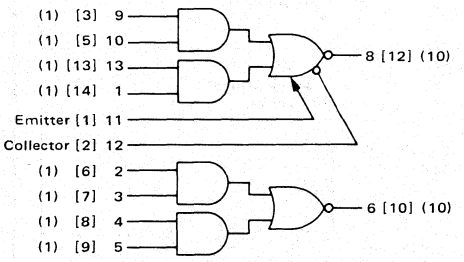
MC5430/MC7430
8-Input NAND Gate



$8 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 5 \cdot 6 \cdot 11 \cdot 12}$

t_{pd} = 10 ns typ
P_D = 10 mW typ/pkg

MC5450/MC7450
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate



$8 = \overline{(9 \cdot 10) + (13 \cdot 1)} + (\text{Expanders})$

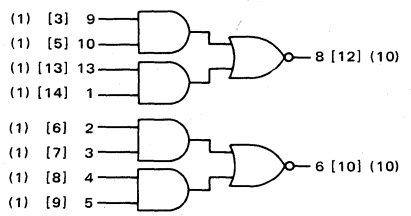
t_{pd} = 13 ns typ
P_D = 28 mW typ/pkg

(continued)

LOGIC DIAGRAMS (continued)

GATES (continued)

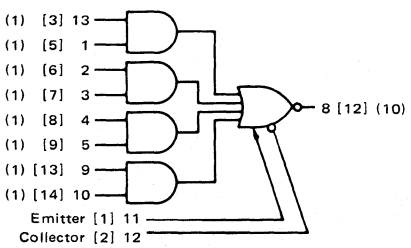
MC5451/MC7451
Dual 2-Wide 2-Input AND-OR-INVERT Gate



$8 = \overline{(9 \cdot 10) + (13 \cdot 1)}$

t_{pd} = 13 ns typ
P_D = 28 mW typ/pkg

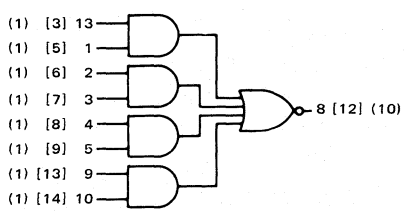
MC5453/MC7453
Expandable 4-Wide 2-Input AND-OR-INVERT Gate



$8 = \overline{(13 \cdot 1) + (2 \cdot 3) + (4 \cdot 5) + (9 \cdot 10) + (\text{Expanders})}$

t_{pd} = 13 ns typ
P_D = 22 mW typ/pkg

MC5454/MC7454
4-Wide 2-Input AND-OR-INVERT Gate

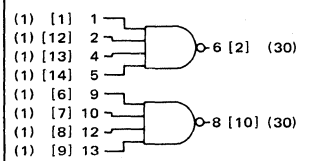


$8 = \overline{(13 \cdot 1) + (2 \cdot 3) + (4 \cdot 5) + (9 \cdot 10)}$

t_{pd} = 13 ns typ
P_D = 22 mW typ/pkg

BUFFER

MC5440/MC7440
Dual 4-Input NAND Buffer

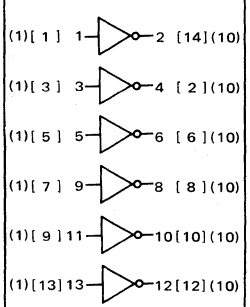


$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

t_{pd} = 13 ns typ
P_D = 50 mW typ/pkg

INVERTERS

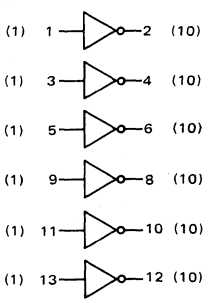
MC5404/MC7404
Hex Inverter



$2 = \overline{1}$

t_{pd} = 13 ns typ
P_D = 60 mW typ/pkg

MC5405/MC7405
Hex Inverter (Open Collector)

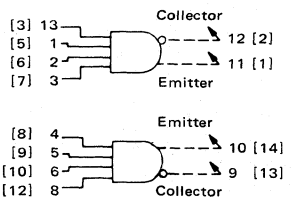


$2 = \overline{1}$

t_{pd} = 35 ns typ
P_D = 60 mW typ/pkg

EXPANDER

MC5460/MC7460
Dual 4-Input Expander for AND-OR-INVERT Gates



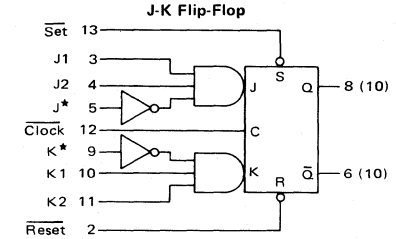
t_{pd} = 5.0 ns typ
P_D = 8.0 mW typ/pkg

A maximum of 4 Expanders may be connected to the MC7450/MC5450 or MC7453/MC5453.

LOGIC DIAGRAMS (continued)

FLIP-FLOPS

MC5470/MC7470
J-K Flip-Flop

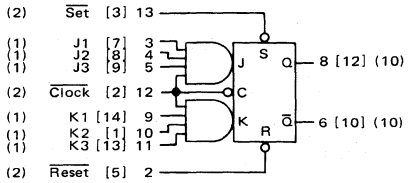


t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

$J = J1 \cdot J2 \cdot \overline{J^*}$
$K = K1 \cdot K1 \cdot \overline{K^*}$

t_{pd} = 30 ns typ
P_D = 65 mW typ/pkg

MC5472/MC7472
J-K Flip-Flop

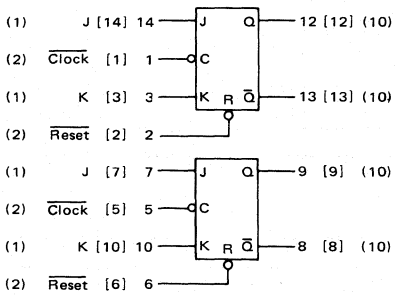


t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

$J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$

f = 20 MHz
P_D = 40 mW typ/pkg

MC5473/MC7473
Dual J-K Flip-Flop

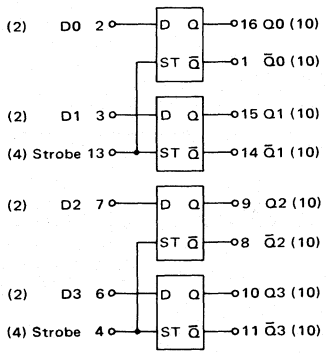


t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

f = 15 MHz
P_D = 80 mW typ/pkg

V_{CC} = Pin 4, Gnd = Pin 11 for both packages.

MC7475
Quad Latch

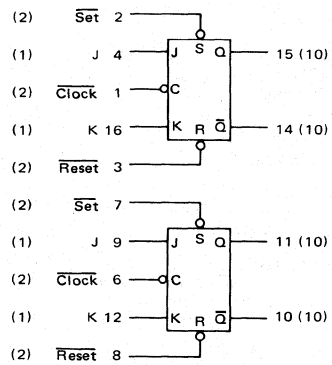


V_{CC} = Pin 5
Gnd = Pin 12

t_n	t_{n+1}	
D	Q	Q̄
1	1	0
0	0	1

t_{pd} = 30 ns typ
P_D = 160 mW typ/pkg

MC7476
Dual J-K Flip-Flop



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

f = 15 MHz
P_D = 80 mW typ/pkg

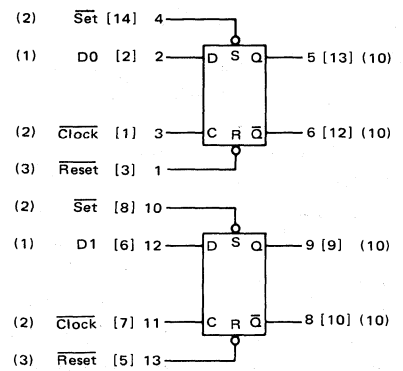
16 Pin Package
V_{CC} = Pin 5, GND = Pin 13

(continued)

LOGIC DIAGRAMS (continued)

FLIP-FLOPS (continued)

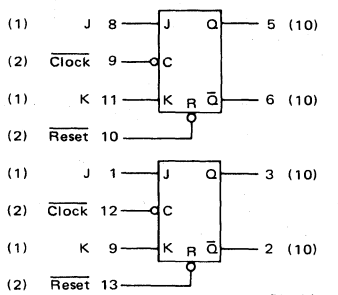
MC5479/MC7479
Dual Type D Flip-Flop



t_n		t_{n+1}	
D		Q	$\overline{Q}$
0		0	1
1		1	0

f = 30 MHz
P_D = 84 mW typ/pkg

MC54107/MC74107
Dual J-K Flip Flop



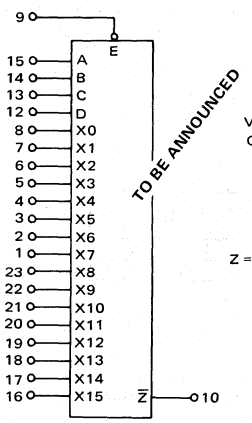
V_{CC} = Pin 14
Gnd = Pin 7

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

f = 15 MHz
P_D = 80 mW typ/pkg

DATA ROUTING FUNCTIONS

MC54150/MC74150
16-Channel Data Selector

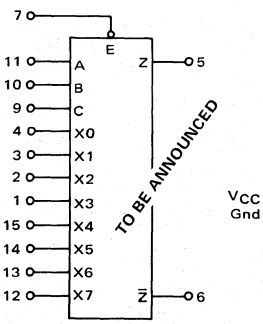


V_{CC} = Pin 24
Gnd = Pin 12

$Z = E \bullet (\overline{A}\overline{B}\overline{C}\overline{D}\,X0 + A\overline{B}\overline{C}\overline{D}\,X1 + \overline{A}B\overline{C}\overline{D}\,X2 + AB\overline{C}\overline{D}\,X3 + \overline{A}\overline{B}C\overline{D}\,X4 + A\overline{B}C\overline{D}\,X5 + \ldots + ABCD\,X15)$

t_{pd} = 8.5 to 35 ns typ
P_D = 200 mW typ/pkg

MC54151/MC74151
8-Channel Data Selector



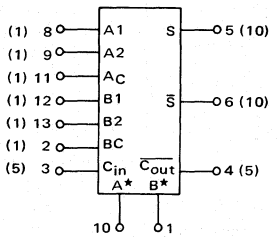
V_{CC} = Pin 16
Gnd = Pin 8

$Z = E \bullet (\overline{A}\overline{B}\overline{C}X0 + A\overline{B}\overline{C}X1 + \overline{A}B\overline{C}X2 + AB\overline{C}X3 + \overline{A}\overline{B}CX4 + A\overline{B}CX5 + \overline{A}BCX6 + ABCX7)$

t_{pd} = 8.5 to 35 ns typ
P_D = 145 mW typ/pkg

ADDERS

MC5480/MC7480
Gated Full Adder



V_{CC} = Pin 7
Gnd = Pin 14

t_{pd} (Add Delay) = 55 ns typ
t_{pd} (Carry Delay = 10 ns typ
P_D = 105 mW typ/pkg

C_{in}	B	A	$\overline{C_{out}}$	$\overline{S}$	S
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

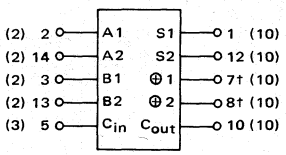
1. $A = \overline{A^* \cdot A_C}$, $B = \overline{B^* \cdot B_C}$

   where $A^* = \overline{A_1 \cdot A_2}$

   $B^* = \overline{B_1 \cdot B_2}$

2. When A^* (or B^*) is used as an input, A1 and A2 (or B1 and B2) must be connected to ground.
3. When A1 and A2 (or B1 and B2) are used as inputs, A^* (or B^*) must be open, or used to perform wired-OR logic.

MC15482/MC17482
MC25482/MC27482
2-Bit Full Adder



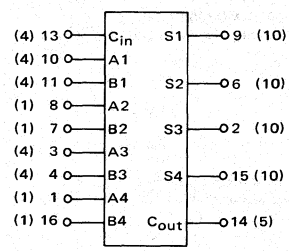
V_{CC} = Pin 4
Gnd = Pin 11

t_{pd} (Add Delay) = 15 ns
t_{pd} (Carry Delay) = 12 ns
P_D = 165 mW typ/pkg

†Available only on MC25482/27482

INPUT				OUTPUT							
				C_{in} = 0			C_{in} = 1				
A1	B1	A2	B2	S1	S2	C_0	S1	S2	C_0	⊕1†	⊕2†
0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	1	0	1	0
0	1	0	0	1	0	0	0	1	0	1	0
1	1	0	0	0	1	0	1	1	0	0	0
0	0	1	0	0	1	0	1	1	0	0	1
1	0	1	0	1	1	0	0	0	1	1	1
0	1	1	0	1	1	0	0	0	1	1	1
1	1	1	0	0	0	1	1	0	1	0	1
0	0	0	1	0	1	0	1	1	0	0	1
1	0	0	1	1	1	0	0	0	1	1	1
0	1	0	1	1	1	0	0	0	1	1	1
1	1	0	1	0	0	1	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	0	0
1	0	1	1	1	0	1	0	1	1	1	0
0	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	0	1	1	1	1	1	0	0

MC5483/MC7483
4-Bit Binary Adder



V_{CC} = Pin 5
Gnd = Pin 12

t_{pd} = 35 ns typ
P_D = 390 mW typ/pkg

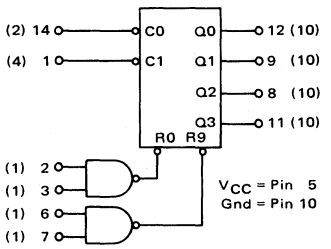
INPUT				OUTPUT											
				When C_{in} = 0						When C_{in} = 1					
				When C2 = 0			When C2 = 1			When C2 = 0			When C2 = 1		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	S1 / S3	S2 / S4	C2	S1 / S3	S2 / S4	C2	S1 / S3	S2 / S4	C_0	S1 / S3	S2 / S4	C_0
0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0
1	0	0	0	1	0	0	0	1	0	0	1	0	1	1	0
0	1	0	0	1	0	0	0	1	0	0	1	0	1	1	0
1	1	0	0	0	1	0	1	1	0	1	1	0	0	0	1
0	0	1	0	0	1	0	1	1	0	1	1	0	0	0	1
1	0	1	0	1	1	0	0	0	1	0	0	1	1	0	1
0	1	1	0	1	1	0	0	0	1	0	0	1	1	0	1
1	1	1	0	0	0	1	1	0	1	1	0	1	0	1	1
0	0	0	1	0	1	0	1	1	0	1	1	0	0	0	1
1	0	0	1	1	1	0	0	0	1	0	0	1	1	0	1
0	1	0	1	1	1	0	0	0	1	0	0	1	1	0	1
1	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1
0	0	1	1	0	0	1	1	0	1	0	1	0	0	1	1
1	0	1	1	1	0	1	0	1	1	1	1	0	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	0	1	1	1
1	1	1	1	0	1	1	1	1	1	0	1	1	0	0	1

Input conditions at A1, A2, B1, B2, and C_{in} are used to determine outputs S1 and S2, and the value of the internal carry, C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs S3, S4, and C_{out}.

LOGIC DIAGRAMS (continued)

COUNTERS

MC5490/MC7490
Decade Counter



RESET/COUNT TRUTH TABLE

R0		R9		OUTPUT			
Pin 2	Pin 3	Pin 6	Pin 7	Q3	Q2	Q1	Q0
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

X = Don't care.

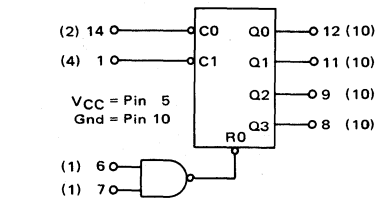
t_{pd} = 20 ns typ/bit
P_D = 160 mW typ/pkg

COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Q0 connected to $\overline{C1}$

MC5492/MC7492
Divide-by-Twelve Counter

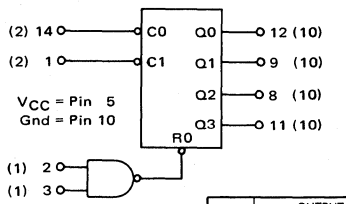


COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

Q0 connected to $\overline{C1}$

t_{pd} = 60 ns typ
P_D = 160 mW typ/pkg

MC5493/MC7493
4-Bit Binary Counter



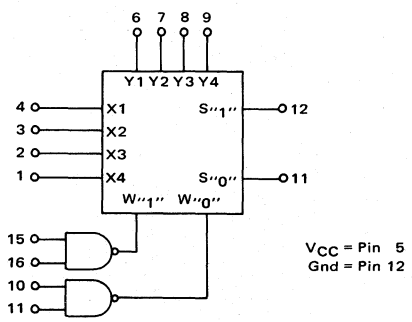
COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Q0 connected to $\overline{C1}$

t_{pd} = 20 ns typ/bit
P_D = 160 mW typ/pkg

MEMORIES

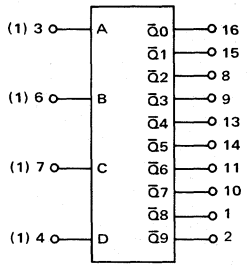
MC5484/MC7484
16-Bit Scratch Pad Memory Cell With Gated Inputs



t_{pd}: Write Mode = 25 ns typ
Read Mode = 15 ns typ
P_D = 250 mW typ/pkg

DECODERS

MC7441A
BCD-to-Decimal Decoder and High-Level Driver

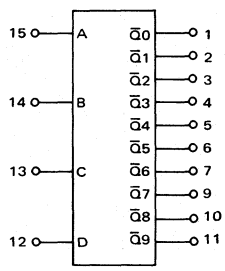


V_{CC} = Pin 5
Gnd = Pin 12

INPUT				OUTPUT									
D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1	1	1

P_D = 105 mW typ/pkg

MC5445/MC7445
MC54145/MC74145
BCD to 1-of-10 Decoder/Driver



V_{CC} = Pin 16
Gnd = Pin 8

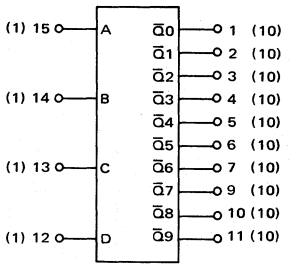
INPUT				OUTPUT									
D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

t_{pd} = 50 ns max
P_D = 215 mW typ/pkg

MC5442/MC7442
BCD-to-Decimal Decoder

MC5443/MC7443
Excess Three-to-Decimal Decoder

MC5444/MC7444
Excess Three Gray-to-Decimal Decoder

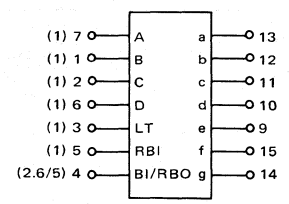


V_{CC} = Pin 16
Gnd = Pin 8

t_{pd}, 2 Logic Levels = 22 ns typ
3 Logic Levels = 23 ns typ
P_D = 140 mW typ/pkg

MC5442/MC7442 BCD INPUT				MC5443/MC7443 EXCESS 3 INPUT				MC5444/MC7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	0	1	1	1	0	1	1	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	1
0	1	1	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1	0	1	1
0	1	1	1	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	0	0	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

MC5446/MC7446
MC5447/MC7447
MC5448/MC7448
BCD-to-Seven Segment Decoder/Drivers



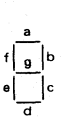
V_{CC} = Pin 16
Gnd = Pin 8

P_D = 265 mW typ/pkg

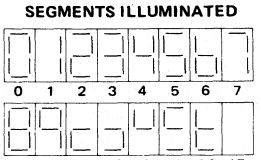
DIGIT OR FUNCTION	ALL TYPES							MC5446/MC7446 MC5447/MC7447 OUTPUT							MC5448/MC7448 OUTPUT						
	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	a	b	c	d	e	f	g
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0
1	1	X	0	0	0	1	1	1	0	0	1	1	1	1	0	1	1	0	0	0	0
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0	1	1	0	1	1	0	1
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0	1	1	1	1	0	0	1
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0	1	0	1	1	0	1	1
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0	1	1	1	0	0	1	1
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0	0	0	0	1	1	0	1
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1	0	0	1
12	1	X	1	1	0	0	1	1	0	1	1	1	0	0	0	1	0	0	0	1	1
13	1	X	1	1	0	1	1	0	1	1	0	1	0	0	1	0	0	0	1	0	1
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
BI	X	X	X	X	X	X	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0
LT	0	X	X	X	X	X	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1

X = Don't care

SEGMENT IDENTIFICATION



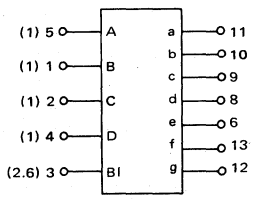
SEGMENTS ILLUMINATED



(continued)

DECODERS (continued)

MC5449/MC7449
BCD-to-Seven Segment Decoder/Driver



V_{CC} = Pin 16
Gnd = Pin 8

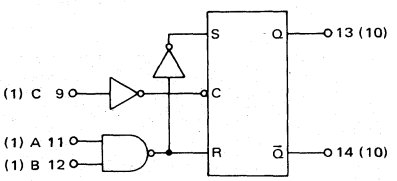
DIGIT OR FUNCTION	INPUT D	C	B	A	BI	OUTPUT a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	1	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	1	0	0	1
4	0	1	0	0	1	0	1	1	0	0	1	1
5	0	1	0	1	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	0	1	1
10	1	0	1	0	1	0	0	0	1	1	0	1
11	1	0	1	1	1	0	0	1	1	0	0	1
12	1	1	0	0	1	0	1	0	0	0	1	1
13	1	1	0	1	1	1	0	0	1	0	1	1
14	1	1	1	0	1	0	0	0	1	1	1	1
15	1	1	1	1	1	0	0	0	0	0	0	0
BI	X	X	X	X	0	0	0	0	0	0	0	0

X = Don't care

P_D = 165 mW typ/pkg

SHIFT REGISTERS

MC5491A/MC7491A
8-Bit Shift Register



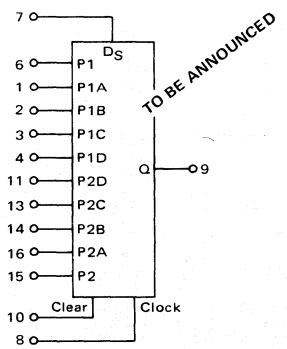
V_{CC} = Pin 5
Gnd = Pin 10

TRUTH TABLE
Synchronous Inputs

t_n		t_{n+8}	
A	B	Q	$\overline{Q}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

t_{pd} = 25 ns typ
P_D = 175 mW typ/pkg
f = 18 MHz typ

MC5494/MC7494
4-Bit Shift Register



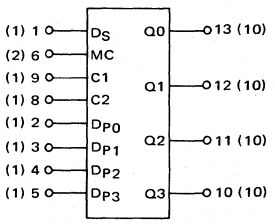
V_{CC} = Pin 5
Gnd = Pin 12

t_{pd}, Clock to Q = 25 ns typ
P_D = 175 mW typ/pkg
f_{Tog} = 10 MHz

(continued)

SHIFT REGISTERS (continued)

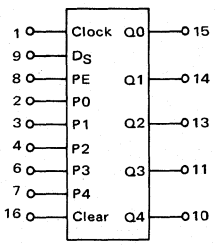
MC5495/MC7495
4-Bit Shift Register



V_{CC} = Pin 14
Gnd = Pin 7

t_{pd} = 25 ns typ
P_D = 250 mW typ/pkg
f = 31 MHz typ

MC5496/MC7496
5-Bit Shift Register

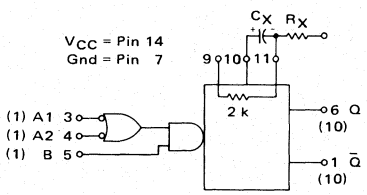


V_{CC} = Pin 5
Gnd = Pin 12

t_{pd}, Clock to Q4 = 25 ns typ
P_D = 240 mW typ/pkg
f_{Tog} = 10 MHz

MULTIVIBRATORS

MC54121/MC74121
Monostable Multivibrator



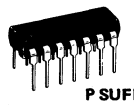
t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	Triggering
X	0	0	X	0	1	Triggering
1	1	1	X	0	1	Triggering
1	1	1	0	X	1	Triggering
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

X = Don't care
t_n = Time period prior to input transition
t_{n+1} = Time period following input transition

t_{pd}, B to Q = 35 ns typ
P_D = 90 mW typ/pkg (50% duty cycle)

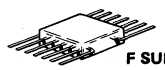
MC3000 Series (0 to +75°C)
MC3100 Series (-55 to +125°C)

MTTL III integrated circuits comprise a family of transistor-transistor logic designed for general purpose digital applications. The family has a high operating speed (30-50 MHz clock rate), good external noise immunity, high fan-out, and the capability of driving lines up to 600 pF capacitance.



P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Function	Type ① Case 605, 607, 632 0 to +75°C	Type ① Case 607, 632 -55°C to +125°C	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg
Quad 2-Input NAND Gate	MC3000	MC3100	10	6.0	88
Quad 2-Input AND Gate	MC3001	MC3101	10	9.0	112
Quad 2-Input NOR Gate	MC3002	MC3102	10	6.0	122
Quad 2-Input OR Gate	MC3003	MC3103	10	9.0	150
Quad 2-Input NAND Gate (Open Collector)	MC3004	MC3104	10	8.0	88
Triple 3-Input NAND Gate	MC3005	MC3105	10	6.0	66
Triple 3-Input AND Gate	MC3006	MC3106	10	9.0	84
Triple 3-Input NAND Gate (Open Collector)	MC3007	MC3107	10	8.0	66
Hex Inverter	MC3008	MC3108	10	6.0	140
Hex Inverter	MC3009	MC3109	10	8.0	90
Dual 4-Input NAND Gate	MC3010	MC3110	10	6.0	44
Dual 4-Input AND Gate	MC3011	MC3111	10	9.0	56
Dual 4-Input NAND Gate (Open Collector)	MC3012	MC3112	10	8.0	44
8-Input NAND Gate	MC3015	MC3115	10	8.0	22
8-Input NAND Gate	MC3016	MC3116	10	8.0	22
4-Wide 3-2-2-3 Input Expander For AND-OR-INVERT Gates	MC3018	MC3118	**	Δt_{pd1} = 0.4 Δt_{pd0} = 0.05	40
Triple 3-Input Expander For AND-OR Gates	MC3019	MC3119	**	Δt_{pd1} = 0.4 Δt_{pd0} = 0.05	25
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC3020	MC3120	10	6.0	62.5
Quad 2-Input Exclusive OR Gate	MC3021	MC3121	8	14	100
Quad 2-Input Exclusive NOR Gate	MC3022	MC3122	8	14	85
Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC3023	MC3123	10	6.0	62.5
Dual 4-Input NAND Buffer Gate	MC3024	MC3124	30	6.0	90
Dual 4-Input NAND Power Gate	MC3025	MC3125	20	6.0	70
Dual 4-Input AND Power Gate	MC3026	MC3126	20	9.0	90
Dual 3-Input 3-Output AND Series Terminated Line Driver	MC3028	MC3128	*	9.0	56
Dual 3-Input 3-Output NAND Series Terminated Line Driver	MC3029	MC3129	*	6.0	44
Dual 4-Input Expander for AND-OR-INVERT Gates	MC3030	MC3130	**	Δt_{pd} = 1.0	15
Expandable 4-Wide 2-2-2-3 Input AND-OR Gate	MC3031	MC3131	10	10	87.5
Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	MC3032	MC3132	10	7.0	40
4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	MC3033	MC3133	10	7.0	40
Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC3034	MC3134	10	7.0	30
AND J-K Flip-Flop	MC3050	MC3150	10	f = 40 MHz	80
AND Input J-K Flip-Flop	MC3051	MC3151	10	f = 50 MHz	50
AND Input $J\overline{J}$-$K\overline{K}$ Flip-Flop	MC3052	MC3152	10	f = 40 MHz	75
Double-Edge-Triggered Master-Slave Type D Flip-Flop	MC3053	MC3153	10	–	100
OR Input J-K Flip-Flop	MC3054	MC3154	10	f = 30 MHz	95
AND Input J-K Flip-Flop	MC3055	MC3155	10	f = 30 MHz	80
Dual Type D Flip-Flop	MC3060	MC3160	10	f = 30 MHz	120
Dual J-K Flip-Flop	MC3061	MC3161	10	f = 50 MHz	100
Dual J-K Flip-Flop	MC3062	MC3162	10	f = 50 MHz	100
• Dual J-K Flip-Flop	MC3063	MC3163	10	f = 30 MHz	176

① F suffix denotes Flat Package, L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Plastic Package, (i.e., MC3000F = Flat Package, MC3000L = Ceramic Package, MC3000P = Plastic Package).
*Direct Output = 10 minus the number of resistor-terminated outputs being used.
**Full output loading factor of the expandable gate is maintained.
• New Devices

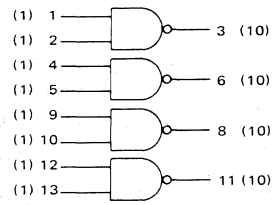
MTTL III LOGIC DIAGRAMS

Numbers at ends of terminals represent pin numbers.
Numbers in parenthesis indicate loading.

V_{CC} = Pin 14, Gnd = Pin 7.

GATES

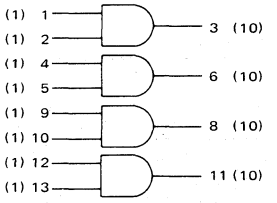
MC3000/MC3100
Quad 2-Input NAND Gate



$3 = \overline{1 \bullet 2}$

t_{pd} = 6.0 ns typ
P_D = 88 mW typ/pkg

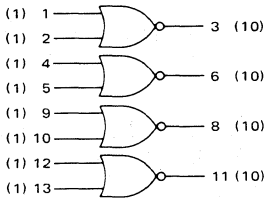
MC3001/MC3101
Quad 2-Input AND Gate



$3 = 1 \bullet 2$

t_{pd} = 9.0 ns typ
P_D = 112 mW typ/pkg

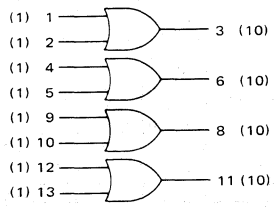
MC3002/MC3102
Quad 2-Input NOR Gate



$3 = \overline{1 + 2}$

t_{pd} = 6.0 ns typ
P_D = 122 mW typ/pkg

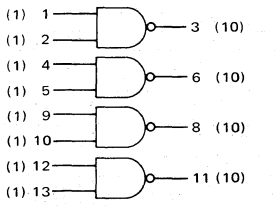
MC3003/MC3103
Quad 2-Input OR Gate



$3 = 1 + 2$

t_{pd} = 9.0 ns typ
P_D = 150 mW typ/pkg

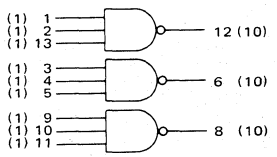
MC3004/MC3104
Quad 2-Input NAND Gate
(Open Collector)



$3 = \overline{1 \bullet 2}$

t_{pd} = 8.0 ns typ
P_D = 88 mW typ/pkg

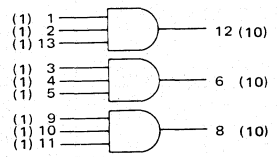
MC3005/MC3105
Triple 3-Input NAND Gate



$12 = \overline{1 \bullet 2 \bullet 13}$

t_{pd} = 6.0 ns typ
P_D = 66 mW typ/pkg

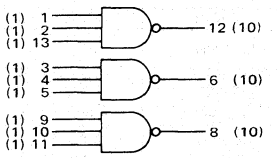
MC3006/MC3106
Triple 3-Input AND Gate



$12 = 1 \bullet 2 \bullet 13$

t_{pd} = 9.0 ns typ
P_D = 84 mW typ/pkg

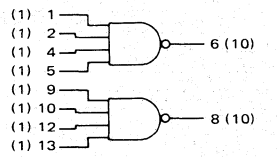
MC3007/MC3107
Triple 3-Input NAND Gate
(Open Collector)



$12 = \overline{1 \bullet 2 \bullet 13}$

t_{pd} = 8.0 ns typ
P_D = 66 mW typ/pkg

MC3010/MC3110
Dual 4-Input NAND Gate



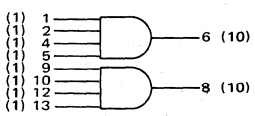
$6 = \overline{1 \bullet 2 \bullet 4 \bullet 5}$

t_{pd} = 6.0 ns typ
P_D = 44 mW typ/pkg

(continued)

GATES (continued)

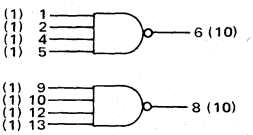
MC3011/MC3111
Dual 4-Input AND Gate



$6 = 1 \bullet 2 \bullet 4 \bullet 5$

t_{pd} = 9.0 ns typ
P_D = 56 mW typ/pkg

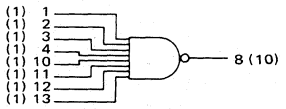
MC3012/MC3112
Quad 4-Input NAND Gate
(Open Collector)



$6 = \overline{1 \bullet 2 \bullet 4 \bullet 5}$

t_{pd} = 8.0 ns typ
P_D = 44 mW typ/pkg

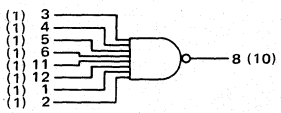
MC3015/MC3115
8-Input NAND Gate



$8 = \overline{1 \bullet 2 \bullet 3 \bullet 4 \bullet 10 \bullet 11 \bullet 12 \bullet 13}$

t_{pd} = 8.0 ns typ
P_D = 22 mW typ/pkg

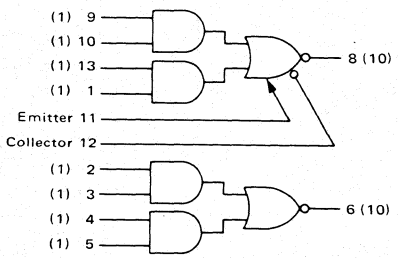
MC3016/MC3116
8-Input NAND Gate



$8 = \overline{3 \bullet 4 \bullet 5 \bullet 6 \bullet 11 \bullet 12 \bullet 1 \bullet 2}$

t_{pd} = 8.0 ns typ
P_D = 22 mW typ/pkg

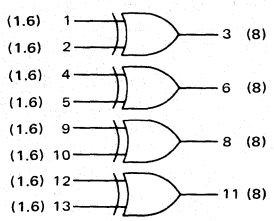
MC3020/MC3120
Expandable Dual 2-Wide 2-Input
AND-OR-INVERT Gate



$8 = \overline{(9 \bullet 10) + (13 \bullet 1) + (\text{Expanders})}$

t_{pd} = 6.0 ns typ
P_D = 62.5 mW typ/pkg

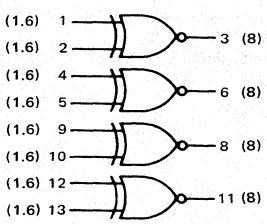
MC3021/MC3121
Quad 2-Input
Exclusive OR Gate



$3 = 1 \bullet \overline{2} + \overline{1} \bullet 2$

t_{pd} = 14 ns typ
P_D = 100 mW typ/pkg

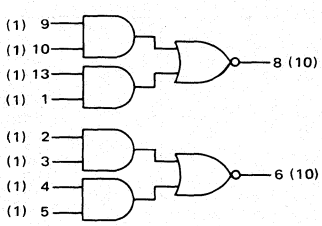
MC3022/MC3122
Quad 2-Input
Exclusive NOR Gate



$3 = \overline{1} \bullet \overline{2} + 1 \bullet 2$

t_{pd} = 14 ns typ
P_D = 85 mW typ/pkg

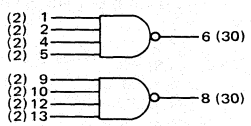
MC3023/MC3123
Dual 2-Wide 2-Input
AND-OR-INVERT GATE



$8 = \overline{(9 \bullet 10) + (13 \bullet 1)}$

t_{pd} = 6.0 ns typ
P_D = 62.5 mW typ/pkg

MC3024/MC3124
Dual 4-Input NAND
Buffer Gate



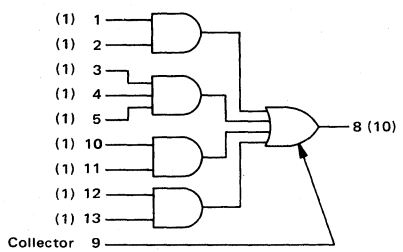
$6 = \overline{1 \bullet 2 \bullet 4 \bullet 5}$

typ = 6.0 ns typ
P_D = 90 mW typ/pkg

(continued)

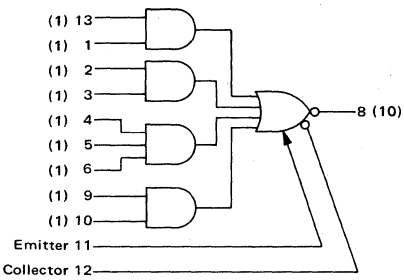
GATES (continued)

MC3031/MC3131
Expandable 4-Wide 2-2-2-3-Input AND-OR Gate



t_{pd} = 10 ns typ
P_D = 87.5 mW typ/pkg

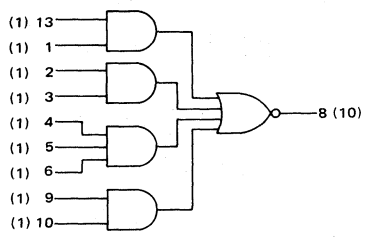
MC3032/MC3132
Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate



$8 = \overline{(13 \cdot 1) + (2 \cdot 3) + (4 \cdot 5 \cdot 6) + (9 \cdot 10) + (\text{Expanders})}$

t_{pd} = 7 ns typ
P_D = 40 mW typ/pkg

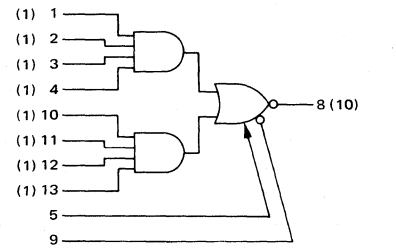
MC3033/MC3133
4-Wide 2-2-2-3-Input AND-OR-INVERT Gate



$8 = \overline{(13 \cdot 1) + (2 \cdot 3) + (4 \cdot 5 \cdot 6) + (9 \cdot 10)}$

t_{pd} = 7 ns typ
P_D = 40 mW typ/pkg

MC3034/MC3134
Expandable 2-Wide 4-Input AND-OR-INVERT Gate

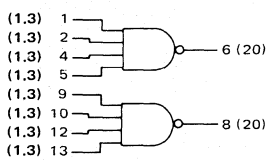


$8 = \overline{(1 \cdot 2 \cdot 3 \cdot 4) + (10 \cdot 11 \cdot 12 \cdot 13) + (\text{Expanders})}$

t_{pd} = 7.0 ns typ
P_D = 30 mW typ/pkg

POWER GATES

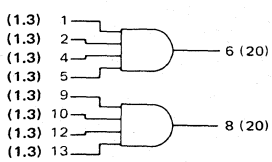
MC3025/MC3125
Dual 4-Input NAND Power Gate



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

t_{pd} = 6.0 ns typ
P_D = 70 mW typ/pkg

MC3026/MC3126
Dual 4-Input AND Power Gate

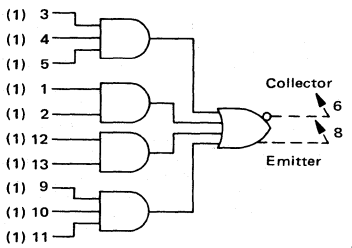


$6 = 1 \cdot 2 \cdot 4 \cdot 5$

t_{pd} = 9.0 ns typ
P_D = 90 mW typ/pkg

EXPANDERS

MC3018/MC3118
3-2-2-3 Input Expander For AND-OR-INVERT Gate



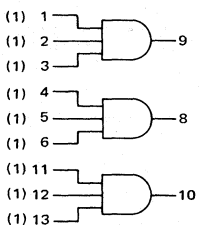
Full output loading factor of the expandable gate is maintained.

Propagation Delay Time:
Δt_{pd1} = +0.4 ns typ
Δt_{pd0} = 0.05 ns typ
When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd1/pF}$ = +0.3 ns/pF typ
$\Delta t_{pd0/pF}$ = +0.04 ns/pF typ
Caused by additional capacitance at expansion points.

P_D = 40 mW typ/pkg

MC3019/MC3119
Triple 3-Input Expander For AND-OR Gates



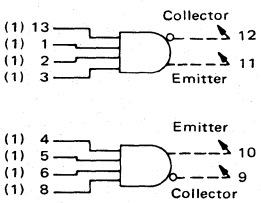
Full output loading factor of the expandable gate is maintained.

Propagation Delay Time:
Δt_{pd1} = +0.4 ns typ
Δt_{pd0} = +0.05 ns typ
When added to the expandable "AND-OR" gate.

$\Delta t_{pd1/pF}$ = +0.3 ns/pF typ
$\Delta t_{pd0/pF}$ = +0.04 ns/pF typ
Caused by additional capacitance at expansion points.

P_D = 25 mW typ/pkg

MC3030/MC3130
Dual 4-Input Expander for AND-OR-INVERT Gates



Full output loading factor of the expandable gate is maintained.

Δt_{pd} = +1.0 ns typ
When added to the expandable "AND-OR-INVERT" gate.

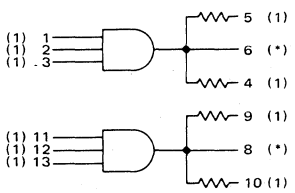
$\Delta t_{pd/pF}$ = +1.0 ns/pF typ
Caused by additional capacitance at expansion points.

P_D = 15 mW typ/pkg

LOGIC DIAGRAMS (continued)

LINE DRIVERS

MC3028/MC3128
Dual 3-Input 3-Output AND
Series Terminated Line Driver

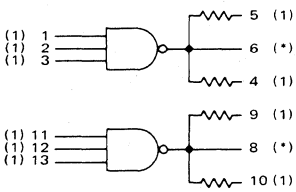


4, 5, 6, = 1 • 2 • 3

t_{pd} = 9.0 ns typ
P_D = 56 mW typ/pkg

*8 MINUS THE NUMBER OF RESISTOR-TERMINATED OUTPUTS BEING USED.

MC3029/MC3129
Dual 3-Input 3-Output NAND
Series Terminated Line Driver



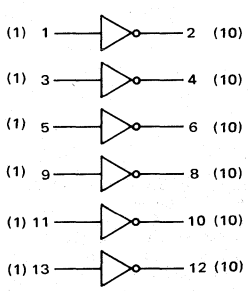
4, 5, 6 = $\overline{1 \cdot 2 \cdot 3}$

t_{pd} = 6.0 ns typ
P_D = 44 mW typ/pkg

*8 MINUS THE NUMBER OF RESISTOR-TERMINATED OUTPUTS BEING USED.

INVERTERS

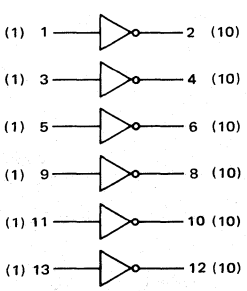
MC3008/MC3108
Hex Inverter



2 = $\overline{1}$

t_{pd} = 6.0 ns typ
P_D = 140 mW typ/pkg

MC3009/MC3109
Hex Inverter

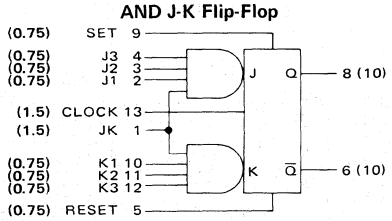


2 = $\overline{1}$

t_{pd} = 8.0 ns typ
P_D = 90 mW typ/pkg

FLIP-FLOPS

MC3050/MC3150
AND J-K Flip-Flop



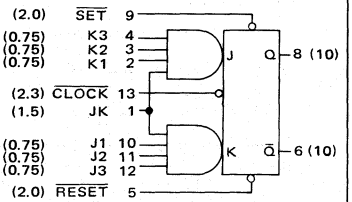
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where:
J = J1 • J2 • J3 • JK
K = K1 • K2 • K3 • JK

f = 40 MHz
P_D = 80 mW typ/pkg

MC3051/MC3151
AND J-K Flip-Flop

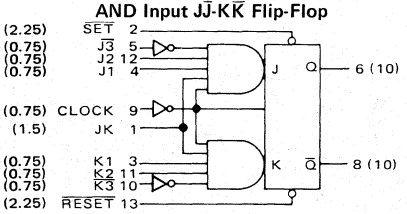
J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



where
J = J1 • J2 • J3 • JK
K = K1 • K2 • K3 • JK

f = 50 MHz
P_D = 50 mW typ/pkg

MC3052/MC3152
AND Input JJ̄-KK̄ Flip-Flop

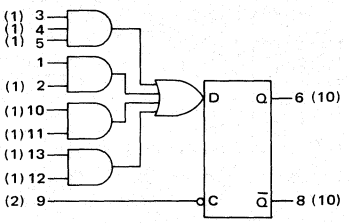


J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where:
J = J1 • J2 • $\overline{J3}$ • JK
K = K1 • K2 • $\overline{K3}$ • JK

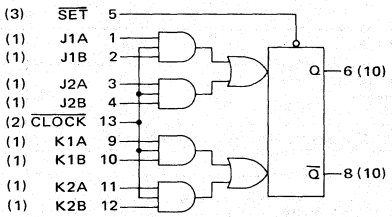
f = 40 MHz
P_D = 75 mW typ/pkg

MC3053/MC3153
Double-Edge-Triggered Master-Slave Type D Flip-Flop



P_D = 100 mW typ/pkg

MC3054/MC3154
OR Input J-K Flip-Flop

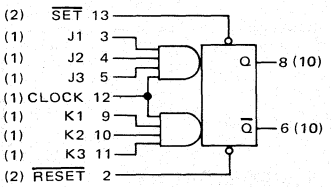


t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

J = J1A • J1B + J2A • J2B
K = K1A • K1B + K2A • K2B

t_{pd} = 20 ns typ
f = 30 MHz typ
P_D = 95 mW typ/pkg

MC3055/MC3155
AND Input J-K Flip-Flop



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

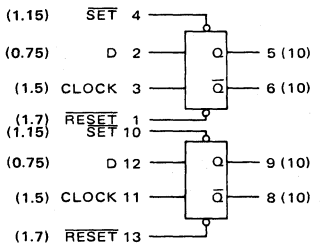
J = J1 • J2 • J3
K = K1 • K2 • K3

t_{pd} = 10 ns typ
f = 30 MHz typ
P_D = 80 mW typ/pkg

LOGIC DIAGRAMS (continued)

FLIP-FLOPS (continued)

MC3060/MC3160
Dual Type D Flip-Flop

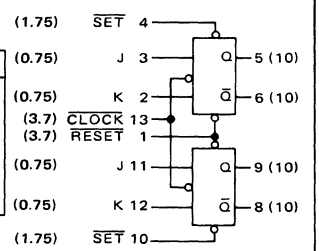


D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$Q_{n+1} = D_n$

f = 30 MHz
P_D = 120 mW typ/pkg

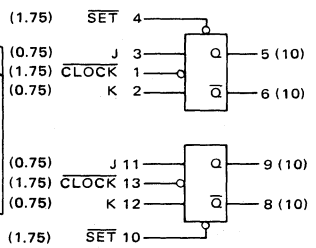
MC3061/MC3161
Dual J-K Flip-Flop



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

f = 50 MHz
P_D = 100 mW typ/pkg

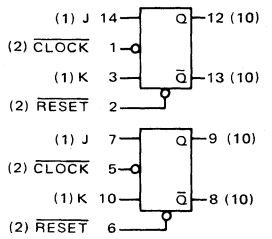
MC3062/MC3162
Dual J-K Flip-Flop



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

f = 50 MHz
P_D = 100 mW typ/pkg

MC3063/MC3163
DUAL J-K FLIP-FLOP



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

P_D = 176 mW typ/pkg
t_{pd} = 10 ns typ
f = 30 MHz typ

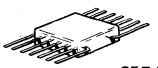
MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage — Continuous MC3100 series MC3000 series	 +7.0 +7.0	 Vdc Vdc
Supply Operating Voltage Range	4.5 to 5.5	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range MC3100 series MC3000 series	 -55 to +125 0 to +75	 °C °C
Storage Temperature Range — Ceramic Package Plastic Package	 -65 to +175 -55 to +125	 °C °C

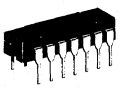
MTTL II INTEGRATED CIRCUITS MTTL II

MC2000 Series (0 to +75°C)
MC2100 Series (–55 to +125°C)

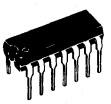
MTTL II integrated circuits comprise a family of transistor-transistor logic designed for general purpose digital applications. The family has a high operating speed (30-50 MHz clock rate), good external noise immunity, high fan out, and the capability of driving capacitive loads to 600 pF.



F SUFFIX
CERAMIC FLAT PACKAGE
CASE 607



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116

MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage-Continuous – MC2100 Series MC2000 Series	+8.0 +7.0	Vdc
Supply Operating Voltage Range	4.5 to 6.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range – MC2100 Series MC2000 Series	–55 to +125 0 to +75	°C
Storage Temperature Range – Ceramic Package – Plastic Package	–65 to +150 –55 to +125	°C
Maximum Junction Temperature – MC2100 Series MC2000 Series	+175 +150	°C
Thermal Resistance-Junction to Case (θ_{JC}) – Ceramic Package – Plastic Package	 0.09 0.15	°C/mW
Thermal Resistance-Junction to Ambient (θ_{JA}) – Ceramic Package – Plastic Package	 0.26 0.30	°C/mW

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Function	Type ① Case 605, 607, 632 0 to +75°C	Type ① Case 607, 632 –55 to +125°C	Output Loading Factor Each Output MC2000 Series	Output Loading Factor Each Output MC2100 Series	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg
Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC2000 MC2050	MC2100 MC2150	9 5	11 6	7.0	27
Quad 2-Input NAND Gate	MC2001 MC2051	MC2101 MC2151	9 5	11 6	6.0	88
4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates	MC2002 MC2052	MC2102 MC2152	9 5	11 6	–	28
Dual 4-Input NAND Gate	MC2003 MC2053	MC2103 MC2153	9 5	11 6	6.0	44
Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	MC2004 MC2054	MC2104 MC2154	9 5	11 6	7.0	36
8-Input NAND Gate	MC2005 MC2055	MC2105 MC2155	9 5	11 6	8.0	22
Dual 4-Input Expander for AND-OR-INVERT Gates	MC2006 MC2056	MC2106 MC2156	9 5	11 6	–	14
Triple 3-Input NAND Gate	MC2007 MC2057	MC2107 MC2157	9 5	11 6	6.0	66
Expandable 8-Input NAND Gate	MC2011 MC2061	MC2111 MC2161	9 9	11 6	11	22
Expandable 3-Wide 3-Input AND-OR-INVERT Gate	MC2012 MC2062	MC2112 MC2162	9 5	11 6	6.0	39
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC2013 MC2063	MC2113 MC2163	9 5	11 6	7.0	58
Quad 2-Input Lamp/ Line Driver	– MC2065	– MC2165	– –	– –	20	105
Hex Inverter	MC2016 MC2066	MC2116 MC2166	5 5	9 9	6.0	132
Dual J-K Flip-Flop (separate clock)	MC2023 MC2073	MC2123 MC2173	9 5	11 6	f = 70 MHz	110
Dual J-K Flip-Flop (common clock)	MC2024 MC2074	MC2124 MC2174	9 5	11 6	f = 70 MHz	110
AND J-K Flip-Flop	MC2025 MC2075	MC2125 MC2175	9 5	11 6	f = 50 MHz	50
OR J-K Flip-Flop	MC2026 MC2076	MC2126 MC2176	9 5	11 6	f = 50 MHz	60
OR J-K Flip-Flop	MC2028 MC2078	MC2128 MC2178	9 5	11 6	f = 35 MHz	60

① F suffix denotes Flat Package, L denotes Dual In-Line Ceramic Package, P denotes Plastic Package, (i.e., MC2000F = Flat Package, MC2100L = Dual In-Line Ceramic, MC2000P = Plastic Package.)

Individual data sheets for this series of TTL devices are available. To obtain copies, send your request to: Technical Information Center, Motorola Semiconductor Products, Inc., P.O. Box 20924, Phoenix, Arizona 85036.

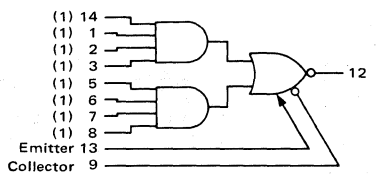
MTTL II LOGIC DIAGRAMS

Numbers at ends of terminals represent pin numbers.
Numbers in parenthesis indicate input loading factor.
For output loading capability, see Functions and Characteristics table.

V_{CC} = Pin 4, Gnd = Pin 10.

GATES

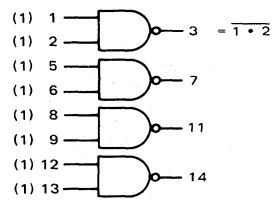
MC2000/MC2050 MC2100/MC2150 Expandable 2-Wide 4-Input AND-OR-INVERT Gate



$12 = \overline{(14 \cdot 1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7 \cdot 8) + (\text{Expander})}$

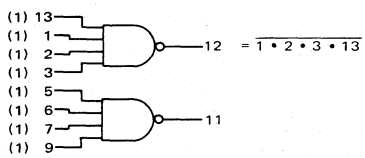
t_{pd} = 7.0 ns typ
P_D = 27 mW typ/pkg

MC2001/MC2051 MC2101/MC2151 Quad 2-Input NAND Gate



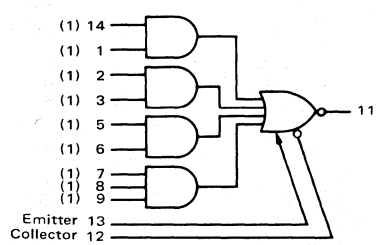
t_{pd} = 6.0 ns typ
P_D = 88 mW typ/pkg

MC2003/MC2053 MC2103/MC2153 Dual 4-Input NAND Gate



t_{pd} = 6.0 ns typ
P_D = 44 mW typ/pkg

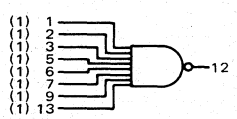
MC2004/MC2054 MC2104/MC2154 Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate



$11 = \overline{(14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9) + (\text{Expander})}$

t_{pd} = 7.0 ns typ
P_D = 36 mW typ/pkg

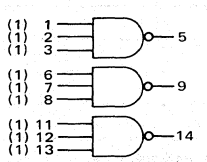
MC2005/MC2055 MC2105/MC2155 8-Input NAND Gate



$12 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 13}$

t_{pd} = 8.0 ns typ
P_D = 22 mW typ/pkg

MC2007/MC2057 MC2107/MC2157 Triple 3-Input NAND Gate



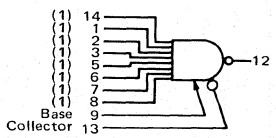
$5 = \overline{1 \cdot 2 \cdot 3}$

t_{pd} = 6.0 ns typ
P_D = 66 mW typ/pkg

LOGIC DIAGRAMS (continued)

GATES (continued)

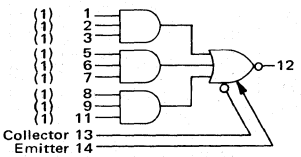
MC2011/MC2061
MC2111/MC2161
Expandable 8-Input NAND Gate



$12 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 8 \cdot 14 \cdot Exp}$

t_{pd} = 11 ns typ
P_D = 22 mW typ/pkg

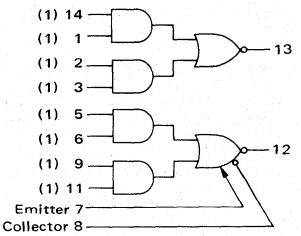
MC2012/MC2062
MC2112/MC2162
Expandable 3-Wide 3-Input AND-OR-INVERT Gate



$12 = \overline{(1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7) + (8 \cdot 9 \cdot 11) + Exp}$

t_{pd} = 6.0 ns typ
P_D = 39 mW typ/pkg

MC2013/MC2063
MC2113/MC2163
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate

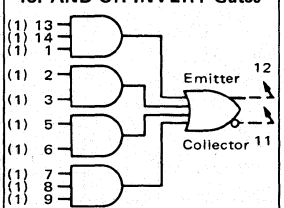


$13 = \overline{(1 \cdot 14) + (2 \cdot 3)}$
$12 = \overline{(5 \cdot 6) + (9 \cdot 11) + (Expander)}$

t_{pd} = 7.0 ns typ
P_D = 58 mW typ/pkg

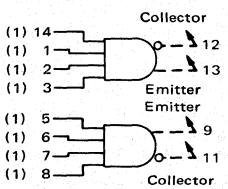
EXPANDERS

MC2002/MC2052
MC2102/MC2152
4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates



P_D = 28 mW typ/pkg

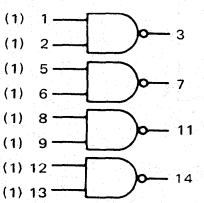
MC2006/MC2056
MC2106/MC2156
Dual 4-Input Expander for AND-OR-INVERT Gates



P_D = 14 mW typ/pkg

DRIVER

MC2165/MC2065
Quad 2-Input Lamp/Line Driver

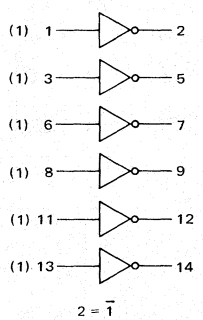


$3 = \overline{1 \cdot 2}$

t_{pd} = 20 ns typ
P_D = 105 mW typ/pkg

INVERTER

MC2016/MC2066
MC2116/MC2166
Hex Inverter



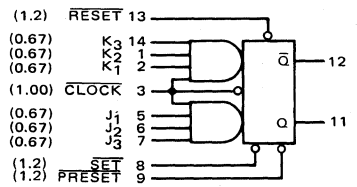
$2 = \overline{1}$

t_{pd} = 6.0 ns typ
P_D = 132 mW typ/pkg

5

FLIP-FLOPS

MC2025/MC2075, MC2125/MC2175 AND J-K Flip-Flop

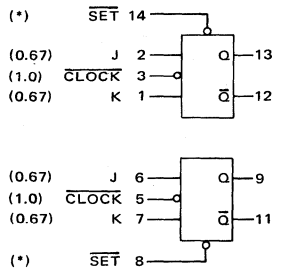


J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$

f = 50 MHz typ
P_D = 50 mW typ/pkg

MC2023/MC2073 MC2123/MC2173 Dual J-K Flip-Flop (Separate Clock)



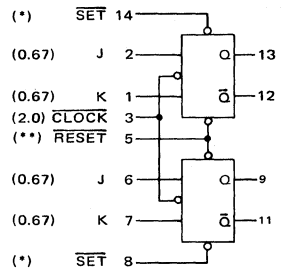
t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
0	1	0	1
1	0	1	0
1	1	$\bar{Q}_n$	Q_n

MC2000 Series
*1.15

MC2100 Series
*1.2

f = 70 MHz typ
P_D = 110 mW typ/pkg

MC2024/MC2074 MC2124/MC2174 Dual J-K Flip-Flop (Common Clock)



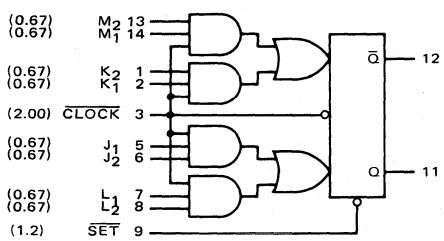
t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
0	1	0	1
1	0	1	0
1	1	$\bar{Q}_n$	Q_n

MC2000 Series
*1.15
**2.3

MC2100 Series
*1.2
**2.4

f = 70 MHz typ
P_D = 110 mW typ/pkg

MC2026/MC2076, MC2126/MC2176 OR J-K Flip-Flop



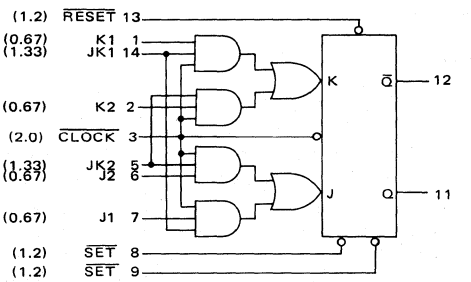
J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care

$J = J_1 \cdot J_2$
$L = L_1 \cdot L_2$
$K = K_1 \cdot K_2$
$M = M_1 \cdot M_2$

f = 50 MHz typ
P_D = 60 mW typ/pkg

MC2028/MC2078 MC2128/MC2178 OR J-K FLIP-FLOP



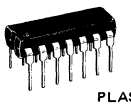
J1	J2	K1	K2	JK1	JK2	Q_{n+1}
X	X	X	X	0	0	Q_n
X	1	X	0	0	1	1
X	0	X	1	0	1	0
X	1	X	1	0	1	Q_n
1	X	0	X	1	0	1
0	X	1	X	1	0	0
1	X	1	X	1	0	Q_n
0	0	0	0	1	1	Q_n
X	1	0	0	1	1	1
1	X	0	0	1	1	1
0	0	X	1	1	1	0
0	0	1	X	1	1	0
1	X	1	X	1	1	Q_n
X	1	X	1	1	1	Q_n

X = Don't Care

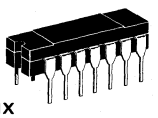
f = 35 MHz typ
P_D = 60 mW typ/pkg

MC400 Series (0 to +75°C)
MC500 Series (-55 to +125°C)

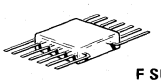
MTTL integrated circuits comprise a family of transistor-transistor logic designed for general purpose digital applications. The family has a medium operating speed (20 MHz clock rate), good external noise immunity, high fan out, and the capability of driving lines up to 600 pF capacitance.



P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



F SUFFIX
CERAMIC FLAT PACKAGE
CASE 607

MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage – Continuous MC500/550 Series MC400/450 Series	 +8.0 +7.0	Vdc
Supply Operating Voltage Range	4.5 to 6.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range MC500/550 Series MC400/450 Series	 -55 to +125 0 to +75	°C
Storage Temperature Range Ceramic Package Plastic Package	 -65 to +150 -55 to +125	°C
Maximum Junction Temperature MC500/550 Series MC400/450 Series	 +175 +150	°C
Thermal Resistance – Junction To Case (θ_{JC}) Ceramic Package Plastic Package	 0.09 0.15	°C/mW
Thermal Resistance – Junction To Ambient (θ_{JA}) Ceramic Package Plastic Package	 0.26 0.30	°C/mw

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Function	Type ① Case 605, 607, 632 0 to +75°C	Type ① Case 607, 632 -55 to +125°C	Output Loading Factor Each Output MC400 Series	Output Loading Factor Each Output MC500 Series	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg
Dual 4-Input NAND Gate	MC400 MC450	MC500 MC550	12 6	15 7	10	30
Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate	MC401 MC451	MC501 MC551	12 6	15 7	12	30
8-Input NAND Gate	MC402 MC452	MC502 MC552	12 6	15 7	12	15
2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement	MC403 MC453	MC503 MC553	12 6	15 7	11	35
Expandable 3-Wide 3-Input AND-OR-INVERT Gate	MC404 MC454	MC504 MC554	12 6	15 7	12	25
Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC405 MC455	MC505 MC555	12 6	15 7	12	20
Expandable 8-Input NAND Gate	MC406 MC456	MC506 MC556	12 6	15 7	18	15
Line Driver	MC407 MC457	MC507 MC557	12 6	15 7	25 @ 1000 pF Load	60
Quad 2-Input NAND Gate	MC408 MC458	MC508 MC558	12 6	15 7	10	60
4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates	MC409 MC459	MC509 MC559	12 6	15 7	–	–
Dual 4-Input Expander for AND-OR-INVERT Gates	MC410 MC460	MC510 MC560	12 6	15 7	–	–
Dual 4-Input Expander for NAND Gates	MC411 MC461	MC511 MC561	12 6	15 7	–	–

① F suffix denotes Flat Package, L suffix denotes dual in-line Ceramic Package, P suffix denotes dual in-line Plastic Package, (i.e., MC401F = Flat Package, MC401L = Ceramic Package, MC401P - Plastic Package.)

(continued)

Individual data sheets for this series of TTL devices are available. To obtain copies, send your request to: Technical Information Center, Motorola Semiconductor Products, Inc., P.O. Box 20924, Phoenix, Arizona 85036.

MTTL I LOGIC DIAGRAMS

FUNCTIONS AND CHARACTERISTICS (continued)

Function	Type ① Case 605, 607, 632 0 to +75°C	Type ① Case 607, 632 -55 to +125°C	Output Loading Factor Each Output MC400 Series	Output Loading Factor Each Output MC500 Series	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg
Triple 3-Input NAND Gate	MC412 MC462	MC512 MC562	12 6	15 7	10	45
R-S Flip-Flop	MC413 MC463	MC513 MC563	12 6	15 7	20/15*	30
Gated R-S Flip-Flop	MC414 MC464	MC514 MC564	12 6	15 7	20/7.5*	30
AND J-K Flip-Flop	MC415 MC465	MC515 MC565	12 6	15 7	13/25*	40
OR J-K Flip-Flop	MC416 MC466	MC516 MC566	12 6	15 7	13/25*	50
Triple 2-Input Buss Driver	MC419 MC469	MC519 MC569	– –	– –	50/15*	54
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC420 MC470	MC520 MC570	12 6	15 7	12	40
AC Coupled R-S Flip-Flop	MC421 MC471	MC521 MC571	12 6	15 7	18	30
Dual Type D Flip-Flop	MC422 MC472	MC522 MC572	12 6	15 7	16	84
Dual J-K Flip-Flop (separate clock)	MC423 MC473	MC523 MC573	13 7	16 8	10/12*	110
Dual J-K Flip-Flop (common clock)	MC424 MC474	MC524 MC574	13 7	16 8	10/12*	110
Dual 3-Input Pulse Shaper/Delay AND Gate	MC426 MC476	MC526 MC576	13 7	16 8	15	60
OR Expandable Dual 4-Input AND Gate	MC427 MC477	MC527 MC577	12 6	15 7	10	38
Dual 2-Wide 2-3 Input OR Expander	MC428 MC478	MC528 MC578	– –	– –	–	15
Hex Inverter	MC429 MC479	MC529 MC579	12 6	15 7	10	90

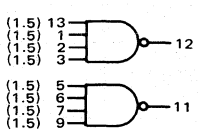
① F suffix denotes Flat Package, L suffix denotes dual in-line Ceramic Package, P suffix denotes dual in-line Plastic Package, (i.e., MC401F = Flat Package, MC401L = Ceramic Package, MC401P - Plastic Package.)

*t_{pd+}/t_{pd-}

6

DRIVERS

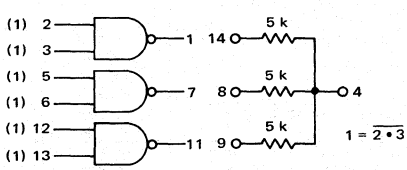
MC407/MC457
MC507/MC557
Dual 4-Input Line Driver



t_{pd} = 25 ns typ
@ 1000 pF Load
P_D = 60 mW typ/pkg

$12 = \overline{1 \cdot 2 \cdot 3 \cdot 13}$

MC419/MC469
MC519/MC569
Triple 2-Input Buss Driver



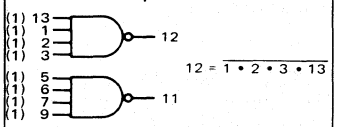
Propagation Delay Time (using 5.0 k ohm pullup resistor):
t_{pd+} = 50 ns typ
t_{pd-} = 15 ns typ
P_D = 54 mW typ/pkg

LOGIC DIAGRAMS (continued)

Numbers at ends of terminals represent pin numbers.
Numbers in parenthesis indicate input loading factor.
For output loading capability, see Functions and Characteristics Table. V_{CC} = Pin 4, Gnd = Pin 10.

GATES

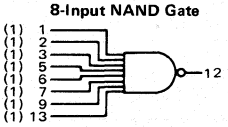
MC400/MC450 MC500/MC550
Dual 4-Input NAND Gate



$12 = \overline{1 \cdot 2 \cdot 3 \cdot 13}$

t_{pd} = 10 ns typ
P_D = 30 mW typ/pkg

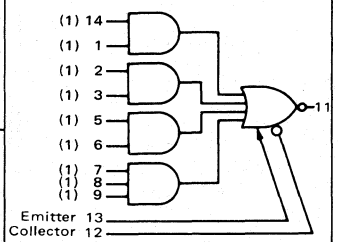
MC402/MC452 MC502/MC552
8-Input NAND Gate



$12 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 13}$

t_{pd} = 12 ns typ
P_D = 15 mW typ/pkg

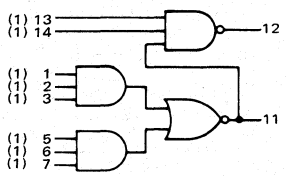
MC401/MC451 MC501/MC551
Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate



$11 = \overline{(14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9) + \ldots}$

t_{pd} = 12 ns typ
P_D = 30 mW typ/pkg

MC403/MC453 MC503/MC553
2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement

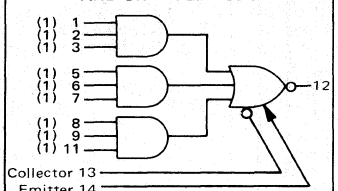


$12 = \overline{11 \cdot 13 \cdot 14}$

$11 = \overline{(1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7)}$

t_{pd} = 11 ns typ
P_D = 35 mW typ/pkg

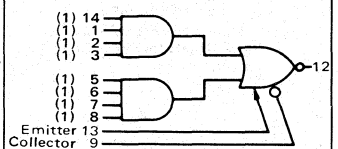
MC404/MC454 MC504/MC554
Expandable 3-Wide 3-Input AND-OR-INVERT Gate



$12 = \overline{(1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7) + (8 \cdot 9 \cdot 11) + \ldots}$

t_{pd} = 12 ns typ
P_D = 25 mW typ/pkg

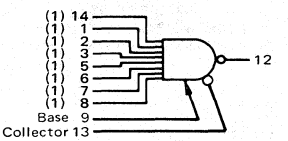
MC405/MC455 MC505/MC555
Expandable 2-Wide 4-Input AND-OR-INVERT Gate



$12 = \overline{(14 \cdot 1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7 \cdot 8) + \ldots}$

t_{pd} = 12 ns typ
P_D = 20 mW typ/pkg

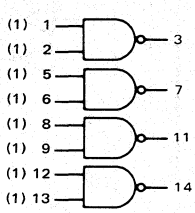
MC406/MC456 MC506/MC556
Expandable 8-Input NAND Gate



$12 = \overline{1 \cdot 3 \cdot 5 \cdot 7 \cdot 8 \cdot 14 \cdot \ldots}$

t_{pd} = 18 ns typ
P_D = 15 mW typ/pkg

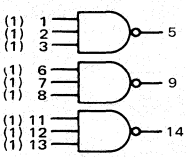
MC408/MC458 MC508/MC558
Quad 2-Input NAND Gate



$3 = \overline{1 \cdot 2}$

t_{pd} = 10 ns typ
P_D = 60 mW typ/pkg

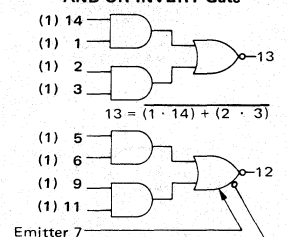
MC412/MC462 MC512/MC562
Triple 3-Input NAND Gate



$5 = \overline{1 \cdot 2 \cdot 3}$

t_{pd} = 10 ns typ
P_D = 45 mW typ/pkg

MC420/MC470 MC520/MC570
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate



$13 = \overline{(1 \cdot 14) + (2 \cdot 3)}$

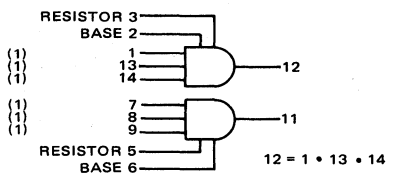
$12 = \overline{(5 \cdot 6) + (9 \cdot 11) + \ldots}$

t_{pd} = 12 ns typ
P_D = 40 mW typ/pkg

(continued)

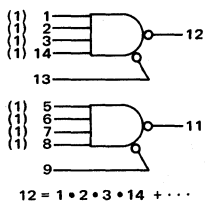
GATES (continued)

MC426/MC476
MC526/MC576
Dual 3-Input
Pulse Shaper/Delay AND Gate



t_{pd} = 15 ns typ
P_D = 60 mW typ/pkg

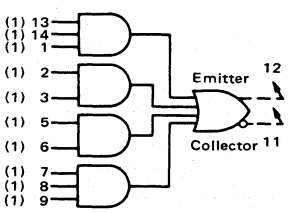
MC427/MC477
MC527/MC577
OR Expandable Dual
4-Input AND Gate



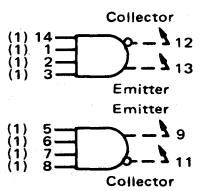
t_{pd} = 10 ns typ
P_D = 38 mW typ/pkg

EXPANDERS

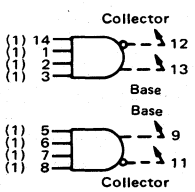
MC409/MC459
MC509/MC559
4-Wide 3-2-2-3 Input Expander
for AND-OR-INVERT Gates



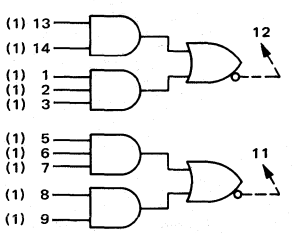
MC410/MC460
MC510/MC560
Dual 4-Input Expander
for AND-OR-INVERT Gates



MC411/MC461
MC511/MC561
Dual 4-Input Expander
for NAND Gates

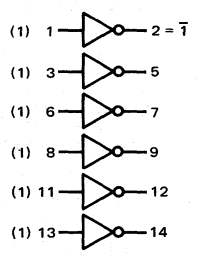


MC428/MC478
MC528/MC578
Dual 2-Wide 2-3 Input
OR Expander



INVERTER

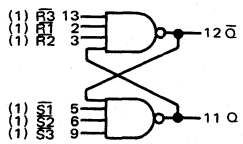
MC429/MC479
MC529/MC579
Hex Inverter



t_{pd} = 10 ns typ
P_D = 90 mW typ/pkg

FLIP-FLOPS

MC413/MC463 MC513/MC563 R-S Flip-Flop

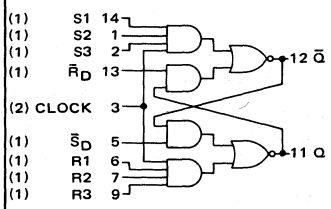


R̄	S̄	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	Not allowed	
0	1	0	1
1	0	1	0
1	1	Q_n	$\bar{Q}_n$

Where $\bar{R} = \bar{R1} \cdot \bar{R2} \cdot \bar{R3}$
$\bar{S} = \bar{S1} \cdot \bar{S2} \cdot \bar{S3}$

t+ = 15 ns typ
t– = 20 ns typ
P_D = 30 mW typ/pkg

MC414/MC464 MC514/MC564 Gated R-S Flip-Flop

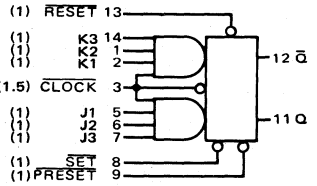


R_C	S_C	Q^{n+1}
0	0	Q^n
0	1	1
1	0	0
1	1	Indeterminate

Where $R_C = 6 \cdot 7 \cdot 9$
$S_C = 1 \cdot 2 \cdot 14$

t+ = 7.5 ns typ
t– = 20 ns typ
P_D = 30 mW typ/pkg

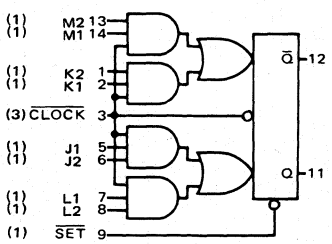
MC415/MC465 MC515/MC565 AND J-K Flip-Flop



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where $J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$
t_{pd-} = 25 ns typ
t_{pd+} = 13 ns typ
P_D = 40 mW typ/pkg

MC416/MC466 MC516/MC566 OR J-K Flip-Flop



J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care

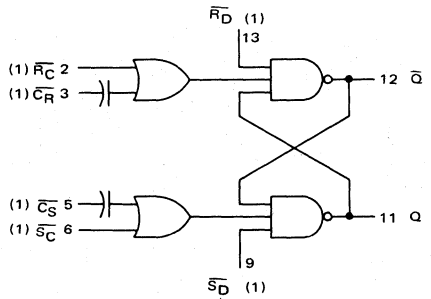
Where $J = J1 \cdot J2$
$L = L1 \cdot L2$
$K = K1 \cdot K2$
$M = M1 \cdot M2$

t_{pd-} = 25 ns typ
t_{pd+} = 13 ns typ
P_D = 50 mW typ/pkg

(continued)

FLIP-FLOPS (continued)

MC421/MC471
MC521/MC571
AC Coupled R-S Flip-Flop



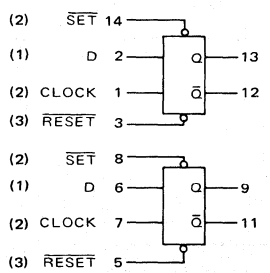
$\overline{S}$	$\overline{R}$	Q^{n+1}
0	0	Not Allowed
0	1	1
1	0	0
1	1	Q^n

Where: $\overline{\overline{S_C} \cdot \overline{C_S}} = \overline{S}$

$\overline{\overline{R_C} \cdot \overline{C_R}} = \overline{R}$

f = 10 MHz typ
P_D = 30 mW typ/pkg

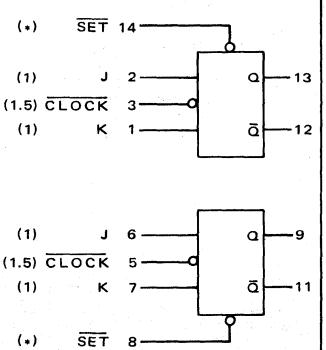
MC422/MC472
MC522/MC572
Dual Type D Flip-Flop



t_n	t_{n+1}	
D	Q	$\overline{Q}$
0	0	1
1	1	0

f = 30 MHz typ
P_D = 84 mW typ/pkg

MC423/MC473
MC523/MC573
Dual J-K Flip-Flop
(Separate Clock)

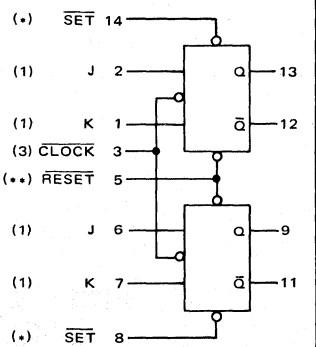


t_n		t_{n+1}	
J	K	Q	$\overline{Q}$
0	0	Q_n	$\overline{Q}_n$
0	1	0	1
1	0	1	0
1	1	$\overline{Q}_n$	Q_n

*MC423, MC473 = 1.7
*MC523, MC573 = 1.8

f = 45 MHz typ
P_D = 110 mW typ/pkg

MC424/MC474
MC524/MC574
Dual J-K Flip-Flop
(Common Clock)



t_n		t_{n+1}	
J	K	Q	$\overline{Q}$
0	0	Q_n	$\overline{Q}_n$
0	1	0	1
1	0	1	0
1	1	$\overline{Q}_n$	Q_n

*MC424, MC474 = 1.7
*MC524, MC574 = 1.8
**MC424, MC474 = 3.4
**MC524, MC574 = 3.6

f = 45 MHz typ
P_D = 110 mW typ/pkg

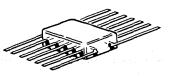
MTTL BEAM LEAD INTEGRATED CIRCUITS MTTL

MCBC5400 Series (-55 to +125°C)
MCB5400F Series (-55 to +125°C)

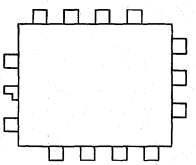
BEAM LEAD

MCBC5400/MCB5400F series integrated circuits comprise a family of transistor-transistor logic designed for general purpose digital applications. The family has a medium operating speed (15-30 MHz clock rate), good external noise immunity, high fan out, and the capability of driving capacitive loads of up to 600 pF.

This series is produced using beam lead sealed junction technology. These devices are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.

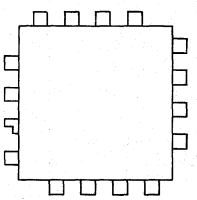


F SUFFIX
CERAMIC PACKAGE
CASE 651



BEAM LEAD CHIP
(14 Lead)

• (actual size)



BEAM LEAD CHIP
(16 Lead)

• (actual size)

MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage	7.0	Vdc
Input Voltage	5.5	Vdc
Operating Temperature Range	-55 to +125	°C
Storage Temperature Range — Ceramic	-65 to +150	°C

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Function	Type		Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg
	Chip -55° to +125°C	Case 651 -55° to +125°C			
Quad 2-Input NAND Gate	MCBC5400	MCB5400F	10	13	40
Quad 2-Input NAND Gate (Open Collector Output)	MCBC5401	MCB5401F	10	35	40
Quad 2-Input NOR Gate	MCBC5402	MCB5402F	10	13	48
Triple 3-Input NAND Gate	MCBC5410	MCB5410F	10	13	30
8-Input NAND Gate	MCBC5430	MCB5430F	10	10	10
Dual 4-Input NAND Buffer	MCBC5440	MCB5440F	30	13	50
Expandable 4-Wide 2-Input AND-OR-INVERT Gate	MCBC5453	MCB5453F	10	13	22
4-Wide 2-Input AND-OR-INVERT Gate	MCBC5454	MCB5454F	10	13	22
Dual 4-Input Expander for AND-OR-INVERT Gate	MCBC5460	MCB5460F	—	5.0	8.0
J-K Flip-Flop	MCBC5472	MCB5472F	10	30	40

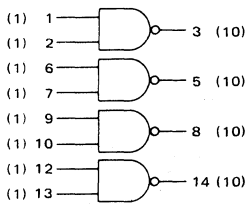
MTTL MCBC5400/MCB5400F SERIES LOGIC DIAGRAMS

Numbers at ends of terminals represent flat package pin numbers. Beam numbers are the same unless otherwise noted. Numbers in parenthesis indicate loading.

V_{CC} = Pin 4, Gnd = Pin 11 unless otherwise noted.

GATES

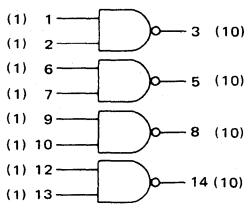
MCBC5400/MCB5400F
Quad 2-Input NAND Gate



$3 = \overline{1 \bullet 2}$

t_{pd} = 13 ns typ
P_D = 40 mW typ/pkg

MCBC5401/MCB5401F
Quad 2-Input NAND Gate

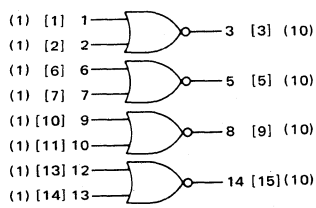


$3 = \overline{1 \bullet 2}$

t_{pd} = 35 ns typ
P_D = 40 mW typ/pkg

MCBC5402/MCB5402F
Quad 2-Input NOR Gate

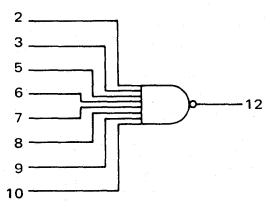
Numbers in brackets denotes beam number.



$3 = \overline{1 + 2}$

t_{pd} = 13 ns typ
P_D = 48 mW typ/pkg

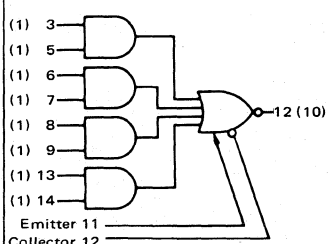
MCBC5430/MCB5430F
8-Input NAND Gate



$12 = \overline{2 \bullet 3 \bullet 5 \bullet 6 \bullet 7 \bullet 8 \bullet 9 \bullet 10}$

t_{pd} = 10 ns typ
P_D = 10 mW typ/pkg

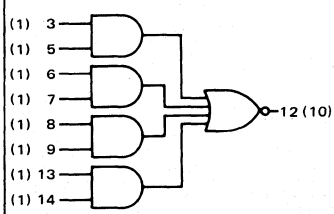
MCBC5453/MCB5453F
Expandable 4-Wide 2-Input AND-OR-INVERT Gate



$12 = \overline{(3 \bullet 5) + (6 \bullet 7) + (8 \bullet 9) + (13 \bullet 14) + (\text{Expanders})}$

t_{pd} = 13 ns typ
P_D = 22 mW typ/pkg

MCBC5454/MCB5454F
4-Wide 2-Input AND-OR-INVERT Gate



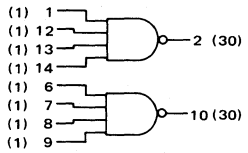
$12 = \overline{(3 \bullet 5) + (6 \bullet 7) + (8 \bullet 9) + (13 \bullet 14)}$

t_{pd} = 13 ns typ
P_D = 22 mW typ/pkg

LOGIC DIAGRAMS (continued)

BUFFER

MCBC5440/MCB5440F
Dual 4-Input NAND Buffer

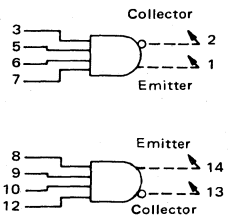


$2 = \overline{1 \cdot 12 \cdot 13 \cdot 14}$

t_{pd} = 13 ns typ
P_D = 50 mW typ/pkg

EXPANDER

MCBC5460/MCB5460F
Dual 4-Input Expander
for AND-OR-INVERT Gates

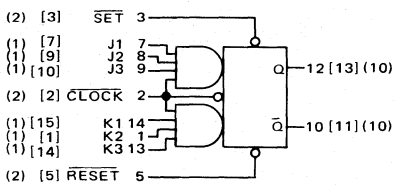


A maximum of 4 expanders may be connected to the MC5450F or MC5453F/MCB5453F.

FLIP-FLOP

MCBC5472/MCB5472F
J-K Flip-Flop

Numbers in brackets denotes beam number.



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

$J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$

f = 15 MHz
P_D = 40 mW typ/pkg

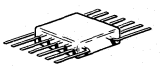
MTTL

MCE54H00 / MCE74H00 SERIES
INTEGRATED CIRCUITS

MTTL

MCE54H00 Series (–55 to +125°C)
MCE74H00 Series (0 to +70°C)

The Dielectrically Isolated Integrated Circuit (DIIC) MTTL family is designed specifically for use in military and space applications that require a high degree of reliability under severe radiation environments and post irradiation operation. The MTTL DIIC family utilizes nichrome resistors, post metalization passivation, monometallic interconnections, and very small high frequency transistor structures to enhance the radiation resistant qualities of this line. Dielectrically Isolated MTTL has the same electrical characteristics and pin configurations as the conventional MTTL 54H/74H family which make them interchangeable. This feature eliminates the need for redesigning existing equipment to gain radiation-resistance, and allows the design engineer to utilize a familiar logic type for new systems.



F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Function	Type Case 607		Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg
	–55 to +125°C	0 to +70°C			
Quad 2-Input NAND Gate	MCE54H00	MCE74H00	10	6.0	80
Quad 2-Input NAND Gate (Open Collector Output	MCE54H01	MCE74H01	10	8.0	80
Hex Inverter	MCE54H04	MCE74H04	10	6.0	120
Triple 3-Input NAND Gate	MCE54H10	MCE74H10	10	6.0	60
Dual 4-Input NAND Gate	MCE54H20	MCE74H20	10	6.0	40
11-Input NAND Gate	MCE54H31	MCE74H31	10	9.0	20
Dual 4-Input NAND Power Gate	MCE54H40	MCE74H40	30	6.0	80
Dual 2-Wide 2-Input AND-OR-INVERT Gate	MCE54H51	MCE74H51	10	6.0	58
4-Wide 2-Input AND-OR-INVERT Gate	MCE54H54A	MCE74H54A	10	6.0	40
Dual 2-Wide 2-3-Input AND-OR-INVERT Gate	MCE54H56	MCE74H56	10	6.0	58
4-Wide 3-3-2-3-Input AND-OR-INVERT Gate	MCE54H57	MCE74H57	10	6.0	40
J-K Flip-Flop	MCE54H72	MCE74H72	10	16	70
Dual J-K Flip-Flop	MCE54H73	MCE74H73	10	15	140
Dual Type D Flip-Flop	MCE54H79	MCE74H79	10	16	140
Binary To One-Of-Eight Line Decoder	MCE54H146	MCE74H146	10	–	130

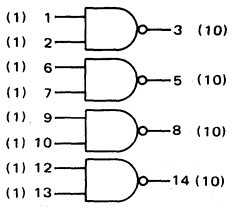
Individual data sheets for this series of TTL devices are available. To obtain copies, send your request to: Technical Information Center, Motorola Semiconductor Products, Inc., P.O. Box 20924, Phoenix, Arizona 85036.

MTTL MCE54H00 / MCE74H00 SERIES LOGIC DIAGRAMS

GATES

Flat Package: V_{CC} = Pin 4, Gnd = Pin 11.

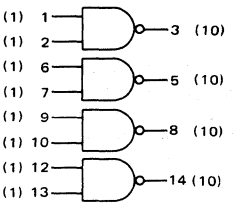
MCE54H00/MCE74H00
Quad 2-Input NAND Gate



$3 = \overline{1 \cdot 2}$

t_{pd} = 6.0 ns typ
P_D = 80 mW typ/pkg

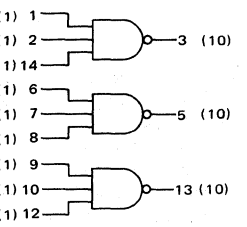
MCE54H01/MCE74H01
Quad 2-Input NAND Gate
(Open Collector Output)



$3 = \overline{1 \cdot 2}$

t_{pd} = 8.0 ns typ
P_D = 80 mW typ/pkg

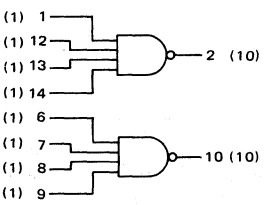
MCE54H10/MCE74H10
Triple 3-Input NAND Gate



$12 = \overline{1 \cdot 2 \cdot 13}$

t_{pd} = 6.0 ns typ
P_D = 60 mW typ/pkg

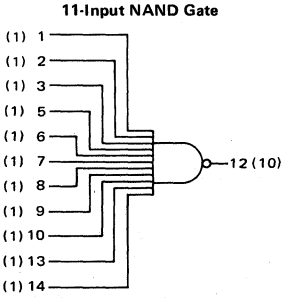
MCE54H20/MCE74H20
Dual 4-Input NAND Gate



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

t_{pd} = 6.0 ns typ
P_D = 40 mW typ/pkg

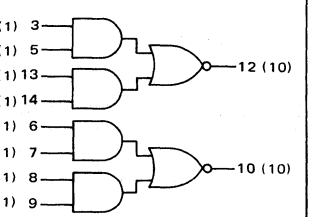
MCE54H31/MCE74H31
11-Input NAND Gate



$8 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 5 \cdot 6 \cdot 11 \cdot 12}$

t_{pd} = 9.0 ns typ
P_D = 20 mW typ/pkg

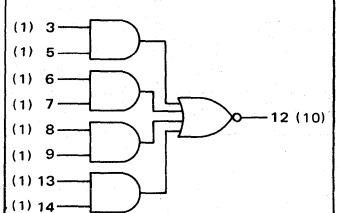
MCE54H51/MCE74H51
Dual 2-Wide 2-Input
AND-OR-INVERT Gate



$8 = \overline{(9 \cdot 10) + (13 \cdot 1)}$

t_{pd} = 6.0 ns typ
P_D = 58 mW typ/pkg

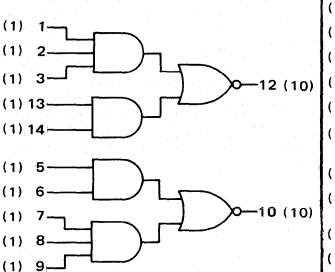
MCE54H54A/MCE74H54A
4-Wide 2-Input
AND-OR-INVERT Gate



$12 = \overline{(3 \cdot 5) + (6 \cdot 7) + (8 \cdot 9) + (13 \cdot 14)}$

t_{pd} = 6.0 ns typ
P_D = 40 mW typ/pkg

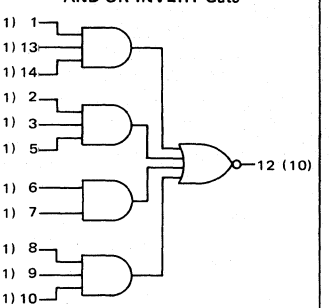
MCE54H56/MCE74H56
Dual 2-Wide 2-3-Input
AND-OR-INVERT Gate



$12 = \overline{(1 \cdot 2 \cdot 3) + (13 \cdot 14)}$

t_{pd} = 6.0 ns typ
P_D = 58 mW typ/pkg

MCE54H57/MCE74H57
4-Wide 3-3-2-3-Input
AND-OR-INVERT Gate



$12 = \overline{(1 \cdot 13 \cdot 14) + (2 \cdot 3 \cdot 5) + (6 \cdot 7) + (8 \cdot 9 \cdot 10)}$

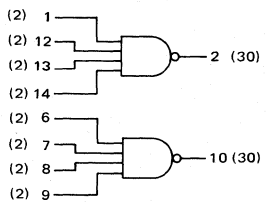
t_{pd} = 6.0 ns typ
P_D = 40 mW typ/pkg

LOGIC DIAGRAMS (continued)

Numbers at ends of terminals represent pin numbers for devices in the flat package.
Numbers in parenthesis indicate loading.

POWER GATE

MCE54H40/MCE74H40
Dual 4-Input NAND Buffer

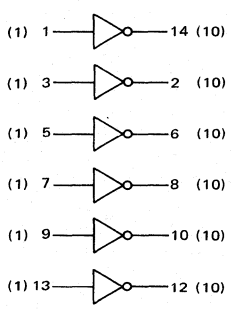


$2 = \overline{1 \cdot 12 \cdot 13 \cdot 14}$

t_{pd} = 6.0 ns typ
P_D = 80 mW typ/pkg

INVERTER

MCE54H04/MCE74H04
Hex Inverter

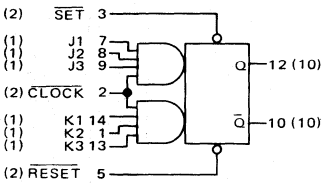


$14 = \overline{1}$

t_{pd} = 6.0 ns typ
P_D = 120 mW typ/pkg

FLIP-FLOPS

MCE54H72/MCE74H72
J-K Flip-Flop

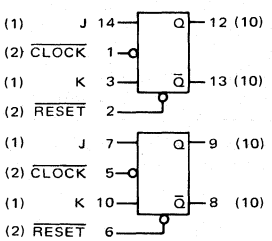


t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

$J = \overline{J1 \cdot J2 \cdot J3}$
$K = \overline{K1 \cdot K2 \cdot K3}$

f = 30 MHz
P_D = 70 mW typ/pkg

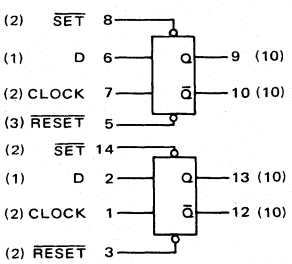
MCE54H73/MCE74H73
Dual J-K Flip-Flop



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

f = 30 MHz
P_D = 140 mW typ/pkg

MCE54H79/MCE74H79
Dual Type D Flip-Flop



D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

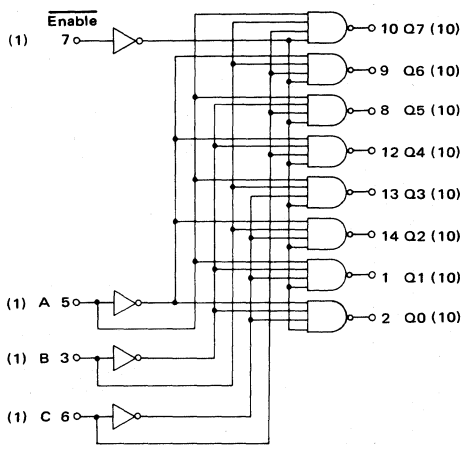
$Q^{n+1} = D^n$

f = 35 MHz
P_D = 140 mW typ/pkg

LOGIC DIAGRAMS (continued)

DECODER

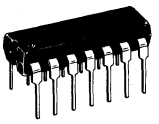
MCE54H146/MCE74H146
Binary to 1-of-8 Line Decoder



t_{pd} = 14 ns typ
P_D = 130 mW typ/pkg

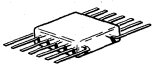
INTEGRATED CIRCUITS

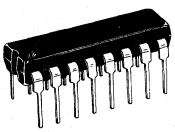
MTTL integrated circuit memories comprise a growing family of memories designed for direct general purpose memory applications in transistor-transistor logic systems. The family consists of both read-only memories (ROMs) for look-up tables, microprograms, or code conversion, and read-write random access memories (RAMs) for scratch pad or cache applications. The family has medium operating speed, good external noise immunity and high fanout.



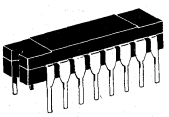
P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116

F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

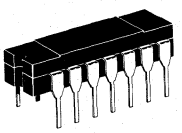




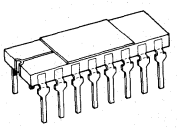
P SUFFIX
PLASTIC PACKAGE
CASE 612



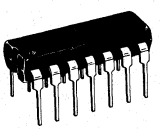
L SUFFIX
CERAMIC PACKAGE
CASE 620



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



L SUFFIX
CERAMIC PACKAGE
CASE 638



P SUFFIX
PLASTIC PACKAGE
CASE 648

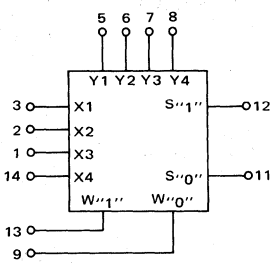
FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Function	Type ① −55 to +125°C	Case	Type ① 0 to +75°C	Case	Output Current Sinking Capability I_{OL} in mA	Propagation Delay t_{pd} ns typ	Power Dissipation P_D mW typ/pkg
16-Bit Scratch Pad Memory Cell (16 One-Bit Words)	MC4304F,L	607,632	MC4004F,L,P	607,632,605	40 (Open Collector)	Write mode: 25 Sense mode: 15	250
16-Bit Scratch Pad Memory Cell (16 One-Bit Words)	MC4305F,L	607,632	MC4005F,L,P	607,632,605	20	Write mode: 25 Sense mode: 15	250
			0 to +70°C				
16-Bit Scratch Pad Memory Cell With Gated Inputs (16 One-Bit Words)	MC5484L	620	—	—	40 (Open Collector)	Write mode: 25 Sense mode: 15	250
	—	—	MC7484L,P	620,612	20		
256-Bit Read Only Memory (32 Eight-Bit Words)	—	—	MCM4002L,P	620,648	12 (Open Collector) 10 (Pullup Resistors)	Address Time <50 ns	350
64-Bit Random Access Memory (16 Four-Bit Words)	—	—	MCM4064L	620	15	Access Time <60 ns	6 mW/bit
			0 to +85°C				
	—	—	MCM4064AL	638			

① F suffix denotes ceramic flat package, L suffix denotes ceramic dual in-line package, P suffix denotes plastic dual in-line package.

MEMORIES

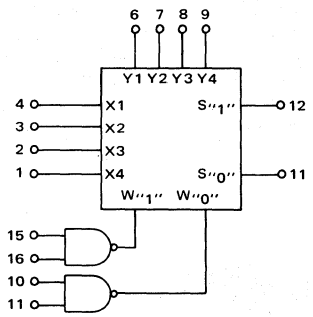
MC4004, MC4005, MC4304, MC4305
16-Bit Scratch Pad Memory Cell



V_{CC} = Pin 4
Gnd = Pin 10

t_{pd}: Write Mode = 25 ns typ
Read Mode = 15 ns typ
P_D = 250 mW typ/pkg

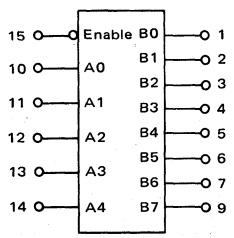
MC5484, MC7484
16-Bit Scratch Pad Memory Cell With Gated Inputs



V_{CC} = Pin 5
Gnd = Pin 12

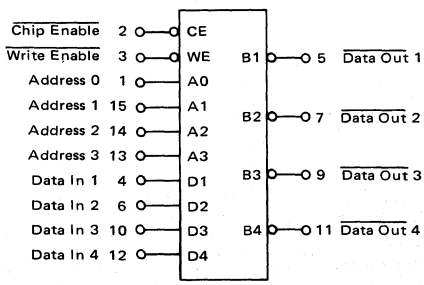
t_{pd}: Write Mode = 25 ns typ
Read Mode = 15 ns typ
P_D = 250 mW typ/pkg

MCM4002
256-Bit Read Only Memory



V_{CC} = Pin 16
Gnd = Pin 8

MCM4064A, MCM4064
64-Bit Random Access Memory



V_{CC} = Pin 16
Gnd = Pin 8

MTTL III

INTEGRATED CIRCUITS

MC3100/MC3000 SERIES

MTTL III

MC3100/3000 SERIES
INTEGRATED CIRCUITS

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INTRODUCTION

MTTL III integrated circuits are designed with speed approaching the limit for saturated logic and for good load driving capability. This line includes all the characteristics that have made transistor-transistor logic so popular. The major advantage of MTTL III over other TTL lines is the square transfer characteristic (Figure 1) that exists only for the MTTL III family. Because of this "ideal" transfer characteristic, the MTTL III family is the only TTL line that is truly compatible with MDTL. Another advantage of this family over competitive TTL lines is that it is designed to minimize problems associated with ringing.

The circuits in the MTTL III family are distinguished by a multiple-emitter input transistor, a darlington active "pull-up" in the upper output network, and an active bypass network in the base of the output pull-down transistor as shown in Figure 2.

The multiple-emitter input configuration offers the maximum logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The Darlington output configuration provides very low output impedances in each of the two output states. These low impedances result in excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

The active bypass shown in the unshaded area of Figure 2 holds the phase inverter transistor "off" until gate threshold is reached. This circuit operation provides the squared transfer characteristic shown in Figure 1.

In addition to improving the transfer characteristic, the bypass network offers a number of advantages compared to a simple resistor that can be traced to a much smaller impedance variation with temperature.

1. *Lower bypass impedance for the reverse current of the output transistor at elevated temperatures, provides faster turn-off.*
2. *A lower current spike during the turn-off transient causes a lower ac power factor resulting in a lower total power consumption. This advantage is even more pronounced at higher temperatures.*
3. *Faster turn-on at low temperature.*

FIGURE 1 – COMPARISON OF CONVENTIONAL TRANSISTOR-TRANSISTOR LOGIC AND MTTL III

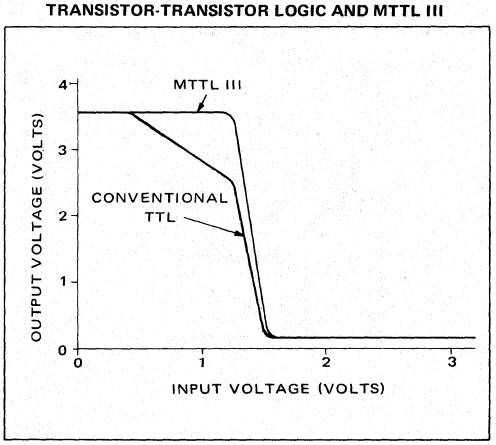
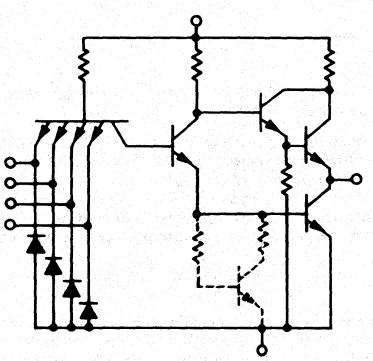


FIGURE 2 – TYPICAL MTTL III CIRCUIT



TYPICAL CHARACTERISTICS

Typical operating characteristics of the MTTL III family include: (Unless otherwise indicated, the parameters are defined for V_{CC} = +5.0 volts and T_A = +25°C.)

Supply Voltage Operating Range = 4.5 to 5.5 volts

Operating Temperature Range:
- MC3100 Series = -55°C to +125°C
- MC3000 Series = 0 to +75°C

Output Drive Capability
- Gates (Output Loading Factor):
  - MC3100 Series = 10 Gates
  - MC3000 Series = 10 Gates
- Capacitance = 600 pF

Output Impedance
- High State = 10 ohms nominal (unsaturated)
- Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits
- +5.5 volts maximum
- -1.5 volts minimum (1)

Switching Threshold = 1.5 volts nominal

Input Impedance
- High State = 400 k ohms nominal
- Low State = 2.4 k ohms nominal

Worst-Case dc Noise Margin
- High State = 0.700 volt minimum
- Low State = 0.700 volt minimum

Power Dissipation
- 22 mW per gate typical
- 50-80 mW per flip-flop typical

Switching Speeds (2)
- Average Propagation Delay = 6.0 ns per gate typical
  13 ns per flip-flop typical
- Rise Time = 1.0 ns typical
- Fall Time = 1.3 ns typical

Flip-Flop Clock Frequency (MC3061) = 50 MHz maximum.

(1) Assuming unused inputs are returned to voltage not greater than 4.0 Vdc.

(2) The switching characteristics of the MTTL III family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2} \text{ ns}$$

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative output transition from the 2.0 V to the 1.0 V level.

"NAND" GATES

The basic gate of the MTTL III logic family is the positive logic NAND gate. This gate is characterized by high speed, good load driving capability, superior transfer characteristic, and freedom from ringing problems. Representative of the various NAND gates presently available in the MTTL III family is the 4-input NAND gate (½ of the MC3110/3010) shown in Figure 3.

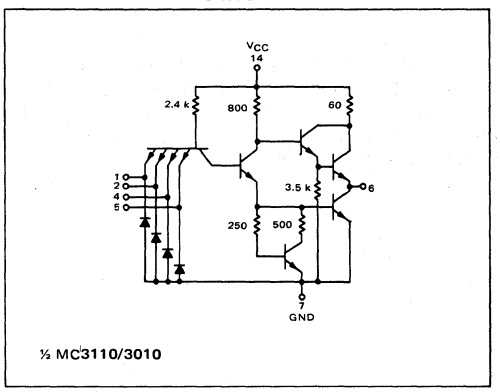
"AND" GATES

While it is possible to design a complete logic system with NAND logic, it is often desirable to use other logic forms to save circuits, power dissipation, and propagation delay. Therefore, Motorola has added the positive logic AND function to the MTTL III family.

Examples of the AND function are the standard quad 2-input gate, dual 4-input gate, dual 4-input power gate and a dual 3-input, 3-output line driver.

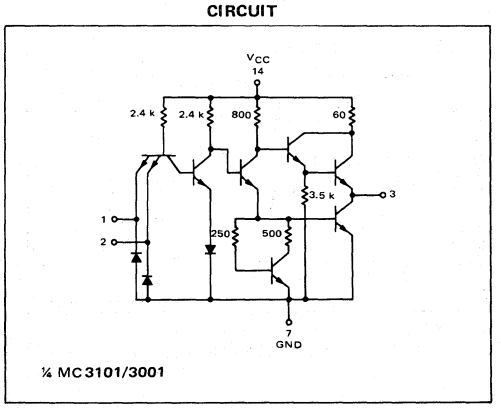
The technique used to form the AND function is the addition of an inverter to the basic NAND circuit. As shown in Figure 4, the inverter transistor with a collector resistor and an offset diode connected to its emitter is inserted between the multiple-emitter input transistor and the basic circuit phase-splitter transistor. The extra inversion adds only 3.0 ns propagation delay and about 6.0 mW additional power dissipation.

FIGURE 3 – MTTL III POSITIVE LOGIC "NAND" GATE CIRCUIT



½ MC3110/3010

FIGURE 4 – MTTL III POSITIVE LOGIC "AND" GATE CIRCUIT



¼ MC3101/3001

"OPEN COLLECTOR" GATES

This open-collector MTTL gate, when supplied with the proper load resistor R_L, may be paralleled with other open-collector MTTL gates to perform the "Implied AND" function, and simultaneously will drive from one to nine MTTL III loads. When used by itself the gate can drive ten MTTL III loads. Only one resistor is needed for any set of paralleled outputs; the upper and lower limit for R_L will be determined by the desired circuit configuration. The maximum resistor value is required to ensure that sufficient load current and off current through the outputs will be available during a logic "1" level at the output. The minimum resistor value is required to ensure that I_{RL} plus the load current will not exceed the current sinking capabilities of one output transistor with the output in the logic "0" state.

For both limits the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

Where V_{RL} is in volts and I_{RL} in amperes.

$R_{L(max)}$ Calculations (See Figure 5)

The allowable voltage drop across R_L (V_{RL}) is the difference between V_{CC} and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH}.$$

The total current through R_L (I_{RL}) is the sum of the load currents (I_R) and the off-level reverse currents (I_{CEX}) through each of the paralleled outputs:

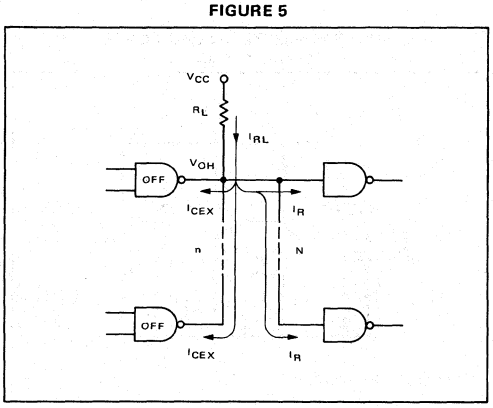
$$I_{RL} = n\, I_{CRX} + N\, I_R,$$

where n = number of outputs paralleled, and N = number of MTTL III loads.

Therefore, the equation for $R_{L(max)}$ is:

$$R_{L(max)} = \frac{V_{CC} - V_{OH}}{n\, I_{CEX} + N\, I_R}.$$

FIGURE 5

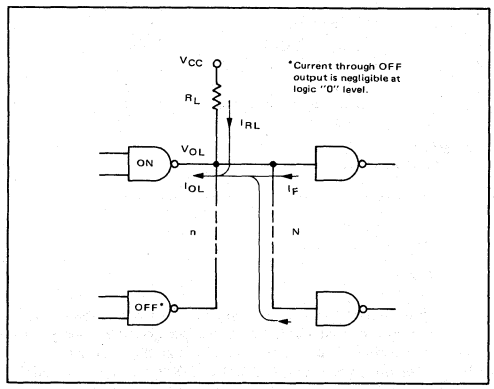


$R_{L(min)}$ Calculations (See Figure 6)

Unless it can be absolutely guaranteed that more than one output transistor will be on during all logic "0" output periods, the sink current (I_{OL}) must be limited to 20 mA, the maximum current which will ensure a maximum logic "0" level (V_{OL}) of 0.4 volt. The sink current comes partly through the load resistor and partly from the inputs being driven (I_F). The equation for calculating the minimum value of R_L is:

$$R_{L(min)} = \frac{V_{CC} - V_{OL}}{I_{OL} - N\, I_F}.$$

FIGURE 6



"AND-OR-INVERT" GATES

Unlike the MDTL family of logic circuits, the outputs of MTTL logic circuits cannot be tied together to perform the "Implied AND", often called the "Wired OR" function. If the outputs of the MTTL family devices are tied together, the lower output transistor of one circuit and the upper output transistor of another circuit can be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground, and due to excessive current flow, the saturated output state cannot be maintained and the desired logic function is not satisfied.

To retain the logical advantages offered by the "Implied AND" with the speed and load driving capability of an active pull-up, the MTTL III family offers an AND-OR-INVERT Gate. The gate in Figure 7 incorporates two 2-input AND functions with outputs that are ORed and inverted. The AND function is provided by two multiple-emitter input transistors (Q1a and Q1b). The OR and INVERT operation is accomplished by two paralleled transistors (Q2a and Q2b) sharing a single collector resistor and a single bypass network. These paralleled transistors in turn drive the standard output.

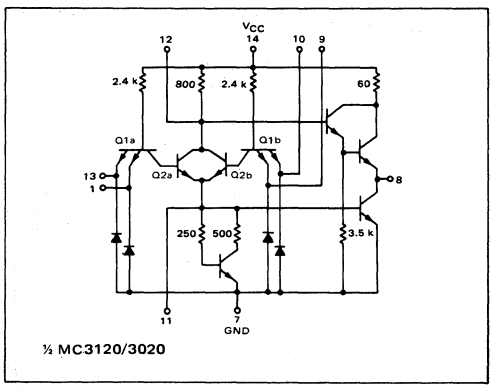
The common collector and emitter nodes of one gate in each package are available externally to permit expansion.

EXPANDER AND EXPANDER NODES

The ORing nodes of 1/2 the MC3120/3020 dual AND-OR-INVERT Gate (Figure 7) are available for expanding the number of AND gates to four. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND

gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 1.0 ns/pF.

FIGURE 7 – MTTL III "AND-OR-INVERT" GATE CIRCUIT



"NOR" GATES

To save inverters, the system designer often needs the positive logic NOR function as well as the negative logic NOR available with the standard NAND gate. This capability is incorporated in the MTTL III line in the form of the MC3102/3002, quad 2-input NOR Gate. The NOR gate is a modified AND-OR-INVERT gate with only a single emitter on each input transistor, as shown in Figure 8.

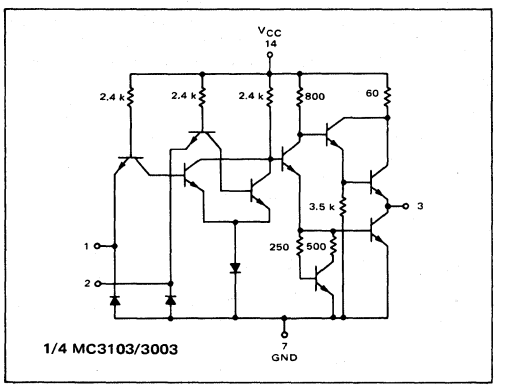
"OR" GATES

To provide the system designer with still another tool for optimum design, the MTTL III Series also offers the positive logic OR function. As shown in Figure 9, the OR is essentially a NOR gate with an additional inverter.

POWER GATES

Standard MTTL III gates offer good load driving capability and high fan-out. In most systems, however, there are a few applications that exceed the capability of a standard gate. The MTTL III power gates, shown in Figure 10, are designed to meet these requirements with a minimum of additional circuitry. Available in both NAND and AND functions, the power gates feature output circuitry designed to provide twice the fan-out of conventional gates: 20 standard gate loads instead of 10.

FIGURE 9 – MTTL III POSITIVE LOGIC "OR" GATE CIRCUIT



LINE DRIVERS

To minimize switching transients on long lines, the MTTL III family includes dual 3-input/3-output series-terminated line drivers. Two outputs have 75-ohm resistors in series with the standard output node, and one is connected directly to the node. A good match can be made at the output of each resistor when driving 93-ohm coax or 120-ohm twisted pair. For loads of 50 to 93 ohms, the two resistive outputs are paralleled for impedance matching. The non-resistive output can be used to drive adjacent loads in a normal fashion. The total number of output loads connected to the direct output (non-resistive output) is the standard fan-out of 10, minus the number of resistor terminated outputs being used.

FIGURE 8 – MTTL III POSITIVE LOGIC "NOR" GATE CIRCUIT

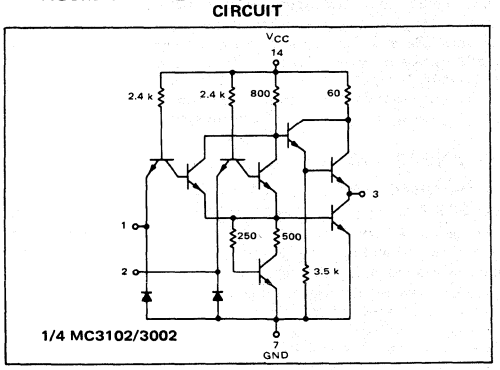


FIGURE 10 – MTTL III POWER GATE CIRCUIT (AND)

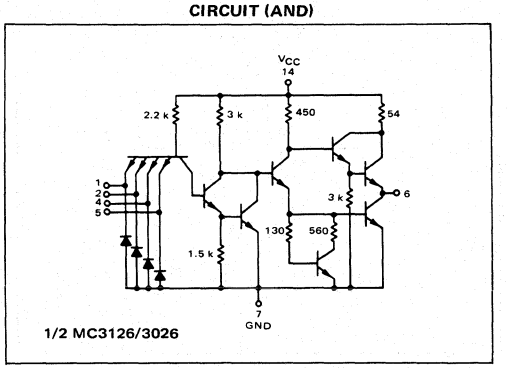


Figure 11 shows 1/2 of the circuit of the MC3129/3029, dual 3-input, 3-output series terminated NAND line driver. Figure 12 shows a typical application of this circuit and Figure 13 demonstrates the effects of series termination without a significant loss in high state noise immunity.

FIGURE 11 – MTTL III TERMINATED LINE DRIVER (NAND)

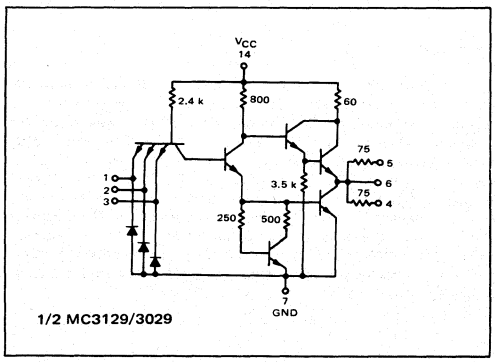


FIGURE 12 – TYPICAL APPLICATION OF THE LINE DRIVER

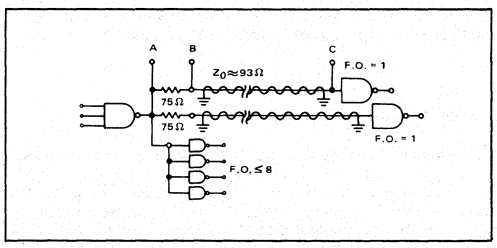
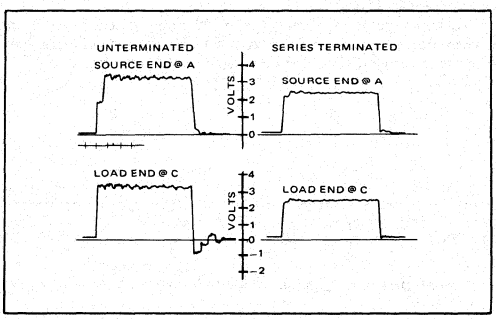


FIGURE 13 – EFFECTS OF SERIES TERMINATION WITH A MTTL III GATE DRIVING A 93-OHM LINE



OPERATING CHARACTERISTICS OF FLIP-FLOPS

The cornerstone of any modern logic family is the capability of its storage elements. The MTTL III flip-flops are designed to give maximum logic performance with fewer system restrictions than their predecessors. Three basic designs are typified by the MC3150/3050, MC3160/3060, MC3161/3061 and MC3162/3062. Common to all designs are:

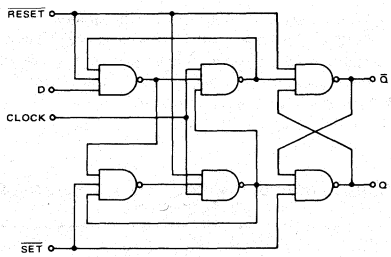
1. Edge clocking.

   The flip-flop is clocked at the normal MTTL III threshold voltage (approximately 1.5 V @ 25°C).

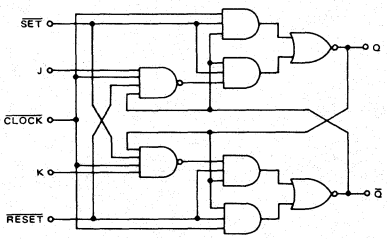
2. Overriding asynchronous inputs.

   The direct SET and RESET inputs control the operation of the flip-flop regardless of the state of the clock or the information on synchronous inputs.

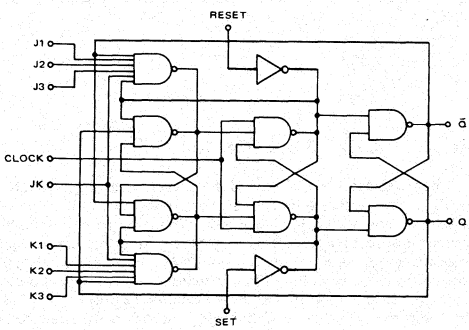
FIGURE 14 – LOGIC DIAGRAMS OF EDGE-CLOCKED MTTL III FLIP-FLOPS



MC3160/3060



MC3161/3061



MC3150/3050

3. Short set-up times.

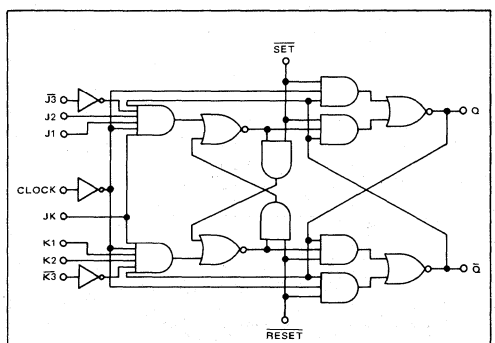
   Prior to the clocking edge, the input information must become stable. The MTTL III flip-flops require only a minimum of time to read a "1" or a "0". Therefore data may be applied anytime in the clock period except during the time interval between the Set-up and Hold times. This characteristic permits higher clock frequencies or eliminates the necessity for critical control of clock pulse width.

4. All inputs to the storage elements including the clock input have inputs that are compatible with all three MTTL families.

The MC3150/3050 and MC3160/3060 flip-flops are positive edge triggered storage elements. That is, the inputs are enabled on the negative edge of the clock and the information is stored in the flip-flop on the positive edge of the clock. The MC3161/3061 and MC3162/3062 dual flip-flops are negative edge triggered devices and therefore operate in precisely the opposite manner. That is, data is stored on the negative edge of the clock.

In addition to the previously mentioned storage elements. The MC3152/3052 Master-Slave flip-flop is also available. Data is stored in Master flip-flop when the clock is low and transferred to the Slave flip-flop when the clock goes high. Detailed discussion of each of the MTTL III flip-flops is provided on the individual data sheets.

FIGURE 15 – LOGIC DIAGRAM OF MTTL III MASTER-SLAVE J-K FLIP-FLOP



MC3152/3052

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL circuit, the designer must always be aware of the problems caused by very high switching speeds. These switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the upper RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions will help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rates of change of current and voltage for a single MTTL III gate are in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL III circuits. A comparatively large, low-inductance type capacitor (in the 1.0 μF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 μF capacitors for every five packages throughout a breadboard is adequate to suppress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The typical average dc power dissipation is given for each MTTL III device (3). It should be noted that the totem-pole output common to all high-level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.4 mW/MHz/output for a 15-pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL III circuits.

Unused Inputs and Unused Gates

To minimize potential problems resulting from external noise, the unused inputs of any MTTL III logic circuit should not be left open, but should either be tied to the used inputs or returned to a voltage between 2.0 and 5.5 Vdc. (For flip-flops, see appropriate data sheet for additional detail.) If the unused inputs are returned to a voltage, care should be exercised to insure that the absolute voltage between the most negative input level and that voltage does not exceed +5.5 volts. The total number of inputs that can be tied to the output of any driving gate is 25. (This is defined as high-state output loading factor.) It should be noted that the low-state output loading rules must still be maintained. The minimum logical "1" level for the high-state output loading is summarized for V_{CC} = 5.0 V, V_{IL} = 1.1 V, and I_{OH} = -2.0 mA: V_{OH} = 2.5 volts minimum @ 0°C.

To minimize power drain, the inputs of any unused gate in a package should be maintained at the level that would place the outputs in the high state (the low power dissipation state).

---

(3) $P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$

where I_{PDL} and I_{PDH} are the typical current drains at V_{CC} = +5.0 V.

DEFINITIONS

BV_{in}	Input breakdown voltage
C_T	Total parasitic capacitance, which includes probe, wiring, and load capacitances
I_C	Collector current
I_{CO}	Expander collector leakage current
I_D	Input diode current with negative voltage applied
I_E	Emitter current
I_{EO}	Expander emitter leakage current
I_{EXE}	Expander drive current at emitter node of AND-OR-INVERT gate
I_F	Input forward current with V_{CC} applied
I_{F1}	Input forward current with V_{CCL} applied
I_{F2}	Input forward current with V_{CCH} applied
I_{FC}	Clock input forward current
I_{FD}	D input forward current
I_{FJ}	J input forward current
I_{FK}	K input forward current
I_{FJK}	JK input forward current
I_{FR}	RESET input forward current
I_{FS}	SET input forward current
I_{in}	Input current
I_{max}	Maximum rated power supply current with V_{max} applied
I_{OH}	Output high state current
I_{OHA}	Unterminated output high state current
$I_{OHB, C}$	Terminated output high state current
I_{OL}	Output low state current
I_{OL1}	Output low state current with V_{CCL} applied
I_{OL1A}	Unterminated output low state current with V_{CCL} applied
I_{OL2}	Output low state current with V_{CCH} applied
I_{OL2A}	Unterminated output low state current with V_{CCH} applied
$I_{OL1B, 1C}$	Terminated output low state current with V_{CCL} applied
$I_{OL2A, 2C}$	Terminated output low state current with V_{CCH} applied
I_{PD}	Flip-flop power supply drain current
I_{PDH}	Power supply drain with inputs high
I_{PDL}	Power supply drain with inputs low
I_R	Input leakage current
I_{RC}	Clock input leakage current
I_{RD}	D input leakage current
I_{RJ}	J input leakage current
I_{RK}	K input leakage current
I_{RJK}	JK input leakage current
I_{RR}	RESET input leakage current
I_{RS}	SET input leakage current
I_{SC}	Short-circuit current
P_1	Pulse used to set flip-flop state
PRF	Pulse repetition frequency
PW	Pulse width
t_-	Fall time
t_+	Rise time
$t_{Hold\ "0"}$	Minimum time that low state data must be maintained after the clocking edge
$t_{Hold\ "1"}$	Minimum time that high state data must be maintained after the clocking edge
Δt_{pd}	Average increase in propagation delay per expander AND gate when connected to an AND-OR-INVERT gate
$\Delta t_{pd}/pF$	Increased propagation delay caused by additional capacitance at expansion points
$t_{pd\ "0"}$	Turn-on delay
$t_{pd\ "1"}$	Turn-off delay
$t_{sd\ "0"}$	Turn-on delay from asynchronous input
$t_{sd\ "1"}$	Turn-off delay from asynchronous input
$t_{Setup\ "0"}$	Minimum time that low state data must be applied prior to the clocking edge
$t_{Setup\ "1"}$	Minimum time that high state data must be applied prior to the clocking edge
TP_{in}	Test point at input of device under test
TP_{out}	Test point at output of device under test
$V_{BE\ max}$	Emitter node threshold voltage for logic "0" output level
$V_{BE\ min}$	Emitter node threshold voltage for logic "1" output level
V_{CC}	Power supply voltage
V_{CCH}	High power supply voltage
V_{CCL}	Low power supply voltage
V_D	Diode clamp voltage
V_{EE1}	Voltage applied to expander emitter for V_{OL} test
V_{EE2}	Voltage applied to expander emitter node for I_{CO} test
V_F	Maximum logic "0" level output voltage
V_{IH}	Logic "1" threshold voltage
V_{IHX}	Reduced supply voltage to hold input above threshold and to prevent noise from entering the device
V_{IL}	Logic "0" threshold voltage
V_{max}	Maximum rated power supply voltage
V_{OH}	Output high voltage with I_{OH} source current
V_{OL}	Output low voltage with I_{OL} source current
V_{OL1}	Maximum output low voltage with V_{CCL} applied
V_{OL2}	Maximum output low voltage with V_{CCH} applied
V_{OL3}	Maximum output low voltage on terminated output with V_{CCL} applied
V_{OL4}	Maximum output low voltage on terminated output with V_{CCH} applied
V_R	Logic "1" minimum reverse voltage
V_{RH}	Logic "1" maximum reverse voltage

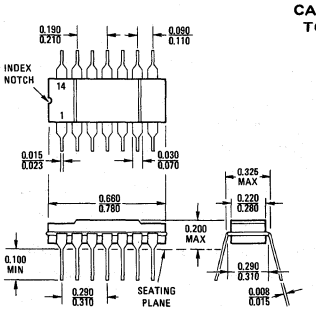
MAXIMUM RATINGS

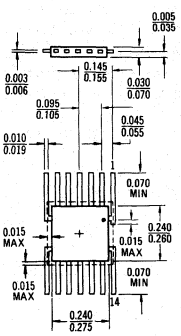
Rating		Value	Unit
Supply Voltage – Continuous	MC3100 series	+7.0	Vdc
	MC3000 series	+7.0	Vdc
Supply Operating Voltage Range		4.5 to 5.5	Vdc
Input Voltage		+5.5	Vdc
Output Voltage		+5.5	Vdc
Operating Temperature Range	MC3100 series	-55 to +125	°C
	MC3000 series	0 to +75	°C
Storage Temperature Range – Ceramic Package		-65 to +175	°C
Plastic Package		-55 to +125	°C

PACKAGING

All MTTL III integrated circuits are available in the TO-86, 14-lead ceramic flat package (add suffix F to type number when ordering), and in the TO-116, 14-lead dual in-line ceramic package (suffix L). MC3000 Series devices are also available in the TO-116, 14-lead dual in-line plastic package (suffix P).

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

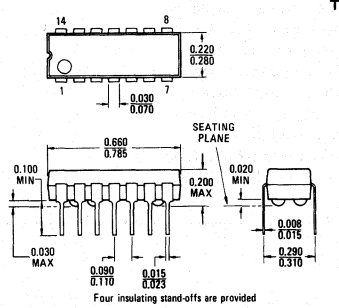




Lead 1 identified by color dot or by elbow on lead.

F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



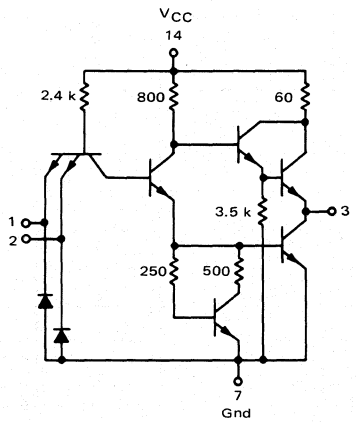
Four insulating stand-offs are provided

QUAD 2-INPUT "NAND" GATE

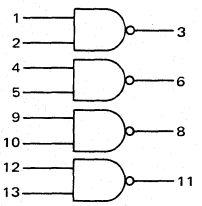
MC3100F • MC3000F
MC3100L • MC3000L,P

(54H00J) (74H00J,N)

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



Positive Logic: $3 = \overline{1 \cdot 2}$

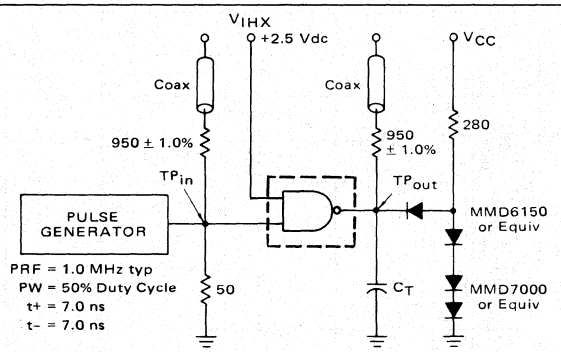
Negative Logic: $3 = \overline{1 + 2}$

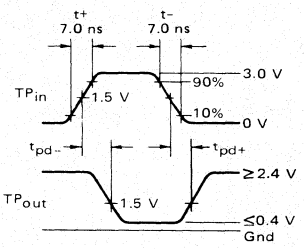
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 88 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

Pin numbers for the 54H00F/74H00F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3100F,L/3000F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H00F/74H00F	1	2	3	6	7	5	11	8	9	10	14	12	13	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





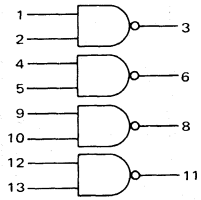
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature	TEST CURRENT / VOLTAGE VALUES													
	mA				Volts									
	I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3100 −55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3100 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
MC3100 +125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3000 0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
MC3000 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
MC3000 +75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

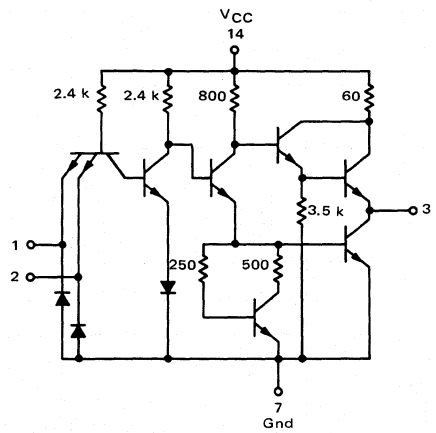
Characteristic	Symbol	Pin Under Test	MC3100 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3000 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	2	-	-	-	14	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2,7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2,7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	1	-	-	2	-	-	14	-	-	7*
	V_{OH}	3	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	1	-	-	-	2	-	-	14	-	-	7*
Short-Circuit Current	I_{SC}	3	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	25	-	-	-	-	-	25	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	40	-	40	-	40	-	40	-	40	-	40	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	16.8	-	16.8	-	16.8	-	16.8	-	16.8	-	16.8	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters Turn-On Delay	t_{pd+}	1, 3	-	-	-	10	-	-	-	-	-	10	-	-	ns	Pulse In 1	Pulse Out 3	-	-	-	-	-	-	-	-	14	-	-	2	7*
Turn-Off Delay	t_{pd-}	1,3	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	14	-	-	2	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

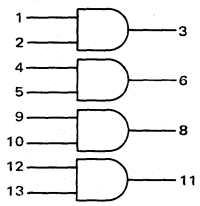
MC3101F • MC3001F
MC3101L • MC3001L,P

(54H08J) **(74H08J,N)**

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



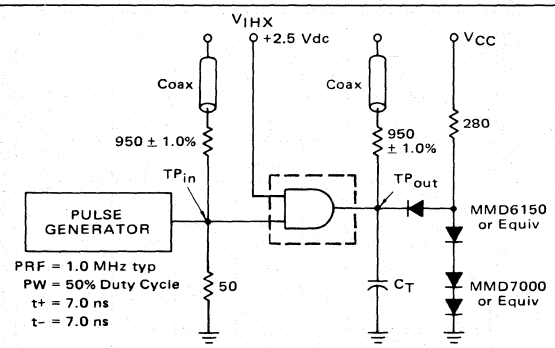
This device consists of four 2-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

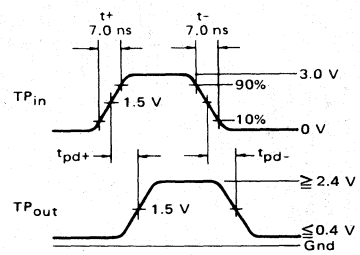


Positive Logic: $3 = 1 \cdot 2$
Negative Logic: $3 = 1 + 2$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 112 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





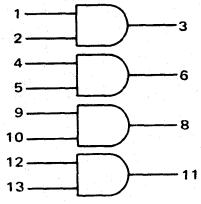
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



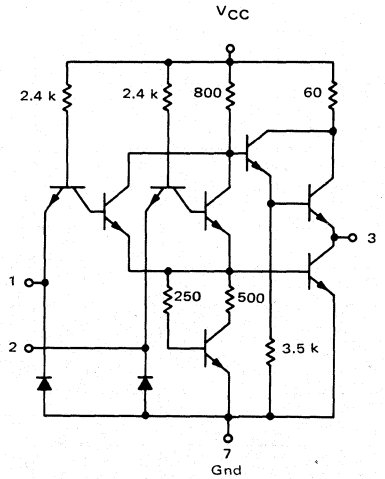
@ Test Temperature		I_{OL} mA	I_{OH} mA	I_{in} mA	I_D mA	V_{IL} Volts	V_{IH} Volts	V_F Volts	V_R Volts	V_{RH} Volts	V_{max} Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts	V_{IHX} Volts
MC3101	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3001	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3101 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3001 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	2*	-	-	14	-	-	7
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2,7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2,7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	1	-	-	-	2*	-	-	14	-	-	7
	V_{OH}	3	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	-	1	-	-	2*	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	3	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	1,2*	-	-	-	14	-	3,7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	34	-	-	-	-	-	34	-	-	mAdc	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	14	-	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	24	-	24	-	24	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	-	-	-	14	-	7
	I_{PDL}	14	-	48	-	48	-	48	-	48	-	48	-	48	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,4,5,7, 9,10,12,13
Switching Parameters																Pulse In	Pulse Out													
Turn-On Delay	t_{pd-}	1,3	-	-	-	15	-	-	-	-	-	15	-	-	ns	1	3	-	-	-	-	-	-	*	-	14	-	-	2	7
Turn-Off Delay	t_{pd+}	1,3	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	*	-	14	-	-	2	7

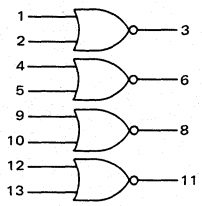
*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

MC3102F • MC3002F
MC3102L • MC3002L,P

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



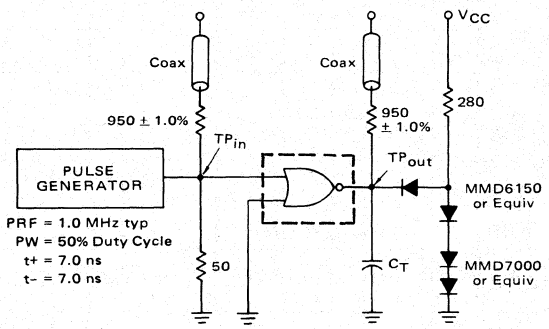
This device consists of four 2-input NOR gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.

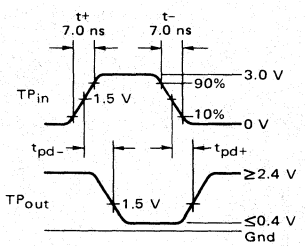


Positive Logic: $3 = \overline{1+2}$
Negative Logic: $3 = \overline{1 \bullet 2}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 122 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





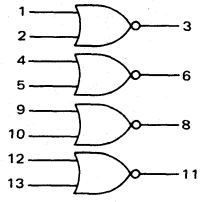
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



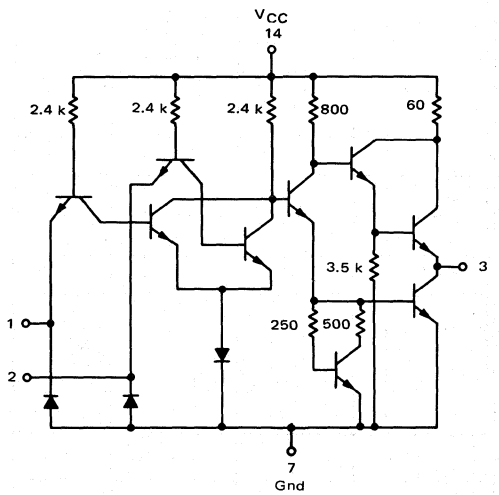
	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES												
		mA				Volts								
		I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
MC3102	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5
MC3002	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC3102 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3002 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	2	-	-	-	14	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	2, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	2, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	14	-	7*
Output Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	1	-	-	-	-	-	14	-	2, 7*
	V_{OH}	3	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	1	-	-	-	-	-	-	14	-	2, 7*
Short-Circuit Current	I_{SC}	3	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	1, 2, 3, 7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	38	-	-	-	-	-	38	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	45	-	45	-	45	-	45	-	45	-	45	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	14	7
	I_{PDL}	14	-	28	-	28	-	28	-	28	-	28	-	28	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1, 3	-	-	-	10	-	-	-	-	-	10	-	-	ns	Pulse In 1	Pulse Out 3	-	-	-	-	-	-	-	-	14	-	-	2, 7*
Turn-Off Delay	t_{pd+}	1, 3	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	14	-	-	2, 7*

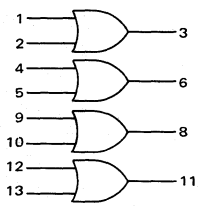
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

MC3103F • MC3003F
MC3103L • MC3003L,P

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



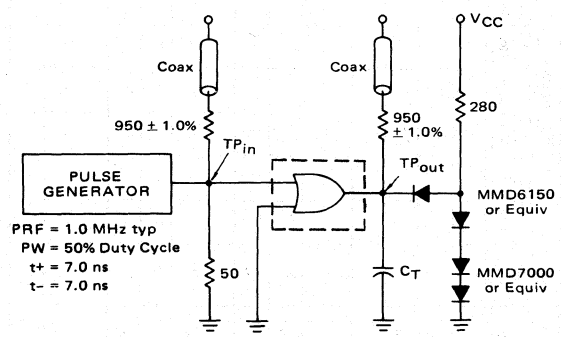
This device consists of four 2-input OR gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

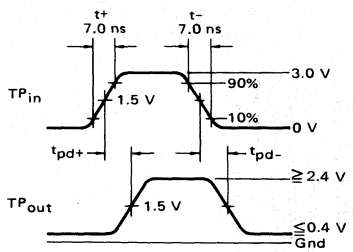


Positive Logic: 3 = 1 + 2
Negative Logic: 3 = 1 • 2

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





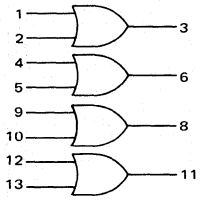
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES												
		mA				Volts								
		I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
MC3103	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5
MC3103	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5
MC3103	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5
MC3003	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25
MC3003	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25
MC3003	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC3103 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3003 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	2*	-	-	-	14	7
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	*	-	-	-	14	2,7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	*	-	-	-	14	2,7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	*	-	-	14	-	7
Output Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	1	-	-	-	2*	-	-	14	-	7
	V_{OH}	3	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	-	1	-	-	2*	-	-	14	-	7
Short-Circuit Current	I_{SC}	3	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	1, 2*	-	-	-	14	3,7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	45	-	-	-	-	-	45	-	-	mAdc	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	14	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	34	-	34	-	34	-	34	-	34	-	34	mAdc	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	-	-	-	14	7
	I_{PDL}	14	-	58	-	58	-	58	-	58	-	58	-	58	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,4,5,7, 9,10,12,13
Switching Parameters																Pulse In	Pulse Out												
Turn-On Delay	t_{pd-}	1, 3	-	-	-	15	-	-	-	-	-	15	-	-	ns	1	3	-	-	-	-	-	-	*	-	14	-	-	7
Turn-Off Delay	t_{pd+}	1, 3	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	*	-	14	-	-	7

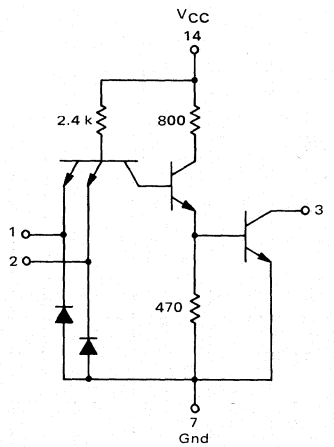
*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}

QUAD 2-INPUT "NAND" GATE
(Open Collector)

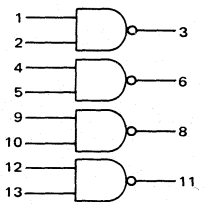
MC3104F • MC3004F
MC3104L • MC3004L,P

(54H01J) (74H01J,N)

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR-function is required or for driving discrete components.



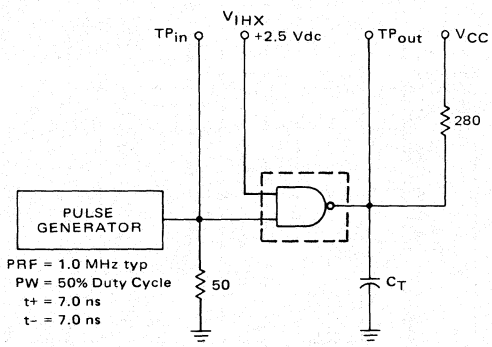
Positive Logic: $3 = \overline{1 \bullet 2}$
Negative Logic: $3 = \overline{1 + 2}$

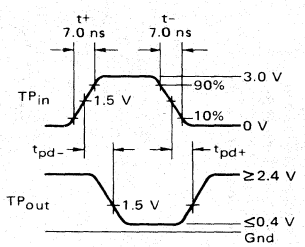
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 88 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

Pin numbers for the 54H01F/74H01F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3104F,L/3004F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H01F/74H01F	1	2	3	6	7	5	11	8	9	10	14	12	13	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



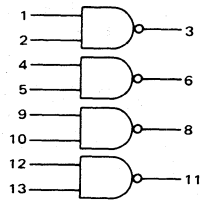


C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES													
		mA			Volts										
		I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3104	−55°C	20	-	-	1.1	2.0	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-
	+25°C	20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	2.5
	+125°C	20	-	-	0.8	1.8	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-
MC3004	0°C	20	-	-	1.1	2.0	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-
	+25°C	20	1.0	-10	1.1	1.8	0.4	2.5	4.0	5.5	7.0	5.0	4.75	5.25	2.5
	+75°C	20	-	-	0.9	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-

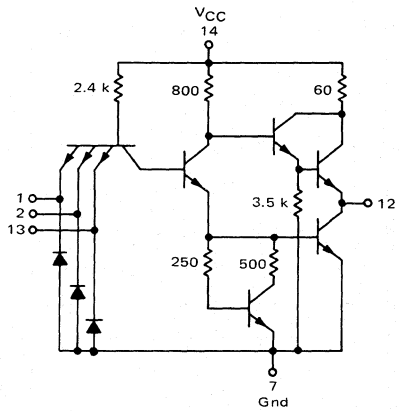
Characteristic	Symbol	Pin Under Test	MC3104 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3004 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	1	-	2	-	-	-	14	-	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	1	-	-	-	-	-	14	-	2,7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	14	-	2,7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	1	-	-	2	-	-	-	14	-	-	7*
Output Leakage Current	I_{CEX}	3	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	1	2	-	-	-	3	-	-	14	-	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	25	-	-	-	-	-	25	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	36	-	36	-	36	-	36	-	36	-	36	mAdc	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	-	14	-	7
	I_{PDL}	14	-	10	-	10	-	10	-	10	-	10	-	10	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1, 3	-	-	-	14	-	-	-	-	-	14	-	-	ns	Pulse In: 1	Pulse Out: 3	-	-	-	-	-	-	-	-	14	-	-	2	7*
Turn-Off Delay	t_{pd+}	1,3	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	3	-	-	-	-	-	-	-	-	14	-	-	2	7*

* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

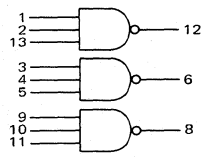
TRIPLE
3-INPUT "NAND" GATE

MC3105F • MC3005F
MC3105L • MC3005L,P
(54H10J) (74H10J,N)

CIRCUIT SCHEMATIC
1/3 OF CIRCUIT SHOWN



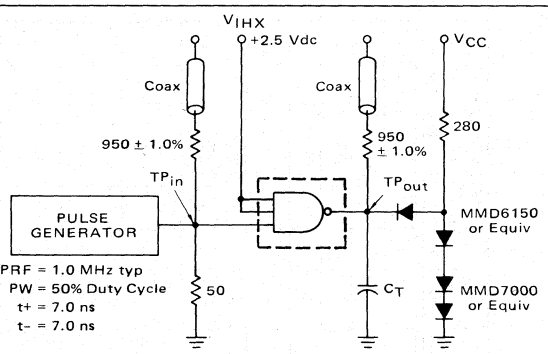
This package consists of three 3-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.

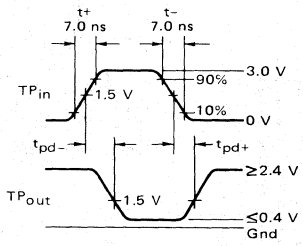


Positive Logic: $12 = \overline{1 \cdot 2 \cdot 13}$
Negative Logic: $12 = \overline{1 + 2 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





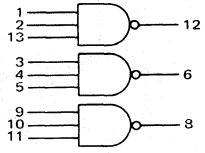
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES														
		mA				Volts										
		I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
MC3105	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-	
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5	
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-	
MC3005	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-	
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5	
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-	

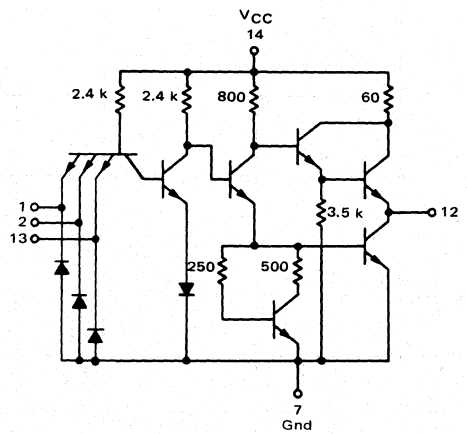
Characteristic	Symbol	Pin Under Test	MC3105 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3005 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	2, 13	-	-	-	14	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 7, 13*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 7, 13*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V_{OL}	12	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	12	-	-	-	-	1	-	-	2, 13	-	-	14	-	-	7*
	V_{OH}	12	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	12	-	-	1	-	-	-	2, 13	-	-	14	-	-	7*
Short-Circuit Current	I_{SC}	12	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 7,* 12, 13
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	20	-	-	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7, 9, 10, 11, 13
Power Supply Drain	I_{PDH}	14	-	30	-	30	-	30	-	30	-	30	-	30	mAdc	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 11, 13	-	-	-	14	-	7
	I_{PDL}	14	-	12.6	-	12.6	-	12.6	-	12.6	-	12.6	-	12.6	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5,7, 9,10,11,13
Switching Parameters Turn-On Delay	t_{pd-}	1, 12	-	-	-	10	-	-	-	-	-	10	-	-	ns	Pulse In: 1	Pulse Out: 12	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*
Turn-Off Delay	t_{pd+}	1, 12	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

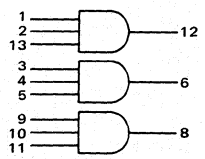
MC3106F • MC3006F
MC3106L • MC3006L,P

(54H11J) (74H11J,N)

CIRCUIT SCHEMATIC
1/3 OF CIRCUIT SHOWN



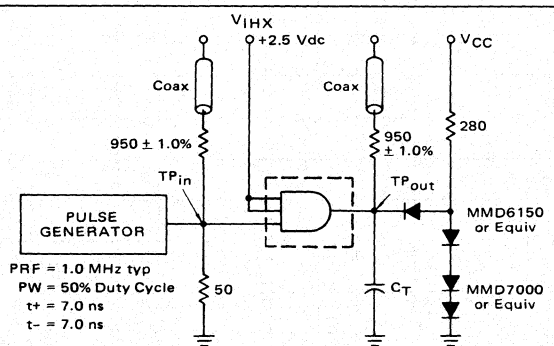
This device consists of three 3-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

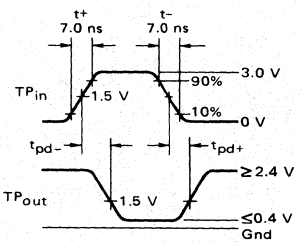


Positive Logic: $12 = 1 \cdot 2 \cdot 13$
Negative Logic: $12 = 1 + 2 + 13$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 84 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





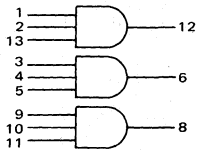
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	MC3106 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3006 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc
Output Output Voltage	V_{OL}	12	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc
	V_{OH}	12	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc
Short-Circuit Current	I_{SC}	12	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	28	-	-	-	-	-	28	-	-	mAdc
Power Supply Drain	I_{PDH}	14	-	20	-	20	-	20	-	20	-	20	-	20	mAdc
	I_{PDL}	14	-	40	-	40	-	40	-	40	-	40	-	40	mAdc
Switching Parameters Turn-On Delay	t_{pd-}	1,12	-	-	-	15	-	-	-	-	-	15	-	-	ns
Turn-Off Delay	t_{pd+}	1,12	-	-	-	12	-	-	-	-	-	12	-	-	ns

@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3106 −55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3106 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
MC3106 +125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3006 0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
MC3006 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
MC3006 +75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

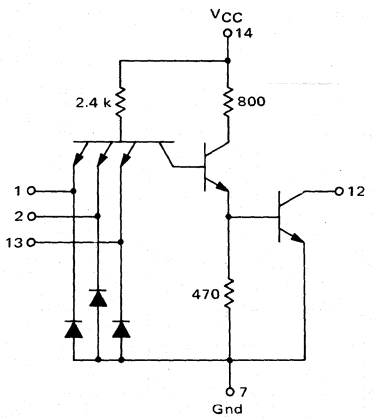
TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
12	-	-	-	-	-	1	-	2,13*	-	-	-	14	-	7
-	-	-	-	-	-	-	1	*	-	-	-	14	-	2,7,13
-	-	1	-	-	-	-	-	*	-	-	-	14	-	2,7,13
-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
12	-	-	-	1	-	-	-	2,13*	-	-	14	-	-	7
-	12	-	-	-	1	-	-	2,13*	-	-	14	-	-	7
-	-	-	-	-	-	-	-	1,2,13*	-	-	-	14	-	7,12
-	-	-	-	-	-	-	-	1,2,3,4,5, 9,10,11,13	14	-	-	-	-	7
-	-	-	-	-	-	-	-	1,2,3,4,5, 9,10,11,13	-	-	-	14	-	7
-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5,7, 9,10,11,13
Pulse In 1	Pulse Out 12	-	-	-	-	-	-	*	-	14	-	-	2,13	7
1	12	-	-	-	-	-	-	*	-	14	-	-	2,13	7

*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

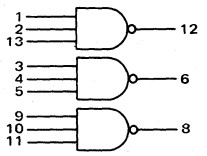
TRIPLE 3-INPUT "NAND" GATE
(Open Collector)

MC3107F • MC3007F
MC3107L • MC3007L,P

CIRCUIT SCHEMATIC
1/3 OF CIRCUIT SHOWN



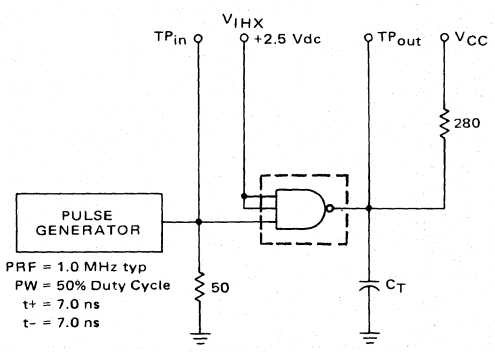
This device consists of three 3-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR function is required or for driving discrete components.



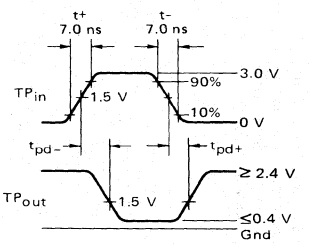
Positive Logic: $12 = \overline{1 \cdot 2 \cdot 13}$
Negative Logic: $12 = \overline{1 + 2 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PRF = 1.0 MHz typ
PW = 50% Duty Cycle
t+ = 7.0 ns
t- = 7.0 ns

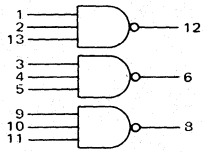


C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES														
		mA			Volts											
		I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
MC3107	−55°C	20	-	-	1.1	2.0	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-	
MC3107	+25°C	20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	2.5	
MC3107	+125°C	20	-	-	0.8	1.8	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-	
MC3007	0°C	20	-	-	1.1	2.0	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-	
MC3007	+25°C	20	1.0	-10	1.1	1.8	0.4	2.5	4.0	5.5	7.0	5.0	4.75	5.25	2.5	
MC3007	+75°C	20	-	-	0.9	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-	

Characteristic	Symbol	Pin Under Test	MC3107 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3007 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	1	-	2, 13	-	-	-	14	-	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	1	-	-	-	-	-	14	-	2, 7, 13*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	14	-	2, 7, 13*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V_{OL}	12	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	12	-	-	-	1	-	-	2, 13	-	-	-	14	-	-	7*
Output Leakage Current	I_{CEX}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	1	2,13	-	-	-	12	-	-	14	-	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	20	-	-	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7, 9, 10, 11, 13
Power Supply Drain	I_{PDH}	14	-	28	-	28	-	28	-	28	-	28	-	28	mAdc	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 11, 13	-	-	-	-	14	-	7
	I_{PDL}	14	-	13.5	-	13.5	-	13.5	-	13.5	-	13.5	-	13.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5,7, 9,10,11,13
Switching Parameters Turn-On Delay	t_{pd-}	1, 12	-	-	-	14	-	-	-	-	-	14	-	-	ns	Pulse In 1	Pulse Out 12	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*
Turn-Off Delay	t_{pd+}	1, 12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*

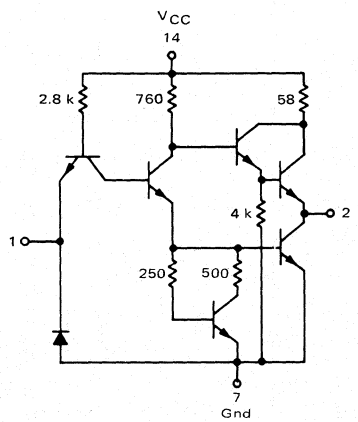
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

HEX INVERTER

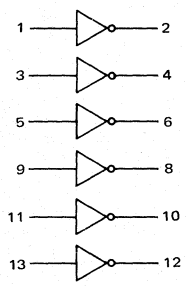
MC3108F • MC3008F
MC3108L • MC3008L,P

(54H04J) (74H04J,N)

CIRCUIT SCHEMATIC
1/6 OF CIRCUIT SHOWN



This device offers six independent inverting gates in a single package. Each gate consists of a single input driving an output inverter.



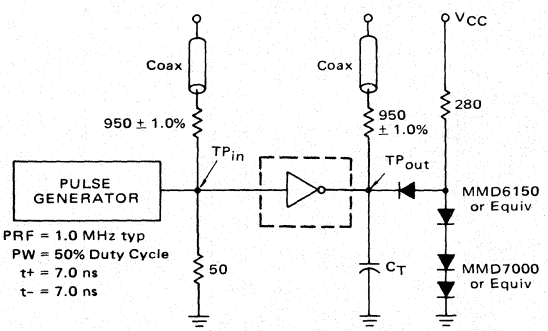
Positive Logic: $2 = \overline{1}$

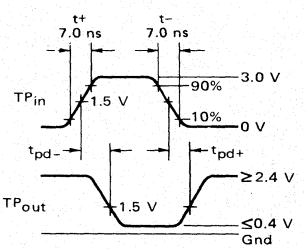
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 140 typ/pkg
Propagation Delay Time = 6 ns typ

Pin numbers for the 54H04F/74H04F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3108F,L/3008F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H04F/74H04F	1	14	3	2	5	6	11	8	7	10	9	12	13	14

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





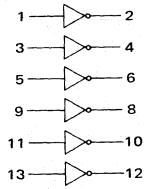
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES													
		mA				Volts									
		I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
MC3108	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	
MC3108	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	
MC3108	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	
MC3008	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	
MC3008	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	
MC3008	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC3108 Test Limits −55°C Min	MC3108 Test Limits −55°C Max	MC3108 Test Limits +25°C Min	MC3108 Test Limits +25°C Max	MC3108 Test Limits +125°C Min	MC3108 Test Limits +125°C Max	MC3008 Test Limits 0°C Min	MC3008 Test Limits 0°C Max	MC3008 Test Limits +25°C Min	MC3008 Test Limits +25°C Max	MC3008 Test Limits +75°C Min	MC3008 Test Limits +75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	-	-	-	-	14	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	14	-	7*
Output Output Voltage	V_{OL}	2	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	2	-	-	-	-	1	-	-	-	-	-	14	-	7*
	V_{OH}	2	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	2	-	-	1	-	-	-	-	-	-	14	-	7*
Short-Circuit Current	I_{SC}	2	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	37.5	-	-	-	-	-	37.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	1,3,5,7,9 11,13
Power Supply Drain	I_{PDH}	14	-	58	-	58	-	58	-	58	-	58	-	58	mAdc	-	-	-	-	-	-	-	-	1,3,5,9, 11,13	-	-	-	14	7
	I_{PDL}	14	-	26	-	26	-	26	-	26	-	26	-	26	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	1,3,5,7,9 11,13
Switching Parameters																Pulse In	Pulse Out												
Turn-On Delay	t_{pd+}	1,2	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	2	-	-	-	-	-	-	-	-	14	-	-	7*
Turn-Off Delay	t_{pd-}	1,2	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	2	-	-	-	-	-	-	-	-	14	-	-	7*

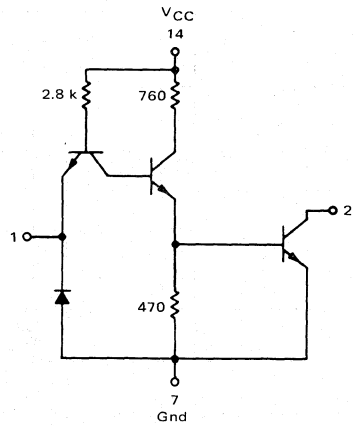
* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

HEX INVERTER

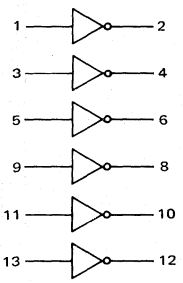
MC3109F • MC3009F
MC3109L • MC3009L,P

(54H05J) (74H05J,N)

CIRCUIT SCHEMATIC
1/6 OF CIRCUIT SHOWN



This device consists of six independent inverting gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.



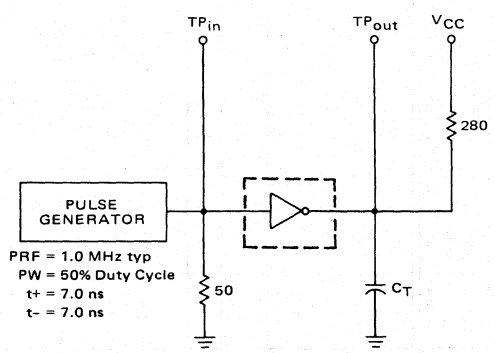
Positive Logic: $2 = \overline{1}$

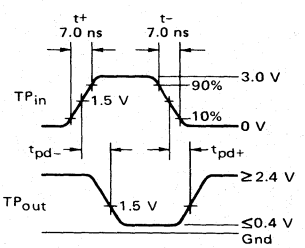
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 90 mW typ/pkg
Propagation Delay Time = 8 ns typ

Pin numbers for the 54H05F/74H05F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3109F,L/3009F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H05F/74H05F	1	14	3	2	5	6	11	8	7	10	9	12	13	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



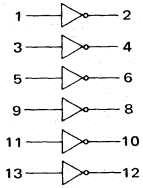


C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



@ Test Temperature	TEST CURRENT / VOLTAGE VALUES													
	mA			Volts										
	I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
MC3109 −55°C	20	-	-	1.1	2.0	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	
MC3109 +25°C	20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	
MC3109 +125°C	20	-	-	0.8	1.8	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	
MC3009 0°C	20	-	-	1.1	2.0	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	
MC3009 +25°C	20	1.0	-10	1.1	1.8	0.4	2.5	4.0	5.5	7.0	5.0	4.75	5.25	
MC3009 +75°C	20	-	-	0.9	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	

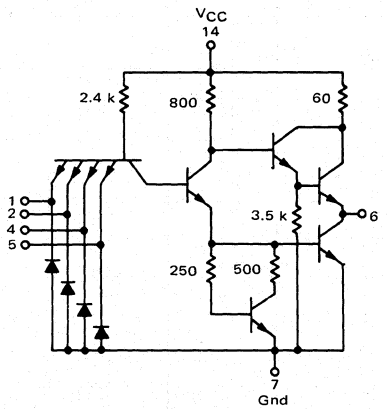
Characteristic	Symbol	Pin Under Test	MC3109 Test Limits −55°C Min	MC3109 Test Limits −55°C Max	MC3109 Test Limits +25°C Min	MC3109 Test Limits +25°C Max	MC3109 Test Limits +125°C Min	MC3109 Test Limits +125°C Max	MC3009 Test Limits 0°C Min	MC3009 Test Limits 0°C Max	MC3009 Test Limits +25°C Min	MC3009 Test Limits +25°C Max	MC3009 Test Limits +75°C Min	MC3009 Test Limits +75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	1	-	-	-	-	-	-	14*	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	1	-	-	-	-	-	14	7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	14	7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	7*
Output Output Voltage	V_{OL}	2	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	2	-	-	-	1	-	-	-	-	-	-	14	-	7*
Output Leakage Current	I_{CEX}	2	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	1	-	-	-	-	2	-	-	14	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	37.5	-	-	-	-	-	37.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	1,3,5,7, 9,11,13
Power Supply Drain	I_{PDH}	14	-	58	-	58	-	58	-	58	-	58	-	58	mAdc	-	-	-	-	-	-	-	1,3,5,7, 9,11,13	-	-	-	-	14	7
	I_{PDL}	14	-	26	-	26	-	26	-	26	-	26	-	26	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	1,3,5,7, 9,11,13
Switching Parameters																Pulse In	Pulse Out												
Turn-On Delay	t_{pd-}	1,2	-	-	-	15	-	-	-	-	-	15	-	-	ns	1	2	-	-	-	-	-	-	-	-	14	-	-	7*
Turn-Off Delay	t_{pd+}	1,2	-	-	-	18	-	-	-	-	-	18	-	-	ns	1	2	-	-	-	-	-	-	-	-	14	-	-	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

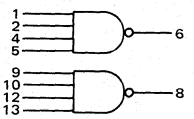
MC3110F • MC3010F
MC3110L • MC3010L,P

(54H20J) (74H20J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND gates. These gates may be cross-coupled to form a set-reset flip-flop.



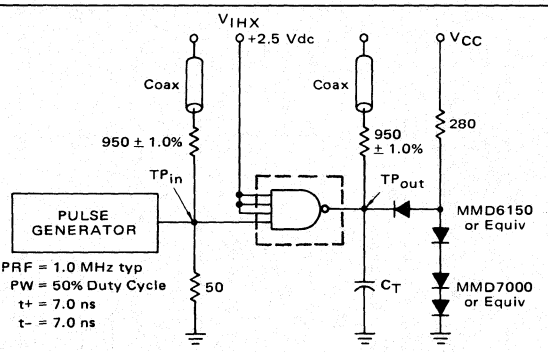
Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$
Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

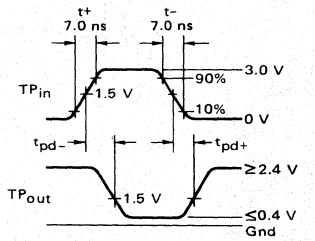
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

Pin numbers for the 54H20F/74H20F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3110F,L/3010F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H20F/74H20F	1	12	3	13	14	2	11	10	6	7	14	8	9	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





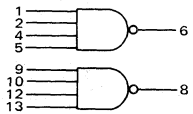
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
		mA				Volts									
		I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3110	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3010	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

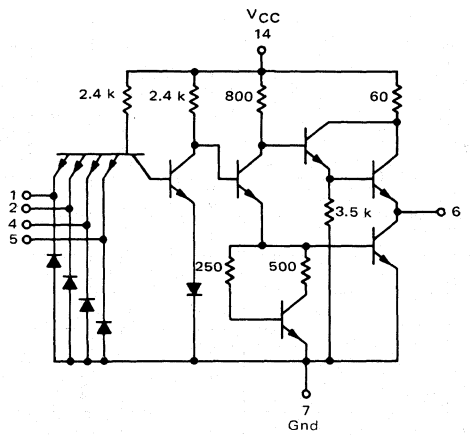
Characteristic	Symbol	Pin Under Test	MC3110 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3010 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 4, 5, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	1	-	-	2, 4, 5	-	-	14	-	-	7*
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	1	-	-	-	2, 4, 5	-	-	14	-	-	7*
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 6, 7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	12.5	-	-	-	-	-	12.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	20	-	20	-	20	-	20	-	20	-	20	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	8.4	-	8.4	-	8.4	-	8.4	-	8.4	-	8.4	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1, 6	-	-	-	10	-	-	-	-	-	10	-	-	ns	Pulse In: 1	Pulse Out: 6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

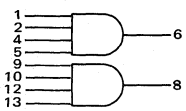
DUAL 4-INPUT "AND" GATE

MC3111F • MC3011F
MC3111L • MC3011L,P
(54H21J) (74H21J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



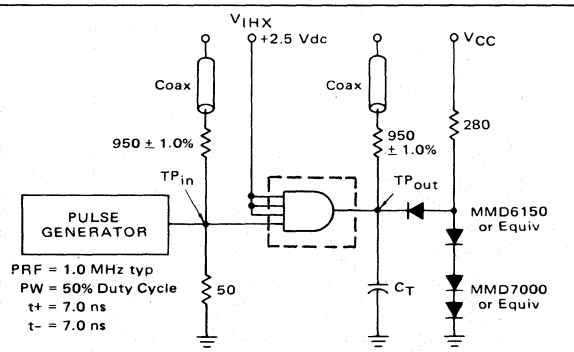
This device consists of two 4-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

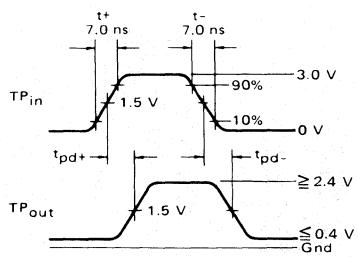


Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$
Negative Logic: $6 = 1 + 2 + 4 + 5$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 56 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





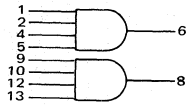
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature		I_{OL} (mA)	I_{OH} (mA)	I_{in} (mA)	I_D (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{RH} (Volts)	V_{max} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	V_{IHX} (Volts)
MC3111	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3011	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3111 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3011 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
																TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	2,4,5*	-	-	-	14	-	7
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2, 4, 5, 7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2, 4, 5, 7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	1	-	-	-	2,4,5*	-	-	14	-	-	7
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	1	-	-	2,4,5*	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	1,2,4,5*	-	-	-	14	-	6,7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	18	-	-	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	1,2,4,5, 9,10,12,13	14	-	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	13.2	-	13.2	-	13.2	-	13.2	-	13.2	-	13.2	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	26	-	26	-	26	-	26	-	26	-	26	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters																Pulse In	Pulse Out													
Turn-On Delay	t_{pd-}	1, 6	-	-	-	15	-	-	-	-	-	15	-	-	ns	1	6	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7

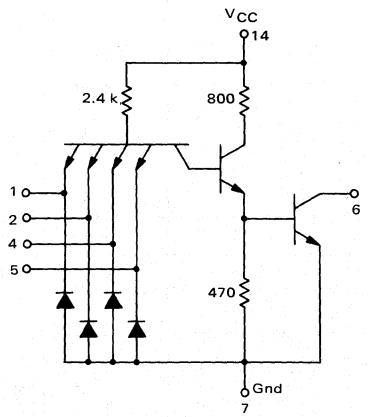
*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}

DUAL 4-INPUT "NAND" GATE
(Open Collector)

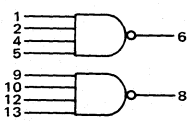
MC3112F • MC3012F
MC3112L • MC3012L,P

(54H22J) (74H22J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR function is required or for driving discrete components.



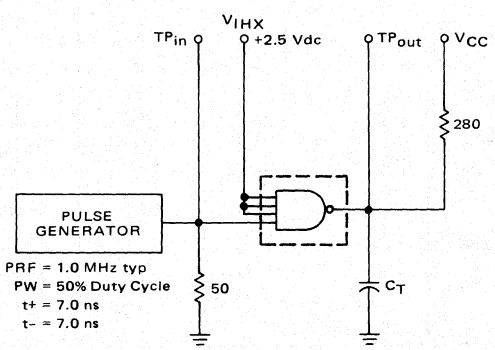
Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$
Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

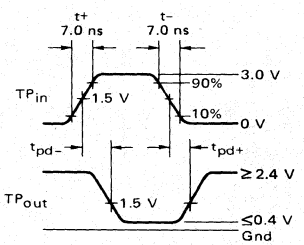
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

Pin numbers for the 54H22F/74H22F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3112F,L/3012F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H22F/74H22F	1	12	3	13	14	2	11	10	6	7	14	8	9	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



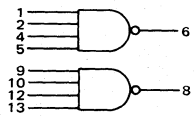


C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

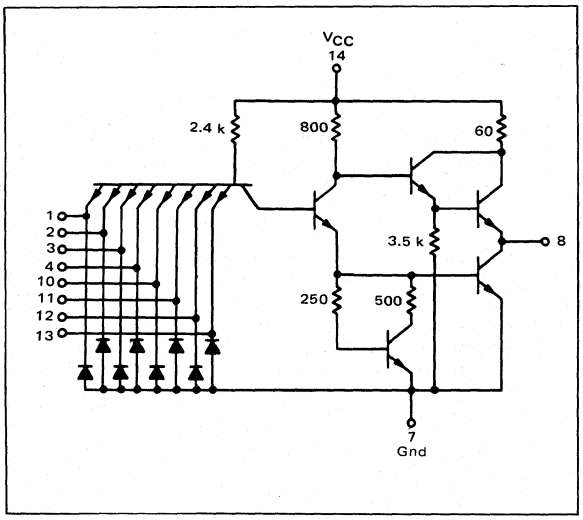


@ Test Temperature		I_{OL} (mA)	I_{in} (mA)	I_D (mA)	V_{IL} (Volts)	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3112	−55°C	20	-	-	1.1	2.0	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-
	+25°C	20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	2.5
	+125°C	20	-	-	0.8	1.8	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-
MC3012	0°C	20	-	-	1.1	2.0	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-
	+25°C	20	1.0	-10	1.1	1.8	0.4	2.5	4.0	5.5	7.0	5.0	4.75	5.25	2.5
	+75°C	20	-	-	0.9	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-

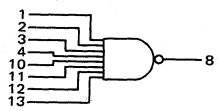
Characteristic	Symbol	Pin Under Test	MC3112 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3012 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	1	-	-	-	-	-	14	-	2, 4, 5, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	-	7
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	1	-	-	2, 4, 5	-	-	-	14	-	-	7*
Output Leakage Current	I_{CEX}	-	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	1	2,4,5	-	-	-	6	-	-	14	-	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	12.5	-	-	-	-	-	12.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	20	-	20	-	20	-	20	-	20	-	20	mAdc	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	-	14	-	7
	I_{PDL}	14	-	5.0	-	5.0	-	5.0	-	5.0	-	5.0	-	5.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1, 6	-	-	-	14	-	-	-	-	-	14	-	-	ns	Pulse In: 1	Pulse Out: 6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

MC3115F • MC3015F
MC3115L • MC3015L,P



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders and decoders.



Positive Logic:

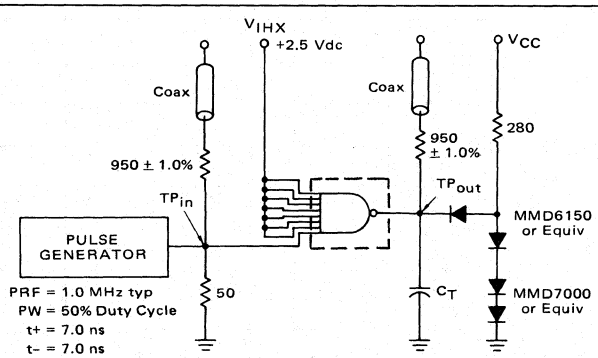
$$8 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 10 \cdot 11 \cdot 12 \cdot 13}$$

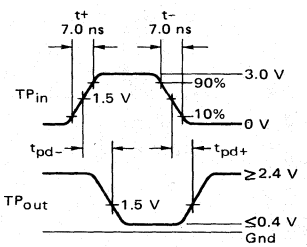
Negative Logic:

$$8 = \overline{1 + 2 + 3 + 4 + 10 + 11 + 12 + 13}$$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 22 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





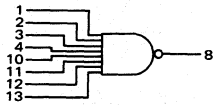
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of this device. To complete testing, sequence through remaining inputs in the same manner.



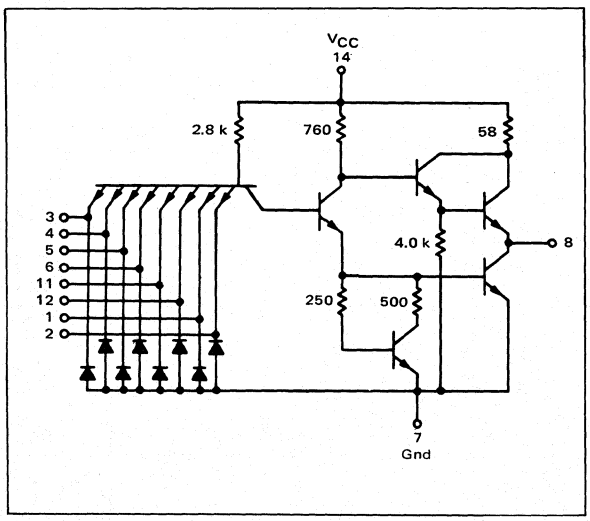
	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
		mA				Volts									
		I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3115	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3015	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3115 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3015 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	2, 3, 4, 10, 11, 12, 13	-	-	-	14	-	7
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 3, 4, 7, 10, 11, 12, 13
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 3, 4, 7, 10, 11, 12, 13
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7
Output Output Voltage	V_{OL}	8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	1	-	-	2, 3, 4, 10 11, 12, 13	-	-	14	-	-	7
	V_{OH}	8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	1	-	-	-	2, 3, 4, 10, 11, 12, 13	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 4, 7, 8, 10, 11, 12, 13
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	6.5	-	-	-	-	-	6.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13
Power Supply Drain	I_{PDH}	14	-	10	-	10	-	10	-	10	-	10	-	10	mAdc	-	-	-	-	-	-	-	-	1, 2, 3, 4, 10, 11, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	4.2	-	4.2	-	4.2	-	4.2	-	4.2	-	4.2	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 4, 7, 10, 11, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1, 8	-	-	-	12	-	-	-	-	-	12	-	-	ns	Pulse In 1	Pulse Out 8	-	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 10, 11, 12, 13,	7
Turn-Off Delay	t_{pd+}	1, 8	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	8	-	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 10, 11, 12, 13	7

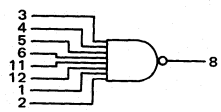
8-INPUT "NAND" GATE

MC3116F • MC3016F
MC3116L • MC3016L,P

(54H30J) (74H30J, N)



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders and decoders.



Positive Logic:

$8 = \overline{3 \bullet 4 \bullet 5 \bullet 6 \bullet 11 \bullet 12 \bullet 1 \bullet 2}$

Negative Logic:

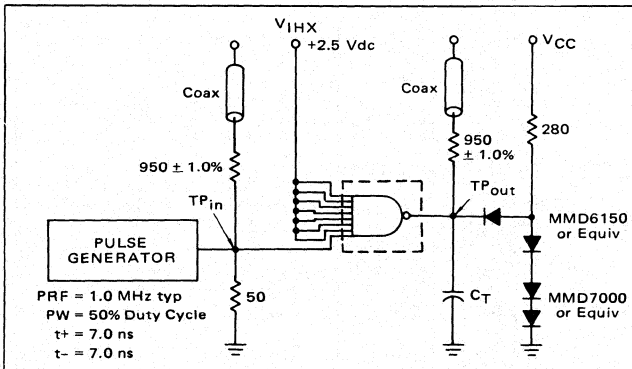
$8 = \overline{3 + 4 + 5 + 6 + 11 + 12 + 1 + 2}$

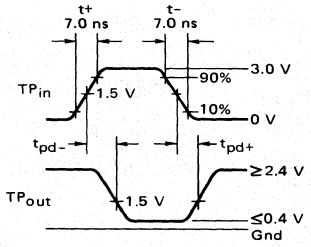
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 22 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

Pin numbers for the 54H30F/74H30F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3116F,L/3016F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H30F/74H30F	9	10	2	3	5	6	11	12	1	14	7	8	13	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





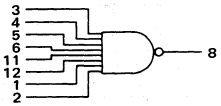
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of this device. To complete testing, sequence through remaining inputs in the same manner.



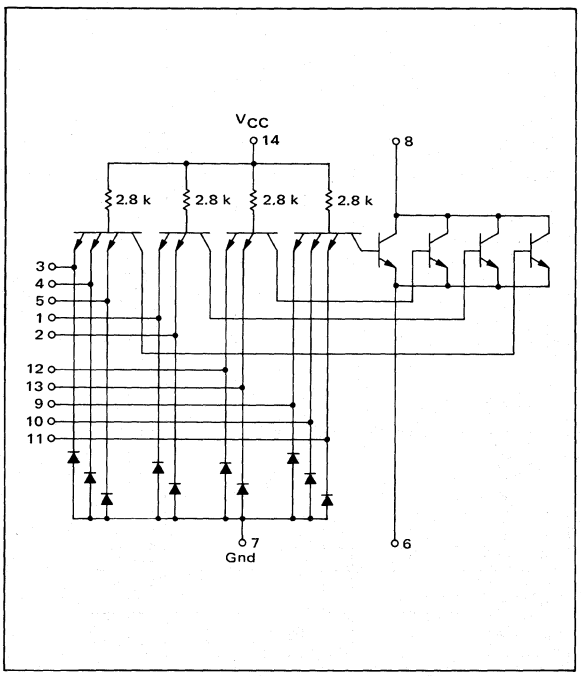
@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
	mA				Volts									
	I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3116 −55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3116 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
MC3116 +125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3016 0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
MC3016 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
MC3016 +75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3116 Test Limits −55°C Min	MC3116 Test Limits −55°C Max	MC3116 Test Limits +25°C Min	MC3116 Test Limits +25°C Max	MC3116 Test Limits +125°C Min	MC3116 Test Limits +125°C Max	MC3016 Test Limits 0°C Min	MC3016 Test Limits 0°C Max	MC3016 Test Limits +25°C Min	MC3016 Test Limits +25°C Max	MC3016 Test Limits +75°C Min	MC3016 Test Limits +75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	3	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	3	-	1, 2, 4, 5, 6, 11, 12	-	-	-	14	-	7
Leakage Current	I_R	3	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	3	-	-	-	-	14	-	1, 2, 4, 5, 6, 7, 11, 12
Breakdown Voltage	BV_{in}	3	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	3	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 6, 7, 11, 12
Clamp Voltage	V_D	3	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	3	-	-	-	-	-	-	-	14	-	-	7
Output Output Voltage	V_{OL}	8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	3	-	-	1, 2, 4, 5 6, 11, 12	-	-	14	-	-	7
	V_{OH}	8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	3	-	-	-	1, 2, 4, 5, 6, 11, 12	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 4, 5, 8, 8, 11, 12
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	6.5	-	-	-	-	-	6.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 4, 5, 7, 11, 12
Power Supply Drain	I_{PDH}	14	-	10	-	10	-	10	-	10	-	10	-	10	mAdc	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 6, 11, 12	-	-	-	14	-	7
	I_{PDL}	14	-	4.2	-	4.2	-	4.2	-	4.2	-	4.2	-	4.2	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 4, 5, 7, 11, 12
Switching Parameters Turn-On Delay	t_{pd-}	3, 8	-	-	-	12	-	-	-	-	-	12	-	-	ns	Pulse In 3	Pulse Out 8	-	-	-	-	-	-	-	-	14	-	-	1, 2, 4, 5, 6, 11, 12	7
Turn-Off Delay	t_{pd+}	3, 8	-	-	-	10	-	-	-	-	-	10	-	-	ns	3	8	-	-	-	-	-	-	-	-	14	-	-	1, 2, 4, 5, 6, 11, 12	7

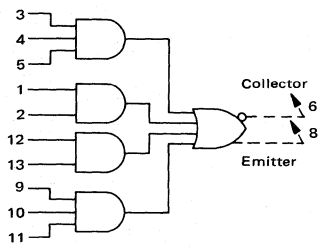
4-WIDE
3-2-2-3 INPUT EXPANDER FOR
"AND-OR-INVERT" GATES

MC3118F • MC3018F
MC3118L • MC3018L,P

(54H62J) **(74H62J,N)**



This expander is designed to expand the AND-OR-INVERT capabilities of the MC3032 and MC3034. One expander can be connected to each expander input of the expandable gate.



Input Loading Factor = 1

Full output loading factor of the expandable gate is maintained.

Total Power Dissipation = 40 mW typ/pkg

Propagation Delay Time:

Δt_{pd1} = +0.4 ns typ

Δt_{pd0} = 0.05 ns typ

When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd1/pF}$ = +0.3 ns/pF typ

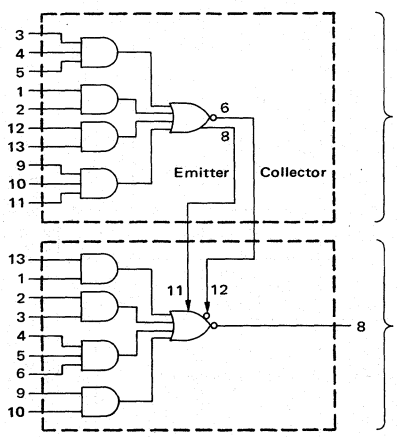
$\Delta t_{pd0/pF}$ = +0.04 ns/pF typ

Caused by additional capacitance at expansion points.

Pin numbers for the 54H62F/74H62F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3118F,L/3018F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H62F/74H62F	2	3	13	14	1	10	11	12	7	8	9	5	6	4

APPLICATION: EXPANDABLE 4-WIDE 2-2-3-2-INPUT AND-OR-INVERT GATE WITH A 4 WIDE 3-2-2-3 INPUT EXPANDER CONNECTED



EXPANDER
MC3018

EXPANDABLE
GATE
MC3032

Positive Logic:

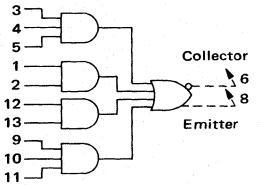
$$8 = \overline{(1 \cdot 13) + (2 \cdot 3) + (4 \cdot 5 \cdot 6) + (9 \cdot 10) + (3 \cdot 4 \cdot 5) + (1 \cdot 2) + (12 \cdot 13) + (9 \cdot 10 \cdot 11)}$$

Expandable Gate — Expander

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES														
		mA			Volts											
		I_{OL}	I_{in}	I_D	V_R	V_{RH}	V_F	V_{EE1}	V_{EE2}	V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
MC3118	−55°C	5.85	-	-	2.4	4.0	0.4	1.0	0.85	2.0	0.8	-	5.0	4.5	5.5	
	+25°C	7.0	1.0	-10	2.4	4.0	0.4	0.85	0.85	1.8	0.8	7.0	5.0	4.5	5.5	
	+125°C	7.85	-	-	2.4	4.0	0.4	0.6	0.85	1.8	0.8	-	5.0	4.5	5.5	
MC3018	0°C	6.3	-	-	2.5	4.0	0.4	1.0	0.85	2.0	0.8	-	5.0	4.75	5.25	
	+25°C	6.7	1.0	-10	2.5	4.0	0.4	0.8	0.85	1.8	0.8	7.0	5.0	4.75	5.25	
	+75°C	7.4	-	-	2.5	4.0	0.4	0.6	0.85	1.8	0.8	-	5.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC3118 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3018 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	I_D	V_R	V_{RH}	V_F	V_{EE1}	V_{EE2}	V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																													
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	2	1	-	-	-	-	-	-	-	14	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	2,7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	-	14	2,7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	7*
Output																													
Output Voltage	V_{OL}**	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	-	8	-	1,2	-	-	14†	14†	14†	7*
Emitter Current	I_{EO}	8	-470	-	-470	-	-470	-	-600	-	-600	-	-600	-	μAdc	-	-	-	-	-	-	8	-	1,2	-	-	-	14	-	7*
Collector Current	I_{CO}††	6	-	320	-	-	-	-	-	570	-	-	-	-	μAdc	-	-	-	-	-	-	-	-	-	1,3,9, 12	-	-	6,14	-	7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	8.0	-	-	-	-	-	8.0	-	-	mAdc	-	-	-	-	-	-	-	8	-	-	14	-	-	-	1,2,3,4,5,7 9,10,12,13
	I_{PDH}	14	-	7.0	-	7.0	-	7.0	-	7.0	-	7.0	-	7.0	mAdc	-	-	-	-	1,2,3,4,5, 9,10,12,13	-	-	8	-	-	-	-	-	14	7
Power Supply Drain	I_{PDL}	14	-	9.0	-	9.0	-	9.0	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	8	-	-	-	-	-	14	1,2,3,4,5,7 9,10,12,13

*Ground inputs to gates not under test.
† Apply to pin 14: @ Low temp. V_{CCL}, @ 25°C V_{CC}, @ Hi temp V_{CCH}

†† Connect 575 Ω resistor from Pin 8 to ground.

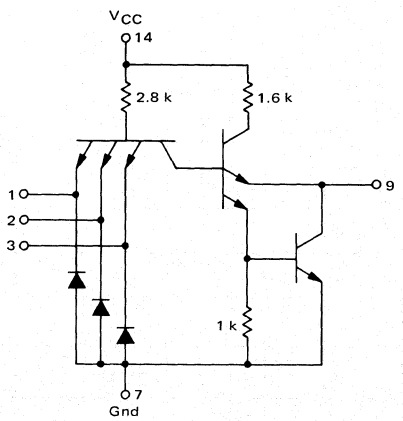
**This test is a measure of potential difference between pins 6 & 8.

TRIPLE 3-INPUT EXPANDER FOR "AND-OR" GATES

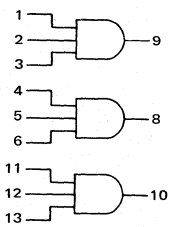
MC3119F • MC3019F
MC3119L • MC3019L,P

(54H61J) (74H61J, N)

1/3 OF CIRCUIT SHOWN



This device consists of three independent 3-input AND gates. The outputs of each gate are available as ORing nodes. Using the MC3019 expander, with the MC3031 expandable gate, up to six AND gates can be ORed together.



Input Loading Factor = 1
Full output loading factor of the expandable gate is maintained.

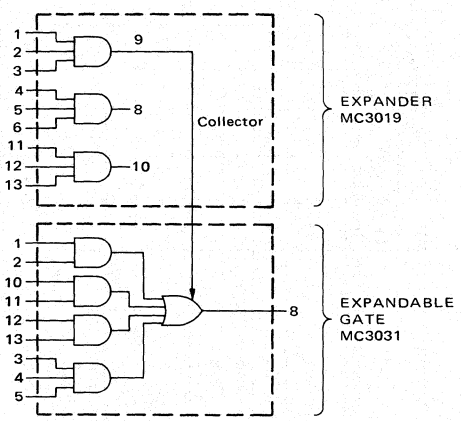
Total Power Dissipation = 25 mW typ/pkg
Propagation Delay Time:
Δt_{pd1} = +0.4 ns typ
Δt_{pd0} = +0.05 ns typ
When added to the expandable "AND-OR" gate.

Δt_{pd1}/pF = +0.3 ns/pF typ
Δt_{pd0}/pF = +0.04 ns/pF typ
Caused by additional capacitance at expansion points.

Pin numbers for the 54H61F/74H61F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3119F,L/3019F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H61F/74H61F	1	2	3	5	6	7	11	13	14	12	8	9	10	4

APPLICATION: EXPANDABLE 4-WIDE 2-2-2-3-INPUT AND-OR GATE WITH A TRIPLE 3-INPUT EXPANDER CONNECTED



Positive Logic:

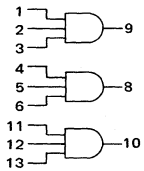
$8 = (1 \bullet 2) + (3 \bullet 4 \bullet 5) + (10 \bullet 11) + (12 \bullet 13) + (1 \bullet 2 \bullet 3)$

Expandable Gate — Expander

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{in}	I_D	Volts V_R	V_{RH}	V_F	V_{CEX}	V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
MC3119	−55°C	4.5	-	-	2.4	4.0	0.4	2.2	2.0	0.8	-	5.0	4.5	5.5
MC3119	+25°C	5.5	1.0	-10	2.4	4.0	0.4	2.2	1.8	0.8	7.0	5.0	4.5	5.5
MC3119	+125°C	7.3	-	-	2.4	4.0	0.4	2.2	1.8	0.8	-	5.0	4.5	5.5
MC3019	0°C	5.35	-	-	2.5	4.0	0.4	2.2	2.0	0.8	-	5.0	4.75	5.25
MC3019	+25°C	5.5	1.0	-10	2.5	4.0	0.4	2.2	1.8	0.8	7.0	5.0	4.75	5.25
MC3019	+75°C	6.2	-	-	2.5	4.0	0.4	2.2	1.8	0.8	-	5.0	4.75	5.25

Characteristics	Symbol	Pin Under Test	MC3119 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3019 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	I_D	V_R	V_{RH}	V_F	V_{CEX}	V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																												
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	2,3	1	-	-	-	-	-	-	14	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	1	-	-	-	-	-	-	-	-	14	2,3,7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	14	2,3,7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	7*
Output																												
Output Voltage	V_{OL}	9	-	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	1.0	Vdc	9	-	-	-	-	-	-	1,2,3	-	-	-	14	-	7*
Emitter Current	I_{CEX}	9	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	2,3	-	9	-	1	-	-	14	-	7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	9.0	-	-	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,3,4,5, 6,7,11,12,13
	I_{PDH}	14	-	18	-	18	-	18	-	18	-	18	-	18	mAdc	-	-	-	-	1,2,3,4,5,6, 11,12,13	-	-	-	-	-	-	-	14	7
Power Supply Drain	I_{PDL}	14	-	6.75	-	6.75	-	6.75	-	6.75	-	6.75	-	6.75	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5, 6,7,11,12,13

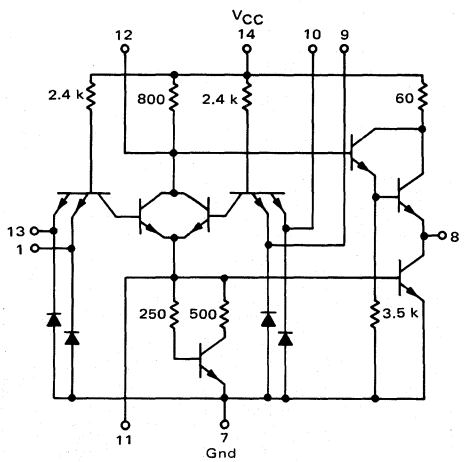
*Ground inputs to gates not under test.

EXPANDABLE DUAL
2-WIDE 2-INPUT
"AND-OR-INVERT" GATE

MC3120F • MC3020F
MC3120L • MC3020L,P

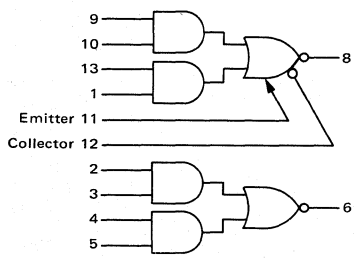
(54H50J) (74H50J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN†



†Other half of circuit omits expander inputs.

One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together, driving an output inverter, and the ORing nodes are available for expansion. Up to four AND gates can be ORed together using the MC3030/3130 expander. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

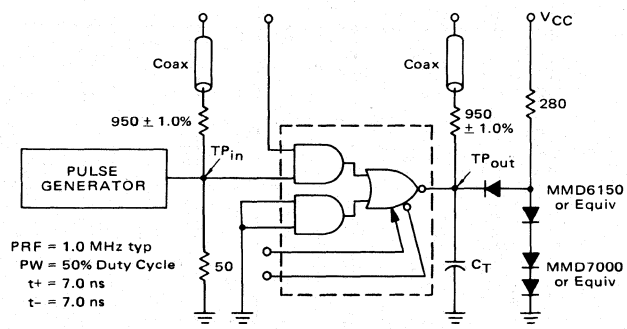
$$8 = \overline{(9 \bullet 10) + (13 \bullet 1) + (\text{Expanders})}$$

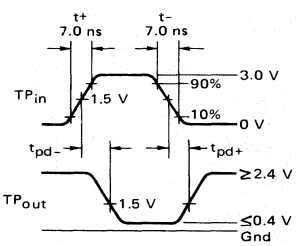
Negative Logic:

$$8 = \overline{(9 + 10) \bullet (13 + 1) \bullet (\text{Expanders})}$$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 62.5 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





Expander pins should be left open when measuring switching times.

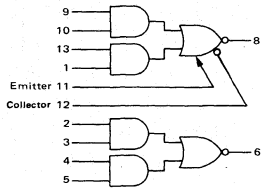
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



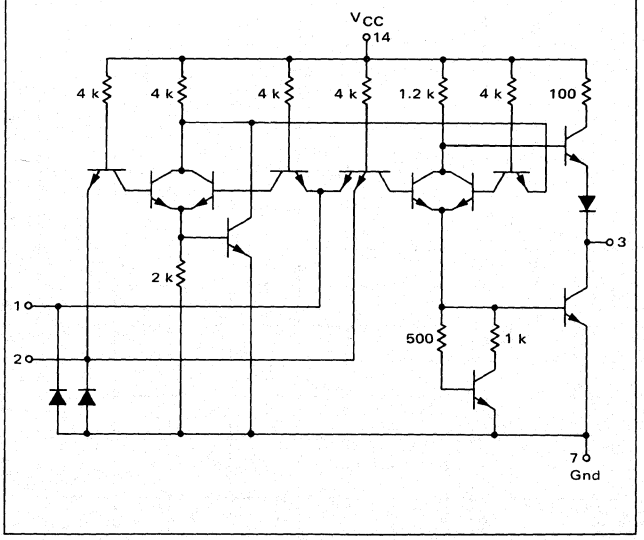
	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES																
		mA						Volts										
		I_{OL}	I_{OH}	I_{in}	I_D	I_E	I_{EXE}	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
MC3120	−55°C	20	-2.0	-	-	0.3	0.55	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-	
	+25°C	20	-2.0	1.0	-10	0.3	0.71	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5	
	+125°C	20	-2.0	-	-	0.3	0.92	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-	
MC3020	0°C	20	-2.0	-	-	0.3	0.65	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-	
	+25°C	20	-2.0	1.0	-10	0.3	0.71	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5	
	+75°C	20	-2.0	-	-	0.3	0.82	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-	

Characteristic	Symbol	Pin Under Test	MC3120 Test Limits −55°C Min	MC3120 Test Limits −55°C Max	MC3120 Test Limits +25°C Min	MC3120 Test Limits +25°C Max	MC3120 Test Limits +125°C Min	MC3120 Test Limits +125°C Max	MC3020 Test Limits 0°C Min	MC3020 Test Limits 0°C Max	MC3020 Test Limits +25°C Min	MC3020 Test Limits +25°C Max	MC3020 Test Limits +75°C Min	MC3020 Test Limits +75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	I_E	I_{EXE}	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	-	-	1	-	13	-	-	-	14	-	7, 9, 10*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	7, 9, 10, 13*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	-	-	14	-	7, 9, 10, 13*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	-	14	-	-	7, 9, 10*
Output Output Voltage	V_{OL}	8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	-	1	-	-	13	-	-	-	14	-	-	7, 9, 10*
	V_{OL}	8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	11, 12	-	-	-	-	-	-	-	-	14	-	-	1,7,9,10,13
	V_{OH}	8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	-	1	-	-	-	13	-	-	-	14	-	-	1, 7, 10*
Short-Circuit Current	I_{SC}	8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 7, 8, 9, 10, 13*
Base-Emitter Voltage	$V_{BE\ max}$	11	-	1.10	-	-	-	-	-	1.00	-	-	-	-	Vdc	8	-	-	-	-	11, 12	-	-	-	-	-	-	-	14	-	-	1, 9, 10, 13*
	$V_{BE\ min}$	11	0.80	-	0.65	-	0.45	-	0.70	-	0.65	-	0.55	-	Vdc	-	-	-	-	11	-	-	-	-	-	-	-	-	14	-	-	1, 9, 10, 12, 13*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	24	-	-	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 4, 5, 7, 9, 10, 13
Power Supply Drain	I_{PDH}	14	-	24	-	24	-	24	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 13	-	-	-	14	-	7
	I_{PDL}	14	-	12.8	-	12.8	-	12.8	-	12.8	-	12.8	-	12.8	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 4, 5, 7, 9, 10, 13
Switching Parameters Turn-On Delay	t_{pd-}	1, 8	-	-	-	11	-	-	-	-	-	11	-	-	ns	Pulse In: 1	Pulse Out: 8	-	-	-	-	-	-	-	-	-	-	14	-	-	13	7, 9, 10*
Turn-Off Delay	t_{pd+}	1, 8	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	8	-	-	-	-	-	-	-	-	-	-	14	-	-	13	7, 9, 10*

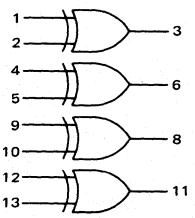
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

MC3121F • MC3021F
MC3121L • MC3021L,P

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



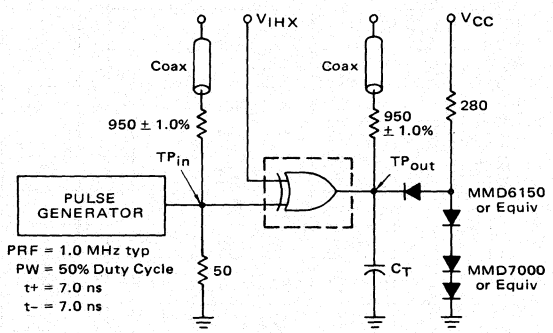
This device consists of four 2-input Exclusive OR gates. They can be used to build parity checking/generating functions. Up/down counters can be built using these gates and J-K flip-flops.

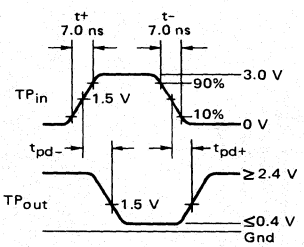


Positive Logic: $3 = 1 \bullet \overline{2} + \overline{1} \bullet 2$

Input Loading Factor = 1.6
Output Loading Factor = 8
Total Power Dissipation = 100 mW typ/pkg
Propagation Delay Time = 14 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





One input to gates not under test must be tied to V_{IHX} the other grounded.

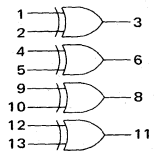
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test proceduresare shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



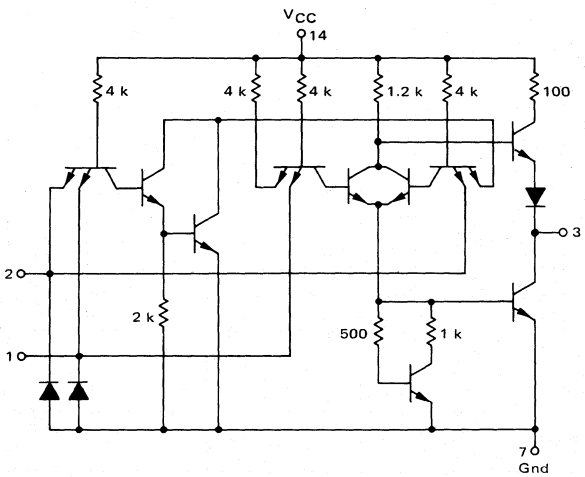
@ Test Temperature		TEST CURRENT/VOLTAGE VALUES														
		mA				Volts										
		I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	V_{max}
MC3121	−55°C	16	-1.6	-	-	1.1	2.0	0.4	2.4	4.0	5.0	4.5	5.5	-	-
	+25°C	16	-1.6	1.0	1.0	1.1	1.8	0.4	2.4	4.0	5.0	4.5	5.5	2.5	7.0
	+125°C	16	-1.6	-	-	0.8	1.8	0.4	2.4	4.0	5.0	4.5	5.5	-	-
MC3021	0°C	16	-1.6	-	-	1.1	2.0	0.4	2.5	4.0	5.0	4.75	5.25	-	-
	+25°C	16	-1.6	1.0	1.0	1.1	1.8	0.4	2.5	4.0	5.0	4.75	5.25	2.5	7.0
	+75°C	16	-1.6	-	-	0.9	1.8	0.4	2.5	4.0	5.0	4.75	5.25	-	-

Characteristic	Symbol	Pin Under Test	MC3121 Test Limits							MC3021 Test Limits							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C														
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	V_{max}	Gnd
Input																														
Forward Current	I_F	1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	1	-	2,5,10,13	-	-	14	-	-	4,7,9,12
Leakage Current	I_R	1	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	5,10,13	-	-	14	-	-	2,4,7,9,12
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	5,10,13	-	-	14	-	-	2,4,7,9,12
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	5,10,13	-	14	-	-	-	4,7,9,12
Output																														
Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	Vdc	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	1,2	-	-	-	5,10,13	-	14	-	-	-	4,7,9,12
		3	-	0.4	-	0.4	-	0.4	Vdc	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	1,2	-	-	5,10,13	-	14	-	-	-	4,7,9,12
	V_{OH}	3	2.4	-	2.4	-	2.4	-	Vdc	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	1	2	-	-	5,10,13	-	14	-	-	-	4,7,9,12
		3	2.4	-	2.4	-	2.4	-	Vdc	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	2	1	-	-	5,10,13	-	14	-	-	-	4,7,9,12
Short-Circuit Current	I_{SC}	3	-20	-65	-20	-65	-20	-65	mAdc	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	1	-	2,5,10,13	-	-	14	-	-	3,4,7,9,12
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	35	-	-	mAdc	-	-	-	40	-	-	mAdc	-	-	-	-	-	-	1,4,9,12	-	2,5,10,13	-	-	-	-	14	7
Power Supply Drain	I_{PDH}	14	-	28.6	-	28.6	-	28.6	mAdc	-	28.6	-	28.6	-	28.6	mAdc	-	-	-	-	-	-	1,4,9,12	-	2,5,10,13	-	-	14	-	-	7
	I_{PDL}	14	-	42.4	-	42.4	-	42.4	mAdc	-	42.4	-	42.4	-	42.4	mAdc	-	-	-	-	-	-	1,2,4,5	-	-	-	-	14	-	-	7
Switching Parameters																														
Turn-On Delay	t_{pd-}	1,3	-	-	-	25	-	-	ns	-	-	-	25	-	-	ns	1	-	-	-	-	-	-	-	-	14	-	-	2,5,10,13	-	4,7,9,12
Turn-Off Delay	t_{pd+}	1,3	-	-	-	25	-	-	ns	-	-	-	25	-	-	ns	1	-	-	-	-	-	-	-	-	14	-	-	2,5,10,13	-	4,7,9,12

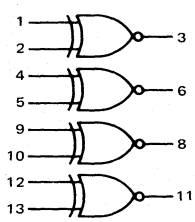
Pins not listed are left open.

MC3122F • MC3022F
MC3122L • MC3022L,P

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



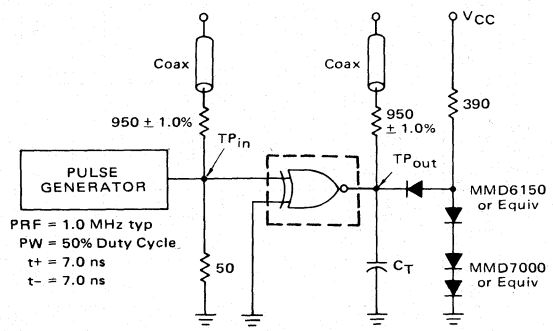
This device consists of four 2-input Exclusive NOR gates. They can be used to build parity checking/generating functions. Up/down counters can be built using these gates and J-K flip-flops.

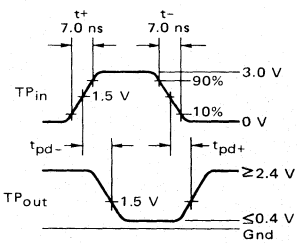


Positive Logic: $3 = \overline{1} \bullet \overline{2} + 1 \bullet 2$

Input Loading Factor = 1.6
Output Loading Factor = 8
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 14 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





Ground inputs of gates not under test.

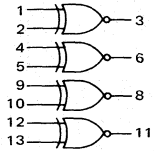
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test proceduresare shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES												
	mA				Volts								
	I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC3122 −55°C	16	-1.6	-	-	1.1	2.0	0.4	2.4	4.0	5.0	4.5	5.5	-
MC3122 +25°C	16	-1.6	2.0	-10	1.1	1.8	0.4	2.4	4.0	5.0	4.5	5.5	7.0
MC3122 +125°C	16	-1.6	-	-	0.8	1.8	0.4	2.4	4.0	5.0	4.5	5.5	-
MC3022 0°C	16	-1.6	-	-	1.1	2.0	0.4	2.5	4.0	5.0	4.75	5.25	-
MC3022 +25°C	16	-1.6	2.0	-10	1.1	1.8	0.4	2.5	4.0	5.0	4.75	5.25	7.0
MC3022 +75°C	16	-1.6	-	-	0.9	1.8	0.4	2.5	4.0	5.0	4.75	5.25	-

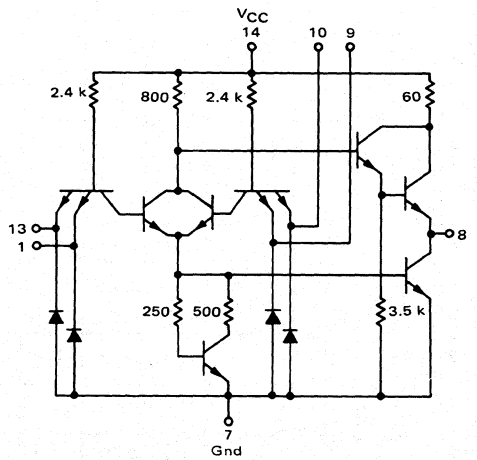
Characteristic	Symbol	Pin Under Test	MC3122 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC3022 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Input																														
Forward Current	I_F	1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	1	-	2	-	-	14	-	4,5,7,9,10,12,13
Leakage Current	I_R	1	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	-	-	-	14	-	2,4,5,7,9,10,12,13
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	2,4,5,7,9,10,12,13
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	14	-	-	4,5,7,9,10,12,13
Output																														
Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	Vdc	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	1	2	-	-	-	-	14	-	-	4,5,7,9,10,12,13
		3	-	0.4	-	0.4	-	0.4	Vdc	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	2	1	-	-	-	-	14	-	-	4,5,7,9,10,12,13
	V_{OH}	3	2.4	-	2.4	-	2.4	-	Vdc	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	1,2	-	-	-	-	-	14	-	-	4,5,7,9,10,12,13
		3	2.4	-	2.4	-	2.4	-	Vdc	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	-	1,2	-	-	-	-	14	-	-	4,5,7,9,10,12,13
Short-Circuit Current	I_{SC}	3	-20	-65	-20	-65	-20	-65	mAdc	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	1,2	-	-	-	-	14	-	3,4,5,7,9,10,12,13
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	24.8	-	-	mAdc	-	-	-	24.8	-	-	mAdc	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	-	-	-	-	-	14	7
Power Supply Drain	I_{PDH}	14	-	34.4	-	34.4	-	34.4	mAdc	-	34.4	-	34.4	-	34.4	mAdc	-	-	-	-	-	-	2,5,10,13	-	1,4,9,12,	-	-	14	-	7
	I_{PDL}	14	-	17.8	-	17.8	-	17.8	mAdc	-	17.8	-	17.8	-	17.8	mAdc	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	-	-	-	-	14	-	7
Switching Parameters																														
Turn-On Delay	t_{pd-}	1,3	-	-	-	22	-	-	ns	-	-	-	22	-	-	ns	1	-	-	-	-	-	-	-	-	14	-	-	-	2,4,5,7,9,10,12,13
Turn-Off Delay	t_{pd+}	1,3	-	-	-	22	-	-	ns	-	-	-	22	-	-	ns	1	-	-	-	-	-	-	-	-	14	-	-	-	2,4,5,7,9,10,12,13

Pins not listed are left open.

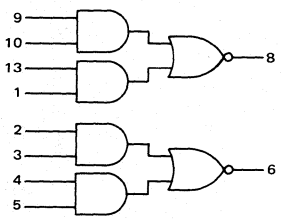
MC3123F • MC3023F
MC3123L • MC3023L,P

(54H51J) (74H51J, N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This dual device consists of two 2-input AND gates ORed together and driving an output inverter.



Positive Logic:

$$8 = \overline{(9 \cdot 10) + (13 \cdot 1)}$$

Negative Logic:

$$8 = \overline{(9 + 10) \cdot (13 + 1)}$$

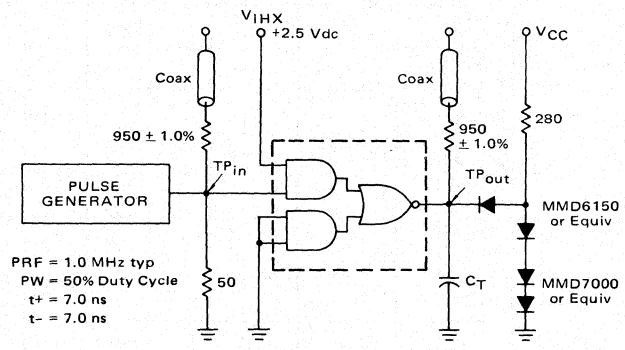
Input Loading Factor = 1
Output Loading Factor = 10

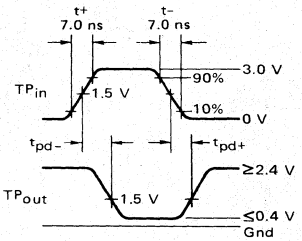
Total Power Dissipation = 62.5 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

Pin numbers for the 54H51F/74H51F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3123F,L/3023F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H51F/74H51F	5	6	7	8	9	10	11	12	13	14	1	2	3	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





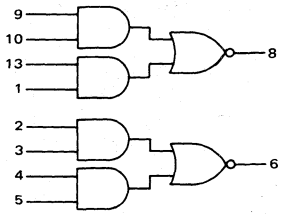
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	MC3123 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3023 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	13	-	-	-	14	-	7, 9, 10 *
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	-	7, 9, 10, 13 *
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	7, 9, 10, 13 *
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7, 9, 10 *
Output Output Voltage	V_{OL}	8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	1	-	-	13	-	-	14	-	-	7, 9, 10 *
	V_{OH}	8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	1	-	-	-	13	-	-	14	-	-	1, 7, 10 *
Short-Circuit Current	I_{SC}	8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 7, 8, 9, 10, 13 *
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	20	-	-	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7, 9,10, 13
Power Supply Drain	I_{PDH}	14	-	24	-	24	-	24	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 13	-	-	-	14	-	7
	I_{PDL}	14	-	12.8	-	12.8	-	12.8	-	12.8	-	12.8	-	12.8	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5,7, 9,10,13
Switching Parameters Turn-On Delay	t_{pd-}	1, 8	-	-	-	11	-	-	-	-	-	11	-	-	ns	Pulse In 1	Pulse Out 8	-	-	-	-	-	-	-	-	14	-	-	13	7, 9, 10 *
Turn-Off Delay	t_{pd+}	1, 8	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	8	-	-	-	-	-	-	-	-	14	-	-	13	7, 9, 10 *

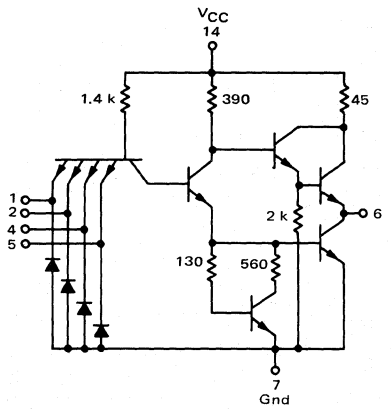
@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3123 −55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3123 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
MC3123 +125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3023 0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
MC3023 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
MC3023 +75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

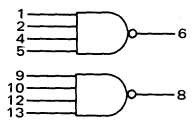
MC3124F • MC3024F
MC3124L • MC3024L,P

(54H40J) (74H40J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (30).



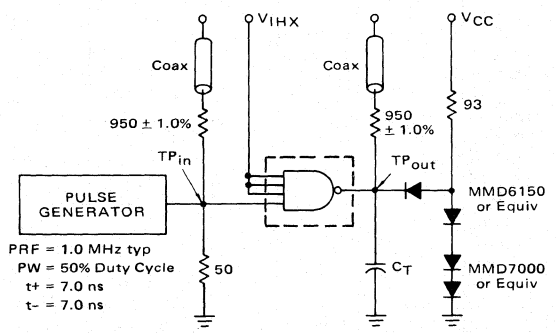
Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$
Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

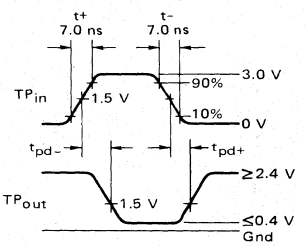
Input Loading Factor = 2
Output Loading Factor = 30
Total Power Dissipation = 90 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

Pin numbers for the 54H40F/74H40F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS												
MC3124F,L/3024F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H40F/74H40F	1	12	3	13	14	2	11	10	6	7	5	8	9	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





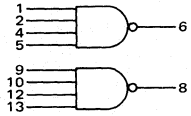
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature		I_{OL} mA	I_{OH} mA	I_{in} mA	I_D mA	V_{IL} Volts	V_{IH} Volts	V_F Volts	V_R Volts	V_{RH} Volts	V_{max} Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts	V_{IHX} Volts
MC3124	−55°C	60	-1.5	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	+25°C	60	-1.5	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.4
	+125°C	60	-1.5	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3024	0°C	60	-1.5	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	+25°C	60	-1.5	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	+75°C	60	-1.5	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

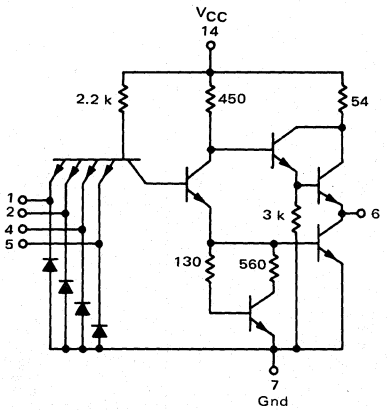
Characteristic	Symbol	Pin Under Test	MC3124 Test Limits −55°C Min	MC3124 Test Limits −55°C Max	MC3124 Test Limits +25°C Min	MC3124 Test Limits +25°C Max	MC3124 Test Limits +125°C Min	MC3124 Test Limits +125°C Max	MC3024 Test Limits 0°C Min	MC3024 Test Limits 0°C Max	MC3024 Test Limits +25°C Min	MC3024 Test Limits +25°C Max	MC3024 Test Limits +75°C Min	MC3024 Test Limits +75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0	mAdc	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 4, 5, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	14	-	7*
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	1.2,4,5	-	-	-	-	-	-	14	-	7*
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	1	-	-	-	2, 4, 5	-	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-	-	-40	-135	-	-	-	-	-40	-125	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,4,5,6,7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	22	-	-	-	-	-	22	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	40	-	40	-	40	-	40	-	40	-	40	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	16	-	16	-	16	-	16	-	16	-	16	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7 9, 10, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1,6	-	-	-	12	-	-	-	-	-	12	-	-	ns	Pulse In 1	Pulse Out 6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*
Turn-Off Delay	t_{pd+}	1,6	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

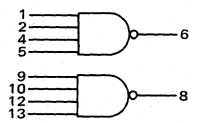
DUAL 4-INPUT "NAND" POWER GATE

MC3125F • MC3025F
MC3125L • MC3025L,P

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (20).

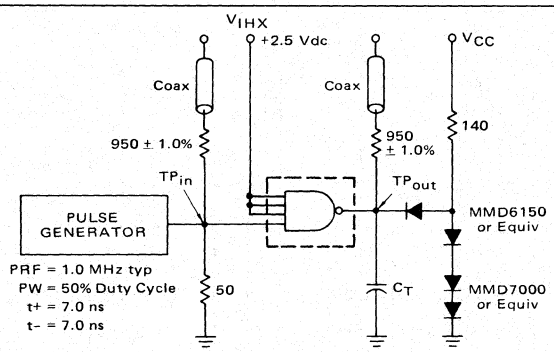


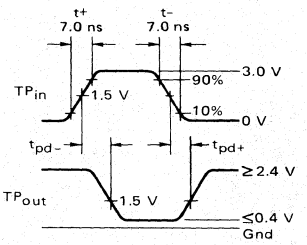
Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

Input Loading Factor = 1.3
Output Loading Factor = 20
Total Power Dissipation = 70 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





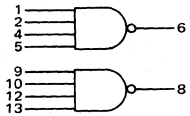
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



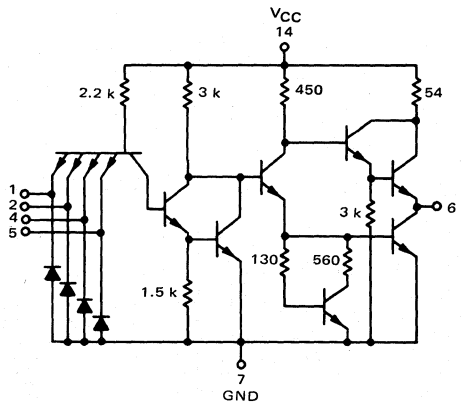
@ Test Temperature		I_{OL} mA	I_{OH} mA	I_{in} mA	I_D mA	V_{IL} Volts	V_{IH} Volts	V_F Volts	V_R Volts	V_{RH} Volts	V_{max} Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts	V_{IHX} Volts
MC3125	−55°C	40	-4.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	+25°C	40	-4.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
	+125°C	40	-4.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3025	0°C	40	-4.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	+25°C	40	-4.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	+75°C	40	-4.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3125 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3025 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.6	-	-2.6	-	-2.6	-	-2.6	-	-2.6	-	-2.6	mAdc	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 4, 5, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	1	-	-	2, 4, 5	-	-	14	-	-	7*
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	1	-	-	-	2, 4, 5	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-50	-125	-50	-125	-50	-125	-50	-125	-50	-125	-50	-125	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,4,5,6,7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	16	-	-	-	-	-	16	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	34	-	34	-	34	-	34	-	34	-	34	mAdc	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	10.6	-	10.6	-	10.6	-	10.6	-	10.6	-	10.6	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7 9, 10, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1,6	-	-	-	12	-	-	-	-	-	12	-	-	ns	Pulse In 1	Pulse Out 6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*
Turn-Off Delay	t_{pd+}	1,6	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

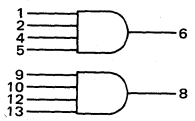
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

MC3126F • MC3026F
MC3126L • MC3026L,P

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



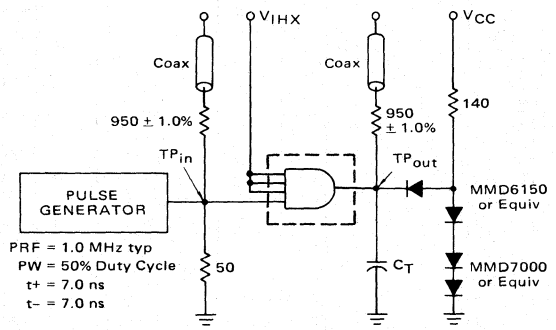
This device consists of two 4-input AND power gates. Each gate is designed for driving high fan-out loads (20).

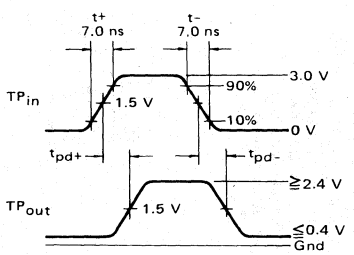


Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$
Negative Logic: $6 = 1 + 2 + 4 + 5$

Input Loading Factor = 1.3
Output Loading Factor = 20
Total Power Dissipation = 90 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





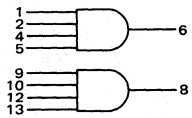
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



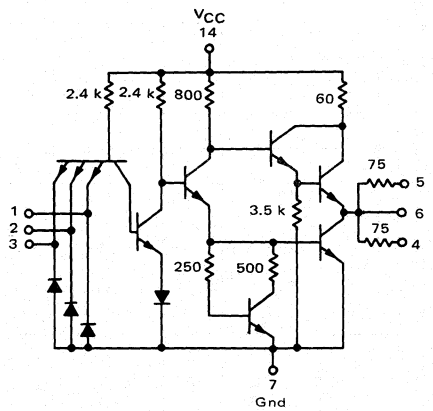
Characteristic	Symbol	Pin Under Test	MC3126 Test Limits −55°C Min	MC3126 Test Limits −55°C Max	MC3126 Test Limits +25°C Min	MC3126 Test Limits +25°C Max	MC3126 Test Limits +125°C Min	MC3126 Test Limits +125°C Max	MC3026 Test Limits 0°C Min	MC3026 Test Limits 0°C Max	MC3026 Test Limits +25°C Min	MC3026 Test Limits +25°C Max	MC3026 Test Limits +75°C Min	MC3026 Test Limits +75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES: @ Test Temperature	mA: I_{OL}	mA: I_{OH}	mA: I_{in}	mA: I_D	Volts: V_{IL}	Volts: V_{IH}	Volts: V_F	Volts: V_R	Volts: V_{RH}	Volts: V_{max}	Volts: V_{CC}	Volts: V_{CCL}	Volts: V_{CCH}	Volts: V_{IHX}
																MC3126 −55°C	40	-4.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
																MC3126 +25°C	40	-4.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
																MC3126 +125°C	40	-4.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
																MC3026 0°C	40	-4.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
																MC3026 +25°C	40	-4.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
																MC3026 +75°C	40	-4.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-
																TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:	I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																														
Forward Current	I_F	1	-	-2.6	-	-2.6	-	-2.6	-	-2.6	-	-2.6	-	-2.6	mAdc		-	-	-	-	-	-	1	-	2, 4, 5 *	-	-	-	14	-	7
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc		-	-	-	-	-	-	-	1	*	-	-	-	14	-	2, 4, 5, 7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc		-	-	1	-	-	-	-	-	*	-	-	-	14	-	2, 4, 5, 7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc		-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc		6	-	-	-	1	-	-	-	2, 4, 5 *	-	-	14	-	-	7
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc		-	-	-	-	-	1	-	-	2, 4, 5 *	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-50	-125	-50	-125	-50	-125	-50	-125	-50	-125	-50	-125	mAdc		-	6	-	-	-	-	-	-	1, 2, 4, 5 *		-	-	14	-	6, 7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	22	-	-	-	-	-	22	-	-	mAdc		-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	14	-	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	15	-	15	-	15	-	15	-	15	-	15	mAdc		-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	40	-	40	-	40	-	40	-	40	-	40	mAdc		-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1, 6	-	-	-	15	-	-	-	-	-	15	-	-	ns		Pulse In: 1	Pulse Out: 6	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	15	-	-	-	-	-	15	-	-	ns		1	6	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7

*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

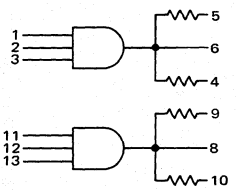
DUAL 3-INPUT 3-OUTPUT
"AND" SERIES TERMINATED
LINE DRIVER

MC3128F • MC3028F
MC3128L • MC3028L,P

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device is a dual 3-input/3-output series-terminated AND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6, = 1 • 2 • 3
Negative Logic: 4, 5, 6, = 1 + 2 + 3

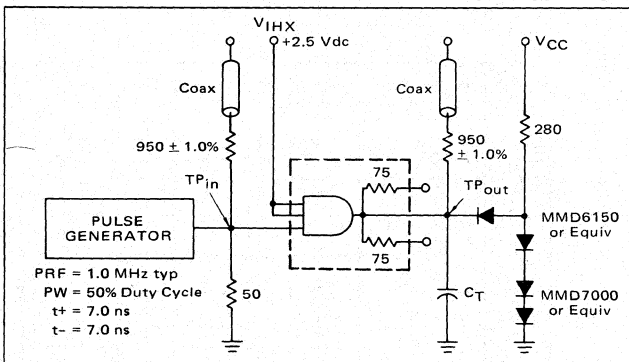
Input Loading Factor = 1

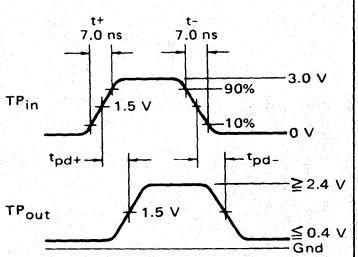
Output Loading Factor, Direct Output (Pins 6 & 8) = 8 minus the number of resistor-terminated outputs being used.

Output Loading Factor, Resistors (Pins 4, 5, 9, & 10) = 1

Total Power Dissipation = 56 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





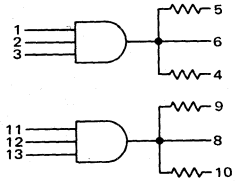
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procedures are shown for only one input of the line driver being tested. To complete testing, sequence through remaining inputs.



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES																		
		mA								Volts										
		$I_{OL\,A}$	$I_{OL\,B}$	$I_{OL\,C}$	$I_{OH\,A}$	$I_{OH\,B}$	$I_{OH\,C}$	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3128	−55°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	+25°C	16	2.0	2.0	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
	+125°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3028	0°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	+25°C	16	2.0	2.0	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	+75°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

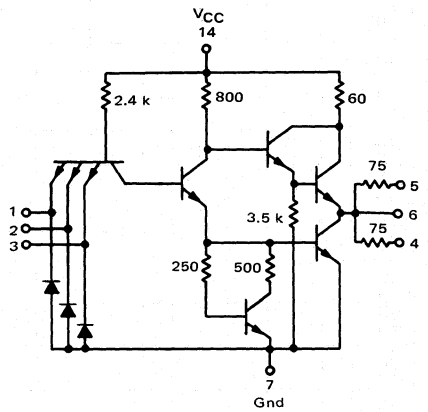
Characteristic	Symbol	Pin Under Test	MC3128 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3028 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{OL\,A}$	$I_{OL\,B}$	$I_{OL\,C}$	$I_{OH\,A}$	$I_{OH\,B}$	$I_{OH\,C}$	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	$I_{F\,2}$	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	-	-	-	-	1	-	2, 3*	-	-	-	14	-	7
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2, 3, 7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2, 3, 7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output Output Voltage	$V_{OL\,1}$	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	5	4	-	-	-	-	-	1	-	-	-	2, 3*	-	-	14	-	-	7
	$V_{OL\,2}$	5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	Vdc	6	5	4	-	-	-	-	-	1	-	-	-	2, 3*	-	-	14	-	-	7
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	-	-	6	5	4	-	-	-	1	-	-	2, 3*	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3*	-	-	-	14	-	6, 7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	18	-	-	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	14	-	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	13.2	-	13.2	-	13.2	-	13.2	-	13.2	-	13.2	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	26.4	-	26.4	-	26.4	-	26.4	-	26.4	-	26.4	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 7 11, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1, 6	-	-	-	15	-	-	-	-	-	15	-	-	ns	Pulse In 1	Pulse Out 6	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2, 3	7
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2, 3	7

*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

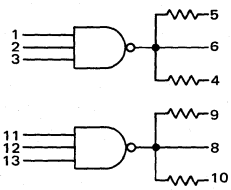
DUAL 3-INPUT 3-OUTPUT
"NAND" SERIES TERMINATED
LINE DRIVER

MC3129F • MC3029F
MC3129L • MC3029L,P

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device is a dual 3-input/3-output series-terminated NAND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6 = $\overline{1 \cdot 2 \cdot 3}$

Negative Logic: 4, 5, 6 = $\overline{1 + 2 + 3}$

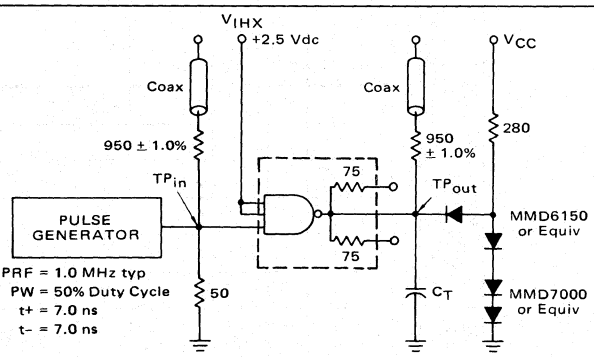
Input Loading Factor = 1

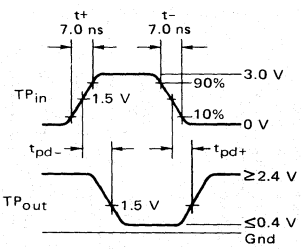
Output Loading Factor, Direct Output (Pins 6 and 8) = 8 Minus The Number of Resistor-Terminated Outputs Being Used.

Output Loading Factor, Resistors (Pins 4, 5, 9 and 10) = 1

Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





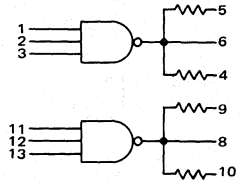
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line driver The other line driver is tested in the same manner. Further, test procecures are shown for only one input of the line driver under test. To complete testing sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES																			
		mA								Volts											
		$I_{OL\,A}$	$I_{OL\,B}$	$I_{OL\,C}$	$I_{OH\,A}$	$I_{OH\,B}$	$I_{OH\,C}$	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{INX}		
MC3129	−55°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-		
	+25°C	16	2.0	2.0	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5		
	+125°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-		
MC3029	0°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-		
	+25°C	16	2.0	2.0	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5		
	+75°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-		

Characteristic	Symbol	Pin Under Test	MC3129 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3029 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{OL\,A}$	$I_{OL\,B}$	$I_{OL\,C}$	$I_{OH\,A}$	$I_{OH\,B}$	$I_{OH\,C}$	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{INX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	-	-	-	-	1	-	2, 3	-	-	-	14	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 3, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 3, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	$V_{OL\,1}$	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	5	4	-	-	-	-	-	-	1	-	-	2, 3	-	-	14	-	-	7*
	$V_{OL\,2}$	5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	Vdc	6	5	4	-	-	-	-	-	-	1	-	-	2, 3	-	-	14	-	-	7*
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	-	-	6	4	5	-	-	1	-	-	-	2, 3	-	-	14	-	-	7*
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100		-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 6, 7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	12	-	-	-	-	-	12	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 7, 11, 12, 13
Power Supply Drain	I_{PDH}	14	-	19	-	19	-	19	-	19	-	19	-	19	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	9.6	-	9.6	-	9.6	-	9.6	-	9.6	-	9.6	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 7, 11, 12, 13
Switching Parameters																Pulse In	Pulse Out																	
Turn-On Delay	t_{pd-}	1, 6	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	2, 3	7*
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	2, 3	7*

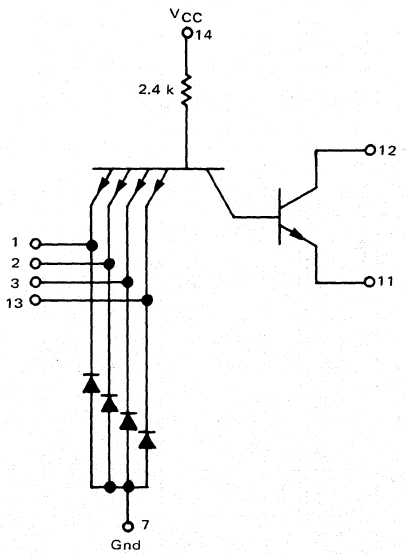
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

DUAL 4-INPUT EXPANDER
FOR "AND-OR-INVERT" GATES

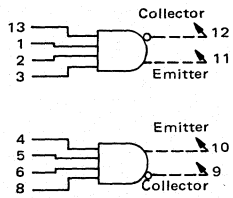
MC3130F • MC3030F
MC3130L • MC3030L,P

(54H60J) (74H60J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device consists of two independent 4-input AND gates. The outputs of each gate are available as ORing nodes. Using the MC3030/3130 expander, with the MC3020/3120 expandable gate, up to four AND gates can be ORed together.



Input Loading Factor = 1
Full output loading factor of the expandable gate is maintained.

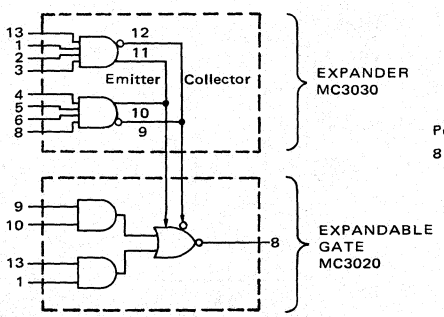
Total Power Dissipation = 15 mW typ/pkg

Propagation Delay Time:

Δt_{pd} = +1.0 ns typ
When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd}/pF$ = +1.0 ns pF typ
Caused by additional capacitance at expansion points.

APPLICATION: EXPANDABLE 2-WIDE 2-INPUT AND-OR-INVERT GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED



Positive Logic:

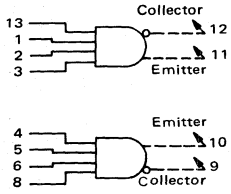
$$8 = \overline{(9 \bullet 10) + (13 \bullet 1)} + \overline{(13 \bullet 1 \bullet 2 \bullet 3) + (4 \bullet 5 \bullet 6 \bullet 8)}$$

Expandable Gate — Expander

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES: mA I_C	I_{in}	I_D	Volts V_R	V_{RH}	V_F	V_{EE1}	V_{EE2}	V_{IH}	V_{IL}	V_{max}	V_{CCL}	V_{CCH}
MC3130 −55°C	6.0	-	-	2.4	4.0	0.4	1.10	0.80	2.0	1.1	-	4.5	5.5
MC3130 +25°C	6.0	1.0	-10	2.4	4.0	0.4	0.95	0.65	1.8	1.1	7.0	4.5	5.5
MC3130 +125°C	6.0	-	-	2.4	4.0	0.4	0.75	0.45	1.8	0.8	-	4.5	5.5
MC3030 0°C	6.0	-	-	2.5	4.0	0.4	1.00	0.70	2.0	1.1	-	4.75	5.25
MC3030 +25°C	6.0	1.0	-10	2.5	4.0	0.4	0.95	0.65	1.8	1.1	7.0	4.75	5.25
MC3030 +75°C	6.0	-	-	2.5	4.0	0.4	0.85	0.55	1.8	0.9	-	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC3130 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3030 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_C	I_{in}	I_D	V_R	V_{RH}	V_F	V_{EE1}	V_{EE2}	V_{IH}	V_{IL}	V_{max}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	2, 3, 13	1	-	-	-	-	-	-	14	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	1	-	-	-	-	-	-	-	-	14	2, 3, 7, 13*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	14	2, 3, 7, 13*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	7*
Output Output Voltage	V_{OL}	12	-	1.5	-	1.35	-	1.15	-	1.4	-	1.35	-	1.25	Vdc	12	-	-	-	-	-	11	-	1	-	-	14	-	7*
Emitter Current	I_{EO}	11	-	-300	-	-300	-	-300	-	-300	-	-300	-	-300	μAdc	-	-	-	-	-	-	-	11	-	1	-	12, 14	-	7**
Collector Current	I_{CO}	12	-	300	-	300	-	300	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	11	1	-	-	12, 14	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	7.0	-	-	-	-	-	7.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,5, 6,7,8,13
Power Supply Drain	I_{PDL}	14	-	4.5	-	4.5	-	4.5	-	4.5	-	4.5	-	4.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5, 6,7,8,13

* Ground inputs to gates not under test unless otherwise noted.

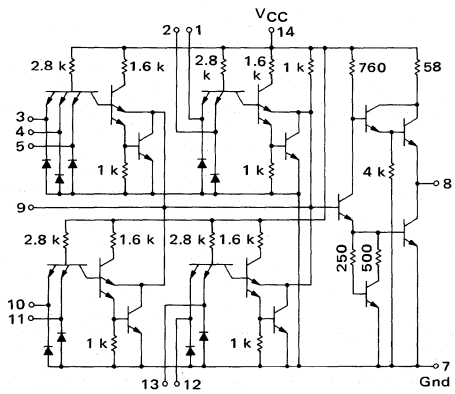
** The inputs to both gates are ungrounded.

EXPANDABLE 4-WIDE
2-2-2-3 INPUT
"AND-OR" GATE

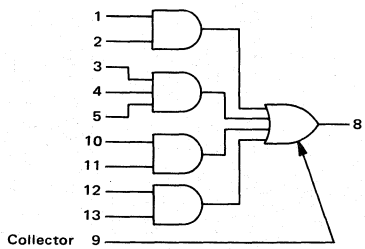
MC3131F • MC3031F
MC3131L • MC3031L,P

(54H52J) (74H52J, N)

CIRCUIT SCHEMATIC



This device consists of three 2-input AND gates and one 3-input AND gate ORED together to provide the AND-OR function. A single expander pin is available which provides the capability to expand this gate to a 10-wide AND-OR gate using the MC3119/3019 triple expander.

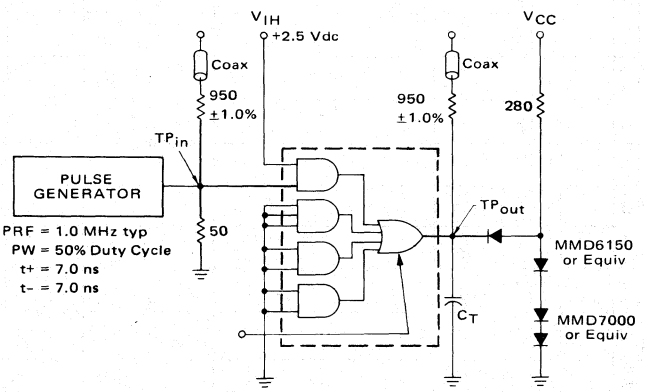


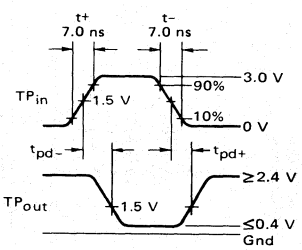
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 87.5 mW typ/pkg
Propagation Delay Time = 10 ns typ

Pin numbers for the 54H52F/74H52F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3131F,L/3031F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H52F/74H52F	5	6	7	8	9	10	11	12	13	14	1	2	3	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





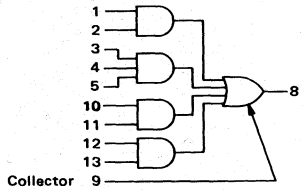
Expander pins should be left open when measuring switching times.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Only one input of the expander is being tested. To complete testing, sequence through remaining inputs.



@ Test Temperature		I_{OL}	I_{OH}	I_{in}	I_D	I_X	V_F	V_{IL}	V_{IH}	V_{RH}	V_X	V_R	V_{CCL}	V_{CCH}	V_{max}
		TEST CURRENT/VOLTAGE VALUES													
		mA					Volts								
MC3131	−55°C	20	-2.0	1.0	-	-0.3	0.4	1.1	2.0	4.5	1.0	2.4	4.5	5.5	-
	+25°C	20	-2.0	1.0	-10	-0.3	0.4	1.1	2.0	4.5	1.0	2.4	4.5	5.5	7.0
	+125°C	20	-2.0	1.0	-	-0.3	0.4	0.8	1.8	4.5	1.0	2.4	4.5	5.5	-
MC3031	0°C	20	-2.0	1.0	-	-0.3	0.4	1.1	2.0	4.5	1.0	2.5	4.75	5.25	-
	+25°C	20	-2.0	1.0	-10	-0.3	0.4	1.1	2.0	4.5	1.0	2.5	4.75	5.25	7.0
	+75°C	20	-2.0	1.0	-	-0.3	0.4	0.9	1.8	4.5	1.0	2.5	4.75	5.25	-

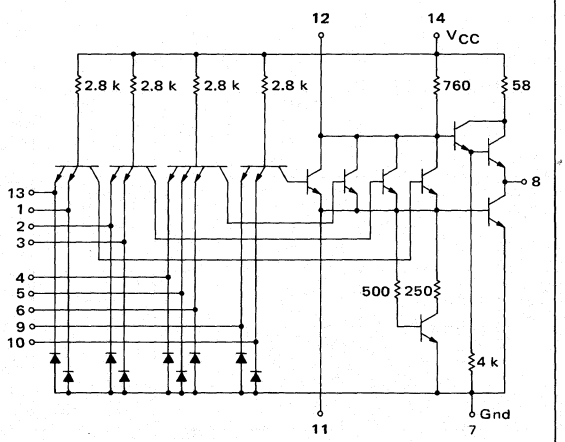
Characteristic	Symbol	Pin Under Test	MC3131 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3031 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	I_X	V_F	V_{IL}	V_{IH}	V_{RH}	V_X	V_R	V_{CCL}	V_{CCH}	V_{max}	Gnd
Input																													
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	1	-	-	2	-	-	-	14	-	7
Reverse Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	-	-	-	1	-	14	-	2,7
Breakdown Voltage	BV_{in}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2,7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	14	-	7
Expander Input Current	I_{EX}	9	-2.7	-4.5	-2.7	-4.5	-2.7	-4.5	-2.9	-5.35	-2.9	-5.35	-2.9	-5.35	mAdc	-	8	-	-	-	-	-	-	-	9	-	14	-	-	1,2,3,4,5, 7,10,11,12,13
Output																													
Output Voltage	V_{OL}	8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	1,3, 10,12	-	2,4,5, 11,13	-	-	14	-	-	7
		8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	9	-	-	-	1,2,3,4,5 10,11,12,13	-	-	14	-	-	7
	V_{OH}	8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	-	-	1,2	-	-	-	14	-	-	3,4,5,7,10,11 12,13
		8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	-	-	-	-	9	-	14	-	-	1,2,3,4,5, 7,10,11,12.13
Short-Circuit Current	I_{SC}	8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	1,2,3,4,5 10,11,12,13	-	-	-	14	-	7,8
Power Requirements																													
Max Power Supply Current	I_{max}	14	-	-	-	34	-	-	-	-	-	34	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5,7, 10,11,12.13
Power Supply Drain	I_{PDH}	14	-	31	-	31	-	31	-	31	-	31	-	31	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	7
	I_{PDL}	14	-	24	-	24	-	24	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5 7,10,11,12,13
Switching Parameters																Pulse In	Pulse Out												
Turn-On Delay	t_{pd-}	1,8	-	-	-	15	-	-	-	-	-	15	-	-	ns	1	8	-	-	-	-	-	-	-	-	2	14	-	-	3,4,5,7, 10,11,12.13
Turn-Off Delay	t_{pd+}	1,8	-	-	-	15	-	-	-	-	-	15	-	-	ns	1	8	-	-	-	-	-	-	-	-	2	14	-	-	3,4,5, 7,10

EXPANDABLE
4-WIDE 2-2-2-3-INPUT
"AND-OR-INVERT" GATE

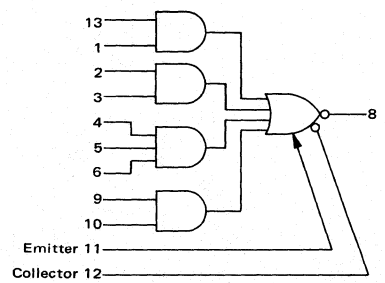
MC3132F • MC3032F
MC3132L • MC3032L,P

(54H53J) (74H53J, N)

CIRCUIT SCHEMATIC



This device consists of four 2-2-2-3-input AND gates ORed together and inverted. Up to four MC3120/3020 or one MC3118/3018 expander gates may be ORed with the device at the expander points.



Positive Logic:

$8 = \overline{(13 \cdot 1) + (2 \cdot 3) + (4 \cdot 5 \cdot 6) + (9 \cdot 10) + \text{(Expanders)}}$

Negative Logic:

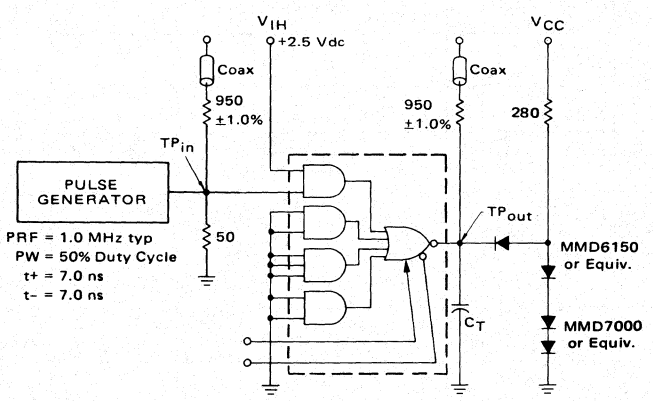
$8 = \overline{13 + 1) \cdot (2 + 3) \cdot (4 + 5 + 6) \cdot (9 + 10) \cdot \text{(Expanders)}}$

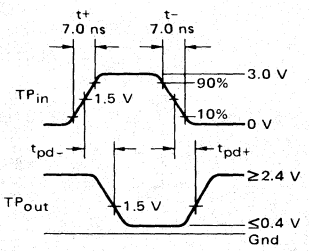
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 7 ns typ

Pin numbers for the 54H53F/74H53F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3132F,L/3032F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H53F/74H53F	5	6	7	8	9	10	11	12	13	14	1	2	3	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





Expander pins should be left open when measuring switching times.

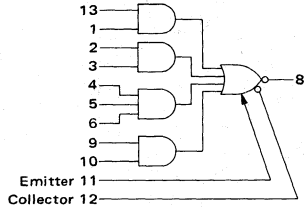
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one input of the device. To complete testing, sequence through remaining inputs in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)																	
	mA								Ohms	Volts								
	I_{OL}	I_{OH}	I_{in}	I_D	I_{X1}	I_{X2}	I_{X3}	I_{X4}	R_{EX} ③	V_{EX} ①	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CC}	V_{CCL}	V_{CCH}
MC3132	20	-2.0	1.0	-10	0.7	0.32	-0.32	-0.47	63	1.4	0.4	2.4	4.0	2.0	0.8	5.0	4.5	5.5
MC3032	20	-2.0	1.0	-10	1.1	0.57	-0.57	-0.6	68	1.4	0.4	2.4	4.0	2.0	0.8	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC3132 Test Limits −55 to +125°C Min	Max	Unit	MC3032 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	I_{X1}	I_{X2}	I_{X3}	I_{X4}	R_{EX} ③	V_{EX} ①	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																										
Forward Current	I_F	1	-	-2.0	mAdc	-	-2.0	mAdc	-	-	-	-	-	-	-	-	-	-	1	-	13	-	-	-	-	14	7
Leakage Current	I_R	1	-	50	μAdc	-	50	μAdc	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	14	2,3,4,5,6, 7,9,10,13
Breakdown Voltage	BV_{in}	1	5.5**	-	mVdc	5.5**	-	mVdc	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	2,3,4,5,6, 7,9,10,13
Clamp Voltage	V_D	1	-	-1.5**	mVdc	-	-1.5**	mVdc	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	14	-	7
Expander Input Current	I_{EX}	12 ①	-	-5.85	mAdc	-	-6.3	mAdc	8	-	-	-	-	-	-	-	-	12	-	-	-	-	-	-	14	-	1,2,3,4,5,6, 7,9,10,13
Base-Emitter Voltage	V_{BE}	11 ②	-	1.0	Vdc	-	1.0	Vdc	8	-	-	-	11, 12	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5,6, 7,9,10,13
Output																										
Output Voltage	V_{OL}	8	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	-	-	-	-	-	-	-	1, 13	-	-	14	-	2,3,4,5,6, 7,9,10
		8 ③	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	-	11	12	-	-	-	-	1, 13	-	-	14	-	1,2,3,4,5,6, 7,9,10,13
	V_{OH}	8	2.4	-	Vdc	2.4	-	Vdc	-	8	-	-	-	-	-	-	-	-	-	-	3, 5 10, 13	-	1,2,4,9	-	14	-	7
		8	2.4	-	Vdc	2.4	-	Vdc	-	8	-	-	-	11	12	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5,6, 7,9,10,13
Short-Circuit Current	I_{SC}	8	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5,6, 7,8,9,10,13
Power Requirements																										
Power Supply Drain	I_{PDH}	14	-	14	mAdc	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3,4,6 5,9,10,13	-	-	-	-	14	7
	I_{PDL}	14	-	11	mAdc	-	11	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5,6, 7,9,10,13
Switching Parameters									Pulse In	Pulse Out																
Turn-On Delay	t_{pd-} †	1, 8	-	11**	ns	-	11**	ns	1	8	-	-	-	-	-	-	-	-	-	13	-	-	-	-	14	-	-	2,3,4,5,6, 7,9,10
Turn-Off Delay	t_{pd+} †	1, 8	-	11**	ns	-	11**	ns	1	8	-	-	-	-	-	-	-	-	-	13	-	-	-	-	14	-	-	2,3,4,5,6, 7,9,10

**Tested only at 25°C † Expander pins open

① See Figure 1.

② See Figure 2.

③ See Figure 3.

FIGURE 1 – I_{EX} TEST CIRCUIT

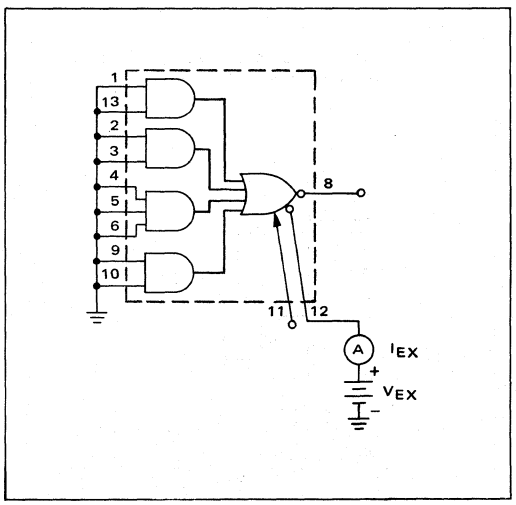


FIGURE 2 – V_{BE} TEST CIRCUIT

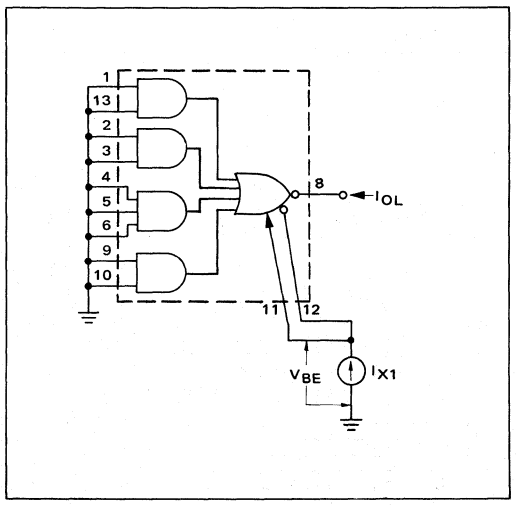
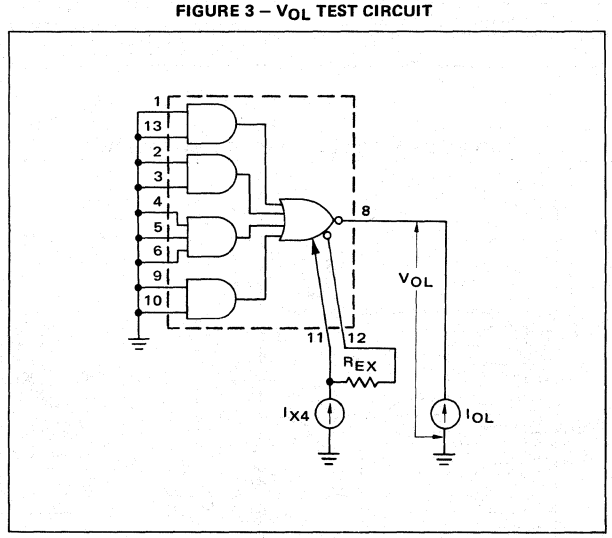


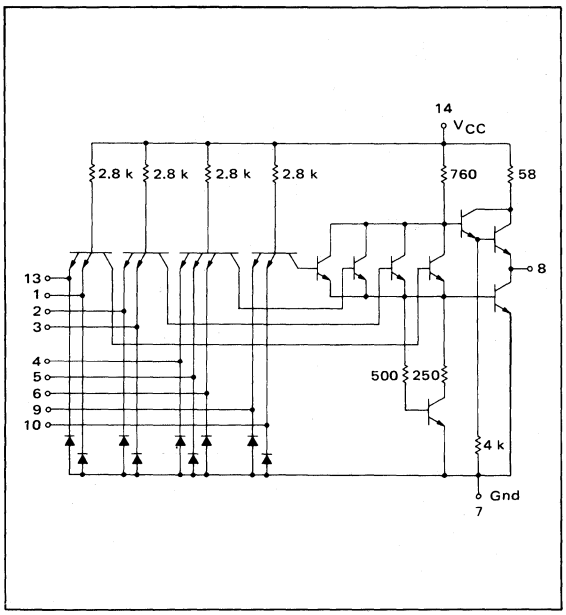
FIGURE 3 – V_{OL} TEST CIRCUIT



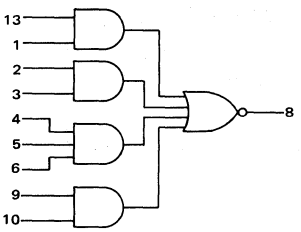
4-WIDE 2-2-2-3-INPUT
"AND-OR-INVERT" GATE

MC3133F • MC3033F
MC3133L • MC3033L,P

(54H54J) **(74H54J,N)**



This device consists of four 2-2-2-3-input AND gates ORed together and inverted.



Positive Logic:

$$8 = (13 \cdot 1) + (2 \cdot 3) + (4 \cdot 5 \cdot 6) + (9 \cdot 10)$$

Negative Logic:

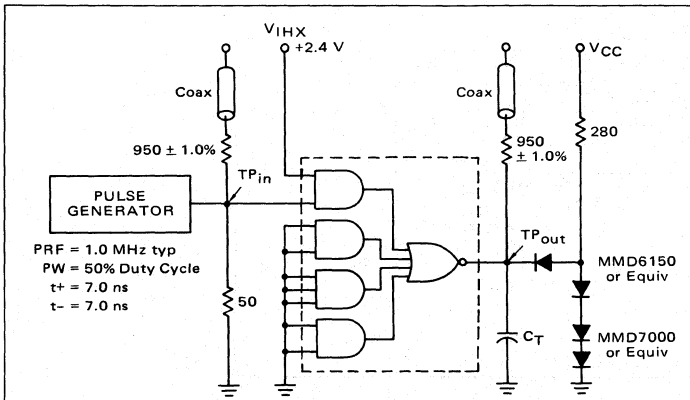
$$8 = \overline{13 + 1) \cdot (2 + 3) \cdot (4 + 5 + 6) \cdot (9 + 10)}$$

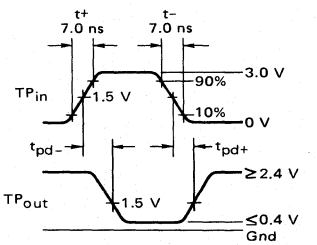
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 7 ns typ

Pin numbers for the 54H54F/74H54F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3133F,L/3033F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H54F/74H54F	5	6	7	8	9	10	11	12	13	14	1	2	3	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





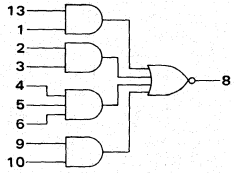
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of this device. To complete testing, sequence through remaining inputs in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA				Volts							
	I_{OL}	I_{OH}	I_{in}	I_D	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CC}	V_{CCL}	V_{CCH}
MC3133	20	-1.6	1.0	-10	0.4	2.4	4.0	2.0	0.8	5.0	4.5	5.5
MC3033	20	-1.6	1.0	-10	0.4	2.4	4.0	2.0	0.8	5.0	4.75	5.25

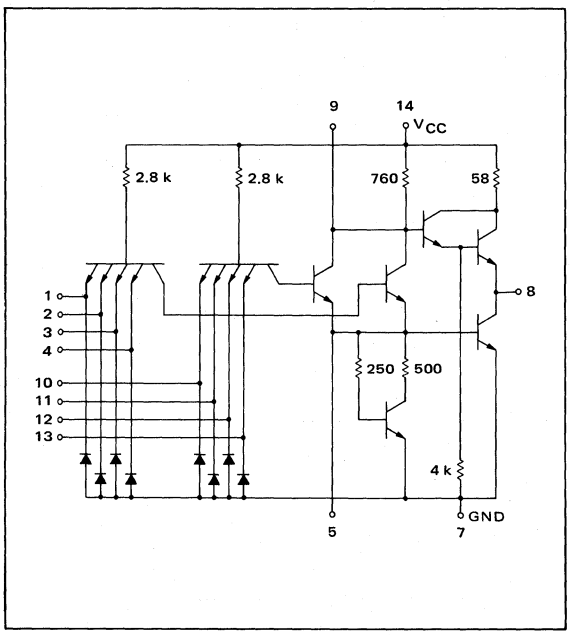
Characteristic	Symbol	Pin Under Test	MC3133 Test Limits −55 to +125°C			MC3033 Test Limits 0 to +75°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												Gnd
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	I_{in}	I_D	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CC}	V_{CCL}	V_{CCH}	
Input																					
Forward Current	I_F	1	-	-2.0	mAdc	-	-2.0	mAdc	-	-	-	-	1	-	13	-	-	-	-	14	7
Leakage Current	I_R	1	-	50	μAdc	-	50	μAdc	-	-	-	-	-	1	-	-	-	-	-	14	2,3,4,5,6 7,9,10,13
Breakdown Voltage	BV_{in}	1	5.5**	-	mVdc	5.5**	-	mVdc	-	-	1	-	-	-	-	-	-	-	-	14	2,3,4,5,6 7,9,10,13
Clamp Voltage	V_D	1	-	-1.5**	mVdc	-	-1.5**	mVdc	-	-	-	1	-	-	-	-	-	-	14	-	7
Output																					
Output Voltage	V_{OL}	8	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	-	1,13	-	-	14	-	2,3,4,5,6 7,9,10
	V_{OH}	8	2.4	-	Vdc	2.4	-	Vdc	-	8	-	-	-	-	3,5, 10,13	-	1,2,4,9	-	14	-	7
Short-Circuit Current	I_{SC}	8	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5,6, 7,8,9,10,13
Power Requirements																					
Power Supply Drain	I_{PHH}	14	-	14	mAdc	-	14	mAdc	-	-	-	-	-	-	1,2,3,4,6, 5,9,10,13	-	-	-	-	14	7
	I_{PDL}	14	-	11	mAdc	-	11	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5,6 7,9,10,13
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1,8	-	11**	ns	-	11**	ns	1	6	-	-	-	13	-	-	-	14	-	-	2,3,4,5,6 7,9,10
Turn-Off Delay	t_{pd+}	1,8	-	11**	ns	-	11**	ns	1	6	-	-	-	13	-	-	-	14	-	-	2,3,4,5, 7,9,10

**Tested only at 25°C

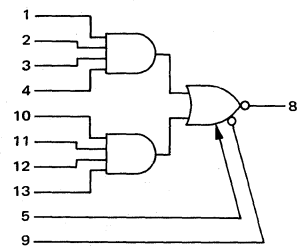
EXPANDABLE 2-WIDE 4-INPUT "AND-OR-INVERT" GATE

MC3134F • MC3034F
MC3134L • MC3034L, P

(54H55J) (74H55J, N)



This device consists of two 4-input AND gates ORed together and inverted. The emitter and collector nodes of the OR stage are brought out to provide expansion capability to a 6-wide AOI gate using the MC3130/3030 or MC3118/3018 expanders.



Positive Logic:

$8 = \overline{(1 \bullet 2 \bullet 3 \bullet 4) + (10 \bullet 11 \bullet 12 \bullet 13) + (\text{Expanders})}$

Negative Logic:

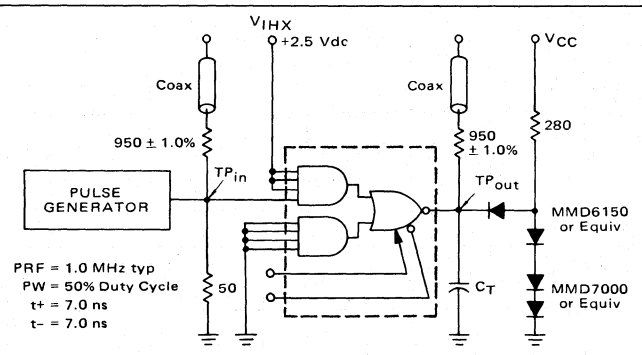
$8 = \overline{(1 + 2 + 3 + 4) \bullet (10 + 11 + 12 + 13) \bullet (\text{Expanders})}$

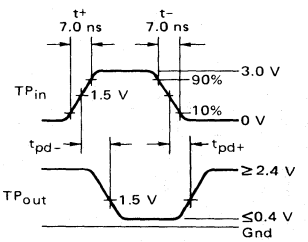
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 30 mW typ/pkg
Propagation Delay Time = 7.0 ns typ

Pin numbers for the 54H55F/74H55F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3134F,L/3034F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H55F/74H55F	14	1	2	3	9	10	11	12	13	5	6	7	8	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





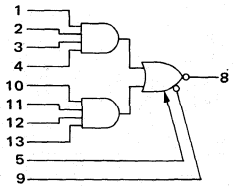
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)																	
	mA								Ohms	Volts								
	I_{OL}	I_{OH}	I_{in}	I_D	I_{X1}	I_{X2}	I_{X3}	I_{X4}	R_{EX} ③	V_{EX} ①	V_F	V_R	V_{RH}	V_{IH}	V_{IHX}	V_{IL}	V_{CC}	V_{CCL}	V_{CCH}
MC3134	20	-2.0	1.0	-10	0.7	0.32	-0.32	0.47	68	1.4	0.4	2.4	4.0	2.0	2.4	0.8	5.0	4.5	5.5
MC3034	20	-2.0	1.0	-10	1.1	0.57	-0.57	0.6	63	1.4	0.4	2.5	4.0	2.0	2.4	0.8	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC3134 Test Limits −55 to +125°C Min	Max	Unit	MC3034 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	I_{X1}	I_{X2}	I_{X3}	I_{X4}	R_{EX} ③	V_{EX} ①	V_F	V_R	V_{RH}	V_{IH}	V_{IHX}	V_{IL}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																											
Forward Current	I_F	1	-	-2.0	mAdc	-	-2.0	mAdc	-	-	-	-	-	-	-	-	-	-	1	-	2,3,4	-	-	-	-	-	14	7
Leakage Current	I_{RI}	1	-	50	μAdc	-	50	μAdc	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	14	2,3,4,7, 10,11,12,13
Breakdown Voltage	BV_{in}	1	5.5**	-	mVdc	5.5**	-	mVdc	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	2,3,4,7, 10,11,12,13
Clamp Voltage	V_D	1	-	-1.5**	Vdc	-	-1.5**	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	7
Expander Input Current	I_{EX}	9 ①	-	-5.85	mAdc	-	-6.3	mAdc	-	-	-	-	-	-	-	-	-	5,9	-	-	-	-	-	-	-	14	-	1,2,3,4,7, 10,11,12,13
Base-Emitter Voltage	V_{BE}	5 ②	-	1.0	Vdc	-	1.0	Vdc	8	-	-	-	5,9	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,7, 10,11,12,13
Output																											
Output Voltage	V_{OL}	8	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	-	-	-	-	-	-	-	1,2, 3,4	-	-	-	14	-	7,10,11,12,13
		8 ③	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	-	5	9	-	-	-	-	1,2, 3,4	-	-	-	14	-	1,2,3,4,7, 10,11,12,13
	V_{OH}	8	2.4	-	Vdc	2.5	-	Vdc	-	8	-	-	-	-	-	-	-	-	-	-	2,3,4, 11,12,13	-	-	1,10	-	14	-	7
		8	2.4	-	Vdc	2.5	-	Vdc	-	8	-	-	-	5	9	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,7, 10,11,12,13
Short-Circuit Current	I_{SC}	8	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,7, 10,11,12,13
Power Requirements																											
Power Supply Drain	I_{PDH}	14	-	12	mAdc	-	12	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3,4,10, 11,12,13	-	-	-	-	-	14	7
	I_{PDL}	14	-	6.4	mAdc	-	6.4	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,7, 10,11,12,13
Switching Parameters									Pulse In	Pulse Out																	
Turn-On Delay	t_{pd-}**	1,8	-	11**	ns	-	11**	ns	1	8	-	-	-	-	-	-	-	-	-	-	-	-	2,3,4	-	14	-	-	7,10,11,12,13
Turn-Off Delay	t_{pd+}**	1,8	-	11**	ns	-	11**	ns	1	8	-	-	-	-	-	-	-	-	-	-	-	-	2,3,4	-	14	-	-	7,10,11,12,13

**Tested only at 25°C

① See Figure 1.

② See Figure 2.

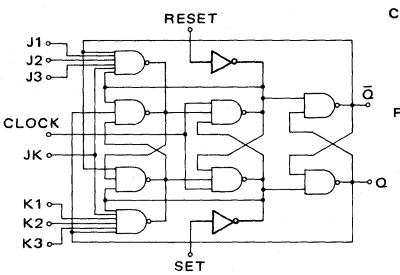
③ See Figure 3.

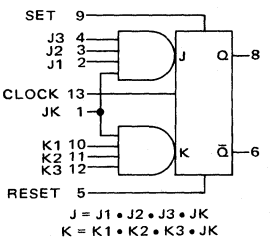
MC3150F • MC3050F
MC3150L • MC3050L,P

This J-K flip-flop triggers on the positive edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct SET and RESET are provided to permit presetting data, such as initial conditions into the flip-flop. The direct SET and RESET fully override the clock; i.e., the direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set up and Hold times. The inputs are inhibited when the clock is high; data is entered into the input steering section of the flip-flop when the clock goes low. The input steering section of the flip-flop continually reflects the input state when the clock is low. Data present during the time interval between the Set up and Hold times is transferred to the bistable section on the positive edge of the clock and the outputs Q and $\bar{Q}$ respond accordingly. The flip-flop can be set or reset directly by applying the high state to the SET or RESET inputs.

LOGIC DIAGRAM





J = J1 • J2 • J3 • JK
K = K1 • K2 • K3 • JK

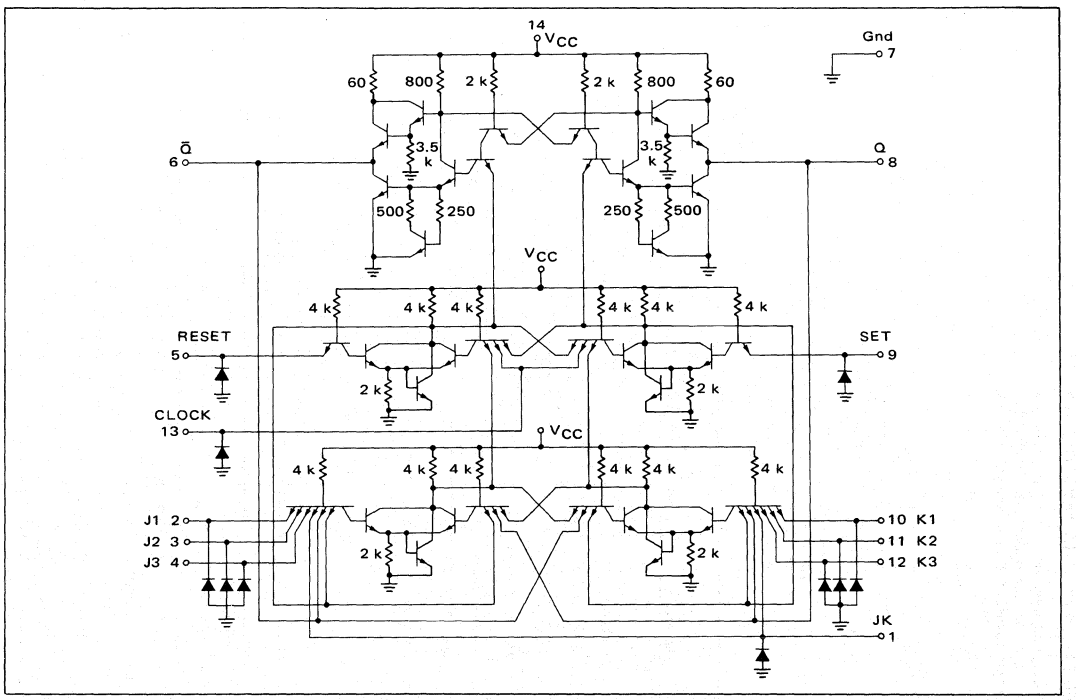
TRUTH TABLE

J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Input Loading Factors:
J, K, SET, RESET = 0.75
CLOCK, JK = 1.5

Output Loading Factor = 10

Typical Characteristics (V_{CC} = 5.0 V, T_A = 25°C)
Total Power Dissipation = 80 mW/pkg
Toggle Frequency = 40 MHz
Logical "1" Setup Time = 10 ns
Logical "0" Setup Time = 5.0 ns
Logical "1" and "0" Hold Time = 5.0 ns
t_{pd-} = 12 ns
t_{pd+} = 14 ns



See General Information section for packaging.

FIGURE 1 – I_{EX} TEST CIRCUIT

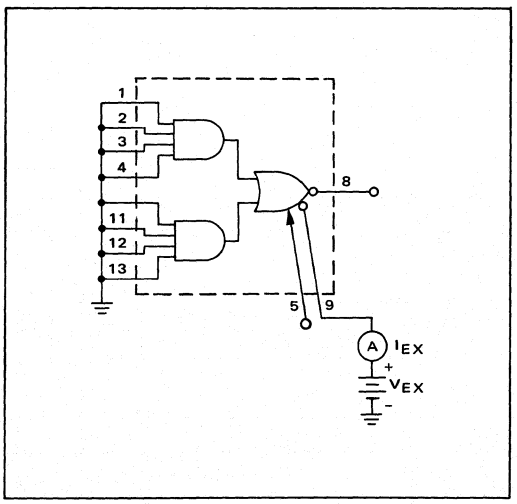


FIGURE 2 – V_{BE} TEST CIRCUIT

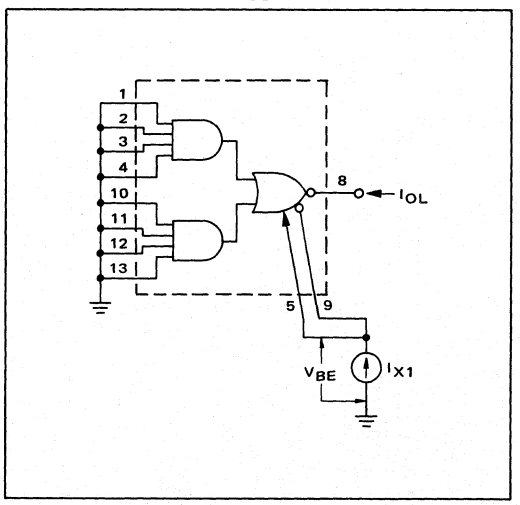
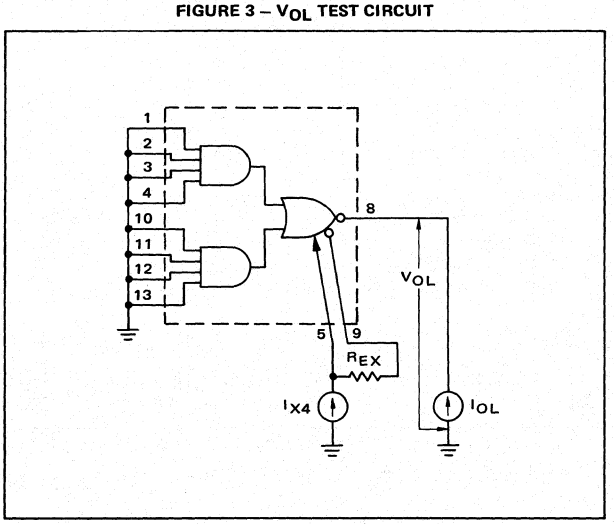
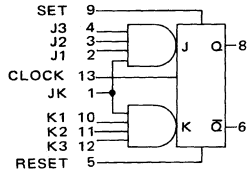


FIGURE 3 – V_{OL} TEST CIRCUIT



ELECTRICAL CHARACTERISTICS



@ Test Temperature		I_{OL} (mA)	I_{OH} (mA)	I_{in} (mA)	I_D (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{RH} (Volts)	V_{max} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)
MC3150	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	4.5	5.5
	+25°C	20	-2.0	1.0	10	1.1	1.8	0.4	2.4	4.0	7.0	4.5	5.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	4.5	5.5
MC3050	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	4.75	5.25
	+25°C	20	-2.0	1.0	10	1.1	1.8	0.4	2.5	4.0	7.0	4.75	5.25
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC3150 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3050 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}	Gnd
Input																												
Forward Current	I_{FJ}	2	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	2	-	1,3,4,5	-	-	14	7,9,13
		3	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	3	-	1,2,4,5	-	-	↓	↓
		4	-		-		-		-		-		-			-	-	-	-	-	-	4	-	1,2,3,5	-	-		
	I_{FK}	10	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	10	-	1,9,11,12	-	-	14	5,7,13
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	11	-	1,9,10,12	-	-	↓	↓
		12	-		-		-		-		-		-			-	-	-	-	-	-	12	-	1,9,10,11	-	-		
	I_{FC}	13	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	13	-	-	-	-	14	1,5,7,9
	I_{FJK}	1	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	1	-	2,3,4,10,11,12	-	-	14	5,7,9,13
	I_{FS}	9	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	9	-	5	-	-	14	7
	I_{FR}	5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	5	-	9	-	-	14	7
Leakage Current	I_{RJ}	2	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	2	9	-	-	14	1,3,4,5,7
		3	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	3		-	-	↓	1,2,4,5,7
		4	-		-		-		-		-		-			-	-	-	-	-	-	-	4		-	-		1,2,3,5,7
	I_{RK}	10	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	10	5	-	-	14	1,7,9,11,12
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	11		-	-	↓	1,7,9,10,12
		12	-		-		-		-		-		-			-	-	-	-	-	-	-	12		-	-		1,7,9,10,11
	I_{RC}	13	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	13	1,2,3,4,5,10,11,12	-	-	14	7,9
	I_{RJK}	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	9	-	-	14	2,3,4,5,7,10,11,12
	I_{RS}	9	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	9	-	-	-	14	7
	I_{RR}	5	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	5	-	-	-	14	7
Breakdown Voltage	BV_{in}	2	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	9	-	-	14	1,3,4,5,7
		3	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	3	-	-	-	-	-	↓	-	-	↓	1,2,4,5,7
		4	-	-		-	-	-	-	-		-	-	-		-	-	4	-	-	-	-	-		-	-		1,2,3,5,7
		10	-	-		-	-	-	-	-		-	-	-		-	-	10	-	-	-	-	-	5	-	-		1,7,9,11,12
		11	-	-		-	-	-	-	-		-	-	-		-	-	11	-	-	-	-	-	↓	-	-		1,7,9,10,12
		12	-	-		-	-	-	-	-		-	-	-		-	-	12	-	-	-	-	-		-	-		1,7,9,10,11
		13	-	-		-	-	-	-	-		-	-	-		-	-	13	-	-	-	-	-	1,2,3,4,5,10,11,12	-	-		7,9
		1	-	-		-	-	-	-	-		-	-	-		-	-	1	-	-	-	-	-	9	-	-		2,3,4,5,7,10,11,12
		9	-	-		-	-	-	-	-		-	-	-		-	-	9	-	-	-	-	-	-	-	-		7
		5	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	5	-	-	-	-	-	-	-	-	↓	7
Clamp Voltage	V_D	2	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	2	-	-	-	-	-	-	14	-	7
		3	-	-	-	↓	-	-	-	-	-	↓	-	-	↓	-	-	-	3	-	-	-	-	-	-	↓	-	↓
		4	-	-	-		-	-	-	-	-		-	-		-	-	-	4	-	-	-	-	-	-		-	
		10	-	-	-		-	-	-	-	-		-	-		-	-	-	10	-	-	-	-	-	-		-	
		11	-	-	-		-	-	-	-	-		-	-		-	-	-	11	-	-	-	-	-	-		-	
		12	-	-	-		-	-	-	-	-		-	-		-	-	-	12	-	-	-	-	-	-		-	
		13	-	-	-		-	-	-	-	-		-	-		-	-	-	13	-	-	-	-	-	-		-	
		1	-	-	-		-	-	-	-	-		-	-		-	-	-	1	-	-	-	-	-	-		-	
		9	-	-	-		-	-	-	-	-		-	-		-	-	-	9	-	-	-	-	-	-		-	
		5	-	-	-	↓	-	-	-	-	-	↓	-	-	↓	-	-	-	5	-	-	-	-	-	-	↓	-	↓
Output																												
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	5	9	-	-	-	-	-	14	7,13
		8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	9	5	-	-	-	-	-	14	7,13
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	9	5	-	-	-	-	14	-	7,13
		8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	5	9	-	-	-	-	14	-	7,13
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	5	-	-	14	6,7,9
		8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	9	-	-	14	5,7,8
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	35	-	-	-	-	-	35	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	1,5,7,13
Power Supply Drain	I_{PD}	14	-	27.6	-	27.6	-	27.6	-	27.6	-	27.6	-	27.6	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,5,7,13

OPERATING CHARACTERISTICS

High state data must be present 17 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

Positive edge triggering: When the clock goes from the low state to the high state, the information in the input steering section is transferred to the bistable section.

The direct SET and RESET inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED TO GROUND.

Unused Inputs:

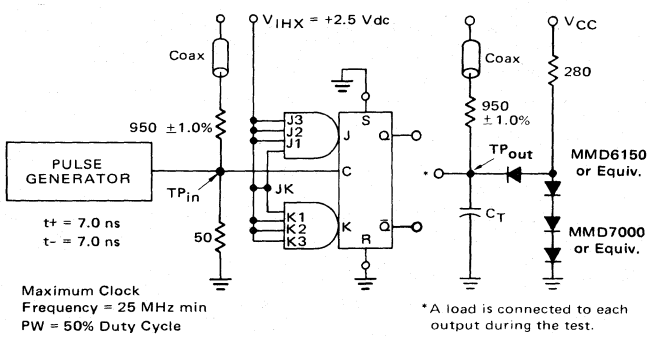
JK input MUST be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and 5.5 Vdc.

Unused J inputs should be tied to used J inputs, the used JK input, $\overline{Q}$, or a voltage between 2.0 and 5.5 Vdc.

Unused K inputs should be tied to used K inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.

Unused SET and RESET inputs MUST be tied to ground.

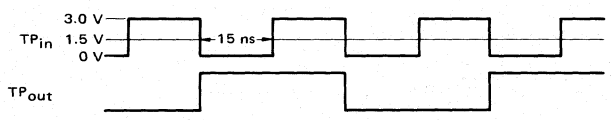
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

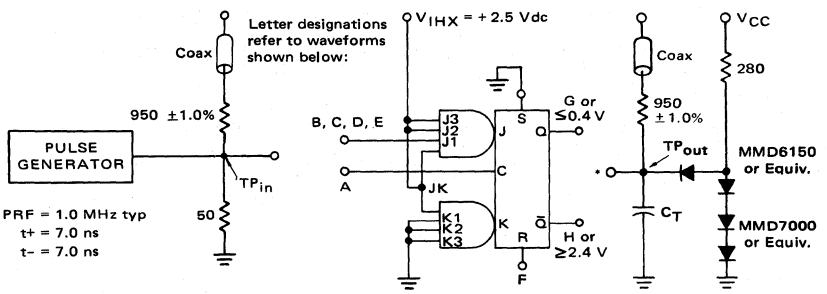
WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)



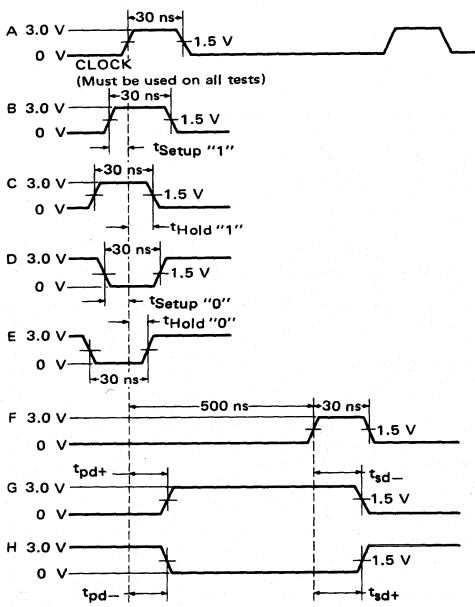
Three pulse generators are required and must be slaved together to provide the waveforms shown.

*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT J**	SET**	RESET**	K**	Q*	Q̄*	LIMITS (ns) Min	Max
t_{Setup} "1" J	B	Gnd	F	Gnd	G	H	-	17
t_{Hold} "1" J	C	Gnd	F	Gnd	G	H	-	0†
t_{Setup} "0" J	D	Gnd	F	Gnd	≤0.4 V	≥2.4 V	-	5.0
t_{Hold} "0" J	E	Gnd	F	Gnd	≤0.4 V	≥2.4 V	-	0†
t_{Setup} "1" K	Gnd	F	Gnd	B	H	G	-	17
t_{Hold} "1" K	Gnd	F	Gnd	C	H	G	-	0†
t_{Setup} "0" K	Gnd	F	Gnd	D	≥2.4 V	≤0.4 V	-	5.0
t_{Hold} "0" K	Gnd	F	Gnd	E	≥2.4 V	≤0.4 V	-	0†
t_{pd+}	Delay from clock to Q during t_{Setup} "1" J test. Delay from clock to Q̄ during t_{Setup} "1" K test.						8.0	30
t_{pd-}	Delay from clock to Q̄ during t_{Setup} "1" J test. Delay from clock to Q during t_{Setup} "1" K test.						8.0	30
t_{sd+}	Delay from SET to Q during t_{Setup} "1" K test. Delay from RESET to Q̄ during t_{Setup} "1" J test.						7.0	23
t_{sd-}	Delay from SET to Q̄ during t_{Setup} "1" K test. Delay from RESET to Q during t_{Setup} "1" J test.						7.0	23

** Letters shown in these columns refer to waveforms at the left.

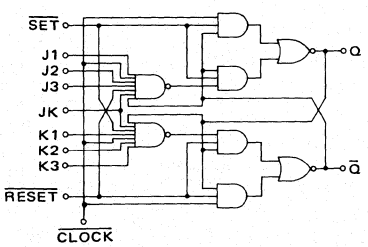
†t_{Hold} is typically a negative number.

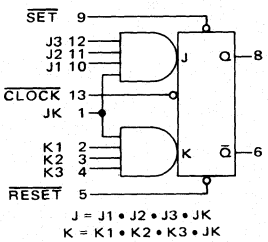
MC3151F • MC3051F
MC3151L • MC3051L,P

This J-K flip-flop triggers on the negative edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct $\overline{SET}$ and $\overline{RESET}$ are provided to permit presetting data, such as initial conditions into the flip-flop. The direct $\overline{SET}$ and $\overline{RESET}$ fully override the clock; i.e., the direct $\overline{SET}$ and $\overline{RESET}$ control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set-up and Hold times. The inputs are inhibited when the clock is low, data is entered into the input steering section of the flip-flop when the clock goes high. The input steering section of the flip-flop continually reflects the input state when the clock is high. Data present during the time interval between the Set-up and Hold times is transferred to the bistable section on the negative edge of the clock and the outputs Q and $\bar{Q}$ respond accordingly. The flip-flop can be set or reset directly by applying the low state to the $\overline{SET}$ or $\overline{RESET}$ inputs.

LOGIC DIAGRAM





J = J1 • J2 • J3 • JK
K = K1 • K2 • K3 • JK

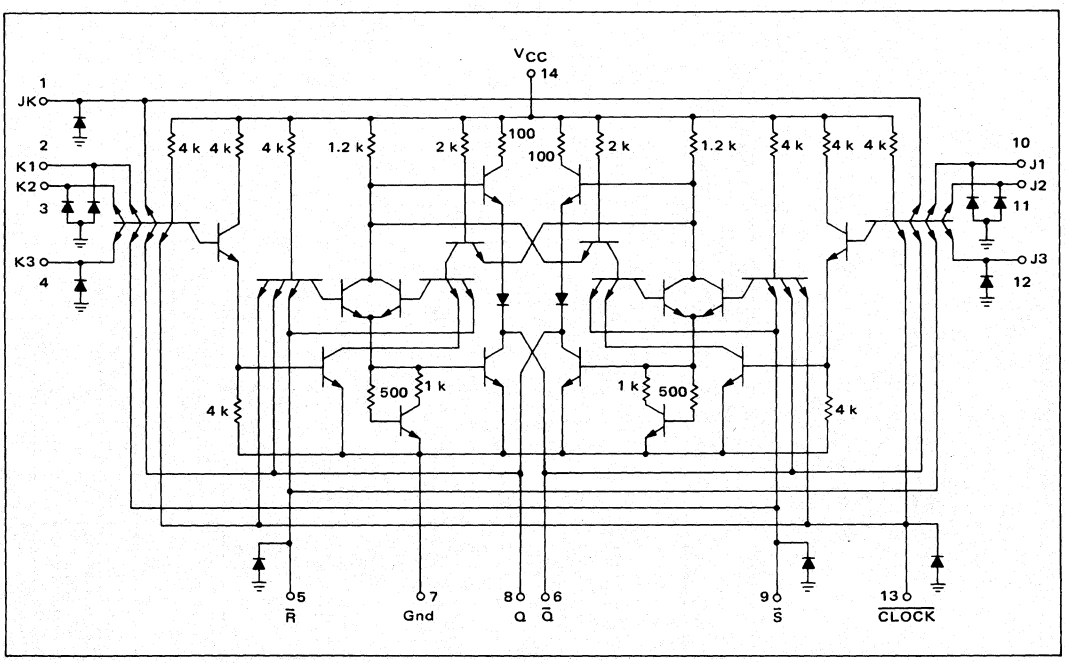
TRUTH TABLE

J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Input Loading Factors:
- J, K = 0.75
- JK = 1.5
- $\overline{Set}$, $\overline{Reset}$ = 2.0
- $\overline{Clock}$ = 2.3

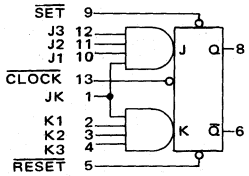
Output Loading Factor = 10

Typical Characteristics (V_{CC} = 5.0 V, T_A = 25°C
- Total Power Dissipation = 50 mW/pkg
- Toggle Frequency = 50 MHz
- Logical "1" Setup Time = 8.0 ns
- Logical "0" Setup Time = 8.0 ns
- Logical "1" and "0" Hold Time = 5.0 ns
- t_{pd-} = 12 ns
- t_{pd+} = 14 ns



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mAdc I_{OL}	I_{OH}	I_{in}	I_D	Volts V_F	V_{IL}	V_{IH}	V_R	V_{RH}	V_{CCL}	V_{CCH}	V_{CC}	V_{max}
MC3151	−55°C	20.0	-2.0	-	-	0.4	1.1	2.0	2.4	4.0	4.5	5.5	5.0	-
	+25°C	20.0	-2.0	1.0	-10	0.4	1.1	1.8	2.4	4.0	4.5	5.5	5.0	7.0
	+125°C	20.0	-2.0	-	-	0.4	0.8	1.8	2.4	4.0	4.5	5.5	5.0	-
MC3051	0°C	20.0	-2.0	-	-	0.4	1.1	2.0	2.5	4.0	4.75	5.25	5.0	-
	+25°C	20.0	-2.0	1.0	-10	0.4	1.1	1.8	2.5	4.0	4.75	5.25	5.0	7.0
	+75°C	20.0	-2.0	-	-	0.4	0.9	1.8	2.5	4.0	4.75	5.25	5.0	-

Characteristic	Symbol	Pin Under Test	MC3151 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3051 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_F	V_{IL}	V_{IH}	V_R	V_{RH}	V_{CCL}	V_{CCH}	V_{CC}	V_{max}	*	Gnd
Input																													
Forward Current	I_F																												
K		2	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	2	-	-	-	1,3,4,5,9,13	-	14	-	-	9	7
J		10	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5		-	-	-	-	10	-	-	-	1,5,9,11,12,13	-		-	-	5	
JK		1	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0		-	-	-	-	1	-	-	-	2,3,4,5,9,10,11,12,13	-		-	-	9	
JK		1	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0		-	-	-	-	1	-	-	-	2,3,4,5,9,10,11,12,13	-		-	-	5	
$\overline{\text{Set}}$		9	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0		-	-	-	-	9	-	-	-	1,2,3,4,5,10,11,12,13	-		-	-	-	
$\overline{\text{Reset}}$		5	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0		-	-	-	-	5	-	-	-	1,2,3,4,10,11,12,13	-		-	-	-	
Clock		13	-	-4.6	-	-4.6	-	-4.6	-	-4.6	-	-4.6	-	-4.6		-	-	-	-	13	-	-	-	1,2,3,4,5,9,10,11,12	-		-	-	5	
Clock		13	-	-4.6	-	-4.6	-	-4.6	-	-4.6	-	-4.6	-	-4.6	▼	-	-	-	-	13	-	-	-	1,2,3,4,5,9,10,11,12	-	▼	-	-	9	▼
Reverse Current	I_R																												
K		2	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	2	9	-	14	-	-	-	1,3,4,5,7,13
J		10	-	50	-	50	-	50	-	50	-	50	-	50		-	-	-	-	-	-	-	10	5	-		-	-	-	1,7,9,11,12,13
JK		1	-	100	-	100	-	100	-	100	-	100	-	100		-	-	-	-	-	-	-	1	-	-		-	-	-	2,3,4,5,7,9,10,11,12,13
$\overline{\text{Set}}$		9	-	140	-	140	-	140	-	140	-	140	-	140		-	-	-	-	-	-	-	9	-	-		-	-	-	1,2,3,4,7,13
$\overline{\text{Reset}}$		5	-	140	-	140	-	140	-	140	-	140	-	140		-	-	-	-	-	-	-	5	-	-		-	-	-	1,7,10,11,12,13
Clock		13	-	145	-	145	-	145	-	145	-	145	-	145	▼	-	-	-	-	-	-	-	13	-	-	▼	-	-	-	1,2,3,4,5,7,9,10,11,12
Breakdown Voltage	BV_{in}																												
K		2	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	9	-	14	-	-	-	1,3,4,5,7,9,13
J		10	-	-		-	-	-	-	-		-	-	-		-	-	10	-	-	-	-	-	5	-		-	-	-	1,5,7,11,12,13
JK		1	-	-		-	-	-	-	-		-	-	-		-	-	-	-	-	-	-	-	-	-		-	-	-	2,3,4,5,7,9,10,11,12,13
$\overline{\text{Set}}$		9	-	-		-	-	-	-	-		-	-	-		-	-	-	-	-	-	-	-	5	-		-	-	5	1,2,3,4,7,10,11,12,13
$\overline{\text{Reset}}$		5	-	-		-	-	-	-	-		-	-	-		-	-	-	-	-	-	-	-	9	-		-	-	9	1,2,3,4,7,10,11,12,13
Clock		13	-	-	▼	-	-	-	-	-	▼	-	-	-	▼	-	-	-	-	-	-	-	-	-	-	▼	-	-	-	1,2,3,4,5,7,9,10,11,12
Clamp Voltage	V_D																												
K		2	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	2	-	-	-	-	-	14	-	-	-	-	7
J		10	-	-	-		-	-	-	-	-		-	-		-	-	-	10	-	-	-	-	-		-	-	-	-	
JK		1	-	-	-		-	-	-	-	-		-	-		-	-	-	1	-	-	-	-	-		-	-	-	-	
$\overline{\text{Set}}$		9	-	-	-		-	-	-	-	-		-	-		-	-	-	9	-	-	-	-	-		-	-	-	-	
$\overline{\text{Reset}}$		5	-	-	-		-	-	-	-	-		-	-		-	-	-	5	-	-	-	-	-		-	-	-	-	
Clock		13	-	-	-	▼	-	-	-	-	-	▼	-	-	▼	-	-	-	13	-	-	-	-	-	▼	-	-	-	-	▼
Output																													
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	9	5	-	-	14	-	-	-	9	7,13
		8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	▼	8	-	-	-	-	5	9	-	-	14	-	-	-	5	7,13
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	5	9	-	-	14	-	-	-	5	7,13
		8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	9	5	-	-	14	-	-	-	9	7,13
Short Circuit Current	I_{SC}	6	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	-	-	9	-	14	-	-	-	5,6,7
		8	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	-	-	5	-	14	-	-	-	7,8,9
Power Requirements (Total Device) Maximum Power Current	I_{max}	14	-	-	-	21	-	-	-	-	-	21	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,7,9,13
Power Supply Drain	I_{PD}	14	-	16	-	16	-	16	-	16	-	16	-	16	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,7,9,13

*Momentary ground before making measurement. If pin number appears in other column, it should be returned to voltage.

OPERATING CHARACTERISTICS

High state data must be present 12 ns prior to the fall of the clock and remain 5.0 ns after the clock signal rises.

Negative edge triggering: When the clock goes from the high state to the low state, the information in the input steering section is transferred to the bistable section.

The direct $\overline{SET}$ and $\overline{RESET}$ inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED to a voltage between 2.0 and 5.5 Vdc.

Unused Inputs:

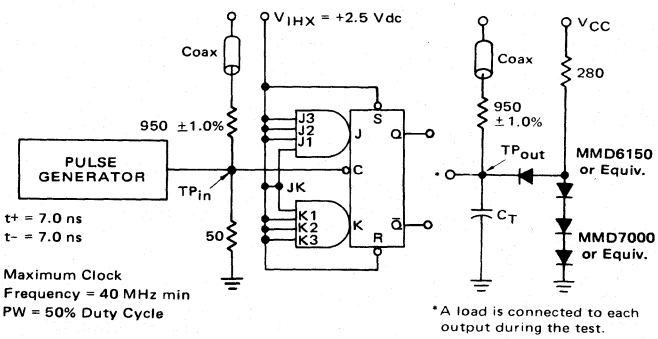
JK input MUST be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and 5.5 Vdc.

Unused J inputs should be tied to used J inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.

Unused K inputs should be tied to used K inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.

Unused $\overline{SET}$ and $\overline{RESET}$ inputs MUST be tied to a voltage between 2.0 and 5.5 Vdc.

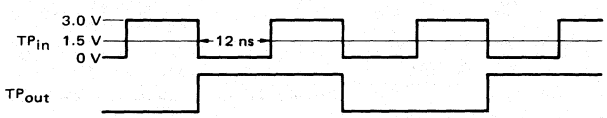
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

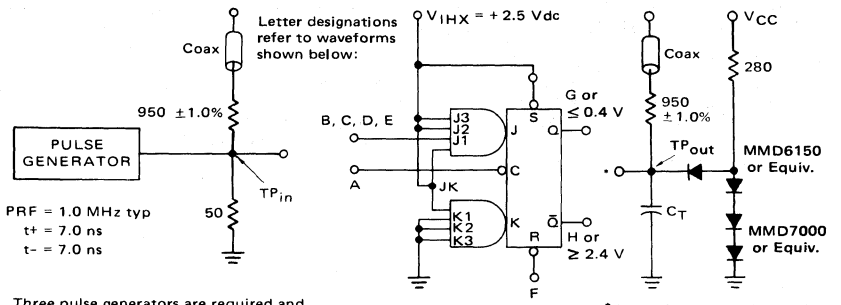
WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

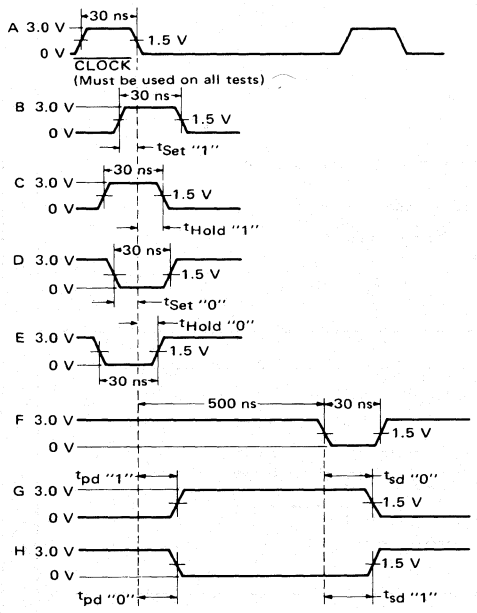
(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT J**	SET**	RESET**	K**	Q**	Q̄**	LIMITS (ns Min	Max
t_{Set} "1" J	B	2.4 V	F	Gnd	G	H	–	12
t_{Hold} "1" J	C	2.4 V	F	Gnd	G	H	–	0
t_{Set} "0" J	D	2.4 V	F	Gnd	≤ 0.4 V	≥ 2.4 V	–	12
t_{Hold} "0" J	E	2.4 V	F	Gnd	≤ 0.4 V	≥ 2.4 V	–	0
t_{Set} "1" K	Gnd	F	2.4 V	B	H	G	–	12
t_{Hold} "1" K	Gnd	F	2.4 V	C	H	G	–	0
t_{Set} "0" K	Gnd	F	2.4 V	D	≥ 2.4 V	≤ 0.4 V	–	12
t_{Hold} "0" K	Gnd	F	2.4 V	E	≥ 2.4 V	≤ 0.4 V	–	0
t_{pd} "1"	Delay from CLOCK to Q during t_{set} "1" J test. Delay from CLOCK to Q̄ during t_{set} "1" K test.							18
t_{pd} "0"	Delay from CLOCK to Q̄ during t_{set} "1" J test. Delay from CLOCK to Q during t_{set} "1" K test.							18
t_{sd} "1"	Delay from SET to Q during t_{set} "1" K test. Delay from RESET to Q̄ during t_{set} "1" J test.							18
t_{sd} "0"	Delay from SET to Q̄ during t_{set} "1" K test. Delay from RESET to Q during t_{set} "1" J test.							18

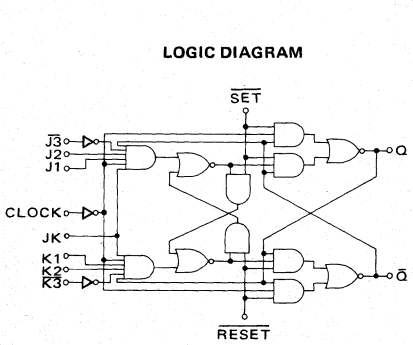
**Letters shown in these columns refer to waveforms at the left.

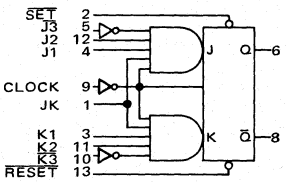
MC3152F • MC3052F
MC3152L • MC3052L,P

This is a master-slave J-K flip-flop that triggers on the positive edge of the clock. The flip-flop has an AND input configuration consisting of two J-inputs and a $\overline{J}$-input ANDed together and two K-inputs and a $\overline{K}$-input ANDed together. An enable input (JK) is also provided consisting of an additional J and K input internally connected together. This input provides gating in addition to the clock for the clocked inputs (J, J, K and K) or an additional logic input (JK) for use in counters or certain other applications. A direct $\overline{SET}$ and $\overline{RESET}$ are provided to enable presetting data into the flip-flop such as initial conditions. The direct $\overline{SET}$ and $\overline{RESET}$ control the operation of the flip-flop regardless of the state of the clock.

Information is normally applied to, or changed at, the clocked inputs while the clock is in the high state, since the inputs are inhibited under this condition. Information may be stored in the master flip-flop section when the clock goes low. Once input data has been stored in the master flip-flop section it cannot be removed (or changed) by means of the clocked inputs. The direct $\overline{SET}$ or $\overline{RESET}$ provide the only means of removing previously stored information. The state of the master flip-flop is transferred to the slave flip-flop section on the positive transition of the clock and the outputs respond accordingly. The flip-flop can be set or reset directly by applying the low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs.

LOGIC DIAGRAM





$J = J1 \cdot J2 \cdot \overline{J3} \cdot JK$

$K = K1 \cdot K2 \cdot \overline{K3} \cdot JK$

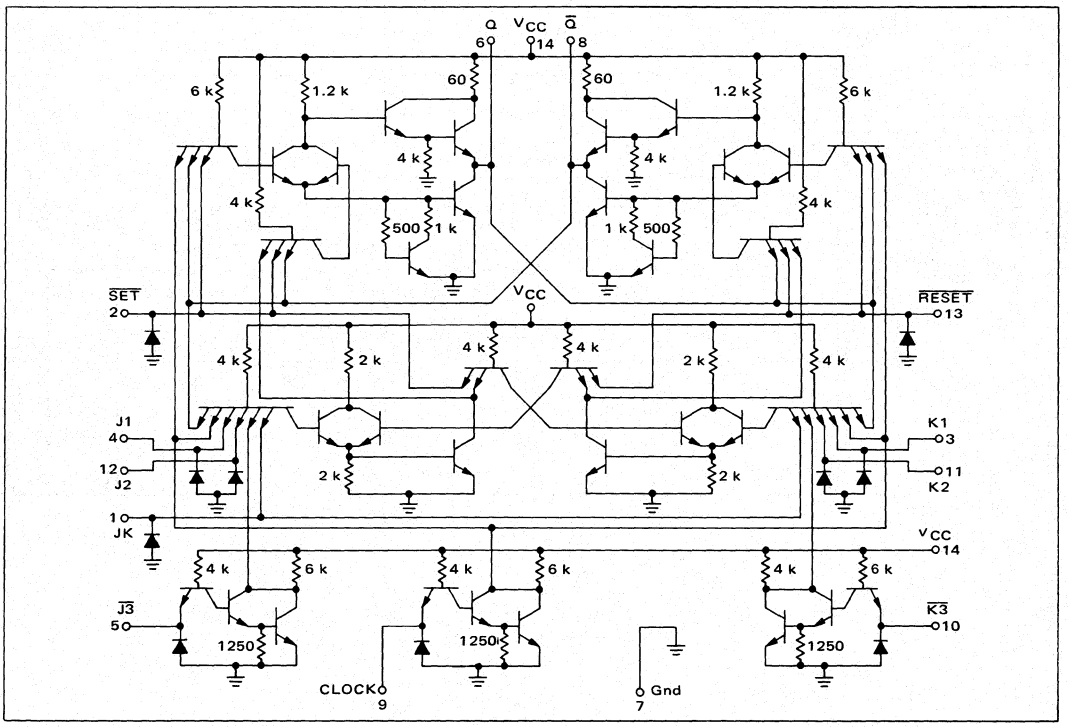
TRUTH TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Input Loading Factors:
JK = 1.5
J, K, CLOCK = 0.75
$\overline{SET}$, $\overline{RESET}$ = 2.25

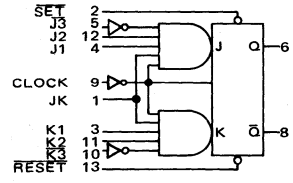
Output Loading Factor = 10

Typical Characteristics:
(V_{CC} = 5.0 V; T_A = 25°C)
Total Power Dissipation = 75 mW/pkg
Toggle Frequency = 40 MHz
Logical "1" Setup Time = 10 ns
Logical "0" Hold Time = 8.0 ns
t_{pd-} = 20 ns
t_{pd+} = 12 ns



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
MC3152	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5
MC3052	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.75
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.75
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.75

Characteristic	Symbol	Pin Under Test	MC3152 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3052 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	$-V_{IH}$	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	P_1*	Gnd
Input																														
Forward Current	I_{FJ}	4	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	4	-	1,12	-	-	-	14	-	5,7,9,13
		12	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	12	-	1,4	-	-	-	14	-	5,7,9,13
	I_{FK}	3	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	3	-	1,11	-	-	-	14	-	2,7,9,10
		11	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	11	-	1,3	-	-	-	14	-	2,7,9,10
	$I_{F\bar{J}}$	5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	5	-	-	-	-	-	14	-	7
	$I_{F\bar{K}}$	10	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	10	-	-	-	-	-	14	-	7
	I_{FC}	9	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	9	-	-	-	-	-	14	-	7
	I_{FJK}	1	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	1	-	3,4,11,12	-	-	-	14	-	2,5,7,9,10,13
	$I_{F\bar{S}}$	2	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-	2	-	-	-	-	-	14	-	7,9,13
	$I_{F\bar{R}}$	13	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-	13	-	-	-	-	-	14	-	2,7,9
Leakage Current	I_{RJ}	4	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	4	5,9	-	-	-	14	-	1,2,7,12
		12	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	12	5,9	-	-	-	14	-	1,2,4,7
	I_{RK}	3	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	3	9,10	-	-	-	14	-	1,7,11,13
		11	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	11	9,10	-	-	-	14	-	1,3,7,13
	$I_{R\bar{J}}$	5	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	5	-	-	-	-	14	-	7
	$I_{R\bar{K}}$	10	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	10	-	-	-	-	14	-	7
	I_{RC}	9	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	9	-	-	-	-	14	-	7
	I_{RJK}	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	5,9,10	-	-	-	14	-	3,4,6,7,8,11,12
	$I_{R\bar{S}}$	2	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	-	-	2	1,4,10,12,13	-	-	-	14	9	3,5,7,11
	$I_{R\bar{R}}$	13	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	-	-	13	1,2,3,5,11	-	-	-	14	9	4,7,10,12
Breakdown Voltage	BV_{in}	4	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	4	-	-	-	-	-	5,9	-	-	-	14	-	1,2,7,12
		12	-	-		-	-	-	-	-		-	-	-		-	-	12	-	-	-	-	-	5,9	-	-	-		-	1,2,4,7
		3	-	-		-	-	-	-	-		-	-	-		-	-	3	-	-	-	-	-	9,10	-	-	-		-	1,7,11,13
		11	-	-		-	-	-	-	-		-	-	-		-	-	11	-	-	-	-	-	9,10	-	-	-		-	1,3,7,13
		1	-	-		-	-	-	-	-		-	-	-		-	-	1	-	-	-	-	-	2,5,9,10,13	-	-	-		-	3,4,6,7,8,11,12
		2	-	-		-	-	-	-	-		-	-	-		-	-	2	-	-	-	-	-	1,4,10,12,13	-	-	-		9	3,5,7,11
		13	-	-		-	-	-	-	-		-	-	-		-	-	13	-	-	-	-	-	1,2,3,5,11	-	-	-		9	4,7,10,12
		5	-	-		-	-	-	-	-		-	-	-		-	-	5	-	-	-	-	-	-	-	-	-		-	7
		9	-	-		-	-	-	-	-		-	-	-		-	-	9	-	-	-	-	-	-	-	-	-		-	7
		10	-	-	▼	-	-	-	-	-	▼	-	-	-	▼	-	-	10	-	-	-	-	-	-	-	-	-	▼	-	7
Clamp Voltage	V_D	4	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	4	-	-	-	-	-	14	-	7
		12	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	12	-	-	-	-	-		-	
		3	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	3	-	-	-	-	-		-	
		11	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	11	-	-	-	-	-		-	
		5	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	5	-	-	-	-	-		-	
		10	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	10	-	-	-	-	-		-	
		9	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	9	-	-	-	-	-		-	
		1	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	1	-	-	-	-	-		-	
		2	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	2	-	-	-	-	-		-	
		13	-	-	▼		-	-	-	-	▼		-	-	▼	-	-	-	-	-	-	13	-	-	-	-	-	▼	-	▼
Output																														
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	-	13	2	-	-	-	-	14	-	-	7,9
		8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	2	13	-	-	-	-	14	-	-	7,9
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	-	2	13	-	-	-	-	14	-	-	7,9
		8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	-	13	2	-	-	-	-	14	-	-	7,9
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	2,6,7
		8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	7,8,13
Power Requirements (Total Device)																														
Maximum Power Current	I_{max}	14	-	-	-	42	-	-	-	-	-	42	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7,9,10,11,12,13

*P_1 = Pulse Applied to Pin

OPERATING CHARACTERISTICS

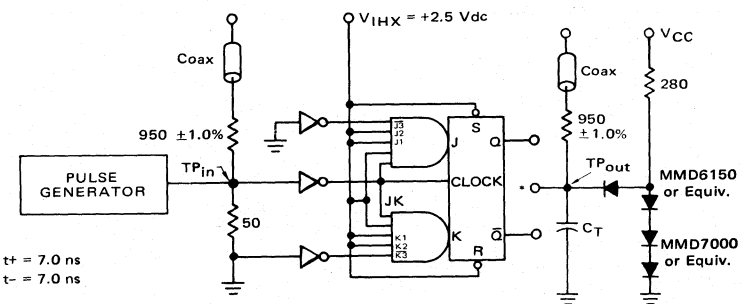
Data should be present prior to the negative clock transition. If data is changed from a "1" to a "0" while the clock is in the low state, the flip-flop will not recognize this new data state.

The application of a low level to the $\overline{SET}$ input sets Q high and low level on the $\overline{RESET}$ input resets Q low. These functions may be performed at any time without regard to the clock area.

Positive edge triggering — When the clock goes from the low to the high state, the information stored in the master flip-flop section is transferred to the slave flip-flop section thus appearing at the outputs. When the clock is in the high state, the inputs are inhibited.

Unused J, K, and JK inputs should be tied together with used inputs, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc. The unused $\overline{J}$ and $\overline{K}$ inputs must be tied to ground. The unused $\overline{SET}$ and $\overline{RESET}$ inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

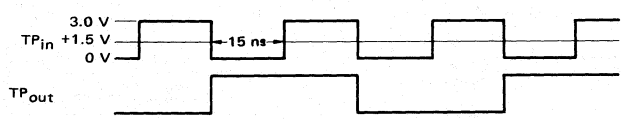
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

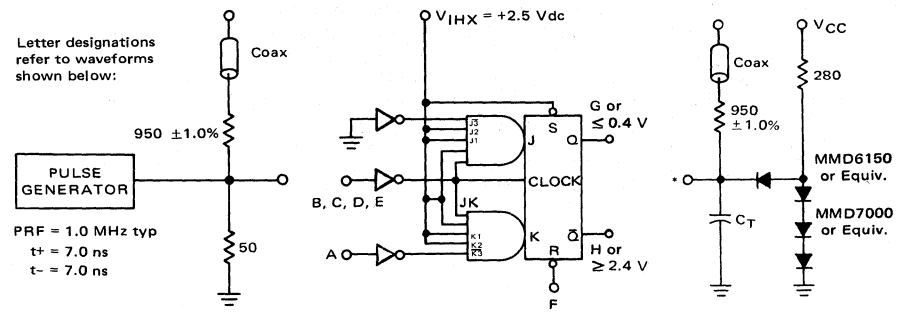
WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

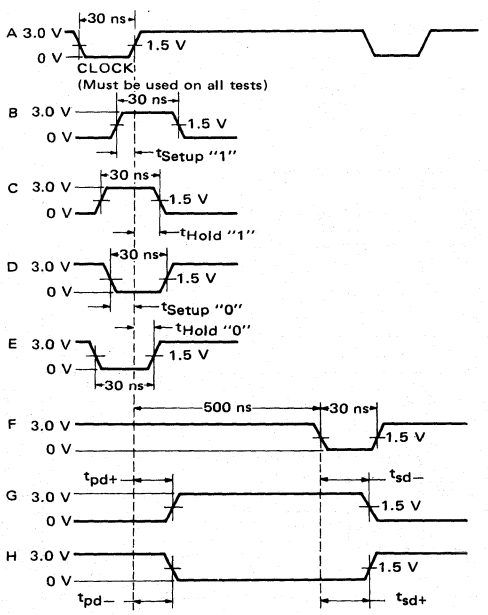
(For J inputs and $\overline{\text{RESET}}$ input; to test other inputs, refer to Test Procedures Chart)



The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

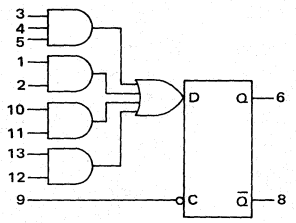
TEST	INPUT J*	INPUT $\overline{J}$*	INPUT $\overline{SET}$*	INPUT $\overline{RESET}$*	INPUT K*	INPUT $\overline{K}$*	Q*	$\overline{Q}$*	LIMITS (ns) Min	LIMITS (ns) Max
t_{Setup} "1" J	C	Gnd	2.4 V	F	Gnd	Gnd	G	H	–	15
t_{Hold} "0" J	B	Gnd	2.4 V	F	Gnd	Gnd	≤0.4 V	≥2.4 V	–	–3.0
t_{Setup} "1" K	Gnd	Gnd	F	2.4 V	C	Gnd	H	G	–	15
t_{Hold} "0" K	Gnd	Gnd	F	2.4 V	B	Gnd	≥2.4 V	≤0.4 V	–	–3.0
t_{Setup} "1" $\overline{J}$	2.4V	E	2.4 V	F	2.4 V	Gnd	G	H	–	15
t_{Hold} "0" $\overline{J}$	2.4 V	D	2.4 V	F	2.4 V	Gnd	≤0.4 V	≥2.4 V	–	–3.0
t_{Setup} "1" $\overline{K}$	2.4V	Gnd	F	2.4 V	2.4 V	E	H	G	–	15
t_{Hold} "0" $\overline{K}$	2.4V	Gnd	F	2.4 V	2.4 V	D	≥2.4 V	≤0.4 V	–	–3.0
t_{pd+}	Delay from clock to Q during t_{Setup} "1" J test. Delay from clock to $\overline{Q}$ during t_{Setup} "1" K test.								8	20
t_{pd-}	Delay from clock to $\overline{Q}$ during t_{Setup} "1" J test. Delay from clock to Q during t_{Setup} "1" K test.								14	28
t_{sd+}	Delay from $\overline{SET}$ to Q during t_{Setup} "1" K test. Delay from $\overline{RESET}$ to $\overline{Q}$ during t_{Setup} "1" J test.								–	18
t_{sd-}	Delay from $\overline{SET}$ to $\overline{Q}$ during t_{Setup} "1" K test. Delay from $\overline{RESET}$ to Q during t_{Setup} "1" J test.								–	25

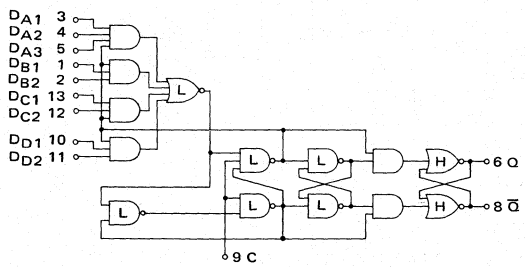
*Letters shown in these columns refer to waveforms.

DOUBLE-EDGE-TRIGGERED
MASTER-SLAVE TYPE D
FLIP-FLOP

MC3153F • MC3053F
MC3153L • MC3053L,P

This double-edge-triggered master-slave type D flip-flop accepts data on the rising clock edge and transfers it to the output when the clock input changes back to the logic "0" state. A 4-wide, 2-2-2-3 input AND-OR gate is internally connected to the D input of the flip-flop. This makes the device useful in forming shift registers using one package per bit.





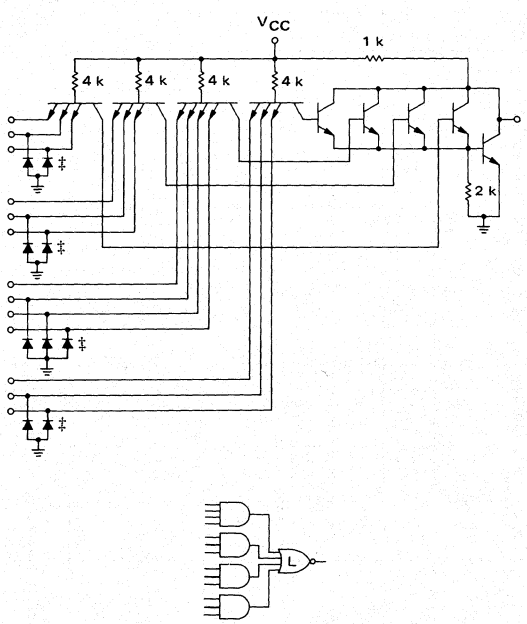
V_{CC} = 14
Gnd = 7

Input Loading Factor:
D Inputs = 1
Clock Input = 2

Output Loading Factor = 10

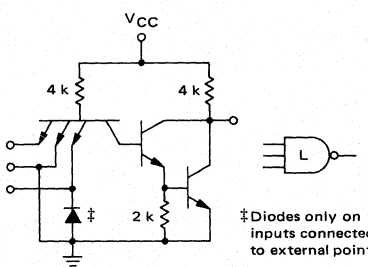
Total Power Dissipation = 100 mW typ

LOW LEVEL "AND-OR-INVERT" GATE



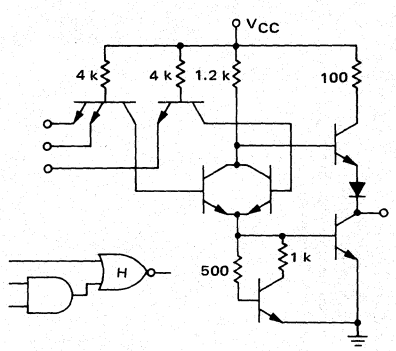
‡Diodes connected from each input to GND.

LOW-LEVEL "NAND" GATE



‡Diodes only on inputs connected to external points.

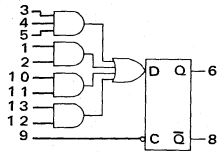
HIGH LEVEL "AND-OR-INVERT" GATE



See General Information section for packaging information.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one of the input AND gates. Furthermore only one input on the AND gate is tested. To complete testing, test other gates and inputs in the same manner.

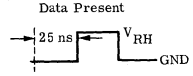


@ Test Temperature		TEST VOLTAGE/CURRENT VALUES mAdc I_{OL1}	I_{OH}	I_{in}	I_D	Vdc V_F	V_{IL}	V_{IH}	V_R	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC3153	−55°C	20.0	-1.6	-	-	0.4	1.1	2.0	2.4	4.0	5.0	4.5	5.5	-
	+25°C	20.0	-1.6	1.0	-10	0.4	1.1	1.8	2.4	4.0	5.0	4.5	5.5	7.0
	+125°C	20.0	-1.6	-	-	0.4	0.8	1.8	2.4	4.0	5.0	4.5	5.5	-
MC3053	0°C	20.0	-1.6	-	-	0.4	1.1	2.0	2.5	4.0	5.0	4.75	5.25	-
	+25°C	20.0	-1.6	1.0	-10	0.4	1.1	1.8	2.5	4.0	5.0	4.75	5.25	7.0
	+75°C	20.0	-1.6	-	-	0.4	0.9	1.8	2.5	4.0	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3153 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3053 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OH}	I_{in}	I_D	V_F	V_{IL}	V_{IH}	V_R	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	**	Gnd*
Input																													
Forward Current	I_F																												
Data		1	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	-	1	-	-	-	2	-	-	14	-	-	7
Clock		9	-	-3.2	-	-3.2	-	-3.2	-	-3.2	-	-3.2	-	-3.2	mAdc	-	-	-	-	9	-	-	-	-	-	-	14	-	-	7
Reverse Current	I_R																												
Data		1	-	40	-	40	-	40	-	40	-	40	-	40	μAdc	-	-	-	-	-	-	-	1	-	-	-	14	-	-	2,7*
Clock		9	-	80	-	80	-	80	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	9	-	-	-	14	-	-	9
Breakdown Voltage	BV_{in}																												
Data		1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	-	2,7*
Clock		9	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	9	-	-	-	-	-	-	-	-	14	-	-	7
Clamp Voltage	V_D																												
Data		1	-	-	-	-1.5	-	-	-	-	-1.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	14	-	-	-	7
Clock		9	-	-	-	-1.5	-	-	-	-	-1.5	-	-	-	Vdc	-	-	-	9	-	-	-	-	-	-	14	-	-	-	7
Output																													
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	1,2,3,4,5, 10,12,13	11	-	-	-	14	-	-	9	7
		8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	1,2,3,4,5,10,11	12,13	-	-	-	14	-	-	9	7
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	3,4,5,10,11,12,13	1,2	-	-	-	14	-	-	9	7
		8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	1,3,4,5,10,11,12,13	2	-	-	-	14	-	-	9	7
Power Requirements (Total Device)																													
Maximum Power Supply Current	I_{max}	14	-	-	-	39	-	-	-	-	-	39	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	7*
	I_{PDH}	14	-	30	-	30	-	30	-	30	-	30	-	30	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	7

*Other input pins grounded.

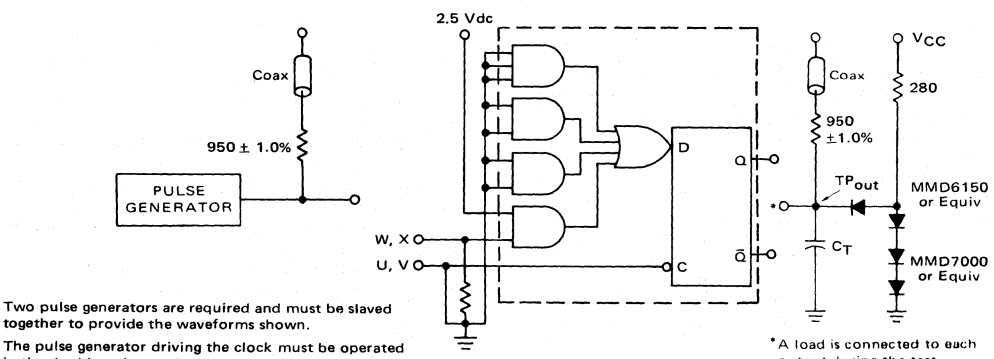
**Apply positive pulse prior to taking measurement to set flip-flop in the desired state.



OPERATING CHARACTERISTICS

Data present at the D inputs 20 ns prior to and 5.0 ns following the rising edge of the clock pulse is stored in the flip-flop until the clock falling edge, when it is transferred to the outputs. The data may change any time except between the setup time (20 ns) and the hold time (5.0 ns) without affecting the outputs.

SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved together to provide the waveforms shown.

The pulse generator driving the clock must be operated in the double pulse mode.

Letter designations refer to waveforms shown below:

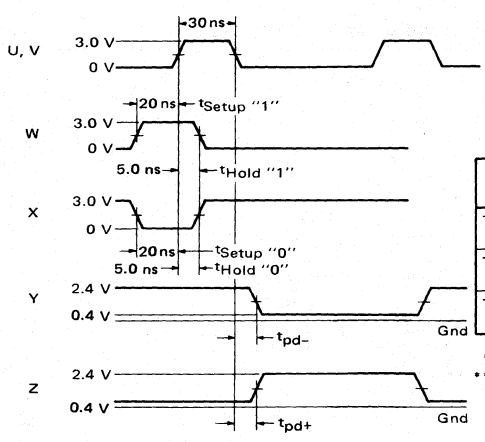
*A load is connected to each output during the test.

SYMBOL	WAVEFORM		
	U	V	W, X
f	20 MHz	1.0 MHz	0.5 MHz
PW	50% Duty Cycle	30 ns	–
t+, t–	7.0 ns	7.0 ns	7.0 ns

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST		SYMBOL	INPUT C̄	INPUT D	Q	Q̄	LIMIT
Turn-On Delay	Q̄	t_{pd-}	V	W	Z	Y	35 ns
	Q		V	X	Y	Z	max.
Turn-Off Delay	Q̄	t_{pd+}	V	X	Y	Z	35 ns
	Q		V	W	Z	Y	max.
Toggle Frequency	Q̄	f_{Tog}	U	*	–	**	20 MHz
	Q		U	*	**	–	min.

*D Input connected to Q̄ output.

**Output must change state with each input pulse.

APPLICATIONS INFORMATION

LOGIC DESCRIPTION

This flip-flop performs the D function, with input logic defined by the following equation:

$$6 = 1 \bullet 2 + 3 \bullet 4 \bullet 5 + 10 \bullet 11 + 12 \bullet 13$$

The operation of the flip-flop is as follows (refer to Figure 1). Assume Q is "0". To set a "1" on the Q output, "1" must be applied to all the inputs on either gate A, B, C, or D. When the clock goes high, a "0" appears on the output of gate G and a "1" appears on the output of gate H. However, because the other input to gate J comes from gate F, the output of J remains "0", and because of the input from gate G to gate I, the output of gate I remains "0". When the clock goes low, the outputs of gates E and F go to "1". Thus gate J now has a "1" applied to both inputs and its output goes to "1". Since gate L now has a "1" applied to it, its output goes to "0", and this is coupled to gate K, which now has zero applied to both inputs causing it to go to a "1". The flip-flop has now switched and Q is a "1". Setting a "0" on the output may be followed through in a similar fashion.

SYSTEM SKEW

Clock skew in a system is one of the most difficult problems that the system designer must solve. Consider the clock driver circuitry shown in Figure 2. Clock skew between C1 and C2 could be caused by a number of factors, including unequal loading, unequal wiring distances, and different turn-on and turn-off times between clock line driver gates that may be in the circuit between C1 and C2. Most flip-flops that are presently available in integrated form do not allow the system designer to control the amount of skew in the system. With the MC3153/3053, system clock skew can be adjusted.

Three basic types of flip-flops are now in use: (1) the charge-controlled flip-flop, (2) the edge-triggered flip-flop, and (3) the master-slave flip-flop. Figure 2 is an example of a system in which the clock skew problem is encountered. The direct-coupled shift register can be made with the two most common types of flip-flops – the negative-edge-triggered flip-flop or the master-slave flip-flop.

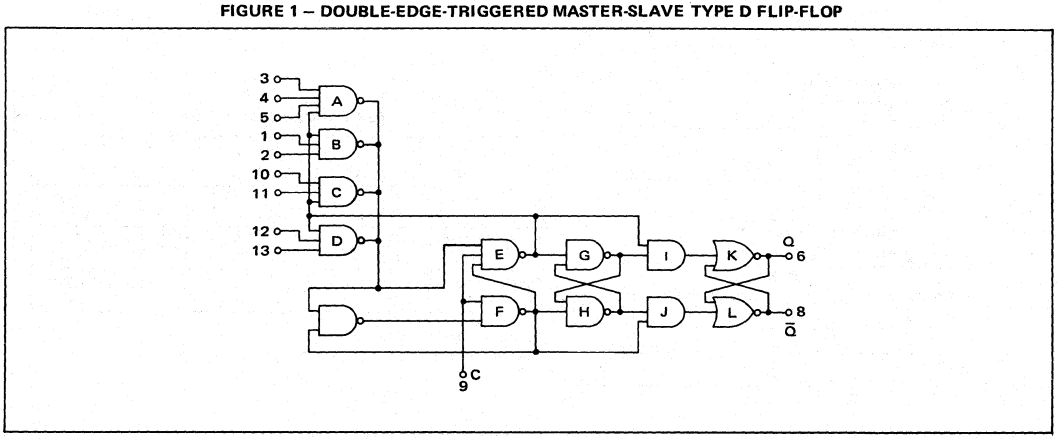
When negative-edge-triggered flip-flops are used to implement the shift register of Figure 2, the maximum allowable clock skew, Figure 3A, is the propagation delay from the falling edge of the clock to the output of flip-flop A minus the hold time of flip-flop B. It should be noted that the maximum propagation delay time and the minimum hold time from data sheets may not be used to calculate maximum allowable clock skew. Instead, the minimum propagation delay and maximum hold times must be used to calculate maximum clock skew to insure proper system operation over the entire temperature and power supply variations expected.

If the shift register of Figure 2 is constructed with master-slave flip-flops, the maximum allowable clock skew, Figure 3B, is the propagation delay from the falling edge of the clock to the output of flip-flop A plus the time required to transfer and latch the information into the master portion of flip-flop B. The minimum propagation delay and latch times must be used in calculating the maximum clock skew to guarantee proper system operation.

By using MC3153/3053 double-edge-triggered master-slave type D flip-flops in the circuit of Figure 2, the maximum clock skew, Figure 3C, is the propagation delay from the falling edge of the clock to the outout of flip-flop A minus the hold time of flip-flop B plus the clock pulse width. In this case, minimum propagation delay and maximum hold time must be used in the skew calculations. However, since the clock pulse width is part of the clock skew calculation, system clock skew can be adjusted to any value the system designer feels necessary to insure proper operation of the system simply by adjusting the clock pulse width. The ability to adjust clock skew is a feature that cannot be stressed too highly because it gives the system designer freedom from maximum allowable clock skew restrictions.

It should be noted in Figure 3C that the maximum clock frequency for the MC3153/3053 is the reciprocal of the propagation

FIGURE 1 – DOUBLE-EDGE-TRIGGERED MASTER-SLAVE TYPE D FLIP-FLOP



delay plus the hold time plus the system skew. Therefore, as the clock pulse width is increased to provide clock skew adjustment, the maximum operating frequency is reduced.

INPUT LOGIC UTILIZATION

The input logic available on the MC3153/3053 makes this flip-flop a very powerful logic block. Figure 4 shows four MC3153/3053's wired together to form a universal, clocked, shift register with the following features: (1) serial data entry and shift right, (2) parallel data entry, (3) shift left, and (4) hold the information (store). Since the $\overline{Q}$'s are also available, a one's complement could be formed by entering each $\overline{Q}$ back into its flip-flop. In this shift register, four MC3153/3053's replace four type D flip-flops of another type plus 4-wide AND-OR-INVERT gates.

FIGURE 2 – DIRECT-COUPLED SHIFT REGISTER

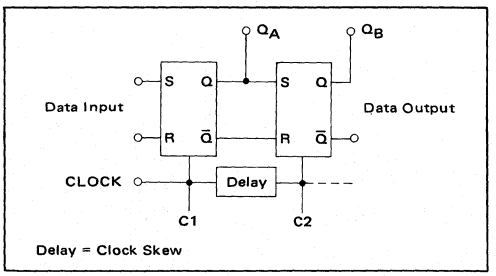
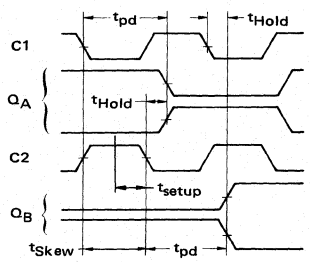


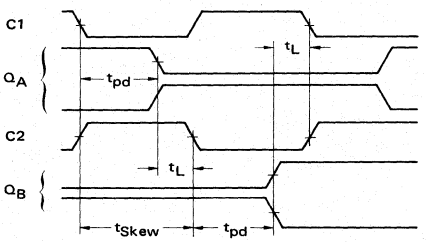
FIGURE 3 – CLOCK SKEW WAVEFORMS

FIGURE 3A – NEGATIVE-EDGE-TRIGGERED FLIP-FLOP



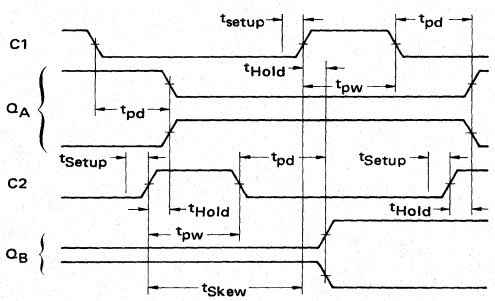
Maximum Clock Skew = $t_{pd} - t_{Hold}$
Minimum Clock Pulse Width (t_{pw}) = t_{Setup}

FIGURE 3B – MASTER-SLAVE FLIP-FLOP



Maximum Clock Skew = $t_{pd} + t_L$
Minimum Clock Pulse Width (t_{pw}) = t_L

FIGURE 3 C – DOUBLE-EDGE-TRIGGERED MASTER-SLAVE TYPE D FLIP-FLOP



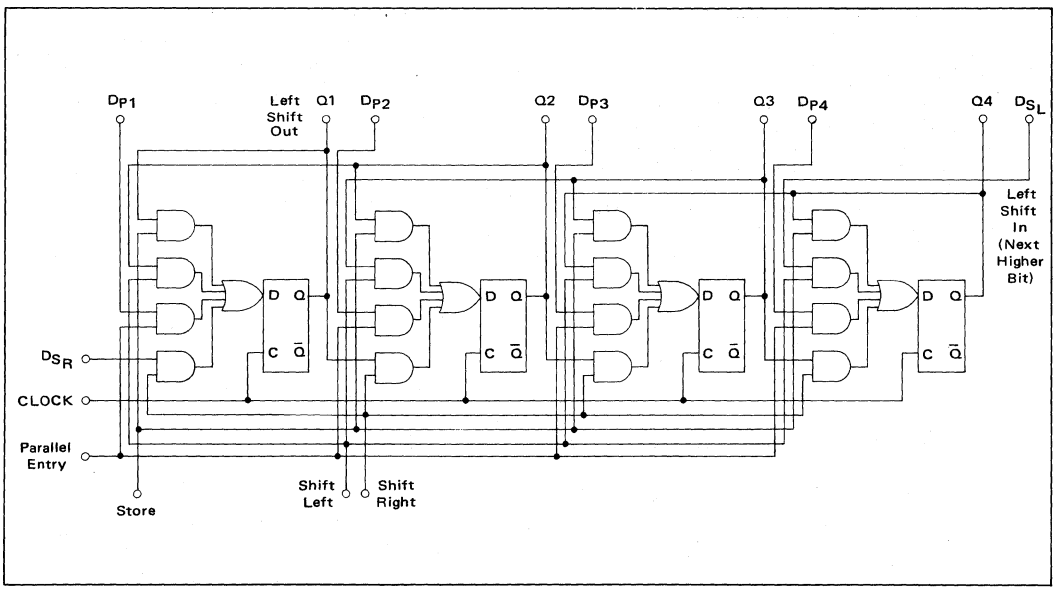
Maximum Clock Skew = $t_{pd} - t_{Hold} + t_{pw}$
Minimum Clock Pulse Width (t_{pw}) = t_{Hold}
Minimum Clock Period = $t_{Setup} + t_{pd} + t_{pw}$
(with $t_{pw} = t_{Skew} + t_{Hold} - t_{pd}$)
$= t_{Setup} + t_{pd} + t_{Skew} + t_{Hold} - t_{pd}$
$= t_{Setup} + t_{Skew} + t_{Hold}$

$$f_{max} = \frac{1}{t_{Setup} + t_{Skew} + t_{Hold}}$$

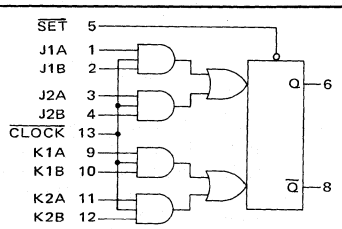
DEFINITIONS

t_{Hold}	Time data must be present after latching edge of clock to be recognized
t_L	Time to recognize and latch data in master portion of master-slave flip-flop
t_{pd}	Propagation delay from latching edge of clock to output
t_{Setup}	Time data must be present before latching edge of clock to be recognized
t_{Skew}	Clock skew time
t_{pw}	Clock positive pulse width

FIGURE 4 – UNIVERSAL CLOCKED SHIFT REGISTER



MC3154F • MC3054F
MC3154L • MC3054L, P
(54H71J) (74H71J, N)



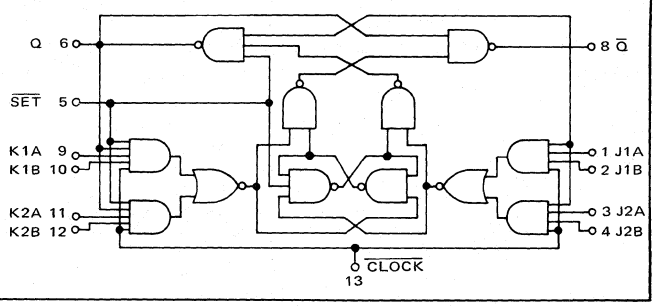
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

$J = J1A \cdot J1B + J2A \cdot J2B$
$K = K1A \cdot K1B + K2A \cdot K2B$

Input Loading Factor:
J, K = 1
$\overline{CLOCK}$ = 2
$\overline{SET}$ = 3
Output Loading Factor = 10

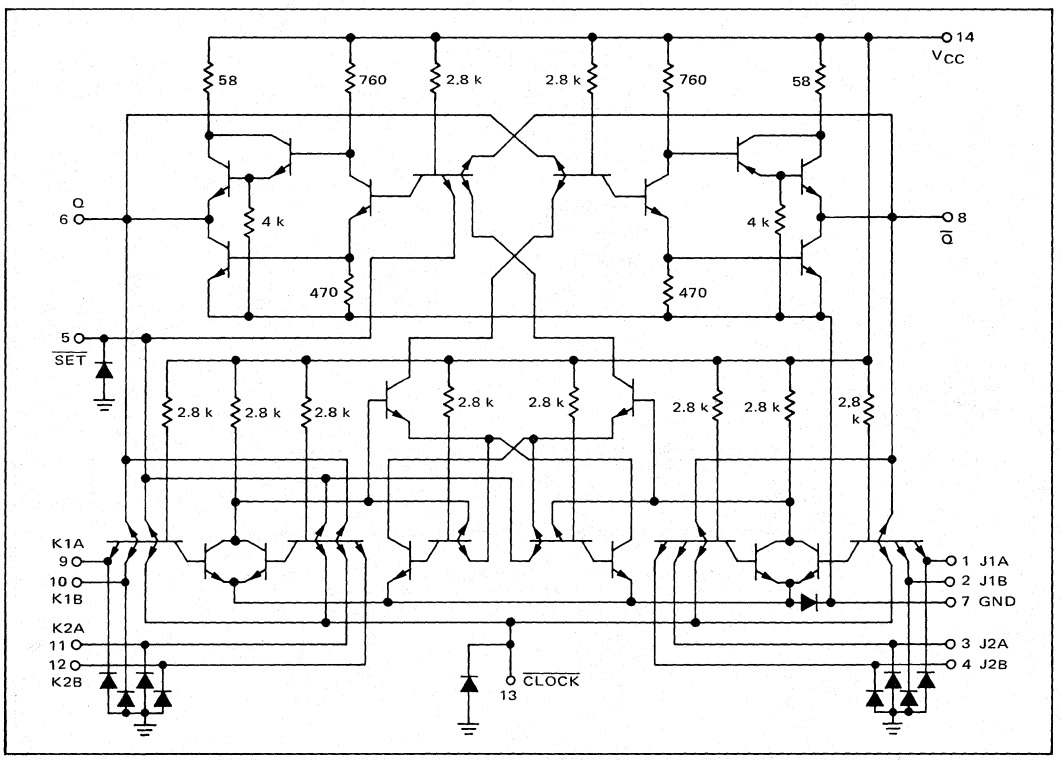
Total Power Dissipation = 95 mW typ/pkg
Propagation Delay Time = 20 ns typ
Operating Frequency = 30 MHz typ

This negative-edge clocked J-K Flip-Flop operates on the master-slave principle. AND-OR gate inputs enter data into the master section on the positive edge of the clock. This data is transferred to the slave section of the Flip-Flop on the negative edge of the clock. In order to assure entry of information into the Flip-Flop, data must not change after the positive edge of the clock.



Pin numbers for the 54H71F/74H71F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3154F,L/3054F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H71F/74H71F	5	6	7	8	9	10	11	12	1	2	13	14	3	4



See General Information section for packaging.

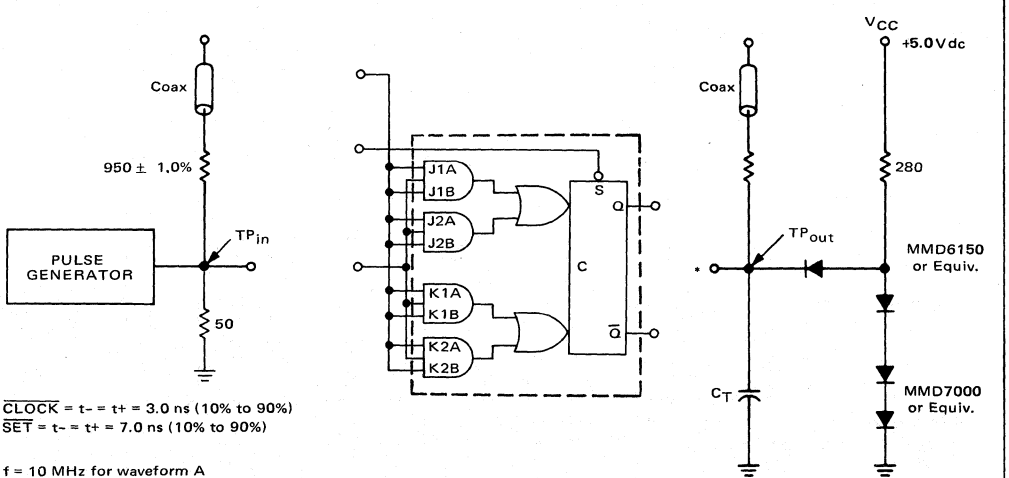
OPERATING CHARACTERISTICS

Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{SET}$ input will force the Q output to the logic "1" state. The $\overline{SET}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 12 ns minimum.

SWITCHING TIME TEST CIRCUIT



$\overline{CLOCK}$ = t- = t+ = 3.0 ns (10% to 90%)
$\overline{SET}$ = t- = t+ = 7.0 ns (10% to 90%)

f = 10 MHz for waveform A
1.0 MHz for waveforms B, E, and F

Two pulse generators are required and must be slaved together for testing $\overline{SET}$. Only one pulse generator is required for J, K, and $\overline{CLOCK}$ tests.

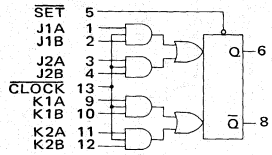
*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input on each AND gate, plus the SET and CLOCK inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA			Volts							
	I_{OL}	I_{OH}	I_{in}	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CCL}	V_{CCH}	
MC3154	20	-1.5	1.0	0.4	2.4	4.5	2.0	0.8	4.5	5.5	
MC3054	20	-1.5	1.0	0.4	2.4	4.5	2.0	0.8	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC3154 Test Limits −55 to +125°C Min	Max	Unit	MC3054 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CCL}	V_{CCH}	P_A**	Gnd
Input																				
Forward Current J1A	I_F	1	-	-2.0	mAdc	-	-2.0	mAdc	-	-	-	1	-	2,13	-	-	-	14	-	7,6
K1A		11	-	-2.0	↓	-	-2.0	↓	-	-	-	11	-	5**,12,13	-	-	-	↓	-	7
$\overline{\text{Set}}$		5	-	-6.0		-	-6.0		-	-	-	5	-	1,2,3,4,9,10,11,12,13	-	-	-		-	7
$\overline{\text{Clock}}$		13	-	-4.0		-	-4.0		-	-	-	13	-	1,2,3,4,5**,9,10,11,12	-	-	-		-	7
Clock		13	-	-4.0	↓	-	-4.0	↓	-	-	-	13	-	1,2,3,4,5,9,10,11,12	-	-	-	↓	-	7,6
Leakage Current J1A	I_{R1}	1	-	50	μAdc	-	50	μAdc	-	-	-	-	1	-	-	-	-	14	-	2,5,7,13
K1A		11	-	50	↓	-	50	↓	-	-	-	-	11	-	-	-	-	↓	-	5,6,7,12,13
$\overline{\text{Set}}$		5	-	150		-	150		-	-	-	-	5	-	-	-	-		-	6,7,9,10,11,12,13
$\overline{\text{Clock}}$		13	-	100		-	100		-	-	-	-	13	-	-	-	-		-	1,2,3,4,5,7,9,10,11,12
Clock		13	-	100	↓	-	100	↓	-	-	-	-	13	-	-	-	-	↓	-	1,2,3,4,5,6,7,9,10,11,12
J1A	BV_{in}	1	5.5*	-	Vdc	5.5*	-	Vdc	-	-	1	-	-	-	-	-	-	14	-	2,5,7,13
K1A		11	↓	-	↓	↓	-	↓	-	-	11	-	-	-	-	-	-	↓	-	5,6,7,12,13
$\overline{\text{Set}}$		5		-			-		-	-	5	-	-	-	-	-	-		-	6,7,9,10,11,12,13
$\overline{\text{Clock}}$		13		-			-		-	-	13	-	-	-	-	-	-			1,2,3,4,5,7,9,10,11,12
Clock		13	↓	-	↓	↓	-	↓	-	-	13	-	-	-	-	-	-	↓		1,2,3,4,5,6,7,9,10,11,12
Output																				
Output Voltage	V_{OL}	8	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	-	5	14	-	-	7,13
		6	-	0.4	Vdc	-	0.4	Vdc	6	-	-	-	-	-	9,10,11,12	1,2,3,4	14	-	13	7
	V_{OH}	6	2.4	-	Vdc	2.4	-	Vdc	-	6	-	-	-	-	-	5	14	-	-	7,13
		8	2.4	-	Vdc	2.4	-	Vdc	-	8	-	-	-	-	9,10,11,12	1,2,3,4	14	-	13	7
Short-Circuit Current	I_{SC}	6	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	1,2,3,4,9,10,11,12,13	-	-	-	14	-	5,6,7
		8	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	1,2,3,4,5,9,10,11,12,13	-	-	-	14	-	6,7,8†
Power Requirements																				
Power Supply Drain	I_{PD}	14	-	30	mAdc	-	30	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5,7,9,10,11,12,13
		14	-	30	mAdc	-	30	mAdc	-	-	-	-	-	1,2,3,4,5,9,10,11,12	-	-	-	14	-	7,13††

*Tested at 25°C only.

**Momentarily ground pin prior to taking measurement, then apply 4.5 volts. P_A = 4.5 V / 0 V

† Limit duration of test to 100 ns.

†† Momentary 4.5 V then apply gnd.

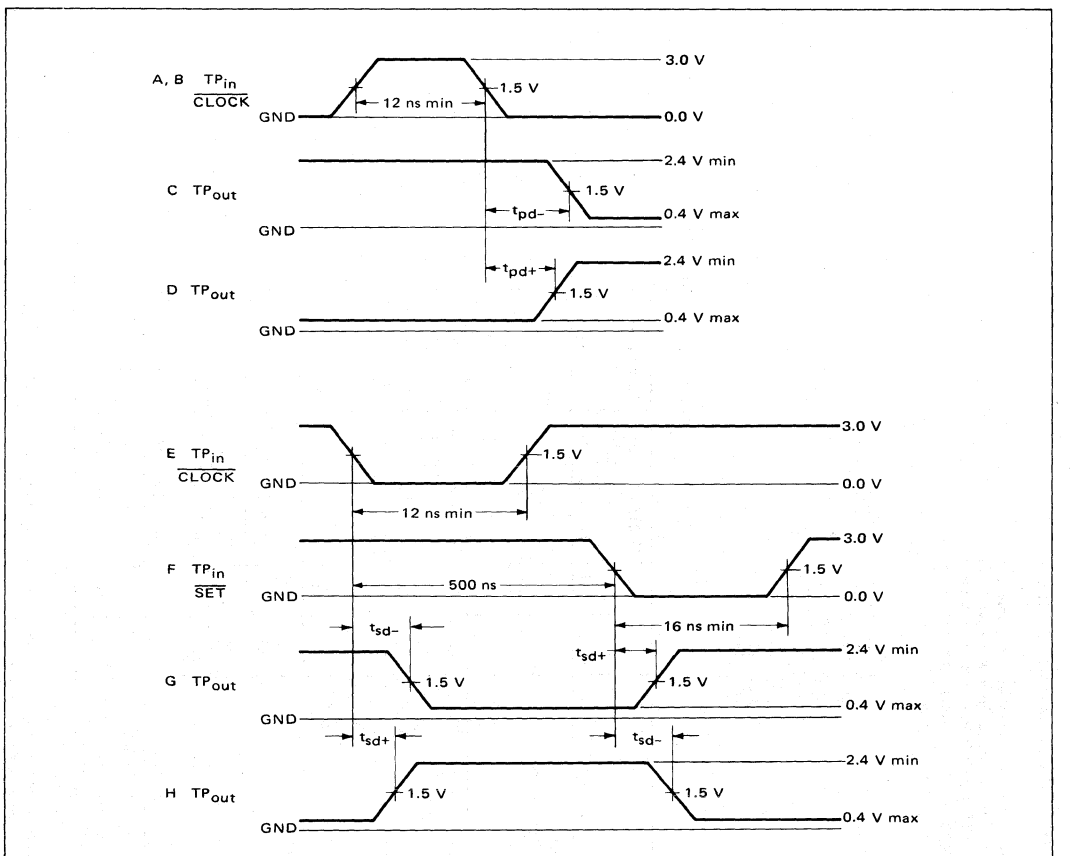
TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT			Q	$\overline{Q}$	LIMITS		
		$\overline{C}$	J, K	$\overline{S}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	2.4 V	2.4 V	†	†	25	–	MHz
Turn-On Delay	t_{pd-}	B	B	2.4 V	C	C	–	27	ns
Turn-Off Delay	t_{pd+}	B	B	2.4 V	D	D	–	21	ns
Turn-On Delay	t_{sd-}	E	2.4 V	F	G	H	–	24	ns
Turn-Off Delay	t_{sd+}	E	2.4 V	F	G	H	–	13	ns

†Output shall toggle with each input pulse.

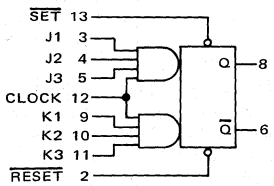
VOLTAGE WAVEFORMS AND DEFINITIONS



MC3155F • MC3055F
MC3155L • MC3055L, P

(54H72J) **(74H72J, N)**

This negative-edge-clocked J-K flip-flop operates on the master-slave principle. Three K inputs are ANDed together, and three J inputs are ANDed together. $\overline{SET}$ and $\overline{RESET}$ inputs are also available. The device helps minimize package count in J-K flip-flop applications requiring AND gating into the J or K inputs.



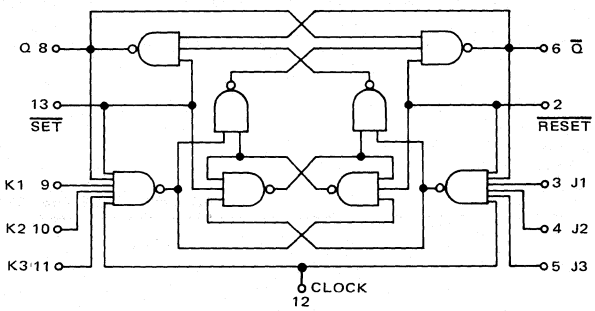
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

$J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$

Input Loading Factor:
J, K, CLOCK = 1
$\overline{SET}$, $\overline{RESET}$ = 2

Output Loading Factor = 10

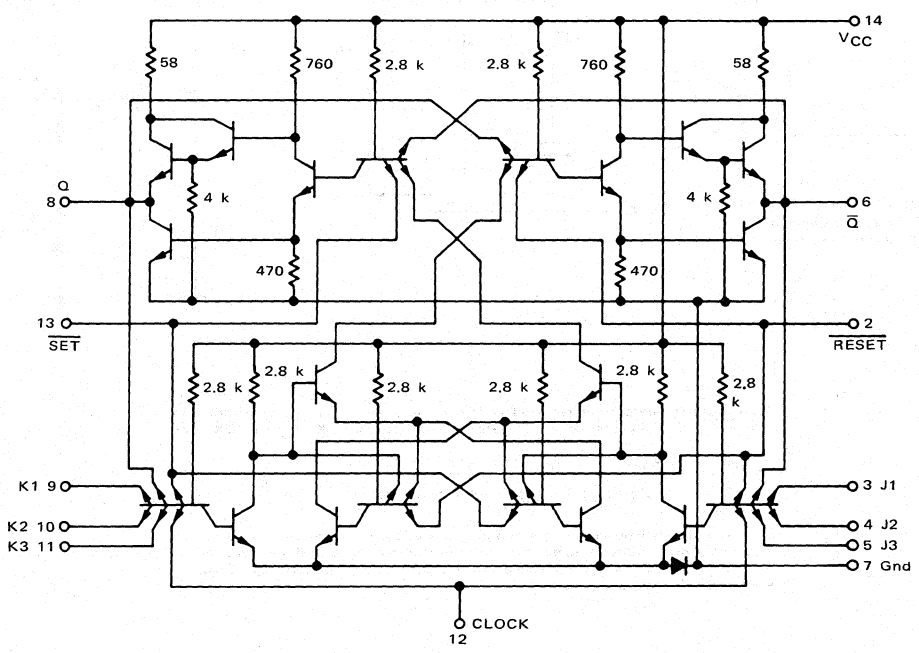
Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 10 ns typ
Operating Frequency = 30 MHz typ



Pin numbers for the 54H72F/74H72F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3155F,L/3055F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H72F/74H72F	6	5	7	8	9	10	11	12	1	13	14	2	3	4

CIRCUIT SCHEMATIC



See General Information section for packaging.

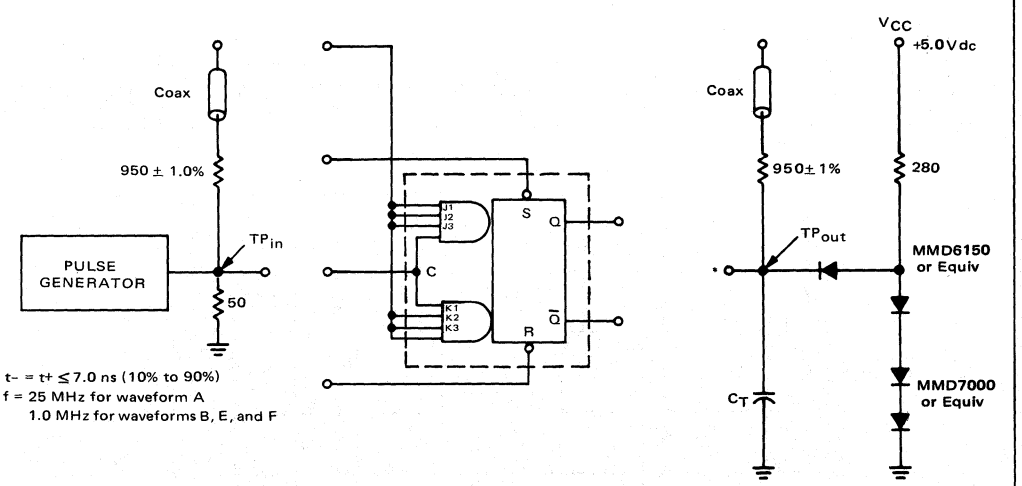
OPERATING CHARACTERISTICS

Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{SET}$ input will force the Q output to the logic "1" state, and application of a logic "0" to the $\overline{RESET}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{SET}$ and $\overline{RESET}$ inputs override the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 12 ns minimum.

SWITCHING TIME TEST CIRCUIT



t- = t+ ≤ 7.0 ns (10% to 90%)
f = 25 MHz for waveform A
1.0 MHz for waveforms B, E, and F

Two pulse generators are required and must be slaved together for testing $\overline{SET}$ and $\overline{RESET}$. Only one pulse generator is required for J, K, and CLOCK tests.

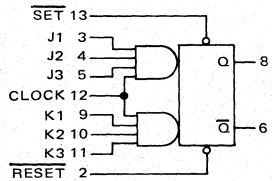
*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, plus the $\overline{SET}$, $\overline{RESET}$, and CLOCK inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



									TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
									mA			Volts						
									I_{OL}	I_{OH}	I_{in}	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CCL}	V_{CCH}
								MC3155	20	-2.0	1.0	0.4	2.4	4.0	2.0	0.8	4.5	5.5
								MC3055	20	-2.0	1.0	0.4	2.4	4.0	2.0	0.8	4.75	5.25

Characteristic		Symbol	Pin Under Test	MC3155 Test Limits −55 to +125°C Min	Max	Unit	MC3055 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CCL}	V_{CCH}	Gnd
Input																				
Forward Current	J	I_F	3	-	-2.0	mAdc	-	-2.0	mAdc	-	-	-	3	-	2*, 4, 5, 12	-	-	-	14	7
	K		9	-	-2.0		-	-2.0		-	-	-	9	-	10, 11, 12, 13*	-	-	-		
	$\overline{Set}$		13	-	-4.0		-	-4.0		-	-	-	13	-	3, 4, 5, 9, 10, 11	-	-	-		
	$\overline{Reset}$		2	-	-4.0		-	-4.0		-	-	-	2	-	3, 4, 5, 9, 10, 11	-	-	-		
	Clock		12	-	-2.0		-	-2.0		-	-	-	12	-	2*, 3, 4, 5, 9, 10, 11	-	-	-		
			12	-	-2.0	↓	-	-2.0	↓	-	-	-	12	-	3, 4, 5, 9, 10, 11, 13*	-	-	-	↓	↓
Leakage Current	J	I_{R1}	3	-	50	μAdc	-	50	μAdc	-	-	-	-	3	-	-	-	-	14	2,4,5,7,12
	K		9	-	50		-	50		-	-	-	-	9	-	-	-	-		7,10,11,12,13
	$\overline{Set}$		13	-	100		-	100		-	-	-	-	13	-	-	-	-		7,9,10,11,12
	$\overline{Reset}$		2	-	100		-	100		-	-	-	-	2	-	-	-	-		3,4,5,7,12
	Clock		12	-	50	↓	-	50	↓	-	-	-	-	12	-	-	-	-	↓	2,3,4,5,7,9,10,11,13
	J	BV_{in}	3	5.5**	-	Vdc	5.5**	-	Vdc	-	-	3	-	-	-	-	-	-	14	2,4,5,7,12
	K		9	↓	-	↓	↓	-	↓	-	-	9	-	-	-	-	-	-		7,10,11,12,13
	$\overline{Set}$		13		-			-		-	-	13	-	-	-	-	-	-		7,9,10,11,12
	$\overline{Reset}$		2		-			-		-	-	2	-	-	-	-	-	-		3,4,5,7,12
	Clock		12	↓	-	↓	↓	-	↓	-	-	12	-	-	-	-	-	-	↓	2,3,4,5,7,9,10,11,13
Output																				
Output Voltage		V_{OL}	6	-	0.4	Vdc	-	0.4	Vdc	6	-	-	-	-	-	2	13	14	-	7
			8	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	13	2	14	-	7
		V_{OH}	6	2.4	-	Vdc	2.4	-	Vdc	-	6	-	-	-	-	13	2	14	-	7
			8	2.4	-	Vdc	2.4	-	Vdc	-	8	-	-	-	-	2	13	14	-	7
Short-Circuit Current		I_{SC}	6	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	14	2, 6, 7, 12
			8	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	14	7, 8, 12, 13
Power Requirements																				
Power Supply Drain		I_{PD}	14	-	25	mAdc	-	25	mAdc	-	-	-	-	-	-	-	-	-	14	2,3,4,5,7,9,10,11,12
			14	-	25	mAdc	-	25	mAdc	-	-	-	-	-	-	-	-	-	14	3,4,5,7,9,10,11,12,13

*Momentarily ground pin prior to taking measurement.
**Tested @ 25°C only.

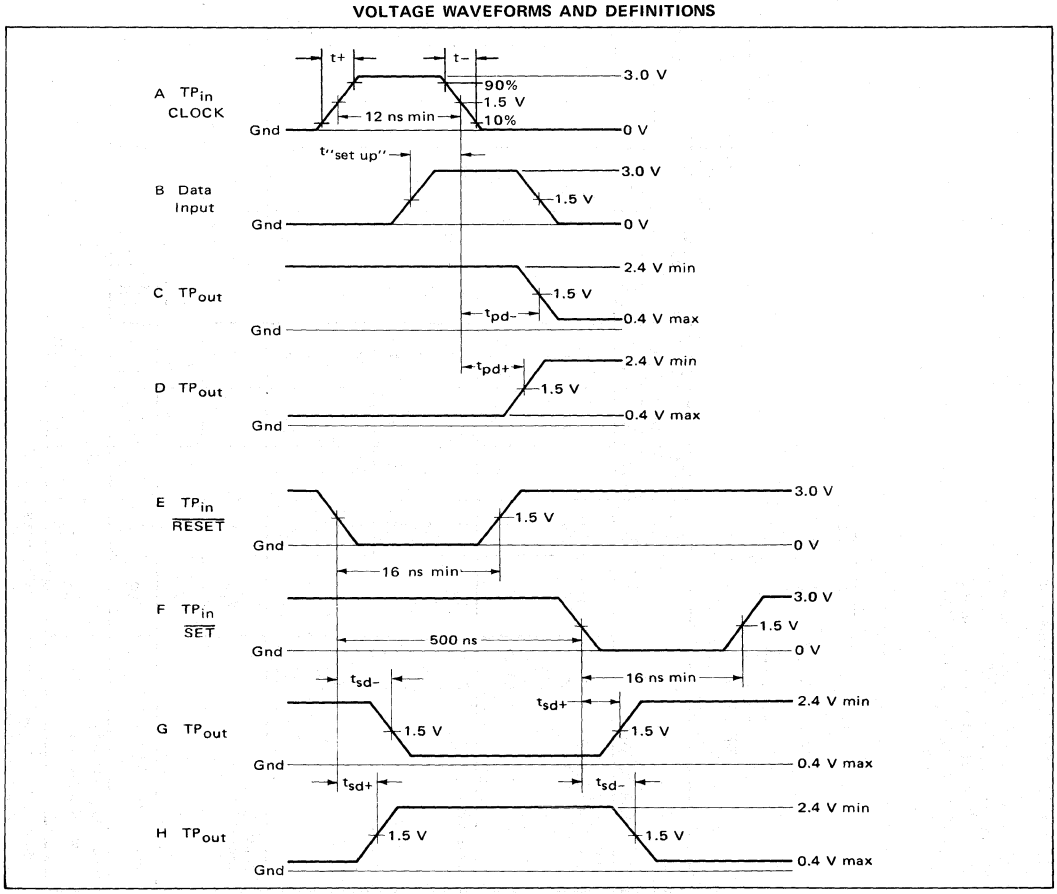
TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

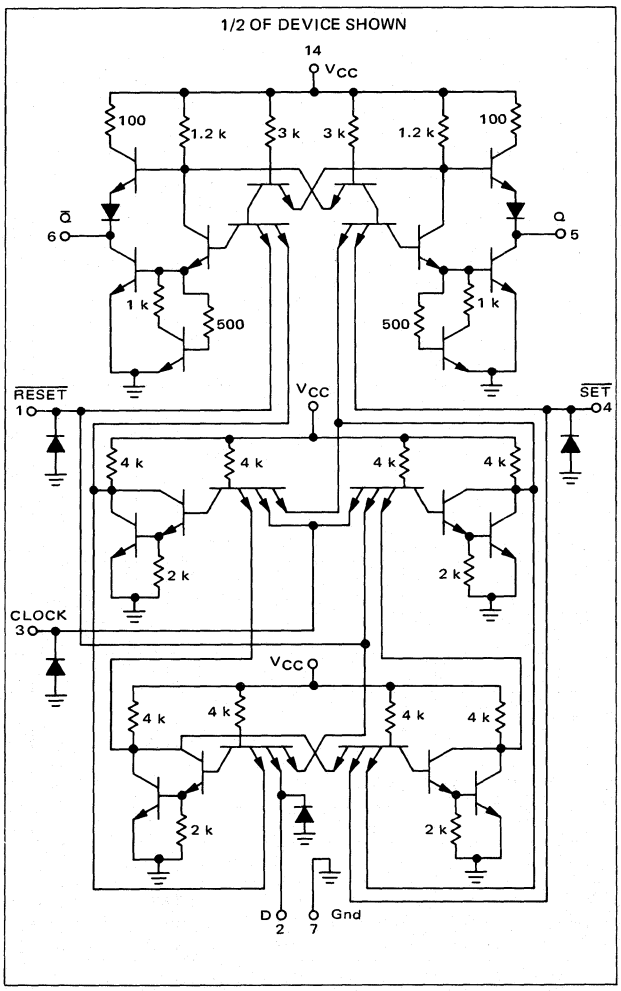
TEST	SYMBOL	INPUT				Q	$\bar{Q}$	LIMITS		
		C	J, K	$\bar{R}$	$\bar{S}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	A	2.4 V	2.4 V	†	†	25	–	MHz
Turn-On Delay	t_{pd-}	B	B	2.4 V	2.4 V	C	D	–	27	ns
Turn-Off Delay	t_{pd+}	B	B	2.4 V	2.4 V	C	D	–	21	ns
Turn-On Delay	t_{sd-}	2.4 V	2.4 V	E	F	G	H	–	24	ns
Turn-Off Delay	t_{sd+}	2.4 V	2.4 V	E	F	G	H	10	13	ns
Enable Voltage ☆	V_{EN}	B	2.0 V	2.4 V	2.4 V	†	†	†	–	–
Inhibit Voltage ☆	V_{INH}	B	0.8 V	2.4 V	2.4 V	‡	‡	‡	–	–

†Output shall toggle with each input pulse.
‡Output shall NOT toggle.
☆Tested at all temperatures.

VOLTAGE WAVEFORMS AND DEFINITIONS



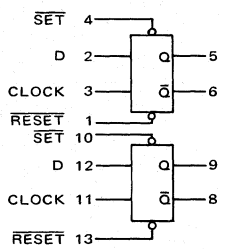
MC3160F • MC3060F
MC3160L • MC3060L,P



This dual flip-flop triggers on the positive edge of the clock and performs the Type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct $\overline{SET}$ and $\overline{RESET}$ inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the Setup and Hold times. The clocked inputs are inhibited when the clock is high and data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Setup and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Q and $\overline{Q}$ respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs.



TRUTH TABLE

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

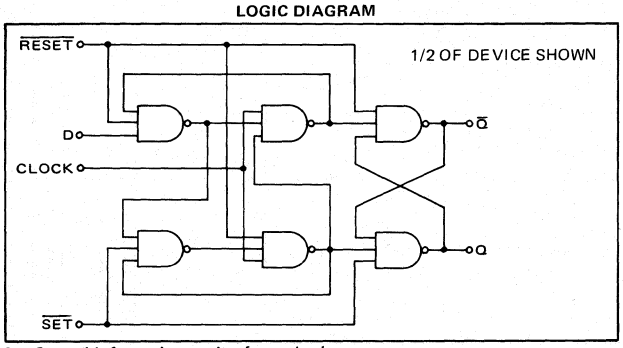
$Q^{n+1} = D^n$

Input Loading Factors:
- $\overline{SET}$ = 1.15
- $\overline{RESET}$ = 1.7
- CLOCK= 1.5
- D = 0.75

Output Loading Factor = 10

Typical Characteristics: (V_{CC} = 5.0 V, T_A = 25°C)
- Total Power Dissipation = 120 mW/pkg
- Toggle Frequency = 30 MHz
- Logical "1" Setup Time = 10 ns
- Logical "0" Setup Time = 5.0 ns
- Logical "1" and "0" Hold Times = 5.0 ns
- t_{pd-} = 17 ns
- t_{pd+} = 15 ns

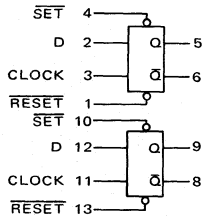
LOGIC DIAGRAM



See General Information section for packaging

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}
MC3160	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	4.5	5.5
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	4.5	5.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	4.5	5.5
MC3060	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	4.75	5.75
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	4.75	5.75
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	4.75	5.75

Characteristic	Symbol	Pin Under Test	MC3160 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3060 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}	P_1*	Gnd
Input																													
Forward Current	I_{FC}	3	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	3	-	1	-	-	14	-	2,4,7,11
	$I_{F\bar{D}}$	2	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	2	-	1,4	-	-	14	-	3,7,11
	$I_{F\bar{S}}$	4	-	-2.3	-	-2.3	-	-2.3	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	4	-	1	-	-	14	-	2,3,7,11
	$I_{F\bar{R}}$	1	-	-3.4	-	-3.4	-	-3.4	-	-3.4	-	-3.4	-	-3.4	mAdc	-	-	-	-	-	-	1	-	2,4	-	-	14	-	3,7,11
Leakage Current	I_{RC}	3	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	3	4	-	-	14	-	1,2,7,11
	I_{RD}	2	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	2	3,4	-	-	14	-	1,7,11
	$I_{R\bar{S}}$	4	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	4	1,2	-	-	14	3	7,11
	$I_{R\bar{R}}$	1	-	140	-	140	-	140	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	1	4	-	-	14	3	2,7,11
Breakdown Voltage	BV_{in}	3	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	3	-	-	-	-	-	4	-	-	14	-	1,2,7,11
		2	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	2	-	-	-	-	-	3,4	-	-	↓	-	1,7,11
		4	-	-		-	-	-	-	-		-	-	-		-	-	4	-	-	-	-	-	1,2	-	-		3	7,11
		1	-	-		-	-	-	-	-		-	-	-		-	-	1	-	-	-	-	-	4	-	-		3	2,7,11
Clamp Voltage	V_D	3	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	3	-	-	-	-	-	-	14	-	-	7,11
		2	-	-	-	↓	-	-	-	-	-	↓	-	-	↓	-	-	-	2	-	-	-	-	-	-	↓	-	-	↓
		4	-	-	-		-	-	-	-	-		-	-		-	-	-	4	-	-	-	-	-	-		-	-	
		1	-	-	-		-	-	-	-	-		-	-		-	-	-	1	-	-	-	-	-	-		-	-	
Output																													
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	4	1	-	-	-	-	14	-	-	2,3,7,11
		5	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	5	-	-	-	1	4	-	-	-	-	14	-	-	2,3,7,11
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	1	4	-	-	-	-	14	-	-	2,3,7,11
		5	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	5	-	-	4	1	-	-	-	-	14	-	-	2,3,7,11
Short-Circuit Current	I_{SC}	6	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	4	1	-	-	-	-	14	-	6,7,11
		5	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	1	4	-	-	-	-	14	-	5,7,11
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	42	-	-	-	-	-	42	-	-	mAdc	-	-	-	-	-	-	-	-	1,13	14	-	-	-	3,4,7,10,11
Power Supply Drain	I_{PD}	14	-	31	-	31	-	31	-	31	-	31	-	31	mAdc	-	-	-	-	-	-	-	-	4,10	-	-	14	-	1,3,7,11,13

* Pulse is used to set flip-flop in desired state. P_1 = 4.0 V (V_{RH}), 0 V. If pin is also in another column, the pin must be returned to that voltage or current for measurement.

OPERATING CHARACTERISTICS

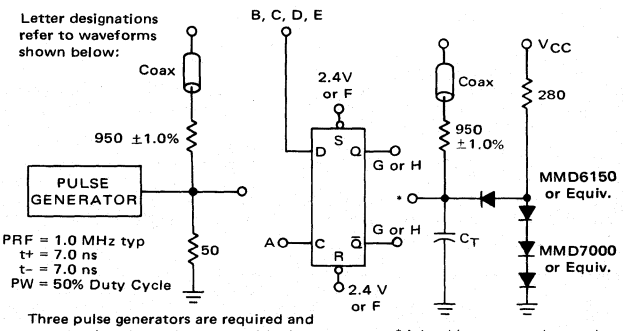
Data must be present 15 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

The direct $\overline{SET}$ and $\overline{RESET}$ inputs may be used at any time as they completely override the clock.

Positive edge triggering: When the clock goes from the low to the high state, the information in the input steering section is transferred to the bistable section.

Unused inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

SWITCHING TIME TEST CIRCUIT



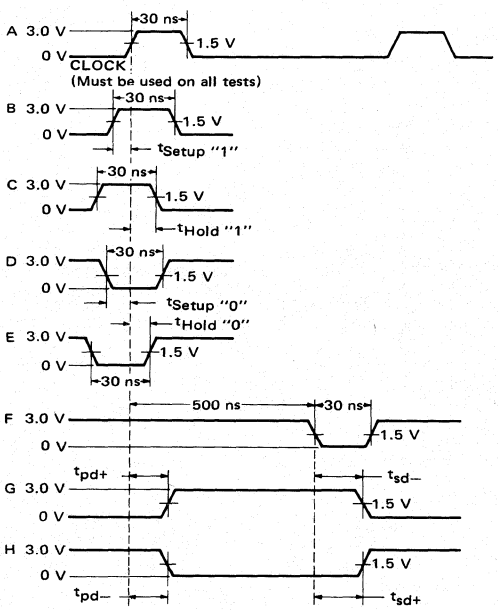
Three pulse generators are required and must be slaved together to provide the waveforms shown.

*A load is connected to each output during the test.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT D*	INPUT $\overline{SET}$*	INPUT $\overline{RESET}$*	Q*	$\overline{Q}$*	LIMITS (ns) Min	LIMITS (ns) Max
t_{Setup} "1" D	B	2.4 V	F	G	H	–	15
t_{Hold} "1" D	C	2.4 V	F	G	H	–	5.0
t_{Setup} "0" D	D	F	2.4 V	H	G	–	15
t_{Hold} "0" D	E	F	2.4 V	H	G	–	5.0
t_{pd+}	Delay from clock to Q during t_{Setup} "1" D test. Delay from clock to $\overline{Q}$ during t_{Setup} "0" D test.					10	25
t_{pd-}	Delay from clock to Q during t_{Setup} "0" D test. Delay from clock to $\overline{Q}$ during t_{Setup} "1" D test.					10	25
t_{sd+}	Delay from $\overline{SET}$ to Q during t_{Setup} "0" D test. Delay from $\overline{RESET}$ to $\overline{Q}$ during t_{Setup} "1" D test.					5.0	20
t_{sd-}	Delay from $\overline{SET}$ to $\overline{Q}$ during t_{Setup} "0" D test. Delay from $\overline{RESET}$ to Q during t_{Setup} "1" D test.					5.0	20

*Letters shown in these columns refer to waveforms at left.

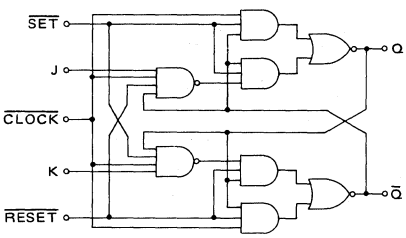
MC3161F • MC3061F
MC3161L • MC3061L,P

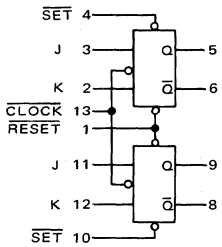
This dual JK flip-flop triggers on the negative edge of clock. Each flip-flop is provided with a separate direct $\overline{SET}$ input in addition to the common direct $\overline{RESET}$ input. These direct inputs provide a means of resetting a group of flip-flops such as a register which may be followed by the presetting of a data pattern. The clock input for this device is common for both flip-flops, making it particularly useful in registers or other common clock applications.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between the Setup and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between the Set-up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the $\overline{SET}$ input. In addition, both flip-flops may be reset simultaneously by using the common $\overline{RESET}$ in a similar manner.

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN

$\overline{RESET}$ AND $\overline{CLOCK}$ COMMON TO BOTH





Input Loading Factors:
$\overline{SET}$ = 1.75
$\overline{RESET}$, $\overline{CLOCK}$ = 3.7
J, K = 0.75

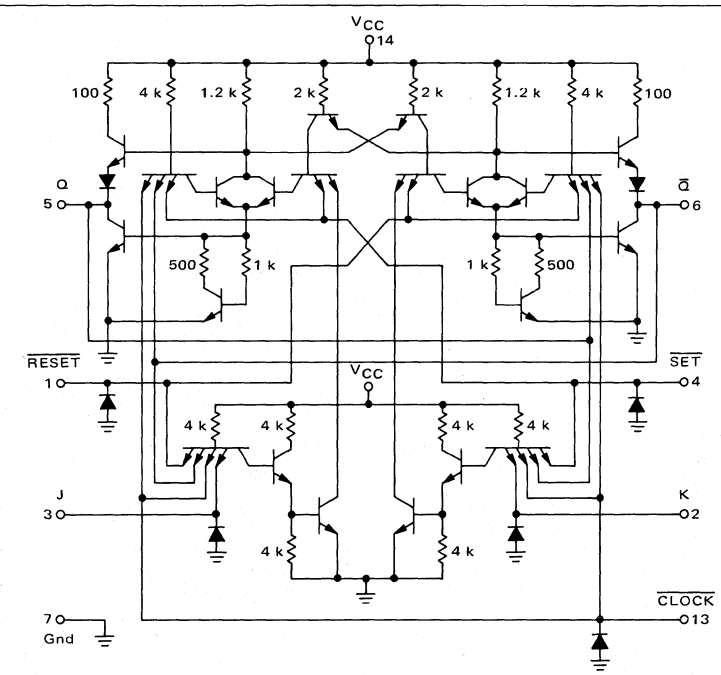
Output Loading Factor = 10

J-K TRUTH TABLE

J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Typical Characteristics
(V_{CC} = 5.0 V; T_A = 25°C)

Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz typ
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
t_{pd-} = 12 ns
t_{pd+} = 12 ns

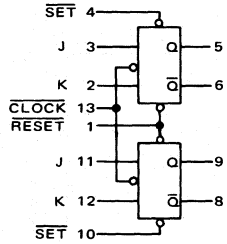


CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN
(RESET AND CLOCK
COMMON TO BOTH)

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop plus the inputs common to both flip-flops. To complete testing, sequence through the remaining inputs in the same manner.



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES: mA I_{OL}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}
MC3161 −55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	4.5	5.5
MC3161 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	4.5	5.5
MC3161 +125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	4.5	5.5
MC3061 0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	4.75	5.25
MC3061 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	4.75	5.25
MC3061 +75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC3161 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3061 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}	P_1*	Gnd
Input																													
Forward Current	I_{FJ}	3	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	3	-	1,4,13	-	-	14	1	2,7
	I_{FK}	2	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	2	-	1,4,13	-	-	14	4	3,7
	$I_{F\overline{R}}$	1	-	-3.5	-	-3.5	-	-3.5	-	-3.5	-	-3.5	-	-3.5	mAdc	-	-	-	-	-	-	1	-	3,4,10,13	-	-	14	-	2,7
	$I_{F\overline{S}}$	4	-	-1.8	-	-1.8	-	-1.8	-	-1.8	-	-1.8	-	-1.8	mAdc	-	-	-	-	-	-	4	-	1,2,13	-	-	14	-	3,7
	$I_{F\overline{C}}$	13	-	-5.7	-	-5.7	-	-5.7	-	-5.7	-	-5.7	-	-5.7	mAdc	-	-	-	-	-	-	13	-	1,2,3,11,12	-	-	14	4,10	7
Leakage Current	I_{RJ}	3	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	3	2,4	-	-	14	-	1,7,13
	I_{RK}	2	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	2	1,3	-	-	14	-	4,7,13
	$I_{R\overline{R}}$	1	-	200	-	200	-	200	-	200	-	200	-	200	μAdc	-	-	-	-	-	-	-	1	2	-	-	14	1	3,4,7,11,13
	$I_{R\overline{S}}$	4	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	-	-	4	3	-	-	14	4	1,2,7,10,13
	$I_{R\overline{C}}$	13	-	300	-	300	-	300	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	13	-	-	-	14	-	1,2,3,4,7,10,11,12
Breakdown Voltage	BV_{in}	3	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	3	-	-	-	-	-	2,4	-	-	14	-	1,7,10,13
		2	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	2	-	-	-	-	-	1,3	-	-	↓	-	4,7,10,13
		1	-	-		-	-	-	-	-		-	-	-		-	-	1	-	-	-	-	-	2	-	-		1	3,4,7,11,13
		4	-	-		-	-	-	-	-		-	-	-		-	-	4	-	-	-	-	-	3	-	-		4	1,2,7,10,13
		13	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	13	-	-	-	-	-	-	-	-	↓	-	1,2,3,4,7,10,11,12
Clamp Voltage	V_D	3	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	3	-	-	-	-	-	-	14	-	-	7,10
		2	-	-	-	↓	-	-	-	-	-	↓	-	-	↓	-	-	-	2	-	-	-	-	-	-	↓	-	-	↓
		1	-	-	-		-	-	-	-	-		-	-		-	-	-	1	-	-	-	-	-	-		-	-	
		4	-	-	-		-	-	-	-	-		-	-		-	-	-	4	-	-	-	-	-	-		-	-	
		13	-	-	-	↓	-	-	-	-	-	↓	-	-	↓	-	-	-	13	-	-	-	-	-	-	↓	-	-	↓
Output																													
Output Voltage	V_{OL}	5	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	5	-	-	-	1	4	-	-	-	-	14	-	1	7,10
		6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	4	1	-	-	-	-	14	-	4	7,10
	V_{OH}	5	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	5	-	-	4	1	-	-	-	-	14	-	4	7,10
		6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	1	4	-	-	-	-	14	-	1	7,10
Short-Circuit Current	I_{SC}	5	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	4,5,7,10
		6	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	1,6,7,10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	42	-	-	-	-	-	42	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	4,7,10
Power Supply Drain	I_{PD}	14	-	32	-	32	-	32	-	32	-	32	-	32	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	1,7

*Momentarily ground pin prior to taking measurement. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

OPERATING CHARACTERISTICS

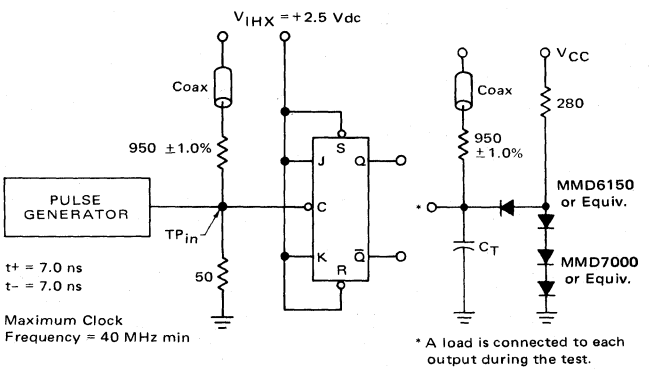
High state data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The direct $\overline{SET}$ (individual) inputs and $\overline{RESET}$ (common) inputs may be used at any time without regard to the clock state. The flip-flop is set to the Q = 1 state by applying a low level to the $\overline{SET}$ input or reset to the Q = 0 state by applying a low level to the $\overline{RESET}$ input. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering – The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low. The clock fall time must be less than 50 ns.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

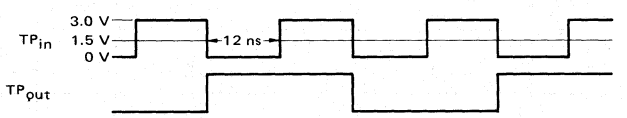
MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

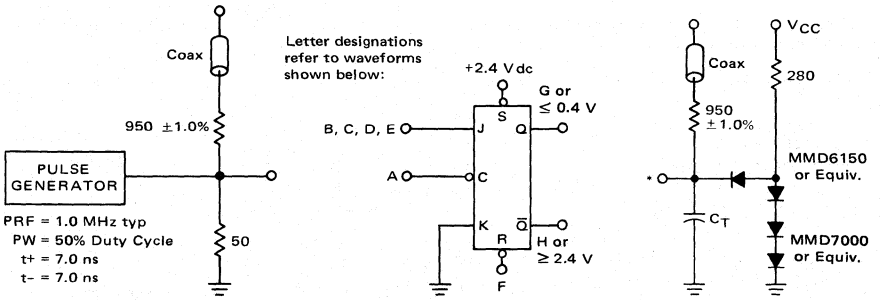
VOLTAGE WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs and $\overline{\text{RESET}}$ Input; to test other inputs, refer to Test Procedures Chart)



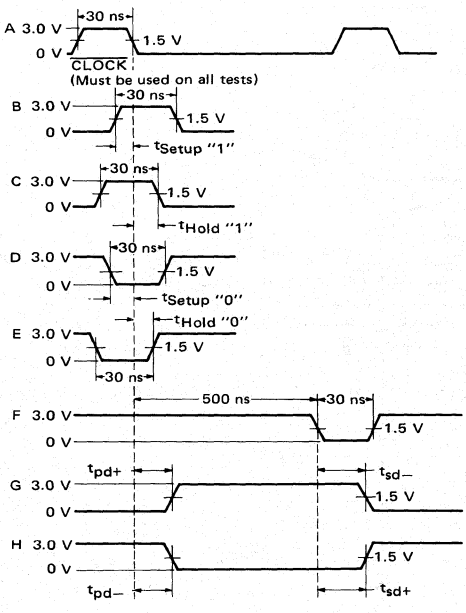
Three pulse generators are required and must be slaved together to provide the waveforms shown.

*A load is connected to each output during the test.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT J*	SET*	RESET*	K*	Q*	Q̄*	LIMITS (ns) Max
t_{Setup} "1" J	B	2.4 V	F	Gnd	G	H	15
t_{Hold} "1" J	C	2.4 V	F	Gnd	G	H	0**
t_{Setup} "0" J	D	2.4 V	F	Gnd	≤0.4 V	≥2.4 V	15
t_{Hold} "0" J	E	2.4 V	F	Gnd	≤0.4 V	≥2.4 V	0**
t_{Setup} "1" K	Gnd	F	2.5 V	B	H	G	15
t_{Hold} "1" K	Gnd	F	2.5 V	C	H	G	0**
t_{Setup} "0" K	Gnd	F	2.5 V	D	≥2.4 V	≤0.4 V	15
t_{Hold} "0" K	Gnd	F	2.5 V	E	≥2.4 V	≤0.4 V	0**
t_{pd+}	Delay from CLOCK to Q during t_{Setup} "1" J test. Delay from CLOCK to Q̄ during t_{Setup} "1" K test.						18
t_{pd-}	Delay from CLOCK to Q̄ during t_{Setup} "1" J test. Delay from CLOCK to Q during t_{Setup} "1" K test.						18
t_{sd+}	Delay from SET to Q during t_{Setup} "1" K test. Delay from RESET to Q̄ during t_{Setup} "1" J test.						18
t_{sd-}	Delay from SET to Q̄ during t_{Setup} "1" K test. Delay from RESET to Q during t_{Setup} "1" J test.						18

*Letters shown in these columns refer to waveforms shown at the left.

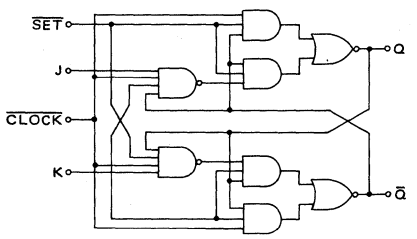
**t_{Hold} is typically a negative number.

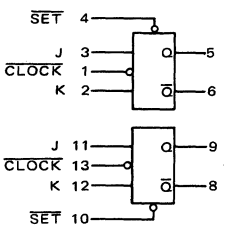
MC3162F • MC3062F
MC3162L • MC3062L,P

This dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct $\overline{SET}$ input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between the Set up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the $\overline{SET}$ input.

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN





Input Loading Factors:
$\overline{CLOCK}$, $\overline{SET}$ = 1.75
J, K, = 0.75

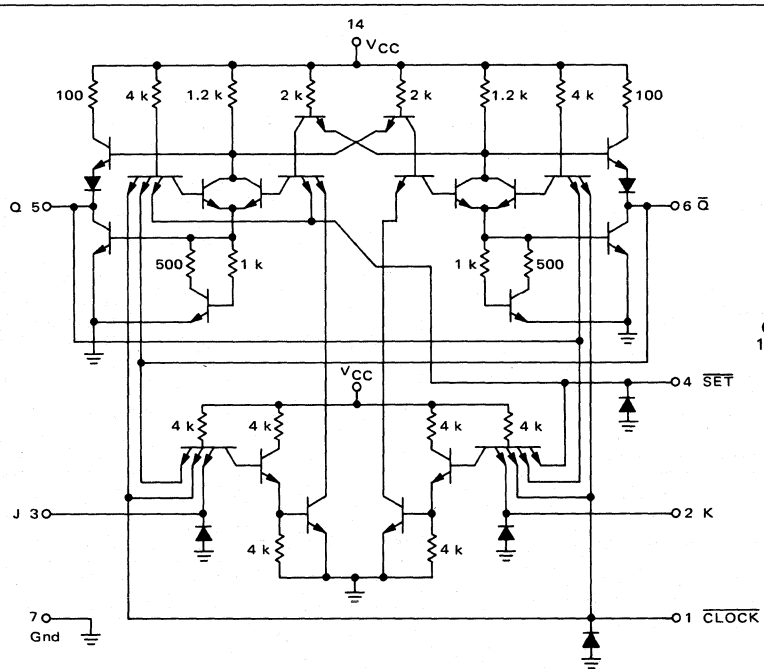
Output Loading Factor = 10

J-K TRUTH TABLE

J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Typical Characteristics:
(V_{CC} = 5.0 V; T_A = 25°C)

Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz typ
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
t_{pd+} = 12 ns
t_{pd-} = 12 ns

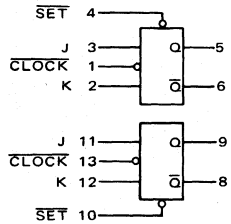


CIRCUIT SCHEMATIC
1/2 OF DEVICE SHOWN

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES										
		mA				Volts						
		I_{OL}	I_{OH}	I_{in}	I_D	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}	
MC3162	−55°C	20	-2.0	-	-	0.4	2.4	4.0	-	4.5	5.5	
	+25°C	20	-2.0	1.0	-10	0.4	2.4	4.0	7.0	4.5	5.5	
	+125°C	20	-2.0	-	-	0.4	2.4	4.0	-	4.5	5.5	
MC3062	0°C	20	-2.0	-	-	0.4	2.5	4.0	-	4.75	5.25	
	+25°C	20	-2.0	1.0	-10	0.4	2.5	4.0	7.0	4.75	5.25	
	+75°C	20	-2.0	-	-	0.4	2.5	4.0	-	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC3162 Test Limits −55°C Min	MC3162 Test Limits −55°C Max	MC3162 Test Limits +25°C Min	MC3162 Test Limits +25°C Max	MC3162 Test Limits +125°C Min	MC3162 Test Limits +125°C Max	MC3062 Test Limits 0°C Min	MC3062 Test Limits 0°C Max	MC3062 Test Limits +25°C Min	MC3062 Test Limits +25°C Max	MC3062 Test Limits +75°C Min	MC3062 Test Limits +75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_F	V_R	V_{RH}	V_{max}	V_{CCL}	V_{CCH}	P_1*	Gnd
Input																											
Forward Current	I_F	2	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	2,6	-	1,4	-	-	14	-	3,7,13
		3	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	3,5	-	1,4	-	-	14	-	2,7,13
	$I_{F\overline{S}}$	4	-	-4.7	-	-4.7	-	-4.7	-	-4.7	-	-4.7	-	-4.7	mAdc	-	-	-	-	4,6	-	1,2	-	-	14	-	3,7,13
	$I_{F\overline{C}}$	1	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	1,6	-	2,3	-	-	14	4	7,13
		1	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	1,5	-	2,3,4	-	-	14	-	7,13
Leakage Current	I_R	2	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	2	3	-	-	14	-	1,4,7,13
		3	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	3	2	-	-	14	-	1,4,7,13
	$I_{R\overline{S}}$	4	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	4	3	-	-	14	-	1,2,7,13
	$I_{R\overline{C}}$	1	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	1	-	-	-	14	-	2,3,4,7,13
Breakdown Voltage	BV_{in}	2	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	-	14	-	1,4,7,13
		3	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	3	-	-	-	-	-	-	↓	-	1,4,7,13
		4	-	-		-	-	-	-	-		-	-	-		-	-	4	-	-	-	-	-	-		-	1,2,7,13
		1	-	-		-	-	-	-	-		-	-	-		-	-	1	-	-	-	-	-	-		-	2,3,4,7,13
Clamp Voltage	V_D	2	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	2	-	-	-	-	14	-	-	7,13
		3	-	-	-	↓	-	-	-	-	-	↓	-	-	↓	-	-	-	3	-	-	-	-	↓	-	-	↓
		4	-	-	-		-	-	-	-	-		-	-		-	-	-	4	-	-	-	-		-	-	
		1	-	-	-		-	-	-	-	-		-	-		-	-	-	1	-	-	-	-		-	-	
Output																											
Output Voltage	V_{OL}	5	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	5	-	-	-	-	-	-	-	14	-	5	1,7,13
		6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	4	-	-	-	14	-	4	1,7,13
	V_{OH}	5	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	5	-	-	4	-	-	-	14	-	4	7
		6	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	-	4	-	14	-	5	1,7,13
Short-Circuit Current	I_{SC}	5	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	-	-	-	14	-	4,5,7,13
Power Requirements (Total Device)																											
Maximum Power Supply Current	I_{max}	14	-	-	-	41	-	-	-	-	-	41	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	4,7,10
Power Supply Drain	I_{PD}	14	-	31	-	31	-	31	-	31	-	31	-	31	mAdc	-	-	-	-	-	-	-	-	-	14	-	4,7,10

* Momentarily ground pin prior to taking measurement. (If pin is also in another column the pin must be returned to that voltage or current for measurement.)

OPERATING CHARACTERISTICS

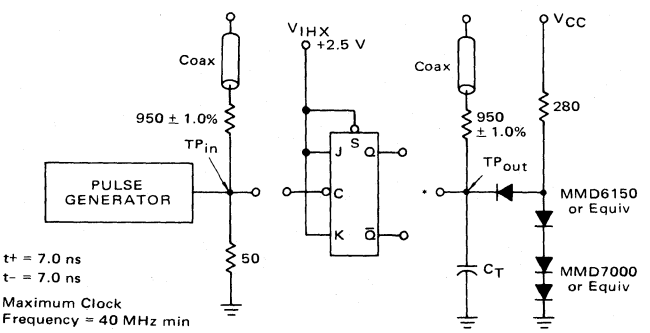
The data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The flip-flop is set to the Q = 1 state by applying a low level to the $\overline{SET}$ input. The direct $\overline{SET}$ inputs may be used at any time without regard to the clock state. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering — The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



t+ = 7.0 ns
t- = 7.0 ns

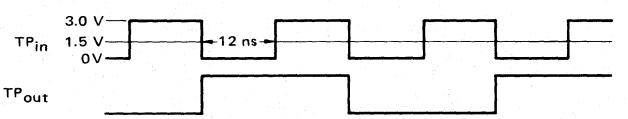
Maximum Clock Frequency = 40 MHz min

*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

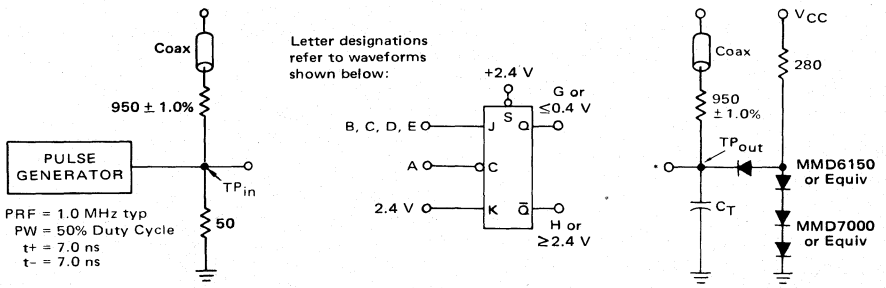
VOLTAGE WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs; to test other inputs, refer to Test Procedures Chart)



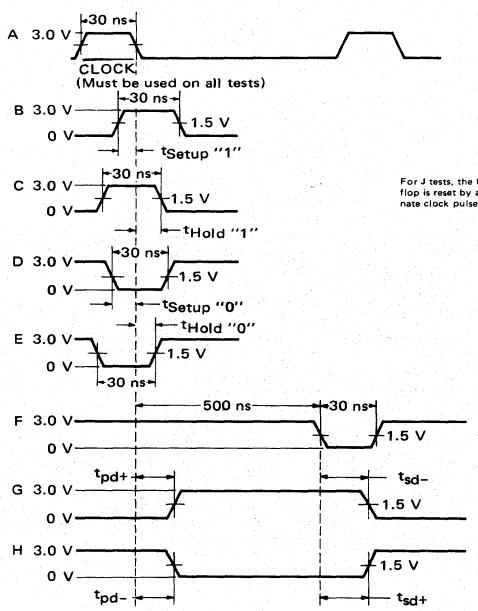
Three pulse generators are required and must be slaved together to provide the waveforms shown.

*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT J*	INPUT $\overline{SET}$*	INPUT K*	INPUT Q*	INPUT $\bar{Q}$*	LIMITS (ns) Max
t_{Setup} "1" J	B	2.4 V	2.4 V	G	H	15
t_{Hold} "1" J	C	2.4 V	2.4 V	G	H	0**
t_{Setup} "0" J	D	2.4 V	2.4 V	≤0.4 V	≥2.4 V	15
t_{Hold} "0" J	E	2.4 V	2.4 V	≤0.4 V	≥2.4 V	0**
t_{Setup} "1" K	Gnd	F	B	H	G	15
t_{Hold} "1" K	Gnd	F	C	H	G	0**
t_{Setup} "0" K	Gnd	F	D	≥2.4 V	≤0.4 V	15
t_{Hold} "0" K	Gnd	F	E	≥2.4 V	≤0.4 V	0**
t_{pd+}	Delay from $\overline{CLOCK}$ to Q during t_{Setup} "1" J test. Delay from $\overline{CLOCK}$ to $\bar{Q}$ during t_{Setup} "1" K test.					18
t_{pd-}	Delay from $\overline{CLOCK}$ to $\bar{Q}$ during t_{Setup} "1" J test. Delay from $\overline{CLOCK}$ to Q during t_{Setup} "1" K test.					18
t_{sd+}	Delay from $\overline{SET}$ to Q during t_{Setup} "1" K test.					18
t_{sd-}	Delay from $\overline{SET}$ to $\bar{Q}$ during t_{Setup} "1" K test.					18

For J tests, the flip-flop is reset by alternate clock pulses

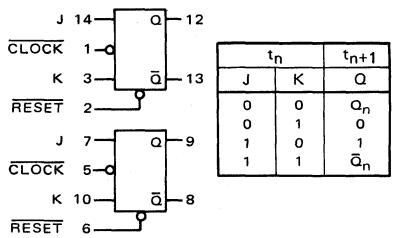
*Letters shown in test columns refer to waveforms shown at the left.

**t_{Hold} is typically a negative number.

DUAL J-K FLIP-FLOP

MC3163F • MC3063F
MC3163L • MC3063L,P

(54H73) (74H73)



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

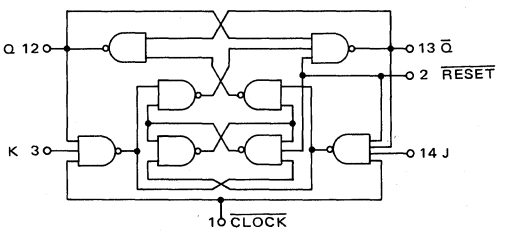
Input Loading Factor:
J, K = 1
$\overline{\text{RESET}}$, $\overline{\text{CLOCK}}$ = 2

Output Loading Factor = 10

Total Power Dissipation = 176 mW typ/pkg
Propagation Delay Time = 10 ns typ
Operating Frequency = 30 MHz typ

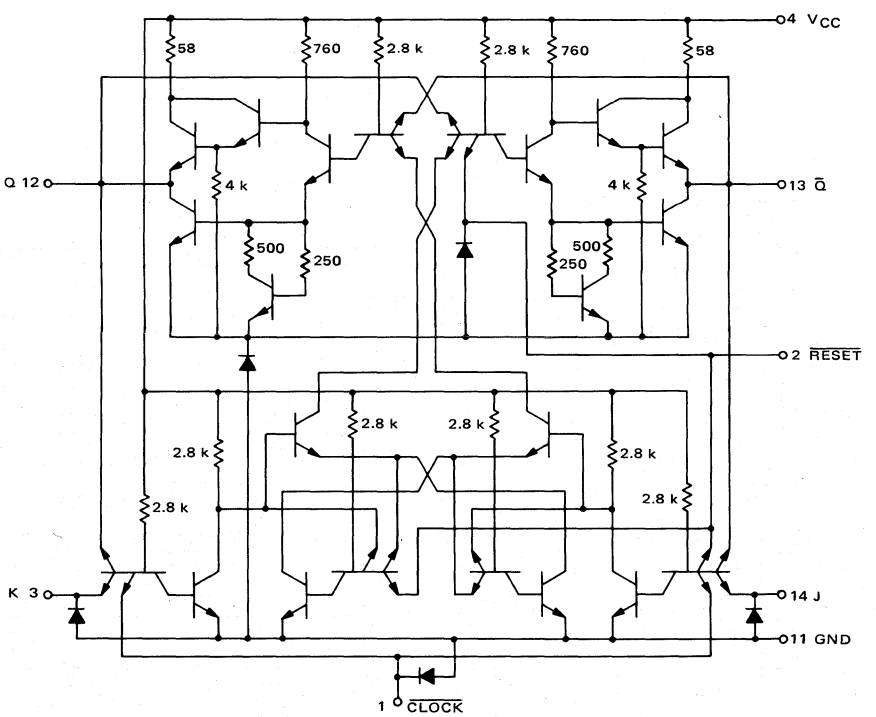
The MC3163/3063 dual J-K master-slave flip-flop is useful in simple register and counter designs, or where relatively slow rise times may be encountered. A similar function, the MC3155/3055 (MC54H72/74H72) AND input J-K flip-flop is available for applications requiring multiple ANDed inputs.

LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



Pin numbers for the 54H73F/74H73F device are the same as the pin numbers for the MC3163F,L/3063F,L,P.
These devices are available on special request.

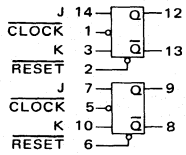
CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
	mA		Volts										
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}		
MC3163	20	-0.5	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.5	5.5		
MC3063	20	-0.5	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25		

Characteristic	Symbol	Pin Under Test	MC3163 Test Limits −55 to +125°C Min	Max	Unit	MC3063 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	**	Gnd
Input																					
Forward Current J	I_F	14	-	-2.0	mAdc	-	-2.0	mAdc	-	-	14	-	-	1,2,3	-	-	-	-	4	12	11*
K		3	-	-2.0	↓	-	-2.0	↓	-	-	3	-	-	1,2,14	-	-	-	-	↓	13	11*
$\overline{\text{Reset}}$		2	-	-4.0		-	-4.0		-	-	2	-	-	1,14	-	-	-	-		-	↓
$\overline{\text{Clock}}$		1	-	-2.0		-	-2.0		-	-	1	-	-	2,3,14	-	-	-	-		2	
Leakage Current J	I_{R1}	14	-	50	μAdc	-	50	μAdc	-	-	-	14	-	-	-	-	-	-	4	-	1,2,11*
K		3	-	50	↓	-	50	↓	-	-	-	3	-	2	-	-	-	-	↓	2	1,11*
$\overline{\text{Reset}}$		2	-	100		-	100		-	-	-	2	-	-	-	-	-	-		-	1,3,11,13,14*
$\overline{\text{Clock}}$		1†	-	50		-	50		-	-	-	1	-	-	-	-	-	-		-	2,3,11,14*
J	I_{R2}	14	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	14	-	-	-	-	-	4	-	1,2,11*
K		3	-	↓	↓	-	↓	↓	-	-	-	-	3	2	-	-	-	-	↓	2	1,11*
$\overline{\text{Reset}}$		2	-			-			-	-	-	-	2	-	-	-	-	-		-	1,3,11*,13,14
$\overline{\text{Clock}}$		1	-	↓	↓	-	↓	↓	-	-	-	-	1	-	-	-	-	-	↓	-	2,3,11,14*
Output																					
Output Voltage	V_{OL}	12	-	0.4	Vdc	-	0.4	Vdc	12	-	-	-	-	-	-	2	-	4	-	-	1,3,11,14*
		13	-	0.4	Vdc	-	0.4	Vdc	13	-	-	-	-	1,3,14	2	-	-	4	-	13	11*
	V_{OH}	12	2.4	-	Vdc	2.4	-	Vdc	-	12	-	-	-	1,3	2	-	-	4	-	13	11,14*
		13	2.4	-	Vdc	2.4	-	Vdc	-	13	-	-	-	-	-	2	-	4	-	-	1,3,11,14*
Short-Circuit Current	I_{SC}	12‡	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	1,3,14	-	-	-	-	4	-	11,12,13*
		13	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	1,3,14	-	-	-	-	4	-	2,11,13*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PD}	4	-	50	mAdc	-	50	mAdc	-	-	-	-	-	1, 2, 5# 6, 7, 14	-	-	-	-	4	-	3, 10, 11

*Ground inputs to flip-flop not under test.

**Momentarily ground pin prior to taking measurement to set flip-flop in the desired state. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

‡Test duration ≤ 100 ms.

†Under normal operating conditions this current is negative. This test guarantees that positive leakage current will not exceed the limit shown.

#Apply momemtarily 4.5 V, then ground to clock.

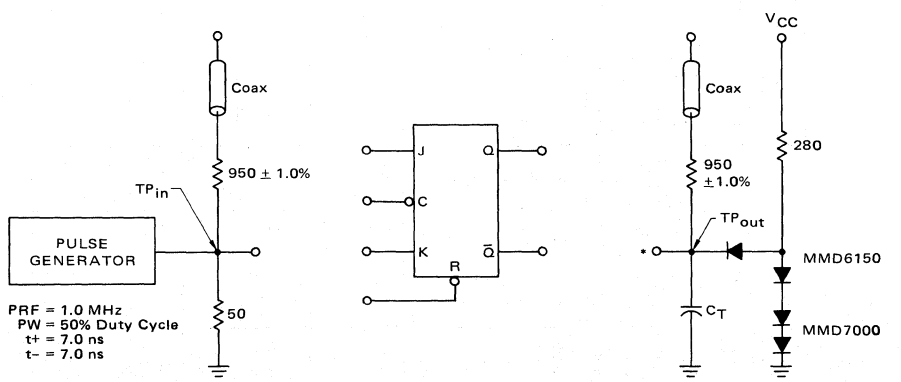
OPERATING CHARACTERISTICS

Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{\text{RESET}}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{\text{RESET}}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation, Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 12 ns minimum.

SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved together for t_{sd} tests.

*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

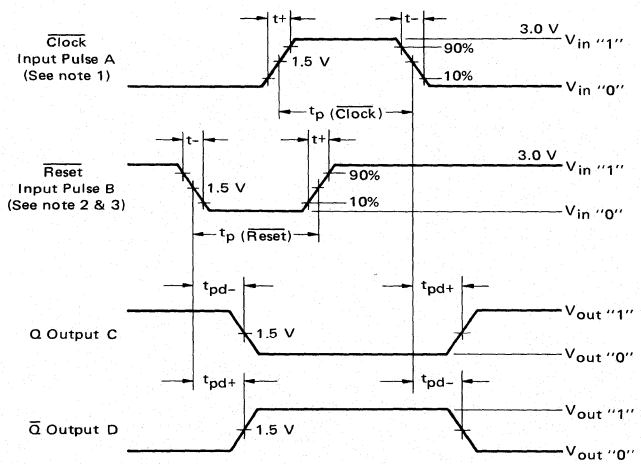
The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

TEST PROCEDURES

TEST	SYMBOL	INPUT			Q	$\bar{Q}$	LIMITS		
		$\bar{C}$	J,K	$\bar{R}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	2.4 V	5.0 V	†	†	25	–	MHz
Turn-On Delay– Clock to Output	t_{pd+}	A	2.4 V	2.4 V	C	D	–	21	ns
Turn-Off Delay– Clock to Output	t_{pd-}	A	2.4 V	2.4 V	C	D	–	27	ns
*Turn-On Delay– Reset to Output	t_{pd+}	A	2.4 V	B	C	D	–	13	ns
*Turn-Off Delay– Reset to Output	t_{pd-}	A	2.4 V	B	C	D	–	24	ns

Letters shown in test columns refer to waveforms shown.
*Clock pulse negative edge must occur when reset pulse is in "1" state.
†Output shall toggle with each input pulse.

VOLTAGE WAVEFORMS AND DEFINITIONS



NOTES

1. When testing f_{Tog}, $\overline{Clock}$ characteristics are t+ = t- ≤3.0 ns, t_p ($\overline{Clock}$) = 12 ns, PRF = 25 MHz.
   When testing t_{pd+}, t_{pd-}, $\overline{Clock}$ characteristics are t+ = t- ≤7.0 ns, t_p ($\overline{Clock}$) = 20 ns, PRF = 1.0 MHz.
2. $\overline{Reset}$ input dominates regardless of state of clock or J-K inputs.
3. $\overline{Reset}$ pulse characteristics t+ = t- ≤7.0 ns, t_p ($\overline{Reset}$) = 16 ns, PRF = 1.0 MHz.

MTTL

INTEGRATED CIRCUITS

MC4300/MC4000 SERIES

MTTL

MC4300/MC4000 SERIES

COMPLEX FUNCTIONS

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GENERAL INFORMATION
MTTL MC4300/4000 Series Complex Functions

INTRODUCTION

The MC4300/4000 Series Transistor-Transistor Logic (MTTL) Complex Functions are advanced logic functions providing significant reduction in package count and increased logic per function. They are designed for digital applications in the medium to high-speed range, with typical clock frequencies of 30 to 40 MHz and typical propagation delays of 5.0 to 10 ns per level of gating.

Each function in this series is specified to complement all families of Transistor-Transistor Logic and Diode-Transistor Logic. The input and output loading factors of each of the functions in the MC4300/4000 Series are defined in terms of the respective MTTL and MDTL specification formats to enable the designer to intermix the functions with ease. An interpretation of the MC4300/4000 Series specifications in terms of the other family specifications is included in this General Information section.

MAXIMUM RATINGS

Rating		Value	Unit
Supply Operating Voltage Range	MC4300 Series MC4000 Series	4.5 to 5.5 4.75 to 5.25	Vdc
Supply Voltage		+7.0	Vdc
Input Voltage		+5.5	Vdc
Output Voltage		+5.5	Vdc
Operating Temperature Range	MC4300 Series MC4000 Series	-55 to +125 0 to +75	°C
Storage Temperature Range – Ceramic Package Plastic Package		-65 to +150 -55 to +125	°C
Maximum Junction Temperature	MC4300 Series MC4000 Series	+175 +150	°C
Thermal Resistance - Junction To Case (θ_{JC}) Ceramic Package Plastic Package		 0.09 0.15	°C/mW
Thermal Resistance - Junction To Ambient (θ_{JA}) Ceramic Package Plastic Package		 0.26 0.30	°C/mW

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range, therefore good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL gate is in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL circuits. A comparatively large, low-inductance type capacitor (in the 1.0 μF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 μF capacitors for every eight packages throughout a breadboard is adequate to suppress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The standard supply voltage of the MTTL logic circuits is +5.0 Vdc. The typical average dc power dissipation is given for each MTTL circuit.(1) It should be noted that the totem pole output of all high-level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.30 mW/MHz/output for a 15 pF load. This ac power dissipation times the number of totem pole outputs should be added when calculating the total power requirements of the MTTL circuits.

---

(1)
$$P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where I_{PDL} and I_{PDH} are the typical dc current drains at V_{CC} = +5.0 V.

(2)Current flowing into the device under test is defined as positive.

Unused Inputs and Unused Gates

The unused inputs of any MTTL logic function should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage or returned to the power supply through a current limiting resistor. The preferred method is to tie the unused inputs to the used inputs. The output high-state drive capabilities of the MC4300/4000 Series are specified to allow this approach.

The unused inputs of the flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Output OR (Implied AND) Function

The functions in the MC4300/4000 Series have three basic output configurations: the active pull-up or totem pole, the passive or resistor pull-up, and the open-collector output.

The functions with the open collector and passive pull-up output configurations have been designed to permit the outputs to be tied together to perform the output OR (Implied AND) function. The outputs of functions with the active pull-up or totem pole output configuration CANNOT be tied together. If the outputs of these devices were tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground and the current that flows (approximately I_{SC}) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

NORMALIZING SPECIFICATION FORMATS

The MC4300/4000 Series of complex functions is specified to allow the functions to be used directly with each of the various families of MTTL and MDTL. Since the specification philosophies and test conditions vary significantly for these families, this section interprets the MC4000 series specifications in terms of the other formats.

Input Forward Current

The input forward current, I_F(mA), is the primary low-state loading current and is used to determine the input loading factors for each of the MC4000 series functions. This current flows out of the device and must be sunk by the driving source.(2) It is specified with an input voltage, V_F, equal to the maximum output low-state voltage, V_{OL}, on the input under test. The unused inputs are returned to a high-state reference voltage, V_{RH}, as shown in Figure 1. The current is specified at both power supply extremes, V_{CCL} and V_{CCH}, to define the guaranteed worst-case low-state input impedance. With this information, it is possible to plot a curve of the maximum guaranteed input forward current, I_F, as a function of the voltage across the input resistor as shown in Figure 2. From this curve, it is possible to find the guaranteed maximum input forward current for any MTTL and MDTL test conditions.

For example, the MTTL I MC500/400 family specifies the input forward current, I_F, for V_{CC} = +5.0 V and V_F = 0 V. Using these conditions, the I_F value for the MC4000 series device shown in Figures 1 and 2 is found directly from Figure 2:

$$I_F \text{ (maximum)} = 1.5 \text{ mA}$$

with V_{CC} = +5.0 V and V_F = 0 V; ΔV_{in} = 5.0 V.

This technique was used to define the normalized input loading factors shown on each of the MC4000 series data sheets.

Input Leakage Current

The input leakage current, $I_R(\mu A)$, is the high-state loading current and defines the amount of current that must be supplied to each input by the driving source. This parameter is tested with an input reverse voltage, V_R, equal to the minimum output high-state voltage, V_{OH}, applied to the input under test; all unused inputs are grounded. The test is made at the worst-case power supply voltage, V_{CCH}, as shown in Figure 3. This input leakage current is a combination of an inverse beta leakage current and an inter-emitter leakage current, and is always larger than just the inverse beta current, $I_L(\mu A)$, which occurs when all the unused inputs are left open. The test with the unused inputs grounded also results in the largest base drive current (I_B) for the input transistor, and represents the worst-case condition for the leakage currents since they are a product of the inverse beta and the base drive of the input device. The maximum power supply voltage, V_{CCH}, produces the maximum base current to the input transistor. The input leakage current therefore guarantees the inverse beta current, and is specified whenever possible.

For the MC4000 series, the voltage applied to the input under test, V_R, is equal to the minimum output high-state voltage, V_{OH}, at the worst-case output loading current condition. The minimum output high-state voltage at maximum output high-state current, I_{OH}, is defined to guarantee a minimum high-state dc noise margin. As the voltage on the input under test is increased, the input leakage current, I_R, also increases, as does the high-state drive current available from the output. For this reason, the input leakage current is specified for the worst-case driving condition on the output. Since all the MTTL and MDTL families specify an output high-state current, I_{OH}, at the minimum output high-state voltage, V_{OH}, the method of specifying I_R at $V_R = V_{OH}$ is compatible with the specification formats of each of the various families.

Input Breakdown

The input breakdown characteristics of the MC4000 series are guaranteed by the input breakdown voltage, BV_{in} (volts), specified at the maximum allowable input current, I_{in}; the unused inputs are grounded and the maximum power supply voltage, V_{CCH}, is applied to the unit under test. The actual breakdown voltage of the input will always be lower with the unused inputs grounded than with the unused inputs open, and the former condition therefore represents the worst case. With the unused inputs grounded, the base of the input transistor is clamped at one V_{BE} drop, while with the unused inputs open, the base of the input transistor is clamped to three diode drops, as shown in Figure 4. Since the objective of the breakdown test is to voltage stress the back-biased base-emitter input junction, the test with the unused inputs grounded is the worst case and guarantees the case with the unused inputs left open. This test is therefore directly compatible with the input breakdown tests for the other families.

FIGURE 1 – INPUT FORWARD CURRENT TEST CONDITIONS

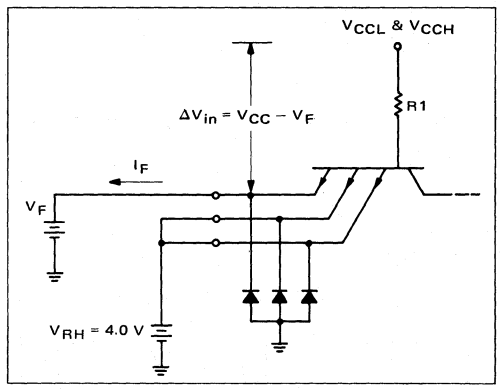


FIGURE 2 – INPUT VOLTAGE CHANGE versus GUARANTEED INPUT FORWARD CURRENT

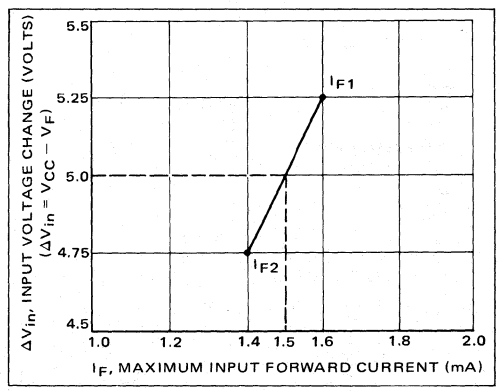


FIGURE 3 – INPUT LEAKAGE CURRENT TEST CONDITIONS

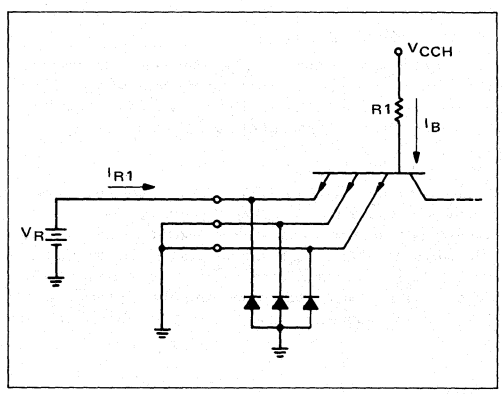
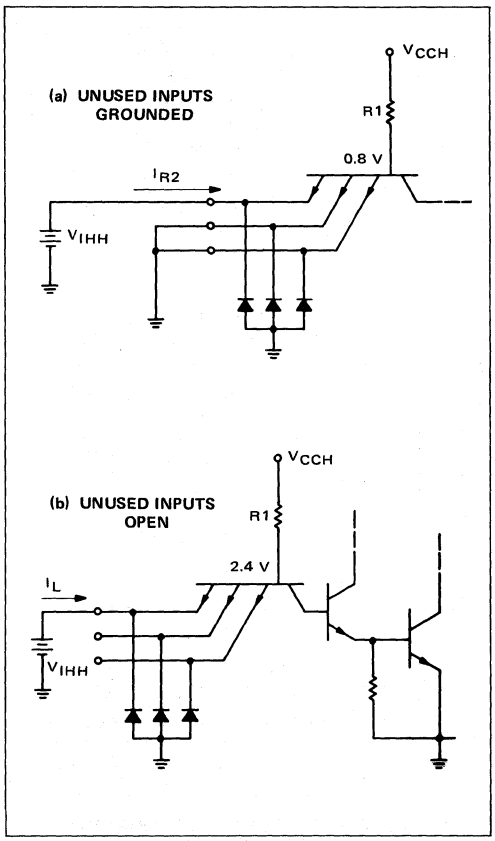


FIGURE 4 – INPUT BREAKDOWN TEST CONDITIONS



Input Clamp Diode Voltage

Each of the signal inputs to the MC4000 series functions has a clamp diode to limit negative ringing that can occur on signal lines. The input clamp diode voltage test, V_D, at the input diode current, I_D, guarantees the maximum impedance of the clamp diode.

Output Low-State Voltage

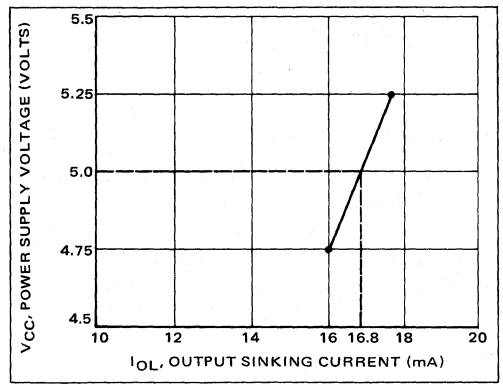
The output low-state voltage, V_{OL}(volts), in conjunction with the minimum input threshold voltage, V_{th} "0", defines the minimum low-state dc noise margin and the maximum drive capability of the output for that guaranteed noise margin. The output low-state voltage is specified at both power supply extremes under maximum output loading conditions with the worst-case input threshold voltage applied to a single input of the unit under test; all unused inputs (common to the unit segment under test) are returned to a reference voltage, V_{RH} = 4.0 V. Since all the characteristics except the maximum loading current, I_{OL}, are held constant for both test points, these tests not only guarantee the dc noise immunity but they also define the maximum drive capability of the output as a function of power supply voltage, as shown in Figure 5. Using this information, it is possible to relate the output drive capability of an MC4000 series function to any of the various MTTL or MDTL specification formats. The input threshold voltages and the output low-state voltage specified on the MC4000 series data sheet must still be used. For example, the MTTL I MC500/400 series specifies the output low-state voltage for V_{CC} = +5.0 V. Relating a typical MC4000 series function, the MC4008, to this format, the following guaranteed limits result at T_A = +75°C:

$$V_{OL} = 0.4 \text{ V at } I_{OL} = 16.8 \text{ mA}$$

with V_{th} "0" = 0.9 V, and all other inputs returned to V_{th} "1" = 1.8 V.

With this information, it is possible to define the V_{OL} at I_{OL} characteristics of the MC4000 series to any of the various MDTL or MTTL specification formats. The input thresholds and the V_{OL} for the MC4000 series must be used as specified on the MC4000 series data sheet.

FIGURE 5 – MAXIMUM DRIVE CAPABILITY AS A FUNCTION OF POWER SUPPLY VOLTAGE



Output High-State Voltage

The output high-state voltage, V_{OH}(volts), specification defines the guaranteed minimum output high-state voltage at maximum high-state loading current. This voltage is defined to guarantee a worst-case, high-state noise immunity. The maximum high-state drive current, I_{OL}, defines the high-state driving characteristics of the device.

The output high-state voltage for the MC4000 series is specified with the worst-case threshold voltage on the input, the minimum power supply voltage, V_{CCL}, and the maximum high-state output current as a load on the output. The unused inputs are returned to an input reference voltage, V_{RH}. This limit, as specified, is compatible with the other families of MTTL and MDTL and can be used independent of power supply variations for the threshold voltages specified on the various MC4000 series data sheets.

The output short circuit current, I_{SC}(mA), the maximum power supply current, I_{max}(mA), and the power supply drain, I_{PD}(mA) can be used directly with the various MTTL and MDTL specification formats.

DEFINITIONS

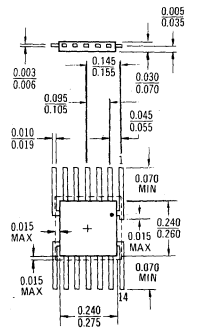
BV_{in}	Input breakdown voltage
C_T	Total parasitic capacitance, which includes probe, wiring, and load capacitances
I_B	Base current
I_{CEX}	Logic "1" output leakage current
I_D	Input diode current
I_F	Input forward current
I_{in}	Input current
I_L	Inverse beta current
I_{max}	Maximum rated power supply current with V_{max} applied
I_{OH}	Output logic "1" state source current
I_{OL}	Output logic "0" state sink current
I_{PD}	Power supply current drain
I_{PDH}	Power supply current drain with inputs in logic "1" state
I_{PDL}	Power supply current drain with inputs in logic "0" state
$I_{PD\ max}$	Maximum power supply current
$I_{PD\ min}$	Minimum power supply current
I_R	Input reverse current
I_{SC}	Logic "1" state source current with output shorted to ground
PRF	Pulse repetition frequency
PW	Pulse width
t+	Voltage rise time
t-	Voltage fall time
t_{pd+}	Turn-off delay time
t_{pd-}	Turn-on delay time
t_{wp}	Write pulse time
t_{wr}	Write recovery time
TP_{in}	Test point at input of device under test
TP_{out}	Test point at output of device under test
V_{BE}	Base-emitter voltage
V_{CC}	Power supply voltage
V_{CCH}	Maximum operating power supply voltage
V_{CCL}	Minimum operating power supply voltage
V_D	Input clamp diode voltage
V_F	Input forward voltage
V_{IH}	Logic "1" state input voltage
V_{IL}	Logic "0" state input voltage
V_{in}	Input voltage
V_{max}	Maximum rated power supply voltage
V_{OH}	Logic "1" state output voltage
V_{OL}	Logic "0" state output voltage
V_R	Input reverse voltage
V_{RH}	High-state reference voltage
V_{th} "0"	Logic "0" state input threshold voltage
V_{th} "1"	Logic "1" state input threshold voltage

PACKAGING

Package type is denoted by a suffix to the part number as follows:

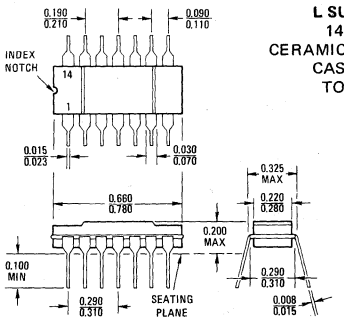
SUFFIX	DESCRIPTION
F	Ceramic Flat
L	Ceramic Dual In-Line
P	Plastic Dual In-Line

F SUFFIX
14-PIN
CERAMIC PACKAGE
CASE 607
TO-86



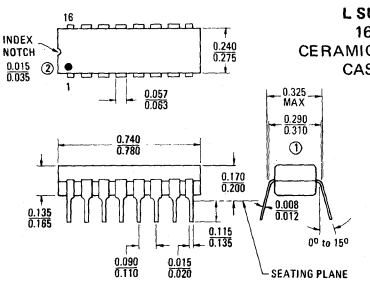
Lead 1 identified by color dot or by elbow on lead.
To convert inches to millimeters multiply by 25.4
All JEDEC dimensions and notes apply

L SUFFIX
14-PIN
CERAMIC PACKAGE
CASE 632
TO-116



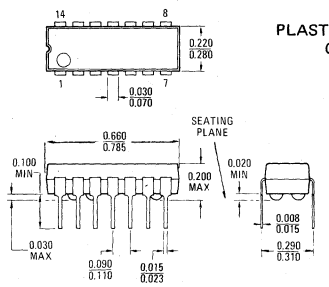
To convert inches to millimeters multiply by 25.4.
All JEDEC TO-116 dimensions and notes apply.

L SUFFIX
16-PIN
CERAMIC PACKAGE
CASE 620



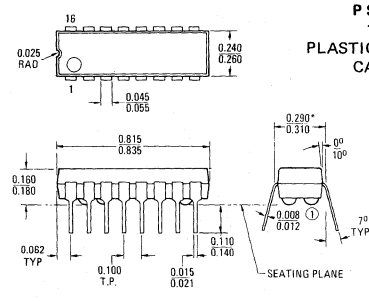
① This dimension is measured from the lead centers at the seating plane with leads vertical.
② Lead 1 identified by color dot, notch in lead, or notch in ceramic.
To convert inches to millimeters multiply by 25.4

P SUFFIX
14-PIN
PLASTIC PACKAGE
CASE 605
TO-116



Four insulating stand-offs are provided
To convert inches to millimeters multiply by 25.4
All JEDEC dimensions and notes apply

P SUFFIX
16-PIN
PLASTIC PACKAGE
CASE 612



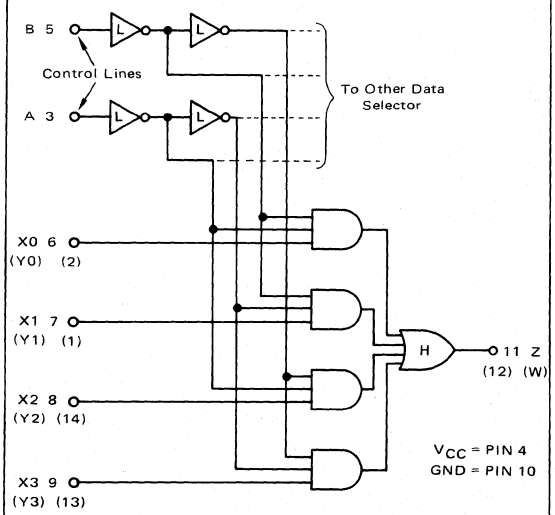
*Dimension is to lead centerline when formed parallel.
① 4 insulating stand-offs are provided.
To convert inches to millimeters multiply by 25.4

DUAL 4-CHANNEL
DATA SELECTOR

MC4300F,L*
MC4000F,L,P*

1/2 OF DEVICE SHOWN

(Numbers and symbols in parenthesis are for other half of device.)



$Z = AB\overline{X}0 + A\overline{B}X1 + \overline{A}BX2 + \overline{A}\overline{B}X3$

$W = AB\overline{Y}0 + A\overline{B}Y1 + \overline{A}BY2 + \overline{A}\overline{B}Y3$

Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg

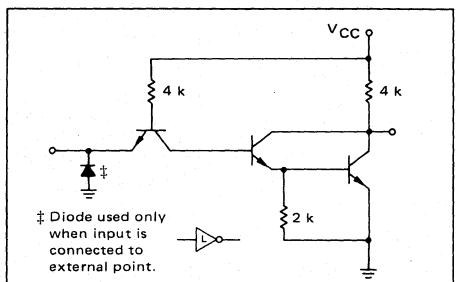
This device consists of two four-channel data selectors with common control lines, constructed from high-level AND-OR gates and low-level inverters. By selecting one of four logic combinations, information on one of the four data inputs will be routed to the output.

Data selectors are useful in applications where digital data is to be routed from one of several registers or locations to another register or location for processing.

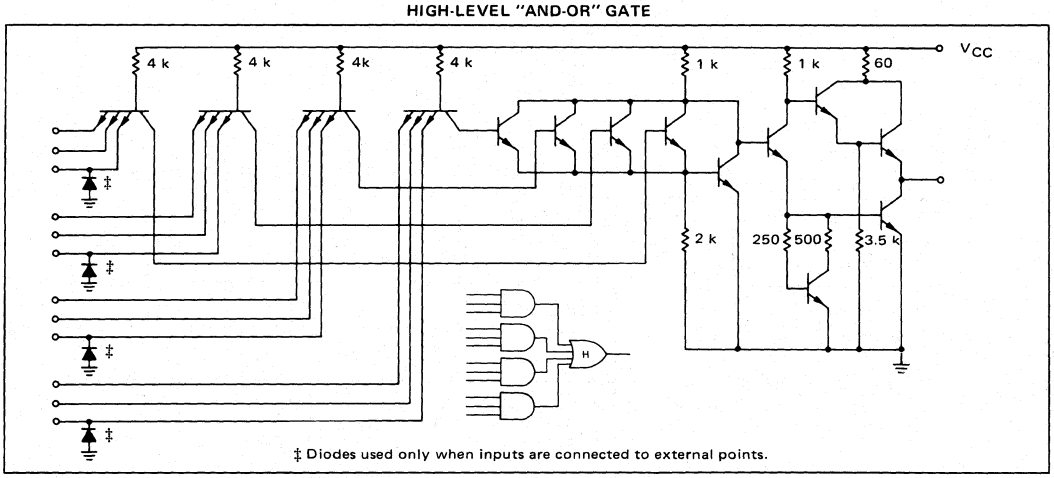
TYPICAL PROPAGATION DELAY TIMES (ns)
$T_A = 25^oC$

INPUT	Z	CONDITIONS
A	18	X0 = X2 = X3 = logic "0", X1 =
B	15	logic "1". A and B are de-
X1	11	fined by the logic equations.

LOW-LEVEL INVERTER

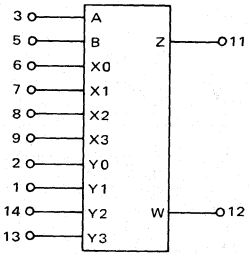


HIGH-LEVEL "AND-OR" GATE



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_{IHX}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
MC4300	-55°C	16	18.4	-1.6	–	–	1.1	2.0	–	0.4	2.4	4.0	–	5.0	4.5	5.5
MC4300	+25°C	16	18.4	-1.6	1.0	-10	1.1	1.8	2.5	0.4	2.4	4.0	7.0	5.0	4.5	5.5
MC4300	+125°C	16	18.4	-1.6	–	–	0.8	1.8	–	0.4	2.4	4.0	–	5.0	4.5	5.5
MC4000	0°C	16	17.6	-1.6	–	–	1.1	2.0	–	0.4	2.5	4.0	–	5.0	4.75	5.25
MC4000	+25°C	16	17.6	-1.6	1.0	-10	1.1	1.8	2.5	0.4	2.5	4.0	7.0	5.0	4.75	5.25
MC4000	+75°C	16	17.6	-1.6	–	–	0.9	1.8	–	0.4	2.5	4.0	–	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4300 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4000 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_{IHX}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																													
Forward Current	I_{F1}	6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	–	–	6	–	–	–	–	–	4	3,5,10
	I_{F2}	6	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	mAdc	–	–	–	–	–	–	–	–	6	–	–	–	–	4	–	3,5,10
Leakage Current	I_R	6	–	40	–	40	–	40	–	40	–	40	–	40	μAdc	–	–	–	–	–	–	–	–	–	3,5,6	–	–	–	–	4	10
Breakdown Voltage	BV_{in}	6	–	–	5.5	–	–	–	–	–	5.5	–	–	–	Vdc	–	–	–	6	–	–	–	–	–	–	3,5	–	–	–	4	10
Clamp Voltage	V_D	6	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	6	–	–	–	–	–	–	–	–	–	4	–	10
Output																															
Output Voltage	V_{OL}	11	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	11	–	–	–	–	1,2,3,5,6,7,8,9,13,14	–	–	–	–	–	–	–	–	4	–	10
		11	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	–	11	–	–	–	1,2,3,5,6,7,8,9,13,14	–	–	–	–	–	–	–	–	–	4	10
	V_{OH}	11	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	Vdc	–	–	11	–	–	1,3,5,7,8,9,13,14	2,6	–	–	–	–	–	–	–	4	–	10
Short-Circuit Current	I_{SC}	11	-30	-100	-30	-100	-30	-100	-30	-100	-30	-100	-30	-100	mAdc	–	–	–	–	–	–	–	–	2,5,6,8,9,13,14	–	1,3,7	–	4	–	–	10,11
Power Requirements (Total Device)																															
Maximum Power Supply Current	I_{max}	4	–	–	–	65	–	–	–	–	–	65	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	–	4	–	–	–	1,2,3,5,6,7, 8,9,10,13,14
Power Supply Drain	I_{PD}	4	–	–	–	45	–	–	–	–	–	45	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	–	–	–	–	4	1,2,3,5,6,7, 8,9,10,13,14
Switching Parameters																Pulse In		Pulse Out												
Turn-On Delay	t_{pd-1}	11	–	–	–	16	–	–	–	–	–	16	–	–	ns	6		11		–	–	–	–	–	–	–	–	4	–	–	1,2,3,5,7,8, 9,10,13,14
	t_{pd-2}	11	–	–	–	22	–	–	–	–	–	22	–	–	ns	5		11		–	–	–	6	–	–	–	–	4	–	–	1,2,3,7,8, 9,10,13,14
	t_{pd-3}	11	–	–	–	27	–	–	–	–	–	27	–	–	ns	3		11		–	–	–	7	–	–	–	–	4	–	–	1,2,5,6,8, 9,10,13,14
Turn-Off Delay	t_{pd+1}	11	–	–	–	16	–	–	–	–	–	16	–	–	ns	6		11		–	–	–	–	–	–	–	–	4	–	–	1,2,3,5,7,8, 9,10,13,14
	t_{pd+2}	11	–	–	–	22	–	–	–	–	–	22	–	–	ns	5		11		–	–	–	6	–	–	–	–	4	–	–	1,2,3,7,8, 9,10,13,14
	t_{pd+3}	11	–	–	–	27	–	–	–	–	–	27	–	–	ns	3		11		–	–	–	7	–	–	–	–	4	–	–	1,2,5,6,8, 9,10,13,14

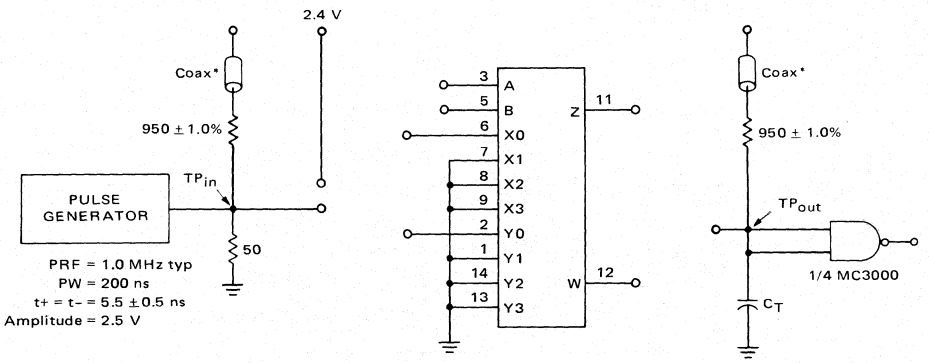
INPUT AND OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4300 INPUT LOADING FACTOR	MC4300 OUTPUT LOADING FACTOR
MC4300	1.0	10
MC500	1.23	12.3
MC2100	0.8	8
MC3100	0.8	8
MC5400	1.0	10
MC930	1.0*	10

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15*	12

*Applies only when input is being driven by MDTL gate with 2.0 kilohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.

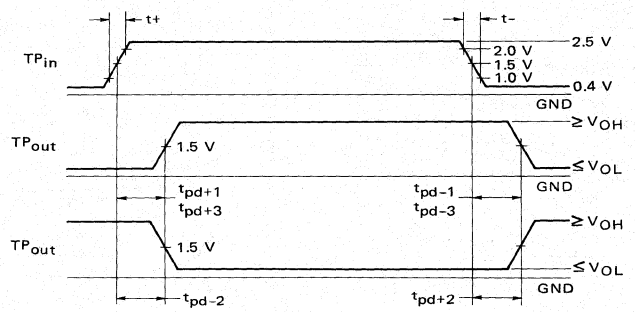
SWITCHING TIME TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS



TYPICAL PROPAGATION DELAY TIMES

FIGURE 1 – FOUR-GATE DELAY versus TEMPERATURE

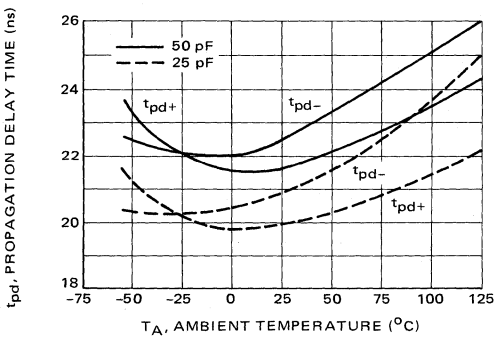


FIGURE 2 – THREE-GATE DELAY versus TEMPERATURE

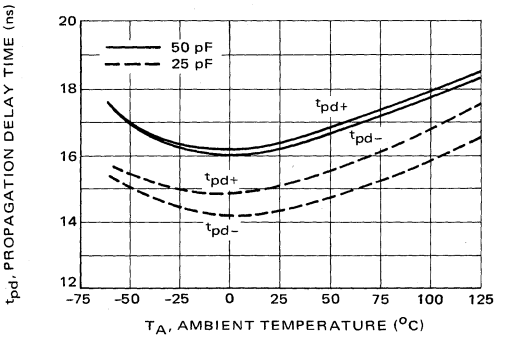


FIGURE 3 – TWO-GATE DELAY versus TEMPERATURE

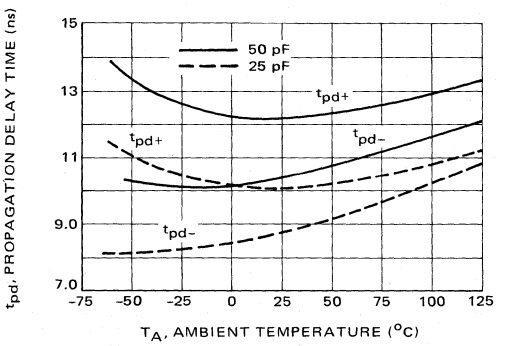


FIGURE 4 – DELAY versus LOAD CAPACITANCE

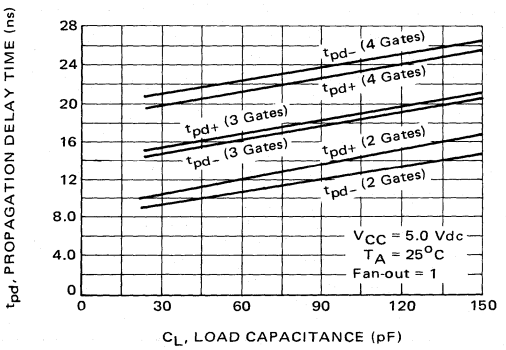


FIGURE 5 – DELAY versus SUPPLY VOLTAGE

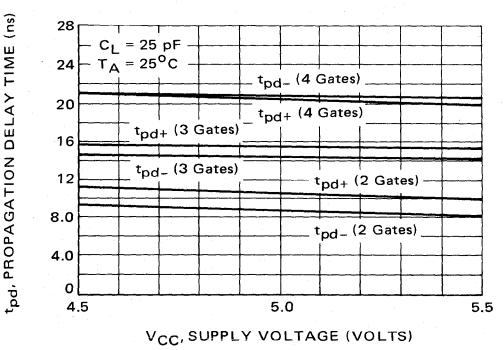
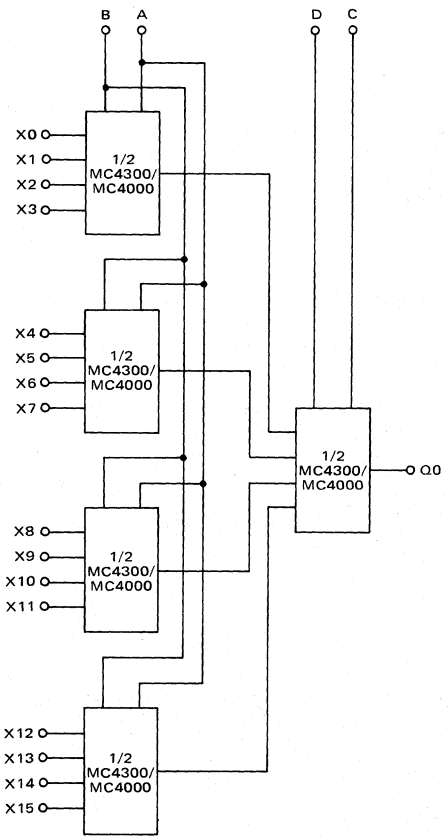


FIGURE 6 – 1-BIT 16-LINE DATA SELECTOR



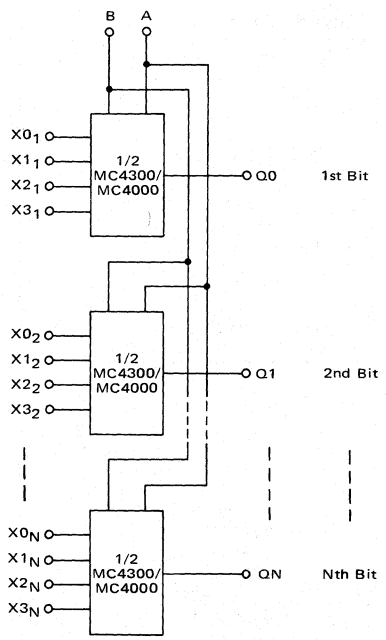
D	C	B	A	Q0
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X6
0	1	1	1	X7
1	0	0	0	X8
1	0	0	1	X9
1	0	1	0	X10
1	0	1	1	X11
1	1	0	0	X12
1	1	0	1	X13
1	1	1	0	X14
1	1	1	1	X15

TYPICAL APPLICATIONS

Data selection from one of sixteen inputs can be accomplished by using multiple MC4300/4000 data selector units, as shown in Figure 6.

An N-bit data selector network may be realized by paralleling N/2 data selectors as shown in Figure 7. Each bit is selected from its own group of four different inputs; therefore from each dual data selector we can obtain two bits. Thus, for N bits we need N/2 dual 4-line selectors.

FIGURE 7 – N-BIT 4-LINE DATA SELECTOR



B	A	$X0_n$	$X1_n$	$X2_n$	$X3_n$	Q_n
0	0	1	ϕ	ϕ	ϕ	X0
0	1	ϕ	1	ϕ	ϕ	X1
1	0	ϕ	ϕ	1	ϕ	X2
1	1	ϕ	ϕ	ϕ	1	X3

ϕ = Don't care
n = any number up to N

MC4001L,P*

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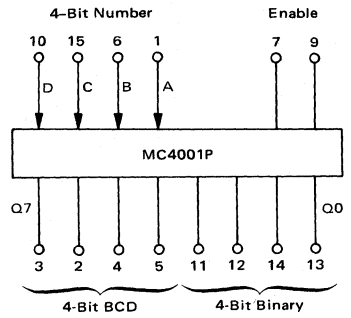


V_{CC} = Pin 16
GND = Pin 8

TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
				Binary to BCD				BCD to Binary			
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	0	0	1	0	1
0	1	1	0	1	0	0	1	0	1	1	0
0	1	1	1	1	0	1	0	0	1	1	1
1	0	0	0	1	0	1	1	0	1	0	1
1	0	0	1	1	1	0	0	0	1	1	0
1	0	1	0	1	0	0	0	0	1	1	1
1	0	1	1	1	0	0	1	1	0	0	0
1	1	0	0	1	1	1	0	1	0	0	1
1	1	0	1	1	1	1	1	0	0	1	0
1	1	1	0	1	0	1	1	0	0	1	0
1	1	1	1	0	1	0	0	0	0	0	0

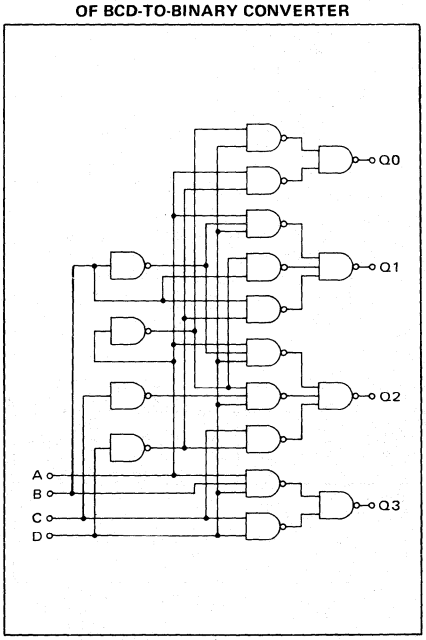
The MC4001 is derived from the XC170/171 128-Bit Read Only Memory. It serves as a basic building block in Binary-to-BCD and BCD-to-Binary converters. Conversion of any length binary or BCD word can be accomplished by interconnecting MC4001 packages. The MC4001 also contains a full adder and subtractor.

Features:
- Address times < 45 ns
- Outputs sink 16 mA
- Output capacitance < 7.0 pF @ 1.5 V

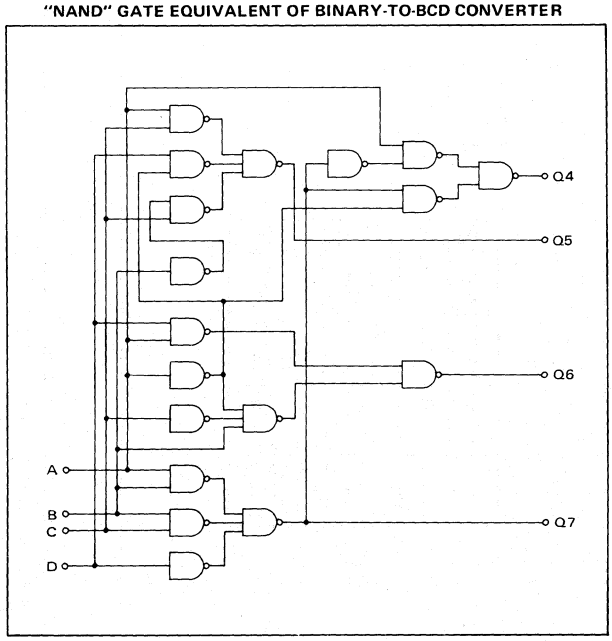
ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							

"NAND" GATE EQUIVALENT OF BCD-TO-BINARY CONVERTER



"NAND" GATE EQUIVALENT OF BINARY-TO-BCD CONVERTER



* L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4001 INPUT LOADING FACTOR	MC4001 OUTPUT LOADING FACTOR
MC4000	1.0	5
MC400	1.0	5
MC2000	0.67	5
MC3000	0.7	6
MC7400	1.0	10
MC830	1.15**	11

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

** Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Supply Operating Voltage Range	V_{CC}	4.75 to 5.25	Vdc
Input Voltage	V_{in}	−0.5 to +5.5	Vdc
Power Dissipation (Package Limitation) Derate above T_A=25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +75°C)

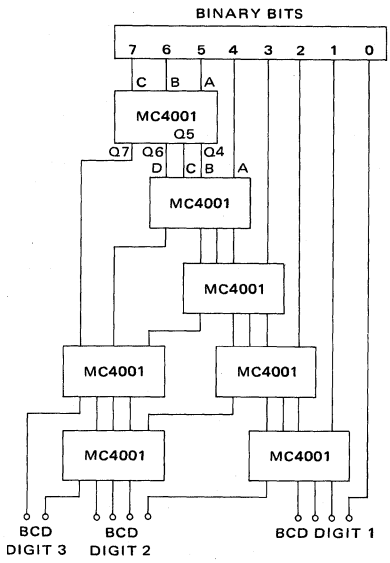
Characteristic	Symbol	Min	Max	Unit
Address Input Forward Current (V_A = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Enable Input Forward Current (V_E = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Address Input Leakage Current (V_A = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Enable Input Leakage Current (V_E = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Logical "0" Output Voltage (I_{OL} = 16 mAdc, V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	V_{OL}	-	0.45	Vdc
Logical "1" Output Voltage (V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, I_{OH} = -0.5 mAdc, V_{CC} = 4.75 Vdc)	V_{OH}	-	2.5	Vdc
Power Supply Drain Current (Memory Enabled, V_{CC} = 5.25 Vdc) (Memory Disabled, V_{CC} = 5.25 Vdc)	I_{PD}	- -	93 55	mAdc

SWITCHING TIMES (V_{CC} = 5.0 Vdc, T_A = +25°C)

Positive Input Address to Positive Output	I_{OL} = 10 mA driving 30 pF	t_{A+Q+}	-	45	ns
Negative Input Address to Negative Output		t_{A-Q-}	-	45	ns
Positive Input Address or Enable to Negative Output		t_{A+Q-} or t_{E+Q-}	-	45	ns
Negative Input Address or Enable to Positive Output		t_{A-Q+} or t_{E-Q+}	-	45	ns

TYPICAL APPLICATIONS

FIGURE 1 – BINARY-TO-BCD CONVERSION

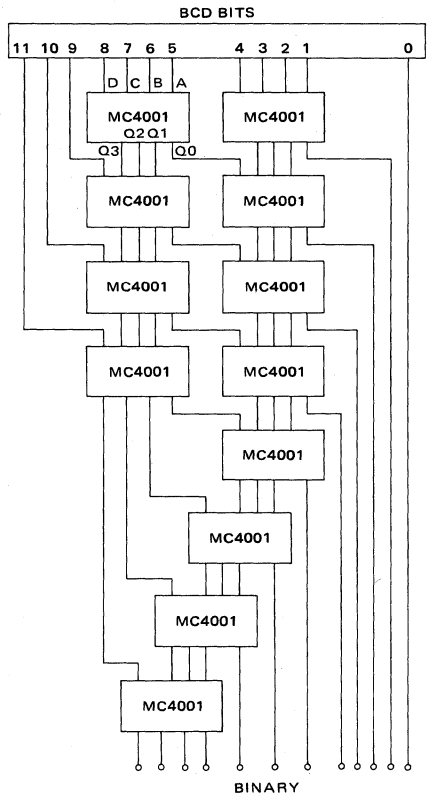


EQUIVALENT CONVERSION ALGORITHM

1. Examine three most significant bits. If sum ≥ 5, add 3.
2. Shift left 1 bit.
3. Examine each BCD decade. If sum ≥ 5, add 3.
4. Shift left 1 bit.
5. Is least significant bit in least significant BCD position: If "no", loop to item 3. If "yes", conversion is finished.

Delay time = 225 ns max

FIGURE 2 – BCD-TO-BINARY CONVERSION



EQUIVALENT CONVERSION ALGORITHM

1. Shift BCD number right 1 bit. Examine each 4-bit decade. If ≥8, subtract 3.
2. Shift right and examine until n–4 levels of examination are completed. (n equals total number of bits in BCD input code.)

FIGURE 3 – 4-BIT BINARY ADDER OUTPUT CONVERTED TO BCD

S4 D	S3 C	S2 B	S1 A	N4	N3	N2	N1	N0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	0	0
0	0	1	0	0	0	1	0	1
0	0	1	1	0	0	1	1	0
0	0	1	1	0	0	1	1	1
0	1	0	0	0	1	0	0	0
0	1	0	0	0	1	0	0	1
0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	1
0	1	1	0	0	1	1	0	0
0	1	1	0	0	1	1	0	1
0	1	1	1	0	1	1	1	0
0	1	1	1	0	1	1	1	1
1	0	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	1
1	0	0	1	1	0	0	1	0
1	0	0	1	1	0	0	1	1

TRUTH TABLE

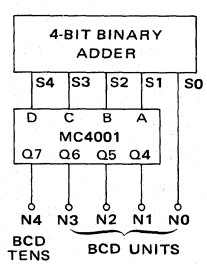
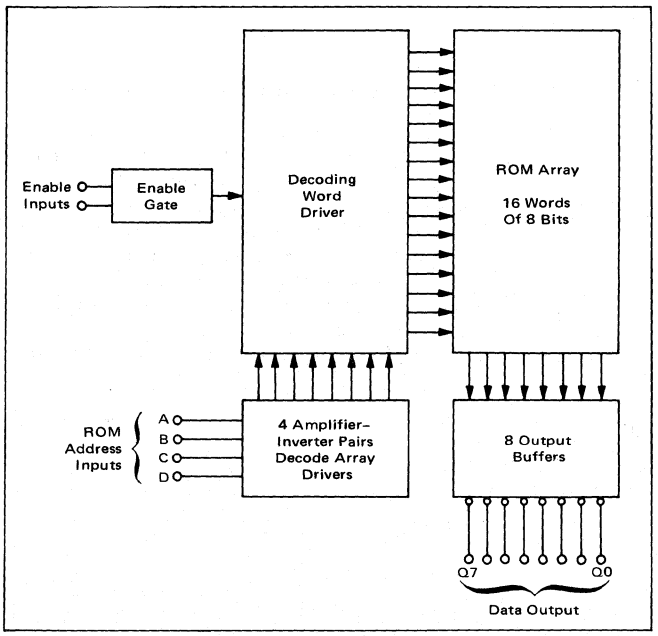
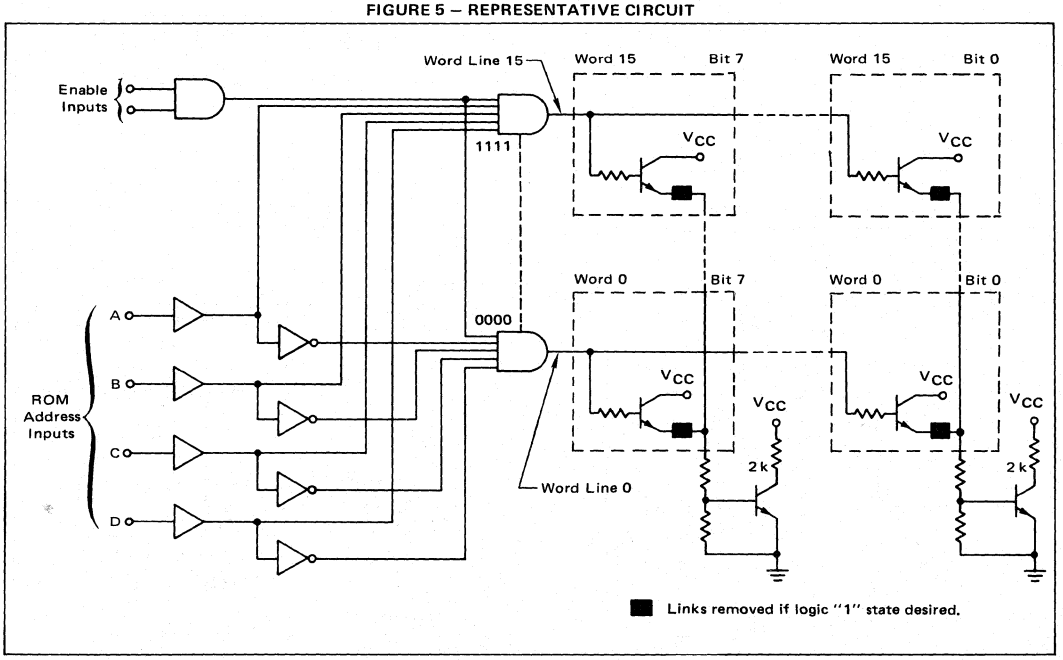


FIGURE 4 – BLOCK DIAGRAM



Many functions can be designed from the XC170/171 Read Only Memory. The MC4001 BCD-to-Binary/Binary-to-BCD converter is made from the XC171, which has 2.0 k ohm pullup resistors on the outputs. Through use of a computer-designed metal mask, the truth table shown on the first page of this data sheet is programmed into the Memory by etching out metal links from the device metalization where a logic "1" level must be stored. Logic "0"s are stored where links are not removed.

FIGURE 5 – REPRESENTATIVE CIRCUIT



MC4002F, L, P*

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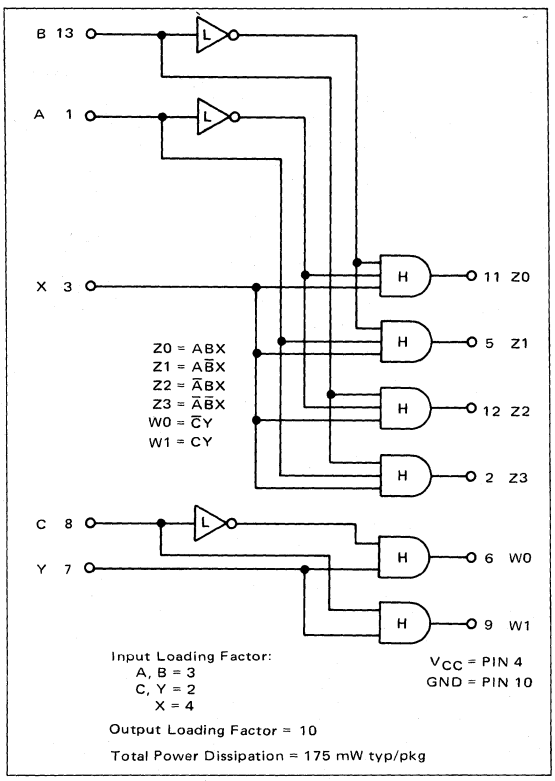


ADVANCE INFORMATION/NEW PRODUCT

This device consists of two data distributors constructed from high-level AND gates and low-level inverters. One distributes information present at the input line to one of four output lines; the other distributes information present at the input to one of two output lines. The routing path is selected by the logic signals at the control lines A, B or C.

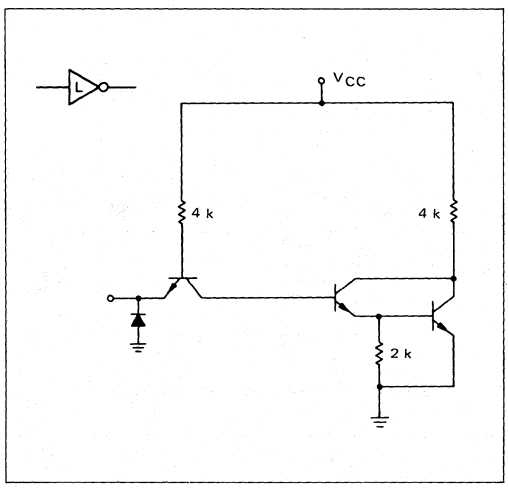
Data distributors are useful in applications where digital data is to be routed from a single register or location to one of several registers or locations for processing.

TYPICAL PROPAGATION DELAY TIMES (ns)
$T_A = 25^oC$

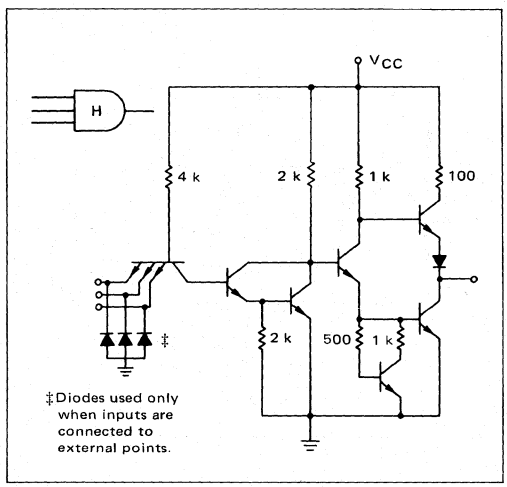
INPUT	Z0	Z1	Z2	Z3
A	14.5	10.5	14.5	10.5
B	14.5	14.5	10.5	10.5
X	10.5	10.5	10.5	10.5

INPUT	W0	W1
C	14.5	10.5
Y	10.5	10.5

LOW-LEVEL INVERTER



HIGH-LEVEL "AND" GATE



‡Diodes used only when inputs are connected to external points.

*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

**Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input			
Forward Current — A, B	I_{F1}	-4.8 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 5.25 Vdc
C, Y		-3.2 mAdc max	
X		-6.4 mAdc max	
A, B	I_{F2}	-4.2 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 4.75 Vdc
C, Y		-2.8 mAdc max	
X		-5.6 mAdc max	
Leakage Current — A, B	I_R	120 μAdc max	V_{in} = 2.5 Vdc, V_{CC} = 5.25 Vdc
C, Y		80 μAdc max	
X		160 μAdc max	
Breakdown Voltage	BV_{in}	5.5 Vdc max	I_{in} = 1.0 mAdc, V_{CC} = 5.25 Vdc, T_A = 25°C
Clamp Voltage	V_D	-1.5 Vdc max	I_D = -10 mAdc, V_{CC} = 4.75 Vdc, T_A = 25°C
Threshold Voltage	V_{th} "1"	2.0 Vdc	T_A = 0°C
		1.8 Vdc	T_A = +25°C, or T_A = +75°C
	V_{th} "0"	1.1 Vdc	T_A = 0°C, or T_A = +25°C
		0.9 Vdc	T_A = +75°C
Output			
Output Voltage	V_{OL}	0.4 Vdc max	I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc †
		0.4 Vdc max	I_{OL} = 17.6 mAdc, V_{CC} = 5.25 Vdc †
	V_{OH}	2.5 Vdc min	I_{OH} = -1.6 mAdc, V_{CC} = 4.75 Vdc †
Short-Circuit Current	I_{SC}	-20 to -65 mAdc	V_{CC} = 5.0 Vdc, output grounded †

†These tests are performed according to the logic equations with a true input equal to V_{th} "1" and a false input equal to V_{th} "0".

MC4304F,L • MC4305F,L*
MC4004F,L,P • MC4005F,L,P*

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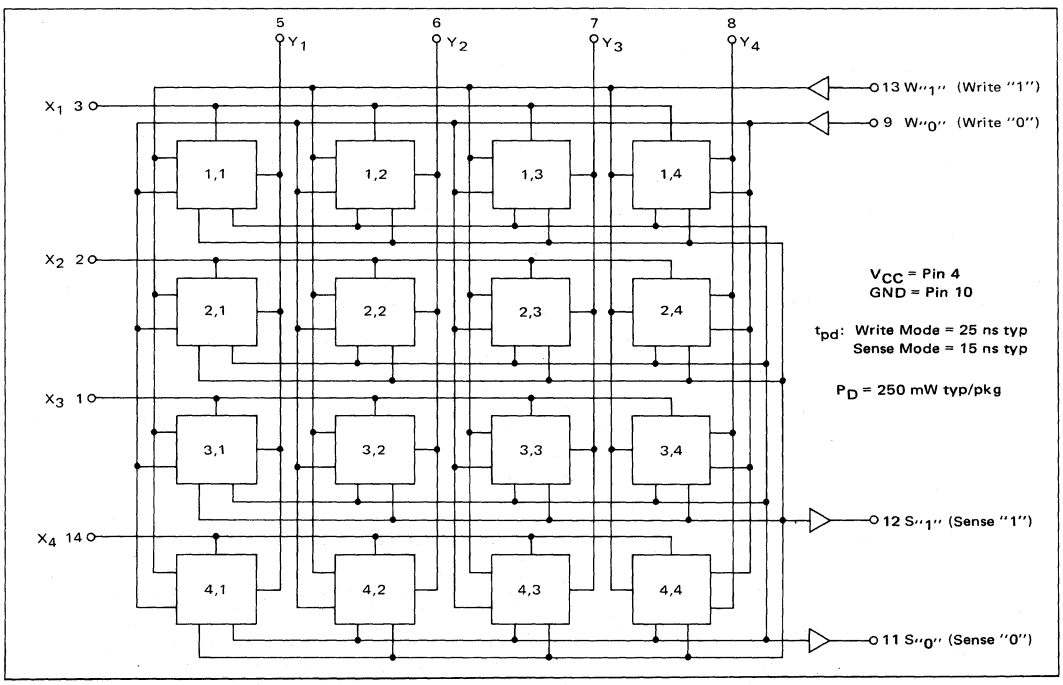
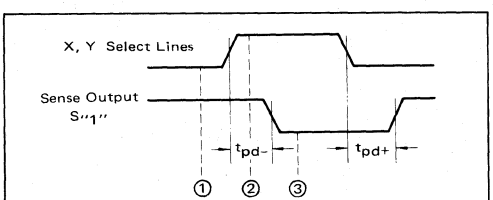
This 16-Bit memory cell serves as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

The memory contains 16 flip-flops arranged in a four-by-four matrix. A single bit of the matrix is selected by driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many devices can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two write amplifiers allow a "1" or a "0" to be written into a selected bit.



– OPERATING SEQUENCE –

FIGURE 1 – READ MODE TIMING DIAGRAM



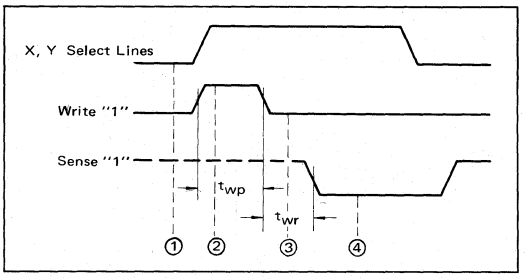
① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Desired bit selected by driving the appropriate X and Y select lines more positive than +2.1 V.

③ After the turn-on delay time (t_{pd-}), the S"1" output will be low (less than +0.45 V) and the S"0" output will be high (more than +2.5 V), providing that a "1" is stored in the selected bit.

*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

FIGURE 2 – WRITE MODE TIMING DIAGRAM



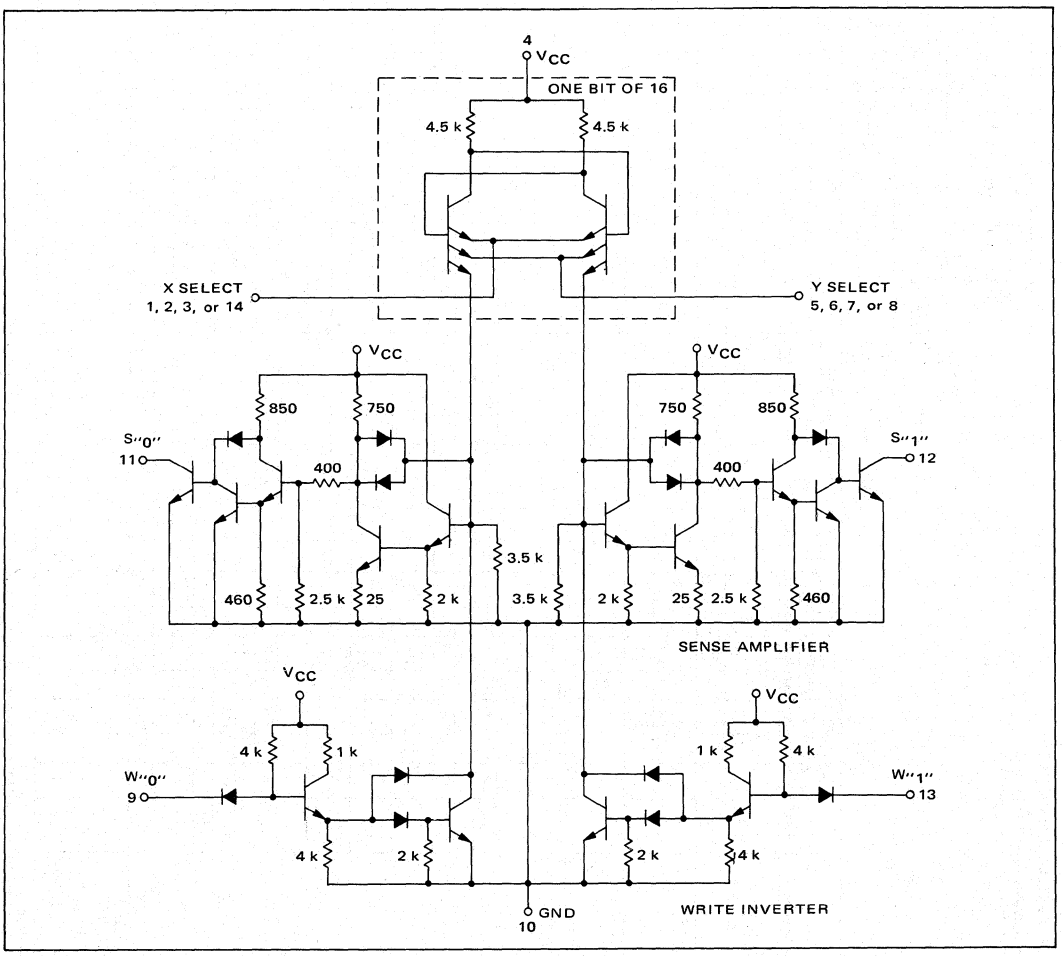
① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Bit location selected by driving the appropriate X and Y select lines more positive than +2.1 V. To write a "1", drive the write "1" input more positive than +2.1 V for a minimum time of 25 ns (t_{wp}).

③ Write "1" line returned to low state.

④ The stored bit can be read after the write recovery time (t_{wr}) of 40 ns. (The sense output is in an indeterminate state between steps 2 and 4.)

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one bit.
Other bits are tested in the same manner.

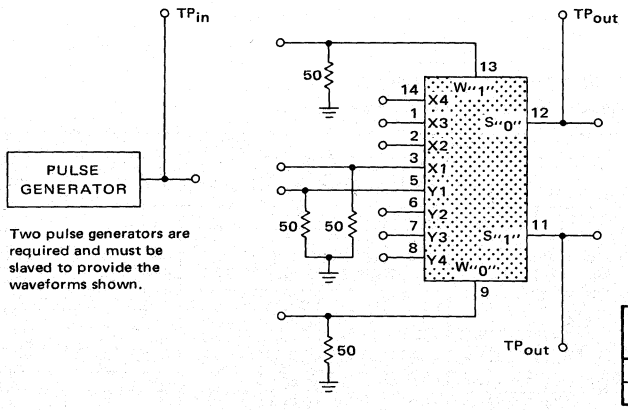
	@ Test Temperature	$I_{5"0"}$ Pr* (mA)	$I_{5"0"}$ Std (mA)	I_W (mA)	I_{XY} (mA)	$V_{in\,1}$ (Volts)	$V_{in\,2}$ (Volts)	$V_{in\,3}$ (Volts)	V_F (Volts)	V_R (Volts)	V_{th} (Volts)	V_{out} (Volts)	V_{CC} (Volts)	BV_{ckt} (Volts)
MC4304*, MC4305	−55°C	40	20	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0	-
	+25°C	40	20	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0	7.0
	+125°C	40	20	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0	-
MC4004*, MC4005	0°C	40	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0	-
	+25°C	40	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0	7.0
	+75°C	40	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0	-

Characteristic	Symbol	Pin Under Test	MC4304, MC4305 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4004, MC4005 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{5"0"}$	I_W	I_{XY}	$V_{in\,1}$	$V_{in\,2}$	$V_{in\,3}$	V_F	V_R	V_{th}	V_{out}	V_{CC}	BV_{ckt}	Gnd
Input																												
Forward Current Address Lines	I_F	3	-	-11	-	-11	-	-11	-	-13.5	-	-13.5	-	-13.5	mAdc	-	-	-	-	-	-	3	5,6,7,8	-	-	4	-	1,2,9,10,13,14
		5	-	-11	-	-11	-	-11	-	-13.5	-	-13.5	-	-13.5	mAdc	-	-	-	-	-	-	5	1,2,3,14	-	-	4	-	6,7,8,9,10,13
Write Inputs		9	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	9	-	-	-	4	-	1,2,3,5,6,7,8,10,13,14
		13	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	13	-	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Leakage Current Address Lines	I_R	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	mAdc	-	-	-	-	-	-	-	3	-	-	4	-	1,2,5,6,7,8,9,10,13,14
		5	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	mAdc	-	-	-	-	-	-	-	5	-	-	4	-	1,2,3,6,7,8,9,10,13,14
Write Inputs		9	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	-	9	-	-	4	-	1,2,3,5,6,7,8,10,13,14
		13	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	-	13	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Breakdown Voltage Address Lines	BV_{in}	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	3	-	-	-	-	-	-	-	4	-	1,2,5,6,7,8,9,10,13,14
		5	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	5	-	-	-	-	-	-	-	4	-	1,2,3,6,7,8,9,10,13,14
Write Inputs		9	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	9	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,10,13,14
		13	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	13	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Output (Note 1)																												
Output Voltage Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	-	-	3,5,13	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "0" Inhibit	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	3,5	-	-	13	9	-	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "0"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13	-	-	3,5,9	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "1" Inhibit	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	3,5	-	-	9	13	-	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	-	-	3,5,13	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Leakage Current Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	-	-	3,5,13	-	4	-	1,2,6,7,8,10,14
Leakage Current	I_{OLK}	12	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	3,5	-	-	-	-	12	4	-	1,2,6,7,8,9,10,13,14
Write "0"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13	-	-	3,5,9	-	4	-	1,2,6,7,8,10,14
Leakage Current	I_{OLK}	11	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	3,5	-	-	-	-	11	4	-	1,2,6,7,9,10,13,14
Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13	3,5,6,7,8	-	4	-	1,2,9,10,14
Leakage Current	I_{OLK}	11	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	-	-	3,5,6,7,8	11	4	-	1,2,9,10,13,14
Write "0"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	3,5,6,7,8	-	4	-	1,2,10,13,14
Leakage Current	I_{OLK}	12	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	-	-	3,5,6,7,8	-	4	-	1,2,9,10,13,14
Power Requirements (Total Device)																												
Power Supply Drain	I_{PD}	4	-	65	-	65	-	65	-	72	-	72	-	72	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,13,14
Power Supply Breakdown Current	I_{ckt}	4	-	-	-	95	-	-	-	-	-	105	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,13,14

*Prime Fan-Out

Note 1. Output logic "0" voltage and leakage current measurements are made as part of a functional test of a memory. Procedures identified by a double asterisk (**) are preconditioning procedures for the subsequent test. All power supply and input voltages must be maintained between tests.

SWITCHING TIME TEST CIRCUIT



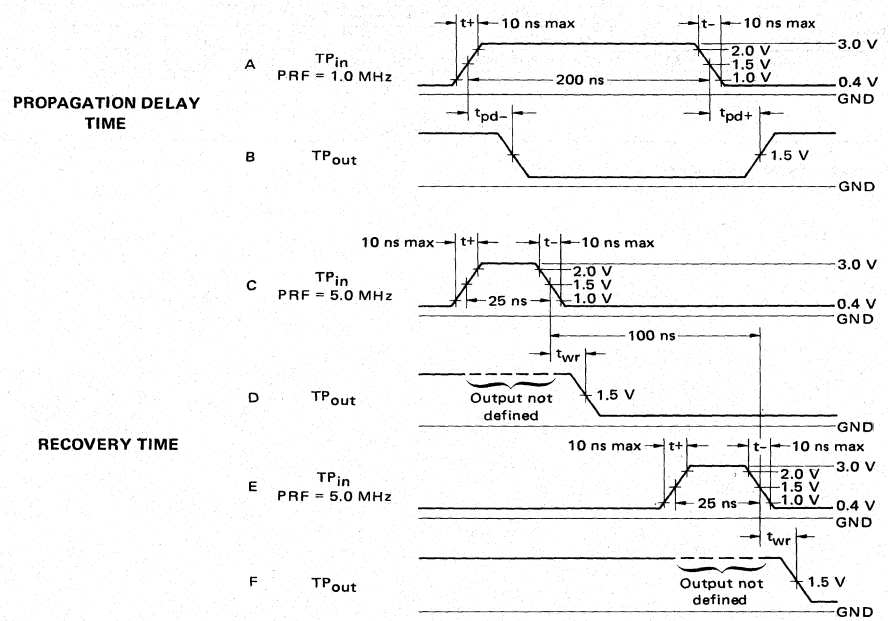
Two pulse generators are required and must be slaved to provide the waveforms shown.

DEVICE UNDER TEST	R1 OHMS	R2 OHMS
MC4304, MC4004	120	330
MC4305, MC4005	240	560

High-impedance probes (>1.0 Megohm) must be used when taking measurements.

See Switching Time Test Procedures table for value of C_T.

VOLTAGE WAVEFORMS AND DEFINITIONS



11

SWITCHING TIME TEST PROCEDURES

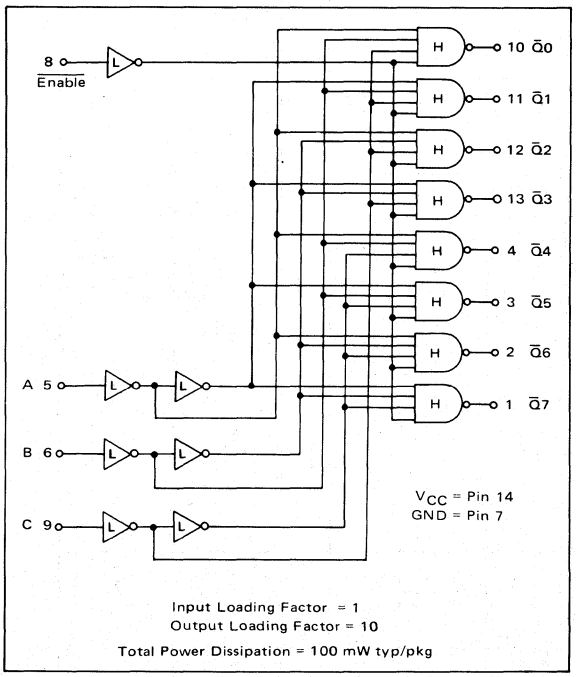
(Letters shown in test columns refer to waveforms)

Test	Symbol	Pin Under Test	Input Pin										Output		C_T* pF	Limits	
			3 X_1	2 X_2	1 X_3	14 X_4	5 Y_1	6 Y_2	7 Y_3	8 Y_4	9 W"0"	13 W"1"	11 S"0"	12 S"1"		MC4304-5 ns max	MC4004-5 ns max
Turn-Off Delay Time (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	30	23	23
	t_{pd+}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	35	35
Turn-Off Delay Time (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	30	23	23
	t_{pd+}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	35	35
Turn-On Delay Time (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd-}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	30	23	23
	t_{pd-}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	35	35
Turn-On Delay Time (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd-}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	30	23	23
	t_{pd-}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	35	35
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	11	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	B	–	30	35	35
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	12	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	–	B	30	35	35
Write Recovery Time	t_{wr}	12	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	–	D	30	40	40
		11	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	F	–	30	40	40
																ns min	ns min
Write Pulse Width	t_{wp}	–	Tested during t_{wr} tests.													25	25

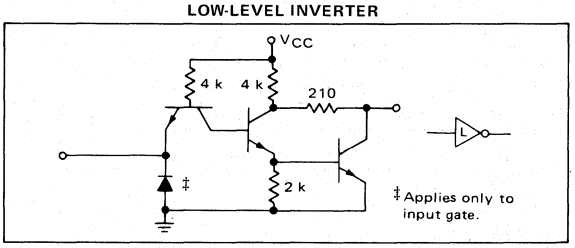
*Capacitance value for load of the Switching Time Test Circuit

**Preconditioning procedures for subsequent test.

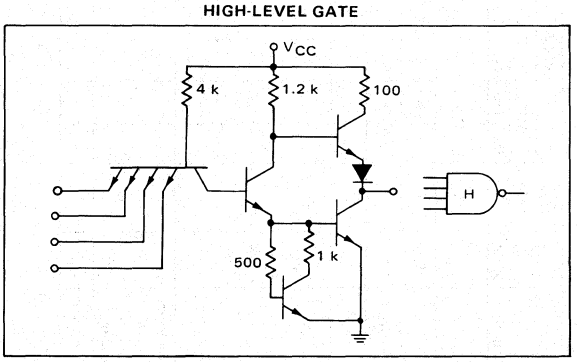
MC4306F,L*
MC4006F,L,P*



LOW-LEVEL INVERTER



HIGH-LEVEL GATE



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 dual in-line ceramic package (Case 632).
P suffix = TO-116 dual in-line plastic package (Case 605).

This device converts three lines of input data to a one-of-eight output. The enable line provides an inhibit capability and also allows the decoder to be expanded for larger decoder systems.

The 3-input/8-output decoder consists of high-level and low-level gates internally connected for minimum power consumption and maximum driving capabilities. The enable gate must be in the low state to perform the decode operation shown in the truth table.

The propagation delays shown in the charts are typical and vary according to loading, interconnection wiring length, and the number of logic levels involved.

$\bar{E}$ = 0

TRUTH TABLE

C	B	A	Q̄7	Q̄6	Q̄5	Q̄4	Q̄3	Q̄2	Q̄1	Q̄0
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

1 = High State
0 = Low State

TYPICAL TURN-ON DELAY TIMES (ns)
T_A = 25°C, C_T = 25 pF

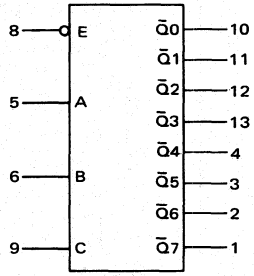
INPUT	Q̄0	Q̄1	Q̄2	Q̄3	Q̄4	Q̄5	Q̄6	Q̄7
A	11.5	16.0	11.5	16.0	11.5	16.0	11.5	16.0
B	11.5	11.5	16.0	16.0	11.5	11.5	16.0	16.0
C	11.5	11.5	11.5	11.5	16.0	16.0	16.0	16.0
$\bar{E}$	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13.5

TYPICAL TURN-OFF DELAY TIMES (ns)
T_A = 25°C, C_T = 25 pF

INPUT	Q̄0	Q̄1	Q̄2	Q̄3	Q̄4	Q̄5	Q̄6	Q̄7
A	14.0	19.5	14.0	19.5	14.0	19.5	14.0	19.5
B	14.0	14.0	19.5	19.5	14.0	14.0	19.5	19.5
C	14.0	14.0	14.0	14.0	19.5	19.5	19.5	19.5
$\bar{E}$	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner. Additionally, test all input-output combinations according to the truth table.



@Test Temperature		TEST CURRENT/VOLTAGE VALUES													
		mA					Volts								
		I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
MC4306	−55°C	18.4	16	-1.6	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5
	+25°C	18.4	16	-1.6	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5
	+125°C	18.4	16	-1.6	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5
MC4006	0°C	17.6	16	-1.6	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25
	+25°C	17.6	16	-1.6	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25
	+75°C	17.6	16	-1.6	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4306 Test Limits						MC4006 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												Gnd
			−55°C		+25°C		+125°C		0°C		+25°C		+75°C			I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max															
Input																													
Forward Current	I_F	5	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	-	-	-	-	5	-	-	-	-	-	14	7
Leakage Current	I_R	5	-	40	-	40	-	40	-	40	-	40	-	40	μAdc	-	-	-	-	-	-	-	-	5	-	-	-	-	14	7
Breakdown Voltage	BV_{in}	5	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	-	5	-	-	-	-	-	-	-	-	-	14	7
Clamp Voltage	V_D	5	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	-	5	-	-	-	-	-	-	-	14	-	7
Output																													
Output Voltage	V_{OL1}	1	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	1	-	-	-	-	8	5,6,9	-	-	-	-	-	-	14	7
	V_{OL2}	1	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	-	1	-	-	-	8	5,6,9	-	-	-	-	-	14	-	7
	V_{OH}	1	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	-	1	-	-	-	5,6,8,9	-	-	-	-	-	14	-	7
Short-Circuit Current	I_{SC}	1	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	-	-	-	8	-	14	-	-	1,7
Power Requirements (Total Device)																													
Maximum Power Supply Current	I_{max}	14	-	-	-	51	-	-	-	-	-	51	-	-	mAdc	-	-	-	-	-	-	-	-	-	5,6,8,9	14	-	-	-	7
Power Supply Drain	I_{PD}	14	-	-	-	34	-	-	-	-	-	34	-	-	mAdc	-	-	-	-	-	-	-	-	8	-	5,6,9	-	14	-	-	7

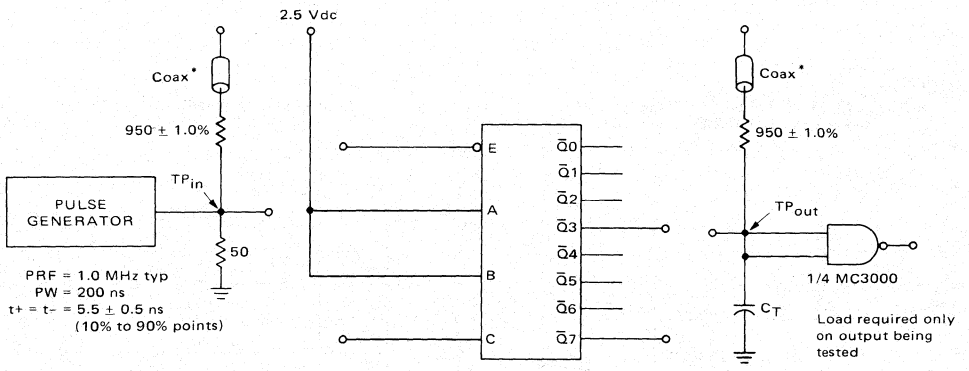
INPUT AND OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4306 INPUT LOADING FACTOR	MC4306 OUTPUT LOADING FACTOR
MC4300	1.0	10
MC500	1.2	12
MC2100	0.8	8
MC3100	0.8	8
MC5400	1.0	10
MC930	1.0*	10

FAMILY	MC4006 INPUT LOADING FACTOR	MC4006 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.8	8
MC7400	1.0	10
MC830	1.15*	12

*Applies only when input is being driven by MDTL gate with 2.0 kilohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.

SWITCHING TIME TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

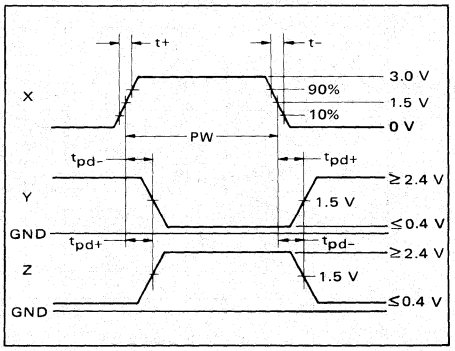
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

(Letters shown in test columns refer to waveforms.)

TEST	$\bar{E}$	C	Q̄3	Q̄7	LIMITS Max	LIMITS Unit
t_{pd+} (C to Q̄3)	Gnd	X	Z	–	20	ns
t_{pd-} (C to Q̄3)	Gnd	X	Z	–	17	ns
t_{pd+} (C to Q̄7)	Gnd	X	–	Y	29	ns
t_{pd-} (C to Q̄7)	Gnd	X	–	Y	23	ns
t_{pd+} ($\bar{E}$ to Q̄7)	X	2.5 V	–	Z	21	ns
t_{pd-} ($\bar{E}$ to Q̄7)	X	2.5 V	–	Z	20	ns

VOLTAGE WAVEFORMS



TYPICAL SWITCHING TIMES

FIGURE 1 – TURN-ON DELAY TIME versus TEMPERATURE

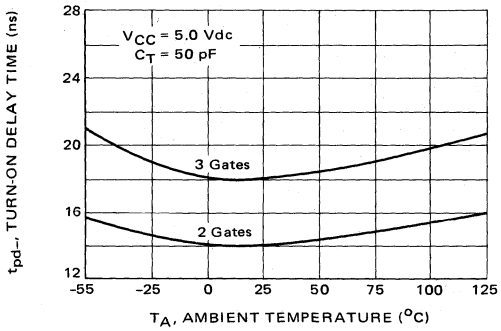


FIGURE 2 – TURN-OFF DELAY TIME versus TEMPERATURE

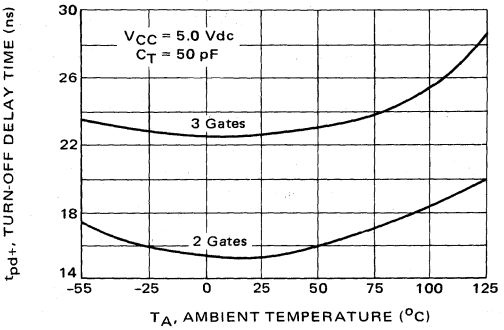


FIGURE 3 – TURN-ON DELAY TIME versus TEMPERATURE

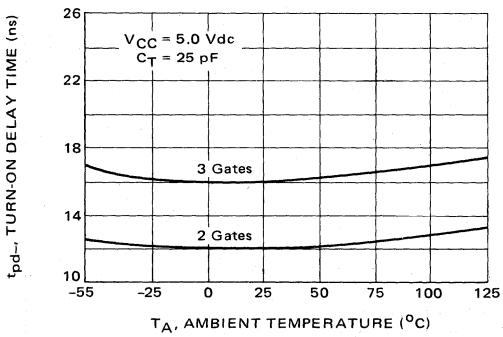


FIGURE 4 – TURN-OFF DELAY TIME versus TEMPERATURE

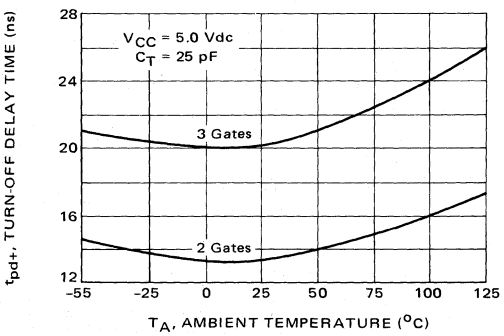


FIGURE 5 – TURN-ON DELAY TIME versus CAPACITIVE LOADING

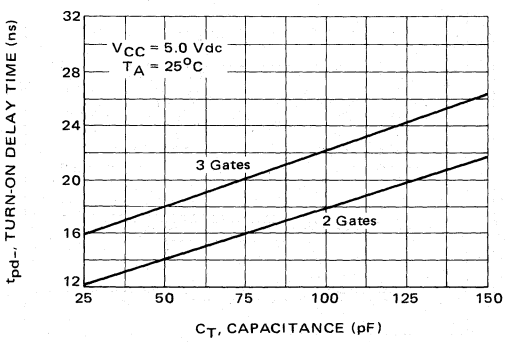
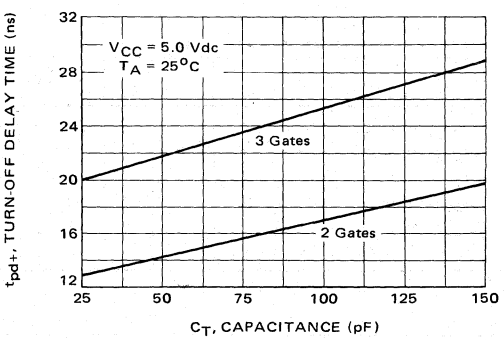


FIGURE 6 – TURN-OFF DELAY TIME versus CAPACITIVE LOADING



TYPICAL SWITCHING TIMES (continued)

FIGURE 7 – TURN-ON DELAY TIME versus POWER SUPPLY VOLTAGE

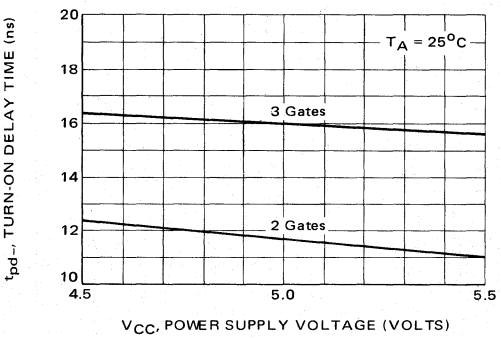
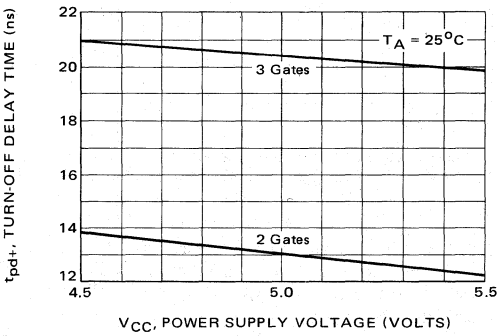


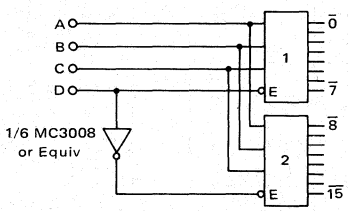
FIGURE 8 – TURN-OFF DELAY TIME versus POWER SUPPLY VOLTAGE



TYPICAL APPLICATIONS

Combinations of MC4306/4006 decoders can be used to produce various decoding operations. Figure 1 illustrates the use of two of these binary to one-of-eight decoders and one inverter to convert four digital inputs into one of 16 mutally exclusive outputs. In this operation the $\overline{\text{Enable}}$ input of both decoders, in conjunction with the inverter, is used for the fourth digital bit. The D input is low from state 0 thru 7, enabling decoder unit 1 and inhibiting decoder unit 2. For states 8 thru 15 the reverse is true, thus providing the eight additional states needed for the fourth input variable. Outputs $\overline{0}$ thru $\overline{15}$ are selected by the natural binary code on inputs A, B, C, and D; however, the MC4306/4006 can be used to decode any four-bit code by appropriately choosing outputs to correspond to the inputs.

FIGURE 1 – BINARY TO 1-OF-16 DECODER



Output Terminal	Input D	C	B	A	Output Device
0	0	0	0	0	1
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	2
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

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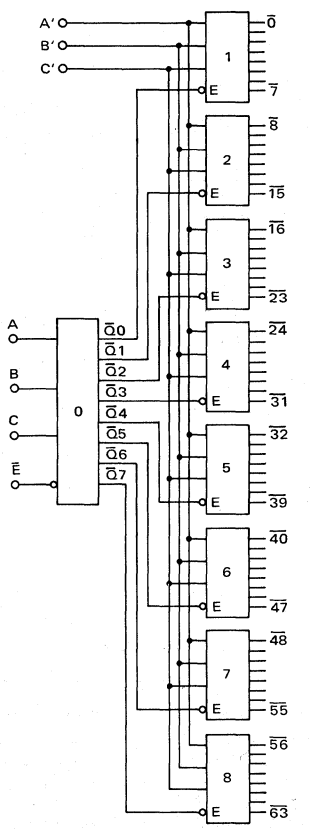
TYPICAL APPLICATIONS
(continued)

Figure 2 illustrates the use of nine MC4306/4006 decoders in a 1-of-64 decoder.

If the $\overline{\text{Enable}}$ input is used as a data input terminal, the data bit will appear at the output terminal selected by the address on lines A, B, and C. Thus the MC4306/4006 can be used as an eight-line data distributor (demultiplexer). All unselected outputs will be at a logic "1" level. Figure 3 shows two MC4312/4012 four-bit shift registers used in conjunction with an MC4306/4006 to yield an eight-bit serial data transmission system. The MC4312/4012's convert eight bits of parallel data to serial for transmission to another part of the system. The MC4306/4006 receives the serial data and distributes it to any of eight locations. By holding the address lines of the MC4306/4006 constant, all data bits are routed to the same location where they may be converted to parallel form again. By changing the MC4306/4006 address inputs at the same rate that data is being transmitted, each data bit can be distributed to a different location.

FIGURE 2 – GATED BINARY TO 1-OF-64 DECODER



Output Terminal	Input C	B	A	C'	B'	A'	Output Device
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	
2	0	0	0	0	1	0	
3	0	0	0	0	1	1	
4	0	0	0	1	0	0	
5	0	0	0	1	0	1	
6	0	0	0	1	1	0	
7	0	0	0	1	1	1	
8	0	0	1	0	0	0	2
9	0	0	1	0	0	1	
10	0	0	1	0	1	0	
11	0	0	1	0	1	1	
12	0	0	1	1	0	0	
13	0	0	1	1	0	1	
14	0	0	1	1	1	0	
15	0	0	1	1	1	1	
16	0	1	0	0	0	0	3
17	0	1	0	0	0	1	
18	0	1	0	0	1	0	
19	0	1	0	0	1	1	
20	0	1	0	1	0	0	
21	0	1	0	1	0	1	
22	0	1	0	1	1	0	
23	0	1	0	1	1	1	
24	0	1	1	0	0	0	4
25	0	1	1	0	0	1	
26	0	1	1	0	1	0	
27	0	1	1	0	1	1	
28	0	1	1	1	0	0	
29	0	1	1	1	0	1	
30	0	1	1	1	1	0	
31	0	1	1	1	1	1	
32	1	0	0	0	0	0	5
33	1	0	0	0	0	1	
34	1	0	0	0	1	0	
35	1	0	0	0	1	1	
36	1	0	0	1	0	0	
37	1	0	0	1	0	1	
38	1	0	0	1	1	0	
39	1	0	0	1	1	1	
40	1	0	1	0	0	0	6
41	1	0	1	0	0	1	
42	1	0	1	0	1	0	
43	1	0	1	0	1	1	
44	1	0	1	1	0	0	
45	1	0	1	1	0	1	
46	1	0	1	1	1	0	
47	1	0	1	1	1	1	
48	1	1	0	0	0	0	7
49	1	1	0	0	0	1	
50	1	1	0	0	1	0	
51	1	1	0	0	1	1	
52	1	1	0	1	0	0	
53	1	1	0	1	0	1	
54	1	1	0	1	1	0	
55	1	1	0	1	1	1	
56	1	1	1	0	0	0	8
57	1	1	1	0	0	1	
58	1	1	1	0	1	0	
59	1	1	1	0	1	1	
60	1	1	1	1	0	0	
61	1	1	1	1	0	1	
62	1	1	1	1	1	0	
63	1	1	1	1	1	1	

FIGURE 3 – 8-LINE MULTIPLEXED TRANSMISSION SYSTEM

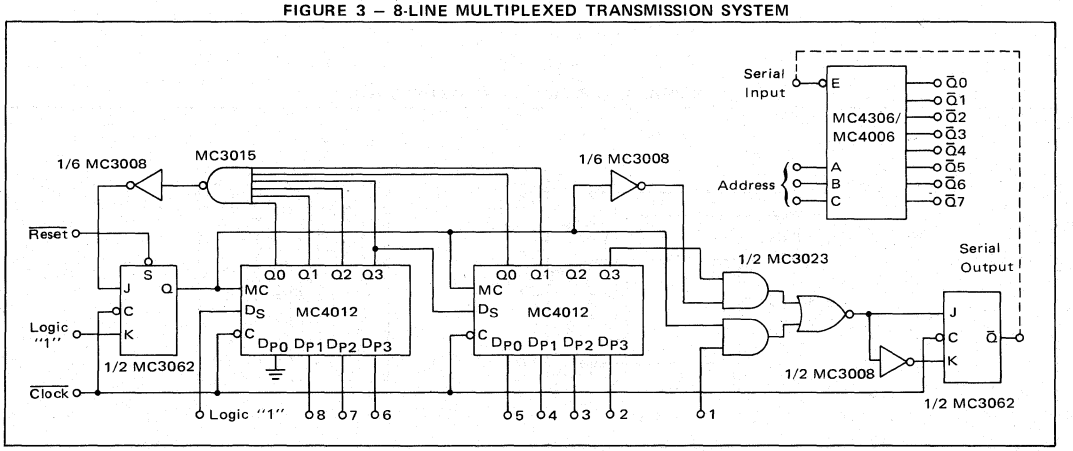
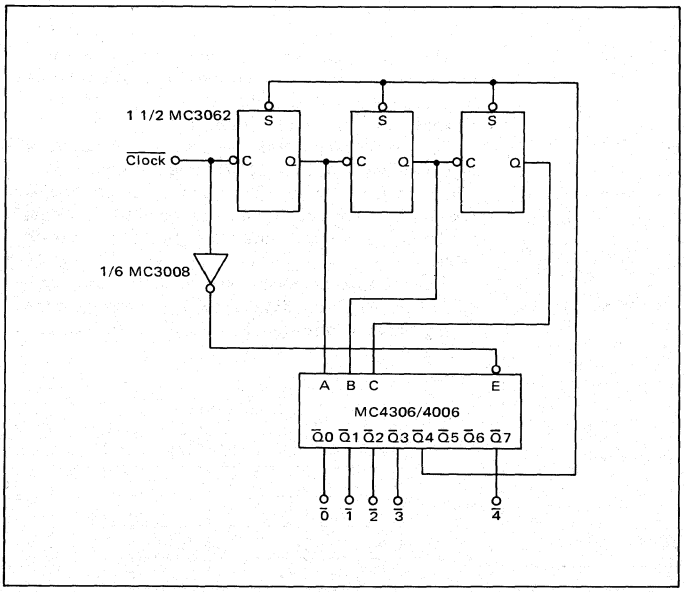


FIGURE 4 – DECODED DIVIDE-BY-FIVE COUNTER



TYPICAL APPLICATIONS
(continued)

In addition to simply decoding the output state of a counter, the MC4306/4006 can be used to make an ordinary binary counter into an odd-modulus counter. For example, three flip-flops and one MC4306/4006 provide a completely decoded divide-by-five counter as shown in Figure 4. The $\overline{4}$ output is used to set all the flip-flops to the 111 state so that the counter will return to 000 on the next clocking edge. The $\overline{\text{Enable}}$ input is used to prevent false outputs due to rippling of the outputs through intermediate states. Output 7 of the MC4306/4006 is used for the fifth counter output state.

MC4007L,P*

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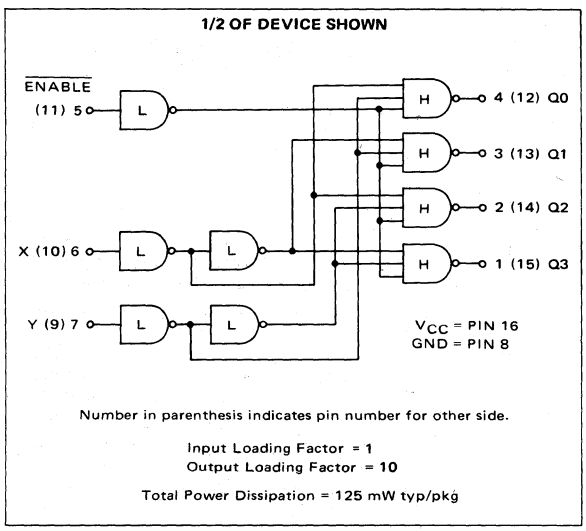
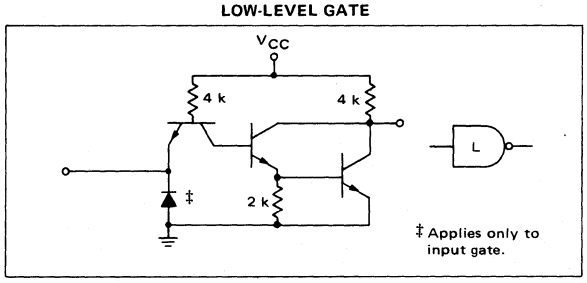
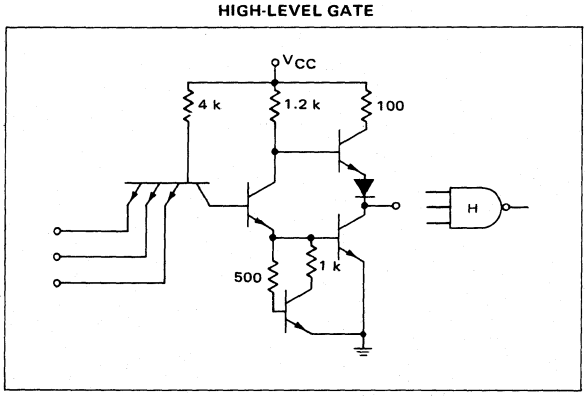


LOW-LEVEL GATE



HIGH-LEVEL GATE



*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin in-line plastic package (Case 612).

This device converts two lines of input data to a one-of-four output. The enable line provides an inhibit capability and also allows the decoder to be expanded for larger decoder systems.

The dual 2-input/4-output decoder consists of high-level and low-level gates internally connected for minimum power consumption and maximum driving capabilities. The enable gate must be in the low state to perform the decode operation shown in the truth table.

The propagation delays shown in the charts are typical and vary according to loading, interconnection wiring length, and the number of logic levels involved.

TRUTH TABLE

E = 0

X	Y	Q0	Q1	Q2	Q3
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

1 = High State
0 = Low State

TYPICAL TURN-ON DELAY TIMES (ns)
$T_A = 25^oC$

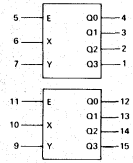
Input	Q0	Q1	Q2	Q3
X	11.5	15.5	11.5	15.5
Y	11.5	11.5	15.5	15.5
$\overline{E}$	13.5	13.5	13.5	13.5

TYPICAL TURN-OFF DELAY TIMES (ns)
$T_A = 25^oC$

Input	Q0	Q1	Q2	Q3
X	14.0	19.0	14.0	19.0
Y	14.0	14.0	19.0	19.0
$\overline{E}$	14.5	14.5	14.5	14.5

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner. Additionally, test all input-output combinations according to the truth table.



@Test Temperature	TEST CURRENT/VOLTAGE VALUES													
	mA					Volts								
	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
0°C	17.6	16	-1.6	1.0	-	1.1	2.0	0.4	2.5	4.5	-	5.0	4.75	5.25
+25°C	17.6	16	-1.6	1.0	-10	1.1	1.8	0.4	2.5	4.5	7.0	5.0	4.75	5.25
+75°C	17.6	16	-1.6	1.0	-	0.9	1.8	0.4	2.5	4.5	-	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4007 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														Gnd
			0°C		+25°C		+75°C			I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
			Min	Max	Min	Max	Min	Max																
Input																								
Forward Current	I_{F1}	5	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	-	-	-	-	5	-	-	-	-	-	16	8
Leakage Current	I_R	5	-	40	-	40	-	40	μAdc	-	-	-	-	-	-	-	-	5	-	-	-	-	16	8
Breakdown Voltage	BV_{in}	5	-	-	5.5	-	-	-	Vdc	-	-	-	5	-	-	-	-	-	-	-	-	-	16	8
Clamp Voltage	V_D	5	-	-	-	-1.5	-	-	Vdc	-	-	-	-	5	-	-	-	-	-	-	-	16	-	8
Output																								
Output Voltage	V_{OL1}	4	-	0.4	-	0.4	-	0.4	Vdc	4	-	-	-	-	5,6,7	-	-	-	-	-	-	16	-	8
	V_{OL2}	4	-	0.4	-	0.4	-	0.4	Vdc	-	4	-	-	-	5,6,7	-	-	-	-	-	-	16	-	8
	V_{OH}	4	2.5	-	2.5	-	2.5	-	Vdc	-	-	4	-	-	5,6	7	-	-	-	-	-	16	-	8
Short-Circuit Current	I_{SC}	4	-20	-60	-20	-60	-20	-60	mAdc	-	-	-	-	-	-	-	-	-	5	-	16	-	-	4,8
Power Requirements (Total Device)																								
Maximum Power Supply Current	I_{max}	16	-	-	-	51	-	-	mAdc	-	-	-	-	-	-	-	-	-	5,6,7,9,10,11	16	-	-	-	8
Power Supply Drain	I_{PD}	16	-	-	-	34	-	-	mAdc	-	-	-	-	-	-	-	5,11	-	6,7,9,10	-	16	-	-	8

11

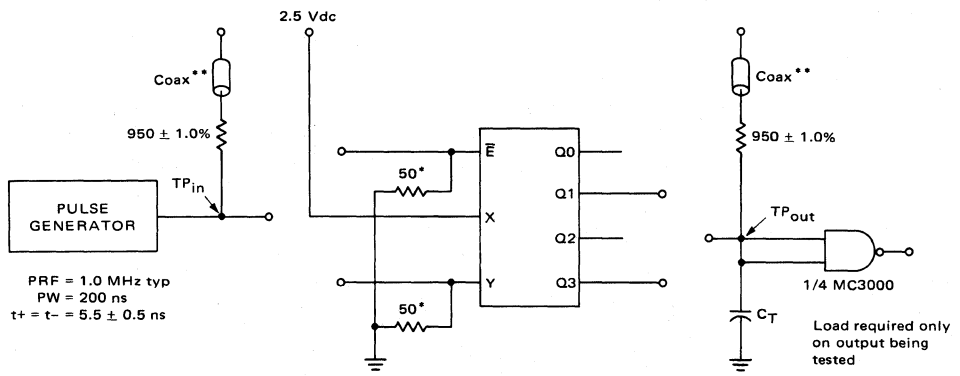
INPUT LOADING and OUTPUT DRIVING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT DRIVE FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

**Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

SWITCHING TIME TEST CIRCUIT



*Resistor used only on input under test.

**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

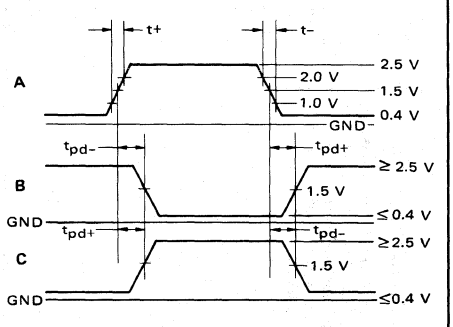
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

TEST PROCEDURES

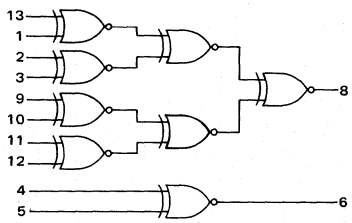
(Letters shown in test columns refer to waveforms.)

TEST	Ē	Y	Q1	Q3	LIMITS Max	LIMITS Unit
t_{pd+} (Y to Q1)	Gnd	A	C	–	20	ns
t_{pd-} (Y to Q1)	Gnd	A	C	–	17	ns
t_{pd+} (Y to Q3)	Gnd	A	–	B	29	ns
t_{pd-} (Y to Q3)	Gnd	A	–	B	23	ns
t_{pd+} (Ē to Q3)	A	2.5 V	–	C	21	ns
t_{pd-} (Ē to Q3)	A	2.5 V	–	C	20	ns

VOLTAGE WAVEFORMS



MC4308F,L*
MC4008F,L,P*



V_{CC} = Pin 14
GND = Pin 7

Positive Logic:
8 = 1⊙2⊙3⊙9⊙10⊙11⊙12⊙13
6 = 4⊙5
where $X \odot Y = (\bar{X} \bullet \bar{Y}) + (X \bullet Y)$

This device consists of seven Exclusive NOR gates connected to check even parity. The output will be in the logic "1" state as long as the "1" state is present on an even number of inputs. The additional Exclusive NOR gate can be used to connect two 8-bit parity trees to form a 16-bit parity tree, or it can be used to convert the parity tree to check odd parity by connecting one gate input to the output of the parity tree and grounding the other input. This conversion can also be accomplished by connecting a simple inverter to the output of the parity tree.

Input Loading Factor = 2
Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 15-30 ns typ

TYPICAL PROPAGATION DELAY TIMES

FIGURE 1 – THREE-GATE DELAY versus TEMPERATURE

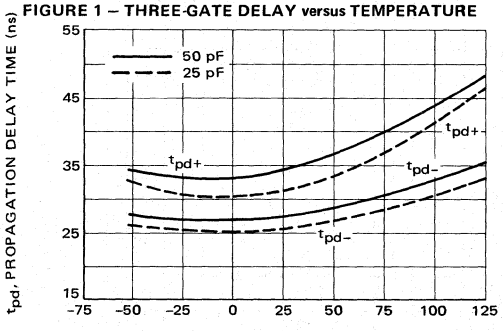


FIGURE 2 – ONE-GATE DELAY versus TEMPERATURE

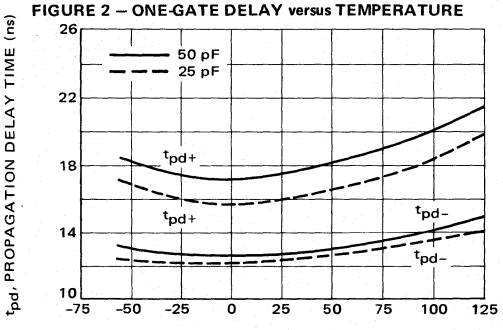


FIGURE 3 – DELAY versus LOAD CAPACITANCE

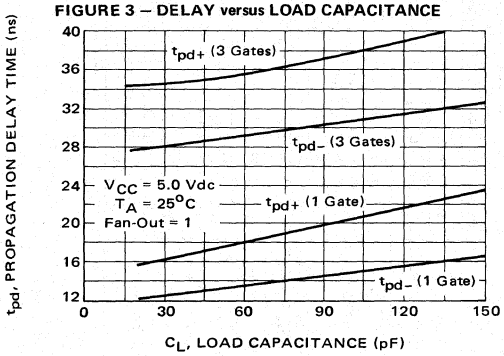
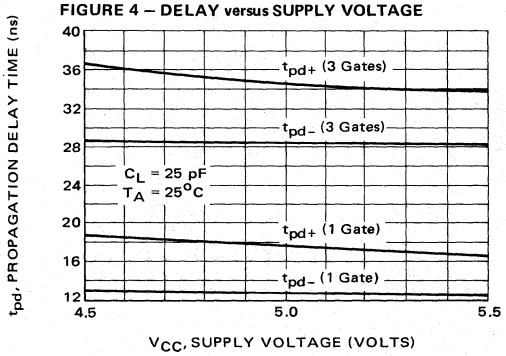


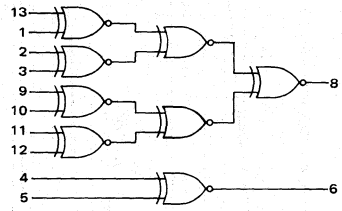
FIGURE 4 – DELAY versus SUPPLY VOLTAGE



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and output in the same manner. To complete testing, test all input-output combinations according to the logic equation.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC4308	-55°C	16	18.4	-1.6	–	–	1.1	2.0	0.4	2.4	4.0	–	5.0	4.5	5.5	–
	+25°C	16	18.4	-1.6	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.4
	+125°C	16	18.4	-1.6	–	–	0.8	1.8	0.4	2.4	4.0	–	5.0	4.5	5.5	–
MC4008	0°C	16	17.6	-1.6	–	–	1.1	2.0	0.4	2.5	4.0	–	5.0	4.75	5.25	–
	+25°C	16	17.6	-1.6	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.4
	+75°C	16	17.6	-1.6	–	–	0.9	1.8	0.4	2.5	4.0	–	5.0	4.75	5.25	–

Characteristic	Symbol	Pin Under Test	MC4308 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4008 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																														
Forward Current	I_F	1	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	mAdc	–	–	–	–	–	–	–	1	–	13	–	–	–	14	–	7
Leakage Current	I_R	1	–	80	–	80	–	80	–	80	–	80	–	80	μAdc	–	–	–	–	–	–	–	–	1	–	–	–	–	14	–	7,13
Breakdown Voltage	BV_{in}	1	–	–	5.5	–	–	–	–	–	5.5	–	–	–	Vdc	–	–	–	1	–	–	–	–	–	–	–	–	–	14	–	7,13
Clamp Voltage	V_D	1	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	1	–	–	–	–	–	–	–	–	14	–	7
Output																														
Output Voltage	V_{OL}	8	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	8	–	–	–	–	2,3,9,10,11,12,13	1	–	–	–	–	–	–	14	–	7
		8	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	–	8	–	–	–	2,3,9,10,11,12,13	1	–	–	–	–	–	14	–	–	7
	V_{OH}	8	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	8	–	–	1,2,3,9,10,11,12,13	–	–	–	–	–	–	14	–	–	7
Short-Circuit Current	I_{SC}	8	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	1,2,3,9,10,11,12,13	–	–	–	–	–	–	14	–	–	7,8
Power Requirements (Total Device)																														
Maximum Power Supply Current	I_{max}	14	–	–	–	58	–	–	–	–	–	58	–	–	mAdc	–	–	–	–	–	–	–	–	–	5,13	14	–	–	–	–	1,2,3,4,7 9,10,11,12
Power Supply Drain	I_{PD}	14	–	–	–	45	–	–	–	–	–	45	–	–	mAdc	–	–	–	–	–	–	–	–	–	5,13	–	14	–	–	–	1,2,3,4,7 9,10,11,12
Switching Parameters																Pulse In		Pulse Out												
Turn-On Delay	t_{pd-1}	1,8	–	–	–	46	–	–	–	–	–	46	–	–	ns	1		8		–	–	–	–	–	–	–	14	–	–	2,3,9,10,11,12	7,13
	t_{pd-2}	4,6	–	–	–	23	–	–	–	–	–	23	–	–	ns	4		6		–	–	–	–	–	–	–	14	–	–	–	5,7
Turn-Off Delay	t_{pd+1}	1,8	–	–	–	46	–	–	–	–	–	46	–	–	ns	1		8		–	–	–	–	–	–	–	14	–	–	2,3,9,10,11,12	7
	t_{pd+2}	4,6	–	–	–	23	–	–	–	–	–	23	–	–	ns	4		6		–	–	–	–	–	–	–	14	–	–	–	5,7

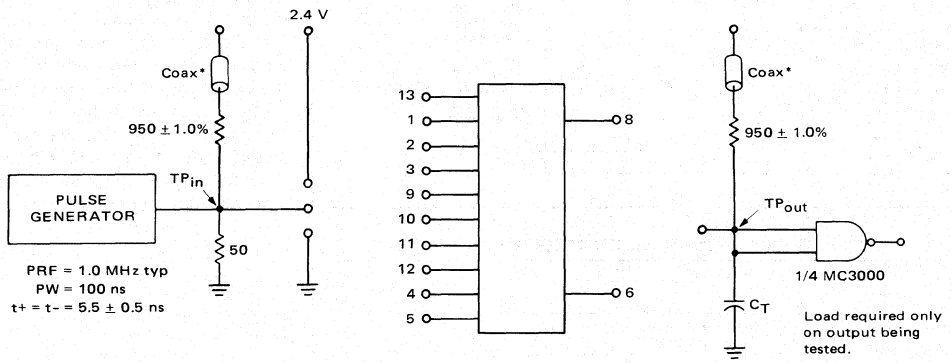
INPUT AND OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4308 INPUT LOADING FACTOR	MC4308 OUTPUT LOADING FACTOR
MC4300	1.0	10
MC500	1.2	12
MC2100	0.8	8
MC3100	0.8	8
MC5400	1.0	10
MC930	1.0*	10

FAMILY	MC4008 INPUT LOADING FACTOR	MC4008 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15*	12

*Applies only when input is being driven by MDTL gate with 2.0 kilohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.

SWITCHING TIME TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS

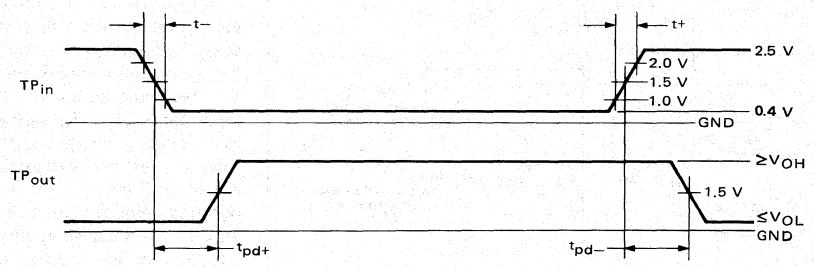
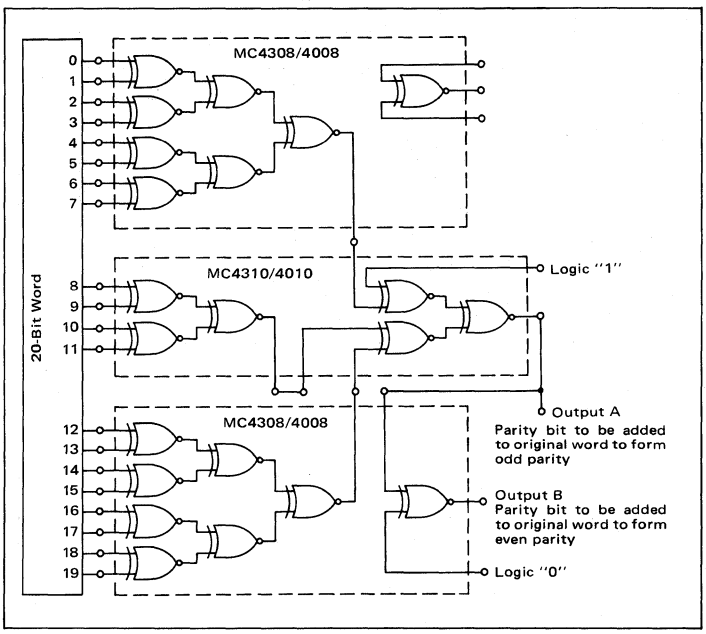


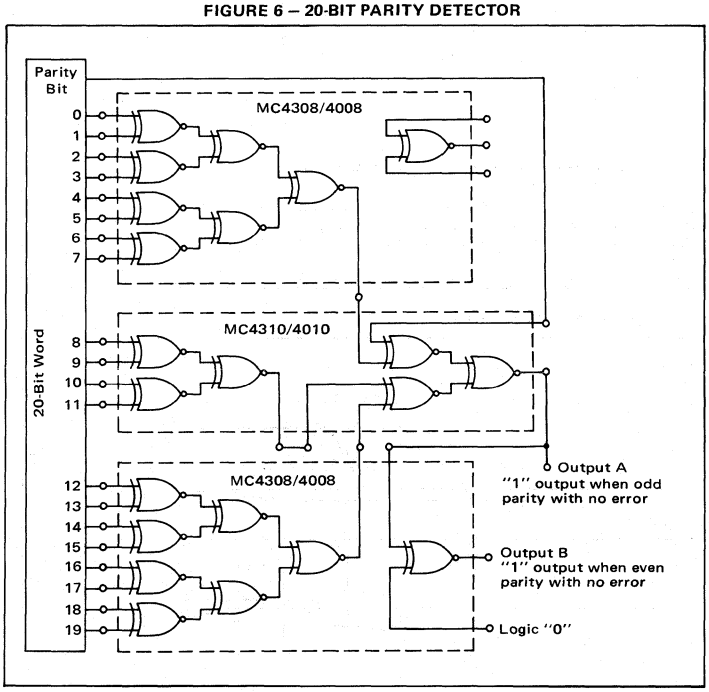
FIGURE 5 – 20-BIT PARITY GENERATOR



APPLICATIONS INFORMATION

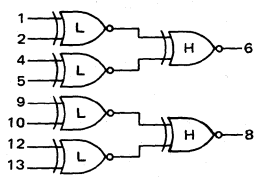
A parity generation tree (simple parity) for a 20-bit word is shown in Figure 5. It uses two MC4308/4008 8-bit parity trees and one MC4310/4010 dual 4-bit parity tree. If a parity word containing odd parity is required (i.e., the 20-bit word plus the parity bit are to contain an odd number of "1's"), the direct output from the parity tree (output A) is used as the parity bit. If even parity is required, the extra Exclusive-NOR gate in one MC4308/4008 provides the inversion when connected as indicated for output B.

FIGURE 6 – 20-BIT PARITY DETECTOR



A parity detection circuit for a 20-bit word is shown in Figure 6. The 20-bit word is connected to a two-stage parity tree identical to that used for the 20-bit parity generator; however, for the detection circuit the output of the tree must be compared with the input parity bit. The parity bit serves as an input to the second stage of the tree. For odd parity detection, output A will be a logic "1" if no error has occurred. For even parity detection, a logic "1" will appear at output B if no error has been introduced. Longer word lengths can be examined in a similar manner.

MC4010L, P *



V_{CC} = PIN 14
GND = PIN 7

Positive Logic:
6 = 1 ⊙ 2 ⊙ 4 ⊙ 5
where $X \odot Y = \overline{X} \cdot \overline{Y} + X \cdot Y$

Input Loading Factor = 2
Output Loading Factor = 10

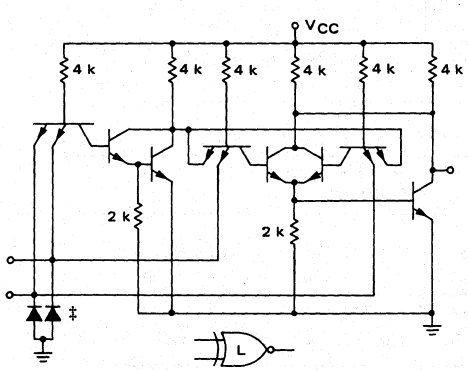
Total Power Dissipation = 125 mW typ/pkg
Propagation Delay Time = 9.5 to 22 ns typ

ADVANCE INFORMATION/NEW PRODUCT

Three Exclusive NOR gates are connected together to form each of the two 4-bit parity trees in the package. An even number of logic "1" states on the inputs will result in a logic "1" output state. An odd parity checker can be made by connecting an inverter to the output of the device.

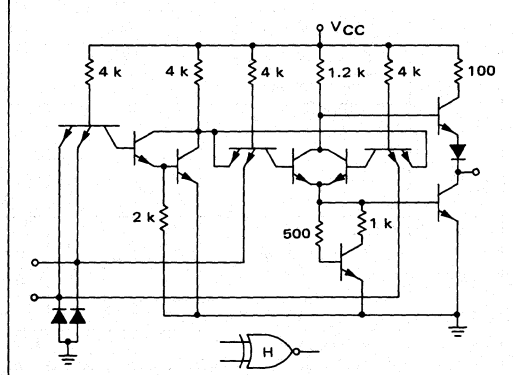
This function is constructed using low and high-level Exclusive NOR gates connected as shown in the logic diagram to maximize output drive capability and minimize power dissipation.

LOW-LEVEL GATE



‡Applies only to input gate.

HIGH-LEVEL GATE



*L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

**Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.

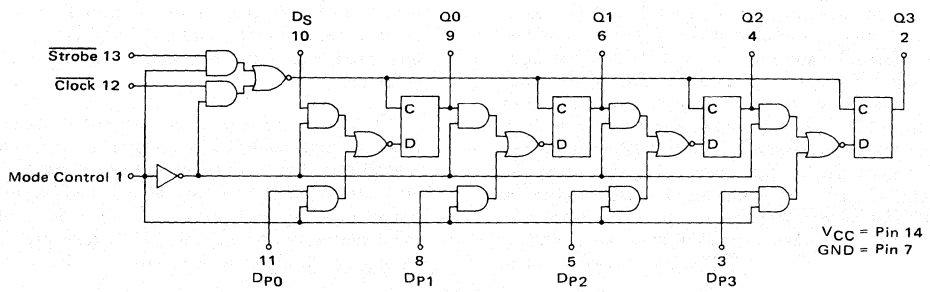
DC ELECTRICAL CHARACTERISTICS
(T_A = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input			
Forward Current	I_{F1}	-3.2 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 5.25 Vdc
	I_{F2}	-2.8 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 4.75 Vdc
Leakage Current	I_R	80 μAdc max	V_{in} = 2.5 Vdc, V_{CC} = 5.25 Vdc
Breakdown Voltage	BV_{in}	5.5 Vdc max	I_{in} = 1.0 mAdc, V_{CC} = 5.25 Vdc, T_A = 25°C
Clamp Voltage	V_D	-1.5 Vdc max	I_D = -10 mAdc, V_{CC} = 4.75 Vdc, T_A = 25°C
Threshold Voltage	V_{th} "1"	2.0 Vdc 1.8 Vdc	T_A = 0°C T_A = +25°C, or T_A = +75°C
	V_{th} "0"	1.1 Vdc 0.9 Vdc	T_A = 0°C, or T_A = +25°C T_A = +75°C
Output			
Output Voltage	V_{OL}	0.4 Vdc max 0.4 Vdc max	I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc† I_{OL} = 17.6 mAdc, V_{CC} = 5.25 Vdc†
	V_{OH}	2.5 Vdc min	I_{OH} = -1.6 mAdc, V_{CC} = 4.75 Vdc†
Short-Circuit Current	I_{SC}	-20 to -65 mAdc	V_{CC} = 5.0 Vdc, output grounded†

†These tests are performed according to the logic equations with a true input equal to V_{th} "1" and a false input equal to V_{th} "0".

MC4012L, P*

This 4-bit register provides parallel or serial data entry and retrieval, determined by the logic state of the mode control input. For parallel operation, set the mode control to the logic "1" state and strobe the information at the Dp inputs into the register. Serial left-shift operation is achieved in this mode by connecting the Q outputs to the Dp inputs of the previous stage. For serial right-shift operation, set the mode control to logic "0" and clock data into the register from D_S.



Input Loading Factor:
Mode Control = 5
Other Inputs = 1

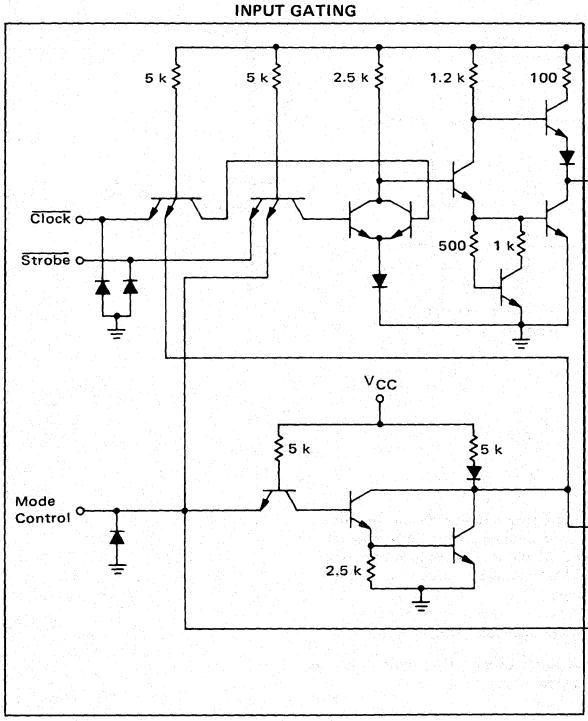
Output Loading Factor = 10

Total Power Dissipation = 180 mW typ/pkg

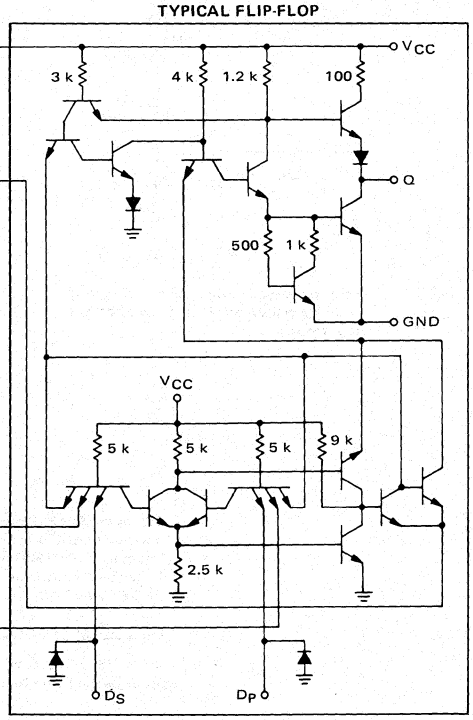
Propagation Delay Time = 25 ns typ/bit
t_{setup} "0" (Mode Control) = 25 ns typ
t_{setup} "1" (Mode Control) = 12 ns typ
t_{setup} "0" (D_{P0}, D_S) = 4.0 ns typ
t_{setup} "1" (D_{P0}, D_S) = 3.0 ns typ

t_{hold} "0" (Mode Control) 5.0 ns typ
t_{hold} "1" (Mode Control) 9.0 ns typ
t_{hold} "0" (D_{P0}, D_S) = 7.0 ns typ
t_{hold} "1" (D_{P0}, D_S) = 11 ns typ
f_{Tog} = 35 MHz typ @ 25°C

INPUT GATING



TYPICAL FLIP-FLOP



*L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

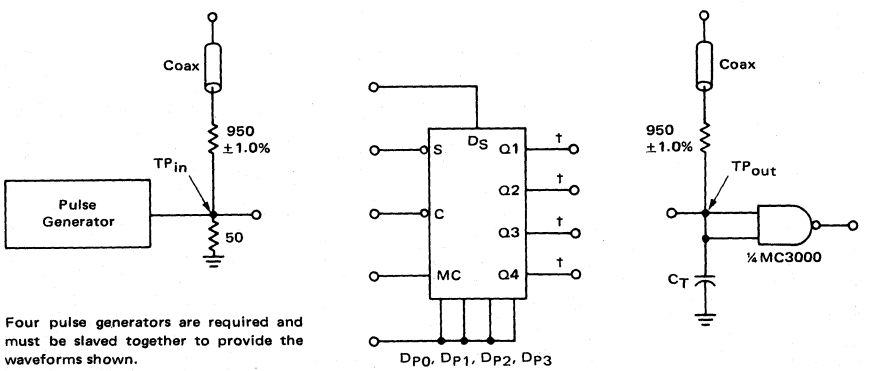
11

OPERATING CHARACTERISTICS

This shift register can be operated in the serial or parallel mode by properly setting the mode control. Data present on the four parallel inputs, D_{P0} through D_{P3}, can be strobed into the register by applying a logic "1" level to the mode control input and applying a positive pulse to the strobe input. The mode control must be in the logic "1" state a minimum of 30 ns prior to the strobe pulse. Operation in the serial mode can be achieved by setting the mode control input to a logic "0" state and applying a positive pulse to the clock input. The mode control must be set to the logic "0" state at least 20 ns prior to the clock pulse. The clock must be in the low state when the mode control is changed from the "0" to the "1" state. The strobe must be in the low state when the mode control is changed from the "1" to the "0" state. Information present on the data inputs between the setup and hold times will be transferred into the register during the negative transition of the clock or strobe.

To operate the register in the serial shift-right mode when the mode control is in the logic "0" state, serial data is applied to D_{P0}, and the clock input is toggled. To operate in the serial shift-left mode, externally connect each output to the parallel data input of the previous stage, set the mode control to the logic "1" state, apply serial data to D_{P3}, and clock the strobe input.

SWITCHING TIME TEST CIRCUIT



Four pulse generators are required and must be slaved together to provide the waveforms shown.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

†Load should be connected to each output during test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

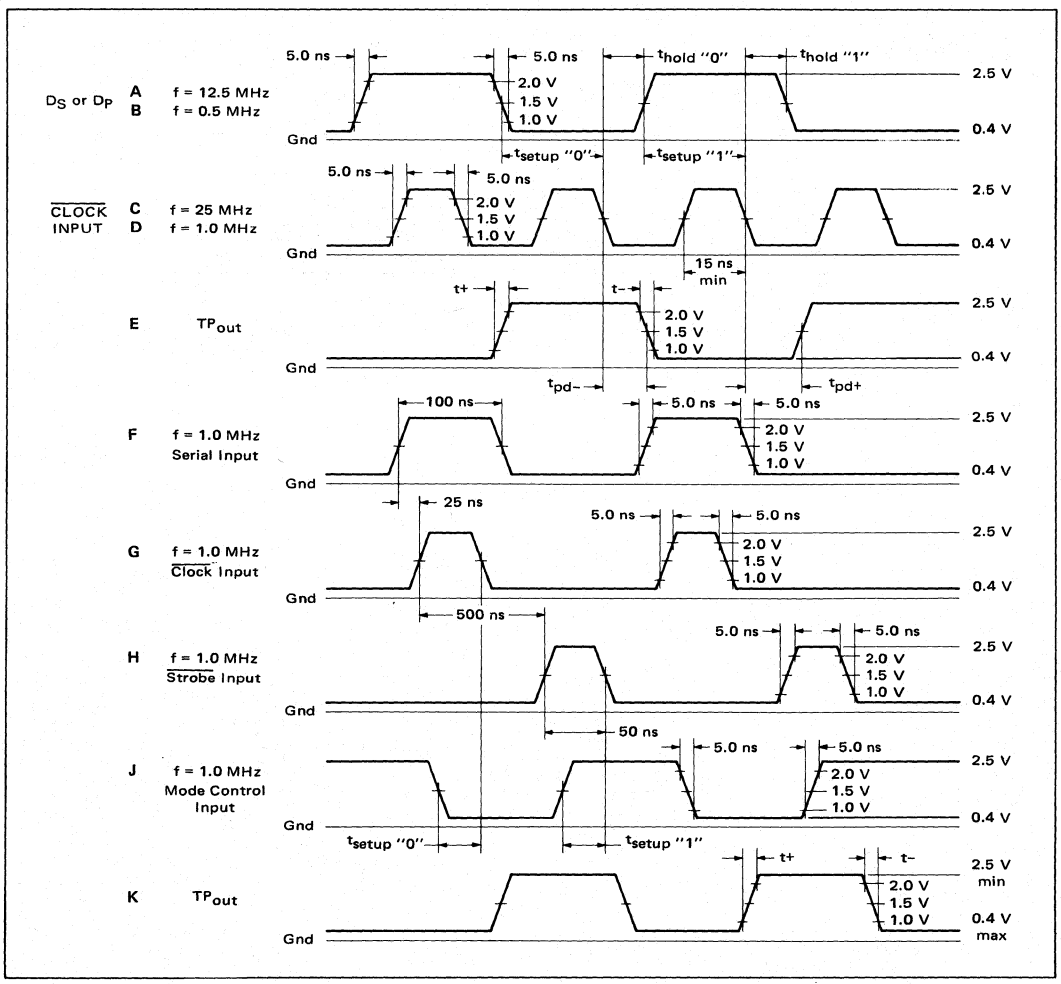
INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family

**Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.

VOLTAGE WAVEFORMS AND DEFINITIONS



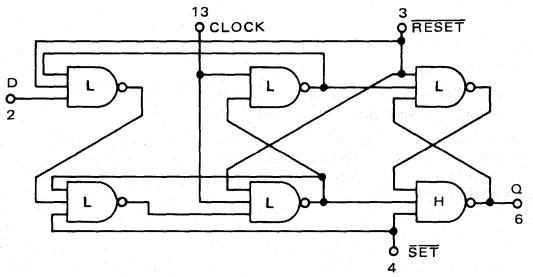
DC ELECTRICAL CHARACTERISTICS
(T_A = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input			
Forward Current — MC	I_{F1}	-8.0 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 5.25 Vdc
Others		-1.6 mAdc max	
MC	I_{F2}	-7.0 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 4.75 Vdc
Others		-1.4 mAdc max	
Leakage Current — MC	I_R	200 μAdc max	V_{in} = 2.5 Vdc, V_{CC} = 5.25 Vdc
Others		40 μAdc max	
Breakdown Voltage	BV_{in}	5.5 Vdc max	I_{in} = 1.0 mAdc, V_{CC} = 5.25 Vdc, T_A = 25°C
Clamp Voltage	V_D	-1.5 Vdc max	I_D = -10 mAdc, V_{CC} = 4.75 Vdc, T_A = 25°C
Threshold Voltage	V_{th} "1"	2.0 Vdc	T_A = 0°C
		1.8 Vdc	T_A = +25°C, or T_A = +75°C
	V_{th} "0"	1.1 Vdc	T_A = 0°C, or T_A = +25°C
		0.9 Vdc	T_A = +75°C
Output			
Output Voltage	V_{OL}	0.4 Vdc max	I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
		0.4 Vdc max	I_{OL} = 17.6 mAdc, V_{CC} = 5.25 Vdc
	V_{OH}	2.5 Vdc min	I_{OH} = -1.6 mAdc, V_{CC} = 4.75 Vdc
Short-Circuit Current	I_{SC}	-20 to -65 mAdc	V_{out} = 0 Vdc, V_{CC} = 5.0 Vdc

QUAD TYPE D FLIP-FLOP

MC4015L,P*

1/4 OF DEVICE SHOWN
(CLOCK AND $\overline{\text{RESET}}$ COMMON TO ALL FOUR FLIP-FLOPS)

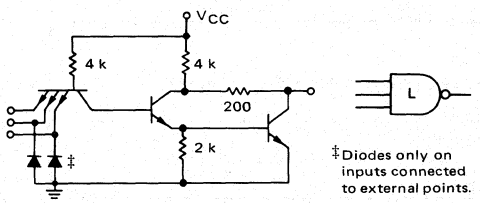


Input Loading Factor:
D = 1 CLOCK = 8
$\overline{\text{SET}}$ = 2 $\overline{\text{RESET}}$ = 8

V_{CC} = PIN 16
GND = PIN 8

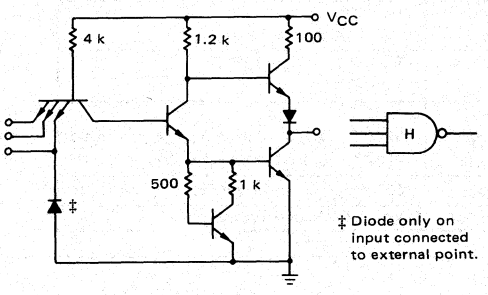
Output Loading Factor = 10
Total Power Dissipation = 190 mW typ/pkg
Propagation Delay Time = 16 ns typ
Setup Time = 10 ns max
Hold Time = 10 ns max
Operating Frequency = 30 MHz typ

LOW-LEVEL GATE



‡Diodes only on inputs connected to external points.

HIGH-LEVEL GATE

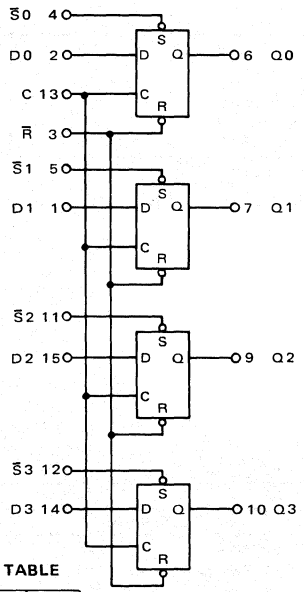


‡ Diode only on input connected to external point.

* L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

This quad type D flip-flop triggers on the positive edge of the clock input. During the clock transition the state of the D input is transferred to the Q output. The device is useful in shift registers and simple counters.

Power dissipation is minimized and output drive capability is maximized by connecting low and high-level gates as shown by the logic diagram to form each of the four flip-flops.



TRUTH TABLE

D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse
Q_n = time period following clock pulse

OPERATING CHARACTERISTICS

Data must be present at the D input 10 ns prior to the rise of the clock, and remain 10 ns after the clock signal rises. Data may be changed any time during the clock cycle except the interval between the setup time (10 ns) and the hold time (10 ns) without affecting the operation of the flip-flop. The data input is inhibited when the clock is high. When the clock is in the low state, the input steering section continually reflects the state of the D input. Information present at the D input during the time interval between the setup and hold times is transferred to the bistable section on the positive edge of the clock, and outputs Q and $\overline{\text{Q}}$ respond accordingly.

The flip-flops can be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct $\overline{\text{Set}}$ or $\overline{\text{Reset}}$ inputs.

11

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4015 INPUT LOADING FACTOR	MC4015 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	12
MC830	1.15**	10

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

**Applies only when input is being driven by MDTL gate with 2.0 kilohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input			
Forward Current — D	I_{F1}	-1.6 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 5.25 Vdc
$\overline{SET}$		-3.2 mAdc max	
$\overline{RESET}$, CLOCK		-12.8 mAdc max	
D	I_{F2}	-1.4 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 4.75 Vdc
$\overline{SET}$		-2.8 mAdc max	
$\overline{RESET}$, CLOCK		-11.2 mAdc max	
Leakage Current — D	I_R	40 μAdc max	V_{in} = 2.5 Vdc, V_{CC} = 5.25 Vdc
$\overline{SET}$		80 μAdc max	
$\overline{RESET}$, CLOCK		320 μAdc max	
Breakdown Voltage	BV_{in}	5.5 Vdc max	I_{in} = 1.0 mAdc, V_{CC} = 5.25 Vdc, T_A = 25°C
Clamp Voltage	V_D	-1.5 Vdc max	I_D = -10 mAdc, V_{CC} = 4.75 Vdc, T_A = 25°C
Threshold Voltage	V_{th} "1"	2.0 Vdc	T_A = 0°C
		1.8 Vdc	T_A = +25°C, or T_A = +75°C
	V_{th} "0"	1.1 Vdc	T_A = 0°C, or T_A = +25°C
		0.9 Vdc	T_A = +75°C
Output			
Output Voltage	V_{OL}	0.4 Vdc max	$\overline{RESET}$ = 0, I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
		0.4 Vdc max	$\overline{RESET}$ = 0, I_{OL} = 17.6 mAdc, V_{CC} = 5.25 Vdc
	V_{OH}	2.5 Vdc min	$\overline{SET}$ = 0, I_{OH} = -1.6 mAdc, V_{CC} = 4.75 Vdc
Short-Circuit Current	I_{SC}	-20 to -65 mAdc	V_{CC} = 5.0 Vdc, output grounded

PROGRAMMABLE MODULO-N
DECADE COUNTER

MC4316L • MC4016L,P*

PROGRAMMABLE MODULO-N
HEXADECIMAL COUNTER

MC4318L • MC4018L,P*

ADVANCE INFORMATION/NEW PRODUCT

These devices are programmable, cascadable, modulo-N counters. The MC4316/4016 can be programmed to divide by any number (N) from 0 thru 9, the MC4318/4018 from 0 thru 15.

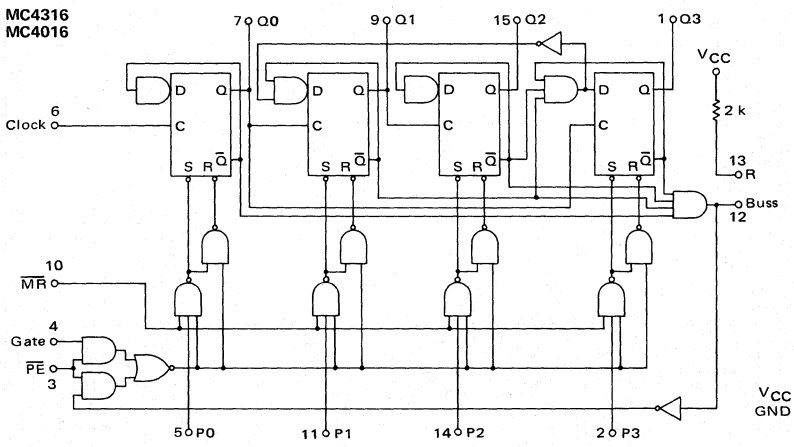
The $\overline{PE}$ input enables the parallel preset inputs P0 thru P3. All zeros are entered into the counter by applying a logic "0" level to the master reset ($\overline{MR}$) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All preset inputs are independent of the logic level of the Clock.

The Gate input and Buss node are useful in cascading of counters. A 2.0 kilohm pullup resistor to be used with the Buss node is provided internally (pin 13).

When the counters are used in divide-by-N capacity, the Buss output provides a pulse of width equal to the clock pulse and at an interval determined by N.

Modulo-N counters are useful in frequency synthesizers, in phase-locked-loops, and in other applications where a simple method for frequency division is needed.

MC4316
MC4016



COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

Both Types:

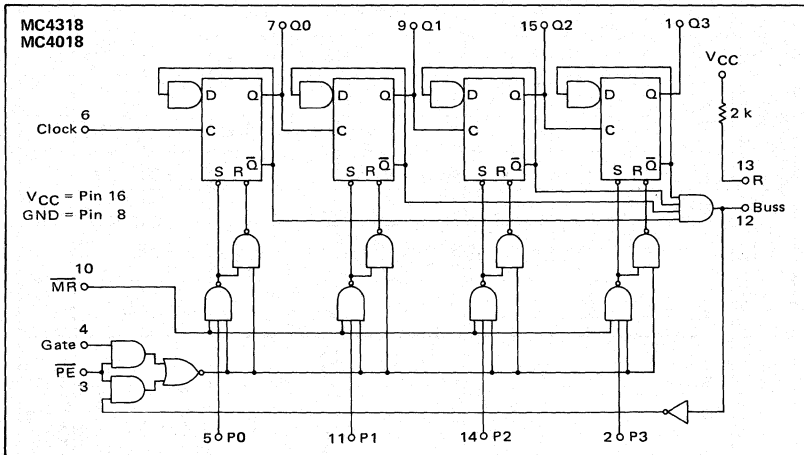
Input Loading Factor:
- Clock, $\overline{PE}$ = 2
- P0, P1, P2, P3, Gate = 1
- $\overline{MR}$ = 4

Output Loading Factor = 8

Total Power Dissipation = 250 mW typ/pkg

Propagation Delay Time:
- Clock to Q3 = 50 ns typ
- Clock to Buss = 35 ns typ

MC4318
MC4018

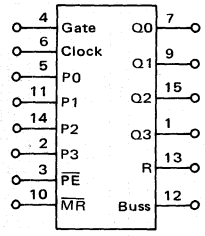


COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

*L suffix = 16-pin ceramic dual in-line package (Case 620).
P suffix = 16-pin plastic dual in-line package (Case 612).

ELECTRICAL CHARACTERISTICS

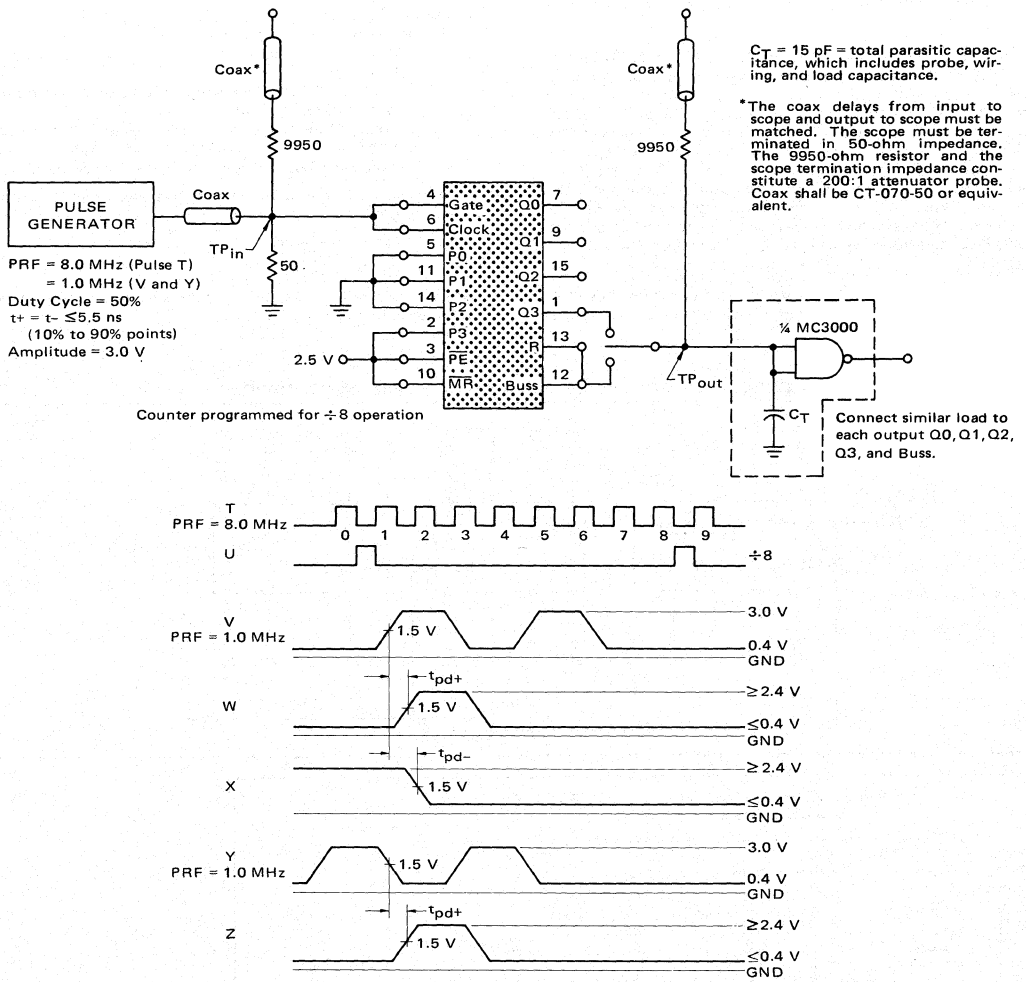
Tests are shown for one output only. Others are tested in the same manner.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{in}	Volts V_{IL}	V_{IH}	V_F	V_R	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
MC4316, MC4318	-55°C	12.8	13.8	9.6	-1.6	–	1.1	2.0	0.4	2.4	–	5.0	4.5	5.5
	+25°C	12.8	13.8	9.6	-1.6	1.0	1.1	1.8	0.4	2.4	8.0	5.0	4.5	5.5
	+125°C	12.8	13.8	9.6	-1.6	–	0.8	1.8	0.4	2.4	–	5.0	4.5	5.5
MC4016, MC4018	0°C	12.8	13.8	9.6	-1.6	–	1.1	2.0	0.4	2.5	–	5.0	4.75	5.25
	+25°C	12.8	13.8	9.6	-1.6	1.0	1.1	1.8	0.4	2.5	7.0	5.0	4.75	5.25
	+75°C	12.8	13.8	9.6	-1.6	–	0.9	1.8	0.4	2.5	–	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4316, MC4318 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4016, MC4018 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																													
Forward Current	I_{F1}	2	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	–	2	10	–	–	–	16	3,8
		3	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2		–	–	–	–	–	–	–	3	4	–	–	–		8,12
		4	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	4	3	–	–	–		8
		5	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	5	10	–	–	–		3,8
		6	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2		–	–	–	–	–	–	–	6	–	–	–	–		8
		10	–	-6.4	–	-6.4	–	-6.4	–	-6.4	–	-6.4	–	-6.4		–	–	–	–	–	–	–	10	2,5,11,14	–	–	–		3,8
		11	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	11	10	–	–	–		
		14	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	14	10	–	–	–		
	I_{F2}	2	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	mAdc	–	–	–	–	–	–	–	2	10	–	–	16	–	3,8
		3	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8		–	–	–	–	–	–	–	3	4	–	–		–	8,12
		4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	–	–	4	3	–	–		–	8
		5	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	–	–	5	10	–	–		–	3,8
		6	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8		–	–	–	–	–	–	–	6	–	–	–			8
		10	–	-5.6	–	-5.6	–	-5.6	–	-5.6	–	-5.6	–	-5.6		–	–	–	–	–	–	–	10	2,5,11,14	–	–		–	3,8
		11	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	–	–	11	10	–	–		–	
		14	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	–	–	14	10	–	–		–	
Leakage Current	I_R	2	–	40	–	40	–	40	–	40	–	40	–	40	μAdc	–	–	–	–	–	–	–	–	2	–	–	–	16	8,10
		3	–	80	–	80	–	80	–	80	–	80	–	80		–	–	–	–	–	–	–	–	3	–	–	–		4,8
		4	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	4	–	–	–		3,8
		5	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	5	–	–	–		8,10
		6	–	80	–	80	–	80	–	80	–	80	–	80		–	–	–	–	–	–	–	–	6	–	–	–		8
		10	–	160	–	160	–	160	–	160	–	160	–	160		–	–	–	–	–	–	–	–	10	–	–	–		2,5,8,11,14
		11	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	11	–	–	–		8,10
		14	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	14	–	–	–		8,10
Breakdown Voltage	BV_{in}	2	5.5	–	5.5	–	5.5	–	5.5	–	5.5	–	5.5	–	Vdc	–	–	–	–	2	–	–	–	–	–	–	–	16	8,10
		3		–		–		–		–		–		–		–	–	–	–	3	–	–	–	–	–	–	–		4,8
		4		–		–		–		–		–		–		–	–	–	–	4	–	–	–	–	–	–	–		3,8
		5		–		–		–		–		–		–		–	–	–	–	5	–	–	–	–	–	–	–		8,10
		6		–		–		–		–		–		–		–	–	–	–	6	–	–	–	–	–	–	–		8
		10		–		–		–		–		–		–		–	–	–	–	10	–	–	–	–	–	–	–		2,5,8,11,14
		11		–		–		–		–		–		–		–	–	–	–	11	–	–	–	–	–	–	–		8,10
		14		–		–		–		–		–		–		–	–	–	–	14	–	–	–	–	–	–	–		8,10
Output																													
Output Voltage	V_{OL}	1	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	1	–	–	–	–	2,3,5,11,14	–	–	–	–	–	16	–	8
		1	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4		–	1	–	–	–	2,3,5,11,14	–	–	–	–	–	–	16	
		12	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5		–	–	12	–	–	3	2,5,11,14	–	–	–	–	16	–	
	V_{OH}	1	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	–	1	–	3	2,5,11,14	–	–	–	–	16	–	8
		12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	–	–	12	2,3,5,11,14	–	–	–	–	–	16	–	8
Short-Circuit Current	I_{SC}	1	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	–	–	3	2,5,11,14	–	16	–	–	1,8
		13	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	8,13
Power Requirements (Total Device)																													
Power Supply Drain	I_{PD}	16	–	–	–	65	–	–	–	–	–	65	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	8

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



SWITCHING TIME TEST PROCEDURES (T_A = 25°C)
(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				OUTPUT		LIMITS		
		Clock Pin 6	Gate Pin 4	P0, P1, P2 Pins 5,11,14	P3, $\overline{PE}$, $\overline{MR}$ Pins 2,3,10	Buss, R Pins 12,13	Q3 Pin 1	Min	Max	Unit
Toggle Frequency (Check before measuring propagation delay.)	f_{Tog}	T	T	Gnd	2.5 V	–	U	8.0	–	MHz
Propagation Delay Clock to Buss	t_{pd+}	V	V	Gnd	2.5 V	W	–	–	65	ns
Propagation Delay Clock to Q3	t_{pd+}	Y	Y	Gnd	2.5 V	–	Z	–	35	ns
	t_{pd-}	V	V	Gnd	2.5 V	–	X	–	78	ns

OPERATING CHARACTERISTICS

Basic operation of the MC4316/4016 and MC4318/4018 is the same. When operated as single stages, the Gate and Clock inputs must be tied together. The internal pullup resistor must be connected to the Buss node (pin 13 to pin 12). The programmable counter is set to count down by a pre-determined number (N) before recycling, according to the binary code present at the parallel preset inputs, P0 thru P3 (see the truth table). The binary information at inputs P0 thru P3 is preset into the counter after applying a logic "0" to the $\overline{PE}$ input. Data may be entered synchronously or asynchronously while $\overline{PE}$ is low, or when outputs Q0, Q1, Q2 and Q3 are in the logic "0" state and the Clock is low.

The counters may be set to divide by 10 (MC4316/4016) or 16 (MC4318/4018) regardless of preset input states by applying a logic "0" to the Buss node. This, in effect, disables the preset inputs and causes a logic "0" to appear at the preset of each flip-flop of the counter. If a binary number greater than nine (1001) is applied to the preset inputs of the MC4316/4016, the counter will ignore the most significant bit and recognize only the three least significant bits.

Cascading of Counters

To cascade counters (Figure 1):

1. Connect Gate inputs of all stages to the Clock of the first stage.
2. Connect all Buss outputs to one common pullup resistor (2.0 kilohms, internal).
3. Connect the Clock input of each stage after the first stage to the Q3 output of the previous stage.
4. Take the divide-by-N pulse from the Buss outputs.

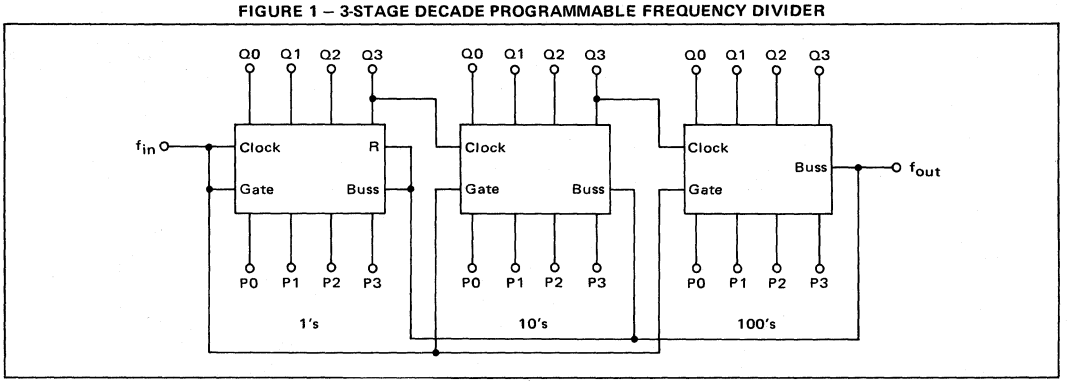
When cascaded, the count mode of the entire string of counters is defined by:

$$N = N_0 + 10\,N_1 + 100\,N_2 + \ldots \text{ (MC4316/4016)}$$

or $$N = N_0 + 16\,N_1 + 256\,N_2 + \ldots \text{ (MC4318/4018)}$$

where N_0, N_1, N_2, . . . are the BCD or binary numbers programmed at the zero, first, second, . . . stages.

FIGURE 1 – 3-STAGE DECADE PROGRAMMABLE FREQUENCY DIVIDER



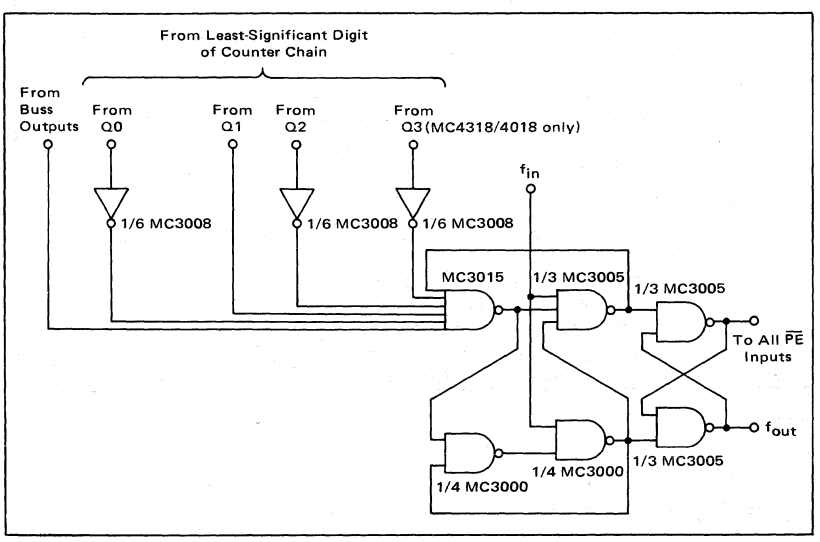


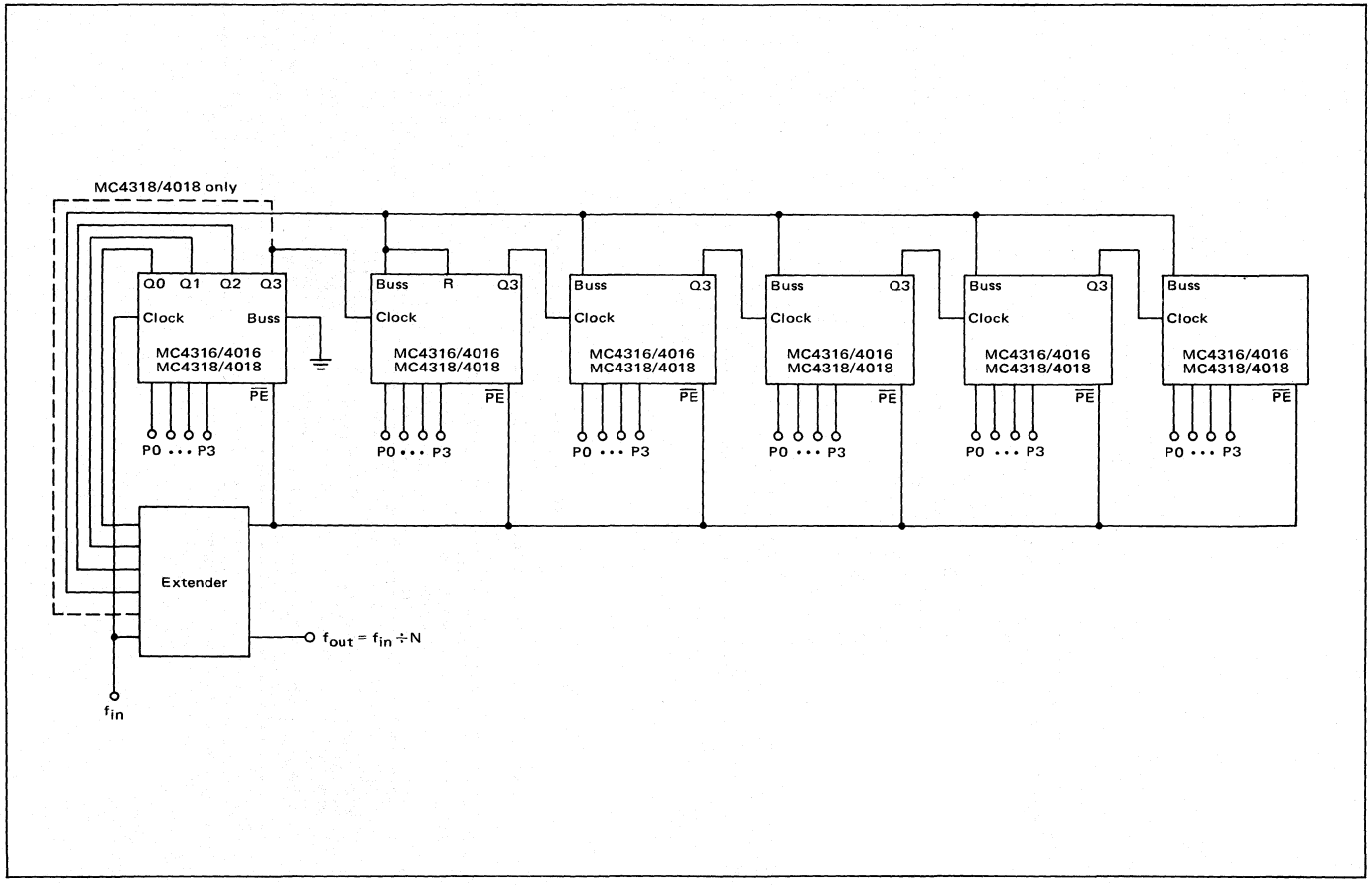
FIGURE 2 – FREQUENCY EXTENDER

APPLICATIONS INFORMATION

The maximum operating frequency of the MC4316/4016 or MC4318/4018 may be extended at the expense of decreased flexibility. By using the circuit shown in Figure 2 it is possible to extend the useful frequency (f_{tog}) of the counters to 25 MHz. It then becomes impossible to count by 0, 1, or 2. The output pulse width of the extended counter-chain is twice the width of the clock pulse.

Figure 3 shows the extended circuitry incorporated in a system of cascaded counters. The inverter shown connected by dotted lines is used only with the MC4318/4018.

FIGURE 3 – CASCADED PROGRAMMABLE COUNTER USING FREQUENCY EXTENDER

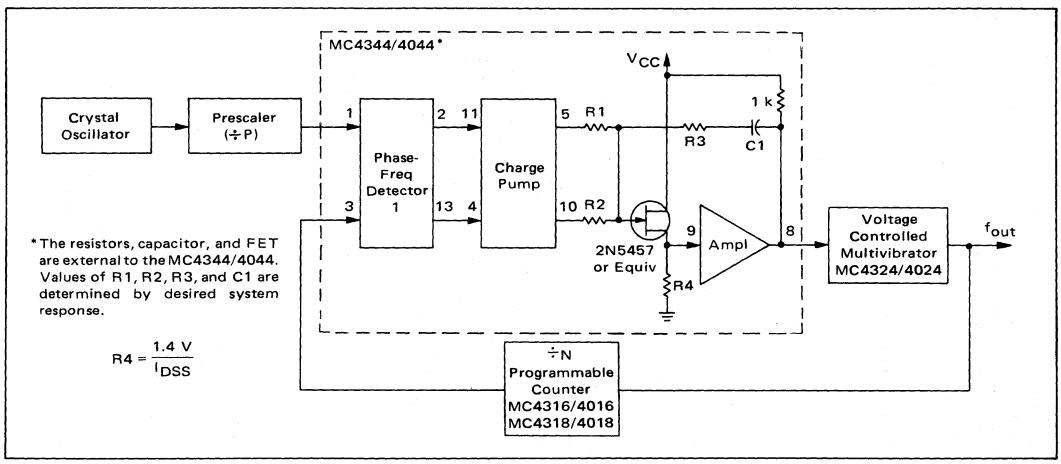


11

FIGURE 4 – PHASE-LOCKED, FREQUENCY SYNTHESIZER LOOP

Figure 4 shows the MC4316/4016 in a phase-locked loop with the MC4324/4024 and MC4344/4044. The loop has the following features:

1. Zero phase error between the reference frequency and the output of the divide-by-N feedback, achieved because phase-frequency detector 1 locks negative edges in the system;
2. Adjustable channel spacing, achieved by changing the pre-scaling factor (÷P) when generating the reference frequency;
3. Digitally programmed tuning of the output, in multiples of the reference frequency, accomplished by changing N in the divide-by-N chain in the feedback loop.



INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4316/4318 INPUT LOADING FACTOR	MC4316/4318 OUTPUT LOADING FACTOR
MC4300	1.0	8.0
MC500	1.1	10
MC2100	0.75	6.6
MC3100	0.8	6.4
MC5400	1.0	8.0
MC9300	1.0	8.6
MC930*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 6 (2.0 k ohm pullup)	9.1

FAMILY	MC4016/4018 INPUT LOADING FACTOR	MC4016/4018 OUTPUT LOADING FACTOR
MC4000	1.0	8.0
MC400	1.0	8.0
MC2000	0.66	5.3
MC3000	0.8	6.4
MC7400	1.0	8.0
MC8300	1.0	8.6
MC830*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 6 (2.0 k ohm pullup)	8.3

*Due to logic "1" state drive limitations of the MDTL family.

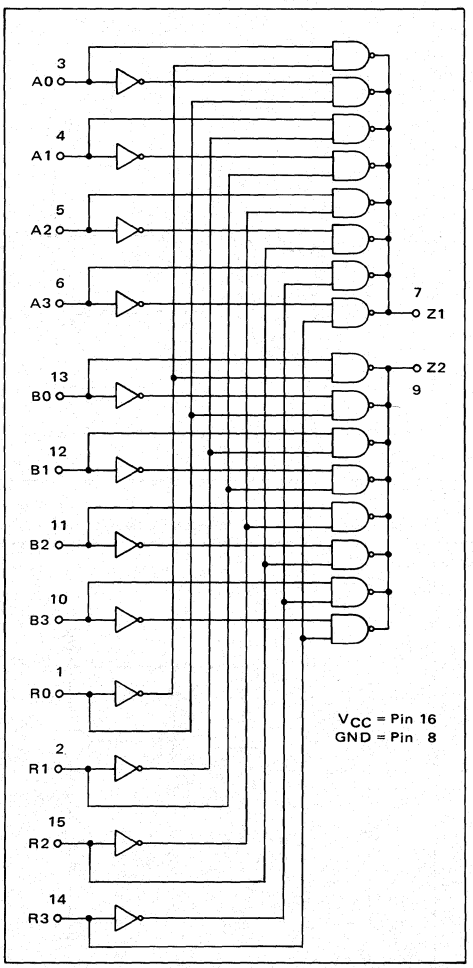
MC4021P • MC4022P*

Advance Information

The 4-bit comparator compares four bits of input information to four bits of reference information. When each bit of the input information is the same as its corresponding reference information, bit for bit, the output of the comparator will be in the high ("1") state. For any other condition, the output of the comparator will be in the low ("0") state.

In this dual 4-bit comparator, the four reference inputs (R) serve both comparators. There is no interrelation between the A and B data inputs of the dual comparator. Output Z1 reflects comparison of the A and R bits, while output Z2 shows conditions at inputs B and R.

The MC4021 has open-collector outputs; the MC4022 has totem-pole outputs.



A0	A1	A2	A3	B0	B1	B2	B3	R0	R1	R2	R3	Z1	Z2
0	0	0	0	0	0	1	1	0	0	0	0	1	0
0	0	0	0	0	0	1	1	0	0	0	1	0	0
0	0	0	0	0	0	1	1	0	0	1	0	0	0
0	0	0	0	0	0	1	1	0	0	1	1	0	1
0	1	1	0	0	1	0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	1	0	1	0	1	0	1
0	1	1	0	0	1	0	1	0	1	1	0	1	0
0	1	1	0	0	1	0	1	0	1	1	1	0	0
1	0	0	1	1	0	0	0	1	0	0	0	0	1
1	0	0	1	1	0	0	0	1	0	0	1	1	0
1	0	0	1	1	0	0	0	1	0	1	0	0	0
1	0	0	1	1	0	0	0	1	0	1	1	0	0
1	1	1	1	1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	1	1	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Input Loading Factor = 2
Output Loading Factor = 10
Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time = 20 ns typ

This is advance information on a new introduction and specifications are subject to change without notice.

*P suffix = 16-pin dual in-line plastic package (Case 612).

MC4023F, L, P*

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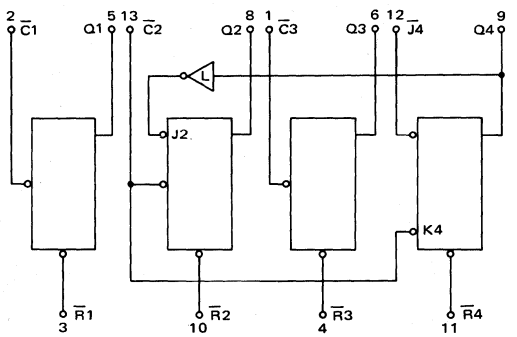
ADVANCE INFORMATION/NEW PRODUCT



V_{CC} = Pin 14
GND = Pin 7

Input Loading Factor:
J̄ = 1
C̄1, C̄3 = 2
C̄2, R̄ = 3

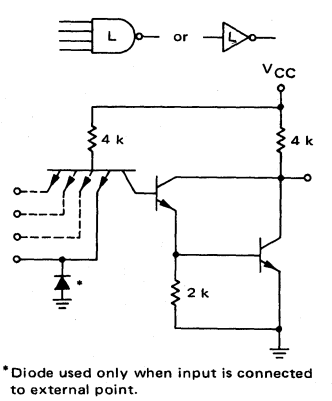
Output Loading Factor = 10

Total Power Dissipation = 200 mW typ/pkg
Propagation Delay Time = 16 ns typ/bit
Operating Frequency = 30 MHz typ

This device is a 4-bit counter with internally connected feedback. Inputs and outputs can be connected to count to any number between two and twelve except seven and eleven. Reset inputs are provided on each flip-flop to allow direct setting of the Q outputs to zero any time during the counting cycle.

Each flip-flop in the counter is built from high and low-level gates as shown by the logic diagram. The flip-flops and the feedback inverter are connected as shown by the block diagram to provide minimum power dissipation and maximum drive capability.

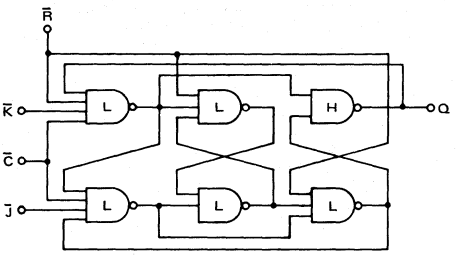
LOW-LEVEL GATE



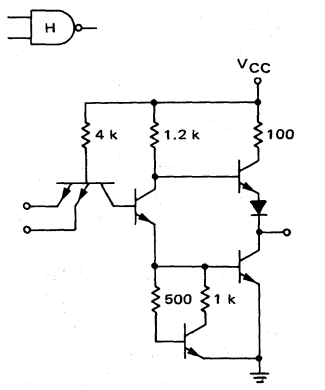
*Diode used only when input is connected to external point.

LOGIC DIAGRAM

One flip-flop shown. Only inputs shown on block diagram are present.



HIGH-LEVEL GATE



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

INPUT LOADING and OUTPUT DRIVING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT DRIVE FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family

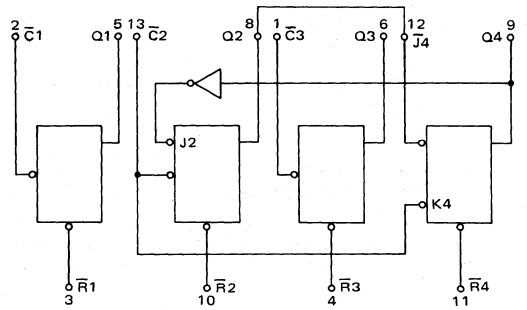
**Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input			
Forward Current — J	I_{F1}	-1.6 mAdc max	
C1, C3		-3.2 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 5.25 Vdc
C2, R		-4.8 mAdc max	
J	I_{F2}	-1.4 mAdc max	
C1, C3		-2.8 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 4.75 Vdc
C2, R		-4.2 mAdc max	
Leakage Current — J	I_R	40 μAdc max	
C1, C3		80 μAdc max	V_{in} = 2.5 Vdc, V_{CC} = 5.25 Vdc
C2, R		120 μAdc max	
Breakdown Voltage	BV_{in}	5.5 Vdc max	I_{in} = 1.0 mAdc, V_{CC} = 5.25 Vdc, T_A = 25°C
Clamp Voltage	V_D	-1.5 Vdc max	I_D = -10 mAdc, V_{CC} = 4.75 Vdc, T_A = 25°C
Threshold Voltage	V_{th} "1"	2.0 Vdc	T_A = 0°C
		1.8 Vdc	T_A = +25°C, or T_A = 75°C
	V_{th} "0"	1.1 Vdc	T_A = 0°C, or T_A = +25°C
		0.9 Vdc	T_A = +75°C
Output			
Output Voltage	V_{OL}	0.4 Vdc max	I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
		0.4 Vdc max	I_{OL} = 17.6 mAdc, V_{CC} = 5.25 Vdc
	V_{OH}	2.5 Vdc max	I_{OH} = -1.6 mAdc, V_{CC} = 4.75 Vdc
Short-Circuit Current	I_{SC}	-20 to -65 mAdc	V_{out} = 0 Vdc, V_{CC} = 5.0 Vdc

COUNTING SEQUENCES



DIVIDE BY 3

$\bar{C}2$	Q2	Q4
0	0	0
1	1	0
2	0	1

DIVIDE BY 4

$\bar{C}1$	Q1	Q3
0	0	0
1	1	0
2	0	1
3	1	1

DIVIDE BY 6

$\bar{C}1$	Q1	Q2	Q4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1

DIVIDE BY 12

$\bar{C}3$	Q3	Q1	Q2	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1

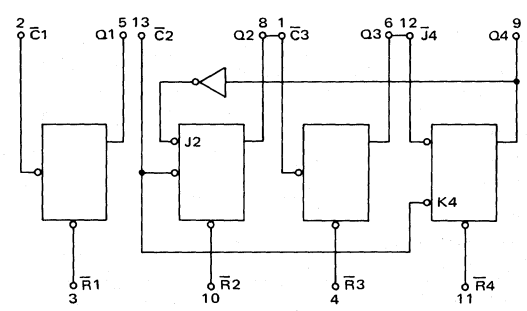
DIVIDE BY 2: Use flip-flop 1 or 3.

DIVIDE BY 3: Use flip-flops 2 and 4, connected as shown. The input signal is applied to $\bar{C}2$; the output is taken from Q4.

DIVIDE BY 4: Use flip-flops 1 and 3; connect Q1 to $\bar{C}3$. Apply the input signal to $\bar{C}1$.

DIVIDE BY 6: In addition to the connection for divide by 3, connect Q1 to $\bar{C}2$. Apply the input signal to $\bar{C}1$.

DIVIDE BY 12: In addition to the connections for divide by 6, connect Q3 to $\bar{C}1$. Apply the input signal to $\bar{C}3$.



DIVIDE BY 5

$\bar{C}2$	Q2	Q3	Q4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1

DIVIDE BY 8

$\bar{C}1$	Q1	Q2	Q3
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

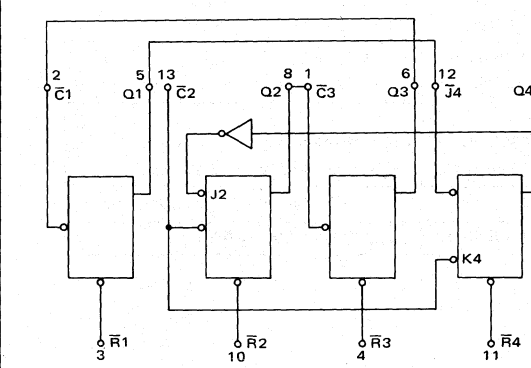
DIVIDE BY 10

$\bar{C}1$	Q1	Q2	Q3	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

DIVIDE BY 5: Connect flip-flops 2, 3, and 4 as shown. The input signal is applied to $\bar{C}2$; the output is taken from Q4.

DIVIDE BY 8: Connect flip-flops 2 and 3 as shown for divide by 5, but do not connect Q3 to $\bar{J}4$. Connect Q1 to $\bar{C}2$. The input signal is applied to $\bar{C}1$; the output is taken from Q3.

DIVIDE BY 10: In addition to the connections for divide by 5, connect Q1 to $\bar{C}2$. Apply the input signal to $\bar{C}1$.



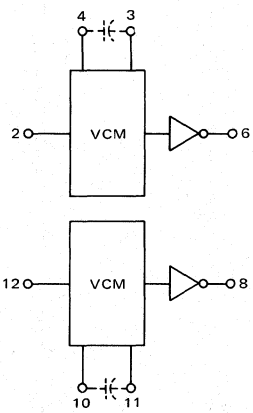
DIVIDE BY 9

$\bar{C}2$	Q2	Q3	Q1	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1

DIVIDE BY 9: The input signal is applied to $\bar{C}2$; the output is taken from Q4.

DUAL
VOLTAGE-CONTROLLED
MULTIVIBRATOR

MC4324F, L*
MC4024F, L, P*



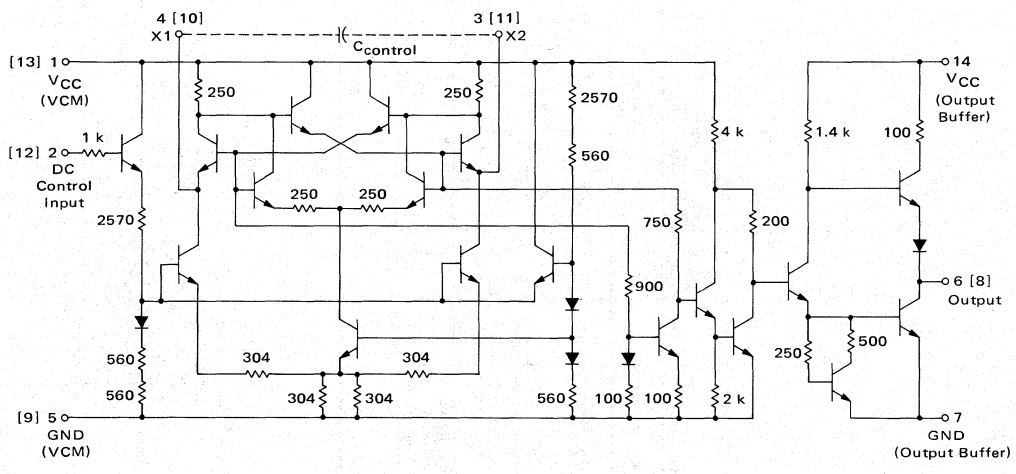
The MC4324/4024 voltage-controlled multivibrator provides appropriate level shifting to produce an output compatible with MTTL logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single capacitor. Variation of the output frequency over a 3.5 to 1 range is possible with an input dc control voltage of +1.0 to +5.0 volts.

Voltage-controlled multivibrators are used in phase-locked loops for digital frequency control. They may also be used for some types of A to D converters.

V_{CC}: VCM = 1, 13
Output Buffer = 14
GND: VCM = 5, 9
Output Buffer = 7
External Capacitor for
Frequency Range Determination
Output Loading Factor = 7
Power Dissipation = 150 mW typ/pkg
Maximum Operating Frequency = 30 MHz typ

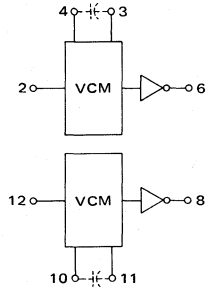
CIRCUIT SCHEMATIC

1/2 OF CIRCUIT SHOWN
(Numbers in brackets are pin numbers for other half.)



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

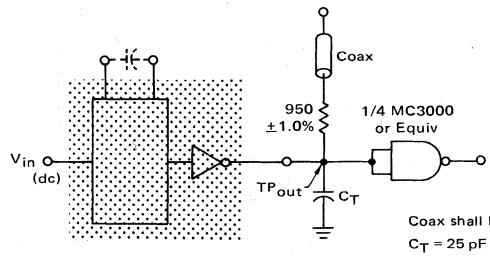
ELECTRICAL CHARACTERISTICS

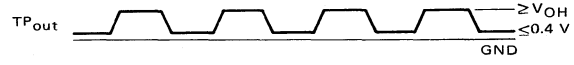


	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	Volts V_{IH}	V_{CC}	V_{CCL}	V_{CCH}
MC4324	-55°C	9.8	11.2	-1.6	5.0	5.0	4.5	5.5
MC4324	+25°C	9.8	11.2	-1.6	5.0	5.0	4.5	5.5
MC4324	+125°C	9.8	11.2	-1.6	5.0	5.0	4.5	5.5
MC4024	0°C	9.8	11.2	-1.6	5.0	5.0	4.75	5.25
MC4024	+25°C	9.8	11.2	-1.6	5.0	5.0	4.75	5.25
MC4024	+75°C	9.8	11.2	-1.6	5.0	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4324 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4024 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	V_{IH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																							
Forward Current	I_{in}	2	–	40	–	40	–	40	–	40	–	40	–	40	μAdc	–	–	–	2	–	–	14	5,7,9
		12	–	40	–	40	–	40	–	40	–	40	–	40	μAdc	–	–	–	12	–	–	14	5,7,9
Output																							
Output Voltage	V_{OL}	6	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	6	–	–	2	–	1,4,14	–	5,7,9
		8	–	↓	–	↓	–	↓	–	↓	–	↓	–	↓	↓	8	–	–	12	–	10,13,14	–	↓
		6	–		–		–		–		–		–			–	6	–	2	–	–	1,4,14	
		8	–		–		–		–		–		–			–	8	–	12	–	–	10,13,14	
	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	6	2	–	1,3,14	–	5,7,9
		8	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	8	12	–	11,13,14	–	5,7,9
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	–	–	–	2	1,3,14	–	–	5,6,7,9
		8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	–	–	–	12	11,13,14	–	–	5,7,8,9
Power Requirements (Total Device)																							
Power Supply Drain	I_{PD}	1,3,14	–	–	–	37	–	–	–	–	–	37	–	–	mAdc	–	–	–	2,4,10,12	1,13,14	–	–	5,7,9

AC TEST CIRCUIT AND WAVEFORMS





Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

AC TEST LIMITS

TEST	SYMBOL	CONDITIONS	LIMITS Min
Maximum Operating Frequency	f_{max}	$C_{control}$ = 10 pF, V_{in} = 5.0 Vdc Frequency Ratio = 3.5:1	25 MHz
Ratio of Frequency of Oscillation over Specified Input Voltage Range	$\frac{f_{high}}{f_{low}}$	$C_{control}$ = 100 pF, V_{in} high = 5.0 Vdc, V_{in} low = 1.0 Vdc	3.5:1.0

OPERATING CHARACTERISTICS

The operating frequency range of this multivibrator is controlled by the value of an external capacitor that is connected between X1 and X2. Either of the two equations shown below may be used to define the value of $C_{control}$:

$$C_{control} = \frac{500}{f_{max}}\ \mu F, \quad \text{or} \quad C_{control} = \frac{100}{f_{min}}\ \mu F,$$

with f given in Hz. The maximum operating frequency of this device is typically 30 MHz.

Three power supply and three ground connections are provided in this circuit. Each multivibrator has a separate power supply and ground connection. The output buffers have a common power supply and ground pin. This provides isolation between VCM's and minimizes the effect of output buffer transients on the multivibrators in critical applications. This separation of power supply and ground lines also provides the capability of disabling one VCM by disconnecting its V_{CC} pin. All grounds must always be connected to insure substrate grounding and proper isolation.

The output buffer transforms the logic levels of the VCM to MTTL logic levels.

FIGURE 1 – INPUT VOLTAGE versus OUTPUT FREQUENCY (15 pF FEEDBACK CAPACITOR)

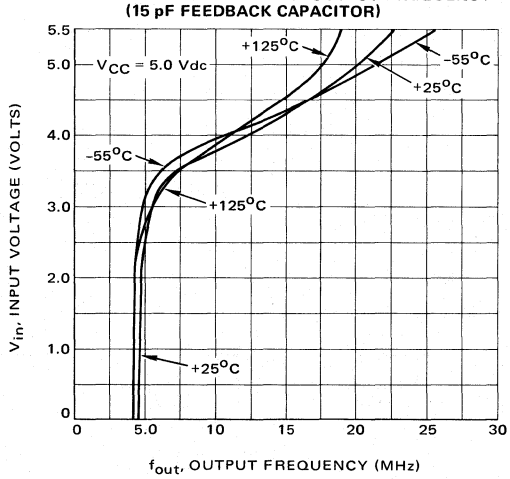


FIGURE 2 – INPUT VOLTAGE versus OUTPUT FREQUENCY (100 pF FEEDBACK CAPACITOR)

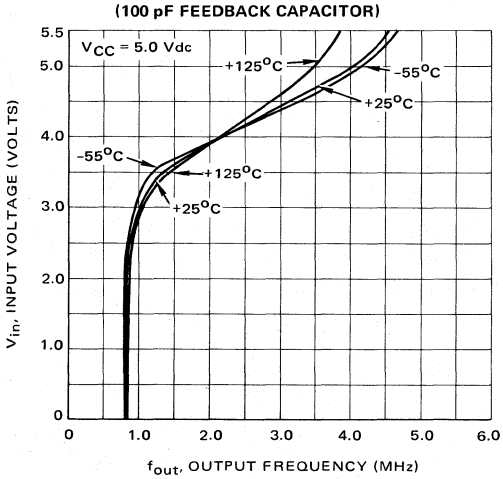
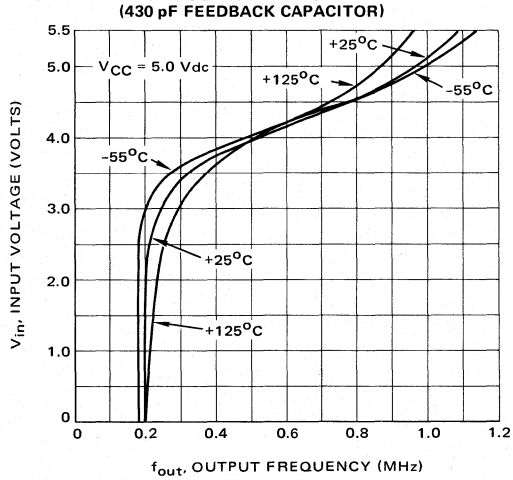


FIGURE 3 – INPUT VOLTAGE versus OUTPUT FREQUENCY (430 pF FEEDBACK CAPACITOR)



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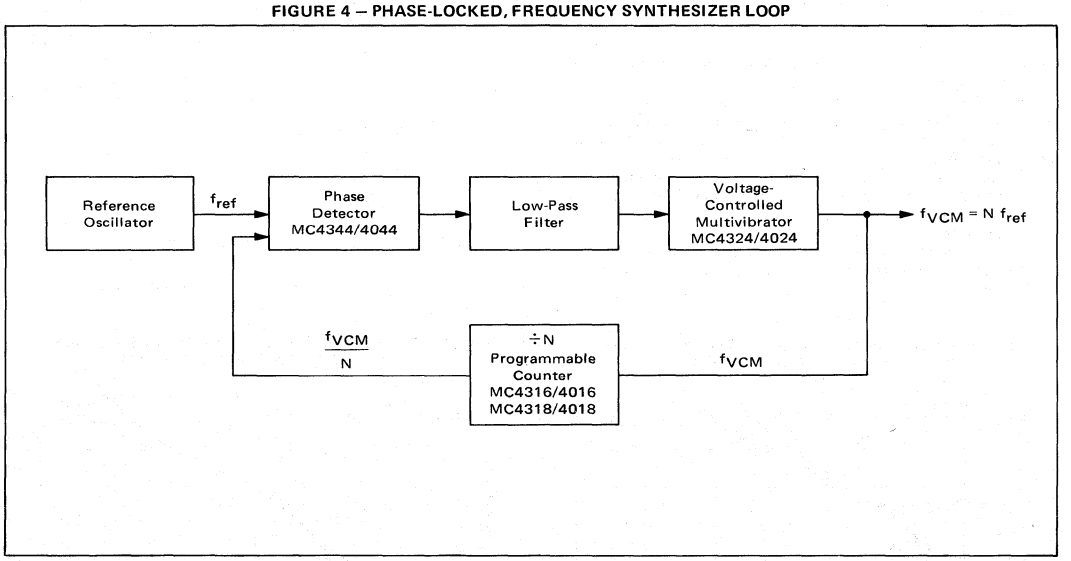
APPLICATIONS INFORMATION

The basic frequency synthesizer loop shown in Figure 4 consists of five basic components: the reference oscillator, the phase detector, the low-pass filter, the voltage controlled multivibrator/oscillator, and the divide by N counter.

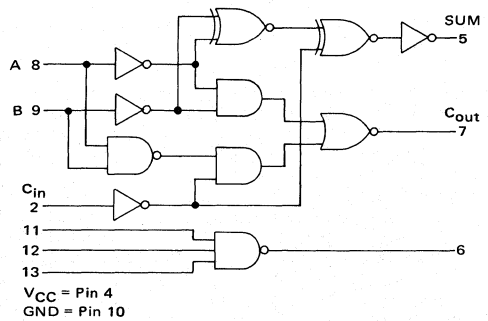
This loop achieves a stable state when $f_{VCM} = N f_{ref}$. When this condition does not exist the VCM searches through its frequency spectrum until it finds the frequency at which the stable state occurs. At this point the loop locks. This system allows the generation of many discrete frequencies from a single, highly stable source (f_{ref}). A system such as this has many useful applications in communications (frequency control systems), computer systems (for synchronizing data tracks and clocking systems), in instruments (frequency synthesizers and counters) and filter networks.

In addition to its function in the phase-locked loop, the VCM may be used as a fixed oscillator (plug crystal into capacitor pins and ground control input), in simple A to D converter systems, and as an FM modulator.

FIGURE 4 – PHASE-LOCKED, FREQUENCY SYNTHESIZER LOOP



MC4326F,L • MC4327F,L*
MC4026F,L,P • MC4027F,L,P*



These full adders are designed for serial and ripple-carry parallel adder systems. True Sum and Carry are produced at the output from the input information. A separate 3-input NAND gate is provided on the monolithic chip to provide the inverted Sum or Carry output.

Input Loading Factor:
A, B = 2
C_{in}, Pins 11, 12, 13 = 1

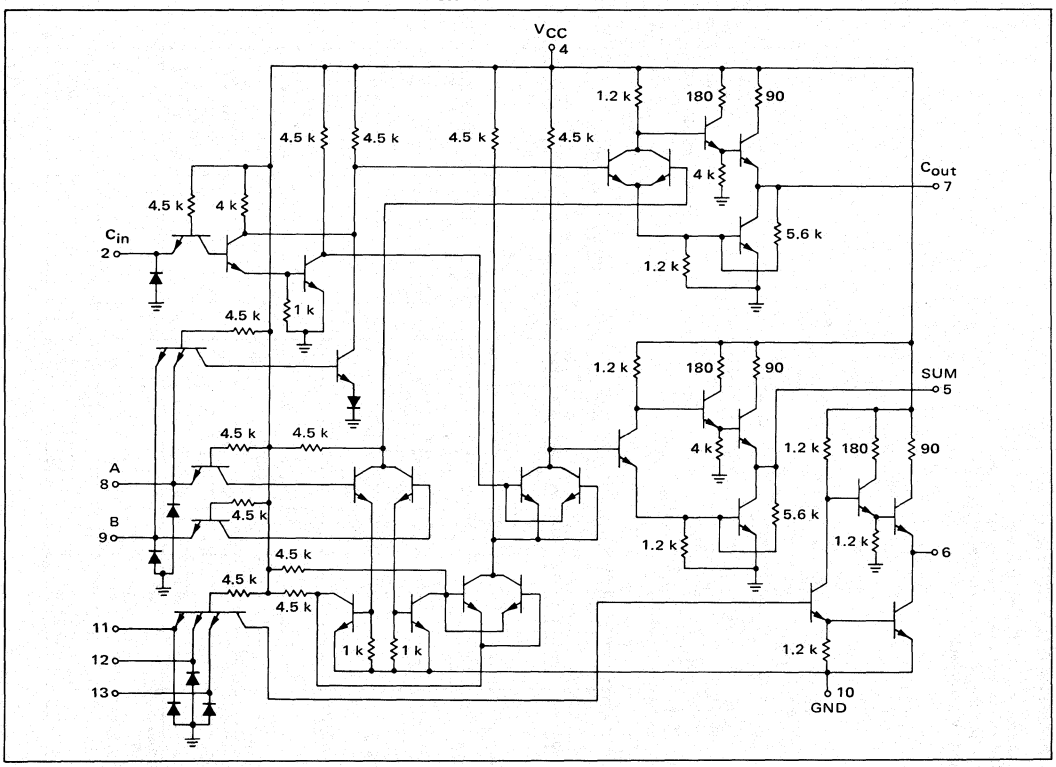
Output Loading Factor:
MC4326 = 15 MTTL I Loads
MC4327 = 7 MTTL I Loads
MC4026 = 12 MTTL I Loads
MC4027 = 6 MTTL I Loads

TRUTH TABLE

Input Pins			Output Pins	
8	9	2	5	7
A	B	C_{in}	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Total Power Dissipation = 90 mW typ/pkg
Add Delay = 25 ns typ
Carry Delay = 13 ns typ

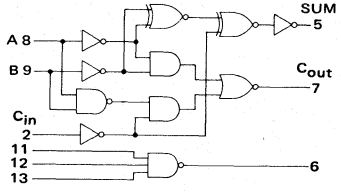
CIRCUIT SCHEMATIC



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for inputs A and C_{in}. Other inputs are tested in the same manner. Output tests should be completed according to the truth table.

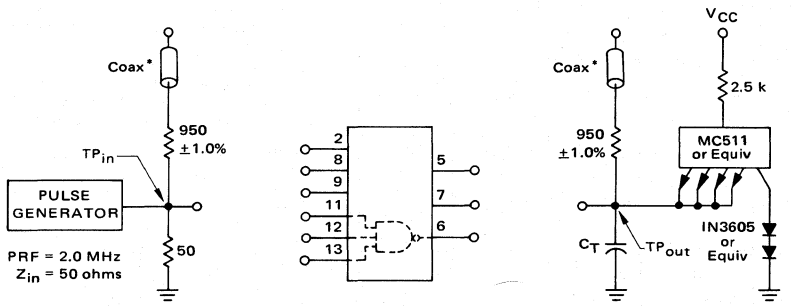


	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	$2I_{in}$	Volts V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{max}	V_{CC}
MC4326*, MC4327	−55°C	20	10	-2.2	-1.2	-	-	0.45	2.8	4.5	2.0	0.9	5.5	-	5.0
	+25°C	20	10	-2.2	-1.2	1.0	2.0	0.45	2.8	4.5	1.7	1.0	5.5	8.0	5.0
	+125°C	20	10	-2.2	-1.2	-	-	0.45	2.8	4.5	1.4	0.8	5.5	-	5.0
MC4026*, MC4027	0°C	20	10	-2.2	-1.2	-	-	0.45	3.0	4.5	1.9	1.0	5.5	-	5.0
	+25°C	20	10	-2.2	-1.2	1.0	2.0	0.45	3.0	4.5	1.8	1.0	5.5	7.0	5.0
	+75°C	20	10	-2.2	-1.2	-	-	0.45	3.0	4.5	1.7	1.0	5.5	-	5.0

Characteristic	Symbol	Pin Under Test	MC4326, MC4327 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4026, MC4027 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{max}	V_{CC}	Gnd
Input																												
Forward Current	I_F	2	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	8,9,11,12,13	-	-	-	-	4	2,10
		8	-	-2.66	-	-2.66	-	-2.66	-	-3.32	-	-3.32	-	-3.32	mAdc	-	-	-	-	-	-	2,9,11,12,13	-	-	-	-	4	8,10
Leakage Current	I_R	2	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	2	-	-	-	-	4	8,9,10,11,12,13
		8	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	-	8	-	-	-	-	4	2,9,10,11,12,13
Inverse Beta Current	I_L	2	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	2	-	-	-	-	4	10
		8	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	-	8	-	-	-	-	4	10
Breakdown Voltage	BV_{in}	2	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	-	-	-	4	8,9,10,11,12,13
		2	-	-	↓	-	-	-	-	-	↓	-	-	-		-	-	2	-	-	-	-	-	-	-	-	4	10
		8	-	-		-	-	-	-	-		-	-	-		-	-	-	8	-	-	-	-	-	-	-	4	2,9,10,11,12,13
		8	-	-		-	-	-	-	-		-	-	-	↓	-	-	-	8	-	-	-	-	-	-	-	4	10
Output																												
Output Voltage	V_{out} "0"	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	5	-	-	-	-	-	-	-	2,8,9	-	-	4	10
	V_{out} "1"	5	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	5	-	-	-	-	-	2	8,9	-	-	4	10
Leakage Current	I_{OLK}	5	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	2,8,9	-	-	-	5	-	4	10
Short-Circuit Current	I_{SC}	5	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	2,8,9	-	-	-	-	-	4	5,10
Output Voltage	V_{OL}	5	-	0.4	-	0.4	-	0.45	-	0.4	-	0.4	-	0.45	Vdc	5	-	-	-	2,8,9	-	-	-	-	-	-	4	10
	V_{OH}	5	2.8	-	3.1	-	3.15	-	3.0	-	3.1	-	3.15	-	Vdc	-	5	-	-	-	2,8,9	-	-	-	-	-	4	10
Power Requirements (Total Device)																												
Maximum Power Supply Current	I_{max}	4	-	-	-	38	-	-	-	-	-	47	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	2,8,9,10,11,12,13
Power Supply Drain	I_{PDH}	4	-	27	-	27	-	27	-	35	-	35	-	35	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	10
	I_{PDL}	4	-	32	-	32	-	32	-	41	-	41	-	41	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	2,8,9,10,11,12,13

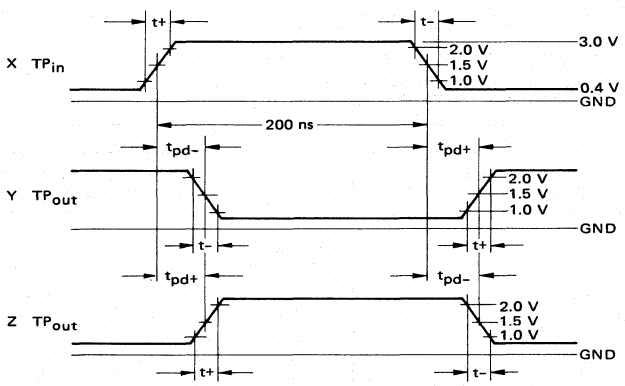
*Prime Fan-Out

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	PINS UNDER TEST (In/Out)	INPUT PIN					OUTPUT PIN			LIMITS
		8 A	9 B	11	12	13	5 SUM	6	7 C_{out}	ns max
t_{pd+}	9/5	Open	X	Open	Open	Open	Z	–	–	35
t_{pd-}	9/5	Open	X	Open	Open	Open	Z	–	–	35
t_{pd+}	11/6	Open	Open	X	3.0 V	3.0 V	–	Y	–	20
t_{pd-}	11/6	Open	Open	X	3.0 V	3.0 V	–	Y	–	20
t_{pd+}	8, 9/7	X	X	Open	Open	Open	–	–	Z	20
t_{pd-}	8, 9/7	X	X	Open	Open	Open	–	–	Z	20
t+	Tested during each of the above tests.									8.0
t-										5.0

MC4328F,L thru MC4331F,L*
MC4028F,L,P thru MC4031F,L,P*

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CONDENSED TRUTH TABLE FOR THE Nth STAGE

Pin Numbers									
8	9	11	12,13	13, 14, 1	5	6	7		
A_n	B_n	$C_{in1(n-1)}$	Note 1	Note 2	Sum	$\oplus_{out}$	MC4330/4030 MC4331/4031 C_{out}	MC4328/4028 MC4329/4029 C_{out}	Comment Note 3
0	0	0	0	0	0	0	0	0	—
0	0	0	0	1	1	0	0	0	—
0	0	0	1	0	1	0	0	0	—
0	0	0	1	1	1	0	0	0	ϕ
0	0	1	0	0	1	0	0	0	—
0	0	1	0	1	1	0	0	0	ϕ
0	0	1	1	0	1	0	0	0	ϕ
0	0	1	1	1	1	0	0	0	ϕ
0	1	0	0	0	1	1	0	0	—
0	1	0	0	1	0	1	0	1	—
0	1	0	1	0	0	1	0	1	—
0	1	0	1	1	0	1	0	1	ϕ
0	1	1	0	0	0	1	0	1	—
0	1	1	0	1	0	1	0	1	ϕ
0	1	1	1	0	0	1	0	1	ϕ
0	1	1	1	1	0	1	0	1	ϕ
1	0	0	0	0	1	1	0	0	—
1	0	0	0	1	0	1	0	1	—
1	0	0	1	0	0	1	0	1	—
1	0	0	1	1	0	1	0	1	ϕ
1	0	1	0	0	0	1	0	1	—
1	0	1	0	1	0	1	0	1	ϕ
1	0	1	1	0	0	1	0	1	ϕ
1	0	1	1	1	0	1	0	1	ϕ
1	1	0	0	0	0	0	1	1	—
1	1	0	0	1	1	0	1	1	—
1	1	0	1	0	1	0	1	1	—
1	1	0	1	1	1	0	1	1	ϕ
1	1	1	0	0	1	0	1	1	—
1	1	1	0	1	1	0	1	1	ϕ
1	1	1	1	0	1	0	1	1	ϕ
1	1	1	1	1	1	0	1	1	ϕ

Note 1. This column represents the AND function whose inputs are pins 13 and 12, and is defined by the expression $(A_{n-1} \oplus B_{n-1})(C_{in\,[n-2]})$.

Note 2. This column represents the AND function whose inputs are pins 13, 14, and 1, and is defined by the expression $(A_{n-1} \oplus B_{n-1})(A_{n-2} \oplus B_{n-2})(C_{n-3})$.

Note 3. ϕ = Don't Care. The "Don't Care" occurs for the MC4330-31/4030-31 only, because the C_n and the $\oplus_n$ from any one previous stage entering a given subsequent stage cannot be simultaneously at logic "1"

This family of fast adders is designed for use in parallel look-ahead carry adder applications where high-speed addition is required. The dependent-carry fast adders have a Carry output that is dependent upon the two input bits for that stage plus the Carry input from all previous stages. The Carry output from the MC4330/31 is independent of the carry from the previous stages.

Input Loading Factor:
$\oplus_{in1}$, A, B = 2
$\oplus_{in2}$, C_{in1}, C_{in2}, C_{in3} = 1

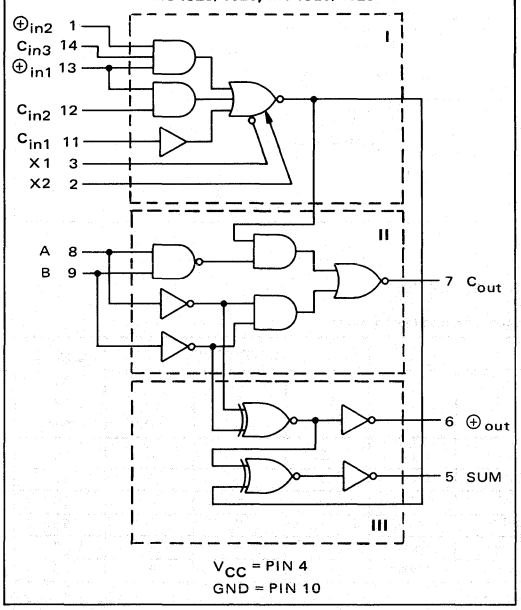
Output Loading Factor:
MC4328, MC4330 = 15 MTTL I Loads
MC4329, MC4331 = 7 MTTL I Loads
MC4028, MC4030 = 12 MTTL I Loads
MC4029, MC4031 = 6 MTTL I Loads

Total Power Dissipation = 125 mW typ/pkg

Add Delay = 25 ns typ

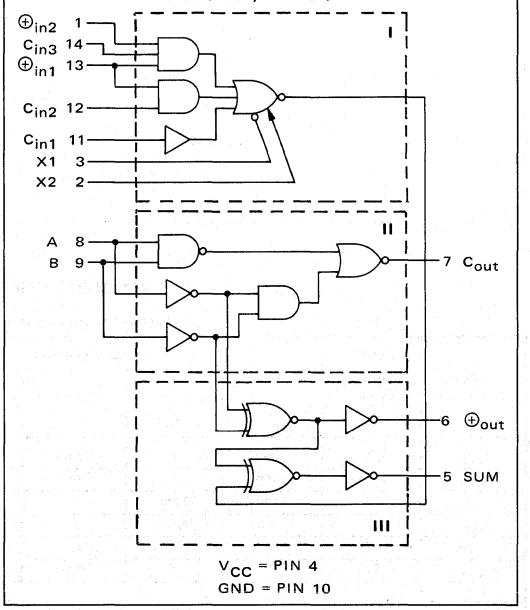
Carry Delay = 13 ns typ

DEPENDENT-CARRY FAST ADDER
MC4328/4028, MC4329/4029



V_{CC} = PIN 4
GND = PIN 10

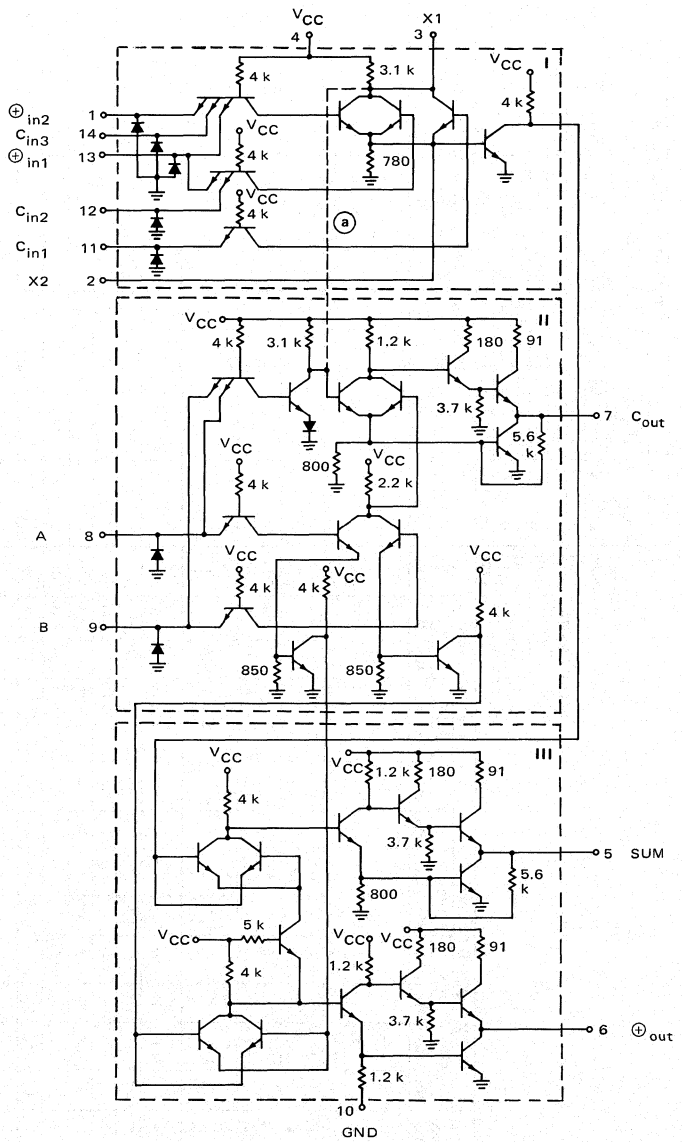
INDEPENDENT-CARRY FAST ADDER
MC4330/4030, MC4331/4031



V_{CC} = PIN 4
GND = PIN 10

*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

CIRCUIT SCHEMATIC



(a) Connection shown by dashed line used only on dependent-carry devices.

ELECTRICAL CHARACTERISTICS

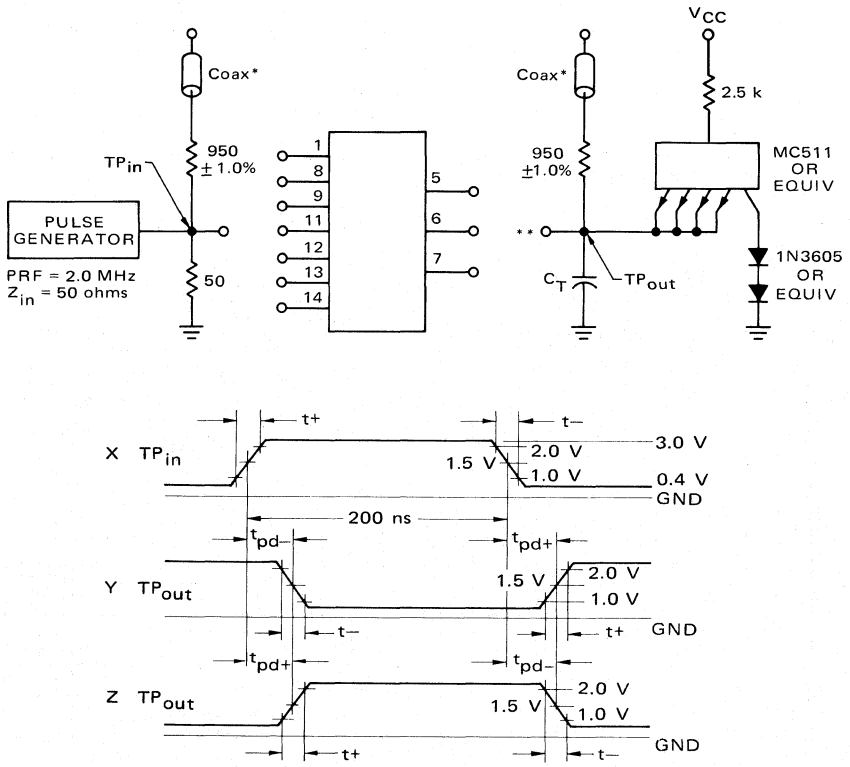
Input test procedures are shown for only inputs ⊕ $_{in2}$ and A. Other inputs are tested in the same manner. Output tests should be completed according to the truth table.

@ Test Temperature	I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	V_{th1} Volts	V_{th0} Volts	V_{out} Volts	V_{max} Volts	V_{CC} Volts
MC4328*, MC4329, MC4330*, MC4331 −55°C	20	10	-2.2	-1.2	-	0.45	2.8	4.5	2.0	0.9	5.5	-	5.0
MC4328*, MC4329, MC4330*, MC4331 +25°C	20	10	-2.2	-1.2	1.0	0.45	2.8	4.5	1.7	1.0	5.5	8.0	5.0
MC4328*, MC4329, MC4330*, MC4331 +125°C	20	10	-2.2	-1.2	-	0.45	2.8	4.5	1.4	0.8	5.5	-	5.0
MC4028*, MC4029, MC4030*, MC4031 0°C	20	10	-2.2	-1.2	-	0.45	3.0	4.5	1.9	1.0	5.5	-	5.0
MC4028*, MC4029, MC4030*, MC4031 +25°C	20	10	-2.2	-1.2	1.0	0.45	3.0	4.5	1.8	1.0	5.5	7.0	5.0
MC4028*, MC4029, MC4030*, MC4031 +75°C	20	10	-2.2	-1.2	-	0.45	3.0	4.5	1.7	1.0	5.5	-	5.0

Characteristic	Symbol	Pin Under Test	MC4328 thru MC4331 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4028 thru MC4031 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{max}	V_{CC}	Gnd
Input																											
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	8,9,11,12,13,14	-	-	-	-	4	1,10
		8	-	-2.66	-	-2.66	-	-2.66	-	-3.32	-	-3.32	-	-3.32	mAdc	-	-	-	-	-	1,9,11,12,13,14	-	-	-	-	4	8,10
Leakage Current	I_R	1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	1	-	-	-	-	4	8,9,10,11,12,13,14
		8	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	8	-	-	-	-	4	1,9,10,11,12,13,14
Inverse Beta Current	I_L	1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	1	-	-	-	-	4	10
		8	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	8	-	-	-	-	4	10
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	4	8,9,10,11,12,13,14
		1	-	-	↓	-	-	-	-	-	↓	-	-	-	↓	-	-	1	-	-	-	-	-	-	-	4	10,12,14
		8	-	-		-	-	-	-	-		-	-	-		-	-	8	-	-	-	-	-	-	-	4	1,9,10,11,12,13,14
		8	-	-		-	-	-	-	-		-	-	-		-	-	8	-	-	-	-	-	-	-	4	10,12,14
Output																											
Output Voltage	V_{out} "0"	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	5	-	-	-	-	-	8,9	11,13	-	-	4	10
	V_{out} "1"	7	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	7	-	-	-	-	8,9	11,13	-	-	4	10
Leakage Current	I_{OLK}	6	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	-	-	6	-	4	8,10
Short-Circuit Current	I_{SC}	5**	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	-	4	5,10
Output Voltage	V_{OL}	5	-	0.4	-	0.4	-	0.45	-	0.4	-	0.4	-	0.45	Vdc	5	-	-	11,13	8,9	-	-	-	-	-	4	10
	V_{OH}	7	2.7	-	3.1	-	3.15	-	2.8	-	3.1	-	3.15	-	Vdc	-	7	-	11,13	8,9	-	-	-	-	-	4	10
Power Requirements (Total Device)																											
Maximum Power Supply Current	I_{max}	4	-	-	-	55	-	-	-	-	-	65	-	-	mAdc	-	-	-	-	-	-	-	-	-	4	-	8, 9, 10, 11, 13
Power Supply Drain	I_{PDH}	4	-	32	-	32	-	32	-	41	-	41	-	41	mAdc	-	-	-	-	-	-	-	-	-	-	4	10
	I_{PDL}	4	-	38	-	38	-	38	-	48	-	48	-	48	mAdc	-	-	-	-	-	-	-	-	-	-	4	8, 9, 10, 11, 13

*Prime Fan-Out
**Short one output at a time.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

**Load only pin 5 when testing output 5. Load both outputs 6 and 7 when testing pin 6 or 7.

SWITCHING TIME TEST PROCEDURES
(Letters shown in test columns refer to waveforms.)

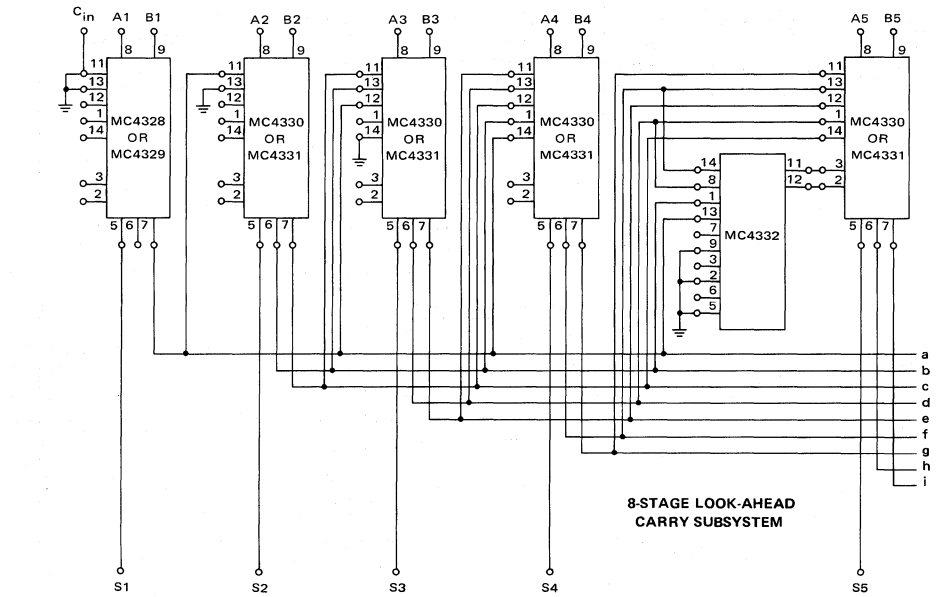
TEST	PINS UNDER TEST (In/Out)	INPUT PIN							OUTPUT PIN			LIMITS ns max
		8 A	9 B	11 C_{in1}	12 C_{in2}	13 $\oplus_{in1}$	14 C_{in3}	1 $\oplus_{in2}$	5 SUM	6 $\oplus_{out}$	7 C_{out}	
t_{pd+}	11/5	Open	Gnd	X	Open	Gnd	Open	Open	Y	–	–	35
t_{pd-}	11/5	Open	Gnd	X	Open	Gnd	Open	Open	Y	–	–	35
t_{pd+}	8/6	X	3.0 V	Gnd	Gnd	Open	Gnd	Open	–	Y	–	30
t_{pd-}	8/6	X	3.0 V	Gnd	Gnd	Open	Gnd	Open	–	Y	–	30
t_{pd+}	8/7	X	3.0 V	Gnd	Gnd	Open	Gnd	Open	–	–	Z	20
t_{pd-}	8/7	X	3.0 V	Gnd	Gnd	Open	Gnd	Open	–	–	Z	20
t+	Tested during each of the above tests.											8.0
t–												5.0

TYPICAL APPLICATION

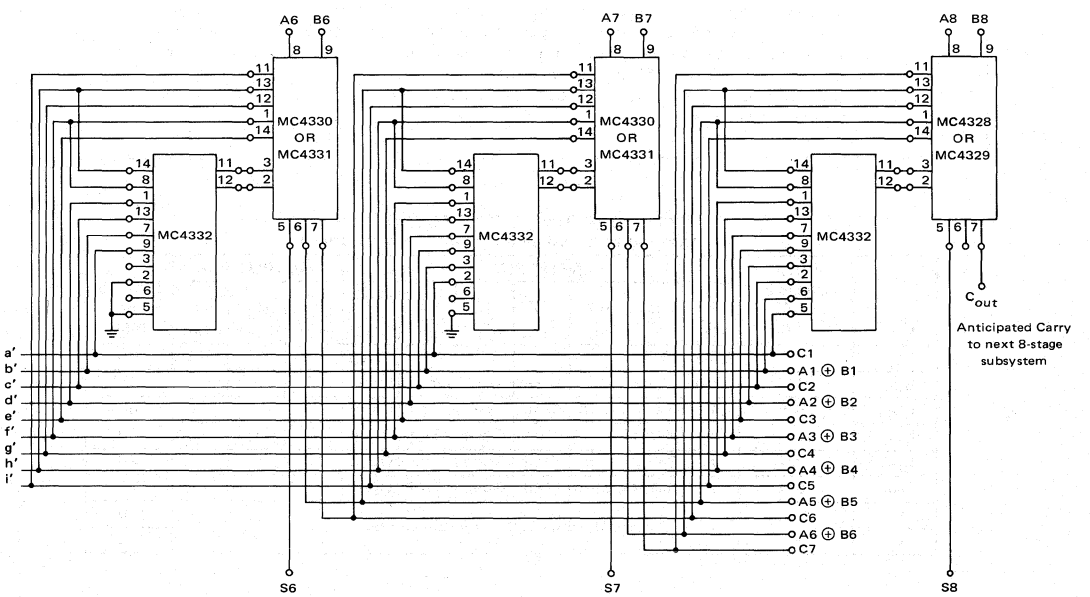
The MC4328/29 and MC4330/31 adders can be used with the MC4332 Carry Decoder to build 8-stage look-ahead carry subsystems. Each stage examines the carry outputs from all previous stages while adding bits A and B for that stage. The carry outputs of the first and eighth stages are dependent upon the carry inputs from previous stages; thus the MC4328/29 adder is used for stages one and eight while the MC4330/31 adder is used for stages two through seven. The MC4332 Carry Decoder is used to expand the look-ahead carry input capability required for stages four through eight.

The add delay of an eight stage adder is equal to the sum of the add delay and the delay from the A and B inputs to the ⊕output of one stage. Thus the typical add delay for an 8-stage adder is 25 ns + 13 ns or 38 ns typical.

When expander inputs are not used they should not be connected to any external point. This minimizes possible problems resulting from noise pick-up.



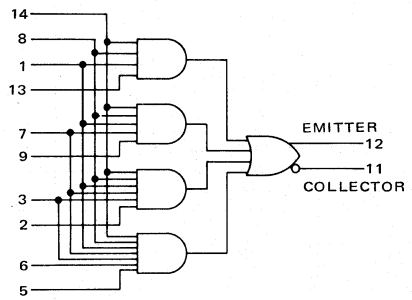
8-STAGE LOOK-AHEAD CARRY SUBSYSTEM



CARRY DECODER

MC4332F,L*
MC4032F,L,P*

This 4-wide 4, 5, 6, 7 input AND-OR expander provides the necessary logic for carry decoding between look-ahead carry adder stages using the MC4328/29 and MC4330/31 fast adders.

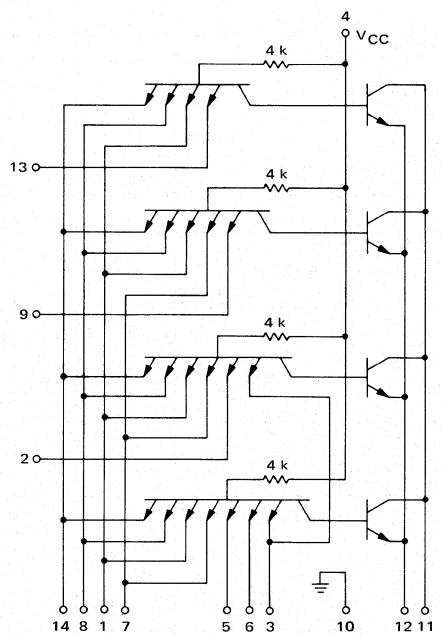


V_{CC} = Pin 4
GND = Pin 10

Input Loading Factor:
Pins 1, 8, 14 = 4
Pin 7 = 3
Pin 3 = 2
Pins 2, 5, 6, 9, 13 = 1

Total Power Dissipation = 20 mW typ/pkg

Δt_{pd} = 4.0 ns typ/decoder
1.0 ns typ/pF at expander nodes



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

TYPICAL APPLICATION

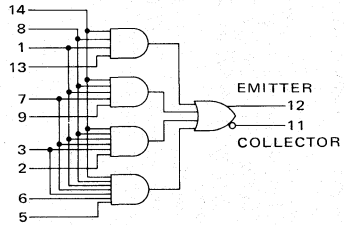
The MC4328/29 and MC4330/31 adders can be used with the MC4332 Carry Decoder to build 8-stage look-ahead carry subsystems. (See the MC4328-31) data sheet for a diagram.) Each stage examines the carry outputs from all previous stages while adding bits A and B for that stage. The carry outputs of the first and eighth stages are dependent upon the carry inputs from previous stages; thus the MC4328/29 adder is used for stages one and eight while the MC4330/31 adder is used for stages two through seven. The MC4332 Carry Decoder is used to expand the look-ahead carry input capability required for stages four through eight.

The add delay of an eight stage adder is equal to the sum of the add delay and the delay from the A and B inputs to the ⊕ output of one stage. Thus the typical add delay for an 8-stage adder is 25 ns +13 ns or 38 ns typical.

When expander inputs are not used they should not be connected to any external point. This minimizes possible problems resulting from noise pick-up.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one set of inputs. Test remaining inputs in the same manner.



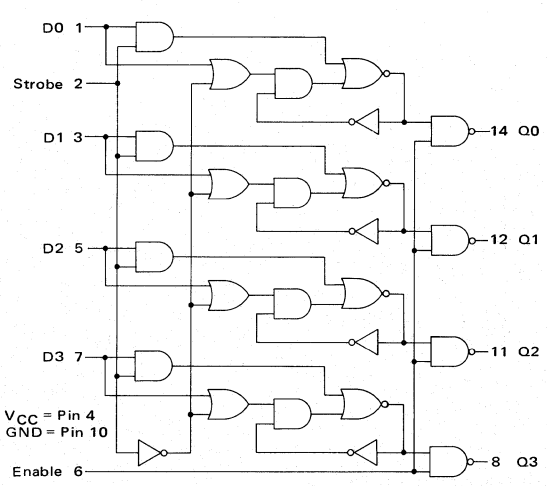
	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{in}	$2\ I_{in}$	$3\ I_{in}$	$4\ I_{in}$	Volts V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	$V_{out\,1}$	$V_{out\,2}$	$V_{E\,1}$	$V_{E\,2}$	$V_{E\,3}$	V_{max}	V_{CC}
MC4332	−55°C	2.5	1.0	2.0	3.0	4.0	0	4.5	2.0	0.9	4.8	5.5	1.0	0.9	-	-	5.0
MC4332	+25°C	2.5	1.0	2.0	3.0	4.0	0	4.5	1.7	1.0	4.8	5.5	0.85	0.75	0.8	7.0	5.0
MC4332	+125°C	2.5	1.0	2.0	3.0	4.0	0	4.5	1.4	0.8	4.8	5.5	0.65	0.55	-	-	5.0
MC4032	0°C	2.5	1.0	2.0	3.0	4.0	0	4.5	1.9	1.0	4.8	5.5	0.9	0.8	-	-	5.0
MC4032	+25°C	2.5	1.0	2.0	3.0	4.0	0	4.5	1.8	1.0	4.8	5.5	0.85	0.75	0.8	7.0	5.0
MC4032	+75°C	2.5	1.0	2.0	3.0	4.0	0	4.5	1.7	1.0	4.8	5.5	0.75	0.65	-	-	5.0

Characteristic	Symbol	Pin Under Test	MC4332 Test Limits −55°C Min	−55°C Max	+25° Min	+25° Max	+125°C Min	+125°C Max	MC4032 Test Limits 0°C Min	0°C Max	+25° Min	+25° Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	$2\ I_{in}$	$3\ I_{in}$	$4\ I_{in}$	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	$V_{out\,1}$	$V_{out\,2}$	$V_{E\,1}$	$V_{E\,2}$	$V_{E\,3}$	V_{max}	V_{CC}	Gnd
Input																															
Forward Current	I_F	1	-	-5.32	-	-5.32	-	-5.32	-	-6.64	-	-6.64	-	-6.64	mAdc	-	-	-	-	-	1	2,3,5,6,7,8,9,13,14	-	-	-	-	-	-	-	-	4	10
		2	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	↓	-	-	-	-	-	2	1,3,5,6,7,8,9,13,14	-	-	-	-	-	-	-	-	↓	↓
		3	-	-2.66	-	-2.66	-	-2.66	-	-3.32	-	-3.32	-	-3.32		-	-	-	-	-	3	1,2,5,6,7,8,9,13,14	-	-	-	-	-	-	-	-		
		7	-	-3.99	-	-3.99	-	-3.99	-	-4.98	-	-4.98	-	-4.98		-	-	-	-	-	7	1,2,3,5,6,8,9,13,14	-	-	-	-	-	-	-	-		
Leakage Current	I_R	1	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	mAdc	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	4	2,3,5,6,7,8,9,10,13,14
		2	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1		-	-	-	-	-	-	2	-	-	-	-	-	-	-	-		1,3,5,6,7,8,9,10,13,14
		3	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2		-	-	-	-	-	-	3	-	-	-	-	-	-	-	-		1,2,5,6,7,8,9,10,13,14
		7	-	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	0.3	↓	-	-	-	-	-	-	7	-	-	-	-	-	-	-	-	↓	1,2,3,5,6,8,9,10,13,14
Inverse Beta Current	I_L	1	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	mAdc	-	-	-	-	-	-	1	-	-	-	-	12	-	-	-	4	10
		2	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1		-	-	-	-	-	-	2	-	-	-	-		-	-	-		
		3	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2		-	-	-	-	-	-	3	-	-	-	-		-	-	-		
		7	-	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	0.3	↓	-	-	-	-	-	-	7	-	-	-	-	↓	-	-	-	↓	↓
Breakdown Voltage	BV_{in}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	4	2,3,5,6,7,8,9,10,13,14
		2		-		-		-		-		-		-		-	2	-	-	-	-	-	-	-	-	-	-	-	-	-	1,3,5,6,7,8,9,10,13,14
		3		-		-		-		-		-		-		-	-	3	-	-	-	-	-	-	-	-	-	-	-	-	1,2,5,6,7,8,9,10,13,14
		7		-		-		-		-		-		-		-	-	-	7	-	-	-	-	-	-	-	-	-	-	-	1,2,3,5,6,8,9,10,13,14
		1		-		-		-		-		-		-		-	-	-	-	1	-	-	-	-	-	12	-	-	-	10
		2		-		-		-		-		-		-		-	2	-	-	-	-	-	-	-	-	-	-	-	-		
		3		-		-		-		-		-		-		-	-	3	-	-	-	-	-	-	-	-	-	-	-		
		7		-		-		-		-		-		-	↓	-	-	-	7	-	-	-	-	-	-	-	↓	-	-	-	↓	↓
Output																															
Output Voltage	V_{out} "0"	11/12*	-	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	0.3	Vdc	11	-	-	-	-	-	-	1	-	-	-	12	-	-	-	4	2,3,5,6,7,9,10
Leakage Current	I_{OLK}	11	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	-	-	-	-	11		12	-	-	4	1,10
	I_{CEX}	11	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	-	-	1	11	-		12	-	-	4	10
Power Requirements																															
Maximum Power Supply Current	I_{max}	4	-	-	-	8.7	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	12	4	-	1,2,3,5,6,7,8,9,10,13,14
Power Supply Drain	I_{PDH}	4	-	5.0	-	5.0	-	5.0	-	6.0	-	6.0	-	6.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	12	-	-	-	4	, 10
	I_{PDL}	4	-	6.0	-	6.0	-	6.0	-	7.0	-	7.0	-	7.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,13,14

*Voltage measured between pins 11 and 12.

QUAD LATCH
(Open Collector)

MC4335F, L*
MC4035F, L, P*



Two 5.0 k ohm pullup resistors are internally connected to V_{CC} and brought out on pins 9 and 13.

This monolithic device consists of four latch circuits with open collector outputs, common Strobe input, and output enable input. The output of each latch will follow the data input when the Strobe input is in a logical "1" state. When the Strobe is in a logical "0" state, the latch will store the logic state of the data input just prior to the change of the Strobe from a "1" level to a "0" level.

The open collector outputs make this device useful for bussing or wire ORing outputs together. Two 5.0 k ohm resistors are available in the package to provide the passive pullup function in wired-OR or bussed operation. The output enable is useful where it is desirable to gate information out of the latches according to a predetermined timing scheme.

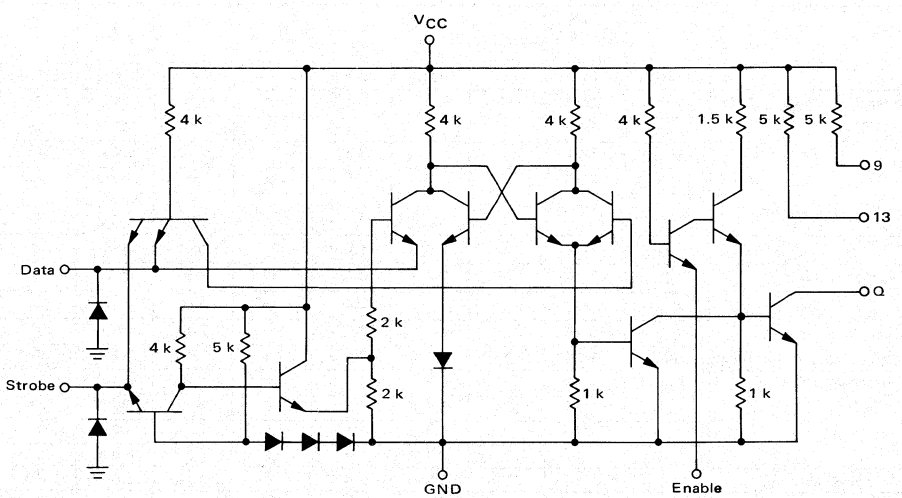
Input Loading Factor (MTTL I Loads):
- Data Input (Strobe High) — MC4335 = 4.2, MC4035 = 4.0
- Data Input (Strobe Low) — MC4335 = 1.1, MC4035 = 0.9
- Output Enable — MC4335 = 4.0, MC4035 = 3.6
- Strobe — MC4335 = 5.2, MC4035 = 5.2

Output Loading Factor (MTTL I Loads):
- MC4335 = 7 (I_{OL} = 9.3 mAdc)
- MC4035 = 7 (I_{OL} = 11.6 mAdc)

Total Power Dissipation = 140 mW typ/pkg
Propagation Delay Time = 25 ns typ

CIRCUIT SCHEMATIC

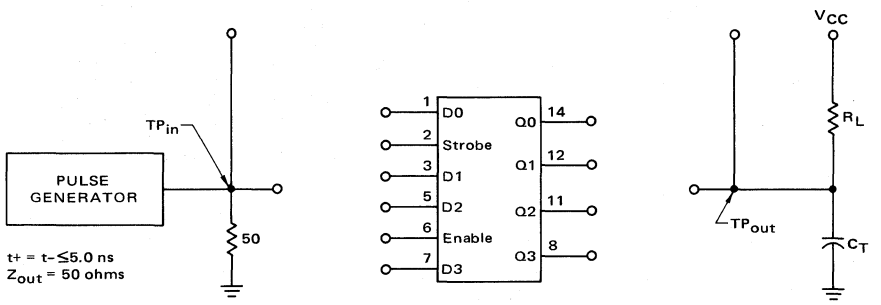
1/4 OF DEVICE SHOWN



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

11

SWITCHING TIME TEST CIRCUIT



R_L value given in Switching Time Test Procedures table.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 Megohm) must be used.

SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

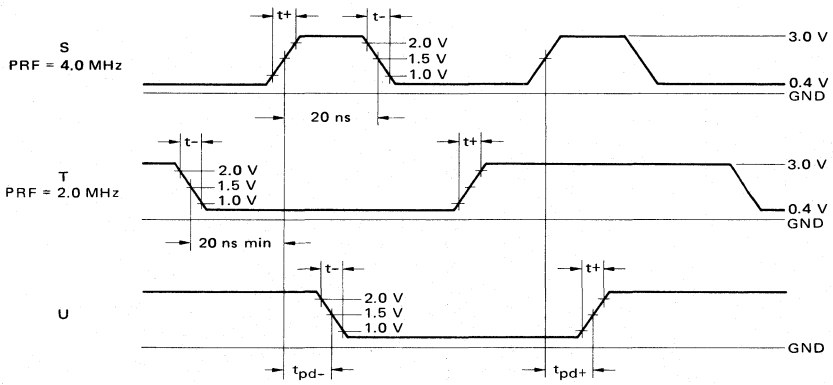
(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	PIN UNDER TEST (In/Out)	INPUT Pin 1 D0	INPUT Pin 2 Strobe	INPUT Pin 6 Enable	OUTPUT Pin 14 D0	R_L Ohms MC4335	R_L Ohms MC4035	LIMITS (ns) Max MC4335	LIMITS (ns) Max MC4035
Strobe Propagation Delay	t_{pd+1}	2/14	T	S	2.4 V	U	510	390	25	25
	t_{pd-1}	2/14	T	S	2.4 V	U	510	390	40	35
	t_{pd+2}	2/14	T	S	2.4 V	U	5.0 k	5.0 k	50	50
	t_{pd-2}	2/14	T	S	2.4 V	U	5.0 k	5.0 k	34	34
Rise Time	t+	14	T	S	2.4 V	U	510 or 5.0 k	390 or 5.0 k	0.3 RC	0.3 RC
Fall Time	t-	14	T	S	2.4 V	U	510	390	9.0	5.0
Data Propagation Delay	t_{pd+3}	1/14	V	2.4 V	2.4 V	W	510	390	20	20
	t_{pd-3}	1/14	V	2.4 V	2.4 V	W	510	390	30	25
	t_{pd+4}	1/14	V	2.4 V	2.4 V	W	5.0 k	5.0 k	50	50
	t_{pd-4}	1/14	V	2.4 V	2.4 V	W	5.0 k	5.0 k	25	25
Enable Propagation Delay	t_{pd+3}	1/14	X	2.4 V	Y	Z	510	390	20	20
	t_{pd-3}	1/14	X	2.4 V	Y	Z	510	390	30	25
	t_{pd+4}	1/14	X	2.4 V	Y	Z	5.0 k	5.0 k	50	50
	t_{pd-4}	1/14	X	2.4 V	Y	Z	5.0 k	5.0 k	25	25
Minimum Strobe Enable	–	1/14	T ①	1.8 V	2.4 V	②	5.0 k	5.0 k	②	②
Maximum Strobe Inhibit	–	1/14	T ①	1.0 V	2.4 V	③	5.0 k	5.0 k	③	③

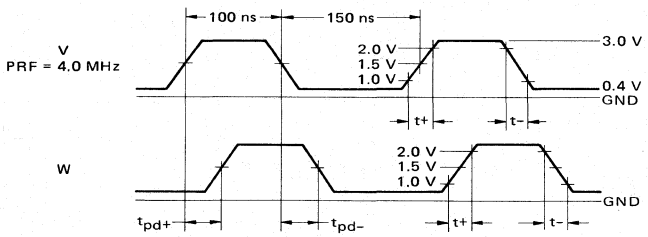
① Pulse T conditions changed: V_L = 1.0 V, V_H = 1.8 V
② Output shall follow data input.
③ Output shall not toggle.

VOLTAGE WAVEFORMS

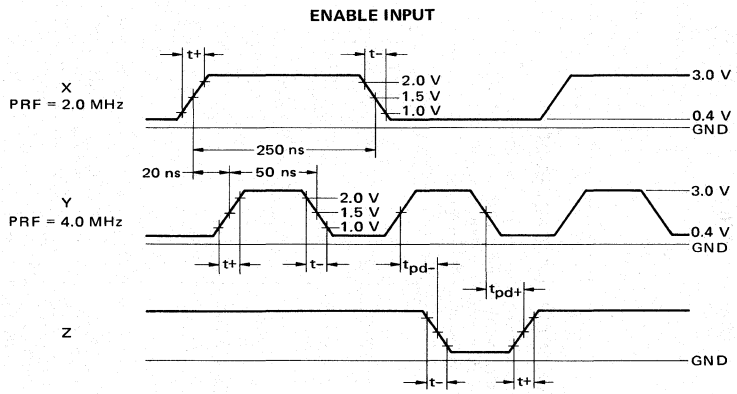
STROBE INPUT



DATA INPUTS

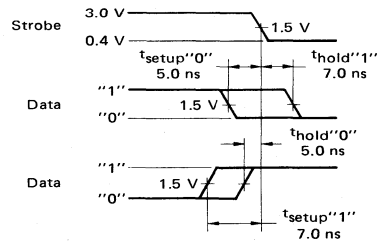


ENABLE INPUT



OPERATING CHARACTERISTICS

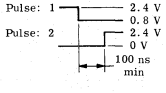
This quad latch consists of four gated latches that store data on the negative edge of the strobe input. Information must be present at the data inputs prior to the setup time and remain at the data inputs through the hold time to insure that it will be stored by the latch when the negative edge of the strobe occurs. The setup time is 7.0 ns for a logical "1" and 5.0 ns for a logical "0". Hold time is 7.0 ns after the strobe edge for a logical "1" and 5.0 ns prior to the strobe edge for a logical "0".



ELECTRICAL CHARACTERISTICS

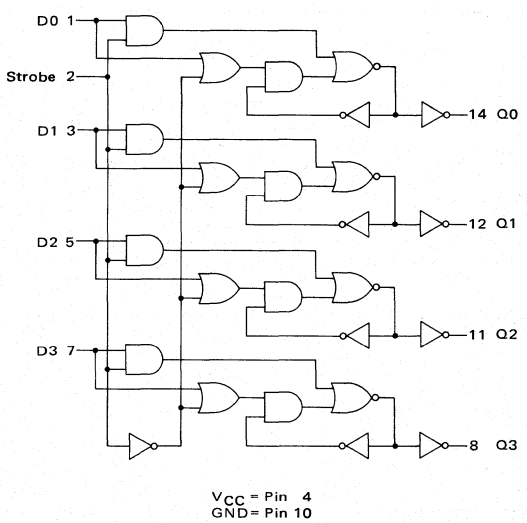
Test procedures are shown for the Strobe, Enable, and only one data input, and for one output. Other data inputs and outputs are tested in the same manner.

																TEST CURRENT/VOLTAGE VALUES (All Temperatures)																		
																mA			Volts													
																I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}						
															MC4335	11.6	0.1	1.0	0.8	2.0	0.4	4.5	5.5	7.0	5.0	4.5	5.5						
															MC4035	9.3	0.1	1.0	0.8	2.0	0.4	4.5	5.5	7.0	5.0	4.75	5.25						
			MC4335 Test Limits						MC4035 Test Limits							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																		
		Pin	−55°C		+25°C		+125°C		0°C		+25°C		+75°C																Pulse	Pulse	
Characteristic	Symbol	Under Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	1	2	Gnd
Input																																
Forward Current	I_F	1	-	-5.6	-	-5.6	-	-5.6	-	-6.7	-	-6.7	-	-6.7	mAdc	-	-	-	-	-	1	2	-	-	-	-	4	-	-	10
		1	-	-1.5	-	-1.5	-	-1.5	-	-1.8	-	-1.8	-	-1.8	↓	-	-	-	2	-	1	3,5,7	-	-	-	-	↓	-	-	↓
		2	-	-7.0	-	-7.0	-	-7.0	-	-8.6	-	-8.6	-	-8.6		-	-	-	-	-	2	1,3,5,6,7	-	-	-	-		-	-	
		6	-	-5.3	-	-5.3	-	-5.3	-	-6.0	-	-6.0	-	-6.0		-	-	-	-	-	6	1,2,3,5,7	-	-	-	-		-	-	
		13	-	-1.3	-	-1.3	-	-1.3	-	-1.6	-	-1.6	-	-1.6		-	-	-	-	-	13	1	-	-	-	-		-	-	
Leakage Current	I_R	1	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	-	1	-	-	-	-	4	-	-	2,10
		2	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	↓	-	-	-	-	-	-	2	-	-	-	-	↓	-	-	1,3,5,7,10
		6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4		-	-	-	-	-	-	6	-	-	-	-		-	-	1,2,3,5,7,10
Breakdown Voltage	BV_{in}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	-	-	2,10
		2	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	2	-	-	-	-	-	-	-	-	↓	-	-	1,3,5,6,7,10
		6		-		-		-		-		-		-		-	-	6	-	-	-	-	-	-	-	-		-	-	1,2,3,5,7,10
Output																																
Output Voltage	V_{OL}	14	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	14	-	-	-	6	-	2,3,5,7	-	-	-	4	-	-	-	1,10
		14	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	14	-	-	1	2,6	-	-	-	-	-	↓	-	-	-	10
		14	-		-		-		-		-		-			14	-	-	-	-	-	-	-	-	-		-	2	1	10
	V_{OH}	14	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	Vdc	-	14	-	6	-	-	2	-	-	-	4	-	-	-	1,3,5,7,10
		14	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	Vdc	-	14	-	-	1,2,6	-	-	-	-	-	4	-	-	-	10
Leakage Current	I_{CEX}	14	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	1,2	14	-	-	-	4	-	-	10
		14	-	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	1.0	mAdc	-	-	-	-	-	-	-	-	14	4	-	-	-	-	6,10
Power Requirements (Total Device)																																
Maximum Power Supply Current	I_{max}	4	-	-	-	44	-	-	-	-	-	52	-	-	mAdc	-	-	-	-	-	-	2	-	4	-	-	-	-	-	1,3,5,6,7,10
Power Supply Drain	I_{PDH}	4	-	42	-	42	-	42	-	50	-	50	-	50	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	-	10
	I_{PDL}	4	-	34	-	34	-	34	-	40	-	40	-	40	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	-	1,3,5,6,7,10



QUAD LATCH

MC4337F, L*
MC4037F, L, P*

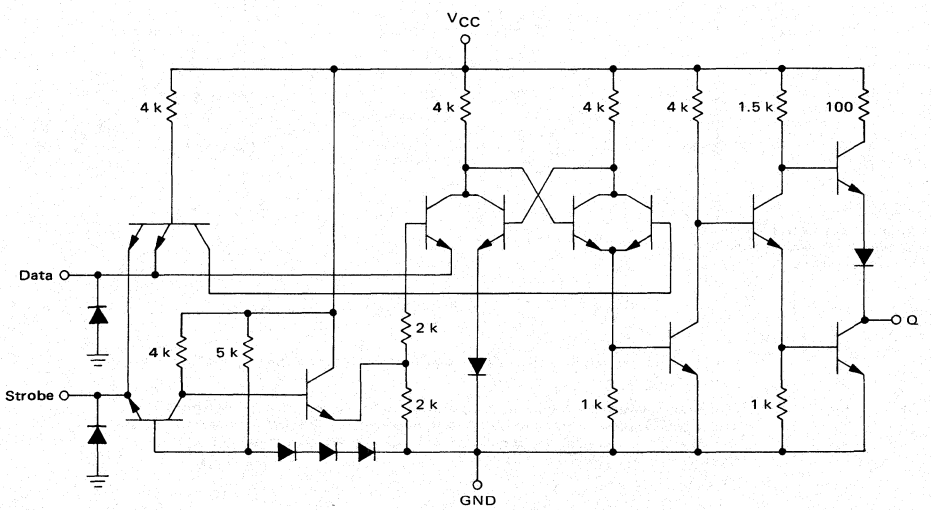


This monolithic device consists of four latch circuits with active pullup networks for high capacitive load drive capability. Separate data inputs and a common Strobe input are provided. Information present on the data inputs prior to the negative edge of the strobe input will be stored in the latch. When the strobe input is high, the Q output will follow the data input.

Input Loading Factor (MTTL I Loads):
Data Input (Strobe High) – MC4337 = 4.2
MC4037 = 4.0
Data Input (Strobe Low) – MC4337 = 1.1
MC4037 = 0.9
Strobe – MC4337 = 5.2
MC4037 = 5.2
Output Loading Factor (MTTL I Loads):
MC4337 = 10 (I_{OL} = 13.3 mAdc)
MC4037 = 10 (I_{OL} = 16.6 mAdc)
Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 25 ns typ

CIRCUIT SCHEMATIC

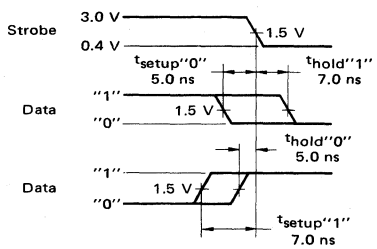
1/4 OF DEVICE SHOWN



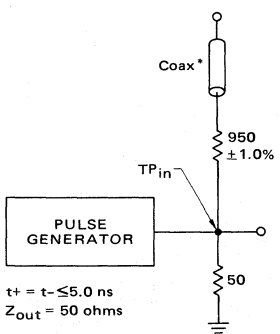
*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

OPERATING CHARACTERISTICS

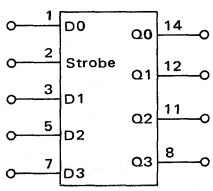
This quad latch consists of four gated latches that store data on the negative edge of the strobe input. Information must be present at the data inputs prior to the setup time and remain at the data inputs through the hold time to insure that it will be stored by the latch when the negative edge of the strobe occurs. The setup time is 7.0 ns for a logical "1" and 5.0 ns for a logical "0". Hold time is 7.0 ns after the strobe edge for a logical "1" and 5.0 ns prior to the strobe edge for a logical "0".

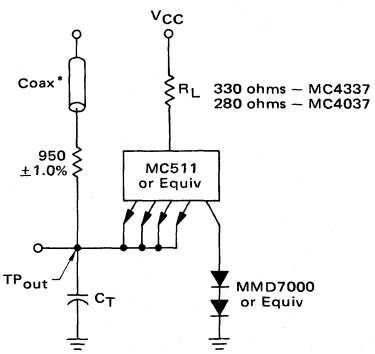


SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved to provide the waveforms shown.



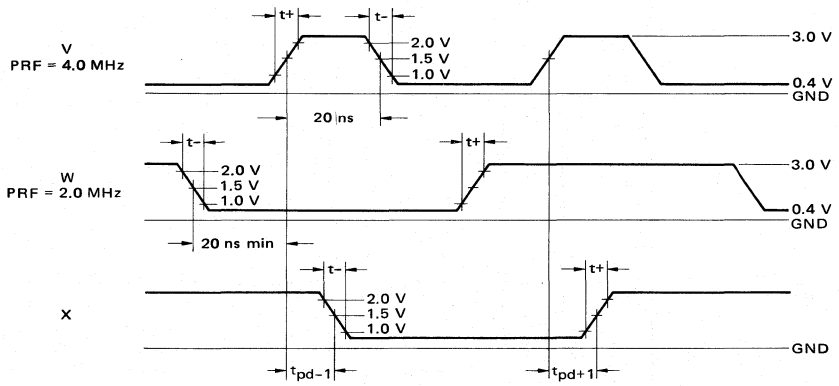


C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

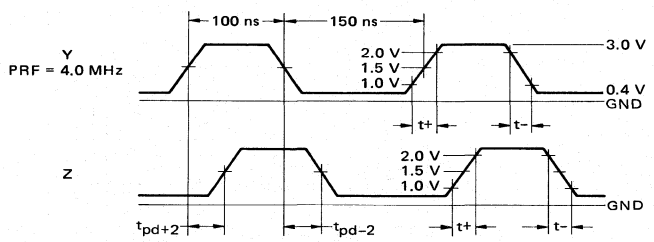
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS

STROBE INPUT



DATA INPUTS



SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

(Letters shown in test columns refer to waveforms.)

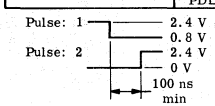
TEST	SYMBOL	PIN UNDER TEST (In/Out)	INPUT		OUTPUT	LIMITS (ns)
			Pin 1 D0	Pin 2 Strobe	Pin 14 Q0	Max
Strobe Propagation Delay	t_{pd+1}	2/14	W	V	X	25
	t_{pd-1}	2/14	W	V	X	40
Rise Time	t+	14	W	V	X	8.0
Fall Time	t-	14	W	V	X	5.0
Data Propagation Delay	t_{pd+2}	1/14	Y	2.4 V	Z	20
	t_{pd-2}	1/14	Y	2.4 V	Z	30
Minimum Strobe Enable	—	1/14	W①	1.8 V	②	②
Maximum Strobe Inhibit	—	1/14	W①	1.0 V	③	③

① Pulse W conditions changed: V_L = 1.0 V, V_H = 1.8 V.
② Output shall follow data input.
③ Output shall not toggle.

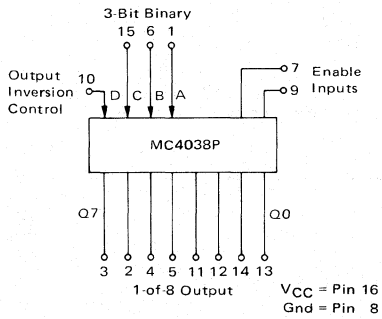
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only the Strobe input, one data input, and one output. Other data inputs and outputs are tested in the same manner.

																TEST CURRENT / VOLTAGE VALUES (All Temperatures)														
																mA			Volts											
																I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}			
																MC4337	13.3	-1.4	1.0	0.8	2.0	0.4	4.5	5.5	7.0	5.0	4.5	5.5		
																MC4037	13.3	-1.4	1.0	0.8	2.0	0.4	4.5	5.5	7.0	5.0	4.75	5.25		
			MC4337 Test Limits						MC4037 Test Limits								TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:														
		Pin	−55°C		+25°C		+125°C		0°C		+25°C		+75°C																Pulse	Pulse	
Characteristic	Symbol	Under Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	1	2	Gnd
Input																														
Forward Current	I_F	1	-	-5.6	-	-5.6	-	-5.6	-	-6.7	-	-6.7	-	-6.7	mAdc	-	-	-	-	-	1	2	-	-	-	-	4	-	-	10
		1	-	-1.5	-	-1.5	-	-1.5	-	-1.8	-	-1.8	-	-1.8	↓	-	-	-	2	-	1	3,5,7	-	-	-	-	↓	-	-	↓
		2	-	-7.0	-	-7.0	-	-7.0	-	-8.6	-	-8.6	-	-8.6		-	-	-	-	-	2	1,3,5,7	-	-	-	-		-	-	
Leakage Current	I_R	1	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mAdc	-	-	-	-	-	-	1	-	-	-	-	4	-	-	2,10
		2	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	mAdc	-	-	-	-	-	-	2	-	-	-	-	4	-	-	1,3,5,7,10
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	-	-	2,10
		2	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	-	-	-	4	-	-	1, 3, 5, 7, 10
Output																														
Output Voltage	V_{OL}	14	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	14	-	-	1	2	-	-	-	-	-	4	-	-	-	10
		14	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	14	-	-	-	-	-	-	-	-	-	4	-	2	1	10
	V_{OH}	14	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	Vdc	-	14	-	-	1,2	-	-	-	-	-	4	-	-	-	10
Short-Circuit Current	I_{SC}	14	-15	-60	-15	-60	-15	-60	-15	-60	-15	-60	-15	-60	mAdc	-	-	-	-	-	-	1	-	-	-	-	4	-	-	10,14
Leakage Current	I_{CEX}	14	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	1,2	14	-	-	-	4	-	-	10
Power Requirements (Total Device)																														
Maximum Power Supply Current	I_{max}	4	-	-	-	40	-	-	-	-	-	50	-	-	mAdc	-	-	-	-	-	-	2	-	4	-	-	-	-	-	10
Power Supply Drain	I_{PDH}	4	-	26	-	26	-	26	-	32	-	32	-	32	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	-	10
	I_{PDL}	4	-	45	-	45	-	45	-	55	-	55	-	55	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	-	1, 3, 5, 7, 10



MC4038P*



TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Total Power Dissipation = 240 mW typ/pkg

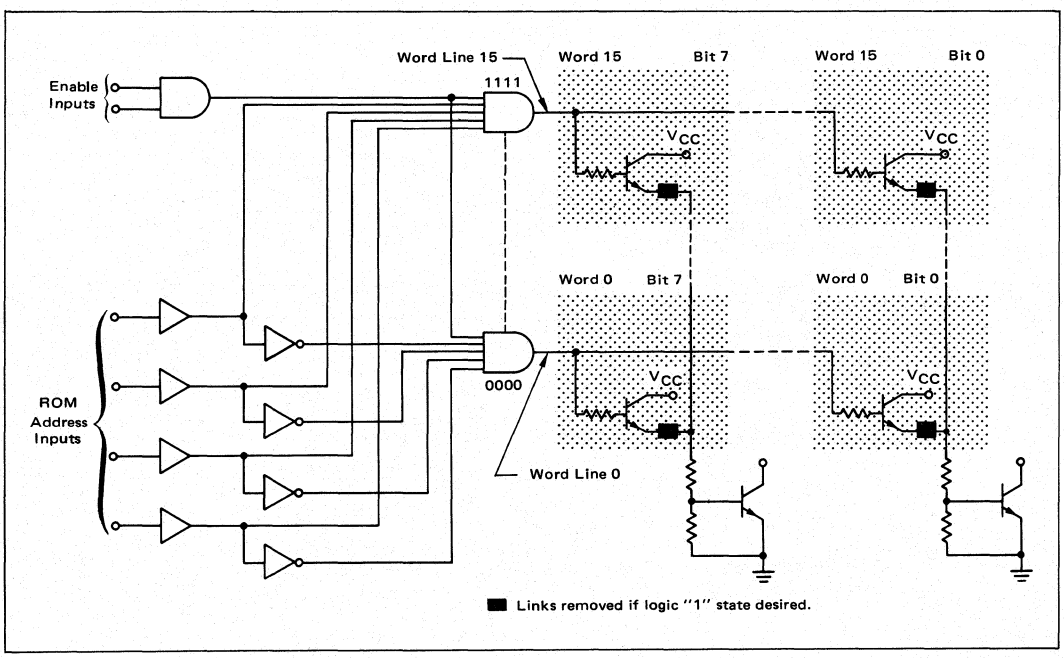
The MC4038P is derived from the XC170 128-Bit Read Only Memory. A 3-bit binary address selects the desired word for the 8-bit output. The inversion control, D, selects half of the memory chip with the bit pattern that defines a 1-of-8 decoder function. When D is a logic "0", the selected output is designated as a logic "0". A logic "1" on D produces a logic "1" on the selected output.

Features:

- Address times < 45 ns
- Outputs sink 20 mA
- Output capacitance < 7.0 pF @ 1.5 V
- Wired OR capability to 64 memories

ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							



*P suffix = 16-pin dual in-line plastic package (Case 612).

MC4038P (continued)

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	Open Collector I_{OL} = 20 mA
MC400	1.0	
MC2000	0.67	
MC3000	0.7	
MC7400	1.0	
MC830	1.15**	

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

** Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Supply Operating Voltage Range	V_{CC}	4.5 to 5.5	Vdc
Input Voltage	V_{in}	−1.5 to +5.5	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

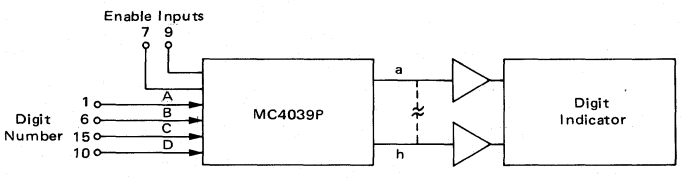
ELECTRICAL CHARACTERISTICS (T_A = 0 to +75°C)

Characteristic	Symbol	Min	Max	Unit
Address Input Forward Current (V_A = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Enable Input Forward Current (V_E = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Address Input Leakage Current (V_A = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Enable Input Leakage Current (V_E = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Logical "0" Output Voltage (I_{OL} = 20 mAdc, V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	V_{OL}	-	0.45	Vdc
Logical "1" Output Leakage Current (V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CEX} = 7.0 Vdc, V_{CC} = 5.25 Vdc)	I_{CEX}	-	100	μAdc
Power Supply Drain Current				mAdc
(Memory Enabled, V_{CC} = 5.25 Vdc)	$I_{PD\ max}$	-	73	
(Memory Disabled, V_{CC} = 5.25 Vdc)	$I_{PD\ min}$	-	55	

SWITCHING TIMES (V_{CC} = 5.0 Vdc)

Positive Input Address to Positive Output	I_{OL} = 10 mA driving 30 pF	t++	-	45	ns
Negative Input Address to Negative Output		t−−	-	45	ns
Positive Input Address or Enable to Negative Output		t+−	-	45	ns
Negative Input Address or Enable to Positive Output		t−+	-	45	ns

MC4039P*



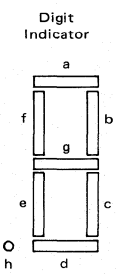
Output	a	b	c	d	e	f	g	h
Pin No.	12	11	5	4	13	14	2	3

V_{CC} = Pin 16
Gnd = Pin 8
Total Power Dissipation = 240 mW typ/pkg

The MC4039P is derived from the XC170 128-Bit Read Only Memory. It can directly operate low-voltage lamp indicators. A four digit binary input is translated into combinations of the eight outputs. These combinations correspond to different illuminated segments of the seven-bar digit indicator. The input and output codes with their related numerical digits are shown in the diagram. The enable inputs can be used for automatic blanking.

Features:
- Address times < 45 ns
- Outputs sink 20 mA
- Output capacitance < 7.0 pF @ 1.5 V
- Wired OR capability to 64 memories

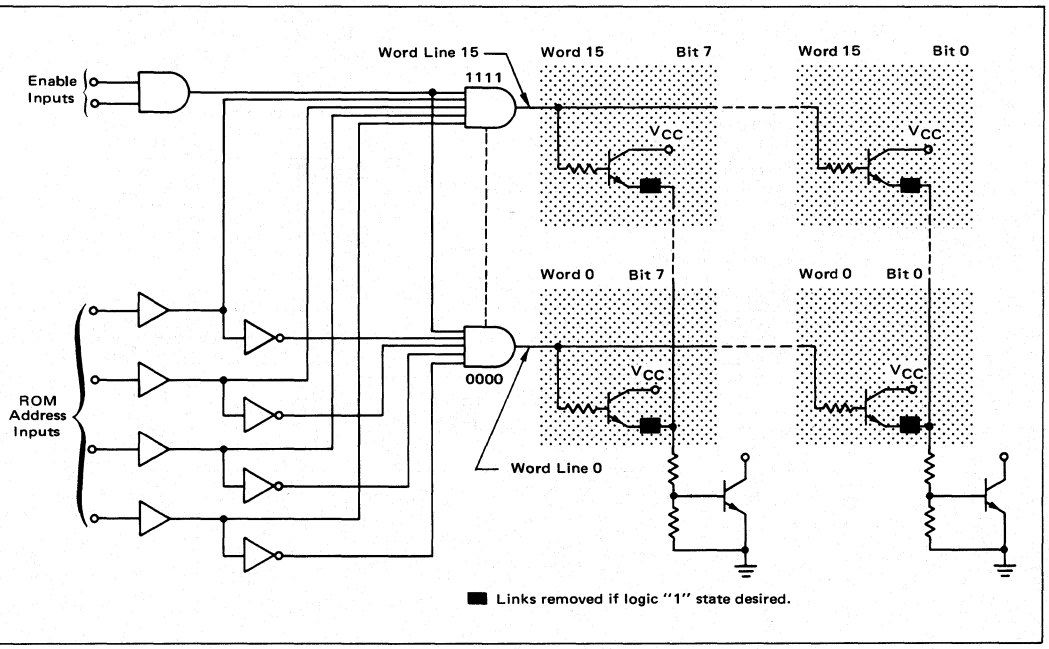
TRUTH TABLE (POSITIVE LOGIC)



DIGIT	SEGMENTS ILLUMINATED	INPUT D	C	B	A	OUTPUT a	b	c	d	e	f	g	h
0	a,b,c,d,e,f	0	0	0	0	0	0	0	0	0	0	1	1
1	b,c	0	0	0	1	1	0	0	1	1	1	1	1
2	a,b,d,e,g	0	0	1	0	0	0	1	0	0	1	0	1
3	a,b,c,d,g	0	0	1	1	0	0	0	0	1	1	0	1
4	b,c,f,g	0	1	0	0	1	0	0	1	1	0	0	1
5	a,c,d,f,g	0	1	0	1	0	1	0	0	1	0	0	1
6	c,d,e,f,g	0	1	1	0	1	1	0	0	0	0	0	1
7	a,b,c	0	1	1	1	0	0	0	1	1	1	1	1
8	a,b,c,d,e,f,g	1	0	0	0	0	0	0	0	0	0	0	1
9	a,b,c,f,g	1	0	0	1	0	0	0	1	1	0	0	1
NONE		1	0	1	0	1	1	1	1	1	1	1	1
•	h (Ext.)	1	0	1	1	1	1	1	1	1	1	1	0
–	g	1	1	0	0	1	1	1	1	1	1	0	1
NONE		1	1	0	1	1	1	1	1	1	1	1	1
NONE		1	1	1	0	1	1	1	1	1	1	1	1
NONE		1	1	1	1	1	1	1	1	1	1	1	1

ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	a	b	c	d	e	f	g	h
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							



*P suffix = 16-pin dual in-line plastic package (Case 612).

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	
MC400	1.0	
MC2000	0.67	Open Collector I_{OL} = 20 mA
MC3000	0.7	
MC7400	1.0	
MC830	1.15**	

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

** Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Supply Operating Voltage Range	V_{CC}	4.5 to 5.5	Vdc
Input Voltage	V_{in}	−1.5 to +5.5	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +75°C)

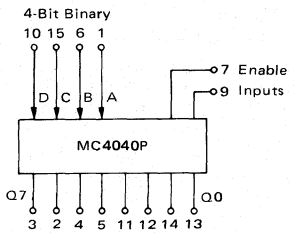
Characteristic	Symbol	Min	Max	Unit
Address Input Forward Current (V_A = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Enable Input Forward Current (V_E = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Address Input Leakage Current (V_A = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Enable Input Leakage Current (V_E = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Logical "0" Output Voltage (I_{OL} = 20 mAdc, V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	V_{OL}	-	0.45	Vdc
Logical "1" Output Leakage Current (V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CEX} = 7.0 Vdc, V_{CC} = 5.25 Vdc)	I_{CEX}	-	100	μAdc
Power Supply Drain Current				mAdc
(Memory Enabled, V_{CC} = 5.25 Vdc)	I_{PD} max	-	73	
(Memory Disabled, V_{CC} = 5.25 Vdc)	I_{PD} min	-	55	

SWITCHING TIMES (V_{CC} = 5.0 Vdc)

Positive Input Address to Positive Output	I_{OL} = 10 mA driving 30 pF	t++	-	45	ns
Negative Input Address to Negative Output		t−−	-	45	ns
Positive Input Address or Enable to Negative Output		t+−	-	45	ns
Negative Input Address or Enable to Positive Output		t−+	-	45	ns

BINARY TO
TWO-OF-EIGHT DECODER

MC4040P*



V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0	1	1	1	0
0	0	0	1	1	1	1	0	1	1	0	1
0	0	1	0	1	1	1	0	1	0	1	1
0	0	1	1	1	1	1	0	0	1	1	1
0	1	0	0	1	1	0	1	1	1	1	0
0	1	0	1	1	1	0	1	1	1	0	1
0	1	1	0	1	1	0	1	1	0	1	1
0	1	1	1	1	1	0	1	0	1	1	1
1	0	0	0	1	0	1	1	1	1	1	0
1	0	0	1	1	0	1	1	1	1	0	1
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	0	1	1	0	1	1	1
1	1	0	0	0	1	1	1	1	1	1	0
1	1	0	1	0	1	1	1	1	1	0	1
1	1	1	0	0	1	1	1	1	0	1	1
1	1	1	1	0	1	1	1	0	1	1	1

Total Power Dissipation = 200 mW typ/pkg

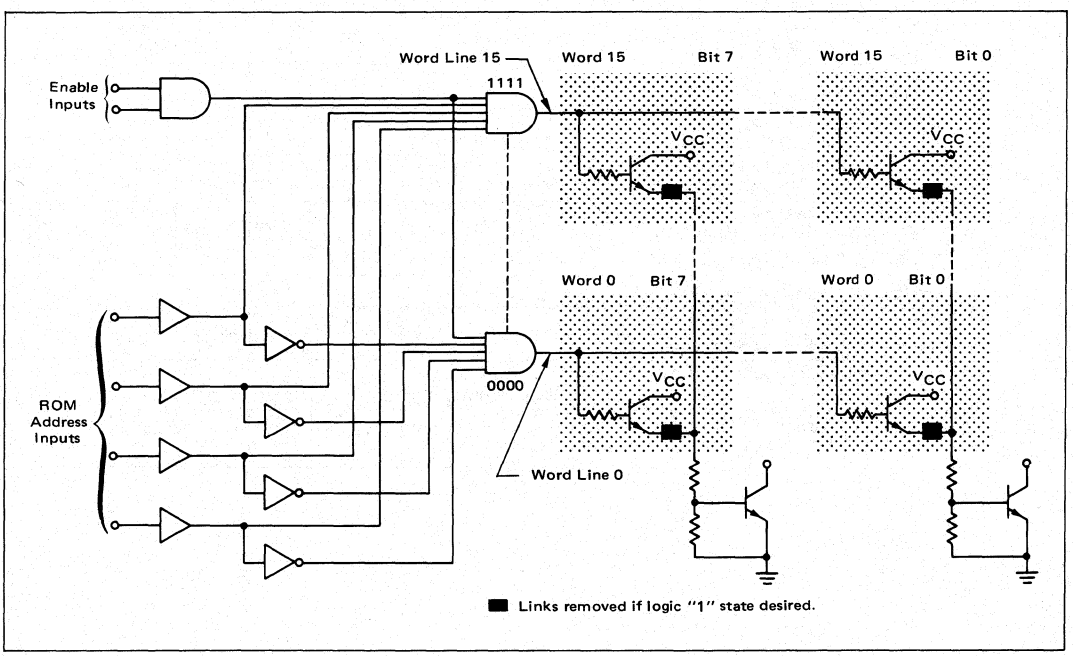
The MC4040P is derived from the XC170 128-Bit Read Only Memory. This device, with two enable inputs, transforms any 4-bit binary number to a 2-of-8-bit coded number. The device can also be thought of as a dual binary to 1-of-4 decoder.

Features:

- Address times < 45 ns
- Outputs sink 20 mA
- Output capacitance < 7.0 pF @ 1.5 V
- Wired OR capability to 64 memories

ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							



*P suffix = 16-pin dual in-line plastic package (Case 612).

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	
MC400	1.0	
MC2000	0.67	Open Collector I_{OL} = 20 mA
MC3000	0.7	
MC7400	1.0	
MC830	1.15**	

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

**Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Supply Operating Voltage Range	V_{CC}	4.5 to 5.5	Vdc
Input Voltage	V_{in}	−1.5 to +5.5	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +75°C)

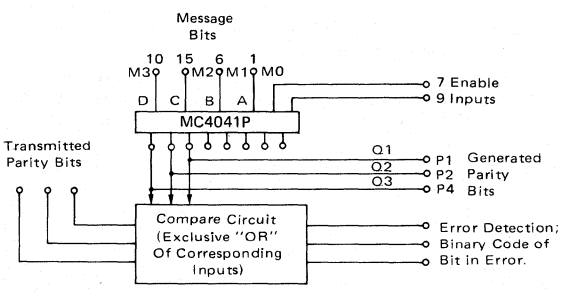
Characteristic	Symbol	Min	Max	Unit
Address Input Forward Current (V_A = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Enable Input Forward Current (V_E = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Address Input Leakage Current (V_A = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Enable Input Leakage Current (V_E = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Logical "0" Output Voltage (I_{OL} = 20 mAdc, V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	V_{OL}	-	0.45	Vdc
Logical "1" Output Leakage Current (V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CEX} = 7.0 Vdc, V_{CC} = 5.25 Vdc)	I_{CEX}	-	100	μAdc
Power Supply Drain Current				mAdc
(Memory Enabled, V_{CC} = 5.25 Vdc)	$I_{PD\ max}$	-	60	
(Memory Disabled, V_{CC} = 5.25 Vdc)	$I_{PD\ min}$	-	55	

SWITCHING TIMES (V_{CC} = 5.0 Vdc)

Positive Input Address to Positive Output	I_{OL} = 10 mA driving 30 pF	t++	-	45	ns
Negative Input Address to Negative Output		t−−	-	45	ns
Positive Input Address or Enable to Negative Output		t+−	-	45	ns
Negative Input Address or Enable to Positive Output		t−+	-	45	ns

SINGLE-ERROR HAMMING CODE DETECTOR AND GENERATOR

MC4041P*



Output	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Pin No.	13	14	12	11	5	4	2	3

V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	0
0	0	0	1	0	0	1	1	1	0	0	1
0	0	1	0	0	0	1	0	0	1	0	1
0	0	1	1	1	1	1	0	0	0	1	0
0	1	0	0	0	0	0	1	0	0	1	1
0	1	0	1	1	1	0	1	0	1	0	0
0	1	1	0	1	1	0	0	1	0	0	0
0	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	1	1	0	0	0	1	1	0
1	0	1	0	1	1	0	1	1	0	1	0
1	0	1	1	0	0	0	1	1	1	0	1
1	1	0	0	1	1	1	0	1	1	0	0
1	1	0	1	0	0	1	0	1	0	1	1
1	1	1	0	0	0	1	1	0	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

Simple Parity: The outputs of bits 0, 6, and 7 provide parity check over the 4 message bits.

Hamming Detection and Correction: Bits 1, 2, and 3 perform the parity calculations necessary for Hamming Code generation or detection on 4 message bits. For greater than 4 bits per message, ROM's may be cascaded. In these cases, bits 4, 5, 6, and 7 perform the necessary parity calculations.

Total Power Dissipation = 240 mW typ/pkg

For more information on this function and its uses, see Application Note AN-446, "The XC170 128-Bit Read Only Memory".

The MC4041P is a programmed 128-bit Read Only Memory suitable for a variety of error detection and correction applications.

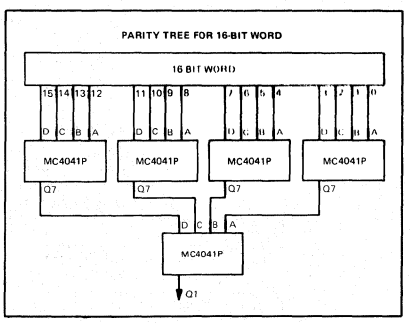
Simple parity trees for error detection can be constructed using the MC4041P as the basic building block. Also, more complex error control schemes, such as Hamming single error detection and correction, can be implemented with this device.

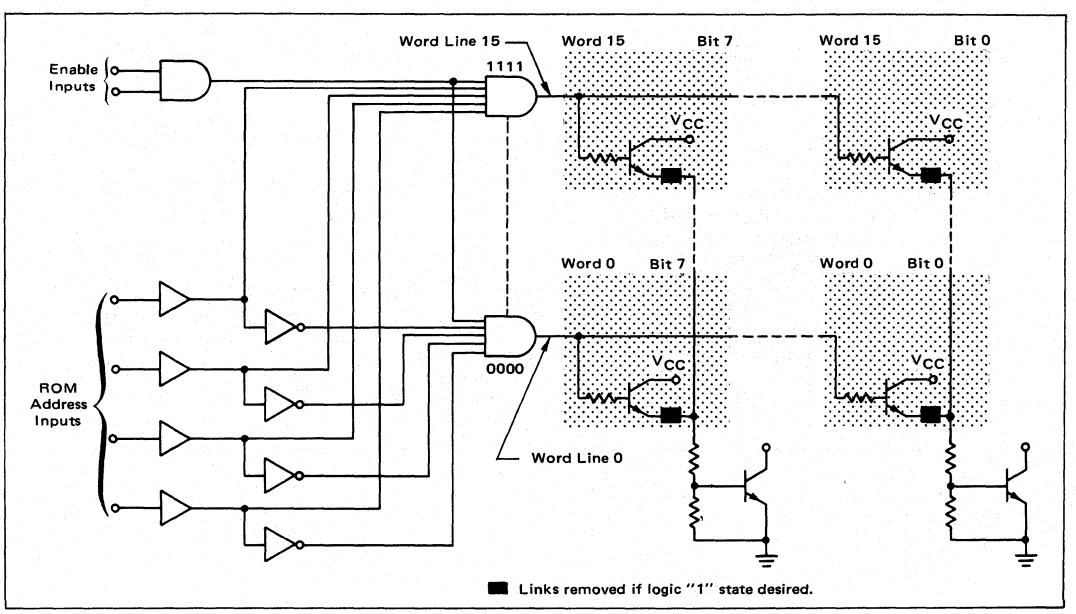
Features:

- Address times < 45 ns
- Outputs sink 20 mA
- Output capacitance < 7.0 pF @ 1.5 V
- Wired OR capability to 64 memories

ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							





*P suffix = 16-pin dual in-line plastic package (Case 612).

MC4041P (continued)

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	
MC400	1.0	
MC2000	0.67	Open Collector I_{OL} = 20 mA
MC3000	0.7	
MC7400	1.0	
MC830	1.15**	

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

**Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Supply Operating Voltage Range	V_{CC}	4.5 to 5.5	Vdc
Input Voltage	V_{in}	−1.5 to +5.5	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +75°C)

Characteristic	Symbol	Min	Max	Unit
Address Input Forward Current (V_A = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Enable Input Forward Current (V_E = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Address Input Leakage Current (V_A = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Enable Input Leakage Current (V_E = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Logical "0" Output Voltage (I_{OL} = 20 mAdc, V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	V_{OL}	-	0.45	Vdc
Logical "1" Output Leakage Current (V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CEX} = 7.0 Vdc, V_{CC} = 5.25 Vdc)	I_{CEX}	-	100	μAdc
Power Supply Drain Current				mAdc
(Memory Enabled, V_{CC} = 5.25 Vdc)	$I_{PD\ max}$	-	73	
(Memory Disabled, V_{CC} = 5.25 Vdc)	$I_{PD\ min}$	-	55	

SWITCHING TIMES (V_{CC} = 5.0 Vdc)

Positive Input Address to Positive Output	I_{OL} = 10 mA driving 30 pF	t++	-	45	ns
Negative Input Address to Negative Output		t−−	-	45	ns
Positive Input Address or Enable to Negative Output		t+−	-	45	ns
Negative Input Address or Enable to Positive Output		t−+	-	45	ns

QUAD PREDRIVER

MC4042F, L, P*

DUAL LINE SELECTOR

MC4043F, L, P*

The MC4042 and MC4043 are designed for magnetic memory driver/selector applications.

The MC4042 monolithic quad predriver consists of four high-speed switching transistors, each driven by an MTTL compatible NOR gate. Each NOR gate has an individual address input and a common timing input. The inputs of the MC4042 can be driven directly with standard MTTL decoders such as the MC4006 binary to one-of-eight decoder or the MC4007 dual binary to one-of-four decoder. The open-collector output transistor of the MC4042 will sink 50 mA.

The MC4043 monolithic dual line selector consists of two high-speed 400 mA switches driven by MTTL compatible NOR gates. Each NOR gate has an individual address input and a common timing input. The address and timing inputs of the MC4043 can also be driven directly with standard MTTL decoders such as the MC4006 and MC4007.

The MC4042 and MC4043 input circuits are the same, but the output circuitry is different as shown in the device schematics. The output transistors of both devices have a minimum BV_{CEX} of 15 volts, and are gold doped to increase switching speeds.

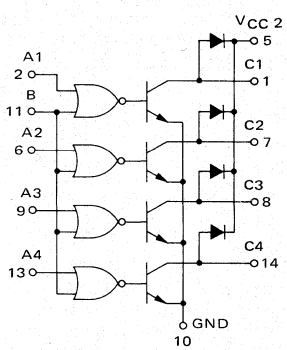
Many memory predriver applications employ transformer coupling between the predriver and driver stages. In such designs, large voltage overshoots occur due to the transformer inductance and high-speed switching currents. The collector of the MC4042 is internally clamped to prevent the collector from exceeding the maximum rated voltage during the switching transitions. The voltage applied to the diode clamp, pin 5, should be the same or greater than the collector voltages at pins 1, 7, 8, and 14, to prevent the diode clamp from being forward biased during nonswitching periods. The output transistor is driven with a conventional totem pole arrangement to provide active pullup and pulldown.

The collectors of the pullup transistors of the MC4043 are available at pins 1 and 7. An external load resistor to V_{CC} must be provided. This reduces power dissipation of the package and provides a means by which the speed of the device can be varied by changing the value of the pullup resistance.

The internal decoding circuitry of the MC4043 is such that both switches can be turned on at one time. However, due to power limitations, care must be taken to ensure that only one switch is turned on at any one time.

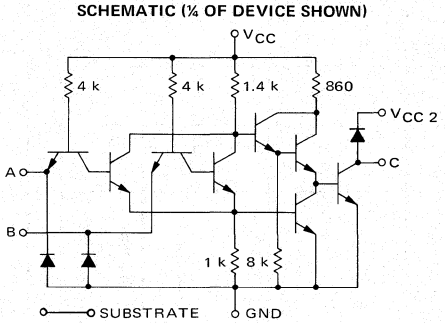
The MC4042 and MC4043 can provide a memory system with an inexpensive, reliable, fast drive system. They are also useful as relay or lamp drivers, high fan-out gates, and MOS drivers.

MC4042



Input Loading Factors:
A = 1, B = 4
Total Power Dissipation = 120 mW typ/pkg
Propagation Delay Time = 15 ns typ

SCHEMATIC (¼ OF DEVICE SHOWN)



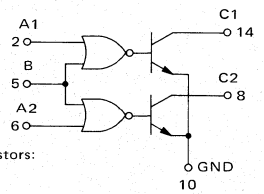
MC4042 AND MC4043

V_{CC} = PIN 4
GND = PIN 10
SUBSTRATE = PIN 3

TRUTH TABLE (One gate only)

A1	B	C1
0	0	0
0	1	1
1	0	1
1	1	1

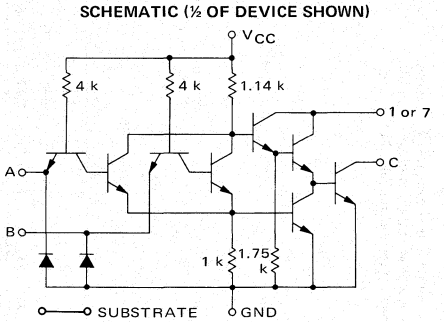
MC4043



Collectors of Output Transistors:
Gate 1 = Pin 1
Gate 2 = Pin 7

Input Loading Factors: A = 1, B = 2
Total Power Dissipation = 70 mW typ/pkg
Propagation Delay Time = 20 ns typ

SCHEMATIC (½ OF DEVICE SHOWN)



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS – MC4042

Test procedures are shown for the timing input, one address input, and one output. Test other inputs and outputs in the same manner.

@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
	mA				Volts									
	I_{OL}	I_{in}	4 I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{CC2}
0°C	50	1.0	4.0	-	1.0	2.0	0.4	2.5	15	-	5.0	4.75	5.25	12
+25°C	50	1.0	4.0	10	1.0	1.7	0.4	2.5	15	7.0	5.0	4.75	5.25	12
+75°C	50	1.0	4.0	-	1.0	1.4	0.4	2.5	15	-	5.0	4.75	5.25	12

Characteristic	Symbol	Pin Under Test	MC4042 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	4 I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{CC2}	Gnd
Input																								
Forward Current	I_F	2	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	-	-	-	2	11	-	-	-	-	4	-	3,10
		11	-	-6.4	-	-6.4	-	-6.4	mAdc	-	-	-	-	-	-	11	2,6,9,13	-	-	-	-	4	-	3,10
Leakage Current	I_R	2	-	40	-	40	-	40	μAdc	-	-	-	-	-	-	-	2	-	-	-	-	4	-	3,10
		11	-	160	-	160	-	160	μAdc	-	-	-	-	-	-	-	11	-	-	-	-	4	-	3,10
Breakdown Voltage	BV_{in}	2	5.5	-	5.5	-	5.5	-	Vdc	-	2	-	-	-	-	-	-	-	-	-	-	4	-	3,10
		11	5.5	-	5.5	-	5.5	-	Vdc	-	-	11	-	-	-	-	-	-	-	-	-	4	-	3,10
Output																								
Output Voltage	V_{OL}	1	-	0.5	-	0.5	-	0.5	Vdc	1	-	-	-	2	-	11	-	-	-	-	4	-	-	3,10
		1	-	0.5	-	0.5	-	0.5	Vdc	1	-	-	-	11	-	2	-	-	-	-	4	-	-	3,10
Output Leakage Current	I_{CEX}	1	-	250	-	250	-	250	μAdc	-	-	-	-	-	2	11	-	1	-	-	4	-	-	3,10
		1	-	250	-	250	-	250	μAdc	-	-	-	-	-	11	2	-	1	-	-	4	-	-	3,10
Clamp Voltage	V_D	1	-	-	-	1.5	-	-	Vdc	-	-	-	1	-	-	-	2,11	-	-	-	4	-	-	3,5,10
Power Requirements																								
Maximum Power Supply Current	I_{max}	4	-	-	-	36	-	-	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	-	3,10
Power Supply Drain	I_{PDL}	4	-	42	-	42	-	42	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	-	-	2,3,6,9,10,11,13
	I_{PDH}	4	-	23	-	23	-	23	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	-	-	3,10
Switching Parameters										Pulse In A	Pulse In B		Pulse Out											
Turn-On Delay Time	t_{pd-}	11,1	-	-	-	25	-	-	ns	2	11		1	-	-	-	-	-	-	4	-	-	5	3,10
Turn-Off Delay	t_{pd+}	11,1	-	-	-	25	-	-	ns	2	11		1	-	-	-	-	-	-	4	-	-	5	3,10

ELECTRICAL CHARACTERISTICS – MC4043

Test procedures are shown for the timing input, one address input, and one output. Test other inputs and outputs in the same manner.

@ Test Temperature	I_{OL} (mA)	I_{in} (mA)	2 I_{in} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{out} (Volts)	V_{CEX} (Volts)	V_{max} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)
0°C	400*	1.0	2.0	1.1	2.0	0.4	2.5	5.5	15	-	5.0	4.75	5.25
+25°C	400*	1.0	2.0	1.1	1.8	0.4	2.5	5.5	15	7.0	5.0	4.75	5.25
+75°C	400*	1.0	2.0	0.9	1.8	0.4	2.5	5.5	15	-	5.0	4.75	5.25

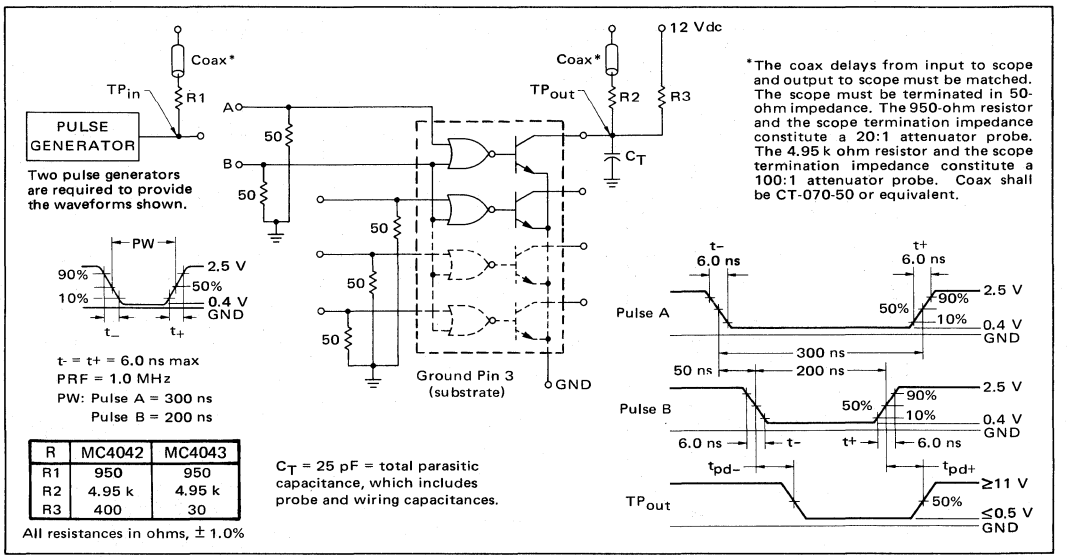
Characteristic	Symbol	Pin Under Test	MC4043 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	2 I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{out}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	**	Gnd
Input																								
Forward Current	I_F	2	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	-	-	2	5.6	-	-	-	-	-	4	-	3,10
		5	-	-3.2	-	-3.2	-	-3.2	mAdc	-	-	-	-	-	5	2.6	-	-	-	-	-	4	-	3,10
Leakage Current	I_R	2	-	40	-	40	-	40	μAdc	-	-	-	-	-	-	2	-	-	-	-	-	4	-	3,5,6,10
		5	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	5	-	-	-	-	-	4	-	2,3,6,10
Breakdown Voltage	BV_{in}	2	5.5	-	5.5	-	5.5	-	Vdc	-	2	-	-	-	-	-	-	-	-	-	-	4	-	3,10
		5	5.5	-	5.5	-	5.5	-	Vdc	-	-	5	-	-	-	-	-	-	-	-	-	4	-	3,10
Output																								
Output Voltage	V_{OL}*	14	-	0.5	-	0.5	-	0.5	Vdc	14	-	-	5	-	2	-	-	-	-	-	4	-	1	3,10
		14	-	0.5	-	0.5	-	0.5	Vdc	14	-	-	2	-	5	-	-	-	-	-	4	-	1	3,10
Output Leakage Current	$I_{CEX\ 1}$	14	-	2.0	-	2.0	-	2.0	mAdc	-	-	-	-	5	-	-	-	14	-	-	4	-	-	3,10
		14	-	2.0	-	2.0	-	2.0	mAdc	-	-	-	-	2	-	-	-	14	-	-	4	-	-	3,10
	$I_{CEX\ 2}$	1	-	500	-	500	-	500	μAdc	-	-	-	2	5	-	-	1	-	-	-	-	4	-	3,10
		1	-	500	-	500	-	500	μAdc	-	-	-	5	2	-	-	1	-	-	-	-	4	-	3,10
Power Requirements																								
Maximum Power Supply Current	I_{max}	4	-	-	-	35	-	-	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	-	-	3,10
Power Supply Drain	I_{PD}	4	-	12	-	12	-	12	mAdc	-	-	-	2	-	5	-	-	-	-	4	-	-	-	3,10
		4	-	12	-	12	-	12	mAdc	-	-	-	6	-	5	-	-	-	-	4	-	-	-	3,10
Switching Parameters										Pulse In A	Pulse In B	Pulse Out												
Turn-On Delay Time	t_{pd-}	5,14	-	-	-	35	-	-	ns	2	5	1‡	-	-	-	-	-	-	-	4	-	-	1	3,10
Turn-Off Delay Time	t_{pd+}	5,14	-	-	-	26	-	-	ns	2	5	1‡	-	-	-	-	-	-	-	4	-	-	1	3,10

*Pulsed, 40% duty cycle @ 1.0 MHz.

**Connect pins to V_{CC} through a 75-ohm resistor.

11

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



R	MC4042	MC4043
R1	950	950
R2	4.95 k	4.95 k
R3	400	30

All resistances in ohms, ± 1.0%

C_T = 25 pF = total parasitic capacitance, which includes probe and wiring capacitances.

MC4042 TYPICAL SWITCHING TIMES

FIGURE 1 – TURN-ON DELAY TIME versus TEMPERATURE

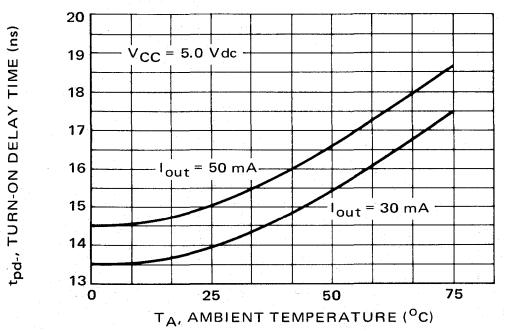


FIGURE 2 – TURN-OFF DELAY TIME versus TE

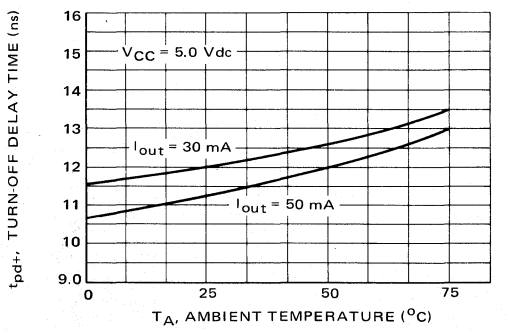


FIGURE 3 – TURN-ON DELAY TIME versus POWER SUPPLY VOLTAGE

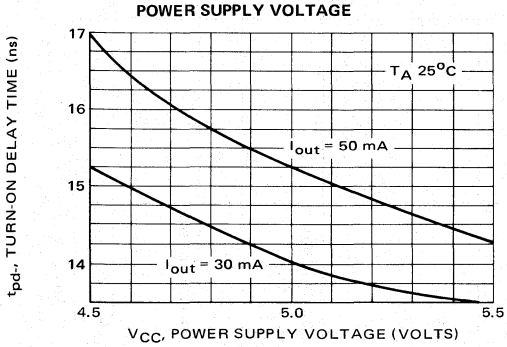
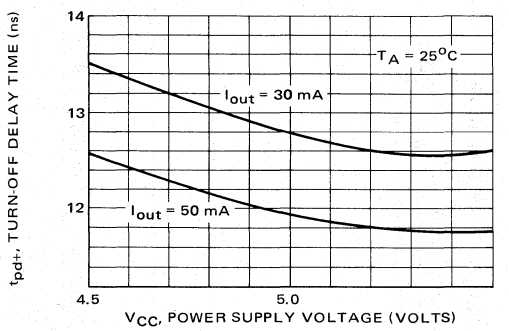


FIGURE 4 – TURN-OFF DELAY TIME versus POWER SUPPLY VOLTAGE



MC4043 TYPICAL SWITCHING TIMES

FIGURE 5 – PROPAGATION DELAY TIME versus PULLUP RESISTANCE (Pins 1 and 7)

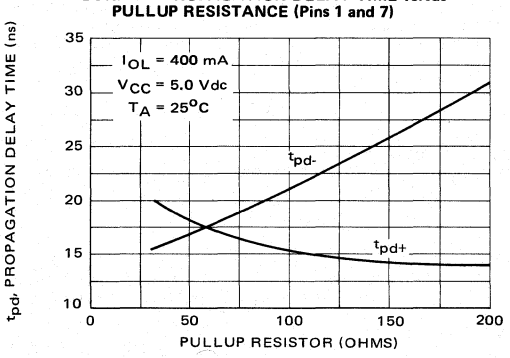


FIGURE 6 – PROPAGATION DELAY TIME versus TEMPERATURE

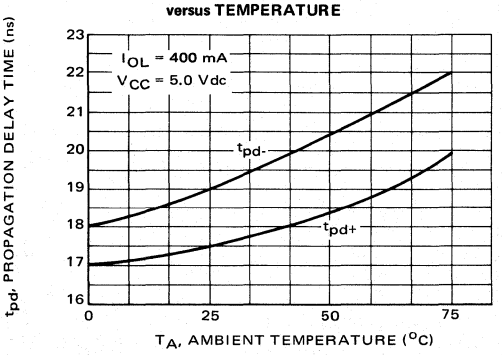


FIGURE 7 – PROPAGATION DELAY TIME versus COLLECTOR CURRENT

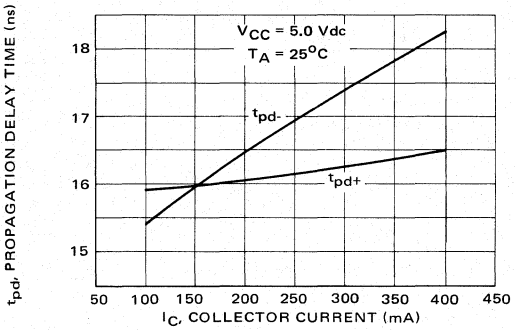
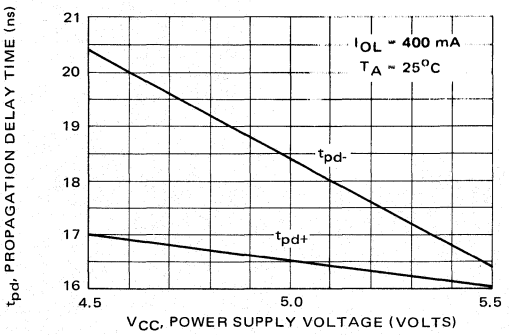
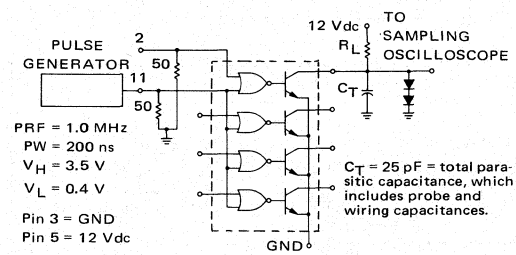


FIGURE 8 – PROPAGATION DELAY TIME versus POWER SUPPLY VOLTAGE



OUTPUT VOLTAGE VARIATIONS

FIGURE 9 – MC4042



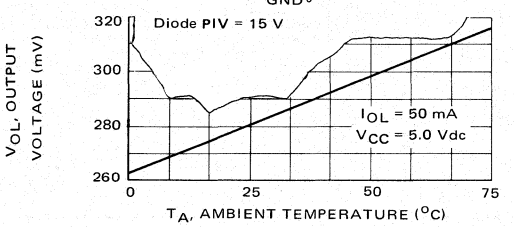
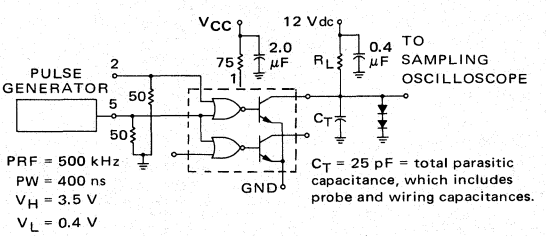
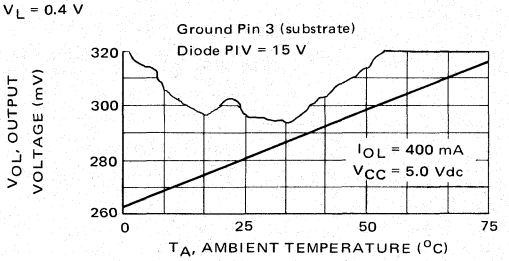


FIGURE 10 – MC4043

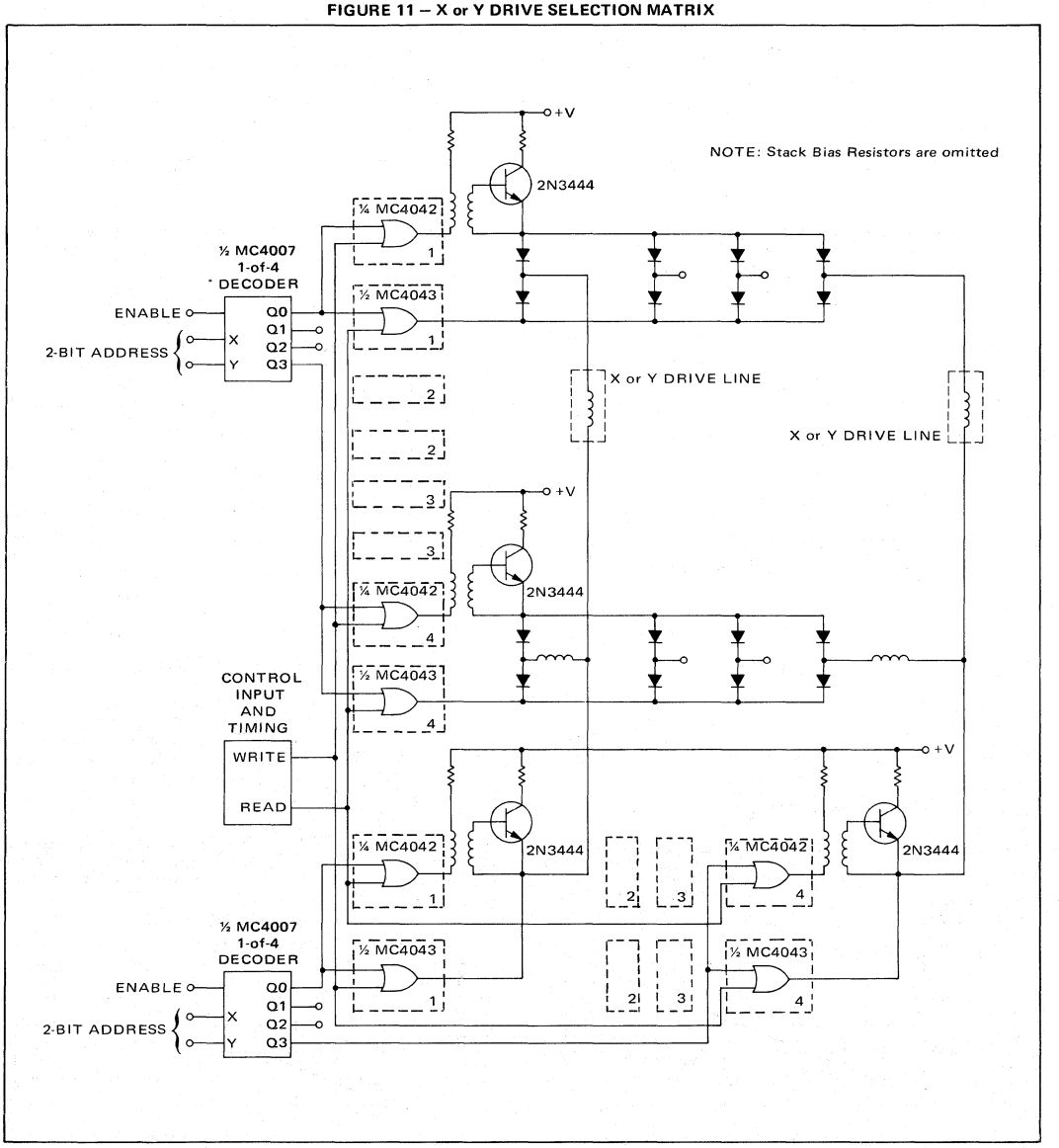




TYPICAL APPLICATION

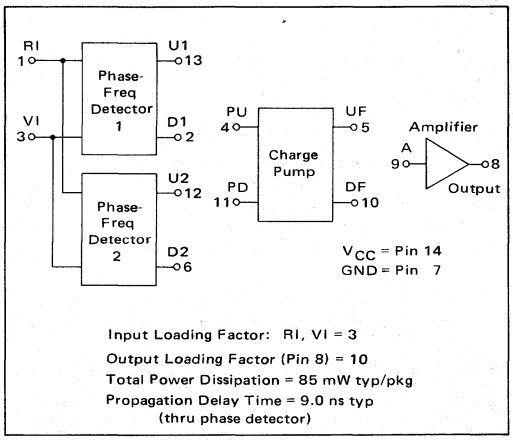
Figure 11 illustrates a typical core memory driver/selector using MC4042 and MC4043 devices. The source circuit for the X or Y drive line consists of an MC4042 predriver transformer coupled to a fast high-current transistor. The sink circuit is the MC4043 line selector. The source and sink circuits are used in pairs and are arranged to permit bipolar currents to pass through a selected drive line. Supply voltage and resistor values are determined by system requirements.

FIGURE 11 – X or Y DRIVE SELECTION MATRIX



PHASE-FREQUENCY DETECTOR

MC4344F, L*
MC4044F, L, P*



Input Loading Factor: RI, VI = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

This device contains two digital phase detectors and a charge pump circuit which converts MTTL inputs to a dc voltage level for use in frequency discrimination and phase-locked-loop applications.

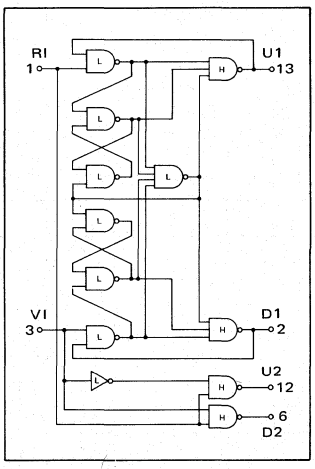
The two phase detectors have common inputs. Phase-frequency detector 1 is locked in (indicated by both outputs high) when the negative transitions of the variable input (VI) and reference input (RI) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, the U1 (up) output goes low; conversely the D1 (down) output goes low when the variable input is higher in frequency or leads the reference input in phase. It is important to note that the duty cycles of the variable input and the reference input are not important since negative transitions control system operation.

Phase detector 2, on the other hand, is locked in when the variable input phase lags the reference phase by 90° (indicated by the U2 and D2 outputs alternately going low with equal pulse widths). If the variable input phase lags by more than 90°, U2 will remain low longer than D2, and, conversely, if the variable input phase lags the reference phase by less than 90°, D2 remains low longer. In this phase detector the variable input and the reference must have 50% duty cycles.

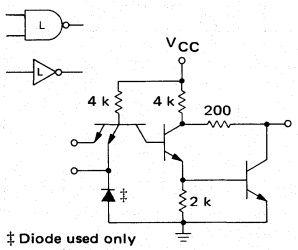
The charge pump accepts the phase detector outputs (U1 or U2 applied to PU, and D1 or D2 applied to PD) and converts them to fixed amplitude positive and negative pulses at the UF and DF outputs respectively. These pulses are applied to a lag-lead active filter, which incorporates external components, as well as the amplifier provided in the MC4344/4044 circuit. The filter provides a dc voltage proportional to the phase error.

PHASE DETECTOR

The phase detector portion of this device is constructed using low and high-level gates interconnected as shown by the logic diagram.

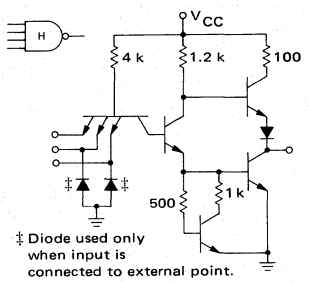


LOW-LEVEL "NAND" GATE



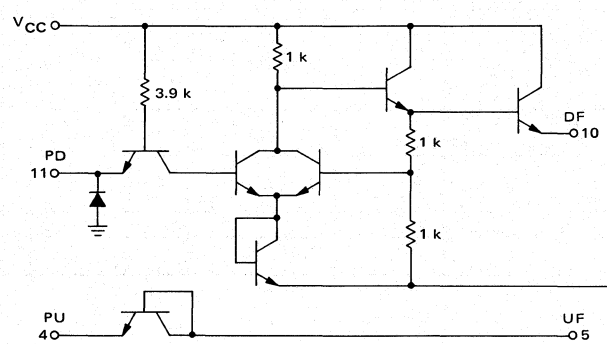
‡ Diode used only when input is connected to external point.

HIGH-LEVEL "NAND" GATE

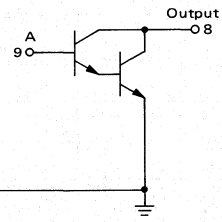


‡ Diode used only when input is connected to external point.

CHARGE PUMP



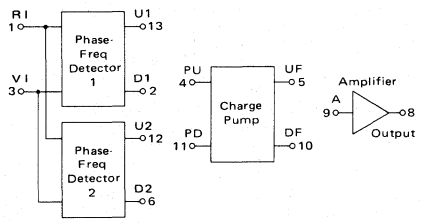
AMPLIFIER



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

MC4344F,L , MC4044F,L,P (continued)

ELECTRICAL CHARACTERISTICS



INPUT STATE	INPUT RI	INPUT VI	OUTPUT U1	OUTPUT D1	OUTPUT U2	OUTPUT D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

1. X indicates output state unknown.
2. U1 and D1 outputs are sequential; i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_D	I_A	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}
MC4344	-55°C	20	-1.6	-1.0	–	–	0.002	1.1	2.0	0.4	2.4	4.5	1.5	5.0	4.5	5.5
	+25°C	20	-1.6	-1.0	1.0	-10	0.002	1.1	1.8	0.4	2.4	4.5	1.5	5.0	4.5	5.5
	+125°C	20	-1.6	-1.0	–	–	0.002	0.9	1.8	0.4	2.4	4.5	1.5	5.0	4.5	5.5
MC4044	0°C	20	-1.6	-1.0	–	–	0.002	1.1	2.0	0.4	2.5	4.5	1.5	5.0	4.75	5.25
	+25°C	20	-1.6	-1.0	1.0	-10	0.002	1.1	1.8	0.4	2.5	4.5	1.5	5.0	4.75	5.25
	+75°C	20	-1.6	-1.0	–	–	0.002	0.9	1.8	0.4	2.5	4.5	1.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4344 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4044 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_D	I_A	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Gnd
Input																																
Forward Current	I_F	1	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	mAdc	–	–	–	–	–	–	–	–	1	–	–	–	–	–	14	–	7
		3	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	↓	–	–	–	–	–	–	–	–	3	–	–	–	–	–	↓	–	↓
		11	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	–	11	–	–	–	–	–		–	
Leakage Current	I_R	1	–	120	–	120	–	120	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	–	–	1	–	–	–	–	14	–	7
		3	–	120	–	120	–	120	–	120	–	120	–	120		–	–	–	–	–	–	–	–	–	3	–	–	–	–	14	–	7
		4	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0		–	–	–	–	–	–	–	–	–	–	–	–	–	–	4	–	5,7
		11	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	–	11	–	–	–	–	14	–	7
Breakdown Voltage	BV_{in}	1	–	–	5.5	–	–	–	–	–	5.5	–	–	–	Vdc	–	–	–	1	–	–	–	–	–	–	–	–	–	–	14	–	7
		3	–	–	↓	–	–	–	–	–	↓	–	–	–	↓	–	–	–	3	–	–	–	–	–	–	–	–	–	–	↓	–	↓
		11	–	–		–	–	–	–	–		–	–	–		–	–	–	11	–	–	–	–	–	–	–	–	–	–		–	
Clamp Voltage	V_D	1	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	1	–	–	–	–	–	–	–	–	–	14	–	7
		3	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	3	–	–	–	–	–	–	–	–	–	14	–	7
Output (Note 1)																																
Output Voltage	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	6	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
		12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	12	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OL}	6	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	6	–	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	V_{OH}	12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	12	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	6	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OL}	12	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	12	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	V_{OL}	13	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	13	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OL}	13	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	13	–	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OL}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	2	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	V_{OL}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	2	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
Short-Circuit Current	I_{SC}	2	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	–	3	1	–	–	–	–	–	–	14	2,7
		6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	6,7
		12														–	–	–	–	–	–	1,3	–	–	–	–	–	↓	–	–	7,12
		13														–	–	–	–	–	–	3	1	–	–	–	–		–	–	7,13
Leakage Current	I_{OLK}	2	–	250	–	250	–	250	–	250	–	250	–	250	μAdc	–	–	–	–	–	–	3	1	–	–	–	–	14	–	–	7
		6	–	↓	–	↓	–	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	–	–	1,3	–	–	–	–	–	↓	–	–	↓
		12	–		–		–		–		–		–			–	–	–	–	–	–	1,3	–	–	–	–	–		–	–	
		13	–		–		–		–		–		–			–	–	–	–	–	–	3	1	–	–	–	–		–	–	
Collector-Emitter Voltage	V_{CE}	5	–	–	0.5	–	–	–	–	–	0.5	–	–	–	Vdc	–	–	–	5	–	–	–	–	–	–	–	–	–	–	–	–	4,7
Output Voltage	V_{EH}	10	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	Vdc	–	–	10	–	–	–	11	–	–	–	–	–	–	14	–	–	7
Output Current	I_O	8	0.2	–	0.8	–	1.0	–	0.5	–	0.8	–	1.0	–	mAdc	–	–	–	–	9	–	–	–	–	–	–	–	–	–	8	–	7
Leakage Current	I_{OLK}	8	–	120	–	120	–	120	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	–	–	–	–	–	–	8	–	7,9
		10	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	μAdc	–	–	–	–	–	–	–	–	–	11	10	–	–	14	–	7
Power Requirements (Total Device)																																
Power Supply Drain	I_{PD}	14	–	40	–	40	–	40	–	40	–	40	–	40	mAdc	–	–	–	–	–	–	–	–	–	–	–	–	14	–	–	7

Note 1. The outputs of the device must be tested by sequencing through the indicated input states according to the truth table and functional diagram. All input, power supply and ground voltages must be maintained between tests unless otherwise noted. Procedures identified by a double asterisk (**) in the Symbol column are necessary to change the state of the sequential logic.

Pulse 1: V_{CCL} ⌐ V_{CC} Used to change power supply voltage from previous test.

APPLICATIONS INFORMATION

FIGURE 1 – PHASE-LOCKED, FREQUENCY SYNTHESIZER LOOP

Figure 1 shows the MC4344/4044 in a phase-locked loop with the following features:

1. Zero phase error between the reference frequency and the output of the divide-by-N feedback, achieved because phase-frequency detector 1 locks negative edges in the system;
2. Adjustable channel spacing, achieved by changing the pre-scaling factor (÷P) when generating the reference frequency;
3. Digitally programmed tuning of the output, in multiples of the reference frequency, accomplished by changing N in the divide-by-N chain in the feedback loop.

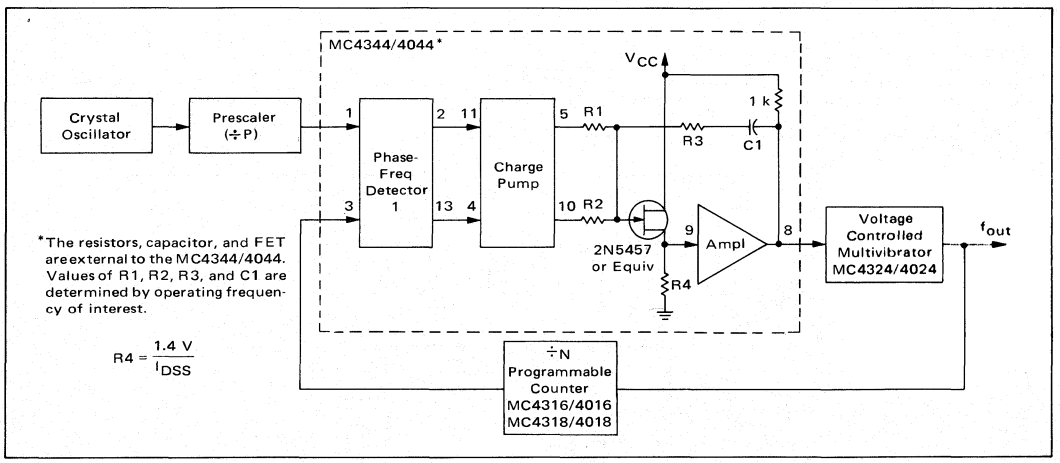
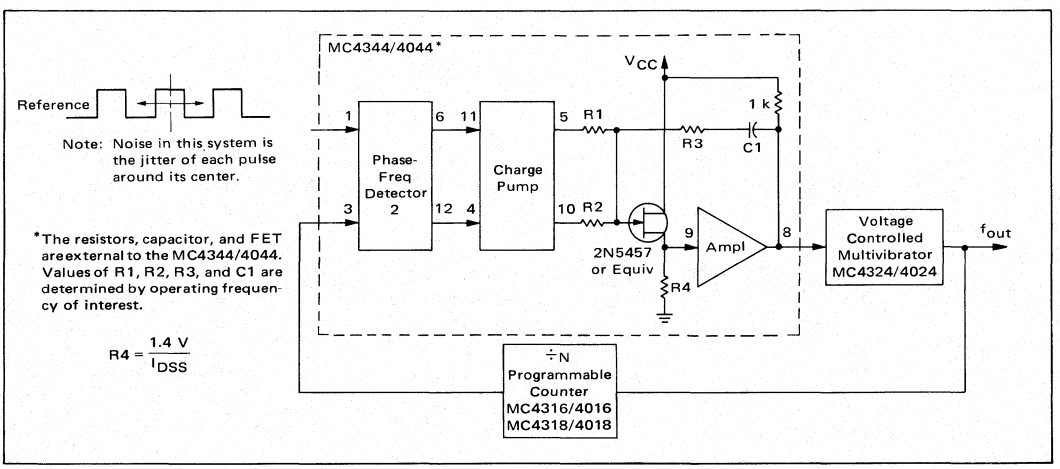


Figure 2 shows phase detector 2 of the MC4344/4044, which operates as a correlation detector, used in a phase-locked loop. There are two differences between this system and that shown in Figure 1. First, the VCM output, when locked in, lags the reference by 90°. Second, since the correlation detector integrates the product of its two inputs over each cycle, it can handle signals in a high-noise environment. This loop is sensitive to harmonics, therefore care must be taken to limit the frequency range of the VCM.

FIGURE 2 – PHASE-LOCKED, CORRELATION DETECTOR LOOP

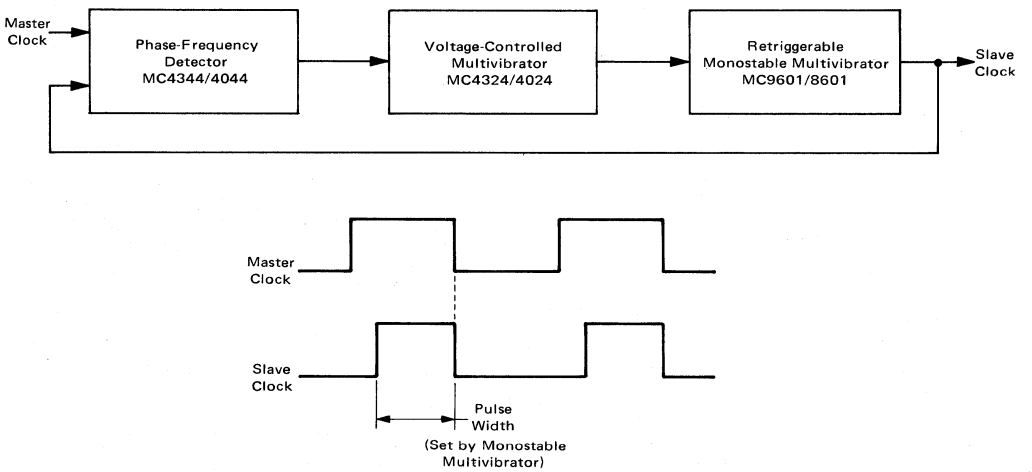


APPLICATIONS INFORMATION (continued)

FIGURE 3 – SLAVE CLOCK PULSE GENERATOR

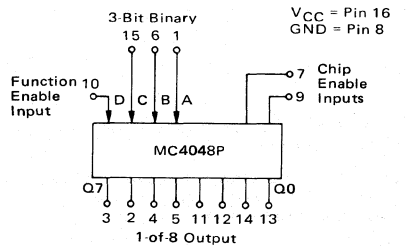
Figure 3 depicts the MC4344/4044 in a system used to generate a slave clock pulse with its negative edge locked to the negative edge of the master clock, but with adjustable pulse width. The pulse width of the slave clock pulse is controlled only by the monostable multivibrator, which is triggered from the negative edge of an input pulse.

The slave clock application is useful when the clock from a master computer must be slaved to that of a satellite.



NON-INVERTING
ONE-OF-EIGHT DECODER

MC4048P*



TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Total Power Dissipation
= 240 mW typ/pkg

ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

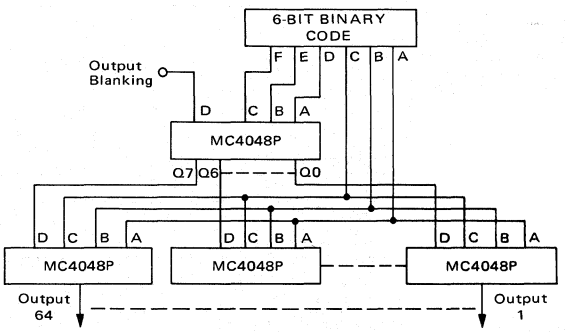
E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							

The MC4048P is derived from the XC171 128-bit Read Only Memory. A 3-bit binary address selects the desired word for the 8-bit output, and the selected output goes to a logic "1". The function enable input, D, is useful for expansion of the decoding function. When D is a logic "0" all outputs are logic "0". A logic "1" on D produces a logic "1" on the selected output.

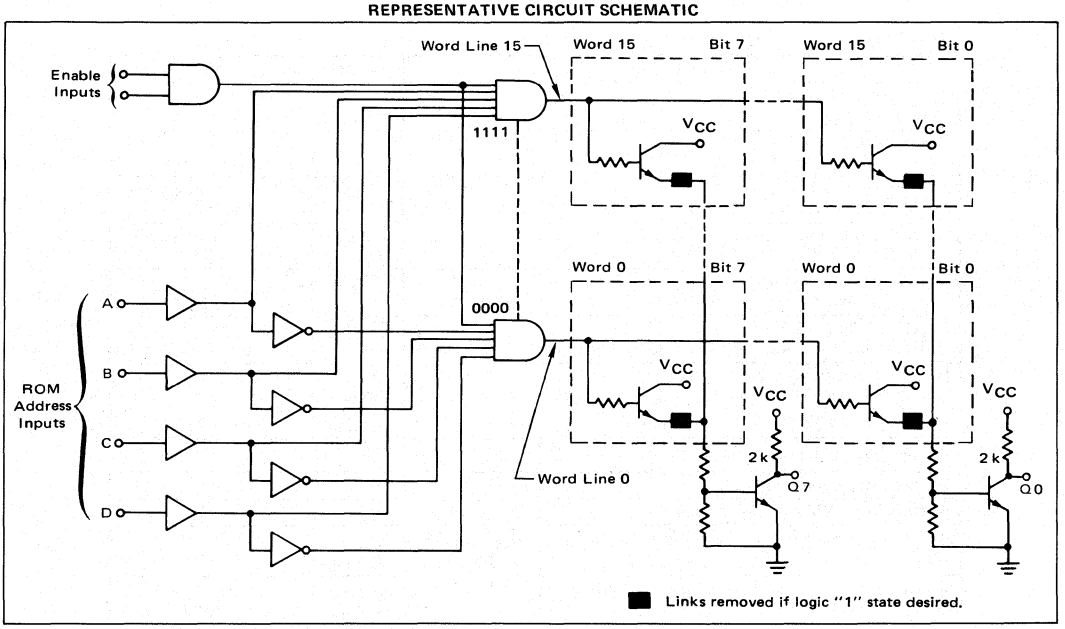
Features:

- Address times < 50 ns
- Outputs sink 16 mA
- Output capacitance < 7.0 pF @ 1.5 V

1-OF-64 DECODER
(Selected output is a positive logic "1")



REPRESENTATIVE CIRCUIT SCHEMATIC



*P suffix = 16-pin dual in-line plastic package (Case 612).

INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4048 INPUT LOADING FACTOR	MC4048 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	7
MC3000	0.7	7
MC7400	1.0	10
MC830	1.15**	11

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

** Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Supply Operating Voltage Range	V_{CC}	4.5 to 5.5	Vdc
Input Voltage	V_{in}	−1.5 to +5.5	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +75°C)

Characteristic	Symbol	Min	Max	Unit
Address Input Forward Current (V_A = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Enable Input Forward Current (V_E = 0, V_{CC} = 5.0 Vdc)	I_F	-	1.6	mAdc
Address Input Leakage Current (V_A = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Enable Input Leakage Current (V_E = 5.5 Vdc, V_{CC} = 5.0 Vdc)	I_R	-	100	μAdc
Logical "0" Output Voltage (I_{OL} = 16 mAdc, V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	V_{OL}	-	0.45	Vdc
Logical "1" Output Voltage (I_{OH} = 0.5 mAdc, V_{IL} = 0.9 Vdc, V_{IH} = 2.0 Vdc, V_{CC} = 4.75 Vdc)	V_{OH}	2.5	-	Vdc
Power Supply Drain Current (Memory Enabled, V_{CC} = 5.25 Vdc)	I_{PD} max	-	85	mAdc
(Memory Disabled, V_{CC} = 5.25 Vdc)	I_{PD} min	-	55	

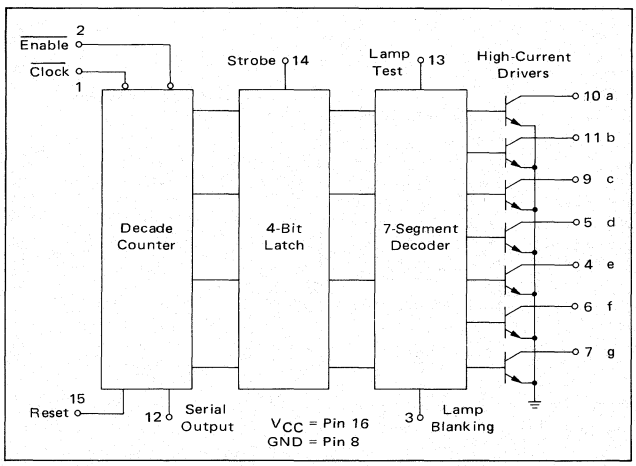
SWITCHING TIMES (V_{CC} = 5.0 Vdc)

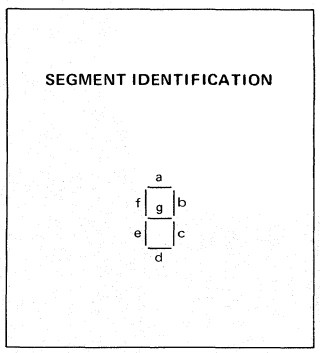
Positive Input Address to Positive Output	I_{OL} = 10 mA driving 30 pF	t_{A+B+}	-	50	ns
Negative Input Address to Negative Output		t_{A-B-}	-	50	ns
Positive Input Address or Enable to Negative Output		t_{A+B-} or t_{E+B-}	-	50	ns
Negative Input Address or Enable to Positive Output		t_{A-B+} or t_{E-B+}	-	50	ns

MC4350L*
MC4050L, P*

ADVANCE INFORMATION/NEW PRODUCT

This device is a monolithic MSI integrated circuit combining the functions of an NBCD counter, four-bit latch, and a seven-segment decoder/driver. The counter advances on the negative edge of the $\overline{\text{Clock}}$, subject to control by the $\overline{\text{Enable}}$ input. The Serial Output is high driving the ninth count, allowing synchronous or asynchronous counter operation when used in conjunction with the $\overline{\text{Enable}}$ input and some external gating. The counter Reset places the counter in a non-NBCD state, turning off the output driver transistors when transferred through the latch and decoded. This feature gives automatic suppression of leading zeros in the display. The latch section admits information while the Strobe is high and latches the data on the negative edge of the strobe. The seven-segment decoder/driver provides up to 40 mA drive capability for displays which require current sinking in the active mode. A lamp blanking input is provided for intensity modulation. A lamp test feature is also available.



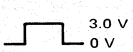


Total Power Dissipation = 450 mW typ/package
Maximum Toggle Frequency = 35 MHz typ

FUNCTIONAL TRUTH TABLE

FUNCTION	INPUT $\overline{C}$	$\overline{E}$	R	S	LT	LB	OUTPUT S_{out}	a	b	c	d	e	f	g
Lamp Test	X	X	X	X	1	X	–	0	0	0	0	0	0	0
Lamp Blanking	X	X	X	X	0	1	–	1	1	1	1	1	1	1
Reset	X	X	1	1	0	0	0	1	1	1	1	1	1	1
Enable	P	1	0	1	0	0	0	1	1	1	1	1	1	1
State Sequence 1	P1	0	0	1	0	0	0	1	0	0	1	1	1	1
2	P2	0	0	1	0	0	0	0	0	1	0	0	1	0
3	P3	0	0	1	0	0	0	0	0	0	0	1	1	0
4	P4	0	0	1	0	0	0	1	0	0	1	1	0	0
5	P5	0	0	1	0	0	0	0	1	0	0	1	0	0
6	P6	0	0	1	0	0	0	0	1	0	0	0	0	0
7	P7	0	0	1	0	0	0	0	0	0	1	1	1	1
8	P8	0	0	1	0	0	0	0	0	0	0	0	0	0
9	P9	0	0	1	0	0	1	0	0	0	0	1	0	0
0	P10	0	0	1	0	0	0	0	0	0	0	0	0	1
1	P11	0	0	1	0	0	0	1	0	0	1	1	1	1
Latch	P	0	0	0	0	0	0	1	0	0	1	1	1	1

P = any number of pulses may be applied
P_n = n pulses on the Clock input
X = Don't care



*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

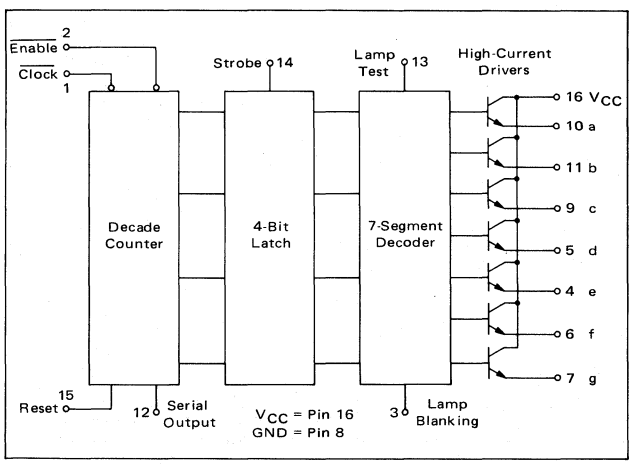
MC4051P*

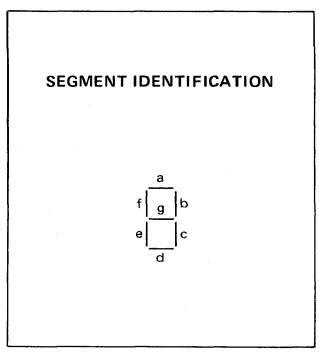
11

Advance Information

This device is a monolithic MSI integrated circuit combining the functions of an NBCD counter, four-bit latch, and a seven-segment decoder/driver. The counter advances on the negative edge of the $\overline{\text{Clock}}$, subject to control by the $\overline{\text{Enable}}$ input. The Serial Output is high driving the ninth count, allowing synchronous or asynchronous counter operation when used in conjunction with the $\overline{\text{Enable}}$ input and some external gating. The counter Reset places the counter in a non-NBCD state, turning off the output driver transistors when transferred through the latch and decoded. This feature gives automatic suppression of leading zeros in the display. The latch section admits information while the Strobe is high and latches the data on the negative edge of the strobe. The seven-segment decoder/driver is active high and will source up to 40 mA at a 10% duty cycle or 15 mA at a 100% duty cycle. A lamp blanking input is provided for intensity modulation. A lamp test feature is also available.

The output structure of this device is an open emitter-follower configuration whose equivalent circuit is a voltage source with a relatively small series resistance. Although this resistance increases when the output is grounded, the situation is potentially destructive to the device. When the outputs are in the high ("1") state, they should not be connected to ground through an impedance of less than 100 ohms.



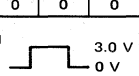


Total Power Dissipation = 450 mW typ/package
Maximum Toggle Frequency = 35 MHz typ

FUNCTIONAL TRUTH TABLE

FUNCTION		INPUT $\overline{C}$	$\overline{E}$	R	S	LT	LB	OUTPUT S_{out}	a	b	c	d	e	f	g
Lamp Test		X	X	X	X	1	X	–	1	1	1	1	1	1	1
Lamp Blanking		X	X	X	X	0	1	–	0	0	0	0	0	0	0
Reset		X	X	1	1	0	0	0	0	0	0	0	0	0	0
$\overline{\text{Enable}}$		P	1	0	1	0	0	0	0	0	0	0	0	0	0
State Sequence	1	P1	0	0	1	0	0	0	0	1	1	0	0	0	0
	2	P2	0	0	1	0	0	0	1	1	0	1	1	0	1
	3	P3	0	0	1	0	0	0	1	1	1	1	0	0	1
	4	P4	0	0	1	0	0	0	0	1	1	0	0	1	1
	5	P5	0	0	1	0	0	0	1	0	1	1	0	1	1
	6	P6	0	0	1	0	0	0	1	0	1	1	1	1	1
	7	P7	0	0	1	0	0	0	1	1	1	0	0	0	0
	8	P8	0	0	1	0	0	1	1	1	1	1	1	1	1
	9	P9	0	0	1	0	0	0	1	1	1	1	0	1	1
	0	P10	0	0	1	0	0	0	1	1	1	1	1	1	0
	1	P11	0	0	1	0	0	0	0	1	1	0	0	0	0
	Latch	P	0	0	0	0	0	0	0	1	1	0	0	0	0

P = any number of pulses may be applied
P_n = n pulses on the Clock input
X = Don't care



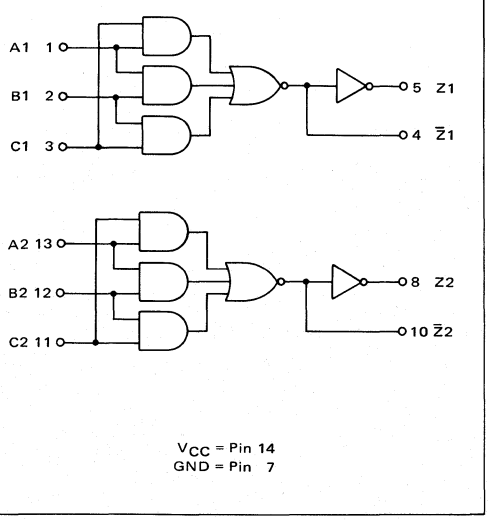
*P suffix = 16-pin dual in-line plastic package (Case 612).

This is advance information on a new introduction and specifications are subject to change without notice.

DUAL
MAJORITY LOGIC GATE

MC4062P*

Advance Information

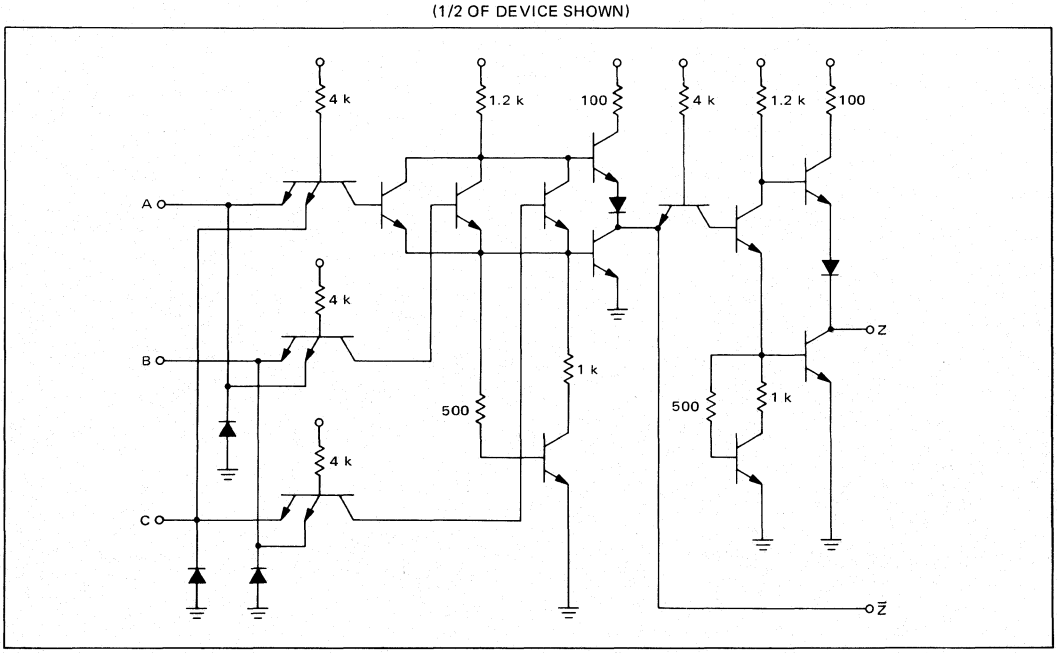


This integrated circuit offers the designer additional versatility in logic design. When any two or all three of the inputs are raised to the "1" level, the output goes to the "1" level. The output, Z, and its complement, $\overline{Z}$, are both available.

INPUT			OUTPUT	
A	B	C	Z	$\overline{Z}$
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

Total Power Dissipation = 75 mW typ/pkg
Propagation Delay Time = 20 ns typ (Z Output)
11 ns typ ($\overline{Z}$ Output)

CIRCUIT SCHEMATIC
(1/2 OF DEVICE SHOWN)



This is advance information on a new introduction and specifications are subject to change without notice.
*P suffix = TO-116 dual in-line plastic package (Case 605).

MTTL

INTEGRATED CIRCUITS

MC5400/MC7400 SERIES

MTTL

MC5400/7400 SERIES
INTEGRATED CIRCUITS

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MTTL

GENERAL INFORMATION

MC5400/7400 Series

INTRODUCTION

The MTTL MC5400/7400 series of transistor-transistor logic is a medium-speed, high-noise immunity family of saturating integrated logic circuits designed for general digital logic applications requiring clock frequencies to 30 MHz and switching speeds in the 7-11 ns range under moderate capacitive loading.

The circuits in the MC5400/7400 series are identified by a multiple emitter input transistor and an active "pull-up" in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The active pull-up output configuration provides low impedance in the high output state. The resulting low impedances in both states provide excellent ac noise immunity and allows high-speed operation while driving large capacitive loads.

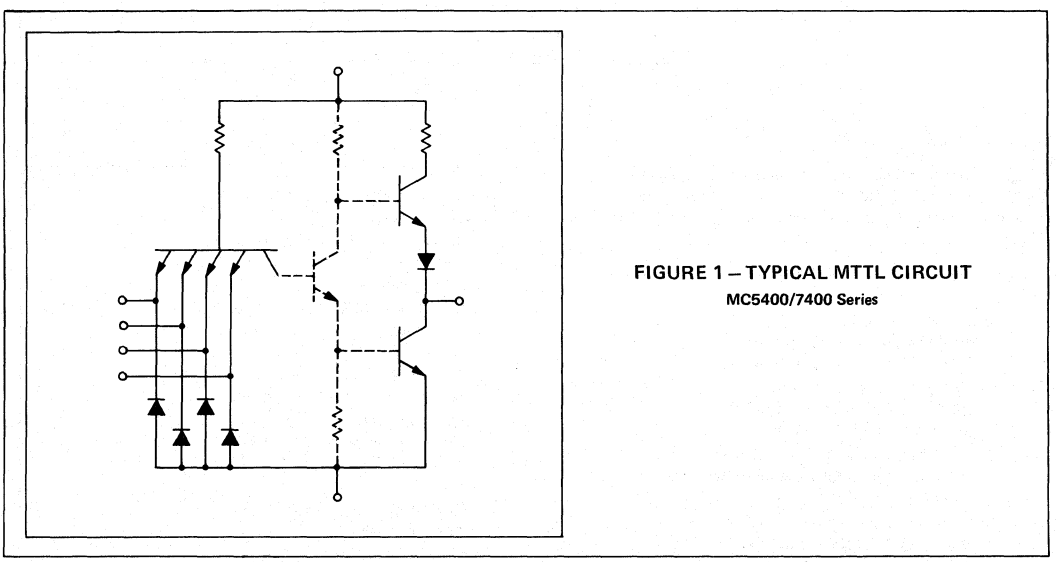


FIGURE 1 – TYPICAL MTTL CIRCUIT
MC5400/7400 Series

1.0 – General Description

The purpose of this section is to provide guidelines for the use of MC5400/7400 series digital integrated circuits. It is arranged in three parts: the first containing maximum ratings, typical characteristics, package descriptions, and definitions; the second a briefly worded description of recommended design procedures; and the third a more detailed explanation of the reasoning behind these recommendations.

1.1 – Maximum Ratings

The maximum rating table is perhaps the most important portion of the General Information Section. Failure to observe these ratings can result in catastrophic device failure. It is important to note that this rating table does not guarantee that a device will operate if the values noted are not exceeded—it only states that exceeding these values may induce failures. Also, it is not enough to guarantee that any one limit is not exceeded. For example, a maximum supply voltage of 6.5 volts is within the rating, but may induce failure if the design is such that input voltage ratings or maximum junction temperatures are exceeded as a result of the high supply voltage. The only exceptions to this rule involve currents and voltages applied to input terminals. The table is constructed to allow the designer to limit either current or voltage to a safe value.

MAXIMUM RATINGS

Rating		Value	Unit
Supply Voltage, Operating	MC5400 Series MC7400 Series	4.5 to 5.5 4.75 to 5.25	Vdc
Supply Voltage, Continuous	All Types	7.0	Vdc
Input Forward Current — Continuous — Pulsed < 30 ms		-10 -30	mAdc
OR			
Negative Voltage at Input — Continuous — Pulsed < 30 ms		-0.5 -1.5	Vdc
Maximum Input Reverse Current		1.5	mAdc
OR			
Maximum Positive Voltage at Input		5.5	Vdc
Operating Temperature Range	MC5400 Series MC7400 Series	-55 to +125 0 to + 70	°C
Storage Temperature Range	MC5400 Series MC7400 Series	-65 to +150 -55 to +125	°C
Maximum Junction Temperature	MC5400 Series MC7400 Series	+175 +150	°C

1.2 – Typical Characteristics

The following summary presents the typical operating characteristics of the MTTL MC5400/7400 series. Unless otherwise indicated, the parameters are defined for V_{CC} = +5.0 volts and T_A = +25°C.

Supply Voltage Operating Range
- MC5400 Series = 4.5 to 5.5 volts
- MC7400 Series = 4.75 to 5.25 volts

Operating Temperature Range
- MC5400 Series = -55 to +125°C
- MC7400 Series = 0 to +70°C

Output Drive Capability
- Other Gates (Output Loading Factor) = 10
- Capacitance = 600 pF

Output Impedance
- High State = 70 ohms (unsaturated) nominal
- Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits
- +5.5 volts maximum
- -0.5 volt minimum

Switching Threshold = 1.5 volts nominal

Input Impedance
- High State = 400 kilohms nominal
- Low State = 4.0 kilohms nominal

Worst-Case DC Noise Margin
- High State — 0.400 volt minimum
- Low State — 0.400 volt minimum

Power Dissipation
- Basic Gate = 10 mW typ/gate
- Basic Flip-Flop = 40 mW typ/pkg

Thermal Resistance — Junction To Case (θ_{JC})
- Ceramic Package = 0.09°C/mW
- Plastic Package = 0.15°C/mW

Thermal Resistance — Junction To Ambient (θ_{JA})
- Ceramic Package = 0.26°C/mW
- Plastic Package = 0.30°C/mW

Switching Speeds
- Average Propagation Delay = 10 ns per gate typical
  30 ns per flip-flop typical
- Rise Time = 2.5 ns typical
- Fall Time = 1.5 ns typical

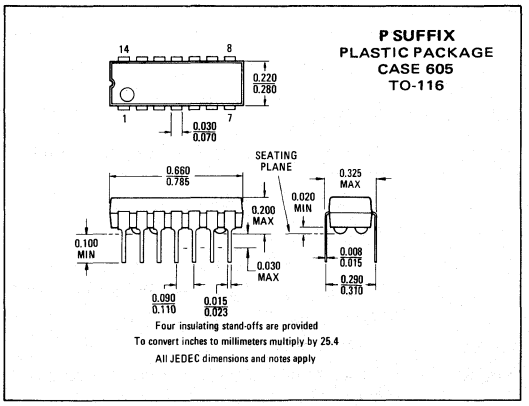
Flip-Flop Clock Frequency = 30 MHz maximum

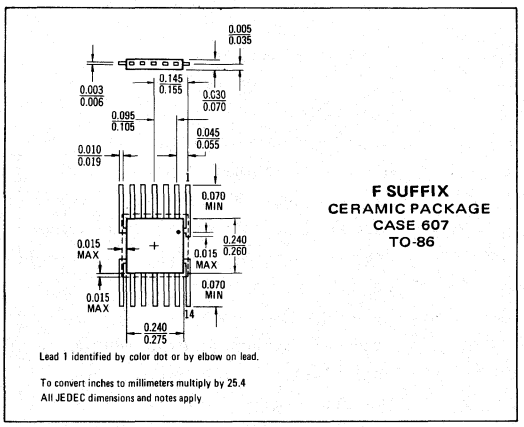
1.3 – Package Description

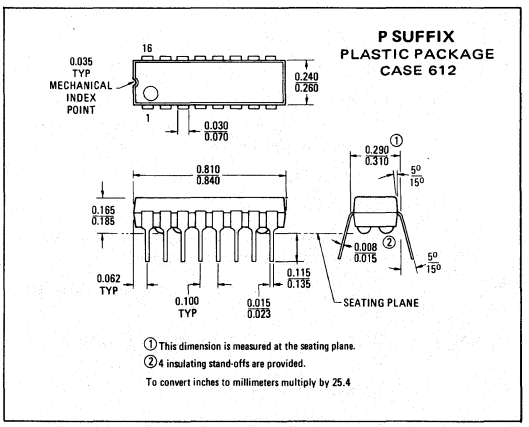
Package type is denoted by a suffix to the part number as follows:

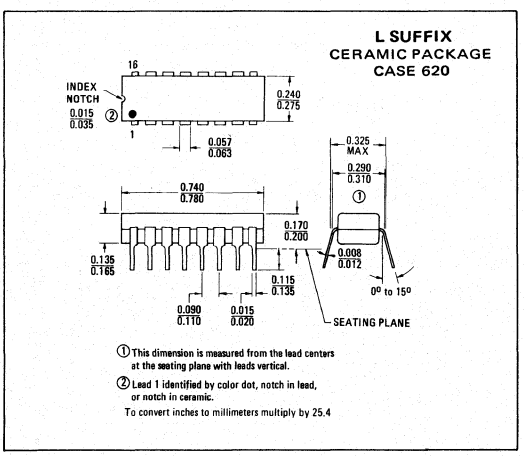
Suffix	Description
F	Ceramic Flat
L	Ceramic Dual In-Line
P	Plastic Dual In-Line

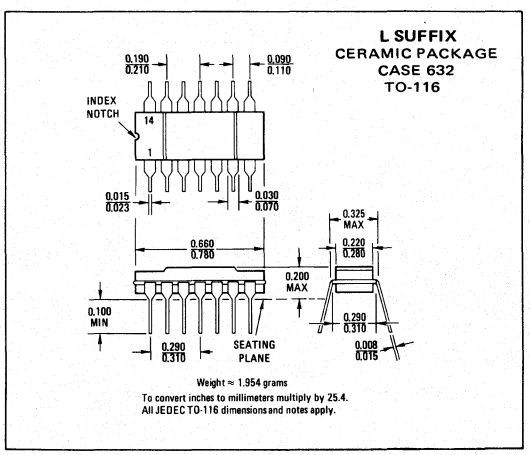
PACKAGE DIMENSIONS











1.4 – Definitions

C_T	Total parasitic capacitance, which include probe, wiring, and load capacitances	t_{pd+}	Turn-off delay time
f_{Tog}	Toggle frequency	t_{pd-}	Turn-on delay time
I_{CEX}	Collector-emitter leakage of the output transistor	t_{sd+}	Turn-off delay time from direct $\overline{SET}$ and $\overline{RESET}$ inputs
I_{DR}	Expander output drive current	t_{sd-}	Turn-on delay time from direct $\overline{SET}$ and $\overline{RESET}$ inputs
I_{EX}	Expander input current	TP_{in}	Test point at input of device under test
I_F	Input forward current	TP_{out}	Test point at output of device under test
I_{OH}	Output logic "1" state source current	V_{BE}	Base-emitter voltage
I_{OL}	Output logic "0" state sink current	V_{CC}	Power supply voltage
I_{PD}	Power supply current drain	V_{CCH}	Maximum operating power supply voltage
I_{PDH}	Power supply current drain with inputs in logic "1" state	V_{CCL}	Minimum operating power supply voltage
I_{PDL}	Power supply current drain with inputs in logic "0" state	V_{CEX}	Output transistor collector-emitter voltage
I_{R1}	Input reverse current with V_{IH} applied	V_{EN}	Input enable voltage level
I_{R2}	Input reverse current with V_{IHH} applied	V_{EX}	Expander terminal voltage
I_{SC}	Logic "1" state source current with output shorted to ground	V_{IH}	Logic "1" state input voltage
I_X	Expander terminal test current	V_{IHH}	Input breakdown voltage
PRF	Pulse repetition frequency	V_{IL}	Logic "0" state input voltage
R_{EX}	Resistor connected between expander terminals on expandable AOI gates	V_{INH}	Input inhibit voltage level
R_{EX1}	Resistor from expander output emitter to ground	V_{O1}	Expander output reverse voltage
R_{EX2}	Resistor from expander output collector to V_{CCL}	V_{O2}, V_{O3}	Expander output transistor emitter voltage
t+	Voltage rise time	V_{OH}	Logic "1" state output voltage
t-	Voltage fall time	V_{OL}	Logic "0" state output voltage
		V_R	Input reference voltage
		V_{th} "0"	Logic "0" state input threshold voltage
		V_{th} "1"	Logic "1" state input threshold voltage
		Z_{out}	Output impedance

2.0 — Summary of MC5400/7400 Series Usage Suggestions

This portion of the General Information section presents answers to some of the most commonly asked questions regarding the use of MC5400/7400 series components. This summary only presents the recommendations, while part 3.0 of this section also gives the reasoning behind the suggestion. Coincident numbering is used to facilitate referencing. For example, paragraph 2.2 gives suggestions for bypassing—paragraph 3.2 further explains the reasons for bypassing.

It should be noted that these suggestions are for optimum system design and may not be applicable in all situations.

2.1 — Power and Ground Distribution

1. Use ground planes where practical.
2. When ground planes cannot be used, leave as much metal as possible for the ground line.

2.2 — Bypassing

1. Use a comparatively large (1.0 μF range) capacitor where power and ground enter the board.
2. Use one or more high-frequency (0.01 μF or less) capacitors per board. Distribute these as follows:
   a. Use a minimum of one high-frequency capacitor for every eight packages.
   b. Decrease the IC package/capacitor ratio when driving large capacitive loads, operating near the upper frequency limit, or using a high concentration of complex functions.
   c. Use more high-frequency capacitors if necessary to insure that no package power (or ground) pin is located more than eight inches from a capacitor terminal.

2.3 — Power Supply Requirements

1. Maintain voltage within nominal 5.0 volt value ±10% for MC5400 series, ±5% for MC7400 series.
2. Multiple supplies may be used without sacrifice in load capability provided item 1 is followed and ground is common.
3. For worst-case design, sum the values of I_{PDL} or I_{PDH} (whichever is greater) for all packages in the system to determine dc power drain. Add ac power requirement from item 5.
4. For typical design, sum the average of I_{PDL} and I_{PDH} for all packages in the system to determine dc power drain. Add ac power requirement from item 5 as well as an appropriate safety factor.
5. Determine ac power drain from product of system clock rate, total number of outputs, and ac power factor (0.06 mA/MHz).

2.4 — Disposition of Unused Inputs

1. NAND Gates — Tie to used input or return to logic "1".
2. NOR Gates — Return to ground.
3. AND-OR-INVERT Gates — Leave unused expander inputs open. If all inputs of an AND section are unused, return one or more to ground. If at least one input on all AND sections is used, apply rule for NAND gates to unused inputs.
4. Flip-flop J, K, $\overline{SET}$, $\overline{RESET}$ — Return to logic "1".
5. Flip-flop $\overline{J}$, $\overline{K}$, SET, RESET, CLOCK, $\overline{CLOCK}$ — Return to ground.

2.5 — Disposition of Unused Gates

1. NAND Gates — Return one or more inputs of the unused gate to ground.
2. NOR Gates — Return all inputs of the unused gate to ground.
3. AND-OR-INVERT Gates — Leave expander inputs open, Return at least one input of each AND section to ground.
4. Flip-flops — Return CLOCK ($\overline{CLOCK}$), J ($\overline{J}$), K ($\overline{K}$), and either SET ($\overline{SET}$) or RESET ($\overline{RESET}$) to ground.

2.6 — Generation of Logic "1" for Unused Input Disposition

1. Use output of unused gate.
2. Use V_{CC} directly if power supply spikes can be limited such that input voltage is always less than 5.5 volts.
3. Use 1.0 kilohm limiting resistor to V_{CC}. Up to 35 inputs may be connected to a single resistor. Restriction on V_{CC} is governed by maximum rating.
4. Use reference voltage supply between 2.4 and 5.5 volts.

2.7 — Expander Inputs of AOI Gates

1. Keep lead length to expander input nodes as short as possible.
2. Make allowances for additional propagation delay (typically 1.0 ns/AND input) if expanders are used.
3. Observe restriction on data sheet as to the maximum number of expanders that may be used.

2.8 — Parallel Operation of Outputs

1. The "Implied AND" function (wired collector) should not be implemented with active pull-up MTTL gates.
2. Parallel operation of both inputs and outputs to obtain increased load driving capability is permissible from a dc standpoint. See 3.8 for ac restrictions.

2.9 — Open-Collector Gates

1. Connect an external pull-up resistor from V_{CC} to the output of the open collector gate when used to drive other logic circuits.
2. When driving lines greater than 18 inches, locate a pull-up resistor at the receiving end of line.
3. The pull-up resistor must satisfy both of the following equations:

   a. $$R \leq \frac{V_{CC} - V_{OH}}{N_1 I_R + N_2 I_{CEX}}$$

   b. $$R \geq \frac{V_{CC} - V_{OL}}{I_{OL} - N_1 I_F}$$

   where N_1 = number of inputs driven
   N_2 = number of open-collector gate outputs in parallel.

4. System design should not subject output transistors to voltage greater than V_{CEX}.

2.10 – Loading Factors

1. When driving other MC5400/7400 series inputs, the output loading factor of the driving gate should not exceed the sum of all input loading factors connected to that load.
2. When driving MTTL circuits other than MC5400/7400 series, the sum of all input forward currents (I_F) connected to an output should not exceed the specified low-level output load current (I_{OL}). Similarly, the sum of all input reverse currents (I_R) should not exceed the specified high-level output load current (I_{OH}).
3. Use the criteria outlined in item 2 when driving MC5400/7400 series loads with other MTTL circuits or when interfacing with MDTL.

3.0 – MC5400/MC7400 Series Usage Suggestions

The guidelines presented here for use of MC5400/7400 series devices are intended for optimizing a system from a performance standpoint. Sometimes it is desirable to compromise on performance in order to reduce size or cost, etc. Thus, the following paragraphs not only present the suggestions for use, but also the reasoning behind these recommendations.

3.1 – Power and Ground Distribution

The typical rate of change of currents and voltages for a single MTTL gate is in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system. Ground planes represent the most effective way of reducing this impedance, but this isnot mandatory. It is best to leave as much metal as possible for the ground line, however, as this helps to reduce I_R drops.

3.2 – Bypassing

A single bypass capacitor at the output of the power supply usually does not provide adequate filtering for MTTL circuitry. The supply lines must be regarded as antennas in addition to the fact that they are inherently inductive. Thus, if the supply terminals are more than a few inches from the point where power enters the board, either internally or externally generated noise can be troublesome. It is therefore normally wise to bypass supply and ground at the point where power and ground enter the board.

When dealing with low-speed devices, bypass capacitors are usually judged by their size—the bigger the better. It must be remembered, however, that MTTL circuits generate (and respond to) signals of only a few nanoseconds. At these speeds, a large capacitor takes on the characteristics of an inductor. While a large capacitor is advisable to filter low-frequency voltage changes, one or more small (high-frequency) capacitors should be used to effectively reduce the noise on supply and ground lines. In order to be most effective, the inductance of the entire bypass circuitry must be minimized. This not only requires small bypass capacitors, ($\leq 0.1\ \mu F$) but also limits the line length permissible between the capacitor and the integrated circuit. Eight inches has been found to be a good rule of thumb for this distance.

Mention should be made of the fact that MTTL circuits generate noise on the supply line due to current spikes during switching. This is caused by both transistors in the totem pole output conducting simultaneously for a short period of time. The exact time period is determined by circuit characteristics and by the amount of capacitance which must be charged by the output. Thus, the number of bypass capacitors needed depends on how many totem-pole outputs are being served, the operating frequency, and the capacitive load on the outputs. One capacitor for every eight packages is normally adequate.

3.3 – Power Supply Requirements

The MC5400 series circuits are tested over a voltage range of 4.5 to 5.5 volts while the MC7400 series is tested at 4.75 to 5.25 volts. If the supply voltage is allowed to deviate from these limits, the devices may fail to function. In general, gate circuits will operate over a wider range than that specified if output loading is reduced, but flip-flops (and complex functions containing flip-flops) may cease to operate regardless of loading if proper supply voltage is not maintained.

The parameters used to determine loading factors are tested under absolute worst-case supply conditions. For example, the drive current (I_{OL}) of an MC7400 series gate is tested with a supply voltage of 4.75 volts while the input load current (I_F) is specified at a supply voltage of 5.25 volts. This means that operation is guaranteed even when multiple supplies are used.

Power-drain current is specified for all MTTL components. In many cases, this parameter is specified with all inputs low (I_{PDL}) as well as with all inputs high (I_{PDH}). For a worst-case design, the greater of these two limits should be used. In many systems, however, it is safe to assume that 50 percent of the gates will be in a low dissipation state at any given time. In such instances, the required current can be calculated by averaging I_{PDH} and I_{PDL}.

For system operation at 1.0 MHz and above, ac power dissipation can become important. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.30 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL circuits.

3.4 – Disposition of Unused Inputs

An unused input of an MC5400/7400 series circuit represents a high-impedance node which is inherently susceptable to noise. Termination of the unused input is required to counteract this. Connecting an unused input to a used input on the same gate is a simple method of termination, but it does increase loading and cannot always be used on flip-flops and complex functions, etc. Paragraph 3.6 explains methods of generating a logic "1" when required.

3.5 – Disposition of Unused Gates

An unused component may oscillate if inputs and outputs are left open, thus generating noise and increasing power dissipation. To counteract this, inputs should be terminated in such a way that minimum power is consumed. Note that flip-flops which have both SET ($\overline{SET}$) and RESET ($\overline{RESET}$) terminals available represent a special case. One of these should be left open. However, if only one is available, it should be returned to ground.

3.6 – Generation of Logic "1"

In termination of unused inputs, a logic "1" level is sometimes required. This can be done by using the output of an inverting gate whose inputs are grounded. This is convenient if a gate exists on the board which is not being used. Another method is to use V_{CC} as a logic "1". This is acceptable only if the supply voltage can be

maintained at a voltage below that of the input voltage limit (5.5 V). Since spikes on power supplies can usually be expected, it is often wise to use a current limiting resistor. Assuming that the supply voltage will always be less than 7.0 volts and that inputs can withstand an avalanche current of 1.5 mA at 5.5 volts, the limiting resistor should be 1.0 kilohm or greater. This resistor must supply leakage current to inputs under normal operation, which limits the number of inputs that can be connected to a given resistor to 35 standard loads.

3.7 — Expander Inputs of AOI Gates

The expander inputs of AOI gates represent high-impedance nodes and are therefore susceptible to noise. In addition, capacitance at these points greatly increases propagation delay. Keeping leads short is an effective countermeasure for both these effects, but some degradation in speed must be expected if the inputs are used.

The data sheets for expandable AOI gates specify a maximum number of expanders which can be used with them without seriously affecting performance. One effect of adding expanders is to decrease operating speed. A more important restriction is the fact that leakage current across the expander nodes is also increased. This can reduce V_{OH} to a value below specification if too many expanders are used.

3.8 — Parallel Operation of Outputs

Theoretically, the AND-OR-INVERT function can be obtained by connecting outputs of two or more NAND gates together. This is feasible with MTTL if open-collector gates are used, but is not practical for active pull-up gates. The problem occurs when input conditions are such that one output would normally be high and another low. With the two outputs connected together, the result could be high, low, or somewhere in between. In any event, the current through two transistors may be high enough to cause failure.

Outputs of similar gates can usually be connected in parallel if corresponding inputs are also operated in parallel. Under dc conditions, the situation described in the previous paragraph would not exist. During switching, however, one gate may be faster than another, producing the same result for a few nanoseconds. This would increase the magnitude and duration of the current spike associated with switching and can also cause a discontinuity in the output waveform. This is particularly evident as the output voltage goes from high to low at reduced ambient temperatures. Under these conditions, the output fall time is normal until threshold potential is reached. The voltage level tends to remain at or near threshold for a period equivalent to the difference in propagation delays of the two gates. At the end of this period, the output voltage falls at a normal rate to V_{OL}.

The same discontinuity can occur as the output goes from low to high. In either case, the effects can be minimized by insuring that the gates connected in parallel are contained in the same package.

3.9 — Open-Collector Gates

Open-collector gates are intended for use in the "Implied-AND" configuration and to drive discrete components. Whenever such an output is used to drive other MTTL inputs, a pull-up resistor to V_{CC} should be used. Failure to do this creates a situation identical to leaving an unused input open (noise immunity is reduced). In addition, any passive pull-up element must be a compromise. The resistor value should be low enough to insure that required input leakage current is supplied, and high enough to represent a reasonable load current when the output is low. This is the purpose of the two equations in paragraph 2.9, item 3.

Since the output impedance of an open-collector gate is necessarily larger than that of an active pull-up gate, special precautions may be required in noisy environments. One recommendation is to locate the pull-up resistor close to the inputs being driven. Effectively, a negative-going signal (noise) coupled into the circuit at a gate input "sees" only the gate input impedance for a period of time equal to twice the propagation time along the line from the gate input to the current source. For optimum performance, this period should be much less than one gate delay. (Normal line propagation delay is $\approx$ 0.1 ns per inch.)

3.10 — Loading Factors

In order to complete a system, the designer must have knowledge of how many inputs can safely be driven by a given output. This information is provided by assigning an OUTPUT LOADING FACTOR to each output and an INPUT LOADING FACTOR to each input. In a system, the sum of the input loading factors of all inputs connected to a given output should not exceed the output loading factor. By following this simple rule, the designer can be assured that dc overloading conditions will not exist.

The input loading factor of a logic element is actually defined by two factors: (1) the amount of current that must be forced into an input to maintain an input voltage of 2.4 volts or greater, and (2) the amount of current that must be pulled out of the input to insure that an input voltage of 0.4 volt or less is maintained. These currents are designated as I_R (Reverse Current) and I_F (Forward Current) respectively. A unit load for an input corresponds to a reverse current of 40 μA and a forward current of 1.6 mA.

The output loading factor is also governed by two conditions: (1) the amount of current that may be sourced from an output in a high state while maintaining an output voltage of 2.4 volts or greater, and (2) the amount of current that may be forced into an output in a low state while maintaining an output voltage of 0.4 volt or less. These currents are designated as I_{OH} (output high-level current) and I_{OL} (output low-level current) respectively. In general, an MC7400 series component is specified with an output loading factor of 10 (corresponding to an I_{OH} of 10 I_R, or 400 μA, and an I_{OL} of 10 I_F, or 16 mA). There are exceptions to this as noted on the individual data sheets.

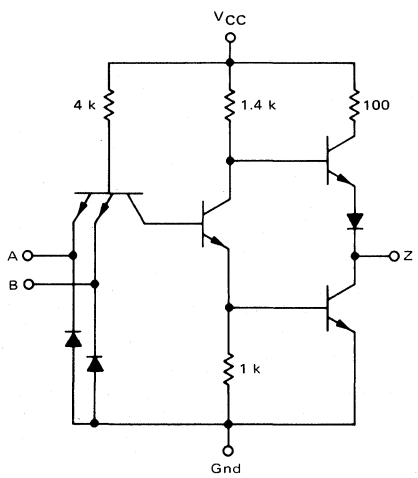
3.11 — Noise Immunity

In discussing loading factors, two voltages are noted. The 2.4-volt figure is designated as V_{OH} (output high-level voltage) while the 0.4 volt figure corresponds to V_{OL} (output low-level voltage). It is important to note that two different voltage levels are used at the inputs when the output characteristics are tested. Considering an inverter circuit, a logic "0" state input threshold voltage ($V_{th\ 0}$) is applied to the input during testing of output high-level characteristics (V_{OH} and I_{OH}). The value of $V_{th\ 0}$ is 0.8 volt. Thus, the dc value of a logic "0" input state (exclusive of noise) can be no greater than 0.4 volt (V_{OL}), yet MC5400/7400 series components recognize any voltage less than 0.8 volt as a logic "0". The dc noise immunity of the series is therefore 400 mV with the input in a logic "0" state. A similar comparison of $V_{th\ 1}$ to V_{OH} reveals that the components also exhibit 400 mV noise immunity in the logic "1" state.

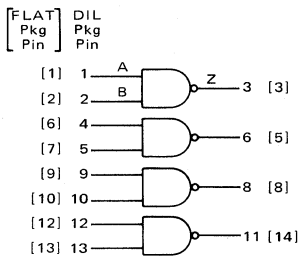
MC5400 • MC7400

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7400 only.

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



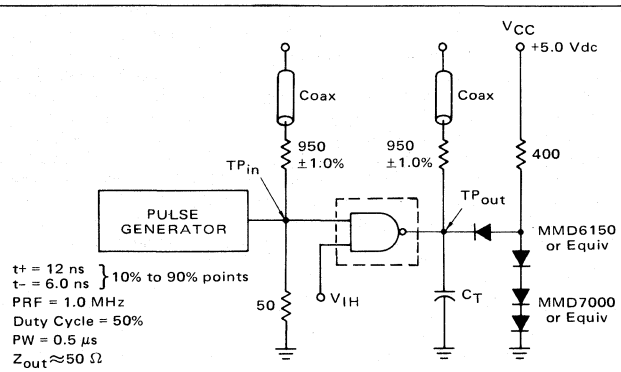
V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

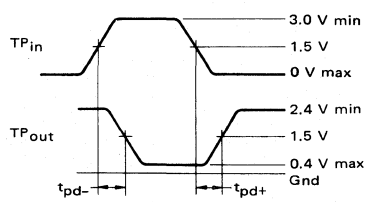


Positive Logic: $Z = \overline{A \bullet B}$
Negative Logic: $Z = \overline{A + B}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 10 ns typ

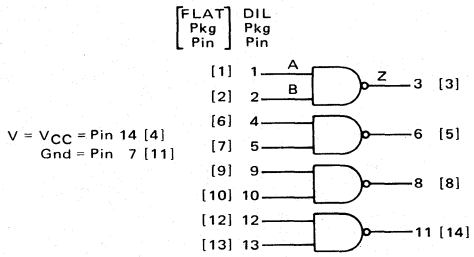
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
	mA		Volts										
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	
MC5400	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50	
MC7400	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25	Pin 7[11] is grounded for all tests in addition to the pins listed below:

Characteristic	Symbol	Pin Under Test	MC5400 Test Limits −55 to +125°C			MC7400 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										Gnd
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	
Input																					
Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	-	A	-	-	B	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	-	A	-	-	-	-	-	-	-	V	B*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	A	-	-	-	-	-	-	V	B*
Output																					
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	A,B	-	-	V	-	*
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	B	-	-	A	-	V	-	*
Short-Circuit Current	I_{SC}†	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B,Z*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	V	-	22	mAdc	-	22	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	V	*
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	All Inputs
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	-	B	-	-	-	-	-	V	-	-	*
Turn-Off Delay	t_{pd+}	A,Z	-	22**	ns	-	22**	ns	A	Z	-	B	-	-	-	-	-	V	-	-	*

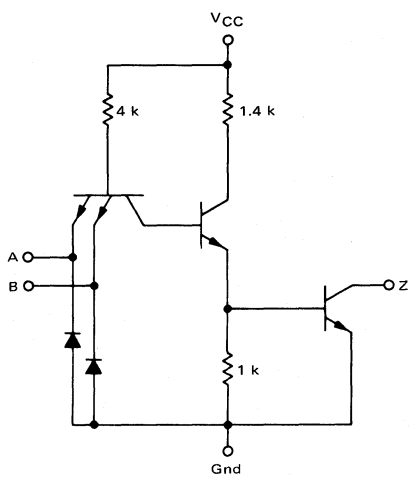
*Ground inputs to gates not under test.
**Tested only at 25° C.
†Only one output should be shorted at a time.

QUAD 2-INPUT "NAND" GATE
WITH OPEN COLLECTOR

MC5401 • MC7401

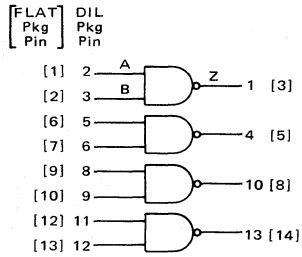
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7401 only.

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

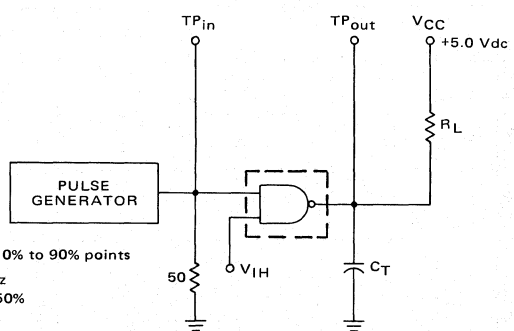
This device consists of four 2-input NAND gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.



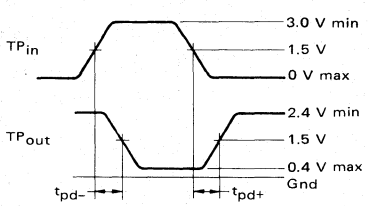
Positive Logic: $Z = \overline{A \bullet B}$
Negative Logic: $Z = \overline{A + B}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 35 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



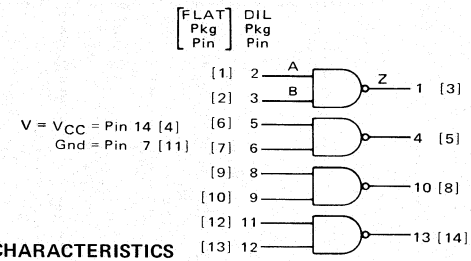
t+ = 12 ns
t- = 6.0 ns
} 10% to 90% points
PRF = 1.0 MHz
Duty Cycle = 50%
PW = 0.5 μs
$Z_{out} \approx 50\ \Omega$



R_L = 400 ohms for t_{pd-} test.
4.0 k ohms for t_{pd+} test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 megohm) must be used for tests.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
	mA	Volts											
	I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
MC5401	16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.50	5.50	
MC7401	16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.75	5.25	Pin 7[11] is grounded for all tests in addition to the pins listed below:

Characteristic	Symbol	Pin Under Test	MC5401 Test Limits −55 to +125°C Min	Max	Unit	MC7401 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	A	-	-	B	-	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	A	-	-	-	-	-	-	-	-	V	B*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	A	-	-	-	-	-	-	-	V	B*
Output																					
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	A,B	-	-	-	V	-	*
Output Leakage Current	I_{CEX}	Z	-	0.25	mAdc	-	0.25	mAdc	-	-	-	-	A	-	-	B	Z	-	V	-	*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	V	-	22	mAdc	-	22	mAdc	-	-	-	-	-	All Inputs	-	-	-	-	-	V	-
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B*
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	B	-	-	-	-	-	-	V	-	-	-
Turn-Off Delay	t_{pd+}	A,Z	-	45**	ns	-	45**	ns	A	Z	B	-	-	-	-	-	-	V	-	-	-

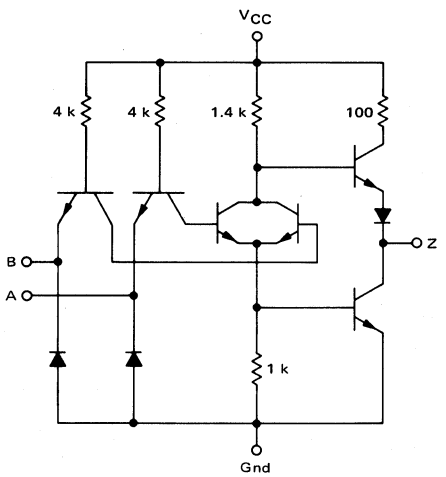
*Ground inputs to gates not under test.
**Tested only at 25°C.

MC5402 • MC7402

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7402 only.

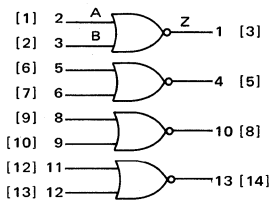
12

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

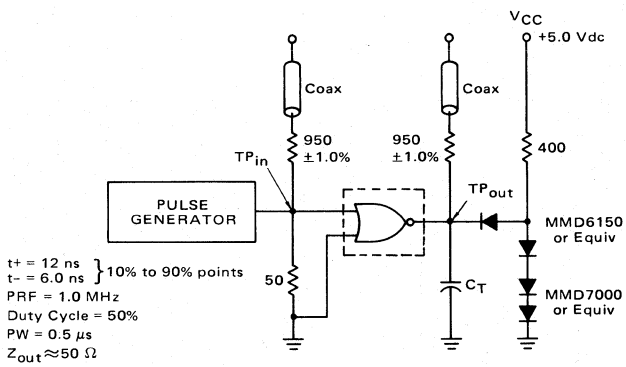
[FLAT Pkg Pin] DIL Pkg Pin

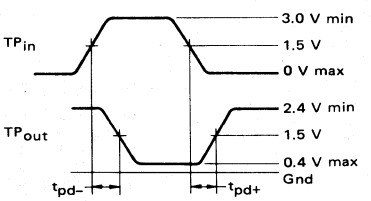


Positive Logic: $Z = \overline{A + B}$
Negative Logic: $Z = \overline{A \bullet B}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 10 ns typ

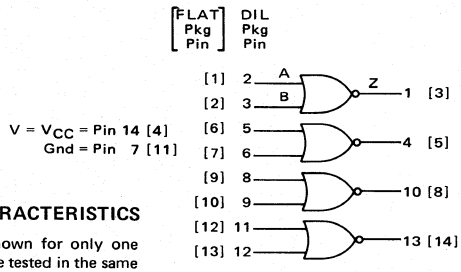
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA	Volts										
	I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	
MC5402	16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50	
MC7402	16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25	Pin 7[11] is grounded for all tests in addition to the pins listed below:

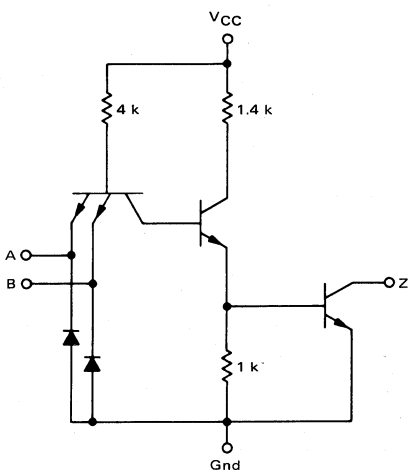
Characteristic	Symbol	Pin Under Test	MC5402 Test Limits −55 to +125°C			MC7402 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										Gnd
			Min	Max	Unit	Min	Max	Unit	I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	
Input																			
Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	A	-	-	B	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	A	-	-	-	-	-	-	-	V	B*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	A	-	-	-	-	-	-	V	B*
Output																			
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	A	-	-	V	-	B*
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	-	-	B	-	V	-	A*
Short-Circuit Current	I_{SC}†	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	V	Z,A,B*
Power Requirements (Total Device)																			
Power Supply Drain	I_{PDH}	V	-	27	mAdc	-	27	mAdc	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	16	mAdc	-	16	mAdc	-	-	-	-	-	-	-	-	-	-	V	A,B*
Switching Parameters									Pulse In	Pulse Out										
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	-	-	-	-	-	-	V	-	-	A*
Turn-Off Delay	t_{pd+}	A,Z	-	22**	ns	-	22**	ns	A	Z	-	-	-	-	-	-	V	-	-	A*

*Ground inputs to gates not under test.
**Tested only at 25°C.
†Only one output should be shorted at a time.

MC5403 • MC7403

Add Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 607) MC7403 only.

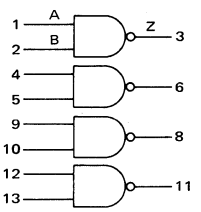
CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



V_{CC} = Pin 14
Gnd = Pin 7

Device available only in dual in-line package.

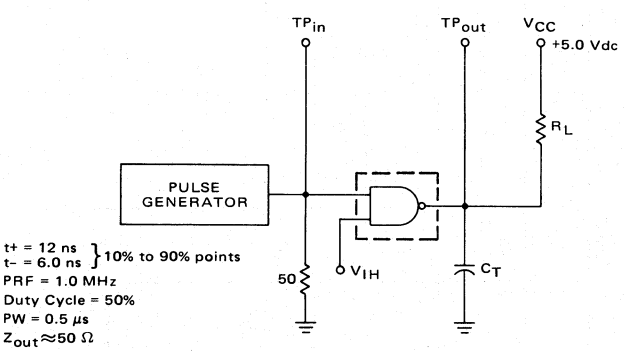
This device consists of four 2-input NAND gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.



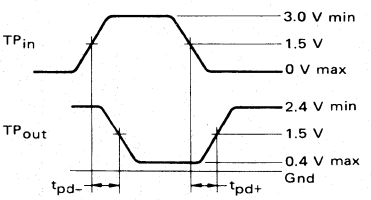
Positive Logic: $Z = \overline{A \bullet B}$
Negative Logic: $Z = \overline{A + B}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 35 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



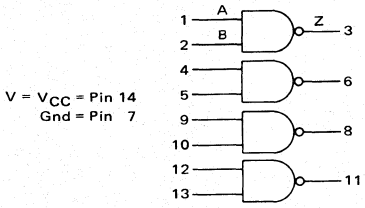
t+ = 12 ns
t- = 6.0 ns } 10% to 90% points
PRF = 1.0 MHz
Duty Cycle = 50%
PW = 0.5 μs
$Z_{out} \approx 50\ \Omega$



R_L = 400 ohms for t_{pd-} test.
4.0 k ohms for t_{pd+} test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 megohm) must be used for tests.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

									TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
									mA	Volts											
									I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
									MC5403 16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.50	5.50	
									MC7403 16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.75	5.25	Pin 7 is grounded for all tests in addition to the pins listed below:
Characteristic	Symbol	Pin Under Test	MC5403 Test Limits −55 to +125°C Min	Max	Unit	MC7403 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	A	-	-	B	-	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	A	-	-	-	-	-	-	-	-	V	B*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	A	-	-	-	-	-	-	-	V	B*
Output Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	A,B	-	-	-	V	-	*
Output Leakage Current	I_{CEX}	Z	-	0.25	mAdc	-	0.25	mAdc	-	-	-	-	A	-	-	B	Z	-	V	-	*
Power Requirements (Total Device) Power Supply Drain	I_{PDH}	V	-	22	mAdc	-	22	mAdc	-	-	-	-	-	All Inputs	-	-	-	-	-	V	-
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B*
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	B	-	-	-	-	-	-	V	-	-	-
Turn-Off Delay	t_{pd+}	A,Z	-	45**	ns	-	45**	ns	A	Z	B	-	-	-	-	-	-	V	-	-	-

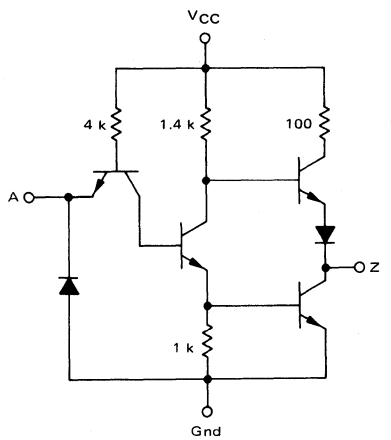
*Ground inputs to gates not under test.
**Tested only at 25°C.

HEX INVERTER

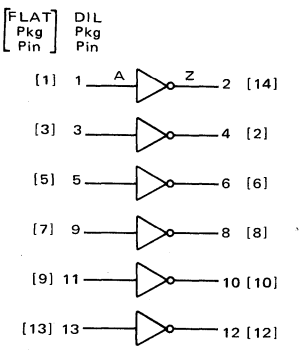
MC5404 • MC7404

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7404 only.

CIRCUIT SCHEMATIC
1/6 OF CIRCUIT SHOWN



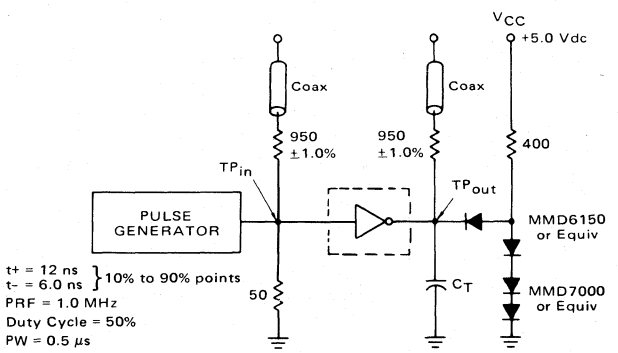
V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

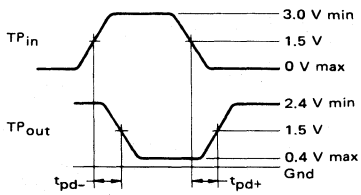


Positive Logic: $Z = \overline{A}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 60 mW typ/pkg
Propagation Delay Time = 13 ns typ

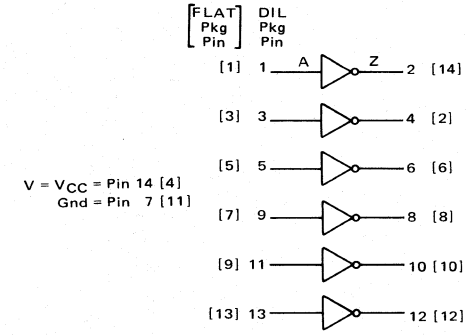
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}
MC5404	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
MC7404	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25

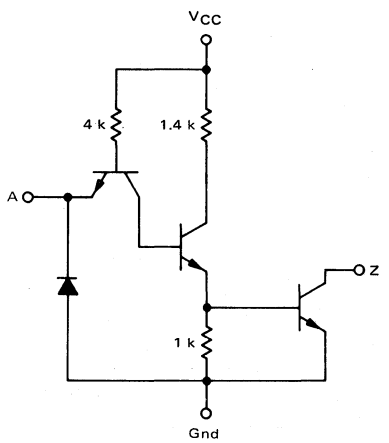
Characteristic	Symbol	Pin Under Test	MC5404 Test Limits −55 to +125°C			MC7404 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											Pin 7[11] is grounded for all tests in addition to the pins listed below:
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																				
Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	-	A	-	-	-	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	-	A	-	-	-	-	-	-	-	V	*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	A	-	-	-	-	-	-	V	*
Output																				
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	A	-	-	V	-	*
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	-	-	-	A	-	V	-	*
Short-Circuit Current	I_{SC}†	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,Z*
Power Requirements (Total Device)																				
Power Supply Drain	I_{PDH}	V	-	33	mAdc	-	33	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	12	mAdc	-	12	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	All Inputs
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	-	-	-	-	-	-	-	V	-	-	*
Turn-Off Delay	t_{pd+}	A,Z	-	22**	ns	-	22**	ns	A	Z	-	-	-	-	-	-	-	V	-	-	*

*Ground inputs to inverters not under test.
**Tested only at 25°C.
†Only one output should be shorted at a time.

MC5405 • MC7405

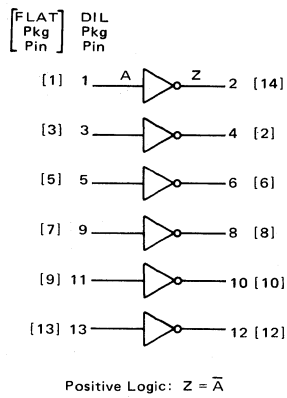
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7405 only.

CIRCUIT SCHEMATIC
1/6 OF CIRCUIT SHOWN



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

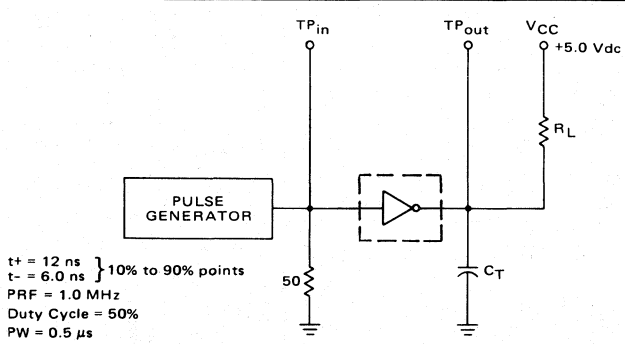
This device consists of six independent inverting gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.

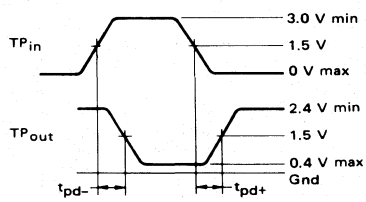


Positive Logic: $Z = \overline{A}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 60 mW typ/pkg
Propagation Delay Time = 35 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



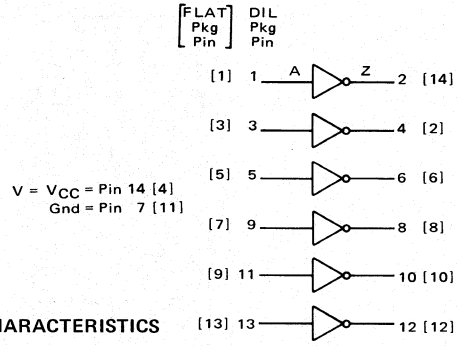


t+ = 12 ns
t- = 6.0 ns } 10% to 90% points
PRF = 1.0 MHz
Duty Cycle = 50%
PW = 0.5 μs
$Z_{out} \approx 50\ \Omega$

R_L = 400 ohms for t_{pd-} test.
4.0 k ohms for t_{pd+} test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 megohm) must be used for tests.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC5405 Test Limits −55 to +125°C Min	MC5405 Test Limits −55 to +125°C Max	MC5405 Test Limits −55 to +125°C Unit	MC7405 Test Limits 0 to +70°C Min	MC7405 Test Limits 0 to +70°C Max	MC7405 Test Limits 0 to +70°C Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	V_{CEX}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Pin 7[11] is grounded for all tests in addition to the pins listed below: Gnd
Input																					
Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	-	A	-	-	-	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	-	A	-	-	-	-	-	-	-	V	*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	A	-	-	-	-	-	-	V	*
Output																					
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	A	-	-	V	-	*
Output Leakage Current	I_{CEX}	Z	0.25	-	mAdc	0.25	-	mAdc	-	Z	-	-	-	-	-	-	A	-	V	-	*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	V	-	33**	mAdc	-	33**	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	12**	mAdc	-	12**	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	All Inputs
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	-	-	-	-	-	-	-	V	-	-	*
Turn-Off Delay	t_{pd+}	A,Z	-	55**	ns	-	55**	ns	A	Z	-	-	-	-	-	-	-	V	-	-	*

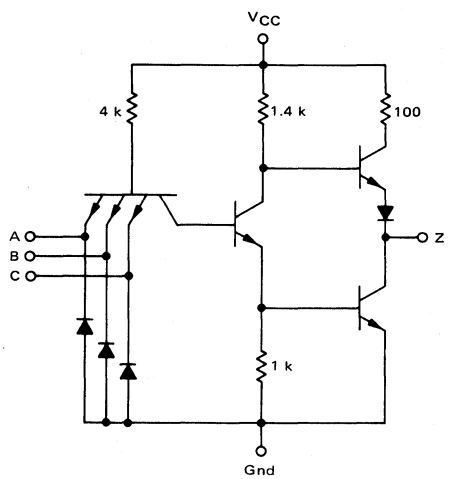
TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
mA	Volts										
I_{OL}	V_{CEX}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}
MC5405 16	5.5	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
MC7405 16	5.5	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25

*Ground inputs to inverters not under test.
**Tested only at 25°C.

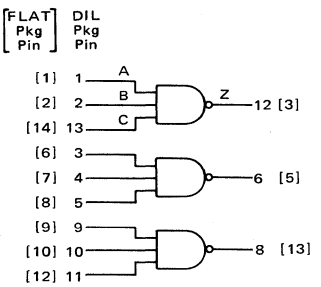
MC5410 • MC7410

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7410 only.

CIRCUIT SCHEMATIC
1/3 OF CIRCUIT SHOWN



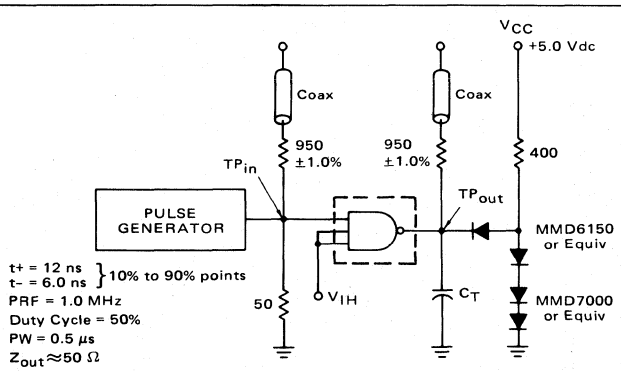
V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

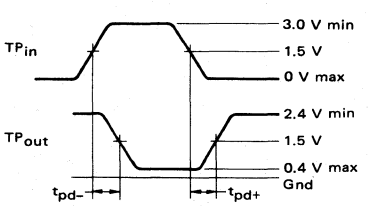


Positive Logic: $Z = \overline{A \bullet B \bullet C}$
Negative Logic: $Z = \overline{A + B + C}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 30 mW typ/pkg
Propagation Delay Time = 10 ns typ

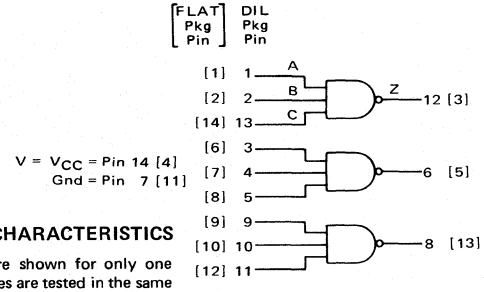
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

Characteristic	Symbol	Pin Under Test	MC5410 Test Limits −55 to +125°C Min	MC5410 Test Limits −55 to +125°C Max	MC5410 Test Limits −55 to +125°C Unit	MC7410 Test Limits 0 to +70°C Min	MC7410 Test Limits 0 to +70°C Max	MC7410 Test Limits 0 to +70°C Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_{IHH} (Volts)	V_{R1} (Volts)	V_{R2} (Volts)	$V_{th\,1}$ (Volts)	$V_{th\,0}$ (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	Gnd
Input																					
Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	-	A	-	-	B,C	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	-	A	-	-	-	-	-	-	-	V	B,C*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	A	-	-	-	-	-	-	V	B,C*
Output																					
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	A,B,C	-	-	V	-	*
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	B,C	-	-	A	-	V	-	*
Short-Circuit Current	I_{SC}†	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B,C*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	V	-	16.5	mAdc	-	16.5	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	6.0	mAdc	-	6.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B,C*
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	-	B,C	-	-	-	-	-	V	-	-	*
Turn-Off Delay	t_{pd+}	A,Z	-	22**	ns	-	22**	ns	A	Z	-	B,C	-	-	-	-	-	V	-	-	*

TEST CURRENT/VOLTAGE VALUES (All Temperatures)

	I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_{IHH} (Volts)	V_{R1} (Volts)	V_{R2} (Volts)	$V_{th\,1}$ (Volts)	$V_{th\,0}$ (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)
MC5410	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
MC7410	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25

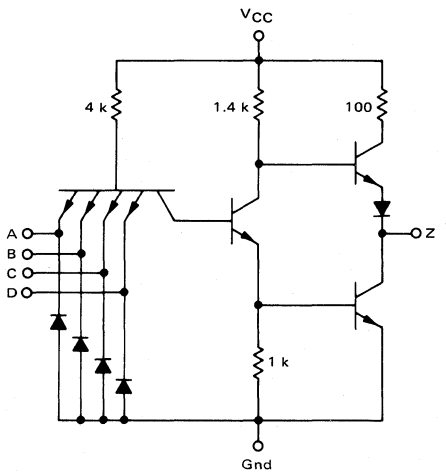
Pin 7[14] is grounded for all tests in addition to the pins listed below:

*Ground inputs to gates not under test.
**Tested only at 25°C.
†Only one output should be shorted at a time.

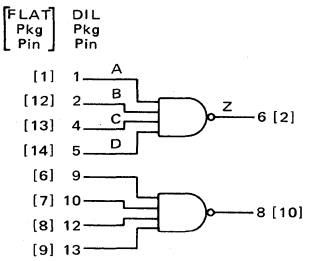
MC5420 • MC7420

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7420 only.

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



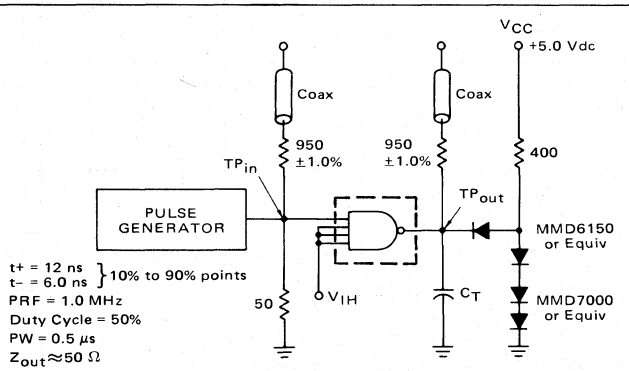
V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

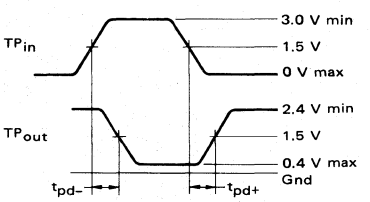


Positive Logic: $Z = \overline{A \bullet B \bullet C \bullet D}$
Negative Logic: $Z = \overline{A + B + C + D}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 20 mW typ/pkg
Propagation Delay Time = 10 ns typ

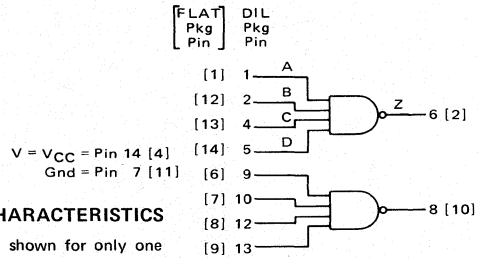
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}
MC5420	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
MC7420	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25

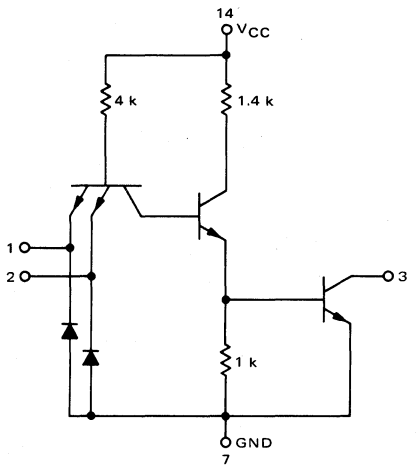
Characteristic	Symbol	Pin Under Test	MC5420 Test Limits −55 to +125°C			MC7420 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											Pin 7[11] is grounded for all tests in addition to the pins listed below:
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	-	A	-	-	B,C,D	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	-	A	-	-	-	-	-	-	-	V	B,C,D*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	A	-	-	-	-	-	-	V	B,C,D*
Output																					
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	A,B,C,D	-	-	V	-	*
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	B,C,D	-	-	A	-	V	-	*
Short-Circuit Current	I_{SC}†	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	All Inputs
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	V	-	11	mAdc	-	11	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	4.0	mAdc	-	4.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B,C,D*
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	-	B,C,D	-	-	-	-	-	V	-	-	*
Turn-Off Delay	t_{pd+}	A,Z	-	22**	ns	-	22**	ns	A	Z	-	B,C,D	-	-	-	-	-	V	-	-	*

*Ground inputs to gate not under test.
**Tested only at 25°C.
†Only one output should be shorted at a time.

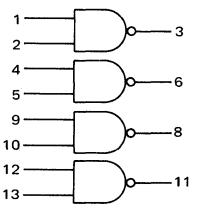
QUAD 2-INPUT INTERFACE
"NAND" GATE

MC5426L*
MC7426P,L*

1/4 OF CIRCUIT SHOWN



This device features high-output voltage ratings for use as an interface circuit with 12 volt systems, such as low threshold voltage MOS logic circuits. The output is rated at 15 volts, however, V_{CC} is connected to the standard 5 volt source. The output transistor has a 16 milliamp sink capability at an output voltage of 0.4 volt maximum, thus allowing high fan-out drive capability while maintaining the nominal power dissipation of the standard gate.



Positive Logic: $3 = \overline{1 \cdot 2}$

Negative Logic: $3 = \overline{1 + 2}$

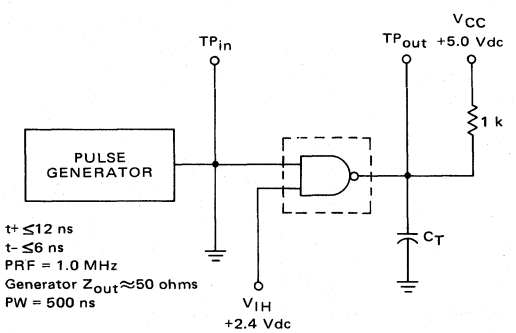
Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 40 mW typ/pkg

Propagation Delay Time = 17 ns typ

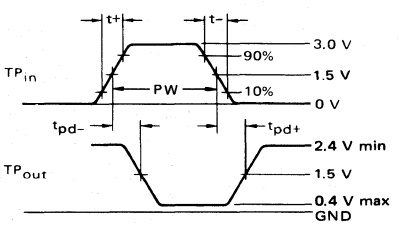
*L suffix = TO-116 ceramic package (Case 632)
P suffix = TO-116 plastic package (Case 605)
See General Information section for package outline dimensions.

VOLTAGE WAVEFORMS AND DEFINITIONS



t+ ≤12 ns
t- ≤6 ns
PRF = 1.0 MHz
Generator $Z_{out} \approx 50$ ohms
PW = 500 ns

SWITCHING TIME TEST CIRCUIT

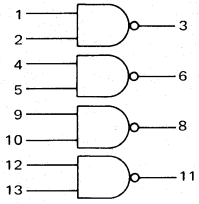


C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 megohm) must be used for tests.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



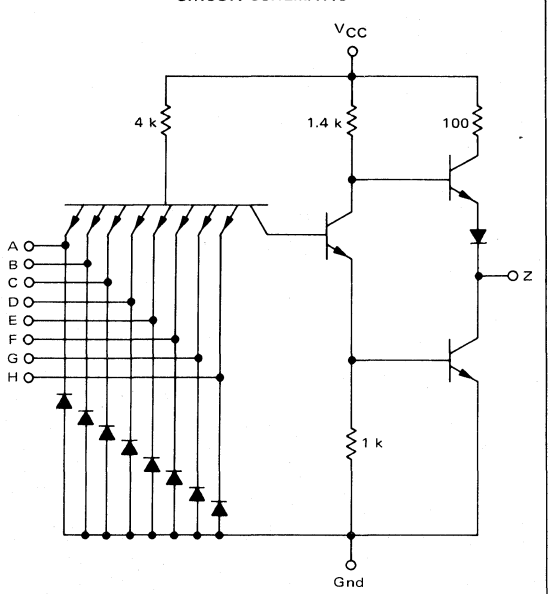
									TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
									mA		Volts										
									I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{R1}	V_{R2}	$V_{th\ 1}$	$V_{th\ 0}$	V_{OH}	V_{CC}	V_{CCL}	V_{CCH}	
								MC5426	16	1	0.4	2.4	4.5	5.5	2.0	0.8	12	5.0	4.5	5.5	
								MC7426	16	1	0.4	2.4	4.5	5.5	2.0	0.8	12	5.0	4.75	5.25	
			MC5426 Test Limits -55 to +125°C			MC7426 Test Limits 0 to 70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{R1}	V_{R2}	$V_{th\ 1}$	$V_{th\ 0}$	V_{OH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_F	1	–	-1.6	mAdc	–	-1.6	mAdc	–	–	1	–	2	–	–	–	–	–	–	14	7*
Leakage Current	I_{R1}	1	–	40	µAdc	–	40	µAdc	–	–	–	1	–	–	–	–	–	–	–	14	2,7*
	I_{R2}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	1	–	–	–	–	–	14	2,7*
Output																					
Output Voltage	V_{OL}	3	–	0.4	Vdc	–	0.4	Vdc	3	–	–	–	–	–	1,2	–	–	–	14	–	7*
	V_{OH}	3	15	–	Vdc	15	–	Vdc	–	3	–	–	–	–	–	2	–	–	1,14	–	7*
Output Current	I_{OH}	3	–	50	µAdc	–	50	µAdc	–	–	–	–	–	–	–	2	3	–	1,14	–	7*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	14	–	22	mAdc	–	22	mAdc	–	–	–	–	–	–	–	–	–	12	–	14	7
	I_{PDL}	14	–	8.0	mAdc	–	8.0	mAdc	–	–	–	–	–	–	–	–	–	–	–	14	1,4,7,9,12
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1,3	–	17**	ns	–	17**	ns	1	3	–	2	–	–	–	–	–	14	–	–	7
Turn-Off Delay	t_{pd+}	1,3	–	24**	ns	–	24**	ns	1	3	–	2	–	–	–	–	–	14	–	–	7

*Ground inputs to gates not under test.
**Tested only at 25°C.

MC5430 • MC7430

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7430 only.

CIRCUIT SCHEMATIC



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

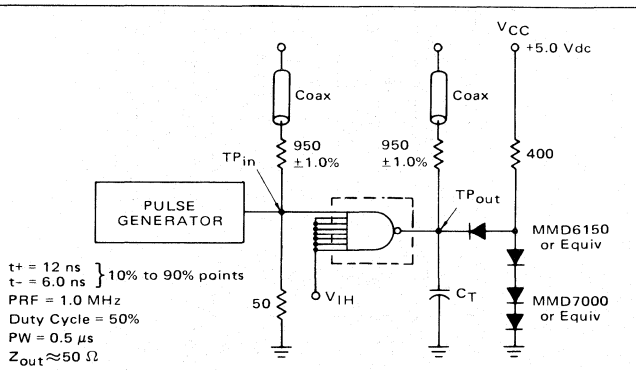
[FLAT Pkg Pin]	DIL Pkg Pin	
[2]	1	A
[3]	2	B
[5]	3	C
[6]	4	D
[7]	5	E
[8]	6	F
[9]	11	G
[10]	12	H

Z = 8 [12]

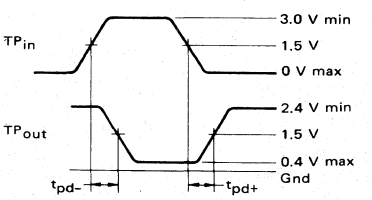
Positive Logic:
$Z = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}$
Negative Logic:
$Z = \overline{A + B + C + D + E + F + G + H}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 10 mW typ/pkg
Propagation Delay Time = 10 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



t+ = 12 ns
t- = 6.0 ns } 10% to 90% points
PRF = 1.0 MHz
Duty Cycle = 50%
PW = 0.5 μs
$Z_{out} \approx 50\ \Omega$

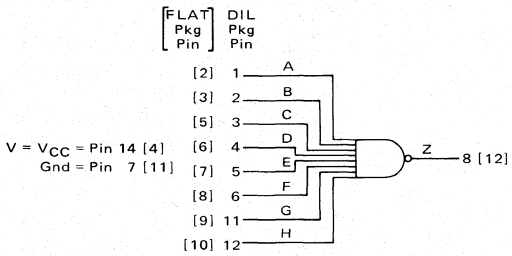


C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input. To complete testing, sequence through remaining inputs in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}
MC5430	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
MC7430	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5430 Test Limits −55 to +125°C Min	Max	Unit	MC7430 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Pin 7[11] is grounded for all tests in addition to the pins listed below: Gnd
Input																					
Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	-	A	-	-	B,C,D,E, F,G,H	-	-	-	-	-	V	-
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	-	A	-	-	-	-	-	-	-	V	B,C,D,E,F,G,H
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	A	-	-	-	-	-	-	V	B,C,D,E,F,G,H
Output																					
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	All Inputs	-	-	V	-	-
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	B,C,D,E, F,G,H	-	-	A	-	V	-	-
Short-Circuit Current	I_{SC}†	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	All Inputs, Z
Power Requirements																					
Power Supply Drain	I_{PDH}	V	-	6.0	mAdc	-	6.0	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	2.0	mAdc	-	2.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	All Inputs
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15*	ns	-	15*	ns	A	Z	-	B,C,D,E, F,G,H	-	-	-	-	-	V	-	-	-
Turn-Off Delay	t_{pd+}	A,Z	-	22*	ns	-	22*	ns	A	Z	-	B,C,D,E, F,G,H	-	-	-	-	-	V	-	-	-

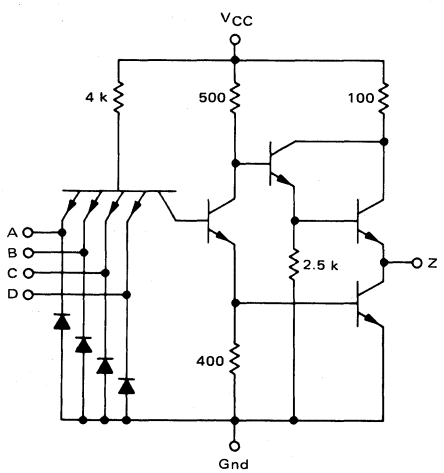
*Tested only at 25°C.
†Only one output should be shorted at a time.

DUAL 4-INPUT "NAND" BUFFER

MC5440 • MC7440

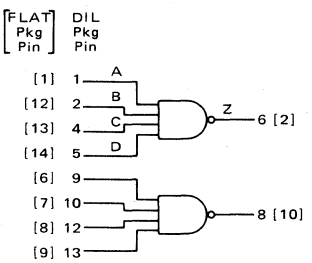
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7440 only.

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

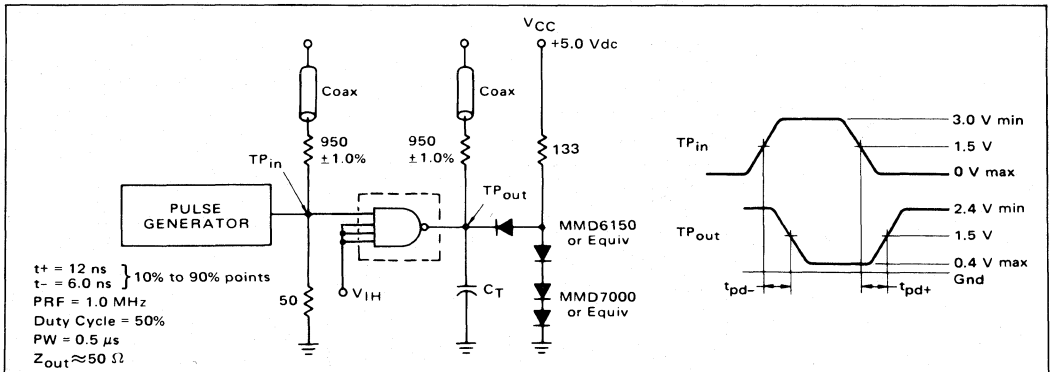
This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (30).



Positive Logic: $Z = \overline{A \bullet B \bullet C \bullet D}$
Negative Logic: $Z = \overline{A + B + C + D}$

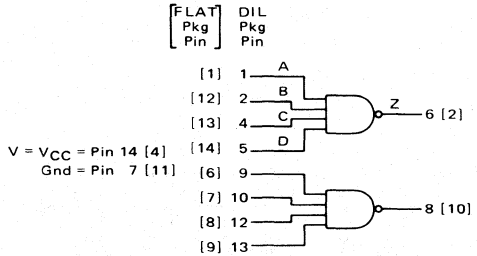
Input Loading Factor = 1
Output Loading Factor = 30
Total Power Dissipation = 50 mW typ/pkg
Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}
MC5440	48	-1.2	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
MC7440	48	-1.2	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25

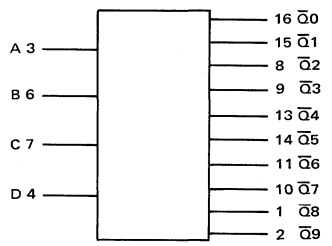
Characteristic	Symbol	Pin Under Test	MC5440 Test Limits −55 to +125°C Min	MC5440 Test Limits −55 to +125°C Max	MC5440 Test Limits −55 to +125°C Unit	MC7440 Test Limits 0 to +70°C Min	MC7440 Test Limits 0 to +70°C Max	MC7440 Test Limits 0 to +70°C Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Pin 7[11] is grounded for all tests in addition to the pins listed below: Gnd
Input																					
Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	-	A	-	-	B,C,D	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	-	A	-	-	-	-	-	-	-	V	B,C,D*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	A	-	-	-	-	-	-	V	B,C,D*
Output																					
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	A,B,C,D	-	-	V	-	*
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	B,C,D	-	-	A	-	V	-	*
Short-Circuit Current	I_{SC}†	Z	-20	-70	mAdc	-18	-70	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B,D,D,Z*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	V	-	27	mAdc	-	27	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B,C,D*
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	-	B,C,D	-	-	-	-	-	V	-	-	*
Turn-Off Delay	t_{pd+}	A,Z	-	22**	ns	-	22**	ns	A	Z	-	B,C,D	-	-	-	-	-	V	-	-	*

*Ground inputs to gate not under test.
**Tested only at 25°C.
†Only one output should be shorted at a time.

BCD-TO-DECIMAL DECODER
AND HIGH-LEVEL DRIVER

MC7441AL,P*

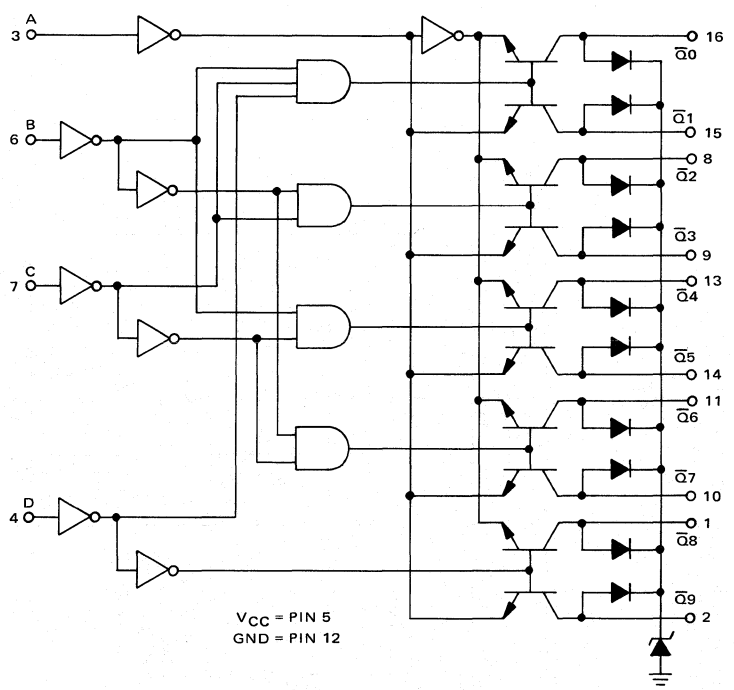
This monolithic device is a BCD to one-of-ten decoder with high-level outputs capable of driving gas-filled cold-cathode indicator tubes or other devices requiring high-voltage drivers. In a typical application, this device would be driven by the MC7490 decade counter through the MC7475 quad bistable latch. The outputs are guaranteed to operate at 55 volts with a maximum of 200 μA leakage current. The outputs of this device are protected by zener diodes to eliminate the possibility of oscillation due to the breakdown of the output devices.



Input Loading Factor = 1
Total Power Dissipation = 105 mW typ/pkg

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1



*L suffix = 16-pin ceramic package (Case 620).
P suffix = 16-pin plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only the A input and one output. To complete testing, sequence through the remaining inputs and outputs as shown in the truth table.

						TEST CURRENT / VOLTAGE VALUES (All Temperatures)										
						mA	Volts									
						I_{on}	V_{IL}	V_{IH}	V_{IHH}	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCL}	V_{CCH}	
						7.0	0.4	2.4	5.5	2.0	0.8	55	5.0	4.75	5.25	
Characteristic	Symbol	Pin Under Test	MC7441A Test Limits 0 to +70°C			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:										
			Min	Max	Unit	I_{on}	V_{IL}	V_{IH}	V_{IHH}	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_F	3	-	-1.6	mAdc	-	3	-	-	-	-	-	-	-	5	12
Leakage Current	I_{R1}	3	-	40	μAdc	-	-	3	-	-	-	-	-	-	5	12
	I_{R2}	3	-	1.0	mAdc	-	-	-	3	-	-	-	-	-	5	12
Output Output Voltage	V_{OL}	1	-	2.5	Vdc	1	-	-	-	4	3,6,7	-	-	5	-	12
Output Leakage Current	I_{OLK}	1	-	200	μAdc	-	-	-	-	-	3,4,6,7	1	-	5	-	12
Power Requirements (Total Device) Power Supply Drain	I_{PD}	5	-	32	mAdc	-	-	-	-	-	-	-	5	-	-	4,12

BCD-TO-DECIMAL DECODER

MC5442L* • MC7442L,P*

EXCESS THREE-TO-DECIMAL DECODER

MC5443L* • MC7443L,P*

EXCESS THREE GRAY-TO-DECIMAL DECODER

MC5444L* • MC7444L,P*

Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 140 mW typ/pkg

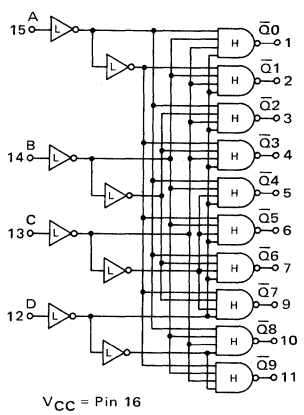
Propagation Delay Time:
2 Logic Levels = 22 ns typ
3 Logic Levels = 23 ns typ

DC Noise Margin = 1.0 V typ

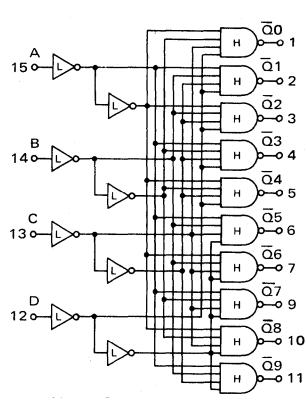
These devices decode four-bit BCD, Excess 3, or Excess 3 Gray inputs to select one-of-ten outputs. The selected output is in the logic "0" state, while all other outputs are in the logic "1" state. Full decoding of all valid input logic ensures that outputs remain off for any invalid input condition.

These devices are useful in memory selection, industrial control, and data routing applications.

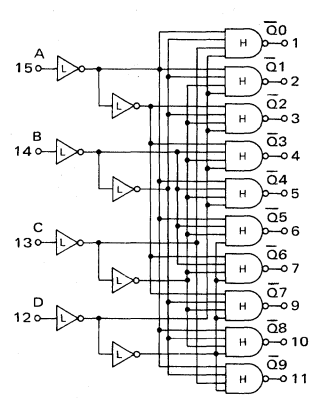
MC5442/MC7442



MC5443/MC7443



MC5444/MC7444



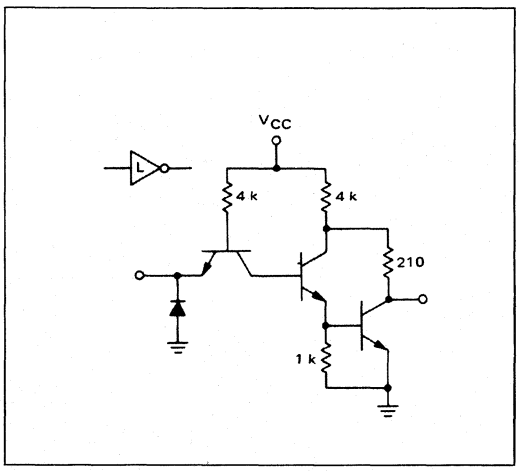
These decoders are constructed using low-level inverters and high-level NAND gates interconnected as shown by the logic diagrams. The inverter and gate schematics appear on the next page of this data sheet.

MC5442/MC7442 BCD INPUT				MC5443/MC7443 EXCESS 3 INPUT				MC5444/MC7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	0	1	0	0	0	1	1	0	1	1	1	1	1	1	1	1	0	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

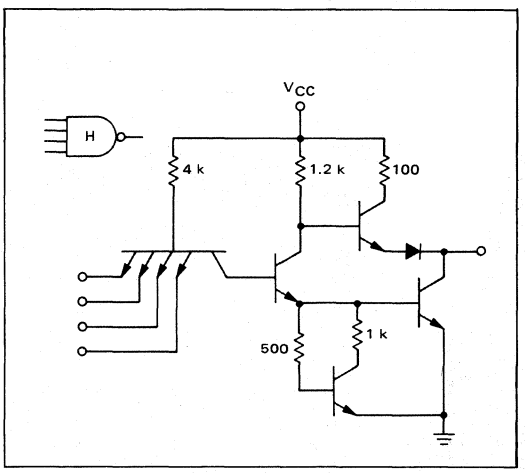
*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

CIRCUIT SCHEMATICS

LOW-LEVEL INVERTER



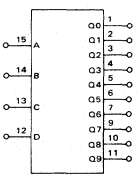
HIGH-LEVEL "NAND" GATE



MC5442/MC7442

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner according to the truth table. Additionally, test all input-output combinations according to the truth table.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA			Volts							
	I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	
MC5442	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.5	5.5	
MC7442	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.75	5.25	

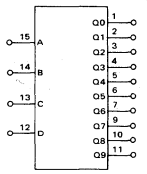
Characteristic	Symbol	Pin Under Test	MC5442 Test Limits -55 to +125°C			MC7442 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										Gnd
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	
Input																			
Forward Current	I_F	12	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	12	–	–	–	–	–	16	8
Leakage Current	I_R	12	–	40	μAdc	–	40	μAdc	–	–	–	–	12	–	–	–	–	16	8
Breakdown Voltage	BV_{in}	12	5.5	–	Vdc	5.5	–	Vdc	–	–	12	–	–	–	–	–	–	16	8
Output																			
Output Voltage	V_{OL}	1	–	0.4	Vdc	–	0.4	Vdc	1	–	–	–	–	–	12,13,14,15	–	16	–	8
	V_{OH}	1	2.4	–	Vdc	2.4	–	Vdc	–	1	–	–	–	15	12,13,14	–	16	–	8
Short-Circuit Current	I_{SC}	1	-20	-55	mAdc	-18	-55	mAdc	–	–	–	–	–	12,14	13,15	–	–	16	1,8
Power Requirements (Total Device)																			
Power Supply Drain	I_{PD}	16	–	41*	mAdc	–	56*	mAdc	–	–	–	–	–	–	–	16	–	–	8,12,13,14,15
Switching Parameters									Pulse In	Pulse Out									
Two Logic Levels																			
Turn-On Delay	t_{pd-2}	15,1	10*	30*	ns	10*	30*	ns	15	1	–	–	–	–	–	16	–	–	8,12,13,14
Turn-Off Delay	t_{pd+2}	15,1	10*	25*	ns	10*	25*	ns	15	1	–	–	–	–	–	16	–	–	8,12,13,14
Three Logic Levels																			
Turn-On Delay	t_{pd-3}	15,2	–	35*	ns	–	35*	ns	15	2	–	–	–	–	–	16	–	–	8,12,13,14
Turn-Off Delay	t_{pd+3}	15,2	–	35*	ns	–	35*	ns	15	2	–	–	–	–	–	16	–	–	8,12,13,14

*Tested only at 25°C.

MC5443/MC7443

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner according to the truth table. Additionally, test all input-output combinations according to the truth table.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA			Volts							
	I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC5443	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.5	5.5	2.5
MC7443	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.75	5.25	2.5

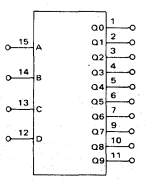
Characteristic	Symbol	Pin Under Test	MC5443 Test Limits -55 to +125°C Min	Max	Unit	MC7443 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																				
Forward Current	I_F	12	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	12	–	–	–	–	–	16	–	8
Leakage Current	I_R	12	–	40	μAdc	–	40	μAdc	–	–	–	–	12	–	–	–	–	16	–	8
Breakdown Voltage	BV_{in}	12	5.5	–	Vdc	5.5	–	Vdc	–	–	12	–	–	–	–	–	–	16	–	8
Output																				
Output Voltage	V_{OL}	1	–	0.4	Vdc	–	0.4	Vdc	1	–	–	–	–	14,15	12,13	–	16	–	–	8
	V_{OH}	1	2.4	–	Vdc	2.4	–	Vdc	–	1	–	–	–	13	12,14,15	–	16	–	–	8
Short-Circuit Current	I_{SC}	1	-20	-55	mAdc	-18	-55	mAdc	–	–	–	–	–	12,13,14	15	–	–	16	–	1,8
Power Requirements (Total Device)																				
Power Supply Drain	I_{PD}	16	–	41*	mAdc	–	56*	mAdc	–	–	–	–	–	–	–	16	–	–	–	8,12,13,14,15
Switching Parameters									Pulse In	Pulse Out										
Two Logic Levels Turn-On Delay	t_{pd-2}	15,2	10*	30*	ns	10*	30*	ns	15	2	–	–	–	–	–	16	–	–	13	8,12,14
Turn-Off Delay	t_{pd+2}	15,2	10*	25*	ns	10*	25*	ns	15	2	–	–	–	–	–	16	–	–	13	8,12,14
Three Logic Levels Turn-On Delay	t_{pd-3}	15,3	–	35*	ns	–	35*	ns	15	3	–	–	–	–	–	16	–	–	13	8,12,14
Turn-Off Delay	t_{pd+3}	15,3	–	35*	ns	–	35*	ns	15	3	–	–	–	–	–	16	–	–	13	8,12,14

*Tested only at 25°C.

MC5444/MC7444

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner according to the truth table. Additionally, test all input-output combinations according to the truth table.

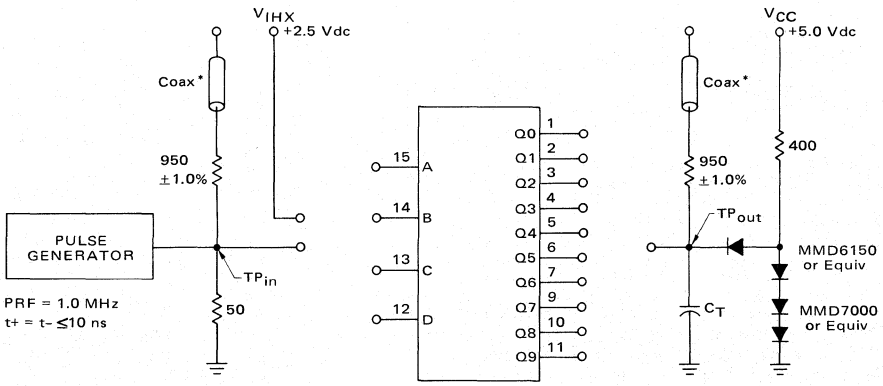


	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA			Volts							
	I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC5444	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.5	5.5	2.5
MC7444	16	-0.4	1.0	0.4	2.4	2.0	0.8	5.0	4.75	5.25	2.5

Characteristic	Symbol	Pin Under Test	MC5444 Test Limits -55 to +125°C Min	Max	Unit	MC7444 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_F	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																				
Forward Current	I_F	12	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	12	–	–	–	–	–	16	–	8
Leakage Current	I_R	12	–	40	μAdc	–	40	μAdc	–	–	–	–	12	–	–	–	–	16	–	8
Breakdown Voltage	BV_{in}	12	5.5	–	Vdc	5.5	–	Vdc	–	–	12	–	–	–	–	–	–	16	–	8
Output																				
Output Voltage	V_{OL}	1	–	0.4	Vdc	–	0.4	Vdc	1	–	–	–	–	14	12,13,15	–	16	–	–	8
	V_{OH}	1	2.4	–	Vdc	2.4	–	Vdc	–	1	–	–	–	13,14	12,15	–	16	–	–	8
Short-Circuit Current	I_{SC}	1	-20	-55	mAdc	-18	-55	mAdc	–	–	–	–	–	–	12,13,14,15	–	–	16	–	1,8
Power Requirements (Total Device)																				
Power Supply Drain	I_{PD}	16	–	41*	mAdc	–	56*	mAdc	–	–	–	–	–	–	–	16	–	–	–	8,12,13,14,15
Switching Parameters									Pulse In	Pulse Out										
Two Logic Levels Turn-On Delay	t_{pd-2}	13,1	10*	30*	ns	10*	30*	ns	13	1	–	–	–	–	–	16	–	–	14	8,12,15
Turn-Off Delay	t_{pd+2}	13,1	10*	25*	ns	10*	25*	ns	13	1	–	–	–	–	–	16	–	–	14	8,12,15
Three Logic Levels Turn-On Delay	t_{pd-3}	13,2	–	35*	ns	–	35*	ns	13	2	–	–	–	–	–	16	–	–	14	8,12,15
Turn-Off Delay	t_{pd+3}	13,2	–	35*	ns	–	35*	ns	13	2	–	–	–	–	–	16	–	–	14	8,12,15

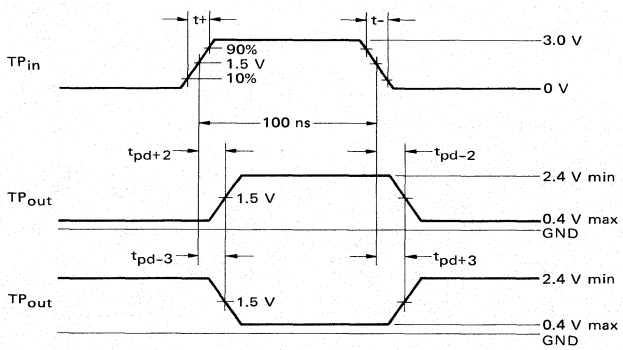
*Tested only at 25°C.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



TYPICAL APPLICATIONS

Two MC5442/7442 decoders may be used to perform 4-line to 16-line decoding. Data inputs A, B, and C are paralleled to the two decoders, while input D is applied to one decoder and $\overline{D}$ to the other. (See Figure 1.)

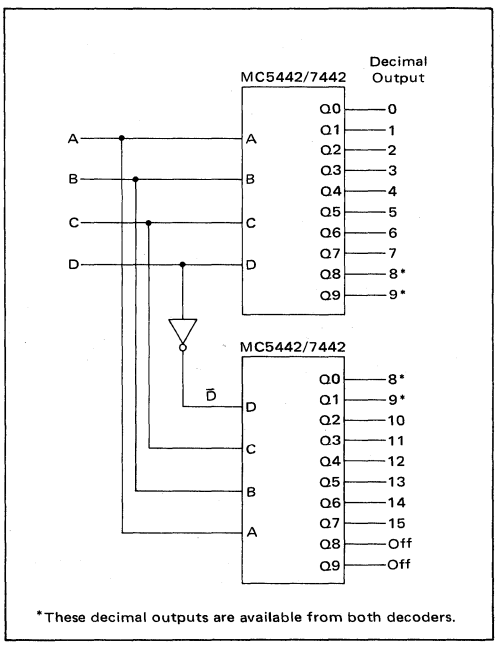
The excess 3 code is similar to the BCD code except that 3 is added to each digit before coding. This code has the advantage of being self-complementing. If all zeros in a BCD number are changed to ones and all ones are changed to zeros, the nines complement of the decimal number is obtained. The ability to obtain the nines complement can reduce the hardware necessary to perform subtraction. (See Figure 2.)

All Gray codes have one basic characteristic in common. As the code is advanced from any number to the next, only one bit of the code will change at a time. When a non-Gray code such as straight binary is advanced from 3 to 4 (0011 to 0100) three bits of the code must change. Since in many applications the voltages on the three lines do not change simultaneously, a number of false outputs may be generated which last for a short time. These false outputs are easily accepted by the high-speed devices now in use. In contrast, the excess 3 Gray code of the MC5444/7444 would change from 0101 to 0100 to advance from 3 to 4.

Analog measuring devices require a converter for information fed to a digital system. These converters usually use a Gray code output. Gray codes are also useful in sequential circuitry because of the change of only one bit at a time.

Figure 3 shows the MC5444/7444 used for decoding 3-line binary-to-octal. The input to A, B, and D is the binary code ABC. The C input of the device is used as a strobe. Octal data is taken from outputs Q1 through Q8 when the strobe is taken to a logic "1". Outputs Q0 and Q9 are not used.

FIGURE 1 – BINARY-TO-DECIMAL DECODING USING MC5442/7442



*These decimal outputs are available from both decoders.

FIGURE 2 – 4-LINE EXCESS THREE CODE-TO-NINES COMPLEMENT DECIMAL DECODING USING MC5443/7443

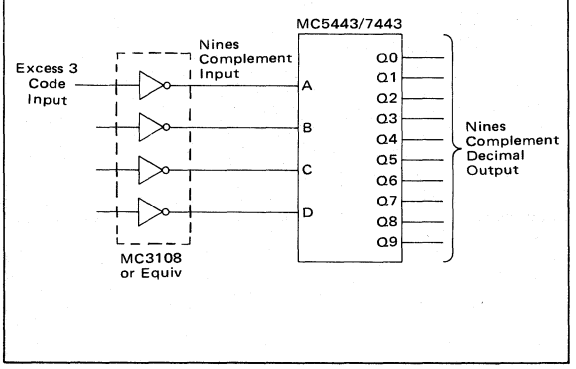
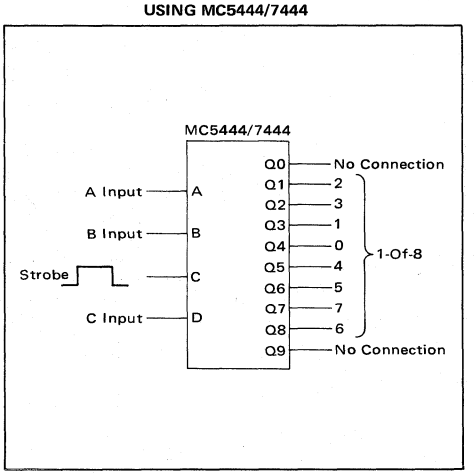
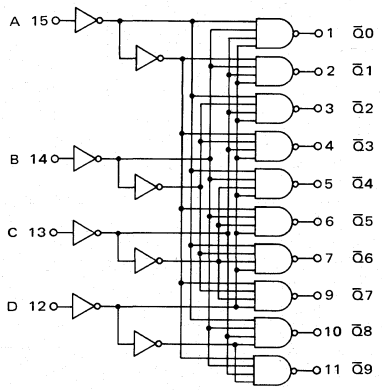


FIGURE 3 – 3-LINE BINARY-TO-OCTAL DECODING USING MC5444/7444



MC5445L • MC7445L,P*
MC54145L • MC74145L,P*



V_{CC} = Pin 16
GND = Pin 8

These devices are intended for use as drivers for indicators or relays, rather than drivers for MTTL logic gates, as is the case with the MC5442/7442, which is functionally identical. The output transistors of these devices are capable of sinking 80 mA, and have breakdown voltages of 30 V (MC5445/7445) and 15 V (MC54145/74145). The outputs are suitable for open-collector logic applications, and are compatible for interfacing with most MOS integrated circuits. Since full decoding is included, all outputs remain off for non-BCD inputs

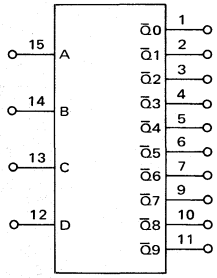
Total Power Dissipation = 215 mW typ/pkg
Propagation Delay Time = 50 ns max

INPUTS				OUTPUTS									
D	C	B	A	Q̄9	Q̄8	Q̄7	Q̄6	Q̄5	Q̄4	Q̄3	Q̄2	Q̄1	Q̄0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

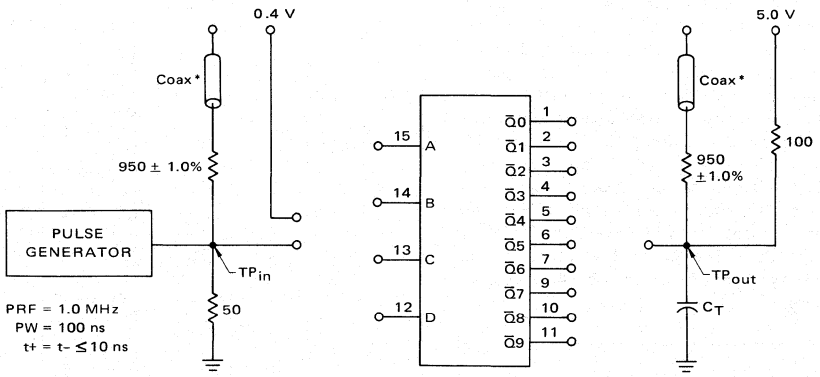
Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner according to the truth table. Test all input-output combinations according to the truth table.



									TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
									mA			Volts								
									I_{OL1}	I_{OL2}	I_{CEX}	V_{IL}	V_{IH}	V_{IHH}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	
									MC5445, MC54145	20	80	0.25	0.4	2.4	5.5	2.0	0.8	5.0	4.5	5.5	
									MC7445, MC74145	20	80	0.25	0.4	2.4	5.5	2.0	0.8	5.0	4.75	5.25	
			MC5445/MC54145 Test Limits -55 to +125°C			MC7445/MC74145 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL1}	I_{OL2}	I_{CEX}	V_{IL}	V_{IH}	V_{IHH}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																				
Forward Current	I_F	12	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	12	–	–	–	–	–	–	16	8
Leakage Current	I_{R1}	12	–	40	μAdc	–	40	μAdc	–	–	–	–	12	–	–	–	–	–	16	8
	I_{R2}	12	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	12	–	–	–	–	16	8
Output																				
Output Voltage	V_{OL}	1	–	0.9	Vdc	–	0.9	Vdc	–	1	–	–	–	–	–	12,13,14,15	–	16	–	8
		1	–	0.4	Vdc	–	0.4	Vdc	1	–	–	–	–	–	–	12,13,14,15	–	16	–	8
MC5445/7445	V_{CEX}	1	30	–	Vdc	30	–	Vdc	–	–	1	–	–	–	12,13,14,15	–	–	–	16	8
MC54145/74145		1	15	–	Vdc	15	–	Vdc	–	–	1	–	–	–	12,13,14,15	–	–	–	16	8
Power Requirements (Total Device)																				
Power Supply Drain	I_{PD}	16	–	62	mAdc	–	70	mAdc	–	–	–	–	–	–	–	–	–	–	16	8,12,13,14,15
Switching Parameters									Pulse In		Pulse Out									
Turn-On Delay	t_{pd-}	15,1	–	50#	ns	–	50#	ns	15		1	12,13,14	–	–	–	–	16	–	–	8
Turn-Off Delay	t_{pd+}	15,1	–	50#	ns	–	50#	ns	15		1	12,13,14	–	–	–	–	16	–	–	8

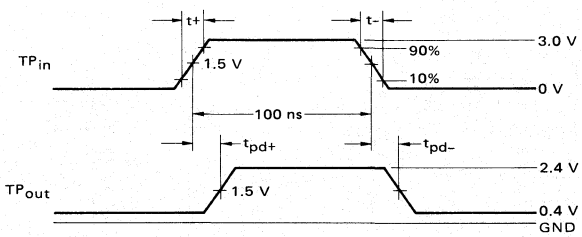
#Tested only at 25°C.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



TYPICAL APPLICATIONS

Two MC5445/7445 or MC54145/74145 decoder/drivers (depending on drive requirements) may be used to perform 4-line to 16-line decoding. Data inputs A, B, and C are applied to both decoder/drivers, while input D is applied to one decoder and $\overline{D}$ to the other. (See Figure 1.)

In addition to the obvious decoder applications, these circuits can also be used for data distribution (Figure 2). Inputs A, B, and C of the decoder/driver are used as control inputs, while the D input serves as the data input. In a typical compound data routing application, origin data is selected by the control inputs of the MC54151/74151 8-channel data selector. The data is then routed to the proper destination by means of the MC5445/7445 decoder/driver control lines.

FIGURE 1 – BINARY-TO-DECIMAL DECODING USING MC5445/7445 OR MC54145/74145

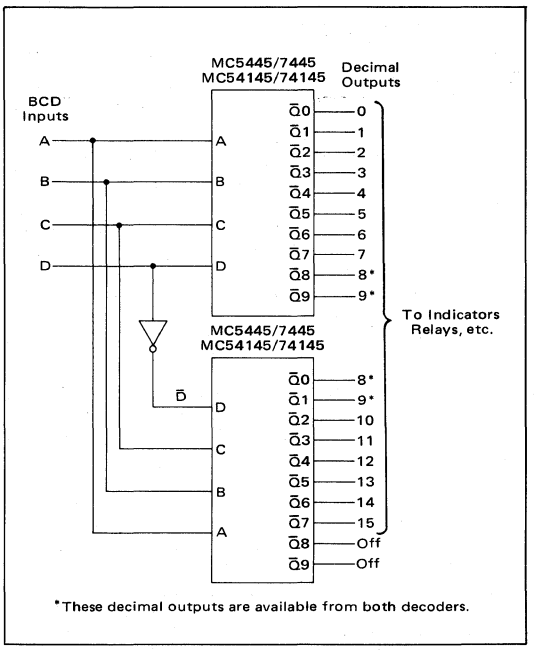
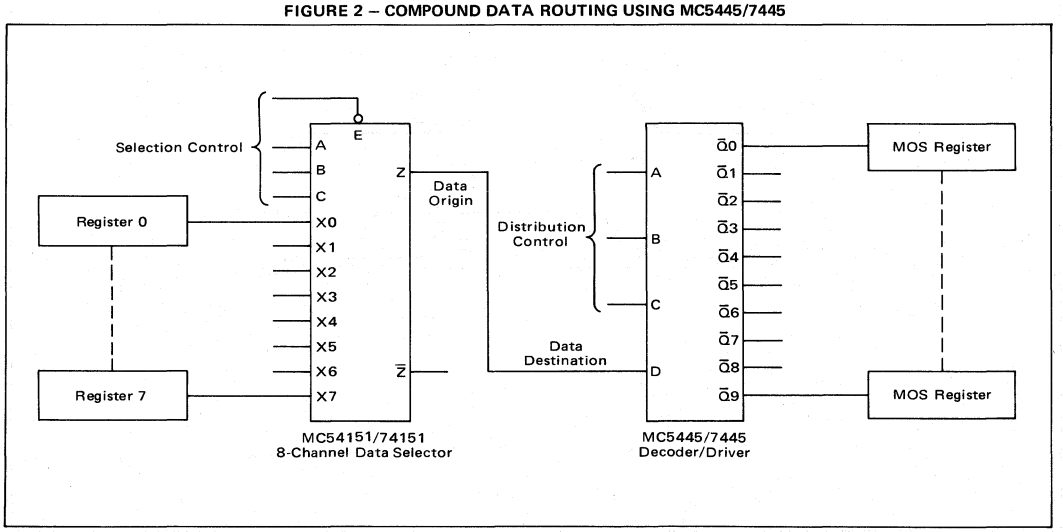
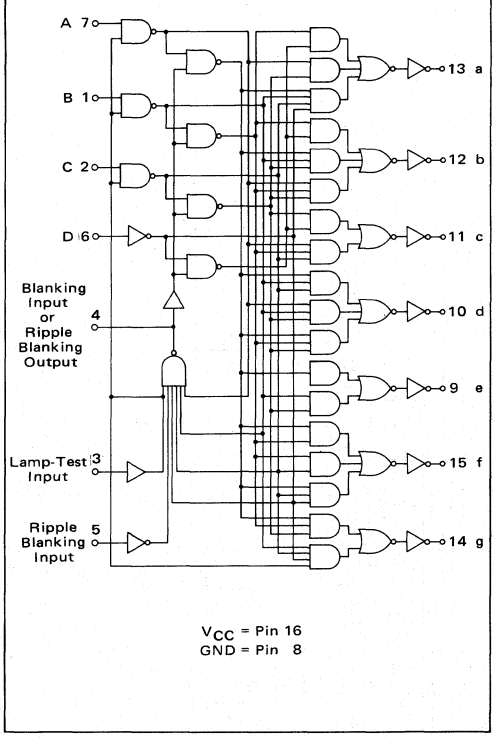


FIGURE 2 – COMPOUND DATA ROUTING USING MC5445/7445



MC5446L • MC7446L, P*
MC5447L • MC7447L, P*

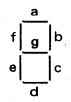
Compatible with MC5400/7400 Series devices.



V_{CC} = Pin 16
GND = Pin 8

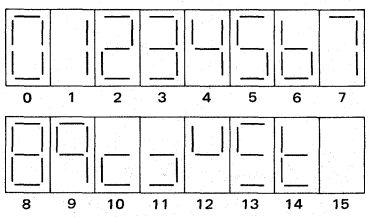
These devices decode 4-bit binary coded decimal data, dependent on the state of auxiliary inputs, and provide direct driving of incandescent, seven-segment, display indicators.

Ripple blanking inputs provide capability for suppression of non-significant zeros in a system. The blanking input can be used to control lamp intensity.



SEGMENT IDENTIFICATION

NUMERICAL DESIGNATION – SEGMENTS ILLUMINATED



Input Loading Factor:
BI/RBO = 2.6
Other Inputs = 1

Output Loading Factor:
BI/RBO = 5

Total Power Dissipation =
265 mW typ/pkg

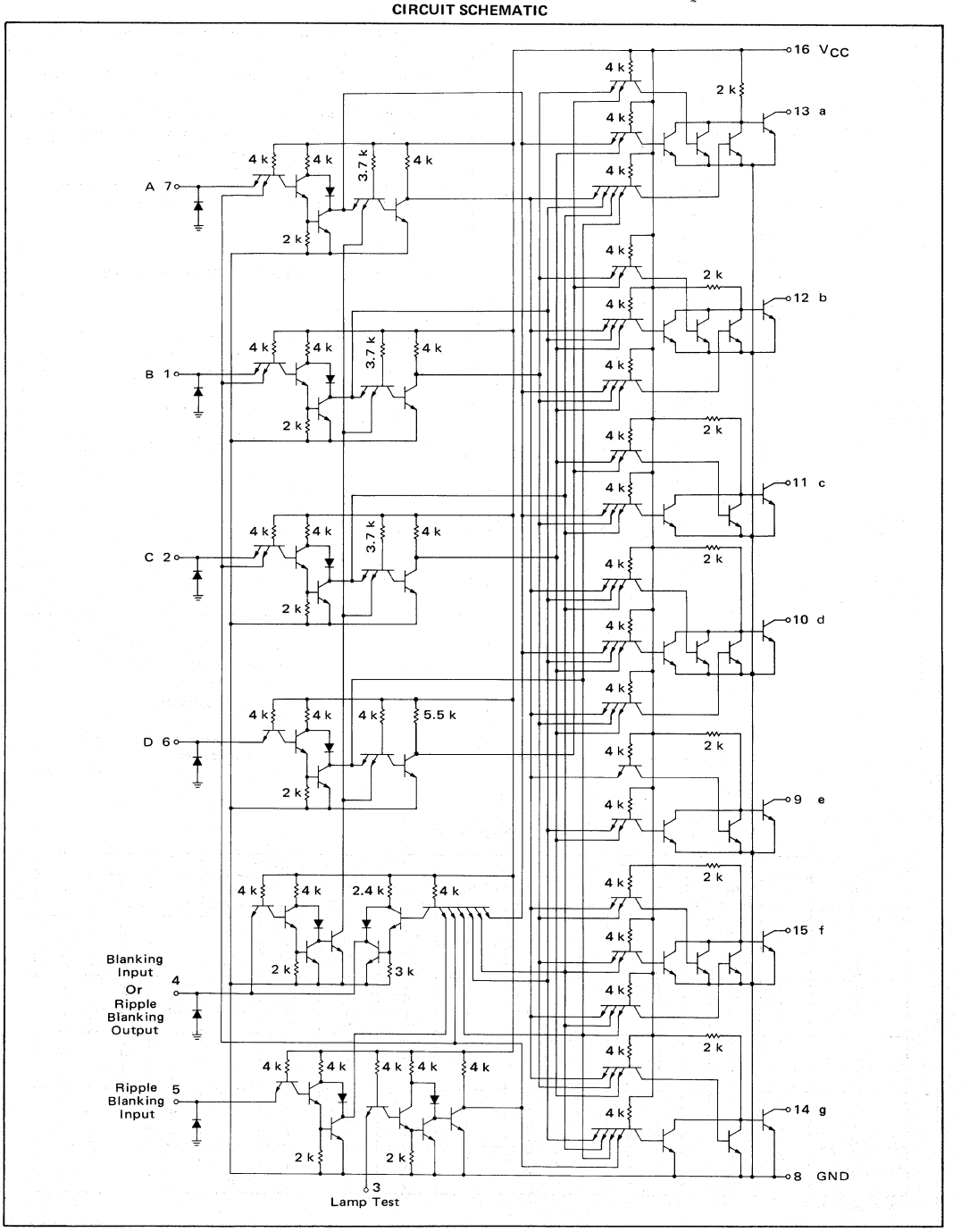
TRUTH TABLE

DIGIT OR FUNCTION	INPUT							OUTPUT						
	LT Pin 3	RBI Pin 5	D Pin 6	C Pin 2	B Pin 1	A Pin 7	BI/RBO Pin 4	a Pin 13	b Pin 12	c Pin 11	d Pin 10	e Pin 9	f Pin 15	g Pin 14
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1
1	1	X	0	0	0	1	1	1	0	0	1	1	1	1
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0
12	1	X	1	1	0	0	1	1	0	1	1	1	0	0
13	1	X	1	1	0	1	1	0	1	1	0	1	0	0
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1
BI	X	X	X	X	X	X	0	1	1	1	1	1	1	1
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1
LT	0	X	X	X	X	X	1	0	0	0	0	0	0	0

X = Don't care

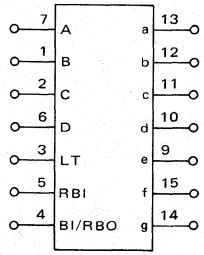
*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one data input and the blanking input, and for one driver output and the ripple blanking output. Test other inputs and outputs in the same manner according to the truth table. Test all input-output combinations according to the truth table.

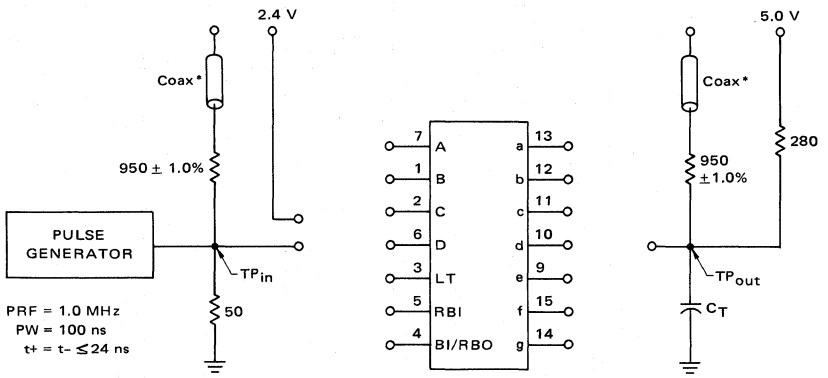


	TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
	mA				Volts								
	I_{OL1}	I_{OL2}	I_{OH}	I_{CEX}	V_{IL}	V_{IH}	V_{IHH}	$V_{th\ 1}$	$V_{th\ 0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC5446, MC5447	20	8.0	-0.2	0.25	0.4	2.4	5.5	2.0	0.8	5.0	4.5	5.5	2.4
MC7446, MC7447	20	8.0	-0.2	0.25	0.4	2.4	5.5	2.0	0.8	5.0	4.75	5.25	2.4

Characteristic	Symbol	Pin Under Test	MC5446/MC5447 Test Limits -55 to +125°C			MC7446/MC7447 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:													Gnd
			Min	Max	Unit	Min	Max	Unit	I_{OL1}	I_{OL2}	I_{OH}	I_{CEX}	V_{IL}	V_{IH}	V_{IHH}	$V_{th\ 1}$	$V_{th\ 0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
Input																						
Forward Current	I_F	1	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	–	1	3	–	–	–	–	–	16	–	8
		4	–	-4.2	mAdc	–	-4.2	mAdc	–	–	–	–	4	–	–	–	–	–	–	16	–	8
Leakage Current	I_{R1}	1	–	40	μAdc	–	40	μAdc	–	–	–	–	–	1	–	–	–	–	–	16	–	3,8
	I_{R2}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	–	1	–	–	–	–	16	–	3,8
Output																						
Output Voltage	V_{OL}	9*	–	0.4	Vdc	–	0.4	Vdc	9	–	–	–	–	–	–	3,4,5	1,2,6,7	–	16	–	–	8
		4**	–	0.4	Vdc	–	0.4	Vdc	–	4	–	–	–	–	–	3	1,2,5,6,7	–	16	–	–	8
	V_{OH}	4**	2.4	–	Vdc	2.4	–	Vdc	–	–	4	–	–	–	–	3,5	1,2,6,7	–	16	–	–	8
MC5446/7446	V_{CEX}	9*	30	–	Vdc	30	–	Vdc	–	–	–	9	–	–	–	3,4,7	1,2,6	–	–	16	–	8
MC5447/7447		9*	15	–	Vdc	15	–	Vdc	–	–	–	9	–	–	–	3,4,7	1,2,6	–	–	16	–	8
Short-Circuit Current	I_{SC}	4	–	-4.0	mAdc	–	-4.0	mAdc	–	–	–	–	–	–	–	3,5	1,2,6,7	–	–	16	–	4,8
Power Requirements (Total Device)																						
Power Supply Drain	I_{PD}	16	–	76	mAdc	–	90	mAdc	–	–	–	–	–	–	–	1,2,3,4,5,6,7	–	–	–	16	–	8
Switching Parameters									Pulse In		Pulse Out											
Turn-On Delay	t_{pd-1}	7,9	–	100#	ns	–	100#	ns	7		9		–	–	–	–	–	16	–	–	1,2,3,4,5	6,8
Turn-Off Delay	t_{pd+1}	7,9	–	100#	ns	–	100#	ns	7		9		–	–	–	–	–	16	–	–	3,4,5	1,2,6,8
Turn-On Delay	t_{pd-2}	4,5,13	–	100#	ns	–	100#	ns	4,5		13		–	–	–	–	–	16	–	–	3	1,2,6,7,8
Turn-Off Delay	t_{pd+2}	4,5,13	–	100#	ns	–	100#	ns	4,5		13		–	–	–	–	–	16	–	–	3	1,2,6,7,8

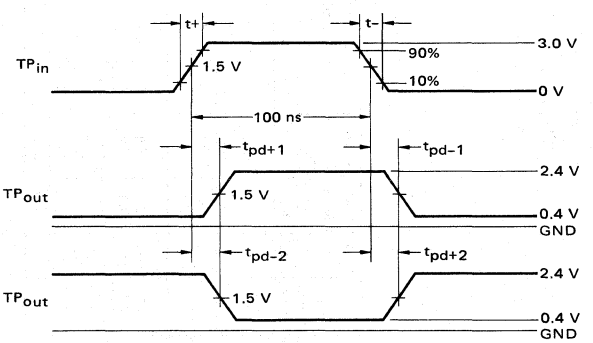
*Test procedure for outputs a thru g.
**Test procedure for BI/RBO only.
#Tested only at 25°C.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



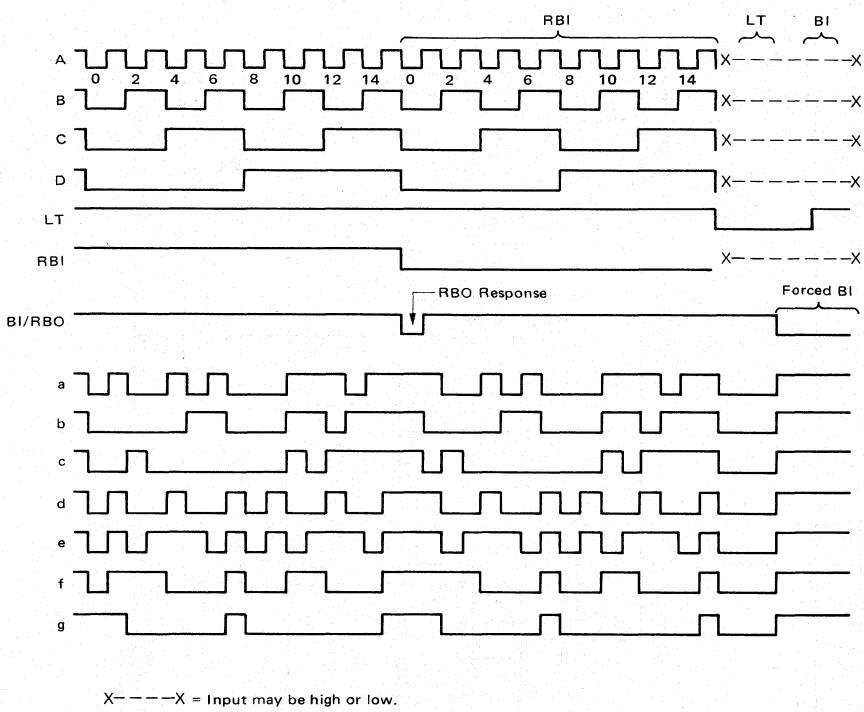
OPERATING CHARACTERISTICS

These monolithic integrated circuits provide the logic necessary to decode a BCD input and drive a seven-segment numerical indicator. Input buffers give an input loading factor of 1 on all but the BI/RBO input. High-sink-current outputs, designed to withstand the relatively high voltages of incandescent seven-segment indicators, permit direct driving of the indicators. Both devices will draw a maximum reverse current of 250 microamperes at the maximum output voltage (30 volts for the MC5446/7446 and 15 volts for the MC5447/7447).

Pin 4 serves as both a blanking input and a ripple blanking output (BI/RBO). For displaying digits 0 thru 15 the blanking input must be held at a logic "1" or open (see the truth table). For a decimal 0 output the ripple blanking input (RBI) must also be at a logic "1" or open.

When a logic "0" is applied to BI, outputs a thru g go to a logic "1" regardless of the state of any other input. With RBI at a logic "0" and A = B = C = D also at a logic "0", outputs a thru g go to a logic "1" and RBO goes to a logic "0". When a logic "0" is applied to lamp-test and BI/RBO is open or held at a logic "1", outputs a thru g go to a logic "0".

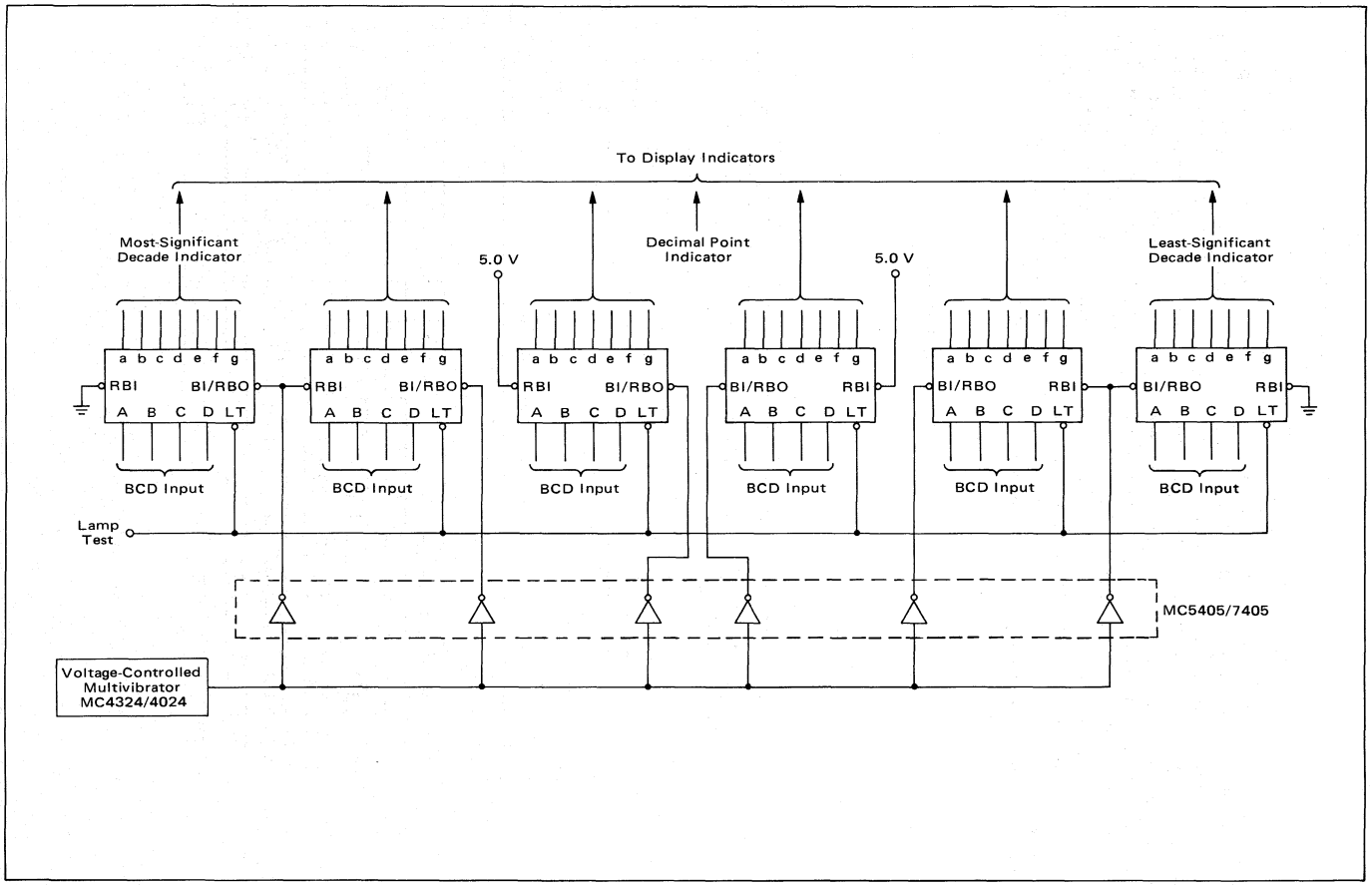
INPUT/OUTPUT VOLTAGE WAVEFORMS



TYPICAL APPLICATION

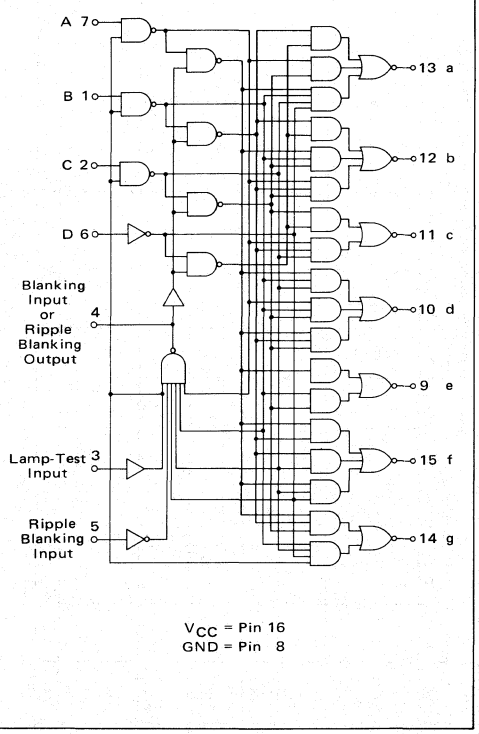
This 6-digit display provides blanking of non-significant zeros in the two most-significant and two least-significant decades. This causes the number 6.3 to be displayed instead 006.300. Blanking is achieved by grounding input RBI of the most-significant and least-significant decades and connecting the BI/RBO terminal of these two decades to input RBI of the adjacent decades. The RBI inputs of the decades on either side of the fixed decimal point are inhibited by connecting them to a 5.0-volt source, causing zeros to be retained in these positions.

Lamp intensity control is achieved by modulating input BI with a multivibrator.



BCD-TO-SEVEN SEGMENT
DECODER/DRIVER

MC5448L • MC7448L, P*



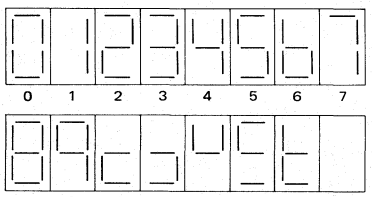
V_{CC} = Pin 16
GND = Pin 8

This device decodes 4-bit binary coded decimal input data in a format suitable for use with incandescent, seven-segment, display indicators. It is intended for use with other logic elements or discrete components rather than for the direct driving of display indicators as is the case with the MC5446/7446 and MC5447/7447 which are similar.

Ripple blanking inputs provide capability for suppression of non-significant zeros in a system. The blanking input may be used to control lamp intensity.

SEGMENT IDENTIFICATION

NUMERICAL DESIGNATION – SEGMENTS ILLUMINATED



Input Loading Factor:
BI/RBO = 2.6
Other Inputs = 1

Output Loading Factor:
BI/RBO = 5
a thru g = 4

Total Power Dissipation =
265 mW typ/pkg

TRUTH TABLE

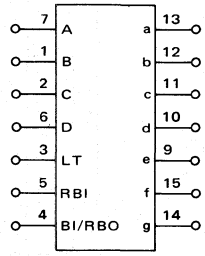
DIGIT OR FUNCTION	INPUT							OUTPUT						
	LT Pin 3	RBI Pin 5	D Pin 6	C Pin 2	B Pin 1	A Pin 7	BI/RBO Pin 4	a Pin 13	b Pin 12	c Pin 11	d Pin 10	e Pin 9	f Pin 15	g Pin 14
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1

X = Don't care

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

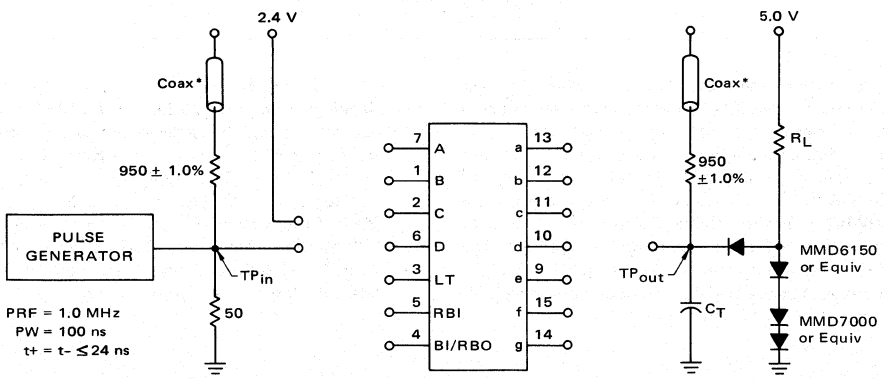
Test procedures are shown for only one data input and the blanking input, and for one driver output and the ripple blanking output. Test other inputs and outputs in the same manner according to the truth table. Test all input-output combinations according to the truth table.



									TEST CURRENT/VOLTAGE VALUES (All Temperatures)													
									mA				Volts									
									I_{OL1}	I_{OL2}	I_{OH1}	I_{OH2}	V_{IL}	V_{IH}	V_{IHH}	V_{Load}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
								MC5448	6.4	8.0	-0.4	-0.2	0.4	2.4	5.5	0.85	2.0	0.8	5.0	4.5	5.5	2.4
								MC7448	6.4	8.0	-0.4	-0.2	0.4	2.4	5.5	0.85	2.0	0.8	5.0	4.75	5.25	2.4
		Pin	MC5448 Test Limits −55 to +125°C			MC7448 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:													
Characteristic	Symbol	Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL1}	I_{OL2}	I_{OH1}	I_{OH2}	V_{IL}	V_{IH}	V_{IHH}	V_{Load}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																							
Forward Current	I_F	1	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	–	1	3	–	–	–	–	–	–	16	–	8
		4	–	-4.2	mAdc	–	-4.2	mAdc	–	–	–	–	4	–	–	–	–	–	–	–	16	–	8
Leakage Current	I_{R1}	1	–	40	µAdc	–	40	µAdc	–	–	–	–	–	1	–	–	–	–	–	–	16	–	3,8
	I_{R2}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	–	1	–	–	–	–	–	16	–	3,8
Output																							
Output Voltage	V_{OL}	9*	–	0.4	Vdc	–	0.4	Vdc	9	–	–	–	–	–	–	–	3,4,5,7	1,2,6	–	16	–	–	8
		4**	–	0.4	Vdc	–	0.4	Vdc	–	4	–	–	–	–	–	–	3	1,2,5,6,7	–	16	–	–	8
	V_{OH}	9*	2.4	–	Vdc	2.4	–	Vdc	–	–	9	–	–	–	–	–	3	1,2,5,6,7	–	16	–	–	8
		4**	2.4	–	Vdc	2.4	–	Vdc	–	–	–	4	–	–	–	–	3,5	1,2,6,7	–	–	16	–	8
Load Current	I_{Load}	9*	-1.3	–	mAdc	-1.3	–	mAdc	–	–	–	–	–	–	–	9	–	1,2,5,6,7	–	16	–	–	8
Short-Circuit Current	I_{SC}	4	–	-4.0	mAdc	–	-4.0	mAdc	–	–	–	–	–	–	–	–	3,5	1,2,6,7	–	–	16	–	4,8
Power Requirements (Total Device)																							
Power Supply Drain	I_{PD}	16	–	76	mAdc	–	90	mAdc	–	–	–	–	–	–	–	–	1,2,3,4,5,6,7	–	–	–	16	–	8
Switching Parameters									Pulse In		Pulse Out												
Turn-On Delay	t_{pd-1}	7,9	–	100#	ns	–	100#	ns	7		9		–	–	–	–	–	–	16	–	–	1,2,3,4,5	6,8
Turn-Off Delay	t_{pd+1}	7,9	–	100#	ns	–	100#	ns	7		9		–	–	–	–	–	–	16	–	–	3,4,5	1,2,6,8
Turn-On Delay	t_{pd-2}	4,5,13	–	100#	ns	–	100#	ns	4,5		13		–	–	–	–	–	–	16	–	–	3	1,2,6,7,8
Turn-Off Delay	t_{pd+2}	4,5,13	–	100#	ns	–	100#	ns	4,5		13		–	–	–	–	–	–	16	–	–	3	1,2,6,7,8

*Test procedure for outputs a thru g.
**Test procedure for BI/RBO only.
#Tested only at 25°C.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

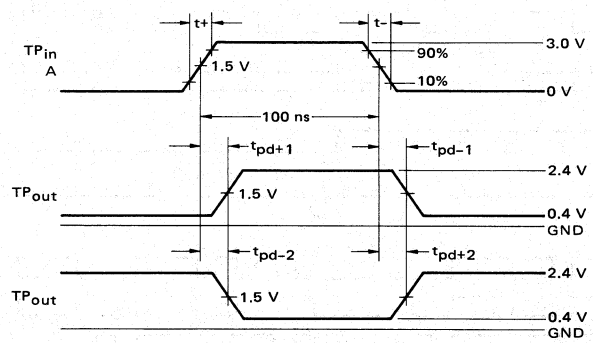


R_L = 1.0 kΩ for MC5448, 667 Ω for MC7448.

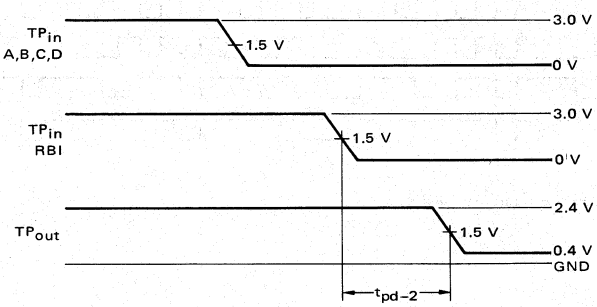
C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

A INPUT TO OUTPUTS



RBI INPUT TO OUTPUTS



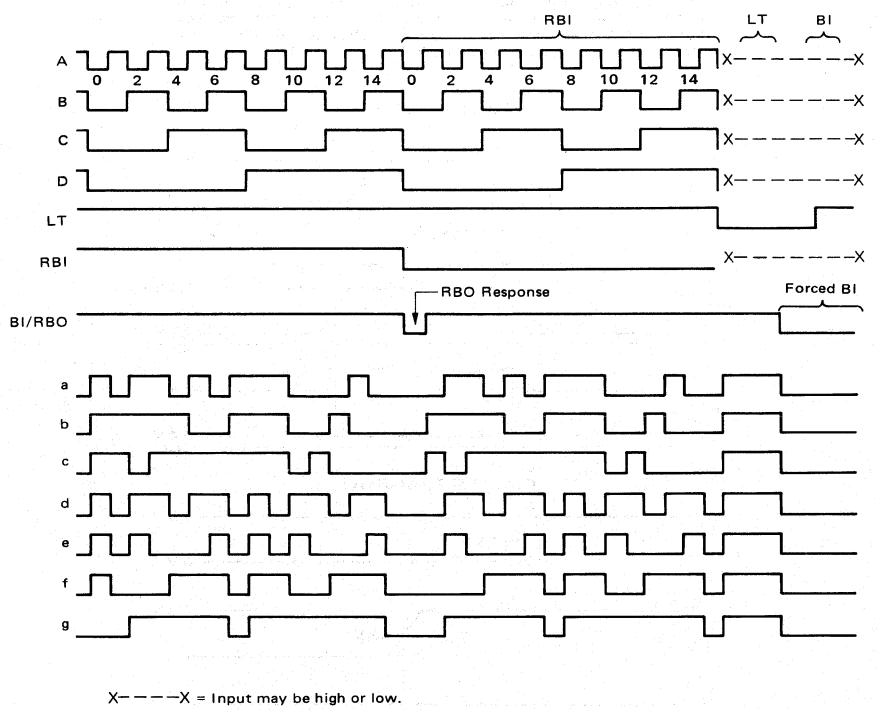
OPERATING CHARACTERISTICS

This monolithic integrated circuit provides the logic necessary to decode a BCD input and drive a seven-segment numerical indicator. It is intended for use primarily as a driver for discrete, active components or logic elements. If direct driving of display indicators is desired, the MC5446/7446 (30 volts maximum output voltage) or the MC5447/7447 (15 volts) should be used, since they are designed to handle the relatively high voltages and sink currents (20 mA) of incandescent indicators.

Pin 4 serves as both a blanking input and a ripple blanking output (BI/RBO). For displaying digits 0 thru 15 the blanking input must be held at a logic "1" or open (see the truth table). For a decimal 0 output the ripple blanking input (RBI) must also be at a logic "1" or open.

When a logic "0" is applied to BI, outputs a thru g go to a logic "0" regardless of the state of any other input. With RBI at a logic "0" and A = B = C = D also at a logic "0", outputs a thru g and RBO go to a logic "0". When a logic "0" is applied to lamp-test and BI/RBO is open or held at a logic "1", outputs a thru g go to a logic "1".

INPUT/OUTPUT VOLTAGE WAVEFORMS



APPLICATIONS INFORMATION

The MC5448/7448 is useful in applications requiring higher output currents and/or voltages than is available with the MC5446/7446. The decoder/driver may be used to drive buffer transistors selected for the required output characteristics. A suitable interface circuit is shown in Figure 1, where each decoder/driver output drives two lamp segments.

If the buffer load current is known, then base current is obtained from $I_B \approx I_L/h_{FE}$. From this and the approximate MC5448/7448 output characteristics, suitable values of R_B can be determined. For a given load current, I_{Load}, ($2I_B$ in this example) the output voltage, V_o, is given by $V_o = 2.5 - 0.139\ I_{Load} = 2.22$ volts. (See the load line of Figure 2, with $I_{Load} = 2.0$ mA.) R_B is then found from:

$$R_B = \frac{V_o - V_{BE}}{I_B} = \frac{2.22 - 0.75}{10^{-3}} \approx 1.5\ k\Omega$$

Operation of the blanking controls is identical to that of the MC5446/7446 and is illustrated in a typical application on the MC5446/7446 data sheet.

FIGURE 1 – TYPICAL INTERFACE CIRCUIT

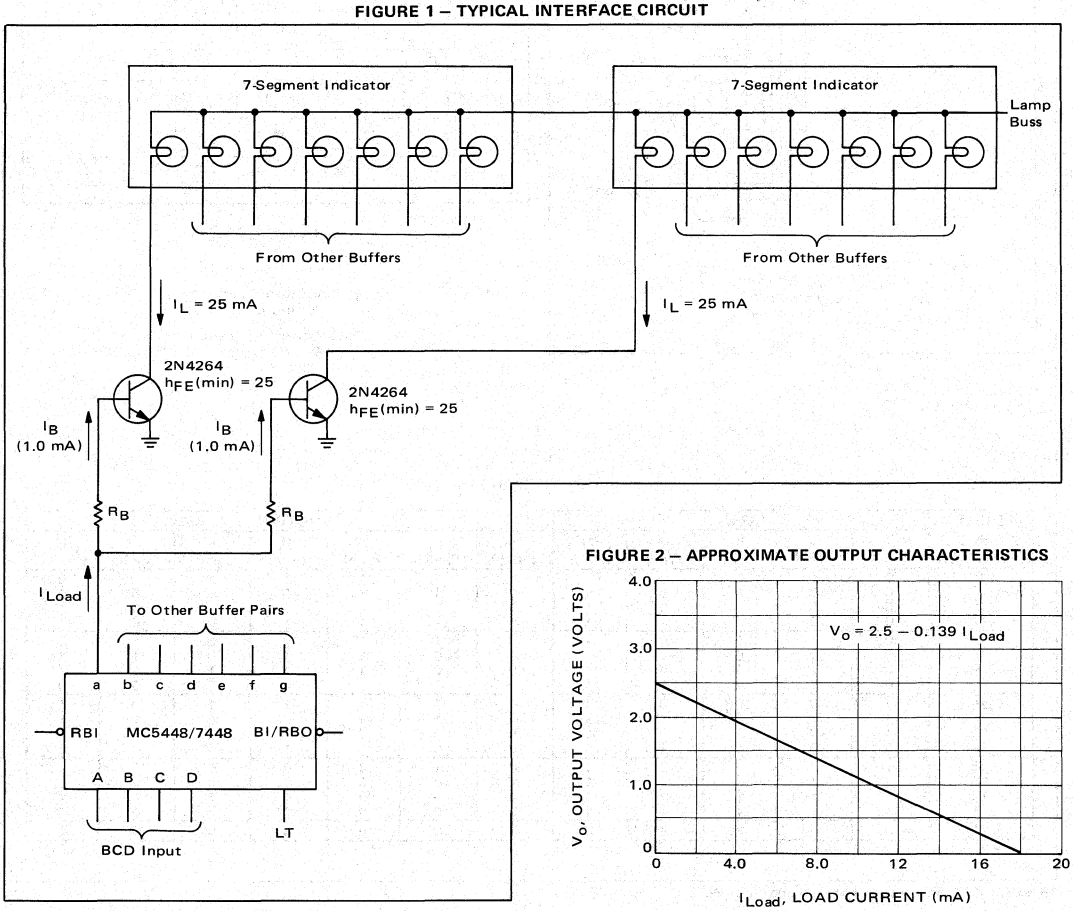
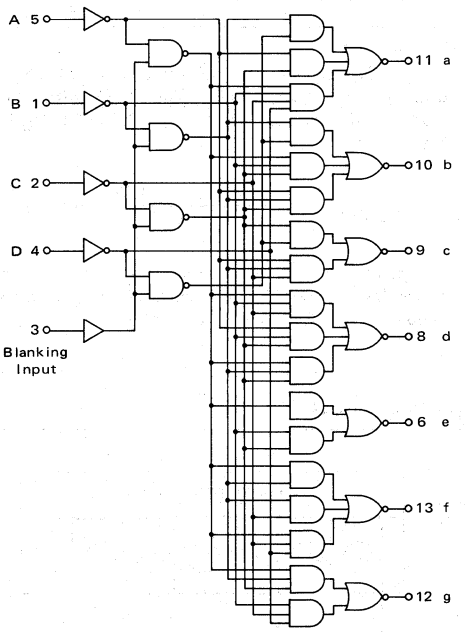


FIGURE 2 – APPROXIMATE OUTPUT CHARACTERISTICS

BCD-TO-SEVEN SEGMENT
DECODER/DRIVER

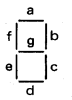
MC5449F • MC7449F*



V_{CC} = Pin 14
GND = Pin 7

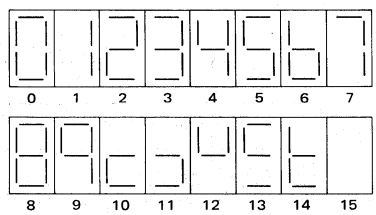
This device decodes 4-bit binary coded decimal input data in a format suitable for use with incandescent, seven-segment, display indicators. It is intended for use with other logic elements or discrete components rather than for the direct driving of display indicators as is the case with the MC5446/7446, which is similar.

Lamp intensity can be controlled by applying a variable duty cycle signal to the blanking input.



SEGMENT IDENTIFICATION

NUMERICAL DESIGNATION – SEGMENTS ILLUMINATED



Input Loading Factor:
BI = 2.6
Other Inputs = 1

Output Loading Factor:
a thru g = 6

Total Power Dissipation =
165 mW typ/pkg

TRUTH TABLE

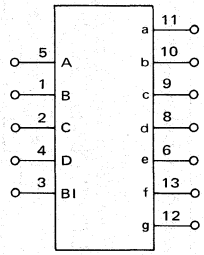
DIGIT OR FUNCTION	INPUT D Pin 4	C Pin 2	B Pin 1	A Pin 5	BI Pin 3	OUTPUT a Pin 11	b Pin 10	c Pin 9	d Pin 8	e Pin 6	f Pin 13	g Pin 12
0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	1	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	1	0	0	1
4	0	1	0	0	1	0	1	1	0	0	1	1
5	0	1	0	1	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	0	1	1
10	1	0	1	0	1	0	0	0	1	1	0	1
11	1	0	1	1	1	0	0	1	1	0	0	1
12	1	1	0	0	1	0	1	0	0	0	1	1
13	1	1	0	1	1	1	0	0	1	0	1	1
14	1	1	1	0	1	0	0	0	1	1	1	1
15	1	1	1	1	1	0	0	0	0	0	0	0
BI	X	X	X	X	0	0	0	0	0	0	0	0

X = Don't care

*F suffix = TO-86 ceramic flat package (Case 607).

ELECTRICAL CHARACTERISTICS

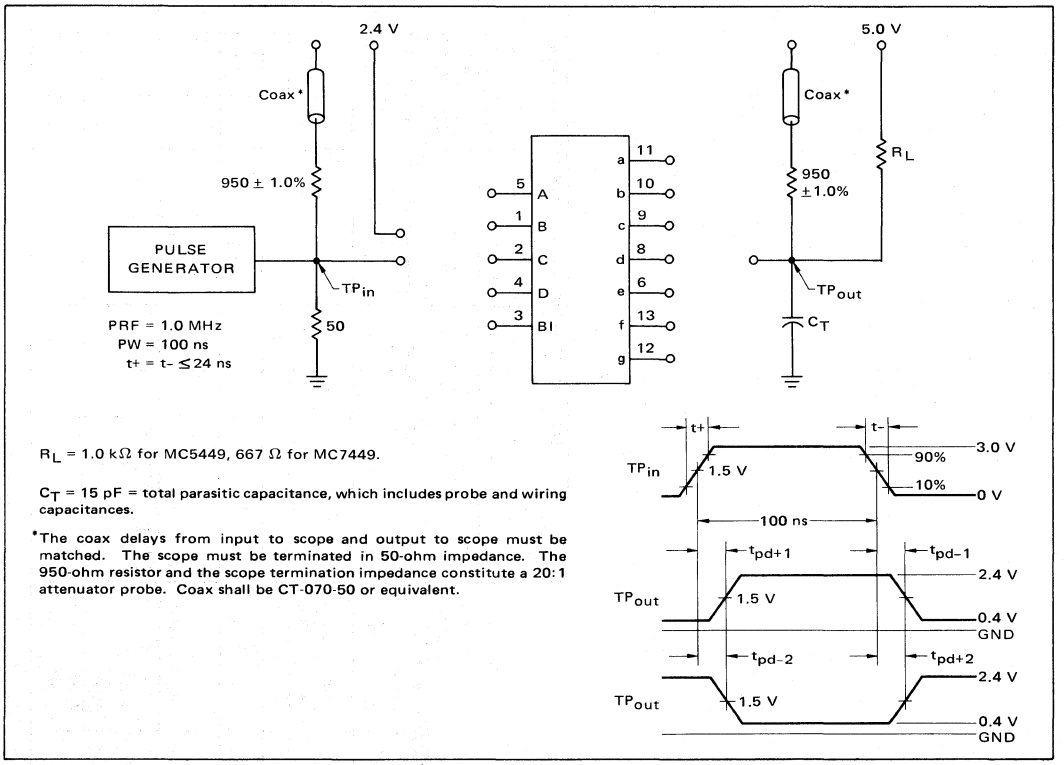
Test procedures are shown for only one data input and the blanking input, and for one driver output and the ripple blanking output. Test other inputs and outputs in the same manner according to the truth table. Test all input-output combinations according to the truth table.



									TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
									mA	Volts									
									I_{OL}	V_{IL}	V_{IH}	V_{IHH}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
								MC5449	10	0.4	2.4	5.5	2.0	0.8	5.0	4.5	5.5	2.4	
								MC7449	10	0.4	2.4	5.5	2.0	0.8	5.0	4.75	5.25	2.4	
			MC5449 Test Limits −55 to +125°C			MC7449 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL}	V_{IL}	V_{IH}	V_{IHH}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																			
Forward Current	I_F	1	–	-1.6	mAdc	–	-1.6	mAdc	–	1	–	–	–	–	–	–	14	–	7
Leakage Current	I_{R1}	1	–	40	μAdc	–	40	μAdc	–	–	1	–	–	–	–	–	14	–	7
	I_{R2}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	1	–	–	–	–	14	–	7
Output																			
Output Voltage	V_{OL}	9	–	0.4	Vdc	–	0.4	Vdc	9	–	–	–	1,2,3,4,5	–	–	14	–	–	7
Power Requirements (Total Device)																			
Power Supply Drain	I_{PD}	14	–	47	mAdc	–	56	mAdc	–	–	–	–	1,2,3,4,5	–	–	–	14	–	7
Switching Parameters									Pulse In	Pulse Out									
Turn-On Delay	t_{pd-1}	5,9	–	100#	ns	–	100#	ns	5	9	–	–	–	–	14	–	–	1,2,3	4,7
Turn-Off Delay	t_{pd+1}	5,9	–	100#	ns	–	100#	ns	5	9	–	–	–	–	14	–	–	3	1,2,4,7
Turn-On Delay	t_{pd-2}	3,13	–	100#	ns	–	100#	ns	3	13	–	–	–	–	14	–	–	–	1,2,4,5,7
Turn-Off Delay	t_{pd+2}	3,13	–	100#	ns	–	100#	ns	3	13	–	–	–	–	14	–	–	–	1,2,4,5,7

#Tested only at 25°C.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



R_L = 1.0 kΩ for MC5449, 667 Ω for MC7449.

C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

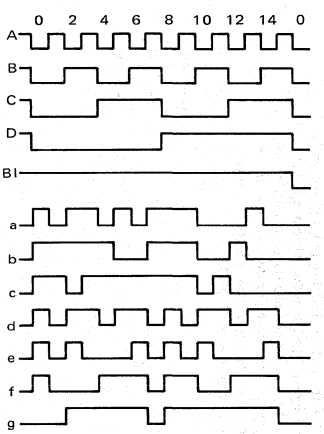
OPERATING CHARACTERISTICS

This monolithic integrated circuit provides the logic necessary to decode a BCD input and drive a seven-segment numerical indicator. It is intended for use primarily as a driver for discrete, active components or logic elements. Open collector outputs provide the capability for wire ORing the outputs with other devices.

If direct driving of display indicators is desired, the MC5446/7446 (30 volts maximum output voltage) or the MC5447/7447 (15 volts) should be used, since they are designed to handle the relatively high voltages and sink currents (20 mA) of incandescent indicators.

Ripple blanking and lamp test inputs are not available, due to the pin limitations of the 14-pin flat package. The blanking input can be used in conjunction with external gates to obtain suppression of non-significant zeros in a multiple digit display. Design of zero-suppression systems is discussed in Application Note AN-516.

INPUT/OUTPUT VOLTAGE WAVEFORMS



TYPICAL APPLICATION

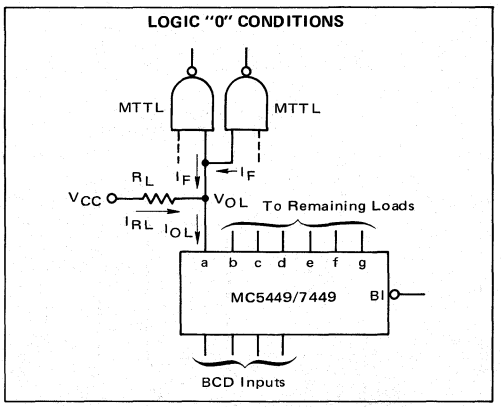
This open-collector output device may be used to drive other logic circuits by adding an external pull-up resistor as shown. Maximum and minimum values for the external resistor, R_L, must be determined for the particular circuit configuration. The maximum value will be determined by the requirements for sufficient current to external loads when the decoder/driver output is high (logic "1"). The minimum value must be selected to ensure that the current through the resistor plus the current from external loads will not cause the low output voltage (logic "0") of the decoder/driver to rise above the specified value.

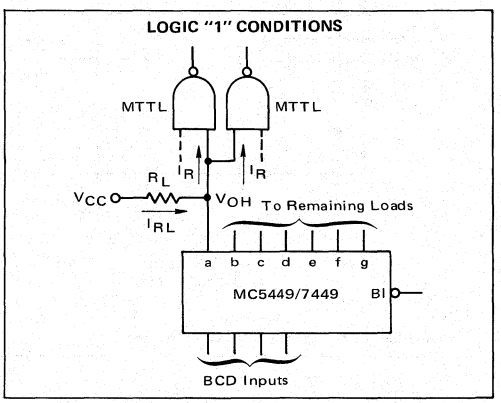
The allowable drop across the load resistor, R_L, for the high state is the difference between V_{CC} (5.0 volts), and the required output voltage, V_{OH} (2.4 volts) for the MTTL gates. The current through the resistor is the sum of the load currents, NI_{R1}, where N is the number of gates being driven and I_{R1} is the leakage current, 40 μA for a typical MTTL gate. From this, the maximum value of R_L is

$$R_L(\text{max}) = \frac{V_{CC} - V_{OH}}{NI_{R1}} = \frac{5.0 - 2.4}{2(40)\ 10^{-6}} \approx 33\ \text{k}\Omega$$

for two loads. Since the MC5449/7449 sink current, I_{OL}, is 10 mA, the minimum value of R_L in this case is given by:

$$R_L(\text{min}) = \frac{V_{CC} - V_{OL}}{I_{OL} - NI_F} = \frac{5.0 - 0.4}{[10 - 2(1.6)]\ 10^{-3}} = 680\ \Omega$$



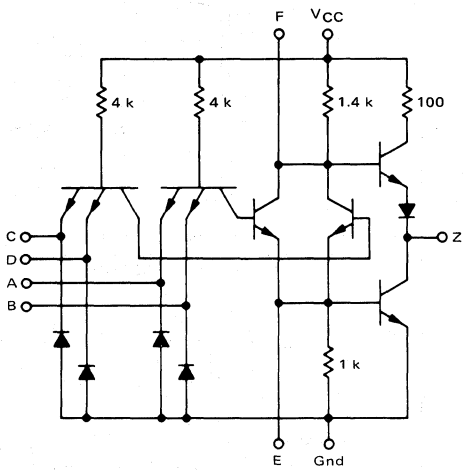


EXPANDABLE DUAL
2-WIDE 2-INPUT
"AND-OR-INVERT" GATE

MC5450 • MC7450

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7450 only.

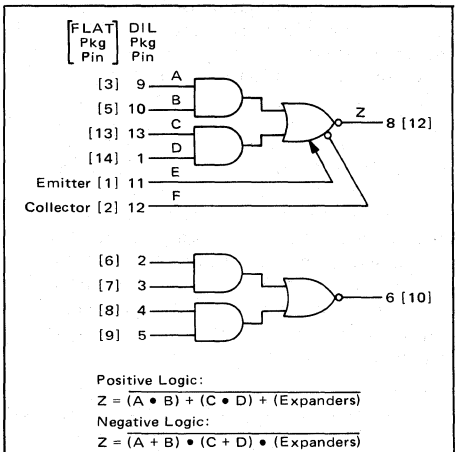
CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN†



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

†Other half of circuit omits expander inputs.

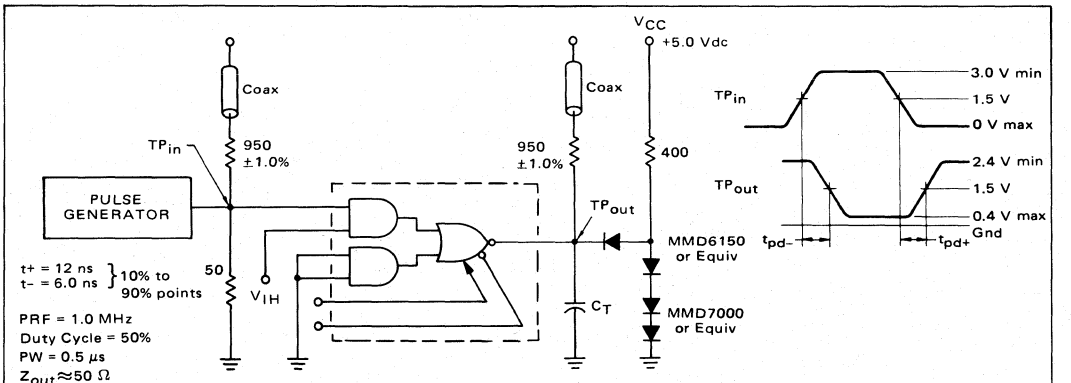
This device consists of two AND-OR-INVERT gates, one of which OR expandable. Up to four MC5460/7460 expander gates may be ORed with the device at the expander points.



Positive Logic:
$Z = \overline{(A \bullet B) + (C \bullet D) + (\text{Expanders})}$
Negative Logic:
$Z = \overline{(A + B) \bullet (C + D) \bullet (\text{Expanders})}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 28 mW typ/pkg
Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

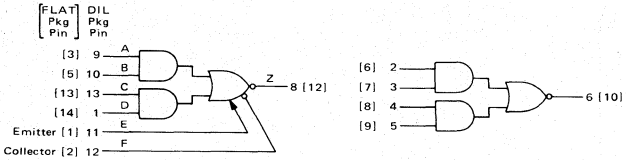


C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



V= V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

									TEST CURRENT/VOLTAGE VALUES (All Temperatures)																			
									mA						Ohms	Volts											
									I_{OL}	I_{OH}	I_{X1}	I_{X2}	I_{X3}	I_{X4}	R_{EX}③	V_{EX}①	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Pin 7[11] is grounded for all tests in addition to the pins listed below:
									MC5450	16	-0.4	0.41	0.15	-0.15	0.3	138	0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50	
									MC7450	16	-0.4	0.62	0.27	-0.27	0.43	130	0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25	
			MC5450 Test Limits −55 to +125°C			MC7450 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																			
Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	I_{X1}	I_{X2}	I_{X3}	I_{X4}	R_{EX}③	V_{EX}①	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																											
Forward Current	I_F	D	-	-1.6	mAdc	-	-1.6	mAdc	-	-	-	-	-	-	-	-	D	-	-	C	-	-	-	-	-	V	*
Leakage Current	I_{R1}	D	-	40	μAdc	-	40	μAdc	-	-	-	-	-	-	-	-	-	D	-	-	-	-	-	-	-	V	A,B,C*
	I_{R2}	D	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	-	-	-	-	-	-	D	-	-	-	-	-	-	V	A,B,C*
Expander Input Current	I_{EX}	F ①	-	-2.9#	mAdc	-	-3.1#	mAdc	Z	-	-	-	-	-	-	E,F	-	-	-	-	-	-	-	-	-	V	-	A,B,C*,D
Base-Emitter Voltage	V_{BE}	E ②	-	1.0#	Vdc	-	1.0#	Vdc	Z	-	E,F	-	-	-	-	-	-	-	-	-	-	-	-	-	-	V	-	A,B,C*,D
Output																											
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	-	-	-	-	-	-	C,D	-	-	V	-	A,B*
		Z ③	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	E	F	-	-	-	-	-	-	C,D	-	-	V	-	A,B
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	-	-	-	-	-	-	C	-	-	D	-	V	-	A,B*
		Z	2.4#	-	Vdc	2.4#	-	Vdc	-	Z	-	E	F	-	-	-	-	-	-	-	-	-	-	-	V	-	A,B,C*,D
Short-Circuit Current	I_{SC}†	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	V	A,B,C*, D,Z
Power Requirements (Total Device)																											
Power Supply Drain	I_{PDH}	V	-	14	mAdc	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	V	A,B,C*,D
Switching Parameters									Pulse In	Pulse Out																	
Turn-On Delay	t_{pd-}	D,Z	-	15**	ns	-	15**	ns	D	Z	-	-	-	-	-	-	-	C	-	-	-	-	-	V	-	-	A,B*
Turn-Off Delay	t_{pd+}	D,Z	-	29**	ns	-	29**	ns	D	Z	-	-	-	-	-	-	-	C	-	-	-	-	-	V	-	-	A,B*

*Ground inputs to gate not under test. †Only one output should be shorted at a time. #Tested only at low temperature limit.
** Tested only at 25°C.

① See Figure 1.
② See Figure 2.
③ See Figure 3.

FIGURE 1 – I_{EX} TEST CIRCUIT

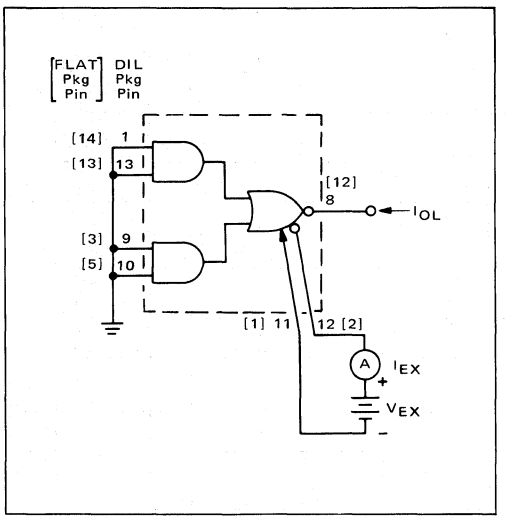


FIGURE 2 – V_{BE} TEST CIRCUIT

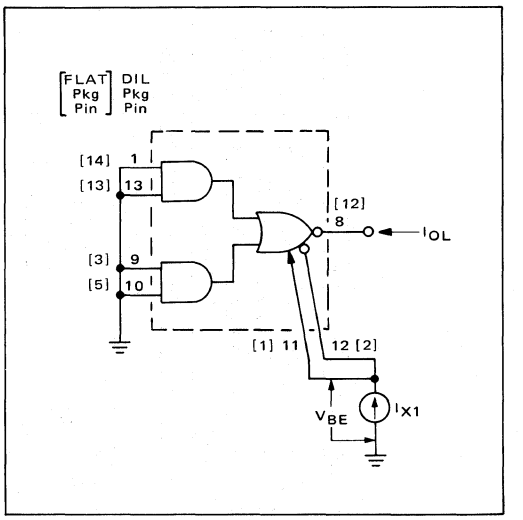
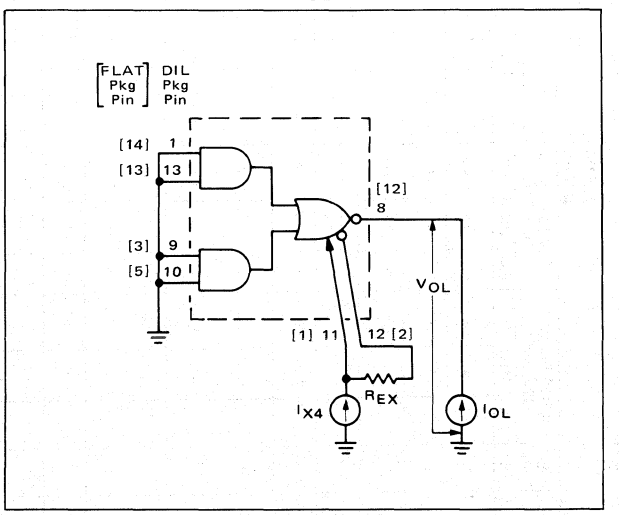


FIGURE 3 – V_{OL} TEST CIRCUIT

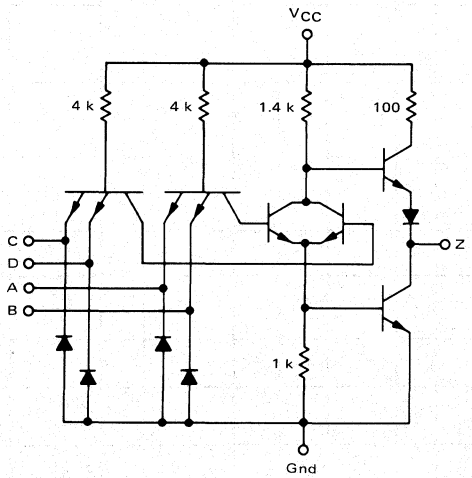


DUAL 2-WIDE 2-INPUT
"AND-OR-INVERT" GATE

MC5451 • MC7451

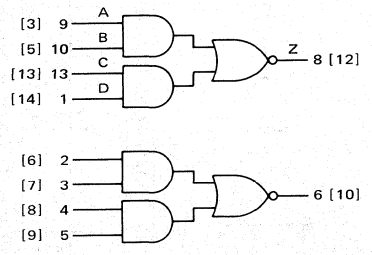
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7451 only.

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

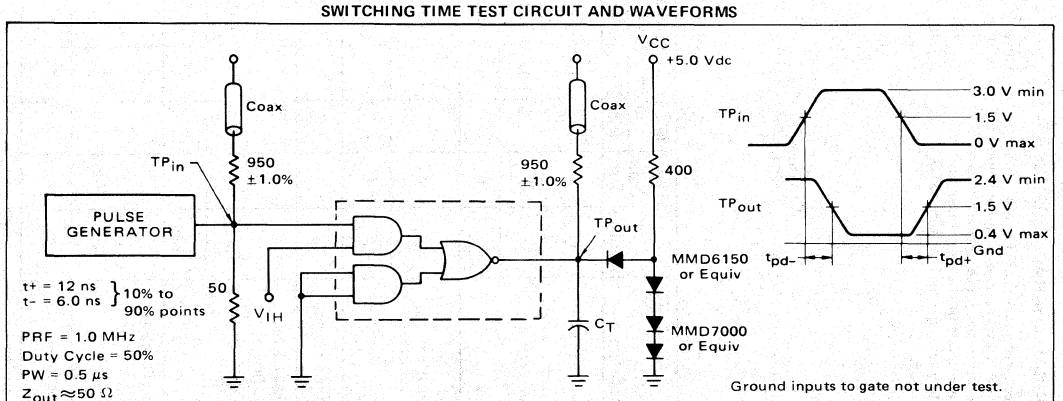
[FLAT Pkg Pin] DIL Pkg Pin



Positive Logic: $Z = \overline{(A \bullet B) + (C \bullet D)}$
Negative Logic: $Z = \overline{(A + B) \bullet (C + D)}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 28 mW typ/pkg
Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



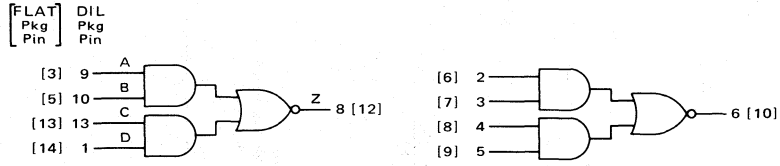
Ground inputs to gate not under test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



V = V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

									TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
									mA		Volts										
									I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	
									MC5451												
									16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50	
									MC7451												
									16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25	Pin 7[11] is grounded for all tests in addition to the pins listed below:
Characteristic	Symbol	Pin Under Test	MC5451 Test Limits −55 to +125°C			MC7451 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_F	D	-	-1.6	mAdc	-	-1.6	mAdc	-	-	D	-	-	C	-	-	-	-	-	V	*
Leakage Current	I_{R1}	D	-	40	μAdc	-	40	μAdc	-	-	-	D	-	-	-	-	-	-	-	V	A,B,C*
	I_{R2}	D	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	D	-	-	-	-	-	-	V	A,B,C*
Output																					
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	C,D	-	-	V	-	A,B*
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	C	-	-	D	-	V	-	A,B*
Short-Circuit Current	I_{SC}†	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B,C*,D,Z
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	V	-	14	mAdc	-	14	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B,C*,D
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	D,Z	-	15**	ns	-	15**	ns	D	Z	-	C	-	-	-	-	-	V	-	-	A,B*
Turn-Off Delay	t_{pd+}	D,Z	-	22**	ns	-	22**	ns	D	Z	-	C	-	-	-	-	-	V	-	-	A,B*

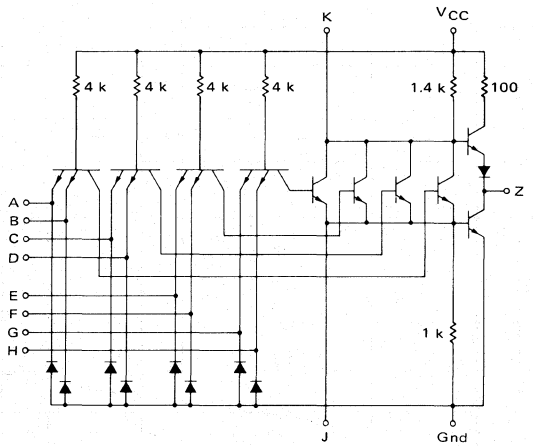
*Ground inputs to gates not under test.
**Tested only at 25°C.
†Only one output should be shorted at a time.

EXPANDABLE 4-WIDE 2-INPUT "AND-OR-INVERT" GATE

MC5453 • MC7453

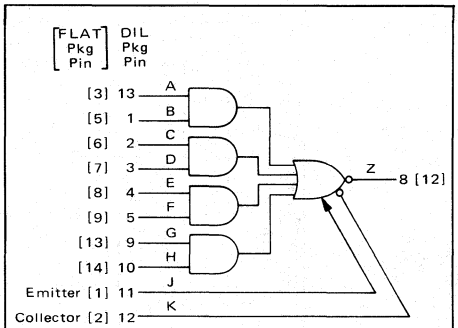
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7453 only.

CIRCUIT SCHEMATIC



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

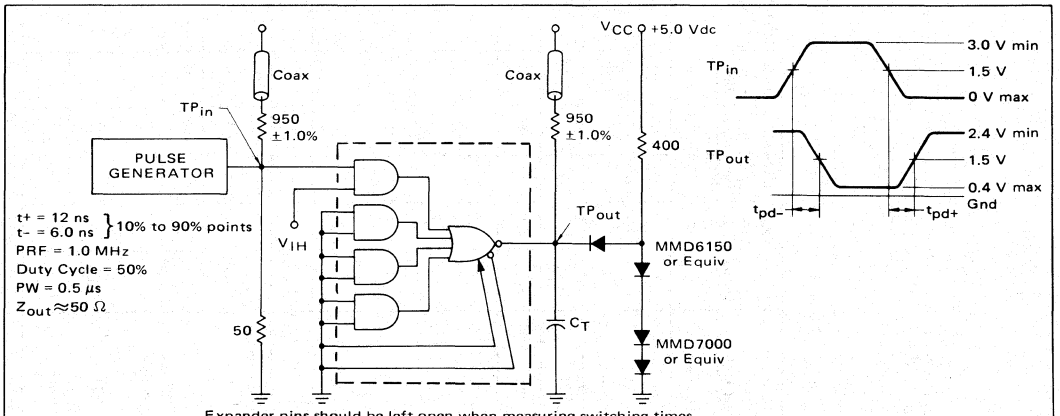
This device consists of four 2-input AND gates ORed together and inverted. Up to four MC5460/7460 expander gates may be ORed with the device at the expander points.



Positive Logic:
$Z = \overline{(A \bullet B) + (C \bullet D) + (E \bullet F) + (G \bullet H) + (\text{Expanders})}$
Negative Logic:
$Z = \overline{(A + B) \bullet (C + D) \bullet (E + F) \bullet (G + H) \bullet (\text{Expanders})}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 22 mW typ/pkg
Propagation Delay Time = 13 ns typ

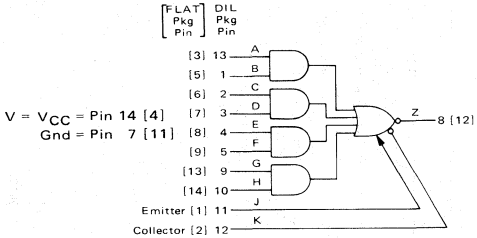
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Expander pins should be left open when measuring switching times.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one input of the device. To complete testing, sequence through remaining inputs in a similar manner.

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)																	
	mA						Ohms	Volts										
	I_{OL}	I_{OH}	I_{X1}	I_{X2}	I_{X3}	I_{X4}	R_{EX}③	V_{EX}①	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}
MC5453	16	-0.4	0.41	0.27	-0.27	0.3	138	0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
MC7453	16	-0.4	0.62	0.15	-0.15	0.43	130	0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25

Pin 7[11] is grounded for all tests in addition to the pins listed below: Gnd

Characteristic	Symbol	Pin Under Test	MC5453 Test Limits −55 to +125°C Min	Max	Unit	MC7453 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{X1}	I_{X2}	I_{X3}	I_{X4}	R_{EX}③	V_{EX}①	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																										
Forward Current	I_F	B	-	-1.6	mAdc	-	-1.6	mAdc	-	-	-	-	-	-	-	-	B	-	-	A	-	-	-	-	-	V	-
Leakage Current	I_{R1}	B	-	40	μAdc	-	40	μAdc	-	-	-	-	-	-	-	-	-	B	-	-	-	-	-	-	-	V	A,C,D,E, F,G,H
	I_{R2}	B	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	-	-	-	-	-	-	B	-	-	-	-	-	-	V	A,C,D,E, F,G,H
Expander Input Current	I_{EX}	K ①	-	-2.9#	mAdc	-	-3.1#	mAdc	Z	-	-	-	-	-	-	J,K	-	-	-	-	-	-	-	-	V	-	All Inputs
Base-Emitter Voltage	V_{BE}	J ②	-	1.0#	Vdc	-	1.0#	Vdc	Z	-	J,K	-	-	-	-	-	-	-	-	-	-	-	-	-	V	-	All Inputs
Output																											
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	-	-	-	-	-	-	A,B	-	-	V	-	C,D,E,F,G,H
		Z ③	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	J	K	-	-	-	-	-	-	-	-	-	V	-	All Inputs
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	-	-	-	-	-	-	A,D, F,H	-	-	B,C, E,G	-	V	-	-
		Z	2.4#	-	Vdc	2.4#	-	Vdc	-	Z	-	J	K	-	-	-	-	-	-	-	-	-	-	-	V	-	All Inputs
Short-Circuit Current	I_{SC}†	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	V	All Inputs, Z
Power Requirements																											
Power Supply Drain	I_{PDH}	V	-	9.5	mAdc	-	9.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	V	All Inputs
Switching Parameters									Pulse In	Pulse Out																	
Turn-On Delay	t_{pd-}	B,Z	-	15*	ns	-	15*	ns	B	Z	-	-	-	-	-	-	-	A	-	-	-	-	-	V	-	-	C,D,E,F, G,H
Turn-Off Delay	t_{pd+}	B,Z	-	22*	ns	-	22*	ns	B	Z	-	-	-	-	-	-	-	A	-	-	-	-	-	V	-	-	C,D,E,F, G,H

* Tested only at 25°C. †Only one output should be shorted at a time. # Tested at low temperature limits

① See Figure 1. ② See Figure 2. ③ See Figure 3.

FIGURE 1 – I_{EX} TEST CIRCUIT

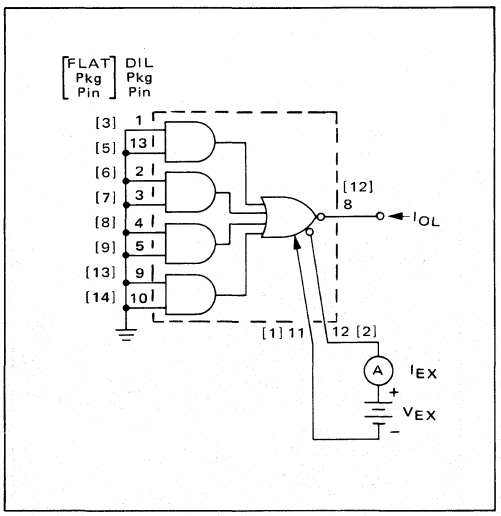


FIGURE 2 – V_{BE} TEST CIRCUIT

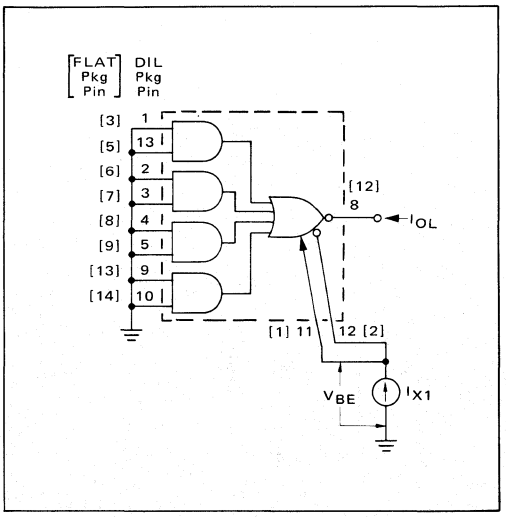
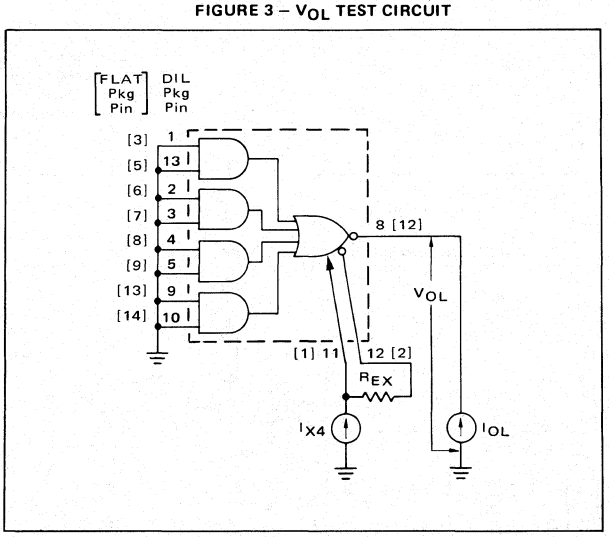


FIGURE 3 – V_{OL} TEST CIRCUIT

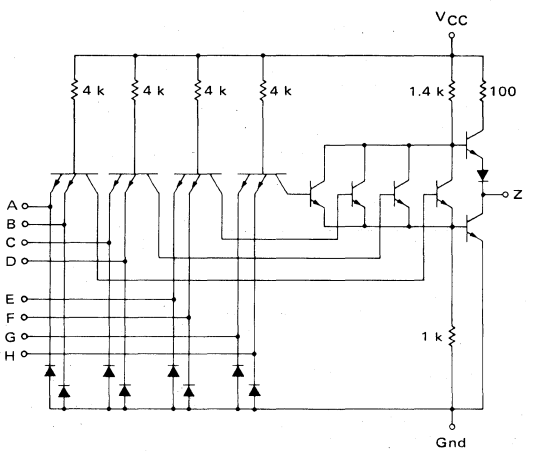


4-WIDE 2-INPUT
"AND-OR-INVERT" GATE

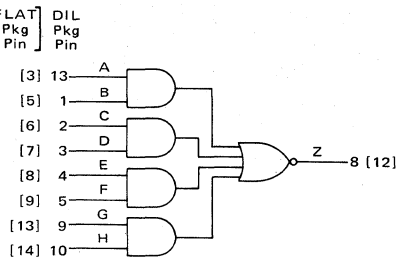
MC5454 • MC7454

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7454 only.

CIRCUIT SCHEMATIC



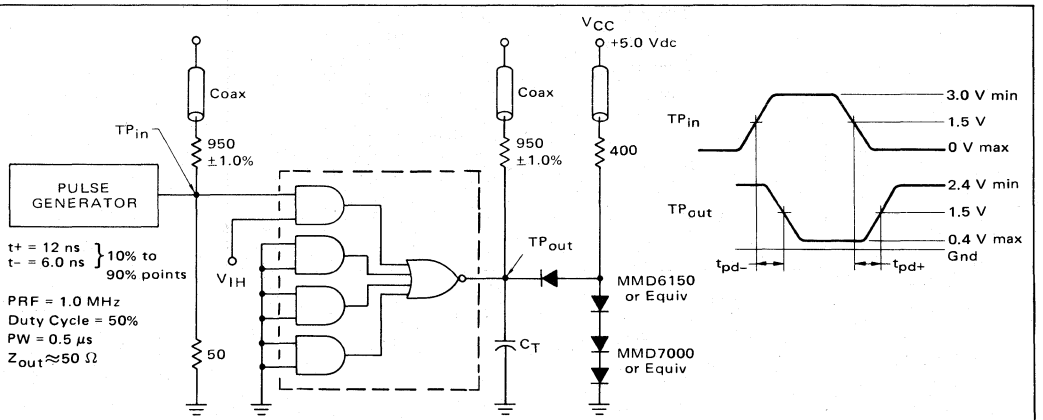
V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]



Positive Logic:
$Z = \overline{(A \bullet B) + (C \bullet D) + (E \bullet F) + (G \bullet H)}$
Negative Logic:
$Z = \overline{(A + B) \bullet (C + D) \bullet (E + F) \bullet (G + H)}$

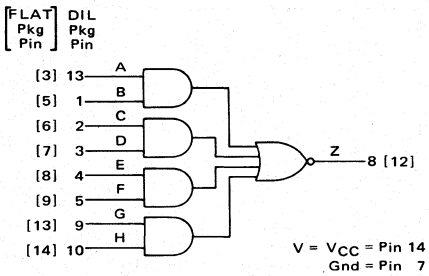
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 22 mW typ/pkg
Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input. To complete testing, sequence through remaining inputs in the same manner.

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}
MC5454	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
MC7454	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25

Pin 7[11] is grounded for all tests in addition to the pins listed below: **Gnd**

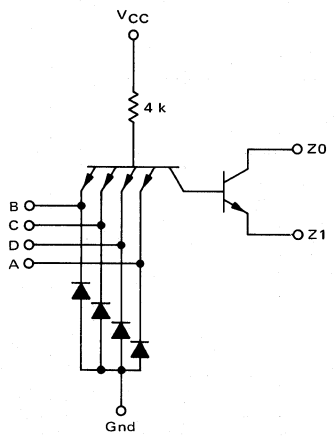
Characteristic	Symbol	Pin Under Test	MC5454 Test Limits −55 to +125°C			MC7454 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}
Input																			
Forward Current	I_F	B	-	-1.6	mAdc	-	-1.6	mAdc	-	-	B	-	-	A	-	-	-	-	-	V	-
Leakage Current	I_{R1}	B	-	40	μAdc	-	40	μAdc	-	-	-	B	-	-	-	-	-	-	-	V	A,C,D,E,F,G,H
	I_{R2}	B	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	B	-	-	-	-	-	-	V	A,C,D,E,F,G,H
Output																					
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	A,B	-	-	V	-	C,D,E,F,G,H
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	A,D,F,H	-	-	B,C,E,G	-	V	-	-
Short-Circuit Current	I_{SC} †	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	All Inputs, Z
Power Requirements																					
Power Supply Drain	I_{PDH}	V	-	9.5	mAdc	-	9.5	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	All Inputs
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	B,Z	-	15*	ns	-	15*	ns	B	Z	-	A	-	-	-	-	-	V	-	-	C,D,E,F,G,H
Turn-Off Delay	t_{pd+}	B,Z	-	22*	ns	-	22*	ns	B	Z	-	A	-	-	-	-	-	V	-	-	C,D,E,F,G,H

† Only one output should be shorted at a time.
*Tested only at 25°C.

MC5460 • MC7460

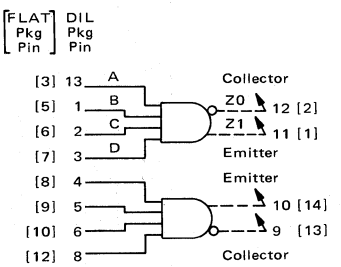
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7460 only.

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



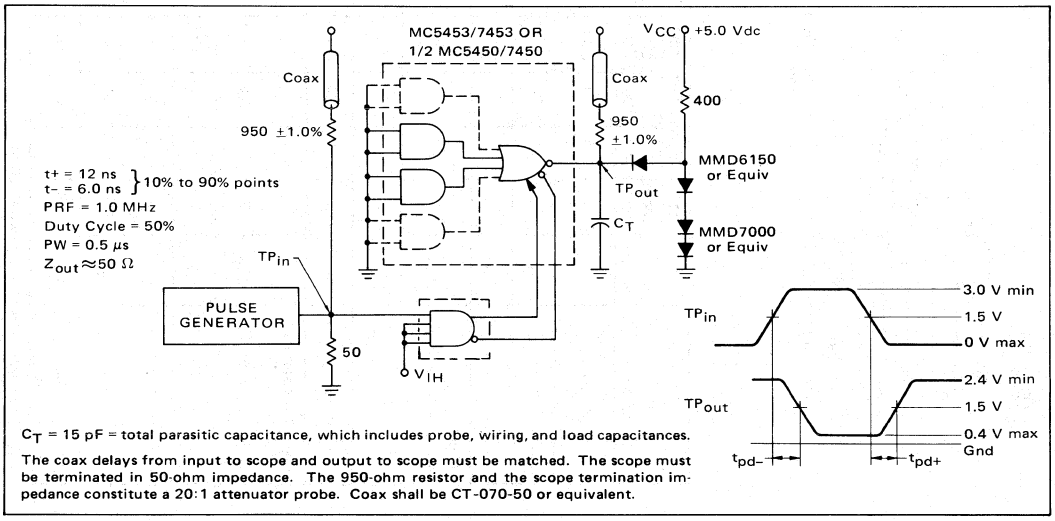
V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

This device consists of two 4-input OR expanders for use with the AND-OR-INVERT gates. A maximum of four expander gates can be added to the MC5450/7450 or MC5453/7453 expandable gates without seriously affecting their operation.



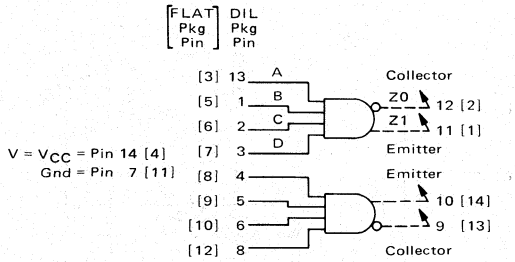
Input Loading Factor = 1
Full output loading factor of the expandable gate is maintained.
Total Power Dissipation = 8.0 mW typ/pkg
Propagation Delay Time = 5.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in the same manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.

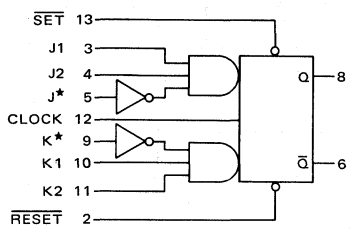
	TEST VOLTAGE VALUES (All Temperatures)															
	Ohms		Volts													
	$R_{EX\,1}$	$R_{EX\,2}$	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{O1}	V_{O2}	V_{O3}	V_{CC}	V_{CCL}	V_{CCH}	Pin 7[11] is grounded for all tests in addition to the pins listed below:
MC5460	1.2 k*	1.1 k‡	0.4	2.4	5.5	4.5	5.0	2.0	0.8	4.5	1.0	0.85	5.0	4.50	5.50	
MC7460	1.2 k*	1.1 k‡	0.4	2.4	5.5	4.5	5.0	2.0	0.8	4.5	1.0	0.85	5.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC5460 Test Limits −55 to +125°C			MC7460 Test Limits 0 to +70°C			TEST VOLTAGE APPLIED TO PINS LISTED BELOW:															Gnd
			Min	Max	Unit	Min	Max	Unit	$R_{EX\,1}$	$R_{EX\,2}$	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{O1}	V_{O2}	V_{O3}	V_{CC}	V_{CCL}	V_{CCH}	
Input																								
Forward Current	I_F	B	-	-1.6	mAdc	-	-1.6	mAdc	-	-	B	-	-	A,C,D	-	-	-	-	-	-	-	-	V	-
Leakage Current	I_{R1}	B	-	40	μAdc	-	40	μAdc	-	-	-	B	-	-	-	-	-	-	-	-	-	-	V	A,C,D
	I_{R2}	B	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	B	-	-	-	-	-	-	-	-	-	V	A,C,D
Output																								
Output Voltage	V_{OL}†	Z0,Z1	-	0.4	Vdc	-	0.4	Vdc	-	Z0	-	-	-	-	-	A,B,C,D	-	-	Z1	-	-	V	-	-
Leakage Current	I_{CEX}	Z0	-	150§	μAdc	-	270§	μAdc	Z1	-	-	-	-	A,C,D	-	-	B	Z0	-	-	-	V	-	-
Drive Current	I_{DR}	Z1	-0.3§	-	mAdc	-0.43§	-	mAdc	-	-	-	-	-	-	-	A,B,C,D	-	-	Z1	-	-	V	-	-
Power Requirements (Total Device)																								
Power Supply Drain	I_{PDL}	V	-	4.0	mAdc	-	4.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	Z1	-	-	V	All Inputs
	I_{PDH}	V	-	2.5	mAdc	-	2.5	mAdc	-	-	-	-	-	-	All Inputs	-	-	-	-	Z0	-	-	V	-
Switching Parameters									Pulse In															
Turn-On Delay	t_{pd-}	#	-	20**	ns	-	20**	ns	B	-	-	A,C,D	-	-	-	-	-	-	-	-	V	-	-	-
Turn-Off Delay	t_{pd+}	#	-	34**	ns	-	34**	ns	B	-	-	A,C,D	-	-	-	-	-	-	-	-	V	-	-	-

*Resistor to ground.
‡Resistor to V_{CCL}.
#See test circuit.
†V_{OL} measured between pins 11 and 12.
§Tested only at low temperature limit; i.e., at -55°C for MC5460, at 0°C for MC7460.
**Tested only at 25°C; times include delay of expandable gate.

J-K FLIP-FLOP

MC5470L*
MC7470L,P*



This J-K flip-flop triggers on the positive edge of the clock pulse. The multiple-input gating configuration helps minimize package count in J-K flip-flop applications requiring AND gating at the inputs. This device requires relatively fast clock rise and fall times (≤ 150 ns) but is more suitable for use in high-speed systems since information may be applied to, or changed at the steering inputs any time in a clock cycle except during the interval of time between the setup and hold times. The inputs are inhibited when the clock is high; data is entered into the input steering section when the clock goes low. The input steering section continually reflects the input states when the clock is low. The flip-flop can be set or reset directly by applying a logic "0" to $\overline{SET}$ or $\overline{RESET}$, respectively, while clock is at logical zero level

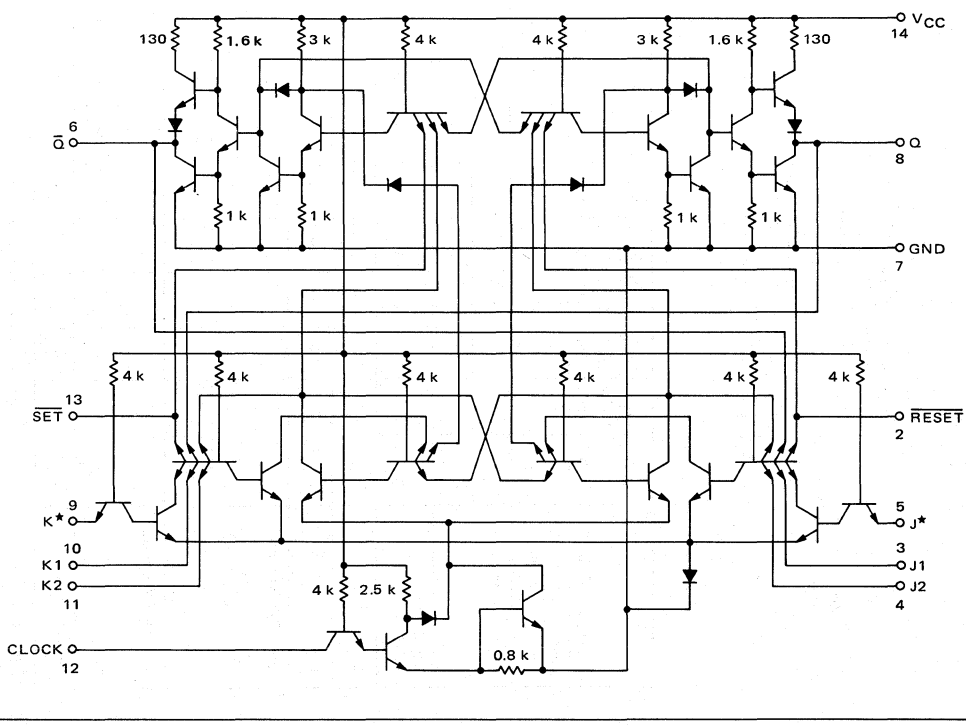
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

$J = J1 \cdot J2 \cdot \overline{J^*}$

$K = K1 \cdot K1 \cdot \overline{K^*}$

Output Loading Factor = 10
Total Power Dissipation = 65 mW typ/pkg
Propagation Delay Time = 30 ns typ
Operating Frequency = 35 MHz typ

* L suffix = TO-116 ceramic package (Case 632)
P suffix = TO-116 plastic package (Case 605)
See General Information section for package outline dimensions.



OPERATING CHARACTERISTICS

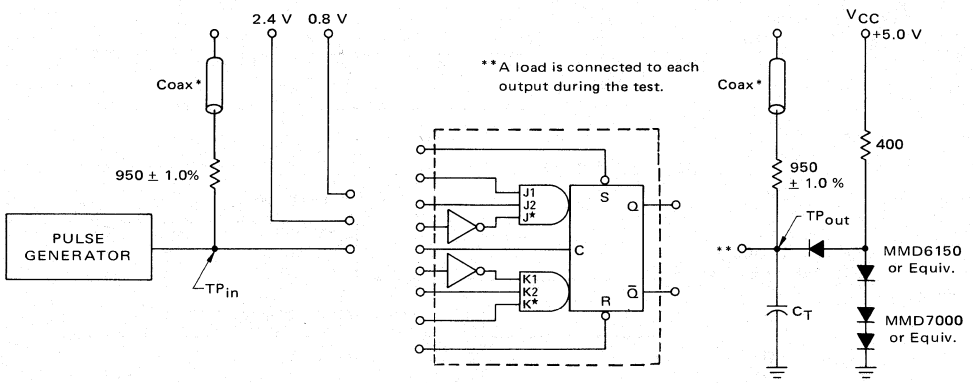
Data present during the time interval between the Set-up and Hold times is transferred to the bistable section on the positive edge of the clock pulse. Steering data should be present 20 ns prior to rise of the clock and remain 5.0 ns after the clock signal rises.

The direct $\overline{SET}$ and $\overline{RESET}$ inputs should be applied only when clock is low. A low input to $\overline{SET}$ sets Q to a logic "1"; a low input to $\overline{RESET}$ sets $\bar{Q}$ to a logic "1".

Unused inputs: If J★ and K★ are not used they should be grounded. Unused $\overline{SET}$ and $\overline{RESET}$ inputs should be tied to a voltage between 2.4 and 5.5 Vdc.
Unused J or K inputs should be tied to the used J or K inputs, respectively, or to a voltage between 2.4 and 5.5 Vdc.

12

SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved together for testing $\overline{SET}$ and $\overline{RESET}$. Only one pulse generator is required for J, K, and CLOCK tests.

* The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

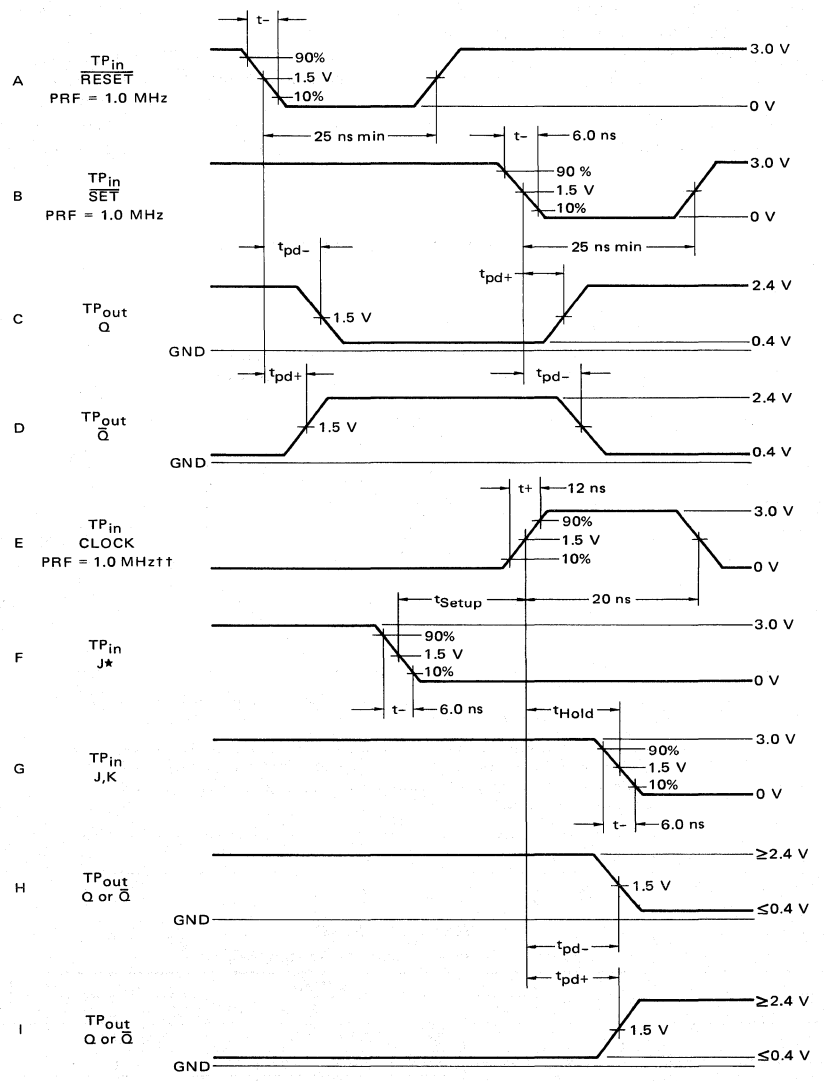
TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT							Q	$\bar{Q}$	LIMITS		
		C	J	K	J★	K★	$\bar{R}$	$\bar{S}$			Min	Max	Unit
Toggle Frequency	t_{Tog}	E	2.4 V	2.4 V	Gnd	Gnd	2.4 V	2.4 V	†	†	20	—	MHz
Turn-On Delay from $\overline{SET}$ or $\overline{RESET}$	t_{pd-}*	0.8 V	5.0 V	5.0 V	Gnd	Gnd	A	B	C	D	—	50	ns
Turn-Off Delay from $\overline{SET}$ or $\overline{RESET}$	t_{pd+}*	0.8 V	5.0 V	5.0 V	Gnd	Gnd	A	B	C	D	—	50	ns
Turn-On Delay from Clock	t_{pd-}	E	2.4 V	2.4 V	Gnd	Gnd	5.0 V	5.0 V	H,I	H,I	10	50	ns
Turn-Off Delay from Clock	t_{pd+}	E	2.4 V	2.4 V	Gnd	Gnd	5.0 V	5.0 V	H,I	H,I	10	50	ns
Minimum Input Setup Time at J★	t_{Setup}**	E	2.4 V	2.4 V	F	Gnd	5.0 V	5.0 V	H,I	H,I	—	20	ns
Minimum Input Hold Time at J1, J2	t_{Hold}**	E	G	2.4 V	Gnd	Gnd	5.0 V	5.0 V	H,I	H,I	—	5	ns

†Output shall toggle with each input pulse
*$\overline{SET}$ or $\overline{RESET}$ function can occur only when clock input is low. Other gates are inhibited.
**Identical test to be performed on K★ Input.

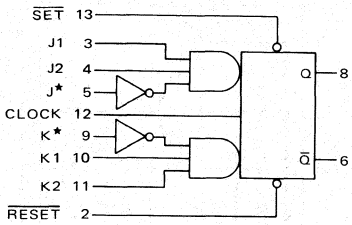
VOLTAGE WAVEFORMS AND DEFINITIONS



††PRF varies when testing f_{Tog}.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, plus the $\overline{SET}$, $\overline{RESET}$, and CLOCK inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
	mA		Volts							
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CCL}	V_{CCH}
MC5470	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	4.5	5.5
MC7470	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	4.75	5.25

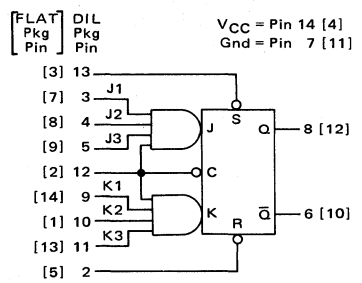
Characteristic		Symbol	Pin Under Test	MC5470 Test Limits -55 to +125°C Min	Max	Unit	MC7470 Test Limits 0° to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CCL}	V_{CCH}	Gnd
Input																				
Forward Current**	J	I_F	3	–	-1.6	mAdc	–	-1.6	mAdc	–	–	3	–	–	2*,4,10,11	–	–	–	14	5,7,9
	K		10	–	-1.6	↓	–	-1.6	↓	–	–	10	–	–	3,4,11,13*	–	–	–	↓	↓
	$\overline{Set}$		13	–	-3.2	↓	–	-3.2	↓	–	–	13	–	–	3,4,10,11	–	–	–	↓	↓
	$\overline{Reset}$		2	–	-3.2	↓	–	↓	↓	–	–	2	–	–	3,4,10,11	–	–	–	↓	↓
	Clock		12	–	-1.6	↓	–	↓	↓	–	–	12	–	–	2*,3,4,10,11	–	–	–	↓	↓
			12	–	-1.6	↓	–	↓	↓	–	–	12	–	–	3,4,10,11,13*	–	–	–	↓	↓
Leakage Current**	J	I_{R1}	3	–	40	μAdc	–	40	μAdc	–	–	–	3	–	5	–	–	–	14	2,4,7
	K		10	–	40	↓	–	40	↓	–	–	–	10	–	9	–	–	–	↓	7,11,13
	$\overline{Set}$		13	–	80	↓	–	80	↓	–	–	–	13	–	9	–	–	–	↓	7,10,11
	$\overline{Reset}$		2	–	80	↓	–	80	↓	–	–	–	2	–	5	–	–	–	↓	7,10,11
	Clock		12	–	40	↓	–	40	↓	–	–	–	12	–	–	–	–	–	↓	3,4,7
	J	I_{R2}	3	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	3	5	–	–	–	14	2,4,7
	K		10	–	↓	↓	–	↓	↓	–	–	–	–	10	9	–	–	–	↓	7,11,13
	$\overline{Set}$		13	–	↓	↓	–	↓	↓	–	–	–	–	13	9	–	–	–	↓	7,10,11
	$\overline{Reset}$		2	–	↓	↓	–	↓	↓	–	–	–	–	2	5	–	–	–	↓	7,10,11
	Clock		12	–	↓	↓	–	↓	↓	–	–	–	–	12	–	–	–	–	↓	7
Output																				
Output Voltage		V_{OL}	6	–	0.4	Vdc	–	0.4	Vdc	6	–	–	–	–	–	2	13	14	–	7,12
			8	–	0.4	Vdc	–	0.4	Vdc	8	–	–	–	–	–	13	2	14	–	7,12
		V_{OH}	6	2.4	–	Vdc	2.4	–	Vdc	–	6	–	–	–	–	13	2	14	–	7,12
			8	2.4	–	Vdc	2.4	–	Vdc	–	8	–	–	–	–	2	13	14	–	7,12
Short-Circuit Current		I_{SC}	6	-20	-57	mAdc	-18	-57	mAdc	–	–	13	–	–	–	–	–	–	14	5,7,9,12
			8	-20	-57	mAdc	-18	-57	mAdc	–	–	2	–	–	–	–	–	–	14	5,7,9,12
Power Requirements																				
Power Supply Drain		I_{PD}	14	–	26	mAdc	–	26	mAdc	–	–	–	–	–	–	–	–	–	14	2,7,12
			14	–	26	mAdc	–	26	mAdc	–	–	–	–	–	–	–	–	–	14	7,12,13

*Momentarily ground pin prior to taking measurement.
**When testing J* or K* other inputs are left open.

J-K FLIP-FLOP

MC5472 • MC7472

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7472 only.



J = J1 • J2 • J3
K = K1 • K2 • K3

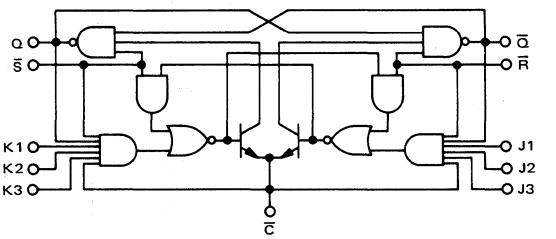
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Input Loading Factor:
J, K = 1
Clock, Set, Reset = 2

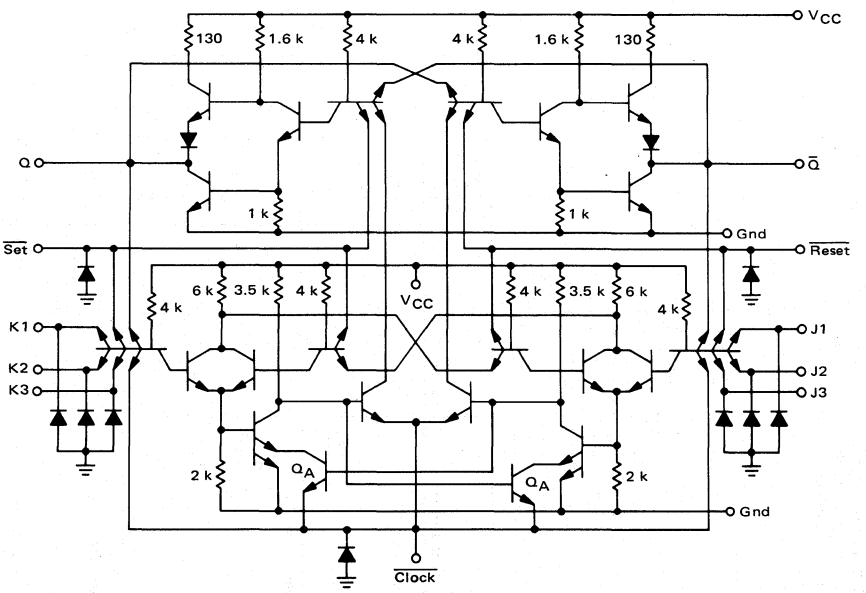
Output Loading Factor = 10
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 30 ns typ
Operating Frequency = 20 MHz typ

This negative-edge-clocked J-K flip-flop operates on the master-slave principle. Three K inputs are ANDed together, and three J inputs are ANDed together. SET and RESET inputs are also available. The device helps minimize package count in J-K flip-flop applications requiring AND gating into the J or K inputs.

LOGIC DIAGRAM

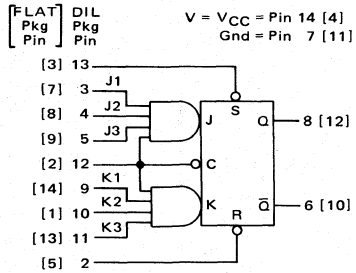


CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, plus the $\overline{\text{Set}}$, $\overline{\text{Reset}}$, and $\overline{\text{Clock}}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											Pin 7[11] is grounded for all tests in addition to the pins listed below:
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	
MC5472	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.50	5.50	
MC7472	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25	

Characteristic		Symbol	Pin Under Test	MC5472 Test Limits −55 to +125°C Min	Max	Unit	MC7472 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	J	I_F	J1	-	-1.6	mAdc	-	-1.6	mAdc	-	-	J1	-	-	C,J2,J3,R*	-	-	-	-	V	-
	K		K1	-	-1.6		-	-1.6		-	-	K1	-	-	C,K2,K3,S*	-	-	-	-		-
	$\overline{\text{Set}}$		S	-	-3.2		-	-3.2		-	-	S	-	-	C,J1,J2,J3,K1,K2,K3	-	-	-	-		-
	$\overline{\text{Reset}}$		R	-			-			-	-	R	-	-	C,J1,J2,J3,K1,K2,K3	-	-	-	-		-
	$\overline{\text{Clock}}$		C	-			-			-	-	C	-	-	J1,J2,J3,K1,K2,K3,R*	-	-	-	-		-
			C	-			-			-	-	C	-	-	J1,J2,J3,K1,K2,K3,S*	-	-	-	-		-
Leakage Current	J	I_{R1}	J1	-	40	μAdc	-	40	μAdc	-	-	-	J1	-	-	-	-	-	-	V	C,J2,J3,R
	K		K1	-	40		-	40		-	-	-	K1	-	-	-	-	-	-		C,K2,K3,S
	$\overline{\text{Set}}$		S	-	80		-	80		-	-	-	S	-	-	-	-	-	-		C,J1,J2,J3
	$\overline{\text{Reset}}$		R	-			-			-	-	-	R	-	-	-	-	-	-		C,K1,K2,K3
	$\overline{\text{Clock}}$		C**	-			-			-	-	-	C	-	-	-	-	-	-		C,J1,J2,J3,K1,K2,K3,R
	J	I_{R2}	J1	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	J1	-	-	-	-	-	V	C,J2,J3,R
	K		K1	-			-			-	-	-	-	K1	-	-	-	-	-		C,K2,K3,S
	$\overline{\text{Set}}$		S	-			-			-	-	-	-	S	-	-	-	-	-		C,J1,J2,J3
	$\overline{\text{Reset}}$		R	-			-			-	-	-	-	R	-	-	-	-	-		C,K1,K2,K3
	$\overline{\text{Clock}}$		C	-			-			-	-	-	-	C	-	-	-	-	-		C,J1,J2,J3,K1,K2,K3,S
Output																					
Output Voltage		V_{OL}	$\overline{Q}$	-	0.4	Vdc	-	0.4	Vdc	$\overline{Q}$	-	-	-	-	-	R	S	-	V	-	-
			Q	-	0.4	Vdc	-	0.4	Vdc	Q	-	-	-	-	-	S	R	-	V	-	-
		V_{OH}	$\overline{Q}$	2.4	-	Vdc	2.4	-	Vdc	-	$\overline{Q}$	-	-	-	-	S	R	-	V	-	-
			Q	2.4	-	Vdc	2.4	-	Vdc	-	Q	-	-	-	-	R	S	-	V	-	-
Short-Circuit Current		I_{SC}†	$\overline{Q}$	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	J1,J2,J3,K1,K2,K3	-	-	-	-	V	C,$\overline{Q}$,R
			Q	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	J1,J2,J3,K1,K2,K3	-	-	-	-	V	C,Q,S
Power Requirements																					
Power Supply Drain		I_{PD}	V	-	12	mAdc	-	12	mAdc	-	-	-	-	-	-	-	-	V	-	-	R
			V	-	12	mAdc	-	12	mAdc	-	-	-	-	-	-	-	-	V	-	-	S

*Momentarily ground pin prior to taking measurement.
**Under normal operating conditions this current is negative.
†Only one output should be shorted at a time.
This test guarantees that positive leakage current will not exceed the limit shown.

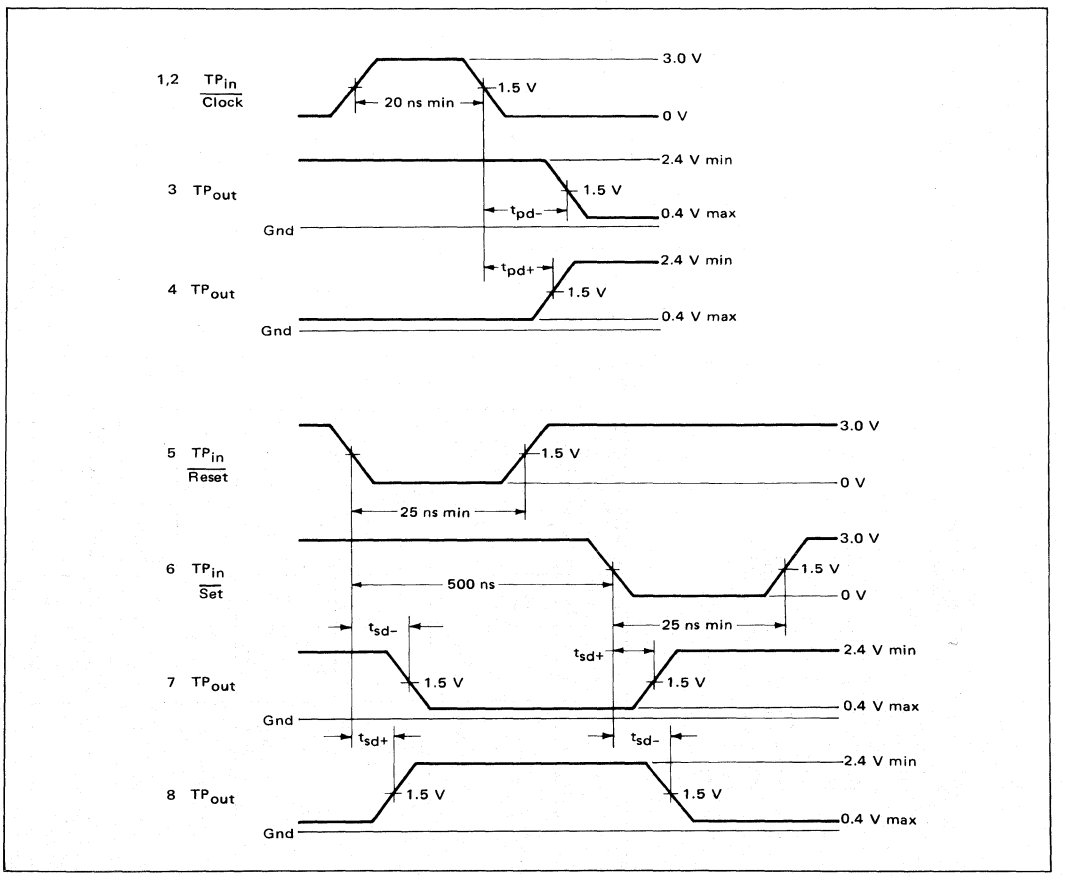
TEST PROCEDURES

(Numbers shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				Q	$\overline{Q}$	LIMITS		
		$\overline{C}$	J, K	$\overline{R}$	$\overline{S}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	1	1	2.4 V	2.4 V	†	†	15	–	MHz
Turn-On Delay	t_{pd-}	2	2	2.4 V	2.4 V	3	3	10	40	ns
Turn-Off Delay	t_{pd+}	2	2	2.4 V	2.4 V	4	4	10	25	ns
Turn-On Delay	t_{sd-}	2.4 V	2.4 V	5	6	7	8	–	40	ns
Turn-Off Delay	t_{sd+}	2.4 V	2.4 V	5	6	7	8	–	25	ns
Enable Voltage	V_{EN}	2	2.0 V	2.4 V	2.4 V	†	†	†	–	–
Inhibit Voltage	V_{INH}	2	0.8 V	2.4 V	2.4 V	‡	‡	‡	–	–

†Output shall toggle with each input pulse.
‡Output shall NOT toggle.

VOLTAGE WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS

Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

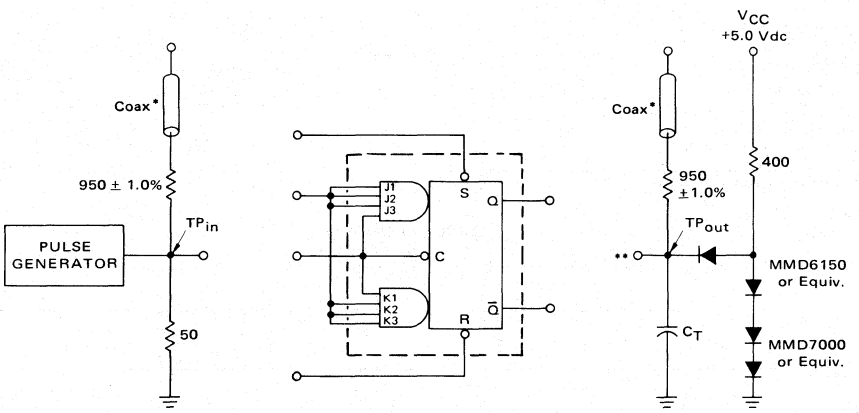
Application of a logic "0" to the $\overline{\text{Reset}}$ input will force the Q output to the logic "1" state. The $\overline{\text{Reset}}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 20 ns minimum.

Transistors Q_A have been added to the standard flip-flop circuit to protect the device against negative clock transients. This addition prevents both outputs from changing to the logic "1" state when transients in excess of –2.0 V appear at the clock.

12

SWITCHING TIME TEST CIRCUIT



t+ = 10 ns
t– = 5 ns
PRF = 15 MHz for waveform 1
1.0 MHz for waveforms 2, 5, and 6

Two pulse generators are required and must be slaved together for testing $\overline{\text{Set}}$ and $\overline{\text{Reset}}$. Only one pulse generator is required for J, K, and Clock tests.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

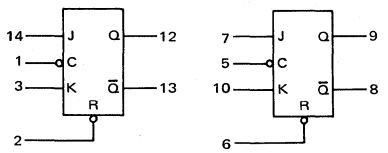
**A load is connected to each output during the test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

DUAL J-K FLIP-FLOP

MC5473 • MC7473

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7473 only.



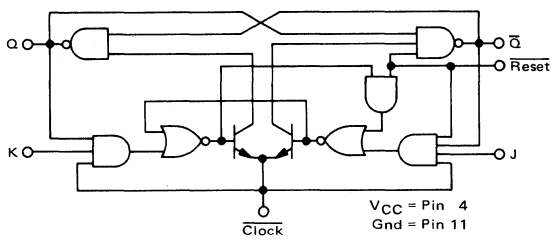
This negative-edge-clocked dual J-K flip-flop operates on the master-slave principle. The device is quite useful for simple registers and counters where multiple J and K inputs are not required.

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Input Loading Factor:
J, K = 1
$\overline{\text{Reset}}$, $\overline{\text{Clock}}$ = 2

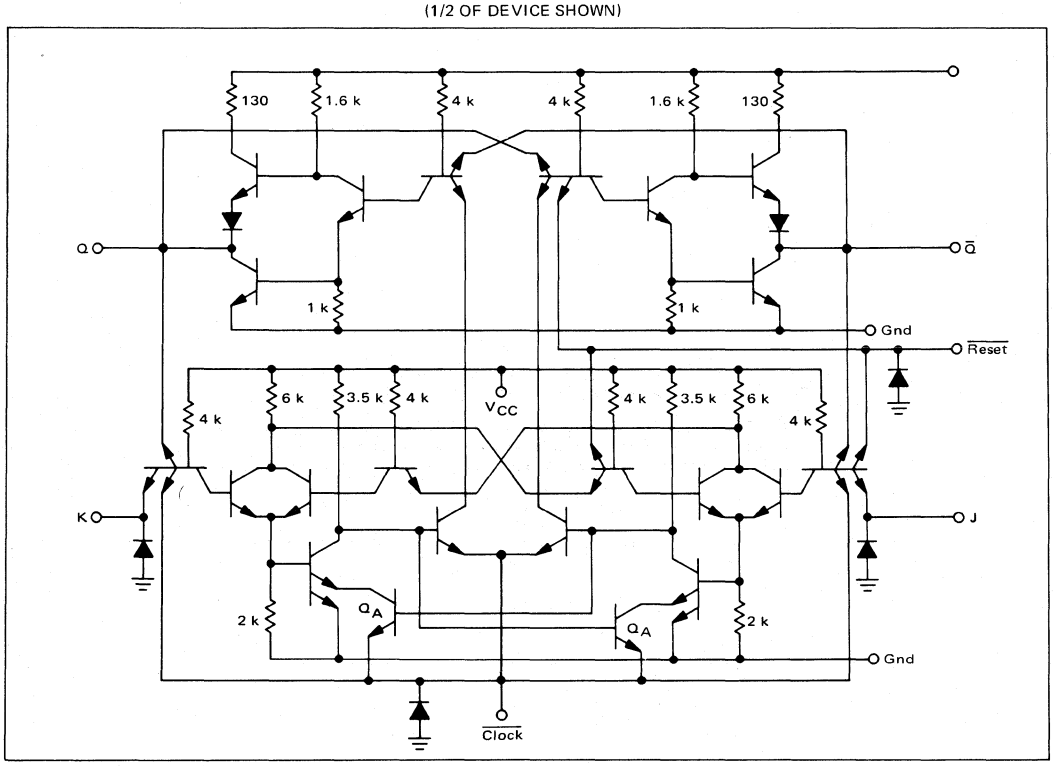
Output Loading Factor = 10
Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 30 ns typ
Operating Frequency = 15 MHz typ

LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



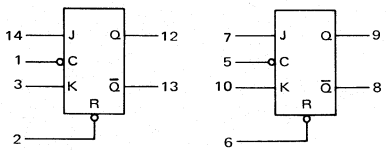
Pin numbers are the same in all packages.

LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



V = V_{CC} = Pin 4
Gnd = Pin 11

Characteristic	Symbol	Pin Under Test	MC5473 Test Limits −55 to +125°C Min	Max	Unit	MC7473 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	**	Pin 11 is grounded for all tests in addition to the pins listed below: Gnd
									MC5473 16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.50	5.50		
									MC7473 16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25		
									TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
Input																					
Forward Current J	I_F	J	-	-1.6	mAdc	-	-1.6	mAdc	-	-	J	-	-	C,R	-	-	-	-	V	Q	-
K		K	-	-1.6	↓	-	-1.6	↓	-	-	K	-	-	C,R	-	-	-	-	↓	$\bar{Q}$	-
Reset		R	-	-3.2		-	-3.2		-	-	R	-	-	C,J	-	-	-	-		-	-
Clock		C	-	-3.2	↓	-	-3.2	↓	-	-	C	-	-	J,K,R	-	-	-	-	↓	R	-
Leakage Current J	I_{R1}	J	-	40	μAdc	-	40	μAdc	-	-	-	J	-	-	-	-	-	-	V	-	C,R*
K		K	-	40	↓	-	40	↓	-	-	-	K	-	R	-	-	-	-	↓	R	C*
Reset		R	-	80		-	80		-	-	-	R	-	-	-	-	-	-		$\bar{Q}$	C,J*
Clock		C†	-	80	↓	-	80	↓	-	-	-	C	-	-	-	-	-	-	↓	-	J*,K,R
J	I_{R2}	J	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	J	-	-	-	-	-	V	-	C,R*
K		K	-	↓	↓	-	↓	↓	-	-	-	-	K	R	-	-	-	-	↓	R	C*
Reset		R	-	↓	↓	-	↓	↓	-	-	-	-	R	-	-	-	-	-		$\bar{Q}$	C,J*
Clock		C	-	↓	↓	-	↓	↓	-	-	-	-	C	-	-	-	-	-	↓	-	J*,K,R
Output																					
Output Voltage	V_{OL}	Q	-	0.4	Vdc	-	0.4	Vdc	Q	-	-	-	-	-	-	R	-	V	-	-	C,J*,K
		$\bar{Q}$	-	0.4	Vdc	-	0.4	Vdc	$\bar{Q}$	-	-	-	-	-	R	-	-	V	-	$\bar{Q}$	C,J*,K
	V_{OH}	Q	2.4	-	Vdc	2.4	-	Vdc	-	Q	-	-	-	-	-	-	-	V	-	$\bar{Q}$	C,J*,K
		$\bar{Q}$	2.4	-	Vdc	2.4	-	Vdc	-	$\bar{Q}$	-	-	-	-	-	R	-	V	-	-	C,J*,K
Short-Circuit Current	I_{SC}‡	Q	-20	-57	mAdc	-18	-57	mAdc	-	-	-	C,J,K	-	-	-	-	-	-	V	-	Q,$\bar{Q}$*
		$\bar{Q}$	-20	-57	mAdc	-18	-57	mAdc	-	-	-	C,J,K	-	-	-	-	-	-	V	-	R,$\bar{Q}$*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PD}	V	-	40	mAdc	-	40	mAdc	-	-	-	-	-	-	-	-	-	-	V	-	Both R Inputs
		V	-	40	mAdc	-	40	mAdc	-	-	-	-	-	-	-	-	-	-	V	Both $\bar{Q}$	-

*Ground inputs to flip-flop not under test.

**Momentarily ground pin prior to taking measurement to set flip-flop in the desired state. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

‡Only one output should be shorted at a time.

†Under normal operating conditions this current is negative. This test guarantees that positive leakage current will not exceed the limit shown.

OPERATING CHARACTERISTICS

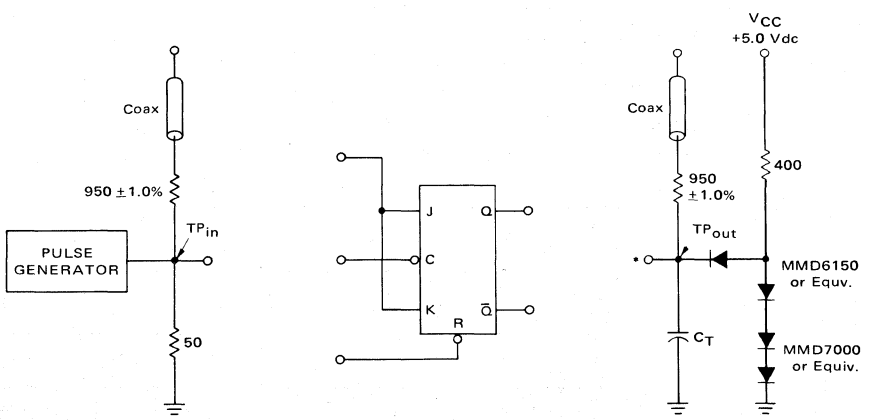
Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{\text{Reset}}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{\text{Reset}}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 20 ns minimum.

Transistors Q_A have been added to the standard flip-flop circuit to protect the device against negative clock transients. This addition prevents both outputs from changing to the logic "1" state when transients in excess of -2.0 V appear at the clock.

SWITCHING TIME TEST CIRCUIT



t+ = 12 ns
t- = 6.0 ns
} 10% to 90% Points
f = 15 MHz for waveform 1
1.0 MHz for waveforms 2 and 3

*A load is connected to each output during the test.

Two pulse generators are required and must be slaved together for t_{sd} tests.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

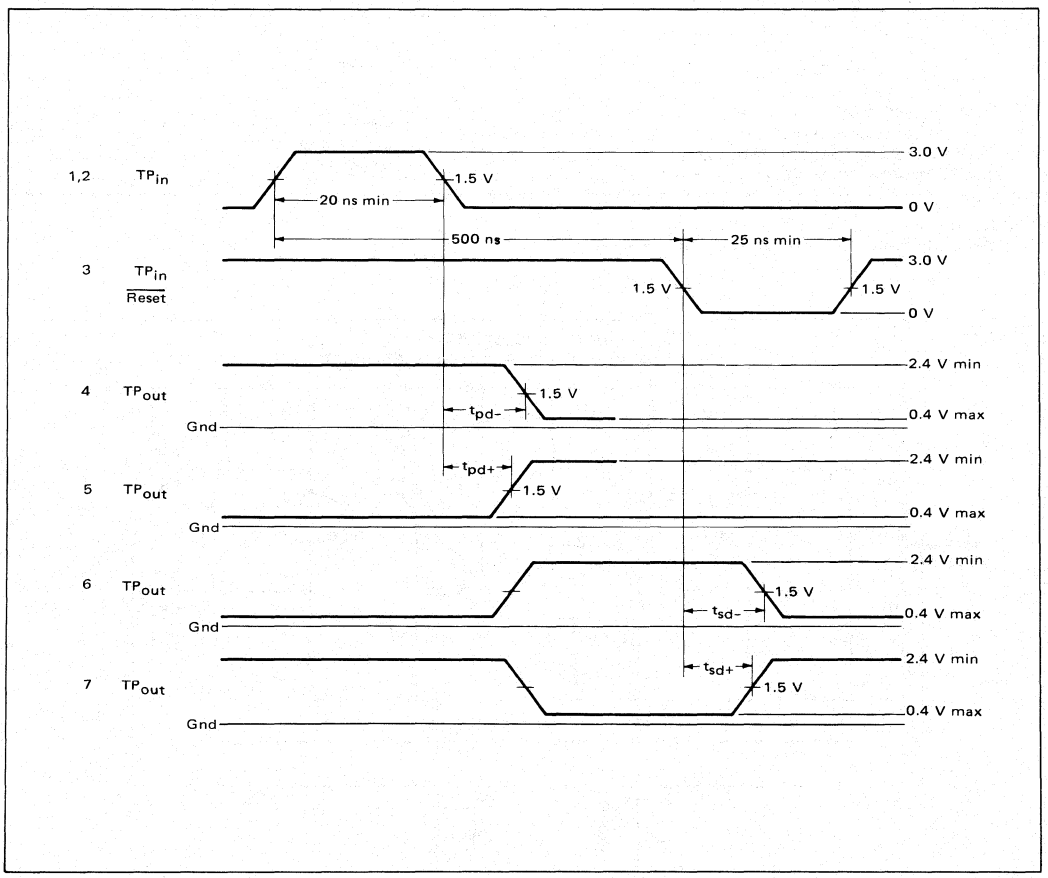
TEST PROCEDURES

(Numbers shown in test columns refer to waveforms.)

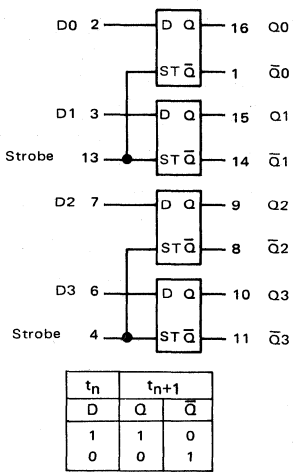
TEST	SYMBOL	INPUT			Q	$\overline{Q}$	LIMITS		
		$\overline{C}$	J, K	$\overline{R}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	1	1	2.4 V	†	†	15	–	MHz
Turn-On Delay	t_{pd-}	2	2	2.4 V	4	4	10	40	ns
Turn-Off Delay	t_{pd+}	2	2	2.4 V	5	5	10	25	ns
Turn-On Delay	t_{sd-}	2	2	3	6	7	–	40	ns
Turn-Off Delay	t_{sd+}	2	2	3	6	7	–	25	ns
Enable Voltage	V_{EN}	2	2.0 V	2.4 V	†	†	†	–	–
Inhibit Voltage	V_{INH}	2	0.8 V	2.4 V	‡	‡	‡	–	–

†Output shall toggle with each input pulse.
‡Output shall NOT toggle.

VOLTAGE WAVEFORMS AND DEFINITIONS



MC7475P*



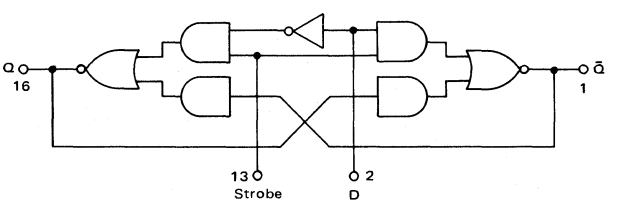
t_n	t_{n+1}	
D	Q	Q̄
1	1	0
0	0	1

Input Loading Factor:
D = 2
Strobe = 4

Output Loading Factor = 10
Total Power Dissipation = 160 mW typ/pkg
Propagation Delay Time = 30 ns typ

This device consists of four bistable latch circuits in one 16-pin package. Both Q and Q̄ outputs are available on all four devices. When the strobe is in the logic "1" state, the Q output will follow the state of the data input. When the strobe goes to the logic "0" state, the Q output will retain the state of the data input at the time of the transition from the logic "1" state.

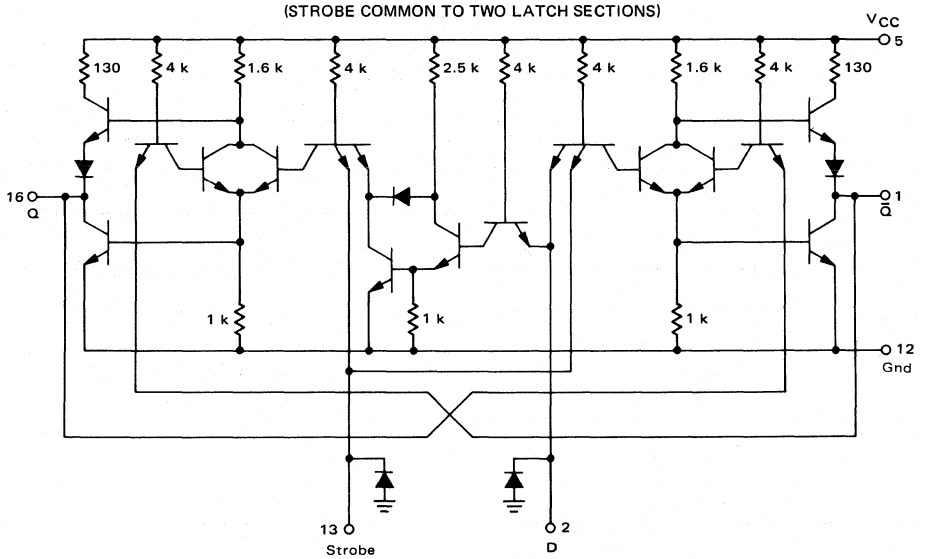
LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN; STROBE COMMON TO TWO LATCH SECTIONS)



V_{CC} = Pin 5
Gnd = Pin 12
16–Pin Package

* P suffix = 16-pin plastic package (Case 612)
See General Information section for package outline dimensions.

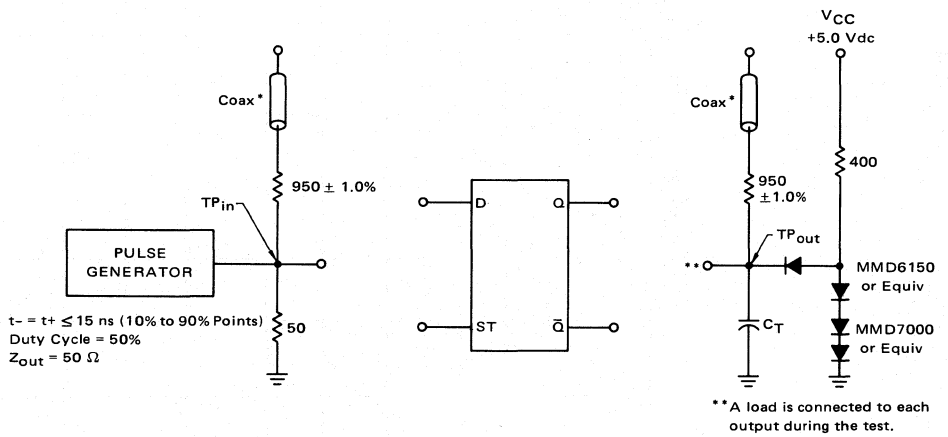
1/4 OF CIRCUIT SHOWN
(STROBE COMMON TO TWO LATCH SECTIONS)



OPERATING CHARACTERISTICS

Data present on the D input between the setup and hold times will be transferred to the Q output when the strobe input changes from the logic "0" state to the logic "1" state. As long as the strobe remains in the logic "1" state, the Q output will follow the state of the D input. When the strobe input changes from the logic "1" state to the logic "0" state, data present on the D input between the setup and hold times will be retained on the Q output until the strobe returns to the logic "1" state.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

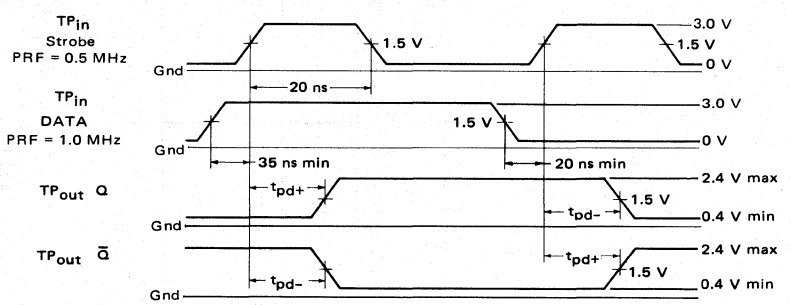


**A load is connected to each output during the test.

Two pulse generators are required and must be slaved together to provide the waveforms shown.

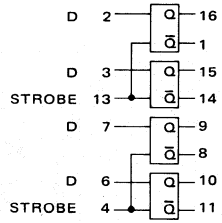
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.



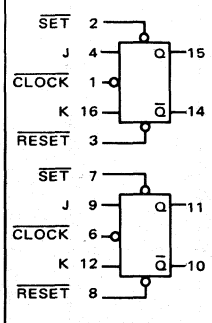
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one latch. The other latches are tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC7475 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
						I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	
Input																	
Forward Current	I_F	2	-	-3.2	mAdc	-	-	2	-	-	13	-	-	-	-	5	12
		13	-	-3.2	mAdc	-	-	13	-	-	-	-	-	-	-	5	12
Leakage Current	I_{R1}	2	-	80	μAdc	-	-	-	2	-	-	-	-	-	-	5	12,13
		13	-	80	μAdc	-	-	-	13	-	-	-	-	-	-	5	2,3,12
	I_{R2}	2	-	1.0	mAdc	-	-	-	-	2	-	-	-	-	-	5	12,13
		13	-	1.0	mAdc	-	-	-	-	13	-	-	-	-	-	5	2,3,12
Output																	
Output Voltage	V_{OL}	1	-	0.4	Vdc	1	-	-	-	-	-	2,13	-	-	5	-	12
		16	-	0.4	Vdc	16	-	-	-	-	-	13	2	-	5	-	12
	V_{OH}	1	2.4	-	Vdc	-	1	-	-	-	-	13	2	-	5	-	12
		16	2.4	-	Vdc	-	16	-	-	-	-	2,13	-	-	5	-	12
Short-Circuit Current	I_{SC}	1	-18	-57	mAdc	-	-	-	-	-	13	-	-	-	-	5	1,2,12
		16	-18	-57	mAdc	-	-	-	-	-	2,13	-	-	-	-	5	12,16
Power Requirements (Total Device)																	
Power Supply Drain	I_{PD}	5	-	49	mAdc	-	-	-	-	-	-	-	-	5	-	-	2,3,4,6,7,12,13

MC7476P*



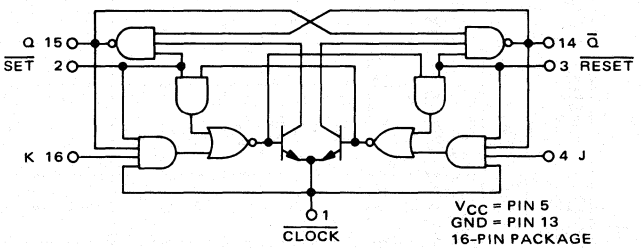
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Input Loading Factor:
J, K = 1
CLOCK, SET, RESET = 2

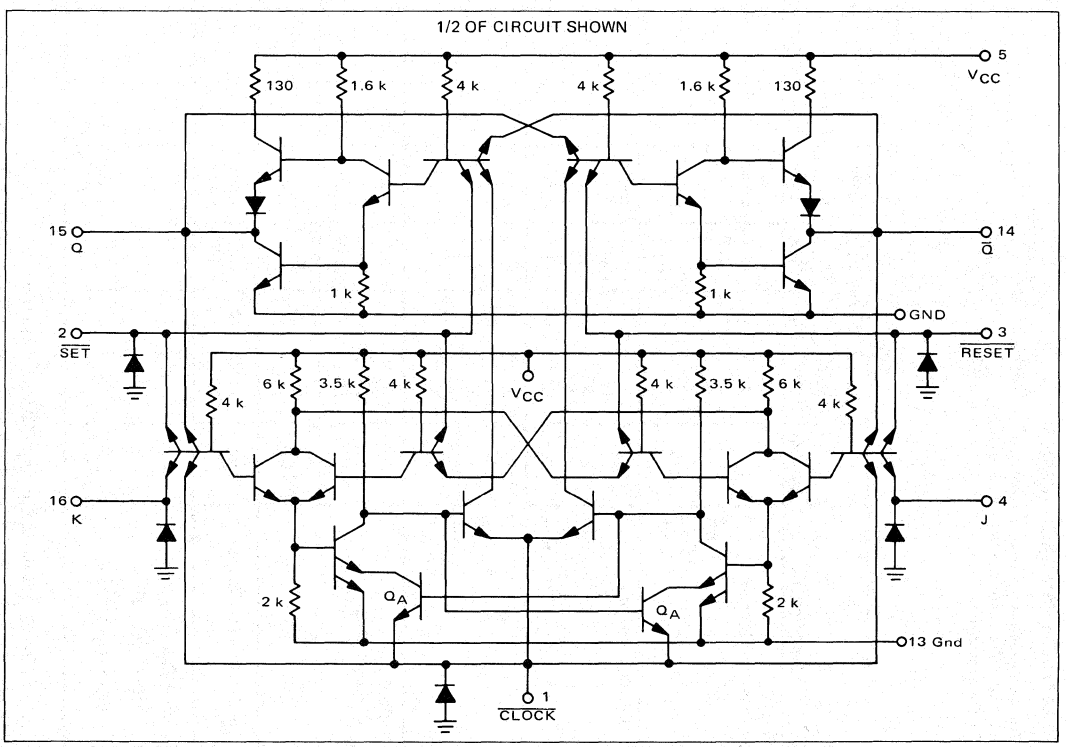
Output Loading Factor = 10
Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 30 ns typ
Operating Frequency = 15 MHz typ

This negative-edge-clocked dual J-K flip-flop operates on the master-slave principle. The device is quite useful for simple registers and counters where multiple J and K inputs are not required. Available only in the 16-pin package, this device provides both SET and RESET inputs on both flip-flops in the package.

LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

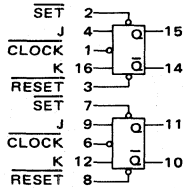


* P suffix = 16-pin plastic package (Case 612)
See General Information section for package outline dimensions.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC7476 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
Input																	
Forward Current J	I_F	4	-	-1.6	mAdc	-	-	4	-	-	1,3*	-	-	-	-	5	6,9,12,13
K		16	-	-1.6		-	-	16	-	-	1,2*	-	-	-	-		
$\overline{\text{Set}}$		2	-	-3.2		-	-	2	-	-	4,16	-	-	-	-		
$\overline{\text{Reset}}$		3	-			-	-	3	-	-	4,16	-	-	-	-		
$\overline{\text{Clock}}$		1	-			-	-	1	-	-	2*,4,16	-	-	-	-		
		1	-			-	-	1	-	-	3*,4,16	-	-	-	-		
Leakage Current J	I_{R1}	4	-	40	μAdc	-	-	-	4	-	-	-	-	-	-	5	1,3,6,9,12,13
K		16	-	40		-	-	-	16	-	-	-	-	-	-		1,2,6,9,12,13
$\overline{\text{Set}}$		2	-	80		-	-	-	2	-	-	-	-	-	-		1,6,9,12,13,16
$\overline{\text{Reset}}$		3	-			-	-	-	3	-	-	-	-	-	-		1,4,6,9,12,13
$\overline{\text{Clock}}$		1**	-			-	-	-	1	-	-	-	-	-	-		2,3,4,6,9,12,13,16
J	I_{R2}	4	-	1.0	mAdc	-	-	-	-	4	-	-	-	-	-	5	1,3,6,9,12,13
K		16	-			-	-	-	-	16	-	-	-	-	-		1,2,6,9,12,13
$\overline{\text{Set}}$		2	-			-	-	-	-	2	-	-	-	-	-		1,6,9,12,13,16
$\overline{\text{Reset}}$		3	-			-	-	-	-	3	-	-	-	-	-		1,4,6,9,12,13
$\overline{\text{Clock}}$		1	-			-	-	-	-	1	-	-	-	-	-		2,3,4,6,9,12,13,16
Output																	
Output Voltage	V_{OL}	14	-	0.40	Vdc	14	-	-	-	-	-	3	2	-	5	-	6,9,12,13
		15	-	0.40	Vdc	15	-	-	-	-	-	2	3	-	5	-	6,9,12,13
	V_{OH}	14	2.4	-	Vdc	-	14	-	-	-	-	2	3	-	5	-	6,9,12,13
		15	2.4	-	Vdc	-	15	-	-	-	-	3	2	-	5	-	6,9,12,13
Short-Circuit Current	I_{SC}	14	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	5	3,6,9,12,13,14
		15	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	5	2,6,9,12,13,15
Power Requirements (Total Device)																	
Power Supply Drain	I_{PD}	5	-	32	mAdc	-	-	-	-	-	-	-	-	5	-	-	2,7,13
		5	-	32	mAdc	-	-	-	-	-	-	-	-	5	-	-	3,8,13

*Momentarily ground pin prior to taking measurement.

**Under normal operating conditions this current is negative. This test guarantees that positive leakage will not exceed the limit shown.

OPERATING CHARACTERISTICS

Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{\text{RESET}}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{\text{RESET}}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 20 ns minimum.

Transistors Q_A have been added to the standard flip-flop circuit to protect the device against negative clock transients. This addition prevents both outputs from changing to the logic "1" state when transients in excess of -2.0 V appear at the clock.

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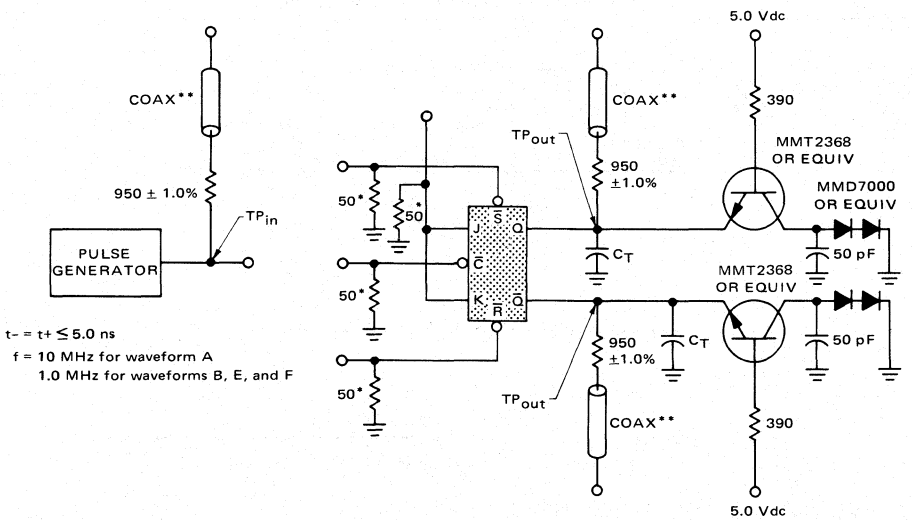
SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved together for testing $\overline{\text{SET}}$ and $\overline{\text{RESET}}$. Only one pulse generator is required for J, K, and $\overline{\text{CLOCK}}$ tests.

*Resistor used only when that input is under test.

**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

OPERATING CHARACTERISTICS (continued)

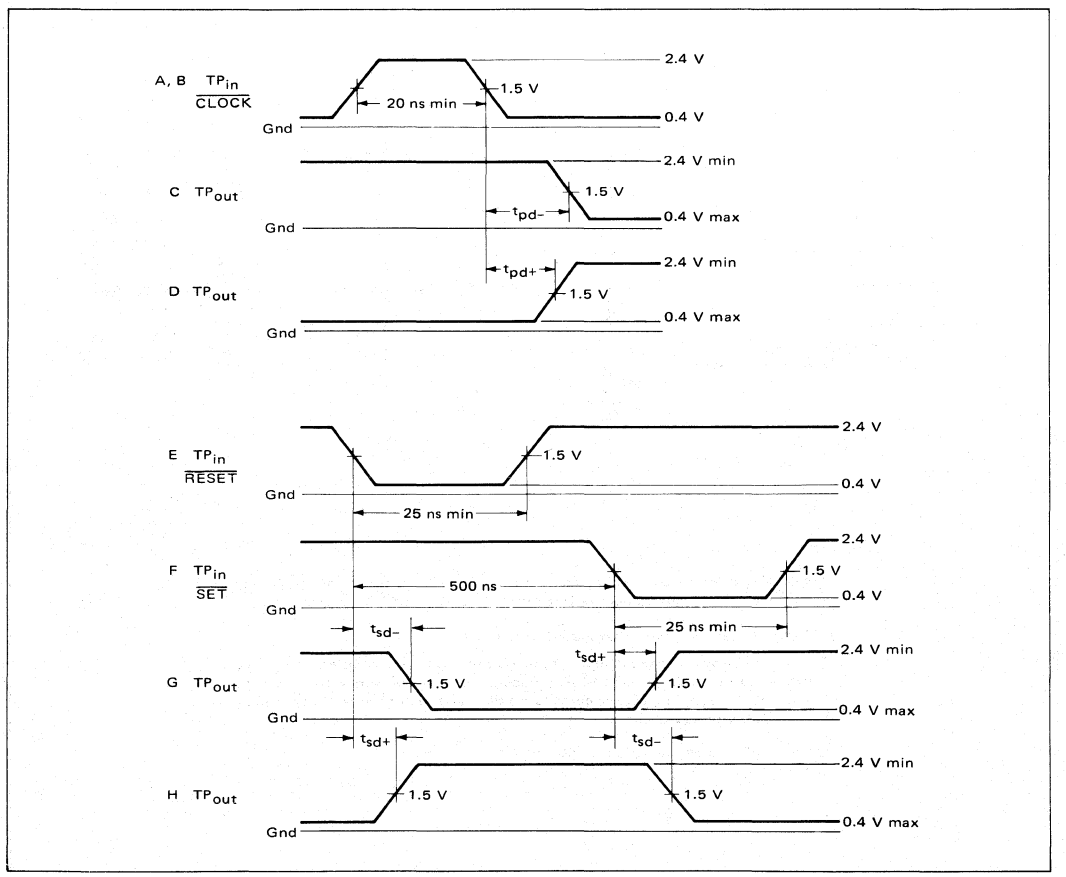
TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				Q	$\overline{Q}$	LIMITS		
		$\overline{C}$	J, K	$\overline{R}$	$\overline{S}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	A	2.4 V	2.4 V	†	†	10	–	MHz
Turn-On Delay	t_{pd-}	B	B	2.4 V	2.4 V	C	C	–	50	ns
Turn-Off Delay	t_{pd+}	B	B	2.4 V	2.4 V	D	D	–	50	ns
Turn-On Delay	t_{sd-}	2.4 V	2.4 V	E	F	G	H	10	50	ns
Turn-Off Delay	t_{sd+}	2.4 V	2.4 V	E	F	G	H	10	50	ns
Enable Voltage	V_{EN}	B	2.0 V	2.4 V	2.4 V	†	†	†	–	–
Inhibit Voltage	V_{INH}	B	0.8 V	2.4 V	2.4 V	‡	‡	‡	–	–

†Output shall toggle with each input pulse.
‡Output shall NOT toggle.

VOLTAGE WAVEFORMS AND DEFINITIONS

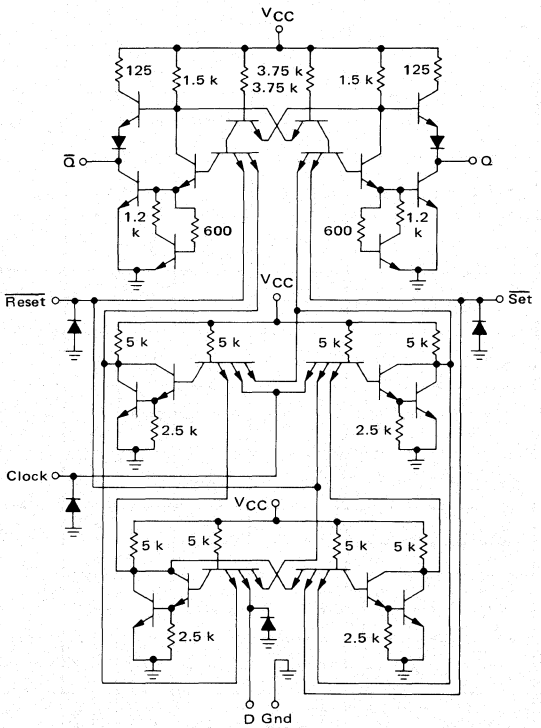


DUAL TYPE D FLIP-FLOP

MC5479 • MC7479

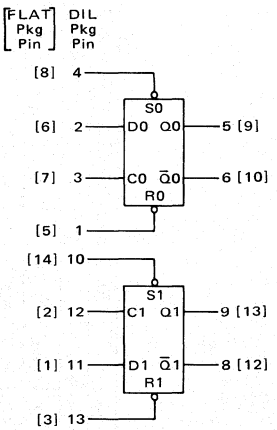
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7479 only.)

CIRCUIT SCHEMATIC
1/2 OF DEVICE SHOWN



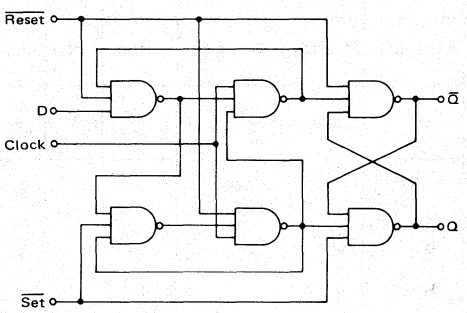
V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

This dual type D flip-flop triggers on the positive edge of the clock input. During the clock transition the state of the D input is transferred to the Q output. The device is useful in shift registers and simple counters.



t_n	t_{n+1}	
D	Q	$\bar{Q}$
0	0	1
1	1	0

Input Loading Factor:
D = 1
$\overline{Set}$, Clock = 2
$\overline{Reset}$ = 3
Output Loading Factor = 10
Total Power Dissipation = 84 mW typ/pkg
Propagation Delay Time = 16 ns typ
Operating Frequency = 30 MHz typ

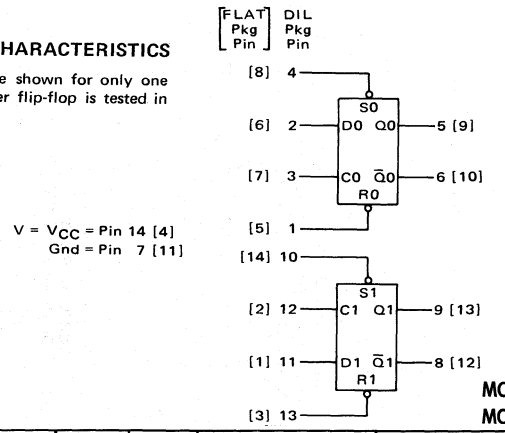


LOGIC DIAGRAM
1/2 OF DEVICE SHOWN

12

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA		Volts								
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}
MC5479	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.50	5.50
MC7479	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5479 Test Limits −55 to +125°C Min	Max	Unit	MC7479 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Pin 7[11] is grounded for all tests in addition to the pins listed below: Gnd
Input																				
Forward Current D	I_F	D	-	-1.6	mAdc	-	-1.6	mAdc	-	-	D	-	-	R,S	-	-	-	-	V	C0,C1
$\overline{\text{Set}}$		S	-	-3.2	↓	-	-3.2	↓	-	-	S	-	-	R	-	-	-	-	↓	C0,C1,D0
$\overline{\text{Reset}}$		R	-	↓	↓	-	↓	↓	-	-	R	-	-	D,S	-	-	-	-	↓	C0,C1
Clock		C	-	↓	↓	-	↓	↓	-	-	C	-	-	R	-	-	-	-	↓	C1,D0,S0
Leakage Current D	I_{R1}	D	-	40	μAdc	-	40	μAdc	-	-	-	D	-	C,S	-	-	-	-	V	C1,R0
$\overline{\text{Set}}$		S	-	80	↓	-	80	↓	-	-	-	S	-	C*,D,R	-	-	-	-	↓	C1
$\overline{\text{Reset}}$		R	-	120	↓	-	120	↓	-	-	-	R	-	C*,S	-	-	-	-	↓	C1, D0
Clock		C	-	80	↓	-	80	↓	-	-	-	C	-	S	-	-	-	-	↓	C1,D0,R0
D	I_{R2}	D	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	D	C,S	-	-	-	-	V	C1,R0
$\overline{\text{Set}}$		S	-	↓	↓	-	↓	↓	-	-	-	-	S	C*,D,R	-	-	-	-	↓	C1
$\overline{\text{Reset}}$		R	-	↓	↓	-	↓	↓	-	-	-	-	R	C*,S	-	-	-	-	↓	C1,D0
Clock		C	-	↓	↓	-	↓	↓	-	-	-	-	C	S	-	-	-	-	↓	C1,D0,R0
Output																				
Output Voltage	V_{OL}	Q	-	0.4	Vdc	-	0.4	Vdc	Q	-	-	-	-	-	S	R	-	V	-	C0,C1,D0
		$\bar{Q}$	-	0.4	Vdc	-	0.4	Vdc	$\bar{Q}$	-	-	-	-	-	R	S	-	V	-	C0,C1,D0
	V_{OH}	Q	2.4	-	Vdc	2.4	-	Vdc	-	Q	-	-	-	-	R	S	-	V	-	C0,C1,D0
		$\bar{Q}$	2.4	-	Vdc	2.4	-	Vdc	-	$\bar{Q}$	-	-	-	-	S	R	-	V	-	C0,C1,D0
Short-Circuit Current	I_{SC}†	Q	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	V	C0,S0,Q0
		$\bar{Q}$	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	V	C1,R0,Q0
Power Requirements (Total Device)																				
Power Supply Drain	I_{PD}	V	-	30	mAdc	-	30	mAdc	-	-	-	-	-	-	-	-	-	-	V	C0,C1,D0,D1,S0,S1
		V	-	30	mAdc	-	30	mAdc	-	-	-	-	-	-	-	-	-	-	V	C0,D0,R0,C1,D1,R1

*Momentarily ground pin prfor to taking measurement, then set to state indicated.

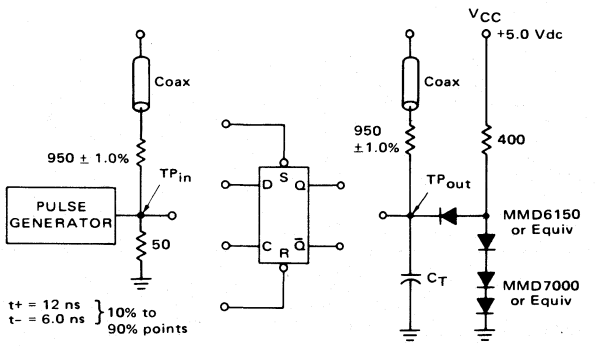
†Only one output should be shorted at a time.

OPERATING CHARACTERISTICS

Data may be applied to the D input any time following 5.0 ns after the leading edge of a clock pulse and 20 ns before the leading edge of the following clock pulse. The state of the D input when the clock changes from the positive logic "0" state to the positive logic "1" state is transferred to the Q output of the flip-flop. The data input cannot be changed between the setup time (20 ns) and the hold time (5.0 ns) without adversely affecting the operation of the flip-flop.

The direct $\overline{\text{Set}}$ and $\overline{\text{Reset}}$ inputs override the clock, and may be applied any time during the operating cycle.

SWITCHING TIME TEST CIRCUIT



PRF = 20 MHz for waveform 1
= 1.0 MHz for waveforms 2 thru 5

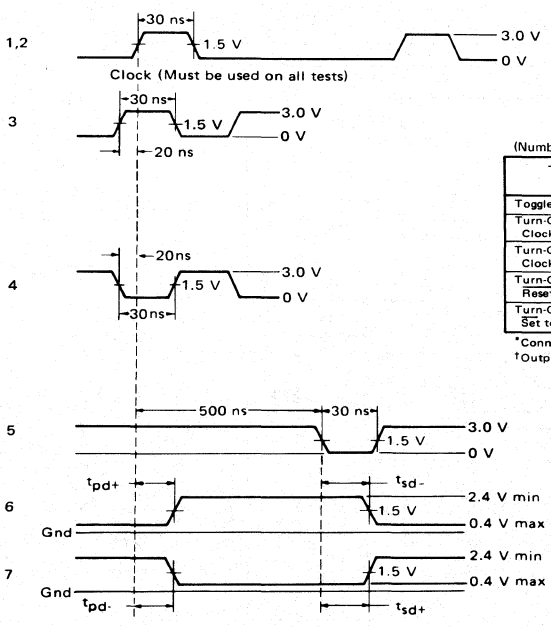
$Z_{out} \approx 50\ \Omega$

Two pulse generators are required and must be slaved together to provide the waveforms shown. Only one pulse generator (duty cycle = 50%) is required to test toggle frequency.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

(Numbers shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				Q	Q̄	LIMITS		
		C	D	R̄	S̄			Min	Max	Unit
Toggle Frequency	f_{Tog}	1	*	2.4 V	2.4 V	†	†	20	–	MHz
Turn-On Delay Clock to Q	t_{pd-}	2	4	2.4 V	2.4 V	7	6	–	30	ns
Turn-Off Delay Clock to Q	t_{pd+}	2	3	2.4 V	2.4 V	6	7	–	30	ns
Turn-On Delay Reset to Q	t_{sd-}	2	3	5	2.4 V	7	6	–	25	ns
Turn-Off Delay Set to Q	t_{sd+}	2	4	2.4 V	5	6	7	–	25	ns

*Connect to Q̄.

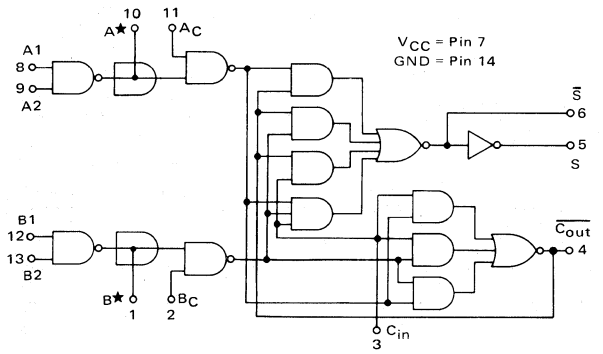
†Output shall toggle with each input pulse.

GATED FULL ADDER

MC5480L*
MC7480L, P*

The MC5480/7480 is a one-bit binary full adder with gated complementary inputs, complementary Sum and $\overline{\text{Sum}}$ outputs, and an inverted Carry output. The circuit uses DTL inputs and a high-speed, high-fan-out, TTL "totem pole" configuration for the Sum, $\overline{\text{Sum}}$, and Carry outputs. The design of the high-speed carry circuitry reduces the need for external "look ahead carry" cascading in system designs. The use of low-level, low-power gates in a monolithic design provides significantly lower power dissipation than equivalent adders built from standard integrated circuits.

This full adder provides a basic building block for medium and high-speed, multiple-bit, parallel-add/serial-carry subsystems.



Input Loading Factor:

A1, A2, A_C, B1, B2, B_C = 1

A★, B★ = 1.625

C_{in} = 5

Output Loading Factor:

$\overline{C_{out}}$ = 5

S, $\bar{S}$ = 10

A★, B★ = 3

TRUTH TABLE

C_{in}	B	A	$\overline{C_{out}}$	$\bar{S}$	S
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

1. $A = \overline{A★ \cdot A_C}$, $B = \overline{B★ \cdot B_C}$

   where $A★ = \overline{A_1 \cdot A_2}$

   $B★ = \overline{B_1 \cdot B_2}$

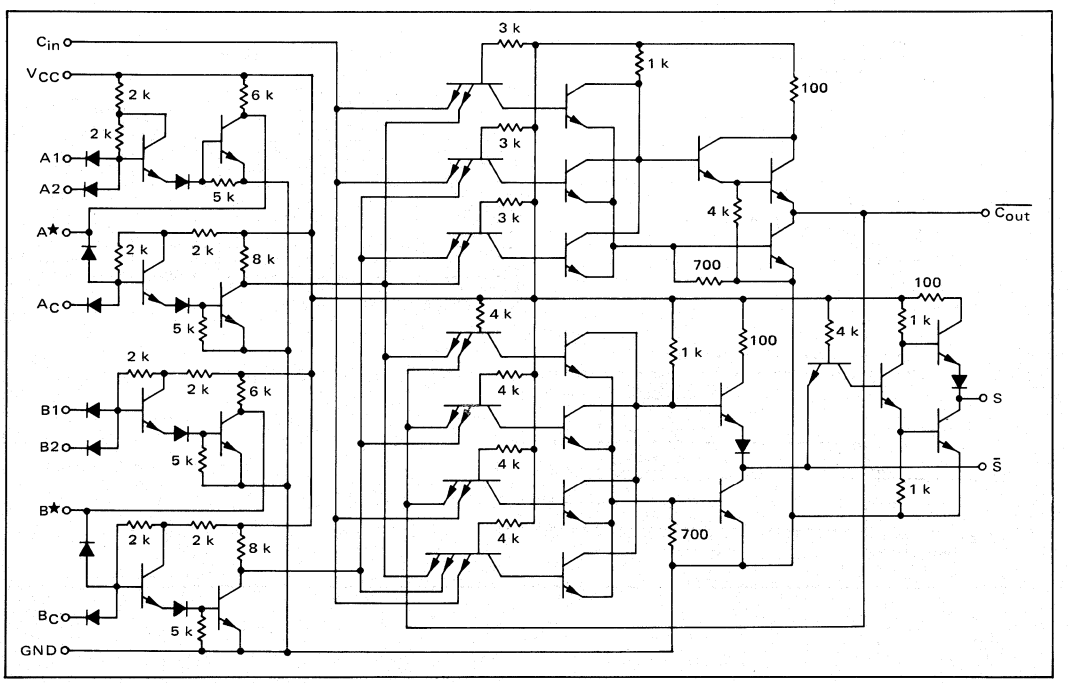
2. When A★ (or B★) is used as an input, A1 and A2 (or B1 and B2) must be connected to ground.
3. When A1 and A2 (or B1 and B2) are used as inputs, A★ (or B★) must be open, or used to perform wired-OR logic.

Total Power Dissipation = 105 mW typ/pkg

Propagation Delay Time:

Carry Delay = 10 ns typ

Add Delay = 55 ns typ



*L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

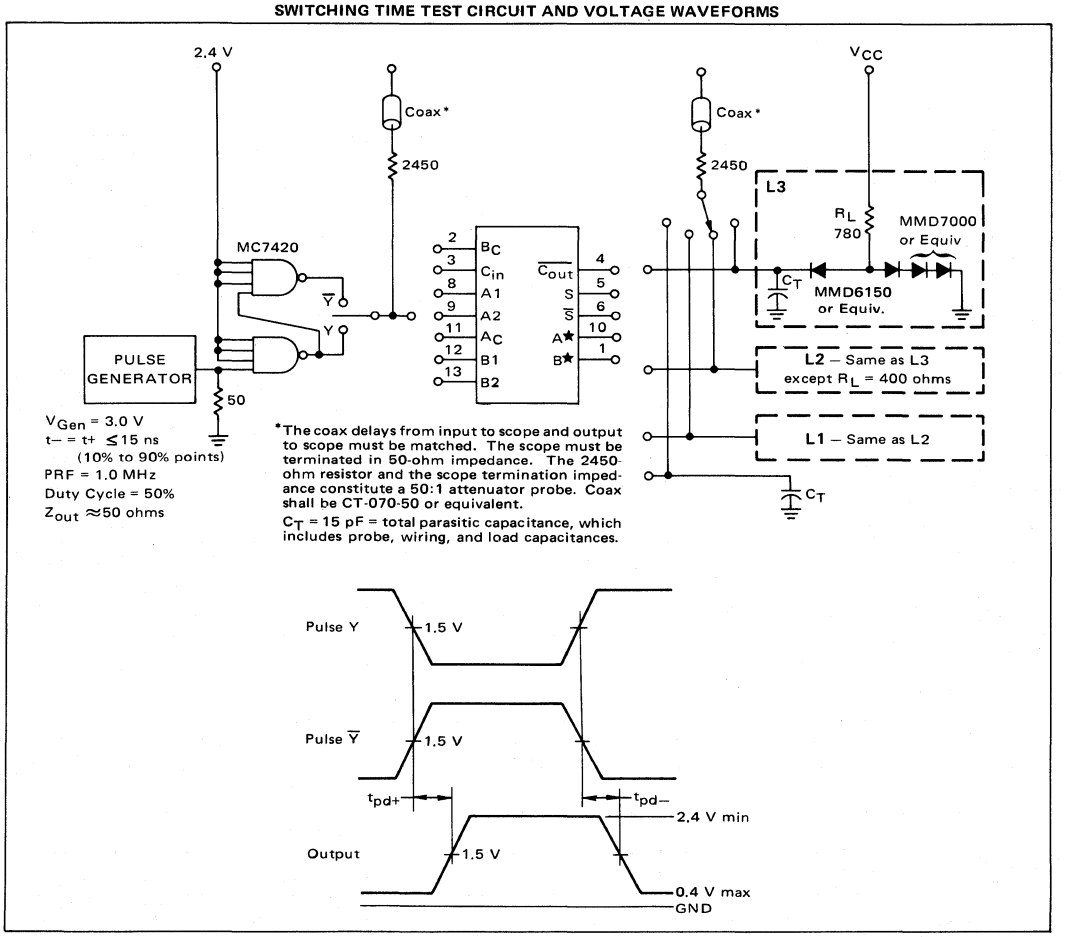
Output voltage (logic level) tests are shown only for each output. The complete circuit can be tested by following the truth table.

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)													
	mA						Volts							
	I_{OL1}	I_{OL2}	I_{OL3}	I_{OH1}	I_{OH2}	I_{OH3}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CCL}	V_{CCH}
MC5480	4.8	8.0	16	-0.12	-0.2	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	4.5	5.5
MC7480	4.8	8.0	16	-0.12	-0.2	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5480 Test Limits −55 to +125°C Min	Max	Unit	MC7480 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OH1}	I_{OH2}	I_{OH3}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CCL}	V_{CCH}	Gnd
Input																							
Forward Current B✱	I_F	1	-	-2.6	mAdc	-	-2.6	mAdc	-	-	-	-	-	-	1	-	-	2	-	-	-	14	7, 12, 13
B_C		2	-	-1.6		-	-1.6		-	-	-	-	-	-	2	-	-	-	-	-	-		7, 12, 13
C_{in}		3	-	-8.0		-	-8.0		-	-	-	-	-	-	3	-	-	-	-	-	-		7
A1		8	-	-1.6		-	-1.6		-	-	-	-	-	-	8	-	-	9	-	-	-		
A2		9	-	-1.6		-	-1.6		-	-	-	-	-	-	9	-	-	8	-	-	-		
A✱		10	-	-2.6		-	-2.6		-	-	-	-	-	-	10	-	-	11	-	-	-		7, 8, 9
A_C		11	-	-1.6		-	-1.6		-	-	-	-	-	-	11	-	-	-	-	-	-		7, 8, 9
B1		12	-	↓	↓	-	↓	↓	-	-	-	-	-	-	12	-	-	13	-	-	-		7
B2		13	-			-			-	-	-	-	-	-	13	-	-	12	-	-	-	↓	7
Leakage Current B_C	I_{R1}	2	-	15	μAdc	-	15	μAdc	-	-	-	-	-	-	-	2	-	-	-	-	-	14	1, 7
C_{in}		3	-	200		-	200		-	-	-	-	-	-	-	3	-	-	-	-	-		7, 8, 9, 12, 13
A1		8	-	15		-	15		-	-	-	-	-	-	-	8	-	-	-	-	-		7, 9
A2		9	-	↓		-	↓		-	-	-	-	-	-	-	9	-	-	-	-	-		7, 8
A_C		11	-			-			-	-	-	-	-	-	-	11	-	-	-	-	-		7, 10
B1		12	-			-			-	-	-	-	-	-	-	12	-	-	-	-	-		7, 13
B2		13	-	↓	↓	-	↓	↓	-	-	-	-	-	-	-	13	-	-	-	-	-	↓	7, 12
B_C	I_{R2}	2	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	-	-	-	-	2	-	-	-	-	14	1, 7
C_{in}		3	-	↓	↓	-	↓	↓	-	-	-	-	-	-	-	-	3	-	-	-	-		7, 8, 9, 12, 13
A1		8	-			-			-	-	-	-	-	-	-	-	8	-	-	-	-		7, 9
A2		9	-			-			-	-	-	-	-	-	-	-	9	-	-	-	-		7, 8
A_C		11	-			-			-	-	-	-	-	-	-	-	11	-	-	-	-		7, 10
B1		12	-			-			-	-	-	-	-	-	-	-	12	-	-	-	-		7, 13
B2		13	-	↓	↓	-	↓	↓	-	-	-	-	-	-	-	-	13	-	-	-	-	↓	7, 12
Output																							
Output Voltage A✱	V_{OL}	1	-	0.4	Vdc	-	0.4	Vdc	1	-	-	-	-	-	-	-	-	-	12, 13	-	14	-	7
$\overline{C}_{out}$		4	-	↓	↓	-	↓	↓	-	4	-	-	-	-	-	-	-	-	8, 12	2,3,9,11,13	-	-	
S		5	-			-			-	-	5	-	-	-	-	-	-	-	2, 11	3,8,9,12,13	-	-	
$\overline{S}$		6	-			-			-	-	6	-	-	-	-	-	-	-	2,3,8,11,12	9, 13	-	-	
B✱		10	-	↓	↓	-	↓	↓	10	-	-	-	-	-	-	-	-	-	8, 9	-	-	↓	
A✱	V_{OH}	1	2.4	-	Vdc	2.4	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	12,13	14	-	7
$\overline{C}_{out}$		4	↓	-	↓	↓	-	↓	-	-	-	-	4	-	-	-	-	-	2, 11	3,8,9,12,13	-	-	
S		5		-			-		-	-	-	-	-	5	-	-	-	-	2, 9, 13	3,8,11,12	-	-	
$\overline{S}$		6		-			-		-	-	-	-	-	6	-	-	-	-	3, 10, 11	1,2,8,9,12,13	-	-	
B✱		10	↓	-	↓	↓	-	↓	-	-	-	10	-	-	-	-	-	-	-	8, 9	↓	-	↓	
Short-Circuit Current	I_{SC}																						
$\overline{C}_{out}$		4	-20	-70	mAdc	-18	-70	mAdc	-	-	-	-	-	-	-	-	-	2,3,8,11,12	-	-	-	14	4,7,9,13
S		5	↓	-57	↓	↓	-57	↓	-	-	-	-	-	-	-	-	-	2,9,13	-	-	-		3,5,7,8,11,12
$\overline{S}$		6	↓	-57	↓	↓	-57	↓	-	-	-	-	-	-	-	-	-	3,10,13	-	-	-	↓	1,2,6,7,8,9,12,13
Power Requirements																							
Power Supply Drain	I_{PD}	14	-	31**	mAdc		35**	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	14	7

**Tested only at 25°C.

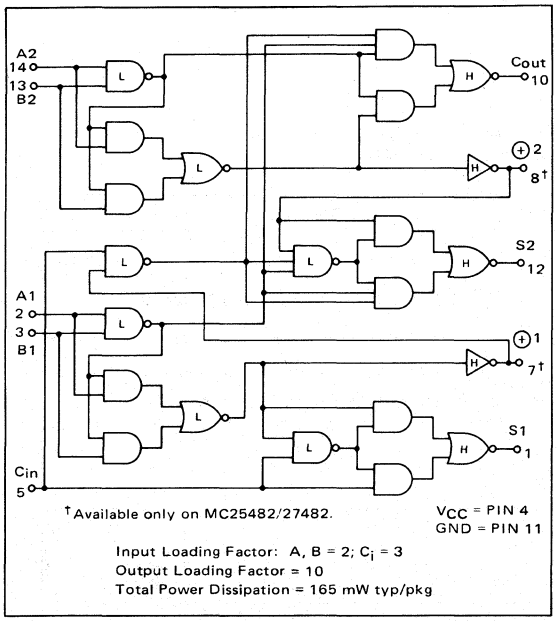
SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



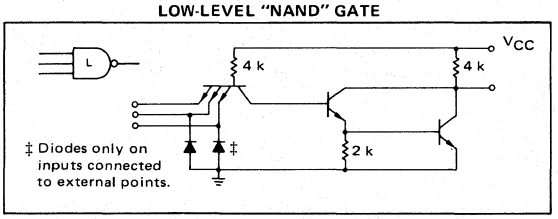
TEST PROCEDURES (T_A = 25°C)

TEST	PIN UNDER TEST	INPUT B_C Pin 2	C_{in} Pin 3	A1 Pin 8	A2 Pin 9	A_C Pin 11	B1 Pin 12	B2 Pin 13	OUTPUT $\overline{C_{out}}$ Pin 4	S Pin 5	$\overline{S}$ Pin 6	A★ Pin 10	B★ Pin 1	MAX LIMIT
t_{pd+} $\overline{C_{out}}$	4	–	Y	–	–	–	Gnd	–	L3	–	–	–	–	17 ns
t_{pd-} $\overline{C_{out}}$	4	–	Y	–	–	–	Gnd	–	L3	–	–	–	–	12 ns
t_{pd+} $\overline{C_{out}}$	4	$\overline{Y}$	2.4 V	Gnd	–	–	Gnd	–	L3	–	–	–	–	25 ns
t_{pd-} $\overline{C_{out}}$	4	$\overline{Y}$	2.4 V	Gnd	–	–	Gnd	–	L3	–	–	–	–	55 ns
t_{pd+} S	5	–	2.4 V	Gnd	–	$\overline{Y}$	Gnd	–	L3	L1	L2	–	–	70 ns
t_{pd-} S	5	–	2.4 V	Gnd	–	$\overline{Y}$	Gnd	–	L3	L1	L2	–	–	80 ns
t_{pd+} $\overline{S}$	6	$\overline{Y}$	2.4 V	–	–	–	Gnd	–	–	–	L2	–	–	55 ns
t_{pd-} $\overline{S}$	6	$\overline{Y}$	2.4 V	–	–	–	Gnd	–	–	–	L2	–	–	75 ns
t_{pd+} A★	10	–	–	Y	2.4 V	–	–	–	–	–	–	C_T	–	65 ns
t_{pd-} A★	10	–	–	Y	2.4 V	–	–	–	–	–	–	C_T	–	25 ns
t_{pd+} B★	1	–	–	–	–	–	Y	2.4 V	–	–	–	–	C_T	65 ns
t_{pd-} B★	1	–	–	–	–	–	Y	2.4 V	–	–	–	–	C_T	25 ns

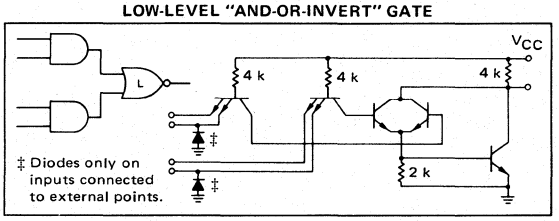
MC15482L • MC17482L*
MC25482L • MC27482L*



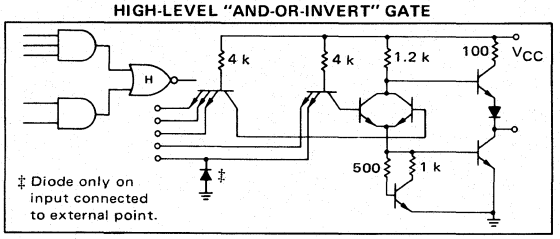
LOW-LEVEL "NAND" GATE



LOW-LEVEL "AND-OR-INVERT" GATE



HIGH-LEVEL "AND-OR-INVERT" GATE



*L suffix = TO-116 ceramic dual in-line package (Case 632).

ADVANCE INFORMATION/NEW PRODUCT

Each bit of this device performs the logical addition of two binary numbers. The sum outputs, the carry output for the second bit, and Exclusive OR outputs for each bit are available. A look-ahead carry is provided internally. The Exclusive OR outputs of the MC25482/MC27482 can be used for look-ahead carry when adding more than two bits.

This device is constructed from low and high-level NAND and AND-OR-INVERT gates as shown in the logic diagram to maximize output drive capability and minimize power dissipation.

TRUTH TABLE

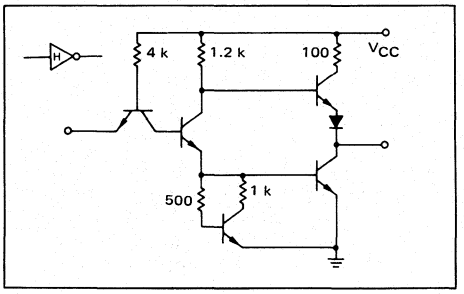
INPUT				OUTPUT							
				C_{in} = 0			C_{in} = 1				
A1	B1	A2	B2	S1	S2	C_o	S1	S2	C_o	⊕1†	⊕2†
0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	1	0	1	0
0	1	0	0	1	0	0	0	1	0	1	0
1	1	0	0	0	1	0	1	1	0	0	0
0	0	1	0	0	1	0	1	1	0	0	1
1	0	1	0	1	1	0	0	0	1	1	1
0	1	1	0	1	1	0	0	0	1	1	1
1	1	1	0	0	0	1	1	0	1	0	1
0	0	0	1	0	1	0	1	1	0	0	1
1	0	0	1	1	1	0	0	0	1	1	1
0	1	0	1	1	1	0	0	0	1	1	1
1	1	0	1	0	0	1	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	0	0
1	0	1	1	1	0	1	0	1	1	1	0
0	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	0	1	1	1	1	1	0	0

†Available only on MC25482/27482.

TYPICAL PROPAGATION DELAY TIMES
T_A = 25°C

	t_{pd-} (ns)				t_{pd+} (ns)			
	OUTPUT				OUTPUT			
INPUT	S1	S2	C_o	⊕	S1	S2	C_o	⊕
B2	–	18.5	–	9.5	–	27	–	14
C_i	5.5	13	9.5	–	9.0	18.5	14	–

HIGH-LEVEL INVERTER



DC ELECTRICAL CHARACTERISTICS

T_A = 0 to +70°C for MC17482 and MC27482
T_A = -55 to +125°C for MC15482 and MC25482

Characteristic	Symbol	Value	Conditions
Input			
Forward Current — A, B	I_F	-3.2 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 5.5 Vdc ① or 5.25 Vdc ②
C_i		-4.8 mAdc max	
Leakage Current — A, B	I_R	80 μAdc max	V_{in} = 2.4 Vdc, V_{CC} = 5.5 Vdc ① or 5.25 Vdc ②
C_i		120 μAdc max	
A, B, C_i		1.0 mAdc max	V_{in} = 5.5 Vdc, V_{CC} = 5.5 Vdc ① or 5.25 Vdc ②
Threshold Voltage	V_{th} "1"	2.0 Vdc	
	V_{th} "0"	0.8 Vdc	
Output			
Output Voltage	V_{OL}	0.4 Vdc max	I_{OL} = 16 mAdc, V_{CC} = 4.5 Vdc ① or 4.75 Vdc ② — Tested according to truth table. Logical "1" = V_{th} "0"; Logical "0" = V_{th} "1".
	V_{OH}	2.4 Vdc min	I_{OH} = -400 μAdc, V_{CC} = 4.5 Vdc ① or 4.75 Vdc ② — Tested according to truth table. Logical "1" = V_{th} "0"; Logical "0" = V_{th} "1".
Short-Circuit Current	I_{SC}	① -20 to -57 mAdc ② -18 to -57 mAdc	V_{CC} = 5.5 Vdc, output grounded. Tested according to truth table. Logical "1" = 4.5 Vdc; Logical "0" = Gnd.

① MC15482, MC25482
② MC17482, MC27482

4-BIT BINARY
FULL ADDER

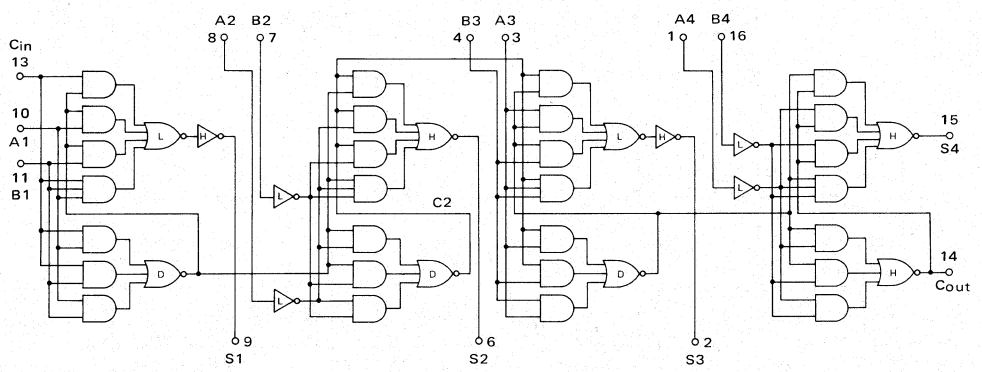
MC5483L*
MC7483L,P*

INPUT				OUTPUT					
				When $C_{in}=0$			When $C_{in}=1$		
				When C2 = 0			When C2 = 1		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	S1 / S3	S2 / S4	C2 / C_o	S1 / S3	S2 / S4	C2 / C_o
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

This device performs the logical addition of two 4-bit binary numbers. The Sum outputs for each bit and the Carry from the fourth bit (C4) are provided. A look-ahead carry is provided internally, utilizing a Darlington-connected serial carry within each bit.

Low and high-level inverters and gates are used in the construction of the MC5483/7483 to maximize output drive capability and minimize power dissipation.

Input conditions at A1, A2, B1, B2, and C_{in} are used to determine outputs S1 and S2, and the value of the internal carry, C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs S3, S4, and C_{out}.



V_{CC} = Pin 5
Gnd = Pin 12

Input Loading Factor:
A1, A3, B1, B3, C0 = 4
A2, A4, B2, B4 = 1

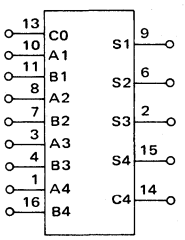
Output Loading Factor:
S1, S2, S3, S4 = 10
C_{out} = 5

Total Power Dissipation = 390 mW typ/pkg
Propagation Delay Time = 35 ns typ

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one set of input conditions. To complete testing, sequence through remaining input conditions according to the truth table.

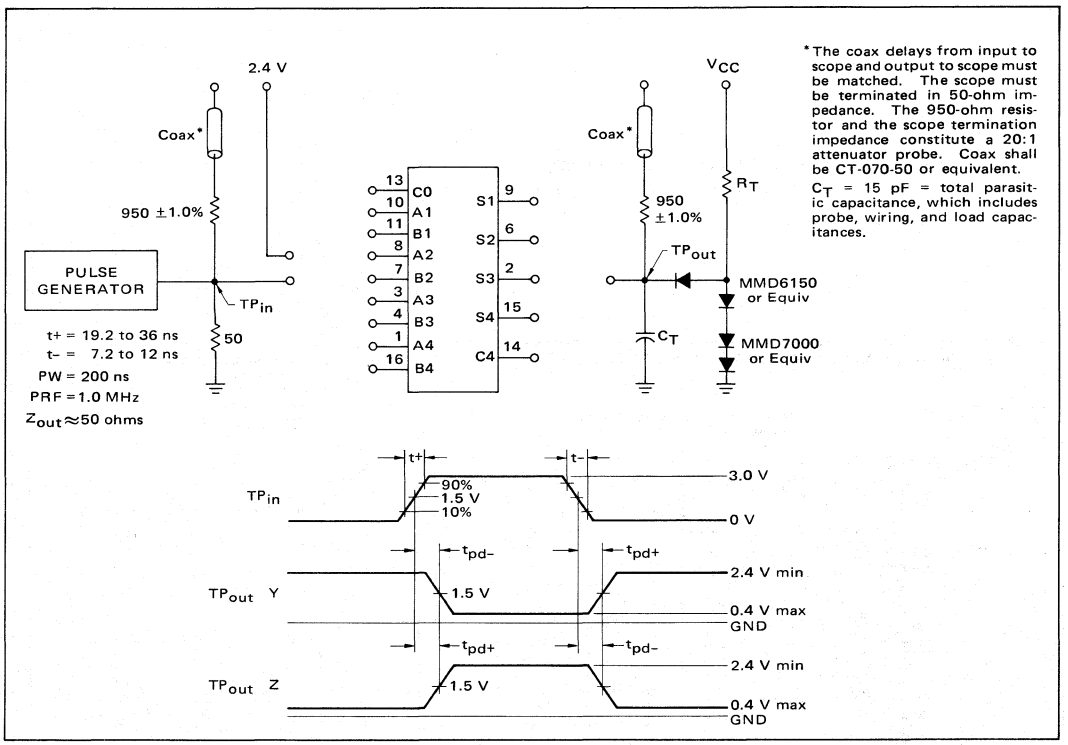


	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA				Volts							
	I_{OL1}	I_{OL2}	I_{OH1}	I_{OH2}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CCL}	V_{CCH}
MC5483	16	8.0	-0.4	-0.2	0.4	2.4	5.5	4.5	2.0	0.8	4.5	5.5
MC7483	16	8.0	-0.4	-0.2	0.4	2.4	5.5	4.5	2.0	0.8	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5483 Test Limits -55 to +125°C Min	Max	Unit	MC7483 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH1}	I_{OH2}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_F	1	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	–	1	–	–	–	–	–	–	5	12
		3	–	-6.4		–	-6.4		–	–	–	–	3	–	–	4,7,8	–	–	–		
		4	–	-6.4		–	-6.4		–	–	–	–	4	–	–	3,7,8	–	–	–		
		7	–	-1.6		–	-1.6		–	–	–	–	7	–	–	–	–	–	–		
		8	–	-1.6		–	-1.6		–	–	–	–	8	–	–	–	–	–	–		
		10	–	-6.4		–	-6.4		–	–	–	–	10	–	–	11,13	–	–	–		
		11	–	↓		–	↓		–	–	–	–	11	–	–	10,13	–	–	–		
		13	–	↓		–	↓		–	–	–	–	13	–	–	10,11	–	–	–		
		16	–	-1.6	↓	–	-1.6	↓	–	–	–	–	16	–	–	–	–	–	–	↓	↓
Leakage Current	I_{R1}	1	–	40	μAdc	–	40	μAdc	–	–	–	–	–	1	–	–	–	–	–	5	12
		3	–	160		–	160		–	–	–	–	–	3	–	–	–	–	–		4,7,8,12
		4	–	160		–	160		–	–	–	–	–	4	–	–	–	–	–		3,7,8,12
		7	–	40		–	40		–	–	–	–	–	7	–	–	–	–	–		12
		8	–	40		–	40		–	–	–	–	–	8	–	–	–	–	–		12
		10	–	160		–	160		–	–	–	–	–	10	–	–	–	–	–		11,12,13
		11	–	↓		–	↓		–	–	–	–	–	11	–	–	–	–	–		10,12,13
		13	–	↓		–	↓		–	–	–	–	–	13	–	–	–	–	–		10,11,12
		16	–	40	↓	–	40	↓	–	–	–	–	–	16	–	–	–	–	–	↓	12
	I_{R2}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	–	–	1	–	–	–	5	12
		3	–			–			–	–	–	–	–	–	–	3	–	–	–		4,7,8,12
		4	–			–			–	–	–	–	–	–	–	4	–	–	–		3,7,8,12
		7	–			–			–	–	–	–	–	–	–	7	–	–	–		12
		8	–			–			–	–	–	–	–	–	–	8	–	–	–		12
		10	–			–			–	–	–	–	–	–	–	10	–	–	–		11,12,13
		11	–			–			–	–	–	–	–	–	–	11	–	–	–		10,12,13
		13	–			–			–	–	–	–	–	–	–	13	–	–	–		10,11,12
		16	–	↓	↓	–	↓	↓	–	–	–	–	–	–	–	16	–	–	–	↓	12
Output																					
Output Voltage	V_{OL}	2	–	0.4	Vdc	–	0.4	Vdc	2	–	–	–	–	–	–	–	–	1,3,4,7,8,16	5	–	12
		6	–			–			6	–	–	–	–	–	–	–	–	7,8,10,11,13		–	
		9	–			–			9	–	–	–	–	–	–	–	–	7,8,10,11,13		–	
		14	–			–			–	14	–	–	–	–	–	–	–	1,16		–	
		15	–	↓	↓	–	↓	↓	15	–	–	–	–	–	–	–	–	1,3,4,7,8,16	↓	–	↓
	V_{OH}	2	2.4	–	Vdc	2.4	–	Vdc	–	–	2	–	–	–	–	–	3	1,4,7,8,16	5	–	12
		6		–			–		–	–	6	–	–	–	–	–	10,11	7,8,13		–	
		9		–			–		–	–	9	–	–	–	–	–	10,11,13	7,8		–	
		14		–			–		–	–	–	14	–	–	–	–	1,16	3,4		–	
		15	↓	–	↓	↓	–	↓	–	–	15	–	–	–	–	–	3,7,8	1,4,16	↓	–	↓
Short-Circuit Current	I_{SC}	2	-20	-55	mAdc	-18	-55	mAdc	–	–	–	–	–	–	–	1,3,4,7,8, 10,11,13,16	–	–	–	5	2,12
		6							–	–	–	–	–	–	–		–	–	–		6,12
		9		↓			↓		–	–	–	–	–	–	–		–	–	–		9,12
		14		-70			-70		–	–	–	–	–	–	–		–	–	–		12,14
		15	↓	-55	↓	↓	-55	↓	–	–	–	–	–	–	–	↓	–	–	–	↓	12,15
Power Requirements (Total Device)																					
Power Supply Drain	I_{PD}	16	–	110**	mAdc	–	128**	mAdc	–	–	–	–	–	–	–	1,3,8,10	–	–	–	5	4,7,11,12,16

**Tested only at 25°C.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

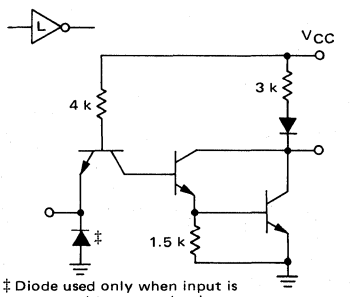
(Letters shown in output columns refer to waveforms. Dash indicates pin left open.)

TEST	FROM INPUT	TO OUTPUT	INPUT A4 Pin 1	A3 Pin 3	B3 Pin 4	B2 Pin 7	A2 Pin 8	A1 Pin 10	B1 Pin 11	C0 Pin 13	B4 Pin 16	OUTPUT S1 Pin 9	S2 Pin 6	S3 Pin 2	S4 Pin 15	C4 Pin 14	R_T Ohms	LIMITS (ns) Max
t_{pd+}	C0	S1	–	–	–	Gnd	Gnd	2.4 V	Gnd	–	–	Y	–	–	–	–	400	34
t_{pd-}																		40
t_{pd+}	C0	S2	–	–	–	Gnd	2.4 V	2.4 V	Gnd	–	–	–	Y	–	–	–	400	38
t_{pd-}																		42
t_{pd+}	C0	S3	–	2.4 V	Gnd	Gnd	2.4 V	2.4 V	Gnd	–	–	–	–	Y	–	–	400	50
t_{pd-}																		60
t_{pd+}	C0	S4	2.4 V	2.4 V	Gnd	Gnd	2.4 V	2.4 V	Gnd	–	Gnd	–	–	–	Y	–	400	55
t_{pd-}																		55
t_{pd+}	C0	C4	2.4 V	2.4 V	Gnd	Gnd	2.4 V	2.4 V	Gnd	–	Gnd	–	–	–	①	Z	780	48
t_{pd-}																		32
t_{pd+}	A2	S2	–	–	–	Gnd	–	Gnd	Gnd	Gnd	–	–	Z	–	–	–	400	40
t_{pd-}																		35
t_{pd+}	B2	S2	–	–	–	–	Gnd	Gnd	Gnd	Gnd	–	–	Z	–	–	–	400	40
t_{pd-}																		35
t_{pd+}	A4	S4	–	Gnd	Gnd	–	–	–	–	–	Gnd	–	–	–	Z	–	400	40
t_{pd-}																		35
t_{pd+}	B4	S4	Gnd	Gnd	Gnd	–	–	–	–	–	–	–	–	–	Z	–	400	40
t_{pd-}																		35

① Apply load circuit of same configuration as load of Switching Time Test Circuit.

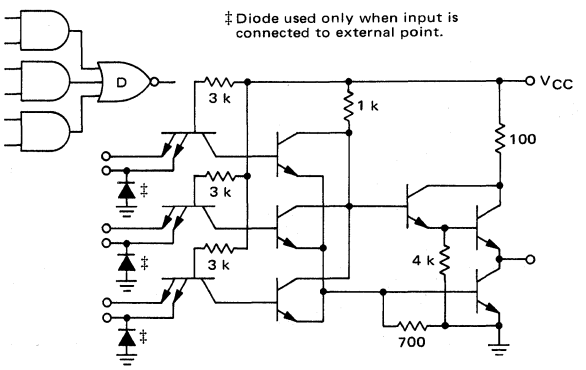
This full adder is constructed using gates and inverters interconnected as shown by the logic diagram.

LOW-LEVEL INVERTER

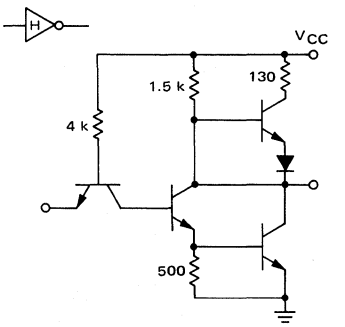


‡ Diode used only when input is connected to external point.

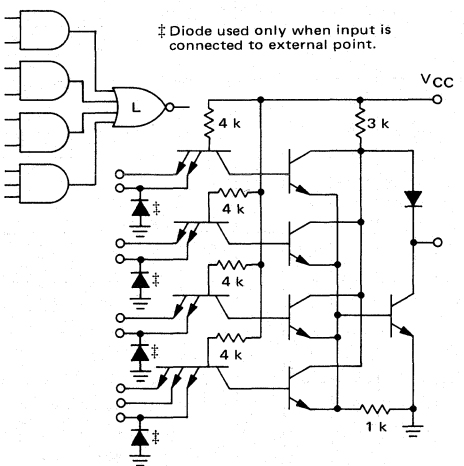
"AND-OR-INVERT" GATE WITH DARLINGTON OUTPUT



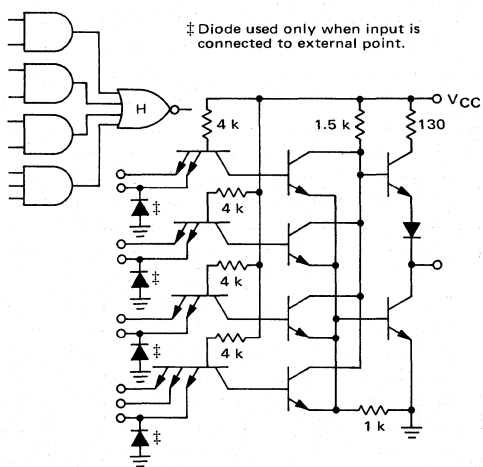
HIGH-LEVEL INVERTER



LOW-LEVEL "AND-OR-INVERT" GATE



HIGH-LEVEL "AND-OR-INVERT" GATE

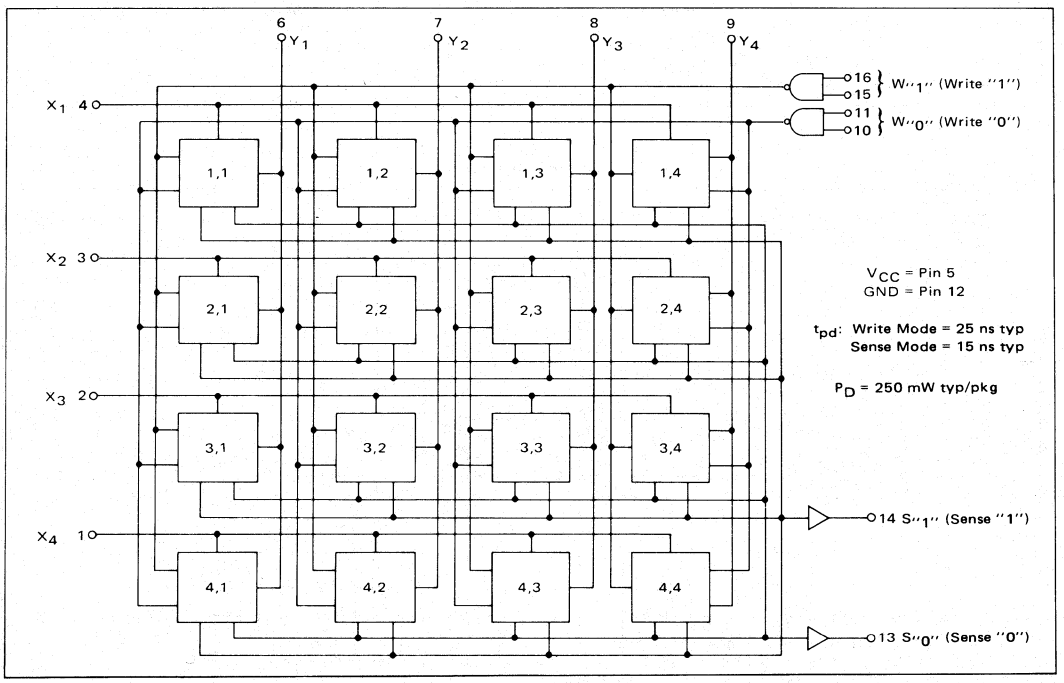


16-BIT SCRATCH PAD MEMORY CELL WITH GATED INPUTS

MC5484L*
MC7484L,P*

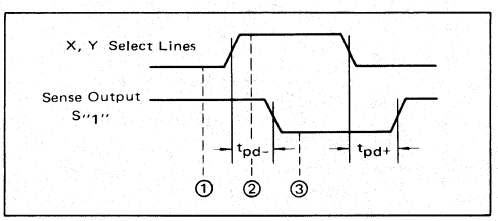
This 16-Bit memory cell serves as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

The memory contains 16 flip-flops arranged in a four-by-four matrix. A single bit of the matrix is selected by driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many devices can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two gated write amplifiers allow a "1" or a "0" to be written into a selected bit.



– OPERATING SEQUENCE –

FIGURE 1 – READ MODE TIMING DIAGRAM



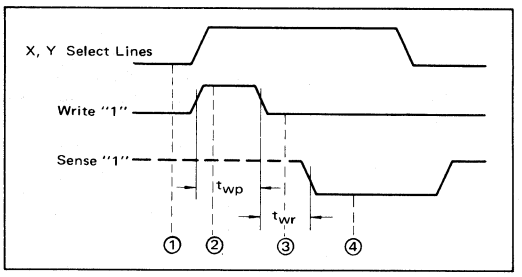
① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Desired bit selected by driving the appropriate X and Y select lines more positive than +2.1 V.

③ After the turn-on delay time(t_{pd-}), the S"1" output will be low (less than +0.45 V) and the S"0" output will be high (more than +2.5 V), providing that a "1" is stored in the selected bit.

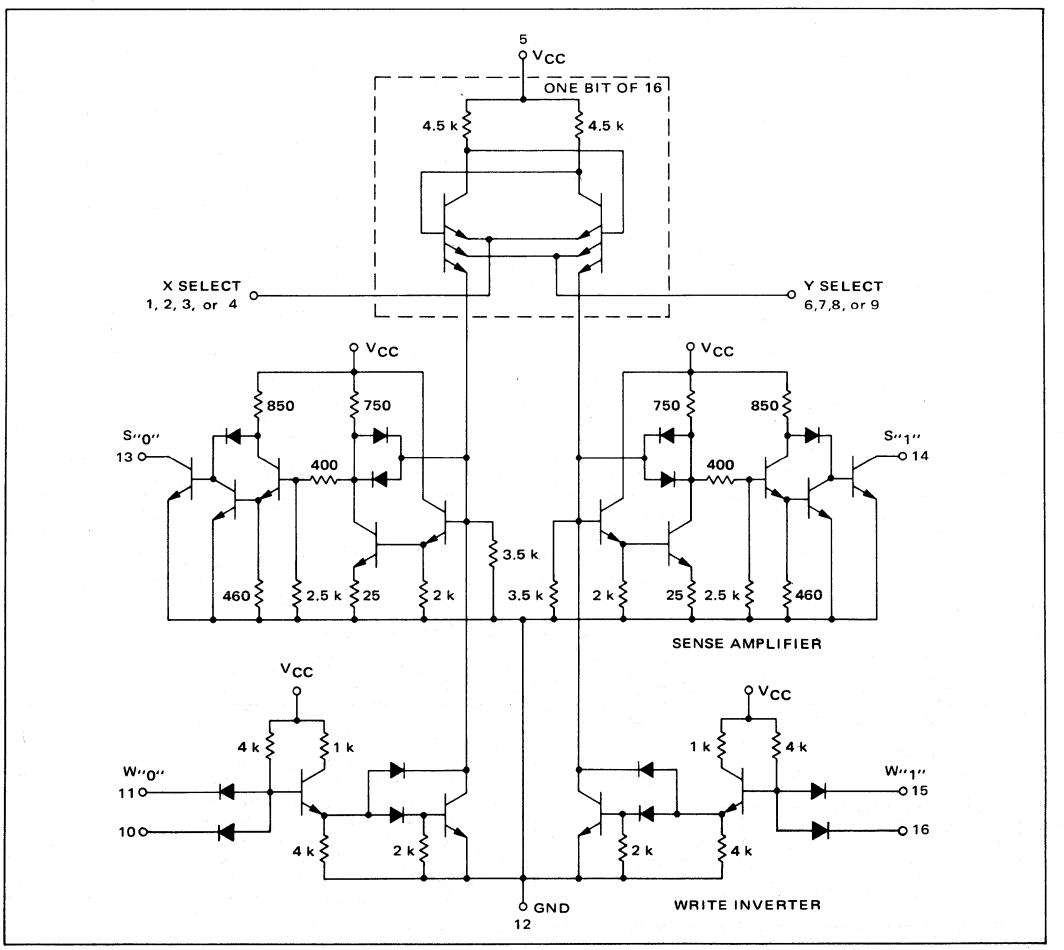
*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

FIGURE 2 – WRITE MODE TIMING DIAGRAM



① All X and Y selection lines and both write inputs are low (less than +0.8 V).
② Bit location selected by driving the appropriate X and Y select lines more positive than +2.1 V. To write a "1", drive the write "1" input more positive than +2.1 V for a minimum time of 25 ns (t_{wp}).
③ Write "1" line returned to low state.
④ The stored bit can be read after the write recovery time (t_{wr}) of 60 ns. (The sense output is in an indeterminate state between steps 2 and 4.)

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one bit. Other bits are tested in the same manner. In addition, test procedures are shown for only one Write input of each level. The other Write inputs are tested in the same manner.

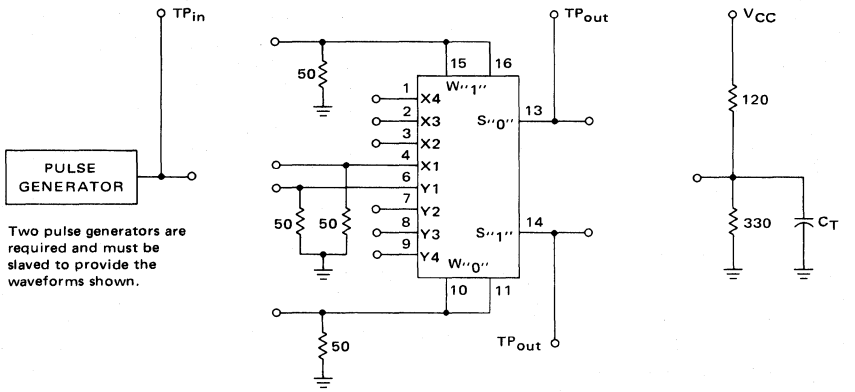
	TEST CURRENT/VOLTAGE VALUES (All Temperatures)													
	mA			Volts										
	$I_{S"0"}$	I_W	I_{XY}	$V_{in\ 1}$	$V_{in\ 2}$	$V_{in\ 3}$	V_F	V_R	V_{th}	$V_{th\ W}$	V_{out}	V_{CCL}	V_{CCH}	
MC5484	40	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	2.0	2.0	4.5	5.5	
MC7484	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	2.0	2.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC5484 Test Limits -55 to +125°C			MC7484 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											Gnd
			Min	Max	Unit	Min	Max	Unit	$I_{S"0"}$	I_W	I_{XY}	$V_{in\ 1}$	$V_{in\ 2}$	$V_{in\ 3}$	V_F	V_R	V_{th}	$V_{th\ W}$	V_{out}	V_{CCL}	V_{CCH}	
Input																					
Forward Current																					
Address Lines	I_F	1	–	-11	mAdc	–	-11	mAdc	–	–	–	–	–	–	1	6,7,8,9	–	–	–	–	5	2,3,4,10,11,12,15,16
		6	–	-11	mAdc	–	-11	mAdc	–	–	–	–	–	–	6	1,2,3,4	–	–	–	–	5	7,8,9,10,11,12,15,16
Write Inputs		10	–	-1.60	mAdc	–	-1.60	mAdc	–	–	–	–	–	–	10	–	–	–	–	–	5	1,2,3,4,6,7,8,9,12,15,16
		15	–	-1.60	mAdc	–	-1.60	mAdc	–	–	–	–	–	–	15	–	–	–	–	–	5	1,2,3,4,6,7,8,9,10,11,12
Leakage Current																					
Address Lines	I_R	1	–	0.4	mAdc	–	0.4	mAdc	–	–	–	–	–	–	–	1	–	–	–	–	5	2,3,4,6,7,8,9,10,11,12,15,16
		6	–	0.4	mAdc	–	0.4	mAdc	–	–	–	–	–	–	–	6	–	–	–	–	5	1,2,3,4,7,8,9,10,11,12,15,16
Write Inputs		10	–	0.1	mAdc	–	0.1	mAdc	–	–	–	–	–	–	–	10	–	–	–	–	5	1,2,3,4,6,7,8,9,12,15,16
		15	–	0.1	mAdc	–	0.1	mAdc	–	–	–	–	–	–	–	15	–	–	–	–	5	1,2,3,4,6,7,8,9,10,11,12
Breakdown Voltage																					
Address Lines	BV_{in}	1	5.5	–	Vdc	5.5	–	Vdc	–	–	1	–	–	–	–	–	–	–	–	–	5	2,3,4,6,7,8,9,10,11,12,15,16
		6	5.5	–	Vdc	5.5	–	Vdc	–	–	6	–	–	–	–	–	–	–	–	–	5	1,2,3,4,7,8,9,10,11,12,15,16
Write Inputs		10	5.5	–	Vdc	5.5	–	Vdc	–	10	–	–	–	–	–	–	–	–	–	–	5	1,2,3,4,6,7,8,9,12,15,16
		15	5.5	–	Vdc	5.5	–	Vdc	–	15	–	–	–	–	–	–	–	–	–	–	5	1,2,3,4,6,7,8,9,10,11,12
Output (Note 1)																					
Output Voltage																					
Write "1"	**	–	–	–	–	–	–	–	–	–	–	–			10,11	–	–	1,6	15,16	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	14	–	0.45	Vdc	–	0.45	Vdc	14	–	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "0" Inhibit	**	–	–	–	–	–	–	–	–	–	–	1,6	–	–	15,16	10,11	–	–	–	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	14	–	0.45	Vdc	–	0.45	Vdc	14	–	–	–			–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "0"	**	–	–	–	–	–	–	–	–	–	–	–	–	15,16	–	–	–	1,6	10,11	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	13	–	0.45	Vdc	–	0.45	Vdc	13	–	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "1" Inhibit	**	–	–	–	–	–	–	–	–	–	–	1,6	–	–	10,11	15,16	–	–	–	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	13	–	0.45	Vdc	–	0.45	Vdc	13	–	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "1"	**	–	–	–	–	–	–	–	–	–	–	–	–	10,11	–	–	–	1,6	15,16	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	14	–	0.45	Vdc	–	0.45	Vdc	14	–	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Leakage Current																					
Write "1"	**	–	–	–	–	–	–	–	–	–	–	–	–	10,11	–	–	–	1,6	15,16	–	5	–	2,3,4,7,8,9,12
Leakage Current	I_{OLK}	14	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	1,6	–	–	–	–	–	14	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "0"	**	–	–	–	–	–	–	–	–	–	–	–	–	15,16	–	–	1,6	10,11	–	5	–	2,3,4,7,8,9,12
Leakage Current	I_{OLK}	13	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	1,6	–	–	–	–		13	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "1"	**	–	–	–	–	–	–	–	–	–	–	–	–	–	–	15,16	1,6,7,8,9	–	–	5	–	2,3,4,10,11,12
Leakage Current	I_{OLK}	13	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	–	–	–	–	1,6,7,8,9	–	13	5	–	2,3,4,10,11,12,15,16
Write "0"	**	–	–	–	–	–	–	–	–	–	–	–	–	–	–	10,11	1,6,7,8,9	–	–	5	–	2,3,4,12,15,16
Leakage Current	I_{OLK}	14	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	–	–	–	–	1,6,7,8,9	–	14	5	–	2,3,4,10,11,12,15,16
Power Requirements (Total Device)																					
Power Supply Drain	I_{PD}	5	–	78#	mAdc	–	91#	mAdc	–	–	–	–	–	–	–	–	–	–	–	5		1,2,3,4,6,7,8,9,10, 11,12,13,14,15,16

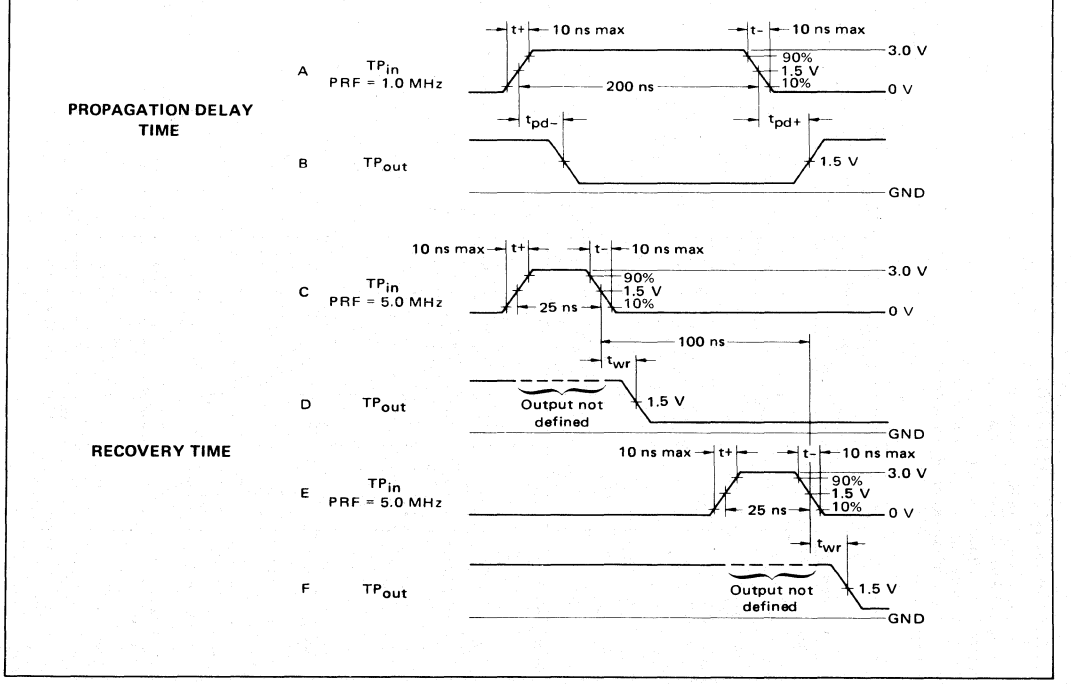
Note 1. Output logic "0" voltage and leakage current measurements are made as part of a functional test of a memory.
** Indicates preconditioning procedures for the subsequent test. All power supply and input voltages must be maintained between tests.

Tested only at 25°C.

SWITCHING TIME TEST CIRCUIT



VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms)

Test	Symbol	Pin Under Test	Input Pin										Output		C_T* pF	Limits	
			4 X_1	3 X_2	2 X_3	1 X_4	6 Y_1	7 Y_2	8 Y_3	9 Y_4	10 W"0"	15 W"1"	13 S"0"	14 S"1"		MC5484 ns max	MC7484 ns max
Turn-Off Delay Time (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	15	25	25
	t_{pd+}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	35	35
Turn-Off Delay Time (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	15	25	25
	t_{pd+}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	35	35
Turn-On Delay Time (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd-}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	15	45	45
	t_{pd-}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	55	55
Turn-On Delay Time (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd-}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	15	45	45
	t_{pd-}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	55	55
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	13	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	B	–	15	30	30
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	14	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	–	B	15	30	30
Write Recovery Time	t_{wr}	14	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	–	D	15	60	60
		13	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	F	–	15	60	60
																ns min	ns min
Write Pulse Width	t_{wp}	–	Tested during t_{wr} tests.													25	25

*Capacitance value for load of the Switching Time Test Circuit

**Preconditioning procedures for subsequent test.

OPERATING CHARACTERISTICS

Sixteen flip-flops are arranged in a 4-by-4 matrix with each flip-flop representing one bit of 16 words. Each flip-flop, consisting of two cross-coupled triple-emitter transistors, is used to store one bit. Memory status of a particular bit is determined by sensing which of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logical "1" sensing outputs are connected to the sense logic "1" amplifier input, and all 16 of the logical "0" sensing outputs are connected to the sense logic "0" amplifier input. The remaining emitters on each transistor provides the matrix connections required for the X- and Y-address lines. Address line inputs are normally held at logic "0" and currents from all conducting flip-flop transistors flow out of these address lines.

To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a logic "1" voltage. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a logic "0" level and no change will occur on those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense amplifier associated with a logic "1" or the sense amplifier associated with a logic "0" is activated. When this occurs, the output of the activated sense amplifier drops from a logic "1" to a logic "0" level. The memory is non-destructive as the states of the flip-flops are not disturbed during sensing.

To store new information in a flip-flop, it is necessary to address it and apply logic "1" voltage to the appropriate write amplifier input. The output of the write amplifier responds by dropping to a logic "0" level. Since all logic "0" sense lines are connected to the output of the logic "0" write amplifier and all logic "1" sense lines are connected to the output of the logic "1" write amplifier, a logic "0" voltage on the output of a write amplifier will apply the same voltage to emitters of all flip-flop transistors connected to that amplifier. In all flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. But two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. But if the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on, causing the other transistor to turn off.

TYPICAL APPLICATIONS

A fast scratch pad memory offers the system designer several design alternatives. Temporary memory with a greater storage capacity than simple registers can be distributed throughout a system. The basic technique for expanding bit capacity is shown in Figure 3; Figure 4 illustrates a method for expanding word capacity.

Optimum design of the selection line drivers depends on the specific system application. The maximum load presented to the drivers by the selection lines is a function of the sequence used to address the memory. The desired logic swing and noise immunity should also be considered when designing the drivers. Each of the 16 flip-flops draws a maximum dc supply current of 2.75 mA (for V_{CC} = 5.0 Vdc). The total current flowing in all 16 flip-flops, and consequently the summed current in the eight selection lines, is 44 mA. (Each selection line is tested for a maximum of 11 mA).

Consider the sequence involved in selecting the four bits X_1Y_1, X_1Y_2, X_1Y_3, and X_1Y_4 simultaneously. If the four Y select lines are enabled before the X_1 line then each of the four X lines must carry the full current from four cells, i.e., 11 mA. The Y drivers must also have the capability of sinking 11 mA if the four X drivers are enabled before a Y driver. However, if the memory accessing sequence specifies that only a single bit may be selected at a time and, consequently, that only one of the X (or Y) selection lines may be high at a time, then the driver requirements can be relaxed somewhat. This is possible because of current sharing in the multi-emitters of the storage flip-flop transistors. If the voltages at the emitters of the "on" transistor differ by no more than approximately 100 mV, then each emitter will carry an appreciable portion of the transistor current. The saturation characteristics of the drivers determine the emitter potentials and, therefore, the division of cell current among the various drivers. Since the V_{OL} of the driver will increase if the collector current increases, the selection currents will be almost evenly distributed among the drivers if the driver saturation characteristics are reasonably uniform. If operation is restricted to a single X selection line and a single Y selection line and current sharing is assumed, then each select line must be capable of carrying the full current from a single cell plus approximately one half of the current from three cells. Each line must, therefore, carry:

$$11/4 + (3)\ (1/2)\ (11/4) = 6.88\ \text{mA}.$$

Since the dc output levels of the driver transistors determine the noise immunity of the selection line, the system noise environment and the desired noise immunity should enter into the driver selection.

FIGURE 3 – 16 WORD, N BIT MEMORY

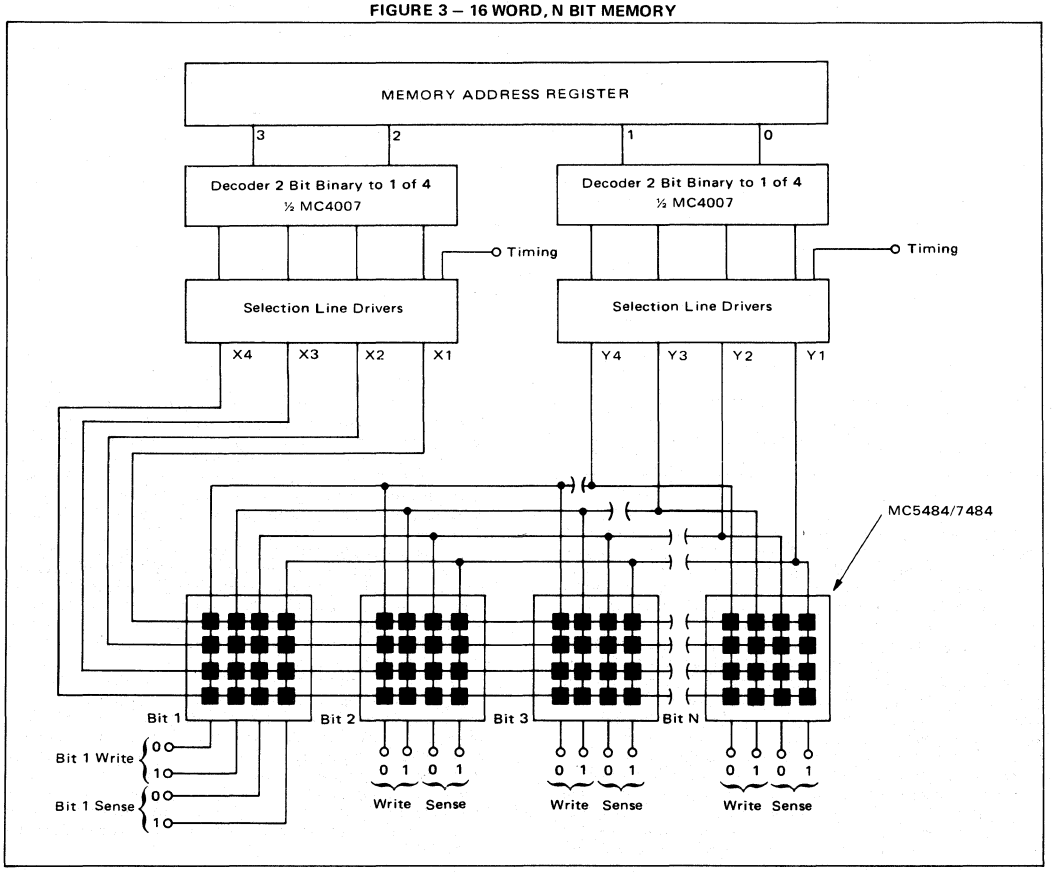
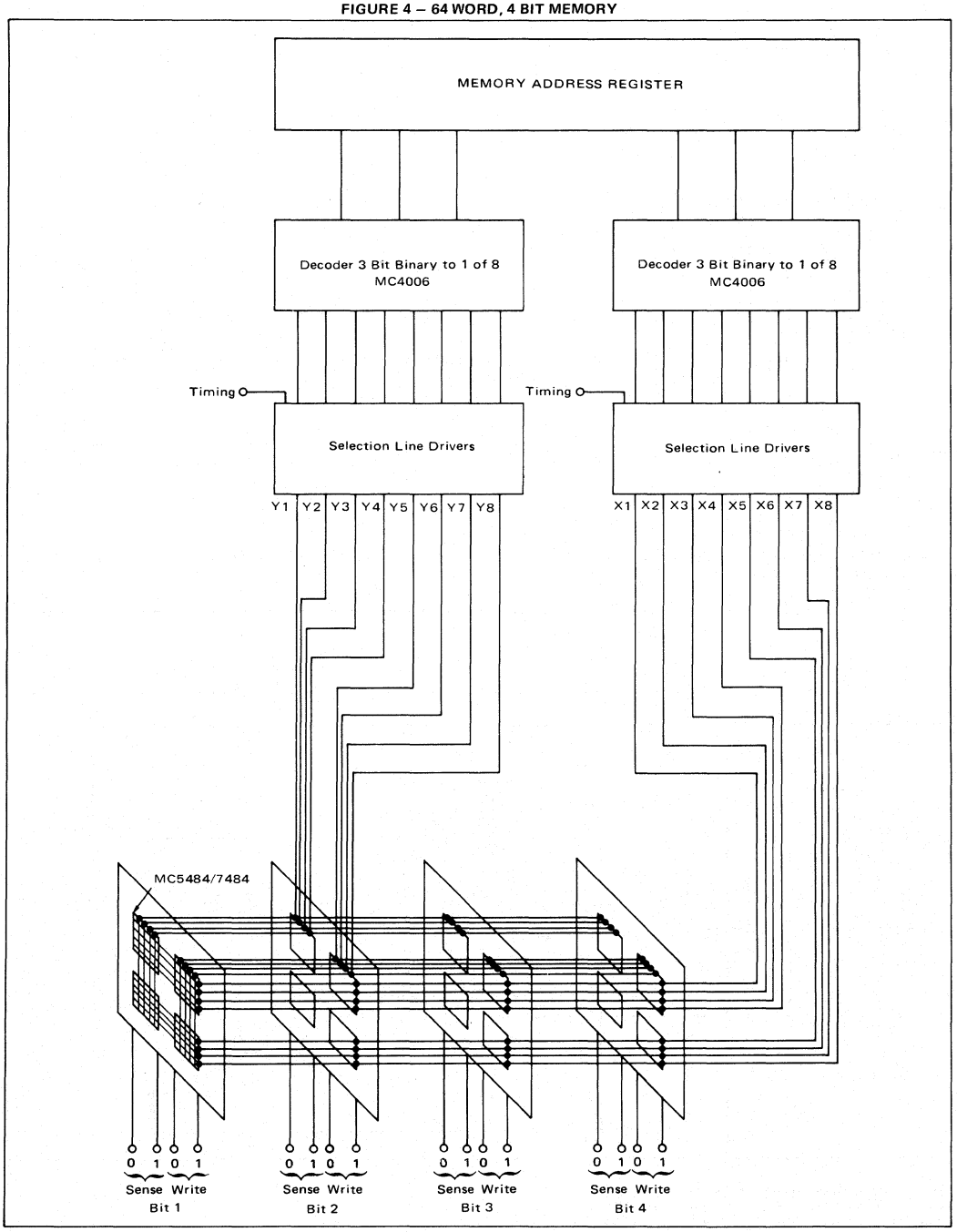


FIGURE 4 – 64 WORD, 4 BIT MEMORY



DECADE COUNTER

MC5490F, L*
MC7490F, L, P*

This 4-bit counter is comprised of a divide-by-two section and a divide-by-five section. These sections can be used independently, or can be connected to perform the counting function or the simple divide-by-ten function with an output duty cycle of 50%. Two sets of direct RESET inputs are provided to allow setting all outputs to a logic "0" or to the BCD count of 9.

RESET/COUNT TRUTH TABLE

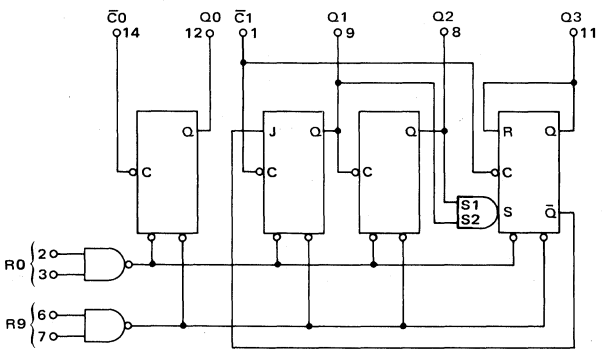
R0		R9		OUTPUT			
Pin 2	Pin 3	Pin 6	Pin 7	Q3	Q2	Q1	Q0
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

X = Don't care.

COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Q0 connected to $\overline{C}1$.



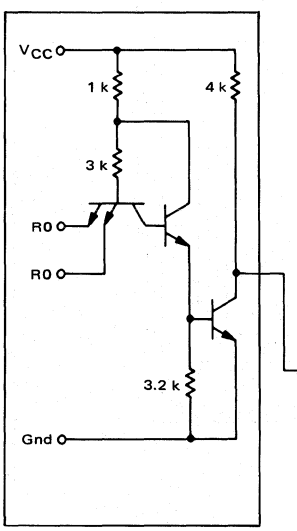
Input Loading Factor:
R0, R9 = 1
$\overline{C}0$ = 2
$\overline{C}1$ = 4

Output Loading Factor = 10

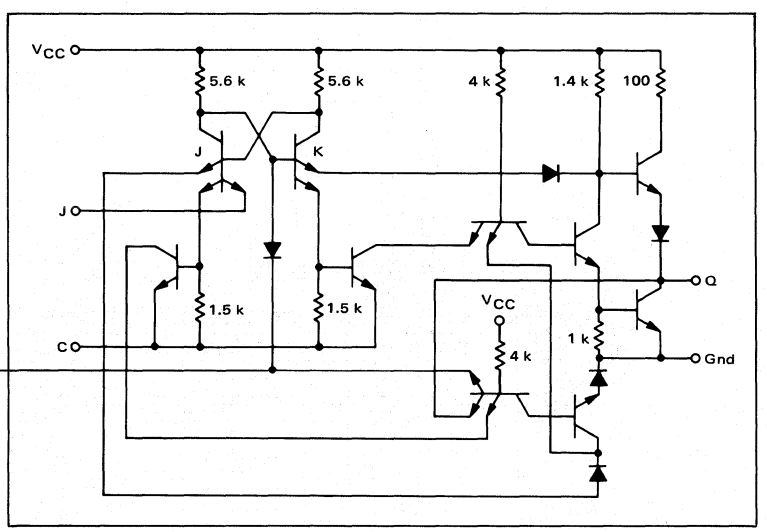
Total Power Dissipation = 160 mW typ/pkg
Propagation Delay Time = 20 ns typ/bit

V_{CC} = Pin 5
GND = Pin 10

TYPICAL RESET GATE



TYPICAL FLIP-FLOP



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

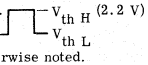
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of each reset gate. The other input of each reset gate is tested in the same manner.

	TEST CURRENT / VOLTAGE VALUES (All Temperatures)													
	mA		Volts											
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{RI}	$V_{th\,1}$	$V_{th\,0}$	$V_{th\,L}$	V_{CC}	V_{CCL}	V_{CCH}		
MC5490	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	0.7	5.0	4.5	5.5		
MC7490	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	0.8	5.0	4.75	5.25		

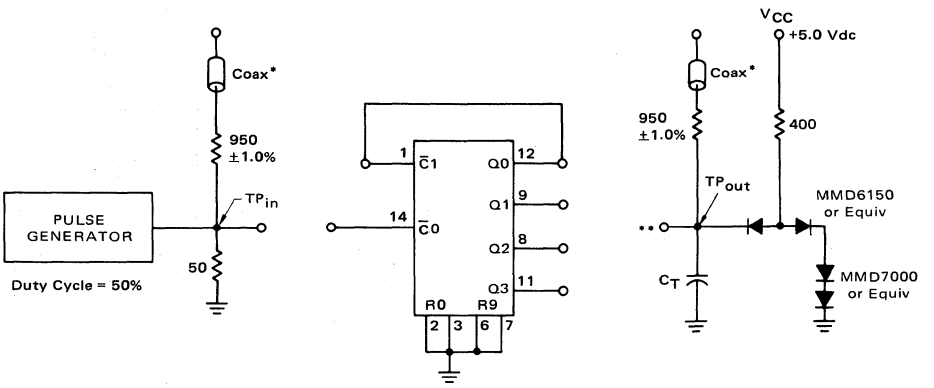
Characteristic		Symbol	Pin Under Test	MC5490 Test Limits −55 to +125°C Min	Max	Unit	MC7490 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{RI}	$V_{th\,1}$	$V_{th\,0}$	$V_{th\,L}$	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Gnd
Input																						
Forward Current	R0	I_F	2	-	-1.6	mAdc	-	-1.6	mAdc	-	-	2	-	-	3	-	-	-	-	-	5	-	10
	R9		6	-	-1.6		-	-1.6		-	-	6	-	-	7	-	-	-	-	-		-	10
	$\overline{C}0$		14	-	-3.2		-	-3.2		-	-	14	-	-	-	-	-	-	-	-		-	2,10
	$\overline{C}1$		1	-	-6.4		-	-6.4		-	-	1	-	-	-	-	-	-	-	-		-	2,10
Leakage Current	R0	I_{R1}	2	-	40	μAdc	-	40	μAdc	-	-	-	2	-	-	-	-	-	-	-	5	-	3,10
	R9		6	-	40		-	40		-	-	-	6	-	-	-	-	-	-	-		-	7,10
	$\overline{C}0$		14	-	80		-	80		-	-	-	14	-	-	-	-	-	-	-		-	10
	$\overline{C}1$		1	-	160		-	160		-	-	-	1	-	-	-	-	-	-	-		-	10
	R0	I_{R2}	2	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	2	-	-	-	-	-	-	5	-	3,10
	R9		6	-			-			-	-	-	-	6	-	-	-	-	-	-		-	7,10
	$\overline{C}0$		14	-			-			-	-	-	-	14	-	-	-	-	-	-		-	10
	$\overline{C}1$		1	-			-			-	-	-	-	1	-	-	-	-	-	-		-	10
Output																						
Output Voltage	Q0 ①	V_{OL}	12	-	0.4	Vdc	-	0.4	Vdc	12	-	-	-	-	-	2,3,14	6,7	-	-	5	-	-	10
Short-Circuit Current		I_{SC}		-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	2,3,6,7	14	-	-	5	14	10,12
Output Voltage		V_{OH}		2.4	-	Vdc	2.4	-	Vdc	-	12	-	-	-	-	-	2,3,6,7,14	-	-	5	-	-	10
	Q1 ①	V_{OL}	9	-	0.4	Vdc	-	0.4	Vdc	9	-	-	-	-	-	2,3	6,7	1	-	5	-	-	10
		I_{SC}		-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	2,3,6,7	1	-	-	5	1	9,10
		V_{OH}		2.4	-	Vdc	2.4	-	Vdc	-	9	-	-	-	-	-	2,3,6,7	1	-	5	-	-	10
	Q2 ①	V_{OL}	8	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	-	2,3,6,7	1	-	5	-	-	10
		I_{SC}		-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-		-	-	-	5	1	8,10
		V_{OH}		2.4	-	Vdc	2.4	-	Vdc	-	8	-	-	-	-	-		1	-	5	-	-	10
	Q3 ①	V_{OL}	11	-	0.4	Vdc	-	0.4	Vdc	11	-	-	-	-	-	-	2,3,6,7	1	-	5	-	-	10
		I_{SC}		-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	6,7	2,3		-	-	5	-	10,11
		V_{OH}		2.4	-	Vdc	2.4	-	Vdc	-	11	-	-	-	-	6,7	2,3		-	5	-	-	10
Power Requirements (Total Device)																						
Power Supply Drain		I_{PD}	5	-	46	mAdc	-	53	mAdc	-	-	-	-	-	-	-	-	-	-	-	5	-	6,7,10

Pulse 1: Apply positive pulse prior to taking measurement to set the device in the desired state. Maintain $V_{th\,L}$ voltage for measurement.



① All input, power supply and ground voltages must be maintained between each test unless otherwise noted.

SWITCHING TIME TEST CIRCUIT



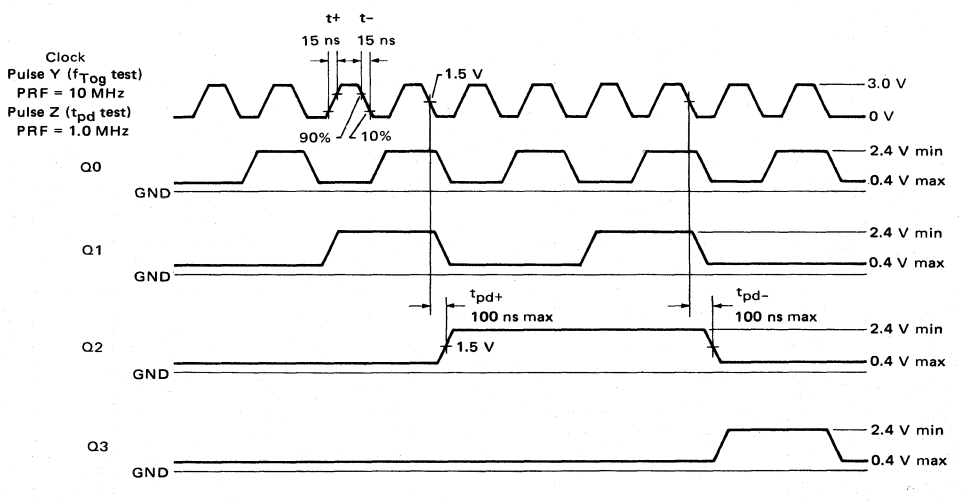
f_{Tog} = 10 MHz min

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

**A load is connected to each output during the test.

VOLTAGE WAVEFORMS AND DEFINITIONS

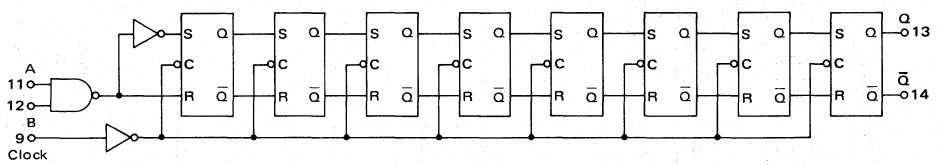


MC5491AL*
MC7491AL,P*

The 8-bit serial-in, serial-out shift register is composed of eight R-S master-slave flip-flops, an input AND gate, and a clock driver.

Single rail data inputs are ANDed together and applied to the input of the first flip-flop. The clock inverter-driver is common to all eight flip-flops and causes information to be shifted to the output on the positive edge of the input clock pulse. Both Q and $\overline{Q}$ are available from the last bit.

The 8-bit shift register may be used as an 8-bit delay line in data handling systems and control systems.



V_{CC} = Pin 5
Gnd = Pin 10

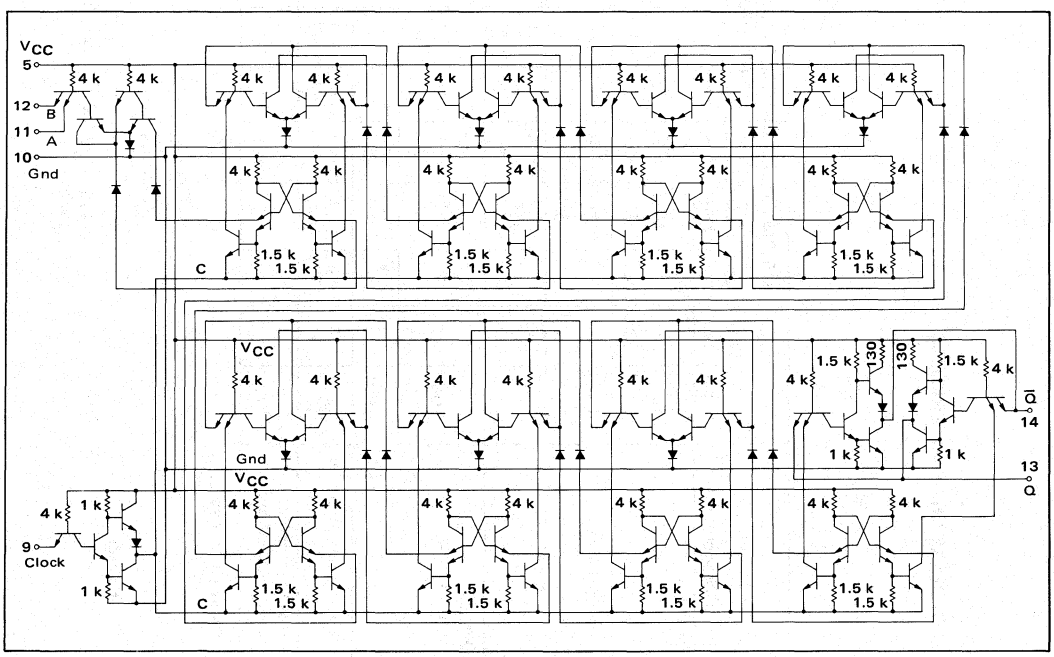
TRUTH TABLE

Synchronous Inputs

t_n		t_{n+8}	
A	B	Q	$\overline{Q}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 175 mW typ/pkg
Propagation Delay Time = 25 ns typ
Operating Frequency = 18 MHz typ



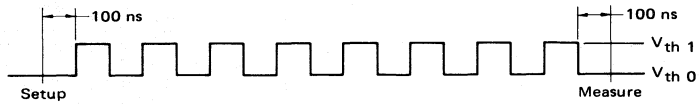
*L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

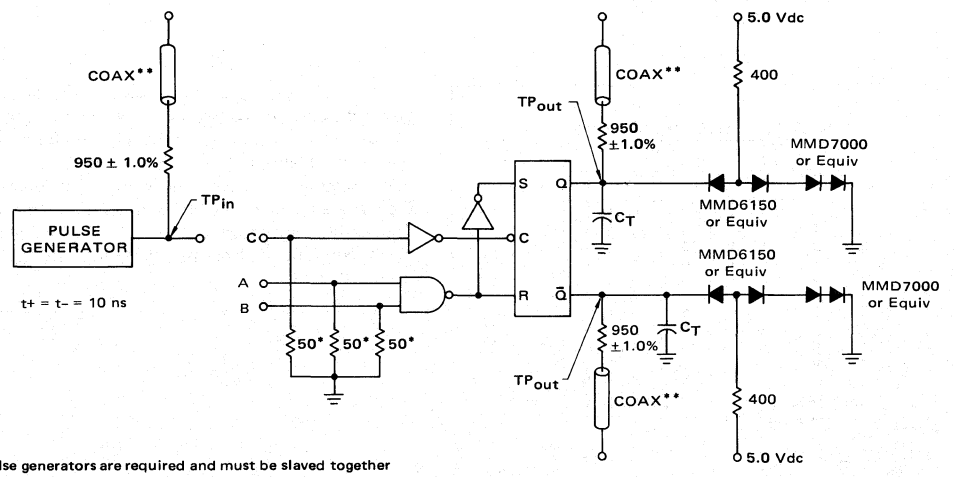
									TEST CURRENT / VOLTAGE VALUES (All Temperatures)											
									mA		Volts									
									I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CCL}	V_{CCH}	
									MC5491A	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	4.5	5.5	
									MC7491A	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	4.75	5.25	
			MC5491A Test Limits −55 to +125°C			MC7491A Test Limits 0 to +70°C			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												
Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CCL}	V_{CCH}	**	Gnd
Input																					
Forward Current	I_F	9	-	-1.6	mAdc	-	-1.6	mAdc	-	-	9	-	-	-	-	-	-	-	5	-	10
		11	-	↓	↓	-	↓	↓	-	-	11	-	-	12	-	-	-	-	↓	-	↓
		12	-			-			-	-	12	-	-	11	-	-	-	-		-	
Leakage Current	I_{R1}	9	-	40	μAdc	-	40	μAdc	-	-	-	9	-	-	-	-	-	-	5	-	10
		11	-	↓	↓	-	↓	↓	-	-	-	11	-	-	-	-	-	-	↓	-	10,12
		12	-			-			-	-	-	12	-	-	-	-	-	-		-	10,11
	I_{R2}	9	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	9	-	-	-	-	-	5	-	10
		11	-	↓	↓	-	↓	↓	-	-	-	-	11	-	-	-	-	-	↓	-	10,12
		12	-			-			-	-	-	-	12	-	-	-	-	-		-	10,11
Output																					
Output Voltage	V_{OL}	13	-	0.4	Vdc	-	0.4	Vdc	13	-	-	-	-	-	-	-	11,12	5	-	9	10
		13	-	↓	↓	-	↓	↓	13	-	-	-	-	-	-	12	11	↓	-	↓	↓
		14	-			-			14	-	-	-	-	-	-	11,12	-		-		
	V_{OH}	13	2.4	-	Vdc	2.4	-	Vdc	-	13	-	-	-	-	-	11,12	-	5	-	9	10
		14	2.4	-	Vdc	2.4	-	Vdc	-	14	-	-	-	-	-	11	12	5	-	9	10
Short-Circuit Current	I_{SC}	13	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	5	-	9,10,11,12,13,14
		14	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	5	-	9,10,11,12,13,14
Power Requirements																					
Power Supply Drain	I_{PD}	10	-	50*	mAdc	-	58*	mAdc	-	-	-	-	-	-	-	-	-	-	5	9	10,11,12

*Tested only at 25°C.

**Input pulse:



SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved together to provide the waveforms shown. Pulse generator for Pulses A and B must be operated in the double pulse mode.

*Resistor used only when that input is under test.

**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

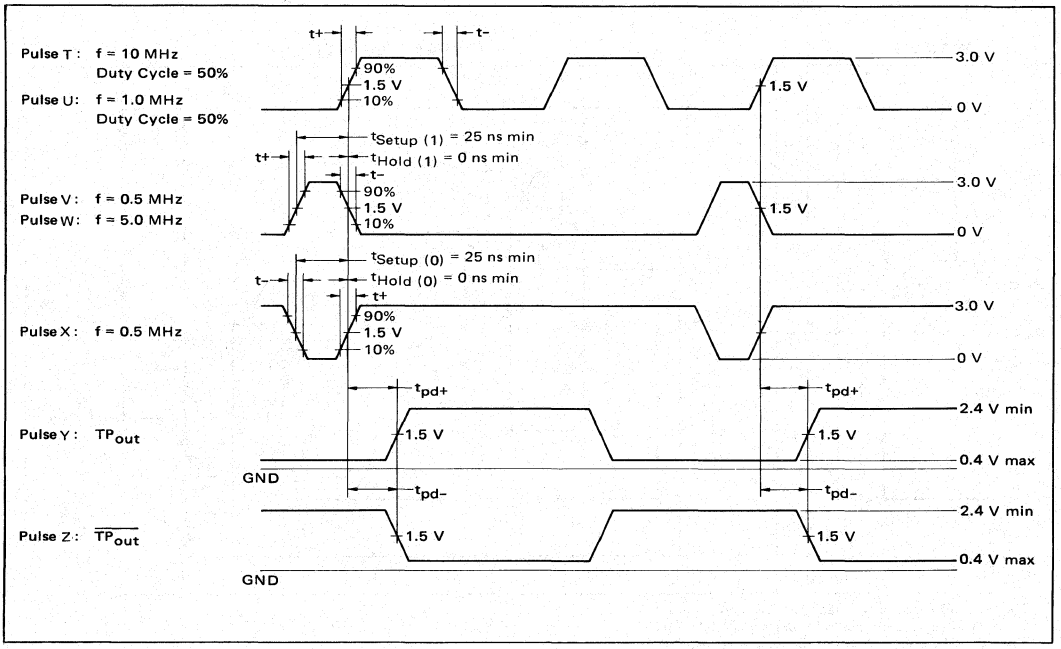
TEST PROCEDURES

(Letters shown in test columns refer to waveforms)

TEST	INPUT			Q	Q̄	LIMITS		
	B	A	C			Min	Max	Unit
f_{Tog}	W	W	T	*	—	10	—	MHz
t_{pd+}	V	2.4 V	U	Y	—	—	40	ns
t_{pd+}	2.4 V	V	U	—	Y	—	40	ns
t_{pd-}	2.4 V	X	U	Z	—	—	40	ns
t_{pd-}	X	2.4 V	U	—	Z	—	40	ns

*Output shall toggle with each input pulse.

VOLTAGE WAVEFORMS AND DEFINITIONS



DIVIDE-BY-TWELVE COUNTER

MC5492F, L*
MC7492F, L, P*

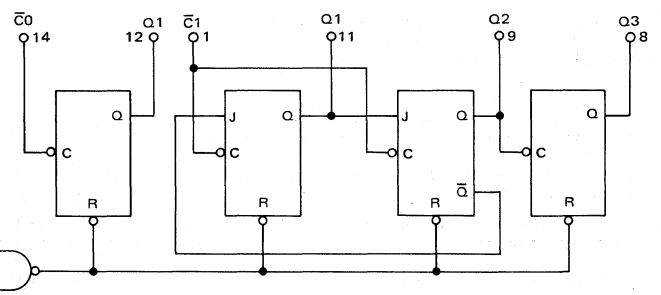
COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

A connected to $\overline{C1}$

This 4-bit counter is comprised of a divide-by-two section and a divide-by-six section. These sections can be used independently, or can be connected to perform the divide-by-twelve function. When used independently, the divide-by-six section provides the divide-by-three function at the C output and the divide-by-six function at the D output. The outputs may be set to the logic "0" state any time during the counting sequence by setting both R0 inputs to the logic "1" state.

V_{CC} = PIN 5
Gnd = PIN 10



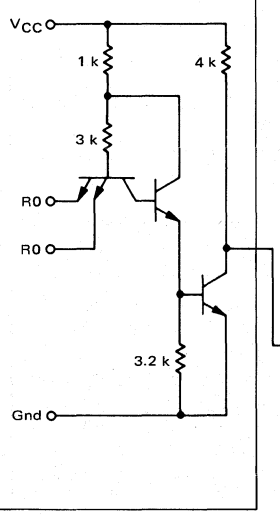
Input Loading Factor:
R0 = 1
C1 = 2
C2 = 4

Output Loading Factor = 10

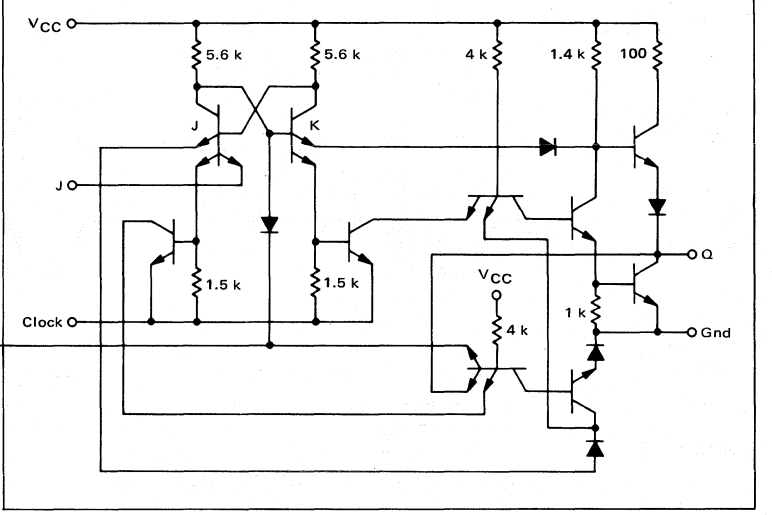
Total Power Dissipation = 160 mW typ/pkg

Propagation Delay Time = 60 ns typ

RESET GATE

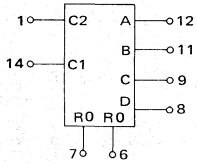


TYPICAL FLIP-FLOP



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

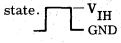


	TEST CURRENT / VOLTAGE VALUES (All Temperatures)											
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{RI}	$V_{th\ 1}$	$V_{th\ 0}$	$V_{th\ L}$	V_{CC}	V_{CCL}	V_{CCH}
MC5492	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	0.7	5.0	4.5	5.5
MC7492	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	0.8	5.0	4.75	5.25

Characteristic		Symbol	Pin Under Test	MC5492 Test Limits −55 to +125°C Min	Max	Unit	MC7492 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{RI}	$V_{th\ 1}$	$V_{th\ 0}$	$V_{th\ L}$	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Pulse 2	Gnd
Input																							
Forward Current	R0	I_F	6	-	-1.6	mAdc	-	-1.6	mAdc	-	-	6	-	-	7	-	-	-	-	-	5	-	-	10
			7	-	-1.6	↓	-	-1.6	↓	-	-	7	-	-	6	-	-	-	-	-	↓	-	-	↓
	C1		14	-	-3.2		-	-3.2		-	-	14	-	-	-	-	-	-	-	-		-	-	
	C2		1	-	-6.4		-	-6.4		-	-	1	-	-	-	-	-	-	-	-		-	-	
Leakage Current	R0	I_{R1}	6	-	40	μAdc	-	40	μAdc	-	-	-	6	-	-	-	-	-	-	-	5	-	-	7,10
			7	-	40	↓	-	40	↓	-	-	-	7	-	-	-	-	-	-	-	↓	-	-	6,10
	C1		14	-	80		-	80		-	-	-	14	-	-	-	-	-	-	-		-	-	10
	C2		1	-	160		-	160		-	-	-	1	-	-	-	-	-	-	-		-	-	10
	R0	I_{R2}	6	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	6	-	-	-	-	-	-	5	-	-	7,10
			7	-	↓	↓	-	↓	↓	-	-	-	-	7	-	-	-	-	-	-	↓	-	-	6,10
	C1		14	-			-			-	-	-	-	14	-	-	-	-	-	-		-	-	10
	C2		1	-			-			-	-	-	-	1	-	-	-	-	-	-		-	-	10
Output																							
Output Voltage	A ①	V_{OL}	12	-	0.4	Vdc	-	0.4	Vdc	12	-	-	-	-	-	6,7,14	-	-	-	5	-	-	-	1,10
Short-Circuit Current		I_{SC}		-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	6,7	-	-	-	5	14	-	1,10,12
Output Voltage		V_{OH}	↓	2.4	-	Vdc	2.4	-	Vdc	-	12	-	-	-	-	-	6,7,14	-	-	5	-	-	-	1,10
	B ①	V_{OL}	11	-	0.4	Vdc	-	0.4	Vdc	11	-	-	-	-	-	6,7	-	1	-	5	-	-	-	10,14
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	6,7	-	-	-	5	-	1	10,11,14
		V_{OH}	↓	2.4	-	Vdc	2.4	-	Vdc	-	11	-	-	-	-	-	6,7	1	-	5	-	-	-	10,14
	C ①	V_{OL}	9	-	0.4	Vdc	-	0.4	Vdc	9	-	-	-	-	-	-	6,7	1	-	5	-	-	-	10,14
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	↓	-	-	-	5	-	1	9,10,14
		V_{OH}	↓	2.4	-	Vdc	2.4	-	Vdc	-	9	-	-	-	-	-	↓	1	-	5	-	-	-	10,14
	D ①	V_{OL}	8	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	-	6,7	1	-	5	-	-	-	10,14
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	↓	-	-	-	5	-	1	8,10,14
		V_{OH}	↓	2.4	-	Vdc	2.4	-	Vdc	-	8	-	-	-	-	-	↓	1	-	5	-	-	-	10,14
Power Requirements (Total Device)																							
Power Supply Drain		I_{PD}	5	-	40	mAdc	-	46	mAdc	-	-	-	-	-	-	-	-	-	5	-	-	-	-	6,7,10

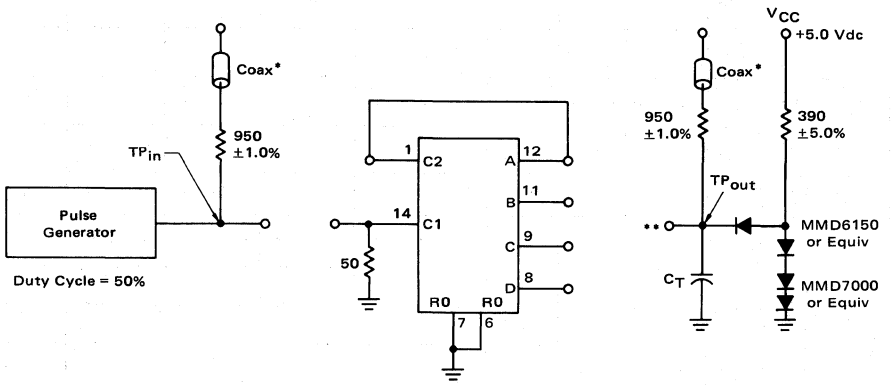
Pulse 1: Momentarily apply $V_{th\ 1}$ then ground prior to taking measurement to set the device in the desired state. Maintain ground for measurement.

Pulse 2: Apply positive pulse prior to taking measurement to set the device in the desired state. Maintain ground for measurement.



① All input, power supply and ground voltages must be maintained between each test unless otherwise noted.

SWITCHING TIME TEST CIRCUIT



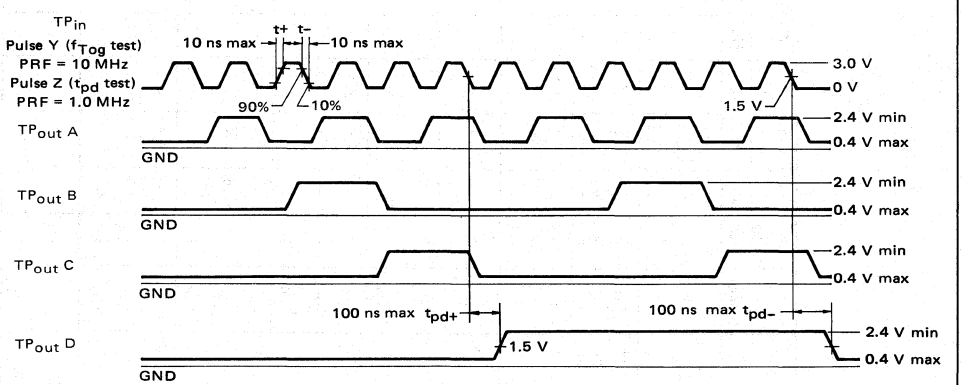
f_{Tog} = 10 MHz min

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

**A load is connected to each output during the test.

VOLTAGE WAVEFORMS AND DEFINITIONS



4-BIT BINARY COUNTER

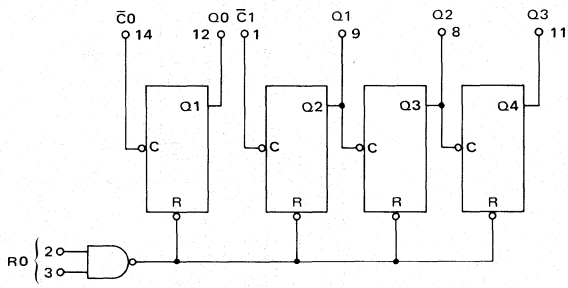
MC5493L*
MC7493L,P*

This 4-bit counter is comprised of two sections: a divide-by-two section and a divide-by-eight section. These sections can be used independently, or can be connected to provide the divide-by-16 function. All outputs of the counter can be set to the logic "0" state by applying a logic "1" level to the Reset input.

TRUTH TABLE

Connect Q0 to $\overline{C}1$

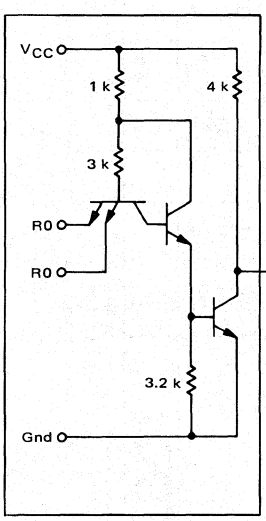
	OUTPUT			
COUNT	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1



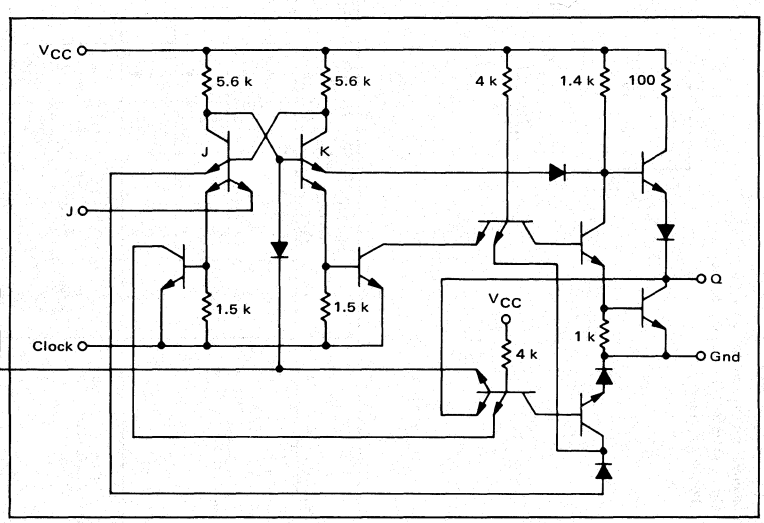
V_{CC} = Pin 5
Gnd = Pin 10

Input Loading Factor
R0 = 1
$\overline{C}0$, $\overline{C}1$ = 2
Output Loading Factor = 10
Total Power Dissipation = 160 mW typ/pkg
Propagation Delay Time = 20 ns typ/bit

RESET GATE



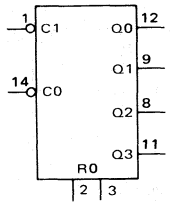
TYPICAL FLIP-FLOP



*L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the reset gate. The other input is tested in the same manner.

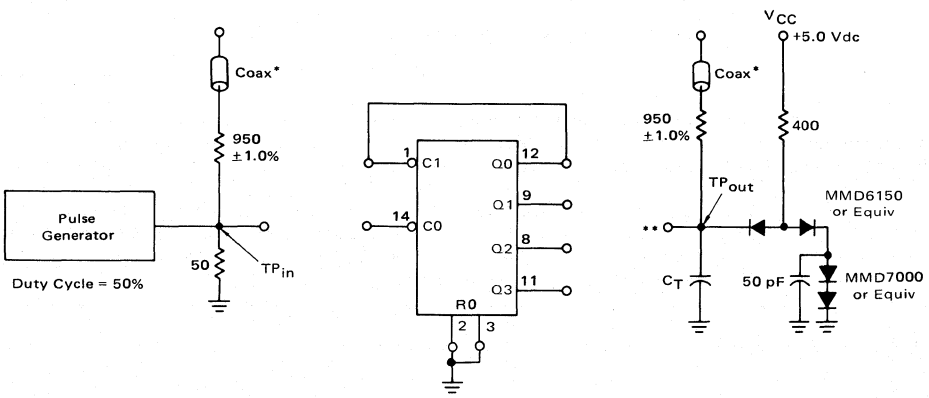


										TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
										mA		Volts										
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{RI}	$V_{th\ 1}$	$V_{th\ 0}$	$V_{th\ L}$	V_{CCL}	V_{CCH}		
									MC5493	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	0.7	4.5	5.5		
									MC7493	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	0.8	4.75	5.25		
			Pin	MC5493 Test Limits -55 to +125°C			MC7493 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											Pulse	
Characteristic		Symbol	Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{RI}	$V_{th\ 1}$	$V_{th\ 0}$	$V_{th\ L}$	V_{CCL}	V_{CCH}	1	Gnd
Input																						
Forward Current	R0	I_F	2	–	-1.6	mAdc	–	-1.6	mAdc	–	–	2	–	–	3	–	–	–	–	5	–	10
	$\bar{C}0$		14	–	-3.2	↓	–	-3.2	↓	–	–	14	–	–	–	–	–	–	–	↓	–	↓
	$\bar{C}1$		1	–	-3.2		–	-3.2		–	–	1	–	–	–	–	–	–	–		–	
Leakage Current	R0	I_{R1}	2	–	40	μAdc	–	40	μAdc	–	–	–	2	–	–	–	–	–	–	5	–	3,10
	$\bar{C}0$		14	–	80	↓	–	80	↓	–	–	–	14	–	–	–	–	–	–	↓	–	10
	$\bar{C}1$		1	–	80		–	80		–	–	–	1	–	–	–	–	–	–		–	10
	R0	I_{R2}	2	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	2	–	–	–	–	–	5	–	3,10
	$\bar{C}0$		14	–	↓	↓	–	↓	↓	–	–	–	–	14	–	–	–	–	–	↓	–	10
	$\bar{C}1$		1	–			–			–	–	–	–	1	–	–	–	–	–		–	10
Output																						
Output Voltage	Q0 ①	V_{OL}	12	–	0.4	Vdc	–	0.4	Vdc	12	–	–	–	–	–	2,3	–	–	5	–	–	10
Short-Circuit Current		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	–	–	14	–	5	14	2,3,10,12
Output Voltage		V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	12	–	–	–	–	–	2,3	14	5	–	–	10
	Q1 ①	V_{OL}	9	–	0.4	Vdc	–	0.4	Vdc	9	–	–	–	–	–	2,3	–	–	5	–	–	10
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	–	–	1	–	5	1	2,3,9,10
		V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	9	–	–	–	–	–	2,3	1	5	–	–	10
	Q2 ①	V_{OL}	8	–	0.4	Vdc	–	0.4	Vdc	8	–	–	–	–	–	2,3	–	1	5	–	–	10
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	–	–	↓	–	5	1	2,3,8,10
		V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	8	–	–	–	–	–	2,3		5	–	–	10
	Q3 ①	V_{OL}	11	–	0.4	Vdc	–	0.4	Vdc	11	–	–	–	–	–	2,3	–	1	5	–	–	10
		I_{SC}	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	–	–	↓	–	5	1	2,3,10,11
		V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	11	–	–	–	–	–	2,3		5	–	–	10
Power Requirements (Total Device)																						
Power Supply Drain		I_{PD}	5	–	46	mAdc	–	53	mAdc	–	–	–	–	–	–	–	–	–	–	5	–	10

Pulse 1: Apply positive pulse prior to taking measurement to set the device in the desired state. Maintain $V_{th\ L}$ voltage for measurement.

① All input, power supply and ground voltages must be maintained between each test unless otherwise noted.

SWITCHING TIME TEST CIRCUIT



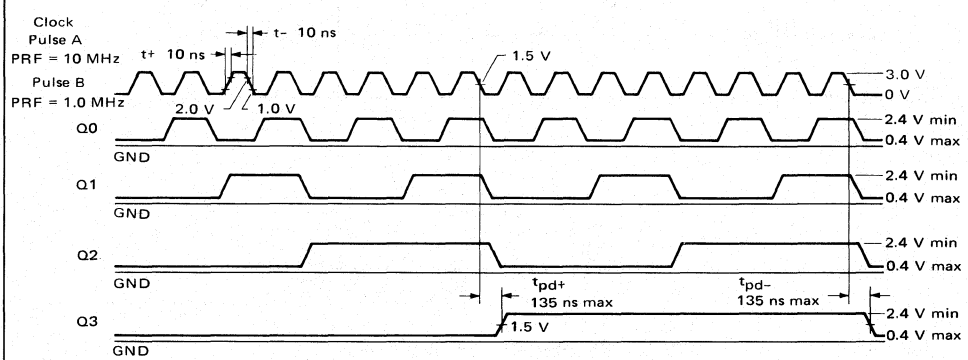
f_{Tog} = 10 MHz min

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

**A load is connected to each output during the test.

VOLTAGE WAVEFORMS AND DEFINITIONS



4-BIT SHIFT REGISTER

MC5494
MC7494

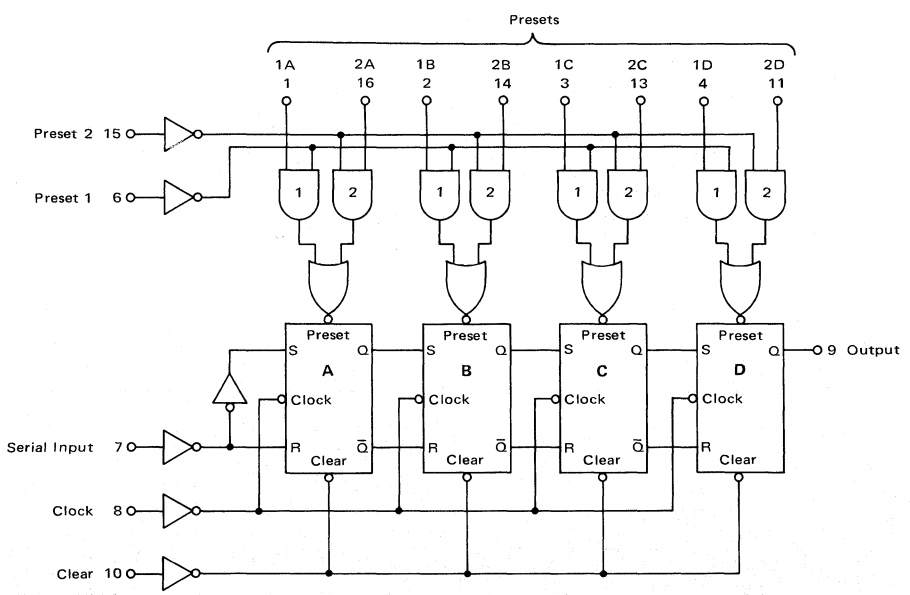
Compatible with MC5400/7400 Series devices.

ADVANCE INFORMATION/PRODUCT PREVIEW*

Soon to be announced, the MC5494/7494 4-bit shift register is constructed of four R-S master-slave flip-flops plus internal gating to accomplish right-shift or parallel-to-serial conversion.

Right-shift operation is accomplished by entering serial data at the serial input prior to the positive transition of the clock pulse.

Parallel operation is accomplished by first clearing all flip-flops and then setting the appropriate flip-flop(s) to the logic "1" state. The common clear input is independent of the clock input, and the separate preset inputs are independent of either clock or clear inputs.



V_{CC} = Pin 5
GND = Pin 12

Total Power Dissipation = 175 mW typ/pkg
Propagation Delay Time (Clock to Output) = 25 ns typ
Maximum Toggle Frequency = 10 MHz

*Products to be introduced

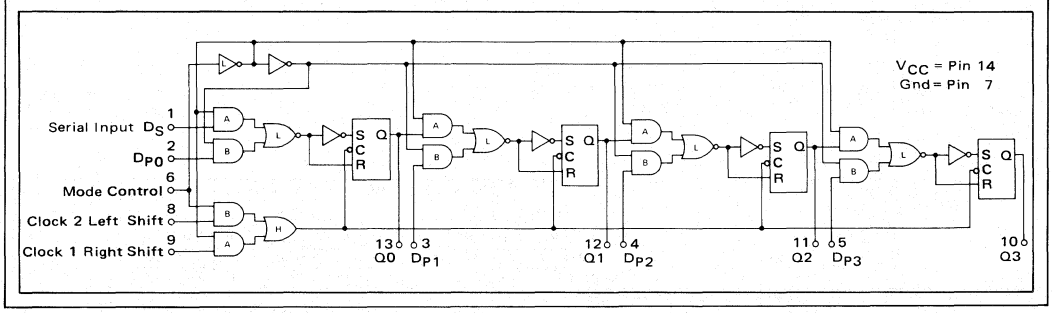
MC5495 • MC7495

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for To-116 plastic package (Case 605) MC7495 only.

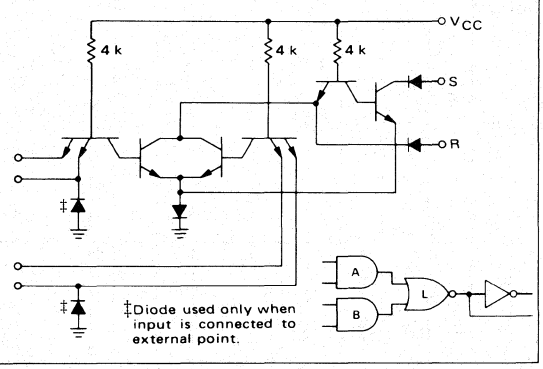
Input Loading Factor:
Mode Control = 2
Other Inputs = 1
Output Loading Factor = 10
Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time = 25 ns typ
Maximum Shift Frequency = 31 MHz typ

The MC5495/7495 performs as a right-shift or left-shift register, or a parallel-in/parallel-out storage register, depending on the logic level present at the Mode Control input.

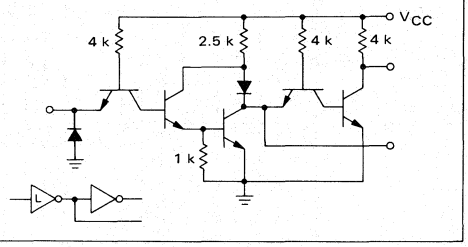
The device consists of R-S master-slave flip-flops, high and low-level gates and inverters interconnected as shown by the logic diagram.



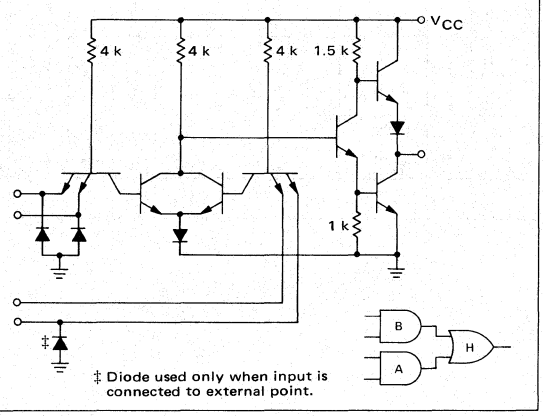
LOW-LEVEL "AND-OR-INVERT" GATE WITH INVERTER DRIVER



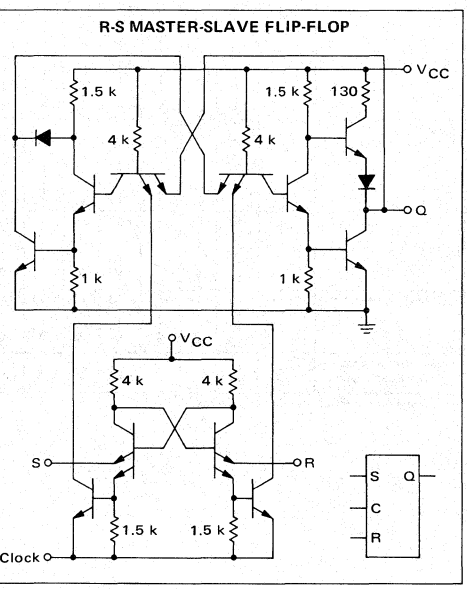
LOW-LEVEL INVERTER



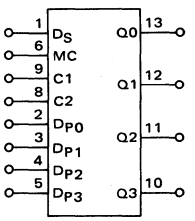
HIGH-LEVEL "AND-OR" GATE



R-S MASTER-SLAVE FLIP-FLOP



ELECTRICAL CHARACTERISTICS



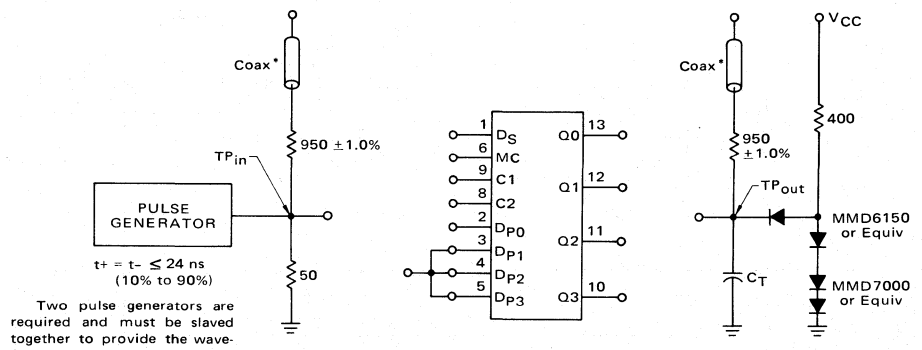
V_{CC} = Pin 14
Gnd = Pin 7

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA		Volts								
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}
MC5495	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.5	5.5
MC7495	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5495 Test Limits -55 to +125°C			MC7495 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										Pulse 1	Gnd
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}		
Input																				
Forward Current	I_F	1	–	-1.6	mAdc	–	-1.6	mAdc	–	–	1	–	–	–	–	–	–	–	14	–	6,7
		2	–	↓	↓	–	↓	↓	–	–	2	–	–	6	–	–	–	–	↓	–	7
		3	–			–			–	–	3	–	–	↓	–	–	–	–		–	↓
		4	–			–			–	–	4	–	–		–	–	–	–		–	
		5	–	↓		–	↓		–	–	5	–	–		–	–	–	–		–	
		6	–	-3.2		–	-3.2		–	–	6	–	–	8	–	–	–	–		–	
		8	–	-1.6		–	-1.6		–	–	8	–	–	6	–	–	–	–		–	
		9	–	-1.6	↓	–	-1.6	↓	–	–	9	–	–	–	–	–	–	–	↓	–	6,7
Leakage Current	I_{R1}	1	–	40	μAdc	–	40	μAdc	–	–	–	1	–	6	–	–	–	–	14	–	7
		2	–	↓	↓	–	↓	↓	–	–	–	2	–	–	–	–	–	–	↓	–	6,7
		3	–			–			–	–	–	3	–	–	–	–	–	–		–	↓
		4	–			–			–	–	–	4	–	–	–	–	–	–		–	
		5	–			–			–	–	–	5	–	–	–	–	–	–		–	
		6	–	80		–	80		–	–	–	6	–	–	–	–	–	–		–	7
		8	–	40		–	40		–	–	–	8	–	–	–	–	–	–		–	6,7
		9	–	40	↓	–	40	↓	–	–	–	9	–	6	–	–	–	–	↓	–	7
	I_{R2}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	1	6	–	–	–	–	14	–	7
		2	–	↓	↓	–	↓	↓	–	–	–	–	2	–	–	–	–	–	↓	–	6,7
		3	–			–			–	–	–	–	3	–	–	–	–	–		–	↓
		4	–			–			–	–	–	–	4	–	–	–	–	–		–	
		5	–			–			–	–	–	–	5	–	–	–	–	–		–	
		6	–			–			–	–	–	–	6	–	–	–	–	–		–	7
		8	–			–			–	–	–	–	8	–	–	–	–	–		–	6,7
		9	–	↓	↓	–	↓	↓	–	–	–	–	9	6	–	–	–	–	↓	–	7
Output																				
Output Voltage	V_{OL}	10	–	0.4	Vdc	–	0.4	Vdc	10	–	–	–	–	–	–	2,3,4,5	–	14	–	8	7
		11	–	↓	↓	–	↓	↓	11	–	–	–	–	–	–	1,6	–	↓	–	↓	↓
		12	–			–			12	–	–	–	–	–	–	2,3,4,5	–		–		
		13	–			–			13	–	–	–	–	–	–	1,6	–		–		
		13	–	↓	↓	–	↓	↓	13	–	–	–	–	–	–	1,6	–	↓	–	9	↓
	V_{OH}	10	2.4	–	Vdc	2.4	–	Vdc	–	10	–	–	–	–	2,3,4,5,6	–	–	14	–	8	7
		11	↓	–	↓	↓	–	↓	–	11	–	–	–	–	↓	–	–	↓	–	↓	↓
		12		–			–		–	12	–	–	–	–		–	–		–		
		13		–			–		–	13	–	–	–	–		–	–		–		
		13	↓	–	↓	↓	–	↓	–	13	6	–	–	–	↓	–	–	↓	–	9	↓
Short-Circuit Current	I_{SC} †	10	-18	-57	mAdc	-18	-57	mAdc	–	–	–	3,4,5,6	–	–	–	–	–	–	14	8	7,10
		11	↓	↓	↓	↓	↓	↓	–	–	–	↓	–	–	–	–	–	–	↓	↓	7,11
		12							–	–	–		–	–	–	–	–	–			7,12
		13							–	–	–		–	–	–	–	–	–			7,13
Power Requirements																				
Power Supply Drain	I_{PD}	14	–	72	mAdc	–	82	mAdc	–	–	2,3,4,5	6	–	–	–	–	14	–	–	8,9	7

†Only one output should be shorted at a time.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

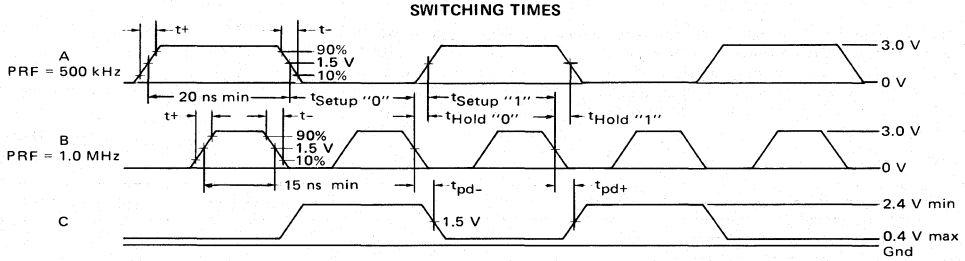


Two pulse generators are required and must be slaved together to provide the waveforms shown.

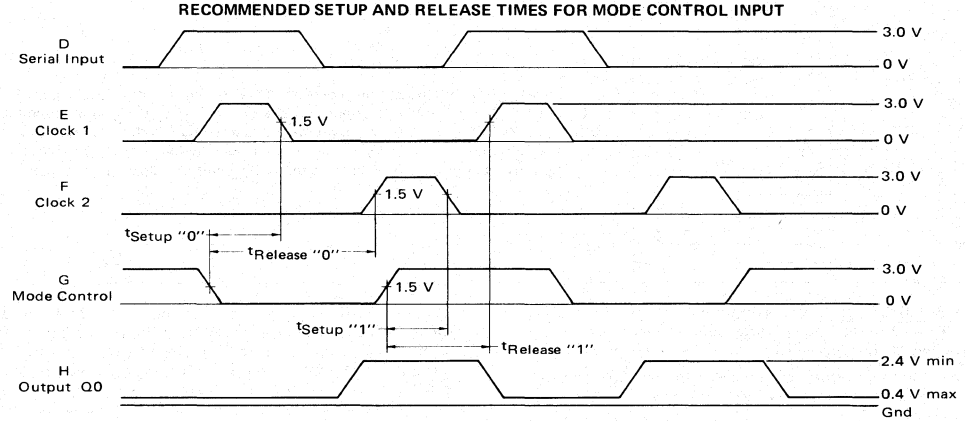
* The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

SWITCHING TIMES



RECOMMENDED SETUP AND RELEASE TIMES FOR MODE CONTROL INPUT



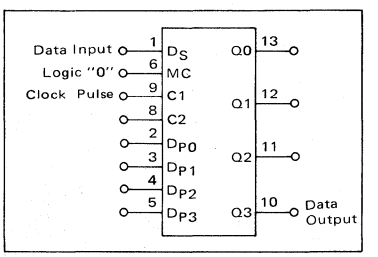
SWITCHING TIME TEST PROCEDURES (T_A = 25°C)
(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT D_S Pin 1	INPUT D_{P0}, D_{P1}, D_{P2} or D_{P3} Pin 2, 3, 4, or 5	INPUT MC Pin 6	INPUT C2 Pin 8	INPUT C1 Pin 9	OUTPUT Q0, Q1, Q2 or Q3 Pin 13, 12, 11, or 10	VALUE Min	VALUE Typ	VALUE Max	VALUE Unit
Propagation Delay Time Clock to Output	t_{pd+}	A	–	0.4 V	Gnd	B	C	–	26	35	ns
		–	A	2.4 V	B	Gnd	C	–	26	35	ns
	t_{pd-}	A	–	0.4 V	Gnd	B	C	–	26	35	ns
		–	A	2.4 V	B	Gnd	C	–	26	35	ns
Maximum Shift Frequency	f_{max}	Tested during t_{pd} tests.						20	31	–	MHz
Setup Time, Serial or Parallel Inputs	t_{Setup}							–	10	20	ns
Hold Time, Serial or Parallel Inputs	t_{Hold}							–	-10	0	ns
			D_{P0}				Q0				
Setup Time, Mode Control Clock 1	t_{Setup}	D	0.4 V	G	0.4 V	E	H	–	–	20	ns
Clock 2		D	0.4 V	G	F	0.4 V	H	–	–	20	ns
Release Time, Mode Control Clock 1	$t_{Release}$	D	0.4 V	G	0.4 V	E	H	–	–	10	ns
Clock 2		D	0.4 V	G	F	0.4 V	H	–	–	10	ns

OPERATING CHARACTERISTICS

FIGURE 1 – SERIAL RIGHT-SHIFT OPERATION

For serial right-shift operation, the Mode Control input is held at a logic "0". This enables the "A" AND gates and inhibits the "B" gates, coupling the output of each flip-flop to the input of the succeeding flip-flop, and inhibiting all four parallel data inputs and Clock 2. Serial data is entered at D_S and the clock pulse applied at Clock 1. The input information shifts one output to the right on each negative edge of the clock pulse.



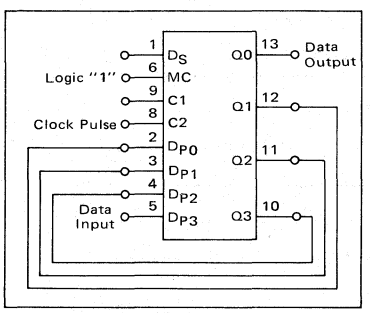


FIGURE 2 – SERIAL LEFT-SHIFT OPERATION

For serial left-shift operation, the Mode Control input is held at a logic "1". This enables the "B" AND gates and inhibits the "A" AND gates, decoupling the output of each flip-flop from the input of the succeeding flip-flop. The output of each flip-flop must be externally connected to the parallel data input of the preceding flip-flop. Serial data is entered at input D_{P3} and the clock pulse applied at Clock 2.

A parallel-in/parallel-out storage register is obtained by applying a logic "1" level to the Mode Control input, applying parallel data at inputs D_{P0}, D_{P1}, D_{P2}, and D_{P3}, and a clock pulse at Clock 2.

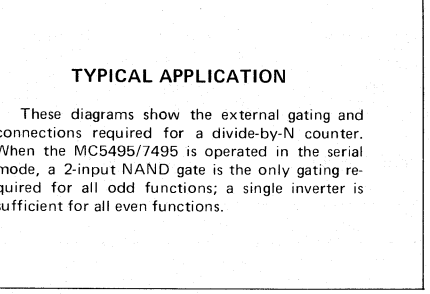
In either mode, information is transferred to the outputs of the device on the negative transition of the clock pulse.

The Mode Control must be in a logic "0" state 20 ns (t_{Setup} "0") prior to the negative transition of the Clock 1 pulse, and in a logic "1" state 20 ns (t_{Setup} "1") prior to the negative transition of the Clock 2 pulse. The Mode control must also be in a logic "0" state 10 ns ($t_{Release}$ "0") prior to the positive transition of the Clock 2 pulse, and in a logic "1" state 10 ns ($t_{Release}$ "1") prior to the positive transition of the Clock 1 pulse.

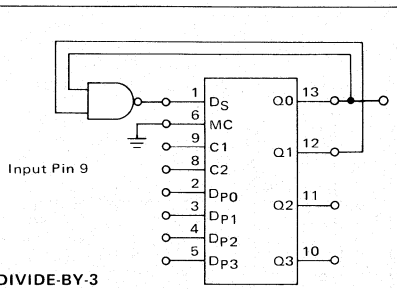
Clock 1 must be high when the Mode Control goes from high to low. Clock 2 must be high when the Mode Control goes from low to high.

TYPICAL APPLICATION

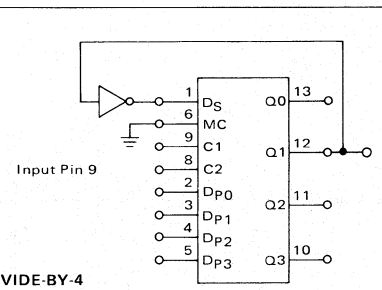
These diagrams show the external gating and connections required for a divide-by-N counter. When the MC5495/7495 is operated in the serial mode, a 2-input NAND gate is the only gating required for all odd functions; a single inverter is sufficient for all even functions.



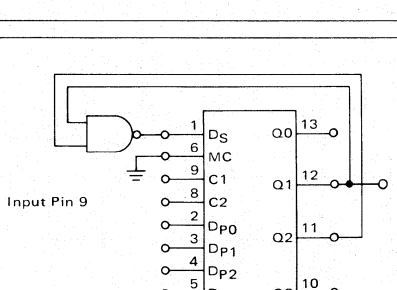
DIVIDE-BY-2



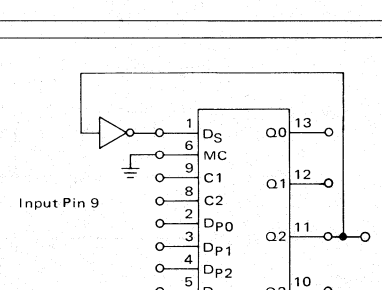
DIVIDE-BY-3



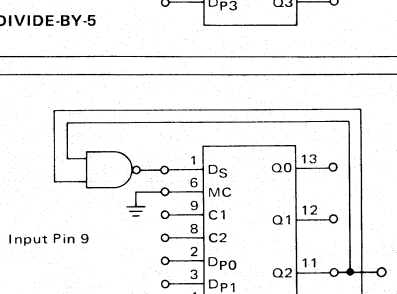
DIVIDE-BY-4



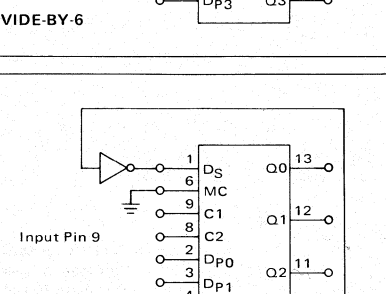
DIVIDE-BY-5



DIVIDE-BY-6



DIVIDE-BY-7



DIVIDE-BY-8

5-BIT SHIFT REGISTER

MC5496
MC7496

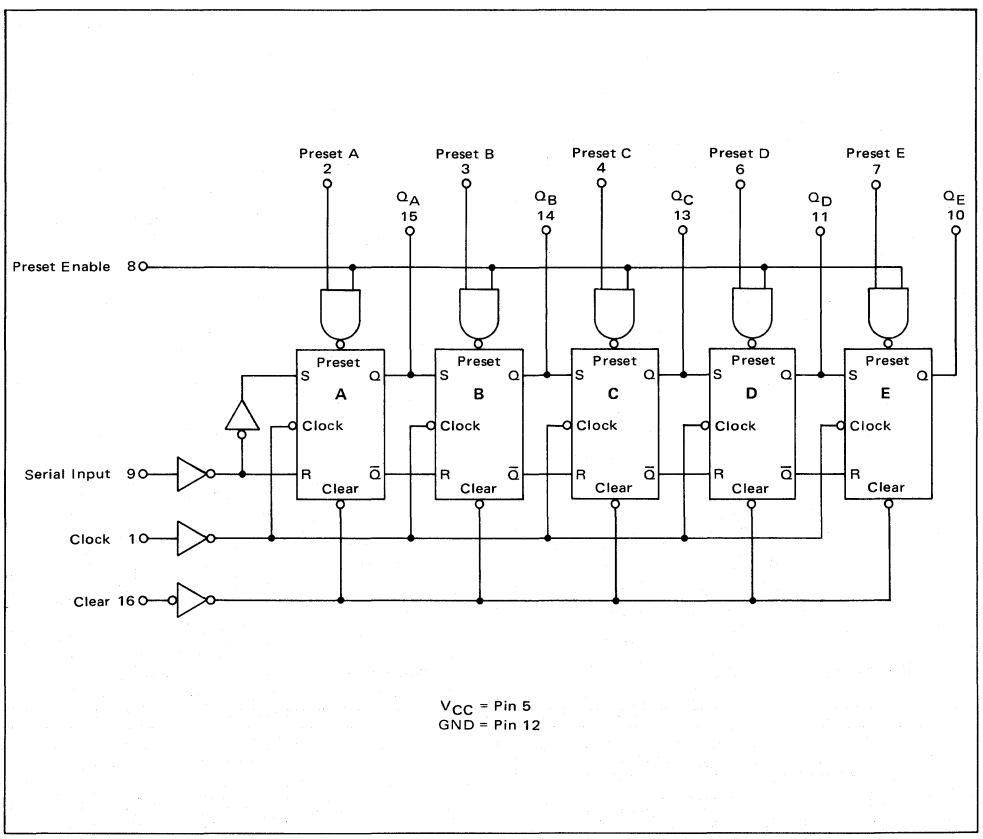
ADVANCE INFORMATION

Soon to be announced, the MC5496/7496 5-bit shift register is constructed of five R-S master-slave flip-flops plus internal gating to accomplish serial-to-parallel or parallel-to-serial conversion, and parallel-in/parallel-out or serial-in/serial-out operation.

Right-shift operation is accomplished by entering serial data at the serial input prior to the positive transition of clock pulse.

The common clear input is independent of the clock, and the separate preset inputs are independent of the clock or clear inputs.

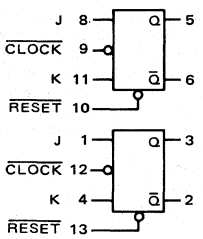
The clear input must be at a logic "1" level and the preset input must be at a logic "0" level when clocking occurs.



Total Power Dissipation = 240 mW typ/pkg
Propagation Delay Time (Clock to Output) = 25 ns typ
Maximum Toggle Frequency = 10 MHz

DUAL J-K FLIP-FLOP

MC54107L*
MC74107P, L*



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

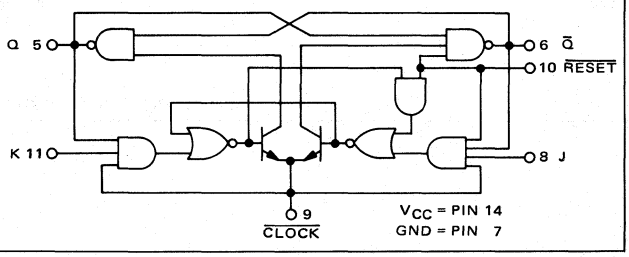
Input Loading Factor:
J, K = 1
$\overline{\text{RESET}}$, $\overline{\text{CLOCK}}$ = 2

Output Loading Factor = 10

Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 30 ns typ
Operating Frequency = 15 MHz typ

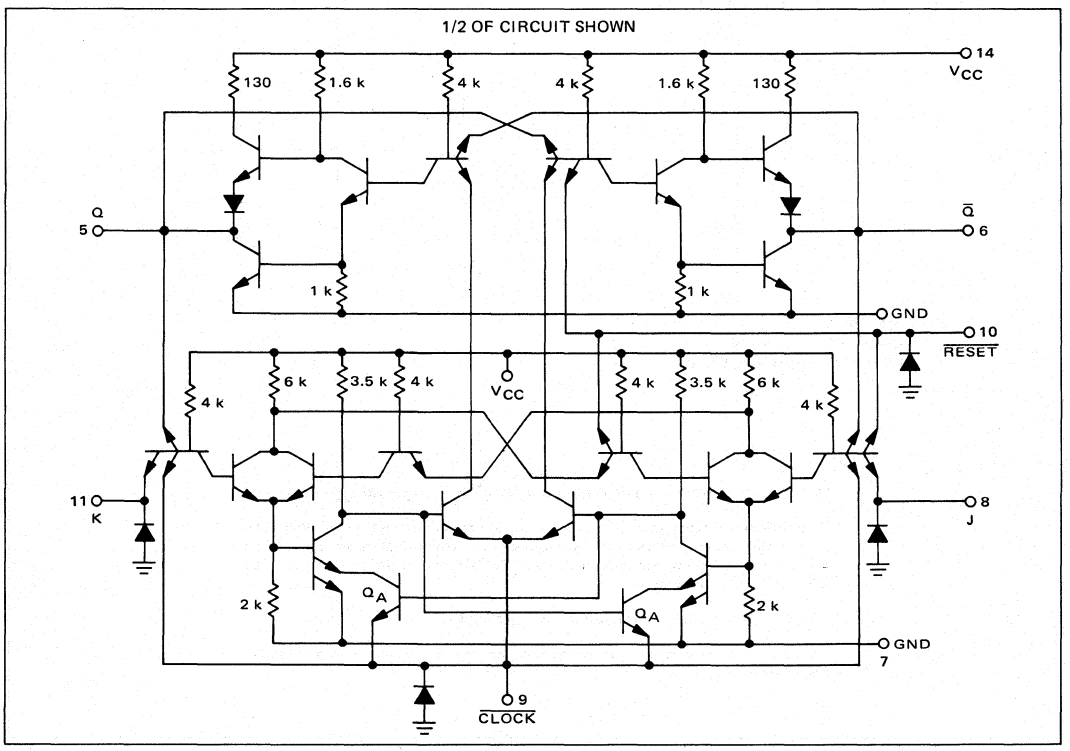
This negative-edge-clocked dual J-K flip-flop operates on the master-slave principle. The device is quite useful for simple registers and counters where multiple J and K inputs are not required.

LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



*L suffix = TO-116 ceramic package (Case 632)
P suffix = TO-116 plastic package (Case 605)
See General Information section for package outline dimensions.

1/2 OF CIRCUIT SHOWN



OPERATING CHARACTERISTICS

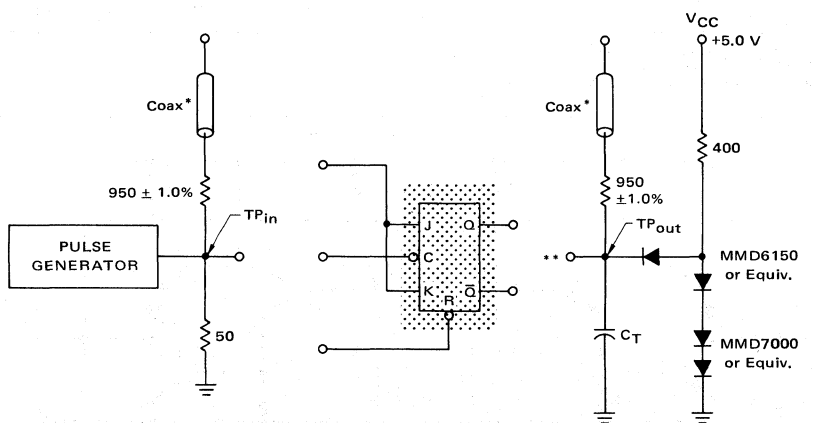
Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{\text{RESET}}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{\text{RESET}}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 20 ns minimum.

Transistors Q_A have been added to the standard flip-flop circuit to protect the device against negative clock transients. This addition prevents both outputs from changing to the logic "1" state when transients in excess of –2.0 V appear at the clock.

SWITCHING TIME TEST CIRCUIT



$t_- = t_+ \leq 5.0$ ns

f = 10 MHz for waveform A
1.0 MHz for waveforms B and C

Two pulse generators are required and must be slaved together for t_{sd} tests.

* The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

** A load is connected to each output during the test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

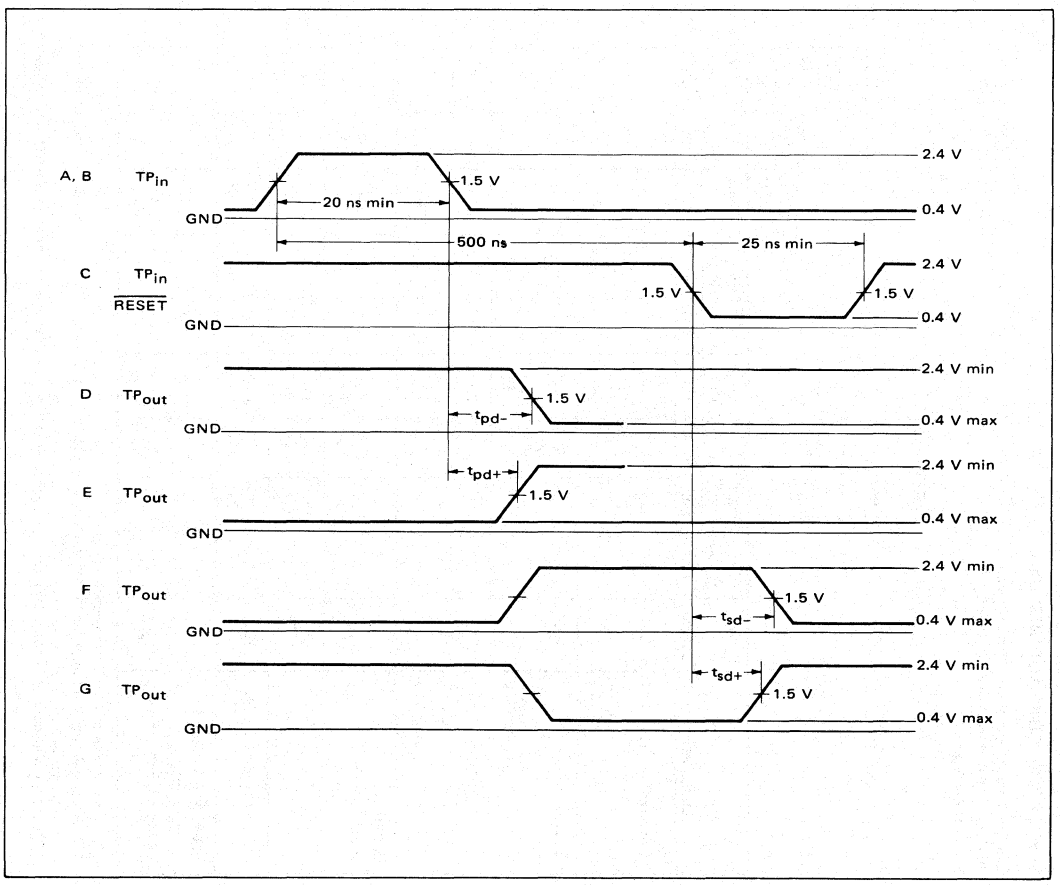
TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT			Q	$\bar{Q}$	LIMITS		
		$\bar{C}$	J, K	$\bar{R}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	A	2.4 V	†	†	10	–	MHz
Turn-On Delay	t_{pd-}	B	B	2.4 V	D	D	10	50	ns
Turn-Off Delay	t_{pd+}	B	B	2.4 V	E	E	10	50	ns
Turn-On Delay	t_{sd-}	B	B	C	F	–	–	50	ns
Turn-Off Delay	t_{sd+}	B	B	C	–	G	–	50	ns
Enable Voltage	V_{EN}	B	2.0 V	2.4 V	†	†	†	–	–
Inhibit Voltage	V_{INH}	B	0.8 V	2.4 V	‡	‡	‡	–	–

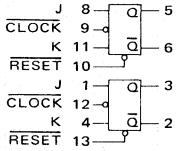
†Output shall toggle with each input pulse.
‡Output shall NOT toggle.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
	mA		Volts										
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}		
MC54107	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.5	5.5		
MC74107	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25		

Characteristic	Symbol	Pin Under Test	MC54107 Test Limits −55 to +125°C			MC74107 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:													
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	**	Gnd
Input																						
Forward Current J	I_F	8	-	-1.6	mAdc	-	-1.6	mAdc	-	-	8	-	-	9,10	-	-	-	-	14	5	7*
K		11	-	-1.6	↓	-	-1.6	↓	-	-	11	-	-	9,10	-	-	-	-	↓	6	7*
$\overline{\text{Reset}}$		10	-	-3.2		-	-3.2		-	-	10	-	-	8,9	-	-	-	-		-	7*
$\overline{\text{Clock}}$		9	-	-3.2	↓	-	-3.2	↓	-	-	9	-	-	2,3,14	-	-	-	-	↓	10	7*
Leakage Current J	I_{R1}	8	-	40	μAdc	-	40	μAdc	-	-	-	8	-	-	-	-	-	-	14	-	7,9,10*
K		11	-	40		-	40		-	-	-	11	-	10	-	-	-	-		10	7,9*
$\overline{\text{Reset}}$		10	-	80		-	80		-	-	-	10	-	-	-	-	-	-		-	7,8,9*
$\overline{\text{Clock}}$		9	-	80	↓	-	80	↓	-	-	-	9	-	-	-	-	-	-	↓	-	7,8,10,11*
J	I_{R2}	8	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	8	-	-	-	-	-	14	-	7,9,10*
K		11	-			-			-	-	-	-	11	10	-	-	-	-		10	7,9*
$\overline{\text{Reset}}$		10	-			-			-	-	-	-	10	-	-	-	-	-		-	7,8,9*
$\overline{\text{Clock}}$		9	-	↓	↓	-	↓	↓	-	-	-	-	9	-	-	-	-	-	↓	-	7,8,10,11*
Output																					
Output Voltage	V_{OL}	5	-	0.4	Vdc	-	0.4	Vdc	5	-	-	-	-	-	-	10	-	14	-	-	7,8,9,11*
		6	-	0.4	Vdc	-	0.4	Vdc	6	-	-	-	-	-	10	-	-	14	-	6	7,8,9,11*
	V_{OH}	5	2.4	-	Vdc	2.4	-	Vdc	-	5	-	-	-	-	10	-	-	14	-	6	7,8,9,11*
		6	2.4	-	Vdc	2.4	-	Vdc	-	6	-	-	-	-	-	10	-	14	-	-	7,8,9,11*
Short-Circuit Current	I_{SC}	5	-20	-57	mAdc	-18	-57	mAdc	-	-	-	8,9,11	-	-	-	-	-	-	14	6	5,7*
		6	-20	-57	mAdc	-18	-57	mAdc	-	-	-	8,9,11	-	-	-	-	-	-	14	-	6,7,10*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PD}	14	-	32	mAdc	-	32	mAdc	-	-	-	-	-	-	-	-	14	-	-	-	7,10,13
		14	-	32	mAdc	-	32	mAdc	-	-	-	-	-	-	-	-	14	-	-	2,6	7

*Ground inputs to flip-flop not under test.

**Momentarily ground pin prior to taking measurement to set flip-flop in the desired state. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

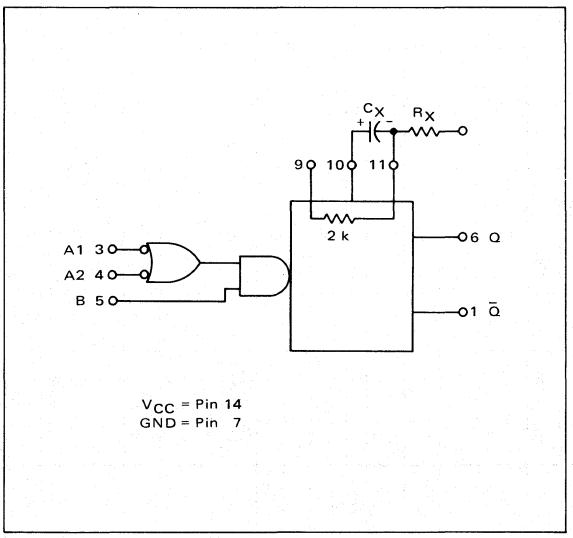
‡Test duration ≤ 100 ms.

†Under normal operating conditions this current is negative. This test guarantees that positive leakage current will not exceed the limit shown.

MONOSTABLE MULTIVIBRATOR

MC54121F,L*
MC74121F,L,P*

This monostable multivibrator produces accurate output pulses from either edge of an input pulse. The output pulse widths may be varied from 40 nanoseconds to 40 seconds by using appropriate external timing components. Internal compensation provides pulse width stability of better than 1.0% with variation of V_{CC} and ambient temperature. In most applications, overall stability will be determined by the accuracy of the external components. Inputs A1 and A2 trigger on the negative-going edge of the input pulse, and input B triggers on the positive-going edge.



Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 90 mW typ/pkg
(50% duty cycle)

TRUTH TABLE

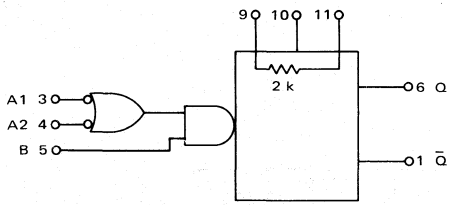
t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	Triggering
X	0	0	X	0	1	Triggering
1	1	1	X	0	1	Triggering
1	1	1	0	X	1	Triggering
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

X = Don't care
t_n = Time period prior to input transition
t_{n+1} = Time period following input transition

*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one A input. The other A input is tested in the same manner.

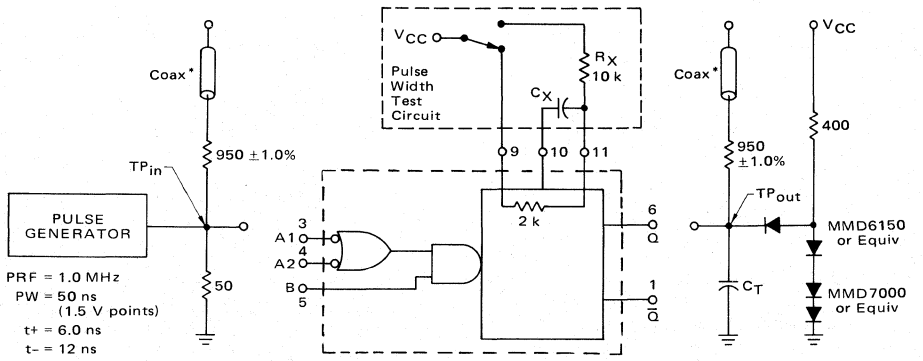


			TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
			mA		Volts								
			I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\ 1}$	$V_{th\ 0}$	V_{CC}	V_{CCL}	V_{CCH}
	MC54121		16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.5	5.5
	MC74121		16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC54121 Test Limits -55 to +125°C Min	Max	Unit	MC74121 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	$V_{th\ 1}$	$V_{th\ 0}$	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																				
Forward Current	I_F	3	–	-1.6	mAdc	–	-1.6	mAdc	–	–	3	–	–	4	–	–	–	–	14	5,7
		5	–	-3.2	mAdc	–	-3.2	mAdc	–	–	5	–	–	3,4	–	–	–	–	14	6*,7
Leakage Current	I_{R1}	3	–	40	μAdc	–	40	μAdc	–	–	–	3	–	–	–	–	–	–	14	4,5,7
		5	–	80	μAdc	–	80	μAdc	–	–	–	5	–	3,4	–	–	–	–	14	7
	I_{R2}	3	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	3	–	–	–	–	–	14	4,5,7
		5	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	5	3,4	–	–	–	–	14	7
Output																				
Output Voltage	V_{OL}	6	–	0.4	Vdc	–	0.4	Vdc	6	–	–	–	–	–	–	3,4,5	–	14	–	7
	V_{OH}	6	2.4	–	Vdc	2.4	–	Vdc	–	6	–	–	–	–	–	3,4,5	–	14	–	7,11
Short-Circuit Current	I_{SC}	1	-20	-55	mAdc	-18	-55	mAdc	–	–	–	–	–	–	–	–	–	–	9,14	1,3,4,5,7
		6	-20	-55	mAdc	-18	-55	mAdc	–	–	–	–	–	–	–	–	–	–	14	3,4,5,6,7,10,11**
Power Requirements																				
Power Supply Drain	I_{PD}	14	–	25	mAdc	–	25	mAdc	–	–	–	–	–	–	–	5	–	–	9,14	3,4,7
		14	–	40	mAdc	–	40	mAdc	–	–	–	–	–	–	5	–	–	–	9,14	3,4,7
Switching Parameters (C_X = 80 pF unless otherwise noted.)									Pulse In	Pulse Out										
Turn-Off Delay — A to Q	t_{pd+}	6	–	70#	ns	–	70#	ns	3	6	–	4,5	–	–	–	–	9,14	–	–	7
B to Q		6	–	55#	ns	–	55#	ns	5	6	3,4	–	–	–	–	–	9,14	–	–	7
Turn-On Delay — A to $\bar{Q}$	t_{pd-}	1	–	80#	ns	–	80#	ns	3	1	–	4,5	–	–	–	–	9,14	–	–	7
B to $\bar{Q}$		1	–	65#	ns	–	65#	ns	5	1	3,4	–	–	–	–	–	9,14	–	–	7
Output Pulse Witdth	PW																			
With Internal Timing Resistor		5,1	70#	150#	ns	70#	150#	ns	5	1	–	–	–	–	–	–	9,14	–	–	3,4,7
With C_X = 0		↓	20#	50#	↓	20#	50#	↓	↓	↓	–	–	–	–	–	–	9,14	–	–	↓
With R_X = 10 kΩ, C_X = 100 pF			600#	800#		600#	800#				–	–	–	–	–	–	14	–	–	
R_X = 10 kΩ, C_X = 1.0 μF			6.0#	8.0#	ms	6.0#	8.0#	ms			–	–	–	–	–	–	14	–	–	
Minimum Duration of Trigger Pulse	t_{Hold}	5,1	–	50#	ns	–	50#	ns	5	1	–	–	–	–	–	–	9,14	–	–	3,4,7

*Momentarily ground this pin before taking measurement.
**Pin 10 should be grounded after pin 11.
#Tested only at 25°C.

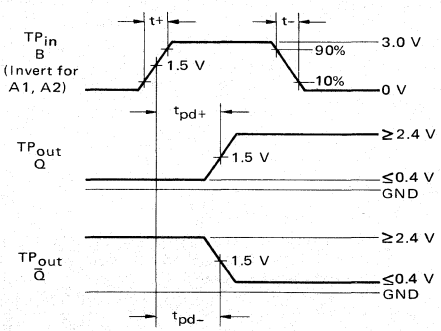
TEST CIRCUIT AND VOLTAGE WAVEFORMS



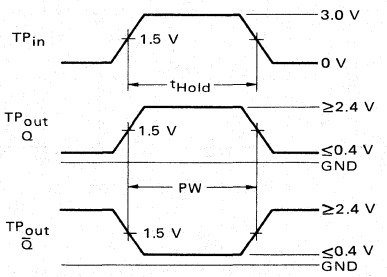
* The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

SWITCHING TIMES



OUTPUT PULSE WIDTH



APPLICATIONS INFORMATION

Inputs A1 and A2 are negative-edge-triggered and will trigger the monostable multivibrator into the active state when either or both go low while B is high. The B input will trigger the one-shot when B goes high while either A or B is low. Triggering occurs at a particular voltage level and is independent of the input pulse transition time. The Schmitt-trigger capability of the B input can be used to obtain level detection and to process relatively slow leading edges. Jitter-free triggering is obtained with transition times as slow as 1.0 volt/second, providing the circuit with a typical noise immunity of 1.2 volts. Internal latching circuitry provides for a typical noise immunity of 1.5 volts on the V_{CC} line.

During the active state, the outputs are independent of further transitions on the inputs and depend only on the external timing components. With no external timing components and pin 9 connected to V_{CC} (pins 10 and 11 left open), an output pulse of approximately 30 nanoseconds is obtained. An external timing capacitor connected between pins 10 and 11 will extend the pulse width. Accurate repeatable pulse width may be obtained by leaving pin 9 open and connecting an external resistor between pin 11 and V_{CC}. This resistor should be at least 1.4 kilohms and may be as large as 40 kilohms for the MC74121 and 30 kilohms for the MC54121. The timing capacitor may be as large as 1000 μF. Within these limits, the output pulse width is given by:

$$PW = C_X R_X \log_e 2.$$

FIGURE 1 – SCHMITT TRIGGER THRESHOLD VOLTAGE versus TEMPERATURE

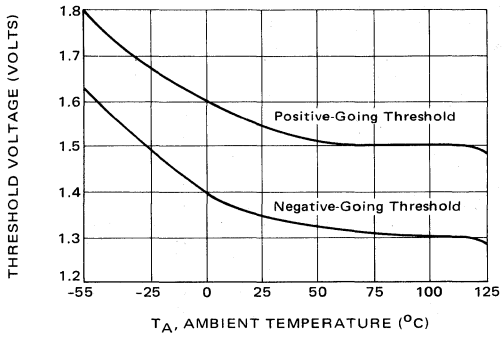


FIGURE 2 – INTERNAL TIMING RESISTOR VARIATION versus TEMPERATURE

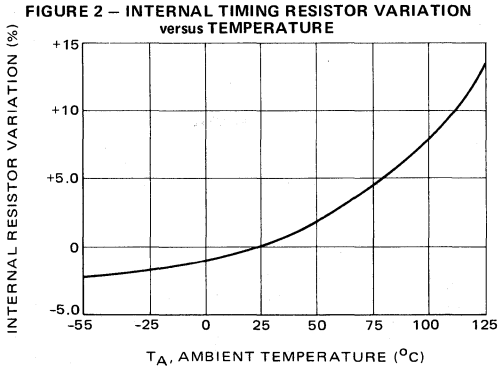


FIGURE 3 – OUTPUT PULSE WIDTH VARIATION versus TEMPERATURE

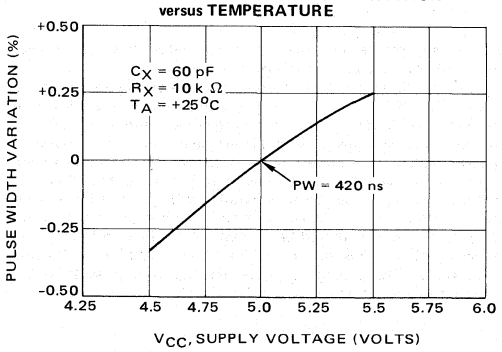


FIGURE 4 – OUTPUT PULSE WIDTH versus EXTERNAL TIMING RESISTOR VALUE

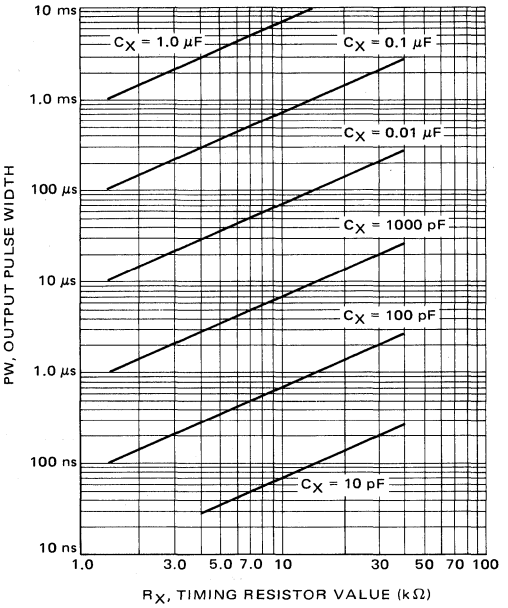
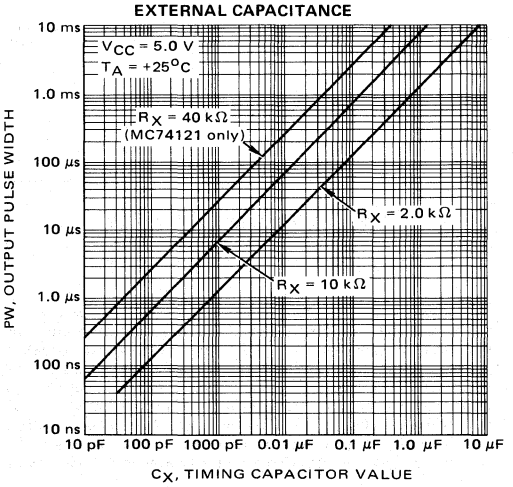
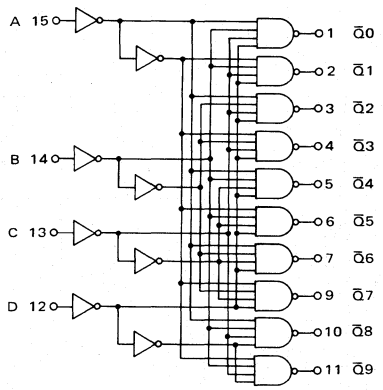


FIGURE 5 – OUTPUT PULSE WIDTH versus EXTERNAL CAPACITANCE



BCD TO ONE-OF-TEN
DECODER/DRIVERS

MC54145L • MC74145L,P*
MC5445L • MC7445L,P*



V_{CC} = Pin 16
GND = Pin 8

These devices are intended for use as drivers for indicators or relays, rather than drivers for MTTL logic gates, as is the case with the MC5442/7442, which is functionally identical. The output transistors of these devices are capable of sinking 80 mA, and have breakdown voltages of 30 V (MC5445/7445) and 15 V (MC54145/74145). The outputs are suitable for open-collector logic applications, and are compatible for interfacing with most MOS integrated circuits. Since full decoding is included, all outputs remain off for non-BCD inputs

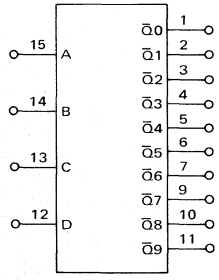
Total Power Dissipation = 215 mW typ/pkg
Propagation Delay Time = 50 ns max

INPUTS				OUTPUTS									
D	C	B	A	Q̄9	Q̄8	Q̄7	Q̄6	Q̄5	Q̄4	Q̄3	Q̄2	Q̄1	Q̄0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner according to the truth table. Test all input-output combinations according to the truth table.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA			Volts								
	I_{OL1}	I_{OL2}	I_{CEX}	V_{IL}	V_{IH}	V_{IHH}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	
MC5445, MC54145	20	80	0.25	0.4	2.4	5.5	2.0	0.8	5.0	4.5	5.5	
MC7445, MC74145	20	80	0.25	0.4	2.4	5.5	2.0	0.8	5.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC5445/MC54145 Test Limits -55 to +125°C			MC7445/MC74145 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										Gnd
			Min	Max	Unit	Min	Max	Unit	I_{OL1}	I_{OL2}	I_{CEX}	V_{IL}	V_{IH}	V_{IHH}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	
Input																			
Forward Current	I_F	12	–	-1.6	mAdc	–	-1.6	mAdc	–	–	–	12	–	–	–	–	–	–	16	8
Leakage Current	I_{R1}	12	–	40	μAdc	–	40	μAdc	–	–	–	–	12	–	–	–	–	–	16	8
	I_{R2}	12	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	12	–	–	–	–	16	8
Output																			
Output Voltage	V_{OL}	1	–	0.9	Vdc	–	0.9	Vdc	–	1	–	–	–	–	–	12,13,14,15	–	16	–	8
		1	–	0.4	Vdc	–	0.4	Vdc	1	–	–	–	–	–	–	12,13,14,15	–	16	–	8
MC5445/7445	V_{CEX}	1	30	–	Vdc	30	–	Vdc	–	–	1	–	–	–	12,13,14,15	–	–	–	16	8
MC54145/74145		1	15	–	Vdc	15	–	Vdc	–	–	1	–	–	–	12,13,14,15	–	–	–	16	8
Power Requirements (Total Device)																			
Power Supply Drain	I_{PD}	16	–	62	mAdc	–	70	mAdc	–	–	–	–	–	–	–	–	–	–	16	8,12,13,14,15
Switching Parameters									Pulse In		Pulse Out								
Turn-On Delay	t_{pd-}	15,1	–	50#	ns	–	50#	ns	15		1	12,13,14	–	–	–	–	16	–	–	8
Turn-Off Delay	t_{pd+}	15,1	–	50#	ns	–	50#	ns	15		1	12,13,14	–	–	–	–	16	–	–	8

#Tested only at 25°C.

TYPICAL APPLICATIONS

Two MC5445/7445 or MC54145/74145 decoder/drivers (depending on drive requirements) may be used to perform 4-line to 16-line decoding. Data inputs A, B, and C are applied to both decoder/drivers, while input D is applied to one decoder and $\overline{D}$ to the other. (See Figure 1.)

In addition to the obvious decoder applications, these circuits can also be used for data distribution (Figure 2). Inputs A, B, and C of the decoder/driver are used as control inputs, while the D input serves as the data input. In a typical compound data routing application, origin data is selected by the control inputs of the MC54151/74151 8-channel data selector. The data is then routed to the proper destination by means of the MC5445/7445 decoder/driver control lines.

FIGURE 1 – BINARY-TO-DECIMAL DECODING USING MC5445/7445 OR MC54145/74145

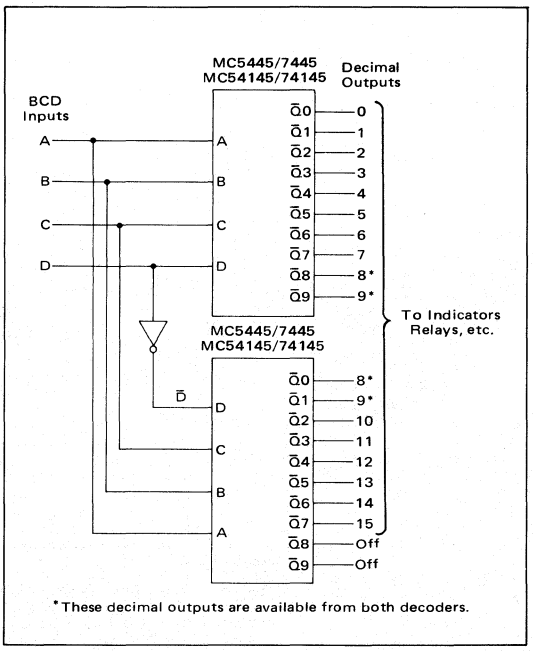
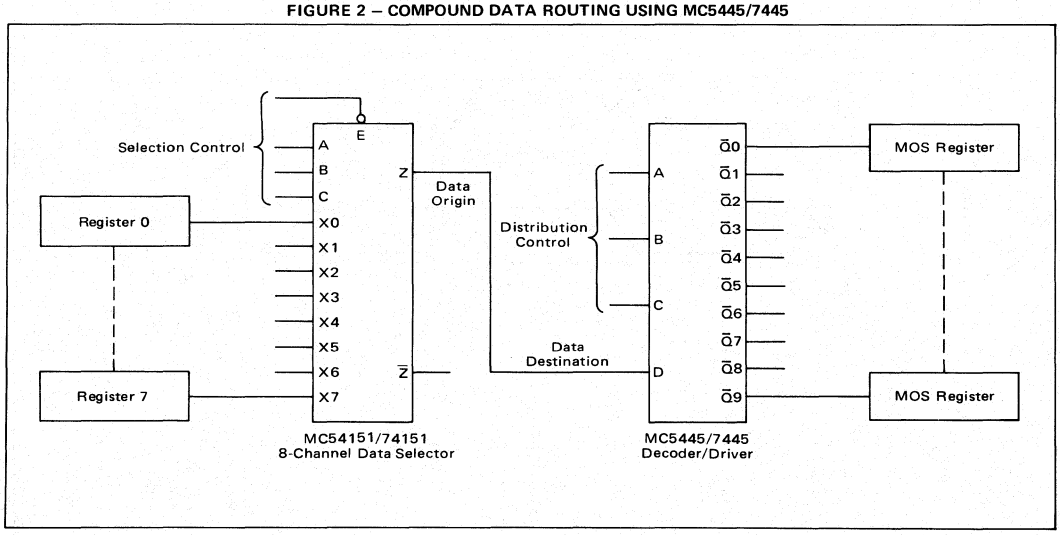
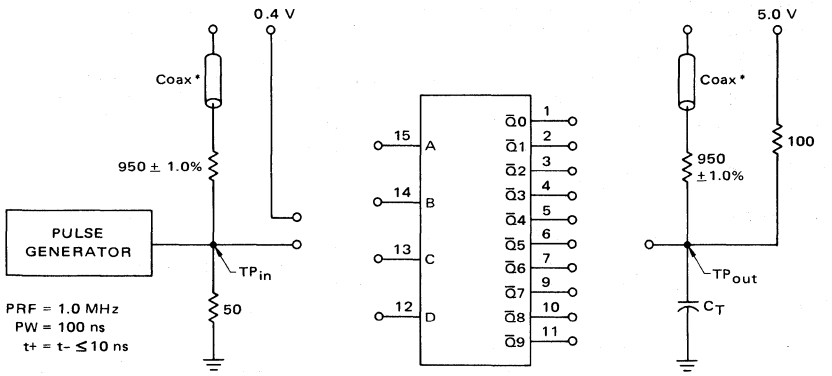


FIGURE 2 – COMPOUND DATA ROUTING USING MC5445/7445

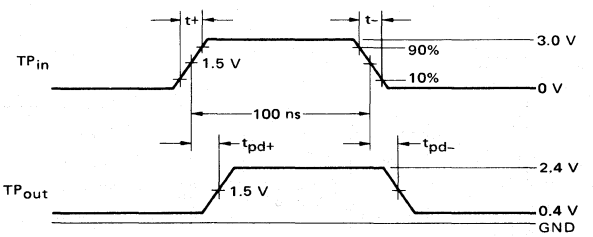


SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

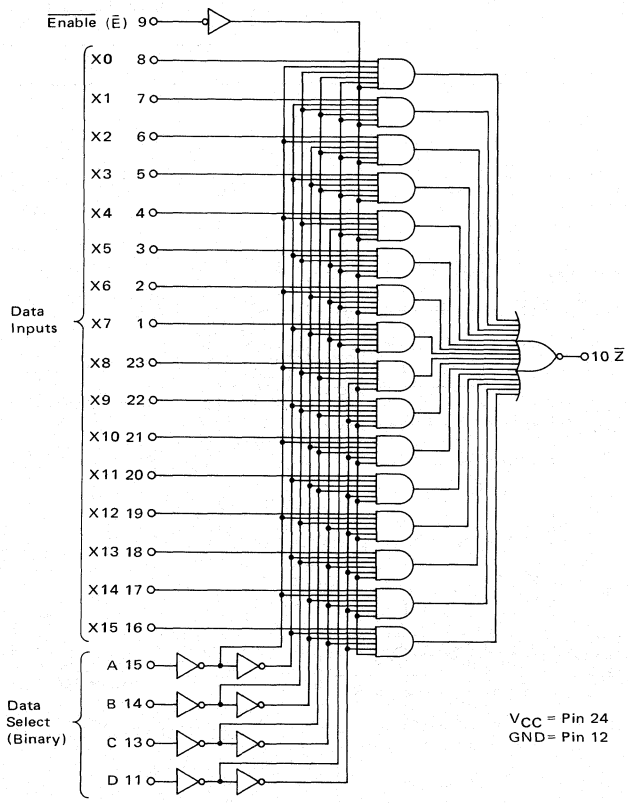


MC54150
MC74150

Compatible with MC5400/7400 Series devices.

ADVANCE INFORMATION/PRODUCT PREVIEW*

Soon to be announced, the MC54150/74150 16-channel data selector routes digital data present at one of the 16 inputs to the output, Z. The input data to be routed is chosen according to the select code (binary number) present at the select inputs.



$$Z = E \bullet (\bar{A}\bar{B}\bar{C}\bar{D}\,X0 + A\bar{B}\bar{C}\bar{D}\,X1 + \bar{A}B\bar{C}\bar{D}\,X2 + AB\bar{C}\bar{D}\,X3 + \bar{A}\bar{B}C\bar{D}\,X4 + A\bar{B}C\bar{D}\,X5 + \ldots + ABCD\,X15)$$

Total Power Dissipation = 200 mW typ/pkg
Propagation Delay Time = 8.5 to 35 ns typ

*Products to be introduced

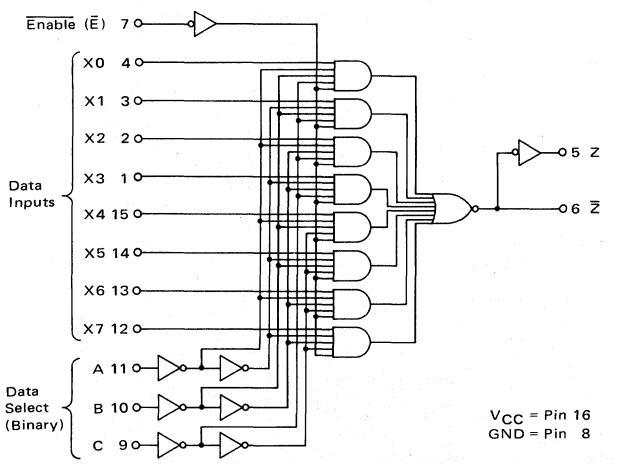
MC54151
MC74151

Compatible with MC5400/7400 Series devices.

ADVANCE INFORMATION/PRODUCT PREVIEW *

Total Power Dissipation = 145 mW typ/pkg
Propagation Delay Time = 8.5 to 35 ns typ

Soon to be announced, the MC54151/74151 8-channel data selector routes digital data present at one of the eight inputs to complementary outputs, Z and $\overline{Z}$. The input data to be routed is chosen according to the select code (binary number) present at the three select inputs.



$$Z = E \bullet (\bar{A}\bar{B}\bar{C}\,X0 + A\bar{B}\bar{C}\,X1 + \bar{A}B\bar{C}\,X2 + AB\bar{C}\,X3 + \bar{A}\bar{B}C\,X4 + A\bar{B}C\,X5 + \bar{A}BC\,X6 + ABC\,X7)$$

*Products to be introduced

MTTL

INTEGRATED CIRCUITS

MC8200/MC7200 SERIES

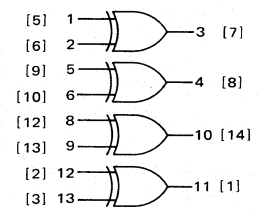
MTTL

MC8200/MC7200 SERIES
COMPLEX FUNCTIONS
INTEGRATED CIRCUITS

INDEX

MC8241F, L*
MC7241F, L, P*

ADVANCE INFORMATION/NEW PRODUCT



$3 = 1 \bullet \overline{2} + \overline{1} \bullet 2$

V_{CC} = Pin 14 [4]
GND = Pin 7 [11]

Numbers at ends of terminals represent pin numbers for devices in the dual in-line package.
Numbers in brackets represent pin numbers for devices in the flat package.

This device contains two independent gating structures to perform the Exclusive OR function on two input variables. The output employs the totem-pole structure.

Input Loading Factor = 2
Output Loading Factor = 10
Total Power Dissipation = 225 mW typ/pkg

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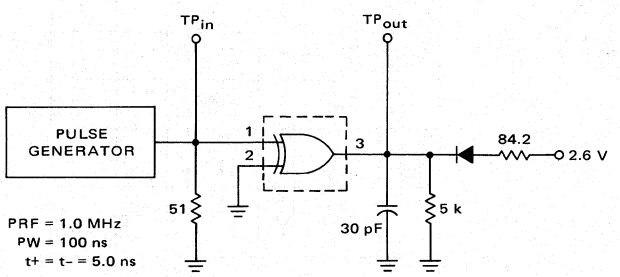
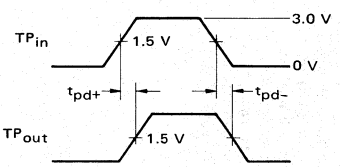
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



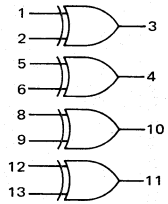


5 kΩ and 30 pF include jig and scope.

*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Pin numbers indicated are for devices in dual in-line packages only. To test devices in the flat package, substitute pin numbers shown in brackets on the logic diagram on the first page of this data sheet.



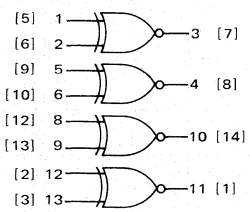
@ Test Temperature		TEST CURRENT/VOLTAGE VALUE mA I_{OL}	I_{OH}	I_{in}	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
MC8241	-55°C	16	-0.5	–	0.8	2.0	0.4	4.5	5.0	4.75	5.25
	+25°C	16	-0.5	10	0.8	2.0	0.4	4.5	5.0	4.75	5.25
	+125°C	16	-0.5	–	0.8	2.0	0.4	4.5	5.0	4.75	5.25
MC7241	0°C	16	-0.5	–	0.8	2.0	0.4	4.5	5.0	4.75	5.25
	+25°C	16	-0.5	10	0.8	2.0	0.4	4.5	5.0	4.75	5.25
	+75°C	16	-0.5	–	0.8	2.0	0.4	4.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC8241 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC7241 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																											
Forward Current	I_F	1	-0.1	-3.2	-0.1	-3.2	-0.1	-3.2	mAdc	-0.1	-3.2	-0.1	-3.2	-0.1	-3.2	mAdc	–	–	–	–	–	1	2	–	–	14	7
		2	-0.1	-3.2	-0.1	-3.2	-0.1	-3.2	mAdc	-0.1	-3.2	-0.1	-3.2	-0.1	-3.2	mAdc	–	–	–	–	–	2	1	–	–	14	7
Leakage Current	I_R	1	–	50	–	50	–	50	μAdc	–	50	–	50	–	50	μAdc	–	–	–	–	–	–	1	14	–	–	2,7
		2	–	50	–	50	–	50	μAdc	–	50	–	50	–	50	μAdc	–	–	–	–	–	–	2	14	–	–	1,7
Breakdown Voltage	BV_{in}	1	–	–	6.0	–	–	–	Vdc	–	–	6.0	–	–	–	Vdc	–	–	1	–	–	–	–	14	–	–	2,7
		2	–	–	6.0	–	–	–	Vdc	–	–	6.0	–	–	–	Vdc	–	–	2	–	–	–	–	14	–	–	1,7
Output																											
Output Voltage	V_{OL}	3	–	0.4	–	0.4	–	0.4	Vdc	–	0.4	–	0.4	–	0.4	Vdc	3	–	–	–	1,2	–	–	–	14	–	7
	V_{OH}	3	2.6	–	2.8	–	2.6	–	Vdc	2.6	–	2.8	–	2.6	–	Vdc	–	3	–	1	2	–	–	–	14	–	7
		3	2.6	–	2.8	–	2.6	–	Vdc	2.6	–	2.8	–	2.6	–	Vdc	–	3	–	2	1	–	–	–	14	–	7
Short Circuit Current	I_{SC}	3	–	–	-20	-70	–	–	mAdc	–	–	-20	-70	–	–	mAdc	–	–	–	–	–	–	1	14	–	–	2,3,7
Power Requirements (Total Device)																											
Power Supply Drain	I_{PD}	14	–	–	–	57	–	–	mAdc	–	–	–	57	–	–	mAdc	–	–	–	–	–	–	–	–	–	14	1,6,7,8,13
Switching Parameters					Typ	Max						Typ	Max				Pulse In		Pulse Out								
Turn-On Delay	t_{pd-}	3	–	–	10	–	–	–	ns	–	–	10	–	–	–	ns	1		3	–	–	–	14	–	–	2,7
Turn-Off Delay	t_{pd+}	3	–	–	10	–	–	–	ns	–	–	10	–	–	–	ns	1		3	–	–	–	14	–	–	2,7

QUAD EXCLUSIVE
"NOR" GATE
(Open Collector)

MC8242F, L*
MC7242F, L, P*

ADVANCE INFORMATION/NEW PRODUCT



$3 = \overline{1} \cdot \overline{2} + 1 \cdot 2$

V_{CC} = Pin 14 [4]
GND = Pin 7 [11]

Numbers at ends of terminals represent pin numbers for devices in the dual in-line package.
Numbers in brackets represent pin numbers for devices in the flat package.

This device contains four independent Exclusive NOR gates with open collector outputs which may be used to implement digital comparison functions. A four-bit comparison may be made by connecting the outputs together.

Input Loading Factor = 2
Output Loading Factor = 10
Total Power Dissipation = 170 mW typ/pkg

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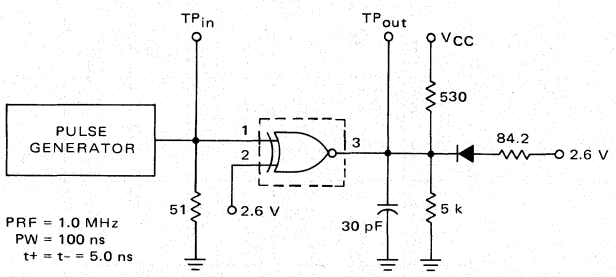
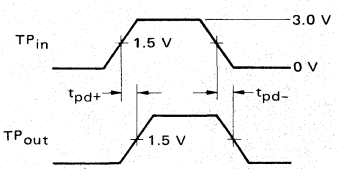
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



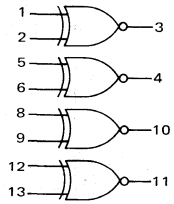


5 kΩ and 30 pF include jig and scope.

*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

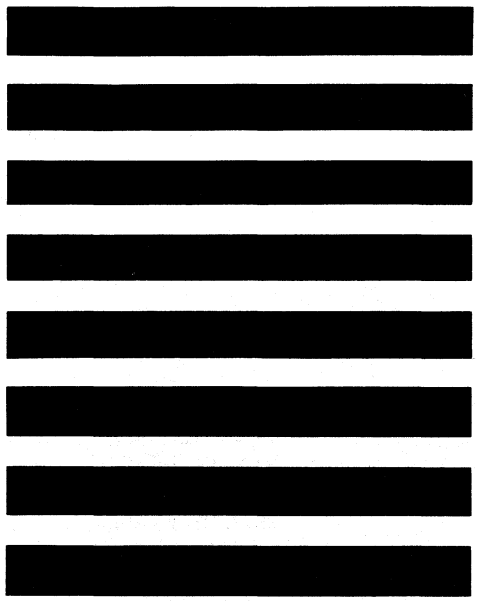
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Pin numbers indicated are for devices in dual in-line packages only. To test devices in the flat package, substitute pin numbers shown in brackets on the logic diagram on the first page of this data sheet.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUE								
		mA		Volts						
		I_{OL}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
MC8242	-55°C	25	–	0.8	2.0	0.4	4.5	5.0	4.75	5.25
	+25°C	25	10	0.8	2.0	0.4	4.5	5.0	4.75	5.25
	+125°C	25	–	0.8	2.0	0.4	4.5	5.0	4.75	5.25
MC7242	0°C	25	–	0.8	2.0	0.4	4.5	5.0	4.75	5.25
	+25°C	25	10	0.8	2.0	0.4	4.5	5.0	4.75	5.25
	+75°C	25	–	0.8	2.0	0.4	4.5	5.0	4.75	5.25

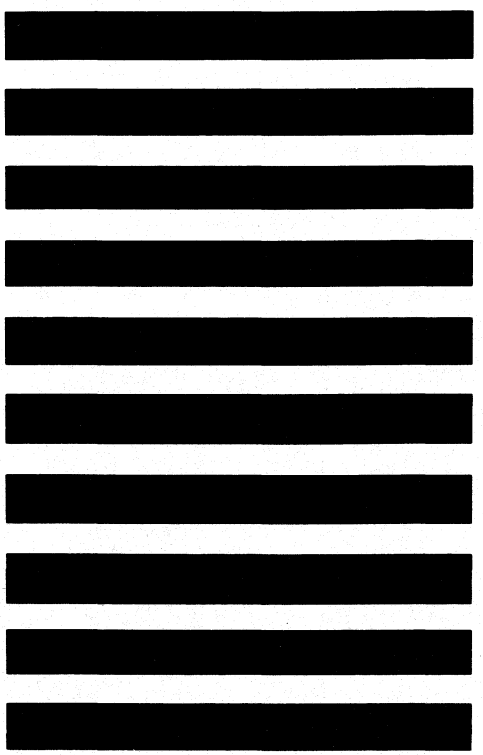
Characteristic	Symbol	Pin Under Test	MC8242 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC7242 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																										
Forward Current	I_F	1	-0.1	-3.2	-0.1	-3.2	-0.1	-3.2	mAdc	-0.1	-3.2	-0.1	-3.2	-0.1	-3.2	mAdc	–	–	–	–	1	2	–	–	14	7
		2	-0.1	-3.2	-0.1	-3.2	-0.1	-3.2	mAdc	-0.1	-3.2	-0.1	-3.2	-0.1	-3.2	mAdc	–	–	–	–	2	1	–	–	14	7
Leakage Current	I_R	1	–	50	–	50	–	50	µAdc	–	50	–	50	–	50	µAdc	–	–	–	–	–	1	14	–	–	2,7
		2	–	50	–	50	–	50	µAdc	–	50	–	50	–	–	µAdc	–	–	–	–	–	2	14	–	–	1,7
Breakdown Voltage	BV_{in}	1	–	–	6.0	–	–	–	Vdc	–	–	6.0	–	–	–	Vdc	–	1	–	–	–	–	14	–	–	2,7
		2	–	–	6.0	–	–	–	Vdc	–	–	6.0	–	–	–	Vdc	–	2	–	–	–	–	14	–	–	1,7
Output																										
Output Voltage	V_{OL}	3	–	0.4	–	–	–	0.4	Vdc	–	0.4	–	–	–	0.4	Vdc	3	–	1	2	–	–	–	14	–	7
		3	–	–	–	0.4	–	–	Vdc	–	–	–	0.4	–	–	Vdc	3	–	2	1	–	–	–	14	–	7
Leakage Current	I_{OLK}	3	–	–	–	25	–	25	µAdc	–	–	–	25	–	25	µAdc	–	–	–	1,2	–	–	3,14	–	–	7
Power Requirements (Total Device)																										
Power Supply Drain	I_{PD}	14	–	–	–	48	–	–	mAdc	–	–	–	48	–	–	mAdc	–	–	–	–	1,5,8,12	2,6,9,13	–	–	14	7
Switching Parameters					Typ	Max						Typ	Max				Pulse In		Pulse Out		V_{IHX} = 2.6 V					
Turn-On Delay	t_{pd-}	3	–	–	18	–	–	–	ns	–	–	18	–	–	–	ns	1		3		2		–	–	14	7
Turn-Off Delay	t_{pd+}	3	–	–	18	–	–	–	ns	–	–	18	–	–	–	ns	1		3		2		–	–	14	7



MTTL

INTEGRATED CIRCUITS

MC9300/MC8300 SERIES



MTTL

MC9300/MC8300 SERIES

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UNIVERSAL
4-BIT SHIFT REGISTER

MC9300L*
MC8300L,P*

Input Loading Factor
J, $\overline{K}$, $\overline{MR}$, D_{P0}, D_{P1}, D_{P2}, D_{P3} = 1
$\overline{PE}$ = 2.3
Clock = 4

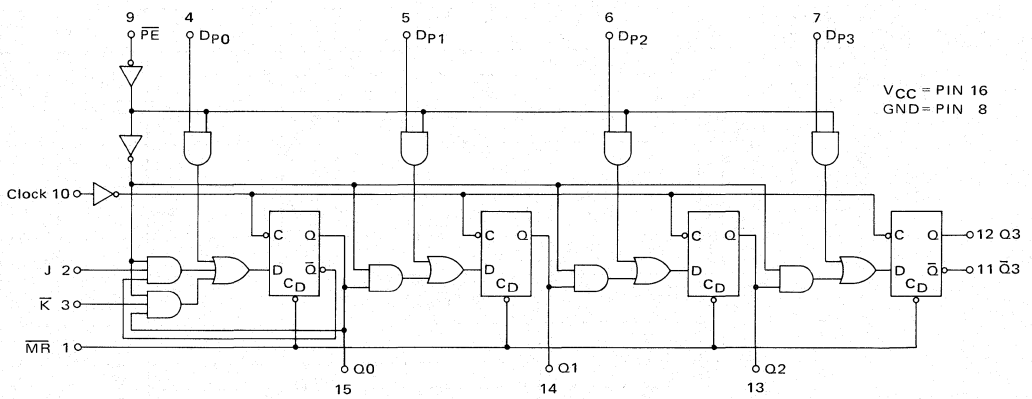
Output Loading Factor = 6

Total Power Dissipation = 300 mW typ/pkg

Propagation Delay Time = 25 ns typ

This serial/parallel shift register consists of four flip-flops operated in the synchronous mode. Functions available are shift left, shift right, serial-to-serial, parallel-to-parallel, serial to-parallel, and parallel-to-serial conversion.

This device operates on the positive-going edge of the clock pulse in both the serial and parallel mode. The device includes an internal clock buffer, input clamp diodes to reduce ringing, Q outputs for all four stages, $\overline{Q}$ output for the last stage, synchronous parallel entry, and an asychronous master reset. The J and $\overline{K}$ inputs are available, and may be tied together to produce a D input.



INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC9300 INPUT LOADING FACTOR	MC9300 OUTPUT LOADING FACTOR
MC9300	1.0	6
MC500	1.06	6.4
MC2100	0.7	4.25
MC3100	0.7	3.6
MC4300	1.0	4.65
MC5400	1.0	4.65
MC930**	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	5.6

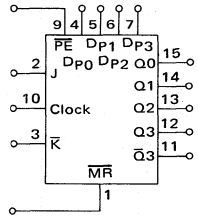
FAMILY	MC8300 INPUT LOADING FACTOR	MC8300 OUTPUT LOADING FACTOR
MC8300	1.0	6
MC400	1.0	5.45
MC2000	0.6	4.5
MC3000	0.7	4.25
MC4000	1.0	5.3
MC7400	1.0	5.3
MC830**	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	6.1

**Due to logic "1" state drive limitations of the MDTL family.

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one parallel data input. Other parallel data inputs are tested in the same manner. Further, test procedures are shown for only one output. Complete testing according to the Functional Test Diagram.

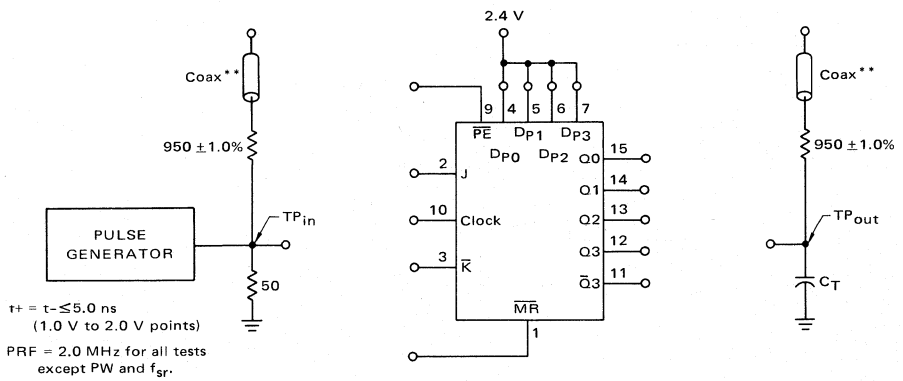


@ Test Temperature		TEST CURRENT/VOLTAGE VALUE mA I_{OL1}	I_{OL2}	I_{OH}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
MC9300	−55°C	9.6	7.44	−0.36	–	0.80	2.0	0.4	4.5	–	4.5	5.5
	+25°C	9.6	7.44	−0.36	−10	0.90	1.7	0.4	4.5	5.0	4.5	5.5
	+125°C	9.6	7.44	−0.36	–	0.80	1.4	0.4	4.5	–	4.5	5.5
MC8300	0°C	9.6	8.5	−0.36	–	0.85	1.9	0.45	4.5	–	4.75	5.25
	+25°C	9.6	8.5	−0.36	−10	0.85	1.8	0.45	4.5	5.0	4.75	5.25
	+75°C	9.6	8.5	−0.36	–	0.85	1.6	0.45	4.5	–	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC9300 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC8300 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Gnd
Input																												
Forward Current — $\overline{MR}$	I_{F1}	1	–	−1.6	–	−1.6	–	−1.6	mAdc	–	−1.6	–	−1.6	–	−1.6	mAdc	–	–	–	–	–	–	1	–	–	–	16	–	8
J		2	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	1	–	2	–	–	–	↓	–	↓
$\overline{K}$		3	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	4	3	–	–	–	↓	1	↓
D_{P0}		4	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	–	4	–	–	–	↓	–	↓
$\overline{PE}$		9	–	−3.68	–	−3.68	–	−3.68	↓	–	−3.68	–	−3.68	–	−3.68	↓	–	–	–	–	–	–	9	–	–	–	↓	–	↓
Clock		10	–	−6.4	–	−6.4	–	−6.4	↓	–	−6.4	–	−6.4	–	−6.4	↓	–	–	–	–	–	–	10	–	–	–	↓	–	↓
$\overline{MR}$	I_{F2}	1	–	−1.24	–	−1.24	–	−1.24	mAdc	–	−1.41	–	−1.41	–	−1.41	mAdc	–	–	–	–	–	–	1	–	–	16	–	–	8
J		2	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	1	–	2	–	–	↓	–	–	↓
$\overline{K}$		3	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	4	3	–	–	–	–	1	↓
D_{P0}		4	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	–	4	–	–	–	–	–	↓
$\overline{PE}$		9	–	−2.85	–	−2.85	–	−2.85	↓	–	−3.24	–	−3.24	–	−3.24	↓	–	–	–	–	–	–	9	–	–	–	–	–	↓
Clock		10	–	−4.95	–	−4.95	–	−4.95	↓	–	−5.65	–	−5.65	–	−5.65	↓	–	–	–	–	–	–	10	–	–	↓	–	–	↓
Leakage Current — $\overline{MR}$	I_R	1	–	60	–	60	–	60	μAdc	–	60	–	60	–	60	μAdc	–	–	–	–	–	–	–	1	–	–	16	–	8
J		2	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	–	–	2	–	–	↓	–	↓
$\overline{K}$		3	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	9	–	–	3	–	–	↓	–	↓
D_{P0}		4	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	–	–	–	4	–	–	↓	–	↓
$\overline{PE}$		9	–	140	–	140	–	140	↓	–	140	–	140	–	140	↓	–	–	–	–	–	–	–	9	–	–	↓	–	↓
Clock		10	–	240	–	240	–	240	↓	–	240	–	240	–	240	↓	–	–	–	–	–	–	–	10	–	–	↓	–	↓
Clamp Voltage — $\overline{MR}$	V_D	1	–	–	–	−1.5	–	–	Vdc	–	–	–	−1.5	–	–	Vdc	–	–	–	1	–	–	–	–	–	16	–	–	8
J		2	–	–	–	↓	–	–	↓	–	–	–	↓	–	–	↓	–	–	–	2	–	–	–	–	–	↓	–	–	↓
$\overline{K}$		3	–	–	–	↓	–	–	↓	–	–	–	↓	–	–	↓	–	–	–	3	–	–	–	–	–	↓	–	–	↓
D_{P0}		4	–	–	–	↓	–	–	↓	–	–	–	↓	–	–	↓	–	–	–	4	–	–	–	–	–	↓	–	–	↓
$\overline{PE}$		9	–	–	–	↓	–	–	↓	–	–	–	↓	–	–	↓	–	–	–	9	–	–	–	–	–	↓	–	–	↓
Clock		10	–	–	–	↓	–	–	↓	–	–	–	↓	–	–	↓	–	–	–	10	–	–	–	–	–	↓	–	–	↓
Output																												
Output Voltage	V_{OL}	12	–	0.4	–	0.4	–	0.4	Vdc	–	0.45	–	0.45	–	0.45	Vdc	12	–	–	–	4,5,6,7,9	–	–	–	–	–	16	1	8
		12	–	0.4	–	0.4	–	0.4	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	12	–	–	4,5,6,7,9	–	–	–	–	16	–	1	8
	V_{OH}	11	2.4	–	2.4	–	2.4	–	Vdc	2.4	–	2.4	–	2.4	–	Vdc	–	–	11	–	4,5,6,7,9	–	–	–	–	16	–	1	8
Power Requirements (Total Device)																												
Power Supply Drain	I_{PD}	16	–	–	–	75	–	–	mAdc	–	–	–	80	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	1,8

Pulse 1: V_{IH}, V_{IL}, 100 ns min

SWITCHING TIME TEST CIRCUIT



t+ = t-≤5.0 ns
(1.0 V to 2.0 V points)

PRF = 2.0 MHz for all tests except PW and f_{sr}.

Three pulse generators are required and must be slaved together to provide the waveforms shown.

**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.

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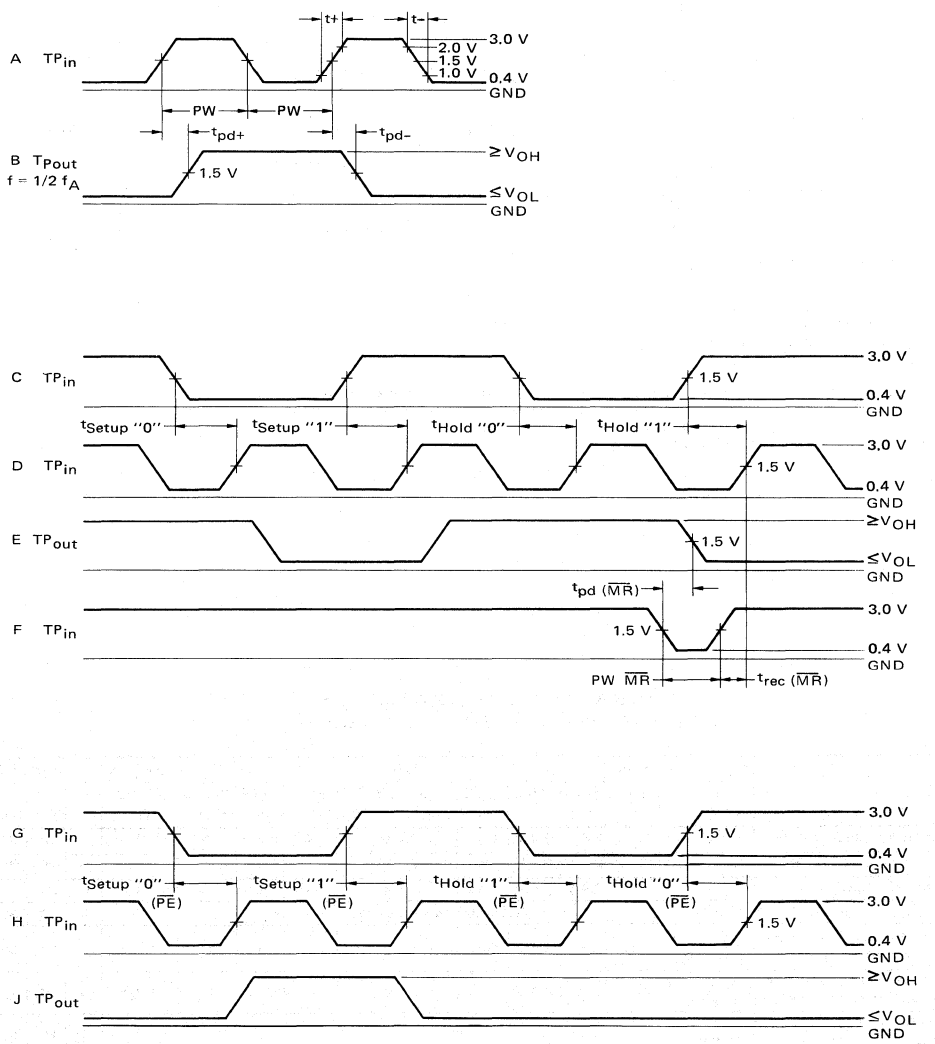
SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	PIN UNDER TEST	INPUT Pin 1 $\overline{MR}$	Pin 2 J	Pin 3 K	Pins 4, 5, 6 D_{P0}, D_{P1}, D_{P2}	Pin 7 D_{P3}	Pin 9 $\overline{PE}$	Pin 10 Clock	OUTPUT Pin 12 Q3	VALUE Min	Typ	Max	Unit
Turn-Off Delay, Clock to Q3	t_{pd+}	10,12	2.4 V	2.4 V	Gnd	2.4 V	2.4 V	2.4 V	A	B	–	18	35	ns
Turn-On Delay, Clock to Q3	t_{pd-}	10,12	2.4 V	2.4 V	Gnd	2.4 V	2.4 V	2.4 V	A	B	–	25	45	ns
Maximum Shift Rate	f_{sr}	12	2.4 V	2.4 V	Gnd	2.4 V	2.4 V	2.4 V	A	B	15	25	–	MHz
Minimum Clock Pulse Width	PW	Tested during each of the above tests.									–	13	35	ns
Minimum Data Input Setup Time (Serial or Parallel Inputs)	t_{Setup} "1" t_{Setup} "0"	7,12	F	2.4 V	Gnd	2.4 V	C	Gnd	D	E ①	–	14	35	ns
Maximum Data Input Hold Time (Serial or Parallel Inputs)	t_{Hold} "1" t_{Hold} "0"	7,12	F	2.4 V	Gnd	2.4 V	C	Gnd	D	E ②	0	16	–	ns
Minimum Recovery Time, $\overline{MR}$ Input	t_{rec}	Tested during Data Input t_{Setup} and t_{Hold} tests.									–	19	30	ns
Minimum $\overline{MR}$ Pulse Width	PW										–	15	30	ns
Turn-On Delay, $\overline{MR}$ to Q3	t_{pd-}	1,12	F	2.4 V	Gnd	2.4 V	2.4 V	Gnd	D	E	–	29	45	ns
Minimum $\overline{PE}$ Input Setup Time	t_{Setup} "1" t_{Setup} "0"	9,10	2.4 V	Gnd	Gnd	2.4 V	2.4 V	G	H	J ①	–	22	45	ns
Maximum $\overline{PE}$ Input Hold Time	t_{Hold} "1" t_{Hold} "0"	9,10	2.4 V	Gnd	Gnd	2.4 V	2.4 V	G	H	J ②	10	18	–	ns

① Output toggles. ② Output does not toggle.

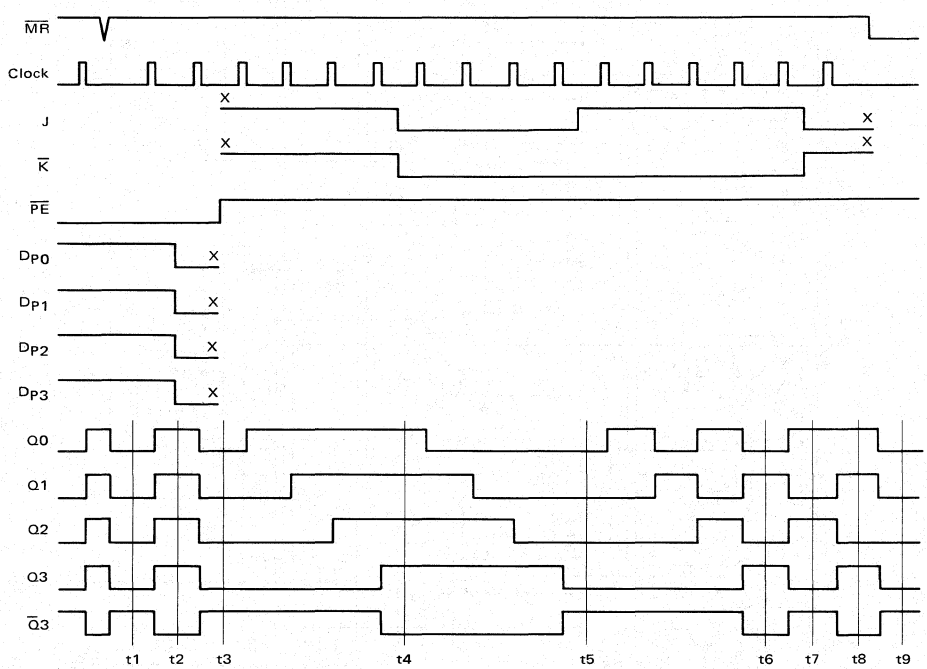
VOLTAGE WAVEFORMS



FUNCTIONAL DESCRIPTION

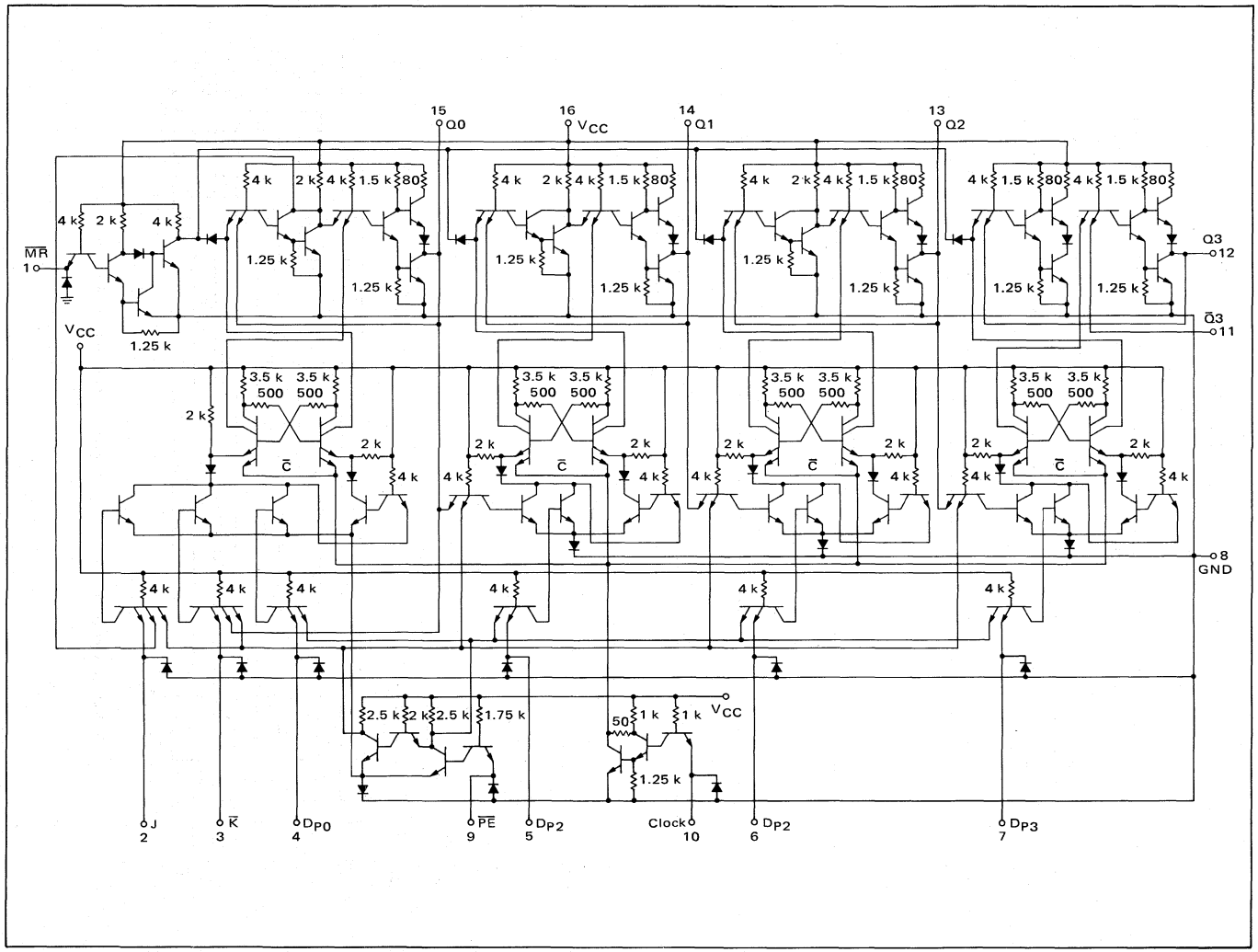
1. J and $\overline{K}$ inputs are made available on the first flip-flop of the register to provide full input logic capability without restrictions other than setup and release times. The simpler D type input can be obtained by wiring the J and $\overline{K}$ inputs together.
2. Parallel data inputs are provided to each stage of the register. These inputs are enabled only when the Parallel Enable is low. Information is transferred to the register on the positive transition of the clock. This information is shifted to the right on the next positive transition of the clock if the Parallel Enable is high. Shift left operation is achieved by driving the parallel inputs with the Q outputs of the right-adjacent stage. For this operation the Parallel Enable must be low.
3. An internal clock buffer has been included to reduce clock input loading, allowing the clock input of the register to be driven by a single gate.
4. The true output is provided for all stages; the complementary output is also provided for the last stage.
5. The master asynchronous $\overline{\text{reset}}$ input will clear the register independent of the conditions of the other inputs.

FUNCTIONAL DIAGRAM

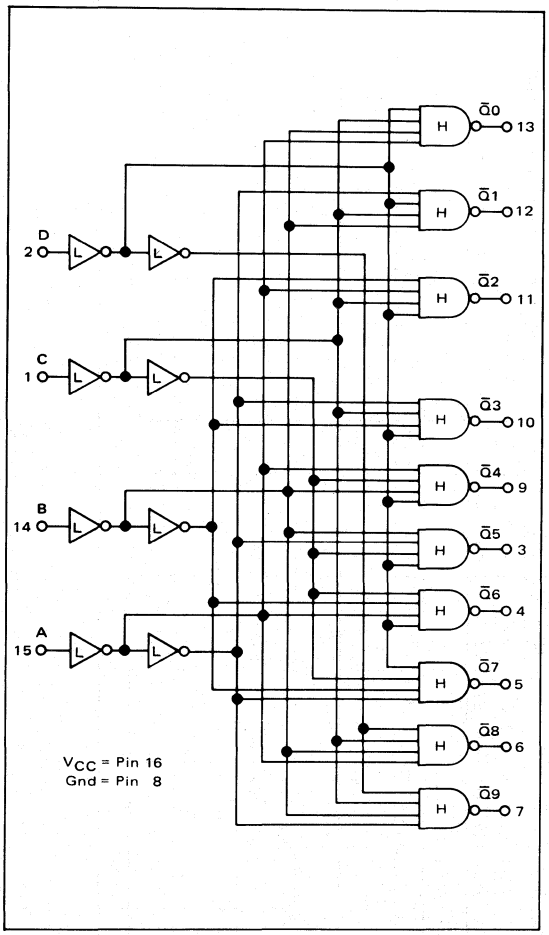


X = Voltage level of unspecified area(s) preceding or following "X" are unimportant.

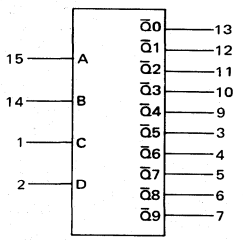
CIRCUIT SCHEMATIC



MC9301L*
MC8301L, P*



This decoder converts four-bit BCD inputs to select one-of-ten outputs. The selected output is in the logic "0" state while all other outputs are in the logic "1" state. When a binary code greater than nine is applied to the inputs, all outputs will be in the logic "1" state. This device is useful in memory selection, industrial control, and data routing applications.

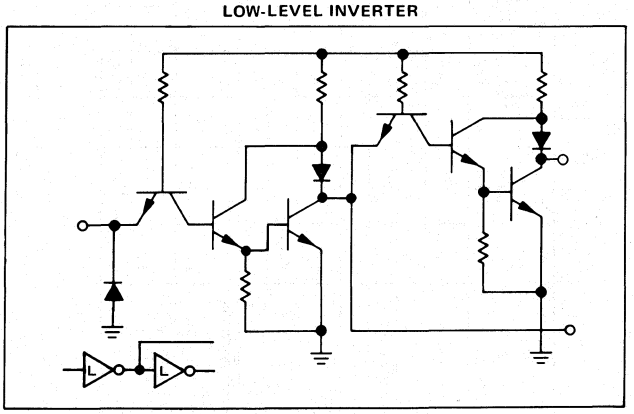


Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 125 mW typ/pkg
Propagation Delay Time = 22 ns typ

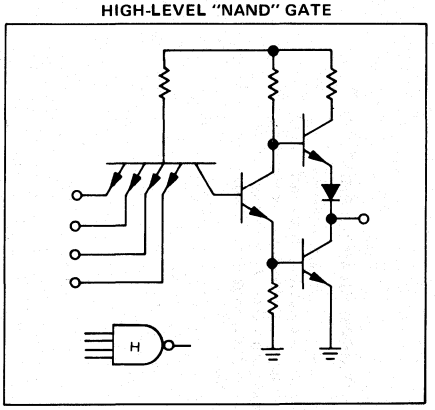
TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

LOW-LEVEL INVERTER



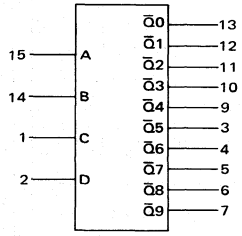
HIGH-LEVEL "NAND" GATE



*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in the same manner according to the truth table. Additionally, test all input-output combinations according to the truth table.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES											
		mA				Volts							
		I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC9301	−55°C	12.4	16	-0.6	-	0.80	2.0	0.4	4.5	-	4.5	5.5	-
MC9301	+25°C	12.4	16	-0.6	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5	2.4
MC9301	+125°C	12.4	16	-0.6	-	0.80	1.4	0.4	4.5	-	4.5	5.5	-
MC8301	0°C	14.1	16	-0.6	-	0.85	1.9	0.45	4.5	-	4.75	5.25	-
MC8301	+25°C	14.1	16	-0.6	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25	2.4
MC8301	+75°C	14.1	16	-0.6	-	0.85	1.6	0.45	4.5	-	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC9301 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC8301 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_{F1}	1	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	-	-	-	1	-	-	-	16	-	8
	I_{F2}	1	-	-1.24	-	-1.24	-	-1.24	mAdc	-	-1.41	-	-1.41	-	-1.41	mAdc	-	-	-	-	-	-	1	-	-	16	-	-	8
Leakage Current	I_R	1	-	-	-	60	-	60	μAdc	-	60	-	60	-	60	μAdc	-	-	-	-	-	-	-	1	-	-	16	-	8
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	16	-	-	8
Output Output Voltage	V_{OL1}	3	-	0.4	-	0.4	-	0.4	Vdc	-	0.45	-	0.45	-	0.45	Vdc	3	-	-	-	2,14	1,15	-	-	-	16	-	-	8
	V_{OL2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	0.45	-	0.45	-	0.45	Vdc	-	3	-	-	2,14	1,15	-	-	-	-	16	-	8
	V_{OH}	3	2.4	-	2.4	-	2.4	-	Vdc	2.4	-	2.4	-	2.4	-	Vdc	-	-	3	-	14	1,2,15	-	-	-	16	-	-	8
Power Requirements (Total Device) Power Supply Drain	I_{PD}	16	-	-	-	50	-	-	mAdc	-	-	-	50	-	-	mAdc	Pulse In: -	Pulse Out: -	-	-	-	-	-	-	16	-	-	-	8
Switching Parameters Turn-On Delay	t_{pd-}	15,3	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	15	3	-	-	-	-	-	-	16	-	-	1	2,8,14
Turn-Off Delay	t_{pd+}	15,3	-	-	-	35	-	-	ns	-	-	-	35	-	-	ns	15	3	-	-	-	-	-	-	16	-	-	1	2,8,14

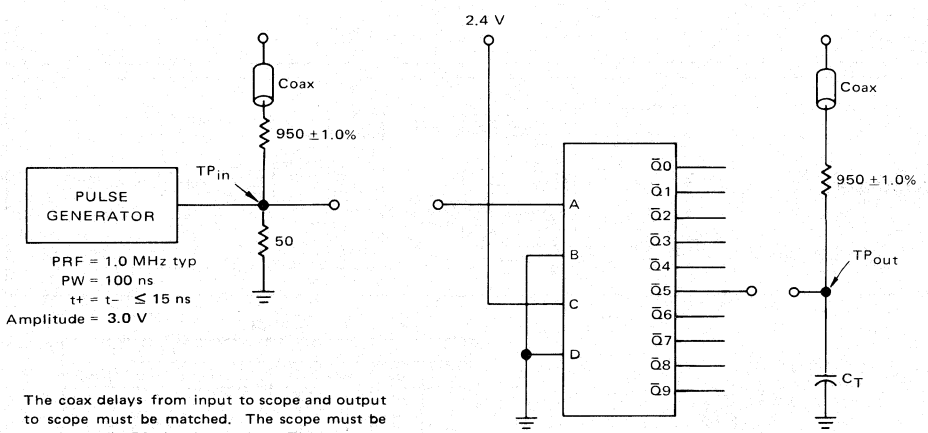
INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC9301 INPUT LOADING FACTOR	MC9301 OUTPUT LOADING FACTOR
MC9300	1.0	10
MC500	1.06	10.6
MC2100	0.7	7.0
MC3100	0.7	7.0
MC4300	1.0	10
MC5400	1.0	7.75
MC930*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	9.4

FAMILY	MC8301 INPUT LOADING FACTOR	MC8301 OUTPUT LOADING FACTOR
MC8300	1.0	10
MC400	1.0	9.0
MC2000	0.6	6.0
MC3000	0.7	7.4
MC4000	1.0	10
MC7400	1.0	8.75
MC830*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	10.8

*Due to logic "1" state drive limitations of the MDTL family.

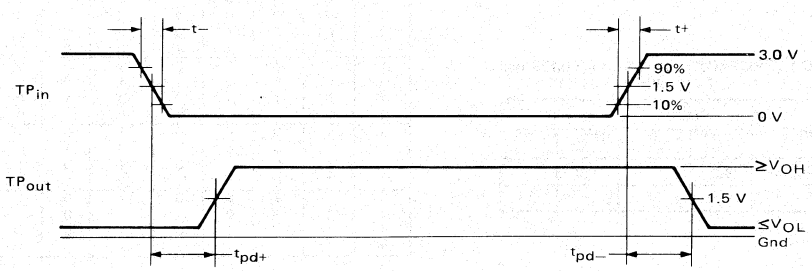
SWITCHING TIME TEST CIRCUIT



The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS

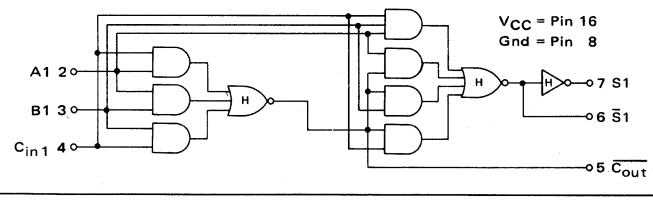


MC9304L*
MC8304L,P*

ADDER 1

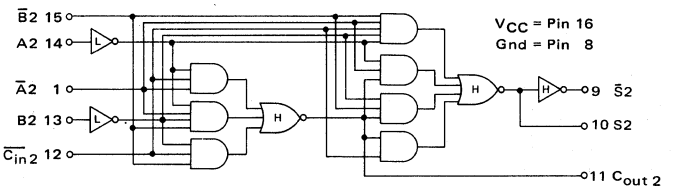
INPUT			OUTPUT		
C_{in1}	B1	A1	$\overline{C_{out1}}$	$\overline{S1}$	S1
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

This device consists of two independent, high-speed, binary full adders, with complementary Sum outputs. Adder two has provisions for both active high and active low inputs. Carry In and Carry Out of adder two are complementary to those of adder one. These choices provide greater design flexibility and minimum package count.



FULL ADDER 1

FULL ADDER 2



Input Loading Factors:
Adder 1: A1, B1, C_{in1} = 4
Adder 2: $\overline{A2}$, $\overline{B2}$, $\overline{C_{in2}}$ = 4
A2, B2 = 1

Output Loading Factors:
Adder 1: $\overline{C_{out1}}$ = 7
S1 = 10
$\overline{S1}$ = 9
Adder 2: C_{out2} = 7
S2 = 9
$\overline{S2}$ = 10

Total Power Dissipation = 110 mW typ/pkg

TYPICAL PROPAGATION DELAY TIMES (ns)
$T_A = 25^oC$

INPUT	t_{pd-}		t_{pd+}	
	$\overline{C_{out}}$	$\overline{S}$	$\overline{C_{out}}$	$\overline{S}$
C_{in}	8.0	–	8.0	–
A1	–	25	–	28

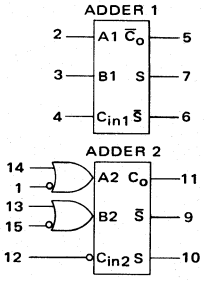
ADDER 2

INPUT					OUTPUT		
$\overline{C_{in}}$ 2	B2	A2	$\overline{B2}$	$\overline{A2}$	C_{out} 2	S2	$\overline{S2}$
0	0	0	0	0	1	1	0
0	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	1	1	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	0	1
0	0	1	1	1	1	0	1
0	1	0	0	0	1	1	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	1	0
0	1	1	0	1	1	1	0
0	1	1	1	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	0	1	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	1	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	1
1	1	0	0	1	0	1	0
1	1	0	1	0	1	0	1
1	1	0	1	1	0	1	0
1	1	1	0	0	1	0	1
1	1	1	0	1	1	0	1
1	1	1	1	0	1	0	1
1	1	1	1	1	1	0	1

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

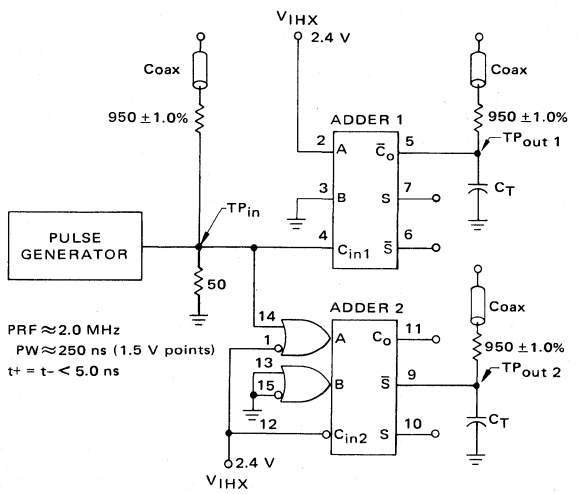
Test procedures are shown for only one adder. The other adder is tested in the same manner. Output tests are shown for only one set of input conditions. To complete testing, sequence through all input combinations according to the appropriate truth table.

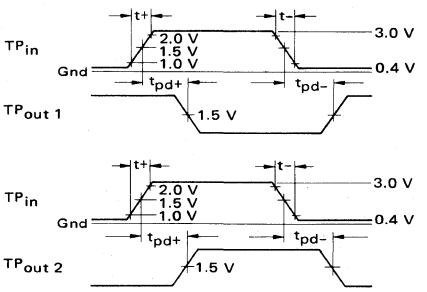


	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES																	
		mA										Volts							
		I_{OL1}	I_{OL2}	I_{OL3}	I_{OL4}	I_{OL5}	I_{OL6}	I_{OH1}	I_{OH2}	I_{OH3}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC9304	−55°C	16.0	14.4	11.2	12.4	11.2	8.70	-1.2	-1.08	-0.84	-	0.85	2.0	0.40	4.5	5.0	4.5	5.5	-
	+25°C	16.0	14.4	11.2	12.4	11.2	8.70	-1.2	-1.08	-0.84	-10	0.85	1.7	0.40	4.5	5.0	4.5	5.5	2.4
	+125°C	16.0	14.4	11.2	12.4	11.2	8.70	-1.2	-1.08	-0.84	-	0.85	1.4	0.40	4.5	5.0	4.5	5.5	-
MC8304	0°C	16.0	14.4	11.2	14.1	12.7	9.85	-1.2	-1.08	-0.84	-	0.8	1.9	0.45	4.5	5.0	4.75	5.25	-
	+25°C	16.0	14.4	11.2	14.1	12.7	9.85	-1.2	-1.08	-0.84	-10	0.9	1.8	0.45	4.5	5.0	4.75	5.25	2.4
	+75°C	16.0	14.4	11.2	14.1	12.7	9.85	-1.2	-1.08	-0.84	-	0.8	1.6	0.45	4.5	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC9304 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC8304 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OL4}	I_{OL5}	I_{OL6}	I_{OH1}	I_{OH2}	I_{OH3}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																																	
Forward Current	I_{F1}	1	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1	2,3,4,12,13,14,15	-	-	16	-	8
		12	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4		-	-	-	-	-	-	-	-	-	-	-	-	12	1,2,3,4,13,14,15	-	-		-	
		13	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6		-	-	-	-	-	-	-	-	-	-	-	-	13	1,2,3,4,12,14,15	-	-		-	
		14	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6		-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,12,13,15	-	-		-	
		15	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4	-	-6.4		-	-	-	-	-	-	-	-	-	-	-	-	15	1,2,3,4,12,13,14	-	-		-	
	I_{F2}	1	-	-4.96	-	-4.96	-	-4.96	-	-5.64	-	-5.64	-	-5.64	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1	2,3,4,12,13,14,15	-	16	-	-	8
		12	-	-4.96	-	-4.96	-	-4.96	-	-5.64	-	-5.64	-	-5.64		-	-	-	-	-	-	-	-	-	-	-	-	12	1,2,3,4,13,14,15	-			-	
		13	-	-1.24	-	-1.24	-	-1.24	-	-1.41	-	-1.41	-	-1.41		-	-	-	-	-	-	-	-	-	-	-	-	13	1,2,3,4,12,14,15	-			-	
		14	-	-1.24	-	-1.24	-	-1.24	-	-1.41	-	-1.41	-	-1.41		-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,3,4,12,13,15	-			-	
		15	-	-4.96	-	-4.96	-	-4.96	-	-5.64	-	-5.64	-	-5.64		-	-	-	-	-	-	-	-	-	-	-	-	15	1,2,3,4,12,13,14	-			-	
Leakage Current	I_R	1	-	240	-	240	-	240	-	240	-	240	-	240	μAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	16	-	2,3,4,8,12,13,14,15
		12	-	240	-	240	-	240	-	240	-	240	-	240		-	-	-	-	-	-	-	-	-	-	-	-	-	12	-	-		-	1,2,3,4,8,13,14,15
		13	-	60	-	60	-	60	-	60	-	60	-	60		-	-	-	-	-	-	-	-	-	-	-	-	-	13	-	-		-	1,2,3,4,8,12,14,15
		14	-	60	-	60	-	60	-	60	-	60	-	60		-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-		-	1,2,3,4,8,12,13,15
		15	-	240	-	240	-	240	-	240	-	240	-	240		-	-	-	-	-	-	-	-	-	-	-	-	-	15	-	-		-	1,2,3,4,8,12,13,14
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	16	-	8
		12	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	-	-	-	12	-	-	-	-	-	-		-	
		13	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	-	-	-	13	-	-	-	-	-	-		-	
		14	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	-	-	-	14	-	-	-	-	-	-		-	
		15	-	-	-		-	-	-	-	-		-	-		-	-	-	-	-	-	-	-	-	15	-	-	-	-	-	-		-	
Output																																	
Output Voltage	V_{OL}	9	-	0.4	-	0.4	-	0.4	-	0.45	-	0.45	-	0.45	Vdc	9	-	-	-	-	-	-	-	-	-	1,12,13,14,15	-	-	-	-	-	16	-	8
		10	-		-		-		-		-		-			-	10	-	-	-	-	-	-	-	12,13,14,15	1	-	-	-	-		-	
		11	-		-		-		-		-		-			-	-	11	-	-	-	-	-	-	12,13,14	1,15	-	-	-	-		-	
		9	-		-		-		-		-		-			-	-	-	9	-	-	-	-	-	1,12,13,14,15	-	-	-	-	-		-	
		10	-		-		-		-		-		-			-	-	-	-	10	-	-	-	-	12,13,14,15	1	-	-	-	-		-	
		11	-		-		-		-		-		-			-	-	-	-	-	11	-	-	-	12,13,14	1,15	-	-	-	-		-	
	V_{OH}	9	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	Vdc	-	-	-	-	-	-	9	-	-	-	12,13,14,15	1	-	-	-	-	16	-	8
		10		-		-		-		-		-		-		-	-	-	-	-	-	-	10	-	1,12,13,14,15	-	-	-	-	-		-	
		11		-		-		-		-		-		-		-	-	-	-	-	-	-	-	11	1,12,13,14,15	-	-	-	-	-		-	
Power Requirements (Total Device)																																	
Power Supply Drain	I_{PD}	16	-	-	-	45	-	-	-	-	-	50	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	16	-	-	8
Switching Parameters																Pulse In		Pulse Out															
Turn-On Delay	t_{pd-1}	4/5	-	-	-	13	-	-	-	-	-	15	-	-	ns	4		5		-	-	-	-	-	-	-	-	-	-	16	-	-	1,2,12	3,8,13,15
	t_{pd-2}	14/9	-	-	-	35	-	-	-	-	-	40	-	-	ns	14		9		-	-	-	-	-	-	-	-	-	-	16	-	-	1,2,12	3,8,13,15
Turn-Off Delay	t_{pd+1}	4/5	-	-	-	13	-	-	-	-	-	15	-	-	ns	4		5		-	-	-	-	-	-	-	-	-	-	16	-	-	1,2,12	3,8,13,15
	t_{pd+2}	14/9	-	-	-	40	-	-	-	-	-	45	-	-	ns	14		9		-	-	-	-	-	-	-	-	-	-	16	-	-	1,2,12	3,8,13,15

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

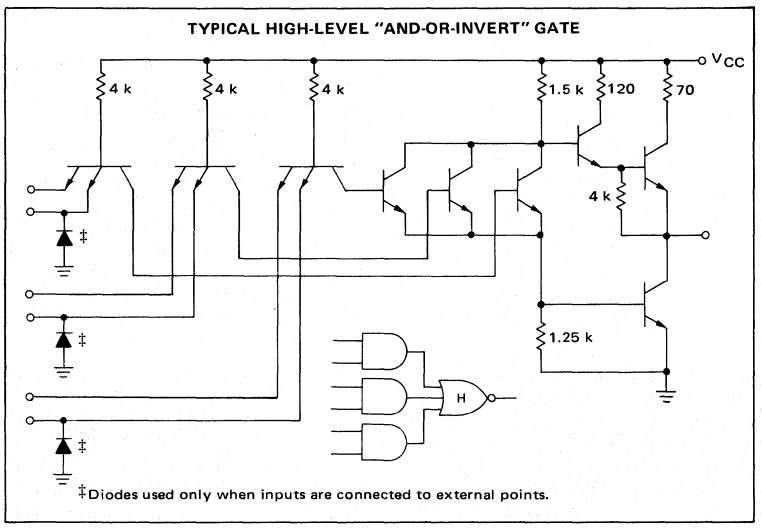


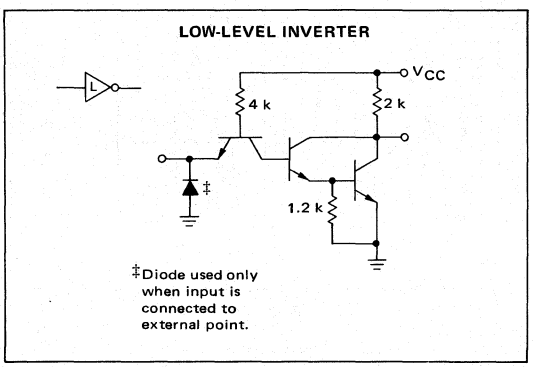


The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.

This full adder is constructed using high and low level gates interconnected as shown by the logic diagram.





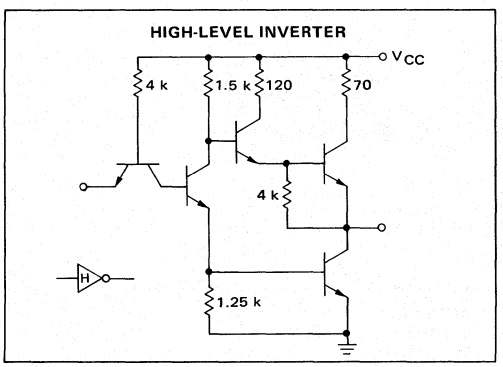
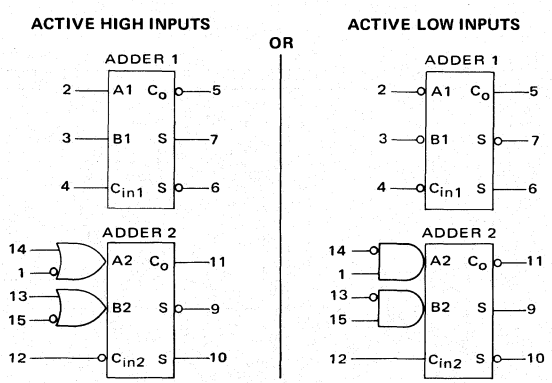


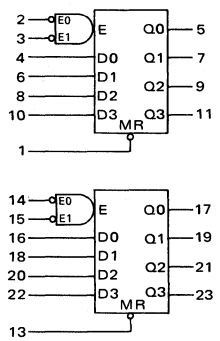
FIGURE 1 – FUNCTION BLOCK DIAGRAM

This diagram illustrates the adder function of the MC9304/8304 using either active low or high inputs.



DUAL 4-BIT LATCH

MC8308P*



V_{CC} = Pin 24
GND = Pin 12

Input Loading Factors:
D0, D1, D2, D3 = 1.5
MR, E0, E1 = 1.0
Output Loading Factor = 9

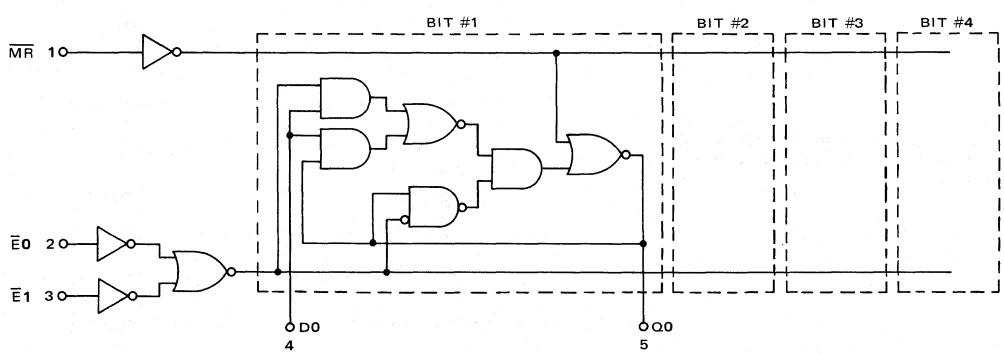
Total Power Dissipation = 325 mW typ/pkg
Propagation Delay Time (Enable to Output) = 25 ns typ

This device is constructed of AND, NAND, and NOR gates. Each half of the device contains four latches with common enable ($\overline{E}0$) and $\overline{E}1$) and common Master Reset ($\overline{MR}$). Data entered at the D input of each latch will appear at the corresponding Q output if the enable inputs are in the logic "0" state. When the enable inputs are in the logic "1" state, each latch will maintain the information present when the enable inputs were last in the logic "0" state. The master reset input overrides all other input states. When a logic "0" is applied to the $\overline{MR}$ input, all outputs of the quad latch will be forced to a logic "0".

INPUTS							OUTPUTS			
$\overline{MR}$	$\overline{E}0$	$\overline{E}1$	D3	D2	D1	D0	Q3	Q2	Q1	Q0
1	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0	0	1
1	0	0	0	0	1	0	0	0	1	0
1	0	0	0	0	1	0	0	1	0	0
1	0	0	1	0	0	0	1	0	0	0
1	0	0	0	0	1	1	0	0	1	1
1	0	0	0	1	0	1	0	1	0	1
1	0	0	1	0	0	1	1	0	0	1
1	0	0	0	1	1	0	0	1	1	0
1	0	0	1	0	1	0	1	0	1	0
1	0	0	1	1	0	0	1	1	0	0
1	0	0	0	1	1	1	0	1	1	1
1	0	0	1	1	0	1	1	0	1	1
1	0	0	1	1	1	0	1	1	0	0
1	0	0	1	1	1	1	1	1	1	1
1	1	0	X	X	X	X	LATCHED			
1	1	1	X	X	X	X	LATCHED			
0	X	X	X	X	X	X	LATCHED			
							0	0	0	0

X = Don't Care

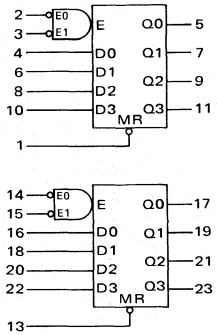
LOGIC DIAGRAM
1/2 OF DEVICE SHOWN



*P suffix = 24-pin dual in-line plastic package (Case 649).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one bit of one half of the device. The other bits are tested in the same manner.

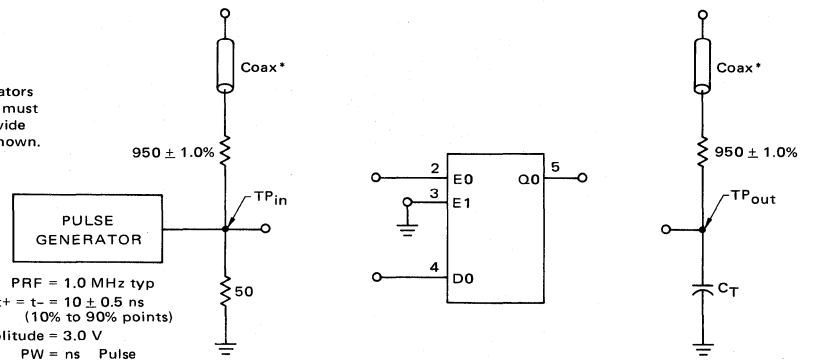


@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
0°C	12.7	14.4	-0.6	–	0.85	1.9	0.45	4.5	–	4.75	5.25
+25°C	12.7	14.4	-0.6	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25
+75°C	12.7	14.4	-0.6	–	0.85	1.6	0.45	4.5	–	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC8308 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_F	1	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	1	–	–	–	24	12
		2	–	-1.6	–	-1.6	–	-1.6	↓	–	–	–	–	–	–	2	–	–	–	↓	12
		4	–	-2.7	–	-2.7	–	-2.7	↓	–	–	–	–	–	–	–	–	–	–	↓	4, 12
Leakage Current	I_R	1	–	–	–	60	–	–	μAdc	–	–	–	–	–	–	–	1	–	–	24	12
		2	–	–	–	60	–	–	↓	–	–	–	–	–	–	–	2	–	–	↓	↓
		4	–	–	–	90	–	–	↓	–	–	–	–	–	–	–	4	–	–	↓	↓
Clamp Voltage	V_D	1	–	–	–	-1.5	–	–	Vdc	–	–	–	1	–	–	–	–	–	–	24	12
		2	–	–	–	↓	–	–	↓	–	–	–	2	–	–	–	–	–	–	↓	↓
		4	–	–	–	↓	–	–	↓	–	–	–	4	–	–	–	–	–	–	↓	↓
Output																					
Output Voltage	V_{OL1}	5	–	0.45	–	0.45	–	0.45	Vdc	5	–	–	–	2,3,4	–	–	–	–	24	–	12
	V_{OL2}	5	–	0.45	–	0.45	–	0.45	Vdc	–	5	–	–	2,3,4	–	–	–	–	–	24	12
	V_{OH}	5	2.4	–	2.4	–	2.4	–	Vdc	–	–	5	–	2,3	4	–	–	–	24	–	12
Power Requirements														V_{IL}							
(Total Device)																					
Power Supply Drain	I_{PHD}	24	–	–	–	117	–	–	mAdc	–	–	–	–	2,3,4,6,8,10,14, 15,16,18,20,22				24	–	–	12
Switching Parameters										Pulse In		Pulse Out									
Data Setup "1" Time	t_{Setup} "1"	5	–	–	2.0	–	–	–	ns	2, 4		5		–				24	–	–	3, 12
Data Hold "1" Time	t_{Hold} "1"	5	–	–	15	–	–	–	ns	2, 4		5		–				24	–	–	3, 12
Turn-Off Delay	t_{pd+}	5	–	–	–	44	–	–	ns	2, 4		5		–				24	–	–	3, 12
Data Setup "0" Time	t_{Setup} "0"	5	–	–	6.0	–	–	–	ns	2, 4		5		–				24	–	–	3, 12
Data Hold "0" Time	t_{Hold} "0"	5	–	–	8.0	–	–	–	ns	2, 4		5		–				24	–	–	3, 12
Turn-On Delay	t_{pd-}	5	–	–	–	30	–	–	ns	2, 4		5		–				24	–	–	3, 12

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

Two pulse generators are required and must be slaved to provide the waveforms shown.



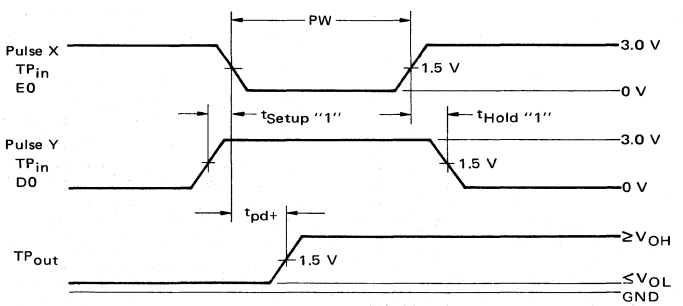
PRF = 1.0 MHz typ
$t+ = t- = 10 \pm 0.5$ ns
(10% to 90% points)
Amplitude = 3.0 V

PW = ns	Pulse
30	X
47	Y
44	Z

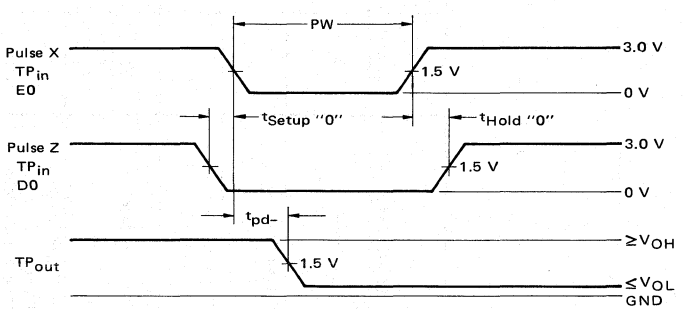
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

STORING A "1"



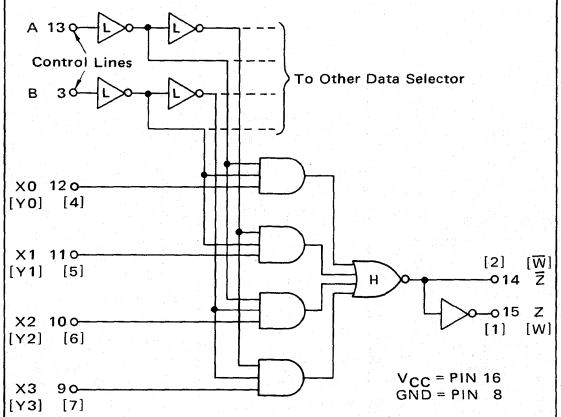
STORING A "0"



DUAL 4-CHANNEL
DATA SELECTOR

MC9309L*
MC8309L,P*

1/2 OF DEVICE SHOWN
(Numbers and symbols in parenthesis are for other half of device)



$\bar{Z} = \bar{A}\bar{B}X0 + A\bar{B}X1 + \bar{A}BX2 + ABX3$
$\bar{Z} = \bar{A}\bar{B}\bar{X0} + A\bar{B}\bar{X1} + \bar{A}B\bar{X2} + AB\bar{X3}$
$W = \bar{A}\bar{B}Y0 + A\bar{B}Y1 + \bar{A}BY2 + ABY3$
$\bar{W} = \bar{A}\bar{B}\bar{Y0} + A\bar{B}\bar{Y1} + \bar{A}B\bar{Y2} + AB\bar{Y3}$

Input Loading Factor = 1
Output Loading Factor: $Z, W = 10$
$\bar{Z}, \bar{W} = 9$
Total Power Dissipation = 150 mW typ/pkg

This device consists of two four-channel data selectors with common control lines, constructed from high-level AND-OR-INVERT gates with active pullup outputs, and low-level inverters on the control inputs. By selecting one of four logic combinations, information on one of the four data inputs will be routed to the complementary outputs.

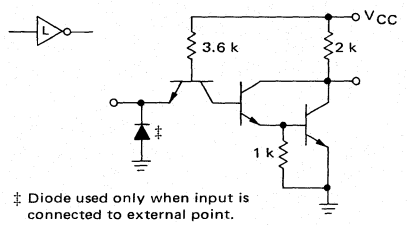
Data selectors are useful in applications where digital data is to be routed from one of several registers or locations to another register or location for processing.

The MC9309/8309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss.

TYPICAL PROPAGATION DELAY TIMES (ns)
$T_A = 25°C$

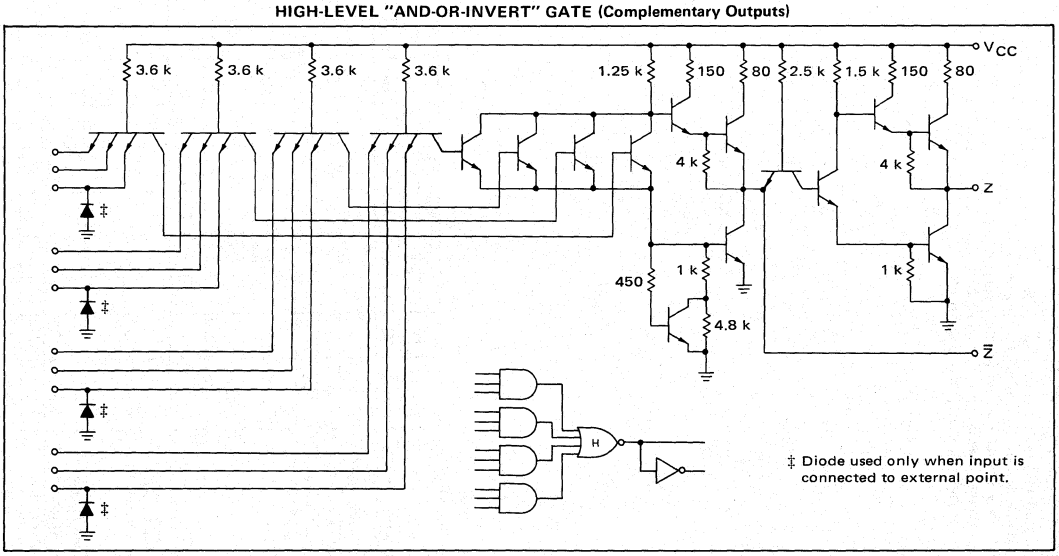
INPUT	Z	$\bar{Z}$	CONDITIONS
A	24	16	X0 = X2 = X3 = logic "0", X1 = logic "1". A and B are defined by the logic equations.
X1	17	9	

LOW-LEVEL INVERTER



‡ Diode used only when input is connected to external point.

HIGH-LEVEL "AND-OR-INVERT" GATE (Complementary Outputs)



‡ Diode used only when input is connected to external point.

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

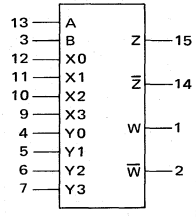
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in a similar manner according to the truth table. Additionally, test all input-output combinations according to the truth table.

TRUTH TABLE

INPUTS						OUTPUTS		INPUTS				OUTPUTS	
A	B	X0	X1	X2	X3	Z	$\overline{Z}$	Y0	Y1	Y2	Y3	W	$\overline{W}$
0	0	0	ϕ	ϕ	ϕ	0	1	0	ϕ	ϕ	ϕ	0	1
0	0	1	ϕ	ϕ	ϕ	1	0	1	ϕ	ϕ	ϕ	1	0
1	0	ϕ	0	ϕ	ϕ	0	1	ϕ	0	ϕ	ϕ	0	1
1	0	ϕ	1	ϕ	ϕ	1	0	ϕ	1	ϕ	ϕ	1	0
0	1	ϕ	ϕ	0	ϕ	0	1	ϕ	ϕ	0	ϕ	0	1
0	1	ϕ	ϕ	1	ϕ	1	0	ϕ	ϕ	1	ϕ	1	0
1	1	ϕ	ϕ	ϕ	0	0	1	ϕ	ϕ	ϕ	0	0	1
1	1	ϕ	ϕ	ϕ	1	1	0	ϕ	ϕ	ϕ	1	1	0

ϕ = Input level does not affect output.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES														
		mA							Volts							
		I_{OL1}	I_{OL2}	I_{OL3}	I_{OL4}	I_{OH1}	I_{OH2}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC9309	-55°C	12.4	11.2	16.0	14.4	-1.2	-1.08	–	0.80	2.0	0.4	4.5	–	4.5	5.5	–
MC9309	+25°C	12.4	11.2	16.0	14.4	-1.2	-1.08	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5	2.4
MC9309	+125°C	12.4	11.2	16.0	14.4	-1.2	-1.08	–	0.80	1.4	0.4	4.5	–	4.5	5.5	–
MC8309	0°C	14.1	12.7	16.0	14.4	-1.2	-1.08	–	0.85	1.9	0.45	4.5	–	4.75	5.25	–
MC8309	+25°C	14.1	12.7	16.0	14.4	-1.2	-1.08	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25	2.4
MC8309	+75°C	14.1	12.7	16.0	14.4	-1.2	-1.08	–	0.85	1.6	0.45	4.5	–	4.75	5.25	–

Characteristic	Symbol	Pin Under Test	MC9309 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC8309 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OL4}	I_{OH1}	I_{OH2}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																													
Forward Current	I_F	3	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	–	–	–	3	–	–	–	16	–	8
Leakage Current	I_R	3	–	60	–	60	–	60	–	60	–	60	–	60	μAdc	–	–	–	–	–	–	–	–	–	–	3	–	–	16	–	8
Clamp Voltage	V_D	3	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	–	3	–	–	–	–	16	–	–	–	8
Output																														
Output Voltage	V_{OL1}	1	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	1	–	–	–	–	–	–	6,13	3	–	–	–	16	–	–	8
		2	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	–	2	–	–	–	–	–	13	3,6	–	–	–	16	–	–	8
	V_{OL2}	1	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	–	–	1	–	–	–	–	6,13	3	–	–	–	–	16	–	8
		2	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	–	–	–	2	–	–	–	13	3,6	–	–	–	–	16	–	8
	V_{OH}	1	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	Vdc	–	–	–	–	1	–	–	13	3,6	–	–	–	16	–	–	8
		2	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	Vdc	–	–	–	–	–	2	–	6,13	3	–	–	–	16	–	–	8
Power Requirements (Total Device) Power Supply Drain	I_{PDH}	16	–	–	–	40	–	–	–	–	–	43	–	–	mAdc	–	–	–	–	–	–	–	–	3,4,5,6, 7,9,10, 11,12,13	–	–	16	–	–	–	8
Switching Parameters																Pulse In		Pulse Out													
Turn-On Delay	t_{pd-}	13/15	–	–	–	32	–	–	–	–	–	36	–	–	ns	13		15		–	–	–	–	–	–	–	16	–	–	11	3,8,9,10,12
Turn-Off Delay	t_{pd+}	13/15	–	–	–	32	–	–	–	–	–	36	–	–	ns	13		15		–	–	–	–	–	–	–	16	–	–	11	3,8,9,10,12

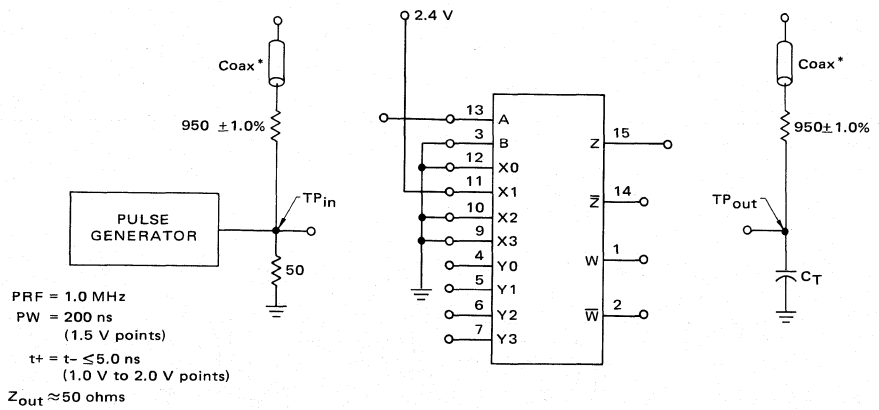
INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC9309 INPUT LOADING FACTOR	MC9309 OUTPUT LOADING FACTOR Z	MC9309 OUTPUT LOADING FACTOR $\overline{Z}$
MC9300	1.0	10	9.0
MC500	1.06	10.6	9.5
MC2100	0.7	7.0	6.3
MC3100	0.7	7.0	6.3
MC4300	1.0	10	9.0
MC5400	1.0	7.75	7.0
MC930*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	9.4	8.4

FAMILY	MC8309 INPUT LOADING FACTOR	MC8309 OUTPUT LOADING FACTOR Z	MC8309 OUTPUT LOADING FACTOR $\overline{Z}$
MC8300	1.0	10	9.0
MC400	1.0	9.0	8.1
MC2000	0.6	6.0	5.4
MC3000	0.7	7.4	6.6
MC4000	1.0	10	9.0
MC7400	1.0	8.75	7.8
MC830*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	10.8	9.7

*Due to logic "1" state drive limitations of the MDTL family.

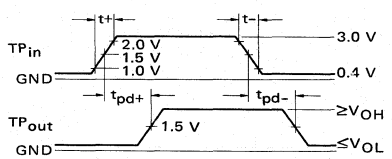
SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



PRF = 1.0 MHz
PW = 200 ns (1.5 V points)
t+ = t- ≤5.0 ns (1.0 V to 2.0 V points)
$Z_{out} \approx 50$ ohms

**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.



14

PRESETTABLE
DECADE COUNTER

MC9310L*
MC8310L,P*

COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

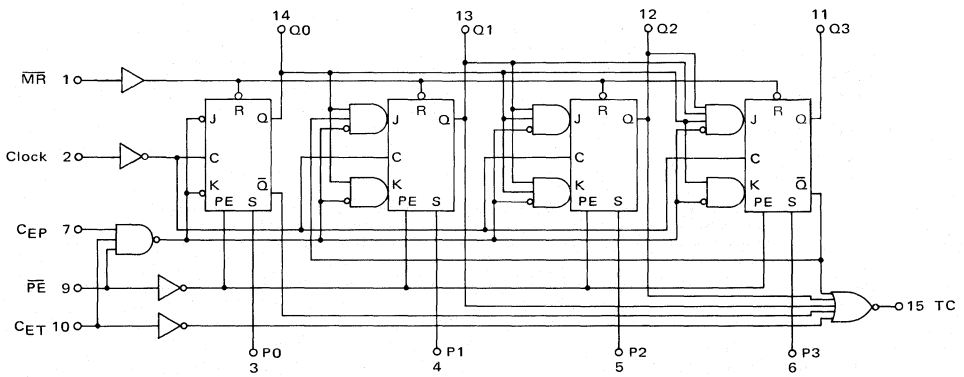
The MC9310/8310 decade counter consists of four J-K master-slave flip-flops plus additional gating to accomplish the counter function. Parallel inputs are provided for presetting data and parallel outputs for full counting flexibility.

An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of other input states. Parallel information may be preset only while the parallel enable ($\overline{PE}$) is in the logic "0" state.

Inputs C_{EP} and C_{ET} and output TC are useful in cascading counters. TC provides an output pulse each time the counter reaches its maximum count.

Input Loading Factors:
$\overline{MR}$, C_{EP} = 1
Clock, $\overline{PE}$, C_{ET} = 2
P0, P1, P2, P3 = 2/3
Output Loading Factor = 6

Total Power Dissipation = 300 mW typ/pkg
Propagation Delay Time = 14 to 35 ns typ
Toggle Frequency = 28 MHz typ

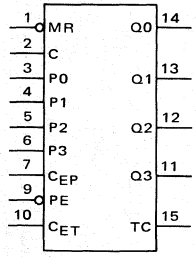


V_{CC} = Pin 16
GND = Pin 8

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

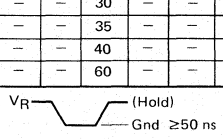
Test procedures are shown for only one input and one output. Test other inputs and outputs in a similar manner according to the truth table.



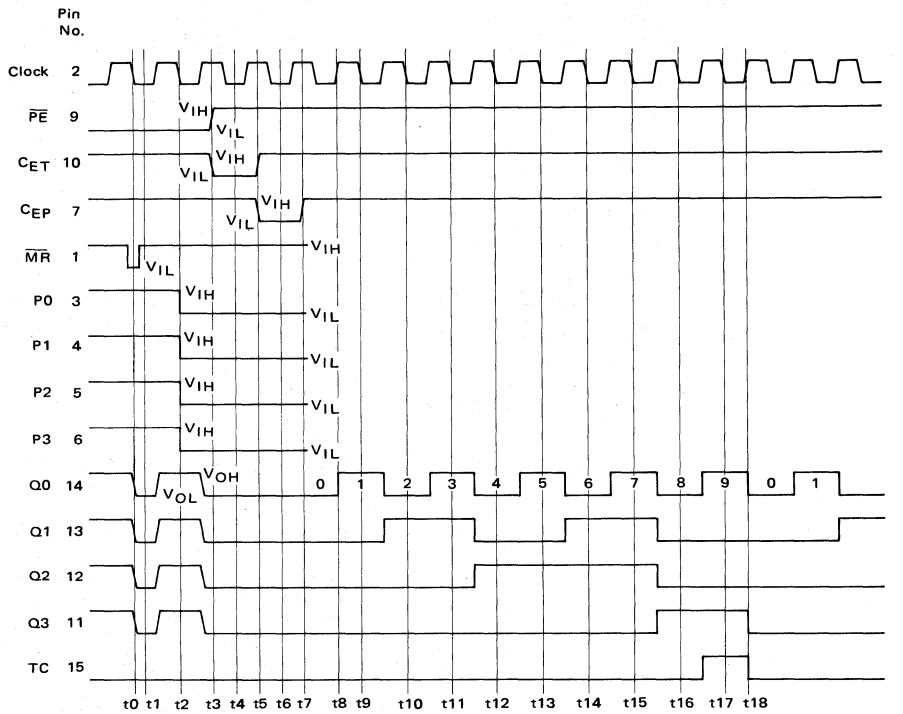
@ Test Temperature	TEST CURRENT/VOLTAGE VALUES										
	mA				Volts						
	I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
MC9310 -55°C	9.6	7.44	-0.36	–	0.80	2.0	0.4	4.5	–	4.5	5.5
MC9310 +25°C	9.6	7.44	-0.36	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5
MC9310 +125°C	9.6	7.44	-0.36	–	0.80	1.4	0.4	4.5	–	4.5	5.5
MC8310 0°C	9.6	8.50	-0.36	–	0.85	1.9	0.45	4.5	–	4.75	5.25
MC8310 +25°C	9.6	8.50	-0.36	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25
MC8310 +75°C	9.6	8.50	-0.36	–	0.85	1.6	0.45	4.5	–	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC9310 Test Limits							MC8310 Test Limits							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:								
			-55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																											
Forward Current	I_F	1	–	-1.6	–	-1.6	–	-1.6	mAdc	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	1	–	–	–	16	8
		2	–	-3.2	–	-3.2	–	-3.2	mAdc	–	-3.2	–	-3.2	–	-3.2	mAdc	–	–	–	–	–	–	2	–	–	–	16	8
		3	–	-1.07	–	-1.07	–	-1.07	mAdc	–	-1.07	–	-1.07	–	-1.07	mAdc	–	–	–	–	–	–	3	–	–	–	16	8
Leakage Current	I_R	1	–	60	–	60	–	60	µAdc	–	60	–	60	–	60	µAdc	–	–	–	–	–	–	–	1	–	–	16	8
		2	–	120	–	120	–	120	µAdc	–	120	–	120	–	120	µAdc	–	–	–	–	–	–	–	2	–	–	16	8
		3	–	40	–	40	–	40	µAdc	–	40	–	40	–	40	µAdc	–	–	–	–	–	–	–	3	–	–	16	8
Clamp Voltage	V_D	1	–	–	–	-1.5	–	–	Vdc	–	–	–	-1.5	–	–	Vdc	–	–	–	1	–	–	–	–	16	–	–	8
Output																											
Output Voltage	V_{OL1}	11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	11	–	–	See Timing Diagram @ t1					–	16	8
	V_{OL2}	11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	11	–	See Timing Diagram @ t1					16	–	8
		11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	11	–	See Timing Diagram @ t4					16	–	8
		11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	11	–	See Timing Diagram @ t6					16	–	8
	V_{OH}	11	2.4	–	2.4	–	2.4	–	Vdc	2.4	–	2.4	–	2.4	–	Vdc	–	–	11	See Timing Diagram @ t2					16	–	8
		11	2.4	–	2.4	–	2.4	–	Vdc	2.4	–	2.4	–	2.4	–	Vdc	–	–	11	See Timing Diagram @ t16					16	–	8
Power Requirements (Total Device)																											
Power Supply Drain Current	I_{PD}	16	–	–	–	75	–	–	mAdc	–	–	–	75	–	–	mAdc	–	–	–	–	–	2,7 9,10	–	1*	16	–	–	8
Switching Parameters																	Pulse In		Pulse Out		V_{IHX} = 3.0 Vdc						
Turn-On Delay – Q	t_{pd-}	2,14	–	–	–	30	–	–	ns	–	–	–	40	–	–	ns	2		14		1,3,4,5,6,7,9,10				16	–	–	8
Turn-Off Delay – Q	t_{pd+}	2,14	–	–	–	35	–	–	ns	–	–	–	30	–	–	ns	2		14		1,3,4,5,6,7,9,10				16	–	–	8
Turn-On Delay – TC	t_{pd-}	2,15	–	–	–	40	–	–	ns	–	–	–	70	–	–	ns	2		15		1,3,4,5,6,7,9,10				16	–	–	8
Turn-Off Delay – TC	t_{pd+}	2,15	–	–	–	60	–	–	ns	–	–	–	40	–	–	ns	2		15		1,3,4,5,6,7,9,10				16	–	–	8

*Apply after potentials have been applied to other pins.



TIMING DIAGRAM



NOTES

1. The Clock pulse must be in the high state during the high to low transition of C_{ET} and C_{EP}, and the low to high transition of $\overline{PE}$ for correct logic operation.
2. Pin conditions reflected on timing diagram for tests at time specified:

t0: Parallel (P) inputs high, Parallel Enable ($\overline{PE}$) low, asynchronous Master Reset ($\overline{MR}$) pulsed; Q outputs make transition from high to low.

t1: Measure both V_{OL1} and V_{OL2} on Q0, Q1, Q2, Q3 and TC before Clock goes high.

t2: Clock has been pulsed, Q outputs are high; measure V_{OH}.

t3: Clock is in high state while transitions of $\overline{PE}$ and C_{ET} occur (necessary condition). Parallel entry is now inhibited, P inputs are at the low level.

t4: Count enable (C_{ET}) is at the low level (disabled), count cannot occur; check Q outputs to see that they remain at the low level.

t5: C_{ET} is set to a high level and C_{EP} is set at the low level while the Clock is high.

t6: Check Q outputs to see that count is disabled, outputs remain low.

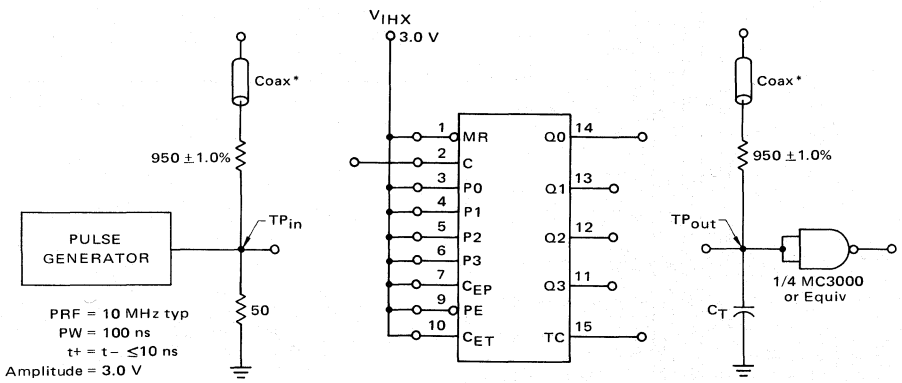
t7: C_{EP} is set high while Clock is high; count is now enabled.

t8: Clock is pulsed, count begins from 0000 to 0001.

t9 thru t17: Check Q and TC output states.

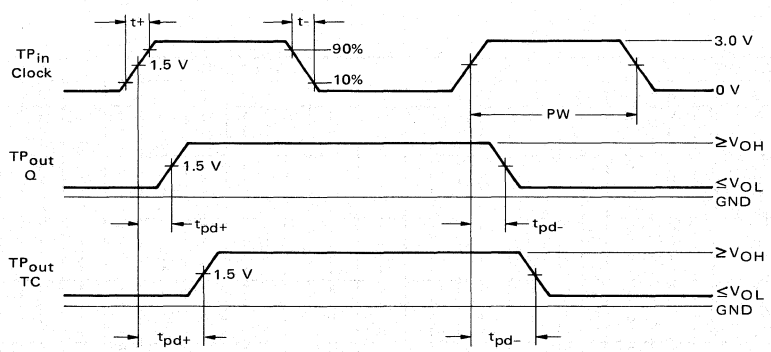
t18: Outputs go to low state, count begins (0000).

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

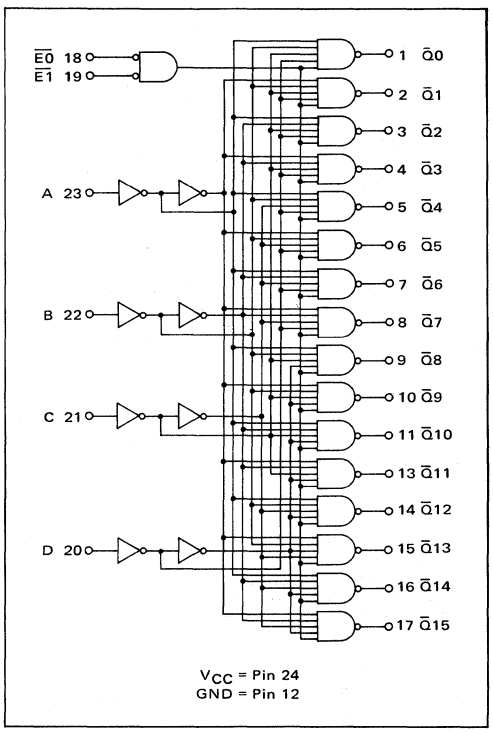


C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



MC8311P*



This device converts four BCD inputs to select one of sixteen outputs. The selected output is in the logic "0" state while all other outputs are in the logic "1" state. Two $\overline{\text{Enable}}$ inputs are provided for increased logic capability. This device is useful in memory selection control and data routing applications.

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 175 mW typ/pkg
Propagation Delay Time $\overline{\text{Enable}}$ to Output = 26 ns max

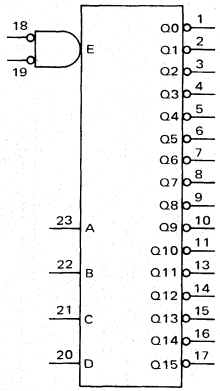
INPUT						OUTPUT															
$\overline{E0}$	$\overline{E1}$	D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

X = Don't care

*P suffix = 24-pin dual in-line plastic package (Case 649).

ELECTRICAL CHARACTERISTICS

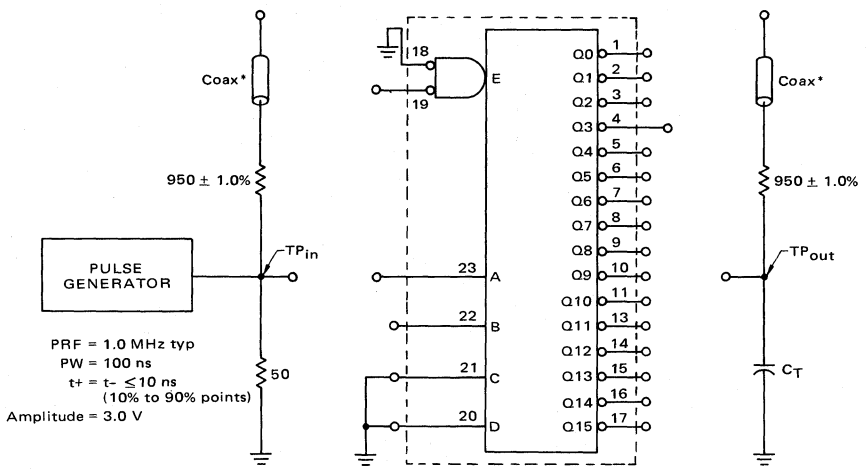
Test procedures are shown for only one input and one output. Test other inputs and outputs in a similar manner according to the truth table. Additionally, test all input-output combinations according to the truth table.



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
0°C	14.1	16	-0.6	–	0.85	1.9	0.45	4.5	–	4.75	5.25
+25°C	14.1	16	-0.6	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25
+75°C	14.1	16	-0.6	–	0.85	1.6	0.45	4.5	–	4.75	5.25

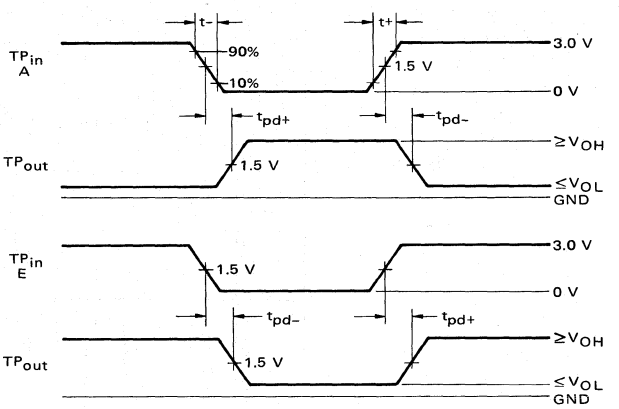
Characteristic	Symbol	Pin Under Test	MC8311 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_{F1}	18	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	18	–	–	–	24	12
		20	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	20	–	–	–	24	12
	I_{F2}	18	–	-1.41	–	-1.41	–	-1.41	mAdc	–	–	–	–	–	–	18	–	–	24	–	12
		20	–	-1.41	–	-1.41	–	-1.41	mAdc	–	–	–	–	–	–	20	–	–	24	–	12
Leakage Current	I_R	18	–	60	–	60	–	60	μAdc	–	–	–	–	–	–	–	18	–	–	24	12
		20	–	60	–	60	–	60	μAdc	–	–	–	–	–	–	–	20	–	–	24	12
Clamp Voltage	V_D	18	–	–	–	-1.5	–	–	Vdc	–	–	–	18	–	–	–	–	–	24	–	12
		20	–	–	–	-1.5	–	–	Vdc	–	–	–	20	–	–	–	–	–	24	–	12
Output																					
Output Voltage	V_{OL1}	1	–	0.45	–	0.45	–	0.45	Vdc	1	–	–	–	18,19,20,21,22,23	–	–	–	–	24	–	12
	V_{OL2}	1	–	0.45	–	0.45	–	0.45	Vdc	–	1	–	–	18,19,20,21,22,23	–	–	–	–	–	24	12
	V_{OH}	1	2.4	–	2.4	–	2.4	–	Vdc	–	–	1	–	18,20,21,22,23	19	–	–	–	24	–	12
Power Requirements (Total Device)																					
Power Supply Drain	I_{PD}	24	–	–	–	60	–	–	mAdc	–	–	–	–	–	–	–	–	24	–	–	12
Switching Parameters										Pulse In	Pulse Out			V_{IHX} = 2.4 Vdc							
Turn-On Delay – $\bar{E}$	t_{pd-}	19,4	–	–	–	26	–	–	ns	19	4	–	–	22,23	–	–	–	24	–	–	12,18,20,21
Turn-Off Delay – $\bar{E}$	t_{pd+}	19,4	–	–	–	31	–	–	ns	19	4	–	–	22,23	–	–	–	24	–	–	12,18,20,21
Turn-On Delay – A	t_{pd-}	23,4	–	–	–	35	–	–	ns	23	4	–	–	22	–	–	–	24	–	–	12,18,19,20,21
Turn-Off Delay – A	t_{pd+}	23,4	–	–	–	40	–	–	ns	23	4	–	–	22	–	–	–	24	–	–	12,18,19,20,21

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

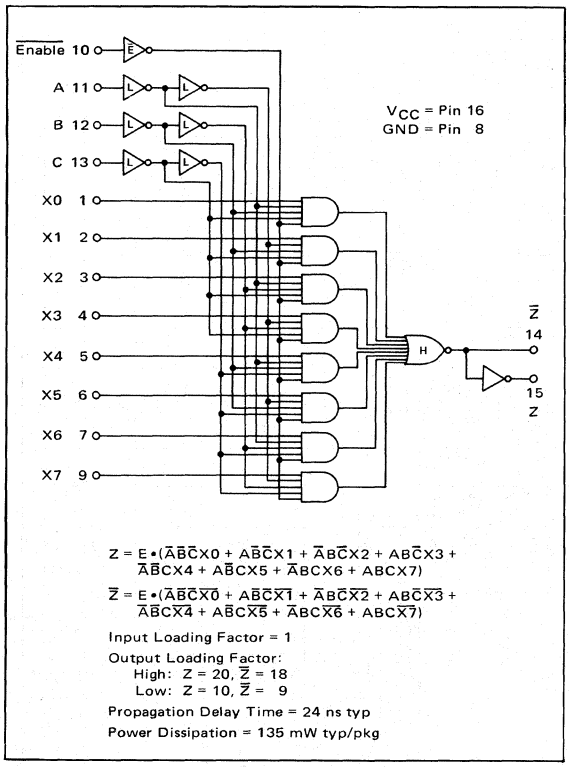


C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



MC9312L*
MC8312L,P*



$Z = E \cdot (\bar{A}\bar{B}\bar{C}X0 + A\bar{B}\bar{C}X1 + \bar{A}B\bar{C}X2 + AB\bar{C}X3 + \bar{A}\bar{B}CX4 + A\bar{B}CX5 + \bar{A}BCX6 + ABCX7)$

$\bar{Z} = E \cdot (\bar{A}\bar{B}\bar{C}\bar{X0} + A\bar{B}\bar{C}\bar{X1} + \bar{A}B\bar{C}\bar{X2} + AB\bar{C}\bar{X3} + \bar{A}\bar{B}C\bar{X4} + A\bar{B}C\bar{X5} + \bar{A}BC\bar{X6} + ABC\bar{X7})$

Input Loading Factor = 1

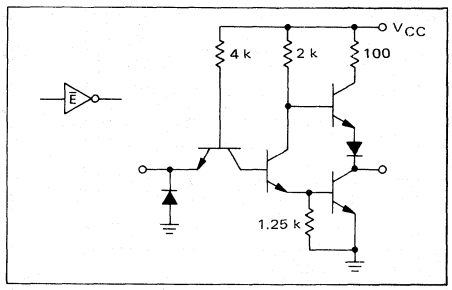
Output Loading Factor:
High: Z = 20, $\bar{Z}$ = 18
Low: Z = 10, $\bar{Z}$ = 9

Propagation Delay Time = 24 ns typ

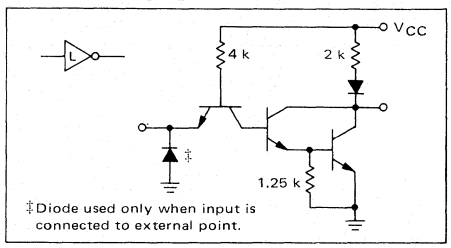
Power Dissipation = 135 mW typ/pkg

This 8-channel data selector is constructed from high-level and low-level gates interconnected as shown in the logic diagram. It is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of the select inputs, A, B, and C. Complementary outputs are provided. The $\overline{\text{Enable}}$ input is active in the low state. When the $\overline{\text{Enable}}$ input is high, the $\bar{Z}$ output is high and the Z output low, regardless of the state of the other inputs.

ENABLE-INPUT INVERTER

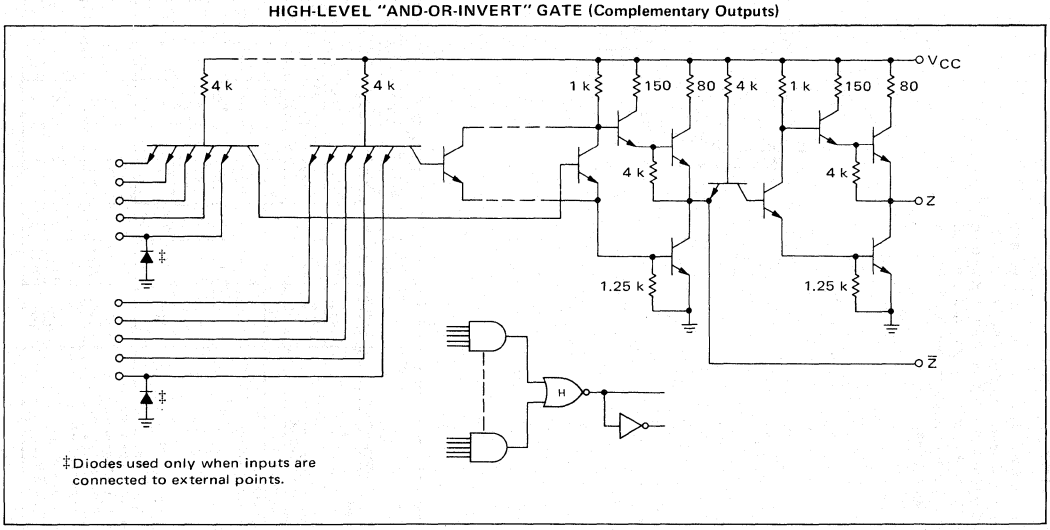


LOW-LEVEL INVERTER



‡Diode used only when input is connected to external point.

HIGH-LEVEL "AND-OR-INVERT" GATE (Complementary Outputs)

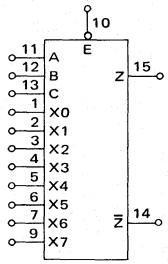


‡Diodes used only when inputs are connected to external points.

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and outputs in a similar manner according to the truth table. Additionally, test all input-output combinations according to the truth table.



TRUTH TABLE

E	C	B	A	X0	X1	X2	X3	X4	X5	X6	X7	Z̄	Z
1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	1	0
0	0	0	0	0	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	1	0
0	0	0	0	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	0	1
0	0	0	1	ϕ	0	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	1	0
0	0	0	1	ϕ	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	0	1
0	0	1	0	ϕ	ϕ	0	ϕ	ϕ	ϕ	ϕ	ϕ	1	0
0	0	1	0	ϕ	ϕ	1	ϕ	ϕ	ϕ	ϕ	ϕ	0	1
0	0	1	1	ϕ	ϕ	ϕ	0	ϕ	ϕ	ϕ	ϕ	1	0
0	0	1	1	ϕ	ϕ	ϕ	1	ϕ	ϕ	ϕ	ϕ	0	1
0	1	0	0	ϕ	ϕ	ϕ	ϕ	0	ϕ	ϕ	ϕ	1	0
0	1	0	0	ϕ	ϕ	ϕ	ϕ	1	ϕ	ϕ	ϕ	0	1
0	1	0	1	ϕ	ϕ	ϕ	ϕ	ϕ	0	ϕ	ϕ	1	0
0	1	0	1	ϕ	ϕ	ϕ	ϕ	ϕ	1	ϕ	ϕ	0	1
0	1	1	0	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	0	ϕ	1	0
0	1	1	0	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	1	ϕ	0	1
0	1	1	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	0	1	0
0	1	1	1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	1	0	1

ϕ = Input level does not affect output.

	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OL3}	I_{OL4}	I_{OH1}	I_{OH2}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC9312	-55°C	11.2	12.4	14.4	16.0	-1.2	-1.08	–	0.80	2.0	0.4	–	5.0	4.5	5.5	–
MC9312	+25°C	11.2	12.4	14.4	16.0	-1.2	-1.08	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5	2.4
MC9312	+125°C	11.2	12.4	14.4	16.0	-1.2	-1.08	–	0.80	1.4	0.4	4.5	5.0	4.5	5.5	–
MC8312	0°C	12.7	14.1	14.4	16.0	-1.2	-1.08	–	0.85	1.9	0.45	–	5.0	4.75	5.25	–
MC8312	+25°C	12.7	14.1	14.4	16.0	-1.2	-1.08	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25	2.4
MC8312	+75°C	12.7	14.1	14.4	16.0	-1.2	-1.08	–	0.85	1.6	0.45	4.5	5.0	4.75	5.25	–

Characteristic	Symbol	Pin Under Test	MC9312 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC8312 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OL4}	I_{OH1}	I_{OH2}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																														
Forward Current	I_{F1}	1	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	–	–	–	1	–	–	–	16	–	8,10,11,12,13
	I_{F2}	1	–	-1.24	–	-1.24	–	-1.24	–	-1.41	–	-1.41	–	-1.41	mAdc	–	–	–	–	–	–	–	–	–	1	–	–	–	16	–	8,10,11,12,13
Leakage Current	I_R	1	–	–	–	60	–	60	–	–	–	60	–	60	μAdc	–	–	–	–	–	–	–	–	–	–	1	–	–	16	–	8
Clamp Voltage	V_D	1	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	–	1	–	–	–	–	16	–	–	–	8
Output																														
Output Voltage	V_{OL1}	14	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	14	–	–	–	15	–	–	10,11,12,13	1	–	–	–	16	–	–	8
		15	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	–	15	–	–	–	14	–	1,10,11,12,13	–	–	–	–	16	–	–	8
	V_{OL2}	14	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	–	–	14	–	15	–	–	10,11,12,13	1	–	–	–	–	16	–	8
		15	–	0.4	–	0.4	–	0.4	–	0.45	–	0.45	–	0.45	Vdc	–	–	–	15	–	14	–	1,10,11,12,13	–	–	–	–	–	16	–	8
	V_{OH}	14	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	Vdc	–	–	–	15	–	14	–	1,10,11,12,13	–	–	–	–	16	–	–	8
		15	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	Vdc	–	–	14	–	15	–	–	10,11,12,13	1	–	–	–	16	–	–	8
Power Requirements (Total Device)																														
Power Supply Drain	I_{PDH}	16	–	40	–	40	–	40	–	43	–	43	–	43	mAdc	–	–	–	–	–	–	–	–	–	–	–	16	–	–	–	8
Switching Parameters																Pulse In		Pulse Out													
Turn-On Delay	t_{pd-}	11/15	–	–	–	36	–	–	–	–	–	36	–	–	ns	11		15		–	–	–	–	–	–	–	16	–	–	2,3,4,5,6,7,9	1,8,10,12,13
Turn-Off Delay	t_{pd+}	11/15	–	–	–	34	–	–	–	–	–	34	–	–	ns	11		15		–	–	–	–	–	–	–	16	–	–	2,3,4,5,6,7,9	1,8,10,12,13

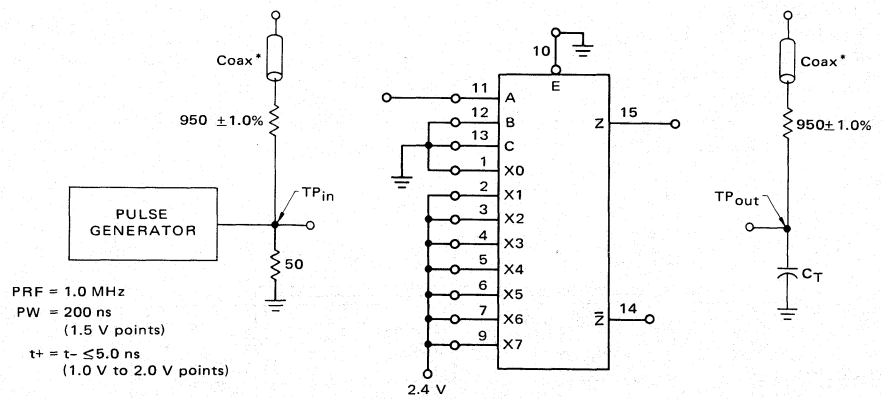
INPUT and OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC9312 INPUT LOADING FACTOR	MC9312 OUTPUT LOADING FACTOR Z	MC9312 OUTPUT LOADING FACTOR $\overline{Z}$
MC9300	1.0	10	9.0
MC500	1.06	10.6	9.5
MC2100	0.7	7.0	6.3
MC3100	0.7	7.0	6.3
MC4300	1.0	10	9.0
MC5400	1.0	7.75	7.0
MC930*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	9.4	8.4

*Due to logic "1" state drive limitations of the MDTL family.

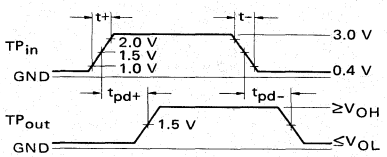
FAMILY	MC8312 INPUT LOADING FACTOR	MC8312 OUTPUT LOADING FACTOR Z	MC8312 OUTPUT LOADING FACTOR $\overline{Z}$
MC8300	1.0	10	9.0
MC400	1.0	9.0	8.1
MC2000	0.6	6.0	5.4
MC3000	0.7	7.4	6.6
MC4000	1.0	10	9.0
MC7400	1.0	8.75	7.8
MC830*	Fan-Out = 2 (6.0 k ohm pullup) Fan-Out = 8 (2.0 k ohm pullup)	10.8	9.7

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances.



14

PRESETTABLE
4-BIT BINARY COUNTER

MC9316L*
MC8316L,P*

The MC9316/8316 hexadecimal counter consists of four J-K master-slave flip-flops plus additional gating to accomplish the counter function. Parallel inputs are provided for presetting data and parallel outputs for full counting flexibility.

An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of other input states. Parallel information may be preset only while the parallel enable ($\overline{PE}$) is in the logic "0" state.

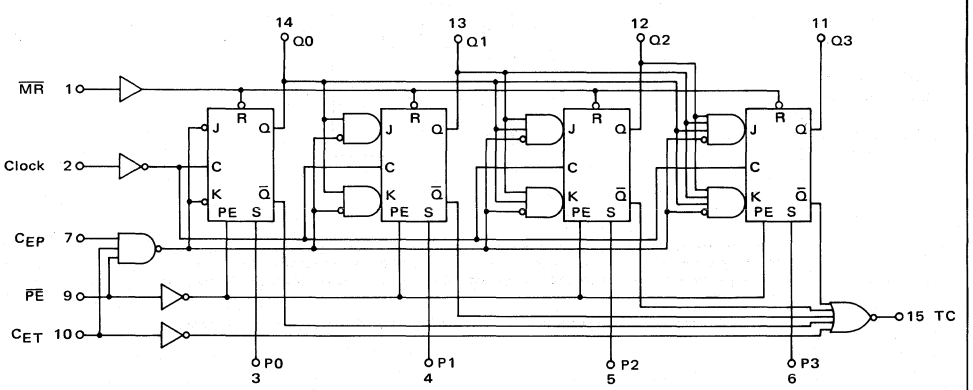
Inputs C_{EP} and C_{ET} and output TC are useful in cascading counters. TC provides an output pulse each time the counter reaches its maximum count.

COUNT SEQUENCE TRUTH TABLE

	OUTPUT			
COUNT	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Input Loading Factors:
$\overline{MR}$, C_{EP} = 1
Clock, $\overline{PE}$, C_{ET} = 2
P0, P1, P2, P3 = 2/3
Output Loading Factor = 6

Total Power Dissipation = 300 mW typ/pkg
Propagation Delay Time = 14 to 35 ns typ
Toggle Frequency = 28 MHz typ

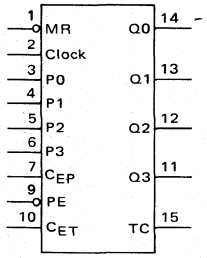


V_{CC} = Pin 16
GND = Pin 8

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

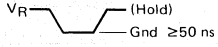
Test procedures are shown for only one input and one output. Test other inputs and outputs in a similar manner according to the truth table.



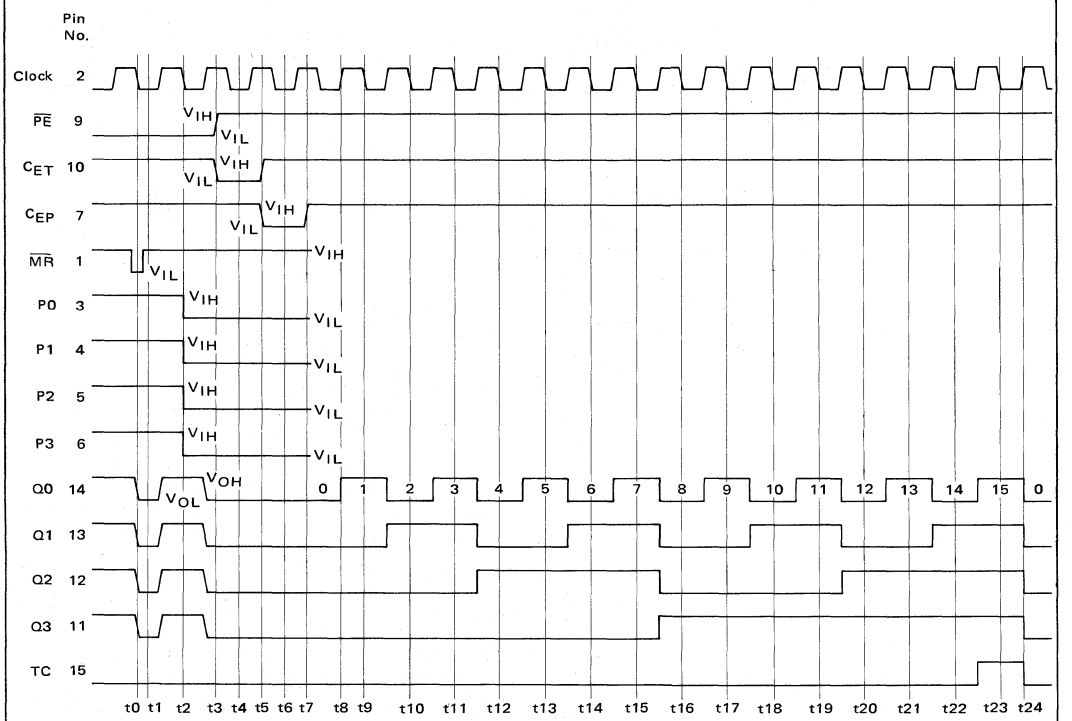
@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
MC9316 -55°C	9.6	7.44	-0.36	–	0.80	2.0	0.4	4.5	5.0	4.5	5.5
MC9316 +25°C	9.6	7.44	-0.36	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5
MC9316 +125°C	9.6	7.44	-0.36	–	0.80	1.4	0.4	4.5	5.0	4.5	5.5
MC8316 0°C	9.6	8.50	-0.36	–	0.85	1.9	0.45	4.5	5.0	4.75	5.25
MC8316 +25°C	9.6	8.50	-0.36	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25
MC8316 +75°C	9.6	8.50	-0.36	–	0.85	1.6	0.45	4.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC9316 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC8316 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																												
Forward Current	I_F	1	–	-1.6	–	-1.6	–	-1.6	mAdc	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	1	–	–	–	16	8
		2	–	-3.2	–	-3.2	–	-3.2	mAdc	–	-3.2	–	-3.2	–	-3.2	mAdc	–	–	–	–	–	–	2	–	–	–	16	8
		3	–	-1.07	–	-1.07	–	-1.07	mAdc	–	-1.07	–	-1.07	–	-1.07	mAdc	–	–	–	–	–	–	3	–	–	–	16	8
Leakage Current	I_R	1	–	60	–	60	–	60	μAdc	–	60	–	60	–	60	μAdc	–	–	–	–	–	–	–	1	–	–	16	8
		2	–	120	–	120	–	120	μAdc	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	2	–	–	16	8
		3	–	40	–	40	–	40	μAdc	–	40	–	40	–	40	μAdc	–	–	–	–	–	–	–	3	–	–	16	8
Clamp Voltage	V_D	1	–	–	–	-1.5	–	–	Vdc	–	–	–	-1.5	–	–	Vdc	–	–	–	1	–	–	–	–	16	–	–	8
Output																												
Output Voltage	V_{OL1}	11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	11	–	–	See Timing Diagram @ t1						–	16	8
	V_{OL2}	11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	11	–	See Timing Diagram @ t4						16	–	8
		11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	11	–	See Timing Diagram @ t9						16	–	8
		11	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	11	–	See Timing Diagram @ t10						16	–	8
	V_{OH}	11	2.4	–	2.4	–	2.4	–	Vdc	2.4	–	2.4	–	2.4	–	Vdc	–	–	11	See Timing Diagram @ t2						16	–	8
		11	2.4	–	2.4	–	2.4	–	Vdc	2.4	–	2.4	–	2.4	–	Vdc	–	–	11	See Timing Diagram @ t16						16	–	8
Power Requirements (Total Device) Power Supply Drain Current	I_{PD}	16	–	–	–	75	–	–	mAdc	–	–	–	75	–	–	mAdc	–	–	–	–	–	2,7 9,10	–	1*	16	–	–	8
Switching Parameters																	Pulse In		Pulse Out		V_{IHX} = 3.0 Vdc							
Turn-On Delay – Q	t_{pd-}	2,14	–	–	–	30	–	–	ns	–	–	–	30	–	–	ns	2		14		1,3,4,5,6,7,9,10				16	–	–	8
Turn-Off Delay – Q	t_{pd+}	2,14	–	–	–	35	–	–	ns	–	–	–	35	–	–	ns	2		14		1,3,4,5,6,7,9,10				16	–	–	8
Turn-On Delay – TC	t_{pd-}	2,15	–	–	–	40	–	–	ns	–	–	–	40	–	–	ns	2		15		1,3,4,5,6,7,9,10				16	–	–	8
Turn-Off Delay – TC	t_{pd+}	2,15	–	–	–	60	–	–	ns	–	–	–	60	–	–	ns	2		15		1,3,4,5,6,7,9,10				16	–	–	8

*Apply after potentials have been applied to other pins.



TIMING DIAGRAM



NOTES

1. The Clock pulse must be in the high state during the high to low transition of C_{ET} and C_{EP}, and the low to high transition of $\overline{PE}$ for correct logic operation.
2. Pin conditions reflected on timing diagram for tests at time specified:

t0: Parallel (P) inputs high, Parallel Enable ($\overline{PE}$) low, asynchronous Master Reset ($\overline{MR}$) pulsed; Q outputs make transition from high to low.

t1: Measure both V_{OL1} and V_{OL2} on Q0, Q1, Q2, Q3 and TC before Clock goes high.

t2: Clock has been pulsed, Q outputs are high; measure V_{OH}.

t3: Clock is in high state while transitions of $\overline{PE}$ and C_{ET} occur (necessary condition). Parallel entry is now inhibited, P inputs are at the low level.

t4: Count enable (C_{ET}) is at the low level (disabled), count cannot occur; check Q outputs to see that they remain at the low level.

t5: C_{ET} is set to a high level and C_{EP} is set at the low level while the Clock is high.

t6: Check Q outputs to see that count is disabled, outputs remain low.

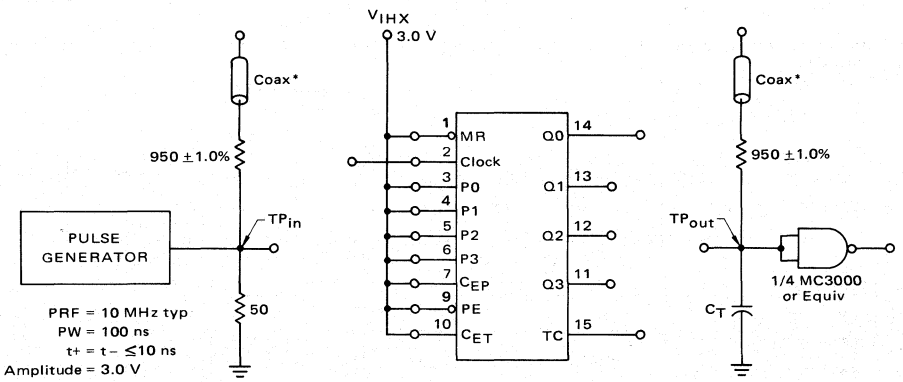
t7: C_{EP} is set high while Clock is high; count is now enabled.

t8: Clock is pulsed, count begins from 0000 to 0001.

t9 thru t23: Check Q and TC output states.

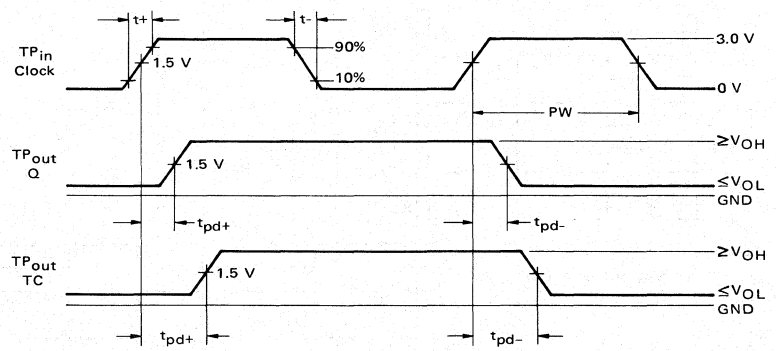
t24: Outputs go to low state, count begins (0000).

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



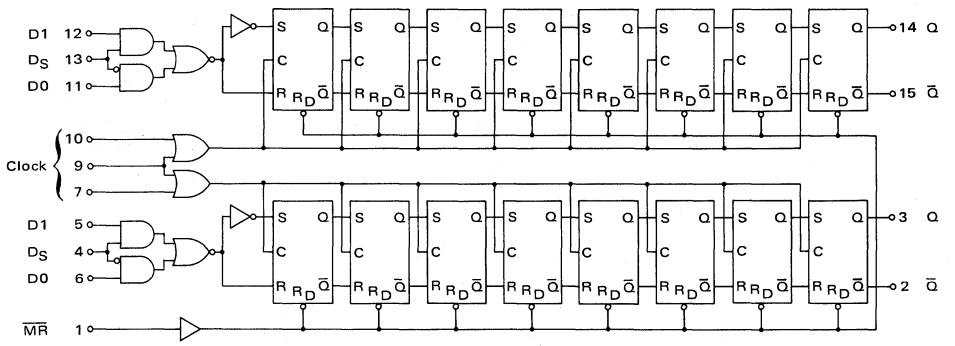
MC9328L*
MC8328L,P*

Input Loading Factors:
$\overline{MR}$, D0, D1 = 1
D_S = 2
Clock — Pins 7, 10 = 1.5
Pin 9 = 3
Output Loading Factor = 6

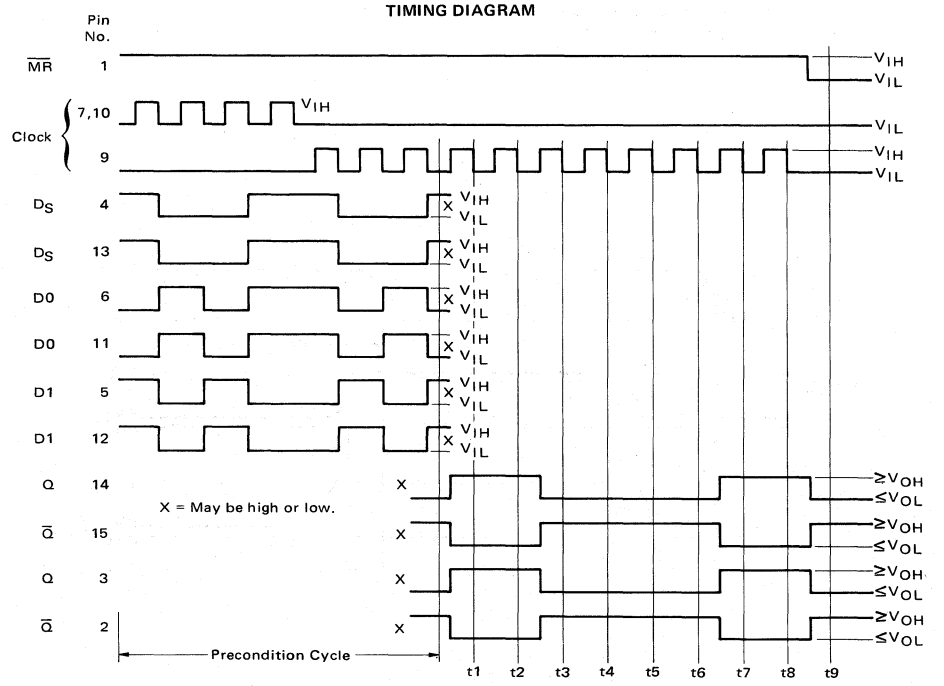
Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time = :
Clock to Output, t_{pd-} = 22 ns typ
t_{pd+} = 13 ns typ
$\overline{MR}$ to Output, t_{pd-} or t_{pd+} = 35 ns typ

The MC9328/8328 is a monolithic dual 8-bit serial shift register. Each 8-bit register is provided with a 2-input multiplexer circuit and complementary serial outputs. The two registers can be clocked together with a common line, or clocked separately with separate lines. A common Master Reset input is active in the low level and overrides all other inputs.

V_{CC} = Pin 16
GND = Pin 8



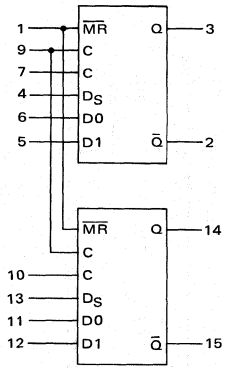
TIMING DIAGRAM



* L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output of one half of the device. To complete testing, sequence through other inputs and outputs in the same manner

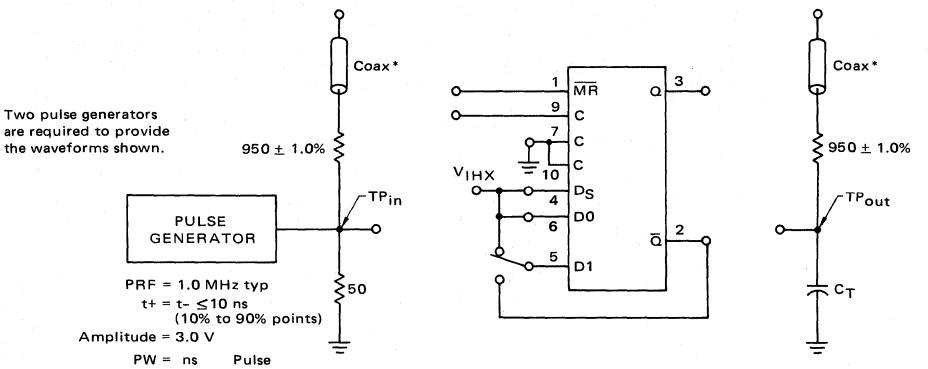


@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
MC9328	-55°C	7.44	9.6	-0.36	–	0.80	2.0	0.4	4.5	–	4.5	5.5
	+25°C	7.44	9.6	-0.36	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5
	+125°C	7.44	9.6	-0.36	–	0.80	1.4	0.4	4.5	–	4.5	5.5
MC8328	0°C	8.5	9.6	-0.36	–	0.85	1.9	0.45	4.5	–	4.75	5.25
	+25°C	8.5	9.6	-0.36	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25
	+75°C	8.5	9.6	-0.36	–	0.85	1.6	0.45	4.5	–	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC9328 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC8328 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																											
Forward Current	I_F	1	–	-1.6	–	-1.6	–	-1.6	mAdc	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	1	–	–	–	16	8
		4	–	-3.2	–	-3.2	–	-3.2	↓	–	-3.2	–	-3.2	–	-3.2	↓	–	–	–	–	–	–	4	–	–	–	↓	↓
		7	–	-2.4	–	-2.4	–	-2.4		–	-2.4	–	-2.4	–	-2.4		–	–	–	–	–	–	7	–	–	–		
		9	–	-4.8	–	-4.8	–	-4.8		–	-4.8	–	-4.8	–	-4.8		–	–	–	–	–	–	9	–	–	–		
Leakage Current	I_R	1	–	60	–	60	–	60	µAdc	–	60	–	60	–	60	µAdc	–	–	–	–	–	–	–	1	–	–	16	8
		4	–	120	–	120	–	120	↓	–	120	–	120	–	120	↓	–	–	–	–	–	–	–	4	–	–	↓	↓
		7	–	90	–	90	–	90		–	90	–	90	–	90		–	–	–	–	–	–	–	7	–	–		
		9	–	180	–	180	–	180		–	180	–	180	–	180		–	–	–	–	–	–	–	9	–	–		
Clamp Voltage	V_D	1	–	–	–	-1.5	–	–	Vdc	–	–	–	-1.5	–	–	Vdc	–	–	–	1	–	–	–	–	–	16	–	8
Output																												
Output Voltage	V_{OL1}	3	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	3	–	–	See Timing Diagram						16	–	7,8,10
	V_{OL2}	3	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	3	–	See Timing Diagram						–	16	7,8,10
	V_{OH}	3	2.4	–	2.4	–	2.4	–	Vdc	2.4	–	2.4	–	2.4	–	Vdc	–	–	3	See Timing Diagram						16	–	7,8,10
Power Requirements (Total Device) Power Supply Drain	I_{PDH}	16	–	–	–	73	–	–	mAdc	–	–	–	73	–	–	mAdc	–	–	–	–	–	–	–	–	16	–	–	8
Switching Parameters																	Pulse In*		Pulse Out		V_{IHX} = 2.4 Vdc					#	##	
Turn-On Delay C to Q	t_{pd-}	3	–	–	–	44	–	–	ns	–	–	–	44	–	–	ns	9 (W)		3		1, 4, 6, 11, 13				16	2, 5	12, 15	7,8,10
Turn-Off Delay C to Q	t_{pd+}	3	–	–	–	26	–	–	ns	–	–	–	26	–	–	ns	9 (W)		3		1, 4, 6, 11, 13				16	2, 5	12, 15	7,8,10
Turn-On Delay $\overline{MR}$ to Q	t_{pd-}	3	–	–	–	70	–	–	ns	–	–	–	70	–	–	ns	1 (Y), 9 (X)		3		4, 5, 6, 11, 12, 13				16	–	–	7,8,10
Turn-On Delay $\overline{MR}$ to Q	t_{pd-}	3	–	–	–	70	–	–	ns	–	–	–	70	–	–	ns	1 (Z), 9 (X)		3		4, 5, 6, 11, 12, 13				16	–	–	7,8,10

*Letters in parenthesis refer to waveform.
#These pins tied together
##These pins tied together

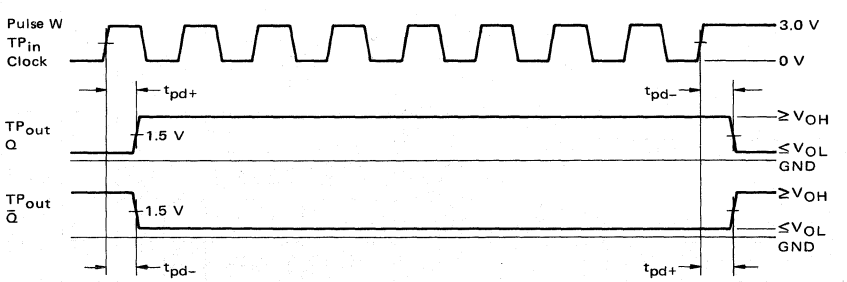
SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



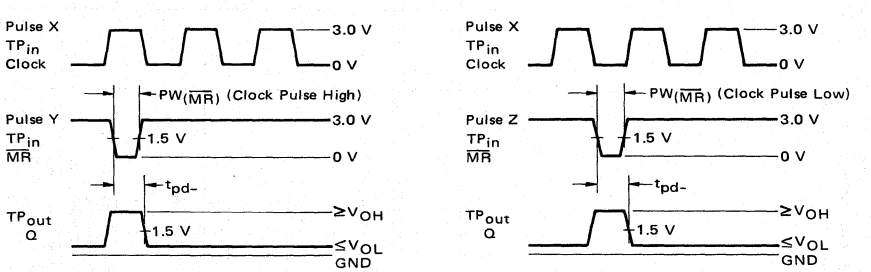
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

CLOCK PROPAGATION DELAY



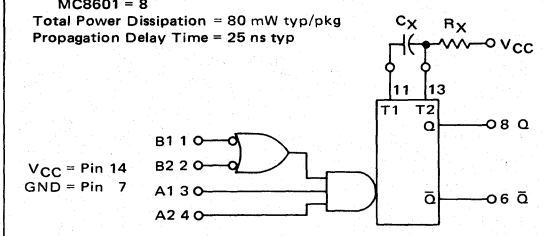
MASTER RESET PROPAGATION DELAY



RETRIGGERABLE
MONOSTABLE
MULTIVIBRATOR

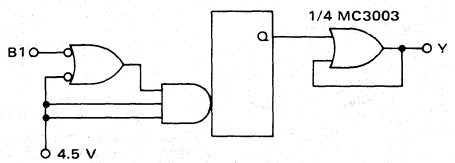
MC9601F, L*
MC8601F, L, P*

Input Loading Factor = 1
Output Loading Factor:
MC9601 = 6
MC8601 = 8
Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 25 ns typ



The MC9601/8601 monostable multivibrator may be triggered from either edge of an input pulse and will produce accurate output pulse over a wide range of widths. The duration and accuracy of the complementary output pulses are determined by the external timing components, R_X and C_X. Each time the input conditions for triggering are met the external timing capacitor, C_X, is discharged, starting a new output pulse. The output goes to the high state while C_X is being discharged and remains there until the capacitor recharges through R_X, to a threshold determined by an internal comparator. Input pulses applied during the active state again discharge the capacitor, thus adding another full timing cycle to the output pulse width. This retriggering feature can be inhibited if not required.

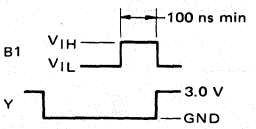
FUNCTIONAL TEST



SEQUENCE

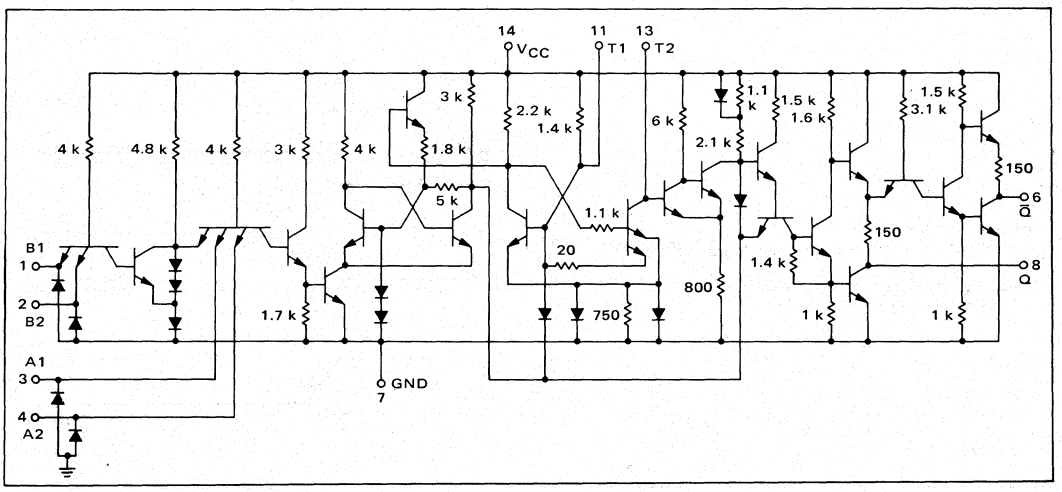
1. Apply V_{IL} to B1.
2. Momentarily ground Y.
3. Apply V_{IH} to B1.
4. Apply V_{IL} to B1.
5. Check Y for logical "1" level.

TIMING DIAGRAM



Device	Temperature	V_{IL}	V_{IH}
MC9601	-55	0.85	2.0
	+25	0.9	1.7
	+125	0.85	1.4
MC8601	0	0.85	1.9
	+25	0.85	1.8
	+75	0.85	1.6

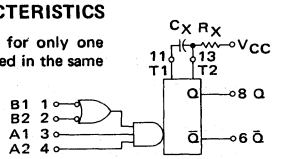
CIRCUIT SCHEMATIC



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input. Other inputs are tested in the same manner.

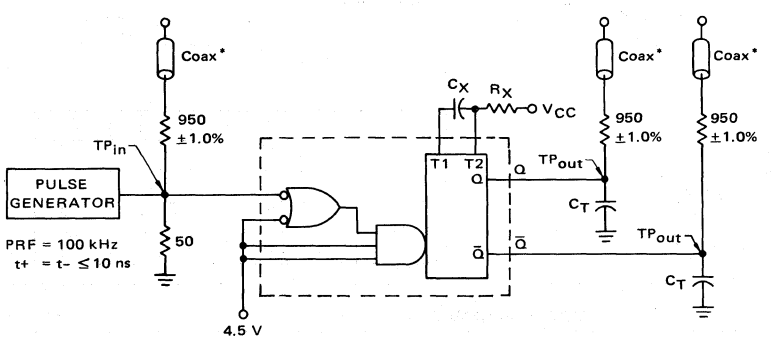


	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES (1) mA I_{OL}	I_{OH}	I_D	Volts V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
MC9601	−55°C	10.0	-0.72	-	0.4	4.5	-	4.5	5.5
	+25°C	10.0	-0.72	-10	0.4	4.5	5.0	4.5	5.5
	+125°C	10.0	-0.72	-	0.4	4.5	-	4.5	5.5
MC8601	0°C	12.8	-0.96	-	0.45	4.5	-	4.75	5.25
	+25°C	12.8	-0.96	-10	0.45	4.5	5.0	4.75	5.25
	+75°C	12.8	-0.96	-	0.45	4.5	-	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC9601 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC8601 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_D	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																									
Forward Current	I_F	1	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	1	-	-	-	14	7
Leakage Current	I_R	1	-	-	-	60	-	60	μAdc	-	-	-	60	-	60	μAdc	-	-	-	-	1	-	-	14	7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	14	-	7
Output																									
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	Vdc	-	0.45	-	0.45	-	0.45	Vdc	6	-	-	-	-	-	14	-	7,11
		8	-	0.4	-	0.4	-	0.4	Vdc	-	0.45	-	0.45	-	0.45	Vdc	8	-	-	-	-	-	14	-	7
	V_{OH}	6	2.4	-	2.4	-	2.4	-	Vdc	2.4	-	2.4	-	2.4	-	Vdc	-	6	-	-	-	-	14	-	7
		8	2.4	-	2.4	-	2.4	-	Vdc	2.4	-	2.4	-	2.4	-	Vdc	-	8	-	-	-	-	14	-	7,11
Short-Circuit Current	I_{SC}	6	-	-	-10	-40	-	-	mAdc	-	-	-10	-40	-	-	mAdc	-	-	-	-	-	14	-	-	6,7
		8	-	-	-10	-40	-	-	mAdc	-	-	-10	-40	-	-	mAdc	-	-	-	-	-	14	-	-	7,8,11
Power Requirements																									
Power Supply Drain	I_{PD}	14	-	25	-	25	-	25	mAdc	-	25	-	25	-	25	mAdc	-	-	-	-	-	-	-	14	7

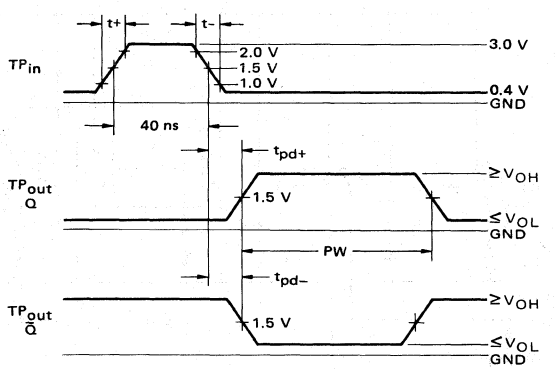
(1) A 10-kilohm resistor (R_X) is placed between Pin 13 and V_{CC} for all tests unless otherwise noted.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.



When R_X = 5.0 kΩ, C_X = 0:
PW = 65 ns max, t_{pd+} = 40 ns max, t_{pd-} = 40 ns max

When R_X = 10 kΩ ± 1.0%, C_X = 1000 pF:
PW = 3.08 μs min, 3.76 μs max

TYPICAL CHARACTERISTICS

FIGURE 1 – INPUT LOAD CURRENT versus INPUT VOLTAGE

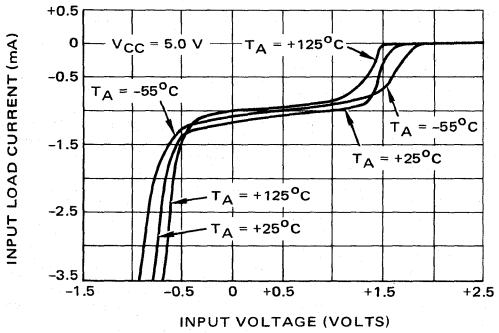


FIGURE 2 – INPUT LEAKAGE CURRENT versus INPUT VOLTAGE

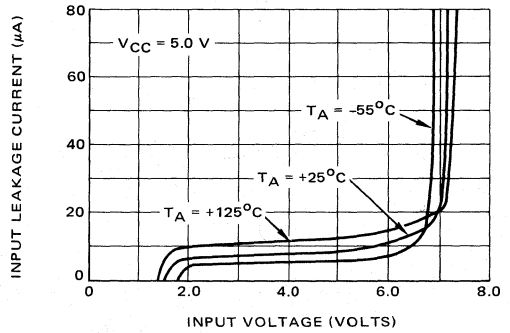


FIGURE 3 – OUTPUT CURRENT versus OUTPUT VOLTAGE (LOW STATE)

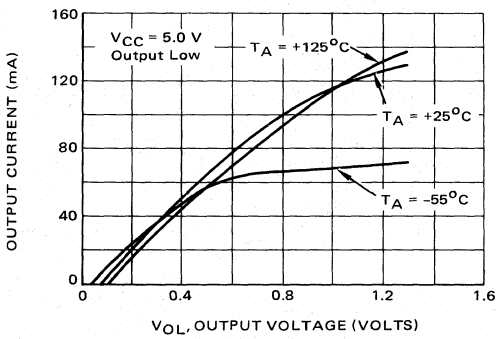


FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE (HIGH STATE)

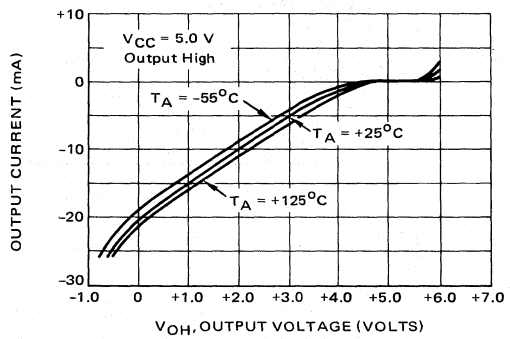


FIGURE 5 – POWER DISSIPATION versus AMBIENT TEMPERATURE and SUPPLY VOLTAGE

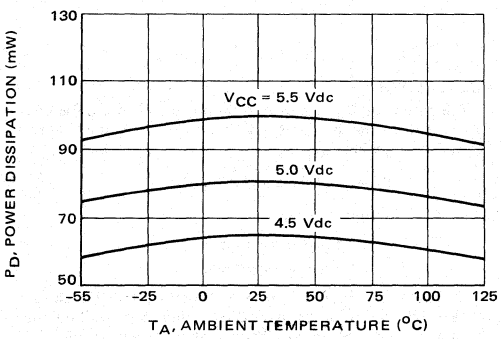
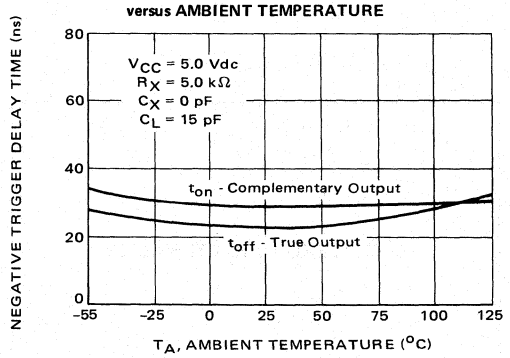


FIGURE 6 – NEGATIVE TRIGGER DELAY TIME versus AMBIENT TEMPERATURE



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TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – NORMALIZED OUTPUT PULSE WIDTH versus AMBIENT TEMPERATURE

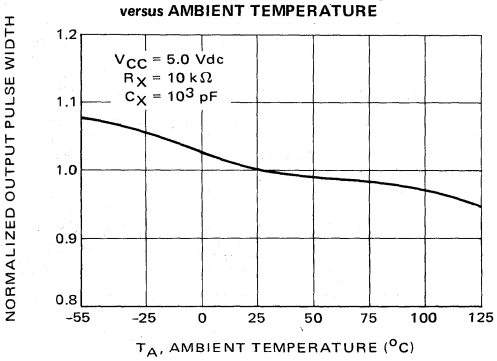


FIGURE 8 – NORMALIZED OUTPUT PULSE WIDTH versus SUPPLY VOLTAGE

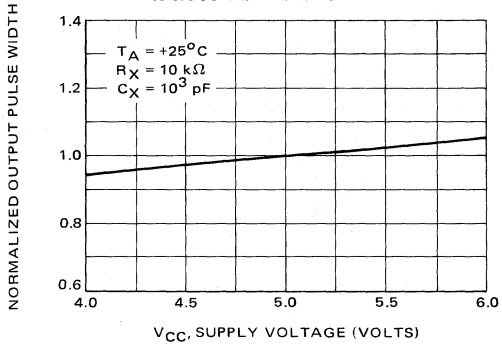


FIGURE 9 – NORMALIZED OUTPUT PULSE WIDTH versus OPERATING DUTY CYCLE

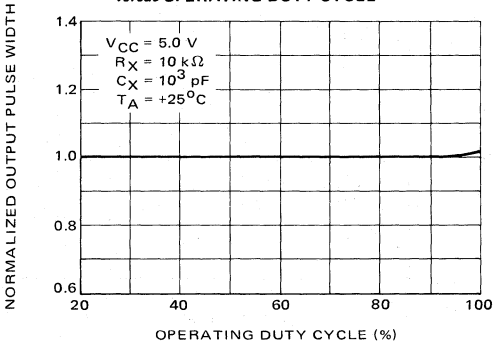
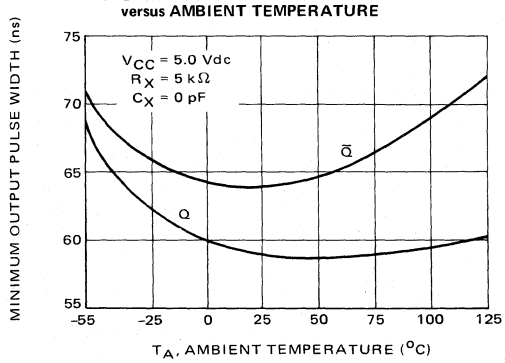


FIGURE 10 – OUTPUT PULSE WIDTH versus AMBIENT TEMPERATURE



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OPERATING CHARACTERISTICS

PULSE WIDTH

For values of C_X less than 1000 pF, the output pulse width, PW, is defined by the curves of Figure 11. For larger values of C_X use the equation:

$$PW = 0.32\ R_X C_X\ [1 + (0.7/R_X)]$$

where PW is in nanoseconds,

R_X is in kilohms,

C_X is in picofarads.

Values of R_X may vary from 5.0 kilohms to 50 kilohms for 0° to +75°C operation of the MC8601, and from 5.0 kilohms to 25 kilohms for -55° to +125°C operation of the MC9601. The range of capacitance values is unlimited, hence maximum pulse width is limited only by the values of available capacitors.

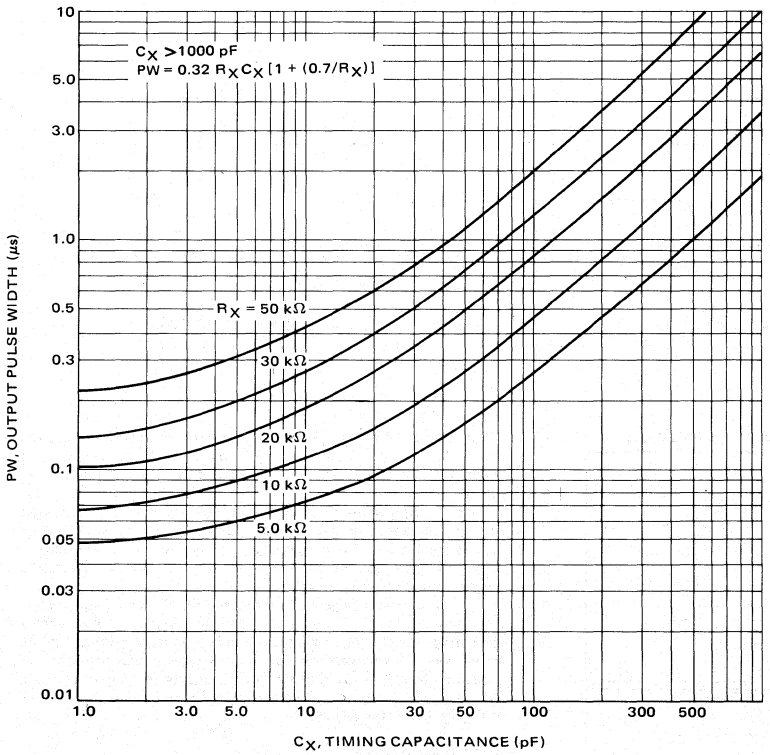


FIGURE 11 – OUTPUT PULSE WIDTH versus TIMING RESISTANCE AND CAPACITANCE

PULSE INITIATION

Output pulses are initiated by any combination of inputs satisfying the logic expression A1 • A2 • (B1 + B2); A1 and A2 must be high and either B1 or B2 must be low. Output pulses are generated by transitions from low to high on A1 or A2, and by transitions from high to low on B1 or B2. Leading edge triggering may be accomplished by either of the methods shown in Figure 12.

Similarly, trailing edge triggering may be accomplished by either of the methods shown in Figure 13.

FIGURE 12 – LEADING EDGE TRIGGERING

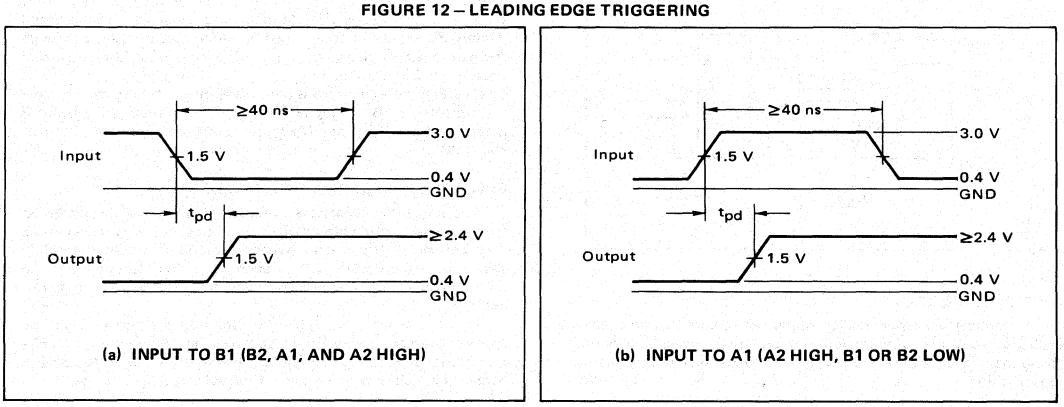
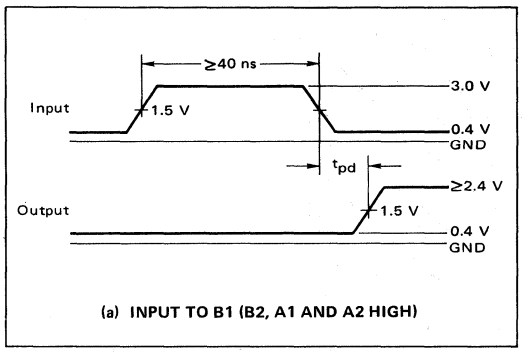
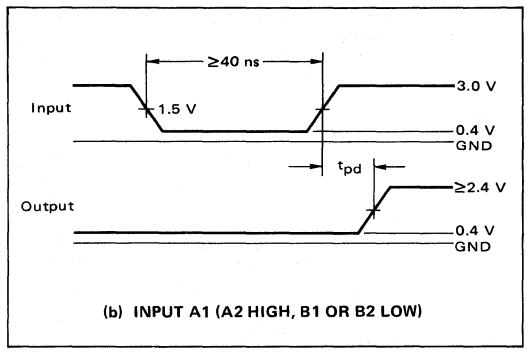


FIGURE 13 – TRAILING EDGE TRIGGERING

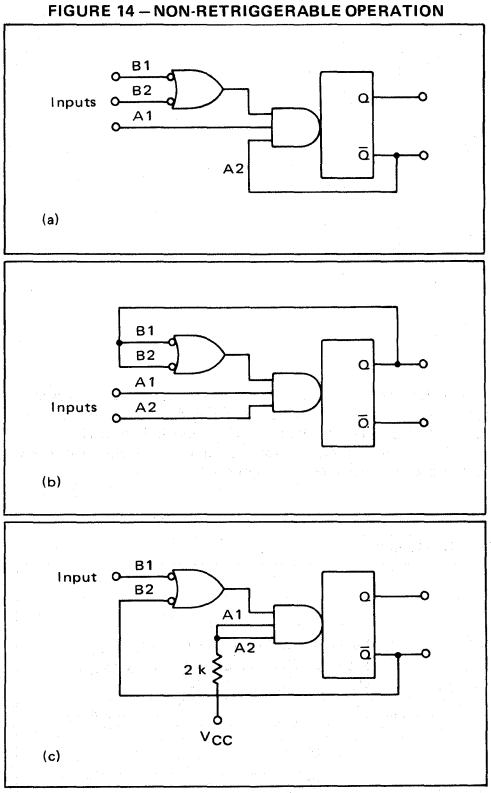


(a) INPUT TO B1 (B2, A1 AND A2 HIGH)



(b) INPUT A1 (A2 HIGH, B1 OR B2 LOW)

FIGURE 14 – NON-RETRIGGERABLE OPERATION



RETRIGGER INHIBIT

For applications where retriggering is not required, appropriate feedback from the outputs will inhibit trigger signals arriving during the active timing cycle. Figure 14 illustrates three methods for doing this.

In Figure 14(a), A2 is held low by the $\overline{Q}$ output during the active state. Since both A inputs must be high for triggering to occur, this configuration inhibits retriggering at all of the remaining inputs.

The configuration of Figure 14(b) will be triggered active on the trailing edge of a negative going pulse applied to either A1 or A2. B2 and B1 are then held high by the Q output. Since either B1 or B2 must be low for triggering to occur, further triggering during a timing cycle is inhibited.

The feedback arrangement of Figure 14(c) holds B2 low during the active timing cycle. Since this keeps the output of the inverted OR gating circuitry high, subsequent input signals to B1 during the active state do not retrigger the monostable. Noise immunity is improved by returning unused "high" inputs to V_{CC} through a 2.0 kilohm resistor instead of leaving them open (see A1 and A2 of Figure 14(c), for example.)

ASTABLE OPERATION

Astable applications requiring adjustable duty cycles may be accomplished by the conventional method of cascading two one-shots as shown in Figure 15. In applications where narrow output pulses are satisfactory, a single monostable may be used. One method for doing this is illustrated in Figure 16, monostable A. The clock generation for a simple pulse generator is accomplished by connecting the $\overline{Q}$ output of the "A" monostable back to an AND input. The period of oscillation, or pulse repetition frequency, PRF, is determined by the external timing components, R_{XA} and C_{XA}. At the end of each timing cycle, the $\overline{Q}_A$ output generates a low-to-high transition at the AND input and thus triggers another cycle. The nominal output pulse width is approximately 30 ns, and is determined by the propagation time through the gating and discharge circuitry. The maximum PRF is approximately 15 MHz, obtained with C_{XA} = 0 pF and R_{XA} = 5.0 kΩ. The variable delay feature is controlled by the timing components of monostable "B", C_{XB} and R_{XB}. The output pulse width is determined by C_{XC} and R_{XC}, the timing components of monostable "C".

ELECTROLYTIC CAPACITOR PROTECTION

If electrolytic capacitors are used they should be protected from reverse voltage; either of the methods indicated in Figure 16 may be used. Any silicon switching diode, such as the 1N4001 shown for monostable "B", is adequate. The transistor method of monostable "C" requires a silicon transistor with gain at low currents.

This figure also illustrates the preferred method of using remotely located variable timing components. Noise pickup will be minimized by locating R_X and C_X physically close to the device. Stray capacitance at pins 11 and 13 should be 50 pF or less.

FIGURE 15 – ASTABLE OPERATION – ADJUSTABLE DUTY CYCLE

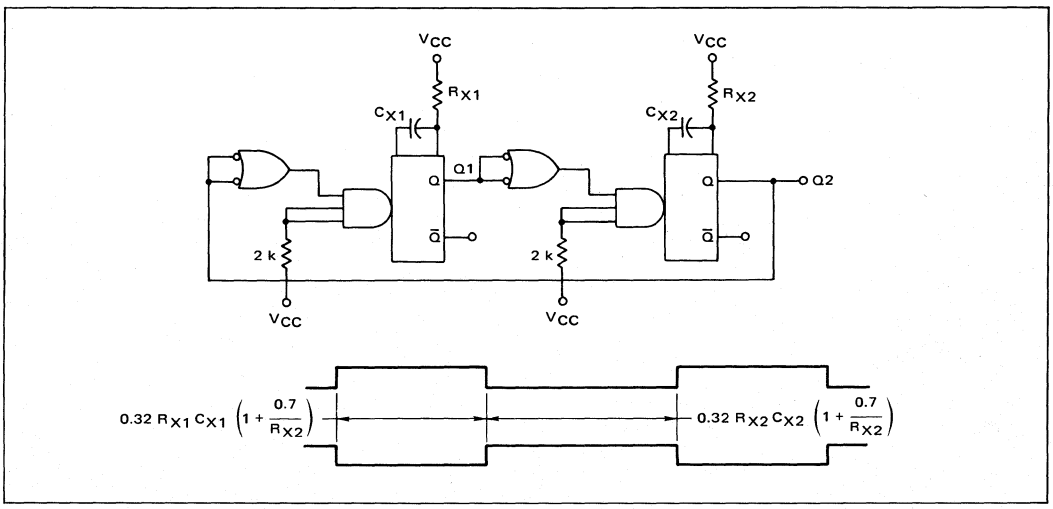
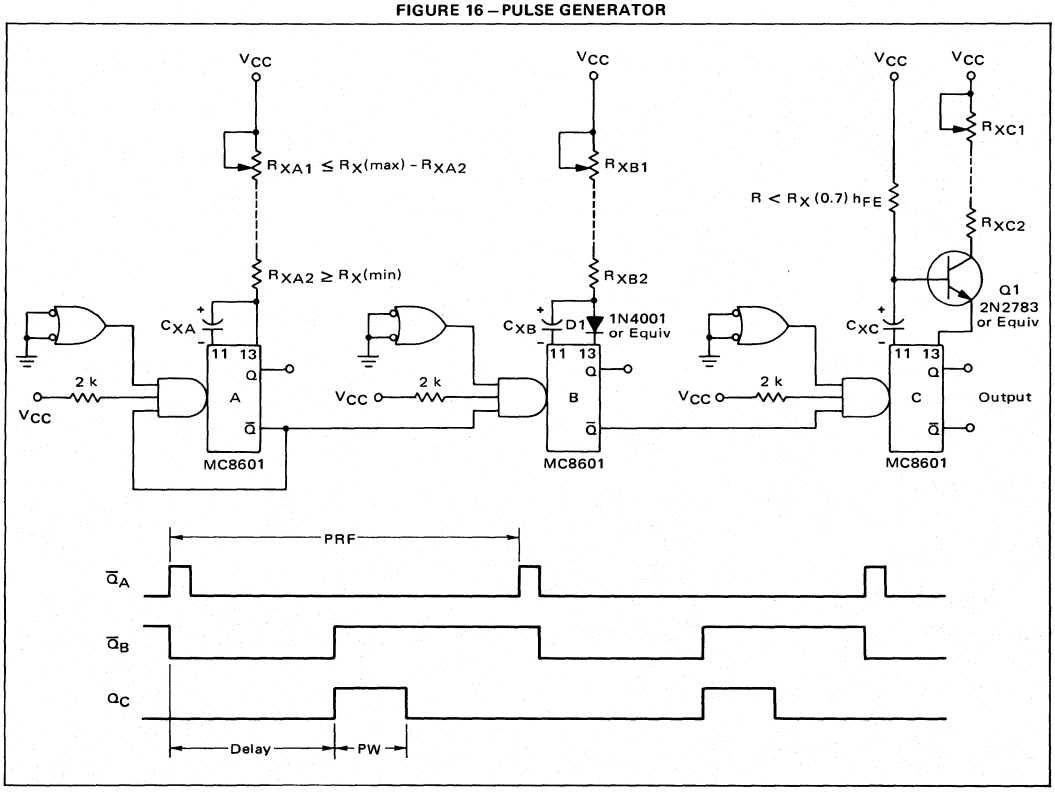


FIGURE 16 – PULSE GENERATOR



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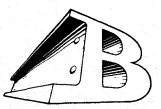
MTTL



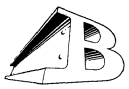
INTEGRATED CIRCUITS

MCBC5400/MCB5400F SERIES

MTTL

MCBC5400/MCB5400F SERIES

BEAM LEAD
INTEGRATED CIRCUITS



INDEX

DEVICE SPECIFICATIONS

MCBC5400	MCB5400F	Quad 2-Input NAND Gate
MCBC5401	MCB5401F	Quad 2-Input NAND Gate (Open Collector Output)
MCBC5402	MCB5402F	Quad 2-Input NOR Gate
MCBC5430	MCB5430F	8-Input NAND Gate
MCBC5440	MCB5440F	Dual 4-Input NAND Buffer
MCBC5453	MCB5453F	Expandable 4-Wide 2-Input AND-OR-INVERT Gate
MCBC5454	MCB5454F	4-Wide 2-Input AND-OR-INVERT Gate
MCBC5460	MCB5460F	Dual 4-Input Expander for AND-OR-INVERT Gate
MCBC5472	MCB5472F	J-K Flip-Flop

MTTL

GENERAL INFORMATION

MCBC5400/MCB5400F Series
BEAM LEAD INTEGRATED CIRCUITS

INTRODUCTION

The MTTL MCBC5400/MCB5400F series of transistor-transistor logic is a medium-speed, high noise immunity family of saturating integrated logic circuits designed for digital logic applications requiring clock frequencies to 30 MHz and switching speeds in the 12-15 ns range under moderate capacitive loading.

The beam lead sealed-junction technology used in this MTTL family makes the devices useful in military, aerospace, and commercial applications that require a high degree of reliability under environmental conditions of severe temperature extremes, mechanical shock, and high humidity. The beam lead products employ a silicon nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metalized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

The circuits in the MCBC5400/MCB5400F series are identified by a multiple emitter input transistor and an active pullup in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical applications such as driving long interconnect wiring. The active pullup output configuration provides low impedance in the high output state. The resulting low impedances in both states provide excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

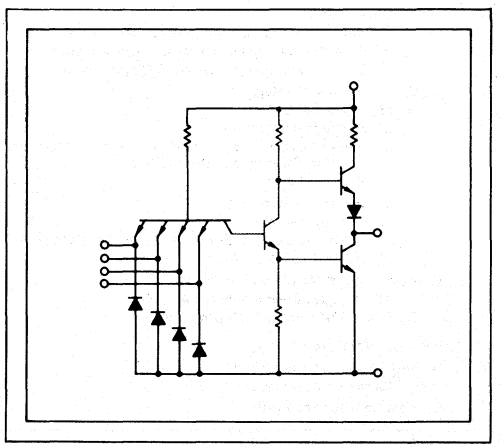
These beam lead MTTL units have the same electrical characteristics as the conventional flat-pack units and may be used interchangeably with them. This eliminates the need for electrically redesigning equipment for improved reliability after the successful performance of prototype or pre-production units with conventional devices.

BEAM LEAD TECHNOLOGY

Junction Sealing

In conventional integrated circuits, the P-N junctions are protected by a layer of silicon dioxide. This oxide, while acting as an simulator and providing a degree of protection, is permeable to mobile ions. Ions impinging on the surface of the finished circuit can cause high leakage current and reduction of current gain. Silicon nitride passivation applied over the oxide prevents contaminants that can result in such degradation from reaching the oxide.

FIGURE 1 – TYPICAL MTTL CIRCUIT
MCBC5400/MCB5400F Series



Metalization

The metalization on the Motorola beam lead integrated circuits of platinum silicide ohmic contacts topped by layers of titanium and platinum. These in turn are followed by two layers of gold. The first gold layer provides the chip intraconnection and the second, thicker layer forms the cantilevered beams that connect the chip to the outside world (see Figure 2). This metalization method has the ability to withstand conditions of high humidity over extended periods of time without degradation or the formation of undesirable inter-metallics. It is also capable of being bonded to a gold-metalized substrate and provides a highly relaible gold-to-gold bond, which is easily made and readily inspectable. Bonds have also been made to other substrate metal materials without difficulty.

During the bonding process, beam lead devices lift off the substrate surface, which, with the ductility of the gold metal beams and the high quality bond, allows the device to withstand wide variations in temperature without failure due to fatigue.

Separation Etch

Conventional integrated circuits are separated with a "scribe and break" technique which not only results in a yield loss due to cracking of the die, but can also result in minute cracks, which do not immediately reveal themselves and can cause device failure at a later date. The beam lead sealed-junction devices are separated by chemically etching through the silicon from the back side, thereby avoiding mechanical stresses and/or other latent defects.

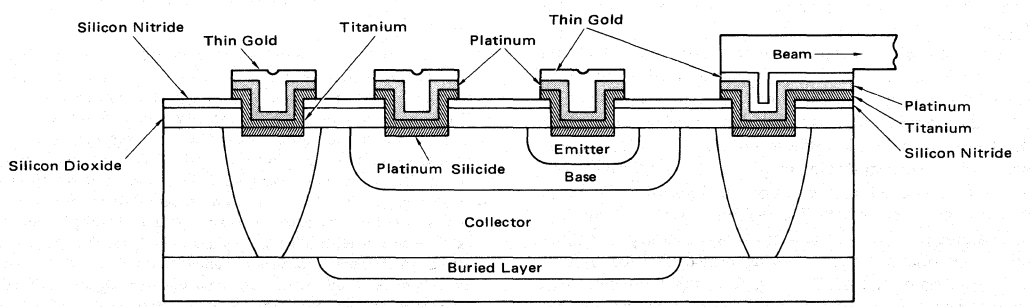
TABLE 1

Beam Lead Reliability Assurance Steps

I. Chips
- A. Tests performed after wafer separation etch
  1. Post separation etch visual inspection (backside)
  2. Wafer electrical probe (100% dc test per data sheet at 25°C.
- B. Tests performed on a bonded sample after die transfer and pick
  1. Beam integrity
     a) Bond qualification samples to test header
     b) Push die off header from metallization side
     c) Each beam must withstand 2.00 gm. min.
  2. Junction seal integrity
     a) Electrical test
     b) Apply NaCl over die
     c) Reverse bias input junctions at T_A = 300°C for eight hours in forming gas atmosphere
     d) Electrical test
  3. Electrical qualification
     a) Package sample
     b) DC parameters at all temperatures per data sheet
     c) AC test per data sheet
- C. Inspection after die pick and sort
  1. 100% high power visual inspection
  2. R and QA sample high power inspection

II. Packaged Devices
- A. Inspection after die bond
  1. Sample visual inspection
- B. Testing after encapsulation
  1. Lot stress screening
     a) Temperature cycling: -65°C to 150°C min; 10 cycles
     b) Water immersion: boiling water (≈100°C; 1 hour)
     c) Electrical measurements: dc leakage parameters
     d) Stabilization bake: T_A = 175°C min; 24 hours min
     e) High temperature reverse bias (cost option)
- C. Testing after package cleaning and marking
  1. Electrical tests
     a) Final dc test per data sheet at 25°C (100%)
     b) Final ac test per data sheet at 25°C (sample)
  2. R and QA final outgoing inspection
     a) Burn in screen (cost option)
     b) Group A – visual/mechanical inspection per MIL-STD-883, method 2009. Group A tests are performed on every lot on a sample basis.
        D.C. electrical measurements per data sheet (sample)
        A.C. electrical measurements (sample)
     c) Group B environmental testing per MIL-STD-883 Class A as applicable. These tests are performed periodically during the manufacturing period on a production lot of a representative circuit type. The circuit type selected each period is changed routinely and is representative of all structurally similar devices produced on the same line by the same processes during that period.
     d) Group C – life testing per MIL-STD-883 Class A as applicable. These tests are performed periodically on at least one lot of every circuit family produced during that period.

FIGURE 2 – BEAM LEAD SEALED JUNCTION TRANSISTOR



Reliability Processing

Conventional integrated circuits have established an outstanding reputation for reliability. Beam lead integrated circuits provide even higher reliability by eliminating the major failure modes of conventional circuits. Most failures in conventional integrated circuits are due to contaminants reaching the active chip or to failure in the bonds between the package and the chip. Beam lead technology solves both of these problems. The silicon nitride hermetically seals the chip so that even a leaking package causes no failure. The all-gold beam lead interconnection system eliminates the sources of conventional bond failure. These processes are completely documented by in-process specifications and are carefully monitored for adherance to process requirements and inspection

FIGURE 3 – 14-Lead Chip

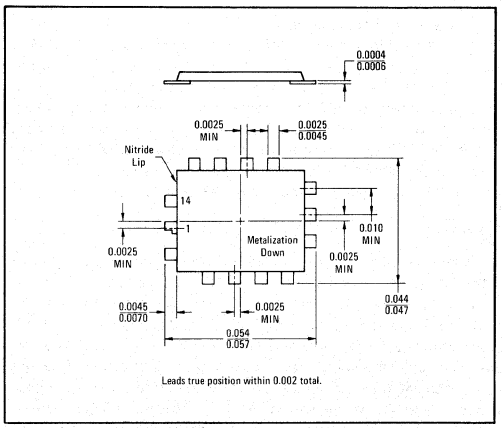


FIGURE 4 – 16-Lead Chip

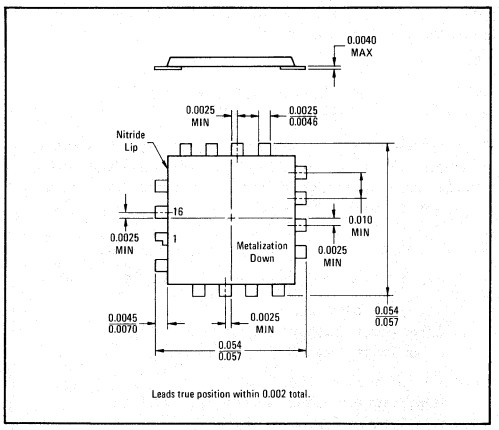
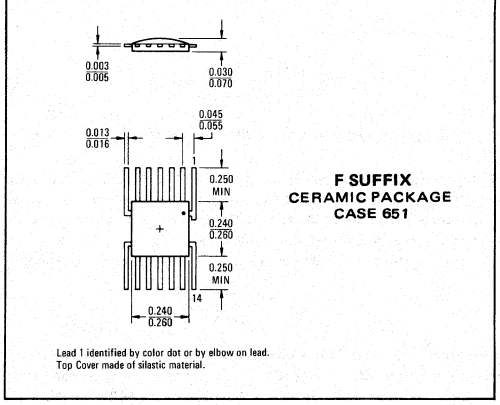


FIGURE 5 – Die Size

Device Number	Function	Die Size	No. Beams	No. Pins.	Ceramic Size
5400	Quad 2-Input NAND Gate	35 x 45	14	14	¼ x ¼
5401	Quad 2-Input NAND Gate Open Collector	35 x 45	14	14	¼ x ¼
5402	Quad 2-Input NOR Gate	45 x 45	16	14	¼ x ¼
5410	Triple 3-Input NAND Gate	35 x 45	14	14	¼ x ¼
5440	Dual 4-Input NAND Buffer	35 x 45	14	14	¼ x ¼
5453	Expandable AND/OR Inverter	35 x 45	14	14	¼ x ¼
5454	4 Wide 2-Input AND/OR Inverter	35 x 45	14	14	¼ x ¼
5460	Dual 4-Input Expander	35 x 45	14	14	¼ x ¼
5472	J-K Flip Flop	45 x 45	16	16	¼ x ¼
5473	Dual J-K Flip Flop	–	–	14	¼ x ¼

FIGURE 6



standards by the Motorola Reliability and Quality Assurance Department. In addition, the tests itemized in Table 1 are conducted on all lots from which die are taken for sale either as dice or packaged circuits.

Mechanical Properties

The beam leads, which are cantilevered from each die, are tested for beam-strength, hardness, ductility and adhesion to the chip by suitable tests to demonstrate that the die are readily bondable and will be reliable under extreme temperature and mechanical stress conditions.

Packaging and Handling

The MCBC5400/MCB5400F series of beam lead sealed-junction digital integrated circuits is available in the chip form and in a ¼" x ¼" ceramic flat package. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. This is most easily done by using a vacuum pick-up for this purpose.

Standard beam patterns are used depending on the die size required. Figures 3, 4, and 5 show these configurations and list the devices that are made from each.

TYPICAL CHARACTERISTICS

The following summary presents the typical operating characteristics of the MTTL MCBC5400/MCB5400F series. Unless otherwise indicated, the parameters are defined for V_{CC} = +5.0 volts and T_A = +25°C.

Supply Voltage Operating Range = 4.5 to 5.5 volts

Operating Temperature Range = -55 to +125°C

Output Drive Capability
- Other Gates (Output Loading Factor) = 10
- Capacitance = 600 pF

Output Impedance
- High State = 70 ohms (unsaturated) nominal
- Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits
- +5.5 volts maximum
- -0.5 volt minimum

Switching Threshold = 1.5 volts nominal

Input Impedance
- High State = 400 k ohms nominal
- Low State = 4.0 k ohms nominal

Worst-Case DC Noise Margin
- High State — 0.400 volt minimum
- Low State — 0.400 volt minimum

Power Dissipation (1)
- Basic Gate = 10 mW typ/gate
- Basic Flip-Flop = 40 mW typ/pkg

Switching Speeds (2)
- Average Propagation Delay = 13 ns per gate typical
  30 ns per flip-flop typical
- Rise Time = 2.5 ns typical
- Fall Time = 1.5 ns typical

Maximum Flip-Flop Clock Frequency = 20 MHz typical

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL gate is in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL circuits. A comparatively large, low-inductance type capacitor (in the 1.0 μF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 μF capacitors for every eight packages throughout a breadboard is adequate to suppress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The standard supply voltage of the MTTL logic circuits is +5.0 Vdc. The typical average dc power dissipation is given for each MTTL circuit.(1) It should be noted that the totem pole output common to all high level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.30 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL circuits.

Unused Inputs and Unused Gates

The unused inputs of any MTTL logic circuit should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting

---

(1)
$$P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where I_{PDL} and I_{PDH} are the typical dc current drains at V_{CC} = ±5.0 V.

(2) The switching characteristics of the MTTL family are defined with respect to the associated transistions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

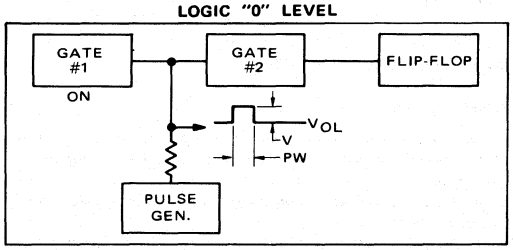
$$t_{pd} = \frac{t_{on} + t_{off}}{2} \text{ ns.}$$

Rise time is defined as the positive going transition of the output from the 10% to the 90% V level. Fall time is defined as the negative transition of the output from the 90% to the 10% V level.

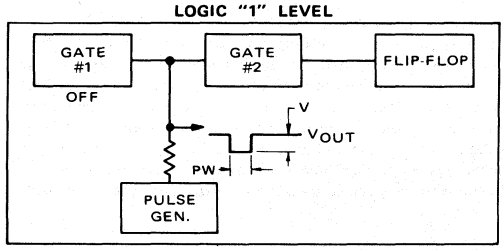
from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage. The total number of inputs that can be tied to the output of any driving gate is 50. (This is defined as high state output loading factor.) It should be noted that the low state output loading rules must still be maintained. The minimum logical "1" level, V_{OH} = 2.4 V minimum for the high-state output loading, with V_{tho} = 0.8 V, I_{OH} = -0.4 mA, and V_{CCL}.

SIGNAL LINE NOISE IMMUNITY

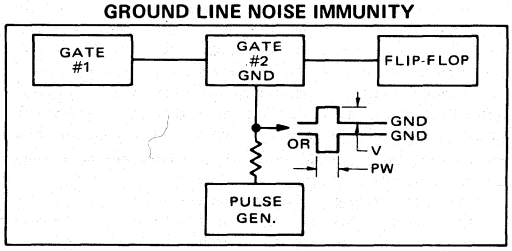
LOGIC "0" LEVEL



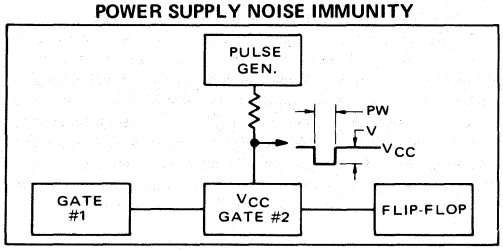
LOGIC "1" LEVEL



GROUND LINE NOISE IMMUNITY

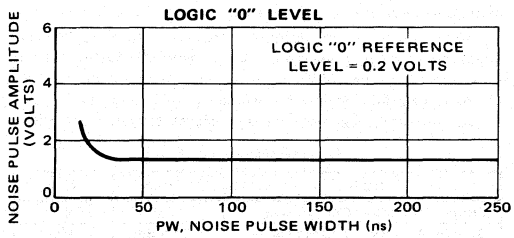


POWER SUPPLY NOISE IMMUNITY

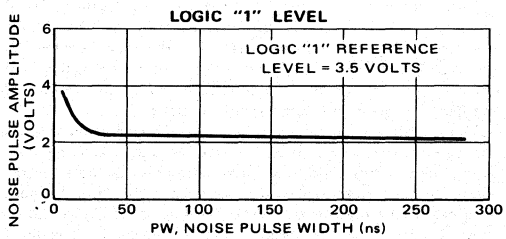


SIGNAL LINE NOISE IMMUNITY

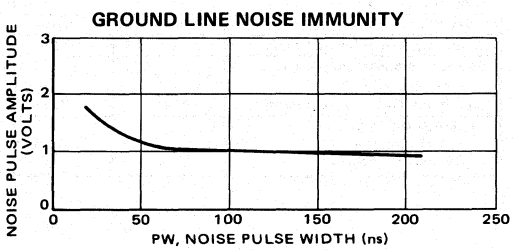
LOGIC "0" LEVEL



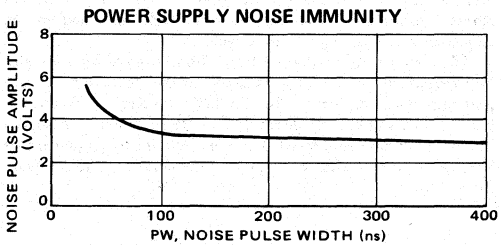
LOGIC "1" LEVEL



GROUND LINE NOISE IMMUNITY



POWER SUPPLY NOISE IMMUNITY



The unused inputs of the various flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Expanders and Expander Nodes

The ORing nodes of all the MTTL AND-OR-INVERT gates are made available for expanding the number of AND gates to 6 (MC5450F) or 8 (MC5453F). Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 1.0 ns/pF.

Output OR (AND) Function

Unlike the MDTL family of logic circuits, the outputs of the MTTL logic circuits cannot be tied together to perform the output OR, or more correctly, the output AND function. If the outputs of the MTTL family devices are tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground and the current that flows (approximately I_{SC}) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

Operating Characteristics of Flip-Flops

J-K Flip-Flop — MCBC5472/MCB5472F

This master-slave J-K flip-flop triggers on the negative edge of the clock. An AND-input configuration is used, consisting of three J inputs ANDed together and three K inputs ANDed together. A direct $\overline{SET}$ and $\overline{RESET}$ are provided to permit presetting data into the flip-flop. The direct $\overline{SET}$ and $\overline{RESET}$ control the operation of the flip-flop regardless of the state of the clock.

Information is normally applied to, or changed at the clocked inputs while the clock is in the low state since the master memory is inhibited in this condition. Information may be stored in the master flip-flop section when the clock goes high. Once the input data has been stored in the master flip-flop section it cannot be removed (or changed) by means of the clocked inputs. The direct $\overline{SET}$ or $\overline{RESET}$ provide the only means of removing previously stored information. They override the clock input and can be applied any time during the clock cycle.

The state of the master flip-flop is transferred to the slave flip-flop section on the negative transition of the clock, and the outputs respond accordingly. The flip-flop can be set or reset by applying a low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs. A special clamp circuit has been included on the clock line to guarantee that negative transients, such as ringing on the clock line, do not false-trigger the flip-flop. In addition, clamp diodes have been provided on all data inputs to limit any undershoot or negative ringing on the data lines.

Dual J-K Flip-Flop — MCB5473F

This dual master-slave J-K flip-flop also triggers on the negative edge of the clock. Each of the independent flip-flops has a single J and a single K input. A direct $\overline{RESET}$ has been provided for preclearing the flip-flop regardless of the state of the clock. The operation of this device is the same as the MCB5472F. Each of the flip-flops has the special clamp circuit on the clock line as well as clamp diodes on all the data inputs.

Noise Immunity

In a typical system noise begins to pose a problem when it is of such a magnitude that it can change the state of a flip-flop in the system or prevent a flip-flop from changing state at the proper time. Noise can be present on the ground line, the power supply line or the signal line.

In designing a system using MTTL, particular care must be taken due to the extremely high rate of change of voltage and current on the signal lines and current on the power supply and ground lines (see sections on Power and Ground Distribution and Bypassing). These factors increase the possibility of noise generation within the system itself in addition to externally generated noise.

Noise immunity in a digital system is a function of the propagation delays of the gates and flip-flops in the system and the dc threshold levels of these devices. The following block diagrams show typical test set-ups for measuring signal line, ground line and power supply line immunity of a gate in a digital system.

The system is considered disturbed when the flip-flop begins toggling. The curves show the typical noise amplitude a system can accept as a function of noise pulse width. As the pulse widths become narrower the amplitude can increase without disturbing the system. This can begin occurring when the pulse width is less than 20 ns on the signal line or 50 ns on the power supply or ground line. This pulse width-amplitude product is an indication of the minimum noise energy that is required to disturb a system. The low input and output impedances of MTTL gates and flip-flops requires more energy on the signal lines to distrub the system than in DTL or RTL systems. With proper power and ground distribution and bypassing, noise on power supply and ground lines can be maintained below levels which would be detrimental to system operation.

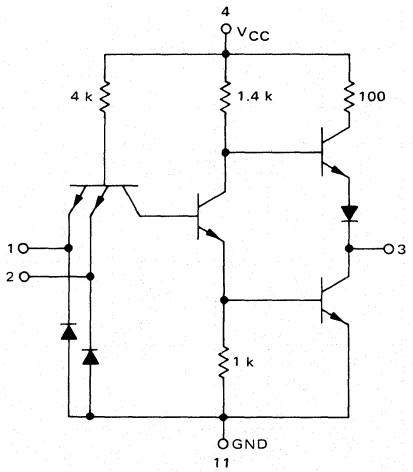
MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage — Continuous	+7.0	Vdc
Supply Operating Voltage Range	4.5 to 5.5	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range	-55 to +125	°C
Storage Temperature Range — Ceramic Package	-65 to +150	°C
Maximum Junction Temperature	+175	°C
Thermal Resistance — Junction-to-Case, θ_{JC} Ceramic Package	0.09	°C/mW

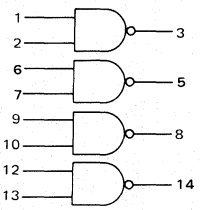
MCBC5400*
MCB5400F*

BEAM LEAD

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NAND gates that is produced using beam lead sealed junction technology. These devices are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.



Positive Logic: $3 = \overline{1 \bullet 2}$

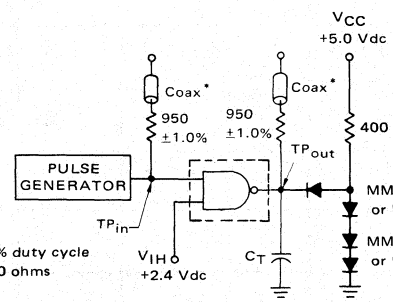
Negative Logic: $3 = \overline{1 + 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 40 mW typ/pkg

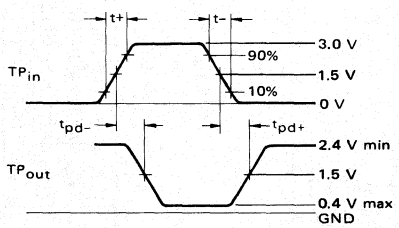
Propagation Delay Time = 10 ns typ

SWITCHING TIME TEST CIRCUIT



t+ = 12 ns
t- = 6.0 ns
PRF = 1.0 MHz, 50% duty cycle
Generator $Z_{out} \approx 50$ ohms

VOLTAGE WAVEFORMS AND DEFINITIONS



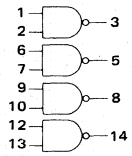
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

*F suffix = 1/4" x 1/4" ceramic package (Case 651). MCBC-prefixed devices are unencapsulated. Beam numbers are the same as the pin numbers for flat-packaged devices. See General Information section for package and chip details.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	Test Limits MCBC5400/MCBC5400F −55 to +125°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.5	5.5	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
Input																		
Forward Current	I_F	1	-	-1.6	mAdc	-	-	1	-	-	2	-	-	-	-	-	4	11*
Leakage Current	I_{R1}	1	-	40	μAdc	-	-	-	1	-	-	-	-	-	-	-	4	2,11*
	I_{R2}	1	-	1.0	mAdc	-	-	-	-	1	-	-	-	-	-	-	4	2,11*
Output																		
Output Voltage	V_{OL}	3	-	0.4	Vdc	3	-	-	-	-	-	-	1,2	-	-	4	-	11*
	V_{OH}	3	2.4	-	Vdc	-	3	-	-	-	2	-	-	1	-	2,4	-	11*
Short-Circuit Current	I_{SC}	3	-20	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,11*
Power Requirements (Total Device)																		
Power Supply Drain	I_{PDH}	4	-	22	mAdc	-	-	-	-	-	-	1,2,6,7,9, 10,12,13	-	-	-	-	4	11
	I_{PDL}	4	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,11*
Switching Parameters						Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1,3	-	15**	ns	1	3	-	2	-	-	-	-	-	4	-	-	11*
Turn-Off Delay	t_{pd+}	1,3	-	22**	ns	1	3	-	2	-	-	-	-	-	4	-	-	11*

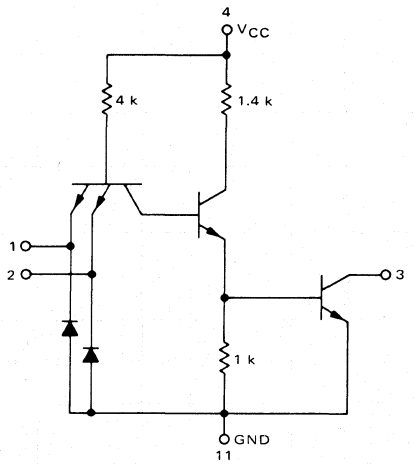
*Ground inputs to gates not under test.
**Tested only at 25°C.

QUAD 2-INPUT "NAND" GATE
WITH OPEN COLLECTOR

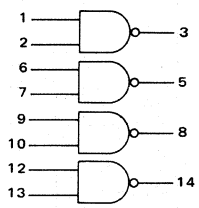
MCBC5401*
MCB5401F*

BEAM LEAD

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NAND gates with no output pullup network that is produced using beam lead sealed junction technology. These devices are particularly useful in highly reliable systems using hybrid beam lead assembly techniques, or standard flat package assembly techniques.



Positive Logic: $3 = \overline{1 \cdot 2}$
Negative Logic: $3 = \overline{1 + 2}$

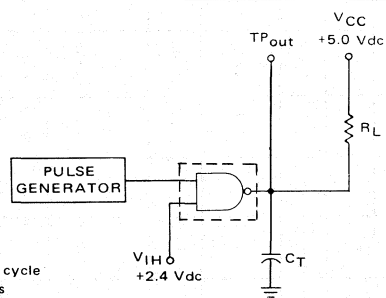
Input Loading Factor = 1
Output Loading Factor = 10

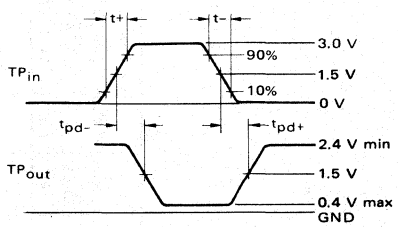
Total Power Dissipation = 40 mW typ/pkg

Propagation Delay Time = 35 ns typ

VOLTAGE WAVEFORMS AND DEFINITIONS

SWITCHING TIME TEST CIRCUIT





t+ = 12 ns
t- = 6.0 ns
PRF = 1.0 MHz, 50% duty cycle
Generator Z_{out} = 50 ohms

R_L = 400 ohms for t_{pd-} test.
4.0 k ohms for t_{pd+} test.

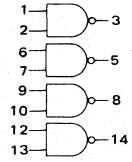
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 megohm) must be used for tests.

*F suffix = 1/4" x 1/4" ceramic package (Case 651). MCBC-prefixed devices are unencapsulated. Beam numbers are the same as the pin numbers for flat-packaged devices. See General Information section for package and chip details.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



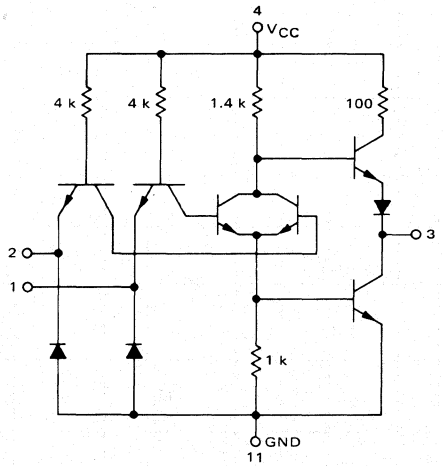
Characteristic	Symbol	Pin Under Test	Test Limits MCBC5401/MCBC5401F −55 to +125°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.5	5.5	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
						I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
Input																		
Forward Current	I_F	1	-	-1.6	mAdc	-	1	-	-	2	-	-	-	-	-	-	4	11*
Leakage Current	I_{R1}	1	-	40	μAdc	-	-	1	-	-	-	-	-	-	-	-	4	2,11*
	I_{R2}	1	-	1.0	mAdc	-	-	-	1	-	-	-	-	-	-	-	4	2,11*
Output																		
Output Voltage	V_{OL}	3	-	0.4	Vdc	3	-	-	-	-	-	1,2	-	-	-	4	-	11*
Output Leakage Current	I_{CEX}	3	-	0.25	mAdc	-	-	-	-	1	-	-	2	3	-	4	-	11*
Power Requirements (Total Device)																		
Power Supply Drain	I_{PDH}	4	-	22	mAdc	-	-	-	-	-	1,2,6,7,9, 10,12,13	-	-	-	-	-	4	11
	I_{PDL}	4	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,11*
Switching Parameters						Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1,3	-	15**	ns	1	3	2	-	-	-	-	-	-	4	-	-	11
Turn-Off Delay	t_{pd+}	1,3	-	45**	ns	1	3	2	-	-	-	-	-	-	4	-	-	11

*Ground inputs to gates not under test.
**Tested only at 25°C.

MCBC5402*
MCB5402F*

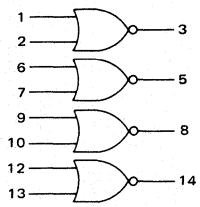
BEAM LEAD

1/4 OF CIRCUIT SHOWN



Pin numbers on drawings are for devices in the flat package.

This device consists of four 2-input NOR gates that is produced using beam lead sealed junction technology. These devices are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.



Positive Logic: $3 = \overline{1 + 2}$

Negative Logic: $3 = \overline{1 \cdot 2}$

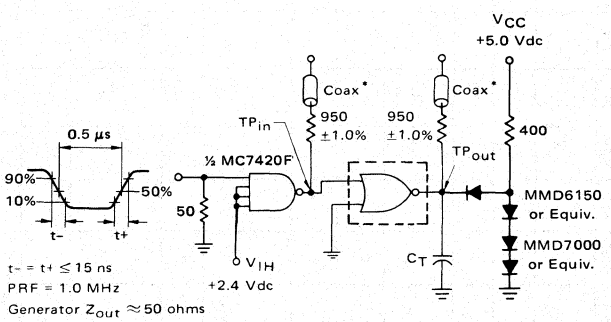
Input Loading Factor = 1
Output Loading Factor = 10

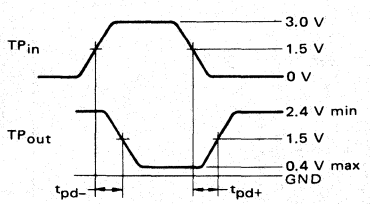
Total Power Dissipation = 48 mW typ/pkg
Propagation Delay Time = 10 ns typ

Package No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Beam No.	1	2	3	4	5	6	7	9	10	11	12	13	14	15

VOLTAGE WAVEFORMS AND DEFINITIONS

SWITCHING TIME TEST CIRCUIT





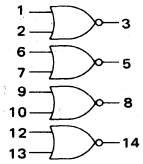
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

*F suffix = 1/4" x 1/4" ceramic package (Case 651) MCBC-prefixed devices are unencapsulated. See General Information section for package and chip details.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs. Pin numbers used are for devices in the flat package.

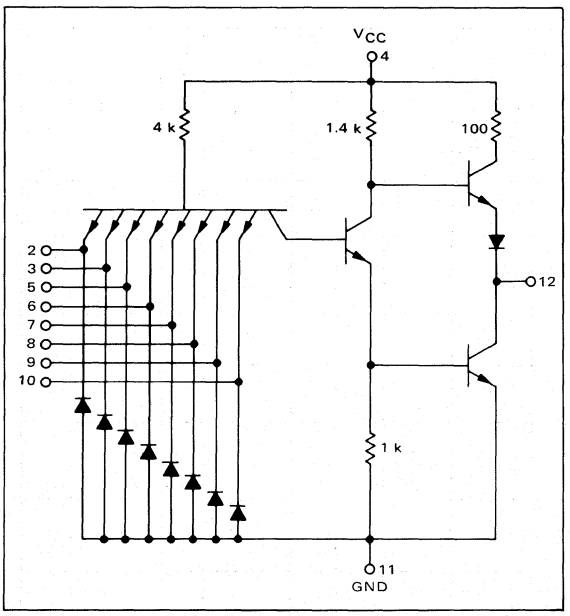


Characteristic	Symbol	Pin Under Test	Test Limits MCBC5402/MCB5402F −55 to +125°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						16	0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.5	5.5	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
Input																		
Forward Current	I_F	1	-	-1.6	mAdc	-	-	1	-	-	2	-	-	-	-	-	4	11*
Leakage Current	I_{R1}	1	-	40	μAdc	-	-	-	1	-	-	-	-	-	-	-	4	2,11*
	I_{R2}	1	-	1.0	mAdc	-	-	-	-	1	-	-	-	-	-	-	4	2,11*
Output																		
Output Voltage	V_{OL}	3	-	0.4	Vdc	3	-	-	-	-	-	-	1	-	-	4	-	2,11*
	V_{OH}	3	2.4	-	Vdc	-	3	-	-	-	-	-	-	2	-	4	-	1,11*
Short-Circuit Current	I_{SC}	3	-20	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,11*
Power Requirements (Total Device)																		
Power Supply Drain	I_{PDH}	4	-	27	mAdc	-	-	-	-	-	-	1,2,6,7,9, 10,12,13	-	-	-	-	4	11
	I_{PDL}	4	-	16	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,11*
Switching Parameters						Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1,3	-	15**	ns	1	3	-	-	-	-	-	-	-	4	-	-	2,11*
Turn-Off Delay	t_{pd+}	1,3	-	22**	ns	1	3	-	-	-	-	-	-	-	4	-	-	2,11*

*Ground inputs to gates not under test.
**Tested only at 25°C.

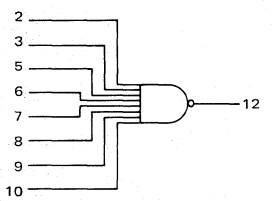
MCBC5430*
MCB5430F*

BEAM LEAD



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders and decoders.

Beam lead sealed junction technology is used to manufacture these devices. They are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.



Positive Logic:

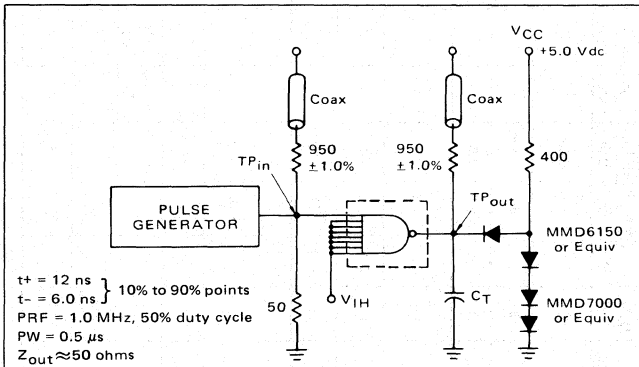
$12 = \overline{2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 8 \cdot 9 \cdot 10}$

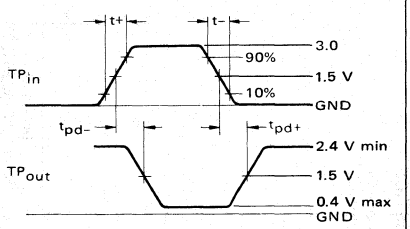
Negative Logic:

$12 = \overline{2 + 3 + 5 + 6 + 7 + 8 + 9 + 10}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 10 mW typ/pkg
Propagation Delay Time = 10 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





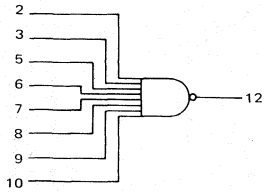
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

*F suffix = 1/4" x 1/4" ceramic package (Case 651). MCBC-prefixed devices are unencapsulated. Beam numbers are the same as the pin numbers for flat-packaged devices. See General Information section for package and chip details.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input. To complete testing, sequence through remaining inputs in the same manner.



Characteristic	Symbol	Pin Under Test	Test Limits MCBC5430/MCB5430F −55 to +125°C Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
						mA		Volts										
						16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
Input																		
Forward Current	I_F	2	-	-1.6	mAdc	-	-	2	-	-	3,5,6,7,8,9,10	-	-	-	-	-	4	11
Leakage Current	I_{R1}	2	-	40	μAdc	-	-	-	2	-	-	-	-	-	-	-	4	3,5,6,7,8,9,10
	I_{R2}	2	-	1.0	mAdc	-	-	-	-	2	-	-	-	-	-	-	4	3,5,6,7,8,9,10
Output																		
Output Voltage	V_{OL}	12	-	0.4	Vdc	12	-	-	-	-	-	-	2,3,5,6,7,8,9,10	-	-	4	-	11
	V_{OH}	12	2.4	-	Vdc	-	12	-	-	-	3,5,6,7,8,9,10	-	-	2	-	4	-	11
Short-Circuit Current	I_{SC}	12	-20	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	2,3,5,6,7,8,9,10,11,12
Power Requirements																		
Power Supply Drain	I_{PDH}	4	-	6.0	mAdc	-	-	-	-	-	-	2,3,5,6,7,8,9,10	-	-	-	-	4	11
	I_{PDL}	4	-	2.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	2,3,5,6,7,8,9,10,11
Switching Parameters						Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	2,12	-	15**	ns	2	12	-	3,5,6,7,8,9,10	-	-	-	-	-	4	-	-	11
Turn-Off Delay	t_{pd+}	2,12	-	22**	ns	2	12	-	3,5,6,7,8,9,10	-	-	-	-	-	4	-	-	11

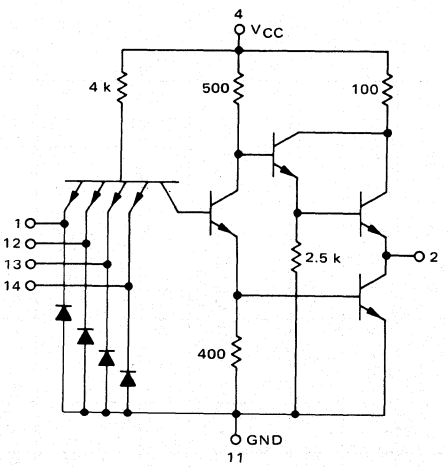
**Tested only at 25°C.

DUAL 4-INPUT "NAND" BUFFER

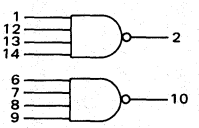
MCBC5440*
MCB5440F*

BEAM LEAD

1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND power gates that are produced using beam lead sealed junction technology. These devices are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.



Positive Logic: $2 = \overline{1 \cdot 12 \cdot 13 \cdot 14}$

Negative Logic: $2 = \overline{1 + 12 + 13 + 14}$

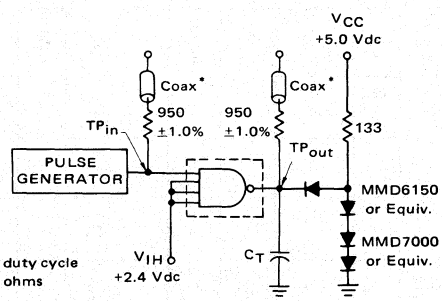
Input Loading Factor = 1

Output Loading Factor = 30

Total Power Dissipation = 50 mW typ/pkg

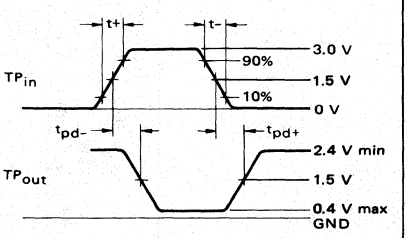
Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT



t+ = 12 ns
t- = 6.0 ns
PRF = 1.0 MHz, 50% duty cycle
Generator $Z_{out} \approx 50$ ohms

VOLTAGE WAVEFORMS AND DEFINITIONS



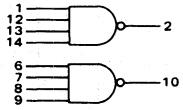
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

*F suffix = 1/4" x 1/4" ceramic package (Case 651). MCBC-prefixed devices are unencapsulated. Beam numbers are the same as the pin numbers for flat-packaged devices. See General Information section for package and chip details.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

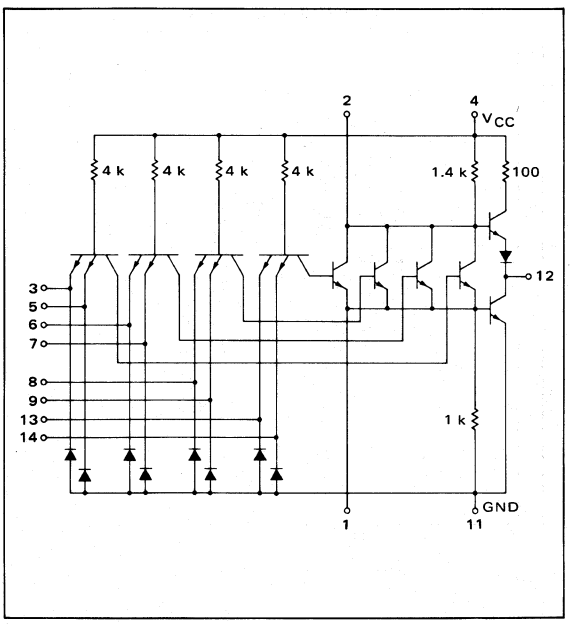


Characteristic	Symbol	Pin Under Test	Test Limits MCBC5440/MCB5440F −55 to +125°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						48	-1.2	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.5	5.5	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
						I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CC}	V_{CCL}	V_{CCH}	
Input																		
Forward Current	I_F	1	-	-1.6	mAdc	-	-	1	-	-	12,13,14	-	-	-	-	-	4	11*
Leakage Current	I_{R1}	1	-	40	μAdc	-	-	-	1	-	-	-	-	-	-	-	4	11,12,13,14*
	I_{R2}	1	-	1.0	mAdc	-	-	-	-	1	-	-	-	-	-	-	4	11,12,13,14*
Output																		
Output Voltage	V_{OL}	2	-	0.4	Vdc	2	-	-	-	-	-	-	1,12,13,14	-	-	4	-	11*
	V_{OH}	2	2.4	-	Vdc	-	2	-	-	-	12,13,14	-	-	1	-	4	-	11*
Short-Circuit Current	I_{SC}	2	-20	-70	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,11,12,13,14*
Power Requirements (Total Device)																		
Power Supply Drain	I_{PDH}	4	-	27	mAdc	-	-	-	-	-	-	1,6,7,8,9, 12,13,14	-	-	-	-	4	11
	I_{PDL}	4	-	8	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,11,12,13,14*
Switching Parameters						Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1,2	-	15**	ns	1	2	-	12,13,14	-	-	-	-	-	4	-	-	11*
Turn-Off Delay	t_{pd+}	1,2	-	22**	ns	1	2	-	12,13,14	-	-	-	-	-	4	-	-	11*

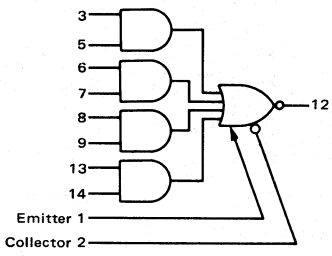
*Ground inputs to gate not under test.
**Tested only at 25°C.

MCBC5453*
MCB5453F*

BEAM LEAD



This device consists of four 2-input AND gates ORed together and inverted. Up to four MCB5460 expander gates may be ORed with the device at the expander points. Beam lead sealed junction technology is used to manufacture these devices. They are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.



Positive Logic:

$12 = \overline{(3 \cdot 5) + (6 \cdot 7) + (8 \cdot 9) + (13 \cdot 14) + (\text{Expanders})}$

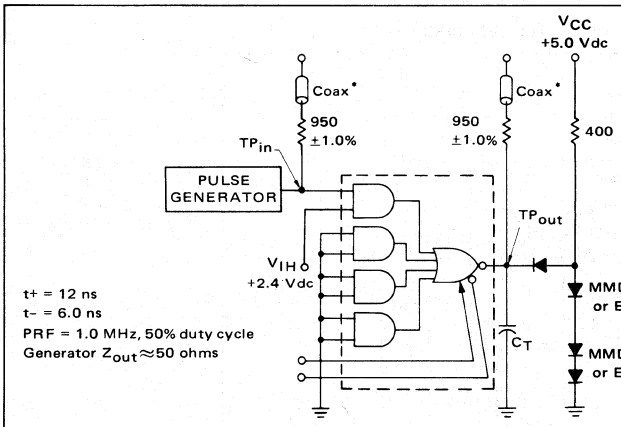
Negative Logic:

$12 = \overline{(3 + 5) \cdot (6 + 7) \cdot (8 + 9) \cdot (13 + 14) \cdot (\text{Expanders})}$

Input Loading Factor = 1
Output Loading Factor = 10

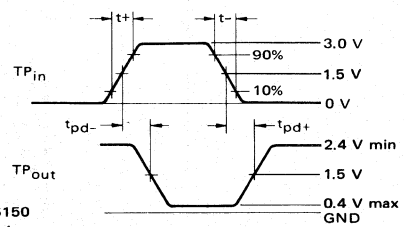
Total Power Dissipation = 22 mW typ/pkg
Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT



t+ = 12 ns
t- = 6.0 ns
PRF = 1.0 MHz, 50% duty cycle
Generator $Z_{out} \approx 50$ ohms

VOLTAGE WAVEFORMS AND DEFINITIONS



Expander pins should be left open when measuring switching times.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

*F suffix = 1/4" x 1/4" ceramic package (Case 651). MCBC-prefixed devices are unencapsulated. Beam numbers are the same as the pin numbers for flat-packaged devices. See General Information section for package and chip details.

FIGURE 1 – I_{EX} TEST CIRCUIT

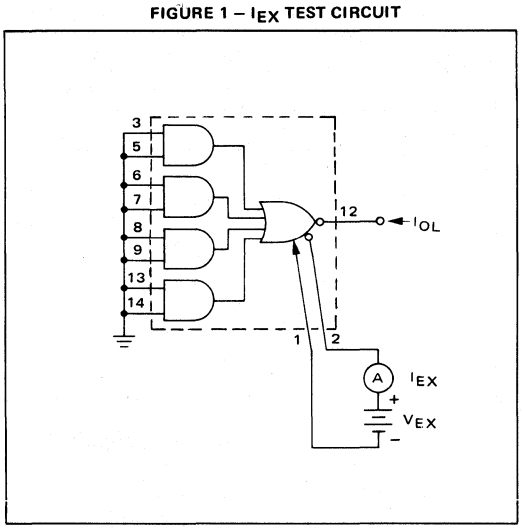


FIGURE 2 – V_{BE} TEST CIRCUIT

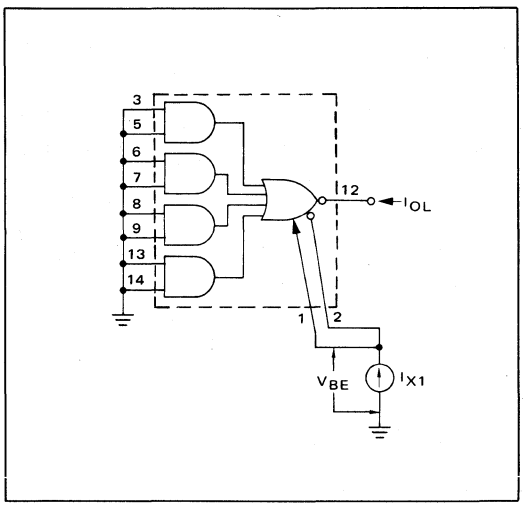
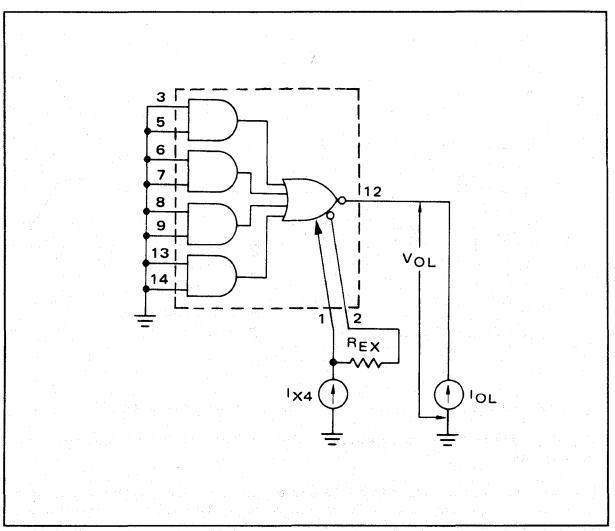
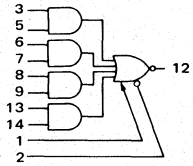


FIGURE 3 – V_{OL} TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one input of the device. To complete testing, sequence through remaining inputs in a similar manner.



Characteristic	Symbol	Pin Under Test	Test Limits MCBC5453/MCBC5453F −55 to +125°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	I_{X1}	I_{X2}	I_{X3}	I_{X4}	Ohms R_{EX}③	Volts V_{EX}①	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						16	-0.4	0.41	0.27	-0.27	0.3	138	0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.5	5.5	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																		
Input																								
Forward Current	I_F	3	-	-1.6	mAdc	-	-	-	-	-	-	-	-	3	-	-	5	-	-	-	-	-	4	11
Leakage Current	I_{R1}	3	-	40	μAdc	-	-	-	-	-	-	-	-	-	3	-	-	-	-	-	-	-	4	3,6,7,8,9, 11,13,14
	I_{R2}	3	-	1.0	mAdc	-	-	-	-	-	-	-	-	-	-	3	-	-	-	-	-	-	4	3,6,7,8,9, 11,13,14
Expander Input Current	I_{EX}	2 ①	-	-2.9	mAdc	12	-	-	-	-	-	-	1,2	-	-	-	-	-	-	-	-	4	-	3,5,6,7,8,9, 11,13,14
Base-Emitter Voltage	V_{BE}	1 ②	-	1.0	Vdc	12	-	1,2	-	-	-	-	-	-	-	-	-	-	-	-	-	4	-	3,5,6,7,8,9, 11,13,14
Output																								
Output Voltage	V_{OL}	12	-	0.4	Vdc	12	-	-	-	-	-	-	-	-	-	-	-	-	3,5	-	-	4	-	6,7,8,9, 11,13,14
		12③	-	0.4	Vdc	12	-	-	-	-	1	2	-	-	-	-	-	-	-	-	-	4	-	3,5,6,7,8,9, 11,13,14
	V_{OH}	12	2.4	-	Vdc	-	12	-	-	-	-	-	-	-	-	-	3,7, 9,14	-	-	5,6,8, 13	-	4	-	11
		12	2.4	-	Vdc	-	12	-	1	2	-	-	-	-	-	-	-	-	-	-	-	4	-	3,5,6,7,8,9, 11,13,14
Short-Circuit Current	I_{SC}	12	-20	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	4	3,5,6,7,8,9,11, 12,13,14
Power Requirements																								
Power Supply Drain	I_{PDH}	4	-	9.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	3,5,6,7,8, 9,13,14	-	-	-	-	4	11
	I_{PDL}	4	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	4	3,5,6,7,8,9, 11,13,14
Switching Parameters						Pulse In	Pulse Out																	
Turn-On Delay	t_{pd-}	3,12	-	15**	ns	3	12	-	-	-	-	-	-	-	5	-	-	-	-	-	4	-	-	6,7,8,9, 11,13,14
Turn-Off Delay	t_{pd+}	3,12	-	22**	ns	3	12	-	-	-	-	-	-	-	5	-	-	-	-	-	4	-	-	6,7,8,9, 11,13,14

** Tested only at 25°C.

① See Figure 1.

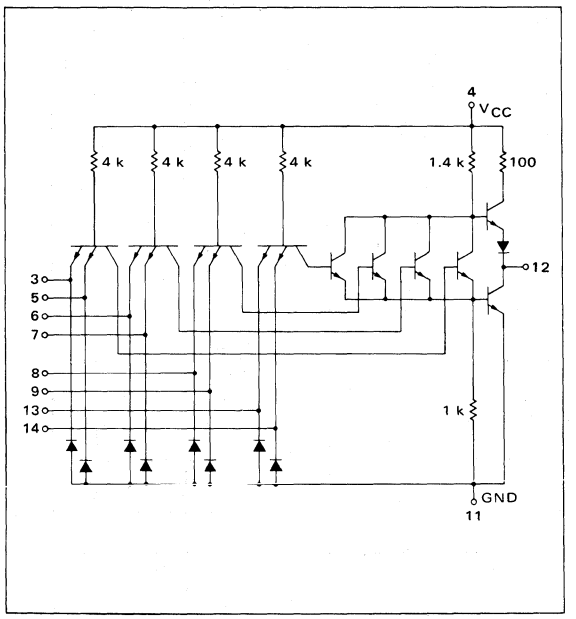
② See Figure 2.

③ See Figure 3.

4-WIDE 2-INPUT
"AND-OR-INVERT" GATE

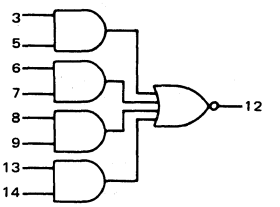
MCBC5454*
MCB5454F*

BEAM LEAD



This device consists of four 2-input AND gates ORed together and inverted.

Beam lead sealed junction technology is used to manufacture these devices. They are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.



Positive Logic:

$12 = \overline{(3 \bullet 5) + (6 \bullet 7) + (8 \bullet 9) + (13 \bullet 14)}$

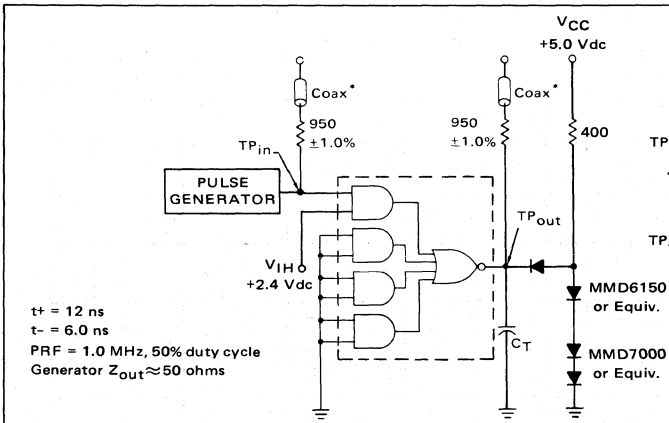
Negative Logic:

$12 = \overline{(3+5) \bullet (6+7) \bullet (8+9) \bullet (13+14)}$

Input Loading Factor = 1
Output Loading Factor = 10

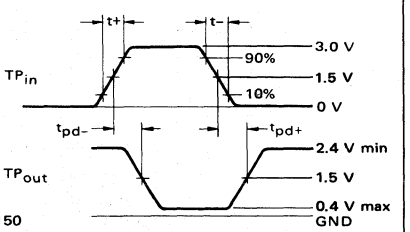
Total Power Dissipation = 22 mW typ/pkg
Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT



t+ = 12 ns
t- = 6.0 ns
PRF = 1.0 MHz, 50% duty cycle
Generator $Z_{out} \approx 50$ ohms

VOLTAGE WAVEFORMS AND DEFINITIONS



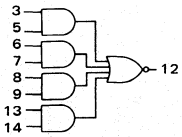
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

*F suffix = 1/4" x 1/4" ceramic package (Case 651). MCBC-prefixed devices are unencapsulated. Beam numbers are the same as the pin numbers for flat-packaged devices. See General Information section for package and chip details.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of this device. To complete testing, sequence through remaining inputs in the same manner.



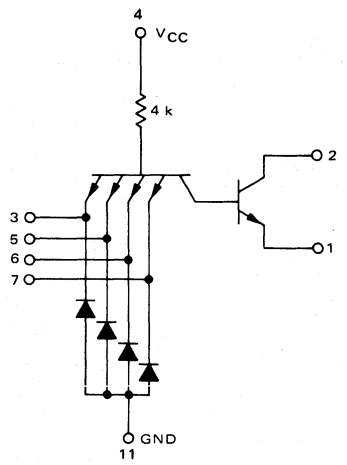
Characteristic	Symbol	Pin Under Test	Test Limits MCBC5454/MCB5454F −55 to +125°C Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
						mA		Volts										
						16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.5	5.5	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
Input																		
Forward Current	I_F	3	-	-1.6	mAdc	-	-	3	-	-	5	-	-	-	-	-	4	11
Leakage Current	I_{R1}	3	-	40	μAdc	-	-	-	3	-	-	-	-	-	-	-	4	5,6,7,8,9,11,13,14
	I_{R2}	3	-	1.0	mAdc	-	-	-	-	3	-	-	-	-	-	-	4	5,6,7,8,9,11,13,14
Output																		
Output Voltage	V_{OL}	12	-	0.4	Vdc	12	-	-	-	-	-	-	3,5	-	-	4	-	6,7,8,9,11,13,14
	V_{OH}	12	2.4	-	Vdc	-	12	-	-	-	5,7,9, 14	-	-	3,6,8, 13	-	4	-	11
Short-Circuit Current	I_{SC}	12	-20	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	3,5,6,7,8,9,11,12,13,14
Power Requirements																		
Power Supply Drain	I_{PDH}	4	-	9.5	mAdc	-	-	-	-	-	-	3,5,6,7,8, 9,13,14	-	-	-	-	4	11
	I_{PDL}	4	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	3,5,6,7,8,9,11,13,14
Switching Parameters						Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	3,12	-	15**	ns	3	12	-	5	-	-	-	-	-	4	-	-	6,7,8,9,11,13,14
Turn-Off Delay	t_{pd+}	3,12	-	22**	ns	3	12	-	5	-	-	-	-	-	4	-	-	6,7,8,9,11,13,14

**Tested only at 25°C.

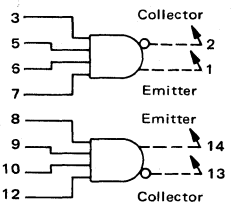
MCBC5460*
MCB5460F*

BEAM LEAD

1/2 OF CIRCUIT SHOWN

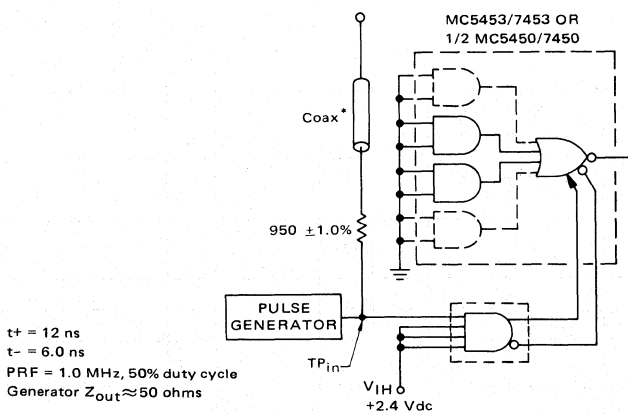


This device consists of two 4-input OR expanders for use with the AND-OR-INVERT gates. A maximum of four expander gates can be added to the MCB5450 or MCB5453 expandable gates without seriously affecting their operation. Beam lead sealed junction technology is used to manufacture these devices. They are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.



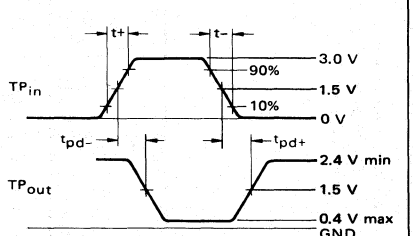
Input Loading Factor = 1
Full output loading factor of the expandable gate is maintained.
Total Power Dissipation = 8.0 mW typ/pkg
Propagation Delay Time = 5.0 ns typ

SWITCHING TIME TEST CIRCUIT



t+ = 12 ns
t- = 6.0 ns
PRF = 1.0 MHz, 50% duty cycle
Generator $Z_{out} \approx 50$ ohms

VOLTAGE WAVEFORMS AND DEFINITIONS



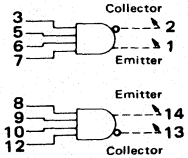
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

*F suffix = 1/4" x 1/4" ceramic package (Case 651). MCBC-prefixed devices are unencapsulated. Beam numbers are the same as the pin numbers for flat-packaged devices. See General Information section for package and chip details.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in the same manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	Test Limits MCBC5460/MCBC5460F −55 to +125°C Min	Max	Unit	TEST VOLTAGE VALUES (All Temperatures) Ohms R_{EX1}	R_{EX2}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{O1}	V_{O2}	V_{O3}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						1.2 k*	1.1 k‡	0.4	2.4	5.5	4.5	5.0	2.0	0.8	4.5	1.0	0.85	5.0	4.5	5.5	
						TEST VOLTAGE APPLIED TO PINS LISTED BELOW:															
						R_{EX1}	R_{EX2}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{O1}	V_{O2}	V_{O3}	V_{CC}	V_{CCL}	V_{CCH}	
Input																					
Forward Current	I_F	5	-	-1.6	mAdc	-	-	5	-	-	3,6,7	-	-	-	-	-	-	-	-	4	11
Leakage Current	I_{R1}	5	-	40	μAdc	-	-	-	5	-	-	-	-	-	-	-	-	-	-	4	3,6,7,11
	I_{R2}	5	-	1.0	mAdc	-	-	-	-	5	-	-	-	-	-	-	-	-	-	4	3,6,7,11
Output																					
Output Voltage	V_{OL}	1,2†	-	0.4	Vdc	-	2	-	-	-	-	-	3,5,6,7	-	-	1	-	-	4	-	11
Leakage Current	I_{CEX}	2	-	150§	μAdc	1	-	-	-	-	3,6,7	-	-	5	2	-	-	-	4	-	11
Drive Current	I_{DR}	1	-0.3	-	mAdc	-	-	-	-	-	-	-	3,5,6,7	-	-	1	-	-	4	-	11
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDL}	4	-	4.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	1,14	-	-	4	3,5,6,7,8,9,10,11,12
	I_{PDH}	4	-	2.5	mAdc	-	-	-	-	-	-	3,5,6,7,8, 9,10,12	-	-	-	-	1,14	-	-	4	11
Switching Parameters						Pulse In															
Turn-On Delay	t_{pd-}	#	-	20**	ns	5	-	-	3,6,7	-	-	-	-	-	-	-	-	4	-	-	11
Turn-Off Delay	t_{pd+}	#	-	30**	ns	5	-	-	3,6,7	-	-	-	-	-	-	-	-	4	-	-	11

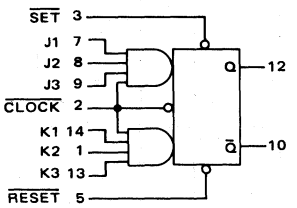
*Resistor to ground.
‡Resistor to V_{CCL}.
#See test circuit.
†V_{OL} measured between pins 1 and 2.
§Tested only at low temperature limit; i.e., at -55°C for MCB5460.
**Tested only at 25°C; times include delay of expandable gate.

J-K FLIP-FLOP

MCBC5472*
MCB5472F*

BEAM LEAD

This negative-edge-clocked J-K flip-flop operates on the master-slave principle. Three K inputs are ANDed together, and three J inputs are ANDed together. $\overline{SET}$ and $\overline{RESET}$ inputs are also available. The device helps minimize package count in J-K flip-flop applications requiring AND gating into the J or K inputs. Beam lead sealed junction technology is used to manufacture these devices. They are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

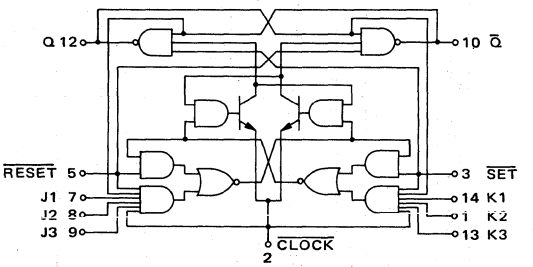
J = J1 • J2 • J3
K = K1 • K2 • K3

Input Loading Factor:
J, K = 1
$\overline{CLOCK}$, $\overline{SET}$, $\overline{RESET}$ = 2

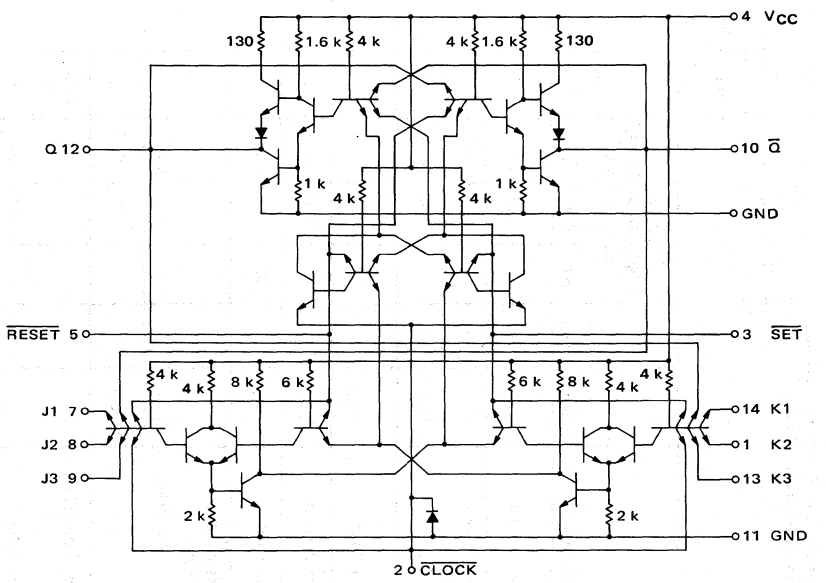
Output Loading Factor = 10

Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 30 ns typ
Max Operating Frequency = 20 MHz typ

LOGIC DIAGRAM



Package No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Beam No.	1	2	3	4	5	6	7	9	10	11	12	13	14	15



*F suffix = 1/4" x 1/4" ceramic package (Case 651) MCBC-prefixed devices are unencapsulated. See General Information section for package and chip details.

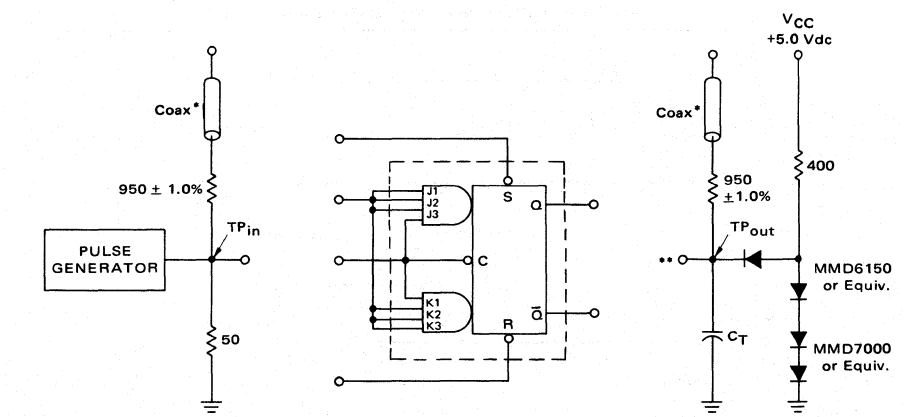
OPERATING CHARACTERISTICS

Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{SET}$ input will force the Q output to the logic "1" state, and application of a logic "0" to the $\overline{RESET}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{SET}$ and $\overline{RESET}$ inputs override the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 20 ns minimum.

SWITCHING TIME TEST CIRCUIT



t+ = 12 ns
t− = 6 ns } 10% to 90% points
f = 10 MHz for waveform A
1.0 MHz for waveforms B, E, and F

Two pulse generators are required and must be slaved together for testing $\overline{SET}$ and $\overline{RESET}$. Only one pulse generator is required for J, K, and $\overline{CLOCK}$ tests.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

**A load is connected to each output during the test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

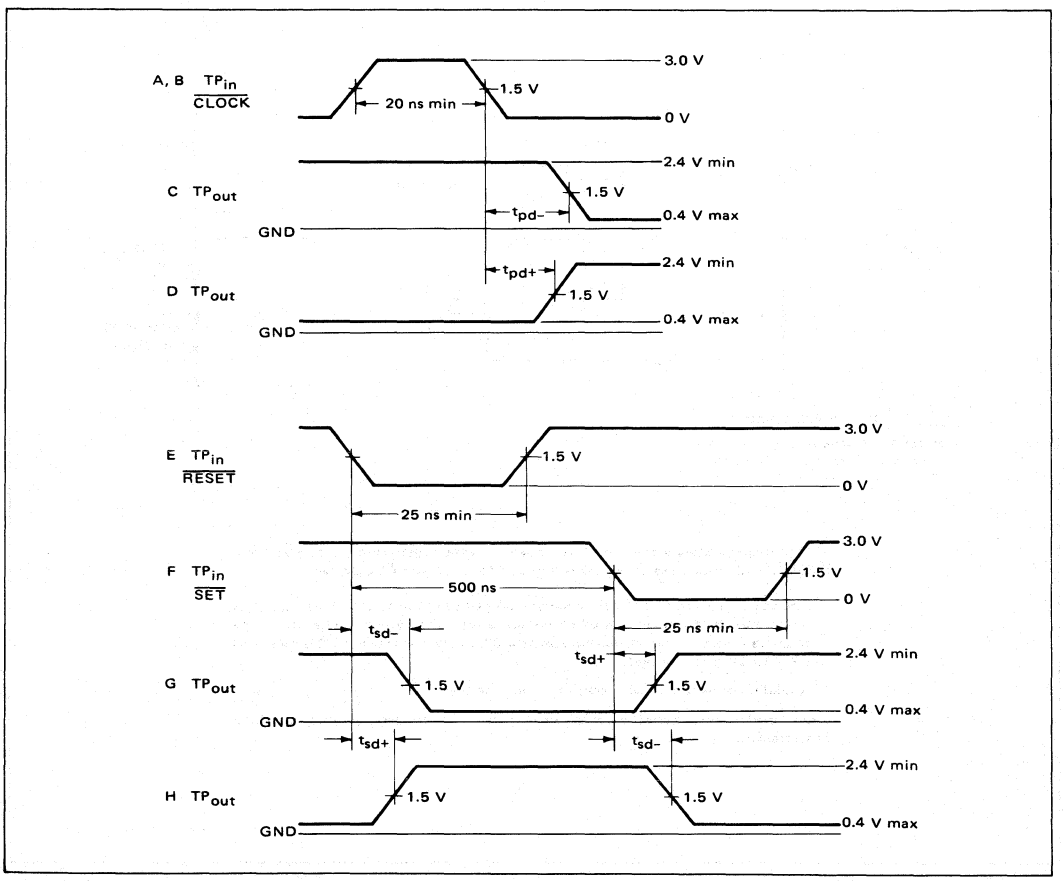
TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				Q	$\bar{Q}$	LIMITS		
		$\bar{C}$	J, K	$\bar{R}$	$\bar{S}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	A	2.4 V	2.4 V	†	†	15	–	MHz
Turn-On Delay	t_{pd-}	B	B	2.4 V	2.4 V	C	C	10	40	ns
Turn-Off Delay	t_{pd+}	B	B	2.4 V	2.4 V	D	D	10	25	ns
Turn-On Delay	t_{sd-}	2.4 V	2.4 V	E	F	G	H	–	40	ns
Turn-Off Delay	t_{sd+}	2.4 V	2.4 V	E	F	G	H	–	25	ns
Enable Voltage	V_{EN}	B	2.0 V	2.4 V	2.4 V	†	†	†	–	–
Inhibit Voltage	V_{INH}	B	0.8 V	2.4 V	2.4 V	‡	‡	‡	–	–

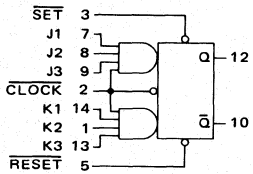
†Output shall toggle with each input pulse.
‡Output shall NOT toggle.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, plus the $\overline{SET}$, $\overline{RESET}$, and $\overline{CLOCK}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



Characteristic		Symbol	Pin Under Test	Test Limits MCBC5472/MCB5472F −55 to +125°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CCL}	V_{CCH}	Gnd
							16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	4.5	5.5	
							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
							I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CCL}	V_{CCH}	Gnd
Input																	
Forward Current	J	I_F	7	-	-1.6	mAdc	-	-	7	-	-	2,5*,8,9	-	-	-	4	11
	K		14	-	-1.6		-	-	14	-	-	1,2,3*,13	-	-	-		
	$\overline{Set}$		3	-	-3.2		-	-	3	-	-	1,2,7,8,9,13,14	-	-	-		
	$\overline{Reset}$		5	-			-	-	5	-	-	1,2,7,8,9,13,14	-	-	-		
	$\overline{Clock}$		2	-			-	-	2	-	-	1,5*,7,8,9,13,14	-	-	-		
			2	-			-	-	2	-	-	1,3*,7,8,9,13,14	-	-	-		
Leakage Current	J	I_{R1}	7	-	40	μAdc	-	-	-	7	-	-	-	-	-	4	2,5,8,9,11
	K		14	-	40		-	-	-	14	-	-	-	-	-		1,2,3,11,13
	$\overline{Set}$		3	-	80		-	-	-	3	-	-	-	-	-		2,7,8,9,11
	$\overline{Reset}$		5	-			-	-	-	5	-	-	-	-	-		1,2,11,13,14
	$\overline{Clock}$		2**	-			-	-	-	2	-	-	-	-	-		1,2,5,7,8,9,11,13,14
	J	I_{R2}	7	-	1.0	mAdc	-	-	-	-	7	-	-	-	-	4	2,5,8,9,11
	K		14	-			-	-	-	-	14	-	-	-	-		1,2,3,11,13
	$\overline{Set}$		3	-			-	-	-	-	3	-	-	-	-		2,7,8,9,11
	$\overline{Reset}$		5	-			-	-	-	-	5	-	-	-	-		1,2,11,13,14
	$\overline{Clock}$		2	-			-	-	-	-	2	-	-	-	-		1,3,5,7,8,9,11,13,14
Output																	
Output Voltage		V_{OL}	10	-	0.4	Vdc	10	-	-	-	-	-	5	3	4	-	11
			12	-	0.4	Vdc	12	-	-	-	-	-	3	5	4	-	11
		V_{OH}	10	2.4	-	Vdc	-	10	-	-	-	-	3	5	4	-	11
			12	2.4	-	Vdc	-	12	-	-	-	-	5	3	4	-	11
Short-Circuit Current		I_{SC}	10	-20	-57	mAdc	-	-	-	-	-	1,7,8,9,13,14	-	-	-	4	2,5,10,11
			12	-20	-57	mAdc	-	-	-	-	-	1,7,8,9,13,14	-	-	-	4	2,3,11,12
Power Requirements																	
Power Supply Drain		I_{PD}	4	-	20	mAdc	-	-	-	-	-	-	-	-	-	4	5,11
			4	-	20	mAdc	-	-	-	-	-	-	-	-	-	4	3,11

*Momentarily ground pin prior to taking measurement.
**Under normal operating conditions this current is negative. This test guarantees that positive leakage current will not exceed the limit shown.

MTTL

INTEGRATED CIRCUIT

MEMORIES

MTTL

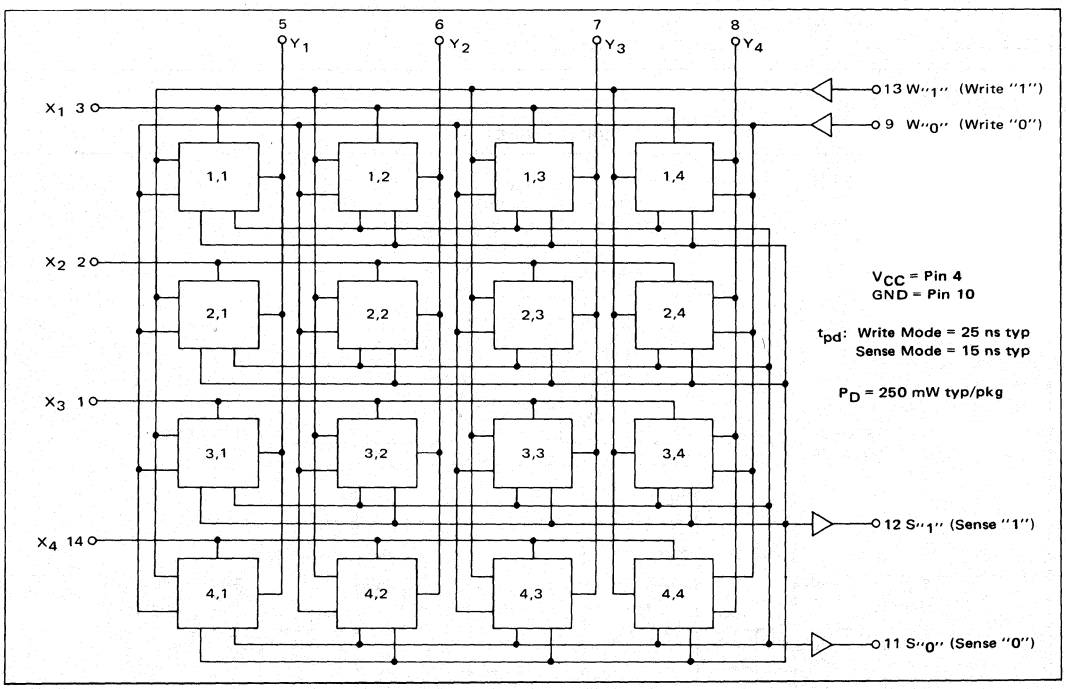
MEMORIES

INDEX

MC4304F,L • MC4305F,L*
MC4004F,L,P • MC4005F,L,P*

This 16-Bit memory cell serves as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

The memory contains 16 flip-flops arranged in a four-by-four matrix. A single bit of the matrix is selected by driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many devices can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two write amplifiers allow a "1" or a "0" to be written into a selected bit.



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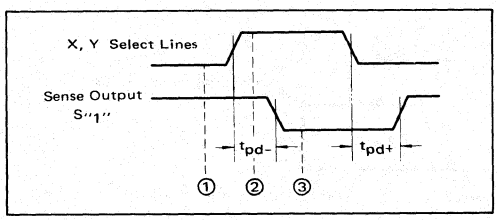
– OPERATING SEQUENCE –

FIGURE 1 – READ MODE TIMING DIAGRAM



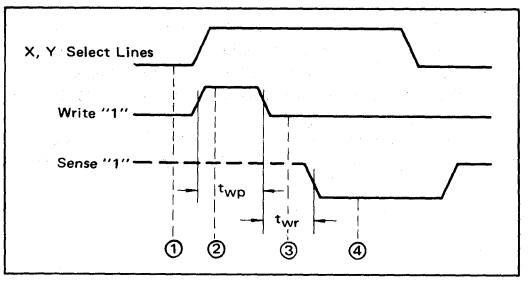
① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Desired bit selected by driving the appropriate X and Y select lines more positive than +2.1 V.

③ After the turn-on delay time(t_{pd-}), the S"1" output will be low (less than +0.45 V) and the S"0" output will be high (more than +2.5 V), providing that a "1" is stored in the selected bit.

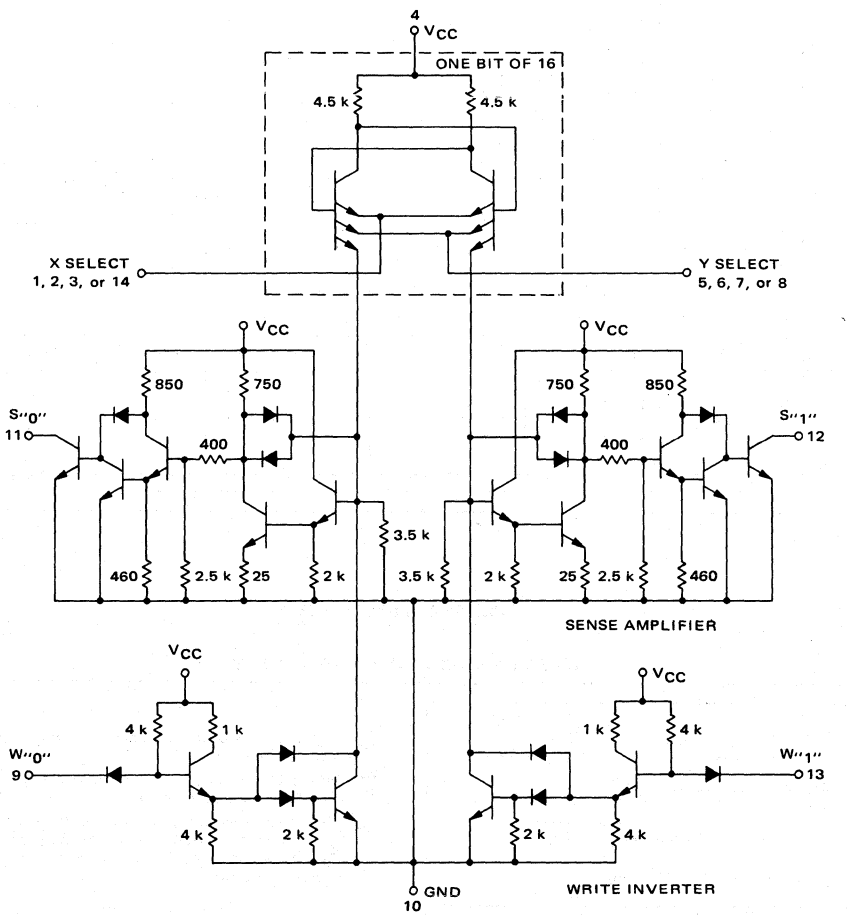
*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

FIGURE 2 – WRITE MODE TIMING DIAGRAM



① All X and Y selection lines and both write inputs are low (less than +0.8 V).
② Bit location selected by driving the appropriate X and Y select lines more positive than +2.1 V. To write a "1", drive the write "1" input more positive than +2.1 V for a minimum time of 25 ns (t_{wp}).
③ Write "1" line returned to low state.
④ The stored bit can be read after the write recovery time (t_{wr}) of 40 ns. (The sense output is in an indeterminate state between steps 2 and 4.)

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one bit.
Other bits are tested in the same manner.

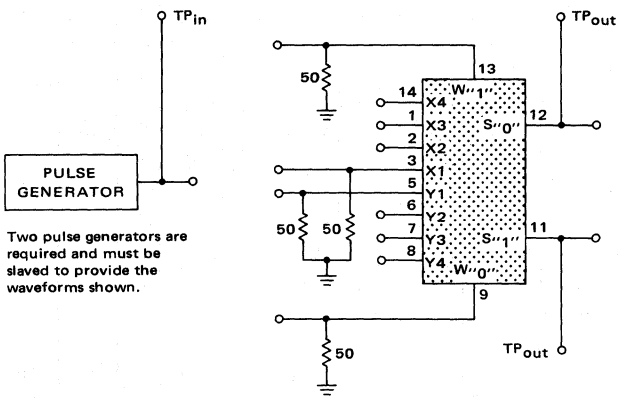
	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
		mA				Volts									
		$I_{S''0''}$		I_W	I_{XY}	$V_{in\,1}$	$V_{in\,2}$	$V_{in\,3}$	V_F	V_R	V_{th}	V_{out}	V_{CC}	BV_{ckt}	
		Pr*	Std												
MC4304*, MC4305	−55°C	40	20	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0	-	
	+25°C	40	20	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0	7.0	
	+125°C	40	20	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0	-	
MC4004*, MC4005	0°C	40	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0	-	
	+25°C	40	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0	7.0	
	+75°C	40	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0	-	

Characteristic	Symbol	Pin Under Test	MC4304, MC4305 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4004, MC4005 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{S''0''}$	I_W	I_{XY}	$V_{in\,1}$	$V_{in\,2}$	$V_{in\,3}$	V_F	V_R	V_{th}	V_{out}	V_{CC}	BV_{ckt}	Gnd
Input																												
Forward Current Address Lines	I_F	3	-	-11	-	-11	-	-11	-	-13.5	-	-13.5	-	-13.5	mAdc	-	-	-	-	-	-	3	5,6,7,8	-	-	4	-	1,2,9,10,13,14
		5	-	-11	-	-11	-	-11	-	-13.5	-	-13.5	-	-13.5	mAdc	-	-	-	-	-	-	5	1,2,3,14	-	-	4	-	6,7,8,9,10,13
Write Inputs		9	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	9	-	-	-	4	-	1,2,3,5,6,7,8,10,13,14
		13	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	13	-	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Leakage Current Address Lines	I_R	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	mAdc	-	-	-	-	-	-	-	3	-	-	4	-	1,2,5,6,7,8,9,10,13,14
		5	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	mAdc	-	-	-	-	-	-	-	5	-	-	4	-	1,2,3,6,7,8,9,10,13,14
Write Inputs		9	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	-	9	-	-	4	-	1,2,3,5,6,7,8,10,13,14
		13	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	-	13	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Breakdown Voltage Address Lines	BV_{in}	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	3	-	-	-	-	-	-	-	4	-	1,2,5,6,7,8,9,10,13,14
		5	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	5	-	-	-	-	-	-	-	4	-	1,2,3,6,7,8,9,10,13,14
Write Inputs		9	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	9	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,10,13,14
		13	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	13	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Output (Note 1)																												
Output Voltage Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	-	-	3,5,13	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "0" Inhibit	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	3,5	-	-	13	9	-	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "0"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13	-	-	3,5,9	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "1" Inhibit	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	3,5	-	-	9	13	-	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	-	-	3,5,13	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Leakage Current Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	-	-	3,5,13	-	4	-	1,2,6,7,8,10,14
Leakage Current	I_{OLK}	12	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	3,5	-	-	-	-	12	4	-	1,2,6,7,8,9,10,13,14
Write "0"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13	-	-	3,5,9	-	4	-	1,2,6,7,8,10,14
Leakage Current	I_{OLK}	11	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	3,5	-	-	-	-	11	4	-	1,2,6,7,9,10,13,14
Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13	3,5,6,7,8	-	4	-	1,2,9,10,14
Leakage Current	I_{OLK}	11	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	-	-	3,5,6,7,8	11	4	-	1,2,9,10,13,14
Write "0"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	3,5,6,7,8	-	4	-	1,2,10,13,14
Leakage Current	I_{OLK}	12	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	-	-	3,5,6,7,8	-	4	-	1,2,9,10,13,14
Power Requirements (Total Device)																												
Power Supply Drain	I_{PD}	4	-	65	-	65	-	65	-	72	-	72	-	72	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,13,14
Power Supply Breakdown Current	I_{ckt}	4	-	-	-	95	-	-	-	-	-	105	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,13,14

*Prime Fan-Out

Note 1. Output logic "0" voltage and leakage current measurements are made as part of a functional test of a memory. Procedures identified by a double asterisk (**) are preconditioning procedures for the subsequent test. All power supply and input voltages must be maintained between tests.

SWITCHING TIME TEST CIRCUIT



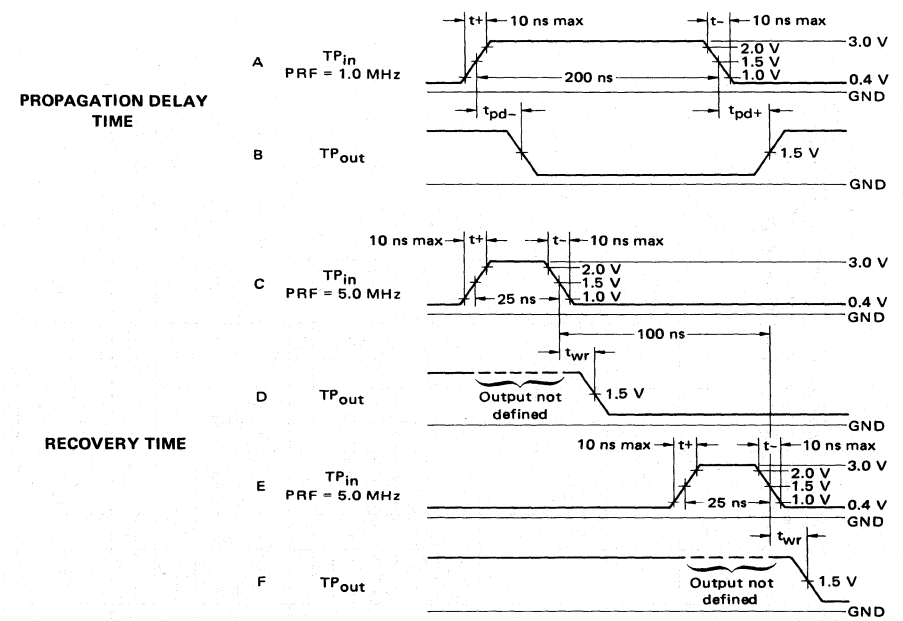
Two pulse generators are required and must be slaved to provide the waveforms shown.

High-impedance probes (>1.0 Megohm) must be used when taking measurements.

DEVICE UNDER TEST	R1 OHMS	R2 OHMS
MC4304, MC4004	120	330
MC4305, MC4005	240	560

See Switching Time Test Procedures table for value of C_T.

VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms)

Test	Symbol	Pin Under Test	Input Pin										Output		C_T* pF	Limits	
			3 X_1	2 X_2	1 X_3	14 X_4	5 Y_1	6 Y_2	7 Y_3	8 Y_4	9 W"0"	13 W"1"	11 S"0"	12 S"1"		MC4304-5 ns max	MC4004-5 ns max
Turn-Off Delay Time (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	30	23	23
	t_{pd+}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	35	35
Turn-Off Delay Time (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	30	23	23
	t_{pd+}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	35	35
Turn-On Delay Time (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd-}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	30	23	23
	t_{pd-}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	35	35
Turn-On Delay Time (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd-}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	30	23	23
	t_{pd-}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	35	35
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	11	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	B	–	30	35	35
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	12	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	–	B	30	35	35
Write Recovery Time	t_{wr}	12	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	–	D	30	40	40
		11	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	F	–	30	40	40
																ns min	ns min
Write Pulse Width	t_{wp}	–	Tested during t_{wr} tests.													25	25

*Capacitance value for load of the Switching Time Test Circuit

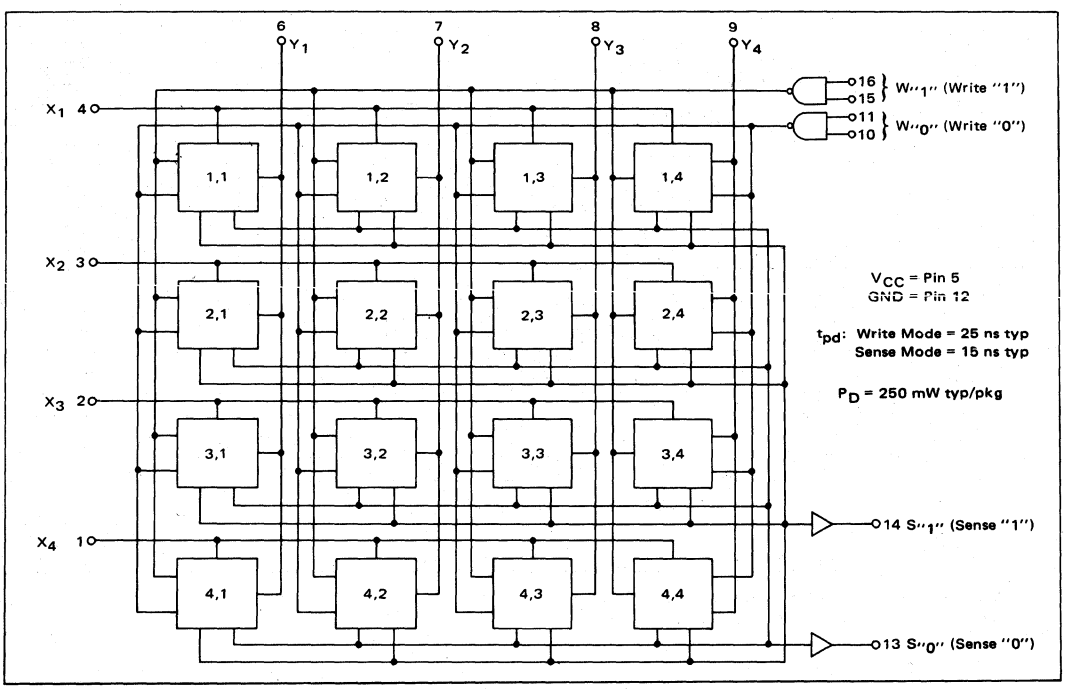
**Preconditioning procedures for subsequent test.

16-BIT SCRATCH PAD
MEMORY CELL
WITH GATED INPUTS

MC5484L*
MC7484L,P*

This 16-Bit memory cell serves as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

The memory contains 16 flip-flops arranged in a four-by-four matrix. A single bit of the matrix is selected by driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many devices can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two gated write amplifiers allow a "1" or a "0" to be written into a selected bit.



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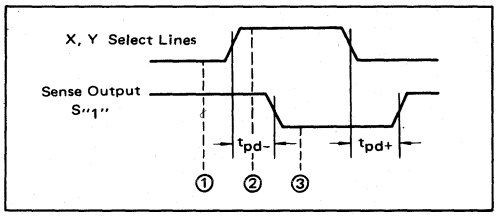
– OPERATING SEQUENCE –

FIGURE 1 – READ MODE TIMING DIAGRAM



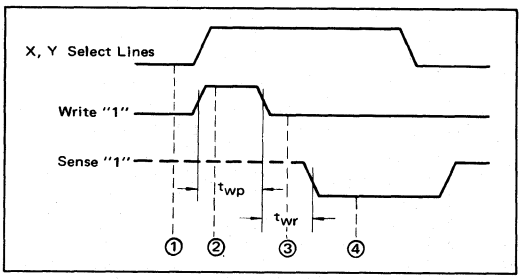
① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Desired bit selected by driving the appropriate X and Y select lines more positive than +2.1 V.

③ After the turn-on delay time(t_{pd-}), the S"1" output will be low (less than +0.45 V) and the S"0" output will be high (more than +2.5 V), providing that a "1" is stored in the selected bit.

*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

FIGURE 2 – WRITE MODE TIMING DIAGRAM



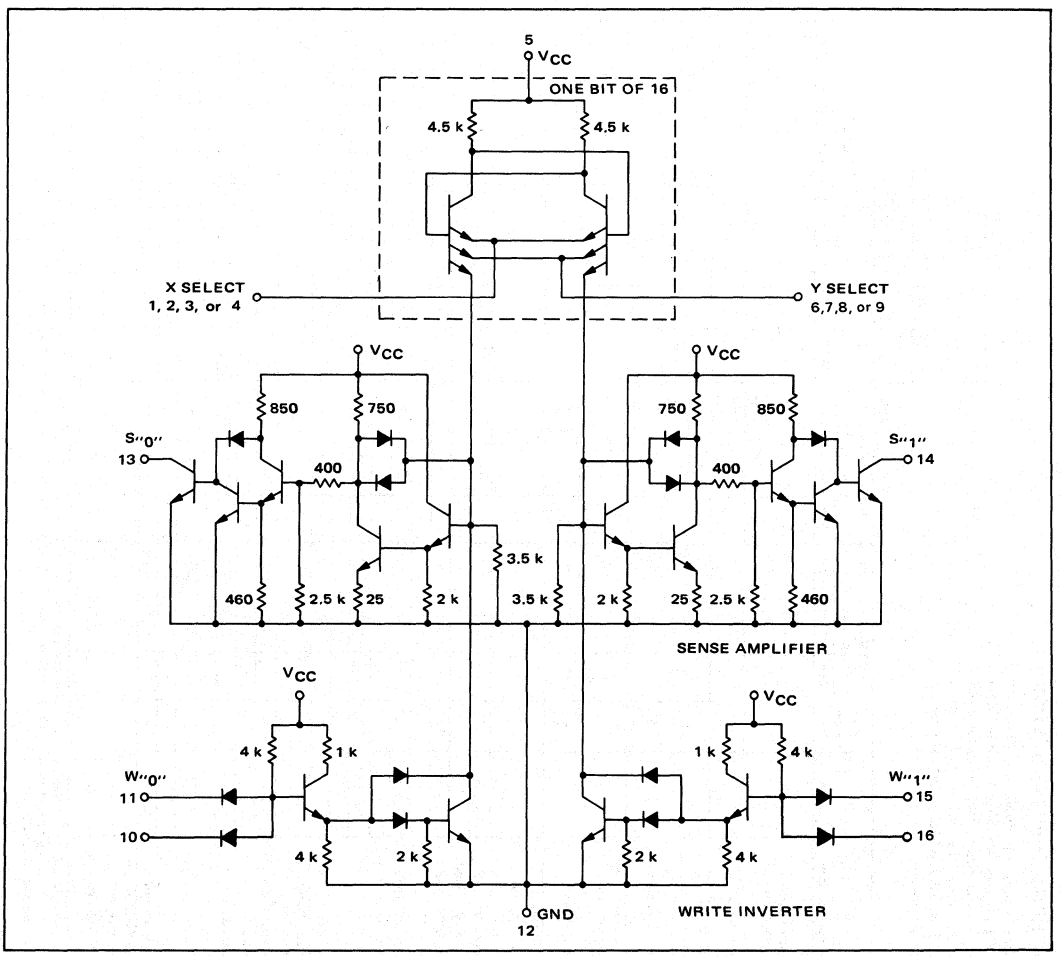
① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Bit location selected by driving the appropriate X and Y select lines more positive than +2.1 V. To write a "1", drive the write "1" input more positive than +2.1 V for a minimum time of 25 ns (t_{wp}).

③ Write "1" line returned to low state.

④ The stored bit can be read after the write recovery time (t_{wr}) of 60 ns. (The sense output is in an indeterminate state between steps 2 and 4.)

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one bit. Other bits are tested in the same manner. In addition, test procedures are shown for only one Write input of each level. The other Write inputs are tested in the same manner.

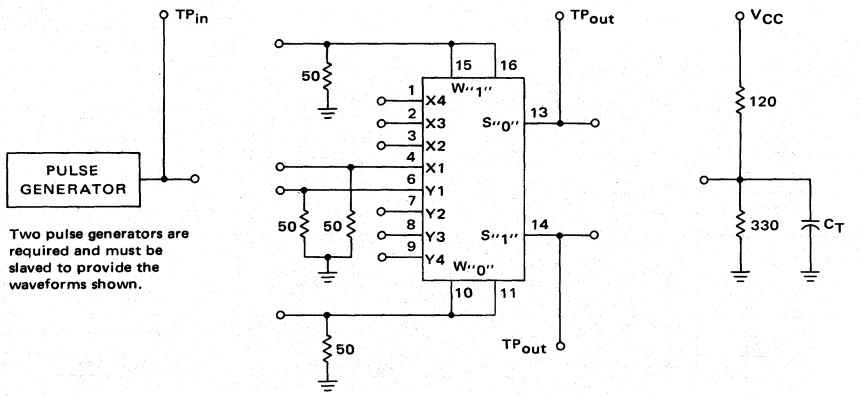
	TEST CURRENT/VOLTAGE VALUES (All Temperatures)													
	mA			Volts										
	$I_{S"0"}$	I_W	I_{XY}	$V_{in\,1}$	$V_{in\,2}$	$V_{in\,3}$	V_F	V_R	V_{th}	$V_{th\,W}$	V_{out}	V_{CCL}	V_{CCH}	
MC5484	40	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	2.0	2.0	4.5	5.5	
MC7484	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	2.0	2.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC5484 Test Limits -55 to +125°C			MC7484 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												Gnd
			Min	Max	Unit	Min	Max	Unit	$I_{S"0"}$	I_W	I_{XY}	$V_{in\,1}$	$V_{in\,2}$	$V_{in\,3}$	V_F	V_R	V_{th}	$V_{th\,W}$	V_{out}	V_{CCL}	V_{CCH}	
Input																					
Forward Current Address Lines	I_F	1	–	-11	mAdc	–	-11	mAdc	–	–	–	–	–	–	1	6,7,8,9	–	–	–	–	5	2,3,4,10,11,12,15,16
		6	–	-11	mAdc	–	-11	mAdc	–	–	–	–	–	–	6	1,2,3,4	–	–	–	–	5	7,8,9,10,11,12,15,16
Write Inputs		10	–	-1.60	mAdc	–	-1.60	mAdc	–	–	–	–	–	–	10	–	–	–	–	–	5	1,2,3,4,6,7,8,9,12,15,16
		15	–	-1.60	mAdc	–	-1.60	mAdc	–	–	–	–	–	–	15	–	–	–	–	–	5	1,2,3,4,6,7,8,9,10,11,12
Leakage Current Address Lines	I_R	1	–	0.4	mAdc	–	0.4	mAdc	–	–	–	–	–	–	–	1	–	–	–	–	5	2,3,4,6,7,8,9,10,11,12,15,16
		6	–	0.4	mAdc	–	0.4	mAdc	–	–	–	–	–	–	–	6	–	–	–	–	5	1,2,3,4,7,8,9,10,11,12,15,16
Write Inputs		10	–	0.1	mAdc	–	0.1	mAdc	–	–	–	–	–	–	–	10	–	–	–	–	5	1,2,3,4,6,7,8,9,12,15,16
		15	–	0.1	mAdc	–	0.1	mAdc	–	–	–	–	–	–	–	15	–	–	–	–	5	1,2,3,4,6,7,8,9,10,11,12
Breakdown Voltage Address Lines	BV_{in}	1	5.5	–	Vdc	5.5	–	Vdc	–	–	1	–	–	–	–	–	–	–	–	–	5	2,3,4,6,7,8,9,10,11,12,15,16
		6	5.5	–	Vdc	5.5	–	Vdc	–	–	6	–	–	–	–	–	–	–	–	–	5	1,2,3,4,7,8,9,10,11,12,15,16
Write Inputs		10	5.5	–	Vdc	5.5	–	Vdc	–	10	–	–	–	–	–	–	–	–	–	–	5	1,2,3,4,6,7,8,9,12,15,16
		15	5.5	–	Vdc	5.5	–	Vdc	–	15	–	–	–	–	–	–	–	–	–	–	5	1,2,3,4,6,7,8,9,10,11,12
Output (Note 1)																					
Output Voltage Write "1"	**	–	–	–	–	–	–	–	–	–	–	–		10,11	–	–	1,6	15,16	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	14	–	0.45	Vdc	–	0.45	Vdc	14	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "0" Inhibit	**	–	–	–	–	–	–	–	–	–	–	1,6	–	–	15,16	10,11	–	–	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	14	–	0.45	Vdc	–	0.45	Vdc	14	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "0"	**	–	–	–	–	–	–	–	–	–	–	–	–	15,16	–	–	1,6	10,11	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	13	–	0.45	Vdc	–	0.45	Vdc	13	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "1" Inhibit	**	–	–	–	–	–	–	–	–	–	–	1,6	–	–	10,11	15,16	–	–	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	13	–	0.45	Vdc	–	0.45	Vdc	13	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "1"	**	–	–	–	–	–	–	–	–	–	–	–	–	10,11	–	–	1,6	15,16	–	5	–	2,3,4,7,8,9,12
Logic "0" Level	V_{out} "0"	14	–	0.45	Vdc	–	0.45	Vdc	14	–	–	–	–	–	–	–	1,6	–	–	5	–	2,3,4,7,8,9,10,11,12,15,16
Leakage Current Write "1"	**	–	–	–	–	–	–	–	–	–	–	–	–	10,11	–	–	1,6	15,16	–	5	–	2,3,4,7,8,9,12
Leakage Current	I_{OLK}	14	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	1,6	–	–	–	–	–	14	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "0"	**	–	–	–	–	–	–	–	–	–	–	–	–	15,16	–	–	1,6	10,11	–	5	–	2,3,4,7,8,9,12
Leakage Current	I_{OLK}	13	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	1,6	–	–	–	–		13	5	–	2,3,4,7,8,9,10,11,12,15,16
Write "1"	**	–	–	–	–	–	–	–	–	–	–	–	–	–	–	15,16	1,6,7,8,9	–	–	5	–	2,3,4,10,11,12
Leakage Current	I_{OLK}	13	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	–	–	–	–	1,6,7,8,9	–	13	5	–	2,3,4,10,11,12,15,16
Write "0"	**	–	–	–	–	–	–	–	–	–	–	–	–	–	–	10,11	1,6,7,8,9	–	–	5	–	2,3,4,12,15,16
Leakage Current	I_{OLK}	14	–	0.25	mAdc	–	0.25	mAdc	–	–	–	–	–	–	–	–	1,6,7,8,9	–	14	5	–	2,3,4,10,11,12,15,16
Power Requirements (Total Device)																					
Power Supply Drain	I_{PD}	5	–	78#	mAdc	–	91#	mAdc	–	–	–	–	–	–	–	–	–	–	–	–	5	1,2,3,4,6,7,8,9,10, 11,12,13,14,15,16

Note 1. Output logic "0" voltage and leakage current measurements are made as part of a functional test of a memory. ** Indicates preconditioning procedures for the subsequent test. All power supply and input voltages must be maintained between tests.

Tested only at 25°C.

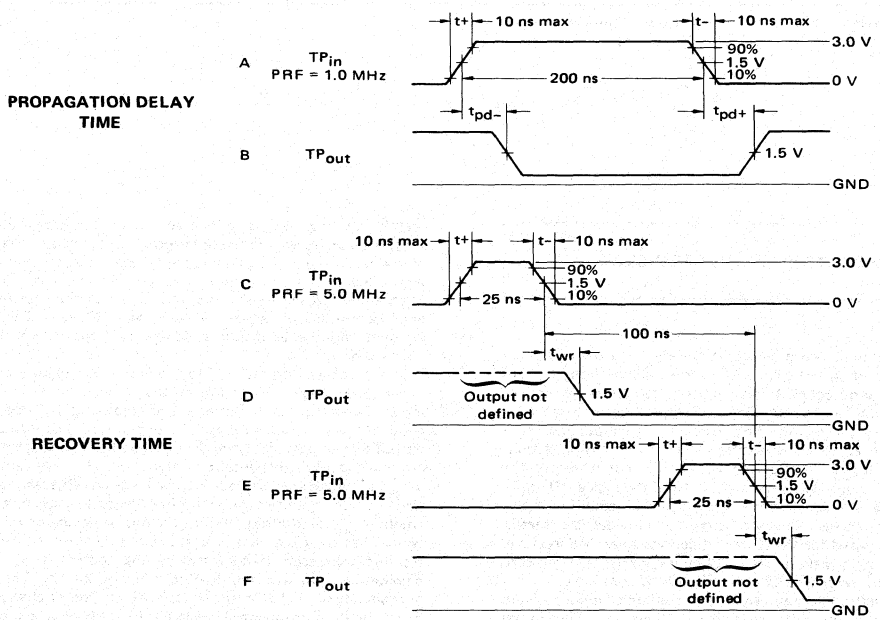
SWITCHING TIME TEST CIRCUIT



High-impedance probes (>1.0 Megohm) must be used when taking measurements.

See Switching Time Test Procedures table for value of C_T.

VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms)

Test	Symbol	Pin Under Test	Input Pin										Output		C_T* pF	Limits	
			4 X_1	3 X_2	2 X_3	1 X_4	6 Y_1	7 Y_2	8 Y_3	9 Y_4	10 W"0"	15 W"1"	13 S"0"	14 S"1"		MC5484 ns max	MC7484 ns max
Turn-Off Delay Time (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	15	25	25
	t_{pd+}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	35	35
Turn-Off Delay Time (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	15	25	25
	t_{pd+}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	35	35
Turn-On Delay Time (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd-}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	15	45	45
	t_{pd-}	13	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	55	55
Turn-On Delay Time (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd-}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	15	45	45
	t_{pd-}	14	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	55	55
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "0" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	13	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	B	–	15	30	30
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "1" Output)	**	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	**	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	14	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	–	B	15	30	30
Write Recovery Time	t_{wr}	14	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	–	D	15	60	60
		13	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	F	–	15	60	60
																ns min	ns min
Write Pulse Width	t_{wp}	–	Tested during t_{wr} tests.													25	25

*Capacitance value for load of the Switching Time Test Circuit

**Preconditioning procedures for subsequent test.

OPERATING CHARACTERISTICS

Sixteen flip-flops are arranged in a 4-by-4 matrix with each flip-flop representing one bit of 16 words. Each flip-flop, consisting of two cross-coupled triple-emitter transistors, is used to store one bit. Memory status of a particular bit is determined by sensing which of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logical "1" sensing outputs are connected to the sense logic "1" amplifier input, and all 16 of the logical "0" sensing outputs are connected to the sense logic "0" amplifier input. The remaining emitters on each transistor provides the matrix connections required for the X- and Y-address lines. Address line inputs are normally held at logic "0" and currents from all conducting flip-flop transistors flow out of these address lines.

To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a logic "1" voltage. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a logic "0" level and no change will occur on those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense amplifier associated with a logic "1" or the sense amplifier associated with a logic "0" is activated. When this occurs, the output of the activated sense amplifier drops from a logic "1" to a logic "0" level. The memory is non-destructive as the states of the flip-flops are not disturbed during sensing.

To store new information in a flip-flop, it is necessary to address it and apply logic "1" voltage to the appropriate write amplifier input. The output of the write amplifier responds by dropping to a logic "0" level. Since all logic "0" sense lines are connected to the output of the logic "0" write amplifier and all logic "1" sense lines are connected to the output of the logic "1" write amplifier, a logic "0" voltage on the output of a write amplifier will apply the same voltage to emitters of all flip-flop transistors connected to that amplifier. In all flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. But two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. But if the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on, causing the other transistor to turn off.

TYPICAL APPLICATIONS

A fast scratch pad memory offers the system designer several design alternatives. Temporary memory with a greater storage capacity than simple registers can be distributed throughout a system. The basic technique for expanding bit capacity is shown in Figure 3; Figure 4 illustrates a method for expanding word capacity.

Optimum design of the selection line drivers depends on the specific system application. The maximum load presented to the drivers by the selection lines is a function of the sequence used to address the memory. The desired logic swing and noise immunity should also be considered when designing the drivers. Each of the 16 flip-flops draws a maximum dc supply current of 2.75 mA (for V_{CC} = 5.0 Vdc). The total current flowing in all 16 flip-flops, and consequently the summed current in the eight selection lines, is 44 mA. (Each selection line is tested for a maximum of 11 mA).

Consider the sequence involved in selecting the four bits X_1Y_1, X_1Y_2, X_1Y_3, and X_1Y_4 simultaneously. If the four Y select lines are enabled before the X_1 line then each of the four X lines must carry the full current from four cells, i.e., 11 mA. The Y drivers must also have the capability of sinking 11 mA if the four X drivers are enabled before a Y driver. However, if the memory accessing sequence specifies that only a single bit may be selected at a time and, consequently, that only one of the X (or Y) selection lines may be high at a time, then the driver requirements can be relaxed somewhat. This is possible because of current sharing in the multi-emitters of the storage flip-flop transistors. If the voltages at the emitters of the "on" transistor differ by no more than approximately 100 mV, then each emitter will carry an appreciable portion of the transistor current. The saturation characteristics of the drivers determine the emitter potentials and, therefore, the division of cell current among the various drivers. Since the V_{OL} of the driver will increase if the collector current increases, the selection currents will be almost evenly distributed among the drivers if the driver saturation characteristics are reasonably uniform. If operation is restricted to a single X selection line and a single Y selection line and current sharing is assumed, then each select line must be capable of carrying the full current from a single cell plus approximately one half of the current from three cells. Each line must, therefore, carry:

$$11/4 + (3)\ (1/2)\ (11/4) = 6.88\ \text{mA}.$$

Since the dc output levels of the driver transistors determine the noise immunity of the selection line, the system noise environment and the desired noise immunity should enter into the driver selection.

FIGURE 3 – 16 WORD, N BIT MEMORY

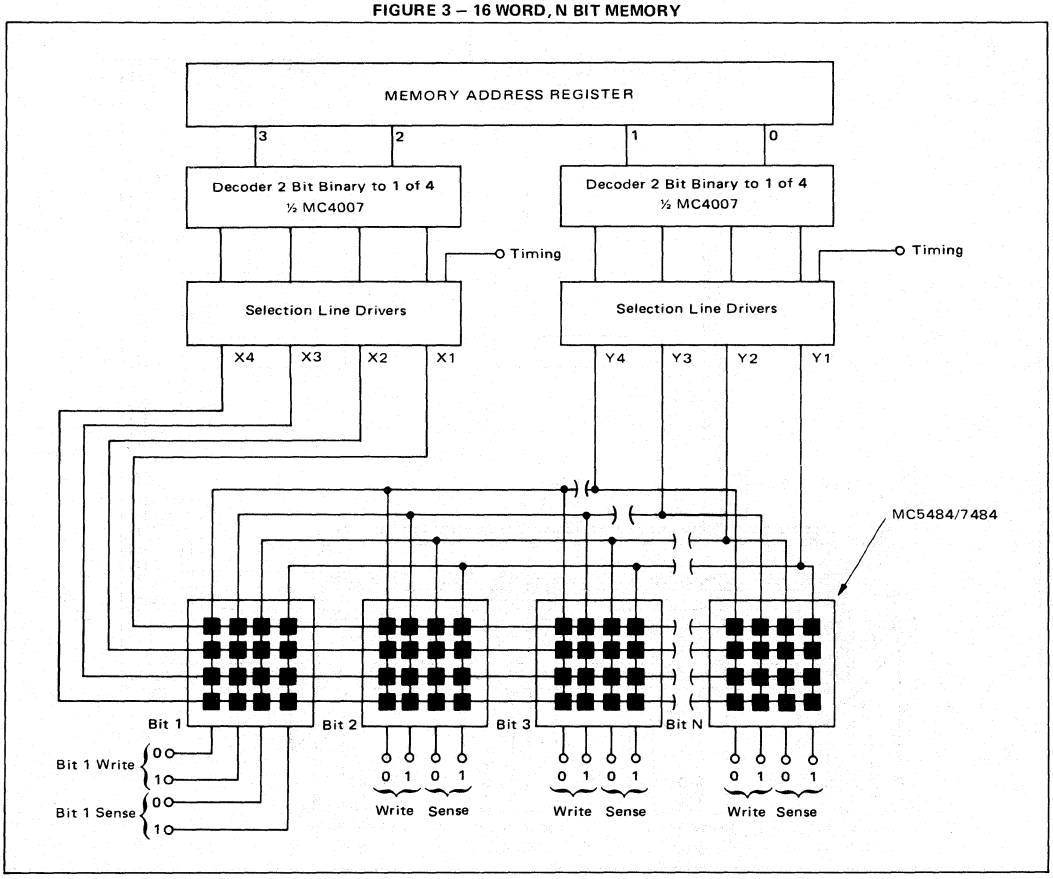
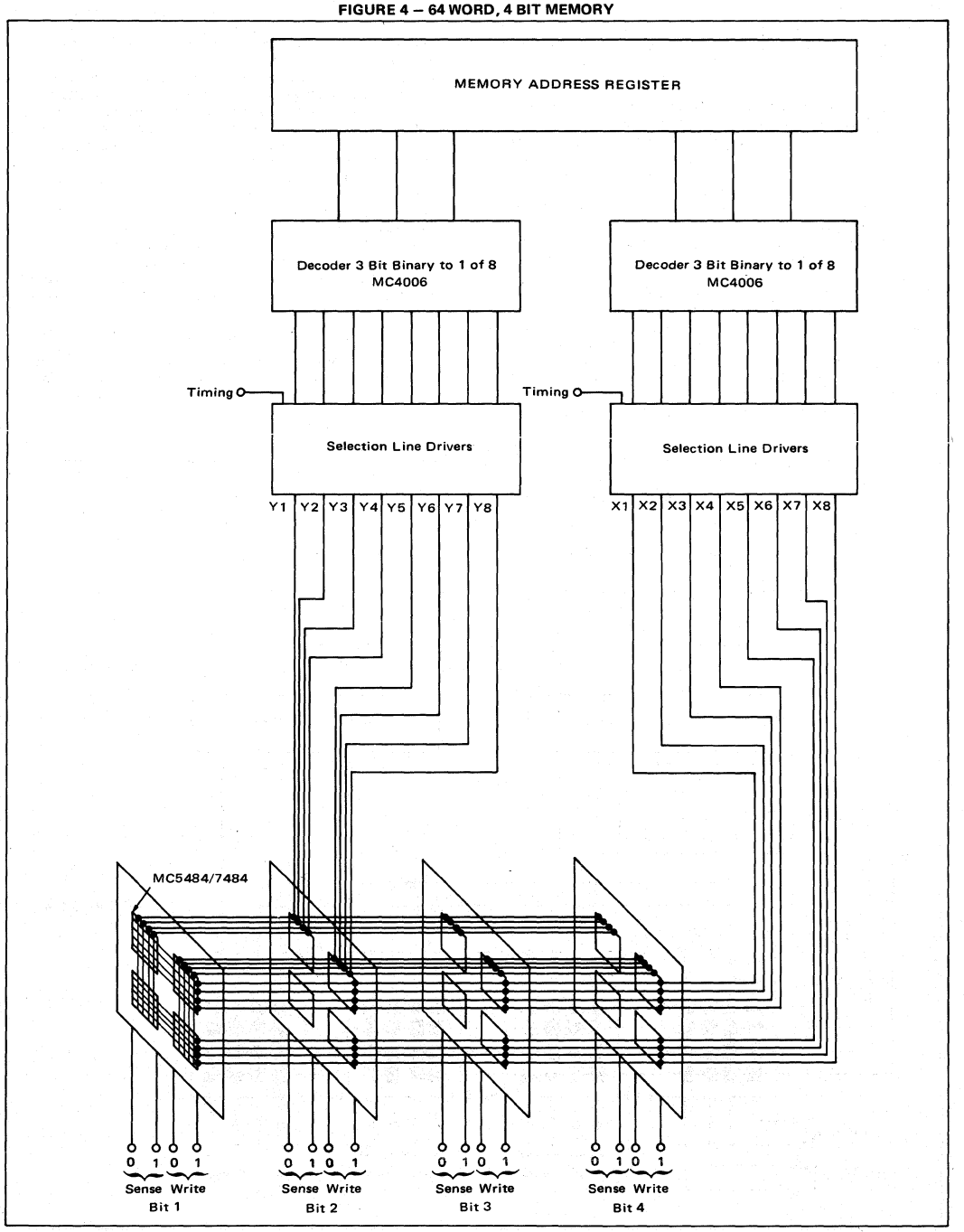


FIGURE 4 – 64 WORD, 4 BIT MEMORY



MCM4002

256-BIT READ ONLY MEMORY

The MCM4002 is a monolithic 256-bit Read Only Memory (ROM) that can be programmed for custom requirements. The basic organization of the memory is 32 eight-bit words, with each bit initially in the logic "0" storage state established by the metal intraconnection. By removing appropriate metal links on the device metalization, these bits can be changed to the logic "1" state to meet specific program requirements.

The MCM4002 also features optional 2.0 kilohm pullup resistors on the eight collector outputs. The open collector output option is obtained by removing metal links to the 2.0 kilohm resistors on the device metalization. Utilizing the open collector option at the buffered output bit lines allows several memories to be "Wire ORed" to form large arrays. In these cases an external pullup resistor must be connected from the open collector outputs to V_{CC}.

The ROM truth table and the pullup/open collector design options are specified by the ordering information on a customer data card as shown in this data sheet. The "scribe-it-yourself" feature allows the design engineer to breadboard his pattern prior to submitting his final design for production by Motorola, thus minimizing costly design errors.

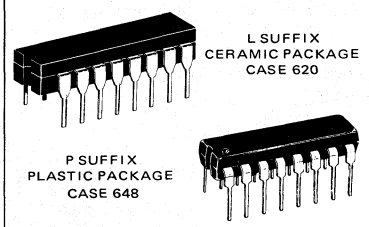
FEATURES:

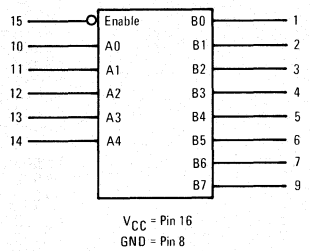
- Positive Logic for Both Inputs and Outputs:
  Logic "0" = Output Device ON (V_{OL})
  Logic "1" = Output Device OFF (V_{OH})
- Logic Levels Compatible with MDTL and All MTTL Families
- Address Times < 50 ns
- Outputs Sink 12 mA Open Collector, 10 mA with Pullup Resistors.
- Configuration allows mechanical programming ("scribe-it-yourself") to verify pattern before processing

APPLICATIONS:

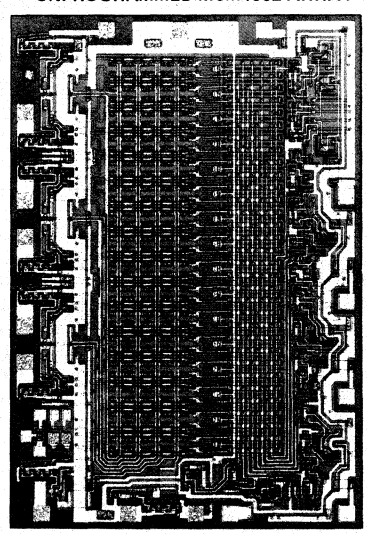
- Look Up Tables
- Micro Programs
- Decode Functions
- Code Conversion
- Number Conversion
- Random Logic
- Character Generation

256-BIT
READ ONLY MEMORY





UNPROGRAMMED MCM4002 ARRAY



DESIGNING A CUSTOM FUNCTION FROM THE MCM4002 READ ONLY MEMORY

A custom function may be designed with the MCM4002 by defining whether metalization links on the memory array should be removed or left in place. The memory is originally programmed with logic "0's" and with 2.0 kilohm pullup resistors on the collector outputs. Logic "1's" may be programmed into the array by removing metalization links from the pattern. Open collectors may also be programmed into the array by similar means. The following procedure is suggested for obtaining the final, correct design.

1. Define the required truth table, using the format shown in Figure 1.
2. Select the output option desired: either 2.0 kilohm pullup resistors, or open collectors.
3. Scribe the pattern into the breadboard device.

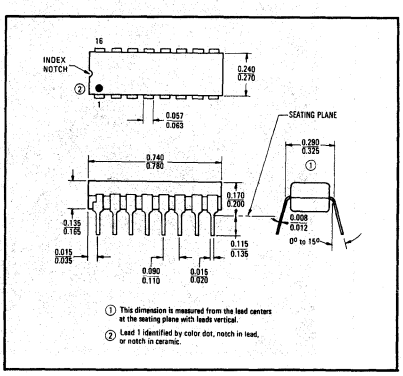
   Method A: Purchase lidless device from Motorola and "scribe-it-yourself." Use Figures 2 and 3 as a guide to placement of the metalization links.

   Method B: Purchase custom-scribed lidless device from Motorola or selected Motorola franchised distributors.
4. Order custom function for production by following ordering information on this data sheet.

FIGURE 1 – TRUTH TABLE FORMAT

	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
WORD 0								
WORD 1								
WORD 2								
WORD 3								
WORD 4								
WORD 5								
WORD 6								
WORD 7								
WORD 8								
WORD 9								
WORD 10								
WORD 11								
WORD 12								
WORD 13								
WORD 14								
WORD 15								
WORD 16								
WORD 17								
WORD 18								
WORD 19								
WORD 20								
WORD 21								
WORD 22								
WORD 23								
WORD 24								
WORD 25								
WORD 26								
WORD 27								
WORD 28								
WORD 29								
WORD 30								
WORD 31								

L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

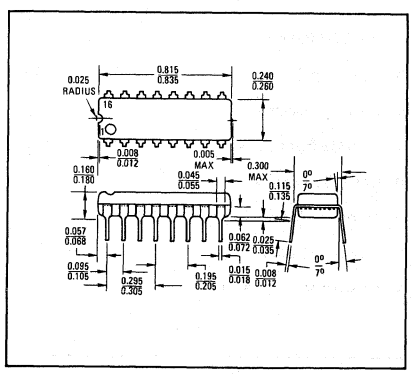
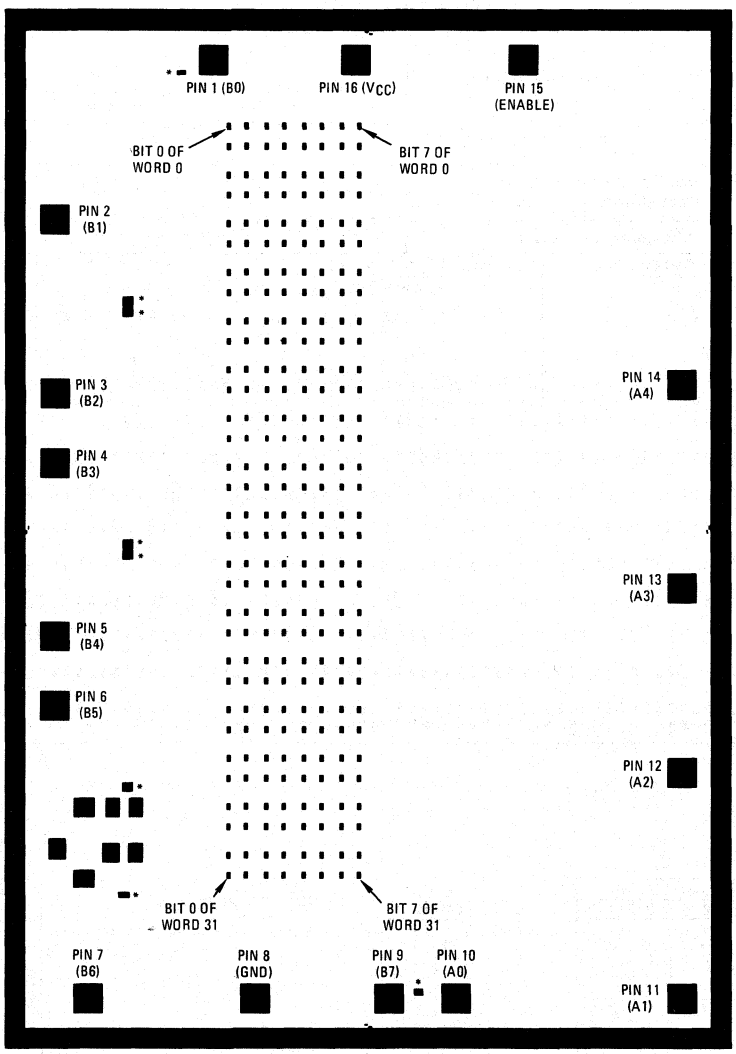


FIGURE 2 – PASSIVATION MASK

The passivation mask indicates not only the positioning of the metalization links for the ROM, but also defines bonding pads and pullup resistor links. This figure, with Figure 1, should be used to determine links to be removed in programming the memory.

Outputs must be specified as having either all pullup resistors or all open collectors. Pullup resistor and open collector options cannot be mixed on an individual chip.



*Metalization links which connect optional 2.0 kilohm pullup resistors to outputs.

ORDERING INFORMATION

After the memory bit pattern is established by the user, the information is transmitted to Motorola by supplying punched cards (rectangular punched holes) as described in Figure 3. Figure 4 explains how truth table information is converted from the binary bit pattern to the hexadecimal numbering system. This is done to accommodate most computer equipment presently in use for best user-supplier interfacing and to obtain standard Hollerith punch throughout the card.

The punched card provides the mask-making instructions utilizing Computer-Aided Design Techniques. This card accompanies the manufactured parts to the Final Test and Quality Control areas. Motorola's automatic testing facility compares the function of the completed memory circuits with the program specified on the card, and tests the input-output electrical characteristics.

FIGURE 3 – PUNCHED CARD FORMAT

Two cards are required: card 01 defines words 0 thru 15, card 02 defines words 16 thru 31.

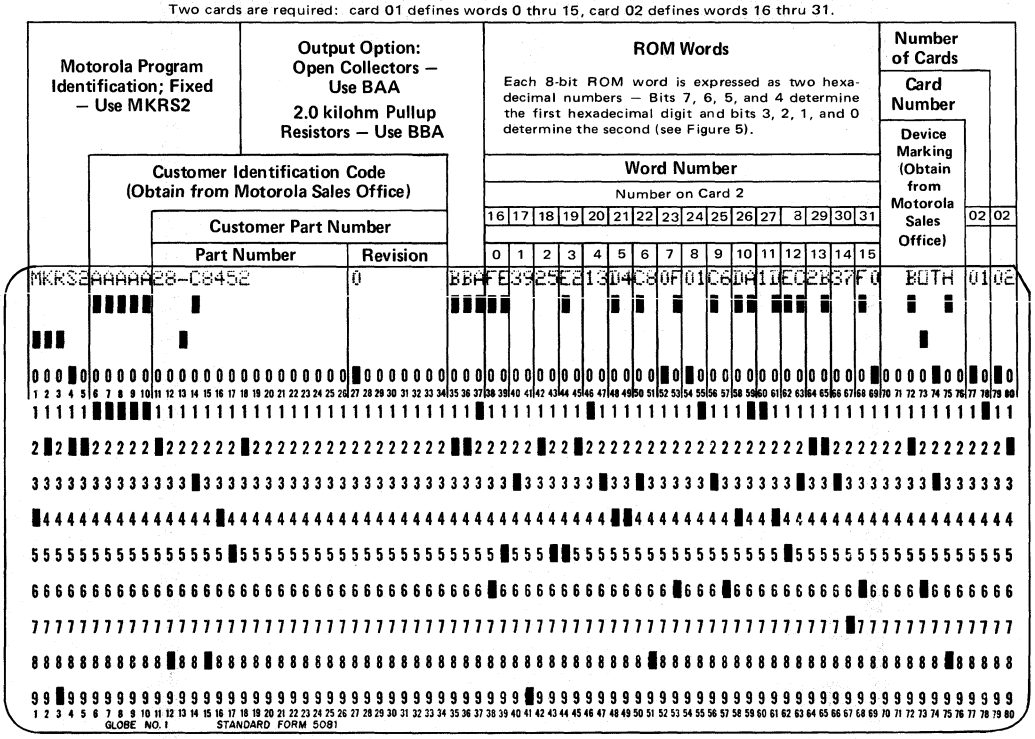


FIGURE 4 – ROM WORD PROGRAMMING FORMAT FOR PUNCHED CARD

	INPUT (A) 4 3 2 1 0	OUTPUT (B) 7 6 5 4 3 2 1 0	CARD COLUMN
Word 0	0 0 0 0 0	1 1 1 1 1 1 1 0	38 and 39
1	0 0 0 0 1	0 0 1 1 1 0 0 1	40 and 41
2	0 0 0 1 0	0 0 1 0 0 1 0 1	42 and 43
3	0 0 0 1 1	1 1 1 0 0 0 1 0	44 and 45
4	0 0 1 0 0	0 0 0 1 0 0 1 1	46 and 47
5	0 0 1 0 1	1 1 0 1 0 1 0 0	48 and 49
6	0 0 1 1 0	1 1 0 0 1 0 0 0	50 and 51
7	0 0 1 1 1	0 0 0 0 1 1 1 1	52 and 53
8	0 1 0 0 0	0 0 0 0 0 0 0 1	54 and 55
9	0 1 0 0 1	1 1 0 0 0 1 1 0	56 and 57
10	0 1 0 1 0	1 1 0 1 1 0 1 0	58 and 59
11	0 1 0 1 1	0 0 0 1 1 1 0 1	60 and 61
12	0 1 1 0 0	1 1 1 0 1 1 0 0	62 and 63
13	0 1 1 0 1	0 0 1 0 1 0 1 1	64 and 65
14	0 1 1 1 0	0 0 1 1 0 1 1 1	66 and 67
15	0 1 1 1 1	1 1 1 1 0 0 0 0	68 and 69

→ Transfer to CARD COLUMN

COL 38 COL 39 (~~ ~~)

as F and E (1111 1110) using conversion table

Note: Words 16 thru 31 transfer to card 02 in the same manner.

BINARY TO HEXADECIMAL CONVERSION TABLE

BINARY DATA	CARD CHARACTER
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

MCM4002 (continued)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{in}	-1.5 to +5.5	Vdc
Output Voltage (Open Collectors)	V_{OH}	-0.5 to +7.0	Vdc
Operating Temperature Range			
Plastic Package	T_A	0 to +75	°C
Thermal Resistance, Junction to Ambient (Typical)	θ_{JA}	200	°C/W
Ceramic Package	T_A	-55 to +125	°C
Thermal Resistance, Junction to Ambient (Typical)	θ_{JA}	95	°C/W
Storage Temperature	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS (Plastic Package, T_A = 0°C to 75°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Input Forward Current (V_{in} = 0.4 Vdc, V_{CC} = 5.25 Vdc)		I_F	–	1.6	mAdc
Input Leakage Current (V_{in} = 4.5 Vdc, V_{CC} = 5.25 Vdc)		I_R	–	100	μAdc
Logic "0" Output Voltage		V_{OL}			Vdc
(I_O = 12 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 0.8 Vdc, V_{CC} = 4.75 Vdc)	Open Collectors		–	0.45	
(I_O = 10 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 0.8 Vdc, V_{CC} = 4.75 Vdc)	Pullup Resistors		–	0.45	
Logic "1" Output Voltage (I_{OH} = -0.5 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 2.0 Vdc, V_{CC} = 5.25 Vdc)	Pullup Resistors	V_{OH}	2.5	–	Vdc
Output Leakage Current (V_{out} = 5.25 Vdc, V_{Enable} = 2.0 Vdc, V_{CC} = 5.25 Vdc)	Open Collectors	I_{CEX}	–	200	μAdc
Power Supply Drain Current		I_{CC}			mAdc
(Memory Enabled, V_{Enable} = 0 Vdc, Other Inputs = 0 Vdc, V_{CC} = 5.25 Vdc)	Open Collectors		–	80	
	Pullup Resistors		–	95	
(Memory Disabled, V_{Enable} = 2.0 Vdc, Other Inputs = 0 Vdc, V_{CC} = 5.25 Vdc)			–	65	

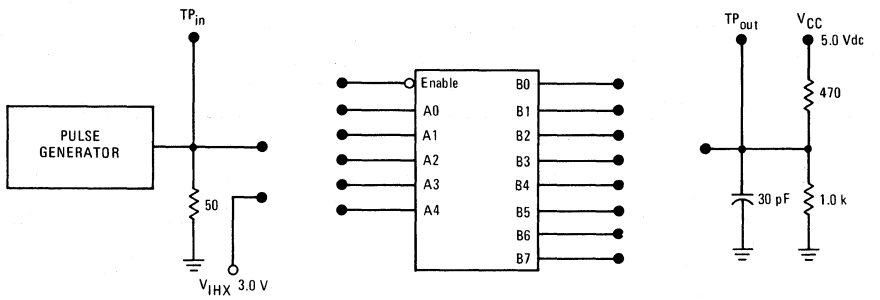
ELECTRICAL CHARACTERISTICS (Ceramic Package, T_A = -55°C to +125°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Input Forward Current (V_{in} = 0.4 Vdc, V_{CC} = 5.5 Vdc)		I_F	–	1.6	mAdc
Input Leakage Current (V_{in} = 4.5 Vdc, V_{CC} = 5.5 Vdc)		I_R	–	100	μAdc
Logic "0" Output Voltage		V_{OL}			Vdc
(I_O = 12 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 0.8 Vdc, V_{CC} = 4.5 Vdc)	Open Collectors		–	0.45	
(I_O = 10 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 0.8 Vdc, V_{CC} = 4.5 Vdc)	Pullup Resistors		–	0.45	
Logic "1" Output Voltage (I_{OH} = -0.5 mAdc, V_{IL} = 0.8 Vdc, V_{IH} = 2.0 Vdc, V_{Enable} = 2.0 Vdc, V_{CC} = 5.5 Vdc)	Pullup Resistors	V_{OH}	2.5	–	Vdc
Output Leakage Current (V_{out} = 5.5 Vdc, V_{Enable} = 2.0 Vdc, V_{CC} = 5.5 Vdc)	Open Collectors	I_{CEX}	–	200	μAdc
Power Supply Drain Current		I_{CC}			mAdc
(Memory Enabled, V_{Enable} = 0 Vdc, Other Inputs = 0 Vdc, V_{CC} = 5.5 Vdc)	Open Collectors		–	80	
	Pullup Resistors		–	95	
(Memory Disabled, V_{Enable} = 2.0 Vdc, Other Inputs = 0 Vdc, V_{CC} = 5.5 Vdc)			–	65	

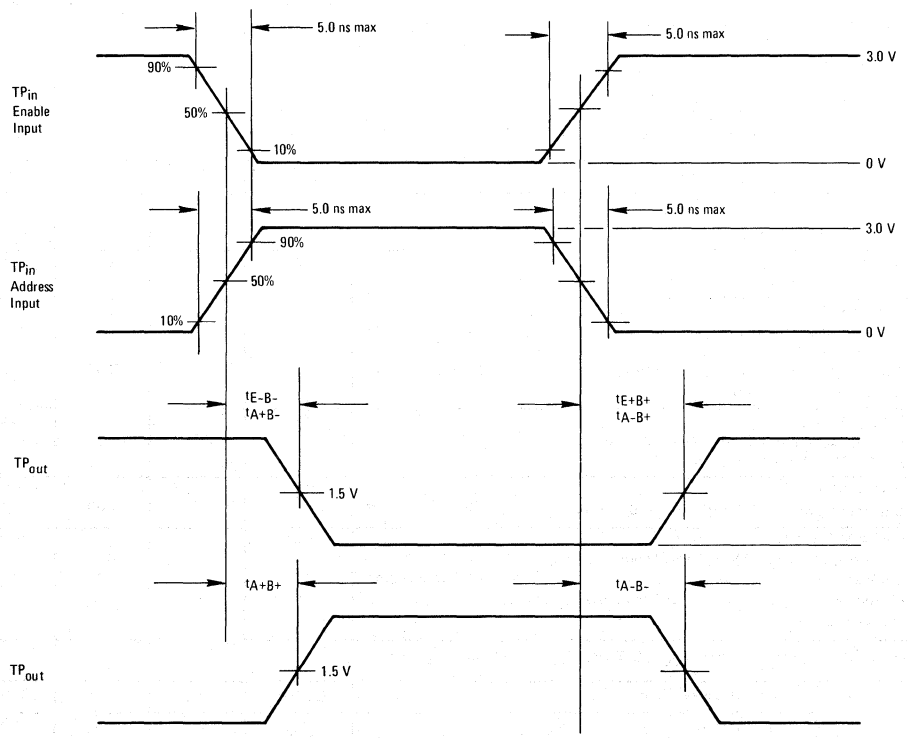
SWITCHING TIMES (Both Packages, V_{CC} = 5.0 Vdc, T_A = 25°C) (see Figure 5)

Enable Input	Turn-Off Delay Time	t_{E+B+}	–	50	ns
	Turn-On Delay Time	t_{E-B-}	–	50	ns
Address Input	Turn-Off Delay Time	t_{A+B+} or t_{A-B+}	–	50	ns
	Turn-On Delay Time	t_{A+B-} or t_{A-B-}	–	50	ns

FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Enable Input Test: Connect data inputs to V_{IHX}.
Address Input Test: Inputs not under test left open.
High impedance probes must be used when making these measurements.



MCM4064AL
MCM4064L

Advance Information / New Product

64-BIT RANDOM ACCESS MEMORY

The MCM4064AL/4064L is a 64-Bit random access memory organized as a 16-word by 4-bit array. Schottky-diode-clamped transistors are utilized to obtain fast switching speeds, and Schottky clamp diodes are used on all inputs to provide minimum line reflection. The high speed of this memory makes it ideal in scratch pad operation.

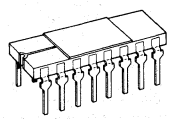
Address decoding is incorporated in the circuit providing 1-of-16 decoding from the four address lines. Separate Data In and Data Out lines, together with a Chip Enable, provide for easy expansion of memory capacity. A Write Enable is provided to enable data presented at the Data In lines to be entered at the addressed storage cells. When writing, Data Out is the complement of the Data In.

The open-collector output transistors are also Schottky barrier devices and combine greater current sinking capability with lower leakage currents, thereby increasing the wire-or capability of these devices.

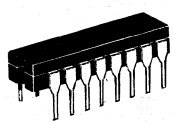
Features:

- Both Minimum and Maximum Access Times Specified
- Binary Addressing
- Chip Enable for Memory Expansion
- Outputs May Be "Wire ORed"
- Logic Levels Compatible with MDTL and All MTTL Families
- Low-Voltage Input Clamp Diodes
- Access Time < 60 ns
- Power Dissipation Typically 6 mW/bit
- Outputs Sink 15 mA

MTTL
64-BIT
RANDOM ACCESS
MEMORY



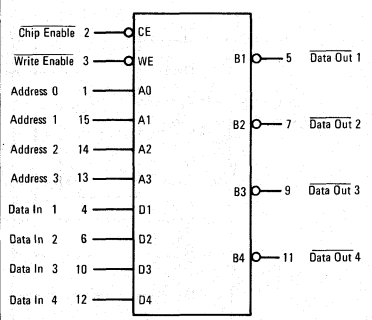
MCM4064AL
CASE 638



MCM4064L
CASE 620

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage – All Inputs	V_{in}	5.5	Vdc
Output Voltage – All Outputs	V_D	5.5	Vdc
Output Current	I_D	100	mAdc
Operating Temperature Range			
MCM4064AL (Case 638)	T_A	0 to +85	°C
Thermal Resistance, Junction to Ambient (Typical)	θ_{JA}	80	°C/W
Thermal Resistance, Junction to Case (Typical)	θ_{JC}	45	°C/W
MCM4064L (Case 620)	T_A	0 to +70	°C
Thermal Resistance, Junction to Ambient (Typical)	θ_{JA}	110	°C/W
Thermal Resistance, Junction to Case (Typical)	θ_{JC}	60	°C/W
Storage Temperature Range	T_{stg}	-65 to +160	°C



V_{CC} = Pin 16
GND = Pin 8

DC ELECTRICAL CHARACTERISTICS (MCM4064AL: (T_A = 0 to +85°C, Case 638; MCM4064L: T_A = 0 to +70°C, Case 620)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Forward Current — All Inputs (V_{IL} = 0.4 Vdc, V_{CC} = 5.25 Vdc)	I_F	–	–	1.6	mAdc
Input Leakage Current — All Inputs (V_{IH} = V_{CC} = 5.25 Vdc)	I_R	–	–	80	μAdc
Input Clamp Voltage — All Inputs (I_{in} = -5.0 mAdc, V_{CC} = 4.75 Vdc)	V_C	–	–	-1.0	Vdc
Input Logic Levels — All Inputs (V_{CC} = 5.0 Vdc) "0" Level	V_{IL}	–	–	0.8	Vdc
"1" Level	V_{IH}	2.0	–	–	
Logic "0" Output Voltage — All Outputs (V_{CC} = 4.75 Vdc, I_{OL} = 15 mAdc)	V_{OL}	–	–	0.45	Vdc
Output Leakage Current — All Outputs (V_{CC} = V_{CEX} = 5.25 Vdc)	I_{CEX}	–	–	100	μAdc
Power Supply Current (V_{CC} = 5.25 Vdc, all inputs except WE grounded)*	I_{CC}	–	–	105	mAdc
Input Capacitance — All Inputs (V_{in} = 2.0 Vdc, V_{CC} = 5.0 Vdc)	C_{in}	–	6.0	–	pF
Output Capacitance — All Outputs (V_{out} = 2.0 Vdc, V_{CC} = 5.0 Vdc)	C_{out}	–	8.0	–	pF

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Access Times — Address Input or Chip Enable to Output Delay. (See Figures 1 and 2)	t_{A+B+}	15	–	60	ns
	t_{A-B-}	15	–	60	
	t_{A+B-}	15	–	60	
	t_{A-B+}	15	–	60	
	t_{CE+B+}	15	–	60	
	t_{CE-B-}	15	–	60	
Write Pulse Width (See Figures 1 and 3)	t_{wp}	40	–	–	ns
Write Recovery Time (See Figures 1 and 3)	t_{wr}	–	–	50	ns
Address and Data Hold Time After Write (See Figures 1 and 3)	t_{HAW}	5.0	–	–	ns

*Worst-case dc input condition.

BLOCK DIAGRAM

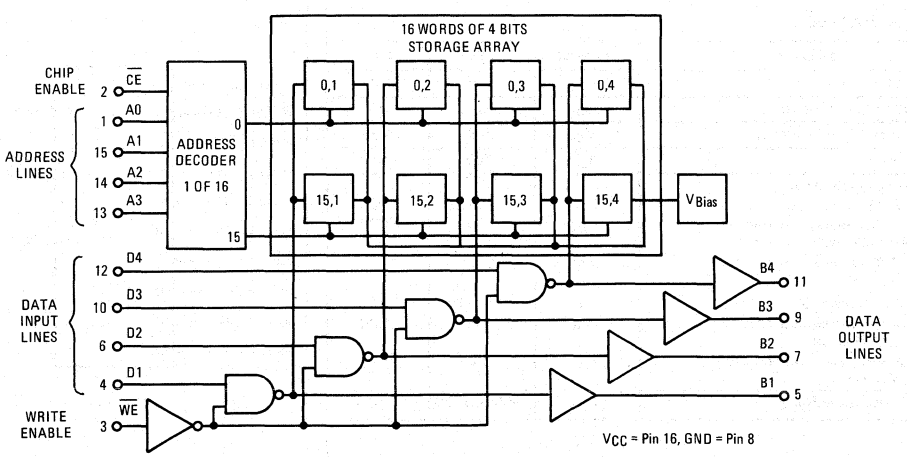


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FIGURE 1 – SWITCHING TIME TEST CONDITIONS AND LOAD CIRCUIT

V_{CC} = 5.0 Vdc, T_A = 25°C

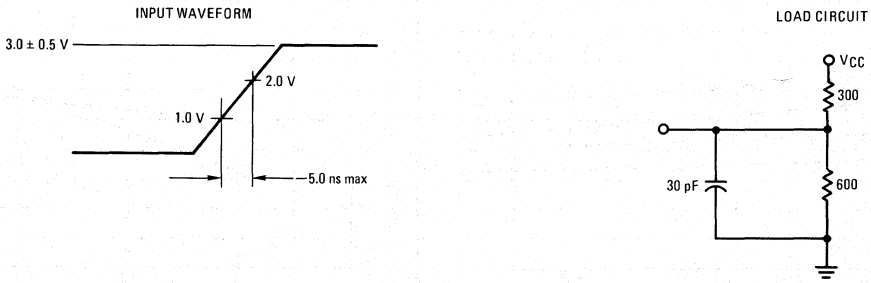
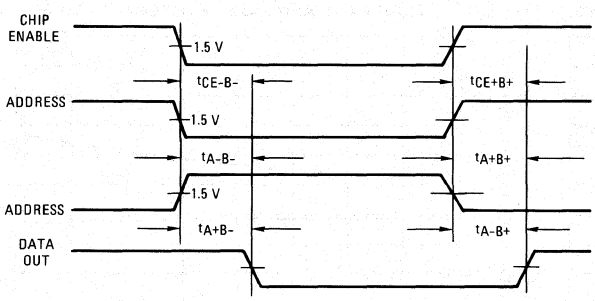


FIGURE 2 – ACCESS TIME DEFINITIONS



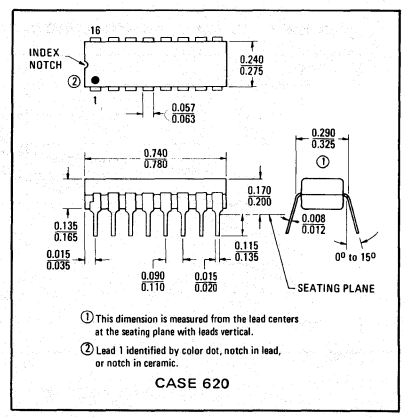
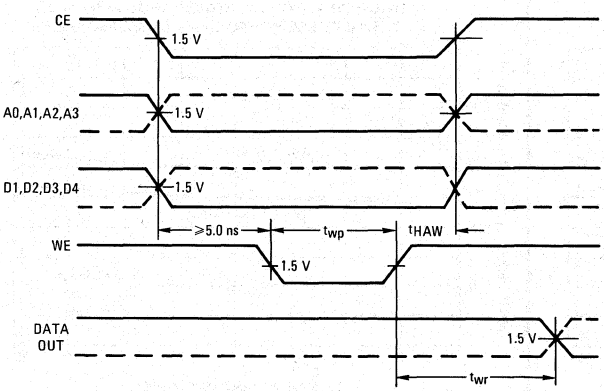
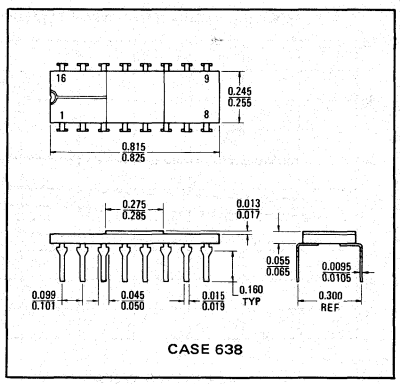


FIGURE 3 – WRITE TIME DEFINITIONS





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TYPICAL ACCESS TIMES

ADDRESS TO OUTPUT

FIGURE 4 – VARIATIONS WITH SUPPLY VOLTAGE

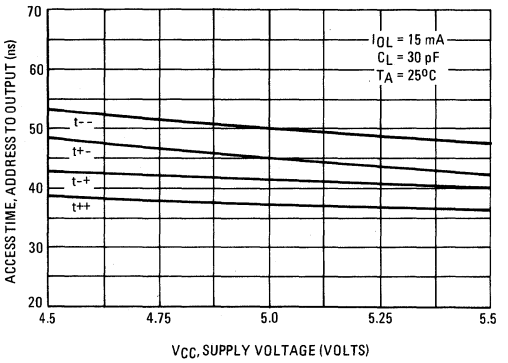


FIGURE 5 – VARIATIONS WITH LOAD CAPACITANCE

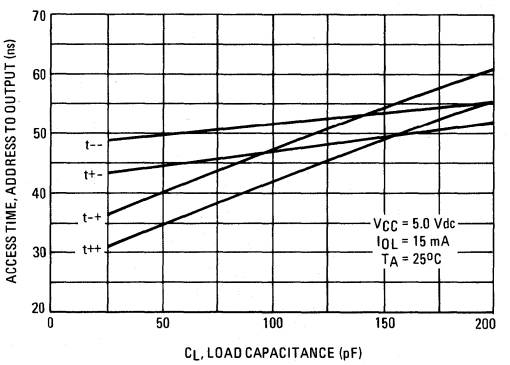
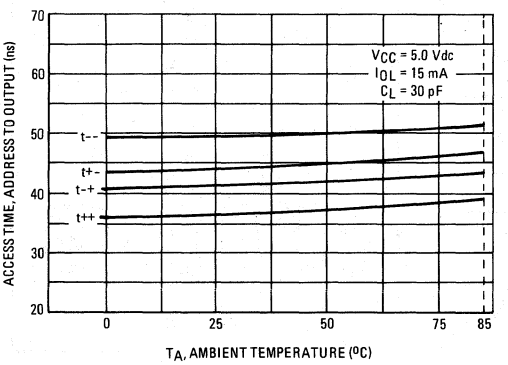


FIGURE 6 – VARIATIONS WITH TEMPERATURE



CHIP ENABLE TO OUTPUT

FIGURE 7 – VARIATIONS WITH LOAD CAPACITANCE

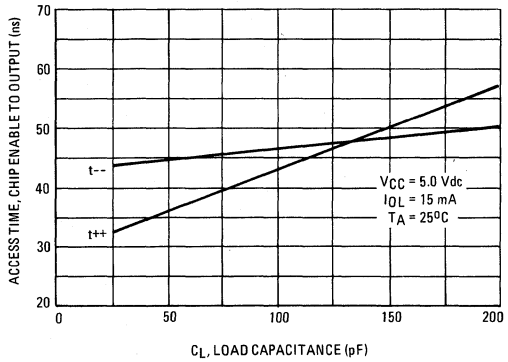


FIGURE 8 – VARIATIONS WITH TEMPERATURE

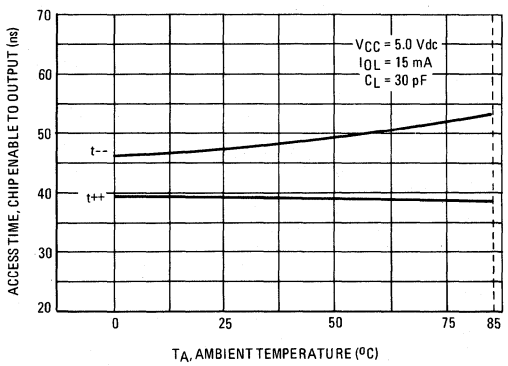
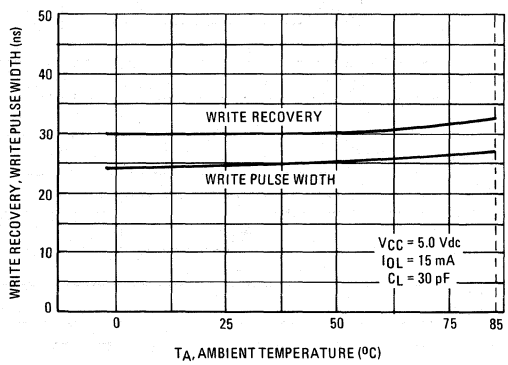


FIGURE 9 – TYPICAL WRITE RECOVERY AND WRITE PULSE WIDTH versus TEMPERATURE



TYPICAL DC CHARACTERISTICS

FIGURE 10 – TYPICAL SUPPLY CURRENT versus TEMPERATURE

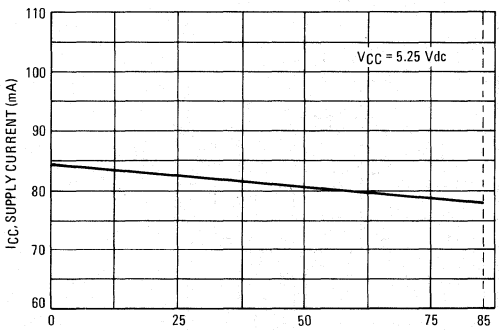
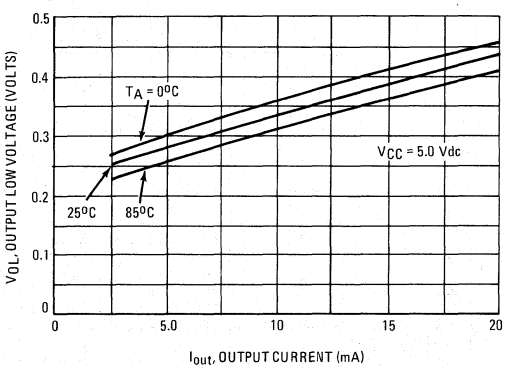


FIGURE 11 – TYPICAL OUTPUT LOW VOLTAGE versus OUTPUT CURRENT



APPLICATIONS INFORMATION

The MCM4064 64-bit MTTL RAM has several features which should be considered when designing larger systems with this device.

1. Chip Enable – This input essentially turns off the device when in the high state. The chip will neither read out nor write in data when disenabled. The open collector output devices allow Wire ORing or phantom logic for expansion into larger systems. Graphs in this data sheet show the relationship between access time and capacitance on the output due to Wire ORing.

2. Write Enable – The $\overline{WE}$ input gates the data on the data input leads into the memory cells. The output amplifiers are tied directly to the write amplifiers and follow as the inverse of the input for either state of $\overline{CE}$ as long as $\overline{WE}$ is low. There is, however, a "glitch" on the output lines just after $\overline{WE}$ returns high or goes low. For proper writing into the memory, the address and data hold time after writing (t_{HAW}) must be greater than 5.0 ns.

3. The address inputs have standard TTL-compatible input thresholds and standard TTL loading rules can be used.

The data outputs have open-collector, Schottky-clamped transistors and can be wire ORed with the incumbent cost in propagation delay. Typical output capacitance is specified for aid in system design.

Figure 12 shows a typical system design using TTL logic and the MCM4064 as a main frame store. This figure will be used to discuss several design considerations.

The four address inputs of the MCM4064 are common to all devices in the system. The gates driving these addresses have a fanout of eight, which is a typical and reasonable TTL fanout. In the diagram, each address driver shown represents four devices, one for each address. Thus, 8 x 4 or 32 inverters are required for address driving.

The chip enable inputs are used for further address expansion and a one-of-eight decoder (MC4006) is used for selecting one chip of eight with Wired OR outputs. Again a TTL fanout of eight is used. This chip enable decodings adds three address bits, A5, A6 and A7.

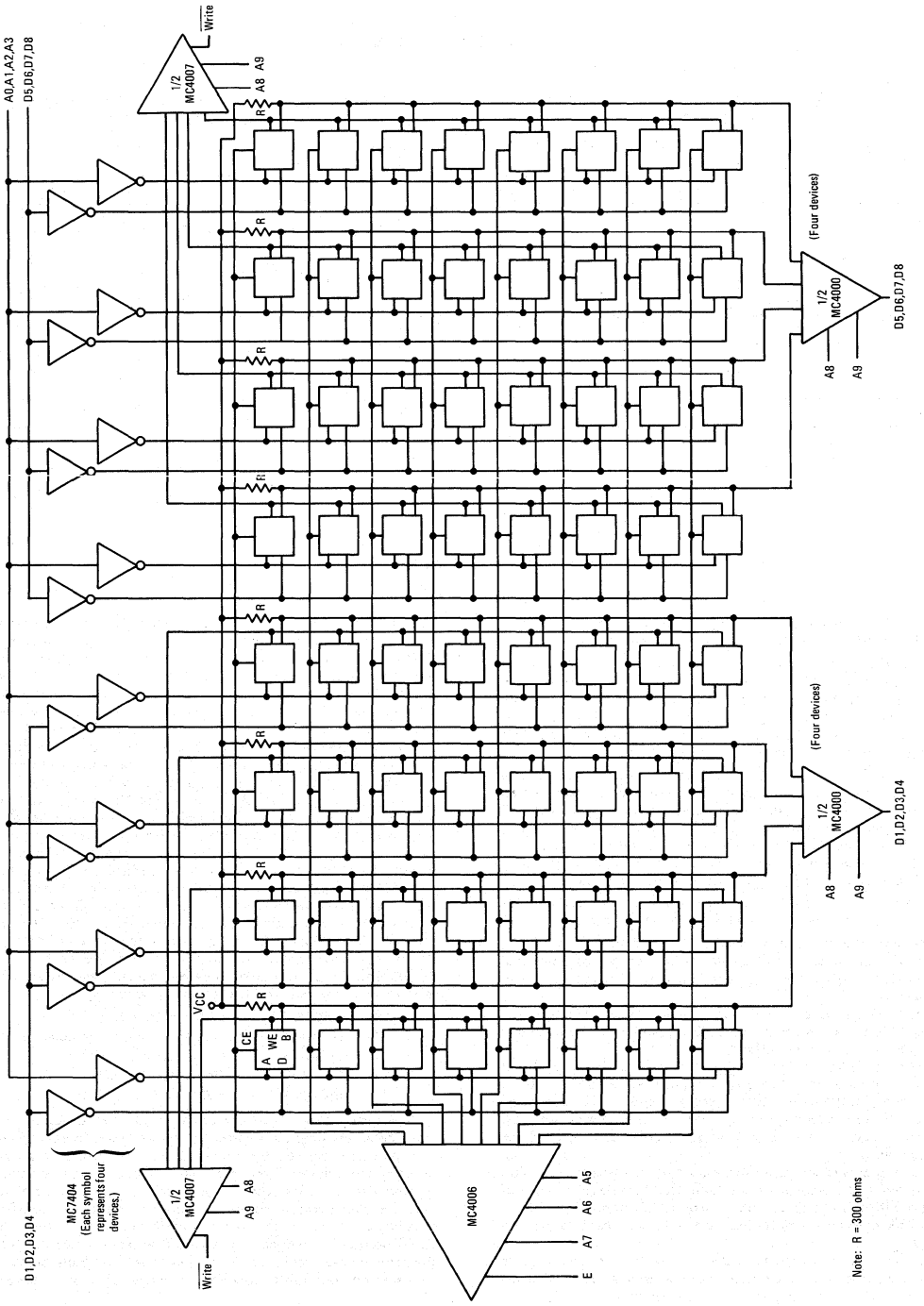
The memory chips are Wire-ORed in sections of eight. This figure of eight is used as a trade-off in decoding array time versus increase in access time due to output capacitance. The eight outputs at 8.0 pF each, plus an average of 5.0 pF for board capacitance give a total of slightly more than 100 pF for a total typical access time (from Figure 5) of about 50 ns. Each section of eight memory chips is connected to a one-of-four data selector (MC4000) which selects one of four sections. This adds a further two address bits, A8 and A9, for a total of 512 address locations. A one-of-four decoder is required for each data output and eight selectors, or four MC4000 devices, are required for the system. Four selectors give output bits D1 through D4 and the second set provides D5 through D8 from a second 8 x 4 array of memory devices.

The input data drivers shown in Figure 12 also represent four inverters, one for each data input bit, in the same manner as the address drivers and output selectors. The input data is distributed in common to both 8 x 4 memory arrays. The particular column of eight MCM4064's for which the data is intended is selected by the MC4007 data selectors which drive the write enable inputs. Only one of the eight MCM4064's in the columns will actually write in this data and is selected by the chip enable input. Thus only one device in the 8 x 4 array will actually accept the input data: that device chosen by the coincidence of the $\overline{CE}$ and $\overline{WE}$ lines.

The entire system shown, therefore, constitutes a 512-word by 8-bit memory and requires the following devices:

64	MCM4064	64 bit memories
4	MC4000	One-of-four data selectors
1	MC4006	One-of-eight decoders
1	MC4007	One-of-four decoders
11	MC7404	Hex inverters

The system access time is the total of the input decoding times, memory access times, and output selection delay times. However, this may be decreased for read-read cycles by utilizing the maximum and minimum access times. Thus, if one changes the address or chip enable inputs every 60 ns, there is at least 15 ns of valid data on the memory output. Therefore, an output buffering scheme which can latch up the memory contents within 15 ns could be used to reduce the read-read access time to 60 ns plus the address/chip enable skew times which are invariably present. A similar technique could be used for read-write and write-write cycles.


A0,A1,A2,A3
D5,D6,D7,D8
Write
1/2 MC4007
A8 A9
R
(Four devices)
1/2 MC4000
D5,D6,D7,D8
A8
A9
D1,D2,D3,D4
VCC
CE
WE
A
D
B
MC7404
(Each symbol represents four devices.)
MC4006
A5
A6
A7
E
Note: R = 300 ohms

APPLICATION NOTE ABSTRACTS

The application notes listed in this section have been prepared to acquaint the circuits and systems engineer with Motorola TTL integrated circuits and their applications. To obtain copies of the notes, simply list the AN number or numbers and send your request on your company letterhead to: Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20924, Phoenix, Arizona 85036.

AN-464 MTTL Designer's Note — The MC4004/ MC4005, A 16-Bit Random Access Memory

High speed, non-destructive readout (NDRO) memory systems can be constructed with the MTTL 16-bit memory chip. Information concerning the chip that is pertinent to the design of a complete memory system is herein presented. The topics discussed are: (1) operation of the 16-bit memory including typical read and write sequences, (2) typical dc and switching characteristics as a function of temperature, power supply, and output load, and (3) examples of memory system organization utilizing the 16-bit memory as the basic cell.

AN-465 MTTL Designer's Note — The MC4006/ MC4007 Decoders

Two MTTL complex functions, the MC4006 Binary to One-of-Eight Decoder and the MC4007 Dual Binary to One-of-Four Decoder are discussed. Their basic modes of operation and expansion capabilities are described. Examples of the use of the decoders in various systems are presented.

AN-476 MTTL Designer's Note — The MC4000 Data Selector and the MC4002 Data Distributor

Two MTTL complex functions, the MC4002 four and two-channel data distributor, and the MC4000 dual four-channel data selector are discussed. Their basic modes of operation and expansion capabilities are described. Examples of the use of the data distributor and the data selector in various systems are presented.

AN-488 High-Speed Addition Using Lookahead Carry Techniques

The use of the lookahead carry principle to increase the operating speed of adder systems is described. Several adders of different sizes using variations of lookahead carry are developed and the logical implementation of these using the MTTL III and MECL II and III logic families is given.

AN-492 Operating Characteristics of Motorola MC3000/MC3100 Series Transistor-Transistor Logic Gates

This application note explains the advantages of using the MC3000/MC3100 Series of conventional TTL. Design data is included which should allow determination of the operating characteristics under almost any set of conditions.

AN-493 The MC3000/MC3100 Series Transistor-Transistor Logic Flip-Flops

This application note explains the basic operation of the various flip-flops available in the MC3000/MC3100 series of transistor-transistor logic from Motorola. Typical operating characteristics are included so that operation under different conditions can be determined.

AN-494 The Motorola Transistor-Transistor Logic Lines

This application note contains a general description and comparison of Motorola's MTTL I, MTTL II, MTTL III, MTTL 5400/7400, and the MC4000 lines. The basic gate and the MTTL III bypass circuit are discussed and tables of electrical characteristics are included. Two appendices provide definitions of common MTTL terms, a discussion of the effect of input diodes, and loading rules for the MC4000 series complex functions.

AN-496 Error Detection and Correction Using Exclusive OR Gates and Parity Trees

The availability of Exclusive OR gates and parity trees allows digital system designers to use error detection and correction codes to improve their system reliability and maintainability without the major cost penalty that has existed in the past. Use of Exclusive-OR gates and parity trees available in the MRTL, MTTL, MDTL, and MECL families to design simple parity and single error Hamming parity detection and correction circuits is discussed.

AN-505 The MC4012, An MTTL 4-Bit Shift Register

The MC4012 is a 4-bit shift register consisting of four D-type flip-flops operated in the synchronous mode and may be used for temporary storage of information. The MC4012 may be operated in either the parallel or serial mode input depending upon the logic state of the mode control. Circuit operation and various applications of the device are the subject of this application note.

AN-516 Direct Digital Display Using MTTL Complex Functions

This application note examines some of the different design methods for digital readouts with the added circuitry advantage of integrated circuit complex functions; in particular the MC5400/7400 series.

AN-528 Binary-To-BCD-To-Binary Conversion With Complex IC Functions

Complex function integrated circuits reduce the cost of performing conversion from binary to the BCD code or from the BCD code to binary. Four methods of performing each conversion are discussed and compared.

AN-530A The MC7491A Eight-Bit Serial Shift Register and the MC7495 Four-Bit Shift Register

Operation of the MC5491A/7491A 8-bit shift register and the MC5495/7495 4-bit universal shift register is discussed. Typical applications are covered for each device and use of the two devices in a data transmission system is illustrated.

AN-532 MTTL and MECL Avionics Digital Frequency Synthesizer

This application note discusses several approaches that illustrate applications of complex digital integrated circuits directed toward avionics frequency synthesizers. The techniques presented point out the simplicity with which both MTTL and MECL digital integrated circuits can be used to produce frequency synthesis for avionic communications.

AN-534 Commutating Filter Techniques

This note describes the design and construction of commutating (digital) filters using Motorola MECL II, MTTL III and MC7400 digital integrated circuits. A short section on commutating filter theory is included along with examples of filters and their responses.

AN-535 Phase-Locked Loop Design Fundamentals

The fundamental design concepts for phase locked loops implemented with integrated circuits are outlined. The necessary equations required to evaluate the basic loop performance are given in conjunction with a brief design example.

AN-537 The MC4023, An MTTL 4-Bit Universal Counter

The MC4023 Universal Counter can be connected to count any number from two through twelve except seven and eleven. For all settings, counting is in a binary sequence from count zero to the selected number. Operating characteristics and applications of the device are the subject of this application note.

AN-539 Interfacing With MOS I/C's

This application note discusses the problem of interfacing MOS integrated circuits with the logic levels of MECL, MDTL, MTTL, and MRTL. The emphasis is placed primarily on the use of other integrated circuits to achieve this interfacing.

AN-541 Medium Scale Integration in the Numerical Control Field

Since medium scale integration means complex functions, the logic design engineer must understand both the product and its end use in order that his design be optimized. Transistor-Transistor Logic has a number of devices such as programmable counters, phase detectors, voltage controlled multivibrators, comparators, etc., which are available today in integrated circuit form. The devices can be applied to the numerical controls field and are the subject of this paper.

NOTES

NOTES

TECHNICAL DATA

GENERAL INFORMATION

SELECTOR GUIDES

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