LINEAR INTEGRATED CIRCUITS DATA BOOK

THIRD EDITION

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MOTOROLA Semiconductor Products Inc.

LINEAR
INTEGRATED CIRCUITS DATA BOOK

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Linear Integrated Circuits have achieved a level of maturity which now rivals that of their digital counterparts. In all market categories and for a wide variety of applications functions, linear ICs are serving the needs of equipment manufacturers to reduce cost and improve equipment form, factor and reliability.

They've matured, too, from the standpoint of availability. The number of off-the-shelf linear circuits and their varying capabilities makes them highly useful as building blocks for system design. Moreover, the now-prevalent practice of second sourcing assures competitive pricing and quantity delivery.

The Motorola Semiconductor Products Division has been in the forefront of linear IC development since the inception of integrated circuit technology. This Linear Integrated Circuit Data Book, therefore, contains data sheets for one of the largest selections of linear ICs in the industry. Included are devices that were developed by the various Motorola R&D groups, as well as an extensive second-source inventory of the most popular circuits developed elsewhere.

For easy reference, the data sheets in this book are in alpha-numeric sequence, without regard as to product category or applications. However, to provide the user with a quick overview of Motorola's complete line of standard linear ICs, a number of selector guides separate the total line into market and/or functional divisions. This provides a quick comparison of similar devices, spelling out the most significant differences. Also included are a cross-reference table of second-source devices and other product-related information.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of any manufacturer.

Third Edition
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LINEAR INTEGRATED CIRCUITS
MASTER INDEX

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MASTER INDEX (continued)

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MC?

UNDERSTANDING MOTOROLA'S DEVICE NUMBERING SYSTEM

A great deal of information is given in the device number on Motorola ICs. This section will present the meanings of the prefixes, numbers and suffixes used to designate Motorola linear ICs. Normally the package style and operating temperature range may be obtained from the device number.

Although there are exceptions to many of the codes listed below, these codes are generally true and can provide the user with pertinent information on the particular device type.

Prefix

MC	Packaged Integrated Circuits
MCB	Packaged Beam-lead Integrated Circuits. (Followed by F suffix when in flat pack.)
MCBC	Beam-lead Integrated Circuit chips
MCC	Unencapsulated Integrated Circuit chips
MCCF	Flip-Chip Linear Integrated Circuits
MFC	Low cost Integrated Circuits packaged in Motorola's unique "Functional Circuits" plastic package (Package suffix not used in this device series.)
MLM	Pin-for-pin equivalent to Linear Integrated Circuits made by National Semiconductor

Body Number for Motorola Proprietary Devices

1500-1599 3500-3599	Military temperature grade (-55 to +125°C) Linear ICs
1400-1499 3400-3499	Equivalent to devices above but with Industrial temperature range (0 to +70°C)
1300-1399 3300-3399	Linear ICs aimed at the Consumer industry

Suffix

A	Designates improved or modified IC type, followed by package suffix, i.e., MC1489AL.	
C	Designates limited temperature, or limited performance device. Followed by package designation suffix, i.e., MC1709CL	
F	Flat package	Package Designation
G	Metal can package (TO-5 types)	Package Designation
K	Metal power package (TO-3 type)	Package Designation
L	Ceramic dual in-line case (14 or 16 pin)	Package Designation
P	Plastic package	Package Designation
PQ	ICs packaged in staggered-lead plastic DIP packages	Package Designation
P1,P2	Used when an IC is available in more than one plastic package. i.e., P1 = 8 lead plastic DIP, P2 = 14 pin plastic DIP	Package Designation
R	Metal power package (TO-66 type)	Package Designation

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NOTES

LINEAR

INTEGRATED CIRCUITS

HIGHLIGHTS

2

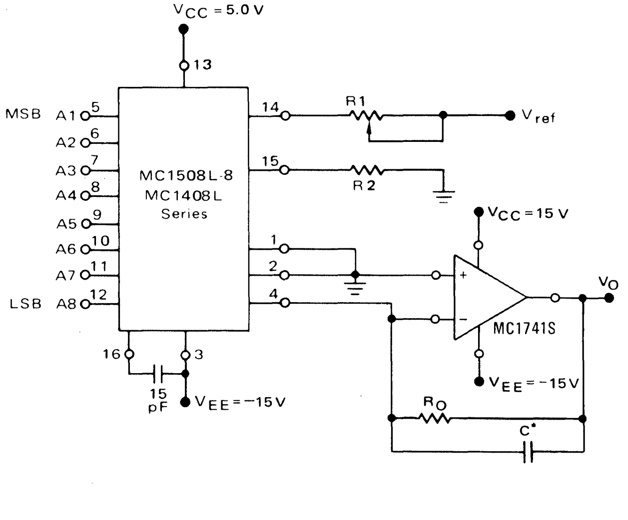
OPERATIONAL AMPLIFIERS

2

The operational amplifier has always been the most popular and versatile Linear IC type. Op amps have found wide usage in control circuitry, signal processing equipment, active filters for communications systems, Modems, and many other types of equipment. With the addition of a few external components, this basic feedback type amplifier can be transformed into a multitude of functions ranging from summing amplifiers and simple inverters to integrating amplifiers and Sample and Hold circuits.

Motorola offers a broad line of op amp types. Both proprietary and popular industry-standard types are covered. The range of high precision to low cost plastic-packaged multiple op amps is spanned by over 50 device types. Two representative devices are discussed here. An overview of the entire line appears on pages 3-2 and 3-3.

HIGH SLEW RATE OPERATIONAL AMPLIFIER



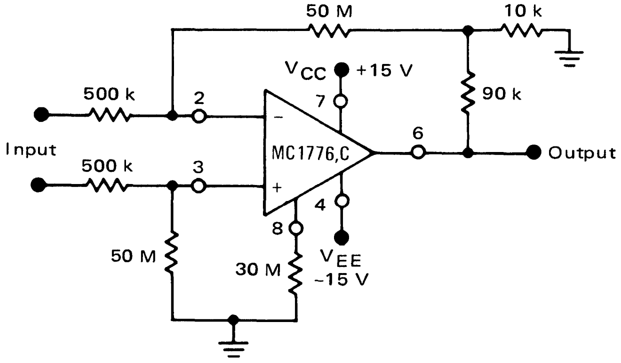
High-Slew Op-Amp (MC1741S)

It is not often that the advantages of the old workhorse can be combined with the speed of the thoroughbred. However, the MC1741S op-amp has done just that; it has all the familiar easy-to-use features of the industry-standard MC1741 internally compensated op-amp. In addition, it offers a guaranteed minimum slew rate of 10 V/μs with a typical slew rate of some 20 times greater than the comparable figure for the conventional MC1741. Power bandwidth has also increased by a factor of 20 and is now specified at 150 kHz minimum.

Applications where pulses are processed or where distortion must be kept low under large-signal conditions are ideal candidates for the MC1741S. Since the unit is a pin-for-pin replacement with all other specs identical to the conventional MC1741, it is easy to update existing designs to improve their performance.

Of particular significance is the 3.0 μs settling time (to 0.1%) of the new device. When combined with an MC1508L digital-to-analog converter, a low-cost, two-package converter with a voltage-mode output and total settling time to within ±1.0 least significant bit of 4.0 μs can be obtained.

PROGRAMMABLE OPERATIONAL AMPLIFIER



Micro-Power, Programmable Op-Amp (MC1776)

The ability to operate with minimal power consumption from a wide range of power supply voltages is the salient feature of the MC1776 programmable op-amp. Whether two 1.2 V mercury cells or supplies up to ±18 V are utilized, the performance features best suited for a particular application can be selected. A single resistor or a current source can be used to set all the quiescent current levels for this circuit. Thus, the designer is free to choose, for example, low bias and power supply currents, or perhaps greater gain-bandwidth and slew rate.

The MC1776 can be combined with McMOS logic to create electronics systems well suited for critical low-drain, battery-powered equipment. The MC1776 uses a maximum of only 120 μW at ±3.0 V and a programming current of 1.5 μA. This assures long life from the battery.

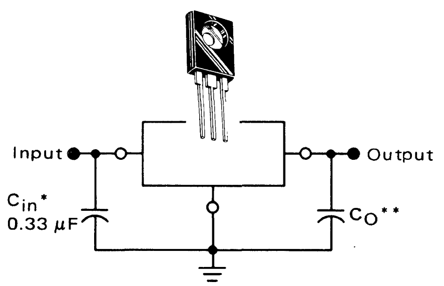
To demonstrate the versitility of the MC1776, all static and dynamic parameters are specified at four combinations of power supply voltages and programming current. Thus, the user is assured that the op-amp will perform over this wide range of operating conditions without having to guess how changes in the programming conditions will affect a particular operating parameter.

For operating flexibility and micropower consumption considerations, the MC1776 is the logical choice.

VOLTAGE REGULATORS

The sensitivity of semiconductor devices to voltage and temperature changes makes the voltage regulator circuit an important integral part of many critical systems and subsystems. Today's designer has considerable choice in integrated regulators, with a variety of characteristics, capabilities, and prices. The integrated circuit voltage regulator offers ease of design, simplified assembly and improved performances over discrete transistor designs. Motorola offers a series of IC voltage regulators with a variety of specifications, see pages 3-12 thru 3-14. Highlighted here are two circuits that merit special attention.

BASIC REGULATOR



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

The Negative Three-Terminal Regulator Complements (MC7900)

The popular MC7800 series voltage regulators described above are all well suited when a positive voltage is required, but they are not intended for negative supplies. For these applications the negative complements, series MC7900 were created. These units are identical to the MC7800 series devices except that the voltage and current are of the opposite polarity. The negative regulators are supplied in the same voltages available in the positive series plus two additional voltages commonly used in MECL systems. These supplementary voltages are -2.0 V and -5.2 V, making them well suited for on-card regulation in high-speed logic systems.

The same short-circuit, thermal over-load and safe-operating area protection circuitry is employed in the negative devices making them very rugged. In addition, the devices have the same simplicity of use as the positive MC7800 series devices. Three-terminals, fixed-voltages, easy-heatsinking, and the lack of required external components are features that make the MC7900 series negative regulators applicable to nearly any electronic system power supply.

The Simplest Voltage Regulator to Use (MC7800)

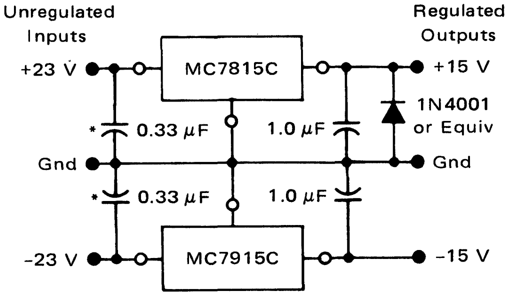
The introduction of the three-terminal voltage regulator marked a milestone in integrated circuit development. Traditionally, IC voltage regulators required numerous external components, and supplied only a few milliamperes without additional current boosting transistors. They had to be programmed to the desired voltage with precision resistors, and could oscillate if proper circuit layout considerations were ignored. The MC7800 Series three-terminal fixed voltage regulators have eliminated these problems.

The new devices are housed in popular power transistor packages which conveniently connect to heatsinks if necessary. They require only three connections — Input, Output, and Ground. External components are required only if the regulator is located an appreciable distance from the supply filter capacitors or if current boosting is required to supply greater than the 1.5 Amperes the devices can provide. Ease of use and low cost make these units ideal as on-card voltage regulators, or in almost any electronic system.

The MC7800 series devices are available in seven popular fixed voltages. The last two numbers of the part type indicate the nominal output voltage. Each type features short-circuit protection, thermal-shutdown, and safe-operating area compensation for the internal series pass transistors. These techniques combine to make the units extremely rugged.

With the arrival of the new MC7800 series voltage regulators, a regulated power supply is available at a minimum of cost and design effort for almost any electronic device. By adding an additional transistor package, regulated voltage can be available almost any place in a system.

COMPLEMENTARY REGULATORS



*Required only if the regulators are located an appreciable distance from the power supply filters.

INTERFACE CIRCUITS

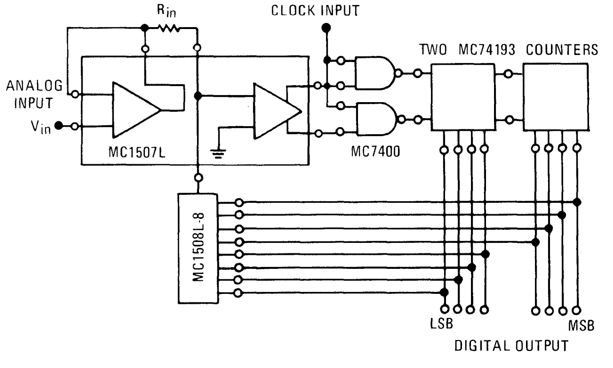
Interface circuits is the name applied to devices that operate with both linear signals and digital logic levels. Most have both linear and digital properties. Examples of interface circuits are D/A and A/D converters, memory sense amplifiers, comparators, and line drivers and receivers.

The rapidly expanding fields of data communications and digital instrumentation make wide use of these interface devices. Line drivers and receivers, for example, are used whenever data must be transmitted over long distances in a computer or piece of peripheral equipment. Also, the industry standard MC1488-89 devices provide the level translation between a Modem and a computer terminal in accordance with the EIA RS-232C specifications. Likewise comparators are used as voltage level detectors in control and instrumentation applications.

Motorola offers a broad line of interface circuits. Two of the newest interface devices are discussed in this section while the complete lineup is outlined beginning on page 3-4.

2

8-BIT TRACKING A-TO-D CONVERTER



Versatile Analog-Digital Control Function (MC1507)

The MC1507 is the third member of the Motorola "building block" series aimed at bridging the gap between the analog and digital worlds. This device is particularly useful when combined with either the MC1508 or MC1506 monolithic Digital-to-Analog (D/A) converters to implement either Tracking or Successive Approximation Analog-to-Digital (A/D) Converter designs.

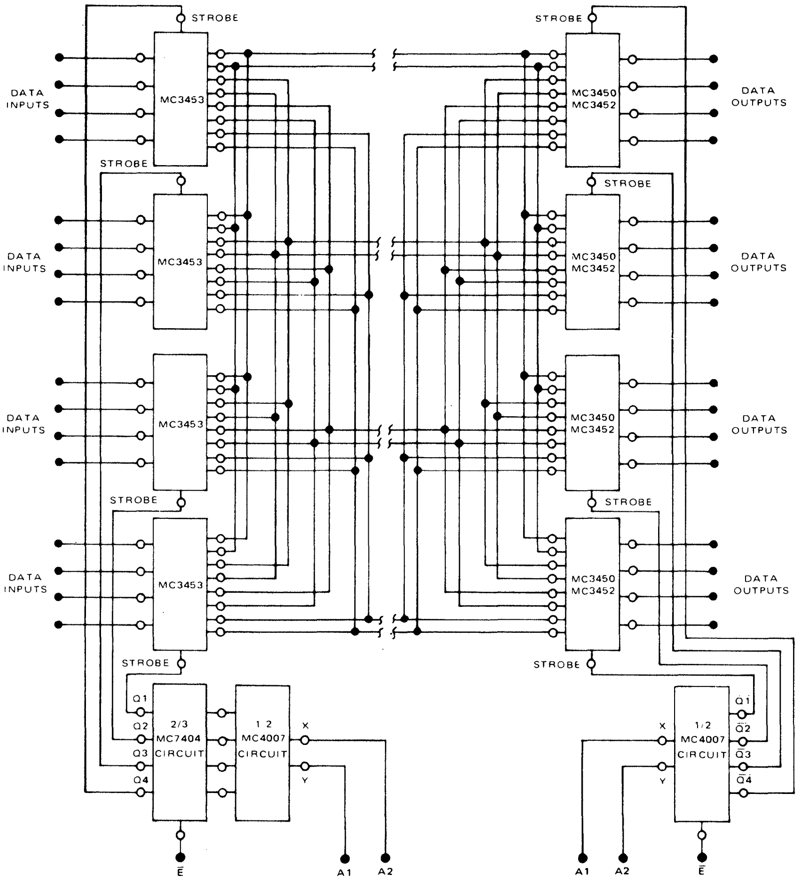
The MC1507 consists of a high-slew-rate op-amp used as an input buffer and a dual-comparator which provides two adjustable, but symmetrical, thresholds. The comparator is used in tracking A/D systems to command a counter chain to increment either up or down. The comparator section is also applicable to "dead-band" or "window" comparator designs where indication is given if an input voltage is greater than or less than a specified voltage range.

The tracking A/D converter, for which the MC1507 is primarily intended, makes use of the high-speed capability inherent in the current mode output of the MC1508 and MC1506 D/A converters. An 8-bit tracking A/D system, for example, using a 5-MHz clock rate provides a normal conversion or update every 0.2 to 1.0 μs, and a full-scale conversion time of 50 μs. Adding a second MC1507 and a "panic mode" circuit decreases the full-scale conversion time to 14 μs.

By disabling the down counting function, the tracking converter can be used as a peak-detecting track and hold circuit. This system will store the maximum value of an input waveform until it is reset. Unlike traditional sample and hold circuits utilizing the charge on a capacitor, the MC1507 system will not suffer a voltage decay after a period of time.

The versatile MC1507 has many additional applications bridging the analog and digital realms. When combined with other building blocks, solutions to numerous analog-digital interface requirements can be economically provided.

PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



Quad Line Drivers and Receivers (MC3450, MC3452, MC3453)

These devices are quad versions of the popular MC75107, MC75108 and MC75110 type dual line Driver/Receivers. They are commonly employed to transmit logic signals over long lengths of cable in large digital systems.

The MC3453 is an MTTL-compatible differential driver with a single enable input common to all four monolithic drivers in the packages.

The MC3452 is a differential line receiver featuring open-collector outputs and a common strobe input. The MC3450 is also a quad receiver; however, it provides active pull-up outputs, and a three-state strobe input, allowing the outputs to be placed in a high impedance state.

In addition to their usage to transmit data within large computer systems, the quad receivers are well suited for use as sense amplifiers with "1103" type MOS memory systems. The quad configuration results in a considerable package savings over existing devices commonly used in this type of application.

ENTERTAINMENT CIRCUITS

The high-volume, low-cost, and highly specialized requirements of the electronic components for consumer entertainment equipment match the capabilities of today's linear ICs. A great variety of the necessary functional blocks for television, stereo phonographs, and radio receivers is now available in low-cost plastic-packaged ICs. The need for improved performance and increased reliability and, at the same time, for a lower selling price, is met by state-of-the-art monolithic circuits.

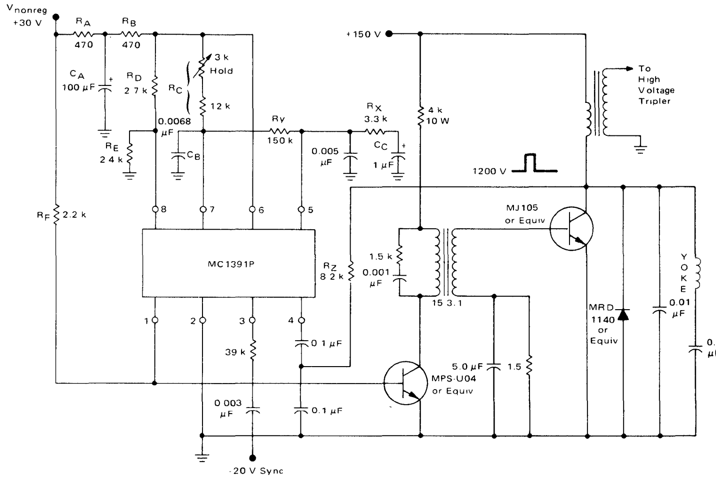
Motorola's traditional leadership in plastic transistors for the customer electronics industry is being extended with a complete lineup of low-cost ICs for those functions which can best be accomplished with monolithic integrated circuits. Both original innovative designs and popular second-source devices which have been well accepted by the industry are included in this diverse family of products. Some typical examples are highlighted here.

2

For Television *alone, Motorola offers more than 20 different types of ICs to give the designer a wide choice of performance levels and partitioning approaches. To aid in the parade toward fully solid-state sets, Motorola offers ICs for the video IF amplifier and detector, AFT, chroma processor and detector, deflection, audio stages, and a combination device which supplies AGC, sync separator and noise-suppression circuitry. Often these ICs permit circuit complexity and performance which would not be technically and economically practical with discrete components.*

A selector guide to ICs for use in television sets is provided on page 3-16. Several new TV ICs are previewed on page 4-6.

TYPICAL HORIZONTAL SECTION



TV Horizontal Processor (MC1391)

The MC1391 TV horizontal processor packs the phase detector, oscillator and pre-driver functions into a single, convenient 8-lead plastic package. The new unit provides the entire low-level horizontal signal processing function and may be used with either transistor or vacuum tube output stages. This device is one of the first inroads of ICs into the television deflection circuitry.

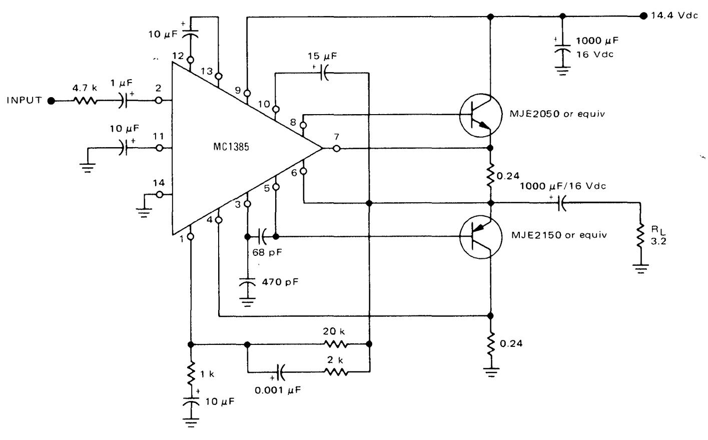
FEATURES:

- Internal shunt regulator
- Preset Hold control capability
- ±300 Hz typical pull-in range
- Balanced phase detector
- Variable output duty cycle for driving tube or transistor
- Low thermal frequency drift
- Small static phase error

For Audio . . .

Linear ICs are rapidly penetrating the audio amplifier stages of television, radio, and stereo phonographs. Both low level and power amplifier applications are realizing greater performance and lower total cost due to the reduced assembly requirements and the ability to use more complex circuitry with these advanced ICs. A wide range of IC types permits the designer a wide lattitude of flexibility to create the exact system performance and costs he requires.

TYPICAL CLASS B AMPLIFIER



Class B Audio Driver (MC1385)

The MC1385 is designed to be used in conjunction with complementary output transistors MJE2050/2150 to produce a 5-watt class B audio amplifier suitable for use in automotive, consumer, and industrial electronics.

FEATURES:

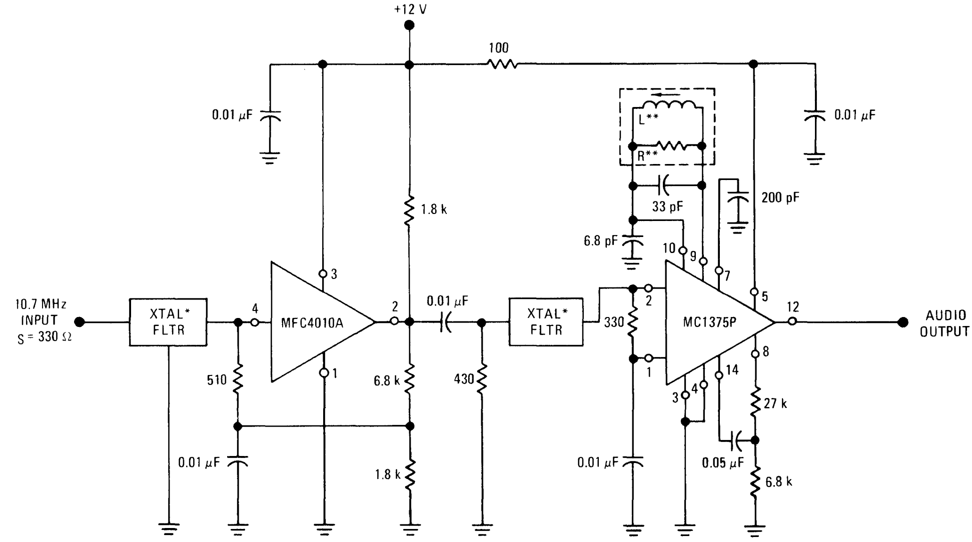
- Internal power supply transient protection
- Built-in programmable short-circuit-current limiting
- Excellent sensitivity – 4.0 mV(RMS) typical
- Excellent power-supply ripple rejection – 35 dB typical
- Wide operating temperature range
- Single supply operation

For Radio . . . .

2

Two sections in FM radios have lent themselves well to integration: The IF amplifier and detector, and the stereo multiplex decoder sections. In both high-quality tuners and in low-priced table radios, the high performance of these ICs and lower assembly costs they make possible, permit more efficient designs.

TYPICAL FM APPLICATION



*10.7 MHz Filter; Vernitron FM-4 or equivalent
**L = 6.0 µH nom
Adjust R for $Q_L \approx 55$

FM IF Circuit (MC1375)

Combining several functions required in solid-state FM receivers, the MC1375 provides the IF amplifier, limiter, FM detector and audio pre-amplifier in a single 14-lead package. The unit requires a minimum of external components.

The IF amplifier/limiter section provides excellent AM rejection and uses an internal zener diode voltage regulator. The detector is a differential peak design which promotes simplified single-coil alignment. The audio preamplifier supplies a voltage gain of ten.

FEATURES:

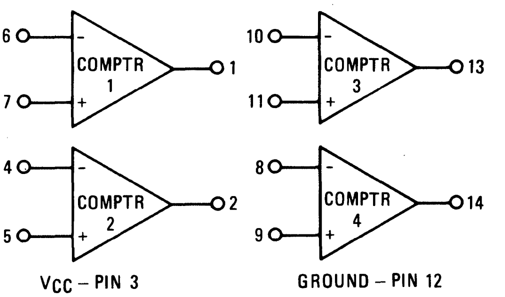
- Good sensitivity: input limiting voltage (Knee) = 250 µV typical
- Excellent AM rejection: 55 dB typical at 10.7 MHz
- Internal zener diode regulation for the IF amplifier section
- Low harmonic distortion
- Differential peak detection: permits simplified single-coil timing
- Audio preamplifier voltage gain: 21 dB typical

For Automotive . . .

In response to consumer demand and government legislation, the automotive industry is undergoing a major engineering evolution. Electronics will be used to perform many of the new complex functions required for the modern automobile. Two approaches are being accepted for applying ICs to automotive electronics: custom and building block. Because of the large volume potential, almost all programs can be expected to end with a specialized custom circuit. However, in the interim, while the systems are being defined and refined, the Motorola building block approach has received wide acceptance.

Highlighted below is one of the new devices in this series of building blocks.

EQUIVALENT CIRCUIT



Quad Comparator (MC3302)

The MC3302 contains four independent comparators designed for wide operating temperatures and single positive-power-supply operation requiring very low supply current.

High density and low cost make this device ideal for automotive, consumer, and industrial applications.

FEATURES:

- Wide operating temperature range — -40 to +85°C
- Single-supply operation — +2.0 to +28 volts
- Differential input voltage = $\pm V_{CC}$
- Compare voltages at ground potential
- MTTL compatible
- Low current drain — 700 μA typical @ V_{CC} = +5.0 to +28 Vdc
- Outputs can be connected to give the Implied AND function

3

LINEAR

INTEGRATED CIRCUITS

SELECTOR GUIDES

OPERATIONAL AMPLIFIERS

Motorola offers a broad line of operational amplifiers to meet a wide range of usages. From low-cost, industry standard types to high precision circuits the span encompasses a large range of performance capabilities. These linear integrated circuits are available as single, dual, and quad monolithic devices in a variety of package styles as well as standard and beam-lead chips.

OPERATIONAL AMPLIFIERS

Listed in order of increasing input bias current within temperature group.

INTERNALLY COMPENSATED

I_{IB} (μA max)	V_{IO} (mV max)	I_{IO} (nA max)	A_{vol} (V/V min)	V_O (V_{pk} min)	@ R_L (kΩ)	& V_{CC}, V_{EE} (Vdc)	f_c (MHz typ)	BW_p (kHz typ)	SR (V/μs typ)	Case	Type
-55 to +125°C Temperature Range											
0.003	4.0	–	Unity	10	10	±15	20	300	30	601	MLM110
0.0075	5.0	3.0	200,000	12	75	±15	0.2	1.5	0.1	601	MC1776‡
0.015	4.0	2.0	100,000	12	2.0	±15	1.0	40	2.5	601	MC1556
0.02	5.0	3.0	100,000	22	5.0	±28	1.0	23	2.0	601	MC1536*
0.075	2.0	10	50,000	10	2.0	±15	1.0	10	0.5	601	MLM107
0.5	5.0	200	50,000	10	2.0	±15	1.0	10	0.8	601,606,632	MC1741* **†
0.5	5.0	200	50,000	10	2.0	±15	1.0	200	15	601	MC1741S
-25 to +85°C Temperature Range											
0.003	4.0	–	Unity	10	10	±15	20	300	30	601	MLM210
0.075	2.0	10	50,000	10	2.0	±15	1.0	10	0.5	601	MLM207
0 to +75°C Temperature Range											
0.007	7.5	–	Unity	10	10	±15	20	300	30	601	MLM310
0.01	6.0	6.0	50,000	12	75	±15	0.2	1.5	0.1	601	MC1776C‡
0.03	10	10	70,000	11	2.0	±15	1.0	40	2.5	601	MC1456
0.04	10	10	70,000	20	5.0	±28	1.0	23	2.0	601	MC1436*
0.09	12	30	25,000	10	2.0	±15	1.0	40	2.5	601	MC1456C
0.09	12	25	50,000	20	5.0	±28	1.0	23	2.0	601	MC1436C
0.25	7.5	50	25,000	10	2.0	±15	1.0	10	0.57	601	MLM307
0.5	6.0	200	20,000	10	2.0	±15	1.0	10	0.8	601,606,626,632,646	MC1741C*†
0.5	6.0	200	20,000	10	2.0	±15	1.0	200	15	601,626	MC1741SC

NONCOMPENSATED

I_{IB} (μA max)	V_{IO} (mV max)	I_{IO} (nA max)	A_{vol} (V/V min)	V_O (V_{pk} min)	@ R_L (kΩ)	& V_{CC}, V_{EE} (Vdc)	f_c (MHz typ)	BW_p (kHz typ)	SR (V/μs typ)	Case	Type
-55 to +125°C Temperature Range											
0.075	2.0	10	50,000	10	2.0	±15	1.0	10	0.5	601	MLM101A
0.15	10	25	2,500	4.5	1.0	±6.0	2.0	100	1.4	602B,606	MC1531
0.5	3.0	60	50,000	10	1.0	±15	2.0	50	4.2	601,632	MC1539*
0.5	5.0	200	50,000	10	2.0	±15	1.0	10	0.8	601,606	MC1748* **
0.5	5.0	200	25,000	10	2.0	±15	0.5	4.0	0.25	601,606,632	MC1709* **†
1.0	5.0	150	40,000	11	2.0	±15	0.8	2.0	2.0	602B,606,632	MC1533
2.0	10	100	1,000	3.5	7.0	±6.0	10	150	5.0	602A,606	MC1520
5.0	2.0	500	2,500	3.5	10	+12,-6.0	7.0	10	1.5	601,606,632	MC1712
10	5.0	2000	4,500	4.5	1.0	±6.0	3.0	100	1.7	602B,606	MC1530
-25 to +85°C Temperature Range											
0.075	2.0	10	50,000	10	2.0	±15	1.0	10	0.5	601, 626	MLM201A
0 to +75°C Temperature Range											
0.25	7.5	50	25,000	10	2.0	±15	1.0	10	0.5	601,626	MLM301A
0.3	15	100	1,500	4.0	1.0	±6.0	2.0	100	1.4	602B,606,646	MC1431
0.5	6.0	200	20,000	10	2.0	±15	1.0	10	0.8	601	MC1748C*
1.0	7.5	100	15,000	10	2.0	±15	2.0	50	4.2	601,626,632,646	MC1439*
1.5	7.5	500	15,000	10	2.0	±15	0.5	4.0	0.25	601,606,626,632,646	MC1709C*†
2.0	7.5	500	30,000	10	2.0	±15	0.8	2.0	2.0	602B,606,632,646	MC1433
4.0	15	200	750	3.0	7.0	±6.0	10	150	5.0	602A,606	MC1420
7.5	5.0	2000	2,000	3.5	10	+12,-6.0	7.0	10	1.5	601,606,632	MC1712C
15	10	4000	3,000	4.0	1.0	±6.0	3.0	100	1.7	602B,606,646	MC1430

*Use MCC prefix for nonencapsulated chip.

**Use MCBC prefix for nonencapsulated beam-lead device, use MCB prefix for beam-lead device in flat ceramic package.

†Use MCCF prefix for nonencapsulated flip-chip.

‡I_{set} = 1.5 μA, $|V_{EE}|$ = V_{CC} = 15 V.

DUAL OPERATIONAL AMPLIFIERS

Listed in increasing order of input bias current.

INTERNALLY COMPENSATED

I_{IB} (μA max)	V_{IO} (mV max)	I_{IO} (nA max)	A_{vol} (V/V min)	V_O (V_{pk} min)	@ R_L (kΩ)	& V_{CC}, V_{EE} (Vdc)	f_c (MHz typ)	BW_p (kHz typ)	SR (V/μs typ)	Case	Type
-55 to +125°C Temperature Range											
0.5	5.0	200	50,000	10	2.0	±15	1.1	14	0.8	601,632	MC1558*†
0.5	5.0	200	50,000	10	2.0	±15	1.0	10	0.5	601,606,632	MC1747
0 to +75°C Temperature Range											
0.5	6.0	200	20,000	10	2.0	±15	1.1	14	0.8	601,626,632,646	MC1458*†
0.5	6.0	200	25,000	10	2.0	±15	1.0	10	0.5	601,606,632	MC1747C
0.7	10	300	20,000	9.0	2.0	±15	1.1	14	0.8	601,626,632,646	MC1458C

*Use MCC prefix for nonencapsulated chip.
†Use MCCF for nonencapsulated flip-chip.

NONCOMPENSATED

I_{IB} (μA max)	V_{IO} (mV max)	I_{IO} (nA max)	A_{vol} (V/V min)	V_O (V_{pk} min)	@ R_L (kΩ)	& V_{CC}, V_{EE} (Vdc)	f_c (MHz typ)	BW_p (kHz typ)	SR (V/μs typ)	Case	Type
-55 to +125°C Temperature Range											
0.5	5.0	200	25,000	12	10	±15	1.0	3.0	0.25	632	MC1537
3.0	3.0	300	4,000	2.5	10	±6.0	1.0	40	0.013	602B,607,632	MC1535
0 to +75°C Temperature Range											
1.5	7.5	500	15,000	12	10	±15	1.0	3.0	0.25	632,646	MC1437
5.0	5.0	500	3,500	2.3	10	±6.0	1.0	40	0.013	602B,607,632	MC1435

QUAD OPERATIONAL AMPLIFIERS

Internally Compensated

. . .for automotive applications

-40 to +85°C Temperature Range

I_{IB} (μA max)	V_{IO} (mV max)	I_{IO} (nA max)	A_{vol} (V/V min)	V_O (V_{pk} min)	@ R_L (kΩ)	& V_{CC}, V_{EE} (Vdc)	f_c (MHz typ)	BW_p (kHz typ)	SR (V/μs typ)	Case	Type
0.3	–	–	1,000	10	5.0	+15	4.0	20	0.6	646	MC3301
. . .for industrial applications											
0 to +75°C Temperature Range											
0.3	–	–	1,000	10	5.0	+15	5.0	20	0.6	646	MC3401

POWER DRIVERS

INTERNALLY COMPENSATED

I_{IB} (μA max)	V_{IO} (mV max)	I_{IO} (nA max)	A_{vol} (V/V min)	V_O (V_{pk} min)	@ R_L (Ω)	& V_{CC}, V_{EE} (Vdc)	f_c (MHz typ)	BW_p (kHz typ)	SR (V/μs typ)	Case	Comments	Type
-55 to +125°C Temperature Range												
200	–	–	900	12	300	±15	–	1500	75	614	High current gain (70 dB) op ampl power booster I_O = 300 mA max	MC1538
0 to +75°C Temperature Range												
300	–	–	850	11	300	±15	–	1500	75	614	High current gain (70 dB) op ampl power booster, I_O = 300 mA max	MC1438

3

INTERFACE CIRCUITS

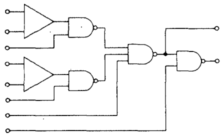
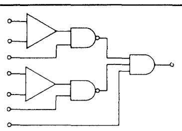
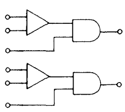
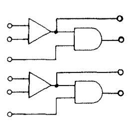
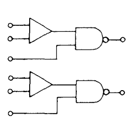
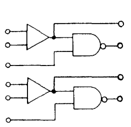
Interface circuits fit in the gray area between the linear and digital realms. Usually these IC's perform the necessary translation between an analog signal input and the required digital logic levels or vice versa. To aid in selection, the devices have been divided into five main categories: Sense Amplifiers, Drivers, D/A Converters, Receivers, and Comparators.

SENSE AMPLIFIERS

The sense amplifiers listed provided the necessary translation from the outputs of core or plated-wire memories to MTTL (unless otherwise noted) logic levels. Unless noted, all devices are designed to operate from ±5.0 volt power supplies. The output of these sense amplifiers changes logic states when the differential input voltage exceeds a specified threshold level, regardless of input polarity.

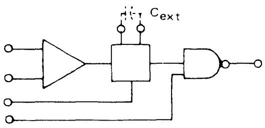
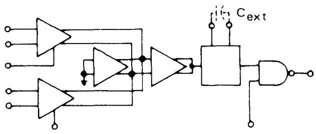
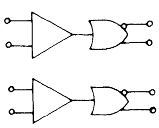
3

CORE MEMORY

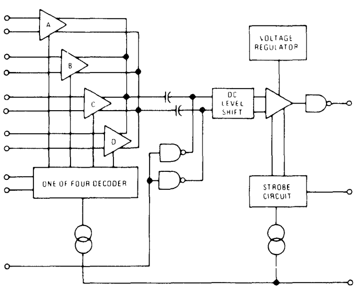
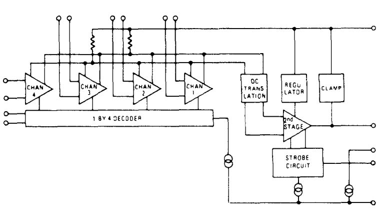
Function		Threshold Voltage (mV) min	Threshold Voltage (mV) max	@ V_{ref} (mV)	Propagation Delay (ns max)	Case	Type -55 to +125°C	Type 0 to +70°C
	Dual channel with independent gating, complementary outputs, memory data register	11 36	19 44	15 40	55	620	–	MC7520
		8.0 33	22 47	15 40	55	620	–	MC7521
	Dual channel with open-collector output, high sink current capability	11 36	19 44	15 40	45	620	–	MC7522
		8.0 33	22 47	15 40	45	620	–	MC7523
	Dual with independent strobing	11 36	19 44	15 40	40	620	–	MC7524
		8.0 33	22 47	15 40	40	620	–	MC7525
	Same as MC7524-25 except amplifier test points included	11 36	19 44	15 40	40	620, 648*	–	MC7528
		10 35	20 45	15 40	40	620	MC5528	–
		8.0 33	22 47	15 40	40	620, 648*	MC5529	MC7529
	Same as MC7524-25 except NAND outputs	11 36	19 44	15 40	40	620, 648*	–	MC7534
		10 35	20 45	15 40	40	620	MC5534	–
		8.0 33	22 47	15 40	40	620, 648*	MC5535	MC7535
	Same as MC7528-29 except NAND outputs	11 36	19 44	15 40	40	620, 648*	–	MC7538
		10 35	20 45	15 40	40	620	MC5538	–
		8.0 33	22 47	15 40	40	620, 648*	MC5539	MC7539

*Case 648 used with commercial-temperature-range devices only.

SENSE AMPLIFIERS (continued)
CORE MEMORY (Continued)

Function	Threshold Voltage @ (mV) min	Threshold Voltage @ (mV) max	V_{ref} (mV)	Propagation Delay (ns max)	Case	Type -55 to +125°C	Type 0 to +75°C
 0.5μs cycle time, 20ns typ response time, ±6.0V power supply	14	20	-6.0V	30	602B, 606, 632	MC1540	MC1440
 0.4μs cycle time, 1.5V common-mode inputs, 1.0mV typ input offset	14	20	-5.0V	30	607, 632	MC1541	MC1441
 Compatible with MECL, +5.0V, -5.2V power supplies, threshold insensitive to supply variations, complementary outputs	17	23	540	35	632	MC1543	–

PLATED-WIRE MEMORIES

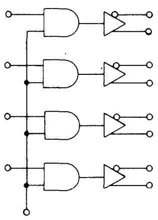
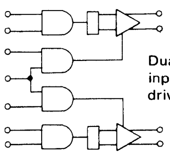
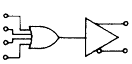
Function	Threshold Voltage (mV – typ)	Propagation Delay (ns – max)	Case	Type -55 to +125°C	Type 0 to +75°C
 AC-coupled, decoded input channel selection, wired-OR output capability, output strobe capability, +5.0V, -6.0V power supply	±1.0	25	620	MC1544	MC1444
 DC coupled, decoded input, 0.5 mV input offset, output strobe capability, +5.0 V, -6.0 V power supply useful with the MCM7001 NMOS memory.	±1.4 (±4.0 max)	14 typ	620	–	MC1446

3

DRIVERS

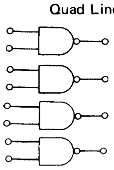
Several types of interface drivers are tabulated in this section: twisted-pair drivers for transmitting data over long lines, RS-232 drivers for interfacing modems and terminals, peripheral drivers for driving lamps, relays and memories, and MOS clock drivers for providing the required clock pulses to highly-capacitive loads.

TWISTED-PAIR LINE DRIVERS

Function	Compatibility	I_O(on) mA (min/max)	$I_{O(off)}$ (μA – max)	t_{PLH}/t_{PHL} Input to Output (ns – typ)	Case	Type -55 to +125°C	Type 0 to +70°C
 Quad MC 75110 Type Driver with common inhibit input	MTTL	6.5/15	100	9.0/9.0	620 648	–	MC3453
 Dual Driver with inhibit inputs for party-line driver applications	MTTL	3.5/7.0 6.5/15	100 100	9.0/9.0 9.0/9.0	632, 646 632, 646	– –	MC75109 MC75110
 Differential Party-Line Driver with push-pull outputs	MDTL	±18/26	–	25/15	632	–	MC75113†

† 0 to +75°C Temperature Range

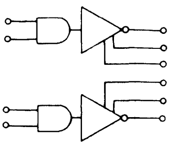
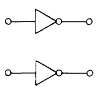
RS-232 LINE DRIVER

Function	Compatibility	V_{OL} & Vdc min	V_{OH} & Vdc min	& V_{CC} Vdc	V_{EE} Vdc	t_{PLH}/t_{PHL} ns typ	Case	Type 0 to +75°C
Quad Line Driver 	MDTL, MTTL	-6.0 -9.0	+6.0 +9.0	+9.0 +13.2	-9.0 -13.2	150/65*	632	MC1488

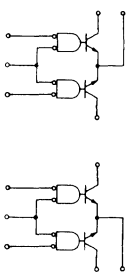
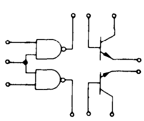
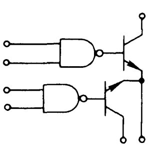
* @ 3000 ohms, 15 pF

INTERFACE CIRCUITS (Continued)

DRIVERS (continued)
MOS CLOCK DRIVERS

Function	Input Compatibility	PRR (max) C = 1000 pF	@ V_{CC}/V_{EE} (volts)	t_{PLH}	t_{TLH}	t_{PHL}	t_{THL}	Temperature (°C)	Case	Type
				Switching Times C = 1000 pF, ns-typ						
Dual MOS Clock Driver with Strobe 	MDTL,MTTL	2.0 MHz	5.0/-20	75	75	50	50	-55 to +125	632	MC1585
Dual MOS clock Driver 	MTTL	–	0/-20	12	17	7.5	20	-55 to +125	601 632	MMH0026
		–	0/-20	12	17	7.5	20	0 to +85	601 626 632	MMH0026C

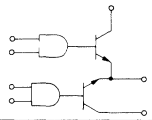
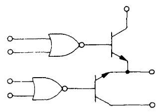
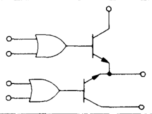
PERIPHERAL DRIVERS

Function	Compatibility	$I_{O(on)}$ (mA – max)	t_{PLH}/t_{PHL} Input to Output (ns – typ)	Case	Type -55 to +125°C	Type 0 to +70°C
 Dual Memory Driver with logic inputs, 24-volt output capability	MDTL,MTTL	600	25/25 (to source collectors) 20/20 (to sink outputs)	620, 648#	MC55325	MC75325
 Dual Peripheral Positive AND Driver, plus two noncommitted NPN output transistors	MDTL,MTTL	300*	21/16	632 646	–	MC75450
 Dual Peripheral Positive AND Driver with logic gate outputs internally connected to NPN output transistors	MDTL,MTTL	300*	17/18	626	–	MC75451

#Case 648 used with industrial-temperature-range devices only.
*Each transistor

INTERFACE CIRCUITS (Continued)

DRIVERS (continued)
PERIPHERAL DRIVERS (continued)

Function		Compatibility	$I_{O(on)}$ (mA – max)	t_{PLH}/t_{PHL} Input to Output (ns – typ)	Case	Type	
						-55 to +125°C	0 to +70°C
	Dual positive NAND driver with logic gate outputs internally connected to NPN output transistors	MDTL, MTTL	300*	18/16	626	–	MC75452
	Dual positive OR Driver with logic gate outputs internally connected to NPN output transistors	MDTL, MTTL	300*	12/17	626	–	MC75453
	Dual positive NOR Driver with logic gate output internally connected to NPN output transistors	MDTL, MTTL	300*	25/19	626	–	MC75454

*Each Transistor

MOS-LED DISPLAY DRIVERS

Function	Sink Current (mA-max)	Source Current (mA-max)	t_{PLH}/t_{PHL} Input to Collector Output (ns - typ)	Collector Voltage (V - max)	Case	Type 0 to + 70° C
Quad Segment Driver	50	50	40 / 20	10	632 646	MC75491
Hex Digit Driver	250	—	80 / 40	10	632 646	MC75492

D/A CONVERTERS

The low-cost D/A converters described here find wide usage in communications, control, and instrumentation systems. They provide a current output which is the product of a digital word and an analog reference voltage.

DIGITAL-TO-ANALOG CONVERTERS

Function	Compatibility	Error (% – max)	I_O (mA – typ)	t_S (ns – typ)	TCI_O (ppm/°C – typ)	Case	Type	
							-55 to +125°C	0 to +70°C
6-Bit Multiplying Digital-to-Analog Converters	MDTL, MTTL	±0.78	2.0	150	–	632	MC1506	MC1406
8-Bit Multiplying Digital-to-Analog Converters	MDTL, MTTL, CMOS	±0.19 ±0.39 ±0.78	2.0 2.0 2.0	300 200 200	-20 -20 -20	620 620 620	MC1508L8 – –	MC1408L8 MC1408L7 MC1408L6

A/D CONVERTERS

This analog-digital control circuit is useful in high-speed tracking A/D converters, window comparators, and peak detecting sample and hold circuits.

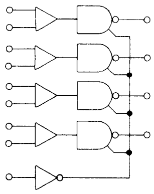
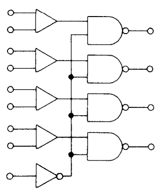
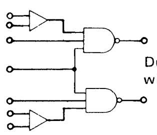
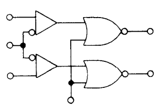
ANALOG-DIGITAL CONTROL CIRCUIT

Amplifier Slew Rate $A_V = \pm 1$ (V/µs - typ)	Amplifier Settling Time $A_V = \pm 1$ (µs - typ)	Comparator Threshold V_{ref} = 40 mV (mV – min/max)	Comparator Bias Current (µA - max)	Case	Temperature (°C)	Type
20	0.8	±36/±44	1.5	620	-55 to +125	MC1507
20	0.8	±30/±50	2.5	620	0 to +70	MC1407

RECEIVERS

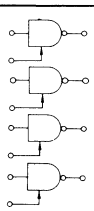
Mating with the driver types listed in the previous section are the receivers tabulated in this section: twisted-pair receivers for computer applications, and RS-232 receivers to interface with similar drivers.

TWISTED-PAIR LINE RECEIVERS

Function		Compatibility	Input Threshold (mV – typ)	Input Common Mode Range (V – min)	t_{PLH}/t_{PHL} Input to Output (ns – typ)	Case	Type -55 to +125°C	Type 0 to +70°C
	Quad Receiver with common 3-state strobe input, active pullup outputs (Quad MC75107 type)	MTTL	±25	±3.0	19/19	620 648	–	MC3450
	Quad Receiver with common strobe input, open collector outputs (Quad MC75108 type)	MTTL	±25	±3.0	19/19	620 648	–	MC3452
 Dual Line Receiver with strobe inputs	Active Pullup Outputs	MTTL	±25	±3.0	17/17	632, 646#	MC55107	MC75107
	Open Collector Outputs	MTTL	±25	±3.0	19/19	632, 646#	MC55108	MC75108
	Dual Single-Ended Receiver with common reference input	MTTL	±100	5.5	22/22	626	–	MC75140

#Case 646 used with industrial-temperature-range devices only.

RS-232 LINE RECEIVERS

Function		Compatibility	Input Turn-On Threshold (Vdc – max)	Input Turn-Off Threshold (Vdc – max)	Input Hysteresis (mV – typ)	t_{PLH}/t_{PHL} (ns – typ)	Case	Type 0 to +75°C
	Quad Line Receiver	MDTL,MTTL MDTL,MTTL	1.5 2.25	1.25 1.25	250 1150	25/25 25/25	632 632	MC1489 MC1489A

COMPARATORS

A comparator provides a logical output in response to the polarity of the differential voltage applied to the inputs of the device. High-speed, high-input-impedance/precision, and low-cost quad-type comparators are tabulated to aid in the selection of the proper device type for any given circuit application.

A_{vol} (V/V min)	V_{IO} (mVdc max)	I_{IB} (μAdc max)	V_{OH} (Vdc)		V_{OL} (Vdc)		I_{Os} (mAdc min)	tp (ns typ)	Case	Type	Features
			min	max	min	max					
-55 to +125°C Temperature Range											
200,000 typ	3.0	0.01	–	–	–	1.5	–	200	601,606,632	MLM111	High input impedance
1,250	2.0	20	2.5	4.0	-1.0	0	2.0	40	601,606,632	MC1710* **	Output impedance = 200 ohms
1,250	2.0	20	2.5	4.0	-1.0	0	2.8	40	607,632	MC1514	Dual, strobe capability
750	3.5	75	2.5	5.0	-1.0	0	0.5	40	603,606, 632	MC1711*	Dual with outputs wired OR, strobe capability
-25 to +85°C Temperature Range											
200,000 typ	3.0	0.01	–	–	–	1.5	–	200	601,606,632	MLM211	High input impedance
0 to +75°C Temperature Range											
200,000 typ	7.5	0.05	–	–	–	1.5	–	200	601,606, 626,632	MLM311	High input impedance
1,000	5.0	25	2.5	4.0	-1.0	0	1.6	40	601,606, 632,646	MC1710C*	Output impedance = 200 ohms
1,000	5.0	25	2.5	4.0	-1.0	0	1.6	40	607,632,646	MC1414	Dual, strobe capability
700	5.0	100	2.5	5.0	-1.0	0	0.5	40	603,606, 632,646	MC1711C*	Dual with outputs wired OR strobe capability

QUAD COMPARATOR

V_{IO} (mVdc max)	I_{IB} (μAdc max)	V_{OL} (Vdc max)	Output Leakage Current (μA max)	I_{Os} (mAdc typ)	V_{IDR} (Vdc max)	Case	Type
-40 to +85°C Temperature Range							
20	0.5	0.4	10	5.0	$\pm V_{CC}$	646	MC3302

Features

These comparators are designed specifically for single positive-power-supply operation from +2.0 to +28 Vdc. Each monolithic device contains four independent comparators, yet total package power supply current drain is 1.5 mA max.

*Use MCC prefix for nonencapsulated chip.

**Use MCBC prefix for nonencapsulated beam-lead device; use MCB prefix for beam-lead device in ceramic flat package.

DEFINITIONS

A_{vol}	Open-Loop Voltage Gain	V_{OH}	Positive Output Voltage
V_{ID}	Differential Voltage Range	V_{OL}	Negative Output Voltage
V_{IO}	Input Offset Voltage	I_{Os}	Output Sink Current
I_{IB}	Input Bias Current	tp	Propagation Delay Time

HIGH-FREQUENCY AMPLIFIERS

Motorola's high-frequency amplifiers simplify the design of receivers and signal processors. Many offer AGC capability or several gain options to provide extra design flexibility.

HIGH-FREQUENCY AMPLIFIERS

Bandwidth (MHz)	V_{OS} (Vp-p)	$\lvert z_{in} \rvert$ (kΩ @ kHz)		$\lvert z_o \rvert$ (Ω @ kHz)		A_{VS} (dB)	Gp @ 60 MHz (dB)	Diff. Input and Output	AGC	V_{CC}, V_{EE} (Vdc)	Case	Type -55 to +125°C	Type 0 to +75°C
dc to 40	4.5	6.0	20	35	20	90 (fixed)	–	Yes	No	±6.0	601	MC1510	MC1410
dc to 75	2.5	10	50	25	50	18 (fixed)	–	Yes	Yes	±5.0	602A, 607, 632	MC1545	MC1445
22 min	6.0	1.8	1.0 M	100 k	1.0 M	26 (AGC = 0)	25	No	Yes	+6.0	602B, 606	MC1550	–
40 @ A_V = 34 dB 35 @ A_V = 40 dB	4.2	10	100	16	100	30 – 40 (fixed)	–	No	No	+6.0	602B	MC1552	–
35 @ A_V = 46 dB 15 @ A_V = 52 dB	4.2	10	100	16	100	46 – 52 (fixed)	–	No	No	+6.0	602B	MC1553	–
100 @ A_V = 4.0 dB 60 @ A_V = 25 dB	7.0	3.0	1.0 M	100 k	1.0 M	44 (AGC = 0)	45	Yes	Yes	+12	601	MC1590	–
40 @ A_V = 52 dB 90 @ A_V = 40 dB 120 @ A_V = 20 dB	4.0	4.0 30 250	1.0 1.0 1.0	20	1.0	52 40 20	–	Yes	No	±6.0	603 632	MC1733	MC1733C

3

REGULATORS

Motorola offers a broad line of voltage regulators ranging from low-cost "Functional Circuits" to high-precision units. Regulators for positive and negative voltages are available as well as a unique floating regulator, type MC1566L, whose maximum output voltage and current are limited only by the external pass transistor.

3

POSITIVE VOLTAGE REGULATORS

V_O Vdc min	V_O Vdc max	I_O (mAdc max)	$\|V_{in}-V_O\|$ (Vdc) min	$\|V_{in}-V_O\|$ (Vdc) max	V_{in} (Vdc) min	V_{in} (Vdc) max	I_{IB} (mAdc max)	Reg_{in} $\%V_O/V_{in}$ (max)	Reg_L ($\%V_O$ max)	P_D (W max) T_C = 25°C	P_D (W max) T_A = +25°C	Case	Type
-55 to +125°C Temperature Range													
4.5	40	20	3.0	30	8.5	50	2.0	0.06	0.05 mV	–	0.68	601	MLM105
2.5	37	200 500	2.7	40	8.5	40	9.0	0.015	0.13 0.05	1.8 17.5	0.68 3.0	602A 614	MC1569*
2.5	37	200 500	2.7	40	8.5	40	9.0	0.015	0.13 0.05	1.8 17.5	0.68 3.0	602A 614	MC1561
2.5	17	200 500	2.7	20	8.5	20	9.0	0.015	0.13 0.05	1.8 12	0.68 3.0	602A 614	MC1560
2.0	37	150	3.0	38	9.5	40	3.5	0.030	0.15	–	0.8	603,606, 632,607**	MC1723* **
-25 to +85°C Temperature Range													
4.5	40	20	3.0	30	8.5	50	2.0	0.06	0.05 mV	–	0.68	601	MLM205
-10 to +75°C Temperature Range													
4.6	32	200	3.0	–	9.0	35	–	0.03	0.2	–	1.0	206A	MFC4060A
4.6	32	200	3.0	–	9.0	35	–	0.03	0.2	–	1.0	643A	MFC6030A
4.6	32	200	3.0	–	9.0	35	–	0.06	0.4	–	1.0	206A	MFC4062A
4.6	32	200	3.0	–	9.0	35	–	0.06	0.4	–	1.0	643A	MFC6032A
4.6	17	200	3.0	–	9.0	20	–	0.03	0.2	–	1.0	206A	MFC4063A
4.6	17	200	3.0	–	9.0	20	–	0.03	0.2	–	1.0	643A	MFC6033A
4.6	17	200	3.0	–	9.0	20	–	0.06	0.4	–	1.0	206A	MFC4064A
4.6	17	200	3.0	–	9.0	20	–	0.06	0.4	–	1.0	643A	MFC6034A
0 to +70°C Temperature Range													
4.5	30	20	3.0	30	8.5	40	2.0	0.06	0.05 mV	–	0.68	601	MLM305
2.5	32	200 500	3.0	35	9.0	35	12	0.030	0.13 0.05	1.8 17.5	0.68 3.0	602A 614	MC1469*
2.5	32	200 500	3.0	35	9.0	35	12	0.030	0.13 0.05	1.8 17.5	0.68 3.0	602A 614	MC1461
2.5	17	200 500	3.0	20	9.0	20	12	0.030	0.13 0.05	1.8 12	0.68 3.0	602A 614	MC1460
2.0	37	150	3.0	38	9.5	40	4.0	0.030	0.20	–	0.8	603,606, 632	MC1723C*

*Also available as nonencapsulated chip. use MCC prefix.

**Also available as nonencapsulated beam-lead device; use MCBC prefix, use MCB prefix for device in ceramic flat package.

FIXED OUTPUT POSITIVE VOLTAGE REGULATORS

V_O (Vdc) min	V_O (Vdc) max	I_O (mAdc max)	$\|V_{in}-V_O\|$ (Vdc) min	$\|V_{in}-V_O\|$ (Vdc) max	V_{in} (Vdc) min	V_{in} (Vdc) max	I_{IB} (mAdc max)	Reg_{in} (mV max)	Reg_L (mV max)	P_D (W max) $T_C = +25^{\circ}C$	P_D (W max) $T_A = +25^{\circ}C$	Case	Type
-55 to +150°C Junction Temperature Range													
4.7	5.3	1000 200	2.0	30	7.0	35	10	50	100 50	20 2.0	3.5 0.8	11 79	MLM109
-25 to +125°C Junction Temperature Range													
4.7	5.3	1000 200	2.0	30	7.0	35	10	50	100 50	20 2.0	3.5 0.8	11 79	MLM209
0 to +125°C Junction Temperature Range													
4.8	5.2	1000 200	2.0	30	7.0	35	10	50	100 50	20 2.0	3.5 0.8	11 79	MLM309
4.8	5.2	750	2.0	30	7.0	35	8.0	100	100	7.5	2.0	199-04	MC7705C
5.75	6.25	750	2.0	29	8.0	35	8.0	120	120	7.5	2.0	199-04	MC7706C
7.7	8.3	750	2.5	27	10.5	35	8.0	160	160	7.5	2.0	199-04	MC7708C
11.5	12.5	750	2.5	23	14.5	35	8.0	240	240	7.5	2.0	199-04	MC7712C
14.4	15.6	750	2.5	20	17.5	35	8.0	300	300	7.5	2.0	199-04	MC7715C
17.3	18.7	500	3.0	17	21	35	8.0	360	360	7.5	2.0	199-04	MC7718C
19.2	20.8	500	3.0	20	23	40	8.0	400	400	7.5	2.0	199-04	MC7720C
23	25	500	3.0	16	27	40	8.0	480	480	7.5	2.0	199-04	MC7724C
4.8	5.2	1500	2.0	30	7.0	35	8.0	100	100	15	2.0 2.5	199-04 11	MC7805C
5.75	6.25	1500	2.0	29	8.0	35	8.0	120	120	15	2.0 2.5	199-04 11	MC7806C
7.7	8.3	1500	2.5	27	10.5	35	8.0	160	160	15	2.0 2.5	199-04 11	MC7808C
11.5	12.5	1500	2.5	23	14.5	35	8.0	240	240	15	2.0 2.5	199-04 11	MC7812C
14.4	15.6	1500	2.5	20	17.5	35	8.0	300	300	15	2.0 2.5	199-04 11	MC7815C
17.3	18.7	1000	3.0	17	21	35	8.0	360	360	15	2.0 2.5	199-04 11	MC7818C
23	25	1000	3.0	16	27	40	8.0	480	480	15	2.0 2.5	199-04 11	MC7824C

TRACKING VOLTAGE REGULATORS

V_{OR}† (Vdc) min	V_{OR}† (Vdc) max	I_O (mAdc max)	$\|V_{in}-V_O\|$ (Vdc) min	V_{in} (Vdc) min	V_{in} (Vdc) max	I_{IB} (mAdc max)	Reg_{in} $\%V_O/V_{in}$ (max)	Reg_L ($\%V_O$ max)	P_D (W max) $T_C = 25^{\circ}C$	P_D (W max) $T_A = 25^{\circ}C$	Case	Type
-55 to +125°C Temperature Range												
±14.8	±15.2	100†	2.0	±17.2	±30	+4.0,-3.0	0.006	0.07	2.1 2.5 9.0	0.8 1.0 2.4	603 632 614	MC1568
0 to +75°C Temperature Range												
±14.5	±15.5	100†	2.0	±17.5	±30	+4.0,-3.0	0.01	0.07	2.1 2.5 9.0	0.8 1.0 2.4	603 632 614	MC1468

†Preset Voltage Range; range is adjustable by adding external resistors from ±8.0 to ±20 Vdc.

NEGATIVE VOLTAGE REGULATORS

V_O (Vdc) min	V_O (Vdc) max	I_O (mAdc max)	$\lvert V_{in}-V_O \rvert$ (Vdc) min	$\lvert V_{in}-V_O \rvert$ (Vdc) max	V_{in} (Vdc) min	V_{in} (Vdc) max	I_{IB} (mAdc max)	Reg_{in} $\%V_O/V_{in}$ (max)	Reg_L ($\%V_O$ max)	P_D (W max) $T_C = 25°C$	P_D (W max) $T_A = +25°C$	Case	Type
-55 to +125°C Temperature Range													
-3.6	37	200 500	-2.7	35	-8.5	-40	11	0.015	0.13 0.05	1.8 9.0	0.68 2.4	602A 614	MC1563*
-0.015	-40	20	2.0	50	-8.0	-50	5.0	0.1	0.05	1.8	0.68	603	MLM104
-25 to +85°C Temperature Range													
-0.015	-40	20	2.0	50	-8.0	-50	5.0	0.1	0.05	1.8	0.68	603	MLM204
0 to +70°C Temperature Range													
-3.8	-32	200 500	-3.0	40	-9.0	-35	14	0.030	0.13 0.05	1.8 9.0	0.68 2.4	602A 614	MC1463*
-0.035	-30	20	2.0	40	-8.0	-40	5.0	0.1	0.05	1.8	0.68	603	MLM304

*Also available as nonencapsulated chip, use MCC prefix.

FIXED OUTPUT NEGATIVE VOLTAGE REGULATORS

V_O (Vdc) min	V_O (Vdc) max	I_O (mAdc max)	$\lvert V_{in}-V_O \rvert$ (Vdc) min	$\lvert V_{in}-V_O \rvert$ (Vdc) max	V_{in} (Vdc) min	V_{in} (Vdc) max	I_{IB} (mAdc max)	Reg_{in} (mV max)	Reg_L (mV max)	P_D (W max) $T_C = +25°C$	P_D (W max) $T_A = +25°C$	Case	Type
0 to +125°C Junction Temperature Range													
-1.92	-2.08	1500	5.0	33	-7.2	-35	8.0	40	120	15	2.0 2.5	199-04 11	MC7902C
-4.8	-5.2	1500	2.0	30	-7.0	-35	8.0	100	100	15	2.0 2.5	199-04 11	MC7905C
-5.0	-5.4	1500	2.0	29.8	-7.0	-35	8.0	105	105	15	2.0 2.5	199-04 11	MC7905.2C
-5.75	-6.25	1500	2.0	29	-8.0	-35	8.0	120	120	15	2.0 2.5	199-04 11	MC7906C
-7.7	-8.3	1500	2.5	27	-10.5	-35	8.0	160	160	15	2.0 2.5	199-04 11	MC7908C
-11.5	-12.5	1500	2.5	23	-14.5	-35	8.0	240	240	15	2.0 2.5	199-04 11	MC7912C
-14.4	-15.6	1500	2.5	20	-17.5	-35	8.0	300	300	15	2.0 2.5	199-04 11	MC7915C
-17.3	-18.7	1000	3.0	17	-21	-35	8.0	360	360	15	2.0 2.5	199-04 11	MC7918C
-23	-25	1000	3.0	16	-27	-40	8.0	480	480	15	2.0 2.5	199-04 11	MC7924C

SPECIAL-PURPOSE REGULATORS

V_O min	V_O max	Reg_{in} (max)	Reg_L (max)	Current Regulation	P_D (W max)	Case	Type	Features
-55 to +125°C Temperature Range								
0	1000*	0.01% +1mV	0.01% +1mV	0.1% +1mA	0.300	632	MC1566	A floating regulator, can be used as a voltage controlled current source.
0 to +75°C Temperature Range								
0	1000*	0.03% +3mV	0.03% +3mV	0.02% +1mA	0.360	632	MC1466	A floating regulator, can be used as a voltage controlled current source.

*Limited only by the characteristics of the external series pass transistor.

3

SPECIAL-PURPOSE CIRCUITS

The linear-integrated-circuits listed in this section were developed by Motorola for the system design engineer to fill special-purpose requirements as indicated by the subheadings. Temperature ranges and package availability are also tailored to provide versatility.

MULTIPLIERS

Function	Linearity Error (typ)	Input Voltage Range (Vdc min)	Case	Type -55 to +125°C	Type 0 to +70°C
A four-quadrant multiplier designed to operate with ±15-volt supplies; has internal level-shift circuitry and voltage regulator.	±0.3%	±10	620	MC1594	–
	±0.5%	±10	620	–	MC1494
Applications include multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.	X Input = 0.5% Y Input = 1.0%	±10	632	MC1595*	–
	X Input = 1.0% Y Input = 2.0%	±10	632	–	MC1495*

*Also available as a nonencapsulated chip, use MCC prefix.

BALANCED MODULATOR/DEMODULATOR

Function	Carrier Suppression dB @ f (MHz) (typ)		Common-Mode Rejection (dB typ)	Case	Type -55 to +125°C	Type 0 to +75°C
Balanced modulator/demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier).	65 50	0.5 10	85	602A, 632	MC1596	MC1496

LOW-FREQUENCY CIRCUITS

Function	Output Power (W typ)	Voltage Gain – typ (V/V typ)	Total Harmonic Distortion (% typ)	Case	Type -55 to +125°C	Type 0 to +70°C
A power amplifier device capable of single or split supply operation.	1.0	10, 18, 36	0.4	602B	MC1554	MC1454

POWER-CONTROL CIRCUITS

Function	Temperature	Case	Type
Zero voltage switch for use in ac power switching with output capable of triggering triacs.	-10 to +75°C	644A	MFC8070

TIMING CIRCUIT

Function	Supply Voltage V_{CC} (Vdc – max)	Initial Timing Error V_{CC} = 5 & 15 V, C = 0.1 µF (%-typ)	V_{OL} V_{CC} = 15 V I_{sink} = 50 mA (Vdc – max)	V_{OH} V_{CC} = 15 V I_{source} = 100 mA (Vdc – min)	Case	Type -55 to +125°C	Type 0 to +75°C
Wide range adjustable timers	16	1.0	0.75	12.75	601, 626	–	MC1455
	18	0.5	0.5	13	601	MC1555	–

3

CONSUMER APPLICATION SELECTOR GUIDE

. . .reflecting Motorola's continuing commitment to semiconductor products necessary for consumer system designs. The tabulation contains data for a large number of components designed principally for entertainment product applications. It is arranged to simplify first-order of linear integrated circuit device lineups to satisfy primary functions for Television, Audio, Radio, Automotive and Organ applications.

3

TELEVISION CIRCUITS

SOUND

Function	Features	Case	Type
Sound IF, Detector, Limiter, Audio Preamplifier	80 μV, 3 dB Limiting Sensitivity, 3.5 V(RMS) Output, Sufficient for Single Transistor Output Stage	646,647	MC1351
Sound IF Detector	Interchangeable with ULN2111A	646,647	MC1357
Sound IF Detector, DC Volume Control, Preamplifier	Excellent AMR, Interchangeable with CA3065	646,647	MC1358

VIDEO

Function	Features	Case	Type
1st and 2nd Video IF Amplifier	IF Gain @ 45 MHz – 60 dB typ AGC Range – 70 dB min	626	MC1349
	IF Gain @ 45 MHz – 46 dB typ, AGC Range – 60 dB min	626	MC1350
1st and 2nd Video IF, AGC Keyer and Amplifier	IF Gain @ 45 MHz – 53 dB typ, AGC Range – 65 dB min "Forward AGC" Provided for Tuner	646	MC1352
	Same as MC1352, with Opposite AGC for Tuner	646	MC1353
3rd IF and Video Detector	Low-Level Detection, Low Harmonic Generation, Reduced Circuit Cost and Complexity Reduced Shielding	626	MC1330
3rd IF, Video Detector, Sound IF Detector, and Sync Separator	Low-Level Detection, Separate Sound Detector, Differential Inputs	646	MC1331
AGC Keyer, AGC Amplifier, Noise Gate, Sync Separator	High-Quality Noise Gate, One IF AGC Output and Two Tuner AGC Outputs, Adjustable AGC Delay	646	MC1344
Automatic Fine Tuning	High Gain AFT System, Interchangeable with CA3064	646 686	MC1364

CHROMA

Function	Features	Case	Type
Chroma IF Amplifier and Subcarrier System	Includes Complete Chroma IF, AGC, dc Gain and Tint Controls, Injection Locked Oscillator, Low Peripheral Parts Count	646	MC1398
Chroma Subcarrier System	Interchangeable with CA3070, APC Chroma Reference System	648	MC1370
Chroma IF Amplifier	Interchangeable with CA3071, Automatic and Manual Gain Control	646	MC1371
Dual Chroma Demodulators	Industry Standard Demodulator, Low Differential Output dc Drift	603 646, 647	MC1328
	Same as MC1328 with short-circuit protected outputs, and improved dc tracking and temperature coefficients on outputs.	646	MC1329
	Similar to MC1328 but with Luminance and Blanking Inputs, Internal Matrix Provides RGB Outputs	646,647	MC1326
	Same as MC1326 with short-circuit protected outputs, and improved dc tracking and temperature coefficients on outputs.	646	MC1324
	Dual Doubly Balanced Demodulator with RGB Output Matrix and PAL Switch	646,647	MC1327

DEFLECTION

Function	Features	Case	Type
Horizontal Processor	Includes Phase-Detector, Oscillator and Predriver; Linear Balanced Phase Detector; Adjustable dc Loop Gain	626	MC1391

CONSUMER APPLICATION SELECTOR GUIDE (Continued)

AUDIO CIRCUITS

PREAMPLIFIERS

Function	V_{CC} (Vdc – max)	A_{vol} (dB min)	THD (% typ)	z_o (Ohms typ)	Case	Type
Dual Preamplifier	±15	80	0.1	100	632	MC1303
Dual Low-Noise Preamplifier	16	63	0.1	100	646	MC1339
Low-Noise Preamplifier	33	80	0.1	100	644A	MFC8040

DRIVERS

Function	V_{CC} (Vdc – max)	Drive Current (mA)	A_{vol} (dB)	Case	Type
Class A Audio Driver	18	30 min	42 min	206A	MFC4050
Class B Audio Drivers	35	150 peak	89 typ	644A	MFC8020A
	20	150 peak	87 typ	644A	MFC8021A
	45	150 peak	90 typ	644A	MFC8022A
	25	50 max	–	646	MC1385

POWER AMPLIFIERS

Function	P_O (Watts)	V_{CC} (Vdc max)	e_{in} @ rated P_O (mV – max)	P_D (mA – max)	R_L (Ohms)	Case	Type
Audio Power Amplifiers	0.5	12	3.0	4.0	8.0	626	MC1306
	0.25	12	3.0	3.5	16	206A	MFC4000B
	1.0	20	100	5.0	16	643A	MFC6070

RADIO CIRCUITS

IF AMPLIFIERS

Function	Gain @ 10.7 MHz (dB – typ)	3 dB Limiting @ 10.7 MHz (mV(RMS) typ)	AMR (dB – typ)	Recovered Audio Output Δf = 75 kHz (mV(RMS))	Power Supply (Volts – max)	Case	Type
IF Amplifier	58	–	–	–	18	626	MC1350
Limiting FM-IF Amplifier	–	0.175	60	690	18	646,647	MC1355
Limiting IF Ampl/Quadrature Detector	53	0.600	45	480	16	646,647	MC1357
IF Amplifier	42	0.4	–	–	18	206A	MFC4010A
IF Amplifier, Nonsaturating Limiter	40	60	50	500	20	643A	MFC6010
IF Amplifier, Limiter, Detector, Audio Preamplifier	21	0.25	55	625	16	646	MC1375

DECODERS

Function	Channel Separation (dB – typ)	THD (% – typ)	Stereo – Indicator Lamp Driver (mA – max)	Features	Case	Type
FM Multiplex Stereo Decoders	45	0.5	40	Audio Muting	646	MC1304
	45	0.5	40	Audio Muting	646	MC1305
	40	0.5	40	–	646	MC1307
	40	0.3	75	Coilless Operation	646	MC1310
	40	0.5	100	Coilless Operation, Emitter Follower Outputs, and Unity Gain	648	MC1311
Four-Channel SQ* Decoders	45	0.1	–	V_{CC} = 20 Vdc nom	646	MC1312
	45	0.25	–	V_{CC} = 12 Vdc nom	646	MC1313

*Trademark of Columbia Broadcasting System, Inc.

AUTOMOTIVE CIRCUITS

OPERATIONAL AMPLIFIER

Function	V_{CC} Range (Vdc)	A_{vol} (V/mV – typ)	I_{IB} (μA – max)	Unity Gain Bandwidth (MHz – typ)	R_{in} (MegΩ typ)	Case	Type
Quad Operational Amplifier	4.0 to 28	2.0	0.3	4.0	1.0	646	MC3301

COMPARATOR

Function	V_{CC} Range (Vdc)	V_{IDR} (Vdc)	I_{IB} (μA-max)	Output Leakage Current (μA-max)	Sink Current	Case	Type
Quad Comparator	2.0 to 28	$\pm V_{CC}$	0.5	1.0	6.0	646	MC3302

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ORGAN CIRCUITS

FREQUENCY DIVIDERS

Function	V_{CC} Range (Vdc)	f_{Tog} (MHz – typ)	V_{OH} (Vdc – min)	Case	Type
Toggle Flip-Flop	6.0 to 16	3.0	15.5	206A	MFC4040
Dual Toggle Flip-Flop	6.0 to 16	3.0	15.5	643A	MFC6020

RHYTHM

Function	V_{CC} Range (Vdc)	f_{Tog} (MHz – typ)	V_{OH} (Vdc – min)	Case	Type
Dual Toggle Flip-Flop with Reset	6.0 to 16	3.0	15.5	643A	MFC6050

ATTENUATOR

Function	V_{CC} Range (Vdc)	THD (% – typ)	A_V (dB – typ)	Attenuation Range (dB – typ)	Case	Type
Electronic Attenuator	9.0 to 18	0.6	13	90	643A	MFC6040

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LINEAR

INTEGRATED CIRCUITS

PREVIEWS

INDUSTRIAL PRODUCTS

Linear ICs have traditionally found wide application in the diverse Industrial market place. Numerous types of op amps, voltage regulators, analog multipliers and timers fill important roles in process control, instrumentation, and signal processing functions. The devices previewed below complement an already substantial lineup of Motorola Industrial products.

MC3503 MC3403 Quad Operational Amplifiers

The MC3503/3403 is a quad, true differential-input operational amplifier designed for either single or split power supply (±15 V) operation.

The four internally-compensated amplifiers within a package draw a total supply current of only 2.5 mA maximum — independent of supply voltages. When the device is operated with split supplies, most specifications equal or exceed comparable parameters for the popular MC1741.

FEATURES:

- Wide supply voltage range:
  $3.0\ V \leqslant V \leqslant 36\ V$ or
  $|\pm 1.5\ V| \leqslant V \leqslant |\pm 18\ V|$
- Low power drain: 2.5 mA maximum for all four amplifiers
- Internally compensated
- Low bias currents: 200 nA maximum

MC3570 High-Slew Operational Amplifier

The MC3570G is intended for applications requiring optimum speed. It has a typical unity gain slew rate of 100 V/μs with a 30 pF load. Power bandwidth is an impressive 1.5 MHz, and unity gain crossover frequency is at 15 MHz. The units are internally compensated for unity gain stability with 30° of phase margin.

High-speed signal processing, A/D and D/A conversion, and high-frequency instrumentation are just three examples of areas which can make use of this high-speed monolithic operational amplifier.

FEATURES:

- High slew rate: 100 V/μs
- Power bandwidth = 1.5 MHz
- Unity gain crossover at 15 MHz

LINEAR-DIGITAL INTERFACE PRODUCTS

The need to span the gap between analog information and digital processing is becoming increasingly prevalent. In fact, a whole family of linear (analog)/digital interface devices has arisen in the past few years. This category is highlighted at Motorola by a number of new monolithic D/A and A/D converters. Several of the newest elements in this rapidly expanding field are the topics of the following paragraphs.

MC3537 Hex Unified Bus Receiver
MC3538 Quad Unified Bus Transceiver

Where bus-organized data transmission systems are employed, the MC3537 and MC3538 can be efficiently utilized to solve interface problems. The MC3537 contains six bus receivers, while the MC3538 contains four drivers and four receivers with each driver-receiver pair sharing common input-output pins.

Both types incorporate hysteresis in the receivers to permit excellent noise immunity, and are optimized for bus rise and fall times less than 10 μs.

FEATURES:

- Hysteresis of 1.0 V provided in receivers
- High receiver noise immunity: 2.0 V typical
- Receiver input threshold voltage insensitive to temperature changes
- MTTL-compatible logic levels
- Equivalent to DM7837 and DM7838 respectively

MC1505 Digital Voltmeter Subsystem (A/D Converter)

The MC1505 is the analog front-end portion of either a 4½ or 3½ digit DVM. It is designed for use with the MC14435 McMOS logic subsystem to produce the complete 3½ digit DVM function (excluding display). The MC1505 can also be used alone as a general purpose A/D converter.

The MC1505 uses the proven dual ramp A/D conversion technique. The subsystem consists of an on-chip voltage reference, a pair of voltage/current converters, an integrator, a current switch, a comparator, and associated control and calibration circuitry. The device requires only one capacitor and two potentiometers for operation.

FEATURES:

- Accuracies to 13 bits
- Single power supply of +5.0 to +18 V
- Accepts positive or negative input voltage
- Digital input and output both MTTL and McMOS compatible

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MC3430 thru MC3433 High-Speed Quad Comparators

Both of these comparators feature 20 ns response time and a strobe input common to the four units. However, the MC3430-31 have active pullup outputs and a three-state strobe, while the MC3432-33 are equipped with open-collector outputs.

In applications requiring numerous comparators, such as the sensing of 1103-type MOS memories, the greater package density permitted by the quad configuration results in considerable saving in circuit board space.

FEATURES:

- Response time = 20 ns typical
- Input offset voltage = 3.0 mW typical
- Choice of either three-state or open-collector outputs
- Strobe input common to all four comparators

MC3459 MC3460 Quad NMOS Memory Drivers

These quad drivers provide the interface between MTTL logic and NMOS memories. The MC3459 is a low-voltage driver for address lines while the MC3460 is a high-voltage device for driving the clock lines. The devices will drive 350 pF loads with propagation delay times of 25 ns and 35 ns respectively.

The high-voltage version uses a multiplexed pullup circuit to reduce power consumption.

FEATURES:

- Four drivers per package
- MTTL-compatible inputs
- Maximum operating frequency greater than 2.0 MHz

MC3463 Quad MECL Line Driver

The MC3463 is a quad line driver with MECL 10,000 compatible inputs. The device switches a 12 mA current sink between each of the two outputs per channel in response to the input logic condition. A pair of inhibit inputs is provided with each inhibit common to two of the channels.

Typical propagation delay time is less than 3.0 ns from the logic inputs and 5.0 ns from the inhibit inputs.

FEATURES:

- MECL 10,000 compatible
- Quad configuration
- High-speed operation
- 12 mA output current capability

MC3462 Quad MECL Line Receiver

The MC3462 is a quad MECL 10,000 compatible line receiver designed for use with the MC3463 line driver. The MC3462 has a strobe input common to all four channels, sensitivity of 8.0 mV, and propagation delay time of only 5.0 ns.

FEATURES:

- MECL 10,000 compatible
- High-speed operation
- 8.0 mV sensitivity
- ±3.0 V common mode input voltage range

CONSUMER PRODUCTS

Linear ICs are helping the consumer obtain greater functional value for his dollar. They are permitting greater performance and complexity in entertainment equipment without increasing costs. In addition, Linear IC useage is growing exponentially in automotive electronic systems to aid in solving safety and environmental problems. The following new devices are specifically conceived for use in consumer oriented products.

Radio Circuits

MC1314 Four-Channel Audio Voltage-Controlled Amplifier

The MC1314 is a gain control and balance adjustment unit for use with the CBS SQ* system decoders. It consists of four amplifiers, with the gain of each being adjustable by varying a dc voltage. Thus with four variable resistors, the master volume and L_F/R_F, L_B/R_B and F/B balance may be controlled.

The unit also has inputs which may be connected to the MC1315 logic enhancement unit to provide increased front to back separation. This feature is highly desirable in high performance four channel stereo systems.

FEATURES:
- DC controlled gain and balance
- Compatible with MC1312 decoder and MC1315 logic enhancement unit
- Excellent tracking between all four channels
- High density
- Very low output transients

MC1315 Four-Channel Audio Logic Circuit

The MC1315 provides the basic logic function for enhancing the front to back separation in the CBS SQ* four channel decoding system. The new IC is designed to interface with the MC1312 decoder and MC1314 gain control unit. The MC1315 provides variable dc logic enhancement control signals to the MC1314.

This unit extends the performance of the basic SQ system to the levels desired for top-of-the-line systems.

FEATURES:
- Provides logic enhancement to extend front to back separation to 20 dB
- Provisions for variable enhancement control
- High density

*SQ is a trademark of Columbia Broadcasting System, Inc.

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MC1356 FM Detector/Limiter

The MC1356 includes a limiting amplifier, a quadrature discriminator, and a voltage regulator. It has been designed primarily for FM receiver applications. While similar to the MC1357, it includes built-in regulation capable of supplying 20 mA to external circuitry.

FEATURES:
- Good line and load regulation
- Low harmonic distortion
- Permits single tuning coil design
- Direct replacement for μLN-2136
- Regulator is short-circuit protected

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TV Circuits

MC1359 Sound System

The MC1359 is a complete sound system for a television receiver. It includes the IF amplifier, detector, electronic volume control, and audio amplifier. The IC provides two watts of audio output. All this is packed into a single plastic package with two heat dissipating tabs.

The dc voltage-controlled volume attenuator saves the necessity of long lengths of shielded cable between the volume control and the audio amplifier circuitry. This advanced system provides 80 dB of audio attenuation range.

FEATURES:

- Excellent AM rejection
- DC volume control with 80 dB typical attenuation range
- Signal to noise ratio = 63 dB typical
- Few external components required

MC1394 Horizontal Processor (Negative Sync)

The MC1394 horizontal processor packs the phase detector, oscillator and pre-driver functions into a single, convenient 8-lead plastic package. The new unit provides the entire low-level horizontal signal processing function and may be used with either transistor or vacuum tube output stages. This device is a negative-sync version of the MC1391.

FEATURES:

- Negative sync pulse operation
- Internal shunt regulator
- Preset Hold control capability
- ±300 Hz typical pull-in range
- Balanced phase detector
- Variable output duty cycle for driving tube or transistor
- Low thermal frequency drift
- Small static phase error

MC1395/TBA395 PAL Chroma

The MC1395 forms a complete three-chip PAL chroma system when used with the MC1396 PAL luma and the MC1327 chroma demodulator.

It includes the APC detector, oscillator, ACC detector and controlled stage, PAL bistable,color killer, and burst gating.

FEATURES:

- Internal shunt regulator
- Balanced phase detector
- ±450 Hz typical pull-in range
- Low thermal frequency drift

MC1396/TBA396 PAL Luma

The MC1396 forms a complete three-chip PAL chroma system when used with the MC1395 PAL chroma and the MC1327 chroma demodulator.

It includes the chroma amplifier, chroma control, PAL delay line driver, luminance amplifier, black level clamp, and beam current limiter.

FEATURES:

- Tracking dc contrast and chroma level controls
- DC brightness control
- Beam current limiter operating on the contrast control
- Feedback black level clamp

MC13120/TBA120 FM IF Amplifier

The MC13120 is a six-stage differential amplifier/limiter, balanced coincidence detector with dc volume control designed for use in radio and TV FM/IF applications.

FEATURES:

- Low harmonic distortion
- One coil detector alignment
- DC volume control
- Excellent sensitivity

LINEAR

INTEGRATED CIRCUITS INTERCHANGEABILITY GUIDE

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INTERCHANGEABILITY GUIDE

This interchangeability guide describes equivalent circuits in two ways: (1) the "Direct Replacement" which is both electrically and mechanically a direct replacement; and, (2) the "Functional Equivalent" that is generally similar and is suggested as an alternate. When a functional equivalent circuit is used for a replacement, the specific data sheet should be consulted.

Packaging availability information for each Motorola device is listed in the Linear Application Selector Guides section and also appears on the individual data sheet for the device. Exact outline dimensions are shown in the Packaging Information section of this data book.

TYPE NUMBER	MOTOROLA DIRECT REPLACEMENT	MOTOROLA FUNCTIONAL EQUIVALENT
CA3000		MC1550G
CA3001		MC1723G
CA3002		MC1550G
CA3004		MC1550G
CA3005		MC1550G
CA3006		MC1550G
CA3007		MC1550G
CA3008		MC1709F
CA3008A		MC1709F
CA3010		MC1709G
CA3010A		MC1709G
CA3011	MC1590G	
CA3012	MC1590G	
CA3013	MC1355P	
CA3014	MC1357P	
CA3015		MC1709G
CA3015A		MC1709G
CA3016		MC1709F
CA3016A		MC1709F
CA3020		MC1554G
CA3020A		MC1554G
CA3021		MC1590G
CA3022		MC1590G
CA3023		MC1590G
CA3028A		MC1550G
CA3028B		MC1550G
CA3029		MC1709CP2
CA3029A		MC1709CP2
CA3030		MC1709CP2
CA3030A		MC1709CP2
CA3031	MC1712G	
CA3032	MC1712CG	
CA3033		MC1533L
CA3033A		MC1533L
CA3035		MC1352P
CA3037		MC1709L
CA3037A		MC1709L
CA3038	MC1709L	
CA3038A	MC1709L	
CA3040		MC1510G
CA3041		MC1351P
CA3042		MC1357P
CA3043		MC1357P
CA3047		MC1433L
CA3047A		MC1433L
CA3048		MC3401P
CA3052		MC1339P
CA3053		MC1550G
CA3055		MC1723G
CA3056		MC1741CG
CA3056A		MC1741G
CA3058		MFC8070
CA3059		MFC8070
CA3064	MC1364P	
CA3064/5A		MC1364G
CA3065	MC1358P	
CA3065/7F		MC1358PQ
CA3066		MC1398P
CA3067		MC1328P
CA3070	MC1370P	
CA3071	MC1371P	
CA3072	MC1328P	
CA3075		MC1375P
CA3076		MC1590G
CA3079		MFC8070
CA3085		MC1723G
CA3085A		MC1723G
CA3085B		MC1723G
CA3909Q		MC1310P
CA3741CT	MC1741CG	
CA3741T	MC1741G	
LH101F		MC1741F
LH101H		MC1741G
LH201H		MC1741G
LM100H		MC1723G
LM101AH	MLM101AG	
LM101H	MC1748G	
LM102H	MLM110G	
LM104H	MLM104G	
LM105H	MLM105G	
LM106H		MC1710G
LM107H	MLM107G	
LM108AH		MC1556G
LM108H		MC1556G
LM109K	MLM109K	
LM110H	MLM110G	
LM111D	MLM111L	
LM111F	MLM111F	
LM111H	MLM111G	
LM112H		MC1556G
LM118H		MC1539G
LM1303N	MC1303L	
LM1304N	MC1304P	
LM1305N	MC1305P	
LM1307N	MC1307P	
LM1310N	MC1310P	

INTERCHANGEABILITY GUIDE (continued)

TYPE NUMBER	MOTOROLA DIRECT REPLACEMENT	MOTOROLA FUNCTIONAL EQUIVALENT
LM1351N	MC1351P	
LM139AN	MC3302P	
LM139D		MC3302P
LM1414J	MC1414L	
LM1414N	MC1414L	
LM1458H	MC1458G	
LM1458N	MC1458P1	
LM1489AJ	MC1489AL	
LM1489J	MC1489L	
LM1496H	MC1496G	
LM1496N	MC1496L	
LM1514J	MC1514L	
LM1558H	MC1558G	
LM1596H	MC1596G	
LM200H		MC1723CG
LM201AH	MLM201AG	
LM201H	MC1748CG	
LM202H	MLM210G	
LM204H	MLM204G	
LM205H	MLM205G	
LM206G		MC1710CG
LM207H	MLM207G	
LM208H		MC1456G
LM209K	MLM209K	
LM210H	MLM210G	
LM211D	MLM211L	
LM211F	MLM211F	
LM211H	MLM211G	
LM2111N	MC1357P	
LM212H		MC1456G
LM218H		MC1439G
LM239AN	MC3302P	
LM239D		MC3302P
LM330H		MC1723CG
LM301AH	MLM301AG	
LM301AN	MLM301API	
LM302H	MLM310G	
LM304H	MLM304G	
LM305H	MLM305G	
LM306H		MC1710CG
LM3064H	MC1364G	
LM3064N	MC1364P	
LM3065N	MC1358P	
LM3067N		MC1328P
LM307H	MLM307G	
LM3070N	MC1370P	
LM3071N	MC1371P	
LM3075N	MC1375P	
LM308AH		MC1456G
LM308H		MC1456G
LM309K	MLM309K	
LM310H	MLM310G	
LM311D	MLM311L	
LM311F	MLM311F	
LM311H	MLM311G	
LM312H		MC1456G
LM318H		MC1439G
LM320-05K		MC7905CK
LM320-05.2K		MC7905.2CK
LM320-12K		MC7912CK
LM320-15K		MC7915CK
LM339AN	MC3302P	
LM339D		MC3302P
LM339N	MC3302P	
LM340-05K	MC7805CK	
LM340-05T	MC7805CP	
LM340-06K	MC7806CK	

TYPE NUMBER	MOTOROLA DIRECT REPLACEMENT	MOTOROLA FUNCTIONAL EQUIVALENT
LM340-06T	MC7806CP	
LM340-08K	MC7808CK	
LM340-08T	MC7808CP	
LM340-12K	MC7812CK	
LM340-12T	MC7812CP	
LM340-15K	MC7815CK	
LM340-15T	MC7815CP	
LM340-18K	MC7818CK	
LM340-18T	MC7818CP	
LM340-24K	MC7824CK	
LM340-24T	MC7824CP	
LM370H		MC1590G
LM370N		MC1350P
LM371H		MFC6010
LM376N		MFC6030A
LM380N		MFC9020
LM381N		MC1339P
LM382N		MC1339P
LM3900N	MC3401P	
LM3901N	MC3302P	
LM4250CH		MC1776CG
LM4250H		MC1776G
LM5520J		MC7520L
LM5521J		MC7521L
LM5523J		MC7523L
LM5525J		MC7525L
LM5528J		MC7528L
LM5529J		MC7529L
LM5534J		MC7534L
LM5535J		MC7535L
LM5538J		MC7538L
LM5539J		MC7539L
LM555CH	MC1455G	
LM555D	MC1455P1	
LM555H	MC1555G	
LM703LN		MFC6010
LM709CH	MC1709CG	
LM709CN	MC1709CP2	
LM709H	MC1709G	
LM710CH	MC1710CG	
LM710CN	MC1710CP	
LM710H	MC1710G	
LM711CH	MC1711CG	
LM711H	MC1711G	
LM723CD	MC1723CL	
LM723CH	MC1723CG	
LM723D	MC1723L	
LM723H	MC1723G	
LM733CD	MC1733CL	
LM733CH	MC1733C	
LM733D	MC1733L	
LM733H	MC1733G	
LM741CD	MC1741CL	
LM741CH	MC1741CG	
LM741CN	MC1741CP1	
LM741CN-14	MC1741CP2	
LM741D	MC1741L	
LM741F	MC1741F	
LM741H	MC1741G	
LM746N	MC1328P	
LM747CC	MC1747CL	
LM747D	MD1747L	
LM748CH	MC1748CG	
LM748H	MC1748G	
LM75107N		MC75107L
LM75108N		MC75108L

TYPE NUMBER	MOTOROLA DIRECT REPLACEMENT	MOTOROLA FUNCTIONAL EQUIVALENT
LM75109N		MC75109L
LM75110N		MC75110L
LM7520J	MC7520L	
LM7520N	MC7520L	
LM7521J	MC7521L	
LM7521N	MC7521L	
LM7522J	ML7522L	
LM7522N	MC7522L	
LM7523J	MC7523L	
LM7523N	MC7523L	
LM7524J	MC7524L	
LM7524N	MC7524L	
LM7525J	MC7525L	
LM7525N	MC7525L	
LM7528J	MC7528L	
LM7528N	MC7528L	
MC7529J	MC7529L	
LM7529N	MC7529L	
LM75325N	MC75325P	
LM7534J	MC7534L	
LM7534N	MC7534L	
LM7535J	MC7535L	
LM7535N	MC7535L	
LM7538J	MC7538L	
LM7538N	MC7538L	
LM7539J	MC7539L	
LM7539N	MC7539L	
LM75450AN	MC75450P	
LM75451AN	MC75451P	
LM75452N	MC75452P	
LM75453N	MC75453P	
MH0026CH	MMH0026CG	
MH0026CN	MMH0026CP1	
NE501A		MC1733CL
NE501K		MC1733CG
NE515A		MC1420G
NE515G		MC1520F
NE515K		MC1420G
NE516A		MC1420G
NE516G		MC1520F
NE516K		MC1420G
NE528B		MC1444L
NE528E		MC1444L
NE531G		MC1439G
NE531T		MC1439G
NE531V		MC1439P
NE533G		MC1776CG
NE533T		MC1776CG
NE533V		MC1776CG
NE537G		MC1456G
NE537T		MC1456G
NE540L		MFC8020A
NE550A		MFC6030A
NE550L		MC1723CG
NE555T	MC1455G	
NE555V	MC1455P1	
N5070B	MC1370P	
N5071A	MC1371P	
N5072A	MC1328P	
N5111	MC1357P	
N5556T	MC1456G	
N5556V		MC1456G
N5558F	MC1458L	
N5558T	MC1458G	
N5558V	MC1458P1	
N5595A	MC1495L	
N5595F	MC1495L	

TYPE NUMBER	MOTOROLA DIRECT REPLACEMENT	MOTOROLA FUNCTIONAL EQUIVALENT
N5596A	MC1496L	
N5596K	MC1496G	
N5709A	MC1709CP2	
N5709G	MC1709CF	
N5709T	MC1709CG	
N5709V	MC1709CP1	
N5710A	MC1710CP	
N5710T	MC1710CG	
N5711A	MC1711CP	
N5711K	MC1711CG	
N5723A		MFC6030A
N5723T	MC1723CG	
N5733K	MC1733CG	
N5741A	MC1741CP2	
N5741T	MC1741CG	
N5741V	MC1741CP1	
N5747A	MC1747CL	
N5747F	MC1747CL	
N5748A		MC1747CG
N5748T	MC1748CG	
N7520B	MC7520P	
N7521B	MC7521P	
N7522B	MC7522P	
N7523B	MC7523P	
N7524B	MC7524P	
N7525B	MC7525P	
PA239A	MC1339P	
SE501K		MC1733G
SE515G		MC1520F
SE515K		MC1520G
SE516A		MC1520G
SE516G		MC1520F
SE516K		MC1520G
SE528E		MC1544L
SE528R		MC1544L
SE531G		MC1539G
SE531T		MC1539G
SE533G		MC1776G
SE533T		MC1776G
SE537G		MC1556G
SE537T		MC1556G
SE540L		MFC8020A
SE550L		MC1723G
SE555T	MC1555G	
SN52101AL	MLM101AG	
SN52107L	MLM107G	
SN52558L	MC1558G	
SN52702F	MC1712F	
SN52702L	MC1712G	
SN52702Z	MC1712F	
SN52709F	MC1709F	
SN52709L	MC1709G	
SN52710J	MC1710L	
SN52710L	MC1710G	
SN52710N	MC1710P	
SN52710S	MC1710F	
SN52711J	MC1711L	
SN52711L	MC1711G	
SN52711S	MC1711F	
SN52733L	MC1733G	
SN52741J	MC1741L	
SN52741L	MC1741G	
SN52741Z	MC1741F	
SN52747J	MC1747L	
SN52748J		MC1748G
SN52748L	MC1748G	
SN52770L		MC1556G

INTERCHANGEABILITY GUIDE (continued)

TYPE NUMBER	MOTOROLA DIRECT REPLACEMENT	MOTOROLA FUNCTIONAL EQUIVALENT
SN52771L		MC1556G
SN5510F	MC1510F	
SN5510L	MC1510G	
SN55107J	MC55107L	
SN55108J	MC55108L	
SN55109J		MC75109L
SN5511F		MC1510F
SN5511L		MC1510G
SN55110J		MC75110L
SN5524J		MC7524L
SN5525J		MC7524L
SN552702N	MC1712L	
SN56514L		MC1596G
SN72301AL	MLM301AG	
SN72301AN	MLM301AP1	
SN72301AP	MLM301AP1	
SN72307L	MLM307G	
SN72558L	MC1458G	
SN72558P	MC1458P1	
SN72611S	MC1711CF	
SN72702F	MC1712CF	
SN72702L	MC1712CG	
SN72702N	MC1712CL	
SN72709L	MC1709CG	
SN72709N	MC1709CP2	
SN72709P	MC1709CP1	
SN72709S	MC1709CF	
SN7271N	MC1711CP2	
SN72710J	MC1710CL	
SN72710L	MC1710CG	
SN72710N	MC1710CP2	
SN72710S	MC1710CF	
SN72711J	MC1711CL	
SN72711L	MC1711CG	
SN72720N	MC1414L	
SN72733L	MC1733CG	
SN72733N	MC1733CL	
SN72741J	MC1741CL	
SN72741L	MC1741CG	
SN72741N	MC1741CP2	
SN72741P	MC1741CP1	
SN72741Z	MC1741CF	
SN72747J	MC1747CL	
SN72747N	MC1747CL	
SN72748L	MC1748CG	
SN72770L		MC1456G
SN72771L		MC1456G
SN7510F	MC1410F	
SN7510L	MC1410G	
SN75107J	MC75107L	
SN75107N	MC75107L	
SN75108J	MC75109L	
SN75108N	MC75108L	
SN75109J	MC75109L	
SN75109N	MC75109L	
SN7511L		MC1410G
SN75110J	MC75110L	
SN75110N	MC75110L	
SN75140P	MC75140P1	
SN75150J		MC1488L
SN75150N		MC1488L
SN75188J	MC1488L	
SN75189J	MC1489L	
SN7520J	MC7520L	
SN7520N	MC7520L	
SN7521J	MC7521L	
SN7521N	MC7521L	

TYPE NUMBER	MOTOROLA DIRECT REPLACEMENT	MOTOROLA FUNCTIONAL EQUIVALENT
SN7522J	MC7522L	
SN7522N	MC7522L	
SN7523J	MC7523L	
SN7523N	MC7523L	
SN75234J	MC75234L	
SN75235J	MC75235L	
SN75238J	MC75238L	
SN75239J	MC75239L	
SN7524J	MC7524L	
SN7524N	MC7524L	
SN7525J	MC7525L	
SN7525N	MC7525L	
SN7528J	MC7528L	
SN7528N	MC7528L	
SN7529J	MC7529L	
SN7529N	MC7529L	
SN75325J	MC75325L	
SN75450AN		MC75450P2
SN75450N	MC75450P2	
SN75451AP		MC75451P
SN75451P	MC75451P	
SN75452P	MC75452P	
SN75453P	MC75453P	
SN75454P	MC5454P	
SN75491N	MC75491P	
SN75492N	MC75492P	
SN76104N	MC1304P	
SN76105N	MC1305P	
SN76107N	MC1370P	
SN76242N	MC1370P	
SN76243N	MC1371P	
SN76246N	MC1328P	
SN76514L		MC1496G
SN76514N		MC1496L
SN76530P	MC1330P	
SN76564N	MC1364P	
SN76600P	MC1350P	
SN76642N	MC1357P	
SN76650N	MC1352P	
SN76651N	MC1351P	
SN76653N	MC1353P	
SN76665N	MC1353P	
SN76675N	MC1375P	
S5556T	MC1556G	
S5558F	MC1558L	
S5558T	MC1558G	
S5596F	MC1596L	
S5596K	MC1596G	
S5709G	MC1709F	
S5709T	MC1709G	
S5710T	MC1710G	
S5711K	MC1711G	
S5723T	MC1723G	
S5733K	MC1733G	
S5741T	MC1741G	
55325D	MC55325L	
702DC	MC1712CL	
702DM	MC1712L	
702FC	MC1712CF	
702FM	MC1712F	
702HC	MC1712CG	
702HM	MC1712G	
703HC		MFC6010
703HM		MFC6010
709DC	MC1709CL	
709DM	MC1709L	

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INTERCHANGEABILITY GUIDE (continued)

TYPE NUMBER	MOTOROLA DIRECT REPLACEMENT	MOTOROLA FUNCTIONAL EQUIVALENT
709FC	MC1709CF	
709FM	MC1709F	
709HC	MC1709CG	
709HM	MC1709G	
710DC	MC1710CL	
710DM	MC1710L	
710FC	MC1710CF	
710FM	MC1710F	
710HC	MC1710CG	
710HM	MC1710G	
711DC	MC1711CL	
711DM	MC1711L	
711FC	MC1711CF	
711FM	MC1711F	
711HC	MC1711CG	
711HM	MC1711G	
719HC		MC1357P
719HM		MC1357P
723DC	MC1723CL	
723DM	MC1723L	
723HC	MC1723CG	
723HM	MC1723G	
729DC		MC1305P
732DC		MC1304P
733DC	MC1733CL	
733DM	MC1733L	
733FC	MC1733CF	
733FM	MC1733F	
733HC	MC1733CG	
733HM	MC1733G	
739DC		MC1303P
739DM		MC1303P
741DC	MC1741CL	
741DM	MC1741L	
741FC	MC1741CF	
741FM	MC1741F	
741HC	MC1741CG	
741HM	MC1741G	
741TC	MC1741CP1	
746DC		MC1328P
746HC		MC1328P
747DC	MC1747CL	
747DM	MC1747L	
747HC	MC1747CG	
747HM	MC1747G	
748HC	MC1748CG	
748HM	MC1748G	
7524DC	MC7524L	
7525DC	MC7525L	
75325D	MC75325L	
75325P	MC75325P	
754DC		MC1355P
754HC		MC1355P
754TC		MC1355P
757DC		MC1350P
757DM		MC1350P
767DC		MC1307P
776HC	MC1776CG	
776HM	MC1776G	
780DC		MC1370P
7805KC	MC7805CK	
7805UC	MC7805CP	
7806KC	MC7806CK	
7806UC	MC7806CP	
7808KC	MC7808CK	
7808UC	MC7808CP	
781DC		MC1371P
7812KC	MC7812CK	
7812UC	MC7812CP	
7815KC	MC7815CK	
7815UC	MC7815CP	
7818KC	MC7818CK	
7818UC	MC7818CP	
7824KC	MC7824CK	
7824UC	MC7824CP	
796HC	MC1496G	
796HM	MC1596G	

LINEAR

INTEGRATED CIRCUITS

CHIP INFORMATION

6

6

LINEAR INTEGRATED CIRCUIT

CHIPS

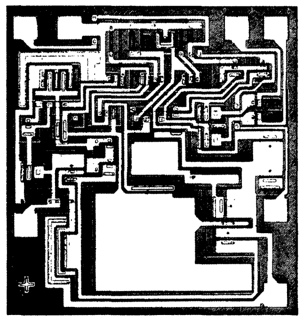
Most of the linear integrated circuit devices in this Data Book are available in chip form. Many are offered in several options – such as conventional (face up bonding), beam lead, and flip-chip versions. Motorola offers many standard linear chips from warehouse stock either directly from the factory or through franchised distributors. In addition, custom linear IC chips may be designed and produced to meet a specific need.

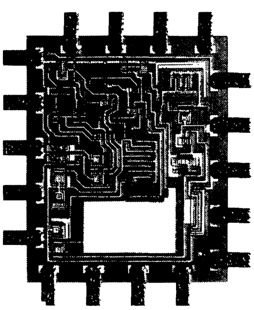
Specific information on chip processing, testing, and handling can be obtained in the **Semiconductor Chips Data Book.**

Electrical limits for stocked linear IC chips in conventional, beam lead, and flip-chip formats are included on data sheets in this book. *(See page 6-4 for listing of stocked chips.)*

LINEAR CHIP FORMATS

Conventional Chips encompass by far the greatest number of available linear IC chips. These silicon chips use gold backside metalization for easy eutectic bonding to the metalized area of hybrid assemblies. The interconnecting metalization and bonding pad areas are formed from evaporated aluminum. Either gold or aluminum wire may be employed for connection between on-chip bonding pads and the external circuit.





Beam-Lead Chips are distinguished from conventional chips by the presence of cantilevered beams used to interconnect the chip circuit element with the substrate circuit bonding pads. In production, a complex integrated circuit chip with a large number of interconnecting beams can be connected to the substrate, forming all necessary interconnections in a single operation, using wobble-bonding techniques. In addition, the entire surface of a beam-lead chip, except the beams, is covered with a passivating layer of silicon nitride that is as effective as a hermetically sealed package in protecting the circuit against contamination.

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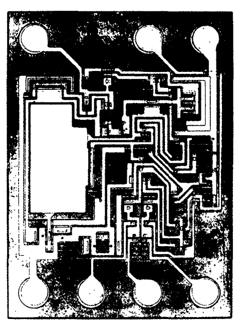
Flip-Chips, like beam-lead chips, can be mounted to a hybrid substrate in a single operation.

In the case of flip-chips, connection to the substrate bonding pads is made by means of raised "solder bumps" that protrude above the chip surface at the integrated-circuit bonding pads. The devices are mounted to the substrate metalization areas circuit side down by means of conventional reflow solder techniques.



STOCK CHIP AVAILABILITY

All of the chip options listed below are stock items. In addition, nearly all linear devices are available in chip form. Generally these chips are specified only at room temperature (25°C).

Packaged Device Part Number	Standard Chip Part Number*	Beam-Lead Chip Part Number#	Flip-Chip Part Number*
MC1436	MCC1436		
MC1536	MCC1536		
MC1439	MCC1439		
MC1539	MCC1539		
MC1458	MCC1458		MCCF1458
MC1558	MCC1558		MCCF1558
MC1463	MCC1463		
MC1563	MCC1563		
MC1469	MCC1469		
MC1569	MCC1569		
MC1495	MCC1495		
MC1595	MCC1595		
MC1709	MCC1709	MCBC1709	MCCF1709
MC1709C	MCC1709C		MCCF1709C
MC1710	MCC1710	MCBC1710	
MC1710C	MCC1710C		
MC1711	MCC1711		
MC1711C	MCC1711C		
MC1723	MCC1723	MCBC1723	
MC1723C	MCC1723C		
MC1741	MCC1741	MCBC1741	MCCF1741
MC1741C	MCC1741C		MCCF1741C
MC1748	MCC1748	MCBC1748	
MC1748C	MCC1748C		

*Standard chips and flip-chips are sold only in multiples of 10 or 100. Add -1 to part number when ordering multiples of 10; add -2 to part number when ordering multiples of 100.

#Beam-lead devices are sold only in multiples of 5.

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LINEAR

INTEGRATED CIRCUITS

MIL-M-38510 PROGRAM

7

7

MIL-M-38510
LINEAR INTEGRATED CIRCUITS

Under the MIL-M-38510 program, Motorola linear integrated circuits may be procured to the specifications of MIL-M-38510 and to four levels of processing which meet the screening requirements of MIL-STD-883.

This comprehensive program is structured to provide an environment in which proven methods of manufacturing, quality assurance, monitoring, screening, and testing can produce the most reliable product on the market. Because it is a "standard" hi-rel program, it is designed to facilitate delivery and to minimize specification preparation time.

Motorola has qualified a variety of linear integrated circuits under the MIL-M-38510 program. These device types are available (more will be available during 1974) as JAN-QUALIFIED product. These devices have specific detailed specifications called "slash specs".

In addition, nearly all full-temperature-range linear device types are available as JAN-PROCESSED product with the same MIL-M-38510 processing sequences as Qualified product, but with other requirements as listed on page 7-5.

Further details and specific processing information can be obtained from your Motorola representative.

Note that this program supercedes the Checkmate high-reliability processing program.

MIL-M-38510 JAN-QUALIFIED PRODUCT

JAN-QUALIFIED devices are built to the stringent specifications outlined by the Defense Electronics Supply Center (DESC). These devices must be manufactured in a government-approved facility and are screened to electrical limits outlined in government documents referred to as "slash sheets". These specifications may differ from standard Motorola electrical limits as stated in the device data sheets.

MAJOR REQUIREMENTS OF JAN-QUALIFIED PRODUCT

1. G.S.I. (Government Source Inspection) provided upon request.
2. Must be manufactured in a Government approved facility.
3. Product inventoried in distributor and OEM warehouses.

LINEAR ICs QUALIFIED or In Process of Qualification

MIL-M-38510 Device Type	Motorola Source Device Type
JM38510/10101BCG BGC BHB	MC1741
JM38510/10102BAB BCB BIC	MC1747
JM38510/10103BGC	MLM101A
JM38510/10104BAB BCB BGC	MLM108
JM38510/10201BCB BHB BIC	MC1723
JM38510/10301BCB BGC BHB	MC1710
JM38510/10302BCB BHB BIC	MC1711
JM38510/10304BCB BGC BHB	MLM111
JM38510/10401BCB	MC55107
JM38510/10402BCB	MC55108

HOW TO ORDER MIL-M-38510 JAN-QUALIFIED PRODUCT

Military Part No.

A typical military part number consists of the following elements:

J	M38510	/XXX	XX	B	C	B
(1)	(2)	(3)	(4)	(5)	(6)	(7)

(1) J – This indicates a qualified device.

(2) M38510 – This is the military designator.

(3) /XXX – This three-digit number signifies the detail specification ("slash spec") in which the device type is found. This specification generally contains more than one device type and is written for various generic groupings (i.e., Op Amps, Voltage Regulators, etc.).

(4) XX – This two-digit number identifies the device type within the detail specification.

(5) B – This is a single letter and specifies the device class per MIL-M-38510 and will be class A, B, or C.

(6) Case outline (see listing on page 7-5).

(7) Lead finish (see listing on page 7-5).

Motorola Part No.

The Motorola equivalent of the JAN M38510 part number is as follows, and should be referenced when ordering your specific device requirement:

MCXXXX	BCB	J
(1)	(2)	(3)

(1) The MCXXXX designates the Motorola source device type.

(2) The first three letters after the part number have the same meaning and order as in the JAN part numbering system; this will simplify your cross-referencing.

(3) J, which is the last letter in the part number, designates a JAN-QUALIFIED device.

Example:

Order No.: MC1741BCBJ
Device Marking: JM38510/10101BCB

MIL-M-38510 JAN-PROCESSED PRODUCT

JAN-PROCESSED product is intended to assure the same high reliability manufacturing sequences as JAN-Qualified devices, but without the requirement for government source inspection. JAN-Processed devices are available tested to either "slash-sheet" limits or to Motorola data sheet electrical limits. This part of the program replaces the Motorola Checkmate hi-rel program and encompasses all military-temperature-range linear ICs rather than just those covered under existing "slash sheets".

MAJOR REQUIREMENTS OF JAN-PROCESSED PRODUCT

1. No G.S.I. provided.
2. Government-approved facility not required.
3. Product supplied with MIL-M-38510 electrical specifications will be designated by an "M" suffix.
4. Product supplied with Motorola standard data sheet electrical specifications will be designated by an "S" suffix.
5. Devices will be manufactured using design and processing guidelines contained in MIL-M-38510.
6. Inventories will be maintained prior to burn-in and final electrical tests.

DESIGNATIONS COMMON TO BOTH JAN-QUALIFIED AND JAN-PROCESSED PRODUCTS

Case Outline Designator

#A	1/4" x 1/4" flat pack, 14 pin
B	1/8" x 1/4" flat pack, 14 pin
C	1/4" x 3/4" dual-in-line, 14 pin
#D	1/4" x 3/8" flat pack, 14 pin
E	1/4" x 3/4" dual-in-line, 16 pin
F	1/4" x 3/8" flat pack, 16 pin
G	8 lead can
H	1/4" x 1/4" flat pack, 10 pin
I	10 lead can
J	1/2" x 1-1/4" dual-in-line, 24 pin
K	3/8" x 1/2" flat pack, 24 pin
Z	1/4" x 1/2" flat pack, 24 pin

#A and D outlines are interchangeable

Lead Material and Finish

A	Kovar or Alloy 42, with hot solder dip
B	Kovar or Alloy 42, with bright acid tin plate
C	Kovar or Alloy 42, with gold plate

HOW TO ORDER MIL-M-38510 JAN-PROCESSED PRODUCT

Motorola Part No.

The part number for ordering a JAN-Processed device consists of the following elements:

MCXXXX	B	C	B	S
(1)	(2)	(3)	(4)	(5)

(1) The MCXXXX designates the Motorola source device type.

(2) B — This is a single letter and specifies the device class per MIL-M-38510 for classes A, B, and C. Class D is an added Motorola JAN-Processing class and is the same as the MIL-M-38510 Class B except for the differences shown in the Screening Procedures table.

(3) Case outline (see listing on this page).

(4) Lead finish (see listing on this page).

(5) S — This is a single letter and specifies the electrical specifications to which the device is to be screened during electrical testing, and will be either an S or M. An S specifies the use of Motorola standard data sheet electrical specifications. An M specifies the use of JAN "slash sheet" electrical specifications where they exist.

Example:

Order No.: MC1741BCB (M or S)
Device Marking: MC38510/1741BCB (M or S)

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SCREENING PROCEDURES
(To MIL-STD-883 Requirements)

This program establishes screening procedures for total lot screening of integrated circuits to assist in achieving levels of quality and reliability commensurate with the intended application. In recognition of the fact that the level of screening has a direct impact on the cost of the product as well as its quality and reliability, four standard levels of screening are provided to coincide with four device classes or levels of product assurance.

Flexibility is provided in the choice of conditions and stress levels to provide screens, tailored to a particular product or application. Selection of a level **better** than that required for the specific product and application will, of course, result in unnecessary expense. A level **less** than that required will result in an unwarranted risk that reliability and other requirements will not be met. For general hi-rel applications, the Class B screening level should be considered.

	CLASS A		CLASS B		CLASS C		CLASS D	
SCREEN	METHOD	RQMT	METHOD	RQMT	METHOD	RQMT	METHOD	RQMT
Internal Visual (Precap)	2010 Cond A and 38510	100%	2010 Cond B and 38510	100%	2010 Cond B and 38510	100%	2010 Cond B and 38510	100%
Stabilization Bake	1008 24 hrs min, test condition C	100%	1008, 24 hrs min, test condition C	100%	1008, 24 hrs min, test condition C	100%	1008, 24 hrs min, test condition C	100%
Thermal Shock	1011, Cond A	100%		—		—		—
Temperature Cycling	1010, Cond C	100%	1010, Cond C	100%	1010 Cond C	100%	1010, Cond C	100%
Mechanical Shock	2002 Cond F One Shock in Y_1 plane only **or** 5 shocks at Cond B in Y_1 plane	100%		—		—		—
Constant Acceleration	2001 Cond E (min) in Y_2 plane then Y_1 plane	100%	2001 Cond E (min) Y_1 plane	100%	2001 Cond E (min) Y_1 plane	100%	2001 Cond E (min) Y_1 plane	100%
Seal (a) Fine (b) Gross	1014	100%	1014	100%	1014	100%	1014	100%
Interim Electrical Parameters	JAN slash-sheet electrical specification unless otherwise designated	100%	JAN slash-sheet electrical specifications unless otherwise designated	100%		—	Motorola stand. data sheet electrical specs unless otherwise indicated	100%
Burn-in test	1015 240 hrs @ 125°C min	100%	1015 168 hrs @ 125°C min	100%		—	1015 168 hrs @ 125°C min	100%
Interim Electricals	JAN slash-sheet electrical specifications unless otherwise designated	100%						
Reverse Bias Burn-in	1015 Cond A or C 72 hrs at 150°C min	100%						
Final Electrical tests (a) Static tests (1) 25°C (Subgroup 1 table 1 5005)	JAN slash-sheet electrical specifications unless otherwise designated	100%	JAN slash-sheet electrical specifications unless otherwise designated	100%	JAN slash-sheet electrical specifications unless otherwise designated	100%	Motorola stand. data sheet electrical specs unless otherwise indicated	100%
(2) Max and min rated op. temperature (subgroups 2 and 3 table 1, 5005)		100%		100%		—		—
(b) Dynamic tests and/or switching tests 25°C (subgroup 4 and 9 table 1, 5005)		100%		100%		—		—
(C) Functional test 25°C (subgroup 7 table 1, 5005)		100%		100%		100%		100%
Radiographic	2012	100%		—		—		—
Qualification or quality conformance inspection	5005 Class A	per 38510 *	5005 Class B	per 38510 *	5005 Class C	per 38510 *	5005 Class B	*
External Visual	2009	100%	2009	100%	2009	100%	2009	100%

*Group A per 5005, Generic data available for groups B & C on devices produced to Class B, C, D for JAN processed (from JAN program)

LINEAR

INTEGRATED CIRCUITS

DATA SHEETS

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MC1303L

DUAL STEREO PREAMPLIFIER

MONOLITHIC DUAL STEREO PREAMPLIFIER

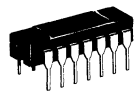
. . . designed for amplifying low-level stereo audio signals with two preamplifiers built into a single monolithic semiconductor.

Each Preamplifier Features:

- Large Output Voltage Swing – 4.0 V(rms) min
- High Open-Loop Voltage Gain = 6000 min
- Channel Separation = 60 dB min at 10 kHz
- Short-Circuit-Proof Design

DUAL STEREO PREAMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

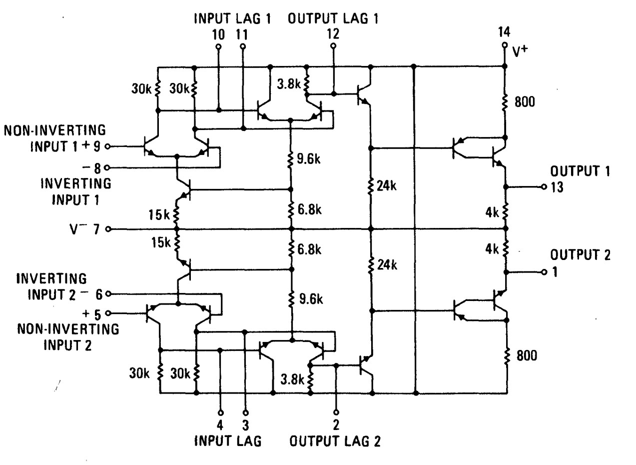


CERAMIC PACKAGE
CASE 632
TO-116

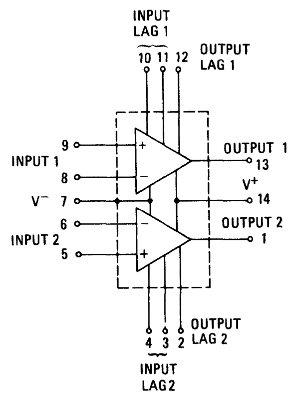
MAXIMUM RATINGS (T_A = + 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+15 -15	Vdc Vdc
Power Dissipation (Package Limitation) Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

CIRCUIT SCHEMATIC

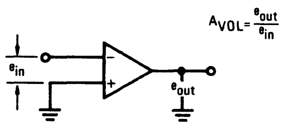
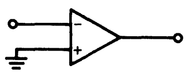
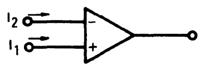
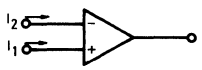
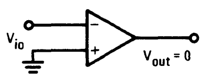
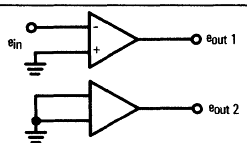


EQUIVALENT CIRCUIT



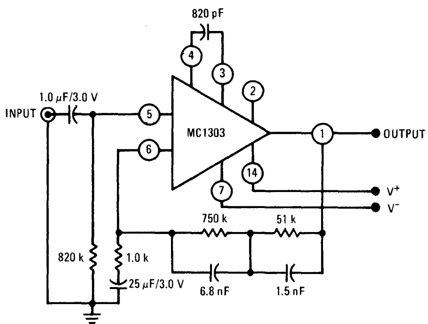
See Packaging Information Section for outline dimensions.

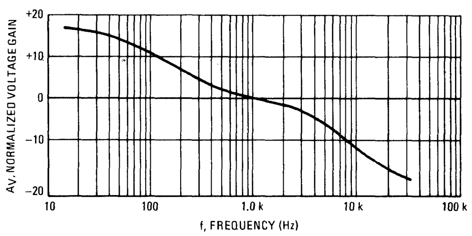
ELECTRICAL CHARACTERISTICS (Each Preamplifier) (V^+ = +13 Vdc, V^- = -13 Vdc, T_A = +25°C unless otherwise noted)

Characteristic Definitions (linear operations)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain	A_{VOL}	6,000	10,000	-	V/V
	Output Voltage Swing (R_L = 10 kΩ)	V_{out}	4.0	5.5	-	V(rms)
	Input Bias Current $I_b = \frac{I_1 + I_2}{2}$	I_b	-	1.0	10	μA
	Input Offset Current ($I_{io} = I_1 - I_2$)	I_{io}	-	0.2	0.4	μA
	Input Offset Voltage	V_{io}	-	1.5	10	mV
	DC Power Dissipation (Power Supply = ±13 V, V_{out} = 0)	P_D	-	-	400	mW
	Channel Separation (f = 10 kHz)	$\frac{e_{out\,1}}{e_{out\,2}}$	60	70	-	dB

TYPICAL PREAMPLIFIER APPLICATIONS

FIGURE 1 – MAGNETIC PHONO PLAYBACK PREAMPLIFIER/RIAA EQUALIZED

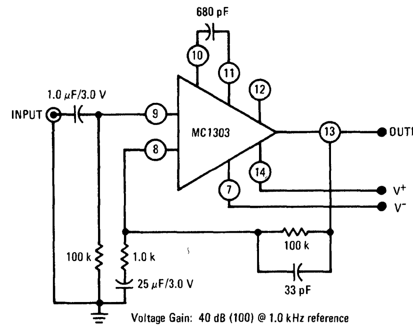




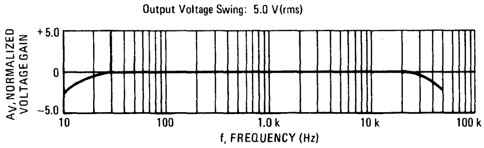
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain	: 34 dB (50) @ 1.0 kHz
Input Overload Point	: 100 mVrms @ 1.0 kHz
Output Voltage Swing	: 5.0 Vrms @ 1.0 kHz @ 0.1% THD.
Output Noise Level	: Better Than 70 dB Below 10 mV Phono Input (Input Shorted)

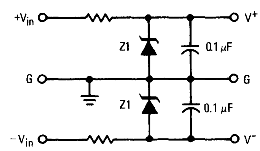
FIGURE 2 – BROADBAND AUDIO AMPLIFIER



Voltage Gain: 40 dB (100) @ 1.0 kHz reference
Output Voltage Swing: 5.0 V(rms)

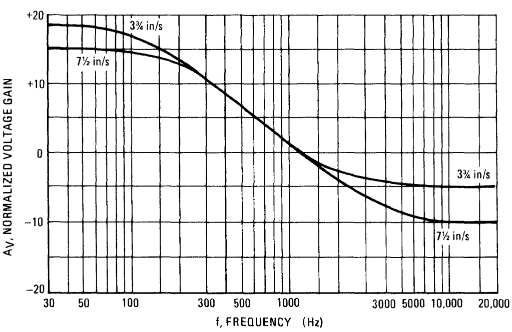


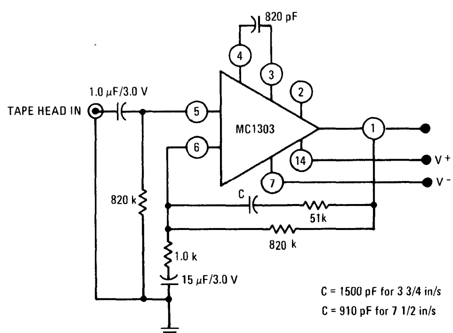
SUGGESTED POWER SUPPLY CIRCUIT



Z1 = MZ-500-19 (13 V nom.)
Select series R by allowing 11 mA for zener, and each dual I/C Preamplifier

FIGURE 3 – NAB TAPE HEAD EQUALIZATION





C = 1500 pF for 3 3/4 in/s
C = 910 pF for 7 1/2 in/s

Voltage Gain: 35 dB @ 1.0 kHz
Output Voltage Swing: 5.0 V(rms)

8

FIGURE 4 – POWER DISSIPATION versus SUPPLY VOLTAGE

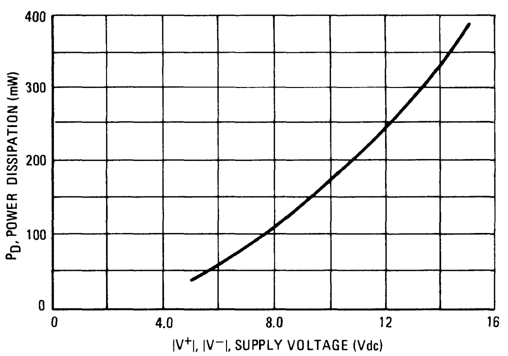


FIGURE 5 – OUTPUT LINEARITY

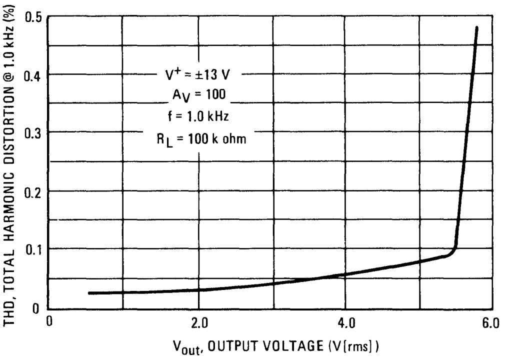
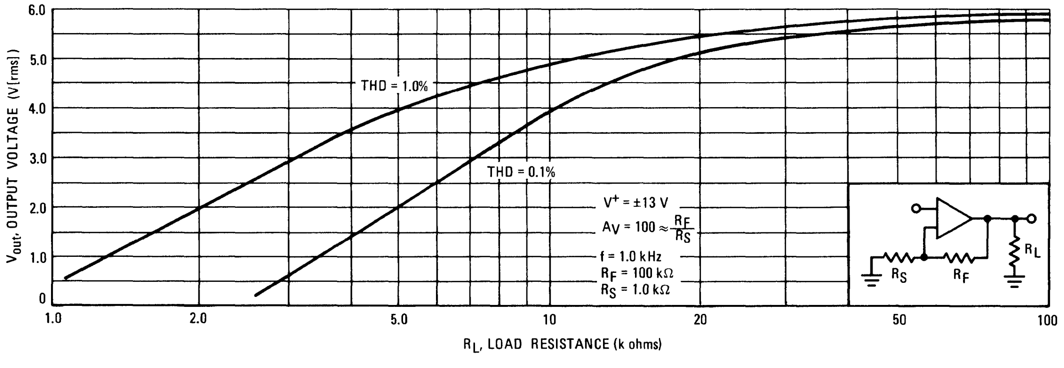


FIGURE 6 – INFLUENCE OF OUTPUT LOADING



NOISE CHARACTERISTICS

FIGURE 7A – INFLUENCE OF SOURCE RESISTANCE & BANDWIDTH

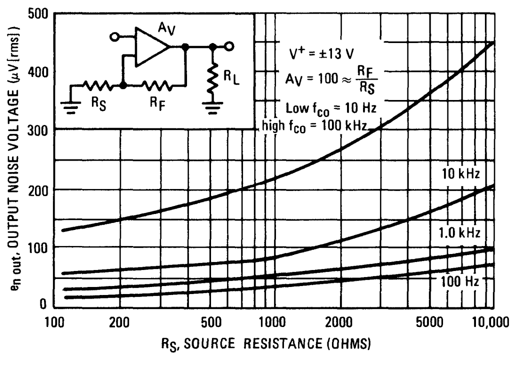
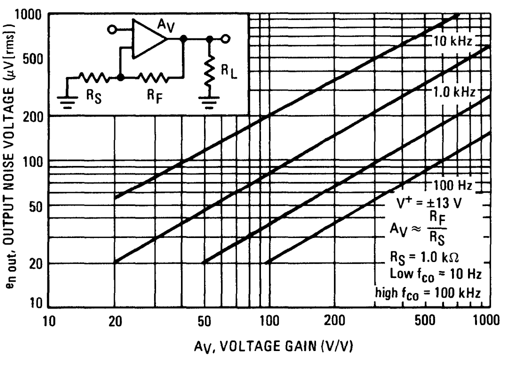


FIGURE 7B – INFLUENCE OF VOLTAGE GAIN & BANDWIDTH



8

MC1304P
MC1305P

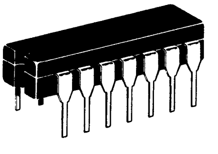
MONOLITHIC FM MULTIPLEX STEREO DEMODULATORS

. . . derive the left and right audio information from the detected composite signal. The MC1304P eliminates the need for an external stereo-channel separation control. The MC1305P is similar to the MC1304P but permits the use of an external stereo-channel separation control for maximum separation.

- Operation Practicable Over Wide Power-Supply Range, 8-14 Vdc
- Built-in Stereo-Indicator Lamp Driver
- Total Audio Muting Capability
- Automatic Switching – Stereo-Monaural
- Monaural Squelch Capability

FM MULTIPLEX STEREO DEMODULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS



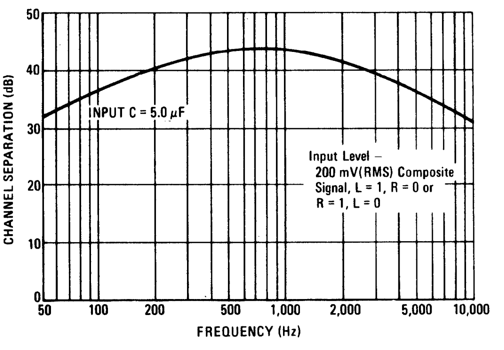
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

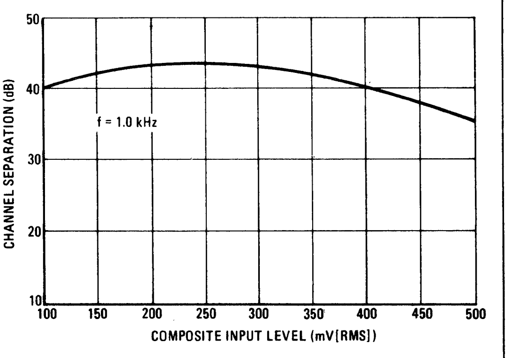
Rating	Value	Unit
Power Supply Voltage (Pins 1, 6, 9,*11, 12) (Pin 7 is grounded)	+22	Vdc
Lamp Driver Current	40	mAdc
Power Dissipation (Package Limitation) Plastic Package	625	mW
Derate above T_A = 25°C	5.0	mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

*Pin 8 for MC1305P

CHANNEL SEPARATION versus FREQUENCY



CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL



See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted. Test made with 75 μs de-emphasis network (3.9 kΩ, 0.02 μF) unless otherwise noted).

Characteristics	Min	Typ	Max	Unit
Input Impedance (f = 20 Hz)	12	20	–	kΩ
Stereo Channel Separation (See Notes 1 and 2) (f = 100 Hz) (f = 1.0 kHz) (f = 10 kHz)	– – –	35 45 30	– – –	dB
Channel Balance (Monaural Input = 200 mV[RMS]), (Monaural, Left and Right Outputs)	–	0.5	–	dB
Total Harmonic Distortion (See Notes 1 and 3) (Modulation frequency - 1.0 kHz)	–	0.5	1.0	%
Ultrasonic Frequency Rejection (See Note 4) (19 kHz) (38 kHz)	– –	25 20	– –	dB
Inherent SCA Rejection (without filter) @ 60 kHz, 67 kHz and 74 kHz	–	50	–	dB
Lamp Indicator (R_A = 120Ω) Minimum 19 kHz Input Level for lamp on Maximum 19 kHz Input Level for lamp off	– 5.0	16 14	25 –	mV(RMS)
Audio Muting Mute on (Voltage required at pin 5) Mute off (Voltage required at pin 5) Attentuation in Mute Mode (Note 5)	0.6 1.3 –	– – 55	1.0 2.0 –	Vdc Vdc dB
Stereo-Monaural Switching Stereo (Voltage required at pin 4) Monaural (Voltage required at pin 4)	1.3 –	– –	2.0 1.0	Vdc
Power Dissipation (V_{CC} = 10 V) (Without lamp) (With lamp)	– –	150 180	300 300	mW

Note 1 – Measurement made with 200 mV(RMS) Standard Multiplex Composite Signal and L = 1, R = 0 or R = 1, L = 0. Standard Multiplex Composite signal is here defined as a signal containing left and/or right audio information with a 10% (19 kHz) pilot signal in accordance with FCC regulations.

Note 2 – Stereo channel separation is adjustable for the MC1305P with a resistor from pin 9 to ground.

Note 3 – Distortion specification also applies to Monaural Signal.

Note 4 – Referenced to 1.0 kHz output signal with Standard Multiplex Composite Input Signal.

Note 5 – This is referenced to 1.0 kHz output signal with either Standard Multiplex Composite Signal or Monaural Input Signal.

FIGURE 1 – DISTORTION COMPONENTS IN AUDIO SIGNAL

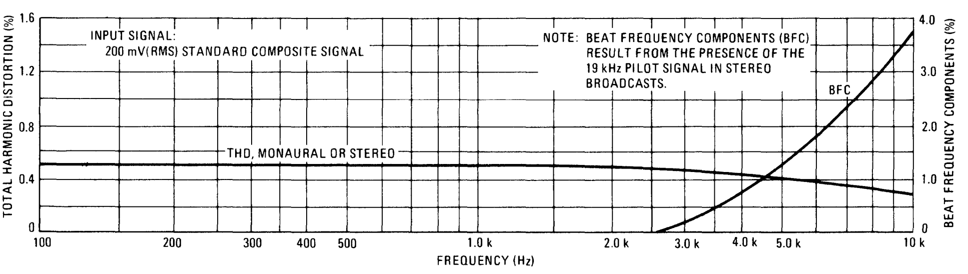


FIGURE 2 – TOTAL HARMONIC DISTORTION

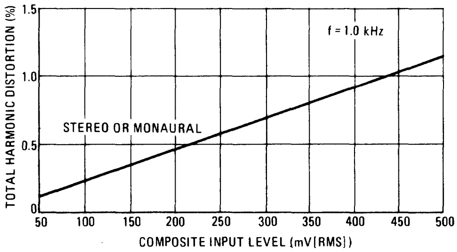
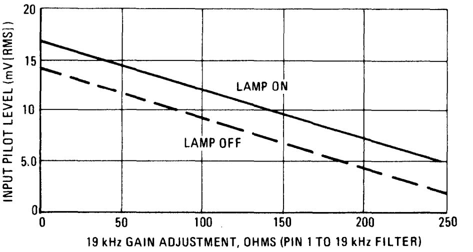


FIGURE 3 – MULTIPLEX SENSITIVITY



8

FIGURE 4 – MC1304 CIRCUIT SCHEMATIC

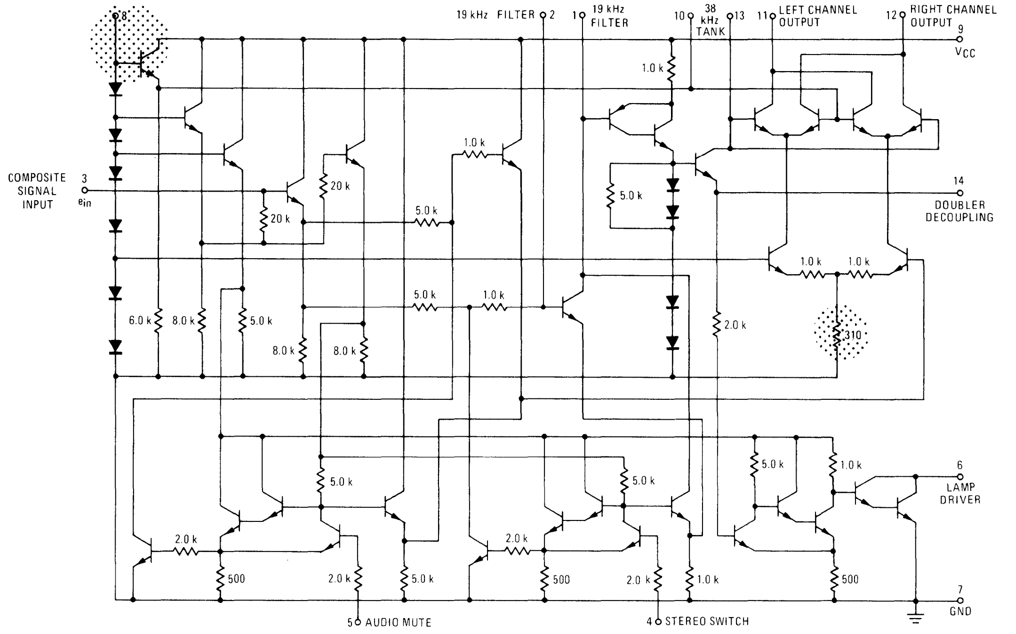
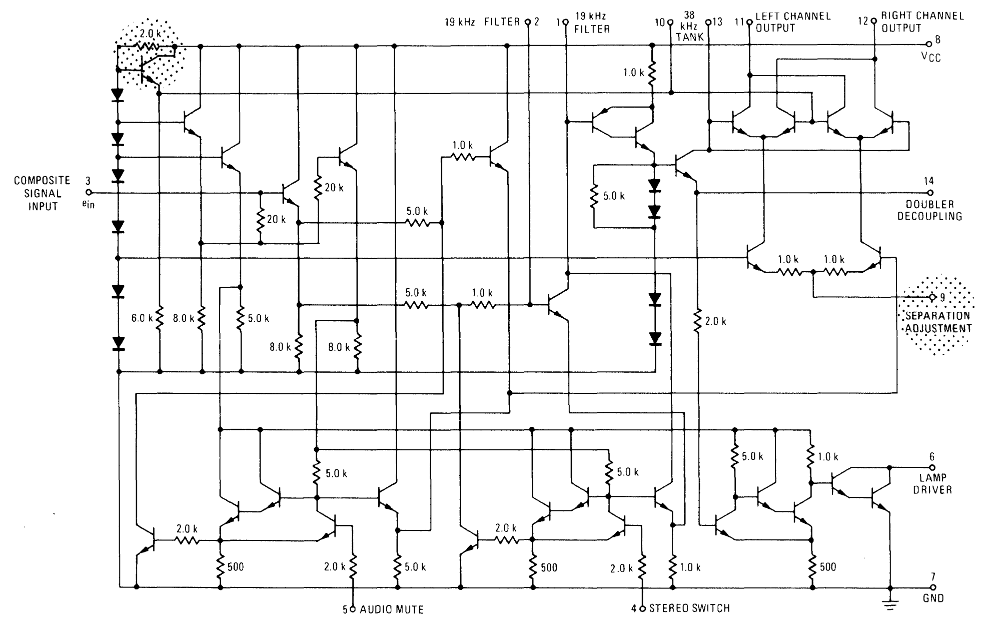


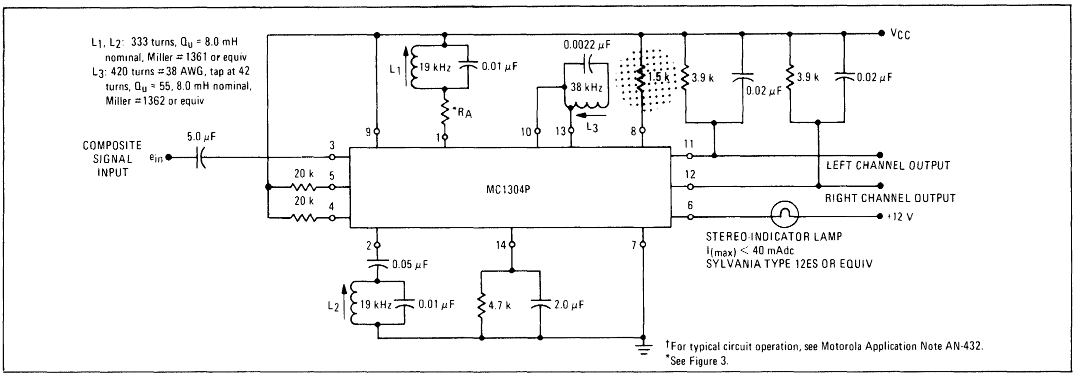
FIGURE 5 – MC1305 CIRCUIT SCHEMATIC



Portions of the circuits shown within the dotted areas pertain to the MC1304P or MC1305P as indicated by the titles of the circuits.

8

FIGURE 6 – MC1304P TYPICAL CIRCUIT CONFIGURATION†

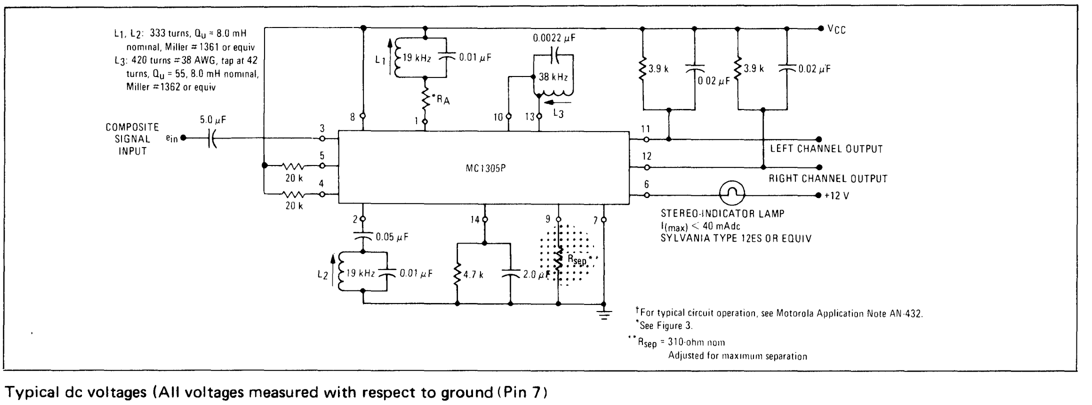


Typical dc voltages (All voltages measured with respect to ground, Pin 7, R_A = 0)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
V_{CC} = 8.5 Vdc	8.5	2.0	2.8	1.6	1.6	0.8	0	4.6*	8.5	3.9	6.3	6.3	3.9	1.9
V_{CC} = 12 Vdc	12	2.0	2.8	1.9	1.9	0.8	0	4.6**	12	3.9	9.7	9.7	3.9	1.9

*1.5 kΩ in series with pin 8
**2.7 kΩ in series with pin 8

FIGURE 7 – MC1305P TYPICAL CIRCUIT CONFIGURATION†



Typical dc voltages (All voltages measured with respect to ground (Pin 7)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
V_{CC} = 8.5 Vdc	8.5	2.0	2.8	1.6	1.6	0.8	0	8.5	0.32	3.9	6.3	6.3	3.9	1.9
V_{CC} = 12 Vdc	12	2.0	2.8	1.9	1.9	0.8	0	12	0.36	3.9	9.7	9.7	3.9	1.9

Portions of the circuits shown within the dotted areas pertain to the MC1304P or MC1305P as indicated by the titles of the circuits.

8

MC1306P

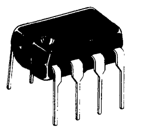
AUDIO AMPLIFIER

1/2-WATT AUDIO AMPLIFIER

The MC1306P is a monolithic complementary power amplifier and preamplifier designed to deliver 1/2-Watt into a loudspeaker with a 3.0 mV(rms) typical input. Gain and bandwidth are externally adjustable. Typical applications include portable AM-FM radios, tape recorder, phonographs, and intercoms.

- 1/2-Watt Power Output (9.0 Vdc Supply, 8-Ohm Load)
- High Overall Gain – 3.0 mV(rms) Sensitivity for 1/2-Watt Output
- Low Zero-Signal Current Drain – 4.0 mAdc @ 9.0 V typ
- Low Distortion – 0.5% at 250 mW typ

1/2-WATT AUDIO AMPLIFIER



PLASTIC PACKAGE
CASE 626

TYPICAL APPLICATIONS

FIGURE 1 – AM-FM RADIO, AUDIO SECTION

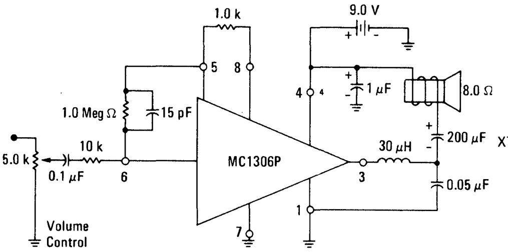
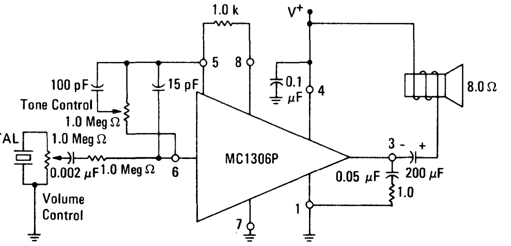
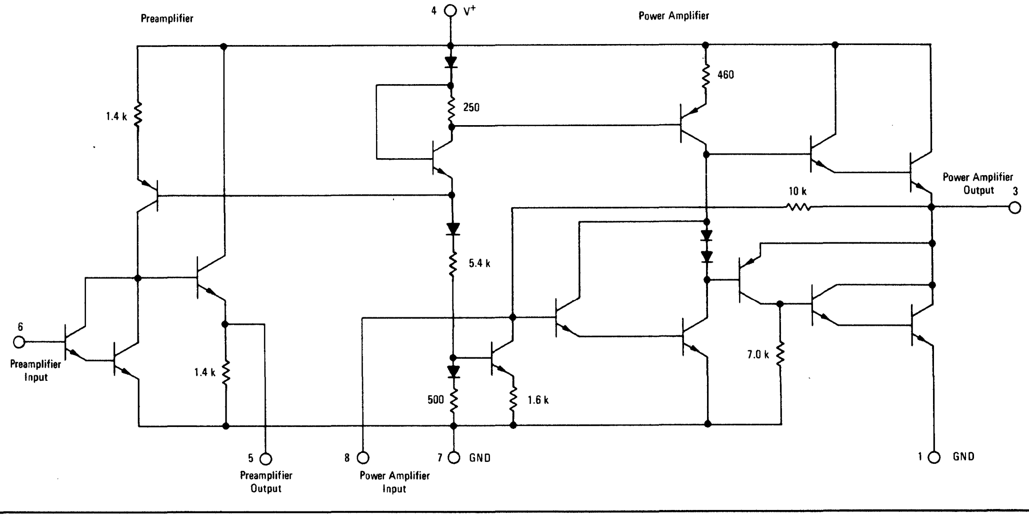


FIGURE 2 – PHONOGRAPH AMPLIFIER (CERAMIC CARTRIDGE)



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	12	Vdc
Load Current	I_L	400	mAdc
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	P_D $1/\theta_{JA}$	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = 9.0 V, R_L = 8.0 ohms, f = 1.0 kHz, (using test circuit of Figure 3), T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Open Loop Voltage Gain Pre-amplifier R_L = 1.0 k ohm Power-amplifier R_L = 16 ohms	A_{VOL}	 – –	 270 360	 – –	V/V
Sensitivity (P_o = 500 mW)	S	–	3.0	–	mV(rms)
Output Impedance (Power-amplifier)	Z_o	–	0.5	–	Ohm
Signal to Noise Ratio (P_o = 150 mW, f = 300 Hz to 10 kHz)	S/N	–	55	–	dB
Total Harmonic Distortion (P_o = 250 mW)	THD	–	0.5	–	%
Quiescent Output Voltage	V_o	–	$V^+/2$	–	Vdc
Output Power (THD ≤ 10%)	P_o	 500	 570	–	mW
Current Drain (zero signal)	I_D	–	4.0	–	mA
Power Dissipation (zero signal)	P_D	–	36	–	mW

FIGURE 3 – TEST CIRCUIT

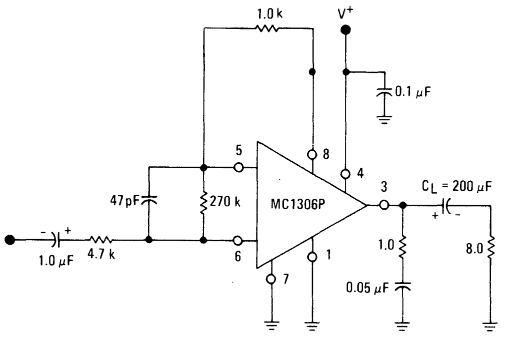
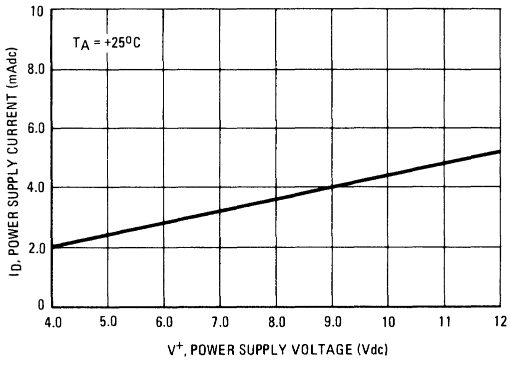


FIGURE 4 – ZERO SIGNAL BIAS CURRENT



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TYPICAL CHARACTERISTICS

(V^+ = 9.0 V, f = 1.0 kHz, T_A = +25°C unless otherwise noted)

FIGURE 5 – EFFICIENCY

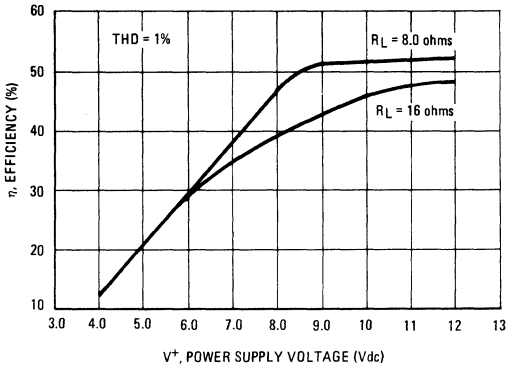

FIGURE 6 – OUTPUT POWER

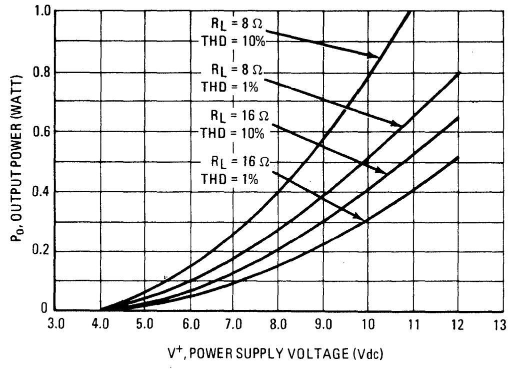

FIGURE 7 – TOTAL HARMONIC DISTORTION

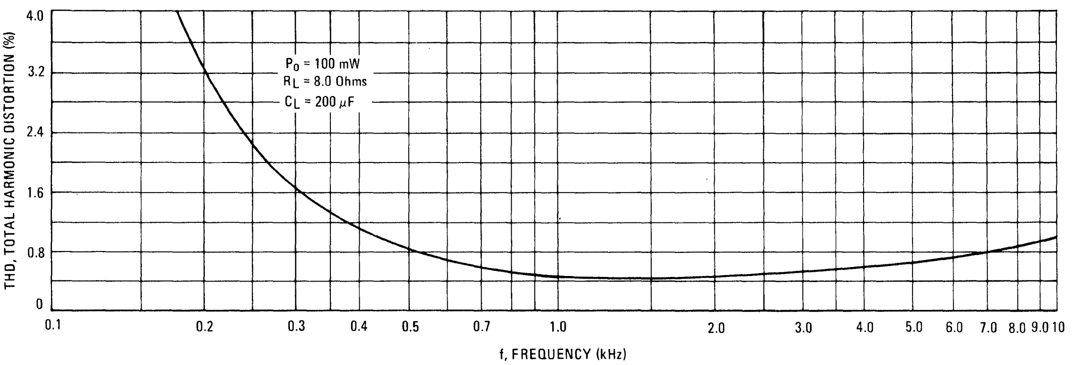

FIGURE 8 – EFFECT OF BATTERY AGING ON LOW-LEVEL DISTORTION

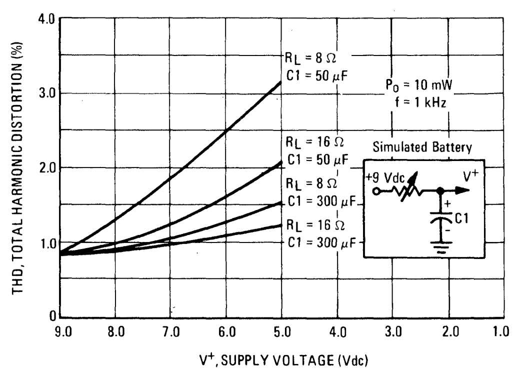

FIGURE 9 – DISTORTION

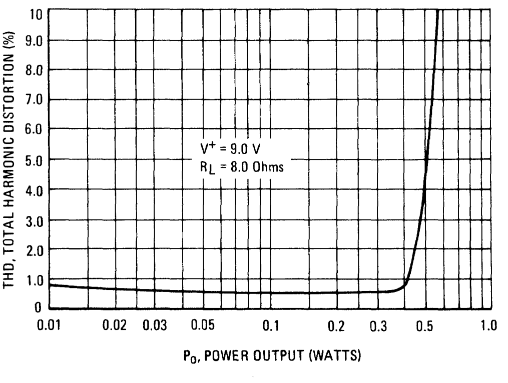

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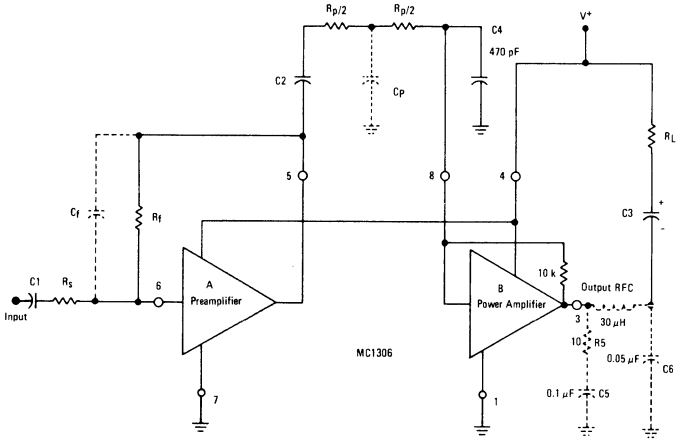
FIGURE 10 – TYPICAL CIRCUIT CONNECTION



DESIGN CONSIDERATIONS

The MC1306P provides the designer with a means to control preamplifier gain, power amplifier gain, input impedance, and frequency response. The following relationships will serve as guides.

1. Gain

The Preamplifier Stage Voltage Gain is:

$$A_{VA} \approx \frac{R_f}{R_s}$$

and is limited only by the open-loop gain (270 V/V). For good preamplifier dc stability R_f should be no larger than 1.0-megohm.

The Power Amplifier Voltage Gain is controlled in a similar manner where:

$$A_{VB} \approx \frac{10\text{ k}}{R_p}$$

The 10-k ohm feedback resistor is provided in the integrated circuit.

Recommended values of R_p range from 500-ohms to 3.3-k ohms. The low end is limited primarily by low-level distortion and the upper end is limited due to the voltage drive capabilities of the pre-amplifier. (A resistor can be added in the dc feedback loop, from pin 6 to ground, to increase this drive). The Overall Voltage Gain, then, is:

$$A_{VT} = \frac{R_f\ 10\text{ k}}{R_s\ R_p}$$

2. Input Impedance

The Preamplifier Input Impedance is:

$$Z_{in\,A} \approx R_s$$

and the Power Amplifier Input Impedance is:

$$Z_{in\,B} \approx R_p$$

3. Frequency Response

The low frequency response is controlled by the cumulative effect of the series coupling capacitors C1, C2, and C3. High-frequency response can be determined by the feedback capacitor, C_f, and the -3.0 dB point occurs when

$$X_{C_f} = R_f$$

Additional high frequency roll-off and noise reduction can be achieved by placing a capacitor from the center point of R_p to ground as shown in Figure 10.

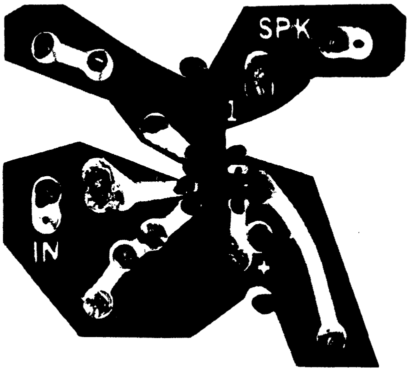
Capacitor C4 and the RC network shown in dotted lines may be needed to prevent high frequency parasitic oscillations. The RF choke, shown in series with the output, and capacitor C6 are used to prevent the high-frequency components in a large-signal clipped audio output waveform from radiating into the RF or IF sections of a radio (Figure 10).

4. Battery Operation

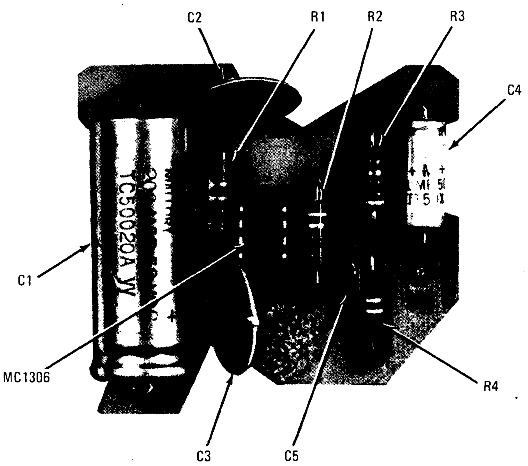
The increase of battery resistance with age has two undesirable effects on circuit performance. One effect is the increasing of amplifier distortion at low signal levels. This is readily corrected by increasing the size of the filter capacitor placed across the battery (as shown in Figure 8; a 300-μF filter capacitor gives distortions at low-tonal levels that are comparable to the "stiff" supply). The second effect of supply impedance is a lowering of power output capability for steady signals. This condition is not correctable, but is of questionable importance for music and voice signals.

5. Application Examples: (1) The audio section of the AM-FM radio (Figure 1) is adjusted for a preamplifier gain of 100 with an input impedance of 10-k ohms. The power amplifier gain is set at 10, which gives an overall voltage gain of 1000. The bandwidth has been set at 10-kHz. (2). The phono amplifier (Figure 2) is designed for a preamplifier gain of unity and a power amplifier gain of 10. The input impedance is 1.0-megohm. An adjustable treble control is provided within the feedback loop.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT



LOCATION OF COMPONENTS



See Figure 3 for schematic diagram.

PARTS LIST

Component	Value
C1	200 μF
C2	0.1 μF
C3	0.05 μF
C4	1.0 μF
C5	47 pF
R1	1 ohm
R2	1 k ohm
R3	4.7 k ohms
R4	270 k ohms
MC1306	–
PC Board	–

8

MC1307P

STEREO DEMODULATOR

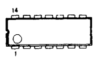
MONOLITHIC FM MULTIPLEX STEREO DEMODULATOR

. . . designed to derive the left and right channel audio information from the detected composite signal.

- Capable of Operation Over a Wide Power Supply Range — 8.0 – 14 Vdc
- Built-in Stereo-Indicator Lamp Driver

FM MULTIPLEX STEREO DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



(top view)

PLASTIC PACKAGE
CASE 646

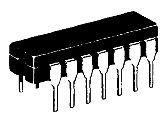
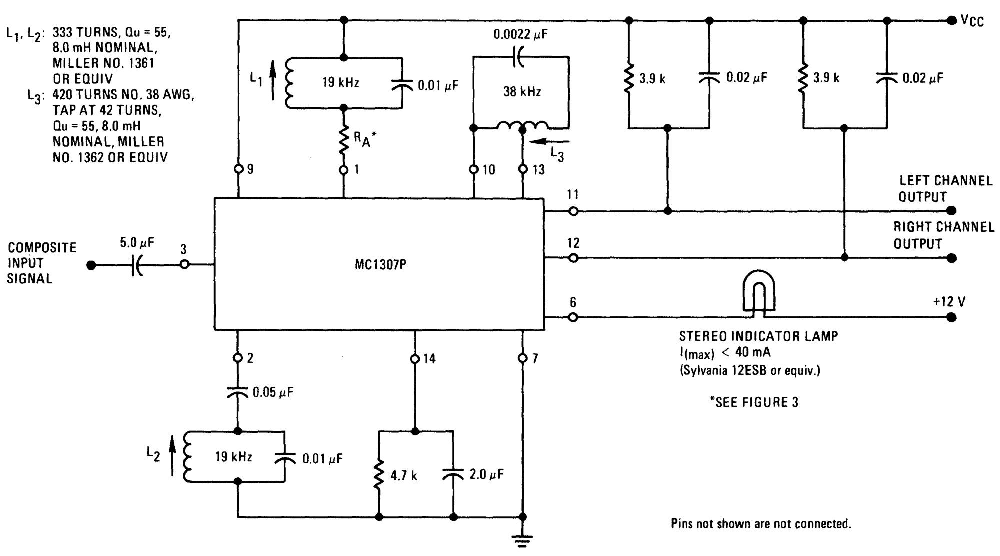


FIGURE 1 – TYPICAL CIRCUIT CONFIGURATION

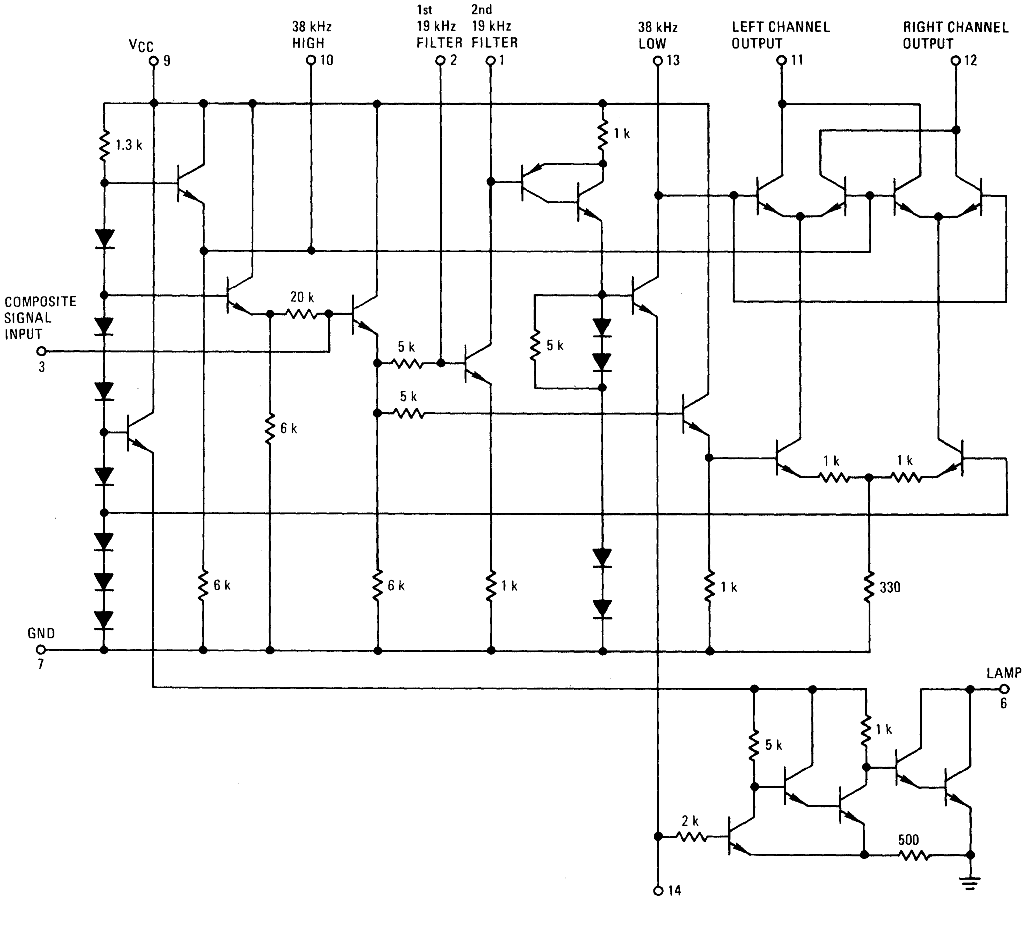


TYPICAL DC VOLTAGES (All measured using a VTVM with respect to Pin 7 (lamp on), R_A = 180 ohms, see Figure 3)

Pin Numbers	1	2	3	4	5	6	7	8	9	10	11	12	13	14
V_{CC} = 8.5 Vdc	8.5	2.7	3.6	–	–	0.8	0	–	8.5	4.4	6.2	6.2	4.4	1.5
V_{CC} = 12 Vdc	12	2.9	3.9	–	–	0.9	0	–	12	4.7	9.7	9.7	4.7	1.7

See Packaging Information Section for outline dimensions.

FIGURE 2 – CIRCUIT SCHEMATIC



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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage (Pins 1, 6, 9, 11, 12) (Pin 7 is grounded)	+22	Vdc
Lamp Driver Current	40	mAdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = +25°C, tests made with a 75 μs de-emphasis network (3.9 kΩ, 0.02 μF) unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Input Impedance (f = 1.0 kHz)	12	20	–	kΩ
Stereo Channel Separation (See Note 1)				dB
(f = 100 Hz)	–	35	–	
(f = 1.0 kHz)	20	40	–	
(f = 10 kHz)	–	30	–	
Total Harmonic Distortion (See Notes 1 and 2) (Modulation Frequency = 1.0 kHz)	–	0.5	1.0	%
Channel Balance (Monaural Input = 200 mV [rms]) (Monaural, Left and Right Outputs)	–	0.5	–	dB
Ultrasonic Frequency Rejection (See Note 3)				dB
(19 kHz)	–	25	–	
(38 kHz)	–	20	–	
Inherent SCA Rejection (without filter) (f = 60 kHz, 67 kHz and 74 kHz) (See Note 3)	–	50	–	dB
Lamp Indicator (R_A = 180 Ω)				mV(rms)
(Minimum 19 kHz input level for lamp "on")	–	16	25	
(Maximum 19 kHz input level for lamp "off")	5.0	14	–	
Power Dissipation (V_{CC} = 12 V)				mW
(Without lamp)	–	140	300	
(With lamp)	–	170	300	

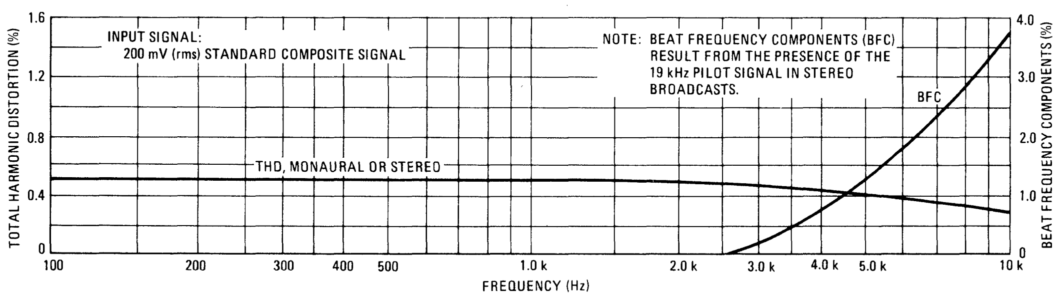
Note 1 – Measurement made with 200 mV(rms) Standard Multiplex Composite Signal where L = 1, R = 0 or R = 1, L = 0. Standard Multiplex Composite Signal is here defined as a signal containing left and/or right audio information with a 10% (19 kHz) pilot signal in accordance with FCC regulations.

Note 2 – Distortion specification also applies to Monaural Signal.

Note 3 – Referenced to 1.0 kHz output signal with Standard Multiplex Composite Input Signal.

TYPICAL CHARACTERISTICS

FIGURE 3 – DISTORTION COMPONENTS IN AUDIO SIGNAL



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TYPICAL CHARACTERISTICS (continued)

FIGURE 4 – TOTAL HARMONIC DISTORTION

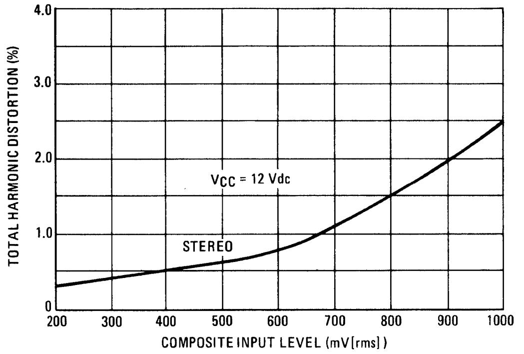


FIGURE 5 – MULTIPLEX SENSITIVITY

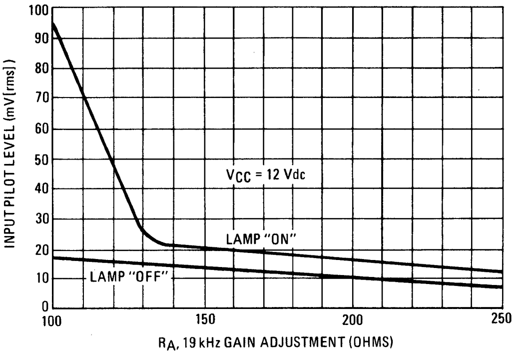


FIGURE 6 – CHANNEL SEPARATION

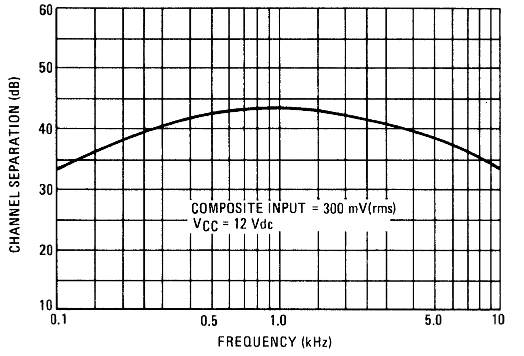
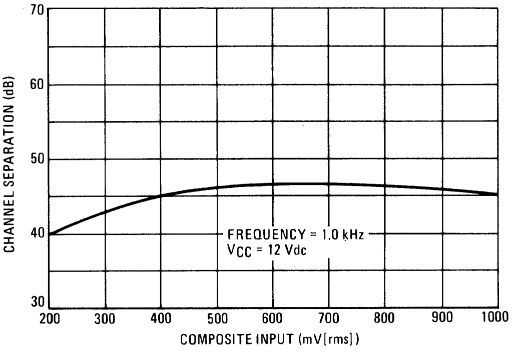


FIGURE 7 – CHANNEL SEPARATION



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MC1310P

STEREO DEMODULATOR

Specifications and Applications Information

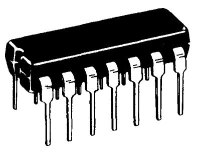
FM STEREO DEMODULATOR

. . . a monolithic device designed for use in solid-state stereo receivers.

- Requires no Inductors
- Low External Part Count
- Only Oscillator Frequency Adjustment Necessary
- Integral Stereo/Monaural Switch 75 mA Lamp Driving Capability
- Wide Dynamic Range: 0.5–2.8 V(p-p) Composite Input Signal
- Wide Supply Range: 8–14 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range
- Low Distortion: Typically 0.3% THD at 560 mV (RMS) Composite Input Signal
- Excellent SCA Rejection

FM STEREO DEMODULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



CASE 646

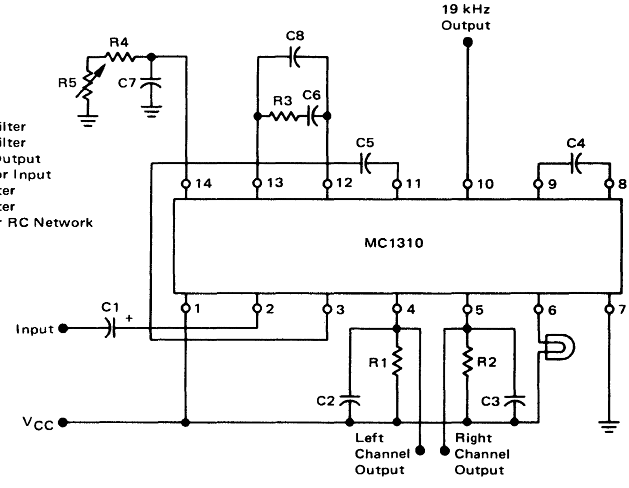
FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT

Pin Functions

Pin 1 = V_{CC}	Pin 8 = Switch Filter
Pin 2 = Input	Pin 9 = Switch Filter
Pin 3 = Amplifier Output	Pin 10 = 19 kHz Output
Pin 4 = Left Channel Output	Pin 11 = Modulator Input
Pin 5 = Right Channel Output	Pin 12 = Loop Filter
Pin 6 = Lamp Indicator	Pin 13 = Loop Filter
Pin 7 = Ground	Pin 14 = Oscillator RC Network

Parts List

C1 = 2.0 μF	C8 = 0.25 μF
C2 = 0.02 μF	R1 = 3.9 kΩ
C3 = 0.02 μF	R2 = 3.9 kΩ
C4 = 0.25 μF	R3 = 1.0 kΩ
C5 = 0.05 μF	R4 = 16 kΩ
C6 = 0.5 μF	R5 = 5.0 kΩ
C7 = 470 pF	



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25° unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	14	Volts
Lamp Current	75	mA
Power Dissipation (Package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS Unless otherwise noted; V_{CC} = +12 Vdc, T_A = +25°C, 560 mV(RMS) (2.8 $V_{(p-p)}$) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

Characteristic	Min	Typ	Max	Unit
Maximum Standard Composite Input Signal (0.5% THD)	2.8	–	–	$V_{(p-p)}$
Maximum Monaural Input Signal (1.0% THD)	2.8	–	–	$V_{(p-p)}$
Input Impedance	20	50	–	kΩ
Stereo Channel Separation	30	40	–	dB
Audio Output Voltage (desired channel)	–	485	–	mV(RMS)
Monaural Channel Balance (pilot tone "off")	–	–	1.5	dB
Total Harmonic Distortion	–	0.3	–	%
Ultrasonic Frequency Rejection 19 kHz 38 kHz	– –	34.4 45	– –	dB
Inherent SC A Rejection (f = 67 kHz; 9.0 kHz beat note measured with 1.0 kHz modulation "off")	–	75	–	dB
Stereo Switch Level 19 kHz input level for lamp "on" 19 kHz input level for lamp "off"	 – 5.0	 – –	 20 –	mV(RMS)
Capture Range (permissible tuning error of internal oscillator, reference circuit values of Figure 1)	–	±3.5	–	%
Current Drain (lamp "off")	–	13	–	mAdc

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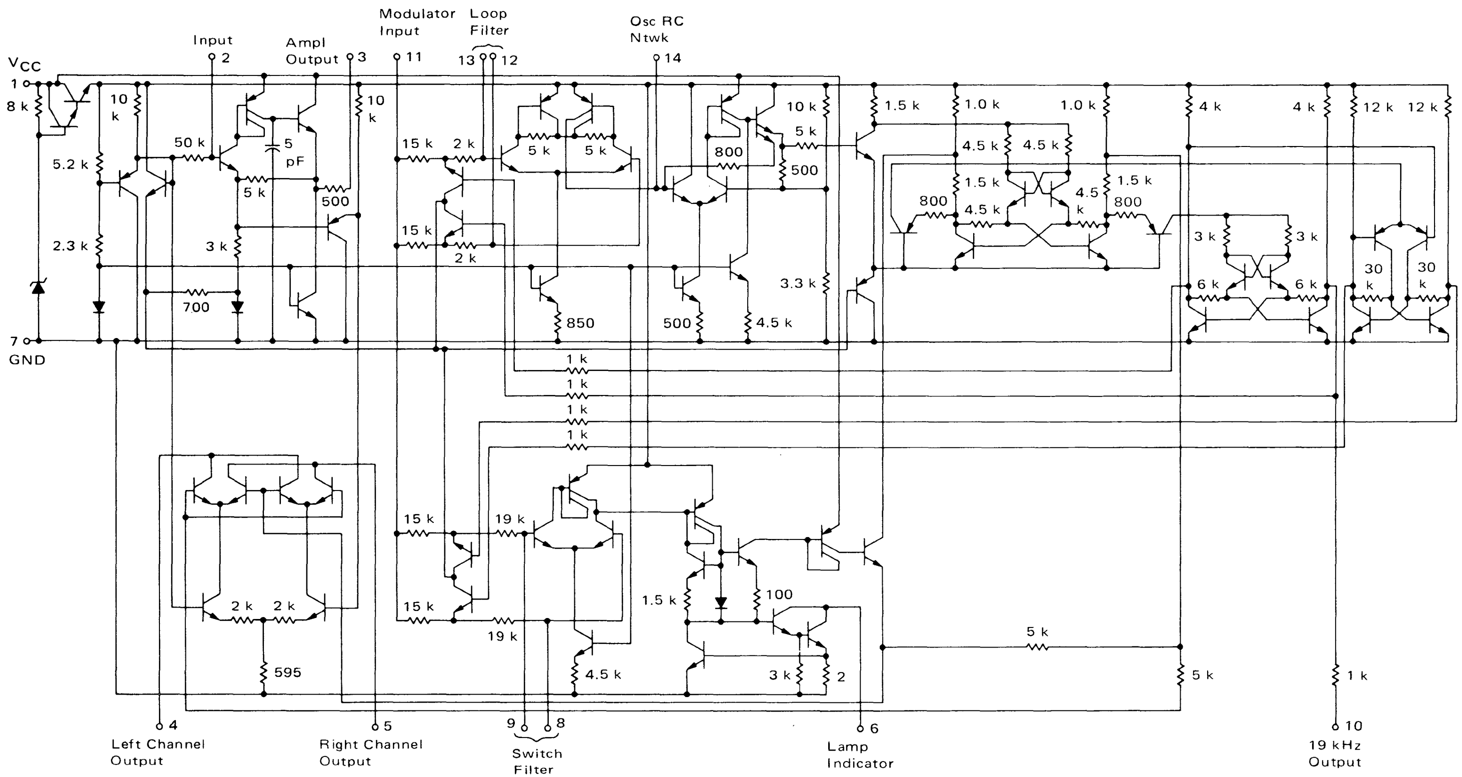
FIGURE 2 – CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

Unless otherwise noted: V_{CC} = +12 Vdc, T_A = +25°C; 560 mV(RMS) (2.8 $V_{[p-p]}$) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

FIGURE 3 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL

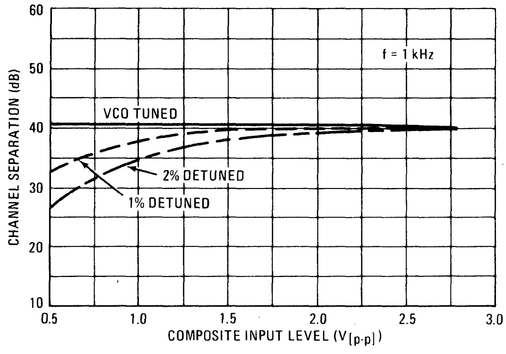


FIGURE 4 – CHANNEL SEPARATION versus FREQUENCY

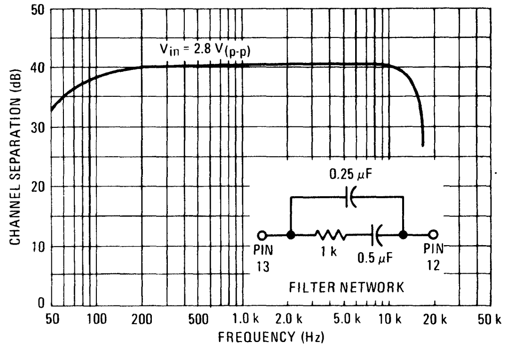


FIGURE 5 – CHANNEL SEPARATION versus VCO FREE-RUNNING FREQUENCY

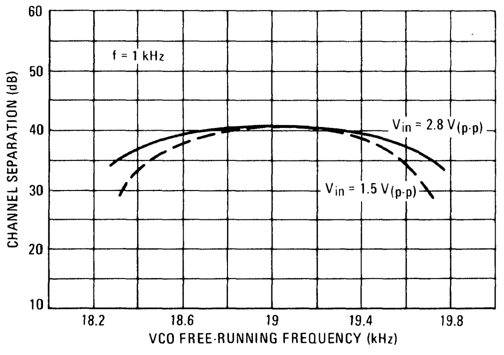


FIGURE 6 – CHANNEL SEPARATION versus SUPPLY VOLTAGE

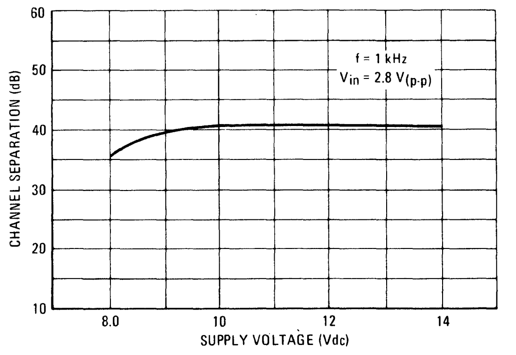


FIGURE 7 – THD versus COMPOSITE INPUT LEVEL*

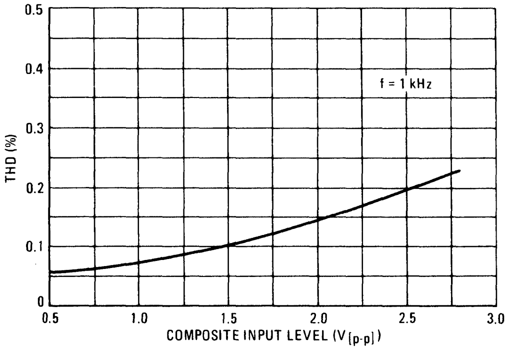
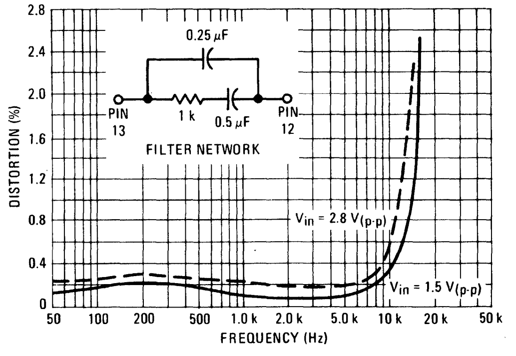


FIGURE 8 – DISTORTION versus FREQUENCY*



*Measured with Low Pass Filter (BW = 15 kHz).

TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DISTORTION versus FREQUENCY*

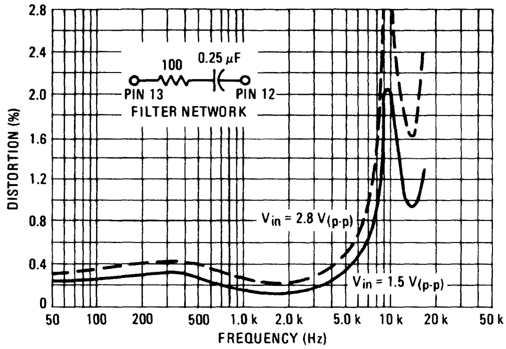


FIGURE 10 – VCO FREE-RUNNING FREQUENCY versus TEMPERATURE

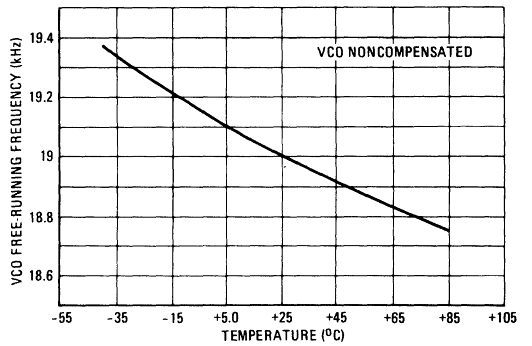
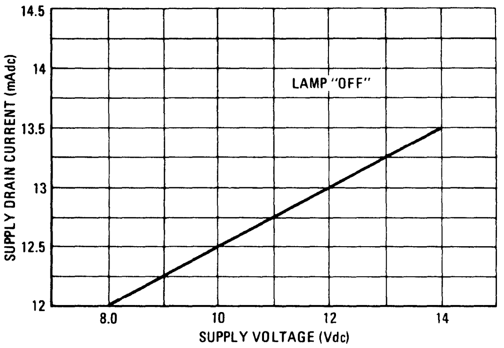


FIGURE 11 – CURRENT DRAIN versus SUPPLY VOLTAGE



*Measured with Low Pass Filter (BW = 15 kHz)

FIGURE 12 – PILOT LEVEL REQUIRED FOR VCO LOCKUP versus VCO FREE-RUNNING FREQUENCY

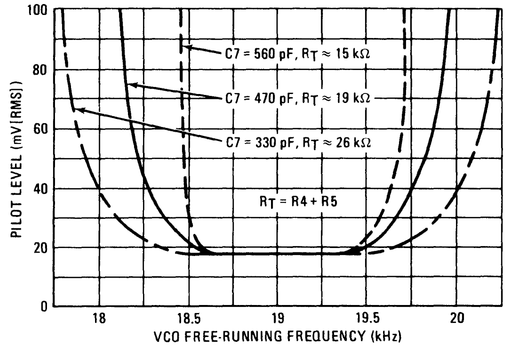
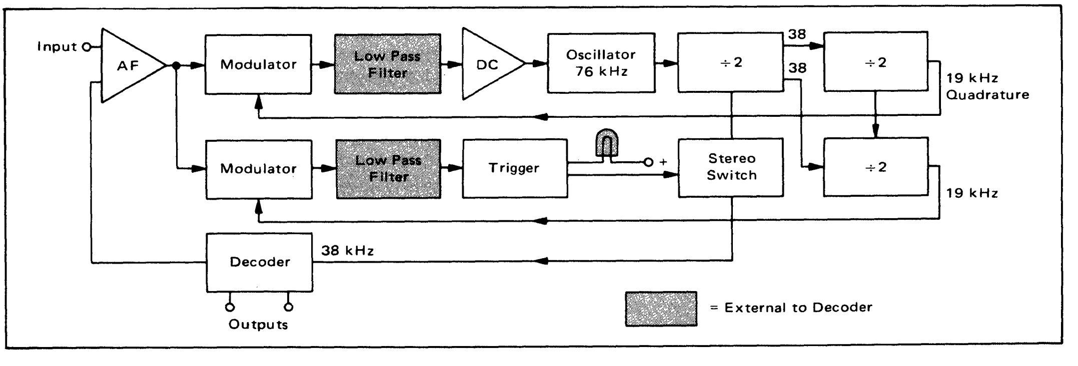


FIGURE 13 – SYSTEM BLOCK DIAGRAM



CIRCUIT OPERATION

Figure 13, on the previous page, shows the system block diagram. The upper line, comprising the 38-kHz regeneration loop operates as follows: the internal oscillator running at 76-kHz and feeding through two divider stages returns a 19-kHz signal to the input modulator. There the returned signal is multiplied with the incoming signal so that when a 19-kHz pilot tone is received a dc component is produced. The dc component is extracted by the low pass filter and used to control the frequency of the internal oscillator which consequently becomes phase-locked to the pilot tone. With the oscillator phase-locked to the pilot the 38-kHz output from the first divider is in the correct phase for decoding a stereo signal. The decoder is essentially another modulator in which the incoming signal is multiplied by the regenerated 38-kHz signal. The regenerated 38-kHz signal is fed to the stereo decoder via an internal switch, which closes when a sufficiently large 19 kHz pilot tone is received.

The 19-kHz signal returned to the 38-kHz regeneration loop modulator is in quadrature with the 19-kHz pilot tone when the loop is locked. With the third divider state appropriately connected, a 19-kHz signal in phase with the pilot tone is generated. This is multiplied with the incoming signal in the stereo switch modulator yielding a dc component proportional to the pilot tone amplitude. This component after filtering is applied to the trigger circuit which activates both the stereo switch and an indicator lamp.

APPLICATIONS INFORMATION

(Component numbers refer to Figure 1)

External Component Functions and Values

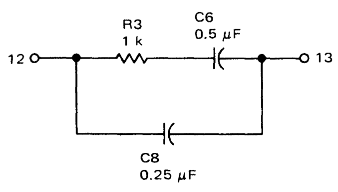
C1 — Input coupling capacitor; 2.0 µF is recommended but a lower value is permissible if reduced separation at low frequencies is acceptable.

R1, R2, C2, C3 — See Maximum Load Resistance section.

C4 — Filter capacitor for stereo switch level detector; time constant is C4 x 53 kilohms ±30%, maximum dc voltage appearing across C4 is 0.25 V (pin 8 positive) at 100 mV(RMS) pilot level. The signal voltage across C4 is negligible.

C5 — See Phase Compensation section.

R3, C6, C8 — Phase-locked loop filter components; the following network is recommended:



When less performance is required a simpler network consisting of R3 = 100 ohms and C6 = 0.25 µF may be used (omit C8). See Figure 9.

R4, R5, C7 — Oscillator timing network; recommended values:

C7 = 470 pF		1%
R4 = 16 kΩ		1%
R5 = 5 kΩ		Preset

These values give ±3.5% typical capture range. Capture range may be increased by reducing C7 and increasing R4, R5 proportionally but at the cost of increasing beat-note distortion (due to oscillator-phase jitter) at high-signal levels. See Figure 12.

Stereo Lamp — Nominal rating up to 75 mA at 12 V; the circuit includes surge limiting which restricts cold-lamp current to approximately 250 mA.

19-kHz Output — A buffer output providing a 3.0-V_{pk} square wave at 19 kHz is available at pin 10. A frequency counter may be connected to this point to measure the oscillator free-running frequency for alignment. See Alignment section.

External Monaural/Stereo Switching

If it is desired to maintain the circuit in monaural mode, the following procedure must be followed. First, the stereo switch must be disabled to prevent false lamp triggering. This can be accomplished by connecting pin 8 negative or pin 9 positive by 0.3 volt. Pin 8 may be grounded directly if desired. Note that the voltage across C4 increases to approximately 2 volts with pin 9 positive when pin 8 is grounded.

Second, the 76-kHz oscillator must be killed to prevent interference when on AM. This can be accomplished by connecting pin 14 to ground via a current limiting resistor (3.3 kilohms is recommended).

Phase Compensation/IF Roll-off Compensation

Phase-shifts in the circuit cause the regenerated 38-kHz sub-carrier to lead the original 38 kHz by approximately 2°. The coupling capacitor C5 generates an

APPLICATIONS INFORMATION (continued)

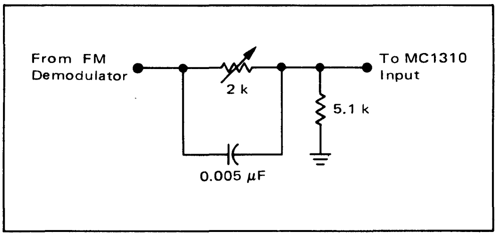
additional lead of 3.5° (for C5 = 0.05 μF) giving a total lead of 5.5°.

The circuit is so designed that phase lag may be generated by adding a capacitor from pin 3 to ground. The source resistance at this point is 500 ohms. A capacitance of 820 pF compensates the 5.5° phase lead: increase above this value causes the regenerated sub-carrier to lag the original. However, a 5.5° phase error if left noncompensated will not degrade separation appreciably.

Note that these phase shifts occur within the phase-locked loop and affect only the regenerated 38-kHz sub-carrier: the circuit causes no significant phase or amplitude variation in the actual stereo signal prior to decoding.

Most IF amplifiers have a frequency response that limits separation to a value significantly lower than the capability of the MC1310. For example, if the response produces a 1-dB roll-off at 38 kHz, the separation will be limited to about 32 dB. This error can be compensated by using an RC lead network as shown in Figure 14. The exact values will be determined by the IF amplifier design. However, the values shown in Figure 14 are suitable for use with the MC1357 and MC1375 IF amplifiers.

FIGURE 14 – IF COMPENSATION NETWORK



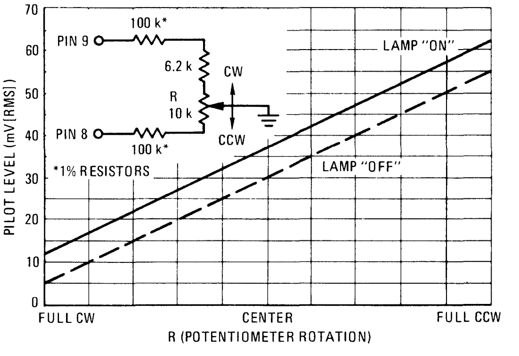
Voltage Control Oscillator Compensation

Figure 10 illustrates noncompensated Oscillator Drift versus temperature. The recommended T_C of the R4, R5, C7 combination is -300 PPM. This will hold the oscillator drift to approximately ±1% over a temperature range of -40 to +85°C. Allowing ±2% for aging of the timing components acceptable performance is still obtained.

Lamp Sensitivity

It may be desirable in some cases, to change the lamp sensitivity due to differing signal levels produced by various FM detectors. The lamp sensitivity can be changed by making use of the external circuit shown. Typical sensitivities versus potentiometer rotation are also shown in Figure 15.

FIGURE 15 – PILOT SENSITIVITY versus POTENTIOMETER ROTATION



Alignment Procedure

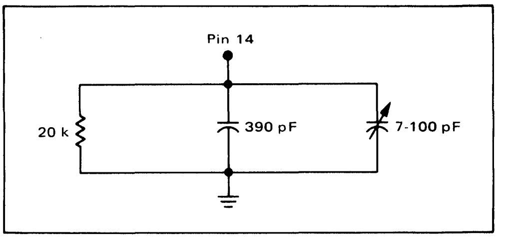
The optimum alignment procedure, with no input signal applied, is to adjust R5 until 19.00 kHz is read at pin 10 on the frequency counter.

Another procedure requiring no equipment, other than the receiver itself, will result in separation of within a few dB of optimum. This latter method is merely to tune the receiver to a stereo broadcast and adjust R5 until the pilot lamp turns "on". To find the center of the lock-in range, rotate the potentiometer back and forth until the center of the lamp "on" range is found. This completes the alignment.

Alternate Timing Network

The alternate timing network shown, incorporating a trimmer capacitor rather than a potentiometer, may be used if desired. Again, to provide correct temperature compensation, the temperature coefficient of the timing network must be approximately -300 PPM.

FIGURE 16

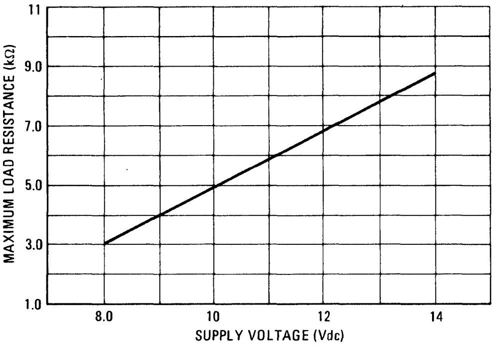


Maximum Load Resistance

The curve shown gives absolute maximum load resistance values versus supply voltage used for full-signal handling capability. With desired load resistance choose C2, C3 capacitors to provide standard 75 μs de-emphasis.

APPLICATIONS INFORMATION (continued)

FIGURE 17 – MAXIMUM LOAD RESISTANCE versus SUPPLY VOLTAGE



Audio Output

$$\text{The ratio } G = \frac{\text{p-p audio output (one-channel)}}{\text{p-p input signal}} \text{ for}$$

different types of input is as follows:

INPUT

Single-Channel Composite Signal	Monaural Signal
0.45	0.5

These figures are for 3.9-kilohm load resistors and for low-audio frequencies where de-emphasis roll-off is insignificant.

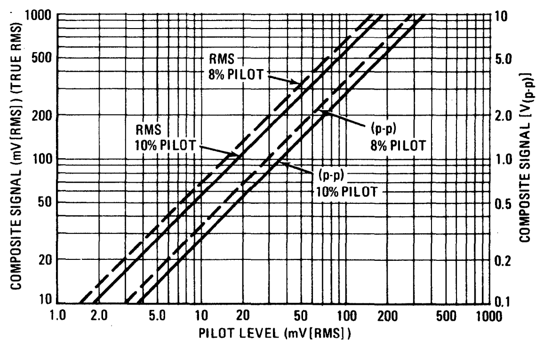
Capture Range versus Timing Components

The capture range can be changed to some extent by use of different timing components. Typical values are shown in Figure 12.

Composite Signal

Due to confusion concerning the measurement of the stereo composite signal, a curve showing both RMS and p-p composite levels versus pilot level follows, see Figure 18.

FIGURE 18 – COMPOSITE LEVEL versus PILOT (L or R Modulation Only)



MC1311P

FM STEREO DEMODULATOR

Product Preview

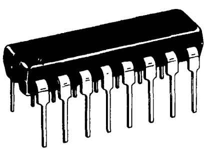
FM STEREO DEMODULATOR

. . . a monolithic device designed for use in solid-state stereo receivers.

- Unity Gain
- Requires no Inductors
- Low External Part Count
- Emitter-Follower Outputs
- Only Oscillator Frequency Adjustment Necessary
- Integral Stereo/Monaural Switch 100 mA Lamp Driving Capability
- Wide Dynamic Range: 0.5 - 2.8 Vp-p Composite Input Signal
- Excellent Supply Range and Ripple Rejection
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range
- Low Distortion: Typically 0.5% THD at 560 mV (RMS) Composite Input Signal
- Excellent SCA Rejection

FM STEREO DEMODULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

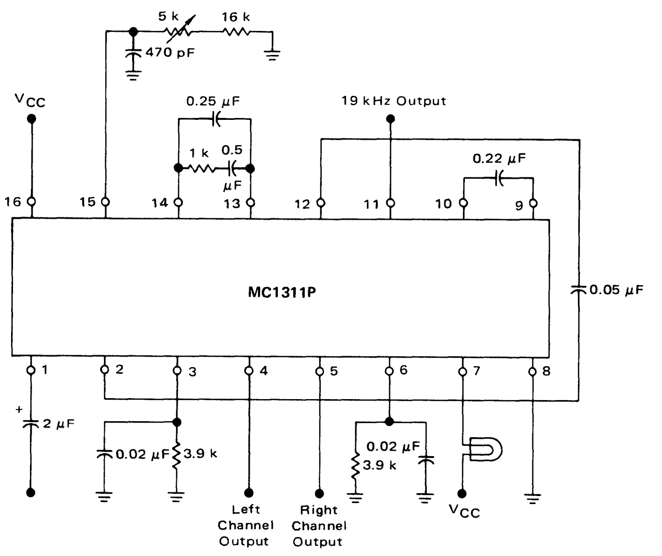


PLASTIC PACKAGE
CASE 648

FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT

Pin Functions

Pin 1 = Input
Pin 2 = Amplifier Output
Pin 3 = Left Channel Output
Pin 4 = Left Emitter Follower Output
Pin 5 = Right Emitter Follower Output
Pin 6 = Right Channel Output
Pin 7 = Lamp Indicator
Pin 8 = Ground
Pin 9 = Switch Filter
Pin 10 = Switch Filter
Pin 11 = 19 kHz Output
Pin 12 = Modulator Input
Pin 13 = Loop Filter
Pin 14 = Left Filter
Pin 15 = Oscillator RC Network
Pin 16 = V_{CC}



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	16	Volts
Lamp Current	100	mA
Power Dissipation (Package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	-30 to +85	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS Unless otherwise noted: V_{CC} = +12 Vdc, T_A = +25°C, 560 mV(RMS) (2.8 Vp-p) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

Characteristic	Min	Typ	Max	Unit
Maximum Input Signal (1.0% THD)	2.8	–	–	Vp-p
Power Supply Ripple Rejection (100 Hz)	–	45	–	dB
Input Impedance	20	50	–	kΩ
Stereo Channel Separation	30	40	–	dB
Voltage Gain (Vp-p out/Vp-p in)	–	1.0	–	V/V
Monaural Channel Balance (pilot tone "off")	–	–	1.5	dB
Total Harmonic Distortion	–	0.5	–	%
Ultrasonic Frequency Rejection 19 kHz 38 kHz	– –	34.4 45	– –	dB
Inherent SCA Rejection (f = 67 kHz; 9.0 kHz beat note measured with 1.0 kHz modulation "off")	–	75	–	dB
Stereo Switch Level 19 kHz input level for lamp "on" 19 kHz input level for lamp "off"	 – 5.0	 – –	 20 –	mV(RMS)
Capture Range (permissible tuning error of internal oscillator, reference circuit values of Figure 1)	–	±3.5	–	%
Current Drain (lamp "off")	–	27	–	mAdc

MC1312P
MC1313P

SQ* DECODER

MONOLITHIC CBS SQ* DECODER

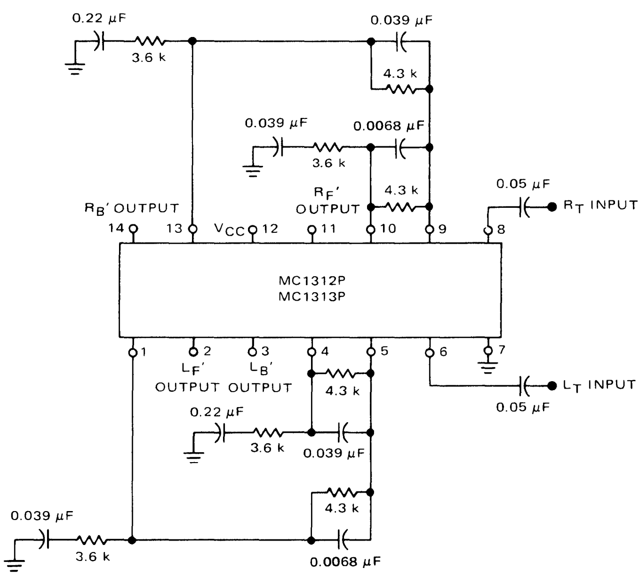
. . . a matrix system designed to decode an SQ* encoded program into four separate channels. These devices conform to specifications for decoding quadraphonic records produced by the largest record companies in the world.

- Both Home Entertainment (MC1312) and Automotive (MC1313) Versions Available
- High Input Impedance
  MC1312P – 3.0 Megohms typ, MC1313P – 1.8 Megohms typ
- Low Harmonic Distortion
  MC1312P – 0.1% typ, MC1313P – 0.25% typ
- High Signal Handling Capability
  MC1312P – 2.0 V(RMS) min, MC1313P – 0.8 V(RMS) min
- MC1313 Provides Excellent Performance at V_{CC} = +8.0 Vdc

FOUR-CHANNEL SQ* DECODER

MONOLITHIC SILICON INTEGRATED CIRCUIT

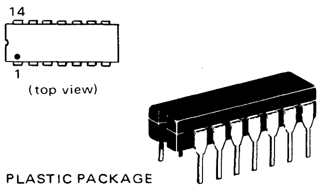
FIGURE 1 – TYPICAL APPLICATION CIRCUIT



Note: For optimum performance ±5% tolerance components are recommended with the exception of the input capacitors.

DEFINITIONS	
L_T = Left total	R_T = Right total
L_F' = Left front	L_B' = Left back
R_F' = Right front	R_B' = Right back

This component is sold without patent indeminity and any infringement resulting from use or resale thereof shall be the sole responsibility of purchaser and shall not be the responsibility of manufacturer or distributor even though such use is in accordance with manufacturer's recommendations.



PLASTIC PACKAGE
CASE 646

*Trademark of Columbia Broadcasting System, Inc.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	25	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range MC1312P MC1313P	0 to +75 -40 to +85	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} for MC1312P = +20 Vdc, V_{in} = 0.5 V(RMS), for MC1313P V_{CC} = +12 Vdc, V_{in} = 0.2 V(RMS), T_A = +25°C unless otherwise noted.) (See Figure 3.)

Characteristic	Min	Typ	Max	Unit
Supply Current Drain MC1312P MC1313P	11 6.5	16 9.0	21 12.5	mA
Input Impedance MC1312P MC1313P	1.8 1.0	3.0 1.8	– –	MΩ
Output Impedance	–	5.0	–	kΩ
Channel Balance (L_F/R_F)	-1.0	0	+1.0	dB
Voltage Gain L_F/L_T or R_F/R_T	-1.0	0	+1.0	dB
Relative Voltage Gain L_B'/L_F', R_B'/L_F', L_B'/R_F', R_B'/R_F' L_F' measurements made with L_T input, R_F' measurements made with R_T input.	-2.0	-3.0	-4.0	dB
Maximum Input Voltage for 1%THD at Output MC1312P R_T or L_T MC1313P	2.0 0.8	– –	– –	V(RMS)
Total Harmonic Distortion MC1312P R_T or L_T MC1313P	– –	0.1 0.25	– –	%
Signal to Noise Ratio (Short-Circuit Input V_O = 0.5 V(RMS) MC1312P with Output Noise Referenced to Output V_O = 0.2 V(RMS) MC1313P Voltage, V_O) (BW = 20 Hz to 20 kHz)	– –	80 74	– –	dB

TYPICAL CHARACTERISTICS

FIGURE 2 – CURRENT DRAIN

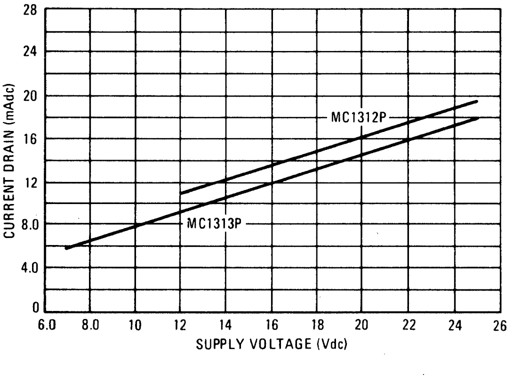
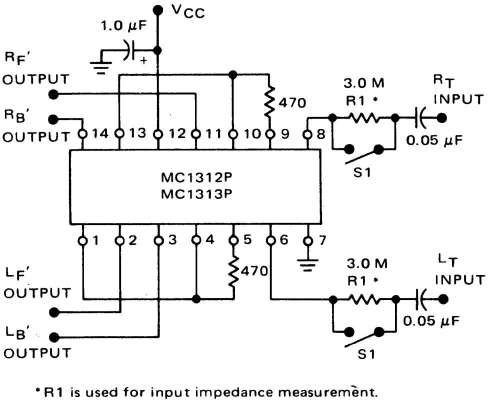


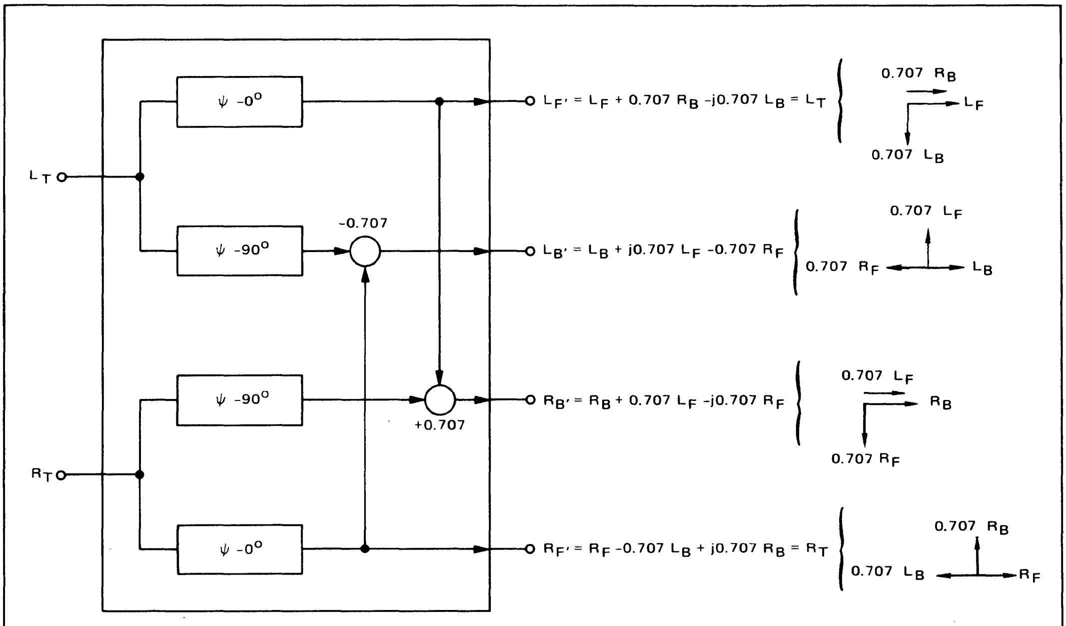
FIGURE 3 – TEST CIRCUIT



* R1 is used for input impedance measurement.
S1 is normally closed.

APPLICATIONS INFORMATION

FIGURE 4 – DECODING PROCESS DIAGRAM



$L_T = L_F + 0.707\ R_B - j\ 0.707\ L_B$

$R_T = R_F - 0.707\ L_B + j\ 0.707\ R_B$

L_T and R_T are composite signals from SQ encoded records or SQ broadcast.

The decoding process is shown schematically in Figure 4. The MC1312P/MC1313P circuits that perform this function consists of two preamplifiers which are fed with left total, L_T, and right total, R_T, signals. The preamplifiers each feed two all-pass* networks that are used to generate two L_T signals in quadrature and two R_T signals in quadrature. The four signals are matrixed to yield left-front, left-back, right-front, and right-back signals (L_F', L_B', R_F', R_B').

The all-pass networks are of the Wein bridge form with the resistive arms realized in the integrated circuit and the RC arms formed by external components. The values shown in Figure 1 are for a 100-Hz to 10-kHz bandwidth and a phase ripple of ±8.5° on a 90° phase difference.

It is generally desirable to enhance center-front to center-back separation. This is accomplished by connecting a resistor between pins 2 and 11 (front outputs) and a resistor between pins 3 and 14 (back outputs). For a 10% front channel blending† and a 40% back channel blending†, 47 kilohms between pins 2 and 11 and 7.5 kilohms between pins 3 and 14 is required and results in the following equations:

†$R_F'' = 0.912\ L_T + 0.088\ R_T$

$L_F'' = 0.912\ R_T + 0.088\ L_T$

$R_B'' = \frac{\sqrt{2}}{2}\left[0.714\ (JR_T - L_T) + 0.286\ (R_T - JL_T)\right]$

$L_B'' = \frac{\sqrt{2}}{2}\left[0.714\ (JL_T - R_T) + 0.286\ (L_T - JR_T)\right]$

To meet the EIA matrix standards with 10/40 blend use the circuit of Figure 5, which results in the following equations:

$R_F'' = 0.772\ (0.995\ R_T + 0.0972\ L_T)$

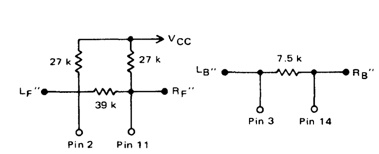
$L_F'' = 0.772\ (0.995\ L_T + 0.0972\ R_T)$

$R_B'' = \frac{\sqrt{2}}{2}\ (0.769)\left[0.928\ (JR_T - L_T) + 0.372\ (R_T - JL_T)\right]$

$L_B'' = \frac{\sqrt{2}}{2}\ (0.769)\left[0.928\ (JL_T - R_T) + 0.372\ (L_T - JR_T)\right]$

***An all-pass network produces phase shift without amplitude variations.**

FIGURE 5 – EIA STANDARD BLEND



MC1324P

DUAL CHROMA DEMODULATOR

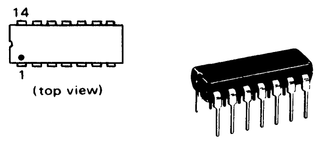
DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B MATRIX AND CHROMA DRIVER STAGES

. . . a monolithic device designed for use in solid-state color television receivers.

- Luminance Input Provided
- Good Chroma Sensitivity – 0.36 Vp-p Input for 5 Vp-p Output
- Low Differential Output DC Offset Voltage – 0.6 V max
- DC Temperature Stability – 3 mV/°C typ
- Negligible Change in Output Voltage Swing and Varying 3.58-MHz Reference Input Signal
- High Ripple Rejection Achieved with MOS Filter Capacitors
- High Blue Output Voltage Swing – 10 V(p-p) typ
- Blanking Input Provided
- Improved MC1326
- Short-Circuit Protected Outputs

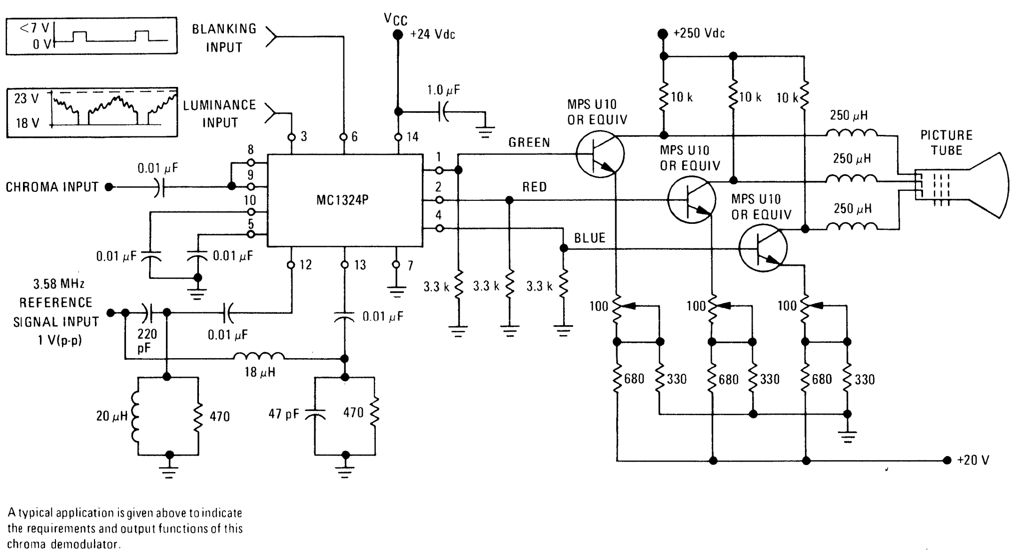
DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B OUTPUT MATRIX

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – MC1324 TYPICAL APPLICATION



A typical application is given above to indicate the requirements and output functions of this chroma demodulator.

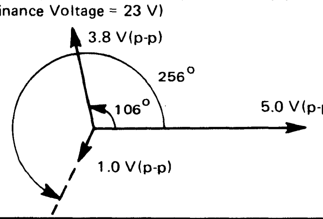
See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5.0	V(pk)
Reference Signal Input Voltage	5.0	V(pk)
Minimum Load Resistance	2.2	k ohms
Luminance Input Voltage	12	V(p-p)
Blanking Input Voltage	7.0	V(p-p)
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, V_{ref} = 1.0 V(p-p), R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted.)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS (See Figure 2.)					
Quiescent Output Voltage	1,2,4	14.3	15	16.3	Vdc
Quiescent Input Current (R_L = ∞) (R_L = 3.3 k ohms)		 – 16.5	 6.0 19	 – 25.5	mA
Reference Input dc Voltage	5,12,13	–	6.8	–	Vdc
Chroma Input dc Voltage	8,9,10	–	3.6	–	Vdc
Differential Output Voltage	1,2,4	–	0.3	0.6	Vdc
Output Temperature Coefficient (Reference Input Voltage = 1.0 V(p-p), +25° to +65°C)	1,2,4	–	3.0	–	mV/°C
DYNAMIC CHARACTERISTICS (See Figure 3.)					
Detected Output Voltage (See Note 1.) +(B-Y) -(B-Y)	4	 4.0 4.0	 5.0 5.0	 – –	V(pk)
Chroma Input Voltage (B-Y Output = 5.0 V[p-p]) (See Note 2.)	8	–	0.36	0.7	V(p-p)
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz)	1,2,4	 – –	 0.95 0.5	 – –	–
Blanking Input Resistance 1.0 Vdc 0 Vdc	6	 – –	 1.1 75	 – –	kΩ
Detected Output Voltage (Adjust B-Y Output to 5.0 V(p-p), Luminance Voltage = 23 V) G-Y Output R-Y Output	4 1 2	 0.75 3.5	 1.0 3.8	 1.25 4.2	V(p-p)
Relative Output Phase (B-Y Output = 5.0 V(p-p), Luminance Voltage = 23 V) B-Y to R-Y Output B-Y to G-Y Output	 4,2 4,1	 101 248	 106 256	 111 264	Degrees



Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1,2,4	–	100	500	mV(p-p)
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B-Y Output = 5.0 V[p-p])	1,2,4	–	–	1.0	V(p-p)
Reference Input Resistance	12,13	–	2.0	–	kΩ
Reference Input Capacitance	12,13	–	6.0	–	pF
Chroma Input Resistance	9,10	–	2.0	–	kΩ
Chroma Input Capacitance	9,10	–	2.0	–	pF

NOTES:

1. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 1.2 V(p-p).
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5 V(p-p). The Chroma Input Voltage at this point should be equal to or less than 0.7 V(p-p).

8

TEST CIRCUITS

(V_{CC} = 24 Vdc, R_L = 3.3 Kilohms, T_A = +25°C unless otherwise noted.)

FIGURE 2 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

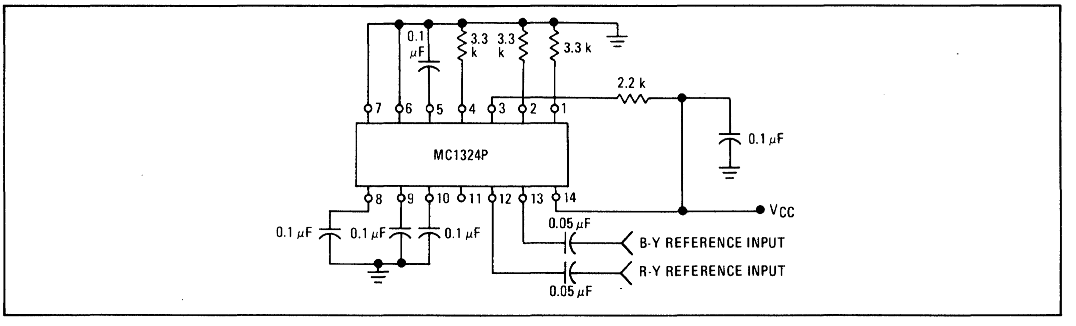
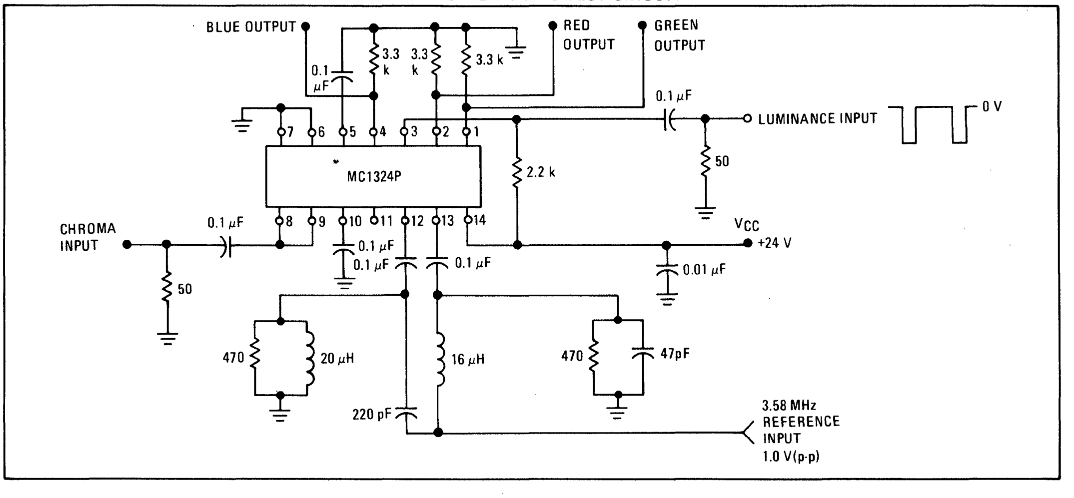


FIGURE 3 – DYNAMIC TEST CIRCUIT



TYPICAL CHARACTERISTICS

FIGURE 4 – DETECTED OUTPUT VOLTAGE
(Test Circuit of Figure 3)

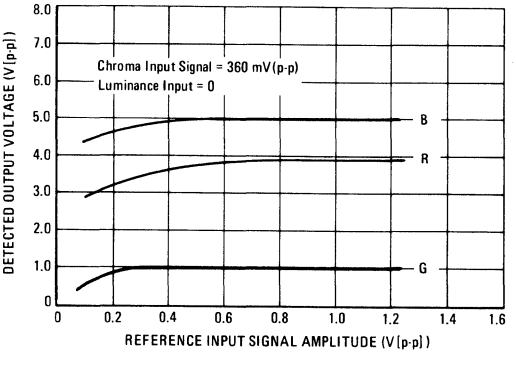
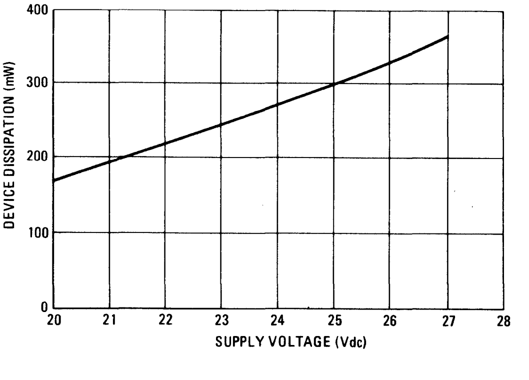
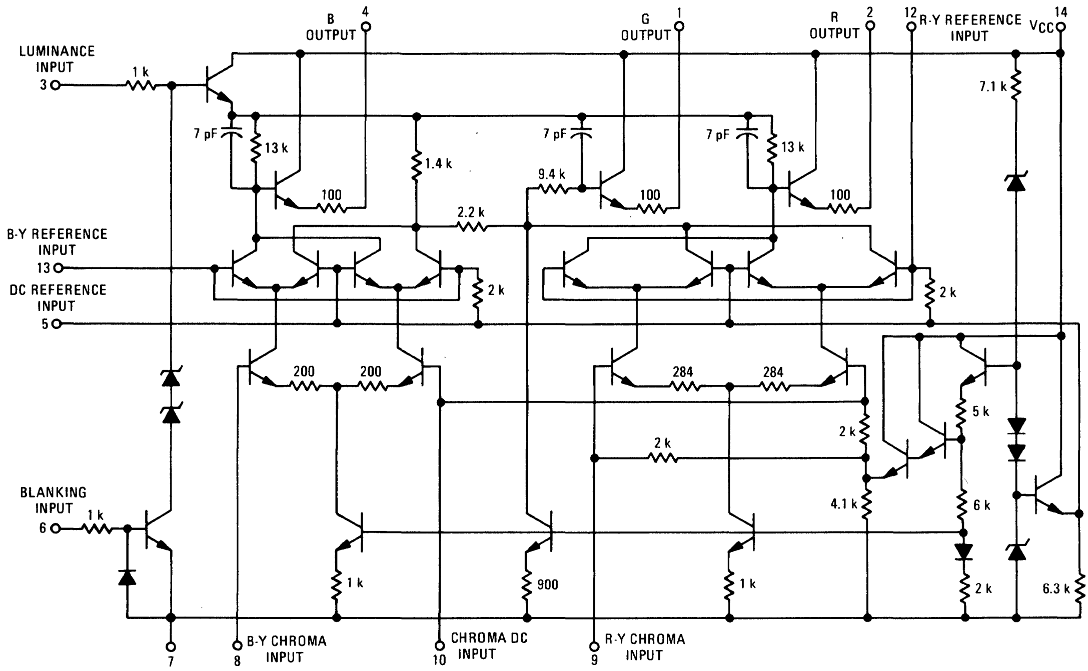


FIGURE 5 – POWER DISSIPATION



8

FIGURE 6 – CIRCUIT SCHEMATIC



MC1326

DUAL CHROMA DEMODULATOR

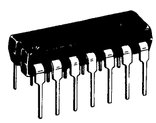
DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B MATRIX AND CHROMA DRIVER STAGES

. . . a monolithic device designed for use in solid-state color television receivers.

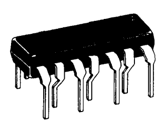
- Luminance Input Provided
- Good Chroma Sensitivity – 0.3 Vp-p Input for 5 Vp-p Output
- Low Differential Output DC Offset Voltage – 0.6 V max
- DC Temperature Stability – 3 mV/^{o}C typ
- Negligible Change in Output Voltage Swing with Varying 3.58 MHz Reference Input Signal
- High Ripple Rejection Achieved with MOS Filter Capacitors
- High Blue Output Voltage Swing – 10 Vp-p typ
- Blanking Input Provided

DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B OUTPUT MATRIX

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

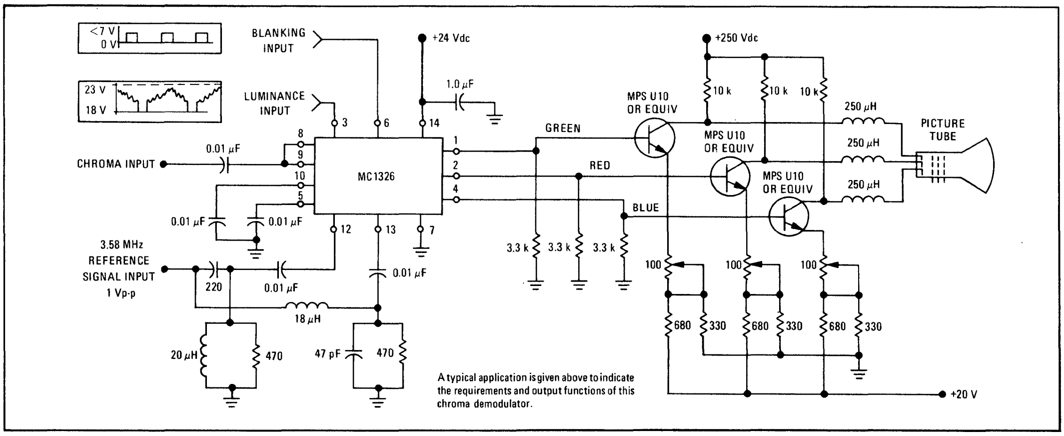


PQ SUFFIX
PLASTIC PACKAGE
CASE 647

MAXIMUM RATINGS (T_A = +25^{o}C unless otherwise noted)

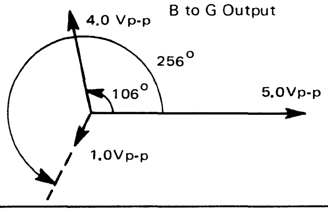
Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5.0	Vpk
Reference Signal Input Voltage	5.0	Vpk
Minimum Load Resistance	3.0	k ohms
Luminance Input Voltage	12	Vp-p
Blanking Input Voltage	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25^{o}C	 625 5.0	 mW mW/^{o}C
Operating Temperature Range (Ambient)	0 to +75	^{o}C
Storage Temperature Range	–65 to +150	^{o}C

FIGURE 1 – MC1326 TYPICAL APPLICATION



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Quiescent Output Voltage See Figure 2	1, 2, 4	13	14.4	16	Vdc
Quiescent Input Current from Supply (Figure 2) (R_L = ∞) (R_L = 3.3 k ohms)		 – 16.5	 6.0 19	 – 25.5	mA
Reference Input DC Voltage (Figure 2)	5,12,13	–	6.2	–	Vdc
Chroma Reference Input DC Voltage (Figure 2)	8,9,10	–	3.4	–	Vdc
Differential Output Voltage (Reference Input Voltage = 1.0 Vp-p) See Note 1 and Figure 3	1, 2, 4	–	0.3	0.6	Vdc
Output Voltage Temperature Coefficient (Reference Input Voltage = 1.0 Vp-p, +25° to +65°C) See Note 1 and Figure 3	1, 2, 4	–	3.0	–	mV/°C
DYNAMIC CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)					
Blue Output Voltage Swing See Note 2 and Figure 4	4	8.0	10	–	Vp-p
Chroma Input Voltage (B Output = 5.0 Vp-p) See Note 3 and Figure 4	8	–	0.3	0.7	Vp-p
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz)	1, 2, 4	 – –	 0.95 0.5	 – –	–
Blanking Input Resistance 1.0 Vdc 0 Vdc	6	 – –	 1.1 75	 – –	kΩ
Detected Output Voltage (Adjust B Output to 5.0 Vp-p, Luminance Voltage = 23 V) See Note 4 G Output R Output	4 1 2	 0.75 3.5	 1.0 3.8	 1.25 4.2	Vp-p
Relative Output Phase (B Output = 5.0 Vp-p, Luminance Voltage = 23 V) B to R Output B to G Output 	 4, 2 4, 1	 101 248	 106 256	 111 264	Degrees
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1, 2, 4	–	250	500	mVp-p
B-Y Phase Shift (B-Y Reference Input to B-Y Output)	4, 13	–	3	–	Degrees
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B Output = 5.0 Vp-p)	1, 2, 4	–	0.7	1.5	Vp-p
Reference Input Resistance (Chroma Input = 0)	12, 13	–	2.0	–	kΩ
Reference Input Capacitance (Chroma Input = 0)	12, 13	–	6.0	–	pF
Chroma Input Resistance	8, 9, 10	–	2.0	–	kΩ
Chroma Input Capacitance	8, 9, 10	–	2.0	–	pF

NOTES:

1. With Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage = 1.0 Vp-p, all output voltages will be within specified limits and will not differ from each other by greater than 0.6 Vdc.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 0.6 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5 Vp-p. The Chroma Input Voltage at this point should be equal to or less than 0.7 Vp-p.
4. With normal Reference Input Signal Voltage, adjust the Chroma Input Signal until the Blue Output Voltage = 5 Vp-p. At this point, the Red and Green voltages will fall within the specified limits.

8

TEST CIRCUITS

(V+ = 24 Vdc, R_L = 3.3 Kilohms, T_A = +25°C unless otherwise noted)

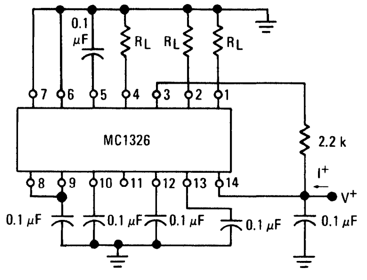


FIGURE 2 – DC TEST CIRCUIT WITHOUT REFERENCE INPUT SIGNAL VOLTAGE (B-Y AND R-Y)
(For Testing Quiescent Current, DC Output Voltage, Difference Voltage)

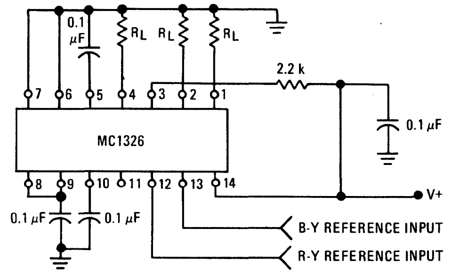


FIGURE 3 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

FIGURE 4 – DYNAMIC TEST CIRCUIT

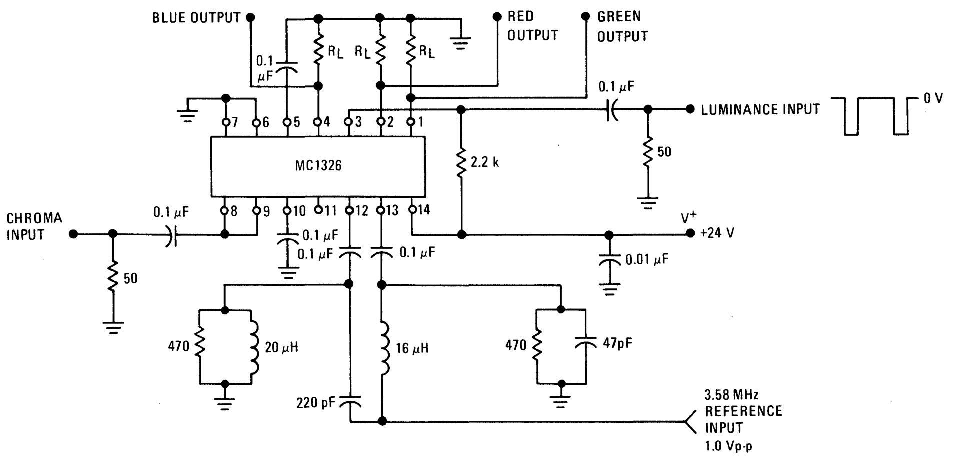


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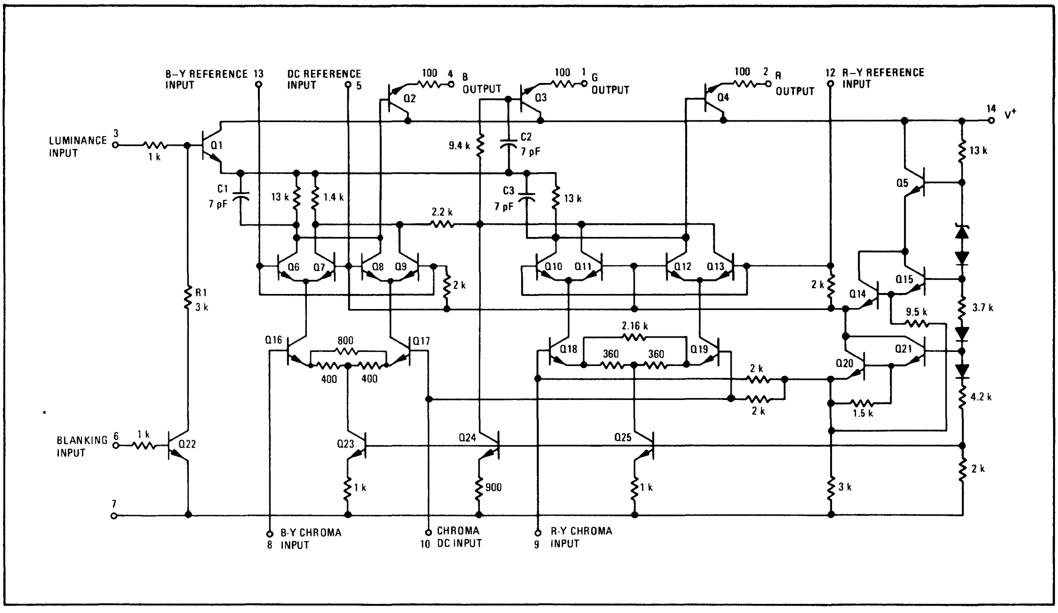
FIGURE 5 – CIRCUIT SCHEMATIC



CIRCUIT OPERATION

A double sideband suppressed carrier chroma signal flows between the bases of the two differential pairs, Q16 and Q17, Q18 and Q19. A reference signal of approximately 1 Vp-p amplitude having the same frequency as the suppressed chroma carrier with an appropriate phase relationship is supplied between the bases of the upper differential pairs Q6 and Q7, Q8 and Q9, Q10 and Q11, Q12 and Q13. The upper pairs are switched between full conduction and zero conduction at the carrier frequency rate. The collectors of the upper pairs are cross-coupled so that "doubly balanced" or "full-wave" synchronous detected chroma signals are obtained. Both positive and negative phases of the detected signal are available at opposite collector pairs.

While the detector section is almost identical to other available units, several excellent additional features are incorporated. Transistor Q1 is used as an emitter follower to which the collector load resistors of the detectors are returned. The collector impedances of the upper pair transistors are high compared with the collector load resistors, and any signal at the emitter of Q1 appears virtually unattenuated at the collectors of the upper pairs, and hence at the three detector output terminals. This feature may be used to mix the correct amount of the luminance portion of the color TV signal with the color difference signals produced by the detectors to give R-G-B outputs directly.

Capacitors C1, C2, and C3 compensate for most of the high frequency roll-off in the luminance signal. This is due to the collector capacitances of the detector transistors and the input capacitances of the emitter followers, Q2, Q3, Q4. Capacitors C1, C2, and C3 provide filtering of carrier harmonics from the detected color difference signals. This increases the available swing before clipping for the color difference signal, and reduces the high frequency components which must pass through the emitter followers (Q2, Q3, Q4) into the video output stages. Since high capacitance (>100 pF) is characteristic of the input impedance of a video output stage, the transistor emitter followers must operate at a high quiescent current (>5 mA) in order to pass large high frequency components without distortion. The filtering reduces the quiescent current required in the emitter followers and thus reduces dissipation in the integrated circuit.

If it is not required to mix the luminance signal via Q1, this transistor can be used for brightness control. If the base of Q1 is connected to a suitable variable dc voltage, this will vary the dc output levels of the three detected outputs accordingly and thereby vary the picture brightness level.

Blanking of the picture during line and frame flyback may be achieved by applying a positive-going blanking signal to the base of Q22. With an extra external resistor in series with the Q1 base of approximately 5 k ohms, when Q22 is turned on by the blanking pulse, the base of Q1 will be pulled negative by the current in R1, thus forcing all three detected outputs to go negative by the same amount. In a conventional solid-state receiver with a single video output stage driving the picture tube cathode, a negative-going signal at the base of the video output stage will blank the picture tube. When using the blanking input be certain the blanking pulse does not switch off the luminance input stage Q1 completely; this would turn off the collector supply for the demodulators and put the entire chroma demodulator out of lock at each blanking pulse.

Matrix for MC1326

$$\frac{\text{R-Y gain}}{\text{B-Y gain}} = 0.77$$

$$-G\text{-}Y = 0.11\ (B\text{-}Y) + 0.28\ (R\text{-}Y)$$

For indicated requirements and output functions of the MC1326 chroma demodulator please refer to the typical application shown on the first page of this specification.

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

(Figures 6 through Figure 10 Reference Test Circuit of Figure 2)

FIGURE 6 – DC OUTPUT VOLTAGE

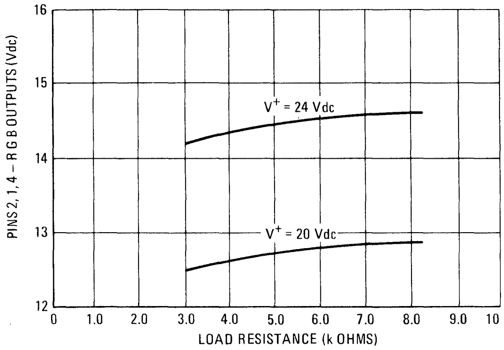


FIGURE 7 – POWER DISSIPATION

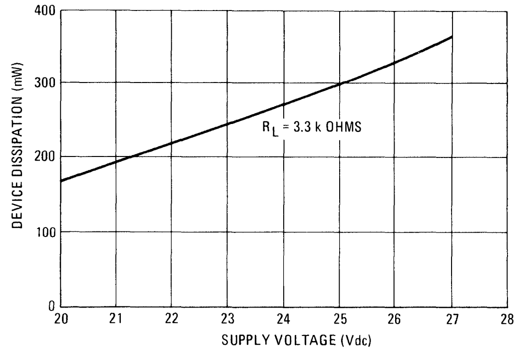


FIGURE 8 – DC OUTPUT VOLTAGE

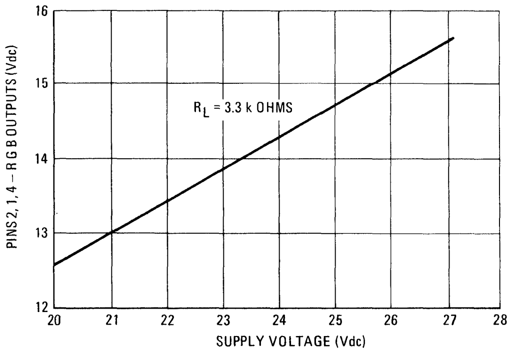


FIGURE 9 – POWER DISSIPATION

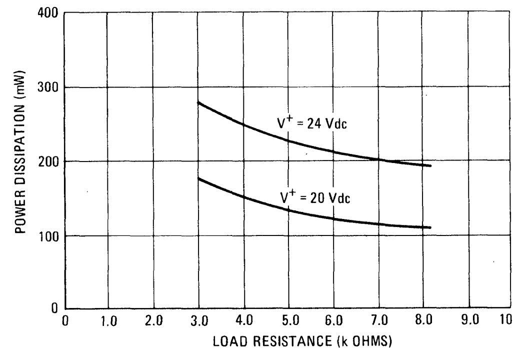


FIGURE 10 – DC OUTPUT VOLTAGE

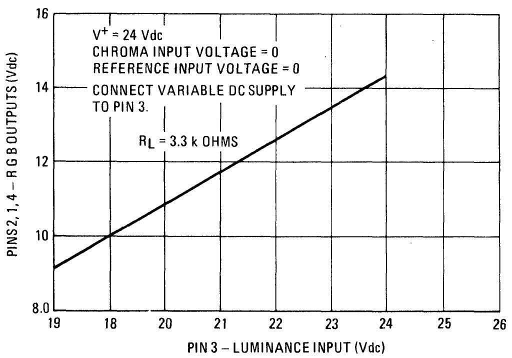
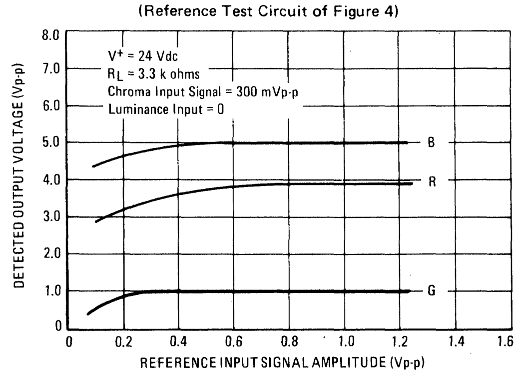


FIGURE 11 – DETECTED OUTPUT VOLTAGE

(Reference Test Circuit of Figure 4)



TYPICAL CHARACTERISTICS (continued)
(T_A = +25°C unless otherwise noted)

(Figures 12 through Figure 17 Reference Test Circuit of Figure 4)

FIGURE 12 – OUTPUT VOLTAGE

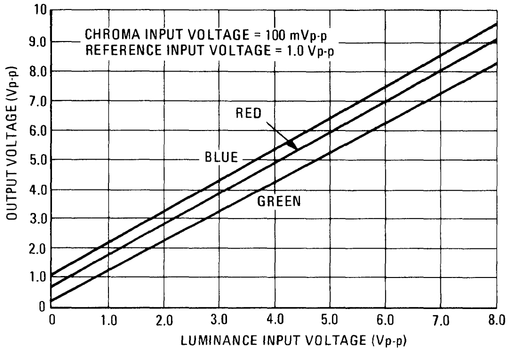


FIGURE 13 – GREEN OUTPUT

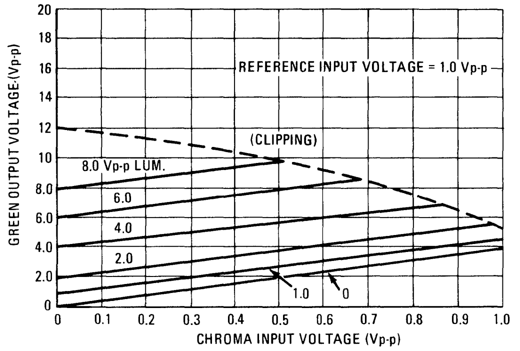


FIGURE 14 – RED OUTPUT

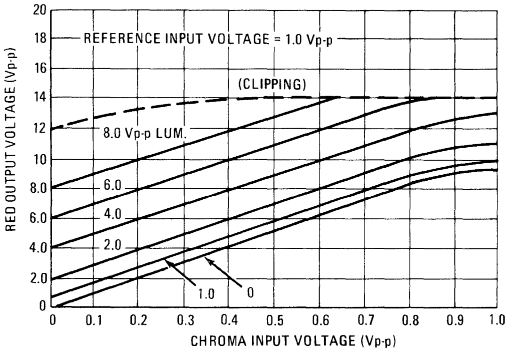


FIGURE 15 – BLUE OUTPUT

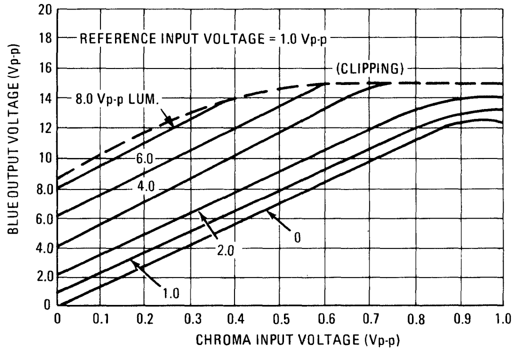


FIGURE 16 – LUMINANCE BANDWIDTH

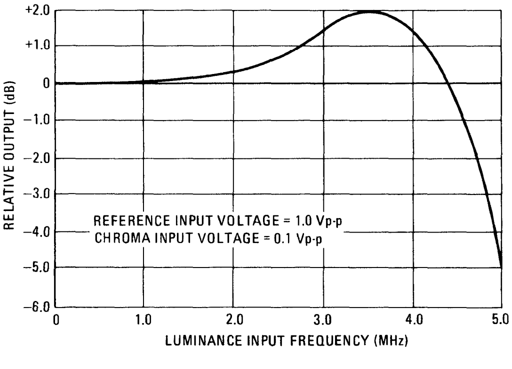
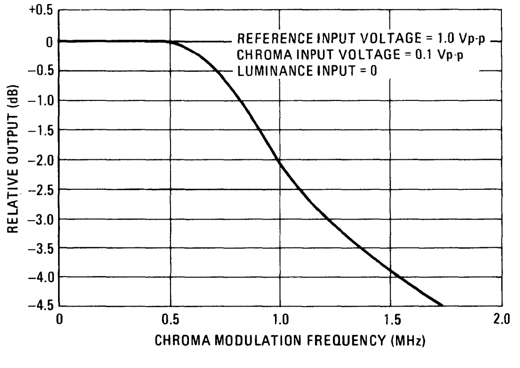


FIGURE 17 – CHROMA BANDWIDTH



8

MC1327

CHROMA DEMODULATOR

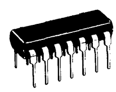
DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH RGB MATRIX, PAL SWITCH, AND CHROMA DRIVER STAGES

. . . a monolithic device designed for use in solid-state color television receivers.

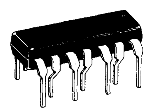
- Good Chroma Sensitivity – 0.28 Vp-p Input Typical for 5.0 Vp-p Output
- Low Differential Output DC Offset Voltage – 0.6 V Maximum
- Differential DC Temperature Stability – 0.7 mV/^{o}C
- High Blue Output Voltage Swing – 10 Vp-p Typical
- Blanking Input Provided
- Luminance Bandwidth Greater than 5.0 MHz

DUAL DOUBLY BALANCED CHROMA DEMODULATOR with RGB OUTPUT MATRIX AND PAL SWITCH

MONOLITHIC SILICON INTEGRATED CIRCUIT

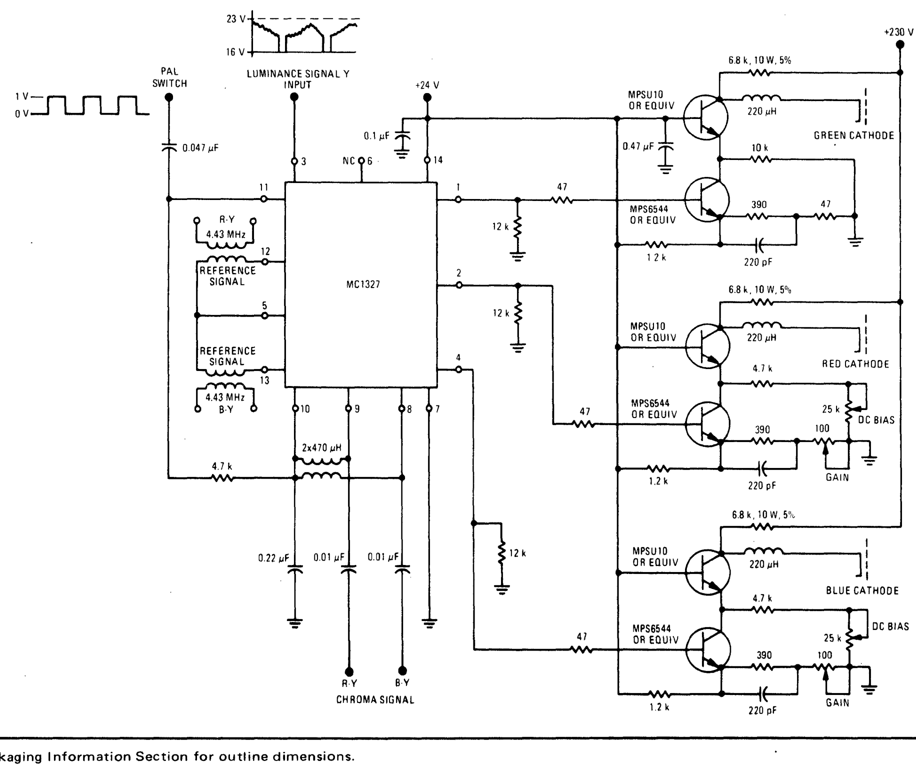


P SUFFIX
PLASTIC PACKAGE
CASE 646



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

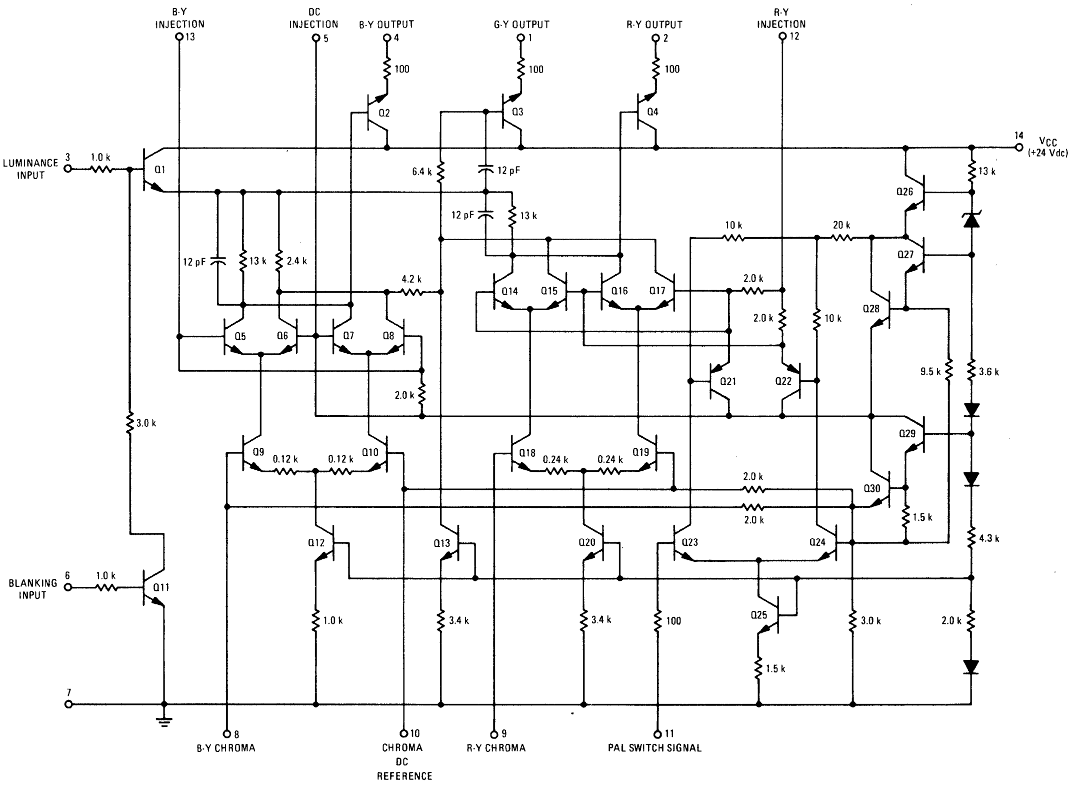
Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5.0	Vpk
Reference Signal Input Voltage	5.0	Vpk
Minimum Load Resistance	3.0	k ohms
Luminance Input Voltage	12	Vp-p
Blanking Input Voltage	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Quiescent Output Voltage (See Figure 2)	1,2,4	13.2	14.5	15.8	Vdc
Quiescent Input Current from Supply (Figure 2) ($R_L = \infty$) (R_L = 3.3 k ohms)		 – 16	 7.5 19	 – 26	mA
Reference Input DC Voltage (Figure 2)	5,12,13	–	6.2	–	Vdc
Chroma Reference Input DC Voltage (Figure 2)	8,9,10	–	3.4	–	Vdc
Differential Output Voltage (See Note 1 and Figure 2)	1,2,4	–	0.3	0.6	Vdc
Differential Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C)	1,2,4	 –	 0.7	 –	mV/°C
Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C)	1,2,4	–	+0.5	±5.0	mV/°C
DYNAMIC CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)					
Blue Output Voltage Swing (See Note 2 and Figure 3)	4	8.0	10	–	Vp-p
Chroma Input Voltage (B Output = 5.0 Vp-p) (See Note 3 and Figure 3)	8	–	280	550	mVp-p
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz, reference at 100 kHz)	1,2,4	 – –	 0.95 -1.8	 – –	– dB
Differential Luminance Gain, RGB Outputs (@ 5.0 MHz)		 –	 0.3	 –	dB
Blanking Input Resistance (1.0 Vdc) (0 Vdc)	6	 – –	 1.1 75	 – –	kΩ
Detected Output Voltage (Adjust B Output to 5.0 Vp-p, Luminance Voltage = 23 V) (See Note 4) G Output R Output	4 1 2	 1.4 2.5	 1.8 2.9	 2.2 3.3	Vp-p
PAL Switch Operating Voltage Range (7.8 kHz Square Wave)	11	 0.3	 –	 3.0	Vp-p
R-Y Output dc Offset with PAL Switch Operation		–	–	100	mVdc
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1,2,4	–	200	300	mVp-p
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B Output = 5.0 Vp-p)	1,2,4	–	0.6	1.0	Vp-p
Reference Input Resistance (Chroma Input = 0)	12,13	–	2.0	–	kΩ
Reference Input Capacitance (Chroma Input = 0)	12,13	–	6.0	–	pF
Chroma Input Resistance	8,9,10	–	2.0	–	kΩ
Chroma Input Capacitance	8,9,10	–	2.0	–	pF

NOTES:
1. Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage = 1.0 Vp-p.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 1.2 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5.0 Vp-p.
4. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5.0 Vp-p. At this point, the Red and Green voltages will fall within the specified limits.

MC1327 CHROMA DEMODULATOR (PAL)



TEST CIRCUITS

(V_{CC} = 24 Vdc, R_L = 3.3 kilohms, T_A = +25°C unless otherwise noted)

FIGURE 2 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

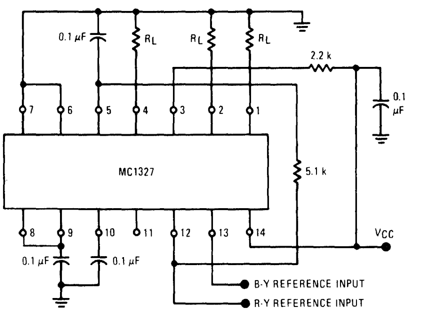
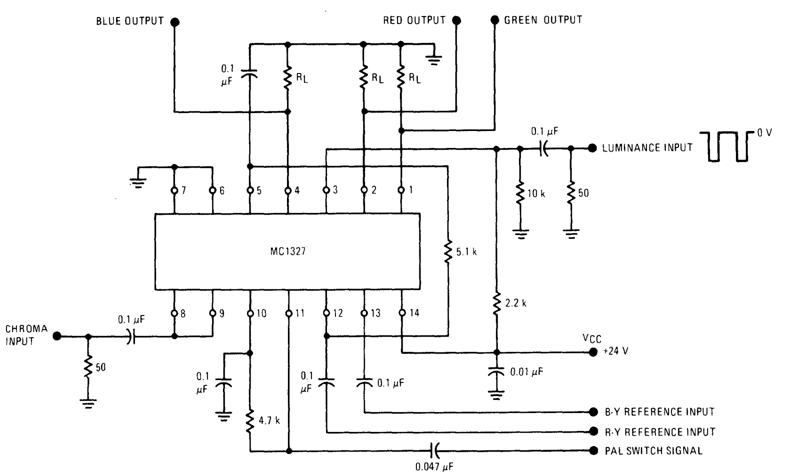


FIGURE 3 – DYNAMIC TEST CIRCUIT



8

MC1328

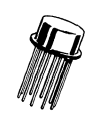
DUAL CHROMA DEMODULATOR

MONOLITHIC DUAL DOUBLY BALANCED CHROMA DEMODULATOR

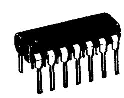
- Good Chroma Sensitivity (0.3 Vp-p Input Produces 5.0 Vp-p Output)
- Good dc Temperature Stability (3 mV/°C typ)
- Low Output dc Offset Voltages (0.6 V max)
- Pin Compatible with ULN-2114, ULN-2114A
- Negligible Change in Output Voltage Swing With Varying 3.58 MHz Reference Signal
- High Ripple Rejection Due To Built-In MOS Filter Capacitors
- High Output Voltage Swing (10 Vp-p Typ) – B-Y

DUAL DOUBLY BALANCED CHROMA DEMODULATOR

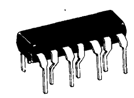
Monolithic Silicon Integrated Circuit



G SUFFIX
METAL PACKAGE
CASE 603
(TO-100)

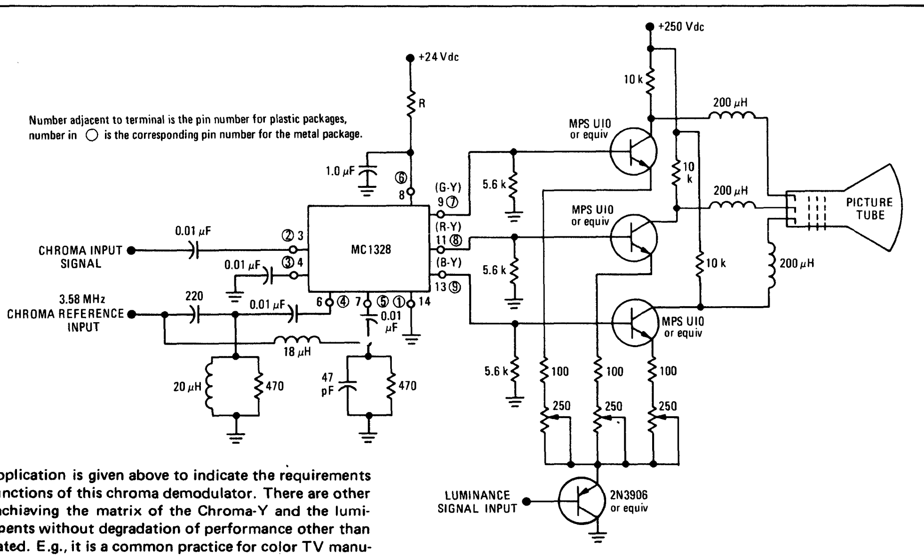


P SUFFIX
PLASTIC PACKAGE
CASE 646



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – MC1328 TYPICAL APPLICATION



A practical application is given above to indicate the requirements and output functions of this chroma demodulator. There are other methods of achieving the matrix of the Chroma-Y and the luminance components without degradation of performance other than the one indicated. E.g., it is a common practice for color TV manufacturers to matrix in the picture tube.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Power Dissipation (Package Limitation)		
Plastic Packages	625	mW
Derate above T_A = +25°C	5.0	mW/°C
Metal Package	680	mW
Derate above T_A = +25°C	4.5	mW/°C
Chroma Signal Input Voltage	5.0	Vpk
Reference Signal Input Voltage	5.0	Vpk
Minimum Load Resistance	3.0	k ohms
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

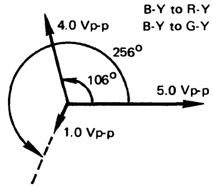
Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

STATIC CHARACTERISTICS

Characteristic	Pin No. Suffix G Pkg	Pin No. Suffix P, PQ Pkgs	Min	Typ	Max	Unit
Quiescent Output Voltage See Figure 2	7,8,9	9,11,13	13	14.3	16	Vdc
Quiescent Input Current (See Figure 2) (R_L = ∞, Chroma and Reference Input Voltages = 0)	6	8	–	6.0	–	mA
(R_L = 3.3 k ohms, Chroma and Reference Input Voltages = 0)			16.5	19	25.5	
Reference Input DC Voltage	4,5	6,7	–	6.2	–	Vdc
Chroma Input DC Voltage	2,3	3,4	–	3.4	–	Vdc
Differential Output Voltage See Note 1 and Figure 3	7,8,9	9,11,13	–	0.3	0.6	Vdc
Output Temperature Coefficient (No Output Differential Voltage > 0.6 Vdc, +25°C to +65°C) See Note 1 and Figure 3	7,8,9	9,11,13	–	3.0	–	mV/°C

DYNAMIC CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, Referenced Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

Detected Output Voltage (B-Y) See Note 2	9	13	8.0	9.0	–	Vp-p
Chroma Input Voltage (B-Y Output = 5.0 Vp-p) See Note 3	2	3	–	0.3	0.7	Vp-p
Detected Output Voltage (Adjust B-Y Output to 5.0 Vp-p) See Note 4 G-Y	7	9	0.75	1.0	1.25	Vp-p
R-Y	8	11	3.5	3.8	4.2	
Relative Output Phase (B-Y Output = 5.0 Vp-p) B-Y to R-Y	9-8	13-11	101	106	111	Degrees
B-Y to G-Y	9-7	13-9	248	256	264	
						
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	7,8,9	9,11,13	–	250	500	mVp-p
B-Y Phase Shift (B-Y Reference Input to B-Y Output)	5-9	7-13	–	3	–	Degrees
Residual Carrier and Harmonics (with Input Signal Voltage, normal Reference Signal Voltage and B-Y = 5.0 Vp-p)	7,8,9	9,11,13	–	–	1.5	Vp-p
Reference Input Resistance (Chroma Input = 0)	4,5	6,7	–	2.0	–	k ohms
Reference Input Capacitance (Chroma Input = 0)	4,5	6,7	–	6.0	–	pF
Chroma Input Resistance	2,3	3,4	–	2.0	–	k ohms
Chroma Input Capacitance	2,3	3,4	–	2.0	–	pF

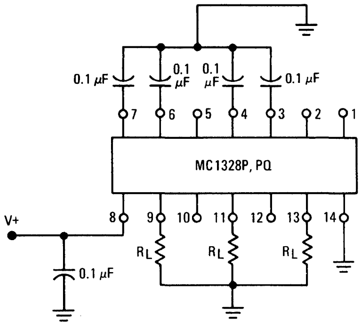
NOTES:

1. With Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage (1.0 Vp-p),all output voltages will be within specified limits and will not differ from each other by greater than 0.6 Vdc.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 0.6 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the B-Y Output Voltage = 5 Vp-p. The Chroma Input Voltage at this point should be equal to or less than 0.7 Vp-p.
4. With normal Reference Input Signal Voltage, adjust the Chroma Input Signal until the B-Y Output Voltage = 5 Vp-p. At this point, the R-Y and G-Y voltages will fall within the specified limits.

TEST CIRCUITS

(V^+ = 24 Vdc, R_L = 3.3 kΩ, T_A = +25°C unless otherwise noted)

FIGURE 2 – TEST CIRCUIT WITH NO REFERENCE INPUT SIGNAL



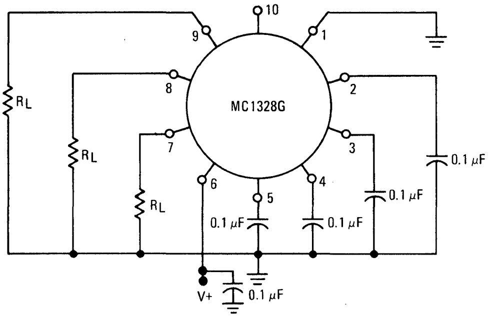
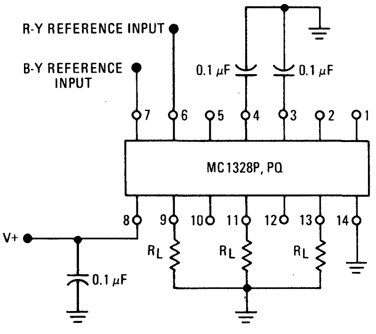
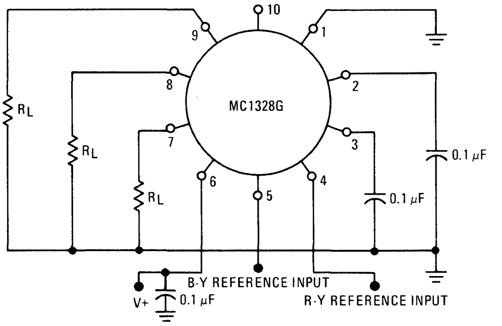


FIGURE 3 – TEST CIRCUIT WITH REFERENCE INPUT SIGNAL

(Quiescent Current, DC Output Voltage, Difference Voltage)





TYPICAL CHARACTERISTICS

FIGURE 4 – DETECTED OUTPUT

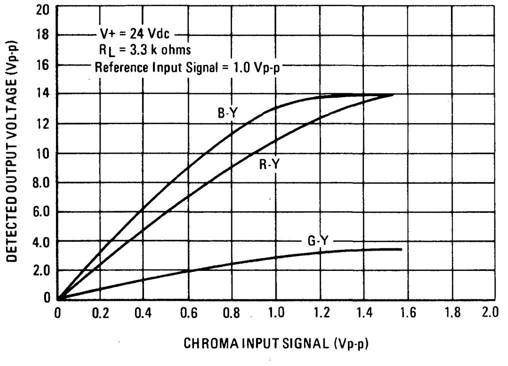
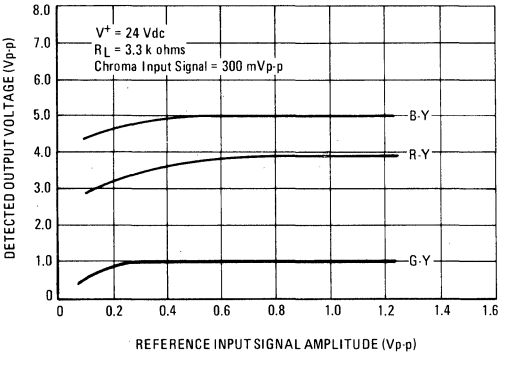


FIGURE 5 – DETECTED OUTPUT



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TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – DETECTED OUTPUT VOLTAGE

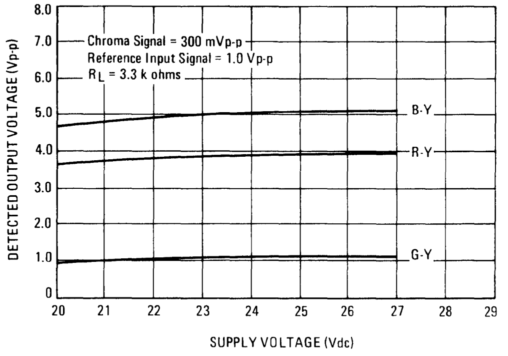


FIGURE 7 – DC OUTPUT VOLTAGE

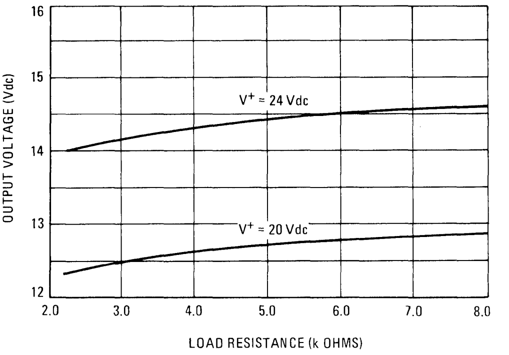


FIGURE 8 – DC OUTPUT VOLTAGE

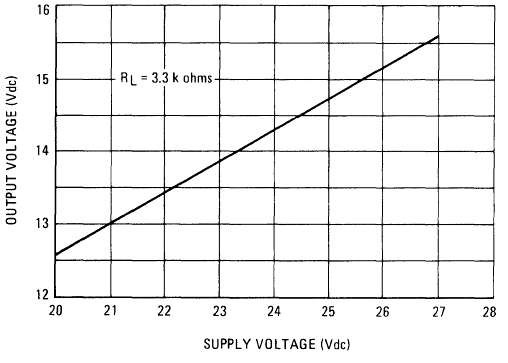


FIGURE 9 – POWER DISSIPATION

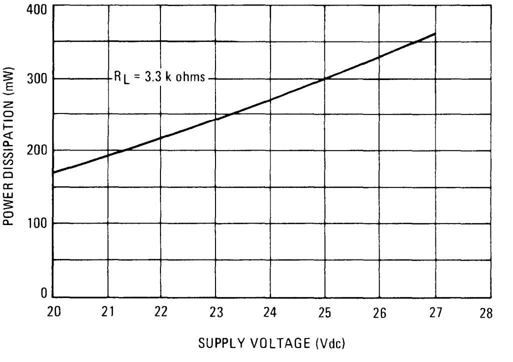
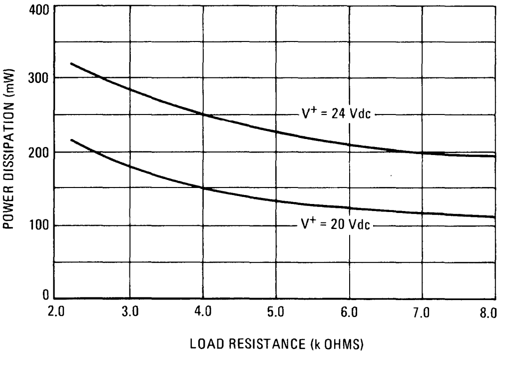
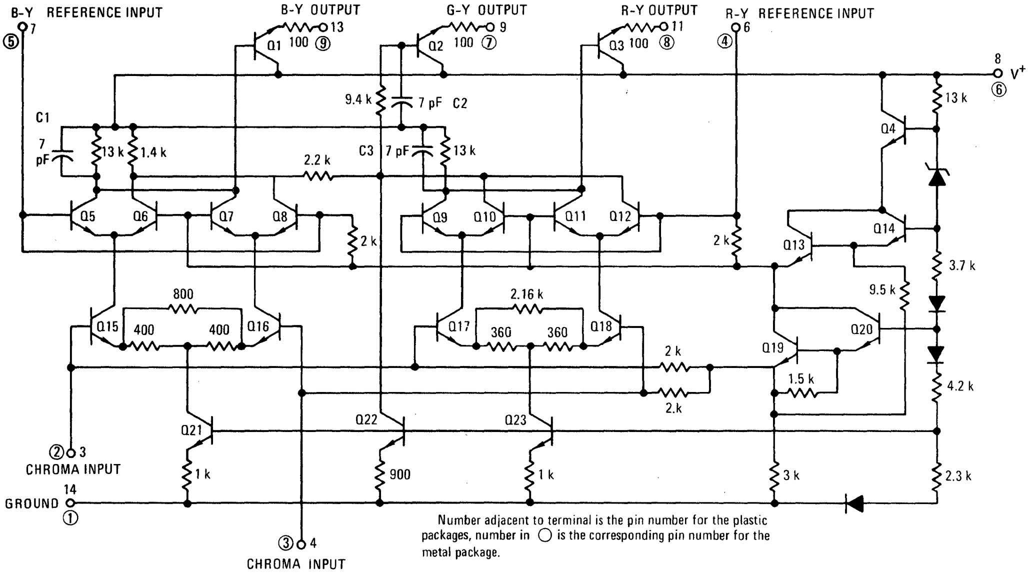


FIGURE 10 – POWER DISSIPATION



8

FIGURE 11 – CIRCUIT SCHEMATIC



CIRCUIT OPERATION

A double sideband suppressed carrier chroma signal flows between the bases of the two differential pairs, Q15 and Q16, Q17 and Q18. A reference signal of approximately 1 Vp-p amplitude having the same frequency as the suppressed chroma carrier with an appropriate phase relationship is supplied between the bases of the upper differential pairs Q5 and Q6, Q7 and Q8, Q9 and Q10, Q11 and Q12. The upper pairs are switched between full conduction and zero conduction at the carrier frequency rate. The collectors of the upper pairs are cross-coupled so that "doubly balanced" or "full-wave" synchronous detected chroma signals are obtained. Both positive and negative phases of the detected signal are available at opposite collector pairs.

Capacitors C1, C2 and C3 provide filtering of carrier harmonics from the detected color difference signals. This increases the available swing before clipping for the color difference signal, and reduces the high frequency components which must pass through the emitter followers (Q1, Q2, Q3) into the video output stages. Since high capacitance (>100 pF) is characteristic of the input impedance of a video output stage, the transistor emitter followers must operate at a high quiescent current (>5 mA) in order to pass large high frequency components without distortion. The filtering reduces the quiescent current required in the emitter followers and thus reduces dissipation in the integrated circuit.

8

DUAL CHROMA DEMODULATOR

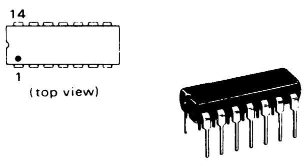
MC1329P

MONOLITHIC DUAL DOUBLY BALANCED CHROMA DEMODULATOR

- Good Chroma Sensitivity (0.36 V(p-p) Input Produces 5.0 V(p-p) Output)
- Good dc Temperature Stability (3 mV/^{o}C typ)
- Low Output dc Offset Voltages (0.6 V max)
- Pin Compatible with ULN-2114, ULN-2114A
- Negligible Change in Output Voltage Swing With Varying 3.58-MHz Reference Signal
- High Ripple Rejection Due to Built-In MOS Filter Capacitors
- High Output Voltage Swing (11 V(p-p) Typ – B-Y)
- Short-Circuit Protected Outputs

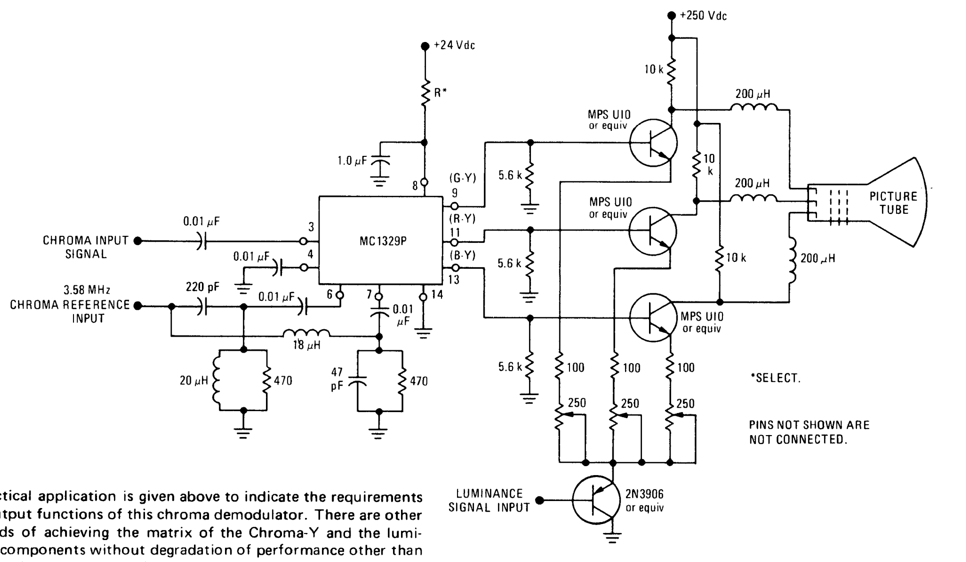
DUAL DOUBLY BALANCED CHROMA DEMODULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – MC1329P TYPICAL APPLICATION



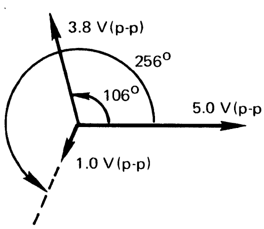
A practical application is given above to indicate the requirements and output functions of this chroma demodulator. There are other methods of achieving the matrix of the Chroma-Y and the luminance components without degradation of performance other than the one indicated. E.g., it is a common practice for color TV manufacturers to matrix in the picture tube.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise specified.)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Chroma Signal Input Voltage	5.0	V(pk)
Reference Signal Input Voltage	5.0	V(pk)
Minimum Load Resistance	2.2	k ohms
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3.3 k ohms, V_{ref} = 1.0 V(p-p), T_A = +25°C unless otherwise noted.)

Characteristics		Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS (See Figure 2.)						
Quiescent Output Voltage		9,11,13	13	14.5	16	Vdc
Quiescent Input Current (R_L = ∞) (R_L = 3.3 k ohms)		8	 – 16.5	 6.0 19	 – 25.5	mA
Reference Input dc Voltage		6,7	–	6.9	–	Vdc
Chroma Input dc Voltage		3,4	–	3.6	–	Vdc
Differential Output Voltage		9-11, 9-13, 11-13	–	0.3	0.6	Vdc
Output Temperature Coefficient (No Output Differential Voltage > 0.6 Vdc, +25°C to +65°C)		9,11,13	–	3.0	–	mV/°C
DYNAMIC CHARACTERISTICS (Pin 4 bypassed to ground, chroma (3.56 MHz) on pin 3.)						
Detected Output Voltage See Note 1.	 +(B-Y) –(B-Y)	13	 4.0 4.0	 5.5 5.5	 – –	V(p-p)
Chroma Input Voltage (B-Y Output = 5.0 V[p-p]) See Note 2.		3	–	0.36	0.7	V(p-p)
Detected Output Voltage (Adjust B-Y Output to 5.0 V[p-p])	 G-Y R-Y	 9 11	 0.75 3.5	 1.0 3.8	 1.25 4.2	V(p-p)
Relative Output Phase (B-Y Output = 5.0 V[p-p]) 	 B-Y to R-Y B-Y to G-Y	 13-11 13-9	 101 248	 106 256	 111 264	Degrees
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)		9,11,13	–	100	500	mV(p-p)
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B-Y = 5.0 V[p-p])		9,11,13	–	–	1.0	V(p-p)
Reference Input Resistance		6,7	–	2.0	–	k ohms
Reference Input Capacitance		6,7	–	6.0	–	pF
Chroma Input Resistance		3,4	–	1.0	–	k ohms
Chroma Input Capacitance		3,4	–	2.0	–	pF

NOTES:

1. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 1.2 V(p-p).
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the B-Y Output Voltage = 5.0 V(p-p). The Chroma Input Voltage at this point should be equal to or less than 0.7 V(p-p).

TYPICAL CHARACTERISTICS

(V_{CC} = 24 Vdc, R_L = 3.3 kΩ, T_A = +25°C unless otherwise noted.)

FIGURE 2 – TEST CIRCUIT WITH REFERENCE INPUT SIGNAL
(Quiescent Current, DC Output Voltage, Difference Voltage)

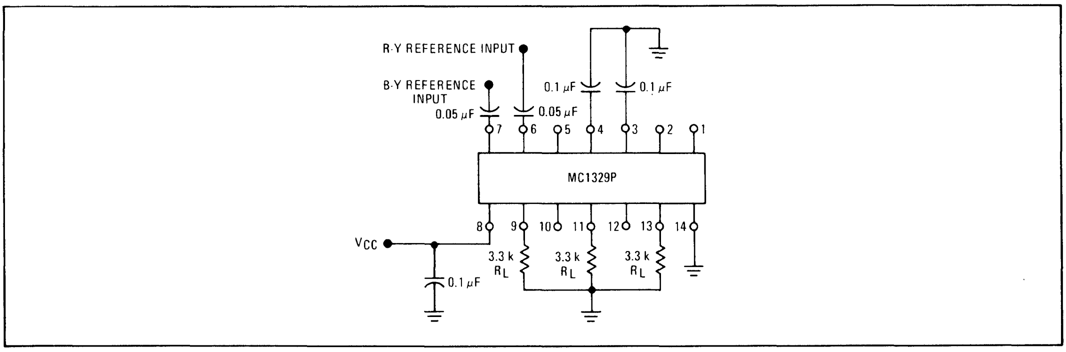


FIGURE 3 – DETECTED OUTPUT

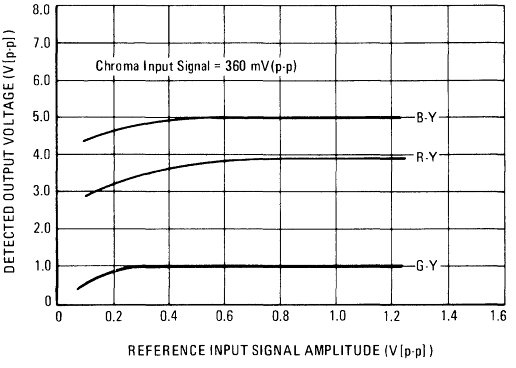


FIGURE 4 – DETECTED OUTPUT VOLTAGE

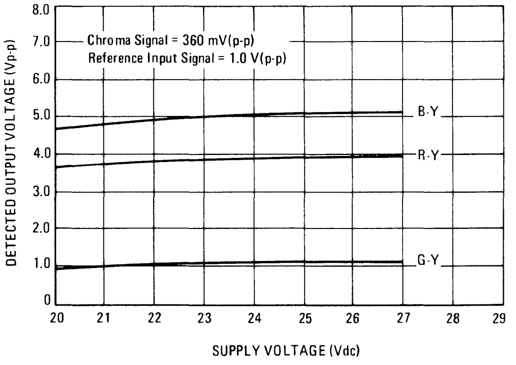
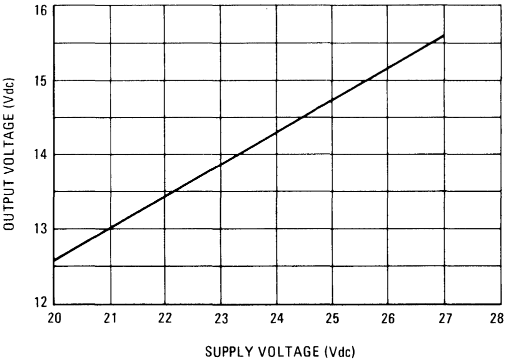
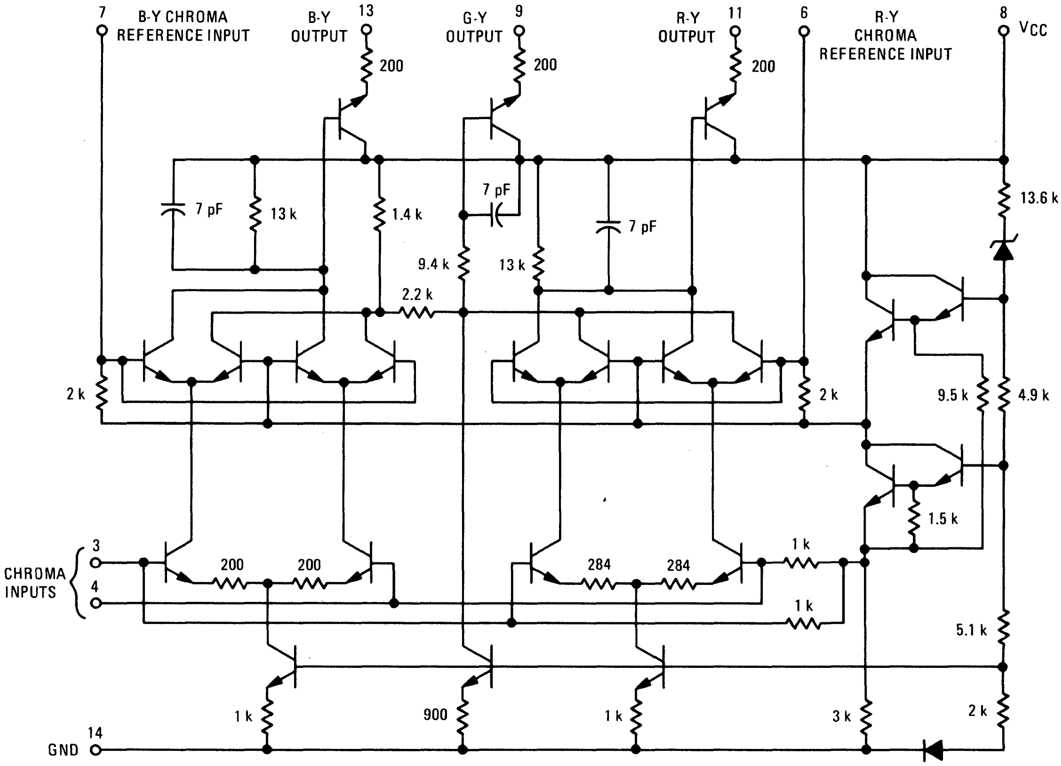


FIGURE 5 – POWER DISSIPATION



8

FIGURE 6 – CIRCUIT SCHEMATIC



MC1330P

VIDEO DETECTOR

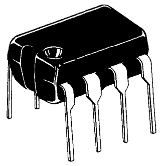
MONOLITHIC LOW-LEVEL VIDEO DETECTOR

. . . an integrated circuit featuring very linear video characteristics, wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and the AFC buffer.

- Conversion Gain – 34 dB typ
- Video Frequency Response @ 6.0 MHz < 1.0 dB
- Input of 36 mV Produces 3.0 Vp-p Output
- High Video Output – 7.7 Vp-p
- Fully Balanced Detector
- High Rejection of IF Carrier
- Low Radiation of Spurious Frequencies

LOW-LEVEL VIDEO DETECTOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	+24	Vdc
Supply Current	26	mAdc
Input Voltage	1.0	V(rms)
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

FIGURE 1 – DETECTED COLOR BARS

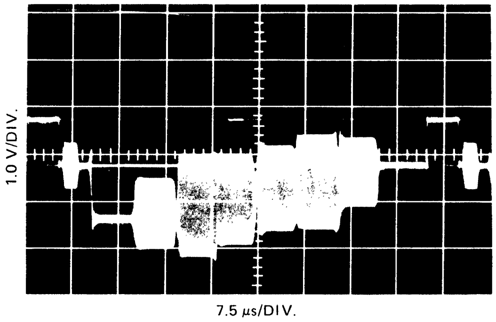
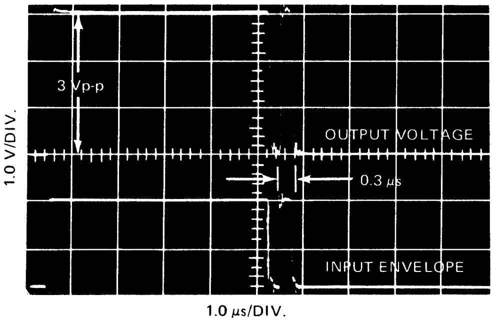


FIGURE 2 – PULSE RESPONSE



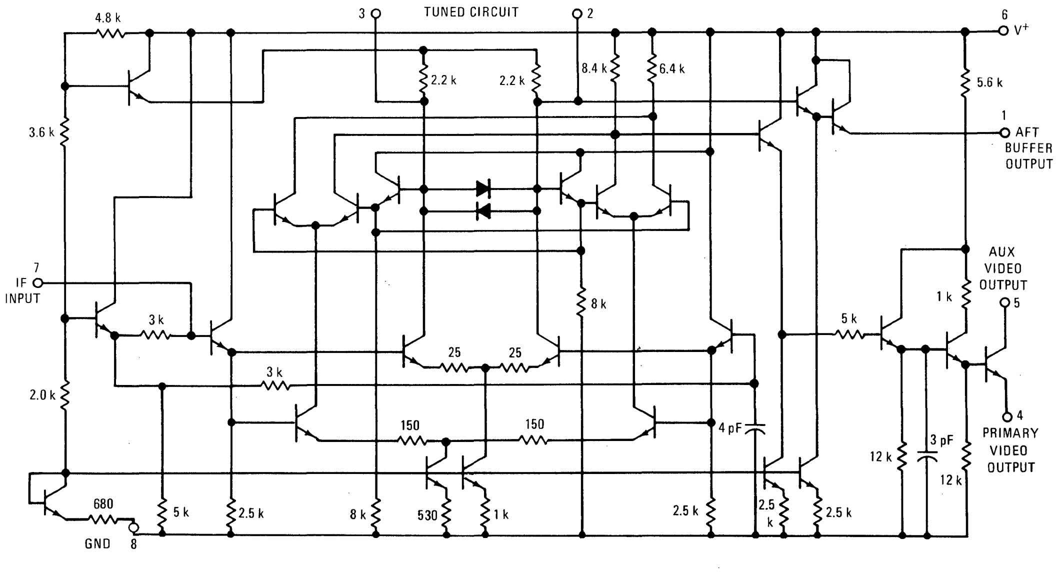
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = 20 Vdc, Q = 30, f_C = 45 MHz, T_A = +25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage Range	6	12	20	24	Vdc
Supply Current	5,6	–	15	–	mA
Zero Signal dc Output Voltage	4	6.8	7.7	8.3	Vdc
Maximum Signal dc Output Voltage	4	–	0	–	Vdc
Input Signal Voltage for 3.0 Vp-p Video Output (90% Modulation)	7	–	36	–	mV(rms)
Maximum Output Voltage Swing	4	–	7.7	–	Vp-p
Carrier Rejection at Output	4	42	60	–	dB
Carrier Output Voltage (at 3.0 Vp-p output) $f_{out} = f_C$ $f_{out} = 2 f_C$		 – –	 1.0 3.0	 – –	mV(rms)
3.0 dB Bandwidth of IF Carrier	7	–	80	–	MHz
3.0 dB Bandwidth of Video Output	4	–	12.3	–	MHz
Input Resistance Input Capacitance	7	– –	3.5 3.0	– –	kilohms pF
Output Resistance	4	–	180	–	ohms
Internal Resistance } (across tuned circuit) Internal Capacitance }	2,3	– –	4.4 1.0	– –	kilohms pF
AFT Buffer Output at Carrier Frequency ①	1	–	350	–	mVp-p
AFT Buffer dc Level	1	–	6.5	–	Vdc

① Measured with 10 times probe.

FIGURE 3 – CIRCUIT SCHEMATIC



8

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 4 – TEST CIRCUIT

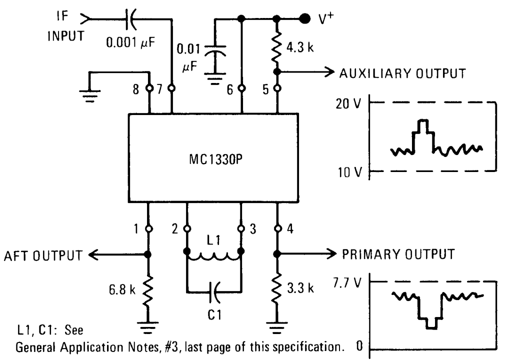


FIGURE 5 – OUTPUT VOLTAGE

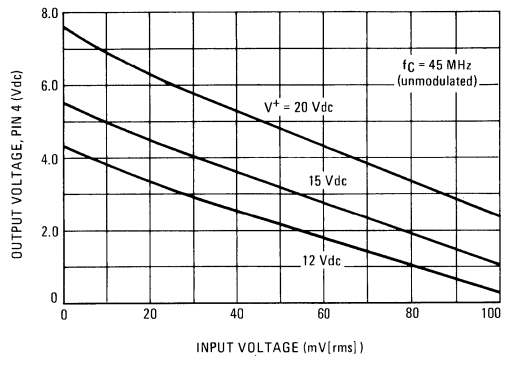


FIGURE 6 – OUTPUT VOLTAGE

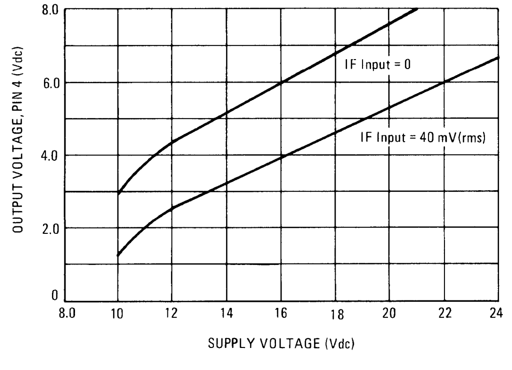


FIGURE 7 – DETECTOR LINEARITY

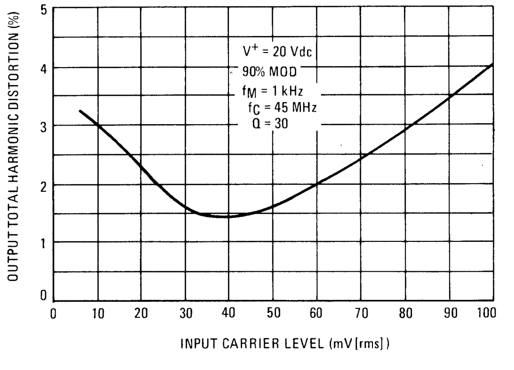


FIGURE 8 – VIDEO FREQUENCY RESPONSE

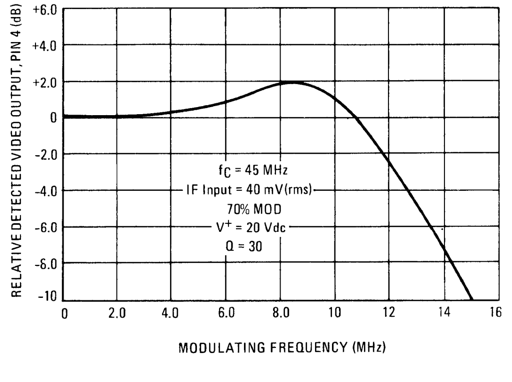
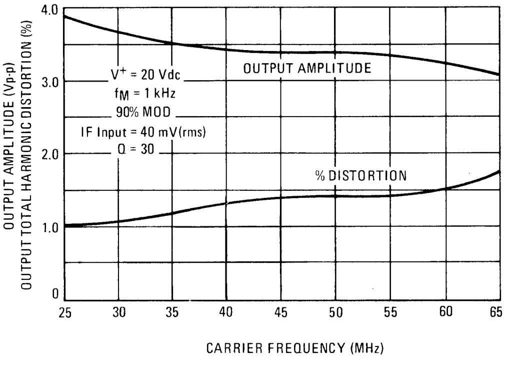


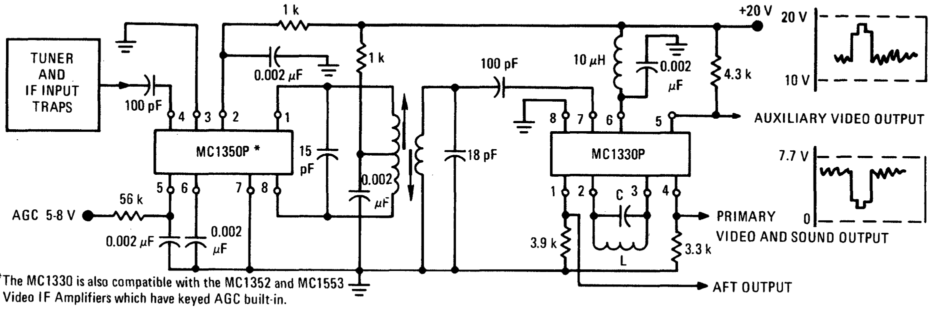
FIGURE 9 – CARRIER FREQUENCY PERFORMANCE



8

APPLICATIONS INFORMATION

FIGURE 10 – COLOR IF AMPLIFIER TYPICAL APPLICATION

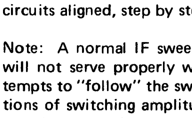


*The MC1330 is also compatible with the MC1352 and MC1553 Video IF Amplifiers which have keyed AGC built-in.

TV-IF Amplifier Information

A very compact high performance IF amplifier constructed as shown in Figure 11 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 84 dB voltage gain and can accomodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1350P input ($Z_{in} \approx 7.0$ kilohms). The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3 volt peak-to-peak output can be varied from 0 to 7.0 V with excellent linearity and freedom from spurious output products.

FIGURE 11 – TRANSFORMER



Primary Winding: 8 turns of AWG #26 close wound, CT
Secondary Winding: 6 turns of AWG #26 close wound, CT
Core: Arnold Type-TH slugs or equiv.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate the low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.
This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude.

MC1330P General Information

The MC1330P offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode.
Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:
1. The device provides excellent linearity of output versus input, as shown in Figure 6. This graph also shows that video peak-to-peak amplitude (ac) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)
2. The dc output level does change linearly with supply voltage. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.
3. The choice of Q for the tuned circuit of pins 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. Values of Q from 20 to 50 are recommended. (Note the internal resistance.)
4. A video output with positive-going sync is available at pin 5 if required. This signal has a higher output impedance than pin 4 so it must be handled with greater care. If not used, pin 5 may be connected directly to the supply voltage (pin 6).
5. An AFT output (pin 1) provides 350 mV of clipped carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.

8

MC1331P

VIDEO DETECTOR

Product Preview

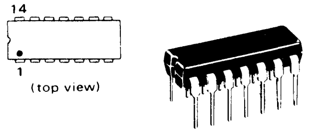
MONOLITHIC LOW-LEVEL VIDEO DETECTOR

. . . an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer, AFC buffer, sound IF detector, and sync separator.

- Conversion Gain – 34 dB typical
- Video Frequency Response at 6.0 MHz < 3.0 dB
- Input of 36 mV Produces 3.0 V(p-p) Output
- High Video Output – 6.0 V(p-p)
- Fully Balanced Detector
- Separate Sound Detector
- Differential Inputs

LOW-LEVEL VIDEO DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – OUTPUT VOLTAGE

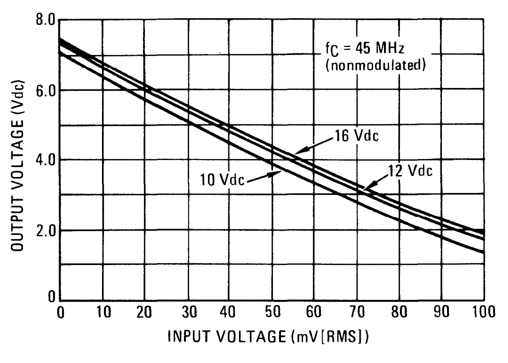
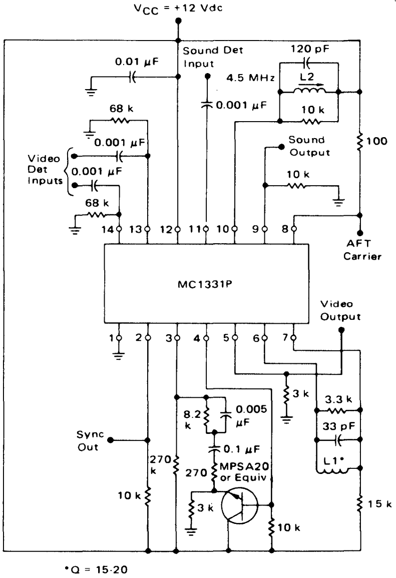


FIGURE 2 – TYPICAL APPLICATION CIRCUIT



*Q = 15-20
L1 = Coilcraft unicoil or T-form, 7½ turns of AWG #22, core-3/8 inch E.
L2 = Coilcraft T-form, 36 2/3 turns of AWG #30, core-½ inch #33 material.

See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	16	Vdc
Supply Current	30	mAdc
Input Voltage	2.0	V(RMS)
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 750 6.7	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, Q = 20, f_C = 45 MHz, T_A = +25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage Range	12	10	12	16	Vdc
Supply Current	12	–	25	–	mA
Zero Signal dc Output Voltage	5	6.4	7.0	7.6	Vdc
Maximum dc Current	5	–	5.0	–	mA
Maximum Signal dc Output Voltage	5	–	0	–	Vdc
Input Signal Voltage for 3.0 V(p-p) Video Output (90% modulation from HP608E)	13,14	–	36	–	mV(RMS)
Maximum Output Voltage Swing	5	–	6.0	–	V(p-p)
Carrier Rejection at Output	5	–	20	–	dB
3.0 dB Bandwidth of Video Output	5	–	6.5	–	MHz
Input Resistance	13,14	–	3.0	–	kΩ
Input Capacitance		–	3.0	–	pF
Internal Resistance (across tuned circuit)	6,7	–	5.0	–	kΩ
Internal Capacitance (across tuned circuit)	6,7	–	3.0	–	pF
Output Resistance	5	–	100	–	Ω
AFT Buffer Output Voltage at Carrier Frequency (measured with 10 times probe)	8	–	100	–	mV(p-p)
AFT Buffer dc Voltage Level	8	–	12	–	Vdc
Sound Detector Gain (1.0 mV(RMS), 41.25 MHz input to pin 11)	9	–	16	–	dB
Sound Detector Output Resistance	9	–	100	–	Ω
Positive Video Output Swing Voltage	4	–	8.0	–	V(p-p)
Sync Output Amplitude Voltage	2	–	11	–	V(p-p)

MC1339P

STEREO PREAMPLIFIER

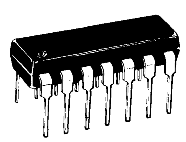
MONOLITHIC DUAL STEREO PREAMPLIFIER

. . . designed for low noise preamplification of stereo audio signals.

- Low Audio Noise
- High Channel Separation
- Single Power Supply
- High Input Impedance
- Built-In Power Supply Filter
- Emitter Follower Output

DUAL LOW-NOISE STEREO PREAMPLIFIER

MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT

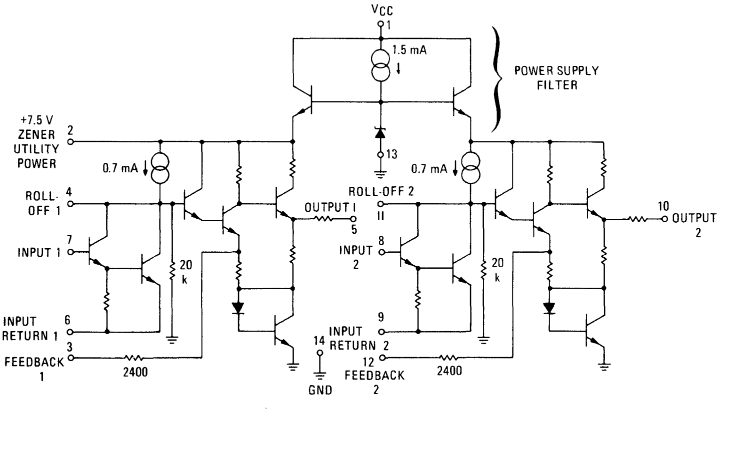


PLASTIC PACKAGE
CASE 646

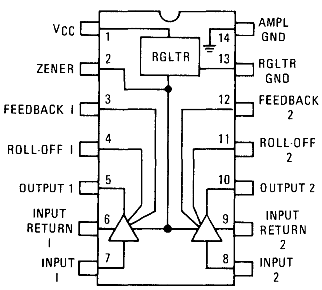
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	+16	Vdc
Power Dissipation (Package Limitation) (Derate above T_A = +25°C)	625 5.0	mW mW/°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

CIRCUIT SCHEMATIC



CONNECTION DIAGRAM



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (Each Preamplifier) (V_{CC} = +12 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Power Supply Current	–	17.5	22	mA
Voltage Gain	63	66	71	dB
Gain Balance	–	0.3	2.0	dB
Channel Separation (f = 1.0 kHz) See Figure 1, S1 in position 1.	45	70	–	dB
Input Resistance	100	250	–	kilohms
Signal Output Voltage No load 3.0-kilohm load	 – –	 1.5 1.0	 – –	V(RMS)
Output Resistance	–	100	–	ohms
Power Supply Rejection (f = 1.0 kHz) See Figure 2	–	33	–	dB
Total Harmonic Distortion without Feedback (0.5 V(RMS) into a 3.0-kilohm load, 1.0 kHz)	–	1.2	–	%
Input Bias dc Current	–	0.8	–	μA
Gain to Feedback Terminals (pins 3 and 12)	–	45	–	dB
Impedance at Feedback Terminals	–	2400	–	ohms
Equivalent Input Noise Voltage (100 Hz to 10 kHz) See Figure 1, S1 in position 2.	–	0.7	3.0	μV(RMS)

TEST CIRCUITS

FIGURE 1 – CHANNEL SEPARATION AND AUDIO NOISE

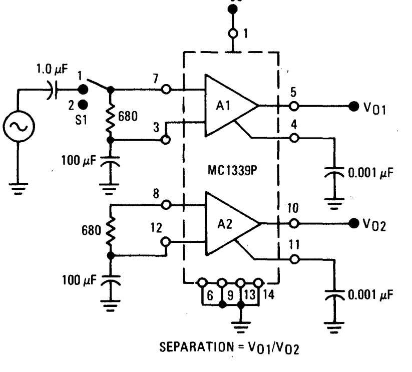
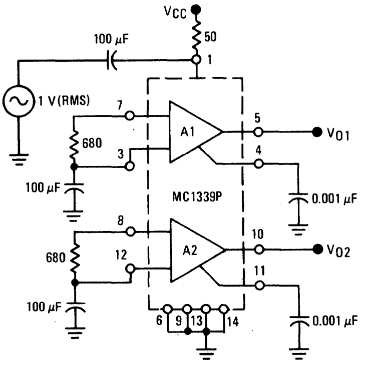


FIGURE 2 – POWER SUPPLY REJECTION



8

APPLICATIONS INFORMATION

The circuit diagrams shown in this section are examples of applications for the MC1339P. Included are circuits for a broadband preamplifier with tape playback and record amplifiers, and a phono preamplifier.

Broadband Amplifiers

The MC1339P is useful as a broadband amplifier in applications requiring a low-signal level low-noise amplifier. The circuit in Figure 3 fills these requirements with a voltage gain of 40 dB and an input impedance of 10 kilohms.

FIGURE 3 – BROADBAND AMPLIFIER

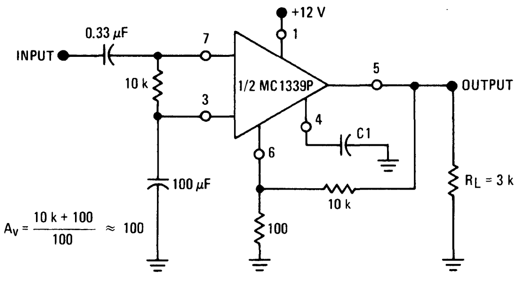
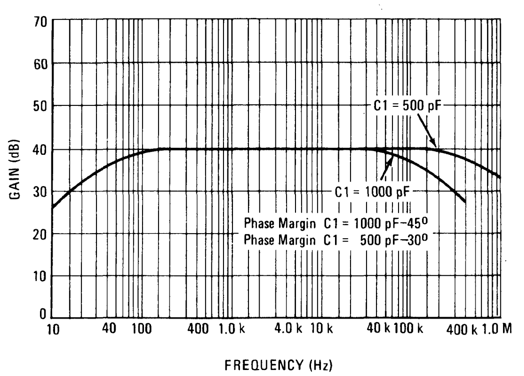


Figure 4 shows the response of the broadband amplifier with two different values of compensation capacitors, C1. Other capacitor values can be used; however, as the phase margin is reduced a greater possibility of oscillation exists.

FIGURE 4 – BROADBAND AMPLIFIER RESPONSE

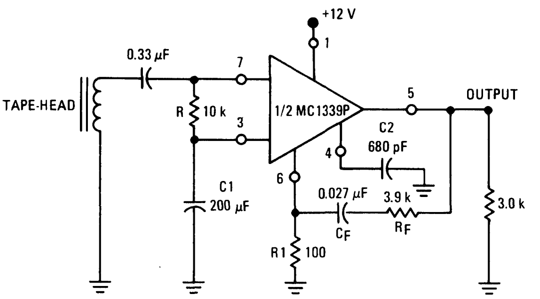


Tape Playback Preamplifier

A low-noise, high-gain preamplifier to properly process the low-level output of the magnetic tape-heads is shown in Figure 5 illustrating a tape-head preamplifier using the MC1339P.

To faithfully reproduce recorded music from magnetic tape, special frequency compensation is required to provide the NAB standard tape playback equalization characteristics, see the response curves shown in Figure 6. The circuit shown in Figure 5 is designed to provide an output of 100 millivolts with an input signal of 2.2 millivolts at a frequency of 1.0 kHz. (Reference gain is 33 dB).

FIGURE 5 – TAPE PLAYBACK PREAMPLIFIER



The lower -3.0 dB corner frequency (f1) is determined by the value for capacitor C1 in accordance with equation 1.

$$C1 = \frac{A_3}{2\pi\, z3 f1} \qquad (1)$$

where z3 is the impedance at pin 3 (2.4 kilohms) and A3 is the amplifier gain at pin 3 (178).

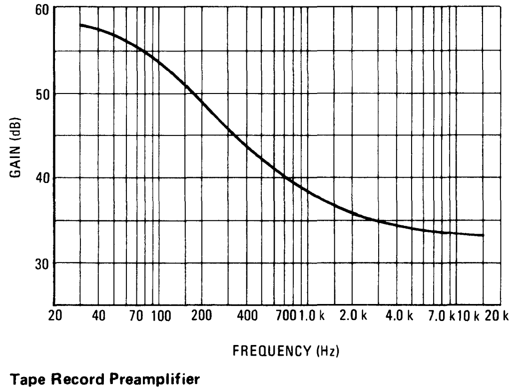
The minimum high-frequency gain (5 dB below reference gain of 33 dB) of the amplifier is determined by the ratio of $\frac{R1 + R_F}{R1}$ while the value of capacitor C_F provides the bass boost corner frequency in accordance with equation 2.

$$C_F = \frac{1}{2\pi\, R_F f2} \qquad (2)$$

Based on measurements made on the amplifier (See Figure 5), the value of C2 is chosen for a phase margin greater than thirty degrees.

The nearest 10% tolerance component values were used in the circuit of Figure 5.

FIGURE 6 – FREQUENCY RESPONSE FOR TAPE PLAYBACK PREAMPLIFIER (TAPE SPEED 1 7/8 OR 3 3/4 IN/S)



Tape Record Preamplifier

The frequency response of a tape recording preamplifier must be the mirror image of the NAB playback equalization characteristic, so that the composite record and playback response is flat. Figure 7 shows the record characteristic superimposed on the NAB playback response and Figure 8 illustrates the output characteristic of

8

APPLICATIONS INFORMATION (continued)

a typical laminated core tape head. Figure 9 shows the necessary amplifier response characteristic to make a composite signal of Figures 8 and 9 that will meet the proper NAB recording characteristic of Figure 7.

FIGURE 7 – NAB TAPE EQUALIZATION CHARACTERISTIC CURVES

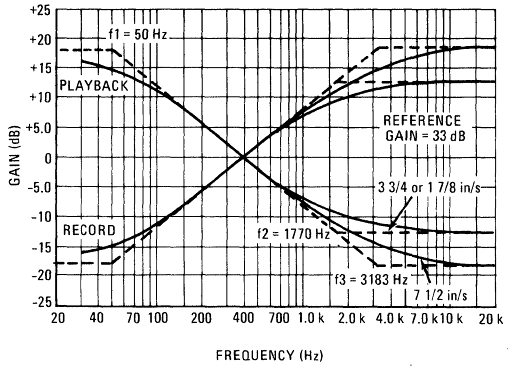


FIGURE 8 – TYPICAL TAPE HEAD OUTPUT CHARACTERISTICS (constant flux)

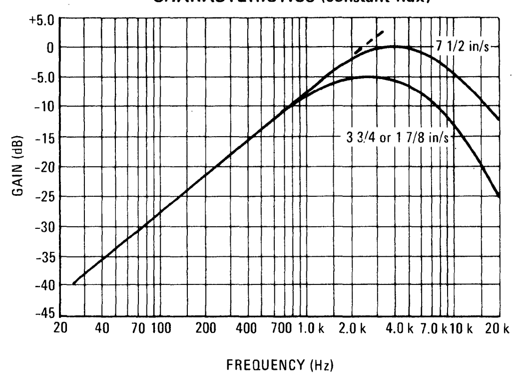


FIGURE 9 – TAPE RECORD AMPLIFIER RESPONSE

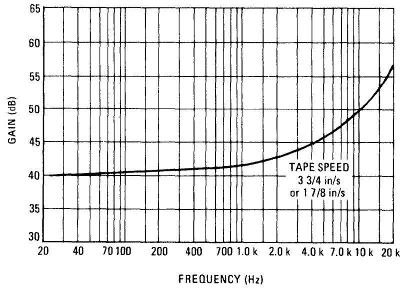
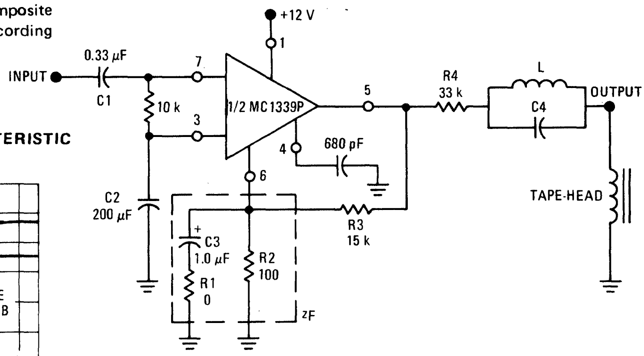


FIGURE 10 – TAPE RECORD PREAMPLIFIER



The circuit shown in Figure 10 will give the preamplifier response as presented in Figure 9.

The gain is established by the equation

$$\text{GAIN} = \frac{R3 + z_f}{z_f} \quad \text{where } z_f = \frac{R2\left(R1 + \frac{1}{2\pi f\, C3}\right)}{R2 + \left(R1 + \frac{1}{2\pi f\, C3}\right)} \qquad (3)$$

The high corner frequency, f2, is determined by equation 4.

$$C3 = \frac{1}{2\pi\, f2\, R2} \qquad (4)$$

At high frequencies the feedback impedance z_f is R1 in parallel with R2 and at low frequencies is R2. Again, capacitor C1 is chosen by equation 1 to give the desired low frequency breakpoint, f1. As an example, consider a recording head requiring 30 µA is used with a microphone with a 10-mV output. The 30-µA current source is simulated by a 1.0 V(RMS) output driving a 33-kilohm resistor, R4, at the reference frequency of 1.0 kHz. The gain requirement is therefore 100 or 40 dB. The low-frequency gain is calculated by letting R2 = 100 ohms and calculating the value of R3 for frequencies below f2.

$$A_V = \frac{R2 + R3}{R2} = 125 \qquad R3 = 124\,(R2) \approx 12\ \text{k}\Omega. \qquad (5)$$

A 15-kilohm resistor is used to achieve the gain necessary since the open-loop gain of the amplifier is not infinite.

The typical response for a quarter-track (3¾ in/s) tape-head is 3.0 dB down at 1770 Hz. Therefore, the high-corner frequency (f2) of the record amplifier should be at the same frequency. Using equation 4 the value of C3 is calculated to be 1.0 µF. Resistor R1 is not needed to roll-off the high-frequency gain at frequencies above 20 kHz since the limited open-loop gain of the MC1339P accomplishes the same thing. The parallel LC circuit at the amplifier output is used to trap the bias oscillator signal and is tuned to that frequency.

Phonographic Preamplifier

Crystal and ceramic phono-cartridges seldom require a preamplifier due to high-output signal levels (100 mV to 1.0 V). However, magnetic cartridges have output levels of from 2.0 to 12 mV and require a preamplifier such as the MC1339P. Special equalization of the preamplifier is necessary to make the response match the RIAA recording characteristic which is used universally. The amplifier shown in Figure 11 does provide the proper response

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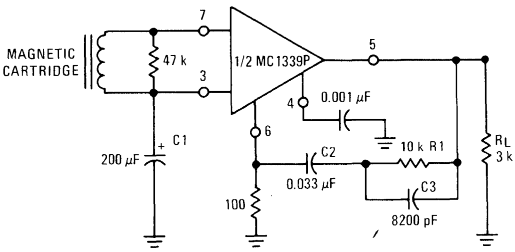
APPLICATIONS INFORMATION (continued)

FIGURE 11 – PHONOGRAPH PREAMPLIFIER



$$f2 = \frac{1}{2\pi\ R1\ C2} \qquad (7)$$

and f3 is calculated from $f3 = \frac{1}{2\pi\ R1\ C3}$

Printed Circuit Board Layout

Most of the circuits in the applications section can be built on this printed circuit board layout. Printed circuit board design is not particularly critical with the MC1339P. However, usual layout practices such as keeping the input and output lines separated and providing maximum ground plane area should be used. The layout shown is for Figure 5 but it can easily be modified without any problem for the other application circuits given.

FIGURE 12 – FREQUENCY RESPONSE OF PHONO-PREAMPLIFIER (compensated for RIAA Equalization)

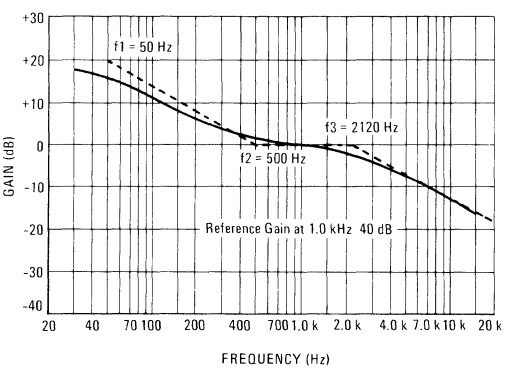
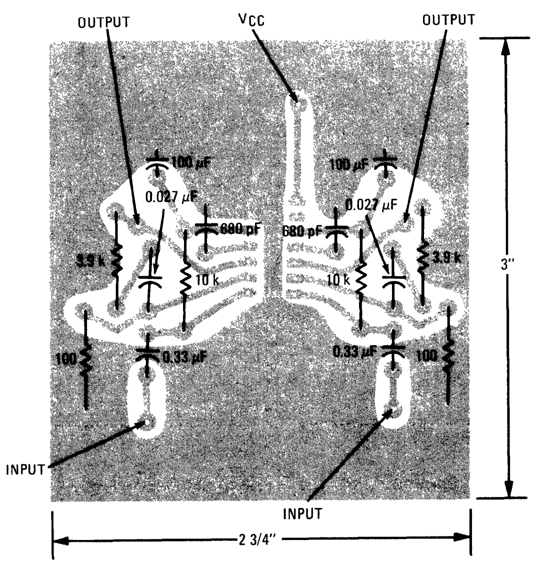


FIGURE 13 – PRINTED CIRCUIT BOARD (copper side shown)



for RIAA equalization. Figure 12 illustrates the RIAA response of the amplifier in Figure 11. The dashed line shows the ideal response with the corner frequencies indicated. The lower corner frequency (f1) is determined by the input capacitance C1 and the equation

$$f1 = \frac{A_f}{2\pi\ C1\ z3} \qquad (6)$$

where A_f is the feedback gain of 45 dB and z3 equals the terminal resistance at pin 3. The corner frequency f2 is determined by

MC1344P

TV SIGNAL PROCESSOR

Product Preview

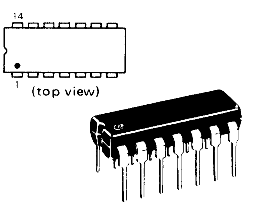
TV SIGNAL PROCESSOR

. . . a monolithic TV circuit with sync separator, advanced noise inversion, AGC comparator, and versatile RF AGC delay amplifier for use in color or monochrome TV receivers.

- Video Internally Delayed for Total Noise Inversion
- Low Impedance, Noise Cancelled Sync Output
- Refined AGC Gate
- Small IF AGC Output Change During RF AGC Interval
- Positive and Negative Going RF AGC Outputs
- Noise Threshold May Be Externally Adjusted
- Time Constants for Sync Separator Externally Chosen
- Stabilized for ±10% Supply Variations

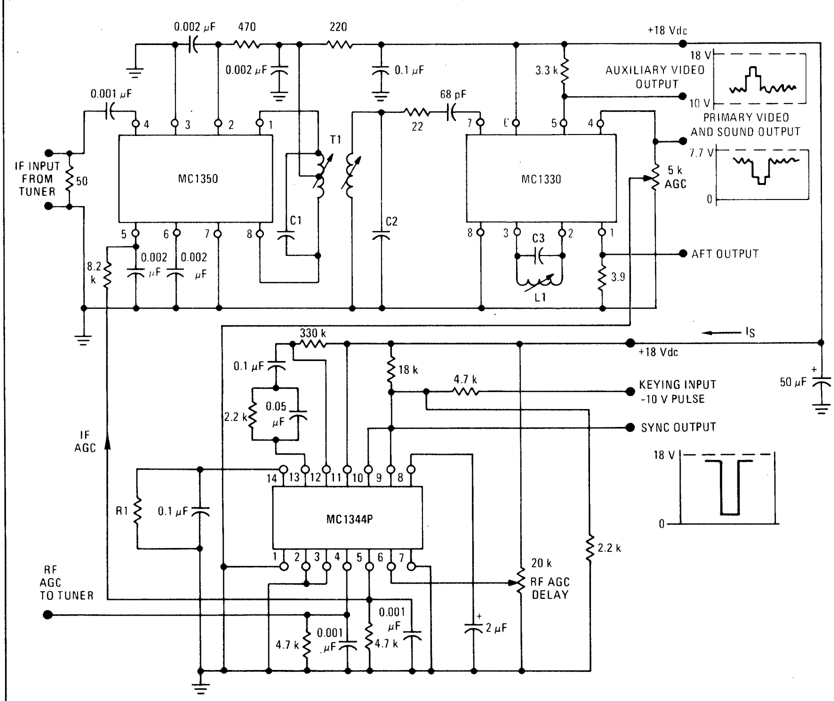
TV SIGNAL PROCESSOR

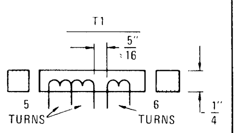
MONOLITHIC SILICON INTEGRATED CIRCUIT



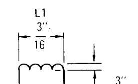
PLASTIC PACKAGE
CASE 646

FIGURE 1 — TYPICAL MC1344 APPLICATION CIRCUIT





All windings #30 AWG tinned nylon acetate wire tuned with high permeability cores. Complete transformer is available from Coilcraft, Type R4786.



L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

	39 MHz	45 MHz	58 MHz
C1	24 pF	15 pF	10 pF
C2	18 pF	12 pF	10 pF
C3	33 pF	33 pF	18 pF
L1	12 Turns	10 Turns	
R1	Select		

See Packaging Information Section for outline dimensions.

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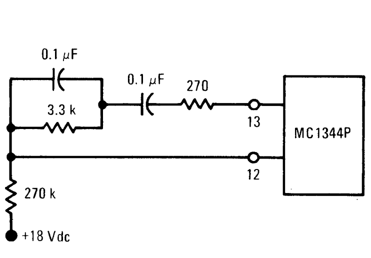
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage (Pin 11)	+22	Vdc
Video Input Voltage (Pin 1)	+10	Vdc
Negative RF AGC Supply Voltage (Pin 3)	-10	Vdc
Gating Voltage (Pin 9)	15	Vp-p
Sync Separator Drive Voltage (Pin 12)	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +70	°C
Storage Temperature Range	-55 to +150	°C

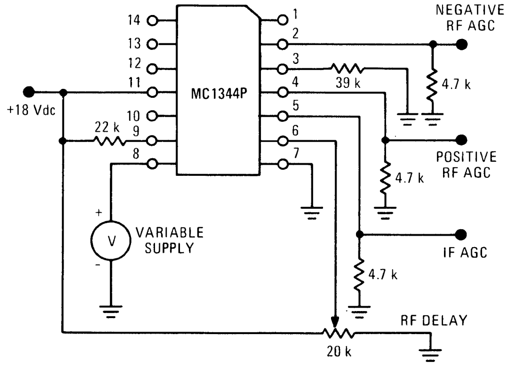
ELECTRICAL CHARACTERISTICS (V_{CC} = +18 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Sync Tip dc Level of Input Signal	3.4	3.9	4.2	Vdc
Temperature Coefficient of Sync Tip (Input)	–	–	1.0	mV/°C
Sync Output Amplitude	–	16	–	Vp-p
Sync Output Impedance	–	–	100	Ohms
Sync Tip to Noise Threshold Separation (Input)	0.45	0.7	0.95	Vdc
IF AGC Voltage Change During RF Interval	–	0.10	0.5	Vdc
Peak AGC Charge Current	–	15	–	mAdc
Peak AGC Discharge Current	–	0.9	–	mAdc
IF AGC Voltage Range	9.0	–	–	Vdc
Positive RF AGC Voltage Range	–	10	–	Vdc
Positive RF AGC Minimum Voltage	0.5	1.5	2.0	Vdc
Negative RF AGC Voltage Range	–	10	–	Vdc
Negative RF AGC Maximum Voltage	9.5	10.2	12	Vdc
Total Supply Current, I_S (Circuit of Figure 1)	–	22	–	mAdc

NORMAL SYNC SEPARATION NETWORK



TEST CIRCUIT FOR AGC AMPLIFIER MEASUREMENTS



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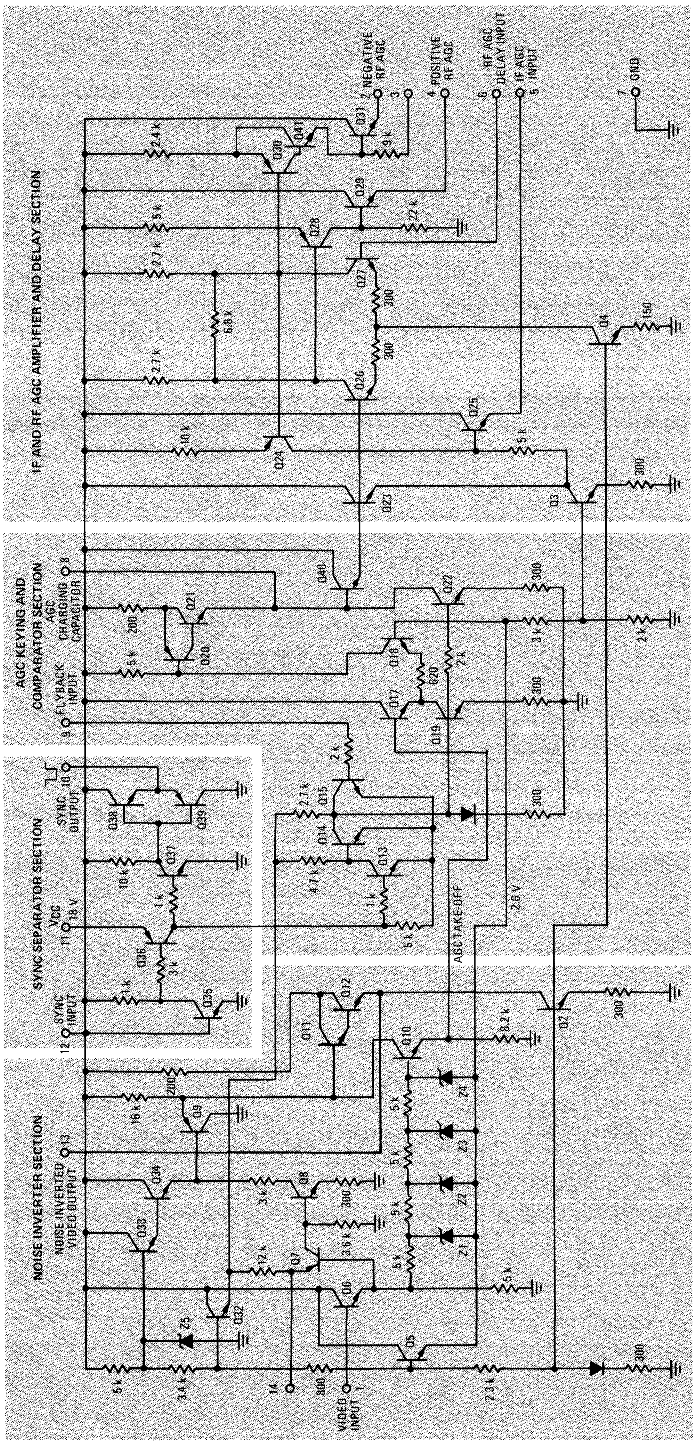
CIRCUIT SCHEMATIC



8

MC1349P

IF AMPLIFIER

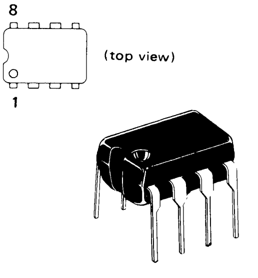
MONOLITHIC IF AMPLIFIER

. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and television applications over the temperature range 0 to +70°C.

- Power Gain – 60 dB typ at 45 MHz (pin 3 open)
  - 56 dB typ at 58 MHz (pin 3 open)
  - 61 dB typ at 45 MHz (pin 3 bypassed)
  - 59 dB typ at 58 MHz (pin 3 bypassed)
- AGC Range – 80 dB typ, dc to 45 MHz
- High Output Impedance
- Low Reverse Transfer Admittance
- 15-Volt Operation, Single-Polarity Power Supply
- Improved Noise Figure versus AGC

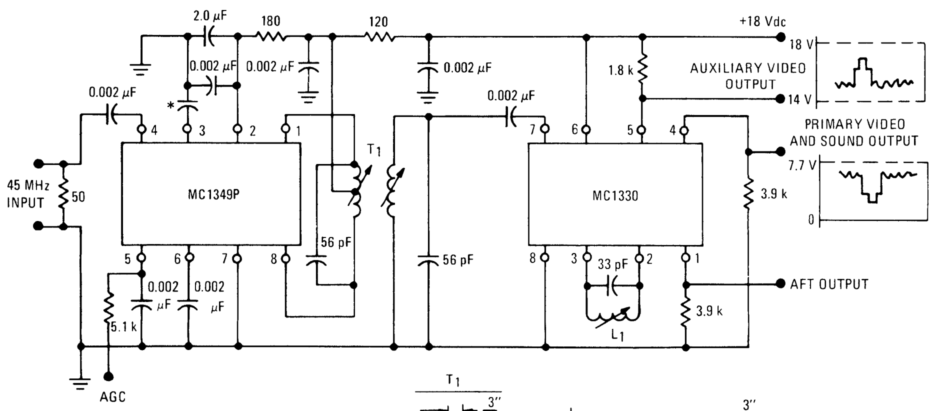
IF AMPLIFIER

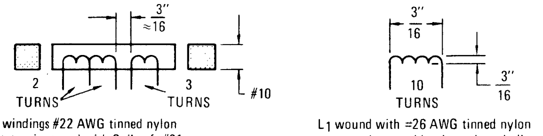
MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

FIGURE 1 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT





All windings #22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10-32, or equivalent.

L1 wound with =26 AWG tinned nylon acetate wire tuned by distorting winding.

*See Note 1 (page 3), and C4, Parts List (page 4) of this specification.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating	Value	Unit
Power Supply Voltage (V_{CC1})	+18	Vdc
Output Supply Voltage (V_{CC2})	+18	Vdc
AGC Supply Voltage	$\leq V_{CC1}$ (pin 2)	Vdc
Differential Input Voltage	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC1} = +12 Vdc [pin 2], V_{CC2} = +15 Vdc [pins 1 and 8], T_A = +25°C unless otherwise noted.)

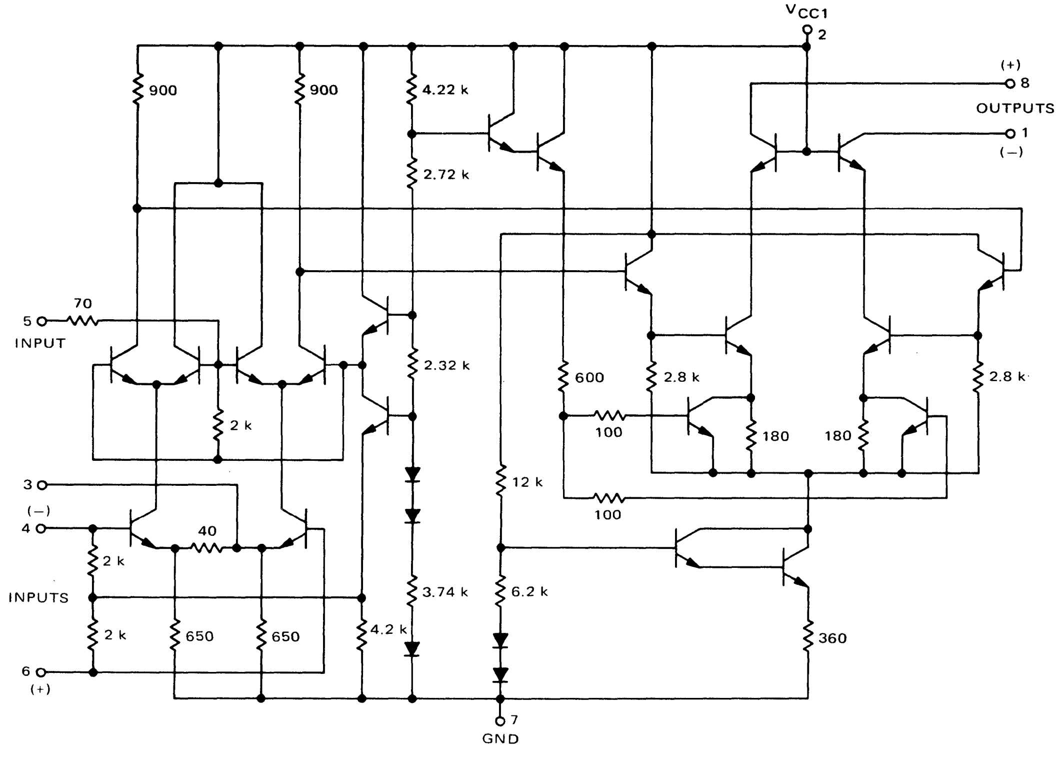
Characteristic	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.5 V) (Figure 3)	70	80	–	dB
Power Gain (Pin 5 grounded via 5.1 kΩ resistor, input pin 4) f = 45 MHz, BW (3 dB) = 4.5 MHz, Tuned Input, pin 3 open Untuned Input, pin 3 bypassed f = 58 MHz, BQ (3 dB) = 4.5 MHz, Tuned Input, pin 3 open Untuned Input, pin 3 bypassed	 52 – – –	 60 61 56 59	 – – – –	dB
Maximum Differential Output Voltage Swing	–	6.0	–	Vp-p
Output Stage Current (pins 1 and 8)	–	9.0	–	mA
Amplifier Current (pin 2)	–	15	20	mAdc
Power Dissipation	–	315	400	mW
Noise Figure f = 45 MHz, Tuned Input, pin 3 open, Gain Reduction = 15 dB	–	8.5	–	dB

DESIGN PARAMETERS (V_{CC1} = +12 Vdc, [pin 2], V_{CC2} = +15 Vdc, [pins 1 and 8], T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Frequency 45 MHz	Frequency 58 MHz	Unit
Single-Ended Input Admittance, input pin 4, AGC min Pin 3 open Pin 3 open Pin 3 bypassed Pin 3 bypassed	 g11 b11 g11 b11	 0.74 1.9 4.1 6.5	 0.95 2.4 5.4 6.9	mmhos
Differential Output Admittance, AGC max	g22 b22	5.5 270	8.3 360	μmhos
Reverse Transfer Admittance (magnitude)		1.5	2.0	μmhos
Forward Transfer Admittance Magnitude, pin 3 open Angle (0 dB AGC), pin 3 open Magnitude, pin 3 bypassed Angle (0 dB AGC), pin 3 bypassed		 520 100 1020 120	 400 130 800 400	 mmhos degrees mmhos degrees
Single-Ended Input Capacitance, AGC min Pin 3 open Pin 3 bypassed		 6.8 2.3	 6.7 20	pF
Differential Output Capacitance (AGC max)		1.0	1.0	pF

8

FIGURE 2 – CIRCUIT SCHEMATIC



GENERAL INFORMATION

The MC1349P is an improved version of the MC1350P. Featuring higher gain, a lower noise figure, and greater AGC range; in addition, an emitter of the input amplifier is available for bypassing. This provides a low input impedance with good gain, useful for untuned input configurations.

Both input and output IF amplifier sections are gain-controlled in the MC1349P, with the input amplifier also serving as an AGC amplifier for the output section. During the initial part of AGC gain reduction, the gain of the input amplifier decreases only a few dB while the output section decreases 15 dB; further AGC acts upon the input section. Although the gain reduction curve was taken with 5.1 kilohms at pin 5, higher series resistance can be used to reduce the voltage and temperature sensitivity of the AGC. Pin 5 currents are shown on the AGC curve, see Figure 10.

In use, it is important to bypass pin 2, both for IF frequencies and for low frequencies, (as shown in the test circuits). This is due to the dual function of the input amplifier. If replacing MC-1350P take precaution not to ground pin 3, (not used in the MC1350P). Due to the significantly higher gain of the MC1349P, extra care in layout should be exercised.

NOTE 1: The references to bypasses at pin 3 do not give specific values (C4, see Figures 1 and 4). In all cases, measurements were taken with a bypass at a standard value as near as possible to series resonance. The values are dependent on test frequency and circuit layout. Fully bypassing pin 3 reduces the input signal handling capability before distortion from over 100 mV(RMS) to approximately 25 mV(RMS). C4 = 0.002 μF at f = 45 MHz is a typical value for printed circuit applications.

TEST CIRCUITS

FIGURE 3 – TUNED INPUT
(PIN 3 OPEN)

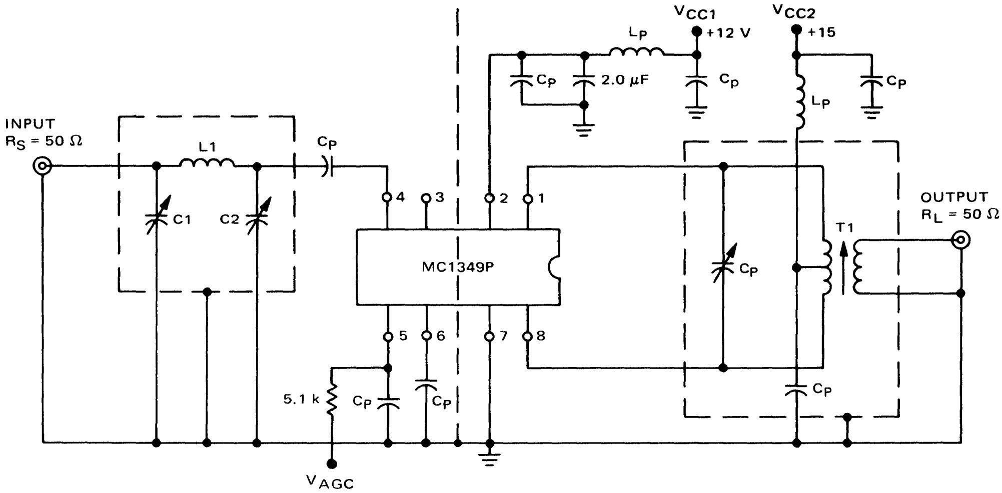
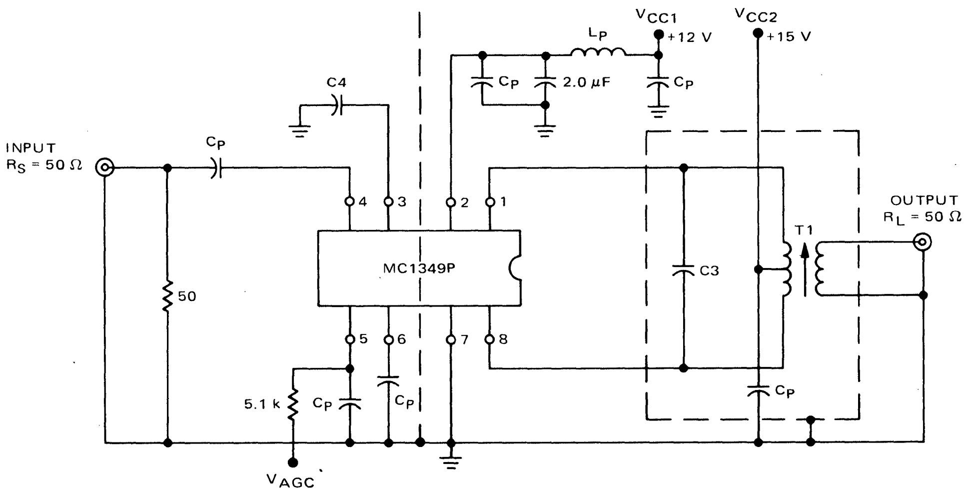


FIGURE 4 – UNTUNED INPUT
(PIN 3 BYPASSED TO GROUND)



PARTS LIST

COMPONENT	45 MHz	58 MHz
C1	8-60 pF	50-100 pF
C2	3-35 pF	3-35 pF
C3	1-7.0 pF	1-7.0 pF
C4	82-470 pF	82-470 pF
C_P	0.0015 μF	0.001 μF
L1	0.84 μH	0.33 μH
L_P	10 μH	10 μH

T1 Primary: 14 turns center-tapped
Secondary: 2½ turns (45 MHz tuned input pin #3 open) 1½ turns (all other fixtures) wound over primary
Wire: #26 AWG tinned nylon acetate wound on 1/4" diameter coil form
Core: Arnold Type TH, 1/2" long or equivalent.

TYPICAL CHARACTERISTICS

FIGURE 5 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 OPEN)

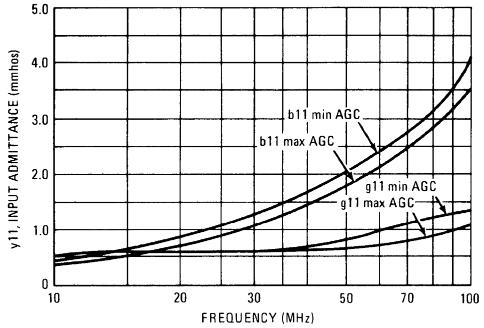


FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 BYPASSED TO GROUND)

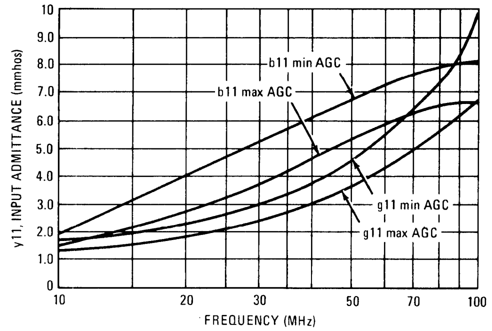


FIGURE 7 – SINGLE-ENDED FORWARD TRANSFER ADMITTANCE

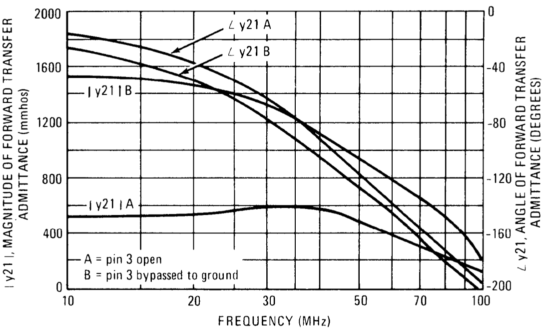


FIGURE 8 – DIFFERENTIAL OUTPUT ADMITTANCE (MAXIMUM AGC)

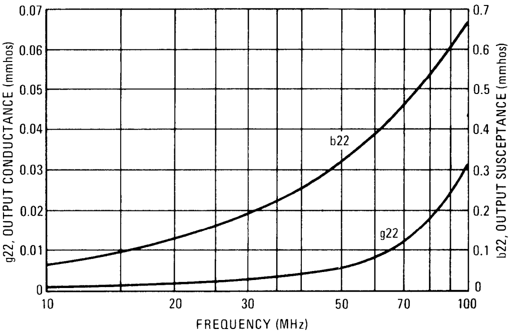


FIGURE 9 – NOISE FIGURE

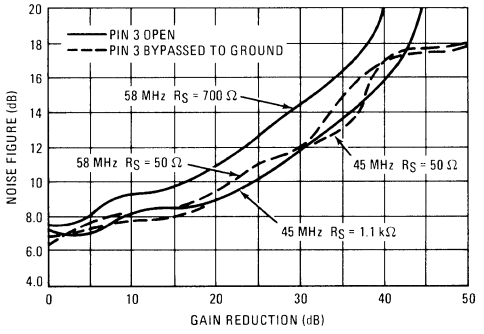
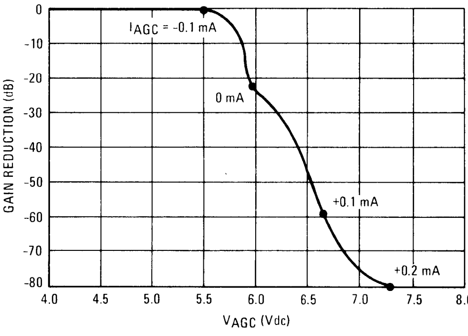


FIGURE 10 – GAIN REDUCTION



8

MC1350P

SOUND IF AMPLIFIER

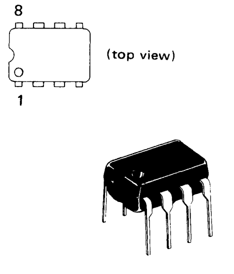
MONOLITHIC IF AMPLIFIER

. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over the temperature range 0 to +75°C. The MC1352 is similar in design but has a keyed-AGC amplifier as an integral part of the same chip.

- Power Gain – 50 dB typ at 45 MHz,
  – 48 dB typ at 58 MHz
- AGC Range – 60 dB min, dc to 45 MHz
- Nearly Constant Input and Output Admittance Over the Entire AGC Range
- y_{21} Constant (-3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance – << 1.0 μmho typ
- 12-Volt Operation, Single-Polarity Power Supply

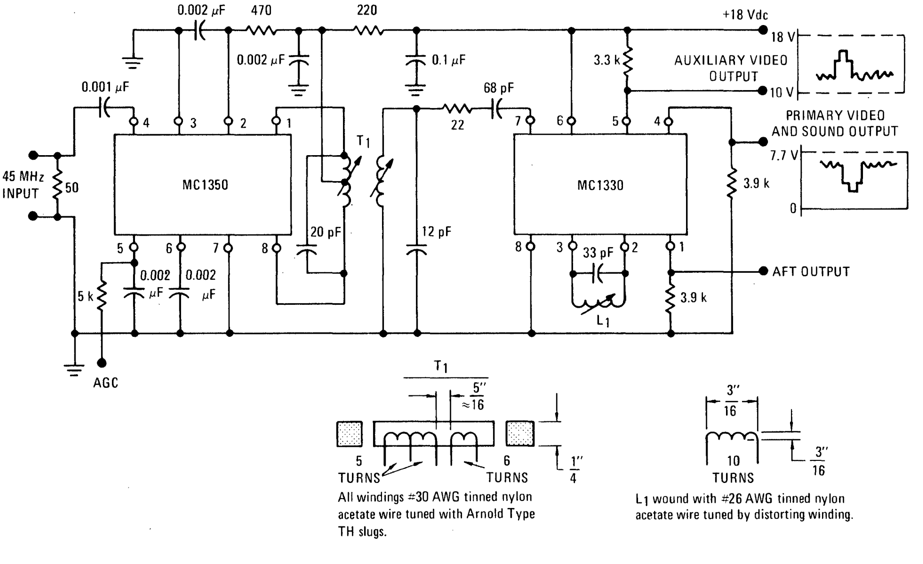
IF AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

FIGURE 1 – TYPICAL MC1350 VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc; T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)		60	68	–	dB
Power Gain (Pin 5 grounded via a 5.1 kΩ resistor) f = 58 MHz, BW = 4.5 MHz } See Figure 5 f = 45 MHz, BW = 4.5 MHz } f = 10.7 MHz, BW = 350 kHz } See Figure 6 f = 455 kHz, BW = 20 kHz }	A_p	 – 46 – –	 48 50 58 62	 – – – –	dB
Maximum Differential Voltage Swing 0 dB AGC -30 dB AGC	V_o	 – –	 20 8.0	 – –	V_{p-p}
Output Stage Current (Pins 1 and 8)	$I_1 + I_8$	–	5.6	–	mA
Total Supply Current (Pins 1, 2 and 8)	I_S	–	14	17	mAdc
Power Dissipation	P_D	–	168	204	mW

DESIGN PARAMETERS, Typical Values (V+ = +12 Vdc, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Frequency				Unit
		455 kHz	10.7 MHz	45 MHz	58 MHz	
Single-Ended Input Admittance	g_{11} b_{11}	0.31 0.022	0.36 0.50	0.39 2.30	0.5 2.75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	– –	– –	60 0	– –	μmhos
Differential Output Admittance	g_{22} b_{22}	4.0 3.0	4.4 110	30 390	60 510	μmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	– –	– –	4.0 90	– –	μmhos
Reverse Transfer Admittance (Magnitude)	$\lvert y_{12} \rvert$	<<1.0	<<1.0	<<1.0	<<1.0	μmho
Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (-30 dB AGC)	 $\lvert y_{21} \rvert$ $\angle y_{21}$ $\angle y_{21}$	 160 -5.0 -3.0	 160 -20 -18	 200 -80 -69	 180 -105 -90	 mmhos degrees degrees
Single-Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_o	1.2	1.2	1.3	1.6	pF

FIGURE 2 – TYPICAL GAIN REDUCTION
(Figures 5 and 6)

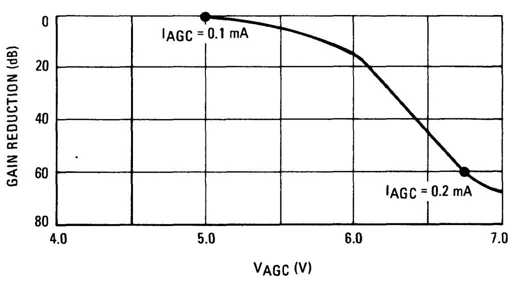
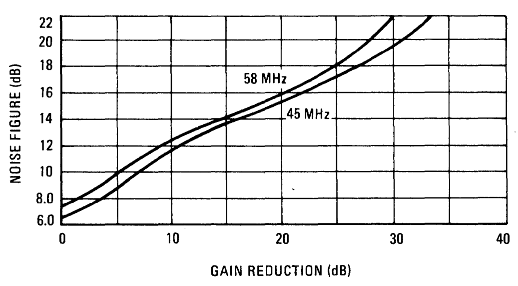


FIGURE 3 – NOISE FIGURE
(Figure 5)



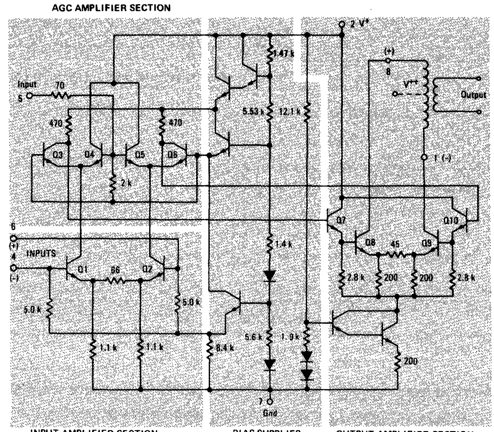
GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

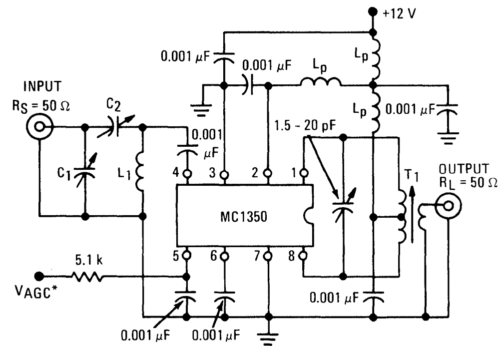
FIGURE 4 – CIRCUIT SCHEMATIC

AGC AMPLIFIER SECTION



INPUT AMPLIFIER SECTION — BIAS SUPPLIES — OUTPUT AMPLIFIER SECTION

FIGURE 5 – POWER GAIN, AGC and NOISE FIGURE TEST CIRCUIT (45 MHz and 58 MHz)



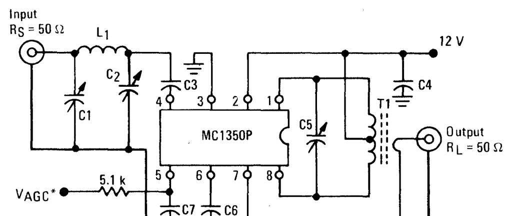
*Connect to ground for maximum power gain test.
All power-supply chokes (L_p), are self-resonate at input frequency. $L_p \geq 20\ k\Omega$

See Figure 10 for frequency response curve.

L_1 @ 45 MHz = 7 1/4 Turns on a 1/4" coil form.
@ 58 MHz = 6 Turns on a 1/4" coil form
T_1 Primary Winding = 18 Turns on a 1/4" coil form, center-tapped
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Arnold TH Material 1/2" Long

	45 MHz		58 MHz	
L_1	0.4 μH	Q ≥ 100	0.3 μH	Q ≥ 100
T_1	1.3 -3.4 μH	Q ≥ 100 @ 2 μH	1.2 -3.8 μH	Q ≥ 100 @ 2 μH
C_1	50 - 160 pF		8 - 60 pF	
C_2	8 - 60 pF		3 - 35 pF	

FIGURE 6 – POWER GAIN and AGC TEST CIRCUIT (455 kHz and 10.7 MHz)



*Grounded for maximum power gain.

Note 1. Primary: 120 μH (center-tapped)
Q_u = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13

Note 2. Primary: 6.0 μH
Primary winding = 24 turns #36 AWG (close-wound on 1/4" dia. form)
Core = Arnold Type TH or equiv.
Secondary winding = 1-1/2 turns #36 AWG, 1/4" dia. (wound over center-tap)

	Frequency	
Component	**455 kHz**	**10.7 MHz**
C1	–	80–450 pF
C2	–	5.0–80 pF
C3	0.05 μF	0.001 μF
C4	0.05 μF	0.05 μF
C5	0.001 μF	36 pF
C6	0.05 μF	0.05 μF
C7	0.05 μF	0.05 μF
L1	–	4.6 μH
T1	Note 1	Note 2

TYPICAL CHARACTERISTICS

($V^+ = 12$ V, $T_A = +25°C$)

FIGURE 7 – SINGLE-ENDED INPUT ADMITTANCE

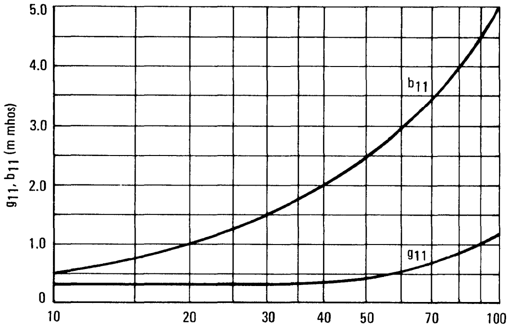


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

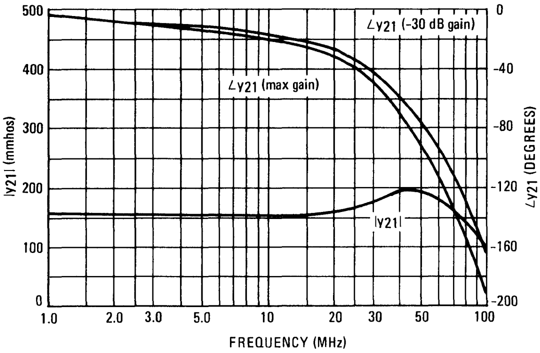


FIGURE 9 – DIFFERENTIAL OUTPUT ADMITTANCE

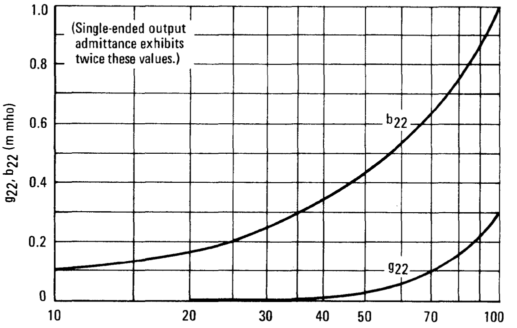
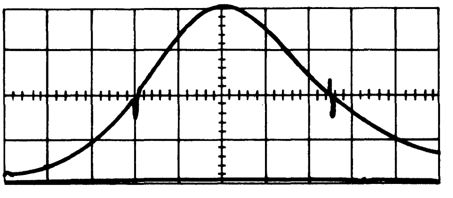
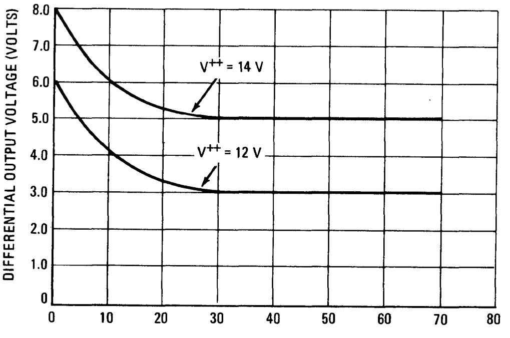


FIGURE 10 – TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)



Scale: 1 MHz/cm

FIGURE 11 – DIFFERENTIAL OUTPUT VOLTAGE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control", by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

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MC1351

SOUND IF AMPLIFIER

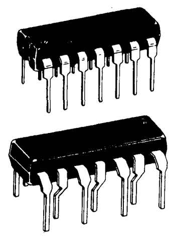
WIDE-BAND FM-AMPLIFIER; LIMITER, DETECTOR, AND AUDIO AMPLIFIER INTEGRATED CIRCUIT

. . . designed for IF limiting, detection, audio preamplifier and driver for the sound portion of a TV receiver.

- Excellent Limiting with 80 μV(rms) Input Signal typ
- Large Output-Voltage Swing – to 3.5 V(rms) typ
- High IF Voltage Gain – 65 dB typ
- Zener Power-Supply Regulation Built-In
- Short-Circuit Protection
- A Coincidence Discriminator that Requires Only One RLC Phase Shift Network
- Preamplifier to Drive a Single External-Transistor Class-A Audio-Output Stage

TV SOUND CIRCUIT

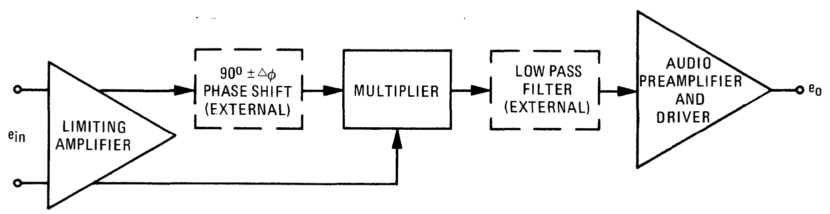
MONOLITHIC SILICON EPITAXIAL PASSIVATED



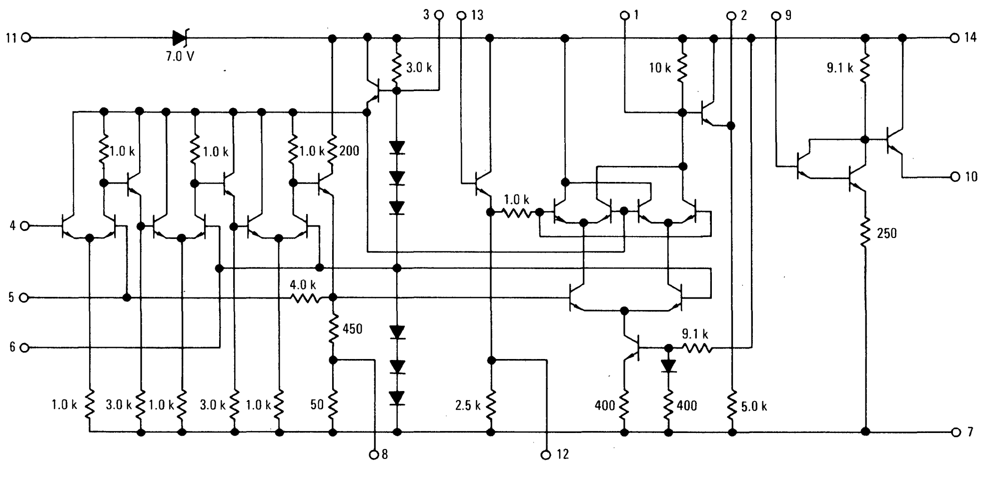
P SUFFIX
PLASTIC PACKAGE
CASE 646

PQ SUFFIX
PLASTIC PACKAGE
CASE 647

BLOCK DIAGRAM



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25° unless otherwise noted)

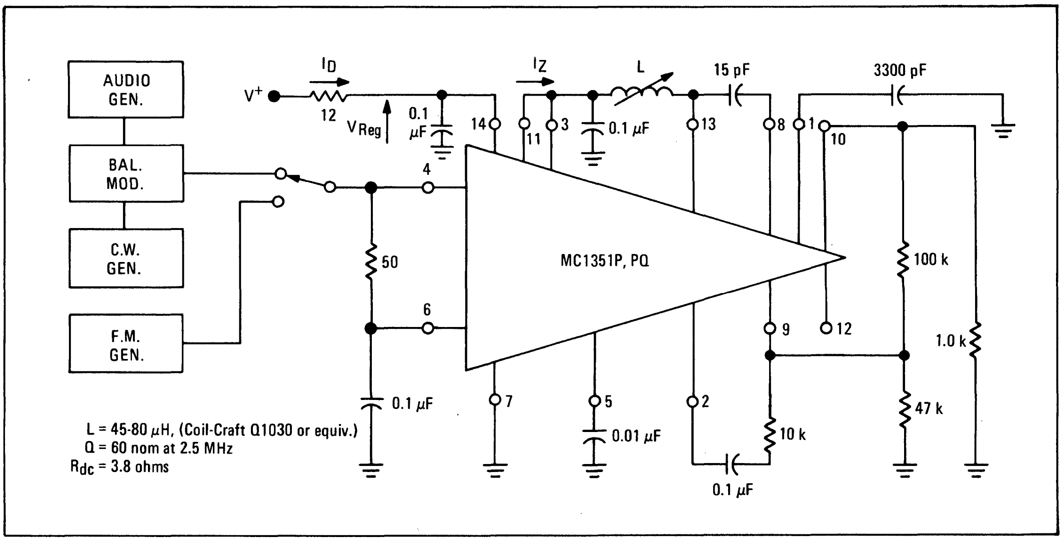
Rating	Symbol	Value	Unit
Power Supply Voltage	V+	+16	Vdc
Input Voltage	V_{in}	0.7	$V_{(rms)}$
Power Dissipation (Package Limitation) Plastic Packages Derate above +25°C	 P_D $1/\theta_{JA}$	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = 12 Vdc, T_A = +25°C, f = 4.5 MHz, Deviation = ±25 kHz unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage (−3.0 dB Limiting)	V_L	–	80	160	µV(rms)
AM Rejection (V_{in} = 20 mV(rms), AM = 30%) (See Note 1) $AMR = 20 \log \frac{V_{OFM}}{V_{OAM}} \begin{cases} f = 4.5\text{ MHz, Deviation} = \pm 25\text{ kHz, } Q_L = 24 \\ f = 5.5\text{ MHz, Deviation} = \pm 50\text{ kHz, } Q_L = 30 \end{cases}$	AMR	 – –	 45 45	 – –	dB
Total Harmonic Distortion (Q_L = 24) (See Note 1) (7.5 kHz Deviation)	THD	–	1.0	–	%
Maximum Undistorted Audio Output Voltage (Pin 10) (See Note 1) (Audio Gain Adjusted Externally) (Q = 24)	$V_{o(max)}$	–	3.5	–	V(rms)
Recovered Audio (Pin 2) (See Note 1) (f = 4.5 MHz, Deviation = ±25 kHz, Q_L = 24) (f = 5.5 MHz, Deviation = ±50 kHz, Q_L = 30)	V_A	 0.35 –	 0.50 0.80	 – –	V(rms)
Audio Preamplifier Open Loop Gain	A_{VP}	–	25	–	dB
IF Voltage Gain	A_{VIF}	–	65	–	dB
Parallel Input Resistance	R_{in}	–	9.0	–	kΩ
Parallel Input Capacitance	C_{in}	–	6.0	–	pF
Nominal Zener Voltage (I_Z = 5.0 mAdc)	V_{Reg}	–	11.6	–	Vdc
Power Supply Current (I_Z = 5.0 mAdc)	I_D	–	31	–	mAdc
Power Dissipation (I_Z = 5.0 mAdc)	P_D	–	300	375	mW

Note 1: Q_L is loaded circuit Q.

FIGURE 1 – TEST CIRCUIT (V^+ = +12 Vdc, T_A = +25°C)



TYPICAL CHARACTERISTICS

FIGURE 2 – DETECTED AUDIO OUTPUT versus INPUT LEVEL @ f = 4.5 MHz, ±25 kHz DEVIATION

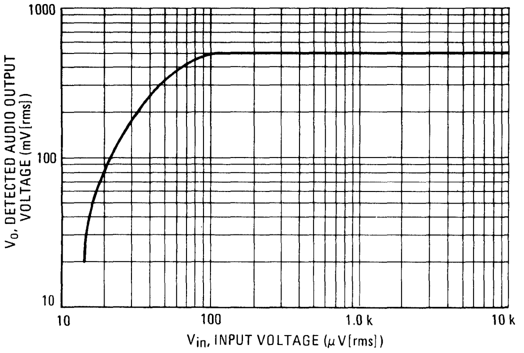


FIGURE 3 – DETECTED AUDIO OUTPUT versus INPUT LEVEL @ f = 5.5 MHz, ±50 kHz DEVIATION

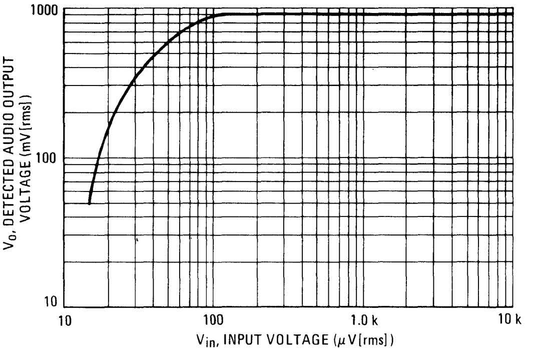


FIGURE 4 – DETECTOR "S" CURVE @ f = 4.5 MHz, BW = 200 kHz, Q = 24

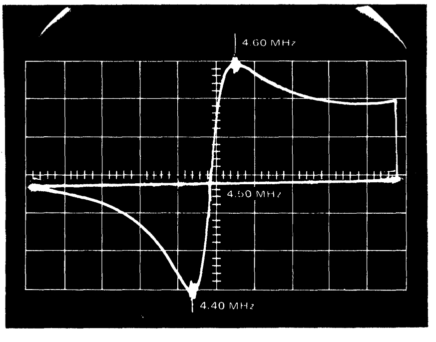


FIGURE 5 – DETECTOR "S" CURVE @ f = 5.5 MHz, BW = 220 kHz, Q = 30

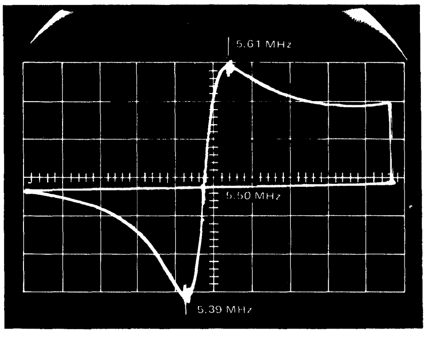


FIGURE 6 – IF VOLTAGE GAIN versus FREQUENCY

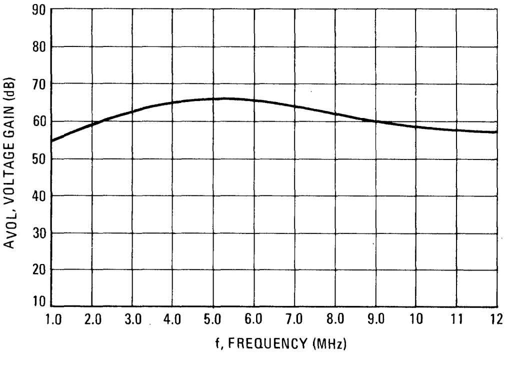


FIGURE 7 – AM REJECTION

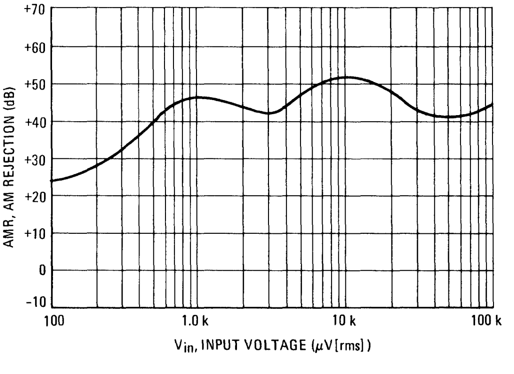


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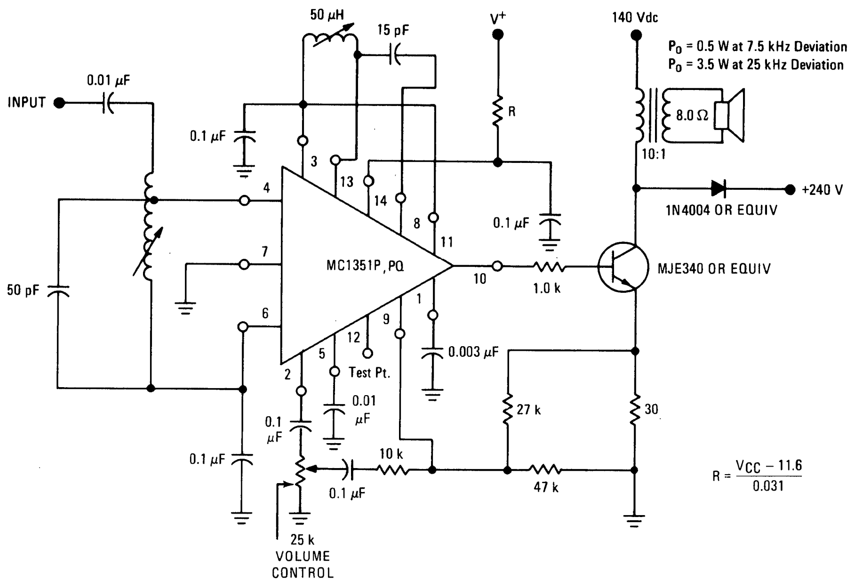
FIGURE 8 — 4.5 MHz TYPICAL APPLICATION



TV VIDEO IF AMPLIFIER

MC1352
MC1353

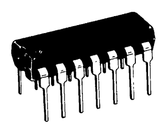
TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

. . . a monolithic IF amplifier with a complete gated wide-range AGC system for use as the 1st and 2nd IF stages and AGC keyer and amplifier in color or monochrome TV receivers.

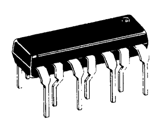
- Power Gain at 45 MHz, 52 dB typ
- Extremely Low Reverse-Transfer Admittance – << 1.0 μmho typ
- Nearly Constant Input and Output Admittance Over AGC Range
- Single-Polarity Power-Supply Operation
- High-Gain Gated AGC System for Either Positive or Negative-Going Video Signals
- Control Signal Available for Delayed AGC of Tuner
- Two Complementary Devices – MC1352 and MC1353 – Offer Opposite Tuner AGC Polarity

TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

MONOLITHIC SILICON INTEGRATED CIRCUIT

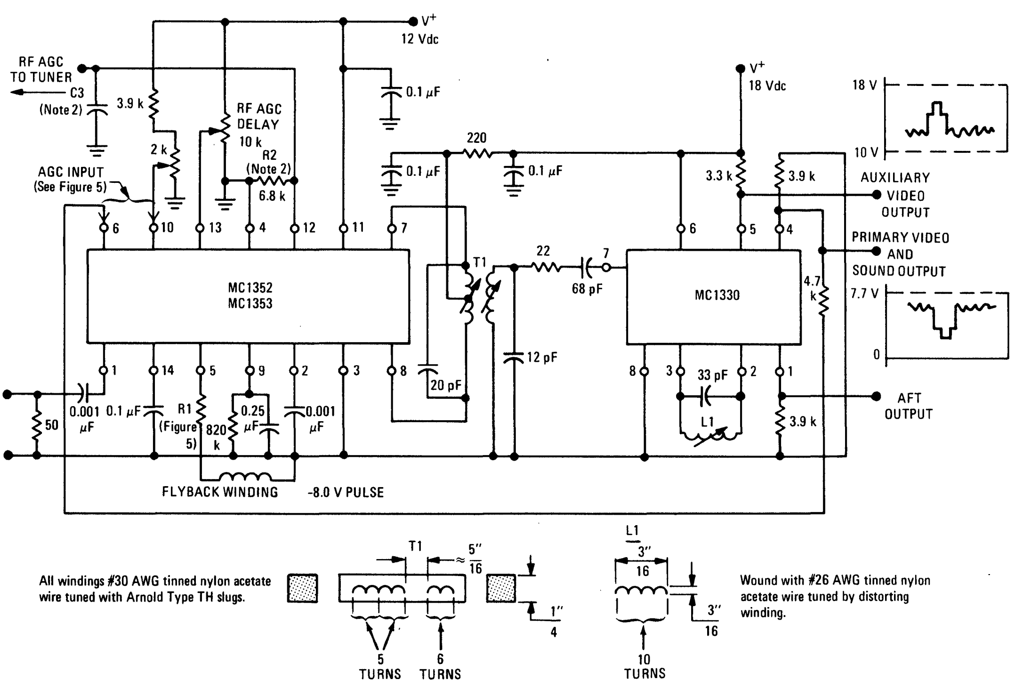


P SUFFIX
PLASTIC PACKAGE
CASE 646



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL VIDEO IF AMPLIFIER APPLICATION



See Packaging Information Section for outline dimensions.

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MAXIMUM RATINGS (Voltages referenced to pin 4, ground; T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply (Pin 11)	+18	Vdc
Output Supply (Pins 7 and 8)	+18	Vdc
Signal Input Voltage (Pin 1 or 2, other pin ac grounded)	10	V_{p-p}
AGC Input Voltage (Pin 6 or 10, other pin ac grounded)	+6.0	Vdc
Gating Voltage, Pin 5	+10, -20	Vdc
Power Dissipation Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V+ = +12 Vdc, Voltages referenced to pin 4, ground; T_A = +25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
AGC Range	–	75	–	dB
Power Gain f = 35 MHz or 45 MHz f = 58 MHz	 – –	 52 50	 – –	dB
Maximum Differential Output Voltage Swing 0 dB AGC -30 dB AGC	 – –	 16.8 8.4	 – –	V_{p-p}
Voltage Range for RF-AGC at Pin 12 Maximum Minimum	 – –	 7.0 0.2	 – –	Vdc
IF Gain Change Over RF-AGC Range	–	10	–	dB
Output Stage Current ($I_7 + I_8$)	–	5.7	–	mAdc
Total Supply Current ($I_7 + I_8 + I_{11}$)	–	27	31	mAdc
Total Power Dissipation	–	325	370	mW

DESIGN PARAMETERS, TYPICAL VALUES (V+ = 12 Vdc, T_A = +25°C unless otherwise noted)

Parameters	Symbol	f = 35 MHz	f = 45 MHz	f = 58 MHz	Unit
Single-Ended Input Admittance	g_{11} b_{11}	0.55 2.25	0.70 2.80	1.1 3.75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	50 0	60 0	– –	μmhos
Differential Output Admittance	g_{22} b_{22}	20 430	40 570	75 780	μmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	3.0 80	4.0 100	– –	μmhos
Reverse Transfer Admittance	$\lvert y_{12}\rvert$	<<1.0	<<1.0	<<1.0	μmho
Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (-30 dB AGC)	 $\lvert y_{12}\rvert$ $\angle y_{21}$ $\angle y_{21}$	 260 -73 -52	 240 -100 -72	 210 -135 -96	 mmhos degrees
Single-Ended Input Capacitance		9.5	10	10.5	pF
Differential Output Capacitance		2.0	2.0	2.5	pF

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FIGURE 2 – CIRCUIT SCHEMATIC

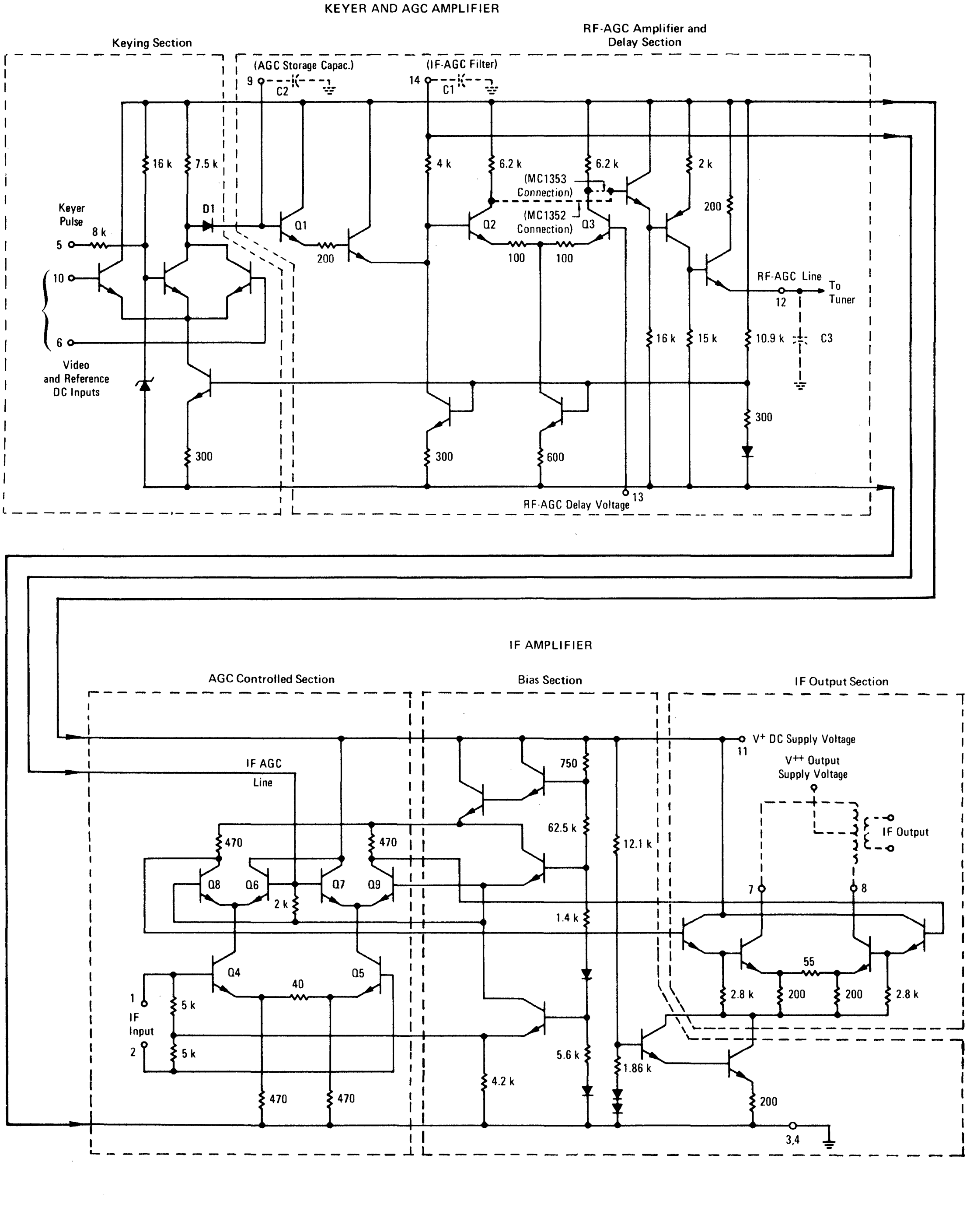
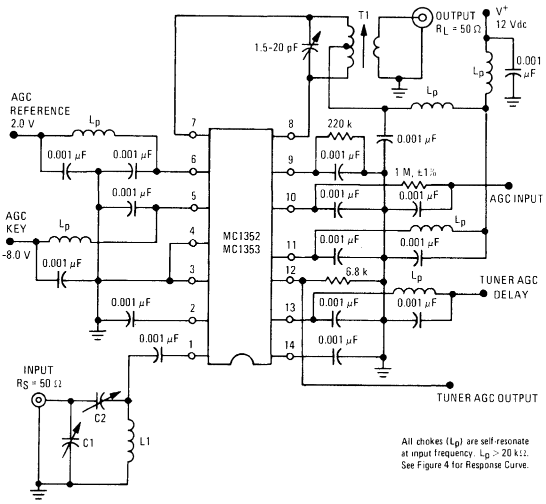


FIGURE 3 – POWER GAIN, AGC AND NOISE TEST CIRCUIT



All chokes (L_p) are self-resonate at input frequency. L_p > 20 kΩ. See Figure 4 for Response Curve.

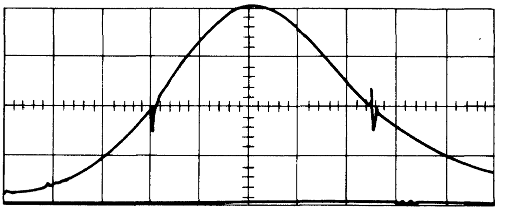
	35 and 45 MHz		58 MHz	
L1	0.4 µH	Q ⩾ 100	0.3 µH	Q ⩾ 100
T1	1.3-3.4 µH	Q ⩾ 100 @ 2 µH	1.2-3.8 µH	Q ⩾ 100 @ 2 µH
C1	48-100 pF		40-80 pF	
C2	8-60 pF		12-45 pF	

L1 and T1 = #26 AWG Tinned Nylon Acetate Wire.

L1 @ 35 or 45 MHz = 7-1/4 Turns on a 1/4″ coil form
@ 58 MHz = 6 Turns on a 1/4″ coil form
T1 Primary Winding = 18 Turns on a 1/4″ coil form
Secondary Winding = 2 Turns Wound Evenly over Primary Winding for 35 or 45 MHz and 1 Turn for 58 MHz
Slug = Arnold TH Material 1/2″ long

V_C, is maintained across the external capacitor, C2, for a particular video level and dc reference setting. The voltage V_C, is the result of the charge delivered through D1 and the charge drained by Q1. The charge delivered occurs during the time of the gating pulse, and its magnitude is determined by the amplitude of the video signal relative to the dc reference level. The voltage V_C is delivered via the IF-AGC amplifier and applied to the variable gain stage of the IF signal amplifier and is also applied to the RF-AGC amplifier, where it is compared to the fixed RF-AGC delay voltage reference by the differential amplifier, Q2 and Q3. The following stages amplify the output signal of either Q2 for MC1352, or Q3 for MC1353 and shift the dc levels causing the RF-AGC voltage to vary (positive-going for MC1352 or negative-going for MC1353).

FIGURE 4 – TEST CIRCUIT RESPONSE CURVE
(45 and 58 MHz)



Scale: 1 MHz/cm

GENERAL OPERATING INFORMATION

Each device, MC1352 and MC1353, consists of an AGC section and an IF signal amplifier (Figure 2) subdivided into different functions as indicated by the illustration.

A gating pulse, a reference level, and a composite video signal are required for proper operation of the AGC section. Either positive or negative-going video may be used; necessary connections and signal levels are shown in Figure 1. The essential difference is that the video is fed into Pin 10 and the AGC reference level is applied to Pin 6 for a video signal with positive-going sync while the input connections are reversed for negative-going sync.

The action of the gating section is such that the proper voltage,

The input amplifiers (Q4 and Q5) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac). Terminals 1 and 2 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q6 and Q7 causing those transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q8 and Q9. The output amplifiers are fed from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant.

NOTES:

1. The 12-V supply must have a low ac impedance to prevent low-frequency instability in the RF-AGC loop. This can be achieved by a 12-V zener diode and a large decoupling capacitor. (5 µF).

2. Choices of C1, C2 and C3 depend somewhat on the set designers' preference concerning AGC stability versus AGC recovery speed. Typical values are C1 = 0.1 µF, C2 = 0.25 µF, C3 = 10 µF.

3. To set a fixed IF-AGC operating point (e.g., for receiver alignment) connect a 22 kΩ resistor from pin 9 to pin 11 to give minimum gain, then bias pin 14 to give the correct operating point using a 200 kΩ variable resistor to ground.

4. Although the unit will normally be operating with a very high power gain, the pin configuration has been carefully chosen so that shielding between input and output terminals will not normally be necessary even when a standard socket is used.

FIGURE 5 – TYPICAL AGC APPLICATION CHART

Video Polarity	Pin 6 Voltage	Pin 10 Voltage	Pin 5 R1 (Ω)
Negative-Going Sync.	5.5 2.0 0	Adj. 1.0–4.0 Vdc Nom 2.0 V	0
Positive-Going Sync.	Adj. 1.0–8.0 Vdc Nom 4.5 V	4.5 0	3.9 k

8

TYPICAL CHARACTERISTICS
(V^+ = +12 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE

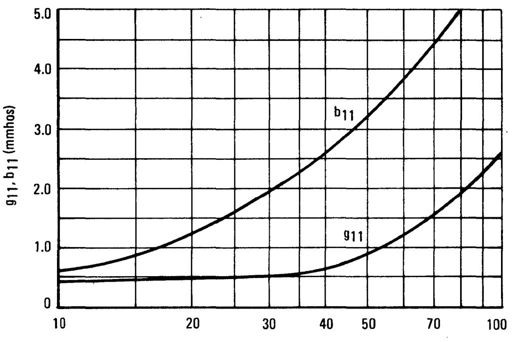


FIGURE 7 – DIFFERENTIAL OUTPUT ADMITTANCE

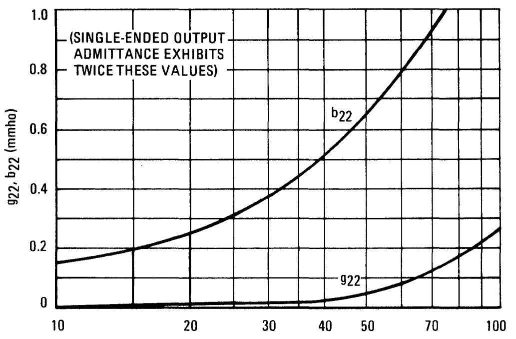


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

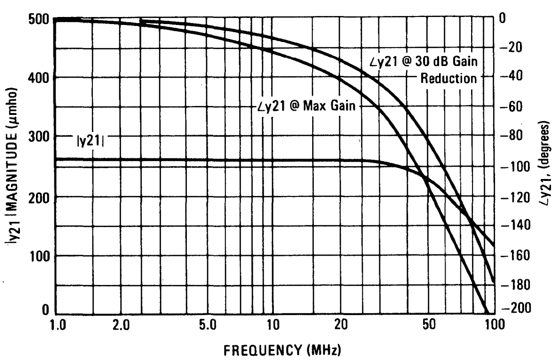


FIGURE 9 – DIFFERENTIAL OUTPUT VOLTAGE

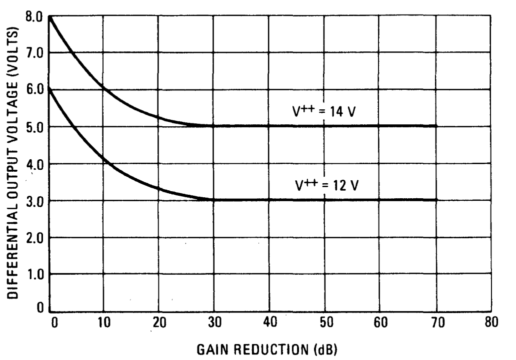


FIGURE 10 – MC1352 AGC CHARACTERISTICS

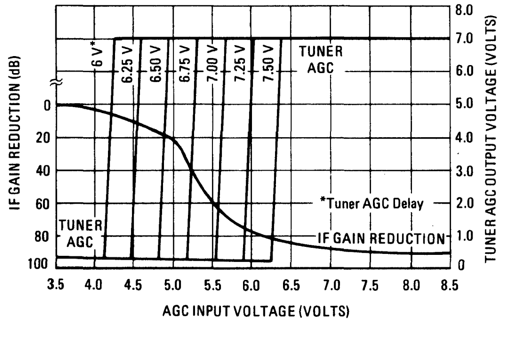
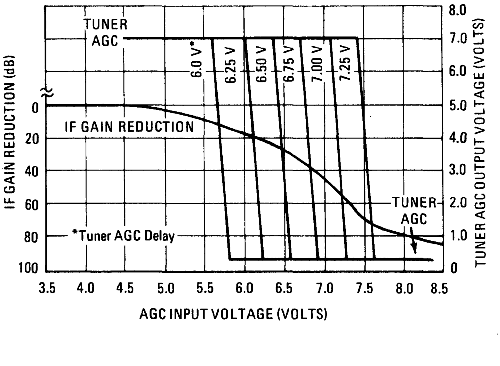


FIGURE 11 – MC1353 AGC CHARACTERISTICS



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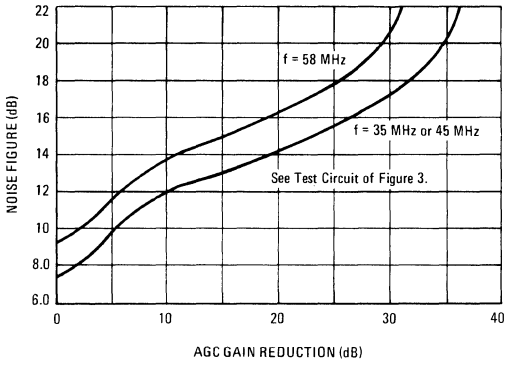
TYPICAL CHARACTERISTICS (continued)

(V^+ = +12 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 12 – TYPICAL NOISE FIGURE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control", by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

8

MC1355

FM IF AMPLIFIER

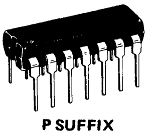
BALANCED MONOLITHIC FOUR-STAGE HIGH-GAIN FM/IF AMPLIFIER

. . . designed for use with Foster-Seeley discriminator or ratio detector in high quality FM systems.

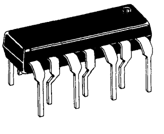
- High AM Rejection (60 dB typ)
- Wide Range of Supply Voltages (8 to 18 Vdc)
- Low Distortion (0.5% typ)

LIMITING FM IF AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT

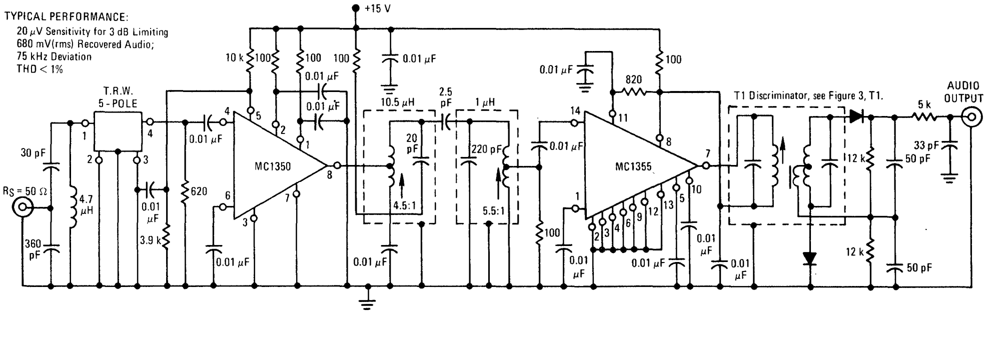


P SUFFIX
PLASTIC PACKAGE
CASE 646



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL FM-IF APPLICATION



When using the device as a non-saturating limiter the load must be chosen to prevent voltage saturation of the output stage. The load impedance can be calculated from: $R_L \leq \frac{2(V^+ - 5.3)}{5.0}$ kilohms

See Packaging Information Section for outline dimensions.

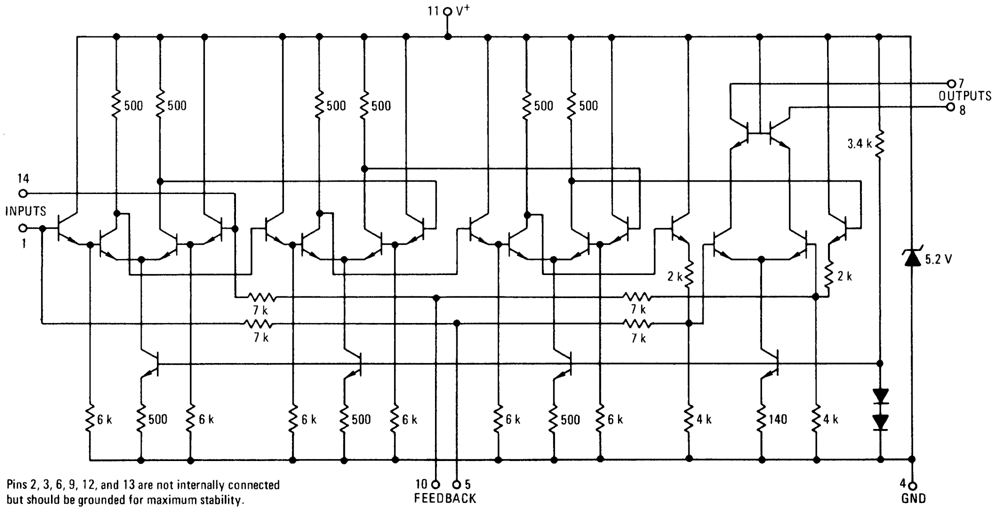
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Output Voltage (pins 7 & 8)	40	Vdc
Supply Current to pin 11	20	mA
Input Signal Voltage (single-ended)	5.0	Vp-p
Input Signal Voltage (differential)	10	Vp-p
Power Dissipation (package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = 15 Vdc, f = 10.7 MHz, T_A = +25°C, R_S = 820 ohms unless otherwise noted)

Characteristic	Min	Typ	Max	Units
Power Supply Voltage Range	8.0	15	18	Vdc
Total Circuit Current	–	16	–	mAdc
Total Output Stage Current	–	4.2	–	mA
Device Dissipation	–	125	–	mW
Internal Zener Voltage	–	5.2	–	Vdc
Input Signal for 3 dB Limiting	–	175	250	μV(rms)
Output Current Swing	3.5	4.2	5.0	mA p-p
AM Rejection (10 mv to 1.0 v (rms) input, FM @ 100%, AM @ 80%, Foster Seeley detector)	–	60	–	dB
Maximum AM Signal before Breakup (FM @ 100%, AM @ 80%)	–	–	1.4	V(rms)
Admittance Parameters Y_{11}	–	120 + j320	–	μmhos
Y_{12}	–	j0.6	–	μmho
Y_{21}	–	8 + j5.9	–	mhos
Y_{22}	–	15 + j230	–	μmhos

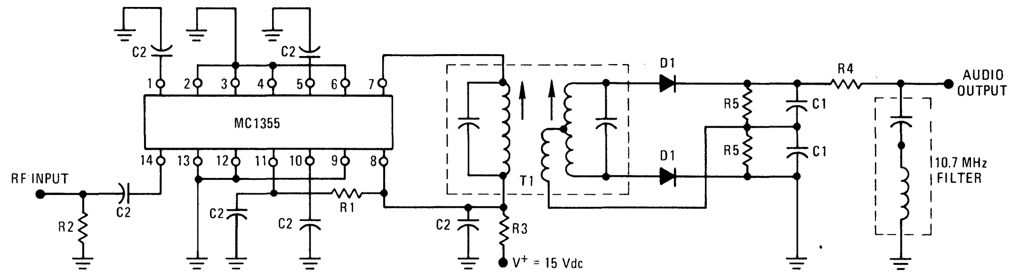
FIGURE 2 – CIRCUIT SCHEMATIC



Pins 2, 3, 6, 9, 12, and 13 are not internally connected but should be grounded for maximum stability.

TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT



R1 820 ohms
R2 50 ohms
R3 100 ohms
R4 5 kilohms
R5 12 kilohms

C1 50 pF
C2 0.01 μF
T1 10.7 MHz Foster-Seeley Discriminator, Primary Impedance = 3.9 k, Peak-to-Peak Separation = 600 kHz

D1 Small Signal Germanium Diode (1N542 or equiv)

Specifications are given for a Foster-Seeley discriminator. Improved AM rejection at low signal levels can be obtained with a ratio detector.

For optimum circuit stability it is important to ground pins 2, 3, 4, 6, 9, 12, and 13.

FIGURE 4 – AM REJECTION TEST BLOCK DIAGRAM

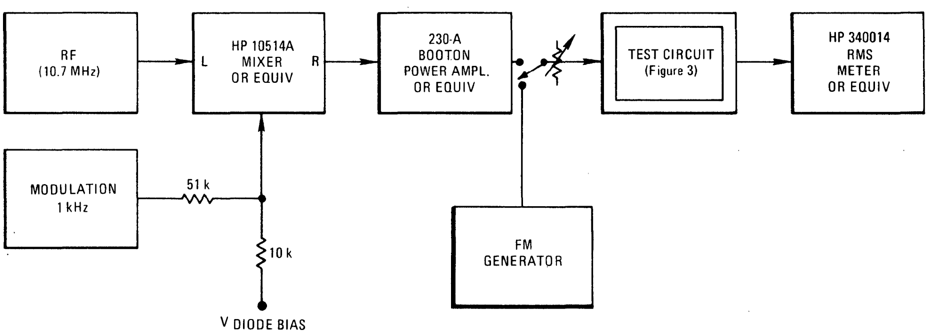


FIGURE 5 – LIMITING

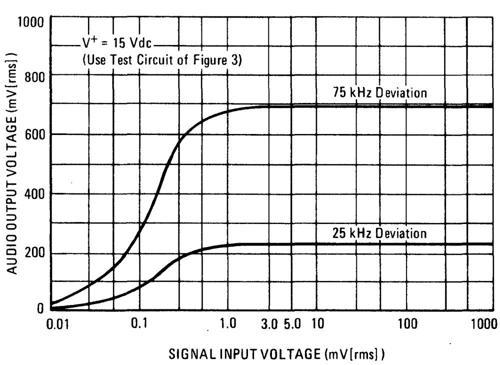
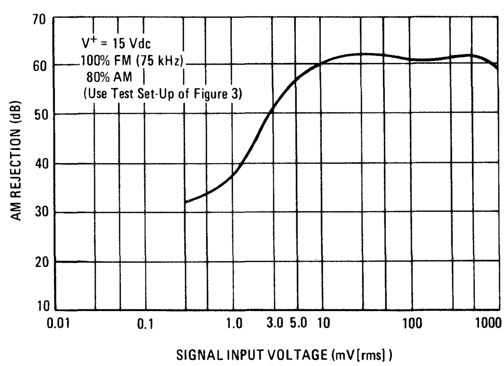


FIGURE 6 – AM REJECTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT DISTORTION

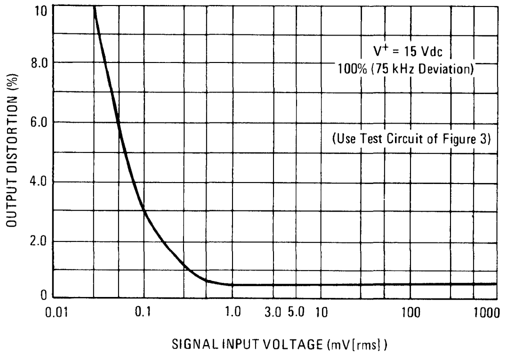


FIGURE 8 – SIGNAL-TO-NOISE RATIO SIGNAL

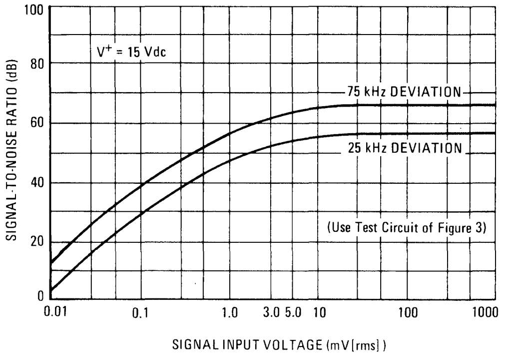
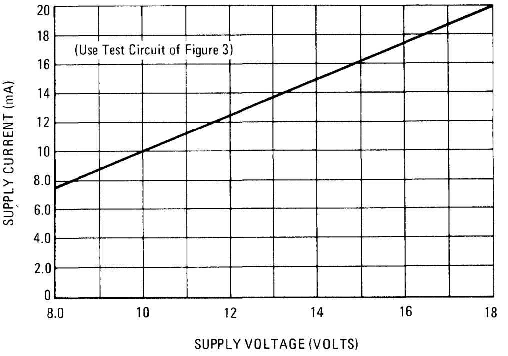


FIGURE 9 – TOTAL SUPPLY CURRENT



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MC1357

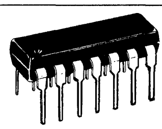
SOUND IF AMPLIFIER

MONOLITHIC TV SOUND IF OR FM IF AMPLIFIER WITH QUADRATURE DETECTOR

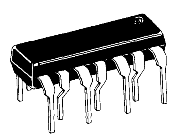
- A Direct Replacement for the ULN2111A
- Greatly Simplified FM Demodulator Alignment
- Excellent Performance at $V^+ = 8.0$ Vdc

IF AMPLIFIER AND QUADRATURE DETECTOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

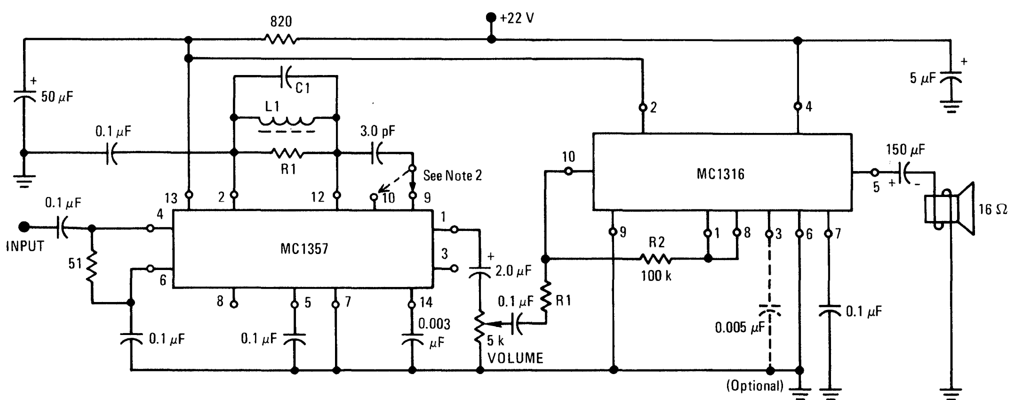


P SUFFIX
PLASTIC PACKAGE
CASE 646



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 — TV TYPICAL APPLICATION CIRCUIT



Typical Performance:
2 Watts Output
2% Distortion
250 μV Sensitivity (3 dB Lim.)

C1 = 120 pF
L1 = 14 μH
R1 = 20 kΩ
Q = 30

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Vdc
Input Voltage (Pin 4)	3.5	V_p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = 12 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current V^+ = 8 V V^+ = 12 V	13	10 –	12 15	19 21	mA
Amplifier Input Reference Voltage	6	–	1.45	–	Vdc
Detector Input Reference Voltage	2	–	3.65	–	Vdc
Amplifier High Level Output Voltage	10	1.25	1.45	1.65	Vdc
Amplifier Low Level Output Voltage	9	–	0.145	0.2	Vdc
Detector Output Voltage V^+ = 8 V V^+ = 12 V	1	– –	3.7 5.4	– –	Vdc
Amplifier Input Resistance	4	–	5.0	–	kΩ
Amplifier Input Capacitance	4	–	11	–	pF
Detector Input Resistance	12	–	70	–	kΩ
Detector Input Capacitance	12	–	2.7	–	pF
Amplifier Output Resistance	10	–	60	–	ohms
Detector Output Resistance	1	–	200	–	ohms
De-Emphasis Resistance	14	–	8.8	–	kΩ

DYNAMIC CHARACTERISTICS (FM Modulation Freq. = 1.0 kHz, Source Resistance = 50 ohms, T_A = +25°C for all tests.)

(V^+ = 12 Vdc, f_o = 4.5 MHz, Δf = ±25 kHz, Peak Separation = 150 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	60	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	36	–	dB
Input Limiting Threshold Voltage	4	–	250	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.72	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	3	–	%

(V^+ = 12 Vdc, f_o = 5.5 MHz, Δf = ±50 kHz, Peak Separation = 260 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	60	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	40	–	dB
Input Limiting Threshold Voltage	4	–	250	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	1.2	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	5	–	%

(V^+ = 8.0 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	53	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	37	–	dB
Input Limiting Threshold Voltage	4	–	600	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.30	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	1.4	–	%

(V^+ = 12 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	53	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	45	–	dB
Input Limiting Threshold Voltage	4	–	600	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.48	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	1.4	–	%

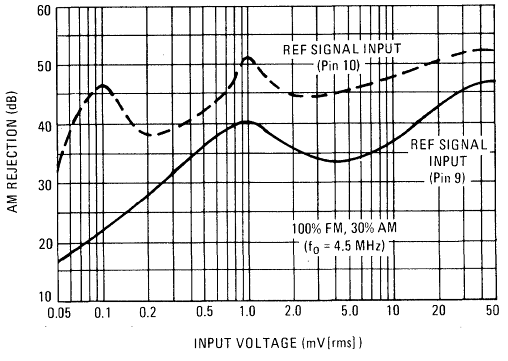
*100% FM, 30% AM Modulation

TYPICAL CHARACTERISTICS

(V+ = 12 V, T_A = +25°C unless otherwise noted)
(Use Test Circuit of Figure 13)

(f_o = 4.5 MHz)

FIGURE 2 – AM REJECTION



(f_o = 5.5 MHz)

FIGURE 3 – AM REJECTION

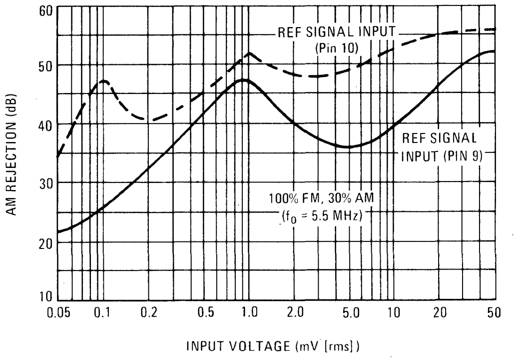


FIGURE 4 – DETECTED AUDIO OUTPUT

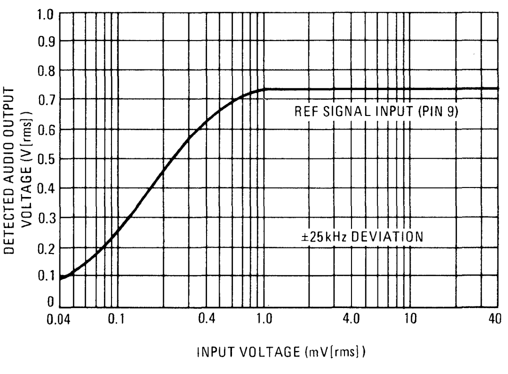


FIGURE 5 – DETECTED AUDIO OUTPUT

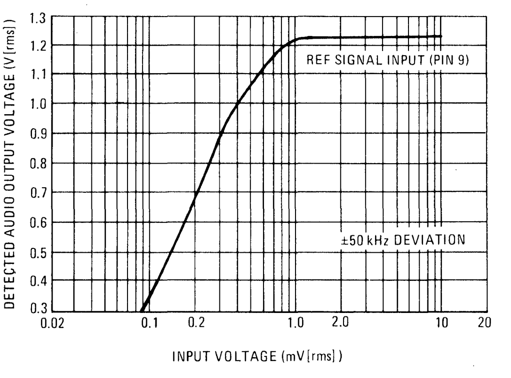


FIGURE 6 – DETECTOR TRANSFER CHARACTERISTIC

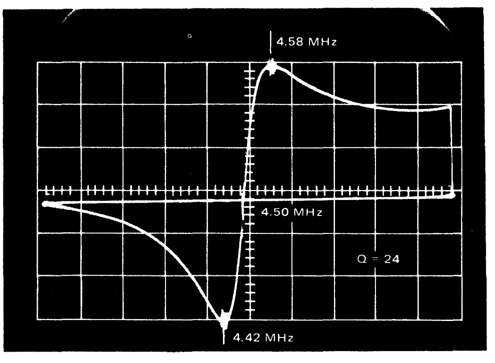
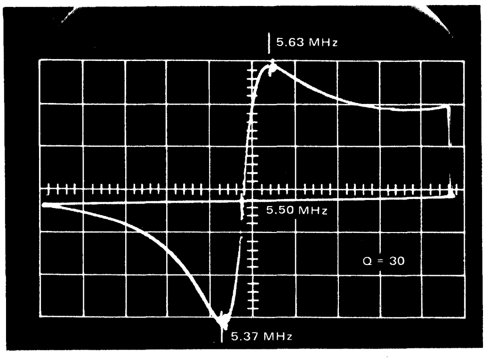


FIGURE 7 – DETECTOR TRANSFER CHARACTERISTIC



TYPICAL CHARACTERISTICS (continued)

(f_o = 10.7 MHz, T_A = +25°C unless otherwise noted.)
(Use Test Circuit of Figure 13)

FIGURE 8 – AM REJECTION

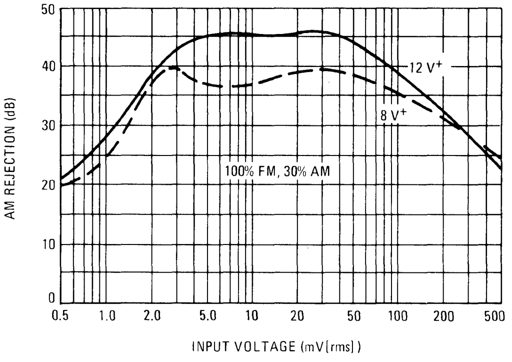


FIGURE 9 – AFC VOLTAGE DRIFT (1.0 mV INPUT CARRIER @ 10.7 MHz)

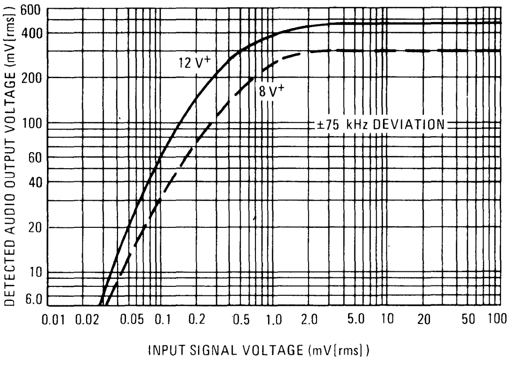


FIGURE 10 – LIMITING

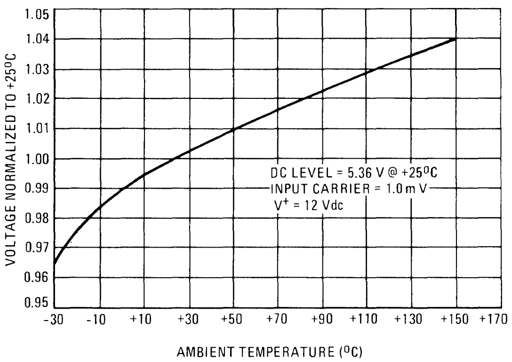


FIGURE 11 – SIGNAL-TO-NOISE RATIO

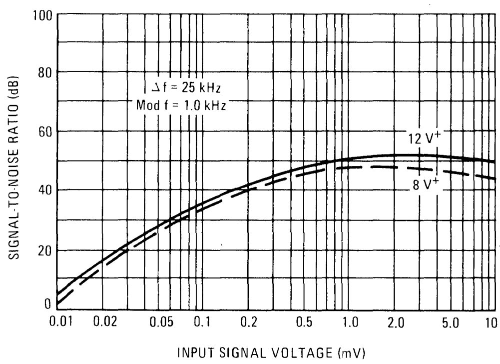


FIGURE 12 – DETECTOR TRANSFER CHARACTERISTIC

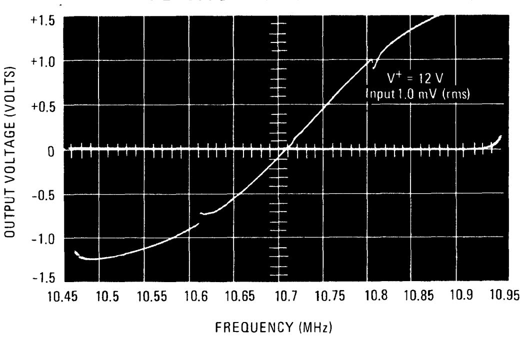
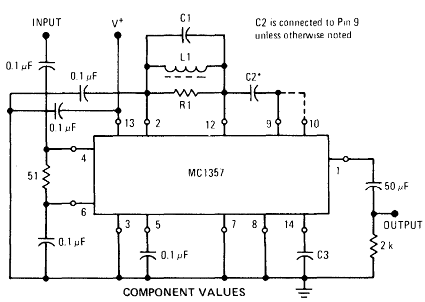


FIGURE 13 – TEST CIRCUIT



COMPONENT VALUES

f	L1	C1	R1	Q(R1, L1)	C2	C3
MHz	μH	pF	kΩ		pF	μF
4.5	14	120	20	30	3.0	0.003
5.5	8.0	100	20	30	3.0	0.003
10.7	2.0	120	3.9	20	4.7	0.01

FIGURE 14 – FM RADIO TYPICAL APPLICATION CIRCUIT

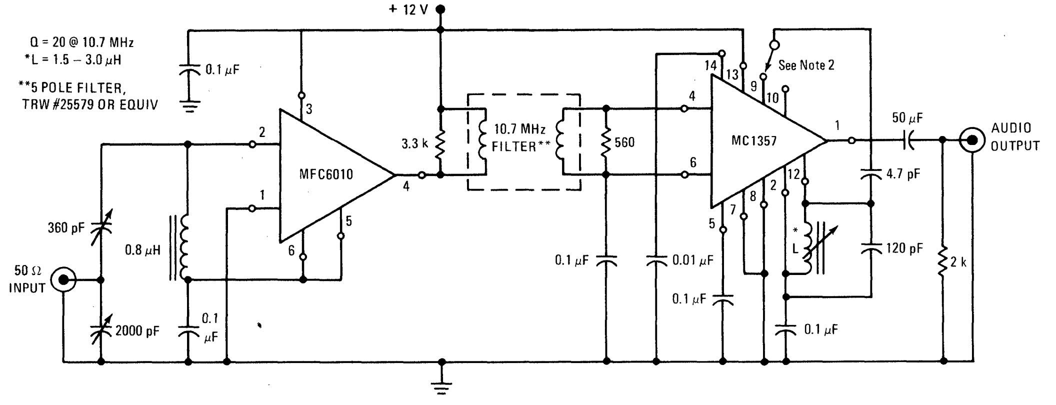
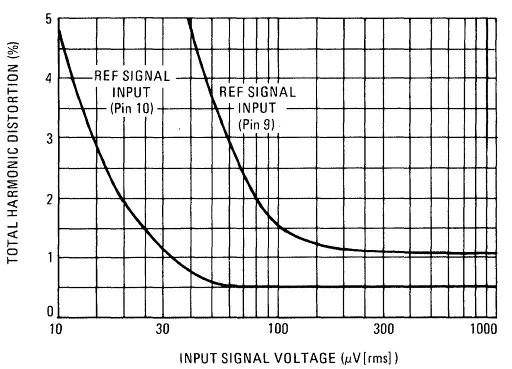


FIGURE 15 – OUTPUT DISTORTION



Note 1:

Information shown in Figures 15, 16, and 17 was obtained using the circuit of Figure 14.

Note 2:

Optional input to the quadrature coil may be from either pin 9 or pin 10 in the applications shown. Pin 9 has commonly been used on this type of part to avoid overload with various tuning techniques. For this reason, pin 9 is used in tests on the preceding pages (except as noted). However, a significant improvement of limiting sensitivity can be obtained using pin 10, see Figure 17, and no overload problems have been incurred with this tuned circuit configuration.

FIGURE 16 – SIGNAL-TO-NOISE RATIO

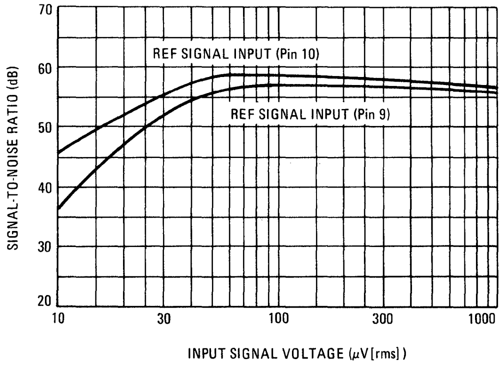


FIGURE 17 – RECOVERED AUDIO OUTPUT

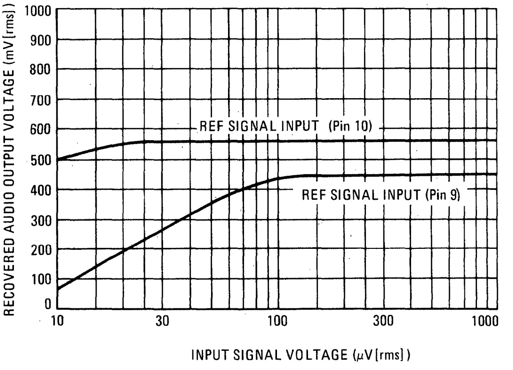


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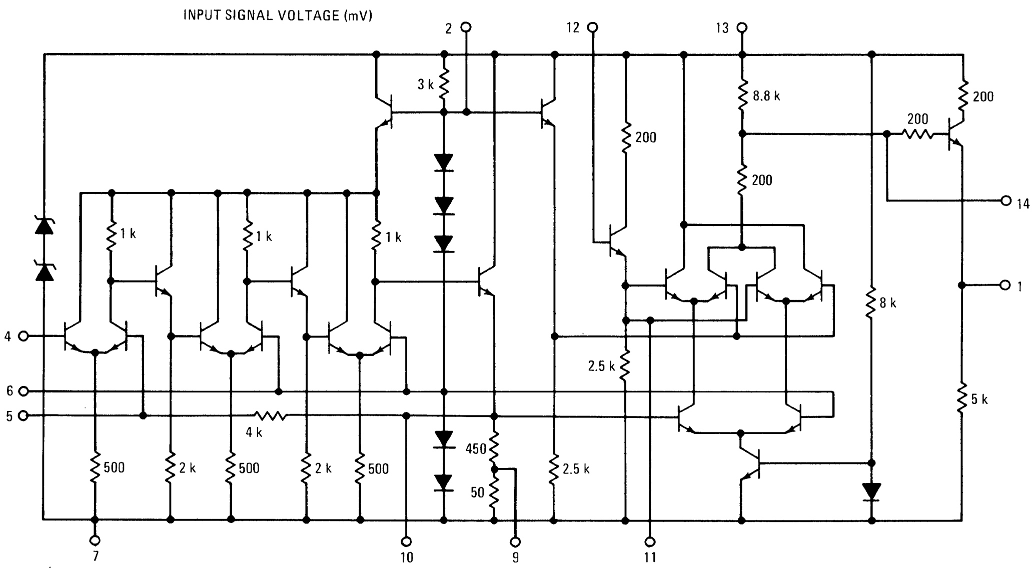
FIGURE 18 – CIRCUIT SCHEMATIC



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MC1358

SOUND IF AMPLIFIER

TV SOUND IF AMPLIFIER

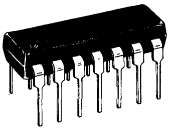
. . . a versatile monolithic device incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

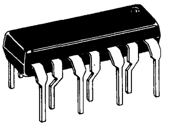
- Direct Replacement for the CA3065
- Differential Peak Detector Requiring a Single Tuned Circuit
- Electronic Attenuator Replaces Conventional ac Volume Control – Range > 60 dB
- Excellent AM Rejection @ 4.5 and 5.5 MHz
- High Stability
- Low Harmonic Distortion
- Audio Drive Capability – 6.0 mAp-p
- Minimum Undesirable Output Signal @ Maximum Attenuation

IF AMPLIFIER, LIMITER, FM DETECTOR, AUDIO DRIVER, ELECTRONIC ATTENUATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

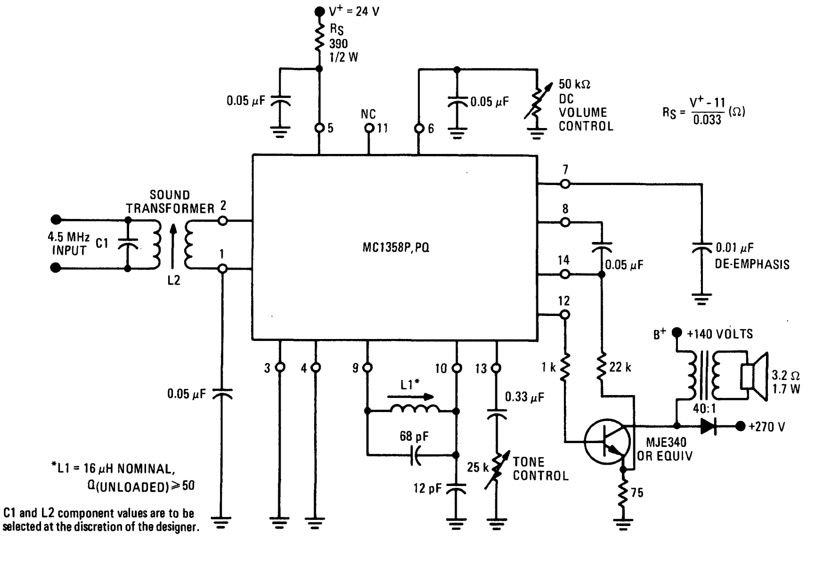
P SUFFIX
PLASTIC PACKAGE
CASE 646





PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL TV APPLICATION CIRCUIT



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Input Signal Voltage (Pins 1 and 2)	±3.0	Vdc
Power Supply Current	50	mA
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = 24 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Unit
Regulated Voltage	5	10.3	11	12.2	Vdc
DC Supply Current (V^+ = 9 Vdc, R_S = 0)	5	10	16	24	mA
Quiescent Output Voltage	12	–	5.1	–	Vdc

DYNAMIC CHARACTERISTICS (V^+ = 24 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
IF AMPLIFIER AND DETECTOR				
f_o = 4.5 MHz, Δf = ±25 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	51	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	0.5	0.70	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.4	2.0	%
f_o = 5.5 MHz, Δf = ±50 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	53	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV [rms])	0.5	0.91	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.9	–	%
Input Impedance Components (f = 4.5 MHz, measurement between pins 1 and 2) Parallel Input Resistance Parallel Input Capacitance	 – –	 17 4.0	 – –	 kΩ pF
Output Impedance Components (f = 4.5 MHz, measurement between pin 9 and GND) Parallel Output Resistance Parallel Output Capacitance	 – –	 3.25 3.6	 – –	 kΩ pF
Output Resistance, Detector Pin 7 Pin 8	 – –	 7.5 250	 – –	 kΩ Ω
ATTENUATOR				
Volume Reduction Range (See Figure 8) (dc Volume Control = ∞)	60	–	–	dB
Maximum Undesirable Signal (See Note 1) (dc Volume Control = ∞)	–	0.07	1.0	mV
AUDIO AMPLIFIER				
Voltage Gain (V_{in} = 0.1 V(rms), f = 400 Hz)	17.5	20	–	dB
Total Harmonic Distortion (V_o = 2.0 V(rms), f = 400 Hz)	–	2.0	–	%
Output Voltage (THD = 5%, f = 400 Hz)	2.0	3.0	–	V(rms)
Input Resistance (f = 400 Hz)	–	70	–	kΩ
Output Resistance (f = 400 Hz)	–	270	–	Ω

*100% FM, 30% AM Modulation.

Note 1. Undesirable signal is measured at pin 8 when volume control is set for minimum output.

8

TYPICAL CHARACTERISTICS

(V^+ = 24 V, T_A = +25°C unless otherwise noted)

(f_o = 4.5 MHz)

FIGURE 2 – AM REJECTION

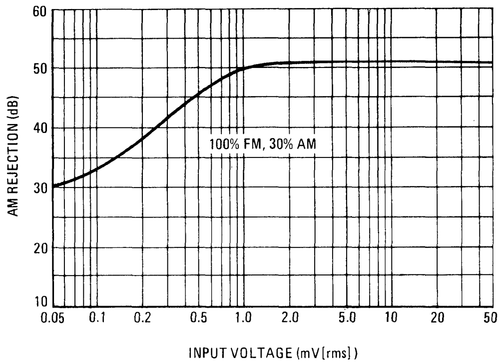


FIGURE 4 – DETECTED AUDIO OUTPUT

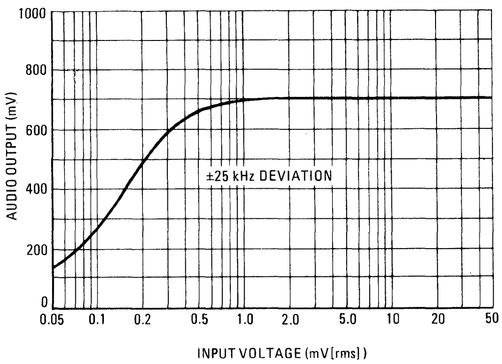
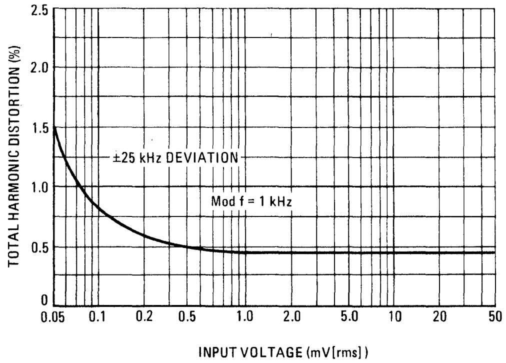


FIGURE 6 – IF AMPLIFIER AND DETECTOR THD



(f_o = 5.5 MHz)

FIGURE 3 – AM REJECTION

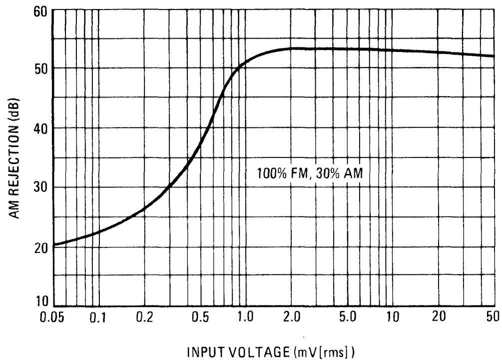


FIGURE 5 – DETECTED AUDIO OUTPUT

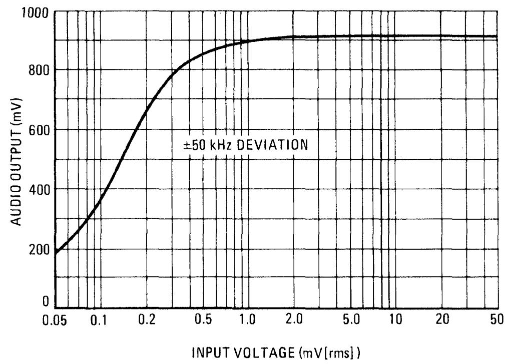
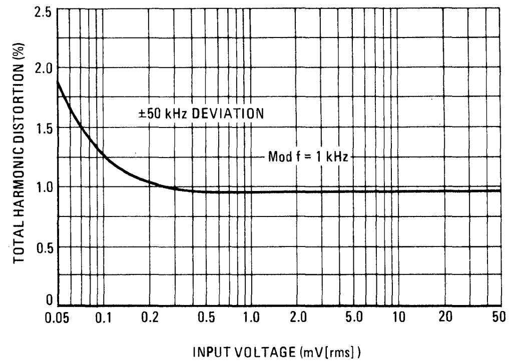


FIGURE 7 – IF AMPLIFIER AND DETECTOR THD



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – GAIN REDUCTION OF ATTENUATOR

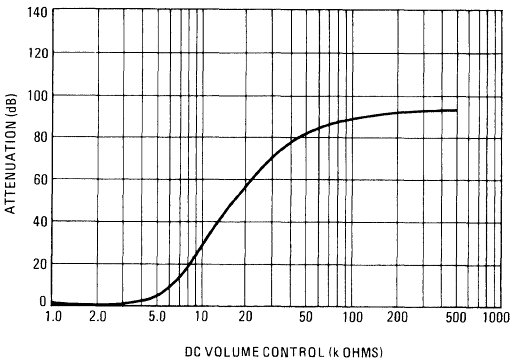


FIGURE 9 – AUDIO AMPLIFIER THD

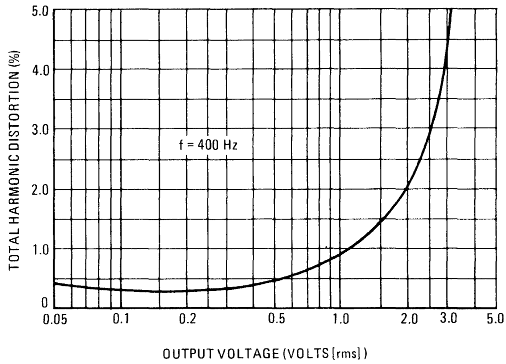


FIGURE 10 – IF FREQUENCY RESPONSE

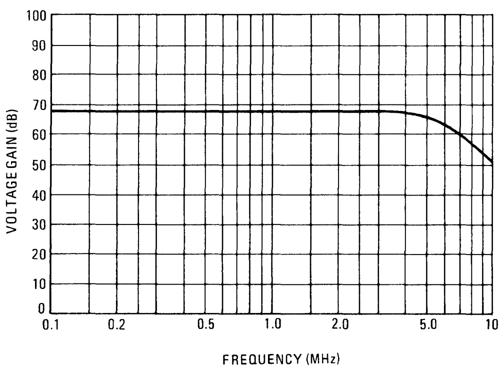


FIGURE 11 – IF FREQUENCY RESPONSE TEST CIRCUIT

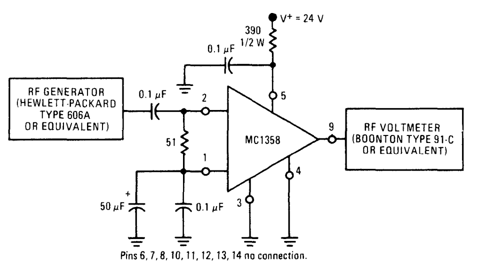


FIGURE 12 – AM REJECTION, DETECTED AUDIO, THD, ATTENUATION TEST CIRCUIT

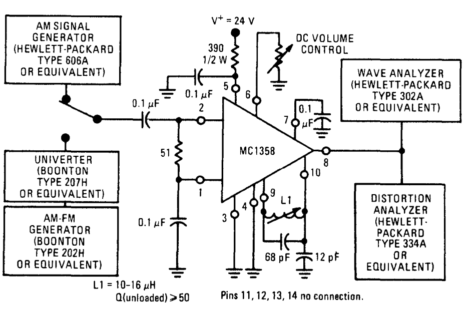


FIGURE 13 – AUDIO VOLTAGE GAIN, AUDIO THD TEST CIRCUIT

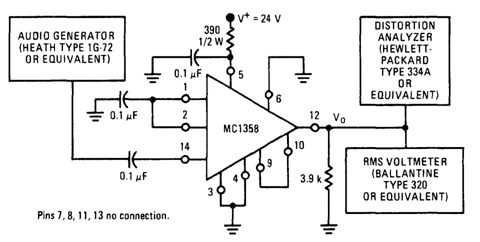
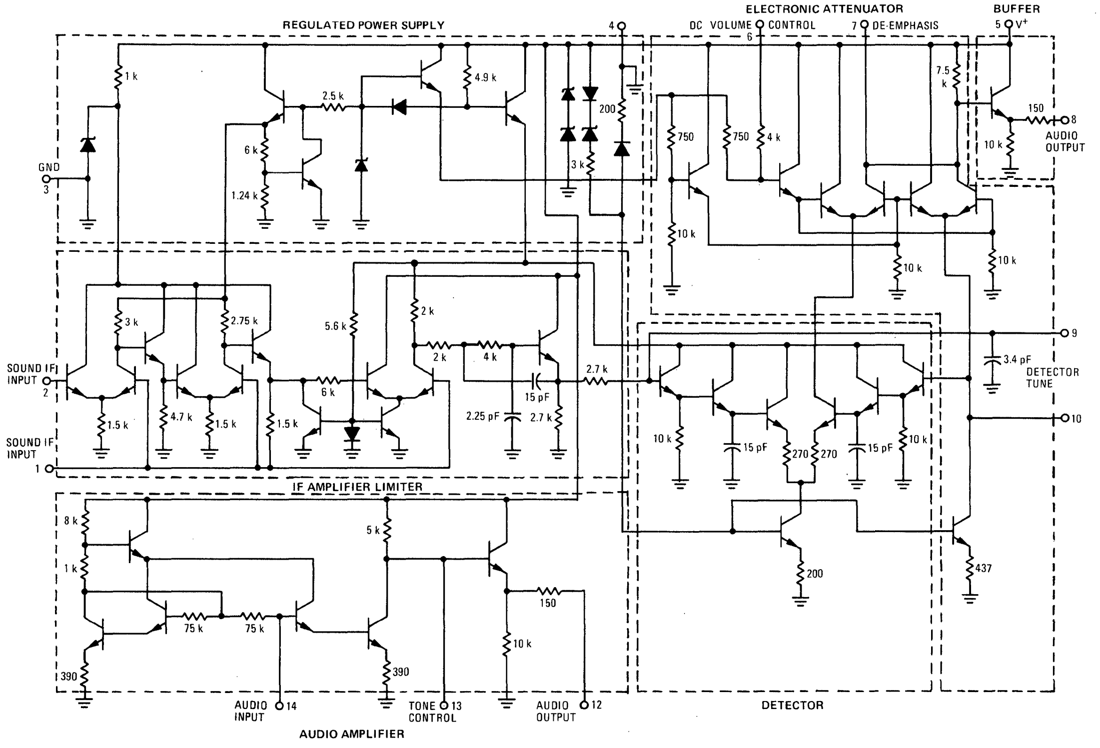


FIGURE 14 – CIRCUIT SCHEMATIC



MC1364

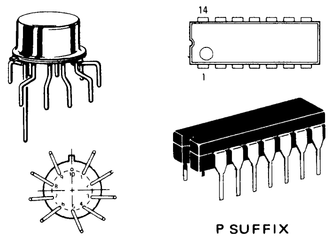
AUTOMATIC FREQUENCY CONTROL

MONOLITHIC TV AUTOMATIC FREQUENCY CONTROL

- High Gain Amplifier – 18 mV Input for Full Output
- Direct Replacement for the CA3064
- Also Available in the 14-Lead Dual In-Line Package

AUTOMATIC FREQUENCY CONTROL

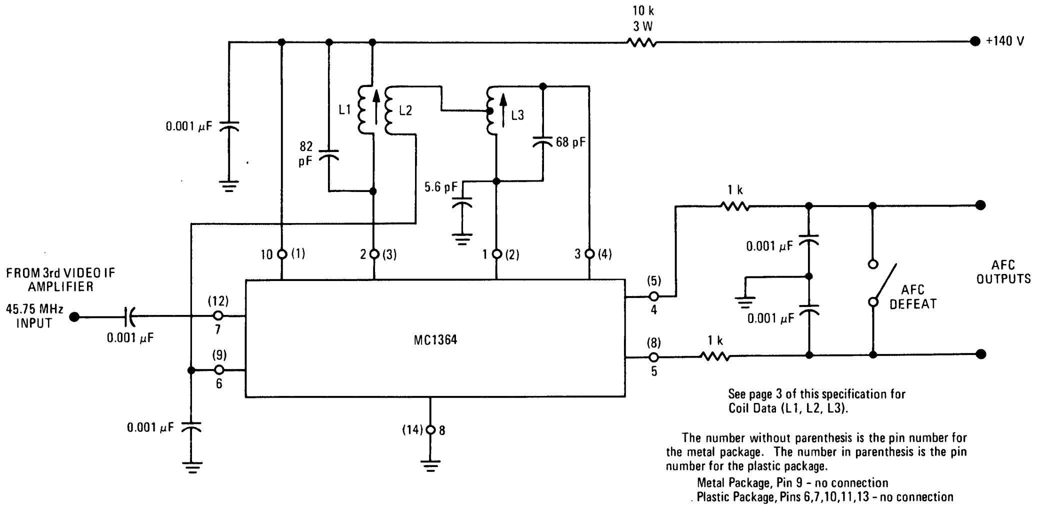
MONOLITHIC SILICON INTEGRATED CIRCUIT



G SUFFIX
CASE 686
METAL PACKAGE

P SUFFIX
CASE 646
PLASTIC PACKAGE

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



See page 3 of this specification for Coil Data (L1, L2, L3).

The number without parenthesis is the pin number for the metal package. The number in parenthesis is the pin number for the plastic package.
Metal Package, Pin 9 - no connection
Plastic Package, Pins 6,7,10,11,13 - no connection

See Packaging Information Section for outline dimensions.

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted, see Note 1)

Rating	MC1364G	MC1364P	Unit
Input Signal Voltage (Pin 7 to 8)	+2.0, -10	+2.0, -10	Vdc
Output Collector Voltage (Pins 2 and 8)	20	20	Volts
Power Dissipation (Package Limitation) Derate above T_A = +25°C	680 5.6	625 5.0	mW mW/°C
Operating Temperature Range	-40 to +85	0 to +75	°C
Storage Temperature Range	-65 to +150	-65 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +30 Vdc, T_A = +25°C, see Test Circuit of Figure 4 unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Total Device Dissipation	–	140	–	mW
Total Supply Current	–	12	–	mA
Current Drain, Total (Reduce V_{CC} so that V10 = 10.5 Vdc)	4.0	6.5	9.5	mA
Zener Regulating Voltage	10.9	11.8	12.8	V
Quiescent Current to Pin 2	1.0	2.0	4.0	mA
Quiescent Voltage at Pin 4 or Pin 5	5.0	6.6	8.0	V
Output Offset Voltage (Pin 4 to Pin 5)	-1.0	0	+1.0	V

DESIGN PARAMETERS, TYPICAL VALUES (V_{CC} = +30 Vdc, R_S = 1.5 k, f = 45.75 MHz).

Parameter	Symbol	Typ	Unit
Input Admittance	y_{11}	0.4 + j1	mmho
Reverse Transfer Admittance	y_{12}	0 + j3.4	μmho
Forward Transfer Admittance	y_{21}	110 + j140	mmhos
Output Admittance (Pin 2)	y_{22}	0.02 + j1	mmho

Note 1: Pin numbers used in the above tables are for the metal package, Case 686. For corresponding pin numbers for the plastic package, Case 646, see the Test Circuit, Figure 4 .

TYPICAL CHARACTERISTICS

(See Test Circuit of Figure 2)

FIGURE 2 – TYPICAL NARROW BAND DYNAMIC CHARACTERISTICS

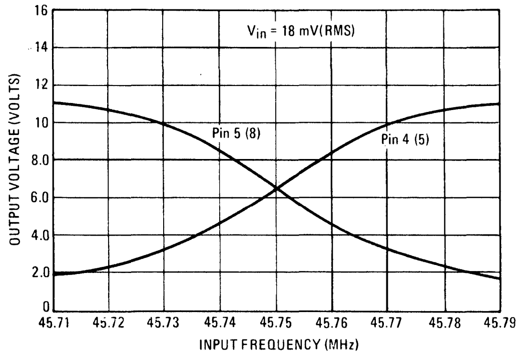
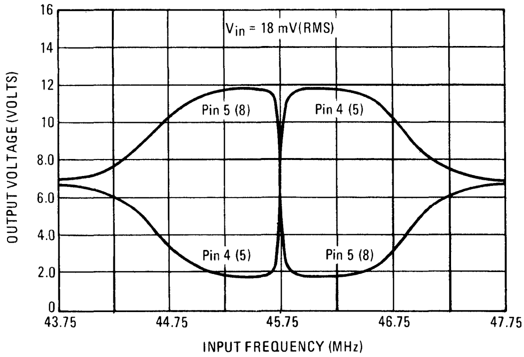
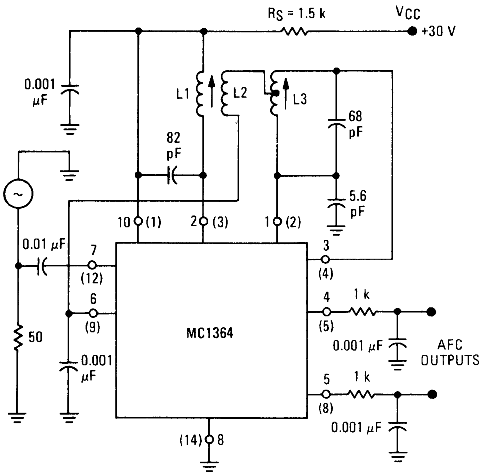


FIGURE 3 – TYPICAL WIDE BAND DYNAMIC CHARACTERISTICS



8

FIGURE 4 – TEST CIRCUIT



$$R_S = \frac{V_{CC} - 11.8}{0.012} \text{ ohms}$$

The number without parenthesis is the pin number for the metal package. The number in parenthesis is the pin number for the plastic package.
Metal Package, Pin 9 - no connection
Plastic Package, Pins 6,7,10,11,13 - no connection

COIL DATA FOR DISCRIMINATOR WINDINGS FOR FIGURES 1 AND 4

L1 – Discriminator Primary: 3-1/6 turns; AWG #20 enamel-covered wire – close-wound, at bottom of coil form. Inductance of L1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz.
Start winding at Terminal #6; finish at Terminal #1. See Notes below.

L2 – Tertiary Windings: 2-1/6 turns; AWG #20 enamel-covered wire – close-wound over bottom end of L1.
Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L3 – Discriminator Secondary: 3-1/2 turns; AWG #20 enamel-covered wire, center-tapped, space wound at bottom of coil form.
Start winding at Terminal #2; finish at Terminal #5, connect center tap to Terminal #7. See Notes below.

Notes:
1. Coil Forms; Cylindrical; -0.30" Dia. Max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   Material: Carbinal J or equivalent.
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.
5. Mount the coils 3/4" apart, center to center.

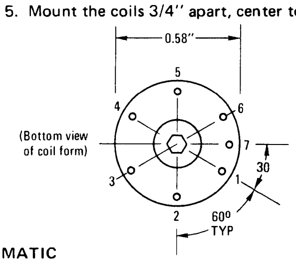
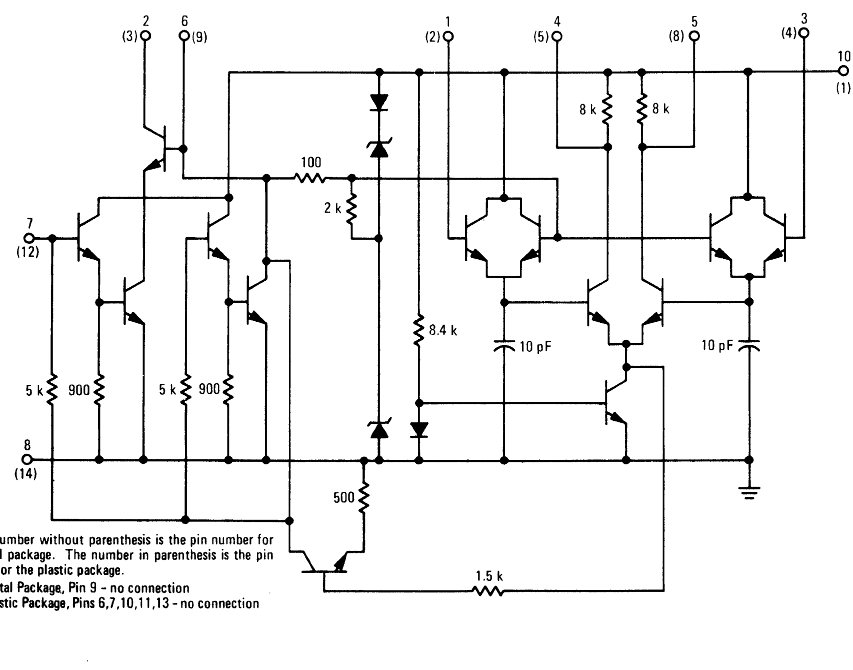


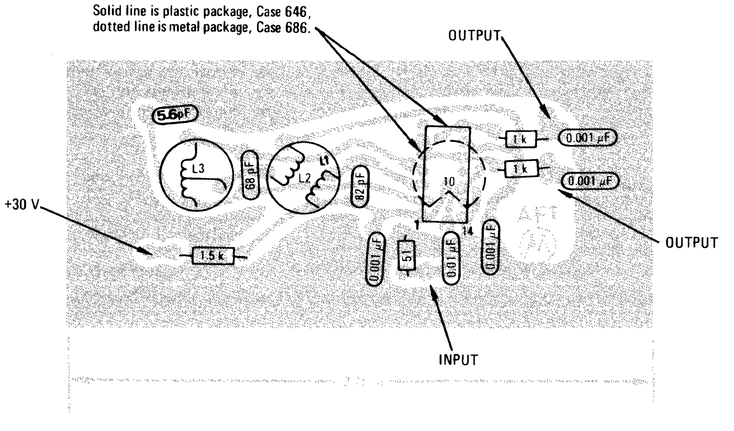
FIGURE 5 – CIRCUIT SCHEMATIC



The number without parenthesis is the pin number for the metal package. The number in parenthesis is the pin number for the plastic package.
Metal Package, Pin 9 - no connection
Plastic Package, Pins 6,7,10,11,13 - no connection

8

FIGURE 6 – PRINTED CIRCUIT BOARD AND PARTS ARRANGEMENT
(Copper Side)



MC1370P

CHROMA SUBCARRIER SYSTEM

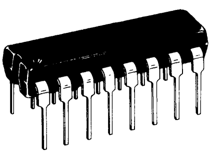
TELEVISION CHROMA SUBCARRIER REGENERATOR

. . . a monolithic device designed for solid-state television receivers, provides a gated voltage controlled oscillator, phase-locked loop and dc hue control.

- Sensitive Voltage Controlled 3.58 MHz Crystal Oscillator
- High-Gain Automatic Phase Control (APC) Loop
- Wide-Range dc Control of Regenerated Subcarrier Phase
- Synchronous Automatic Chroma Control (ACC) Detector
- Internal Shunt Regulated Power Supply
- Internal Gating for Color Burst
- Complements MC1371P Color IF Amplifier
- Direct Replacement for the CA3070

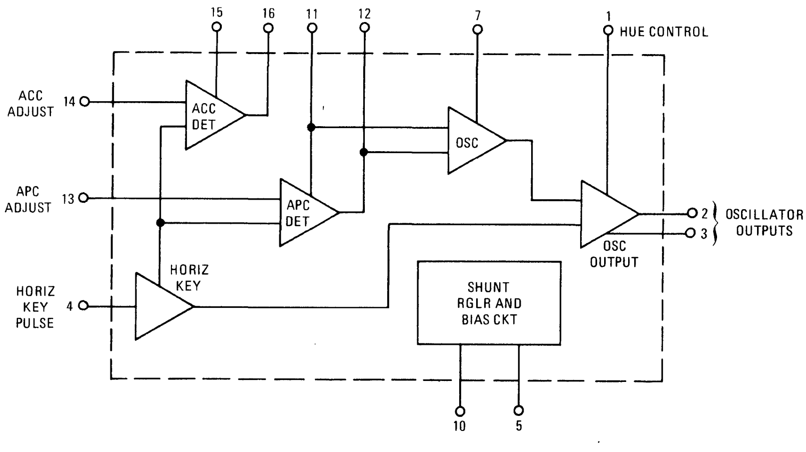
TELEVISION CHROMA SUBCARRIER REGENERATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

FIGURE 1 – MC1370P SYSTEM BLOCK DIAGRAM



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Maximum Supply Voltage (through 470 ohms to pin 10)	30	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +24 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
STATIC CHARACTERISTICS (See Test Circuit of Figure 2, S1, S2 and S3 in position 1 unless otherwise noted.)				
Power Supply Current (S2 in position 2)	–	27	–	mA
Regulator Voltage (pin 10)	11	11.8	12.9	Vdc
Load Regulation (pin 10) (V_{CC} from +21 V to +27 V)	–	35	–	mVdc
Oscillator Current (pins 2 and 3, S1 in position 2)	4.1	6.5	7.5	mA
APC Detector Current (pin 11 or pin 12)	1.0	1.5	1.8	mA
ACC Detector Current (pin 15 or pin 16)	1.0	1.5	1.8	mA
APC Detector Leakage Current (pin 11 or 12, S2 in position 3)	–	–	40	μA
ACC Detector Leakage Current (pin 15 or 16, S2 in position 3)	–	–	30	μA
APC Detector Balance (voltage between pins 11 and 12)	-375	-40	+375	mVdc
ACC Detector Balance (voltage between pins 15 and 16)	-300	-50	+300	mVdc
Oscillator Control Balance (voltage between pins 7 and 8, S2 in position 3, S3 in position 2)	-330	-10	+330	mVdc
Oscillator Gate Leakage (pin 2 and pin 3)	–	–	2.0	μA
Voltage (pin 1) S2 in position 2 S1 and S2 in position 2 (pin 13) S2 in position 2 (pin 14) S2 in position 2 (pin 6) S2 in position 2	– 7.2 6.0 6.0 –	100 7.7 6.5 6.5 2.8	300 8.2 7.0 7.0 –	mVdc Vdc
DYNAMIC CHARACTERISTICS (E_{burst} = 200 mVp-p at pin 13, see test circuit of Figure 3 and note for setup.)				
Oscillator Output Voltage (pin 2, S1 in position 1) (pin 3, S1 in position 3)	– –	1.6 1.6	– –	Vp-p
Oscillator Control Sensitivity (β)	–	10	–	Hz/mV
Oscillator Pull-in Range (Above f_O = 3.579545 MHz) (Below f_O = 3.579545 MHz)	– –	+400 -600	– –	Hz
APC Loop Static Phase Error (with oscillator free-running frequency offset)	–	0.02	–	Deg/Hz
APC Detector Sensitivity (μ)	–	5.0	–	mV/Deg
ACC Detector Sensitivity (ACC output level change for input burst level change)	–	1.4	–	mVdc/mVp-p
Oscillator Noise Bandwidth (f_{NN})	–	150	–	Hz
APC Filter Damping Coefficient (K)	–	0.5	–	–
Input Impedance (pin 13) (pin 14) (pin 6)	– – –	2.1 2.1 2.2	– – –	kΩ

8

FIGURE 2 – STATIC CHARACTERISTICS TEST CIRCUIT

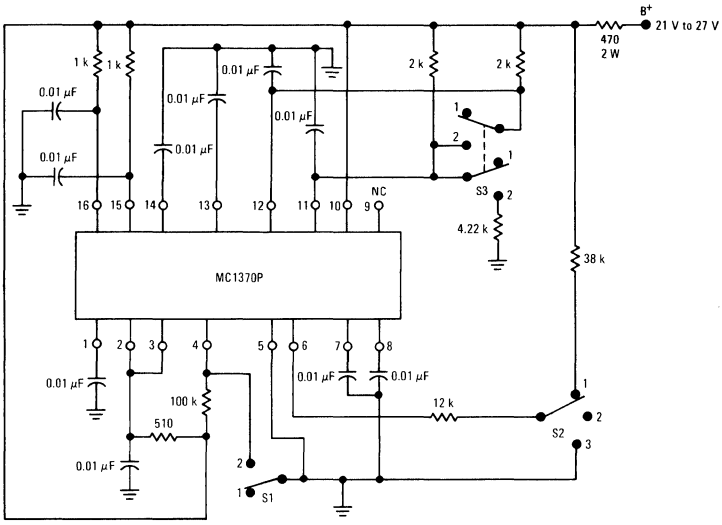
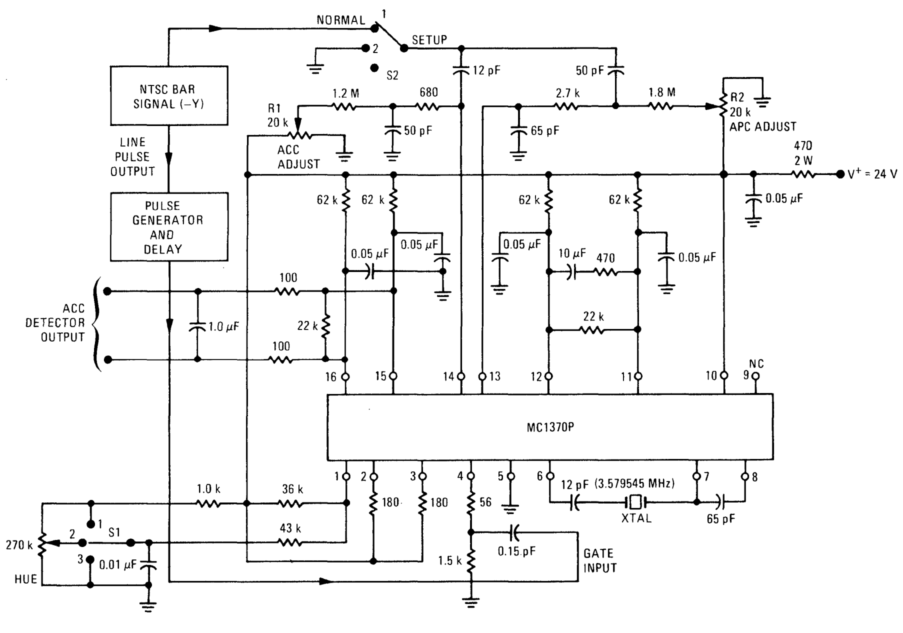


FIGURE 3 – DYNAMIC CHARACTERISTICS TEST CIRCUIT



NOTE: The Set-up Procedure for Dynamic Characteristics Test Circuit

The signal source is an NTSC color bar generator (minus luminance or Y content) applied through an adjustable 3.58 MHz attenuator. The generator horizontal output is used to trigger a pulse generator set to give an output pulse of +4.0 volts, 4.5 μs wide, at a repetition rate of 15.734 kHz. The pulse delay is adjusted to center the pulse during the burst of the color signal (compare gated portion of output at pin 2 or 3 with burst pulse of signal). With S1 set to position 2 and S2 set to position 2, the oscillator is adjusted to 3.579545 MHz by R2. R1 is adjusted to produce zero offset between pins 15 and 16. When S2 is set to position 1, the oscillator should synchronize to the incoming signal.

8

FIGURE 4 – TYPICAL CHROMA APPLICATIONS CIRCUIT
(MC1370P, MC1371, MC1328 AND MPSU10)

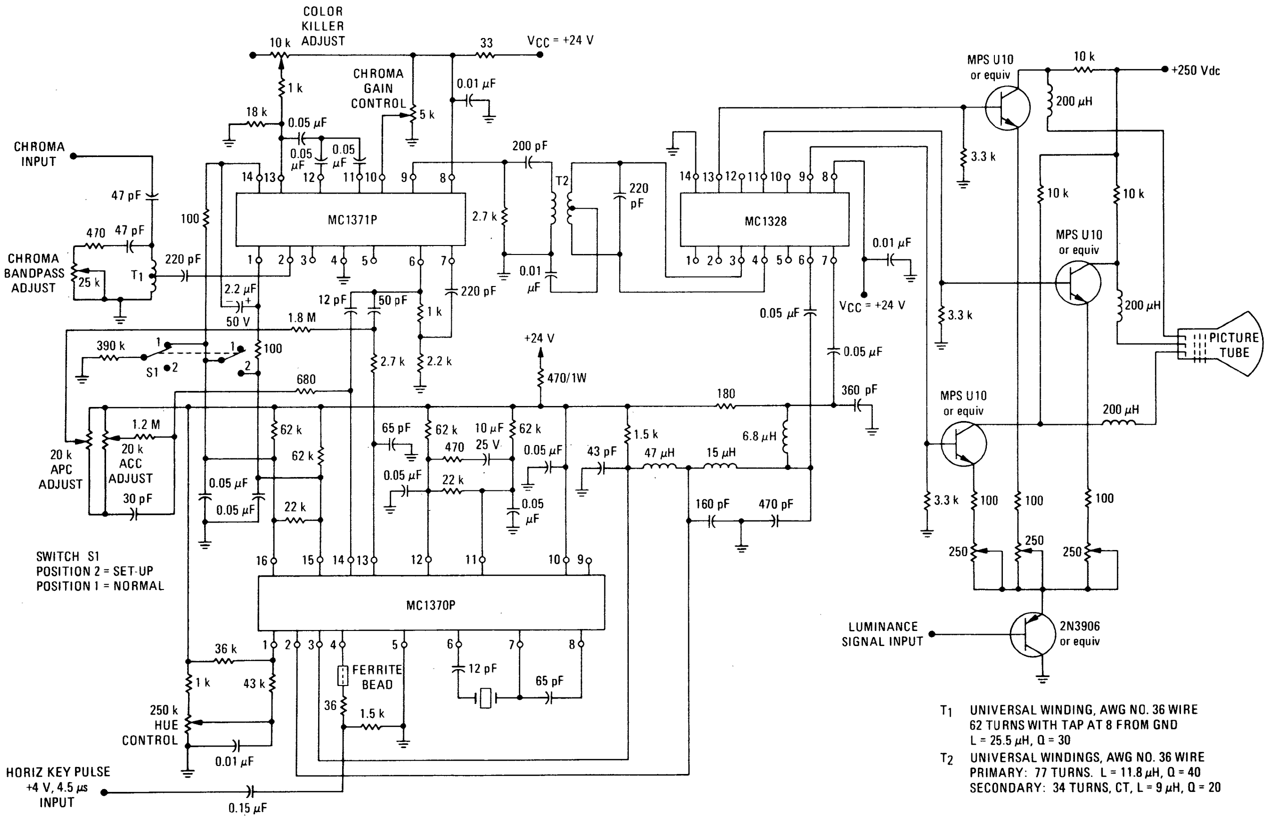
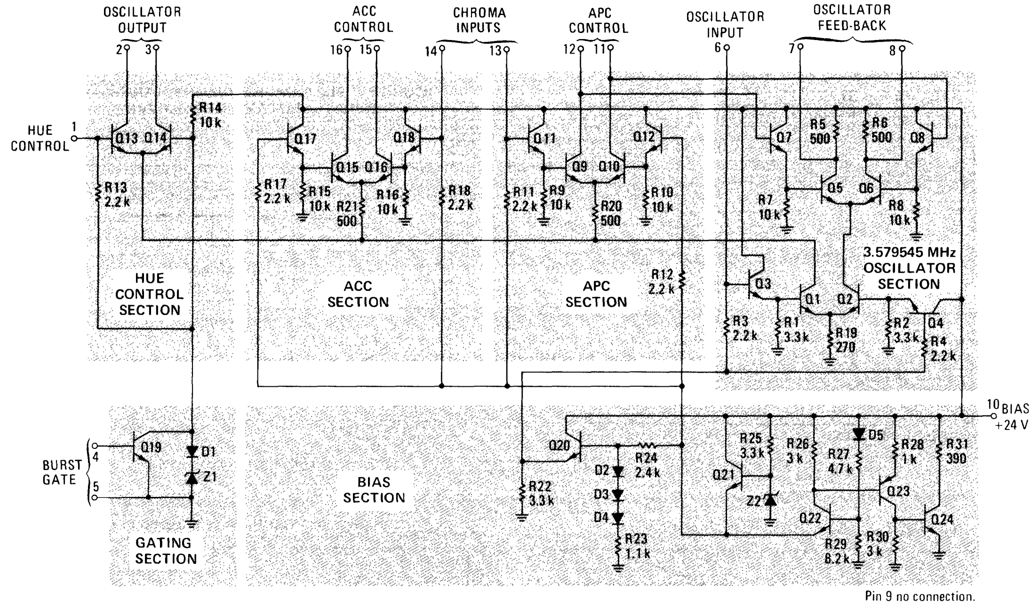


FIGURE 5 – CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1370 monolithic circuit provides the sub-carrier regeneration function necessary for a color television receiver to decode the NTSC color signal. An internal gate extracts the burst voltage and this signal is processed in two-phase detectors, the quadrature detector controls the phase of the local oscillator and the in-phase detector is used to provide a noise immune ACC and color killer control voltage. A shunt regulator sets the bias voltages and ensures stable operation when there are supply voltage variations.

The basic 3.579545 MHz oscillator consists of the differential amplifier (Q1 and Q2) with a feed-back loop through a quartz crystal operating in series resonance from Q2 collector to the noninverting input of the amplifier represented by Q1 base. To control the oscillator frequency the phase shift of the feed-back path is made variable by the addition of Q5 and Q6. A capacitor connected between pins 7 and 8, together with the collector loads, forms a RC phase-shift network. Consequently, the oscillator signal appearing at pin 7 can be moved in phase over a 45^{o} range by the differential bias applied to Q5 and Q6 bases. The crystal between pins 7 and 6 completes the feed-back loop. The automatic phase control to the upper differential pairs of the (Q5, Q6) oscillator is through the buffer stages Q7 and Q8. The oscillator amplifier is buffered by Q3 and Q4. Output from the oscillator is obtained from the collector of Q1 and is essentially a square wave of 9 mA peak-to-peak with a frequency range of several hundred Hertz.

The control voltage for Q5 and Q6 is obtained from the phase detector Q9 and Q10. As Q1 is the current source for this pair, the voltages appearing at pins 11 and 12 will correspond to the phase difference between the oscillator current and the burst signal applied to pin 13. The loop characteristics are controlled in part by a filter connected between pins 11 and 12. This is usually a double-time constant network to yield good pull-in times with a low-noise bandwidth.

To ensure that the quadrature phase detector functions only during the burst portion of the incoming chroma signal, the detector is gated into conduction by a pulse from the line flyback transformer – applied at pin 4. This has the additional advantage that the average current in the phase detector has been reduced by the gate duty factor thus relaxing the input offset stability requirements of the differential pair and enabling them to be used with high dc gain.

For the ACC control voltage and color-killer function a similar phase detector, Q15 and Q16, is used. However, the chroma signal input to pin 14 is phase shifted externally by 90^{o} with respect to pin 13. As a result, Q15 and Q16 is an in-phase detector and the control voltage at pins 15 and 16 will be proportional to the amplitude of the burst. Thus filtering of pins 15 and 16 provides the control voltage for the gain control stage in the chroma IF and an indication of the incoming signal strength for the color-killer circuit.

When the phase detectors are not gated "on" by a positive pulse at pin 4, the bases of Q13 and Q14 are held above the bases of the phase detector inputs. Therefore, between gate pulses, all the current from the oscillator output Q1 passes through Q13 and Q14 to pins 2 and 3. When a phase-shift network is connected between pins 2 and 3, the phase of the oscillator drive to the demodulators can be controlled by changing the relative conduction of Q13 and Q14 with a bias on pin 1. As a result the oscillator output is controlled in phase providing a dc hue control and is gated "off" during the burst period, negating the need for burst blanking in the chroma IF amplifier.

TYPICAL CHARACTERISTICS

FIGURE 6 – STATIC PHASE ERROR versus FREQUENCY OFFSET

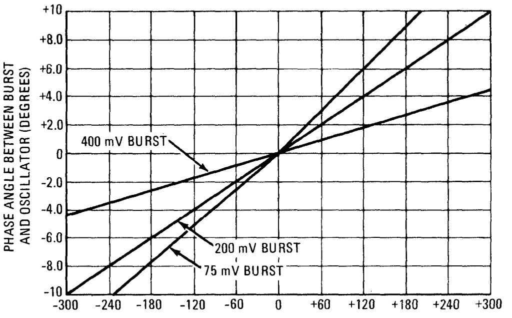


FIGURE 7 – PULL-IN FREQUENCY RANGE versus BURST INPUT VOLTAGE LEVEL

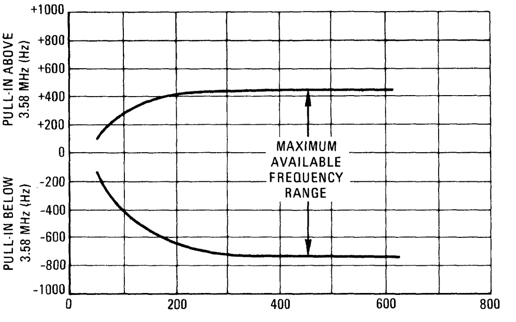


FIGURE 8 – ACC DETECTOR SENSITIVITY

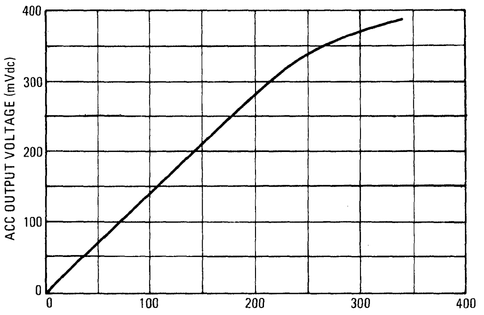
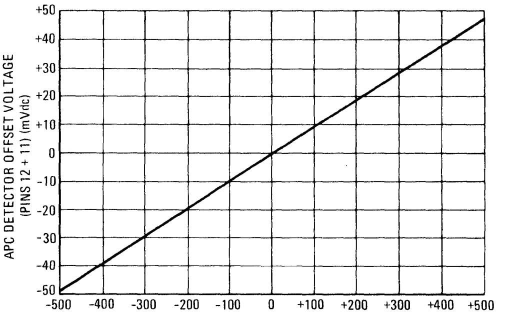


FIGURE 9 – OSCILLATOR SENSITIVITY



DEFINITIONS

Oscillator Sensitivity (β)
. . . the change in oscillator free-running frequency for a change in differential control voltage, measured in Hertz/millivolts.

APC Detector Sensitivity (μ)
. . . the differential voltage change produced at the detector output for a given change in oscillator phase relative to burst phase, measured for a given burst input amplitude in millivolts/degrees.

ACC Detector Sensitivity
. . . the differential voltage produced at the detector output for a given change in burst input amplitude with the oscillator locked in synchronism, measured in millivolts dc/millivolts (p-p).

Noise Bandwidth (f_N)
. . . actually noise semibandwidth, f_{NN} (= 2 X f_N); a measure of the susceptibility of the burst channel to thermal noise (i.e. dynamic phase error).

Filter Damping Coefficient (K)
. . . describes the shape of the loop input phase versus output phase response ($Q\omega$) – K = 1 represents critical damping, K > 1 over damping.

MC1371P

CHROMA IF AMPLIFIER

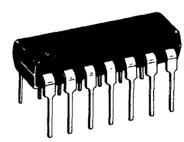
TELEVISION CHROMA IF AMPLIFIER

. . . a monolithic device designed to provide the basic control and color signal amplification stages of a solid-state color television receiver. The MC1371 is a combination of two wideband chroma amplifiers and a color control circuit.

- Schmitt Color-Killer Circuit with Adjustable Trigger Level
- Linear Action dc Manual Gain Control
- Short-Circuit Protected
- Gain Stabilized Against Supply Voltage and Temperature Changes
- Low Phase Distortion
- Excellent Gain Linearity Over Full Output Range
- Direct Replacement for the CA3071

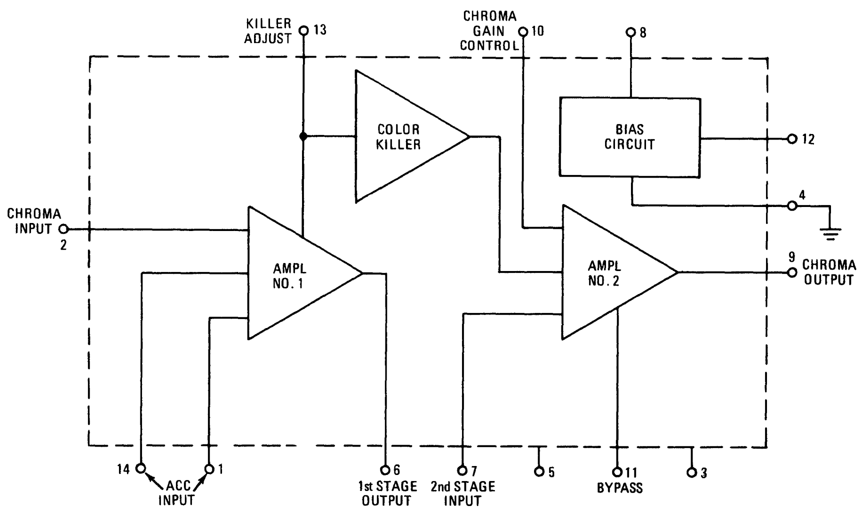
TELEVISION CHROMA IF AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – MC1371P SYSTEM BLOCK DIAGRAM



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Amplifier Output Short-Circuit Duration	30	s
Power Dissipation (Package Limitation) Plastic Dual In-Line Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +24 Vdc, T_A = +25°C unless otherwise noted. See Test Circuit of Figure 2; switch S1 in position 1, R1 wiper at ground, R2 = 10 kilohms.)

Characteristic	Min	Typ	Max	Unit
Static Characteristics				
Quiescent Power Supply Current	17	28	31	mA
Short-Circuit Current (pin 6 momentarily grounded) (pin 9 momentarily grounded)	 – –	 68 48	 – –	mA
First Chroma Stage Input Bias Voltage (pin 2)	–	1.7	–	Vdc
First Chroma Stage Output Bias Voltage (pin 6) ACC Balanced (S1 in position 1) ACC Unbalanced (S1 in position 2)	 13.7 7.5	 16.3 10.5	 20 13.5	Vdc
Second Chroma Stage Input Bias Voltage (pin 7)	–	1.4	–	Vdc
Second Chroma Stage Output Bias Voltage (pin 9)	16.6	17.6	18.6	Vdc
Quiescent Bias Voltage (pin 12)	13.8	14.8	15.7	Vdc
Dynamic Characteristics (f = 3.579545 MHz, input pin 2 = 35 mV [RMS] unless otherwise noted.)				
First Chroma Amplifier Stage Gain (ACC Balanced)	14	17	20	dB
Second Chroma Amplifier Stage Gain (R1 wiper at ground)	 12	 15.5	 17	 dB
Maximum Linear Output (output level at pin 9)	–	2.0	–	V(RMS)
Output Voltage, pin 9 (input pin 2 = 50 mV [RMS]) (R1 wiper at V_{CC}) (R1 wiper at ground, R2 adjusted for abrupt ac change in pin 9 output voltage)	 – –	 – –	 12 12	mV(RMS)
Pin 10 Bias Voltage (R1 set for 10% of pin 9 maximum output) (R1 set for 90% of pin 9 maximum output)	 16.7 2.5	 20.2 3.2	 21.6 4.5	Vdc
Second Amplifier Gain Stability (V_{CC} + 15%) (V_{CC} –15%) (T_A = +25°C to +75°C)	 – – –	 +0.5 –0.5 +0.5	 +1.5 -1.5 –	dB
Input Impedance (pin 2) (pin 7) 	 – – – –	 2.0 3.5 2.2 3.6	 – – – –	 kΩ pF kΩ pF
Output Impedance (pin 6) (pin 9)	 – –	 85 85	 – –	ohms

8

TYPICAL CHARACTERISTICS

(V_{CC} = +24 Vdc, f_O = 3.579545 MHz, T_A = +25°C unless otherwise noted.)

FIGURE 2 – TEST CIRCUIT

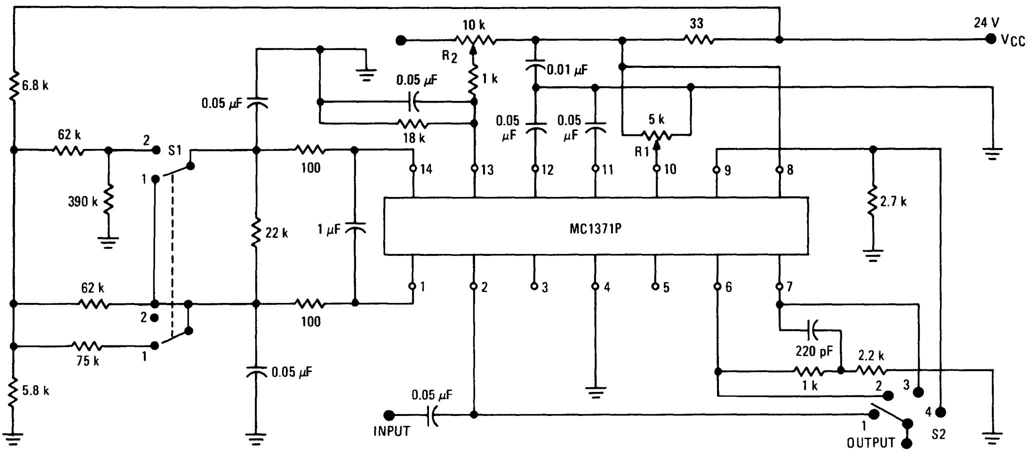


FIGURE 3 – MANUAL GAIN CONTROL LINEARITY

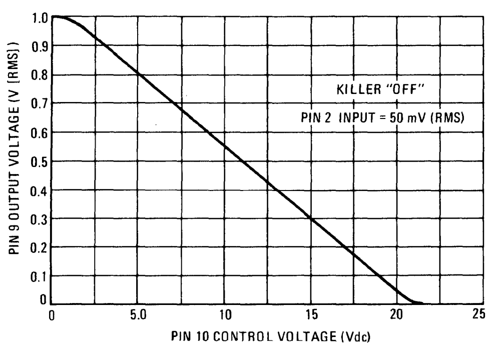


FIGURE 4 – FIRST STAGE GAIN WITH ACC BIAS

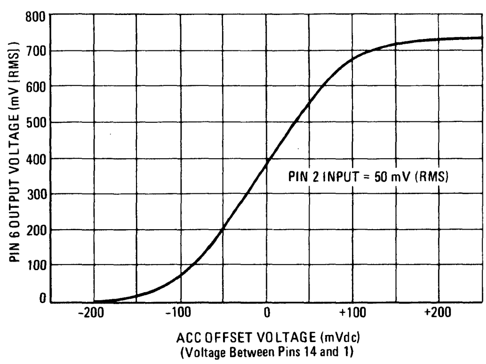


FIGURE 5 – AMPLIFIER LINEARITY

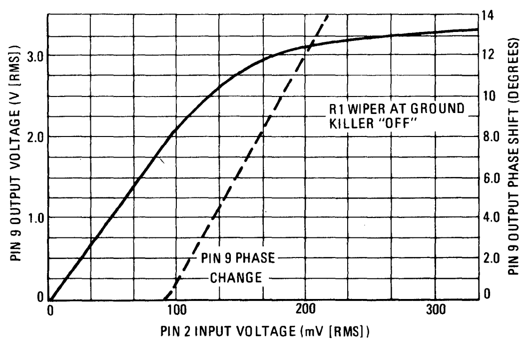
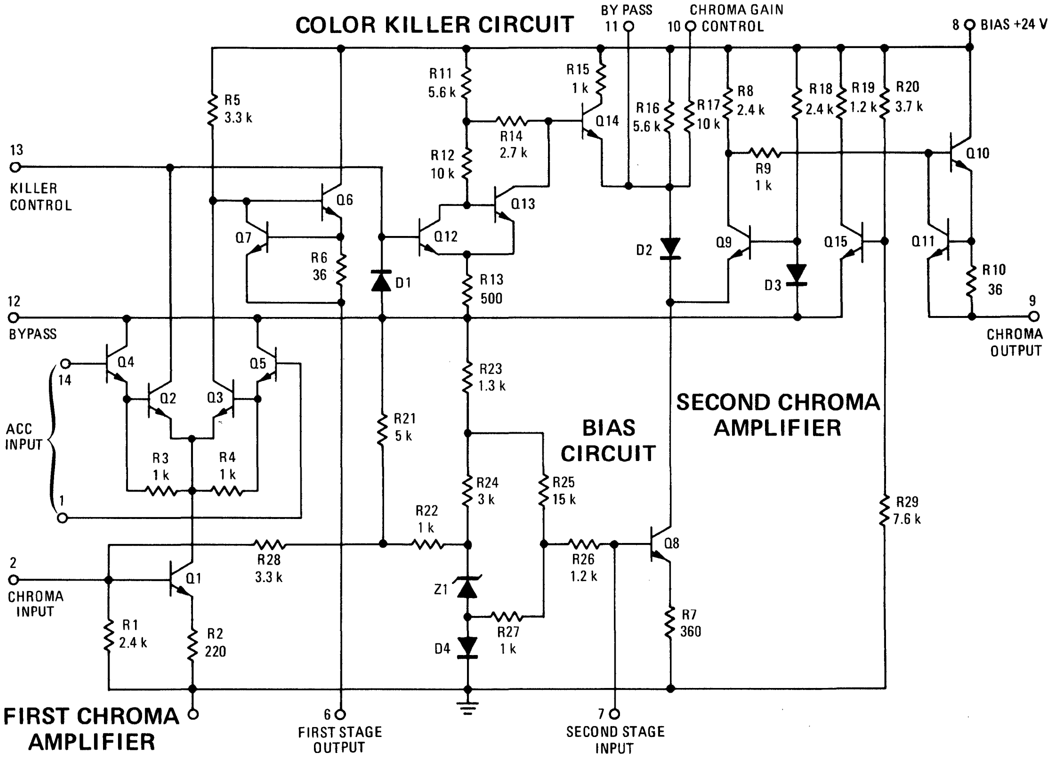


FIGURE 6 – CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1371 is a monolithic wide-band amplifier circuit that functions as the basic control and color signal amplification stages of a color television receiver. The first stage contains the gain control function of the ACC loop and the second stage performs the dc manual gain control function. Also included is a Schmitt trigger circuit providing effective color-killer action during monochrome transmissions.

Q1 is a current source modulated by the input signal applied at pin 2. The current in Q1 is divided between the differential pair (Q2 and Q3) in a ratio determined by the ACC voltage applied through the buffer stages, Q4 and Q5. Pin 14 is usually offset with respect to pin 1 by a resistor connected to ground so that at low-signal levels most of the signal current is taken by Q3 and passed to the load resistor R5 (the input stage appears as a cascode amplifier to the signal with the intrinsic ac stability of that configuration). The amplified signal is then buffered at pin 6 by the emitter follower stage Q6 which is protected from accidental grounding at the output by the current limiter Q7.

At strong signals when the amplitude of the burst is high, the ACC voltages at pins 1 and 14 divert most of the signal current from Q3. The signal is "dumped" into the collector load of Q2. Q2 is connected externally at pin 13 and bypassed to ground at signal frequencies by a capacitor. However, the dc voltage at the collector of Q2 is dependent on the burst amplitude and therefore on the input signal strength. As the input signal level falls, more current is fed into Q3 by the ACC loop and the output at pin 6 remains constant while Q2 collector voltage increases. At a point predetermined by Q2 collector load (the killer-control setting) the input Q12 of the color-killer circuit is biased "on", shutting down the second chroma amplifier stage.

The second chroma stage is similar in configuration to the first stage. The signal input at pin 7 (which is the output from pin 6) modulates the current source Q8. For a maximum gain voltage setting on pin 10 the signal current passes through Q9 to the output buffer stage Q10. Q10 is protected from short circuit currents by Q11. To reduce the stage gain, current is diverted from Q9 by biasing the diode D2 into conduction. D2 can be regarded as a transistor with 100% dc negative feedback applied between collector and base. Without the feedback path the gain characteristic of the second stage is that of a differential pair, this S shaped curve would make tracking of ganged color level and contrast controls quite difficult. In this limiting form the current through D2 is directly proportional to the voltage difference between the supply and D2 anode and hence to the control voltage at pin 10. When the input to the color-killer is biased "on", Q13 is turned "off" and the voltage at the base of Q14 rises abruptly. D2 then takes all the current from Q8 and the output at pin 9 is suppressed.

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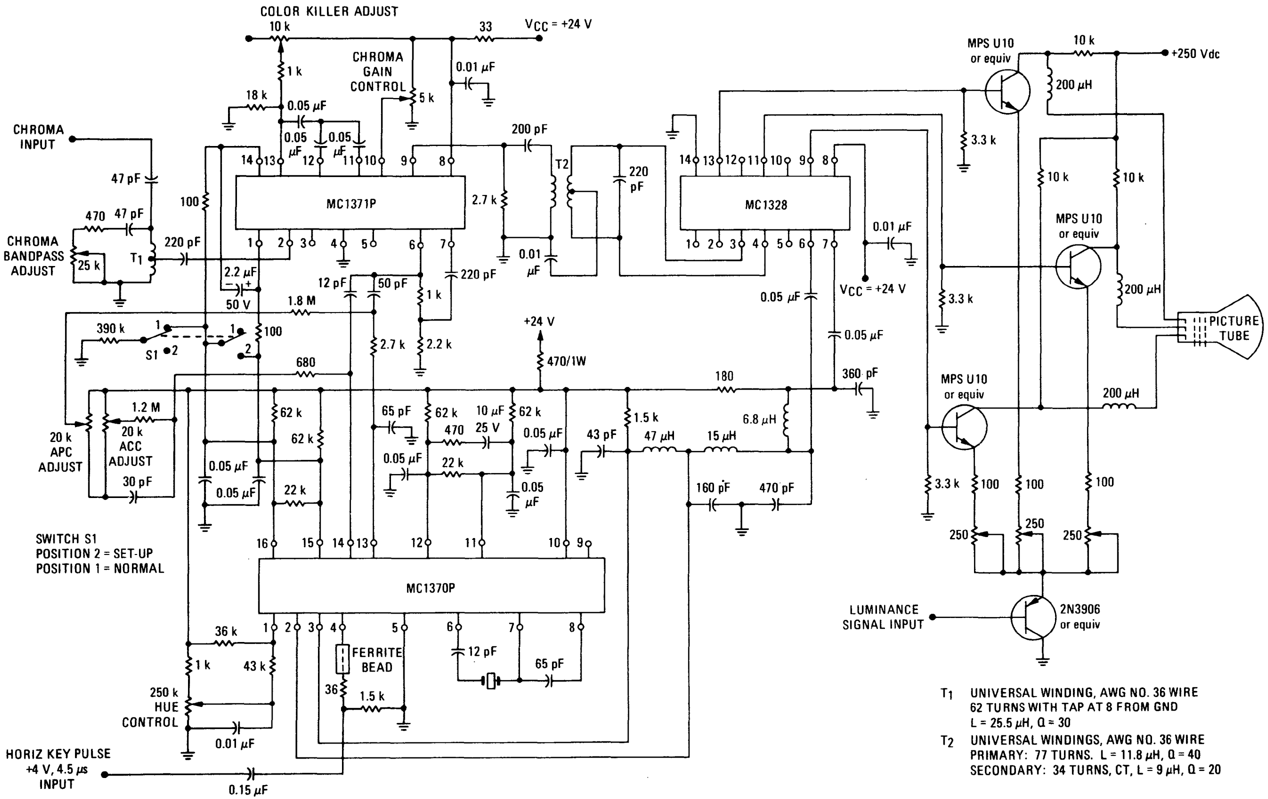
FIGURE 7 – TYPICAL CHROMA APPLICATIONS CIRCUIT
(MC1370, MC1371, and MPS U10)



T_1 UNIVERSAL WINDING, AWG NO. 36 WIRE
62 TURNS WITH TAP AT 8 FROM GND
L = 25.5 μH, Q = 30

T_2 UNIVERSAL WINDINGS, AWG NO. 36 WIRE
PRIMARY: 77 TURNS. L = 11.8 μH, Q = 40
SECONDARY: 34 TURNS, CT, L = 9 μH, Q = 20

MC1375P

FM IF CIRCUIT

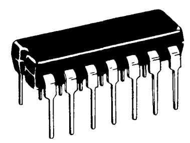
FM IF AMPLIFIER, LIMITER, FM DETECTOR, AND AUDIO PREAMPLIFIER

. . . a monolithic device designed for use in solid-state FM receivers.

- Excellent Sensitivity: Input Limiting Voltage (Knee) = 250 μV typical
- Excellent AM Rejection: 55 dB typical at 10.7 MHz
- Internal Zener Diode Regulation for the IF Amplifier Section
- Low Harmonic Distortion
- Differential Peak Detection: Permits Simplified Single-Coil Tuning
- Audio Preamplifier Voltage Gain: 21 dB typical
- Minimum Number of External Parts Required
- Direct Replacement for CA3075

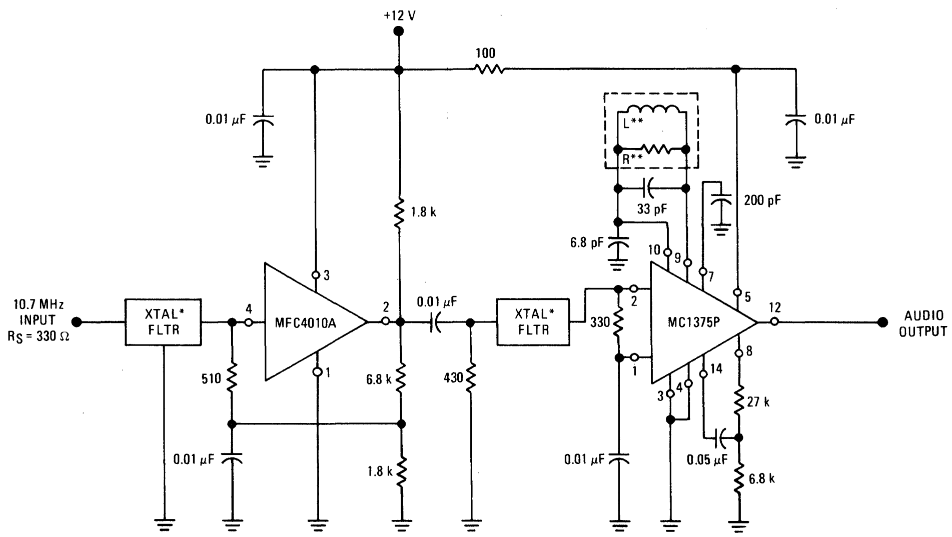
FM IF AMPLIFIER, LIMITER, FM DETECTOR AND AUDIO PREAMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – TYPICAL FM APPLICATION



*10.7 MHz Filter; Vernitron FM-4 or equivalent
**L = 6.0 μH nom
Adjust R for $Q_L \approx 55$

Pins not shown are not connected.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	+16	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +11.2 Vdc, V_{EE} = Gnd, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Current Drain	–	19	29	mA
DC Voltage at pin 8 (V_{in} = 0)	–	5.4	–	Vdc
Amplifier Input Resistance (V_{in} = 20 mV, 10.7 MHz)	–	5.0	–	kΩ
Amplifier Input Capacitance (V_{in} = 20 mV, 10.7 MHz)	–	5.0	–	pF

DYNAMIC CHARACTERISTICS (V_{CC} = +11.2 Vdc, V_{EE} = Gnd, f_{mod} = 1.0 kHz, T_A = +25°C unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
IF AMPLIFIER AND DETECTOR (f_O = 10.7 MHz, Δf = ±75 kHz)				
AM Rejection* (V_{in} = 10 mV)	–	55	–	dB
Input Limiting Threshold Voltage	–	250	600	μV(RMS)
Recovered Audio Output Voltage	500	625	–	mV(RMS)
Output Distortion (V_{in} = 10 mV[RMS])	–	0.75	–	%
Signal-to-Noise Ratio (V_{in} = 1.0 mV)	–	68	–	dB
AUDIO AMPLIFIER (Audio Test Frequency; f = 1.0 kHz)				
Voltage Gain (V_{in} = 100 mV)	–	21	–	dB
Total Harmonic Distortion (V_O = 2.0 V[RMS])	–	1.2	–	%
Input Impedance (pin 14)	–	100	–	kΩ

*100% FM, 30% AM Signal

TYPICAL CHARACTERISTICS

(All measurements at $T_A = +25^oC$, V_{CC} = 11.2 V; see test circuits of Figure 9 and 10.)

FIGURE 2 – AM REJECTION

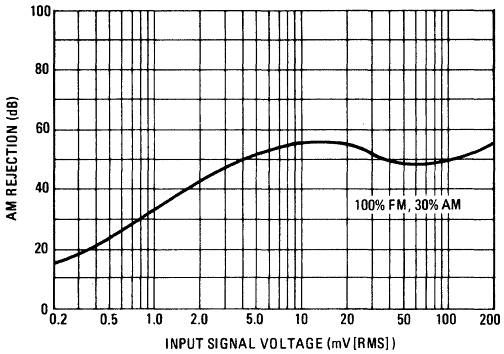


FIGURE 3 – RECOVERED AUDIO OUTPUT

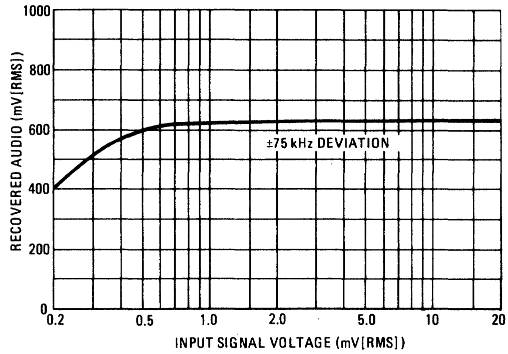


FIGURE 4 – IF AMPLIFIER AND DETECTOR THD

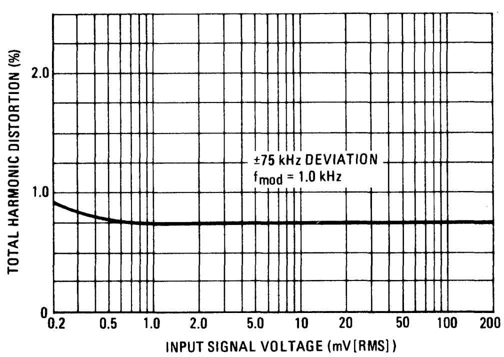


FIGURE 5 – SIGNAL TO NOISE

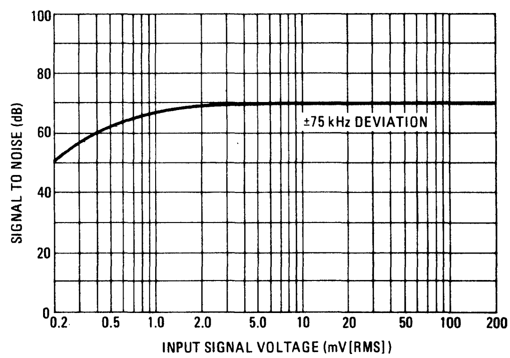


FIGURE 6 – AUDIO AMPLIFIER THD

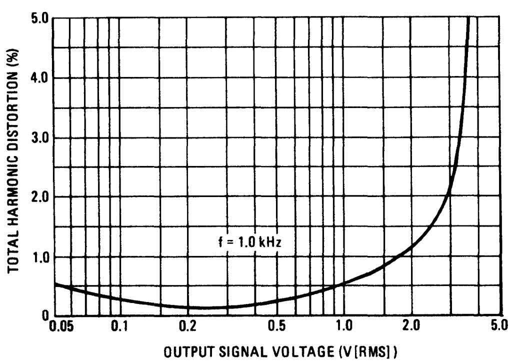


FIGURE 7 – CURRENT DRAIN versus SUPPLY VOLTAGE

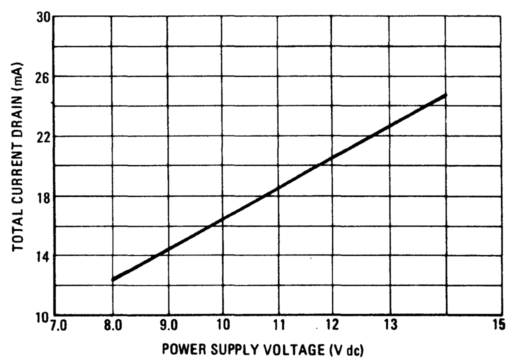


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FIGURE 8 – CIRCUIT SCHEMATIC

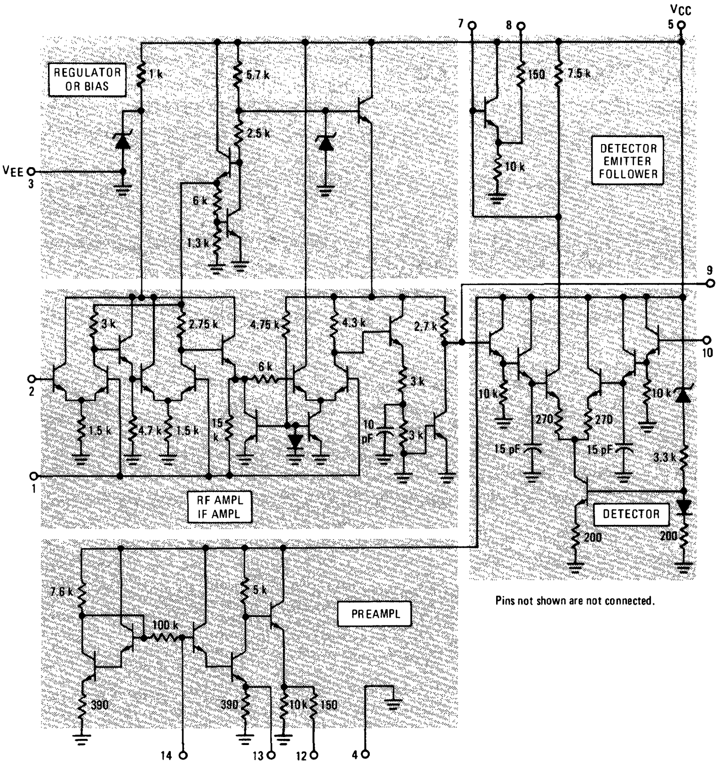


FIGURE 9 – AM REJECTION, THD, RECOVERED AUDIO, AND S/N TEST CIRCUIT

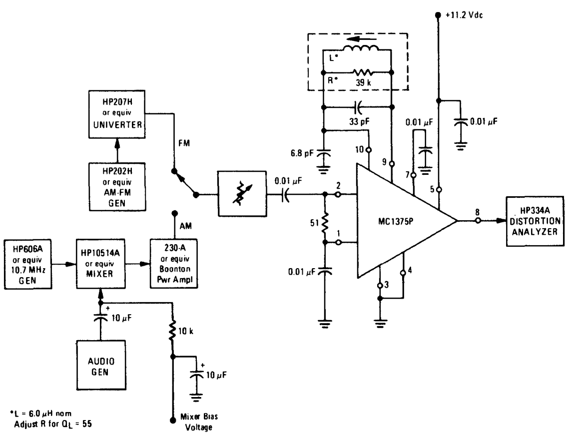
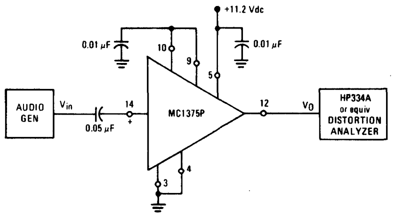


FIGURE 10 – AUDIO VOLTAGE GAIN AND THD TEST CIRCUIT



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MC1385P

AUDIO DRIVER

Product Preview

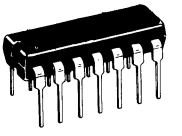
MONOLITHIC CLASS B AUDIO DRIVER

. . . designed to be used in conjunction with class B output transistors MJE2050/MJE2150 to produce a class B audio amplifier suitable for auto radio. It is ideal for low-voltage, single-supply audio driver applications as found in Automotive, Consumer and Industrial Electronics.

- Internal Power Supply Transient Protection
- Built-in Programmable Short-Circuit Current Limiting
- Excellent Sensitivity - 4.0 mV(RMS) typical
- Class B Operation
- Excellent Power-Supply Ripple Rejection – 35 dB typical

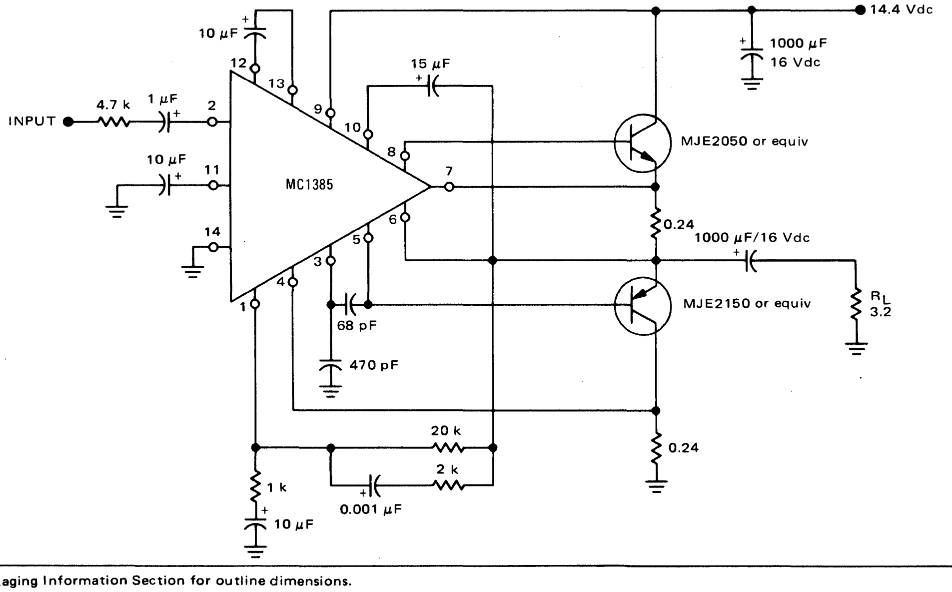
CLASS B
AUDIO DRIVER

MONOLITHIC SILICON
INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Value	Unit
Power Supply Voltage	Steady State	25	Vdc
	Transients of 50 ms or less (Note 1)	40	Vdc
Maximum Sink or Source Current Pin 5 or 8		50	mA
Power Dissipation (Package Limitation) Plastic Package Derate Above T_A = +25°C		 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)		-40 to +85	°C
Storage Temperature Range		-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.4 Vdc, R_L = 3.2 ohms, f = 1.0 kHz, See Figure 1, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Recommended Operating Power Supply Voltage Range	9.0	14.4	16	Vdc
Power Supply Overvoltage Shutdown (Note 1)	–	22	–	Vdc
Drain Current	–	10		mA
Power Output THD = 10%	5.0	–	–	W
Input Sensitivity Voltage P_O = 1.0 W	–	4.0	–	mV(RMS)
Total Harmonic Distortion P_O = 1.0 W	–	0.7	–	%
Output Noise R_S = 4.7 k ohms, BW = 50 Hz – 6.0 kHz	–	2.0	–	mV(RMS)
Power-Supply Ripple Rejection Ripple = 1.0 V(p-p) @ f = 100 Hz, input shorted	–	35	–	dB
Input Impedance	–	5.0	–	k Ω

Note 1 - These specifications were set to meet typical automotive load dump requirements.

8

MC1391P

TV HORIZONTAL PROCESSOR

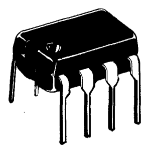
TV HORIZONTAL PROCESSOR

. . . low-level horizontal sections including phase detector, oscillator and pre-driver — a device designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ±300 Hz Typical Pull-In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable dc Loop Gain

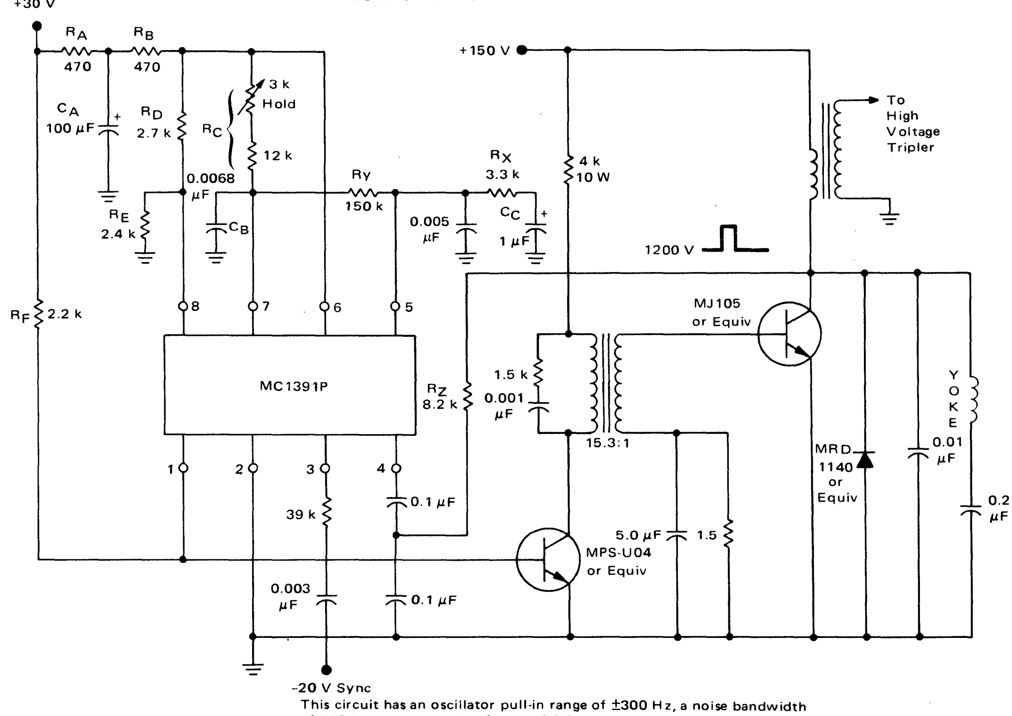
TV HORIZONTAL PROCESSOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

FIGURE 1 — TYPICAL APPLICATION CIRCUIT



This circuit has an oscillator pull-in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Supply Current	40	mAdc
Output Voltage	40	Vdc
Output Current	30	mAdc
Sync Input Voltage (Pin 3)	5.0	$V_{(p-p)}$
Flyback Input Voltage (Pin 4)	5.0	$V_{(p-p)}$
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.) (See Test Circuit of Figure 2, all switches in position 1.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (Pin 6)	8.0	8.4	8.8	Vdc
Supply Current (Pin 6)	–	20	–	mAdc
Collector-Emitter Saturation Voltage (Output Transistor Q1 in Figure 6) (I_C = 20 mA, Pin 1) Vdc	–	0.30	0.35	Vdc
Voltage (Pin 4)	–	2.0	–	Vdc
Oscillator Pull-in Range (Adjust R_H in Figure 2)	–	±300	–	Hz
Oscillator Hold-in Range (Adjust R_H in Figure 2)	–	±900	–	Hz
Static Phase Error (Δf = 300 Hz)	–	0.5	–	μs
Free-running Frequency Supply Dependance (S1 in position 2)	–	±3.0	–	Hz/Vdc
Phase Detector Leakage (Pin 5) (All switches in position 2)	–	–	±1.0	μA
Sync Input Voltage (Pin 3)	2.0	–	5.0	V(p-p)
Sawtooth Input Voltage (Pin 4)	1.0	–	3.0	V(p-p)

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 2 – TEST CIRCUIT

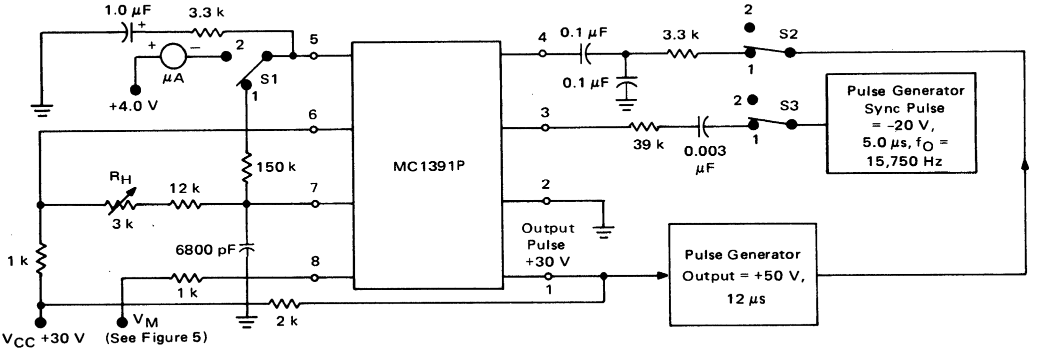


FIGURE 3 – FREQUENCY versus TEMPERATURE

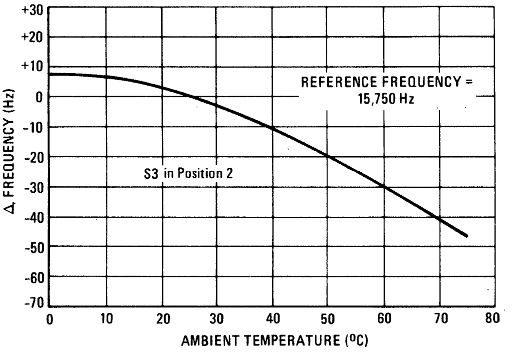


FIGURE 4 – FREQUENCY DRIFT versus WARM-UP TIME

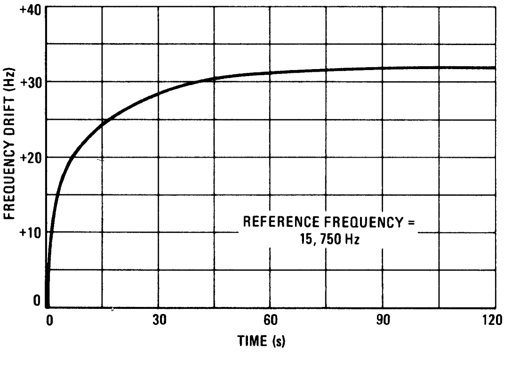


FIGURE 5 – MARK-SPACE RATIO

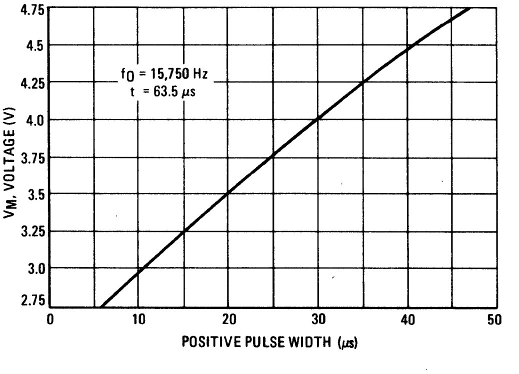
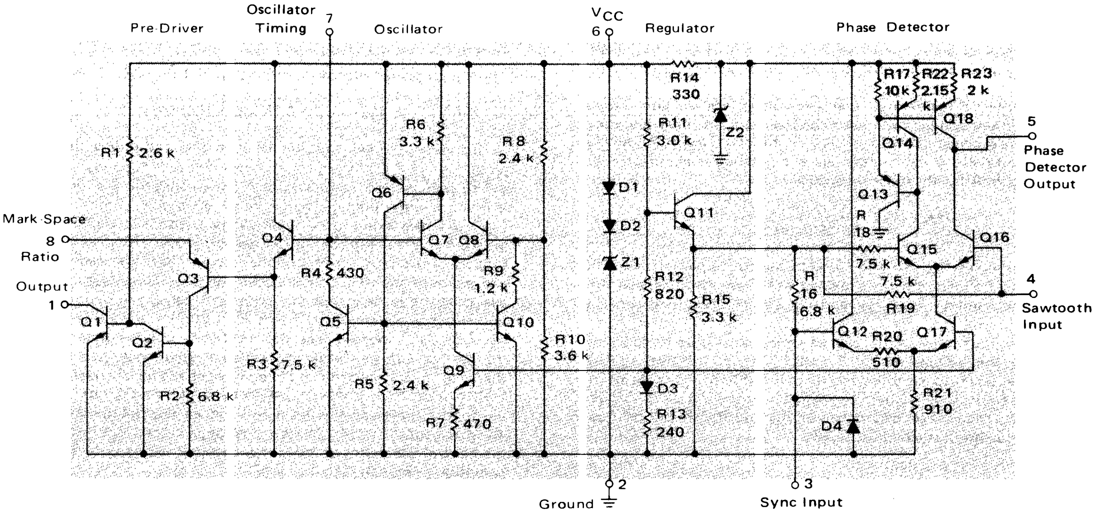


FIGURE 6 – CIRCUIT SCHEMATIC



MC1391P CIRCUIT OPERATION

The MC1391P contains the oscillator, phase detector and pre-driver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing. The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor (R_C) connected to Pin 6. As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 and Q10. Transistor Q10 will set a new, lower potential at the base of Q8 determined by R8, R9 and R10. Then, transistor Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate either tube or transistor horizontal output stages.

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each for half the sync pulse period. The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5. This pin is connected via an external low-pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1.

8

MC1391P APPLICATIONS INFORMATION

Although it is an integrated circuit, the MC1391P has all the flexibility of a conventional discrete component horizontal APC loop.

The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2mA for the external dividers

$$R_A + R_B = \frac{V_{nonreg(min)} - 8.8}{20 \times 10^{-3}}$$

Components R_A, R_B and C_A are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 Volt supply) then R_A and R_B can be combined and C_A omitted.

The output pulse width can be varied from 6 μs to 48 μs by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible to prevent ringing which can result in erroneous output pulses at Pin 1. The parallel impedance of R_D and R_E should be close to 1 kΩ to ensure stable pulse widths.

For 15 mA drive at saturation

$$R_F = \frac{V_{nonreg} - 0.3}{15 \times 10^{-3}}$$

The oscillator free-running frequency is set by R_C and C_B connected to Pin 7. For values of $R_C \gg R_{discharge}$ (R4 in Figure 6), a useful approximation for the free-running frequency is

$$f_O = \frac{1}{0.6\, R_C C_B}$$

Proper choice of R_C and C_B will give a wide range of oscillator frequencies — operation at 31.5 kHz for count-down circuits is possible for example. As long as the product $R_C C_B \approx 10^{-4}$ many combinations of values of R_C and C_B will satisfy the free-running frequency requirement of 15.734 kHz. However, the sensitivity of the oscillator (β) to control-current from the phase detector is directly dependent on the magnitude of R_C, and this provides a convenient method of adjusting the dc loop gain (fc).

For a given phase detector sensitivity (μ) = 1.60×10^{-4} A/rad

$$fc = \mu\beta \text{ and } \beta = 3.15 \times R_C \text{ Hz/mA}$$

Increasing R_C will raise the dc loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop (ω_n) and give a wider pull-in range from an out-of-lock condition. The loop will also tend to be underdamped with fast pull-in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the dc loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the dc loop gain has been selected for adequate S.P.E. performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor R_X with respect to R_Y which modifies the ac/dc gain ratio (m) of the loop. Lowering this ratio will reduce the pull-in range and noise bandwidth (fnn). (Note: very large values of R_Y will limit the control capability of the phase detector with a corresponding reduction in hold-in range).

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT.

NOTE:

In adjusting the loop parameters, the following equations may prove useful:

$$f_{nn} = \frac{1 + \chi^2 T\omega_c}{4\chi T} \qquad \chi = \frac{R_X}{R_Y}$$

$$\omega_n = \sqrt{\frac{\omega_c}{(1+\chi)\,T}} \qquad \omega_c = 2\pi fc$$

$$T = R_Y C_C$$

$$K = \frac{\chi^2 T\omega_c}{4}$$

where:

K = loop damping coefficient

8

MC1398P

TV COLOR PROCESSING CIRCUIT

TV COLOR PROCESSING CIRCUIT

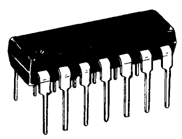
. . . a chroma IF amplifier with automatic chroma control, color killer, dc chroma control, and injection lock reference system followed by dc hue control.

MC1398P is a monolithic device designed for use in solid-state color television receivers.

- Minimum Number of External Components
- DC Control of Both Chroma Amplitude and Hue Shift
- Crystal-Controlled Internal Feedback Oscillator
- Built-in Noise Immunity
- Schmitt Trigger Color Killer
- Automatic Chroma Control
- Internal Burst Gate and Gate Pulse Shaping Circuit
- High Oscillator Lock-in Sensitivity
- Built-in Supply Regulation

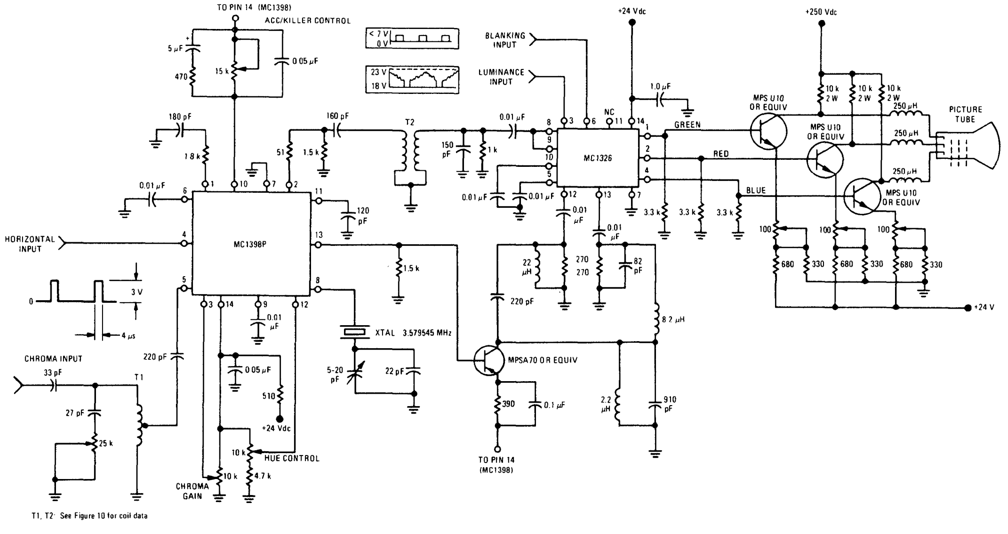
TV COLOR PROCESSING CIRCUIT

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – TYPICAL CHROMA APPLICATIONS CIRCUIT (MC1398P, MC1326 and MPSU10)



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

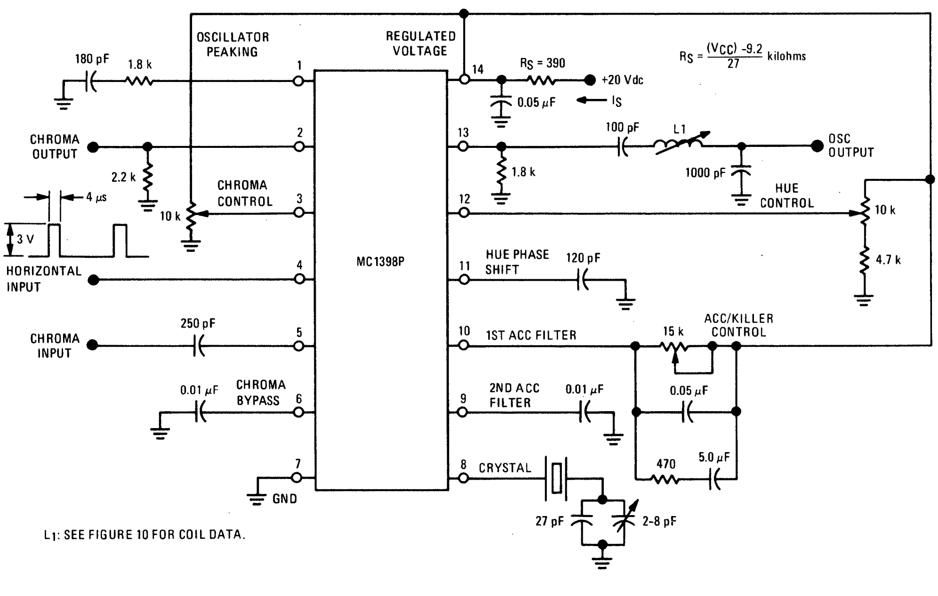
Rating	Value	Unit
Power Supply Current	35	mAdc
Horizontal Pulse Input Current	250	µA Peak
Power Dissipation (package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, R_S = 390 ohms, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (I_S = 35 mA) (I_S = 27 mA)	9.0 –	9.6 9.2	11.5 –	Vdc
Maximum Undistorted Chroma Output, See Note 1, $E_{(pin\ 3)} = E_{(pin\ 14)}$	0.8	1.75	–	V(p-p)
Maximum Chroma Gain $E_{(pin\ 3)} = E_{(pin\ 14)}$, See Note 1	34	40	–	dB
Automatic Chroma Control Range (ACC) -3.0 dB down from maximum undistorted output, see Note 1	–	19	–	dB
Chroma Burst Level to Kill, See Note 1	–	1.4	–	mV(p-p)
Manual Chroma Gain Control Range ($\Delta V_{(pin\ 3)}$ ($V_{(pin\ 14)}$ to 0 Vdc)	50	60	–	dB
Chroma Input Resistance	–	2.3	–	k ohms
Chroma Input Capacitance	–	13	–	pF
Chroma Output Impedance	–	15	–	ohms
Horizontal Input Pulse	2.2	3.0	4.0	Vp
Oscillator Output	100	–	–	mV(RMS)
Oscillator Output Impedance	–	15	–	ohms
Hue Control Range ($\Delta V_{(pin\ 12)}$ ($V_{(pin\ 14)}$ to 4.3 Vdc)	100	126	–	degrees
Oscillator Pull-In Range	1200	–	–	Hz
Oscillator Noise Bandwidth (f_N)	–	900	–	Hz
Static Phase Error with Oscillator Detuning 25 mV(p-p) Burst Amplitude 2.0 mV(p-p) Burst Amplitude	 – –	 0.20 0.25	 – –	degrees/Hz

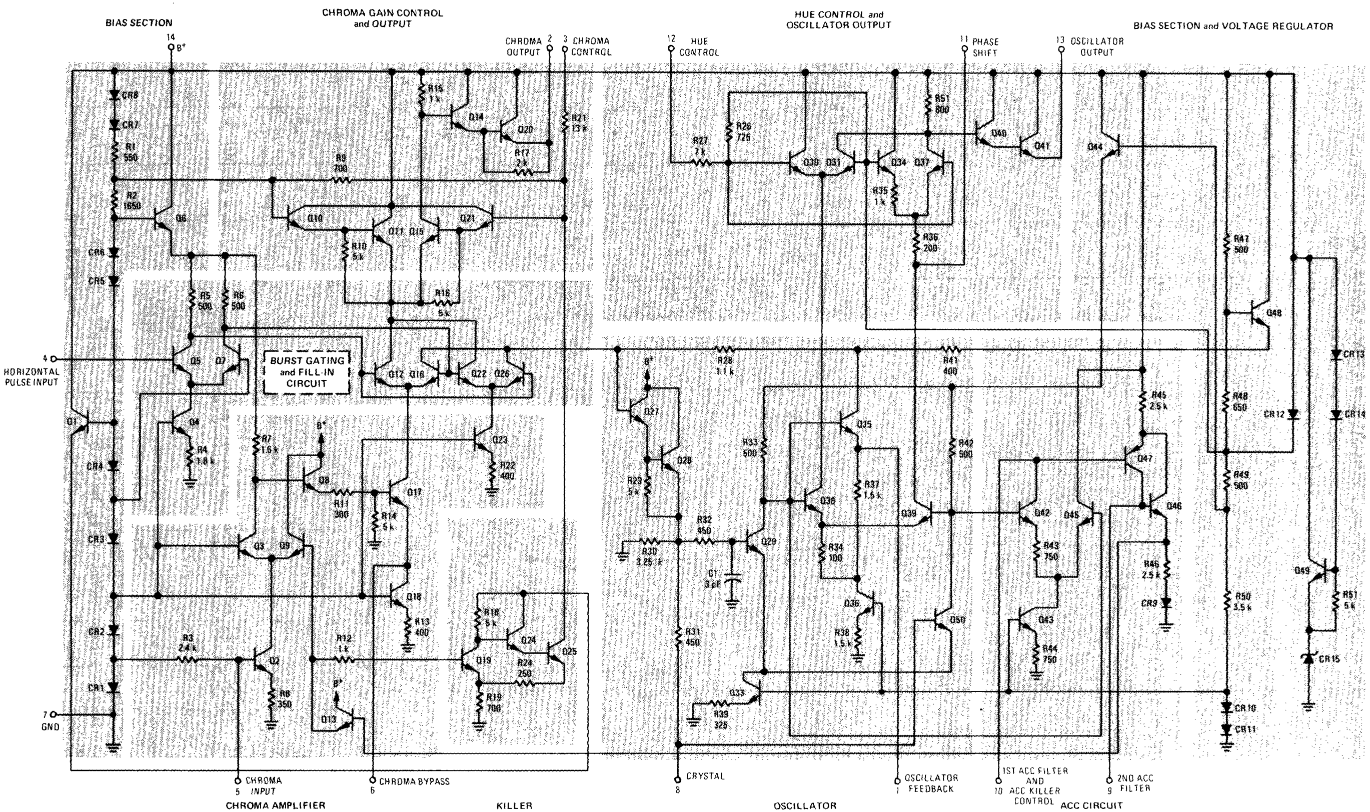
Note 1: With 5.0 mV(p-p) burst input at pin 5 set $E_{(pin\ 10)}$ to just "unkill"

FIGURE 2 – MC1398P TEST CIRCUIT



L1: SEE FIGURE 10 FOR COIL DATA.

FIGURE 3 – MC1398 CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)
(Figures 4 through 9, See Test Circuit of Figure 2.)

FIGURE 4 – INPUT/OUTPUT CHARACTERISTICS

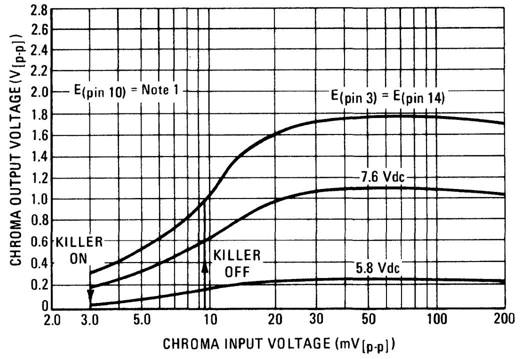


FIGURE 5 – REGULATED VOLTAGE

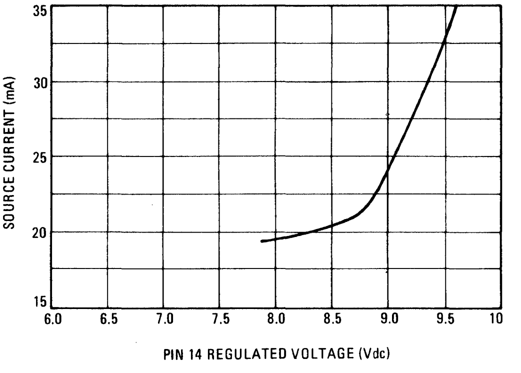


FIGURE 6 – HUE CONTROL OPERATION

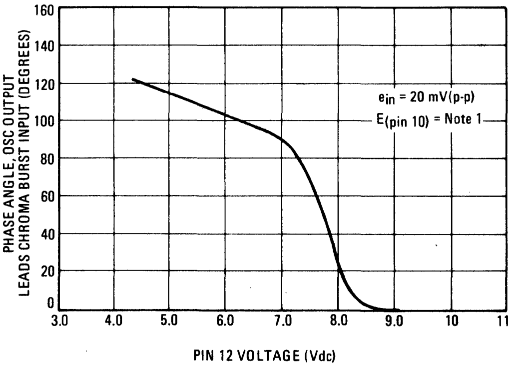


FIGURE 7 – OSCILLATOR OUTPUT versus PIN 12 VOLTAGE

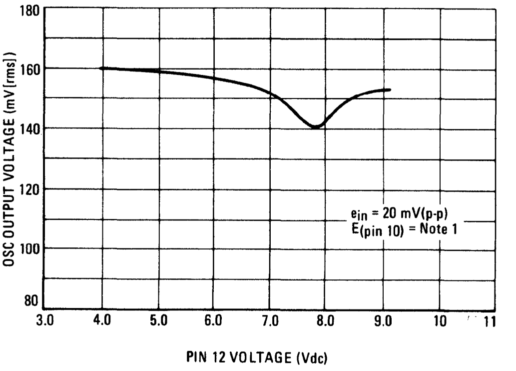


FIGURE 8 – STATIC PHASE ERROR

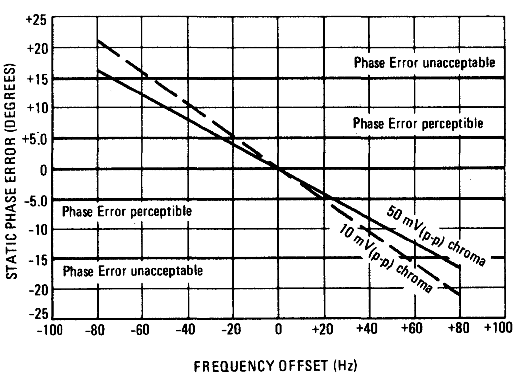


FIGURE 9 – TEMPERATURE STABILITY of the MC1398 OSCILLATOR
(I/C only subjected to temperature change)

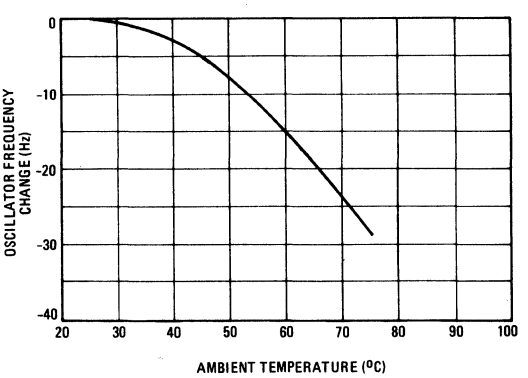


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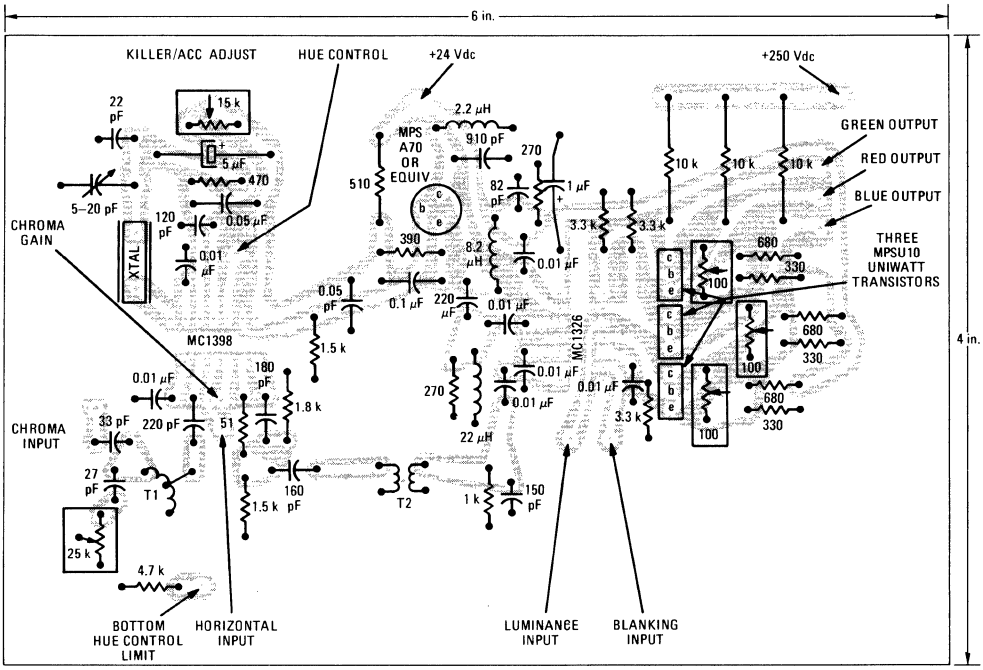
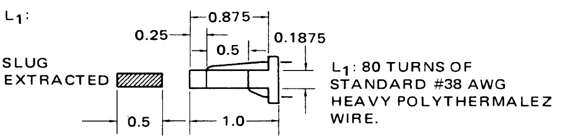
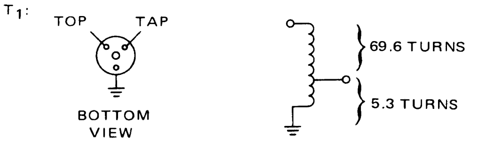
FIGURE 10 – PRINTED CIRCUIT LAYOUT OF MC1398P, MC1326, and MPSU 10 TRANSISTORS

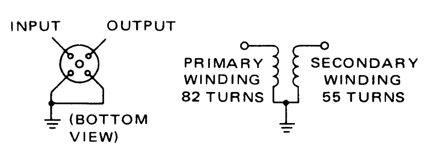


NOTES:
All resistors are 1/4 W unless otherwise noted.
(Copper Side Shown)





COILCRAFT FORM #10-32 OR EQUIV
UNIVERSAL AWG #36 WIRE OR EQUIV
L = 26 μH



COILCRAFT FORM #10-32 OR EQUIV
UNIVERSAL AWG #36 WIRE OR EQUIV
L_P = 12 μH primary winding
L_S = 8.8 μH secondary winding
K = 0.4

This coil data is intended as an aid only. It is expected that many designers will want to use other approaches.

MC1398P APPLICATIONS INFORMATION

MC1398P is a multifunction circuit with considerable gain associated with the chroma amplifier and oscillator sections. It is important to the circuit layout utilizing the MC1398P that the chroma amplifier, oscillator, and oscillator output/hue section grounds are separated from each other. Ground loop problems will interfere with oscillation stability and lock-up if this precaution is not observed.

Care must be exercised to avoid coupling from the oscillator output to the crystal circuitry connected to pin 8. Stray coupling of these two points can result in excessive oscillator shift; or in some cases, oscillator drop-out during adjustment of the hue control.

A suitable circuit layout for the MC1398P is shown in Figure 10.

An adjustable capacitor (1.5–20 pF in parallel with a fixed 22 pF capacitor) is shown in series with the 3.58 MHz crystal. This capacitor is used to adjust the oscillator exactly on frequency, and ensures excellent oscillator lock-up. However, acceptable oscillator performance can be obtained with a fixed value of capacitance (this value is dependent on the designers' choice of crystals).

8

MC1398P CIRCUIT DESCRIPTION

The MC1398P is capable of providing the entire color processing function between the second detector and the demodulator for television color receivers.

A band pass filter from the second detector provides a 50 mV (p-p) signal (for a saturated color bar pattern) at the input to the first chroma amplifier stage (Q_2, Q_3, Q_8, Q_9). Because of Q_2 emitter load resistor the input impedance is determined primarily by the bias resistor (R_3) and is about 2.3 kilohms. Since Q_2 is the current source for the differential pair (Q_3 and Q_9), the chroma information will pass to the load resistor (R_7) and then to the second chroma amplifier (Q_{17}). To avoid overload of Q_{17}, the maximum gain to Q_{17} base is only X3 and by varying the bias at the base of Q_9 it is possible to reduce the stage gain by 23 dB without signal distortion; the signal being "dumped" by Q_9 collector into the supply. Since this automatic chroma control action will vary the dc bias at Q_{17} base the emitter load of Q_{17} is the current source Q_{18}, maintaining the dc operating current. Q_{18} collector is bypassed externally to prevent ac signal attenuation.

During picture scan time, the chroma signal passes through the output level control amplifier (Q_{10}, Q_{11}, Q_{15}, Q_{21}). By changing the bias on Q_{11} and Q_{15} bases the signal can either pass to the output pin 2 or be "dumped" into the supply through Q_{11}. The use of buffer stages Q_{10} and Q_{21} prevent distortion at low-signal levels and the control range is better than 70 dB. The signal output is also buffered by Q_{14} and Q_{20}, thus providing a low impedance drive of up to 2.0 V (p-p) to the demodulator, with an overall gain between pins 5 and 2 of 40 dB. To enable the chroma signal output to reach the amplifiers from Q_{17} collector, Q_{12} is held in conduction by Q_5 which in the absence of any input on pin 4 is not conducting. This high collector voltage also holds Q_{26} in conduction, clamping the input to the burst channel and preventing chroma information reaching the oscillator. During picture retrace time, a positive-going 4.0 μs pulse from the line sweep transformer will turn Q_5 "on" and Q_7 "off". When Q_5 collector goes low, Q_{12} will become "cut-off" preventing the burst signal at Q_{17} collector from reaching the output pin 2. At the same time, Q_{26} turns "off" opening the burst channel. The high collector voltage of Q_7 turns on Q_{16} and Q_{22}. Q_{16} passes the burst signal from Q_{17} collector to the subcarrier regenerator and Q_{22} "fills-in" for Q_{12} during the gate period to prevent a dc shift in the pin 2 output voltage.

The gated burst signal is applied to the oscillator through Q_{27} and Q_{28}. Q_{29}, Q_{50} and Q_{35} together with Q_{27} and Q_{28} form an injection locked oscillator circuit. At series resonance of the crystal connected to pin 8 the impedance of pin 8 is very low, thereby reducing the 3.579545 MHz carrier level at the base of Q_{50}. The signal at the base of Q_{29} is not reduced but the output voltages in R_{33} and R_{42} will change. Any signals outside the response band of the crystal will appear equally at Q_{50} and Q_{29} bases and be suppressed in the output by the differential amplifier common-mode rejection ratio (about 40 dB). To maintain oscillation, a feedback signal with the correct phase is passed by Q_{35} back to the input of Q_{27}. Careful control of the resistor ratios ensures that Q_{29} and Q_{50} are operated linearly with about 350 mV (p-p) at R_{33} and R_{42}, due to self oscillation. A burst signal as low as 2.0 mV (p-p) at the chroma input is sufficient to cause the oscillator to lock to the reference phase and frequency.

As the burst amplitude increases, the level at Q_{29} and Q_{50} collectors changes and this shift is used to provide the automatic chroma control function. Q_{42} and Q_{45} form a modified differential amplifier and with zero offset bias Q_{45} conducts most of the current from Q_{43}. As an increasing burst level swings Q_{29} and Q_{50} collectors, the current from Q_{43} is shunted into Q_{42}. At a point predetermined by the setting of the automatic chroma control connected to pin 10, the composite lateral PNP of Q_{47} and Q_{46} will be biased into conduction. This amplifier has a gain of unity and a filter capacitor (connected to Q_{46} base) prevents any tendency to oscillations. Diode CR_9 provides thermal compensation to ensure a steady color-killer threshold point. The increasing current through Q_{13} emitter is used to control Q_9 base, attenuating the input signal as the burst amplitude increases. The current from Q_{13} also keeps Q_{19} in saturation. When the input signal becomes too small for satisfactory color rendition, Q_{13} current falls and Q_{19} comes out of saturation. This means Q_{25} will saturate, clamping Q_{21} base and "killing" the chroma output stage. R_{24} in the Schmitt trigger circuit ensures that the color-killer will have hysteresis to prevent fluttering between "on" and "off" states.

The oscillator output voltages at R_{33} and R_{42} are used to drive Q_{38} and Q_{39} into limiting so that as the burst amplitude increases the oscillator activity to around 700 mV (p-p), there will be no change in the oscillator output amplitude at pin 13. Q_{38} and Q_{39} are used as current sources with a 180° phase difference for the differential pairs Q_{30} and Q_{31}, Q_{34} and Q_{37}. A small capacitor attached externally to Q_{39} collector adjusts the total phase difference to 135°. Since the signal appearing in the load resistor R_{51} will be the vector sum of Q_{31} and Q_{37} signals, varying the base bias of Q_{30} and Q_{34} will change the oscillator output phase over the 135° range. Q_{40} and Q_{41} buffer the oscillator output providing a low impedance drive at pin 13 for the demodulator.

To minimize crosstalk between the burst and chroma channels, separate bias chains are used. Further, the oscillator bias chain is zener regulated to prevent phase shifts in the reference output with power-supply variations.

MC1446L

SENSE AMPLIFIER

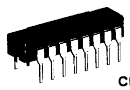
FOUR-CHANNEL LOW-THRESHOLD SENSE AMPLIFIER

. . . a sense amplifier designed to convert positive or negative 4.0 mV signals from plated-wire memories to transistor-transistor logic levels (MTTL). The problems encountered with ac-coupled plated-wire sense amplifiers are eliminated with this direct-coupled sense amplifier.

- Positive or Negative 4.0 mV Signal to Any of Four Input Channels Produces a Logic 1 or 0 Output
- Useful with the MCM7001 NMOS Memory
- Wired "OR" Capability at Amplifier Output Results in Fewer Associated Circuits
- 1 by 4 Internal Decoder Simplifies Channel Selection
- Fast Recovery Time from Overload Signals — 40 ns typ
- Good Isolation Between ON and OFF Channels
- Channel Select and Strobe Operate from Standard MTTL Levels

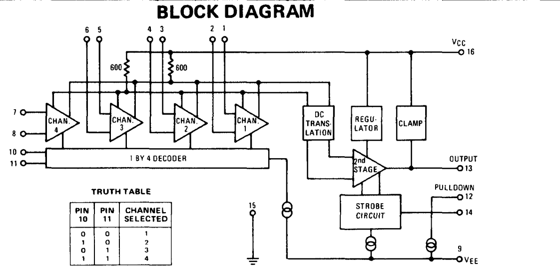
FOUR-CHANNEL LOW-THRESHOLD SENSE AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT

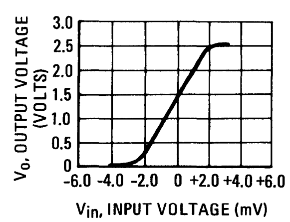


CERAMIC PACKAGE
CASE 620

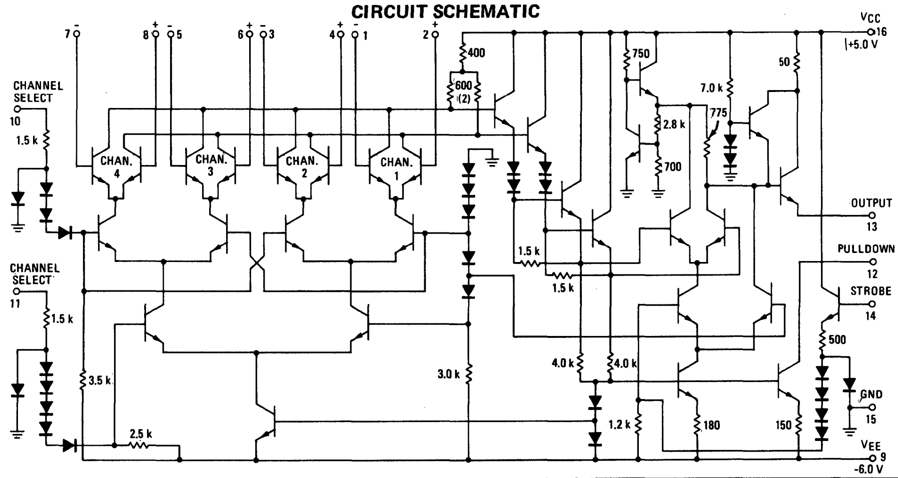
BLOCK DIAGRAM



TRANSFER CHARACTERISTICS



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+10 -10	Vdc
Differential Input Voltage	V_{ID}	±5.0	Volts
Common-Mode Input Voltage	V_{IC}	±5.0	Volts
Output Current	I_O	25	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 575 3.85	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc ±1%, V_{EE} = -6.0 Vdc ±1%, T_A = +25°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Voltage Gain	1	A_V	–	600	–	–
Output Voltage Level e_{in} = 0 T_A = 0°C to +75°C e_{in} = +4.0 mV e_{in} = -4.0 mV	2	V_O	 0.4 2.0 –	 1.4 – –	 2.4 – 0.4	Vdc
Input Bias Current	3	I_{IB}	–	15	60	µA
Input Offset Current	3	I_{IO}	–	0.1	4.0	µA
Channel Select Current High Level Low Level	4	 I_{CH} I_{CL}	 – –	 1.7 0.5	 2.6 1.0	mA
Channel Select Voltage High Level Low Level	5	 V_{CH} V_{CL}	 2.0 –	 – –	 – 0.8	Volts
Strobe Voltage High Level Low Level	5	 V_{SH} V_{SL}	 2.0 –	 – –	 – 0.8	Volts
Strobe Input Current	4	I_S	–	30	150	µA
Output Source Current	6	I_{O+}	4.0	8.0	–	mA
Output Sink Current	6	I_{O-}	-2.5	-4.0	–	mA
Positive Supply Current	6	I_{CC}	–	19	27	mA
Negative Supply Current	6	I_{EE}	–	-17	-24	mA
Input Common-Mode Voltage Range Channel Selected Channels Not Selected	7	V_{ICR}	 – – – –	 +2.7 -1.0 +2.7 -6.0	 – – – –	Volts
Input Differential-Mode Voltage Range Channel Selected Channels Not Selected	7	V_{IDR}	 – –	 ±0.5 ±2.0	 – –	Volts

SWITCHING CHARACTERISTICS

Propagation Delay Time	8	t_{PHL}	–	14	–	ns
Output Rise or Fall Time	8	t_{TLH}, t_{THL}	–	30	–	ns
Strobe Delay Time	9	t_{dS}	–	14	–	ns
Strobe Width (Min)	9	$t_{S(min)}$	–	20	–	ns
Channel Select Time	10	t_{Csel}	–	14	–	ns
Common-Mode Recovery Time (channel selected)	7	t_{CMR}	–	60	–	ns
Differential-Mode Recovery Time (channel selected)	8	t_{DMR}	–	40	–	ns

8

TEST CIRCUITS

FIGURE 1 – VOLTAGE GAIN

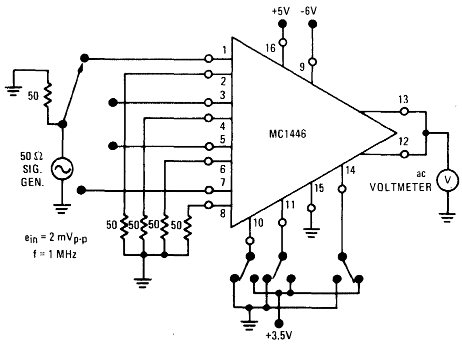


FIGURE 2 – OUTPUT DC LEVELS

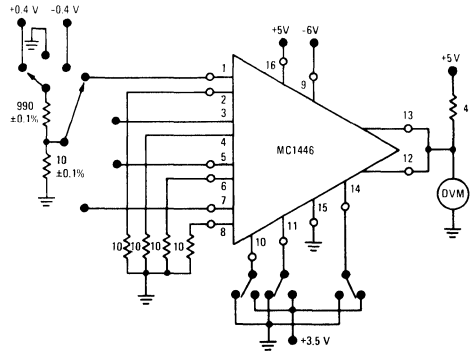


FIGURE 3 – INPUT CURRENTS

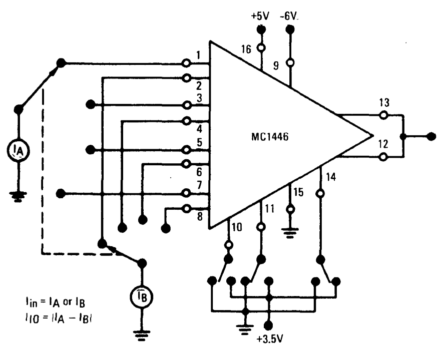


FIGURE 4 – CHANNEL SELECT AND STROBE INPUT CURRENTS

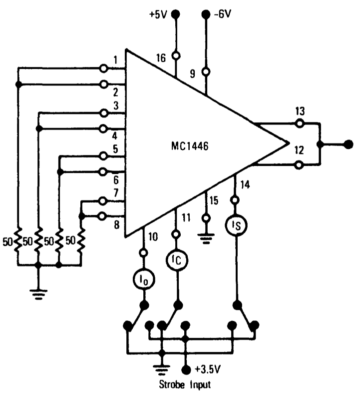


FIGURE 5 – CHANNEL SELECT TRANSFER CHARACTERISTICS

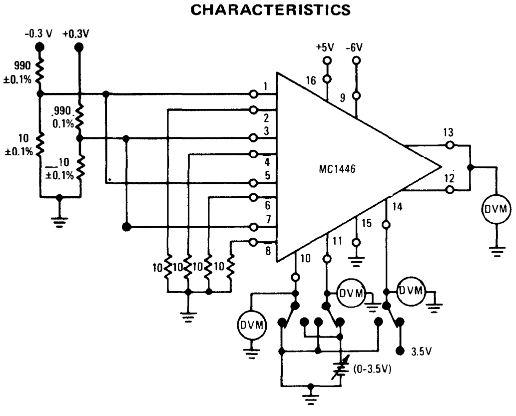


FIGURE 6 – OUTPUT CURRENTS

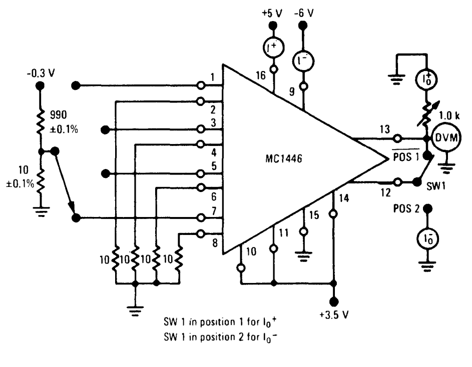


FIGURE 7 — INPUT COMMON-MODE CHARACTERISTICS

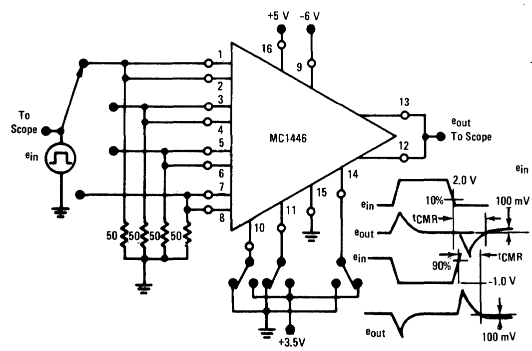


FIGURE 8 — CIRCUIT PROPAGATION DELAY, OUTPUT RISE AND FALL TIMES, AND DIFFERENTIAL-MODE RECOVERY TIME

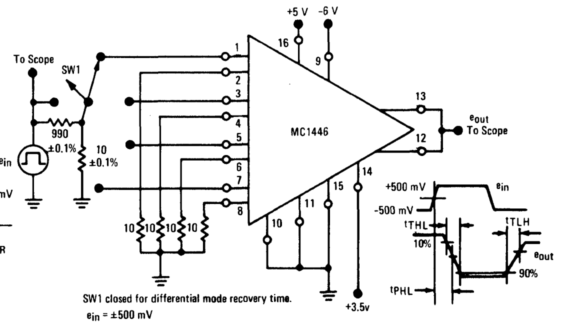


FIGURE 9 — STROBE CHARACTERISTICS

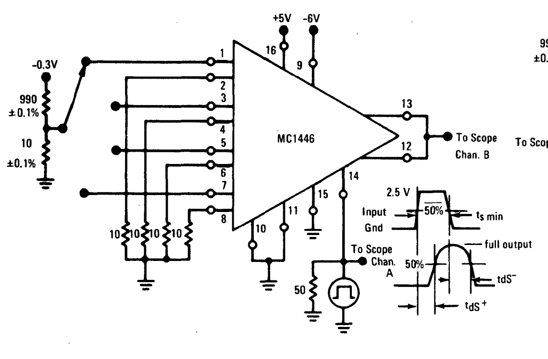
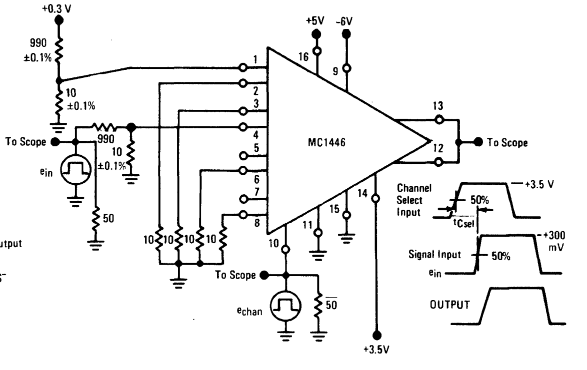


FIGURE 10 — CHANNEL SELECT TIME



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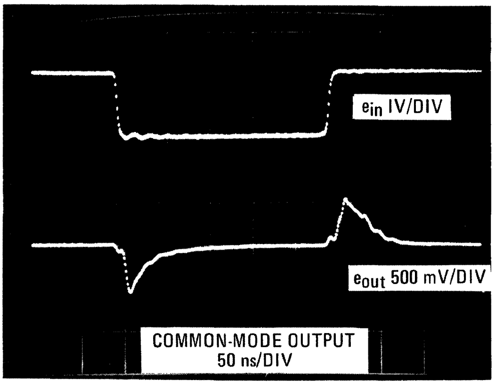
TYPICAL RECOVERY TIME WAVEFORMS

FIGURE 11 – COMMON-MODE RECOVERY TIME



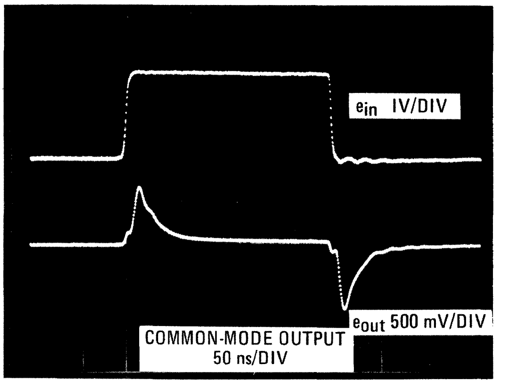
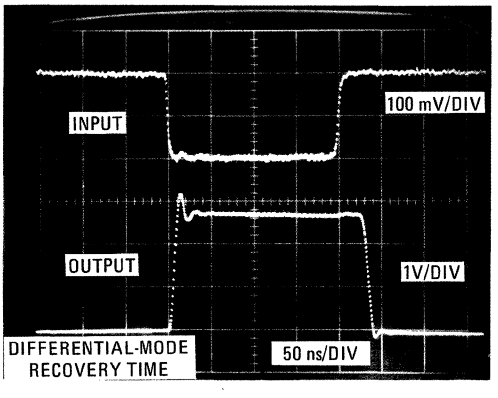
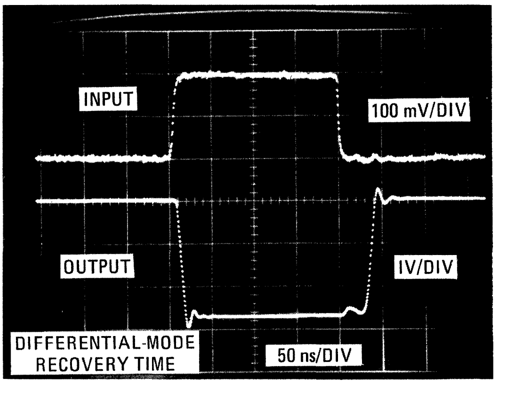


FIGURE 12 – DIFFERENTIAL-MODE RECOVERY TIME





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TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted)

FIGURE 13 – VOLTAGE GAIN versus TEMPERATURE

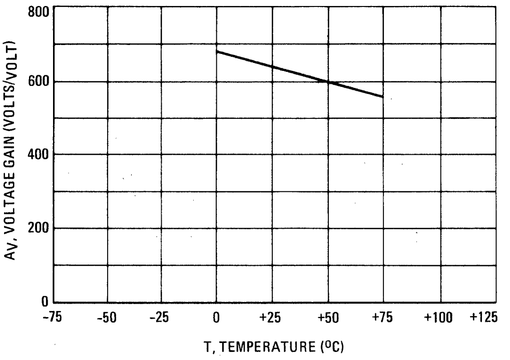


FIGURE 14 – DC OUTPUT VOLTAGE LEVEL versus TEMPERATURE (All Inputs Grounded)

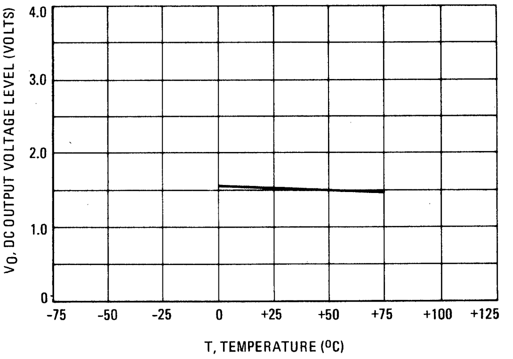


FIGURE 15 – AMPLIFIER TRANSFER CHARACTERISTICS

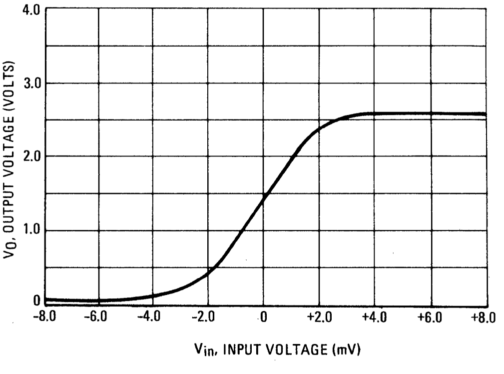


FIGURE 16 – CHANNEL SELECT versus OUTPUT TRANSFER CHARACTERISTICS

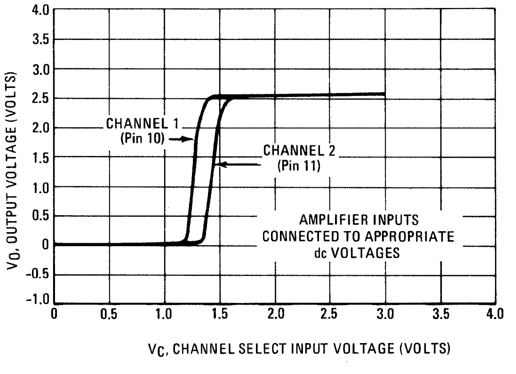


FIGURE 17 – STROBE INPUT TRANSFER CHARACTERISTICS (Input High)

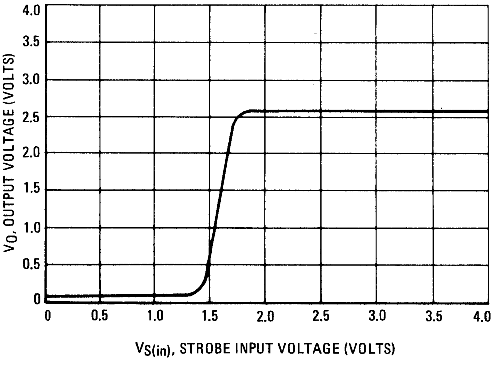
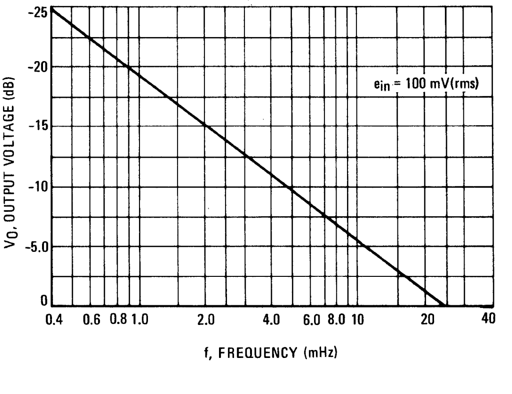


FIGURE 18 – COMMON-MODE GAIN versus FREQUENCY



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TYPICAL CHARACTERISTICS (continued)

FIGURE 19 — VOLTAGE GAIN versus FREQUENCY

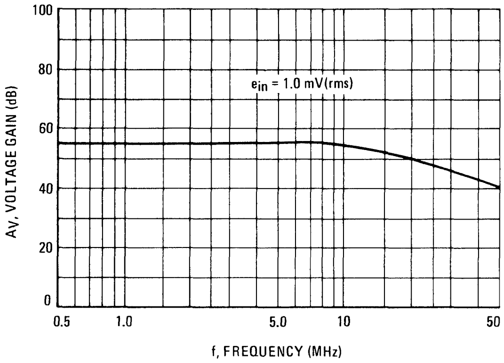
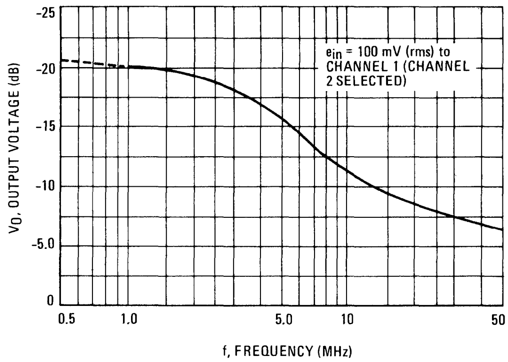


FIGURE 20 — ADJACENT CHANNEL ISOLATION versus FREQUENCY



CIRCUIT DESCRIPTION

The MC1446L is designed to translate a positive 4.0 mV signal from a plated wire memory to an MTTL "1" level, or a negative 4.0 mV to an MTTL "0" level. This sense amplifier also eliminates the requirement for a bipolar switch in series with the plated wire because the bit selection is done inside the sense amplifier.

The circuit operation can be described in sections as follows:

1. All channels have been designed for low input offsets — 0.5 V typical.
2. Channel "ORing" is accomplished by using common collector load resistors for four differential amplifier pairs.
3. Channel selection is accomplished by current steering through the four differential pairs. The circuit below the four differential pairs forms a matrix tree which can be thought of as a 1-by-4 decode matrix. The bottom transistor is the current source for the first stage of gain.
4. DC translation between the first and second stages of gain is done through an emitter-follower stage, two diodes and another emitter follower for each side of the differential amplifier. The currents in these translator legs are combined and run through diodes to the negative supply. These diodes are used to bias both the first and second gain stages. This also gives the appropriate gain versus temperature and dc output level versus temperature characteristics.
5. The top of the second stage amplifier is regulated at a voltage equal to five diode drops above ground. It can be seen that if the 700 ohm resistor in the regulator has one diode (or V_{BE}) across it then the 2.8 k ohm resistor will have four diode drops across it. This makes a five diode drop voltage above ground that is fairly independent of the positive supply.
6. The current in the second stage of the amplifier is set by the 180-ohm resistor in the emitter of the current source. It can be seen that this resistor has one diode drop (approximately 750 mV) across it. Therefore, an analysis will show that the voltage drop across the 775-ohm load resistor in the second stage will be approximately two diodes when the differential amplifier is balanced. Accounting for the additional diode voltage drop of the emitter-follower output transistor will set the output dc level at two diodes above ground or very near the center of MTTL threshold.
7. The strobe circuit works by steering current in the second stage. When the strobe is low, the entire current of the second stage current source is steered through the 775-ohm load resistor. This clamps the output to a low state so that an input signal cannot cause an output. When the strobe is high, the current is steered through the second stage differential amplifier pair and the output will go to a level dictated by the presence of an input signal.
8. The output circuit of the sense amplifier may be thought of as a push-pull type. The emitter of the push transistor is brought out to a separate pin from the collector of the pull transistor. This will facilitate "Wire ORing" the outputs of several sense amplifiers. Several emitter outputs can be wired together along with only one collector pull-down transistor. The unused collectors of the pulldown transistor must be grounded. An example of the use of "Wire ORing" is to have four MC1446 devices wired-OR into a 16-channel sense amplifier in which a channel may be selected by selecting channels in parallel at the amplifier inputs and strobing the proper sense amplifier.

APPLICATIONS INFORMATION

The MC1446 is designed to convert signals as small as positive or negative 4.0 mV to MTTL logic levels. The output level of the sense amplifier with no input signal present and with the strobe high is typically 1.4 volts (typical input threshold of MTTL logic). Hence, if the strobe goes high during the absence of an input signal from the plated-wire memory, the sense amplifier output will rise to 1.4 volts. This condition could cause false outputs; therefore careful considerations must be given to strobe timing. Figure 21 illustrates a typical timing sequence of the MC1446 device as recommended for proper operation.

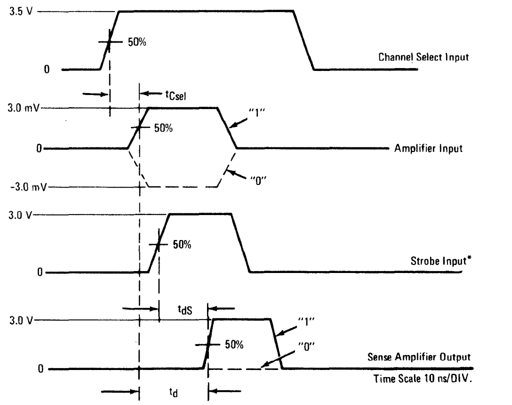
Figure 22 shows how these sense amplifiers are used in an N-word-line-by-32-bit basic memory plane organized as 4-N words of 8 bits each. During a read cycle, the read current is pulsed through a selected word-line and thus generates outputs to all of the 32-bit positions in the line. The internal one-of-four decoder selects the desired channels of the eight sense amplifiers for a particular system word. When the strobe goes high, the sense amplifier outputs switch according to the data present at the amplifier inputs. The data readout on the other 24-bit lines is not lost due to the Non-Destructive Read-Out properties of a plated-wire memory. On the next read cycle the decoder of the sense amplifier in combination with the selected word-line determines the 8-bits of data to read.

APPLICATIONS INFORMATION (continued)

Memory organizations that have more than four words per word-line require that the sense amplifier outputs be wire-ORed. To wire-OR the outputs of several sense amplifiers all of the emitters of the output-pullup transistors are tied together. Only one collector of the pulldown transistors is tied to the wire-ORed emitters of the pullup transistors. The remaining pulldown transistors must be grounded as noted in Figure 23. Ten or more sense amplifiers may be wire-ORed together without any reduction in usable logic levels since only one sense amplifier per bit is on at any given time. Variations in propagation delay time (t_{pd}), versus the number of wire-ORed sense amplifiers and the output capacitance are given in Figure 24.

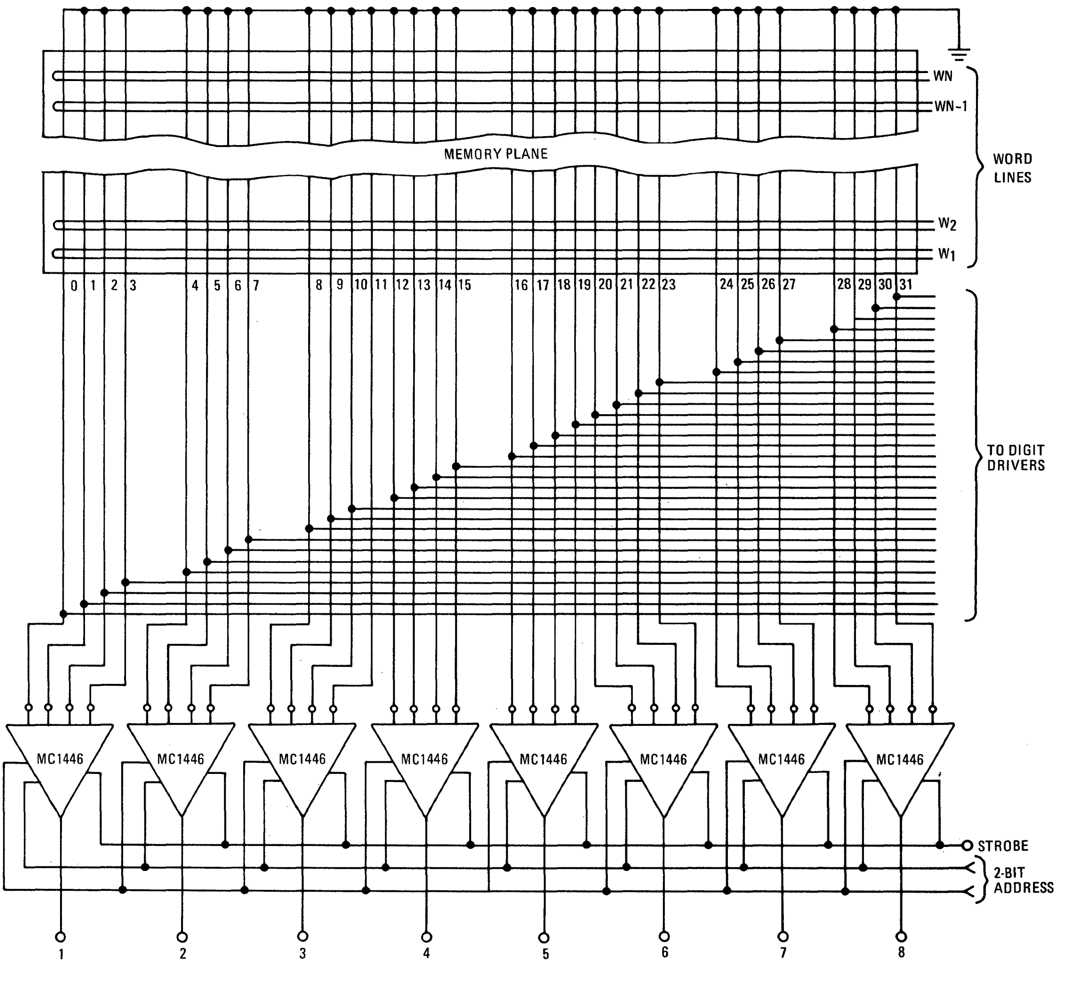
The fast propagation delay time and low threshold of the MC1446 make it useful as the sense amplifier for the MCM7001 N-channel MOS memory. The data output of the MCM7001 is referenced around +7.5 volts; thus the power supply inputs of the MC1446, as well as the MECL-level Channel Select and Strobe inputs, are translated to MTTL and then referenced around this level, as shown in Figure 25. The minimum 200 μA current from the memory generates an input of 20 mV, which is easily detected by the MC1446. The MC1446 otuput is a TTL-level signal with a +7.5 volt reference. This signal can be translated back to MECL levels with a zener diode as shown.

FIGURE 21 – TYPICAL TIMING SEQUENCE



*The strobe pulse width is smaller than the amplifier input pulse width.

FIGURE 22 – N-WORD-LINE-BY-32-BIT MEMORY PLANE ORGANIZED AS 4-N WORDS OF 8 BITS EACH



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APPLICATIONS INFORMATION (continued)

FIGURE 23 – WIRED "OR" MC1446 DEVICES

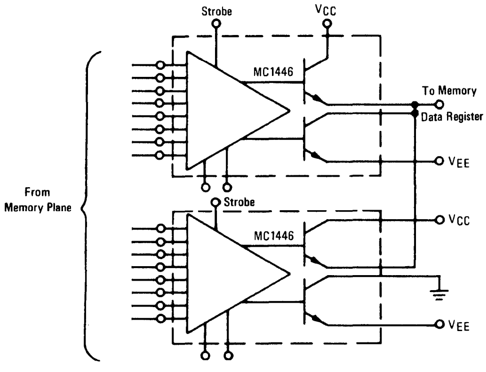


FIGURE 24 – TYPICAL PROPAGATION DELAY TIME VARIATION
(per number of devices at stated capacitance)

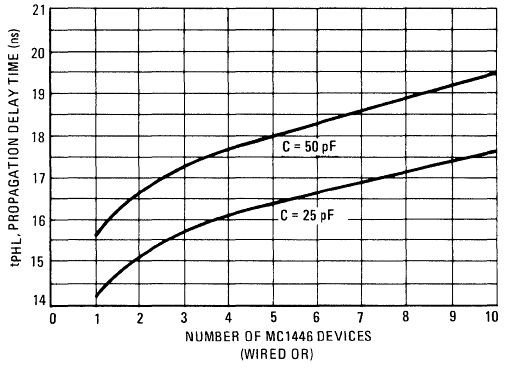
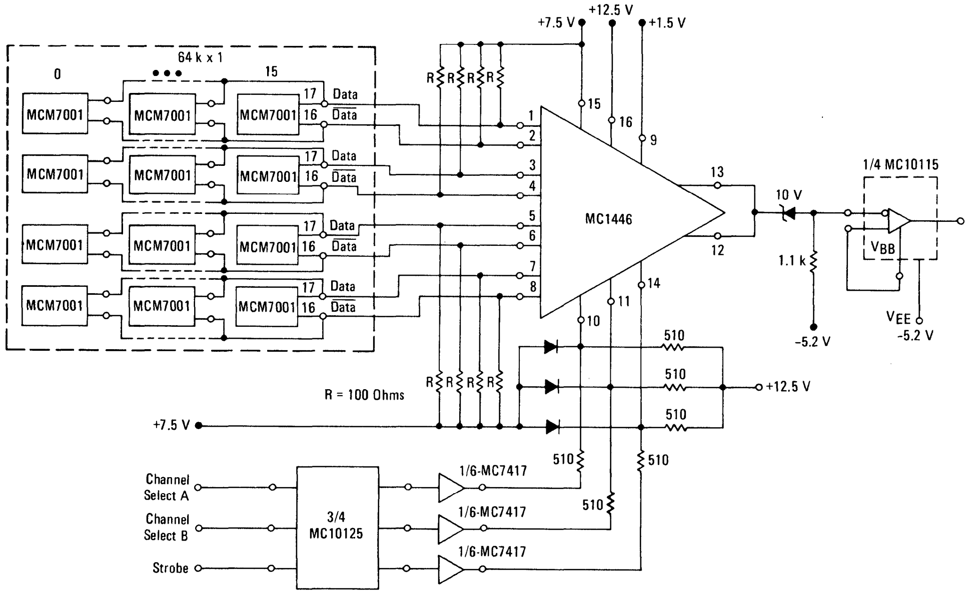


FIGURE 25 – SENSE AMPLIFIER FOR MCM7001 MEMORY



DEFINITIONS

A_V	the voltage gain from a channel input to amplifier output (input signal is 2 mV peak-to-peak and the strobe is high)
CMV_{in}	maximum input common-mode voltage on any channel that will not cause the amplifier to saturate
DMV_{in}	maximum input differential-mode voltage on any channel signal that will not saturate the amplifier
I_{CC}	current from the positive supply with no load (pin 12 shorted to pin 13)
I_{EE}	current into the negative supply with both channel select pins at +3.5 volts
I_{IB}	input current into the base of any input transistor when the opposite transistor of the differential pair is at the same voltage
I_{CH}	input current at channel select pin when the channel select voltage is at V_{CH}
I_{CL}	input current at channel select pin when the channel select voltage is at V_{CL}
I_{IO}	difference between base currents of any input differential pair of transistors
I_{O+}	output source current to a load with the output remaining above 2.4 volts, excluding the amplifier's own sink current
I_{O-}	the current that the amplifier will sink into pin 12
t_{CMR}	time required for the amplifier to recover from the maximum specified common-mode input, (recovery – output within 10% of its quiescent state)
$t_{C\,sel}$	time between the 50% point of the channel gate input and the 50% point of the signal input that still allows a full width signal at the amplifier output
t_{DMR}	time required for the amplifier to recover from maximum specified differential-mode input, (recovery – output within 10% of its quiescent state)
t_{dS}	delay time from the 50% point of the strobe input leading or trailing edge to the corresponding 50% point of the output
t_{PHL}	the delay time from the 50% point of a 5.0 mV input leading edge to the 50% point of the amplifier output
t_{THL}, t_{TLH}	time between 10% and 90% points of the output signal with a 5.0 mV input signal
t_{Smin}	minimum pulse width at 50% points at strobe input allows a full output (pulse rise times of less than 10 ns, amplifier differential input equal to 3 mV)
V_{CH}	minimum voltage required at the channel select pin to cause a given channel to give 99% of the maximum gain through the amplifier
V_{CL}	maximum voltage allowable at the channel select pin to cause a given channel to give 1% or less of the gain when channel is fully selected
V_O	output dc level with inputs grounded and strobe high
V_{OH}	minimum output high level
V_{OL}	maximum output low level
V_{SH}	the minimum voltage required at the strobe pin to allow 99% of a full output
V_{SL}	the maximum voltage allowable at the strobe pin to allow 1% or less of a full output

8

MC1488L

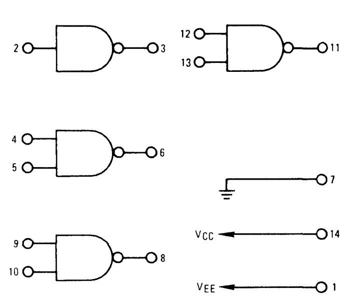
QUAD LINE DRIVER

The MC1488L is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

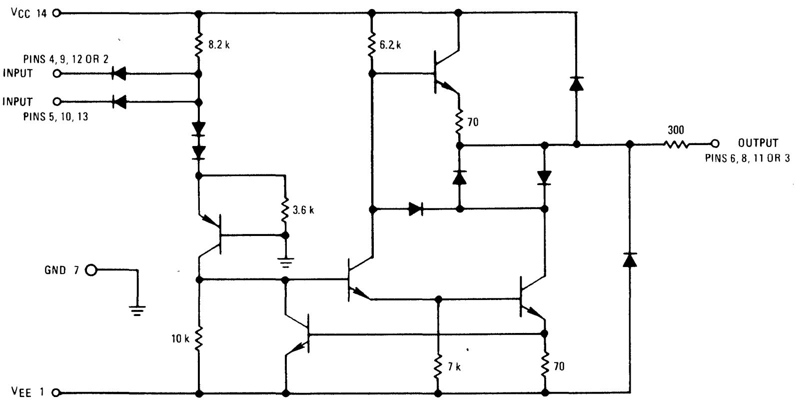
Features:

- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

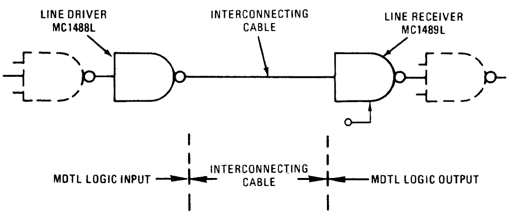
QUAD MDTL LINE DRIVER
RS-232C
MONOLITHIC SILICON
INTEGRATED CIRCUIT

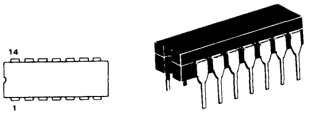


CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



TYPICAL APPLICATION





CERAMIC PACKAGE
CASE 632
TO-116

See Packaging Information Section for outline dimensions.

8

Maximum Rating (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 -15	Vdc
Input Signal Voltage	V_{in}	$-15 \leq V_{in} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, Ceramic Dual-In-Line Package) Derate above T_A = +25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +9.0 ± 1% Vdc, V_{EE} = -9.0 ± 1% Vdc, T_A = 0 to +75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Forward Input Current (V_{in} = 0 Vdc)	1	I_F	–	1.0	1.6	mA
Reverse Input Current (V_{in} = +5.0 Vdc)	1	I_R	–	–	10	μA
Output Voltage High	2	V_{OH}				Vdc
(V_{in} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = -9.0 Vdc)			+6.0	+7.0	–	
(V_{in} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = -13.2 Vdc)			+9.0	+10.5	–	
Output Voltage Low	2	V_{OL}				Vdc
(V_{in} = 1.0 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = -9.0 Vdc)			-6.0	-7.0	–	
(V_{in} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = -13.2 Vdc)			-9.0	-10.5	–	
Positive Output Short-Circuit Current	3	I_{SC+}	+6.0	+10	+12	mA
Negative Output Short-Circuit Current	3	I_{SC-}	-6.0	-10	-12	mA
Output Resistance ($V_{CC} = V_{EE} = 0$, $\|V_O\| = \pm 2.0$ V)	4	R_O	300	–	–	Ohms
Positive Supply Current ($R_l = \infty$)	5	I_{CC}				mA
(V_{in} = 1.9 Vdc, V_{CC} = +9.0 Vdc)			–	+15	+20	
(V_{in} = 0.8 Vdc, V_{CC} = +9.0 Vdc)			–	+4.5	+6.0	
(V_{in} = 1.9 Vdc, V_{CC} = +12 Vdc)			–	+19	+25	
(V_{in} = 0.8 Vdc, V_{CC} = +12 Vdc)			–	+5.5	+7.0	
(V_{in} = 1.9 Vdc, V_{CC} = +15 Vdc)			–	–	+34	
(V_{in} = 0.8 Vdc, V_{CC} = +15 Vdc)			–	–	+12	
Negative Supply Current ($R_L = \infty$)	5	I_{EE}				
(V_{in} = 1.9 Vdc, V_{EE} = -9.0 Vdc)			–	-13	-17	mA
(V_{in} = 0.8 Vdc, V_{EE} = -9.0 Vdc)			–	–	-15	μA
(V_{in} = 1.9 Vdc, V_{EE} = -12 Vdc)			–	-18	-23	mA
(V_{in} = 0.8 Vdc, V_{EE} = -12 Vdc)			–	–	-15	μA
(V_{in} = 1.9 Vdc, V_{EE} = -15 Vdc)			–	–	-34	mA
(V_{in} = 0.8 Vdc, V_{EE} = -15 Vdc)			–	–	-2.5	mA
Power Dissipation		P_D				mW
(V_{CC} = 9.0 Vdc, V_{EE} = -9.0 Vdc)			–	–	333	
(V_{CC} = 12 Vdc, V_{EE} = -12 Vdc)			–	–	576	

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ± 1% Vdc, V_{EE} = -9.0 ± 1% Vdc, T_A = +25°C.)

Propagation Delay Time (z_l = 3.0 k and 15 pF)	6	t_{PLH}	–	275	350	ns
Fall Time (z_l = 3.0 k and 15 pF)	6	t_{THL}	–	45	75	ns
Propagation Delay Time (z_l = 3.0 k and 15 pF)	6	t_{PHL}	–	110	175	ns
Rise Time (z_l = 3.0 k and 15 pF)	6	t_{TLH}	–	55	100	ns

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CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

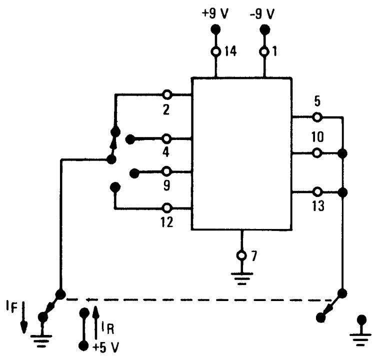


FIGURE 2 – OUTPUT VOLTAGE

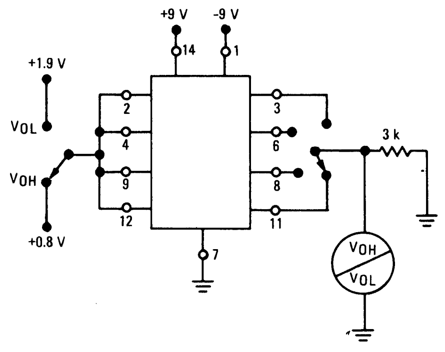


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

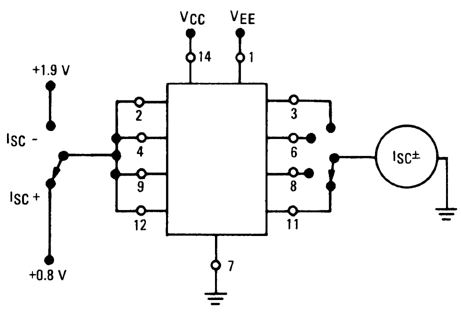


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

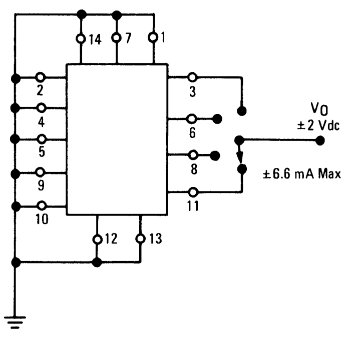


FIGURE 5 – POWER-SUPPLY CURRENTS

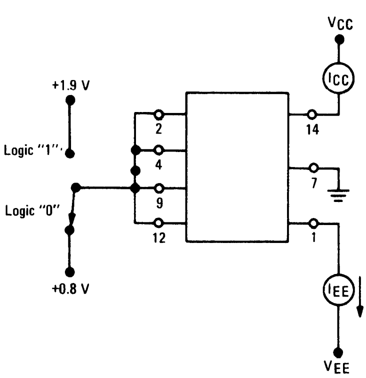
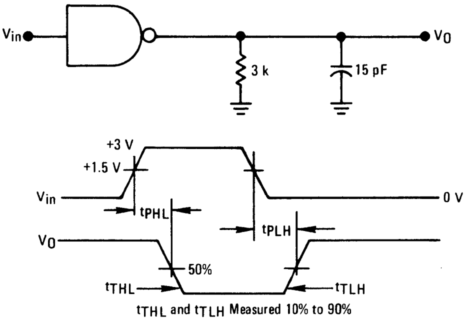


FIGURE 6 – SWITCHING RESPONSE



8

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE

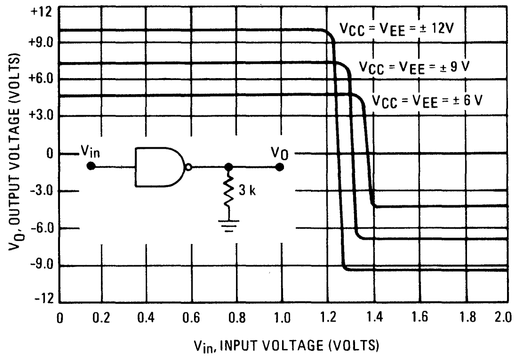


FIGURE 8 – SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE

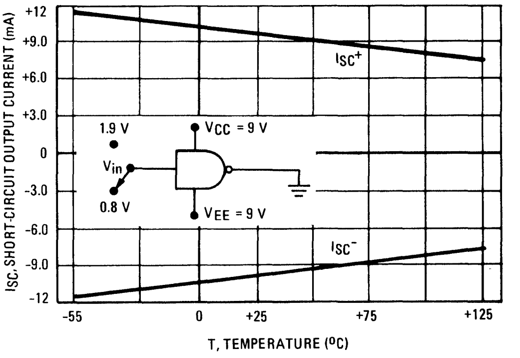


FIGURE 9 – OUTPUT SLEW RATE versus LOAD CAPACITANCE

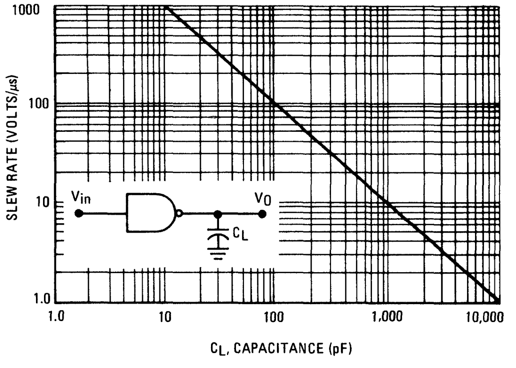


FIGURE 10 – OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

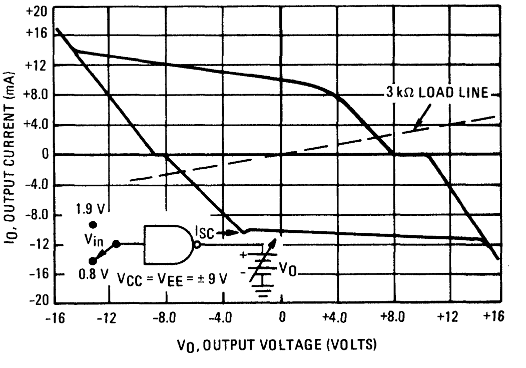
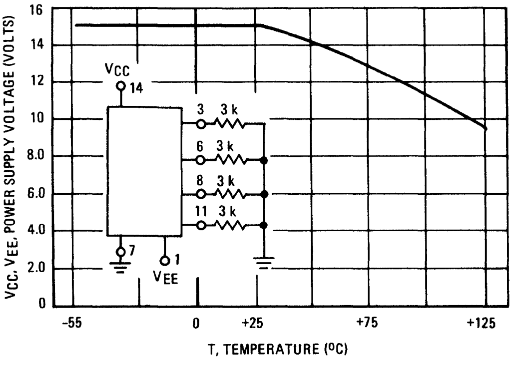


FIGURE 11 – MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



8

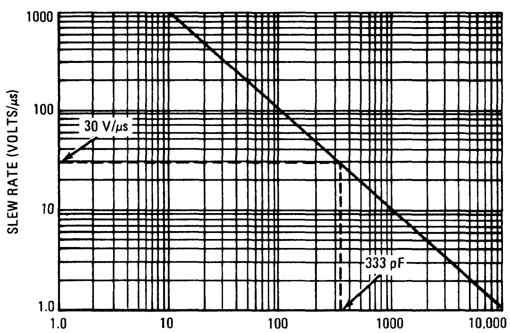
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488L quad driver and its companion circuit, the MC1489L quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488L meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

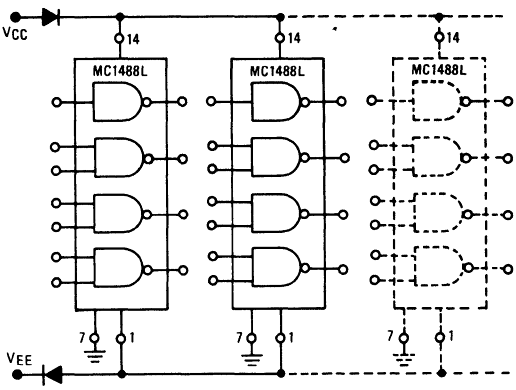
The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488L is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{SC} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488L is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geqslant 9.0$ V; $V_{EE} \leqslant -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488L effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488L to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488L to withstand faults with power-supplies of less than the 9.0 volts stated above.

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488L is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488L used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power-Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488L will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

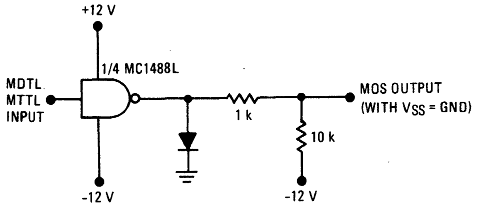
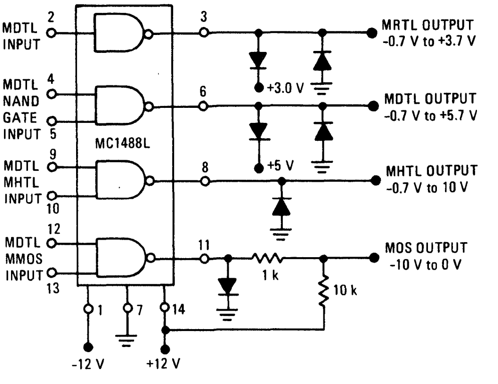


FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS



8

LINEAR/DIGITAL INTERFACE CIRCUITS

MC1489L
MC1489AL

QUAD LINE RECEIVERS

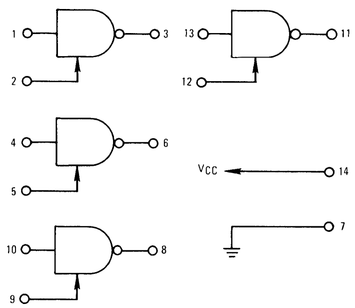
The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

- Input Resistance – 3.0 k to 7.0 kilohms
- Input Signal Range – ± 30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  a) Logic Threshold Shifting
  b) Input Noise Filtering

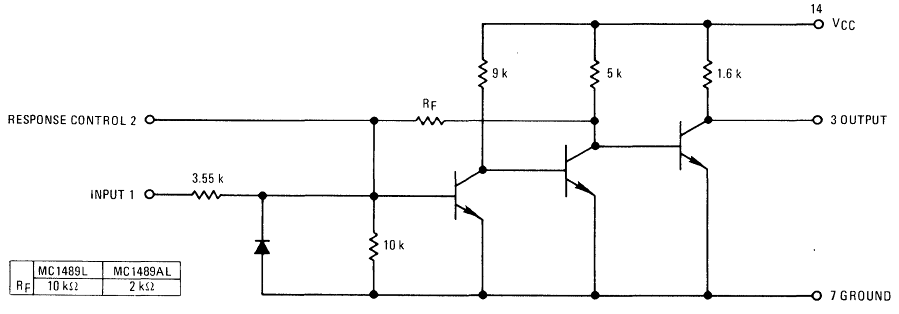
QUAD MDTL
LINE RECEIVERS
RS-232C

INTEGRATED CIRCUIT

LOGIC DIAGRAM

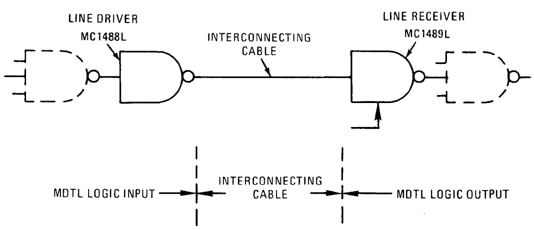


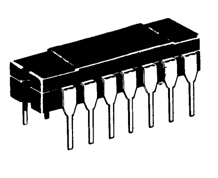
CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



	MC1489L	MC1489AL
RF	10 kΩ	2 kΩ

TYPICAL APPLICATION





CERAMIC PACKAGE
CASE 632
TO-116

See Packaging Information Section for outline dimensions.

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Signal Range	V_{in}	±30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic Dual In-Line Package) Derate above T_A = +25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = +5.0 Vdc ±1%, T_A = 0 to +75°C unless otherwise noted)

Characteristics		Figure	Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{in} = +25 Vdc) (V_{in} = +3.0 Vdc)	1	I_{IH}	3.6 0.43	– –	8.3 –	mA
Negative Input Current	(V_{in} = -25 Vdc) (V_{in} = -3.0 Vdc)	1	I_{IL}	-3.6 -0.43	– –	-8.3 –	mA
Input Turn-On Threshold Voltage (T_A = +25°C, V_{OL} ≤ 0.45 V)	MC1489L MC1489AL	2	V_{IH}	1.0 1.75	– 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage (T_A = +25°C, V_{OH} ≥ 2.5 V, I_L = -0.5 mA)	MC1489L MC1489AL	2	V_{IL}	0.75 0.75	– 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{in} = 0.75 V, I_L = -0.5 mA) (Input Open Circuit, I_L = -0.5 mA)	2	V_{OH}	2.6 2.6	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{in} = 3.0 V, I_L = 10 mA)	2	V_{OL}	–	0.2	0.45	Vdc
Output Short-Circuit Current		3	I_{SC}	–	3.0	–	mA
Power Supply Current	(V_{in} = +5.0 Vdc)	4	I^+	–	20	26	mA
Power Dissipation	(V_{in} = +5.0 Vdc)	4	P_D	–	100	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 1%, T_A = +25°C)

Propagation Delay Time	(R_L = 3.9 kΩ)	5	t_{PLH}	–	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	5	t_r	–	120	175	ns
Propagation Delay Time	(R_L = 390 Ω)	5	t_{PHL}	–	25	50	ns
Fall Time	(R_L = 390 Ω)	5	t_f	–	10	20	ns

TEST CIRCUITS

FIGURE 1 – INPUT CURRENT

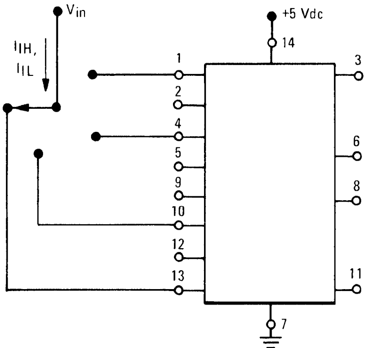


FIGURE 2 – OUTPUT VOLTAGE and INPUT THRESHOLD VOLTAGE

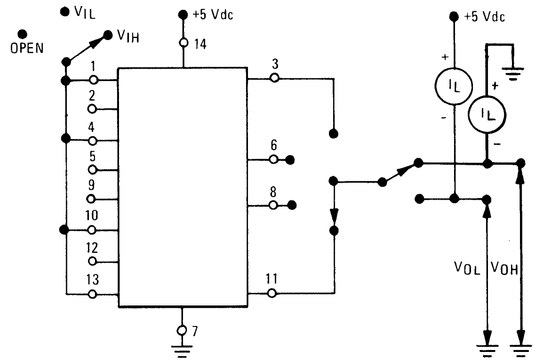


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

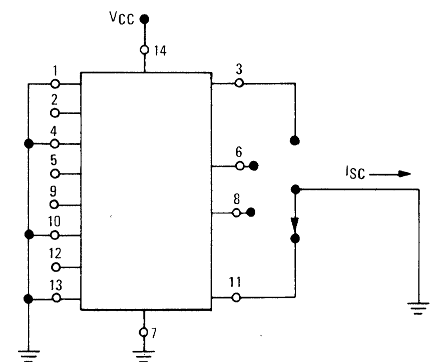


FIGURE 4 – POWER-SUPPLY CURRENT

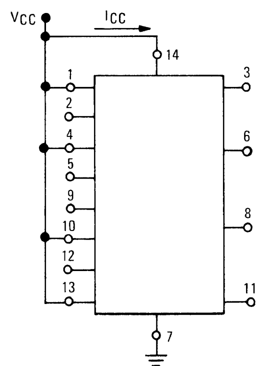
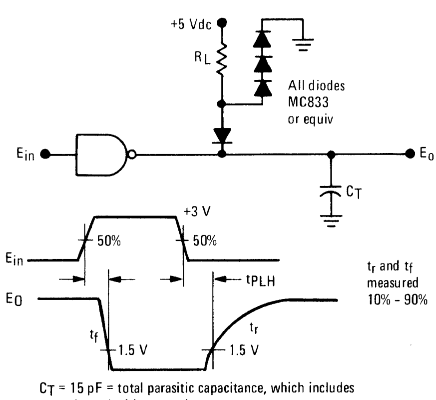
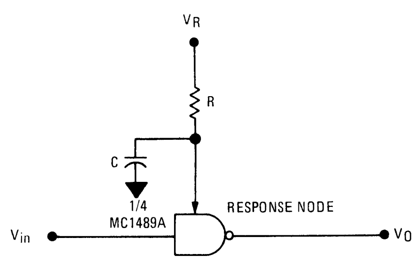


FIGURE 5 – SWITCHING RESPONSE



C_T = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances

FIGURE 6 – RESPONSE CONTROL NODE



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

8

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 7 – INPUT CURRENT

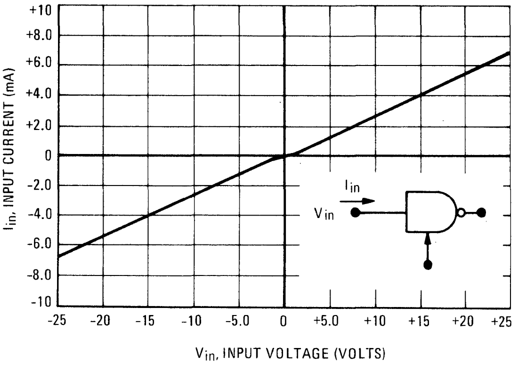


FIGURE 8 – MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

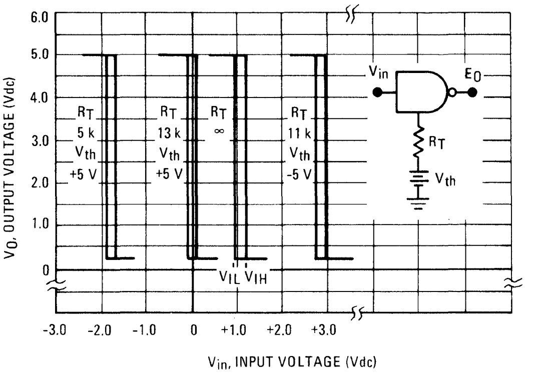


FIGURE 9 – MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

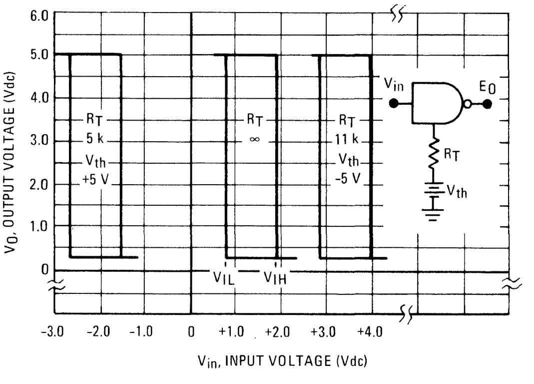


FIGURE 10 – INPUT THRESHOLD VOLTAGE versus TEMPERATURE

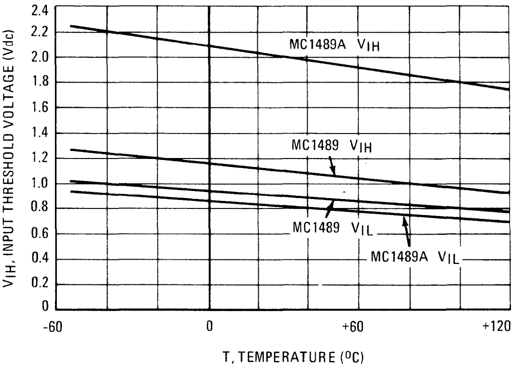
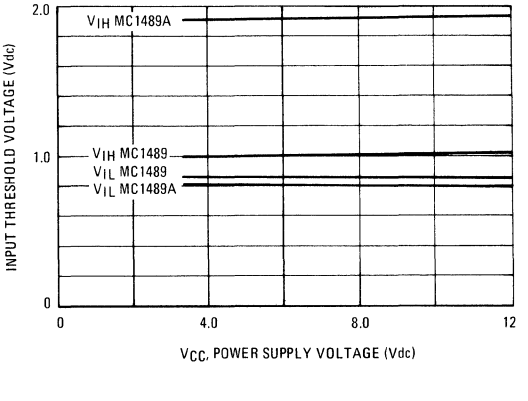


FIGURE 11 – INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



8

APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488L quad driver and its companion circuit, the MC1489L quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE} (Ref. Sect. 2.4).

The receiver shall detect a voltage between -3.0 and -25 volts as a logic "1" and inputs between +3.0 and +25 volts as a logic "0" (Ref. Sect. 2.3). On some interchange leads, an open circuit or power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or logic "1" (Ref. Sect. 2.5). For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489L input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489AL has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 6, 8 and 9 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 12 and 13 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 14)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 15 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

FIGURE 12 – TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

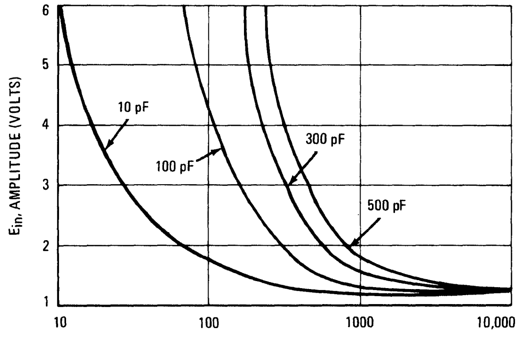
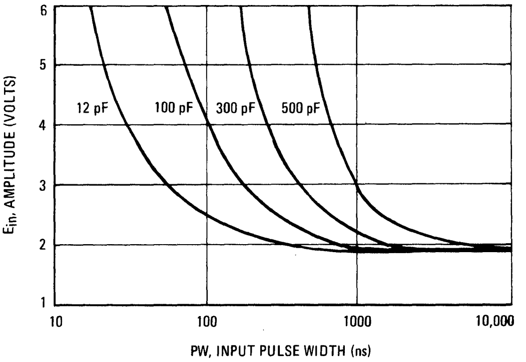


FIGURE 13 – TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



APPLICATIONS INFORMATION (continued)

FIGURE 14 – TYPICAL TRANSLATOR APPLICATION – MOS TO DTL OR TTL

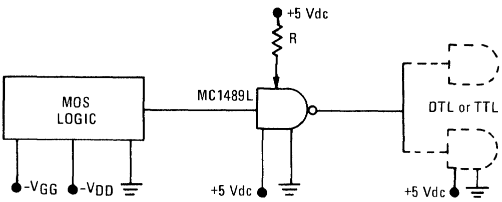
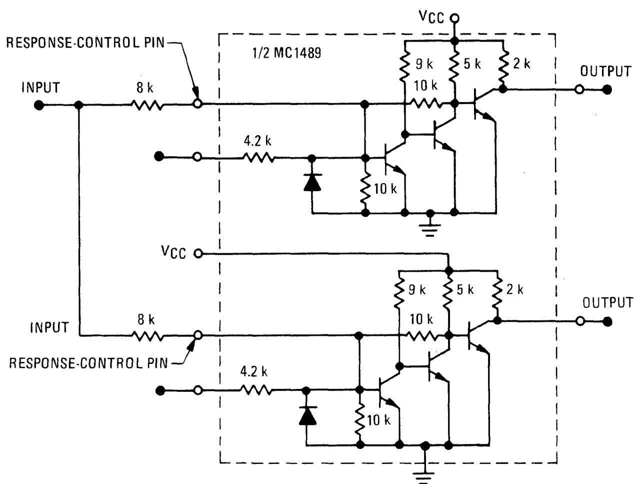


FIGURE 15 – TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C



D-TO-A CONVERTER

MC1506L
MC1406L

Specifications and Applications Information

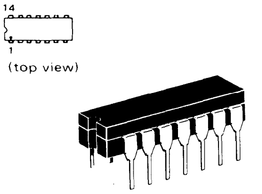
MONOLITHIC SIX BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of a six-bit digital word and an analog input voltage.

- Digital Inputs are MDTL and MTTL Compatible
- Relative Accuracy – ±0.78% Error maximum
- Low Power Dissipation – 85 mW typical @ ±5.0 V
- Adjustable Output Current Scaling
- Fast Settling Time – 150 ns typical
- Standard Supply Voltage: +5.0 V and -5.0 V to -15 V

SIX BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

MONOLITHIC SILICON INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 – OUTPUT CURRENT SETTLING TIME (ALL BITS SWITCHED, R_L = 50 Ω)

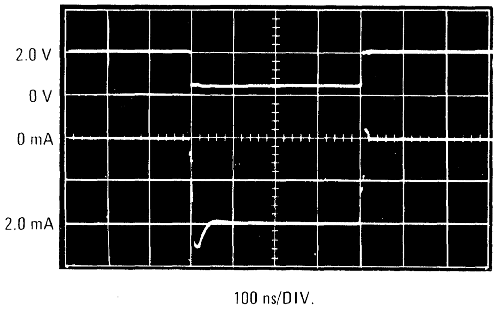
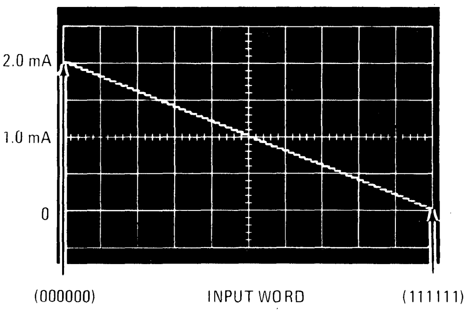


FIGURE 2 – D-to-A TRANSFER CHARACTERISTICS



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- Digital-to-Analog Meter Readout
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- Digital Varicap Tuning
- Video Systems
- Stepping Motor Drive
- CRT Character Generation
- Digital Addition and Subtraction
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Programmable Power Supplies
- Speech Encoding

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{10}	+8.0, V_{EE}	Vdc
Applied Output Voltage	V_O	±5.0	Vdc
Reference Current	I_{12}	5.0	mA
Reference Amplifier Inputs	V_{12}, V_{13}	V_{CC}, V_{EE}	Vdc
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 1000 6.7	 mW mW/°C
Operating Temperature Range MC1506L MC1406L	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R12}$ = 2.0 mA, $T_A = T_{low}$* to T_{high}* unless otherwise noted. All digital inputs at low logic levels.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O)	10	E_r	–	–	±0.78	%
Settling Time (within 1/2 LSB [includes t_d] T_A = +25°C)	9	t_S	–	150	300	ns
Propagation Delay Time T_A = +25°C	9	t_{PHL}, t_{PLH}	–	10	50	ns
Output Full Scale Current Drift		$\lvert TCI_O \rvert$	–	80	–	PPM/°C
Digital Input Logic Levels High Level, Logic "1" (MC1406L, MC1506L) Low Level, Logic "0" (MC1406L) (MC1506L)	3,14	 V_{IH} V_{IL}	 2.0 – –	 – – –	 – 0.8 0.5	Vdc
Digital Input Current High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3,13	 I_{IH} I_{IL}	 – –	 0 -0.7	 +0.01 -1.5	mA
Reference Input Bias Current (Pin 13)	3	I_{13}	–	-0.002	-0.01	mA
Output Current Range V_{EE} = -5.0 V V_{EE} = -6.0 to -15 V	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{ref} = 2.000 V, R_{12} = 1.000 kΩ	3	I_O	1.9	1.97	2.1	mA
Output Current (all bits high)	3	$I_{O(min)}$	–	0	10	µA
Output Voltage Compliance ($E_r \leqslant \pm 0.78\%$ at T_A = +25°C)	3,4,5	V_O	–	–	±0.4	Vdc
Reference Current Slew Rate (T_A = +25°C)	8,15	SR I_{ref}	–	2.0	–	mA/µs
Output Current Power Supply Sensitivity	10	PSRR (–)	–	0.002	0.010	mA/V
Power Supply Current A1 thru A6; V_{IL} = 0.8 V A1 thru A6; V_{IH} = 2.0 V	3,11,12	 I_{CC} I_{EE}	 – –	 +7.2 -9.0	 +11 -11	mA
Power Dissipation (all bits high) V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc		P_D	 – –	 85 175	 120 240	mW

*T_{high} = +75°C for MC1406L T_{low} = 0°C for MC1406L
= +125°C for MC1506L = -55°C for MC1506L

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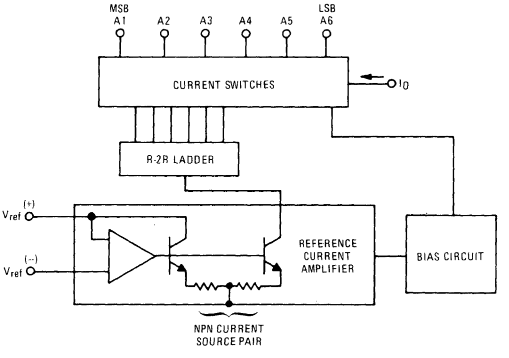
The MC1506L consists of a reference current amplifier, and R-2R ladder, and six high-speed current switches. For many applications, only a reference resistor and a reference supply voltage need be added.

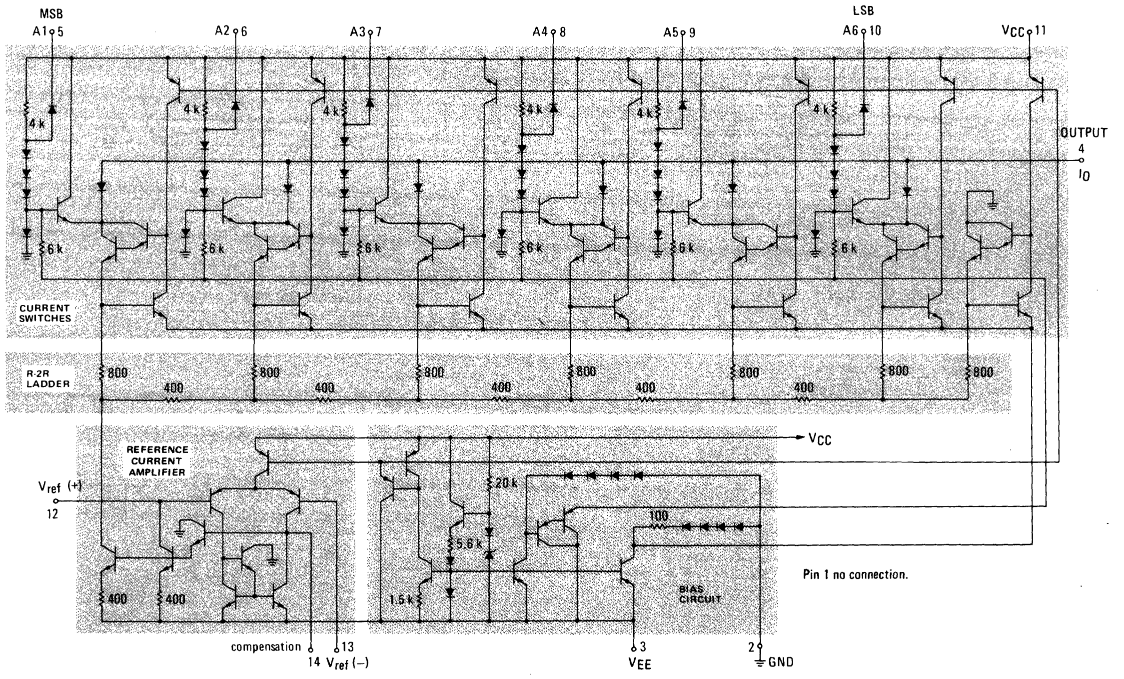
The switches are inverting in operation, therefore a low state at the input turns on the specified output current component. The switches use a current steering technique for high speed and a termination amplifier that consists of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components which are fed to the switches. Note that there is always a remainder current that is equal to the least significant bit. This current is shunted to ground, and the maximum current is 63/64 of the reference amplifier current, or 1.969 mA for a 2.0 mA reference current if the NPN current source pair is perfectly matched.

BLOCK DIAGRAM



COMPLETE CIRCUIT SCHEMATIC
(Digital Inputs; pins 5,6,7,8,9,10)



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TEST CIRCUITS AND TYPICAL CHARACTERISTICS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT

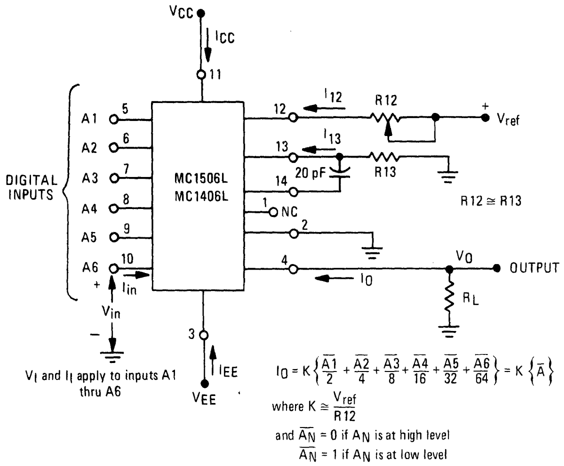


FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE

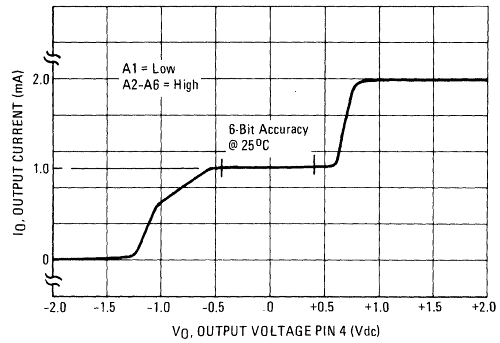


FIGURE 5 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE

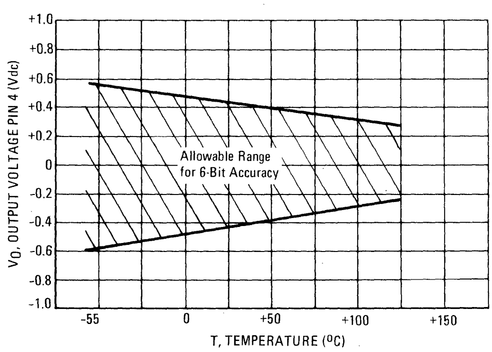


FIGURE 6 – POSITIVE V_{ref}

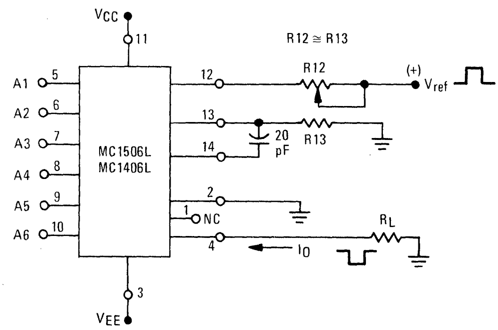


FIGURE 7 – NEGATIVE V_{ref}

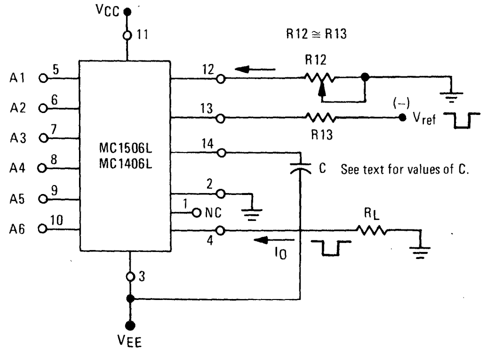
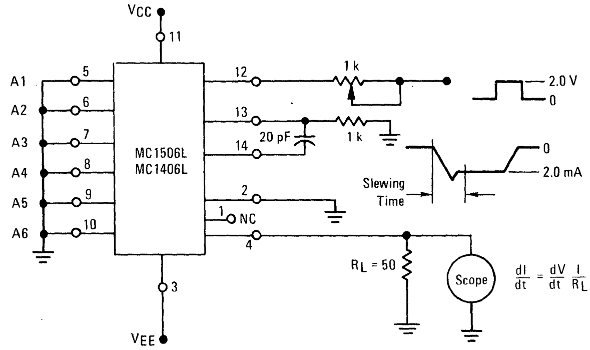


FIGURE 8 – REFERENCE CURRENT SLEW RATE MEASUREMENT TEST CIRCUIT



TEST CIRCUITS and TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – TRANSIENT RESPONSE

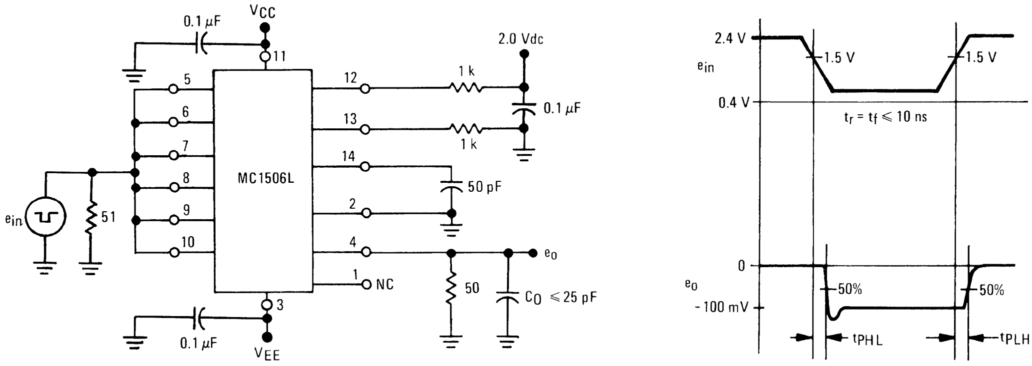


FIGURE 10 – RELATIVE ACCURACY TEST CIRCUIT

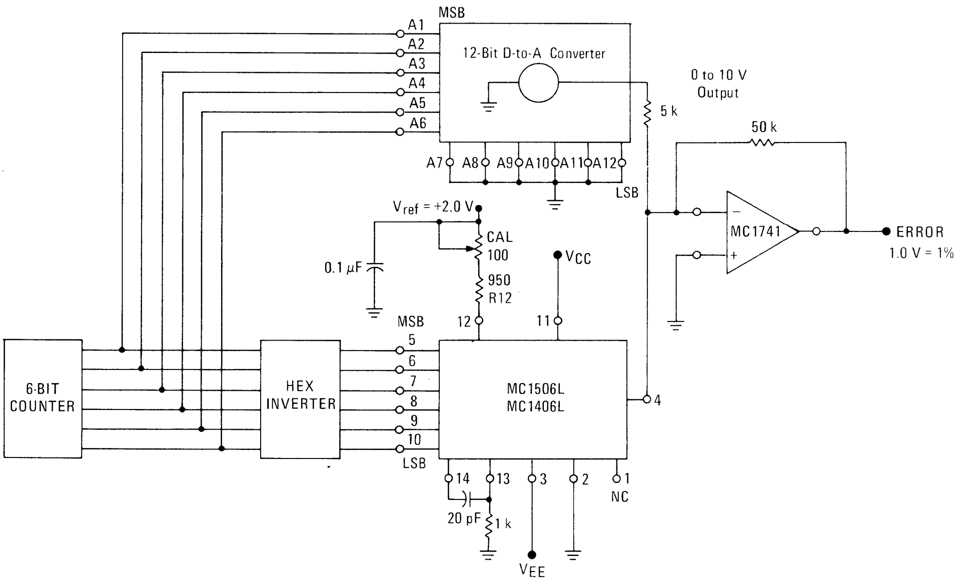


FIGURE 11 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE

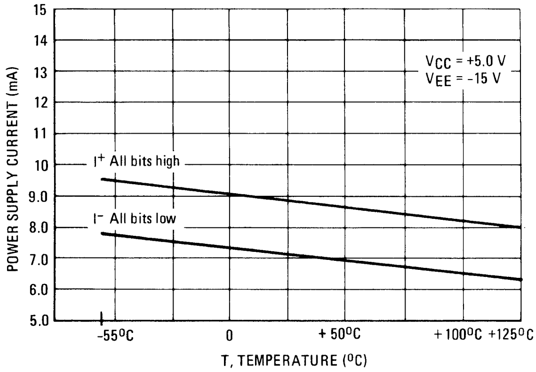
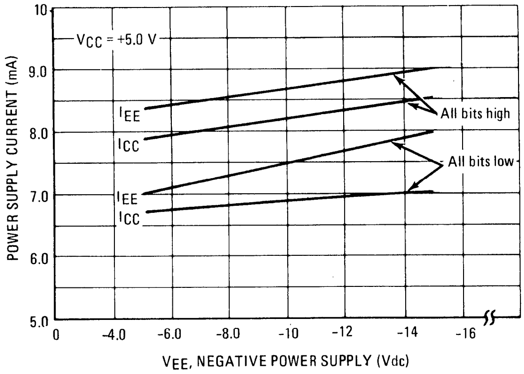


FIGURE 12 – TYPICAL POWER SUPPLY CURRENT versus V_{EE}



TYPICAL CHARACTERISTICS (continued)

FIGURE 13 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

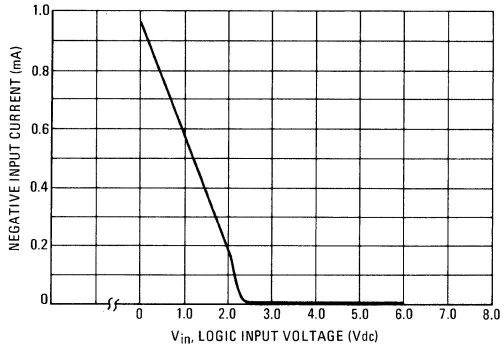


FIGURE 14 – MSB TRANSFER CHARACTERISTICS versus TEMPERATURE (MSB IS "WORST CASE")

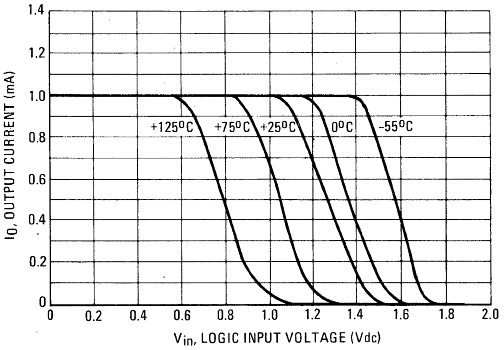
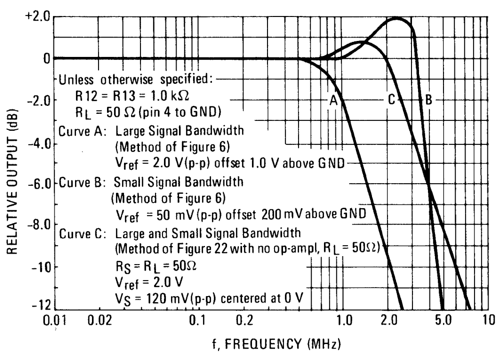


FIGURE 15 – REFERENCE INPUT FREQUENCY RESPONSE



GENERAL INFORMATION

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages below -6.0 volts, due to the increased voltage drop across the 400-ohm resistors in the reference current amplifier.

Output Voltage Compliance

The MC1506L current switches have been designed for high-speed operation and as a result have a restricted output voltage range, as shown in Figures 4 and 5. When a current switch is turned "off", the follower emitter is near ground and a positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington amplifier is one diode voltage below ground; thus a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

For example, at +25°C the allowable voltage compliance on pin 4 to maintain six-bit accuracy is ±0.4 volt. With a full scale output current of 2.0 mA, the maximum resistor value that can be connected from pin 4 to ground is 200 ohms.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1506L is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current.

The best temperature performance is achieved with a -6.0 V supply and a reference voltage of -3.0 volts. These conditions match the voltage across the NPN current source pair in the reference amplifier at the lowest possible voltage, matching and optimizing the output impedance of the pair.

The MC1506L/MC1406L is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.969 mA. This corresponds to a reference amplifier output current drive to the ladder of 2.0 mA, with the loss of one LSB = 31 μA that is the ladder remainder shunted to ground. The input current to pin 12 has a guaranteed current range value of between 1.9 to 2.1 mA, allowing

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GENERAL INFORMATION (continued)

some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 10. The 12-bit converter is calibrated for a full scale output current of 1.969 mA. This is an optional step since the MC1506L accuracy is essentially the same between 1.5 to 2.5 mA. Then the MC1506L full scale current is trimmed to the same value with R12 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 6-bit D-to-A converters may not be used to construct a 12-bit accurate D-to-A converter. 12-bit accuracy implies a total error of ±1/2 of one part in 4096, or ±0.012%, which is more accurate than the ±0.78% specification provided by the MC1506L.

Multiplying Accuracy

The MC1506L may be used in the multiplying mode with six-bit accuracy when the reference current is varied over a range of 64:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions these six amplifiers can contribute a total of 6.0 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 60 μA to 4.0 mA, the 6.0 μA contributes an error of 0.1 LSB. This is well within six-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1506L is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a high-to-low transition for all bits. This time is typically 150 ns to within ±1/2 LSB, while the turn "off" is typically under 50 ns.

The slowest single switch is the least significant bit, which turns "on" and settles in 50 ns and turns "off" in 30 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 150 ns may be realized.

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 12 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I12, must always flow into pin 12 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6. The reference voltage source supplies the full current I12. Compensation is accomplished by Miller feedback from pin 14 to pin 13. This compensation method yields the best slew rate, typically better than 2.0 mA/μs, and is independent of the value of R12. R13 must be used to establish the proper impedance for compensation at pin 13. For bipolar reference signals, as in the multiplying mode, R13 can be tied to a negative voltage corresponding to the minimum input level. Another method is shown in Figure 22.

It is possible to eliminate R13 with only a small sacrifice in accuracy and temperature drift. For instance when high-speed operation is not needed, a capacitor is connected from pin 14 to V_{EE}. The capacitor value must be increased when R12 is made larger to maintain a proper phase margin. For R12 values of 1.0, 2.5, and 5.0 kilohms, minimum capacitor values are 50, 125, and 250 pF.

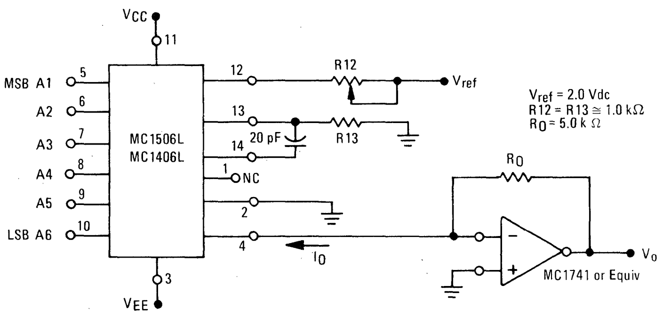
Connections for a negative reference voltage are shown in Figure 7. A high input impedance is the advantage of this method, but Miller feedback cannot be used because it feeds the input signal around the PNP directly into the high impedance node, causing slewing problems and high frequency peaking. Compensation involves a capacitor to V_{EE} on pin 14, using the values of the previous paragraph. The negative reference voltage must be at least 3.0 V above V_{EE}. Bipolar input signals may be handled by connecting R12 to a positive reference voltage equal to the peak positive input level at pin 13.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0 V logic supply is not recommended as a reference voltage. If a well regulated 5.0 V supply which drives logic is to be used as the reference, R12 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 12 and ground.

If pin 12 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, thus decreasing the overall bandwidth.

APPLICATIONS INFORMATION

FIGURE 16 – OUTPUT CURRENT VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R12}(R_O)\left(\frac{\bar{A1}}{2}+\frac{\bar{A2}}{4}+\frac{\bar{A3}}{8}+\frac{\bar{A4}}{16}+\frac{\bar{A5}}{32}+\frac{\bar{A6}}{64}\right) = K\,R_O\{\bar{A}\}$$

Adjust R_{ref} so that V_O with all digital inputs at low level is equal to 9.844 volts.

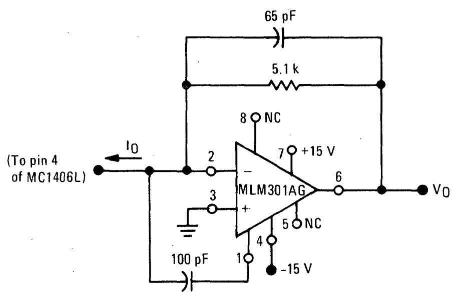
$$V_O = \frac{2\,V}{1\,K}(5\,K)\left(\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}\right) = 10\,V\left(\frac{63}{64}\right) = 9.844\,V$$

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1506L at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

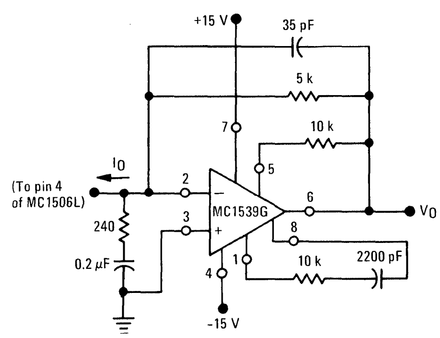
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 17

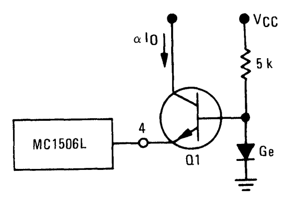


An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 18



The positive voltage range may be extended by cascoding the output with a high beta common base transistor, Q1, as shown.



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing.

APPLICATIONS INFORMATION (continued)

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1506L requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive, with the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current, see Figure 19. Instead of powering the MC1723G from a single positive voltage supply, it uses a negative bias as well. Although the reference voltage of the MC1723G is then developed with respect to that negative voltage it appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

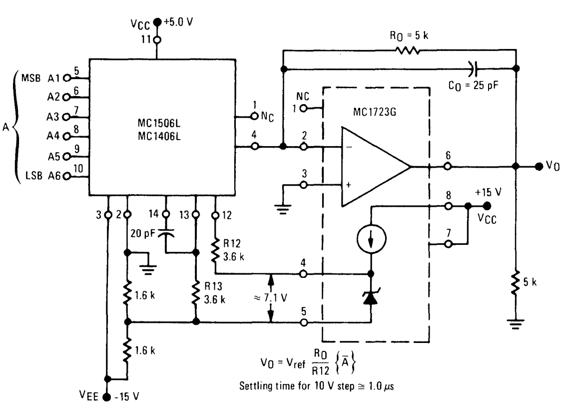
Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

Programmable Power Supply

The circuit of Figure 19 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +6.3 volts in 0.1-volt increments, ±0.05 volt; or 0 to 31.5 volts in 0.5-volt increments, ±0.25 volt.

FIGURE 19 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



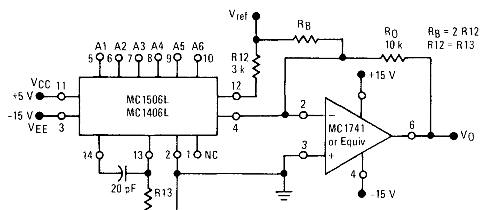
$V_O = V_{ref}\frac{R_O}{R12}\{\bar{A}\}$

Settling time for 10 V step ≅ 1.0 μs

Bipolar or Negative Output Voltage

The circuit of Figure 20 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 6-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V (p-p) output range.

FIGURE 20 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT

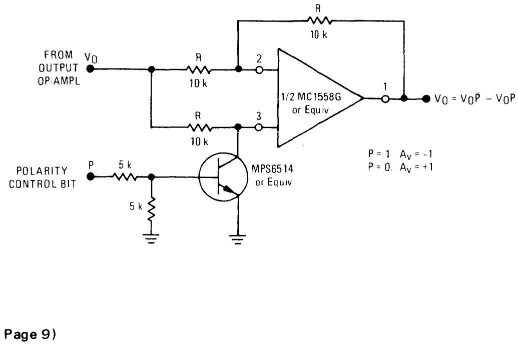


$V_O = \frac{V_{ref}}{R12}(R_O)\left(\frac{\bar{A1}}{2}+\frac{\bar{A2}}{4}+\frac{\bar{A3}}{8}+\frac{\bar{A4}}{16}+\frac{\bar{A5}}{32}+\frac{\bar{A6}}{64}\right) - \frac{V_{ref}}{R_B}(R_O)$

Polarity Switching Circuit, 6-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 21, gives 6-bits magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 21 – POLARITY SWITCHING CIRCUIT (6-Bit Magnitude Plus Sign D-to-A Converter)



APPLICATIONS INFORMATION (continued)

Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1506L can be applied as a digital attenuator. See Figure 22. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed and a wide large signal bandwidth is achieved. The small and large signal bandwidths are now identical and are shown in Figure 15.

The best frequency response is obtained by not allowing I_{12} to reach zero. R_S can be set for a ±1.0 mA variation in relation to I_{12}. I_{12} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word that makes ac coupling necessary.

FIGURE 22 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT

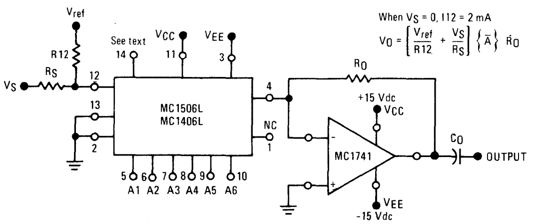
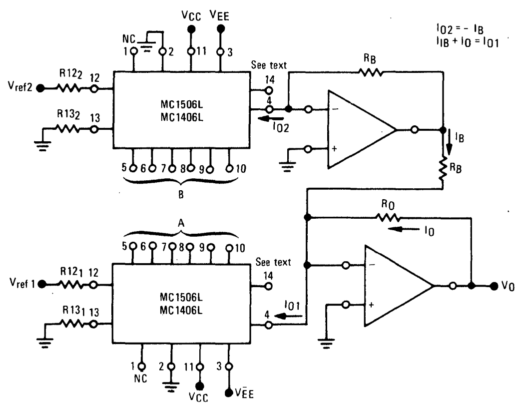


FIGURE 24 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



$I_O = I_{O1} - I_{O2} = \frac{V_{ref1}}{R12_1}\{A\} - \frac{V_{ref2}}{R12_2}\{B\}$

Digital Subtraction:

let $\frac{V_{ref1}}{R12_1} = \frac{V_{ref2}}{R12_2}$

$V_O = \frac{V_{ref1}}{R12_1} R_O \left|\{\bar{A}\} - \{\bar{B}\}\right|$

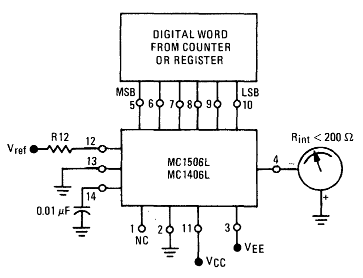
Programmable Amplifier:
Connect digital inputs so A = B

$V_O = \{\bar{A}\}\left|\frac{V_{ref1}}{R12_1} - \frac{V_{ref2}}{R12_2}\right|$

Panel Meter Readout

The MC1506L can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R12 or V_{ref}.

FIGURE 23 – PANEL METER READOUT CIRCUIT

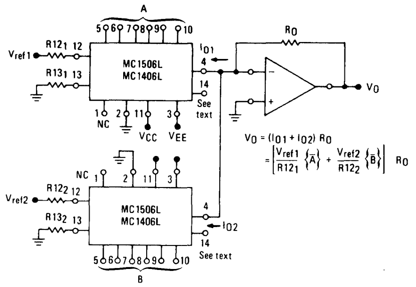


This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to $R12_1$ and $R12_2$ or $R13_1$ and $R13_2$. V_O will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect $R12_1$ and $R12_2$ to a positive reference higher than the most positive input, and drive $R13_1$ and $R13_2$. This yields high input impedance, bipolar differential and common-mode range. The compensation depends on the input method used, as shown in previous sections.

APPLICATIONS INFORMATION (continued)

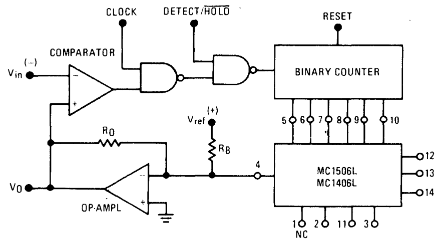
FIGURE 25 – DIGITAL SUMMING and CHARACTER GENERATION



In a character generation system one MC1506L circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 12-bit D-to-A converter (see Accuracy Section).

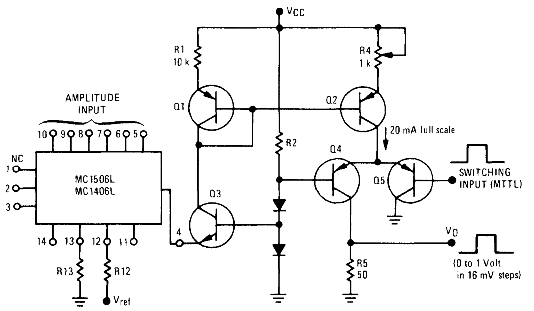
FIGURE 26 – PEAK DETECTING SAMPLE and HOLD

(Features infinite hold time and optional digital output.)



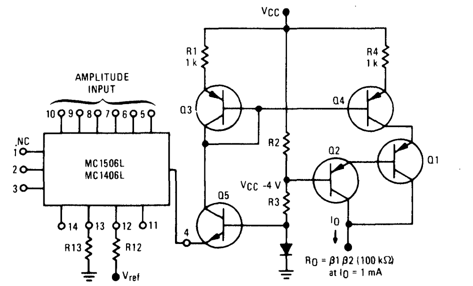
Positive peaks may be detected by inserting a hex inverter between the counter and MC1506L, reversing the comparator inputs, and connecting the output amplifier for unipolar operation.

FIGURE 27 – PROGRAMMABLE PULSE GENERATOR



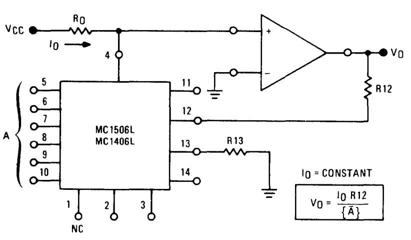
Fast rise and fall times require the use of high speed switching transistors for the differential pair, Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input.

FIGURE 28 – PROGRAMMABLE CONSTANT CURRENT SOURCE



Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

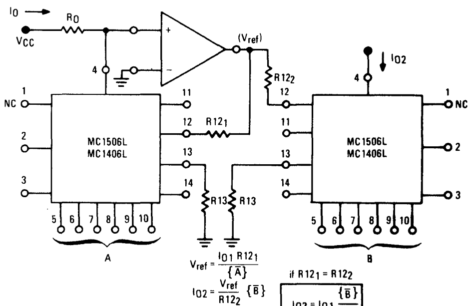
FIGURE 29 – ANALOG DIVISION BY DIGITAL WORD



This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, I_O can be set at 62 μA so that I_{12} will have a maximum value of 3.938 mA for a digital bit input configuration of 111110.

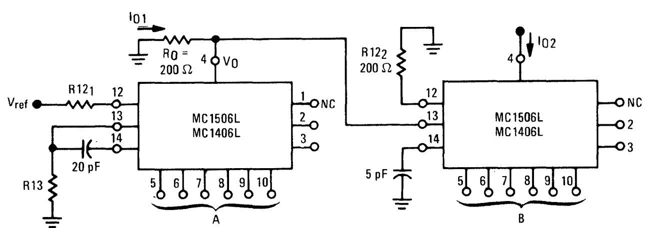
Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If this cannot be done, the reference amplifier can furnish the dominant pole with extra Miller feedback from pin 14 to 13. If the MC1723 or another wideband amplifier is used, the reference amplifier should always be overcompensated.

FIGURE 30 – ANALOG QUOTIENT OF TWO DIGITAL WORDS



APPLICATIONS INFORMATION (continued)

FIGURE 31 – ANALOG PRODUCT OF TWO DIGITAL WORDS (High-Speed Operation)



$$V_O = I_{O1} R_O = \frac{V_{ref1}}{R12_1}\{\bar{A}\} R_O$$

$$I_{O2} = \frac{\{\bar{B}\}\,|V_O|}{R12_2}$$

$$= \frac{\{\bar{B}\}}{R12_2}\left[R_O\left(\frac{V_{ref1}}{R12_1}\right)\{\bar{A}\}\right]$$

since $R_O = R12_2$ and $K = V_{ref}/R12_1$

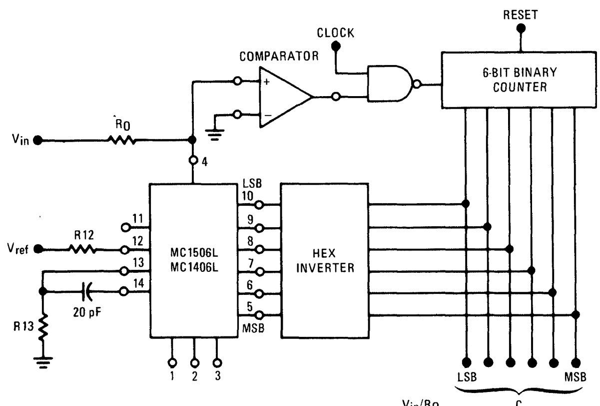
$\boxed{I_{O2} = K\{\bar{A}\}\{\bar{B}\}}$ K can be an analog variable.

Two Digit BCD Conversion

MC1506L parts which meet the specification for 7-bit accuracy can be used for the most significant word when building a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten.

FIGURE 32 – DIGITAL QUOTIENT of TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.



$$C = \frac{V_{in}/R_O}{V_{ref}/R12}$$

(MC1506 – Page 12)

MC1507L
MC1407L

A-TO-D CONTROL CIRCUIT

Specifications and Applications Information

MONOLITHIC ANALOG – DIGITAL CONTROL CIRCUIT

. . . designed for wide application in analog-to-digital, interface and high-speed instrumentation systems. The MC1507L/MC1407L consists of a wide bandwidth operational amplifier and a high-speed, dual-threshold comparator.

The comparator, which has separate Up and Down outputs, also possesses a differential reference input that sets both comparator thresholds for equal levels – but of opposite polarities.

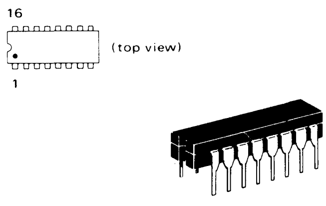
The high slew rate of the amplifier makes it particularly advantageous for use as a current-to-voltage converter for the MC1506L and the MC1508L-8 D-to-A converters. Moreover, the operational amplifier is useful as a high-speed buffer.

The MC1507L/MC1407L is well-suited for application with the above-mentioned monolithic D-to-A converters to produce an inexpensive high-speed tracking analog-to-digital converter.

- Operational Amplifier Features High Slew Rate – 20 V/μs typical and Wide Bandwidth – 24 MHz typical Unity Gain Crossover
- Fast Dual Threshold Schottky Comparator – 75 ns typical Propagation Delay Time and Input Current of Only 0.4 μA typical
- MTTL and CMOS System Compatability
- Standard Supply Voltages of +5.0 and ±15 Vdc
- Compatible with MC1508L-8 and MC1506L D-to-A Converters
- Comparator Thresholds Simultaneously Adjustable with a Single Reference Input Voltage

ANALOG-DIGITAL CONTROL CIRCUIT

MONOLITHIC SILICON INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 620

FIGURE 1 – MC1507L/MC1407L BLOCK DIAGRAM

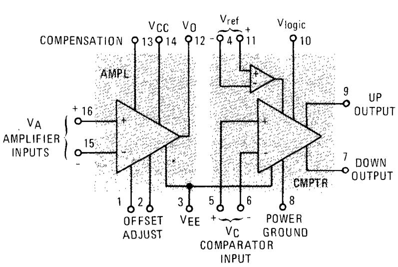
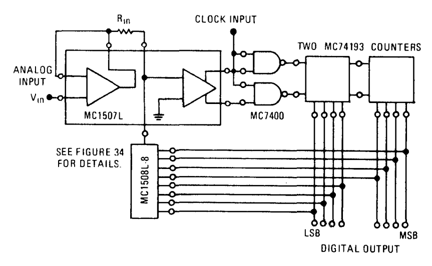


FIGURE 2 – TYPICAL APPLICATION 8-BIT TRACKING A-TO-D CONVERTER



TYPICAL APPLICATIONS

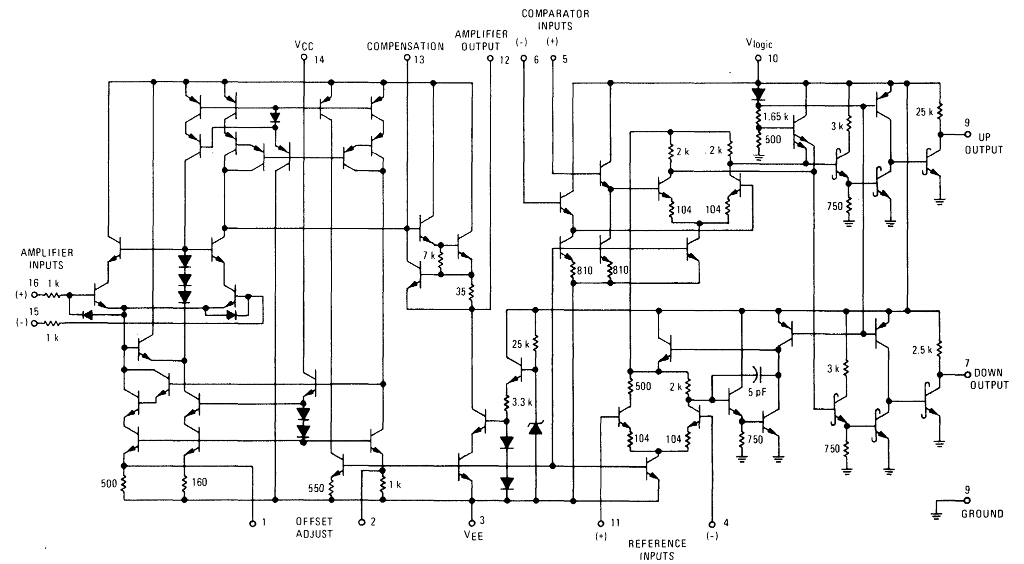
- High-Speed Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- Speech Conversion
- DAC Current-to-Voltage Converter
- Control Systems
- Signal Generators
- High-Speed Buffer
- Window Comparator
- Peak Detecting Sample and Hold
- Voltage-to-Frequency Conversion
- Fast Integrator
- Delta Modulation

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages			
Logic Voltage Supply	V_{logic}	+5.5	Vdc
Positive Voltage Supply	V_{CC}	+16.5	
Negative Voltage Supply	V_{EE}	-16.5	
Differential Input Voltage Signal			
Amplifier Voltage	$V_{16} - V_{15}$	±10	V
Comparator Voltage	$V_6 - V_5$	±10	
Comparator Reference Voltage	$V_{11} - V_4$	±5.0	
Common-Mode Input Voltage Swing			
Amplifier Voltage	V_{ICRA}	V_{CC}, V_{EE}	V
Comparator Voltage	V_{ICRC}	V_{logic}, V_{EE}	
Comparator Reference Voltage	$V_{ICRC_{ref}}$	V_{logic}, V_{EE}	
Amplifier Output Short-Circuit Duration	t_{SC}	10	s
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		1000	mW
Derate above T_A = +25°C		6.0	mW/°C
Operating Temperature Range	T_A		°C
MC1507L		-55 to +125	
MC1407L		0 to +75	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, V_{logic} = +5.0 Vdc, $V_{ref}(+)$ = 40 mVdc, $V_6 = V_4$ = 0 V, T_A = +25°C unless otherwise noted.)

AMPLIFIER SECTION

Characteristic	Symbol	MC1507 Min	MC1507 Typ	MC1507 Max	MC1407 Min	MC1407 Typ	MC1407 Max	Unit
Input Offset Voltage $R_S \leq 2.0$ kΩ, T_A = +25°C $T_A = T_{low}$* to T_{high}*	$\|V_{IO}\|$	 – –	 1.0 –	 2.0 3.0	 – –	 2.0 –	 6.0 7.5	mV
Open-Loop Voltage Gain (V_O = 0 to +10 V, 0 to -10 V, R_L = 5.0 kΩ, $T_A = T_{low}$ to T_{high})	$A_{vol}\pm$	10,000	35,000	–	5,000	20,000	–	V/V
Input Bias Current T_A = +25°C $T_A = T_{low} = T_{high}$	I_{IBA}	 – –	 0.6 –	 1.5 2.5	 – –	 1.2 –	 2.5 4.0	µA
Input Offset Current T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IOA}	 – –	 0.03 –	 0.15 0.25	 – –	 0.06 –	 0.30 0.45	µA
Common-Mode Input Voltage Swing	V_{ICRA}	±11	–	–	±11	–	–	V
Common-Mode Rejection Ratio	CMRR	10,000	35,000	–	10,000	35,000	–	V/V
Output Impedance (f = 20 Hz)	z_O	–	1.8	–	–	1.8	–	kΩ
Output Voltage Swing (R_L = 5.0 kΩ) V_{16} = -10 V or A_v = +1 mode, T_A = +25°C V_{16} = -10 V or A_v = +1 mode, $T_A = T_{low}$ to T_{high} V_{16} = 0 V, T_A = +25°C V_{16} = 0 V, $T_A = T_{low}$ to T_{high}	$V_O\pm$	 ±11 ±10 +11,-1.0 +10,-1.0	 ±12 – +12,-2.0 –	 – – – –	 ±11 ±10 +11,-1.0 +10,-1.0	 ±12 – +12,-2.0 –	 – – – –	V
Unity Gain Crossover Frequency Compensated for Unity Gain C13 = 10 pF, (Pulse Margin = 35°C typical) Open-Loop Noncompensated (Phase Margin = 0° typical)	f_C	 – –	 12 24	 – –	 – –	 12 24	 – –	MHz
Large-Signal Step Response Gain = +1, V_{in} = 0 to 10 V (See Figure 16) Slew Rate Settling time to within 0.1% Gain = +1, V_{in} = -10 to +10 V (See Figure 16) Settling time to within 0.1% Gain = -1, V_{in} = 0 to -10 V Slew Rate Settling time to within 0.1% Gain = -10, V_{in} = 0 to -10 V Slew Rate Settling time to within 0.1% Gain = -10, V_{in} = 0 to -1.0 V Slew Rate Settling time to within 0.1% Gain = -100, V_{in} = 0 to -100 mV Settling time to within 0.1%	 SR t_{setlg} t_{setlg} SR t_{setlg} SR t_{setlg} SR t_{setlg} t_{setlg}	 10 – – 10 – 10 – 10 – –	 20 0.8 1.1 20 0.8 20 0.8 20 0.8 2.0	 – – – – – – – – – –	 10 – – 10 – 10 – 10 – –	 20 – 1.1 20 0.8 20 0.8 20 0.8 2.0	 – 0.8 – – – – – – – –	 V/µs µs µs V/µs µs V/µs µs V/µs µs µs
Small-Signal Step Response Propagation Delay Time (50% to 50%) Gain = +1, V_{in} = -50 mV to +50 mV	$t_{pd}\pm$	–	18	–	–	18	–	ns
Power Bandwidth Gain = +1, V_{in} = 10 V(p-p)	BW	320	640	–	320	640	–	kHz
Output Source Current (Short-circuit limited)	I_{source}	10	17	30	10	17	30	mA
Output Sink Current	I_{sink}	2.0	3.0	–	2.0	3.0	–	mA
Power Supply Sensitivity V_{CC} varied ±10%, V_{EE} constant V_{EE} varied ±10%, V_{CC} constand	 $PSSA^+$ $PSSA^-$	 – –	 – –	 150 150	 – –	 – –	 150 150	µV/V

*T_{low} = -55°C for MC1507L, 0°C for MC1407L
*T_{high} = +125°C for MC1507L, +75°C for MC1407L

COMPARATOR SECTION

Characteristic	Symbol	MC1507 Min	MC1507 Typ	MC1507 Max	MC1407 Min	MC1407 Typ	MC1407 Max	Unit
Input Threshold, UP Output	V_{th+}	36	40	44	30	40	50	mV
Input Threshold, DOWN Output	V_{th-}	-36	-40	-44	-30	-40	-50	mV
Input Threshold Range	$\|V_{TR}\|$	–	-150 to +320	–	–	-150 to +320	–	mV
Input Bias Current T_A = +25°C $T_A = T_{low}$* to T_{high}*	I_{IBC}	 – –	 0.4 –	 1.5 2.5	 – –	 0.8 –	 2.5 4.0	µA

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, V_{logic} = +5.0 Vdc, $V_{ref}(+)$ = 40 mVdc, V_6 = V_4 = 0 V, T_A = +25°C unless otherwise noted.)

COMPARATOR SECTION (continued)

Characteristic	Symbol	MC1507 Min	MC1507 Typ	MC1507 Max	MC1407 Min	MC1407 Typ	MC1407 Max	Unit
Input Offset Current	I_{IOC}							
T_A = +25°C		–	0.01	0.15	–	0.02	0.25	μA
T_A = T_{low} to T_{high}		–	–	0.25	–	–	0.40	
Reference Input Bias Current	I_{ref}	–	4.0	18	–	4.0	18	μA
Common-Mode Input Voltage Swing	V_{ICRC}	-10 to +1.0	–	–	-10 to +1.0	–	–	V
Low-Level Logic Output Voltage R_L = 1.4 kΩ, T_A = T_{low} to T_{high}	$V_{OL}(D)$	–	0.3	0.5	–	0.3	0.5	V
	$V_{OL}(U)$	–	0.3	0.5	–	0.3	0.5	
High-Level Logic Output Voltage T_A = T_{low} to T_{high}	$V_{OL}(D)$	4.0	4.95	–	4.0	4.95	–	V
	$V_{OL}(U)$	4.0	4.95	–	4.0	4.95	–	
Output Sink Current (each output) T_A = T_{low} to T_{high}	I_{sink}	3.2	–	–	3.2	–	–	mA
Propagation Delay Time (each output) V_{in} = 0 to V_{th} +20 mV, R_L = 1.4 kΩ	t_{PLH}	–	75	–	–	75	–	ns
	t_{PHL}	–	75	–	–	75	–	
Power Supply Sensitivity of Input Thresholds								
V_{logic} varied ±10%, V_{EE} constant	$PSSC^+$	–	–	1.0	–	–	1.0	mV/V
V_{EE} varied ±10%, V_{CC} constant	$PSSC^-$	–	–	1.0	–	–	1.0	

AMPLIFIER AND COMPARATOR SECTIONS

Characteristic	Symbol	MC1507 Min	MC1507 Typ	MC1507 Max	MC1407 Min	MC1407 Typ	MC1407 Max	Unit
Power-Supply Voltage Range (See Note 1.)								
Positive Supply Voltage	V_{CC}	+4.5	+15	+16.5	+4.5	+15	+16.5	Vdc
Negative Supply Voltage	V_{EE}	-4.5	-15	-16.5	-4.5	-15	-16.5	
Logic Supply Voltage	V_{logic}	+4.5	+5.0	+5.5	+4.5	+5.0	+5.5	
Power-Supply Currents Comparator V_{in} = 0, V_{EE} = -15 V, V_{CC} = +15 V, V_{logic} = 5.0 V								
Positive Supply Current	I_{CC}	–	+4.0	+6.0	–	+4.0	+8.0	mA
Negative Supply Current	I_{EE}	–	-10	-13	–	-10	-16	
Logic Supply Current	I_{logic}	–	+16	+20	–	+16	+25	
Power Dissipation	P_D							
V_{EE} = -5.0 V		–	190	255	–	190	325	mW
V_{EE} = -15 V		–	290	385	–	290	485	

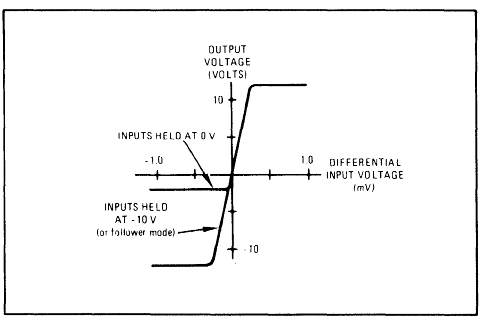
Note 1. Amplifier Output Swing decreases with reduced V_{CC} and V_{EE} supply voltages. At ±5.0-volt supplies, common-mode and output swing voltages are typically ±2.0 volts.

*T_{low} = -55°C for MC1507L, 0°C for MC1407L
T_{high} = +125°C for MC1507L, +75°C for MC1407L

THREE-QUADRANT OPERATIONAL AMPLIFIER

The amplifier is a single-gain stage especially designed for high gain and fast response. Very high impedance current sources provide a typical resistance of 20 megohms at pin 13, which is the gain node of the circuit and its major RC pole. The input of the amplifier is protected against breakdown of the NPN differential pair, and the output is short-circuit protected. Since the amplifier is a single-gain stage with all NPN transistors in the signal path, it has one limitation when compared with standard operational amplifiers. The amplifier transfer characteristic, Figure 4, shows that the output can swing no more negative than -2.0 volts with respect to the inputs. Hence, the circuit is called a three-quadrant operational amplifier. The amplifier may be used as a standard operational amplifier in the noninverting unity gain mode with an output swing of ±11 V minimum, and as an inverting amplifier to convert negative voltages to positive voltages. For output swings under 4.0 volts (p-p), as in active filter applications, the amplifier is especially useful since it offers four-quadrant operation with very wide bandwidth.

FIGURE 4 – TYPICAL TRANSFER CHARACTERISTIC FOR THREE-QUADRANT OPERATIONAL AMPLIFIER



8

TEST CIRCUITS AND WAVEFORMS

FIGURE 5 – OPERATING MODES OF THE THREE-QUADRANT OPERATIONAL AMPLIFIER

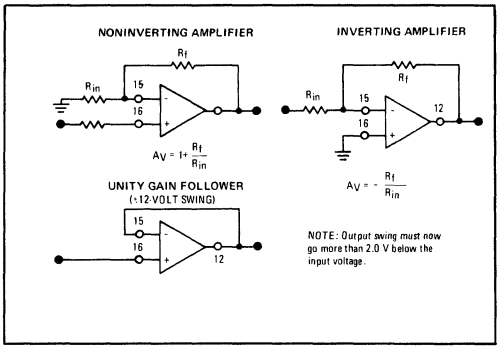


FIGURE 6 – THREE-QUADRANT OPERATIONAL AMPLIFIER PULSE RESPONSE WAVEFORMS
(Applicable to Circuits of Figures 8 or 15)
(A_V = -1, R_L = 5.0 kΩ, C_L (total) = 100 pF)

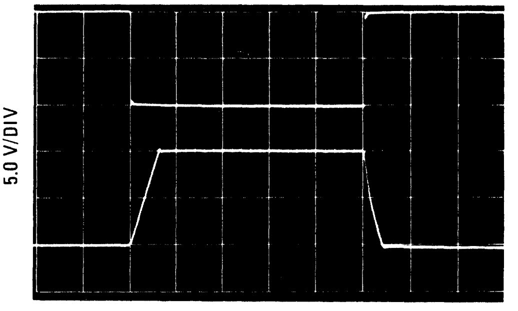


FIGURE 7 – SETTLING TIME DEFINITION

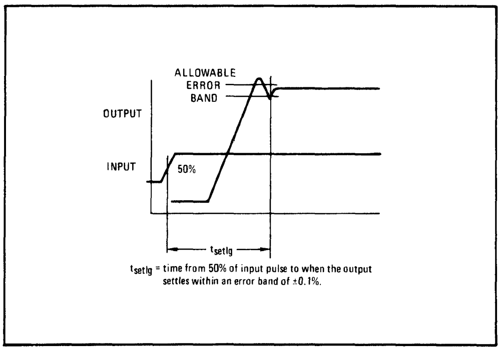


FIGURE 8 – INVERTING GAIN SETTLING-TIME TEST CIRCUIT

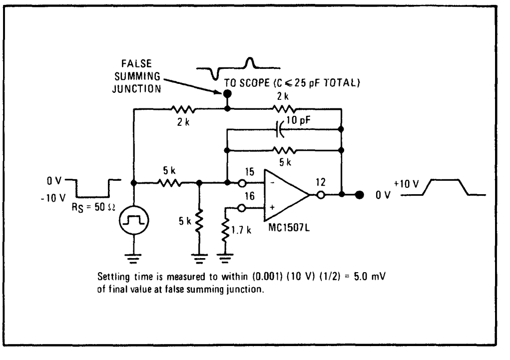


FIGURE 9 – AMPLIFIER PROPAGATION DELAY WAVEFORMS

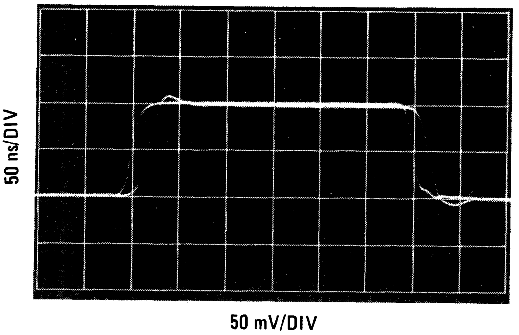
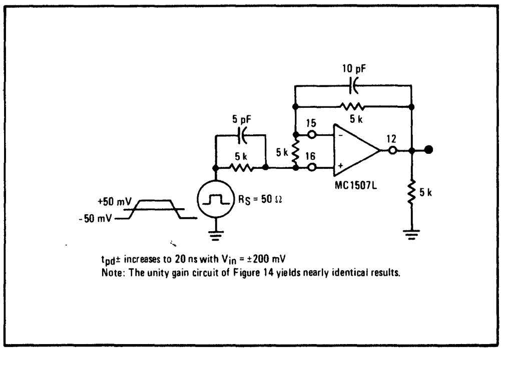


FIGURE 10 – PROPAGATION DELAY TIME TEST CIRCUIT



AMPLIFIER GAIN SELECTION

INVERTING MODE

FIGURE 11 – VOLTAGE GAIN > |-2|

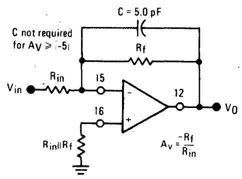
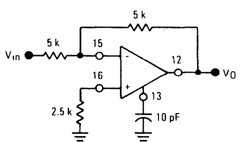
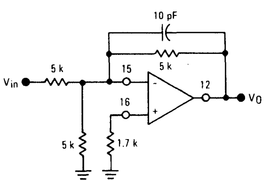


FIGURE 13 – VOLTAGE GAIN = -1



Minimum components; slew rate 5.0 V/μs with V_{in} = 0 to -10 V step, slews and settles to 0.1% in 2.0 μs.

FIGURE 15 – VOLTAGE GAIN = -1



Optimum settling time: with V_{in} = 10 V step, slews and settles to 0.1% in 800 ns.

NONINVERTING MODE

FIGURE 12 – VOLTAGE GAIN ≥ +2

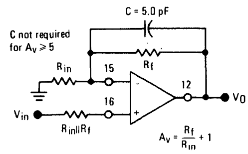
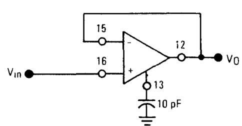
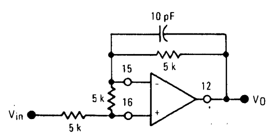


FIGURE 14 – VOLTAGE GAIN = +1



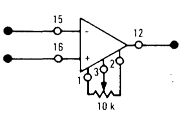
Minimum components: with V_{in} = -10 to +10 V step, slews and settles to 0.1% in 1.8 μs.

FIGURE 16 – VOLTAGE GAIN = +1



Optimum settling time. with V_{in} = -10 to + 10 V step, slews and settles to 0.1% in 1.1 μs with V_{in} = 0 to + 10 V, slews and settles in 0.8 μs and 3.0 dB bandwidth = 14 MHz.

FIGURE 17 – OFFSET VOLTAGE ADJUSTMENT



8

ADJUSTABLE DUAL THRESHOLD COMPARATOR

COMPARATOR

The comparator equivalent circuit is shown in Figure 18. It may be envisioned as two comparators with common inputs and a reference voltage source which sets equal and opposite thresholds. A positive reference voltage on pin 11 sets the thresholds as in the transfer characteristic of Figure 19. If, for example, pin 6 is grounded, when the input signal on pin 5 exceeds V_{th} (+), the UP output goes high. When the input on pin 5 exceeds V_{th} (-) in the negative direction, the DOWN output goes high.

In applications where a single output is desired, as in a window comparator, the outputs may be connected in "wired OR" if the reference voltage polarity is reversed. This inverts the output polarity so that when the input is between thresholds the outputs are in a normal high state. It also interchanges the outputs so that pin 7 responds to an input of V_{th} (+), and pin 9 to an input of V_{th} (-). See Figure 20, which is the transfer characteristic curve. When the outputs are connected together, a low output state results for an input outside the threshold window.

FIGURE 18 – COMPARATOR EQUIVALENT CIRCUIT

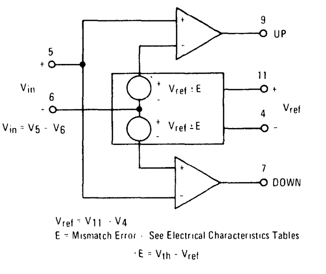


FIGURE 19 – COMPARATOR TRANSFER CHARACTERISTIC, POSITIVE REFERENCE VOLTAGE

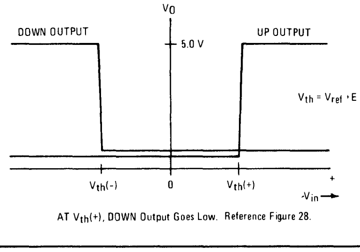
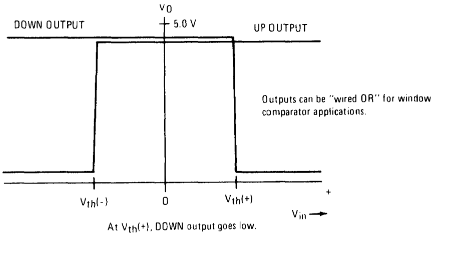
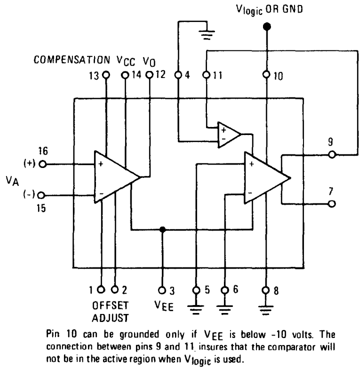


FIGURE 20 – COMPARATOR TRANSFER CHARACTERISTIC, NEGATIVE REFERENCE VOLTAGE



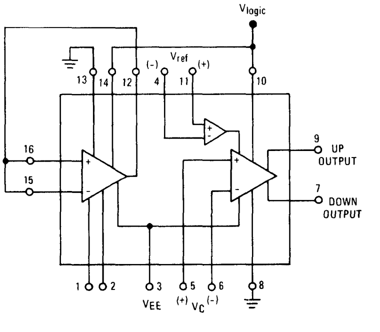
OPERATION OF OPERATIONAL AMPLIFIER OR COMPARATOR ONLY

FIGURE 21 – INDIVIDUAL AMPLIFIER OPERATION ONLY



Pin 10 can be grounded only if V_{EE} is below -10 volts. The connection between pins 9 and 11 insures that the comparator will not be in the active region when V_{logic} is used.

FIGURE 22 – INDIVIDUAL COMPARATOR OPERATION ONLY



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 23 – OPEN-LOOP FREQUENCY RESPONSE (OPERATIONAL AMPLIFIER)

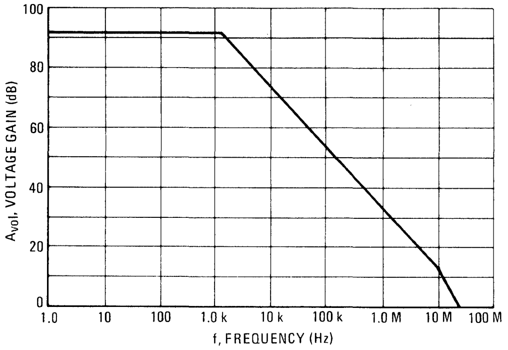


FIGURE 24 – TYPICAL SOURCE CURRENT LIMIT versus TEMPERATURE (OPERATIONAL AMPLIFIER)

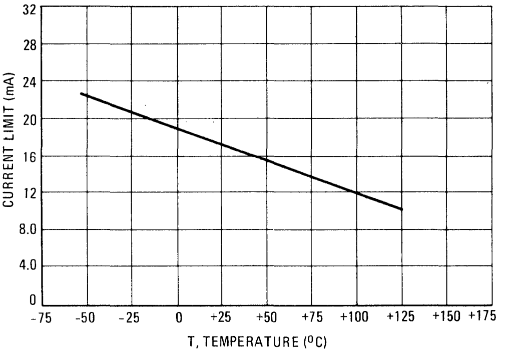


FIGURE 25 – TYPICAL POWER SUPPLY CURRENT versus V_{EE}

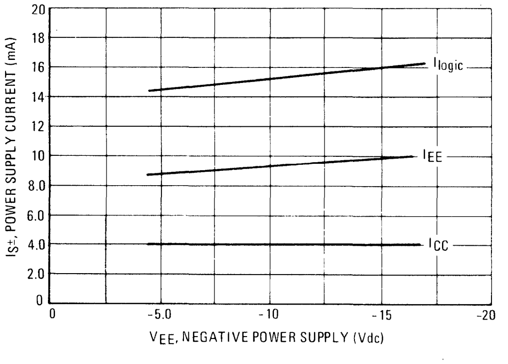


FIGURE 26 – POWER SUPPLY CURRENT versus TEMPERATURE

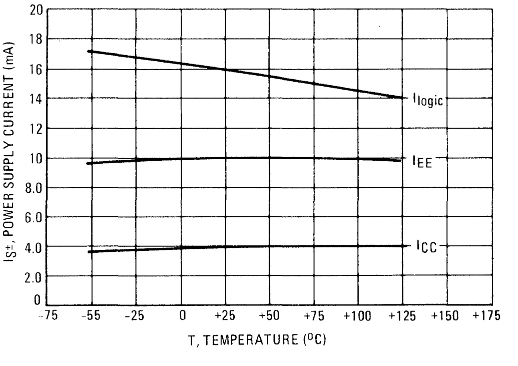


FIGURE 27 – COMPARATOR RESPONSE versus INPUT OVERDRIVE

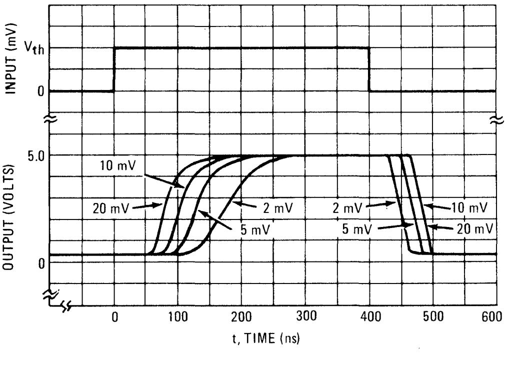
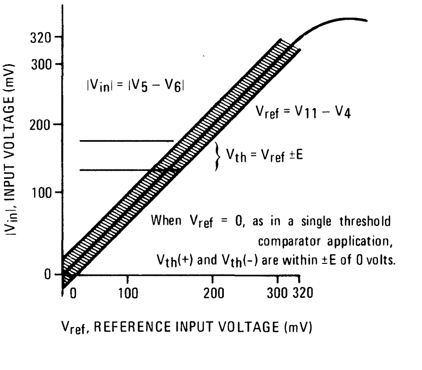
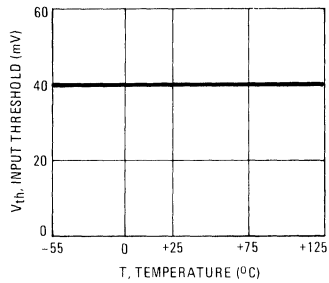


FIGURE 28 – COMPARATOR THRESHOLD versus V_{ref}



TYPICAL CHARACTERISTICS (continued)

FIGURE 29 – COMPARATOR THRESHOLD versus TEMPERATURE



APPLICATIONS INFORMATION

FIGURE 30 – SINGLE THRESHOLD COMPARATOR

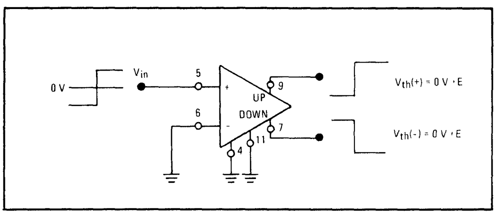


FIGURE 31 – WINDOW COMPARATOR

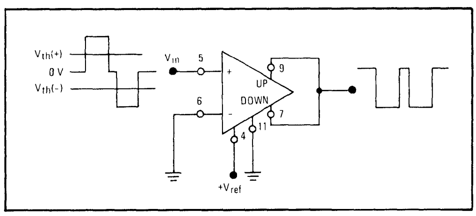
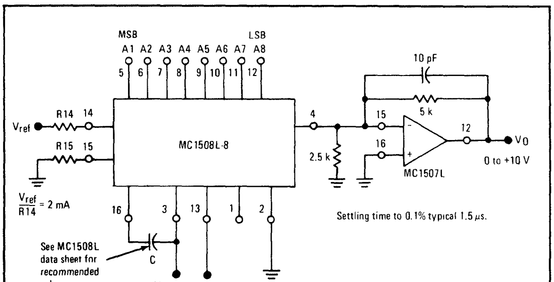


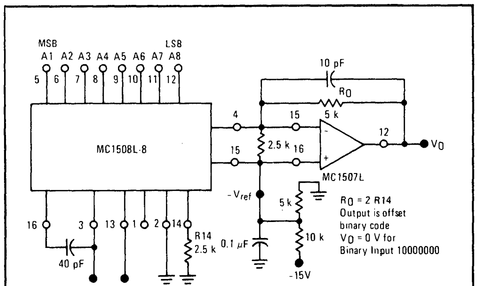
FIGURE 32 – D-TO-A CURRENT-TO-VOLTAGE CONVERTER (POSITIVE OUTPUT)



Leave pin 1 open for -10 ≤ VEE ≤ 16.5 V.

If pin 1 is grounded, a clamp diode is recommended from pin 4 to ground to keep the MC1508L-8 circuit from internally saturating.

FIGURE 33 – D-TO-A CURRENT-TO-VOLTAGE CONVERTER (BIPOLAR OUTPUT)



VO range is from -Vref to (+Vref – 1 LSB). Pins 15 and 16 are high-impedance inputs so -Vref may be derived by a resistive divider from ground to a stable negative supply (reference Figure 34).

APPLICATIONS INFORMATION (continued)

TRACKING A-TO-D CONVERTERS

A tracking A-to-D converter is a system with a digital output which continuously follows the analog input. It can be thought of as an "analog-to-digital operational amplifier" since as a system it has many similar specifications: slew rate, propagation delay, settling time, and adjustable scale factor. The tracking converter is normally used in high-speed applications which require conversion times on the order of 1-to-100 μs.

Successive approximation conversion is the other major method used for A-to-D conversion in this speed category. The advantages of the tracking system over successive approximation system include: 1) the elimination of the sample and hold function at the input, 2) a digital output which is continuously present and can be used in asynchronously sampled systems, and 3) a conversion or update period equal to slightly more than one D-to-A converter settling time. The major disadvantage of the method is that if the system slew rate is exceeded, the conversion time increases. A full scale input step function requires a conversion time of 2^n times the tracking update rate, where n is the number of bits. The full-scale conversion time can be shortened, however, using methods which will be described later, and shown in Figure 36.

Another advantage of the tracking system is that, unlike the successive approximation approach, the output always indicates a value equal to the present or very recent input level. Therefore, in many instances latches or special timing are unnecessary for data readout.

BASIC 8-BIT SYSTEM

An easily constructed tracking A-to-D converter using the MC1407L, two up/down counters, a quad NAND gate, and a monolithic D-to-A converter such as the MC1406 or MC1408L-8 is shown in Figure 34. Assuming a full scale input range of 10 volts, the reference voltage is chosen so that the UP and DOWN thresholds are at least ±1 LSB from ground. For an 8-bit converter, this would be 10 V/256 or ±40 mV. The converter operation is described by assuming that V_{in} = 0 and the counter output is 00000000. The D-to-A converter is pulling no current so the drop across R_{in} is essentially zero. Now assume V_{in} rises until it reaches 40 mV, which is the UP comparator threshold. The UP comparator fires and on the next positive edge of the clock, a pulse is fed to the UP input of the counter. As shown in the converter transfer characteristic, the counter output increases to 00000001. The D-to-A converter now pulls 8 μA, so the summing node voltage drops down to zero. In a similar manner the system could count up to any value up to the full scale 11111111 count.

Since the D-to-A converter output current levels are rated to be accurate to within ±1/2 LSB, the comparator thresholds must be set to allow for this error. If, for instance, all the D-to-A converter error occurred at one transition, one output could be 1/2 LSB or 4 μA low and the next would be 4 μA high. This would be a current step of 16 μA instead of 8 μA, and the summing node would pull back to -40 mV instead of zero. If the comparator thresholds were closer to ground than ±40 mV, this transition would cause the DOWN comparator to fire and the D-to-A current would decrease. Thus the system would oscillate between two output values for this particular transition. This may or may not be undesirable, depending on system requirements. Both outputs would be within ±1 LSB of the correct value, which is a standard A-to-D converter accuracy specification. However, the end of conversion feature described in a later section cannot be used unless the system settles to a stable value.

With thresholds of ±1 LSB, the system has a typical hysteresis of ± 1 LSB, as shown on the transfer characteristic of Figure 35. If the input voltage is ramping up and has just fired the UP comparator, the summing node pulls back to a typical value of zero. With a change in ramp direction, the input must decrease by 1 LSB to fire the DOWN comparator. This hysteresis allows for D-to-A converter error and also lends noise immunity to the system.

An A-to-D converter using a D-to-A converter in its feedback loop cannot be any more accurate than the acuracy of the D-to-A converter plus 1/2 LSB quantization error. In the case of the MC1508L-8, MC1408L-8, MC1506, and MC1406, this D-to-A accuracy is specified as ± 1/2 LSB. In a tracking converter with the comparator thresholds set to zero, the A-to-D converter output toggles between two values, each value within ±1 LSB of the correct value. The ± 1/2 LSB error of the D-to-A converter is added to the ±1 LSB error of the converter, resulting in a system error of ±1 1/2 LSB. The comparator offset or mismatch error (±E) can be trimmed out and eliminated as a source of additional error.

If the MC1507 comparator thresholds are set to ±1 LSB, the ±1/2 LSB of the D-to-A converter must also be added, again, giving a system error of ±1 1/2 LSB. In addition, the comparator mismatch error, (+E), must be added to both the UP threshold and the DOWN threshold.

In order to insure thresholds of at least ±40 mV, V_{ref} for the comparator should be no lower than ±44 mV for the MC1507L and ±50 mV for the MC1407L. This results in an additional ±0.2 LSB error in the MC1507L and an additional ±0.5 LSB error in the MC1407L. Total system error for an 8-bit converter, with ±1 LSB threshold to eliminate toggling and to improve noise immunity, is therefore ±1.7 LSB for a system with the MC1507L, ±2.0 LSB for a system with the MC1407L.

High-speed operation is possible with this converter due to the use of current summing. No operational amplifier is used in the feedback loop, so the principal delays involved are the D-to-A converter settling time and the comparator delay time. The loop delay in Figure 34 is approximately 500 ns, allowing 150 ns for the MC1507L comparator with a small overdrive. The maximum clock frequency is determined by the loop delay.

APPLICATIONS INFORMATION (continued)

Using a clock with a period less than 500 ns would make it possible for two counts to enter the D-to-A converter before the UP comparator turns "off." The turn "on" time of the MC1508L-8 current switches is longer than the turn "off" time so with a clock of slightly over 2 MHz, the steps on the up side of the sine wave of Figure 38 would be twice as large. However, even though a faster clock provides only 7-bit resolution when tracking a sine wave, the system will still settle to 8-bit accuracy for dc or square wave inputs. This principle is used in the high speed system of Figure 36. When a clock frequency of greater than 2 MHz is used, a 100 pF capacitor between the UP and DOWN comparator outputs improves the overall settling time.

TYPICAL PERFORMANCE TABLE FOR BASIC 8-BIT SYSTEM

	2-MHz CLOCK (for continuously varying inputs)	5-MHz CLOCK (for dc or step inputs)
Normal Conversion or Update Time	0.5 μs	0.2 – 1.0 μs
Typical Full-Scale Conversion Time	128 μs	50 μs
Slew Rate (10 V Input Range)	0.08 V/μs	0.2 V/μs
Power Bandwidth (10 V(p-p) Input)	2.6 kHz	6.4 kHz

FIGURE 34 – TRACKING A-TO-D CONVERTER: BASIC 8-BIT SYSTEM

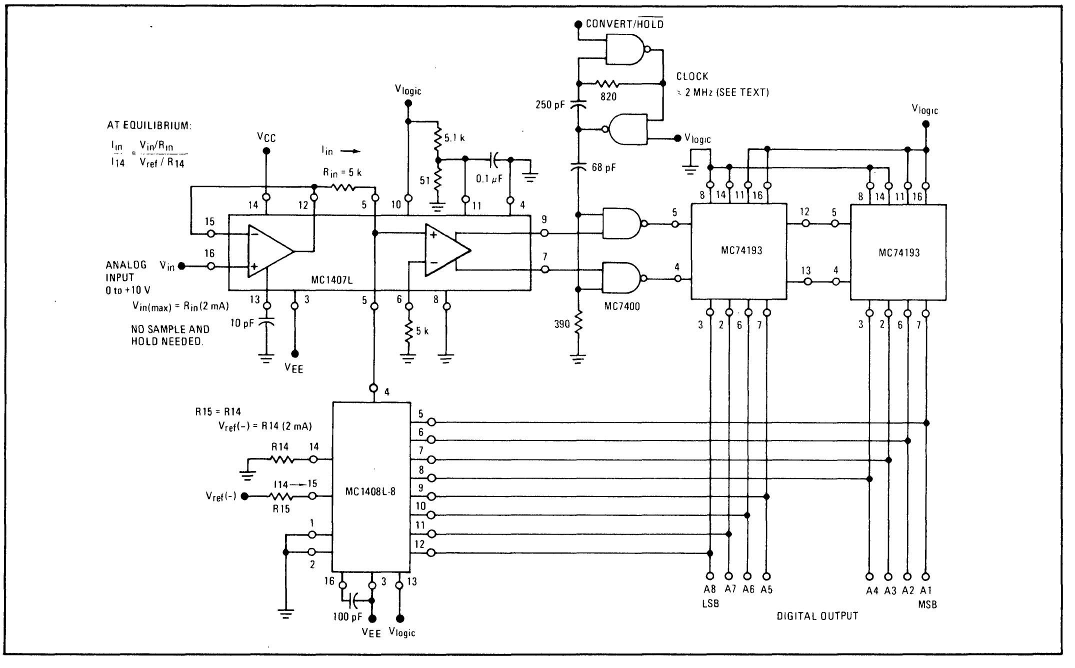
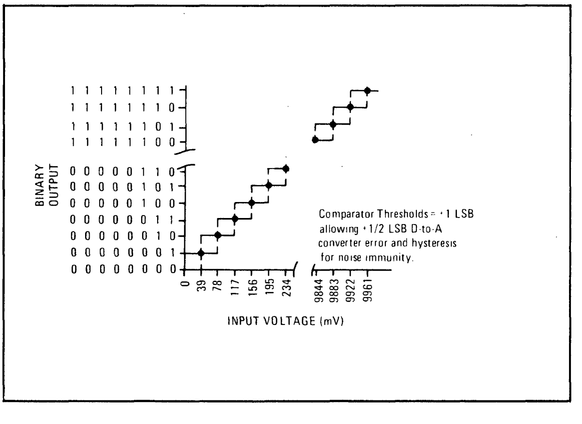


FIGURE 35 – 8-BIT TRACKING A-TO-D CONVERTER TRANSFER CHARACTERISTIC



APPLICATIONS INFORMATION (continued)

HIGH-SPEED SYSTEM

When the input voltage to the tracking A-to-D converter varies more rapidly than the system slew rate, the output will be unable to follow the input and thus there is no need for the D-to-A converter to settle between each clock pulse. A second MC1507L may be employed as a window detector to indicate when the converter summing node is more than a given voltage from the comparator deadband, as shown in Figure 36. When the window detector fires, the MC4024 voltage controlled multivibrator quadruples its clock rate, and the system switches to the "Panic Mode". When the summing node comes back within 130 mV of ground, the system resumes its normal clock rate and cleanly settles into the tracking mode.

The Panic Mode system is well suited to multiplexed data acquisition systems where the voltage presented to the input may step quickly between various levels. Also, the power bandwidth has quadrupled and the system will follow 25 kHz full scale sine waves with slightly more distortion than when in the normal tracking mode.

FIGURE 36 – TRACKING A-TO-D CONVERTER HIGH-SPEED SYSTEM (With Panic Mode Operation and Voltage Reference)

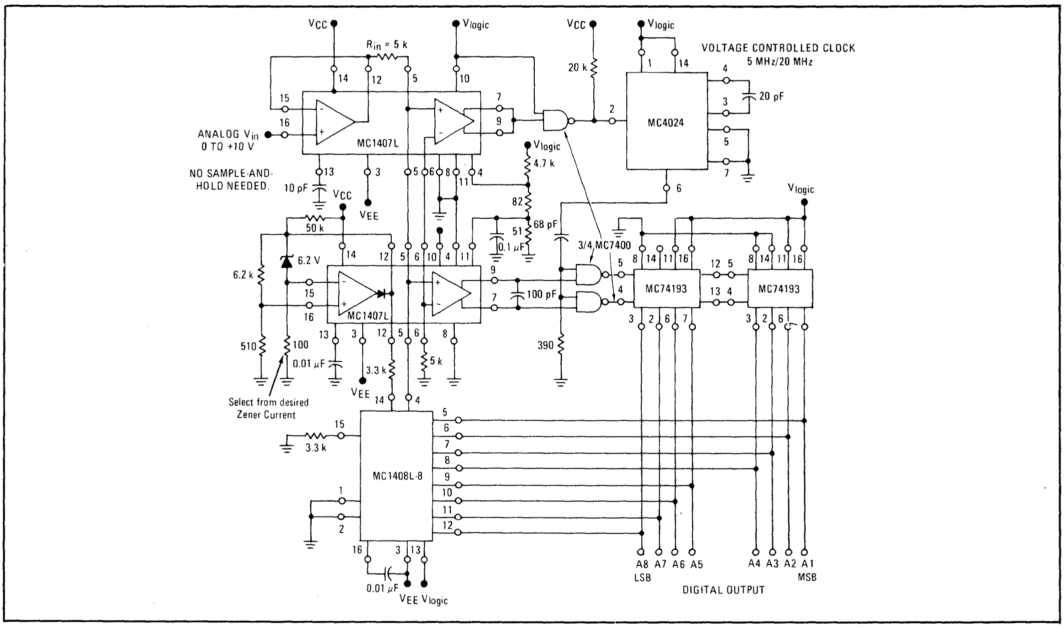
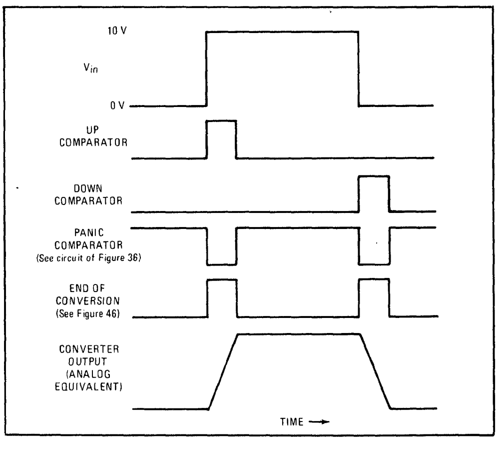


FIGURE 37 – TRACKING A-TO-D CONVERTER WAVEFORMS WITH STEP INPUT



TYPICAL PERFORMANCE TABLE FOR HIGH-SPEED SYSTEM

	2 MHz/8 MHz CLOCK (for continuously varying inputs)	5 MHz/20 MHz CLOCK (for dc or step inputs)
Normal Conversion Update Time	0.5 µs	0.2 – 1 µs
Typical Full-Scale Conversion Time	32 µs	14 µs
Slew Rate (10 V Input Range)	0.32 V/µs	0.8 V/µs
Power Bandwidth 10 V(p-p) Input	10.4 kHz	25.6 kHz

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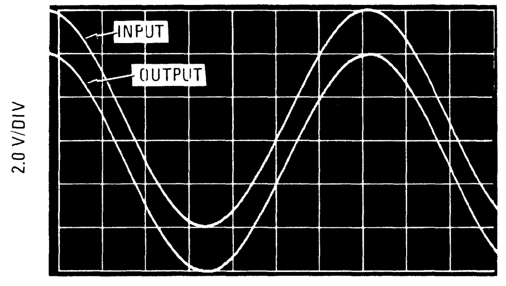
APPLICATIONS INFORMATION (continued)

FIGURE 38 – BASIC 8-BIT TRACKING A-TO-D CONVERTER SINE WAVE RESPONSE



200 µs/DIV
CLOCK FREQUENCY = 2.0 MHz
Digital output has been converted to analog using an ultra-high-speed D-to-A converter.

FIGURE 39 – EXPANDED PORTION OF FIGURE 38

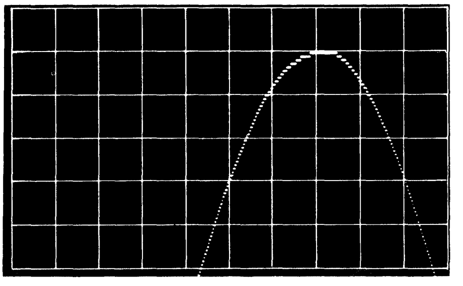
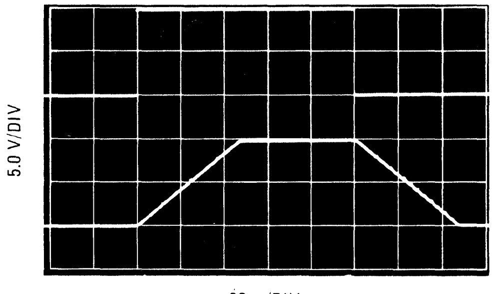
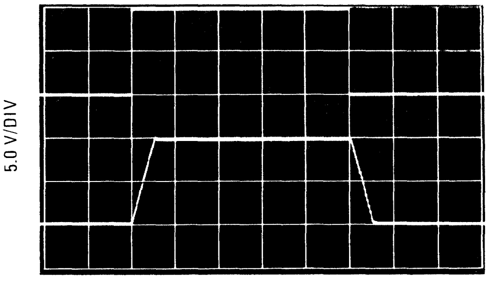


FIGURE 40 – BASIC 8-BIT TRACKING A-TO-D CONVERTER STEP RESPONSE



20 µs/DIV
CLOCK FREQUENCY = 5.0 MHz

FIGURE 41 – HIGH-SPEED 8-BIT TRACKING A TO D CONVERTER STEP RESPONSE



20 µs/DIV
Clock Frequency increases from 5.0 MHz to 20 MHz with voltage controlled MC4024 in Panic Mode operation.

6-BIT TRACKING A-TO-D CONVERTER

A 6-bit tracking A-to-D converter may be constructed with the MC1506. The circuit differs in one respect from the 8-bit system since the MC1506 has inverting logic inputs. In order to preserve negative feedback in the loop, a hex inverter may be used ahead of the D-to-A converter. However, if inverted logic outputs can be tolerated, the hex inverter is not necessary. By merely interchanging the UP and DOWN comparator outputs the counting direction is inverted, compensating for the inversion in the D-to-A converter.

The MC1506 has a faster settling time and one-fourth the number of output states, so the advantage of this system is higher speed.

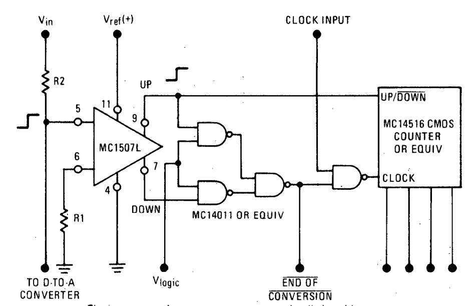
TYPICAL PERFORMANCE DATA FOR 6-BIT SYSTEM

	BASIC-SYSTEM 3 MHz CLOCK (for continuously varying inputs)	PANIC MODE SYSTEM 5 MHz/20 MHz CLOCK (for dc or step inputs)
Normal Conversion or Update Time	0.33 µs	0.2 – 1.0 µs
Typical Full-Scale Conversion Time	21 µs	4.0 µs
Slew Rate (10 V Input Range)	0.5 V/µs	3.3 V/µs
Power BAndwidth 10 V(p-p) Input	16 kHz	105 kHz

APPLICATIONS INFORMATION (continued)

TRACKING CONVERTER SYSTEM OPTIONS

FIGURE 42 – UP/DOWN COUNTER WITH SINGLE-CLOCK INPUT



The inverters on the comparator output may be eliminated by reversing the reference voltage polarity, with the result of a somewhat longer propagation delay.

FIGURE 43 – BIPOLAR INPUT

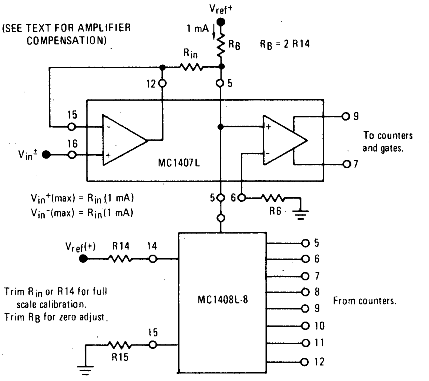


FIGURE 44 – NEGATIVE INPUT

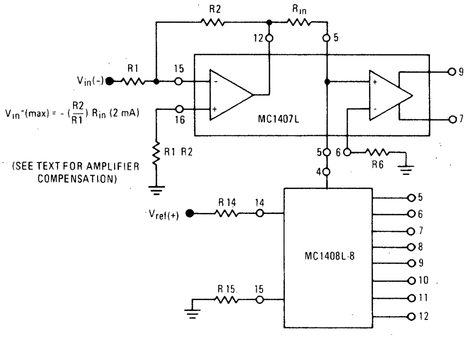
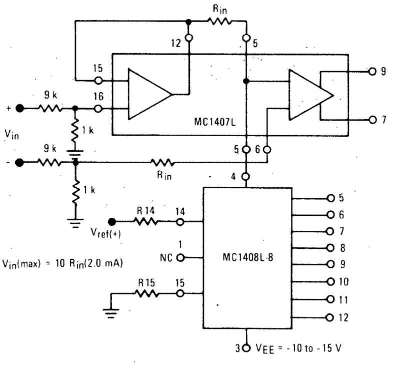


FIGURE 45 – DIFFERENTIAL INPUT



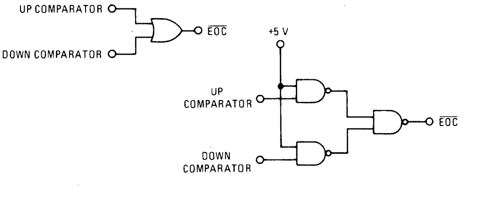
Input Common-Mode Range = +4.0 V to -10 V. D-to-A converter positive output range can be increased by cascode transistor as shown in MC1508L-8 data sheet. Common-mode range would then be ±10 volts.

END OF CONVERSION

A useful feature of the dual threshold tracking A-to-D converter is a simple method of sensing end of conversion. When the system has reached equilibrium the summing-node voltage is in the comparator deadband and both UP and DOWN outputs are low. These outputs can be fed to an OR gate to provide an $\overline{EOC}$ indication, or to three NAND gates as shown in Figure 46. This is a feature which is not available with a single threshold system, since its comparator is continually changing state.

If the A-to-D converter data is stored in latches, the $\overline{EOC}$ output can be fed to a NAND gate with the latch strobe command to insure accurate data transfer. If the strobe command occurs while the system is searching, the output from the previous conversion will be retained. However, an advantage of the tracking system is that, unlike successive approximation, its output always reflects a value equal to the present or very recent input level.

FIGURE 46 – END OF CONVERSION OPTIONS



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APPLICATIONS INFORMATION (continued)

FIGURE 47 – DIGITAL TRACK AND HOLD

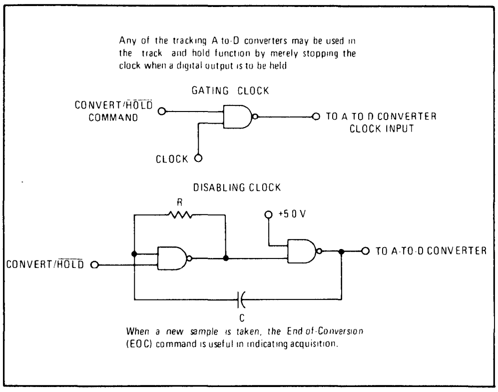
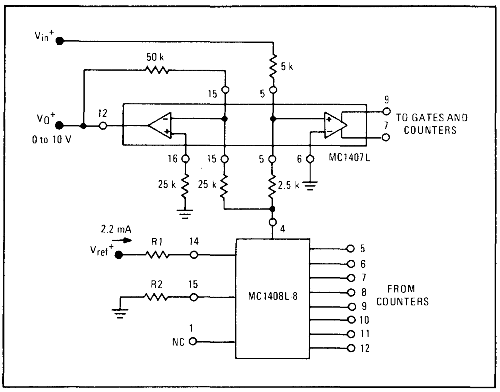


FIGURE 48 – CONNECTION CONFIGURATION FOR POSITIVE INPUT AND OUTPUT



PEAK DETECTING TRACK AND HOLD CIRCUIT WITH DIGITAL OUTPUT AND INFINITE HOLD TIME

The basic tracking A-to-D converter may be used as a positive peak detecting track and hold system by disabling the DOWN counting function. This may be performed by gating or by eliminating the DOWN connections. The system may be reset to zero by the counter reset or by re-enabling the DOWN function, shorting the converter input to ground, and allowing the output to track to zero. If the DOWN gate is disconnected from the MC74193 counter, this counter input must be connected high to allow proper functioning of the UP counter.

A negative peak detecting track and hold system is implemented by modifying the input of the above circuit to accept negative input signals, as shown in Figure 47.

TRACK AND HOLD OR PEAK DETECTION WITH ANALOG OUTPUT

The basic tracking converter system may be modified for use in the track and hold function or as a peak detecting track and hold. Analog output and infinite hold time are available with the methods shown in Figures 48-51.

FIGURE 49 – CONNECTION CONFIGURATION FOR NEGATIVE INPUT AND OUTPUT

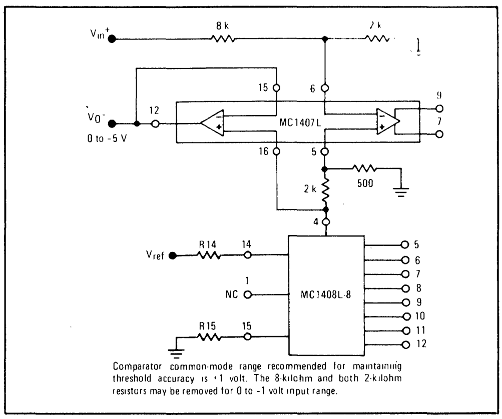


FIGURE 50 – CONNECTION CONFIGURATION FOR POSITIVE INPUT AND NEGATIVE OUTPUT

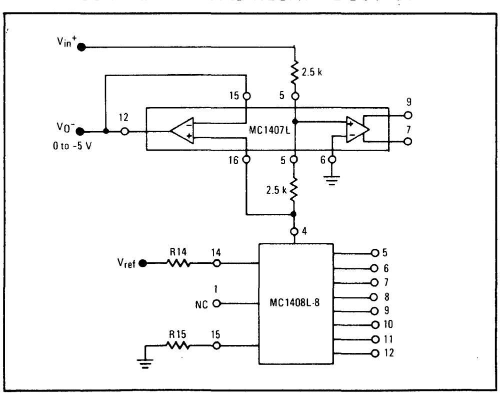
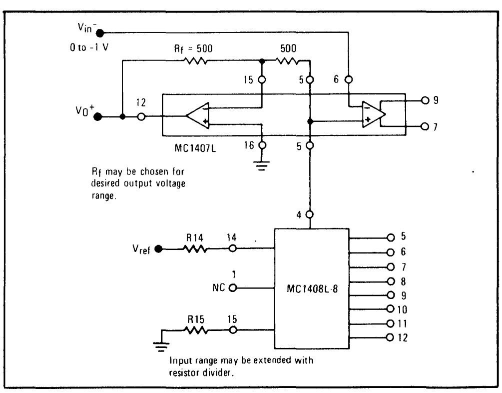


FIGURE 51 – CONNECTION CONFIGURATION FOR NEGATIVE INPUT AND POSITIVE OUTPUT



SUGGESTED DESIGN APPLICATIONS

FIGURE 52 – SUCCESSIVE APPROXIMATION A-TO-D CONVERTER

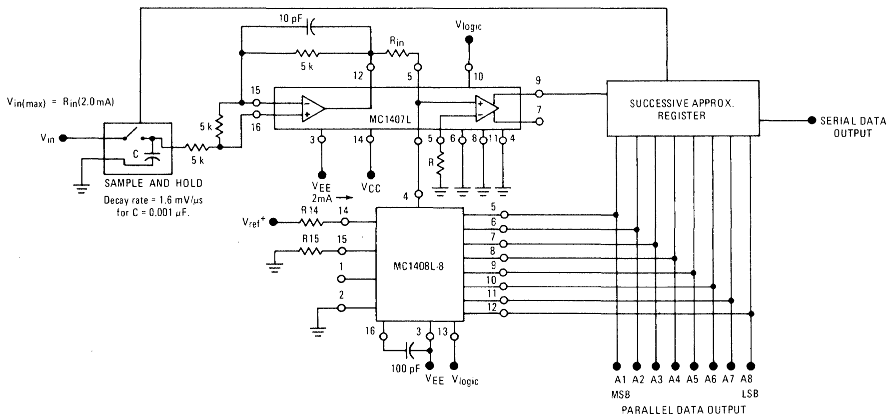


FIGURE 53 – HIGH-SPEED INTEGRATOR

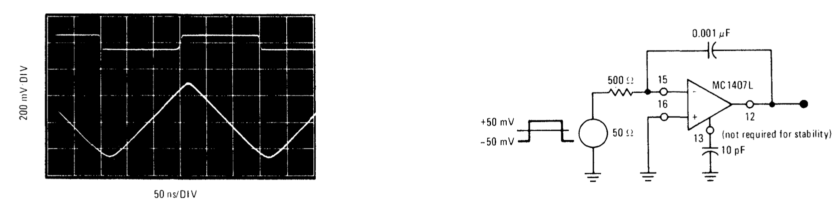
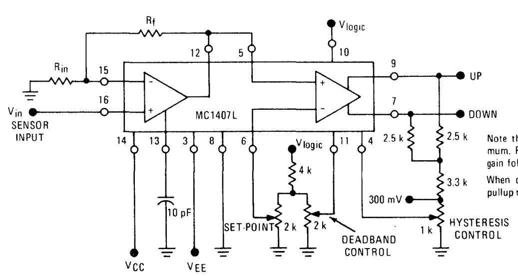


FIGURE 54 – SET-POINT CONTROL CIRCUIT
(Featuring variable deadband and hysteresis)



Note that comparator common-mode input range is +1 volt minimum. For large signals, connect the operational amplifier as a unity gain follower which drives a resistor divider to the comparator input.

When computing the hysteresis divider, remember the 2.5-kilohm pullup resistor in the comparator circuit.

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SUGGESTED DESIGN APPLICATIONS (continued)

Variable Deadband Set-Point Controls are used in control systems to compensate for large time constants in the controlled systems. The dual output control shown in Figure 54 controls two variables, such as heating and cooling, that keep a controlled variable, such as temperature, centered on the set point or operating point.

The set point voltage need not be produced by the potentiometer but can be a reference voltage supplied by the controlled system. As the set point moves linearly this voltage could come from an MC1508L-8 D-to-A converter which would provide digital control of the set point. Deadband could be controlled by the system in a similar manner.

FIGURE 55 – TRANSFER CHARACTERISTIC OF SET-POINT CONTROL

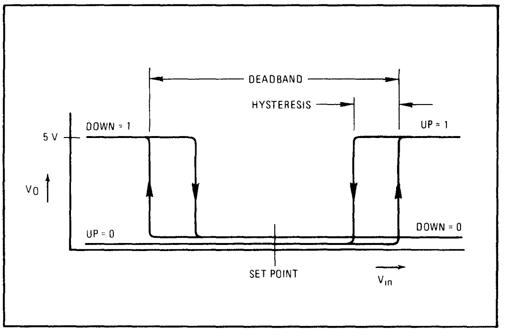


FIGURE 56 – HIGH-SPEED DELTA MODULATOR (with optional hysteresis)

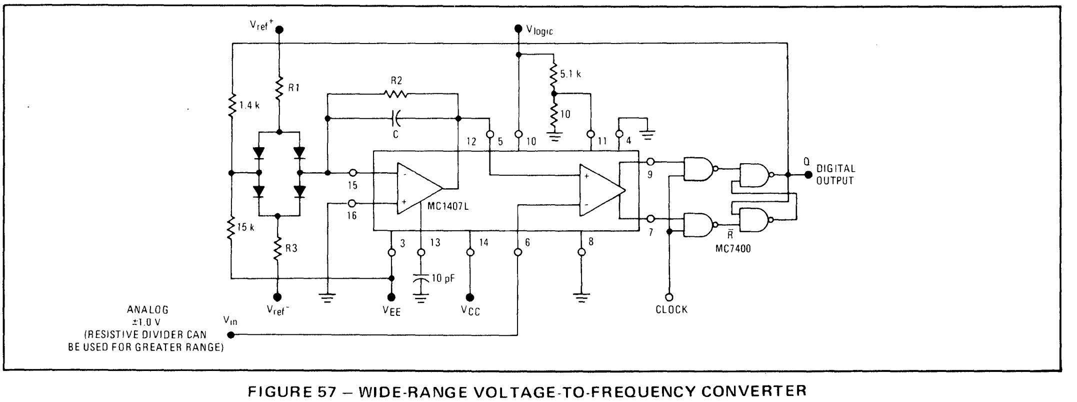
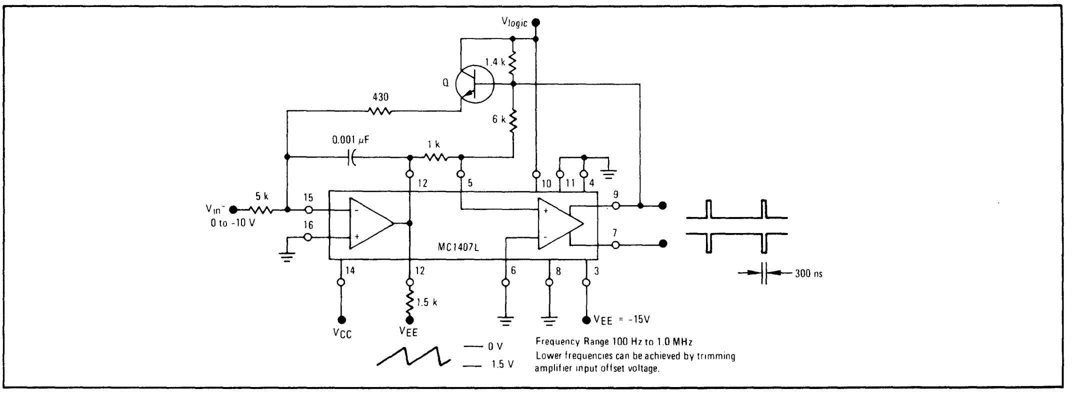


FIGURE 57 – WIDE-RANGE VOLTAGE-TO-FREQUENCY CONVERTER (Useful As Voltage-Controlled Multivibrator, FM Modulator, or Sawtooth Generator.)



8

D-TO-A CONVERTER

MC1508L-8
MC1408L-8
MC1408L-7
MC1408L-6

Specifications and Applications Information

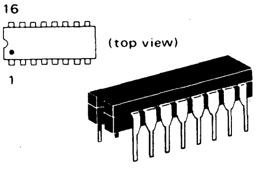
MONOLITHIC EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

- Relative Accuracy: ±0.19% Error maximum (MC1508L-8, MC1408L-8)
- Seven and Six-Bit Accuracy Available (MC1408L-7, MC1408L-6)
- Fast Settling Time – 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing – +0.5 V to -5.0 V
- High-Speed Multiplying Input Slew Rate 4.0 mA/μs
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

MONOLITHIC SILICON INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

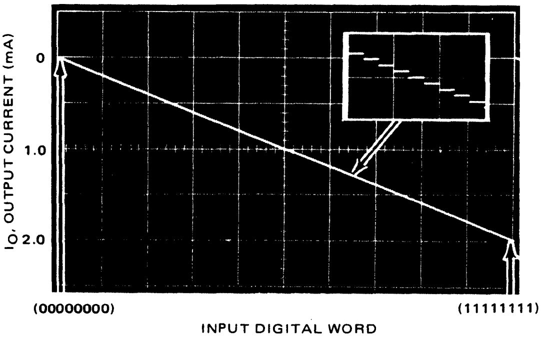
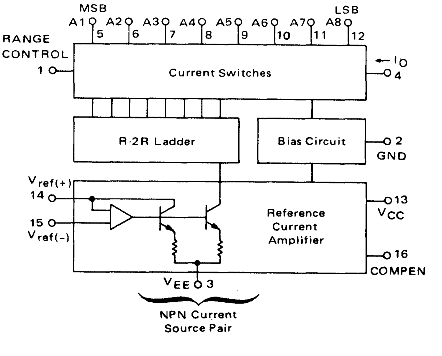


FIGURE 2 – BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	+5.5,0	Vdc
Applied Output Voltage	V_O	+0.5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14}, V_{15}	V_{CC}, V_{EE}	Vdc
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 1000 6.7	 mW mW/°C
Operating Temperature Range MC1508L-8 MC1408L Series	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R14}$ = 2.0 mA, MC1508L-8: T_A = -55°C to +125°C. MC1408L Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

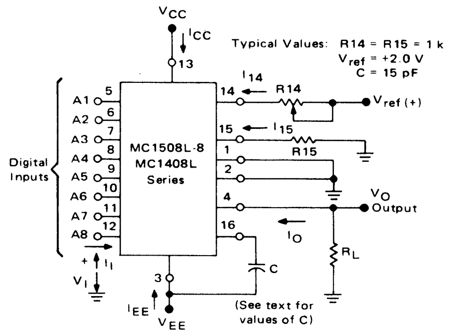
Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) MC1508L-8, MC1408L-8 MC1408L-7, See Note 1 MC1408L-6, See Note 1	4	E_r	 – – –	 – – –	 ±0.19 ±0.39 ±0.78	%
Settling Time to within 1/2 LSB [includes t_{PLH}](T_A=+25°C) See Note 2	5	t_S	–	300	–	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH}, t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	–20	–	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2.0 –	 – –	 – 0.8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3	 I_{IH} I_{IL}	 – –	 0 -0.4	 0.04 -0.8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	–	-1.0	-3.0	µA
Output Current Range V_{EE} = -5.0 V V_{EE} = -6.0 to -15 V	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{ref} = 2.000 V, R14 = 1000 Ω	3	I_O	 1.9	 1.99	 2.1	mA
Output Current (All bits low)	3	$I_{O(min)}$	–	0	4.0	µA
Output Voltage Compliance ($E_r \leq$ 0.19% at T_A = +25°C) Pin 1 grounded Pin 1 open, V_{EE} below -10 V	3	V_O	 – –	 – –	 -0.6,+0.5 -5.0,+0.5	Vdc
Reference Current Slew Rate	6	$SR\ I_{ref}$	–	4.0	–	mA/µs
Output Current Power Supply Sensitivity		PSRR(–)	–	0.5	2.7	µA/V
Power Supply Current (All bits low)	3	I_{CC} I_{EE}	– –	+13.5 -7.5	+22 -13	mA
Power Supply Voltage Range (T_A = +25°C)	3	V_{CCR} V_{EER}	+4.5 -4.5	+5.0 -15	+5.5 -16.5	Vdc
Power Dissipation All bits low V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc All bits high V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc	3	P_D	 – – – –	 105 190 90 160	 170 305 – –	mW

Note 1. All current switches are tested to guarantee at least 50% of rated output current.
Note 2. All bits switched.

8

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT



V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

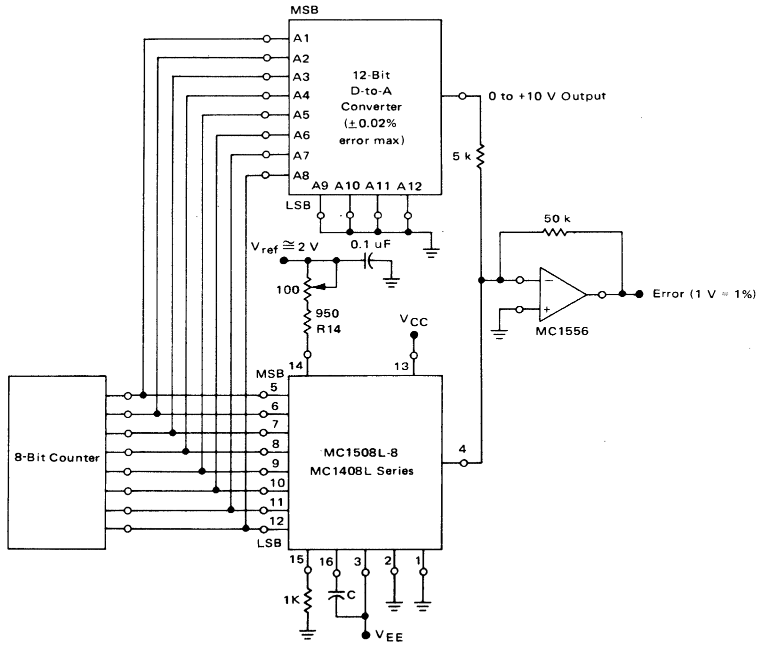
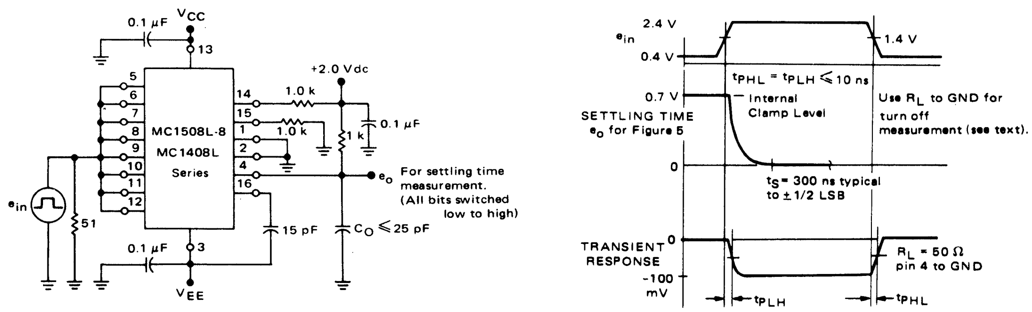


FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME



TEST CIRCUITS (continued)

FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT

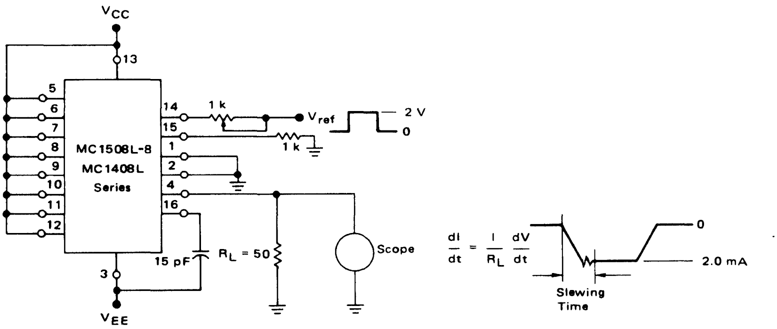


FIGURE 7 – POSITIVE V_{ref}

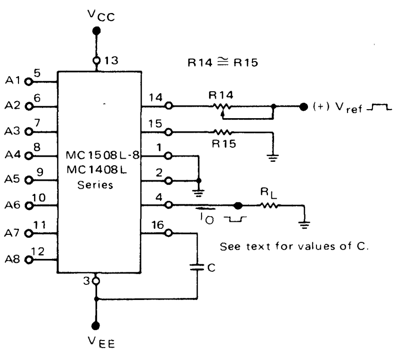


FIGURE 8 – NEGATIVE V_{ref}

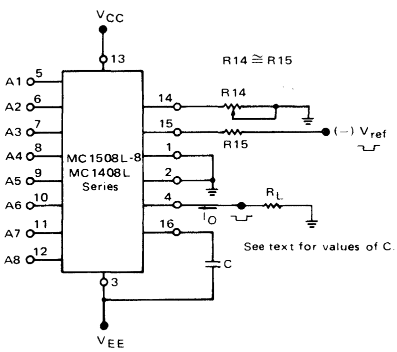


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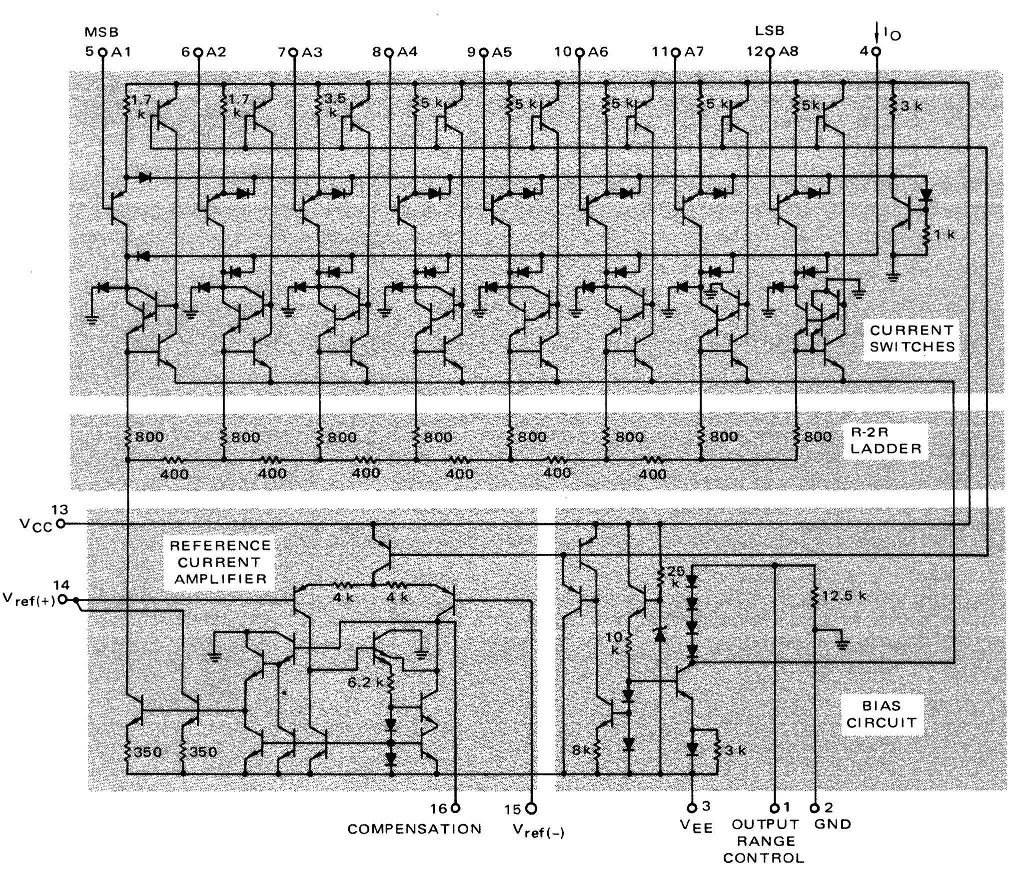
FIGURE 9 – MC1508L-8/MC1408L SERIES EQUIVALENT CIRCUIT SCHEMATIC



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CIRCUIT DESCRIPTION

The MC1508L-8 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0-volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.6 to +0.5 volts at +25°C, due to the current switching methods employed in the MC1508L-8. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1508L-8 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than -6.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1508L-8 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1508L-8 has a very low full scale current drift with temperature.

The MC1508L-8/MC1408L Series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1508L-8 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1508L-8 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1508L-8.

Multiplying Accuracy

The MC1508L-8 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μA to 4.0 mA, the 1.6 μA contributes an error of 0.1 LSB. This is well within eight-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1508L-8 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

GENERAL INFORMATION (Continued)

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leqslant 500$ ohms and $C_O \leqslant 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A6 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC-1508L-8. A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

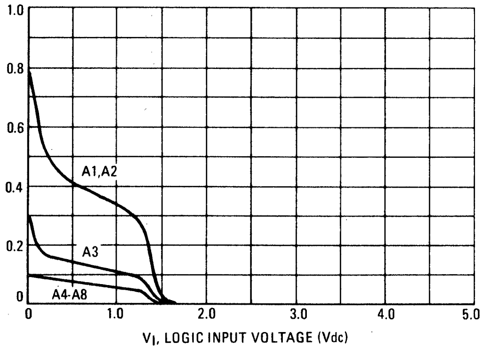


FIGURE 11 – TRANSFER CHARACTERISTIC versus TEMPERATURE
(A5 thru A8 thresholds lie within range for A1 thru A4)

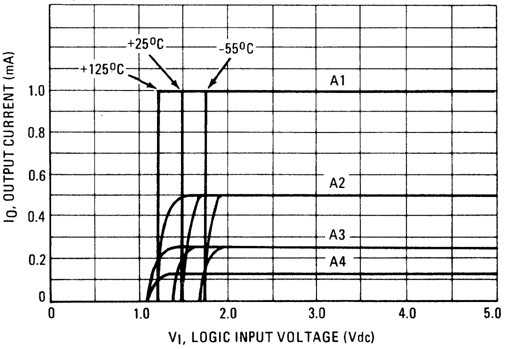


FIGURE 12 – OUTPUT CURRENT versus OUTPUT VOLTAGE
(See text for pin 1 restrictions)

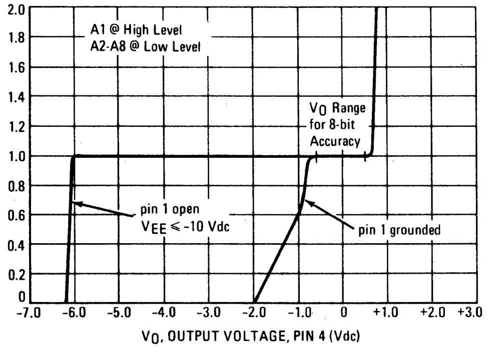
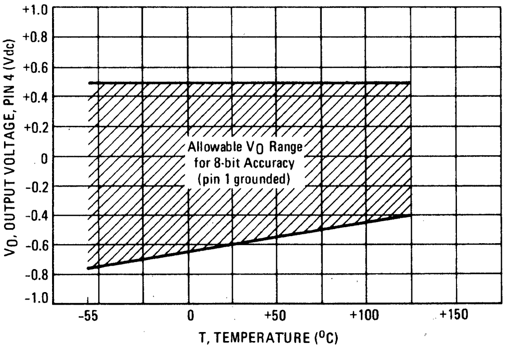


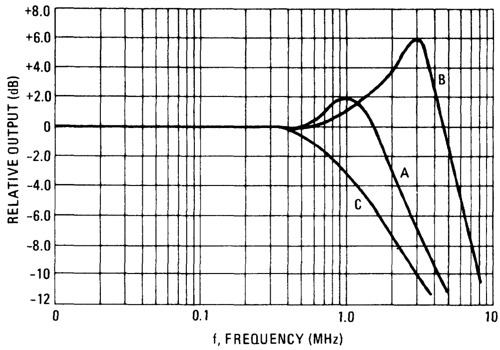
FIGURE 13 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE
(Negative range with pin 1 open is -5.0 Vdc over full temperature range)



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 14 – REFERENCE INPUT FREQUENCY RESPONSE



Unless otherwise specified:

$R14 = R15 = 1.0\ k\Omega$
C = 15 pF, pin 16 to V_{EE}
$R_L = 50\ \Omega$, pin 4 to GND

Curve A: Large Signal Bandwidth
Method of Figure 7
V_{ref} = 2.0 V(p-p) offset 1.0 V above GND

Curve B: Small Signal Bandwidth
Method of Figure 7 $R_L = 250\ \Omega$
V_{ref} = 50 mV(p-p) offset 200 mV above GND

Curve C: Large and Small Signal Bandwidth
Method of Figure 25 (no op-ampl, $R_L = 50\ \Omega$)
$R_S = 50\ \Omega$
V_{ref} = 2.0 V
V_S = 100 mV(p-p) centered at 0 V

FIGURE 15 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)

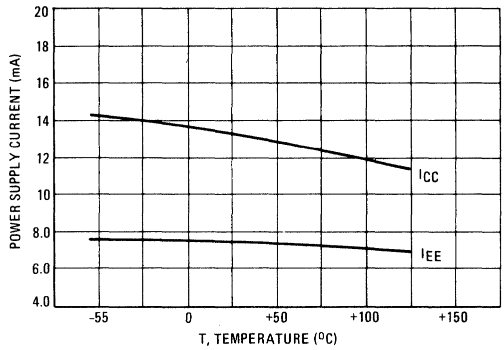
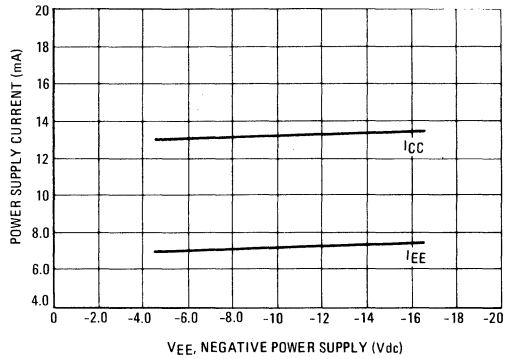
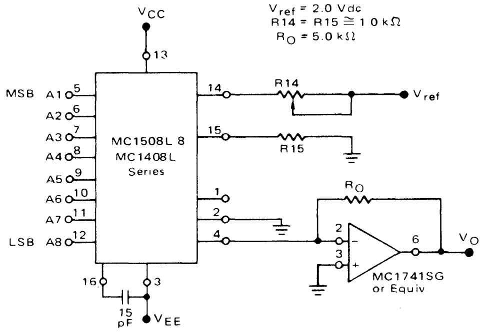


FIGURE 16 – TYPICAL POWER SUPPLY CURRENT versus V_{EE} (all bits low)



APPLICATIONS INFORMATION

FIGURE 17 – OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

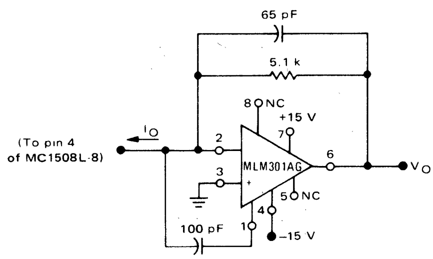
APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1508L-8 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

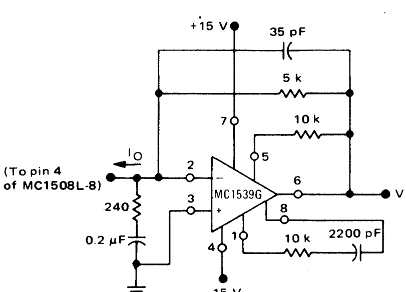
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 µs.

FIGURE 18



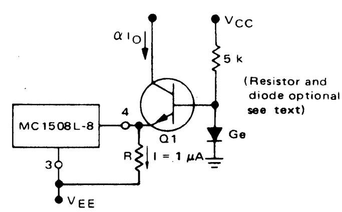
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 µs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because pin 4 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1508L-8 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the −5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from −2.0 to −8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

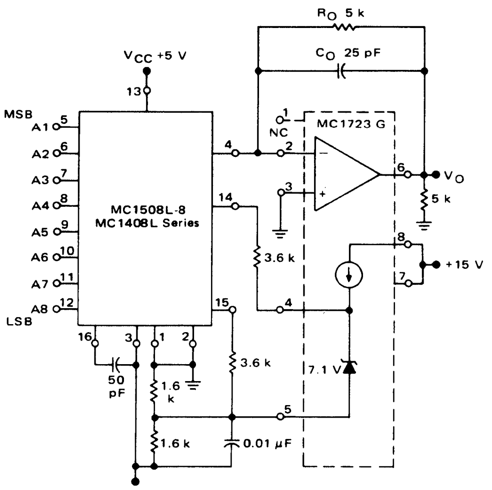
8

APPLICATIONS INFORMATION (continued)

Programmable Power Supply

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +25.5 volts in 0.1-volt increments, ±0.05 volt; or 0 to 5.1 volts in 20 mV increments, ±10 mV.

FIGURE 21 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



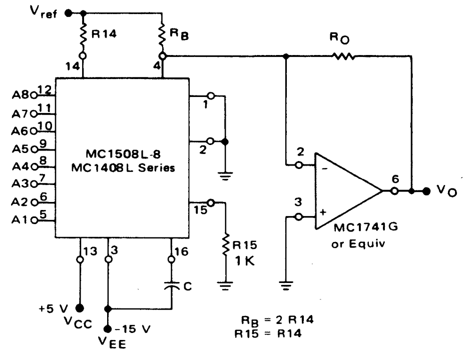
$$V_O = V_{ref} = \frac{R_O}{R12}\{A\}$$

Settling time for a 10-volt step ≅ 1.0 μs

Bipolar or Negative Output Voltage

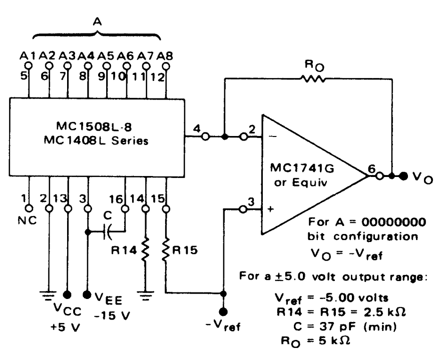
The circuit of Figure 22 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 8-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V(p-p) output range.

FIGURE 22 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right] - \frac{V_{ref}}{R_B}(R_O)$$

FIGURE 23 – BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



Decrease R_O to 2.5 kΩ for a 0 to -5.0-volt output range. This application provides somewhat lower speed, as previously discussed in the Output Voltage Range section of the General Information.

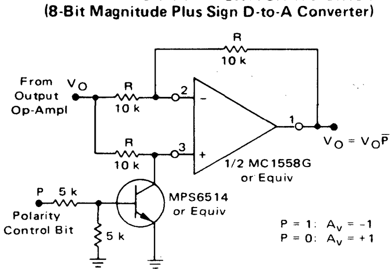
8

APPLICATIONS INFORMATION (continued)

Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8-bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and −1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 – POLARITY SWITCHING CIRCUIT (8-Bit Magnitude Plus Sign D-to-A Converter)



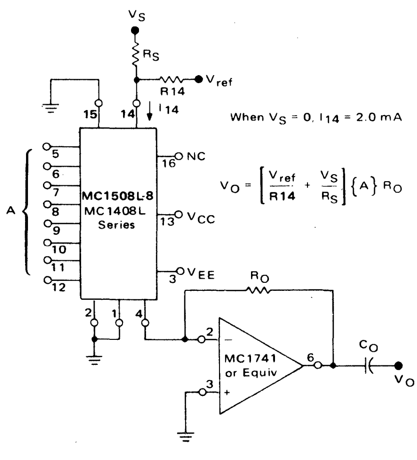
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1508L-8 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ±1.0 mA variation in relation to I_{14}. I_{14} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1508L-8 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref}.

FIGURE 26 – PANEL METER READOUT CIRCUIT

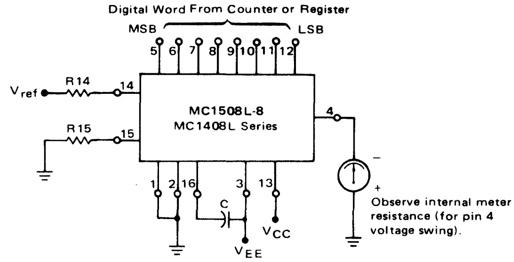
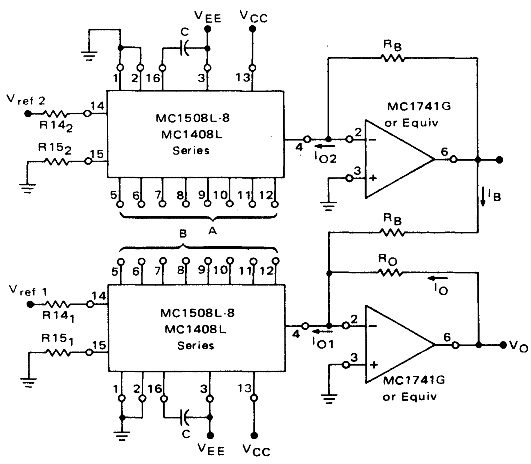


FIGURE 27 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



$$I_O = I_{O1} - I_{O2} = \frac{V_{ref\,1}}{R14_1}\{A\} - \frac{V_{ref\,2}}{R14_2}\{B\}$$

$I_{O2} = -I_B$

$I_B + I_O = I_{O1}$

Digital Subtraction:

Let $\frac{V_{ref\,1}}{R14_1} = \frac{V_{ref\,2}}{R14_2}$

Programmable Amplifier:
Connect Digital Inputs so A = B

$$\boxed{V_O = \frac{V_{ref\,1}}{R14_1} R_O [\{A\} - \{B\}]}$$

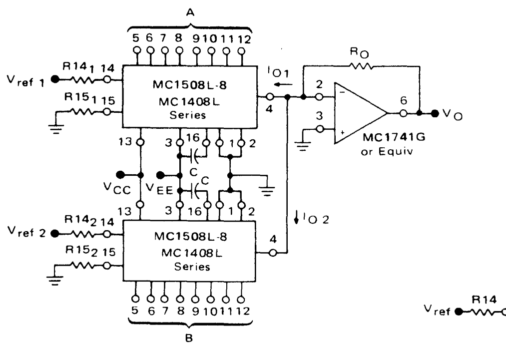
$$\boxed{V_O = \{A\}\left[\frac{V_{ref\,1}}{R14_1} - \frac{V_{ref\,2}}{R14_2}\right]}$$

APPLICATIONS INFORMATION (continued)

This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to $R14_1$ and $R14_2$ or $R15_1$ and $R15_2$. V_O will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect $R14_1$ and $R14_2$ to a positive reference higher than the most positive input, and drive $R15_1$ and $R15_2$. This yields high input impedance, bipolar differential and common-mode range.

FIGURE 28 – DIGITAL SUMMING and CHARACTER GENERATION



$V_O = (I_{O1} + I_{O2})\, R_O$

$$\boxed{V_O = \left[\frac{V_{ref\,1}}{R14_1}\{A\} + \frac{V_{ref\,2}}{R14_2}\{B\}\right] R_O}$$

In a character generation system one MC1508L-8 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 16-bit D-to-A converter (see Accuracy Section).

FIGURE 29 – POSITIVE PEAK DETECTING SAMPLE and HOLD
(Features indefinite hold time and optional digital output.)

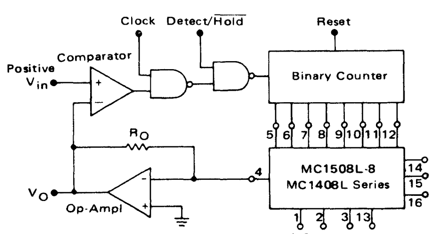
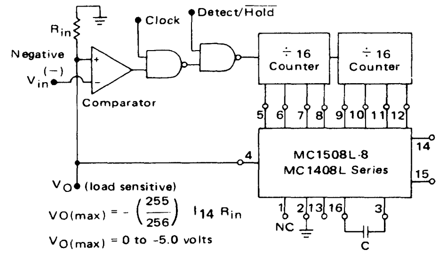


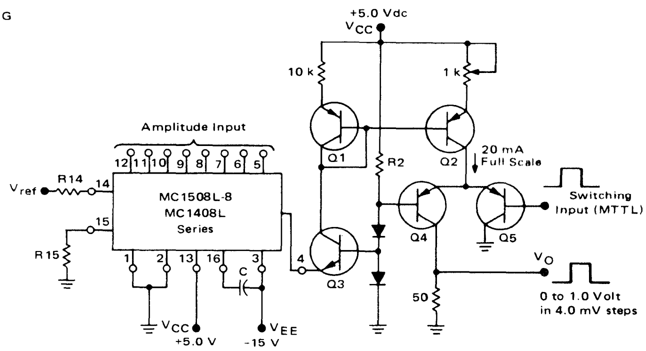
FIGURE 30 – NEGATIVE PEAK DETECTING SAMPLE AND HOLD



$V_{O(max)} = -\left(\frac{255}{256}\right) I_{14}\, R_{in}$

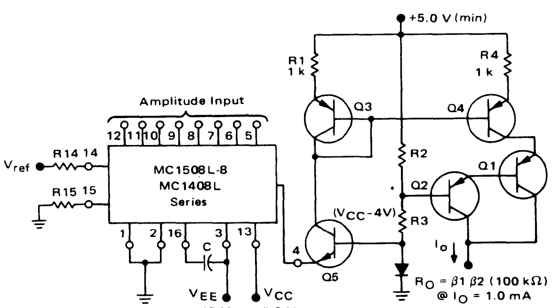
$V_{O(max)} = 0$ to -5.0 volts

FIGURE 31 – PROGRAMMABLE PULSE GENERATION



Fast rise and fall times require the use of high-speed switching transistors for the differential pair, Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input.

FIGURE 32 – PROGRAMMABLE CONSTANT CURRENT SOURCE



$R_O = \beta 1\, \beta 2$ (100 kΩ) @ $I_O = 1.0$ mA

*The base of Q2 must be at least 4 V below supply voltage.

Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

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APPLICATIONS INFORMATION (continued)

FIGURE 33 – ANALOG DIVISION BY DIGITAL WORD

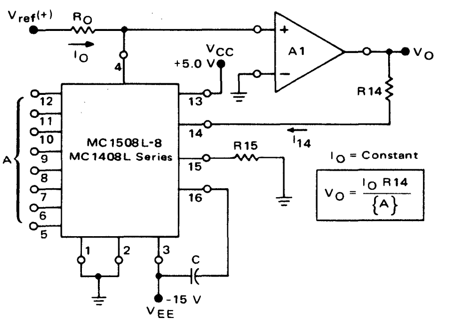
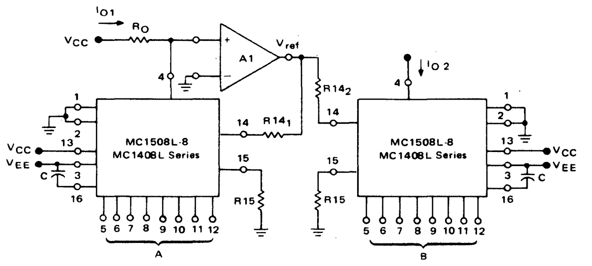


FIGURE 34 – ANALOG QUOTIENT OF TWO DIGITAL WORDS



$$V_{ref} = \frac{I_{O1} R14_1}{\{A\}}$$

$$I_{O2} = \frac{V_{ref}}{R14_2} \{B\}$$

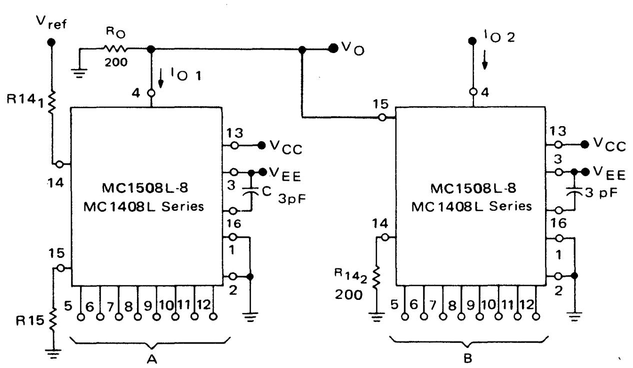
if $R14_1 = R14_2$

$$\boxed{I_{O2} = I_{O1} \frac{\{B\}}{\{A\}}}$$

This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, I_O can be set at 16 μA so that I_{14} will have a maximum value of 3.984 mA for a digital bit input configuration of 00000001.

Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If the MC1723 or another wideband amplifier is used, the reference amplifier should always be overcompensated.

FIGURE 35 – ANALOG PRODUCT OF TWO DIGITAL WORDS
(High-Speed Operation)



$$V_O = -I_{O1} R_O = \frac{V_{ref}}{R14_1} \{A\} R_O$$

$$I_{O2} = \frac{\{B\} |V_O|}{R14_2} = \frac{\{B\}}{R14_2} \left[R_O \left(\frac{V_{ref}}{R14_1} \right) \{A\} \right]$$

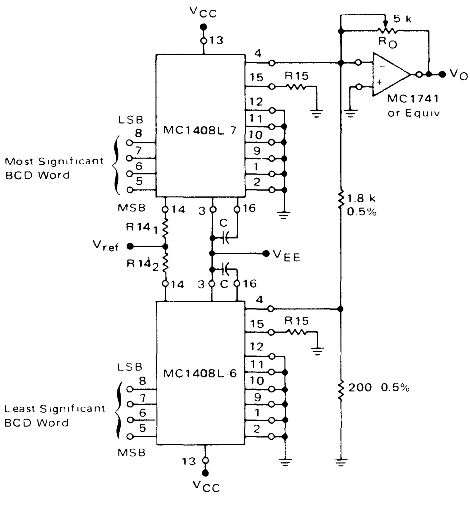
Since $R_O = R14_2$ and $K = \frac{V_{ref}}{R14_1}$

$\boxed{I_{O2} = K \{A\} \{B\}}$ K can be an analog variable.

8

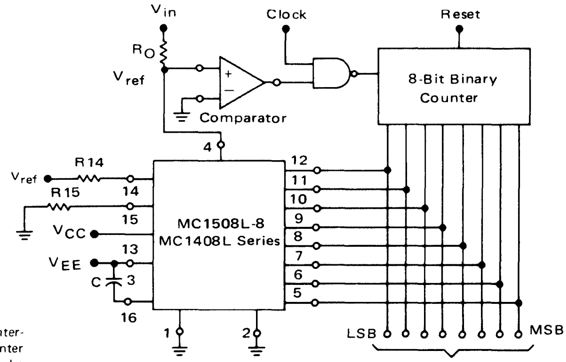
APPLICATIONS INFORMATION (continued)

FIGURE 36 – TWO-DIGIT BCD CONVERSION



Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an MC1408L-6 may be used for the least significant word.

FIGURE 37 – DIGITAL QUOTIENT OF TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION



$$C = \frac{V_{in}/R_O}{V_{ref}/R14}$$

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

8

MC1510G
MC1410G

HIGH-FREQUENCY CIRCUITS

WIDEBAND VIDEO AMPLIFIER

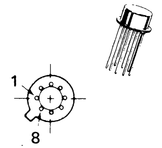
. . . designed for use as a high-frequency differential amplifier with operating characteristics that provide a flat frequency response from dc to 40 MHz.

- High Gain Characteristics
  A_V = 93 typ
- Wide Bandwidth – dc to 40 MHz typ
- Large Output Voltage Swing
  4.5 Vp-p typical @ ±6.0 V Supply
- Low Output Distortion
  THD ⩽ 1.5% typ

VIDEO AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT

METAL PACKAGE
CASE 601



(bottom view)

FIGURE 1 – VOLTAGE GAIN versus FREQUENCY

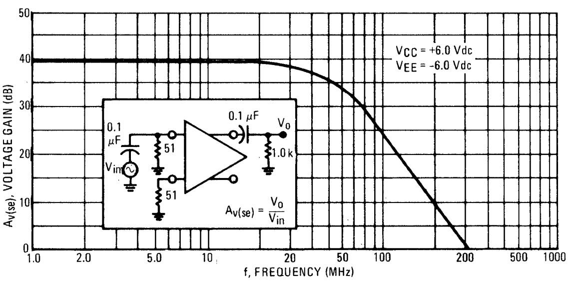
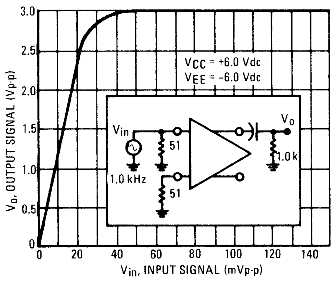
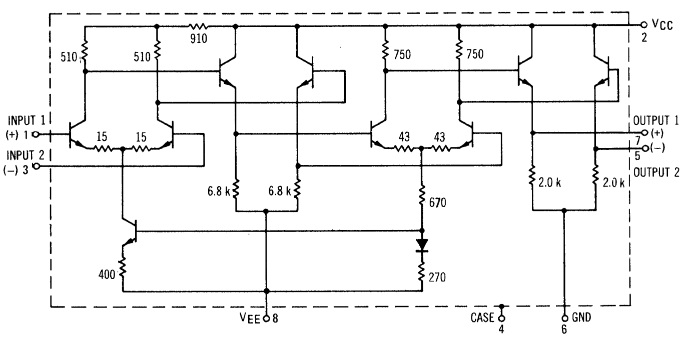


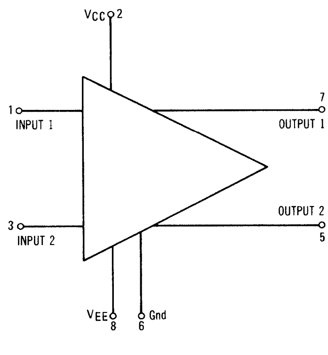
FIGURE 2 – LIMITING CHARACTERISTICS @ 1.0 kHz



CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 -8.0	Vdc Vdc
Differential Input Signal	V_{IDR}	±5.0	Volts
Common Mode Input Swing	V_{ICR}	±6.0	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_s	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C	P_D	 680 4.6	 mW mW/°C
Operating Temperature Range MC1410 MC1510	T_A	 0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, R_L = 5.0 kΩ, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1510 Min	MC1510 Typ	MC1510 Max	MC1410 Min	MC1410 Typ	MC1410 Max	Unit
Single Ended Voltage Gain	$A_{v(se)}$	75	93	110	60	90	120	V/V
Output Impedance (f = 20 kHz)	Z_{out}	–	35	–	–	35	–	Ω
Input Impedance (f = 20 kHz)	Z_{in}	–	6.0	–	–	6.0	–	kΩ
Bandwidth (-3.0 dB)	BW	–	40	–	–	40	–	MHz
Output Voltage Swing (f = 100 kHz)	V_o	–	4.5	–	–	4.5	–	Vp-p
Single Ended Output Distortion (e_{in} < 0.2% Distortion)	THD	–	1.5	5.0	–	2.0	–	%
Input Common Mode Voltage Range	V_{ICR}	–	±1.0	–	–	±1.0	–	V
Common Mode Voltage Gain (V_{in} = 0.3 V rms, f = 100 kHz)	AV_{CM}	-30	-45	–	-20	-40	–	dB
Common Mode Rejection Ratio	CMRR	–	85	–	–	85	–	dB
Input Bias Current $\left(I_{IB} = \frac{I_1 + I_2}{2}\right)$, Differential Output = 0	$\lvert I_{IB} \rvert$	–	20	80	–	50	100	µA
Input Offset Current ($I_{IO} = I_1 - I_2$)	$\lvert I_{IO} \rvert$	–	3.0	20	–	5.0	30	µA
Output Offset Voltage Differential Mode (V_{in} = 0) Common Mode (Differential Output = 0)	 $V_{OO(DM)}$ $V_{OO(CM)}$	 – 2.6	 0.5 3.1	 1.3 3.5	 – 2.0	 0.5 3.0	 2.0 4.0	Vdc
Step Response	t_{THL} t_{PHL}, t_{PLH} t_{TLH}	– – –	9.0 9.0 9.0	12 – 12	– – –	10 9.0 10	15 – 15	ns
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low}* to T_{high}**) ($R_S \leq$ 10 k Ω, T_A = T_{low} to T_{high})	$\Delta V_{IO}/\Delta T$	 – –	 ±3.0 ±6.0	 – –	 – –	 ±3.0 ±6.0	 – –	µV/°C
DC Power Dissipation (Power Supply = ±6.0 V)	P_D	–	150	220	–	165	220	mW
Equivalent Average Input Noise Voltage (f = 10 Hz to 500 kHz, R_S = 0)	V_n	–	6.0	–	–	5.0	–	µV

*T_{low} = 0°C for MC1410 or −55°C for MC1510

**T_{high} = +75°C for MC1410 or +125°C for MC1510

8

TYPICAL CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3
POWER DISSIPATION versus SUPPLY VOLTAGE

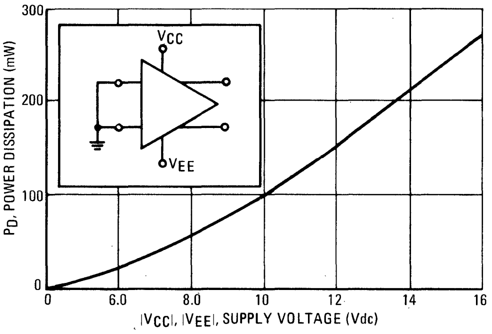


FIGURE 4
VOLTAGE GAIN versus SUPPLY VOLTAGE

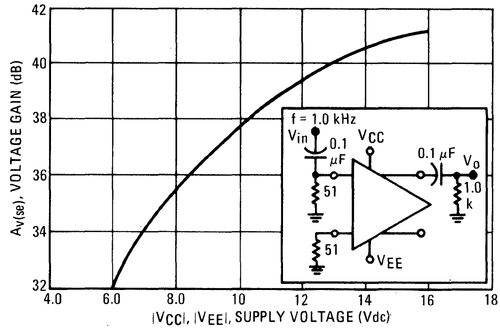


FIGURE 5
VOLTAGE GAIN versus TEMPERATURE

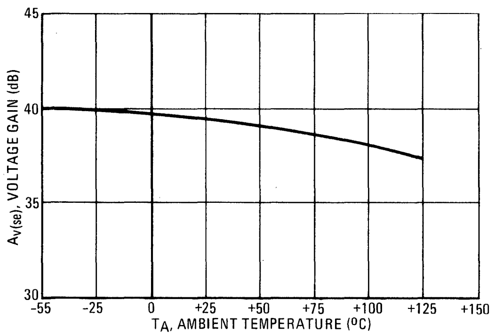


FIGURE 6
DC OUTPUT VOLTAGE versus TEMPERATURE

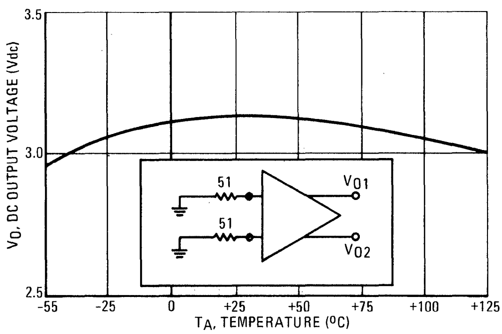


FIGURE 7
INPUT BIAS CURRENT versus TEMPERATURE

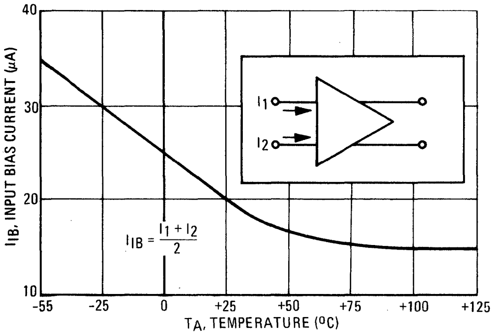
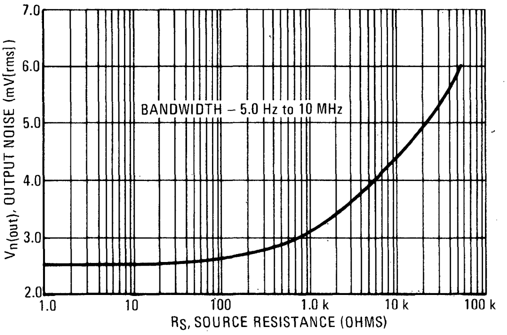


FIGURE 8
OUTPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



TYPICAL CHARACTERISTICS

FIGURE 9
LIMITING CHARACTERISTICS @ 30 MHz

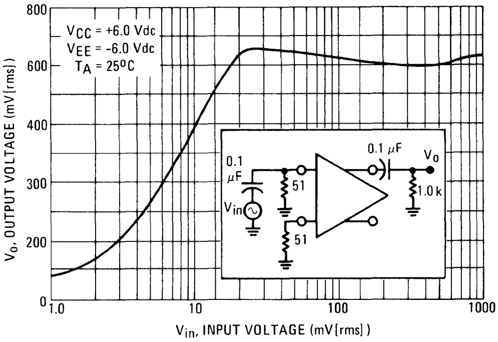
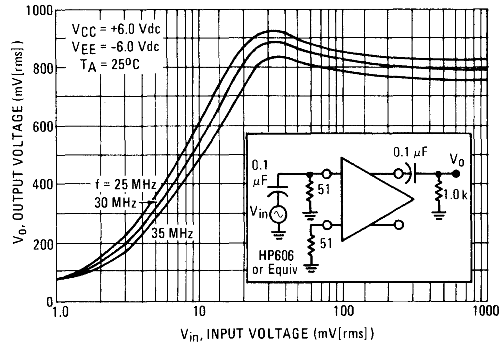


FIGURE 10
LIMITING CHARACTERISTICS versus FREQUENCY



TYPICAL APPLICATIONS

FIGURE 11
ENVELOPE DETECTOR

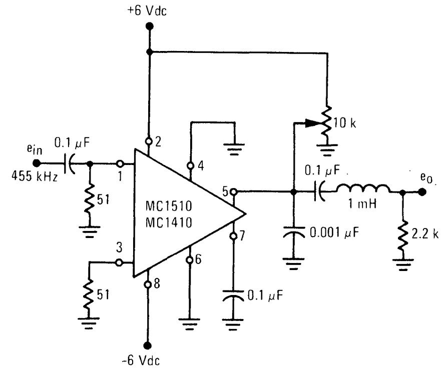


FIGURE 12
SINGLE STAGE WIDEBAND AMPLIFIER

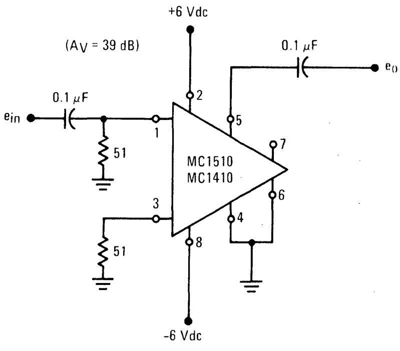
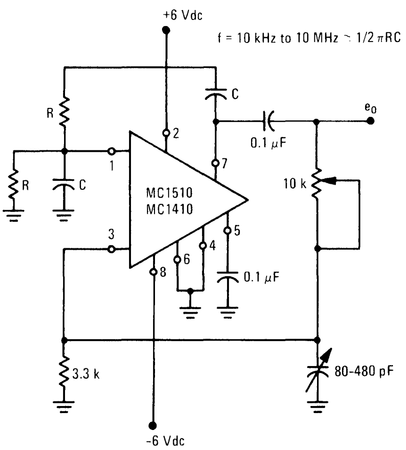


FIGURE 13
WEIN BRIDGE OSCILLATOR



8

MC1514
MC1414

DUAL DIFFERENTIAL COMPARATOR

DUAL DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

- Two Separate Outputs
- Strobe Capability
- High Output Sink Current
  2.8 mA Minimum (Each Comparator) for MC1514
  1.6 mA minimum (Each Comparator) for MC1414
- Differential Input Characteristics
  Input Offset Voltage = 1.0 mV for MC1514
  = 1.5 mV for MC1414
  Offset Voltage Drift = 3.0 μV/^{o}C for MC1514
  = 5.0 μV/^{o}C for MC1414
- Short Propagation Delay Time — 40 ns typical
- Output Compatible with All Saturating Logic Forms
  V_O = +3.2 V to -0.5 V typical

DUAL DIFFERENTIAL COMPARATOR

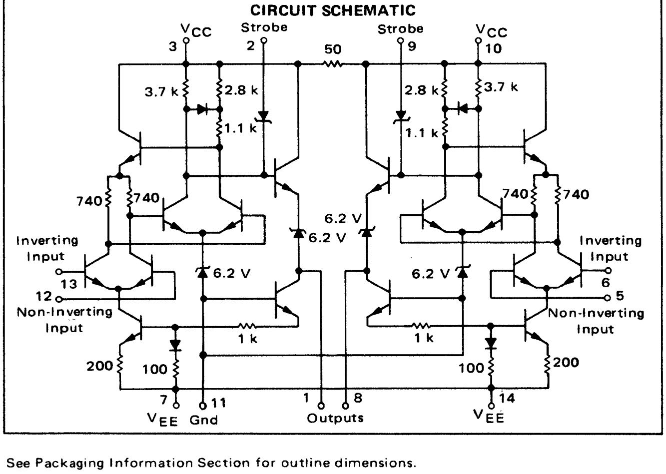
(DUAL MC1710)

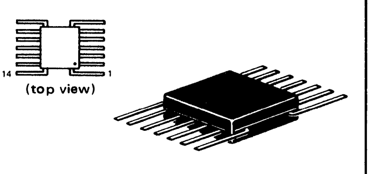
MONOLITHIC SILICON INTEGRATED CIRCUIT

MAXIMUM RATINGS (T_A = 25^{o}C unless otherwise noted.)

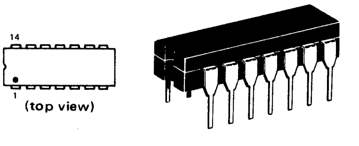
Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+14 -7.0	Vdc
Differential Mode Input Voltage Range	V_{IDR}	±5.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	±7.0	Vdc
Peak Load Current	I_L	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		1000	mW
Derate above T_A = 25^{o}C		6.0	mW/^{o}C
Ceramic Flat Package		500	mW
Derate above T_A = 25^{o}C		3.3	mW/^{o}C
Plastic Dual In-Line Package		625	mW
Derate above T_A = 25^{o}C		5.0	mW/^{o}C
Operating Temperature Range MC1514 MC1414	T_A	-55 to +125 0 to +75	^{o}C
Storage Temperature Range	T_{stg}	-65 to +150	^{o}C

CIRCUIT SCHEMATIC

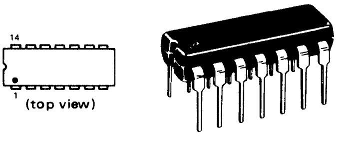




F SUFFIX
CERAMIC PACKAGE
CASE 607



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1414 only)

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = -6 Vdc, T_A = 25°C unless otherwise noted.) (Each Comparator)

Characteristic	Symbol	MC1514 Min	MC1514 Typ	MC1514 Max	MC1414 Min	MC1414 Typ	MC1414 Max	Unit
Input Offset Voltage (V_O = 1.4 Vdc, T_A = 25°C) (V_O = 1.8 Vdc, T_A = T_{low}*) (V_O = 1.0 Vdc, T_A = T_{high}*)	V_{IO}	 — — —	 1.0 — —	 2.0 3.0 3.0	 — — —	 1.5 — —	 5.0 6.5 6.5	mVdc
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	3.0	—	—	5.0	—	μV/°C
Input Offset Current (V_O = 1.4 Vdc, T_A = 25°C) (V_O = 1.8 Vdc, T_A = T_{low}) (V_O = 1.0 Vdc, T_A = T_{high})	I_{IO}	 — — —	 1.0 — —	 3.0 7.0 3.0	 — — —	 1.0 — —	 5.0 7.5 7.5	μAdc
Input Bias Current (V_O = 1.4 Vdc, T_A = 25°C) (V_O = 1.8 Vdc, T_A = T_{low}) (V_O = 1.0 Vdc, T_A = T_{high})	I_{IB}	 — — —	 12 — —	 20 45 20	 — — —	 15 18 —	 25 40 40	μAdc
Open Loop Voltage Gain (T_A = 25°C) (T_A = T_{low} to T_{high})	A_{vol}	 1250 1000	 1700 —	 — —	 1000 800	 1500 —	 — —	V/V
Output Resistance	R_O	—	200	—	—	200	—	ohms
Differential Voltage Range	V_{IDR}	±5.0	—	—	±5.0	—	—	Vdc
High Level Output Voltage (V_{ID} ⩾ 5.0 mV, 0 ⩽ I_O ⩽ 5.0 mA)	V_{OH}	2.5	3.2	4.0	2.5	3.2	4.0	Vdc
Low Level Output Voltage (V_{ID} ⩾ -5.0 mV, I_{OS} = 2.8 mA) (V_{ID} ⩾ -5.0 mV, I_{OS} = 1.6 mA)	V_{OL}	 -1.0 —	 -0.5 —	 0 —	 — -1.0	 — -0.5	 — 0	Vdc
Output Sink Current (V_{ID} ⩾ -5.0 mV, V_{OL} ⩽ 0.4 V, T_A = T_{low} to T_{high})	I_{OS}	2.8	3.4	—	1.6	2.5	—	mAdc
Input Common Mode Voltage Range (V_{EE} = -7.0 Vdc)	V_{ICR}	±5.0	—	—	±5.0	—	—	Vdc
Common-Mode Rejection Ratio (V_{EE} = -7.0 Vdc, R_S ⩽ 200 Ω)	CMRR	80	100	—	70	100	—	dB
Strobe Low Level Current (V_{IL} = 0)	I_{IL}	—	—	2.5	—	—	2.5	mA
Strobe High Level Current (V_{IH} = 5.0 Vdc)	I_{IH}	—	—	1.0	—	—	1.0	μA
Strobe Disable Voltage (V_{OL} ⩽ 0.4 Vdc)	V_{IL}	—	—	0.4	—	—	0.4	Vdc
Strobe Enable Voltage (V_{OH} ⩾ 2.4 Vdc)	V_{IH}	3.5	—	6.0	3.5	—	6.0	Vdc
Propagation Delay Time (Figure 1)	t_{PLH} t_{PHL}	— —	20 40	— —	— —	20 40	— —	ns
Strobe Response Time (Figure 2)	t_{so} t_{sr}	— —	15 6.0	— —	— —	15 6.0	— —	ns
Total Power Supply Current, Both Comparators (V_O ⩽ 0)	I_{CC} I_{EE}	— —	12.8 11	18 14	— —	12.8 11	18 14	mAdc
Total Power Consumption, Both Comparators	P_D	—	230	300	—	230	300	mW

*T_{low} = -55°C for MC1514, 0°C for MC1414
T_{high} = +125°C for MC1514, +75°C for MC1414

FIGURE 1 – PROPAGATION DELAY TIME

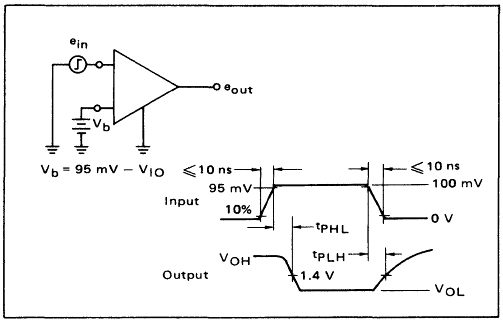
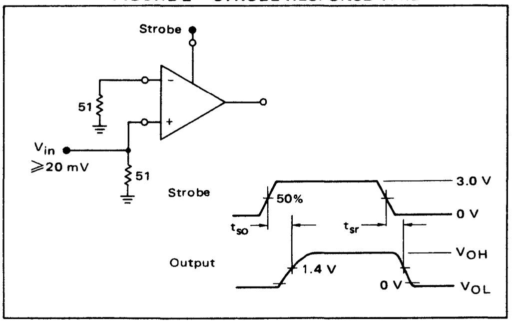


FIGURE 2 – STROBE RESPONSE TIME



8

TYPICAL CHARACTERISTICS
(Each Comparator)

FIGURE 3 – VOLTAGE TRANSFER CHARACTERISTICS

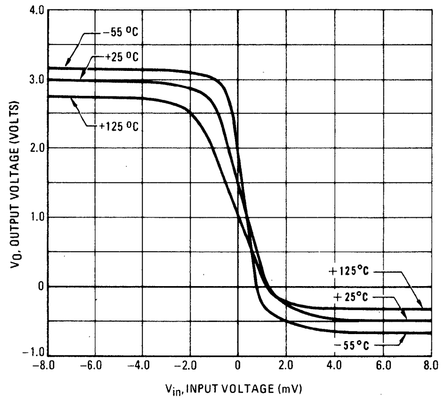


FIGURE 4 – INPUT OFFSET VOLTAGE versus TEMPERATURE

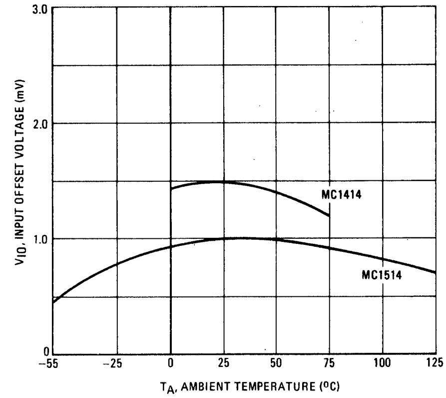


FIGURE 5 – INPUT OFFSET CURRENT versus TEMPERATURE

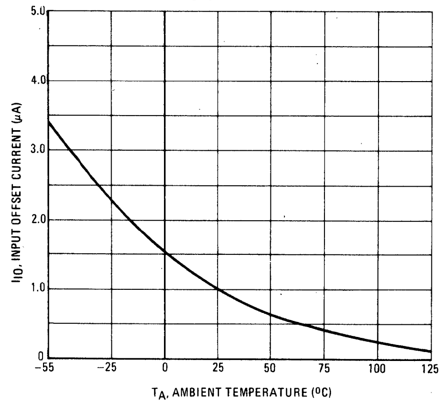


FIGURE 6 – INPUT BIAS CURRENT versus TEMPERATURE

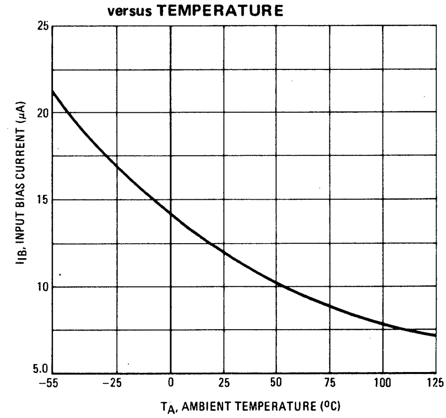


FIGURE 7 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

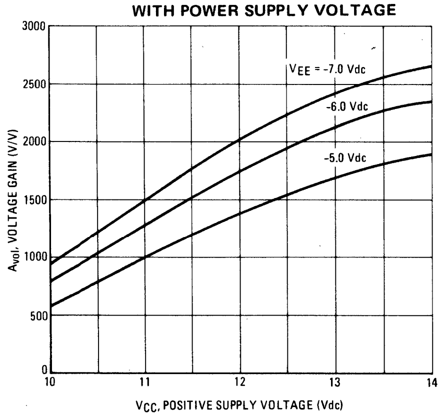
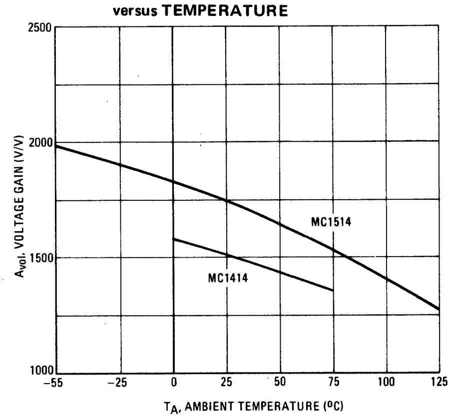


FIGURE 8 – VOLTAGE GAIN versus TEMPERATURE



8

FIGURE 9 – RESPONSE TIME

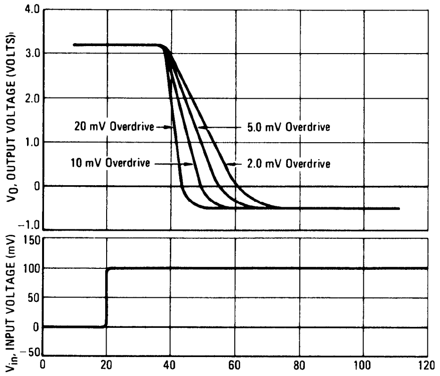


FIGURE 10 – POWER DISSIPATION versus TEMPERATURE

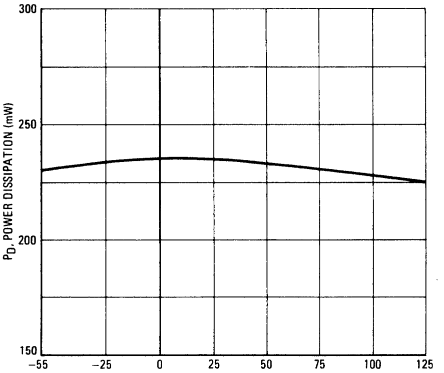


FIGURE 11 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

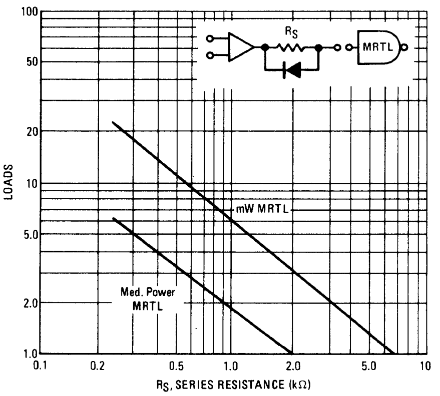


FIGURE 12 – SINK CURRENT versus TEMPERATURE

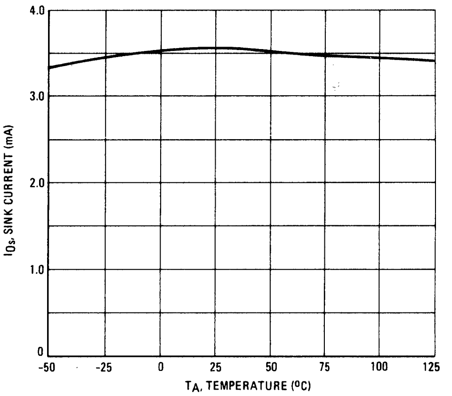
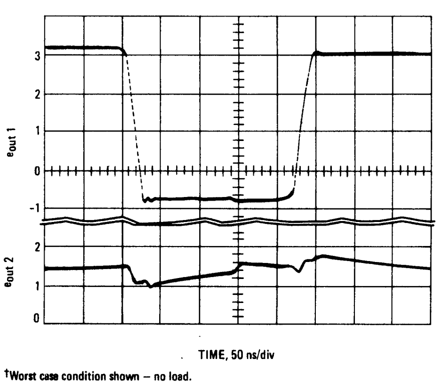
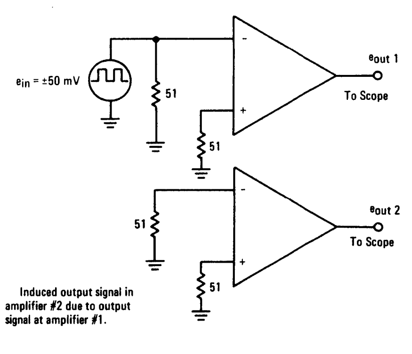


FIGURE 13 – CROSSTALK†





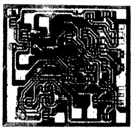
†Worst case condition shown – no load.

8

OPERATIONAL AMPLIFIERS

MC1520
MC1420

MONOLITHIC DIFFERENTIAL OUTPUT OPERATIONAL AMPLIFIER



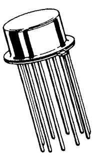
. . . designed for use in general-purpose or wide-band differential amplifier applications, especially those requiring differential outputs.

Typical Characteristics

- Differential Input and Differential Output
- Wide Closed-Loop Bandwidth; 10 MHz
- Differential Gain; 70 dB
- High Input Impedance; 2.0 megohms:
- Low Output Impedance; 50 ohms

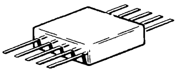
OPERATIONAL AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



Pin 3 connected to case

G SUFFIX
METAL PACKAGE
CASE 602A



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+8.0 -8.0	Vdc
Differential Input Signal	V_{in}	±8.0	Vdc
Load Current	I_{L1}, I_{L2}	15	mA
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Flat Package Derate above T_A = +25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range MC1520 MC1420	T_A	-55 to +125 0 to + 75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATICS

FIGURE 1 – CIRCUIT SCHEMATIC

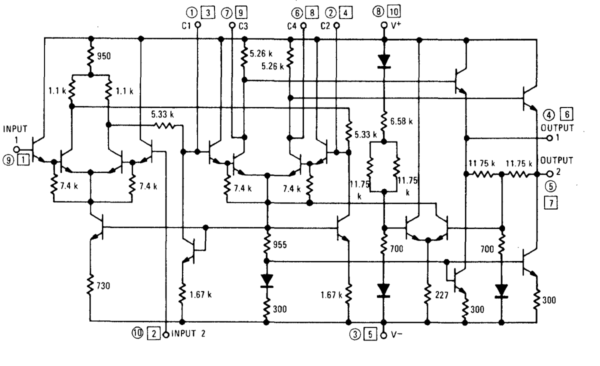
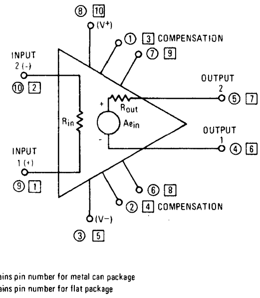


FIGURE 2 – EQUIVALENT CIRCUIT



○ contains pin number for metal can package
□ contains pin number for flat package

See Packaging Information Section for outline dimensions.

SINGLE-ENDED ELECTRICAL CHARACTERISTICS

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1520 Min	MC1520 Typ	MC1520 Max	MC1420 Min	MC1420 Typ	MC1420 Max	Unit
Open Loop Voltage Gain (T_{low} ② $\leq T_A \leq T_{high}$ ②)	A_{VOL}	1000 60	1500 64	– –	750 –	1500 64	– –	V/V dB
Output Impedance (f = 20 Hz)	Z_{out}	–	50	100	–	50	–	ohms
Input Impedance (f = 20 Hz)	Z_{in}	0.5	2.0	–	–	2.0	–	megohms
Output Voltage Swing (R_L = 7.0 kΩ [Figure 8])	V_o	±3.5	±4.0	–	±3.0	±4.0	–	V_{peak}
Input Common-Mode Voltage Swing	CMV_{in}	±2.0	±3.0	–	–	±3.0	–	V_{peak}
Common-Mode Rejection Ratio	CM_{rej}	75	90	–	60	90	–	dB
Input Bias Current $\left(\left[I_b = \frac{I_1 + I_2}{2}\right], T_A = +25^\circ C\right)$	I_b	–	0.8	2.0	–	2.0	40	µA
Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, $T_A = T_{low}$) ($I_{io} = I_1 - I_2$, $T_A = T_{high}$)	$\|I_{io}\|$	– – –	30 – –	100 200 200	– – –	30 – –	200 – –	nA
Input Offset Voltage (T_A = +25°C)	$\|V_{io}\|$	–	5.0	10	–	5.0	15	mV
Step Response Gain = 1.0, 10% Overshoot R_1 = 10 kΩ R_2 = 10 kΩ R_3 = 5.0 kΩ C_s = 39 pF	t_f t_{pd} dV_{out}/dt ①	– – –	80 70 5.0	– – –	– – –	80 70 5.0	– – –	ns ns V/µs
Gain = 10, 10% Overshoot R_1 = 10 kΩ R_2 = 100 kΩ R_3 = 10 kΩ C_s = 10 pF	t_f t_{pd} dV_{out}/dt ①	– – –	80 70 15	– – –	– – –	80 70 15	– – –	ns ns V/µs
Gain = 100, No Overshoot R_1 = 1.0 kΩ R_2 = 100 kΩ R_3 = 1.0 kΩ C_s = 1.0 pF	t_f t_{pd} dV_{out}/dt ①	– – –	80 70 30	– – –	– – –	80 70 30	– – –	ns ns V/µs
Open Loop, No Overshoot R_1 = 50 Ω R_2 = ∞ R_3 = 50 Ω C_s = 0	t_f t_{pd} dV_{out}/dt ①	– – –	180 70 35	– – –	– – –	180 70 35	– – –	ns ns V/µs
Bandwidth: (Open Loop [Figure 4]) (Closed Loop [Unity Gain]) (Figure 5)	–	– –	2.0 10	– –	– –	2.0 10	– –	MHz
Input Noise Voltage (Open Loop) (5.0 Hz - 5.0 MHz)	$V_{n(in)}$	–	11	15	–	11	–	µV(rms)
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low} to T_{high})	$\|TCV_{io}\|$	–	2.0	–	–	2.0	–	µV/°C
DC Power Dissipation (V_o = 0)	P_D	–	120	240	–	120	240	mW
Power Supply Sensitivity ($V^{\pm}$ Constant)	$S^{\pm}$	–	250	450	–	250	–	µV/V

① dV_{out}/dt = Slew Rate ② T_{low} = 0°C for MC1420, -55°C for MC1520; T_{high} = +75°C for MC1420, +125°C for MC1520

DIFFERENTIAL ELECTRICAL CHARACTERISTICS

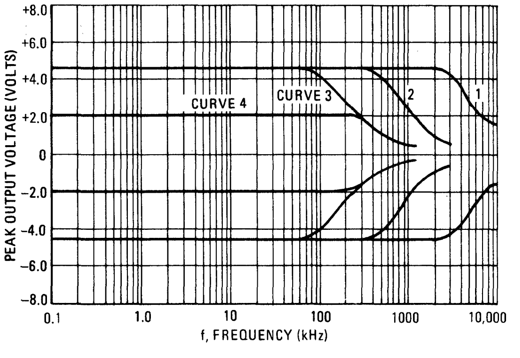
(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1520 Min	MC1520 Typ	MC1520 Max	MC1420 Min	MC1420 Typ	MC1420 Max	Unit
Gain (Open Loop)	A_{VOL}	2000 66	3000 70	– –	1500 64	3000 70	– –	V/V dB
Input Impedance (f = 20 Hz)	Z_{in}	0.5	2.0	–	–	2.0	–	megohms
Output Impedance (f = 20 Hz)	Z_{out}	–	100	200	–	100	–	ohms
Common-Mode Output Voltage	V_o (CM)	-0.5	0	+0.5	–	0	–	Vdc
Output Voltage Swing (R_L = 7.0 kΩ)	V_o	±7.0	±8.0	–	±6.0	±8.0	–	V_{peak}

TYPICAL CHARACTERISTICS

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY



TEST CIRCUIT

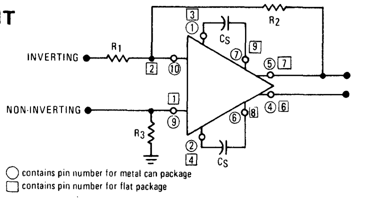


FIGURE NO.	CURVE NO.	MODE	VOLTAGE GAIN	TEST CONDITIONS R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_S (pF)	NOISE OUTPUT mV (rms)
3	1	INVERTING	100	1.0 k	100 k	1.0 k	1.0	2.0
	2	INVERTING	10	10 k	100 k	10 k	10	0.55
	3	INVERTING	1.0	10 k	10 k	5.0 k	39	0.17
	4	NON-INVERTING	1.0	∞	10 k	10 k	39	0.17
4	1	NON-INVERTING	A_{VOL}	0	∞	50	1.0	1.0
	2	NON-INVERTING	A_{VOL}	0	∞	50	10	2.0
	3	NON-INVERTING	A_{VOL}	0	∞	50	39	5.2
5	1	NON-INVERTING	100	100	10 k	100	1.0	2.0
	2	NON-INVERTING	10	1.0 k	9.1 k	910	10	0.55
	3	NON-INVERTING	1.0	∞	10 k	10 k	39	0.17

FIGURE 4 – OPEN LOOP VOLTAGE GAIN

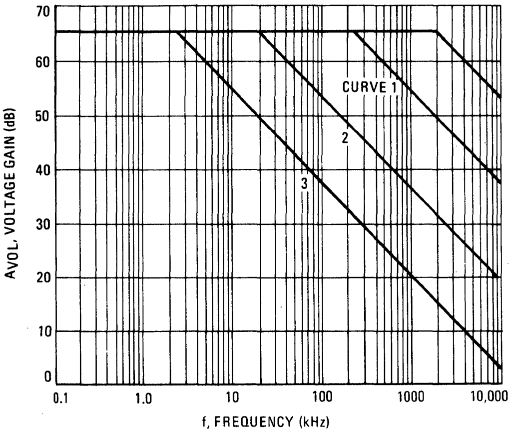
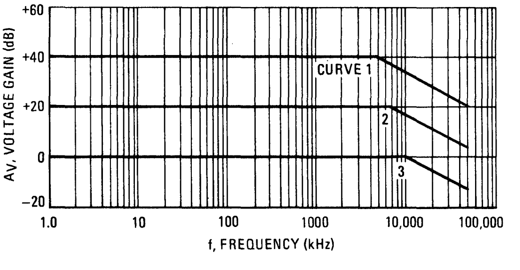


FIGURE 5 – CLOSED LOOP VOLTAGE GAIN versus FREQUENCY



8

TYPICAL OUTPUT CHARACTERISTICS

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, unless otherwise noted.)

FIGURE 6 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

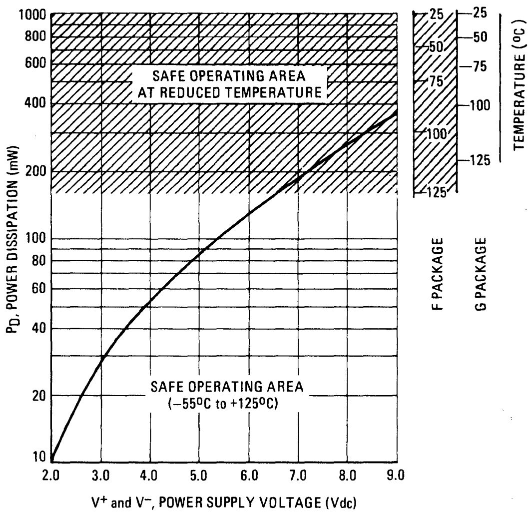


FIGURE 7 – OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

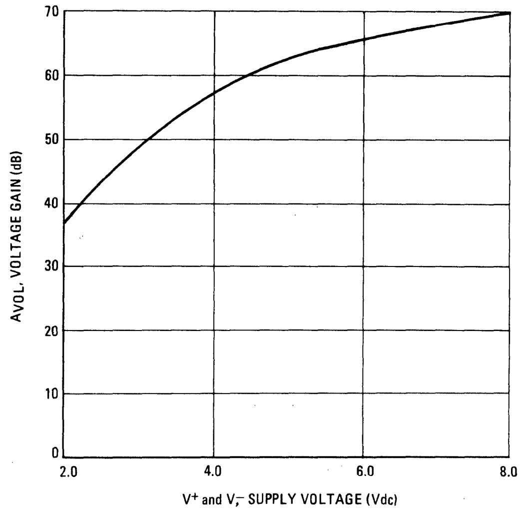


FIGURE 8 – SINGLE ENDED OUTPUT VOLTAGE versus LOAD RESISTANCE

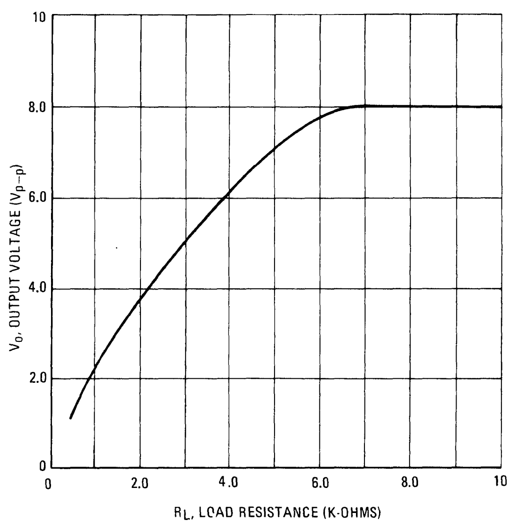
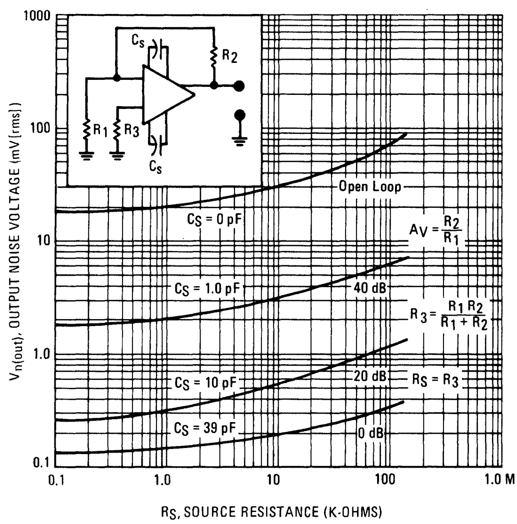


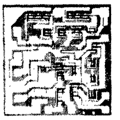
FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



8

MC1530, MC1430
MC1531, MC1431

MONOLITHIC OPERATIONAL AMPLIFIER

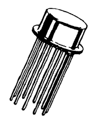


. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

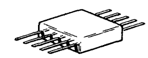
The MC1531 (MC1431) is provided with Darlington inputs to increase input impedance; otherwise the MC1531 (MC1431) circuit is identical with the MC1530 (MC1430) circuit.

- High Open Loop Voltage Gain – 4500 min (MC1530)
  – 2500 min (MC1531)
- High Input Impedance – 10 Kilohms min (MC1530)
  – 1.0 Megohm min (MC1531)
- Low Output Impedance – 50 Ohms max
- High Slew Rate – 6.0 V/μs typ @ A_{VS} = 10
- High Open Loop Bandwidth – 2.0 MHz typ (MC1530)
  0.4 MHz typ (MC1531)

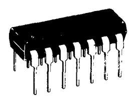
OPERATIONAL AMPLIFIERS INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 602B



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



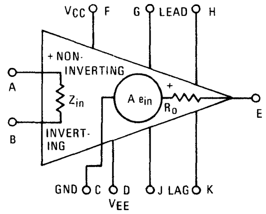
P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1430P/MC1431P only)

MAXIMUM RATINGS (T_A = 25°C unless otherwsie noted)

Rating	Symbol	Value	Unit
Power Supply Voltage MC1530, MC1531 MC1430, MC1431	V_{CC}, V_{EE} V_{CC}, V_{EE}	+9.0, -9.0 +8.0, -8.0	Vdc
Differential Input Signal	V_{ID}(max)	± 5.0	Volts
Load Current	I_L	10	mA
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Flat Package Derate above T_A = +25°C Dual In-Line Plastic Package MC1430, MC1431 Derate above +25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range MC1530, MC1531 MC1430, MC1431	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range Metal and Ceramic Package Plastic Package MC1430, MC1431	T_{stg}	 -65 to +175 -55 to +150	°C

CIRCUIT SCHEMATICS

FIGURE 1 – EQUIVALENT CIRCUIT BOTH TYPES



PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"F" & "G" Pkgs.	1	2	3	4	5	6	7	8	9	10
"P" Package	4	6	8	7	11	12	13	14	1	2

FIGURE 2 – MC1530/MC1430 (STANDARD INPUT)

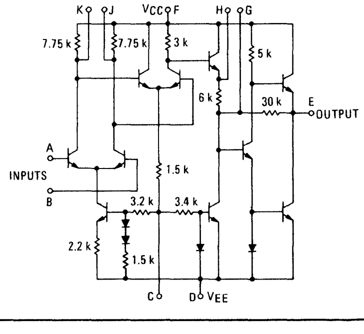
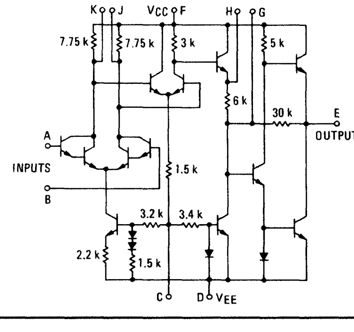


FIGURE 3 – MC1531/MC1431 (DARLINGTON INPUT)



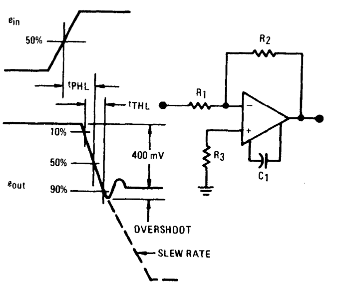
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1530 Min	MC1530 Typ	MC1530 Max	MC1430 Min	MC1430 Typ	MC1430 Max	Unit
Input Bias Current	I_{IB}	–	3.0	10	–	5.0	15	µAdc
Input Offset Current	I_{IO}	–	0.2	2.0	–	0.4	4.0	µAdc
Input Offset Voltage T_A = +25°C	V_{IO}	–	1.0	5.0	–	2.0	10	mVdc
$T_A = T_{low}$ ①		–	–	6.0	–	–	11	
$T_A = T_{high}$ ①		–	–	6.0	–	–	12	
Single-Ended Input Impedance (Open-Loop, f = 30 Hz)	z_{is}	10	20	–	5.0	15	–	k Ω
Common-Mode Input Voltage Swing	V_{ICR}	± 2.0	± 2.7	–	± 2.0	± 2.5	–	V_{pk}
Equivalent Input Noise Voltage (Open-Loop, R_s = 50 ohms, BW = 5.0 MHz)	e_N	–	10	–	–	10	–	µV(rms)
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	70	75	–	65	75	–	dB
Open-Loop Voltage Gain, T_A = +25°C	A_{vol}	–	–	–	3000	5000	–	V/V
$T_A = T_{low}$ to T_{high}		4500	5000	12,500	–	–	–	
Bandwidth (Open-Loop, -3.0 dB, no roll-off capacitance)	BW	1.0	2.0	–	1.0	2.0	–	MHz
Output Impedance (f = 100 Hz)	z_o	–	25	50	–	25	50	ohms
Output Voltage Swing (R_L = 1.0 k ohms)	V_O	± 4.5	± 5.2	–	± 4.0	± 5.0	–	V_{pk}
Power Supply Sensitivity ($R_s \leqslant$ 10 k Ω)	PSRR	–	100	–	–	100	–	µV/V
Power Supply Current	I_D^+, I_D^-	–	9.2	12.5	–	9.2	12.5	mAdc
DC Quiescent Power Dissipation (V_O = 0)	P_D	–	110	150	–	110	150	mW

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol*	MC1531 Min	MC1531 Typ	MC1531 Max	MC1431 Min	MC1431 Typ	MC1431 Max	Unit
Input Bias Current	I_{IB}	–	0.025	0.150	–	0.1	0.3	µAdc
Input Offset Current	I_{IO}	–	0.003	0.025	–	0.01	0.1	µAdc
Input Offset Voltage T_A = +25°C	V_{io}	–	3.0	10	–	5.0	15	mVdc
$T_A = T_{low}$ ①		–	–	18	–	–	–	
$T_A = T_{high}$ ①		–	–	16.5	–	–	–	
Single-Ended Input Impedance (Open-Loop, f = 30 Hz)	z_{is}	1000	2000	–	300	600	–	k Ω
Common-Mode Input Voltage Swing	V_{ICR}	± 2.0	± 2.4	–	± 2.0	± 2.2	–	V_{pk}
Equivalent Input Noise Voltage (Open-Loop, R_s = 50 ohms, BW = 5.0 MHz)	e_N	–	20	–	–	20	–	µV(rms)
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	65	65	–	60	75	–	dB
Open-Loop Voltage Gain T_A = +25°C	A_{vol}	–	–	–	1500	3500	–	V/V
$T_A = T_{low}$ to T_{high}		2500	3500	7000	–	–	–	
Bandwidth (Open-Loop, -3.0 dB, no roll-off capacitance)	BW	–	0.4	–	–	0.4	–	MHz
Output Impedance (f = 30 Hz)	z_o	–	25	50	–	25	50	ohms
Output Voltage Swing (R_L = 1.0 k ohms)	V_O	± 4.5	± 5.2	–	± 4.0	± 5.0	–	V_{pk}
Power Supply Sensitivity ($R_S \leqslant$ 10 k Ω)	PSRR	–	100	–	–	100	–	µV/V
Power Supply Current	I_D^+, I_D^-	–	9.2	12.5	–	9.2	12.5	mAdc
DC Quiescent Power Dissipation (V_O = 0)	P_D	–	110	150	–	110	150	mW

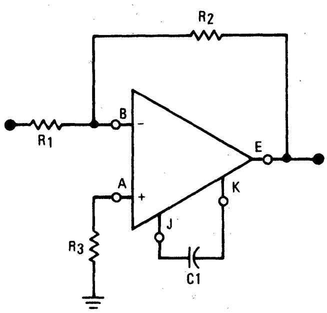


STEP RESPONSE, TYPICAL CHARACTERISTICS
(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, V_O = 400 mVdc, T_A = +25°C)

	Symbol	MC1530 MC1430	MC1531 MC1431	
Step Response				
Gain = 100, 0% overshoot,	t_{THL}	0.13	0.36	µs
R_1 = 1.0 k ohm, R_2 = 100 k ohms,	t_{PHL}	0.11	0.21	µs
R_3 = 1.0 k ohm, C_1 = 750 pF	SR	33	16	V/µs
Gain = 10, 10% overshoot,	t_{THL}	0.34	0.30	µs
R_1 = 10 k ohms, R_2 = 100 k ohms,	t_{PHL}	0.25	0.28	µs
R_3 = 10 k ohms, C_1 = 6800 pF	SR	6.0	5.5,	V/µs
Gain = 1.0, 5.0% overshoot,	t_{THL}	0.28	0.37	µs
R_1 = 10 k ohms, R_2 = 10 k ohms,	t_{PHL}	0.16	0.17	µs
R_3 = 5.0 k ohms, C_1 = 33,000 pF	SR	1.7	1.4	V/µs

① T_{low}: 0°C for MC1430, -55°C for MC1530; T_{high}: +75°C for MC1430, +125°C for MC1530
T_{low}: 0°C for MC1431, -55°C for MC1531; T_{high}: +75°C for MC1431, +125°C MC1531

FIGURE 4 – TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS
(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C)

FIG. NO.	CURVE NO.	VOLTAGE GAIN	DEVICE NO.	TEST CONDITIONS			
				R_1 (kΩ)	R_2 (kΩ)	R_3 (Ω)	C_1 (pF)
5	1,2	100	MC1530/MC1430, MC1531/MC1431	1.0	100	1.0 k	750
	3	10	MC1530/MC1430, MC1531/MC1431	10	100	10 k	6800
	4	1	MC1530/MC1430, MC1531/MC1431	10	10	5.0 k	33,000
6	1	100	MC1530/MC1430	1.0	100	1.0 k	750
	2	10	MC1530/MC1430	10	100	10 k	6800
	3	10	MC1530/MC1430	1.0	10	1.0 k	6800
	4	1	MC1530/MC1430	10	10	5.0 k	33,000
	5	1	MC1530/MC1430	1.0	1.0	500	33,000
7	1	100	MC1531/MC1431	1.0	100	1.0 k	750
	2	10	MC1531/MC1431	10	100	10 k	6800
	3	1	MC1531/MC1431	10	10	5.0 k	33,000
8	1	A_{VOL}	MC1530/MC1430	0	∞	0	0
	2	A_{VOL}	MC1530/MC1430	0	∞	0	750
	3	A_{VOL}	MC1530/MC1430	0	∞	0	6800
	4	A_{VOL}	MC1530/MC1430	0	∞	0	33,000
9	1	A_{VOL}	MC1531/MC1431	0	∞	0	0
	2	A_{VOL}	MC1531/MC1431	0	∞	0	750
	3	A_{VOL}	MC1531/MC1431	0	∞	0	6800
	4	A_{VOL}	MC1531/MC1431	0	∞	0	33,000

FIGURE 5 – LARGE SIGNAL SWING versus FREQUENCY

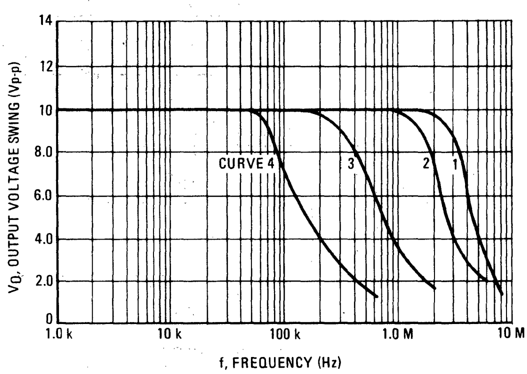


FIGURE 6 – MC1530/MC1430 VOLTAGE GAIN versus FREQUENCY

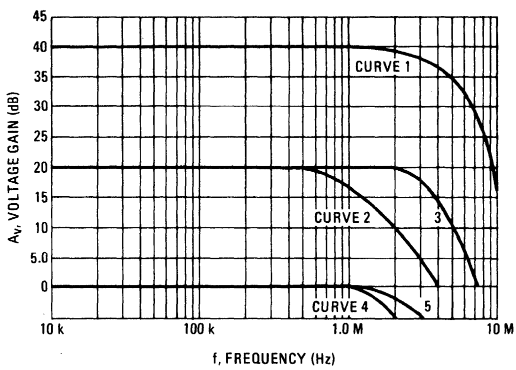


FIGURE 7 – MC1531/MC1431 VOLTAGE GAIN versus FREQUENCY

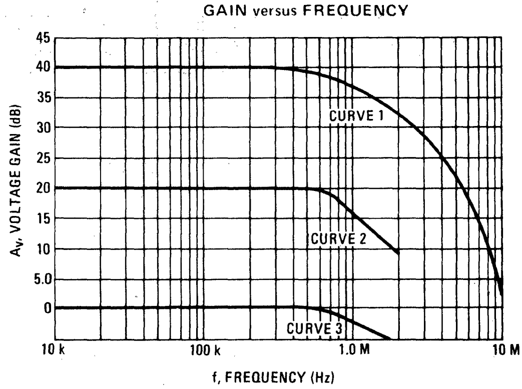


FIGURE 8 – MC1530/MC1430 OPEN LOOP VOLTAGE GAIN versus FREQUENCY

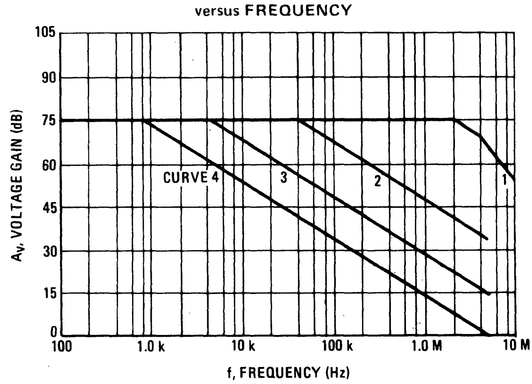


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FIGURE 9 – MC1531/MC1431 OPEN LOOP VOLTAGE GAIN versus FREQUENCY

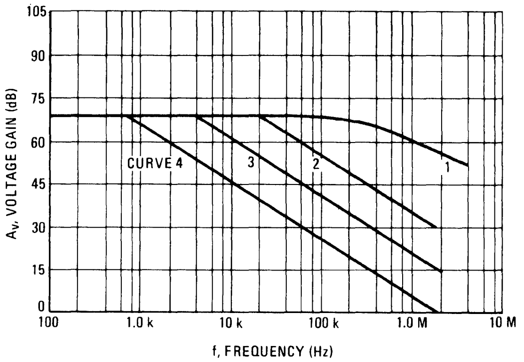


FIGURE 10 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

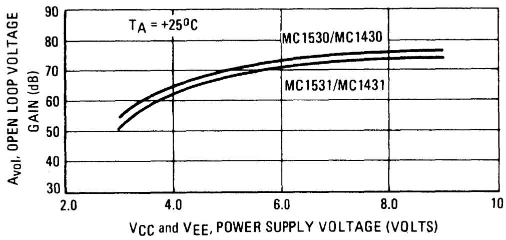


FIGURE 11 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

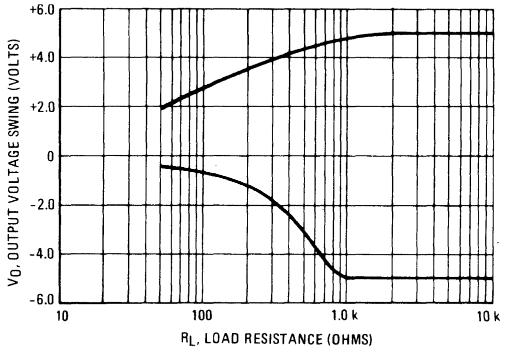


FIGURE 12 – COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

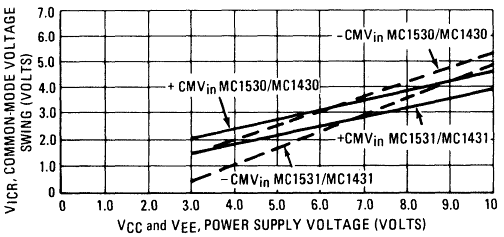
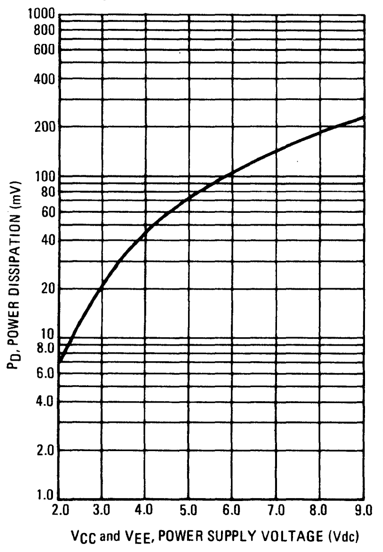


FIGURE 13 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

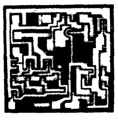


8

OPERATIONAL AMPLIFIERS

MC1533
MC1433

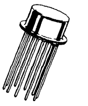
MONOLITHIC OPERATIONAL AMPLIFIER



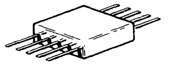
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 60,000 typical
- Low Temperature Drift – ±5 μV/^{o}C
- Large Output Voltage Swing –
  ±13 V typical @ ±15 V Supply
- Low Output Impedance – Z_{out} = 100 ohms typical

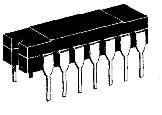
OPERATIONAL AMPLIFIER MONOLITHIC SILICON INTEGRATED CIRCUIT



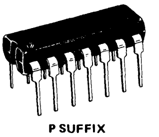
G SUFFIX
METAL PACKAGE
CASE 602B



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 646

(MC1433P Only)

FIGURE 1 – CIRCUIT SCHEMATIC

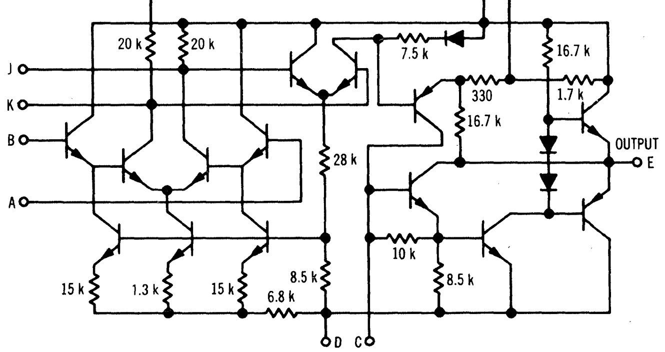
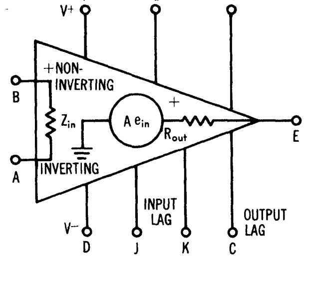


FIGURE 2 – EQUIVALENT CIRCUIT



PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"G" Package	1	2	3	4	5	6	7	8	9	10
"F" Package	10	1	2	3	4	5	6	7	8	9
"L" & "P" Packages	4	5	6	7	11	12	13	14	2	3

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1533 Min	MC1533 Typ	MC1533 Max	MC1433 Min	MC1433 Typ	MC1433 Max	Unit
Open Loop Voltage Gain	A_{VOL}							–
(T_A = +25°C)		40,000	60,000	–	30,000	60,000	–	
(T_A = T_{low} ① to T_{high} ①)		35,000	50,000	–	20,000	50,000	–	
Output Impedance (f = 20 Hz)	Z_{out}	–	100	150	–	100	150	Ω
Input Impedance (f = 20 Hz)	Z_{in}	500	1000	–	300	600	–	kΩ
Output Voltage Swing	V_o							V_{peak}
(R_L = 10 kΩ)		±12	±13	–	±12	±13	–	
(R_L = 2 kΩ)		±11	±12	–	±10	±12	–	
Input Common Mode Voltage Swing	CMV_{in}	+9.0	+10	–	+8.0	+9.0	–	V_{peak}
		-8.0	-9.0	–	-8.0	-9.0	–	
Common Mode Rejection Ratio	CM_{rej}	90	100	–	80	100	–	dB
Input Bias Current	I_b							μA
(T_A = +25°C)		–	0.5	1.0	–	0.5	2.0	
(T_A = T_{low})		–	–	3.0	–	–	4.0	
Input Offset Current	$\|I_{io}\|$							μA
(T_A = +25°C)		–	0.03	0.15	–	0.1	0.50	
(T_A = T_{low})		–	–	0.5	–	–	0.75	
(T_A = T_{high})		–	–	0.2	–	–	0.75	
Input Offset Voltage ②	$\|V_{io}\|$							mV
(T_A = +25°C)		–	1.0	5.0	–	1.0	7.5	
(T_A = T_{low}, T_{high})		–	–	6.0	–	–	10	
Step Response (C_2 = 10 pF)								
Gain = 100, 10% overshoot, R_1 = 10 kΩ, R_2 = 1.0 MΩ, R_3 = 100 Ω, C_1 = 0.01 μF	t_f	–	0.25	–	–	0.25	–	μs
	t_{pd}	–	0.1	–	–	0.1	–	μs
	dV_{out}/dt ③	–	6.2	–	–	6.2	–	V/μs
Gain = 10, no overshoot, R_1 = 10 kΩ, R_2 = 100 kΩ, R_3 = 10 Ω, C_1 = 0.1 μF	t_f	–	0.3	–	–	0.3	–	μs
	t_{pd}	–	0.1	–	–	0.1	–	μs
	dV_{out}/dt ③	–	2.9	–	–	2.9	–	V/μs
Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 10 Ω, C_1 = 1.0 μF	t_f	–	0.2	–	–	0.2	–	μs
	t_{pd}	–	0.1	–	–	0.1	–	μs
	dV_{out}/dt ③	–	2.0	–	–	2.0	–	V/μs
Average Temperature Coefficient of Input Offset Voltage	$\|TC_{Vio}\|$							μV/°C
(T_A = T_{low} to +25°C)		–	8.0	–	–	10	–	
(T_A = +25°C to T_{high})		–	5.0	–	–	8.0	–	
Average Temperature Coefficient of Input Offset Current	$\|TC_{Iio}\|$							nA/°C
(T_A = T_{low} to T_{high})		–	0.1	–	–	0.1	–	
(T_A = +25°C to T_{high})		–	0.05	–	–	0.05	–	
DC Power Dissipation (Power Supply = ±15 V, V_o = 0)	P_D	–	125	170	–	125	240	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	50	150	–	50	200	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	50	150	–	50	200	μV/V

① T_{high} = +75°C for MC1433, +125°C for MC1533; T_{low} = 0 for MC1433, -55°C for MC1533

② Input offset voltage (V_{io}) may be adjusted to zero.

③ dV_{out}/dt = Slew Rate

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Power Supply Voltage	MC1533,MC1433	V^+	+20,+18	Vdc
	MC1533,MC1433	V^-	-20,-18	Vdc
Differential Input Signal		V_{in}	±10	Volts
Common Mode Input Swing		CMV_{in}	$\pm V^+$	Volts
Load Current		I_L	10	mA
Output Short Circuit Duration		t_S	1.0	s
Power Dissipation (Package Limitation)		P_D		
Metal Package			680	mW
Derate above T_A = +25°C			4.6	mW/°C
Flat Package			500	mW
Derate above T_A = +25°C			3.3	mW/°C
Dual In-Line Ceramic Package			625	mW
Derate above T_A = +25°C			5.0	mW/°C
Dual In-Line Plastic Package			400	mW
Derate above T_A = +25°C			3.3	mW/°C
Operating Temperature Range		T_A		°C
	MC1533		-55 to +125	
	MC1433		0 to +75	
Storage Temperature Range		T_{stg}		°C
Metal and Ceramic Packages			-65 to +150	
Plastic Package			-65 to +125	

TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT

V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C

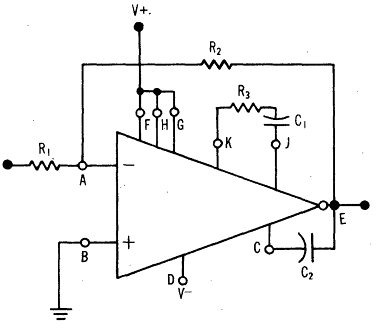


Fig. No.	Curve No.	Test Conditions				
		R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (μF)	C_2 (pF)
4	1	10 k	10 k	10	1.0	10
	2	10 k	100 k	10	0.1	10
	3	10 k	1.0 M	100	0.01	10
	3	1.0 k	1.0 M	390	0.002	10
5	1	10 k	10 k	10	1.0	10
	2	10 k	100 k	10	0.1	10
	3	10 k	1.0 M	100	0.01	10
	4	1.0 k	1.0 M	390	0.002	10
6	1	0	∞	10	1.0	10
	2	0	∞	10	0.1	10
	3	0	∞	100	0.01	10
	4	0	∞	390	0.002	10

8

TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = + 25°C unless otherwise noted)

FIGURE 4 – LARGE-SIGNAL SWING versus FREQUENCY

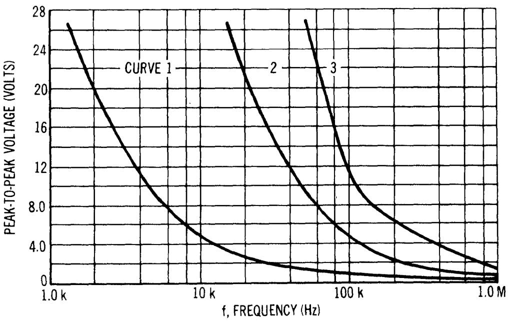


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

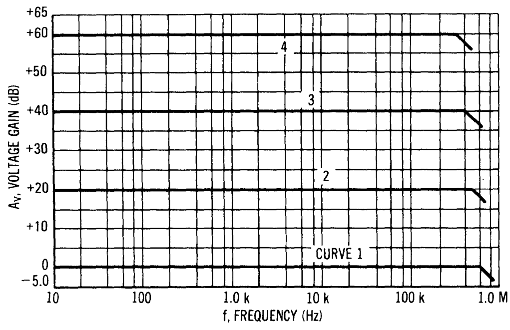


FIGURE 6 – OFFSET ADJUST CIRCUIT

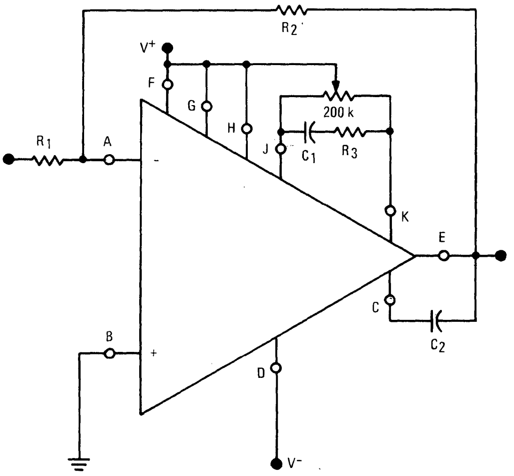
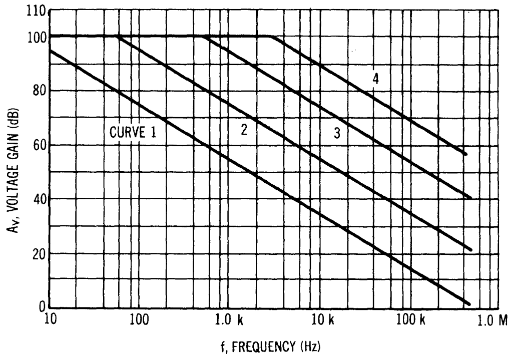


FIGURE 7 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY
(HIGH GAIN CONFIGURATION)



PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"G" Package	1	2	3	4	5	6	7	8	9	10
"F" Package	10	1	2	3	4	5	6	7	8	9
"L" & "P" Packages	4	5	6	7	11	12	13	14	2	3

TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

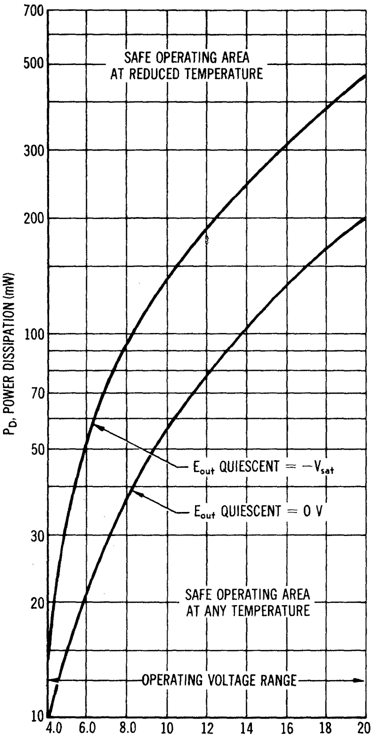


FIGURE 9 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

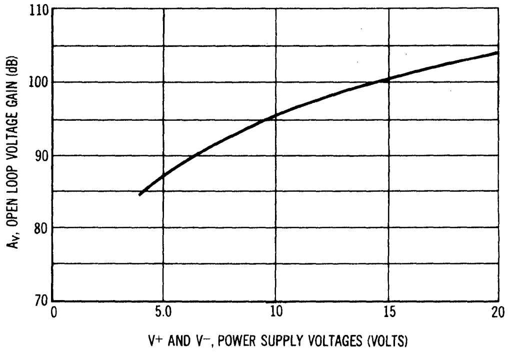


FIGURE 10 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

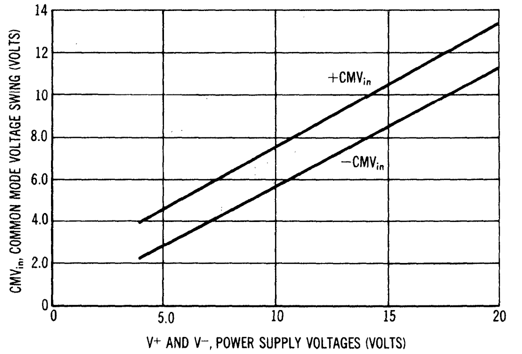
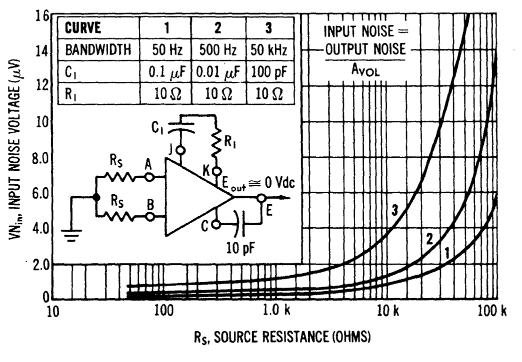


FIGURE 11 – INPUT NOISE VOLTAGE versus SOURCE RESISTANCE

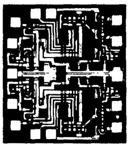


8

MC1535
MC1435

OPERATIONAL AMPLIFIERS

MONOLITHIC DUAL OPERATIONAL AMPLIFIERS



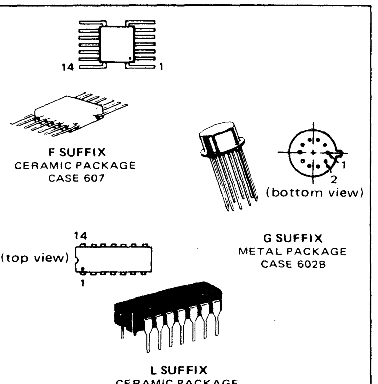
. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

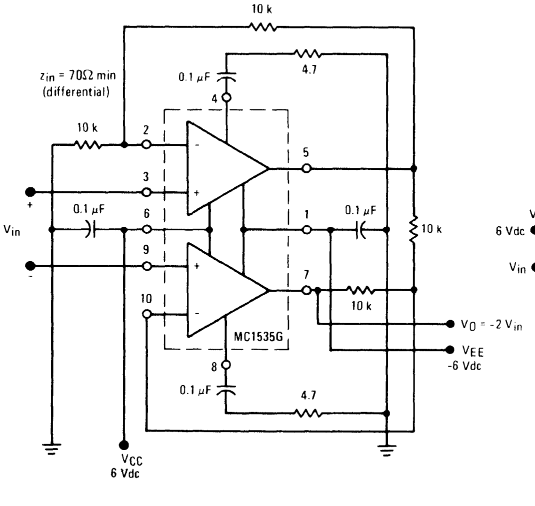
- High Open Loop Gain Characteristics – A_{VOL} = 7,000
- Low Temperature Drift – ±10 μV/°C
- Low Input Offset Voltage – 1.0mV
- Low Input Noise Voltage – 0.5μV

MONOLITHIC DUAL OPERATIONAL AMPLIFIERS

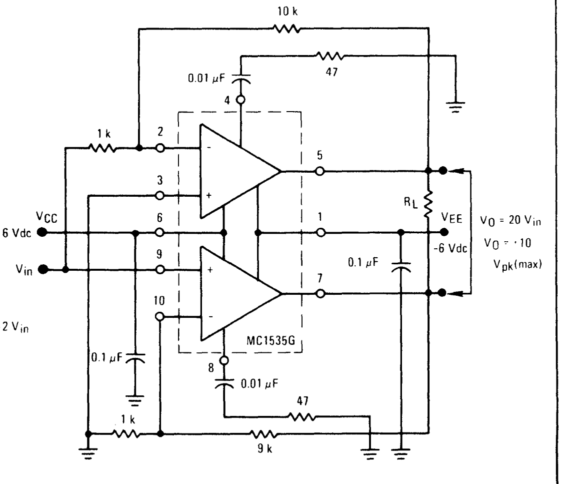
INTEGRATED CIRCUIT EPITAXIAL PASSIVATED



HIGH z_{in}, DIFFERENTIAL TO SINGLE-ENDED AMPLIFIER



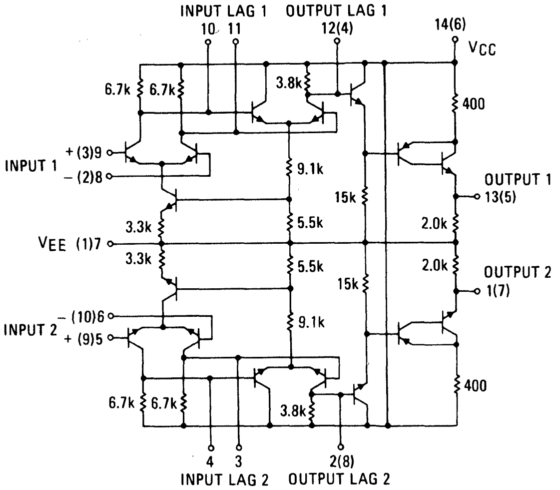
LARGE OUTPUT SWING CONFIGURATION (FLOATING LOAD)



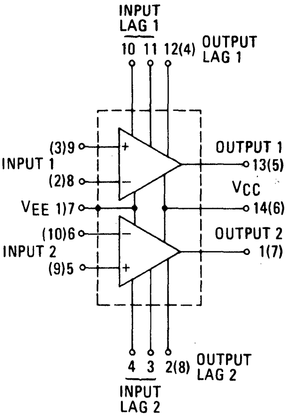
See Packaging Information Section for outline dimensions.

8

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



Number at end of terminal is pin number for ceramic packages.
Number in parenthesis is pin number for metal package. Input Lag available only in ceramic packages.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC1535	MC1435	Unit
Power Supply Voltage	V_{CC} V_{EE}	+10 -10	+9.0 -9.0	Vdc
Differential Input Signal Voltage	V_{in}	±5.0	±5.0	Volts
Common-Mode Input Swing Voltage	V_{ICR}	+5.0, -4.0	+5.0 -4.0	Volts
Load Current	I_L	20	20	mA
Output Short-Circuit Duration	T_{SC}	Continuous		
Power Dissipation (Package Limitation) Flat Ceramic Package Derate above T_A = +25°C Metal Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D	 500 3.3 680 4.6 625 5.0		 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

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ELECTRICAL CHARACTERISTICS (Each Amplifier) (V_{CC} = +6.0 Vdc, V_{EE} = - 6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristics	Symbol	MC1535 Min	MC1535 Typ	MC1535 Max	MC1435 Min	MC1435 Typ	MC1435 Max	Unit
Input Bias Current	I_{IB}							
$I_{IB} = \frac{I_1 + I_2}{2}$, T_A = +25°C		–	1.2	3.0	–	1.2	5.0	µAdc
T_A = T_{low} to T_{high} ①		–	–	6.0	–	–	10	
Input Offset Current	$\|I_{IO}\|$							nAdc
T_A = +25°C		–	50	300	–	50	500	
T_A = +25°C to T_{high}		–	–	300	–	–	1500	
T_A = T_{low} to +25°C		–	–	900	–	–	1500	
Input Offset Voltage	$\|V_{IO}\|$							mVdc
T_A = +25°C		–	1.0	3.0	–	1.0	5.0	
T_A = T_{low} to T_{high}		–	–	5.0	–	–	7.5	
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	10	45	–	10	45	–	k ohms
Parallel Input Capacitance	C_p	–	6.0	–	–	–	–	pF
Common-Mode Input Impedance (f = 20 Hz)	$z_{(in)}$	–	250	–	–	250	–	Megohms
Common-Mode Input Voltage Swing See Figure 7.	V_{ICR}	+3.0	+3.9	–	+3.0	+3.9	–	V_{pk}
		-2.0	-2.7	–	-2.0	-2.7	–	
Equivalent Input Noise Voltage (A_v = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	e_n	–	45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	-70	-90	–	-70	-90	–	dB
Open Loop Voltage Gain (T_A = T_{low} to T_{high})	A_{vol}	4,000	7,000	10,000	3,500	7,000	–	V/V
Power Bandwidth (See Figure 2, Curve 3A.) (A_V = 1, R_L = 2.0 kohms, THD ≤ 5%, V_o = 20 Vp-p)	P_{BW}	–	40	–	–	40	–	kHz
Unity Gain Crossover Frequency (open-loop)		–	2.0	–	–	2.0	–	MHz
Phase Margin (open-loop, unity gain)		–	75	–	–	75	–	degrees
Gain Margin		–	18	–	–	18	–	dB
Step Response								
Gain = 100, 30% overshoot,	t_{PHL}	–	0.3	–	–	0.3	–	µs
R1 = 4.7 kΩ, R2 = 470 kΩ,	t_p	–	0.1	–	–	0.1	–	µs
R3 = 150 Ω, C1 = 1,000 pF	dV_O/dt ②	–	0.167	–	–	0.167	–	V/µs
Gain = 10, 10% overshoot,	t_{PHL}	–	1.9	–	–	1.9	–	µs
R1 = 47 kΩ, R2 = 470 kΩ,	t_p	–	0.3	–	–	0.3	–	µs
R3 = 47 Ω, C1 = 0.01 µF	dV_O/dt ②	–	0.111	–	–	0.111	–	V/µs
Gain = 1, 5% overshoot,	t_{PHL}	–	27	–	–	27	–	µs
R1 = 47 kΩ, R2 = 47 kΩ,	t_p	–	0.25	–	–	0.25	–	µs
R3 = 4.7 Ω, C1 = 0.1 µF	dV_O/dt ②	–	0.013	–	–	0.013	–	V/µs
Output Impedance (f = 20 Hz)	z_o	–	1.7	–	–	1.7	–	k ohms
Short-Circuit Output Current	I_{SC}	–	±17	–	–	±17	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±2.5	±2.8	–	±2.3	±2.7	–	V_{pk}
Power Supply Sensitivity								µV/V
V_{EE} = constant, R_s ⩽ 10 k ohms	S+	–	50	–	–	50	–	
V_{CC} = constant, R_s ⩽ 10 k ohms	S-	–	100	–	–	100	–	
Power Supply Current (Total)	I_D^+	–	8.3	12.5	–	8.3	15	mAdc
	I_D^-	–	8.3	12.5	–	8.3	15	
DC Quiescent Power Dissipation (Total) (V_O = 0)	P_D	–	100	150	–	100	180	mW

MATCHING CHARACTERISTICS

Characteristics	Symbol	MC1535 Min	MC1535 Typ	MC1535 Max	MC1435 Min	MC1435 Typ	MC1435 Max	Unit
Open Loop Voltage Gain	$A_{vol1}-A_{vol2}$	–	±1.0	–	–	±1.0	–	dB
Input Bias Current	$I_{IB1}-I_{IB2}$	–	±0.15	–	–	±0.15	–	µA
Input Offset Current	$I_{IO1}-I_{IO2}$	–	±0.02	–	–	±0.02	–	µA
Average Temperature Coefficient $I_{IB1}-I_{IB2}$	$TCI_{IO1}-TCI_{IO2}$	–	±0.1	–	–	±0.1	–	nA/°C
Input Offset Voltage	$V_{IO1}-V_{IO2}$	–	±0.1	–	–	±0.1	–	mV
Average Temperature Coefficient	$TCV_{IO1}-TCV_{IO2}$	–	±0.5	–	–	±0.5	–	µV/°C
Channel Separation (See Fig. 10) (f = 10 kHz)	$\frac{e_{o1}}{e_{o2}}$	–	-60	–	–	-60	–	dB

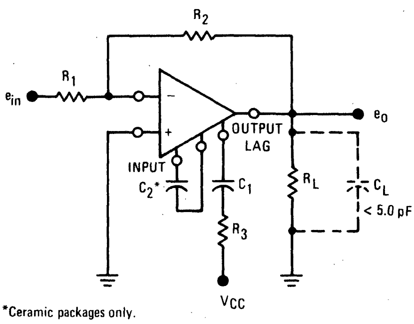
① T_{low}: 0°C for MC1435
-55°C for MC1535
T_{high}: +75°C for MC1435
+125°C for MC1535

② dV_O/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = −6.0 Vdc, T_A = +25°C.)

FIGURE 1 – TEST CIRCUIT



*Ceramic packages only.

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS $R_1(\Omega)$	$R_2(\Omega)$	C_1(pF)	$R_3(\Omega)$	C_2(pF)	OUTPUT NOISE mV(RMS)
2	3	1	47 k	47 k	100,000	4.7	0	0.12
	3A	or 1	47 k	47 k	0	∞	50,000	0.46
3	1	100	4.7 k	470 k	1,000	150	0	1.7
		or 100	4.7 k	470 k	0	∞	510	2.1
	2	10	47 k	470 k	10,000	47	0	1.0
		or 10	47 k	470 k	0	∞	5,000	2.1
	3	1	47 k	47 k	100,000	4.7	0	0.12
		or 1	47 k	47 k	0	∞	50,000	0.46
4	1	or A_{vol}	100	∞	1,000	150	0	8.1
		A_{vol}	100	∞	0	∞	510	8.1
	2	or A_{vol}	100	∞	10,000	47	0	5.5
		A_{vol}	100	∞	0	∞	5,000	5.5
	3	or A_{vol}	100	∞	100,000	4.7	0	4.4
		A_{vol}	100	∞	0	∞	50,000	4.4

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

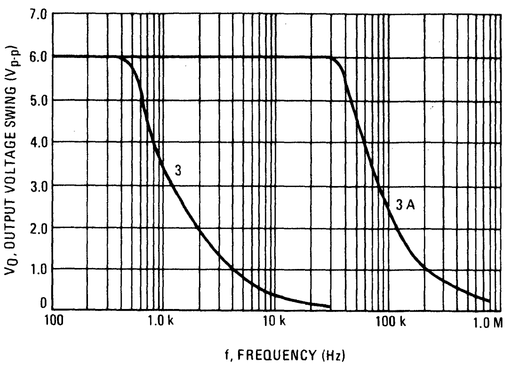


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

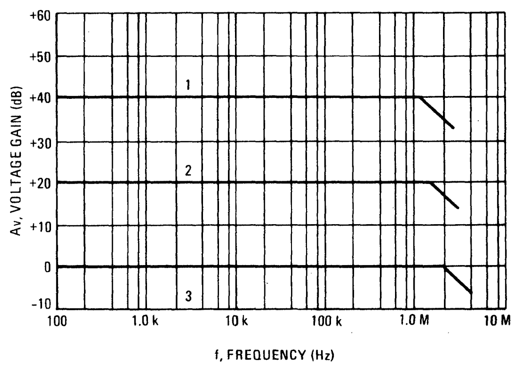


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

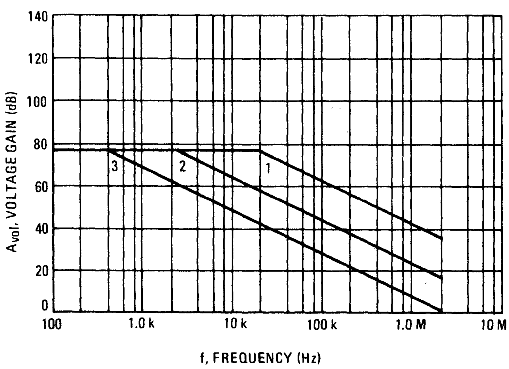
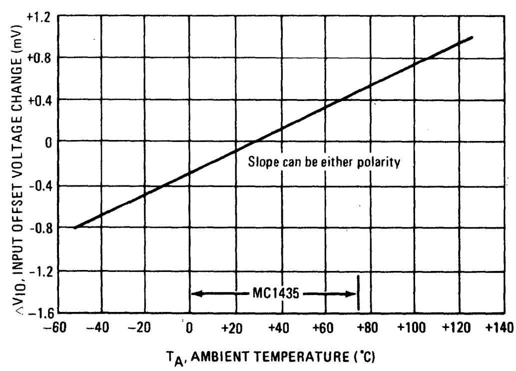


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE



8

MC1535, MC1435 (continued)

TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

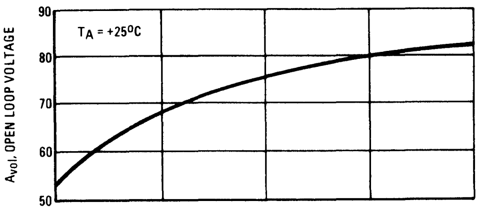


FIGURE 7 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

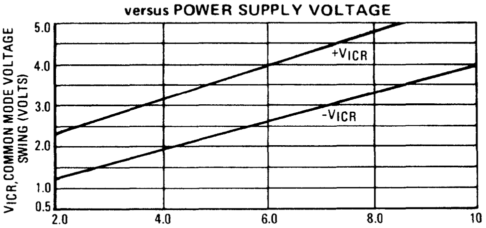


FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

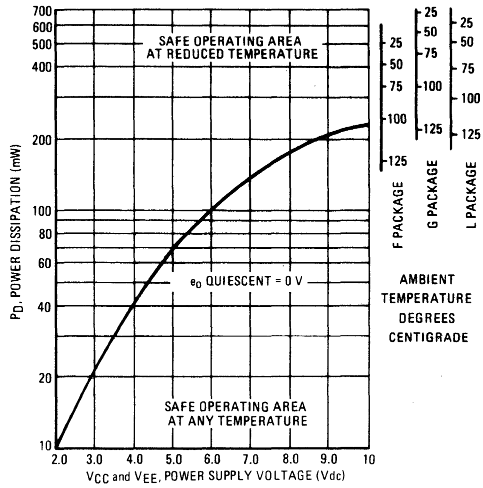
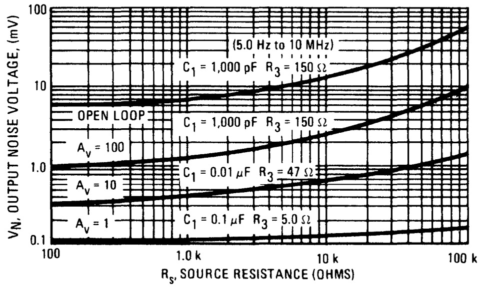


FIGURE 9 – OUTPUT WIDEBAND NOISE VOLTAGE versus SOURCE RESISTANCE



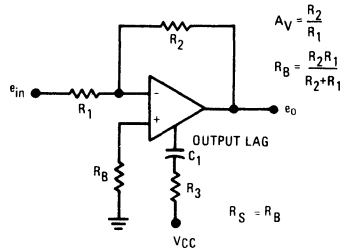
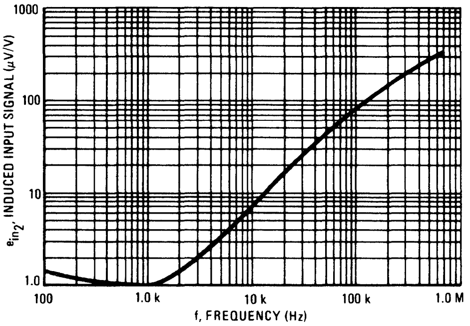
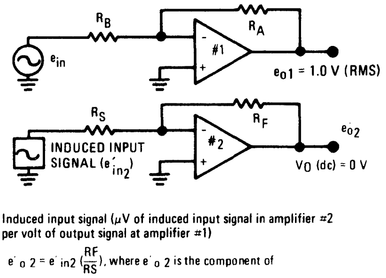


FIGURE 10 – INDUCED INPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced input signal (μV of induced input signal in amplifier #2 per volt of output signal at amplifier #1)

$e'_{o2} = e'_{in2}\left(\frac{RF}{RS}\right)$, where e'_{o2} is the component of e_{o2} due only to lack of perfect separation between the two amplifiers.

8

MC1536G
MC1436G
MC1436CG

OPERATIONAL AMPLIFIER

HIGH VOLTAGE, INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER

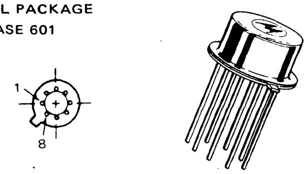
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage – ±40 Vdc (MC1536G)
- Output Voltage Swing –
  ±30 $V_{pk(min)}$ (V^+ = +36 V, V^- = -36 V) (MC1536G)
  ±22 $V_{pk(min)}$ (V^+ = +28 V, V^- = -28 V)
- Input Bias Current – 20 nA max (MC1536G)
- Input Offset Current – 3.0 nA max (MC1536G)
- Fast Slew Rate – 2.0 V/μs typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- A_{VOL} – 500,000 typ
- Characteristics Independent of Power Supply Voltages – (±5.0 Vdc to ±36 Vdc)

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED

METAL PACKAGE
CASE 601



(bottom view)

FIGURE 1 – DIFFERENTIAL AMPLIFIER WITH ±20 V COMMON-MODE INPUT VOLTAGE RANGE

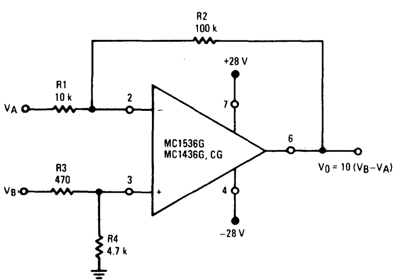


FIGURE 2 – VOLTAGE CONTROLLED CURRENT SOURCE or TRANSCONDUCTANCE AMPLIFIER WITH 0 TO 40 V COMPLIANCE

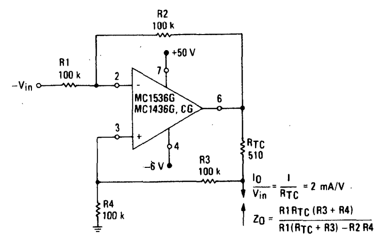


FIGURE 3 – TYPICAL NON-INVERTING X10 VOLTAGE AMPLIFIER

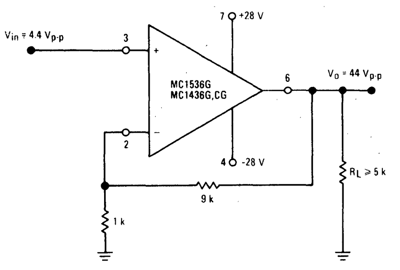
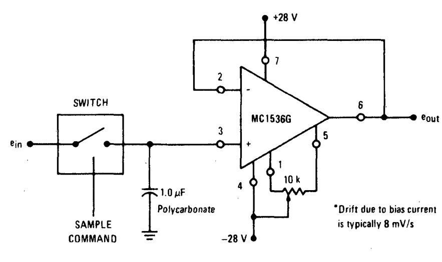


FIGURE 4 – LOW-DRIFT SAMPLE AND HOLD



See Packaging Information Section for outline dimensions.
See current MCC1536/1436 data sheet for standard linear chip information.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1536G	MC1436G	MC1436CG	Unit
Power Supply Voltage	V^+ V^-	+40 -40	+34 -34	+30 -30	Vdc
Differential Input Signal	V_{in}	$\pm(V^+ + \lvert V^-\rvert - 3)$			Volts
Common-Mode Input Swing	CMV_{in}	$+V^+, -(\lvert V^-\rvert - 3)$			Volts
Output Short Circuit Duration ($V^+ = \lvert V^-\rvert$ = 28 Vdc, V_O = 0)	T_{SC}	5.0			s
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6			mW mW/°C
Operating Temperature Range	T_A	-55 to +150	0 to +75		°C
Storage Temperature Range	T_{stg}	-65 to +150			°C

ELECTRICAL CHARACTERISTICS (V^+ = +28 Vdc, V^- = -28 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1536G			MC1436G			MC1436CG			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_b										nAdc
T_A = +25°C		–	8.0	20	–	15	40	–	25	90	
$T_A = T_{low}$ to T_{high} (See Note 1)		–	–	35	–	–	55	–	–	–	
Input Offset Current	$\lvert I_{io}\rvert$										nAdc
T_A = +25°C		–	1.0	3.0	–	5.0	10	–	10	25	
T_A = +25°C to T_{high}		–	–	4.5	–	–	14	–	–	–	
$T_A = T_{low}$ to +25°C		–	–	7.0	–	–	14	–	–	–	
Input Offset Voltage	$\lvert V_{io}\rvert$										mVdc
T_A = +25°C		–	2.0	5.0	–	5.0	10	–	5.0	12	
$T_A = T_{low}$ to T_{high}		–	–	7.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f ≤ 5.0 Hz)											
Parallel Input Resistance	R_p	–	10	–	–	10	–	–	10	–	Meg ohms
Parallel Input Capacitance	C_p	–	2.0	–	–	2.0	–	–	2.0	–	pF
Common-Mode Input Impedance (f ≤ 5.0 Hz)	$Z_{(in)}$	–	250	–	–	250	–	–	250	–	Meg ohms
Common-Mode Input Voltage Swing	CMV_{in}	±24	±25	–	±22	±25	–	±18	±20	–	V_{pk}
Equivalent Input Noise Voltage	e_n										nV/(Hz)½
(A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)		–	50	–	–	50	–	–	50	–	
Common-Mode Rejection Ratio (dc)	CM_{rej}	80	110	–	70	110	–	50	90	–	dB
Large Signal dc Open Loop Voltage Gain	A_{VOL}										V/V
(V_O = ± 10 V, R_L = 100 k ohms) T_A = +25°C		100,000	500,000	–	70,000	500,000	–	50,000	500,000	–	
(V_O = ± 10 V, R_L = 100 k ohms) $T_A = T_{low}$ to T_{high}		50,000	–	–	50,000	–	–	–	–	–	
(V_O = ±10 V, R_L = 10 k ohms, T_A = +25°C)		–	200,000	–	–	200,000	–	–	200,000	–	
Power Bandwidth (Voltage Follower)	P_{BW}										kHz
(A_V = 1, R_L = 5.0 k ohms, THD ≤ 5%, V_O = 40 Vp-p)		–	23	–	–	23	–	–	23	–	
Unity Gain Crossover Frequency (open-loop)	f_c	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)	ϕ	–	50	–	–	50	–	–	50	–	degrees
Gain Margin	A_{GM}	–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)	dV_{out}/dt	–	2.0	–	–	2.0	–	–	2.0	–	V/μs
Output Impedance (f ≤ 5.0 Hz)	Z_{out}	–	1.0	–	–	1.0	–	–	1.0	–	k ohms
Short-Circuit Output Current	I_{SC}	–	±17	–	–	±17	–	–	±19	–	mAdc
Output Voltage Swing (R_L = 5.0 k ohms)	V_O										V_{pk}
V^+ = +28 Vdc, V^- = -28 Vdc		±22	±23	–	±20	±22	–	±20	±22	–	
V^+ = +36 Vdc, V^- = -36 Vdc		±30	±32	–	–	–	–	–	–	–	
Power Supply Sensitivity (dc)											μV/V
V^- = constant, R_s ≤ 10 k ohms	S+	–	15	100	–	35	200	–	50	–	
V^+ = constant, R_s ≤ 10 k ohms	S-	–	15	100	–	35	200	–	50	–	
Power Supply Current (See Note 2)	I_D+	–	2.2	4.0	–	2.6	5.0	–	2.6	5.0	mAdc
	I_D-	–	2.2	4.0	–	2.6	5.0	–	2.6	5.0	
DC Quiescent Power Dissipation	P_D										mW
(V_{oi} = 0)		–	124	224	–	146	280	–	146	280	

Note 1: T_{low}: 0°C for MC1436G,CG
-55°C for MC1536G
T_{high}: +75°C for MC1436G,CG
+150°C for MC1536G

Note 2: $V^+ = \lvert V^-\rvert$ = 5.0 Vdc to 36 Vdc for MC1536G
$V^+ = \lvert V^-\rvert$ = 5.0 Vdc to 30 Vdc for MC1436G
$V^+ = \lvert V^-\rvert$ = 5.0 Vdc to 28 Vdc for MC1436CG

8

FIGURE 5 – POWER BANDWIDTH

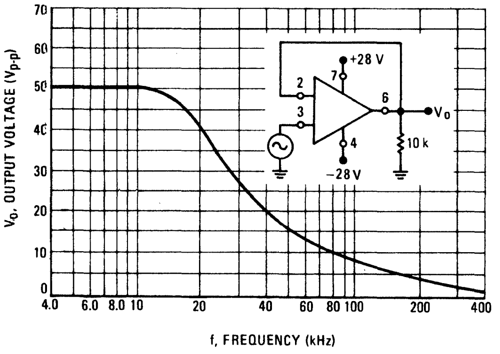


FIGURE 6 – PEAK OUTPUT VOLTAGE SWING versus POWER SUPPLY VOLTAGE

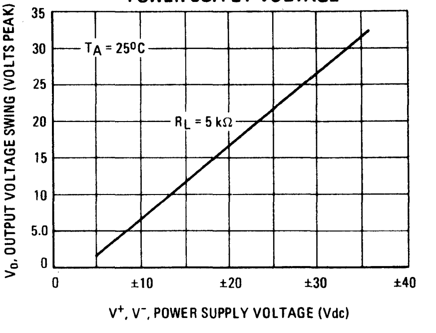


FIGURE 7 – OPEN-LOOP FREQUENCY RESPONSE

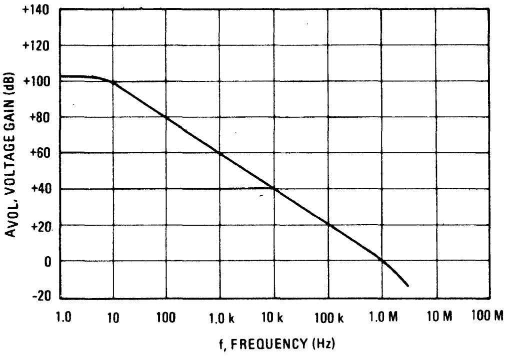


FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

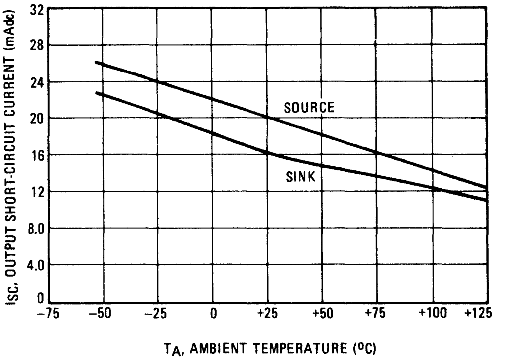


FIGURE 9 – INPUT BIAS CURRENT versus TEMPERATURE

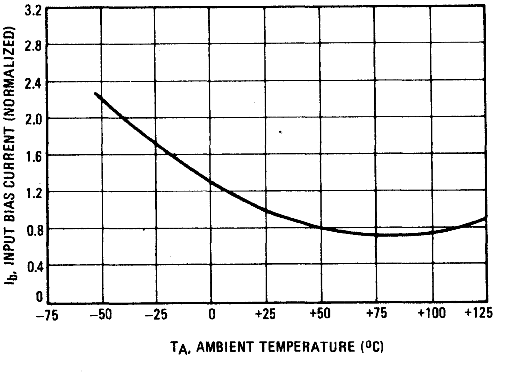


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FIGURE 10 – INVERTING FEEDBACK MODEL

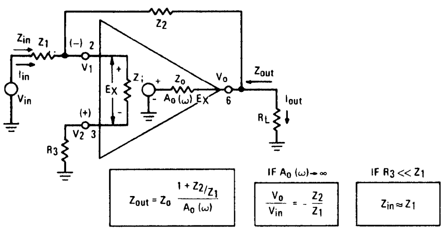


FIGURE 11 – NON-INVERTING FEEDBACK MODEL

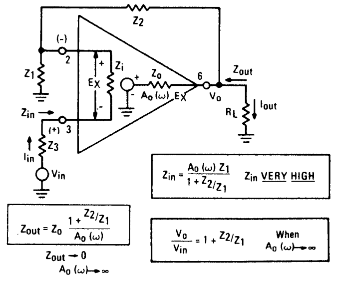


FIGURE 12 – AUDIO AMPLIFIER

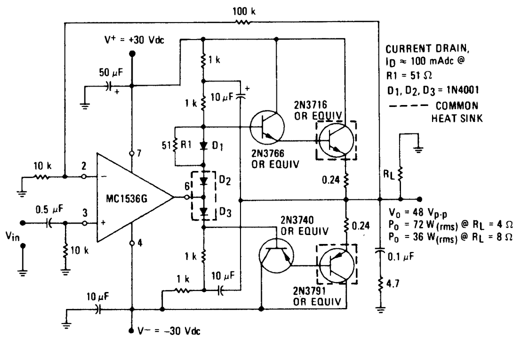


FIGURE 13 – CIRCUIT SCHEMATIC

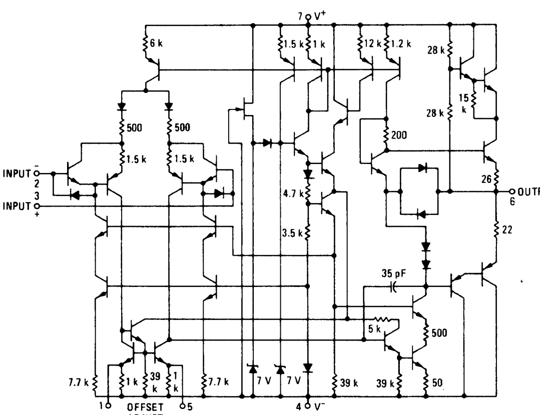
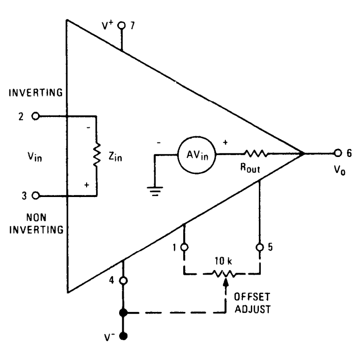


FIGURE 14 – EQUIVALENT CIRCUIT



8

MC1537
MC1437

OPERATIONAL AMPLIFIERS

HIGHLY MATCHED MONOLITHIC DUAL OPERATIONAL AMPLIFIERS

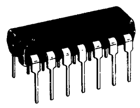
. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics — A_{VOL} = 45,000 typical
- Low Temperature Drift — $\pm 3\ \mu V/^{o}C$
- Large Output Voltage Swing — ± 14 V typical @ ± 15 V Supply

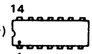
DUAL MC1709 MONOLITHIC SILICON OPERATIONAL AMPLIFIERS INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 646

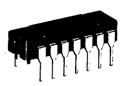


(MC1437 only)

(top view)



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C Plastic Package Derate above T_A = +25°C	P_D	 750 6.0 625 5.0	 mW mW/°C mW mW/°C
Operating Temperature Range MC1537 MC1437	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 — CIRCUIT SCHEMATIC

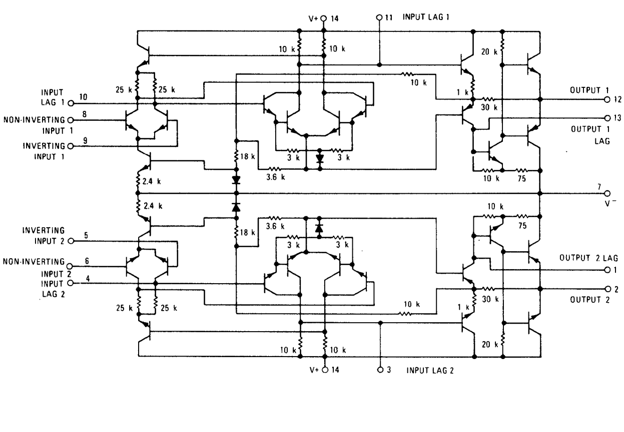
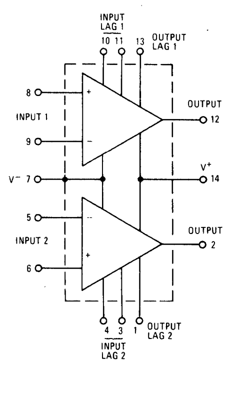


FIGURE 2 — EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

8

MC1537, MC1437 (continued)

ELECTRICAL CHARACTERISTICS — Each Amplifier (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MC1537 Min	MC1537 Typ	MC1537 Max	MC1437 Min	MC1437 Typ	MC1437 Max	Unit
Open Loop Voltage Gain (R_L = 5.0 kΩ, V_O = ±10 V, T_A = T_{low} ① to T_{high} ②)	A_{VOL}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	Z_o	–	30	–	–	30	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	150	400	–	50	150	–	kΩ
Output Voltage Swing (R_L = 10 kΩ)	V_O	±12	±14	–	±12	±14	–	V_{peak}
(R_L = 2.0 kΩ)		±10	±13	–	–	–	–	
Input Common-Mode Voltage Swing	CMV_{in}	±8.0	±10	–	±8.0	±10	–	V_{peak}
Common-Mode Rejection Ratio	CM_{rej}	70	100	–	65	100	–	dB
Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$ (T_A = +25°C)	I_b	–	0.2	0.5	–	0.4	1.5	µA
(T_A = T_{low} ①)		–	0.5	1.5	–	–	2.0	
Input Offset Current ($I_{io} = I_1 - I_2$)	$\|I_{io}\|$	–	0.05	0.2	–	0.05	0.5	µA
($I_{io} = I_1 - I_2$, T_A = T_{low} ①)		–	–	0.5	–	–	0.75	
($I_{io} = I_1 - I_2$, T_A = T_{high} ②)		–	–	0.2	–	–	0.75	
Input Offset Voltage (T_A = +25°C)	$\|V_{io}\|$	–	1.0	5.0	–	1.0	7.5	mV
(T_A = T_{low} ① to T_{high} ②)		–	–	6.0	–	–	10	
Step Response (Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF)	t_f	–	0.8	–	–	0.8	–	µs
	t_{pd}	–	0.38	–	–	0.38	–	µs
	dV_{out}/dt ③	–	12	–	–	12	–	V/µs
(Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF)	t_f	–	0.6	–	–	0.6	–	µs
	t_{pd}	–	0.34	–	–	0.34	–	µs
	dV_{out}/dt ③	–	1.7	–	–	1.7	–	V/µs
(Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF)	t_f	–	2.2	–	–	2.2	–	µs
	t_{pd}	–	1.3	–	–	1.3	–	µs
	dV_{out}/dt ③	–	0.25	–	–	0.25	–	V/µs
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low} ① to T_{high} ②)	$\|TC_{Vio}\|$	–	1.5	–	–	1.5	–	µV/°C
($R_S \leqq$ 10 kΩ, T_A = T_{low} ① to T_{high} ②)		–	3.0	–	–	3.0	–	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} ① to +25°C)	$\|TC_{Iio}\|$	–	0.7	–	–	0.7	–	nA/°C
(T_A = +25°C to T_{high} ②)		–	0.7	–	–	0.7	–	
DC Power Dissipation (Total) (Power Supply = ±15 V, V_O = 0)	P_D	–	160	225	–	160	225	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	10	150	–	10	200	µV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	10	150	–	10	200	µV/V

① T_{low} = 0°C for MC1437
= −55°C for MC1537

② T_{high} = +75°C for MC1437
= +125°C for MC1537

③ dV_{out}/dt = Slew Rate

MATCHING CHARACTERISTICS

Characteristic	Symbol	MC1537 Min	MC1537 Typ	MC1537 Max	MC1437 Min	MC1437 Typ	MC1437 Max	Unit
Open Loop Voltage Gain	A_{VOL1}-A_{VOL2}	–	±1.0	–	–	±1.0	–	dB
Input Bias Current	I_{b1}-I_{b2}	–	±0.15	–	–	±0.15	–	µA
Input Offset Current	$\|I_{io1}\|$-$\|I_{io2}\|$	–	±0.02	–	–	±0.02	–	µA
Average Temperature Coefficient	$\|TC_{Iio1}\|$-$\|TC_{Iio2}\|$	–	±0.2	–	–	±0.2	–	nA/°C
Input Offset Voltage	$\|V_{io1}\|$-$\|V_{io2}\|$	–	±0.2	–	–	±0.2	–	mV
Average Temperature Coefficient	$\|TC_{Vio1}\|$-$\|TC_{Vio2}\|$	–	±0.5	–	–	±0.5	–	µV/°C
Channel Separation (f = 10 kHz)	$\frac{e_{out\,1}}{e_{out\,2}}$	–	90	–	–	90	–	dB

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TYPICAL OUTPUT CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT

$V^+ = +15$ Vdc, $V^- = 15$ Vdc, $T_A = 25^oC$

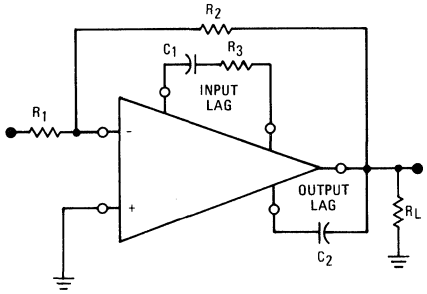


FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS $R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	C_1(pF)	C_2(pF)	OUTPUT NOISE (mV(rms))
4	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
5	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
6	1	A_{VOL}	0	∞	1.5 k	5.0 k	200	5.5
	2	A_{VOL}	0	∞	1.5 k	500	20	10.5
	3	A_{VOL}	0	∞	1.5 k	100	3.0	21.0
	4	A_{VOL}	0	∞	0	10	3.0	39.0
	5	A_{VOL}	0	∞	∞	0	3.0	—

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

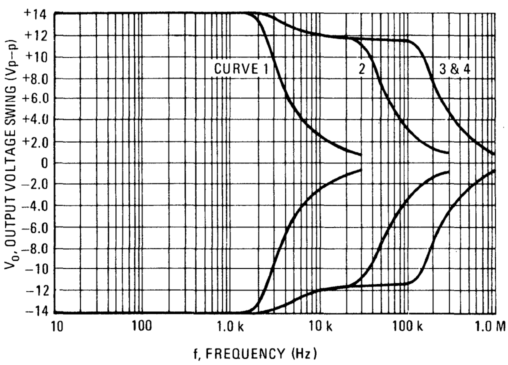


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

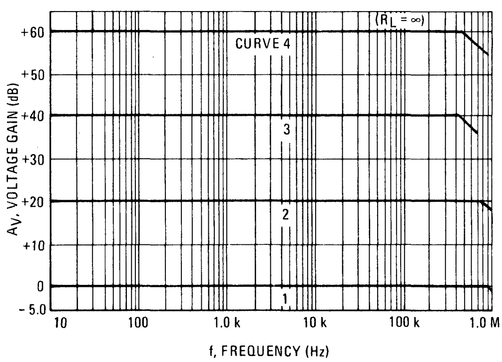


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

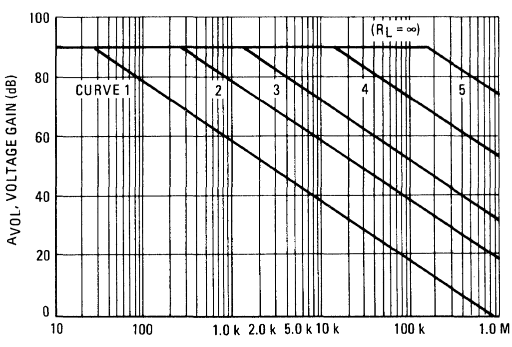
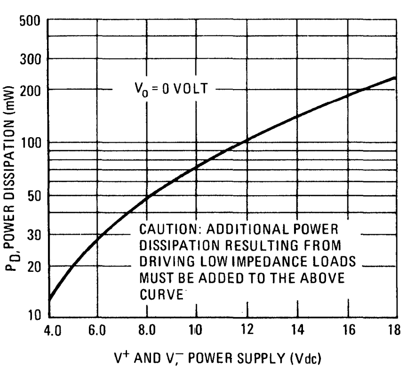


FIGURE 7 – TOTAL POWER DISSIPATION versus POWER SUPPLY VOLTAGE



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TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

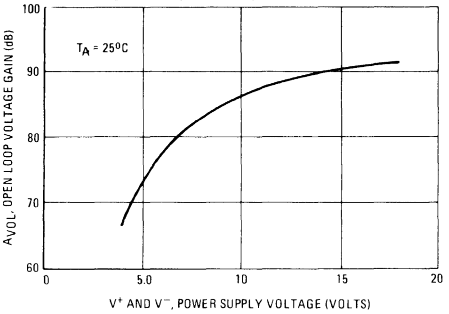


FIGURE 9 – COMMON INPUT SWING versus POWER SUPPLY VOLTAGE

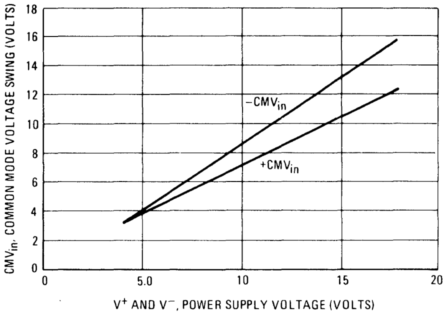


FIGURE 10 – INPUT OFFSET VOLTAGE versus TEMPERATURE

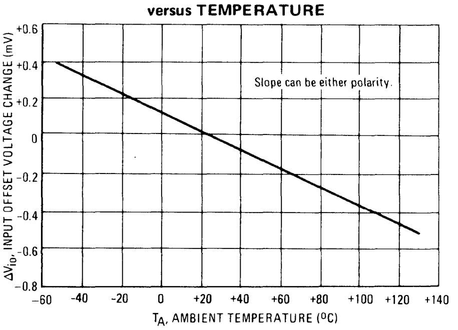


FIGURE 11 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE

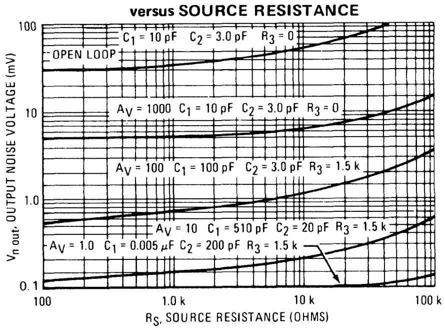
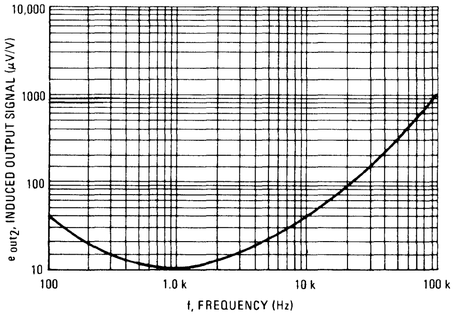
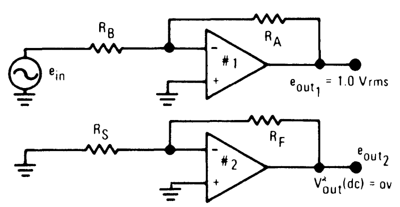


FIGURE 12 – INDUCED OUTPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced output signal (μV of induced output signal in amplifier #2 per volt of output signal at amplifier #1).

8

MC1538R
MC1438R

POWER BOOSTER

MONOLITHIC POWER BOOSTER

The MC1538/MC1438 is designed as a high current gain amplifier (70 dB), with unity voltage gain that can deliver load currents up to ±300 mAdc. This device is ideally suited to follow an operational amplifier (such as MC1556/MC1456) for driving low impedance loads and improving the overall circuit performance.

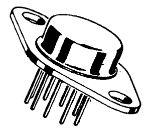
- High Input Impedance – 0.4 Meg-Ohm typ – when driving the MC1538/MC1438, the gain of an operational amplifier will approach the unloaded open-loop gain. Internal power dissipation of the operational amplifier will be independent of output voltage and therefore thermal drift will be reduced.
- Large Power Bandwidth – 1.5 MHz typ – considerably better than present operational amplifiers. Bandwidth and slew rate will be limited by the operational amplifier, not the MC1538/MC1438.
- Low Output Impedance – 10 Ohms typ – allows the MC1538/MC1438 to drive a capacitive load with greatly reduced phase shift compared with an operational amplifier. Output voltage swing capability is much increased when driving small load impedances.
- Adjustable Current Limit – ±5.0 mAdc to ±300 mAdc
- Excellent Power-Supply Rejection – 1.0 mV/V typ
- Current Gain – 3000 typ

POWER BOOSTER

INTEGRATED CIRCUIT FOR OPERATIONAL AMPLIFIERS

EPITAXIAL PASSIVATED

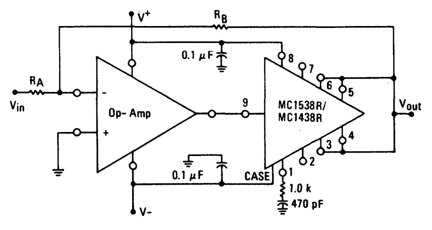
CASE 614



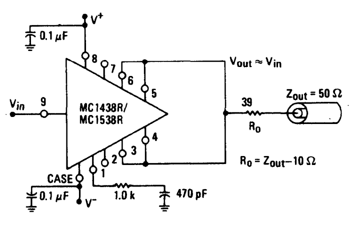
Case connected to V^-

TYPICAL APPLICATIONS

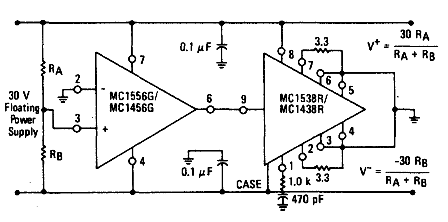
OPERATIONAL AMPLIFIER BOOST CIRCUIT



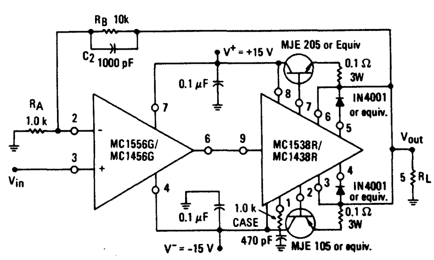
DIGITAL OR ANALOG LINE DRIVER



POWER SUPPLY SPLITTER



SERVO/POWER AMPLIFIER



See Packaging Information Section for outline dimensions.

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MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating	Symbol	MC1538R	MC1438R	Unit
Power Supply Voltage	V^+ V^-	+22 -22	+18 -18	Vdc
Input-Output Voltage Differential	$V_{in} - V_{out}$	-14.5, +44	-14, +36	Vdc
Input Voltage Swing	$\lvert V_{in} \rvert$	V^+ or V^-		Vdc
Load Current	I_L	350		mAdc
Power Dissipation and Thermal Characteristics T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air T_C = +25°C Derate above T_C = +25°C Thermal Resistance, Junction to Case	 P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JC}$ θ_{JC}	 3.0 24 41.6 17.5 140 7.15		 Watts mW/°C °C/W Watts mW/°C °C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

OPERATING TEMPERATURE RANGE

Ambient Temperature	MC1438R MC1538R	T_A	0 to +75 -55 to +125	°C

ELECTRICAL CHARACTERISTICS
(R_L = 300 ohms, T_C = +25°C unless otherwise noted.)

				MC1538R V^+ = +5 V to +20 V, V^- = -5 V to -20 V			MC1438R V^+ = +15 V, V^- = -15 V			
Characteristic (Linear Operation)	Fig	Note	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Voltage Gain (f = 1.0 kHz)	1	–	A_V	0.9	0.95	1.0	0.85	0.95	1.0	V/V
Current Gain ($A_I = \Delta I_o/\Delta I_{in}$)	1	–	A_I	–	3000	–	–	3000	–	A/A
Output Impedance (f = 1.0 kHz)	1	–	Z_{out}	–	10	–	–	10	–	Ohms
Input Impedance (f = 1.0 kHz)	1	–	Z_{in}	–	400	–	–	400	–	k ohms
Output Voltage Swing	1	3	V_{out}	±12	±13	–	±11	±12	–	Vdc
Input Bias Current	2	–	I_b	–	60	200	–	60	300	µAdc
Output Offset Voltage	2	1	V_{oo}	–	25	150	–	25	200	mVdc
Small Signal Bandwidth (R_L = 300 ohms) (V_{in} = 0 Vdc, v_{in} = 100 mV [rms])	1	–	$BW_{3\ dB}$	–	8.0	–	–	8.0	–	MHz
Power Bandwidth (V_{out} = 20 V_{p-p}, THD = 5%)	1	3	PBW	–	1.5	–	–	1.5	–	MHz
Total Harmonic Distortion (f = 1.0 kHz, V_{out} = 20 V_{p-p})	1	3	THD	–	0.5	–	–	0.5	–	%
Short-Circuit Output Current (R1 = R2 = ∞) (R1 = R2 = 3.3. ohms) Adjustable Range	 3 3 4,5	 2	I_{SC}	 75 – –	 95 300 5.0 to 300	 125 – –	 65 – –	 95 300 5.0 to 300	 140 – –	mAdc
Power Supply Sensitivity (V^- constant) (V^+ constant)	2	–	 S^+ S^-	 – –	 1.0 1.0	 – –	 – –	 1.0 1.0	 – –	mV/V
Power Supply Current (R_L = ∞, V_{in} = 0)	2	–	I_{D^+} or I_{D^-}	4.5	6.0	10	2.5	6.0	15	mAdc
Power Dissipation (R_L = ∞, V_{in} = 0.)	2	3	P_D	150	180	300	75	180	450	mW

Note 1. Output offset Voltage is the quiescent dc output voltage with the input grounded.
Note 2. Short-Circuit Current, I_{SC}, is adjustable by varying R1, R2, R3 and R4. The positive current limit is set by R1 or R3, and the negative current limit is set by R2 or R4. See Figures 4 and 5 for curves of short-circuit current versus R1, R2, R3 and R4.
Note 3. V^+ = +15 V, V^- = -15 V.

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TEST CIRCUITS

FIGURE 1

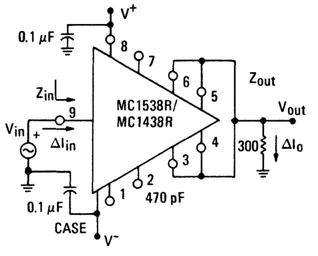


FIGURE 2

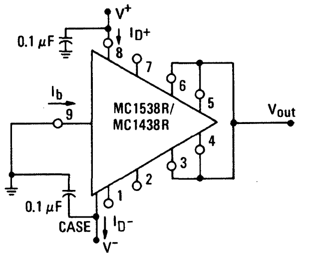
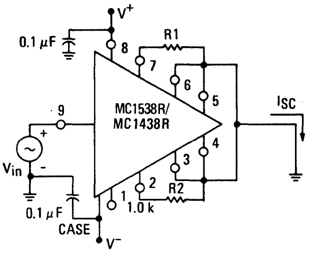
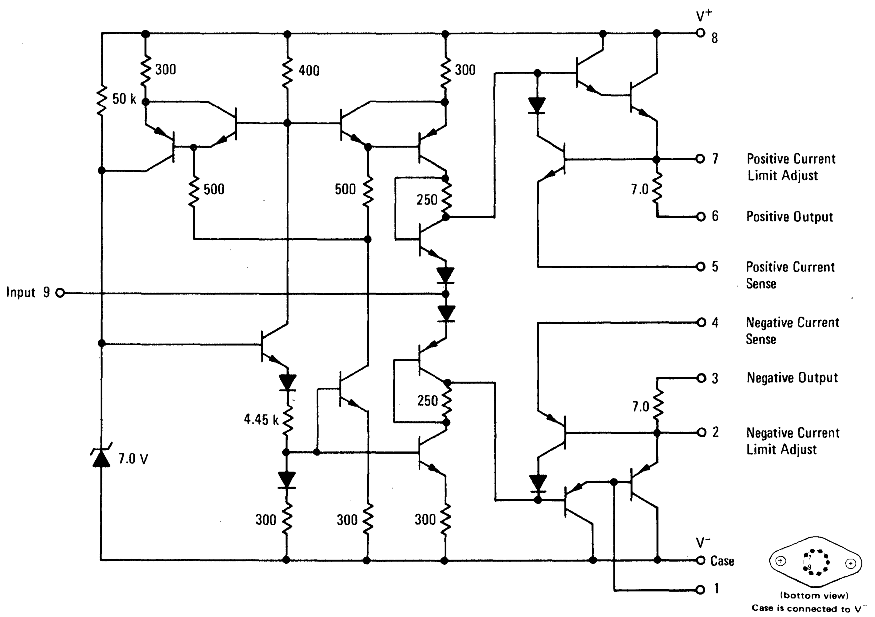


FIGURE 3



CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 4 – SHORT-CIRCUIT CURRENT versus R1 OR R2 (100 mA to 300 mA)

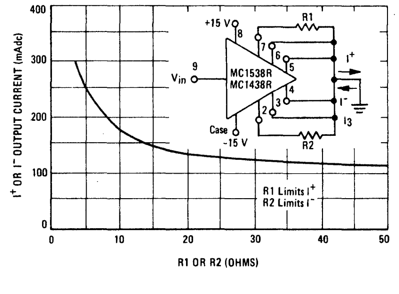
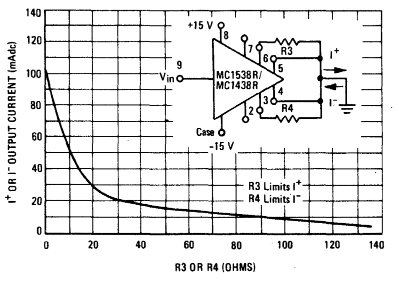


FIGURE 5 – SHORT-CIRCUIT CURRENT versus R3 OR R4 (5.0 mA to 100 mA)



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – POWER SUPPLY CURRENT versus SHUNT RESISTANCE

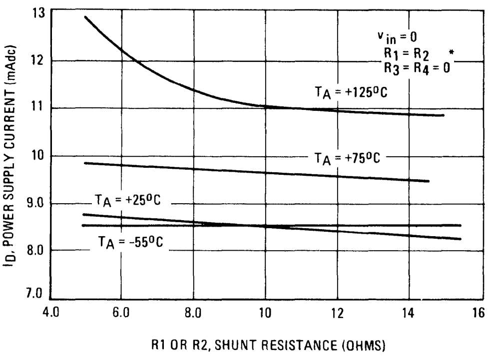


FIGURE 7 – SMALL SIGNAL GAIN AND PHASE RESPONSE

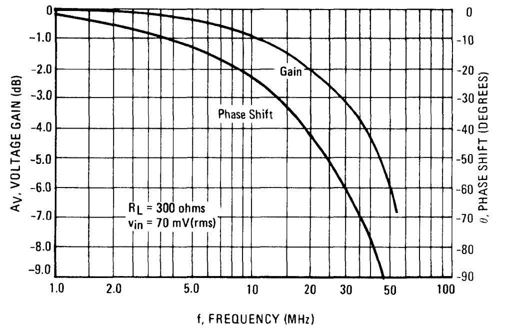


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD CURRENT

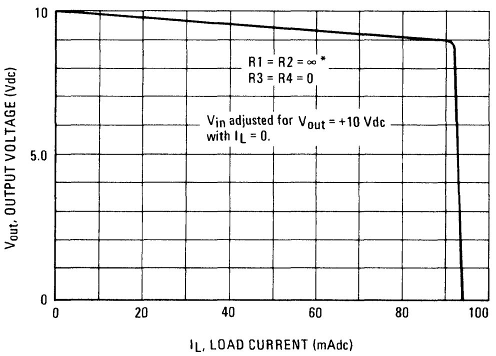


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD CURRENT

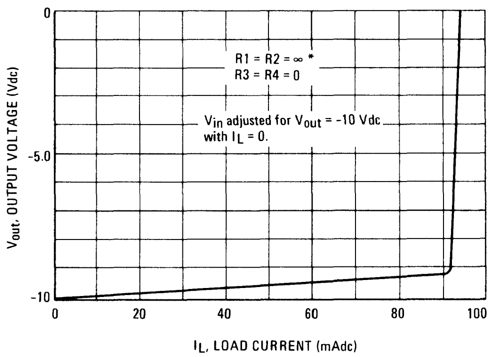


FIGURE 10 – OUTPUT OFFSET VOLTAGE versus TEMPERATURE

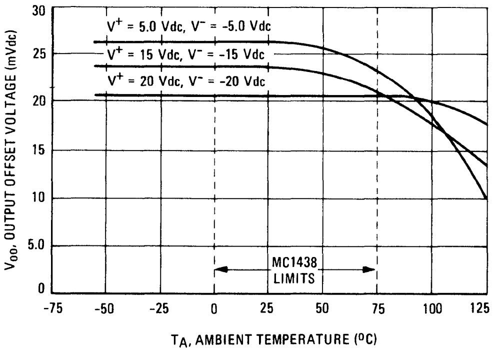
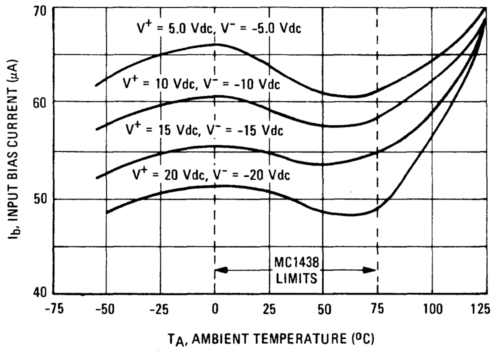


FIGURE 11 – INPUT BIAS CURRENT versus TEMPERATURE



*See figures 4 and 5 for definition of R1, R2, R3, and R4.

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TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^oC$ unless otherwise noted)

FIGURE 12 – PULSE RESPONSE CHARACTERISTICS

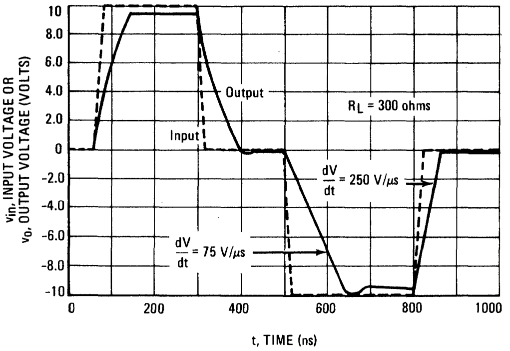
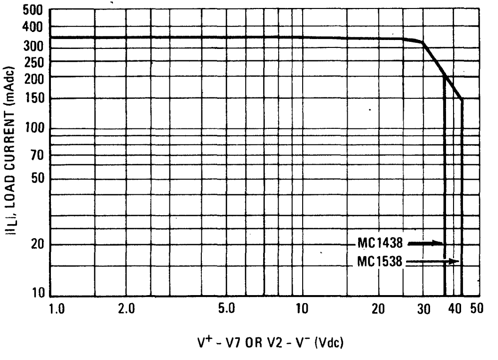
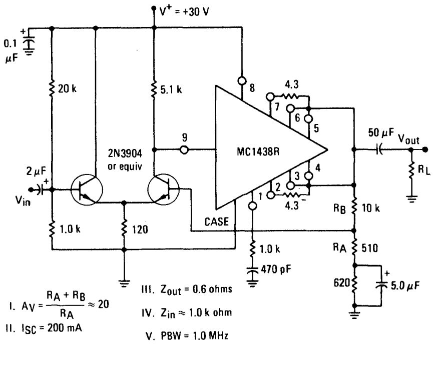


FIGURE 13 – DC SAFE OPERATING AREA



TYPICAL APPLICATIONS

FIGURE 14 – NON-INVERTING AC POWER AMPLIFIER



I. $A_V = \frac{R_A + R_B}{R_A} \approx 20$

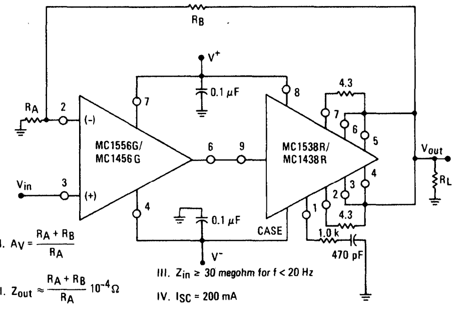
II. I_{SC} = 200 mA

III. Z_{out} = 0.6 ohms

IV. $Z_{in} \approx 1.0$ k ohm

V. PBW = 1.0 MHz

FIGURE 15 – NON-INVERTING POWER AMPLIFIER



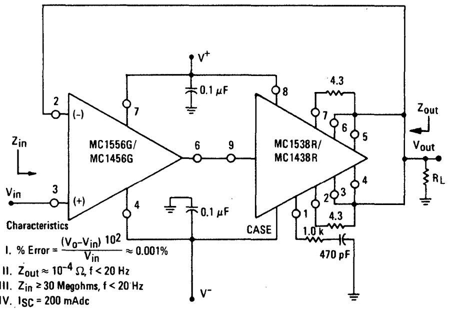
I. $A_V = \frac{R_A + R_B}{R_A}$

II. $Z_{out} \approx \frac{R_A + R_B}{R_A} 10^{-4} \Omega$

III. $Z_{in} \geq 30$ megohm for f < 20 Hz

IV. I_{SC} = 200 mA

FIGURE 16 – NON-INVERTING VOLTAGE FOLLOWER



Characteristics

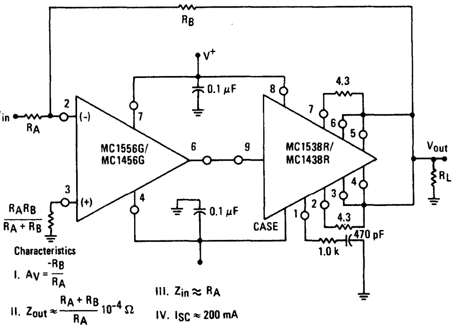
I. % Error = $\frac{(V_o - V_{in})\ 10^2}{V_{in}} \approx 0.001\%$

II. $Z_{out} \approx 10^{-4}\ \Omega$, f < 20 Hz

III. $Z_{in} \geq 30$ Megohms, f < 20 Hz

IV. I_{SC} = 200 mAdc

FIGURE 17 – INVERTING POWER AMPLIFIER



Characteristics

I. $A_V = \frac{-R_B}{R_A}$

II. $Z_{out} \approx \frac{R_A + R_B}{R_A} 10^{-4}\ \Omega$

III. $Z_{in} \approx R_A$

IV. $I_{SC} \approx 200$ mA

TYPICAL APPLICATIONS (continued)

FIGURE 18 – PROGRAMMABLE VOLTAGE SOURCE

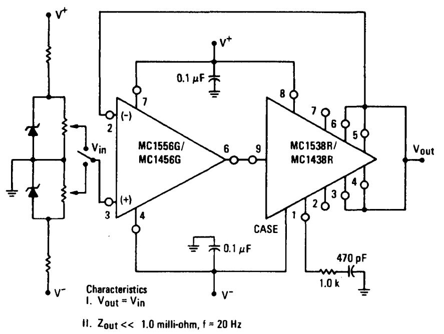


FIGURE 19 – CONSTANT CURRENT SOURCE OR TRANSCONDUCTANCE AMPLIFIER

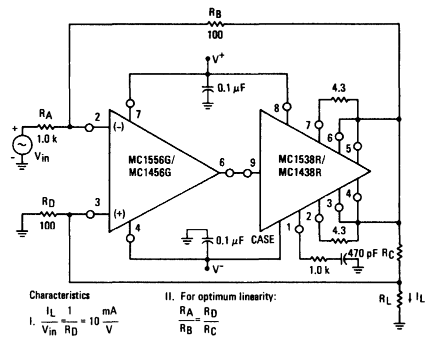


FIGURE 20 – SIGNAL DISTRIBUTION

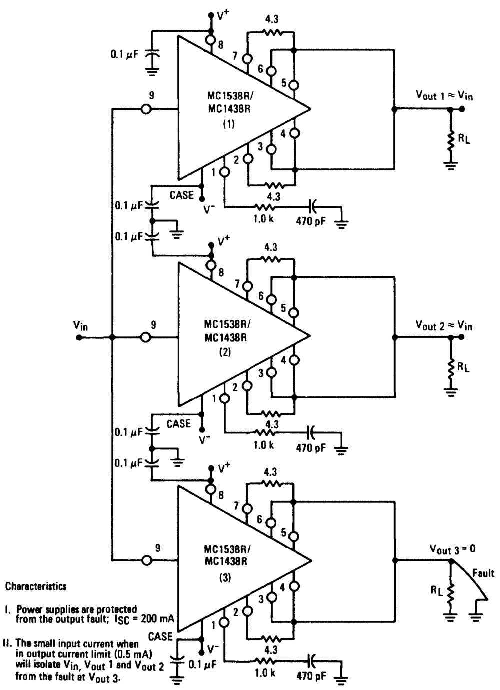


FIGURE 21 – ASTABLE MULTIVIBRATOR

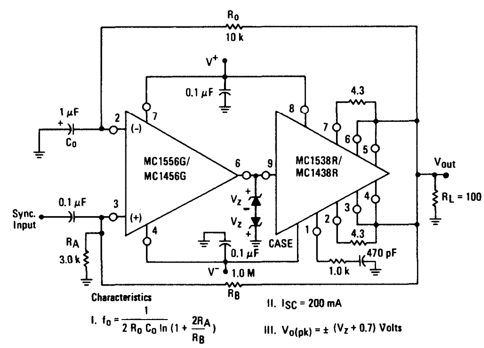
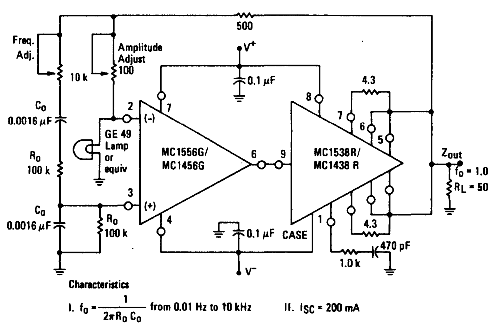


FIGURE 22 – WIEN BRIDGE OSCILLATOR



8

MC1539
MC1439

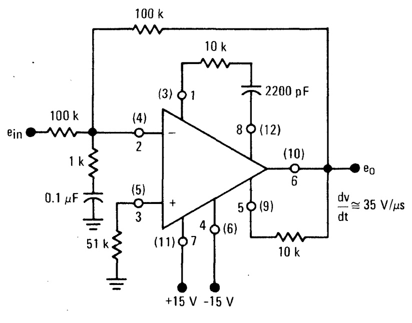
OPERATIONAL AMPLIFIERS

MONOLITHIC OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information see Motorola Application Note AN-439.

- Low Input Offset Voltage – 3.0 mV max
- Low Input Offset Current – 60 nA max
- Large Power-Bandwidth – 20 V_{p-p} Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- Slew Rate – 34 V/μs typ

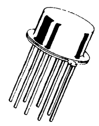
FIGURE 1 – HIGH SLEW-RATE INVERTER



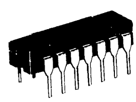
Pin numbers adjacent to terminals apply to 8-pin packages, numbers in parenthesis apply to 14-pin packages.

OPERATIONAL AMPLIFIER

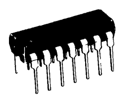
MONOLITHIC SILICON INTEGRATED CIRCUIT



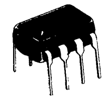
G SUFFIX
METAL PACKAGE
CASE 601



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

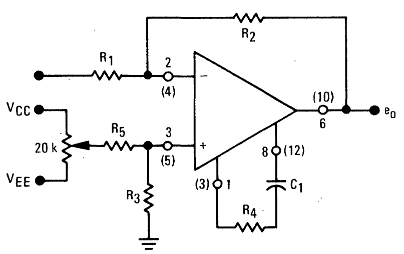


P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1439 only)



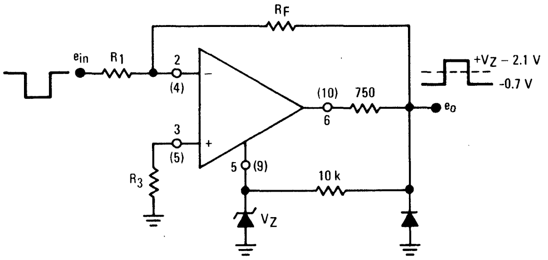
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1439 only)

FIGURE 2 – OUTPUT NULLING CIRCUIT



$10\ k \leq R_5 \leq 100(R_3)(V_{CC}+)$

FIGURE 3 – OUTPUT LIMITING CIRCUIT



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1539 Min	MC1539 Typ	MC1539 Max	MC1439 Min	MC1439 Typ	MC1439 Max	Unit
Input Bias Current	I_{IB}							μA
(T_A = +25°C)		–	0.20	0.50	–	0.20	1.0	
(T_A = T_{low} ①)		–	0.23	0.70	–	0.23	1.5	
Input Offset Current	$\|I_{IO}\|$							nA
(T_A = T_{low})		–	–	75	–	–	150	
(T_A = +25°C)		–	20	60	–	20	100	
(T_A = T_{high} ①)		–	–	75	–	–	150	
Input Offset Voltage	$\|V_{IO}\|$							mV
(T_A = +25°C)		–	1.0	3.0	–	2.0	7.5	
(T_A = T_{low}, T_{high})		–	–	4.0	–	–	–	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} to T_{high})	$\|TCV_{IO}\|$							μV/°C
(R_S = 50 Ω)		–	3.0	–	–	3.0	–	
($R_S \leq$ 10 kΩ)		–	5.0	–	–	5.0	–	
Input Impedance (f = 20 Hz)	z_{in}	150	300	–	100	300	–	kΩ
Input Common-Mode Voltage Swing	V_{ICR}	±11	±12	–	±11	±12	–	V_{pk}
Equivalent Input Noise Voltage (R_S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	e_n	–	30	–	–	30	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 1.0 kHz)	CMRR	80	110	–	80	110	-	dB
Open-Loop Voltage Gain (V_O = ±10 V, R_L = 10 kΩ, R_5 = ∞) (T_A = +25°C to T_{high})	A_{vol}	50,000	120,000	–	15,000	100,000	–	–
(T_A = T_{low})		25,000	100,000	–	15,000	100,000	–	
Power Bandwidth (A_v = 1, THD $\leq$ 5%, V_O = 20 Vp-p)	PBW							kHz
(R_L = 2.0 kΩ)		–	–	–	10	50	–	
(R_L = 1.0 kΩ, R_5 = 10 k)		20	50	–	–	–	–	
Step Response								
Gain = 1000, no overshoot,	t_{PHL}	–	130	–	–	130	–	ns
R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ,	t_p	–	190	–	–	190	–	ns
R4 = 30 kΩ, R5 = 10 kΩ, C1 = 1000 pF	dV_O/dt ②	–	6.0	–	–	6.0	–	V/μs
Gain = 1000, 15% overshoot,	t_{PHL}	–	80	–	–	80	–	ns
R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ,	t_p	–	100	–	–	100	–	ns
R4 = 0, R5 = 10 kΩ, C1 = 10 pF	dV_O/dt	–	14	–	–	14	–	V/μs
Gain = 100, no overshoot,	t_{PHL}	–	60	–	–	60	–	ns
R1 = 1.0 kΩ, R2 = 100 kΩ, R3 = 1.0 kΩ,	t_p	–	100	–	–	100	–	ns
R4 = 10 kΩ, R5 = 10 kΩ, C1 = 2200 pF	dV_O/dt	–	34	–	–	34	–	V/μs
Gain = 10, 15% overshoot,	t_{PHL}	–	120	–	–	120	–	ns
R1 = 1.0 kΩ, R2 = 10 kΩ, R3 = 1.0 kΩ,	t_p	–	80	–	–	80	–	ns
R4 = 1.0 kΩ, R5 = 10 kΩ, C1 = 2200 pF	dV_O/dt	–	6.25	–	–	6.25	–	V/μs
Gain = 1, 15% overshoot,	t_{PHL}	–	160	–	–	160	–	ns
R1 = 10 kΩ, R2 = 10 kΩ, R3 = 5.0 kΩ,	t_p	–	80	–	–	80	–	ns
R4 = 390 Ω, R5 = 10 kΩ, C1 = 2200 pF	dV_O/dt	–	4.2	–	–	4.2	–	V/μs
Output Impedance (f = 20 Hz)	z_o	–	4.0	–	–	4.0	–	kΩ
Output Voltage Swing	V_O							V_{pk}
(R_L = 2.0 kΩ, f = 1.0 kHz)		–	–	–	±10	±13	–	
(R_L = 1.0 kΩ, f = 1.0 kHz)		±10	±13	–	–	–	–	
Positive Supply Sensitivity (V_{EE} constant, R_5 = ∞)	S^+	–	50	150	–	50	200	μV/V
Negative Supply Sensitivity (V_{CC} constant, R_5 = ∞)	S^-	–	50	150	–	50	200	μV/V
Power Supply Current (V_O = 0)	I_D+	–	3.0	5.0	–	3.0	6.7	mAdc
	I_D-	–	3.0	5.0	–	3.0	6.7	

① T_{low} = 0°C for MC1439, −55°C for MC1539; T_{high} = +75°C for MC1439, +125°C for MC1539

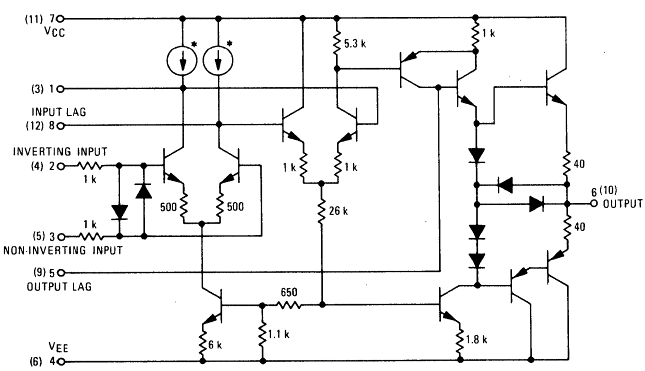
② dV_O/dt = Slew Rate

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 +18	Vdc
Differential Input Signal Voltage	V_{in}	$\pm(V_{CC} + \lvert V_{EE} \rvert)$	Vdc
Common-Mode Input Swing Voltage	V_{ICR}	$+V_{CC}, -\lvert V_{EE} \rvert$	Vdc
Load Current	I_L	15	mA
Output Short-Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C Plastic Dual In-Line Packages MC1439 Derate above T_A = +25°C	P_D	 680 4.6 750 6.0 625 5.0	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range MC1539 MC1439	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 -65 to +150 -55 to +125	°C

FIGURE 4 – CIRCUIT SCHEMATIC



Pin numbers adjacent to terminals apply to 8-pin packages, numbers in parenthesis apply to 14-pin packages.
Pin 7 is electrically connected to the substrate and V_{EE} for Case 646 only.
*Patent pending.

FIGURE 5 – EQUIVALENT CIRCUIT

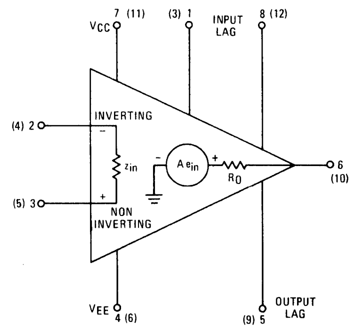
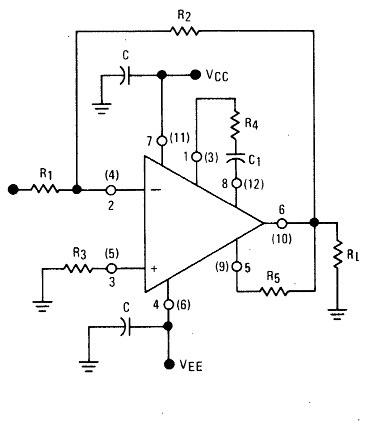


FIGURE 6 – TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS
(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C.)

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS (FIGURE 6)					
			R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	R_5 (Ω)	C_1 (pF)
7,8,10,12	1 2 3 4 5 6	A_{vol} 1 10 100 1000 1000	0 10 k 1.0 k 1.0 k 1.0 k 1.0 k	∞ 10 k 10 k 100 k 1.0 M 1.0 M	0 5.0 k 1.0 k 1.0 k 1.0 k 1.0 k	∞ 390 1.0 k 10 k 30 k 0	∞ 10 k 10 k 10 k 10 k 10 k	0 2200 2200 2200 1000 10
13	ALL	1	10 k	10 k	5.0 k	390	10 k	2200
14	ALL	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
15	ALL	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
16	ALL	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	2200

8

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 7 – LARGE-SIGNAL SWING versus FREQUENCY

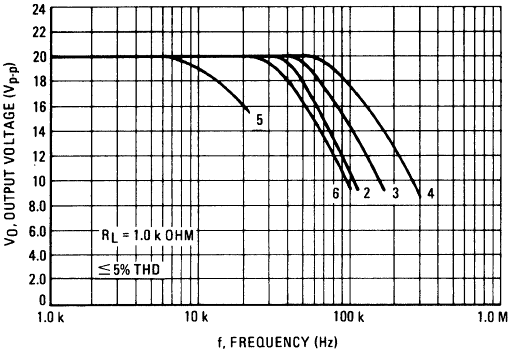


FIGURE 8 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

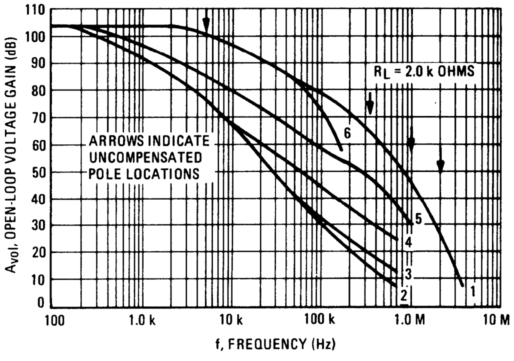


FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

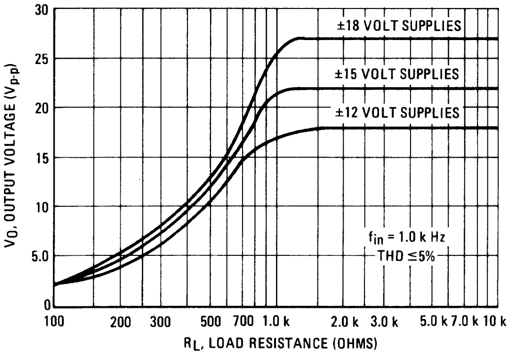


FIGURE 10 – OPEN-LOOP PHASE-SHIFT versus FREQUENCY

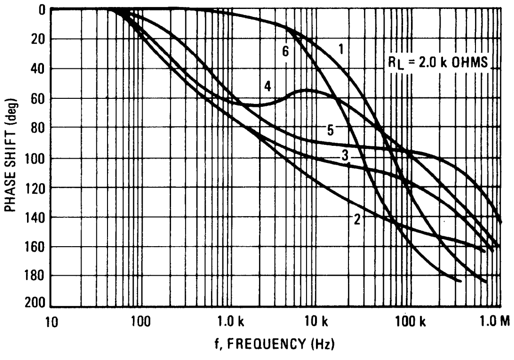


FIGURE 11 – OUTPUT VOLTAGE SWING (to clipping) versus SUPPLY

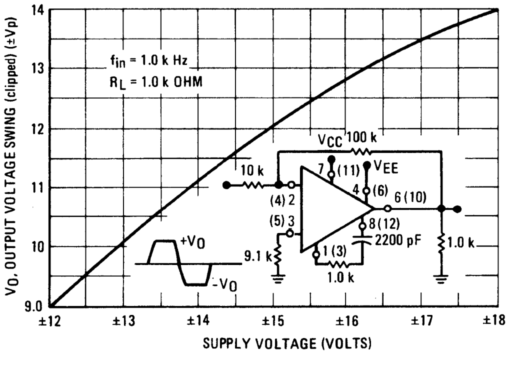
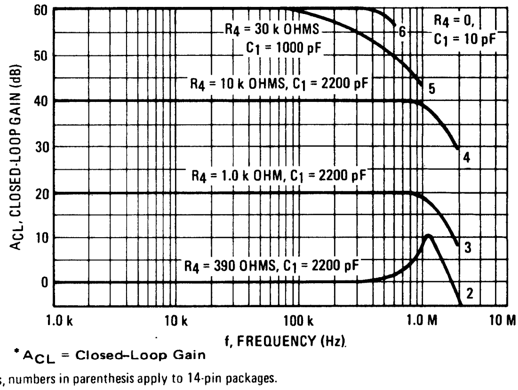


FIGURE 12 – CLOSED-LOOP GAIN versus FREQUENCY



*A_{CL} = Closed-Loop Gain

Pin numbers adjacent to terminals apply to 8-pin packages, numbers in parenthesis apply to 14-pin packages.

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 13 – A_{CL}* = 1 RESPONSE versus TEMPERATURE

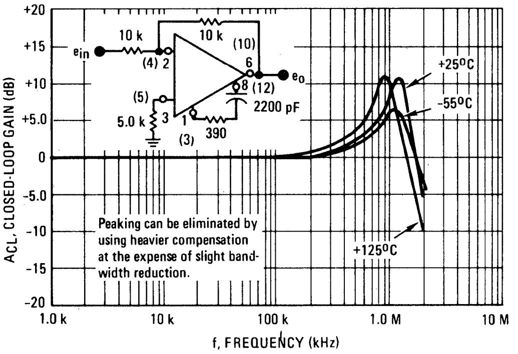


FIGURE 14 – A_{CL} = 10 RESPONSE versus TEMPERATURE

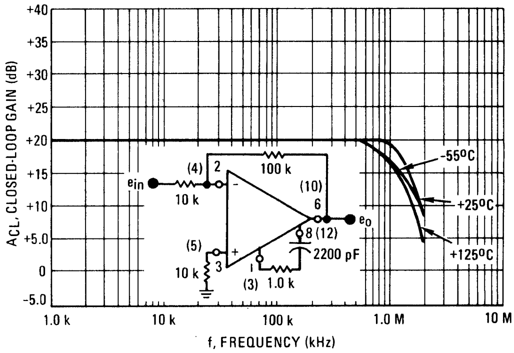


FIGURE 15 – A_{CL} = 100 RESPONSE versus TEMPERATURE

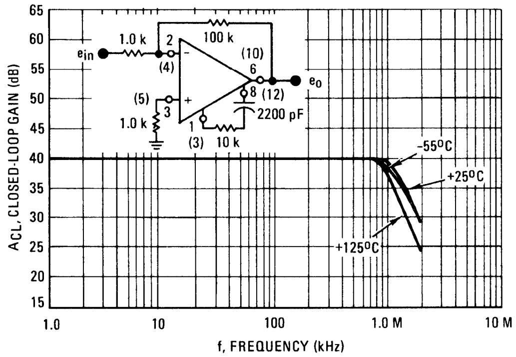


FIGURE 16 – A_{CL} = 1000 RESPONSE versus TEMPERATURE

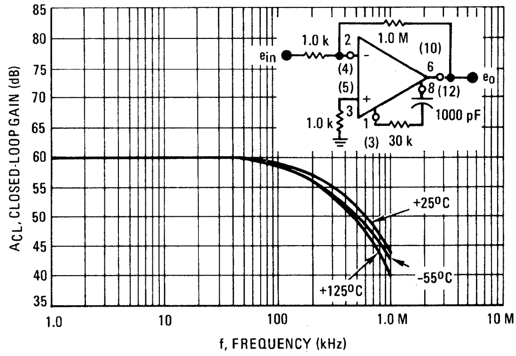


FIGURE 17 – SPECTRAL NOISE DENSITY

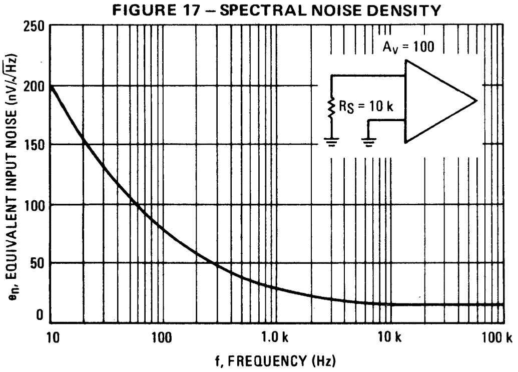
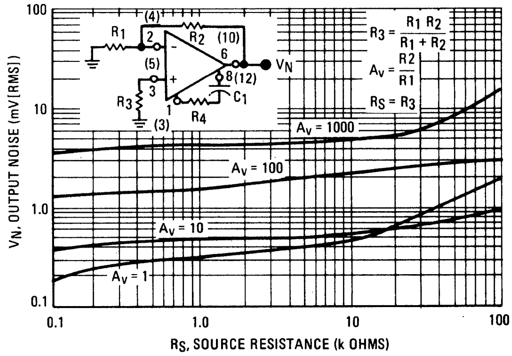


FIGURE 18 – OUTPUT NOISE versus SOURCE RESISTANCE



*A_{CL} = Closed-Loop Gain

Pin numbers adjacent to terminals apply to 8-pin packages, numbers in parenthesis apply to 14-pin packages.

8

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 19 – POWER DISSIPATION versus TEMPERATURE

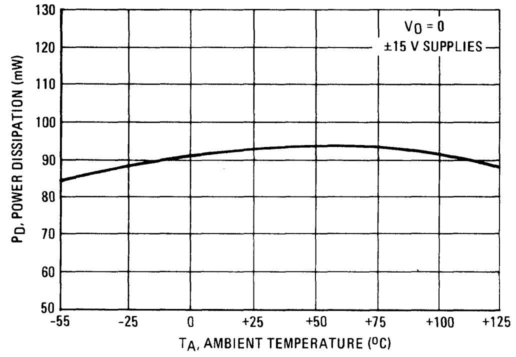


FIGURE 20 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

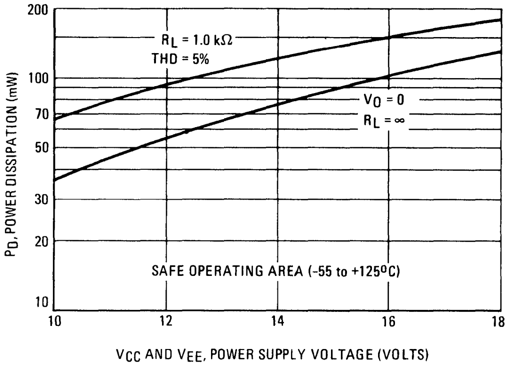


FIGURE 21 – POWER BANDWIDTH (LARGE-SIGNAL SWING versus FREQUENCY)

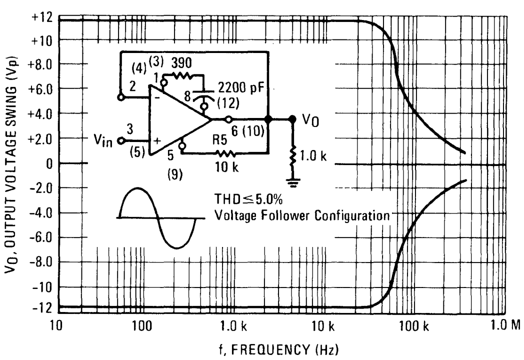


FIGURE 22 – COMMON-MODE INPUT VOLTAGE versus SUPPLY VOLTAGE

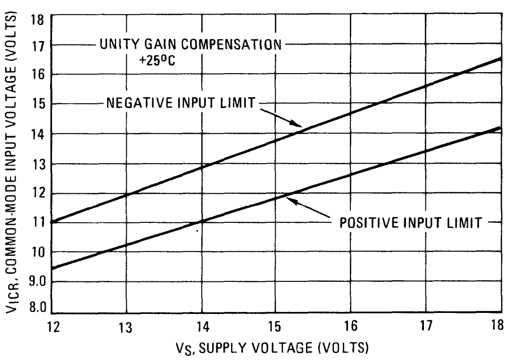


FIGURE 23 – COMMON-MODE REJECTION RATIO versus FREQUENCY

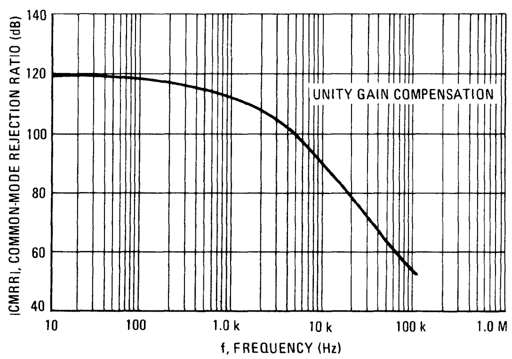
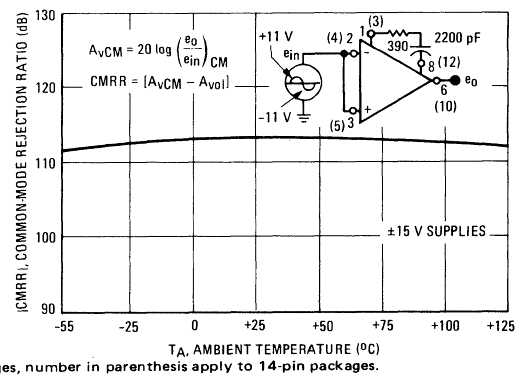


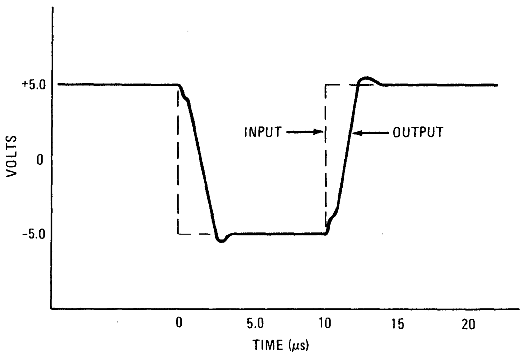
FIGURE 24 – COMMON-MODE REJECTION RATIO versus TEMPERATURE



Pin numbers adjacent to terminals apply to 8-pin packages, number in parenthesis apply to 14-pin packages.

8

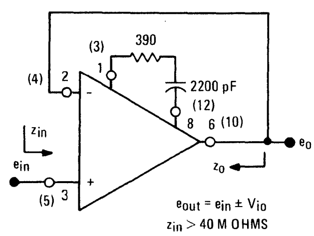
FIGURE 25 – VOLTAGE-FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

Pin numbers adjacent to terminals apply to 8-pin packages, numbers in parenthesis apply to 14-pin packages.

FIGURE 26 – VOLTAGE FOLLOWER

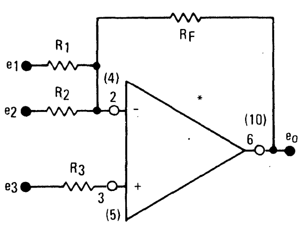


$e_{out} = e_{in} \pm V_{io}$

$z_{in} > 40$ M OHMS

$$z_{oCL} = z_{oOL}\left[\frac{1 + \frac{R_F}{R_i}}{A_{ol}}\right] = 4\,k\left[\frac{1+0}{10^5}\right] \approx 0.04 \text{ OHM}$$

FIGURE 27 – DIFFERENTIAL AMPLIFIER

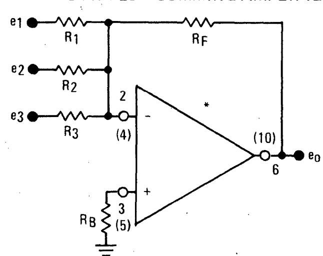


$$e_o = -\left[\frac{R_F}{R_1}\,e1 + \frac{R_F}{R_2}\,e2\right] + \left[1 + \frac{R_F}{R_3}\right] e3$$

$$\text{For } R_3 = \frac{R_1, R_2}{R_1 + R_2}$$

*Properly Compensated

FIGURE 28 – SUMMING AMPLIFIER

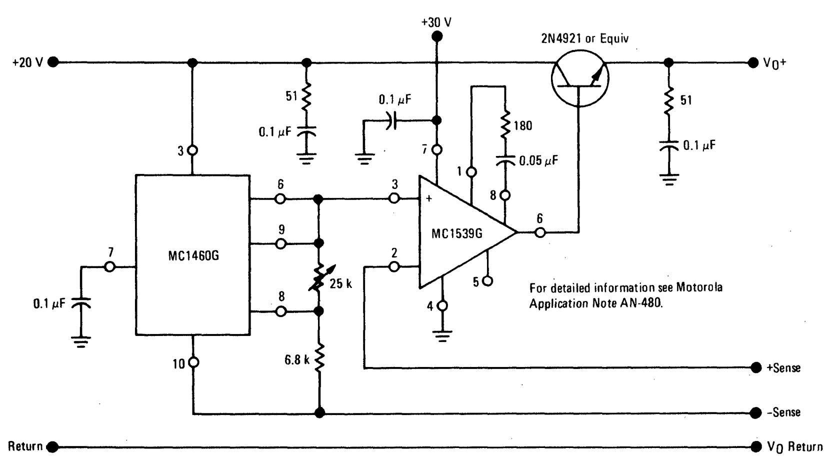


R_B = Parallel Combination of R_1, R_2, R_3, R_F.

$$e_o = -\left[\frac{R_F}{R_1}\,e1 + \frac{R_F}{R_2}\,e2 + \frac{R_F}{R_3}\,e3\right]$$

*Properly Compensated

FIGURE 29 – +15 VOLT REGULATOR



For detailed information see Motorola Application Note AN-480.

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TYPICAL APPLICATIONS (continued)

FIGURE 30 – LOAD REGULATION FOR CIRCUIT OF FIGURE 29

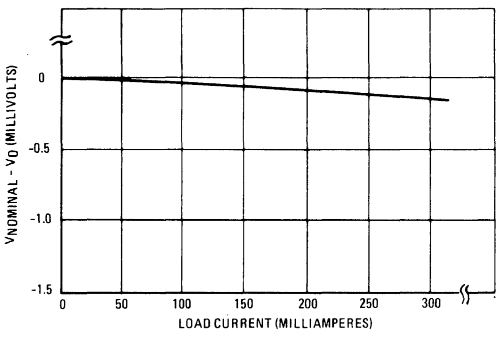
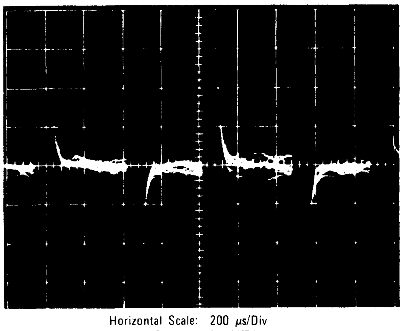


FIGURE 31 – REGULATOR OUTPUT VOLTAGE (under pulsed load condition)



Horizontal Scale: 200 μs/Div
Vertical Scale: 1 mV/Div

8

MC1540
MC1440

SENSE AMPLIFIERS

MONOLITHIC SENSE AMPLIFIER

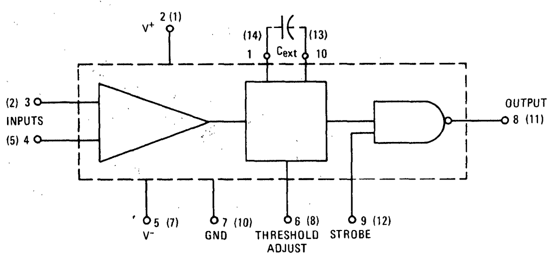
. . . consisting of a wideband differential amplifier, a dc restoration circuit which also incorporates facilities to externally adjust the threshold, and an MDTL output gate which is strobed from saturated logic. It is designed to detect bipolar differential signals derived by a core memory with cycle times as low as 0.5 μs.

- Differential Threshold Characteristics:
  - Adjustable Threshold – 10-25 mV
  - Nominal Threshold – 17 mV @ V_6 = -6 V
  - Input Offset Voltage – 1.0 mV typical
  - Threshold Drift – -10 μV/°C typical
- Fast Response Time – 20 ns typical
- Short Recovery Time:
  - 50 ns max @ e_{in} = 1.8 V Common Mode
  - 50 ns max @ e_{in} = 400 mV Differential Mode

CORE MEMORY SENSE AMPLIFIER INTEGRATED CIRCUIT

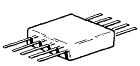
SILICON EPITAXIAL PASSIVATED

MC1540/MC1440 BLOCK DIAGRAM

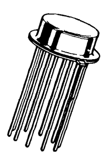


Number at end of terminal represents pin number for devices in flat package and metal can. Number in parenthesis represents pin number for dual in-line package.

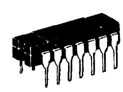
F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



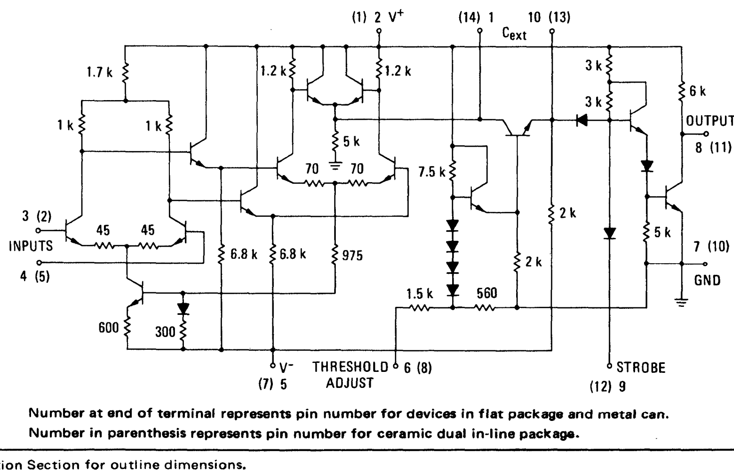
G SUFFIX
METAL PACKAGE
CASE 602B



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



CIRCUIT SCHEMATIC



Number at end of terminal represents pin number for devices in flat package and metal can.
Number in parenthesis represents pin number for ceramic dual in-line package.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+10 -10	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Vdc
Common Mode Input Voltage	CMV_{in}	±5.0	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C Flat Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 500 3.3 625 5.0	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range MC1440F,G,L MC1540F,G,L	T_A	 0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS
(V^+ = +6 Vdc ± 1%, V^- = -6 Vdc ± 1%, C_{ext} = 0.01 μF, T_A = +25°C unless otherwise noted)
Pin number references are for devices in flat package and metal can.
See block diagram for dual in-line package pin numbers.

			MC1540			MC1440			
Characteristic	Fig. No.	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input Threshold Voltage (V_6 = -6.0 Vdc, T_A = 25°C) (V_6 = -6.0 V, T_A = T_{low}*) (V_6 = -6.0 V, T_A = T_{high}*)	1	V_{th}	 14 12 12	 17 17 17	 20 24 22	 12 10 10	 17 17 17	 24 30 30	mV
Input Offset Voltage	1	V_{io}	–	1.0	5.0	–	1.0	6.0	mV
Input Bias Current (V_3 = V_4 = 0, T_A = 25°C) (V_3 = V_4 = 0, T_A = T_{low}*)	2	I_b	 – –	 7.5 –	 50 100	 – –	 7.5 –	 75 100	μA
Input Offset Current	2	I_{io}	–	2.0	10	–	2.0	15	μA
Output Voltage High (V_3 = V_4 = 0)	3	V_{OH}	5.9	–	–	5.8	–	–	Vdc
Output Voltage Low (V_3 = V_4 = 0, V_{10} = +6.0 Vdc, I_8 = 6.0 mAdc) (V_{10} = +6.0 Vdc, I_8 = 6.0 mAdc, T_A = T_{high}*)	3	V_{OL}	 – –	 – –	 350 400	 – –	 – –	 400 450	mVdc
Amplifier Voltage Gain (V_3 = 15 mV peak)	4	A_V	–	85	–	–	85	–	–
Strobe Load Current (V_9 = 0)	–	I_S	–	–	1.2	–	–	1.5	mAdc
Strobe Reverse Current (V_9 = +5.0 Vdc) (V_9 = +6.0 Vdc, T_A = T_{high}*)	–	I_R	 – –	 – –	 2.0 25	 – –	 – –	 5.0 30	μAdc
Propagation Delay Input to Amplifier Output (V_3 = 25 mV pulse, V_9 = +2.0 Vdc)	5	t_{3+10+}	–	10	15	–	10	20	ns
Input to Gate Output (V_3 = 25 mV pulse, V_9 = +2.0 Vdc)	5	t_{3+8-}	–	20	30	–	20	50	
Strobe to Gate Output (V_3 = V_4 = 0, V_9 = +2.0 V pulse)	6	t_{9+8-}	–	10	15	–	10	30	
Recovery Time Differential Mode (V_3 = 400 mV pulse)	7	$t_{R(dm)}$	–	20	50	–	20	90	ns
Common Mode (V_3 = 1.8 V pulse)	8	$t_{R(cm)}$	–	20	50	–	20	60	
Power Dissipation	–	P_D	–	120	180	–	120	250	mW

*T_{low} = -55°C for MC1540 or 0°C for MC1440, T_{high} = +125°C for MC1540 or +75°C for MC1440.

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A_V Amplifier Voltage Gain — the ratio of output voltage at pin 1 to the input voltage at pin 3 or 4

I_b Input Bias Current — the average input current defined as $(I_3 + I_4)/2$

I_{io} Input Offset Current — the difference between input current values, $|I_3 - I_4|$

I_R Strobe Reverse Current — leakage current when the strobe input is high

I_S Strobe Load Current — amount of current drain from the circuit when the strobe pin is grounded

P_D Power Dissipation — amount of power dissipated in the unit as defined by $|I_2 \times V^+| + |I_5 \times V^-|$

t_R Recovery Time — The time that is required for the device to recover from the specified differential and common-mode overload inputs prior to strobe as reference to the 10% point of the trailing edge of an input pulse. The device is considered recovered when the threshold after a differential overload disturbance is within 1.0 mV of the threshold value without the disturbance, or, for common-mode disturbance, when the level at pin 10 is within 100 mV of the quiescent value.

$t_{x\pm y\pm}$ Propagation Delay — The time that is required for the output pulse at pin y to achieve 50% of its final value or the 1.5 V level referenced to 50% of the input pulse at pin x. (The + and - denote positive and negative-going pulse transition.)

V_{OH} Output Voltage High — high-level output voltage when the output gate is turned off

V_{OL} Output Voltage Low — low-level output voltage when the output gate is turned on

V_{th} Input Threshold — input pulse amplitude that causes the output to begin saturation

V_{io} Input Offset Voltage — the difference in V_{th} at each input

FIGURE 1 — INPUT THRESHOLD AT OUTPUT VOLTAGE SWING FROM V_{OL} TO V_{OH}

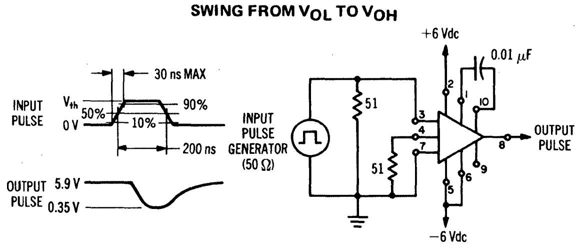


FIGURE 2 — INPUT BIAS CURRENT TEST CIRCUIT

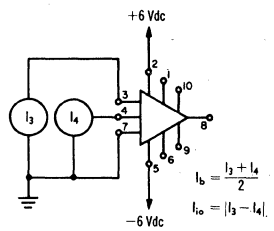


FIGURE 3 — OUTPUT VOLTAGE LEVELS

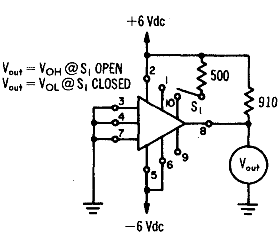


FIGURE 4 — AMPLIFIER VOLTAGE GAIN

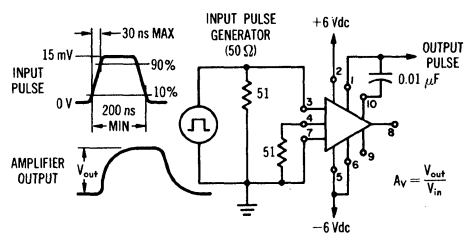


FIGURE 5 — PROPAGATION DELAY (STROBE HIGH)

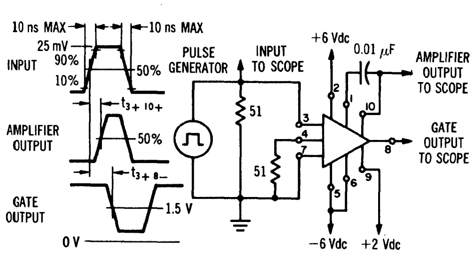


FIGURE 6 — PROPAGATION DELAY (STROBE INPUT)

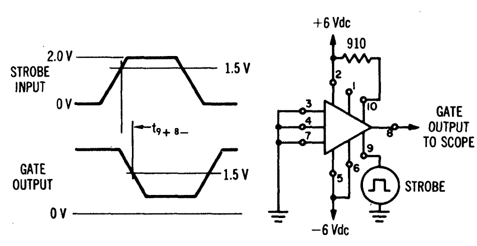


FIGURE 7 – DIFFERENTIAL MODE RECOVERY TIME TEST CIRCUIT

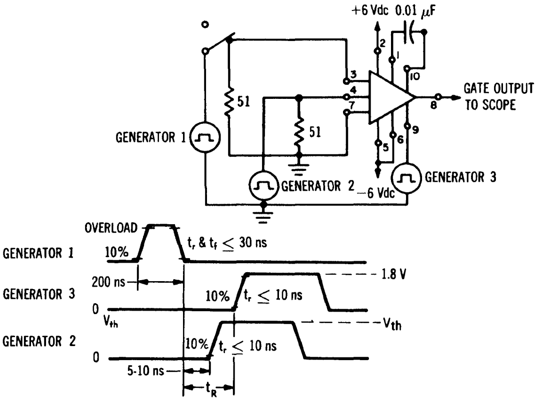
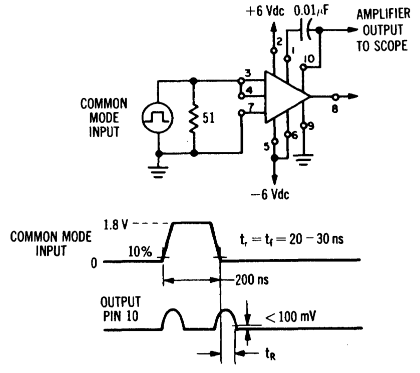


FIGURE 8 – COMMON MODE RECOVERY TIME TEST CIRCUIT



NOTE: The output shown is representative of that obtained. However, the two pulse amplitudes may not be equal or even present.

Pin numbers shown for devices in flat package and metal can. See block diagram for dual in-line package pin numbers.

FIGURE 9 – TYPICAL TRANSFER CHARACTERISTICS

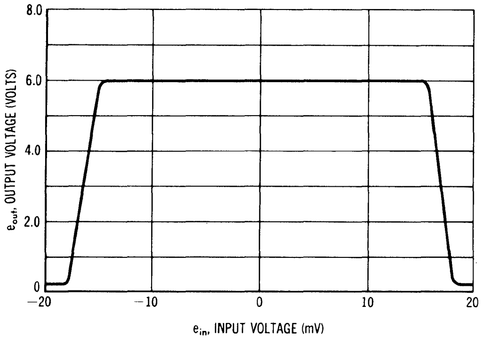


FIGURE 10 – TYPICAL THRESHOLD versus TEMPERATURE

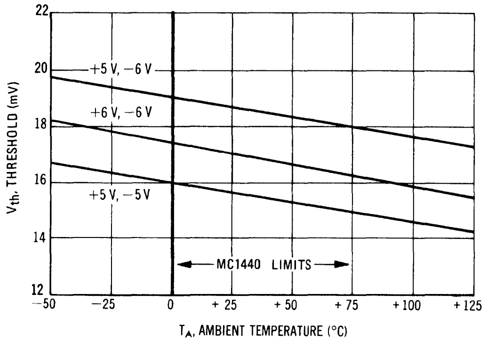


FIGURE 11 – TYPICAL THRESHOLD versus POWER SUPPLIES
T_A = +25°C (Threshold Adjust Attached to V⁻)

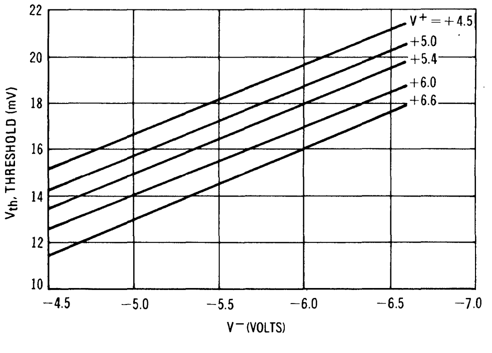
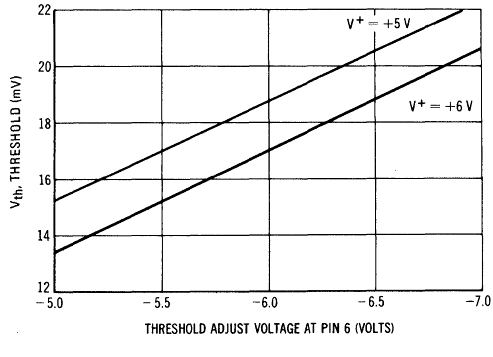


FIGURE 12 – TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST FOR V^- = 6.0V



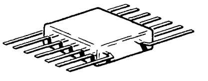
For a more detailed discussion regarding application of sense amplifiers, see Motorola Application Note AN-245, "The MC1540 – An Integrated Core Memory Sense Amplifier."

8

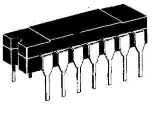
MC1541
MC1441

SENSE AMPLIFIERS

Dual-channel gated sense amplifier with separate wideband differential input amplifiers. Either input can be gated on from saturated logic levels. The sense amplifier features adjustable threshold, saturated logic output levels, and a strobe input that accommodates saturated logic levels. Designed to detect bipolar signals from either of two sense lines. Operates with core memory cycle times less than 0.5 μs.



F SUFFIX
CERAMIC PACKAGE
CASE 607



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

Typical Amplifier Features:

- Nominal Threshold – 17 mV
- Input Offset Voltage – 1.0 mV typical
- Propagation Delay
  - Input to Gate-Output – 20 ns
  - Input to Amplifier-Output – 10 ns
  - Gate Response Time – 15 ns
  - Strobe Response Time – 15 ns
- Common Mode Input Range – 1.5 Volts
- Differential Mode Input Range
  - With Gate On – 600 mV
  - With Gate Off – 1.5 Volts
- Power Dissipation – 140 mW typical

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+10 -10	Vdc Vdc
Differential Input Signal	V_{in}	±5	Vdc
Common Mode Input Voltage	CMV_{in}	±5	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Flat Package Derate above 25°C Ceramic Dual In-Line Package Derate above 25°C	P_D	 500 3.3 600 4.8	 mW mW/°C mW mW/°C
Operating Temperature Range MC1541F, MC1541L MC1441F, MC1441L,	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

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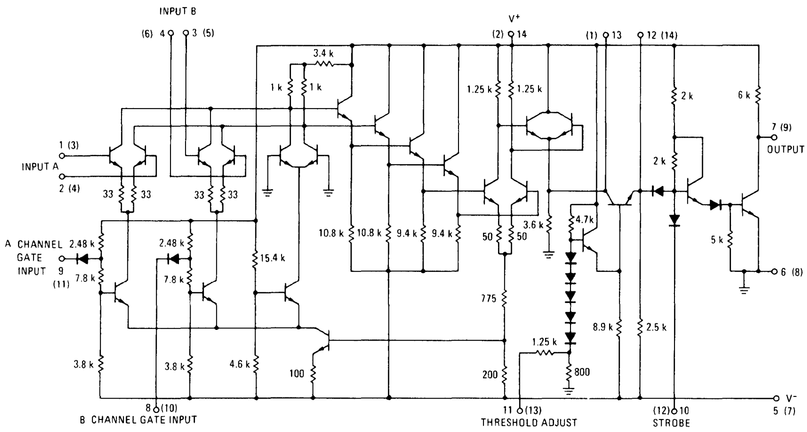
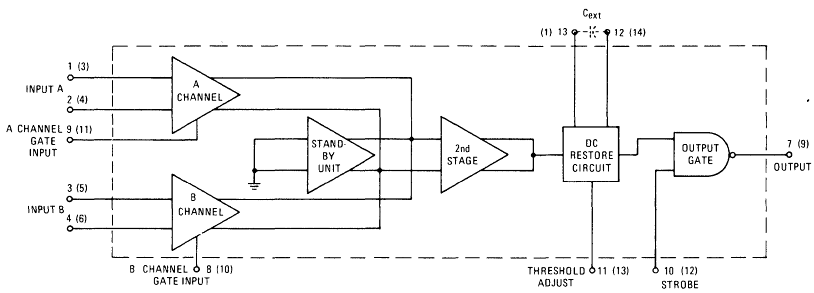
CIRCUIT SCHEMATIC



Number at terminal end denotes pin number for flat (F) package.
Number in parenthesis denotes pin number for dual in-line ceramic (L) package.

LOGIC DIAGRAM



Number at terminal end denotes pin number for flat package. Number in parenthesis denotes pin number for dual in-line package.

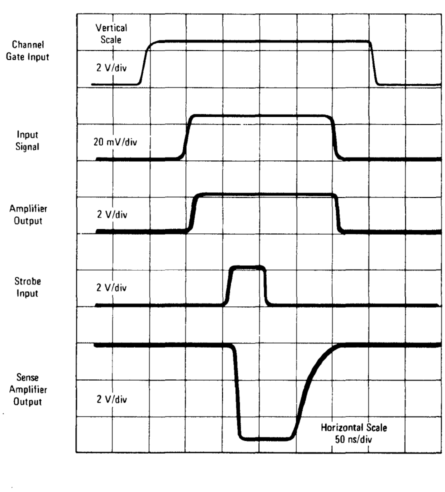


FIGURE 1 – TYPICAL OPERATION

8

ELECTRICAL CHARACTERISTICS

(V^+ = +5.0 Vdc ± 1%, V^- = 5.0 Vdc ± 1%, $V_{th(pin\ 11)}$ = -5.0 Vdc ± 1%, C_{ext} = 0.01 µF, T_A = 25°C unless otherwise noted)
(T_{low} = -55°C for MC1541 or 0°C for MC1441, T_{high} = +125°C for MC1541 or +75°C for MC1441. Pin numbers referenced in table denote flat package; to ascertain corresponding pin number for dual in-line package refer to the equivalent circuit.)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage	8	V_{th}				mV
(T_A = +25°C)			14	17	20	
($T_{low} \le T_A \le T_{high}$) MC1441			13	-	21	
MC1541			12	17	22	
Input Offset Voltage	8	V_{io}	-	1.0	6.0	mV
Input Bias Current	9	I_b				µA
($V_1 = V_2 = V_3 = V_4 = 0$)			-	5.0	25	
($V_1 = V_2 = V_3 = V_4 = 0$, $T_A = T_{low}$)			-	-	50	
Input Offset Current	9	I_{io}	-	1.0	2.0	µA
Output Voltage High ($V_1 = V_2 = V_3 = V_4 = 0$, I_{OH} = 200 µA)		V_{OH}	3.0	-	-	Vdc
Output Voltage Low	10	V_{OL}				mVdc
($V_1 = V_2 = V_3 = V_4 = 0$, V_{12} = +5.0 Vdc, I_7 = 10 mAdc)			-	-	350	
(V_{12} = +5.0 Vdc, I_7 = 10 mAdc, $T_A = +T_{high}$)			-	-	400	
Strobe Load Current (V_{10} = 0)		I_S	-	-	1.5	mAdc
Strobe Reverse Current		I_{SR}				µAdc
(V_{10} = +5.0 Vdc)			-	-	2.0	
(V_{10} = +5.0 Vdc, $T_A = T_{high}$)			-	-	25	
Input Gate Voltage Low ($V_1 = V_3$ = 25 mVdc, $V_2 = V_4 = 0$)	11	V_{GL}	-	0.7	-	Vdc
Input Gate Voltage High ($V_1 = V_3$ = 25 mVdc, $V_2 = V_4 = 0$)	11	V_{GH}	-	1.6	-	Vdc
Input Gate Load Current (V_8 or V_9 = 0)		I_G	-	-	2.5	mAdc
Input Gate Reverse Current (V_8 or V_9 = 5.0 Vdc)		I_{GR}				µAdc
(T_A = 25°C)			-	-	2.0	
($T_A = T_{high}$)			-	-	25	
Common Mode Range	13	V_{CM}				Vdc
Input Gate High			-	±1.5	-	
Input Gate Low			-	±1.5	-	
Differential Mode Range	14					
Input Gate High		V_{DH}	-	±600	-	mV
Input Gate Low		V_{DL}	-	±1.5	-	Vdc
Power Dissipation		P_D	-	140	180	mW

SWITCHING CHARACTERISTICS

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Propagation Delay						ns
Input to Amplifier Output (V_1 = 25 mV pulse, V_{10} = +2.0 Vdc)	8	t_{IA}	-	10	15	
Input to Output (V_1 = 25 mV pulse, V_{10} = +2.0 Vdc)	8	t_{IO}	-	20	30	
Strobe to Output ($V_1 = V_2 = V_3 = V_4 = 0$, V_{10} = +2.0 V pulse)	12	t_{SO}	-	15	20	
Gate Input to Amplifier Input (V_1 = 25 mV pulse, V_9 = 2.0 V pulse)	11	t_{GI}	-	10	15	
Gate Input to Amplifier Output (V_1 = 25 mVdc, V_9 = 2.0 V pulse)	11	t_{GA}	-	30	35	
Recovery Time						ns
Differential Mode	14	t_{DR}				
Input Gate High } V_1 or V_3 = 400 mV pulse			-	30	-	
Input Gate Low }			-	0	-	
Common Mode	13	t_{CMR}				
Input Gate High } V_1 or V_3 = 1.5 V pulse			-	15	30	
Input Gate Low }			-	15	30	

8

FIGURE 2 – TYPICAL INPUT THRESHOLD versus TEMPERATURE

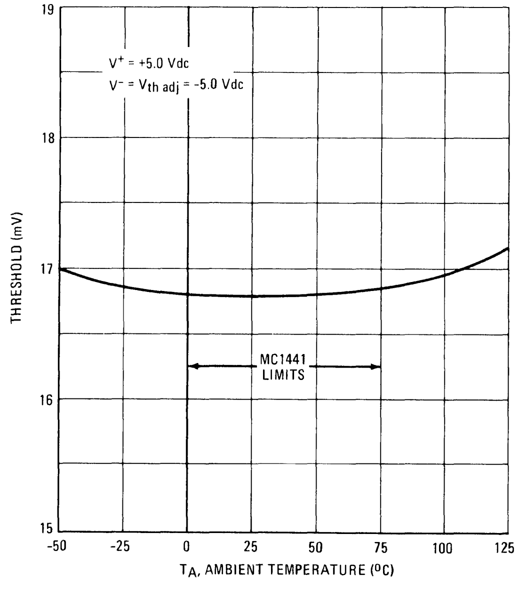


FIGURE 3 – TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST

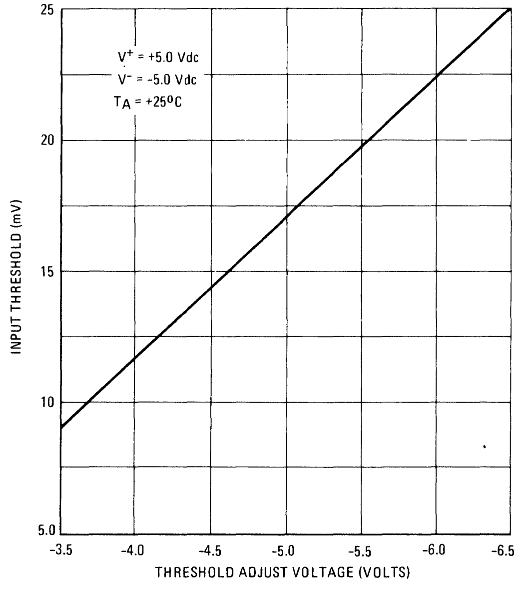


FIGURE 4 – TYPICAL INPUT THRESHOLD versus V-

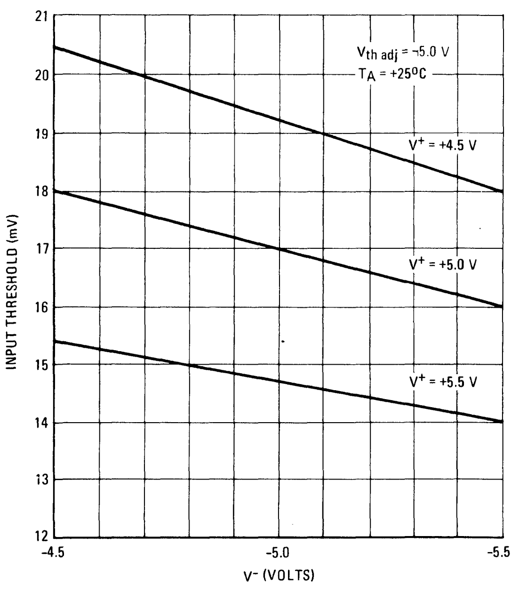


FIGURE 5 – TYPICAL INPUT THRESHOLD versus INPUT PULSE WIDTH

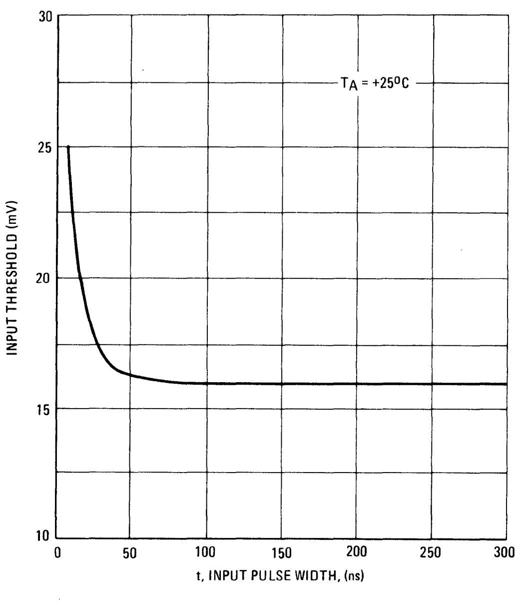


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FIGURE 6 – INPUT-OUTPUT TRANSFER CHARACTERISTICS

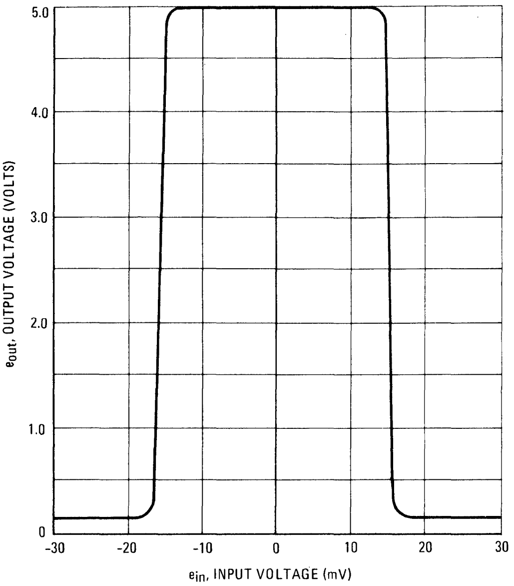


FIGURE 7 – CHANNEL GATE INPUT-AMPLIFIER OUTPUT TRANSFER CHARACTERISTICS

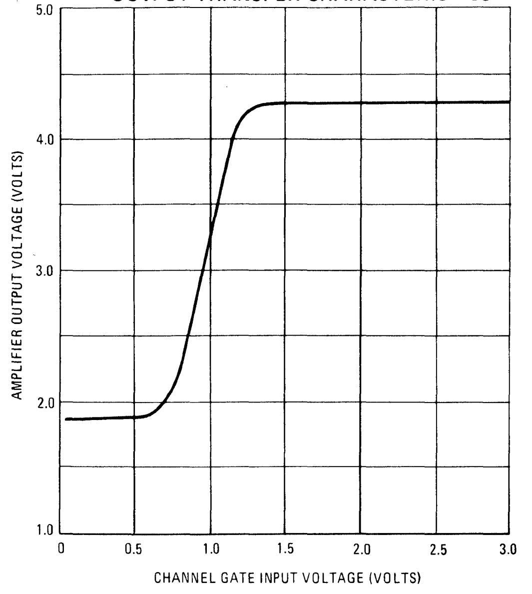
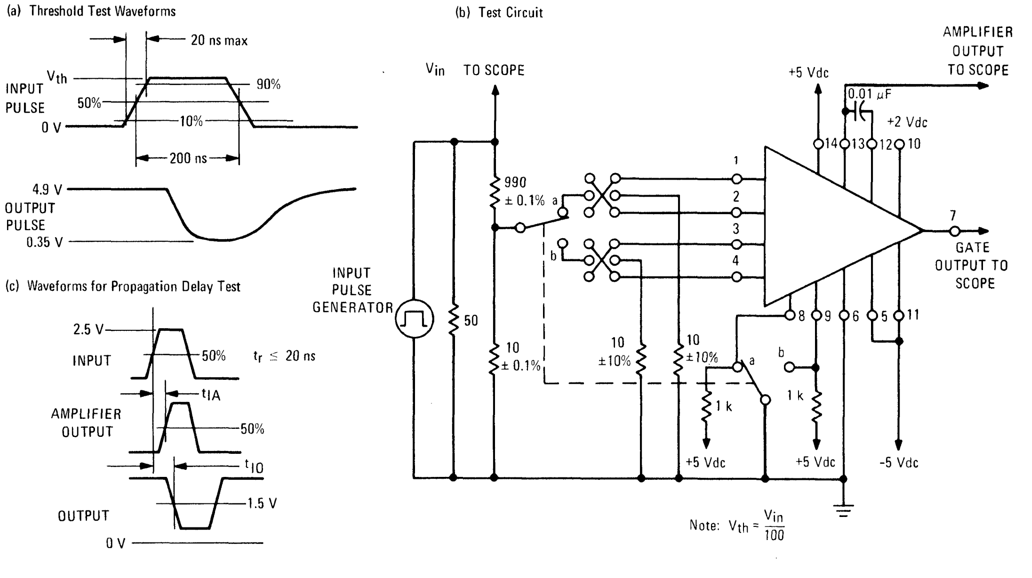
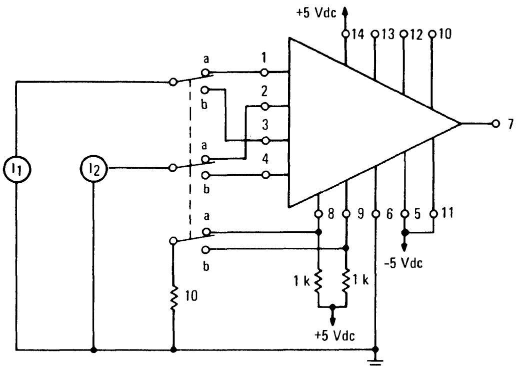


FIGURE 8 – INPUT THRESHOLD FOR OUTPUT VOLTAGE SWING FROM V_{OH} TO V_{OL} PROPAGATION DELAY FROM INPUT TO OUTPUT



Number at terminal end denotes the pin number for flat package only; to ascertain the corresponding pin number for the dual in line packages refer to the circuit schematic on the second page.

FIGURE 9 – INPUT BIAS CURRENT TEST CIRCUIT



$\frac{I_1 + I_2}{2} = I_b$ for "A" channel when switch is in "a" position

$= I_b$ for "B" channel when switch is in "b" position

$|I_1 - I_2| = I_{io}$

FIGURE 10 – OUTPUT VOLTAGE LEVELS

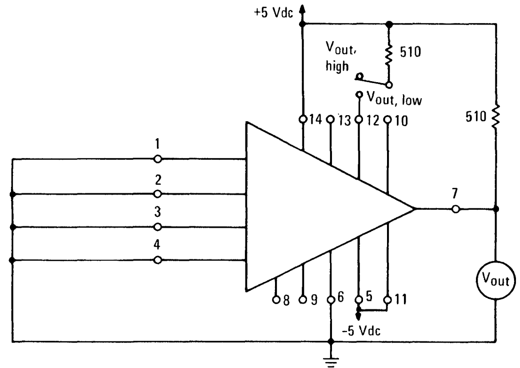
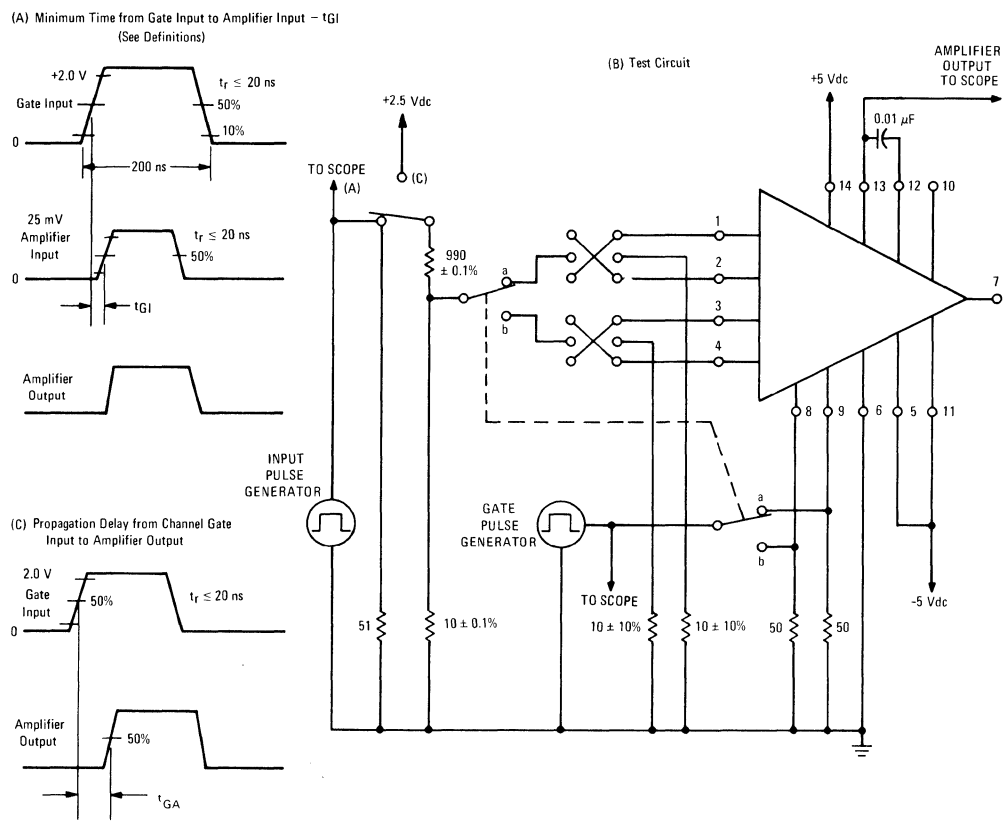


FIGURE 11 – MINIMUM TIME FROM CHANNEL GATE INPUT TO AMPLIFIER INPUT PROPAGATION DELAY FROM CHANNEL GATE INPUT TO AMPLIFIER OUTPUT



(Pin numbers shown on this page denote the pin numbers for the flat package only; to ascertain the corresponding pin numbers for the dual in-line package, refer to the circuit schematic on the second page.)

FIGURE 12 – PROPAGATION DELAY FROM STROBE INPUT TO OUTPUT

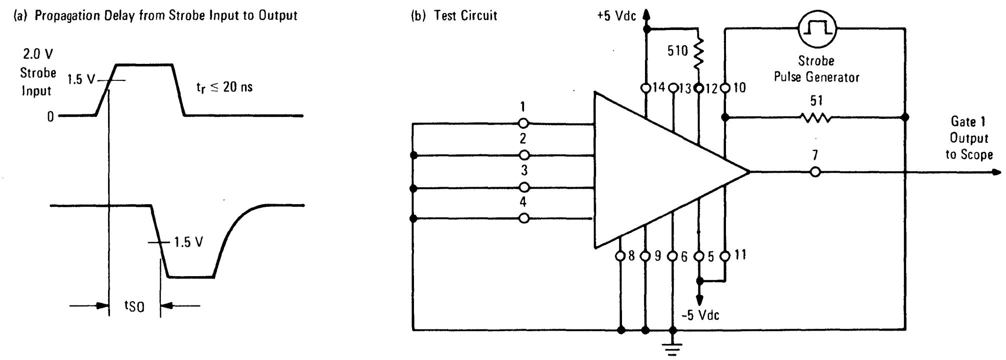


FIGURE 13 – COMMON-MODE RECOVERY AND COMMON-MODE RANGE

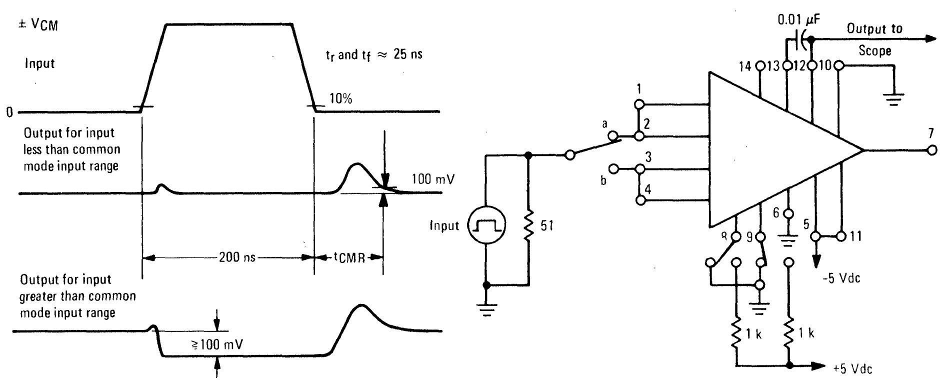
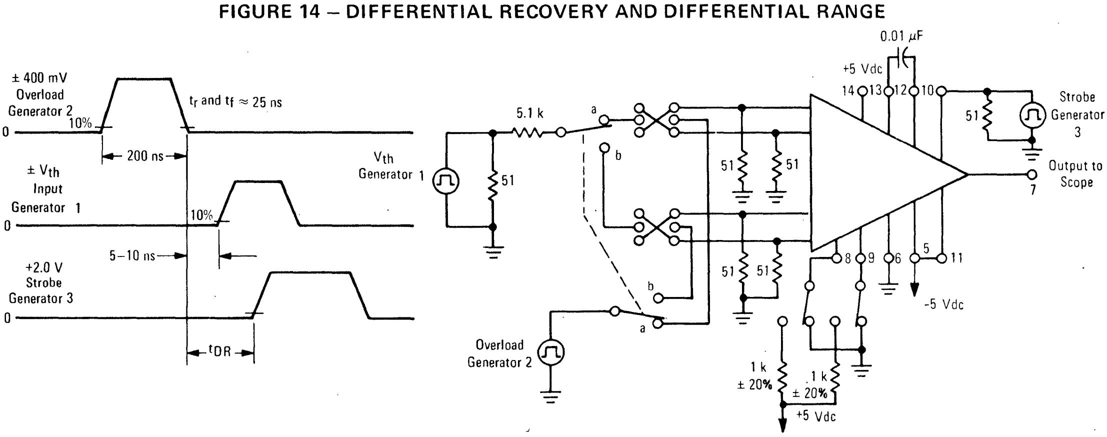


FIGURE 14 – DIFFERENTIAL RECOVERY AND DIFFERENTIAL RANGE



(Pin numbers shown on this page denote the pin numbers for the flat package only; to ascertain the corresponding pin numbers for the dual in-line package , refer to the circuit schematic on the second page.)

DEFINITIONS

Pin numbers referenced in the definitions below denote the flat package only; to ascertain the corresponding pin number for the dual in-line package refer to the circuit schematic.

I_B Input Bias Current – The average input current defined as $(I_1 + I_2 + I_3 + I_4)/4$.

I_G Channel Gate Load Current – The amount of current drain from the circuit when the channel gate input (Pin 8 or 9) is grounded.

I_{GR} Channel Gate Reverse Current – The leakage current when the channel gate input (Pin 8 or 9) is high.

I_{io} Input Offset Current – The difference between amplifier input current values $|I_1 - I_2|$ or $|I_3 - I_4|$.

I_S Strobe Load Current – The amount of current drain from the circuit when the strobe pin is grounded.

I_{SR} Strobe Reverse Current – The leakage current when the strobe input is high.

P_D Power Dissipation – The amount of power dissipated in the unit.

t_{CMR} Common Mode Recovery Time – The time required for the voltage at pin 12 to be within 100 mV of the dc value (after overshoot or ringing) as referenced to the 10% point of the trailing edge of a common mode overload signal.

t_{DR} Differential Recovery Time – The time required for the device to recover from the specified differential input prior to strobe enable as referenced to the 10% point of the trailing edge of an input pulse. The device is considered recovered when the threshold with the overload signal applied is within 1.0 mV of the threshold with no overload input.

t_{GI} Minimum Time Between Channel Gate Input and Signal Input – The minimum time between 50% point of channel gate input (Pin 8 or 9) and 50% point of signal input (Pins 1, 2, 3, or 4) that still allows a full width signal at amplifier output.

t_{GA} Propagation Delay, Channel Gate Input to Amplifier Output – The time required for the amplifier output at pin 13 to reach 50% of its final value as referenced to 50% of the input gate pulse at pin 8 or 9 (Amplifier input = 25 mVdc).

t_{IA} Propagation Delay, Input to Amplifier Output – The time required for the amplifier output pulse at pin 13 to achieve 50% of its final value referenced to 50% of the input pulse at pins 1 and 2 or 3 and 4.

t_{IO} Propagation Delay, Input to Output – The time required for the gate output pulse at pin 7 to reach the 1.5 Volt level as referenced to 50% of the input pulse at pins 1 and 2 or 3 or 4.

t_{SO} Strobe Propagation Delay to Output – The time required for the output pulse at pin 7 to reach the 1.5 Volt level as referenced to the 1.5 Volt level of the strobe input at pin 10.

V_{CM} Maximum Common Mode Input Range – The common mode input voltage which causes the output voltage level of the amplifier to decrease by 100 mV. (This is independent of the channel gate input level.)

V_{DH} Maximum Differential Input Range, Gate Input High – The differential input which causes the input stage to begin saturation.

V_{DL} Maximum Differential Input Range, Gate Input Low – The differential input signal which causes the output voltage level of the amplifier to decrease by 100 mV.

V_{GH} Channel Gate Input Voltage High – Gate pulse amplitude that allows the amplifier output pulse to just reach 100% of its final value. (Amplifier input is set at 25 mVdc).

V_{GL} Channel Gate Input Voltage Low – Gate pulse amplitude that allows the amplifier output to just reach a 100 mV level. (Amplifier input is set at 25 mVdc).

V_{io} Input Offset Voltage – The difference in V_{th} between inputs at pins 1 and 2 or 3 and 4.

V_{OH} Output Voltage High – The high-level output voltage when the output gate is turned off.

V_{OL} Output Voltage Low – The low-level output voltage when the output gate is saturated and the output sink current is 10 mA.

V_{th} Input Threshold – Input pulse amplitude at pins 1, 2, 3 or 4 that causes the output gate to just reach V_{OL}.

8

MC1543L

DUAL SENSE AMPLIFIER

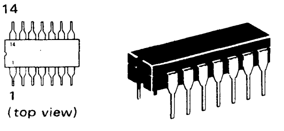
MONOLITHIC DUAL MECL CORE MEMORY SENSE AMPLIFIER

. . . a dual dc coupled sense amplifier providing output levels compatible with emitter-coupled logic levels. The MC1543L offers adjustable threshold and excellent threshold stability over a wide range of power-supply voltage variation.

- Input Threshold – Adjustable from 10 to 40 mV (Positive or Negative Signals)
- Both OR and NOR Outputs Available
- Low Power Dissipation
- Threshold Insensitive V_{CC} or V_{EE} Voltage Variation
- Each Amplifier is Separately Strobed

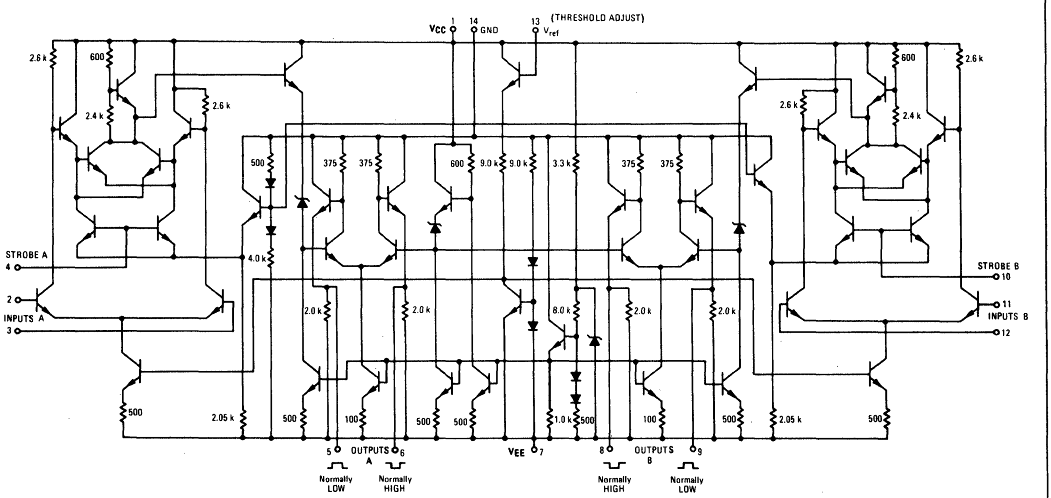
DUAL MECL CORE MEMORY SENSE AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 632
TO-116

CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+10 -10	Vdc Vdc
Differential Input Voltage	V_{ID}	±5.0	Vdc
Common-Mode Input Voltage	V_{ICM}	±5.0	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Ceramic Dual-In-Line Package Derate above T_A = +25°C	P_D	 1000 6.7	 mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Each Amplifier) (V_{CC} = +5.0 Vdc ±5%, V_{EE} = -5.2 Vdc ±5%, V_{ref} = 0.54 V ±1%, T_A = +25°C unless otherwise noted.)

Characteristic	Fig.No.	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage	8	V_{TH}	17	20	23	mV
Power Supply Currents ($V_2 = V_3 = V_{11} = V_{12} = V_{14} = 0$)	6 6	I_{CC} I_{EE}	– –	9.5 26.5	12 33	mAdc mAdc
Input Bias Current	7	I_{IB}	–	3.5	10	µAdc
Input Offset Current	7	I_{IO}	–	0.05	0.5	µAdc
Output Voltage High	9	V_{OH}	-0.85	-0.8	-0.67	Vdc
Output Voltage Low	9	V_{OL}	–	-1.7	-1.46	Vdc
Strobe Threshold Level	10	V_{ST}	–	-1.30	–	Vdc
Strobe Input Current High	10	I_{SH}	–	25	50	µAdc
Strobe Input Current Low	10	I_{SL}	–	0.01	0.1	µAdc
Input Common Mode Range	14	V_{CMR}	3.0	4.0	–	Vdc
Input Threshold Range (by varying V_{ref})	8	V_{THR}	–	10-40	–	mV
Power Dissipation	6	P_D	–	185	230	mW
Reference Supply Input Current (Pin 13)	6	I_{ref}	–	10	40	µA

SWITCHING CHARACTERISTICS

Characteristic	Fig.No.	Symbol	Min	Typ	Max	Unit
Propagation Delay (Input to Output)	1	t_{IO}	–	28	35	ns
Propagation Delay (Strobe to Output)	12	t_{SO}	–	16	20	ns
Strobe Release Time	12	t_{SR}	–	18	30	ns
Recovery Time (Differential-Mode) (e_{in} = 400 mVdc)	13	t_{DR}	–	10	15	ns
Recovery Time (Common-Mode) (e_{in} = 3.0 Vdc)	14	t_{CMR}	–	3.0	15	ns
Strobe Width Minimum	12	t_S	–	8.0	–	ns

TEMPERATURE TESTS (-55°C to +125°C)

Characteristic	Fig.No.	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage T_A = -55°C T_A = +125°C	8	V_{TH}	 18 15	 21.5 18.5	 25 22	mV
Input Bias Current	7	I_{IB}	2.2	7.0	20	µAdc
Input Offset Current	7	I_{IO}	0.02	0.1	1.0	µAdc

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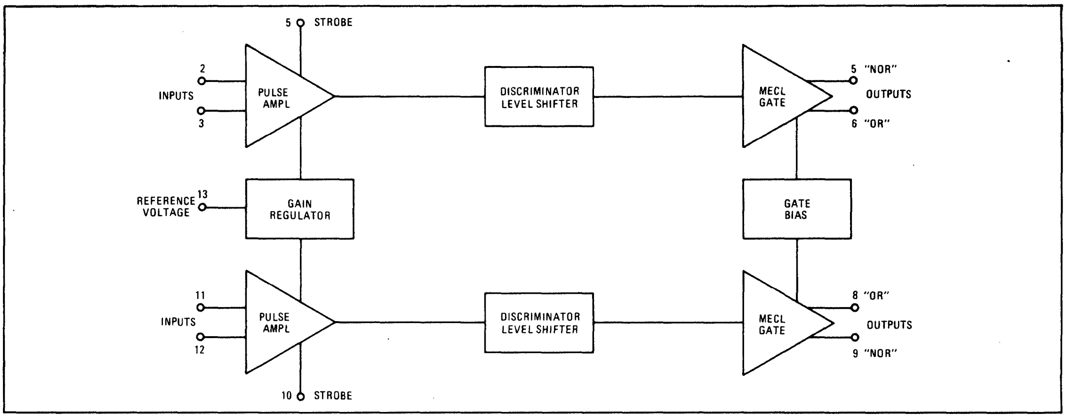
EQUIVALENT CIRCUIT



TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 Vdc, V_{EE} = -5.2 Vdc, V_{ref} set for 20 mV Threshold, T_A = +25°C unless otherwise noted.)

FIGURE 1 – TYPICAL INPUT THRESHOLD versus TEMPERATURE

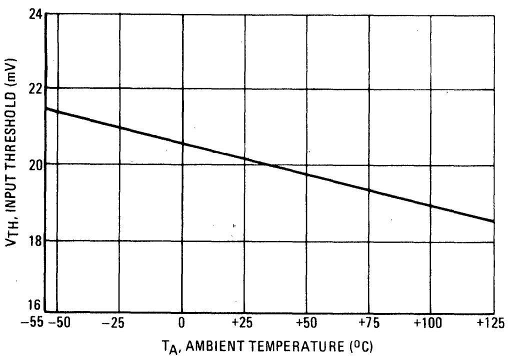


FIGURE 2 – TYPICAL INPUT THRESHOLD versus REFERENCE VOLTAGE

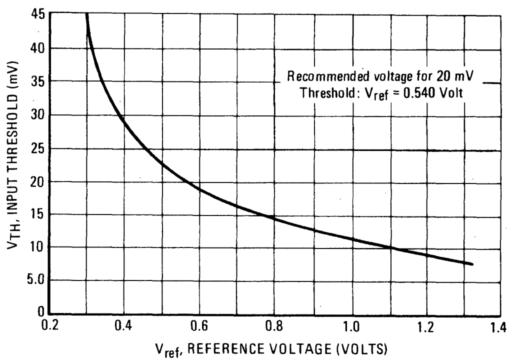


FIGURE 3A – TYPICAL INPUT THRESHOLD versus V_{CC}

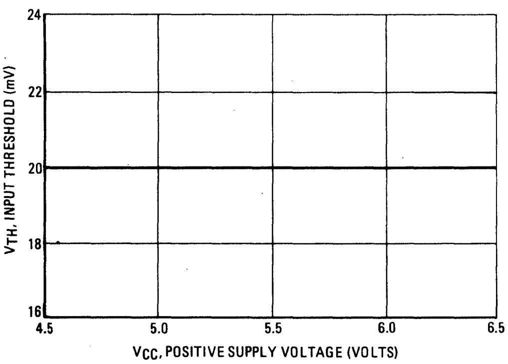
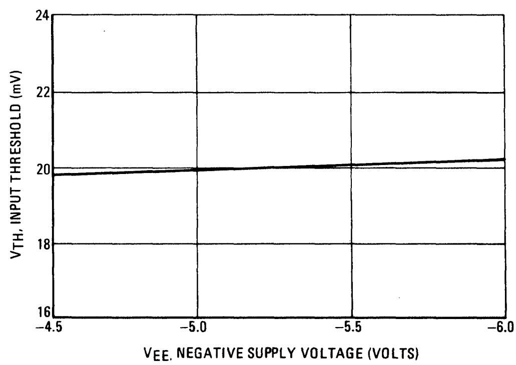


FIGURE 3B – TYPICAL INPUT THRESHOLD versus V_{EE}



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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 Vdc, V_{EE} = -5.2 Vdc, V_{ref} set for 20 mV Threshold, T_A = +25°C unless otherwise noted.)

FIGURE 4 – TYPICAL INPUT THRESHOLD versus INPUT PULSE WIDTH

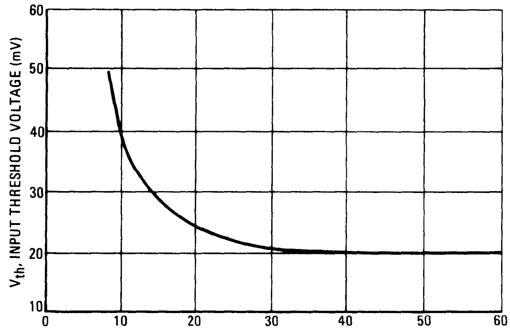
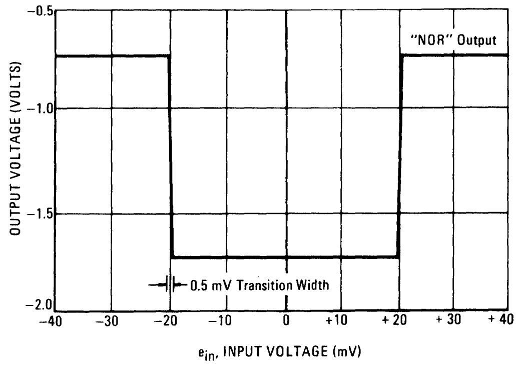


FIGURE 5 – INPUT-OUTPUT TRANSFER CHARACTERISTICS (one output)



TEST CIRCUITS

(V_{CC} = +5.0 Vdc, V_{EE} = -5.2 Vdc, V_{ref} = 0.54 V, T_A = +25°C unless otherwise noted.)

FIGURE 6 – POWER SUPPLY CURRENT DRAIN

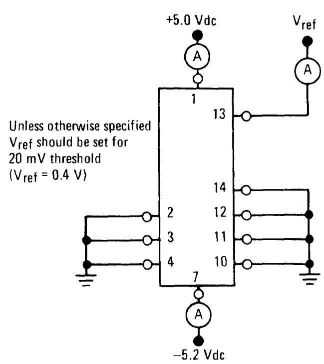


FIGURE 7 – INPUT BIAS CURRENT INPUT OFFSET CURRENT

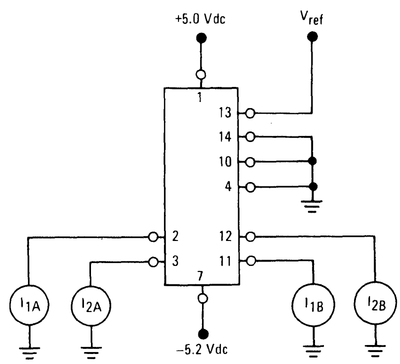


FIGURE 8 – INPUT THRESHOLD LEVEL

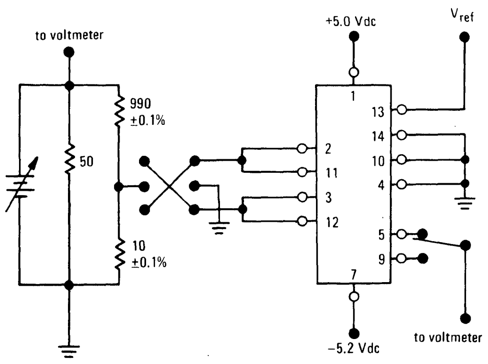
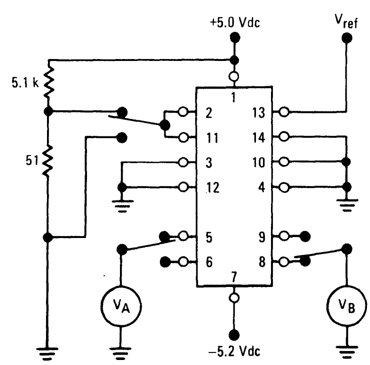


FIGURE 9 – OUTPUT VOLTAGE LEVELS



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TEST CIRCUITS (continued)

FIGURE 10 – STROBE THRESHOLD LEVEL STROBE INPUT CURRENTS

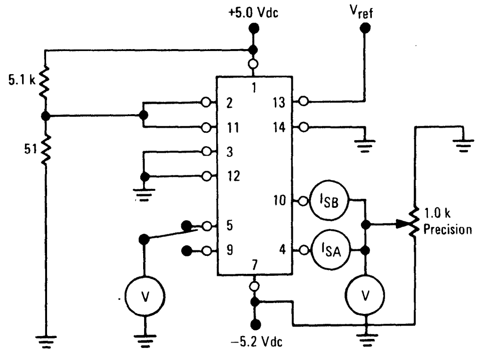


FIGURE 11 – PROPAGATION DELAY – INPUT TO OUTPUT

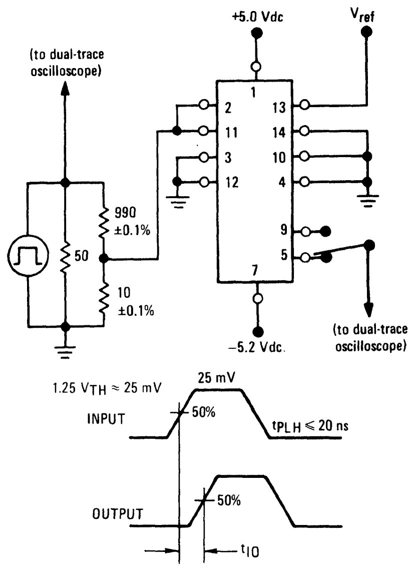


FIGURE 12 – PROPAGATION DELAY – STROBE TO OUTPUT and STROBE RELEASE TIME

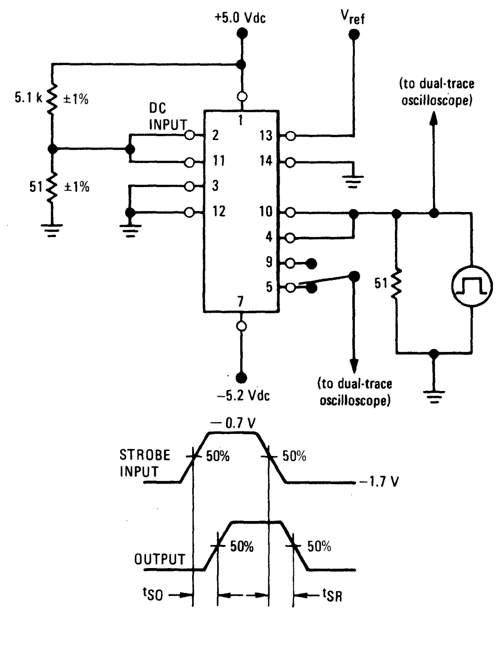
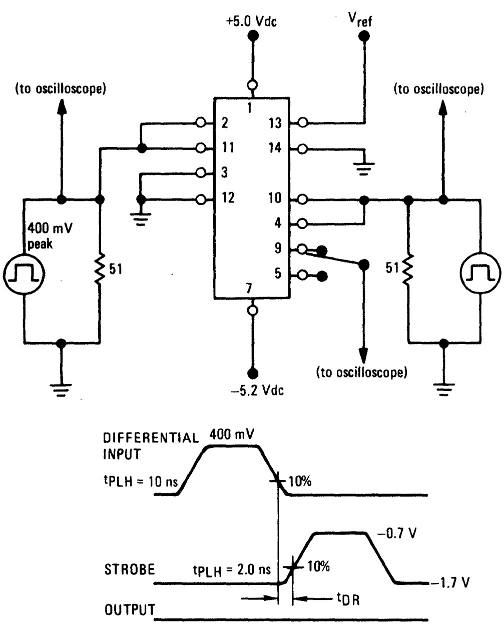


FIGURE 13 – DIFFERENTIAL MODE RECOVERY TIME
(See definition section)



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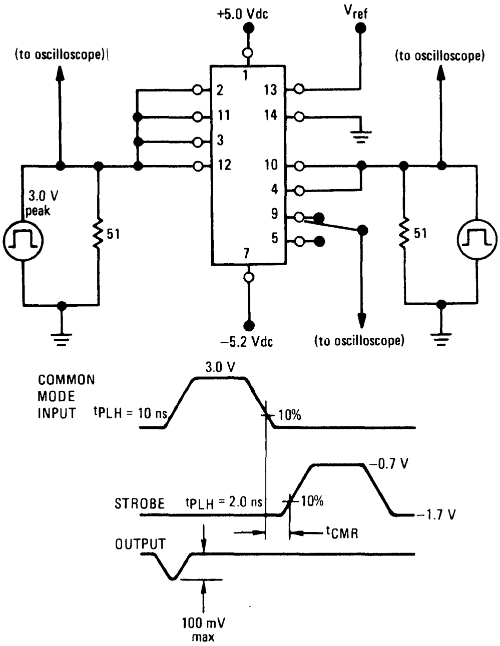
TEST CIRCUITS (continued)

FIGURE 14 – COMMON MODE RECOVERY TIME
COMMON MODE INPUT RANGE
(See definition section)



DEFINITIONS

I_{IO} Input Offset Current – The difference between amplifier input current values $|I_{1A} - I_{2A}|$ or $|I_{1B} - I_{2B}|$.

I_{SH} Strobe High Current – The amount of input current when the strobe pin is grounded.

I_{SL} Strobe Low Current – The leakage current when the strobe input is tied to the negative supply.

P_D Power Dissipation – The amount of power dissipated in the unit.

t_{CMR} Common-Mode Recovery Time – The minimum time by which the strobe input may follow the high level common mode input signal without causing a signal to appear at the amplifier output.

t_{DR} Differential-Mode Recovery Time – Differential recovery time, the minimum time by which the strobe input may follow the high level differential input signal without causing a signal to appear at the amplifier output.

t_{IO} Propagation Delay, Amplifier Input to Amplifier Output – The time required for the amplifier output to reach 50% of its final value as referenced to 50% of the level of the pulse input.(Amplifier input = 25% over set threshold or approximately 25 mVdc.)

t_S Strobe Width – The amount of time the strobe must be high to obtain a given output. Minimum strobe width is that minimum time required to cause the output to complete a full swing V_{OL} to V_{OH} or V_{OH} to V_{OL}.

t_{SO} Propagation Delay, Strobe Input to Amplifier Output – The time required for the amplifier output pulse to achieve 50% of its final value referenced to 50% of the strobe input pulse at pins 4 or 10.

t_{SR} Strobe Release Time – The time required for the output to change to 50% of its swing after the strobe reaches 50% of its level going low. A dc level of 50 mV is the input signal.

V_{CMR} Maximum Common-Mode Input Range – The common-mode input voltage which causes the output voltage level of the amplifier to change by 100 mV (strobe high).

V_{OH} Output Voltage High – The high-level output voltage at pins 6 and 8 with no input – or at pins 5 and 9 with input above threshold.

V_{OL} Output Voltage Low – The low-level output voltage at pins 5 and 9 with no input – or at pins 6 and 8 with input above threshold.

V_{ST} Strobe Threshold Level – The voltage at which the strobe turns the amplifier to the ON state.

V_{TH} Input Threshold – Input pulse amplitude at pins 2, 3, 11, or 12 that causes the output gate to just reach its new value, V_{OL} or V_{OH}.

V_{THR} Input Threshold Range – The maximum spread of input threshold level that can be attained by varying the threshold voltage reference, V_{ref}.

MC1544L
MC1444L

SENSE AMPLIFIERS

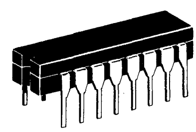
IDEAL FOR PLATED-WIRE, THIN-FILM AND OTHER HIGH-SPEED LOW-LEVEL SENSING APPLICATIONS

MC1544L/MC1444L features four input channels with decoded selection, two stages of gain employing capacitive coupling, and a MTTL compatible output gate. AC coupling reduces access times by eliminating the problems usually associated with input line offset voltages.

- Threshold Level — 1.0 mV typ
- Propagation Delay Time — 18 ns typ
- Decoded Input Channel Selection
- MTTL Compatible Inputs and Outputs
- Wired OR Output Capability
- DC Level Restore Gate on Capacitors Eliminates Repetition Rate Problems Common to ac-Coupled Circuits
- Output Strobe Capability

AC-COUPLED FOUR-CHANNEL SENSE AMPLIFIER

MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 620

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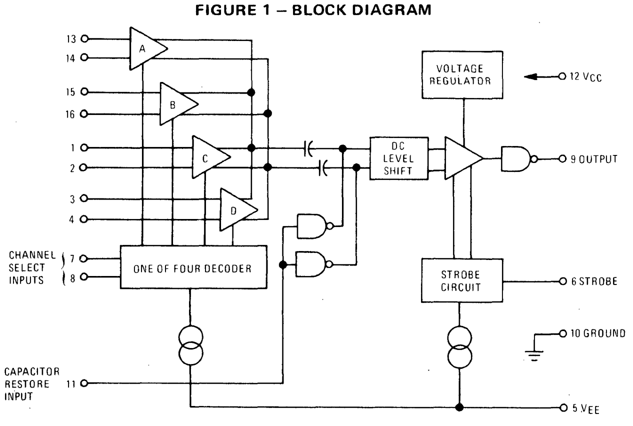
FIGURE 1 — BLOCK DIAGRAM



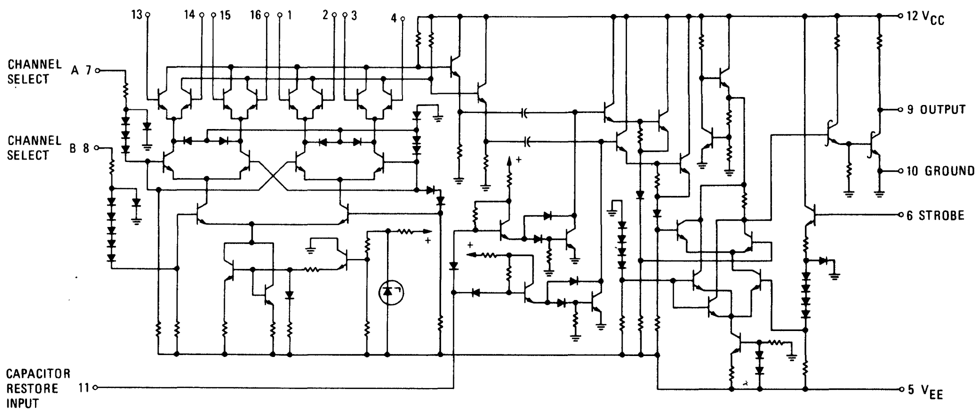
TRUTH TABLE		
PIN 7	PIN 8	CHANNEL SELECTED
HI	HI	A
LO	HI	B
HI	LO	C
LO	LO	D

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Power Supply Voltage	V_{CC} V_{EE}	+7.0 −8.0	Vdc
Common-Mode Input Voltage	$V_{CM}+$ $V_{CM}-$	+5.0 −6.0	Vdc
Differential-Mode Input Voltage	$V_{DM}+$ $V_{DM}-$	+5.0 −6.0	Vdc
Capacitor Restore, Channel Select, and Strobe Input Voltage	V_{CR}, V_{CS}, V_S	+5.5	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	1.0 6.7	W mW/°C
Operating Temperature Range MC1544L MC1444L	T_A	−55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+175	°C

FIGURE 2 – CIRCUIT SCHEMATIC



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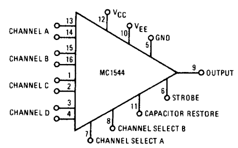

ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

TEST CURRENT/VOLTAGE VALUES														
μA		mA		VOLTS										
I_{CM^+}	I_{CM^-}	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IL2}	V_{IH2}	V_{CCL}	V_{CC}	V_{CCH}	V_{EEL}	V_{EE}	V_{EEH}	
200	−10	10	−0.4	0.8	2.0	0	3.5	4.75	5.0	5.25	−5.7	−6.0	−6.3	

CHARACTERISTIC		Symbol	Pin Under Test	Min	Typ	Max	Unit	I_1	I_2	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IL2}	V_{IH2}	V_{CCL}	V_{CC}	V_{CCH}	V_{EEL}	V_{EE}	V_{EEH}	GND
								TEST CURRENT/VOLTAGES APPLIED TO PINS LISTED BELOW:														
Input Threshold Voltage (Note 1)	MC1544L	V_{TH}	13	0.5	1.0	1.5	mV	–	–	–	–	–	–	–	–	–	12	–	–	5	–	10
T_{low}* to T_{high}*	MC1444L		13	0.3	1.0	2.3	mV	–	–	–	–	–	–	–	–	–	12	–	–	5	–	10
Input Bias Current (Note 1)		I_b	13	–	20	–	μA	–	–	–	–	–	–	13, 14	7, 8	–	–	12	–	–	5	10
Input Offset Current		I_{io}	13, 14	–	1.0	–	μA	–	–	–	–	–	–	13, 14	7, 8	–	–	12	–	–	5	10
Channel Select Input Current (Note 2)	High Level	I_{CSH}	7	–	1.8	3.0	mA	–	–	–	–	–	–	–	7	–	–	12	–	–	5	10
	Low Level	I_{CSL}	7	–	0.6	1.0	mA	–	–	–	–	–	–	7	–	–	–	12	–	–	5	10
Capacitor Restore Input Current	High Level	I_{CRH}	11	–	0	10	μA	–	–	–	–	–	–	–	11	–	–	12	–	–	5	10
	Low Level	I_{CRL}	11	–	−2.5	−3.5	mA	–	–	–	–	–	–	11	–	–	–	12	–	–	5	10
Strobe Input Current	Low/High Level	I_S	6	–	40	200	μA	–	–	–	–	–	–	–	6	–	–	12	–	–	5	10
Channel Select Input Voltage (Note 3)	High Level	V_{CSH}	7	–	1.6	2.1	V	–	–	–	–	–	7	3, 8 13, 15	–	–	12	–	–	5	–	10
	Low Level	V_{CSL}	7	0.7	1.2	–	V	–	–	–	–	7	–	1, 8 13, 15	–	–	12	–	–	5	–	10
Channel Select Input Voltage (Note 3)	High Level	V_{CSH}	8	–	1.5	2.1	V	–	–	–	–	–	8	1, 3 7, 13	–	–	12	–	–	5	–	10
	Low Level	V_{CSL}	8	0.7	1.0	–	V	–	–	–	–	8	–	1, 7 13, 15	–	–	12	–	–	5	–	10
Capacitor Restore Input Voltage (Note 4)	High Level	V_{CRH}	11	–	1.5	2.0	V	–	–	–	–	–	11	–	6	–	12	–	–	5	–	10
	Low Level	V_{CRL}	11	0.8	1.5	–	V	–	–	–	–	11	–	–	6	–	12	–	–	5	–	10
Strobe Input Voltage (Note 4)	High Level	V_{SH}	6	–	1.5	2.0	V	–	–	–	–	–	6	11	–	–	12	–	–	5	–	10
	Low Level	V_{SL}	6	0.8	1.5	–	V	–	–	–	–	6	–	11	–	–	12	–	–	5	–	10
Output Voltage	High Level	V_{OH}	9	2.4	3.6	–	V	–	–	–	9	6	–	–	–	12	–	–	5	–	–	10
	Low Level	V_{OL}	9	–	0.4	0.5	V	–	–	9	–	–	–	–	–	12	–	–	–	–	–	10
Power Supply Currents	Positive	I_{CC}	12	15	22	30	mA	–	–	–	–	–	–	6, 13, 14	7, 8, 11	–	–	12	–	–	5	10
	Negative	I_{EE}	5	15	20	30	mA	–	–	–	–	–	–	6, 13, 14	7, 8, 11	–	–	12	–	–	5	10
Common-Mode Range Voltage (Note 1)		V_{CM^+}	13, 14	–	4.7	–	Vdc	13, 14	–	–	–	–	–	–	7, 8	–	12	–	–	5	–	10
		V_{CM^-}	13, 14	–	−6.0	–	Vdc	13, 14	–	–	–	–	–	–	7, 8	–	12	–	–	5	–	10
Differential-Mode Range Voltage		V_{DM}	13	–	3.7	–	Vdc	13	–	–	–	–	–	14	7, 8	–	12	–	–	5	–	10

*MC1544 T_{low} = −55°C, T_{high} = +125°C; MC1444 T_{low} = 0°C, T_{high} = +75°C.

NOTES:
1. Only one input test is shown, other inputs are tested in the same manner and are selected according to the truth table in Figure 1.
2. Pin 8 is tested in the same manner.
3. This requirement is considered satisfied if the input bias currents of all unselected channels total less than 1.0 μA which guarantees that these channels are "off."
4. This requirement is evaluated during the ac threshold test (Figures 1, 2): A 10 mV signal (e_{in_1}) is applied to the input, V_{CRH} will result in V_{OH} at the output while V_{CRL} will allow normal operation.
5. This requirement is evaluated as in Note 4 except V_{SH} allows normal operation and V_{SL} causes V_{OH} at the output.

SWITCHING CHARACTERISTICS (T_A = +25°C unless otherwise noted)

Characteristic		Symbol	Figure	Min	Typ	Max	Unit
Propagation Delay Time		t_{pd-}	1, 5	–	18	25	ns
		t_{pd+}		–	40	–	
Strobe to Input Lead Time		t_{si}	1, 5	–	10	–	ns
Strobe to Output Delay Time		t_{so-}	1, 6	–	18	25	ns
		t_{so+}		–	30	–	
Channel Select to Input Lead Time		t_{csi}	1, 5	–	15	–	ns
Channel Select to Output Delay Time		t_{cso-}	1, 7	–	25	–	ns
		t_{cso+}		–	40	–	
Capacitor Restore to Input Lead Time		t_{cri}	1, 5	–	10	–	ns
Capacitor Restore Time (50 mV Offset)		t_{cr}	1, 8	–	15	–	ns
Common-Mode Recovery Time	e_{in_1} = +2.0V	t_{CMR+}	19	–	50	–	ns
	e_{in_1} = −2.0V	t_{CRM-}		–	50	–	
Differential-Mode Recovery Time	e_{in_1} = +1.0V	t_{DMR+}	20	–	65	–	ns
	e_{in_1} = −1.0V	t_{DMR-}		–	65	–	

8

FIGURE 3 – AC TEST CIRCUIT

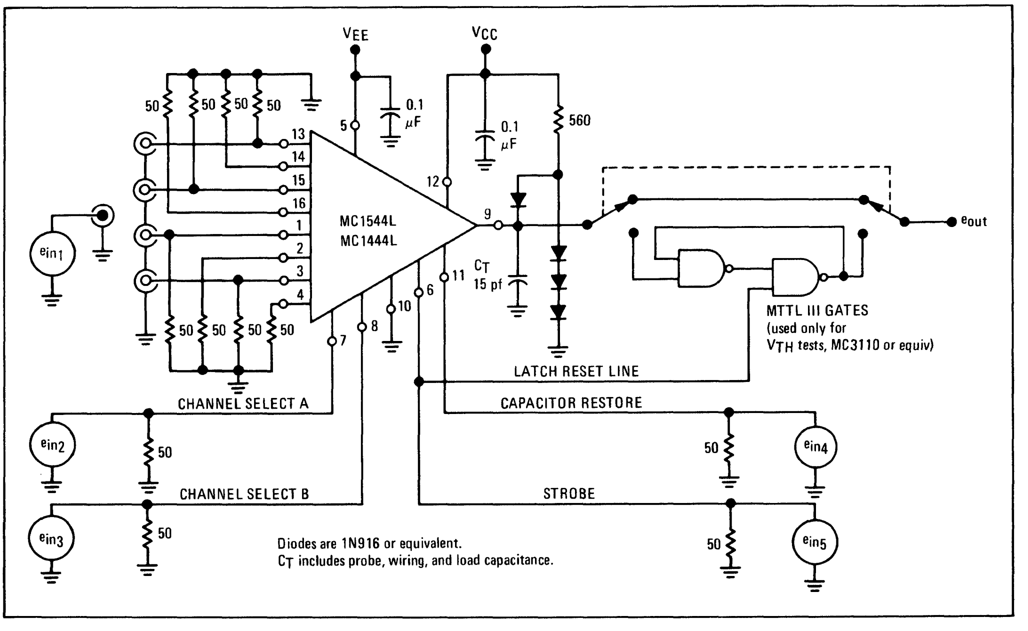

FIGURE 4 – THRESHOLD VOLTAGE TEST

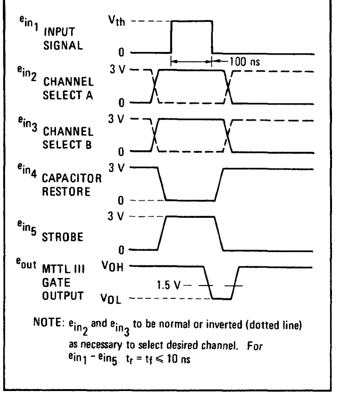

FIGURE 5 – t_{csi}, t_{cri}, t_{si}, t_{pd-}, t_{pd+}

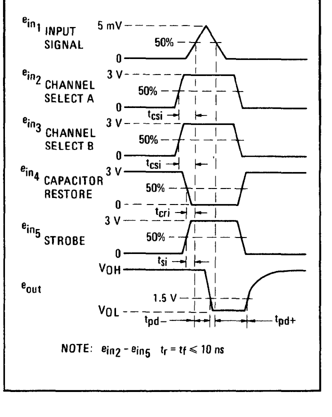

FIGURE 6 – t_{so-}, t_{so+}

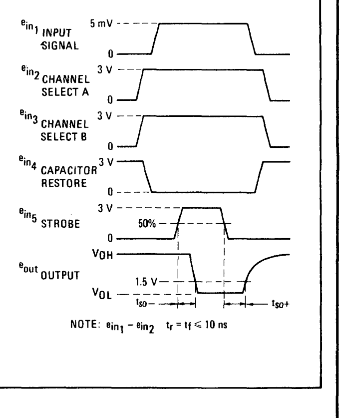

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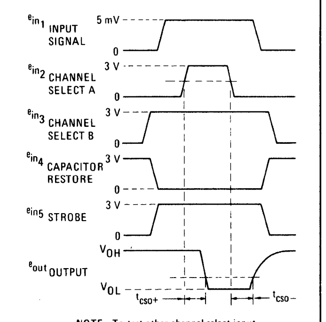
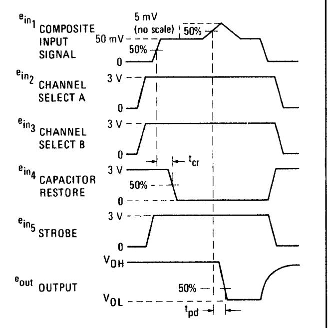
FIGURE 7 – t_{cso+}, t_{cso-}



NOTE: To test other channel select input, reverse e_{in_2} and e_{in_3}.
e_{in_1} – e_{in_5} $t_r = t_f \leq 10$ ns

FIGURE 8 – t_{cr}



NOTE: e_{in_1} – e_{in_5} $t_r = t_f \leq 10$ ns

DEFINITIONS

I_b	Input current to the base of any input transistor when the base of the other transistor of the differential pair is at the same voltage
I_{CC}	Positive power supply current
I_{CRH}	The current into the channel select input when the input is at a high-level of 3.5 volts
I_{CRL}	The current out of the capacitor restore input when the input is at a low-level of 0 volts
I_{CSH}	The input current to a channel select input when that input is at a high-level of 3.5 volts
I_{CSL}	The current into a channel select input when the input is at a low-level of 0 volts
I_{EE}	Negative power supply current
I_{io}	The difference between the base currents of any input differential pair of transistors when the base voltages are equal
I_{OH}	Output logic "1" state source current
I_{OL}	Output logic "0" state sink current
I_{SH}	The current into the strobe input when the input is at a high-level of 3.5 volts
I_{SL}	The current into the strobe input when the input is at a low-level of 0 volts
$t_{CMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or – 2 volt common-mode signal ($t_r = t_f \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 21
t_{cr}	The minimum time between the 50% level of the leading edge of a 50 mV input offset signal and the 50% level of the leading edge of the capacitor restore pulse as shown in Figure 8
t_{cri}	The minimum time between the 50% level of the leading edge of the capacitor restore signal and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 5
t_{csi}	The minimum time between the 50% level of the leading edge of the channel select and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 5
t_{cso+}	The delay time from the 50% level of the trailing edge of the channel select signal to the 1.5 volt level of the positive edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 7
t_{cso-}	The delay time from the 50% level of the leading edge of the channel select signal to the 1.5 volt level of the negative edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 7
$t_{DMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or – 1 volt differential-mode signal ($t_r = t_f \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 22
t_{pd+}	The delay time from the 50% level of the trailing edge of a 5 mV input signal to the 1.5 volt level of the positive edge of the output as shown in Figure 5
t_{pd-}	The delay time from the 50% level of the leading edge of a 5 mV input signal to the 1.5 volt level of the negative edge of the output as shown in Figure 5
t_{si}	The minimum time between the 50% level of the leading edge of the strobe and the 50% level of the leading edge of the input signal as shown in Figure 5
t_{so+}	The delay time from the 50% level of the trailing edge of the strobe to the 1.5 volt level of the positive edge of the output when the input is held at the "1" level as shown in Figure 6
t_{so-}	The delay time from the 50% level of the leading edge of the strobe to the 1.5 volt level of the negative edge of the output when the input is held at the "1" level as shown in Figure 6
V_{CC}	Positive power supply voltage
V_{CCH}	Maximum operating positive power supply voltage
V_{CCL}	Minimum operating positive power supply voltage
V_{CM+}	The maximum common-mode input voltage that will not saturate the amplifier
V_{CM-}	The minimum common-mode input voltage that will not break down the amplifier
V_{CRH}	The minimum high-level voltage at the capacitor restore input required to insure that the capacitors are clamped i.e., the input threshold voltage is greater than 10 mV
V_{CRL}	The maximum low-level voltage at the capacitor restore input which will allow normal operation during the threshold test
V_{CSH}	The minimum high-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
V_{CSL}	The maximum low-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
V_{DM}	The maximum differential-mode input voltage that will not saturate the amplifier
V_{EE}	Negative power supply voltage
V_{EEH}	Maximum operating negative power supply voltage
V_{EEL}	Minimum operating negative power supply voltage
V_{OH}	Logic "1" state output voltage
V_{OL}	Logic "0" state output voltage
V_{SH}	The minimum high-level voltage at the strobe input which will allow normal operation during the threshold test
V_{SL}	The maximum low-level voltage at the strobe input which will result in V_{OH} at the output regardless of input signals
V_{th}	The minimum input signal ($e_{in\,1}$) required to drive the MTTL III gates to obtain the e_o waveform shown in Figure 4

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TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 9 – THRESHOLD VOLTAGE versus TEMPERATURE

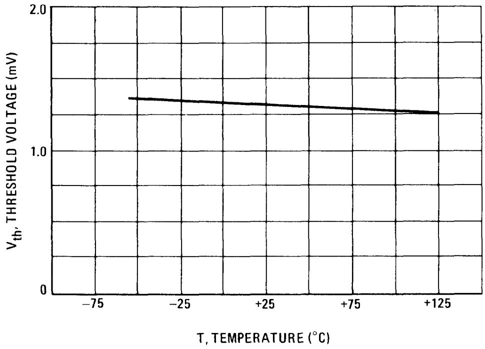


FIGURE 10 – THRESHOLD VOLTAGE versus POWER SUPPLIES

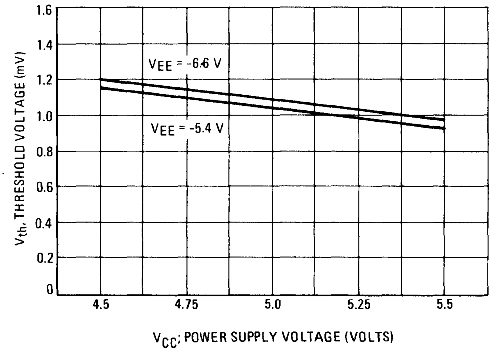


FIGURE 11 – THRESHOLD versus INPUT OFFSET VOLTAGE

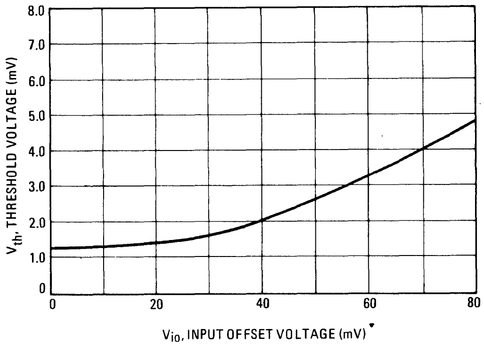


FIGURE 12 – THRESHOLD VOLTAGE versus PULSE WIDTH

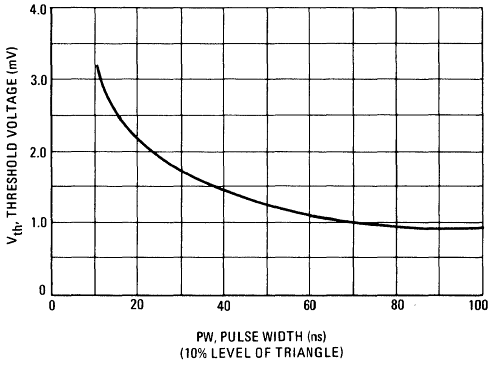


FIGURE 13 – OUTPUT VOLTAGE versus CURRENT and TEMPERATURE

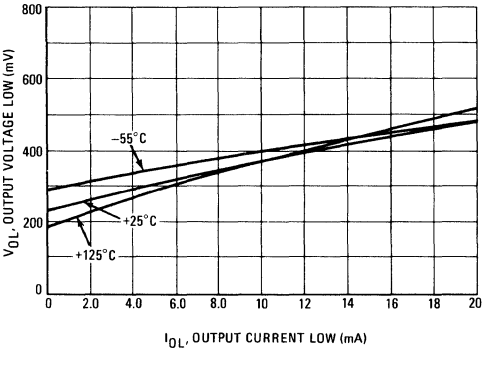
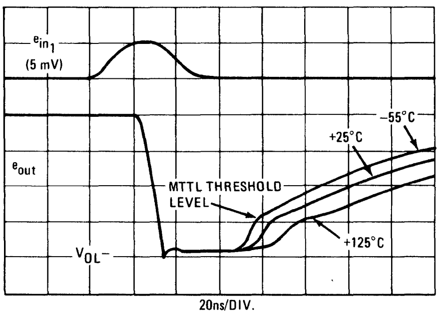


FIGURE 14 – SENSE AMPLIFIER RESPONSE versus TEMPERATURE (See Figures 3 and 5)



8

TYPICAL CHARACTERISTICS (continued)

FIGURE 15 – INPUT IMPEDANCE versus FREQUENCY

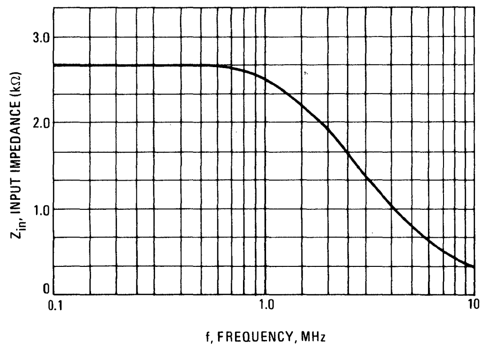


FIGURE 16 – CAPACITOR RESTORE TIME versus INPUT OFFSET VOLTAGE

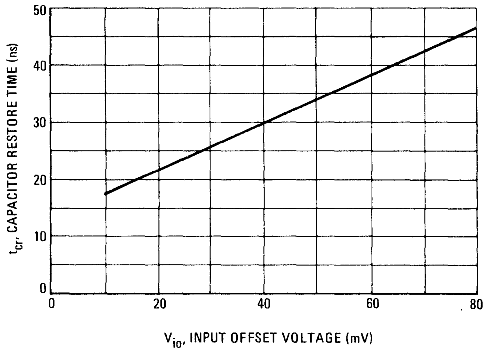


FIGURE 17 – AMPLIFIER INPUT TO OUTPUT TRANSFER CHARACTERISTIC

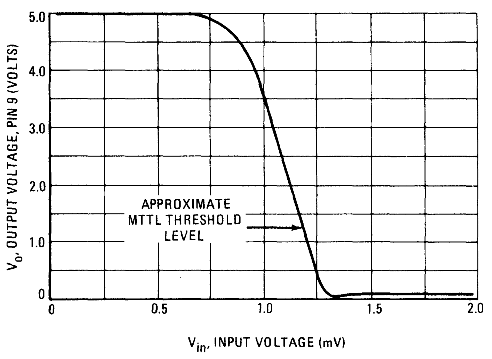


FIGURE 18 – STROBE TO OUTPUT TRANSFER CHARACTERISTICS

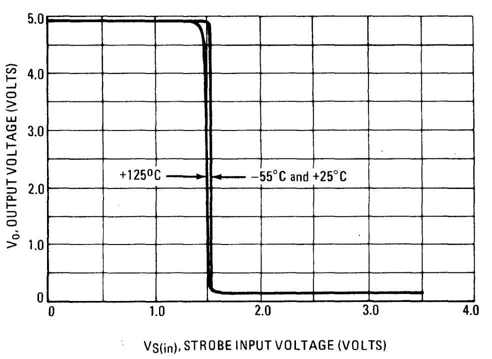


FIGURE 19 – CHANNEL SELECT A to OUTPUT TRANSFER CHARACTERISTICS

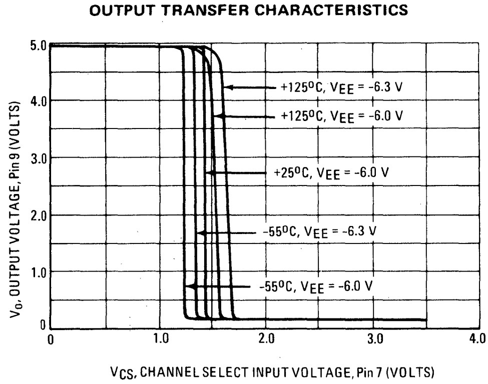


FIGURE 20 – CHANNEL SELECT B to OUTPUT TRANSFER CHARACTERISTICS

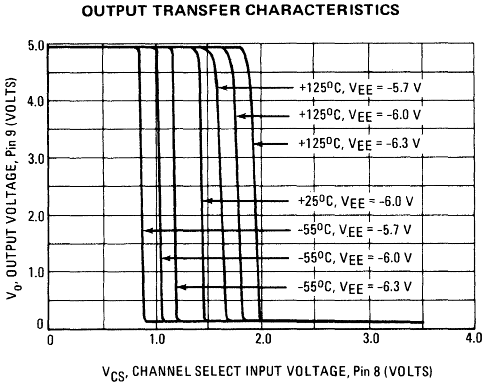
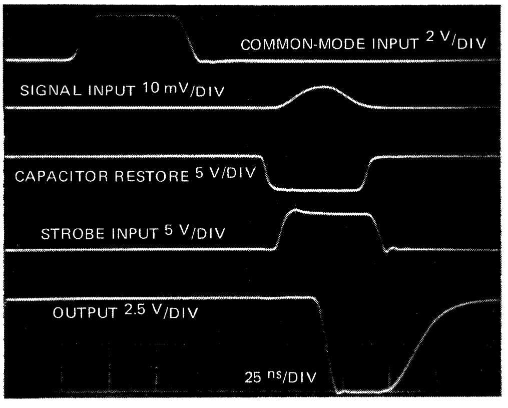


FIGURE 21 – COMMON-MODE CHARACTERISTICS

Note: The 5mV Input Signal (Differential) is superimposed on the Common-Mode Input and is shown separately for reference only.



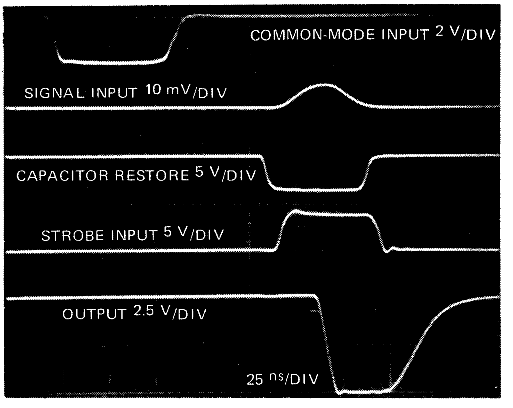
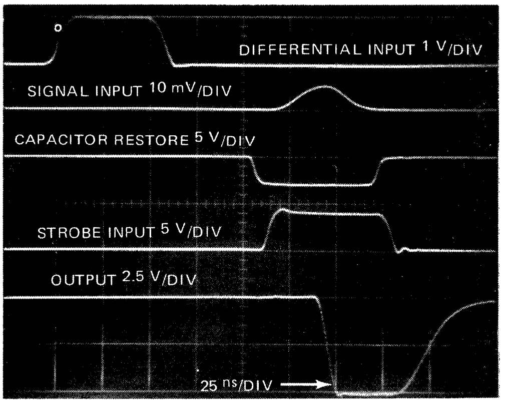
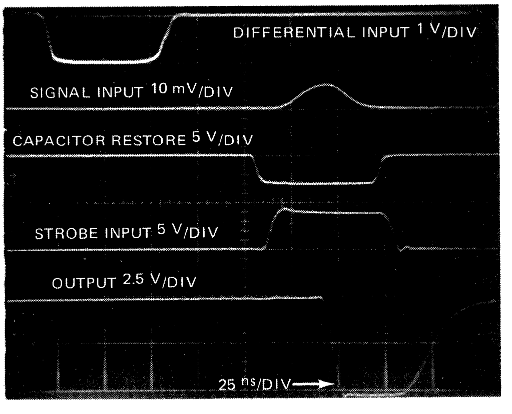


FIGURE 22 – DIFFERENTIAL-MODE CHARACTERISTICS

Note: The 5mV Input Signal is superimposed on the Differential Input and is shown separately for reference only.





8

MC1545
MC1445

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

. . . designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN475 and AN491 for design details.

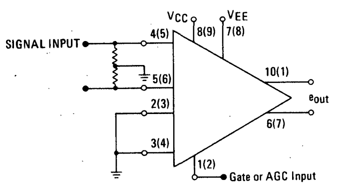
- Large Bandwidth; 75 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

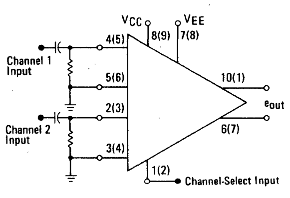
MONOLITHIC SILICON EPITAXIAL PASSIVATED

TYPICAL APPLICATIONS

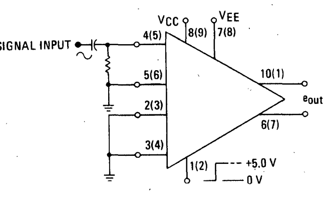
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC



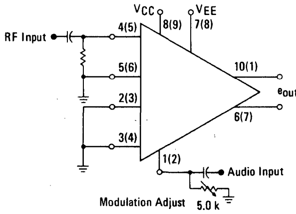
MULTIPLEX OR FSK



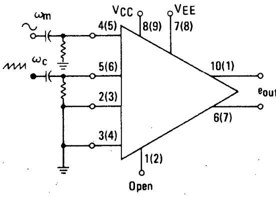
ANALOG SWITCH



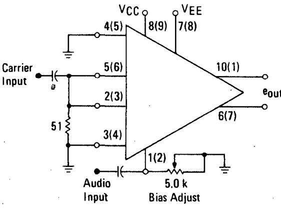
AMPLITUDE MODULATOR



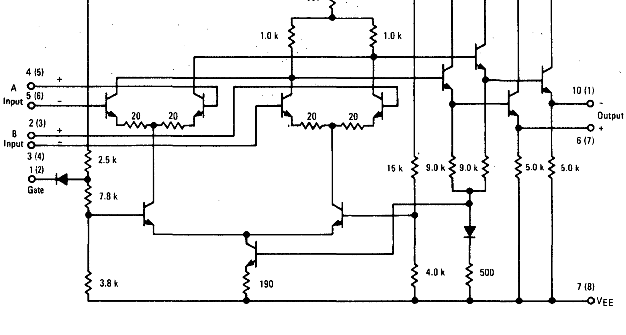
PULSE-WIDTH MODULATOR



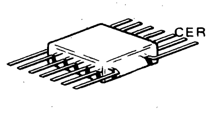
BALANCED MODULATOR



CIRCUIT SCHEMATIC

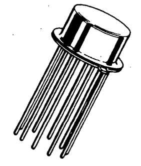


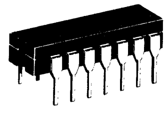
Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.



F SUFFIX
CERAMIC PACKAGE
CASE 607

G SUFFIX
METAL PACKAGE
CASE 602A





L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+12 -12	Vdc Vdc
Differential Input Signal	V_{ID}	±5.0	Volts
Load Current	I_L	25	mA
Power Dissipation (Package Limitation)	P_D		
Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Ceramic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Temperature Range MC1445 MC1545	T_A	0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = 5.0 Vdc, at T_A = +25°C, specifications apply to both input channels unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
Single-Ended Voltage Gain	MC1445 MC1545	1, 12	A_{vs}	16 16	19 18	22 20	dB
Bandwidth	MC1445 MC1545	1, 12	BW	– 50	75 75	– –	MHz
Input Impedance (f = 50 kHz)	MC1445 MC1545	5, 14	z_{is}	3.0 4.0	10 10	– –	k ohms
Output Impedance (f = 50 kHz)		6, 15	z_{os}	–	25	–	Ohms
Output Voltage Swing (R_L = 1.0 k ohm, f = 50 kHz)		4, 13	V_{OD}	1.5	2.5	–	V_{p-p}
Input Bias Current ($I_{IB} = (I_1 + I_2)/2$)	MC1445 MC1545	16	I_{IB}	– –	15 15	30 25	μAdc
Input Offset Current		16	$\|I_{IO}\|$	–	2.0	–	μAdc
Input Offset Voltage	MC1445 MC1545	17	$\|V_{IO}\|$	– –	– 1.0	7.5 5.0	mVdc
Quiescent Output dc Level		17	V_O	–	0.2	–	Vdc
Output dc Level Change (Gate Voltage Change: +5.0 V to 0 V)		17	$\|\Delta V_O\|$	–	15	–	mV
Common-Mode Rejection Ratio (f = 50 kHz)		9, 18	CMRR	–	85	–	dB
Input Common-Mode Voltage Swing		18	V_{ICR}	–	±2.5	–	V_p
Gate Characteristics		8					Vdc
Gate Voltage Low (See Note 1)	MC1445 MC1545		V_{GOL}	0.20 0.45	0.40 0.70	– –	
Gate Voltage High (See Note 2)	MC1445 MC1545		V_{GOH}	– –	1.3 1.5	3.0 2.2	
Gate Current Low (Gate Voltage = 0 V)	MC1445 MC1545	18	I_{GOL}	– –	– –	4.0 2.5	mA
Gate Current High (Gate Voltage = +5.0 V)	MC1445 MC1545	18	I_{GOH}	– –	– –	4.0 2.0	μA
Step Response (e_{in} = 20 mV)	MC1445 MC1545	19	t_{PLH}	– –	6.5 6.5	– 10	ns
	MC1445 MC1545		t_{PHL}	– –	6.3 6.3	– 10	
	MC1445 MC1545		t_r	– –	6.5 6.5	– 10	
	MC1445 MC1545		t_f	– –	7.0 7.0	– 10	
Wideband Input Noise (5.0 Hz - 10 MHz, R_S = 50 ohms)		10, 20	$V_{N(in)}$	–	25	–	μV(rms)
DC Power Dissipation	MC1445 MC1545	11, 20	P_D	– –	70 70	150 110	mW

Note 1 V_{GOL} is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
Note 2 V_{GOH} is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

8

FIGURE 1 – SINGLE-ENDED VOLTAGE GAIN versus FREQUENCY

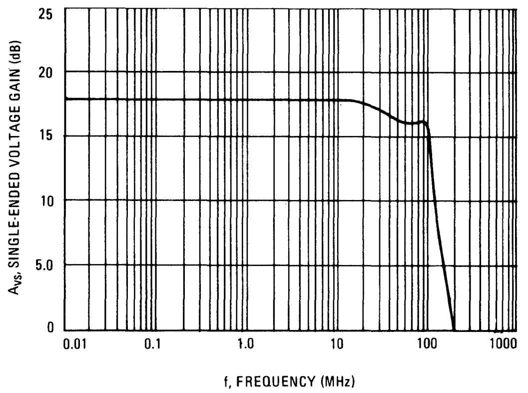


FIGURE 2 – SINGLE-ENDED VOLTAGE GAIN versus TEMPERATURE

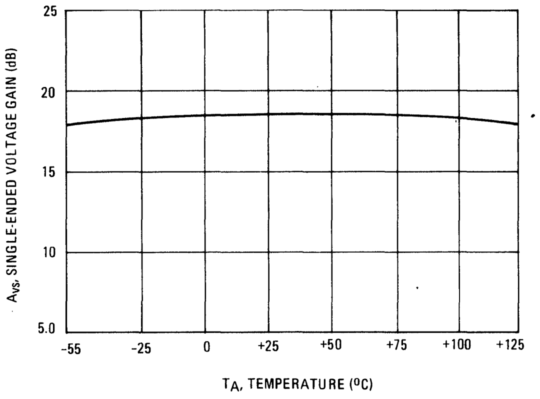


FIGURE 3 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGES

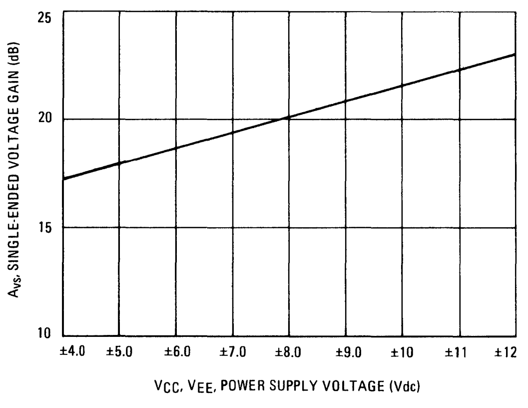


FIGURE 4 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

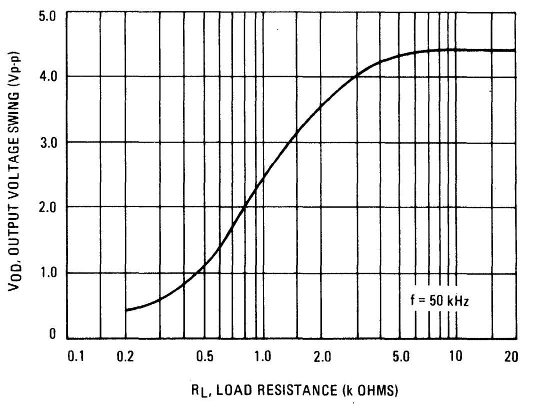


FIGURE 5 – INPUT Cp AND Rp versus FREQUENCY (BOTH CHANNELS)

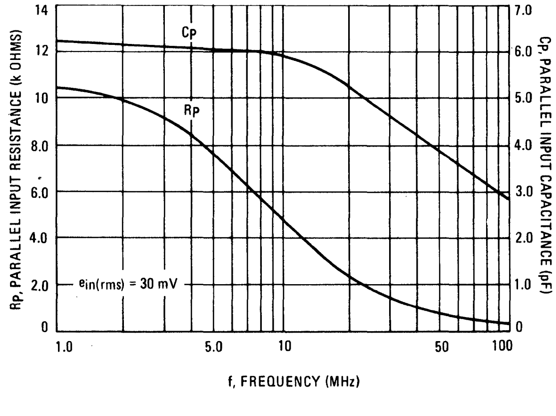


FIGURE 6 – OUTPUT IMPEDANCE versus FREQUENCY

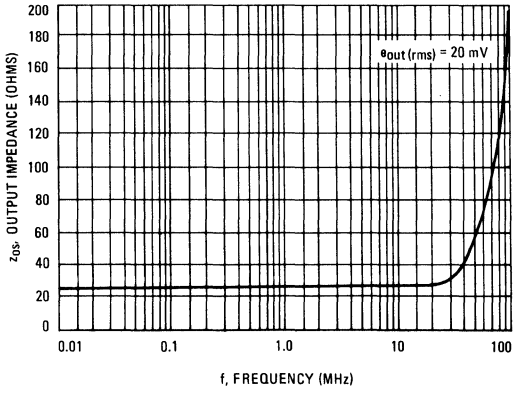


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FIGURE 7 – CHANNEL SEPARATION versus FREQUENCY

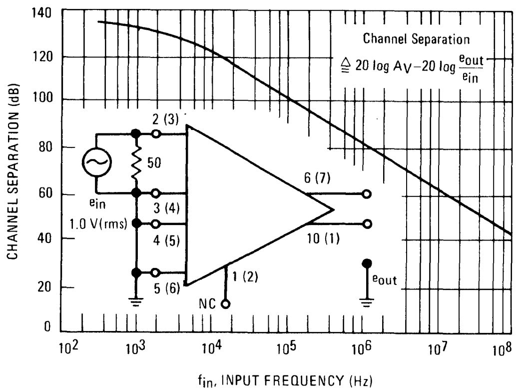


FIGURE 8 – GATE CHARACTERISTICS

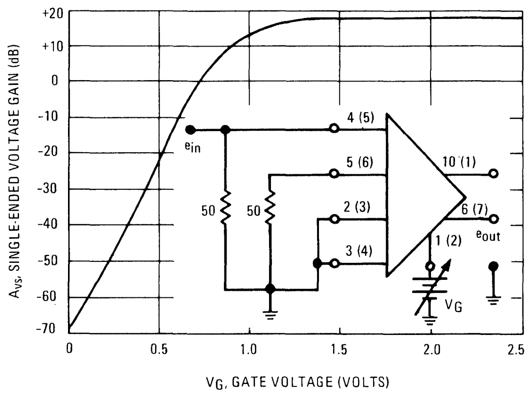


FIGURE 9 – COMMON MODE REJECTION RATIO versus FREQUENCY

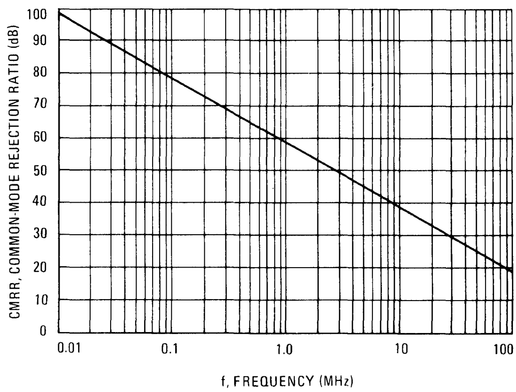


FIGURE 10 – INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

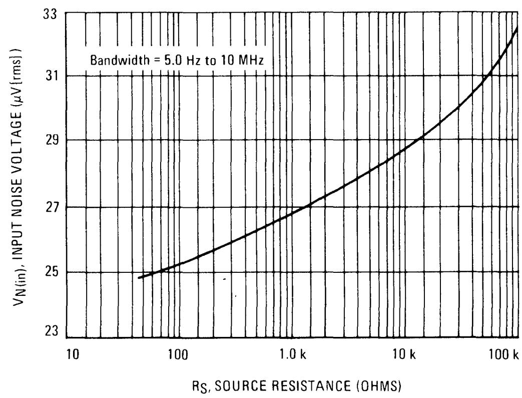


FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

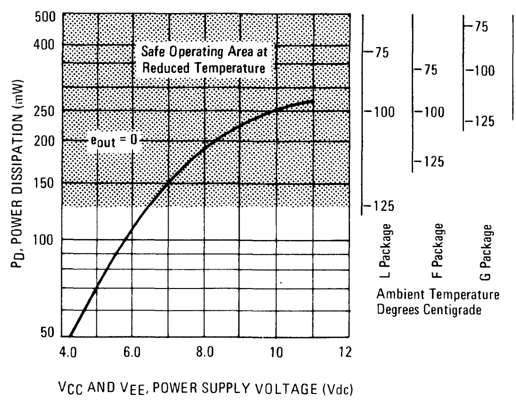
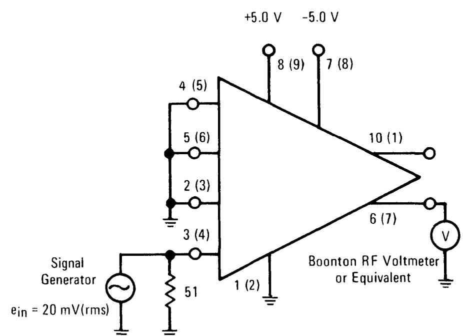


FIGURE 12 – SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

8

FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

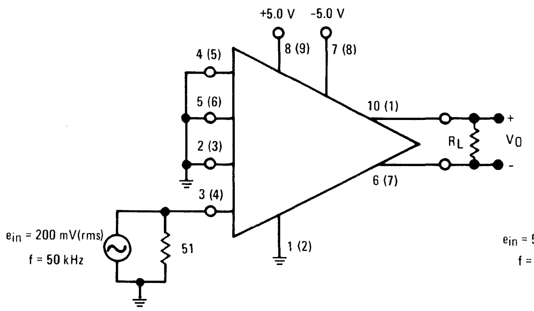


FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

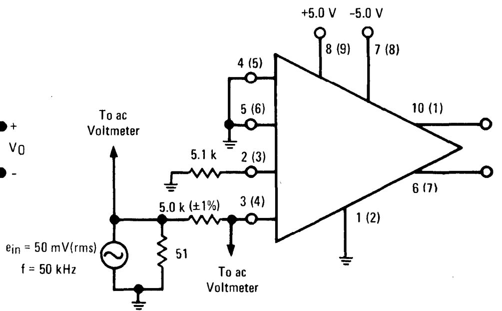


FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

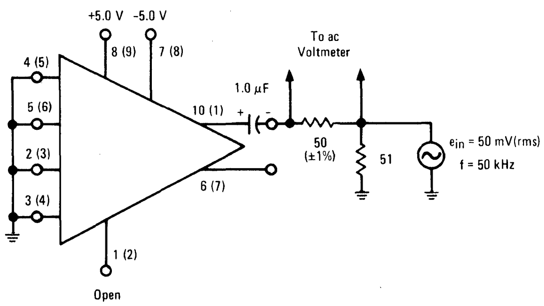


FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT

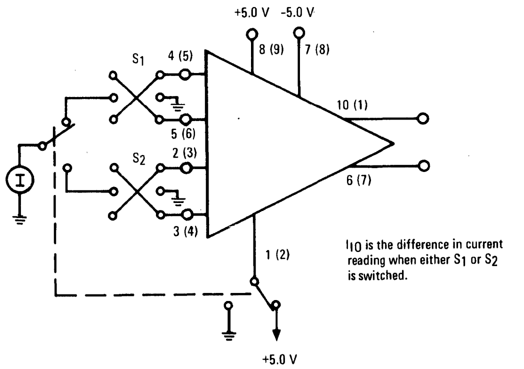


FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT

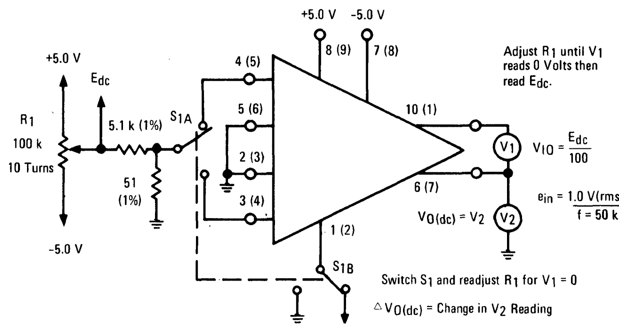
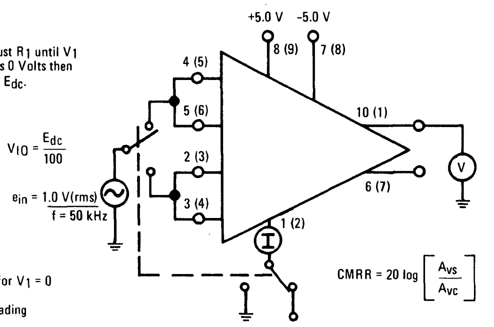


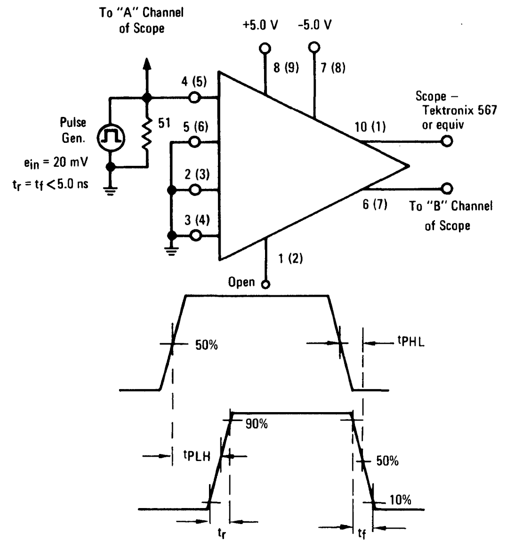
FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

8

FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages,

number at left in each case denotes corresponding pin for G package.

FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT

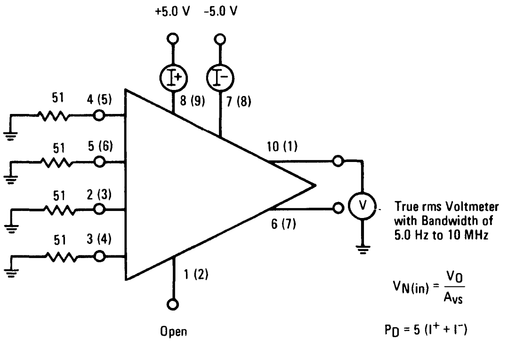
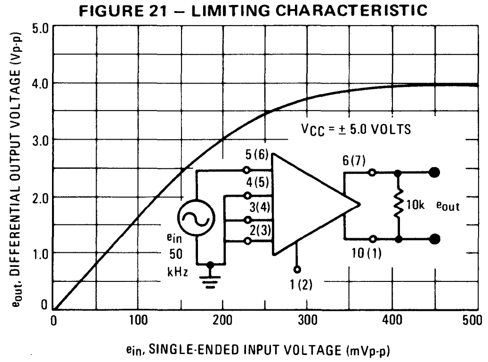


FIGURE 21 – LIMITING CHARACTERISTIC

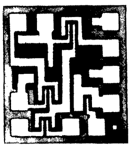


8

MC1550

HIGH-FREQUENCY CIRCUITS

INTEGRATED CIRCUIT LINEAR AMPLIFIER

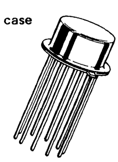


. . . a versatile, common-emitter, common-base cascode circuit for use in communications applications. See Application Notes AN-215, AN-247 and AN-299 for additional information.

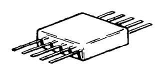
- Constant Input Impedance over entire AGC range
- Extremely Low y_{12} – 4.3 μmhos at 60 MHz
- High Power Gain – 30 dB @ 60 MHz (0.5 MHz BW)
- Good Noise Figure – 5 dB @ 60 MHz

RF – IF AMPLIFIER
INTEGRATED CIRCUIT
MONOLITHIC SILICON
EPITAXIAL PASSIVATED

Pin 7 connected to case



G SUFFIX
METAL PACKAGE
CASE 602B

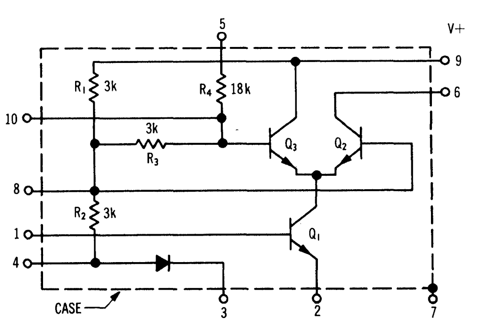


F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V+	20	Vdc
AGC Supply Voltage	V_{AGC}	20	Vdc
Differential Input Voltage, Pin 1 to Pin 4 (R_S = 500 ohms)	V_{in}	±5.0	V(rms)
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1550 is built with monolithic fabrication techniques utilizing diffused resistors and small-geometry transistors. Excellent AGC performance is obtained by shunting the signal through the AGC transistor Q_3 maintaining the operating point of the input transistor Q_1. This keeps the input impedance constant over the entire AGC range.

The amplifier is intended to be used in a common-emitter, common-base configuration (Q_1 and Q_2) with Q_3 acting as an AGC transistor. The input signal is applied between pins 1 and 4, where pin 4 is ac-coupled to ground. DC source resistance between pins 1 and 4 should be small (less than 100 ohms). Pins 2 and 3 should be connected together and grounded. Pins 8 and 10 should be bypassed to ground. The positive supply voltage is applied at pin 9 and at higher frequencies, pin 9 should also be bypassed to ground. The output is taken between pins 6 and 9. The substrate is connected to pin 7 and should be grounded. AGC voltage is applied to pin 5.

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS ($V^+ = +6$ Vdc, $T_A = +25^oC$)

Characteristic	Conditions	Figure	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS							
Output Voltage	$V_{AGC} = 0$ Vdc $V_{AGC} = +6$ Vdc	1	V_o	3.80 5.90	– –	4.65 6.00	Vdc
Test Voltage	$V_{AGC} = 0$ Vdc $V_{AGC} = +6$ Vdc	1	V8	2.85 3.25	– –	3.40 3.80	Vdc
Supply Drain Current	$V_{AGC} = 0$ Vdc $V_{AGC} = +6$ Vdc	1	I_D	– –	– –	2.2 2.5	mAdc
AGC Supply Drain Current	$V_{AGC} = 0$ Vdc $V_{AGC} = +6$ Vdc	1	I_{AGC}	– –	– –	-0.2 0.18	mAdc
SMALL-SIGNAL CHARACTERISTICS							
Small-Signal Voltage Gain	f = 500 kHz	2	A_V	22	–	29	dB
Bandwidth	-3.0 dB	2	BW	22	–	–	MHz
Transducer Power Gain	f = 60 MHz, BW = 6 MHz f = 100 MHz, BW = 6 MHz	3	A_P	– –	25 21	– –	dB

TYPICAL CHARACTERISTICS

($V^+ = 6.0$ Vdc, $T_A = +25^oC$ unless otherwise noted)

FIGURE 1 – DC CHARACTERISTICS TEST CIRCUIT

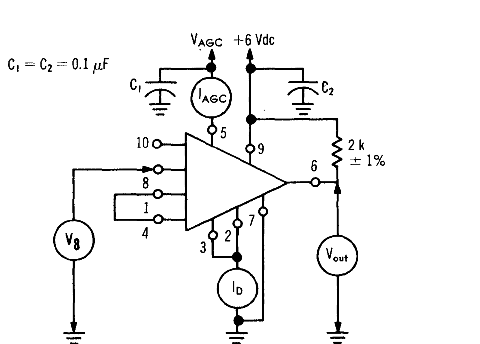


FIGURE 2 – VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT

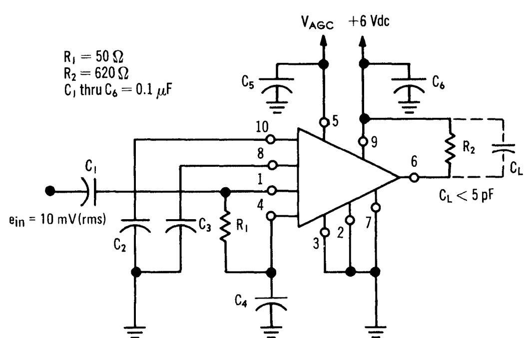


FIGURE 3 – POWER GAIN TEST CIRCUIT @ 60 MHz

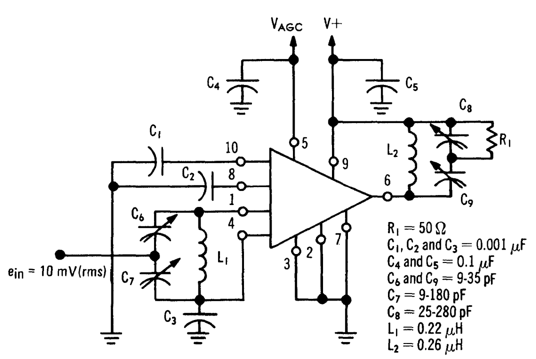
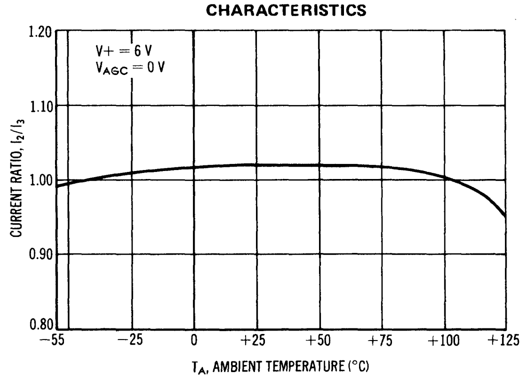


FIGURE 4 – DRAIN CURRENT TEMPERATURE CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

FIGURE 5 – INPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

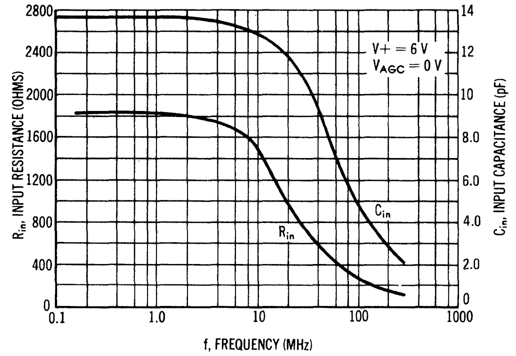


FIGURE 6 – INPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

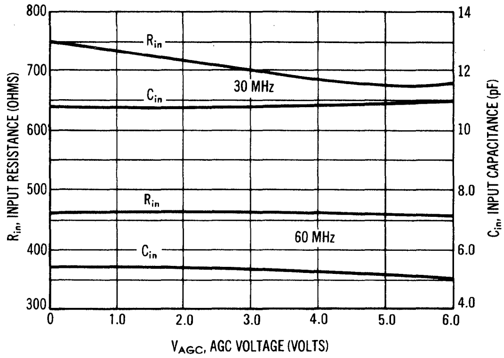


FIGURE 7 – OUTPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

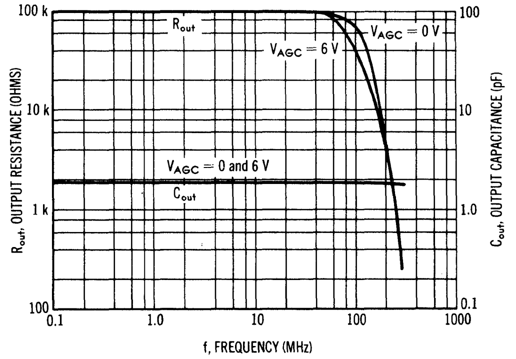


FIGURE 8 – OUTPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

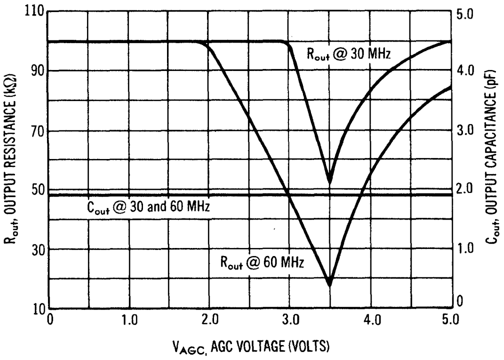


FIGURE 9 – MAXIMUM TRANSDUCER POWER GAIN versus FREQUENCY

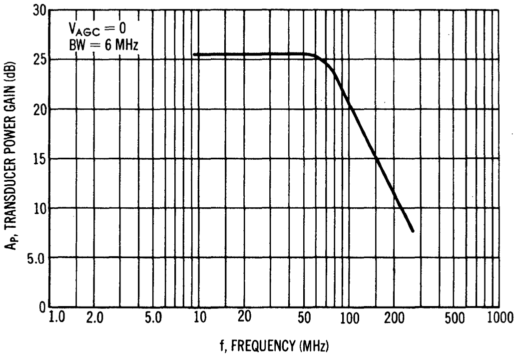
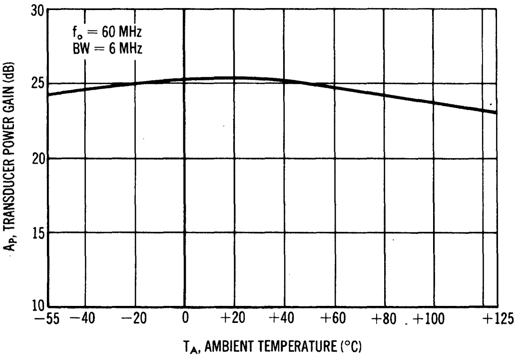


FIGURE 10 – TRANSDUCER POWER GAIN versus TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 11 – TRANSDUCER POWER BANDWIDTH versus AGC VOLTAGE

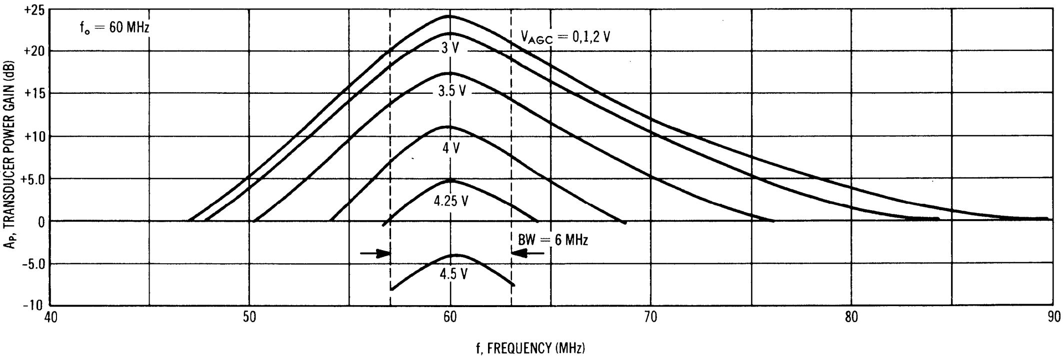


FIGURE 12 – NOISE FIGURE AND OPTIMUM SOURCE RESISTANCE versus FREQUENCY

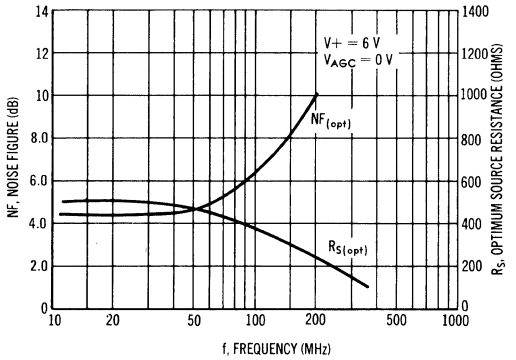


FIGURE 13 – NOISE FIGURE versus SOURCE RESISTANCE

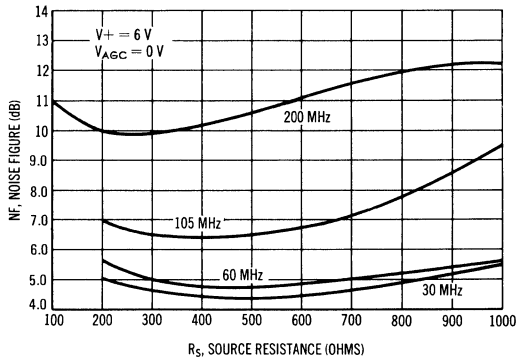


FIGURE 14 – y_{21}, FORWARD-TRANSFER ADMITTANCE versus FREQUENCY

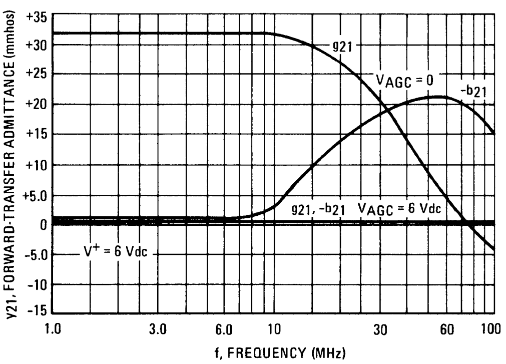
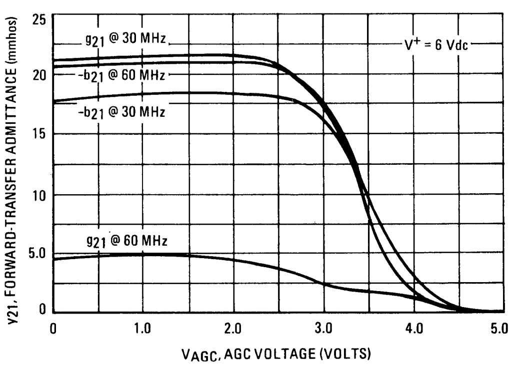


FIGURE 15 – y_{21}, FORWARD-TRANSFER ADMITTANCE versus AGC VOLTAGE



8

TYPICAL CHARACTERISTICS

(V^+ = 6.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 16 — y_{12}, REVERSE TRANSFER-ADMITTANCE versus FREQUENCY

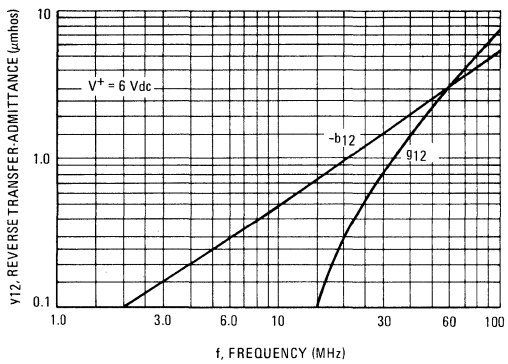
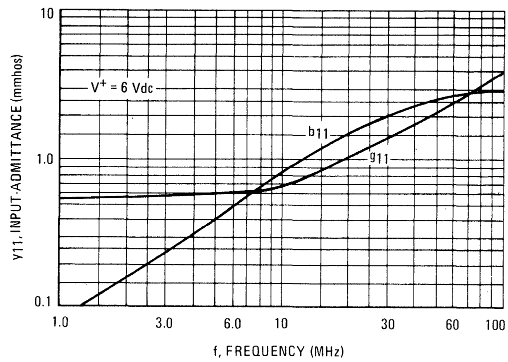


FIGURE 17 — y_{11}, INPUT-ADMITTANCE versus FREQUENCY



The y_{12} shown in Figure 16 illustrates the extremely low feedback of the MC1550 with no contribution from the external mounting circuitry. However, in many cases the external circuitry may contribute as much or more to the total feedback than does the MC1550.

To perform more accurate design calculations of gain, stability, and input - output impedances it is recommended that the designer first determine the total feedback of device plus circuitry.

This can be done in one of two ways:

(1) Measure the total y_{12} or s_{12} of the MC1550 installed in its mounting circuitry, or

(2) Measure the y_{12} of the circuitry alone (without the MC1550 installed) and add the circuit y_{12} to the y_{12} for the MC1550 given in Figure 16.

FIGURE 19 — s_{11} AND s_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

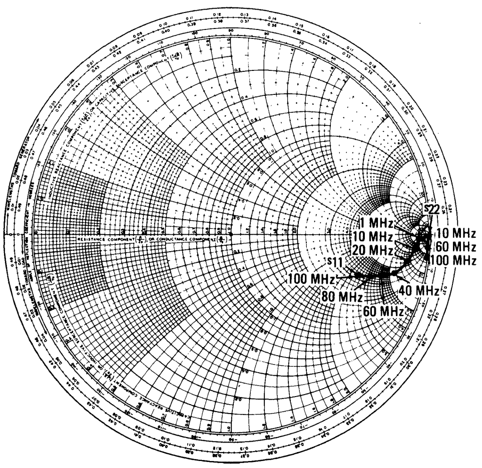
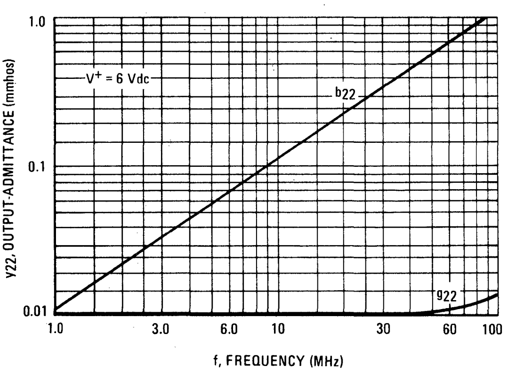


FIGURE 18 — y_{22}, OUTPUT-ADMITTANCE versus FREQUENCY



8

TYPICAL CHARACTERISTICS (continued)

(V^+ = 6.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 20 – s_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY

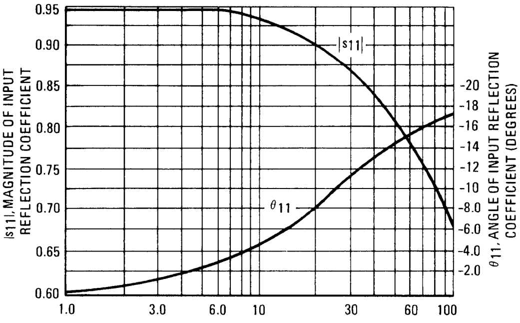


FIGURE 21 – s_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

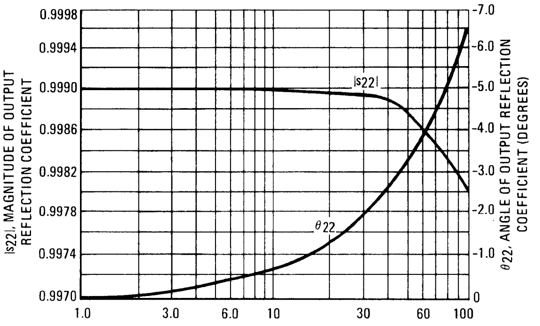


FIGURE 22 – s_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

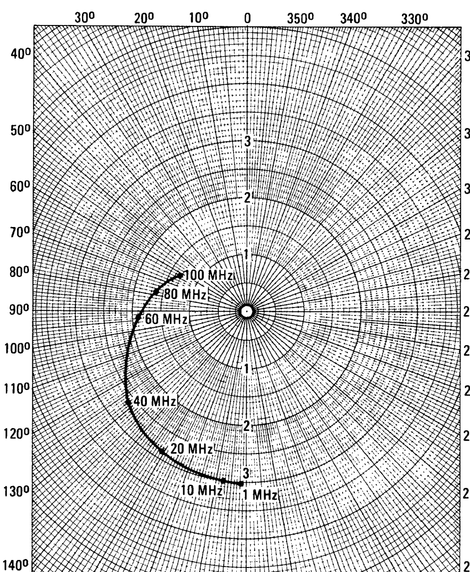
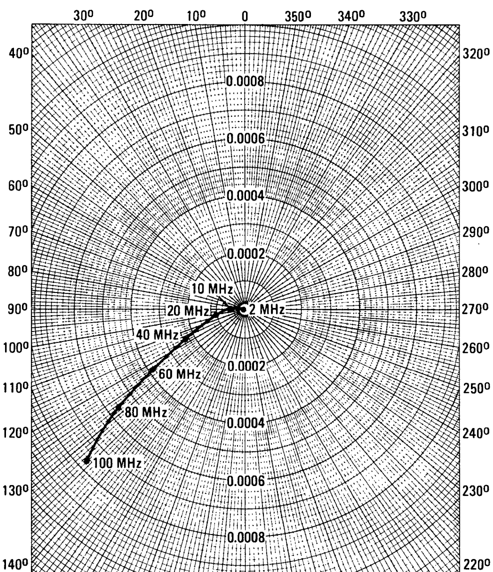


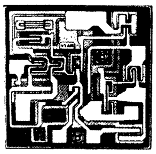
FIGURE 23 – s_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



8

MC1552G
MC1553G

MONOLITHIC VIDEO AMPLIFIER

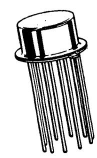


. . . a three-stage, direct-coupled, common-emitter cascade incorporating series-series feedback to achieve stable voltage gain, low distortion, and wide bandwidth. Employs a temperature-compensated dc feedback loop to stabilize the operating point and a current-biased emitter follower output. Intended for use as either a wide-band linear amplifier or as a fast rise pulse amplifier.

- High Gain – 34 dB ± 1 dB (MC1552)
  52 dB ± 1 dB (MC1553)
- Wide Bandwidth – 40 MHz (MC1552)
  35 MHz (MC1553)
- Low Distortion – 0.2% at 200 kHz
- Low Temperature Drift – ±0.002 dB/°C

HIGH FREQUENCY INTEGRATED CIRCUITS

SILICON EPITAXIAL PASSIVATED



METAL PACKAGE
CASE 602B

Pin 6 connected to case

MAXIMUM RATINGS ($T_A = +25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V^+	9	Vdc
Input Voltage, Pin 1 to Pin 2 (R_S = 500 ohms)	V_{in}	1.0	V(rms)
Power Dissipation (Package Limitation) Derate above $T_A = +25°C$	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATICS

FIGURE 1 – MC1552 (LOW GAIN)

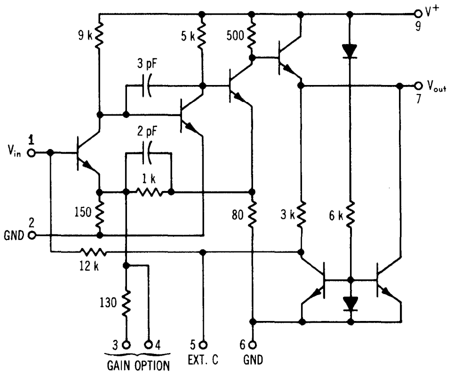
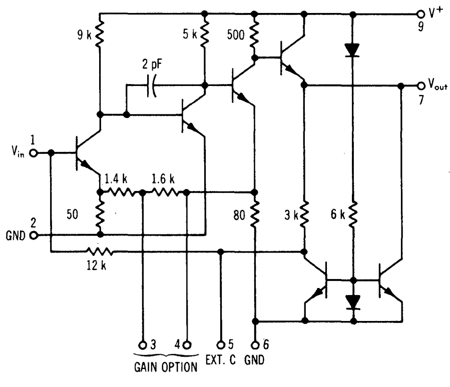


FIGURE 2 – MC1553 (HIGH GAIN)



See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS ($V^+ = +6$ Vdc, $T_A = +25°C$ unless otherwise noted)

Characteristic		Fig. No.	Gain Option*	Symbol	Min	Typ	Max	Unit
Voltage Gain	MC1552	3	50 100	V_{out}/V_{in}	44 87	50 100	56 113	V/V
	MC1553		200 400		175 350	200 400	225 450	
Voltage Gain Variation (T_A = -55°C to +125°C)		3	All	—	—	±0.2	—	dB
Bandwidth	MC1552	3, 6	50 100	BW	21 17	40 35	— —	MHz
	MC1553		200 400		17 7.5	35 15	— —	
Input Impedance (f = 100 kHz, R_L = 1 kΩ)		—	All	$\|Z_{in}\|$	7	10	—	kΩ
Output Impedance (f = 100 kHz, R_S = 50 Ω)		—	All	$\|Z_{out}\|$	—	16	50	Ω
DC Output Voltage		3	All	V_{out} (dc)	2.5	2.9	3.2	Vdc
DC Output Voltage Variation (T_A = -55°C to +125°C)		3	All	ΔV_{out} (dc)	—	±0.05	—	Vdc
Output Voltage Swing ($Z_L \geq 1$ kΩ, V_{in} = 100 mV[rms])		3	All	V_{out}	3.6	4.2	—	Vp-p
Power Dissipation		—	All	P_D	—	75	120	mW
Delay Time	MC1552	3, 4	50 100	t_{pd}	— —	8 9	— —	ns
	MC1553		200 400		— —	10 25	— —	
Rise Time	MC1552	3, 4	50 100	t_r	— —	9 12	16 20	ns
	MC1553		200 400		— —	11 30	20 45	
Overshoot		3, 4	All	$(V_{os}/V_p)100$	—	5	—	%
Noise Figure (R_S = 400 Ω, f_o = 30 MHz, BW = 3 MHz)		—	All	NF	—	5	—	dB
Total Harmonic Distortion (V_{out} = 2 Vp-p, f = 200 kHz, R_L = 1 kΩ)		—	All	THD	—	0.2	—	%

*To obtain the voltage-gain characteristic desired, use the following pin connections:

Type	Voltage Gain	Pin Connections
MC1552	50	Pin 3 Open
	100	Ground Pin 3
MC1553	200	Connect Pin 3 to Pin 4
	400	Pins 3 and 4 Open

NOTES

1. Ground Pin 6 as close to can as possible to minimize overshoot. Best results by directly grounding can.

2. If large input and output coupling capacitors are used, place shield between them to avoid input-output coupling.

3. A high-frequency capacitor must always be used to bypass the power supply. This capacitor should be as close to the circuit as possible.

4. Voltage gain can be adjusted to any value between 50 and 3000 by connecting an external resistor from Pin 4 to ground on MC1552, or from Pin 3 to ground on MC1553, as shown in Figure 8. Under these conditions, the following equations must be used to determine C_1 and C_2 rather than the circuits shown in Figure 5.

Fig. 5b $C_1 = \frac{1}{2\pi f_c (1.7 \times 10^4)}$ Farads; $C_2 = 8\, C_1 (V_{out}/V_{in})$ Farads

Fig. 5c $C_1 = \frac{V_{out}/V_{in}}{2\pi f_c (1.5 \times 10^4)}$ Farads

Fig. 5d $C_2 = \frac{V_{out}/V_{in}}{2\pi f_c (3 \times 10^3)}$ Farads

FIGURE 3 — TEST CIRCUIT

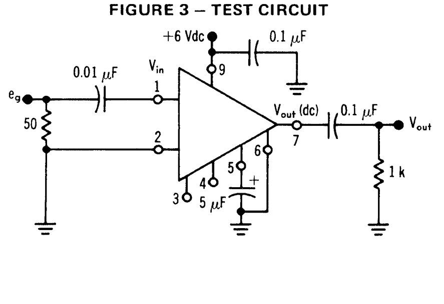
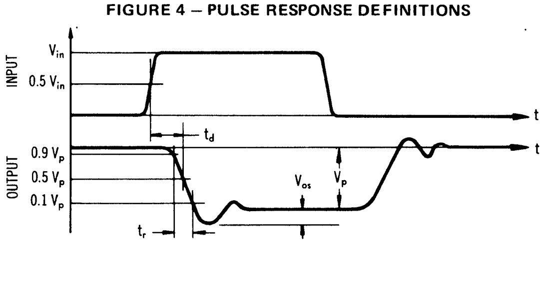


FIGURE 4 — PULSE RESPONSE DEFINITIONS



8

TYPICAL CHARACTERISTICS

$T_A = +25°C$

FIGURE 5a – FREQUENCY RESPONSE

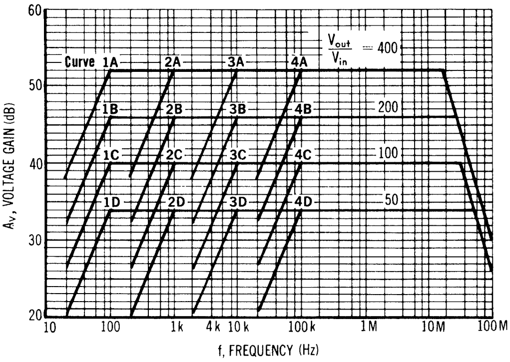
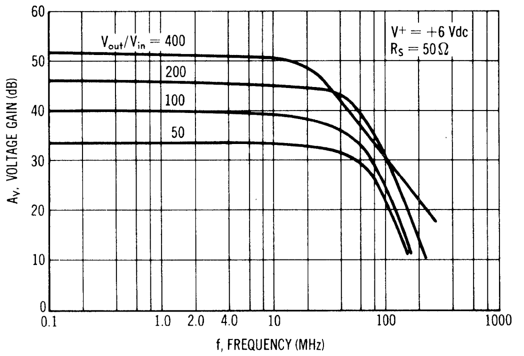
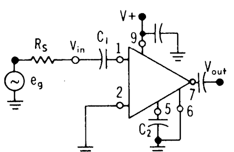


FIGURE 6 – VOLTAGE GAIN versus FREQUENCY



TEST CIRCUITS FOR FREQUENCY RESPONSE

FIGURE 5b – CAPACITIVE COUPLED INPUT (R_S < 5 kΩ)



Curve No.	C_1 (μF)	C_2 (μF)
1A	0.1	250
1B	0.1	150
1C	0.1	70
1D	0.1	40

Curve No.	C_1 (μF)	C_2 (μF)
2A	0.01	30
2B	0.01	18
2C	0.01	8.0
2D	0.01	4.0
	(pF)	
3A	1000	3.0
3B	1000	1.8
3C	1000	0.8
3D	1000	0.4
4A	100	0.3
4B	100	0.18
4C	100	0.08
4D	100	0.04

FIGURE 7 – MAXIMUM NEGATIVE SWING SLEW RATE versus LOAD CAPACITANCE

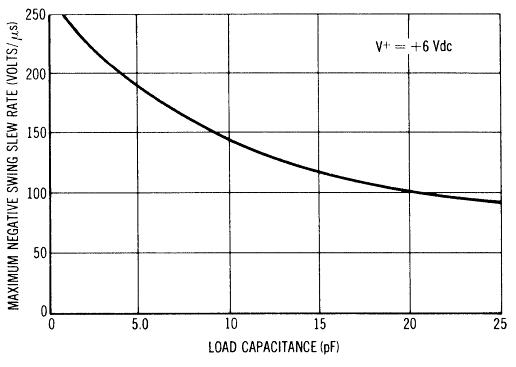
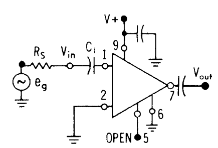


FIGURE 5c – CAPACITIVE COUPLED INPUT (R_S < 500 Ω)



Curve No.	C_1 (μF)	Curve No.	C_1 (μF)
1A	20	3A	0.4
1B	10	3B	0.2
1C	7.0	3C	0.1
1D	3.0	3D	0.06
2A	3.0	4A	0.04
2B	1.0	4B	0.02
2C	0.8	4C	0.01
2D	0.5	4D	0.007

FIGURE 8 – VOLTAGE GAIN ADJUSTMENT BY USE OF EXTERNAL RESISTOR

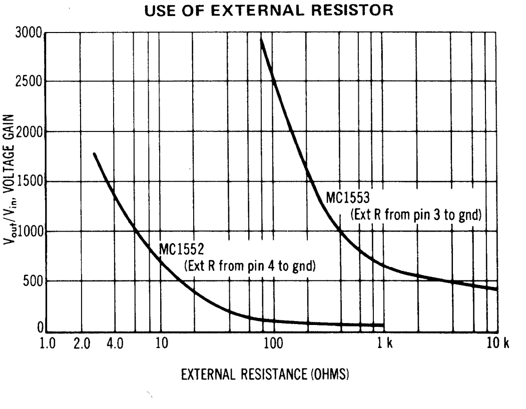
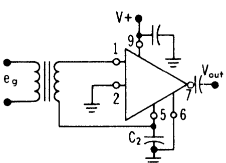


FIGURE 5d – TRANSFORMER COUPLED INPUT



Curve No.	C_2 (μF)	Curve No.	C_2 (μF)
1A	200	3A	2.0
1B	100	3B	1.0
1C	70	3C	0.7
1D	30	3D	0.3
2A	20	4A	0.2
2B	10	4B	0.1
2C	7.0	4C	0.07
2D	3.0	4D	0.03

8

INPUT ADMITTANCE

V+ = 6 Vdc, R_L = 1 kΩ, T_A = +25°C

FIGURE 9 – GAIN = 50

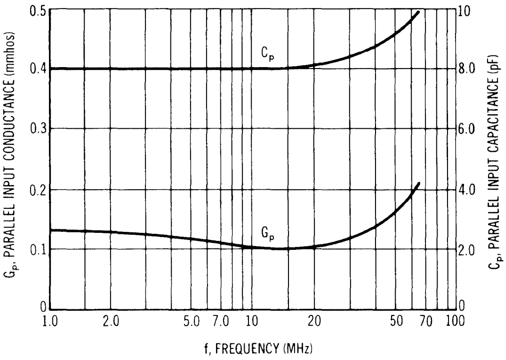


FIGURE 10 – GAIN = 100

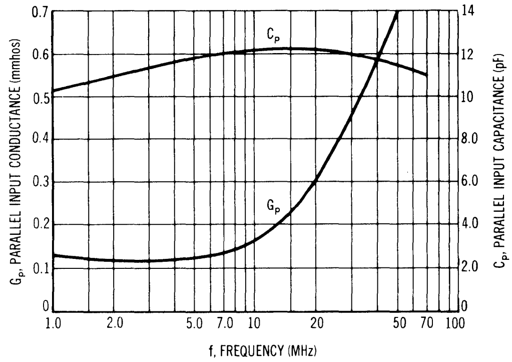


FIGURE 11 – GAIN = 200

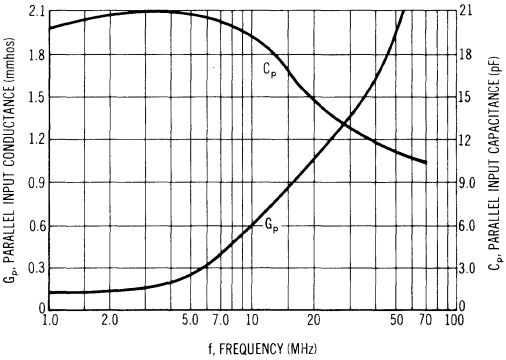


FIGURE 12 – GAIN = 400

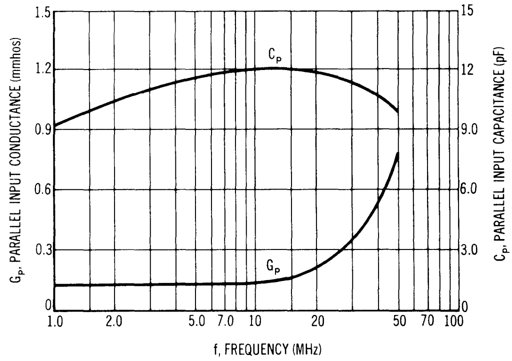


FIGURE 13 – OUTPUT IMPEDANCE versus FREQUENCY

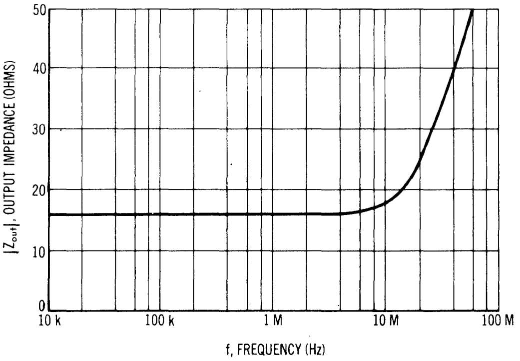
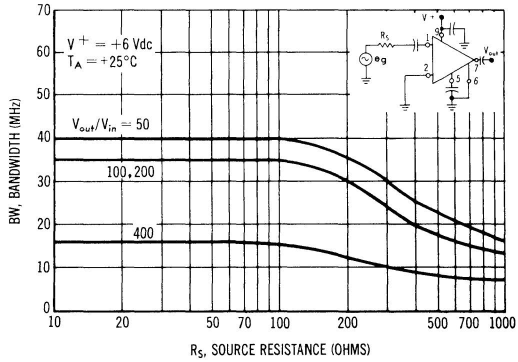


FIGURE 14 – BANDWIDTH versus SOURCE RESISTANCE

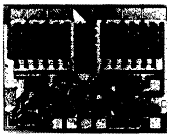


8

MC1554G
MC1454G

POWER AMPLIFIER

MONOLITHIC 1-WATT POWER AMPLIFIERS

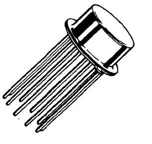


. . . designed to amplify signals to 300-kHz with 1-Watt delivered to a direct coupled or capacitively coupled load.

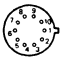
- Low Total Harmonic Distortion – 0.4% (Typ) @ 1 Watt
- Low Output Impedance – 0.2 Ohm
- Excellent Gain – Temperature Stability

1-WATT POWER AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC
SILICON EPITAXIAL PASSIVATED

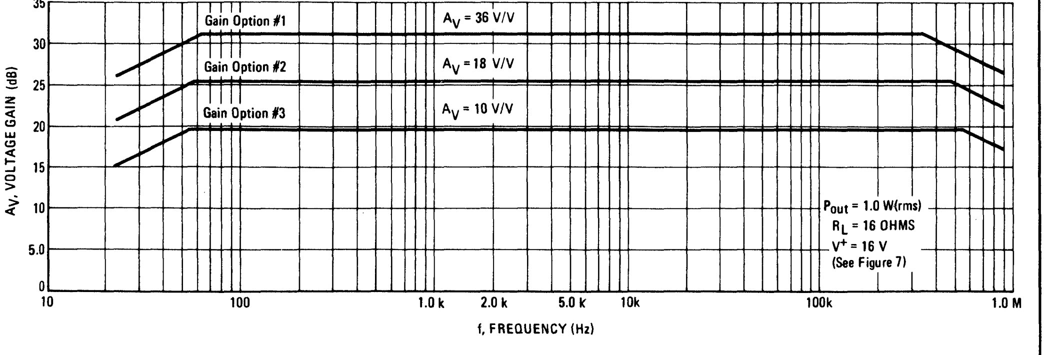


METAL PACKAGE
CASE 602B

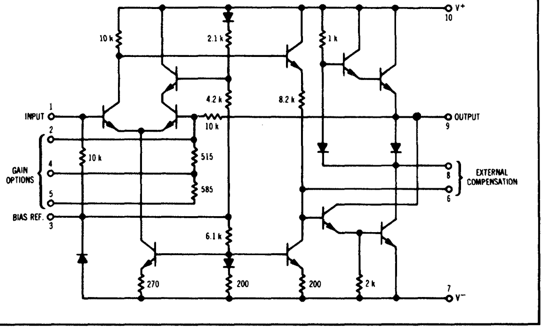


(bottom view)
Pin 7 connected to case

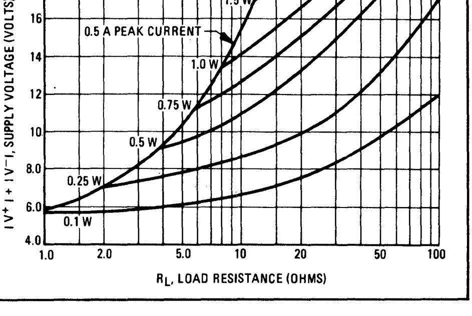
VOLTAGE GAIN versus FREQUENCY (R_L = 16 OHMS)



CIRCUIT SCHEMATIC



MAXIMUM AVAILABLE OUTPUT POWER (SINE WAVE)



See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)
Frequency compensation shown in Figures 6 and 7.

Characteristic	Figure	R_L (Ohms)	Gain Option*	Symbol	MC1554 (-55 to +125°C)			MC1454 (0 to +70°C)			Unit
					Min	Typ	Max	Min	Typ	Max	
Output Power (for e_{out}<5.0% THD)	1	16	–	P_{out}	1.0	1.1	–	–	1.0	–	Watt
Power Dissipation (@ P_{out} = 1.0 W)	1	16	–	P_D	–	0.9	1.2	–	0.9	–	Watt
Voltage Gain	1	16	10	A_V	8.0	10	12	–	10	–	V/V
		16	18		–	18	–	–	18	–	
		16	36		–	36	–	–	36	–	
Input Impedance	1	–	10	Z_{in}	7.0	10	–	3.0	10	–	kΩ
Output Impedance	1	–	10	Z_{out}	–	0.2	–	–	0.4	–	Ω
Power Bandwidth (for e_{out}<5.0% THD)	2	16	10		–	270	–	–	270	–	kHz
		16	18		–	250	–	–	250	–	
		16	36		–	210	–	–	210	–	
Total Harmonic Distortion (for e_{in}<0.05% THD, f = 20 Hz to 20 kHz)	2			THD							%
P_{out} = 1.0 Watt (sinewave)		16	10		–	0.4	–	–	0.4	–	
P_{out} = 0.1 Watt (sinewave)		16	10		–	0.5	–	–	0.5	–	
Zero Signal Current Drain	3	∞	–	I_D	–	11	15	–	11	20	mAdc
Output Noise Voltage	3	16	10	V_n	–	0.3	–	–	0.3	–	mV(rms)
Output Quiescent Voltage (Split Supply Operation)	4	16	–	V_{out}(dc)	–	±10	±30	–	±10	–	mVdc
Positive Supply Sensitivity (V^- constant)	5	∞	–	S^+	–	-40	–	–	-40	–	mV/V
Negative Supply Sensitivity (V^+ constant)	5	∞	–	S^-	–	-40	–	–	-40	–	mV/V

*To obtain the voltage gain characteristic desired, use the following pin connections:

Voltage Gain	Pin Connection
10	Pins 2 and 4 open, Pin 5 to ac ground
18	Pins 2 and 5 open, Pin 4 to ac ground
36	Pin 2 connected to Pin 5, Pin 4 to ac ground

Characteristic Definitions
(Linear Operation)

FIGURE 1

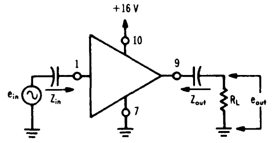


FIGURE 3

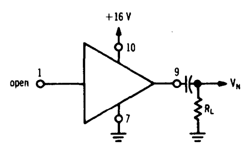


FIGURE 4

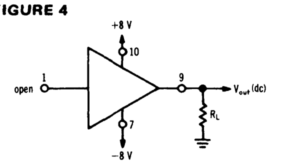


FIGURE 2

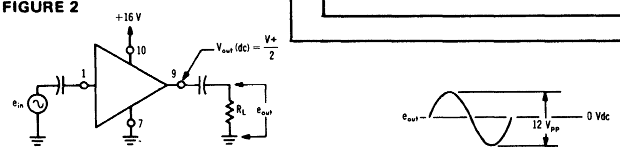
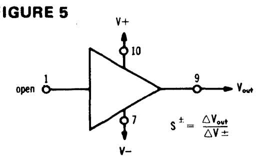


FIGURE 5



8

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Total Power Supply Voltage	$\lvert V^+ \rvert + \lvert V^- \rvert$	18	Vdc
Peak Load Current	I_{out}	0.5	Ampere
Audio Output Power	P_{out}	1.8	Watts
Power Dissipation (package limitation)			
T_A = +25°C	P_D	600	mW
Derate above 25°C	$1/\theta_{JA}$	4.8	mW/°C
T_C = +25°C	P_D	1.8	Watts
Derate above 25°C	$1/\theta_{JC}$	14.4	mW/°C
Operating Temperature Range MC1454	T_A	0 to +70	°C
MC1554		-55 to +125	
Storage Temperature Range	T_{stg}	-55 to +150	°C

TYPICAL CONNECTIONS

FIGURE 6 – SPLIT SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx 25$ Hz

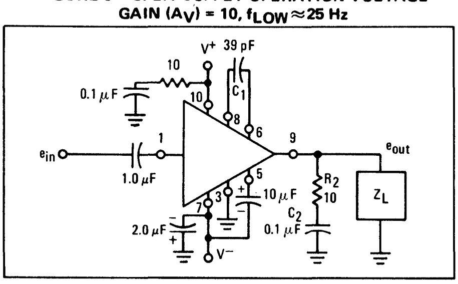
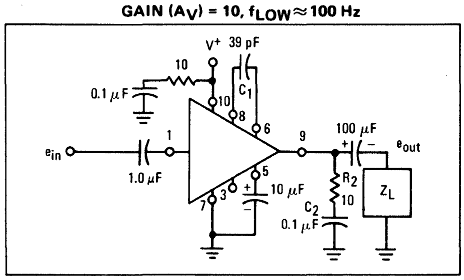


FIGURE 7 – SINGLE SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx 100$ Hz



RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

1. An R-C stabilizing network (0.1 μF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 6 and 7, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from the V+ supply to pin 10 can cause high frequency instability. To prevent this, the V+ by-pass capacitor should be connected with short leads from the V+ pin to ground. If this capacitor is remotely located a series R-C network (0.1 μF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 6 and 7.
3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In applications which require upper band-edge control the input low-pass filter is recommended.

TYPICAL CHARACTERISTICS

FIGURE 8 – TOTAL HARMONIC DISTORTION versus LOAD RESISTANCE

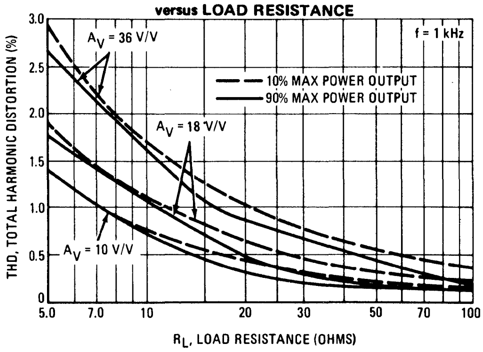
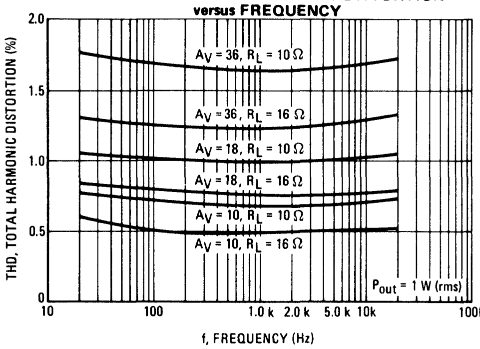


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 — VOLTAGE GAIN versus TEMPERATURE

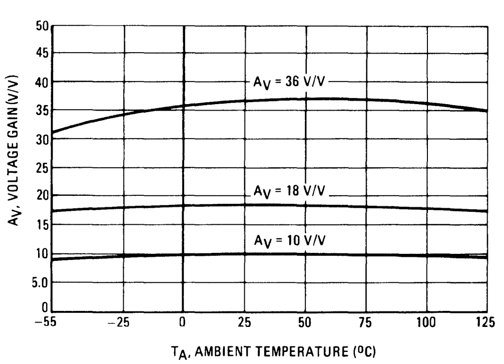


FIGURE 11 — OUTPUT VOLTAGE CHANGE

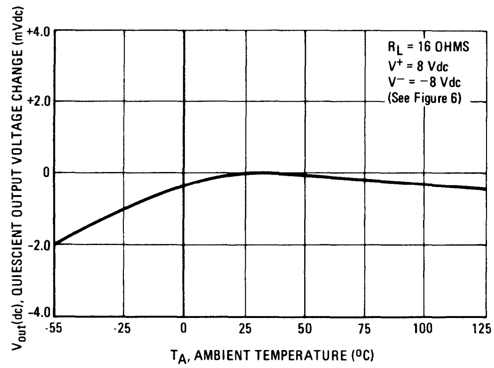


FIGURE 12 — VOLTAGE GAIN versus FREQUENCY ($R_L = \infty$)

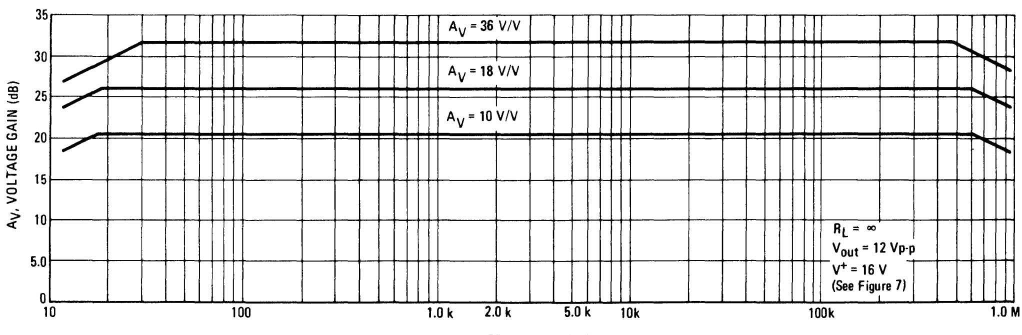
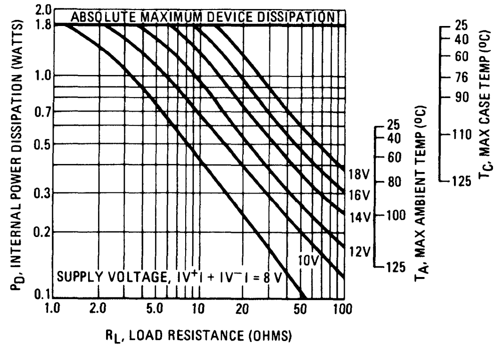


FIGURE 13 — MAXIMUM DEVICE DISSIPATION (SINE WAVE)



8

MC1555
MC1455

TIMING CIRCUIT

Specifications and Applications Information

MONOLITHIC TIMING CIRCUIT

The MC1555/MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE555/SE555 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output

FIGURE 1 – 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

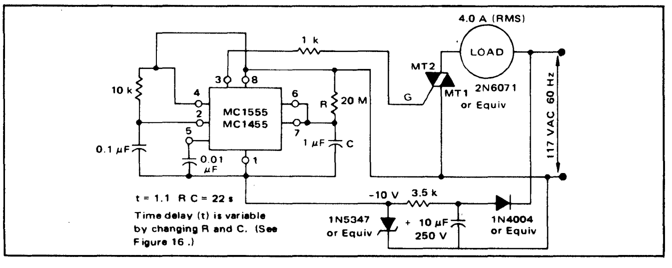
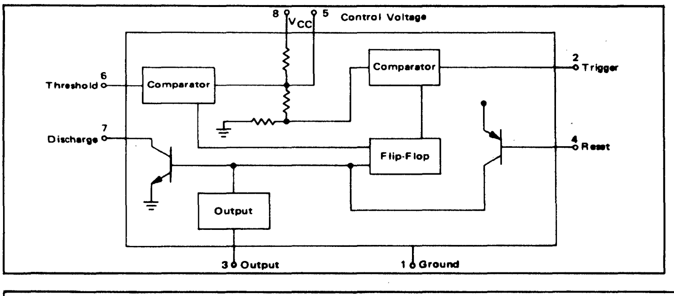


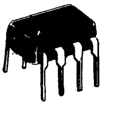
FIGURE 2 – BLOCK DIAGRAM

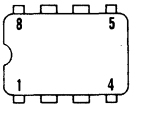


TIMING CIRCUIT

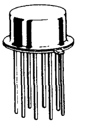
MONOLITHIC SILICON INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(Top View)
(MC1455P1 only)



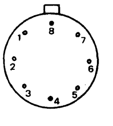


1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}



G SUFFIX
METAL PACKAGE
CASE 601

(Top View)



1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

TYPICAL APPLICATIONS

- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

See Packaging Information Section for outline dimensions.

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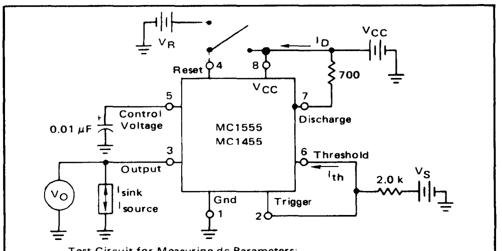
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range (Ambient)	T_A		°C
MC1555		-55 to +125	
MC1455		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters:
(to set output and measure parameters)
a). When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b). When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c). When V_O is low, pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into pin 7. When Reset is not in use, it should be tied to V_{CC}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	MC1555			MC1455			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	–	18	4.5	–	16	V
Supply Current	I_D							mA
V_{CC} = 5.0 V, $R_L = \infty$		–	3.0	5.0	–	3.0	6.0	
V_{CC} = 15 V, $R_L = \infty$		–	10	12	–	10	15	
Low State, (Note 1)								
Timing Error (Note 2)								
R_A, R_B = 1.0 kΩ to 100 kΩ								
Initial Accuracy C = 0.1 µF		–	0.5	2.0	–	1.0	–	%
Drift with Temperature		–	30	100	–	50	–	PPM/°C
Drift with Supply Voltage		–	0.005	0.02	–	0.01	–	%/Volt
Threshold Voltage	V_{th}	–	2/3	–	–	2/3	–	xV_{CC}
Trigger Voltage	V_T							V
V_{CC} = 15 V		4.8	5.0	5.2	–	5.0	–	
V_{CC} = 5.0 V		1.45	1.67	1.9	–	1.67	–	
Trigger Current	I_T	–	0.5	–	–	0.5	–	µA
Reset Voltage	V_R	0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.1	0.25	–	0.1	0.25	µA
Control Voltage Level	V_{CL}							V
V_{CC} = 15 V		9.6	10	10.4	9.0	10	11	
V_{CC} = 5.0 V		2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Low	V_{OL}							
(V_{CC} = 15 V)								V
I_{sink} = 10 mA		–	0.1	0.15	–	0.1	0.25	
I_{sink} = 50 mA		–	0.4	0.5	–	0.4	0.75	
I_{sink} = 100 mA		–	2.0	2.2	–	2.0	2.5	
I_{sink} = 200 mA		–	2.5	–	–	2.5	–	
(V_{CC} = 5.0 V)								
I_{sink} = 8.0 mA		–	0.1	0.25	–	–	–	
I_{sink} = 5.0 mA		–	–	–	–	0.25	0.35	
Output Voltage High	V_{OH}							V
(I_{source} = 200 mA)								
V_{CC} = 15 V		–	12.5	–	–	12.5	–	
(I_{source} = 100 mA)								
V_{CC} = 15 V		13	13.3	–	12.75	13.3	–	
V_{CC} = 5.0 V		3.0	3.3	–	2.75	3.3	–	
Rise Time of Output	t_{OLH}	–	100	–	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	–	100	–	ns

NOTES:
1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

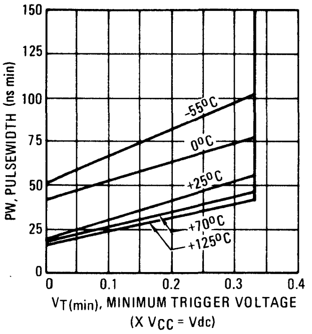


FIGURE 5 – SUPPLY CURRENT

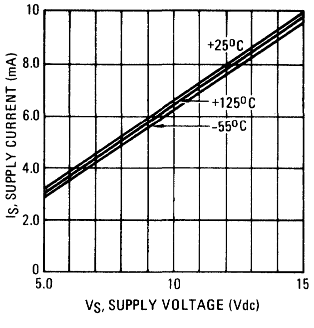


FIGURE 6 – HIGH OUTPUT VOLTAGE

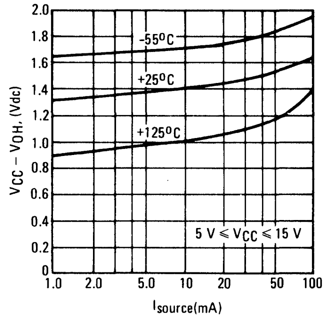


FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

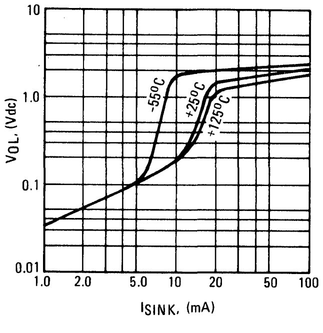


FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

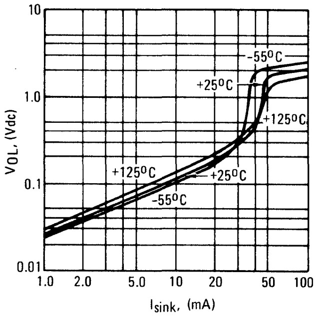


FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

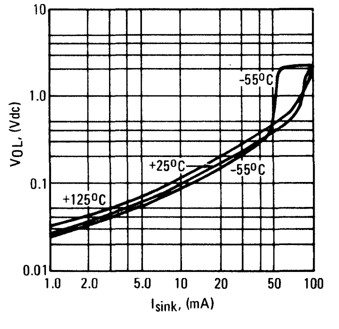


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

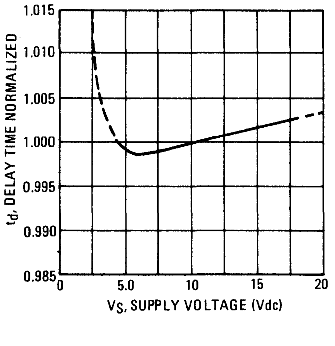


FIGURE 11 – DELAY TIME versus TEMPERATURE

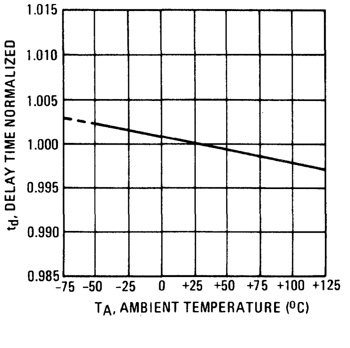
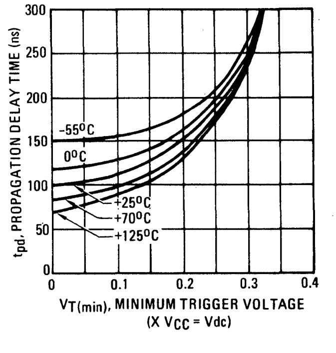


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE



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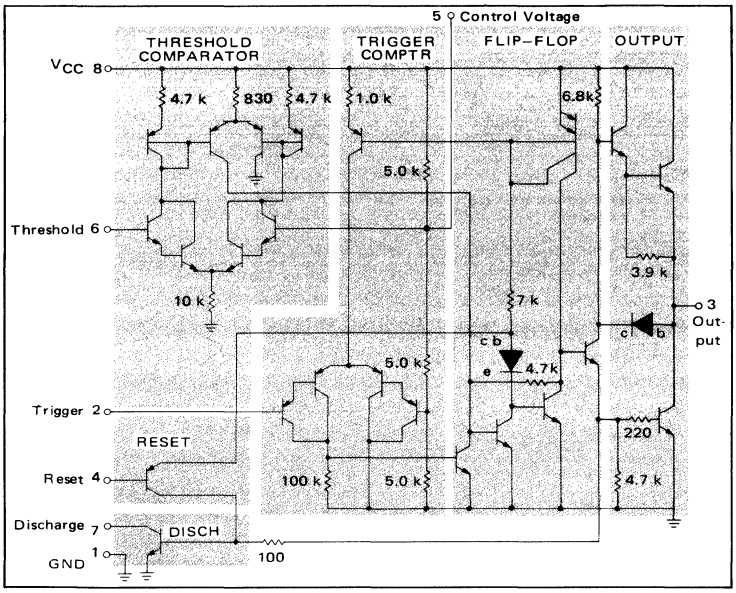


FIGURE 13 – CIRCUIT SCHEMATIC CONTROL VOLTAGE

GENERAL OPERATION

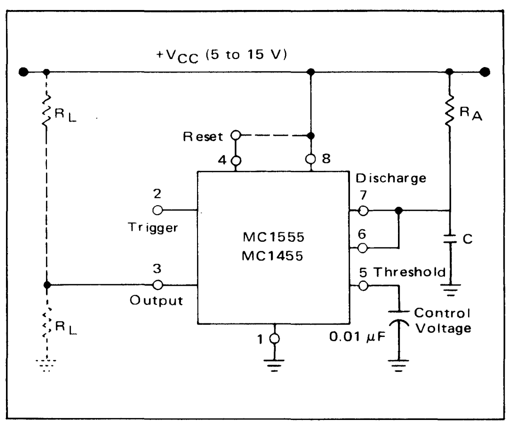
The MC1555 is a monolithic timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

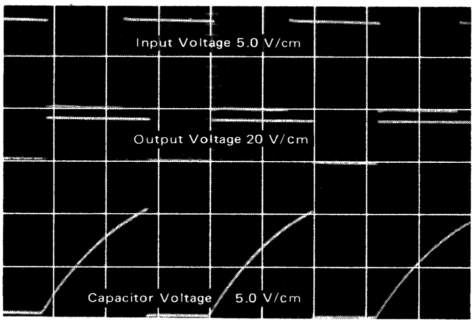
FIGURE 14 – MONOSTABLE CIRCUIT



8

GENERAL OPERATION (continued)

FIGURE 15 – MONOSTABLE WAVEFORMS



t = 50 μs/cm
(R_A = 10 kΩ, C = 0.01 μF, R_L = 1.0 kΩ, V_{CC} = 15 V)

FIGURE 16 – TIME DELAY

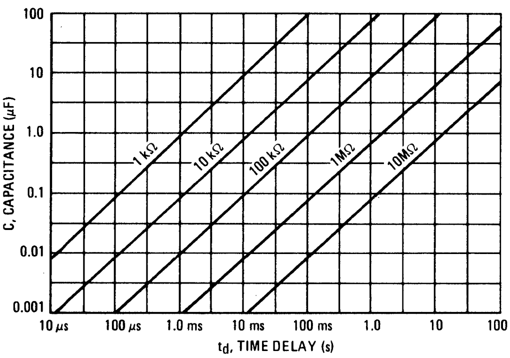


FIGURE 17 – ASTABLE CIRCUIT

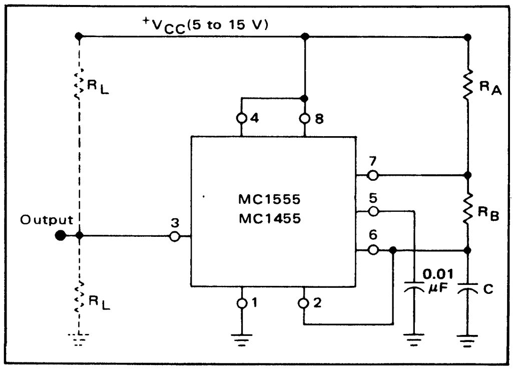
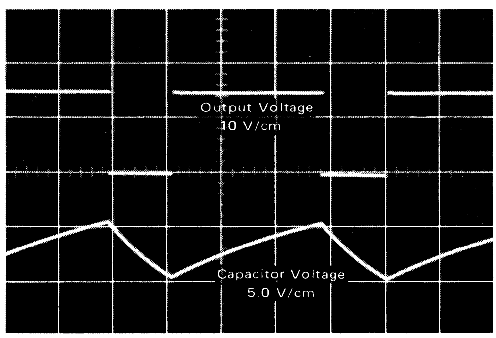


FIGURE 18 – ASTABLE WAVEFORMS



t = 20 μs/cm

(R_A = 5.1 kΩ, C = 0.01 μF, R_L = 1.0 kΩ;
R_B = 3.9 kΩ, V_{CC} = 15 V)

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695\,(R_A+R_B)\,C$

The discharge time (output low) by: $t_2 = 0.695\,(R_B)\,C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695\,(R_A+2R_B)\,C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B)\,C}$

and may be easily found as shown in Figure 19.

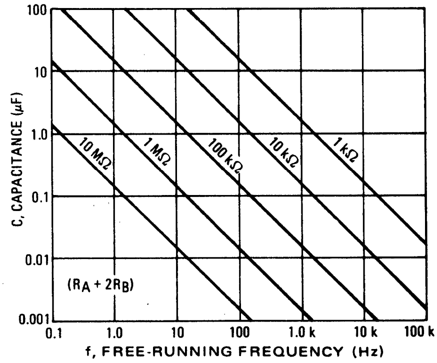
The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geqslant \frac{V_{CC}\ (Vdc)}{I_7\ (A)} \geqslant \frac{V_{CC}\ (Vdc)}{0.2}$$

FIGURE 19 – FREE-RUNNING FREQUENCY



8

APPLICATIONS INFORMATION

Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 to 2/3 V_{CC}. The linear ramp time is given by $t = \frac{2}{3}\frac{V_{CC}}{I}$

where $I = \frac{V_{CC} - V_B - V_{BE}}{R_E}$. If V_B is much larger than V_{BE}, then t can be made independent of V_{CC}.

Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

FIGURE 20 – LINEAR VOLTAGE SWEEP CIRCUIT

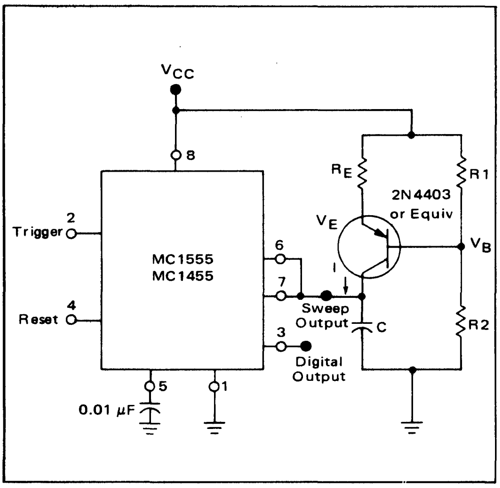


FIGURE 22

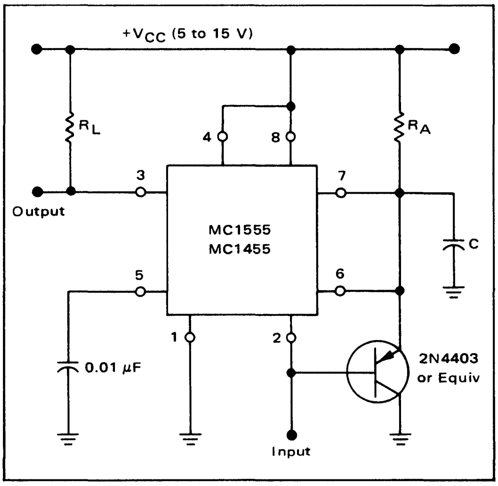
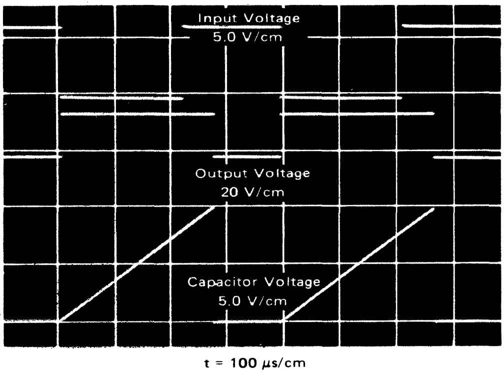
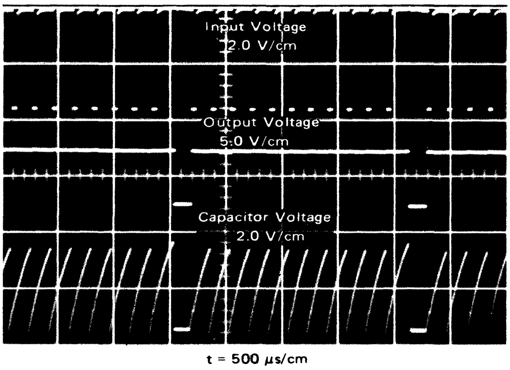


FIGURE 21 – LINEAR VOLTAGE RAMP WAVEFORMS
(R_E = 10 kΩ, R2 = 100 kΩ, R1 = 39 kΩ, C = 0.01 µF, V_{CC} = 15 V)



t = 100 µs/cm

FIGURE 23 – MISSING PULSE DETECTOR WAVEFORMS
(R_A = 2.0 kΩ, R_L = 1.0 kΩ, C = 0.1 µF, V_{CC} = 15 V)



t = 500 µs/cm

8

APPLICATIONS INFORMATION (continued)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 24

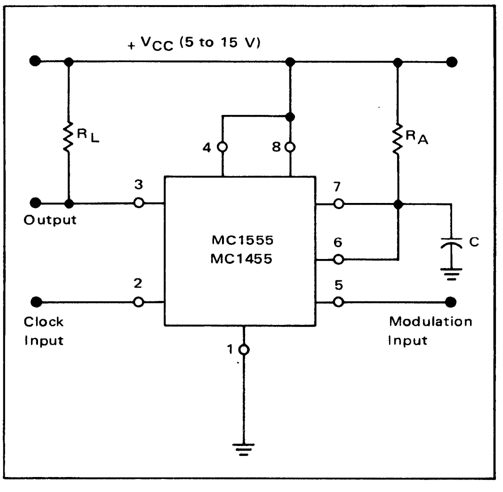
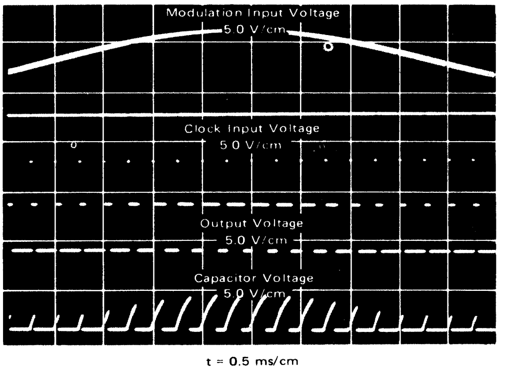


FIGURE 25 – PULSE WIDTH MODULATION WAVEFORMS (R_A = 10 kΩ, C = 0.02 μF, V_{CC} = 15 V)

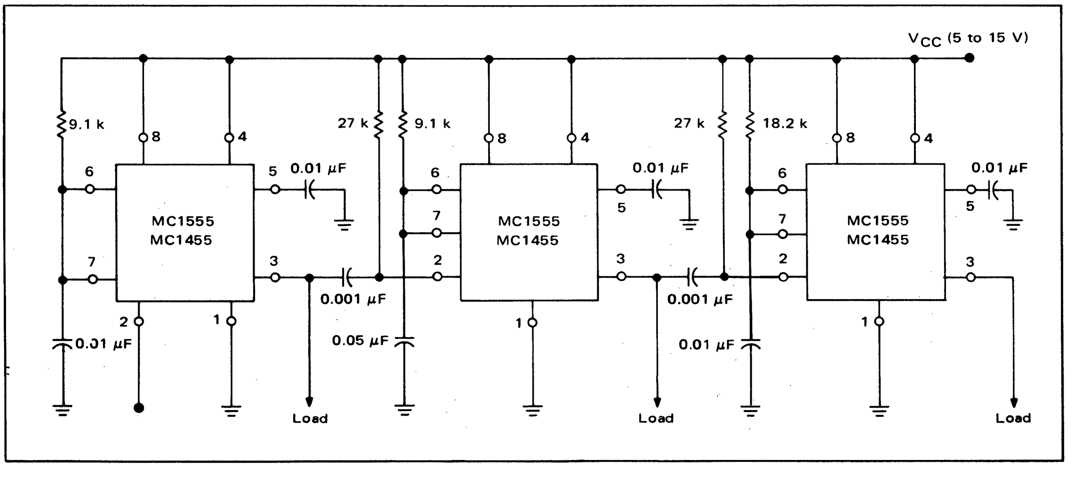


t = 0.5 ms/cm

Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 26



MC1556G
MC1456G
MC1456CG

OPERATIONAL AMPLIFIERS

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

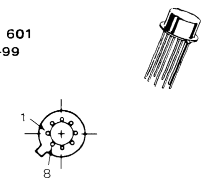
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information, see Application Note AN-522.

- Low Input Bias Current – 15 nA max
- Low Input Offset Current – 2.0 nA max
- Low Input Offset Voltage – 4.0 mV max
- Fast Slew Rate – 2.5 V/µs typ
- Large Power Bandwidth – 40 kHz typ
- Low Power Consumption – 45 mW max
- Offset Voltage Null Capability
- Output Short-Circuit Protection
- Input Over-Voltage Protection

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

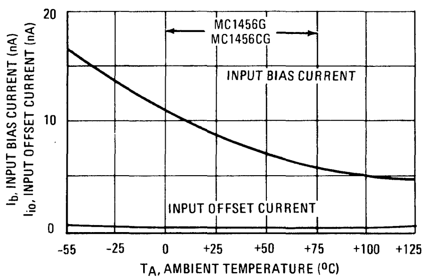
EPITAXIAL PASSIVATED

CASE 601
TO-99



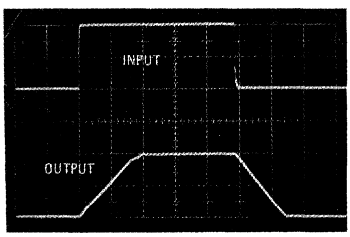
(bottom view)

TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT versus TEMPERATURE for MC1556G



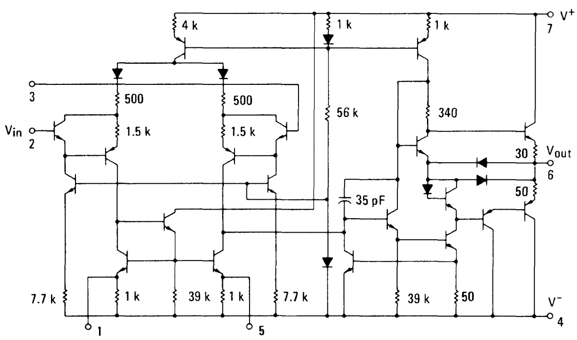
VOLTAGE-FOLLOWER PULSE RESPONSE

5 VOLTS/DIVISION

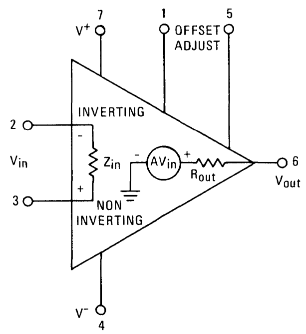


2 µs/DIVISION

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1556G	MC1456G MC1456CG	Unit
Power Supply Voltage	V^+ V^-	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{in}	$\pm V^+$		Volts
Common-Mode Input Swing	CMV_{in}	$\pm V^+$		Volts
Load Current	I_L	20		mA
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Fig.	Symbol	MC1556G Min	MC1556G Typ	MC1556G Max	MC1456G Min	MC1456G Typ	MC1456G Max	MC1456CG Min	MC1456CG Typ	MC1456CG Max	Unit
Input Bias Current		I_b										nAdc
T_A = +25°C			–	8.0	15	–	15	30	–	15	90	
T_A = T_{low} to T_{high} (See Note 1)			–	–	30	–	–	40	–	–	–	
Input Offset Current		$\vert I_{io}\vert$										nAdc
T_A = +25°C			–	1.0	2.0	–	5.0	10	–	5.0	30	
T_A = +25°C to T_{high}			–	–	3.0	–	–	14	–	–	–	
T_A = T_{low} to +25°C			–	–	5.0	–	–	14	–	–	–	
Input Offset Voltage		$\vert V_{io}\vert$										mVdc
T_A = +25°C			–	2.0	4.0	–	5.0	10	–	5.0	12	
T_A = T_{low} to T_{high}			–	–	6.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f = 20 Hz)												
Parallel Input Resistance		R_p	–	5.0	–	–	3.0	–	–	3.0	–	Megohms
Parallel Input Capacitance		C_p	–	6.0	–	–	6.0	–	–	6.0	–	pF
Common-Mode Input Impedance (f = 20 Hz)		Z_{in}	–	250	–	–	250	–	–	250	–	Megohms
Common-Mode Input Voltage Swing	1	CMV_{in}	±12	±13	–	±11	±12	–	±10.5	±12	–	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	2	e_n	–	45	–		45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	3	CM_{rej}	80	110	–	70	110	–	–	110	–	dB
Open-Loop Voltage Gain, (V_{out} = ±10 V, R_L = 2.0 k ohms)	4,5,6	A_{VOL}										V/V
T_A = +25°C			100,000	200,000	–	70,000	100,000	–	25,000	100,000	–	
T_A = T_{low} to T_{high}			40,000	–	–	40,000	–	–	–	–	–	
Power Bandwidth (A_V = 1, R_L = 2.0 k ohms, THD≤5%, V_{out} = 20 Vp-p)	9	P_{BW}	–	40	–	–	40	–		40	–	kHz
Unity Gain Crossover Frequency (open-loop)	5	f_c	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)	5,7		–	70	–	–	70	–	–	70	–	degrees
Gain Margin	5,7		–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)		dV_{out}/dt	–	2.5	–	–	2.5	–	–	2.5	–	V/µs
Output Impedance (f = 20 Hz)		Z_{out}	–	1.0	2.0	–	1.0	2.5	–	1.0	–	kohms
Short-Circuit Output Current	8	I_{SC}	–	-17, +9.0	–	–	-17, +9.0	–	–	-17, +9.0	–	mAdc
Output Voltage Swing (R_L = 2.0 k ohms)	10	V_{out}	±12	±13	–	±11	±12	–	±10	±12	–	V_{pk}
Power Supply Sensitivity												µV/V
V^- = constant, $R_s \le$ 10 k ohms		S+		50	100	–	75	200	–	75	–	
V^+ = constant, $R_s \le$ 10 k ohms		S–		50	100	–	75	200	–	75	–	
Power Supply Current		I_D+	–	1.0	1.5	–	1.3	3.0	–	1.3	4.0	mAdc
		I_D-	–	1.0	1.5	–	1.3	3.0	–	1.3	4.0	
DC Quiescent Power Dissipation (V_{out} = 0)	11	P_D	–	30	45	–	40	90	–	40	120	mW

Note 1: T_{low}: 0° for MC1456G and MC1456CG
-55°C for MC1556G

T_{high}: +75°C for MC1456G and MC1456CG
+125°C for MC1556G

8

TYPICAL CHARACTERISTICS

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 1 – INPUT COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

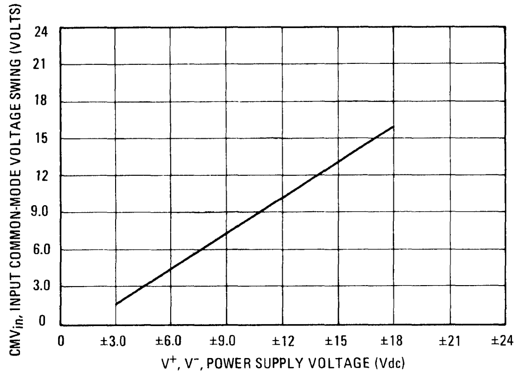


FIGURE 2 – SPECTRAL NOISE DENSITY

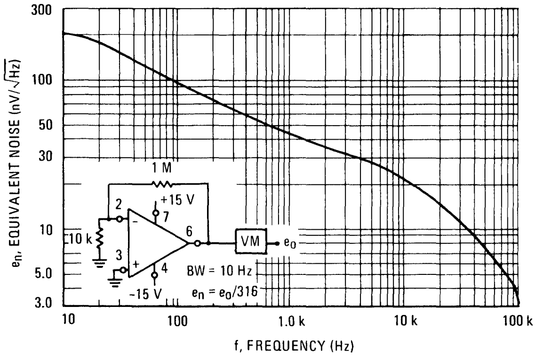


FIGURE 3 – COMMON-MODE REJECTION RATIO versus FREQUENCY

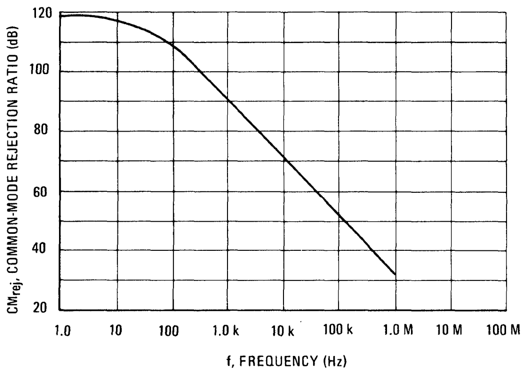


FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

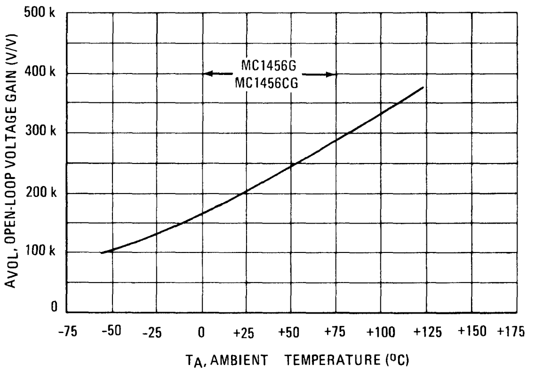


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

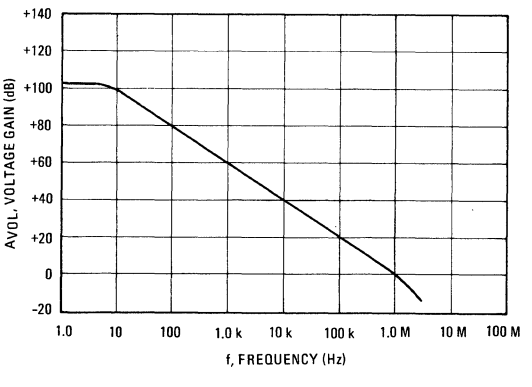
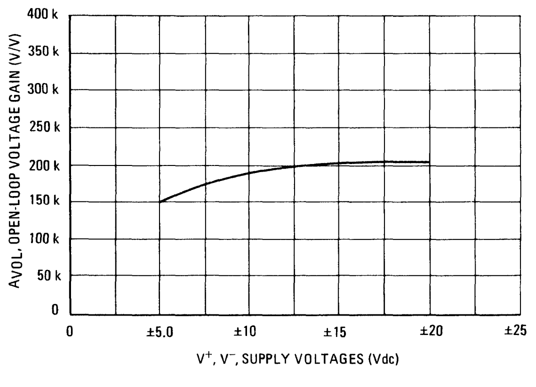


FIGURE 6 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGES



8

TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OPEN-LOOP PHASE SHIFT

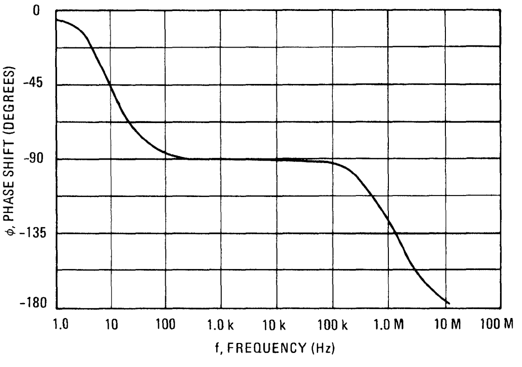


FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

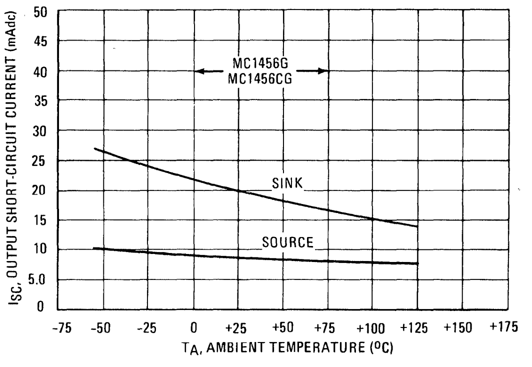


FIGURE 9 – POWER BANDWIDTH

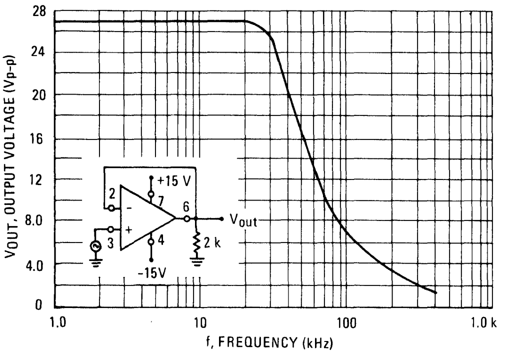


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

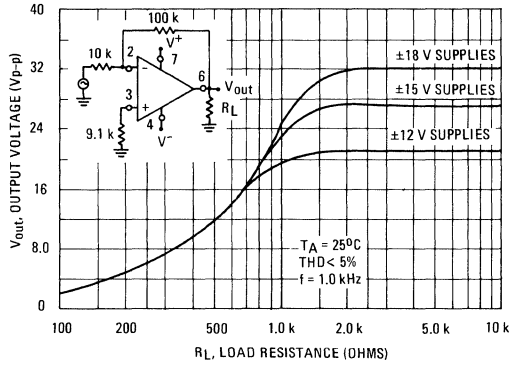
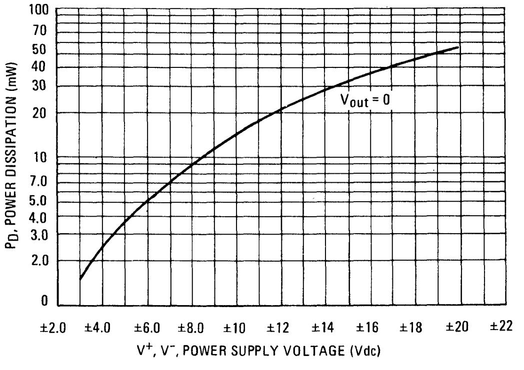


FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



8

TYPICAL APPLICATIONS

Where values are not given for external components they must be selected by the designer to fit the requirements of the system.

FIGURE 12 — INVERTING FEEDBACK MODEL

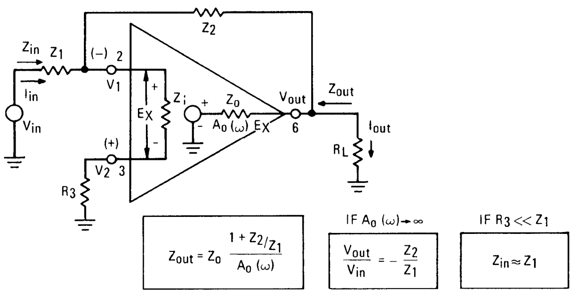


FIGURE 13 — NON-INVERTING FEEDBACK MODEL

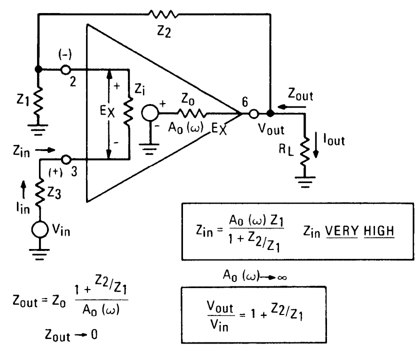


FIGURE 14 — LOW-DRIFT SAMPLE AND HOLD

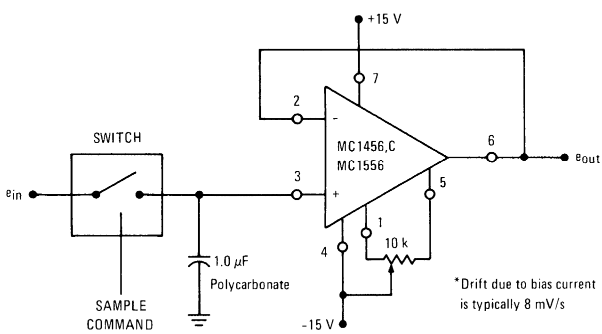
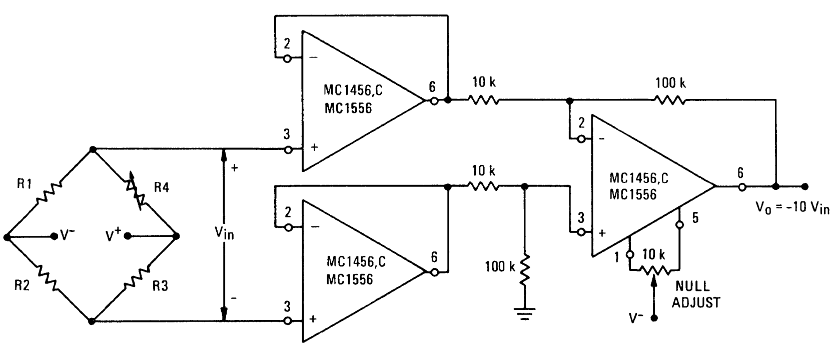
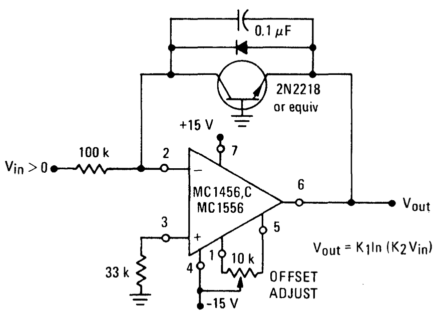


FIGURE 15 — HIGH IMPEDANCE BRIDGE AMPLIFIER



TYPICAL APPLICATIONS (continued)

FIGURE 16 – LOGARITHMIC AMPLIFIER



See Application Note AN-261 for further detail.

FIGURE 17 – VOLTAGE OFFSET NULL CIRCUIT

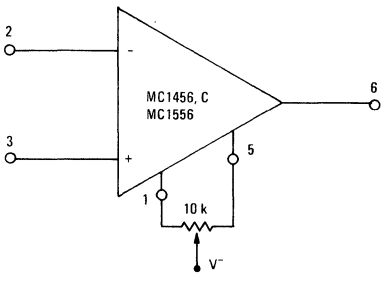
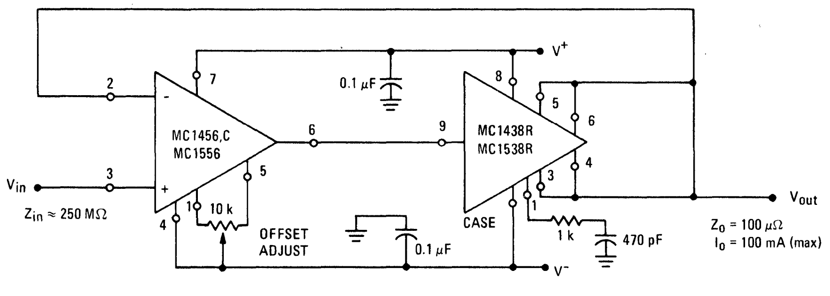


FIGURE 18 – HIGH INPUT IMPEDANCE, HIGH OUTPUT CURRENT VOLTAGE FOLLOWER



8

MC1558
MC1458
MC1458C

OPERATIONAL AMPLIFIERS

DUAL MC1741
INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

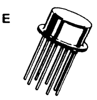
- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

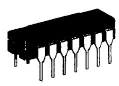
(DUAL MC1741)

DUAL OPERATIONAL AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT

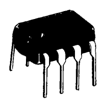
G SUFFIX
METAL PACKAGE
CASE 601



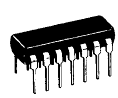


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
MC1458,C (only)



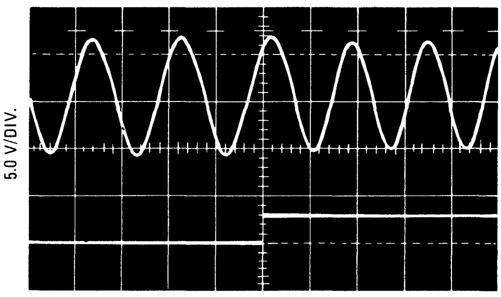
P2 SUFFIX
PLASTIC PACKAGE
CASE 646
MC1458,C (only)

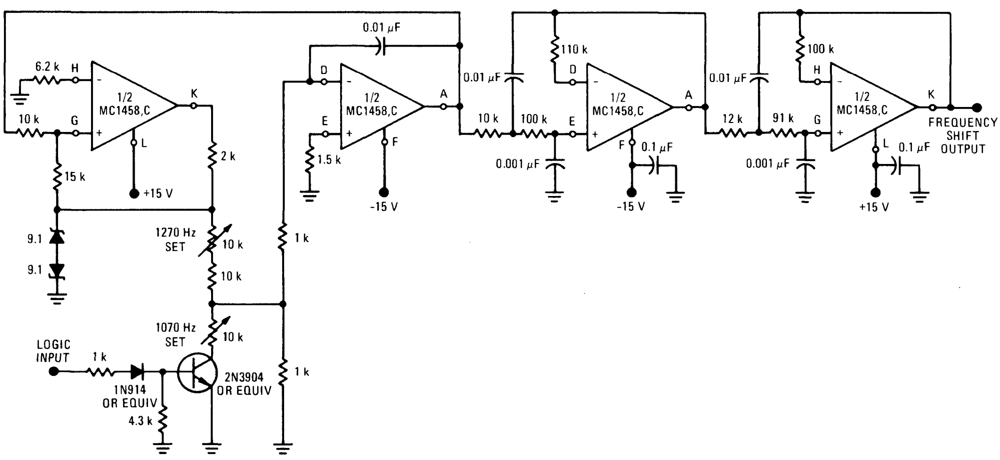


PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	I	J	K	L
G & P1 Packages	1	–	–	2	3	4	5	6	–	–	7	8
L & P2 Packages	2	3	4	5	6	7	8	9	10	11	12	14

FIGURE 1 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR





See Packaging Information Section for outline dimensions.

See current MCCF1558/1458 data sheet for flip-chip information.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1558	MC1458,C	Unit
Power Supply Voltage	V^+ V^-	+22 -22	+18 -18	Vdc
Differential Input Signal ①	V_{in}	±30		Volts
Common-Mode Input Swing ②	CMV_{in}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation)	P_D			
Metal Can		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Plastic Dual In-Line Packages		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Ceramic Dual In-Line Package		750		mW/°C
Derate above T_A = +25°C		6.0		mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

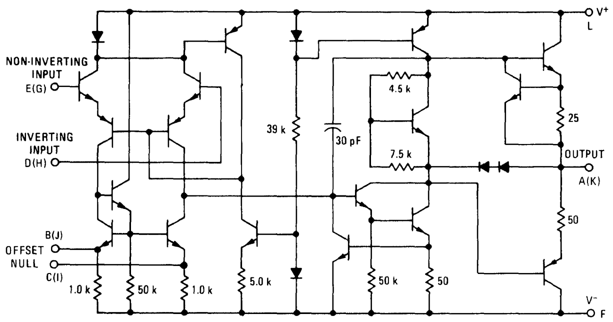
ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_b										µAdc
T_A = +25°C		–	0.2	0.5	–	0.2	0.5	–	0.2	0.7	
$T_A = T_{low}$ to T_{high} ③		–	–	1.5	–	–	0.8	–	–	1.0	
Input Offset Current	$\|I_{io}\|$										µAdc
T_A = +25°C		–	0.03	0.2	–	0.03	0.2	–	0.03	0.3	
$T_A = T_{low}$ to T_{high}		–	–	0.5	–	–	0.3	–	–	0.4	
Input Offset Voltage ($R_S \le 10$ k Ω)	$\|V_{io}\|$										mVdc
T_A = +25°C		–	1.0	5.0	–	2.0	6.0	–	2.0	10	
$T_A = T_{low}$ to T_{high}		–	–	6.0	–	–	7.5	–	–	12	
Differential Input Impedance (Open-Loop, f = 20 Hz)											
Parallel Input Resistance	R_p	0.3	1.0	–	0.3	1.0	–	–	1.0	–	Megohm
Parallel Input Capacitance	C_p	–	6.0	–	–	6.0	–	–	6.0	–	pF
Common-Mode Input Impedance (f = 20 Hz)	$Z_{(in)}$	–	200	–	–	200	–	–	200	–	Megohms
Common-Mode Input Voltage Swing	CMV_{in}	±12	±13	–	±12	±13	–	±11	±13	–	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	e_n	–	45	–	–	45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	70	90	–	70	90	–	60	90	–	dB
Open-Loop Voltage Gain	A_{VOL}										V/V
T_A = +25°C (V_O = ±10 V, R_L = 2.0 k ohms)		50,000	200,000	–	20,000	100,000	–	–	–	–	
$T_A = T_{low}$ to T_{high} (V_O = ±10 V, R_L = 2.0 k ohms)		25,000	–	–	15,000	–	–	–	–	–	
T_A = +25°C (V_O = ±10 V, R_L = 10 k ohms)		–	–	–	–	–	–	20,000	100,000	–	
$T_A = T_{low}$ to T_{high} (V_O = ±10 V, R_L = 10 k ohms)		–	–	–	–	–	–	15,000	–	–	
Power Bandwidth (A_V = 1, R_L = 2.0 k ohms, THD≤5%, V_o = 20 V p-p)	P_{BW}	–	14	–	–	14	–	–	14	–	kHz
Unity Gain Crossover Frequency (open-loop)	f_c	–	1.1	–	–	1.1	–	–	1.1	–	MHz
Phase Margin (open-loop, unity gain)		–	65	–	–	65	–	–	65	–	degrees
Gain Margin		–	11	–	–	11	–	–	11	–	dB
Slew Rate (Unity Gain)	dV_{out}/dt	–	0.8	–	–	0.8	–	–	0.8	–	V/µs
Output Impedance (f = 20 Hz)	Z_{out}	–	75	–	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{SC}	–	20	–	–	20	–	–	20	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_o	±12	±14	–	±12	±14	–	±11	±14	–	Vpk
R_L = 2 k ohms ($T_A = T_{low}$ to t_{high})		±10	±13	–	±10	±13	–	±9.0	±13	–	
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 ohms, $T_A = T_{low}$ to T_{high})	$\|TCV_{io}\|$	–	15	–	–	15	–	–	15	–	µV/°C
Power Supply Sensitivity											µV/V
V^- = constant, $R_s \le 10$ k ohms	S+	–	30	150	–	30	150	–	30	–	
V^+ = constant, $R_s \le 10$ k ohms	S-	–	30	150	–	30	150	–	30	–	
Power Supply Current	I_D^+	–	2.3	5.0	–	2.3	5.6	–	2.3	8.0	mAdc
	I_D^-	–	2.3	5.0	–	2.3	5.6	–	2.3	8.0	
DC Quiescent Power Dissipation (V_O = 0)	P_D	–	70	150	–	70	170	–	70	240	mW

① For supply voltages of less than ±15 V, the maximum differential input voltage is equal to $\pm(V^+ + |V^-|)$.
② For supply voltages of less than ±15 V, the maximum input voltage is equal to the supply voltage $(+V^+, -|V^-|)$.
③ T_{low}: 0°C for MC1458,C; -55°C for MC1558. T_{high}: +75°C for MC1458,C; +125°C for MC1558

8

FIGURE 2 – CIRCUIT SCHEMATIC

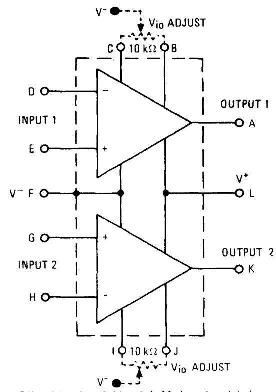


The letters without parenthesis represent the pin numbers for 1/2 of the dual circuit, letters in parenthesis represent the pin numbers for the other half.

PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	I	J	K	L
G & P1 Packages	1	–	–	2	3	4	5	6	–	–	7	8
L & P2 Packages	2	3	4	5	6	7	8	9	10	11	12	14

FIGURE 3 – EQUIVALENT CIRCUIT WITH OFFSET ADJUST



Offset Adjust is available only in 14-pin packaged devices.

TYPICAL CHARACTERISTICS

(V^+ = +15 Vdc, V^- = –15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE

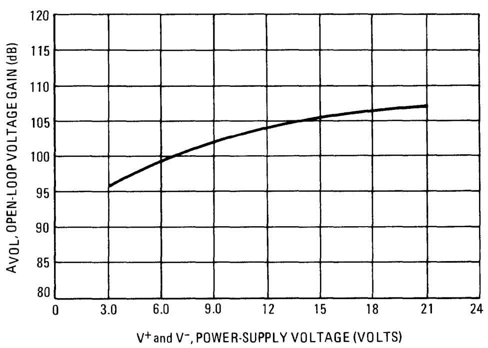


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

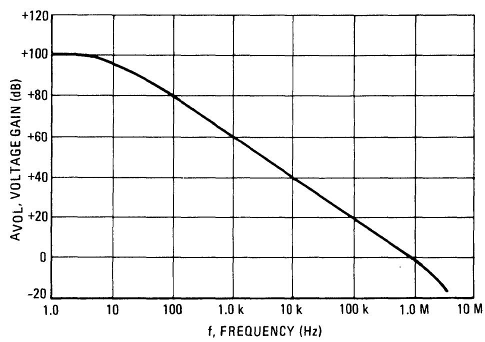


FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

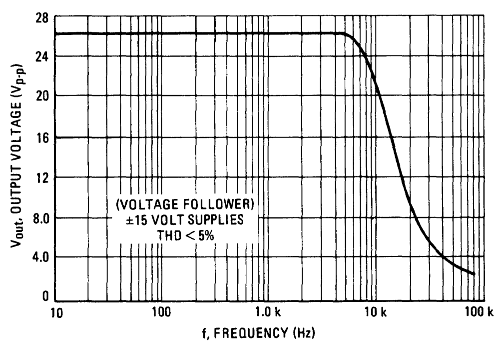
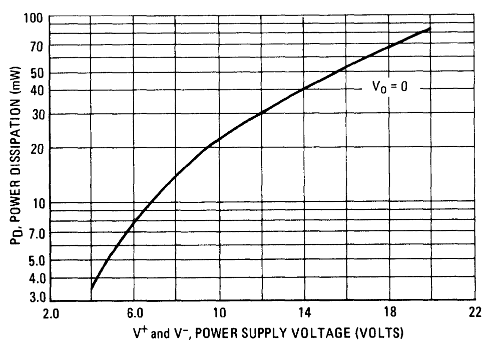


FIGURE 7 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 8 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

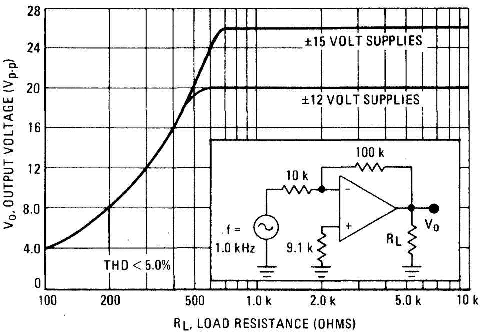


FIGURE 9 – OUTPUT NOISE versus SOURCE RESISTANCE

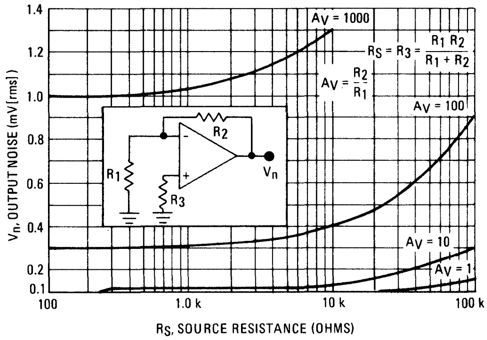
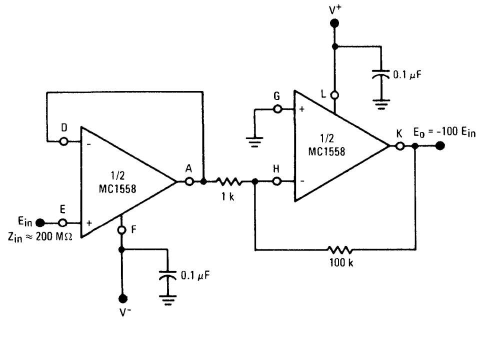


FIGURE 10 – HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER



MC1560, MC1561
MC1460, MC1461

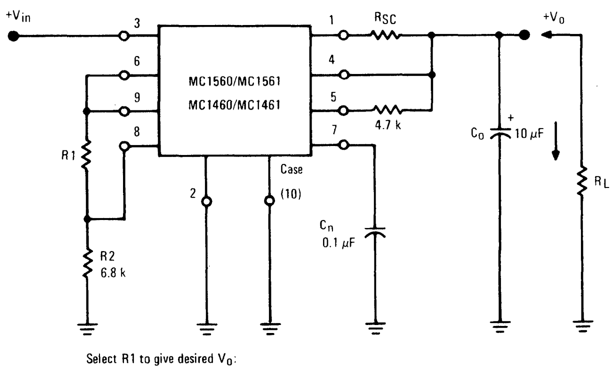
POSITIVE VOLTAGE REGULATORS

MONOLITHIC VOLTAGE REGULATOR

. . . designed to deliver continuous load current up to 500 mA without use of an external power transistor.

- Electronic "Shut-Down" Control and Short-Circuit Protection
- Excellent Load Regulation (Low Output Impedance = 20 milliohms typ from dc to 100 kHz)
- High Power Capability: To 17.5 Watts
- Excellent Transient Response and Temperature Stability
- High Ripple Rejection = 0.002 %/V typ
- Single External Transistor Can Boost Load Current to Greater than 10 Amperes
- Input Voltages to 40 Volts (MC1561)

TYPICAL APPLICATION

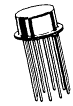


Select R1 to give desired V_O:

$R1 \approx (2\ V_O - 7.0)\ k\Omega$

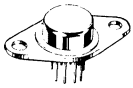
POSITIVE-POWER-SUPPLY VOLTAGE REGULATOR INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED



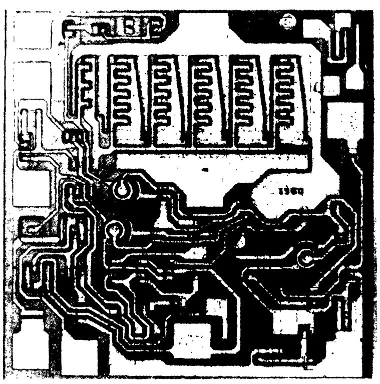
Pin 10 electrically connected to case through substrate.

G SUFFIX
METAL PACKAGE
CASE 602A

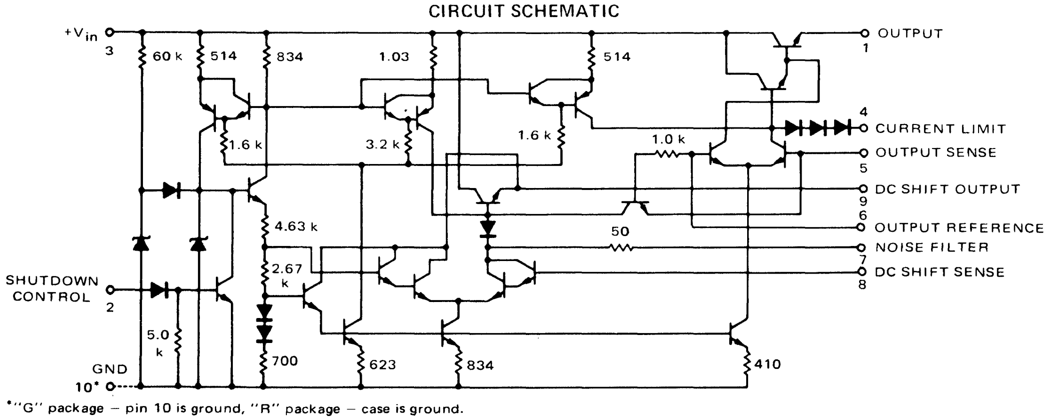


Case is ground terminal

R SUFFIX
METAL PACKAGE
CASE 614



CIRCUIT SCHEMATIC



*"G" package – pin 10 is ground, "R" package – case is ground.

See Packaging Information Section for outline dimensions.

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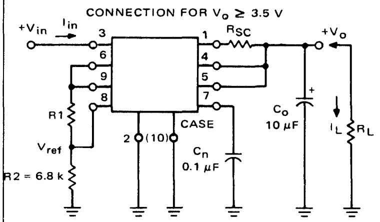
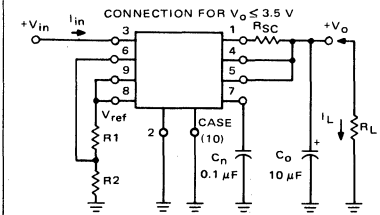
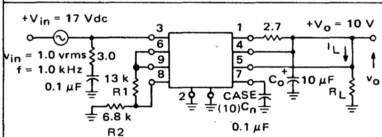
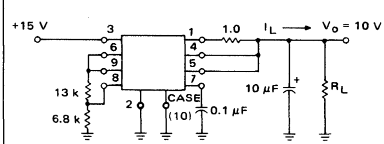
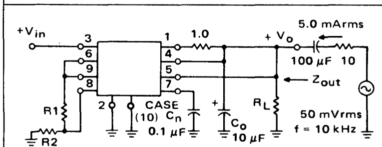
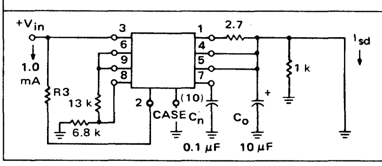
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Load Current = 100 mA for "R" Package device, = 10 mA for "G" Package device, unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic		Symbol	Min	Typ	Max	Units
(R_{SC} = 2.7 ohms unless otherwise noted) CONNECTION FOR $V_o \geq 3.5$ V  Select R1 to give desired V_o: $R1 \approx (2\ V_o - 7)$ kΩ	Input Voltage (See Note 1)		V_{in}				Vdc
	(0 to +75°C)	MC1460		9.0	–	20	
	(-55°C to +125°C)	MC1560		8.5	–	20	
	(0 to +75°C)	MC1461		9.0	–	35	
	(-55°C to +125°C)	MC1561		8.5	–	40	
	Output Voltage Range	MC1460, MC1560	V_o	2.5	–	17	Vdc
		MC1461		2.5	–	32	
		MC1561		2.5	–	37	
	Reference Voltage (V_{in} = 15 V) (Pin 8 to ground)		V_{ref}	3.2	3.5	3.8	Vdc
	Minimum Input-Output Voltage Differential (See Note 2)		V_{in}-V_o				Vdc
	(R_{SC} = 0)	MC1460, MC1461		–	2.1	3.0	
		MC1560, MC1561		–	2.1	2.7	
CONNECTION FOR $V_o \leq 3.5$ V  Select R2 to give desired V_o: $R2 \approx (2\ V_o)$ kΩ; Select R1: $R1 \approx (7.0\ k\Omega - R2)$ kΩ	Bias Current (V_{in} = 15 V) (I_L = 1.0 mAdc, R_2 = 6.8 kΩ, $I_B = I_{in} - I_L$)		I_B				mAdc
		MC1460, MC1461		–	5.0	12	
		MC1560, MC1561		–	4.0	9.0	
	Output Noise (C_n = 0.1 µF, f = 10 Hz to 5.0 MHz)		v_n	–	0.150	–	mV (rms)
	Temperature Coefficient of Output Voltage (See Note 3)		TC_{V_o}				%/°C
	(0 to +75°C)	MC1460, MC1461		–	±0.002	–	
	(-55° to +125°C)	MC1560, MC1561		–	±0.002	–	
	Operating Load Current Range*		I_L				mAdc
	($R_{SC} \leq$ 0.3 ohms) R Package			1.0	–	500	
	($R_{SC} \leq$ 2.0 ohms) G Package			1.0	–	200	
	Input Regulation (% change in output voltage per 1-volt change in input voltage)	MC1460, MC1461	Reg_{in}	–	0.003	0.030	%/V_o
	$Reg_{in} = \frac{v_o\,(rms)\ (100)}{v_{in}\,(rms)\ V_o}$ V_{in} (rms) (See Note 4)	MC1560, MC1561		–	0.002	0.015	
	Load Regulation T_J = Constant (1.0 mA ≤ I_L ≤ 20 mA)	MC1460	Reg_{load}	–	0.5	2.0	mV
		MC1560		–	0.3	1.2	
		MC1461		–	0.7	2.4	
		MC1561		–	0.4	1.6	
	T_C = 25°C (See Note 5) (1.0 mA ≤ I_L ≤ 50 mA)	R Package		–	0.005	0.05	%
		G Package		–	0.01	0.13	
	Output Impedance (See Note 6) (R_{SC} = 1.0 ohms, f = 10 kHz, V_{in} = 14 Vdc)	MC1460	Z_{out}	–	25	100	milli-ohms
		MC1560		–	15	60	
	(I_L = 25 mAdc for G Package)	MC1461		–	35	120	
		MC1561		–	20	80	
	Shutdown Current (V_{in} = 20 Vdc)	MC1460	I_{sd}	–	80	300	µAdc
		MC1560		–	20	50	
	(V_{in} = 35 Vdc)	MC1461		–	140	500	
	$R_3 \approx \frac{V_{in} - 1.4}{1.0\ mA}$	MC1561		–	70	150	

*Operating Load Current is also limited by dc Safe Operating Area (see Figures 15A and 15B). Care must be taken not to exceed the dc Safe Operating Area at any time.

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating		Symbol	Value		Unit
Input Voltage	MC1460, MC1560	V_{in}	20		Vdc
	MC1461		35		
	MC1561		40		
			G Package	R Package	
Load Current		I_L	250	600	mA
Current, Pin 2		$I_{pin\ 2}$	10	10	mA
Current, Pin 9		$I_{pin\ 9}$	5.0	5.0	
Power Dissipation and Thermal Characteristics					
T_A = 25°C		P_D	0.68	3.0	Watts
Derate above T_A = 25°C		$1/\theta_{JA}$	5.44	24	mW/°C
Thermal Resistance, Junction to Air		θ_{JA}	184	41.6	°C/W
T_C = 25°C		P_D	1.8	17.5*	Watts
Derate above T_C = 25°C		$1/\theta_{JC}$	14.4	140	mW/°C
Thermal Resistance, Junction to Case		θ_{JC}	69.4	7.15	°C/W
Operating and Storage Junction Temperature Range		T_J, T_{stg}	-65 to +150		°C

*The MC1460R and MC1560R are limited to 12 watts maximum by the voltage and current maximum ratings.

OPERATING TEMPERATURE RANGE

Ambient Temperature		T_A		°C
	MC1460, MC1461		0 to +75	
	MC1560, MC1561		-55 to +125	

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode. For output voltages greater than approximately 5.5 Vdc the minimum "total instantaneous input voltage" must increase to the extent that it will always exceed the output voltage by at least the "input-output voltage differential".

Note 2. This parameter states that the MC1560/1561 and MC1460/1461 will regulate properly with the input-output voltage differential ($V_{in} - V_o$) as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with ($V_{in} - V_o$) as low as 2.1 Vdc as shown in the typical column.

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$\text{MC1560, MC1561}\quad TCV_o = \frac{\pm (V_o\,max - V_o\,min)(100)}{2\,(180^\circ C)(V_o @ 25^\circ C)} = \%/^\circ C$$

$$\text{MC1460, MC1461}\quad TCV_o = \frac{\pm (V_o\,max - V_o\,min)(100)}{2\,(75^\circ C)(V_o @ 25^\circ C)} = \%/^\circ C$$

The output-voltage adjusting resistors (R1 and R2) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. The input signal can be introduced by use of a transformer which will allow the output of an audio oscillator to be coupled in series with the dc input to the regulator. (The large ac input impedance of the regulator will not load the oscillator.) A 24 V, 1.0 ampere filament transformer with the audio oscillator connected to the 110 V primary winding is satisfactory for this test. $v_{in} \approx 1.0$ V (rms).

Note 5. Load regulation is specified for small ($\leq$ +17°C) changes in junction temperature. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{V_O|_{I_L = 1.0\,mA} - V_O|_{I_L = 50\,mA}}{V_O|_{I_L = 1.0\,mA}} \times 100$$

Note 6. The resulting low level output signal (v_o) will require the use of a tuned voltmeter to obtain a reading. Special care should be used to insure that the measurement technique does not include connection resistance, wire resistance, and wire lead inductance (i.e., measure close to the case). Note that No. 22 AWG hook-up wire has approximately 4.0 milliohms/in. dc resistance and an inductive reactance of approximately 10 milliohms/in. at 100 kHz. Avoid use of alligator clips or banana plug-jack combination.

GENERAL OPERATING INFORMATION

There is a general tendency to consider a voltage regulator as simply a dc circuit and to prepare breadboard construction accordingly. The excellent high-frequency performance and fast response capability of this integrated-circuit regulator, however, makes extra breadboarding care worthwhile when compared with the limited performance achieved in other regulators when low-frequency transistors are used in the feedback amplifier. Due to the use of VHF transistors in the integrated circuit, some VHF care (short, well-dressed leads) must be exercised in the construction and wiring of circuits ("printed-circuit" boards provide an excellent component interconnection technique).

The circuit must be grounded by a low-inductance connection to the case of the "R" package, or to pin 10 of the "G" package.

A series 4.7-kΩ resistor at Pin 5 (Figure 1) will eliminate any VHF instability problems which may result from lead lengths longer than a few inches at the regulator output. The resistor body should be as close to Pin 5 as physically possible (<1/2 inch) although the length of the lead to the load is not critical. If temperature stability is of major concern, a 4.7-kΩ resistor should also be placed in series with Pin 6 in order to cancel any drift due to bias current changes.

8

If long input leads are used, it may be necessary to bypass Pin 3 with a 0.1-μF capacitor (to ground).

The "Shut-Down Control", Pin 2, can be actuated for all possible output voltages and any values of C_o and C_n with no damage to the circuit. The standard logic levels of RTL, DTL, or TTL can be used (see Figure 20). This control can be used to eliminate power consumption by circuit loads which can be put in a "standby" mode, as an ac and dc "squelch" control for communications circuits, and as a dissipation control to protect the regulator under sustained output short-circuiting (see Figures 21 and 25). As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the IC chip, a fixed dc voltage at Pin 2 will cause automatic shut-down for high junction temperatures (see Figure 23, a and b). This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels.

Due to the small value of input current at Pin 8, the external resistors, R1 and R2, can be selected with little regard to their parallel resistance. Further, no match to a diffused-resistor temperature coefficient is required; but R1 and R2 should have the same temperature coefficient to keep their ratio independent of temperature.

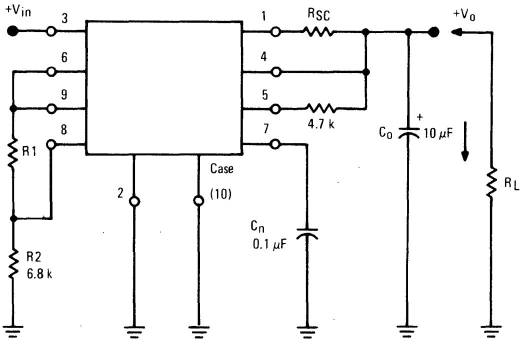
C_n values in excess of 0.1 μF are rarely needed to reduce noise. In cases where more output noise can be tolerated, a smaller capacitor can be used (C_n min. ≈ 0.001 μF).

The connection to Pin 5 can be made by a separate lead directly to the load. Thus "remote sensing" can be achieved and undesired impedances (including that of a milliammeter used to measure I_L) can be greatly reduced in their effect on Z_{out}. A 10-ohm resistor placed from pin 1 to pin 5 (close to the IC) will eliminate undesirable lead-inductance effects.

Short-circuit current-limiting is achieved by selecting a value for R_{SC} which will threshold the internal diode string when the desired maximum load current flows (see Figure 5). If the device dissipation and dc safe area limits (Figure 15) are not exceeded, it can be continuously short-circuited at the output without damage.

TYPICAL CONNECTIONS

FIGURE 1 – CONNECTION FOR $V_o \geq 3.5$ V



Select R1 to give desired V_o: R1 ≈ (2 V_o – 7.0) kΩ

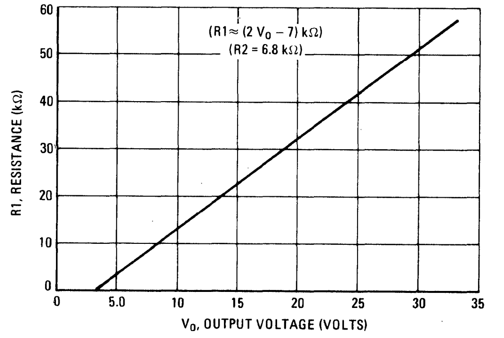
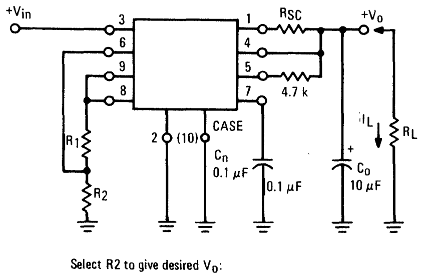
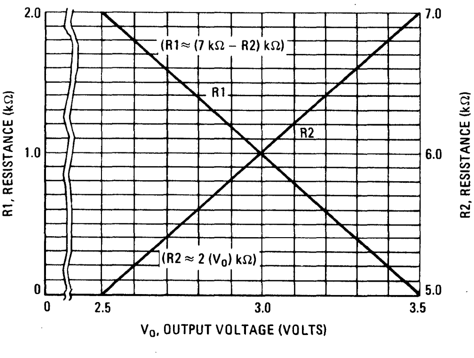


FIGURE 2 – CONNECTIONS FOR $V_o \leq +3.5$ V



Select R2 to give desired V_o:
R2 ≈ (2 V_o) kΩ
Select R1:
R1 ≈ 7.0 kΩ – R2



8

TYPICAL CHARACTERISTICS

Unless otherwise stated: C_n = 0.1 μF, C_o = 10 μF, $V_{o\ nom}$ = +5.0 Vdc, $V_{in\ nom}$ = +9.0 Vdc, T_C = +25°C, I_L > 200 mA for "R" Package only.

FIGURE 3 – INPUT TRANSIENT RESPONSE

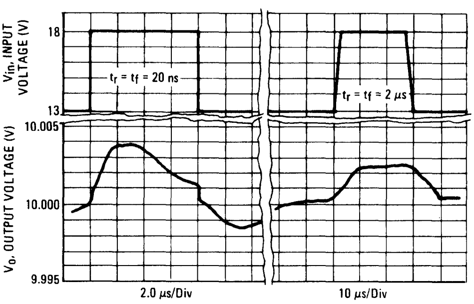


FIGURE 4 – LOAD TRANSIENT RESPONSE

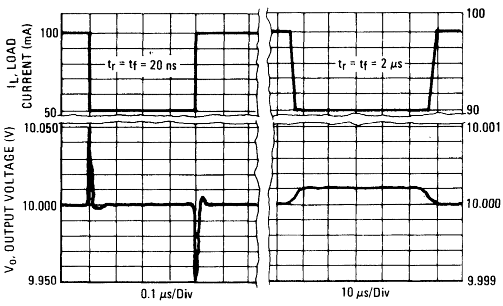


FIGURE 5 – SHORT-CIRCUIT CURRENT versus R_{SC}

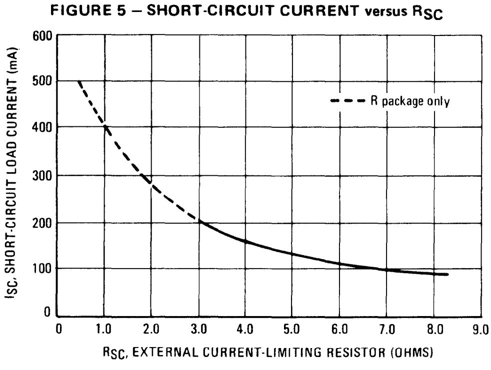


FIGURE 6 – CURRENT-LIMITING CHARACTERISTICS

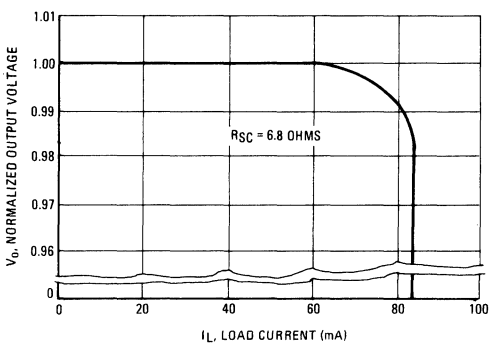


FIGURE 7 – FREQUENCY-DEPENDENCE OF OUTPUT IMPEDANCE

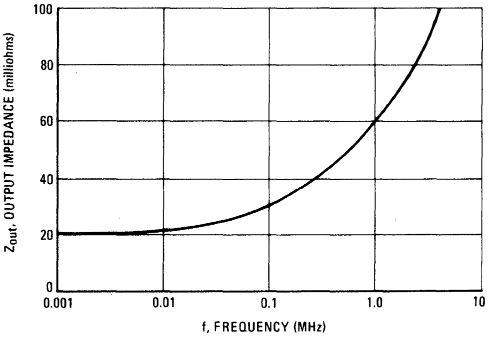
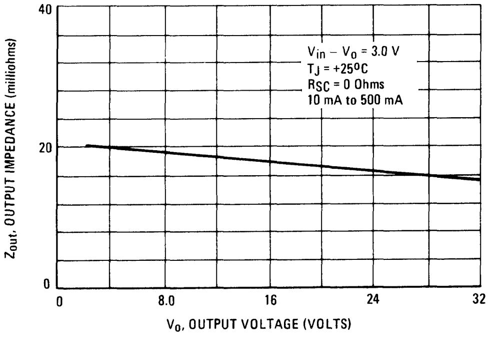


FIGURE 8 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE



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TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated: $C_n = 0.1\ \mu F$, $C_o = 10\ \mu F$, $V_{o\ nom} = +5.0$ Vdc, $V_{in\ nom} = +9.0$ Vdc, $T_C = +25^oC$, $I_L > 200$ mA for "R" Package only.

FIGURE 9 – OUTPUT IMPEDANCE versus R_{SC}

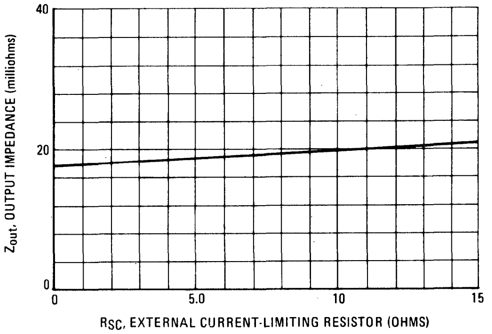


FIGURE 10 – FREQUENCY-DEPENDENCE OF INPUT REGULATION

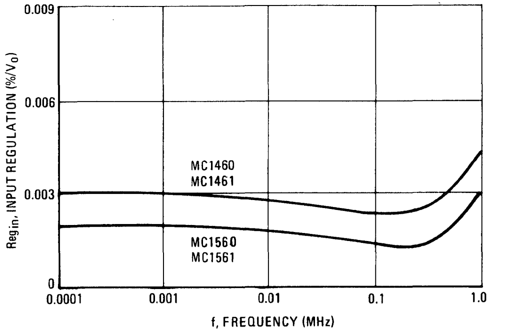


FIGURE 11 – BIAS CURRENT versus INPUT VOLTAGE

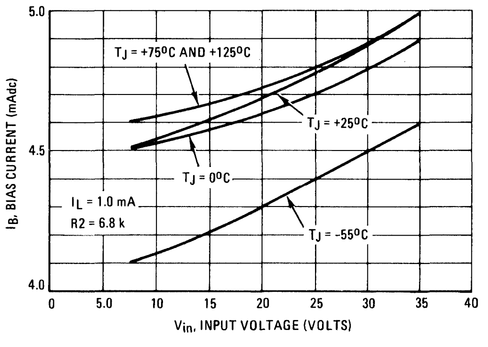


FIGURE 12 – EFFECT OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

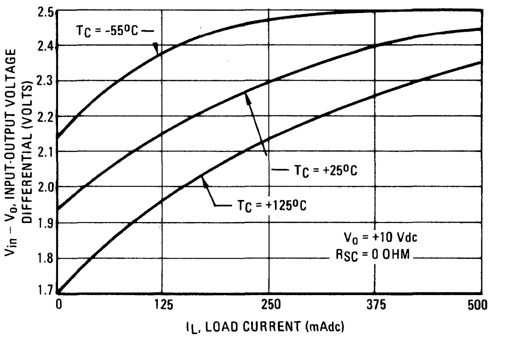


FIGURE 13 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

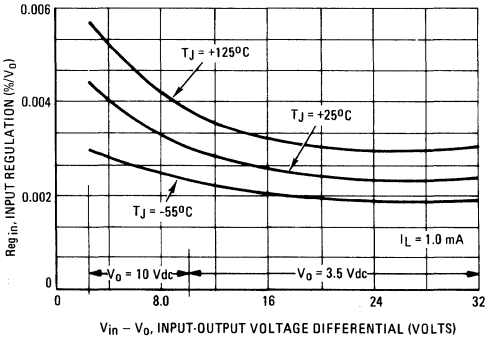
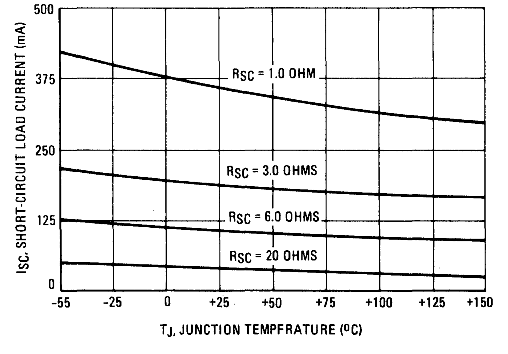


FIGURE 14 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT



TYPICAL CHARACTERISTICS (continued)

FIGURE 15a – DC SAFE OPERATING AREA ("G" PACKAGE)

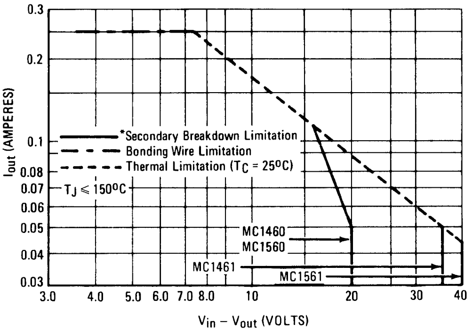
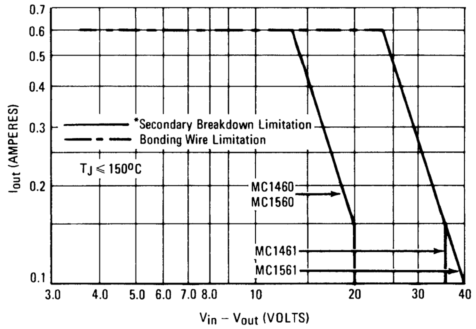


FIGURE 15b – DC SAFE OPERATING AREA ("R" PACKAGE)



*See Application Note AN-415 for an explanation of safe area and second breakdown.

TYPICAL APPLICATIONS

FIGURE 16 – A LABORATORY SUPPLY, 0 TO 25 V

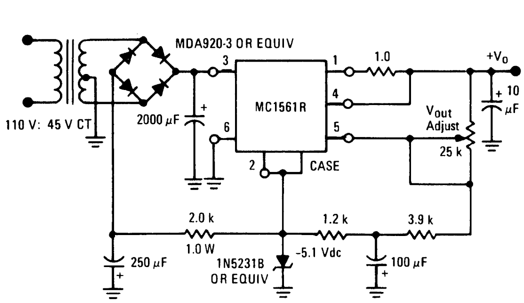


FIGURE 17 – PROVIDING TWO REGULATED OUTPUT VOLTAGES

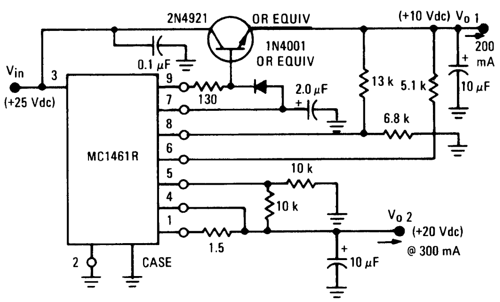
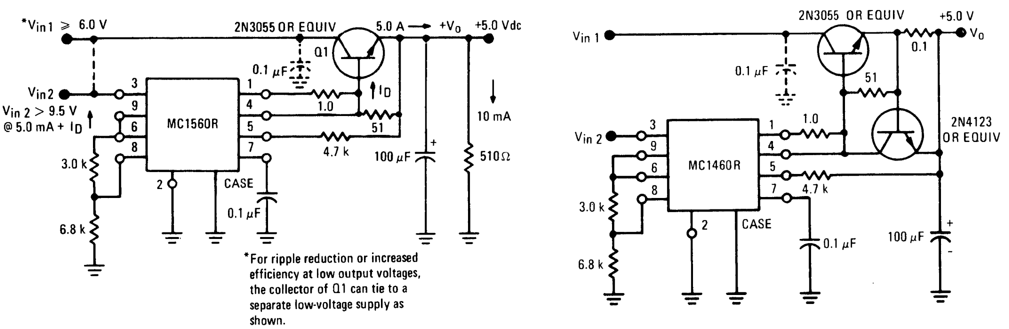


FIGURE 18 – NPN CURRENT BOOST CIRCUITS



*For ripple reduction or increased efficiency at low output voltages, the collector of Q1 can tie to a separate low-voltage supply as shown.

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TYPICAL APPLICATIONS (continued)

FIGURE 19 – PNP CURRENT BOOST CIRCUIT

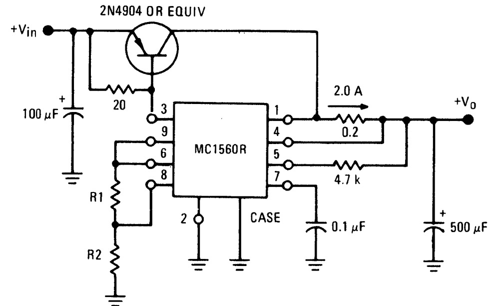
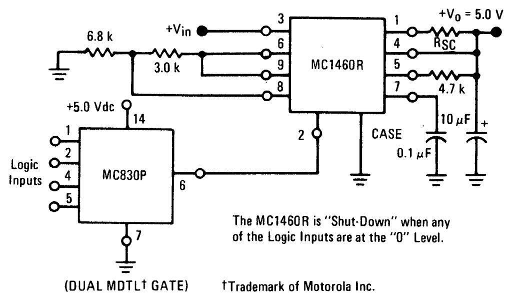


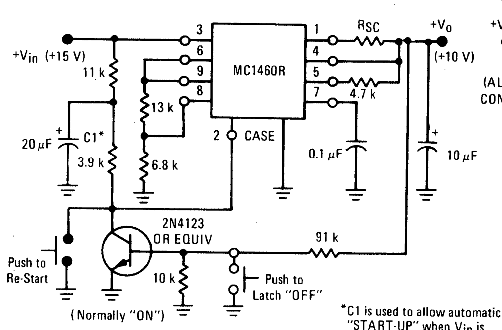
FIGURE 20 – ELECTRONIC SHUT-DOWN USING A MDTL GATE



The MC1460R is "Shut-Down" when any of the Logic Inputs are at the "0" Level.

†Trademark of Motorola Inc.

FIGURE 21 – AUTOMATIC LATCH INTO SHUT-DOWN WHEN OUTPUT IS SHORT-CIRCUITED WITH MANUAL RE-START



*C1 is used to allow automatic "START-UP" when V_{in} is first applied.

FIGURE 22 – SCR "CROWBAR" OVER VOLTAGE PROTECTION

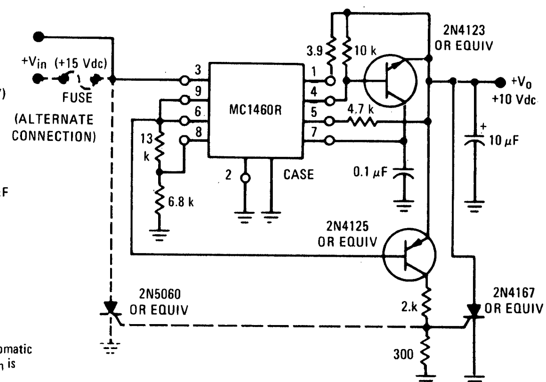


FIGURE 23 – LIMITING MAXIMUM JUNCTION TEMPERATURE

$V_{pin\ 2}$ (for shut-down) $\approx 1.38 - 3.4 \times 10^{-3}\ (T_J - 25^{\circ}C)$

FIGURE a – USING A ZERO TC REFERENCE

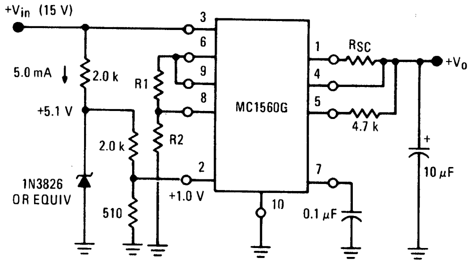
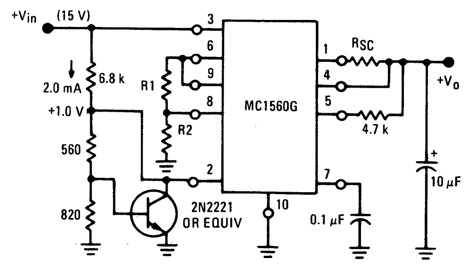


FIGURE b – USING A T_A REFERENCE



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TYPICAL APPLICATIONS (continued)

FIGURE 24 – THERMAL SHUTDOWN WHEN USING EXTERNAL PASS TRANSISTOR

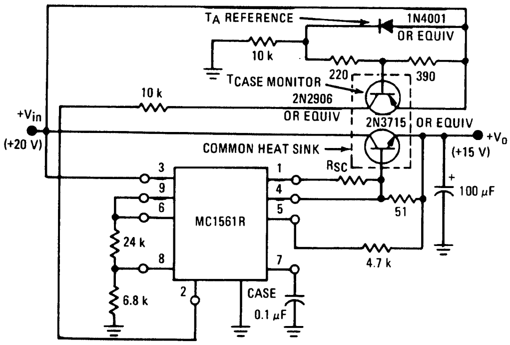


FIGURE 25 – LOW DUTY CYCLE SHORT CIRCUIT PROTECTION WITH AUTOMATIC RESET

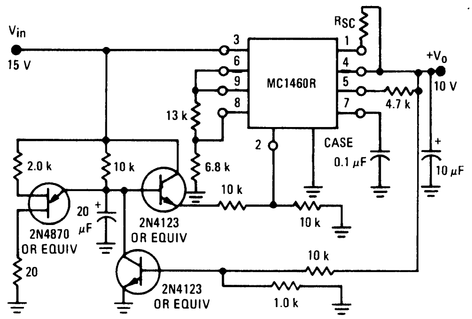


FIGURE 26 – CONNECTION FOR A NEGATIVE OUTPUT VOLTAGE

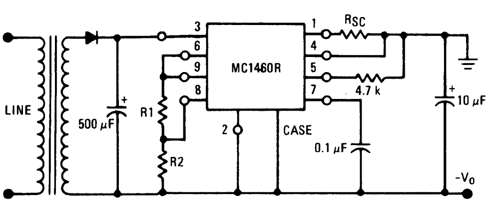


FIGURE 27 – DIGITALLY CONTROLLED 3-TERMINAL NEGATIVE REGULATOR

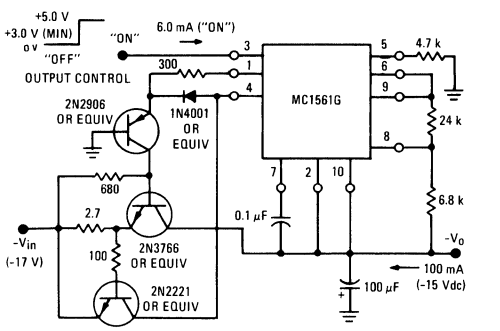
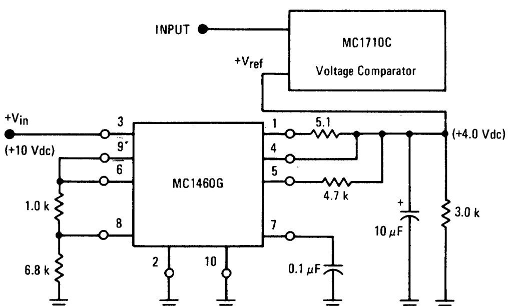


FIGURE 28 – A ZERO TC ADJUSTABLE "ZENER" REFERENCE



GENERAL INFORMATION

Latch-up of these and other regulators can occur if:

1. There are plus and minus voltages available
2. A load exists between Vo^+ and Vo^- (This "common load" may be something inconspicuous –e.g. an operational amplifier. Nearly everyone who uses + and - voltages will have a common load from V^+ to V^-) .
3. $V_{in}{}^+$ and $V_{in}{}^+$ are not applied at the same time.

The above conditions result in one of the two outputs becoming reverse-biased which prevents the regulator from turning "on". Latch-up can be prevented by the circuit configurations shown in Figure 29 and 30.

FIGURE 29

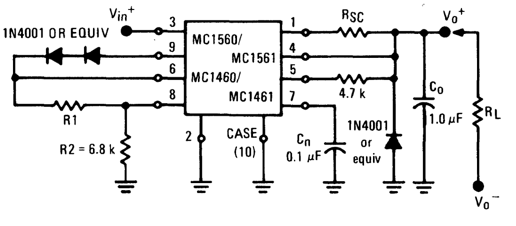
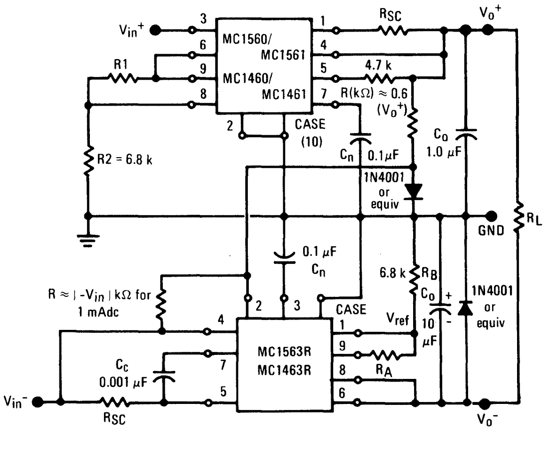


FIGURE 30



VOLTAGE REGULATOR CONSTRUCTION USING THE MC1460, MC1461, MC1560, MC1561 INTEGRATED CIRCUITS

FIGURE 31 – Regulator Layout Using Power Package For Load Currents Up To 500 mA

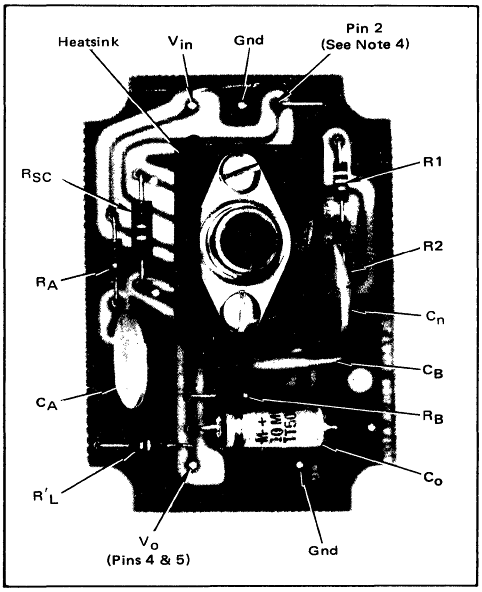
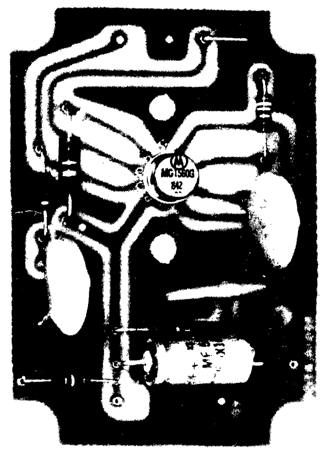


FIGURE 32 – Regulator Layout For Load Currents Up To 200 mA



There is a general tendency to consider a voltage regulator as simply a dc circuit and to prepare circuit layout accordingly. The excellent high-frequency performance and fast response capability of this integrated-circuit regulator, however, makes extra layout care worthwhile. Since short, well-dressed leads must be used, printed-circuit boards provide an excellent component interconnection technique.

The circuit layout, shown in Figure 31 for the "R" or power package IC, applies also to the lower power "G" package circuit shown in Figure 32. The R package circuits will deliver up to 500 mA into a load and the G package, 200 mA.

The circuit schematic, Figure 33, is for output voltages above 3.5 Vdc and the parts list is as follows:

PARTS LIST

Component	Value	Description
R1	Select	1/4 Watt Carbon – See Note 1
R2	6.8 kΩ	1/4 Watt Carbon – See Note 1
R_{SC}	Select	1/2 Watt Carbon – See Note 2
*R_A	3 Ω	1/4 Watt Carbon
*R_B	3 Ω	1/4 Watt Carbon
*R'_L	Select for current of 1 mA minimum	
C_o	10 μF	Sprague 1500 Series, Dickson D10C Series or Equivalent
C_n	0.1 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or Equivalent
*C_A	0.1 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or Equivalent
*C_B	0.1 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or Equivalent
*Heatsink	– Thermalloy #6168 – IERC LB 66B1-77U series	
*Socket	(Not Shown) Robinson Nugent #0001306 Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1	

*Optional Parts, See Note 3 on next page.

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VOLTAGE REGULATOR CONSTRUCTION (continued)

Note 1. The value of R1 is approximately ($2\ V_O$ - 7) kΩ, where V_O is the desired output voltage (3.5 V or greater). Optimum temperature stability can be achieved if R1 and R2 have the same temperature coefficient.

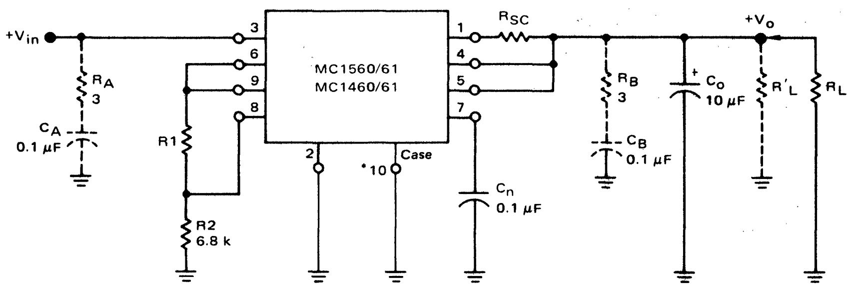
Note 2. R_{SC} is a current sensing resistor for short circuit protection. See Figure 5 for a "Short-Circuit Load Current versus R_{SC}" curve.

Note 3. In cases where long leads are used at the input or output of the regulator, bypass networks R_AC_A and R_BC_B might be necessary to eliminate parasitic oscillation.

With no load, it is possible for a charge to develop on C_O due to leakage currents. R'_L is recommended to insure a minimum load current of 1 mA.

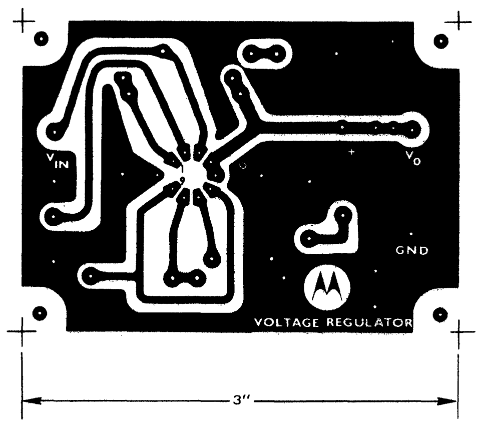
Note 4. It is recommended that Pin 2 (shut-down control) be grounded when not in use. When used, drive current to Pin 2 must be limited to 10 mA maximum.

FIGURE 33 — Schematic of Complete Regulator Showing Both Necessary and Optional Components



*G-Package Pin 10 is ground, R package Case is ground.

FIGURE 34 — Typical Printed Circuit Board Layout



MC1563
MC1463

NEGATIVE VOLTAGE REGULATOR

Specifications and Applications Information

MONOLITHIC NEGATIVE VOLTAGE REGULATOR

The MC1563/MC1463 is a "three terminal" negative regulator designed to deliver continuous load current up to 500 mAdc and provide a maximum negative input voltage of −40 Vdc. Output current capability can be increased to greater than 10 Adc through use of one or more external transistors.

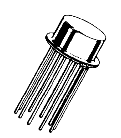
Specifications and performance of the MC1563/MC1463 Negative Voltage Regulator are nearly identical to the MC1569/MC1469 Positive Voltage Regulator. For systems requiring both a positive and negative power supply, these devices are excellent for use as complementary regulators and offer the advantage of operating with a common input ground.

The MC1563R/MC1463R case can be mounted directly to a grounded heat sink which eliminates the need for an insulator.

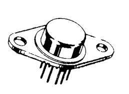
- Case is at Ground Potential (R package)
- Electronic "Shutdown" and Short-Circuit Protection
- Low Output Impedance – 20 Milliohms typical
- High Power Capability – 9.0 Watts
- Excellent Temperature Stability – $TCV_O = \pm 0.002\%/^{\circ}C$ typical
- High Ripple Rejection – 0.002% typical
- 500 mA Current Capability

NEGATIVE-POWER-SUPPLY VOLTAGE REGULATOR INTEGRATED CIRCUIT

SILICON EPITAXIAL PASSIVATED

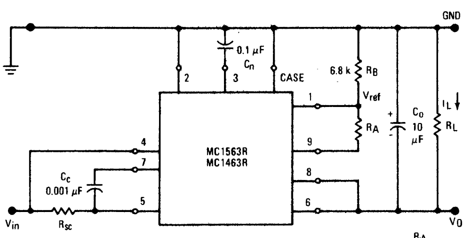


G SUFFIX
METAL PACKAGE
CASE 602A



R SUFFIX
METAL PACKAGE
CASE 614

FIGURE 1 – TYPICAL CIRCUIT CONNECTION
($|-3.5| \leqslant V_O \leqslant |-37|$ Vdc, $1 \leqslant I_L \leqslant 500$ mA)



Select R_A to Give Desired V_O: $R_A \approx (2|V_O| - 7)$ kΩ $\quad V_O \approx -3.5\left(1 + \frac{R_A}{R_B}\right)$

FIGURE 2 – TYPICAL NPN CURRENT BOOST CONNECTION
(V_O = 5.2 Vdc, I_L = 10 Adc [max])

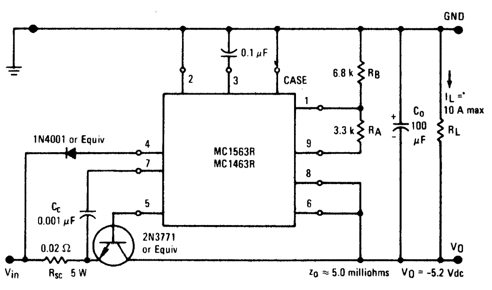
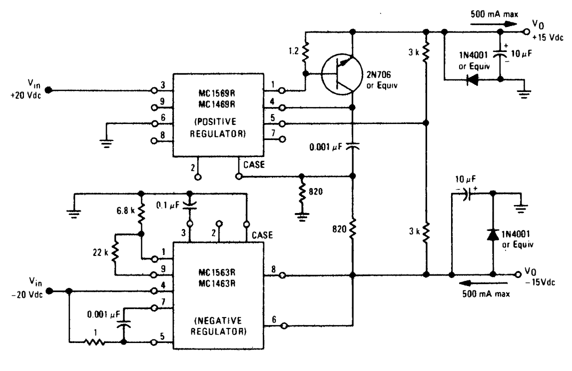
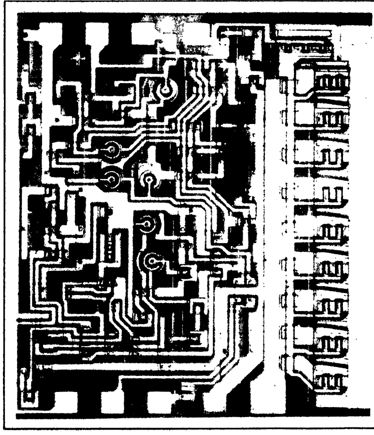


FIGURE 3 – ±15 V, ±400 mA COMPLEMENTARY TRACKING VOLTAGE REGULATOR





See Packaging Information Section for outline dimensions. (MC1563 – Pg. 1)

8

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
Input Voltage	V_{in}			Vdc
MC1463		−35		
MC1563		−40		
		G Package	R Package	
Peak Load Current	I_L pk	250	600	mA
Current, Pin 2	$I_{pin\ 2}$	10	10	mA
Power Dissipation and Thermal Characteristics				
T_A = 25°C	P_D	0.68	2.4	Watts
Derate above T_A = 25°C	$1/\phi_{JA}$	5.44	16	mW/°C
Thermal Resistance, Junction to Air	ϕ_{JA}	184	62	°C/W
T_C = 25°C	P_D	1.8	9.0	Watts
Derate above T_C = 25°C	$1/\phi_{JC}$	14.4	61	mW/°C
Thermal Resistance, Junction to Case	ϕ_{JC}	69.4	17	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175		°C

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1463		0 to +75	
MC1563		-55 to +125	

ELECTRICAL CHARACTERISTICS (I_L = 100 mAdc, T_C = +25°C unless otherwise noted.)

Characteristic	Fig.	Note	Symbol*	MC1563 Min	MC1563 Typ	MC1563 Max	MC1463 Min	MC1463 Typ	MC1463 Max	Unit
Input Voltage (T_A = T_{low} ① to T_{high} ②)	4	1	V_{in}	-8.5	–	-40	-9.0	–	-35	Vdc
Output Voltage Range	4	–	V_O	-3.6	–	-37	-3.8	–	-32	Vdc
Reference Voltage (Pin 1 to Ground)	4	–	V_{ref}	-3.4	-3.5	-3.6	-3.2	-3.5	-3.8	Vdc
Minimum Input-Output Voltage Differential (R_{sc} = 0)	4	2	$\|V_{in} - V_O\|$	–	1.5	2.7	–	1.5	3.0	Vdc
Bias Current (Standby Current) (I_L = 1.0 mAdc, I_B = I_{in} - I_L)	4	–	I_B	–	7.0	11	–	7.0	14	mAdc
Output Noise (C_n = 0.1 µF, f = 10 Hz to 5.0 MHz)	4	–	v_n	–	120	–	–	120	–	µV(rms)
Temperature Coefficient of Output Voltage	4	3	TCV_O	–	±0.002	–	–	±0.002	–	%/°C
Operating Load Current Range	4	–	I_L							mAdc
(R_{sc} = 0.3 ohm) R Package				1.0	–	500	1.0	–	500	
(R_{sc} = 2.0 ohms) G Package				1.0	–	200	1.0	–	200	
Input Regulation	4	4	Reg_{in}	–	0.002	0.015	–	0.003	0.030	%/V_O
Load Regulation	6	5	Reg_L							
(T_J = Constant [1.0 mA ≤ I_L ≤ 20 mA])				–	0.4	1.6	–	0.7	2.4	mV
(T_C = +25°C [1.0 mA ≤ I_L ≤ 50 mA]) R Package				–	0.005	0.05	–	0.005	0.05	%
G Package				–	0.01	0.13	–	0.01	0.13	
Output Impedance (f = 1.0 kHz)	7	–	z_o	–	20	–	–	35	–	milliohms
Shutdown Current (V_{in} = −35 Vdc)	8	–	I_{sd}	–	7.0	15	–	14	50	µAdc

① T_{low} = 0°C for MC1463
= -55°C for MC1563

② T_{high} = +75°C for MC1463
= +125°C for MC1563

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode.

Note 2. This parameter states that the MC1563/MC1463 will regulate properly with the input-output voltage differential $|V_{in} - V_O|$ as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with $|V_{in} - V_O|$ as low as 1.5 Vdc as shown in the typical column.

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min})\ (100)}{\Delta T_A\ (V_O @ T_A = +25^{\circ}C)}$$

where ΔT_A = +180°C for the MC1563
+75°C for the MC1463

The output-voltage adjusting resistors (R_A and R_B) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. Input regulation is the percentage change in output voltage per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{v_o}{V_O\ (v_{in})}\ 100\ (\%/V_O).$$

where v_o is the change in the output voltage V_O for the input change v_{in}.

The following example illustrates how to compute maximum output voltage change for the conditions given:

$$Reg_{in} = 0.015\%/V_O$$
$$V_O = 10 \text{ Vdc}$$
$$v_{in} = 1.0 \text{ V(rms)}$$
$$v_o = \frac{(Reg_{in})(v_{in})(V_O)}{100} = \frac{(0.015)(1.0)(10)}{100} = 0.0015 \text{ V(rms)}$$

Note 5. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{V_O|_{I_L = 1.0\text{ mA}} - V_O|_{I_L = 50\text{ mA}}}{V_O|_{I_L = 1.0\text{ mA}}} \times 100$$

TEST CIRCUITS

(I_L = 100 mAdc, T_C = +25°C unless otherwise noted.)

FIGURE 4 – GENERAL TEST CIRCUIT

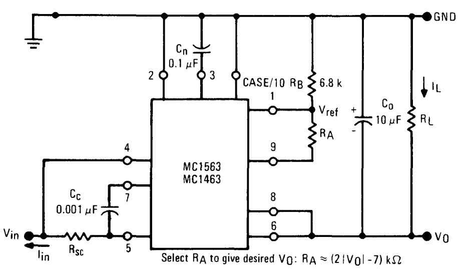


FIGURE 5 – LOAD TRANSIENT RESPONSE

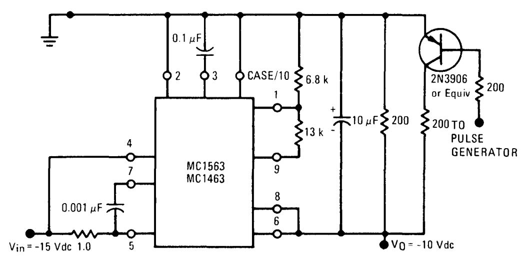


FIGURE 6 – LOAD REGULATION

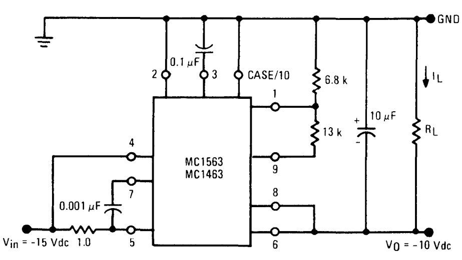


FIGURE 7 – OUTPUT IMPEDANCE

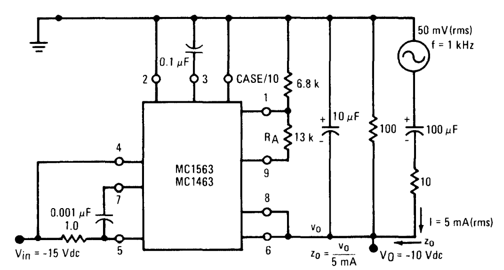
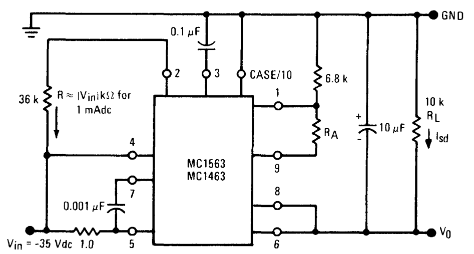


FIGURE 8 – SHUTDOWN CURRENT



(MC1563 – Pg. 3)

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GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
   a) Output Voltage is set by resistors R_A and R_B (see Figure 9). Set R_B = 6.8 k ohms and determine R_A from the graph of Figure 11 or from the equation:

   $$R_A \approx (2\,|V_O| - 7)\ k\Omega$$

   b) Output voltage can be varied by making R_A adjustable as shown in Figures 9 and 10.

   c) Output voltage, V_O, is determined by the ratio of R_A and R_B therefore optimum temperature performance can be achieved if R_A and R_B have the same temperature coefficient.

   d) $V_O = V_{ref}\,(1 + \frac{R_A}{R_B})$; therefore the tolerance on output voltage is determined by the tolerance of V_{ref} and R_A and R_B.

2. Short-Circuit Current, I_{sc}
   Short-Circuit Current, I_{sc} is determined by R_{sc}. R_{sc} may be chosen with the aid of Figure 11 when using the typical circuit connection of Figure 9. See Figure 27 for current limiting during NPN current boost.

3. Compensation, C_c
   A 0.001 μF capacitor (C_c, see Figure 9), will provide adequate compensation in most applications, with or without current boost. Smaller values of C_c will reduce stability and larger values of C_c will degrade pulse response and output impedance versus frequency. The physical location of C_c should be close to the MC1563/MC1463 with short lead lengths.

4. Noise Filter Capacitor, C_n
   A 0.1 μF capacitor, C_n, from pin 3 to ground will typically reduce the output noise voltage to 120 μV(rms). The value of C_n can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of 0.001 μF is recommended.

5. Output Capacitor, C_O
   The value of C_O should be at least 10 μF in order to provide good stability.

6. Shutdown Control
   One method of turning "OFF" the regulator is to draw 1 mA from pin 2 (See Figure 8). This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting. As the magnitude of the input-threshold voltage at pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at pin 2 will cause automatic shutdown for high junction temperatures (see Figure 35). This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard logic levels of MECL, MRTL, MDTL or MTTL* can also be used to turn the regulator "ON" or "OFF" (see Figures 30 and 31).

7. Remote Sensing
   The connection to pin 8 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on z_o can be greatly reduced (see Figure 33).

FIGURE 9 – TYPICAL CIRCUIT CONNECTION

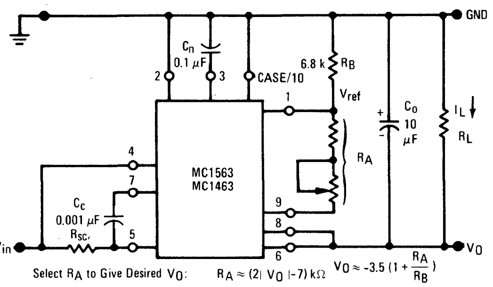


FIGURE 10 – R_A versus V_O

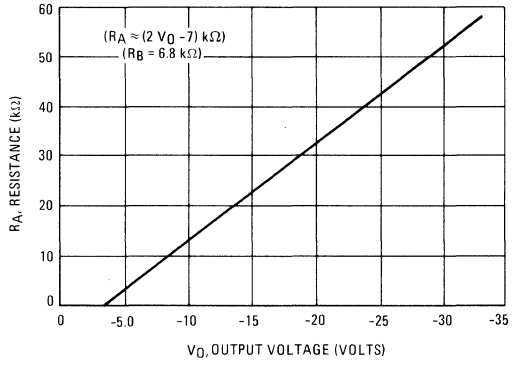
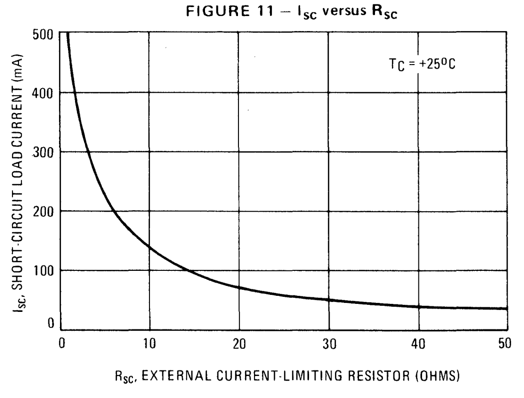


FIGURE 11 – I_{sc} versus R_{sc}



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TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_n = 0.1\,\mu F$, $C_c = 0.001\,\mu F$, $C_O = 10\,\mu F$, $T_C = +25^oC$, $V_{in(nom)} = -15$ Vdc, $V_{O(nom)} = -10$ Vdc, $I_L = 100$ mAdc.

FIGURE 12 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

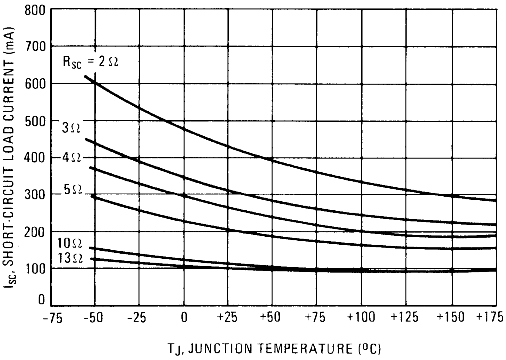


FIGURE 13 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE

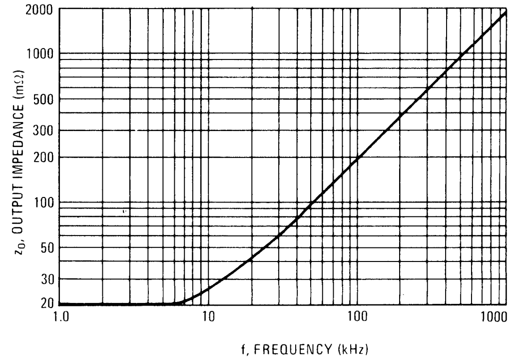


FIGURE 14 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

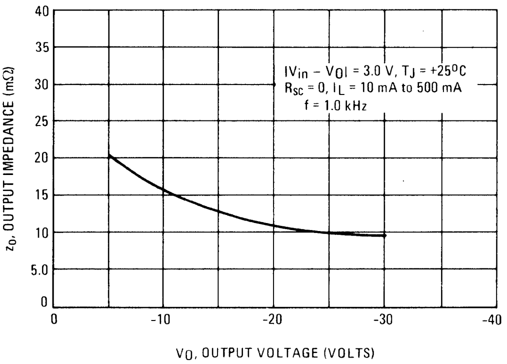


FIGURE 15 – OUTPUT IMPEDANCE versus R_{sc}

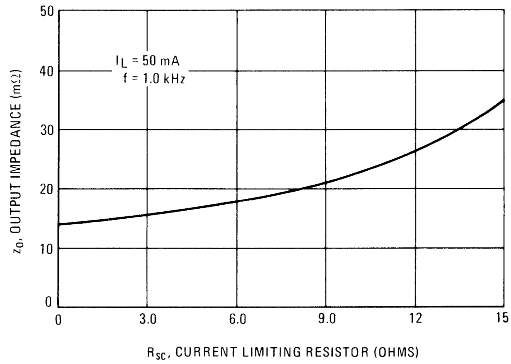
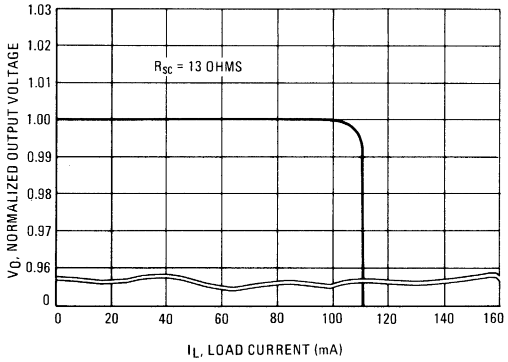


FIGURE 16 – CURRENT LIMITING CHARACTERISTICS



(MC1563 – Pg. 5)

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TYPICAL CHARACTERISTICS (continued)

FIGURE 17 – BIAS CURRENT versus INPUT VOLTAGE

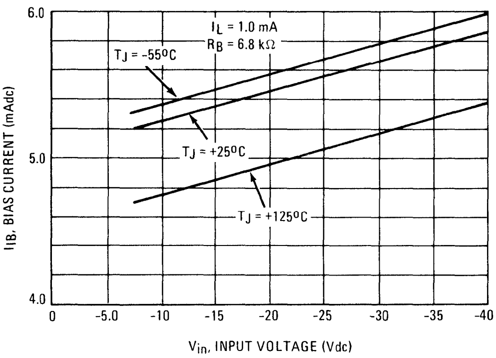


FIGURE 18 – EFFECTS OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

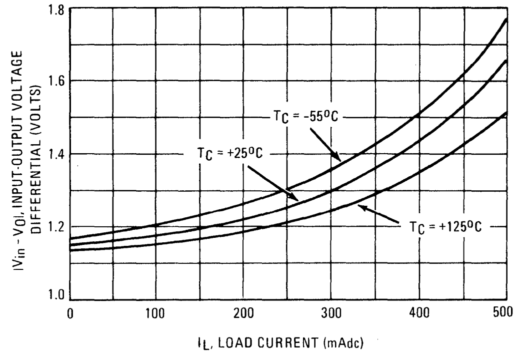


FIGURE 19 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

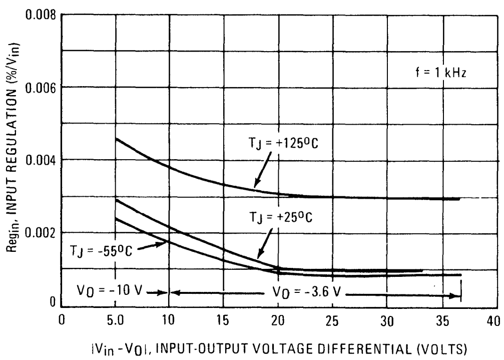


FIGURE 20 – INPUT TRANSIENT RESPONSE

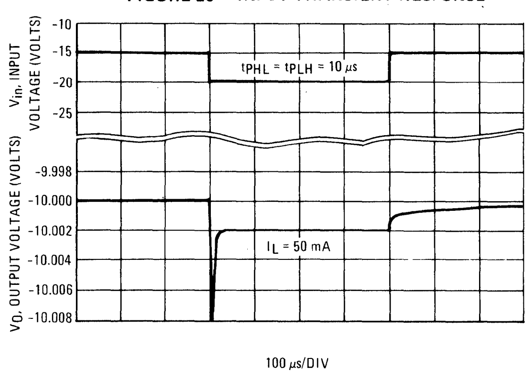


FIGURE 21 – LOAD TRANSIENT RESPONSE

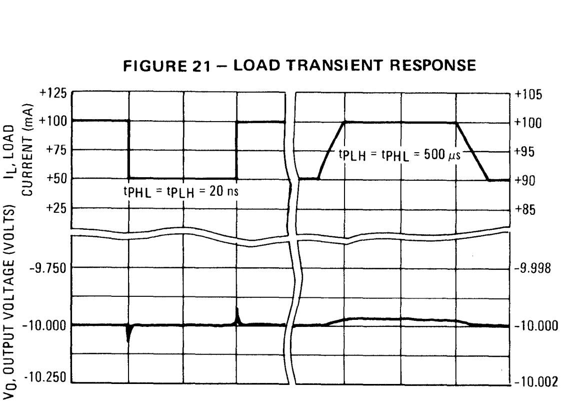
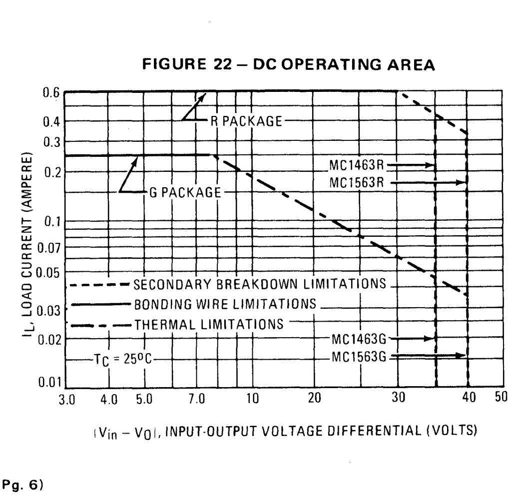


FIGURE 22 – DC OPERATING AREA



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OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1563 (MC1463) negative voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE INDEX

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 23, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 24. The gain-determining resistors may be external, enabling a wide range of output voltages. This is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1563) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1563 negative voltage regulator.

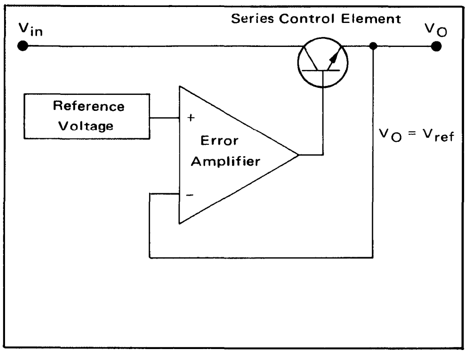


FIGURE 23 — Series Voltage Regulator

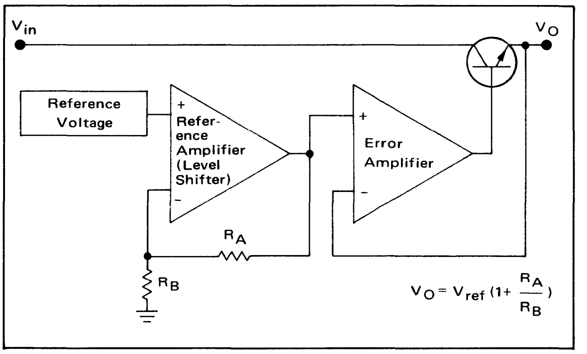
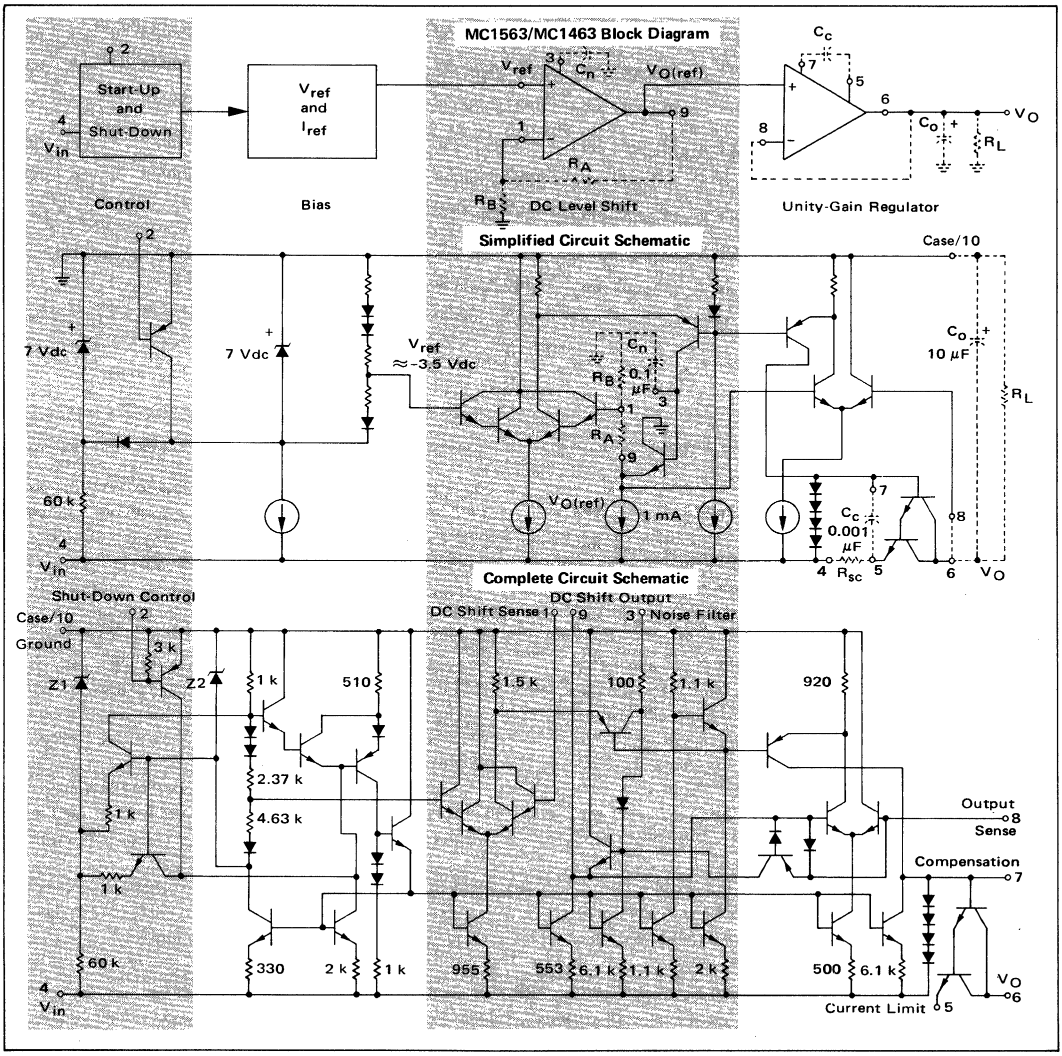


FIGURE 24 — The "Regulator-Within-A-Regulator" Approach

FIGURE 25
(Recommended External Circuitry is Depicted With Dotted Lines.)



MC1563 (MC1463) Operation

Figure 25 shows the MC1563 (MC1463) Negative Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

The shutdown control, in effect, consists of a PNP transistor across the reference zener diode. When this transistor is turned "ON", via pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to $V_{in}/60\ k\Omega$ or 500 μA for a -30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately -3.5 Vdc with a typical temperature coefficient of 0.002%/°C. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R_A and R_B) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_n, is introduced externally into the level shift network (via pin 3) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is 0.1 μF and should have a voltage rating in excess of the desired output voltage. Smaller capacitors (0.001 μF minimum) may be used but will cause a slight increase in output noise. Larger values of C_n will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the shift amplifier is fed internally to the noninverting input of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (pin 8) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{SC}, is connected in the emitter of this transistor to sample the full load current. This connection enables a four-diode string to limit the drive current to the power transistors in a conventional manner.

Stability and Compensation

As has been seen, the MC1563 employs two amplifiers, each using negative feedback. This implies the possibility of frequency instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (pin 7) and pin 5. The recommended value of 0.001 μF will insure stability and still provide acceptable transient response (see Figure 21). It is also necessary to use an output capacitor, C_O, (typically 10 μF) directly from the output (pin 6) to ground. When an external transistor is used to boost the current, C_O = 100 μF is recommended (see Figure 26).

NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 2 or 26, are recommended. The circuit shown in Figure 26 can supply up to approximately 4.0 amperes (subject to safe area limitations). At higher currents the V_{BE} of the pass transistor may itself exceed the threshold of the current limit even for R_{SC} = 0. Figure 2 illustrates the use of an additional external diode from pin 4 for higher current operation or for pass transistors exhibiting higher V_{BE}'s. It will probably be necessary to determine R_{SC} experimentally for each case where a pass transistor is used because V_{BE} varies from device to device. The circuit of Figure 26 when set up for a -10 V output

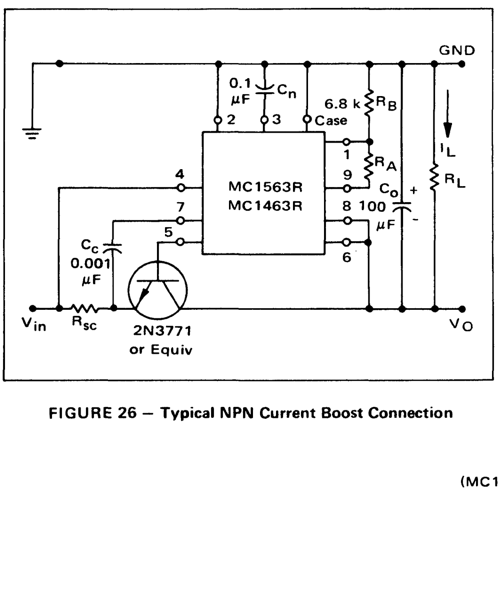


FIGURE 26 – Typical NPN Current Boost Connection

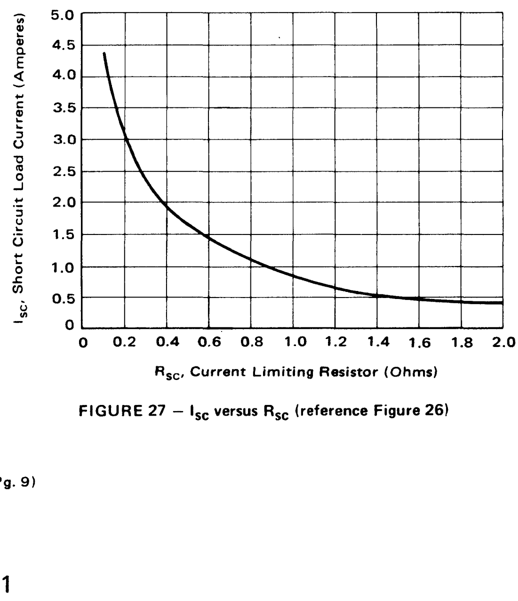


FIGURE 27 – I_{sc} versus R_{sc} (reference Figure 26)

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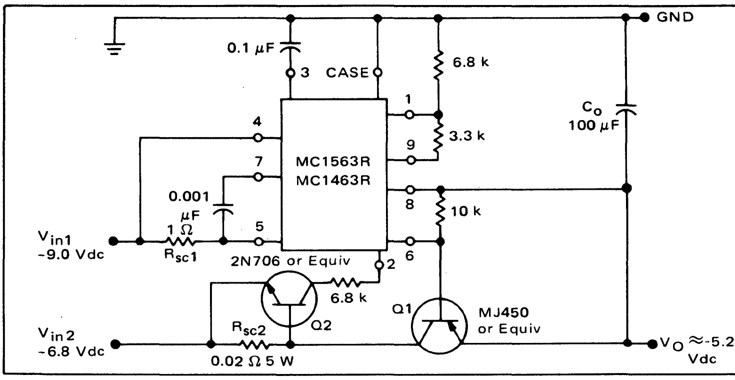


FIGURE 28 – PNP Current Boost Connection

(R_A = 13 kΩ) supply and operating with a - 15 V input, with a R_{SC} of 0.1 Ω, will yield a change in output voltage of only 26 mV over a load current range of from 1 mA to 3.5 A. This corresponds to a dc output impedance of only 7.5 milliohms or a percentage load regulation of 0.26% for a full 3.5-ampere load current change. Figure 27 indicates how the short circuit current varies with the value of R_{SC} for this circuit.

PNP CURRENT BOOSTING

A PNP power transistor can also be used to boost the load current capabilities. To improve the efficiency of the PNP boost configuration, particularly for small output voltages, the circuit of Figure 28, is recommended. An auxiliary -9 volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 10-ampere regulator of Figure 28 this represents a savings of 22 watts when compared with operating the regulator from the single -9 V supply. It can supply current to 10 amperes while requiring an input voltage to the collector of the pass transistor of -6.8 volts minimum. The pass transistor is limited to 10 amperes by the added short-circuit current network in its emitter (R_{SC2}) and the IC regulator is limited to 500 mA in the conventional manner (R_{SC1}). The MJ450 exhibits a minimum h_{FE} of 20 at 10 amperes, thus requiring only 500 mA from the MC1563R. Regulation of this circuit is comparable to that of the NPN boost configuration.

For higher output voltages the additional unregulated power supply is not required. The collector of the PNP boost transistor can tie directly to pin 5 and the internal current limit circuit will provide short-circuit protection using R_{SC} (see Figure 11). Transistor Q2 and R_{SC2} will not be required and pin 2 should be returned to ground.

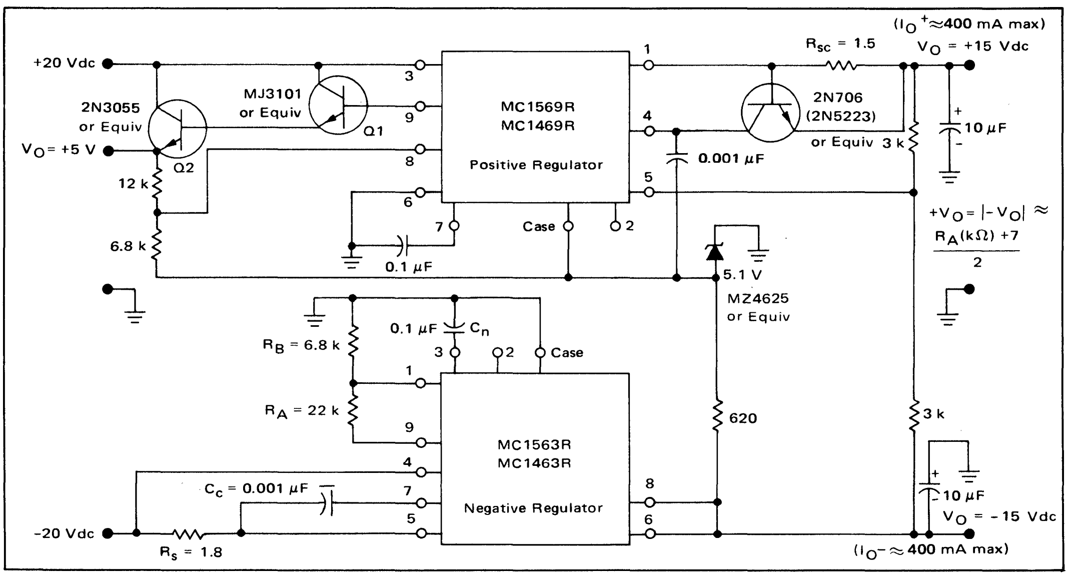
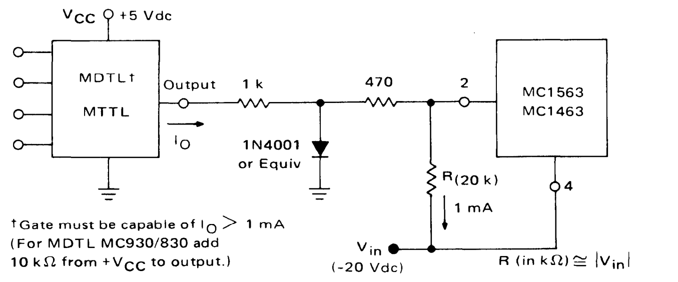


FIGURE 29 – A ±15 Vdc Complementary Tracking Regulator With Auxiliary +5.0 V Supply

FIGURE 30 – Saturated Logic Level Shutdown Circuit



POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1563 is driven from a floating source it is possible to use it as a positive regulator by grounding the negative output terminal. The MC1563 may also be used with the MC1569 to provide completely independent positive and negative power regulators with comparable performance. When used in this manner a silicon diode such as the 1N4001 must be connected as a clamp on the output with the cathode to ground and the anode to the negative output voltage. This is to prevent the positive voltage in the system from forcing the output to a positive value and preventing the MC1563 from starting up.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 3 and 29 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (pin 6 of the MC1569) and using the other side (pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3 k-ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at pin 5 will be zero. When the voltage at pin 5 equals zero, $+|V_O|$ must equal $-|V_O|$.

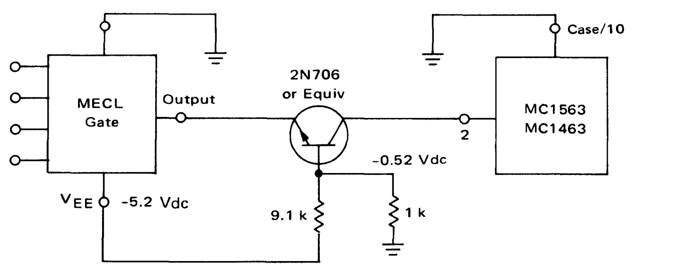
For the configuration shown in Figure 29, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown, is not short-circuit protected.) The -15-volt supply varies less than 0.1 mV over a zero to -300 mAdc current range and the +15-volt supply tracks this variation. The +15-volt supply varies 20 mV over the zero to +300-mAdc load current range. The +5-volt supply varies less than 5 mV for $0 \leq I_L \leq 200$ mA with the other two voltages remaining unchanged. See MC1561 data sheet or MC1569 data sheet for information concerning latch-up when using plus and minus regulations.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1563 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of a PNP transistor; which, if turned "ON", will deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60 k-ohm start resistor (V_{in}/60 kΩ). This feature provides additional versatility in the applications of the MC1563. Various sub-systems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as over-heating, over-voltage, shorted output, etc.

As an illustration of the first case, consider a system consisting of both positive-supply logic (MTTL) and negative-supply logic (MECL). The MECL logic may be used in a high-speed arithmetic processor whose services are not continuously required. Substantial power may

FIGURE 31 – MECL Logic Level Shutdown Circuit



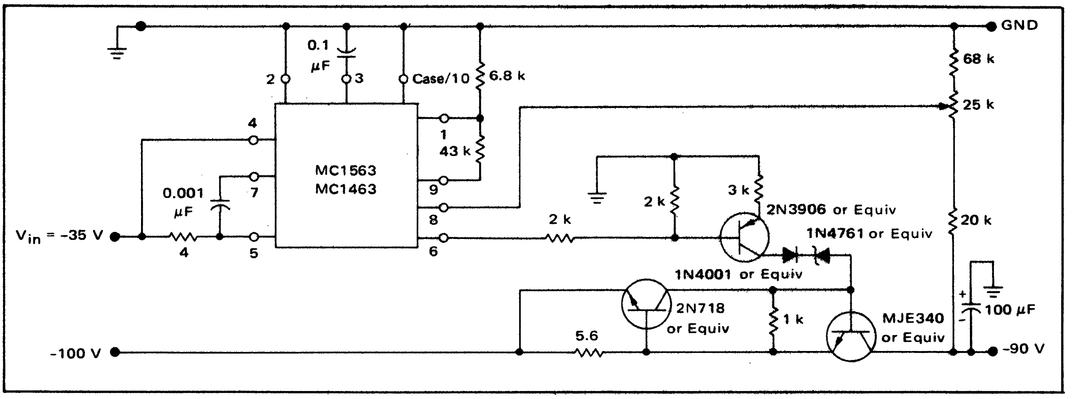


FIGURE 32 – Voltage Boosting Circuit

thus be conserved if the MECL circuitry remains unpowered except when needed. The negative regulator can be shutdown using any of the standard logic swings. For saturated logic control, Figure 30 shows a circuit that allows the normal positive output swing to cause the regulator to shutdown when the logic output is in the low voltage state. The negative output levels of a MECL gate can also be used for shutdown control as shown in Figure 31.

VOLTAGE BOOSTING

Some applications may require a high output voltage which may exceed the voltage rating of the MC1563. This must be solved by assuring that the IC regulator is operated within its limits. Three points in the regulator need to be considered:

1. The input voltage (pin 4),
2. the output voltage (pin 6) and,
3. the output sense lead (pin 8).

A reduced input voltage can be provided by using a separate supply. The output voltage may be zener-level shifted, and the sense line can tie to a portion of the output voltage through a resistive divider. The voltage boost circuit of Figure 32 uses this approach to provide a -90 volt supply. This circuit will exhibit regulation of 0.001% over a 100 mA load current range.

REMOTE SENSING

The MC1563 offers a remote sensing capability. This is important when the load is remote from the regulator, as the resistances of the interconnecting lines (V_{EE} and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 33 shows how remote sensing is accomplished using both a separate sense line from pin 8 and a separate ground line from the regulator to the remote load.

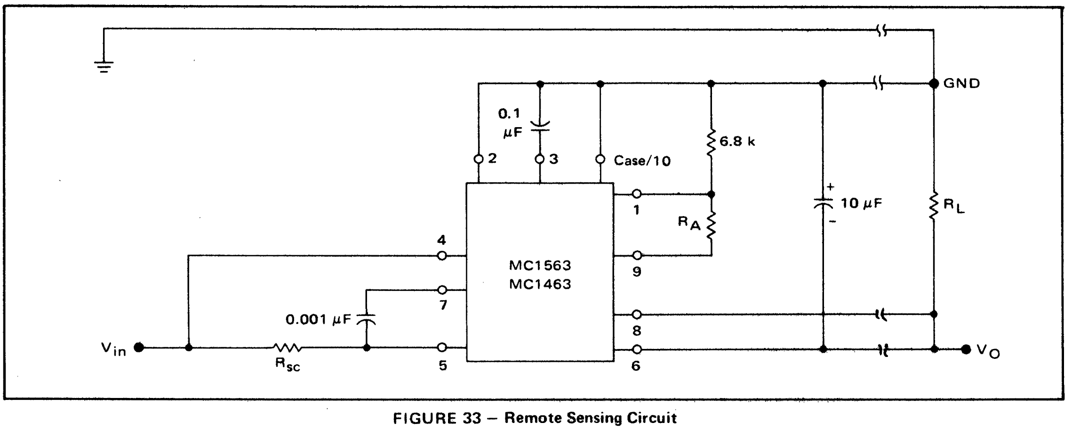


FIGURE 33 – Remote Sensing Circuit

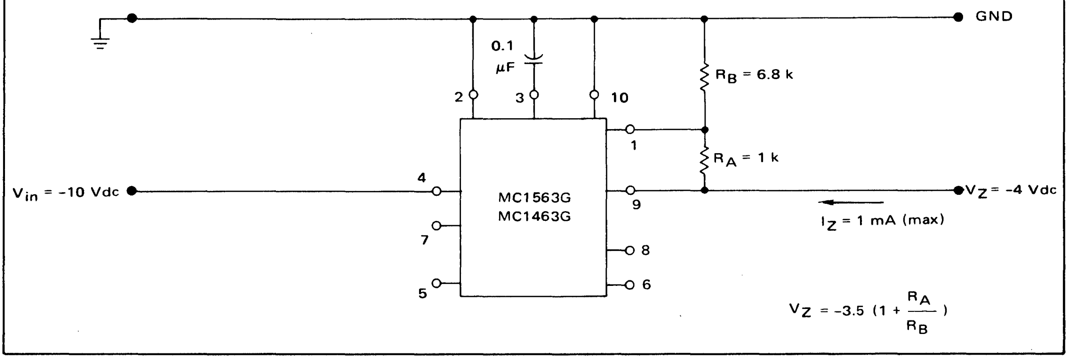


FIGURE 34 – An Adjustable "Zero-TC" Voltage Source

AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE

The MC1563, when used in conjunction with low-TC resistors, makes an excellent reference-voltage generator. If the -3.5 volt reference voltage of the IC regulator is a satisfactory value, then pins 1 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, R_A and R_B, any voltage between -3.5 Vdc and -37 Vdc can be obtained with the same low TC (see Figure 34)

THERMAL SHUTDOWN

By setting a fixed voltage at pin 2, the MC1563 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor (-1.9 x 10^{-3}V/°C). By setting -0.61 Vdc externally, at pin 2, the regulator will shutdown when the chip temperature reaches approximately 140°C. Figure 35 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

In the case where an external pass transistor is employed; its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 36. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application,

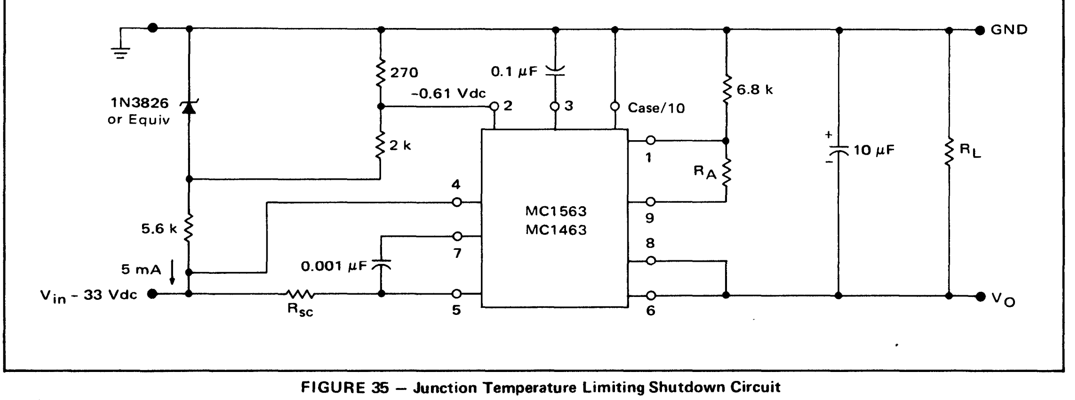


FIGURE 35 – Junction Temperature Limiting Shutdown Circuit

the designer must use caution not to exceed the specified maximum junction temperature (+175°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current (500 mA). Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 22).

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically +0.03%/watt for the MC1563R. For an example of the relative magnitudes of these effects, consider the following conditions:

Given: MC1563R
with V_{in} = -10 Vdc
V_O = -5 Vdc
and I_L = 100 mA to 200 mA
(ΔI_L = 100 mA)
assume T_A = +25°C
TO-66 Type Case with heatsink

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

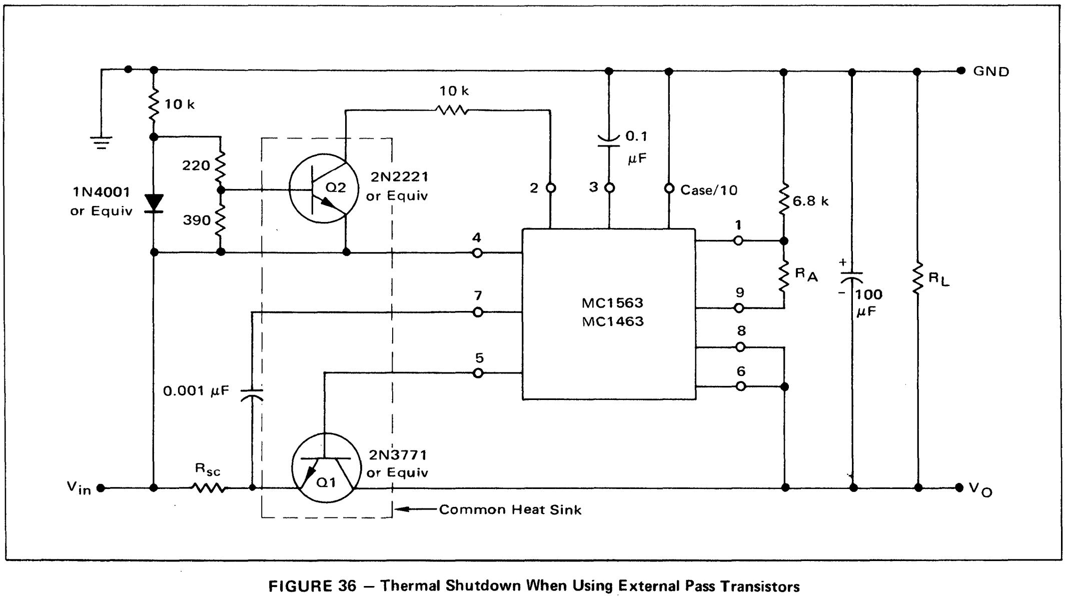


FIGURE 36 – Thermal Shutdown When Using External Pass Transistors

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assume $\theta_{CS} = 0.2^{o}C/W$

and $\theta_{SA} = 2^{o}C/W$

It is desired to find the ΔV_O which results from this ΔI_L. Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_O due to ΔT_J

$$\Delta V_O = (V_O)\,(\Delta P_D)(TCV_O)(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

OR

$$\Delta\ V_O = (5\ V)(5\,V \times 0.1\,A)(\pm 0.002\%/^{o}C)(19.2^{o}C/W)$$

$$\Delta V_O \approx \pm\ 1.0\ mW$$

2. ΔV_O due to z_o

$$|\Delta V_O| = (-z_o)(I_L)$$

$$|\Delta V_O| = -(2 \times 10^{-2})(10^{-1}) = -2\ mV$$

3. ΔV_O due to gradient coefficient, GCV_O

$$|\Delta\ V_O| = (GCV_O)(V_O)(\Delta\,P_D)$$

$$|\Delta\ V_O| = (+3 \times 10^{-4}/W)(5\ volts)(5 \times 10^{-1}W)$$

$$|\Delta\ V_O| = +0.8\ mV$$

Therefore the total $\Delta\ V_O$ is given by

$$|\Delta\ V_O\ total| = \pm\ 1.0 - 2.0 + 0.8\ mV$$

OR

$$-2.2\ mV \leqslant |V_O\ total| \leqslant -0.2\ mV$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

Typical Printed Circuit Board Layout

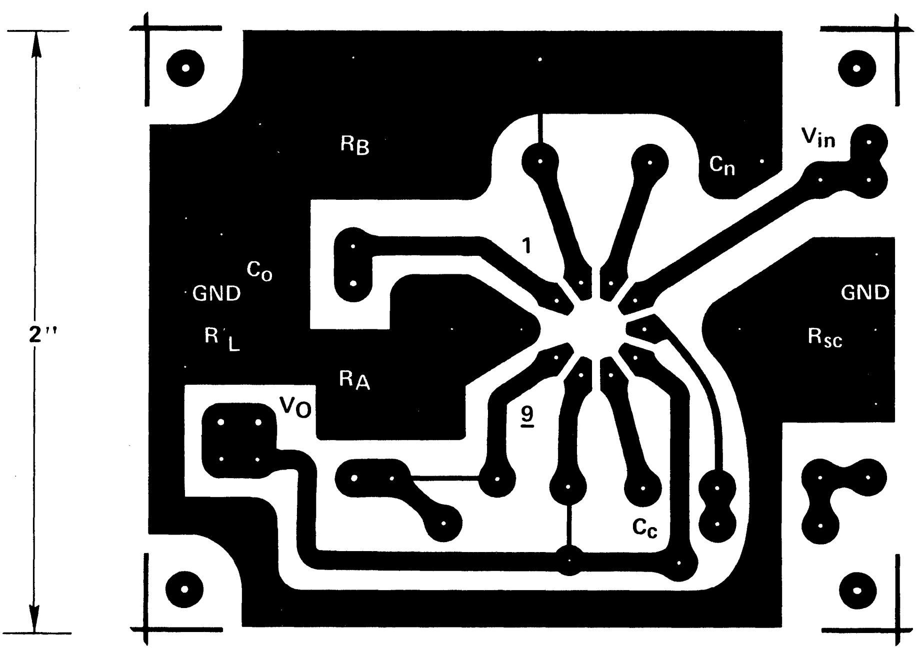

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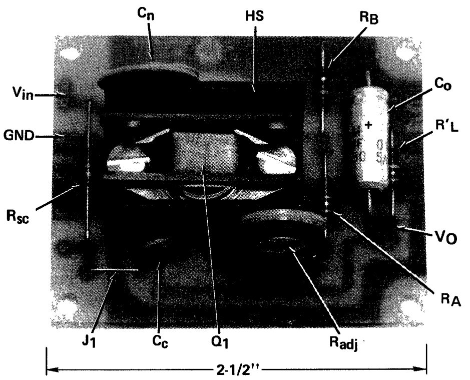
FIGURE 37 – Location of Components



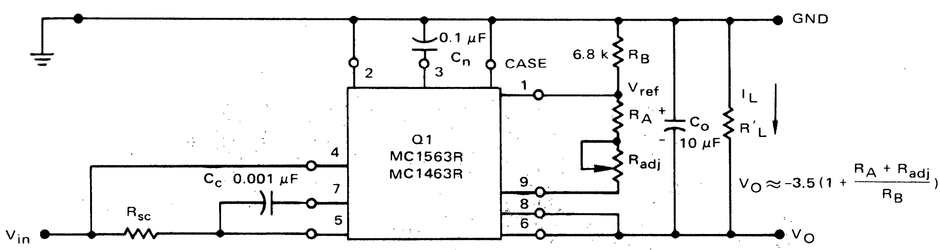
Note 1:
When R_{adj} is used it is necessary to remove the copper which shorts out R_{adj}.

Note 2:
Extra holes are available in the circuit board to permit two resistors to be paralleled to obtain the desired value of R_{sc}.

Note 3:
If pin 2 is used to shut down the regulator, remove the copper which shorts pin 2 to ground.

Note 4:
Remote sensing can be achieved by removing the copper which shorts pin 8 to pin 6 and connecting pin 8 directly to the "minus" load terminal. The circuit board ground should be connected to the unregulated power supply ground at the "plus" load terminal.

Typical Circuit Connection for Output Voltages Between -3.5 and -37 Volts



Select $R_A + R_{adj}$ to Give Desired V_O: $R_A + R_{adj} \approx (2|V_O| - 7)$ kΩ with $R_B = 6.8$ kΩ

PARTS LIST

Component	Value	Description
R_A	Select	1/4 or 1/2 watt carbon
R_B	6.8 k	1/4 or 1/2 watt carbon
R_{adj}	Select	IRC Model X-201, Mallory Model MTC-1 or equivalent
R_{sc}	Select	1/2 watt carbon
R'_L	Select	For minimum current of 1 mAdc
C_o	10 µF	Sprague 1500 Series, Dickson D10C series or equivalent
C_n	0.1 µF	Ceramic Disc – Centralab DDA104, or equivalent
C_C	0.001 µF	Sprague TG-P10, or equivalent
J_1		Jumper
Q1		MC1563R or MC1463R
*HS		Heatsink Thermalloy #6168B or equivalent
*Socket	(Not Shown)	Robinson Nugent #0001306 or equivalent Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1 or equivalent
PC Board		Circuit DOT, Inc. #PC1113 or equivalent 1155 W. 23rd St. Tempe, Arizona 85281

*Optional

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MC1566L
MC1466L

MULTI-PURPOSE REGULATORS

Specifications and Applications Information

MONOLITHIC VOLTAGE AND CURRENT REGULATOR

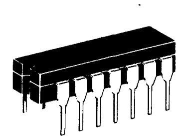
This unique "floating" regulator can deliver hundreds of volts – limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466/MC1566 integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.01% +1.0 mV
- Excellent Load Voltage Regulation, 0.01% +1.0 mV
- Excellent Current Regulation, 0.1% +1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

PRECISION WIDE-RANGE VOLTAGE and CURRENT REGULATOR

EPITAXIAL PASSIVATED

CERAMIC PACKAGE
CASE 632
TO-116



TYPICAL APPLICATIONS

FIGURE 1 – 0-TO-15 VDC, 10-AMPERES REGULATOR

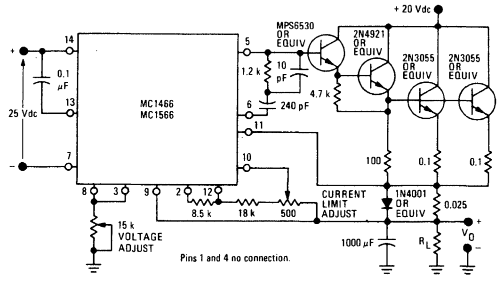


FIGURE 2 – 0-TO-40 VDC, 0.5-AMPERE REGULATOR

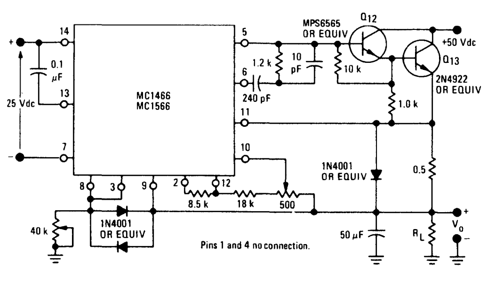


FIGURE 3 – 0-TO-250 VDC, 0.1-AMPERE REGULATOR

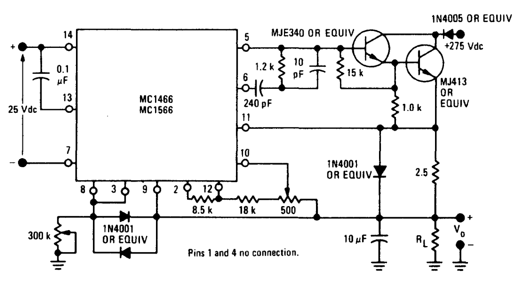
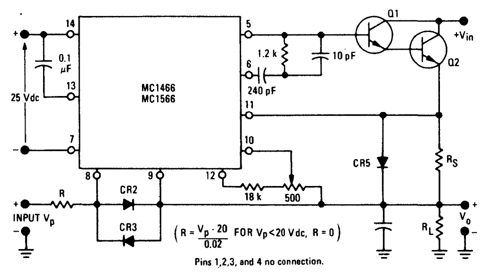


FIGURE 4 – REMOTE PROGRAMMING



(MC1566L – Pg. 1)

See Packaging Information Section for outline dimensions.

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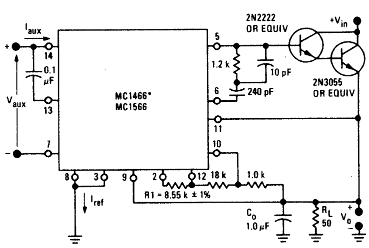
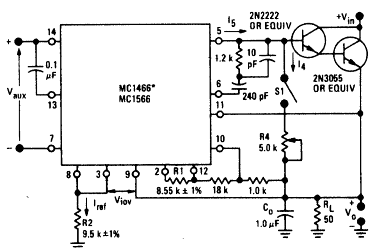
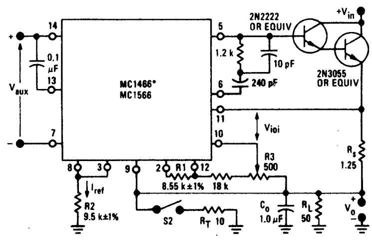
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Auxiliary Voltage		V_{aux}		Vdc
	MC1466		30	
	MC1566		35	
Power Dissipation (Package Limitation)		P_D	750	mW
Derate above T_A = +50°C		$1/\theta_{JA}$	6.0	mW/°C
Operating Temperature Range		T_A		°C
	MC1466		0 to +75	
	MC1566		−55 to +125	
Storage Temperature Range		T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{aux} = +25 Vdc unless otherwise noted)

Characteristic Definition	Characteristic		Symbol	Min	Typ	Max	Units
	Auxiliary Voltage (See Notes 1 & 2)		V_{aux}				Vdc
	(Voltage from pin 14 to pin 7)	MC1466		21	–	30	
		MC1566		20	–	35	
	Auxiliary Current		I_{aux}				mAdc
		MC1466		–	9.0	12	
		MC1566		–	7.0	8.5	
	Internal Reference Voltage		V_{IR}				Vdc
	(Voltage from pin 12 to pin 7)	MC1466		17.3	18.2	19.7	
		MC1566		17.5	18.2	19	
	Reference Current (See Note 3)		I_{ref}				mAdc
		MC1466		0.8	1.0	1.2	
		MC1566		0.9	1.0	1.1	
	Input Current-Pin 8		I_8				µAdc
		MC1466		–	6.0	12	
		MC1566		–	3.0	6.0	
	Power Dissipation		P_D				mW
		MC1466		–	–	360	
		MC1566		–	–	300	
	Input Offset Voltage, Voltage Control Amplifier (See Note 4)		V_{iov}				mVdc
		MC1466		0	15	40	
		MC1566		3.0	15	25	
	Load Voltage Regulation (See Note 5)		ΔV_{iov}				
		MC1466		–	1.0	3.0	mV
		MC1566		–	0.7	1.0	
		MC1466	$\Delta V_{ref}/V_{ref}$	–	0.015	0.03	%
		MC1566		–	0.004	0.01	
	Line Voltage Regulation (See Note 6)		ΔV_{iov}				
		MC1466		–	1.0	3.0	mV
		MC1566		–	0.7	1.0	
		MC1466	$\Delta V_{ref}/V_{ref}$	–	0.015	0.03	%
		MC1566		–	0.004	0.01	
	Temperature Coefficient of Output Voltage		TC_{V_o}				%/°C
	(T_A = 0 to +75°C)	MC1466		–	0.01	–	
	(T_A = −55 to +25°C)	MC1566		–	0.006	–	
	(T_A = +25 to +125°C)	MC1566		–	0.004	–	
	Input Offset Voltage, Current Control Amplifier (See Note 4)		V_{ioi}				mVdc
		MC1466		0	15	40	
	(Voltage from pin 10 to pin 11)	MC1566		3.0	15	25	
	Load Current Regulation (See Note 7)		$\Delta I_L/I_L$				
		MC1466		–	–	0.2	%
		MC1566		–	–	0.1	
		MC1466	ΔI_{ref}	–	–	1.0	mAdc
		MC1566		–	–	1.0	

Pins 1 and 4 no connection.

NOTE 1:
The instantaneous input voltage, V_{aux}, must not exceed the maximum value of 30 volts for the MC1466 or 35 volts for the MC1566. The instantaneous value of V_{aux} must be greater than 20 volts for the MC1566 or 21 volts for the MC1466 for proper internal regulation.

NOTE 2:
The auxiliary supply voltage V_{aux}, must "float" and be electrically isolated from the unregulated high voltage supply, V_{in}.

NOTE 3:
Reference current may be set to any value of current less than 1.2 mAdc by applying the relationship:

$$I_{ref}\ (mA) = \frac{8.55}{R_1\ (k\Omega)}.$$

NOTE 4:
A built-in offset voltage (15 mVdc nominal) is provided so that the power supply output voltage or current may be adjusted to zero.

NOTE 5:
Load Voltage Regulation is a function of two additive components, ΔV_{iov} and ΔV_{ref}, where ΔV_{iov} is the change in input offset voltage (measured between pins 8 and 9) and ΔV_{ref} is the change in voltage across R2 (measured between pin 8 and ground). Each component may be measured separately or the sum may be measured across the load. The measurement procedure for the test circuit shown is:

a. With S1 open ($I_4 = 0$) measure the value of $V_{iov\,(1)}$ and $V_{ref\,(1)}$

b. Close S1, adjust R4 so that $I_4 = 500\ \mu A$ and note $V_{iov\,(2)}$ and $V_{ref\,(2)}$.

Then $\Delta V_{iov} = V_{iov\,(1)} - V_{iov\,(2)}$

% Reference Regulation =

$$\frac{[V_{ref\,(1)} - V_{ref\,(2)}]}{V_{ref\,(1)}}\ (100\%) = \frac{\Delta V_{ref}}{V_{ref}}\ (100\%)$$

Load Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\ (100\%) + \Delta V_{iov}.$$

NOTE 6:
Line Voltage Regulation is a function of the same two additive components as Load Voltage Regulation, ΔV_{iov} and ΔV_{ref} (see note 5). The measurement procedure is:

a. **Set the auxiliary voltage, V_{aux}, to 22 volts for the MC1566 or the MC1466. Read the value of $V_{iov\,(1)}$ and $V_{ref\,(1)}$.**

b. **Change the V_{aux} to 28 volts for the MC1566 or the MC1466 and note the value of $V_{iov\,(2)}$ and $V_{ref(2)}$. Then compute Line Voltage Regulation:**

$$\Delta V_{iov} = \Delta V_{iov\,(1)} - V_{iov\,(2)}$$

% Reference Regulation =

$$\frac{[V_{ref\,(1)} - V_{ref\,(2)}]}{V_{ref\,(1)}}\ (100\%) = \frac{\Delta V_{ref}}{V_{ref}}\ (100\%)$$

Line Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\ (100\%) + \Delta V_{iov}.$$

NOTE 7:
Load Current Regulation is measured by the following procedure:

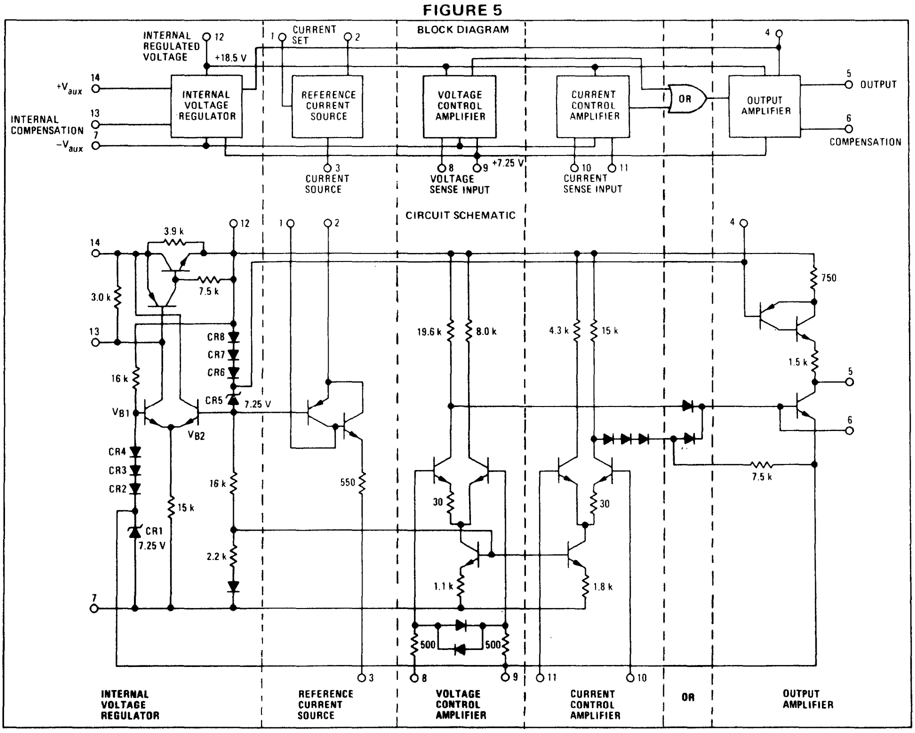
a. With S2 open, adjust R3 for an initial load current, $I_{L(1)}$, such that V_o is 8.0 Vdc.

b. With S2 closed, adjust R_T for $V_o = 1.0$ Vdc and read $I_{L(2)}$. Then Load Current Regulation =

$$\frac{[I_{L(2)} - I_{L(1)}]}{I_{L(1)}}\ (100\%) + I_{ref}$$

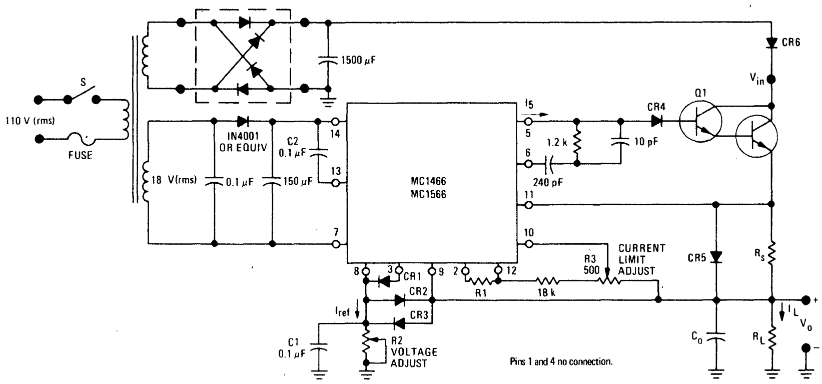
where I_{ref} is 1.0 mAdc, Load Current Regulation is specified in this manner because I_{ref} passes through the load in a direction opposite that of load current and does not pass through the current sense resistor, R_S.

FIGURE 5



(MC1566L – Pg. 3)

FIGURE 6 – TYPICAL CIRCUIT CONNECTION



NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

1. Constant Voltage:
   For constant voltage operation, output voltage V_O is given by:
   $V_O = (I_{ref})\,(R_2)$
   where R2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.
   The recommended value of I_{ref} is 1.0 mAdc. Resistor R1 sets the value of I_{ref}:
   $I_{ref} = \frac{8.5}{R_1}$
   where R1 is the resistance between pins 2 and 12.
2. Constant Current:
   For constant current operation:
   (a) Select R_S for a 250 mV drop at the maximum desired regulated output current, I_{max}.
   (b) Adjust potentiometer R3 to set constant current output at desired value between zero and I_{max}.
3. If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466/MC1566 during short-circuit or transient conditions.
4. In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 μF to 2.0 μF). When R2 is bypassed, CR1 is necessary for protection during short-circuit conditions.
5. CR5 is recommended to protect the MC1466/MC1566 from simultaneous pass transistor failure and output short-circuit.
6. The RC network (10 pF, 240 pF, 1.2 k ohms) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_T of Q1 and Q2 is greater than 0.5 MHz.
7. For remote sense applications, the positive voltage sense terminal (pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2) is connected to the negative load terminal through a separate sense lead.
8. C_O may be selected by using the relationship:
   $C_O = (100\ \mu F)\ I_{L(max)}$, where $I_{L(max)}$ is the maximum load current in amperes.
9. C2 is necessary for the internal compensation of the MC1466/MC1566.
10. For optimum regulation, current out of pin 5, I_5, should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:
    $\frac{I_{max}}{\beta 1 \beta 2} \leqslant 0.5$ mAdc
    where: I_{max} = maximum short-circuit load current (mAdc)
    $\beta 1$ = minimum beta of Q1
    $\beta 2$ = minimum beta of Q2
    Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5$ mAdc will result in a degradation in regulation.
11. CR6 is recommended when $V_O > 150$ Vdc and should be rated such that Peak Inverse Voltage $> V_O$.

OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1566/MC1466 voltage and current regulator and also provides information on useful applications.

SUBJECT SEQUENCE

THEORY OF OPERATION

The schematic of Figure 5 can be simplified by breaking it down into basic functions, beginning with a simplified version of the voltage reference, Figure 7. Zener diodes CR1 and CR5 with their associated forward biased diodes CR2 through CR4 and CR6 through CR8 form the stable reference needed to balance the differential amplifier. At balance ($V_{B1} = V_{B2}$), the output voltage, ($V_{12} - V_7$), is at a value that is twice the drop across either of the two diode strings: $V_{12} - V_7 = 2\,(V_{CR1} + V_{CR2} + V_{CR3} + V_{CR4})$. Other voltages, temperature compensated or otherwise, are also derived from these diodes strings for use in other parts of the circuit.

The voltage controlled current source (Figure 8) is a PNP-NPN composite which, due to the high NPN beta, yields a good working PNP from a lateral device working at a collector current of only a few microamperes. Its base voltage (V_{B2}) is derived from a temperature compensated portion of the diode string and consequently the overall current is dependent on the value of emitter resistor R1. Temperature compensation of the base emitter junction of Q3 is not important because approximately 9 volts exists between V_{B2} and V_{12}, making the ΔV_{BE}'s very small in percentage. Circuit reference voltage is derived from the product of I_R and R_R; if I_R is set at 1 mA (R1 = 8.5 kΩ), then R_R (in kΩ) = V_O. Other values of current may be used as long as the following restraints are kept in mind: 1) package dissipation will be increased by about 11 mW/mA and 2) bias current for the voltage control amplifier is 3 μA, temperature dependent, and is extracted from the reference current. The reference current should

FIGURE 7 – REFERENCE VOLTAGE REGULATOR

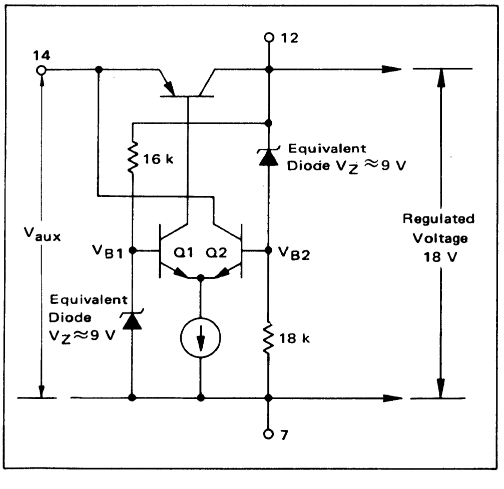
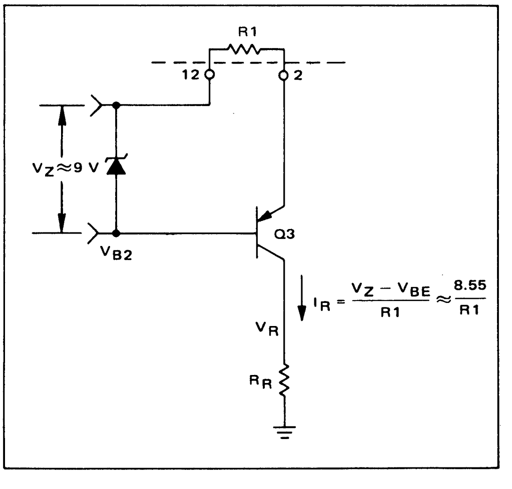


FIGURE 8 – VOLTAGE CONTROLLED CURRENT SOURCE



be at least two orders of magnitude above the largest expected bias current.

Loop amplification in the constant voltage mode is supplied by the voltage controlled amplifier (Figure 9), a standard high-gain differential amplifier. The inputs are diode-protected against differential overvoltages and an emitter degenerating resistor, R_{OS}, has been added to one of the transistors. For an emitter current in both Q5 and Q6 of 1/2 milliampere there will exist a preset offset voltage in this differential amplifier of 15 mV to insure that the output voltage will be zero when the reference voltage is zero. Without R_{OS}, the output voltage could be a few millivolts above zero due to the inherent offset. Since the load resistor is so large in this stage compared with the load (Q9) it will be more instructive to look at the gain on a transconductance basis rather than voltage gain. Transconductance of the differential stage is defined for small signals as:

$$g_m = \frac{1}{2r_e + R_E} \qquad (1)$$

where

$$r_e \approx \frac{0.026}{I_E} \text{ and}$$

R_E = added emitter degenerating resistance.

For $I_E = 0.5$ mA,

$$g_m = \frac{1}{104+30} = \frac{1}{134} = 7.5 \text{ mA/volt.} \qquad (2)$$

FIGURE 9 – VOLTAGE CONTROL AMPLIFIER

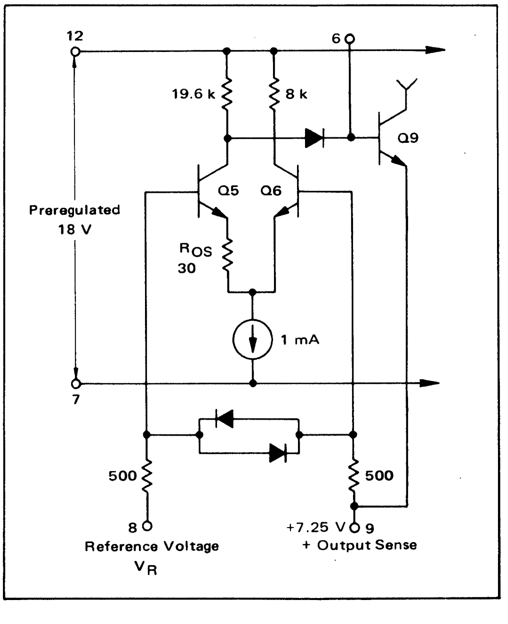
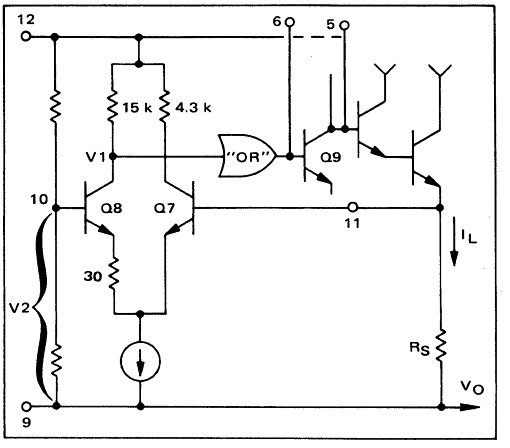


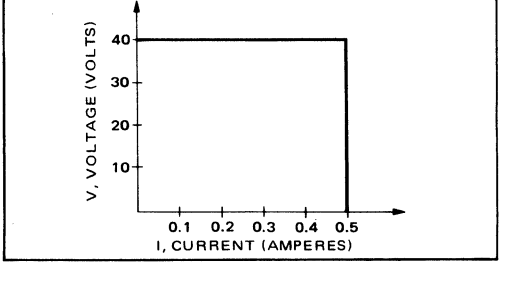
FIGURE 10 – CURRENT CONTROL CIRCUIT



This level is further boosted by the output stage such that in the constant voltage mode overall transconductance is about 300 mA/volt.

A second differential stage nearly identical to the first stage, serves as the current control amplifier (Figure 10). The gain of this stage insures a rapid crossover from the constant voltage to constant current modes and provides a convenient point to control the maximum deliverable load current. In use, a reference voltage derived from the preregulator and a voltage divider is applied to pin 10 while the output current is sampled across R_S by pin 11. When I_L R_S is 15 mV below the reference value, voltage V_1 begins to rapidly rise, eventually gaining complete control of Q9 and limiting output current to a value of V_2/R_S. If V_2 is derived from a variable source, short circuit current may be controlled over the complete output current capability of the regulator. Since the constant-voltage to constant-current change-over requires only a few millivolts the voltage regulation maintains its quality to the current limit and accordingly shows a very sharp "knee" (1% +1 mA, Figure 11). Note that the regulator can switch back into the constant voltage mode if the output voltage reaches a value greater than V_R. Operation through zero milliamperes is guaranteed by the inclusion of another emitter offsetting resistor.

FIGURE 11 – V_I CURVE FOR 0-TO-40 V, 0.5-AMPERE REGULATOR



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Transistor Q9 and five diodes comprise the essential parts of the output stage (Figure 12). The diodes perform an "OR" function which allows only one mode of operation at a time - constant current or constant voltage. However, an additional stage (Q9) must be included to invert the logic and make it compatible with the driving requirements of series pass transistors as well as provide additional gain. A 1.5 mA collector current source sets the maximum deliverable output current and boosts the output impedance to that of the current source.

Note that the negative (substrate) side of the MC1566/MC1466 is 7.25 volts lower than the output voltage, and the reference regulator guarantees that the positive side is 11 volts above the output. Thus the IC remains at a voltage (relative to ground) solely dependent on the output, "floating" above and below V_O. V_{CE} across Q9 is only two or three V_{BE}'s depending on the number of transistors used in the series pass configuration.

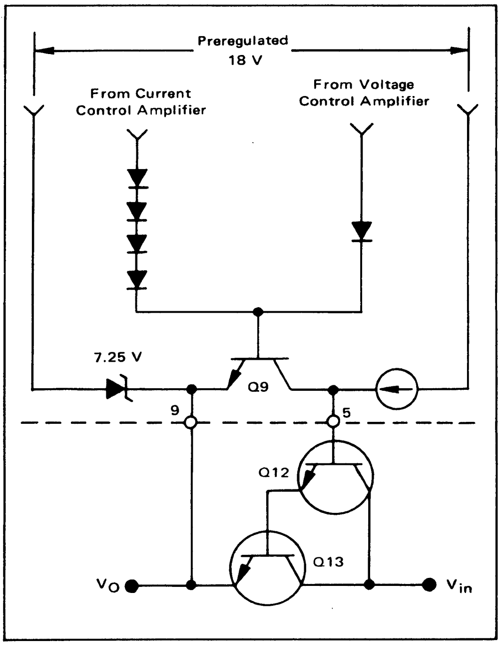
Performance characteristics of the regulator may be approximately calculated for a given circuit (Figure 2). Assuming that the two added transistors (Q12 and Q13) have minimum beta's of 20, then the overall regulator transconductance will be:

$$g_{mT} = (400)\,300\ \text{mA/volt} = 120\ \text{A/volt}. \qquad (3)$$

For a change in current of 500 mA the output voltage will drop only:

$$\Delta V = \frac{0.5}{120} = 4.2\ \text{mV}. \qquad (4)$$

FIGURE 12 – MC1566 OUTPUT STAGE



The analysis thus far does not consider changes in V_R due to output current changes. If I_L increases by 500 mA the collector current of Q9 decreases by 1.25 mA, causing the collector current of Q5 to increase by 30 μA. Accordingly, I_R will be decreased by ≈0.30 μA which will drop the output by 0.03%. This figure may be improved considerably by either using high beta devices as the pass transistors, or by increasing I_R. Note again, however, that the maximum power rating of the package must be kept in mind. For example if I_R = 4 mA, power dissipation is

$$P_D = 20\ \text{V}\ (8\ \text{mA}) + (11\ \text{V} \times 3\ \text{mA}) = 193\ \text{mW}. \qquad (5)$$

This indicates that the circuit may be safely operated up to 118°C using 20 volts at the auxiliary supply voltage. If, however, the auxiliary supply voltage is 35 volts,

$$P_D = 35\ \text{V}\ (8\ \text{mA}) + 26\ \text{V}\ (3\ \text{mA}) = 358\ \text{mW}. \qquad (6)$$

which dictates that the maximum operating temperature must be less than 91°C to keep package dissipation within specified limits.

Line voltage regulation is also a function of the voltage change between pins 8 and 9, and the change of V_{ref}. In this case, however, these voltages change due to changes in the internal regulator's voltages, which in turn are caused by changes in V_{aux}. Note that line voltage regulation is not a function of V_{in}. Note also that the instantaneous value of V_{aux} must always be between 20 and 35 volts.

Figure 6 shows six external diodes (CR_1 to CR_6) added for protective purposes. CR_1 should be used if the output voltage is less than 20 volts and CR_2, CR_3 are absent. For V_o higher than 20 volts, CR_1 should be discarded in favor of CR_2 and CR_3. Diode CR_4 prevents IC failure if the series pass transistors develop collector-base shorts while the main power transistor suffers a simultaneous open emitter. If the possibility of such a transistor failure mode seems remote, CR_4 may be deleted. To prevent instantaneous differential and common-mode breakdown of the current sense amplifier, CR_5 must be placed across the current limit resistor R_s.

Load transients occasionally produce a damaging reversal of current flow from output to input $V_o > 150$ volts (which will destroy the IC). Diode CR_6 prevents such reversal and renders the circuit immune from destruction for such conditions, e.g., adding a large output capacitor after the supply is turned "on". Diodes CR_1, CR_2, CR_3, and CR_5 may be general purpose silicon units such as 1N4001 or equivalent whereas CR_4 and CR_6 should have a peak inverse voltage rating equal to V_{in} or greater.

APPLICATIONS

Figure 2 shows a typical 0-to-40 volts, 0.5-ampere regulator with better than 0.01% performance, The RC network between pins 5 and 6 and the capacitor between pins 13 and 14 provide frequency compensation for the MC1566/MC1466. The external pass transistors are used to boost load current, since the output current of the regulator is less than 2 mA.

Figure 1 is a 0-to-15 volts, 10-ampere regulator with the pass transistor configuration necessary to boost the load current to 10 amperes. Note that C_O has been increased to 1000 μF following the general rule:

$$C_O = 100\ \mu F/A\ I_L.$$

The prime advantage of the MC1566/MC1466 is its use as a high voltage regulator, as shown in Figure 3. This 0-to-250 volts 0.1-ampere regulator is typical of high voltage applications, limited only by the breakdown and safe areas of the output pass transistors.

The primary limiting factor in high voltage series regulators is the pass transistor. Figure 13 shows a safe area curve for the MJ413. Looking at Figure 3, we see that if the output is shorted, the transistor will have a collector current of 100 mA, with a V_{CE} approximately equal to 260 volts. Thus this point falls on the dc line of the safe area curve, insuring that the transistor will not enter secondary breakdown.

In this respect (Safe Operating Area) the foldback circuit of Figure 14 is superior for handling high voltages and yet is short-circuit protected. This is due to the fact that load current is diminished as output voltage drops (V_{CE} increases as V_O drops) as seen in Figure 15. By careful design the load current at a short, I_{SC} can be made low enough such that the combined V_{CE} (V_{in}) and I_{SC} still falls within the dc safe operating area of the transistor. For the illustrated design (Figure 14), an input voltage of 210 volts is compatible with a short-circuit current of 100 mA. Yet current foldback allows us to design for a maximum regulated load current of 500 mA. The pertinent design equations are:

$$\text{Let } R_2\ (k\Omega) = V_O$$

$$\alpha = \frac{0.25}{V_O}\left[\frac{I_k}{I_{SC}} - 1\right]$$

$$R_1\ (k\Omega) = \frac{\alpha}{1-\alpha}\ V_O$$

$$R_{SC} = \frac{0.25}{(1-\alpha)\ I_{SC}}\ .$$

FIGURE 13 – SAFE AREA CURVE FOR THE MJ413

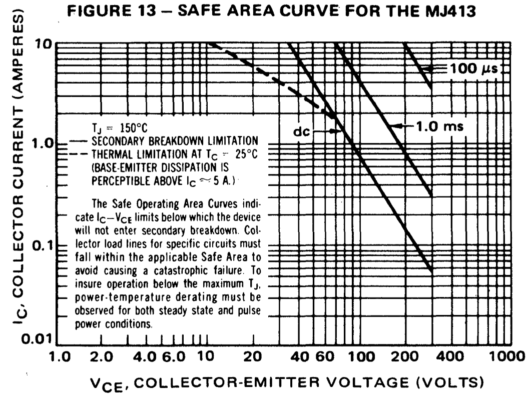
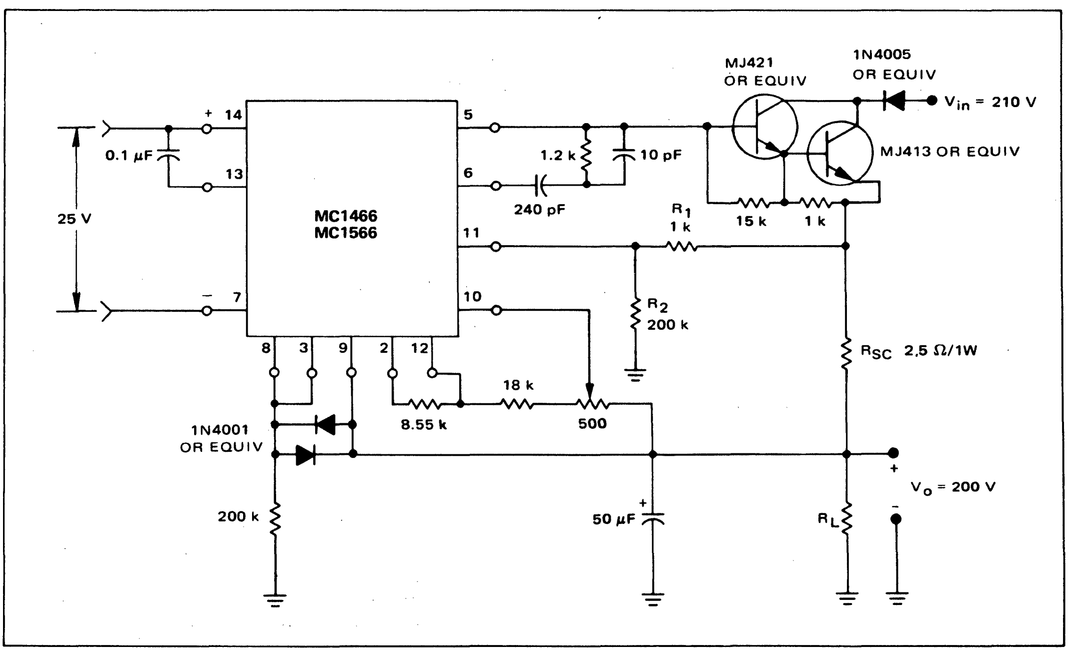


FIGURE 14 – A 200 V, 0.5-AMPERE REGULATOR WITH CURRENT FOLDBACK



The terms I_{SC} and I_k correspond to the short-circuit current and maximum available load current as shown in Figure 15.

FIGURE 15 – TYPICAL FOLDBACK PERFORMANCE

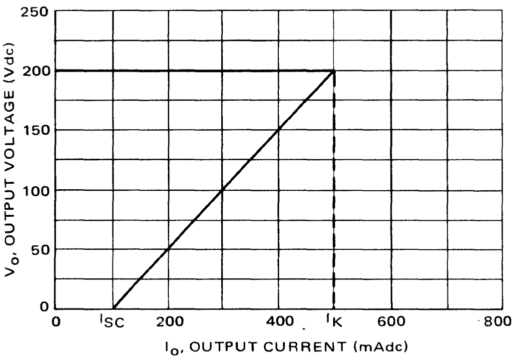


Figure 16 shows a remote sense application which should be used when high current or long wire lengths are used. This type of wiring is recommended for any application where the best possible regulation is desired. Since the sense lines draw only a small current, large voltage drops do not destroy the excellent regulation of the MC1566/MC1466.

TRANSIENT FAILURES

In industrial areas where electrical machinery is used the normal ac line often contains bursts of voltage running from hundreds to thousands of volts in magnitude and only microseconds in duration. Under some conditions this energy is dissipated across the internal zener connected between pins 9 and 7. This transient condition may produce a total failure of the regulator device without any apparent explanation. This type of failure is identified by absence of the 7-volt zener (CR1) between pin 9 and pin 7. To prevent this failure mode, two solutions have been successfully applied. The first method involves the use of an external zener and resistor that shunt more of the transient energy around the IC (Figure 17). The second method is a transient suppression network consisting of capacitors that equalize high frequency components across both the auxiliary and main supply. Figure 18 illustrates the use of five capacitors for the full wave rectified main supply and Figure 19 uses six capacitors when a full wave bridge is used.

VOLTAGE/CURRENT – MODE INDICATOR

There may be times when it is desirable to know when the MC1566/MC1466 is in the constant current mode or constant voltage mode. A mode indicator can be easily added to provide this feature. Figure 20 shows how a PNP transistor has replaced a protection doide between pins 8 and 9 of Figure 2. When the MC1566/MC1466 goes from constant voltage mode to constant current mode, V_O will drop below V_8 and the PNP transistor will turn on. The 1-mA current supplied by pin 8 will now be shunted to ground through R_1 in parallel with R_2, which provides a control voltage, V_C. This voltage V_C can then control a Schmitt trigger which drives front panel lamps to indicate "constant current" or "constant voltage."

FIGURE 16 – REMOTE SENSE

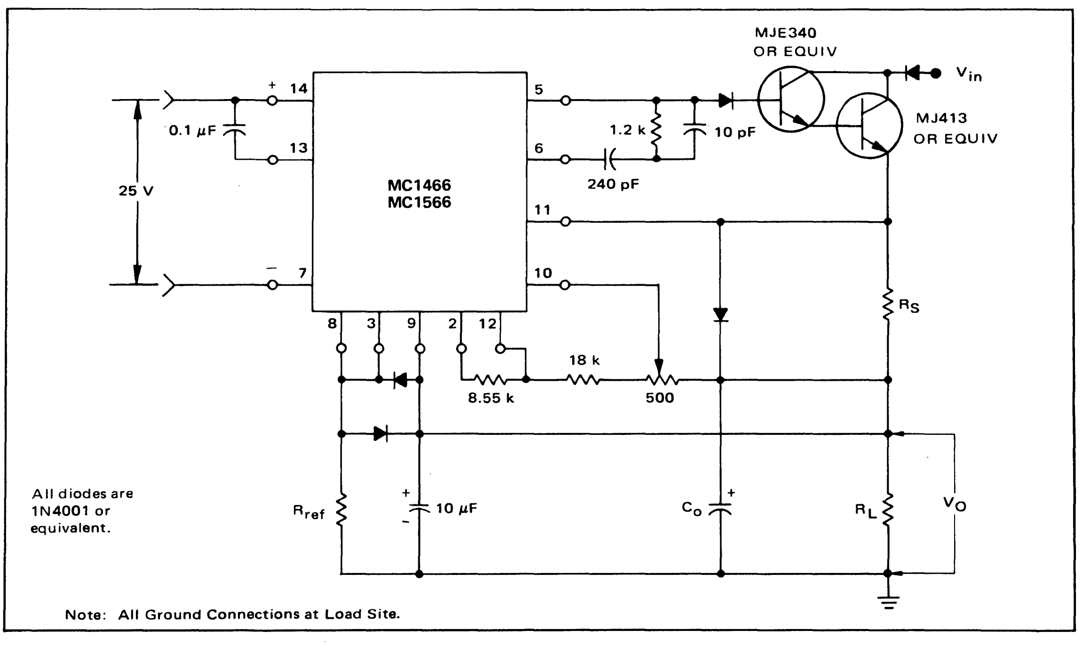


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FIGURE 17 — A 0-TO-250 VOLT, 0.1-AMPERE REGULATOR

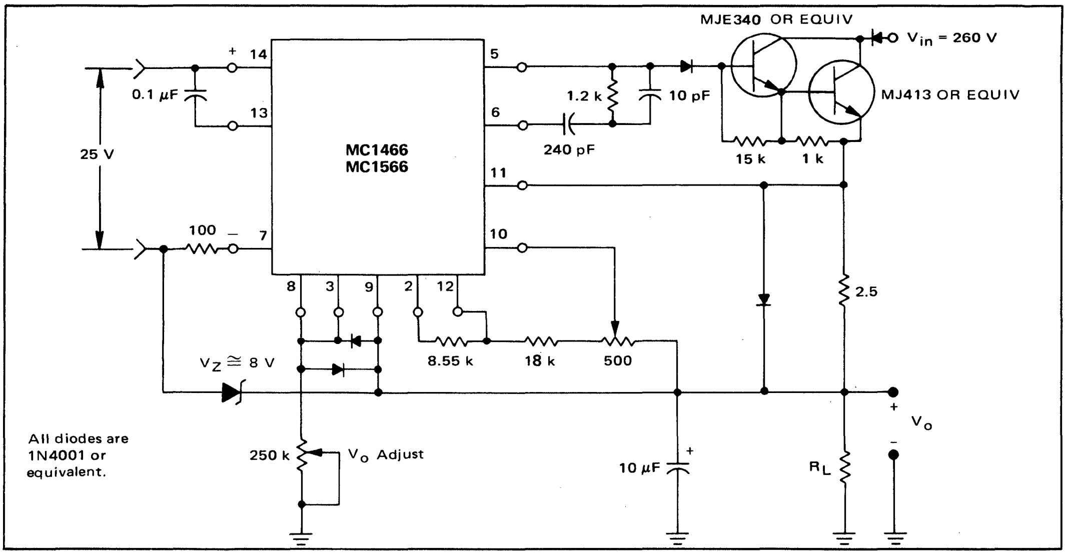


FIGURE 18 — HALF-WAVE RECTIFIER WITH TRANSIENT SUPPRESSION

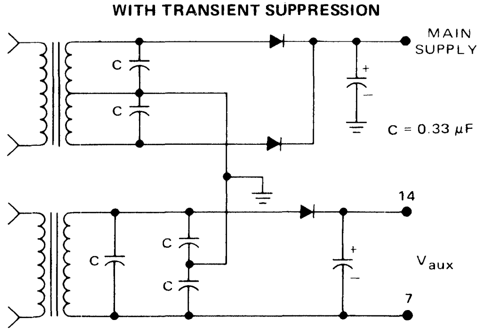


FIGURE 19 — FULL-WAVE RECTIFICATION WITH TRANSIENT SUPPRESSION

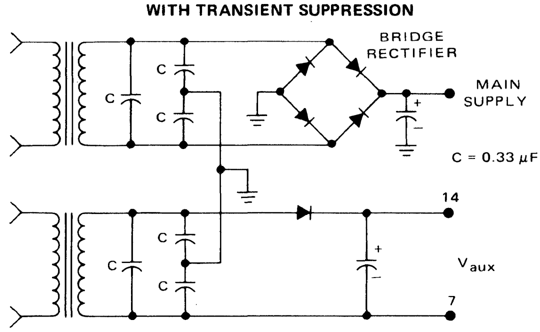
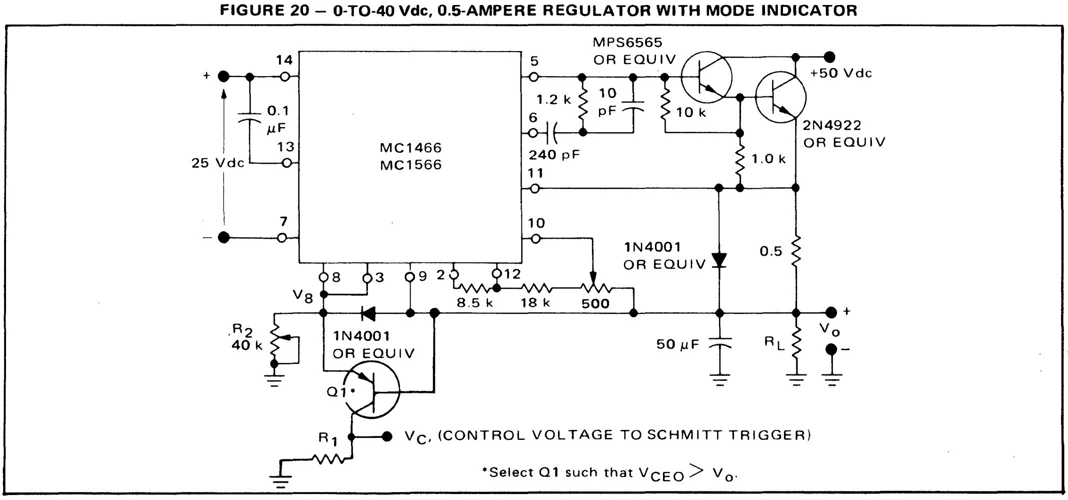


FIGURE 20 — 0-TO-40 Vdc, 0.5-AMPERE REGULATOR WITH MODE INDICATOR



MC1568
MC1468

DUAL VOLTAGE REGULATORS

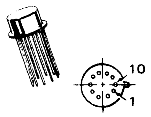
DUAL ±15-VOLT REGULATOR

The MC1568/MC1468 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100 mA. Internally, the device is set for ± 15-volt outputs but an external adjustment can be used to change both outputs simultaneously from 8.0 to 20 volts. Input voltages up to ± 30 volts can be used and there is provision for adjustable current limiting. The device is available in three package types to accomodate various power requirements.

- Internally set to ± 15 V Tracking Outputs
- Output Currents to 100 mA
- Outputs Balanced to within 1% (MC1568)
- Line and Load Regulation of 0.06%
- 1% Maximum Output Variation due to Temperature Changes
- Standby Current Drain of 3.0 mA
- Externally Adjustable Current Limit
- Remote Sensing Provisions
- Case is at Ground Potential (R suffix package)

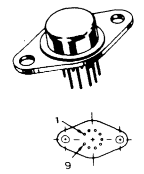
DUAL ±15-VOLT TRACKING REGULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



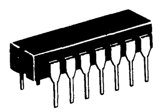
(bottom view)

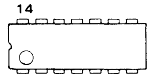
CASE 603
METAL PACKAGE
G SUFFIX



CASE 614
METAL PACKAGE
R SUFFIX

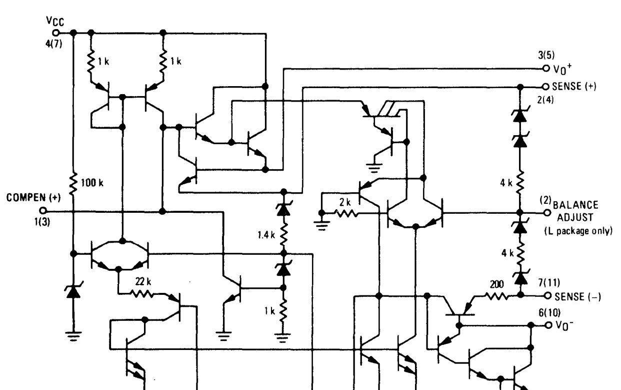
CASE 632
CERAMIC PACKAGE
TO-116
L SUFFIX





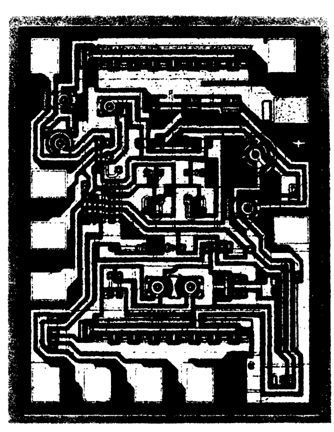
(top view)

CIRCUIT SCHEMATIC



Pin numbers adjacent to terminals are for the G and R suffix packages only. Pin numbers in parentheses are for the L suffix package only.

Pin 10 is ground for the G suffix package only. For the R package, the case is ground.



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
Input Voltage	$V_{CC}, \lvert V_{EE} \rvert$	30			Vdc
Peak Load Current	I_{PK}	100			mA
Power Dissipation and Thermal Characteristics		G Package	R Package	L Package	
T_A = +25°C	P_D	0.8	2.4	1.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	5.4	16	6.7	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	185	62	150	°C/W
T_C = +25°C	P_D	2.1	9.0	2.5	Watts
Derate above T_C = +25°C	$1/\theta_{JC}$	14	61	20	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	70	17	50	°C/W
Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175			°C
Minimum Short-Circuit Resistance	$R_{SC}(min)$	4.0			Ohms

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1468		0 to +75	
MC1568		-55 to +125	

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, V_{EE} = -20 V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 μF, $R_{SC}^+ = R_{SC}^-$ = 4.0 Ω, $I_L^+ = I_L^-$ = 0, T_C = +25°C unless otherwise noted.) (See Figure 1.)

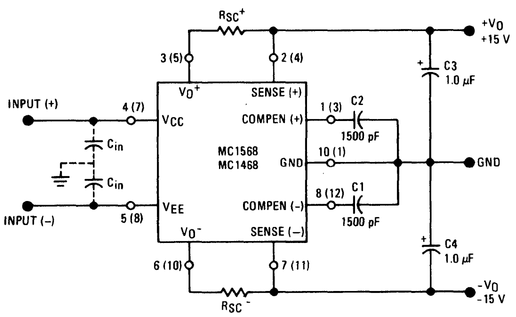
Characteristic	Symbol	MC1568 Min	MC1568 Typ	MC1568 Max	MC1468 Min	MC1468 Typ	MC1468 Max	Unit
Output Voltage	V_O	±14.8	±15	±15.2	±14.5	±15	±15.5	Vdc
Input Voltage	V_{in}	–	–	±30	–	–	±30	Vdc
Input-Output Voltage Differential	$\lvert V_{in} - V_O \rvert$	2.0	–	–	2.0	–	–	Vdc
Output Voltage Balance	V_{Bal}	–	±50	±150	–	±50	±300	mV
Line Regulation Voltage	Reg_{in}							mV
(V_{in} = 18 V to 30 V)		–	–	10	–	–	10	
(T_{low} ① to T_{high} ②)		–	–	20	–	–	20	
Load Regulation Voltage	Reg_L							mV
(I_L = 0 to 50 mA, T_J = constant)		–	–	10	–	–	10	
(T_A = T_{low} to T_{high})		–	–	30	–	–	30	
Output Voltage Range	V_{OR}							Vdc
L Package (See Figure 4.)		±8.0	–	±20	±8.0	–	±20	
R and G Packages (See Figures 2 and 13.)		±14.5	–	±20	±14.5	–	±20	
Ripple Rejection (f = 120 Hz)	RR	–	75	–	–	75	–	dB
Output Voltage Temperature Stability (T_{low} to T_{high})	$\lvert TS_{V_O} \rvert$	–	0.3	1.0	–	0.3	1.0	%
Short-Circuit Current Limit (R_{SC} = 10 ohms)	I_{SC}	–	60	–	–	60	–	mA
Output Noise Voltage (BW = 100 Hz - 10 kHz)	V_N	–	100	–	–	100	–	μV(RMS)
Positive Standby Current (V_{in} = +30 V)	I_B^+	–	2.4	4.0	–	2.4	4.0	mA
Negative Standby Current (V_{in} = -30 V)	I_B^-	–	1.0	3.0	–	1.0	3.0	mA
Long-Term Stability	$\Delta V_O/\Delta t$	–	0.2	–	–	0.2	–	%/k Hr

① T_{low} = 0°C for MC1468
= -55°C for MC1568

② T_{high} = +75°C for MC1468
= +125°C for MC1568

TYPICAL APPLICATIONS

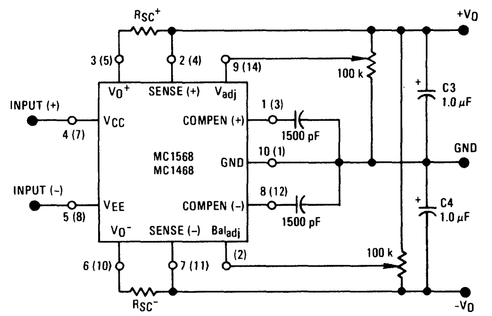
FIGURE 1 – BASIC 50-mA REGULATOR



C1 and C2 should be located as close to the device as possible. A 0.1 μF ceramic capacitor (C_{in}) may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors.

C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation, it may be necessary to bypass C4 with a 0.1 μF ceramic disc capacitor.

FIGURE 2 – VOLTAGE ADJUST AND BALANCE ADJUST CIRCUIT



Balance adjust available in MC1568L, MC1468L ceramic dual in-line package only.

FIGURE 3 – ±1.5-AMPERE REGULATOR
(Short-Circuit Protected, with Proper Heatsinking)
(Metal-Packaged Devices Only, R Suffix)

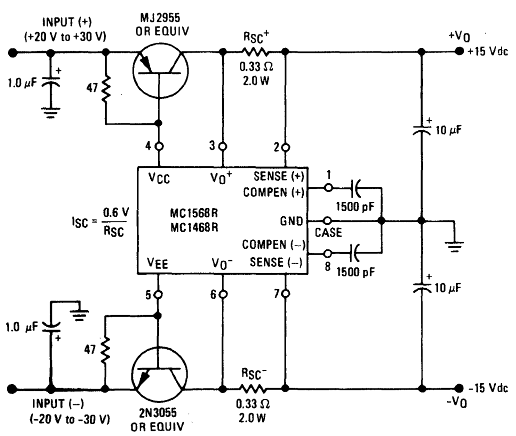
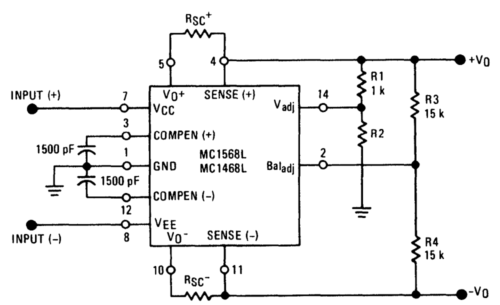


FIGURE 4 – OUTPUT VOLTAGE ADJUSTMENT FOR 8.0 V ≤ |±VO| ≤ 14.5 V
(Ceramic-Packaged Devices Only, L Suffix.)



The presence of the Bal_{adj}, pin 2, on devices housed in the dual in-line package (L suffix) allows the user to adjust the output voltages down to ±8.0 V. The required value of resistor R2 can calculated from

$$R2 = \frac{R1\ R_{int}\ (\phi + V_z)}{R_{int}\ (V_O - \phi - V_z) - \phi\ R1}$$

Where: R_{int} = An Internal Resistor = R1 = 1 kΩ
ϕ = 0.68 V
V_z = 6.6 V

Some common design values are listed below:

$\pm V_O$(V)	R2	$T_C\ V_O$ (%/°C)	I_B + (mA)
14	1.2 k	0.003	10
12	1.8 k	0.022	7.2
10	3.5 k	0.025	5.0
8.0	∞	0.028	2.6

8

TYPICAL CHARACTERISTICS

(V_{CC} = +20 V, V_{EE} = -20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 – LOAD REGULATION

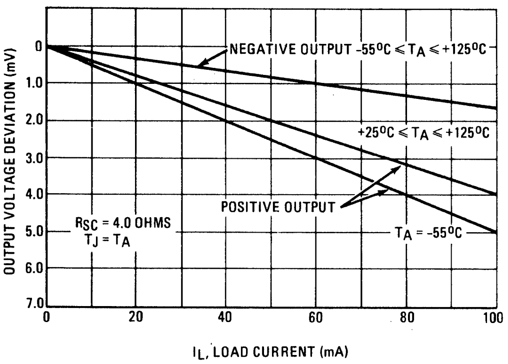


FIGURE 6 – REGULATOR DROPOUT VOLTAGE

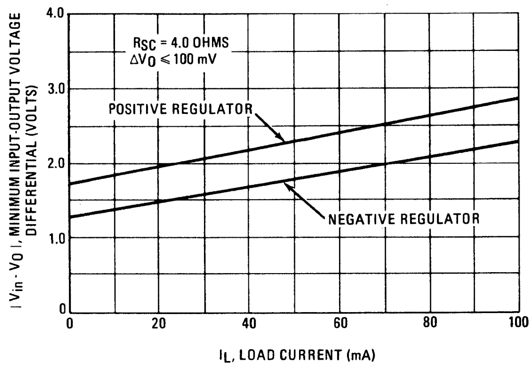


FIGURE 7 – MAXIMUM CURRENT CAPABILITY

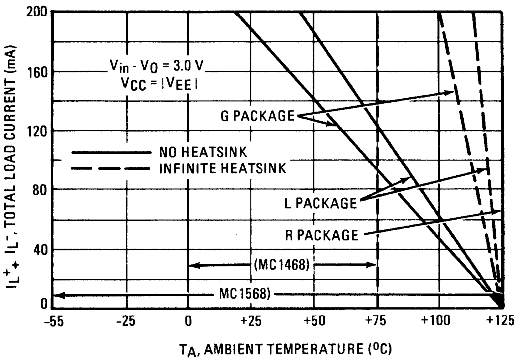


FIGURE 8 – MAXIMUM CURRENT CAPABILITY

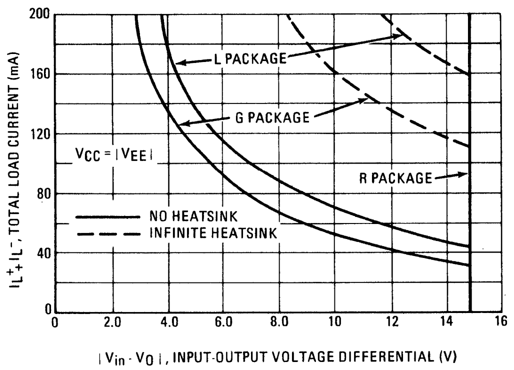


FIGURE 9 – I_{SC} versus R_{SC}

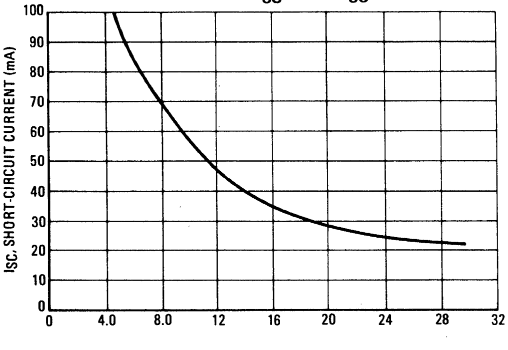
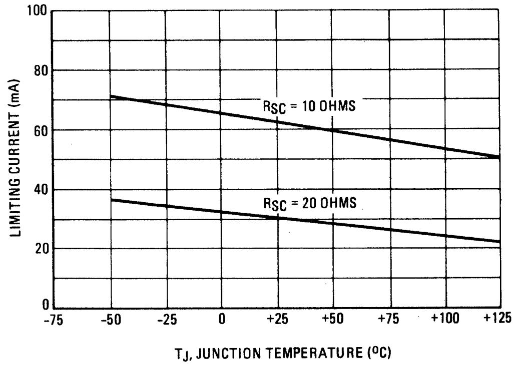


FIGURE 10 – CURRENT-LIMITING CHARACTERISTICS



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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +20 V, V_{EE} = -20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 – STANDBY CURRENT DRAIN

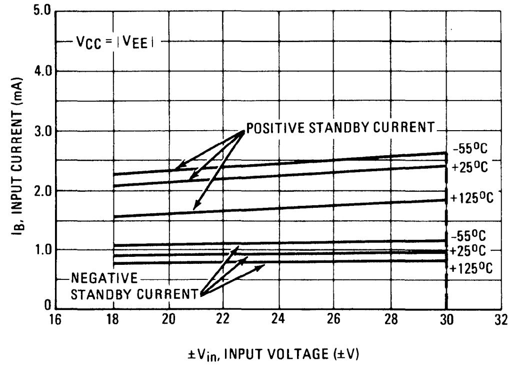


FIGURE 12 – STANDBY CURRENT DRAIN

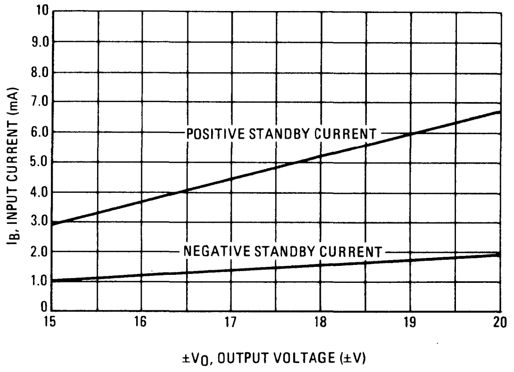


FIGURE 13 – TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

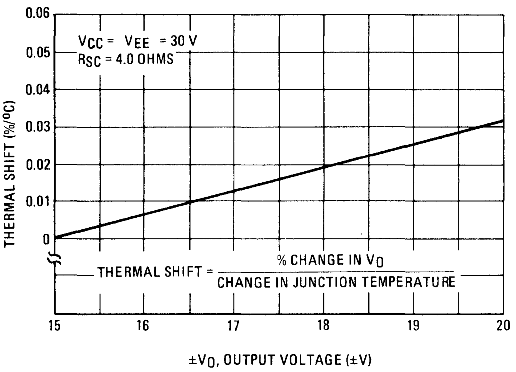


FIGURE 14 – LOAD TRANSIENT RESPONSE

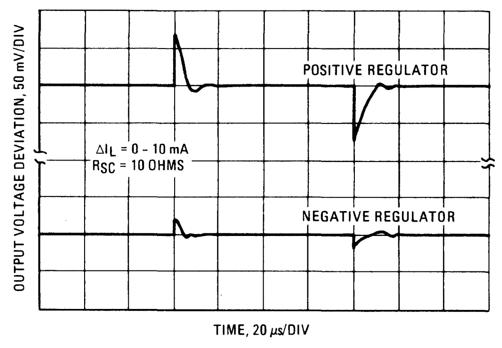


FIGURE 15 – LINE TRANSIENT RESPONSE

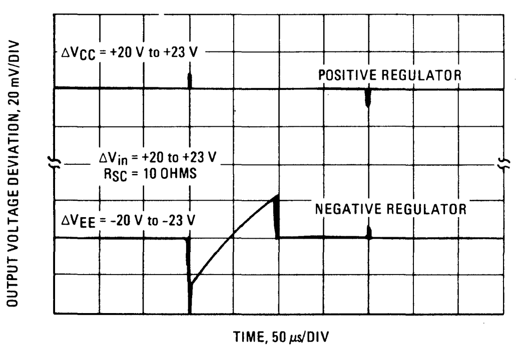
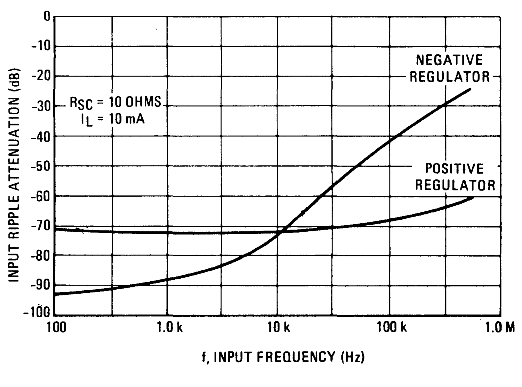


FIGURE 16 – RIPPLE REJECTION



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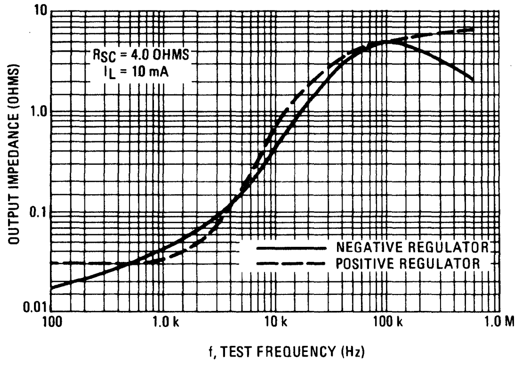
TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +20 V, V_{EE} = -20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 17 – OUTPUT IMPEDANCE



POSITIVE VOLTAGE REGULATORS

MC1569
MC1469

Specifications and Applications Information

MONOLITHIC VOLTAGE REGULATOR

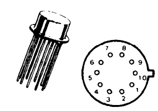
The MC1569/MC1469 is a positive voltage regulator designed to deliver continuous load current up to 500 mAdc. Output voltage is adjustable from 2.5 Vdc to 37 Vdc. The MC1569 is specified for use within the military temperature range (−55 to +125°C) and the MC1469 within the 0 to +70°C temperature range.

For systems requiring a positive regulated voltage, the MC1569 can be used with performance nearly identical to the MC1563 negative voltage regulator. Systems requiring both a positive and negative regulated voltage can use the MC1569 and MC1563 as complementary regulators with a common input ground.

- Electronic "Shut-Down" Control
- Excellent Load Regulation (Low Output Impedance – 20 milli-ohms typ)
- High Power Capability: up to 17.5 Watts
- Excellent Temperature Stability: ±0.002 %/°C typ
- High Ripple Rejection: 0.002 %/V typ

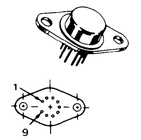
POSITIVE VOLTAGE REGULATOR INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED



(Bottom View)

CASE 602A
METAL PACKAGE
G SUFFIX



CASE 614
METAL PACKAGE
R SUFFIX

FIGURE 1 – TYPICAL CIRCUIT CONNECTION
($3.5 \leqslant V_O \leqslant 37$ Vdc, $1 \leqslant I_L \leqslant 500$ mA)

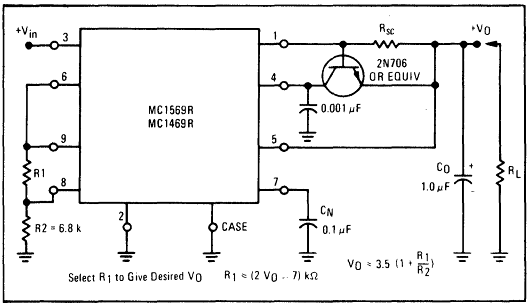


FIGURE 2 – TYPICAL NPN CURRENT BOOST CONNECTION
($V_O = 5.0$ Vdc, $I_L = 10$ Adc [max])

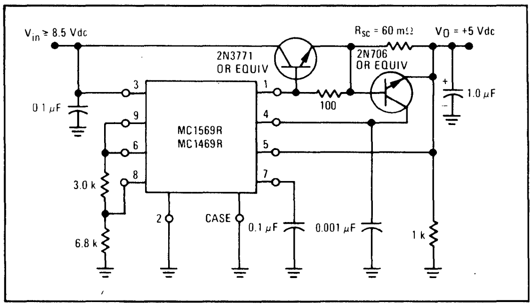
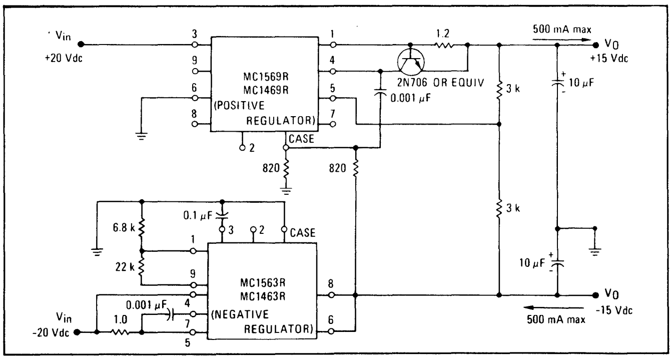
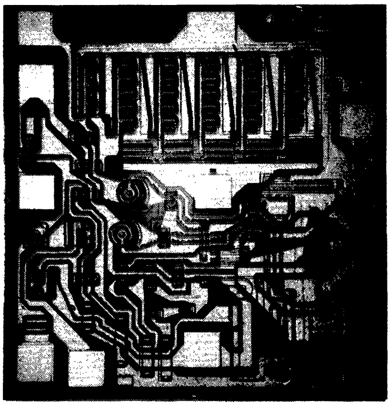


FIGURE 3 – ±15 V, ±400 mA COMPLEMENTARY TRACKING VOLTAGE REGULATOR





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The index to the content of this data sheet appears on page 20.
See current MCC1569/1469 data sheet for standard linear chip information.
See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Input Voltage	V_{in}			Vdc
MC1469		35		
MC1569		40		
		G Package	R Package	
Peak Load Current	I_{PK}	250	600	mA
Current, Pin 2	$I_{pin\ 2}$	10	10	mA
Current, Pin 9	$I_{pin\ 9}$	5.0	5.0	
Power Dissipation and Thermal Characteristics				
T_A = +25°C	P_D	0.68	3.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	5.44	24	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	184	41.6	°C/W
T_C = +25°C	P_D	1.8	17.5	Watts
Derate above T_C = +25°C	$1/\theta_{JC}$	14.4	140	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	69.4	7.15	°C/W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150		°C

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1469		0 to +75	
MC1569		-55 to +125	

ELECTRICAL CHARACTERISTICS

(T_C = +25°C unless otherwise noted) (Load Current = 100 mA for "R" Package device, = 10 mA for "G" Package device, unless otherwise noted)

Characteristic	Fig.	Note	Symbol	MC1569 Min	MC1569 Typ	MC1569 Max	MC1469 Min	MC1469 Typ	MC1469 Max	Unit
Input Voltage (T_A = T_{low} ① to T_{high} ②)	4	1	V_{in}	8.5	–	40	9.0	–	35	Vdc
Output Voltage Range	4,5		V_O	2.5	–	37	2.5	–	32	Vdc
Reference Voltage (Pin 8 to Ground)	4		V_{ref}	3.4	3.5	3.6	3.2	3.5	3.8	Vdc
Minimum Input-Output Voltage Differential (R_{sc} = 0)	4	2	$V_{in} - V_O$	–	2.1	2.7	–	2.1	3.0	Vdc
Bias Current (I_L = 1.0 mAdc, R_2 = 6.8 k ohms, $I_{IB} = I_{in} - I_L$)	4		I_{IB}	–	4.0	9.0	–	5.0	12	mAdc
Output Noise (C_N = 0.1 μF, f = 10 Hz to 5.0 MHz)	4		v_N	–	0.150	–	–	0.150	–	mV(rms)
Temperature Coefficient of Output Voltage	4	3	TCV_O	–	±0.002	–	–	±0.002	–	%/°C
Operating Load Current Range										mAdc
($R_{sc} \leqslant$ 0.3 ohms) R Package	4		I_L	1.0	–	500	1.0	–	500	
($R_{sc} \leqslant$ 2.0 ohms) G Package				1.0	–	200	1.0	–	200	
Input Regulation	6	4	Reg_{in}	–	0.002	0.015	–	0.003	0.030	%/V_O
Load Regulation	7	5	Reg_{load}							
(T_J = Constant [1.0 mA $\leq I_L \leq$ 20 mA])				–	0.4	1.6	–	0.7	2.4	mV
(T_C = +25°C [1.0 mA $\leq I_L \leq$ 50 mA]) R Package				–	0.005	0.05	–	0.005	0.05	%
G Package				–	0.01	0.13	–	0.01	0.13	
Output Impedance (C_c = 0.001 μF, R_{sc} = 1.0 ohm, f = 1.0 kHz, V_{in} = +14 Vdc, V_O = +10 Vdc)	8	6	z_O	–	20	80	–	35	120	milliohms
Shutdown Current (V_{in} = +35 Vdc)	9		I_{sd}	–	70	150	–	140	500	μAdc

① T_{low} = 0°C for MC1469
= -55°C for MC1569

② T_{high} = +75°C for MC1469
= +125°C for MC1569

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Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode. For output voltages greater than approximately 5.5 Vdc the minimum "total instantaneous input voltage" must increase to the extent that it will always exceed the output voltage by at least the "input-output voltage differential".

Note 2. This parameter states that the MC1569/MC1469 will regulate properly with the input-output voltage differential ($V_{in} - V_O$) as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with ($V_{in} - V_O$) as low as 2.1 Vdc as shown in the typical column. (See Figure 21.)

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$\text{MC1569, } TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min})\ (100)}{(180^\circ C)\ (V_O @ 25^\circ C)} = \%/^\circ C$$

$$\text{MC1469, } TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min})\ (100)}{(75^\circ C)\ (V_O @ 25^\circ C)} = \%/^\circ C$$

The output-voltage adjusting resistors (R1 and R2) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. Input regulation is the percentage change in output voltage per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{v_O}{V_O\ (v_{in})}\ 100\ (\%/V_O),$$

where v_O is the change in the output voltage V_O for the input change v_{in}.

The following example illustrates how to compute maximum output voltage change for the conditions given:

$$Reg_{in} = 0.015\ \%/V_O$$
$$V_O = 10\ \text{Vdc}$$
$$v_{in} = 1.0\ \text{V(rms)}$$
$$v_O = \frac{(Reg_{in})\ (v_{in})\ (V_O)}{100} = \frac{(0.015)\ (1.0)\ (10)}{100} = 0.0015\ \text{V(rms)}$$

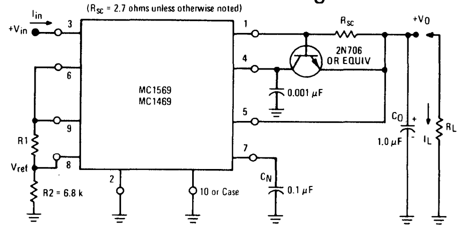
Note 5. Load regulation is specified for small ($\leqslant +17^\circ C$) changes in junction temperature. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{[V_O|I_L = 1.0\text{ mA}] - [V_O|I_L = 50\text{ mA}]}{V_O\,|I_L = 1.0\text{ mA}} \times 100$$

TEST CIRCUITS

FIGURE 4 – CONNECTION FOR $V_O \geqslant 3.5$ Vdc

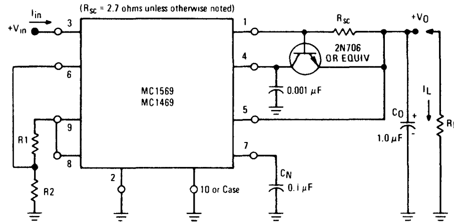
(R_{sc} = 2.7 ohms unless otherwise noted)



Select R1 to give desired V_O: $R1 \approx (2\ V_O - 7)$ k Ω

FIGURE 5 – CONNECTION FOR 2.5 Vdc $\geqslant V_O \leqslant$ 3.5 Vdc

(R_{sc} = 2.7 ohms unless otherwise noted)



Select R2 to give desired V_O: $R2 \approx (2\ V_O)$ k Ω Select R1: $R1 \approx (7.0\text{ k}\Omega - R2)$ k Ω

FIGURE 6 – INPUT REGULATION

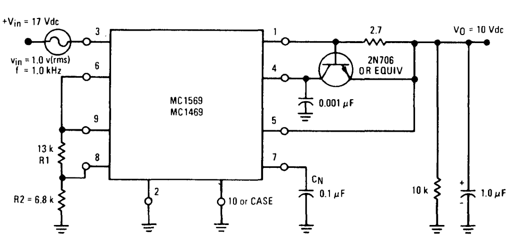


FIGURE 7 – LOAD REGULATION

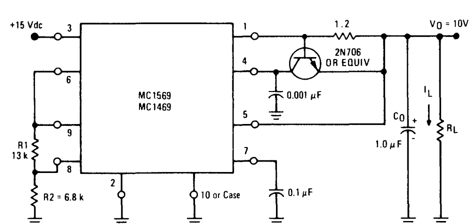


FIGURE 8 – OUTPUT IMPEDANCE

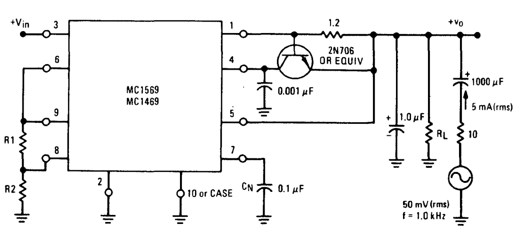
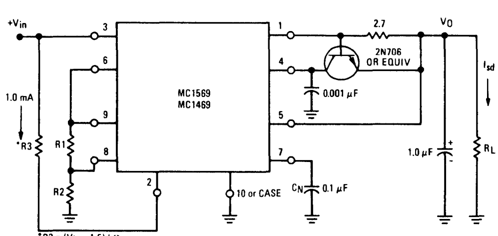


FIGURE 9 – SHUTDOWN CURRENT



*R3 = (V_{in} - 1.5) kΩ

GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
   a) For $V_O \geqslant 3.5$ Vdc – Output voltage is set by resistors R1 and R2 (see Figure 4). Set R2 = 6.8 k ohms and determine R1 from the graph of Figure 10 or from the equation:
   $$R1 \approx (2\,V_O - 7)\ k\Omega$$
   b) For $2.5 \leqslant V_O \leqslant 3.5$ Vdc – Output voltage is set by resistors R1 and R2 (see Figure 5). Resistors R1 and R2 can be determined from the graph of Figure 11 or from the equations:
   $$R2 \approx 2\,(V_O)\ k\Omega$$
   $$R1 \approx (7\ k\Omega - R2)\ k\Omega$$
   c) Output voltage, V_O, is determined by the ratio of R1 and R2, therefore optimum temperature performance can be achieved if R1 and R2 have the same temperature coefficient.
   d) Output voltage can be varied by making R1 adjustable as shown in Figure 43.
   e) If V_O = 3.5 Vdc (to supply MRTL*for example), tie pins 6, 8 and 9 together. R1 and R2 are not needed in this case.
2. Short Circuit Current, I_{sc}
   Short Circuit Current, I_{sc}, is determined by R_{sc}. R_{sc} may be chosen with the aid of Figure 12 or the expression:
   $$R_{sc} \approx \frac{0.6}{I_{sc}}\ \text{ohm}$$
   where I_{sc} is measured in amperes. This expression is also valid when current is boosted as shown in Figures 2, 29 and 30.
3. Compensation, C_c
   A 0.001 μF capacitor, C_c, from pin 4 to ground will provide adequate compensation in most applications, with or without current boost. Smaller values of C_c will reduce stability and larger values of C_c will degrade pulse response and output impedance versus frequency. The physical location of C_c should be close to the MC1569/MC1469 with short lead lengths.
4. Noise Filter Capacitor, C_N
   A 0.1 μF capacitor, C_N, from pin 7 to ground will typically reduce the output noise voltage to 150 μV(rms). The value of C_N can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of 0.001 μF is recommended.
5. Output Capacitor, C_O
   The value of C_O should be at least 1.0 μF in order to provide good stability. The maximum value recommended is a function of current limit resistor R_{sc}:
   $$C_O\ \text{max} \approx \frac{250\ \mu F}{R_{sc}}$$
   where R_{sc} is measured in ohms. Values of C_O greater than this will degrade the pulse response characteristics and increase the settling time.
6. Shut-Down Control
   One method of turning "OFF" the regulator is to apply a dc voltage at pin 2. This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting (see Figures 34, 39 and 40). As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at Pin 2 will cause automatic shut-down for high junction temperatures (see Figure 39). This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard logic levels of MRTL , MDTL or MTTL can also be used to turn the regulator "ON" or "OFF".

8

7. Remote Sensing
   The connection to pin 5 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on z_O can be greatly reduced (see Figure 37).

FIGURE 10 – R1 versus V_O
($V_O \geqslant 3.5$ Vdc, See Figure 4)

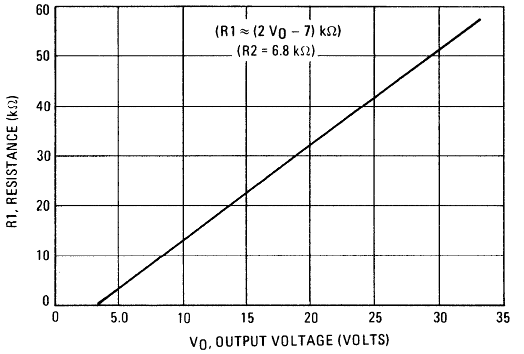


FIGURE 11 – R1 and R2 versus V_O
($2.5 \leqslant V_O \leqslant 3.5$ Vdc, See Figure 5)

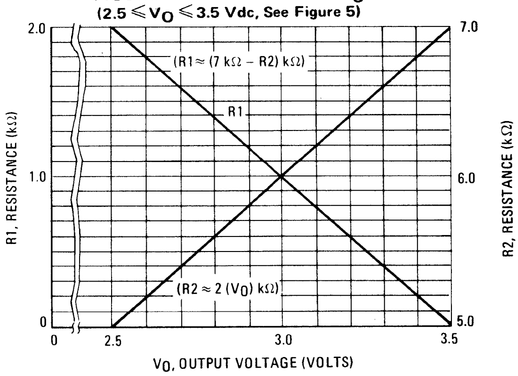
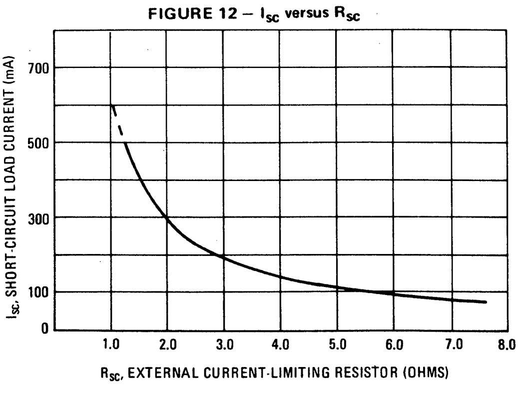


FIGURE 12 – I_{sc} versus R_{sc}



TYPICAL CHARACTERISTICS

Unless otherwise noted: C_N = 0.1 μF, C_c = 0.001 μF, C_O = 1.0 μF, T_C = +25°C,
V_{in} nom = +9.0 Vdc, V_O nom = +5.0 Vdc,
I_L > 200 mA for R package only.

FIGURE 13 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

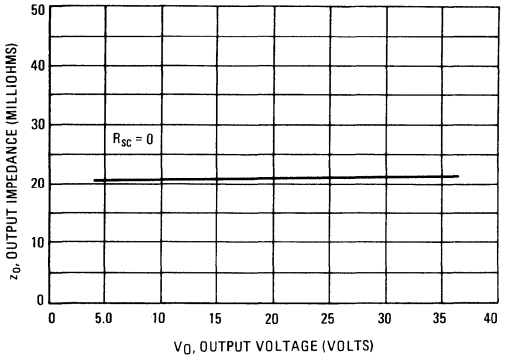


FIGURE 14 – OUTPUT IMPEDANCE versus R_{sc}

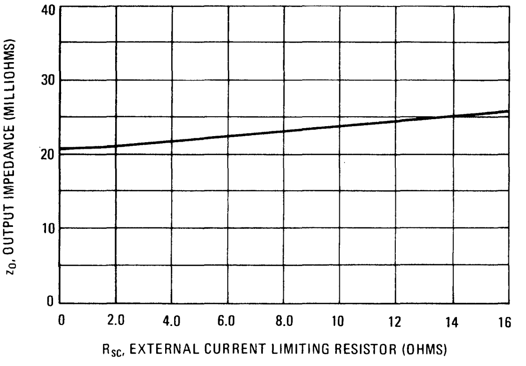


FIGURE 15 – FREQUENCY DEPENDENCE OF INPUT REGULATION, C_O = 10 μF

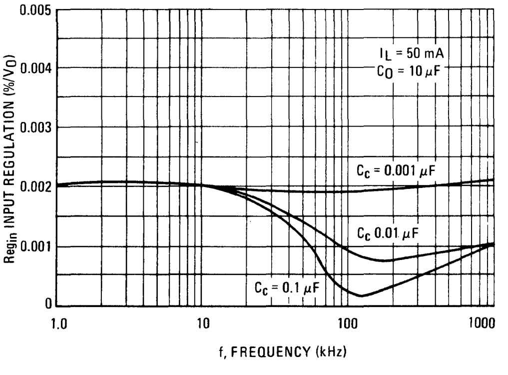


FIGURE 16 – FREQUENCY DEPENDENCE OF INPUT REGULATION, C_O = 2.0 μF

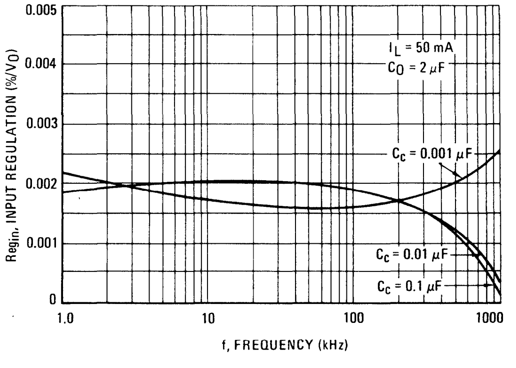


FIGURE 17 – CURRENT-LIMITING CHARACTERISTICS

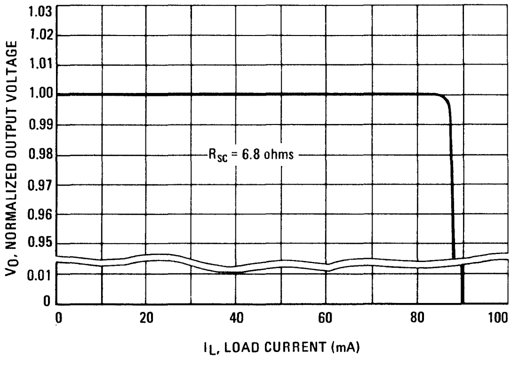
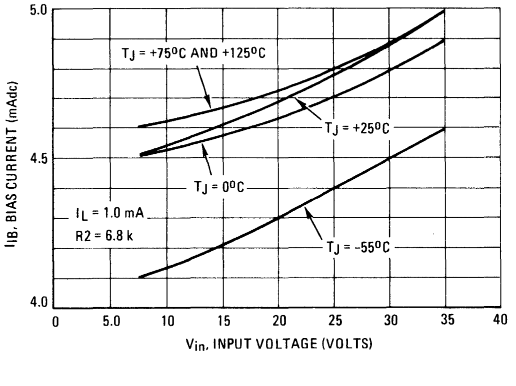


FIGURE 18 – BIAS CURRENT versus INPUT VOLTAGE



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TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted: C_N = 0.1 μF, C_c = 0.001 μF, C_O = 1.0 μF, T_C = +25°C,
V_{in} nom = +9.0 Vdc, V_O nom = +5.0 Vdc,
I_L > 200 mA for R package only.

FIGURE 19 – EFFECT OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

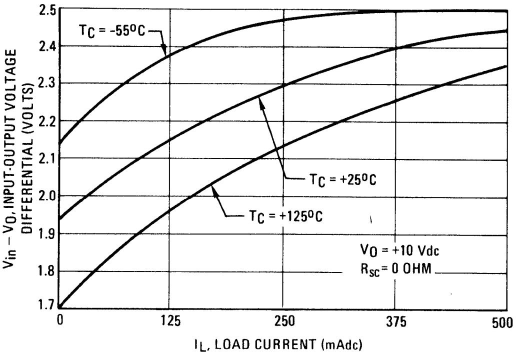


FIGURE 20 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

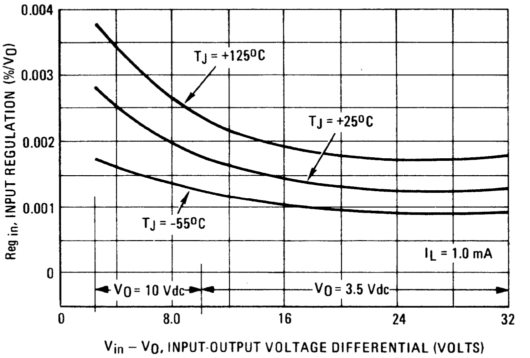


FIGURE 21 – INPUT TRANSIENT RESPONSE

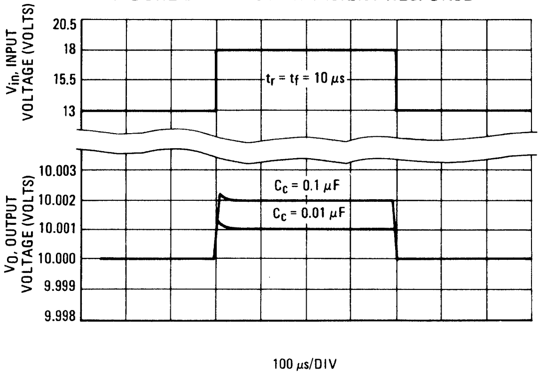


FIGURE 22 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

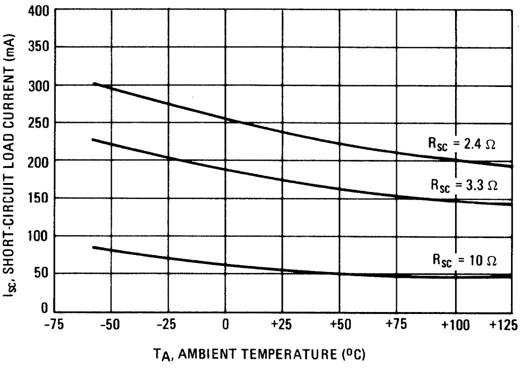


FIGURE 23 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, C_O = 10 μF

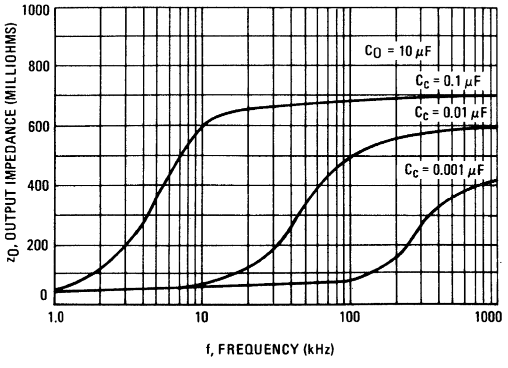
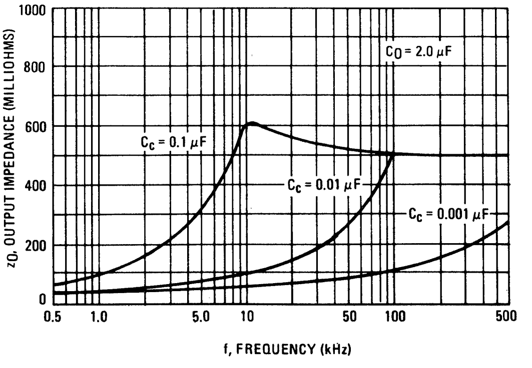


FIGURE 24 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, C_O = 2.0 μF



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OPERATIONS AND APPLICATIONS

This section describes the operation and design of the MC1569 positive voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 25, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 26. The gain-determining resistors may be external, enabling a wide range of output voltages. This is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1569) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1569 positive-voltage regulator.

FIGURE 25 – SERIES VOLTAGE REGULATOR

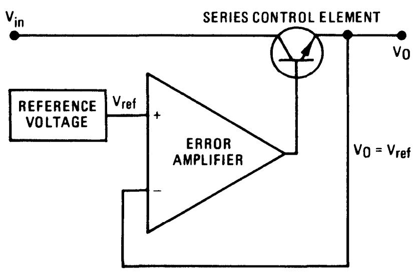


FIGURE 26 – THE "REGULATOR-WITHIN-A-REGULATOR" APPROACH

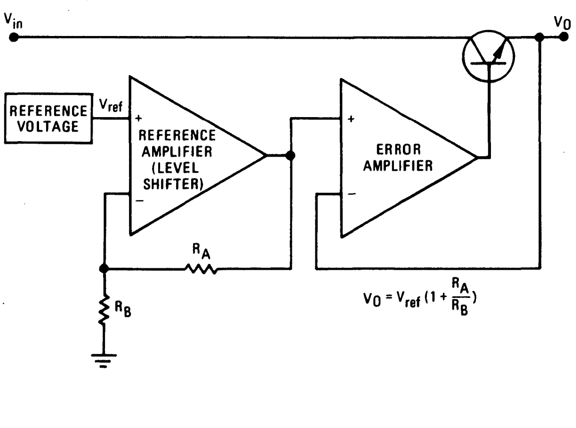
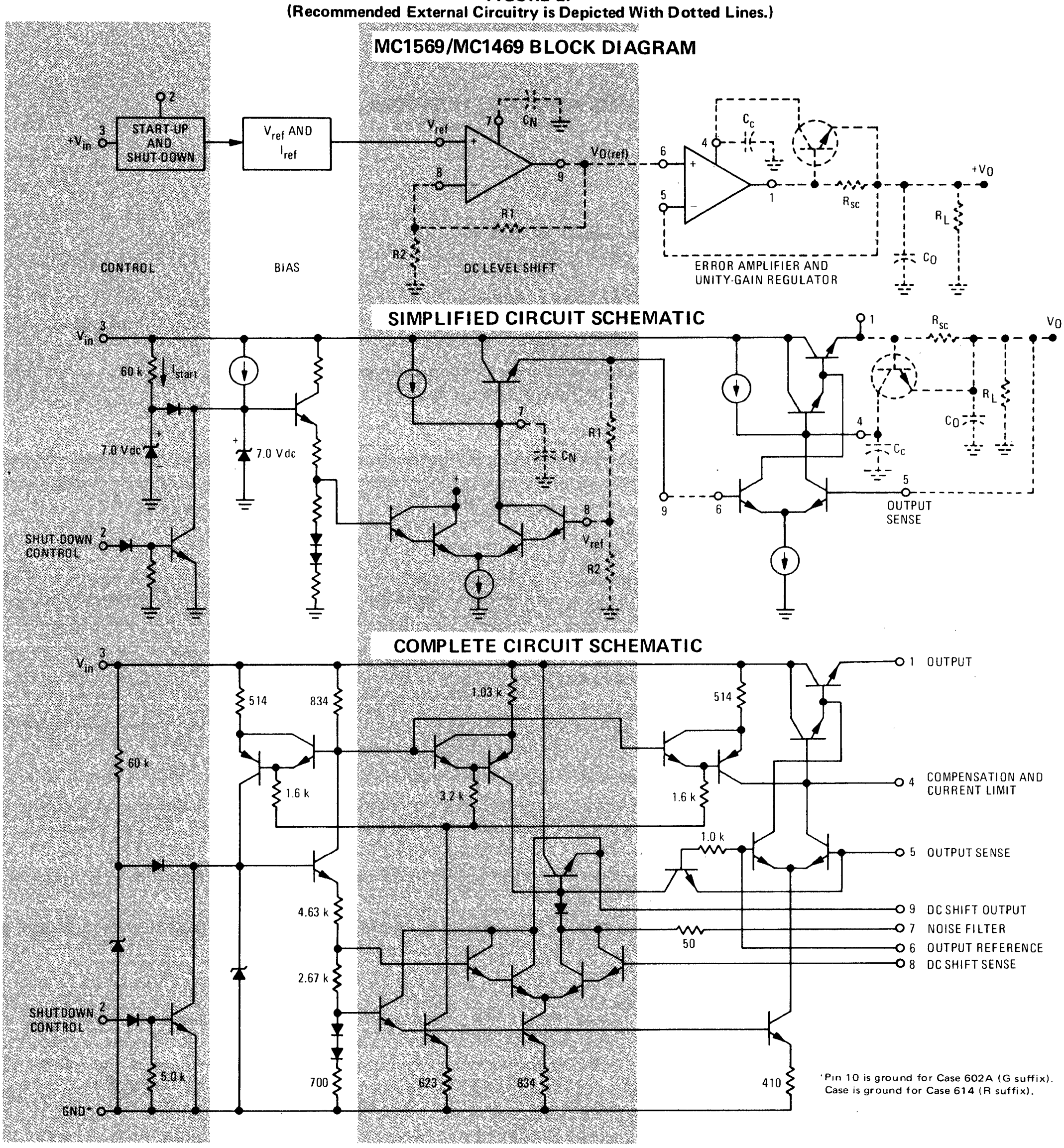


FIGURE 27
(Recommended External Circuitry is Depicted With Dotted Lines.)



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MC1569 Operation

Figure 27 shows the MC1569 Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

The shutdown control consists of an NPN transistor across the reference zener diode. When this transistor is turned "ON", via pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to V_{in}/60 kΩ or 500 μA for a 30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately 3.5 Vdc with a typical temperature coefficient of 0.002 %/°C. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R1 and R2) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_N, is introduced externally into the level shift network (via pin 7) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is 0.1 μF and should have a voltage rating in excess of the desired output voltage. Smaller capacitors (0.001 μF minimum) may be used but will cause a slight increase in output noise. Larger values of C_N will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the level shift amplifier (pin 9) is fed to the noninverting input (pin 6) of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (pin 5) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{SC}, is connected in the emitter of this transistor to sample the full load current. By placing an external low-level NPN transistor across R_{SC} as shown in Figure 27, output current can be limited to a predetermined value:

$$I_L \max \approx \frac{0.6}{R_{SC}} \text{ or } R_{SC} = \frac{0.6}{I_L \max}$$

where I_L max is the maximum load current (amperes) and R_{SC} is the value of the current limiting resistor (ohms).

Stability and Compensation

As has been seen, the MC1569 employs two amplifiers, each using negative feedback. This implies the possibility of instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (pin 4) and ground. The recommended value of 0.001 μF will insure stability and still provide acceptable transient response (see Figure 28, A and B). It is also necessary to use an output capacitor, C_O (typically 1.0 μF) from the output, V_O, to ground. When an external transistor is used to boost the current, C_O = 1.0 μF is also recommended (see Figure 2).

FIGURE 28A – LOAD TRANSIENT RESPONSE

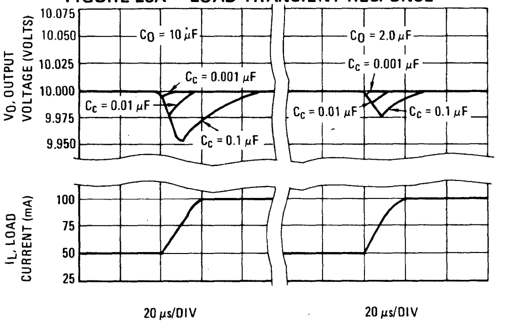
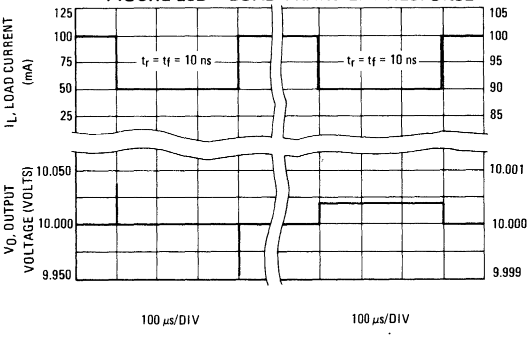
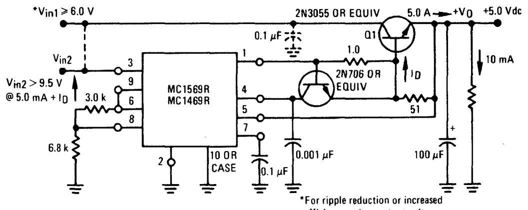


FIGURE 28B – LOAD TRANSIENT RESPONSE



TYPICAL NPN CURRENT BOOST CONNECTIONS

FIGURE 29A – 5 VOLT 5-AMPERE REGULATOR



*For ripple reduction or increased efficiency at low output voltages, the collector of Q1 can tie to a separate low-voltage supply as shown.

FIGURE 29B – 5-VOLT 5-AMPERE REGULATOR

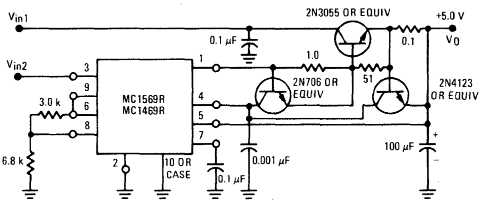
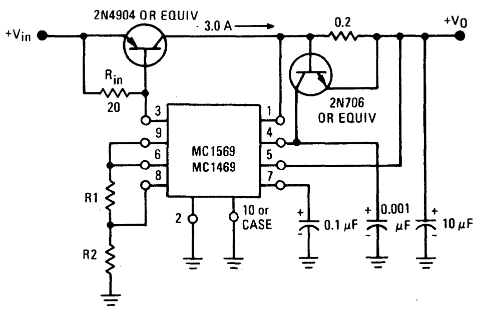


FIGURE 30 – PNP CURRENT BOOST CONNECTION



NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 2 or 29 are recommended. The transistor shown in Figure 29A, the 2N3055 can supply currents to 5.0 amperes (subject, of course, to the safe area limitations). To improve the efficiency of the NPN boost configuration, particularly for small output voltages, the circuit of Figure 29 is recommended. An auxiliary 9.5-volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 5.0 ampere regulator of Figure 29 this represents a savings of 17.5 watts when compared with operating the regulator from the single 9.5 V supply. It can supply current to 5.0 amperes while requiring an input voltage to the collector of the pass transistor of 6.0 volts minimum. The pass transistor is limited to 5.0 amperes by the added short-circuit current network in its emitter (R_{SC}), (Figure 29B).

PNP CURRENT BOOSTING

A typical PNP current boost circuit is shown in Figure 30. Voltages from 2.5 Vdc to 37 Vdc and currents of many amperes can be obtained with this circuit.

Since the PNP transistor must not be turned on by the MC1569 bias current (I_{IB}) the resistor R_{in} must meet the following condition

$$R_{in} < \frac{V_{BE}}{I_{IB}}$$

where V_{BE} is the base-to-emitter voltage required to turn on the PNP pass transistor, (typically 0.6 Vdc for silicon and 0.2 Vdc for germanium).

For germanium pass transistors, a silicon diode may be placed in series with the emitter to provide an additional voltage drop. This allows a larger value of R_{in} than would be possible if the diode were omitted. The diode will, however, be required to carry the maximum load current.

SELF-OSCILLATING SWITCHING REGULATOR

In all of the current boosting circuits shown thus far it has been assumed that the input-output voltage differential can be minimized to obtain maximum efficiency in both the external pass element as well as the MC1569. This may not be possible in applications where only a single supply voltage is available and high current levels preclude zener diode pre-regulating approaches. In such applications a switching-mode voltage regulator is highly desirable since the pass device is either ON or OFF. The theoretical efficiency of an ideal switching regulator is 100%. Realizable efficiencies of 90% are within the realm of possibility thus obviating the need for large power dissipating components. The output voltage will contain a ripple component; however, this can be made quite small if the switching frequency is made relatively high so filtering techniques are effective. Figure 31 shows a functional diagram for a self-oscillating voltage regulator. The comparator-driver will sense the voltage across the inductor, this voltage being related to the load current, I_L, by

$$L\frac{dI_L}{dt} = V.$$

For a first approximation this can be assumed to be a linear relationship.

Initially, V_O will be low and Q1 will be ON. The voltage at the non-inverting input will approach $\beta_1 V_{in}$, when:

$$\beta_1 V_{in} = \frac{V_{ref}R_a}{R_a + R_b} + \frac{V_c R_b}{R_a + R_b}.$$

When this output voltage is reached the comparator will switch, turning Q1 OFF. The diode, CR1, will now become forward biased and will supply a path for the inductor current. This current and the sense voltage will start to decrease until the output voltage reaches

$$\beta_2 V_{in} = \frac{V_{ref}R_a}{R_a + R_b}$$

where the comparator will again switch turning Q1 ON, and the cycle repeats. Thus the output voltage is approximately V_{ref} plus a ripple component.

The frequency of oscillation can be shown to be

$$f = \frac{V_O (V_{in} - V_O)}{L V_C\, I(max) - I_O)} \qquad (1)$$

where

I (max) = The maximum value of inductor current

I_O = The minimum inductor current.

Normally this frequency will be in the range of approximately 2 kHz to 6 kHz. In this range, inductor values can be small and are compatible with the switching times of the pass transistor and diode. The switching time of the comparator is quite fast since positive feedback aids both turn-on and turn-off times. The limiting factors are the diode and pass transistor rise and fall times which should be quite fast or efficiency will suffer.

Figure 32 shows a self oscillating switching regulator which in many respects is similar to the PNP current boost previously discussed. The 6.8 kΩ resistor in conjunction with R1 sets the reference voltage, V_{ref}. Q1 and CR1 are selected for fast switching times as well as the necessary power dissipation ratings. Since a linear inductor is assumed, the inductor cannot be allowed to saturate at maximum load currents and should be chosen accordingly. If core saturation does occur, peak transistor and diode currents will be large and power dissipation will increase.

FIGURE 31 – BASIC SELF-OSCILLATING SWITCHING REGULATOR

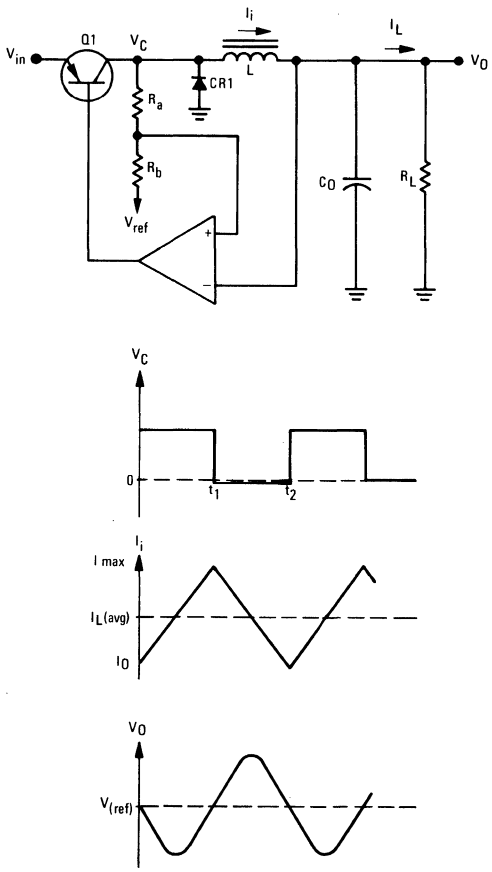
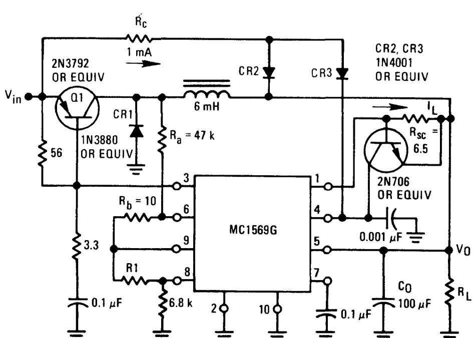


FIGURE 32 – MC1569 SELF-OSCILLATING SWITCHING REGULATOR



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As a design center is required for a practical circuit, assume the following requirements:

V_{in} = +28 Volts

V_O = +10 Volts

ΔV_O = 50 mV

$f \cong 5$ kHz

I(max) = 1.125 A

I_O = 1 A

$$\Delta V \approx V_{in} \frac{R_b}{R_a}. \quad (2)$$

Using Equation (1), the inductor value can be found:

$$L = \frac{(28-10)}{2(1.125-1)} \frac{10}{28} \left(\frac{1}{5 \times 10^3}\right)$$

$$\approx 7 \text{ mH}.$$

For the test circuit, a value of 6 mH was selected. Using for a first approximation

$$C_O = \frac{(V_{in} - V_O)(V_O)}{8L\, f^2\, V_{in}\, (\Delta V)}.$$

$$= \frac{(28 - 10)10}{8(7 \times 10^{-3})(5 \times 10^3)^2 (28)(50 \times 10^{-3})}$$

$$\approx 95\ \mu F.$$

As shown, a value of 100 μF was selected. Since little current is required at pin 6, R_a can be large. Assume R_a = 47 kΩ and then use Equation (2) to determine R_b:

$$50 \times 10^{-3} = \frac{28}{47\ k\Omega} R_b$$

$$R_b = \frac{47}{28} 50 \approx 85\Omega.$$

Since the internal impedance presented by pin 9 is on the order of 60Ω, a value of R_b = 10Ω is adequate.

Diodes CR2, CR3, and R_c may be added to prevent saturation of the error amplifier to increase switching speed. When the output stage of the error amplifier approaches saturation, CR2 becomes forward biased and clamps the error amplifier. Resistor R_c should be selected to supply a total of 1 mAdc to CR2 and CR3.

To show correlation between the predicted and tested specifications the following data was obtained:

V_{in} = +28 (±1%) Volts

V_O = +10 Volts

ΔV_O = 60 mV

f = 7 kHz

@ I_L = 1A

which checks quite well with the predicted values. R_b can be adjusted to minimize the ripple component as well as to trim the operating frequency. Also this frequency will change with varying loads as is normal with this type of circuit. Pin 2 can still be used for shut-down if so desired. R_{SC} should be set such that the ratio of load current to base drive current is 10:1 in this case $I_1 \approx 100$ mA and R_{SC} = 6.5Ω.

POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1569 is driven from a floating source it is possible to use it as a negative regulator by grounding the positive output terminal. The MC1569 may also be used with the MC1563 to provide completely independent positive and negative voltage regulators with comparable performance.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 3 and 33 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (pin 6 of the MC1569) and using the other side (pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3-k ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at pin 5 will be zero. When the voltage at pin 5 equals zero, $+V_O$ must equal $|-V_O|$.

For the configuration shown in Figure 33, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown,

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is not short-circuit protected.) The −15-volt supply varies less than 0.1 mV over a zero to −300 mAdc current range and the +15-volt supply tracks this variation. The +15-volt supply varies 20 mV over the zero to +300 mAdc load current range. The +5-volt supply varies less than 5 mV for $0 \leqslant I_L \leqslant 200$ mA with the other two voltages remaining unchanged. See page 19 for additional information.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1569 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of an NPN transistor; which, if turned "ON", will turn the zener "OFF" and deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60-k-ohm start resistor (V_{in}/60 kΩ). This feature provides additional versatility in the applications of the MC1569. Various subsystems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as overheating, over-voltage, shorted output, etc.

To activate shutdown, one simply applies a potential greater than two diode drops with a current capability of 1 mA. Note that if a hard supply (i.e., +3 V) is applied directly to pin 2, the shutdown circuitry will be destroyed since there is no inherent current limiting. Maximum rating for the drive current into pin 2 is 10 mA, while 1 mA is adequate for shutdown.

FIGURE 33 – A ±15 Vdc COMPLEMENTARY TRACKING REGULATOR WITH AUXILIARY +5.0 V SUPPLY

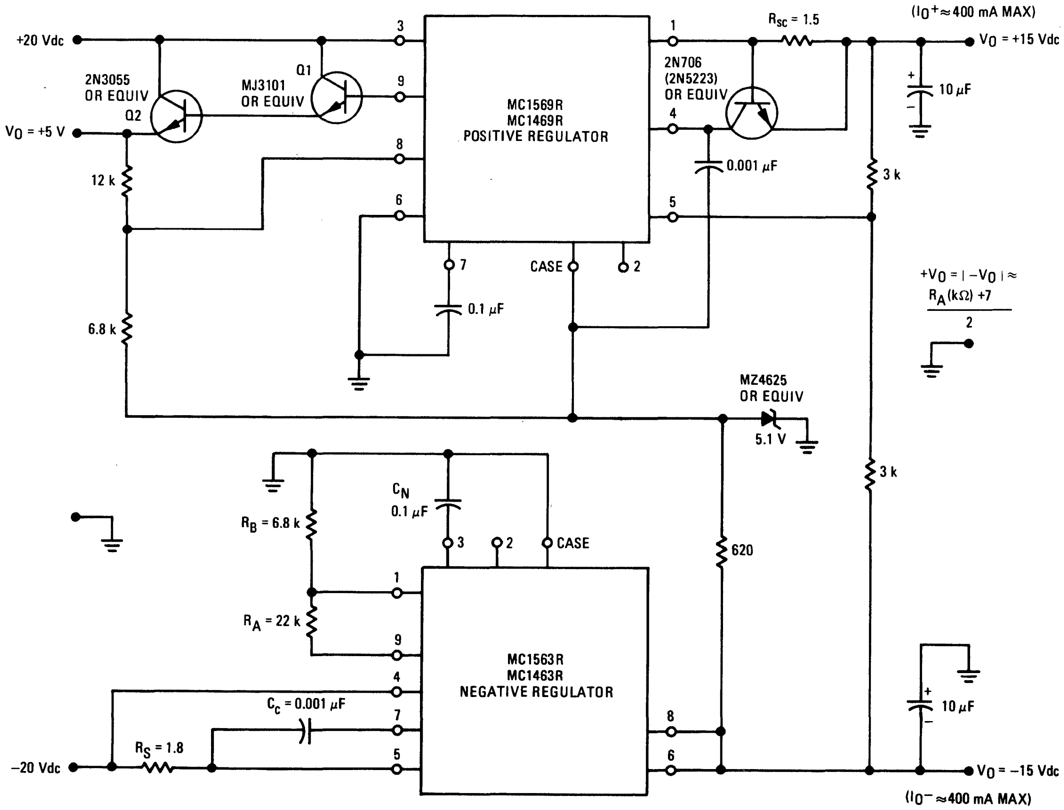

FIGURE 34 – ELECTRONIC SHUT-DOWN USING A MDTL GATE

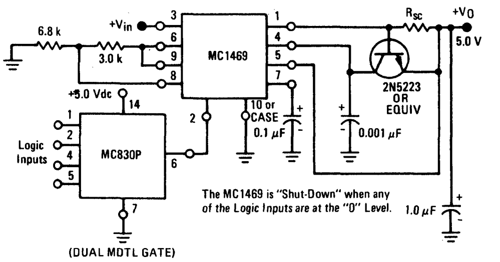

FIGURE 35 – AUTOMATIC LATCH INTO SHUT-DOWN WHEN OUTPUT IS SHORT-CIRCUITED WITH MANUAL RE-START

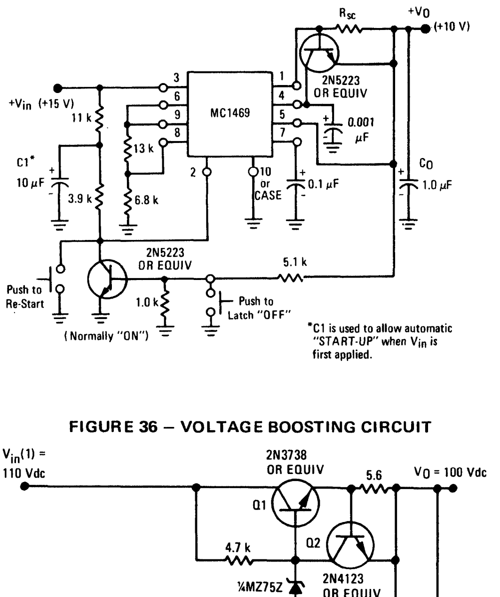

FIGURE 36 – VOLTAGE BOOSTING CIRCUIT

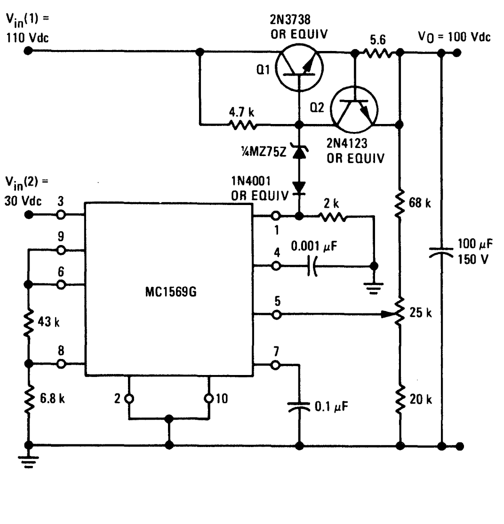

Figure 34 shows how the regulator can be controlled by a logic gate. Here, it is assumed that the regulator operates in its normal mode – as a positive regulator referenced to ground – and that the logic gate is of the saturating type, operating from a positive supply to ground. The high logic level should be greater than about 1.5 V and should source no more than 10 mA into pin 2.

The gate shown is of the MDTL type. MRTL and MTTL can also be used as long as the drive current is within safe limits (this is important when using MTTL, where the output stage uses an active pull-up).

In some cases a regulator can be designed which can handle the power dissipation resulting from normal operation but cannot safely dissipate the power resulting from a sustained short-circuit. The circuit of Figure 35 solves this problem by shutting down the regulator when the output is short-circuited.

VOLTAGE BOOSTING

The MC1569 has a maximum output voltage capability of 37 volts which covers the bulk of the user requirements. However, it is possible to obtain higher output voltages. One such voltage boosting circuit is shown in Figure 36.

Since high voltage NPN silicon devices are readily available, the only problem is the voltage limitations of the MC1569. This can be overcome by using voltage shift techniques to limit the voltage to 35 volts across the MC1569 while referencing to a higher output voltage.

The zener diode in the base lead of the NPN device is used to shift the output voltage of the MC1569 by approximately 75 volts to the desired high voltage level, in this case 100 volts. Another voltage shift is accomplished by the resistor divider on the output to accommodate the required 25 volt reference to the MC1569. The 2 kΩ resistor is used to bias the zener diode so the current through the 4.7 kΩ resistor can be controlled by the MC1569. The 1N4001 diode protects the MC1569 from supplying load current under short circuit conditions and Q2 serves to limit base current to Q1. For R_{SC} as shown, the short circuit current will be approximately 100 mA.

In order to use a single supply voltage, $V_{in}(2)$ can be derived from $V_{in}(1)$ with a zener diode, shunt pre-regulator.

It can be seen that loop gain has been reduced by the resistor divider and hence the closed loop bandwidth will be less. This of course will result in a more stable system, but regulator performance is degraded to some degree.

REMOTE SENSING

The MC1569 offers a remote sensing capability. This is important when the load is remote from the regulator,

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as the resistance of the interconnecting lines (V_O and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 37 shows how remote sensing is accomplished using both a separate sense line from pin 8 and a separate ground line from the regulator to the remote load.

AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE.

The MC1569, when used in conjunction with low TC resistors, makes an excellent reference-voltage generator. If the 3.5 volt reference voltage of the IC regulator is a satisfactory value, then pins 8 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, R1 and R2, any voltage between 3.5 Vdc and 37 Vdc can be obtained with the same low TC (see Figure 38).

THERMAL SHUTDOWN

By setting a fixed voltage at pin 2, the MC1569 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor and the diode in series with pin 2 (-3.4×10^{-3}V/°C). By setting 1.0 Vdc externally at pin 2, the regulator will shutdown when the chip temperature reaches approximately +140°C. Figure 39 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

FIGURE 37 – REMOTE SENSING CIRCUIT

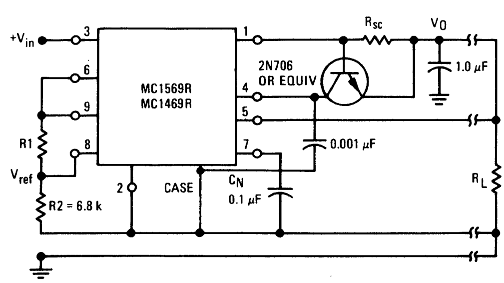
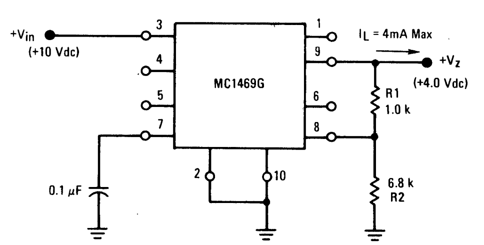


FIGURE 38 – AN ADJUSTABLE "ZERO-TC" VOLTAGE SOURCE



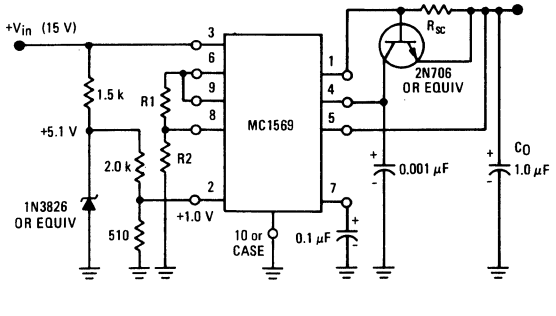
$V_Z = (1 + \frac{R1}{R2})3.5$

FIGURE 39 – JUNCTION TEMPERATURE LIMITING SHUTDOWN CIRCUIT

FIGURE 39A – USING A ZERO TC REFERENCE

FIGURE 39B – USING A T_A REFERENCE

$V_{pin\ 2\ (for\ shutdown)} \approx 1.38 - 3.4 \times 10^{-3} (T_J - 25°C)$



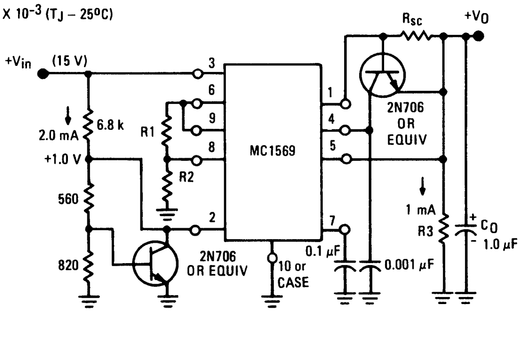


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FIGURE 40 – THERMAL SHUTDOWN WHEN USING EXTERNAL PASS TRANSISTORS

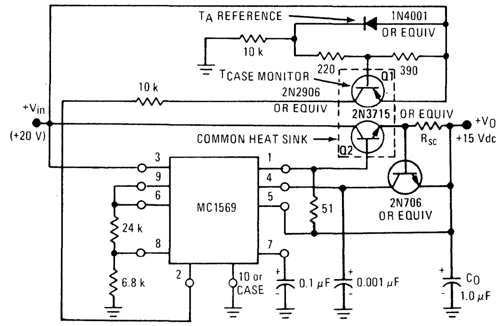
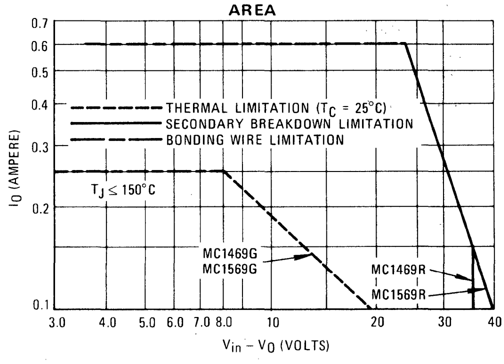


FIGURE 41 – DC SAFE OPERATING AREA



In the case where an external pass transistor is employed, its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 40. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application, the designer must use caution not to exceed the specified maximum junction temperature (+150°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current. Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 41).

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically −0.06%/watt for the MC1569. For an example of the relative magnitudes of these effects, consider the following conditions:

Given MC1569

with V_{in} = 10 Vdc

V_O = 5 Vdc

8

and I_L = 100 mA to 200 mA

$(\Delta I_L = 100\ \text{mA})$

assume $T_A = +25°C$

TO-66 Case with heatsink

assume $\theta_{CS} = 0.2°C/W$

and $\theta_{SA} = 2°C/W$

$\theta_{JC} = 7.15°C/W$ (from maximum ratings table)

It is desired to find the ΔV_O which results from this ΔI_L. Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_O due to ΔT_J

$$\Delta V_O = (V_O)(\Delta P_D)(TCV_O)(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

OR

$$\Delta V_O = (5V)(5\ \text{V} \times 0.1\text{A})(\pm 0.002\%/°C)(9.35°C/W)$$

$$\Delta V_O \approx \pm 0.5\ \text{mV}$$

2. ΔV_O due to z_O

$$|\Delta V_O| = (-z_O)(I_L)$$

$$|\Delta V_O| = -(2 \times 10^{-2})(10^{-1}) = -2\ \text{mV}$$

3. ΔV_O due to gradient coefficient, GCV_O

$$|\Delta V_O| = (GCV_O)(V_O)(\Delta P_D)$$

$$|\Delta V_O| = (-6 \times 10^{-4}/W)(5\ \text{volts})(5 \times 10^{-1}W)$$

$$|\Delta V_O| = -1.6\ \text{mV}$$

Therefore the total ΔV_O is given by

$$|\Delta V_O\ \text{total}| = \pm 0.5 - 2.0 - 1.6\ \text{mV}$$

OR

$$-4.1\ \text{mV} \leqslant |V_O\ \text{total}| \leqslant -3.1\ \text{mV}$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT

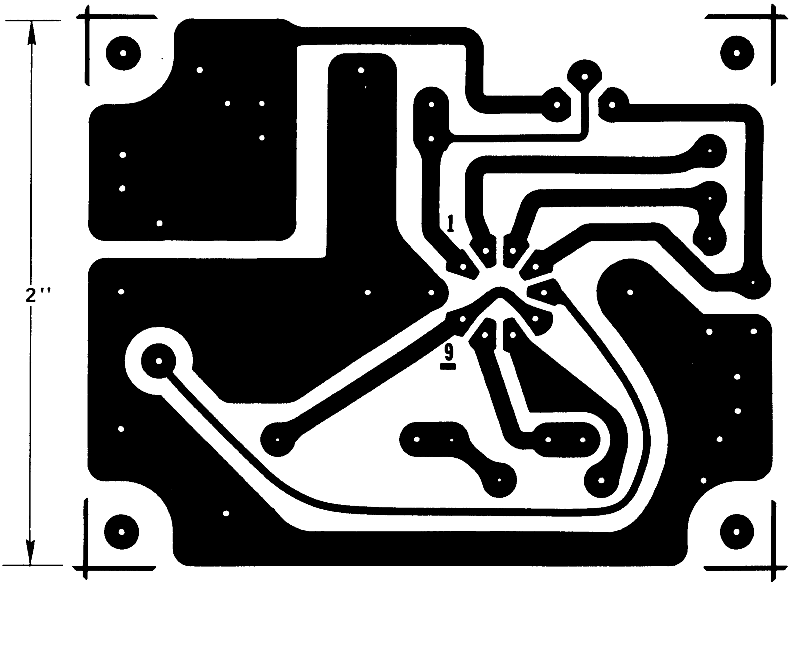


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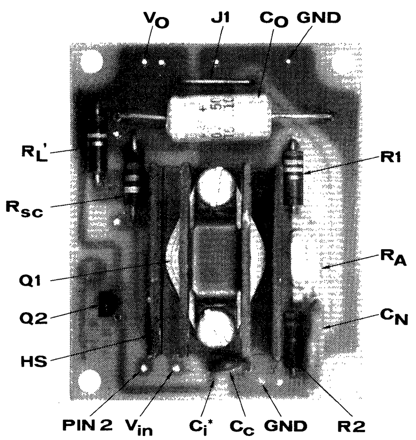
FIGURE 42 – LOCATION OF COMPONENTS



*C_i not shown

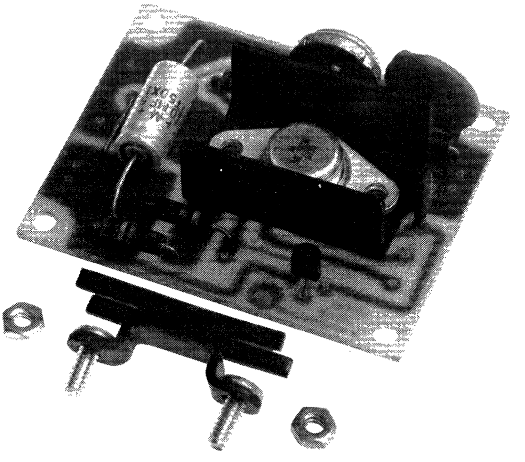
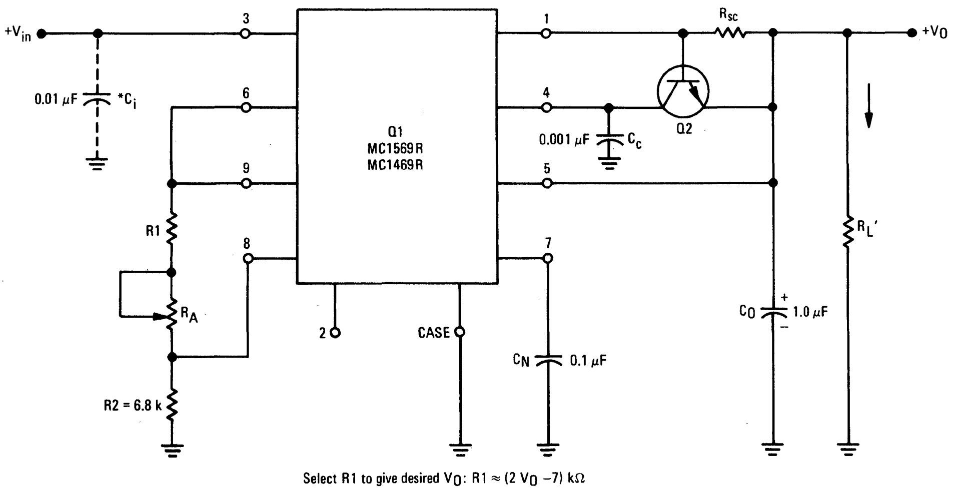


FIGURE 43 – CIRCUIT SCHEMATIC FOR PRINTED CIRCUIT BOARD (Pg. 17)
$3.5\ V \leq V_O \leq 37\ V$, $1\ mA \leq I_L \leq 500\ mA$



Select R1 to give desired V_O: $R1 \approx (2\ V_O - 7)\ k\Omega$

*C_i – May be required if long input leads are used.

PARTS LIST

Component	Value	Description
R1 R2	Select 6.8 k	1/4 or 1/2 watt carbon
$^*R_A$	Select	IRC Model X-201 Mallory Model MTC-1 or equivalent
R_{sc}	Select	1/2 watt carbon
$^*R_L'$	Select	For minimum current of 1 mAdc
C_O	1.0 μF	Sprague 1500 Series, Dickson D10C series or equivalent
C_N C_c $^*C_i$	0.1 μF 0.001 μF 0.01 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or equivalent
Q1 Q2	MC1569R or MC1469R 2N5223, 2N706, or equivalent	
*HS	–	Heatsink Thermalloy #6168B
*Socket	(Not Shown)	Robinson Nugent #0001306 Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1
PC Board	–	Circuit Dot, Inc. #PC1113 1155 W. 23rd St., Tempe, Ariz. 85281
*Optional		

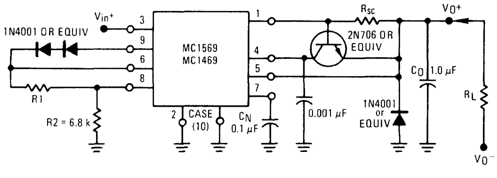
LATCH-UP

Latch-up of these and other regulators can occur if:

1. There are plus and minus voltages available
2. A load exists between V_O^+ and V_O^- (This "common load" may be something inconspicuous – e.g. an operational amplifier. Nearly everyone who uses + and – voltages will have a common load from V_{CC} to V_{EE}.)
3. V_{in}^+ and V_{in}^- are not applied at the same time.

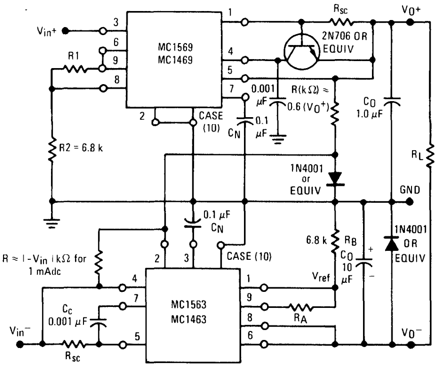
The above conditions result in one of the two outputs becoming reverse-biased which prevents the regulator from turning ON . Latch-up can be prevented by the circuit configurations shown in Figures 44 and 45.

FIGURE 44



Note: This configuration increases minimum input-output differential voltage by ≈ 0.7 V.

FIGURE 45



INDEX

MC1585L

DUAL CLOCK DRIVER

DUAL MOS CLOCK DRIVER

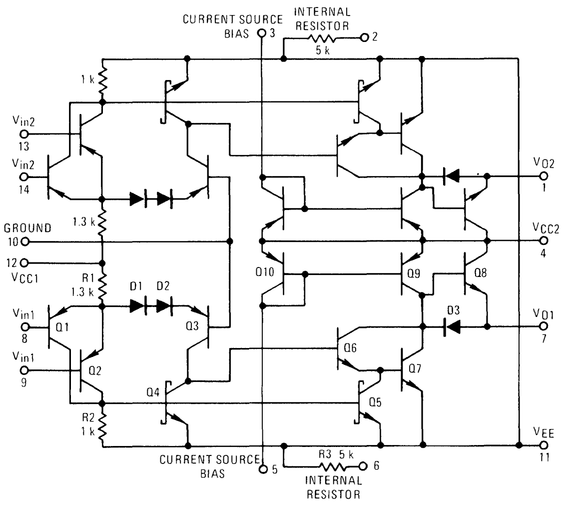
. . . designed for high-speed driving of highly capacitive loads in a MOS system.

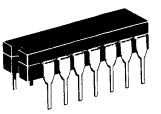
- High Output Current (±400 mA peak)
- MDTL, MTTL Compatible Input
- Output Compatible with High and Low Threshold P-Channel MOS Devices

DUAL MOS CLOCK DRIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT

FIGURE 1 – CIRCUIT SCHEMATIC





CERAMIC PACKAGE
CASE 632
TO-116

TYPICAL OPERATION

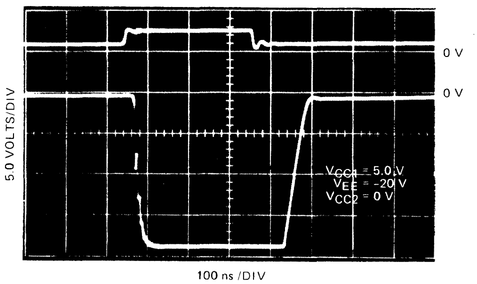
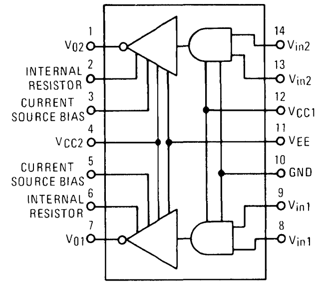


FIGURE 2



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Voltage Supply Range 1 (See Figure 3)	V_{R1}	10	Vdc
Voltage Supply Range 2 (See Figure 3)	V_{R2}	30	Vdc
Voltage Supply Range 3 (See Figure 3)	V_{R3}	22	Vdc
Input Voltage	$V_{in(max)}$	10	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Temperature Range	T_A	-55 to +125	°C
Power Dissipation Ceramic Package Derate above T_A = +25°C	P_D $1/\theta_{JA}$	 1000 6.7	 mW mW/°C

FIGURE 3 – SUPPLY VOLTAGE RANGE DEFINITION

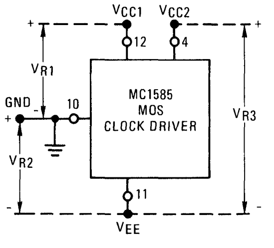
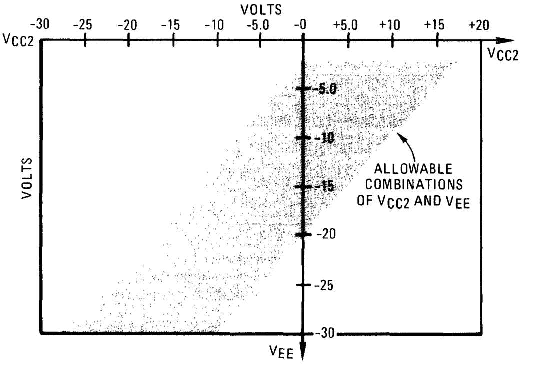


FIGURE 4 – ALLOWABLE VALUES FOR V_{CC2} AND V_{EE}



SWITCHING CHARACTERISTICS (C_L = 1000 pF, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time, Low to High Level	t_{PLH}	–	75	125	ns
Transition Time, Low to High Level	t_{TLH}	–	75	125	ns
Propagation Delay Time, High to Low Level	t_{PHL}	–	50	75	ns
Transition Time, High to Low Level	t_{THL}	–	50	75	ns

The above characteristics were measured with V_{CC1} = 5.0 volts, V_{EE} = -20 volts, V_{CC2} = 0 volts, and C_L = 1000 pF. The switching times are measured as shown in Figure 5.

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FIGURE 5 – SWITCHING TIME WAVEFORM

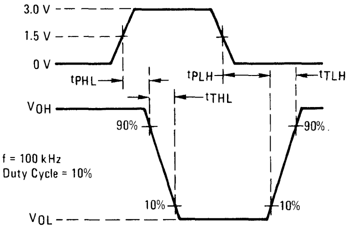
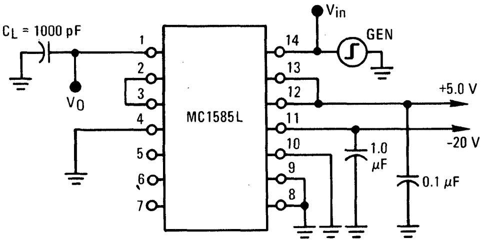


FIGURE 6 – AC TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)
(Pin 2 is shorted to pin 3 and pin 5 is shorted to pin 6.)

							TEST CURRENT AND VOLTAGE VALUES								
						Function	Load Currents		Input Voltages		Supply Voltages				
						Symbol	I_{OH}	I_{OL}	V_{IL}	V_{IH}	V_{CC1L}	V_{CC1H}	V_{EE}	V_{CC2}	
						Unit	mA		Volts						
		Pin Under	Test Limits			Value	-1.0	+1.0	1.1	1.78	4.5	5.5	-15	+5.0	
Characteristic	Symbol	Test	Min	Typ	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:								GND
Input Currents: Forward	I_{IL}	8	–	–	-1.6	mA	–	–	8	9	–	12	11	4	10
Reverse Leakage	I_{IH}	8	–	–	+50	μA	–	–	–	8,9	–	12	11	4	10
Output Voltage: High Output	V_{OH}	7	+3.7	–	–	Volts	7	–	8	9	12	–	11	4	10
Low Output	V_{OL}	7	–	–	-13.4	Volts	–	7	–	8,9	–	12	11	4	10
Supply Current V_{CC1} High Output	I_{CC1H}	12	–	–	+10	mA	–	–	8,13	9,14	–	12	11	4	10
V_{CC1} Low Output	I_{CC1L}	12	–	–	+7.0	mA	–	–	–	8,9,13,14	–	12	11	4	10
V_{EE} High Output	I_{EEH}	11	–	–	-25	mA	–	–	8,13	9,14	–	12	11	4	10
V_{EE} Low Output	I_{EEL}	11	–	–	-64	mA	–	–	–	8,9,13,14	–	12	11	4	10
V_{CC2} High Output	I_{CC2H}	4	–	–	+15	mA	–	–	8,13	9,14	–	12	11	4	10
V_{CC2} Low Output	I_{CC2L}	4	–	–	+57	mA	–	–	–	8,9,13,14	–	12	11	4	10

TYPICAL CHARACTERISTICS

FIGURE 7 – PACKAGE LIMITATION ON POWER DISSIPATION

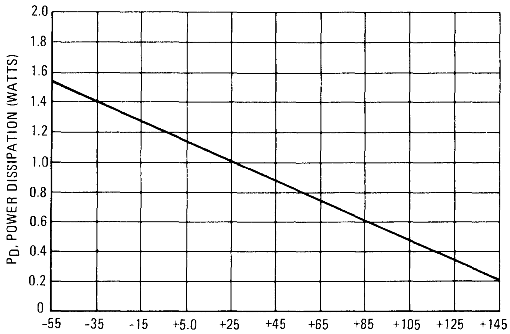


FIGURE 8 – MAXIMUM DIFFERENTIAL LEVEL SHIFT POWER DISSIPATION (WITH BOTH INPUTS HIGH)

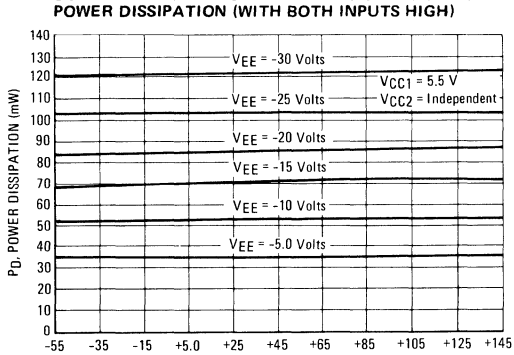
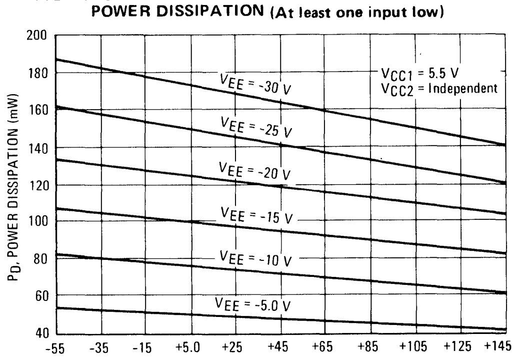


FIGURE 9 – MAXIMUM DIFFERENTIAL LEVEL SHIFT POWER DISSIPATION (At least one input low)



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TYPICAL CHARACTERISTICS (cont.)

FIGURE 10 – MAXIMUM BIAS CURRENT versus VOLTAGE AND TEMPERATURE WHEN USING INTERNAL BIAS RESISTOR

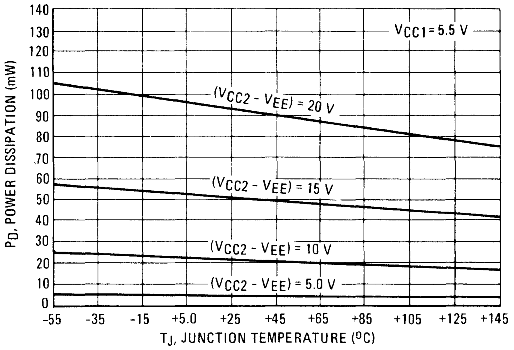


FIGURE 11 – MAXIMUM POWER DISSIPATION OF INTERNAL RESISTOR (R3)

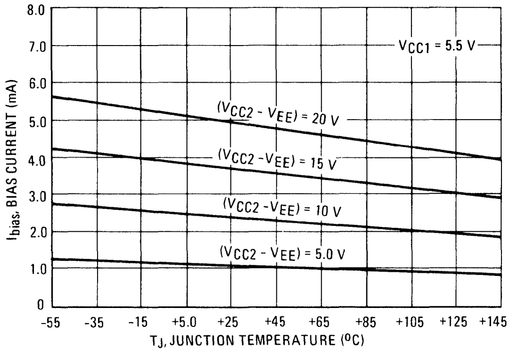


FIGURE 12 – MAXIMUM BIAS POWER DISSIPATION IN Q9, Q10 (INDEPENDENT OF OUTPUT STATE)

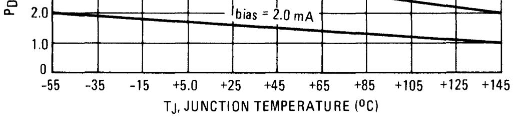
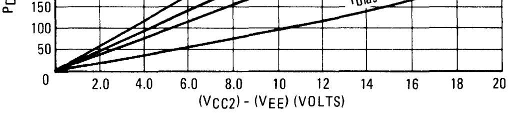


FIGURE 13 – POWER DISSIPATION OF OUTPUT CURRENT OF ACTIVE PULLUP versus BIAS CURRENT versus VOLTAGE



APPLICATIONS INFORMATION

8

The total power dissipation in the MOS clock driver is the sum of a dc and an ac component. The total of these components must not exceed the package power dissipation limit at the maximum temperature of operation. The package limitation on power dissipation is shown in Figure 7.

AC Power Dissipation

The ac component of power dissipation is given in equation 1.

$$P_{ac} = C_L \cdot [(V_{CC2})-(V_{EE})]^2 (PRR) \qquad (1)$$

where C_L is the load capacitance and PRR is the pulse repetition rate.

DC Power Dissipation

For ease of calculation, the dc power dissipation is divided into two parts: 1) differential level shift power 2) output pullup current source power.

Differential Level Shift Power

In Figure 1 it may be seen that the differential level shift consists of the input PNP transistors, Q1, Q2, Q3, and bias resistor, R1. The values of maximum level shift power versus junction temperature are given in Figures 8 and 9 for several values of V_{EE} and both input conditions. If the duty cycle is defined as in equation 2, the total level shift power is given in equation 3.

$$\text{Duty Cycle} = \frac{\text{Time Both Inputs are High}}{\text{Total Time}} \qquad (2)$$

Level Shift Power = (Value from Figure 8) • (Duty Cycle)+ (3)
(Value from Figure 9) • (1-Duty Cycle)

Output Pullup Current Source

The output pullup current source consists of transistors Q9, Q10 and resistor R3. The power dissipated in the output pullup current

APPLICATIONS INFORMATION (continued)

source depends upon temperature, supply voltages, bias current drawn from the collector-base short of transistor Q10 and output logic level. Neglecting the emitter-base drop of transistor Q10 the value of bias current is determined from equation 4.

$$I_{IB} = \frac{V_{CC2}-V_{EE}}{R3} \qquad (4)$$

If the internal bias resistor is used the maximum value of bias current versus temperature is as shown in Figure 10. The maximum power dissipated in the internal bias resistor and the maximum power dissipated in Q9 and Q10 (due to bias current) are independent of output logic level and are shown in Figures 11 and 12. The maximum power dissipation due to collector current in Q9 is approximately zero when the output is high but when the output is low the power dissipation is as shown in Figure 13. The total output pullup current-source power dissipation is thus defined by equation 5.

P(max) current source = (Value from Figure 11) + (Value from Figure 12) + (Value from Figure 13)x(Duty Cycle) (5)

Example Calculation

Suppose it is desired to use the MOS clock driver in an application which requires the following:

V_{CC1} = +5.0 volts
V_{EE} = -15 volts
V_{CC2} = +5.0 volts
PRR = 1.0 MHz
Duty Cycle = 10%

Load capacitance, 500 pF @ T_A(max) +70°C

A calculation of dc and ac power is necessary to find whether or not package limitations will be exceeded. Since each power dissipation figure either decresases or remains constant with temperature, it is assumed that $T_J \geqslant$ +25°C and points at +25°C will be used in this calculation. The total differential level-shift power may be found from Figures 8 and 9 and equation 3 to be:

Level-Shift Power = 92.5 mW

If the internal bias resistor is used, Figure 10 shows the value of the bias current to be 4.9 mA, and the power dissipation of the internal bias resistor is found from Figure 11 to be 90 mW.

The power dissipation in Q9 and Q10 due to bias current is found from Figure 12 to be 4.0 mW.

The power dissipation in Q9 when the output is low is found from Figure 13 to be 490 mW.

The total power dissipated in the output pullup current source can now be found from equation 5 to be:

Power (current source) = 143 mW

The total dc dissipation, the sum of differential level-shift dissipation and output pullup current-source dissipation, is 235.5 mW.

The ac dissipation may be found from equation 1 to be 200 mW.

The total power dissipation for one clock driver is thus 435.5 mW. If both clock drivers are used in an identical fashion the total package dissipation is 871 mW. Referring to Figure 7 it is seen that safe operation to approximately +45°C is possible. If external resistors are used for R3 to produce the same bias current as above, a net total savings in power dissipation of 180 mW can be made reducing the total package dissipation to 691 mW and permitting safe operation at +70°C.

MC1590G

MONOLITHIC RF/IF/AUDIO AMPLIFIER

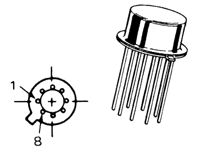
. . . an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, -55 to +125°C. See Motorola Application Note AN-513 for design details.

- High Power Gain — 50 dB typ at 10 MHz
  45 dB typ at 60 MHz
  35 dB typ at 100 MHz
- Wide-Range AGC — 60 dB min, dc to 60 MHz
- Low Reverse Transfer Admittance — <10 μmhos typ at 60 MHz
- 6.0 to 15-Volt Operation, Single-Polarity Power Supply

WIDEBAND AMPLIFIER WITH AGC

SILICON EPITAXIAL PASSIVATED

METAL PACKAGE
CASE 601
TO-99



(bottom view)

FIGURE 1 — UNNEUTRALIZED POWER GAIN versus FREQUENCY (Tuned Amplifier, see Figure 16)

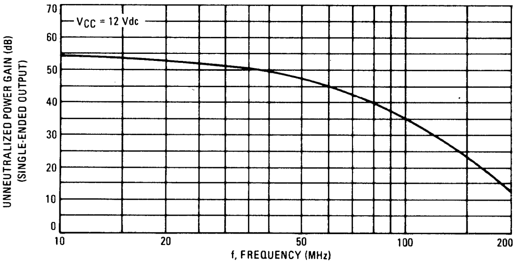
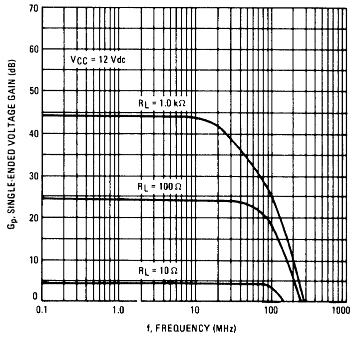
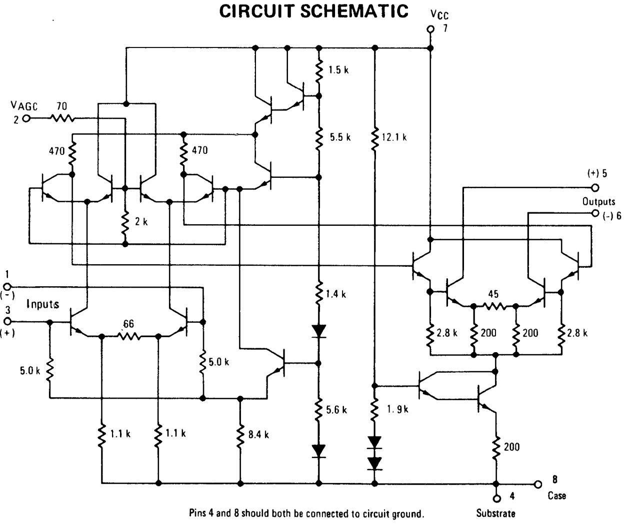


FIGURE 2 — VOLTAGE GAIN versus FREQUENCY (Video Amplifier, see Figure 17)

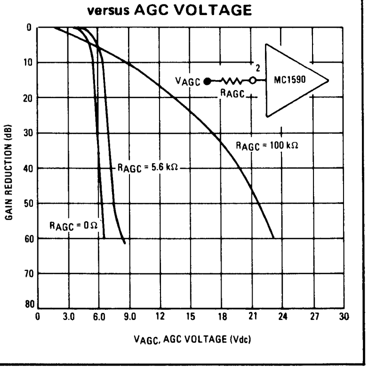


CIRCUIT SCHEMATIC



Pins 4 and 8 should both be connected to circuit ground.

FIGURE 3 — TYPICAL GAIN REDUCTION versus AGC VOLTAGE



See Packaging Information Section for outline dimensions.

See MCBC1590/MCB1590F for beam-lead device information.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Output Supply	V_5, V_6	+18	Vdc
AGC Supply	V_{AGC}	V_{CC}	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = +25°C unless otherwise noted, see Figure 16 for test circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
AGC Range, V_2 = 5.0 Vdc to 7.0 Vdc		60	68	–	dB
Single-Ended Power Gain	G_p	40	45	–	dB
Noise Figure (R_s = 50 ohms)	NF	–	6.0	–	dB
Output Voltage Swing (Pin 5)	V_5				V_{p-p}
Differential Output – 0 dB AGC		–	14	–	
-30 dB AGC		–	6.0	–	
Single-Ended Output – 0 dB AGC		–	7.0	–	
-30 dB AGC		–	3.0	–	
Output Stage Current (Pins 5 and 6)	$I_5 + I_6$	–	5.6	–	mA
Total Supply Power Current (V_o = 0)	I_D	–	14	17	mAdc
Power Dissipation (V_{in} = 0)	P_D	–	168	200	mW

ADMITTANCE PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C)

Parameter	Symbol	Typ f = 30 MHz	Typ f = 60 MHz	Unit
Single-Ended Input Admittance	g_{11} b_{11}	0.4 1.2	0.75 3.4	mmhos
Single-Ended Output Admittance	g_{22} b_{22}	0.05 0.50	0.1 1.0	mmho
Forward Transfer Admittance (Pin 1 to Pin 5)	$\|Y_{21}\|$ θ_{21}	150 -45	150 -105	mmhos degrees
Reverse Transfer Admittance*	g_{12} b_{12}	-0 -5.0	-0 -10	μmhos

*The value of Reverse Transfer Admittance includes the feedback admittance of the test circuit used in the measurement. The total feedback capacitance (including test circuit) is 0.025 pF and is a more practical value for design calculations than the internal feedback of the device alone. (See Figure 6)

SCATTERING PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	Typ f = 30 MHz	Typ f = 60 MHz	Unit
Input Reflection Coefficient	$\|S_{11}\|$ θ_{11}	0.95 -7.3	0.93 -16	– degrees
Output Reflection Coefficient	$\|S_{22}\|$ θ_{22}	0.99 -3.0	0.98 -5.5	– degrees
Forward Transmission Coefficient	$\|S_{21}\|$ θ_{21}	16.8 128	14.7 64.3	– degrees
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	– degrees

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TYPICAL CHARACTERISTICS

(V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 4 – FIXED TUNED POWER GAIN versus TEMPERATURE (See test circuit, Figure 16)

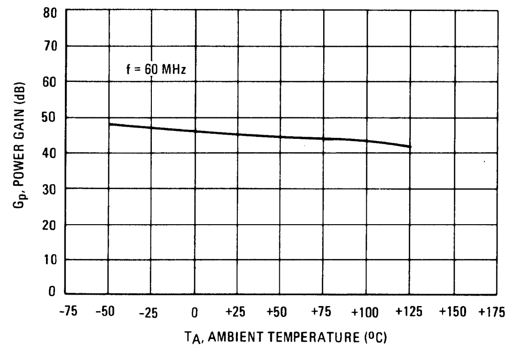


FIGURE 5 – POWER GAIN versus SUPPLY VOLTAGE (See test circuit, Figure 16)

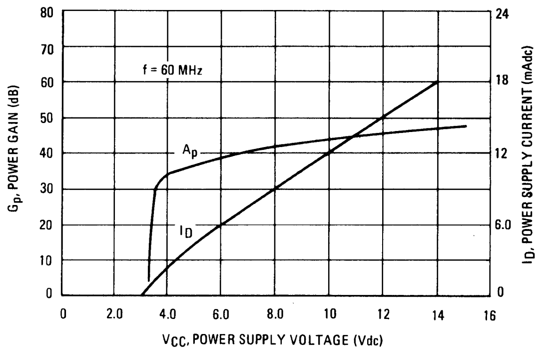


FIGURE 6 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY (See Parameter Table, page 2 of MC1590 specification)

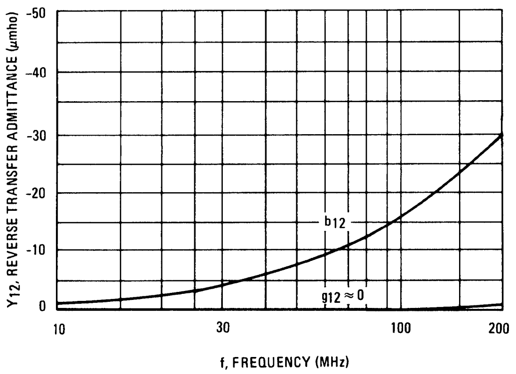


FIGURE 7 – NOISE FIGURE versus FREQUENCY

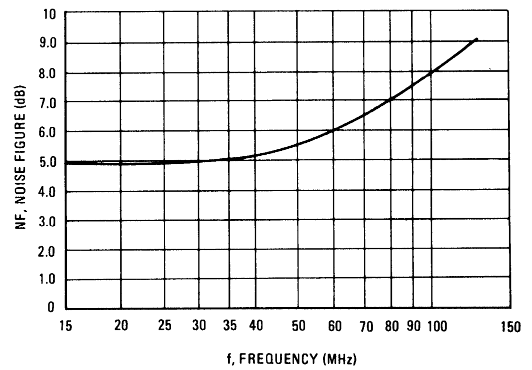


FIGURE 8 – SINGLE-ENDED OUTPUT ADMITTANCE

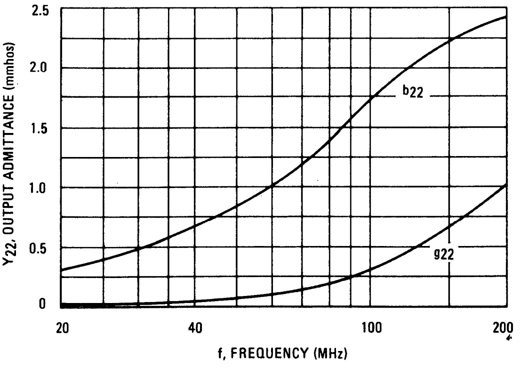
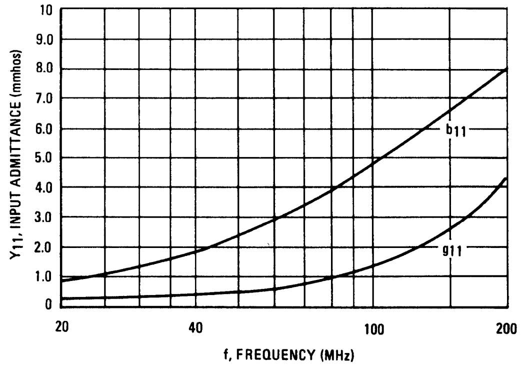


FIGURE 9 – SINGLE-ENDED INPUT ADMITTANCE



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TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – Y_{21}, FORWARD TRANSFER ADMITTANCE, RECTANGULAR FORM

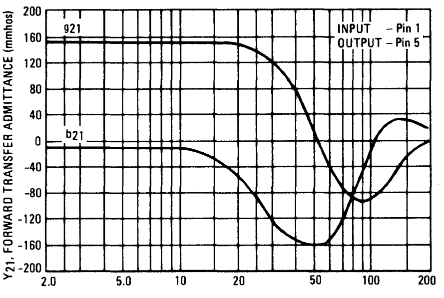


FIGURE 11 – Y_{21}, FORWARD TRANSFER ADMITTANCE, POLAR FORM

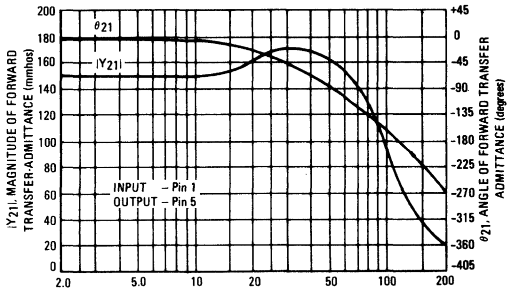


FIGURE 12 – S_{11} and S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

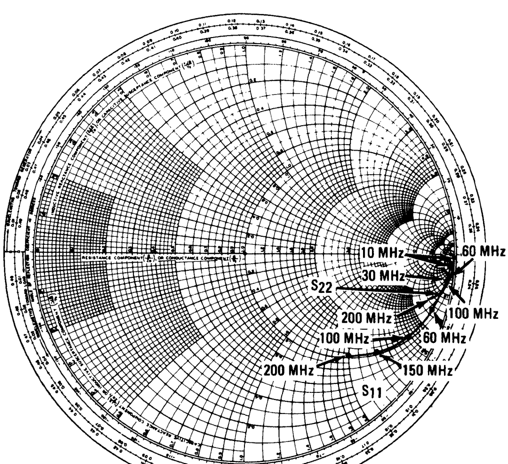
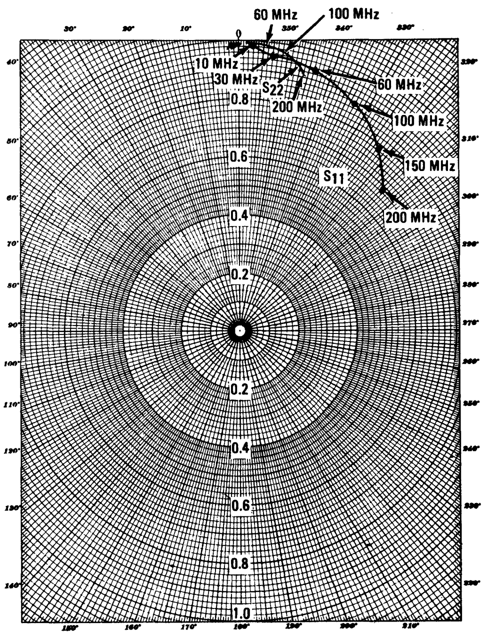


FIGURE 13 – S_{11}, and S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT



8

TYPICAL CHARACTERISTICS (continued)

FIGURE 14 – S_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

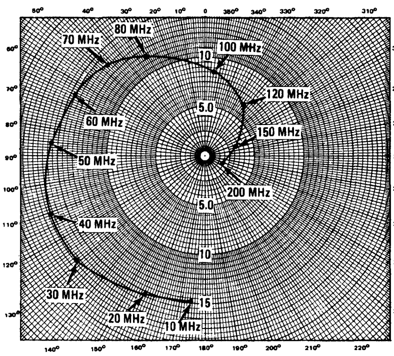
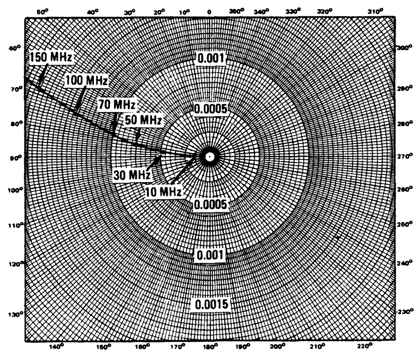
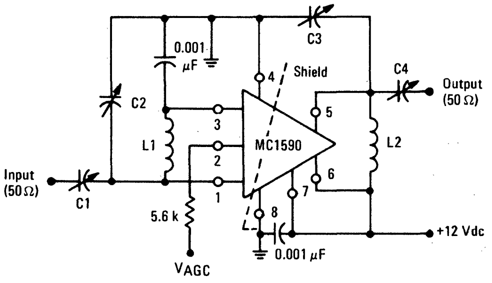


FIGURE 15 – S_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



TYPICAL APPLICATIONS

FIGURE 16 – 60-MHz POWER GAIN TEST CIRCUIT



L1 = 7 Turns, #20 AWG Wire, 5/16" Dia., 5/8" Long
L2 = 6 Turns, #14 AWG Wire, 9/16" Dia., 3/4" Long

C1,C2,C3 = (1-30) pF
C4 = (1-10) pF

FIGURE 17 – VIDEO AMPLIFIER

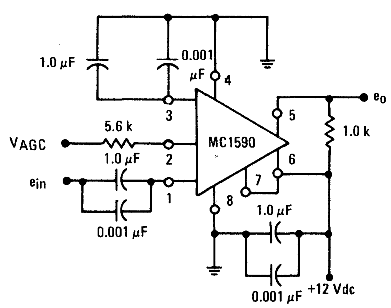
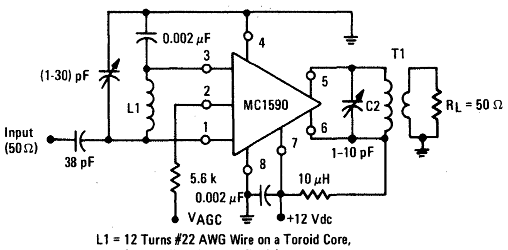
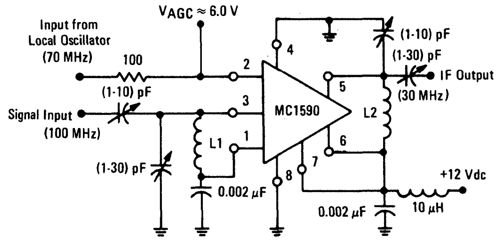


FIGURE 18 – 30-MHz AMPLIFIER (Power Gain = 50 dB, BW ≈ 1.0 MHz)



L1 = 12 Turns #22 AWG Wire on a Toroid Core, (T37-6 Micro Metal or Equiv)
T1: Primary = 17 Turns #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)
Secondary = 2 Turns #20 AWG Wire

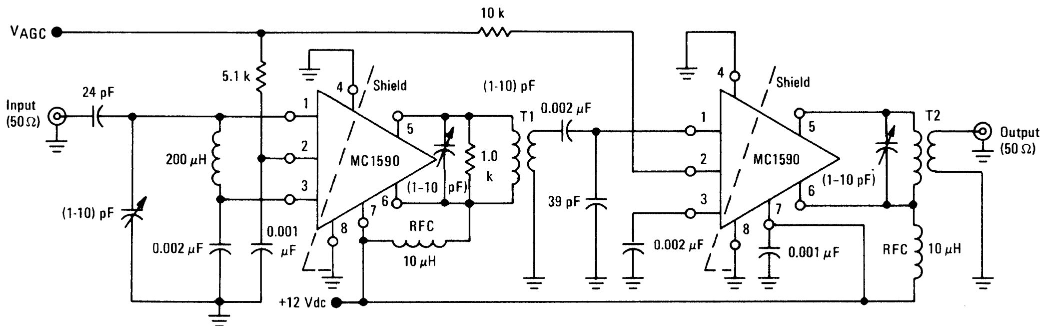
FIGURE 19 – 100-MHz MIXER



L1 = 5 Turns, #16 AWG Wire, 1/4" ID, 5/8" Long
L2 = 16 Turns, #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)

TYPICAL APPLICATIONS (continued)

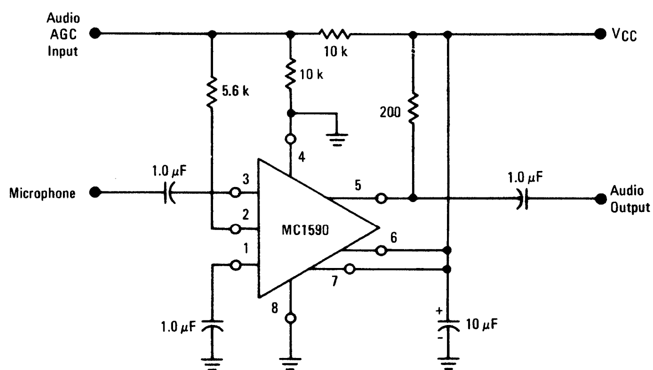
FIGURE 20 – TWO-STAGE 60 MHz IF AMPLIFIER (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)



T1: Primary Winding = 15 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 4 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 2 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

FIGURE 21 – SPEECH COMPRESSOR



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MULTIPLIERS

MC1594L
MC1494L

Specifications and Applications Information

MONOLITHIC FOUR-QUADRANT MULTIPLIER

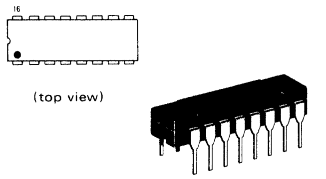
. . . designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

- Operates With ±15 V Supplies
- Excellent Linearity – Maximum Error (X or Y): ± 0.5% (MC1594)
  ± 1.0% (MC1494)
- Wide Input Voltage Range – ±10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single-Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small-Signal) – 1.0 MHz
- Power Supply Sensitivity – 30 mV/V typical

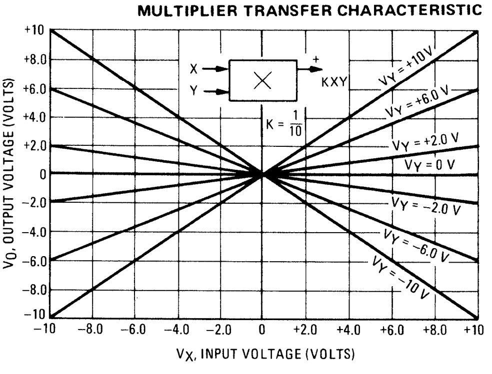
LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

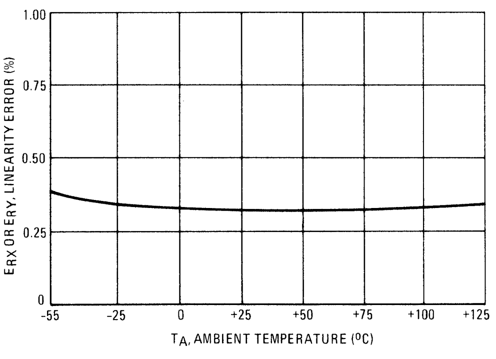


CERAMIC PACKAGE
CASE 620

FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC



TYPICAL LINEARITY ERROR versus TEMPERATURE



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CONTENTS

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	V_9-V_6 $V_{10}-V_{13}$	$\pm\lvert 6+I_1 R_Y\rvert < 30$ $\pm\lvert 6+I_1 R_X\rvert < 30$	Vdc
Common-Mode Input Voltage $V_{CMY} = V_9 = V_6$ $V_{CMX} = V_{10} = V_{13}$	 V_{CMY} V_{CMX}	 ±11.5 ±11.5	Vdc
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	 P_D $1/\theta_{JA}$	 750 5.0	 mW mW/°C
Operating Temperature Range MC1594 MC1494	T_A	 -55 to +125 0 to + 75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 V, V^- = -15 V, T_A = +25°C, R1 = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, unless otherwise noted)

Characteristic	Fig.	Symbol	MC1594 Min	MC1594 Typ	MC1594 Max	MC1494 Min	MC1494 Typ	MC1494 Max	Unit
Linearity	1	E_{RX} or E_{RY}							%
Output error in Percent of full scale									
$-10\text{ V} < V_x < +10\text{ V}$ ($V_y = \pm 10$ V)									
$-10\text{ V} < V_y < +10\text{ V}$ ($V_x = \pm 10$ V)									
T_A = +25°C			–	± 0.3	± 0.5	–	± 0.5	± 1.0	
$T_A = T_{high}$ ①			–	–	± 0.8	–	–	± 1.3	
$T_A = T_{low}$ ②			–	–	± 0.8	–	–	± 1.3	
Input	2,3,4								
Voltage Range ($V_X = V_Y = V_{in}$)		V_{in}	±10	–	–	±10	–	–	V_{pk}
Resistance (X or Y Input)		R_{in}	–	300	–	–	300	–	MΩ
Offset Voltage (X Input) (Note 1)		$\lvert V_{iox}\rvert$	–	0.1	1.6	–	0.2	2.5	V
(Y Input) (Note 1)		$\lvert V_{ioy}\rvert$	–	0.4	1.6	–	0.8	2.5	
Bias Current (X or Y Input)		I_b	–	0.5	1.5	–	1.0	2.5	µA
Offset Current (X or Y Input)		$\lvert I_{io}\rvert$	–	28	150	–	50	400	nA
Output	3,4								
Voltage Swing Capability		V_o	±10	–	–	±10	–	–	V_{pk}
Impedance		R_o	–	850	–	–	850	–	kΩ
Offset Voltage (Note 1)		$\lvert V_{oo}\rvert$	–	0.8	1.6	–	1.2	2.5	V
Offset Current (Note 1)		$\lvert I_{oo}\rvert$	–	17	34	–	25	52	µA
Temperature Stability (Drift)									
$T_A = T_{high}$ to T_{low}									
Output Offset (X = 0, Y = 0) Voltage		$\lvert TCV_{oo}\rvert$	–	1.3	–	–	1.3	–	mV/°C
Current		$\lvert TCI_{oo}\rvert$	–	27	–	–	27	–	nA/°C
X Input Offset (Y = 0)		$\lvert TCV_{iox}\rvert$	–	0.3	–	–	0.3	–	mV/°C
Y Input Offset (X = 0)		$\lvert TCV_{ioy}\rvert$	–	1.5	–	–	1.5	–	
Scale Factor		$\lvert TCK\rvert$	–	0.07	–	–	0.07	–	%/°C
Total dc Accuracy Drift (X = 10, Y = 10)		$\lvert TCE\rvert$	–	0.09	–	–	0.09	–	
Dynamic Response	5								
Small Signal (3 dB) X		$BW_{3\,dB(X)}$	–	0.8	–	–	0.8	–	MHz
Y		$BW_{3\,dB(Y)}$	–	1.0	–	–	1.0	–	
Power Bandwidth (47 k)		P_{BW}	–	440	–	–	440	–	kHz
3° Relative Phase Shift		$f\phi$	–	240	–	–	240	–	
1% Absolute Error		$f\theta$	–	30	–	–	30	–	
Common Mode	6								
Input Swing (X or Y)		CMV	±10.5	–	–	±10.5	–	–	V_{pk}
Gain (X or Y)		A_{CM}	–	-65	–	–	-65	–	dB
Power Supply	7								
Current		I_d^+	–	6.0	9.0	–	6.0	12	mAdc
		I_d^-	–	6.5	9.0	–	6.5	12	
Quiescent Power Dissipation		P_d	–	185	260	–	185	350	mW
Sensitivity		S^+	–	13	50	–	13	100	mV/V
		S^-	–	30	100	–	30	200	
Regulated Offset Adjust Voltages	7								
Positive		V_R^+	+3.5	+4.3	+5.0	+3.5	+4.3	+5.0	Vdc
Negative		V_R^-	-3.5	-4.3	-5.0	-3.5	-4.3	-5.0	
Temperature Coefficient (V_R^+ or V_R^-)		TCV_R	–	0.03	–	–	0.03	–	mV/°C
Power Supply Sensitivity (V_R^+ or V_R^-)		S_R^+, S_R^-	–	0.6	–	–	0.6	–	mV/V

Note 1: Offsets can be adjusted to zero with external potentiometers.

① T_{high} = +125°C for MC1594, + 75°C for MC1494   ② T_{low} = -55°C for MC1594, 0°C for MC1494

(MC1594 - Pg. 2)

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TEST CIRCUITS

FIGURE 1 – LINEARITY

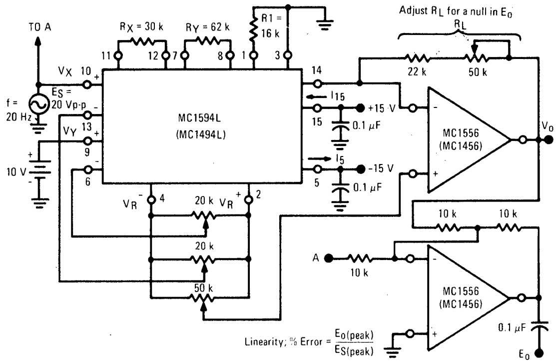


FIGURE 2 – INPUT RESISTANCE

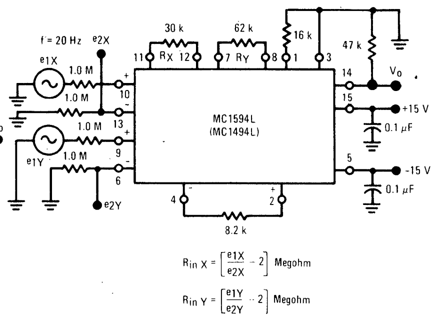


FIGURE 3 – OFFSET VOLTAGES, GAIN

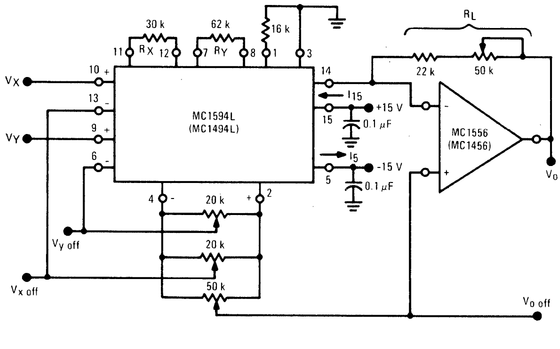


FIGURE 4 – INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE

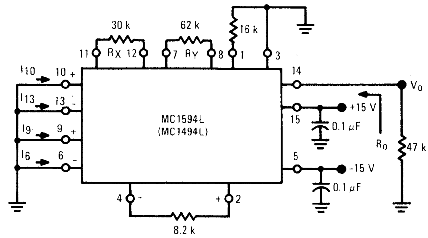


FIGURE 5 – FREQUENCY RESPONSE

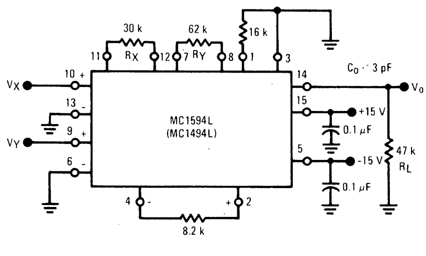


FIGURE 6 – COMMON-MODE

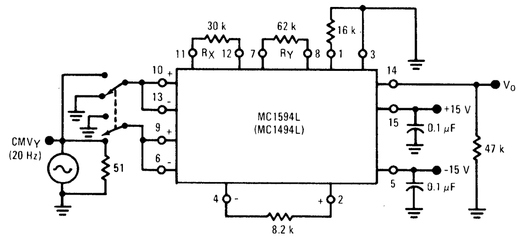


FIGURE 7 – POWER-SUPPLY SENSITIVITY

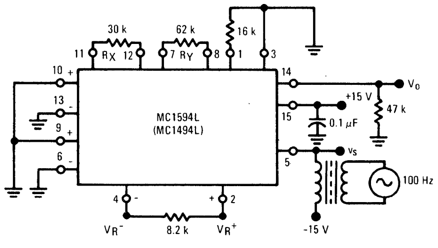
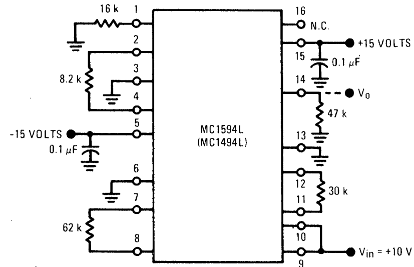


FIGURE 8 – BURN-IN



(MC1594 - Pg. 3)

TYPICAL CHARACTERISTICS

(Unless otherwise noted, $V^+ = +15$ V, $V^- = -15$ V, R1 = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, T_A = +25°C)

FIGURE 9 – FREQUENCY RESPONSE OF Y INPUT versus LOAD RESISTANCE

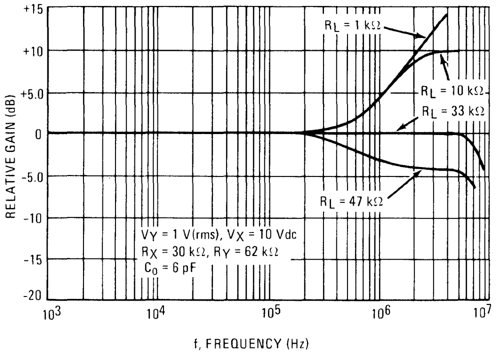


FIGURE 10 – FREQUENCY RESPONSE OF X INPUT versus LOAD RESISTANCE

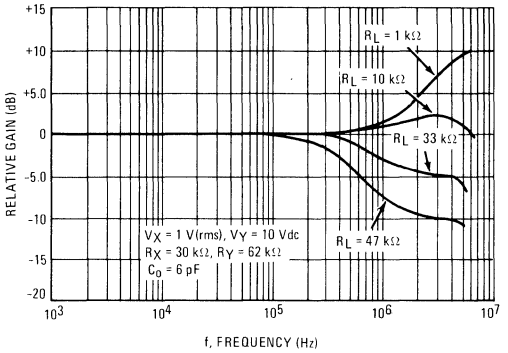


FIGURE 11 – LARGE SIGNAL VOLTAGE versus FREQUENCY

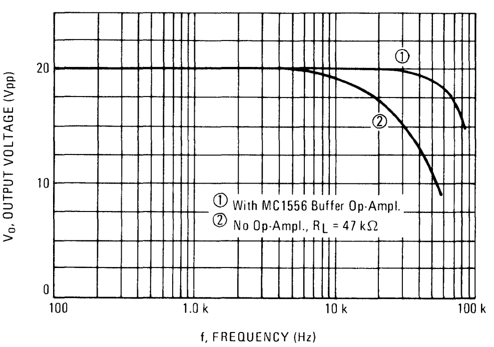


FIGURE 12 – LINEARITY versus R_X OR R_Y WITH K = 1/10

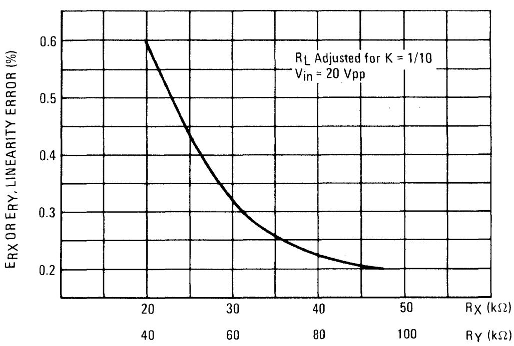


FIGURE 13 – LINEARITY versus R_X OR R_Y WITH K = 1

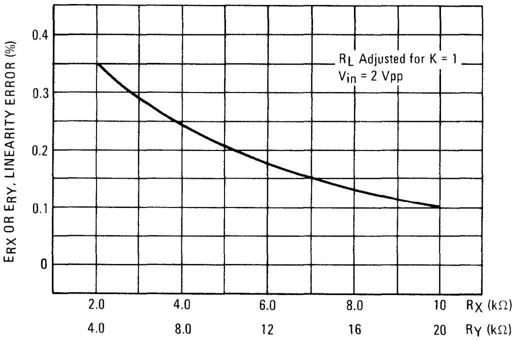
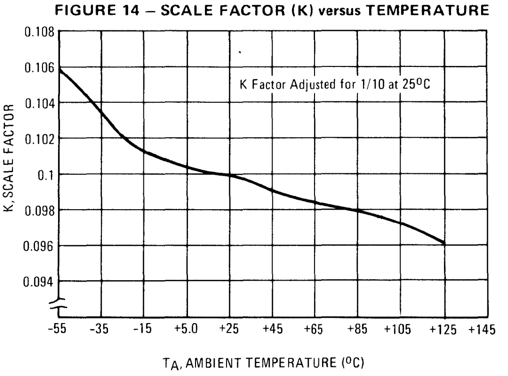


FIGURE 14 – SCALE FACTOR (K) versus TEMPERATURE



GENERAL INFORMATION

1. CIRCUIT DESCRIPTION

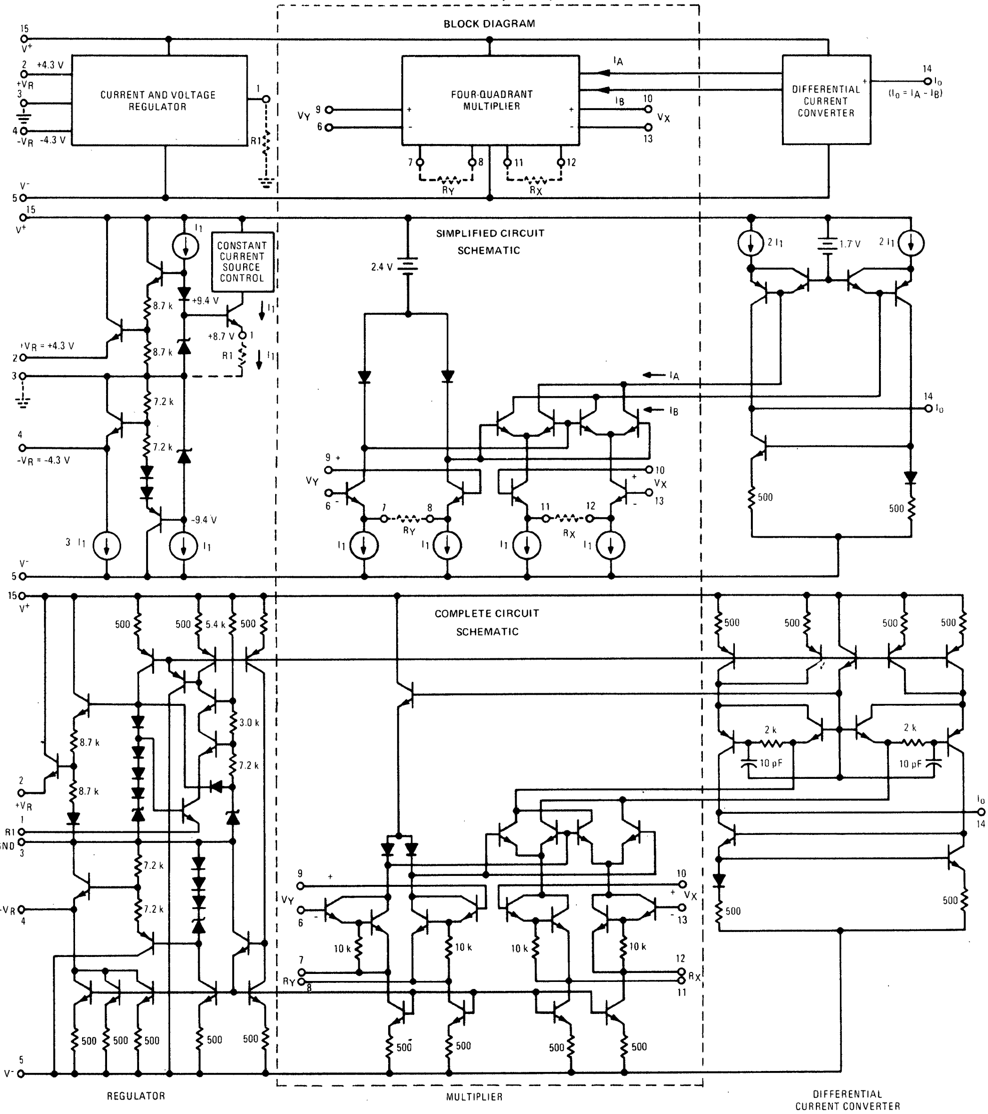
1.1 Introduction

The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features.

FIGURE 15

(Recommended External Circuitry is Depicted With Dotted Lines)



(MC1594 - Pg. 5)

1.2 Regulator (Figure 15)

The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately -4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 k-ohm potentiometers and one 50 k-ohm potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all current sources are related to current I_1 which is determined by R1. For best temperature performance, R1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications.

1.3 Multiplier (Figure 15)

The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595". The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

1.4 Differential Current Converter (Figure 15)

This portion of the circuitry converts the differential output current ($I_A - I_B$) of the multiplier to a single-ended output current (I_o):

$$I_o = I_A - I_B$$

or

$$I_o = \frac{2V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (pin 14) to ground (Figure 17) or by using an op-ampl. as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by:

$$V_o = \frac{2R_L V_X V_Y}{R_X R_Y I_1} = K V_X V_Y$$

$$\text{where K (scale factor)} = \frac{2R_L}{R_X R_Y I_1}$$

2. DC OPERATION

2.1 Selection of External Components

For low frequency operation the circuit of Figure 16 is recommended. For this circuit, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, R1 = 16 kΩ and hence $I_1 \approx 0.5$ mA. Therefore, to set the scale factor, K, equal to 1/10, the value of R_L can be calculated to be:

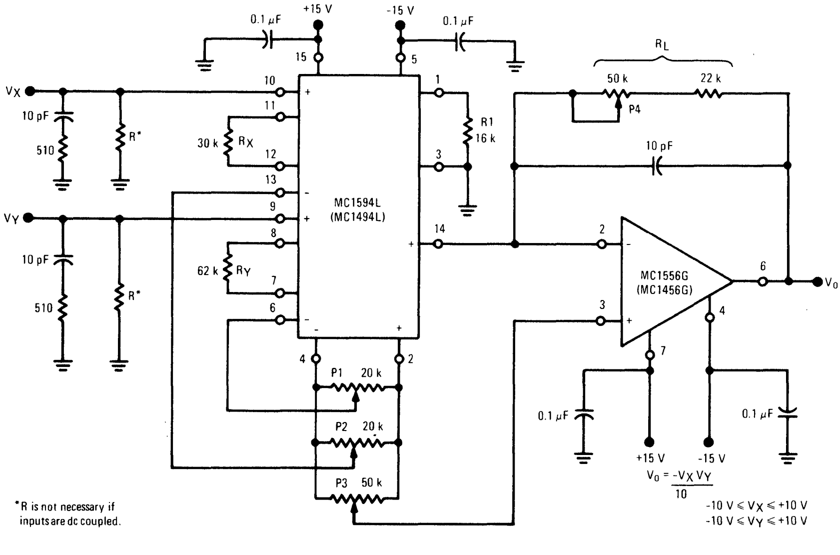
$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

$$\text{or} \quad R_L = \frac{R_X R_Y I_1}{(2)(10)} = \frac{(30\text{ k})(62\text{ k})(0.5\text{ mA})}{20}$$

$$R_L = 46.5\text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 kΩ resistor. However, if it is desired

FIGURE 16 – TYPICAL MULTIPLIER CONNECTION



MC1594 - Pg. 6)

that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ±10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set K = 1/2 or K = 1 or even K = 100. This can be accomplished by adjusting R_X, R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 16 that R_Y is 62 kΩ while R_X is 30 kΩ. The reason for this is that the "Y" side of the multiplier exhibits a second order non-linearity whereas the "X" side exhibits a simple non-linearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the "X" and "Y" sides are made equal. The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations:

$R_X \geq 3\ V_X$ (max) in kΩ when V_X is in volts

$R_Y \geq 6\ V_Y$ (max) in kΩ when V_Y is in volts

For example, if the maximum input on the "X" side is ±1 volt, resistor R_X can be selected to be 3 kΩ. If the maximum input on the "Y" side is also ±1 volt, then resistor R_Y can be selected to be 6 kΩ (6.2 kΩ nominal value). If a scale factor of K = 10 is desired, the load resistor is found to be 47 kΩ. In this example, the multiplier provides a gain of 20 dB.

2.2 Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op-ampl. Since the offset current and bias currents of the op-ampl. will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-ampl., the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-ampl.

2.3 Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op-ampls.) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-ampl. might be employed using slightly heavier compensation than that recommended for unity-gain operation.

2.4 Offset Adjustment

The non-inverting input of the op-ampl. provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

2.5 Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is:

A. X Input Offset
- (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 9)
- (b) connect "X" input (pin 10) to ground
- (c) adjust X-offset potentiometer, P2 for an ac null at the output

B. Y Input Offset
- (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 10)
- (b) connect "Y" input (pin 9) to ground
- (c) adjust Y-offset potentiometer, P1 for an ac null at the output

C. Output Offset
- (a) connect both "X" and "Y" inputs to ground
- (b) adjust output offset potentiometer, P3, until the output voltage V_O, is zero volts dc

D. Scale Factor
- (a) apply +10 Vdc to both the "X" and "Y" inputs
- (b) adjust P4 to achieve -10.00 V at the output
- (c) apply -10 Vdc to both "X" and "Y" inputs and check for V_O = -10.00 V

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

2.6 Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on R_X, R_Y, and R_L and indirect dependence on R1 (through I_1). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

2.7 Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current (≈ 0.5 μA) resistors, R (Figure 16) can be omitted. If the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 kΩ. For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

2.8 Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network is to reduce the "Q" of the source-tuned circuits which cause the oscillation.

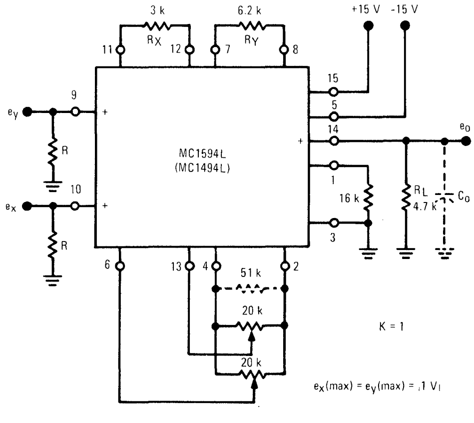
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

3. AC OPERATION

3.1 General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc., the op-ampl. will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17

FIGURE 17 – WIDEBAND MULTIPLIER



shows a typical ac multiplier circuit with a scale factor $K \approx 1$. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1594 is typically 17 μA and 35 μA maximum. Thus, the maximum output offset would be about 160 mV.

3.2 Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance (C_O) of 10 pF, the 3 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The effect of these transmission "zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with the "X" input. For R_X = 30 kΩ and R_Y = 62 kΩ, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for ac applications; (1) the value of resistors R_X, R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole (R_L, C_O) cancels the input zero (R_X, 3.5 pF or R_Y, 3.5 pF) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal.

For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC1596 may be used up to 100 MHz. For wideband multiplier applications, the MC1595 (using small collector loads and ac coupling) can be used.

3.3 Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-ampl. is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew-Rate } \frac{\Delta V_O}{\Delta T} = \frac{I_O}{C}$$

Thus, if C_O is 10 pF, the maximum slew-rate would be:

$$\frac{\Delta V_O}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50 \text{ V}/\mu\text{s}$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer.

3.4 Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector error is best explained by an example. If the "X" input is described in vector notation as

$$X = A \measuredangle 0^{\circ}$$

and the "Y" input is described as

$$Y = B \measuredangle 0^{\circ}$$

then the output product would be expected to be

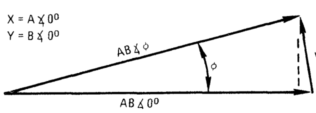
$$V_o = AB \measuredangle 0^{\circ} \text{ (see Figure 18)}$$

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by

$$V_o = AB \measuredangle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector, V, associated with this error is the "phase-vector error". The startling fact about the phase-vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57° will result in a 1% phase-vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase-vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase-vector error will represent a 1% amplitude error at the phase angle of interest.

FIGURE 18 – PHASE-VECTOR ERROR



3.5 Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across R_X and R_Y should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

4. DC APPLICATIONS

4.1 Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_o = KV^2$$

where K is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_o = K(V_x + V_{iox} - V_{x\,off})\,(V_y + V_{ioy} - V_{y\,off}) + V_{oo}$$

(See "Definitions" for an explanation of terms).

With $V_x = V_y = V$ (squaring) and defining

$$\epsilon_x = V_{iox} - V_{x\,off}$$

$$\epsilon_y = V_{ioy} - V_{y\,off}$$

The output voltage equation becomes

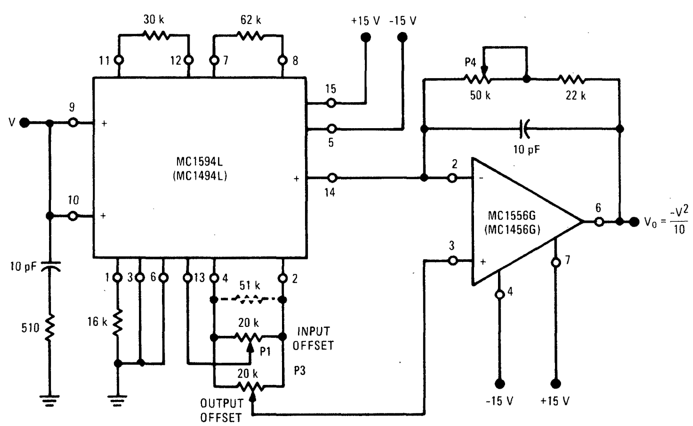
$$V_o = K\,V_x^2 + KV_x\,(\epsilon_x + \epsilon_y) + K\epsilon_x\epsilon_y + V_{oo}$$

This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, ϵ_x is determined by the internal offset, V_{iox}, but ϵ_y is adjustable to the extent that the $(\epsilon_x + \epsilon_y)$ term can be zeroed. Then the output offset adjustment is used to adjust the V_{oo} term and thus zero the remaining error terms. An ac procedure for nulling with three adjustments is:

A. AC Procedure:

1. Connect oscillator (1 kHz, 15 Vpp) to input
2. Monitor output at 2 kHz with tuned voltmeter and adjust P4 for desired gain (Be sure to peak response of voltmeter)
3. Tune voltmeter to 1 kHz and adjust P1 for a minimum output voltage
4. Ground input and adjust P3 (output offset) for zero volts dc out
5. Repeat steps 1 through 4 as necessary.

FIGURE 19 – MC1594 SQUARING CIRCUIT



(MC1594 - Pg. 9)

B. DC Procedure:

1. Set V_X = V_Y = 0 V and adjust P3 (output offset potentiometer) such that V_o = 0.0 Vdc
2. Set V_X = V_Y = 1.0 V and adjust P1 (Y input offset potentiometer) such that the output voltage is -0.100 volts
3. Set V_X = V_Y = 10 Vdc and adjust P4 (load resistor) such that the output voltage is -10.00 volts
4. Set V_X = V_Y = -10 Vdc and check that V_O = -10V Repeat steps 1 through 4 as necessary.

4.2 Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if V_X is allowed to go negative or, in some cases, if V_X approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-ampl. Thus, operation is in the negative feedback mode and the circuit is dc stable. Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from V_X being near zero is a result of the transfer through the multiplier being near zero. The op-ampl. is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-ampl. exceeding the rated common-mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-ampl. to approximately ± 10.7 volts. Five-percent tolerance, 10-volt zeners are used to assure adequate output swing but still limit the output voltage of the op-ampl. from exceeding the common-mode input range of the MC1594.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set V_Z = 0 volts and adjust the output offset potentiometer (P3) until the output voltage (V_o) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 volt and +10 volts.
2. Maintain V_Z at 0 volts, set V_X at +10 volts and adjust the Y input offset potentiometer (P1) until V_o = 0 volts.
3. With V_X = V_Z, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily - 10 volts) constant value as V_Z = V_X is varied between +1.0 volt and +10 volts.
4. Maintain V_X = V_Z and adjust the scale factor potentiometer (R_L) until the average value of V_o is - 10 volts as V_Z = V_X is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-

FIGURE 20 – BASIC DIVIDE CIRCUIT USING MULTIPLIER

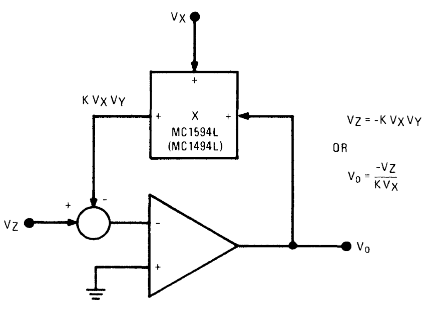
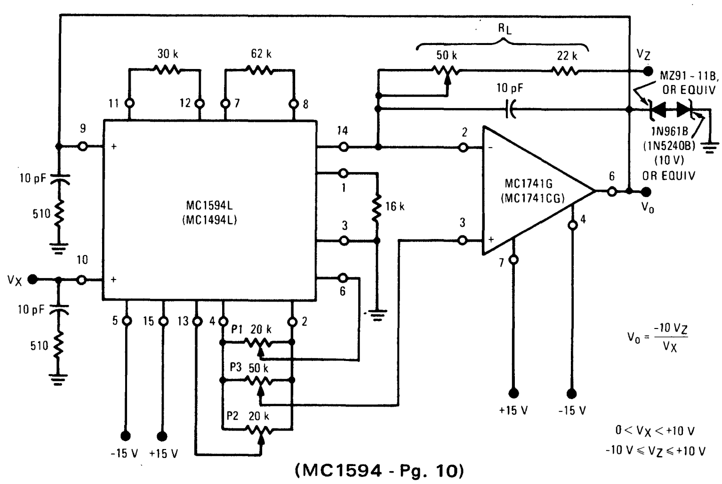
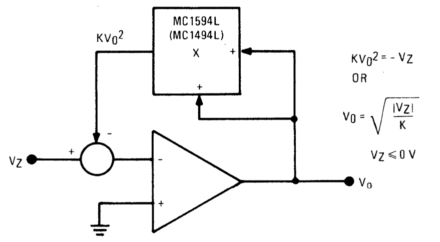


FIGURE 21 – PRACTICAL DIVIDE CIRCUIT



(MC1594 - Pg. 10)

FIGURE 22 – BASIC SQUARE ROOT CIRCUIT



nator voltage. As a result, if V_X is set to 10 volts and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1 volt.

In accordance with an earlier statement, V_X may have only one polarity, positive, while V_Z may be either polarity.

4.3 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode:

1. Set V_Z = -0.01 Vdc and adjust P3 (output offset) for V_O = 0.316 Vdc.
2. Set V_Z to -0.9 Vdc and adjust P2 ("X" adjust) for V_O = +3 Vdc.
3. Set V_Z to -10 Vdc and adjust P4 (gain adjust) for V_O = +10 Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near zero volts input may prove very inaccurate, hence, it may not be possible to adjust V_O to 0 but rather only to within 100 to 400 mV of zero.

5. AC APPLICATIONS

5.1 Wideband Amplifier With Linear AGC

If one input to the MC1594 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control.

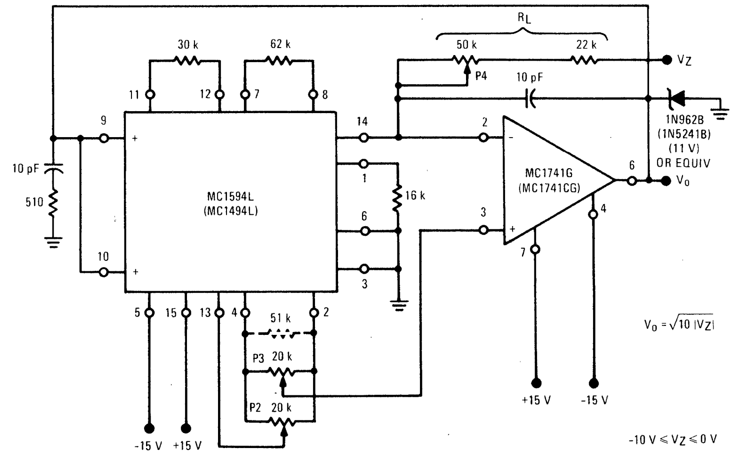
In addition to the advantage of Linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage-swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1 V(rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1 MHz.

5.2 Balanced Modulator

When two-time variant signals are used as inputs, the result-

FIGURE 23 – SQUARE ROOT CIRCUIT



(MC1594 - Pg. 11)

ing output is suppressed-carrier double-sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

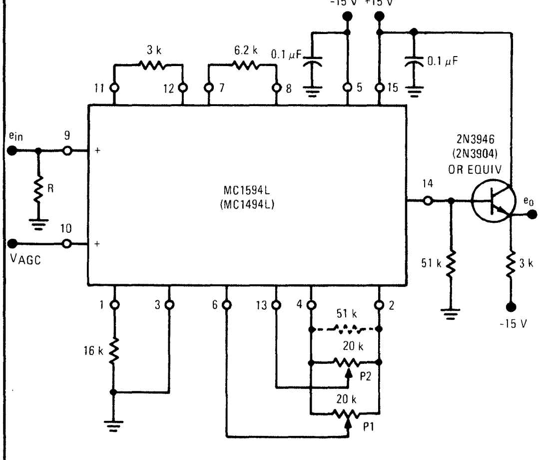
$$V_o = K(e_1 \cos\omega_m t)(e_2 \cos\omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_o = \frac{Ke_1e_2}{2}\,[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

FIGURE 24 – WIDEBAND AMPLIFIER WITH LINEAR AGC

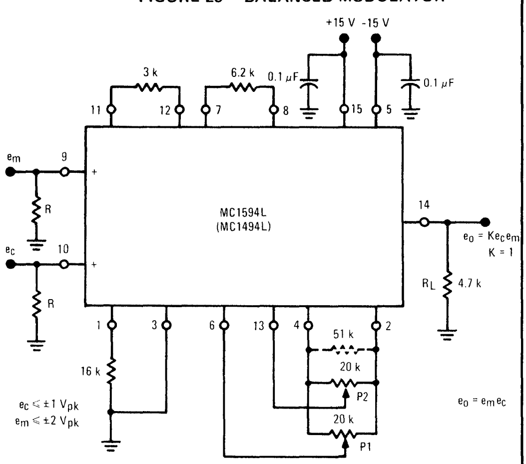


Notice that the resistor values for R_X, R_Y, and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1 volt peak and e_m as high as 2 volts peak. No output offset adjust is employed since we are interested only in the ac output components.

The input R's are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of ≥70 dB from 10 kHz to 1.5 MHz.

FIGURE 25 – BALANCED MODULATOR



The adjustment procedure for this circuit is quite simple.

(1) Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.

(2) Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

5.3 Frequency Doubler

If for Figure 25 both inputs are identical;

$$e_m = e_c = E\cos\omega t$$

Then the output is given by

$$e_o = e_m e_c = E^2\cos^2\omega t$$

which reduces to

$$e_o = \frac{E^2}{2}(1 + \cos 2\omega t)$$

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

5.4 Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modulation input. This procedure places a dc offset on the modulation input of the multiplier such that the carrier still passes thru the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with K = 1,

$$e_o = (E + E_m \cos\omega_m t)\,(E_c \cos\omega_c t)$$

where E is the dc input offset adjust voltage. This expression can be written as:

$$e_o = E_o\,[1 + M \cos\omega_c t]\,\cos\omega_c t$$

where $E_o = EE_c$

and $M = \frac{E_m}{E}$ = modulation index

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, E_m. This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

5.5 Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency but having a relative phase shift the output will be a dc signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos\omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos\omega_c t \cos(\omega_c t + \phi)$$

or

$$e_o = \frac{E_c E_m}{2}\,[\cos\phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

6. DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

6.1 Multiplier Transfer Function

The output of the multiplier may be expressed by this equation:

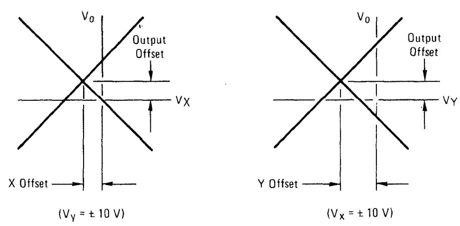
$$V_o = K\,(V_x \pm V_{iox} - V_{x\,off})\,(V_y \pm V_{ioy} - V_{y\,off}) \pm V_{oo} \quad (1)$$

where K = scale factor (see 6.5)

V_x = "x" input voltage
V_y = "y" input voltage
V_{iox} = "x" input offset voltage
V_{ioy} = "y" input offset voltage
$V_{x\,off}$ = "x" input offset adjust voltage
$V_{y\,off}$ = "y" input offset adjust voltage
V_{oo} = output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

FIGURE 26



6.2 Linearity

Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for V_x and V_y separately either using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_o = \frac{V_x V_y}{10} \pm (0.0035)\,(10 \text{ volts})$$

6.3 Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for V_x and V_y separately and is defined to be that dc input offset adjust voltage ("x" or "y") that will result in minimum ac output when ac (5 Vpp, 1 kHz) is applied to the other input ("y" or "x" respectively). From Equation (1) we have:

$$V_{o(ac)} = K\,(0 \pm V_{iox} - V_{x\,off})\,(\sin\omega t)$$

adjust $V_{x\,off}$ so that $(\pm V_{iox} - V_{x\,off}) = 0$.

6.4 Output Offset Current and Voltage

Output offset current (I_{oo}) is the dc current flowing in the output lead when $V_x = V_y = 0$ and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage (V_{oo}) is:

$$V_{oo} = I_{oo}\,R_L$$

where R_L is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

6.5 Scale Factor

Scale factor is the K term in Equation (1). It determines the "gain" of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_x R_y I_1} \text{ where } R_x \text{ and } R_y >> \frac{kT}{qI_1}$$

and I_1 is the current out of pin 1.

6.6 Total DC Accuracy

The total dc accuracy of a multiplier is defined as error in multiplier output with dc (±10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

6.7 Temperature Stability (Drift)

Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by re-adjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by:

$\Delta V_O = \pm[K \pm K\ (TCK)\ (\Delta T)\ ]\ [\ (TCV_{iox})\ (\Delta T)\ ]\ [\ (TCV_{ioy})\ (\Delta T)\ ] \pm (TCV_{oo})\ (\Delta T)$

6.8 Total DC Accuracy Drift

This is the temperature drift in output voltage with 10 volts applied to each input. The output is adjusted to 10 volts at $T_A = +25^oC$. Assuming initial offset voltages have been adjusted to zero at $T_A = +25^oC$, then:

$V_O = [K \pm K\ (TCK)\ (\Delta T)\ ]\ [10 \pm (TCV_{iox})\ (\Delta T)\ ]\ [10 \pm (TCV_{ioy})\ (\Delta T)\ ] \pm (TCV_{oo})\ (\Delta T)$

6.9 Power Supply Rejection

Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1-volt, 100-Hz signal on each supply (±15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

6.10 Output Voltage Swing

Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (note-output offset is adjusted to zero).

If an op-ampl. is used, the multiplier output becomes a virtual ground – the swing is then determined by the scale factor and the op-ampl. selected.

GENERAL INFORMATION INDEX

MC1595L
MC1495L

Specifications and Applications Information

WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

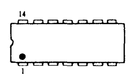
. . . designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

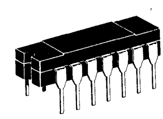
- Wide Bandwidth
- Excellent Linearity – 1% max Error on X-Input, 2% max Error on Y-Input – MC1595L
- Excellent Linearity – 2% max Error on X-Input, 4% max Error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED



(top view)



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 – FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC

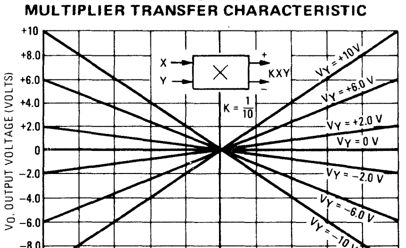


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

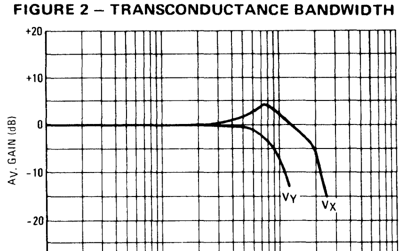
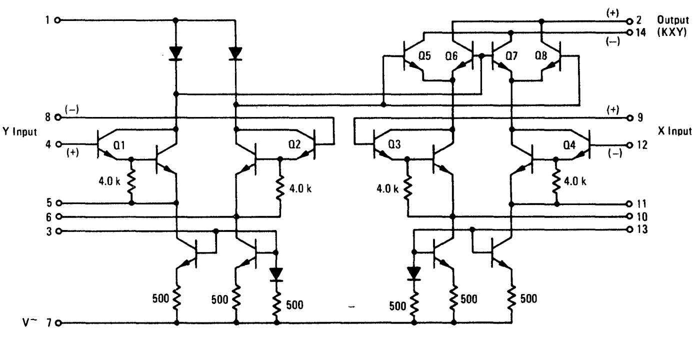


FIGURE 3 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

See current MCC1595/1495 data sheet for standard linear chip information.

ELECTRICAL CHARACTERISTICS (V^+ = +32V, V^- = −15 V, T_A = +25°C, I_3 = I_{13} = 1 mA, R_X = R_Y = 15 kΩ, R_L = 11 kΩ unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Linearity:							
Output Error in Percent of Full Scale:		5					%
T_A = +25°C							
$-10 < V_X < +10$ (V_Y = ±10 V)	MC1495		E_{RX}	–	± 1.0	± 2.0	
	MC1595			–	± 0.5	± 1.0	
$-10 < V_Y < +10$ (V_X = ±10 V)	MC1495		E_{RY}	–	± 2.0	± 4.0	
	MC1595			–	± 1.0	± 2.0	
T_A = 0 to +70°C	MC1495						
$-10 < V_X < +10$ (V_Y = ±10 V)			E_{RX}	–	± 1.5	–	
$-10 < V_Y < +10$ (V_X = ±10 V)			E_{RY}	–	± 3.0	–	
T_A = −55°C to +125°C	MC1595						
$-10 < V_X < +10$ (V_Y = ±10 V)			E_{RX}	–	± 0.75	–	
$-10 < V_Y < +10$ (V_X = ±10 V)			E_{RY}	–	± 1.50	–	
Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment		5	E_{SQ}				%
T_A = +25°C	MC1495			–	± 0.75	–	
	MC1595			–	± 0.5	–	
T_A = 0 to +70°C	MC1495			–	± 1.0	–	
T_A = −55°C to +125°C	MC1595			–	± 0.75	–	
Scale Factor (Adjustable) $\left(K = \dfrac{2R_L}{I_3 R_X R_Y}\right)$		–	K		0.1	–	–
Input Resistance (f = 20 Hz)	MC1495	7	R_{INX}	–	20	–	MegOhms
	MC1595			–	35	–	
	MC1495		R_{INY}	–	20	–	
	MC1595			–	35	–	
Differential Output Resistance (f = 20 Hz)		8	R_o	–	300	–	k Ohms
Input Bias Current $I_{bx} = \dfrac{(I_9 + I_{12})}{2}$, $I_{by} = \dfrac{(I_4 + I_8)}{2}$	MC1495	6	I_{bx}	–	2.0	12	μA
	MC1595			–	2.0	8.0	
	MC1495		I_{by}	–	2.0	12	
	MC1595			–	2.0	8.0	
Input Offset Current $\lvert I_9 - I_{12}\rvert$	MC1495	6	$\lvert I_{iox}\rvert$	–	0.4	2.0	μA
	MC1595			–	0.2	1.0	
$\lvert I_4 - I_8\rvert$	MC1495		$\lvert I_{ioy}\rvert$	–	0.4	2.0	
	MC1595			–	0.2	1.0	
Average Temperature Coefficient of Input Offset Current		6	$\lvert TC_{Iio}\rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495			–	2.0	–	
(T_A = −55°C to +125°C)	MC1595			–	2.0	–	
Output Offset Current $\lvert I_{14} - I_2\rvert$		6	$\lvert I_{oo}\rvert$				μA
	MC1495			–	20	100	
	MC1595			–	10	50	
Average Temperature Coefficient of Output Offset Current		6	$\lvert TC_{Ioo}\rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495			–	20	–	
(T_A = −55°C to +125°C)	MC1595			–	20	–	
Frequency Response							
3.0 dB Bandwidth, R_L = 11 kΩ		9,10	BW_{3dB}	–	3.0	–	MHz
3.0 dB Bandwidth, R_L = 50 Ω (Transconductance Bandwidth)			$T_{BW3\ dB}$	–	80	–	MHz
3° Relative Phase Shift Between V_X and V_Y			f_ϕ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift			f_θ	–	30	–	kHz
Common Mode Input Swing (Either Input)		11	CMV				Vdc
	MC1495			±10.5	±12	–	
	MC1595			±11.5	±13	–	
Common Mode Gain (Either Input)		11	A_{CM}				dB
	MC1495			-40	-50	–	
	MC1595			-50	-60	–	
Common Mode Quiescent Output Voltage		12	V_{o1}	–	21	–	Vdc
			V_{o2}	–	21	–	
Differential Output Voltage Swing Capability		9	V_o	–	±14	–	V_{peak}
Power Supply Sensitivity		12	S^+	–	5.0	–	mV/V
			S^-	–	10	–	
Power Supply Current		12	I_7	–	6.0	7.0	mA
DC Power Dissipation		12	P_D	–	135	170	mW

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2-V_1, $V_{14}-V_1$, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, $V_{12}-V_7$, V_9-V_7, V_8-V_7, V_4-V_7)	ΔV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+I_{13}R_X)$ $\pm(6+I_3R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 750 5.0	 mW mW/°C
Operating Temperature Range MC1495 MC1595	T_A	 0 to +70 -55 to +125	°C °C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TEST CIRCUITS

FIGURE 4 — LINEARITY (USING NULL TECHNIQUE)

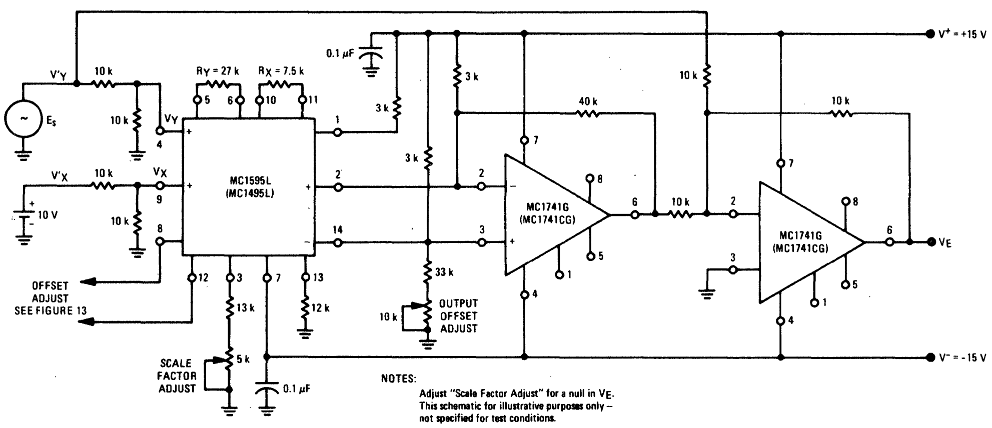
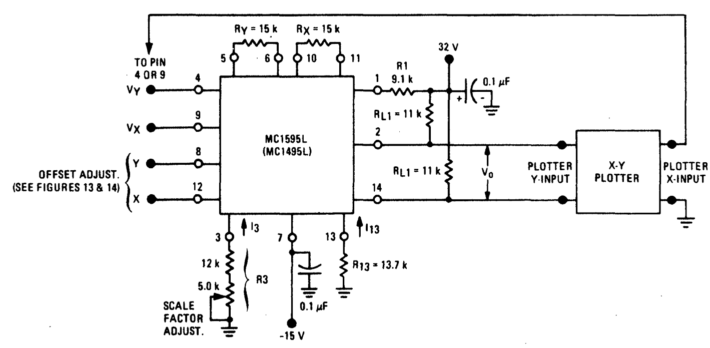


FIGURE 5 — LINEARITY (USING X-Y PLOTTER TECHNIQUE)



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TEST CIRCUITS (continued)

FIGURE 6 – INPUT AND OUTPUT CURRENT

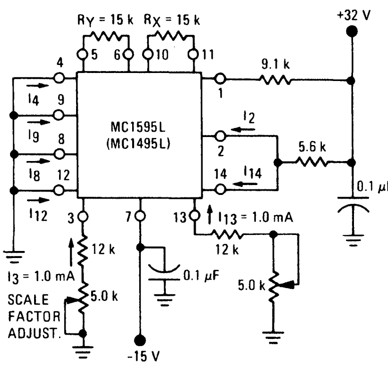


FIGURE 7 – INPUT RESISTANCE

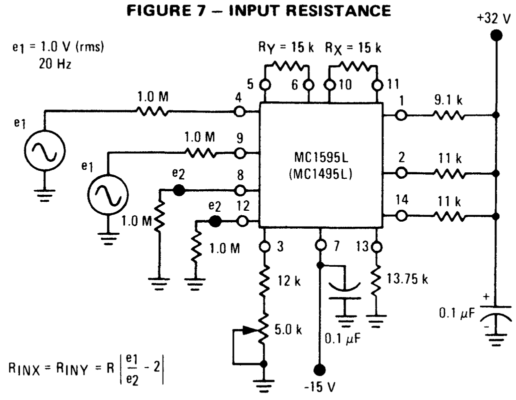


FIGURE 8 – OUTPUT RESISTANCE

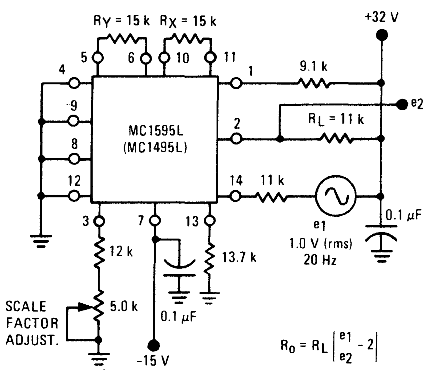


FIGURE 9 – BANDWIDTH (R_L = 11 kΩ)

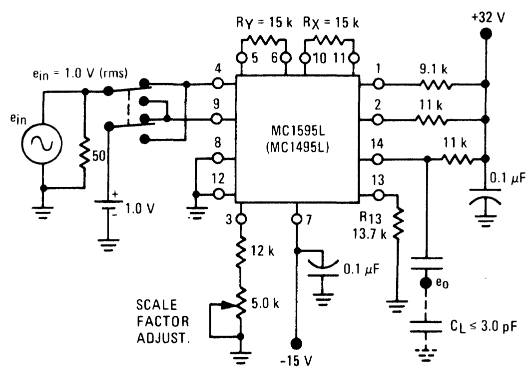


FIGURE 10 – BANDWIDTH (R_L = 50 Ω)

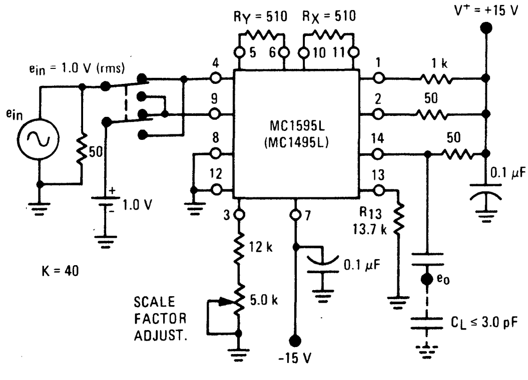
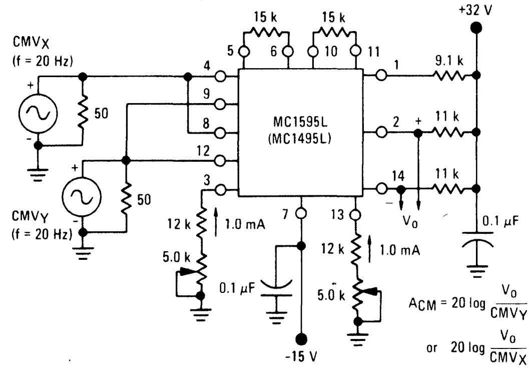


FIGURE 11 – COMMON-MODE GAIN and COMMON-MODE INPUT SWING



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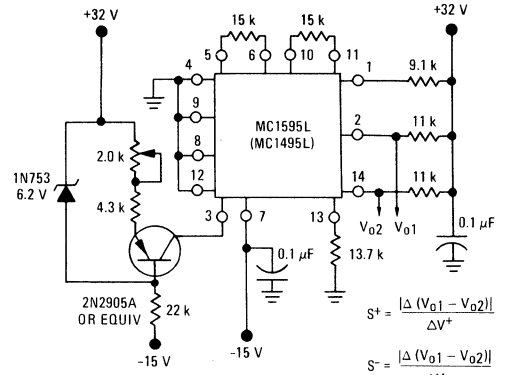
TEST CIRCUITS (continued)

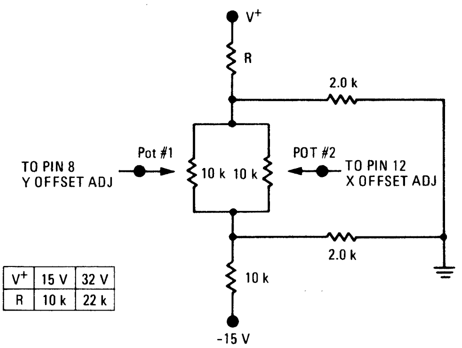
FIGURE 12 – POWER SUPPLY SENSITIVITY



$$S^+ = \frac{|\Delta(V_{o1} - V_{o2})|}{\Delta V^+}$$

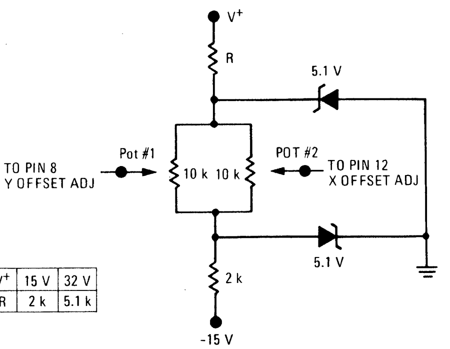
$$S^- = \frac{|\Delta(V_{o1} - V_{o2})|}{\Delta V^-}$$

FIGURE 13 – OFFSET ADJUST CIRCUIT



V^+	15 V	32 V
R	10 k	22 k

FIGURE 14 – OFFSET ADJUST CIRCUIT (ALTERNATE)



V^+	15 V	32 V
R	2 k	5.1 k

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TYPICAL CHARACTERISTICS

FIGURE 15 – LINEARITY versus TEMPERATURE

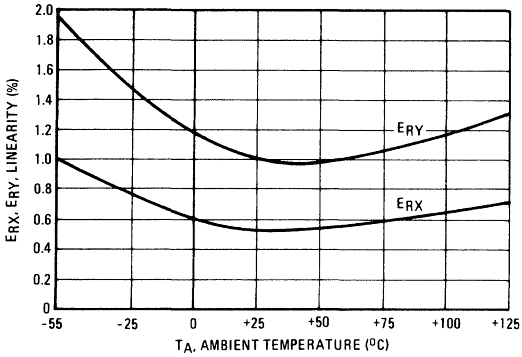


FIGURE 16 – SCALE FACTOR versus TEMPERATURE

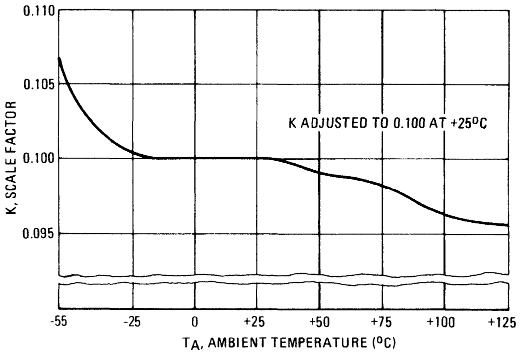


FIGURE 17 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

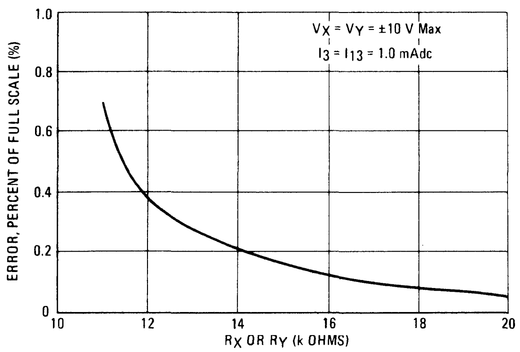


FIGURE 18 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

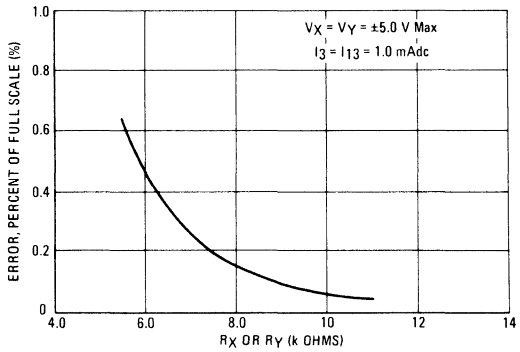
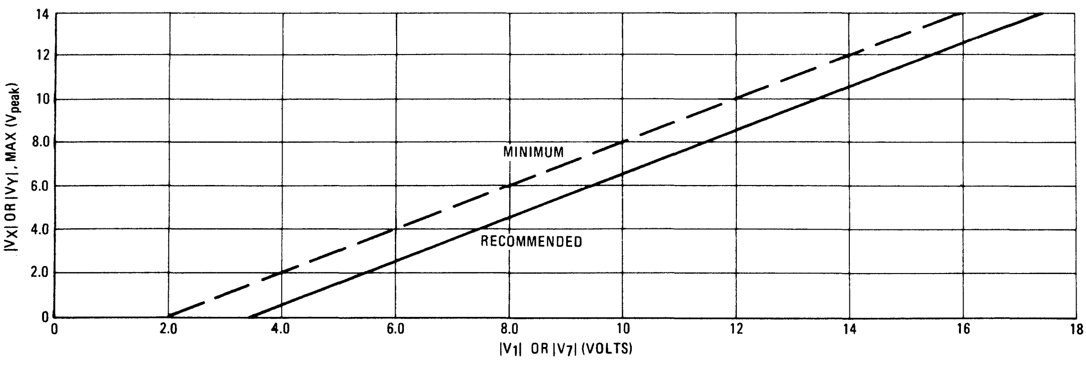


FIGURE 19 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



8

OPERATION AND APPLICATIONS INFORMATION

1. Theory of Operation

The MC1595 (MC1495) is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. The detailed theory of operation is covered in Application Note AN-489, Analysis and Basic Operation of the MC1595. The result of this analysis is that the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_3}$$

where I_A and I_B are the currents into pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

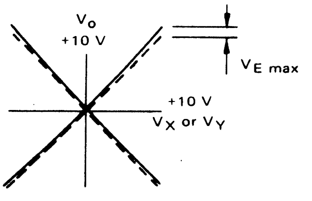
2. Design Considerations

2.1 General

The MC1595 (MC1495) permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

2.1.1 Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 volts, then the percentage error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X − Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_{E(max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

2.1.2 3 dB-Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

2.1.3 Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ maximum input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y.$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause non-linear operation.

Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ volts;

$$R_X = R_Y > \frac{10\ V}{1.0\ mA} = 10\ k\Omega.$$

The equation $I_A - I_B = \dfrac{2V_X V_Y}{R_X R_Y I_3}$

is derived from $I_A - I_B = \dfrac{2V_X V_Y}{(R_X + \frac{2kT}{qI_{13}})(R_Y + \frac{2kT}{qI_3}) I_3}$

with the assumption $R_X \gg \dfrac{2kT}{qI_{13}}$ and $R_Y \gg \dfrac{2kT}{qI_3}$.

At $T_A = +25°C$ and $I_{13} = I_3 = 1$ mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

Therefore, with $R_X = R_Y = 10\ k\Omega$ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of Section 3 (General Design Procedure) for further details.

2.1.4 Maximum Output Voltage Swing

The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7, and Q_8. This potential

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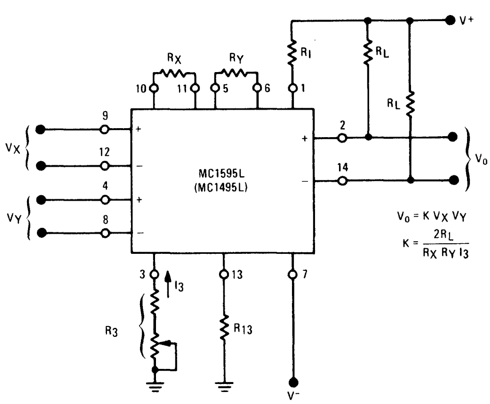
OPERATION AND APPLICATIONS INFORMATION (continued)

should be related so that negative swing at pins 2 or 14 does not saturate those transistors. See Section 3 for further information regarding selection of these potentials.

FIGURE 20 – BASIC MULTIPLIER



If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

3. General Design Procedure

Selection of component values is best demonstrated by the following example: assume resistive dividers are used at the X and Y inputs to limit the maximum multiplier input to ±5.0 volts ($V_X = V_{Y[max]}$) for a ±10-volt input ($V_X' = V_Y'_{[max]}$). (See Figure 21). If an overall scale factor of 1/10 is desired, then

$$V_o = \frac{V_X' \, V_Y'}{10} = \frac{(2V_X)\,(2V_Y)}{10} = 4/10\, V_X V_Y \, .$$

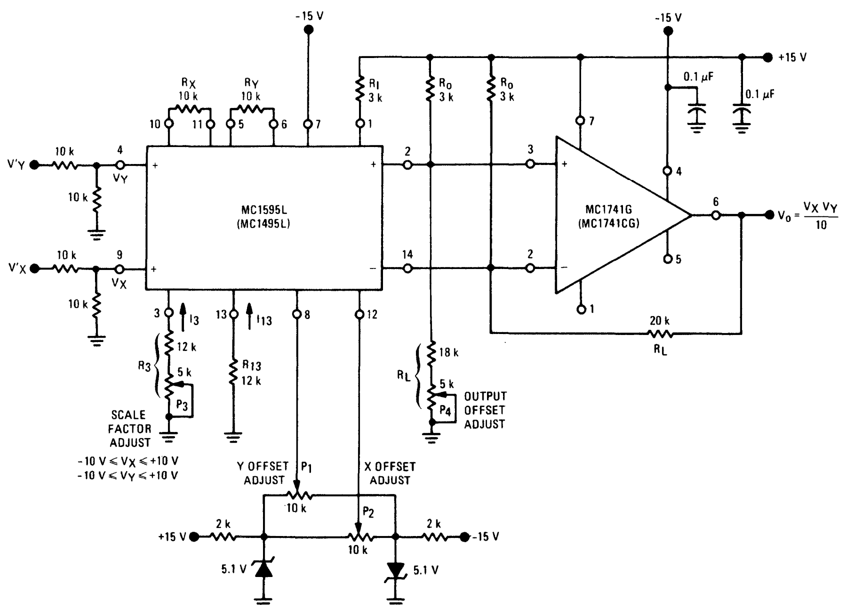
Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The first step is to select current I_3 and current I_{13}. There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be one or two milliamperes. Further, I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1 \text{ mA}.$$

To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between pin 13 and ground, and between pin 3 and ground. From the schematic shown in Figure 3,

FIGURE 21 – MULTIPLIER WITH OP-AMPL. LEVEL SHIFT



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OPERATION AND APPLICATIONS INFORMATION (continued)

it can be seen that the resistor values necessary are given by:

$$R_{13} + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_{13}}$$

$$R_3 + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_3}$$

Let $V^- = -15\ V$

Then $R_{13} + 500 = \frac{14.3\ V}{1\ mA}$ or $R_{13} = 13.8\ k\Omega$

Let $R_{13} = 12\ k\Omega$

Similarly, $R_3 = 13.8\ k\Omega$

Let $R_3 = 15\ k\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the single resistor would have a value of one-half the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \qquad \frac{V_Y}{R_Y} < I_3.$$

A good rule of thumb is to make $I_3 R_Y \geqslant 1.5\ V_{Y(max)}$ and $I_{13} R_X \geqslant 1.5\ V_{X(max)}$.

The larger the $I_3 R_Y$ and $I_{13} R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y = 10\ k\Omega$

Then $I_3 R_Y = 10\ V$

$I_{13} R_X = 10\ V$

since $V_{X(max)} = V_{Y(max)} = 5.0$ volts the value of $R_X = R_Y = 10\ k\Omega$ is sufficient.

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_X R_Y I_3} = \frac{4}{10}$$

or

$$\frac{(2)\ (R_L)}{(10\ k)\ (10\ k)\ (1\ mA)} = \frac{4}{10}$$

Thus $R_L = 20\ k\Omega$.

Step 4. To determine what power-supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_X' = V_Y' = 10$ V or $V_X = 5.0$ V, $V_Y = 5.0$ V), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 are at a potential which is two diode-drops below the voltage at pin 1. Thus, the voltage at pin 1 should be about two volts higher than the maximum input voltage. Therefore, to handle +5.0 volts at the inputs, the voltage at pin 1 must be at least +7.0 volts. Let $V_1 = 9.0$ Vdc.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, R_1 from pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

Let $V^+ = +15\ V$

Then $R_1 = \frac{15\ V - 9\ V}{(2)\ (1\ mA)}$

$R_1 = 3\ k\Omega$.

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode-drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive-supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

Step 5. Level Shifting

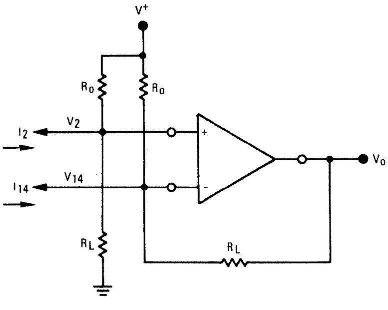
For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_o = (I_2 - I_{14})\ R_L$$

And since $I_A - I_B = I_2 - I_{14} = \frac{2I_X I_Y}{I_3} = \frac{2\ V_X V_Y}{I_3 R_X R_Y}$

Then $V_o = \frac{2R_L V_X' V_Y'}{4R_X R_X I_3}$ where $V_X' V_Y'$ is the voltage at the input to the voltage dividers.

FIGURE 22 — LEVEL SHIFT CIRCUIT



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OPERATION AND APPLICATIONS INFORMATION (continued)

The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common-mode input voltage range as well as a high common-mode rejection ratio. The MC1556, and MC1741 operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20 kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 volts. From this information, R_o can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V_2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_o}$$

And for this example, $\dfrac{11\ \text{V}}{20\ \text{k}\Omega} + 1\ \text{mA} = \dfrac{15\ \text{V} - 11\ \text{V}}{R_o}$

Solving for R_o, $R_o = 2.6\ \text{k}\Omega$

Thus, select $R_o = 3.0\ \text{k}\Omega$

For $R_o = 3.0\ \text{k}\Omega$, the voltage at pins 2 and 14 is calculated to be

$$V_2 = V_{14} = 10.4\ \text{volts.}$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity, and R_X decreased somewhat so as not to materially affect the X linearity, this avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1595 (MC1495) allows the user to to optimize its performance for various input and output signal levels.

4. Offset and Scale Factor Adjustment

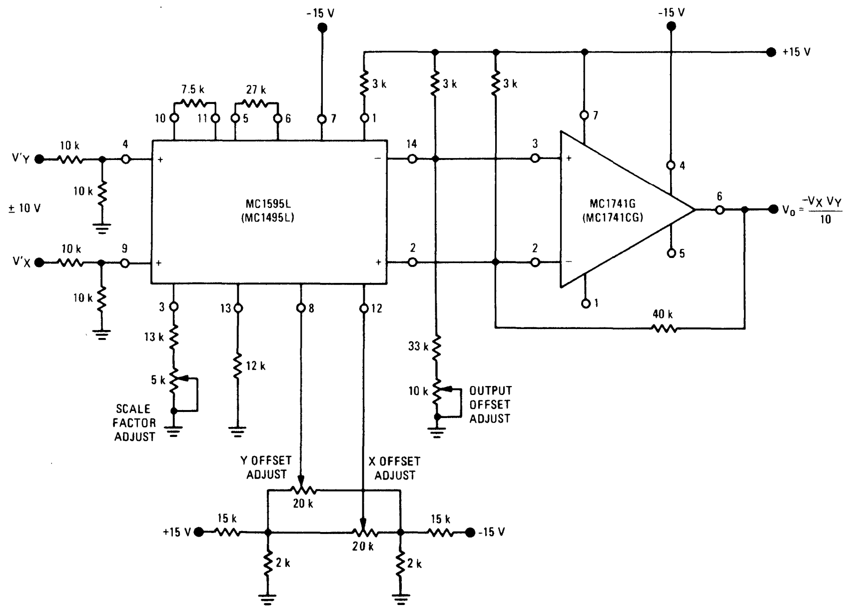
4.1 Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output-offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function:

$$V_o = K(V_X \pm V_{IOX} \pm V_{X\,off})(V_Y \pm V_{IOY} \pm V_{Y\,off}) \pm V_{oo} \quad (1)$$

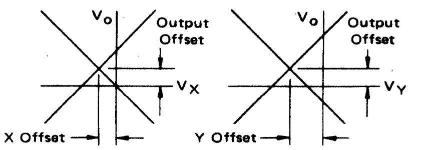
Where K = scale factor
V_X = X input voltage
V_Y = Y input voltage
V_{IOX} = X input offset voltage
V_{IOY} = Y input offset voltage
$V_{X\,off}$ = X input offset adjust voltage
$V_{Y\,off}$ = Y input offset adjust voltage
V_{oo} = output offset voltage.

FIGURE 23 – MULTIPLIER WITH IMPROVED LINEARITY



OPERATION AND APPLICATIONS INFORMATION (continued)

X, Y and Output Offset Voltages



For most dc applications, all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (See Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

4.2 Scale Factor

The scale factor, K, is set by P_3(Figure 21). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one-half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (See Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see Section 3, General Design Procedure).

4.3 Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 21)

1. X Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 4)
   (b) Connect "X" input (pin 9) to ground
   (c) Adjust X offset potentiometer, P_2, for an ac null at the output
2. Y Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 9)
   (b) Connect "Y" input (pin 4) to ground
   (c) Adjust "Y" offset potentiometer, P_1, for an ac null at the output
3. Output Offset
   (a) Connect both "X" and "Y" inputs to ground
   (b) Adjust output offset potentiometer, P_4, until the output voltage V_o is zero volts dc
4. Scale Factor
   (a) Apply +10 Vdc to both the "X" and "Y" inputs
   (b) Adjust P_3 to achieve + 10.00 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1595 (MC1495) depends upon the characteristics of potentiometers P_1 through P_4. Multi-turn, infinite resolution potentiometers with low-temperature coefficients are recommended.

5. DC Applications

5.1 Multiply

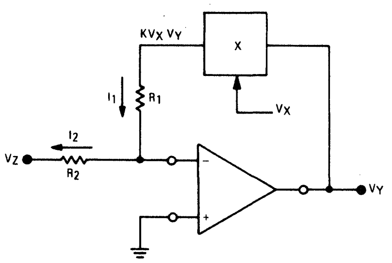
The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large – however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

5.2 Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_o = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

1. AC Procedure:
   (a) Connect oscillator (1 kHz, 15 Vpp) to input
   (b) Monitor output at 2 kHz with tuned voltmeter and adjust P_3 for desired gain (be sure to peak response of the voltmeter)
   (c) Tune voltmeter to 1 kHz and adjust P_1 for a minimum output voltage
   (d) Ground input and adjust P_4 (output offset) for zero volts dc output
   (e) Repeat steps a through d as necessary.
2. DC Procedure:
   (a) Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_o = 0.0$ Vdc
   (b) Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y input offset potentiometer) such that the output voltage is +0.100 volts
   (c) Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is +10.00 volts
   (d) Set $V_X = V_Y = -10$ Vdc. Repeat steps a through d as necessary.

FIGURE 24 – BASIC DIVIDE CIRCUIT



5.3 Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (-) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \tag{1}$$

Solving for V_Y,

$$V_Y = \frac{-R1}{R2\,K}\,\frac{V_Z}{V_X}. \tag{2}$$

If R1 = R2

$$V_Y = \frac{-V_Z}{KV_X} \tag{3}$$

If R1 = KR2

$$V_Y = \frac{-V_Z}{V_X}. \tag{4}$$

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OPERATION AND APPLICATIONS INFORMATION (continued)

Hence, the output voltage is the ratio of V_Z to V_X and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be

$$V_Y = -\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X} + \frac{\Delta E}{K V_X}, \qquad (5)$$

where ΔE is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y. For example, assume that R1 = R2, and K = 1/10. For these conditions the output of the divide circuit is given by:

$$V_Y = \frac{-10\,V_Z}{V_X} + \frac{10\,\Delta E}{V_X}. \qquad (6)$$

From equation 6, it is seen that only when V_X = 10 V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small, (0.1 volt) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from equation (5),

$$P.E._D = \frac{\dfrac{\Delta E}{K V_X}}{\left[\dfrac{R1}{R2\,K}\right]\dfrac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z}. \qquad (7)$$

From equation 7, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25.

1. The input voltage (V'_X) must be greater than zero and must be positive. This insures that the current out of pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z.
2. Pins 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

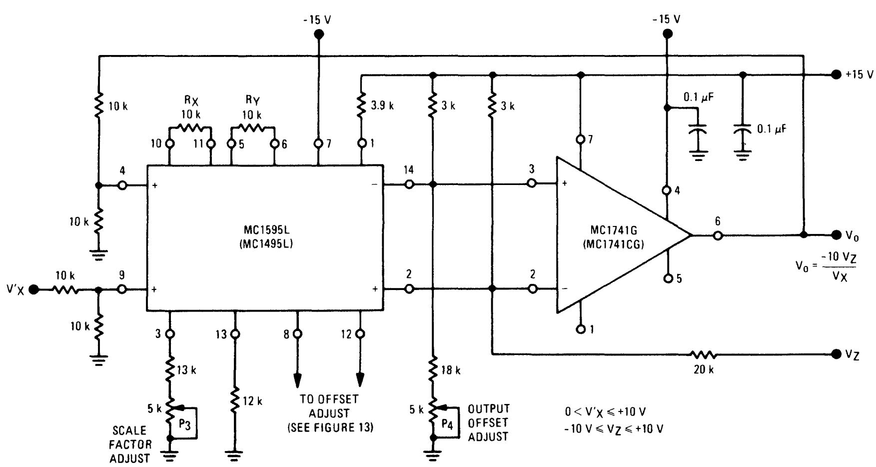
A Suggested Adjustment Procedure for the Divide Circuit

1. Set V_Z = 0 volts and adjust the output offset potentiometer (P_4) until the output voltage (V_o) remains at some (not necessarily zero) constant value as V_X' is varied between +1.0 volt and +10 volts.
2. Keep V_Z at 0 volts, set V_X' at +10 volts and adjust the Y input offset potentiometer (P_1) until V_o = 0 volts.
3. Let V_X' = V_Z and adjust the X input offset potentiometer (P_2) until the output voltage remains at some (not necessarily − 10 volts) constant value as V_Z = V_X' is varied between +1.0 and +10 volts.
4. Keep V_X' = V_Z and adjust the scale factor potentiometer (P_3) until the average value of V_o is − 10 volts as V_Z = V_X' is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

5.4 Square Root

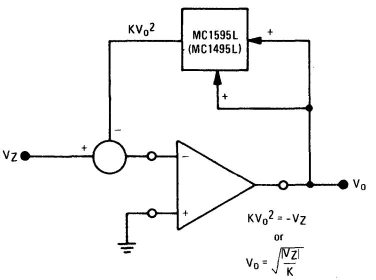
A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function

FIGURE 25 — DIVIDE CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 26 – BASIC SQUARE ROOT CIRCUIT



as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up.

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set V_Z to −0.01 volts and adjust P_4 (output offset) for V_o = +0.316 volts, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set V_Z to −0.9 volts and adjust P_2 (X adjust) for V_o = +3.0 volts.
3. Set V_Z to −10 volts and adjust P_3 (scale factor adjust) for V_o = +10 volts.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

6. AC Applications

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications.

6.1 Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling.

$$e_o = KE^2 \cos^2 \omega t$$

$$e_o = \frac{KE^2}{2} (1 + \cos 2\omega t).$$

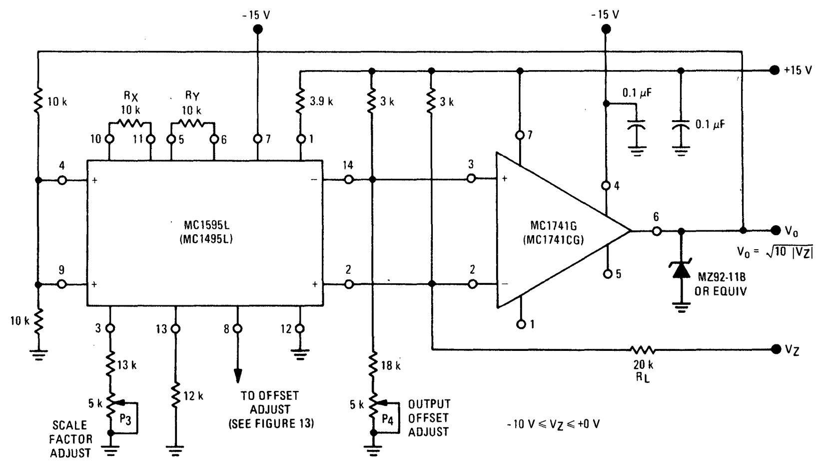
A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplifier. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15-volt supplies are used. An input dynamic range of 5.0 volts peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

A slightly modified version of the MC1595 (MC1495) – the MC1596 (MC1496) – has been successfully used as a doubler to obtain 400 MHz. (See Figure 28.)

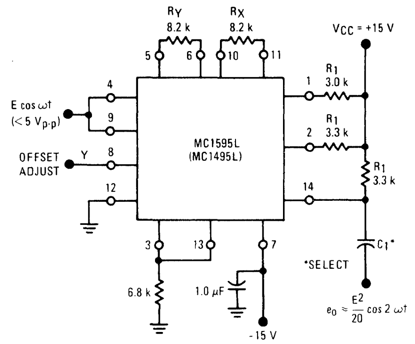
6.2 Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

FIGURE 27 – SQUARE ROOT CIRCUIT



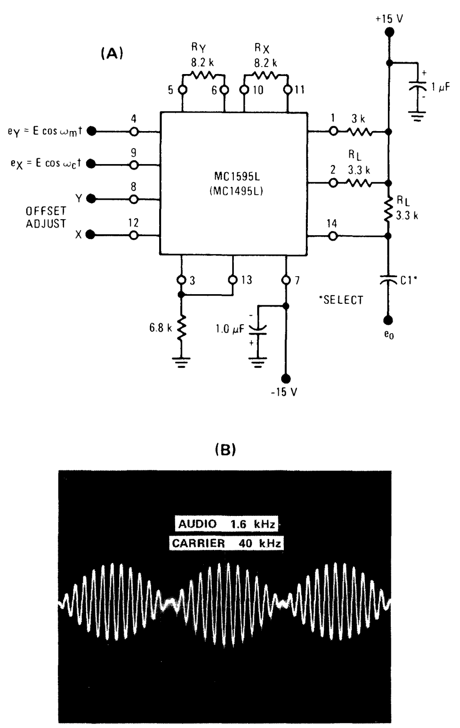
OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 28 – FREQUENCY DOUBLER



When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

FIGURE 29 – BALANCED MODULATOR



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)(E_c \cos \omega_c t) =$$

$$\frac{KE_cE_m}{2}\left[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t\right]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier; a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form

$$e_{ssb} = A \cos(\omega_c + \omega_m)t$$

and if multiplied by the appropriate carrier waveform, $\cos \omega_c t$,

$$e_{ssb}e_{carrier} = \frac{AK}{2}\left[\cos(2\omega_c + \omega_m)t + \cos(\omega_c)t\right].$$

If the frequency of the band-limited carrier signal, ω_c, is ascertained in advance the designer can insert a low-pass filter and obtain the (AK/2) ($\cos \omega_c t$) term with ease. He also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low-pass filter.

6.3 Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulation, when a dc term is added to the modulating signal with the Y offset adjust potentiometer. (See Figure 30.)

Here, the identity is

$$E_m(1 + m \cos \omega_m t) E_c \cos \omega_c t = KE_mE_c \cos \omega_c t +$$

$$\frac{KE_mE_cm}{2}\left[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t\right]$$

where m indicates the degree of modulation. Since m is adjustable, via potentiometer P_1, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where ω_c and ω_m are the same as in the balanced-modulator example.

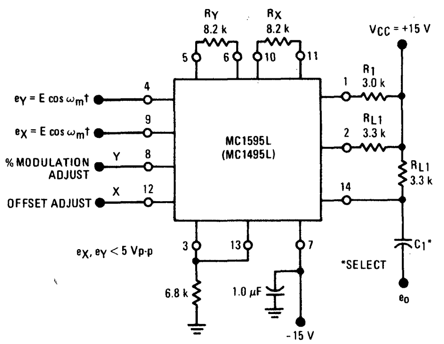
8

6.4 Linear Gain Control

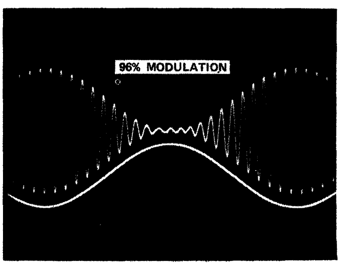
To obtain linear gain control, the designer can feed to one of the two MC1595 (MC1495) inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sine wave, 1.0 volt peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage V_C is 0 to +1.0 volt. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200-kHz operating frequency, load resistors of 100 ohms were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency. (See Figure 31.)

OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 30 – AMPLITUDE MODULATION



(B)



The signal is applied to the unit's Y input. Since the total input range is limited to 1.0 volt p-p, a 2.0-volt swing, a current source of 2.0 mA and an R_Y value of 1.0 kilohm is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X input varies between 0 and +1.0 volt, the current source selected was 1.0 mA and the R_X value chosen was 2.0 kilohms. This also insures linear operation over the X input dynamic range.

Choosing R_L = 100 assures wide-bandwidth operation. Hence, the scale factor for this configuration is

$$K = \frac{R_L}{R_X R_Y I_3}$$

$$= \frac{100}{(2\text{ k})(1\text{ k})(2 \times 10^{+3})} V^{-1}$$

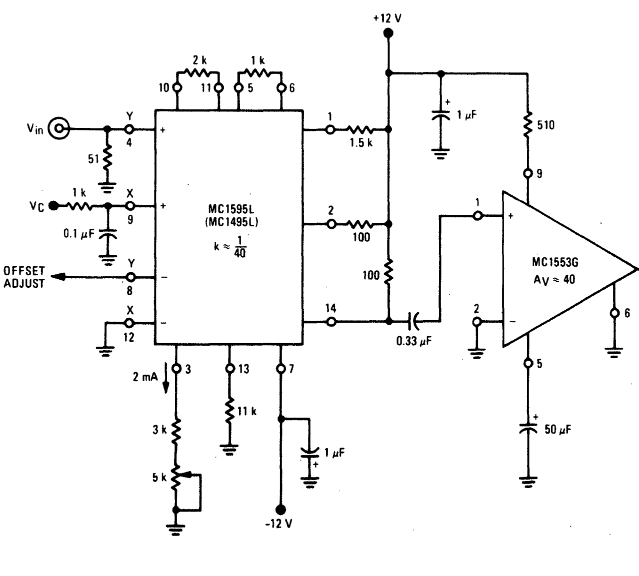
$$= \frac{1}{40} V^{-1}.$$

The 2 in the numerator of the equation is missing in this scale-factor expression because the output is single-ended and ac coupled.

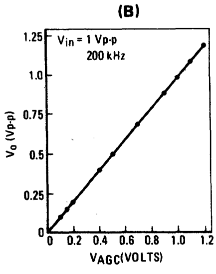
To recover the gain, an MC1552 video amplifier with a gain of 40 is used. An operational amplifier also could have been used with frequency compensation to allow a gain of 40 at 200 kHz. The MC1539 operational amplifier can be tailored for this use; and the MC1520 operational amplifier does it directly.

FIGURE 31 – LINEAR GAIN CONTROL

(A)



(B)



NOTE:
Linear gain control of a 1-volt peak-to-peak signal is performed with a 0-to-1-volt control voltage. If V_C is 0.5 volt the output will be 0.5 volt p-p.

8

OPERATIONS AND APPLICATIONS INFORMATION INDEX

MC1596
MC1496

BALANCED MODULATOR-DEMODULATOR

Specifications and Applications Information

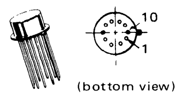
MONOLITHIC BALANCED MODULATOR – DEMODULATOR

. . . designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

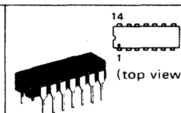
- Excellent Carrier Suppression – 65 dB typ @ 0.5 MHz
  – 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common-Mode Rejection – 85 dB typ

BALANCED MODULATOR – DEMODULATOR

INTEGRATED CIRCUIT SILICON EPITAXIAL PASSIVATED



CASE 602A
Metal Package
Suffix G



CASE 632 (TO-116)
Ceramic Package
Suffix L

FIGURE 1 – SUPPRESSED-CARRIER OUTPUT WAVEFORM

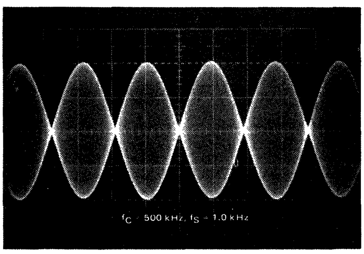


FIGURE 2 – AMPLITUDE-MODULATION OUTPUT WAVEFORM

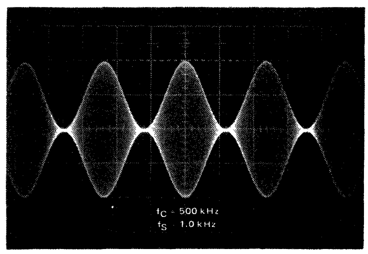


FIGURE 3 – SUPPRESSED-CARRIER SPECTRUM

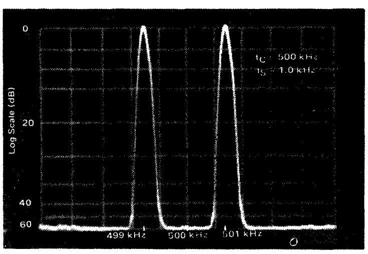


FIGURE 4 – AMPLITUDE-MODULATION SPECTRUM

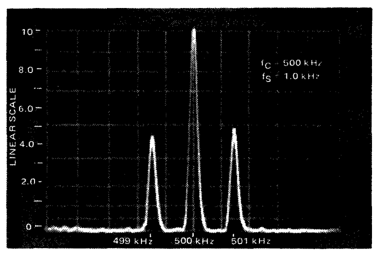
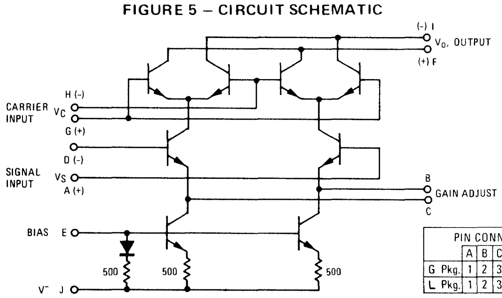


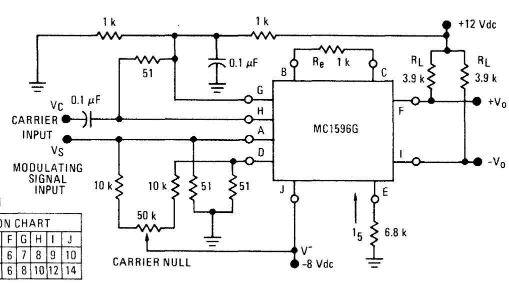
FIGURE 5 – CIRCUIT SCHEMATIC



PIN CONNECTION CHART

	A	B	C	D	E	F	G	H	I	J
G Pkg.	1	2	3	4	5	6	7	8	9	10
L Pkg.	1	2	3	4	5	6	8	10	12	14

FIGURE 6 – TYPICAL MODULATOR CIRCUIT



See Packaging Information Section for outline dimensions.

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage ($V_6 - V_7$, $V_8 - V_1$, $V_9 - V_7$, $V_9 - V_8$, $V_7 - V_4$, $V_7 - V_1$, $V_8 - V_4$, $V_6 - V_8$, $V_2 - V_5$, $V_3 - V_5$)	ΔV	30	Vdc
Differential Input Signal	$V_7 - V_8$ $V_4 - V_1$	+5.0 $\pm(5+I_5R_e)$	Vdc
Maximum Bias Current	I_5	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		575	mW
Derate above T_A = +25°C		3.85	mW/°C
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Temperature Range	T_A		°C
MC1496		0 to +70	
MC1596		-55 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS* (V^+ = +12 Vdc, V^- = -8.0 Vdc, I_5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C unless otherwise noted) (All input and output characteristics are single-ended unless otherwise noted.)

Characteristic	Fig	Note	Symbol	MC1596 Min	MC1596 Typ	MC1596 Max	MC1496 Min	MC1496 Typ	MC1496 Max	Unit
Carrier Feedthrough	7	1	V_{CFT}							µV(rms)
V_C = 60 mV(rms) sine wave and f_C = 1.0 kHz				–	40	–	–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	–	140	–	
V_C = 300 mVp-p square wave:										mV(rms)
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.2	–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	100	–	20	200	
Carrier Suppression	7	2	V_{CS}							dB
f_S = 10 kHz, 300 mV(rms)										
f_C = 500 kHz, 60 mV(rms) sine wave				50	65	–	40	65	–	
f_C = 10 MHz, 60 mV(rms) sine wave				–	50	–	–	50	–	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 ohms)	10	8	BW_{3dB}							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave f_S = 1.0 kHz, 300 mV(rms) sine wave				–	300	–	–	300	–	
Signal Input Port, V_S = 300 mV(rms) sine wave $\lvert V_C \rvert$ = 0.5 Vdc				–	80	–	–	80	–	
Signal Gain V_S = 100 mV(rms), f = 1.0 kHz; $\lvert V_C \rvert$ = 0.5 Vdc	12	3	A_{VS}	2.5	3.5	–	2.5	3.5	–	V/V
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	8	–								
Parallel Input Resistance			r_{ip}	–	200	–	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz	8	–								
Parallel Output Resistance			r_{op}	–	40	–	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	–	5.0	–	pF
Input Bias Current $I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_7 + I_8}{2}$	9	–								µA
			I_{bS}	–	12	25	–	12	30	
			I_{bC}	–	12	25	–	12	30	
Input Offset Current $I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$	9	–								µA
			$\lvert I_{ioS} \rvert$	–	0.7	5.0	–	0.7	7.0	
			$\lvert I_{ioC} \rvert$	–	0.7	5.0	–	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = -55°C to +125°C)	9	–	$\lvert TC_{Iio} \rvert$	–	2.0	–	–	2.0	–	nA/°C
Output Offset Current ($I_6 - I_9$)	9	–	$\lvert I_{oo} \rvert$	–	14	50	–	14	80	µA
Average Temperature Coefficient of Output Offset Current (T_A = -55°C to +125°C)	9	–	$\lvert TC_{Ioo} \rvert$	–	90	–	–	90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	11	4	CMV	–	5.0	–	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C \rvert$ = 0.5 Vdc	11	–	ACM	–	-85	–	–	-85	–	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	12	–	V_o	–	8.0	–	–	8.0	–	Vdc
Differential Output Voltage Swing Capability	12	–	V_{out}	–	8.0	–	–	8.0	–	Vp-p
Power Supply Current	9	6								mAdc
$I_6 + I_9$			I_D^+	–	2.0	3.0	–	2.0	4.0	
I_{10}			I_D^-	–	3.0	4.0	–	3.0	5.0	
DC Power Dissipation	9	5	P_D	–	33	–	–	33	–	mW

* Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

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GENERAL OPERATING INFORMATION *

Note 1 — Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 7).

Note 2 — Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 24. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair — or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Note 3 and Figure 22). Note also that an optimum carrier level is recommended in Figure 24 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 — Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26 \text{ mV}}{I_5 \text{ (mA)}}.$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5

$$V_S \leq I_5 R_E \text{ (Volts peak)}.$$

Note that in the test circuit of Figure 12, V_S corresponds to a maximum value of 1 volt peak.

Note 4 — Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 — Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_9 = V_6$, $I_5 = I_6 = I_9$ and ignoring base current, $P_D = 2\, I_5\, (V_6 - V_{10}) + I_5\, (V_5 - V_{10})$ where subscripts refer to pin numbers.

Note 6 — Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for R_e equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B << I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V^- - \phi}{I_5} - 500\ \Omega$$

where: R_5 is the resistor between pin 5 and ground
ϕ = 0.75 V at T_A = +25°C

The MC1596 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L.$$

Note 7 — Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30 \text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7 \text{ Vdc}.$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_9, \quad V_7 = V_8, \quad V_1 = V_4.$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 — Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$y_{21C} = \left.\frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}}\right|_{V_o = 0}.$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$y_{21S} = \left.\frac{i_o \text{ (signal)}}{v_s \text{ (signal)}}\right|_{V_c = 0.5 \text{ Vdc},\ V_o = 0}.$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

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Note 9 – Coupling and Bypass Capacitors C_1 and C_2

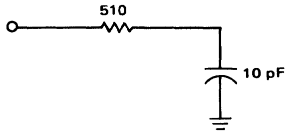
Capacitors C_1 and C_2 (Figure 7) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Note 10 – Output Signal, V_o

The output signal is taken from pins 6 and 9, either balanced or single-ended. Figure 14 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Note 11 – Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

FIGURE 7 – CARRIER REJECTION AND SUPPRESSION

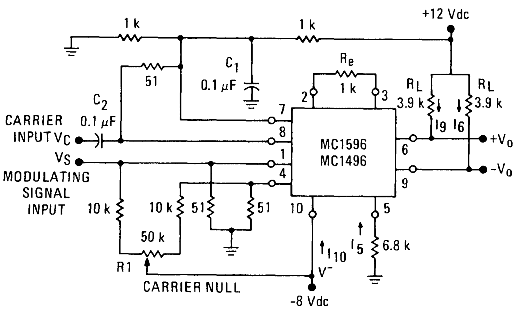


FIGURE 8 – INPUT-OUTPUT IMPEDANCE

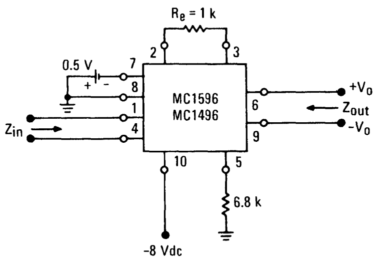


FIGURE 9 – BIAS AND OFFSET CURRENTS

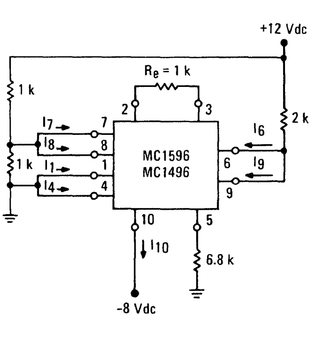
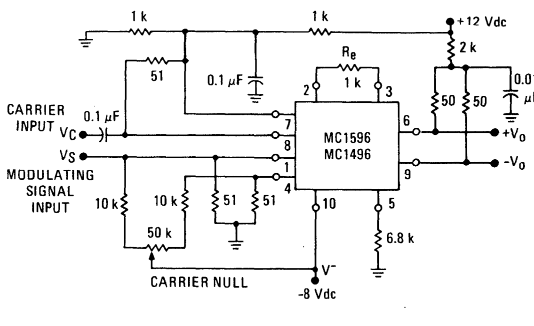


FIGURE 10 – TRANSCONDUCTANCE BANDWIDTH



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TEST CIRCUITS (continued)

FIGURE 11 – COMMON-MODE GAIN

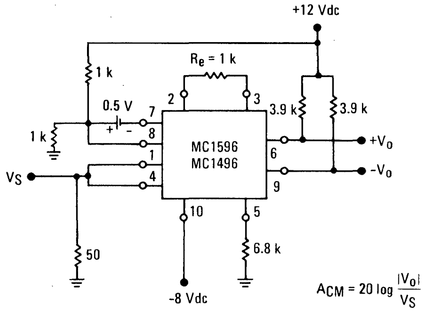
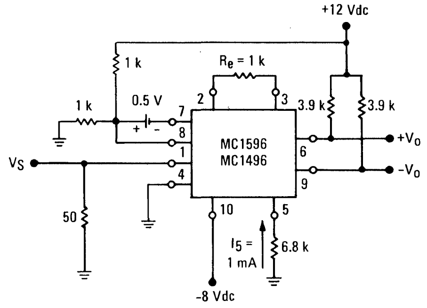


FIGURE 12 – SIGNAL GAIN AND OUTPUT SWING



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 7, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 13 – SIDEBAND OUTPUT versus CARRIER LEVELS

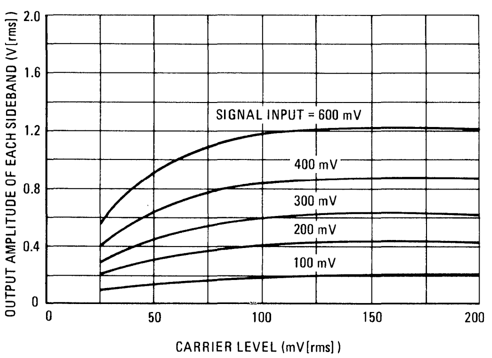


FIGURE 14 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

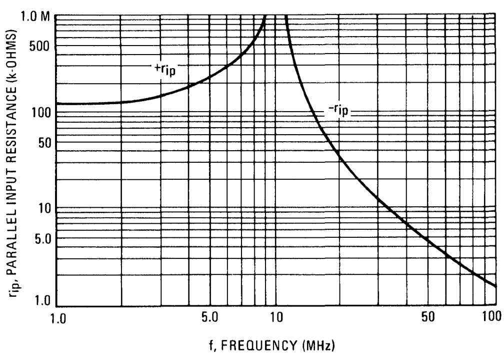


FIGURE 15 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

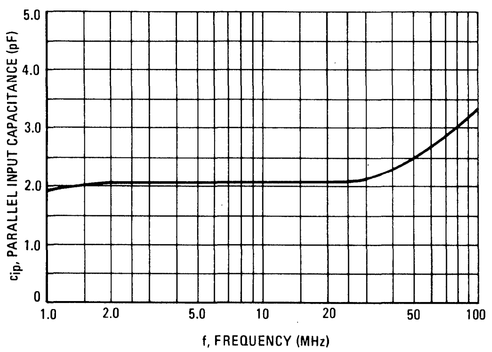
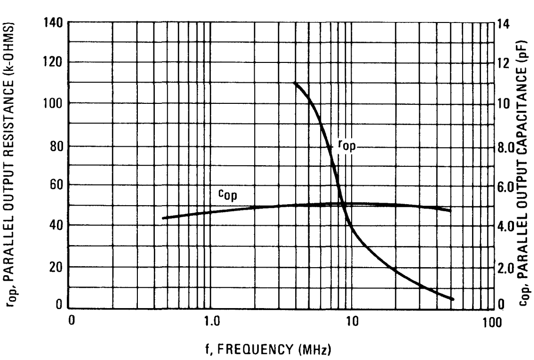


FIGURE 16 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 7, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 17 – SIDEBAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

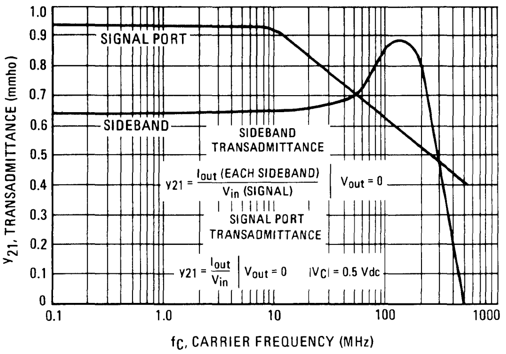


FIGURE 18 – CARRIER SUPPRESSION versus TEMPERATURE

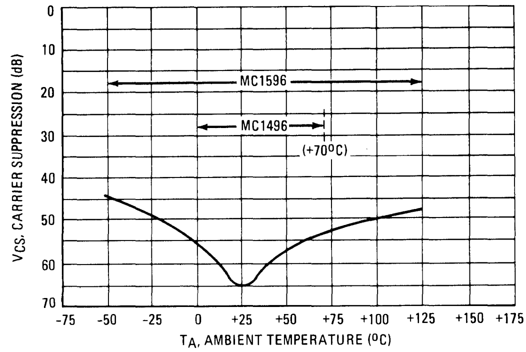


FIGURE 19 – SIGNAL-PORT FREQUENCY RESPONSE

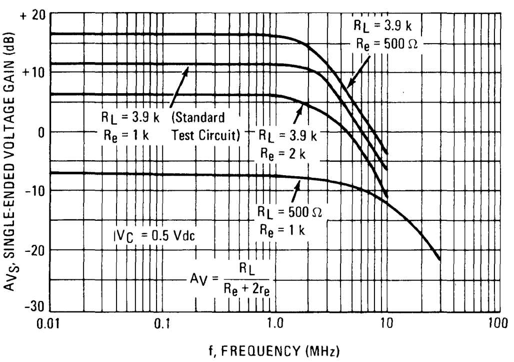


FIGURE 20 – CARRIER SUPPRESSION versus FREQUENCY

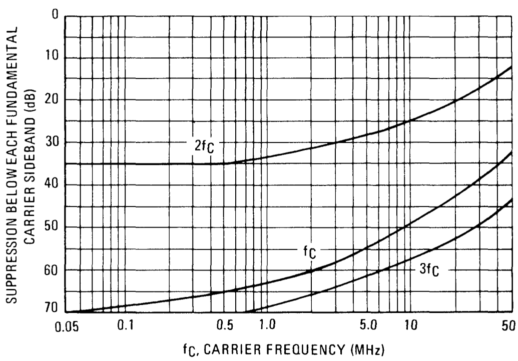


FIGURE 21 – CARRIER FEEDTHROUGH versus FREQUENCY

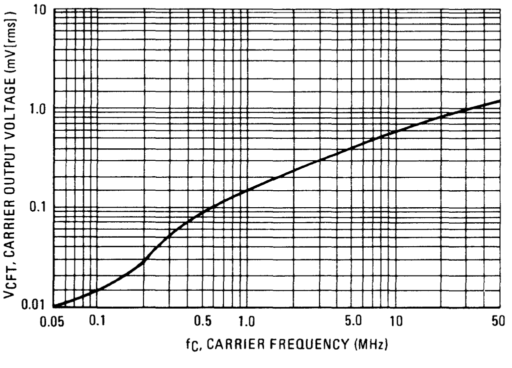
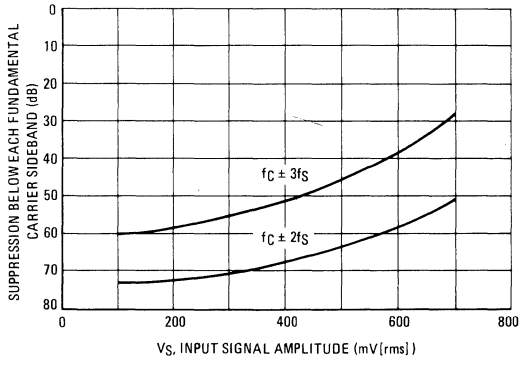


FIGURE 22 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



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TYPICAL CHARACTERISTICS (continued)

FIGURE 23 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

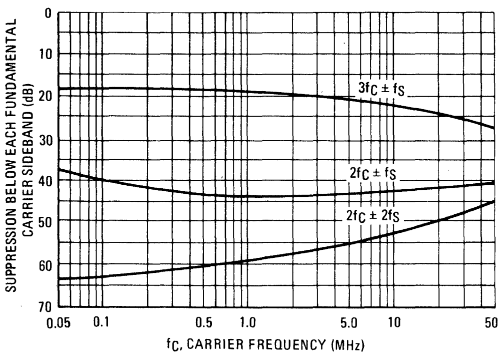
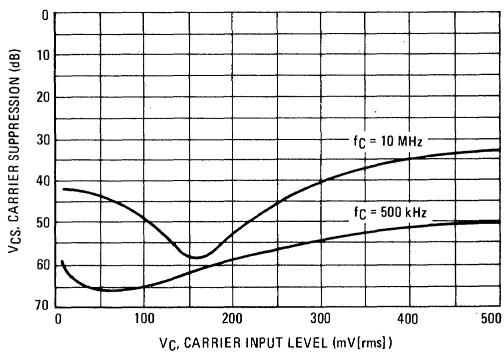


FIGURE 24 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 5.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_5)(R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level dc
2) High-level dc
3) Low-level ac
4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

OPERATIONS INFORMATION (continued)

FIGURE 25 – TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637 R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

NOTES:
1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at +25°C;

$$r_e \approx \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26 \text{ mV at room temperature.}$$

APPLICATION INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 7 and 8 should be increased to 1.0 μF. Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR (+12 Vdc SINGLE SUPPLY)

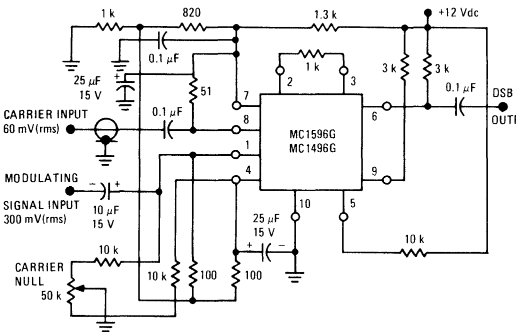


FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

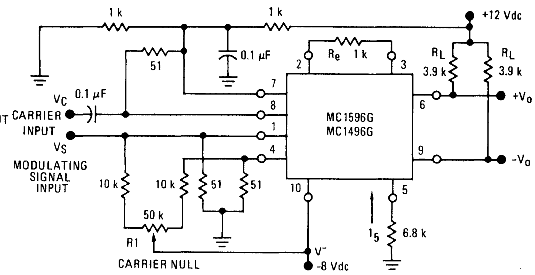


FIGURE 28 – AM MODULATOR CIRCUIT

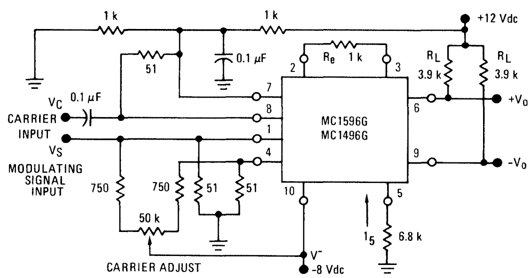


FIGURE 29 – PRODUCT DETECTOR (+12 Vdc SINGLE SUPPLY)

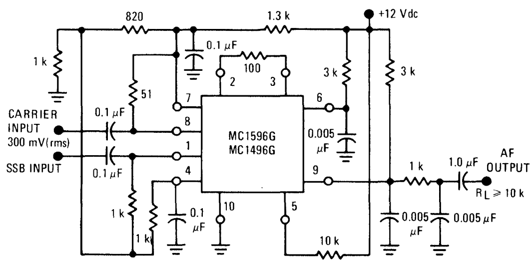
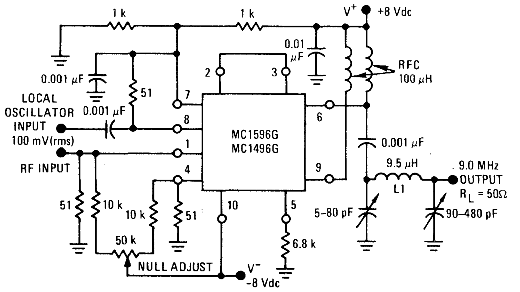
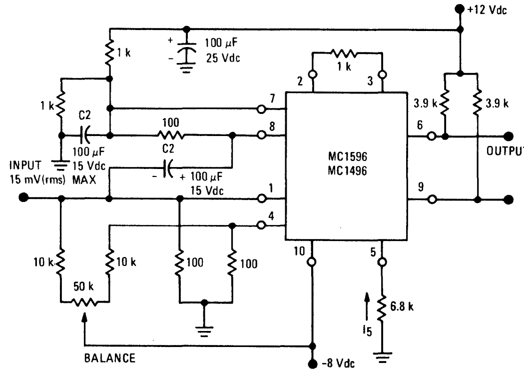


FIGURE 30 – DOUBLY BALANCED MIXER (BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)



L1 = 44 TURNS AWG NO. 28 ENAMELED WIRE, WOUND ON MICROMETALS TYPE 44-6 TOROID CORE.

FIGURE 31 – LOW-FREQUENCY DOUBLER

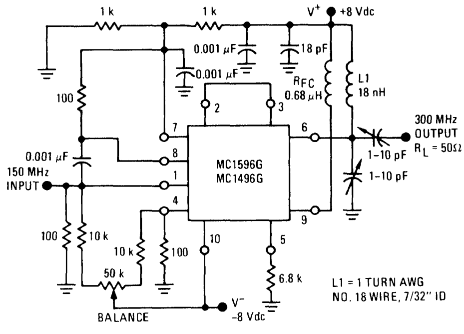


Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

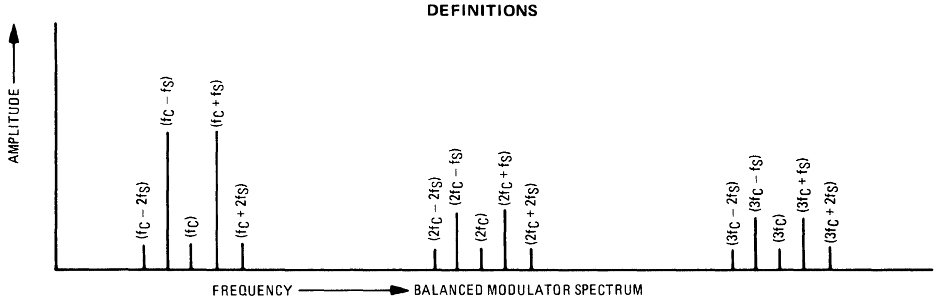
8

TYPICAL APPLICATIONS (continued)

FIGURE 32 – 150 to 300 MHz DOUBLER



DEFINITIONS



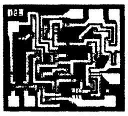
f_C	CARRIER FUNDAMENTAL	$f_C \pm nf_S$	FUNDAMENTAL CARRIER SIDEBAND HARMONICS
f_S	MODULATING SIGNAL	nf_C	CARRIER HARMONICS
$f_C \pm f_S$	FUNDAMENTAL CARRIER SIDEBANDS	$nf_C \pm nf_S$	CARRIER HARMONIC SIDEBANDS

8

MC1709
MC1709C

OPERATIONAL AMPLIFIERS

MONOLITHIC OPERATIONAL AMPLIFIER

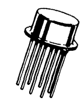


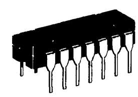
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics A_{VOL} = 45,000 typical
- Low Temperature Drift – ±3.0 μV/^{o}C
- Large Output Voltage Swing – ±14 V typical @ ±15 V Supply
- Low Output Impedance – Z_{out} = 150 ohms typical

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT
MONOLITHIC SILICON

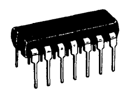
G SUFFIX
METAL PACKAGE
CASE 601

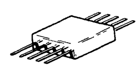




L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

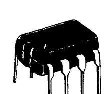
P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1709C only)





F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1709C only)



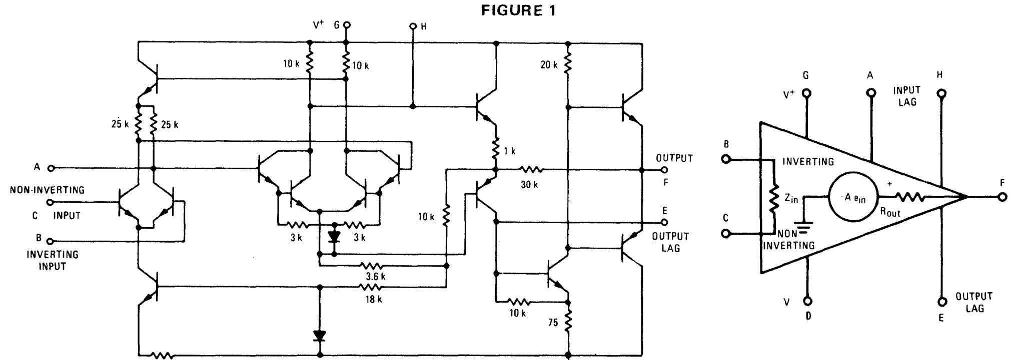
MAXIMUM RATINGS (T_A = +25^{o}C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25^{o}C		4.6	mW/^{o}C
Flat Package		500	mW
Derate above T_A = +25^{o}C		3.3	mW/^{o}C
Plastic Dual In-Line Packages		625	mW
Derate above T_A = +25^{o}C		5.0	mW/^{o}C
Ceramic Dual In-Line Package		750	mW
Derate above T_A = +25^{o}C		6.0	mW/^{o}C
Operating Temperature Range MC1709 MC1709C	T_A	-55 to +125 0 to +75	^{o}C
Storage Temperature Range	T_{stg}		^{o}C
Metal and Ceramic Packages		-65 to +150	
Plastic Packages		-55 to +125	

PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" & "P1" Packages	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	9
"P2" & "L" Packages	3	4	5	6	9	10	11	12

FIGURE 1



CIRCUIT SCHEMATIC **EQUIVALENT CIRCUIT**

See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1709 Min	MC1709 Typ	MC1709 Max	MC1709C Min	MC1709C Typ	MC1709C Max	Unit
Open Loop Voltage Gain (R_L = 2.0 kΩ) (V_O = ±10 V, T_A = T_{low} to T_{high}) ②	A_{VOL}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	Z_{out}	–	150	–	–	150	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	150	400	–	50	250	–	kΩ
Output Voltage Swing (R_L = 10 kΩ) (R_L = 2.0 kΩ)	V_O	 ±12 ±10	 ±14 ±13	 – –	 ±12 ±10	 ±14 ±13	 – –	V_{peak}
Input Common-Mode Voltage Swing	CMV_{in}	±8	±10	–	±8.0	±10	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	70	90	–	65	90	–	dB
Input Bias Current (T_A = +25°C) (T_A = T_{low})	I_b	 – –	 0.2 0.5	 0.5 1.5	 – –	 0.3 –	 1.5 2.0	μA
Input Offset Current (T_A = +25°C) (T_A = T_{low}) (T_A = T_{high})	$\|I_{io}\|$	 – – –	 0.05 – –	 0.2 0.5 0.2	 – – –	 0.1 – –	 0.5 0.75 0.75	μA
Input Offset Voltage (T_A = +25°C) (T_A = T_{low} to T_{high})	$\|V_{io}\|$	 – –	 1.0 –	 5.0 6.0	 – –	 2.0 –	 7.5 10	mV
Step Response Gain = 100, 5.0% overshoot, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF	 t_f t_{pd} dV_{out}/dt ①	 – – –	 0.8 0.38 12	 – – –	 – – –	 0.8 0.38 12	 – – –	 μs μs V/μs
Gain = 10, 10% overshoot, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF	t_f t_{pd} dV_{out}/dt ①	– – –	0.6 0.34 1.7	– – –	– – –	0.6 0.34 1.7	– – –	μs μs V/μs
Gain = 1, 5.0% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_f t_{pd} dV_{out}/dt ①	– – –	2.2 1.3 0.25	– – –	– – –	2.2 1.3 0.25	– – –	μs μs V/μs
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low} to T_{high}) (R_S ≤ 10 kΩ, T_A = T_{low} to T_{high})	$\|TC_{Vio}\|$	 – –	 3.0 6.0	 – –	 – –	 3.0 6.0	 – –	μV/°C
DC Power Dissipation (Power Supply = ±15 V, V_O = 0)	P_D	–	80	165	–	80	200	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	25	150	–	25	200	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	25	150	–	25	200	μV/V

① dV_{out}/dt = Slew Rate

② T_{high} = +75°C for MC1709C, +125°C for MC1709; T_{low} = 0°C for MC1709C, −55°C for MC1709

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT
V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C

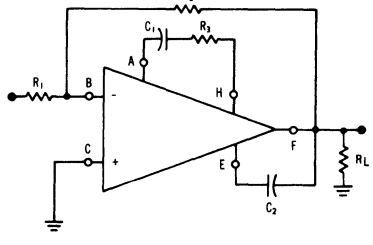


Fig. No.	Curve No.	Test Conditions R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (pF)	C_2 (pF)
3	1	10 k	10 k	1.5 k	5.0 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1.0 M	1.5 k	100	3.0
	4	1.0 k	1.0 M	0	10	3.0
4	1	1.0 k	1.0 M	0	10	3.0
	2	10 k	1.0 M	1.5 k	100	3.0
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5.0 k	200
5	1	0	∞	1.5 k	5.0 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3.0
	4	0	∞	0	10	3.0

TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY

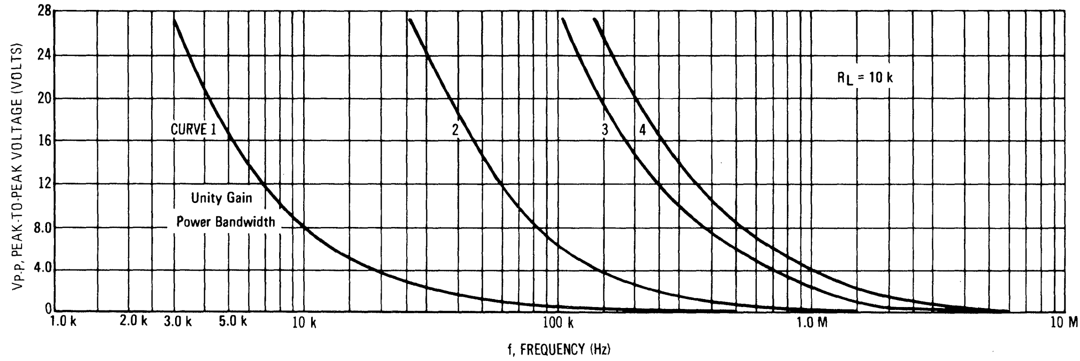


FIGURE 4 – VOLTAGE GAIN versus FREQUENCY

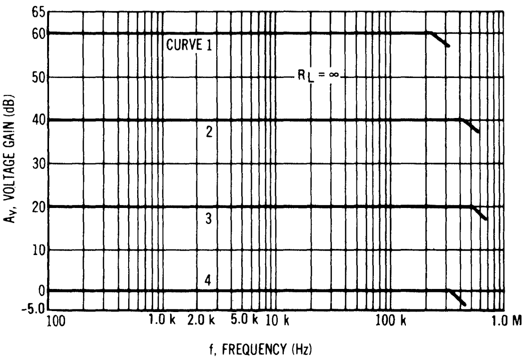


FIGURE 5 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

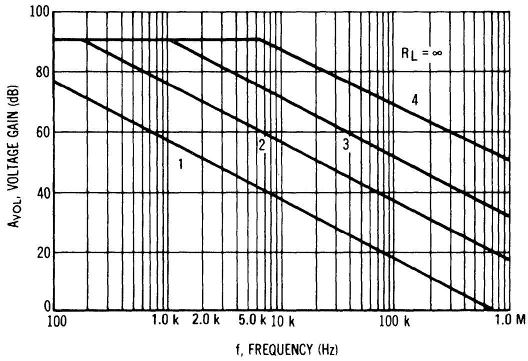


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

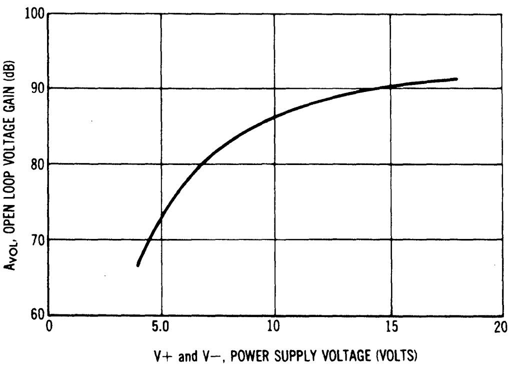
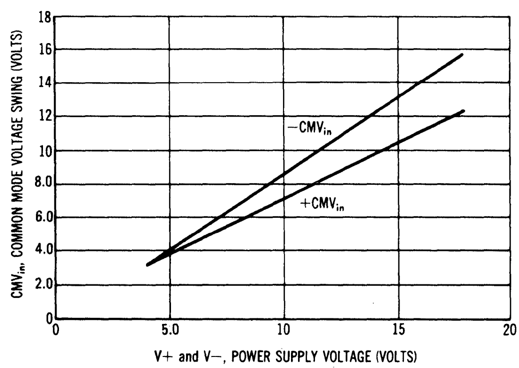


FIGURE 7 – COMMON SWING versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

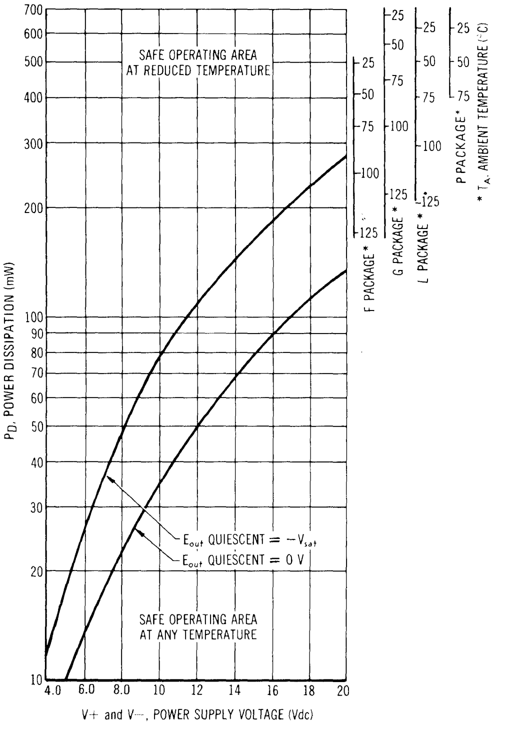


FIGURE 9 – INPUT OFFSET VOLTAGE versus TEMPERATURE

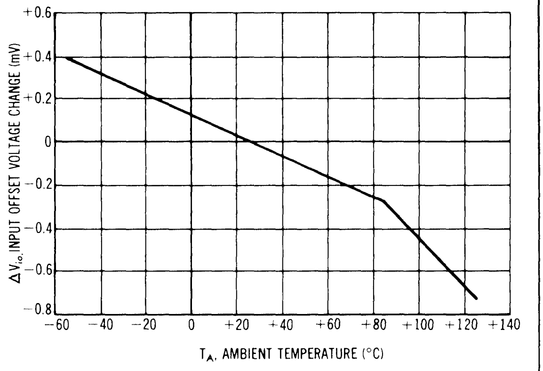
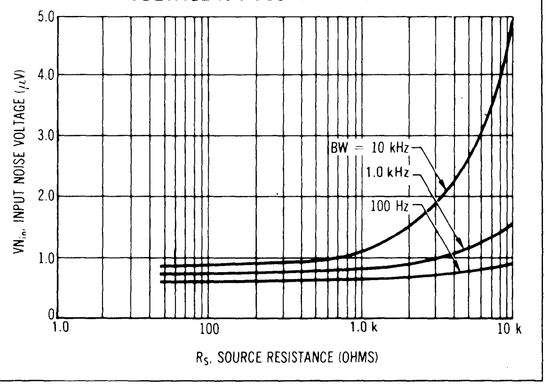


FIGURE 10 – INPUT NOISE VOLTAGE versus SOURCE RESISTANCE



See current MCC1709/1709C data sheet for standard linear chip information.
See current MCBC1709/MCB1709F data sheet for Beam-Lead device information.
See current MCCF1709, 1709C data sheet for flip-chip information.

MC1710

DIFFERENTIAL COMPARATOR

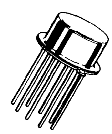
MONOLITHIC DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

- Differential Input Characteristics –
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 3.0 μV/^{o}C
- Fast Response Time – 40 ns
- Output Compatible With All Saturating Logic Forms –
  V_O = +3.2 V to -0.5 V typical
- Low Output Impedance – 200 ohms

DIFFERENTIAL COMPARATOR INTEGRATED CIRCUIT

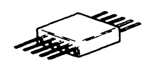
MONOLITHIC SILICON EPITAXIAL PASSIVATED

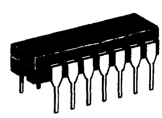


G SUFFIX
METAL PACKAGE
CASE 601

Lead 4 connected to case

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91





L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

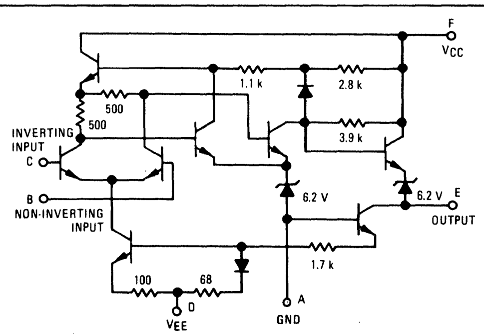
PIN CONNECTIONS

Schematic	A	B	C	D	E	F
"G" Package	1	2	3	4	7	8
"F" Package	1	2	3	5	6	8
"L" Package	2	3	4	6	9	11

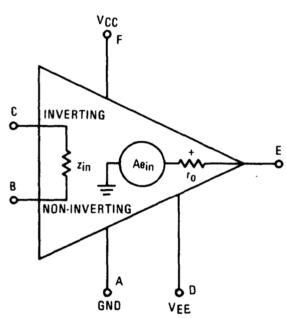
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} max V_{EE} max	+14 -7.0	Vdc Vdc
Differential Input Signal Voltage	V_{ID}	±5.0	Volts
Common Mode Input Swing Voltage	V_{ICR}	±7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (package limitations) Metal Package Derate above T_A = +25°C Flat Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 500 3.3 625 5.0	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC

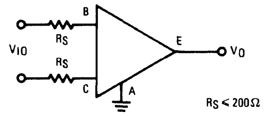
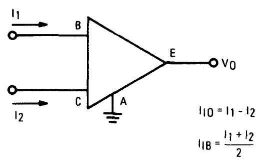
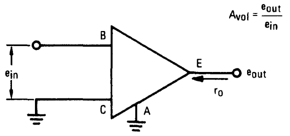
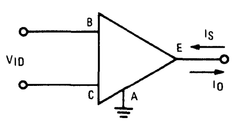
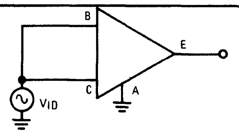
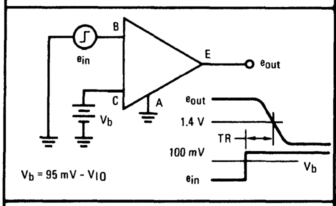
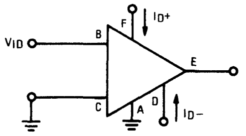


EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.
See current MCC1710/1710C data sheet for standard linear chip information.
See current MCBC1710/MCB1710F for beam-lead device information

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc V_{EE} = -6 Vdc. T_A = +25°C unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage V_O = 1.4 Vdc, T_A = +25°C V_O = 1.8 Vdc, T_A = -55°C V_O = 1.0 Vdc, T_A = +125°C	V_{IO}	 – – –	 1.0 – –	 2.0 3.0 3.0	mVdc
	Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	3.0	–	µV/°C
	Input Offset Current V_O = 1.4 Vdc, T_A = +25°C V_O = 1.8 Vdc, T_A = -55°C V_O = 1.0 Vdc, T_A = +125°C	I_{IO}	 – – –	 1.0 – –	 3.0 7.0 3.0	µAdc
	Input Bias Current V_O = 1.4 Vdc, T_A = +25°C V_O = 1.8 Vdc, T_A = -55°C V_O = 1.0 Vdc, T_A = +125°C	I_{IB}	 – – –	 12 – –	 20 45 20	µAdc
	Open Loop Voltage Gain T_A = +25°C T_A = -55 to +125°C	A_{vol}	 1250 1000	 1700 –	 – –	V/V
	Output Resistance	r_o	–	200	–	ohms
	Differential Voltage Range	V_{ID}	±5.0	–	–	Vdc
	Positive Output Voltage $V_{ID} \geqslant$ 5.0 mV, $0 \leqslant I_O \leqslant$ 5.0 mA	V_{OH}	2.5	3.2	4.0	Vdc
	Negative Output Voltage $V_{ID} \geqslant$ -5.0 mV	V_{OL}	-1.0	-0.5	0	Vdc
	Output Sink Current $V_{ID} \geqslant$ -5.0 mV, $V_O \leqslant 0$, T_A = +25°C $V_{ID} \geqslant$ -5.0 mV, $V_O \geqslant 0$, T_A = -55°C	I_{Os}	 2.0 1.0	 2.5 2.0	 – –	mAdc
	Input Common-Mode Voltage Range	V_{ICR}	±5.0	–	–	Volts
	Common-Mode Rejection Ratio V_{EE} = -7.0 Vdc, $R_S \leqslant 200\Omega$	CMRR	80	100	–	dB
	Propagation Delay Time For Positive and Negative Going Input Pulse	t_p	–	40	–	ns
	Power Supply Current $V_O \leqslant$ 0 Vdc	I_{D^+} I_{D^-}	– –	6.4 5.5	9.0 7.0	mAdc
	Power Consumption		–	115	150	mW

8

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

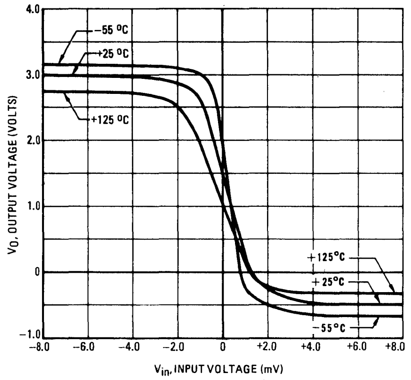


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

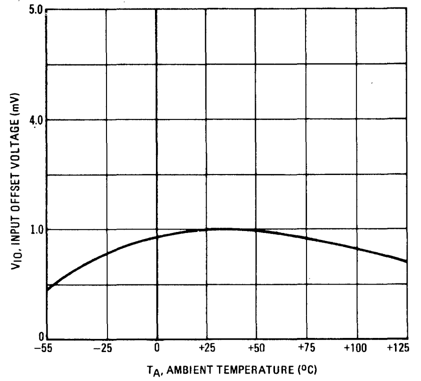


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

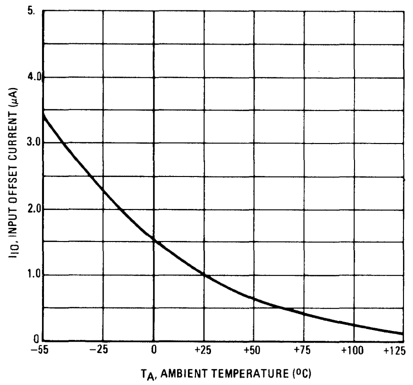


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

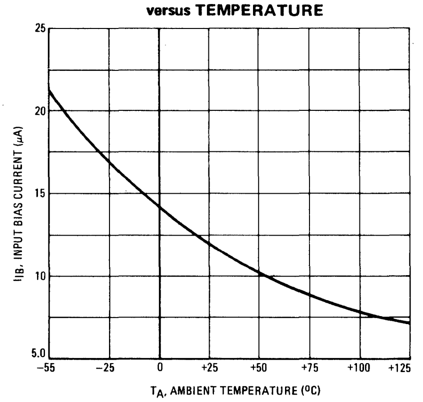


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

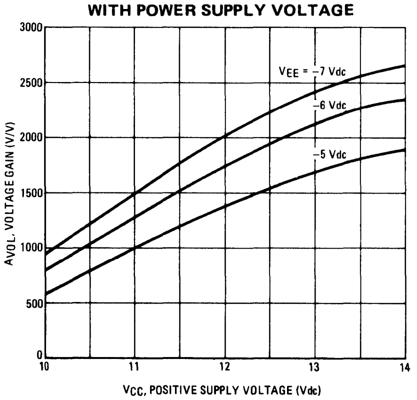
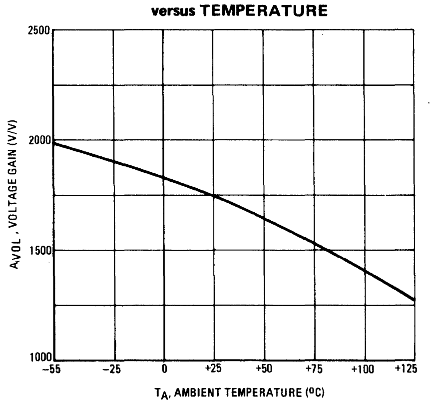


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE



8

TYPICAL CHARACTERISTICS (Continued)

FIGURE 7 – RESPONSE TIME

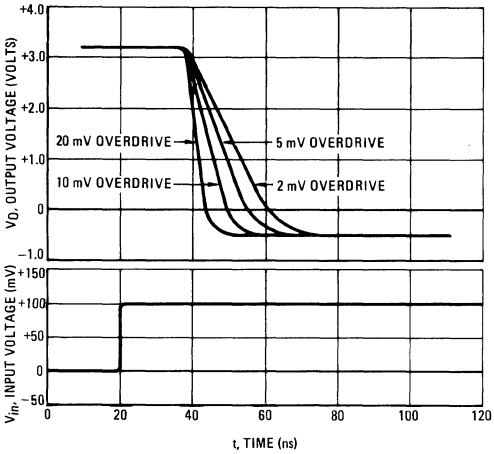


FIGURE 8 – POWER DISSIPATION versus TEMPERATURE

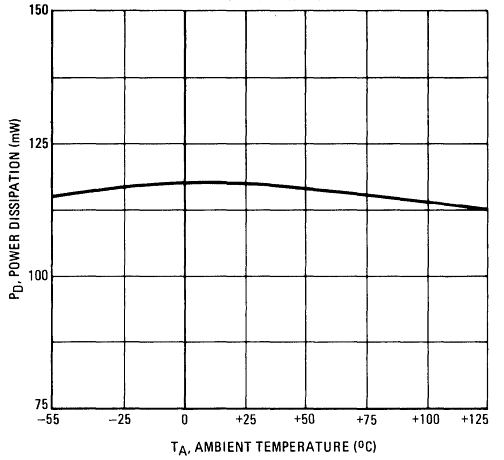


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL* LOADS

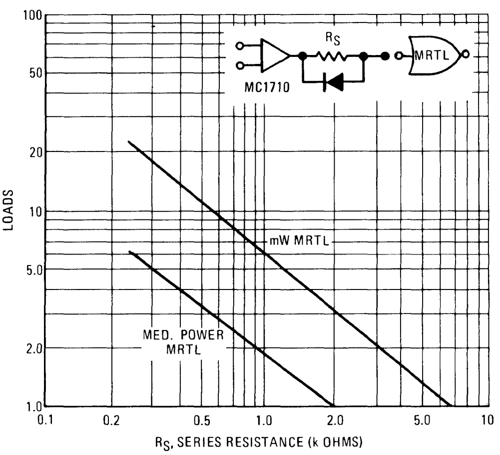
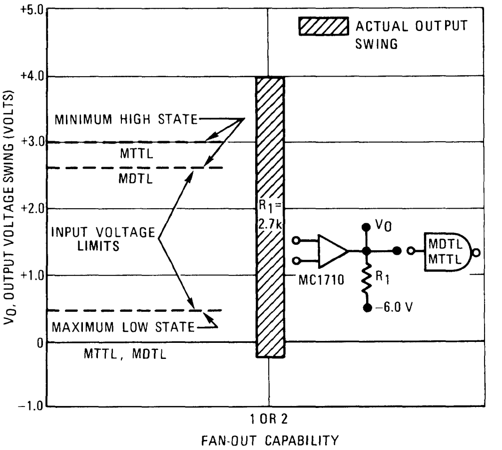


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL* OR MTTL* OUTPUT SWING



MC1710C

DIFFERENTIAL COMPARATOR

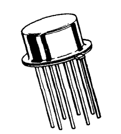
MONOLITHIC DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

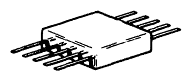
- Differential Input Characteristics –
  Input Offset Voltage = 1.5 mV
  Offset Voltage Drift = 5.0 μV/^{o}C
- Fast Response Time – 40 ns
- Output Compatible With All Saturating Logic Forms –
  V_O = +3.2 V to -0.5 V typical
- Low Output Impedance – 200 ohms

DIFFERENTIAL COMPARATOR

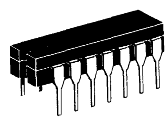
MONOLITHIC
SILICON EPITAXIAL PASSIVATED



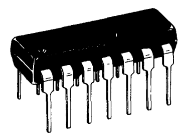
G SUFFIX
METAL PACKAGE
CASE 601



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (T_A = +25^{o}C unless otherwise noted)

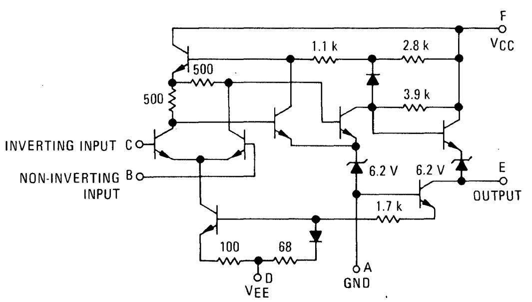
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+14 -7.0	Vdc Vdc
Differential-Mode Input Signal Voltage	V_{ID}	$\pm$5.0	Volts
Common-Mode Input Swing	V_{ICR}	$\pm$7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (package limitations) Metal Package Derate above T_A = +25^{o}C Flat Package Derate above T_A = +25^{o}C Ceramic and Plastic Dual In-Line Packages Derate above T_A = +25^{o}C	P_D	 680 4.6 500 3.3 625 5.0	 mW mW/^{o}C mW mW/^{o}C mW mW/^{o}C
Operating Temperature Range*	T_A	0 to +75	^{o}C
Storage Temperature Range	T_{stg}	-65 to +150	^{o}C

*For fuel temperature range (-55^{o}C to +125^{o}C) and characteristic curves, see MC1710 data sheet.

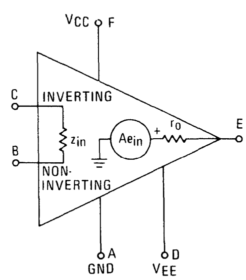
PIN CONNECTIONS

Schematic	A	B	C	D	E	F
"G" Package	1	2	3	4	7	8
"F" Package	1	2	3	5	6	8
"L" and "P" Packages	2	3	4	6	9	11

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT

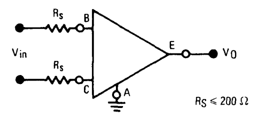
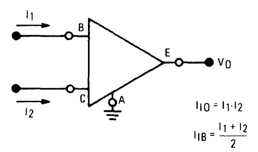
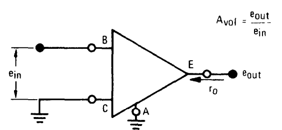
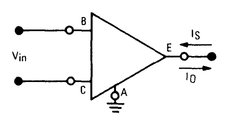
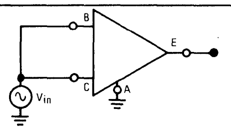
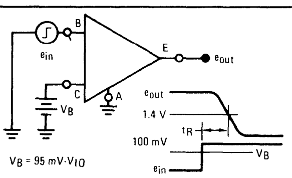
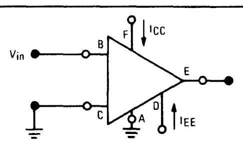


See Packaging Information Section for outline dimensions.
See current MCC1710/1710C data sheet for standard linear chip information.

8

MC1710C (continued)

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage V_O = 1.4 Vdc, T_A = +25°C V_O = 1.5 Vdc, T_A = 0°C V_O = 1.2 Vdc, T_A = +70°C	V_{IO}	 – – –	 1.5 – –	 5.0 6.5 6.5	mVdc
	Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	5.0	–	µV/°C
	Input Offset Current V_O = 1.4 Vdc, T_A = +25°C V_O = 1.5 Vdc, T_A = 0°C V_O = 1.2 Vdc, T_A = +70°C	I_{IO}	 – – –	 1.0 – –	 5.0 7.5 7.5	µAdc
	Input Bias Current V_O = 1.4 Vdc, T_A = +25°C V_O = 1.5 Vdc, T_A = 0°C V_O = 1.2 Vdc, T_A = +70°C	I_{IB}	 – – –	 15 25 –	 25 40 40	µAdc
	Voltage Gain T_A = +25°C T_A = 0 to +70°C	A_{vol}	 1000 800	 1500 –	 – –	V/V
	Output Resistance	r_o	–	200	–	ohms
	Differential-Mode Voltage Range	V_{IDR}	±5.0	–	–	Vdc
	Positive Output Voltage $V_{in} \geqslant$ 5.0 mV, $0 \leqslant I_O \leqslant$ 5.0 mA	V_{OH}	 2.5	 3.2	 4.0	Vdc
	Negative Output Voltage $V_{in} \geqslant$ -5.0 mV	V_{OL}	 -1.0	 -0.5	 0	Vdc
	Output Sink Current $V_{in} \geqslant$ 5.0 mV, $V_O \geqslant 0$ T_A = +25°C T_A = 0°C	I_s	 1.6 0.5	 2.5 –	 – –	mAdc
	Input Common-Mode Range V_{EE} = -7.0 Vdc	V_{ICR}	 ±5.0	 –	 –	Volts
	Common-Mode Rejection Ratio $R_S \leqslant$ 200 Ω	CMRR	 70	 100	 –	dB
	Propagation Delay Time For Positive and Negative Going Input Pulse	$t_{PHL/LH}$	–	40	–	ns
	Power Supply Current $V_O \leqslant$ 0 Vdc	I_{CC} I_{EE}	– –	6.4 5.5	9.0 7.0	mAdc
	Power Consumption		–	110	150	mW

8

MC1711
MC1711C

DIFFERENTIAL COMPARATORS

DUAL DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

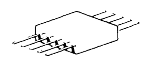
Typical Characteristics:

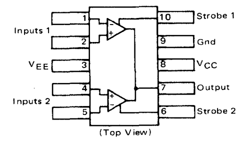
- Differential Input
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 5.0 μV/^{o}C
- Fast Response Time – 40 ns
- Output Compatible with All Saturating Logic Forms
  V_O = +4.5 V to -0.5 V typical
- Low Output Impedance – 200 ohms

DUAL DIFFERENTIAL COMPARATOR

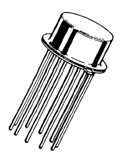
MONOLITHIC SILICON INTEGRATED CIRCUIT

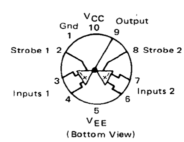
F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

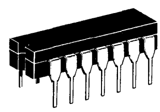




G SUFFIX
METAL PACKAGE
CASE 603-02
TO-100

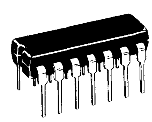


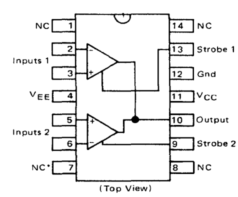




L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1711C only)



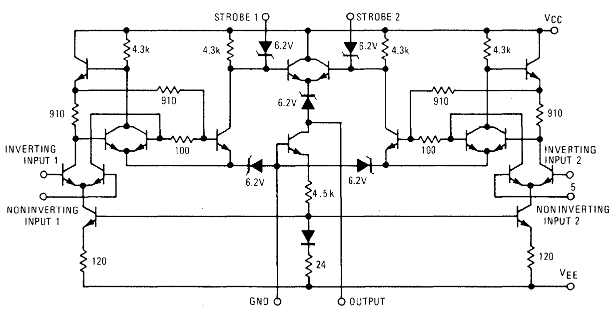


*Connected to pin 4 via the substrate on some plastic units.

MAXIMUM RATINGS (T_A = +25^{o}C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+14 -7.0	Vdc
Differential Input Signal Voltage	V_{IDR}	±5.0	Volts
Common-Mode Input Swing Voltage	V_{ICR}	±7.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (package limitation)	P_D		
Metal Package		680	mW
Derate above T_A = +25^{o}C		4.6	mW/^{o}C
Flat Ceramic Package		500	mW
Derate above T_A = +25^{o}C		3.3	mW/^{o}C
Ceramic and Plastic Dual In-Line Packages		625	mW
Derate above T_A = +25^{o}C		5.0	mW/^{o}C
Operating Temperature Range MC1711 MC1711C	T_A	-55 to +125 0 to +75	^{o}C
Storage Temperature Range	T_{stg}	-65 to +150	^{o}C

CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

8

MC1711, MC1711C (continued)

ELECTRICAL CHARACTERISTICS (each comparator) (V_{CC} = +12 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1711 Min	MC1711 Typ	MC1711 Max	MC1711C Min	MC1711C Typ	MC1711C Max	Unit
Input Offset Voltage	V_{IO}							mVdc
(V_{ICR} = 0 Vdc, T_A = +25°C)		–	1.0	3.5	–	1.0	5.0	
(V_{ICR} ≠ 0 Vdc, T_A = +25°C)		–	1.0	5.0	–	1.0	7.5	
(V_{ICR} = 0 Vdc, T_A = T_{low} to T_{high}*)		–	–	4.5	–	–	6.0	
(V_{ICR} ≠ 0 Vdc, T_A = T_{low} to T_{high})		–	–	6.0	–	–	10	
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	5.0	–	–	5.0	–	μV/°C
Input Offset Current	I_{IO}							μAdc
(V_O = 1.4 Vdc, T_A = +25°C)		–	0.5	10	–	0.5	15	
(V_O = 1.8 Vdc, T_A = -55°C)		–	–	20	–	–	–	
(V_O = 1.5 Vdc, T_A = 0°C)		–	–	–	–	–	25	
(V_O = 1.0 Vdc, T_A = +125°C)		–	–	20	–	–	–	
(V_O = 1.2 Vdc, T_A = +75°C)		–	–	–	–	–	25	
Input Bias Current	I_{IB}							μAdc
(V_O = 1.4 Vdc, T_A = +25°C)		–	25	75	–	25	100	
(V_O = 1.8 Vdc, T_A = -55°C)		–	–	150	–	–	–	
(V_O = 1.5 Vdc, T_A = 0°C)		–	–	–	–	–	150	
(V_O = 1.0 Vdc, T_A = +125°C)		–	–	150	–	–	–	
(V_O = 1.2 Vdc, T_A = +75°C)		–	–	–	–	–	150	
Voltage Gain	A_{vol}							V/V
(T_A = +25°C)		700	1500	–	700	1500	–	
(T_A = T_{low} to T_{high})		500	–	–	500	–	–	
Output Resistance	R_O	–	200	–	–	200	–	ohms
Differential Voltage Range	V_{IDR}	±5.0	–	–	±5.0	–	–	Vdc
High Level Output Voltage ($V_{ID} \geq$ 10 mVdc, 0 ≤ I_O ≤ 5.0 mA)	V_{OH}	2.5	3.2	5.0	2.5	3.2	5.0	Vdc
Low Level Output Voltage ($V_{ID} \geq$ -10 mVdc)	V_{OL}	-1.0	-0.5	0	-1.0	-0.5	0	Vdc
Strobed Output Level (V_{strobe} ≤ 0.3 Vdc)	$V_{OL(st)}$	-1.0	–	0	-1.0	–	0	Vdc
Output Sink Current ($V_{in} \geq$ -10 mV, $V_O \geq$ 0)	I_{Os}	0.5	0.8	–	0.5	0.8	–	mAdc
Strobe Current (V_{strobe} = 100 mVdc)	I_{st}	–	1.2	2.5	–	1.2	2.5	mAdc
Input Common-Mode Range (V_{EE} = -7.0 Vdc)	V_{ICR}	±5.0	–	–	±5.0	–	–	Volts
Response Time (V_b = 5.0 mV + V_{IO})	t_R	–	40	–	–	40	–	ns
Strobe Release Time	t_{SR}	–	12	–	–	12	–	ns
Power Supply Current (V_O ≤ 0 Vdc)	I_{CC}	–	8.6	–	–	8.6	–	mAdc
	I_{EE}	–	3.9	–	–	3.9	–	
Power Consumption		–	130	200	–	130	200	mW

*T_{low} = -55°C for MC1711, 0°C for MC1711C
T_{high} = +125°C for MC1711, +75°C for MC1711C

8

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

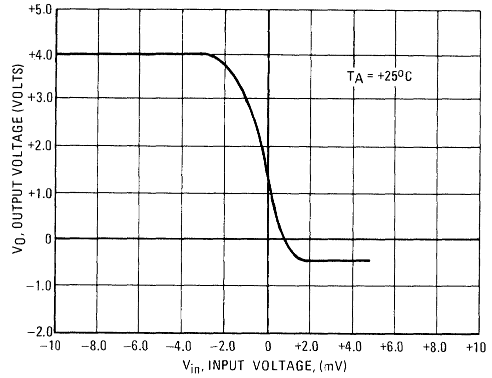


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

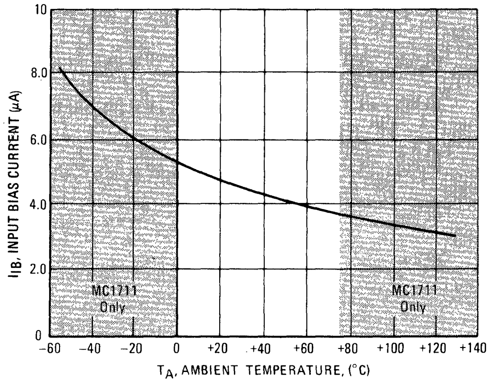


FIGURE 3 – VOLTAGE GAIN versus TEMPERATURE

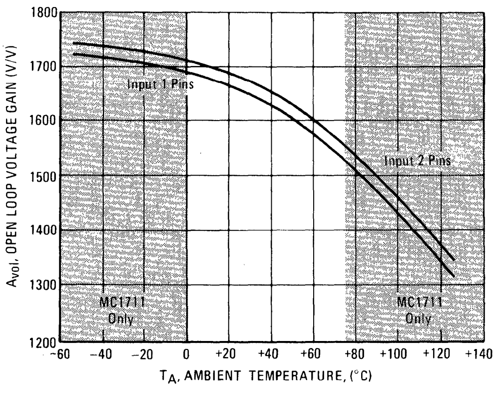


FIGURE 4 – RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

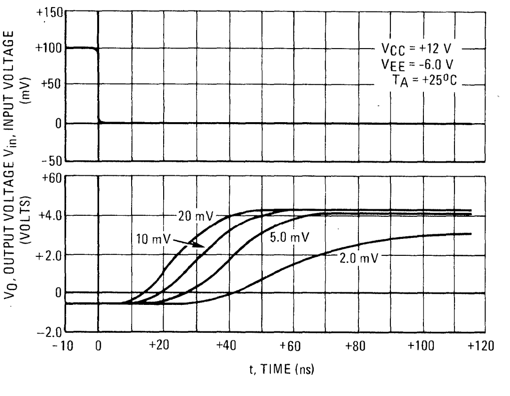


FIGURE 5 – VOLTAGE GAIN VARIATION WITH POWER SUPPLY VOLTAGE

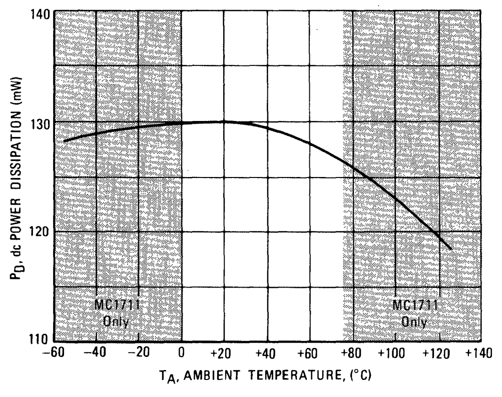
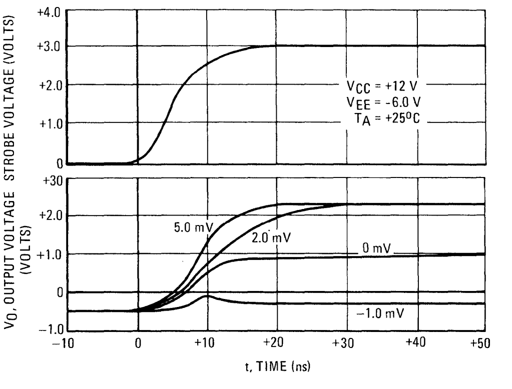


FIGURE 6 – STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



8

FIGURE 7 – COMMON-MODE PULSE RESPONSE

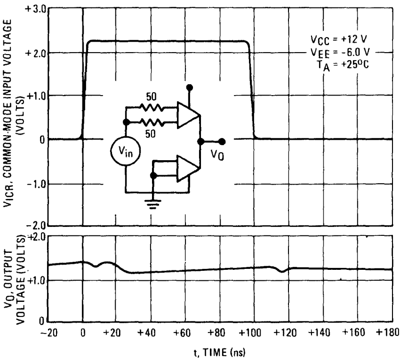


FIGURE 8 – OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

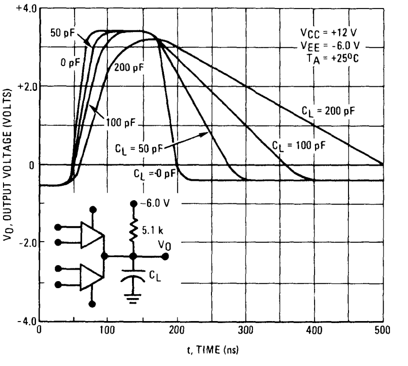


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

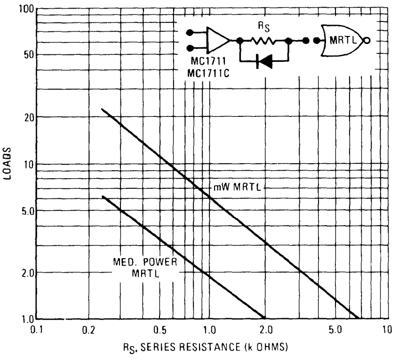
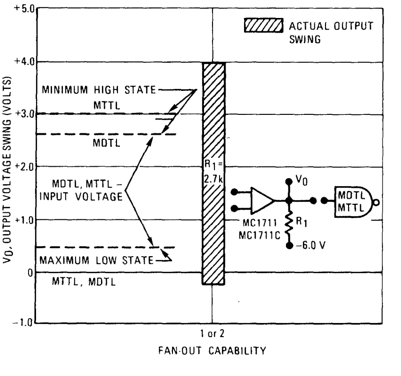


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



8

MC1712
MC1712C

OPERATIONAL AMPLIFIERS

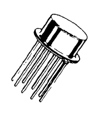
MONOLITHIC WIDEBAND DC AMPLIFIER

. . . designed for use as an operational amplifier utilizing operating characteristics as a function of the external feedback components.

- Open Loop Gain A_{VOL} = 3600 typical
- Low Temperature Drift – ±2.5 μV/°C
- Output Voltage Swing –
  ±5.3 V typical @ +12 V and -6 V Supplies
- Low Output Impedance – Z_{out} = 200 ohms typical

WIDEBAND DC AMPLIFIER INTEGRATED CIRCUIT

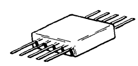
MONOLITHIC SILICON EPITAXIAL PASSIVATED

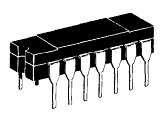


G SUFFIX
METAL PACKAGE
CASE 601

Lead 4 connected to case

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91





L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

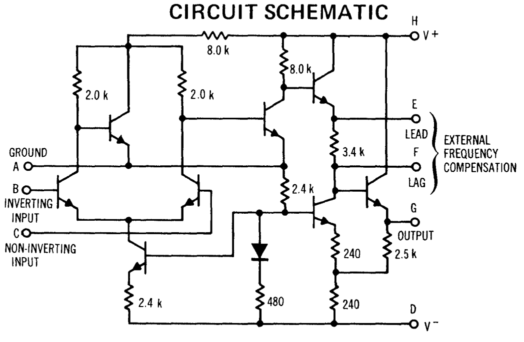
PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" Package	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	10
"L" Package	3	4	5	6	9	10	12	13

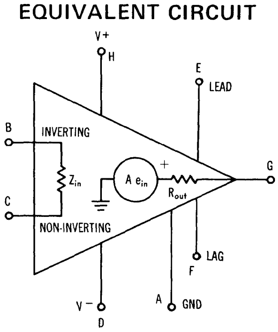
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage (Total between V+ and V- terminals)	$\|V^+\|+\|V^-\|$	21	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	+1.5 -6.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (Package Limitation)	P_D		
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Flat Ceramic Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Dual In-Line Ceramic Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range MC1712 MC1712C	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1712 Min	MC1712 Typ	MC1712 Max	MC1712C Min	MC1712C Typ	MC1712C Max	Unit
Open-Loop Voltage Gain (R_L = 100 kΩ)	A_{VOL}							V/V
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, V_o = ±2.5 V)		600	900	1500	500	800	1500	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, V_o = ±5.0 V)		2500	3600	6000	2000	3400	6000	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, V_o = ±5.0 Vdc, T_A = T_{low}①, T_{high}①)		2000	–	7000	1500	–	7000	
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, V_o = ±2.5 V, T_A = T_{low} to T_{high})		500	–	1750	400	–	1750	
Output Impedance	Z_{out}							ohms
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, f = 20 Hz)		–	300	700	–	300	800	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, f = 20 Hz)		–	200	500	–	200	600	
Input Impedance	Z_{in}							k ohms
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, f = 20 Hz)		22	70	–	16	55	–	
(V^+ = 6.0 Vdc V^- = −3.0 Vdc, f = 20 Hz, T_A = T_{low}, T_{high})		8.0	–	–	10	32	–	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, f = 20 Hz)		16	40	–	–	–	–	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, f = 20 Hz, T_A = T_{low}, T_{high})		6.0	–	–	–	–	–	
Output Voltage Swing	V_o							V_{peak}
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, R_L = 100 kΩ)		±2.5	±2.7	–	±2.5	±2.7	–	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, R_L = 100 kΩ)		±5.0	±5.3	–	±5.0	±5.3	–	
(V^+ = +6.0 Vdc, V^- = −3.0 Vdc, R_L = 10 kΩ)		±1.5	±2.0	–	±1.5	±2.0	–	
(V^+ = +12 Vdc, V^- = −6.0 Vdc, R_L = 10 kΩ)		±3.5	±4.0	–	±3.5	±4.0	–	
Input Common-Mode Voltage Swing	CMV_{in}							V_{peak}
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		+0.5	–	–	+0.5	–	–	
		−1.5	–	–	−1.5	–	–	
(V^+ = 12 Vdc, V^- = −6.0 Vdc)		+0.5	–	–	+0.5	–	–	
		−4.0	–	–	−4.0	–	–	
Common-Mode Rejection Ratio	CM_{rej}							dB
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, f ≤ 1.0 kHz)		80	100	–	70	95	–	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, f ≤ 1.0 kHz)		80	100	–	70	95	–	
Input Bias Current $I_b = \frac{I_1 + I_2}{2}$	I_b							µA
T_A = +25°C								
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		–	1.2	3.5	–	1.5	5.0	
(V^+ = 12 Vdc, V^- = −6.0 Vdc)		–	2.0	5.0	–	2.5	7.5	
T_A = T_{low}								
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		–	2.5	7.5	–	2.5	8.0	
(V^+ = 12 Vdc, V^- = −6.0 Vdc)		–	4.0	10	–	4.0	12	
Input Offset Current ($I_{io} = I_1 - I_2$)	$\|I_{io}\|$							µA
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		–	0.1	0.5	–	0.3	2.0	
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, T_A = T_{low} to T_{high})		–	–	1.5	–	–	2.5	
(V^+ = 12 Vdc, V^- = −6.0 Vdc)		–	0.2	0.5	–	0.5	2.0	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, T_A = T_{low} to T_{high})		–	–	1.5	–	–	2.5	
Input Offset Voltage (R_S = 2.0 kΩ)	$\|V_{io}\|$							mV
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		–	1.3	3.0	–	1.7	6.0	
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, T_A = T_{low}, T_{high})		–	–	4.0	–	–	7.5	
(V^+ = 12 Vdc, V^- = −6.0 Vdc)		–	1.1	2.0	–	1.5	5.0	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, T_A = T_{low}, T_{high})		–	–	3.0	–	–	6.5	
Step Response								
V^+ = 12 Vdc, V^- = −6.0 Vdc	V_{os}	–	20	40	–	20	40	%
Gain = 100, V_{in} = 1.0 mV,	t_f	–	10	30	–	10	30	ns
R_1 = 1.0 kΩ, R_2 = 100 kΩ,	t_{pd}	–	10	–	–	10	–	ns
C_2 = 50 pF, R_3 = ∞, C_1 = open	dV_{out}/dt②	–	12	–	–	12	–	V/µs
V^+ = 12 Vdc, V^- = −6.0 Vdc	V_{os}	–	10	50	–	10	50	%
Gain = 1.0, V_{in} = 10 mV,	t_f	–	25	120	–	25	120	ns
R_1 = 10 kΩ, R_2 = 10 kΩ,	t_{pd}	–	16	–	–	16	–	ns
C_1 = 0.01 µF, R_3 = 20Ω, C_2 = open	dV_{out}/dt②	–	1.5	–	–	1.5	–	V/µs
Average Temperature Coefficient of Input Offset Voltage (R_S = 50Ω)	$\|TC_{Vio}\|$							µV/°C
(T_A = +25°C to T_{high})		–	2.5	–	–	–	–	
(T_A = T_{low} to +25°C)		–	2.0	–	–	–	–	
(T_A = T_{low}, T_{high})		–	–	–	–	5.0	–	
Average Temperature Coefficient Input Offset Current	$\|TC_{Iio}\|$							nA/°C
(T_A = +25°C to T_{high})		–	0.05	–	–	4.0	–	
(T_A = T_{low} to +25°C)		–	1.5	–	–	6.0	–	
DC Power Dissipation	P_D							mW
(V_{out} = 0, V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		–	17	30	–	17	30	
(V_{out} = 0, V^+ = 12 Vdc, V^- = −6.0 Vdc)		–	70	120	–	70	120	
Positive Supply Sensitivity (V^- constant = −6.0 Vdc, V^+ = 12 Vdc to 6.0 Vdc)	S^+	–	60	200	–	60	300	µV/V
Negative Supply Sensitivity (V^+ constant = 12 Vdc, V^- = −6.0 Vdc to −3.0 Vdc)	S^-	–	60	200	–	60	300	µV/V

① T_{low} = 0°C for MC1712C, T_{high} = +75°C for MC1712C
−55°C for MC1712, +125°C for MC1712

② dV_{out}/dt = Slew Rate

8

TYPICAL OUTPUT CHARACTERISTICS

(V^+ = 12 Vdc, V^- = −6.0 Vdc, T_A = +25°C)

FIGURE 1 – OPEN LOOP GAIN versus POWER SUPPLY VARIATIONS

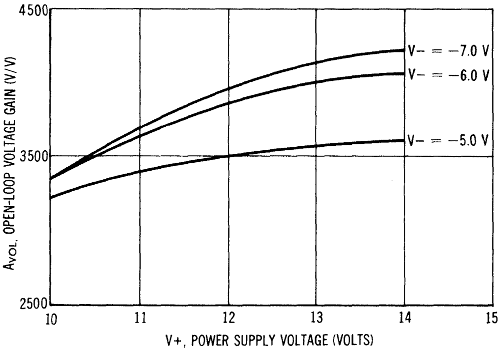


FIGURE 2 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

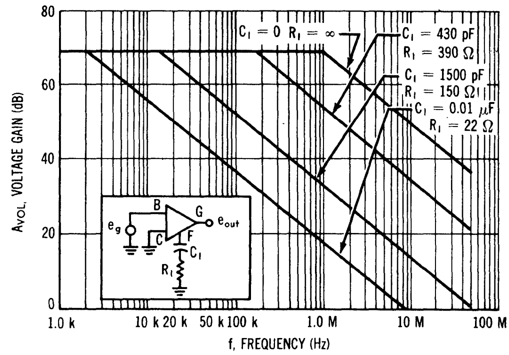


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

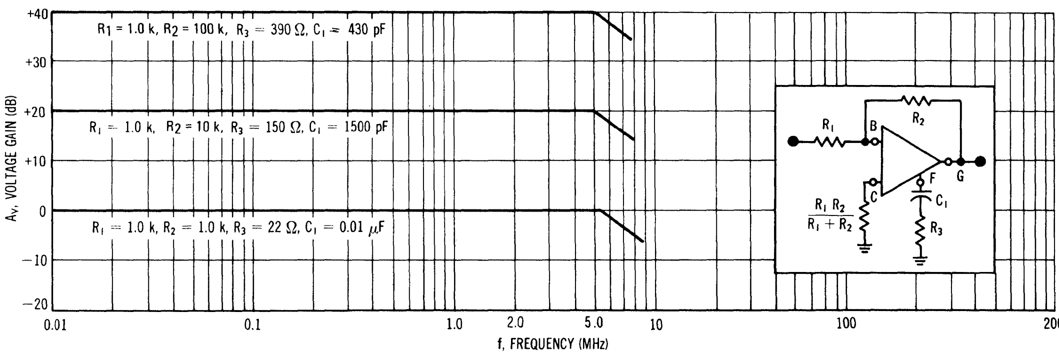


FIGURE 4 – MAXIMUM OUTPUT SWING versus FREQUENCY

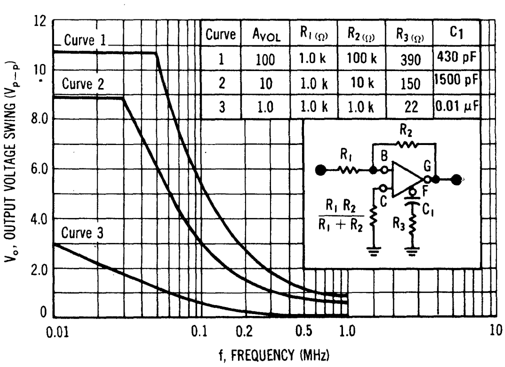
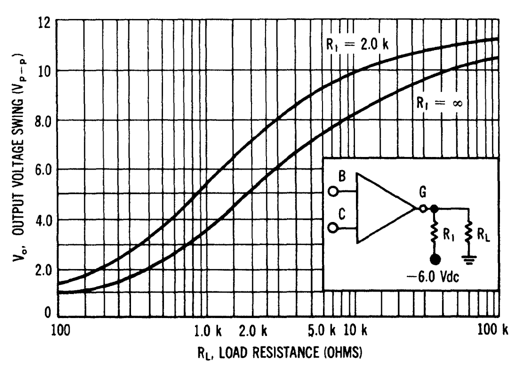


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



8

TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – INPUT BIAS CURRENT versus TEMPERATURE

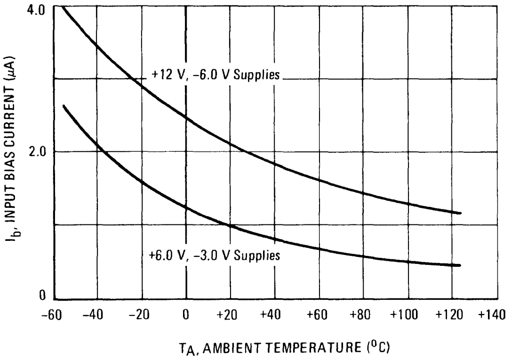


FIGURE 7 – INPUT OFFSET CURRENT versus TEMPERATURE

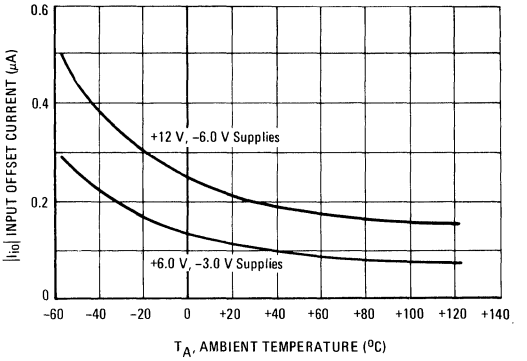


FIGURE 8 – INPUT OFFSET VOLTAGE versus TEMPERATURE

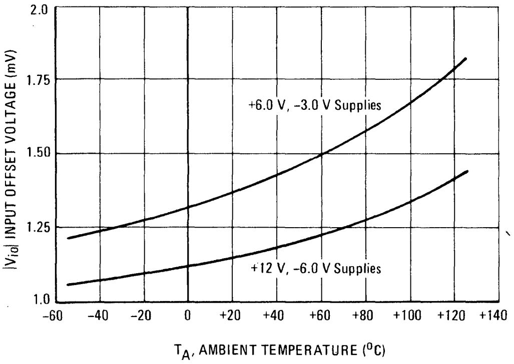
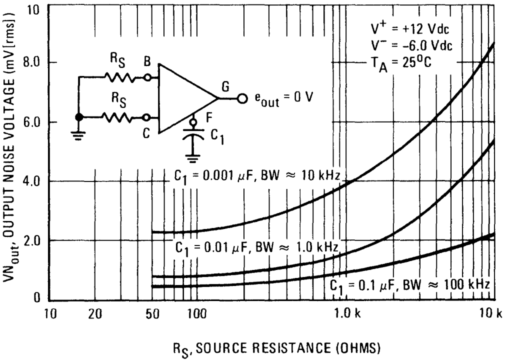


FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



8

POSITIVE VOLTAGE REGULATORS

MC1723
MC1723C

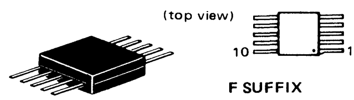
MONOLITHIC VOLTAGE REGULATOR

The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +75°C)

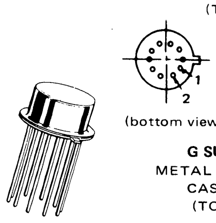
- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

VOLTAGE REGULATOR

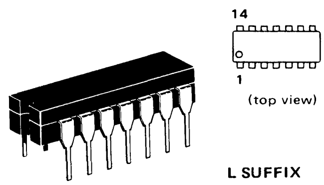
MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT



F SUFFIX
CERAMIC PACKAGE
CASE 606
(TO-91)

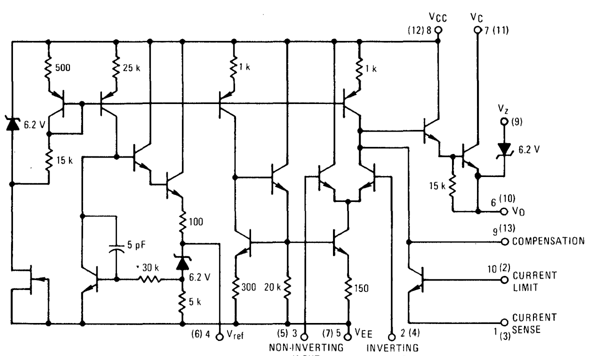


G SUFFIX
METAL PACKAGE
CASE 603
(TO-100)



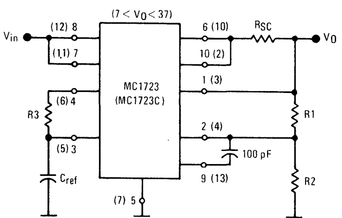
L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

FIGURE 1 – CIRCUIT SCHEMATIC



PIN NUMBERS ADJACENT TO TERMINALS ARE FOR THE METAL AND CERAMIC FLAT PACKAGE; PIN NUMBERS IN PARENTHESIS ARE FOR THE CERAMIC DUAL IN-LINE PACKAGE.

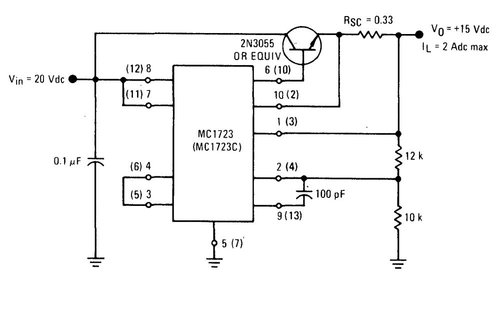
FIGURE 2 – TYPICAL CIRCUIT CONNECTION



$V_O \cong 7\left(\frac{R1 + R2}{R2}\right)$ $\quad I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at $T_J = +25°C$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1||R2

FIGURE 3 – TYPICAL NPN CURRENT BOOST CONNECTION



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Pulse Voltage from V_{CC} to V_{EE} (50 ms)	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V_{CC} to V_{EE}	V_{in}	40	Vdc
Input-Output Voltage Differential	$V_{in} - V_O$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Current from V_z	I_z	25	mA
Power Dissipation and Thermal Characteristics			
Flat Ceramic Package			
T_A = +25°C	P_D	500	mW
Derate above T_A = +25°C	$1/\theta_{JA}$	3.3	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	300	°C/W
Metal Package			
T_A = +25°C	P_D	0.8	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	5.4	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	184	°C/W
T_C = +25°C	P_D	2.1	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	14	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	70	°C/W
Dual In-Line Ceramic Package	P_D	1.0	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	6.7	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}		°C
Metal Package		-65 to +150	
Dual In-Line Ceramic and Ceramic Flat Packages		-65 to +175	
Operating Ambient Temperature Range	T_A		°C
MC1723C		0 to +75	
MC1723		-55 to +125	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 1)

Characteristic	Symbol	MC1723 Min	MC1723 Typ	MC1723 Max	MC1723C Min	MC1723C Typ	MC1723C Max	Unit
Input Voltage Range	V_{in}	9.5	–	40	9.5	–	40	Vdc
Output Voltage Range	V_O	2.0	–	37	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_O$	3.0	–	38	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{IB}	–	2.3	3.5	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_N							µV(RMS)
C_{ref} = 0		–	20	–	–	20	–	
C_{ref} = 5.0 µF		–	2.5	–	–	2.5	–	
Average Temperature Coefficient of Output Voltage (T_{low} ① < T_A < T_{high} ②)	TCV_O	–	0.002	0.015	–	0.003	0.015	%/°C
Line Regulation	Reg_{in}							$\%V_O$
(T_A = +25°C) 12 V < V_{in} < 15 V		–	0.01	0.1	–	0.01	0.1	
(T_A = +25°C) 12 V ≤ V_{in} < 40 V		–	0.02	0.2	–	0.1	0.5	
(T_{low} ① < T_A < T_{high} ②) 12 V < V_{in} < 15 V		–	–	0.3	–	–	0.3	
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_{load}							$\%V_O$
T_A = +25°C		–	0.03	0.15	–	0.03	0.2	
T_{low} ① < T_A < T_{high} ②		–	–	0.6	–	–	0.6	
Ripple Rejection (f = 50 Hz to 10 kHz)	Rej_R							dB
C_{ref} = 0		–	74	–	–	74	–	
C_{ref} = 5.0 µF		–	86	–	–	86	–	
Short Circuit Current Limit (R_{SC} = 10 Ω, V_O = 0)	I_{SC}	–	65	–	–	65	–	mAdc
Long Term Stability	$\Delta V_O/\Delta t$	–	0.1	–	–	0.1	–	%/1000 Hr

① T_{low} = 0°C for MC1723C
= -55°C for MC1723

② T_{high} = +75°C for MC1723C
= +125°C for MC1723

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TYPICAL CHARACTERISTICS

(V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

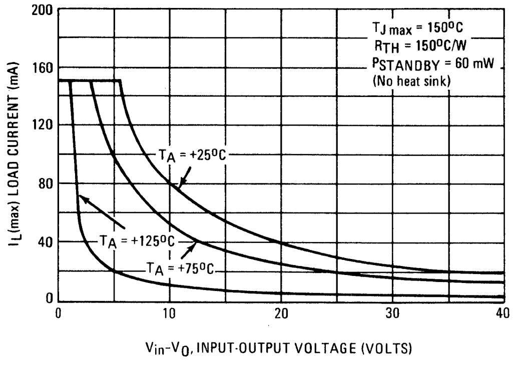


FIGURE 5 – LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

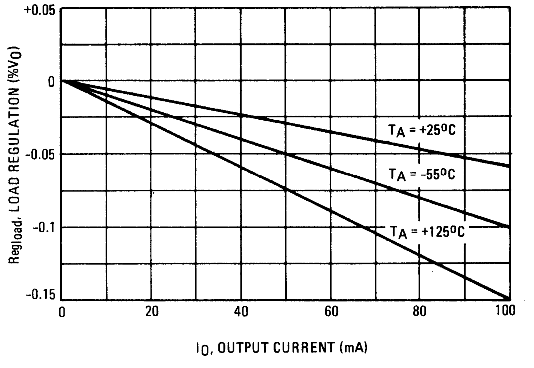


FIGURE 6 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

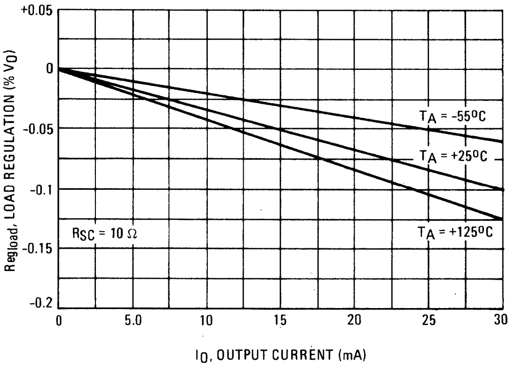


FIGURE 7 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

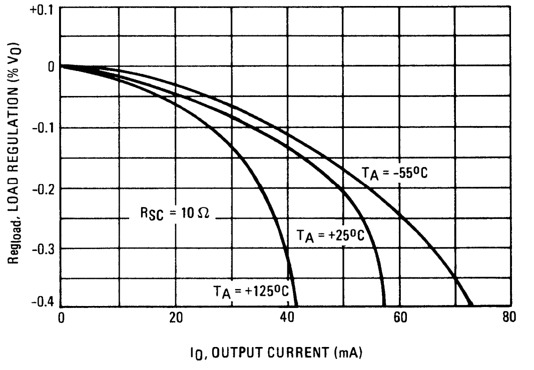


FIGURE 8 – CURRENT LIMITING CHARACTERISTICS

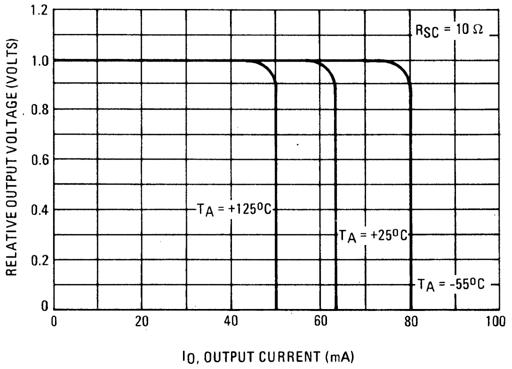
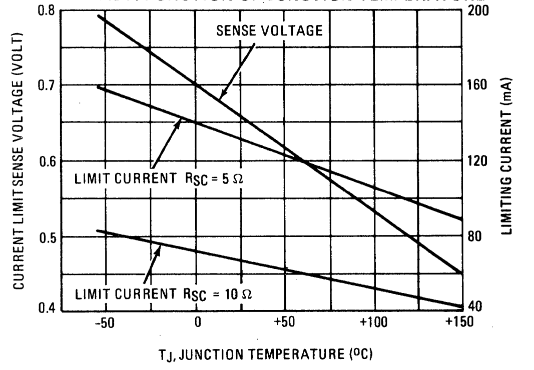


FIGURE 9 – CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

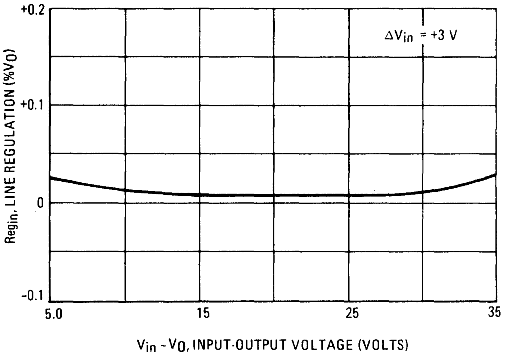


FIGURE 11 – LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

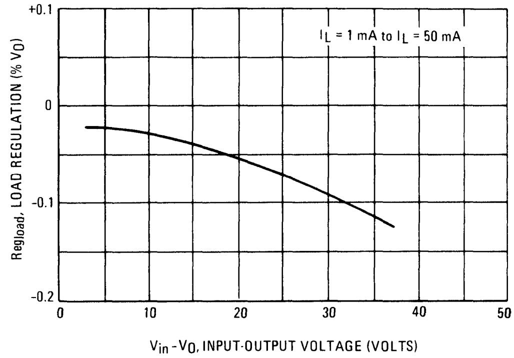


FIGURE 12 – STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

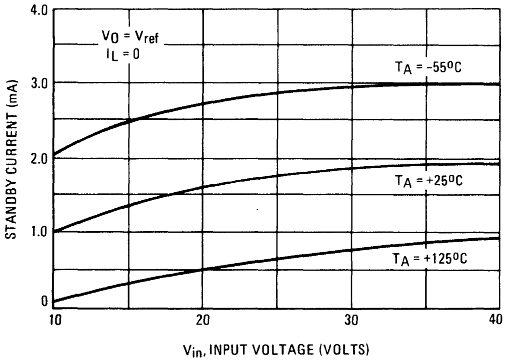


FIGURE 13 – LINE TRANSIENT RESPONSE

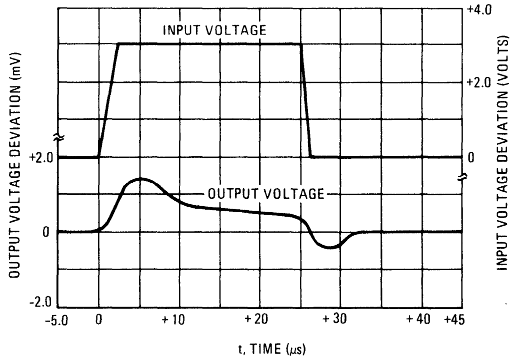


FIGURE 14 – LOAD TRANSIENT RESPONSE

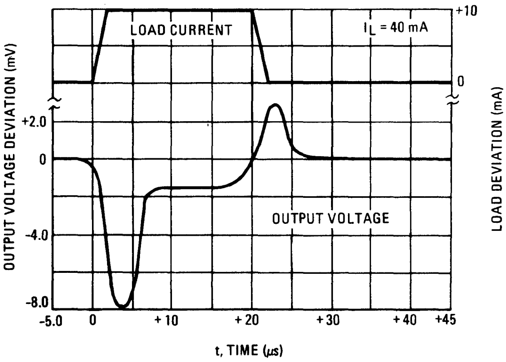
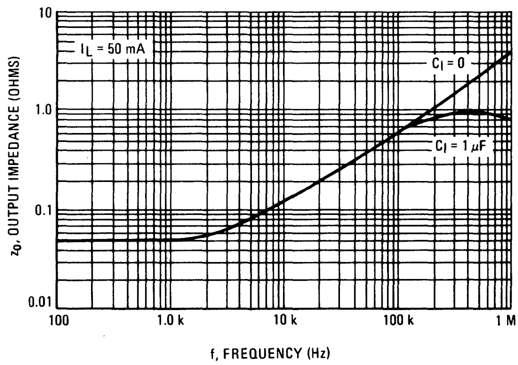


FIGURE 15 – OUTPUT IMPEDANCE AS FUNCTION OF FREQUENCY

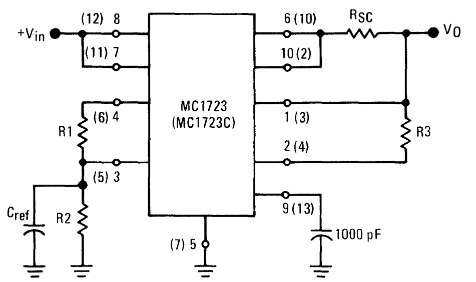


8

TYPICAL APPLICATIONS

Pin numbers adjacent to terminals are for the metal and ceramic flat packages; pin numbers in parenthesis are for the ceramic dual in-line package.

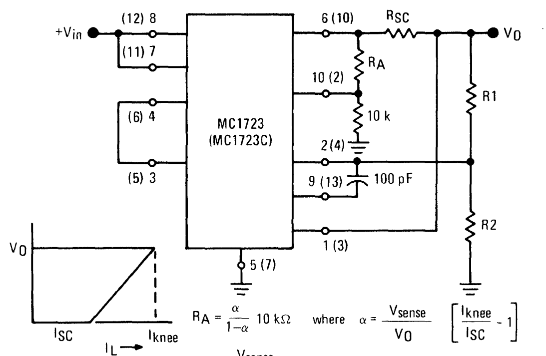
FIGURE 16 – TYPICAL CONNECTION FOR 2 < V_O < 7



$V_O \cong 7\left[\frac{R2}{R1+R2}\right]$ $\quad I_{SC} = \frac{V_{sense}}{R_{SC}} \cong \frac{0.66}{R_{SC}}$ at $T_J = +25^oC$

For best results 10 k < R1 + R2 < 100 k.
For minimum drift R3 = R1||R2.

FIGURE 17 – MC1723,C FOLDBACK CONNECTION



$R_A = \frac{\alpha}{1-\alpha}\ 10\ k\Omega$ where $\alpha = \frac{V_{sense}}{V_O}\left[\frac{I_{knee}}{I_{SC}} - 1\right]$

$R_{SC} = \frac{V_{sense}}{(1-\alpha)\ I_{SC}}$

FIGURE 18 – +5 V, 1-AMPERE SWITCHING REGULATOR

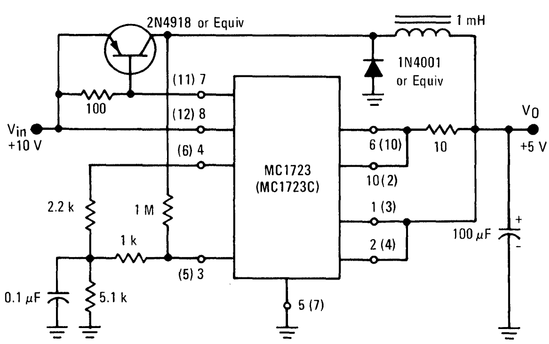


FIGURE 19 – +5 V, 1-AMPERE HIGH EFFICIENCY REGULATOR

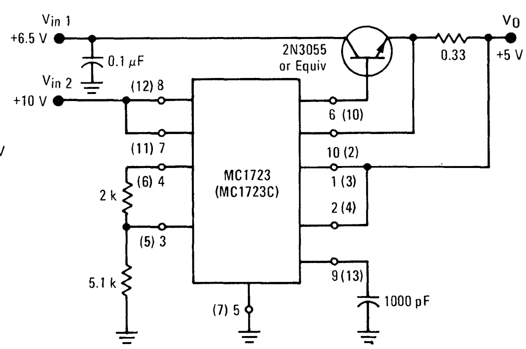


FIGURE 20 – +15 V, 1-AMPERE REGULATOR WITH REMOTE SENSE

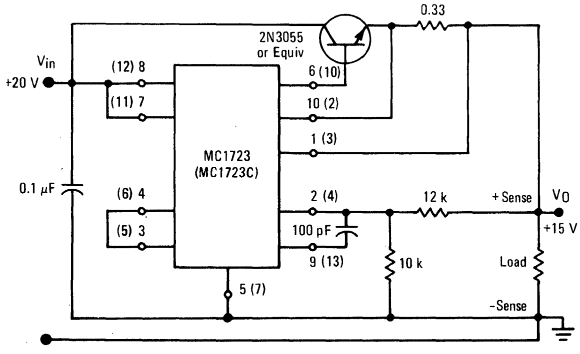
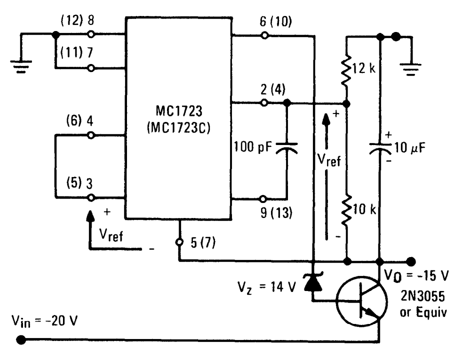


FIGURE 21 – -15 V NEGATIVE REGULATOR



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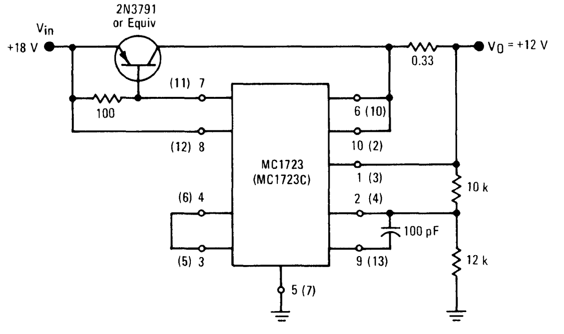
TYPICAL APPLICATIONS (continued)

FIGURE 22 – +12 V, 1-AMPERE REGULATOR USING PNP CURRENT BOOST



Pin numbers adjacent to terminals are for the metal and ceramic flat packages; pin numbers in parenthesis are for the ceramic dual in-line package.

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MC1733
MC1733C

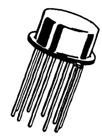
MONOLITHIC DIFFERENTIAL VIDEO AMPLIFIER

. . . a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

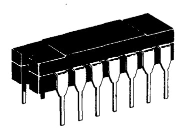
- Bandwidth — 120 MHz typical @ A_{vd} = 10
- Rise Time — 2.5 ns typical @ A_{vd} = 10
- Propagation Delay Time — 3.6 ns typical @ A_{vd} = 10

DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 603
TO-100



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 — BASIC CIRCUIT

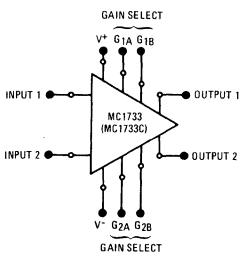


FIGURE 2 — VOLTAGE GAIN ADJUST CIRCUIT

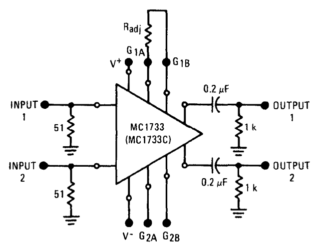
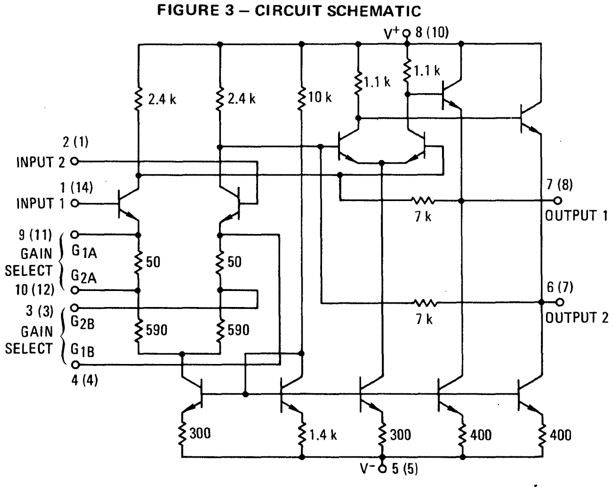
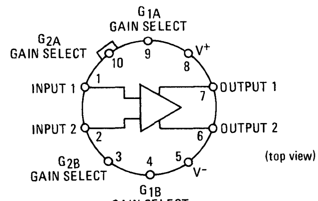


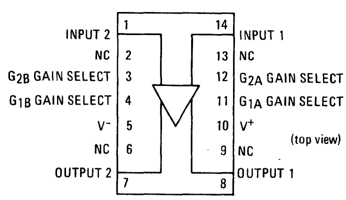
FIGURE 3 — CIRCUIT SCHEMATIC



CONNECTION DIAGRAMS



G SUFFIX, METAL PACKAGE
Pin 5 connected to case.



L SUFFIX, CERAMIC PACKAGE

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+8.0 -8.0	Volts
Differential Input Voltage	V_{in}	±5.0	Volts
Common-Mode Input Voltage	CMV_{in}	±6.0	Volts
Output Current	I_o	10	mA
Internal Power Dissipation (Note 1) Metal Can Package Ceramic Dual In-Line Package	P_D	 500 500	mW
Operating Temperature Range MC1733C MC1733	T_A	0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +6.0 Vdc, V^- = -6.0 Vdc, at T_A = +25°C unless otherwise noted)

		MC1733			MC1733C			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Differential Voltage Gain Gain 1 (Note 2) Gain 2 (Note 3) Gain 3 (Note 4)	A_{vd}	 300 90 9.0	 400 100 10	 500 110 11	 250 80 8.0	 400 100 10	 600 120 12	
Bandwidth ($R_s = 50\,\Omega$) Gain 1 Gain 2 Gain 3	BW	 – – –	 40 90 120	 – – –	 – – –	 40 90 120	 – – –	MHz
Rise Time ($R_s = 50\,\Omega, V_o = 1$ Vp-p) Gain 1 Gain 2 Gain 3	t_r	 – – –	 10.5 4.5 2.5	 – 10 –	 – – –	 10.5 4.5 2.5	 – 12 –	ns
Propagation Delay ($R_s = 50\,\Omega, V_o = 1$ Vp-p) Gain 1 Gain 2 Gain 3	t_{pd}	 – – –	 7.5 6.0 3.6	 – 10 –	 – – –	 7.5 6.0 3.6	 – 10 –	ns
Input Resistance Gain 1 Gain 2 Gain 3	R_{in}	 – 20 –	 4.0 30 250	 – – –	 – 10 –	 4.0 30 250	 – – –	kΩ
Input Capacitance (Gain 2)	C_{in}	–	2.0	–	–	2.0	–	pF
Input Offset Current	$\lvert I_{io}\rvert$	–	0.4	3.0	–	0.4	5.0	µA
Input Bias Current	I_b	–	9.0	20	–	9.0	30	µA
Input Noise Voltage ($R_s = 50\,\Omega$, BW = 1 kHz to 10 MHz)	V_n	–	12	–	–	12	–	µV(rms)
Input Voltage Range	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio Gain 2 ($V_{CM} = \pm 1$ V, f ≤ 100 kHz) Gain 2 ($V_{CM} = \pm 1$ V, f = 5 MHz)	CM_{rej}	 60 –	 86 60	 – –	 60 –	 86 60	 – –	dB
Supply Voltage Rejection Ratio Gain 2 ($\Delta V_s = \pm 0.5$ V)	S^+, S^-	 50	 70	 –	 50	 70	 –	dB
Output Offset Voltage Gain 1 Gain 2 and Gain 3	V_{oo}	 – –	 0.6 0.35	 1.5 1.0	 – –	 0.6 0.35	 1.5 1.5	V
Output Common-Mode Voltage	CMV_O	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	V_O	3.0	4.0	–	3.0	4.0	–	Vp-p
Output Sink Current	I_O	2.5	3.6	–	2.5	3.6	–	mA
Output Resistance	R_{out}	–	20	–	–	20	–	Ω
Power Supply Current	I_D	–	18	24	–	18	24	mA

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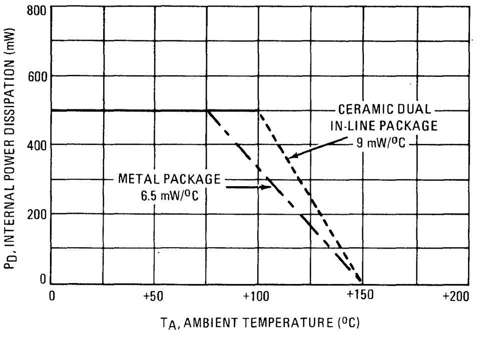
FIGURE 4 – MAXIMUM ALLOWABLE POWER DISSIPATION



NOTES

Note 1: Derate metal package at 6.5 mW/°C for operation at ambient temperatures above 75°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required (MC1733) a heatsink may be necessary to limit maximum junction temperature to 150°C. Thermal resistance, junction-to-case, for the metal package is 69.4°C per Watt.

Note 2: Gain Select pins G_{1A} and G_{1B} connected together.

Note 3: Gain Select pins G_{2A} and G_{2B} connected together.

Note 4: All Gain Select pins open.

TYPICAL CHARACTERISTICS

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

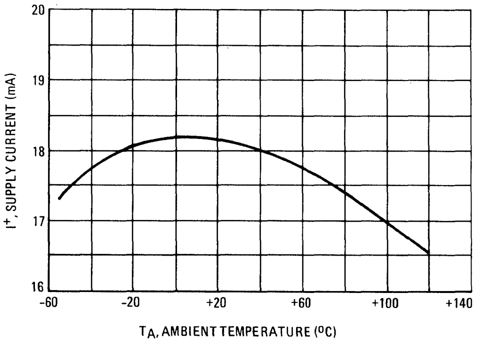
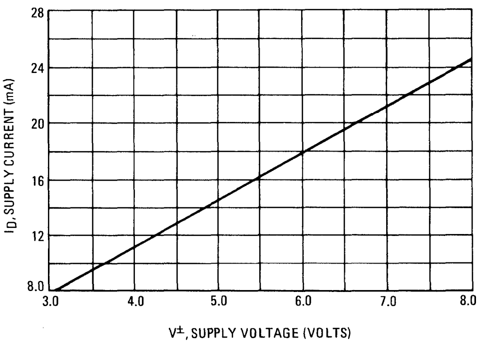


FIGURE 6 – SUPPLY CURRENT versus SUPPLY VOLTAGE



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TYPICAL CHARACTERISTICS (continued)

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 7 – GAIN verus TEMPERATURE

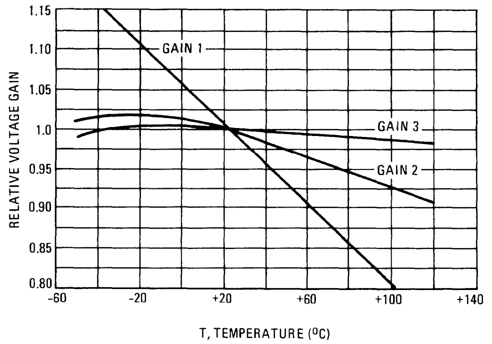


FIGURE 8 – GAIN versus FREQUENCY

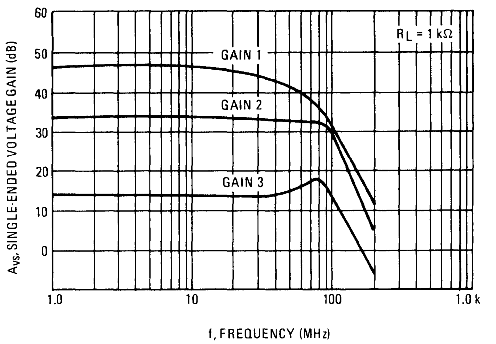


FIGURE 9 – GAIN versus SUPPLY VOLTAGE

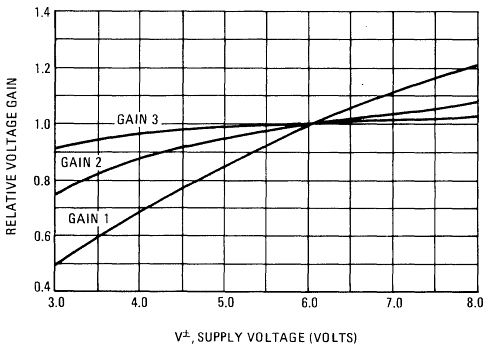


FIGURE 10 – GAIN versus R_{ADJUST}

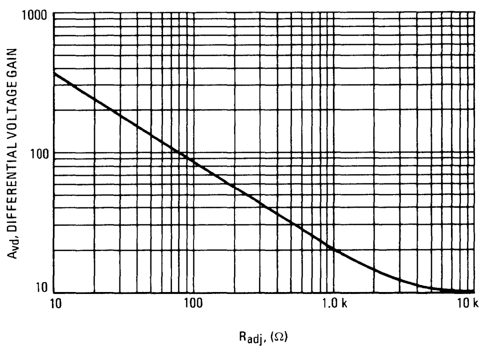


FIGURE 11 – GAIN versus FREQUENCY and SUPPLY VOLTAGE

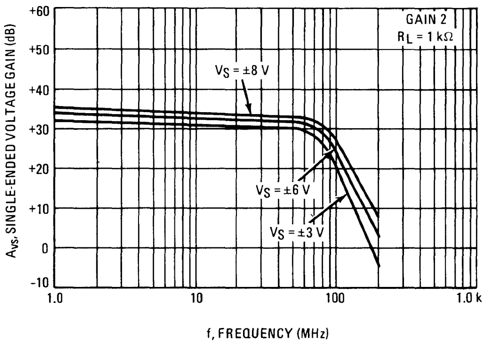
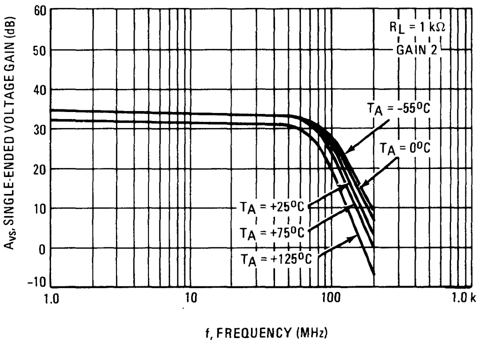


FIGURE 12 – GAIN versus FREQUENCY and TEMPERATURE



8

TYPICAL CHARACTERISTICS (continued)

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 13 – PULSE RESPONSE versus GAIN

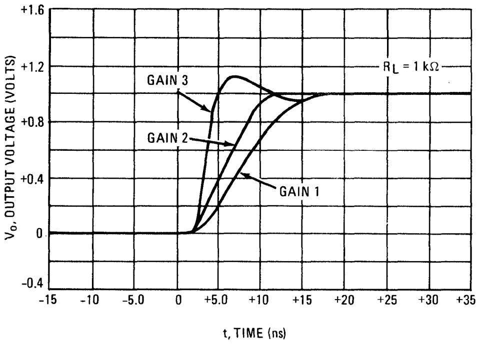


FIGURE 14 – PULSE RESPONSE versus SUPPLY VOLTAGE

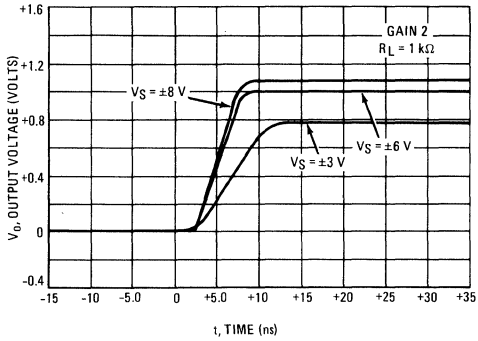


FIGURE 15 – PULSE RESPONSE versus TEMPERATURE

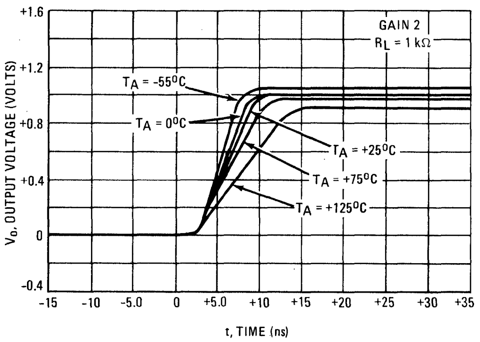


FIGURE 16 – DIFFERENTIAL OVERDRIVE RECOVERY TIME

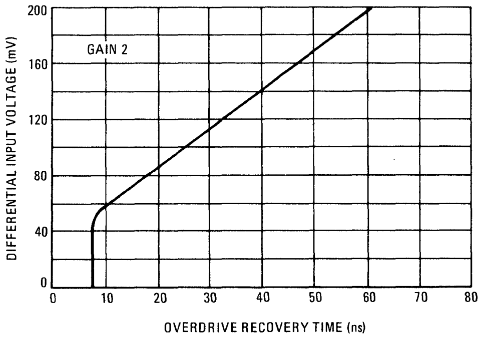


FIGURE 17 – PHASE SHIFT versus FREQUENCY

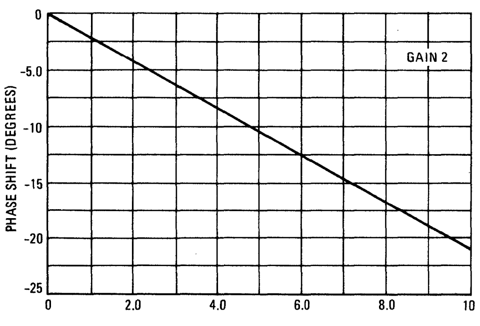
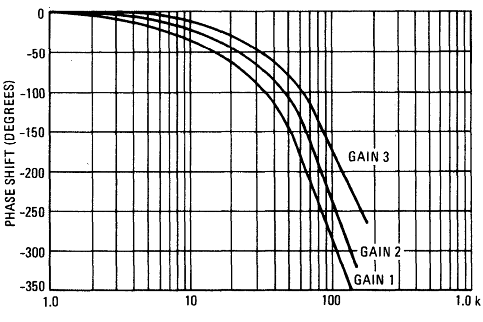


FIGURE 18 – PHASE SHIFT versus FREQUENCY



8

TYPICAL CHARACTERISTICS (continued)

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 19 – INPUT RESISTANCE versus TEMPERATURE

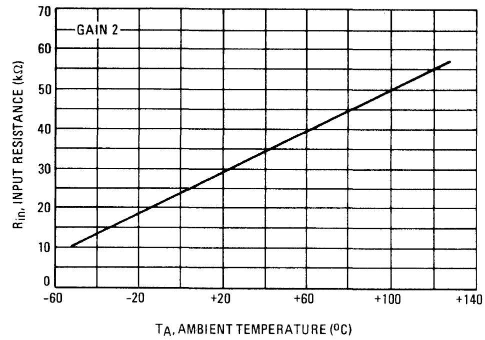


FIGURE 20 – INPUT NOISE VOLTAGE

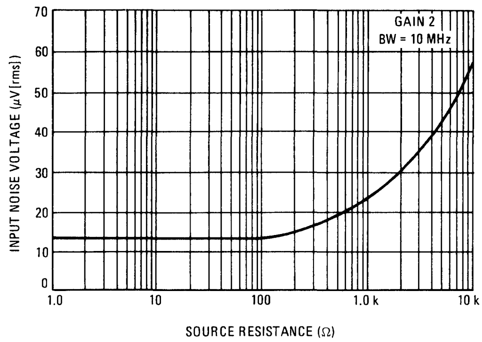


FIGURE 21 – OUTPUT VOLTAGE SWING and SINK CURRENT versus SUPPLY VOLTAGE

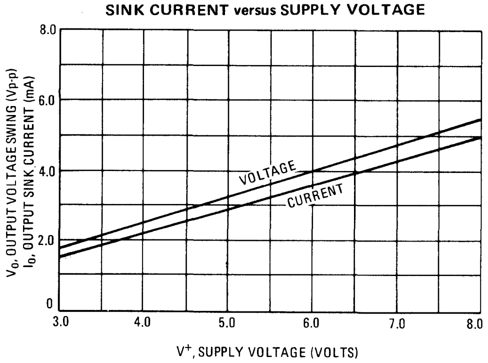


FIGURE 22 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

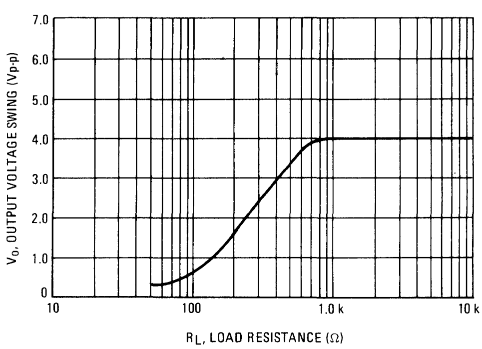


FIGURE 23 – OUTPUT VOLTAGE SWING versus FREQUENCY

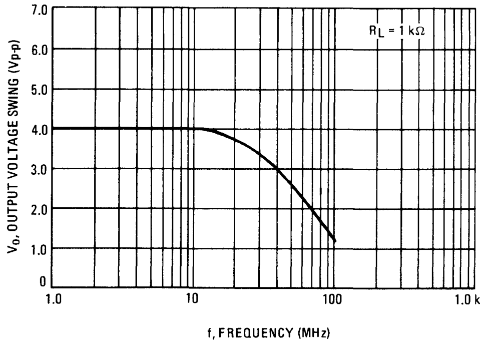
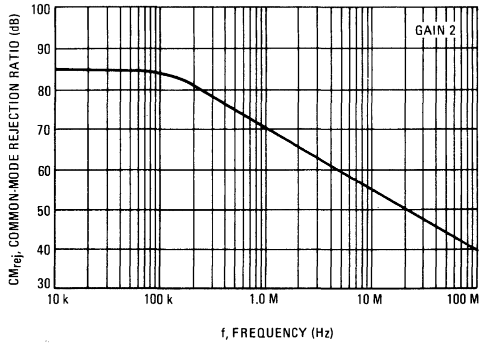


FIGURE 24 – COMMON-MODE REJECTION RATIO



8

MC1741
MC1741C

OPERATIONAL AMPLIFIERS

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

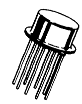
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

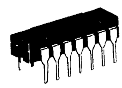
OPERATIONAL AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT

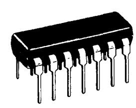
G SUFFIX
METAL PACKAGE
CASE 601



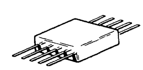
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



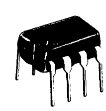
P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1741C only)



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1741C only)



PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G
"G" & "P1" Packages	1	2	3	4	5	6	7
"F" Package	2	3	4	5	6	7	8
"P2" & "L" Packages	3	4	5	6	9	10	11

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
		MC1741C	MC1741	
Power Supply Voltage	V^+ V^-	+18 -18	+22 -22	Vdc Vdc
Differential Input Signal	V_{in}	±30		Volts
Common Mode Input Swing (Note 1)	CMV_{in}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Power Dissipation (Package Limitation)	P_D			
Metal Can		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Flat Package		500		mW
Derate above T_A = +25°C		3.3		mW/°C
Plastic Dual In-Line Packages		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Ceramic Dual In-Line Package		750		mW/°C
Derate above T_A = +25°C		6.0		mW/°C
Operating Temperature Range	T_A	0 to +75	-55 to +125	°C
Storage Temperature Range	T_{stg}			°C
Metal, Flat and Ceramic Packages		-65 to +150		
Plastic Packages		-55 to +125		

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

CIRCUIT SCHEMATIC

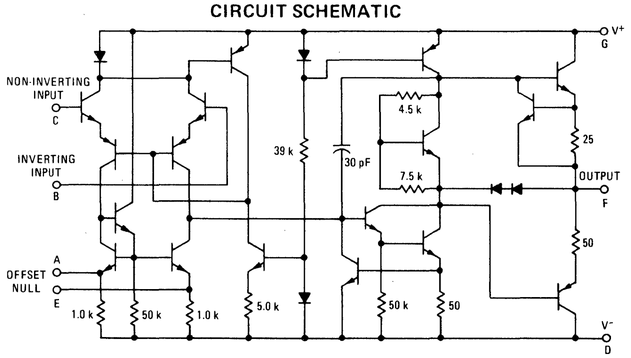
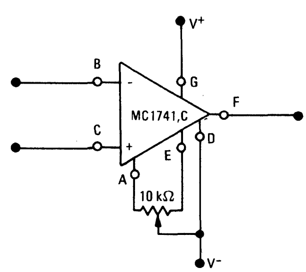


FIGURE 1 – OFFSET ADJUST CIRCUIT



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See Packaging Information Section for outline dimensions.
See current MCBC1741/MCB1741F data sheet for beam-lead chip information.
See current MCCF1741,C data sheet for flip-chip information.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = 15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1741 Min	MC1741 Typ	MC1741 Max	MC1741C ④ Min	MC1741C ④ Typ	MC1741C ④ Max	Unit
Open Loop Voltage Gain (R_L = 2.0 kΩ)	A_{VOL}							–
(V_o = ± 10 V, T_A = +25°C)		50,000	200,000	–	20,000	100,000	–	
(V_o = ± 10 V, T_A = T_{low} ① to T_{high} ②)		25,000	–	–	15,000	–	–	
Output Impedance (f = 20 Hz)	Z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	0.3	1.0	–	0.3	1.0	–	Meg Ω
Output Voltage Swing	V_o							V_{peak}
(R_L = 10 kΩ, T_A = +25°C)		±12	±14	–	±12	±14	–	
(R_L = 2.0 kΩ, T_A = +25°C)		±10	±13	–	±10	±13	–	
(R_L = 2.0 kΩ, T_A = T_{low} ① to T_{high} ②)		±10	–	–	±10	–	–	
Input Common-Mode Voltage Swing	CMV_{in}	±12	±13	–	±12	±13	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	70	90	–	70	90	–	dB
Input Bias Current	I_b							μA
(T_A = +25°C)		–	0.2	0.5	–	0.2	0.5	
(T_A = T_{low} ①)		–	0.5	1.5	–	–	0.8	
Input Offset Current	$\|I_{io}\|$							μA
(T_A = +25°C)		–	0.03	0.2	–	0.03	0.2	
(T_A = T_{low} ① to T_{high} ②)		–	–	0.5	–	–	0.3	
Input Offset Voltage (R_S = ≦ 10 kΩ)	$\|V_{io}\|$							mV
(T_A = +25°C)		–	1.0	5.0	–	2.0	6.0	
(T_A = T_{low} ① to T_{high} ②)		–	–	6.0	–	–	7.5	
Step Response								
Gain = 100, R_1 = 1.0 kΩ,	t_f	–	29	–	–	29	–	μs
R_2 = 100 kΩ, R_3 = 1.0 kΩ	t_{pd}	–	8.5	–	–	8.5	–	μs
	dV_{out}/dt ③	–	1.0	–	–	1.0	–	V/μs
Gain = 10, R_1 = 1.0 kΩ,	t_f	–	3.0	–	–	3.0	–	μs
R_2 = 10 kΩ, R_3 = 1.0 kΩ	t_{pd}	–	1.0	–	–	1.0	–	μs
	dV_{out}/dt ③	–	1.0	–	–	1.0	–	V/μs
Gain = 1, R_1 = 10 kΩ,	t_f	–	0.6	–	–	0.6	–	μs
R_2 = 10 kΩ, R_3 = 5.0 kΩ	t_{pd}	–	0.38	–	–	0.38	–	μs
	dV_{out}/dt ③	–	0.8	–	–	0.8	–	V/μs
Average Temperature Coefficient of Input Offset Voltage	$\|TC_{Vio}\|$							μV/°C
(R_S = 50 Ω, T_A = T_{low} ① to T_{high} ②)		–	3.0	–	–	3.0	–	
(R_S = 10 kΩ, T_A = T_{low} ① to T_{high} ②)		–	6.0	–	–	6.0	–	
Average Temperature Coefficient of Input Offset Current (T_A = T_{low} ① to T_{high} ②)	$\|TC_{Iio}\|$	–	50	–	–	50	–	pA/°C
DC Power Dissipation (Power Supply = ± 15 V, V_o = 0)	P_D	–	50	85	–	50	85	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	30	150	–	30	150	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	30	150	–	30	150	μV/V
Power Bandwidth (A_v = 1, R_L = 2.0 kΩ, THD = 5%, V_o = 20 V_{p-p})	PBW	–	10	–	–	10	–	kHz

① T_{low} = 0°C for MC1741C = -55°C for MC1741

② T_{high} = +75°C for MC1741C = +125°C for MC1741

③ dV_{out}/dt = Slew Rate

④ Plastic package offered in limited temperature range only.

8

TYPICAL CHARACTERISTICS

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 2 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

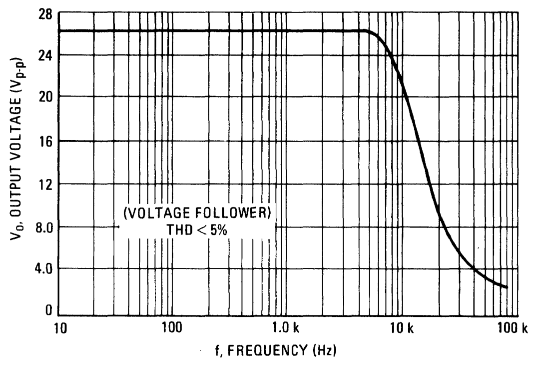

FIGURE 3 – OPEN LOOP FREQUENCY RESPONSE

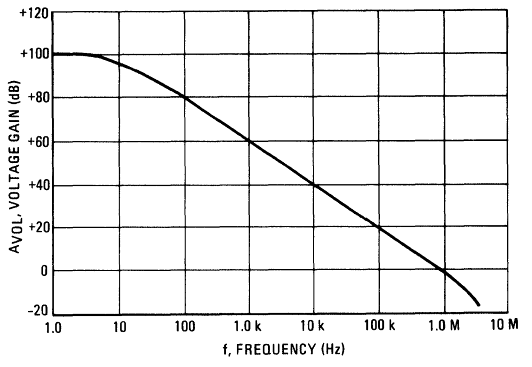

FIGURE 4 – OUTPUT NOISE versus SOURCE RESISTANCE

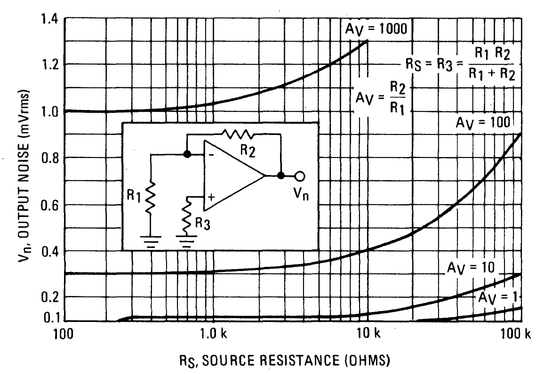

FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE

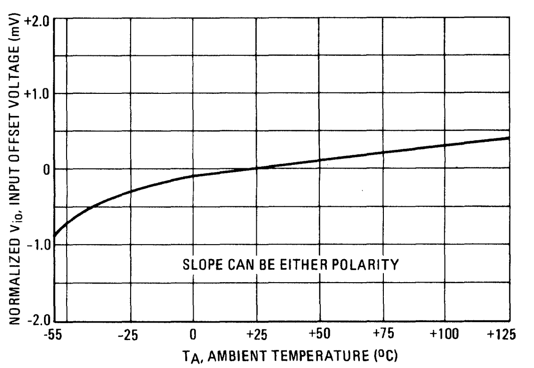

FIGURE 6 – INPUT OFFSET CURRENT versus TEMPERATURE

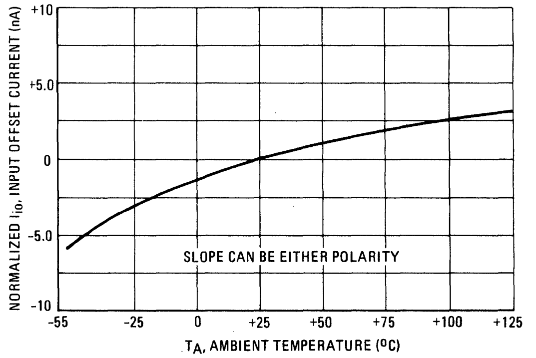

FIGURE 7 – INPUT BIAS CURRENT versus TEMPERATURE

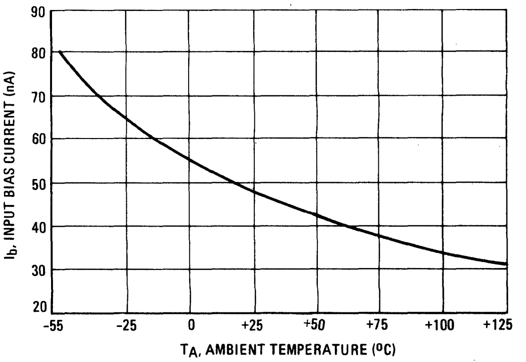

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FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

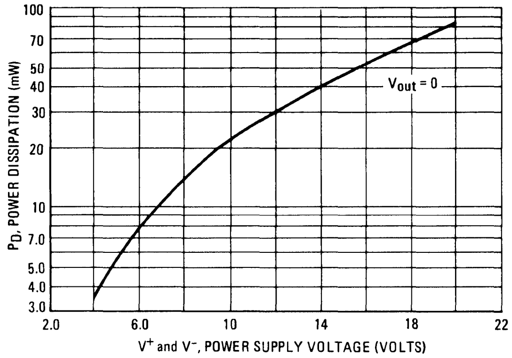


FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

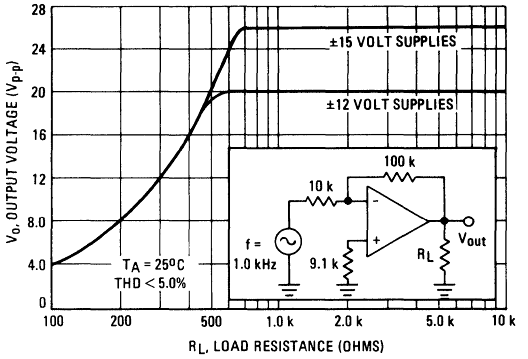
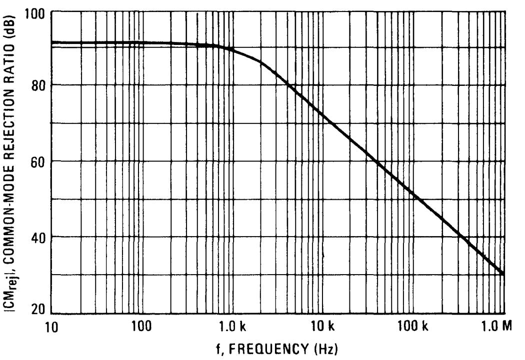


FIGURE 10 – COMMON-MODE REJECTION RATIO versus FREQUENCY



8

MC1741S
MC1741SC

OPERATIONAL AMPLIFIERS

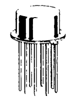
HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIER

The MC1741S/MC1741SC is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1741 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D-to-A converters due to its fast settling time and high slew rate.

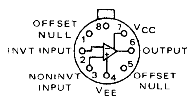
- High Slew Rate — 10 V/µs Guaranteed Minimum
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

OPERATIONAL AMPLIFIER

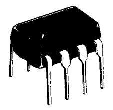
MONOLITHIC SILICON INTEGRATED CIRCUIT



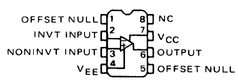
G SUFFIX
METAL PACKAGE
CASE 601



(Top View)

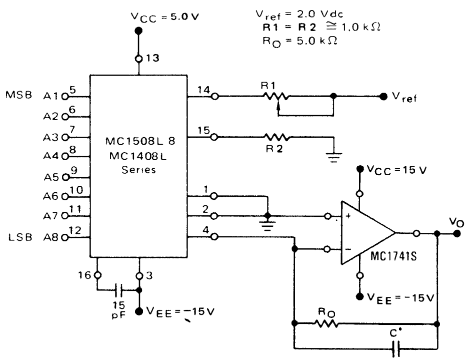


P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1741SC Only)



(Top View)

TYPICAL APPLICATION OF OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Pins not shown are not connected.

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 µs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 150 pF).

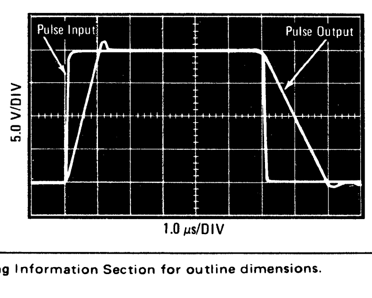
Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

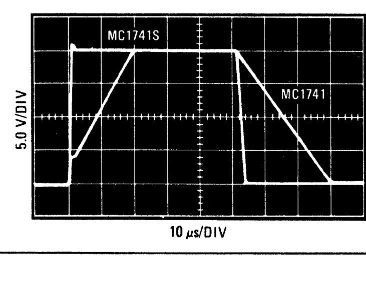
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\text{ V}}{1\text{ k}}(5\text{ k})\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\text{ V}\left[\frac{255}{256}\right] = 9.961\text{ V}$$

MC1741S LARGE-SIGNAL TRANSIENT RESPONSE



STANDARD MC1741 versus MC1741S RESPONSE COMPARISON



See Packaging Information Section for outline dimensions.

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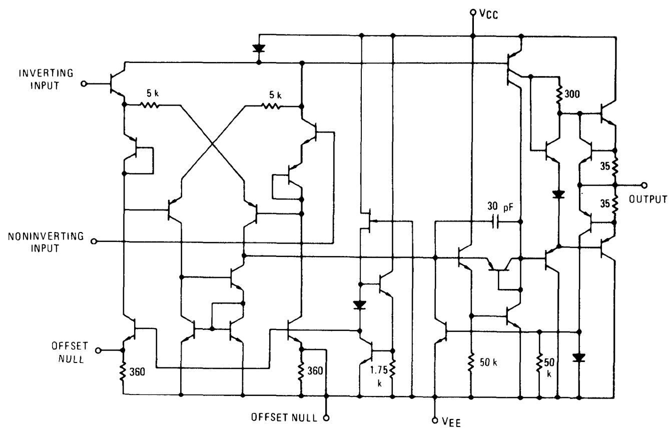
CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value MC1741SC	Value MC1741S	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Differential Input Signal Voltage	V_{in}	±30		Volts
Common-Mode Input Voltage Swing (See Note 1)	V_{ICR}	±15		Volts
Output Short-Circuit Duration (See Note 2)	t_s	Continuous		
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 625 5.0		 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	0 to +75	-55 to +125	°C
Storage Temperature Range Metal Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

FIGURE 1 – OFFSET ADJUST CIRCUIT

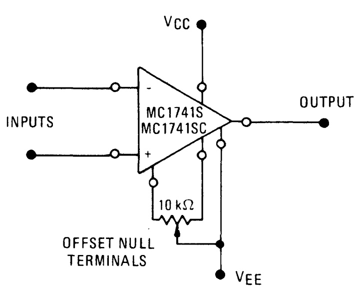
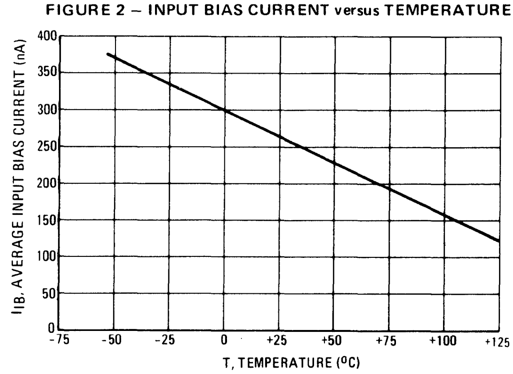


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE



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MC1741S, MC1741SC (continued)

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1741S Min	MC1741S Typ	MC1741S Max	MC1741SC** Min	MC1741SC** Typ	MC1741SC** Max	Unit
Power Bandwidth (See Figure 3)	PBW							kHz
A_V = 1, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)		150	200	–	150	200	–	
Large-Signal Transient Response								
Slew Rate (Figures 10 and 11)	SR							
V(–) to V(+)		10	20	–	10	20	–	V/μs
V(+) to V(–)		10	12	–	10	12	–	
Settling Time (Figures 10 and 11) (to within 0.1%)	t_{setlg}	–	3.0	–	–	3.0	–	μs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8)								
Rise Time	t_{TLH}	–	0.25	–	–	0.25	–	μs
Fall Time	t_{THL}	–	0.25	–	–	0.25	–	μs
Propagation Delay Time	t_{PLH}, t_{PHL}	–	0.25	–	–	0.25	–	μs
Overshoot	V_{OS}/V_O	–	20	–	–	20	–	%
Short-Circuit Output Currents	$I_{SO}\pm$	±10	–	±35	±10	–	±35	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ) (See Figure 4)	A_{vol}							–
V_O = ±10 V, T_A = +25°C		50,000	200,000	–	20,000	100,000	–	
V_O = ±10 V, T_A = T_{low}* to T_{high}*		25,000	–	–	15,000	–	–	
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_{in}	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing	V_O							V_{pk}
R_L = 10 kΩ, T_A = +25°C		±12	±14	–	±12	±14	–	
R_L = 2.0 kΩ, T_A = +25°C		±10	±13	–	±10	±13	–	
R_L = 2.0 kΩ, T_A = T_{low} to T_{high}		±10	–	–	±10	–	–	
Input Common-Mode Voltage Swing	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2)	I_{IB}							μA
T_A = +25°C		–	0.2	0.5	–	0.2	0.5	
T_A = T_{low}		–	0.5	1.5	–	–	0.8	
Input Offset Current	$\|I_{IO}\|$							μA
T_A = +25°C		–	0.03	0.2	–	0.03	0.2	
T_A = T_{low} to T_{high}		–	–	0.5	–	–	0.3	
Input Offset Voltage (R_S = ≤10 kΩ)	$\|V_{IO}\|$							mV
T_A = +25°C		–	1.0	5.0	–	2.0	6.0	
T_A = T_{low} to T_{high}		–	–	6.0	–	–	7.5	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} to T_{high})	$\|TCV_{IO}\|$							μV/°C
R_S = 50Ω		–	3.0	–	–	3.0	–	
R_S = 10 kΩ		–	6.0	–	–	6.0	–	
Average Temperature Coefficient of Input Offset Current (T_A = T_{low} to T_{high})	$\|TCI_{IO}\|$	–	50	–	–	50	–	pA/°C
DC Power Dissipation (See Figure 9) (Power Supply = ±15 V, V_O = 0)	P_D	–	50	85	–	50	85	mW
Positive Voltage Supply Sensitivity (V_{EE} constant)	S^+	–	2.0	150	–	2.0	150	μV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	S^-	–	10	150	–	10	150	μV/V

*T_{low} = 0 for MC1741SC T_{high} = +75°C for MC1741SC
= −55 °C for MC1741S = +125 °C for MC1741S

**Plastic package offered in limited temperature range device only.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

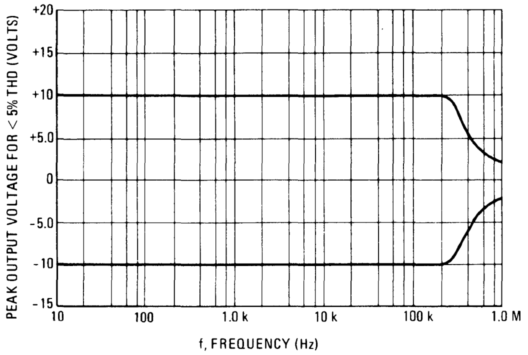


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

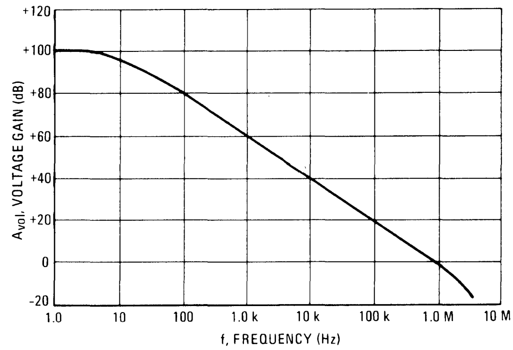


FIGURE 5 – NOISE versus FREQUENCY

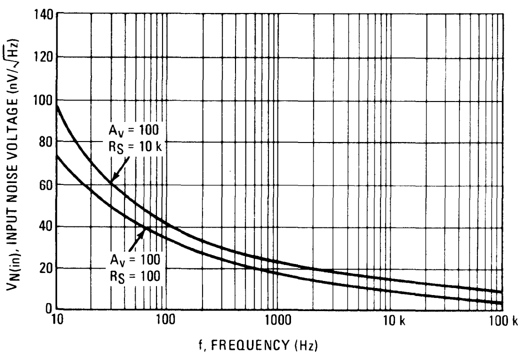


FIGURE 6 – OUTPUT NOISE versus SOURCE RESISTANCE

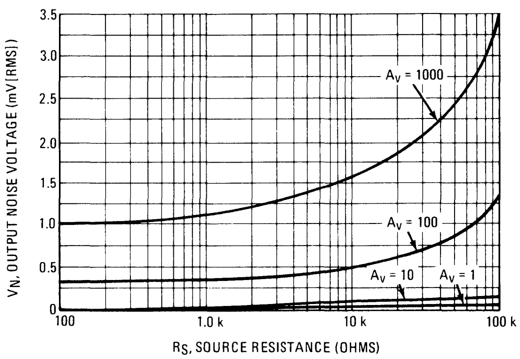


FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

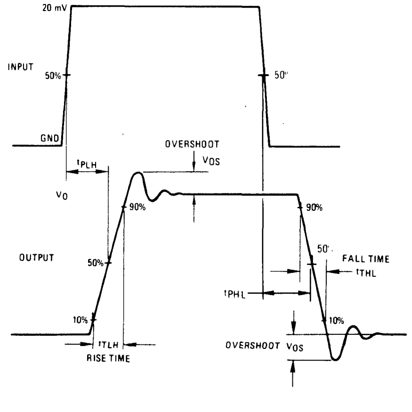
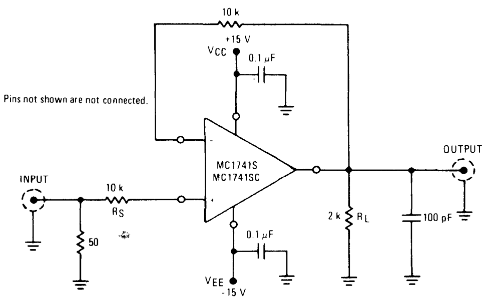


FIGURE 8 – SMALL-SIGNAL TRANSIENT RESPONSE TEST CIRCUIT



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 9 – POWER DISSIPATION versus POWER SUPPLY VOLTAGES

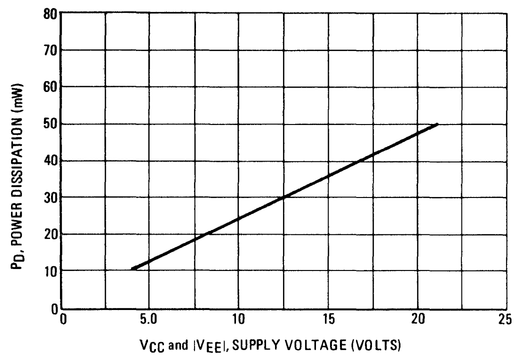


FIGURE 10 – LARGE-SIGNAL TRANSIENT WAVEFORMS

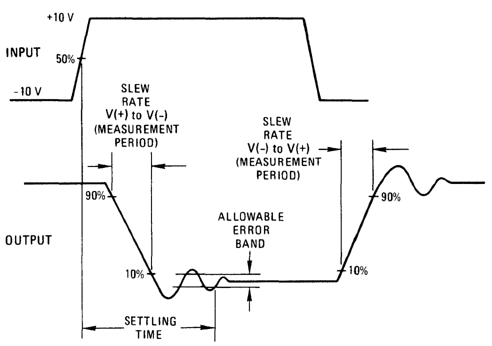
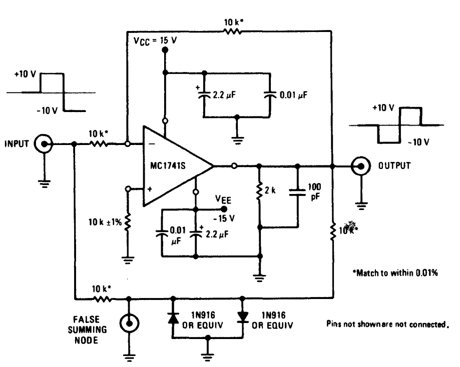


FIGURE 11 – SLEW RATE AND SETTLING TIME TEST CIRCUIT



SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time
x = amplifier settling time (to be determined)
y = false summing junction settling time
z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1741S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L-8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

FIGURE 12 – WAVEFORM AT FALSE SUMMING NODE

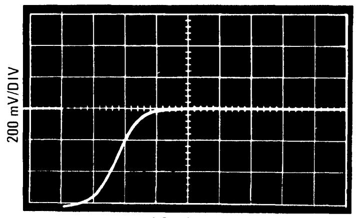
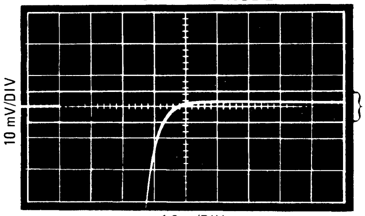
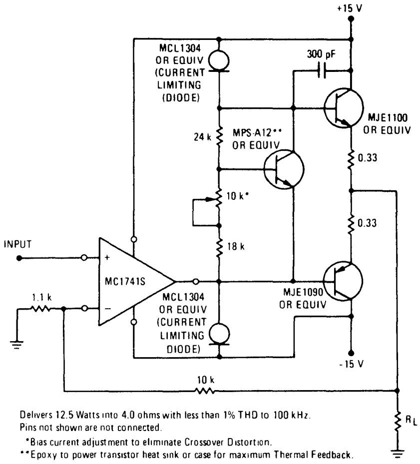


FIGURE 13 – EXPANDED WAVEFORM AT FALSE SUMMING NODE



TYPICAL APPLICATION

FIGURE 14 – 12.5-WATT WIDEBAND POWER AMPLIFIER



Delivers 12.5 Watts into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.
*Bias current adjustment to eliminate Crossover Distortion.
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.

8

MC1747
MC1747C

OPERATIONAL AMPLIFIER

DUAL MC1741
INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

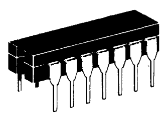
. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally, electrically, and pin-for-pin equivalent to the μA747 and μA747C respectively.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Offset Voltage Null Capability

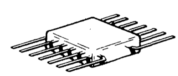
(DUAL MC1741)

DUAL OPERATIONAL AMPLIFIER

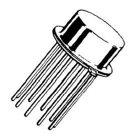
MONOLITHIC SILICON INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

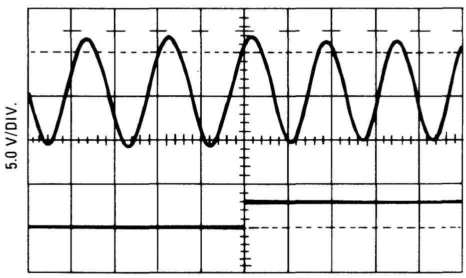


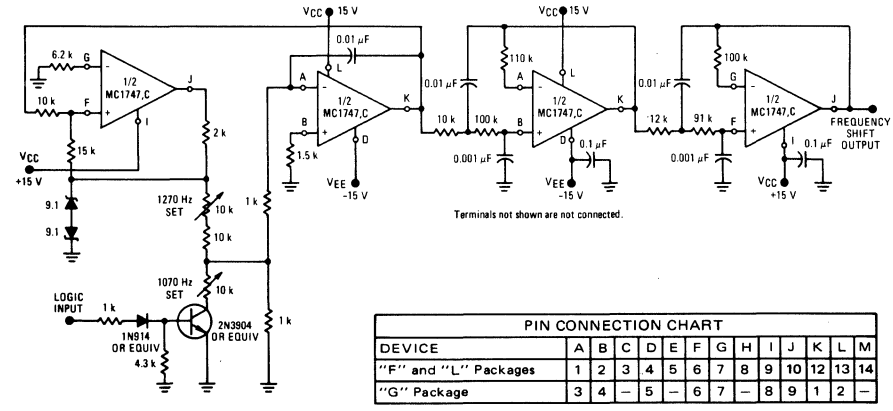
F SUFFIX
CERAMIC PACKAGE
CASE 607



G SUFFIX
METAL PACKAGE
CASE 603
(TO-100)

FIGURE 1 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR





PIN CONNECTION CHART													
DEVICE	A	B	C	D	E	F	G	H	I	J	K	L	M
"F" and "L" Packages	1	2	3	4	5	6	7	8	9	10	12	13	14
"G" Package	3	4	–	5	–	6	7	–	8	9	1	2	–

See Packaging Information Section for outline dimensions.

8

MC1747, MC1747C (continued)

MAXIMUM RATINGS (T_A +25°C unless otherwise noted.)

Rating	Symbol	MC1747	MC1747C	Unit
Power Supply Voltages	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Signal Voltage ①	V_{ID}	± 30		Volts
Common-Mode Input Swing Voltage ②	V_{ICR}	± 15		Volts
Output Short-Circuit Duration	t_{OS}	Continuous		
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +60°C	P_D	 750 6.0		 mW mW/°C
Voltage (Measurement between Offset Null and V_{EE})		± 0.5		Volts
Operating Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

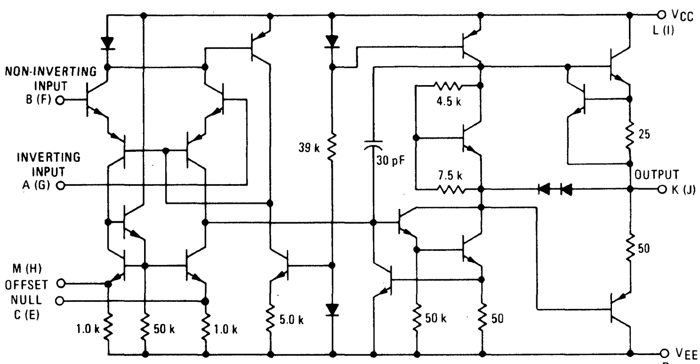
ELECTRICAL CHARACTERISTICS (V_{CC} +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristics	Symbol	MC1747 Min	MC1747 Typ	MC1747 Max	MC1747C Min	MC1747C Typ	MC1747C Max	Unit
Input Bias Current	I_{IB}							nAdc
T_A = +25°C		–	80	500	–	80	500	
T_A = T_{high} ③		–	30	500	–	30	800	
T_A = T_{low} ③		–	300	1500	–	30	800	
Input Offset Current	$\|I_{IO}\|$							nAdc
T_A = +25°C		–	20	200	–	20	200	
T_A = T_{high}		–	7.0	200	–	7.0	300	
T_A = T_{low}		–	85	500	–	7.0	300	
Input Offset Voltage ($R_S \leqslant$ 10 kΩ)	$\|V_{IO}\|$							mVdc
T_A = +25°C		–	1.0	5.0	–	1.0	6.0	
T_A = T_{low} to T_{high}		–	1.0	6.0	–	1.0	7.5	
Offset Voltage Adjustment Range		–	± 15	–	–	± 15	–	mV
Differential Input Impedance (Open-loop, f = 20 Hz)								
Parallel Input Resistance	R_p	0.3	2.0	–	0.3	2.0	–	Megohms
Parallel Input Capacitance	C_p	–	1.4	–	–	1.4	–	pF
Common-Mode Input Voltage Swing $T_{low} \leqslant T_A \leqslant T_{high}$	V_{ICR}	± 12	± 13	–	± 12	± 13	–	Volts
Common-Mode Rejection Ratio (R_S = 10 kΩ) $T_{low} \leqslant T_A \leqslant T_{high}$	CMRR	70	90	–	70	90	–	dB
Open-Loop Voltage Gain	A_{vol}							Volts
T_A = +25°C (V_O = ±10 V, R_L = 2.0 kΩ)		50,000	200,000	–	25,000	200,000	–	
T_A = T_{low} to T_{high} (V_O = ±10 V, R_L = 2.0 kΩ)		25,000	–	–	15,000	–	–	
Transient Response (Unity Gain) (V_{in} = 20 mV, R_L = 2.0 kΩ, $C_L \leqslant$ 100 pF)								
Rise Time	t_{PLH}	–	0.3	–	–	0.3	–	µs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate (Unity Gain)	SR	–	0.5	–	–	0.5	–	V/µs
Output Impedance	z_o	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{OS}	–	25	–	–	25	–	mAdc
Channel Separation		–	120	–	–	120	–	dB
Output Voltage Swing ($T_{low} \leqslant T_A \leqslant T_{high}$)	V_O							V_{pk}
R_L = 10 kΩ		± 12	± 14	–	± 12	± 14	–	
R_L = 2.0 kΩ		± 10	± 13	–	± 10	± 13	–	
Power Supply Sensitivity (T_{low} to T_{high})								µV/V
V_{EE} = Constant, $R_S \leqslant$ 10 kΩ	S^+	–	30	150	–	30	150	
V_{CC} = Constant, $R_S \leqslant$ 10 kΩ	S^-	–	30	150	–	30	150	
Power Supply Current (each amplifier)	I_D^+, I_D^-							mAdc
T_A = +25°C		–	1.7	2.8	–	1.7	2.8	
T_A = T_{low}		–	2.0	3.3	–	2.0	3.3	
T_A = T_{high}		–	1.5	2.5	–	2.0	3.3	
DC Power Dissipation (each amplifier)	P_D							mW
T_A = +25°C		–	50	85	–	50	85	
T_A = T_{low}		–	60	100	–	60	100	
T_A = T_{high}		–	45	75	–	60	100	

① For supply voltages of less than ± 15 V, the maximum differential input voltage is equal to ± (V_{CC} + $|V_{EE}|$).
② For supply voltages of less than ± 15 V, the maximum input voltage is equal to the supply voltage (+V_{CC}, -$|V_{EE}|$).
③ T_{low}: 0°C for MC1747CL
-55°C for MC1747L
T_{high}: +75°C for MC1747CL
+125°C for MC1747L

8

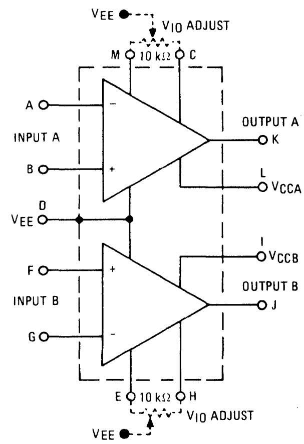
FIGURE 2 – CIRCUIT SCHEMATIC



The letters without parenthesis denote the pin numbers for 1/2 of the dual circuit, letters in parenthesis denote the pin numbers for the other half.

PIN CONNECTION CHART													
DEVICE	A	B	C	D	E	F	G	H	I	J	K	L	M
"F" and "L" Packages	1	2	3	4	5	6	7	8	9	10	12	13	14
"G" Package	3	4	–	5	–	6	7	–	8	9	1	2	–

FIGURE 3 – EQUIVALENT CIRCUIT WITH OFFSET ADJUST



Offset Null is available only in Ceramic flat and dual in-line packages.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = –15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE

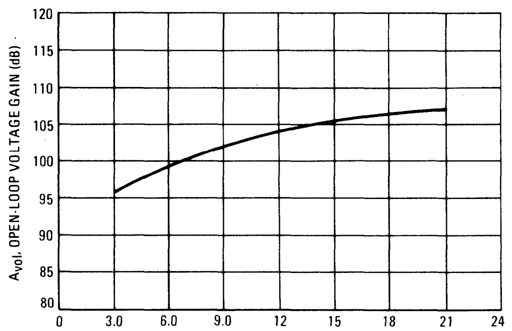


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

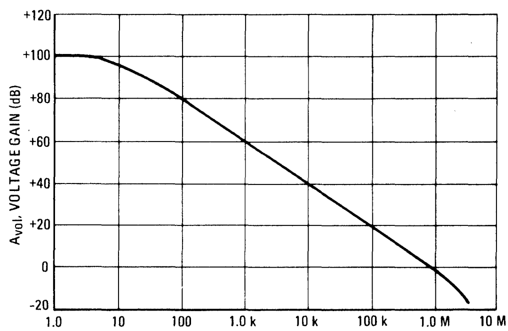


FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

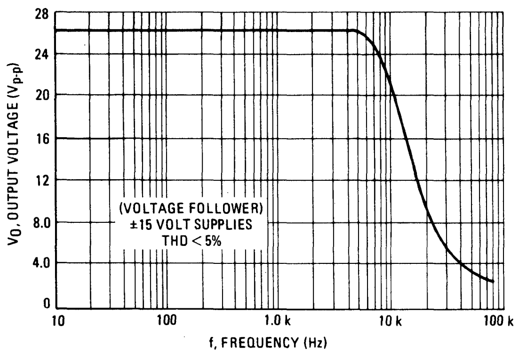
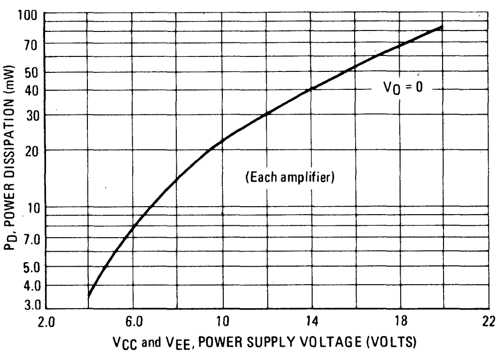


FIGURE 7 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 8 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

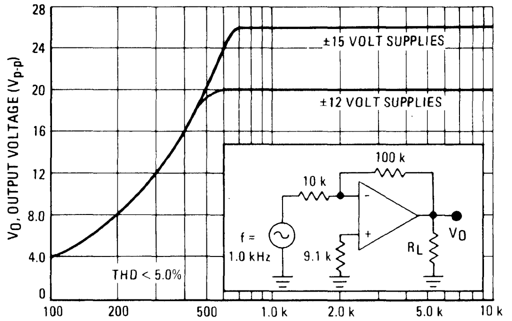


FIGURE 9 – OUTPUT NOISE versus SOURCE RESISTANCE

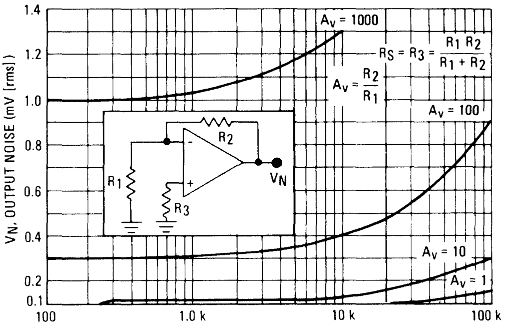
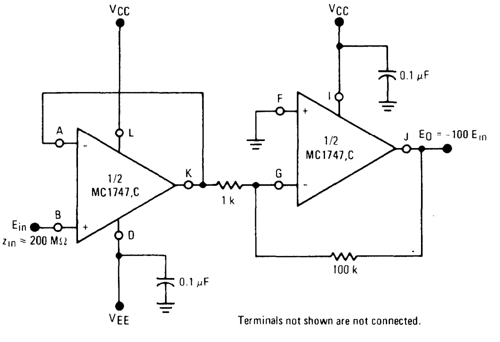


FIGURE 10 – HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER



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MC1748G
MC1748CG

HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Noncompensated MC1741G
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

METAL PACKAGE
CASE 601

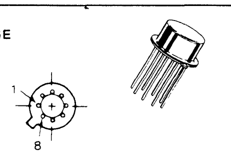


FIGURE 1 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

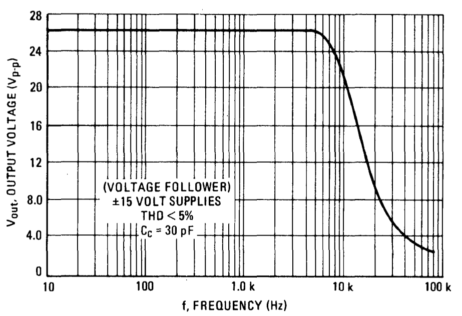


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

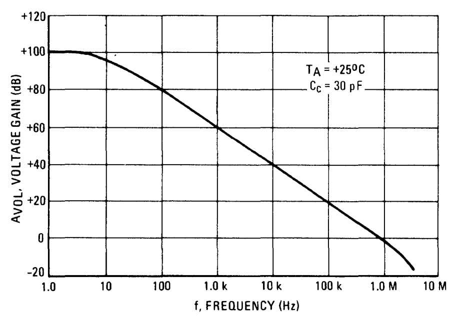


FIGURE 3 – CIRCUIT SCHEMATIC

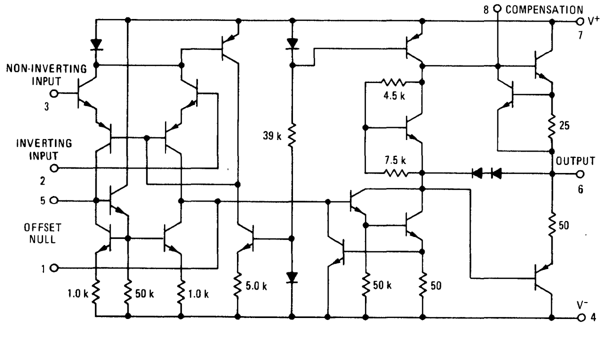
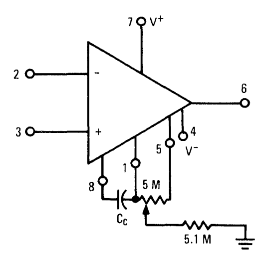


FIGURE 4 – OFFSET ADJUST AND FREQUENCY COMPENSATION



See Packaging Information Section for outline dimensions.

See current MCC1748/1748C data sheet for standard linear chip information.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1748G	MC1748CG	Unit
Power Supply Voltage	V^+ V^-	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{in}	±30		Volts
Common-Mode Input Swing ①	CMV_{in}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1748G Min	MC1748G Typ	MC1748G Max	MC1748CG Min	MC1748CG Typ	MC1748CG Max	Unit
Input Bias Current	I_b							µAdc
T_A = +25°C		–	0.08	0.5	–	0.08	0.5	
T_A = T_{low} to T_{high} ②		–	0.3	1.5	–	–	0.8	
Input Offset Current	$\|I_{io}\|$							µAdc
T_A = +25°C		–	0.02	0.2	–	0.02	0.2	
T_A = T_{low} to T_{high}		–	0.08	0.5	–	–	0.3	
Input Offset Voltage ($R_S \le 10$ k Ω)	$\|V_{io}\|$							mVdc
T_A = +25°C		–	1.0	5.0	–	1.0	6.0	
T_A = T_{low} to T_{high}		–	–	6.0	–	–	7.5	
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	0.3	2.0	–	0.3	2.0	–	Megohm
Parallel Input Capacitance	C_p	–	1.4	–	–	1.4	–	pF
Common-Mode Input Impedance (f = 20 Hz)	$Z_{(in)}$	–	200	–	–	200		Megohms
Common-Mode Input Voltage Swing	CMV_{in}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	70	90	–	70	90	–	dB
Open-Loop Voltage Gain, (V_O = ±10 V, R_L = 2.0 k ohms)	A_{VOL}							V/V
T_A = +25°C		50,000	200,000	–	20,000	200,000	–	
T_A = T_{low} to T_{high}		25,000	–	–	15,000	–	–	
Step Response (V_{in} = 20 mV, C_c = 30 pF, R_L = 2 kΩ, C_L = 100 pF)								
Rise Time	t_r	–	0.3	–	–	0.3	–	µs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate	dV_{out}/dt	–	0.8	–	–	0.8	–	V/µs
Output Impedance (f = 20 Hz)	Z_{out}	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{SC}	–	25	–	–	25	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_o	±12	±14	–	±12	±14	–	Vpk
R_L = 2 k ohms (T_A = T_{low} to t_{high})		±10	±13	–	±10	±13	–	
Power Supply Sensitivity								µV/V
V^- = constant, $R_s \le 10$ k ohms	S+	–	30	150	–	30	150	
V^+ = constant, $R_s \le 10$ k ohms	S–	–	30	150	–	30	150	
Power Supply Current	I_D^+	–	1.67	2.83	–	1.67	2.83	mAdc
	I_D^-	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation (V_o = 0)	P_D	–	50	85	–	50	85	mW

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.

② T_{low}: 0°C for MC1748CG
-55°C for MC1748G
T_{high}: +75°C for MC1748CG
+125°C for MC1748G

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MC1776G
MC1776CG

OPERATIONAL AMPLIFIERS

Specifications and Applications Information

MONOLITHIC MICROPOWER PROGRAMMABLE OPERATIONAL AMPLIFIER

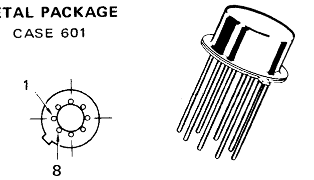
This extremely versatile operational amplifier features low-power consumption, high input impedance and low input noise levels. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current, power consumption and input voltage,and current noise despite wide variations in operating power supply voltages.

- ±1.2 V to ±18 V Operation
- Wide Programming Range
- Low Noise
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

PROGRAMMABLE OPERATIONAL AMPLIFIER

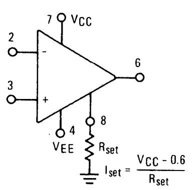
EPITAXIAL PASSIVATED INTEGRATED CIRCUIT

METAL PACKAGE
CASE 601



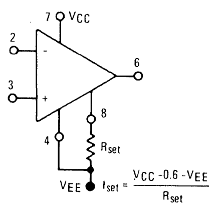
RESISTIVE PROGRAMMING (See Figure 1.)

R_{set} to GROUND



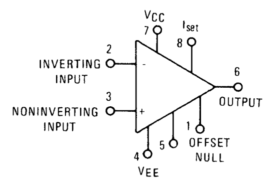
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 μA	I_{set} = 15 μA
±6.0V	3.6 MΩ	360 kΩ
±10V	6.2 MΩ	620 kΩ
±12V	7.5 MΩ	750 kΩ
±15V	10 MΩ	1.0 MΩ

R_{set} to NEGATIVE SUPPLY
(Recommended for supply voltage less than ±6.0 V)



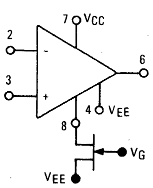
Typical R_{set} Values		
V_{CC}, V_{EE}	Iset = 1.5 μA	I_{set} = 15 μA
±1.5V	1.6 MΩ	160 kΩ
±3.0V	3.6 MΩ	360 kΩ
±6.0V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

PIN CONNECTIONS

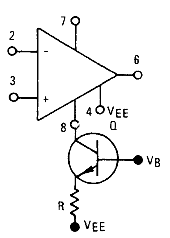


ACTIVE PROGRAMMING

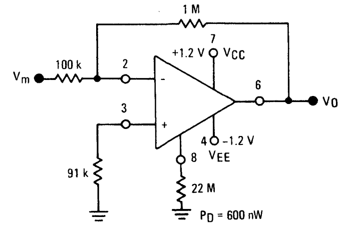
FET CURRENT SOURCE



BIPOLAR CURRENT SOURCE



NANOWATT AMPLIFIER APPLICATION



Pins not shown are not connected.
See Packaging Information Section for outline dimensions.

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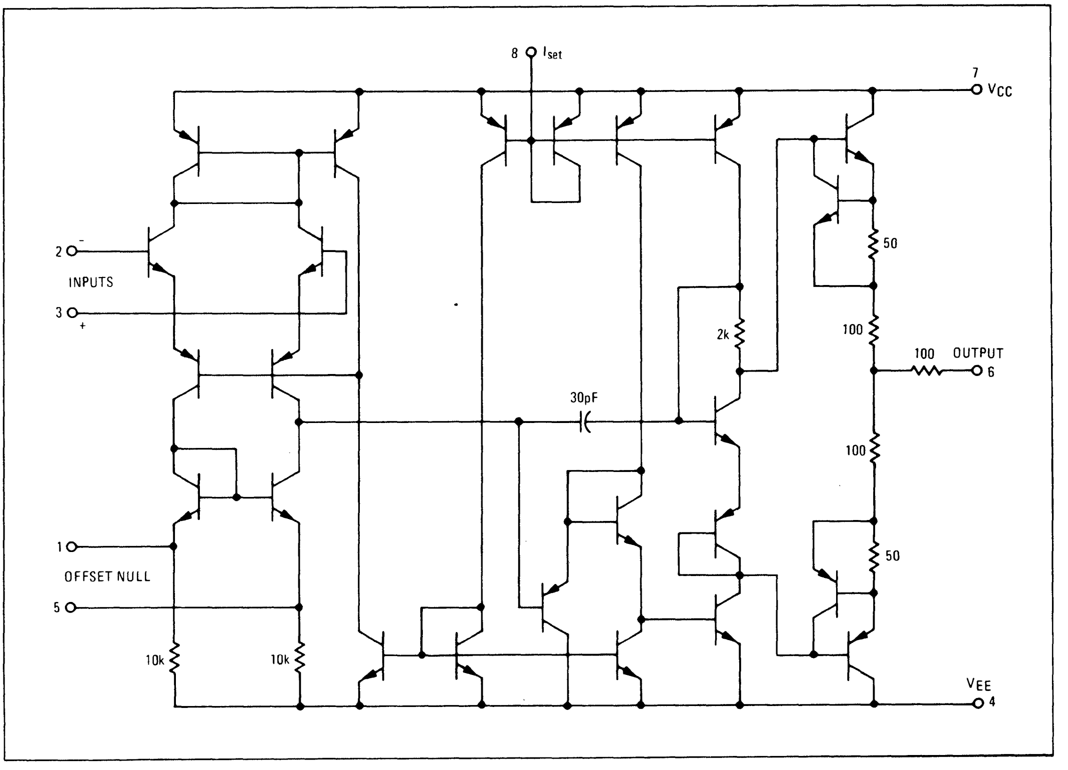
MC1776G, MC1776CG (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Differential Input Voltage	V_{ID}	±30	Vdc
Common-Mode Input Voltage V_{CC} and $\lvert V_{EE} \rvert < 15$ V V_{CC} and $\lvert V_{EE} \rvert \geqslant 15$ V	V_{ICM}	 V_{CC}, V_{EE} ±15	Vdc
Offset Null to V_{EE} Voltage	$V_{off}-V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	500	µA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	(V_{CC} - 2.0 V) to V_{CC}	Vdc
Output Short-Circuit Duration*	t_s	Indefinite	s
Operating Temperature Range MC1776 MC1776C	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6	mW mW/C°

*May be to ground or either Supply Voltage. Rating applies up to a case temperature of +125°C or ambient temperature of +75°C and $I_{set} \leqslant 30\,\mu A$.

SCHEMATIC DIAGRAM



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ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 Vdc, V_{EE} = −3.0 Vdc, I_{set} = 1.5 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leqslant 10$ kΩ)	$\|V_{IO}\|$							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* $\leqslant T_A \leqslant T_{high}$*		–	–	6.0	–	–	7.5	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C		–	0.7	3.0	–	0.7	6.0	
$T_A = T_{high}$		–	–	5.0	–	–	6.0	
$T_A = T_{low}$		–	–	10	–	–	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	2.0	7.5	–	2.0	10	
$T_A = T_{high}$		–	–	7.5	–	–	10	
$T_A = T_{low}$		–	–	20	–	–	20	
Input Resistance	R_{in}	–	50	–	–	50	–	MΩ
Input Capacitance	C_{in}	–	2.0	–	–	2.0	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	–	9.0	–	mV
Large Signal Voltage Gain	A_{vol}							V/V
$R_L \geqslant 75$ kΩ, $V_O = \pm1.0$ V, T_A = +25°C		50 k	200 k	–	25 k	200 k	–	
$R_L \geqslant 75$ kΩ, $V_O = \pm1.0$ V, $T_{low} \leqslant T_A \leqslant T_{high}$		25 k	–	–	25 k	–	–	
Output Resistance	R_O	–	5.0	–	–	5.0	–	kΩ
Output Short-Circuit Current	I_{OSC}	–	3.0	–	–	3.0	–	mA
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	13	20	–	13	20	
$T_{low} \leqslant T_A \leqslant T_{high}$		–	–	25	–	–	25	
Power Dissipation	P_D							μW
T_A = +25°C		–	78	120	–	78	120	
$T_{low} \leqslant T_A \leqslant T_{high}$		–	–	150	–	–	150	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geqslant 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	3.0	–	–	3.0	–	μs
Overshoot	OS	–	0	–	–	0	–	%
Slew Rate ($R_L \geqslant 5.0$ kΩ)	S_R	–	0.03	–	–	0.03	–	V/μs
Output Voltage Swing	V_O							V
$R_L \geqslant 75$ kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$		±2.0	±2.4	–	±2.0	±2.4	–	
Input Voltage Range	V_{ID}							V
$T_{low} \leqslant T_A \leqslant T_{high}$		±1.0	–	–	±1.0	–	–	
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leqslant 10$ kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$		70	86	–	70	86	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leqslant 10$ kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$		–	25	150	–	25	200	

*T_{low} = −55°C for MC1776, 0°C for MC1776C T_{high} = +125°C for MC1776, +70°C for MC1776C

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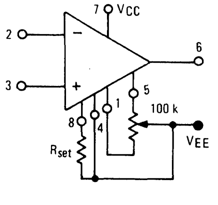
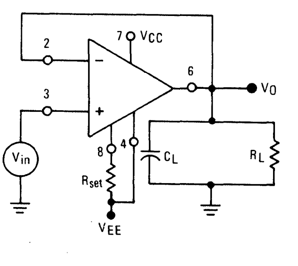
VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT-RESPONSE TEST CIRCUIT



MC1776G, MC1776CG (continued)

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = −3.0 V, I_{set} = 15 µA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	$\lvert V_{IO} \rvert$							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* $\leq T_A \leq T_{high}$*		–	–	6.0	–	–	7.5	
Input Offset Current	$\lvert I_{IO} \rvert$							nA
T_A = +25°C		–	2.0	15	–	2.0	25	
$T_A = T_{high}$		–	–	15	–	–	25	
$T_A = T_{low}$		–	–	40	–	–	40	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	15	50	–	15	50	
$T_A = T_{high}$		–	–	50	–	–	50	
$T_A = T_{low}$		–	–	120	–	–	100	
Input Resistance	R_{in}	–	5.0	–	–	5.0	–	MΩ
Input Capacitance	C_{in}	–	2.0	–	–	2.0	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	–	18	–	mV
Large Signal Voltage Gain	A_{vol}							V/V
$R_L \geq 5.0$ kΩ, $V_O = \pm1.0$ V, T_A = +25°C		50 k	200 k	–	25 k	200 k	–	
$R_L \geq 5.0$ kΩ, V_O = 1.0 V, $T_{low} \leq T_A \leq T_{high}$		25 k	–	–	25 k	–	–	
Output Resistance	R_O	–	1.0	–	–	1.0	–	kΩ
Output Short-Circuit Current	I_{OSC}	–	5.0	–	–	5.0	–	mA
Supply Current	I_{CC}, I_{EE}							µA
T_A = +25°C		–	130	160	–	130	170	
$T_{low} \leq T_A \leq T_{high}$		–	–	180	–	–	180	
Power Dissipation	P_D							µW
T_A = +25°C		–	780	960	–	780	1020	
$T_{low} \leq T_A \leq T_{high}$		–	–	1080	–	–	1080	
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	0.6	–	–	0.6	–	µs
Overshoot	OS	–	5.0	–	–	5.0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	SR	–	0.35	–	–	0.35	–	V/µs
Output Voltage Swing	V_O							V
$R_L \geq 5.0$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±1.9	±2.1	–	±2.0	±2.1	–	
Input Voltage Range	V_{ID}							V
$T_{low} \leq T_A \leq T_{high}$		±1.0	–	–	±1.0	–	–	
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	86	–	70	86	–	
Supply Voltage Rejection Ratio	PSRR							µV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	150	–	25	200	

*T_{low} = −55°C for MC1776, 0°C for MC1776C; T_{high} = +125°C for MC1776, +70°C for MC1776C

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ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 1.5 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \leqslant 10$ kΩ)	$\lvert V_{IO} \rvert$							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* $\leqslant T_A \leqslant T_{high}$*		–	–	6.0	–	–	7.5	
Input Offset Current	$\lvert I_{IO} \rvert$							nA
T_A = +25°C		–	0.7	3.0	–	0.7	6.0	
$T_A = T_{high}$		–	–	5.0	–	–	6.0	
$T_A = T_{low}$		–	–	10	–	–	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	2.0	7.5	–	2.0	10	
$T_A = T_{high}$		–	–	7.5	–	–	10	
$T_A = T_{low}$		–	–	20	–	–	20	
Input Resistance	R_{in}	–	50	–	–	50	–	MΩ
Input Capacitance	C_{in}	–	2.0	–	–	2.0	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	–	9.0	–	mV
Large Signal Voltage Gain	A_{vol}							V/V
$R_L \geqslant 75$ kΩ, V_O = ±10 V, T_A = +25°C		200 k	400 k	–	50 k	400 k	–	
$R_L \geqslant 75$ kΩ, V_O = ±10 V, $T_{low} \leqslant T_A \leqslant T_{high}$		100 k	–	–	50 k	–	–	
Output Resistance	R_O	–	5.0	–	–	5.0	–	kΩ
Output Short-Circuit Current	I_{OSC}	–	3.0	–	–	3.0	–	mA
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	20	25	–	20	30	
$T_{low} \leqslant T_A \leqslant T_{high}$		–	–	30	–	–	35	
Power Dissipation	P_D							mW
T_A = +25°C		–	–	0.75	–	–	0.9	
$T_{low} \leqslant T_A \leqslant T_{high}$		–	–	0.9	–	–	1.05	
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \geqslant 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	1.6	–	–	1.6	–	μs
Overshoot	OS	–	0	–	–	0	–	%
Slew Rate ($R_L \geqslant 5.0$ kΩ)	SR	–	0.1	–	–	0.1	–	V/μs
Output Voltage Swing	V_O							V
$R_L \geqslant 75$ kΩ, T_A = +25°C		±12	±14	–	±12	±14	–	
$R_L \geqslant 75$ kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$		±10	–	–	±10	–	–	
Input Voltage Range $T_{low} \leqslant T_A \leqslant T_{high}$	V_{ID}	±10	–	–	±10	–	–	V
Common-Mode Rejection Ratio $R_S \leqslant 10$ kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio $R_S \leqslant 10$ kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$	PSRR	–	25	150	–	25	200	μV/V

*T_{low} = −55°C for MC1776
0°C for MC1776C

T_{high} = +125°C for MC1776
+70°C for MC1776C

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ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \leqslant 10$ kΩ)	$\|V_{IO}\|$							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* $\leqslant T_A \leqslant T_{high}$*		–	–	6.0	–	–	7.5	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C		–	2.0	15	–	2.0	25	
$T_A = T_{high}$		–	–	15	–	–	25	
$T_A = T_{low}$		–	–	40	–	–	40	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	15	50	–	15	50	
$T_A = T_{high}$		–	–	50	–	–	50	
$T_A = T_{low}$		–	–	120	–	–	100	
Input Resistance	R_{in}	–	5.0	–	–	5.0	–	MΩ
Input Capacitance	C_{in}	–	2.0	–	–	2.0	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	–	18	–	mV
Large Signal Voltage Gain	A_{vol}							V/V
$R_L \geqslant 5.0$ kΩ, $V_O = \pm10$ V, T_A = +25°C		100 k	400 k	–	50 k	400 k	–	
$R_L \geqslant 75$ kΩ, $V_O = \pm10$ V $T_{low} \leqslant T_A \leqslant T_{high}$		75 k	–	–	50 k	–	–	
Output Resistance	R_O	–	1.0	–	–	1.0	–	kΩ
Output Short-Circuit Current	I_{OSC}	–	12	–	–	12	–	mA
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	160	180	–	160	190	
$T_{low} \leqslant T_A \leqslant T_{high}$		–	–	200	–	–	200	
Power Dissipation	P_D							mW
T_A = +25°C		–	–	5.4	–	–	5.7	
$T_{low} \leqslant T_A \leqslant T_{high}$		–	–	6.0	–	–	6.0	
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \geqslant 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	0.35	–	–	0.35	–	μs
Overshoot	OS	–	10	–	–	10	–	%
Slew Rate ($R_L \geqslant 5.0$ kΩ)	SR	–	0.8	–	–	0.8	–	V/μs
Output Voltage Swing	V_O							V
$R_L \geqslant 5.0$ kΩ, T_A = +25°C		±10	±13	–	±10	±13	–	
$R_L \geqslant 75$ kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$		±10	–	–	±10	–	–	
Input Voltage Range	V_{ID}							V
$T_{low} \leqslant T_A \leqslant T_{high}$		±10	–	–	±10	–	–	
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leqslant 10$ kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$		70	90	–	70	90	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leqslant 10$ kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$		–	25	150	–	25	200	

*T_{low} = -55°C for MC1776
0°C for MC1776C

T_{high} = +125°C for MC1776
+70°C for MC1776C

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TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

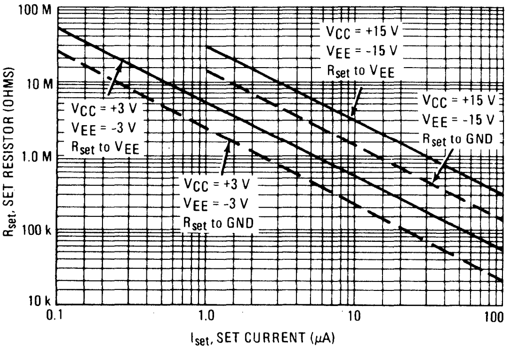


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

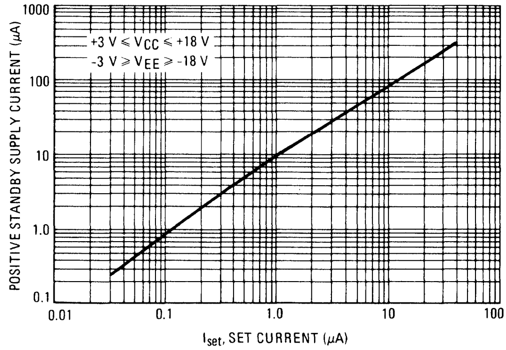


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

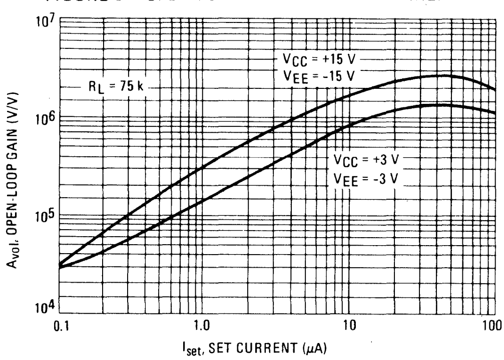


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

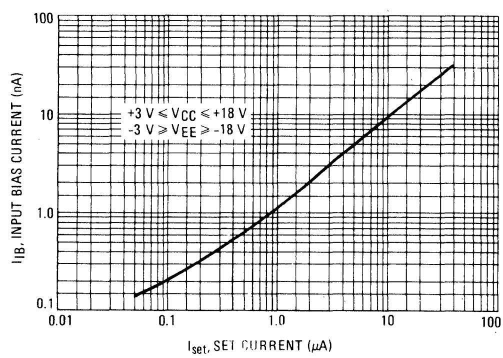


FIGURE 5 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

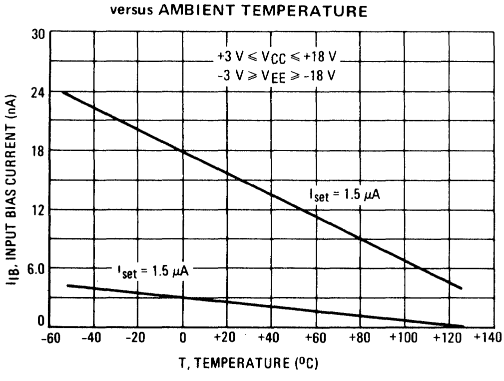
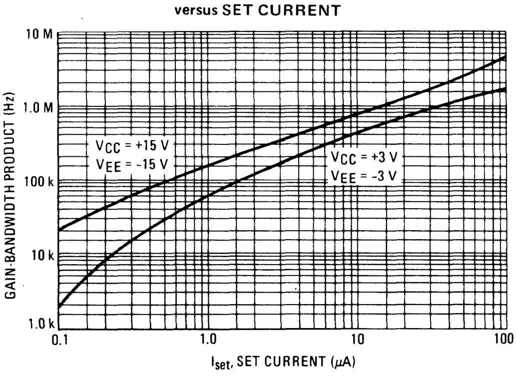


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



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TYPICAL CHARACTERISTICS (continued)

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

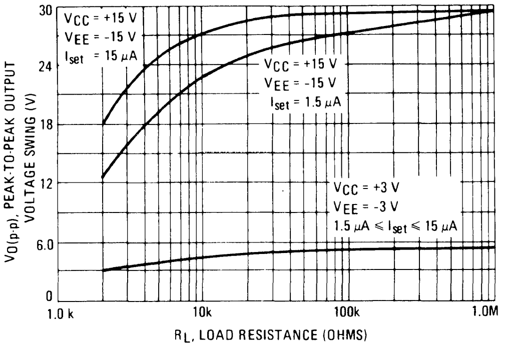


FIGURE 8 – SUPPLY CURRENT versus AMBIENT TEMPERATURE

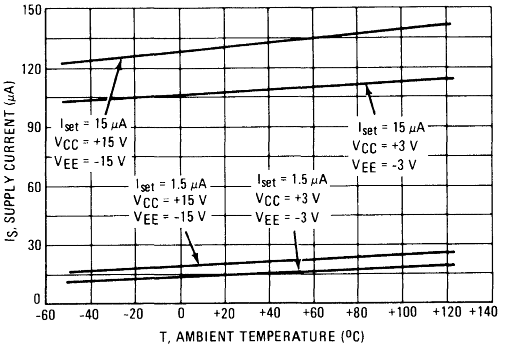


FIGURE 9 – OUTPUT SWING versus SUPPLY VOLTAGE

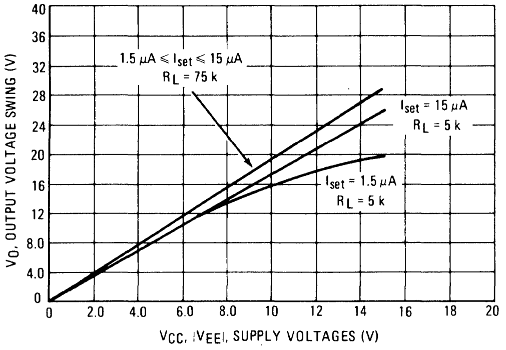


FIGURE 10 – SLEW RATE versus SET CURRENT

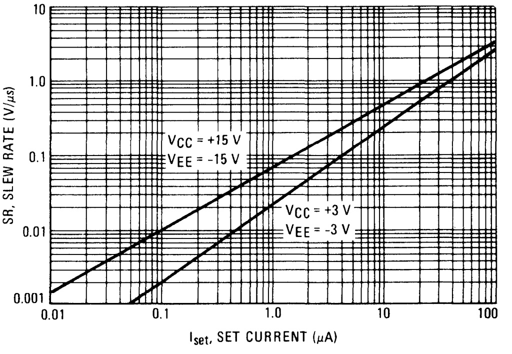


FIGURE 11 – INPUT NOISE VOLTAGE versus SET CURRENT

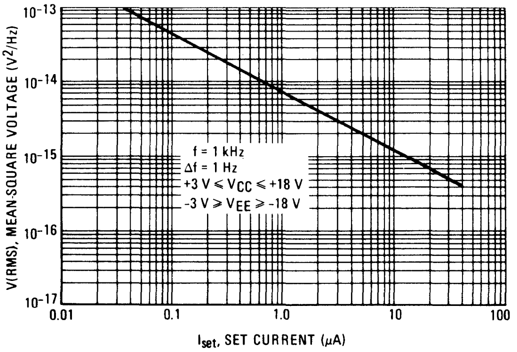
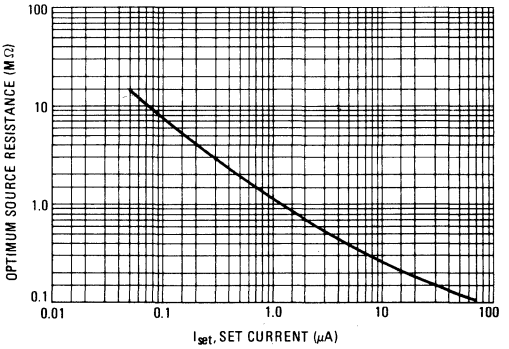


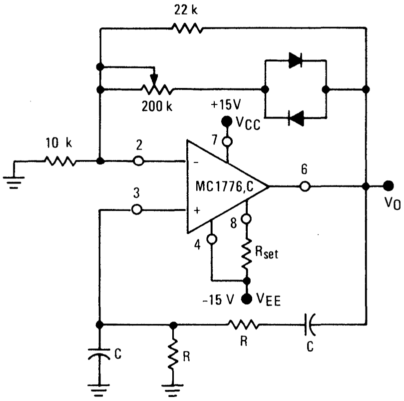
FIGURE 12 – OPTIMUM SOURCE RESISTANCE FOR MINIMUM NOISE versus SET CURRENT



8

APPLICATIONS INFORMATION

FIGURE 13 – WEIN BRIDGE OSCILLATOR

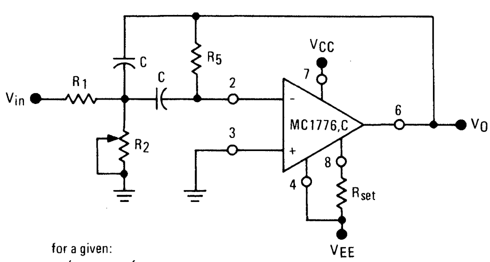


$$f_o = \frac{1}{2\pi RC}$$

(for f_o = 1.0 kHz)

R = 16 kΩ
C = 0.01 μF

FIGURE 14 – MULTIPLE FEEDBACK BANDPASS FILTER



for a given:
- f_o = center frequency
- A (f_o) = Gain at center frequency
- Q = quality factor

Choose a value for C, then

$$R_5 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R5}{2A\,(f_o)}$$

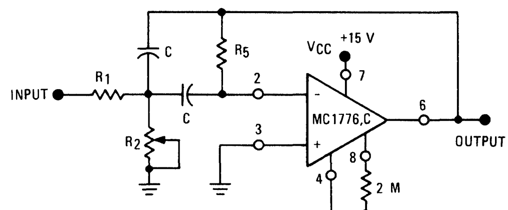
$$R2 = \frac{R1 R5}{4Q^2\,R1 - R5}$$

To obtain less than 10% error from the operational amplifier:

$$\frac{Q_o\,f_o}{GBW} \leq 0.1$$

where f_o and GBW are expressed in Hz. GBW is available from Figure 6 as a function of Set Current, I_{set}.

FIGURE 15 – MULTIPLE FEEDBACK BANDPASS FILTER (1.0 kHz)



for a 1.0 kHz filter with Q = 10 and A (f_o) = 1

R_1 = 160 k
R_2 = 820
R_5 = 300 k
C = 0.01 μF

FIGURE 16 – GATED AMPLIFIER

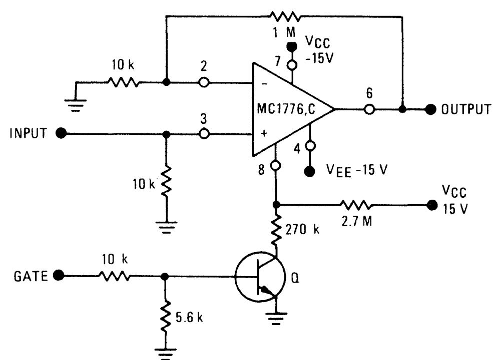
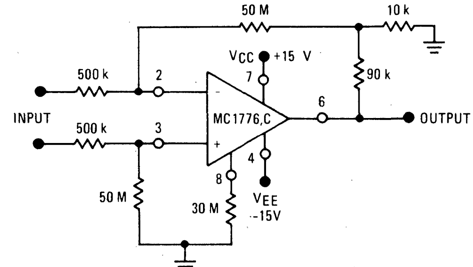


FIGURE 17 – HIGH INPUT IMPEDANCE AMPLIFIER



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MC3301P

OPERATIONAL AMPLIFIER

MONOLITHIC QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER FOR AUTOMOTIVE APPLICATIONS

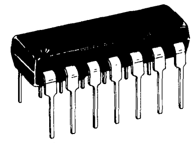
These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in automotive and consumer electronics. Each MC3301P contains four independent amplifiers – making it ideal for automotive safety, pollution, and comfort controls. Some typical applications are tachometer, voltage regulator, logic circuits, power control and other similar usages.

- Wide Operating Temperature Range – -40 to +85°C
- Single-Supply Operation – +4.0 to +28 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth – 4.0 MHz typical
- Low Input Bias Current – 50 nA typical
- High Open-Loop Gain – 2000 V/V typical

MONOLITHIC QUAD OPERATIONAL AMPLIFIER

INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED



PLASTIC PACKAGE
CASE 646

FIGURE 1 – EQUIVALENT CIRCUIT

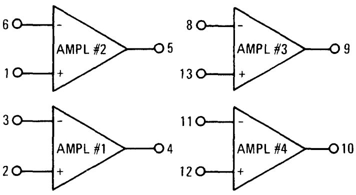


FIGURE 2 – SMALL-SIGNAL TRANSIENT RESPONSE

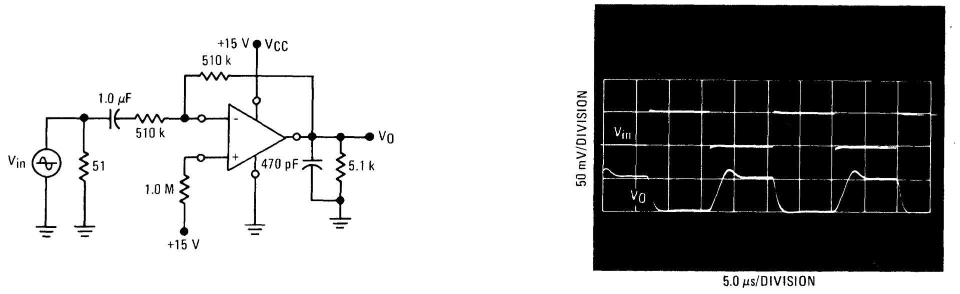


FIGURE 3 – INVERTING AMPLIFIER

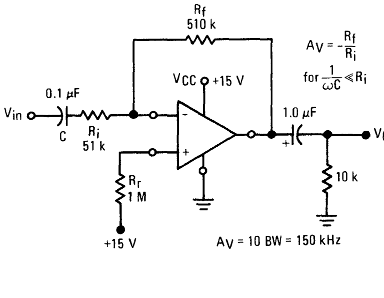
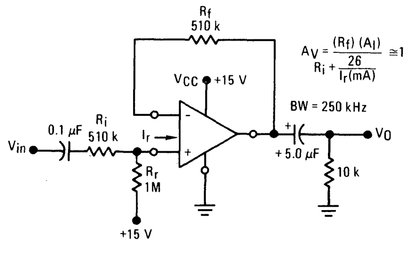


FIGURE 4 – NONINVERTING AMPLIFIER



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+28	Vdc
Noninverting Input Current	I_r	5.0	mA
Sink Current	I_{sink}	50	mA
Source Current	I_{source}	50	mA
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS [V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C (each amplifier) unless otherwise noted]

Characteristic	Fig.No.	Note	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain T_A = +25°C -40°C ⩽ T_A ⩽ +85°C	5		A_{vol}	 1000 –	 2000 1600	 – –	V/V
Quiescent Power Supply Current (Total for four amplifiers) Noninverting inputs open Noninverting inputs grounded	6	1	 I_{DO} I_{DG}	 – –	 6.9 7.8	 10 14	mAdc
Input Bias Current, R_L = ∞ T_A = +25°C -40°C ⩽ T_A ⩽ +85°C	7	2	I_{IB}	 – –	 50 100	 300 –	nAdc
Current Mirror Gain (I_r = 200 μAdc)	7	3	A_I	0.80	0.98	1.16	A/A
Current Mirror Gain Drift -40°C ⩽ T_A ⩽ +85°C				 –	 ±2.5	 –	%
Output Current Source Capability (V_{OH} = 0.4 Vdc) (V_{OH} = 9.0 Vdc) Sink Capability (V_{OL} = 0.4 Vdc)	8		 I_{source} I_{sink}	 3.0 – 0.5	 10 7.0 0.87	 – – –	mAdc
Output Voltage High Voltage Low Voltage (Inverting Input Driven) (Noninverting Input Driven)	6		 V_{OH} $V_{OL(inv)}$ $V_{OL(non)}$	 13.5 – –	 14.2 0.03 0.6	 – 0.1 –	Vdc
Input Resistance (Inverting input only)			R_{in}	0.1	1.0	–	Meg Ω
Slew Rate (C_L = 100 pF, R_L = 5.0 k)			SR	–	0.6	–	V/μs
Unity Gain Bandwidth		4	BW	–	4.0	–	MHz
Phase Margin		4	φm	–	70	–	Degrees
Power Supply Rejection (f = 100 Hz)			PSSR	–	55	–	dB
Channel Separation (f = 1.0 kHz)			e_{o1}/e_{o2}	–	65	–	dB

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NOTES:

1. The quiescent current drain will increase approximately 0.3 mA for each inverting or noninverting input that is grounded.
2. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" – as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
3. Current mirror gain is defined as the current demanded at the inverting input divided by the current into the noninverting input.
4. Bandwidth and phase margin are defined with respect to the voltage gain from the inverting input to the output.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 5 – OPEN-LOOP VOLTAGE GAIN

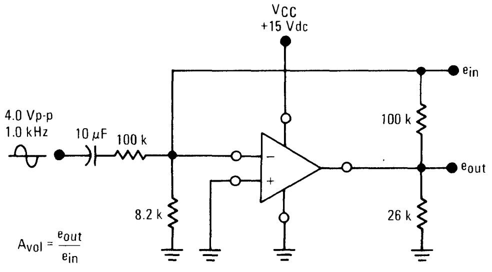


FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT

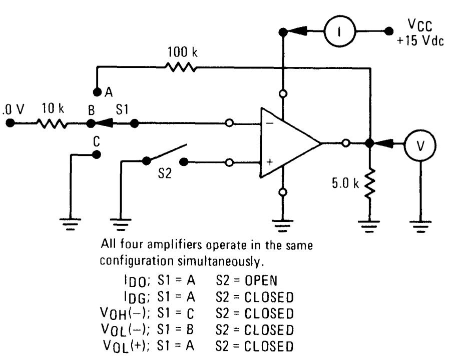


FIGURE 7 – INPUT BIAS CURRENT AND CURRENT MIRROR GAIN

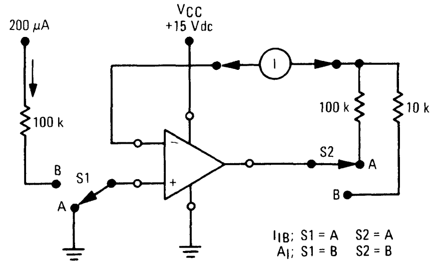
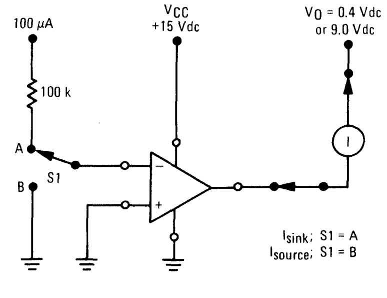


FIGURE 8 – OUTPUT CURRENT



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TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C [each amplifier] unless otherwise noted.)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

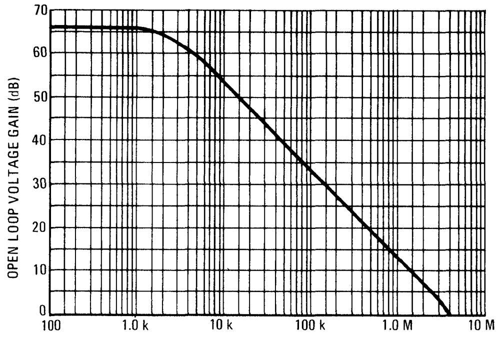


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

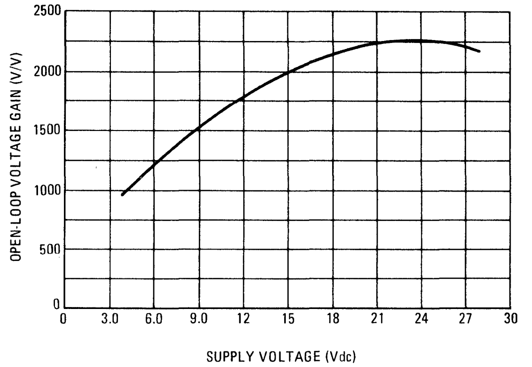


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

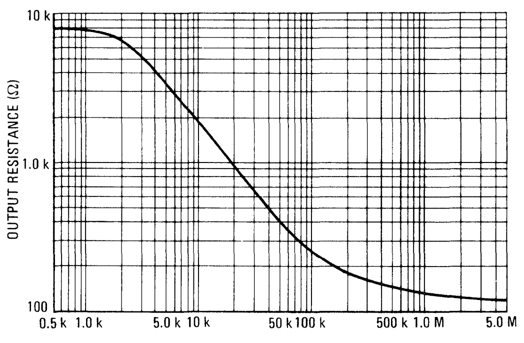


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

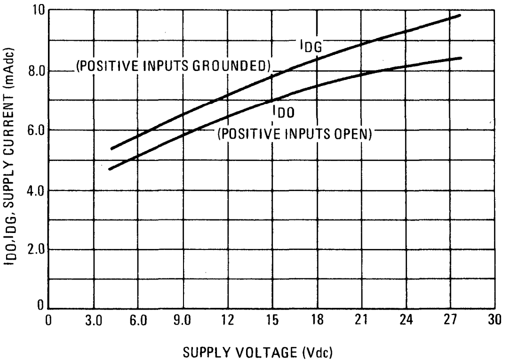


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

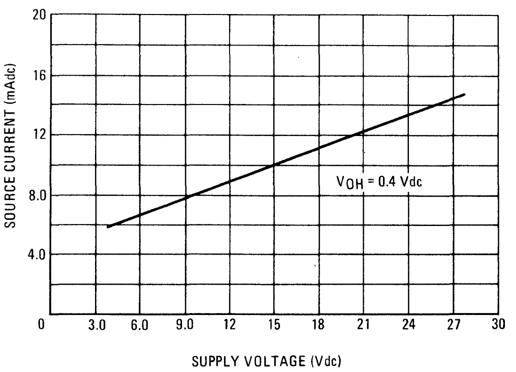
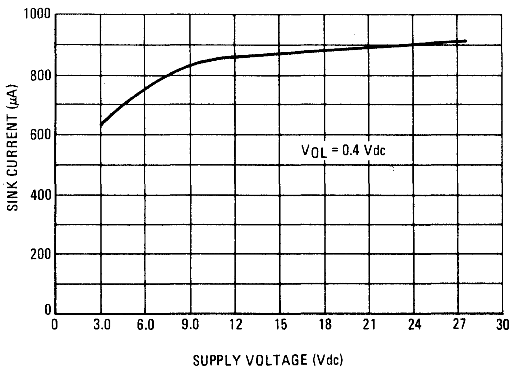


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE



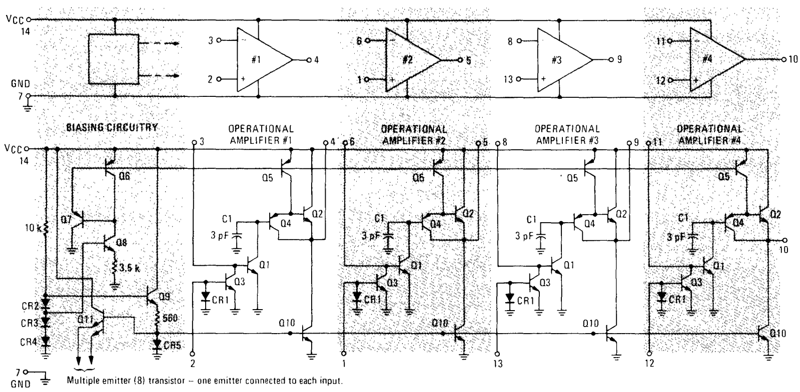
(MC3301–Page 4)

OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 volt resulting in an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18 on the following page. No external compensation is required.

FIGURE 15
BLOCK DIAGRAM



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the noninverting input, I_r, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_r. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to I_r also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 16 – A BASIC GAIN STAGE

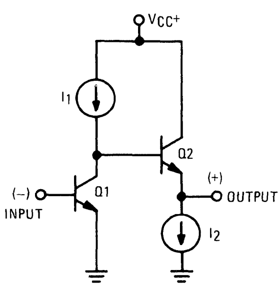
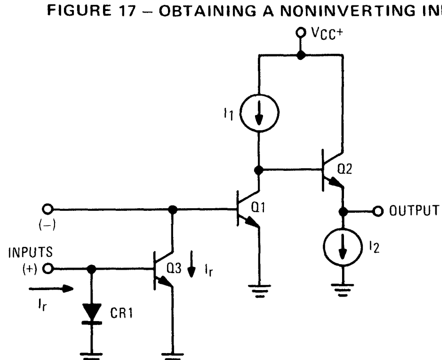


FIGURE 17 – OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19, see next page. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 15) provides circuit protection from signals that are negative with respect to ground.

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OPERATION AND APPLICATIONS (continued)

FIGURE 18 – A BASIC OPERATIONAL AMPLIFIER

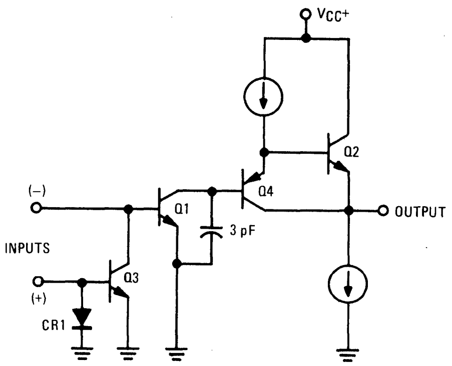
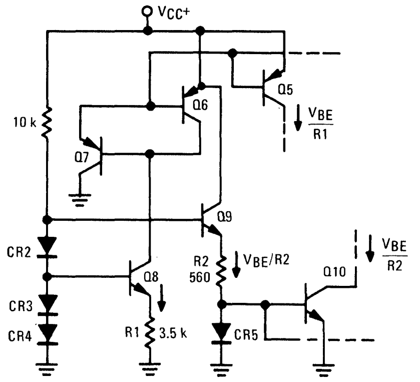


FIGURE 19 – BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing

   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4 (see the first page of this specification). The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μA to 200 μA range.

   B. V_{CC} Reference Voltage (see Figures 3 and 4)

   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 10 μA to 200 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows the maximum dynamic range of the output voltage.

   C. Reference Voltage other than V_{CC} (see Figure 20)

   The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f \doteq R_r$, (still keeping I_r between 10 μA and 200 μA) the output dc level will be equal to V_r. The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_I)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_I\right) \phi$$

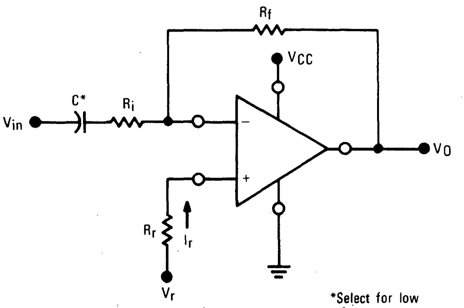
   where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_I is the current mirror gain.

2. Gain Determination

   A. Inverting Amplifier

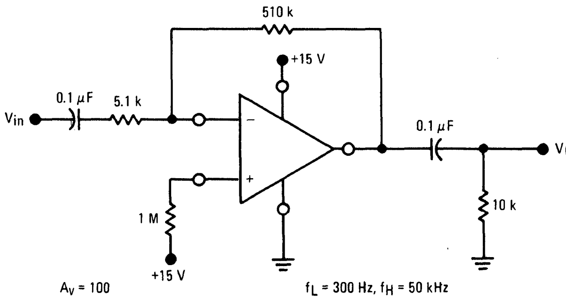
   The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

FIGURE 20 – INVERTING AMPLIFIER WITH ARBITRARY REFERENCE



*Select for low frequency response.

FIGURE 21 – INVERTING AMPLIFIER WITH A_v = 100 AND V_r = V_{CC}



NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_V = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 4.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 400 kHz with 20 dB of closed loop gain or 40 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

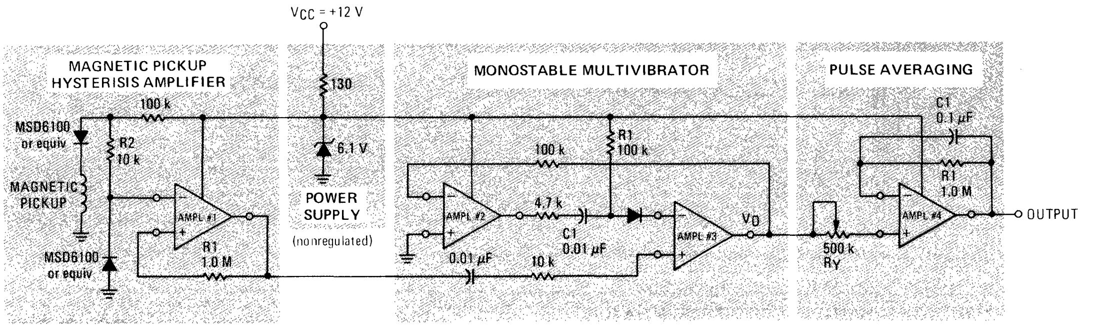
The MC3301P may be used in the noninverting mode (see Figure 4, first page). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting ac gain expression is given by:

$$A_V = \frac{(R_f)(A_I)}{R_i + \dfrac{26}{I_r\ (mA)}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 22 – TACHOMETER CIRCUIT



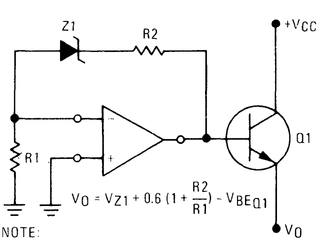
Hysterisis Voltage for Switching

$$V_H = \frac{A_I R2}{R1}\ (V_{CC} - 1.6)$$

Timing Interval: $t \approx 0.7\ R1\ C1$

$$V_{p\text{-}p} \cong \frac{(V_O - 0.6) \cdot A_I \cdot t}{R_Y C1}$$

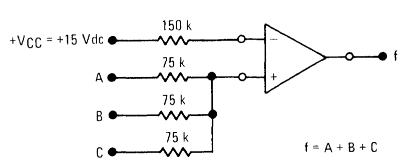
FIGURE 23 – VOLTAGE REGULATOR



$$V_O = V_{Z1} + 0.6\left(1 + \frac{R2}{R1}\right) - V_{BEQ1}$$

NOTE:
For positive T_C zeners R2 and R1 can be selected to give 0 T_C output.

FIGURE 24 – LOGIC "OR" GATE



f = A + B + C

(MC3301–Page 7)

TYPICAL APPLICATIONS (continued)

FIGURE 25 – LOGIC "NAND" GATE (Large Fan-In)

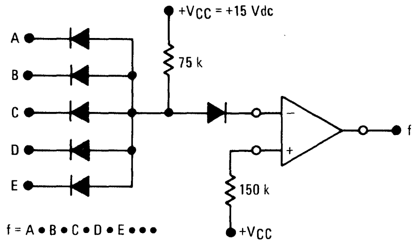


FIGURE 26 – LOGIC "NOR" GATE

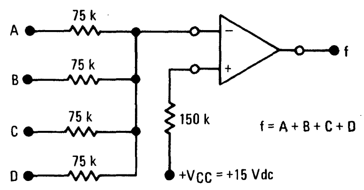


FIGURE 27 – R-S FLIP-FLOP

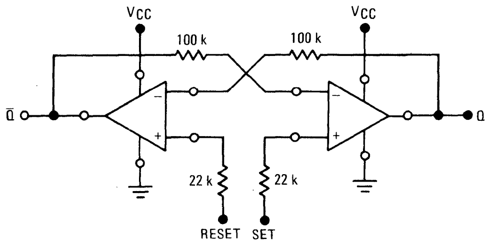


FIGURE 28 – ASTABLE MULTIVIBRATOR

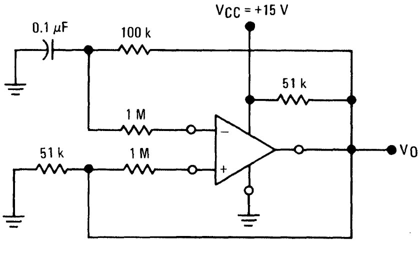


FIGURE 29 – POSITIVE-EDGE DIFFERENTIATOR

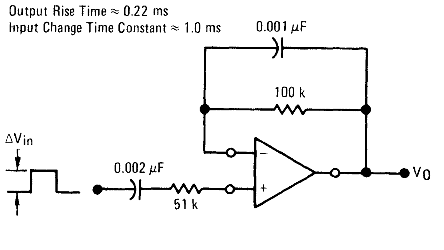
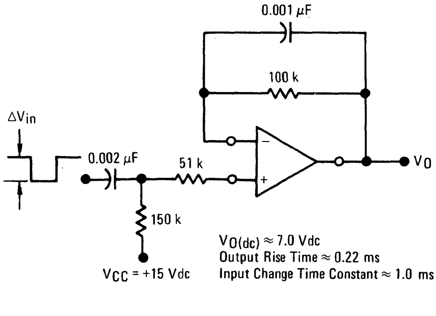


FIGURE 30 – NEGATIVE-EDGE DIFFERENTIATOR



8

MC3302P

QUAD COMPARATOR

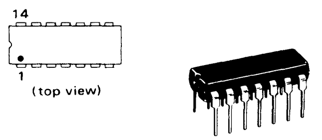
MONOLITHIC QUAD SINGLE-SUPPLY COMPARATOR

These comparators are designed specifically for single positive-power-supply Consumer Automotive and Industrial electronic applications. Each MC3302P contains four independent comparators – suiting it ideally for usages requiring high density and low-cost.

- Wide Operating Temperature Range – -40 to +85°C
- Single-Supply Operation – +2.0 to +28 Vdc
- Differential Input Voltage = $\pm V_{CC}$
- Compare Voltages at Ground Potential
- MTTL Compatible
- Low Current Drain – 700 μA typical @ V_{CC} +5.0 to +28 Vdc
- Outputs can be Connected to Give the Implied AND Function

MONOLITHIC QUAD COMPARATOR INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED



PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Range	V_{CC}	+2.0 to +28	Vdc
Output Sink Current (See Note 1)	I_O	20	mA
Differential Input Voltage	V_{IDR}	$\pm V_{CC}$	Vdc
Common-Mode Input Voltage Range (See Note 2)	V_{ICR}	-0.3 to $+V_{CC}$	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. Requires an external resistor, R_L, to limit current below maximum rating.

Note 2. If either (+) or (–) inputs of any comparator go more than several tenths of a volt below ground, a parasitic transistor turns "on" causing high input current and possible faulty outputs.

FIGURE 1 – EQUIVALENT CIRCUIT

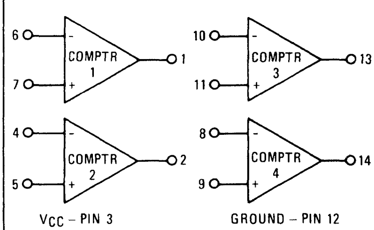
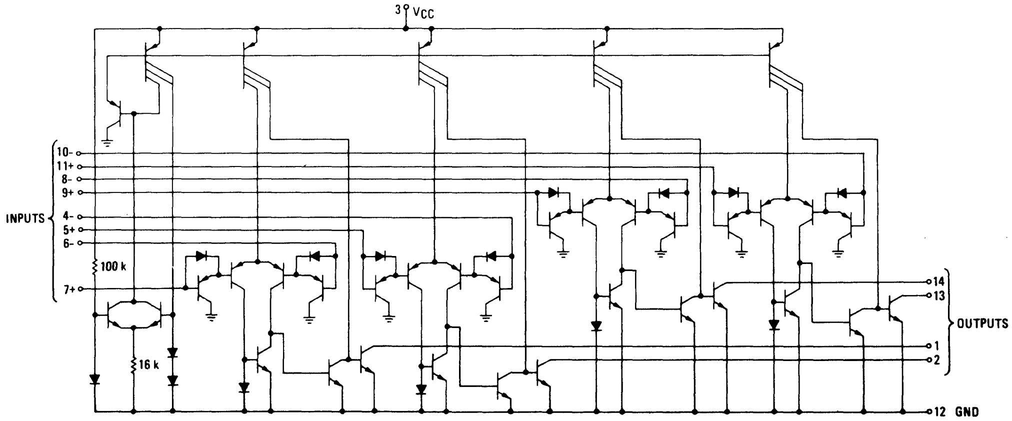


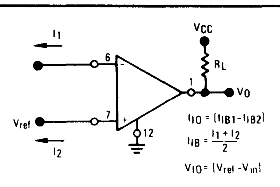
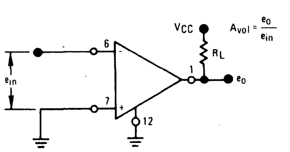
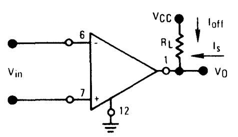
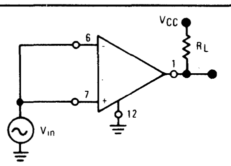
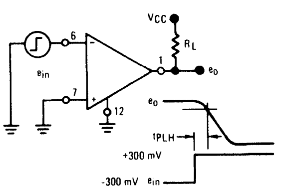
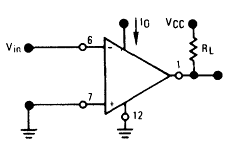
FIGURE 2 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Characteristic Definitions (1/4 Circuit Shown)	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage (V_{ref} = 1.2 Vdc) (T_A = +25°C) (T_A = -40 to +85°C)	V_{IO}	 – –	 3.0 –	 20 40	mVdc
	Input Offset Current	I_{IO}	–	3.0	–	nAdc
	Input Bias Current (T_A = +25°C) (T_A = -40 to +85°C)	I_{IB}	 – –	 30 –	 500 1000	nAdc
	Voltage Gain (T_A = +25°C, R_L = 15 kΩ)	A_{vol}	 2,000	 30,000	 –	V/V
	Transconductance	gm	–	2.0	–	mhos
	Differential Input Voltage Range	V_{IDR}	$\pm V_{CC}$	–	–	Vdc
	Output Leakage Current (Output Voltage High)	I_{off}	 –	 –	 1.0	μAdc
	Negative Output Voltage (I_s = 2.0 mA, V_{CC} = +5.0 to +28 Vdc)	V_{OL}	 –	 150	 400	mVdc
	Output Sink Current (V_{CC} = +5.0 Vdc) (T_A = +25°C, V_{OL} = 400 mV) (T_A = -40 to +85°C, V_{OL} = 800 mV)	I_s	 – 2.0	 6.0 –	 – –	mAdc
	Input Common-Mode Range (V_{CC} = +28 Vdc)	V_{ICR}	 0-26	 –	 –	Volts
	Common-Mode Rejection Ratio	CMRR	–	60	–	dB
	Propagation Delay Time For Positive and Negative-Going Input Pulse	$t_{PHL/LH}$	–	2.0	–	μs
	Slew Rate (R_L = 15 kΩ)	$t_{SR}-$ $t_{SR}+$	– –	200 50	– –	V/μs
	Power Supply Current (Total of four comparators) (I_s = 0, V_{CC} = +5.0 to +28 Vdc)	I_D	 –	 0.7	 1.5	mAdc

8

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

FIGURE 3 – INPUT OFFSET VOLTAGE

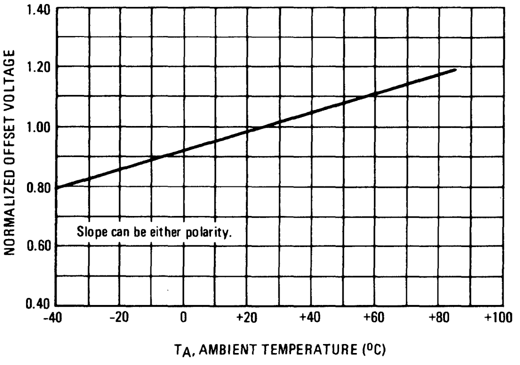


FIGURE 4 – OFFSET BIAS CURRENT

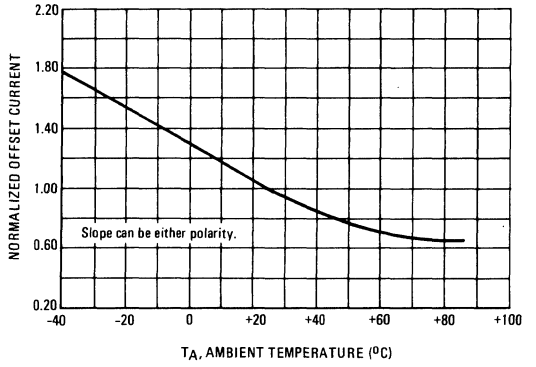
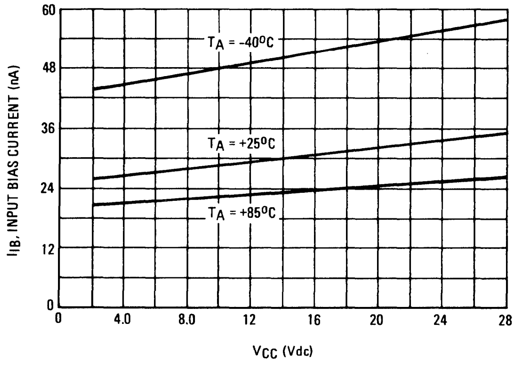


FIGURE 5 – INPUT BIAS CURRENT



TYPICAL APPLICATIONS

FIGURE 6 – FREE-RUNNING SQUARE-WAVE OSCILLATOR

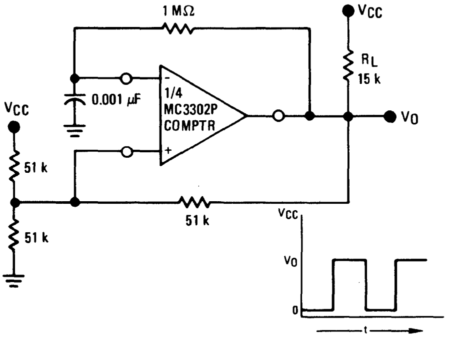
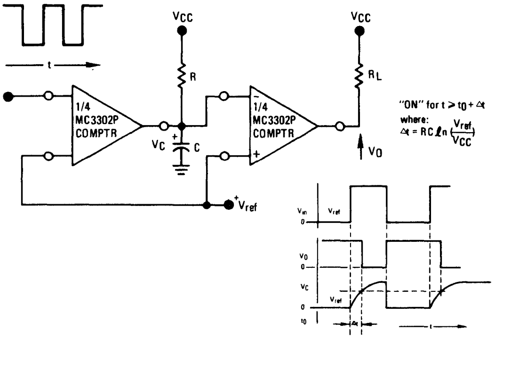
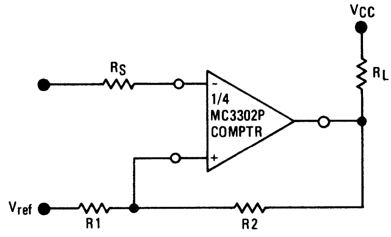


FIGURE 7 – TIME DELAY GENERATOR



TYPICAL APPLICATIONS (continued)

FIGURE 8 – COMPARATOR WITH HYSTERESIS

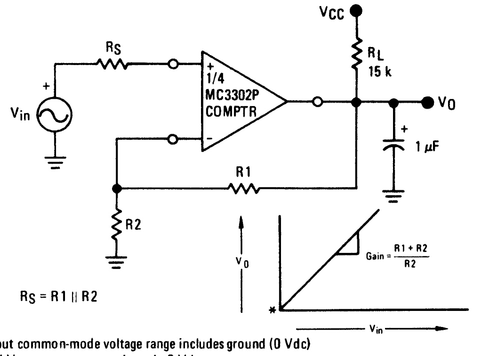


$R_S = R1 \parallel R2$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\,R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{O}\ \text{Low})\,R1}{R1 + R2 + R_L}$$

FIGURE 9 – THE COMPARATOR AS AN OPERATIONAL AMPLIFIER



$R_S = R1 \parallel R2$

*Input common-mode voltage range includes ground (0 Vdc) and V_O can go to approximately 0 Vdc.

8

MC3401P

OPERATIONAL AMPLIFIERS

Specifications and Applications Information

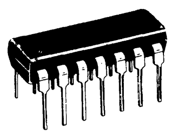
MONOLITHIC QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER

These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each MC3401P device contains four independent amplifiers – making it ideal for applications such as active filters, multi-channel amplifiers, tachometer, oscillator and other similar usages.

- Single-Supply Operation – +5.0 Vdc to +18 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth – 5.0 MHz typical
- Low Input Bias Current – 50 nA typical
- High Open-Loop Gain – 1000 V/V minimum

MONOLITHIC QUAD OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED



PLASTIC PACKAGE
CASE 646

FIGURE 1 – EQUIVALENT CIRCUIT

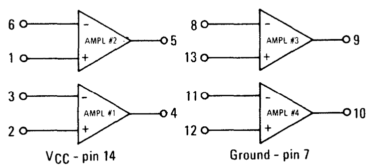
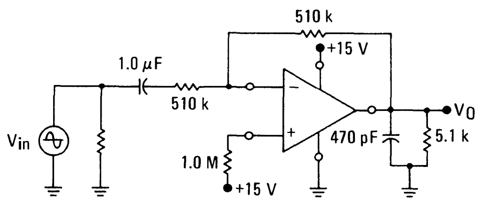


FIGURE 2 – SMALL-SIGNAL TRANSIENT RESPONSE



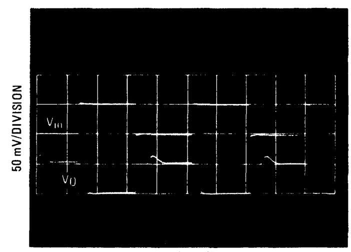


FIGURE 3 – INVERTING AMPLIFIER

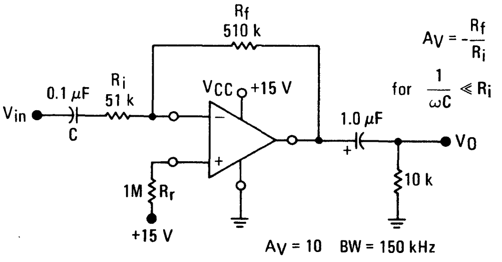
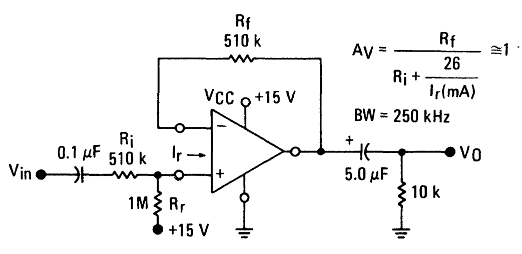


FIGURE 4 – NONINVERTING AMPLIFIER



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Non-inverting Input Current	I_{in}	5.0	mA
Power Dissipation Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS [V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C (each amplifier) unless otherwise noted.]

Characteristic	Fig. No.	Note	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain T_A = +25°C 0°C ≤ T_A ≤ +75°C	5,9,10	1	A_{vol}	 1000 800	 2000 –	 – –	V/V
Quiescent Power Supply Current (Total for four amplifiers) Noninverting inputs open Noninverting inputs grounded	6,12	2	 I_{DO} I_{DG}	 – –	 6.9 7.8	 10 14	mAdc
Input Bias Current, R_L = ∞ T_A = +25°C 0°C ≤ T_A ≤ +75°C	5	3	I_{IB}	 – –	 50 –	 300 500	nAdc
Output Current Source Capability Sink Capability	5 13 14	4	 I_{source} I_{sink}	 5.0 0.5	 10 1.0	 – –	mAdc
Output Voltage High Voltage Low Voltage Undistorted Output Swing (0°C < T_A < +75°C)	 7 7 8	 5 5 6	 V_{OH} V_{OL} $V_{O(p-p)}$	 13.5 – 10	 14.2 0.03 13.5	 – 0.1 –	Vdc $V_{(p-p)}$
Input Resistance	5		R_{in}	0.1	1.0	–	MEG Ω
Slew Rate (C_L = 100 pF, R_L = 5.0 k)			SR	–	0.6	–	V/µs
Unity Gain Bandwidth			BW	–	5.0	–	MHz
Phase Margin			ϕ_m	–	70	–	Degrees
Power Supply Rejection (f = 100 Hz)		7	PSSR	–	55	–	dB
Channel Separation (f = 1.0 kHz)			e_{o1}/e_{o2}	–	65	–	dB

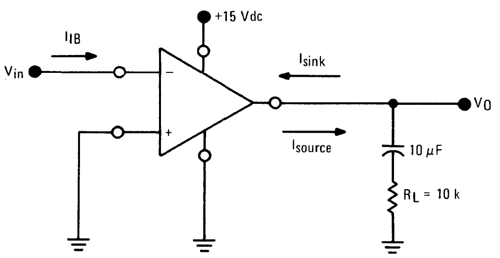
NOTES

1. Open loop voltage gain is defined as the voltage gain from the inverting input to the output.
2. The quiescent current will increase approximately 0.3 mA for each noninverting input which is grounded. Leaving the noninverting input open causes the apparent input bias current to increase slightly (100 nA) at high temperatures.
3. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" – as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
4. Sink current is specified for linear operation. When the device is used as a gate or a comparator (non-linear operation), the sink capability of the device is approximately 5.0 milliamperes.
5. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.
6. Peak-to-peak restrictions are due to the variations of the quiescent dc output voltage in the standard configuration (Figure 8).
7. Power supply rejection is specified at closed loop unity gain, and therefore indicates the supply rejection of both the biasing circuitry and the feedback amplifier.

SIMPLIFIED TEST CIRCUITS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted)

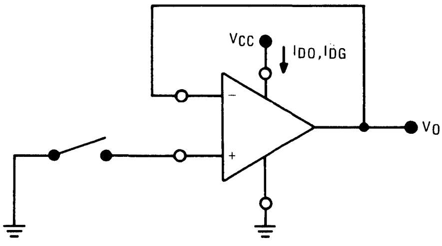
FIGURE 5 – OPEN-LOOP GAIN AND INPUT RESISTANCE (INPUT BIAS CURRENT, OUTPUT CURRENT)



$R_{in} = \frac{\Delta V_{in}}{\Delta I_{IB}}$ $A_{vol} = -\frac{\Delta V_O}{\Delta V_{in}}$

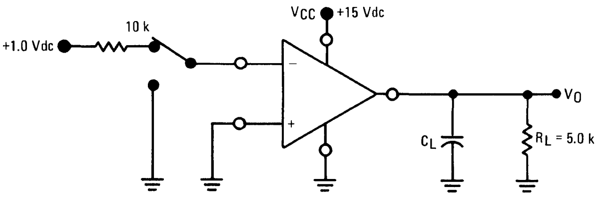
Amplifier must be biased (by V_{in}) in the linear operating region.

FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT



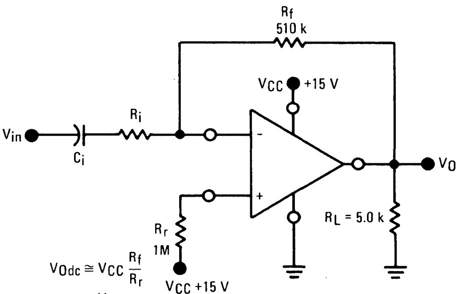
I_{DO} is total supply current with "+" input open.
I_{DG} is total supply current with "+" input grounded.

FIGURE 7 – OUTPUT VOLTAGE SWING



V_{OL} measured with "–" input biased up as shown.
V_{OH} measured with "–" input grounded.

FIGURE 8 – PEAK-TO-PEAK OUTPUT VOLTAGE



$V_{Odc} \cong V_{CC}\frac{R_f}{R_r}$

$\cong \frac{V_{CC}}{2}$

for $R_r \cong 2R_f$

8

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C [each amplifier] unless otherwise noted.)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

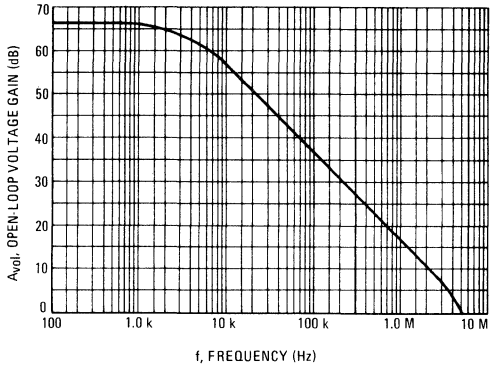


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

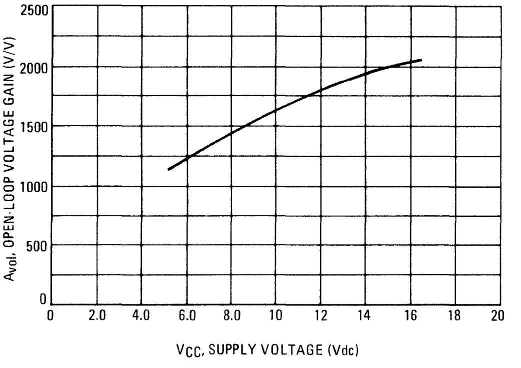


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

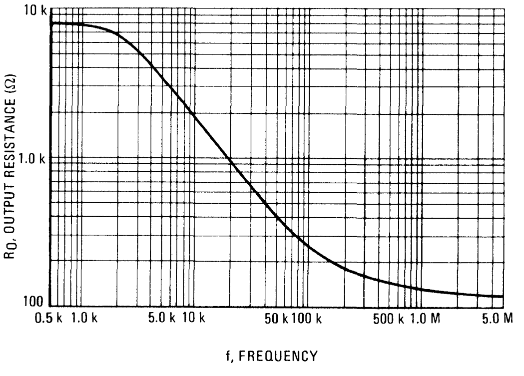


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

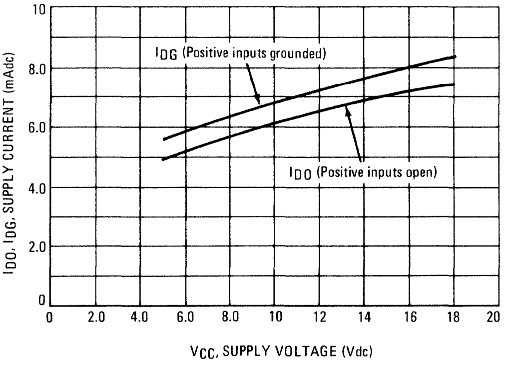


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

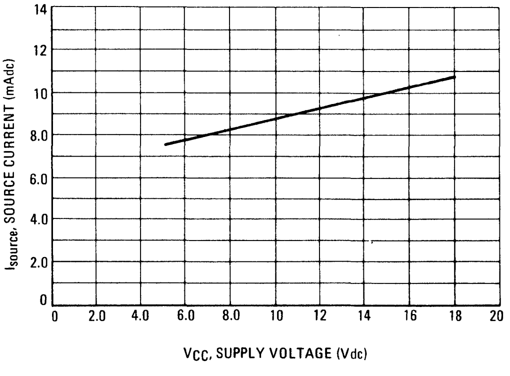
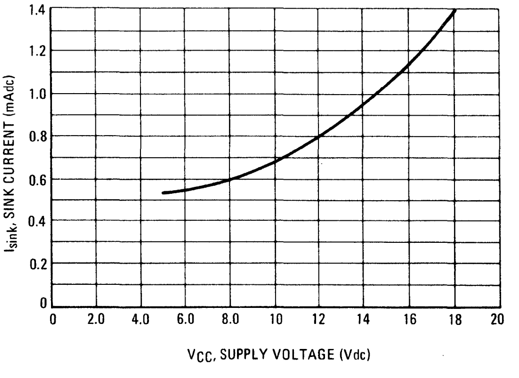


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE



8

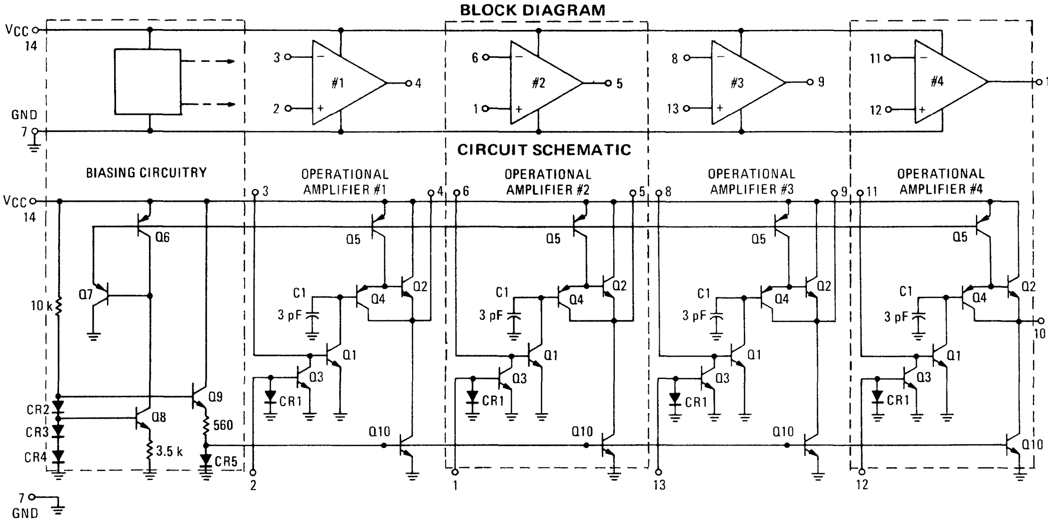
OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level with an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18. No external compensation is required.

FIGURE 15

BLOCK DIAGRAM



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the noninverting input, I_{in2}, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in2}. Since the alpha current gain of Q3 $\approx$ 1, its collector current $\approx I_{in2}$ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 16 – A BASIC GAIN STAGE

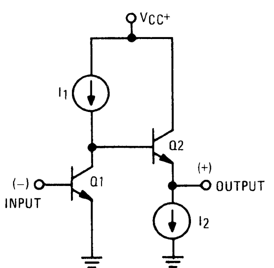
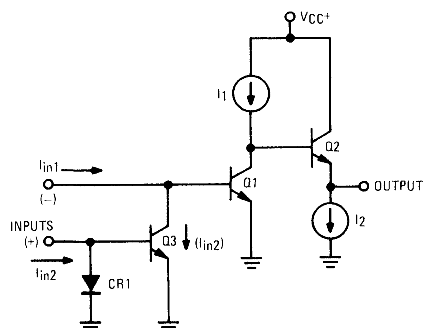


FIGURE 17 – OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude V_{BE}/R1 by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage.

OPERATION AND APPLICATIONS (continued)

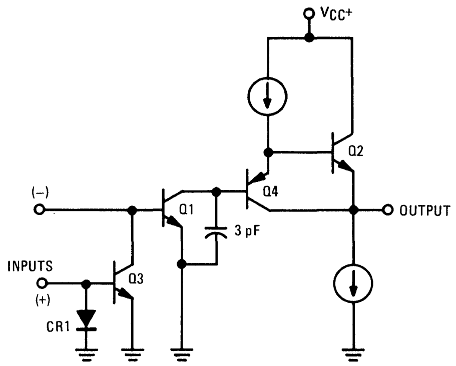


FIGURE 18 – A BASIC OPERATIONAL AMPLIFIER

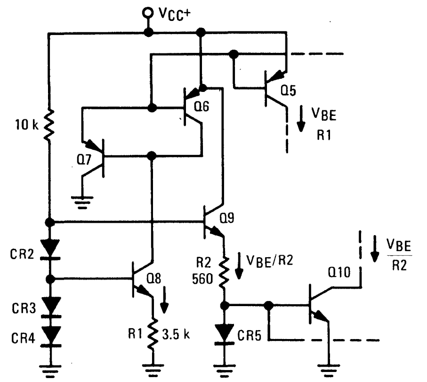


FIGURE 19 – BIASING CIRCUITRY

NORMAL DESIGN PROCEDURE

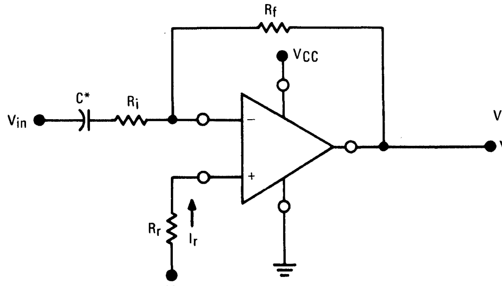
1. Output Q-Point Biasing
   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4. The high impedance of the collector of the non-inverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 5 μA to 100 μA range.
   B. V_{CC} Reference Voltage (see Figures 3 and 4)
   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 5 μA to 100 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows for maximum dynamic range of the output voltage.
   C. Reference Voltage other than V_{CC} (See Figure 20).
   The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_r between 5 μA and 100 μA) the output dc level will be equal to V_r. Neglecting error terms, the expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(V_r)\ (R_f)}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0.7 Vdc @ +25°C).

   The error terms not appearing in the above equation can cause the dc operating point to vary up to 20% from the expected value. Error terms are minimized by setting the input current within the range of 5 μA to 100 μA.
2. Gain Determination
   A. Inverting Amplifier
   The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

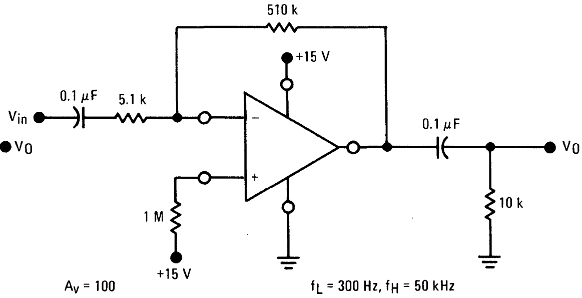
FIGURE 20 – INVERTING AMPLIFIER WITH ARBITRARY REFERENCE



$$V_O = \frac{V_r\,R_f}{R_r} + (1 - \frac{R_f}{R_r})\phi$$

*Select for low frequency response.

FIGURE 21 – INVERTING AMPLIFIER WITH $A_v = 100$ AND $V_r = V_{CC}$



NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_v = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 5.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 500 kHz with 20 dB of closed loop gain or 50 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

Although recommended as an inverting amplifier, the MC 3401P may be used in the noninverting mode (see Figure 4). The amplifier gain in this configuration is subject to the same error terms that affect the output Q point biasing so the gain may deviate as much as ±20% from that expected. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting gain expression is given by:

$$A_v = \frac{R_f}{R_i + \frac{26}{I_r\ (mA)}} \quad \pm 20\%.$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 22 – AMPLIFIER AND DRIVER FOR A 50-OHM LINE

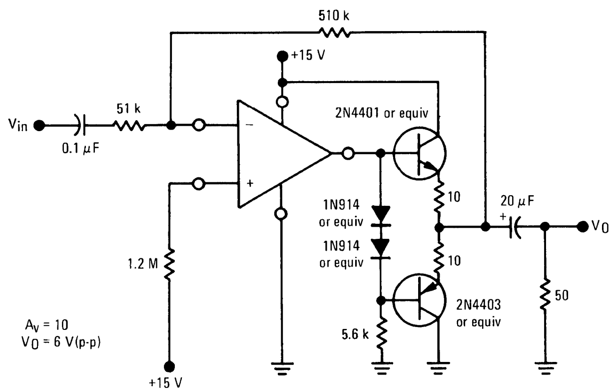
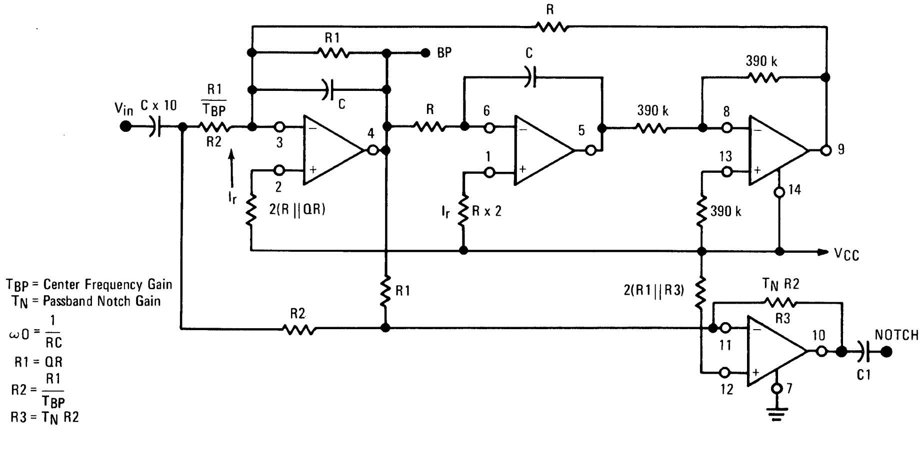


FIGURE 23 – BASIC BANDPASS AND NOTCH FILTER



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TYPICAL APPLICATIONS (continued)

FIGURE 24 — BANDPASS AND NOTCH FILTER

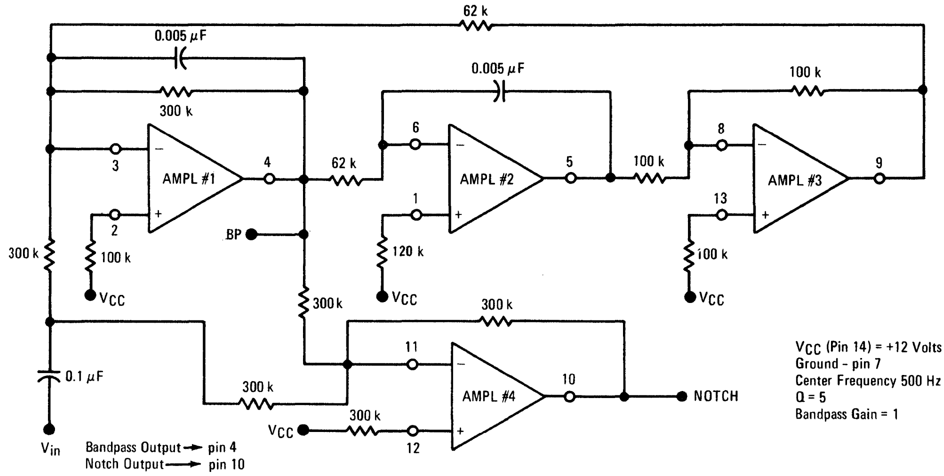
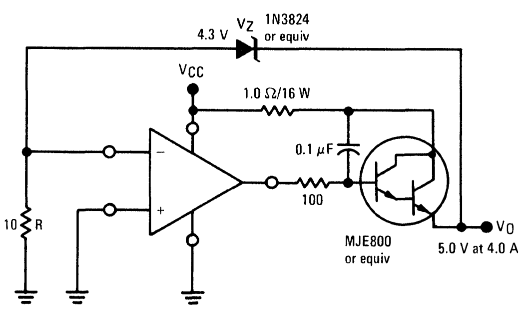


FIGURE 25 — VOLTAGE REGULATOR

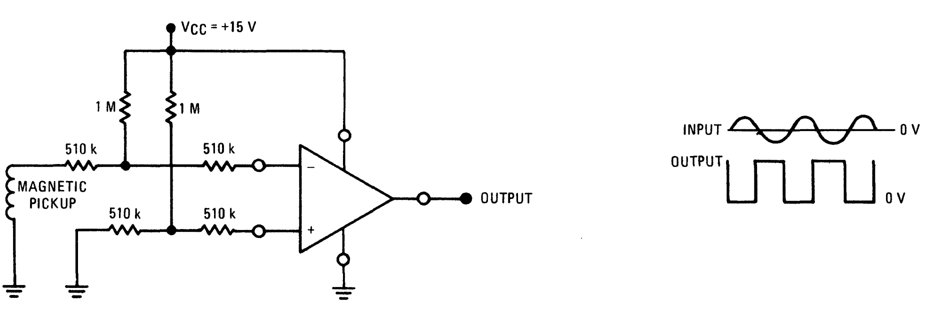


$V_O = V_Z + 0.6$ Vdc

NOTE 1: R is used to bias the zener.

NOTE 2: If the Zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈ 2.0 mV/°C), the output is zero-TC. A 7.0-Volt Zener will give approximately zero-TC.

FIGURE 26 — ZERO CROSSING DETECTOR



8

MC3450
MC3452

QUAD LINE RECEIVER

Specifications and Applications Information

MONOLITHIC QUAD MTTL COMPATIBLE LINE RECEIVERS

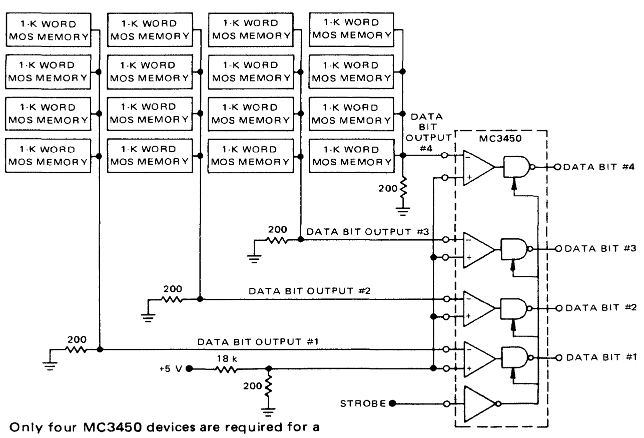
The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three-state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

The MC3452 is the same as the MC3450 except that the outputs are open collector which permits the implied "AND" function.

The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied "AND" Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier

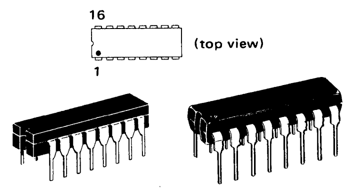
FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES



Only four MC3450 devices are required for a 4-k word by 16-bit memory system.

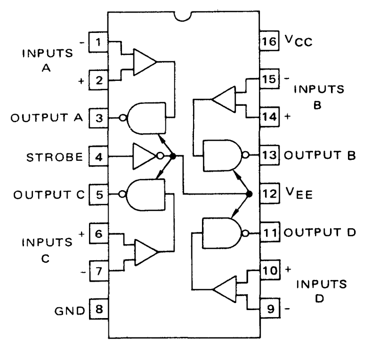
QUAD LINE RECEIVERS WITH COMMON THREE-STATE STROBE INPUT

MONOLITHIC SILICON INTEGRATED CIRCUITS



L SUFFIX CERAMIC PACKAGE CASE 620	P SUFFIX PLASTIC PACKAGE CASE 648

CONNECTION DIAGRAM



TRUTH TABLE

INPUT	STROBE	OUTPUT MC3450	OUTPUT MC3452
$V_{ID} \geq +25$ mV	L	H	Open
	H	Open	Open
-25 mV $\leq V_{ID} \leq +25$ mV	L	I	I
	H	Open	Open
$V_{ID} \leq -25$ mV	L	L	L
	H	Open	Open

L = Low Logic State
H = High Logic State
Open = High Impedance State
I = Indeterminate State

See Packaging Information Section for outline dimensions.

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MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Plastic Dual In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC}	+4.75	+5.0	+5.25	Vdc
	V_{EE}	-4.75	-5.0	-5.25	
Output Load Current	I_{OL}	–	–	16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	–	+3.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = 0 to +70°C unless otherwise noted.)

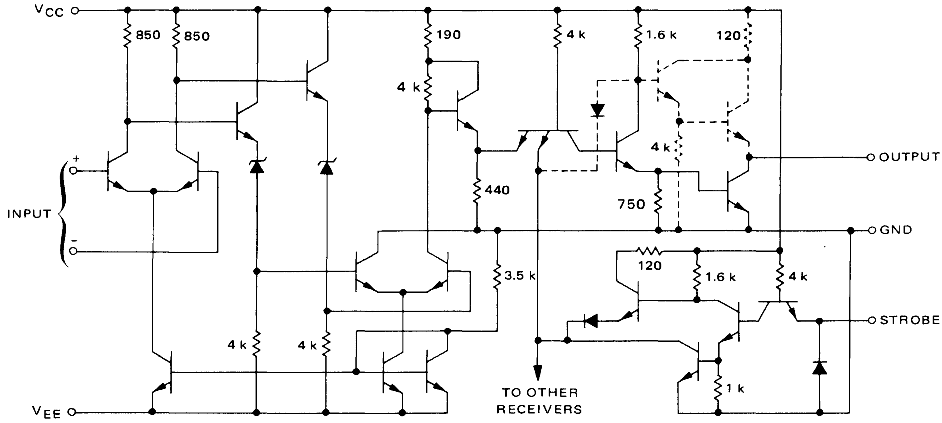
Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High Level Input Current to Receiver Input	$I_{IH(I)}$	7	–	–	75	–	–	75	µA
Low Level Input Current to Receiver Input	$I_{IL(I)}$	8	–	–	-10	–	–	-10	µA
High Level Input Current to Strobe Input	$I_{IH(S)}$	5							
$V_{IH(S)}$ = +2.4 V			–	–	40	–	–	40	µA
$V_{IH(S)}$ = +5.25 V			–	–	1.0	–	–	1.0	mA
Low Level Input Current to Strobe Input $V_{IH(S)}$ = +0.4 V	$I_{IL(S)}$	5	–	–	-1.6	–	–	-1.6	mA
High Level Output Voltage	V_{OH}	3	2.4	–	–	–	–	–	Vdc
High Level Output Leakage Current	I_{CEX}	3	–	–	–	–	–	250	µA
Low Level Output Voltage	V_{OL}	3	–	–	0.4	–	–	0.4	Vdc
Short-Circuit Output Current	I_{OS}	6	-18	–	-70	–	–	–	mA
Output Disable Leakage Current	I_{off}	9	–	–	40	–	–	–	µA
High Logic Level Supply Current from V_{CC}	I_{CCH}	4	–	45	60	–	45	60	mA
High Logic Level Supply Current from V_{EE}	I_{EEH}	4	–	-17	-30	–	-17	-30	mA

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs)	$t_{PHL(D)}$	10	–	–	25	–	–	25	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs)	$t_{PLH(D)}$	10	–	–	25	–	–	25	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{POH(S)}$	11	–	–	21	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHO(S)}$	11	–	–	18	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{POL(S)}$	11	–	–	27	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLO(S)}$	11	–	–	29	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	12	–	–	–	–	–	25	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	12	–	–	–	–	–	25	ns

8

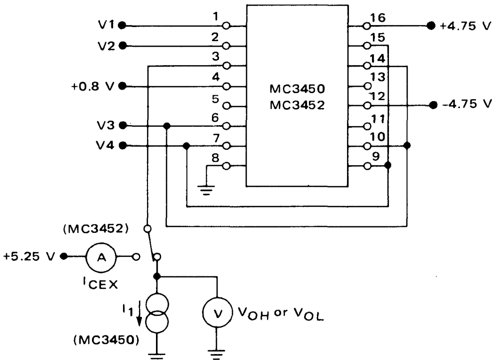
FIGURE 2 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



Dashed components apply to the MC3450 circuit only.

TEST CIRCUITS

FIGURE 3 – I_{CEX}, V_{OH}, AND V_{OL}



TEST TABLE

	V1		V2		V3		V4		
	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	I1
V_{OH}	+2.975 V	–	+3.0 V	–	+3.0 V	–	GND	–	+0.4 mA
	-3.0 V	–	-2.975 V	–	GND	–	-3.0 V	–	
I_{CEX}	–	+2.975 V	–	+3.0 V	–	+3.0 V	–	GND	–
	–	-3.0 V	–	-2.975 V	–	GND	–	-3.0 V	–
V_{OL}	+3.0 V	+3.0 V	+2.975 V	+2.975 V	GND	GND	+3.0 V	+3.0 V	-16 mA
	-2.975 V	-2.975 V	-3.0 V	-3.0 V	-3.0 V	-3.0 V	GND	GND	

Channel A shown under test. Other channels are tested similarly.

FIGURE 4 – I_{CCH} AND I_{EEH}

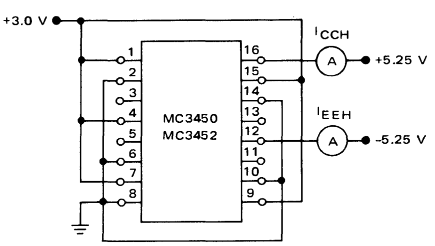
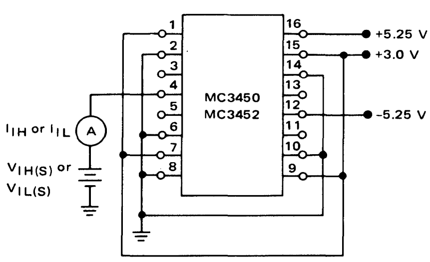


FIGURE 5 – $I_{IH(S)}$ AND $I_{IL(S)}$



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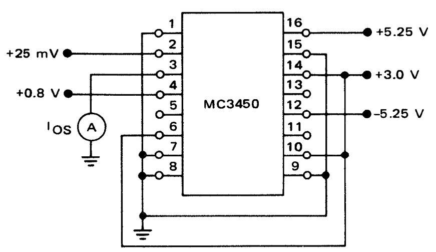
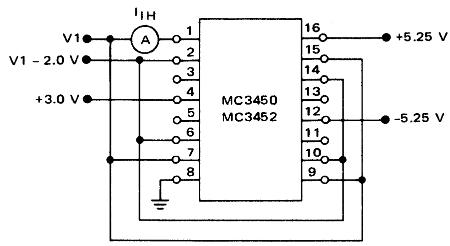
TEST CIRCUITS (continued)

FIGURE 6 – I_{OS}



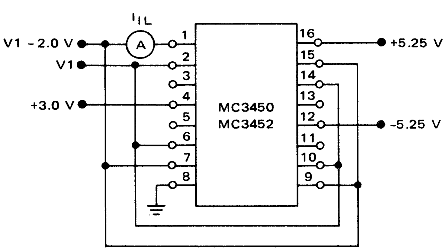
Channel A shown under test, other channels are tested similarly. Only one output shorted at a time.

FIGURE 7 – I_{IH}



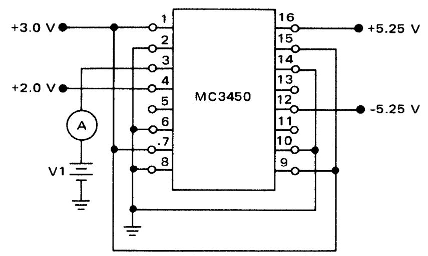
Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to –3.0 V.

FIGURE 8 – I_{IL}



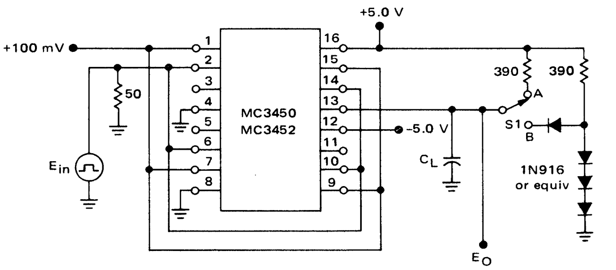
Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to -3.0 V.

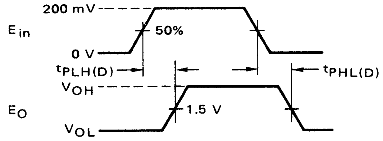
FIGURE 9 – I_{off}



Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4 V and +2.4 V.

FIGURE 10 – RECEIVER PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$





Output of Channel B shown under test, other channels are tested similarly.

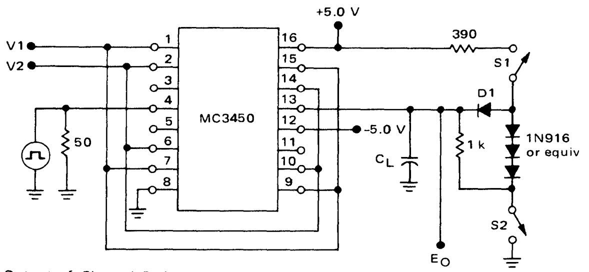
S1 at "A" for MC3452
S1 at "B" for MC3450
C_L = 15 pF total for MC3452
C_L = 50 pF total for MC3450

E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

8

TEST CIRCUITS (continued)

FIGURE 11 – STROBE PROPAGATION DELAY TIMES $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHO(S)}$ and $t_{POH(S)}$



Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

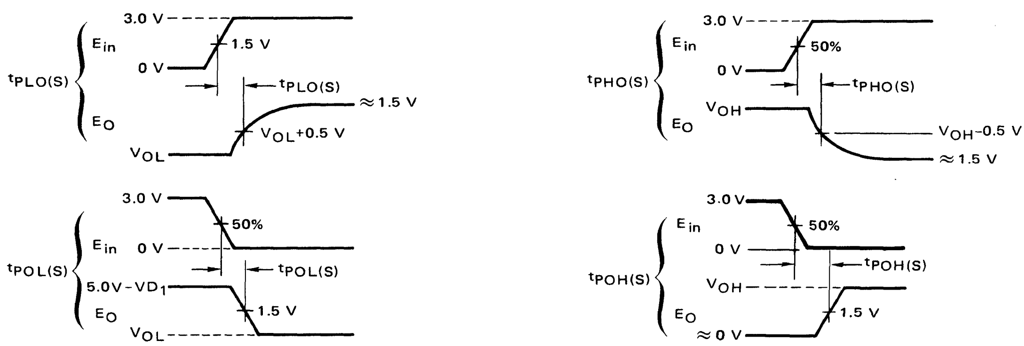
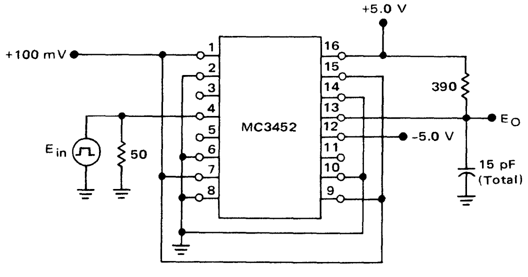
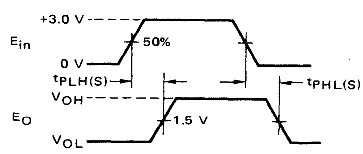


FIGURE 12 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$



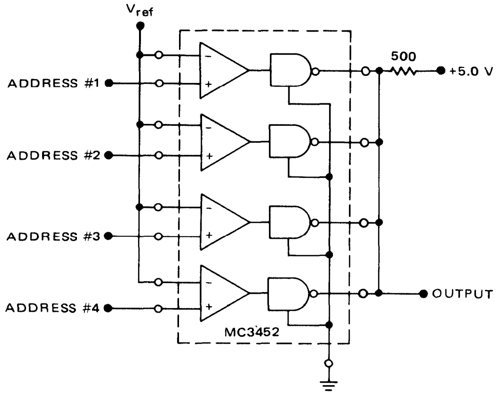
Output of Channel B shown under test, other channels are tested similarly.



E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

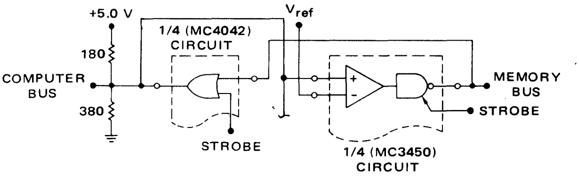
APPLICATIONS INFORMATION

FIGURE 13 – IMPLIED "AND" GATING



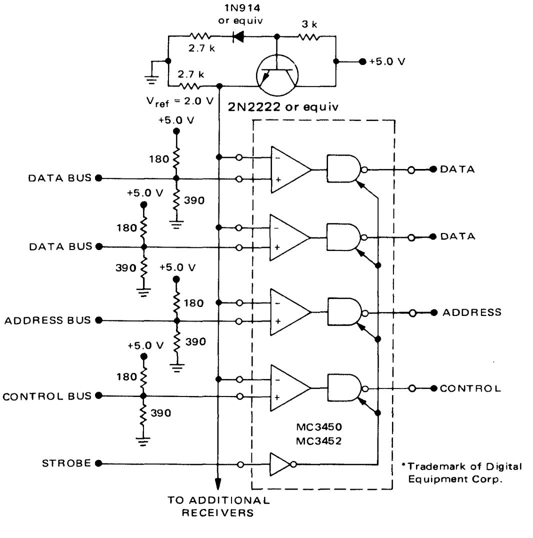
The MC3452 can be used for address decoding as illustrated above. All outputs of the MC3452 are tied together through a common resistor to +5.0 volts. In this configuration the MC3452 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

FIGURE 14 – BIDIRECTIONAL DATA TRANSMISSION



The three-state capability of the MC3450 permits bidirectional data transmission as illustrated.

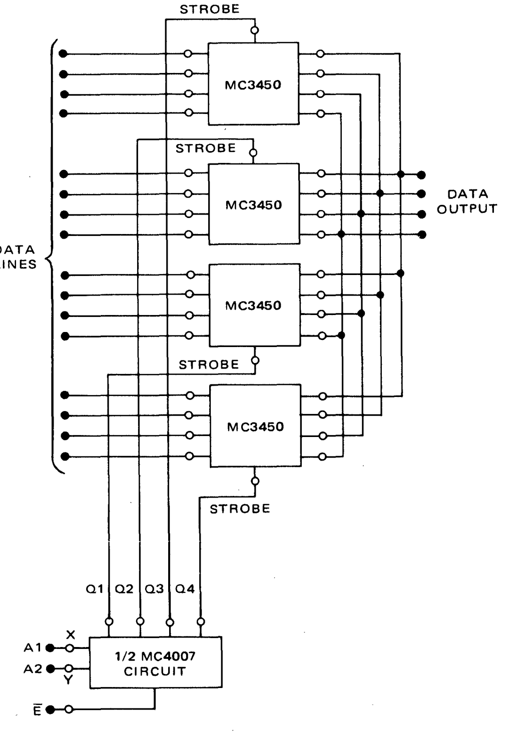
FIGURE 15 – SINGLE-ENDED UNI-BUS* LINE RECEIVER APPLICATION FOR MINICOMPUTERS



*Trademark of Digital Equipment Corp.

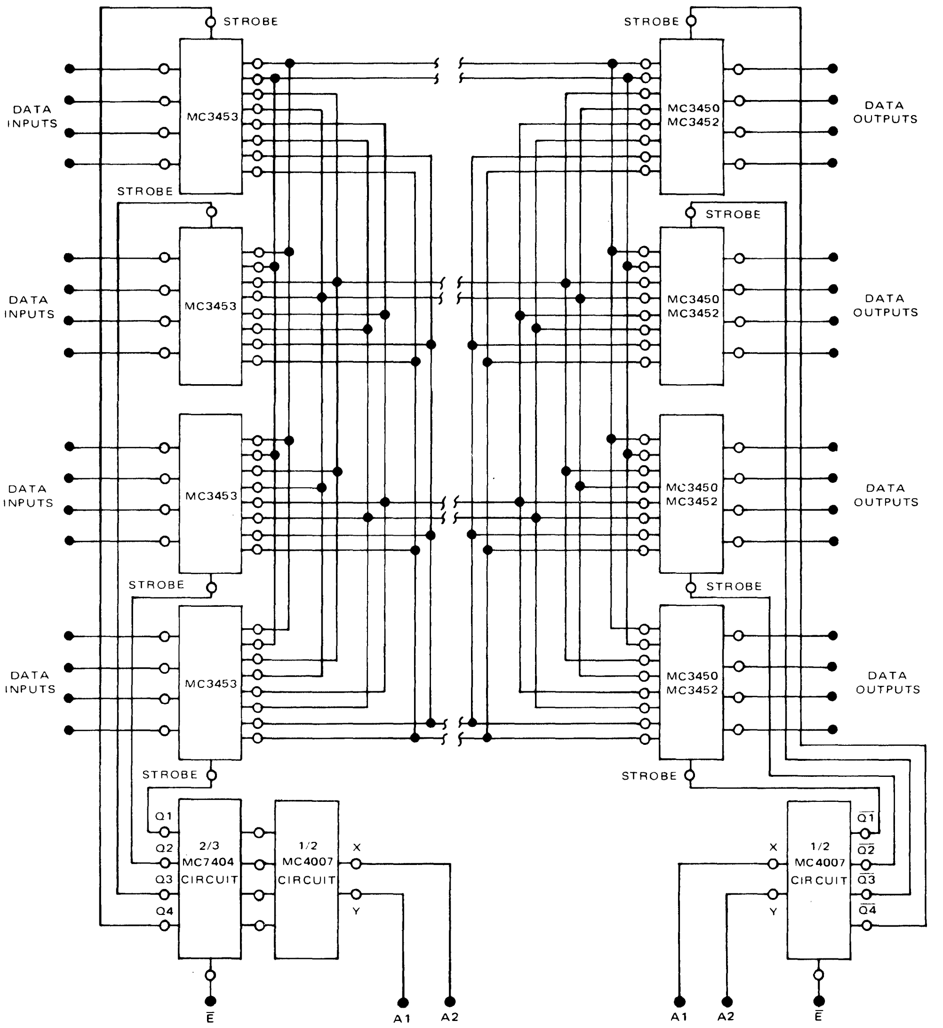
The MC3450/3452 can be used for single-ended as well as differential line receiving. For single-ended line receiver applications, such as are encountered in minicomputers, the configuration shown in Figure 15 can be used. The voltage source, which generates V_{ref}, should be designed so that the V_{ref} voltage is halfway between V_{OH}(min) and V_{OL}(max). The maximum input overdrive required to guarantee a given logic state is extremely small, 25 mV maximum. This low-input overdrive enhances differential noise immunity. Also the high-input impedance of the line receiver permits many receivers to be placed on a single line with minimum load effects.

FIGURE 16 – WIRED "OR" DATA SELECTION USING THREE-STATE LOGIC



APPLICATIONS INFORMATION (continued)

FIGURE 17 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



For further information on Data Transmission Systems see Motorola Application Note AN-708, "Line Driver and Receiver Considerations".

8

MC3453

QUAD LINE DRIVER

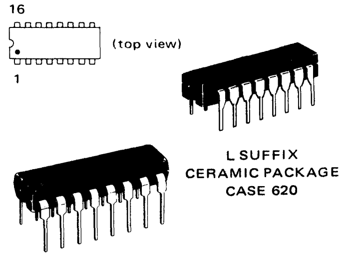
MONOLITHIC MTTL COMPATIBLE QUAD LINE DRIVER

The MC3453 features four MC75110 type line drivers with a common inhibit input. When the inhibit input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the inhibit is low, all channel outputs are nonconductive (transistors biased to cut-off). This minimizes loading in party-line systems where a large number of drivers share the same line.

- Four Independent Drivers with Common Inhibit Input
- -3.0 Volts Output Common-Mode Voltage Over Entire Operating Range
- Improved Driver Design Exceeds Performance of Popular MC75110

QUAD LINE DRIVER WITH COMMON INHIBIT INPUT

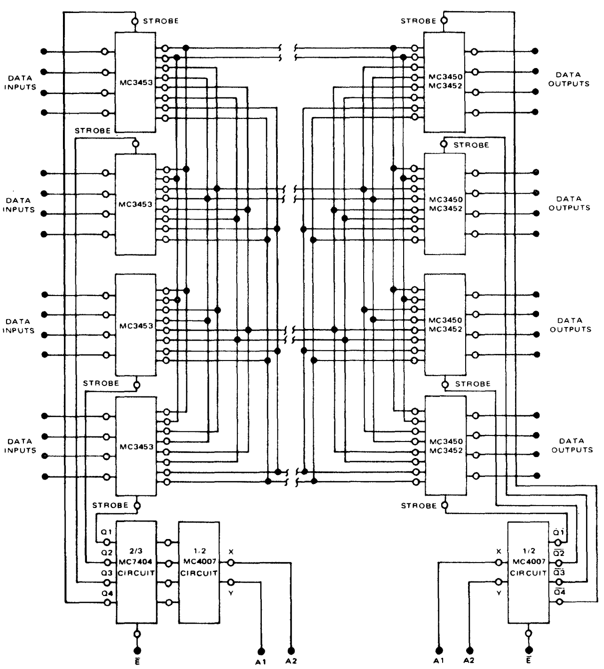
MONOLITHIC SILICON INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

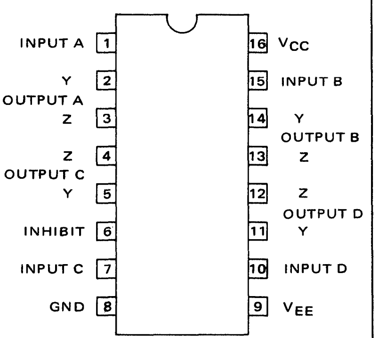
P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 — PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



For further information on Data Transmission Systems see Motorola Application Note AN-708, "Line Driver and Receiver Considerations".

CONNECTION DIAGRAM



TRUTH TABLE
(positive logic)

LOGIC INPUT	INHIBIT INPUT	OUTPUT CURRENT Z	OUTPUT CURRENT Y
H	H	On	Off
L	H	Off	On
H	L	Off	Off
L	L	Off	Off

L = Low Logic Level
H = High Logic Level

See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages	V_{in}	5.5	Volts
Common-Mode Output Voltage Range	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 1000 6.6	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Plastic and Ceramic Dual In-Line Packages	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range Positive Negative	V_{OCR}	 0 0	 – –	 +10 -3.0	Volts

Note 1. These voltage values are in respect to the ground terminal.
Note 2. When not using all four channels, unused outputs must be grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	2.0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	0	0.8	Volts

*The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic##	Symbol	Min	Typ#	Max	Unit
High-Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)	I_{IH_L}	 – –	 – –	 40 1.0	 µA mA
Low-Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	–	–	-1.6	mA
High-Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	 – –	 – –	 40 1.0	 µA mA
Low-Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	–	–	-1.6	mA
Output Current ("on" state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(on)}$	 – 6.5	 11 11	 15 –	mA
Output Current ("off" state) (V_{CC} = Min, V_{EE} = Min)	$I_{O(off)}$	–	5.0	100	µA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	–	35	50	mA
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	–	65	90	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{CC(off)}$	–	35	50	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	–	25	40	mA

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.
##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
Ground unused inputs and outputs.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L} t_{PHL_L}	– –	9.0 9.0	15 15	ns
Propagation Delay Time from Inhibit Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I} t_{PHL_I}	– –	16 20	25 25	ns

FIGURE 2 – LOGIC INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS

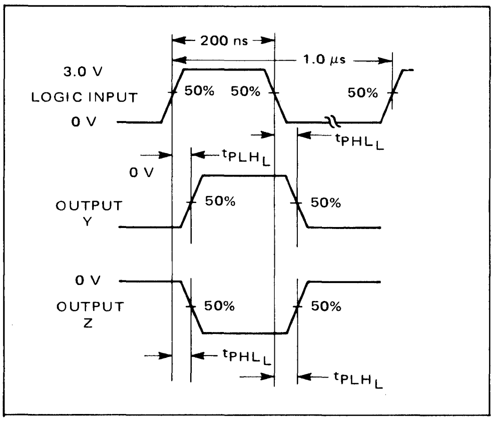
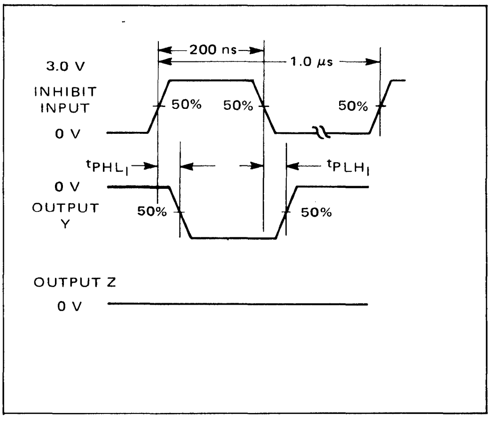


FIGURE 3 – INHIBIT INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS



TEST CIRCUITS

FIGURE 4 – LOGIC INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT

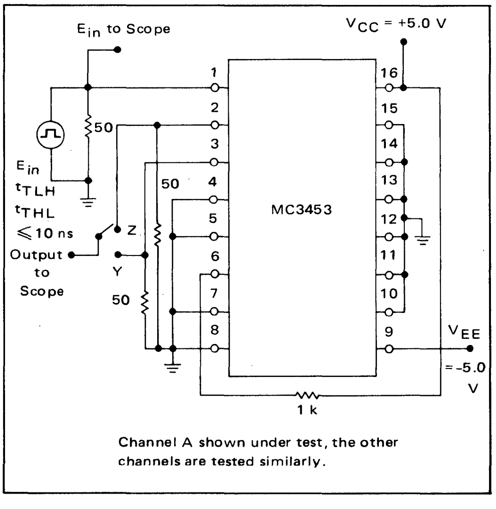
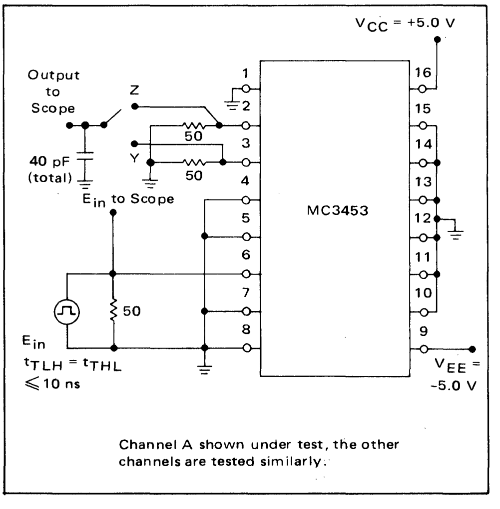
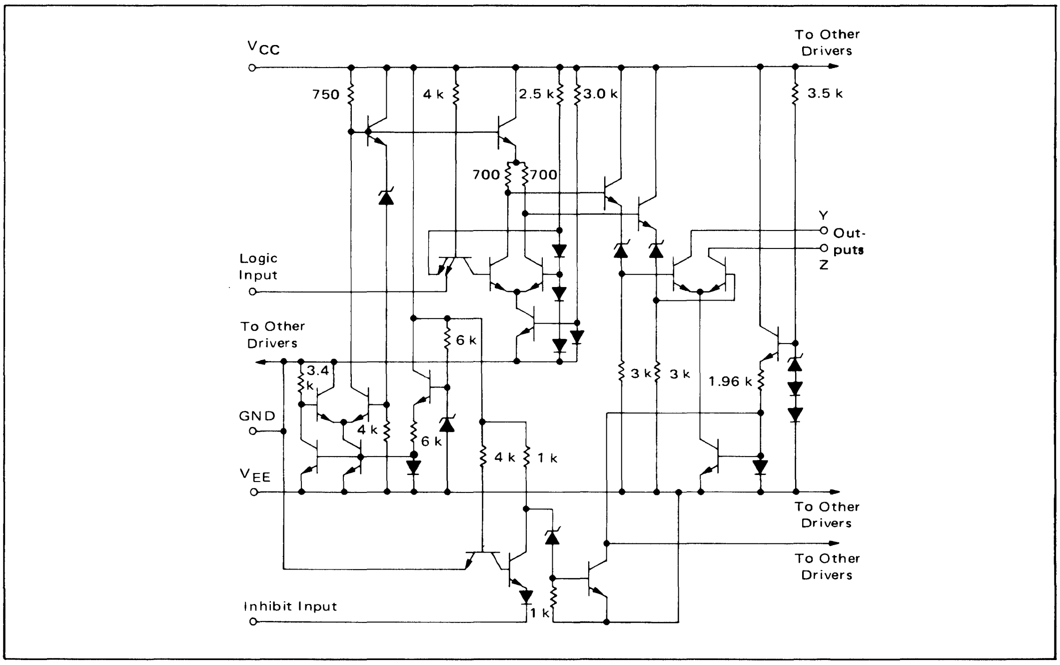


FIGURE 5 – INHIBIT INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT



8

FIGURE 6 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



8

MC5528
MC5529
MC7528
MC7529

DUAL SENSE AMPLIFIERS

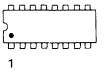
MONOLITHIC DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS

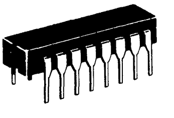
This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits. External preamplifier test points provide for very accurate timing of the strobe with the input signal.

- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
  1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs
- Test Points Available for Accurate Strobe Timing

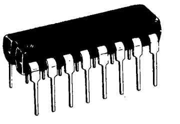
DUAL HIGH-SPEED SENSE AMPLIFIER WITH PREAMPLIFIER TEST POINTS

MONOLITHIC SILICON INTEGRATED CIRCUIT



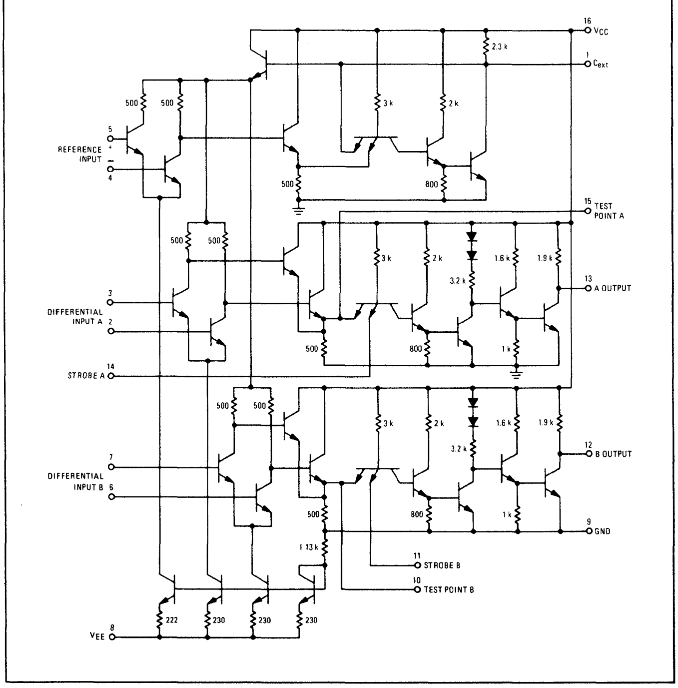


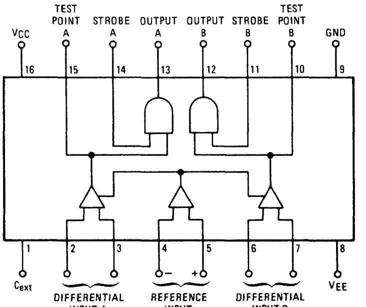
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC7528 and MC7529 only)

SCHEMATIC DIAGRAM





See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Vdc Vdc
Differential Input Voltages	V_{in} or V_{ref}	±5.0	Vdc
Power Dissipation Derate above T_A = +25°C	P_D	575 3.85	mW mW°C
Operating Temperature Range MC5528, MC5529 MC7528, MC7529	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = T_{low}# to T_{high}# unless otherwise noted.)

Characteristic	Symbol	MC5528 ① # MC5529			MC7528 # MC7529			Unit
		Min	Typ	Max	Min	Typ	Max	
Differential Input Threshold Voltage (V_{inS} = +5.0 V, V_{ID} = ±V_{th})	V_{th}							mV
(V_{ref} = 15 mV, I_L = 16 mA, V_O <0.4 V) MC5528,MC7528 MC5529,MC7529		10 8.0	15 –	– –	11 8.0	15 –	– –	
(V_{ref} = 40 mV, I_L = 16 mA, V_O <0.4 V) MC5528,MC7528 MC5529,MC7529		35 33	40 –	– –	36 33	40 –	– –	
(V_{ref} = 15 mV, I_L = -400 µA, V_O >2.4 V) MC5528,MC7528 MC5529,MC7529		– –	15 –	20 22	– –	15 –	19 22	
(V_{ref} = 40 mV, I_L = -400 µA, V_O >2.4 V) MC5528,MC7528 MC5529,MC7529		– –	40 –	45 47	– –	40 –	44 47	
Differential and Reference Input Bias Current (V_{ID} = V_{ref} = 0V, V_{inS} = +5.25 V, V_S = ±5.25 V)	I_{IB}	–	30	100	–	30	75	µA
Differential Input Offset Current (V_{ID} = V_{ref} = 0 V, V_{inS} = +5.25 V, V_S = ±5.25 V)	I_{IOD}	–	0.5	–	–	0.5	–	µA
Input Voltage, Logic "1" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 2.0 V, I_L = 400 µA, V_S = ±4.75 V, V_O > 2.4 V)	$V_{in"1"}$	2.0	–	–	2.0	–	–	V
Input Voltage, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.8 V, I_L = 16 mA, V_S = ±4.75 V, V_{OL} < 0.4 V)	$V_{in"0"}$	–	–	0.8	–	–	0.8	V
Input Current, Logic "1" (V_{ID} = 0 V, V_{ref} = 20 mV, V_{inS} = 2.4 V, V_S = ±5.25 V) MC5528,MC5529 (V_{ID} = 0 V, V_{ref} = 20 mV, V_{inS} = +5.25 V, MC7528,MC7529 V_S = ±5.25 V)	$I_{in"1"}$	– –	5.0 –	40 –	– –	– 0.02	– 1.0	µA mA
Input Current, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.4 V, V_S = ±5.25 V)	$I_{in"0"}$	–	-1.0	-1.6	–	-1.0	-1.6	mA
Output Voltage, Logic "1" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 2.0 V, I_L = -400 µA, V_S = ±4.75 V)	$V_{O"1"}$	2.4	3.9	–	2.4	3.9	–	V
Output Voltage, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.8 V, I_L = 16 mA, V_S = ±4.75 V)	$V_{O"0"}$	–	0.25	0.40	–	0.25	0.40	V
Short-Circuit Output Current (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = +5.25 V, V_S = ±5.25 V)	I_{OSC}	-2.1	-2.8	-3.5	-2.1	-2.8	-3.5	mA
V_{CC} Supply Current (V_{ID} = V_{inS} = 0 V, V_{ref} = 20 mV, V_S = ±5.25 V)	I_{CC}	–	29	40	–	29	40	mA
V_{EE} Supply Current (V_{ID} = V_{inS} = 0 V, V_{ref} = 20 mV, V_S = ±5.25 V)	I_{EE}	–	-13	-18	–	-13	-18	mA

① For 0°C ≤T_A ≤70°C operation; electrical characteristics for MC5528 and MC5529 are guaranteed the same as MC7528 and MC7529 respectively.

T_{low} = -55°C for MC5528, MC5529, 0°C for MC7528, MC7529
T_{high} = +125°C for MC5528, MC5529; +70°C for MC7528, MC7529

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC5528 MC5529 Min	Typ	Max	MC7528 MC7529 Min	Typ	Max	Unit
AC Common-Mode Input Firing Voltage (V_{ref} = 20 mV, V_{inS} = 5.0 V)	V_{CMF}	–	±2.5	–	–	±2.5	–	V
Propagation Delay Time, Differential Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PLHD}	–	20	40	–	20	40	ns
Propagation Delay Time, Differential Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLD}	–	28	–	–	28	–	ns
Propagation Delay Time, Strobe Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PHLS}	–	10	30	–	10	30	ns
Propagation Delay Time, Strobe Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLS}	–	20	–	–	20	–	ns
Overload Recovery Time, Differential Input	t_{RD}	–	10	–	–	10	–	ns
Overload Recovery Time, Common-Mode Input	t_{RCM}	–	5.0	–	–	5.0	–	ns
Minimum Cycle Time	t(min)	–	200	–	–	200	–	ns

② Positive current is defined as current into the referenced pin.
③ Pin 1 to have ≥100 pF capacitor connected to ground.
④ Each test point to have ≤15 pF capacitive load to ground.

8

DUAL SENSE AMPLIFIERS

MC5534
MC5535
MC7534
MC7535

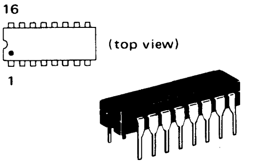
MONOLITHIC DUAL SENSE AMPLIFIERS WITH INVERTED OUTPUTS

This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits. These circuits are identical to the MC7524 except that an additional stage has been added to each output gate to provide an inverted output.

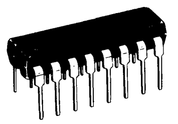
- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
  1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs
- Normally High Outputs Accomodate the Wired-OR of Several Sense Amplifiers

DUAL HIGH-SPEED SENSE AMPLIFIER WITH INVERTED OUTPUTS

MONOLITHIC SILICON INTEGRATED CIRCUIT

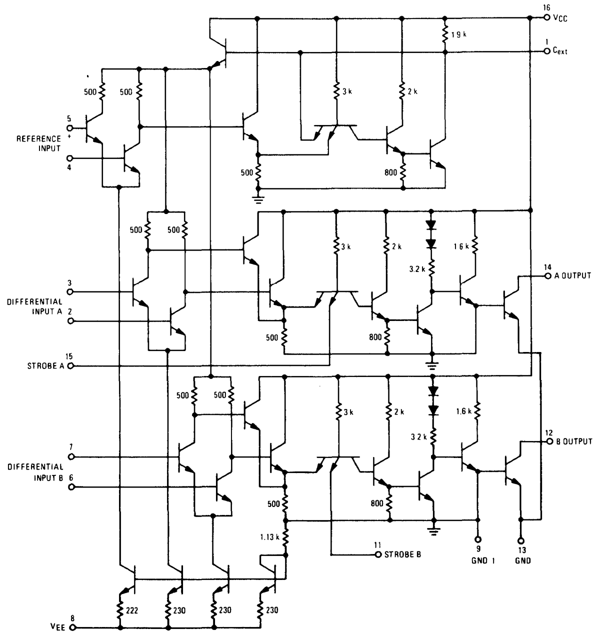


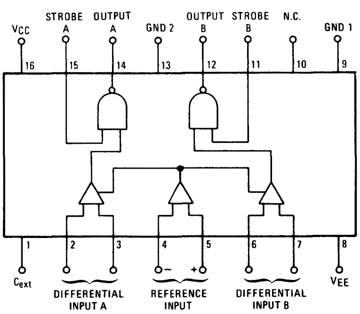
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC7528 and MC7529 only)

SCHEMATIC DIAGRAM





See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Vdc Vdc
Differential Input Voltages	V_{in} or V_{ref}	±5.0	Vdc
Power Dissipation Derate above T_A = +25°C	P_D	575 3.85	mW mW°C
Operating Temperature Range MC5534, MC5535 MC7534, MC7535	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = T_{low}# to T_{high}# unless otherwise noted.)

Characteristic		Symbol	MC5534 ① # MC5535			MC7534# MC7535			Unit
			Min	Typ	Max	Min	Typ	Max	
Differential Input Threshold Voltage (V_{inS} = +5.0 V, V_{ID} = ±V_{th})		V_{th}							mW
(V_{ref} = 15 mV, V_L = +5.25 V, I_L < 250 µA)	MC5534, MC7534		10	15	–	11	15	–	
	MC5535, MC7535		8.0	–	–	8.0	–	–	
(V_{ref} = 40 mV, V_L = +5.25 V, I_L < 250 µA)	MC5534, MC7534		35	40	–	36	40	–	
	MC5535, MC7535		33	–	–	33	–	–	
(V_{ref} = 15 mV, I_L = 20 mA, V_O = < 0.4 V)	MC5534, MC7534		–	15	20	–	15	19	
	MC5535, MC7535		–	–	22	–	–	22	
(V_{ref} = 40 mV, I_L = 200 mA, V_O = < 0.4 V)	MC5534, MC7534		–	40	45	–	40	44	
	MC5535, MC7535		–	–	47	–	–	47	
Differential Reference Input Bias Current (V_{ID} = V_{ref} = 0 V, V_{inS} = +5.25 V, V_S = ±5.25 V)		I_{IB}	–	30	100	–	30	75	µA
Differential Input Offset Current (V_{ID} = V_{ref} = 0 V, V_{inS} = +5.25 V, V_S = ±5.25 V)		I_{IOD}	–	0.5	–	–	0.5	–	µA
Input Voltage, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.8 V, V_L = +5.25 V, V_S = ±4.75 V, I_L = < 250 µA)		V_{in}"0"	–	–	0.8	–	–	0.8	V
Input Voltage, Logic "1" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 2.0 V, I_L = 20 mA, V_S = ±4.75 V, V_O = < 0.4 V)		V_{in}"1"	2.0	–	–	2.0	–	–	V
Input Current, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.4 V, V_S = ±5.25 V)		I_{in}"0"	–	-1.0	-1.6	–	-1.0	-1.6	mA
Input Current, Logic "1" (V_{ID} = 0 V, V_{ref} = 20 mV, V_{inS} = 2.4 V, V_S = ±5.25 V)	MC5534, MC5535	I_{in}"1"	–	5.0	40	–	–	–	µA
	MC7534, MC7535		–	–	–	–	0.02	1.0	mA
Output Voltage, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 2.0 V, I_L = 20 mA, V_S = ±4.75 V)		V_O"0"	–	0.25	0.40	–	0.25	0.40	V
Output Leakage Current (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.8 V, V_L = 5.25 V, V_S = ±4.75 V)		I_{OL}	–	0.01	250	–	0.01	250	µA
V_{CC} Supply Current (V_{ID} = V_{inS} = 0 V, V_{ref} = 20 mV, V_S = ±5.25 V)		I_{CC}	–	28	38	–	28	38	mA
V_{EE} Supply Current (V_{ID} = V_{inS} = 0 V, V_{ref} = 20 mV, V_S = ±5.25 V)		I_{EE}	–	-13	-18	–	-13	-18	mA

① For 0°C ⩽ T_A ⩽ 70°C operation, electrical characteristics for MC5534 and MC5535 are guaranteed the same as MC7534 and MC7535 respectively.

T_{low} = -55°C for MC5534, MC5535, 0°C for MC7534, MC7535
T_{high} = +125°C for MC5534, MC5535, +70°C for MC7534, MC7535

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ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC5534 MC5535 Min	MC5534 MC5535 Typ	MC5534 MC5535 Max	MC7534 MC7535 Min	MC7534 MC7535 Typ	MC7534 MC7535 Max	Unit
AC Common-Mode Input Firing Voltage (V_{ref} = 20 mV, V_{inS} = 5.0 V)	V_{CMF}	–	±2.5	–	–	±2.5	–	V
Propagation Delay Time, Differential Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PLHD}	–	24	–	–	24	–	ns
Propagation Delay Time, Differential Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLD}	–	20	40	–	20	40	ns
Propagation Delay Time, Strobe Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PLHS}	–	16	–	–	16	–	ns
Propagation Delay Time. Strobe Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLS}	–	10	30	–	10	30	ns
Overload Recovery Time, Differential Input	t_{RD}	–	10	–	–	10	–	ns
Overload Recovery Time, Common-Mode Input	t_{RCM}	–	5.0	–	–	5.0	–	ns
Minimum Cycle Time	t(min)	–	200	–	–	200	–	ns

② Positive current is defined as current into the referenced pin.

③ Pin 1 to have ⩾100 pF capacitor connected to ground.

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MC5538
MC5539
MC7538
MC7539

DUAL SENSE AMPLIFIERS

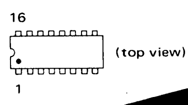
MONOLITHIC DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS AND INVERTED OUTPUTS

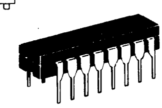
This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits. These devices are identical to MC5528/MC7528 with the exception of the inverted outputs.

- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
  1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs
- Test Points Available for Strobe Timing
- Inverted Outputs to Accomodate Wired-OR Outputs of Several Sense Amplifiers

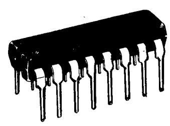
DUAL HIGH-SPEED SENSE AMPLIFIER
WITH PREAMPLIFIER TEST POINTS AND INVERTED OUTPUTS

MONOLITHIC SILICON INTEGRATED CIRCUIT



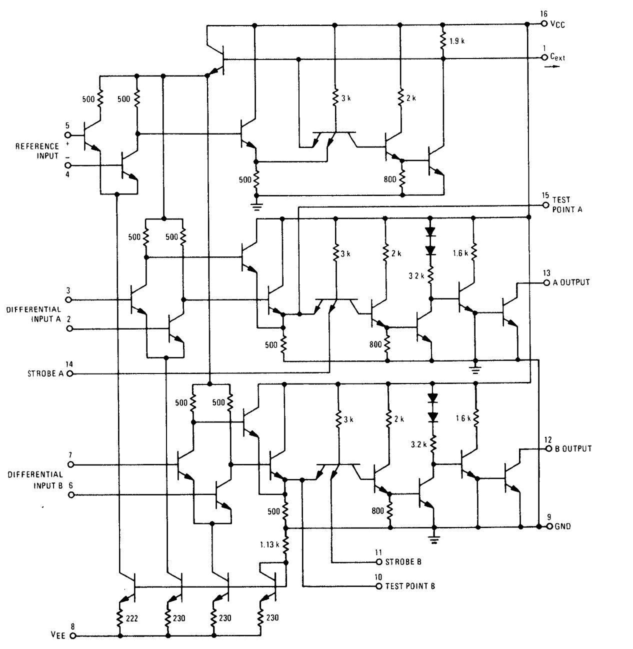


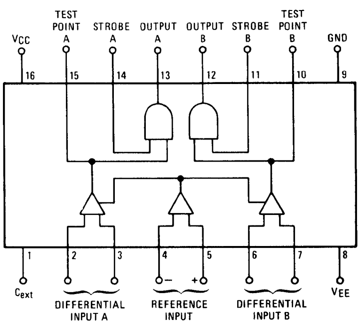
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC7538 and MC7539 only)

SCHEMATIC DIAGRAM





See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Vdc Vdc
Differential Input Voltages	V_{in} or V_{ref}	±5.0	Vdc
Power Dissipation Derate above T_A = +25°C	P_D	575 3.85	mW mW°C
Operating Temperature Range MC5538, MC5539 MC7538, MC7539	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = T_{low}# to T_{high}# unless otherwise noted.)

Characteristic		Symbol	MC5538 ① # MC5539			MC7538 # MC7539			Unit
			Min	Typ	Max	Min	Typ	Max	
Differential Input Threshold Voltage (V_{inS} = +5.0 V, V_{ID} = ±V_{th})		V_{th}							mV
(V_{ref} = 15 mV, V_L = +5.25 V, I_L < 250 µA)	MC5538, MC7538		10	15	–	11	15	–	
	MC5539, MC7539		8.0	–	–	8.0	–	–	
(V_{ref} = 40 mV, V_L = +5.25 V, I_L < 250 µA)	MC5538, MC7538		35	40	–	36	40.	–	
	MC5539, MC7539		33	–	–	33	–	–	
(V_{ref} = 15 mV, I_L = 120 mA, V_L < 0.4 V)	MC5538, MC7538		–	15	20	–	15	19	
	MC5539, MC7539		–	–	22	–	–	22	
(V_{ref} = 40 mV, I_L = +20 mA, V_L < 0.4 V)	MC5538, MC7538		–	40	45	–	40	44	
	MC5539, MC7539		–	–	47	–	–	47	
Differential and Reference Input Bias Current (V_{ID} = V_{ref} = 0 V, V_{inS} = +5.25 V, V_S = ±5.25 V)		I_{IB}	–	30	100	–	30	75	µA
Differential Input Offset Current (V_{ID} = V_{ref} = 0 V, V_{inS} = +5.25 V, V_S = ±5.25 V)		I_{IOD}	–	0.5	–	–	0.5	–	µA
Input Voltage, Logic "1" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = +2.0 V, I_L = 20 mA, V_S = ±4.75 V, V_L < 0.4 V)		V_{in}"1"	2.0	–	–	2.0	–	–	V
Input Voltage, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = +0.8 V, V_L = +5.25 V, V_S = ±4.75 V, I_L < 250 µA)		V_{in}"0"	–	–	0.8	–	–	0.8	V
Input Current, Logic "1" (V_{ID} = 0 V, V_{ref} = 20 mV, V_{inS} = 2.4 V, V_S = ±5.25 V)	MC5538, MC5539	I_{in}"1"	–	5.0	40	–	–	–	µA
(V_{ID} = 0 V, V_{ref} = 20 mV, V_{inS} = +5.25 V, V_S = ±5.25 V)	MC7538, MC7539		–	–	–	–	0.02	1.0	mA
Input Current, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.4 V, V_S = ±5.25 V)		I_{in}"0"	–	-1.0	-1.6	–	-1.0	-1.6	mA
Output Voltage, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 2.0 V, I_L = 20 mA, V_S = ±4.75 V)		V_O"0"	–	0.25	0.40	–	0.25	0.40	V
V_{CC} Supply Current (V_{ID} = V_{inS} = 0 V, V_{ref} = 20 mV, V_S = ±5.25 V)		I_{CC}	–	28	38	–	28	38	mA
V_{EE} Supply Current (V_{ID} = V_{inS} = 0 V, V_S = ±5.25 V)		I_{EE}	–	-13	-18	–	-13	-18	mA

① For 0°C ≤ T_A ≤ 70°C operation, electrical characteristics for MC5538 and MC5539 are guaranteed the same as MC7538 and MC7539 respectively.

T_{low} = -55°C for MC5538, MC5539; 0°C for MC7538, MC7539
T_{high} = +125°C for MC5538, MC5539; +70°C for MC7538, MC7539

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ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC5538 MC5539 Min	MC5538 MC5539 Typ	MC5538 MC5539 Max	MC7538 MC7539 Min	MC7538 MC7539 Typ	MC7538 MC7539 Max	Unit
AC Common-Mode Input Firing Voltage (V_{ref} = 20 mV, V_{inS} = 5.0 V)	V_{CMF}	–	±2.5	–	–	±2.5	–	V
Propagation Delay Time, Differential Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PLHD}	–	24	–	–	24	–	ns
Propagation Delay Time, Differential Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLD}	–	20	40	–	20	40	ns
Propagation Delay Time, Strobe Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PHLS}	–	16	–	–	16	–	ns
Propagation Delay Time, Strobe Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLS}	–	10	30	–	10	30	ns
Overload Recovery Time, Differential Input	t_{RD}	–	10	–	–	10	–	ns
Overload Recovery Time, Common-Mode Input	t_{RCM}	–	5.0	–	–	5.0	–	ns
Minimum Cycle Time	t(min)	–	200	–	–	200	–	ns

② Positive current is defined as current into the referenced pin.
③ Pin 1 to have ≥100 pF capacitor connected to ground.
④ Each test point to have ≤15 pF capacitive load to ground.

8

MC7520L
thru
MC7523L

DUAL SENSE AMPLIFIERS

MONOLITHIC DUAL SENSE AMPLIFIERS

These dual sense amplifiers are designed for high-speed core memory systems. Low-level pulses originating in the memory are converted to logic levels compatible with MTTL and MDTL circuits. Each of the two basic device functions has two different threshold specifications. The dual-input preamplifiers are connected to a common output stage, with each preamplifier output strobed independently.

The output circuit of the MC7520L/MC7521L is comprised of two cascaded NAND gates, each having an external gate input. The external gate inputs may be used to connect the $\overline{Q}$ output to the Gate Q input to achieve a flip-flop or register that responds to the sense and strobe input conditions. Output pulse stretching may be accomplished by resistive/capacitive coupling from the $\overline{Q}$ output to the Gate Q input.

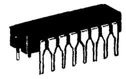
The output circuit of the MC7522L/MC7523L features an open-collector output, permitting the wired-OR function. Load resistor R_L may be used as the output pullup resistor.

- Adjustable Threshold Voltage Levels
- High Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin – 1.0 Volt typical
- Good Fanout Capability

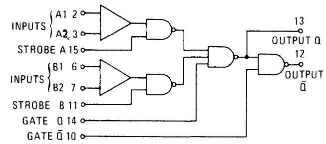
DUAL HIGH-SPEED SENSE AMPLIFIER INTEGRATED CIRCUITS

MONOLITHIC SILICON EPITAXIAL PASSIVATED

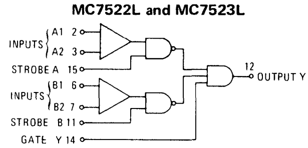
CERAMIC PACKAGE
CASE 620



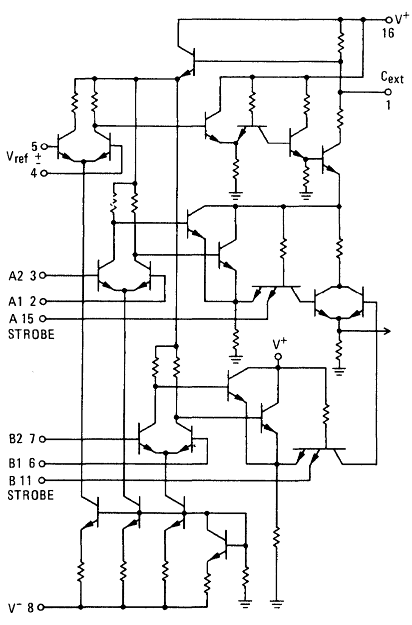
MC7520L and MC7521L



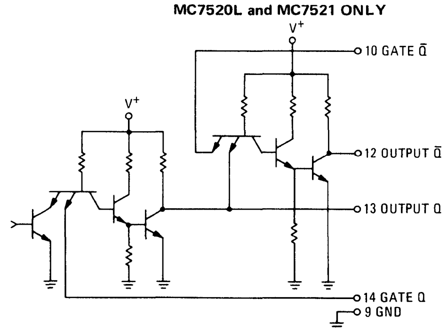
MC7522L and MC7523L



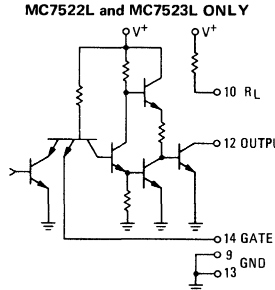
COMMON TO ALL DEVICES



MC7520L and MC7521 ONLY



MC7522L and MC7523L ONLY



See Packaging Information Section for outline dimensions.

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ELECTRICAL CHARACTERISTICS (V^+ = 5.0 V, V^- = -5.0 V, T_A = 0 to +70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Threshold Voltage		V_{th}				mV
V_{ref} = 15 mV	MC7520L,MC7522L		11	15	19	
	MC7521L,MC7523L		8.0	15	22	
V_{ref} = 40 mV	MC7520L,MC7522L		36	40	44	
	MC7521L,MC7523L		33	40	47	
Common-Mode Input Firing Voltage		V_{CMF}	–	±3.0	–	Volts
Input Bias Current		I_{in}	–	30	75	µA
Input Offset Current		I_{io}	–	0.5	–	µA
Input Impedance (f = 1.0 kHz)		$Z_{(in)\,D}$	–	2.0	–	k ohms
Input Voltage Logic "1" Level (Strobe Inputs)	V_{in} "0" = 0.8 V	V_{in} "1"	2.0	–	–	Volts
Input Voltage Logic "0" Level (Strobe Inputs)	V_{in} "1" = 2.0 V	V_{in} "0"	–	–	0.8	Volt
Input Current Logic "0" Level (Strobe Inputs)	V_{in} "0" = 0.4 V	I_{in} "0"	–	–	-1.6	mA
Input Current Logic "1" Level (Strobe Inputs)	V_{in} "1" = 2.4 V	I_{in} "1"	–	–	40	µA
	V_{in} "1" = V^+		–	–	1.0	mA
Output Voltage Logic "1" Level	V_{in} "1" = 2.0 V	V_{out} "1"	2.4	3.9	–	Volts
Output Voltage Logic "0" Level	V_{in} "0" = 0.8 V	V_{out} "0"	–	0.25	0.4	Volt
Short-Circuit Output Current	Q Output MC7520L,MC7521L	I_{SC}	3.3	–	5.0	mA
	$\bar{Q}$ Output MC7520L,MC7521L		2.1	–	3.5	
	Output MC7522L,MC7523L		2.1	–	3.5	
V^+ Supply Current (T_A = +25°C)	MC7520L,MC7521L	I^+	–	28	–	mA
	MC7522L,MC7523L		–	27	–	
V^- Supply Current (T_A = +25°C)	MC7520L,MC7521L	I^-	–	-14	–	mA
	MC7522L,MC7523L		–	-15	–	

SWITCHING CHARACTERISTICS (V^+ = 5.0 V, V^- = -5.0 V, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential-Mode Input Overload Recovery Time	$t_{OR\,DM}$	–	20	–	ns
Common-Mode Input Overload Recovery Time	$t_{OR\,CM}$	–	20	–	ns
Minimum Cycle Time	$t_{c\,(min)}$	–	200	–	ns

MC7520L, MC7521L

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					ns
(Differential Input to Q Output)	t_{pd} "1" DQ	–	20	40	
	t_{pd} "0" DQ	–	30	–	
(Differential Input to $\bar{Q}$ Output)	t_{pd} "1" D$\bar{Q}$	–	25	–	
	t_{pd} "0" D$\bar{Q}$	–	35	55	
(Strobe Input to Q Output)	t_{pd} "1" SQ	–	15	30	
	t_{pd} "0" SQ	–	25	–	
(Strobe Input to $\bar{Q}$ Output)	t_{pd} "1" S$\bar{Q}$	–	15	–	
	t_{pd} "0" S$\bar{Q}$	–	35	55	
(Gate Q Input to Q Output)	t_{pd} "1" G_QQ	–	10	20	
	t_{pd} "0" G_QQ	–	15	–	
(Gate Q Input to $\bar{Q}$ Output)	t_{pd} "1" $G_Q\bar{Q}$	–	15	–	
	t_{pd} "0" $G_Q\bar{Q}$	–	20	30	
(Gate $\bar{Q}$ Input to $\bar{Q}$ Output)	t_{pd} "1" $G_{\bar{Q}}\bar{Q}$	–	15	–	
	t_{pd} "0" $G_{\bar{Q}}\bar{Q}$	–	10	20	

MC7522L, MC7523L

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					ns
(Differential Input to Output)	t_{pd} "1" D	–	20	–	
	t_{pd} "0" D	–	30	45	
(Strobe Input to Output)	t_{pd} "1" S	–	15	–	
	t_{pd} "0" S	–	25	40	
(Gate Input to Output)	t_{pd} "1" G	–	10	–	
	t_{pd} "0" G	–	15	25	

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Units
Power Supply Voltage	V^+ V^-	+7.0 -7.0	Vdc Vdc
Differential Input Signal Voltage	V_{in}	±5.0	Vdc
Strobe and Gate Input Voltage	$V_{in\ S,G}$	±5.5	Vdc
Power Dissipation Derate above T_A = +25°C	P_D	575 3.85	mW mW°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

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MC7524L
MC7525L

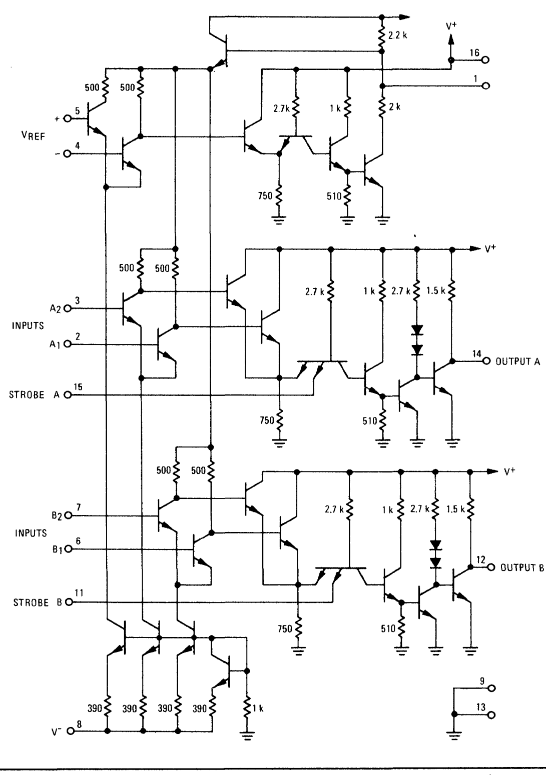
DUAL SENSE AMPLIFIERS

MONOLITHIC DUAL SENSE AMPLIFIERS

This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits.

Features:

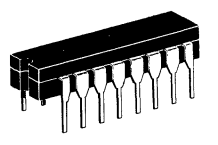
- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
  1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs



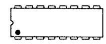
See Packaging Information Section for outline dimensions.

DUAL HIGH-SPEED SENSE AMPLIFIER INTEGRATED CIRCUIT

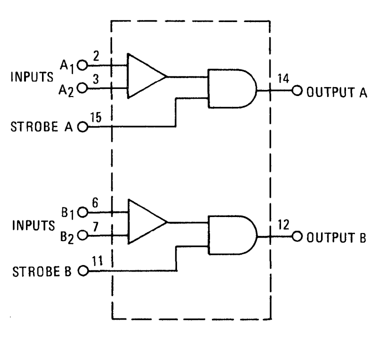
MONOLITHIC SILICON EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 620



Equivalent Circuit



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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Units
Power Supply Voltage	V^+ V^-	+7.0 -7.0	Vdc Vdc
Differential Input Voltages	V_{in} or V_{ref}	±5.0	Vdc
Power Dissipation Derate above T_A = +25°C	P_D	575 3.85	mW mW°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = 5.0 V, V^- = -5.0 V, T_A = 0 to +70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Threshold Voltage		V_{th}				mV
V_{ref} = 15 mV	MC7524L		11	15	19	
	MC7525L		8.0	15	22	
V_{ref} = 40 mV	MC7524L		36	40	44	
	MC7525L		33	40	47	
Common-Mode Input Firing Voltage		V_{CMF}	–	±3.0	–	Volts
Input Bias Current		I_{in}	–	30	75	μA
Input Offset Current		I_{io}	–	0.5	–	μA
Input Impedance (f = 1.0 kHz)		$Z_{(in)\ D}$	–	2.0	–	k ohms
Input Voltage Logic "1" Level (Strobe Inputs)	$V_{in(0)}$ = 0.8 V	$V_{in\ (1)}$	2.0	–	–	Volts
Input Voltage Logic "0" Level (Strobe Inputs)	$V_{in(1)}$ = 2.0 V	$V_{in\ (0)}$	–	–	0.8	Volt
Input Current Logic "0" Level (Strobe Inputs)	$V_{in(0)}$ = 0.4 V	$I_{in\ (0)}$	–	-1.0	-1.6	mA
Input Current Logic "1" Level (Strobe Inputs)	$V_{in(1)}$ = 2.4 V $V_{in(1)} = V^+$	$I_{in\ (1)}$	– –	– –	40 1.0	μA mA
Output Voltage Logic "1" Level	$V_{in(1)}$ = 2.0 V, $V_{in(0)}$ = 0.8 V	$V_{out\ (1)}$	2.4	3.9	–	Volts
Output Voltage Logic "0" Level	$V_{in(0)}$ = 0.8 V	$V_{out\ (0)}$	–	0.25	0.4	Volt
Short-Circuit Output Current		$I_{sc(out)}$	2.1	–	3.5	mA
V^+ Supply Current @ T_A = +25°C		I^+	–	25	–	mA
V^- Supply Current @ T_A = +25°C		I^-	–	-15	–	mA

SWITCHING CHARACTERISTICS (V^+ = 5.0 V, V^- = -5.0 V, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time (Differential Input to Output)	$t_{pd\ (1)\ D}$ $t_{pd\ (0)\ D}$	– –	15 40	40 –	ns
Propagation Delay Time (Strobe Input to Output)	$t_{pd\ (1)\ S}$ $t_{pd\ (0)\ S}$	– –	15 35	30 –	ns
Differential-Mode Input Overload Recovery Time	$t_{OR\ DM}$	–	20	–	ns
Common-Mode Input Overload Recovery Time	$t_{OR\ CM}$	–	20	–	ns
Minimum Cycle Time	$t_{c\ (min)}$	–	200	–	ns

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MC7700CP Series

POSITIVE VOLTAGE REGULATORS

Product Preview

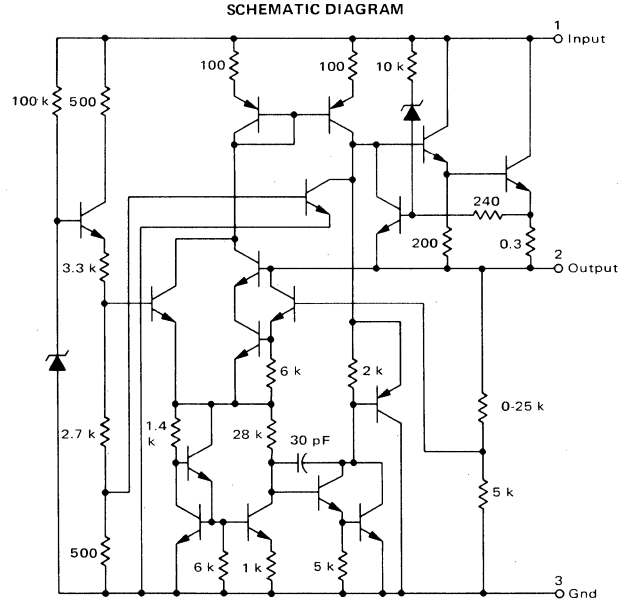
MC7700CP SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC7700CP Series positive voltage regulators are identical to the popular MC7800CP Series devices, except that they are specified for only half the output current. Like the MC7800CP devices, the MC7700CP three-terminal regulators are intended for local, on-card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 750 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 199-04 (Pin Compatible with the VERSAWATT† or TO-220)

SCHEMATIC DIAGRAM



†Trademark of Radio Corporation of America.
See Packaging Information Section for outline dimensions.

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

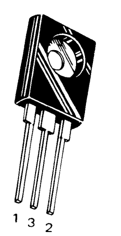
MONOLITHIC SILICON INTEGRATED CIRCUITS

TYPE NO./VOLTAGE	
MC7705CP	5.0 Volts
MC7706CP	6.0 Volts
MC7708CP	8.0 Volts
MC7712CP	12 Volts
MC7715CP	15 Volts
MC7718CP	18 Volts
MC7720CP	20 Volts
MC7724CP	24 Volts

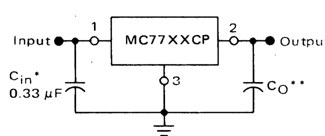
PLASTIC PACKAGE
CASE 199-04

Heat sink surface connected to pin 3.

Pin 1 Input
Pin 2 Output
Pin 3 Ground



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

MC7700CP Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (20 V - 24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air	 P_D $1/\theta_{JA}$ θ_{JA}	 2.0 20 50	 Watts mW/°C °C/W
T_C = +25°C Derate above T_C = +110°C Thermal Resistance, Junction to Case	P_D $1/\theta_{JC}$ θ_{JC}	7.5 500 2.0	Watts mW/°C °C/W
Storage Junction Temperature Range	T_{stg}	-20 to +150	°C
Operating Junction Temperature Range	T_J	0 to +125	°C

MC7705CP ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 250 mA, 0°C $< T_J <$ +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Input Regulation (T_J = +25°C, I_O = 50 mA) 7.0 Vdc $\leqslant V_{in} \leqslant$ 25 Vdc 8.0 Vdc $\leqslant V_{in} \leqslant$ 12 Vdc (T_J = +25°C, I_O = 250 mA) 7.0 Vdc $\leqslant V_{in} \leqslant$ 25 Vdc 8.0 Vdc $\leqslant V_{in} \leqslant$ 12 Vdc	Reg_{in}	 – – – –	 7.0 2.0 35 8.0	 50 25 100 50	mV
Load Regulation T_J = +25°C, 5.0 mA $\leqslant I_O \leqslant$ 750 mA 125 mA $\leqslant I_O \leqslant$ 375 mA	Reg_{load}	 – –	 11 4.0	 100 50	mV
Output Voltage (7.0 Vdc $\leqslant V_{in} \leqslant$ 20 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 500 mA, P $\leqslant$ 7.5 W)	V_O	4.75	–	5.25	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change 7.0 Vdc $\leqslant V_{in} \leqslant$ 25 Vdc 5.0 mA $\leqslant I_O \leqslant$ 750 mA	ΔI_B	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_N	–	40	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	V_{in}-V_O	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	R_O	–	30	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	375	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C $\leqslant T_A \leqslant$ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7706CP ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 250 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 50 mA)					
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	9.0	60	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 250 mA)					
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	43	120	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		–	10	60	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 750 mA		–	13	120	
125 mA ≤ I_O ≤ 375 mA		–	5.0	60	
Output Voltage 8.0 Vdc ≤ V_{in} ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ 7.5 W	V_O	5.7	–	6.3	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 750 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	45	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	$V_{in}-V_O$	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	R_O	–	35	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	275	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7708CP ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 250 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 50 mA)					
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	12	80	
11 Vdc ≤ V_{in} ≤ 17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 250 mA)					
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	50	160	
11 Vdc ≤ V_{in} ≤ 17 Vdc		–	22	80	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 750 mA		–	26	160	
125 mA ≤ I_O ≤ 375 mA		–	9.0	80	
Output Voltage 10.5 Vdc ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ 7.5 W	V_O	7.6	–	8.4	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 750 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	52	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	$V_{in}-V_O$	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	R_O	–	40	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	225	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7700CP Series (continued)

MC7712CP ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 250 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 50 mA)					
14.5 Vdc $\leqslant V_{in} \leqslant$ 30 Vdc		–	13	120	
16 Vdc $\leqslant V_{in} \leqslant$ 22 Vdc		–	6.0	60	
(T_J = +25°C, I_O = 250 mA)					
14.5 Vdc $\leqslant V_{in} \leqslant$ 30 Vdc		–	55	240	
16 Vdc $\leqslant V_{in} \leqslant$ 22 Vdc		–	24	120	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA $\leqslant I_O \leqslant$ 750 mA		–	46	240	
125 mA $\leqslant I_O \leqslant$ 375 mA		–	17	120	
Output Voltage 14.5 Vdc $\leqslant V_{in} \leqslant$ 27 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 500 mA, P $\leqslant$ 7.5 W	V_O	11.4	–	12.6	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change	ΔI_B				mA
14.5 Vdc $\leqslant V_{in} \leqslant$ 30 Vdc		–	–	1.0	
5.0 mA $\leqslant I_O \leqslant$ 750 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_N	–	75	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	$V_{in}-V_O$	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	R_O	–	75	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	175	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C $\leqslant T_A \leqslant$ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7715CP ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 250 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 50 mA)					
17.5 Vdc $\leqslant V_{in} \leqslant$ 30 Vdc		–	14	150	
20 Vdc $\leqslant V_{in} \leqslant$ 26 Vdc		–	6.0	75	
(T_J = +25°C, I_O = 250 mA)					
17.5 Vdc $\leqslant V_{in} \leqslant$ 30 Vdc		–	57	300	
20 Vdc $\leqslant V_{in} \leqslant$ 26 Vdc		–	27	150	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA $\leqslant I_O \leqslant$ 750 mA		–	68	300	
125 mA $\leqslant I_O \leqslant$ 375 mA		–	25	150	
Output Voltage 17.5 Vdc $\leqslant V_{in} \leqslant$ 30 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 500 mA, P $\leqslant$ 7.5 W	V_O	14.25	–	15.75	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change	ΔI_B				mA
17.5 Vdc $\leqslant V_{in} \leqslant$ 30 Vdc		–	–	1.0	
5.0 mA $\leqslant I_O \leqslant$ 750 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_N	–	90	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	$V_{in}-V_O$	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	R_O	–	95	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	115	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C $\leqslant T_A \leqslant$ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7718CP ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 250 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Input Regulation (T_J = +25°C, I_O = 50 mA) 21 Vdc ≤ V_{in} ≤ 33 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc (T_J = +25°C, I_O = 250 mA) 21 Vdc ≤ V_{in} ≤ 33 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc	Reg_{in}	 – – – –	 25 10 90 50	 180 90 360 180	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA 125 mA ≤ I_O ≤ 375 mA	Reg_{load}	 – –	 110 55	 360 180	mV
Output Voltage 21 Vdc ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ 7.5 W	V_O	17.1	–	18.9	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.5	8.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc 5.0 mA ≤ I_O ≤ 500 mA	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	110	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	$V_{in}-V_O$	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	R_O	–	110	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	100	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7720CP ELECTRICAL CHARACTERISTICS (V_{in} = 29 V, I_O = 250 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	19.2	20	20.8	Vdc
Input Regulation (T_J = +25°C, I_O = 50 mA) 23 Vdc ≤ V_{in} ≤ 35 Vdc 26 Vdc ≤ V_{in} ≤ 32 Vdc (T_J = +25°C, I_O = 250 mA) 23 Vdc ≤ V_{in} ≤ 35 Vdc 26 Vdc ≤ V_{in} ≤ 32 Vdc	Reg_{in}	 – – – –	 27 11 100 56	 200 100 400 200	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 750 mA 125 mA ≤ I_O ≤ 375 mA	Reg_{load}	 – –	 123 65	 400 200	mV
Output Voltage 23 Vdc ≤ V_{in} ≤ 35 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ 7.5 W	V_O	19	–	21	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.5	8.0	mA
Quiescent Current Change 23 Vdc ≤ V_{in} ≤ 35 Vdc 5.0 mA ≤ I_O ≤ 750 mA	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	130	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	80	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	58	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	$V_{in}-V_O$	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	R_O	–	123	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	90	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	-1.0	–	mV/°C

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MC7724CP ELECTRICAL CHARACTERISTICS (V_{in} = 33, I_O = 250 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 50 mA)					
27 Vdc $\leqslant V_{in} \leqslant$ 38 Vdc		–	31	240	
30 Vdc $\leqslant V_{in} \leqslant$ 36 Vdc		–	14	120	
(T_J = +25°C, I_O = 250 mA)					
27 Vdc $\leqslant V_{in} \leqslant$ 38 Vdc		–	118	480	
30 Vdc $\leqslant V_{in} \leqslant$ 36 Vdc		–	70	240	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA $\leqslant I_O \leqslant$ 500 mA		–	150	480	
125 mA $\leqslant I_O \leqslant$ 375 mA		–	85	240	
Output Voltage 27 Vdc $\leqslant V_{in} \leqslant$ 38 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 500 mA, P $\leqslant$ 7.5 W	V_O	22.8	–	25.2	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.6	8.0	mA
Quiescent Current Change	ΔI_B				mA
27 Vdc $\leqslant V_{in} \leqslant$ 38 Vdc		–	–	1.0	
5.0 mA $\leqslant I_O \leqslant$ 500 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_N	–	170	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	$V_{in}-V_O$	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	R_O	–	150	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	150	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C $\leqslant T_A \leqslant$ +125°C	TCV_O	–	-1.0	–	mV/°C

DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MC7800C Series

VOLTAGE REGULATORS

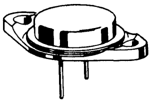
MC7800C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

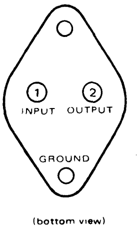
The MC7800C Series of three-terminal positive voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. Available in seven fixed output voltage options from 5.0-to-24 volts, these regulators employ internal current limiting, thermal shutdown, and safe area compensation — making them essentially blow-out proof. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. The last two digits of the part number indicate nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 199-04
  (Pin Compatible with the VERSAWATT† or TO-220)
  Or Hermetic TO-3 Type Metal Power Package (Case 11)

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

MONOLITHIC SILICON INTEGRATED CIRCUITS

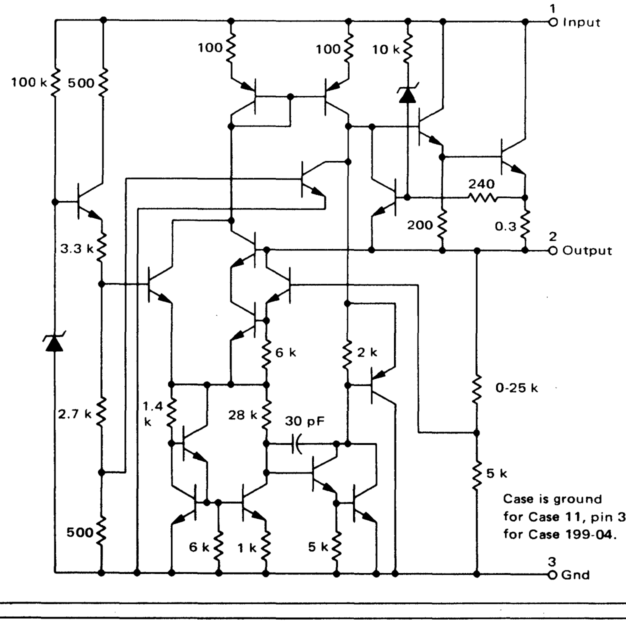




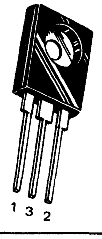
K SUFFIX
METAL PACKAGE
CASE 11
(TO-3 TYPE)

Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

SCHEMATIC DIAGRAM



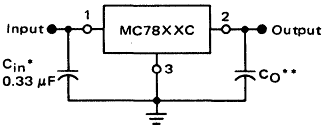
P SUFFIX
PLASTIC PACKAGE
CASE 199-04



Pin 1 Input (Base)
Pin 2 Output (Emitter)
Pin 3 Ground (Collector)

Heat sink surface connected to pin 3.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response

TYPE NO./VOLTAGE

MC7805C 5.0 Volts	MC7808C 8.0 Volts	MC7818C 18 Volts
MC7806C 6.0 Volts	MC7812C 12 Volts	MC7824C 24 Volts
	MC7815C 15 Volts	

See Packaging Information Section for outline dimensions.

†Trademark of Radio Corporation of America.

MC7800C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	2.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	20	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	50	°C/W
T_C = +25°C	P_D	15	Watts
Derate above T_C = +95°C (See Figure 1)	$1/\theta_{JC}$	500	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	2.0	°C/W
Metal Package			
T_A = +25°C	P_D	2.5	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	28.6	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	35	°C/W
T_C = +25°C	P_D	15	Watts
Derate above T_C = +65°C (See Figure 2)	$1/\theta_{JC}$	250	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	4.0	°C/W
Storage Junction Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +125	°C

MC7805C ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, $0°C < T_J < +125°C$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
7.0 Vdc $\leq V_{in} \leq$ 25 Vdc		–	7.0	50	
8.0 Vdc $\leq V_{in} \leq$ 12 Vdc		–	2.0	25	
(T_J = +25°C, I_O = 500 mA)					
7.0 Vdc $\leq V_{in} \leq$ 25 Vdc		–	35	100	
8.0 Vdc $\leq V_{in} \leq$ 12 Vdc		–	8.0	50	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA $\leq I_O \leq$ 1.5 A		–	11	100	
250 mA $\leq I_O \leq$ 750 mA		–	4.0	50	
Output Voltage (7.0 Vdc $\leq V_{in} \leq$ 20 Vdc, 5.0 mA $\leq I_O \leq$ 1.0 A, P $\leq$ 15 W)	V_O	4.75	–	5.25	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
7.0 Vdc $\leq V_{in} \leq$ 25 Vdc		–	–	1.3	
5.0 mA $\leq I_O \leq$ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leq$ f $\leq$ 100 kHz)	V_N	–	40	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	–	2.0	–	Vdc
Output Resistance	R_O	–	30	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	750	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C $\leq T_A \leq$ +125°C	TCV_O	–	-1.0	–	mV/°C

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MC7806C ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	9.0	60	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 500 mA)					
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	43	120	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		–	10	60	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	13	120	
250 mA ≤ I_O ≤ 750 mA		–	5.0	60	
Output Voltage (8.0 Vdc ≤ V_{in} ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	5.7	–	6.3	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	45	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2.0	–	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	35	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	550	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	–1.0	–	mV/°C

MC7808C ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	12	80	
11 Vdc ≤ V_{in} ≤ 17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 500 mA)					
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	50	160	
11 Vdc ≤ V_{in} ≤ 17 Vdc		–	22	80	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	26	160	
250 mA ≤ I_O ≤ 750 mA		–	9.0	80	
Output Voltage (10.5 Vdc ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	7.6	–	8.4	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	52	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2.0	–	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	40	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	450	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7812C ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc (T_J = +25°C, I_O = 500 mA) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc	Reg_{in}	 – – – –	 13 6.0 55 24	 120 60 240 120	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 46 17	 240 120	mV
Output Voltage (14.5 Vdc ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	 11.4	 –	 12.6	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	75	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	 –	 2.0	 –	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	75	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	350	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	TCV_O	 –	 -1.0	 –	mV/°C

MC7815C ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc (T_J = +25°C, I_O = 500 mA) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc	Reg_{in}	 – – – –	 14 6.0 57 27	 150 75 300 150	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 68 25	 300 150	mV
Output Voltage (17.5 Vdc ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	 14.25	 –	 15.75	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	 –	 2.0	 –	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	95	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	230	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	 –	 -1.0	 –	mV/°C

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MC7800C series (continued)

MC7818C ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^oC$)	V_O	17.3	18	18.7	Vdc
Input Regulation ($T_J = +25^oC$, I_O = 100 mA) 21 Vdc $\le V_{in} \le$ 33 Vdc 24 Vdc $\le V_{in} \le$ 30 Vdc ($T_J = +25^oC$, I_O = 500 mA) 21 Vdc $\le V_{in} \le$ 33 Vdc 24 Vdc $\le V_{in} \le$ 30 Vdc	Reg_{in}	 – – – –	 25 10 90 50	 180 90 360 180	mV
Load Regulation $T_J = +25^oC$, 5.0 mA $\le I_O \le$ 1.0 A 250 mA $\le I_O \le$ 750 mA	Reg_{load}	 – –	 110 55	 360 180	mV
Output Voltage (21 Vdc $\le V_{in} \le$ 33 Vdc, 5.0 mA $\le I_O \le$ 1.0 A, P $\le$ 15 W)	V_O	 17.1	 –	 18.9	Vdc
Quiescent Current ($T_J = +25^oC$)	I_B	–	4.5	8.0	mA
Quiescent Current Change 21 Vdc $\le V_{in} \le$ 33 Vdc 5.0 mA $\le I_O \le$ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage ($T_A = +25^oC$, 10 Hz $\le$ f $\le$ 100 kHz)	V_N	–	110	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, $T_J = +25^oC$)	V_{in}-V_O	 –	 2.0	 –	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	110	–	mΩ
Short-Circuit Current Limit ($T_J = +25^oC$)	I_{SC}	–	200	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$	TCV_O	 –	 -1.0	 –	mV/^oC

MC7824C ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^oC$)	V_O	23	24	25	Vdc
Input Regulation ($T_J = +25^oC$, I_O = 100 mA) 27 Vdc $\le V_{in} \le$ 38 Vdc 30 Vdc $\le V_{in} \le$ 36 Vdc ($T_J = +25^oC$, I_O = 500 mA) 27 Vdc $\le V_{in} \le$ 38 Vdc 30 Vdc $\le V_{in} \le$ 36 Vdc	Reg_{in}	 – – – –	 31 14 118 70	 240 120 480 240	mV
Load Regulation $T_J = +25^oC$, 5.0 mA $\le I_O \le$ 1.0 A 250 mA $\le I_O \le$ 750 mA	Reg_{load}	 – –	 150 85	 480 240	mV
Output Voltage (27 Vdc $\le V_{in} \le$ 38 Vdc, 5.0 mA $\le I_O \le$ 1.0 A, P $\le$ 15 W)	V_O	 22.8	 –	 25.2	Vdc
Quiescent Current ($T_J = +25^oC$)	I_B	–	4.6	8.0	mA
Quiescent Current Change 27 Vdc $\le V_{in} \le$ 38 Vdc 5.0 mA $\le I_O \le$ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage ($T_A = +25^oC$, 10 Hz $\le$ f $\le$ 100 kHz)	V_N	–	170	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, $T_J = +25^oC$)	V_{in}-V_O	–	2.0	–	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	150	–	mΩ
Short-Circuit Current Limit ($T_J = +25^oC$)	I_{SC}	–	150	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$	TCV_O	 –	 -1.0	 –	mV/^oC

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (CASE 199-04)

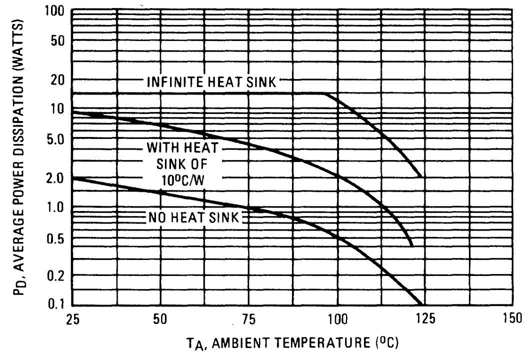


FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3 PACKAGE)

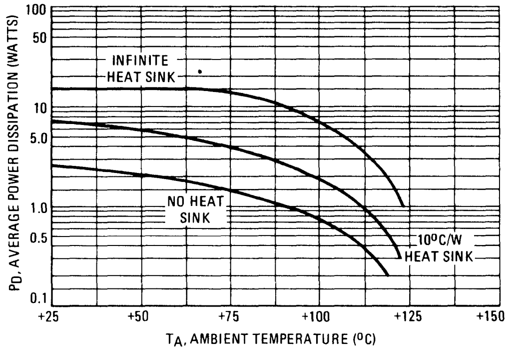


FIGURE 3 – INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE

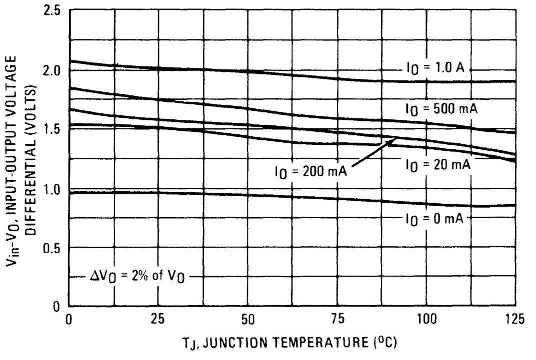


FIGURE 4 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

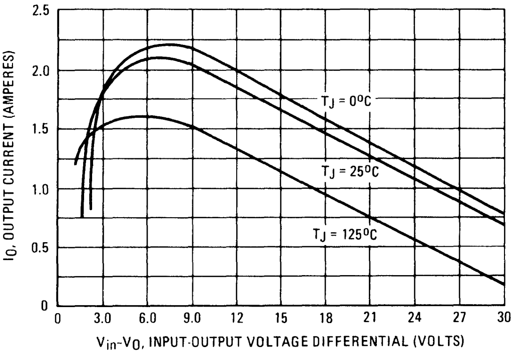


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

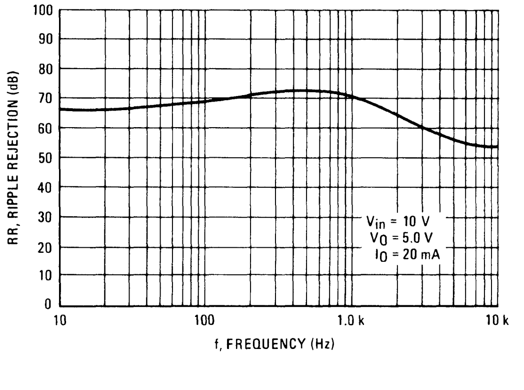
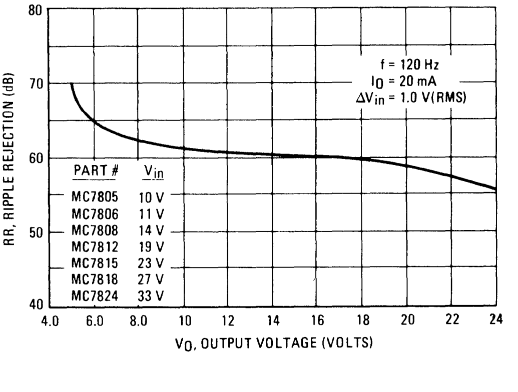


FIGURE 6 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES



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TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

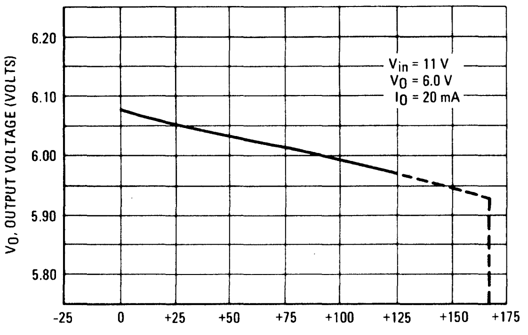


FIGURE 8 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

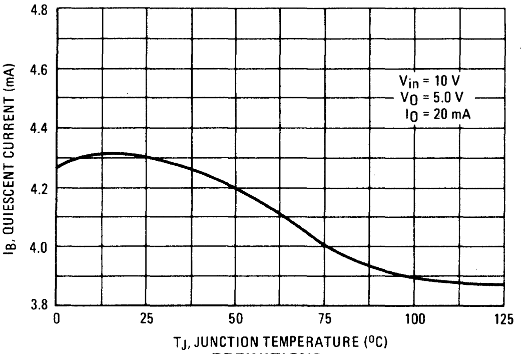
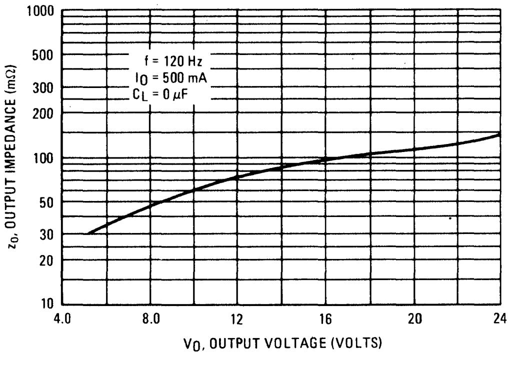


FIGURE 9 – OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

8

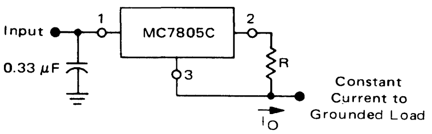
APPLICATIONS INFORMATION

Design Considerations

The MC7800C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. If an aluminum electrolytic capacitor is used, its value should be 10 μF or larger. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 10 – CURRENT REGULATOR



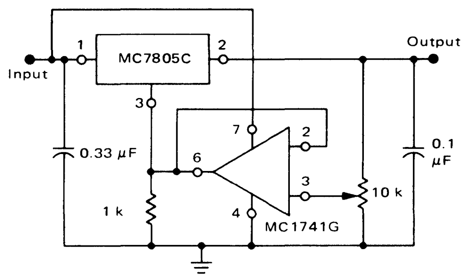
The MC7800C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_Q$$

I_Q = 1.5 mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

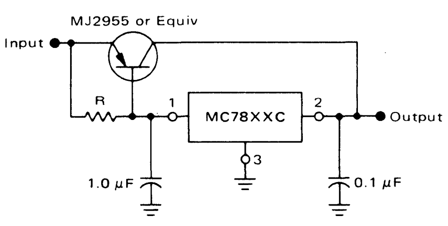
FIGURE 11 – ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
$V_{IN} - V_O \geqslant 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

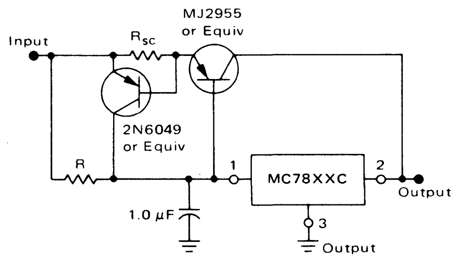
FIGURE 12 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC7800C series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 13 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 12 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

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MC7900C Series

NEGATIVE VOLTAGE REGULATORS

MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

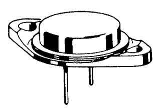
The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

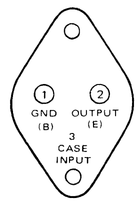
Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation – making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 199-04
  (Pin Compatible with the VERSAWATT† or TO-220)
  Or Hermetic TO-3 Type Metal Power Package

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

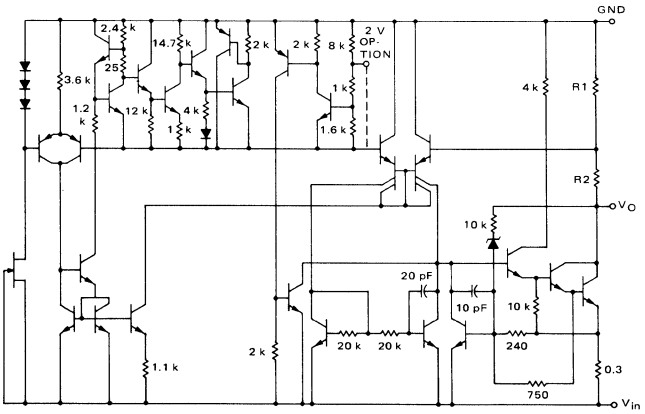
MONOLITHIC SILICON INTEGRATED CIRCUITS



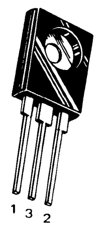


K SUFFIX
METAL PACKAGE
CASE 11
(TO-3 TYPE)

SCHEMATIC DIAGRAM



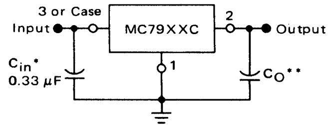
P SUFFIX
PLASTIC PACKAGE
CASE 199-04



Pin 1 GND (B)
Pin 2 Output (E)
Pin 3 Input (C)

Heat sink surface connected to pin 3.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C - 2.0 Volts	MC7906C - 6.0 Volts	MC7915C - 15 Volts
MC7905C - 5.0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C - 5.2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

†Trademark of Radio Corporation of America.

See Packaging Information Section for outline dimensions.

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MC7900C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.0 V – 18 V) (24 V)	V_{in}	-35 -40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	2.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	20	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	50	°C/W
T_C = +25°C	P_D	15	Watts
Derate above T_C = +95°C (See Figure 1)	$1/\theta_{JC}$	500	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	2.0	°C/W
Metal Package			
T_A = +25°C	P_D	2.5	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	28.6	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	35	°C/W
T_C = +25°C	P_D	15	Watts
Derate above T_C = +65°C	$1/\theta_{JC}$	250	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	4.0	°C/W
Storage Junction Temperature Range	T_{stg}	-20 to +150	°C
Operating Junction Temperature Range	T_J	0 to +125	°C

MC7902C ELECTRICAL CHARACTERISTICS (V_{in} = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-1.92	-2.00	-2.08	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.0 Vdc $\geq V_{in} \geq$ -25 Vdc		–	8.0	20	
-8.0 Vdc $\geq V_{in} \geq$ -12 Vdc		–	4.0	10	
(T_J = +25°C, I_O = 500 mA)					
-7.0 Vdc $\geq V_{in} \geq$ -25 Vdc		–	18	40	
-8.0 Vdc $\geq V_{in} \geq$ -12 Vdc		–	8.0	20	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA $\leq I_O \leq$ 1.5 A		–	70	120	
250 mA $\leq I_O \leq$ 750 mA		–	20	60	
Output Voltage -7.0 Vdc $\geq V_{in} \geq$ -20 Vdc, 5.0 mA $\leq I_O \leq$ 1.0 A, P $\leq$ 15 W	V_O	-1.90	–	-2.10	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
-7.0 Vdc $\geq V_{in} \geq$ -25 Vdc		–	–	1.3	
5.0 mA $\leq I_O \leq$ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leq$ f $\leq$ 100 kHz)	V_N	–	40	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_{in}-V_O \rvert$	–	3.5	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C $\leq T_A \leq$ +125°C	TCV_O	–	-1.0	–	mV/°C

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MC7905C ELECTRICAL CHARACTERISTICS (V_{in} = -10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.8	-5.0	-5.2	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.0 Vdc $\geqslant V_{in} \geqslant$ -25 Vdc		–	7.0	50	
-8.0 Vdc $\geqslant V_{in} \geqslant$ -12 Vdc		–	2.0	25	
(T_J = +25°C, I_O = 500 mA)					
-7.0 Vdc $\geqslant V_{in} \geqslant$ -25 Vdc		–	35	100	
-8.0 Vdc $\geqslant V_{in} \geqslant$ -12 Vdc		–	8.0	50	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	11	100	
250 mA $\leqslant I_O \leqslant$ 750 mA		–	4.0	50	
Output Voltage -7.0 Vdc $\geqslant V_{in} \geqslant$ -20 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 1.0 A, P $\leqslant$ 15 W	V_O	-4.75	–	-5.25	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
-7.0 Vdc $\geqslant V_{in} \geqslant$ -25 Vdc		–	–	1.3	
5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_N	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\|V_{in}-V_O\|$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C $\leqslant T_A \leqslant$ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7905.2C ELECTRICAL CHARACTERISTICS (V_{in} = -10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.0	-5.2	-5.4	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.2 Vdc $\geqslant V_{in} \geqslant$ -25 Vdc		–	8.0	52	
-8.0 Vdc $\geqslant V_{in} \geqslant$ -12 Vdc		–	2.2	27	
(T_J = +25°C, I_O = 500 mA)					
-7.2 Vdc $\geqslant V_{in} \geqslant$ -25 Vdc		–	37	105	
-8.0 Vdc $\geqslant V_{in} \geqslant$ -12 Vdc		–	8.5	52	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	12	105	
250 mA $\leqslant I_O \leqslant$ 750 mA		–	4.5	52	
Output Voltage -7.2 Vdc $\geqslant V_{in} \geqslant$ -20 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 1.0 A, P $\leqslant$ 15 W	V_O	-4.94	–	-5.46	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
-7.2 Vdc $\geqslant V_{in} \geqslant$ -25 Vdc		–	–	1.3	
5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_N	–	42	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	68	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\|V_{in}-V_O\|$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C $\leqslant T_A \leqslant$ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7906C ELECTRICAL CHARACTERISTICS (V_{in} = -11 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.75	-6.0	-6.25	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-8.0 Vdc ⩾ V_{in} ⩾ -25 Vdc		–	9.0	60	
-9.0 Vdc ⩾ V_{in} ⩾ -13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 500 mA)					
-8.0 Vdc ⩾ V_{in} ⩾ -25 Vdc		–	43	120	
-9.0 Vdc ⩾ V_{in} ⩾ -13 Vdc		–	10	60	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ⩽ I_O ⩽ 1.5 A		–	13	120	
250 mA ⩽ I_O ⩽ 750 mA		–	5.0	60	
Output Voltage -8.0 Vdc ⩾ V_{in} ⩾ -21 Vdc, 5.0 mA ⩽ I_O ⩽ 1.0 A, P ⩽ 15 W)	V_O	-5.7	–	-6.3	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
-8.0 Vdc ⩾ V_{in} ⩾ -25 Vdc		–	–	1.3	
5.0 mA ⩽ I_O ⩽ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ⩽ f ⩽ 100 kHz)	V_N	–	45	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_{in}-V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ⩽ T_A ⩽ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7908C ELECTRICAL CHARACTERISTICS (V_{in} = -14 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-7.7	-8.0	-8.3	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-10.5 Vdc ⩾ V_{in} ⩾ -25 Vdc		–	12	80	
-11 Vdc ⩾ V_{in} ⩾ -17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 500 mA)					
-10.5 Vdc ⩾ V_{in} ⩾ -25 Vdc		–	50	160	
-11 Vdc ⩾ V_{in} ⩾ -17 Vdc		–	22	80	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ⩽ I_O ⩽ 1.5 A		–	26	160	
250 mA ⩽ I_O ⩽ 750 mA		–	9.0	80	
Output Voltage -10.5 Vdc ⩾ V_{in} ⩾ -23 Vdc, 5.0 mA ⩽ I_O ⩽ 1.0 A, P ⩽ 15 W	V_O	-7.6	–	-8.4	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
-10.5 Vdc ⩾ V_{in} ⩾ -25 Vdc		–	–	1.0	
5.0 mA ⩽ I_O ⩽ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ⩽ f ⩽ 100 kHz)	V_N	–	52	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_{in}-V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ⩽ T_A ⩽ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7912C ELECTRICAL CHARACTERISTICS (V_{in} = -19 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.5	-12	-12.5	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) -14.5 Vdc ≥ V_{in} ≥ -30 Vdc -16 Vdc ≥ V_{in} ≥ -22 Vdc (T_J = +25°C, I_O = 500 mA) -14.5 Vdc ≥ V_{in} ≥ -30 Vdc -16 Vdc ≥ V_{in} ≥ -22 Vdc	Reg_{in}	 – – – –	 13 6.0 55 24	 120 60 240 120	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 46 17	 240 120	mV
Output Voltage -14.5 Vdc ≥ V_{in} ≥ -27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-11.4	–	-12.6	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change -14.5 Vdc ≥ V_{in} ≥ -30 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	75	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\|V_{in}-V_O\|$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7915C ELECTRICAL CHARACTERISTICS (V_{in} = -23 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.4	-15	-15.6	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) -17.5 Vdc ≥ V_{in} ≥ -30 Vdc -20 Vdc ≥ V_{in} ≥ -26 Vdc (T_J = +25°C, I_O = 500 mA) -17.5 Vdc ≥ V_{in} ≥ -30 Vdc -20 Vdc ≥ V_{in} ≥ -26 Vdc	Reg_{in}	 – – – –	 14 6.0 57 27	 150 75 300 150	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 68 25	 300 150	mV
Output Voltage -17.5 Vdc ≥ V_{in} ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-14.25	–	-15.75	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change -17.5 Vdc ≥ V_{in} ≥ -30 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\|V_{in}-V_O\|$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	-1.0	–	mV/°C

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MC7918C ELECTRICAL CHARACTERISTICS (V_{in} = -27 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^oC$)	V_O	-17.3	-18	-18.7	Vdc
Input Regulation	Reg_{in}				mV
($T_J = +25^oC$, I_O = 100 mA)					
-21 Vdc $\geq V_{in} \geq$ -33 Vdc		–	25	180	
-24 Vdc $\geq V_{in} \geq$ -30 Vdc		–	10	90	
($T_J = +25^oC$, I_O = 500 mA)					
-21 Vdc $\geq V_{in} \geq$ -33 Vdc		–	90	360	
-24 Vdc $\geq V_{in} \geq$ -30 Vdc		–	50	180	
Load Regulation	Reg_{load}				mV
$T_J = +25^oC$, 5.0 mA $\leq I_O \leq$ 1.0 A		–	110	360	
250 mA $\leq I_O \leq$ 750 mA		–	55	180	
Output Voltage -21 Vdc $\geq V_{in} \geq$ -33 Vdc, 5.0 mA $\leq I_O \leq$ 1.0 A, P $\leq$ 15 W	V_O	-17.1	–	-18.9	Vdc
Quiescent Current ($T_J = +25^oC$)	I_B	–	4.5	8.0	mA
Quiescent Current Change	ΔI_B				mA
-21 Vdc $\geq V_{in} \geq$ -33 Vdc		–	–	1.0	
5.0 mA $\leq I_O \leq$ 1.0 A		–	–	0.5	
Output Noise Voltage ($T_A = +25^oC$, 10 Hz $\leq f \leq$ 100 kHz)	V_N	–	110	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential I_O = 1.0 A, $T_J = +25^oC$	$\|V_{in}-V_O\|$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$	TCV_O	–	-1.0	–	mV/^oC

MC7924C ELECTRICAL CHARACTERISTICS (V_{in} = -33 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^oC$)	V_O	-23	-24	-25	Vdc
Input Regulation	Reg_{in}				mV
($T_J = +25^oC$, I_O = 100 mA)					
-27 Vdc $\geq V_{in} \geq$ -38 Vdc		–	31	240	
-30 Vdc $\geq V_{in} \geq$ -36 Vdc		–	14	120	
($T_J = +25^oC$, I_O = 500 mA)					
-27 Vdc $\geq V_{in} \geq$ -38 Vdc		–	118	480	
-30 Vdc $\geq V_{in} \geq$ -36 Vdc		–	70	240	
Load Regulation	Reg_{load}				mV
$T_J = +25^oC$, 5.0 mA $\leq I_O \leq$ 1.0 A		–	150	480	
250 mA $\leq I_O \leq$ 750 mA		–	85	240	
Output Voltage -27 Vdc $\geq V_{in} \geq$ -38 Vdc, 5.0 mA $\leq I_O \leq$ 1.0 A, P $\leq$ 15 W	V_O	-22.8	–	-25.2	Vdc
Quiescent Current ($T_J = +25^oC$)	I_B	–	4.6	8.0	mA
Quiescent Current Change	ΔI_B				mA
-27 Vdc $\geq V_{in} \geq$ -38 Vdc		–	–	1.0	
5.0 mA $\leq I_O \leq$ 1.0 A		–	–	0.5	
Output Noise Voltage ($T_A = +25^oC$, 10 Hz $\leq f \leq$ 100 kHz)	V_N	–	170	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential I_O = 1.0 A, $T_J = +25^oC$	$\|V_{in}-V_O\|$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$	TCV_O	–	-1.0	–	mV/^oC

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (CASE 199-04)

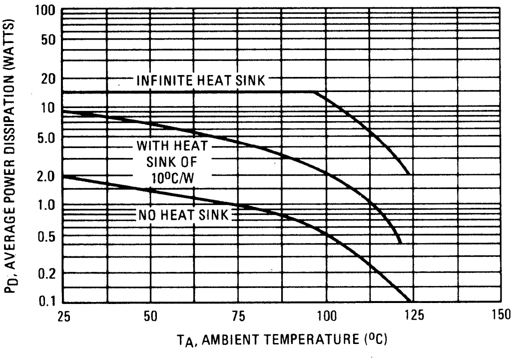


FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3 TYPE PACKAGE)

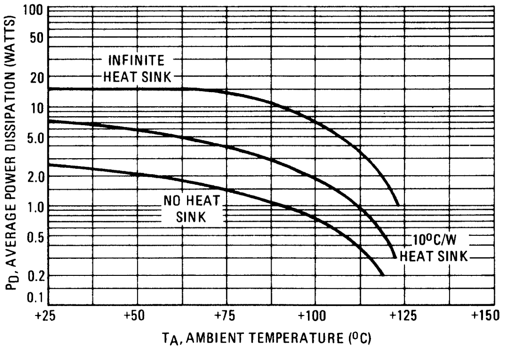


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

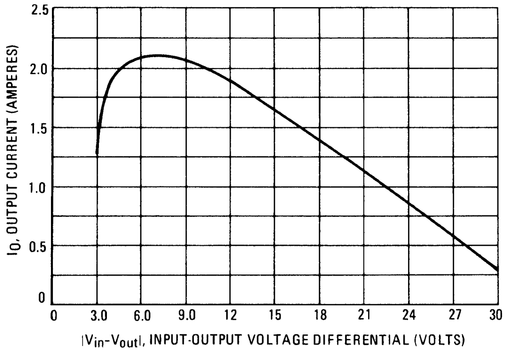


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

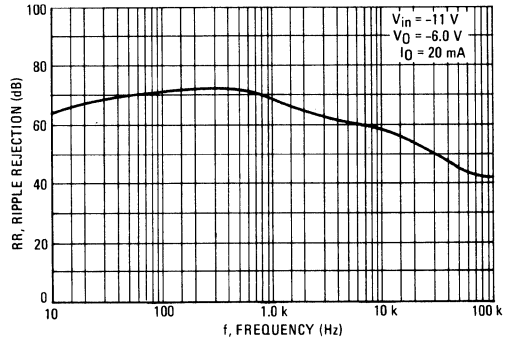


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

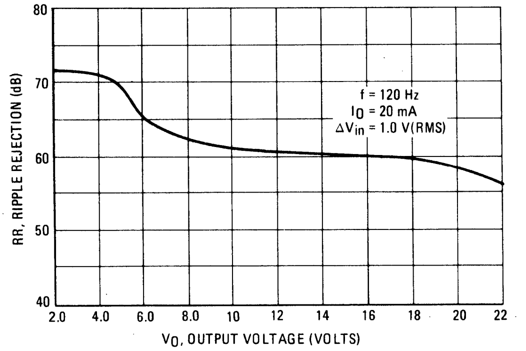
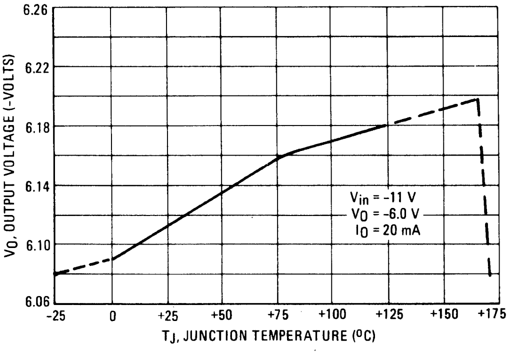


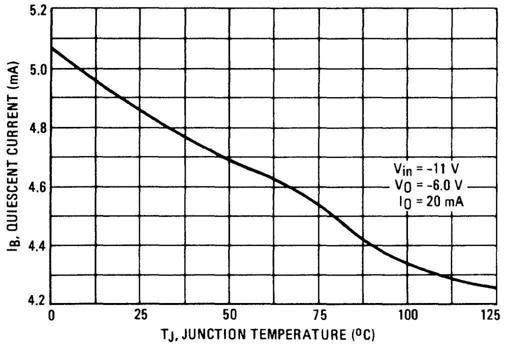
FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



8

TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

8

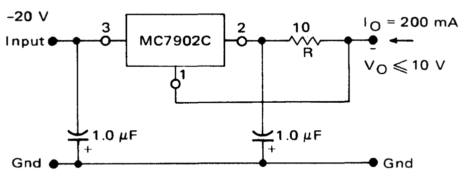
APPLICATIONS INFORMATION

Design Considerations

The MC7900C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. If an aluminum electrolytic capacitor is used, its value should be 1.0 μF or larger. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 – CURRENT REGULATOR

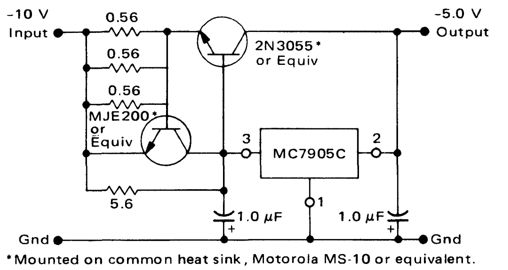


The MC7902, -2.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{2\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 2.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

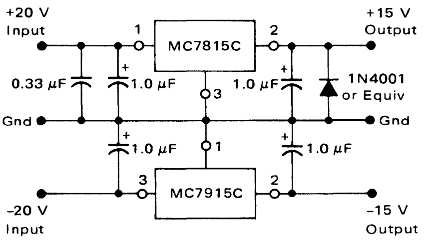
FIGURE 9 – CURRENT BOOST REGULATOR
(-5.0 V @ 4.0 A, with 5.0 A current limiting)



*Mounted on common heat sink, Motorola MS-10 or equivalent.

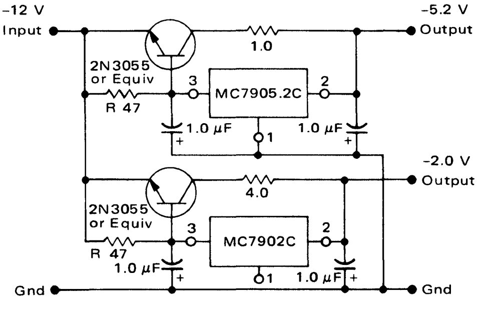
When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

FIGURE 10 – OPERATIONAL AMPLIFIER SUPPLY
(±15 V @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems.

FIGURE 11 – TYPICAL MECL SYSTEM POWER SUPPLY
(-5.2 V @ 4.0 A and -2.0 V @ 2.0 A; for PC Board)



When current-boost power transistors are used, 47-ohm base-to-emitter resistors (R) must be used to bypass the quiescent current at no load. These resistors, in conjunction with the V_{BE} of the NPN transistors, determine when the pass transistors begin conducting. The 1-ohm and 4-ohm dropping resistors were chosen to reduce the power dissipated in the boost transistors but still leave at least 2.0 V across these devices for good regulation.

MC55107
MC55108
MC75107
MC75108

DUAL LINE RECEIVERS

MONOLITHIC DUAL LINE RECEIVERS

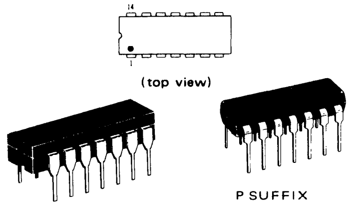
The MC55107/MC75107 and MC55108/MC75108 are MTTL compatible dual line receivers featuring independent channels with common voltage supply and ground terminals. The MC55107/MC75107 circuit features an active pull-up (totem-pole) output. The MC55108/MC75108 circuit features an open-collector output configuration that permits the Wired-OR logic connection with similar outputs (such as the MC5401/MC7401 MTTL gate or additional MC55108/MC75108 receivers). Thus a level of logic is implemented without extra delay.

The MC55107/MC75107 and MC55108/MC75108 circuits are designed to detect input signals of greater than 25 millivolts amplitude and convert the polarity of the signal into appropriate MTTL compatible output logic levels.

- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Voltage Range of ±3.0 V
- Differential Input Common-Mode Voltage of More Than ±15 V Using External Attenuator
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- MTTL or MDTL Drive Capability
- High DC Noise Margins

DUAL LINE RECEIVERS

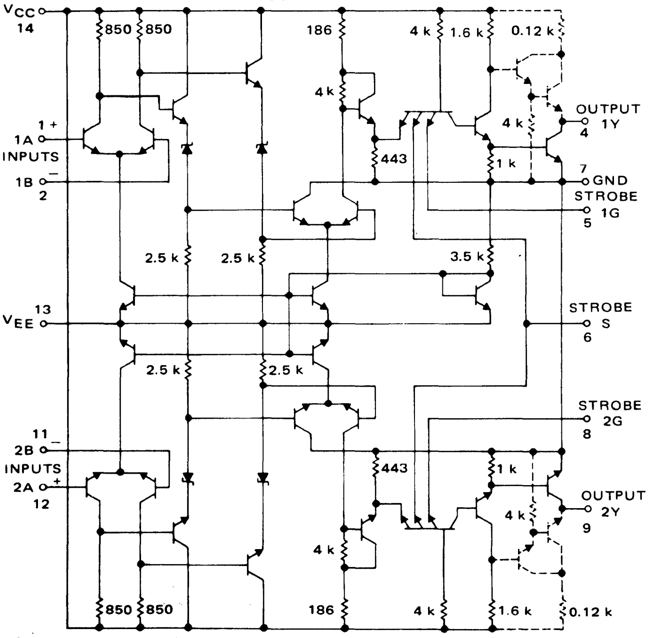
MONOLITHIC SILICON INTEGRATED CIRCUITS



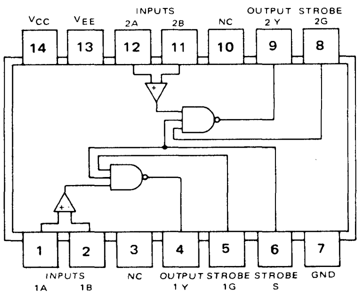
L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC75107, MC75108 only)

CIRCUIT SCHEMATIC



Components shown with dashed lines are applicable to the MC55107 and MC75107 only.



TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS ($T_A = T_{low}$* to T_{high}* unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+7.0 -7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{ID}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation) Plastic and Ceramic Dual-In-Line Packages Derate above $T_A = +25^oC$	P_D	 625 3.85	 mW mW/°C
Operating Temperature Range MC55107, MC55108 MC75107, MC75108	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	MC55107, MC55108 Min	MC55107, MC55108 Typ	MC55107, MC55108 Max	MC75107, MC75108 Min	MC75107, MC75108 Typ	MC75107, MC75108 Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.5 -4.5	+5.0 -5.0	+5.5 -5.5	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Sink Current	I_{OS}		–	-16		–	-16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0		+5.0	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	-3.0	–	+3.0	Vdc
Input Voltage Range, any differential input to ground	V_{IR}	-5.0	–	+3.0	-5.0		+3.0	Vdc
Operating Temperature Range	T_A	-55	–	+125	0	–	+70	°C

DEFINITIONS OF INPUT LOGIC LEVELS

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (between differential inputs)	V_{IDH}	1	0.025	5.0	Vdc
Low-Level Input Voltage (between differential inputs)	V_{IDL}	1	-5.0†	-0.025	Vdc
High-Level Input Voltage (at strobe inputs)	$V_{IH(S)}$	3	2.0	5.5	Vdc
Low-Level Input Voltage (at strobe inputs)	$V_{IL(S)}$	3	0	0.8	Vdc

†The algebraic convention, where the most positive limit is designated maximum, is used with Low-Level Input Voltage Level (V_{IDL})

ELECTRICAL CHARACTERISTICS ($T_A = T_{low}$* to T_{high}* unless otherwise noted)

Characteristic	Symbol	Test Fig.	MC55107,MC75107 Min	MC55107,MC75107 Typ #	MC55107,MC75107 Max	MC55108,MC75108 Min	MC55108,MC75108 Typ #	MC55108,MC75108 Max	Unit
High-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = 0.5 V, V_{IC} = -3.0 V to +3.0 V) ‡	I_{IH}	2	–	30	75	–	30	75	μA
Low-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = -2.0 V, V_{IC} = -3.0 V to +3.0 V) ‡	I_{IL}	2	–	–	-10	–	–	-10	μA
High-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V)‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max)‡	I_{IH}	4	 – –	 – –	 40 1.0	 – –	 – –	 40 1.0	 μA mA
Low-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V)‡	I_{IL}	4	–	–	-1.6	–	–	-1.6	mA
High-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V)‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max)‡	I_{IH}	4	 – –	 – –	 80 2.0	 – –	 – –	 80 2.0	 μA mA
Low-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V)‡	I_{IL}	4	–	–	-3.2	–	–	-3.2	mA
High-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{load} = −400 μA, V_{IC} = -3.0 V to +3.0 V)‡	V_{OH}	3	2.4	–	–	–	–	–	V
Low-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{sink} = 16 mA V_{IC} = -3.0 V to +3.0 V)‡	V_{OL}	3	–	–	0.4	–	–	0.4	V
High-Level Leakage Current (V_{CC} = Min, V_{EE} = Min, V_{OH} = V_{CC} Max)‡	I_{CEX}	3	–	–	–	–	–	250	μA
Short-Circuit Output Current # # (V_{CC} = Max, V_{EE} = Max)‡	I_{OSC}	5	-18	–	-70	–	–	–	mA
High Logic Level Supply Current from V_{CC} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C) ‡	I_{CCH+}	6	–	18	30	–	18	30	mA
High Logic Level Supply Current from V_{EE} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C)‡	I_{CCH-}	6	0	-8.4	-15	0	8.4	-15	mA

‡For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.

#Not more than one output should be shorted at a time.

*T_{low} = 55°C for MC55107 and MC55108, = 0 for MC75107 and MC75108

T_{high} = +125°C for MC55107 and MC55108 = +70°C for MC75107 and MC75108

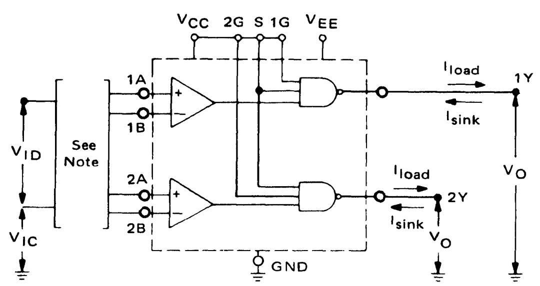
8

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = +25°C)

Characteristic	Symbol	Test Fig.	MC55107,MC75107			MC55108,MC75109			Unit
			Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time, low-to-high level from differential inputs A and B to output	$t_{PLH(D)}$	7							ns
(R_L = 390 Ω, C_L = 50 pF)			–	17	25	–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	–	–	–	19	25	
Propagation Delay Time, high-to-low level from differential inputs A and B to output	$t_{PHL(D)}$	7							ns
(R_L = 390 Ω, C_L = 50 pF)			–	17	25	–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	–	–	–	19	25	
Propagation Delay Time, low-to-high level, from strobe input to G or S output	$t_{PLH(S)}$	7							ns
(R_L = 390 Ω, C_L = 50 pF)			–	10	15	–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	–	–	–	13	20	
Propagation Delay Time, high-to-low level, from strobe input G or S to output	$t_{PHL(S)}$	7							ns
(R_L = 390 Ω, C_L = 50 pF)			–	8.0	15	–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	–	–	–	13	20	

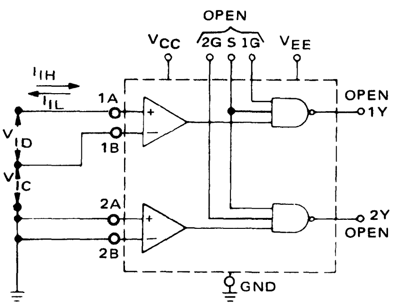
TEST CIRCUITS

FIGURE 1 – V_{IDH} and V_{IDL}



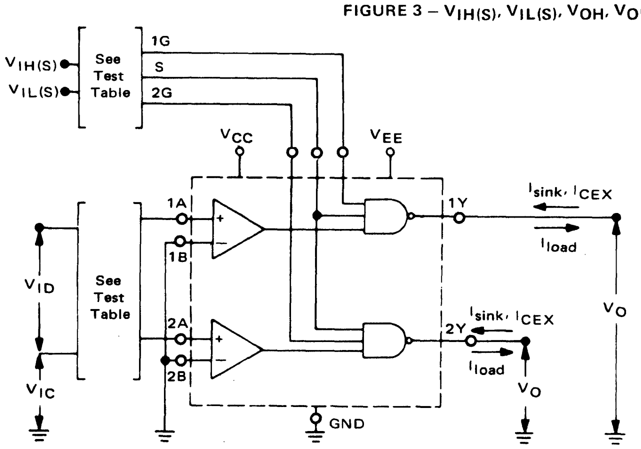
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 2 – I_{IH} and I_{IL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded

FIGURE 3 – $V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, and I_{OH}



TEST TABLE

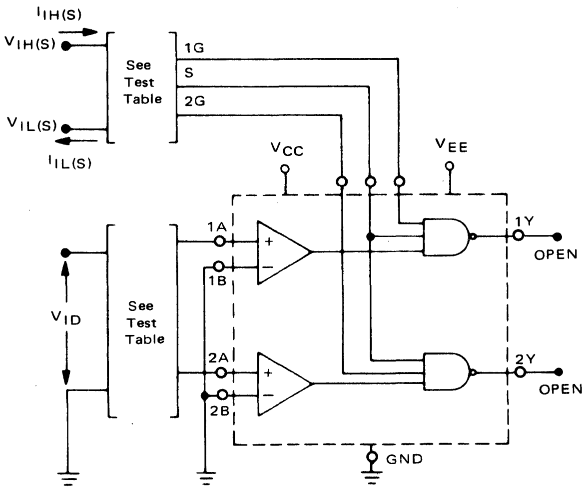
MC55107 MC75107	MC55108 MC75108	V_{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V_{OH}	I_{CEX}	+25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	−25 mV	$V_{IL(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	−25 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	V_{OL}	−25 mV	$V_{IH(S)}$	$V_{IH(S)}$

NOTES: 1. V_{IC} = −3.0 V to +3.0 V.
2. When testing one channel, the inputs of the other channel should be grounded.

8

TEST CIRCUITS (continued)

FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$



TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH(S)}$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH(S)}$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH(S)}$	Gnd
I_{IL} at Strobe 1G	-25 mV	Gnd	$V_{IL(S)}$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	-25 mV	Gnd	4.5 V	$V_{IL(S)}$
I_{IL} at Strobe S	-25 mV	-25 mV	4.5 V	$V_{IL(S)}$	4.5 V

FIGURE 5 – I_{OS}

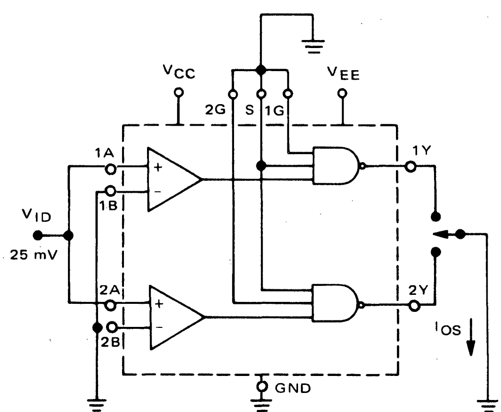
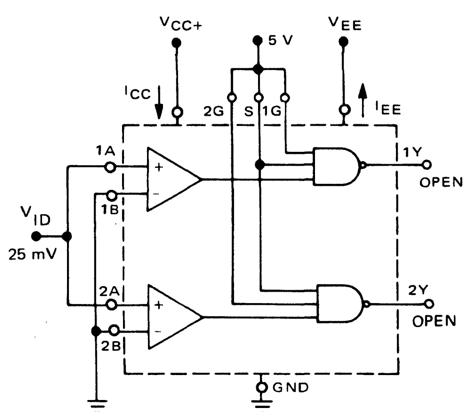


FIGURE 6 – I_{CC} and I_{EE}

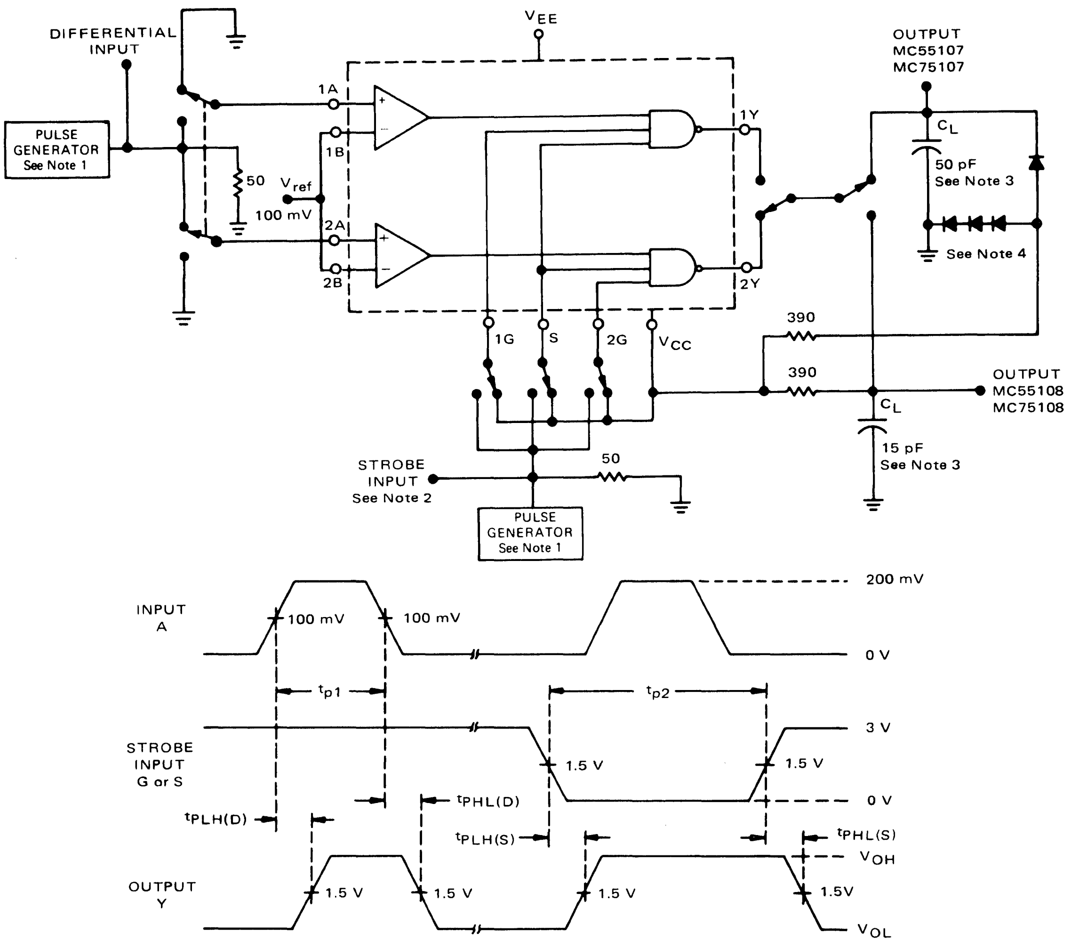


NOTES: 1. Each channel is tested separately.
2. Not more than one output should be tested at one time.

8

TEST CIRCUITS (continued)

FIGURE 7 – PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS

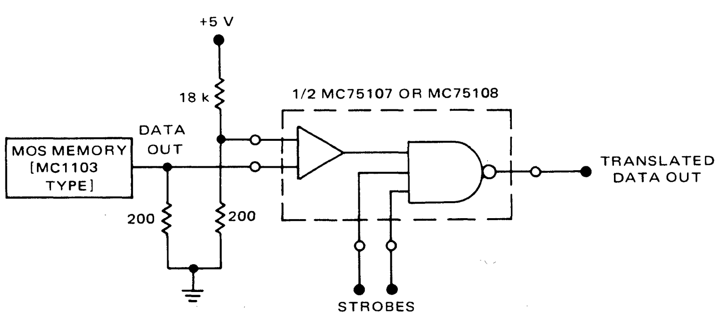


NOTES: 1. The pulse generators have the following characteristics: $z_o = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz $t_{p2} = 1$ ms, PRR = 500 kHz.

2. Strobe input pulse is applied to Strobe 1G when Inputs 1A-1B are being tested, to Strobe S when Inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916 or equivalent.

TYPICAL APPLICATION

FIGURE 8 – MOS-TO-TTL TRANSLATOR



8

MC55325
MC75325

DUAL MEMORY DRIVER

DUAL MEMORY DRIVER

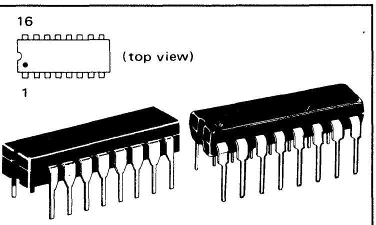
The MC55325/75325 is a monolithic integrated circuit memory driver with logic inputs, and is designed for use with magnetic memories.

The device contains two 600-mA source-switch pairs and two 600-mA sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. With this arrangement selection of one of the four switches provides turn-on with minimum time skew of the output current rise.

- 600-mA Output Capability
- Output Short-Circuit Protection
- Input Clamp Diodes
- Dual Sink and Dual Source Outputs
- MDTL and MTTL Compatibility
- 24-Volt Output Capability

DUAL MEMORY DRIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT



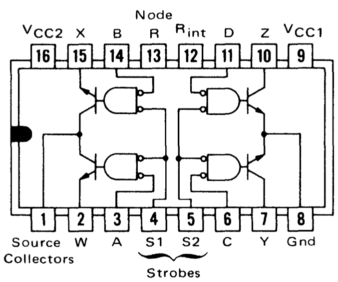
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC75325 only)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage (Note 1)	V_{CC1} V_{CC2}	7.0 25	Vdc Vdc
Input Voltage	V_{in}	5.5	Vdc
Power Dissipation (Package Limitation) Ceramic and Plastic Dual In-Line Pkg. Derate above T_A = +25°C	P_D	 1.0 6.6	 W mW/°C
Operating Temperature Range MC55325 MC75325	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. Voltage values are with respect to the network ground terminal.



SWITCHING CHARACTERISTICS (V_{CC1} = 5.0 V, C_L = 25 pF, T_A = 25°C)

Characteristic		Symbol	ns Typ	ns Max
Propagation Delay Time to Source Collectors (V_{CC2} = 15 V, R_L = 24 ohms)	Low-to-High-Level Output High-to-Low-Level Output	t_{PLH} t_{PHL}	25 25	50 50
Transition Time to Source Outputs (V_{CC2} = 20 V, R_L = 1 k ohms)	Low-to-High-Level Output High-to-Low-Level Output	t_{TLH} t_{THL}	55 7.0	– –
Propagation Delay Time to Sink Outputs (V_{CC2} = 15 V, R_L = 24 ohms)	Low-to-High-Level Output High-to-Low-Level Output	t_{PLH} t_{PHL}	20 20	45 45
Transition Time to Sink Outputs (V_{CC2} = 15 V, R_L = 24 ohms)	Low-to-High-Level Output High-to-Low-Level Output	t_{TLH} t_{THL}	7.0 9.0	15 20
Storage Time to Sink Outputs (V_{CC2} = 15 V, R_L = 24 ohms)		t_s	15	30

TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	On	Off	Off	Off
H	L	X	X	L	H	Off	On	Off	Off
X	X	L	H	H	L	Off	Off	On	Off
X	X	H	L	H	L	Off	Off	Off	On
X	X	X	X	H	H	Off	Off	Off	Off
H	H	H	H	X	X	Off	Off	Off	Off

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

This is advance information on a new introduction and specifications are subject to change without notice.

See Packaging Information Section for outline dimensions.

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ELECTRICAL CHARACTERISTICS ($T_A = T_{low}$# to T_{high}# unless otherwise noted.

Characteristic		Symbol	MC55325 Min	MC55325 Typ*	MC55325 Max	MC75325 Min	MC75325 Typ*	MC75325 Max	Unit
High-Level Input Voltage		V_{IH}	2.0	–	–	2.0	–	–	V
Low-Level Input Voltage		V_{IL}	–	–	0.8	–	–	0.8	V
Input Clamp Voltage (V_{CC1} = 4.5 V, V_{CC2} = 24 V, I_I = -10 mA, T_A = 25°C)		V_I	–	-1.3	-1.7	–	-1.3	-1.7	V
Off-State Current, Source-Collectors Terminal (V_{CC1} = 4.5 V, V_{CC2} = 24 V)	$T_A = T_{low}$ to T_{high}	I_{off}	–	–	500	–	–	200	μA
	T_A = 25°C		–	3.0	150	–	3.0	200	
High-Level Sink Output Voltage (V_{CC1} = 4.5 V, V_{CC2} = 24 V, I_O = 0)		V_{OH}	19	23	–	19	23	–	V
Saturation Voltage**		V_{sat}							V
Source Outputs (V_{CC1} = 4.5 V, V_{CC2} = 15 V, I_{source} ≈ -600 mA, R_L = 24 ohms, Note 2)	$T_A = T_{low}$ to T_{high}		–	–	0.9	–	–	0.9	
	T_A = 25°C		–	0.43	–	–	0.43	–	
Sink Outputs (V_{CC1} = 4.5 V, V_{CC2} = 15 V, I_{sink} ≈ 600 mA, R_L = 24 ohms, Note 2)	$T_A = T_{low}$ to T_{high}		–	–	0.9	–	–	0.9	
	T_A = 25°C		–	0.43	–	–	0.43	–	
Input Current at Maximum Input Voltage (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 5.5 V)	Address Inputs	I_I	–	–	1.0	–	–	1.0	mA
	Strobe Inputs		–	–	2.0	–	–	2.0	
High-Level Input Current (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 2.4 V)	Address Inputs	I_{IH}	–	3.0	40	–	3.0	40	μA
	Strobe Inputs		–	6.0	80	–	6.0	80	
Low-Level Input Current (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 0.4 V)	Address Inputs	I_{IL}	–	-1.0	-1.6	–	-1.0	-1.6	mA
	Strobe Inputs		–	-2.0	-3.2	–	-2.0	-3.2	
Supply Current, All Sources and Sinks "Off" (V_{CC1} = 5.5 V, V_{CC2} = 24 V, T_A = 25°C)	From V_{CC1}	$I_{CC(off)}$	–	14	22	–	14	22	mA
	From V_{CC2}		–	7.5	20	–	7.5	20	
Supply Current from V_{CC1}, Either Sink "On" (V_{CC1} = 5.5 V, V_{CC2} = 24 V, I_{sink} = 50 mA, T_A = 25°C)		I_{CC1}	–	55	70	–	55	70	mA
Supply Current from V_{CC2}, Either Source "On" (V_{CC1} = 5.5 V, V_{CC2} = 24 V, I_{source} = -50 mA, T_A = 25°C)		I_{CC2}	–	32	50	–	32	50	mA

*All typical values are at T_A = 25°C.

**Not more than one output is to be "on" at any one time.

T_{low} = -55°C for MC55325, 0°C for MC75325

T_{high} = +125°C for MC55325, +70°C for MC75325

NOTE 2. Saturation voltage must be measured using pulse techniques: pulse width = 200 μs, duty cycle ⩽ 2%.

8

MC75109
MC75110

DUAL LINE DRIVERS

MONOLITHIC DUAL LINE DRIVERS

The MC75109 and MC75110 dual line drivers feature independent channels with common voltage supply and ground terminals. Each driver circuit provides a constant output current that switches to either of two output terminals subject to the appropriate logic levels at the input terminals. Output current can be switched "off" (inhibited) by appropriate logic levels at the inhibit inputs. Output current is nominally six milliamperes for the MC75109 and twelve millamperes for the MC75110.

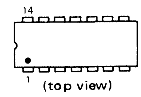
The inhibit feature permits use in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included to increase driver-logic versatility. With output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading occurs when the driver is used in a party-line system with other drivers. Output impedance of the driver in inhibited mode is very high (the output impedance of a transistor biased to cutoff).

All driver outputs have a common-mode voltage range of -3.0 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

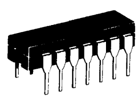
- Insensitive to Supply Variations Over the Entire Operating Range
- MTTL Input Compatibility
- Current-Mode Output (6.0 mA or 12 mA typical)
- High Output Impedance
- High Common-Mode Output Voltage Range (-3.0 V to +10 V)
- Inhibitor Available for Driver Selection

DUAL LINE DRIVERS

MONOLITHIC SILICON INTEGRATED CIRCUIT

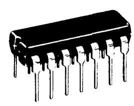


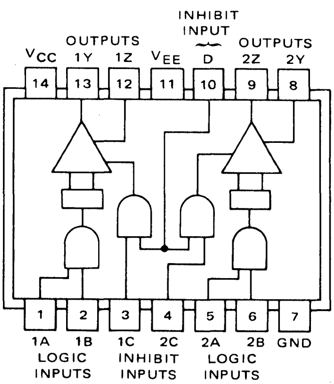
(top view)



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

P SUFFIX
PLASTIC PACKAGE
CASE 646





TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the "on" state.
High output represents the "off" state.

See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltages (See Note 1)	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages (See Note 1)	V_{in}	5.5	Volts
Common-Mode Output Voltage Range (See Note 1)	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 1000 3.85	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Ceramic Dual In-Line Package Plastic Dual In-Line Package	T_{stg}	 -65 to +150 -55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range Positive Negative	V_{OCR}	 0 0	 – –	 +10 -3.0	Volts

Note 1. These voltage values are in respect to the ground terminal.
Note 2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	1,2	2.0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	1,2	0	0.8	Volts

* The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

ELECTRICAL CHARACTERISTICS (T_A · 0 to +70°C unless otherwise noted.)

Characteristic ##	Symbol	Test Fig.	MC75109 Min	MC75109 Typ #	MC75109 Max	MC75110 Min	MC75110 Typ #	MC75110 Max	Unit
High-Level Input Current to 1A, 1B, 2A or 2B (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V)# (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)	I_{IH_L}	1	– –	– –	40 1.0	– –	– –	40 1.0	µA mA
Low-Level Input Current to 1A, 1B, 2A or 2B (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	1	–	–	-3.0	–	–	-3.0	mA
High-Level Input Current into 1C or 2C (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	2	– –	– –	40 1.0	– –	– –	40 1.0	µA mA
Low-Level Input Current into 1C or 2C (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	2	–	–	-3.0	–	–	-3.0	mA
High-Level Input Current into D (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	2	– –	– –	80 2.0	– –	– –	80 2.0	µA mA
Low-Level Input Current into D (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	2	–	–	-6.0	–	–	-6.0	mA
Output Current ("on" state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(on)}$	3	– 3.5	6.0 –	7.0 –	– 6.5	12 –	15 –	mA
Output Current ("off" state) (V_{CC} = Min, V_{EE} = Min)	$I_{O(off)}$	3	–	–	100	–		100	µA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	4	–	25	30	–	28	35	mA
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	4	–	-23	-30	–	-41	-50	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{CC(off)}$	4	–	18	–	–	21	–	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	4	–	-10	–	–	-17	–	mA

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V.

##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

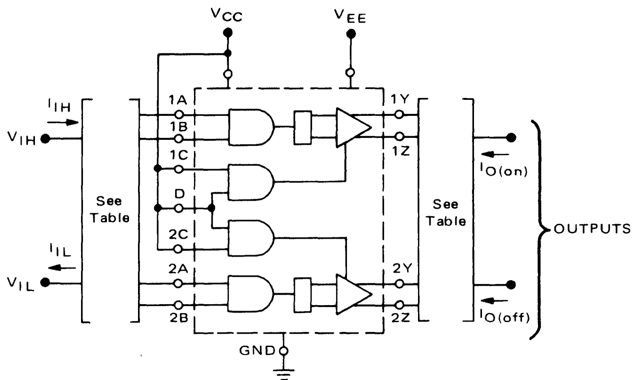
8

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input A or B to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L} t_{PHL_L}	5	– –	9.0 9.0	15 15	ns
Propagation Delay Time from Inhibitor Input C or D to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I} t_{PHL_I}	5	– –	16 13	25 25	ns

TEST CIRCUITS

FIGURE 1 – V_{IH}, V_{IL}, I_{IH}, and I_{IL}

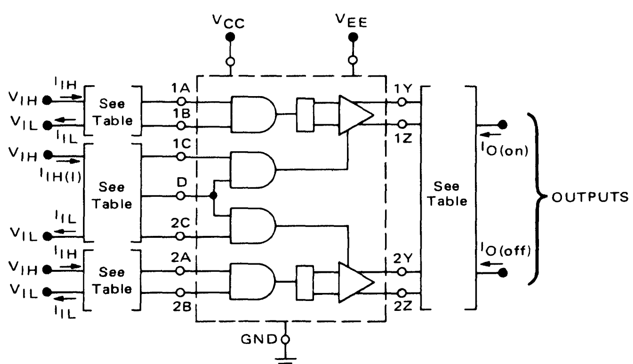


TEST TABLE

TEST AT ANY LOGIC INPUT	LOGIC INPUTS NOT UNDER TEST	ALL INHIBITOR INPUTS	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
V_{IH_L}	Open	V_{IH_I}	H (See Note 1)	L (See Note 1)
V_{IL_L}	V_{CC}	V_{IH_I}	L (See Note 1)	H (See Note 1)
I_{IH_L}	4.5 V	V_{IH_I}	Gnd	Gnd
I_{IL_L}	Gnd	V_{IH_I}	Gnd	Gnd

NOTES: 1. Low output represents the "on" state, high output represents the "off" state.
2. Each input is tested separately.
3. Arrows indicate actual direction of current flow.

FIGURE 2 – V_{IH}, V_{IL}, I_{IH}, I_{IL}



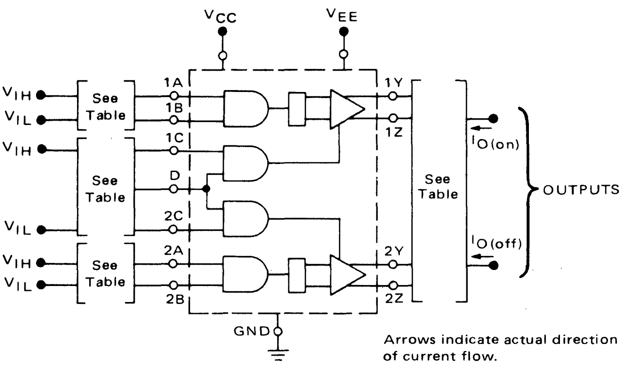
TEST TABLE

TEST AT ANY INHIBITOR INPUT	ALL LOGIC INPUTS	INHIBITOR INPUTS NOT UNDER TEST	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
V_{IH_I}	V_{IH_L}	Open	H(See Note 1)	L(See Note 1)
	V_{IL_L}	Open	L(See Note 1)	H(See Note 1)
V_{IL_I}	V_{IH_L}	V_{CC}	H(See Note 1)	H(See Note 1)
	V_{IL_L}	V_{CC}	H(See Note 1)	H(See Note 1)
I_{IH_I}	Gnd	4.5 V	Gnd	Gnd
I_{IL_I}	Gnd	Gnd	Gnd	Gnd

8

TEST CIRCUITS (continued)

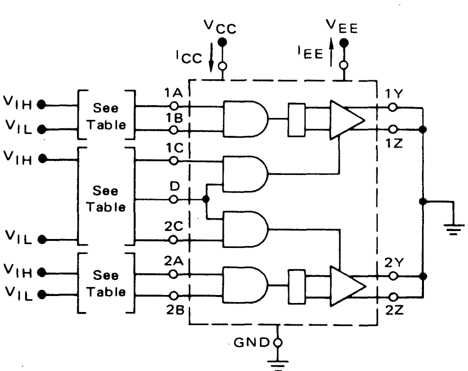
FIGURE 3– $I_{O(on)}$ and $I_{O(off)}$



TEST TABLE

TEST Ground all output pins not under test.		LOGIC INPUTS 1A or 2A	LOGIC INPUTS 1B or 2B	INHIBITOR INPUTS 1C or 2C	INHIBITOR INPUTS D
$I_{O(on)}$	at output 1Y or 2Y	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(on)}$	at output 1Z or 2Z	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Y or 2Y	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Z or 2Z	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(off)}$	at output 1Y, 2Y, 1Z, or 2Z	Either state	Either state	V_{IL}	V_{IL}
				V_{IL}	V_{IH}
				V_{IH}	V_{IL}

FIGURE 4 – I_{CC} and I_{EE}



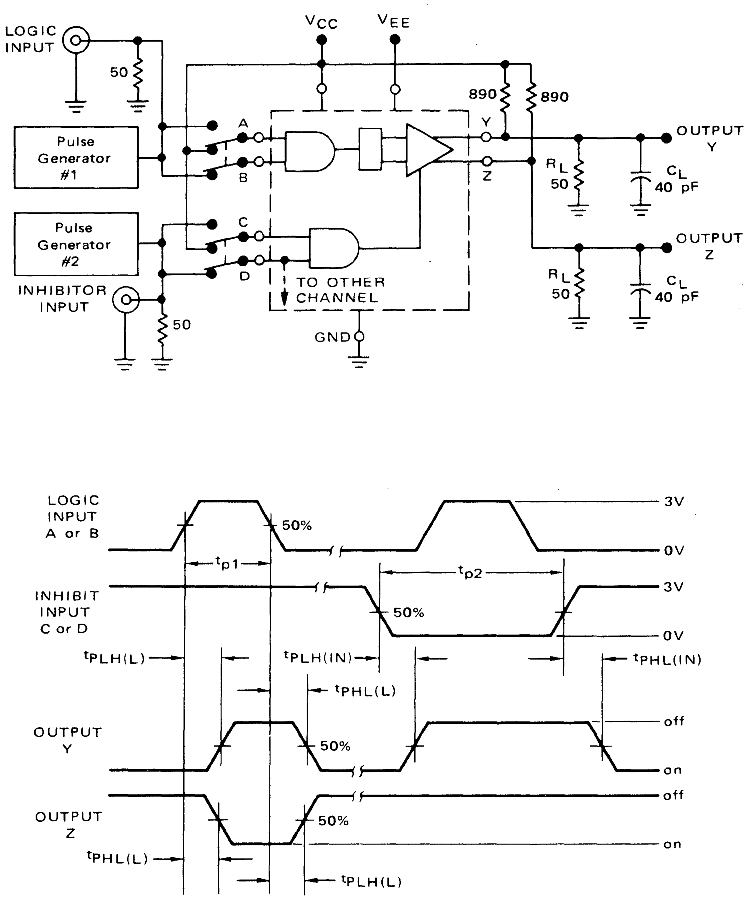
TEST TABLE

TEST		ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
$I_{CC(on)}$	Driver enabled	V_{IL}	V_{IH}
$I_{EE(on)}$	Driver enabled	V_{IL}	V_{IH}
$I_{CC(off)}$	Driver inhibited	V_{IL}	V_{IL}
$I_{EE(off)}$	Driver inhibited	V_{IL}	V_{IL}

8

TEST CIRCUITS (continued)

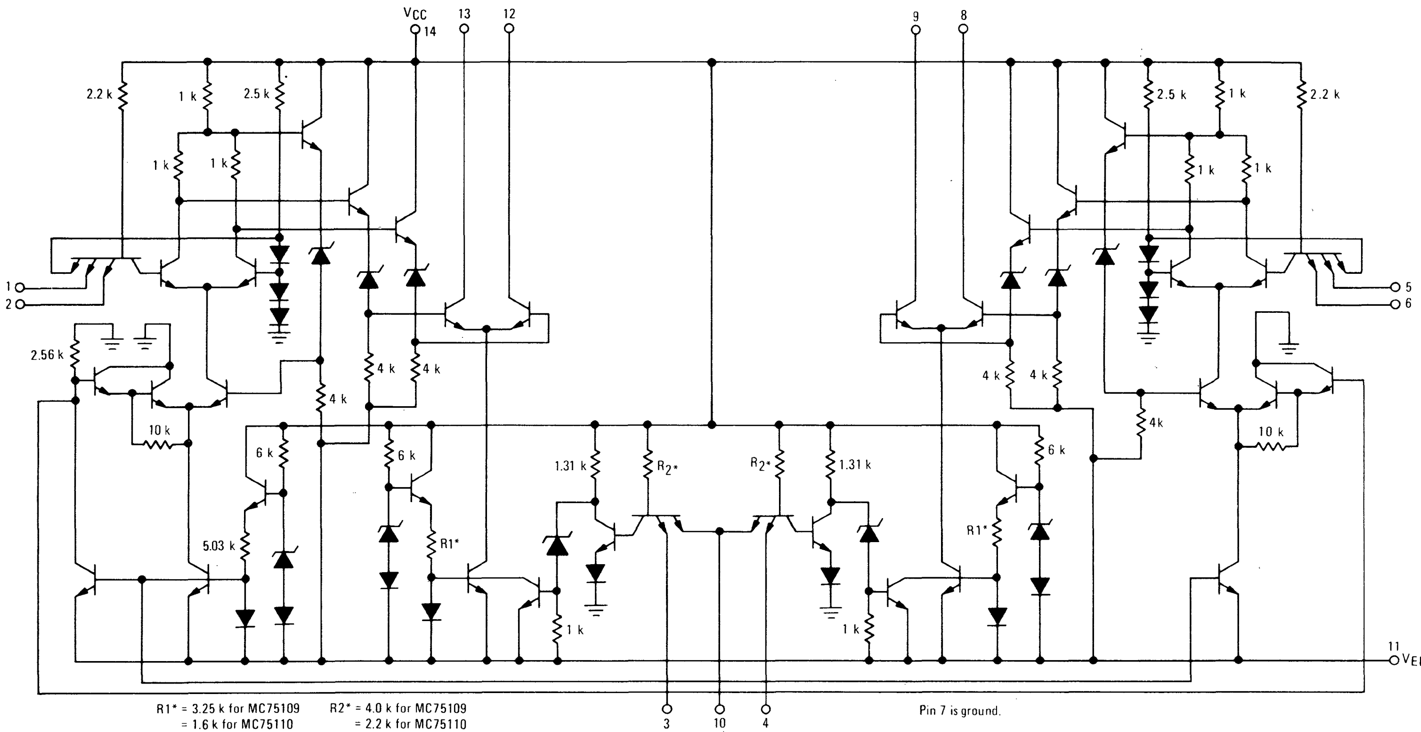
FIGURE 5 – PROPAGATION DELAY TIMES TEST CIRCUIT AND WAVEFORMS



NOTES: 1. The pulse generators have the following characteristics: $z_o = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz, $t_{p2} = 1$ ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

8

CIRCUIT DIAGRAM



R1* = 3.25 k for MC75109
= 1.6 k for MC75110

R2* = 4.0 k for MC75109
= 2.2 k for MC75110

Pin 7 is ground.

MC75113L

DIFFERENTIAL PARTY-LINE DRIVER

Specifications and Applications Information

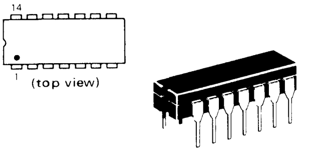
DIFFERENTIAL PARTY-LINE DRIVER

. . . designed for use in high-speed data transmission systems which use balanced terminated transmission lines. The MC75113's push-pull output eliminates ground loop and cross-talk problems. When all the inputs are at logic "0", no current flows through either output, making it ideal for party-line operation.

- Push-Pull Drive Capability, ±20 mA
- MTTL and MDTL Compatible Inputs
- Wide Common-Mode Output Voltage Range: ±3.0 Volts typical

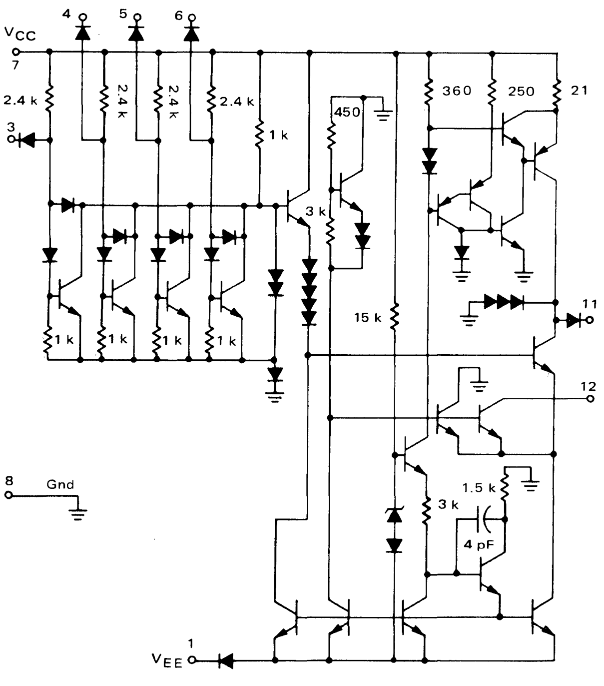
DIFFERENTIAL PARTY-LINE DRIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT

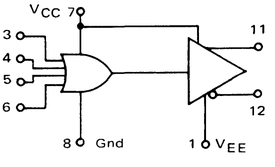


CERAMIC PACKAGE
CASE 632

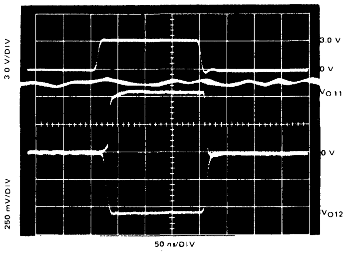
CIRCUIT DIAGRAM



BLOCK DIAGRAM



TYPICAL OPERATION



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Positive Power Supply Voltage (Pin 7)	V_{CC}	+8.0	Volts
Negative Power Supply Voltage (Pin 1)	V_{EE}	-8.0	Volts
Positive Input Voltage (Pins 3,4,5,6)	V_{in}	+8.0	Volts
Negative Input Voltage (Pins 3,4,5,6)	V_{in}	-4.0	Volts
Output Voltage (Pins 11,12)	V_O	+8.0/-3.0	Volts
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Temperature Range	T_A	0 to +75	°C
Power Dissipation (Package Limitation)	P_D	1000	mW
Derate Above T_A = +25°C	$1/\theta JA$	6.7	mW/°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Positive Power Supply Current	1	I_{CC}	–	+46	+61	mA
Negative Power Supply Current	1	I_{EE}	–	-32	-44	mA
Positive Output Current (short circuit)	2	I_{O11}	+18	+20	+26	mA
Negative Output Current (short circuit)	2	I_{O12}	-18	-20	-26	mA
Differential Output Current	3	ΔI_{OD}	–	±2.0	–	mA
Positive Output "On" Common-Mode Range	4	V_{O1}	+2.7	–	–	V
Negative Output "On" Common-Mode Range	4	V_{O2}	-2.7	–	–	V
Positive Output "Off" Common-Mode Range	5	V_{O3}	+3.0	–	–	V
Negative Output "OFF" Common-Mode Range	5	V_{O4}	-2.5	–	–	V
Positive Output "Off" Common-Mode Range	6	V_{O5}	-2.4	–	–	V
Negative Output "Off" Common-Mode Range	6	V_{O6}	+3.0	–	–	V
Power "Off" Positive Output Common-Mode Range	7	V_{O7}	-2.0	–	–	V
Power "Off" Negative Output Common-Mode Range	7	V_{O8}	-2.0	–	–	V
Forward Input Current	8	I_{IF}	–	–	-2.6	mA
Reverse Input Current	8	I_{IR}	–	–	+50	μA

SWITCHING CHARACTERISTICS (T_A = +25°C unless otherwise noted, see Figure 9)

Characteristic	Symbol	Min	Typ	Max	Unit
"ON" Propagation Delay (Positive Output)	$t_{PLH\ 11}$	–	25	30	ns
Rise Time (Positive Output)	$t_{TLH\ 11}$	–	10	15	ns
"OFF" Propagation Delay (Positive Output)	$t_{PHL\ 11}$	–	15	20	ns
Fall Time (Positive Output)	$t_{THL\ 11}$	–	10	15	ns
"ON" Propagation Delay (Negative Output)	$t_{PHL\ 12}$	–	25	30	ns
Fall Time (Negative Output)	$t_{THL\ 12}$	–	10	15	ns
"OFF" Propagation Delay (Negative Output)	$t_{PLH\ 12}$	–	15	20	ns
Rise Time (Negative Output)	$t_{TLH\ 12}$	–	10	15	ns

TEST CIRCUITS

TABLE I – INPUT LOGIC VOLTAGE FOR TEST CIRCUITS

Temperature (°C)	V_{IL} (Volts)	V_{IH} (Volts)
0°	1.16	1.85
+25°	1.08	1.78
+75°	0.94	1.64

FIGURE 1 – POWER SUPPLY CURRENTS

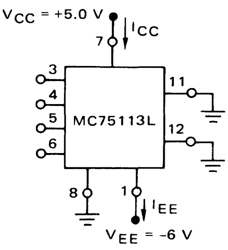


FIGURE 2 – POSITIVE and NEGATIVE OUTPUT CURRENTS (Short Circuit)

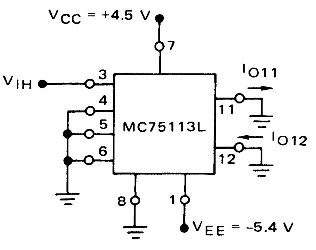


FIGURE 3 – DIFFERENTIAL OUTPUT CURRENT

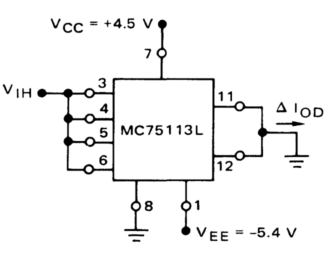


FIGURE 4 – OUTPUT "ON" POSITIVE and NEGATIVE OUTPUT COMMON-MODE RANGE

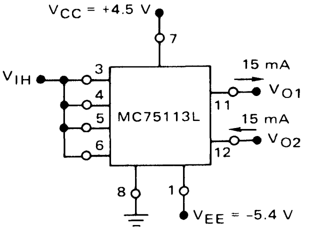


FIGURE 5 – OUTPUT "OFF" POSITIVE and NEGATIVE OUTPUT COMMON-MODE RANGE

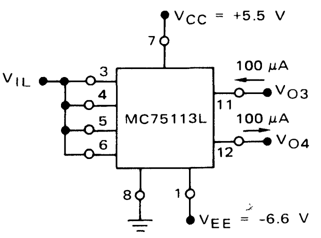


FIGURE 6 – OUTPUT "OFF" POSITIVE and NEGATIVE OUTPUT COMMON-MODE RANGE

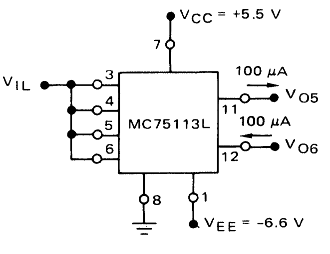
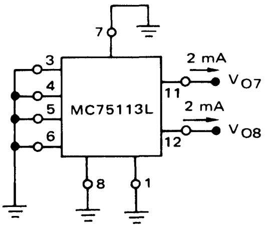


FIGURE 7 – POWER "OFF" POSITIVE and NEGATIVE OUTPUT COMMON-MODE RANGE



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TEST CIRCUITS (continued)

FIGURE 8 – INPUT CURRENT TESTS

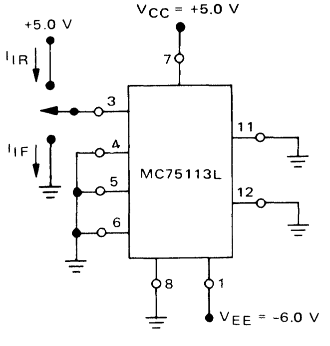
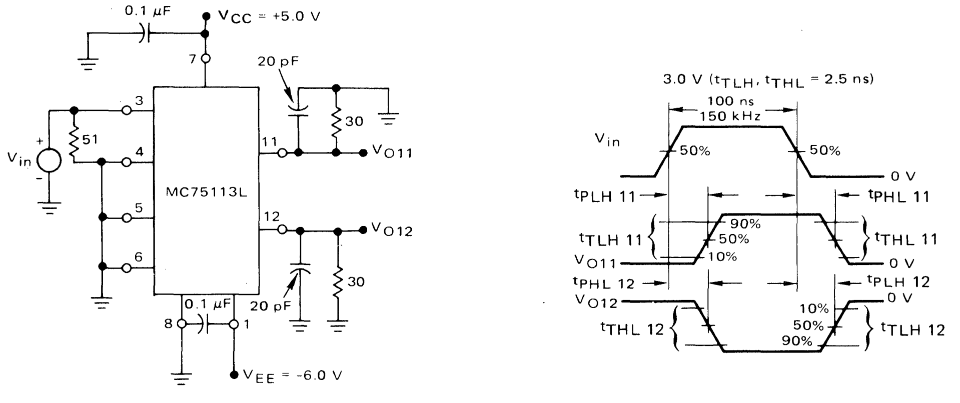


FIGURE 9 – AC TEST CIRCUIT and WAVEFORMS



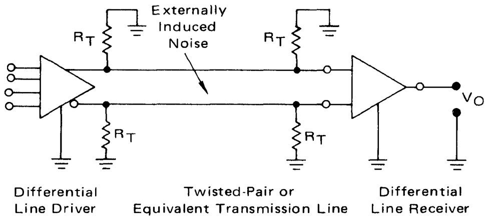
APPLICATIONS INFORMATION

INTRODUCTION

The MC75113L is a differential line driver with current-mode outputs which are designed for driving balanced terminated transmission lines such as twisted-pair cable in computer systems applications.

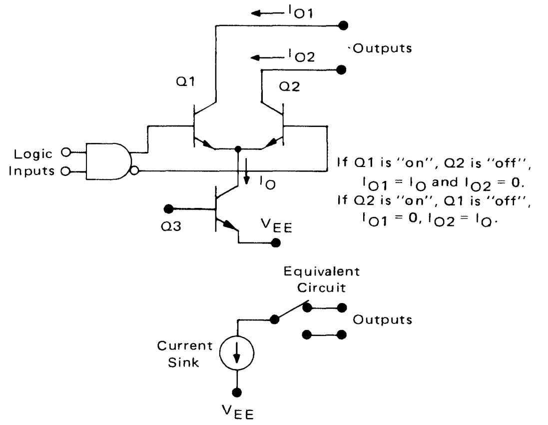
An example of a differential data transmission system is shown in Figure 10. Because the lines are balanced in a differential system, externally induced noise will appear equally on both inputs to the line receiver. Since the line receiver responds only to differential signals, this noise is rejected. This immunity to noise makes the differential method of data transmission far superior to single-ended transmission.

FIGURE 10 – DIFFERENTIAL TRANSMISSION SYSTEM



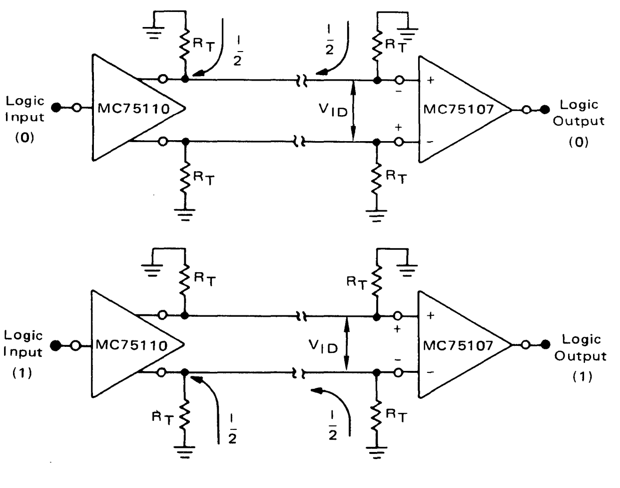
Another advantage of differential line driver systems over single-ended line driver systems is that a noise spike coupled into adjacent lines from the positive-going signal line is cancelled by an equal and opposite noise spike coupled from the negative-going signal line. In single-ended systems, a shield would be required for each transmission line to prevent coupling to adjacent lines in the cable.

FIGURE 11 – SIMPLIFIED OUTPUT CIRCUIT OF "PULL-ONLY" DRIVERS (MC75109/MC75110)



One approach to differential data transmission uses the open-collector output circuitry shown in Figure 11. This output circuit could be called a "Pull-Only" output since current flows in only one direction regardless of which collector is conducting. The MC75109/MC75110 is an example of a driver which utilizes this scheme. Figure 12 illustrates that when driving with the MC75109/MC75110, the current flow through the terminating resistors generates a differential voltage on the lines which changes polarity in response to the logic condition applied to the driver's inputs. The MC75109/MC75110 also has a provision to

FIGURE 12 – "PULL-ONLY" SYSTEM SHOWING BOTH LOGIC CONDITIONS



APPLICATIONS INFORMATION (continued)

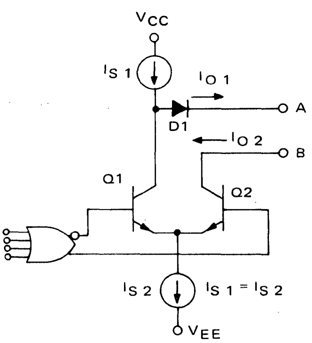
shut down the current source transistor Q3 (Figure 11) so that isolation from other drivers is possible. This feature permits differential operation in party-line systems.

OPERATION OF THE MC75113L

The MC75113L, unlike the MC75109/MC75110 uses a unique "Push-Pull" output circuit shown in Figure 13. The figure shows that when Q1 is "on" and Q2 is "off", the current from both outputs is zero; but when Q1 is "off" and Q2 is "on", the currents from both outputs are nearly equal and opposite. When the output currents are turned "off", D1 and transistor Q2 prevent current flow to or from either output terminal over a wide range of output voltages. Thus with this type of design, numerous drivers can be connected in parallel to the same pair of lines (party-line mode) and those drivers in the "off" state will not load a driver in the "on" state. The output current in both logic states is shown in Figure 14.

One advantage of this type of system is apparent in Figure 15. Due to the symmetry of the line currents in "Push-Pull" systems ground-loop currents are minimized. These ground-loop currents produce voltages that subtract from the useful common-mode operating range of the drivers and receivers. The MC75113L has a typical mismatch of 2.0 mA between the current source and sink while the MC75110 has a typical "Pull Only" current of 10 mA. Therefore, the typical ground-loop current is only 1.0 mA in the "Push-Pull" system compared to 5.0 mA in the "Pull-Only" system.

FIGURE 13 – SIMPLIFIED OUTPUT STAGE OF MC75113L "PUSH-PULL" DRIVER



If Q1 is "on", Q2 is "off", Diode D1 is "off" and current $I_{S\,1}$ flows through Q1 and $I_{S\,2}$ to V_{EE}. However, if Q1 is "off", and Q2 is "on", the current $I_{S\,1}$ flows through diode D1 to output A and current from output B flows through Q2 to current sink $I_{S\,2}$.

EQUIVALENT CIRCUIT

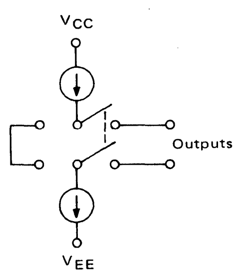


FIGURE 14 – "PUSH-PULL" SYSTEM SHOWING BOTH LOGIC CONDITIONS

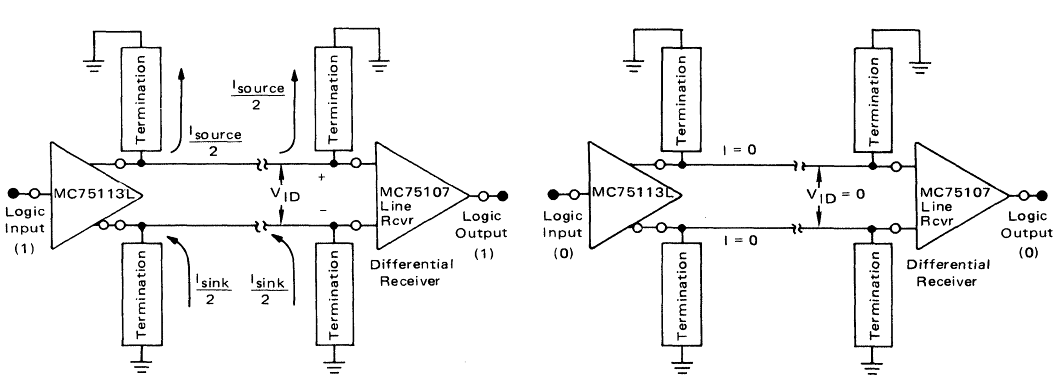
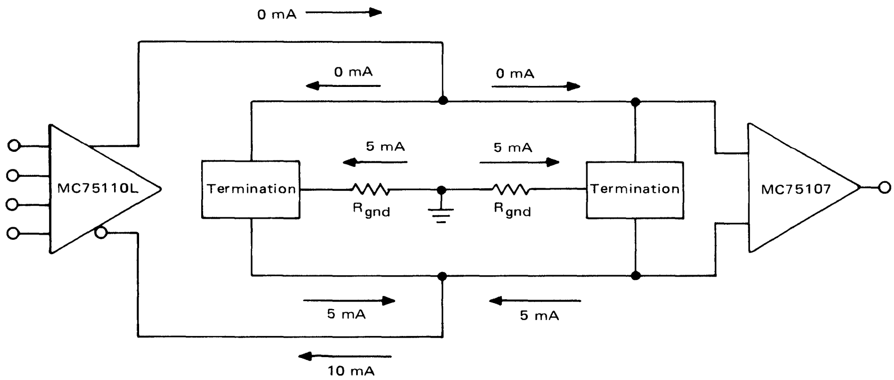
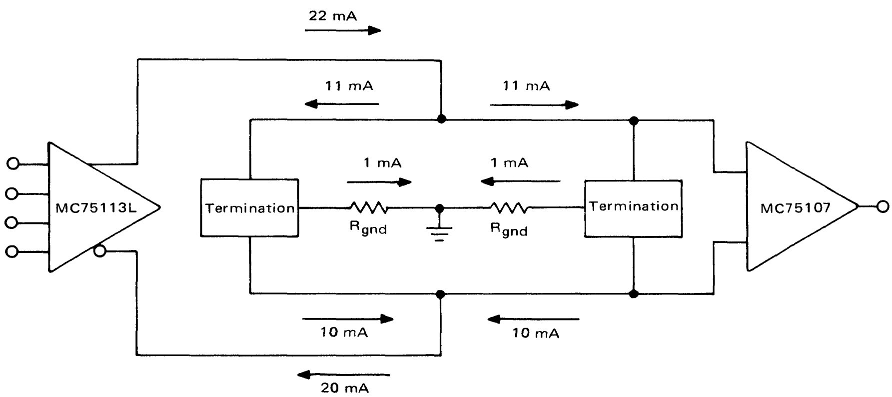


FIGURE 15 – COMPARISON OF GROUND CURRENTS IN "PUSH-PULL" AND "PULL-ONLY" DATA TRANSMISSION SYSTEMS

"Pull-Only" Differential Line Driver Typical Mismatch of Output Currents Indicated (10 mA)



"Push-Pull" Differential Line Driver Typical Mismatch of Output Currents Indicated (2 mA)



DIFFERENTIAL PARTY-LINE OPERATION

Often in large computer systems it is desirable to attach several drivers and receivers at different points along a transmission line. Figure 16 shows an example of such a Party-Line or Data Bus System. Only one driver may be active at a time but all receivers may be active simultaneously. Such sharing or multiplexing of transmission lines results in considerable savings and flexibility in systems interconnections. Isolation of inactive drivers from the active driver is essential in party-line operation. The MC75113L guarantees this isolation even when power supplies of some of the drivers in the system are "off". This important feature makes it unnecessary to simultaneously power-up all system components when the use of only a few is required. As noted previously, all types of differential driver systems have the advantage of differential noise cancellation not available with single-ended driver systems. However, in multiple driver or party-line systems the MC75113L, with "Push-Pull" outputs, has the additional advantage of eliminating the uncancelled common-mode noise spike which occurs during the "enable" and "inhibit" cycles (required for party-line operation in "Pull-Only" differential line drivers).

LINE TERMINATION

In any high-speed data transmission system proper termination to prevent reflections is necessary. Transmission line pairs in close proximity to ground such as

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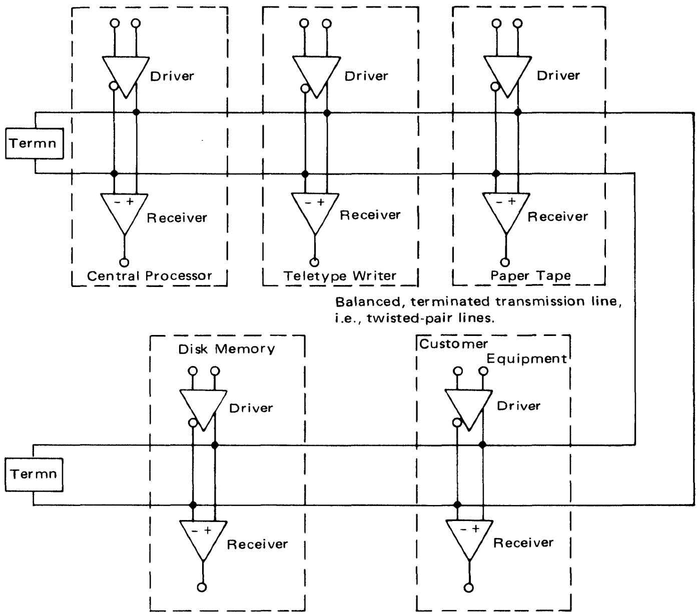
APPLICATIONS INFORMATION (continued)

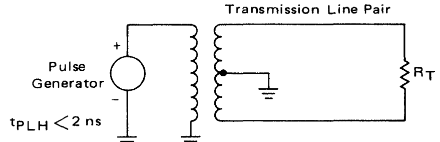
FIGURE 16 – A DIFFERENTIAL PARTY-LINE SYSTEM



microstrip, stripline, ribbon cable, and shielded twisted-pair, exhibit two distinct characteristics impedances. The common-mode characteristic impedance (z_{cm}) is due to the two lines being at the same potential and carrying equal currents in the same direction. The differential-mode characteristic impedance (z_{dm}) is due to the lines being at equal but opposite potentials and carrying equal currents in opposite directions. Since both common-mode noise and differential-mode data signals will be present on the transmission lines, the lines must be terminated so that both types of signals will be absorbed rather than reflected at the termination points. The differential-mode characteristic impedance of a particular line may be measured from the circuit in Figure 17A. The pulse transformer is used to assure equal and opposite voltage and current excursions on the pair of lines. The value of z_{dm} for each line is equal to the value of the resistor needed to prevent differential-mode reflections from appearing on the lines.

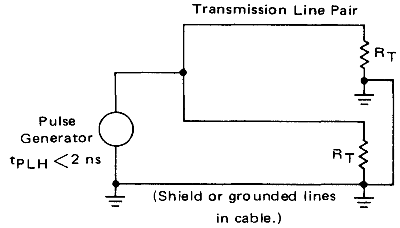
The circuit of Figure 17B may be used to measure the value of common-mode characteristic impedance, z_{cm}. The

FIGURE 17A – CIRCUIT FOR z_{dm} MEASUREMENT



When $R_T = z_{dm}$, no Differential-Mode reflections occur.

FIGURE 17B – CIRCUIT FOR z_{cm} MEASUREMENT



When $R_T = z_{cm}$, no Common-Mode reflections occur.

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APPLICATIONS INFORMATION (continued)

value of resistors which prevent common-mode reflections is z_{cm}. When measuring z_{cm} and z_{dm} for lines which are part of a cable containing many lines, it is important to terminate the remaining lines in approximately the same way as they will eventually be terminated. This is because the number of grounded conductors and terminated conductors in the cable will affect the value of z_{cm} and z_{dm} measured.

Since $2\ z_{cm} > z_{dm}$, it is always possible to choose a delta bridge of resistors which will correctly terminate both the common-mode and differential-mode signals. The common-mode signal is correctly terminated by a resistor of value z_{cm} to ground from each line. The differential-mode signal is correctly terminated by a resistor whose value may be calculated from Equation 1.

$$R2 = \frac{2(z_{dm}\ (z_{cm})}{2\ z_{cm} - z_{dm}} \tag{1}$$

Additional information regarding common-mode and differential-mode characteristic impedance may be found in References 1 and 2. (In the References $z_{cm} = z_{oe}$, the "even" mode characteristic impedance, the $z_{dm} = 2z_{oo}$, the "odd" mode characteristic impedance.)

USE WITH POPULAR DIFFERENTIAL RECEIVERS

The differential-output signal of the MC75113L is zero when the output is "off". However, popular differential line receivers such as the MC75107, which have thresholds of approximately ±25 mV, require a positive differential signal to turn "on" and a negative differential signal to turn "off." Therefore, when using the MC75113L (which has no negative output signal) with this type of line receiver the line must be offset in voltage to provide the required negative differential signal. This is easily accomplished using the termination scheme shown in Figure 18.

The value of R6 is equal to z_{cm}. The value of R2 may be calculated from Equation 1. The value of R1 and R3 may be calculated from Equation 2 and 3 using the desired value of offset voltage, V_{IO}, and supply voltages, V_{CC} and V_{EE}.

$$R1 = \frac{z_{dm}}{2} \times \frac{V_{CC}}{V_{IO}} \tag{2}$$

$$R3 = \frac{-z_{dm}}{2} \times \frac{V_{EE}}{V_{IO}} \tag{3}$$

The resistor values R4 and R5 are chosen so that the parallel combinations of R1 and R4 and also R3 with R5 each equal z_{cm}:

$$R4 = \frac{z_{cm}\ (R1)}{R1 - z_{cm}} \tag{4}$$

$$R5 = \frac{z_{cm}\ (R3)}{R3 - z_{cm}} \tag{5}$$

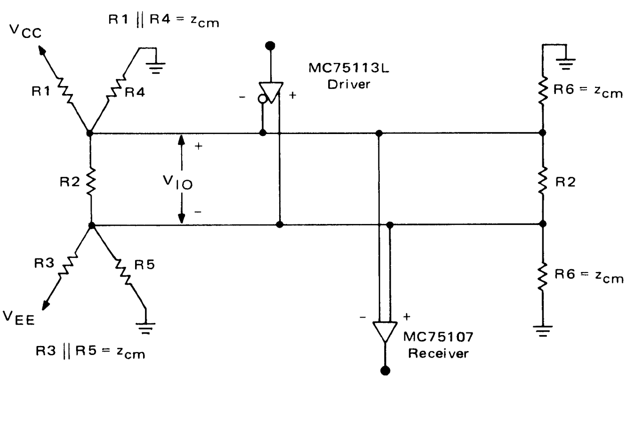
The choice of offset voltage, V_{IO}, depends upon the differential mode characteristic impedance. Since the minimum total differential signal produced by the MC75113L onto a properly terminated transmission path is:

$$V\ \text{driver min} = \frac{18\ \text{mA}}{2} \times (z_{dm})\ \text{(volts)} \tag{6}$$

The amount of offset voltage for equal noise margin on both sides of the receiver's zero volt threshold should be:

$$V_{IO} = \frac{V\ \text{driver min}}{2} = 4.5\ \text{mA} \times z_{dm}\ \text{(volts)} \tag{7}$$

FIGURE 18 — TERMINATION SCHEME FOR USE WITH POPULAR DIFFERENTIAL RECEIVERS



APPLICATIONS INFORMATION (continued)

EXAMPLE OF CALCULATION OF TERMINATION RESISTOR VALUES

Suppose the MC75113L is to be used with V_{CC} = +5.0 volts and V_{EE} = -6.0 volts to drive a transmission line with z_{cm} = 85 Ω and z_{dm} = 112 Ω. The offset voltage required for equal noise margin on both sides of the receiver's zero-volt threshold is found by Equation 7 to be:

$$V_{IO} = 4.5\ \text{mA} \times (112) = 0.504\ \text{volts} \qquad (8)$$

From Figure 17 it may be seen that R6 = z_{cm} = 85Ω. R2 is found from Equation 1:

$$R2 = \frac{2\,(112)\,(85)}{2\,(85) - 112} = 328\ \Omega \qquad (9)$$

R1 and R3 are found from Equations 2 and 3 to be:

$$R1 = \frac{112}{2} \times \frac{5}{0.504} - 556\ \Omega \qquad (10)$$

$$R3 = \frac{-112}{2} \times \frac{-6.0\ V}{0.504} = 667\ \Omega \qquad (11)$$

R3 and R5 are found from Equation 4 and 5:

$$R4 = \frac{85\ (556)}{556-85} = 100\ \Omega \qquad (12)$$

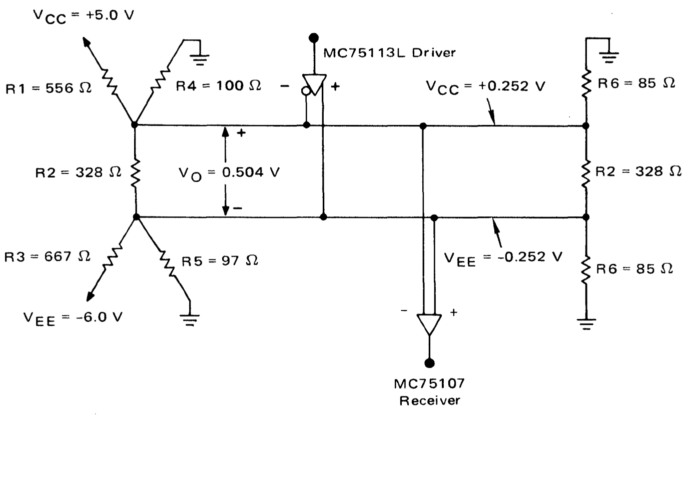
$$R5 = \frac{85\ (667)}{667-85} = 97\ \Omega \qquad (13)$$

The resulting structure is shown in Figure 19.

REFERENCES

1. Ivor Catt, "Crosstalk (Noise) in Digital Systems", IEEE Transactions on Electronic Computers, Vol. EC-16, No. 6, pp. 743-763, December 1967.
2. S. B. Cohn, "Shielded Coupled-Strip Transmission Lines," IRE Transactions Microwave Theory and Techniques, Vol. MTT-3, pp. 29-38, October 1955.
3. Motorola Application Note AN-708, "Line Driver and Receiver Considerations."

FIGURE 19 — EXAMPLE CALCULATION OF TERMINATION AND RECEIVER BIASING RESISTORS



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MC75140P1

DUAL LINE RECEIVER

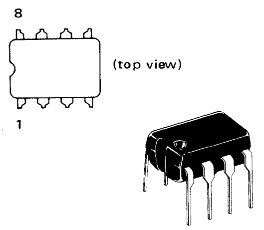
MONOLITHIC DUAL LINE RECEIVER

The MC75140P1 is a dual line receiver with common Strobe and Reference inputs. The Reference voltage is externally applied. This voltage may range from 1.5 to 3.5 volts, thus allowing for adjustment of maximum noise immunity in a given system design. The MC75140P1 is intended for use as a single-ended receiver in MTTL systems. Use in a party-line (bus-organized) system is aided by the low input current of the receiver.

- Single +5.0-Volts Power Supply
- ±100-mV Sensitivity
- Low Input Current
- MTTL Compatible Outputs
- Adjustable Reference Voltage
- Common Output Strobe

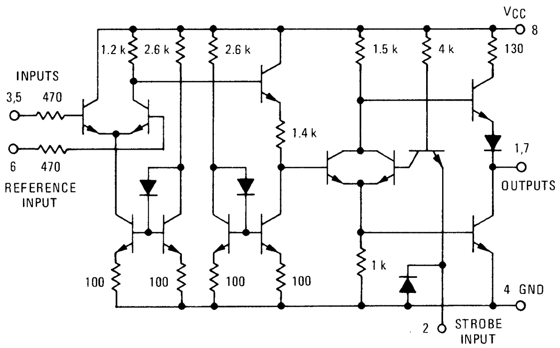
DUAL LINE RECEIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT

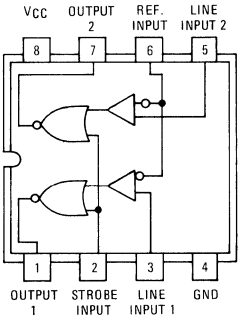


PLASTIC PACKAGE
CASE 626

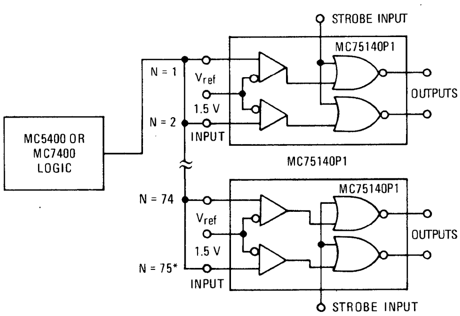
CIRCUIT SCHEMATIC
(1/2 Circuit Shown)



PIN CONNECTIONS



TYPICAL APPLICATION
HIGH FAN-OUT FROM A STANDARD MTTL GATE



*Most MC5400/MC7400 devices are capable of maintaining a 2.4-volt level under loads up to 7.5 mA.

FUNCTION TABLE

LINE INPUT	STROBE	OUTPUT
V_{ref} − 100 mV	L	H
V_{ref} + 100 mV	X	L
X	H	L

Positive Logic
H = High Level, L = Low Level,
X = Nonsignificant

See Packaging Information Section for outline dimensions.

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MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Volts
Reference Voltage	V_{ref}	5.5	Volts
Line Input Voltage (with respect to Ground)	$V_{I(L)}$	-2.0 to +5.5	Volts
Line Input Voltage (with respect to V_{ref})	$V_{I(L)}-V_{ref}$	±5.0	Volts
Strobe Input Voltage	$V_{I(S)}$	5.5	Volts
Power Dissipation (Package Limitation) Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 830 6.6	 mW mW/°C
Operating Temperature Range (Ambient)	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Nom	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts
Reference Voltage Range	$V_{ref\ R}$	1.5	–	3.5	Volts
Input Voltage Range (Line or Strobe)	V_{IR}	0	–	5.5	Volts
Operating Ambient Temperature Range	T_A	0	–	+70	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%, V_{ref} = 1.5 to 3.5 V, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ*	Max	Unit
High-Level Line Input Voltage	$V_{IH(L)}$	V_{ref} + 100	–	–	mV
Low-Level Line Input Voltage	$V_{IL(L)}$	–	–	V_{ref} - 100	mV
High-Level Strobe Input Voltage	$V_{IH(S)}$	2.0	–	–	Volts
Low-Level Strobe Input Voltage	$V_{IL(S)}$	–	–	0.8	Volt
High-Level Output Voltage $V_{IL(L)} = V_{ref}$ - 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OH} = -400 µA	V_{OH}	 2.4	 –	 –	Volts
Low-Level Output Voltage $V_{IH(L)} = V_{ref}$ + 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OL} = 16 mA $V_{IL(L)} = V_{ref}$ - 100 mV, $V_{IH(S)}$ = 2.0 V, I_{OL} = 16 mA	V_{OL}	 – –	 – –	 0.4 0.4	Volt
Strobe Input Clamp Voltage $I_{I(S)}$ = -12 mA	$V_{I(S)}$	 –	 –	 -1.5	Volts
Strobe Input Current (at max Input Voltage) $V_{I(S)}$ = 5.5 V	$I_{I(S)}$	 –	 –	 2.0	mA
High-Level Input Currents Strobe ($V_{I(S)}$ = 2.4 V) Line ($V_{I(L)} = V_{CC}$, V_{ref} = 1.5 V) Reference (V_{ref} = 3.5 V, $V_{I(L)}$ = 1.5 V)	 $I_{IH(S)}$ $I_{IH(L)}$ $I_{IH(ref)}$	 – – –	 – 35 70	 80 100 200	µA
Low-Level Input Currents Strobe ($V_{I(S)}$ = 0.4 V) Line ($V_{I(L)}$ = 0 V, V_{ref} = 1.5 V) Reference (V_{ref} = 0 V, $V_{I(L)}$ = 1.5 V)	 $I_{IL(S)}$ $I_{IL(L)}$ $I_{IL(ref)}$	 – – –	 – – –	 -3.2 -10 -20	 mA µA µA
Short-Circuit Output Current** V_{CC} = 5.5 V	I_{OS}	 -18	 –	 -55	mA
Supply Current (output high) $V_{I(S)}$ = 0 V, $V_{I(L)} = V_{ref}$ - 100 mV	I_{CCH}	 –	 18	 30	mA
Supply Current (output low) $V_{I(S)}$ = 0 V, $V_{I(L)} = V_{ref}$ + 100 mV	I_{CCL}	 –	 20	 35	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, V_{ref} = 2.5 V, C_L = 15 pF, R_L = 400 Ω, T_A = +25°C unless otherwise noted.) See Figure 1.

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time (low-to-high level output from Line input)	$t_{PLH(L)}$	–	22	35	ns
Propagation Delay Time (high-to-low level output from Line input)	$t_{PHL(L)}$	–	22	30	ns
Propagation Delay Time (low-to-high level output from Strobe input)	$t_{PLH(S)}$	–	12	22	ns
Propagation Delay Time (high-to-low level output from Strobe input)	$t_{PHL(S)}$	–	8.0	15	ns

*All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
**Only one output should be shorted at a time.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

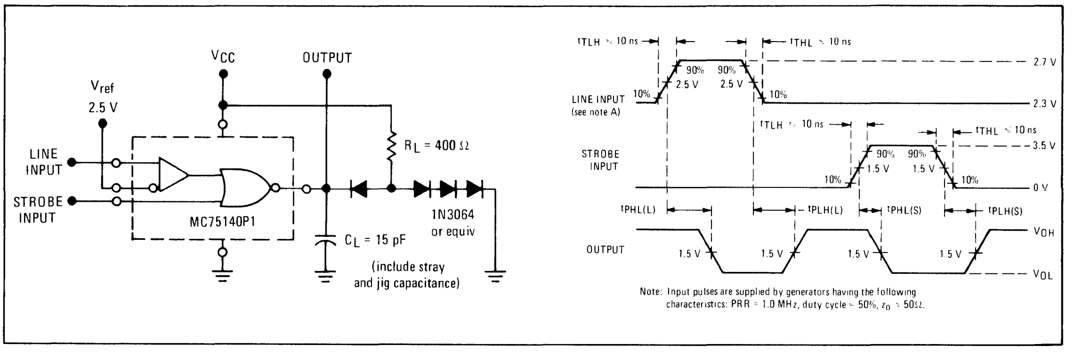


FIGURE 2 – OUTPUT VOLTAGE versus LINE INPUT VOLTAGE

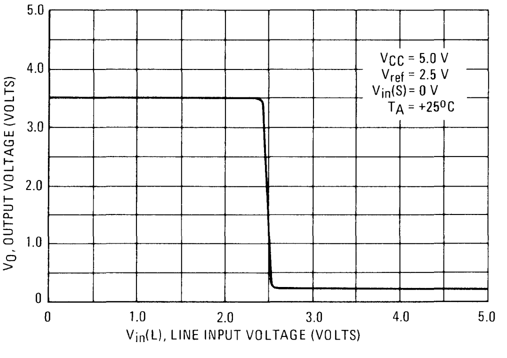


FIGURE 3 – SCHMITT TRIGGER

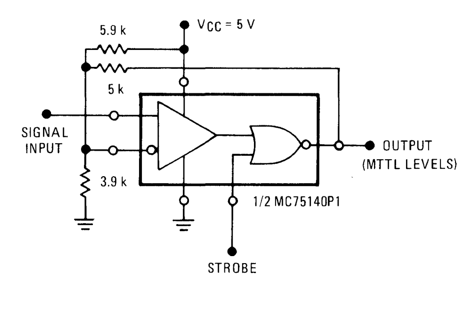


FIGURE 4 – TRANSFER CHARACTERISTICS FOR SCHMITT TRIGGER

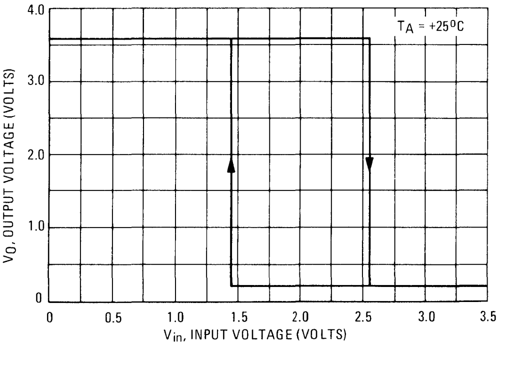


FIGURE 5 – GATED OSCILLATOR

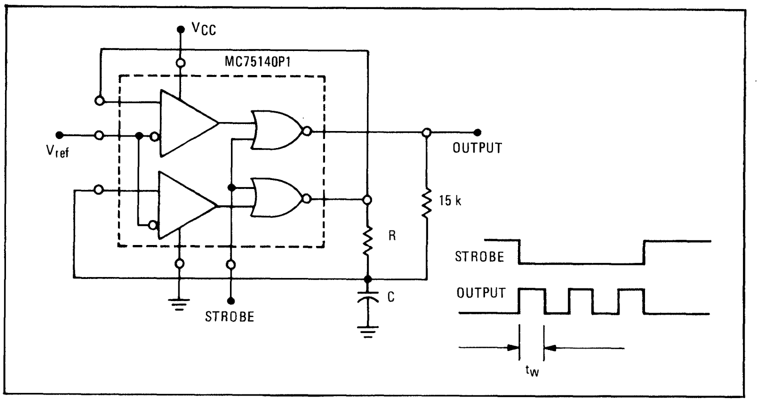


FIGURE 6 – GATE OSCILLATOR FREQUENCY versus RC TIME CONSTANT

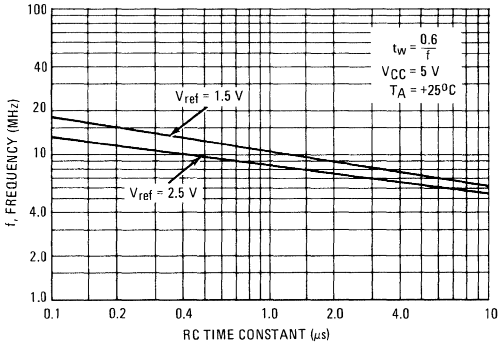
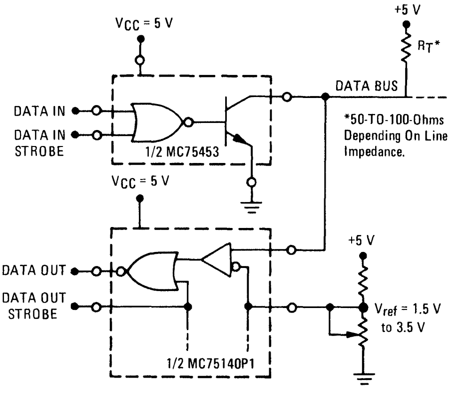


FIGURE 7 – DUAL BUS TRANSCEIVER



8

MC75450

PERIPHERAL DRIVER

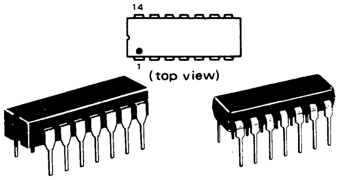
DUAL PERIPHERAL POSITIVE "AND" DRIVER

The MC75450 is a versatile device designed for use as a general-purpose dual interface circuit in MDTL and MTTL type systems. This device features two standard MTTL gates and two noncommitted, high-current, high-voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers.

- MDTL and MTTL Compatibility
- 300 mA Output Current Drive Capability (each transistor)
- Separate Gate and Output Transistor for Maximum Design Flexibility
- High Output Breakdown Voltage: V_{CER} = 30 Volts minimum

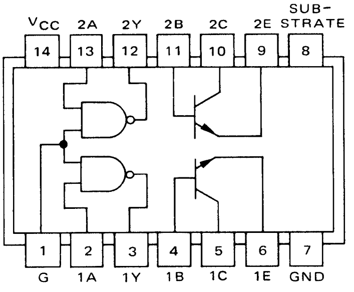
DUAL PERIPHERAL POSITIVE "AND" DRIVER

MONOLITHIC SILICON INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

P SUFFIX
PLASTIC PACKAGE
CASE 646



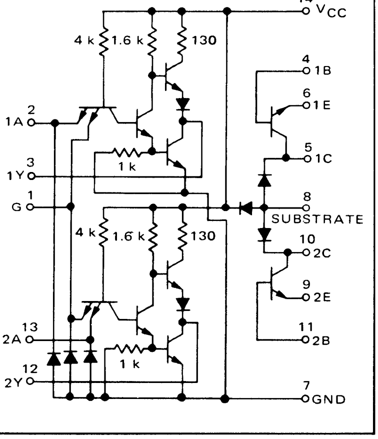
Positive Logic: Y = $\overline{AG}$ (gate only)
C = AG (gate and transistor)

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage (See Note 1)	V_{CC}	+7.0	Vdc
Input Voltage (See Note 1)	V_{in}	5.5	Vdc
V_{CC}-to-Substrate Voltage		35	Vdc
Collector-to-Substrate Voltage		35	Vdc
Collector-Base Voltage	V_{CB}	35	Vdc
Collector-Emitter Voltage (See Note 2)	V_{CE}	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current (continuous) (See Note 3)		300	mA
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 830 6.6	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 ohms.
3. Both halves of these dual circuits may conduct the rated current simultaneously.

CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

RECOMMENDED OPERATING CONDITIONS (See Note 4)

Characteristic	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc

Note 4. The substrate, pin 8, must always be at the most negative device voltage for proper operation.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

MTTL GATES

Characteristic		Symbol	Test Fig.	Min	Typ*	Max	Unit
High-Level Input Voltage		V_{IH}	1	2.0	–	–	Vdc
Low-Level Input Voltage		V_{IL}	2	–	–	0.8	Vdc
High-Level Output Voltage (V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_{OH} = –400 μA)		V_{OH}	2	2.4	3.3	–	Vdc
Low-Level Output Voltage (V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 16 mA)		V_{OL}	1	–	0.22	0.4	Vdc
High-Level Input Current (V_{CC} = 5.25 V, V_{in} = 2.4 V)	Input A	I_{IH}	3	–	–	40	μA
	Input G			–	–	80	
(V_{CC} = 5.25 V, V_{in} = 5.5 V)	Input A			–	–	1.0	mA
	Input G			–	–	2.0	
Low-Level Input Current (V_{CC} = 5.25 V, V_{in} = 0.4 V)	Input A	I_{IL}	4	–	–	-1.6	mA
	Input G			–	–	-3.2	
Short-Circuit Output Current** (V_{CC} = 5.25 V)		I_{OS}	5	-18	–	-55	mA
Supply Current			6				mA
High-Level Output (V_{CC} = 5.25 V, V_{in} = 0)		I_{CCH}		–	2.0	4.0	
Low-Level Output (V_{CC} = 5.25 V, V_{in} = 5.0 V)		I_{CCL}		–	6.0	11	
Input Clamp Voltage (V_{CC} = 4.75 V, I_{in} = –12 mA)		V_{in}	4	–	–	-1.5	V

OUTPUT TRANSISTORS

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)	V_{CBO}	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 μA, R_{BE} = 500 ohms)	V_{CER}	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μA, I_C = 0)	V_{EBO}	5.0	–	–	Vdc
Static Forward Transfer Ratio (See Note 5)	h_{FE}				
(V_{CE} = 3.0 V, I_C = 100 mA, T_A = +25°C)		25	–	–	
(V_{CE} = 3.0 V, I_C = 300 mA, T_A = +25°C)		30	–	–	
(V_{CE} = 3.0 V, I_C = 100 mA, T_A = 0°C)		20	–	–	
(V_{CE} = 3.0 V, I_C = 300 mA, T_A = 0°C)		25	–	–	
Base-Emitter Voltage (See Note 5)	V_{BE}				Vdc
(I_B = 10 mA, I_C = 100 mA)		–	0.85	1.0	
(I_C = 30 mA, I_C = 300 mA)		–	1.05	1.2	
Collector-Emitter Saturation Voltage (See Note 5)	$V_{CE(sat)}$				Vdc
(I_B = 10 mA, I_C = 100 mA)		–	0.25	0.4	
(I_B = 30 mA, I_C = 300 mA)		–	0.5	0.7	

Note 5. These parameters must be measured using pulse techniques; t_W = 300 μs, duty cycle ≤ 2%.
*All typical values at V_{CC} = 5.0 V, T_A = +25°C.
**Not more than one output should be shorted at a time.

8

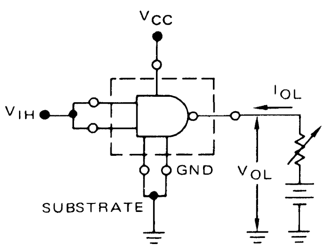
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
MTTL GATES						
Propagation Delay Time (C_L = 15 pF, R_L = 400 ohms)		7				ns
Low-to-High-Level Output	t_{PLH}		–	14	–	
High-to-Low-Level Output	t_{PHL}		–	6.0	–	
OUTPUT TRANSISTORS #						
Switching Times (I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1.0 V, C_L = 15 pF, R_L = 50 ohms)		8				ns
Delay Time	t_d		–	9.0	–	
Rise Time	t_r		–	11	–	
Storage Time	t_s		–	14	–	
Fall Time	t_f		–	8.0	–	
GATES AND TRANSISTORS COMBINED #						
Propagation Delay Time (I_C = 200 mA, C_L = 15 pF, R_L = 50 ohms)		9				ns
Low-to-High-Level Output	t_{PLH}		–	21	–	
High-to-Low Level Output	t_{PHL}		–	16	–	
Transition Time# (I_C = 200 mA, C_L = 15 pF, R_L = 50 ohms)		9				ns
Low-to-High-Level Output	t_{TLH}		–	7.0	–	
High-to-Low-Level Output	t_{THL}		–	8.0	–	

#Voltage and current values are nominal; exact values vary slightly with transistors parameters.

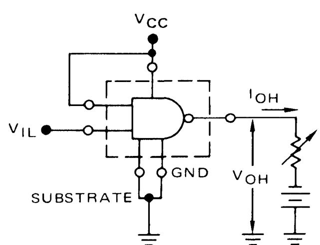
DC TEST CIRCUITS FOR MTTL GATES

FIGURE 1 – V_{IH}, V_{OL}



Both inputs are tested simultaneously.

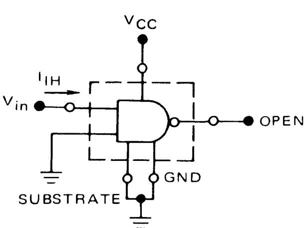
FIGURE 2 – V_{IL}, V_{OH}



Each input is tested separately.

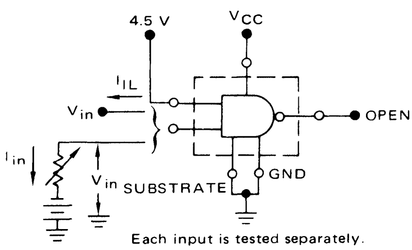
(Arrows indicate actual direction of current flow. Current into a terminal is a positive value.)

FIGURE 3 – I_{IH}



Each input is tested separately.

FIGURE 4 – I_{IL}, V_{in}

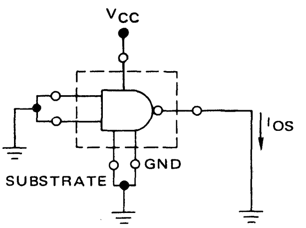


Each input is tested separately.

8

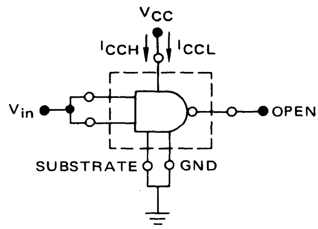
DC TEST CIRCUITS FOR MTTL GATES (continued)

FIGURE 5 – I_{OS}



Each gate is tested separately

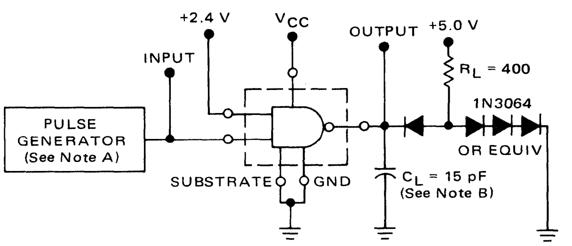
FIGURE 6 – I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

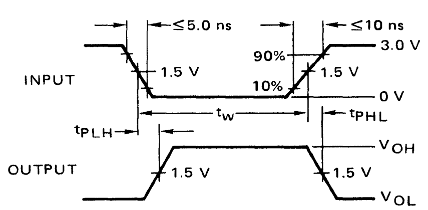
(Arrows indicate actual direction of current flow. Current into a terminal is a positive value.)

FIGURE 7 – PROPAGATION DELAY TIMES, EACH GATE



NOTES: A. The pulse generator has the following characteristics: $t_w = 0.5\ \mu s$, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

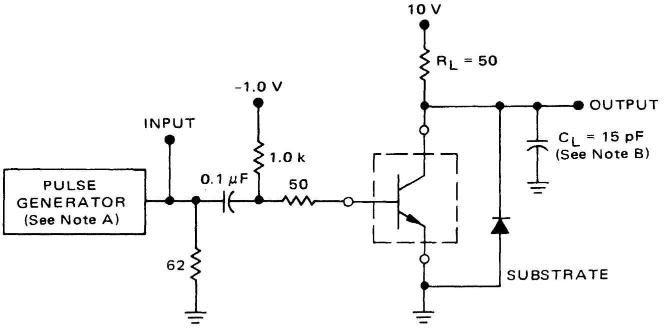
VOLTAGE WAVEFORMS



8

TEST CIRCUITS (continued)

FIGURE 8 – SWITCHING TIMES, EACH TRANSISTOR



NOTES: A. The pulse generator has the following characteristics: t_w = 0.3 μs, duty cycle ≤ 1%, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS

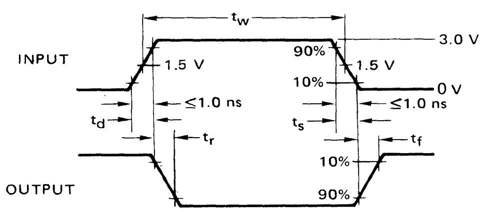
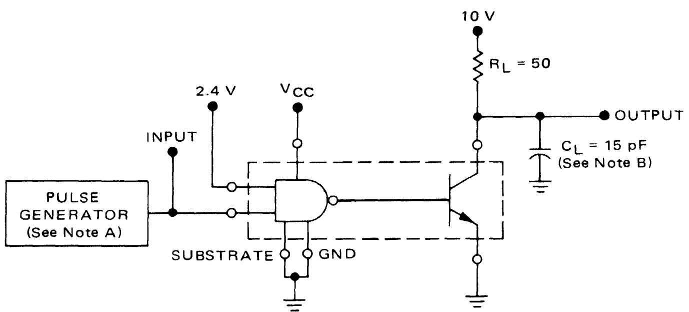
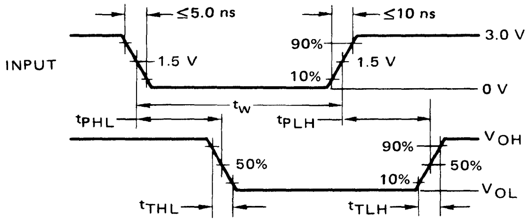


FIGURE 9 – SWITCHING TIMES, GATE AND TRANSISTOR



NOTES: A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS



8

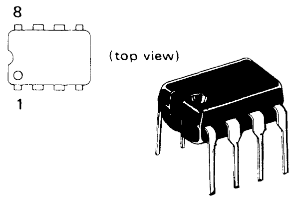
DUAL PERIPHERAL POSITIVE "AND" DRIVER

. . . designed for use as a general-purpose interface circuit in MDTL and MTTL type systems. The MC75451P is a dual peripheral positive AND driver consisting of logic gate outputs internally connected to the bases of two high-current, high-voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers.

- MDTL and MTTL Compatibility
- 300 mA Output Current Drive Capability (each transistor)
- High Output Breakdown Voltage; V_{CER} = 30 Volts minimum

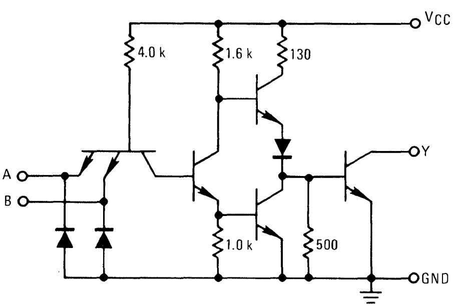
DUAL PERIPHERAL POSITIVE "AND" DRIVER

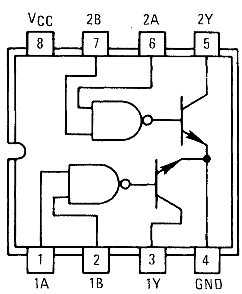
MONOLITHIC SILICON INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 626

CIRCUIT SCHEMATIC
(1/2 circuit shown)





Positive Logic: Y = AB

MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (See Note 1)	V_{CC}	+7.0	Vdc
Input Voltage (See Notes 1 and 2)	V_{in}	5.5	Vdc
Output Voltage (See Notes 1 and 3)	V_O	30	Vdc
Output Current (continuous)	I_O	300	mA
Power Dissipation (Package Limitation) Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 830 6.6	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1. Voltage values are with respect to network ground terminal.
NOTE 2. Input voltage should be zero or positive with respect to device ground terminal.
NOTE 3. This is the maximum voltage which should be applied to any output when it is in the "off" state.

TRUTH TABLE

A B	Y
L L	L ("on" state)
L H	L ("on" state)
H L	L ("on" state)
H H	H ("off" state)

H = high level, L = low level

See Packaging Information Section for outline dimensions.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted)

Characteristic	Symbol	Test Fig.	Min	Typ*	Max	Unit
High-Level Input Voltage	V_{IH}	1	2.0	–	–	Vdc
Low-Level Input Voltage	V_{IL}	2	–	–	0.8	Vdc
Input Clamp Voltage (V_{CC} = 4.75 V, I_{in} = -12 mA)	V_{in}	4	–	–	-1.5	Vdc
High-Level Output Current (V_{CC} = 4.75 V, V_{IH} = 2.0 V, V_{OH} = 30 V)	I_{OH}	1	–	–	100	µA
Low-Level Output Voltage (V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA) (V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA)	V_{OL}	2	– –	0.25 0.5	0.4 0.7	Vdc
High-Level Input Current (V_{CC} = 5.25 V, V_{in} = 2.4 V) (V_{CC} = 5.25 V, V_{in} = 5.5 V)	I_{IH}	3	– –	– –	40 1.0	µA mA
Low-Level Input Current (V_{CC} = 5.25 V, V_{in} = 0.4 V)	I_{IL}	4	–	-1.0	-1.6	mA
Supply Current (V_{CC} = 5.25 V, V_{in} = 5.0 V) High-Level Output (V_{CC} = 5.25 V, V_{in} = 0) Low-Level Output	 I_{CCH} I_{CCL}	5	 – –	 7.0 52	 11 65	mA

*Typical values are at V_{CC} = 5.0 V, T_A = +25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time (I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 ohms) Low-to-High-Level Output High-to-Low-Level Output	 t_{PLH} t_{PHL}	6	 – –	 17 18	 – –	ns
Transition Time (I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 ohms) Low-to-High-Level Output High-to-Low-Level Output	 t_{TLH} t_{THL}	6	 – –	 6.0 11	 – –	ns

8

TEST CIRCUITS

FIGURE 1 – V_{IH}, I_{OH}

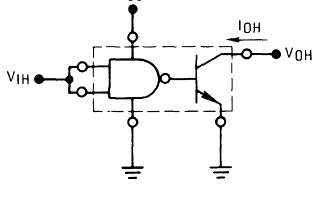
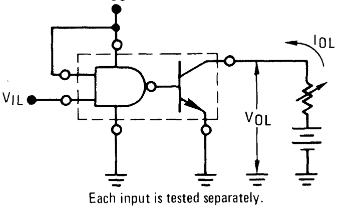


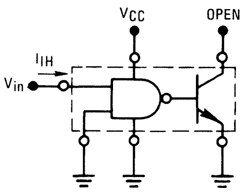
FIGURE 2 – V_{IL}, V_{OL}



Each input is tested separately.

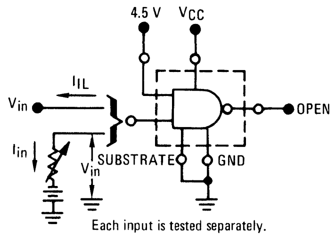
TEST CIRCUITS (continued)

FIGURE 3 – I_{IH}



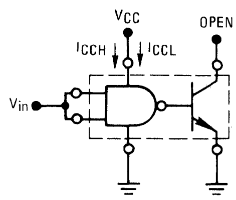
Each input is tested separately.

FIGURE 4 – I_{IL}, V_{in}



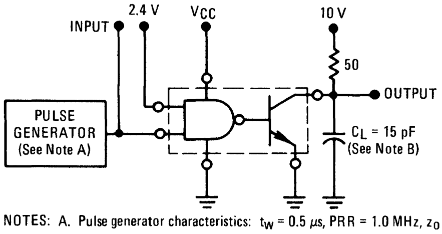
Each input is tested separately.

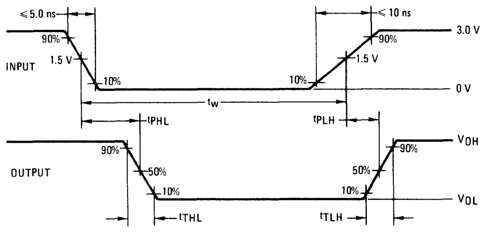
FIGURE 5 – I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

FIGURE 6 – SWITCHING TIMES AND WAVEFORMS





NOTES: A. Pulse generator characteristics: $t_W = 0.5\ \mu s$, PRR = 1.0 MHz, $z_0 \approx 50\ \Omega$.
B. C_L includes probe and test fixture capacitance.

MC75452P

PERIPHERAL DRIVER

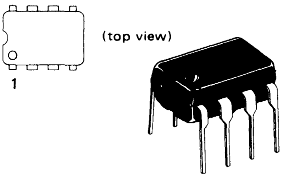
DUAL PERIPHERAL POSITIVE "NAND" DRIVER

. . . designed for use as a general-purpose interface circuit in MDTL and MTTL type systems. The MC75452P is a dual peripheral positive NAND driver consisting of logic gate outputs internally connected to the bases of two high-current, high-voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers.

- MDTL and MTTL Compatibility
- 300 mA Output Current Drive Capability (each transistor)
- High Output Breakdown Voltage; V_{CER} = 30 Volts minimum

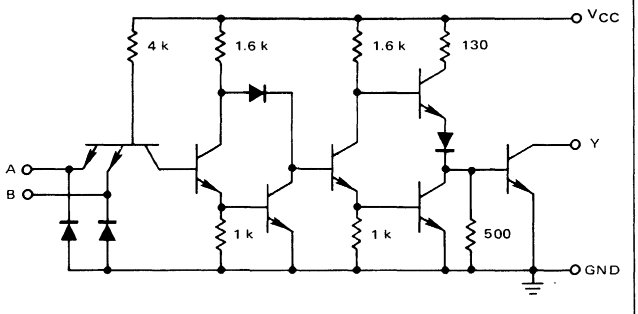
DUAL PERIPHERAL POSITIVE "NAND" DRIVER

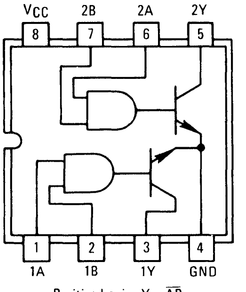
MONOLITHIC SILICON INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 626

CIRCUIT SCHEMATIC
(1/2 circuit shown)





Positive Logic: $Y = \overline{AB}$

MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (See Note 1)	V_{CC}	+7.0	Vdc
Input Voltage (See Notes 1 and 2)	V_{in}	5.5	Vdc
Output Voltage (See Notes 1 and 3)	V_O	30	Vdc
Output Current (continuous)	I_O	300	mA
Power Dissipation (Package Limitation) Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 830 6.6	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1. Voltage values are with respect to network ground terminal.
NOTE 2. Input voltage should be zero or positive with respect to device ground terminal.
NOTE 3. This is the maximum voltage which should be applied to any output when it is in the "off" state.

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	L ("on" state)

H = high level, L = low level

See Packaging Information Section for outline dimensions.

8

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted)

Characteristic	Symbol	Test Fig.	Min	Typ*	Max	Unit
High-Level Input Voltage	V_{IH}	1	2.0	–	–	Vdc
Low-Level Input Voltage	V_{IL}	2	–	–	0.8	Vdc
Input Clamp Voltage (V_{CC} = 4.75 V, I_{in} = -12 mA)	V_{in}	4	–	–	-1.5	Vdc
High-Level Output Current (V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 30 V)	I_{OH}	2	–	–	100	µA
Low-Level Output Voltage	V_{OL}	1				Vdc
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 100 mA)			–	0.25	0.4	
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 300 mA)			–	0.5	0.7	
High-Level Input Current	I_{IH}	3				
(V_{CC} = 5.25 V, V_{in} = 2.4 V)			–	–	40	µA
(V_{CC} = 5.25 V, V_{in} = 5.5 V)			–	–	1.0	mA
Low-Level Input Current (V_{CC} = 5.25 V, V_{in} = 0.4 V)	I_{IL}	4	–	-1.0	-1.6	mA
Supply Current		5				mA
(V_{CC} = 5.25 V, V_{in} = 0 V) High-Level Output	I_{CCH}		–	11	14	
(V_{CC} = 5.25 V, V_{in} = 5.0 V) Low-Level Output	I_{CCL}		–	56	71	

*Typical values are at V_{CC} = 5.0 V, T_A = +25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms)		6				ns
Low-to-High-Level Output	t_{PLH}		–	18	–	
High-to-Low-Level Output	t_{PHL}		–	16	–	
Transition Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms)		6				ns
Low-to-High-Level Output	t_{TLH}		–	8.0	–	
High-to-Low-Level Output	t_{THL}		–	9.0	–	

8

TEST CIRCUITS

FIGURE 1 – V_{IH}, V_{OL}

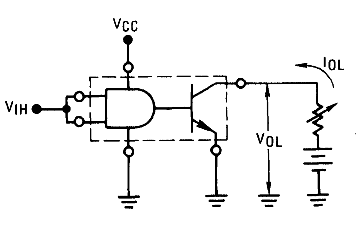
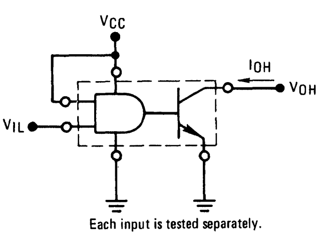


FIGURE 2 – V_{IL}, I_{OH}

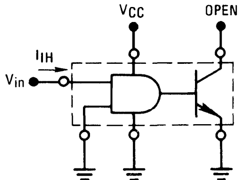


Each input is tested separately.

(Current into a terminal is shown as a positive value. Arrows indicate actual direction of current flow.)

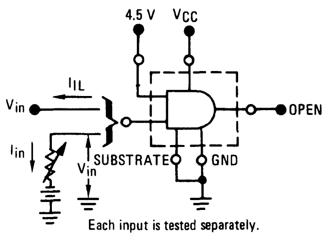
TEST CIRCUITS (continued)

FIGURE 3 – I_{IH}



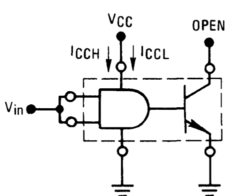
Each input is tested separately.

FIGURE 4 – I_{IL}, V_{in}



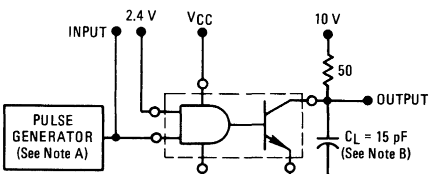
Each input is tested separately.

FIGURE 5 – I_{CCH}, I_{CCL}

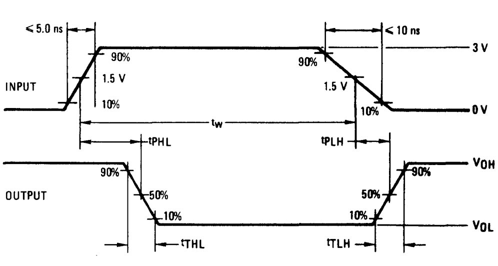


Both gates are tested simultaneously.

FIGURE 6 – SWITCHING TIMES AND WAVEFORMS



NOTES: A. Pulse generator characteristics: $t_w = 0.5\ \mu s$, PRR = 1.0 MHz, $z_0 \approx 50\ \Omega$.
B. C_L includes probe and test fixture capacitance.



8

PERIPHERAL DRIVER

MC75453P

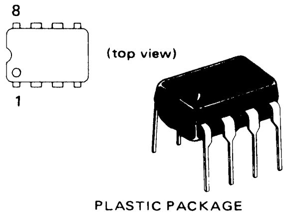
DUAL PERIPHERAL POSITIVE "OR" DRIVER

. . . designed for use as a general-purpose interface circuit in MDTL and MTTL type systems. The MC75453P is a dual peripheral positive OR driver consisting of logic gate outputs internally connected to the bases of two high-current, high-voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers.

- MDTL and MTTL Compatibility
- 300 mA Output Current Drive Capability (each transistor)
- High Output Breakdown Voltage; V_{CER} = 30 Volts minimum

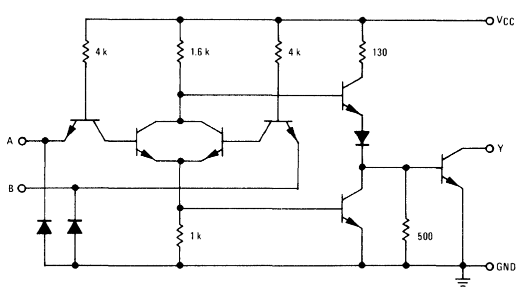
DUAL PERIPHERAL POSITIVE "OR" DRIVER

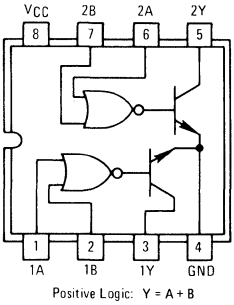
MONOLITHIC SILICON INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 626

CIRCUIT SCHEMATIC
(1/2 circuit shown)





Positive Logic: Y = A + B

MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (See Note 1)	V_{CC}	+7.0	Vdc
Input Voltage (See Notes 1 and 2)	V_{in}	5.5	Vdc
Output Voltage (See Notes 1 and 3)	V_O	30	Vdc
Output Current (continuous)	I_O	300	mA
Power Dissipation (Package Limitation) Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 830 6.6	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1. Voltage values are with respect to network ground terminal.
NOTE 2. Input voltage should be zero or positive with respect to device ground terminal.
NOTE 3. This is the maximum voltage which should be applied to any output when it is in the "off" state.

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	H ("off" state)

H = high level, L = low level

See Packaging Information Section for outline dimensions.

8

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted)

Characteristic	Symbol	Test Fig.	Min	Typ*	Max	Unit
High-Level Input Voltage	V_{IH}	1	2.0	–	–	Vdc
Low-Level Input Voltage	V_{IL}	2	–	–	0.8	Vdc
Input Clamp Voltage (V_{CC} = 4.75 V, I_{in} = -12 mA)	V_{in}	4	–	–	-1.5	Vdc
High-Level Output Current (V_{CC} = 4.75 V, V_{IH} = 2.0 V, V_{OH} = 30 V)	I_{OH}	1	–	–	100	μA
Low-Level Output Voltage	V_{OL}	2				Vdc
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA)			–	0.25	0.4	
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA)			–	0.5	0.7	
High-Level Input Current	I_{IH}	3				
(V_{CC} = 5.25 V, V_{in} = 2.4 V)			–	–	40	μA
(V_{CC} = 5.25 V, V_{in} = 5.5 V)			–	–	1.0	mA
Low-Level Input Current (V_{CC} = 5.25 V, V_{in} = 0.4 V)	I_{IL}	4	–	-1.0	-1.6	mA
Supply Current		5				mA
(V_{CC} = 5.25 V, V_{in} = 5.0 V) High-Level Output	I_{CCH}		–	8.0	11	
(V_{CC} = 5.25 V, V_{in} = 0) Low-Level Output	I_{CCL}		–	54	68	

*Typical values are at V_{CC} = 5.0 V, T_A = +25°C.

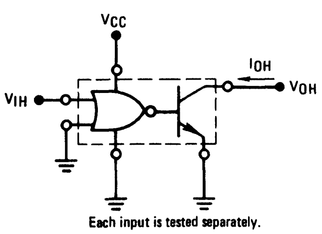
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms)		6				ns
Low-to-High-Level Output	t_{PLH}		–	15	–	
High-to-Low-Level Output	t_{PHL}		–	17	–	
Transition Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms)		6				ns
Low-to-High-Level Output	t_{TLH}		–	5.0	–	
High-to-Low-Level Output	t_{THL}		–	8.0	–	

TEST CIRCUITS

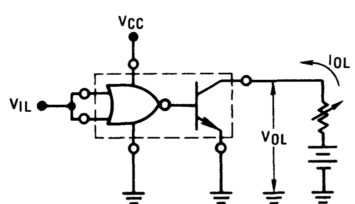
(Current into terminal is shown as a positive value. Arrows indicate direction of current flow.)

FIGURE 1 – V_{IH}, I_{OH}



Each input is tested separately.

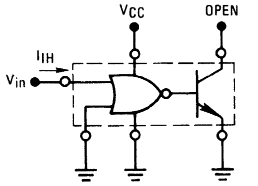
FIGURE 2 – V_{IL}, V_{OL}



8

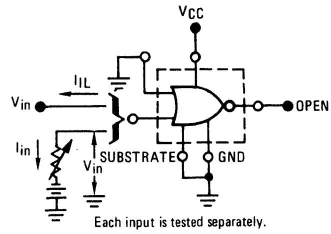
TEST CIRCUITS (continued)

FIGURE 3 – I_{IH}



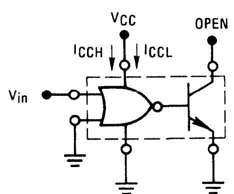
Each input is tested separately.

FIGURE 4 – I_{IL}, V_{in}



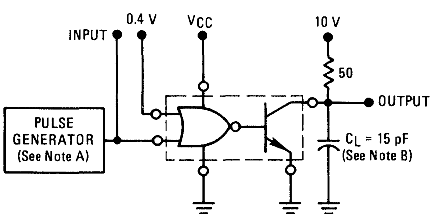
Each input is tested separately.

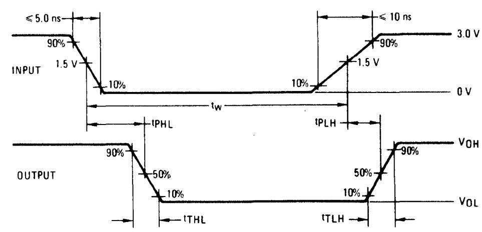
FIGURE 5 – I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

FIGURE 6 – SWITCHING TIMES AND WAVEFORMS





NOTES: A. Pulse generator characteristics: t_W = 0.5 μs, PRR = 1.0 MHz, $z_0 \approx 50\ \Omega$.
B. C_L includes probe and test fixture capacitance.

MC75454P

PERIPHERAL DRIVER

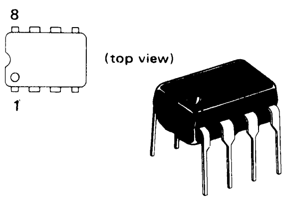
DUAL PERIPHERAL POSITIVE "NOR" DRIVER

. . . designed for use as a general-purpose interface circuit in MDTL and MTTL type systems. The MC75454P is a dual peripheral positive NOR driver consisting of logic gate outputs internally connected to the bases of two high-current, high-voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers.

- MDTL and MTTL Compatibility
- 300 mA Output Current Drive Capability (each transistor)
- High Output Breakdown Voltage; V_{CER} = 30 Volts minimum

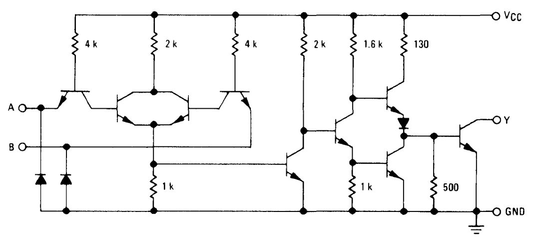
DUAL PERIPHERAL POSITIVE "NOR" DRIVER

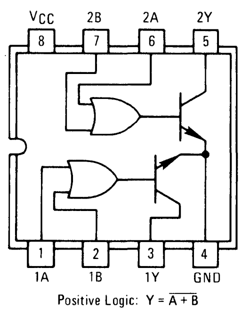
MONOLITHIC SILICON INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 626

CIRCUIT SCHEMATIC
(1/2 circuit shown)





Positive Logic: $Y = \overline{A+B}$

MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (See Note 1)	V_{CC}	+7.0	Vdc
Input Voltage (See Notes 1 and 2)	V_{in}	5.5	Vdc
Output Voltage (See Notes 1 and 3)	V_O	30	Vdc
Output Current (continuous)	I_O	300	mA
Power Dissipation (Package Limitation) Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 830 6.6	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1. Voltage values are with respect to network ground terminal.
NOTE 2. Input voltage should be zero or positive with respect to device ground terminal.
NOTE 3. This is the maximum voltage which should be applied to any output when it is in the "off" state.

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	L ("on" state)

H = high level, L = low level.

See Packaging Information Section for outline dimensions.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ*	Max	Unit
High-Level Input Voltage	V_{IH}	1	2.0	–	–	Vdc
Low-Level Input Voltage	V_{IL}	2	–	–	0.8	Vdc
Input Clamp Voltage (V_{CC} = 4.75 V, I_{in} = -12 mA)	V_{in}	4	–	–	-1.5	Vdc
High-Level Output Current (V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 30 V)	I_{OH}	2	–	–	100	µA
Low-Level Output Voltage (V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 100 mA) (V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 300 mA)	V_{OL}	1	 – –	 0.25 0.5	 0.4 0.7	Vdc
High-Level Input Current (V_{CC} = 5.25 V, V_{in} = 2.4 V) (V_{CC} = 5.25 V, V_{in} = 5.5 V)	I_{IH}	3	 – –	 – –	 40 1.0	 µA mA
Low-Level Input Current (V_{CC} = 5.25 V, V_{in} = 0.4 V)	I_{IL}	4	–	-1.0	-1.6	mA
Supply Current (V_{CC} = 5.25 V, V_{in} = 0 V) High-Level Output (V_{CC} = 5.25 V, V_{in} = 5.0 V) Low-Level Output	 I_{CCH} I_{CCL}	5	 – –	 13 61	 17 79	mA

*Typical values are at V_{CC} = 5.0 V, T_A = +25°C.

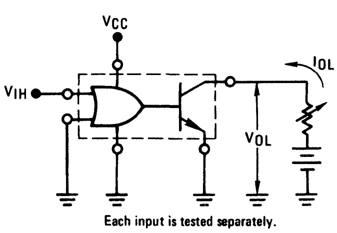
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms) Low-to-High-Level Output High-to-Low-Level Output	 t_{PLH} t_{PHL}	6	 – –	 25 19	 – –	ns
Transition Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms) Low-to-High-Level Output High-to-Low-Level Output	 t_{TLH} t_{THL}	6	 – –	 5.0 8.0	 – –	ns

TEST CIRCUITS

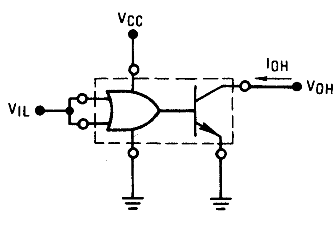
(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 1 – V_{IH}, V_{OL}



Each input is tested separately.

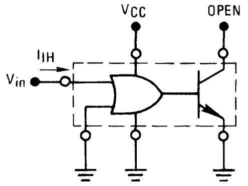
FIGURE 2 – V_{IL}, I_{OH}



8

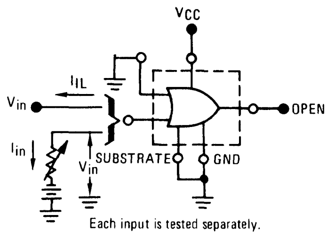
TEST CIRCUITS (continued)

FIGURE 3 – I_{IH}



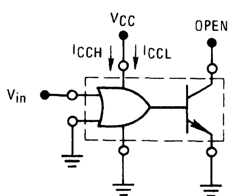
Each input is tested separately.

FIGURE 4 – I_{IL}, V_{in}



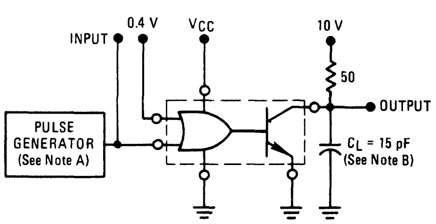
Each input is tested separately.

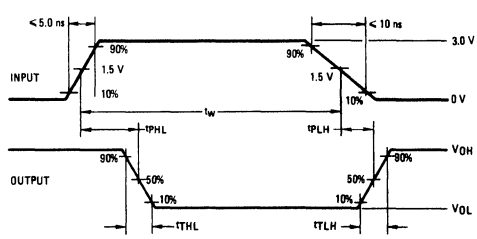
FIGURE 5 – I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

FIGURE 6 – SWITCHING TIMES AND WAVEFORMS





NOTES: A. Pulse generator characteristics: $t_w = 0.5\ \mu s$, PRR = 1.0 MHz, $z_0 \approx 50\ \Omega$.
B. C_L includes probe and test fixture capacitance.

8

MC75491
MC75492

MOS-LED DISPLAY DRIVERS

Specifications and Applications Information

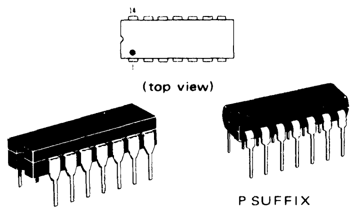
QUAD LED SEGMENT DRIVER – MC75491
HEX LED DIGIT DRIVER – MC75492

The MC75491 and MC75492 are designed to interface MOS logic to common cathode light-emitting diode readouts in serially addressed multi-digit displays. Using a segment address and digit scan LED drive method in a time multiplexing system results in a minimizing of the number of required drivers.

- Low Input Current Requirement for MOS Compatibility
- Low Standby Power Drain
- Source or Sink Current Capability of 50 mA for MC75491
- Sink Current Capability of 250 mA for MC75492
- Four High-Gain Darlington Drivers in a Single Package – MC75491
- Six High-Gain Darlington Drivers in a Single Package – MC75492

MULTIPLE LIGHT-EMITTING DIODE (LED) DRIVERS

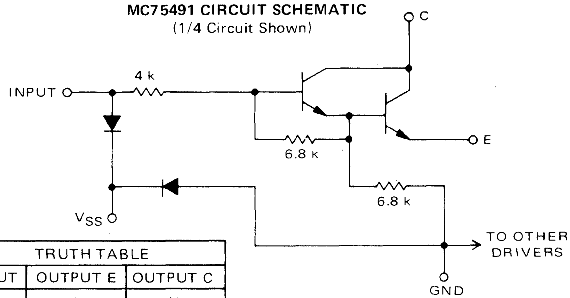
MONOLITHIC SILICON INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

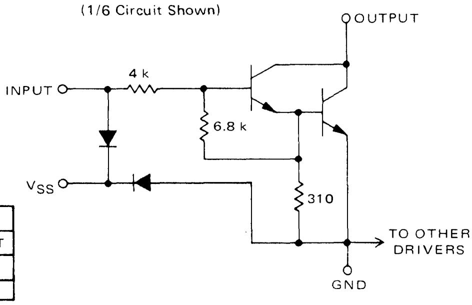
P SUFFIX
PLASTIC PACKAGE
CASE 646

MC75491 CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



TRUTH TABLE		
INPUT	OUTPUT E	OUTPUT C
L	L	H
H	H	L

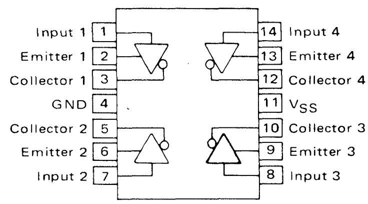
MC75492 CIRCUIT SCHEMATIC
(1/6 Circuit Shown)



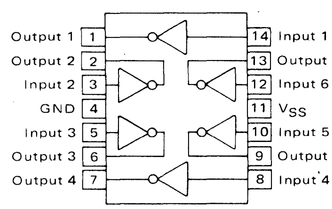
TRUTH TABLE	
INPUT	OUTPUT
L	H
H	L

CONNECTION DIAGRAMS

MC75491



MC75492



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value MC75491	Value MC75492	Unit
Bias Supply Voltage (See Note 1)	V_{SS}	10	10	Vdc
Input Voltage (See Note 2)	V_{in}	-5.0 to V_{SS}	-5.0 to V_{SS}	Vdc
Collector Voltage (See Note 3)	V_C	10	10	Vdc
Collector-to-Emitter Voltage	V_{CE}	10	–	Vdc
Collector-to-Input Voltage	V_{CI}	10	10	Vdc
Emitter Voltage ($V_{in} \geqslant 5.0$ Vdc)	V_E	10	–	Vdc
Emitter-to-Input Voltage	V_{EI}	5.0	–	Vdc
Continuous Collector Current (Each Collector) (All Collectors)	I_C	50 200	250 600	mA mA
Power Dissipation (Package Limitation) Ceramic and Plastic Dual In-Line Packages Derate above T_A = +25°C	P_D	830 6.6		mW mW/°C
Operating Temperature Range	T_A	0 to +70		°C
Storage Temperature Range	T_{stg}	-65 to +150		°C

Note 1. V_{SS} terminal voltage is with respect to any other device terminal.

Note 2. With the exception of the inputs, the GND terminal must always be the most negative device voltage for proper operation.

Note 3. Voltage values are with respect to GND terminal unless otherwise noted.

ELECTRICAL CHARACTERISTICS (V_{SS} = 10 Vdc, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	MC75491 Min	MC75491 Typ	MC75491 Max	MC75492 Min	MC75492 Typ	MC75492 Max	Unit
Low-Level Collector-to-Emitter Voltage (V_{in} = 8.5 V thru 1.0 kΩ, I_{OL} = 50 mA, V_E = 5.0 V)	V_{CEL}							Vdc
T_A = +25°C		–	0.9	1.2	–	–	–	
T_A = 0 to +70°C		–	–	1.5	–	–	–	
High-Level Collector Current	I_{CH}							µA
V_{CH} = 10 V, V_E = 0, I_{in} = 40 µA		–	–	100	–	–	–	
V_{CH} = 10 V, V_E = 0, V_{in} = 0.7 V		–	–	100	–	–	–	
Low-Level Output Voltage (V_{in} = 6.5 V thru 1.0 kΩ, I_{OL} = 250 mA)	V_{OL}							Vdc
T_A = +25°C		–	–	–	–	0.9	1.2	
T_A = 0 to +70°C		–	–	–	–	–	1.5	
High-Level Output Current	I_{OH}							µA
V_{OH} = 10 V, I_{in} = 40 µA		–	–	–	–	–	200	
V_{OH} = 10 V, V_{in} = 0.5 V		–	–	–	–	–	200	
Input Current at Maximum Input Voltage V_{in} = 10 V, I_{OL} = 20 mA	I_{in}	–	2.2	3.3	–	2.2	3.3	mA
Emitter Current – Reverse Bias I_C = 0, V_{in} = 0, V_E = 5.0 V	I_{ER}	–	–	100	–	–	–	µA
Bias Supply Current (V_{SS} = 10 V)	I_{SS}	–	–	1.0	–	–	1.0	mA

SWITCHING CHARACTERISTICS (V_{SS} = 7.5 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC75491 Min	MC75491 Typ	MC75491 Max	MC75492 Min	MC75492 Typ	MC75492 Max	Unit
Propagation Delay Time, High-to-Low Level	t_{PHL}							ns
R_L = 200 Ω, V_{IH} = 4.5 V, C_L = 15 pF, V_E = 0		–	20*	–	–	–	–	
R_L = 39 Ω, V_{IH} = 7.5 V, C_L = 15 pF		–	–	–	–	40	–	
Propagation Delay Time, Low-to-High Level	t_{PLH}							ns
C_L = 15 pF, V_E = 0, R_L = 200 Ω, V_{IH} = 4.5 Vdc		–	40*	–	–	–	–	
C_L = 15 pF, R_L = 39 Ω, V_{IH} = 7.5 Vdc		–	–	–	–	80	–	

*To collector output.

8

TYPICAL CHARACTERISTICS

(V_{SS} = +10 Vdc, T_A = +25°C unless otherwise noted.)

MC75491

FIGURE 1 – COLLECTOR CURRENT versus INPUT VOLTAGE

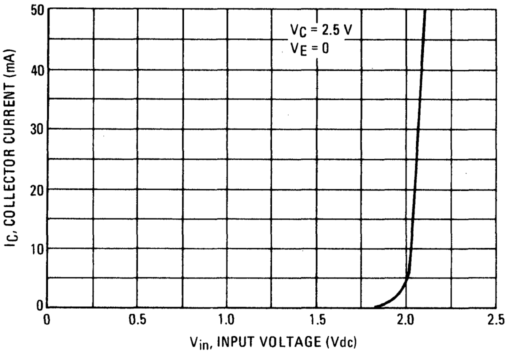


FIGURE 3 – COLLECTOR CURRENT versus INPUT CURRENT

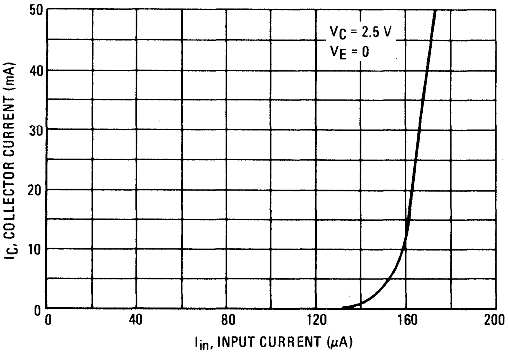
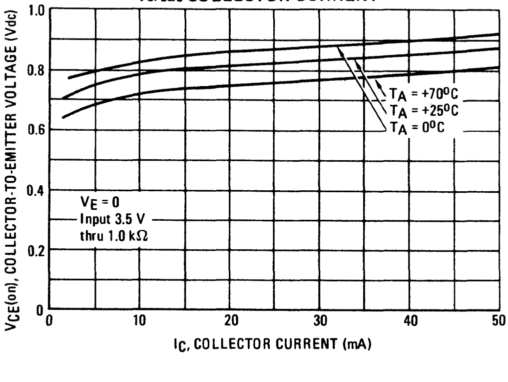


FIGURE 5 – COLLECTOR-TO-EMITTER VOLTAGE (ON) versus COLLECTOR CURRENT



MC75492

FIGURE 2 – OUTPUT CURRENT versus INPUT VOLTAGE

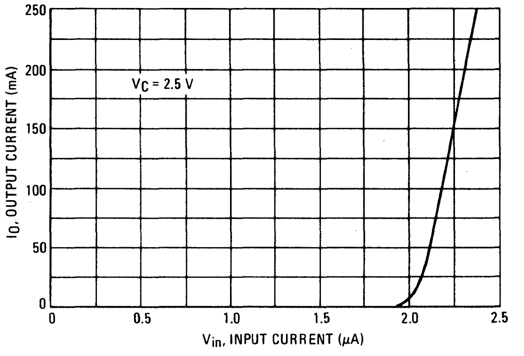


FIGURE 4 – OUTPUT CURRENT versus INPUT CURRENT

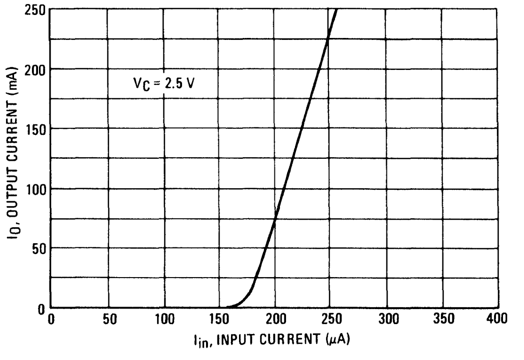
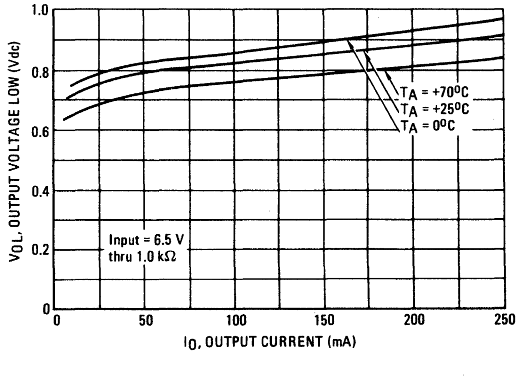


FIGURE 6 – OUTPUT VOLTAGE LOW versus OUTPUT CURRENT



8

TYPICAL CHARACTERISTICS and SWITCHING TIME CIRCUITS

FIGURE 7 – MC75491/MC75492 INPUT CURRENT versus INPUT VOLTAGE

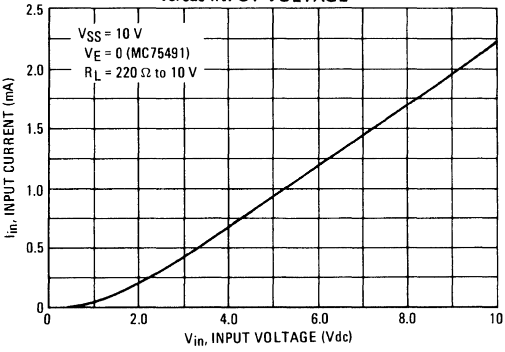


FIGURE 8 – MC75491 SWITCHING CIRCUIT

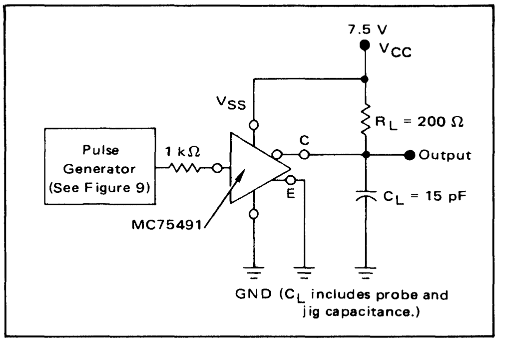
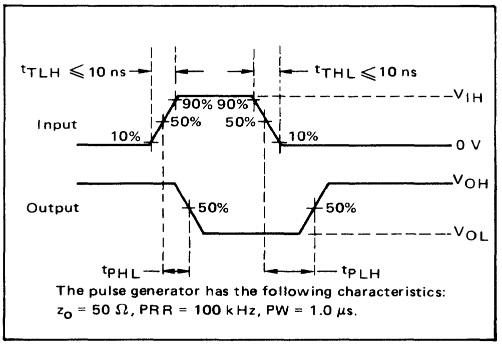
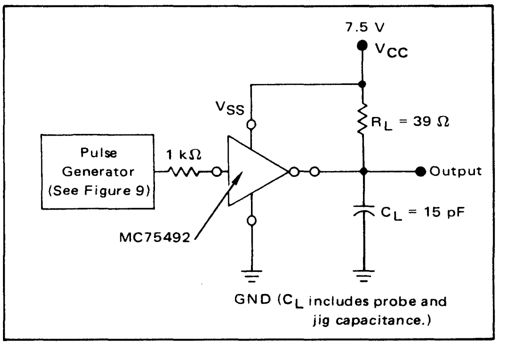


FIGURE 9 – SWITCHING WAVEFORM DEFINITIONS



The pulse generator has the following characteristics: z_o = 50 Ω, PRR = 100 kHz, PW = 1.0 μs.

FIGURE 10 – MC75492 SWITCHING CIRCUIT



TYPICAL APPLICATIONS

FIGURE 11 – QUAD-OR-HEX RELAY DRIVER

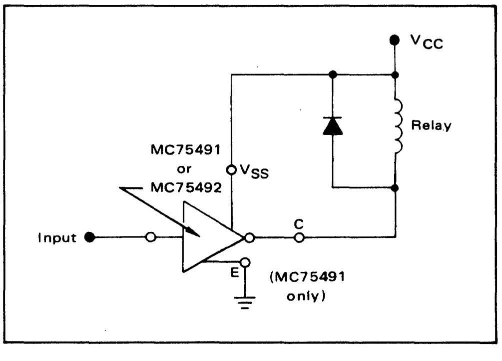
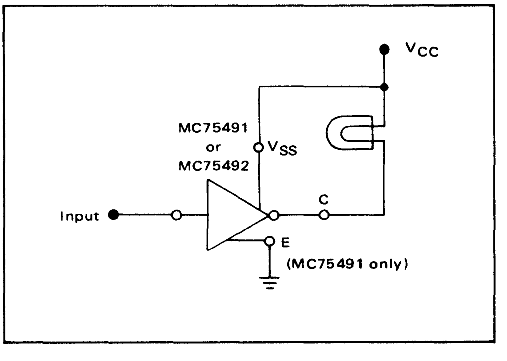


FIGURE 12 – QUAD-OR-HEX LAMP DRIVER



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TYPICAL APPLICATIONS (continued)

FIGURE 13 – MOS-TO-MTTL LEVEL TRANSLATOR

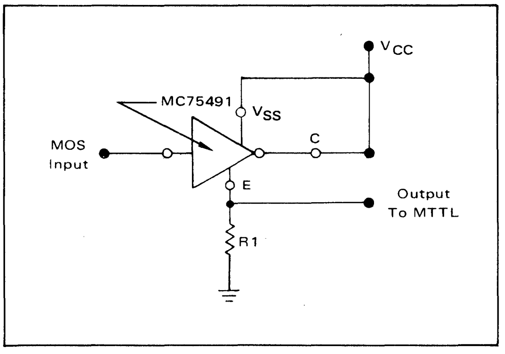


FIGURE 14 – QUAD HIGH-CURRENT NPN TRANSISTOR DRIVER

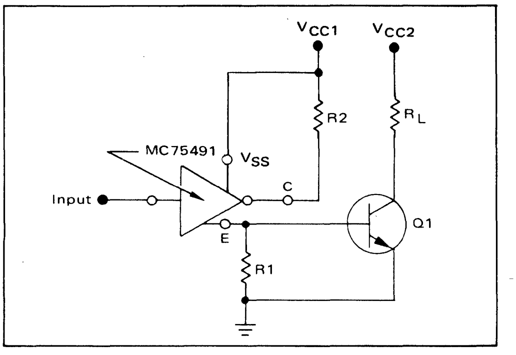


FIGURE 15 – QUAD-OR-HEX HIGH-CURRENT PNP TRANSISTOR DRIVER

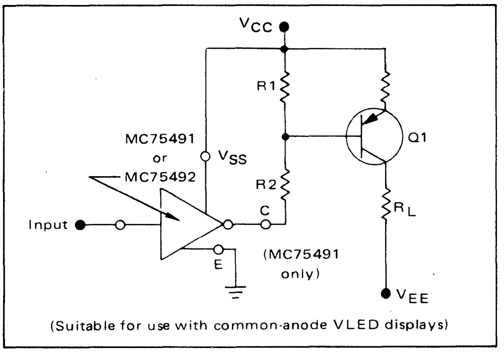


FIGURE 16 – BASE-EMITTER SELECT TRANSISTOR DRIVER

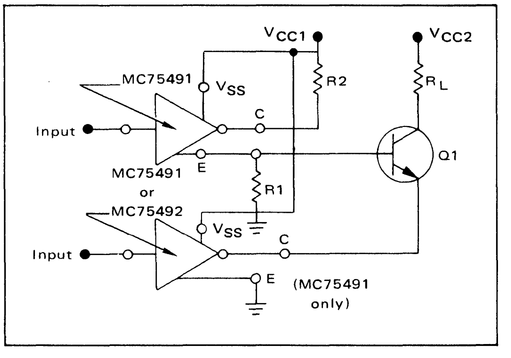
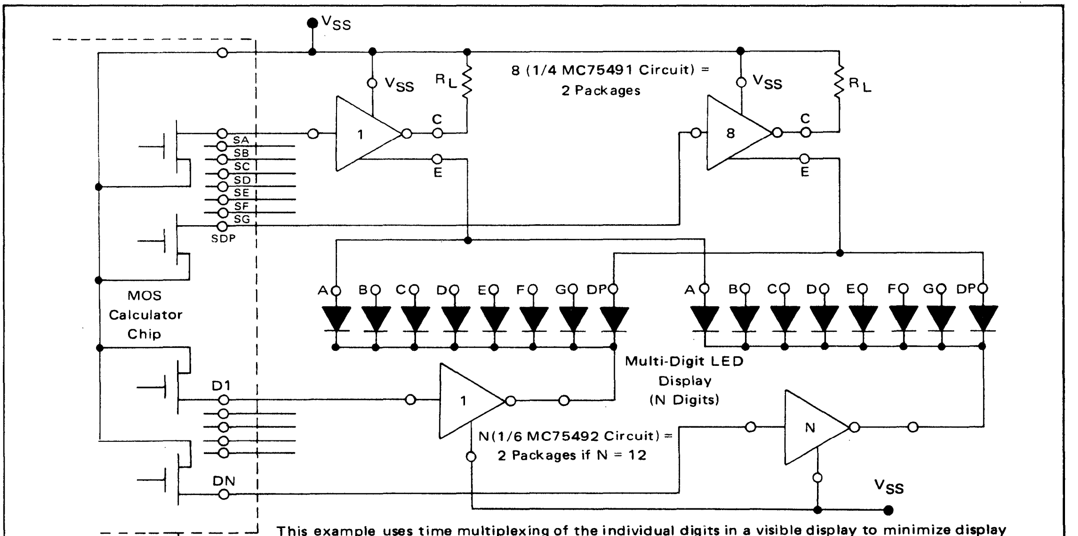


FIGURE 17 – MOS CALCULATOR CHIP-TO-LED INTERFACE CIRCUIT



This example uses time multiplexing of the individual digits in a visible display to minimize display circuitry. Up to twelve digits, each of which use a seven-segment display with decimal point, may be displayed using only two MC75491 and two MC75492 drivers.

TYPICAL APPLICATIONS (continued)

FIGURE 18 – STROBED "NOR" DRIVER

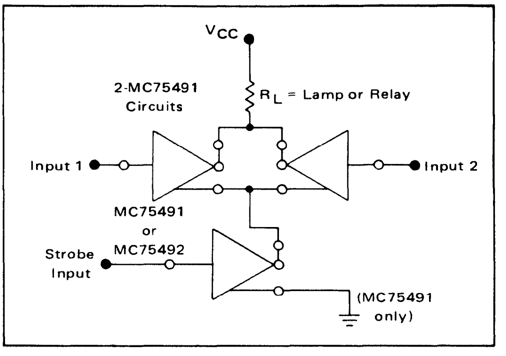
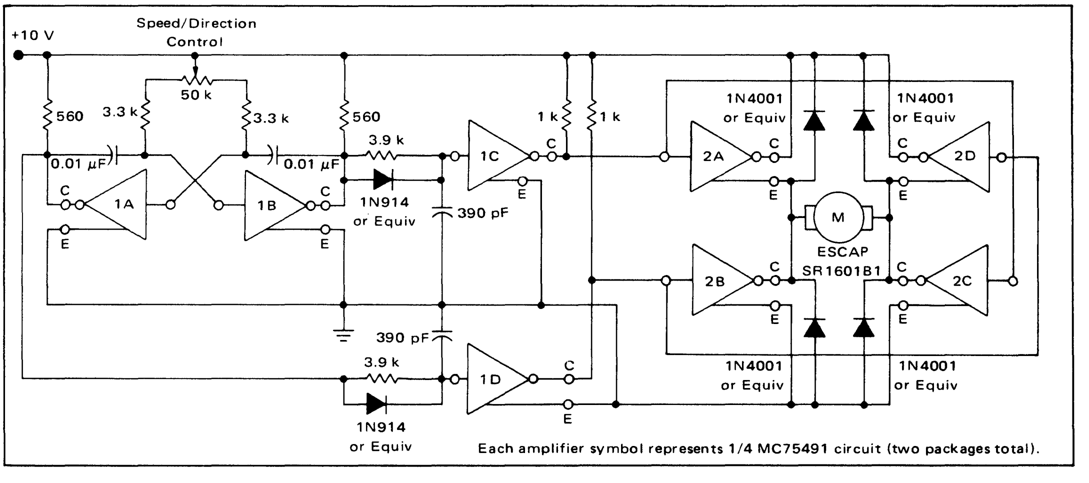


FIGURE 19 – DC MOTOR SPEED/DIRECTION CONTROL CIRCUIT



8

MCBC1709
MCB1709F

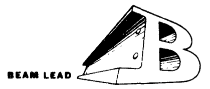
MONOLITHIC OPERATIONAL AMPLIFIER

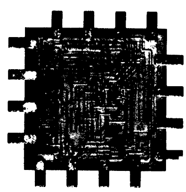
Beam-lead sealed-junction technology and fabrication make the MCBC1709 and MCB1709F devices excellent choices for military, aerospace, and commercial applications; usages requiring a high degree of reliability under environmental conditions of severe temperature extremes, mechanical shock, and high humidity. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metalized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift — ±3.0 $\mu V/^{\circ}C$
- Large Output Voltage Swing — ±14 V typical @ ±15 V Supply
- Low Output Impedance — Z_{out} = 150 ohms typical

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

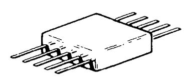
MONOLITHIC SILICON





BEAM-LEAD CHIP
MCBC1709

CERAMIC PACKAGE
CASE 606
(TO-91)

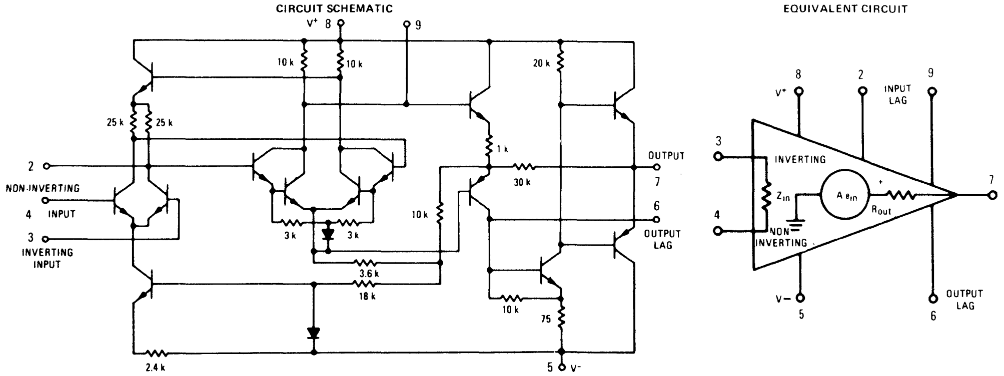


MCB1709F

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation Derate above T_A = +25°C	P_D	500 3.3	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1



Pin numbers shown are for Case 665, refer to Figure 10 for chip bonding diagram.

See Packaging Information Section for outline dimensions.

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ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCBC1709 and MCB1709F			Unit
		Min	Typ	Max	
Open Loop Voltage Gain (V_O = ±10 V, T_A = -55°C to +125°C)	A_{VOL}	25,000	45,000	70,000	–
Output Impedance (f = 20 Hz)	Z_{out}	–	150	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	150	400	–	kΩ
Output Voltage Swing	V_O				V_{peak}
(R_L = 10 kΩ)		±12	±14	–	
(R_L = 2.0 kΩ)		±10	±13	–	
Input Common-Mode Voltage Swing	CMV_{in}	±8.0	±10	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	70	90	–	dB
Input Bias Current	I_b				μA
(T_A = +25°C)		–	0.2	0.5	
(T_A = -55°C)		–	0.5	1.5	
Input Offset Current	$\|I_{io}\|$				μA
(T_A = +25°C)		–	0.05	0.2	
(T_A = -55°C)		–	–	0.5	
(T_A = +125°C)		–	–	0.2	
Input Offset Voltage	$\|V_{io}\|$				mV
(T_A = +25°C)		–	1.0	5.0	
(T_A = -55°C to +125°C)		–	–	6.0	
Step Response					
Gain = 100, 5.0% overshoot, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF	t_f	–	0.8	–	μs
	t_{pd}	–	0.38	–	μs
	dV_{out}/dt ①	–	12	–	V/μs
Gain = 10, 10% overshoot, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF	t_f	–	0.6	–	μs
	t_{pd}	–	0.34	–	μs
	dV_{out}/dt ①	–	1.7	–	V/μs
Gain = 1, 5.0% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_f	–	2.2	–	μs
	t_{pd}	–	1.3	–	μs
	dV_{out}/dt ①	–	0.25	–	V/μs
Average Temperature Coefficient of Input Offset Voltage	$\|TC_{Vio}\|$				μV/°C
(R_S = 50 Ω, T_A = -55°C to +125°C)		–	3.0	–	
($R_S \leq$ 10 kΩ, T_A = -55°C to +125°C)		–	6.0	–	
DC Power Dissipation (Power Supply = ±15 V, V_O = 0)	P_D	–	80	165	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	25	150	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	25	150	μV/V

① dV_{out}/dt = Slew Rate

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT
V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C

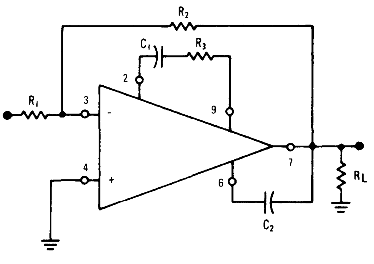


Fig. No.	Curve No.	Test Conditions				
		R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (pF)	C_2 (pF)
3	1	10 k	10 k	1.5 k	5.0 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1.0 M	1.5 k	100	3.0
	4	1.0 k	1.0 M	0	10	3.0
4	1	1.0 k	1.0 M	0	10	3.0
	2	10 k	1.0 M	1.5 k	100	3.0
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5.0 k	200
5	1	0	∞	1.5 k	5.0 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3.0
	4	0	∞	0	10	3.0

TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY

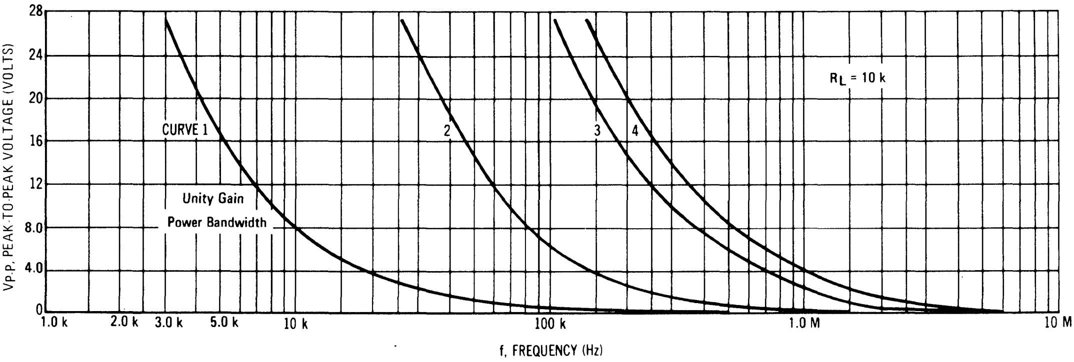


FIGURE 4 – VOLTAGE GAIN versus FREQUENCY

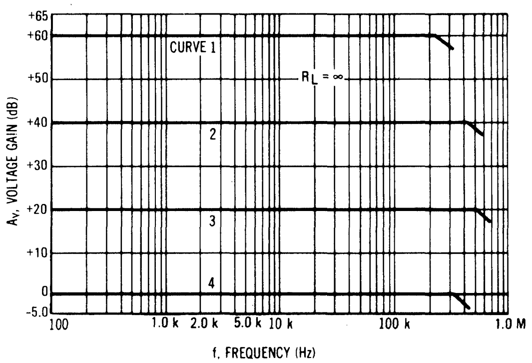


FIGURE 5 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

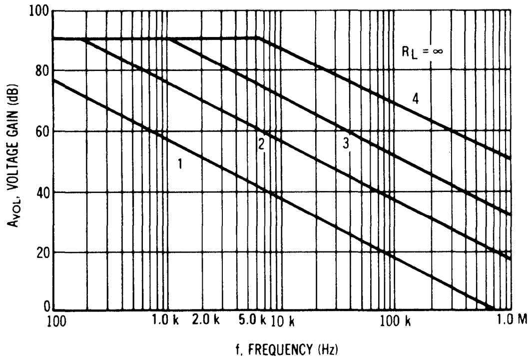


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

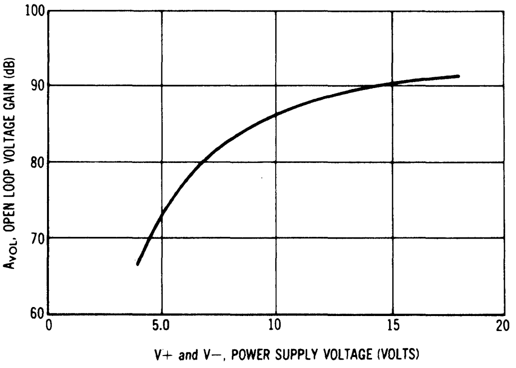
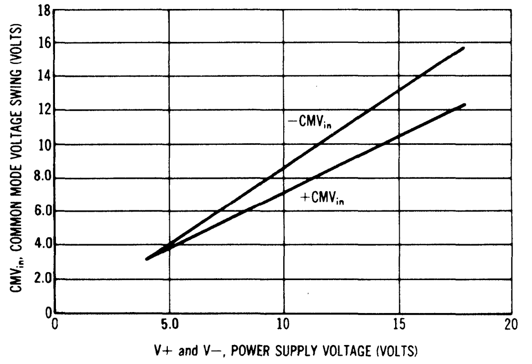


FIGURE 7 – COMMON SWING versus POWER SUPPLY VOLTAGE



8

TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

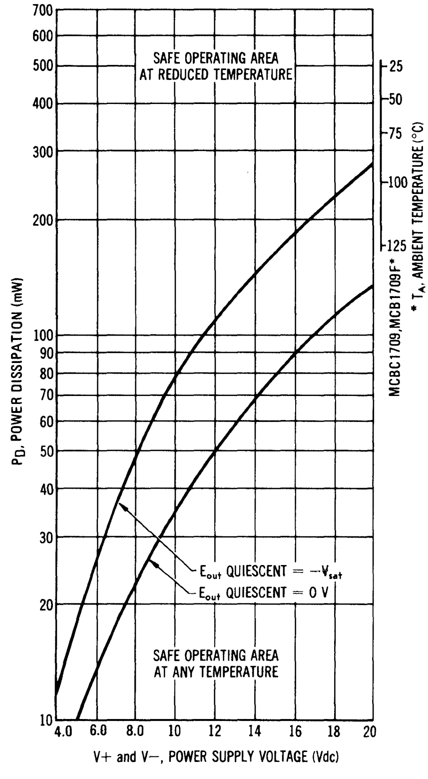


FIGURE 9 – INPUT NOISE VOLTAGE versus SOURCE RESISTANCE

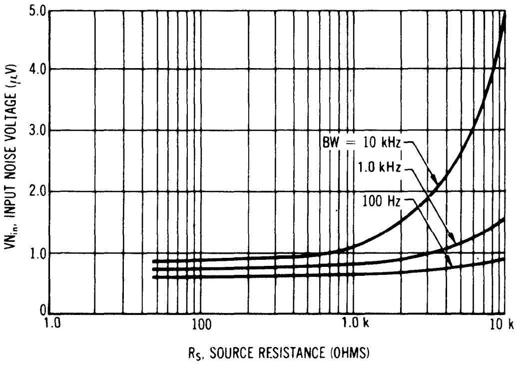
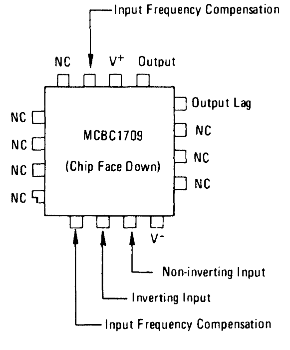
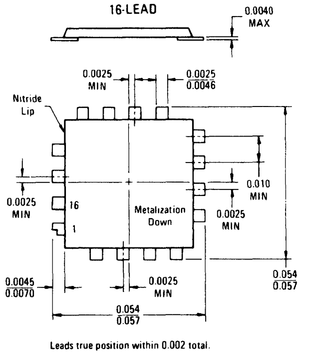


FIGURE 10 – BONDING DIAGRAM



Silicon Thickness = 2.0 mils nominal



Leads true position within 0.002 total.

PACKAGING AND HANDLING

The MCBC1709 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

8

MCBC1710
MCB1710F

DIFFERENTIAL COMPARATOR

Advance Information

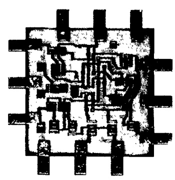
MONOLITHIC DIFFERENTIAL VOLTAGE COMPARATOR

Beam-lead sealed-junction technology and fabrication make the MCBC1710 and MCB1710F devices excellent choices for military, aerospace, and commercial applications. These devices are designed for use in level detection, low-level sensing, and memory applications.

- Differential Input Characteristics –
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 3.0 μV/°C
- Fast Response Time – 40 ns
- Output Compatible With All Saturating Logic Forms –
  V_O = +3.2 V to -0.5 V Typical
- Low Output Impedance – 200 ohms

DIFFERENTIAL COMPARATOR INTEGRATED CIRCUIT MONOLITHIC SILICON

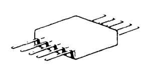
BEAM LEAD



BEAM-LEAD CHIP

MCBC1710

F SUFFIX
CERAMIC PACKAGE
CASE 606
(TO-91)



MCB1710F

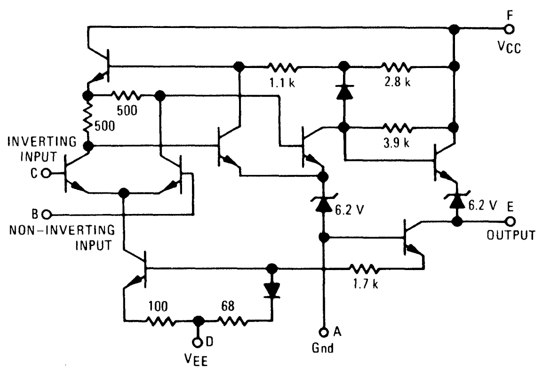
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+14	Vdc
	V_{EE}	−7.0	Vdc
Differential Input Signal	V_{ID}	±5.0	Volts
Common Mode Input Swing	V_{ICR}	±7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (package limitations)	P_D		
Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

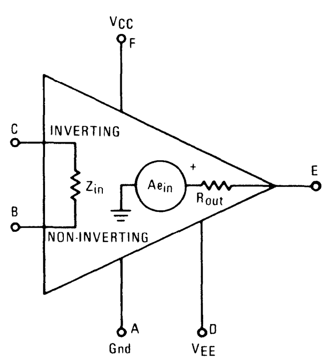
SCHEMATIC PIN CONNECTIONS

Chip	A	B	C	D	E	F
"F" Package	1	2	3	5	6	8

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



This is advance information on a new introduction and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

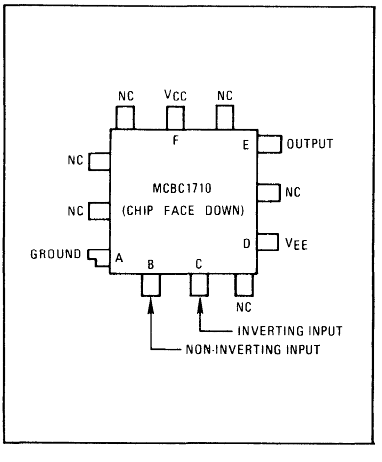
8

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = -6.0 Vdc, T_A = 25°C unless otherwise noted)

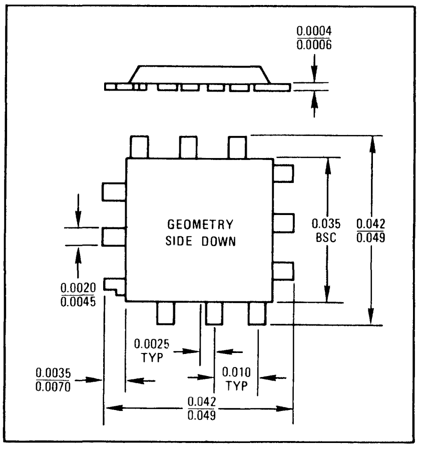
		MCBC1710/MCB1710F			
Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_O = 1.4 Vdc)	V_{IO}	–	1.0	2.0	mVdc
Input Bias Current (V_O = 1.4 Vdc)	I_{IB}	–	12	20	µAdc
Output Resistance	r_o	–	200	–	Ohms
Positive Output Voltage ($V_{in} \geq 5.0$ mV, $0 \leq I_o \leq 5.0$ mA)	V_{OH}	2.5	3.2	4.0	Vdc
Negative Output Voltage ($V_{in} \geq -5.0$ mV)	V_{OL}	-1.0	-0.5	0	Vdc
Output Sink Current ($V_{in} \geq -5.0$ mV, $V_{out} \geq 0$)	I_s	2.0	2.5	–	mAdc
Common Mode Rejection Ratio (V_O = -7.0 Vdc, $R_S \leq 200\ \Omega$)	CMRR	–	100	–	dB
Propagation Delay Time For Positive and Negative Going Input Pulse	t_{pd}	–	40	–	ns
Power Supply Current ($V_O \leq 0$ Vdc)	$I_{D}+$ $I_{D}-$	– –	6.4 5.5	9.0 7.0	mAdc
DC Quiescent Power Dissipation	P_D	–	115	150	mW

See current MC1710/1710C data sheet for additional information.

BONDING DIAGRAM



12 – BEAM CHIP



PACKAGING AND HANDLING

The MCBC1710 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

8

VOLTAGE REGULATORS

MCBC1723
MCB1723F

Advance Information

MONOLITHIC BEAM-LEAD VOLTAGE REGULATOR

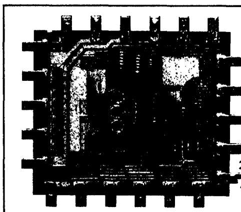
The MCBC1723/MCB1723F is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metalized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line Regulation
- Adjustable Short-Circuit Protection

BEAM-LEAD VOLTAGE REGULATOR INTEGRATED CIRCUIT

BEAM LEAD

▲Trademark of Motorola Inc

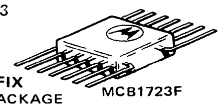


BEAM-LEAD CHIP

22

1

MCBC1723



F SUFFIX
CERAMIC PACKAGE
CASE 607

MCB1723F

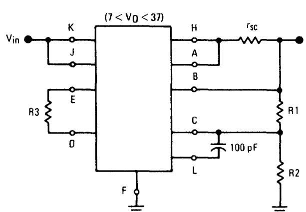
SCHEMATIC PIN CONNECTIONS

Chip	A	B	C	D	E	F	G	H	J	K	L
"F" Package	2	3	4	5	6	7	9	10	11	12	13

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Pulse Voltage from V_{CC} to V_{EE} (50 ms)	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V_{CC} to V_{EE}	V_{in}	40	Vdc
Input-Output Voltage Differential	$V_{in}-V_O$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Operating Temperature Range	T_A	-55 to +125	°C
Junction Temperature Range	T_J	-65 to +150	°C

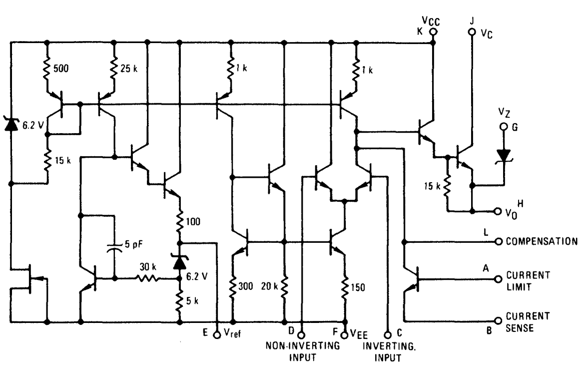
FIGURE 1 – TYPICAL CIRCUIT CONNECTION



$V_O \cong 7\left(\frac{R1 + R2}{R2}\right)$ $I_{sc} = \frac{V_{sense}}{r_{sc}} = \frac{0.66}{r_{sc}}$ at T_J = 25°C

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1||R2

FIGURE 2 – CIRCUIT SCHEMATIC



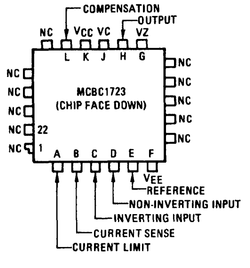
This is advance information on a new introduction and specifications are subject to change without notice.

8

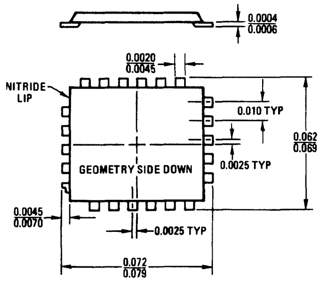
ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} = 12 Vdc, V_o = 5 Vdc, I_L = 1 mAdc, r_{sc} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 1)

Characteristic	Symbol	MCBC1723/MCB1723F			Unit
		Min	Typ	Max	
Input Voltage Range	V_{in}	9.5	–	40	Vdc
Output Voltage Range	V_O	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_O$	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{IB}	–	2.3	3.5	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_n				μV(rms)
C_{ref} = 0		–	20	–	
C_{ref} = 5.0 μF		–	2.5	–	
Line Regulation	Reg_{in}				$\%V_O$
(12 V < V_{in} < 15 V)		–	0.01	0.1	
(12 V < V_{in} < 40 V)		–	0.02	0.2	
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_{load}	–	0.03	0.15	$\%V_O$
Ripple Rejection (f = 50 Hz to 10 kHz)	Rej_R				dB
C_{ref} = 0		–	74	–	
C_{ref} = 5.0 μF		–	86	–	
Short Circuit Current Limit (r_{sc} = 10 Ω, V_O = 0)	I_{sc}	–	65	–	mAdc

BONDING DIAGRAM



22-BEAM CHIP



PACKAGING AND HANDLING

The MCBC1723 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

8

OPERATIONAL AMPLIFIERS

MCBC1741
MCB1741F

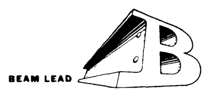
MONOLITHIC OPERATIONAL AMPLIFIER

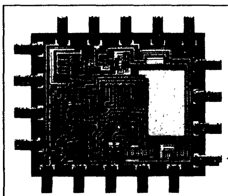
Beam-lead sealed-junction technology and fabrication make the MCBC1741 and MCB1741F devices excellent choices for military, aerospace, and commercial applications; usages requiring a high degree of reliability under environmental conditions of severe temperature extremes, mechanical shock, and high humidity. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metalized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

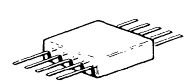
MONOLITHIC SILICON





BEAM-LEAD CHIP
MCBC1741

CERAMIC PACKAGE
CASE 606
(TO-91)



MCB1741F

SCHEMATIC PIN CONNECTIONS

Chip	A	B	C	D	E	F	G
"F" Package	2	3	4	5	6	7	8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+22 -22	Vdc
Differential Input Signal	V_{in}	±30	Volts
Common Mode Input Swing (Note 1)	CMV_{in}	±15	Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous	
Power Dissipation Derate above T_A = +25°C (Flat Package)	P_D	500 3.3	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

FIGURE 1 – CIRCUIT SCHEMATIC

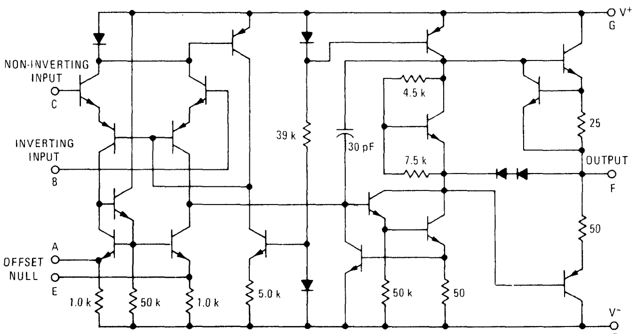
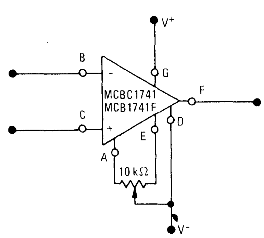


FIGURE 2 – OFFSET ADJUST CIRCUIT



See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCBC1741, MCB1741F Min	Typ	Max	Unit
Open Loop Voltage Gain (R_L = 2.0 kΩ)	A_{VOL}				–
(V_o = ±10 V, T_A = +25°C)		50,000	200,000	–	
(V_o = ± 10 V, T_A = −55 to +125°C)		25,000	–	–	
Output Impedance (f = 20 Hz)	Z_o	–	75	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	0.3	1.0	–	MegΩ
Output Voltage Swing	V_o				V_{peak}
(R_L = 10 kΩ)		±12	±14	–	
(R_L = 2.0 kΩ)		±10	±13	–	
(R_L = 2.0 kΩ, T_A = −55 to +125°C)		±10	–	–	
Input Common-Mode Voltage Swing	CMV_{in}	±12	±13	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	70	90	–	dB
Input Bias Current	I_b				μA
(T_A = +25°C)		–	0.2	0.5	
(T_A = −55°C)		–	0.5	1.5	
Input Offset Current	$\|I_{io}\|$				μA
(T_A = +25°C)		–	0.03	0.2	
(T_A = −55 to +125°C)		–	–	0.5	
Input Offset Voltage	$\|V_{io}\|$				mV
(T_A = +25°C)		–	1.0	5.0	
(T_A = −55°C to +125°C)		–	–	6.0	
Step Response					
Gain = 100, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.0 kΩ	t_f	–	29	–	μs
	t_{pd}	–	8.5	–	μs
	dV_{out}/dt ①	–	1.0	–	V/μs
Gain = 10, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.0 kΩ	t_f	–	3.0	–	μs
	t_{pd}	–	1.0	–	μs
	dV_{out}/dt ①	–	1.0	–	V/μs
Gain = 1, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5.0 kΩ	t_f	–	0.6	–	μs
	t_{pd}	–	0.38	–	μs
	dV_{out}/dt ①	–	0.8	–	V/μs
Average Temperature Coefficient of Input Offset Voltage	$\|TC_{Vio}\|$				μV/°C
(R_S = 50 Ω, T_A = −55°C to +125°C)		–	3.0	–	
(R_S = 10 kΩ, T_A = −55°C to +125°C)		–	6.0	–	
Average Temperature Coefficient of Input Offset Current (T_A = −55 to +125°C)	$\|TC_{Vio}\|$	–	50	–	pA/°C
DC Power Dissipation (Power Supply = ±15 V, V_o = 0)	P_D	–	50	85	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	30	150	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	30	150	μV/V
Power Bandwidth (A_V = 1, R_L = 2.0 kΩ, THD = 5%, V_o = 20 $V_{p\text{-}p}$)	PBW	–	10	–	kHz

① dV_{out}/dt = Slew Rate

8

TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^{\circ}C$ unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

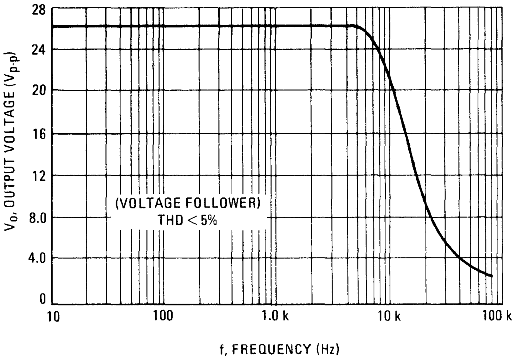


FIGURE 4 – OPEN LOOP FREQUENCY RESPONSE

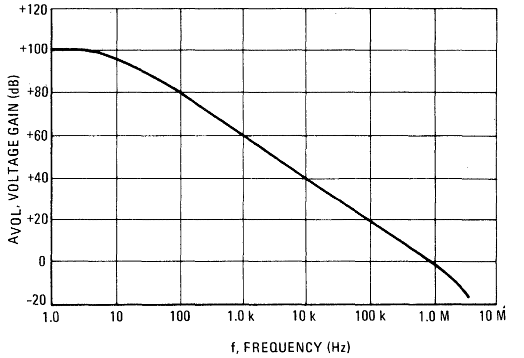


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

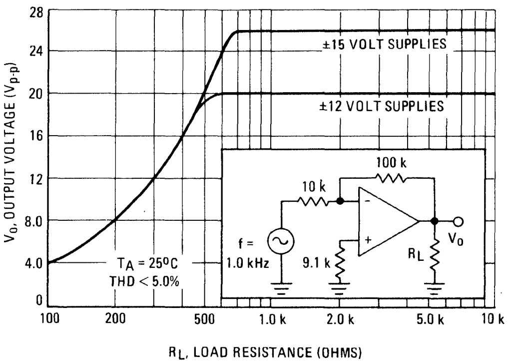


FIGURE 6 – COMMON-MODE REJECTION RATIO versus FREQUENCY

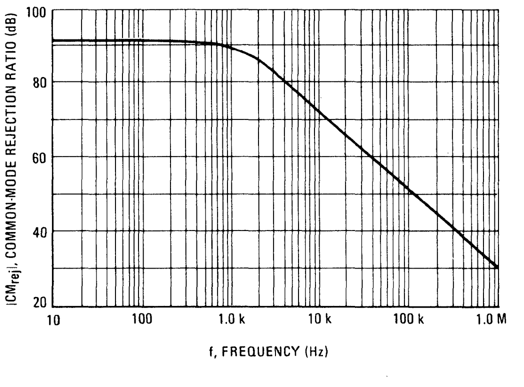


FIGURE 7 – INPUT OFFSET CURRENT versus TEMPERATURE

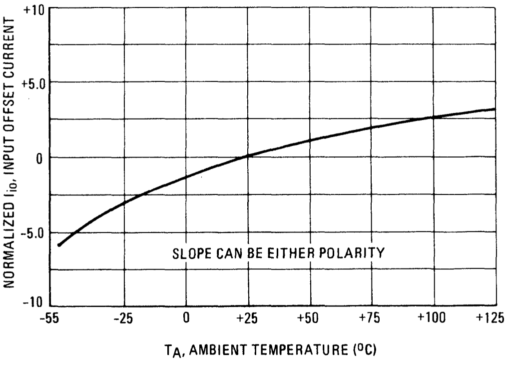
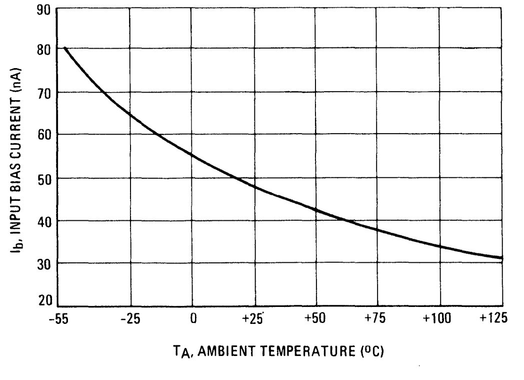


FIGURE 8 – INPUT BIAS CURRENT versus TEMPERATURE



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TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted.)

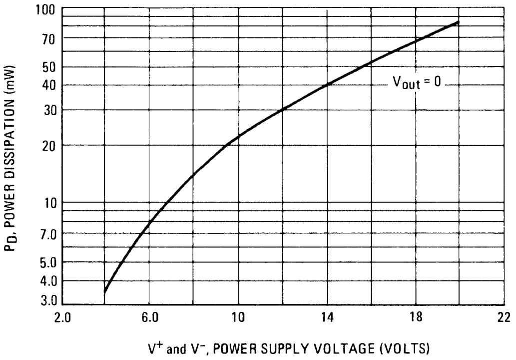


FIGURE 9 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

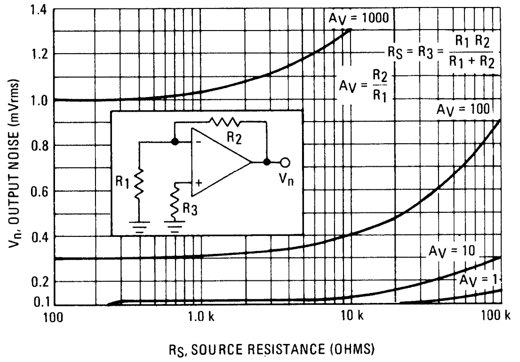
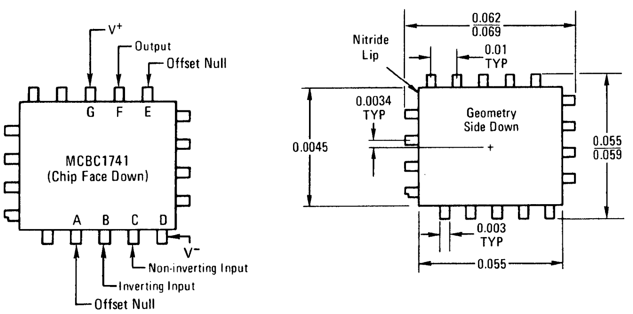


FIGURE 10 – OUTPUT NOISE versus SOURCE RESISTANCE

FIGURE 11 – BONDING DIAGRAM



Silicon Thickness = 2.0 mils nominal

PACKAGING AND HANDLING

The MCBC1741 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

8

MCBC1748
MCB1748F

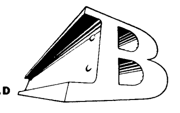
Advance Information

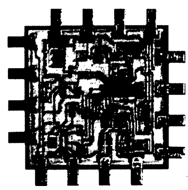
HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

Beam-lead sealed-junction technology and fabrication make the MCBC1748 and MCB1748F devices excellent choices for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metalized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

- Noncompensated MCBC1741
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

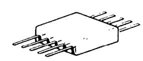




BEAM-LEAD CHIP

MCBC1748

F SUFFIX
CERAMIC PACKAGE
CASE 606
(TO-91)



MCB1748F

SCHEMATIC PIN CONNECTIONS

Chip	A	B	C	D	E	F	G	H
"F" Package	2	3	4	5	6	7	8	9

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing ①	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation Derate above T_A = +25°C (Flat Package)	P_D	500 3.3	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.

FIGURE 1 – CIRCUIT SCHEMATIC

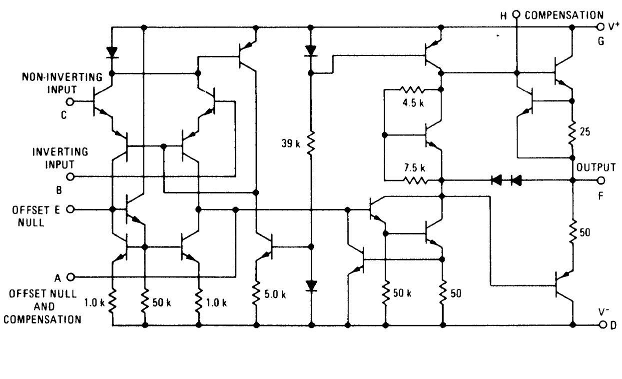
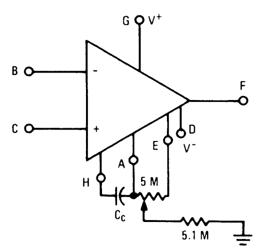


FIGURE 2 – OFFSET ADJUST AND FREQUENCY COMPENSATION



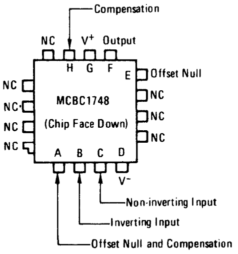
This is advance information on a new introduction and specifications are subject to change without notice.

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

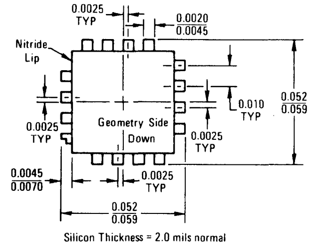
Characteristics	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain, (V_O = +10 V, R_L = 2.0 k ohms)	A_{VOL}	50,000	200,000	–	–
Output Impedance (f = 20 Hz)	Z_o	–	75	–	ohms
Common Mode Input Impedance (f = 20 Hz)	Z_{in}	–	200	–	Megohms
Output Voltage Swing (R_L = 10 k ohms) R_L = 2 k ohms (T_A = -55 to +125°C)	V_o	±12 ±10	±14 ±13	– –	Vpk
Common-Mode Input Voltage Swing	CMV_{in}	–	±13	–	Vpk
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	–	90	–	dB
Input Bias Current	I_b	–	0.08	0.5	μAdc
Input Offset Current	I_{io}	–	0.02	0.2	μAdc
Input Offset Voltage ($R_S \leqslant 10\ k\Omega$)	V_{io}	–	1.0	5.0	mVdc
Step Response (V_{in} = 20 mV, C_c = 30 pF, R_L = 2 kΩ, C_L = 100 pF) Rise Time Overshoot Percentage Slew Rate	 t_r dV_{out}/dt	 – – –	 0.3 5.0 0.8	 – – –	 μs % V/μs
Short-Circuit Output Current	I_{SC}	–	25	–	mAdc
Differential Input Impedance (Open-Loop, f = 20 Hz) Parallel Input Resistance Parallel Input Capacitance	 Rp Cp	 – –	 2.0 1.4	 – –	 Megohms pF
Power Supply Sensitivity V^- = constant, $R_S \leqslant 10$ k ohms V^+ = constant, $R_S \leqslant 10$ k ohms	 S+ S-	 – –	 30 30	 150 150	μV/V
Power Supply Current	I_{D+} I_{D-}	– –	1.67 1.67	2.83 2.83	mAdc
DC Quiescent Power Dissipation (V_O = 0)	P_D	–	50	85	mW

BONDING DIAGRAM



Silicon Thickness = 2.0 mils nominal

16-BEAM CHIP



Silicon Thickness = 2.0 mils normal

PACKAGING AND HANDLING

The MCBC1748 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

MCC1536
MCC1436

HIGH VOLTAGE, INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER CHIP

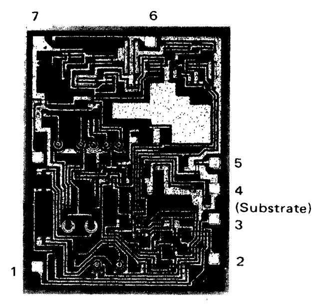
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1536 and MCC1436 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Maximum Supply Voltage – ±40 Vdc
- Output Voltage Swing –
  $\pm 30\ V_{pk(min)}$ ($V^+ = +36$ V, $V^- = -36$ V)
  $\pm 22\ V_{pk(min)}$ ($V^+ = +28$ V, $V^- = -28$ V)
- Input Bias Current – 20 nA max
- Input Offset Current – 3.0 nA max
- Fast Slew Rate – 2.0 V/µs typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- A_{VOL} – 500,000 typ
- Characteristics Independent of Power Supply Voltages – (±5.0 Vdc to ±36 Vdc)

OPERATIONAL AMPLIFIER CHIP MONOLITHIC SILICON INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED



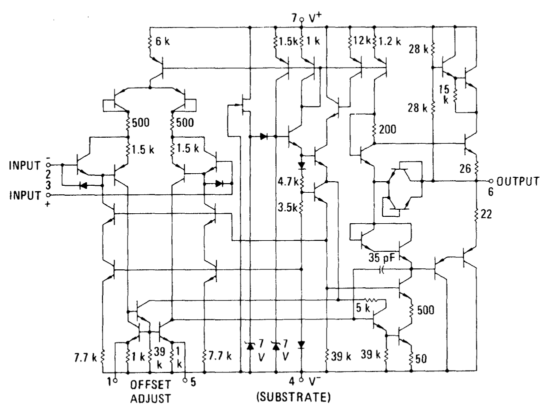
MCC1536/MCC1436

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

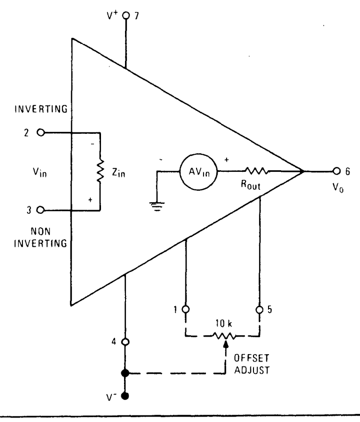
Rating		Symbol	MCC1536	MCC1436	Unit
Power Supply Voltage		V^+ V^-	+40 -40	+34 -34	Vdc
Differential Input Signal (1)		V_{in}	$\pm(V^+ + \lvert V^-\rvert - 3)$		Volts
Common-Mode Input Swing		CMV_{in}	$+V^+, -(\lvert V^-\rvert - 3)$		Volts
Output Short Circuit Duration ($V^+ = \lvert V^-\rvert$ = 28 Vdc, V_O = 0)		T_{SC}	5.0		s
Operating Temperature Range	MCC1536 MCC1436	T_A	-55 to +125 0 to +75		°C
Junction Temperature Range		T_{stg}	-65 to +150		°C

(1) The absolute voltage applied to either input terminal must not exceed $+V^+, -(\lvert V^-\rvert - 3)$.

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



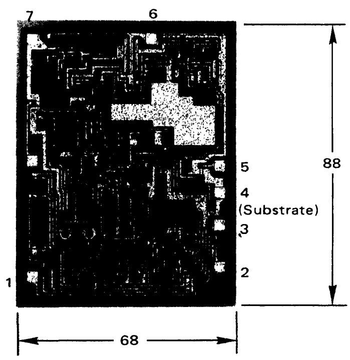
MCC1536, MCC1436 (continued)

ELECTRICAL CHARACTERISTICS (V^+ = +28 Vdc, V^- = -28 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MCC1536			MCC1436			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_b	–	8.0	20	–	15	40	nAdc
Input Offset Current	$\|I_{io}\|$	–	1.0	3.0	–	5.0	10	nAdc
Input Offset Voltage	$\|V_{io}\|$	–	2.0	5.0	–	5.0	10	mVdc
Differential Input Impedance (Open-Loop, f ≤ 5.0 Hz)								
Parallel Input Resistance	R_p	–	10	–	–	10	–	Meg ohms
Parallel Input Capacitance	C_p	–	2.0	–	–	2.0	–	pF
Common-Mode Input Impedance (f ≤ 5.0 Hz)	$Z_{(in)}$	–	250	–	–	250		Meg ohms
Common-Mode Input Voltage Swing	CMV_{in}	–	±25	–	–	±25	–	V_{pk}
Common-Mode Rejection Ratio (dc)	CM_{rej}	–	110	–	–	110	–	dB
Large Signal dc Open Loop Voltage Gain	A_{VOL}							V/V
(V_O = ± 10 V, R_L = 100 k ohms)		100,000	500,000	–	70,000	500,000	–	
(V_O = ±10 V, R_L = 10 k ohms)		–	200,000	–	–	200,000	–	
Power Bandwidth (Voltage Follower) (A_V = 1, R_L = 5.0 k ohms, THD ≤ 5%, V_O = 40 Vp-p)	P_{BW}	–	23	–	–	23	–	kHz
Unity Gain Crossover Frequency (open-loop)		–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)		–	50	–	–	50	–	degrees
Gain Margin		–	18	–	–	18	–	dB
Slew Rate (Unity Gain)	dV_{out}/dt	–	2.0	–	–	2.0	–	V/µs
Output Impedance (f ≤ 5.0 Hz)	Z_{out}	–	1.0	–	–	1.0	–	k ohms
Short-Circuit Output Current	I_{SC}	–	±17	–	–	±17	–	mAdc
Output Voltage Swing (R_L = 5.0 k ohms)	V_o							V_{pk}
V^+ = +28 Vdc, V^- = -28 Vdc		±22	±23	–	±20	±22	–	
V^+ = +36 Vdc, V^- = -36 Vdc		±30	±32	–	–	–	–	
Power Supply Sensitivity (dc)								µV/V
V^- = constant, R_s ≤ 10 k ohms	S+	–	15	100	–	35	200	
V^+ = constant, R_s ≤ 10 k ohms	S-	–	15	100	–	35	200	
Power Supply Current	I_{D+}	–	2.2	4.0	–	2.6	5.0	mAdc
	I_{D-}	–	2.2	4.0	–	2.6	5.0	
DC Quiescent Power Dissipation (V_O = 0)	P_D	–	124	224	–	146	280	mW

See current MC1536/1436 data sheet for additional information.

MCC1536/MCC1436 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

PACKAGING AND HANDLING

The MCC1536/MCC1436 operational amplifier is now available in die (chip) form. The phosphorsilicate passivation protects the metalization and active area of the die but care must be excercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

8

OPERATIONAL AMPLIFIERS

MCC1539
MCC1439

MONOLITHIC OPERATIONAL AMPLIFIER CHIP

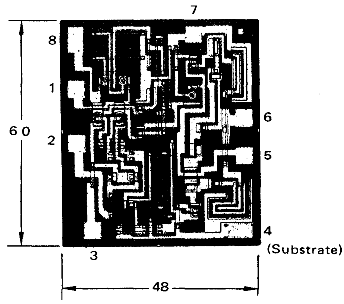
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information see Motorola Application Note AN-439.

The MCC1539 and MCC1439 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Low Input Offset Voltage – 3.0 mV max
- Low Input Offset Current – 60 nA max
- Large Power-Bandwidth – 20 V_{p-p} Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- Slew Rate – 34 V/µs typ

OPERATIONAL AMPLIFIER CHIP INTEGRATED CIRCUIT

MONOLITHIC SILICON

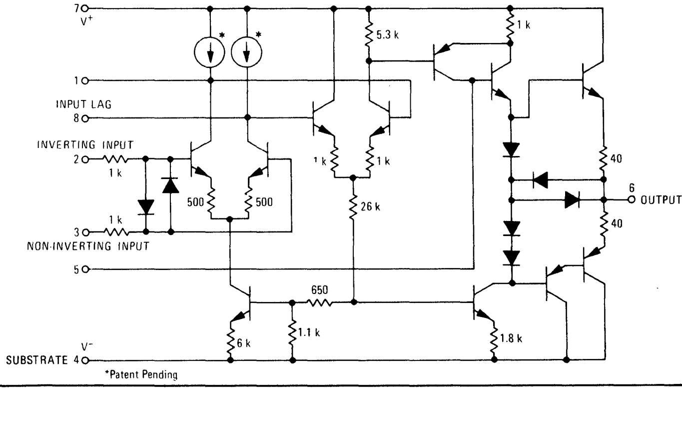


All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

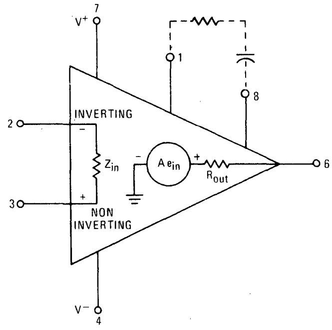
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	$\pm[V^+ + \lvert V^- \rvert]$	Vdc
Common Mode Input Swing	CMV_{in}	$+V^+, -\lvert V^- \rvert$	Vdc
Load Current	I_L	15	mA
Output Short Circuit Duration	t_S	Continuous	
Operating Temperature Range MCC1539 MCC1439	T_A	-55 to +125 0 to +75	°C
Junction Temperature Range	T_J	-65 to +150	°C

FIGURE 1 – CIRCUIT SCHEMATIC



*Patent Pending

FIGURE 2 – EQUIVALENT CIRCUIT



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ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1539 Min	MCC1539 Typ	MCC1539 Max	MCC1439 Min	MCC1439 Typ	MCC1439 Max	Unit
Input Bias Current	I_b	–	0.20	0.50	–	0.20	1.0	μA
Input Offset Current	$\lvert I_{io} \rvert$	–	20	60	–	20	100	nA
Input Offset Voltage	$\lvert V_{io} \rvert$	–	1.0	3.0	–	2.0	7.5	mV
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)	$\lvert TCV_{io} \rvert$	–	3.0	–	–	3.0	–	μV/°C
Input Impedance	Z_{in}	–	300	–	–	300	–	kΩ
Input Common-Mode Voltage Swing	CMV_{in}	–	±12	–	–	±12	–	V_{pk}
Common Mode Rejection Ratio (f = 1.0 kHz)	CM_{rej}	–	110	–	–	110	–	dB
Open Loop Voltage Gain (V_o = ±10 V, R_L = 10 kΩ)	A_{VOL}	50,000	120,000	–	15,000	100,000	–	–
Power Bandwidth (A_V = 1, THD ≤ 5%, V_o = 20 Vp-p, R_L = 1.0 kΩ)	PBW	–	50	–	–	50	–	kHz
Step Response								
Gain = 1000, no overshoot,	t_f	–	130	–	–	130	–	ns
	t_{pd}	–	190	–	–	190	–	ns
	dV_{out}/dt	–	6.0	–	–	6.0	–	V/μs
Gain = 1000, 15% overshoot,	t_f	–	80	–	–	80	–	ns
	t_{pd}	–	100	–	–	100	–	ns
	dV_{out}/dt	–	14	–	–	14	–	V/μs
Gain = 100, no overshoot,	t_f	–	60	–	–	60	–	ns
	t_{pd}	–	100	–	–	100	–	ns
	dV_{out}/dt	–	34	–	–	34	–	V/μs
Gain = 10, 15% overshoot,	t_f	–	120	–	–	120	–	ns
	t_{pd}	–	80	–	–	80	–	ns
	dV_{out}/dt	–	6.25	–	–	6.25	–	V/μs
Gain = 1, 15% overshoot,	t_f	–	160	–	–	160	–	ns
	t_{pd}	–	80	–	–	80	–	ns
	dV_{out}/dt	–	4.2	–	–	4.2	–	V/μs
Output Impedance (f = 20 Hz)	Z_{out}	–	4.0	–	–	4.0	–	kΩ
Output Voltage Swing	V_{out}							V_{pk}
(R_L = 2.0 kΩ, f = 1.0 kHz)		–	–	–	±10	±13	–	
(R_L = 1.0 kΩ, f = 1.0 kHz)		±10	±13	–	–	–	–	
Positive Supply Sensitivity (V^- constant)	S^+	–	50	150	–	50	200	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	50	150	–	50	200	μV/V
Power Supply Current (V_o = 0)	I_D^+	–	3.0	5.0	–	3.0	6.7	mAdc
	I_D^-	–	3.0	5.0	–	3.0	6.7	
DC Quiescent Power Dissipation (V_o = 0)	P_D	–	90	150	–	90	200	mW

See current MC1539/1439 data sheet for additional information.

PACKAGING AND HANDLING

The MCC1539/MCC1439 operational amplifier is now available as a single monolithic die or encapsulated in the TO-99 and TO-116 hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1558
MCC1458

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER CHIP

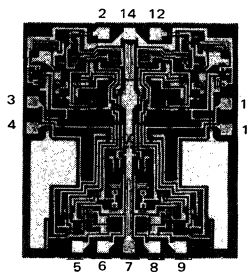
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1558 and MCC1458 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

(DUAL MC1741)

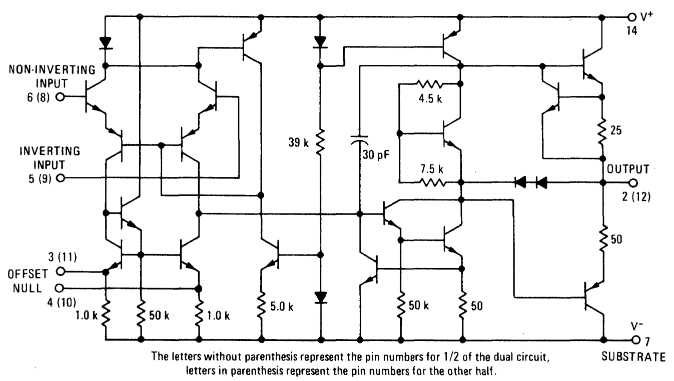
DUAL
OPERATIONAL AMPLIFIER CHIP
INTEGRATED CIRCUIT
MONOLITHIC SILICON



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

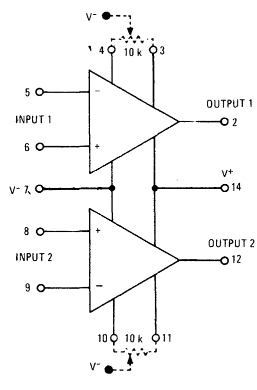
Rating		Symbol	MCC1558	MCC1458	Unit
Power Supply Voltage		V^+ V^-	+22 -22	+18 -18	Vdc
Differential Input Signal		V_{in}	±30		Volts
Common-Mode Input Swing		CMV_{in}	±15		Volts
Output Short Circuit Duration		t_S	Continuous		
Operating Temperature Range	MCC1558 MCC1458	T_A	-55 to +125 0 to +75		°C
Junction Temperature Range		T_J	-65 to +150		°C

FIGURE 1 – CIRCUIT SCHEMATIC



The letters without parenthesis represent the pin numbers for 1/2 of the dual circuit, letters in parenthesis represent the pin numbers for the other half.

FIGURE 2 – OFFSET ADJUST



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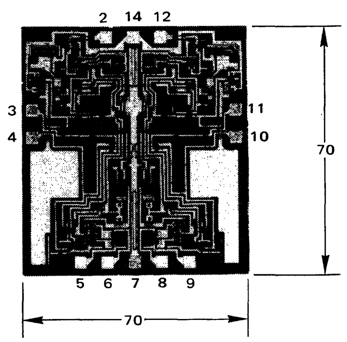
MCC1558, MCC1458 (continued)

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1558 Min	MCC1558 Typ	MCC1558 Max	MCC1458 Min	MCC1458 Typ	MCC1458 Max	Unit
Input Bias Current	I_b	–	0.2	0.5	–	0.2	0.5	μAdc
Input Offset Current	$\lvert I_{io} \rvert$	–	0.03	0.2	–	0.03	0.2	μAdc
Input Offset Voltage ($R_S \le$ 10 k ohms)	$\lvert V_{io} \rvert$	–	1.0	5.0	–	2.0	6.0	mVdc
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	–	1.0	–	–	1.0	–	Megohm
Parallel Input Capacitance	C_p	–	6.0	–	–	6.0	–	pF
Common-Mode Input Impedance (f = 20 Hz)	$Z_{(in)}$	–	200	–	–	200	–	Megohms
Common-Mode Input Voltage Swing	CMV_{in}	–	±13	–	–	±13	–	Vpk
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	–	90	–	–	90	–	dB
Open-Loop Voltage Gain (V_o = ±10 V, R_L = 2.0 k ohms)	A_{VOL}	50,000	200,000	–	20,000	100,000	–	V/V
Power Bandwidth (A_V = 1, R_L = 2.0 k ohms, THD ≤ 5%, V_o = 20 V_{p-p})	P_{BW}	–	14	–	–	14	–	kHz
Unity Gain Crossover Frequency (open-loop)		–	1.1	–	–	1.1	–	MHz
Phase Margin (open-loop, unity gain)		–	65	–	–	65	–	degrees
Gain Margin		–	11	–	–	11	–	dB
Slew Rate (Unity Gain)	dV_{out}/dt	–	0.8	–	–	0.8	–	V/μs
Output Impedance (f = 20 Hz)	Z_{out}	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{SC}	–	20	–	–	20	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_o	±12	±14	–	±12	±14	–	Vpk
Power Supply Sensitivity								μV/V
V^- = constant, $R_s \le$ 10 k ohms	S^+	–	30	150	–	30	150	
V^+ = constant, $R_s \le$ 10 k ohms	S^-	–	30	150	–	30	150	
Power Supply Current	I_D^+	–	2.3	5.0	–	2.3	5.6	mAdc
	I_D^-	–	2.3	5.0	–	2.3	5.6	
DC Quiescent Power Dissipation (V_o = 0)	P_D	–	70	150	–	70	170	mW

See current MC1558/MC1458 data sheet for additional information.

MCC1558/MCC1458 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

PACKAGING AND HANDLING

The MCC1558/MCC1458 dual operational amplifiers are now available as a single monolithic die or encapsulated in a variety of hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

NEGATIVE VOLTAGE REGULATORS

MCC1563
MCC1463

MONOLITHIC NEGATIVE VOLTAGE REGULATOR CHIP

The MCC1563/MCC1463 is a "three terminal" negative regulator designed to deliver continuous load current up to 500 mAdc and provide a maximum negative input voltage of -40 Vdc. Output current capability can be increased to greater than 10 Adc through use of one or more external transistors.

The MCC1563 and MCC1463 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Electronic "Shutdown" and Short-Circuit Protection
- Low Output Impedance – 20 Milliohms typ
- Excellent Temperature Stability – $TCV_O = \pm 0.002\%/^{\circ}C$ typ
- High Ripple Rejection – 0.002% typ
- 500 mA Current Capability

NEGATIVE-POWER SUPPLY VOLTAGE REGULATOR CHIP

MONOLITHIC SILICON INTEGRATED CIRCUIT

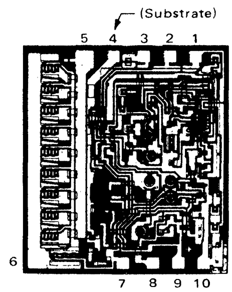
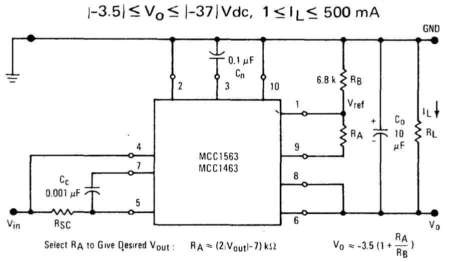


FIGURE 1 – TYPICAL CIRCUIT CONNECTION
$|-3.5| \le V_O \le |-37|$ Vdc, $1 \le I_L \le 500$ mA



Select R_A to Give Desired V_{out}: $R_A \approx (2|V_{out}| - 7)$ kΩ $\qquad V_O \approx -3.5\,(1 + \frac{R_A}{R_B})$

FIGURE 2 – TYPICAL NPN CURRENT BOOST CONNECTION
(V_O = -5.2 Vdc, I_L = 10 Adc [max])

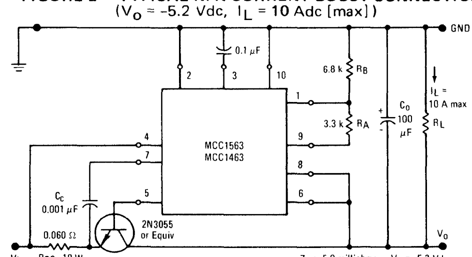
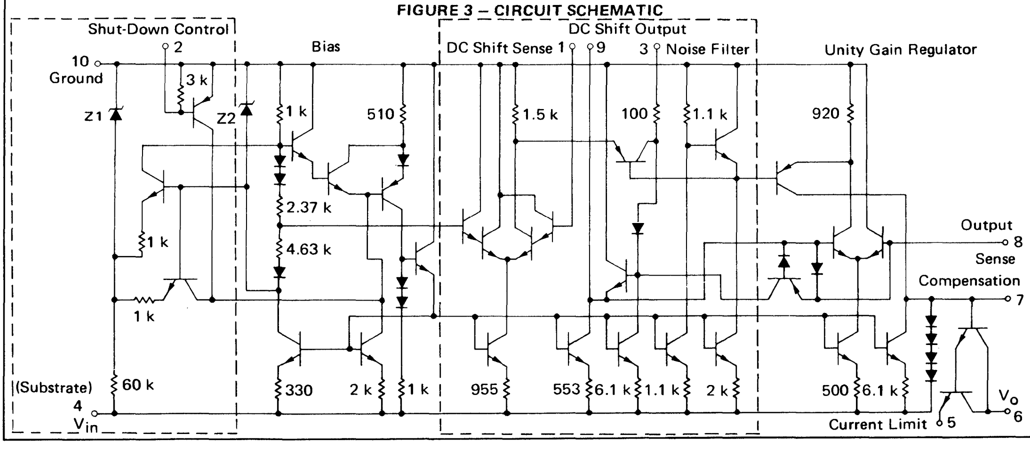


FIGURE 3 – CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

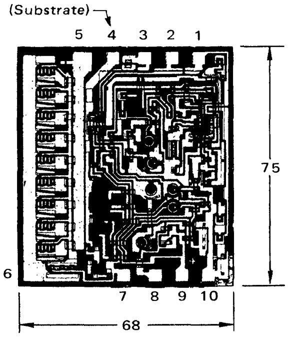
Rating		Symbol	MCC1563	MCC1463	Unit
Input Voltage		V_{in}	-40	-35	Vdc
Peak Load Current		I_L pk	600		mA
Current, Pin 2		$I_{pin\ 2}$	10		mA
Operating Temperature Range	MCC1563 MCC1463	T_A	-55 to +125 0 to +75		°C
Junction Temperature Range		T_J	-65 to +175		°C

ELECTRICAL CHARACTERISTICS (I_L = 100 mAdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1563			MCC1463			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage	V_{in}	–	–	-40	–	–	-35	Vdc
Output Voltage Range	V_O	-3.6	–	-37	-3.8	–	-32	Vdc
Reference Voltage (Pin 1 to Ground)	V_{ref}	-3.4	-3.5	-3.6	-3.2	-3.5	-3.8	Vdc
Minimum Input-Output Voltage Differential (R_{SC} = 0)	$\|V_{in} - V_O\|$	–	1.5	2.7	–	1.5	3.0	Vdc
Bias Current (I_L = 1.0 mAdc, $I_b = I_{in} - I_L$)	I_b	–	7.0	11	–	7.0	14	mAdc
Output Noise (C_n = 0.1 µF, f = 10 Hz to 5.0 MHz)	v_n	–	120	–	–	120	–	µV(rms)
Temperature Coefficient of Output Voltage	TCV_O	–	±0.002	–	–	±0.002	–	%/°C
Input Regulation	Reg_{in}	–	0.002	–	–	0.003	–	%/V_O
Load Regulation (T_J = Constant [1.0 mA ≤ I_L ≤ 20 mA])	Reg_L	–	0.4	–	–	0.7	–	mV
Output Impedance (f = 1.0 kHz)	Z_O	–	20	–	–	35	–	milliohms
Shutdown Current (V_{in} = -35 Vdc)	I_{sd}	–	7.0	15	–	14	50	µAdc

See current MC1563/1463 data sheet for additional information

MCC1563/MCC1463 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

PACKAGING AND HANDLING

The MCC1563/MCC1463 voltage regulator is now available as a single monolithic die or encapsulated in the Case 602A and Case 614 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

POSITIVE VOLTAGE REGULATORS

MCC1569
MCC1469

MONOLITHIC VOLTAGE REGULATOR CHIP

The MCC1569 and MCC1469 are positive voltage regulators designed to deliver continuous load current up to 500 mAdc. Output voltage is adjustable from 2.5 Vdc to 37 Vdc. Systems requiring both a positive and negative regulated voltage can use the MCC1569 and MCC1563 as complementary regulators with a common input ground.

The MCC1569 and MCC1469 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Electronic "Shut-Down" Control
- Excellent Load Regulation (Low Output Impedance – 20 milliohms typ)
- High Power Capability: Up to 17.5 Watts
- Excellent Temperature Stability: ±0.002%/°C typ
- High Ripple Rejection: 0.002%/V typ

POSITIVE VOLTAGE REGULATOR INTEGRATED CIRCUIT CHIP

MONOLITHIC SILICON EPITAXIAL PASSIVATED

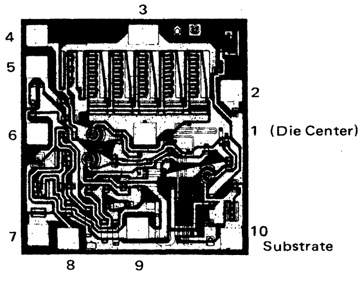
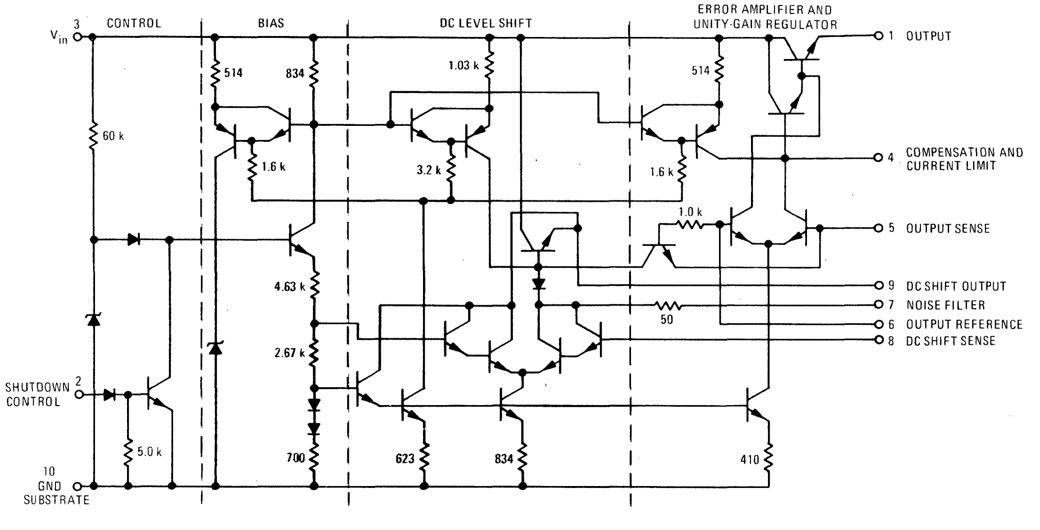


FIGURE 1 – CIRCUIT SCHEMATIC



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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

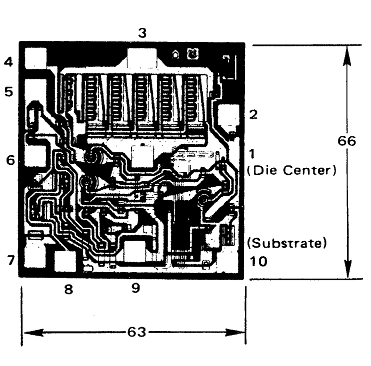
Rating		Symbol	MCC1569	MCC1469	Unit
Input Voltage		V_{in}	40	35	Vdc
Peak Load Current		I_{pk}	600		mA
Current, Pin 2		$I_{pin\ 2}$	10		mA
Current, Pin 9		$I_{pin\ 9}$	5.0		
Operating Temperature Range	MCC1569 MCC1469	T_A	-55 to +125 0 to +75		°C
Junction Temperature Range		T_J	-65 to +150		°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1569 Min	MCC1569 Typ	MCC1569 Max	MCC1469 Min	MCC1469 Typ	MCC1469 Max	Unit
Input Voltage	V_{in}	–	–	40	–	–	35	Vdc
Output Voltage Range	V_O	2.5	–	37	2.5	–	32	Vdc
Reference Voltage (Pin 8 to Ground)	V_{ref}	3.4	3.5	3.6	3.2	3.5	3.8	Vdc
Minimum Input-Output Voltage Differential	$V_{in} - V_O$	–	2.1	2.7	–	2.1	3.0	Vdc
Bias Current (I_L = 1.0 mAdc, R_2 = 6.8 k ohms, $I_b = I_{in} - I_L$)	I_b	–	4.0	9.0	–	5.0	12	mAdc
Output Noise (C_n = 0.1 μF, f = 10 Hz to 5.0 MHz)	v_n	–	0.150	–	–	0.150	–	mV(rms)
Temperature Coefficient of Output Voltage	TCV_O	–	±0.002	–	–	±0.002	–	%/°C
Input Regulation	Reg_{in}	–	0.002	–	–	0.003	–	%/V_{in}
Output Impedance (C_c = 0.001 μF, R_{SC} = 1.0 ohm, f = 1.0 kHz, V_{in} = +14 Vdc, V_O = +10 Vdc)	Z_{out}	–	20	–	–	35	–	milliohms
Shutdown Current (V_{in} = +35 Vdc)	I_{sd}	–	70	150	–	140	500	μAdc

See current MC1569/1469 data sheet for additional information.

MCC1569/MCC1469 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

PACKAGING AND HANDLING

The MCC1569/MCC1469 voltage regulator is now available as a single monolithic die or encapsulated in the Case 602A and Case 614 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

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MCC1595
MCC1495

MONOLITHIC FOUR-QUADRANT MULTIPLIER CHIP

. . . designed for uses where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

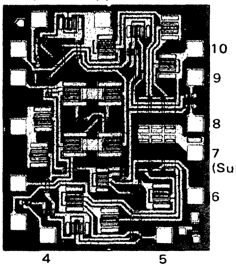
The MCC1595 and MCC1495 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

*When used with an operational amplifier.

- Excellent Linearity – 0.5% typ Error on X-Input, 1% typ Error on Y-Input – MCC1595
- Excellent Linearity – 1% typ Error on X-Input, 2% typ Error on Y-Input – MCC1495
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT CHIP

MONOLITHIC SILICON EPITAXIAL PASSIVATED

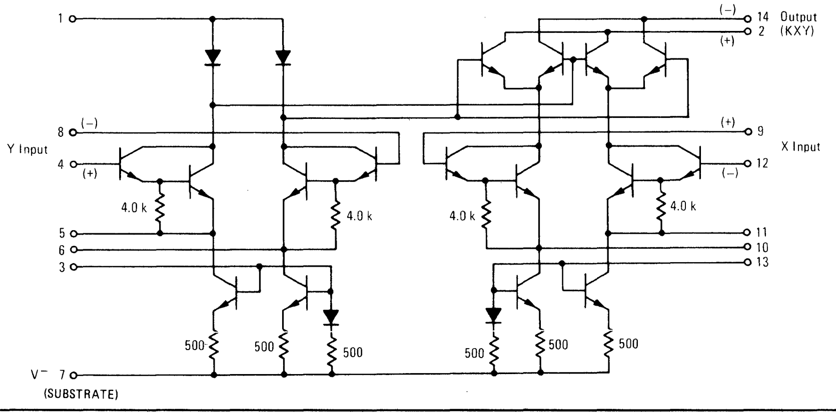


MCC1595/MCC1495 Die

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2-V_1, $V_{14}-V_1$, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, $V_{12}-V_7$, V_9-V_7, V_8-V_7, V_4-V_7)	ΔV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+I_{13}R_X)$ $\pm(6+I_3R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Operating Temperature Range MCC1595 MCC1495	T_A	–55 to +125 0 to +70	°C
Junction Temperature Range	T_J	-65 to +150	°C

CIRCUIT SCHEMATIC

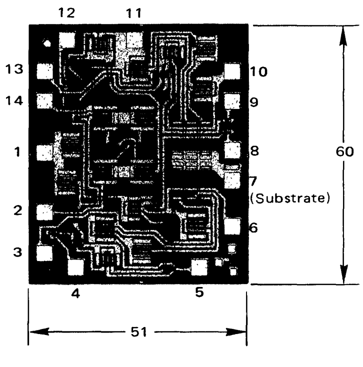


ELECTRICAL CHARACTERISTICS (V^+ = +32 V, V^- = -15 V, T_A = 25°C, $I_3 = I_{13}$ = 1 mA, $R_X = R_Y$ = 15 kΩ, R_L = 11 kΩ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Linearity: Output Error in Percent of Full Scale:						%
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)	MCC1495	E_{RX}	–	1.0	–	
	MCC1595		–	0.5	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)	MCC1495	E_{RY}	–	2.0	–	
	MCC1595		–	1.0	–	
Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment		E_{SQ}				%
	MCC1495		–	0.75	–	
	MCC1595		–	0.5	–	
Scale Factor (Adjustable) $\left(K = \frac{2R_L}{I_3 R_X R_Y}\right)$		K	–	0.1	–	–
Input Resistance (f = 20 Hz)	MCC1495	R_{INX}	–	20	–	Megohms
	MCC1595		–	35	–	
	MCC1495	R_{INY}	–	20	–	
	MCC1595		–	35	–	
Differential Output Resistance (f = 20 Hz)		R_O	–	300	–	k Ohms
Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	MCC1495	I_{bx}	–	2.0	12	μA
	MCC1595		–	2.0	8.0	
	MCC1495	I_{by}	–	2.0	12	
	MCC1595		–	2.0	8.0	
Input Offset Current $\lvert I_9 - I_{12} \rvert$	MCC1495	$\lvert I_{iox} \rvert$	–	0.4	2.0	μA
	MCC1595		–	0.2	1.0	
$\lvert I_4 - I_8 \rvert$	MCC1495	$\lvert I_{ioy} \rvert$	–	0.4	2.0	
	MCC1595		–	0.2	1.0	
Output Offset Current $\lvert I_{14} - I_2 \rvert$		$\lvert I_{oo} \rvert$				μA
	MCC1495		–	20	100	
	MCC1595		–	10	50	
Frequency Response						
3.0 dB Bandwidth		BW_{3dB}	–	3.0	–	MHz
3° Relative Phase Shift Between V_X and V_Y		f_ϕ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift		f_θ	–	30	–	kHz
Common Mode Input Swing (Either input)		CMV				Vdc
	MCC1495		–	±12	–	
	MCC1595		–	±13	–	
Common Mode Quiescent Output Voltage		V_{o1}	–	21	–	Vdc
		V_{o2}	–	21	–	
Differential Output Voltage Swing Capability		V_{out}	–	±14	–	V_{peak}
Power Supply Sensitivity		S^+	–	5.0	–	mV/V
		S^-	–	10	–	
Power Supply Current		I_7	–	6.0	7.0	mA
DC Power Dissipation		P_D	–	135	170	mW

See current MC1595/1495 data sheet for additional information.

MCC1595/MCC1495 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

PACKAGING AND HANDLING

The MCC1595/MCC1495 is the Four-Quadrant Multiplier now available in die (chip) form. The phosphorsilicate passivation protects the metalization and active area of the die but care must be excercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

8

OPERATIONAL AMPLIFIERS

MCC1709
MCC1709C

MONOLITHIC OPERATIONAL AMPLIFIER CHIP

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1709 and MCC1709C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

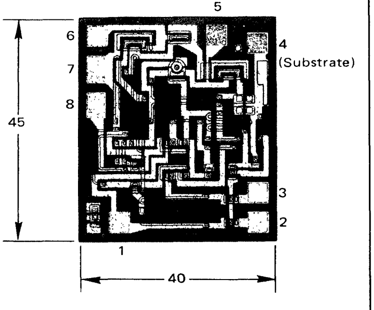
- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift – ±3.0 μV/°C
- Large Output Voltage Swing – ±14 V typical @ ±15 V Supply
- Low Output Impedance – Z_{out} = 150 ohms typical

OPERATIONAL AMPLIFIER CHIP
INTEGRATED CIRCUIT
MONOLITHIC SILICON

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Power Supply Voltage		V^+ V^-	+18 -18	Vdc
Differential Input Signal		V_{in}	±5.0	Volts
Common Mode Input Swing		CMV_{in}	$\pm V^+$	Volts
Load Current		I_L	10	mA
Output Short Circuit Duration		t_S	5.0	s
Operating Temperature Range	MCC1709 MCC1709C	T_A	-55 to +125 0 to +75	°C
Junction Temperature Range		T_J	-55 to +150	°C

OUTLINE DIMENSIONS and BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

FIGURE 1 – CIRCUIT SCHEMATIC

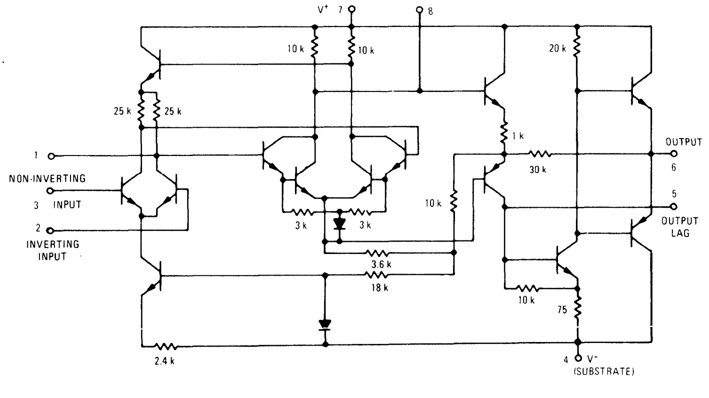
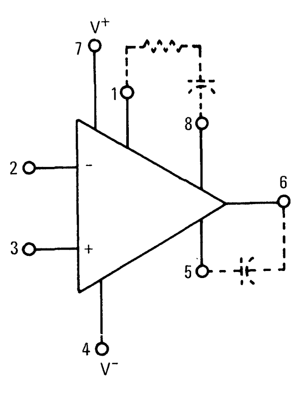


FIGURE 2 – EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1709 Min	MCC1709 Typ	MCC1709 Max	MCC1709C Min	MCC1709C Typ	MCC1709C Max	Unit
Open Loop Voltage Gain (V_O = ±10 V)	A_{VOL}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	Z_{out}	–	150	–	–	150	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	–	400	–	–	250	–	kΩ
Output Voltage Swing (R_L = 10 kΩ)	V_O	±12	±14	–	±12	±14	–	V_{peak}
(R_L = 2.0 kΩ)		±10	±13	–	±10	±13	–	
Input Common-Mode Voltage Swing	CMV_{in}	–	±10	–	–	±10	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	–	90	–	–	90	–	dB
Input Bias Current	I_b	–	0.2	0.5	–	0.3	1.5	μA
Input Offset Current	$\|I_{io}\|$	–	0.05	0.2	–	0.1	0.5	μA
Input Offset Voltage	$\|V_{io}\|$	–	1.0	5.0	–	2.0	7.5	mV
Step Response								
Gain = 100, 5.0% overshoot	t_f	–	0.8	–	–	0.8	–	μs
	t_{pd}	–	0.38	–	–	0.38	–	μs
	dV_{out}/dt	–	12	–	–	12	–	V/μs
Gain = 10, 10% overshoot	t_f	–	0.6	–	–	0.6	–	μs
	t_{pd}	–	0.34	–	–	0.34	–	μs
	dV_{out}/dt	–	1.7	–	–	1.7	–	V/μs
Gain = 1, 5.0% overshoot	t_f	–	2.2	–	–	2.2	–	μs
	t_{pd}	–	1.3	–	–	1.3	–	μs
	dV_{out}/dt	–	0.25	–	–	0.25	–	V/μs
Power Supply Current	I_D^+	–	2.7	5.5	–	2.7	6.7	mAdc
	I_D^-	–	2.7	5.5	–	2.7	6.7	
DC Quiescent Power Dissipation (Power Supply = ±15 V, V_O = 0)	P_D	–	80	165	–	80	200	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	25	150	–	25	200	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	25	150	–	25	200	μV/V

See current MC1709/1709C data sheet for additional information

PACKAGING AND HANDLING

The MCC1709/MCC1709C operational amplifier is now available as a single monolithic die or encapsulated in a variety of hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1710
MCC1710C

DIFFERENTIAL COMPARATORS

MONOLITHIC DIFFERENTIAL VOLTAGE COMPARATOR CHIP

. . . designed for use in level detection, low-level sensing, and memory applications.

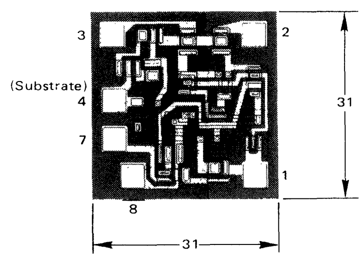
The MCC1710 and MCC1710C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Differential Input Characteristics –
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 3.0 μV/^{o}C
- Fast Response Time – 40 ns
- Output Compatible With All Saturating Logic Forms –
  V_{out} = +3.2 V to -0.5 V typical
- Low Output Impedance – 200 ohms

DIFFERENTIAL COMPARATOR CHIP INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED

OUTLINE DIMENSIONS and BONDING DIAGRAM

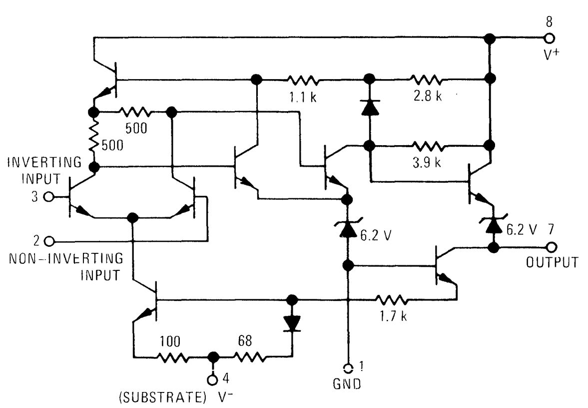


All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

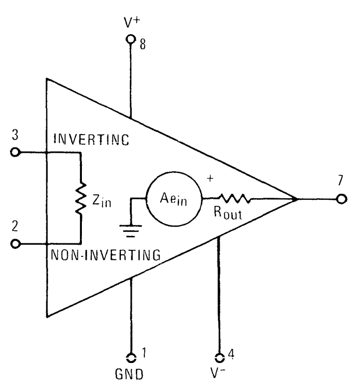
MAXIMUM RATINGS (T_A = 25^{o}C unless otherwise noted)

Rating		Symbol	Value	Unit
Power Supply Voltage		V^+ V^-	+14 -7.0	Vdc
Differential Input Signal		V_{in}	±5.0	Volts
Common Mode Input Swing		CMV_{in}	±7.0	Volts
Peak Load Current		I_L	10	mA
Operating Temperature Range	MCC1710 MCC1710C	T_A	-55 to +125 0 to +75	^{o}C
Junction Temperature Range		T_J	-65 to +150	^{o}C

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



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ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc, V^- = -6.0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MCC1710 Min	MCC1710 Typ	MCC1710 Max	MCC1710C Min	MCC1710C Typ	MCC1710C Max	Unit
Input Offset Voltage (V_O = 1.4 Vdc)	V_{io}	–	1.0	2.0	–	1.5	5.0	mVdc
Input Bias Current (V_O = 1.4 Vdc)	I_b	–	12	20	–	15	25	μAdc
Output Resistance	R_{out}	–	200	–	–	200	–	Ohms
Positive Output Voltage ($V_{in} \geq$ 5.0 mV, $0 \leq I_O \leq$ 5.0 mA)	V_{OH}	2.5	3.2	4.0	2.5	3.2	4.0	Vdc
Negative Output Voltage ($V_{in} \geqq$ -5.0 mV)	V_{OL}	-1.0	-0.5	0	-1.0	-0.5	0	Vdc
Output Sink Current ($V_{in} \geq$ -5.0 mV, $V_{out} \geq$ 0)	I_s	2.0	2.5	–	2.0	2.5	–	mAdc
Common Mode Rejection Ratio (V^- = -7.0 Vdc, $R_S \leq$ 200 Ω)	CM_{rej}	–	100	–	–	100	–	dB
Propagation Delay Time For Positive and Negative Going Input Pulse	t_{pd}	–	40	–	–	40	–	ns
Power Supply Current ($V_{out} \leqq$ 0 Vdc)	I_D^+	–	6.4	9.0	–	6.4	9.0	mAdc
	I_D^-	–	5.5	7.0	–	5.5	7.0	
DC Quiescent Power Dissipation	P_D	–	115	150	–	110	150	mW

See current MC1710/1710C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1710/MCC1710C differential comparator is now available as a single monolithic die or encapsulated in the TO-91, TO-99, and TO-116 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

DIFFERENTIAL COMPARATORS

MCC1711
MCC1711C

MONOLITHIC DUAL DIFFERENTIAL VOLTAGE COMPARATOR CHIP

. . . designed for use in level detection, low-level sensing, and memory applications.

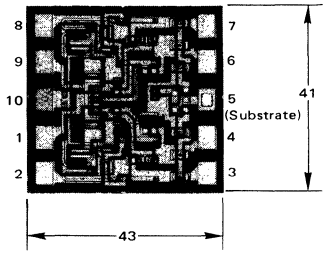
The MCC1711 and MCC1711C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Differential Input –
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 5.0 μV/^{o}C
- Fast Response Time – 40 ns
- Output Compatible with All Saturating Logic Forms –
  V_{out} = +4.5 V to -0.5 V Typical
- Low Output Impedance – 200 Ohms

DUAL DIFFERENTIAL COMPARATOR CHIP INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

OUTLINE DIMENSIONS and BONDING DIAGRAM

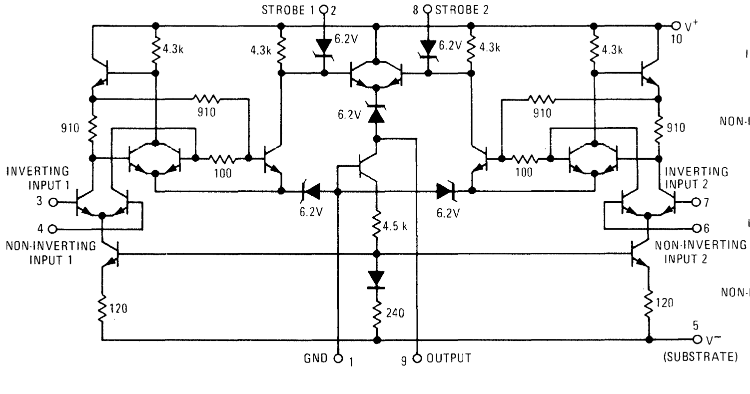


All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

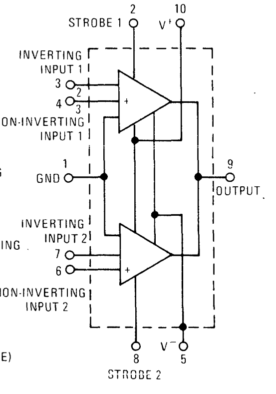
MAXIMUM RATINGS (T_A = 25^{o}C unless otherwise noted)

Rating		Symbol	Value	Unit
Power Supply Voltage		V^+ V^-	+14 -7.0	Vdc Vdc
Differential Input Signal		V_{in}	±5.0	Volts
Common Mode Input Swing		CMV_{in}	±7.0	Volts
Peak Load Current		I_L	50	mA
Operating Temperature Range	MCC1711 MCC1711C	T_A	-55 to +125 0 to +75	^{o}C
Junction Temperature Range		T_J	-65 to +150	^{o}C

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (each comparator) (V^+ = +12 Vdc, V^- = -6.0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MCC1711			MCC1711C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_O = 1.4 Vdc)	V_{io}	–	1.0	3.5	–	1.0	5.0	mVdc
Input Bias Current (V_O = 1.4 Vdc)	I_b	–	25	75	–	25	100	μAdc
Output Resistance	R_{out}	–	200	–	–	200	–	Ohms
Positive Output Voltage ($V_{in} \geqq 10$ mVdc, $0 \leqq I_O \leqq 5.0$ mA)	V_{OH}	2.5	3.2	5.0	2.5	3.2	5.0	Vdc
Negative Output Voltage ($V_{in} \geqq -10$ mVdc)	V_{OL}	-1.0	-0.5	0	-1.0	-0.5	0	Vdc
Strobed Output Level ($V_{strobe} \leqq 0.3$ Vdc)	$V_{OL(st)}$	-1.0	–	0	-1.0	–	0	Vdc
Output Sink Current ($V_{in} \geqq -10$ mV, $V_O \geqq 0$)	I_S	0.5	0.8	–	0.5	0.8	–	mAdc
Strobe Current (V_{strobe} = 100 mVdc)	I_{st}	–	1.2	2.5	–	1.2	2.5	mAdc
Response Time (V_b = 5.0 mV + V_{io})	t_R	–	40	–	–	40	–	ns
Strobe Release Time	t_{SR}	–	12	–	–	12	–	ns
Power Supply Current ($V_O \leqq 0$ Vdc)	I_D^+	–	8.6	–	–	8.6	–	mAdc
	I_D^-	–	3.9	–	–	3.9	–	
Power Consumption		–	130	200	–	130	200	mW

See current MC1711/1711C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1711/MCC1711C dual differential comparator is now available as a single monolithic die or encapsulated in the TO-91, TO-100, and TO-116 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1723
MCC1723C

MONOLITHIC VOLTAGE REGULATOR CHIP

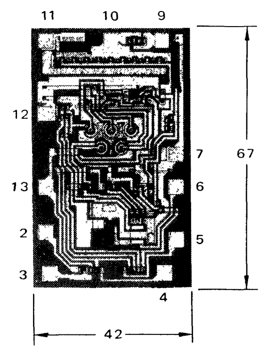
The MCC1723/MCC1723C is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors.

The MCC1723 and MCC1723C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line Regulation
- Adjustable Short-Circuit Protection

VOLTAGE REGULATOR CHIP

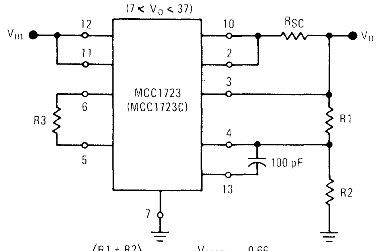
MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

FIGURE 1 – TYPICAL CIRCUIT CONNECTION

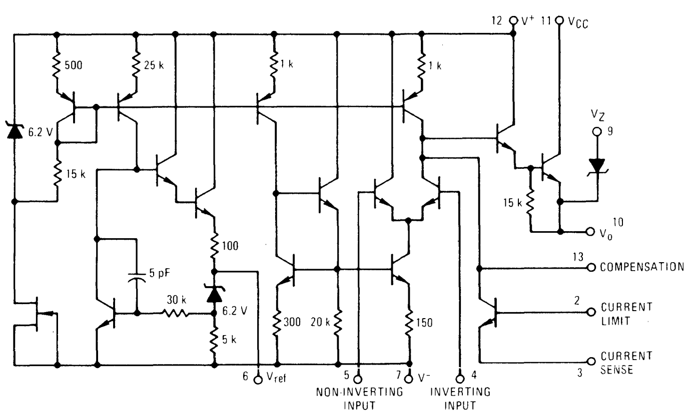
$(7 < V_O < 37)$



$V_O \approx 7\left(\frac{R1 + R2}{R2}\right)$ $I_{SC} \approx \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at $T_J = 25^{\circ}C$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1||R2

FIGURE 2 – CIRCUIT SCHEMATIC



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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Pulse Voltage from V^+ to V^- (50 ms)	MCC1723	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V^+ to V^-		V_{in}	40	Vdc
Input-Output Voltage Differential		$V_{in}-V_O$	40	Vdc
Maximum Output Current		I_L	150	mAdc
Current from V_{ref}		I_{ref}	15	mAdc
Operating Temperature Range	MCC1723 MCC1723C	T_A	-55 to +125 0 to +75	°C
Junction Temperature Range		T_J	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} = 12 Vdc, V_O = 5 Vdc, I_L = 1 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 1)

Characteristic	Symbol	MCC1723			MCC1723C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	9.5	–	40	9.5	–	40	Vdc
Output Voltage Range	V_O	2.0	–	37	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_O$	3.0	–	38	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{sb}	–	2.3	3.5	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_n							μV(rms)
C_{ref} = 0		–	20	–	–	20	–	
C_{ref} = 5.0 μF		–	2.5	–	–	2.5	–	
Line Regulation	Reg_{in}							% V_O
(12 V < V_{in} < 15 V)		–	0.01	0.1	–	0.01	0.1	
(12 V < V_{in} < 40 V)		–	0.02	0.2	–	0.1	0.5	
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_{load}	–	0.03	0.15	–	0.03	0.2	% V_O
Ripple Rejection (f = 50 Hz to 10 kHz)	Rej_R							dB
C_{ref} = 0		–	74	–	–	74	–	
C_{ref} = 5.0 μF		–	86	–	–	86	–	
Short Circuit Current Limit (R_{SC} = 10 Ω, V_O = 0)	I_{SC}	–	65	–	–	65	–	mAdc

See current MC1723/1723C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1723/MCC1723C voltage regulator is now available as a single monolithic die or encapsulated in the Motorola Case 603-03 hermetic package. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1741
MCC1741C

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER CHIP

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

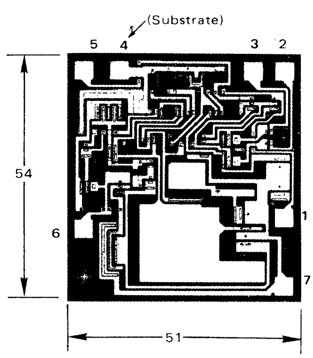
The MCC1741 and MCC1741C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER CHIP

MONOLITHIC SILICON
INTEGRATED CIRCUIT

OUTLINE DIMENSIONS and BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
		MCC1741C	MCC1741	
Power Supply Voltage	V^+ V^-	+18 -18	+22 -22	Vdc Vdc
Differential Input Signal	V_{in}	±30		Volts
Common Mode Input Swing (Note 1)	CMV_{in}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Temperature Range MCC1741 MCC1741C	T_A	-55 to +125 0 to +75		°C
Junction Temperature Range	T_J	-65 to +150		°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

FIGURE 1 – CIRCUIT SCHEMATIC

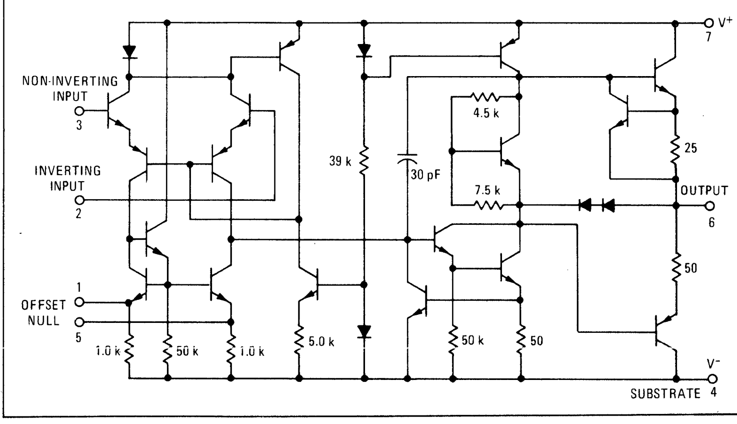
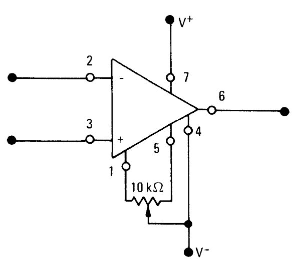


FIGURE 2 – OFFSET ADJUST CIRCUIT



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ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = 15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1741 Min	MCC1741 Typ	MCC1741 Max	MCC1741C Min	MCC1741C Typ	MCC1741C Max	Unit
Open Loop Voltage Gain (R_L = 2.0 kΩ) (V_O = ± 10 V)	A_{VOL}	50,000	200,000	–	20,000	100,000	–	–
Output Impedance (f = 20 Hz)	Z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	–	1.0	–	–	1.0	–	Meg Ω
Output Voltage Swing (R_L = 10 kΩ)	V_O	±12	±14	–	±12	±14	–	V_{peak}
(R_L = 2.0 kΩ)		±10	±13	–	±10	±13	–	
Input Common-Mode Voltage Swing	CMV_{in}	–	±13	–	–	±13	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	–	90	–	–	90	–	dB
Input Bias Current	I_b	–	0.2	0.5	–	0.2	0.5	µA
Input Offset Current	$\|I_{io}\|$	–	0.03	0.2	–	0.03	0.2	µA
Input Offset Voltage (R_S = ≦ 10 kΩ)	$\|V_{io}\|$	–	1.0	5.0	–	2.0	6.0	mV
Step Response Gain = 100	t_f	–	29	–	–	29	–	µs
	t_{pd}	–	8.5	–	–	8.5	–	µs
	dV_{out}/dt ①	–	1.0	–	–	1.0	–	V/µs
Gain = 10	t_f	–	3.0	–	–	3.0	–	µs
	t_{pd}	–	1.0	–	–	1.0	–	µs
	dV_{out}/dt ①	–	1.0	–	–	1.0	–	V/µs
Gain = 1	t_f	–	0.6	–	–	0.6	–	µs
	t_{pd}	–	0.38	–	–	0.38	–	µs
	dV_{out}/dt ①	–	0.8	–	–	0.8	–	V/µs
Power Supply Current	I_D^+	–	1.67	2.83	–	1.67	2.83	mA
	I_D^-	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation (Power Supply = ± 15 V, V_O = 0)	P_D	–	50	85	–	50	85	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	30	150	–	30	150	µV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	30	150	–	30	150	µV/V

PACKAGING AND HANDLING

The MCC1741/MCC1741C operational amplifier is now available as a single monolithic die or encapsulated in a variety of hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

OPERATIONAL AMPLIFIERS

MCC1748
MCC1748C

HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER CHIP

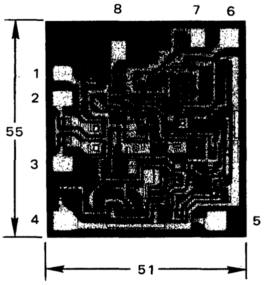
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1748 and MCC1748C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Noncompensated MC1741G
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER CHIP INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

FIGURE 1 – CIRCUIT SCHEMATIC

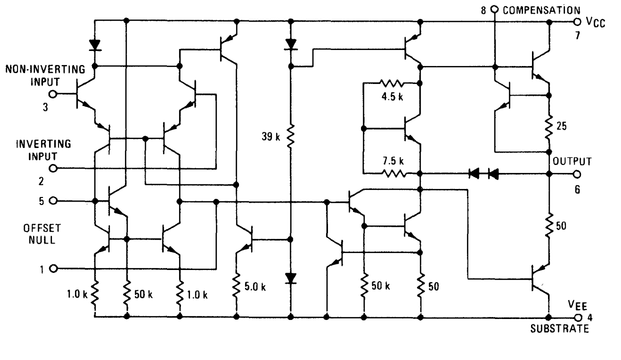
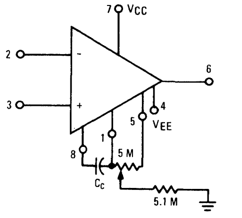


FIGURE 2 – OFFSET ADJUST AND FREQUENCY COMPENSATION



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	MCC1748	MCC1748C	Unit
Power Supply Voltage		V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Signal Voltage		V_{in}	±30		Volts
Common-Mode Input Swing Voltage (1)		V_{ICR}	±15		Volts
Output Short-Circuit Duration		t_S	Continuous		–
Operating Temperature Range	MCC1748 MCC1748C	T_A	-55 to +125 0 to +75		°C
Junction Temperature Range		T_J	-65 to +150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristics	Symbol	MCC1748			MCC1748C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_{IB}	–	0.08	0.5	–	0.08	0.5	µAdc
Input Offset Current	$\|I_{IO}\|$	–	0.02	0.2	–	0.02	0.2	µAdc
Input Offset Voltage ($R_S \leq 10$ k Ω)	$\|V_{IO}\|$	–	1.0	5.0	–	1.0	6.0	mVdc
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	–	2.0	–	–	2.0	–	Megohm
Parallel Input Capacitance	C_p	–	1.4	–	–	1.4	–	pF
Common-Mode Input Impedance (f = 20 Hz)	$z_{(in)}$	–	200	–	–	200		Megohms
Common-Mode Input Voltage Swing	V_{ICR}	–	±13	–	–	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	–	90	–	–	90	–	dB
Open-Loop Voltage Gain (V_O = ±10 V, R_L = 2.0 k ohms)	A_{vol}	50,000	200,000	–	20,000	200,000	–	V/V
Step Response (V_{in} = 20 mV, C_c = 30 pF, R_L = 2 kΩ, C_L = 100 pF)								
Rise Time	t_{PLH}	–	0.3	–	–	0.3	–	µs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate	dV_O/dt	–	0.8	–	–	0.8	–	V/µs
Output Impedance (f = 20 Hz)	z_O	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{SO}	–	25	–	–	25	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±12	±14	–	±12	±14	–	V_{pk}
R_L = 2 k ohms (T_A = T_{low} to T_{high})		±10	±13	–	±10	±13	–	
Power Supply Sensitivity								µV/V
V_{EE} = constant, $R_s \leq$ 10 k ohms	S+	–	30	150	–	30	150	
V_{CC} = constant, $R_s \leq$ 10 k ohms	S-	–	30	150	–	30	150	
Power Supply Current	I_D^+	–	1.67	2.83	–	1.67	2.83	mAdc
	I_D^-	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation (V_O = 0)	P_D	–	50	85	–	50	85	mW

(1) For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.
See current MC1748/1748C data sheet for additional information.

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PACKAGING AND HANDLING

The MCC1748/MCC1748C operational amplifier is now available as a single monolithic die or encapsulated in the TO-99 hermetic package. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

8

OPERATIONAL AMPLIFIERS

MCCF1558
MCCF1458

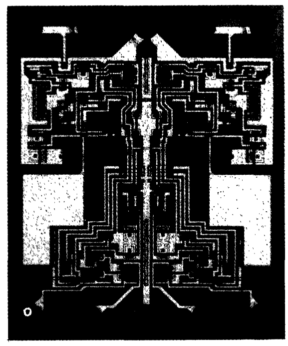
DUAL MC1741
INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER FLIP-CHIP

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCCF1558 and MCCF1458 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. The bumps are 90-10 solder on a chrome-copper-gold base. The interconnecting metalization is evaporated aluminum.

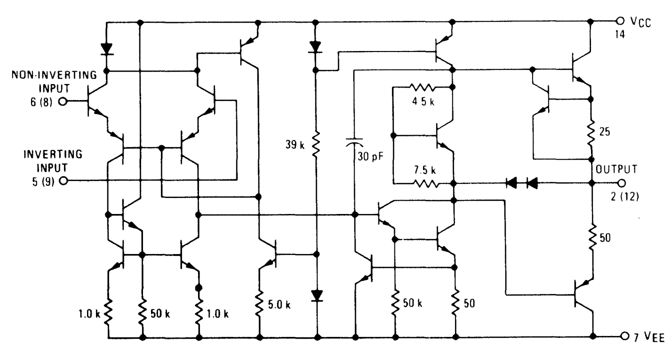
- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

(DUAL MC1741)
DUAL
OPERATIONAL AMPLIFIER
MONOLITHIC SILICON INTEGRATED CIRCUIT

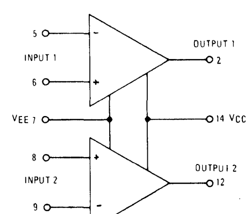


MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MCCF1558	MCCF1458	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{ID}	±30		Volts
Common-Mode Input Swing	V_{IC}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Temperature Range MCCF1558	T_A	-55 to +125		°C
MCCF1458		0 to +75		
Junction Temperature Range	T_J	-65 to +150		°C



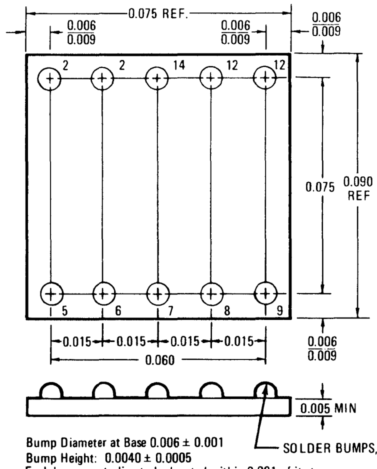
The letters without parenthesis represent the pin numbers for 1/2 of the dual circuit, letters in parenthesis represent the pin numbers for the other half.



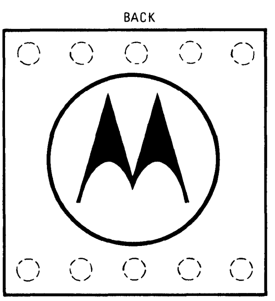
ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MCCF1558			MCCF1458			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_{IB}	–	0.2	0.5	–	0.2	0.5	μAdc
Input Offset Current	$\|I_{IO}\|$	–	0.03	0.2	–	0.03	0.2	μAdc
Input Offset Voltage ($R_S \leq$ 10 k ohms)	$\|V_{IO}\|$	–	1.0	5.0	–	2.0	6.0	mVdc
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	–	1.0	–	–	1.0	–	Megohm
Parallel Input Capacitance	C_p	–	6.0	–	–	6.0	–	pF
Common-Mode Input Impedance (f = 20 Hz)	z_{in}	–	200	–	–	200	–	Megohms
Common-Mode Input Voltage Swing	V_{IC}	–	±13	–	–	±13	–	Vpk
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	–	90	–	–	90	–	dB
Open-Loop Voltage Gain (V_O = ±10 V, R_L = 2.0 k ohms)	A_{vol}	50,000	200,000	–	20,000	100,000	–	V/V
Power Bandwidth (A_v = 1, R_L = 2.0 k ohms, THD ≤ 5%, v_O = 20 Vp-p)	P_{BW}	–	14	–	–	14	–	kHz
Unity Gain Crossover Frequency (open-loop)		–	1.1	–	–	1.1	–	MHz
Phase Margin (open-loop, unity gain)		–	65	–	–	65	–	degrees
Gain Margin		–	11	–	–	11	–	dB
Slew Rate (Unity Gain)	dV_O/dt	–	0.8	–	–	0.8	–	V/μs
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_S	–	20	–	–	20	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±12	±14	–	±12	±14	–	Vpk
Power Supply Sensitivity								μV/V
V_{EE} = constant, $R_s \leq$ 10 k ohms	S^+	–	30	150	–	30	150	
V_{CC} = constant, $R_s \leq$ 10 k ohms	S^-	–	30	150	–	30	150	
Power Supply Current	I_{DCC}	–	2.3	5.0	–	2.3	5.6	mAdc
	I_{DEE}	–	2.3	5.0	–	2.3	5.6	
DC Quiescent Power Dissipation (V_O = 0)	P_D	–	70	150	–	70	170	mW

See current MC1558/MC1458 data sheet for additional information.



Bump Diameter at Base 0.006 ± 0.001
Bump Height: 0.0040 ± 0.0005
Each bump centerline to be located within 0.001 of its true position with respect to any other bump centerline.



EACH CHIP IS MARKED WITH A MOTOROLA EMSIGNIA, THE TOP POINTING TO THE SIDE WHERE PAD 1 IS LOCATED

The popular 1558 type dual operational amplifier is now available in three chip forms: 1) conventional chips, 2) beam-lead chips and 3) flip-chips, as well as in a variety of plastic and hermetic packages. The flip-chip consists of a silicon chip with solder bumps on the geometry surface to provide easy mechanical mounting and electrical connection. These devices are protected by a thin layer of phosphorsilicate passivation which covers the interconnect metalization and active areas of the die.

Care must be exercised when removing the dice from the shipping carrier to avoid scratching the solder bumps. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCCF1709
MCCF1709C

OPERATIONAL AMPLIFIERS

MONOLITHIC OPERATIONAL AMPLIFIER FLIP-CHIP

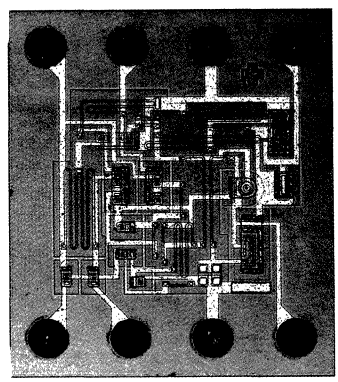
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCCF1709 and MCCF1709C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. The bumps are 90-10 solder on a chrome-copper-gold base. The interconnecting metalization is evaporated aluminum.

- High-Performance Open Loop Gain Characteristics
  A_{vol} = 45,000 typical
- Low Temperature Drift – ±3.0 μV/°C
- Large Output Voltage Swing – ±14 V typical @ ±15 V Supply
- Low Output Impedance – z_o = 150 ohms typical

OPERATIONAL AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC} V_{EE}	+18 -18	Vdc
Differential Input Signal		V_{ID}	±5.0	Volts
Common Mode Input Swing		V_{IC}	$\pm V_S$	Volts
Load Current		I_L	10	mA
Output Short Circuit Duration		t_S	5.0	s
Operating Temperature Range	MCCF1709 MCCF1709C	T_A	-55 to +125 0 to +75	°C
Junction Temperature Range		T_J	-55 to +150	°C

FIGURE 1 – CIRCUIT SCHEMATIC

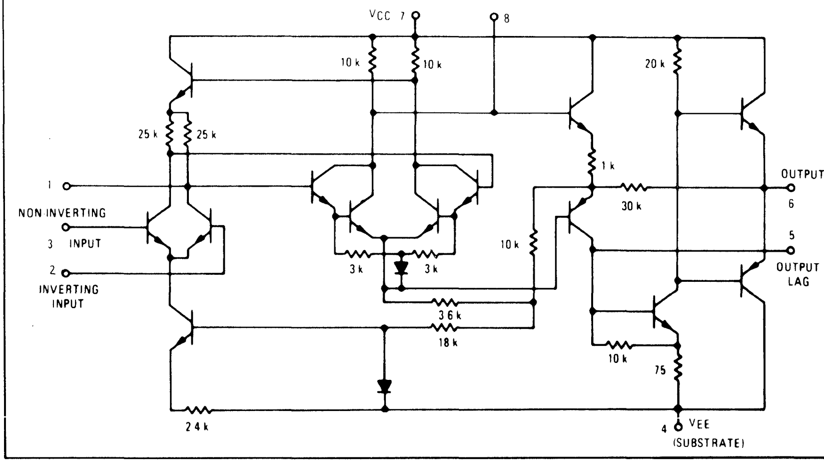
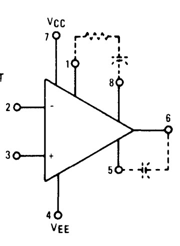


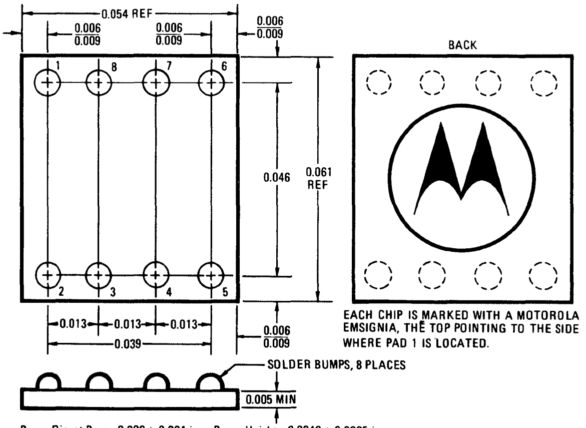
FIGURE 2 – EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MCCF1709 Min	MCCF1709 Typ	MCCF1709 Max	MCCF1709C Min	MCCF1709C Typ	MCCF1709C Max	Unit
Open Loop Voltage Gain (V_O = ±10V)	A_{vol}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	150	–	–	150	–	Ω
Input Impedance (f = 20 Hz)	z_{in}	–	400	–	–	250	–	kΩ
Output Voltage Swing	V_O							V_{peak}
(R_L = 10 kΩ)		±12	±14	–	±12	±14	–	
(R_L = 2.0 kΩ)		±10	±13	–	±10	±13	–	
Input Common-Mode Voltage Swing	V_{IC}	–	±10	–	–	±10	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	–	90	–	–	90	–	dB
Input Bias Current	I_{IB}	–	0.2	0.5	–	0.3	1.5	μA
Input Offset Current	$\|I_{IO}\|$	–	0.05	0.2	–	0.1	0.5	μA
Input Offset Voltage	$\|V_{IO}\|$	–	1.0	5.0	–	2.0	7.5	mV
Step Response								
Gain = 100, 5.0% overshoot	t_{THL}	–	0.8	–	–	0.8	–	μs
	t_d	–	0.38	–	–	0.38	–	μs
	dV_O/dt	–	12	–	–	12	–	V/μs
Gain = 10, 10% overshoot	t_{THL}	–	0.6	–	–	0.6	–	μs
	t_d	–	0.34	–	–	0.34	–	μs
	dV_O/dt	–	1.7	–	–	1.7	–	V/μs
Gain = 1, 5.0% overshoot	t_{THL}	–	2.2	–	–	2.2	–	μs
	t_d	–	1.3	–	–	1.3	–	μs
	dV_O/dt	–	0.25	–	–	0.25	–	V/μs
Power Supply Current	I_{DCC}	–	2.7	5.5	–	2.7	6.7	mAdc
	I_{DEE}	–	2.7	5.5	–	2.7	6.7	
DC Quiescent Power Dissipation (Power Supply = ±15 V, V_O = 0)	P_D	–	80	165	–	80	200	mW
Positive Supply Sensitivity (V_{EE} constant)	S^+	–	25	150	–	25	200	μV/V
Negative Supply Sensitivity (V_{CC} constant)	S^-	–	25	150	–	25	200	μV/V

See current MC1709/1709C data sheet for additional information.



Bump Dia. at Base: 0.006 ± 0.001 in. Bump Height: 0.0040 ± 0.0005 in.
Each bump centerline to be located within 0.001 in. of its true position with respect to any other bump centerline.

PACKAGING AND HANDLING

The popular 1709 type operational amplifier is now available in three chip forms: 1) conventional chips, 2) beam-lead chips and 3) flip-chips, as well as in a variety of plastic and hermetic packages. The flip-chip consists of a silicon chip with solder bumps on the geometry surface to provide easy mechanical mounting and electrical connection. These devices are protected by a thin layer of phosphorsilicate passivation which covers the interconnect metalization and active areas of the die.

Care must be exercised when removing the dice from the shipping carrier to avoid scratching the solder bumps. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

8

MCCF1741
MCCF1741C

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC FLIP-CHIP OPERATIONAL AMPLIFIER

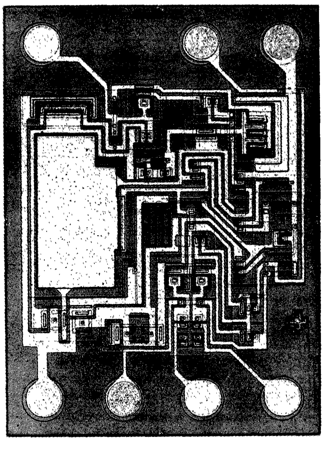
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCCF1741 and MCCF1741C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. The bumps are 90-10 solder on a chrome-copper-gold base. The interconnecting metalization is evaporated aluminum.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		MCCF1741C	MCCF1741	
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Differential Input Signal	V_{ID}	±30		Volts
Common Mode Input Swing (Note 1)	V_{IC}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Temperature Range	T_A	0 to +75	-55 to +125	°C
Junction Temperature Range	T_J	-65 to +150		°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

FIGURE 1 – CIRCUIT SCHEMATIC

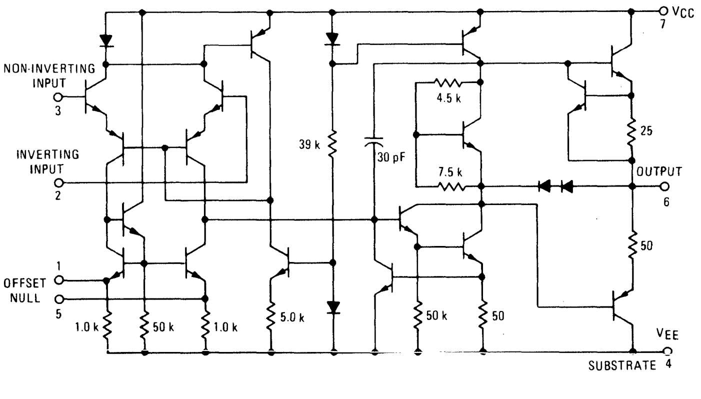
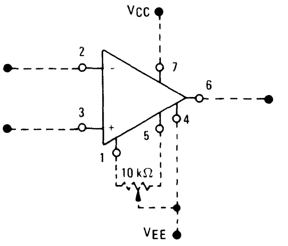


FIGURE 2 – OFFSET ADJUST CIRCUIT



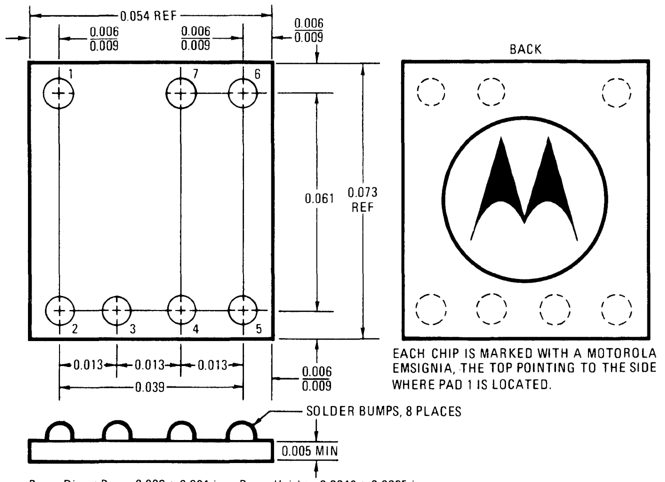
MCCF1741, MCCF1741C (continued)

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = 15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MCCF1741 Min	MCCF1741 Typ	MCCF1741 Max	MCCF1741C Min	MCCF1741C Typ	MCCF1741C Max	Unit
Open Loop Voltage Gain (R_L = 2.0 kΩ) (V_O = ±10 V)	A_{vol}	50,000	200,000	–	20,000	100,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_{in}	–	1.0	–	–	1.0	–	Meg Ω
Output Voltage Swing	V_O							V_{peak}
(R_L = 10 kΩ)		±12	±14	–	±12	±14	–	
(R_L = 2.0 kΩ)		±10	±13	–	±10	±13	–	
Input Common-Mode Voltage Swing	V_{IC}	–	±13	–	–	±13	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	–	90	–	–	90	–	dB
Input Bias Current	I_{IB}	–	0.2	0.5	–	0.2	0.5	μA
Input Offset Current	$\lvert I_{IO} \rvert$	–	0.03	0.2	–	0.03	0.2	μA
Input Offset Voltage (R_S = ≤ 10 kΩ)	$\lvert V_{IO} \rvert$	–	1.0	5.0	–	2.0	6.0	mV
Step Response Gain = 100	t_{THL}	–	29	–	–	29	–	μs
	t_d	–	8.5	–	–	8.5	–	μs
	dV_O/dt ①	–	1.0	–	–	1.0	–	V/μs
Gain = 10	t_{THL}	–	3.0	–	–	3.0	–	μs
	t_d	–	1.0	–	–	1.0	–	μs
	dV_O/dt ①	–	1.0	–	–	1.0	–	V/μs
Gain = 1	t_{THL}	–	0.6	–	–	0.6	–	μs
	t_d	–	0.38	–	–	0.38	–	μs
	dV_O/dt ①	–	0.8	–	–	0.8	–	V/μs
Power Supply Current	I_{DCC}	–	1.67	2.83	–	1.67	2.83	mA
	I_{DEE}	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation (Power Supply = ± 15 V, V_o = 0)	P_D	–	50	85	–	50	85	mW
Positive Supply Sensitivity (V_{EE} constant)	S^+	–	30	150	–	30	150	μV/V
Negative Supply Sensitivity (V_{CC} constant)	S^-	–	30	150	–	30	150	μV/V

① dV_O/dt = Slew Rate   See current MC1741/1741C data sheet for additional information.

MCCF1741/MCCF1741C BONDING DIAGRAM AND DEVICE DIMENSIONS



Bump Dia. at Base: 0.006 ± 0.001 in. Bump Height: 0.0040 ± 0.0005 in.
Each bump centerline to be located within 0.001 in. of its true position with respect to any other bump centerline.

PACKAGING AND HANDLING

The popular 1741 type operational amplifier is now available in three chip forms: 1) conventional chips, 2) beam-lead chips and 3) flip-chips, as well as in a variety of plastic hermetic packages. The flip-chip consists of a silicon chip with solder bumps on the geometry surface to provide easy mechanical mounting and electrical connection. These devices are protected by a thin layer of phosphorsilicate passivation which covers the interconnect metalization and active areas of the die.

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The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MFC4000B

AUDIO AMPLIFIER

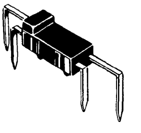
1/4-WATT AUDIO AMPLIFIER

. . . designed for the output stage of battery-powered portable radios.

- 250 mW of Audio Output Power
- Low Standby Current – 3.5 mA typical
- Low Harmonic Distortion
- Reduces Component Count in Portable Radios

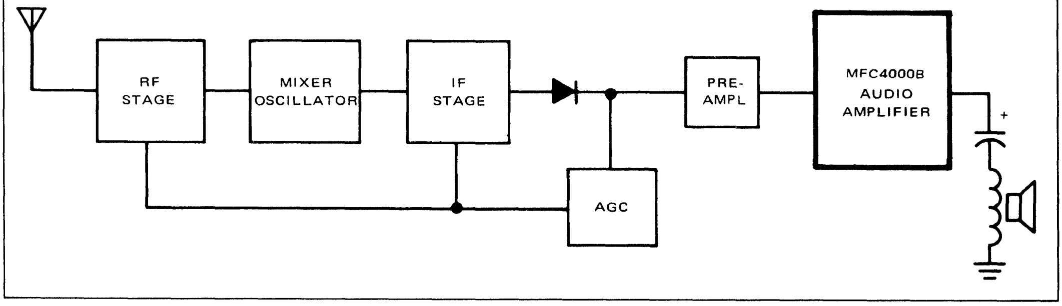
1/4-WATT AUDIO AMPLIFIER

SILICON MONOLITHIC FUNCTIONAL CIRCUIT



PLASTIC PACKAGE
CASE 206A

TYPICAL APPLICATION



MAXIMUM RATINGS (T_A = + 25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	12	Vdc
Power Dissipation (Package Limitation) (Soldered on a circuit board and held in free air) Derate above T_A = +25°C	1.0 10	Watt mW/°C
Operating Temperature Range	-10 to +75	°C

See Packaging Information Section for outline dimensions.

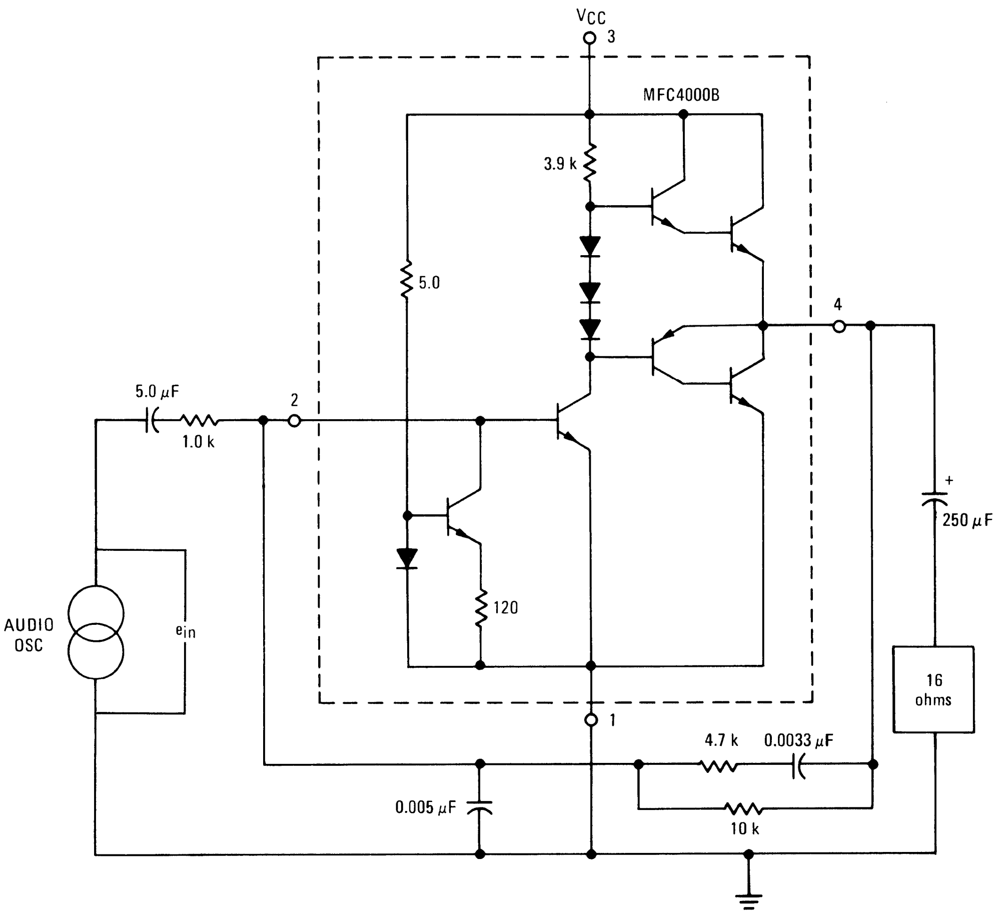
8

ELECTRICAL CHARACTERISTICS* (V_{CC} = 9.0 Vdc, R_L = 16 Ohms, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Zero Signal Current Drain	–	3.0	5.0	mAdc
Sensitivity P_O = 250 mW(RMS)	–	–	240	mV(RMS)
Output Power Total Harmonic Distortion ⩽ 10%	250	350	–	mW(RMS)
Total Harmonic Distortion P_O = 50 mW(RMS) P_O = 50 mW(RMS), V_{CC} = 6.0 Vdc	 – –	 0.7 4.5	 – –	%

*As measured in test circuit shown in Figure 1.

FIGURE 1 – TEST CIRCUIT



8

TOTAL HARMONIC DISTORTION versus OUTPUT POWER

FIGURE 2 – V_{CC} = 9.0 Vdc

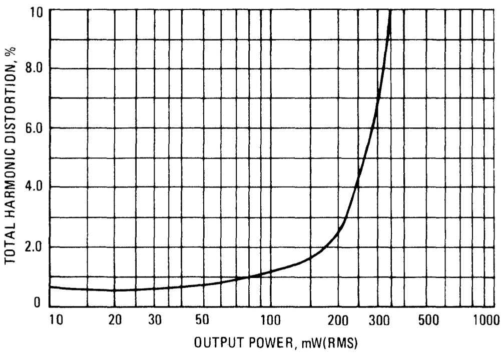


FIGURE 3 – V_{CC} = 6.0 Vdc

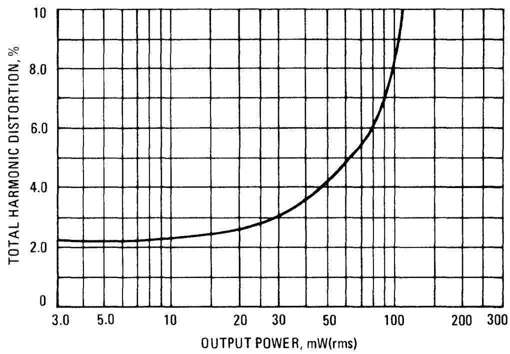


FIGURE 4 – CURRENT DRAIN versus OUTPUT POWER

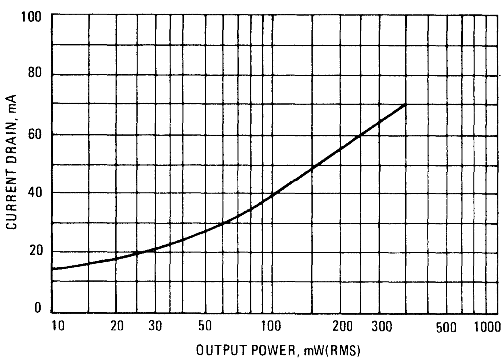


FIGURE 5 – TOTAL HARMONIC DISTORTION versus SUPPLY VOLTAGE

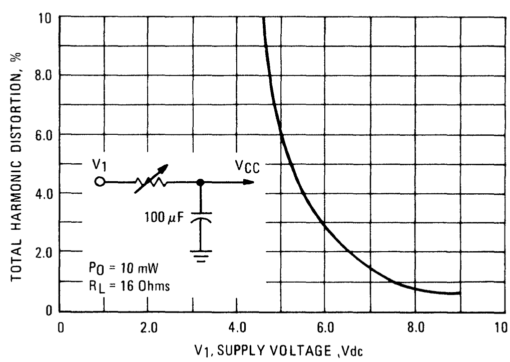
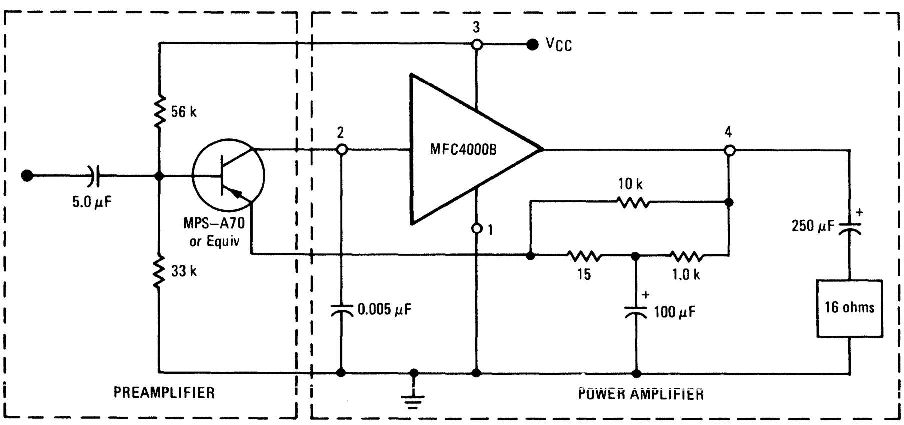


FIGURE 6 – TYPICAL CIRCUIT APPLICATION



MFC4010A

HIGH FREQUENCY CIRCUIT

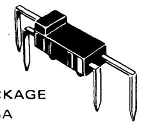
WIDE-BAND AMPLIFIER

. . . designed for FM/IF and low-level audio applications.

- High Audio Gain – 60 dB minimum
- Useful as a Microphone Amplifier and in Tape Recorders and Cassettes
- Excellent Performance as a 10.7 MHz FM/IF Amplifier
- High Transconductance (g_m) Ideally Suited to Low Impedance Ceramic Filters

WIDE-BAND AMPLIFIER

Silicon Monolithic Functional Circuit



PLASTIC PACKAGE
CASE 206A

TYPICAL APPLICATIONS

FIGURE 1 – FM/IF AMPLIFIER

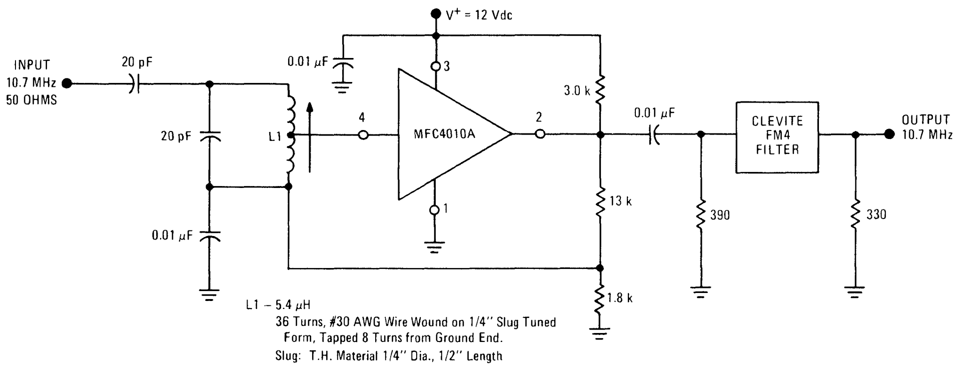
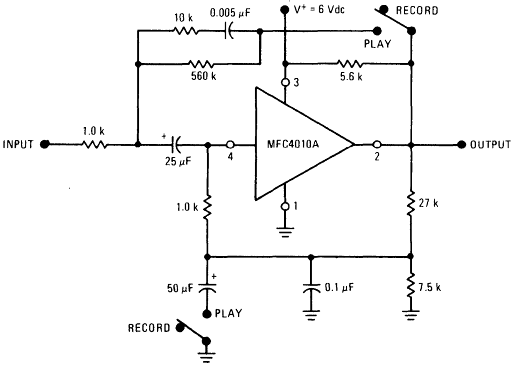


FIGURE 2 – RECORD/PLAY PREAMPLIFIER FOR CASSETTE AND PORTABLE TAPE RECORDERS



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	18	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation) Derate above 25°C	P_D	0.5 5.0	Watt mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

ELECTRICAL CHARACTERISTICS (V^+ = 6.0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Open Loop Voltage Gain (Figure 3) (f = 1.0 kHz)	A_{VOL}	60	68	–	dB
h Parameters (1) (f = 1.0 kHz)	h_{11} h_{12} h_{21} h_{22}	– – – –	1.0 10^{-6} 1000 10^{-5}	– – – –	k ohms – – mhos
Output Noise Voltage (Figure 3) (BW = 20 Hz to 20 kHz, R_S = 1.0 k ohms)	$e_{n(out)}$	–	3.0	–	mV(rms)
Current Drain	I_D	–	3.0	–	mA

HIGH FREQUENCY CHARACTERISTICS (V^+ = 12 Vdc, f = 10.7 MHz, T_A = 25°C unless otherwise noted)

Power Gain (Figure 1) (e_{in} = 0.1 mVrms)	–	–	42	–	dB
Noise Figure (Figure 1) ($R_S \approx$ 740 Ohms)	NF	–	6.0	–	dB
y Parameters(1) (f = 10.7 MHz, I_2 = 2.0 mA)	y_{11} y_{12} y_{21} y_{22}	– – – –	1.3 + j1.5 -3.4 + j8.1 -0.33 + j0.68 120 + j0	– – – –	mmhos μmhos mhos μmhos

(1) Device only, without external passive components.

FIGURE 3 — AUDIO TEST CIRCUIT

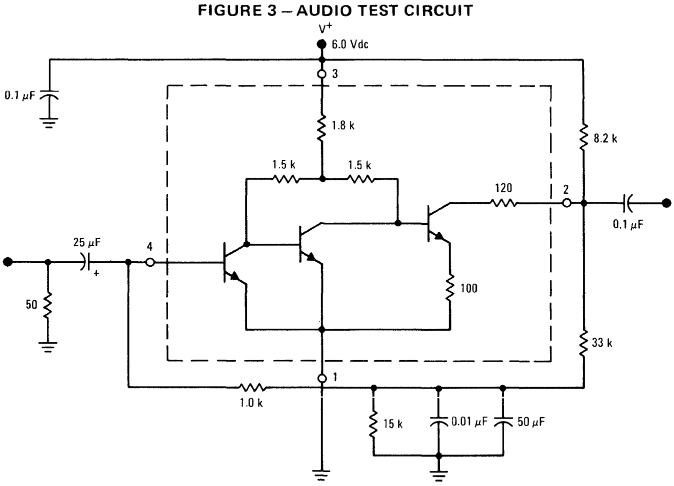
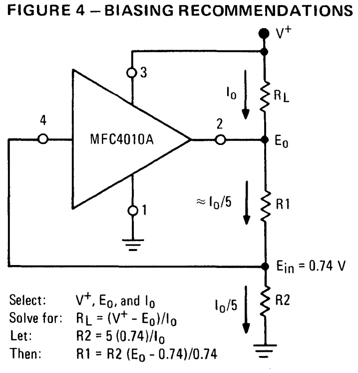


FIGURE 4 — BIASING RECOMMENDATIONS



8

AUDIO PERFORMANCE CHARACTERISTICS
(for Test Circuit Figure 3)

FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

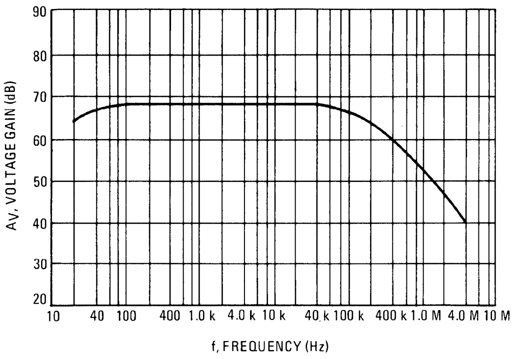
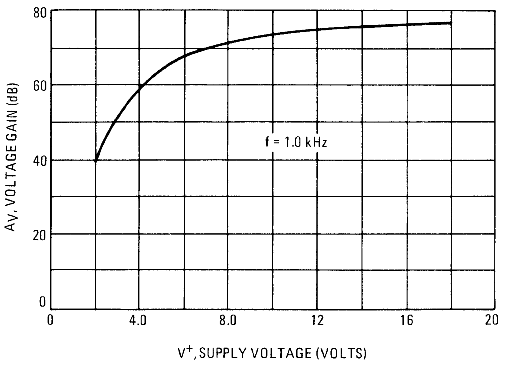


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY



*TAPE PREAMPLIFIER PERFORMANCE
(for Circuit Figure 2)

FIGURE 7 – RECORD VOLTAGE GAIN versus FREQUENCY

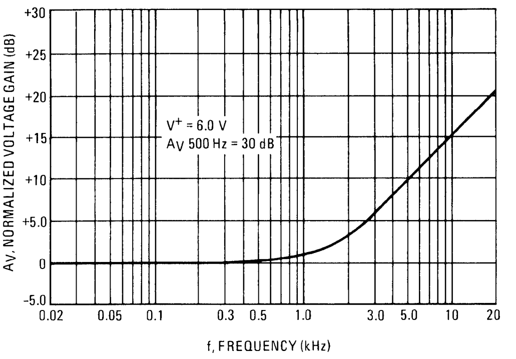
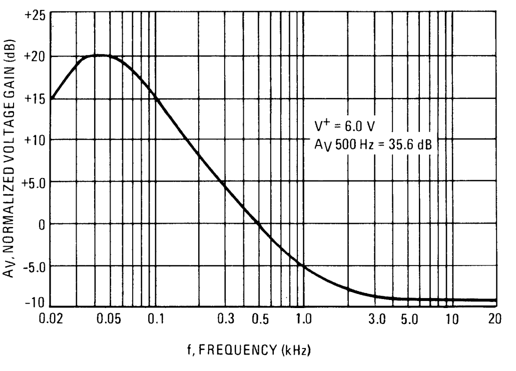


FIGURE 8 – PLAYBACK VOLTAGE GAIN versus FREQUENCY



Note:

The record/playback characteristics shown in Figures 8 and 9 were taken with the preamplifier driven by a 50 ohm source. The curves are typical of a desired response for the preamplifier; however, every type of tape recording and playback head is different and this circuit will not necessarily satisfy all requirements. No particular tape head was used as a basis for circuit design. The circuit is only an example showing the equalization network configuration.

The ideal preamplifier will have an input impedance approximately 10 times the highest impedance of the tape head and every preamplifier circuit must be designed using a test tape to verify the response of the design.

10.7 MHz y PARAMETERS

FIGURE 9 – INPUT ADMITTANCE

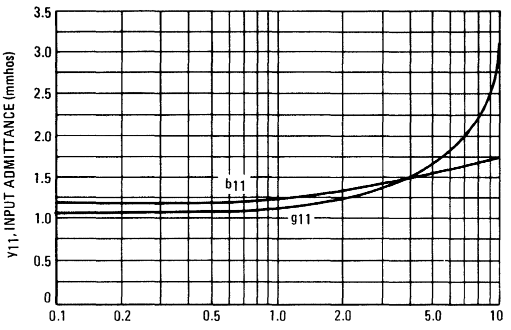


FIGURE 10 – REVERSE TRANSFER ADMITTANCE

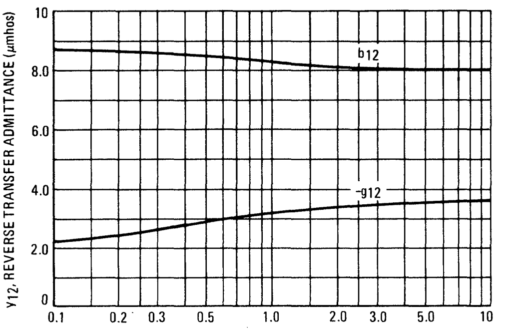


FIGURE 11 – FORWARD TRANSFER ADMITTANCE

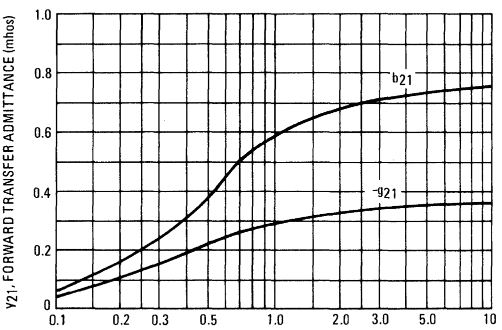
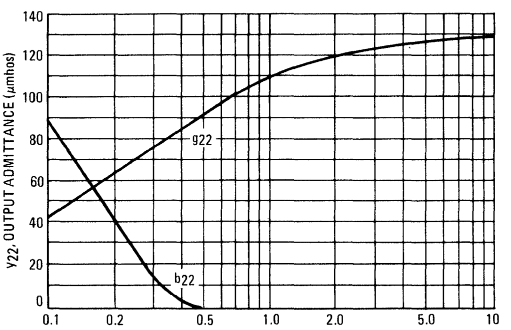


FIGURE 12 – OUTPUT ADMITTANCE



10.7 MHz PERFORMANCE
(Circuit of Figure 1)

FIGURE 13 – POWER GAIN versus SUPPLY VOLTAGE

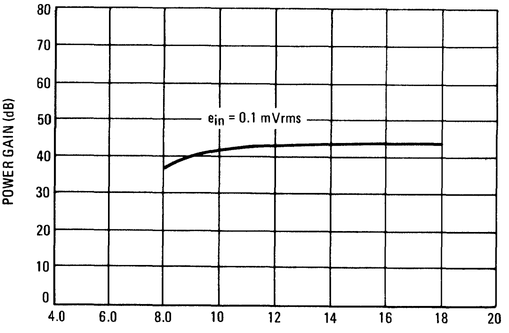
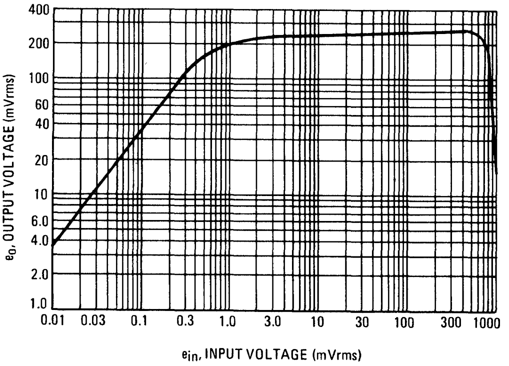


FIGURE 14 – VOLTAGE TRANSFER CHARACTERISTIC



8

MFC4040

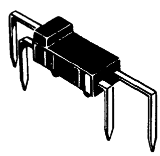
SINGLE TOGGLE FLIP-FLOP

SINGLE TOGGLE FLIP-FLOP

- Wide Operating Voltage Range – 6.0 to 16 Volts
- Regulated Supply Not Required
- Economical 4-Lead Plastic Package

SINGLE TOGGLE FLIP-FLOP

Silicon Monolithic Functional Circuit

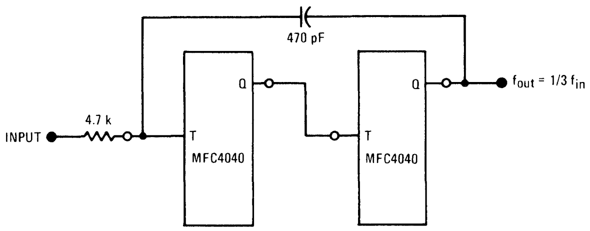


CASE 206A
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

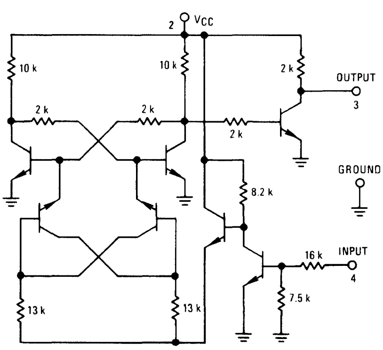
Rating	Value	Volts
Power Supply Voltage	19	Vdc
Output Sinking Current	10	mA
Negative Input Voltage	0.5	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	1.0 10	Watt mW/°C
Operating Temperature Range	-10 to +75	°C

TYPICAL APPLICATION

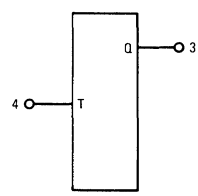


Divide-by-3 Circuit

FIGURE 1 – CIRCUIT SCHEMATIC



BLOCK DIAGRAM



V_{CC} = Pin 2
GND = Pin 1

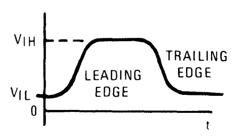
See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, V_{in} = 4.0 V(p-p) Square Pulse, f = 10 kHz, 50% Duty Cycle, t_{PHL} = 1.0 V/µs, T_A = +25°C unless otherwise noted.)

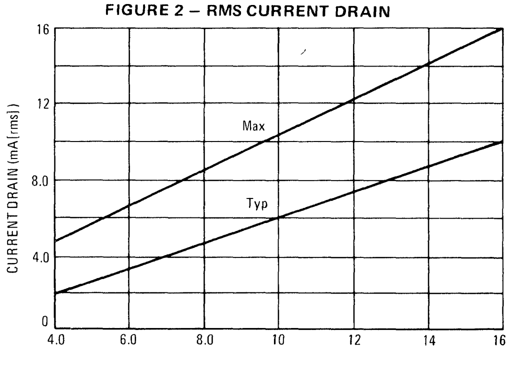
Characteristic	Min	Typ	Max	Unit
Operating Power Supply Voltage	6.0	–	16	Vdc
Toggle Frequency	–	3.0	–	MHz
Output Voltage (High) (V_{CC} = 6.0 Vdc) (V_{CC} = 16 Vdc)	 5.5 15.5	 – –	 – –	Vdc
Output Voltage (Low) (V_{CC} = 6.0 Vdc) (V_{CC} = 16 Vdc)	 – –	 – –	 0.3 0.5	Vdc
Operating Drain Current (V_{CC} = 16 Vdc)	–	–	32	mAdc
Output Sinking Current ($V_O \leqslant$ 1.0 Vdc)	–	2.0	–	mAdc
Rise Time	–	250	–	ns
Storage Time	–	350	–	ns
Fall Time	–	60	–	ns
Input Resistance	10	–	–	kΩ
Output Resistance (Output High)	–	–	2.8	kΩ

INPUT PULSE REQUIREMENTS



Characteristic	Min	Max	Unit
Pulse Magnitude	+4.0	–	Volts
Zero Level	–	+1.0	Volts
Leading Edge	No Requirement		
Trailing Edge $\frac{dv}{dt}$	-1.0	–	$\frac{\text{Volts}}{\text{ms}}$

FIGURE 2 – RMS CURRENT DRAIN



8

MFC4050

AUDIO DRIVER

Advance Information

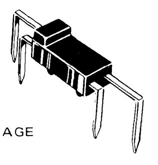
CLASS "A" AUDIO DRIVER

. . . designed for driving Class "A" PNP power output transistor stage applications.

- Drives to 4 Watts of Output Power
- Ideal for 12 Volt Automotive Equipment
- No Gain Selection of Power Transistors Necessary
- Economical 4-Lead Package

CLASS "A" AUDIO DRIVER

Silicon Monolithic Functional Circuit

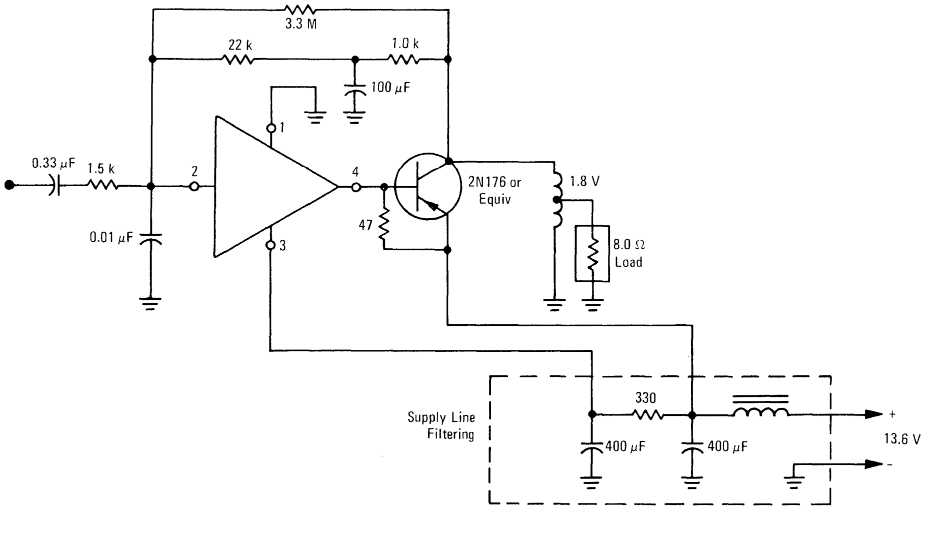


CASE 206A
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	18	Vdc
Power Dissipation @ T_A = 25°C (Package Dissipation)	P_D	1.0	Watt
Derate above 25°C	$1/\theta_{JA}$	10	mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

FIGURE 1 – TYPICAL 4-WATT AMPLIFIER CIRCUIT APPLICATION



See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

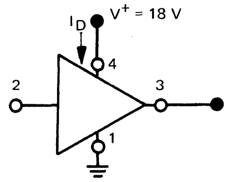
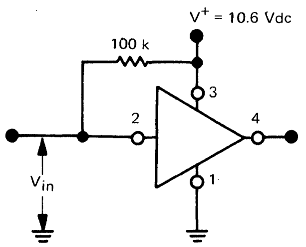
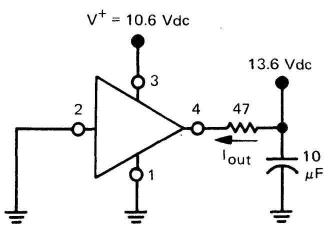
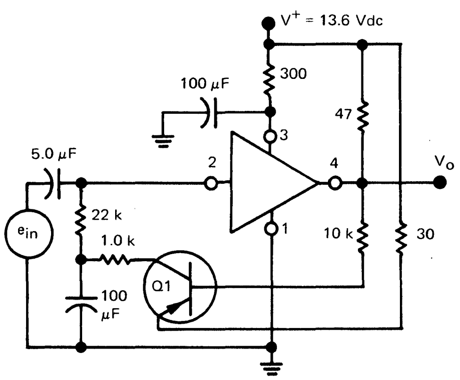
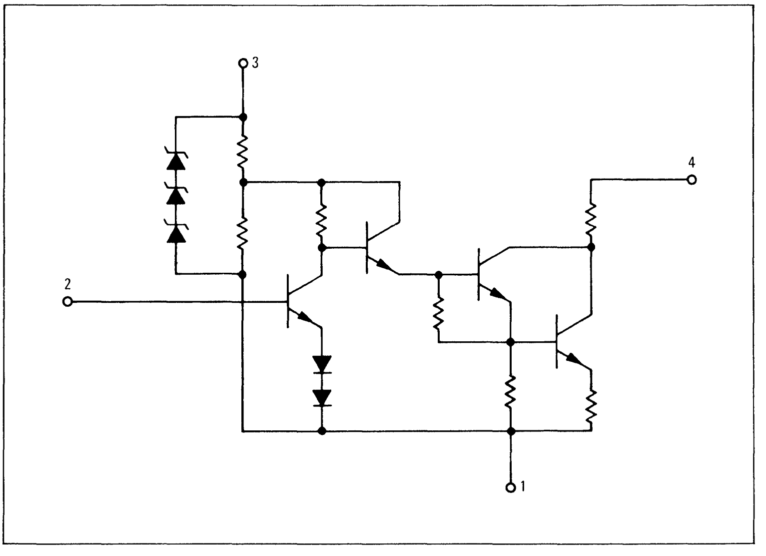
Circuit	Characteristic	Symbol	Min	Max	Unit
	Current Drain No Load	I_D	–	10	mA
	Input Voltage	V_{in}	1.9	2.5	Vdc
	Output Current	I_{out}	30	–	mAdc
	Open Loop Voltage Gain (e_{in} = 1.0 mV(rms) @ 1.0 kHz) Q1: MPS6514 or equiv.	A_{VOL}	130	–	V/V

FIGURE 2 – CIRCUIT SCHEMATIC



MFC4060A
MFC4062A
MFC4063A
MFC4064A

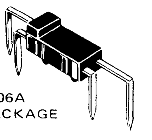
MONOLITHIC VOLTAGE REGULATORS

This series of voltage regulators is designed to deliver load currents to 200 mAdc. Output current capability can be increased to several amperes through the use of external pass transistors. These devices are industrial quality regulators designed for consumer applications requiring high volume and low cost.

- Excellent Line and Load Regulation
- Economical Four-Lead Package

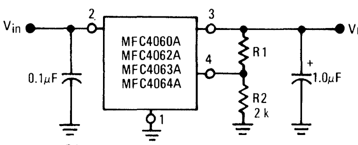
VOLTAGE REGULATORS

Silicon Monolithic Functional Circuit



CASE 206A
PLASTIC PACKAGE

FIGURE 1 – TYPICAL CIRCUIT CONNECTION AND TEST CIRCUIT



$$V_O = \left(\frac{R1}{2k} + 1\right) V_{Ref}$$

$$R1 \approx \left(\frac{V_O}{2} - 2\right) k\Omega$$

FIGURE 2 – 5-VOLT, 5-AMPERE REGULATOR WITH REMOTE SENSING PNP CURRENT BOOST

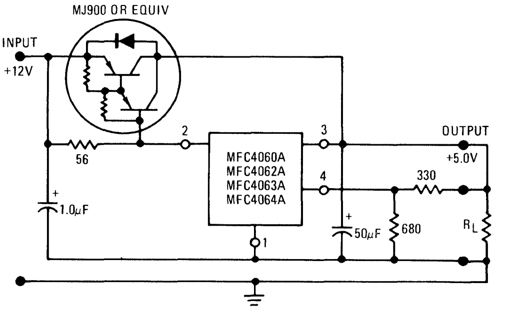
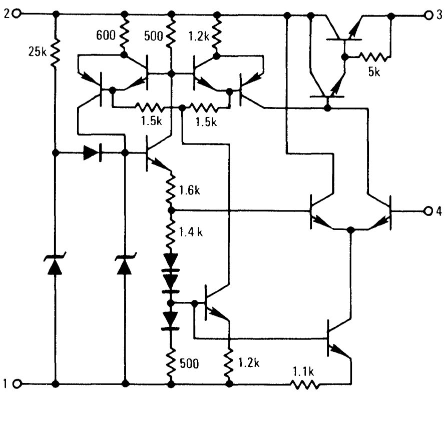


FIGURE 3 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Input Voltage	MFC4060A/MFC4062A MFC4063A/MFC4064A	V_{in}	38 22	Vdc Vdc
Maximum Load Current		I_L	200	mAdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C		P_D	1.0 10	Watt mW/°C
Operating Temperature Range (Ambient)		T_A	-10 to +75	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, See Figure 1.)

Characteristic	Symbol	MFC4060A			MFC4062A			MFC4063A			MFC4064A			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	9.0	–	38	9.0	–	38	9.0	–	22	9.0	–	22	Vdc
Output Voltage Range	V_O	V_{ref}	–	35	V_{ref}	–	35	V_{ref}	–	19	V_{ref}	–	19	Vdc
Input-Output Voltage Differential	V_{in}-V_O	3.0	–	–	3.0	–	–	3.0	–	–	3.0	–	–	Vdc
Reference Voltage	V_{ref}	3.6	4.1	4.6	3.6	4.1	4.6	3.6	4.1	4.6	3.6	4.1	4.6	Vdc
Standby Current Drain (I_L = 0, V_{in} = 20 V)	I_{IB}	–	3.7	6.0	–	3.7	7.0	–	3.7	6.0	–	3.7	7.0	mAdc
Average Temperature Coefficient of Output Voltage (T_A = -10 to +75°C)	TC_{VO}	–	0.003	0.03	–	0.003	0.03	–	0.003	0.03	–	0.003	0.03	%/°C
Line Regulation (V_O = 7.5 V) 12 V < V_{in} < 18 12 V < V_{in} < 30	Reg_{in}	 – –	 – 0.01	 – 0.03	 – –	 – –	 – 0.06	 – –	 0.01 –	 0.03 –	 – –	 – –	 0.06 –	%/V_{in}
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_L	–	0.03	0.2	–	–	0.4	–	0.03	0.2	–	–	0.4	%

LINE REGULATION

$$\%/V_{in} = \frac{\Delta V_O \times 100}{\Delta V_{in} \times V_O}$$

LOAD REGULATION

$$\% = \frac{\Delta V_O}{V_O} \times 100$$

TYPICAL CHARACTERISTICS

(V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT versus INPUT-OUTPUT VOLTAGE

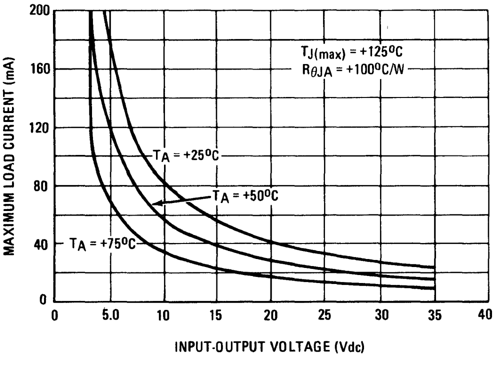
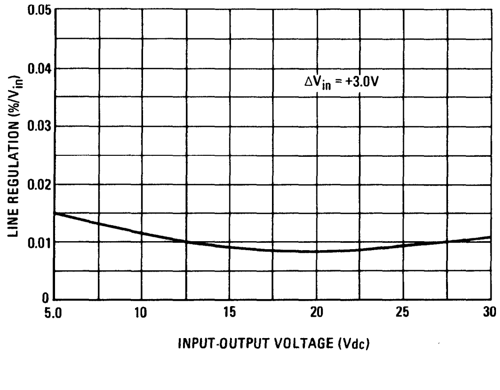


FIGURE 5 – LINE REGULATION versus INPUT-OUTPUT VOLTAGE



8

MFC6010

FM IF AMPLIFIER

FM LIMITING IF AMPLIFIER

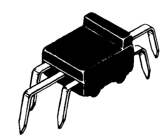
. . . a monolithic silicon integrated circuit designed especially for 10.7 MHz IF applications.

Highlights Include:

- High Stable Gain @ 10.7 MHz (40 dB typ)
- Low Feedback Capacitance ($|y_{12}|$ = 0.01 mmho typ)
- Non-Saturating Limiting (With Suitable Load)
- Compatible With CA3053 and μA703 (See Figures 7 and 8)

FM IF AMPLIFIER

Silicon Monolithic Functional Circuit



CASE 643A

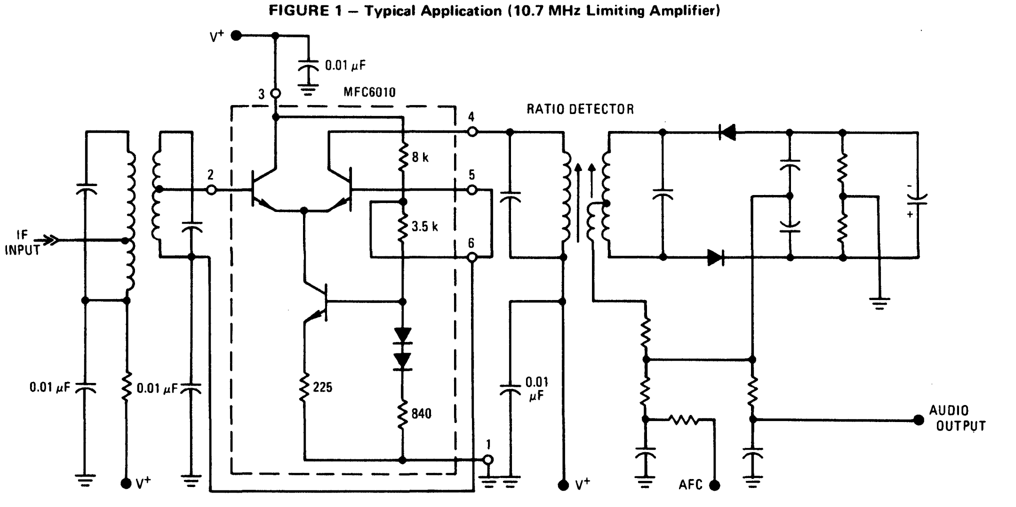
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	20	Vdc
Output Collector Voltage	V_4	20	Vdc
Input Voltage*	V_2, V_5	±5.0	Volts
Power Dissipation @ T_A = 25°C (Package Limitation)	P_D	1.0	Watt
Derate above 25°C	$1/\theta_{JA}$	10	mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

*Differential Voltage Swing.

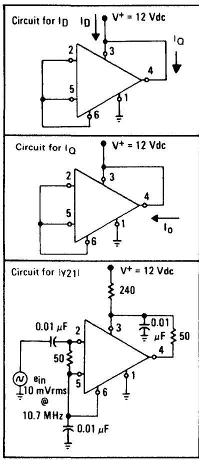
FIGURE 1 – Typical Application (10.7 MHz Limiting Amplifier)



See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS (V^+ = 12 Volts, f = 10.7 MHz, T_A = +25°C, unless otherwise noted.)



Characteristic	Symbol	Min	Typ	Max	Unit
Total Current Drain	I_D	–	–	10	mA
Output Quiescent Current	I_Q	1.75	3.2	5.0	mA
Output Saturation Voltage	V(sat)	–	3.5	–	Volts
Forward Transadmittance	$\|y_{21}\|$	25	–	–	mmhos
Reverse Transadmittance	$\|y_{12}\|$	–	0.01	–	mmho
Input Capacitance	C_{in}	–	6.0	–	pF
Input Conductance	G_{in}	–	0.4	–	mmho
Output Capacitance	C_{out}	–	2.5	–	pF
Output Conductance	G_{out}	–	35	–	µmhos
Noise Figure (R_S = 750 Ω)	N_F	–	7.0	–	dB
Maximum Stable Gain (Stern Factor = 3)	A_V	–	40	–	dB
Input Voltage (3.0 dB Limiting)	e_{in}	–	60	–	mV

FIGURE 2 – LIMITING CHARACTERISTICS

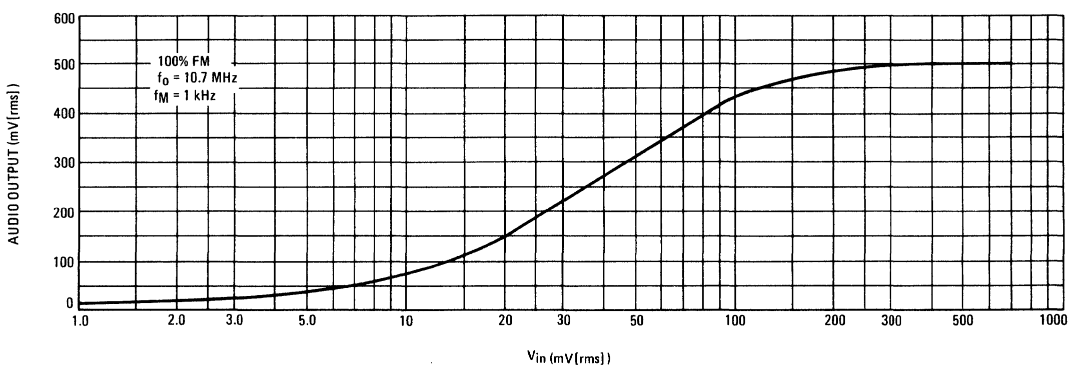


FIGURE 3 – AM REJECTION

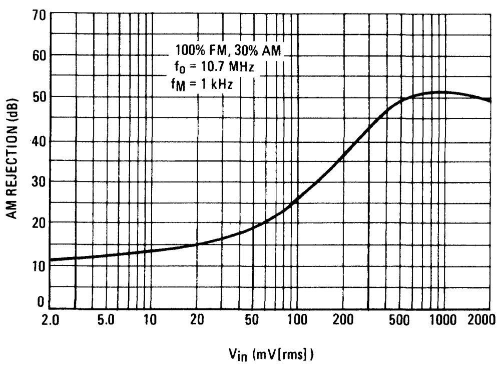
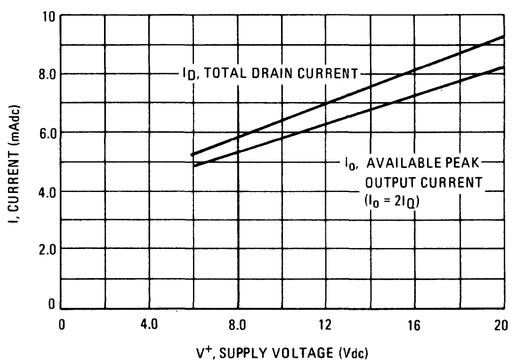
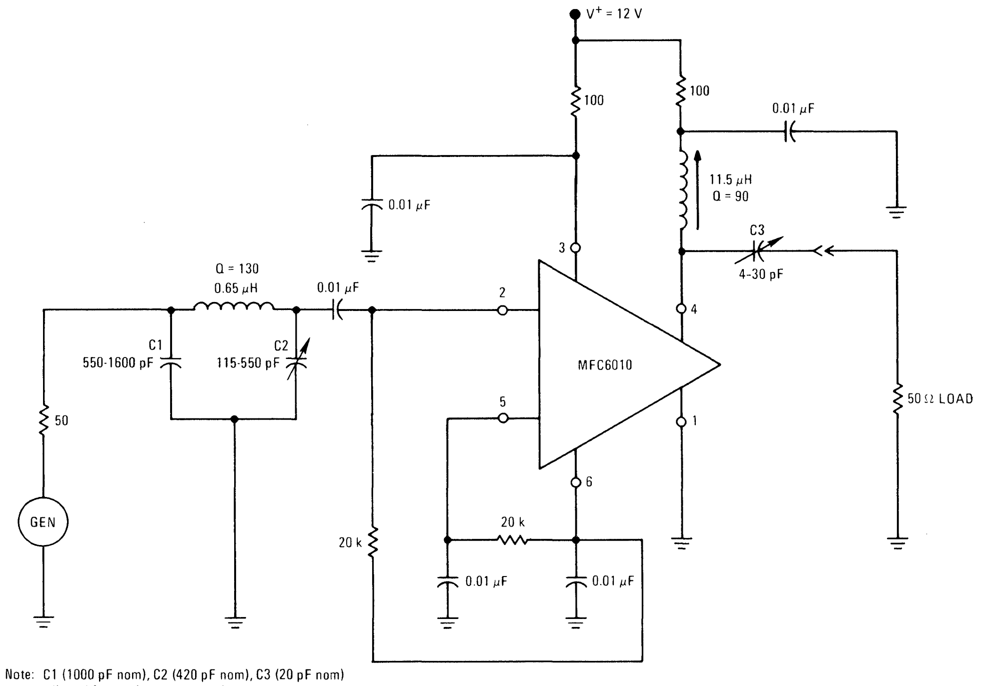


FIGURE 4 – CURRENT DRAIN AND OUTPUT CURRENT



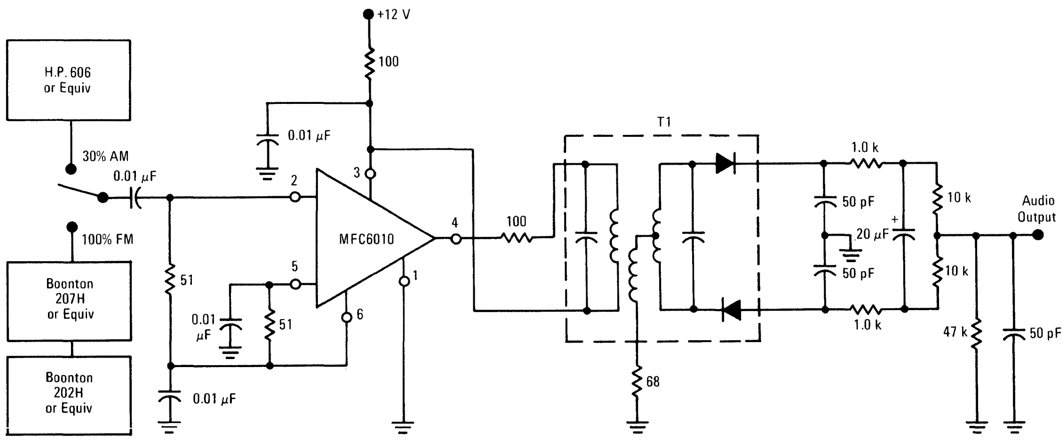
TEST CIRCUITS

FIGURE 5 – POWER-GAIN TEST CIRCUIT



Note: C1 (1000 pF nom), C2 (420 pF nom), C3 (20 pF nom) adjusted for maximum power gain.

FIGURE 6 – LIMITING AND AM REJECTION TEST CIRCUIT



T1 – Ratio Detector Primary Impedance ≈ 1.5 kΩ

APPLICATIONS INFORMATION

Because of the low reverse transfer admittance of the MFC6010, stability will be dependent mainly upon circuit layout. With careful design, very high gain (in the order of 40 dB) may be achieved at 10.7 MHz. The bias and supply currents may be varied from their normal values (shown in Figure 4) by shunting additional resistance from pin 6 to ground or to the supply line.

Although less gain may be realized when using the MFC6010 as a limiter, it is recommended that it be operated in a non-saturated mode. This mode of operation results in a high output impedance at limiting. Therefore the operation of the demodulator circuit is not subject to variable loading of the limiter output.

In order to avoid driving the amplifier transistor components of the MFC6010 into saturation, the load resistance must be chosen to ensure that current limiting occurs before the collector voltage drops to a value low enough to forward bias the collector-base junction. In a transformer coupled circuit, the maximum allowable load can be derived from

$$R_L = \frac{2\,(V^+ - V_5)}{I_o}$$

where values for I_o may be determined from Figure 4 (providing the bias currents have not been altered from their normal values).

In order to avoid degradation of AM rejection, the input signal should not exceed one volt (rms).

COMPATIBLE FOIL PATTERNS

FIGURE 7 — μA703 and MFC6010

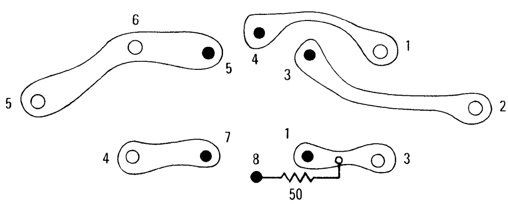
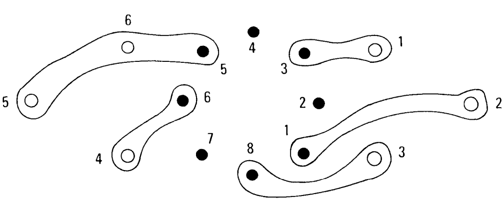


FIGURE 8 — CA3053* and MFC6010



O Motorola terminal and pin number position ● μA703 or CA3053 terminal and pin number position

*Foil patterns shown are intended to show pin-for-pin interconnection. Any change in the number of components is dictated by the requirements of the individual design.

8

MFC6020

DUAL TOGGLE FLIP-FLOP

DUAL TOGGLE FLIP-FLOP

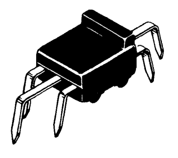
- Wide Operating Voltage Range – 6.0 to 16 Volts
- Regulated Supply Not Required
- Economical 6-Lead Plastic Package

DUAL TOGGLE FLIP-FLOP

Silicon Monolithic Functional Circuit

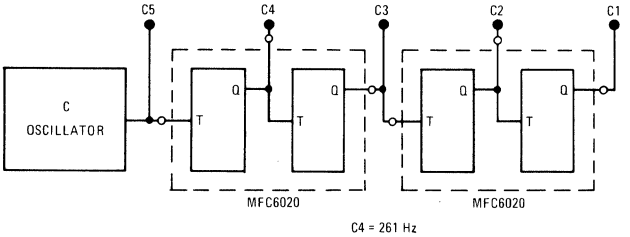
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Volts
Power Supply Voltage	19	Vdc
Output Sinking Current	10	mA
Negative Input Voltage	0.5	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	1.0 10	Watts mW/°C
Operating and Storage Junction Temperature Range	-40 to +125	°C
Operating Temperature	-10 to +75	°C



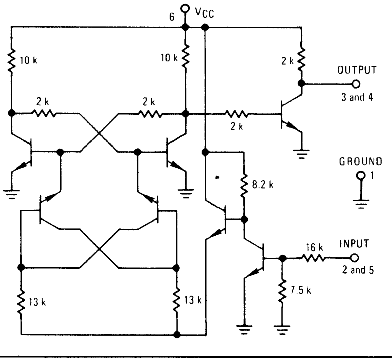
CASE 643A
PLASTIC PACKAGE

TYPICAL APPLICATION – ELECTRONIC ORGAN DIVIDER

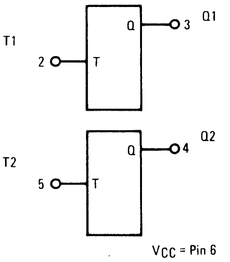


C4 = 261 Hz

FIGURE 1 – CIRCUIT SCHEMATIC (One Half of Circuit Shown)



BLOCK DIAGRAM



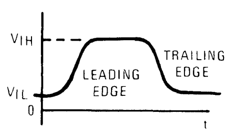
V_{CC} = Pin 6
GND = Pin 1

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, V_{in} = 4.0 V, Square Pulse, f = 10 kHz, 50% Duty Cycle, t_{PHL} = 1.0 V/μs, T_A = +25°C unless otherwise noted.)

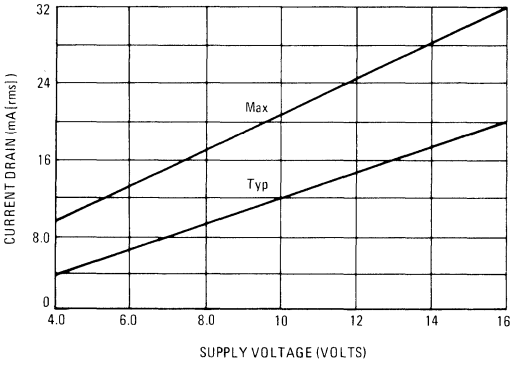
Characteristic	Min	Typ	Max	Unit
Operating Power Supply Voltage	6.0	–	16	Vdc
Toggle Frequency	–	3.0	–	MHz
Output Voltage (High)				Vdc
(V_{CC} = 6.0 Vdc)	5.5	–	–	
(V_{CC} = 16 Vdc)	15.5	–	–	
Output Voltage (Low)				Vdc
(V_{CC} = 6.0 Vdc)	–	–	0.3	
(V_{CC} = 16 Vdc)	–	–	0.5	
Operating Drain Current (V_{CC} = 16 Vdc)	–	–	32	mAdc
Output Sinking Current ($V_O \leqslant 1.0$ Vdc)	–	2.0	–	mAdc
Rise Time	–	250	–	ns
Storage Time	–	350	–	ns
Fall Time	–	60	–	ns
Input Resistance	10	–	–	kΩ
Output Resistance (Output High)	–	–	2.8	kΩ

INPUT PULSE REQUIREMENTS



Characteristic	Min	Max	Unit
Pulse Magnitude	+4.0	–	Volts
Zero Level	–	+1.0	Volts
Leading Edge	No Requirement		
Trailing Edge dv/dt	-1.0	–	Volts/ms

FIGURE 2 – RMS CURRENT DRAIN versus SUPPLY VOLTAGE



8

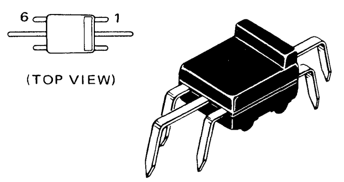
MFC6030A
MFC6032A
MFC6033A
MFC6034A

MONOLITHIC VOLTAGE REGULATORS

This series of voltage regulators is designed to deliver load currents to 200 mAdc. Output current capability can be increased to several amperes through the use of external pass transistors. These devices are industrial quality regulators intended for consumer applications requiring high volume and low cost.

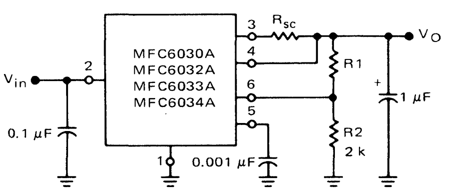
- Excellent Line and Load Regulation
- Current-Limit Feature Available
- Economical Six-Lead Package

VOLTAGE REGULATORS
MONOLITHIC SILICON
FUNCTIONAL CIRCUITS



PLASTIC PACKAGE
CASE 643A

FIGURE 1 – TYPICAL CIRCUIT CONNECTION AND TEST CIRCUIT



$$V_O = \left(\frac{R1}{2k} + 1\right) V_{ref}$$

$$R1 \approx \left(\frac{V_O}{2} - 2\right) k\Omega$$

FIGURE 2 – 15-VOLT, 1.0-AMPERE REGULATOR
(with short-circuit protection)

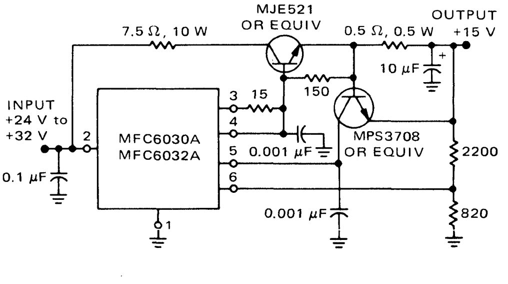
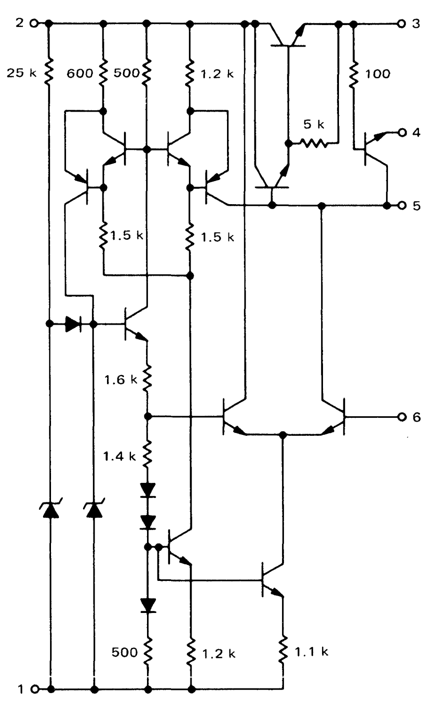


FIGURE 3 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

8

MFC6030A, MFC6032A, MFC6033A, MFC6034A (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating	Symbol	Value	Unit
Input Voltage MFC6030A, MFC6032A MFC6033A, MFC6034A	V_{in}	 38 22	Vdc
Maximum Load Current	I_L	200	mAdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	1.0 10	Watt mW/°C
Operating Temperature Range (Ambient)	T_A	-10 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{in} = +12 Vdc, V_O = +5.0 Vdc, I_L = 1.0 mAdc, R_{sc} = 0, T_A = +25°C unless otherwise noted.) (See Figure 1)

Characteristic	Symbol	MFC6030A			MFC6032A			MFC6033A			MFC6034A			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	9.0	–	38	9.0	–	38	9.0	–	22	9.0	–	22	Vdc
Output Voltage Range	V_O	V_{Ref}	–	35	V_{Ref}	–	35	V_{Ref}	–	19	V_{Ref}	–	19	Vdc
Input-Output Voltage Differential	V_{in}-V_O	3.0	–	–	3.0	–	–	3.0	–	–	3.0	–	–	Vdc
Reference Voltage (R1 = 0)	V_{ref}	3.6	4.1	4.6	3.6	4.1	4.6	3.6	4.1	4.6	3.6	4.1	4.6	Vdc
Standby Current Drain (I_L = 0, V_{in} = 20 V)	I_{IB}	–	3.7	6.0	–	3.7	7.0	–	3.7	6.0	–	3.7	7.0	mAdc
Average Temperature Coefficient of Output Voltage (T_A = -10 to +75°C)	TCV_O	–	0.003	0.03	–	0.003	0.03	–	0.003	0.03	–	0.003	0.03	%/°C
Line Reg. (V_O = 7.5 V) (12 V < V_{in} < 18) (12 V < V_{in} < 30)	Reg_{in}	 – –	 – 0.01	 – 0.03	 – –	 – –	 – 0.06	 – –	 0.01 –	 0.03 –	 – –	 – –	 0.06 –	%/V_{in}
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_L	–	0.03	0.2	–	–	0.4	–	0.03	0.2	–	–	0.4	%/V_O
Short-Circuit Current Limit (R_{sc} = 100 ohms, V_O = 0)	I_{sc}	–	6.5	–	–	6.5	–	–	6.5	–	–	6.5	–	mAdc

LINE REGULATION

$$\%/V_{in} = \frac{\Delta V_O \times 100}{\Delta V_{in} \times V_O}$$

LOAD REGULATION

$$\% = \frac{\Delta V_O}{V_O} \times 100$$

SHORT-CIRCUIT CURRENT

$$I_{SC} = \frac{V_{BE}}{R_{sc}} \approx \frac{0.65\ (\text{at } T_J = +25^\circ C)}{100\ \text{ohms}}$$

TYPICAL CHARACTERISTICS

(V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{sc} = 0, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT versus INPUT-OUTPUT VOLTAGE

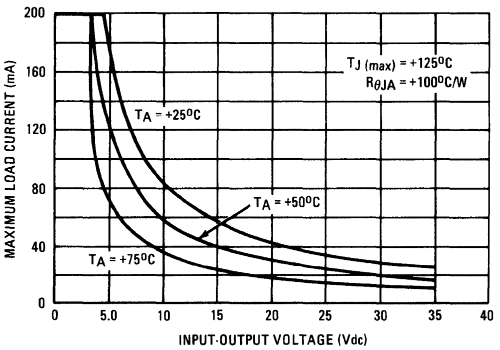
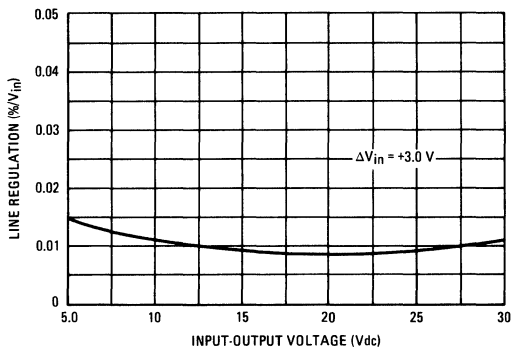


FIGURE 5 – LINE REGULATION versus INPUT-OUTPUT VOLTAGE



8

TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – LOAD REGULATION versus INPUT-OUTPUT VOLTAGE

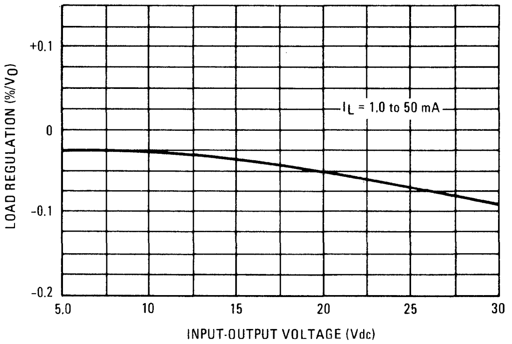


FIGURE 7 – LOAD REGULATION WITH CURRENT LIMITING

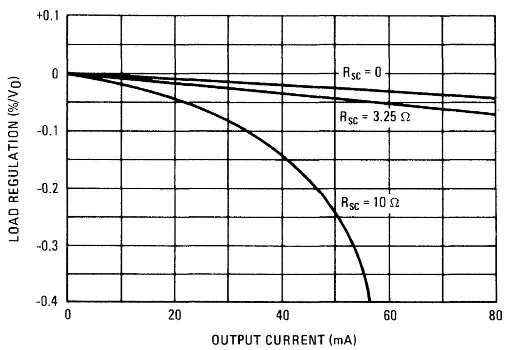
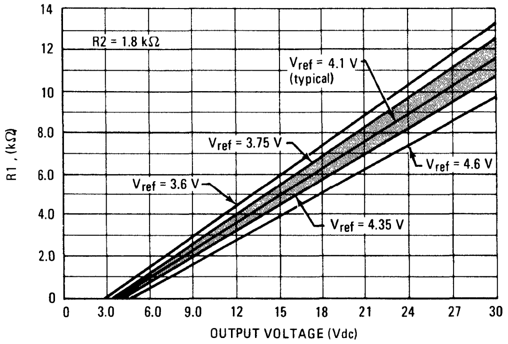
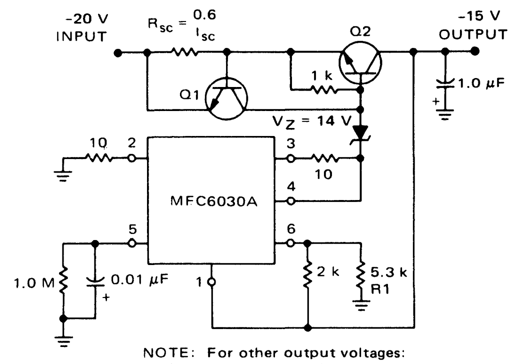


FIGURE 8 – OUTPUT VOLTAGE versus R1



TYPICAL APPLICATIONS

FIGURE 9 – MFC6030A -15 VOLT REGULATOR with CURRENT LIMIT

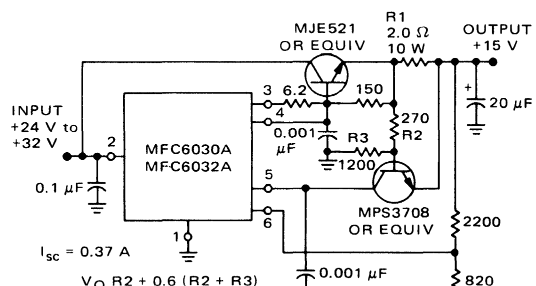


NOTE: For other output voltages:
($-9\ V \leqslant V_O \leqslant -35\ V$)

$$R1\ (k\Omega) = \frac{2\,|V_O|}{V_{ref}} - 2$$

$$V_z = |V_{in}| - \frac{|V_O|}{2} + 1$$

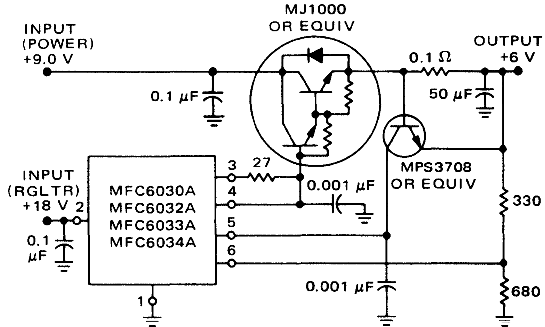
FIGURE 10 – 15-VOLT, 2.0-AMPERE REGULATOR (with current foldback)



I_{sc} = 0.37 A

$$I_O = \frac{V_O\ R2 + 0.6\ (R2 + R3)}{R1\ R3}$$

FIGURE 11 – 6.0-VOLT, 5.0-AMPERE HIGH EFFICIENCY REGULATOR



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TYPICAL APPLICATIONS (continued)

FIGURE 12 – CURRENT BYPASS
(Load current range, 400-to-500 mA)

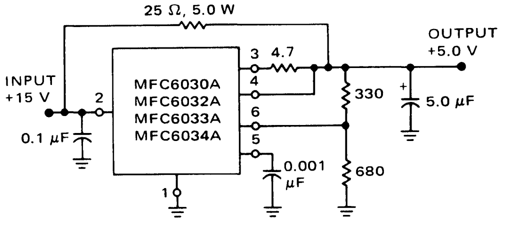


FIGURE 15 – VOLTAGE BOOSTED 40-VOLT, 100 mA REGULATOR
(with short-circuit current limiting)

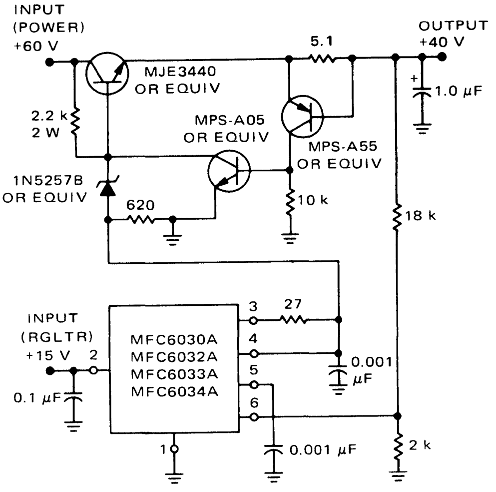
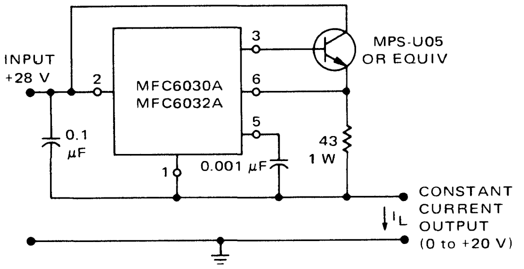
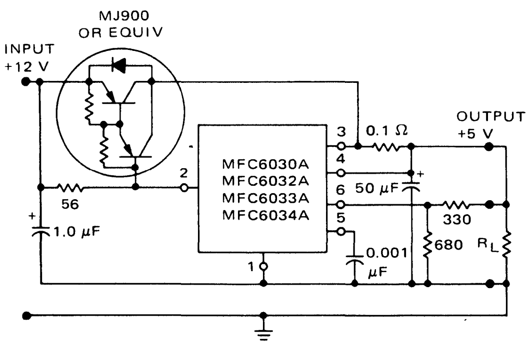


FIGURE 13 – 100 mA CONSTANT CURRENT SOURCE



Pin 4 not connected

FIGURE 14 – 5.0-VOLT, 5.0-AMPERE REGULATOR with REMOTE SENSING, PNP CURRENT BOOST



MFC6040

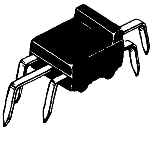
ELECTRONIC ATTENUATOR

ELECTRONIC ATTENUATOR

- Designed for use in:
  - DC Operated Volume Control
  - Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 6-Lead Plastic Package

ELECTRONIC ATTENUATOR

Silicon Monolithic Integrated Circuit



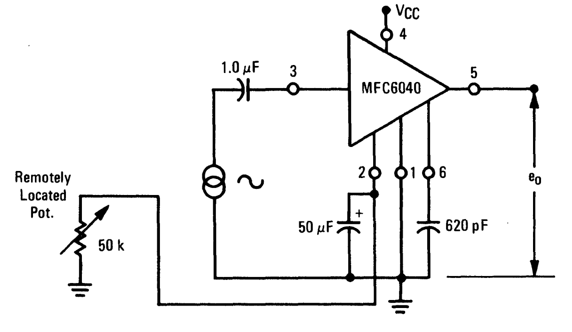
CASE 643A

PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	20	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation) Derate above T_A = 25°C	1.0 10	Watt mW/°C
Operating Temperature Range	0 to +75	°C

FIGURE 1 – TYPICAL DC "REMOTE" VOLUME CONTROL



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (e_{in} = 100 mV (RMS), f = 1.0 kHz, R1 = 0, V_{CC} = 16 Vdc, T_A = +25°C unless otherwise noted.)

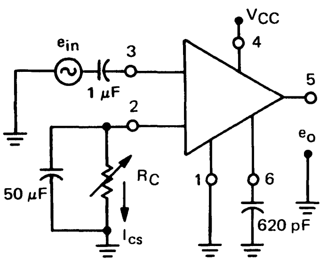
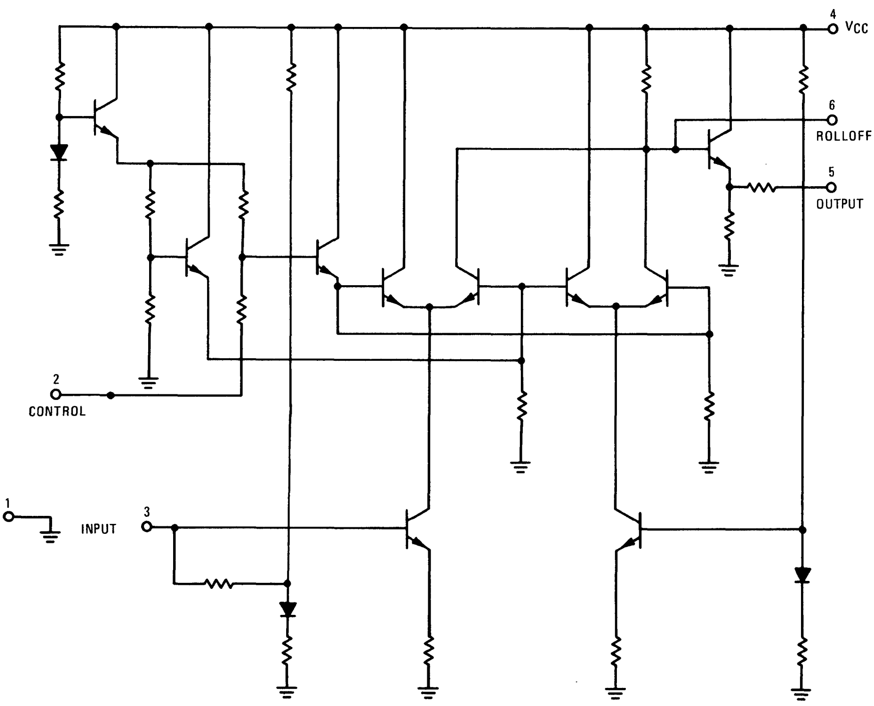
Circuit	Characteristic	Min	Typ	Max	Unit
	Operating Power Supply Voltage	9.0	–	18	Vdc
	Control Terminal Sink Current (e_{in} = 0)	–	–	2.0	mAdc
	Maximum Input Voltage	–	–	0.5	V(RMS)
	Voltage Gain	11	13	–	dB
	Attenuation Range (R_C = 33 k ohms)	70	90	–	dB
	Total Harmonic Distortion (Pin 2 Gnd) (e_{in} = 100 mV (RMS), e_o = A_v x e_{in})	–	0.6	1.0	%

FIGURE 2 – CIRCUIT SCHEMATIC



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TYPICAL ELECTRICAL CHARACTERISTICS

(V_{CC} = 16 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – ATTENUATION versus DC CONTROL VOLTAGE

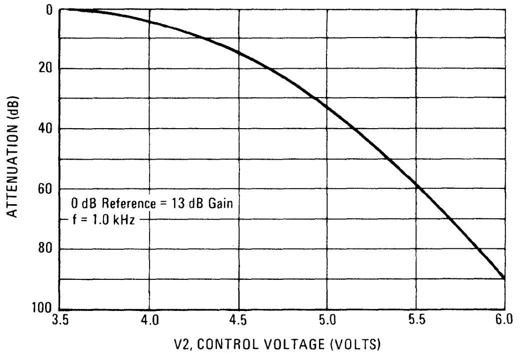


FIGURE 4 – ATTENUATION versus CONTROL RESISTOR

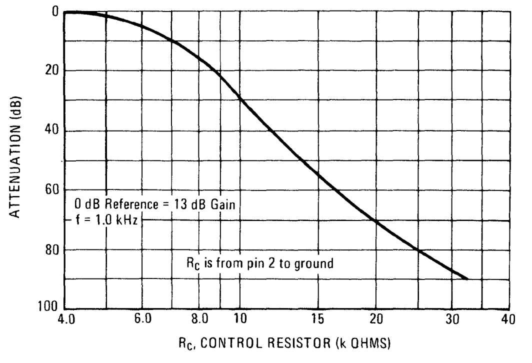


FIGURE 5 – FREQUENCY RESPONSE

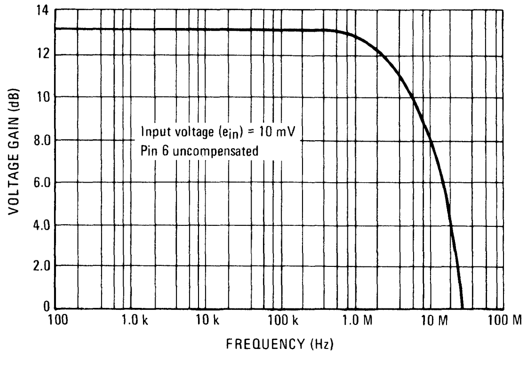


FIGURE 6 – OUTPUT VOLTAGE SWING

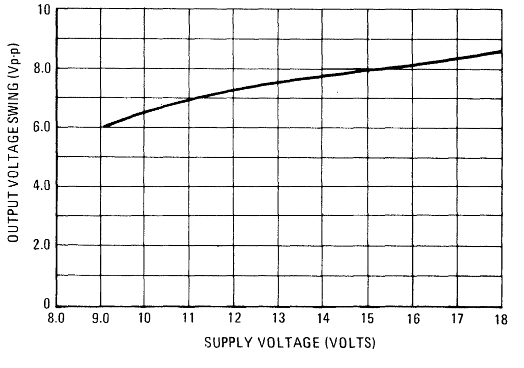
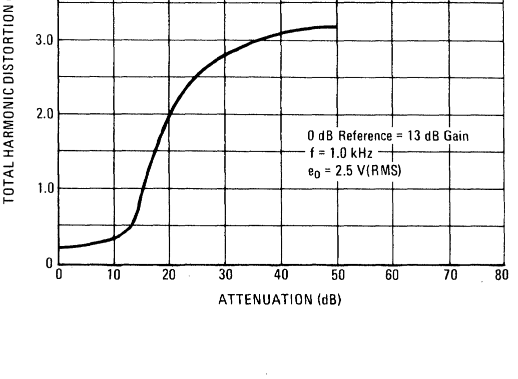


FIGURE 7 – TOTAL HARMONIC DISTORTION



8

MFC6050

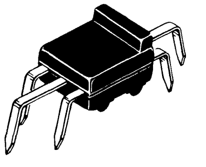
DUAL TOGGLE FLIP-FLOP

DUAL TOGGLE FLIP-FLOP WITH RESET

- Wide Operating Voltage Range – 6.0 to 16 Volts
- Regulated Supply Not Required
- Ideal for Remote Control Applications
- Economical 6-Lead Plastic Package
- Reset (R) Available to Set Output to 0 Regardless of Previous History

DUAL TOGGLE FLIP-FLOP WITH RESET

Silicon Monolithic Functional Circuit

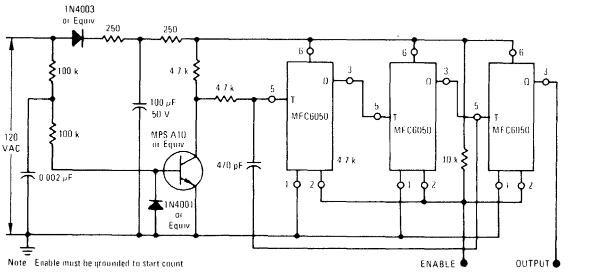


CASE 643A
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

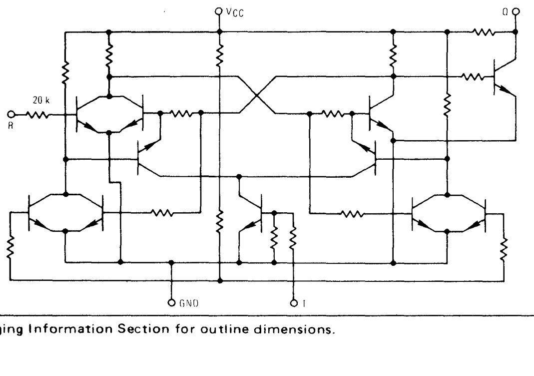
Rating	Value	Volts
Power Supply Voltage	19	Vdc
Output Sinking Current	15	mA
Negative Input Voltage	0.5	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	1.0 10	Watt mW/°C
Operating Temperature Range	+10 to +75	°C

TYPICAL APPLICATION – DIVIDE-BY-60 COUNTER

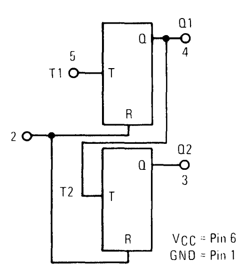


SIMPLIFIED CIRCUIT SCHEMATIC

(One-Half of Circuit Shown)



BLOCK DIAGRAM



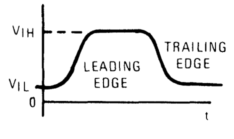
See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, V_{in} = 4.0 V, Square Pulse, f = 10 kHz, 50% Duty Cycle, t_{PHL} = 1.0 V/µs (Min), T_A = +25°C unless otherwise noted.)

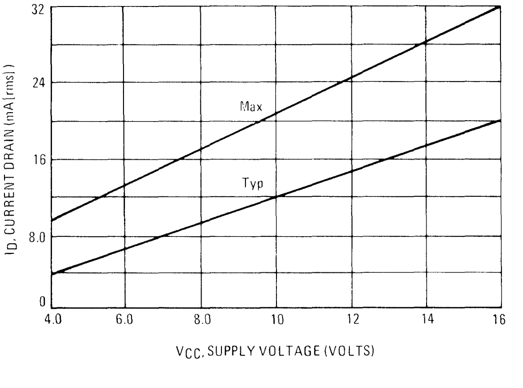
Characteristic		Min	Typ	Max	Unit
Operating Power Supply Voltage		6.0	–	16	Vdc
Toggle Frequency		–	3.0	–	MHz
Output Voltage (High)					Vdc
(V_{CC} = 6.0 Vdc)	Q1	3.7	–	–	
	Q2	5.5	–	–	
(V_{CC} = 16 Vdc)	Q1	10	–	–	
	Q2	15.5	–	–	
Output Voltage (Low)					Vdc
(V_{CC} = 6.0 Vdc)		–	–	0.5	
(V_{CC} = 16 Vdc)		–	–	1.0	
Operating Drain Current		–	–	32	mAdc
Output Sinking Current ($V_O \leqslant$ 1.0 Vdc)		–	8.0	–	mAdc
Rise Time		–	250	–	ns
Storage Time		–	350	–	ns
Fall Time		–	60	–	ns
Input Resistance		10	–	–	kΩ
Output Resistance (Output High)		–	–	6.0	kΩ

INPUT PULSE REQUIREMENTS



Characteristic	Symbol	Min	Max	Unit
Pulse Magnitude	V_{IH}	+4.0	–	Volts
Zero Level	V_{IL}	–	+1.0	Volts
Leading Edge	–	+0.1	–	V/µs
Trailing Edge	$\frac{dv}{dt}$	-1.0	–	$\frac{Volts}{µs}$

FIGURE 2 – RMS CURRENT DRAIN versus SUPPLY VOLTAGE



8

MFC6070

AUDIO POWER AMPLIFIER

1-WATT AUDIO POWER AMPLIFIER

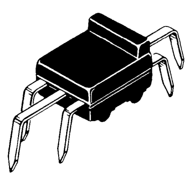
. . . designed primarily for low-cost audio amplifiers in phonograph, TV and radio applications.

- 100 mV Sensitivity for 1-Watt*
- Low Distortion — 1% @ 1-Watt typ*
- Short-Circuit Proof — Short Term (10 seconds typ)
- No Heatsink Required for 1-Watt Output at T_A = 55°C**
- Excellent Hum Rejection

*Circuit Dependent
**Voltage Dependent

1-WATT AUDIO POWER AMPLIFIER

Silicon Monolithic Functional Circuit



CASE 643A
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	20	Vdc
Power Dissipation Derate above T_A = +25°C	P_D $1/\theta_{JA}$	1.0 8.0	Watt mW/°C
Operating Temperature Range	T_A	-10 to +55	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

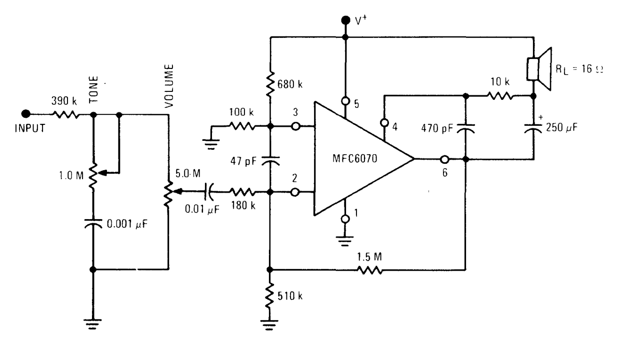
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}*	125	°C/W

*Thermal resistance is measured in still air with fine wires connected to the leads, representing the "worst case" situation.

For a larger power requirement, pin 1 must be soldered to at least one sq. in. of copper foil on the printed circuit board. The θ_{JA} will be no greater than +90°C/W. Thus, 1.39 Watts could be dissipated at +25°C, which must be linearly derated at 11.1 mW/°C from +25°C to +150°C.

FIGURE 1 — TYPICAL 1-WATT PHONOGRAPH AMPLIFIER (Ceramic cartridge input)



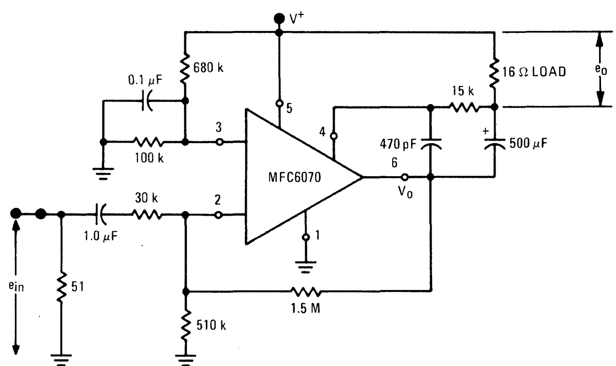
See Packaging Information Section for outline dimensions.

8

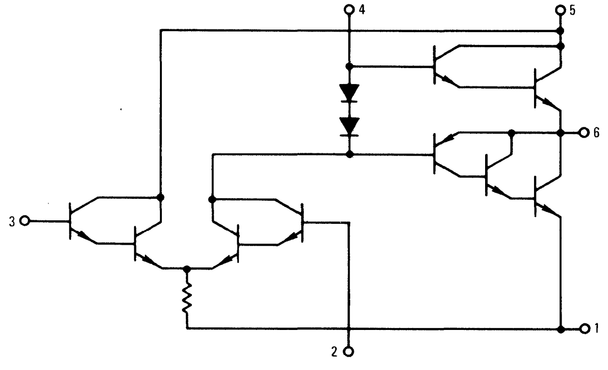
ELECTRICAL CHARACTERISTICS (V^+ = 16 Vdc, See Figure 2 for test circuit, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Quiescent Output Voltage	V_O	–	8.0	–	Vdc
Quiescent Drain Current (e_{in} = 0)	I_D	–	5.0	18	mA
Sensitivity, Input Voltage (e_{in} adjusted for e_o = 4.0 V(rms) @ 1.0 kHz, Power Output = 1.0 Watt)	e_{in}	–	100	150	mV
Total Harmonic Distortion (e_o = 4.0 V(rms) @ 1.0 kHz, Power Output = 1.0 Watt) (e_{in} adjusted for e_o = 1.26 V(rms) @ 1.0 kHz, Power Output = 100 mW)	THD	 – –	 1.0 1.0	 10 3.0	%
Hum and Noise (IHF Standard A201, 1966)	–	–	-40	–	dB

FIGURE 2 – 1-WATT AUDIO POWER AMPLIFIER TEST CIRCUIT



Circuit Schematic



8

TYPICAL CHARACTERISTICS

(V^+ = 16 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 — TOTAL HARMONIC DISTORTION versus OUTPUT POWER

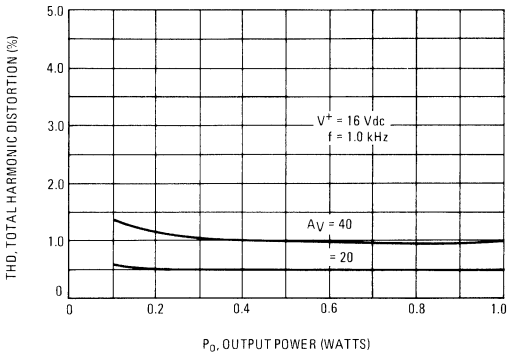


FIGURE 4 — POWER DISSIPATION versus OUTPUT POWER

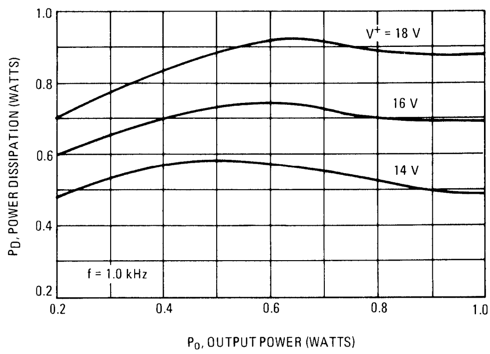
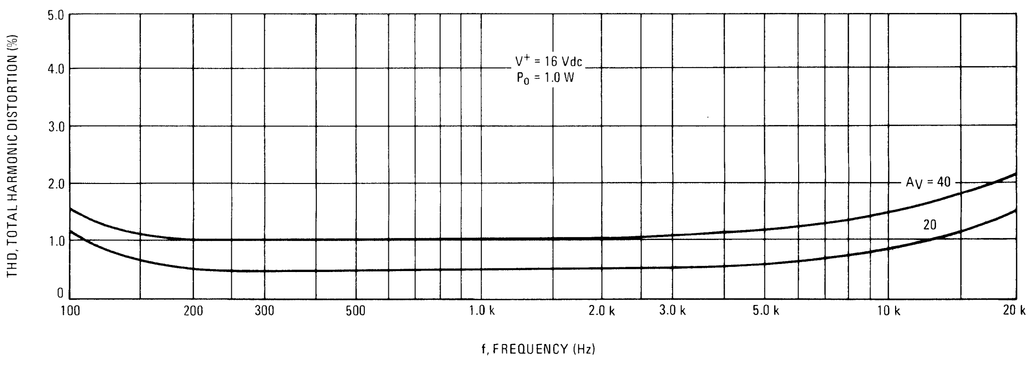


FIGURE 5 — TOTAL HARMONIC DISTORTION versus FREQUENCY



APPLICATIONS INFORMATION

Shown in Figures 7 and 11 are low cost 1 W phono amplifiers with a sensitivity (@ 1 kHz) of approximately 450 mV. The input impedance of both amplifiers is approximately equal to R4 and the gain is determined by (R7 + R10)/R5. To change the gain of the amplifier, change the value of R5 and hold (R7 + R10) between 1 M and 2.2 M. This allows the use of a small and less expensive capacitor for C2.

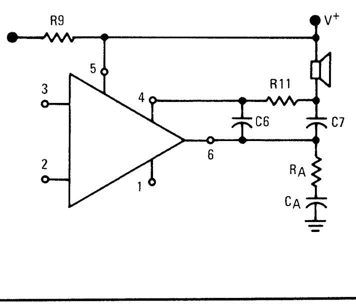
The bass boost effect shown in the frequency response curves (Figures 10 and 14) is provided by the parallel combination of C4 and R10 and can be eliminated by removing C4 and replacing (R7 + R10) with a 2.2 Megohm resistor. High frequency compensation is provided by C6 and the low frequency roll-off is determined by the impedance network of C2 and R5, C3 and R4, and C8 and the speaker. The series combination of R_A and C_A from pin 6 to ground may be required for stability, depending on printed circuit board layout, speaker reactance, and lead lengths.

Device ac short-circuit capability was tested in both the 8-ohm and 16-ohm amplifiers by shorting pin 6 thru a 500 microfarad capacitor to ground for a period of ten seconds with the amplifier operating at full rated output.

The speaker can be connected to V^+ (alternate connection shown below) or ground (Figures 7 and 11). Printed circuit board art work is shown for both systems in Figures 16 and 18. A picture of the completed board for the grounded speaker system is shown in Figure 21.

ALTERNATE CONNECTION FOR SPEAKER TO V^+

(See Figure 20 for Parts List)



8

APPLICATIONS INFORMATION (continued)

(R_L = 8.0 ohms, T_A = +25°C unless otherwise noted)

FIGURE 6 – POWER SUPPLY

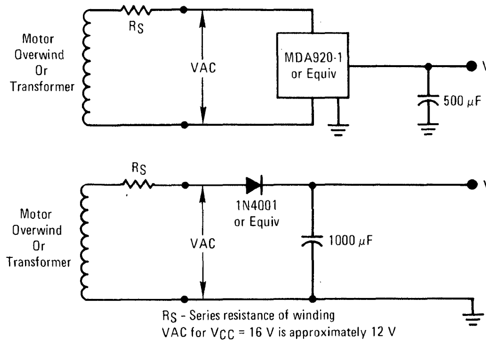


FIGURE 7 – PHONOGRAPH AMPLIFIER 1 WATT - 8 OHM
(See Figure 15 for Parts List)

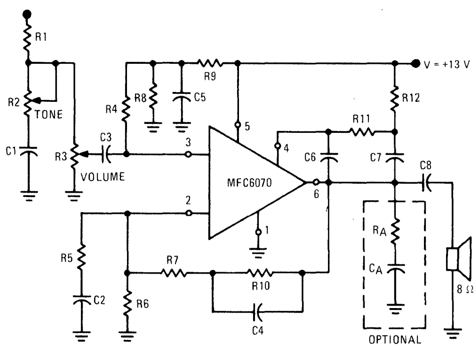


FIGURE 8 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER FOR FIGURE 7

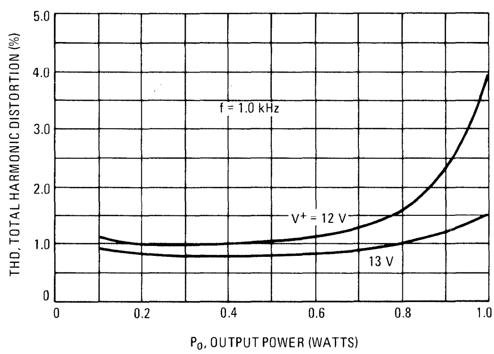


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY FOR FIGURE 7

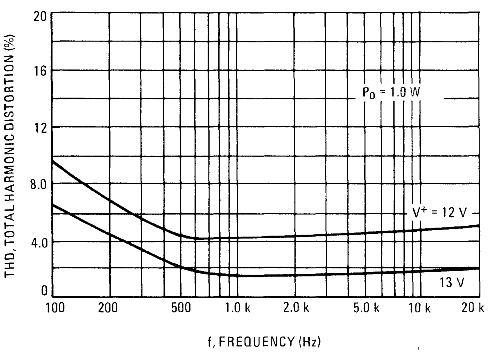
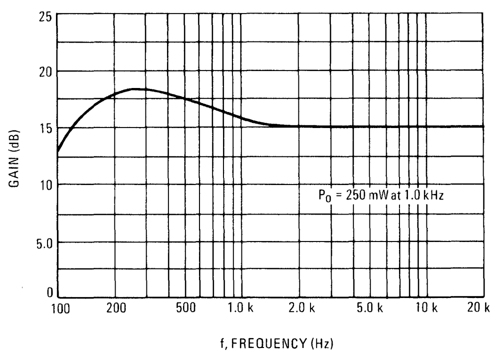


FIGURE 10 – FREQUENCY RESPONSE FOR FIGURE 7



8

APPLICATIONS INFORMATION (continued)

(R_L = 16 ohms, T_A = +25°C unless otherwise noted)

FIGURE 11 – 1.0 WATT, 16 OHM LOAD PHONOGRAPH AMPLIFIER
(See Figure 15 for Parts List)

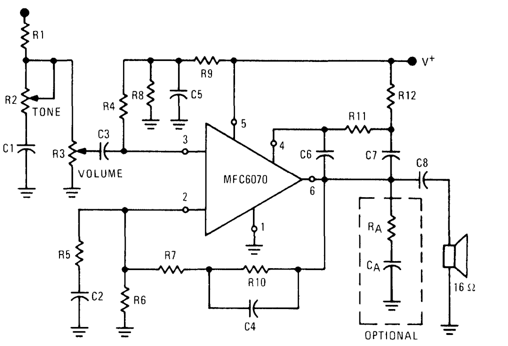


FIGURE 12 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER FOR FIGURE 11

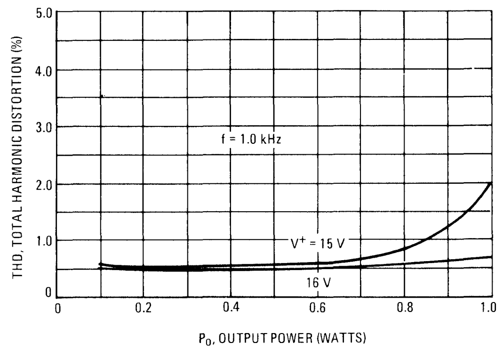


FIGURE 13 – TOTAL HARMONIC DISTORTION versus FREQUENCY FOR FIGURE 11

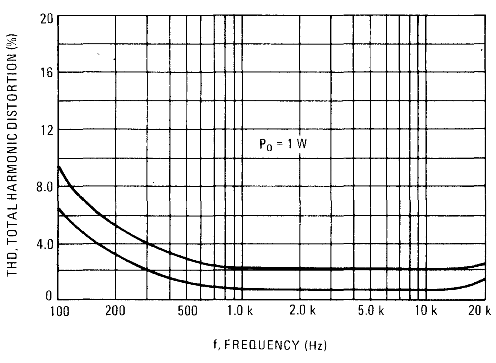


FIGURE 14 – FREQUENCY RESPONSE FOR FIGURE 11

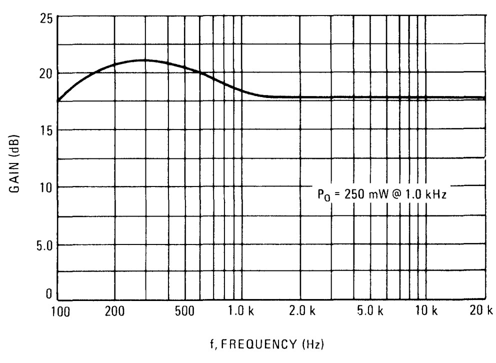


FIGURE 15 – PARTS LIST FOR FIGURES 7 AND 11

R1 = 180 k ohms	R9 = 1.0 Megohm	C3 = 0.05 μF
R2 = 5.0 Megohms	R10 = 1.5 Megohms	C4 = 470 pF
R3 = 5.0 Megohms	R11 = 6.8 k ohms	C5 = 0.1 μF
R4 = 1.0 Megohm	R12 = 6.8 k ohms	C6 = 470 pF
R5 = 150 k ohms*	R_A = 10 ohms**	C7 = 0.1 μF
R6 = 910 k ohms*	C1 = 470 pF	C8 = 500 μF*
R7 = 680 k ohms	C2 = 0.1 μF	C_A = 0.1 μF**
R8 = 180 k ohms		

*For Figure 11 (16-ohm load) change R5 to 100 k ohms, R6 to 820 k ohms and C8 to 250 μF.

**Optional – Not included on board. (See Applications Information Note)

8

APPLICATIONS INFORMATION (continued)

FIGURE 16 – PRINTED CIRCUIT BOARD (Foil Side)
(Speaker Grounded)

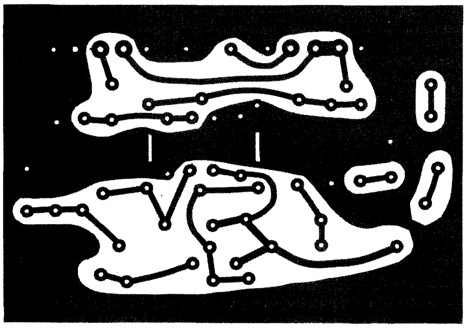


FIGURE 17 – COMPONENT DIAGRAM FOR FIGURE 16

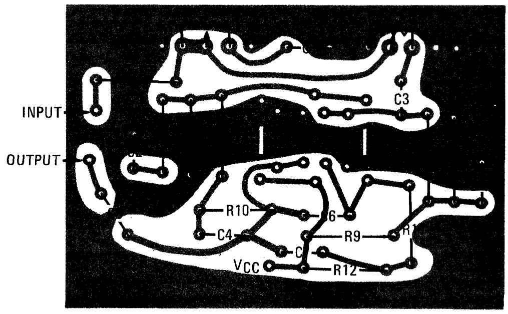


FIGURE 18 – PRINTED CIRCUIT BOARD (Foil Side)
(Speaker to V+)

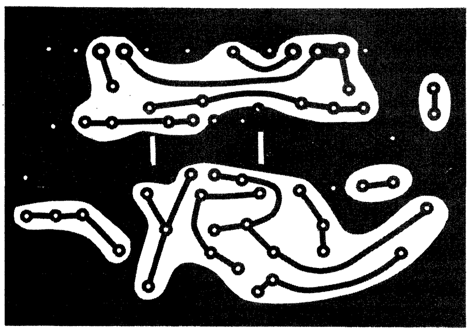


FIGURE 19 – COMPONENT DIAGRAM FOR FIGURE 18

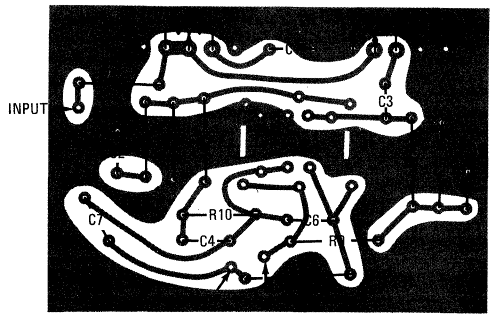


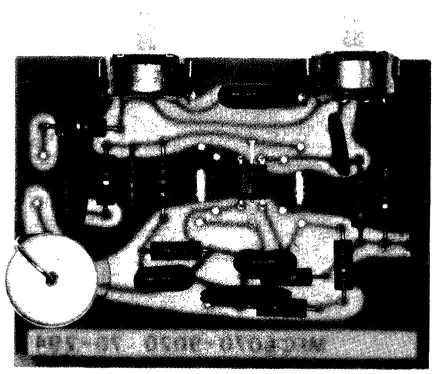
FIGURE 20 – PARTS LIST FOR FIGURE 19
(See Applications Information Note)

R1 = 180 k ohms
R2,R3 = 5.0 Megohms
R4,R9 = 1.0 Megohm
R5 = 82 k ohms
R6 = 820 k ohms
R7 = 680 k ohms
R8 = 180 k ohms
R10 = 1.5 Megohms
R11 = 15 k ohms
R_A = 10 ohms*

C1,C4,C6 = 470 pF
C2,C5 = 0.1 μF
C3 = 0.05 μF
C7 = 250 μF
C_A = 0.1 μF*

*Optional - Not included on board. (See Applications Information Note)

FIGURE 21 – COMPLETED BOARD
(Speaker Grounded)



8

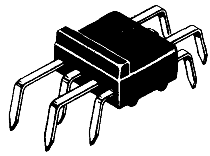
MFC8020A
MFC8021A
MFC8022A

CLASS B AUDIO DRIVERS

. . . designed as preamplifiers and driver circuits for complementary output transistors.

- Driver for Auto Radios – and up to 20-Watt Amplifiers
- High Gain – 7.0 mV for 1.0 Watt, R_L = 3.2 Ohms
- High Input Impedance – 500-Kilohm Capability
- Output Biasing Diodes Included
- No Special h_{FE} Matching of Outputs Required

CLASS B AUDIO DRIVERS
SILICON MONOLITHIC
FUNCTIONAL CIRCUITS



CASE 644A
PLASTIC PACKAGE

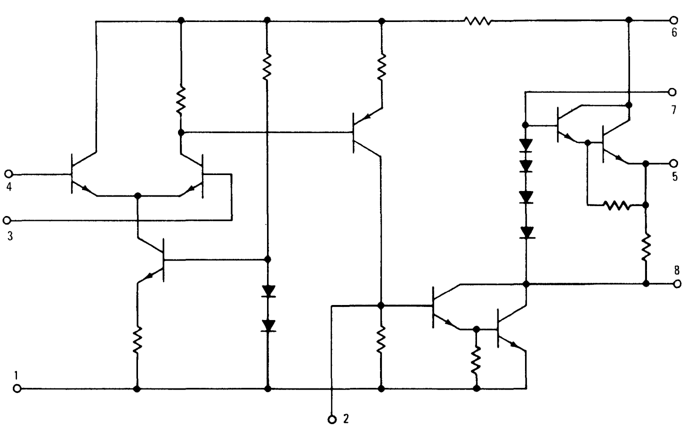
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value MFC8020A	MFC8021A	MFC8022A	Unit
Power Supply Voltage	35	20	45	Vdc
Power Dissipation Derate above T_A = +25°C	1.0 10	1.0 10	1.0 10	Watt mW/°C
Peak Output Current (pins 5 & 8)	150	150	150	mA
Operating Temperature Range	-10 to +75	-10 to +75	-10 to +75	°C
Storage Temperature Range	-55 to +125	-55 to +125	-55 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Value	Unit
Thermal Resistance	100	°C/W
Junction Temperature	125	°C

FIGURE 1 – CIRCUIT SCHEMATIC

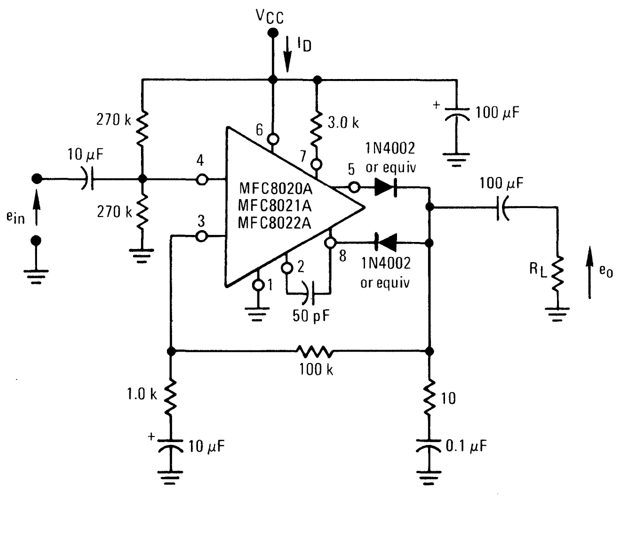


See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted) (See Figure 2)

Characteristic		Min	Typ	Max	Unit
Drain Current (e_{in} = 0)					mA
V_{CC} = 30 Vdc	MFC8020A	–	10	30	
V_{CC} = 14 Vdc	MFC8021A	–	7.0	30	
V_{CC} = 40 Vdc	MFC8022A	–	12	30	
Sensitivity (P_O = 1.0 Watt, f = 1.0 kHz)					mV
e_o = 8.95 V(RMS), R_L = 165 Ω	MFC8020A	–	89	112	
e_o = 3.2 V(RMS), R_L = 65 Ω	MFC8021A	–	32	40	
e_o = 12.65 V(RMS), R_L = 165 Ω	MFC8022A	–	126	160	
Total Harmonic Distortion (f = 1.0 kHz)					%
V_{CC} = 30 V, e_o = 8.95V(RMS), R_L = 165 Ω	MFC8020A	–	0.7	5.0	
V_{CC} = 14 V, e_o = 3.2V(RMS), R_L = 65 Ω	MFC8021A	–	1.0	5.0	
V_{CC} = 40 V, e_o = 12.65 V(RMS), R_L = 165 Ω	MFC8022A	–	1.5	5.0	
Open-Loop Gain					dB
V_{CC} = 30 V, R_L = 165 Ω	MFC8020A	–	89	–	
V_{CC} = 14 V, R_L = 65 Ω	MFC8021A	–	87	–	
V_{CC} = 40 V, R_L = 165 Ω	MFC8022A	–	90	–	
Ripple Rejection f = 60 Hz, A_V ≐ 100, e_{in} = 0, Power Supply Ripple = 1.0 V(RMS)		–	27	–	dB
Equivalent Input Noise e_{in} = 0, R_S = 1.0 k Ω, BW = 100 Hz – 10 kHz		–	18	–	μV
Quiescent Output Voltage (e_{in} = 0)					Vdc
V_{CC} = 30 V	MFC8020A	–	15	–	
V_{CC} = 14 V	MFC8021A	–	7.0	–	
V_{CC} = 40 V	MFC8022A	–	20	–	

FIGURE 2 – TEST CIRCUIT



8

TYPICAL AUTO RADIO AUDIO APPLICATION and CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 3 – APPLICATION CIRCUIT FOR MFC8021A

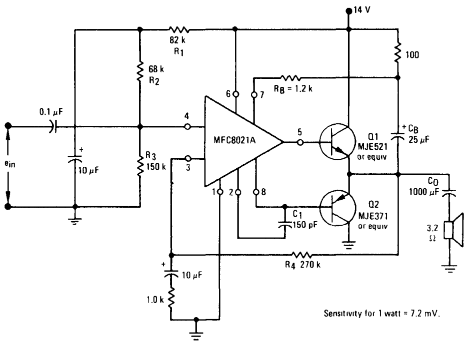


FIGURE 4 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER

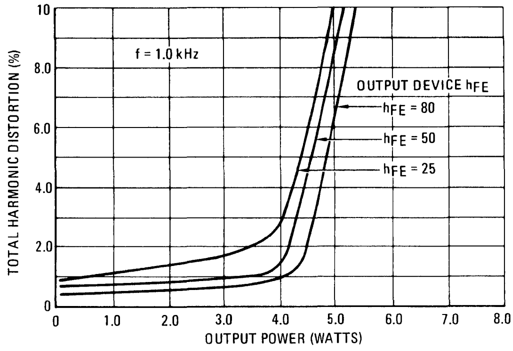


FIGURE 5 – TOTAL HARMONIC DISTORTION versus FREQUENCY

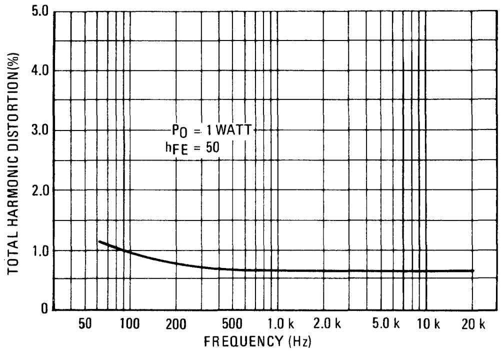
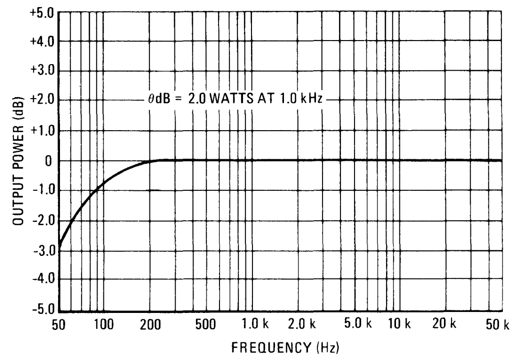


FIGURE 6 – FREQUENCY RESPONSE

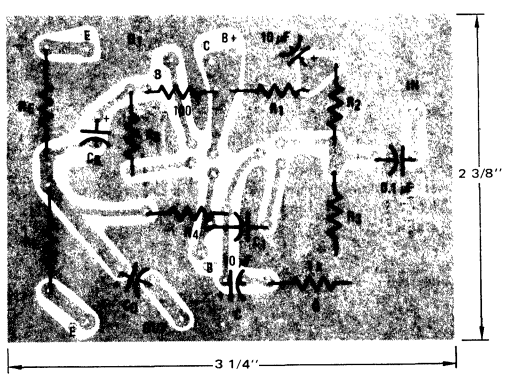


APPLICATIONS INFORMATION for MFC8021A (AUTO RADIO AUDIO)

The MFC8021A combines all the voltage gain required for an automotive radio audio amplifier into one package reducing the circuit-board area requirement. The circuit shown in Figure 3 has an input sensitivity of approximately 7.2 millivolts for a one-watt output. Sensitivity can be adjusted by changing the value of R_4. The circuit performance is a function of the output device h_{FE}, as shown in Figure 4. Figure 4 can be used to determine the minimum h_{FE} of the output transistors. The bandwidth of the amplifier is determined by the capacitor, C_1. If C_1 is increased to 390 pF the high frequency 3.0 dB point is typically 20 kHz.

An illustration of the copper side of the printed-circuit board layout is shown in Figure 7. The output transistors are mounted on the heatsink which for auto radio audio applications should have a maximum thermal resistance of 18°C/W for each device or 9.0°C/W when both output transistors are mounted on the same heatsink.

FIGURE 7 – PRINTED CIRCUIT BOARD for AUTOMOTIVE RADIO AUDIO 10-and-20 WATT AMPLIFIERS (COPPER SIDE)



8

TYPICAL 10-and-20 WATT AMPLIFIER APPLICATION AND CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 8 – APPLICATION CIRCUIT for MFC8020A/and MFC8022A

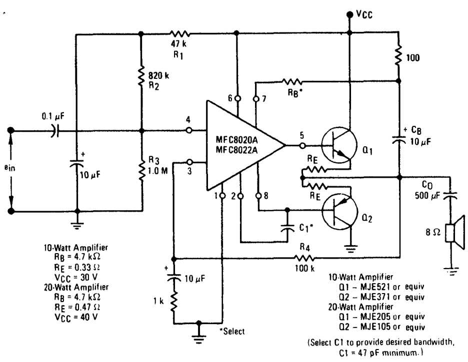


FIGURE 9 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER

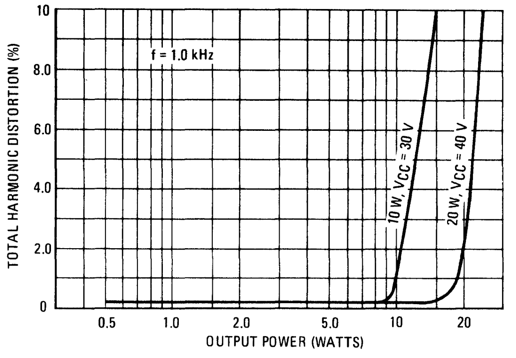


FIGURE 10 – TOTAL HARMONIC DISTORTION versus FREQUENCY

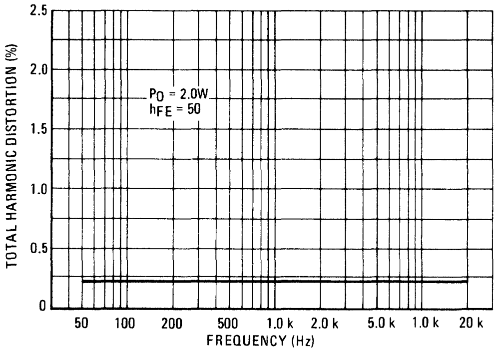
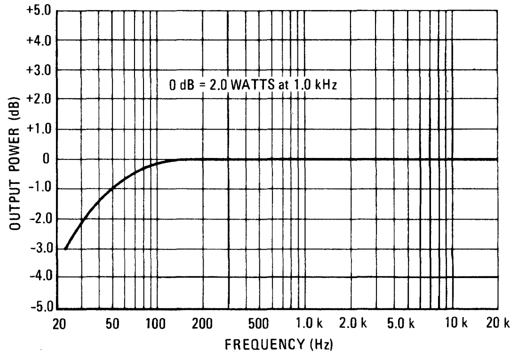


FIGURE 11 – FREQUENCY RESPONSE



APPLICATIONS INFORMATION for MFC8020A and MFC8022A (10-Watt and 20-Watt Amplifiers)

8

The MFC8020A and MFC8022A are high-voltage parts capable of driving 10-to-20 watt audio amplifiers. The gain of the circuit shown in Figure 8 changes when the value of R_4 is varied and the bandwidth is determined by C_1. Emitter resistors are required at the higher voltages used for 10-to-20 watt audio amplifiers to provide thermal stability. The value of R_E is a function of the heatsink thermal resistance and supply voltage. The heatsink requirements for operation at +65°C (with both devices mounted on the same heatsink) is about 14°C/W for the 10-watt amplifier and 8.0°C/W for the 20-watt amplifier. If the maximum ambient operating temperature is reduced then the heatsink can be reduced in size as calculated by

$$\theta_{SA} = \frac{T_J - (\theta_{JS})\,P_D - T_A}{P_D}$$

where

θ_{SA} = Heatsink thermal resistance

T_J = Maximum junction operating temperature

θ_{JS} = Junction to heatsink thermal resistance (includes all surface interface components for thermal resistance such as the insulating washer)

P_D = Maximum power dissipation of transistors (This occurs at about 60% of maximum output power) 6.0 W for 10 W, 7.2 W for 12 W

T_A = Maximum ambient temperature

The printed circuit board layout is shown in Figure 7.

MFC8030

HIGH FREQUENCY CIRCUIT

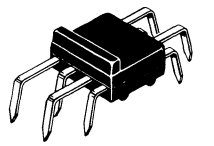
DIFFERENTIAL/CASCODE AMPLIFIER

. . . designed for applications requiring differential or cascode amplifiers.

- Extremely Flexible Amplifier
- Diode Available for Biasing
- Economical 8-Staggered Lead Package

DIFFERENTIAL/CASCODE AMPLIFIER

Silicon Monolithic Functional Circuit

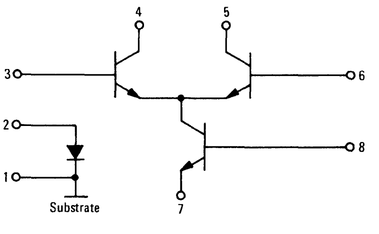


CASE 644A
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

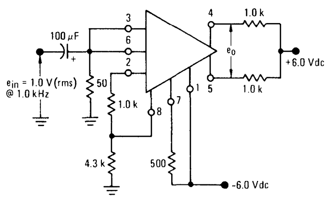
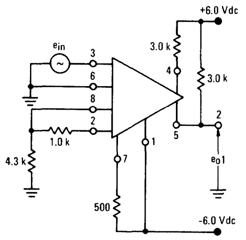
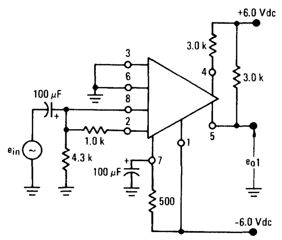
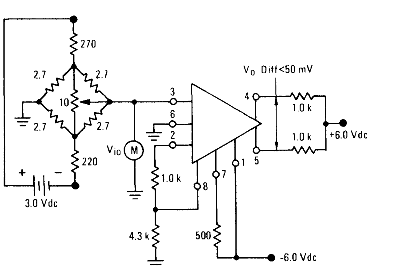
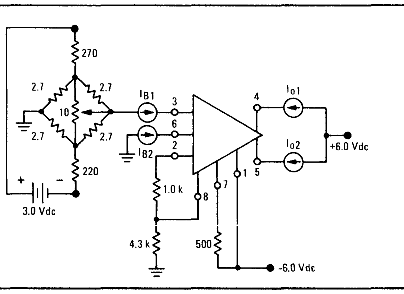
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	20	Vdc
Differential Input Voltage	V_{in}	±5.0	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation)	P_D	1.0	Watt
Derate above 25°C	$1/\theta_{JA}$	10	mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

FIGURE 1 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Circuit	Characteristic	Symbol	Min	Typ	Max	Unit
	AC Common-Mode Rejection $e_{4\text{-}5} = e_o$ $CMR = 20 \log \frac{(e_{in})}{(e_o)}$	CMR_{AC}	–	35	–	dB
	Differential-Mode Voltage Gain $A_V \text{ Diff} = 20 \log \frac{(e_{o1})}{(e_{in})}$ (e_{in} = 1.0 kHz, 1.0 mV[rms]) (e_{in} = 10 MHz, 1.0 mV[rms]) (e_{in} = 50 MHz, 1.0 mV[rms])	$A_{V(dif)}$	 – – –	 32 26 10	 – – –	dB
	Cascode-Mode Voltage Gain $A_V \text{ Cascode} = 20 \log \frac{(e_{o1})}{(e_{in})}$ (e_{in} = 1.0 kHz, 1.0 mV[rms]) (e_{in} = 10 MHz, 1.0 mV[rms]) (e_{in} = 50 MHz, 1.0 mV[rms])	$A_{V(cscd)}$	 – – –	 36 31.5 15	 – – –	dB
	Input Offset Voltage	V_{io}	–	5.0	10	mV
	DC Current Gain Match ($I_{01} = I_{02}$)	$\frac{h_{FE1}}{h_{FE2}}$	0.8	–	1.1	–

8

MFC8040

AUDIO PREAMPLIFIER

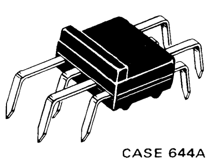
LOW NOISE AUDIO PREAMPLIFIER

. . . designed for high-gain, low-noise applications.

- Special Monolithic "State-of-the-Art" Process to Insure Low Noise – 1.0 μV (Typ)
- Can be Externally Equalized for NAB, RIAA
- Low Distortion – 0.1% (Typ) @ A_V = 100
- Large Dynamic Range – 7.0 V(rms) Out
- Low Output Impedance – 100 Ohms (Max)

LOW NOISE AUDIO PREAMPLIFIER

Silicon Monolithic Functional Circuit

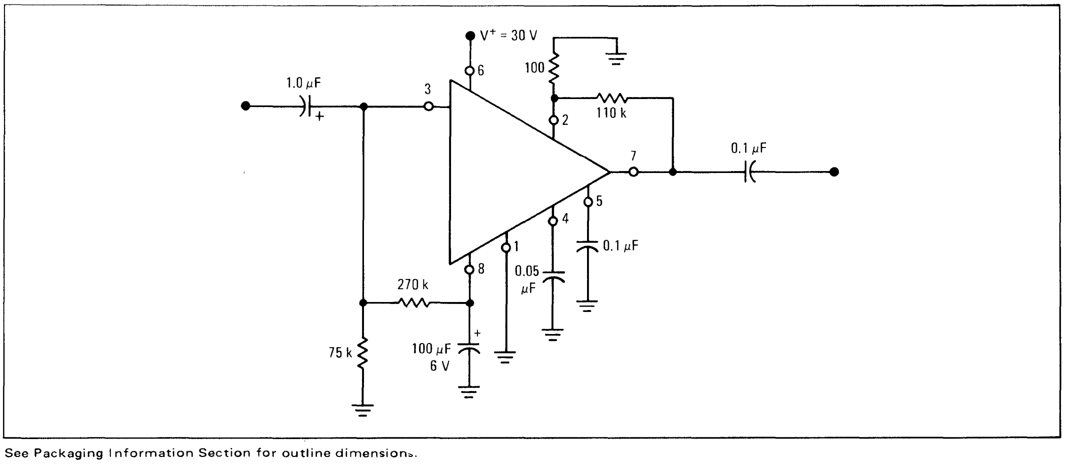


CASE 644A
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	33	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation)	P_D	1.0	Watt
Derate above T_A = 25°C	$1/\theta_{JA}$	10	mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

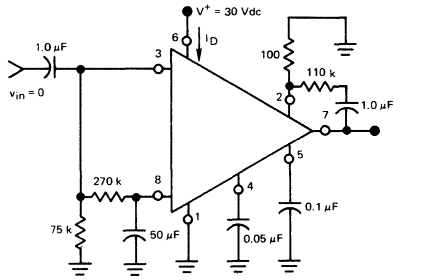
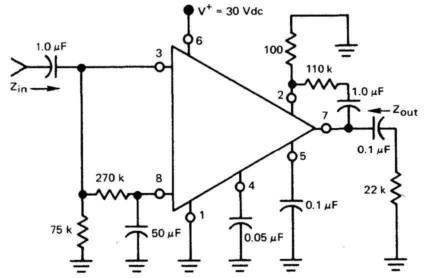
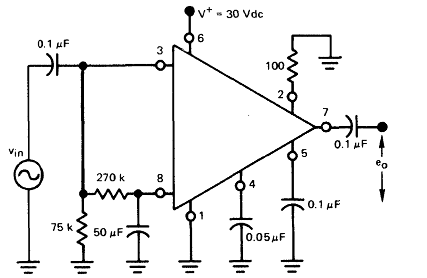
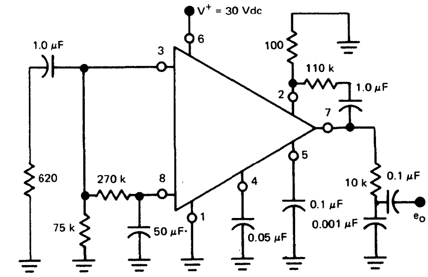
FIGURE 1 – TYPICAL WIDEBAND AMPLIFIER CIRCUIT (A_V = 60 dB)



See Packaging Information Section for outline dimensions.

8

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Circuit	Characteristic	Symbol	Min	Typ	Max	Unit
	Drain Current	I_D	–	8.0	12	mA
	Total Harmonic Distortion (v_O = 1.0 V, f = 1.0 kHz)	THD	–	<0.1	0.25	%
	Input Impedance	Z_{in}	–	75	–	k ohms
	Output Impedance	Z_{out}	–	100	–	ohms
	Open Loop Voltage Gain (v_{in} = 100 µV(rms) @ f = 1.0 kHz)	A_{VOL}	80	–	–	dB
	Wideband Input Noise (–3.0 dB Bandwidth, 10 Hz to 16 kHz, A_V = 60 dB @ 1.0 kHz, $\left(e_n = \frac{e_o}{A_V}\right)$	e_n	–	1.0	3.0	µV (rms)

8

FIGURE 2 – CIRCUIT SCHEMATIC

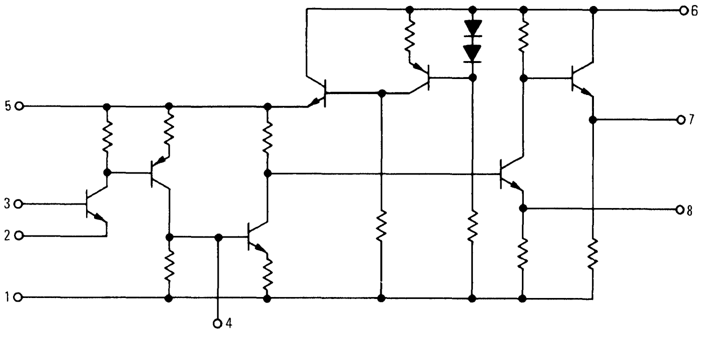


FIGURE 3 – INPUT NOISE

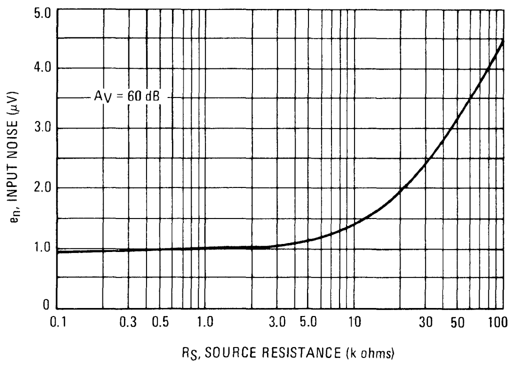


FIGURE 4 – OPEN LOOP TOTAL HARMONIC DISTORTION

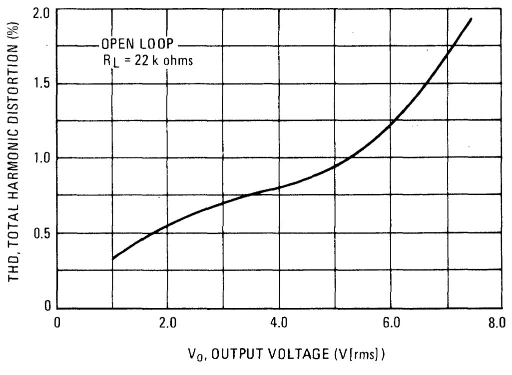
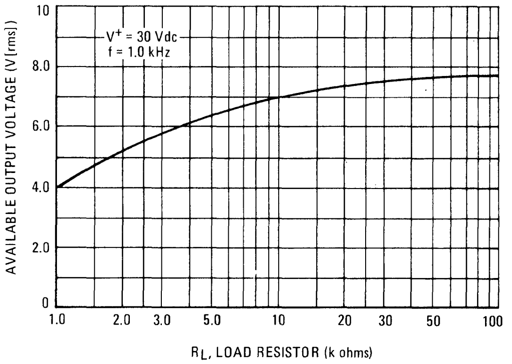


FIGURE 5 – AVAILABLE OUTPUT VOLTAGE



ZERO VOLTAGE SWITCH

MFC8070

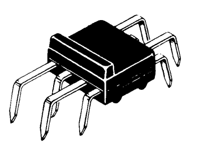
ZERO VOLTAGE SWITCH

. . . designed for use in ac power switching applications with output drive capable of triggering triacs. Other operational features include; (1) a built-in voltage regulator that allows direct ac line operation, (2) a differential input with dual sensor inputs capable of testing the condition of two external sensors and controlling the gate pulse to a triac accordingly; (hysteresis or proportional control to this section may be added if desired) (3) sensor input "open and short" protection; this insures that the triac will never be turned "on" if either of the inputs are shorted or opened (4) a zero crossing detector that synchronizes the triac gate pulses with the zero crossing of the ac line voltage. This eliminates radio frequency interference (RFI) when used with resistive loads.

- Heater Controls
- Photo Controls
- Threshold Detector
- Lamp Driver
- Valve Control
- On-Off Power Controls
- Relay Driver
- Flasher Control

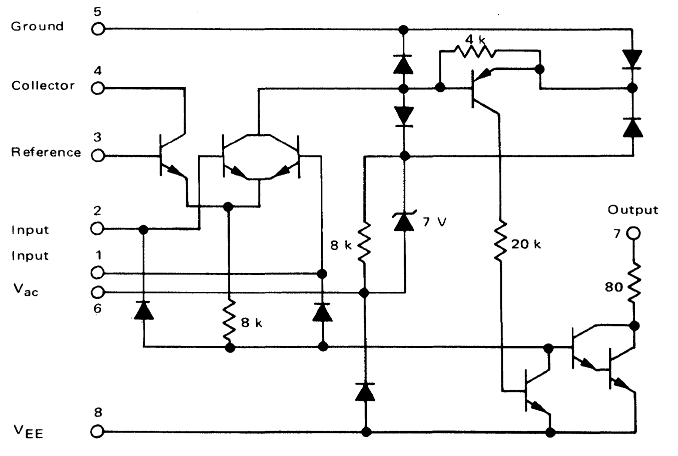
ZERO VOLTAGE SWITCH

SILICON MONOLITHIC FUNCTIONAL CIRCUIT



CASE 644A
PLASTIC PACKAGE

FIGURE 1 – CIRCUIT SCHEMATIC



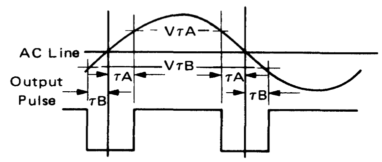
See Packaging Information Section for outline dimensions.

8

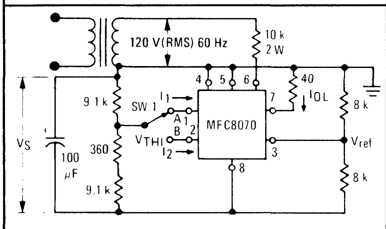
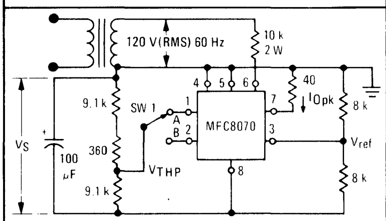
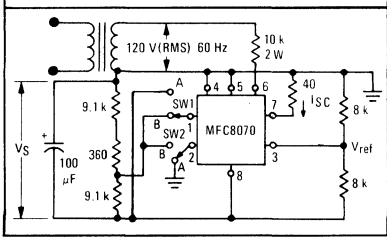
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
DC Voltage	$V_{5\text{-}8}$	15	Vdc
DC Voltage	$V_{4\text{-}8}$	15	Vdc
DC Voltage	$V_{7\text{-}8}$	15	Vdc
Peak Supply Current	I_6	35	mA
Power Dissipation Derate above T_A = +25°C	P_D $1/\theta_{JA}$	1.0 10	Watt mW/°C
Operating Temperature Range	T_A	-10 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

FIGURE 2 – OUTPUT PULSE DEFINITION



ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	V_S with Inhibit Output (Sw 1: A or B)	V_{SIO}	–	9.0	11	Vdc
	Output Leakage Current (Sw 1: A or B)	I_{OL}	–	5.0	100	μA
	Input Current 1 (Sw 1: A)	I_1	–	5.0	15	μA
	Input Current 2 (Sw 1: B)	I_2	–	5.0	15	μA
	Inhibit Threshold Voltage (Sw 1: A or B)	V_{THI}	V_{ref} +100 mV	V_{ref} +10 mV	–	Vdc
	V_S with Pulse Output (Sw 1: A or B)	V_{SPO}	6.0	8.5	–	Vdc
	Peak Output Current (Sw 1: A or B)	$I_{O\,pk}$	50	80	–	mA
	Pulse Threshold Voltage (Sw 1: A or B)	V_{THP}	–	V_{ref} -10 mV	V_{ref} -100 mV	Vdc
	Output Pulse Width (Sw 1: A or B, See Figure 2)	$\tau A, \tau B$ $V\tau A$, $V\tau B$	–	70 ±4.5	– –	μs V
	Output Current With Input Short (Sw 1: B; Sw 2: A) (Sw 1: A; Sw 2: B)	I_{SC}	 – –	 5.0 5.0	 100 100	μA

8

TEST CIRCUIT AND TYPICAL CHARACTERISTICS

FIGURE 3 – CIRCUIT WITH INCREASED PULSE WIDTH AND TRIAC DRIVER TO CONTROL HIGH-CURRENT SCR's

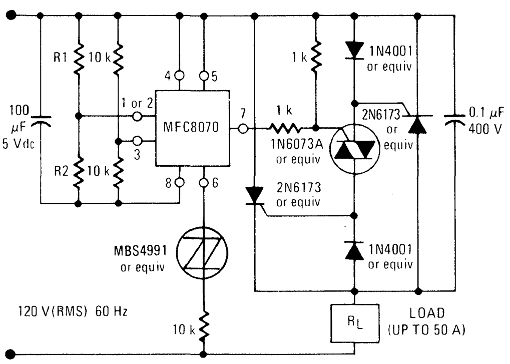
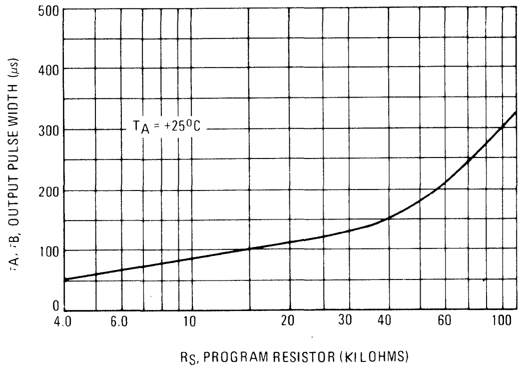
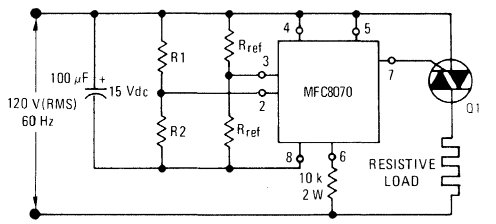


FIGURE 4 – OUTPUT PULSE WIDTH versus SOURCE RESISTANCE (See Figure 6.)



TYPICAL ZERO VOLTAGE SWITCH APPLICATIONS FOR TRIAC CONTROL

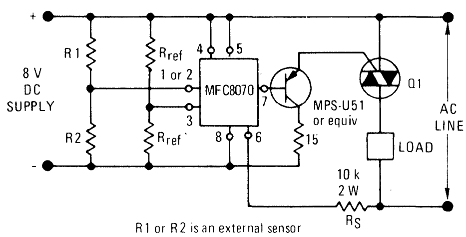
FIGURE 5 – TRIAC CONTROL CIRCUIT



R1 or R2 is an external sensor

Basic triac trigger circuit utilizing the zero crossing detector and the input comparator to control triacs with gate current requirements to 500 mA.

FIGURE 6 – TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING DC SUPPLY



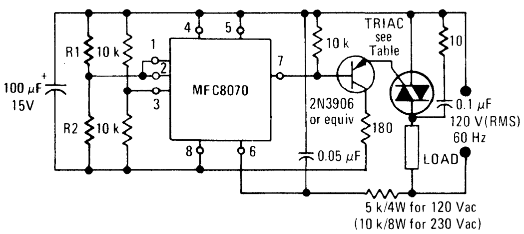
R1 or R2 is an external sensor

Basic dc trigger application using the input comparator to control a PNP capable of furnishing gate drive of approximately 0.5 A.

Suggested circuit to vary output pulse width by value of R_S (See Figure 4).

R2 must be the external sensor for the internal short and open protection to be operative.

FIGURE 7 – TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING AC SUPPLY



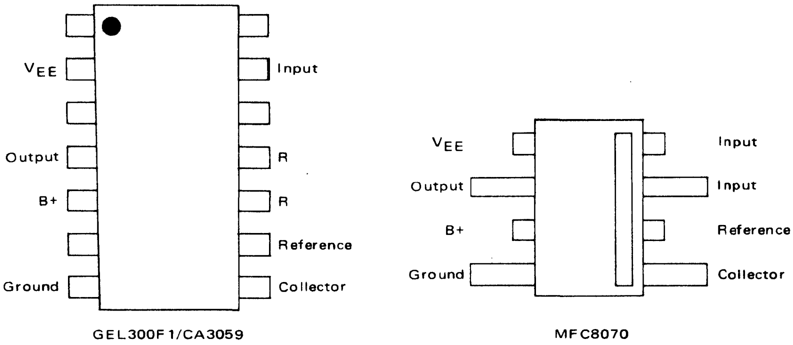
Zero crossing triac control circuit for gate current requirements to 100 mA.

Recommended Motorola triacs for use in circuit.

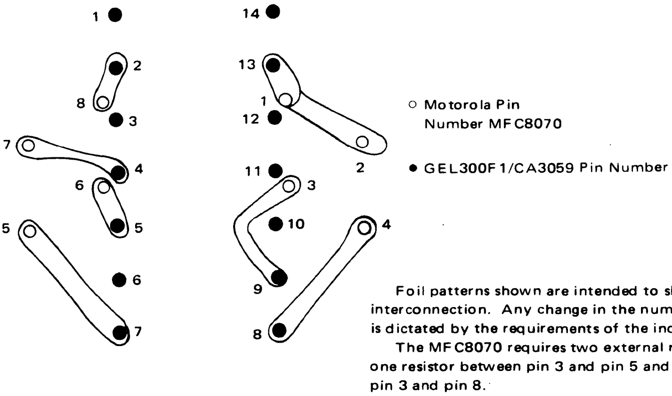
Maximum Continuous Current (A [RMS])	Triac Family	Case No.
10	2N6151/2N6153 2N6346A/2N6349A	90 (Plastic) 221-024 (Plastic)
10	2N6139/2N6144	86, 250
25	2N6157/2N6165	174, 175, 235
40	2N5441/2N5446	237, 238, 239

8

PIN COMPARISON OF MFC8070 AND GEL300F1 (PA424/CA3059)



COMPATIBLE PRINTED CIRCUIT FOIL PATTERN FOR MFC8070, GEL300F1 (PA424) AND CA3059



Foil patterns shown are intended to show pin-for-pin interconnection. Any change in the number of components is dictated by the requirements of the individual design.

The MFC8070 requires two external reference resistors; one resistor between pin 3 and pin 5 and the other between pin 3 and pin 8.

8

OPERATIONAL AMPLIFIERS

MLM101A
MLM201A
MLM301A

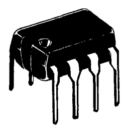
MONOLITHIC OPERATIONAL AMPLIFIER

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation summing amplifier slew rates to 10 V/μs can be obtained.

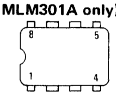
- Low Input Offset Current — 20 nA maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short-Circuit Protection
- Guaranteed Drift Characteristics

OPERATIONAL AMPLIFIER

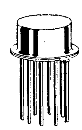
MONOLITHIC SILICON
INTEGRATED CIRCUIT



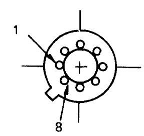
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MLM201A and MLM301A only)



(top view)



G SUFFIX
METAL PACKAGE
CASE 601



(bottom view)

FIGURE 1 — STANDARD COMPENSATING AND OFFSET BALANCING CIRCUIT

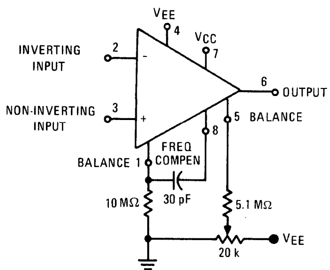
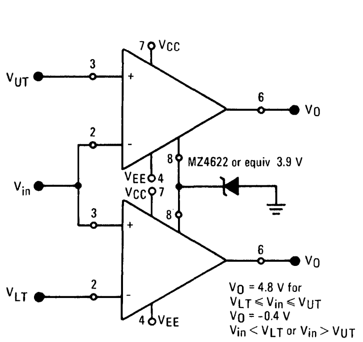
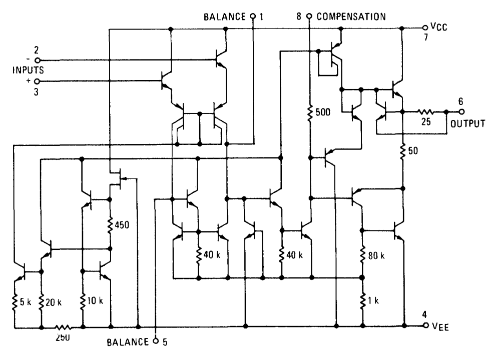


FIGURE 2 — DOUBLE-ENDED LIMIT DETECTOR



PINS NOT SHOWN ARE NOT CONNECTED

FIGURE 3 — CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	VALUE MLM101A	VALUE MLM201A	VALUE MLM301A	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±22	±22	±18	Vdc
Differential Input Voltage	V_{in}	← ±30 →			Volts
Common-Mode Input Swing (Note 1)	V_{ICR}	← ±15 →			Volts
Output Short-Circuit Duration	t_S	← Continuous →			
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +75°C Plastic Dual In-Line Package (MLM201A/301A) Derate above T_A = +25°C	P_D	 ← 500 → ← 6.8 → 625 5.0			 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +75	°C
Storage Temperature Range	T_{stg}	← -65 to +150 →			°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the MLM101A and MLM201A, and from ±5.0 V to ±15 V for the MLM301A.

Characteristics	Symbol	MLM101A MLM201A Min	Typ	Max	MLM301A Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 50$ kΩ)	$\|V_{IO}\|$	–	0.7	2.0	–	2.0	7.5	mV
Input Offset Current	$\|I_{IO}\|$	–	1.5	10	–	3.0	50	nA
Input Bias Current	I_{IB}	–	30	75	–	70	250	nA
Input Resistance	R_{in}	1.5	4.0	–	0.5	2.0	–	Megohms
Supply Current V_S = ±20 V V_S = ±15 V	I_D	 – –	 1.8 –	 3.0 –	 – –	 – 1.8	 – 3.0	mA
Large Signal Voltage Gain V_S = ± 15 V, V_O = ± 10 V, R_L > 2.0 kΩ)	A_v	50	160	–	25	160	–	V/mV

The following specifications apply over the operating temperature range.

Characteristics	Symbol	MLM101A MLM201A Min	Typ	Max	MLM301A Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 50$ kΩ)	$\|V_{IO}\|$	–	–	3.0	–	–	10	mV
Input Offset Current	$\|I_{IO}\|$	–	–	20	–	–	70	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(min) \leq T_A \leq T_A(max)$	$\|\Delta V_{IO}/\Delta T\|$	–	3.0	15	–	6.0	30	µV/°C
Average Temperature Coefficient of Input Offset Current +25°C ≤ $T_A \leq T_A(max)$ $T_A(min) \leq T_A \leq$ 25°C	$\|\Delta I_{IO}/\Delta T\|$	 – –	 0.01 0.02	 0.1 0.2	 – –	 0.01 0.02	 0.3 0.6	nA/°C
Input Bias Current	I_{IB}	–	–	100	–	–	300	nA
Large Signal Voltage Gain V_S = ± 15 V, V_O = ± 10 V, R_L > 2.0 kΩ	A_v	25	–	–	15	–	–	V/mV
Input Voltage Range V_S = ±20 V V_S = ±15 V	V_{in}	 ±15 –	 – –	 – –	 – ±12	 – –	 – –	V
Common-Mode Rejection Ratio $R_S \leq 50$ kΩ	CMRR	80	96	–	70	90	–	dB
Supply Voltage Rejection Ratio $R_S \leq 50$ kΩ	PSSR	80	96	–	70	96	–	dB
Output Voltage Swing V_S = ±15 V, R_L = 10 kΩ R_L = 2.0 kΩ	V_O	 ±12 ±10	 ±14 ±13	 – –	 ±12 ±10	 +14 ±13	 – –	V
Supply Current ($T_A = T_A(max)$, V_S = ± 20 V)	I_D	–	1.2	2.5	–	–	–	mA

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MINIMUM INPUT VOLTAGE RANGE

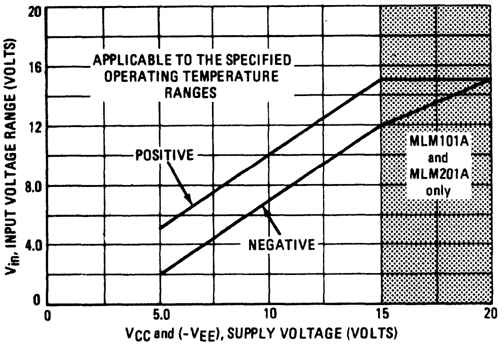


FIGURE 5 – MINIMUM OUTPUT VOLTAGE SWING

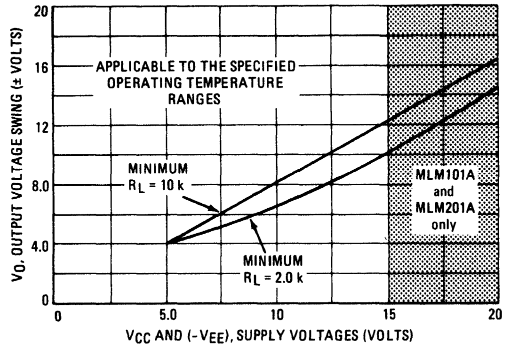


FIGURE 6 – MINIMUM VOLTAGE GAIN

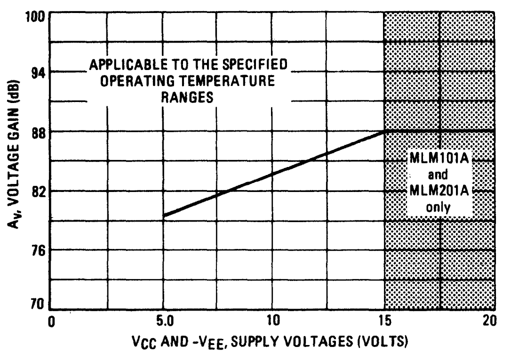


FIGURE 7 – TYPICAL SUPPLY CURRENTS

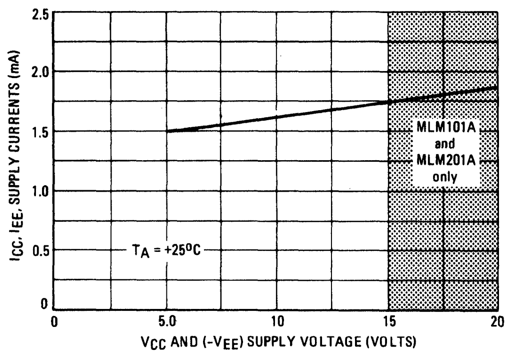


FIGURE 8 – OPEN-LOOP FREQUENCY RESPONSE

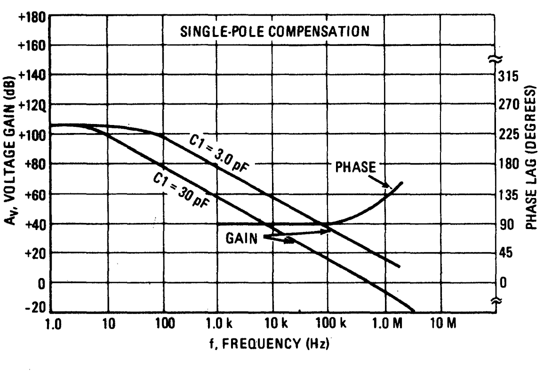
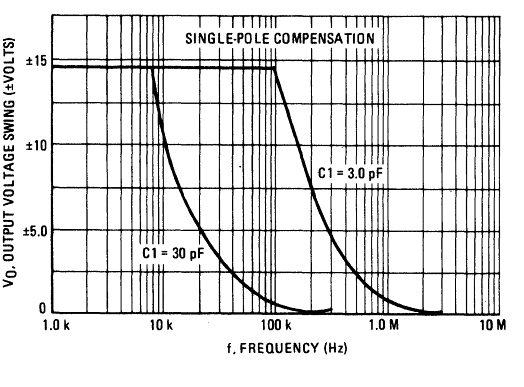


FIGURE 9 – LARGE-SIGNAL FREQUENCY RESPONSE



8

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – VOLTAGE FOLLOWER PULSE RESPONSE

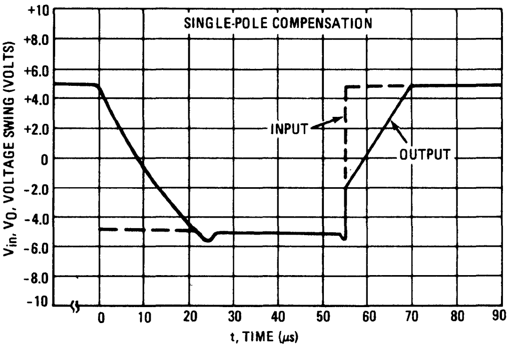


FIGURE 11 – OPEN-LOOP FREQUENCY RESPONSE

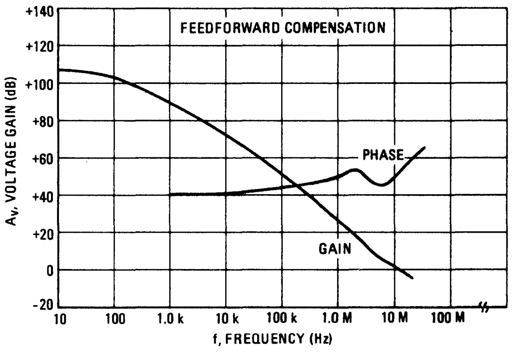


FIGURE 12 – LARGE-SIGNAL FREQUENCY RESPONSE

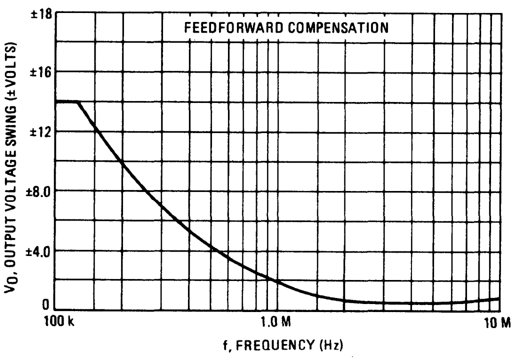
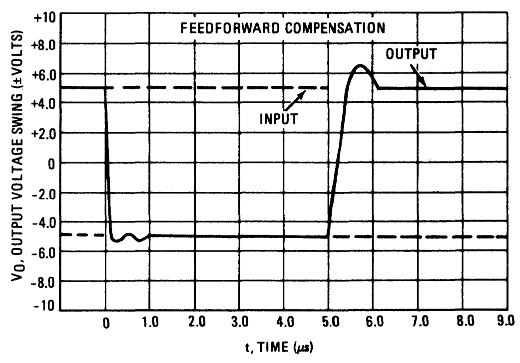
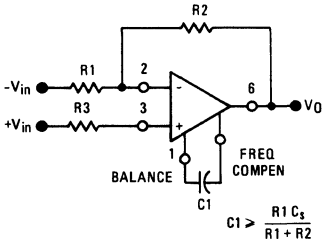


FIGURE 13 – INVERTER PULSE RESPONSE



TYPICAL COMPENSATION CIRCUITS

FIGURE 14 – SINGLE-POLE COMPENSATION

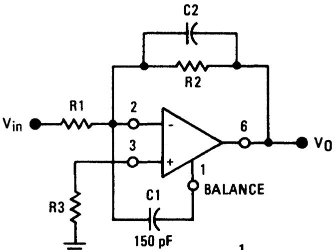


$C1 > \frac{R1\,C_s}{R1 + R2}$

C_s = 30 pF

PINS NOT SHOWN ARE NOT CONNECTED.

FIGURE 15 – FEEDFORWARD COMPENSATION



$C2 = \frac{1}{2\pi f_0 R2}$

f_0 = 3.0 MHz

PINS NOT SHOWN ARE NOT CONNECTED.

8

MLM104G
MLM204G
MLM304G

NEGATIVE VOLTAGE REGULATOR

MONOLITHIC NEGATIVE VOLTAGE REGULATOR

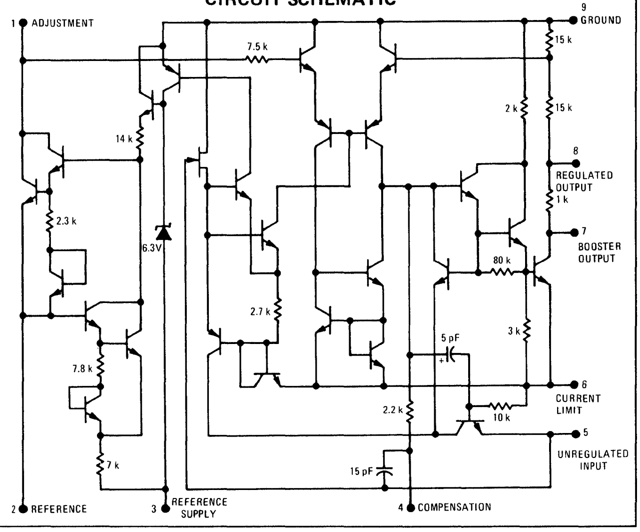
The MLM104G, MLM204G, and MLM304G are functionally, electrically, and pin-for-pin equivalent to the LM104, LM204 and LM304 respecitvely.

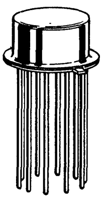
- Regulation No Load to Full Load – 1.0 mV
- Line Regulation – 0.01 %/V
- Ripple Rejection – 0.2 mV/V
- Temperature Stability Over Temperature Range – 0.3%

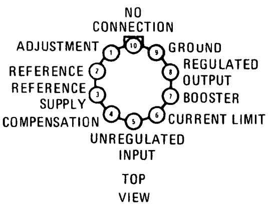
NEGATIVE VOLTAGE REGULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

CIRCUIT SCHEMATIC





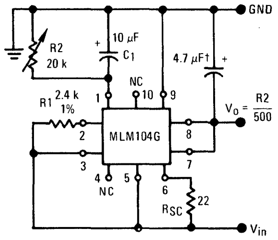


Pin 5 Electrically Connected to Case Through Substrate

METAL PACKAGE
CASE 603
(TO-100)

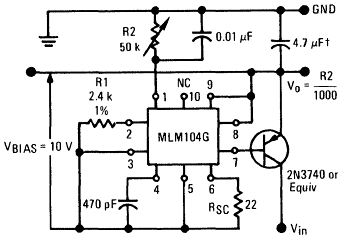
TYPICAL APPLICATIONS

FIGURE 1 – BASIC REGULATOR CIRCUIT



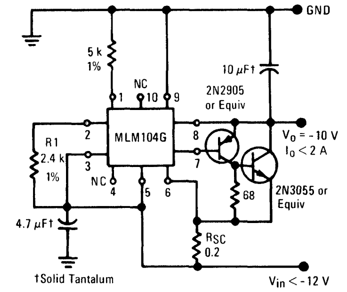
†Solid Tantalum
Trim R1 for exact scale factor.

FIGURE 2 – SEPARATE BIAS SUPPLY OPERATION



†Solid Tantalum

FIGURE 3 – HIGH CURRENT REGULATOR



†Solid Tantalum

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MLM104G	MLM204G	MLM304G	Unit
Input Voltage	V_{in}	50	50	40	Vdc
Input-Output Voltage Differential	$V_{in}-V_o$	50	50	40	Vdc
Power Dissipation (See Note 1)	P_D	680	680	680	mW
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C
Lead Temperature (soldering, t = 10 s)	T_S	300	300	300	°C

ELECTRICAL CHARACTERISTICS (See Note 2)

Characteristic	Symbol	MLM104G MLM204G Min	Typ	Max	MLM304G Min	Typ	Max	Unit
Input Voltage Range	V_{in}	-8.0	–	-50	-8.0	–	-40	Volts
Output Voltage Range	V_o	-0.015	–	-40	-0.035	–	-30	Volts
Output-Input Voltage Differential	$\|V_{in}-V_o\|$							Volts
I_o = 20 mA		2.0	–	50	2.0	–	40	
I_o = 5.0 mA		0.5	–	50	0.5	–	40	
Load Regulation $0 \leq I_o \leq 20$ mA, R_{SC} = 15Ω	Reg_{load}	–	1.0	5.0	–	1.0	5.0	mV
Line Regulation $V_o \leq -5.0$ V, ΔV_{in} = 0.1 V	Reg_{in}	–	0.056	0.1	–	0.056	0.1	%
Ripple Rejection (See Figure 1) (C_1 = 10 μF, f = 120 Hz)	Rej_R							mV/V
$V_{in} < -15$ V		–	0.2	0.5	–	0.2	0.5	
$-7.0\text{ V} \geq V_{in} \geq -15$ V		–	0.5	1.0	–	0.5	1.0	
Output Voltage Scale Factor R_1 = 2.4 k Ω (See Figures 1,2 and 3)	SF	1.8	2.0	2.2	1.8	2.0	2.2	V/k Ω
Temperature Stability	TCV_o $\Delta V_o/\Delta T$							%
$V_o \leq -1.0$ V		–	0.3	1.0	–	–	–	
$V_o \leq -1.0$ V, $0°C \leq T_A \leq +70°C$		–	–	–	–	0.3	1.0	
Output Noise Voltage (See Figure 1) ($10\text{ Hz} \leq f \leq 10\text{ kHz}$)	V_n							
$V_o \leq -5.0$ V, C_1 = 0		–	0.007	–	–	0.007	–	%
C_1 = 10 μF		–	15	–	–	15	–	μV
Standby Current Drain (I_L = 5.0 mA)	I_B							mA
V_o = 0		–	1.7	2.5	–	1.7	2.5	
V_o = -40 V		–	3.6	5.0	–	–	–	
V_o = -30 V		–	–	–	–	3.6	5.0	
Long Term Stability $V_o \leq -1.0$ V	S	–	0.1	1.0	–	0.1	1.0	%

Note 1. The maximum junction temperature of the MLM104G is +150°C, for the MLM204G – +100°C, and for the MLM304G – +85°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance of 150°C/W – junction to ambient, or 45°C/W – junction to case.

Note 2. These specifications apply for junction temperatures of -55°C to +150°C for the MLM104G; -25°C to +100°C for the MLM204G; and 0 to +85°C for the MLM304G. The specifications also apply for input and output voltages within the indicated ranges (unless otherwise specified). Load and line regulation specifications given are for constant junction temperature. Temperature drift effects must be taken into account separately when the device is operating under conditions of high power dissipation.

8

MLM105G
MLM205G
MLM305G

POSITIVE VOLTAGE REGULATOR

MONOLITHIC POSITIVE VOLTAGE REGULATOR

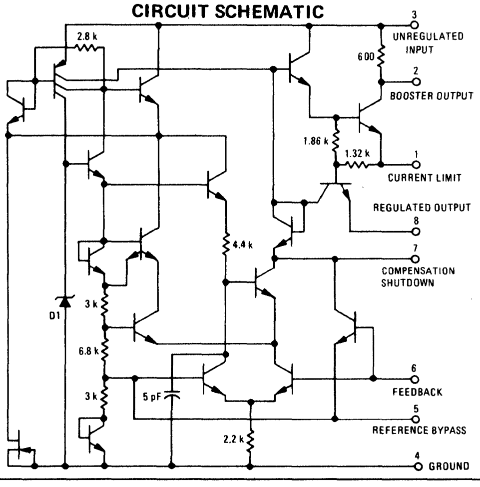
The MLM105G, MLM205G, and MLM305G are functionally, electrically, and pin-for-pin equivalent to the LM105, LM205, and LM305 respectively.

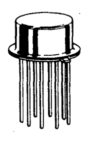
- Output Voltage Adjustable from 4.5 V to 40 V
- Output Currents in Excess of 10 A Possible by Addition of External Transistors
- Load Regulation Better than 0.1%, Full Load with Current Limiting
- DC Line Regulation, 0.03%/V
- Ripple Rejection, 0.01 %/V

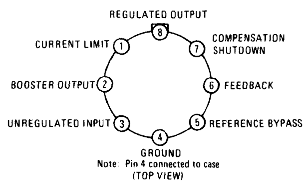
POSITIVE VOLTAGE REGULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

CIRCUIT SCHEMATIC





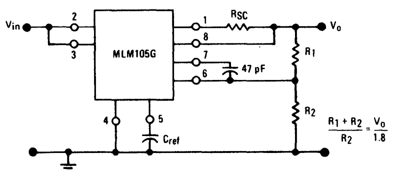


Note: Pin 4 connected to case
(TOP VIEW)

METAL PACKAGE
CASE 601
(TO-99)

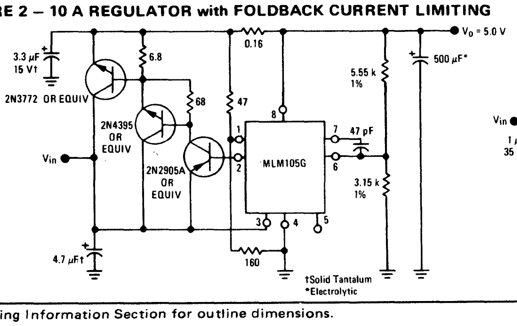
TYPICAL APPLICATIONS

FIGURE 1 – BASIC REGULATOR CIRCUIT



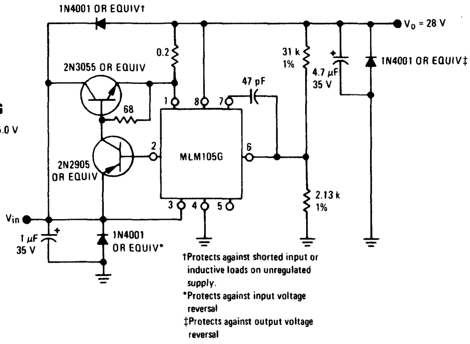
$$\frac{R_1 + R_2}{R_2} = \frac{V_o}{1.8}$$

FIGURE 2 – 10 A REGULATOR with FOLDBACK CURRENT LIMITING



†Solid Tantalum
*Electrolytic

FIGURE 3 – 1.0 A REGULATOR with PROTECTIVE DIODES



†Protects against shorted input or inductive loads on unregulated supply.
*Protects against input voltage reversal
‡Protects against output voltage reversal

See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MLM105G	MLM205G	MLM305G	Unit
Input Voltage	V_{in}	50	50	40	Vdc
Input-Output Voltage Differential	$\lvert V_{in}\text{-}V_o \rvert$	40	40	40	Vdc
Power-Dissipation (See Note 1)	P_D	680	680	680	mW
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C
Lead Temperature (soldering, t = 10 s)	T_S	300	300	300	°C

ELECTRICAL CHARACTERISTICS (See Note 2)

Characteristic	Symbol	MLM105G MLM205G			MLM305G			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	8.5	–	50	8.5	–	40	Volts
Output Voltage Range	V_O	4.5	–	40	4.5	–	30	Volts
Output-Input Voltage Differential	$\lvert V_{in}\text{-}V_O \rvert$	3.0	–	30	3.0	–	30	Volts
Load Regulation (See Figure 1) ($0 \leqslant I_O \leqslant 12$ mA) R_{SC} = 18 Ω, T_A = +25°C R_{SC} = 10 Ω, T_A = T_{high}* R_{SC} = 18 Ω, T_A = T_{low}**	Reg_{load}	 – – –	 0.02 0.03 0.03	 0.05 0.1 0.1	 – – –	 0.02 0.03 0.03	 0.05 0.1 0.1	%
Line Regulation $V_{in}\text{-}V_O \leqslant 5.0$ V $V_{in}\text{-}V_O > 5.0$ V	Reg_{in}	 – –	 0.025 0.015	 0.06 0.03	 – –	 0.025 0.015	 0.06 0.03	%/V
Ripple Rejection (See Figure 1) C_{ref} = 10 μF, f = 120 Hz	$\frac{\Delta V_O}{V_O \Delta V_i}$	–	0.003	0.01	1.0	0.003	0.01	%/V
Temperature Stability $T_{low}^{**} \leqslant T_A \leqslant T_{high}^{*}$	TCV_O	–	0.3	1.0	–	0.3	1.0	%
Feedback Sense Voltage	V_{ref}	1.63	1.7	1.81	1.63	1.7	1.81	Volts
Output Noise Voltage (See Figure 1) ($10 \text{ Hz} \leqslant f \leqslant 10$ kHz) C_{Ref} = 0 $C_{Ref} > 0.1$ μF	V_n	 – –	 0.005 0.002	 – –	 – –	 0.005 0.002	 – –	%
Standby Current Drain V_{in} = 50 V V_{in} = 40 V	I_B	 – –	 0.8 –	 2.0 –	 – –	 – 0.8	 – 2.0	mA
Long Term Stability	S	–	0.1	1.0	–	0.1	1.0	%

*T_{high} = +125°C for MLM105G
+85°C for MLM205G
+70°C for MLM305G

**T_{low} = -55°C for MLM105G
-25°C for MLM205G
0°C for MLM305G

Note 1. The maximum junction temperature of the MLM105G is +150°C, for the MLM205G – +100°C, and for the MLM305G – +85°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance of 150°C/W – junction to ambient, or 45°C/W – junction to case.

Note 2. These specifications apply for junction temperatures of -55°C to +150°C for the MLM105G, -25°C to +85°C for the MLM205G, and 0 to +70°C for the MLM305G. Specifications also apply for input and output voltages within the indicated ranges and for a divider impedance sensed by the feedback terminal of 2.0 kilohms (unless otherwise specified). Load and line regulation specifications given are for constant junction temperature. Temperature drift effects must be taken into account separately when the device is operating under conditions of high power dissipation.

OPERATIONAL AMPLIFIERS

MLM107G
MLM207G
MLM307G

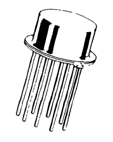
INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER

A general purpose operational amplifier series well suited for applications requiring lower input currents than are available with the popular MC1741. These improved input characteristics permit greater accuracy in sample and hold circuits and long interval integrators.

- Internally Compensated
- Low Offset Voltage: 2.0 mV max (MLM107G)
- Low Input Offset Current: 10 nA max (MLM107G)
- Low Input Bias Current: 75 nA max (MLM107G)

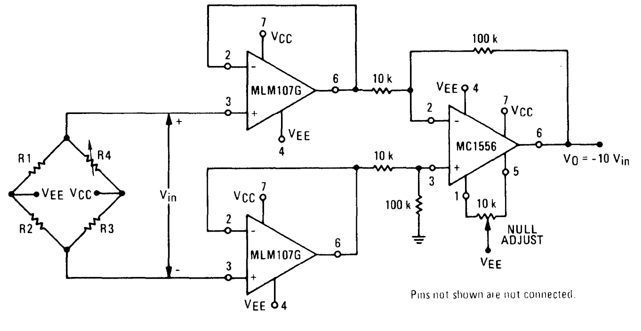
OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED

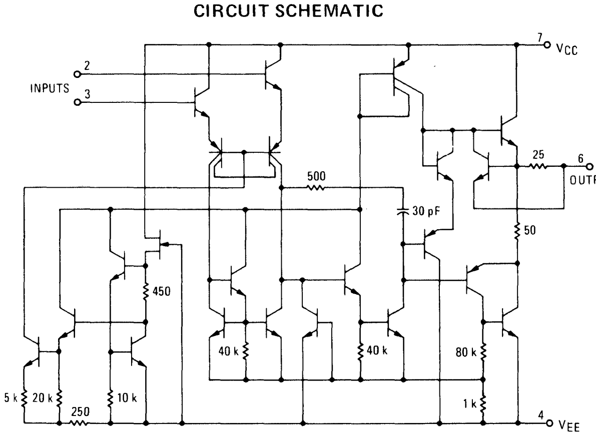


METAL PACKAGE
CASE 601

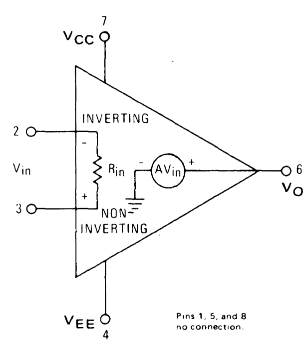
TYPICAL APPLICATION
HIGH IMPEDANCE BRIDGE AMPLIFIER



CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MLM107G	MLM207G	MLM307G	Unit
Power Supply Voltages	V_{CC} V_{EE}	+22 -22	+22 -22	+18 -18	Vdc
Differential Input Signal Voltage	V_{ID}	±30	±30	±30	Volts
Common-Mode Input Swing (Note 1)	V_{ICR}	±15	±15	±15	Volts
Output Short-Circuit Duration	t_{OS}	Indefinite			
Power Dissipation (Package Limitation) (Note 2)	P_D	500	500	500	mW
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted, see Note 3.)

Characteristics	Symbol	MLM107G MLM207G			MLM307G			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$\|V_{IO}\|$							mV
$R_S \le 10\ k\Omega$, T_A = +25°C		–	0.7	2.0	–	–	–	
$R_S \le 10\ k\Omega$, $T_A = T_{low}$ to T_{high}		–	–	3.0	–	–	–	
$R_S \le 50\ k\Omega$, T_A = +25°C		–	–	–	–	2.0	7.5	
$R_S \le 50\ k\Omega$, $T_A = T_{low}$ to T_{high}		–	–	–	–	–	10	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C		–	1.5	10	–	3.0	50	
$T_A = T_{low}$ to T_{high}		–	–	20	–	–	70	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	30	75	–	70	250	
$T_A = T_{low}$ to T_{high}		–	–	100	–	–	300	
Input Resistance	R_{in}	1.5	4.0	–	0.5	2.0	–	Megohms
Supply Current	I_D							mA
V_S = ±20 V, T_A = +25°C		–	1.8	3.0	–	–	–	
V_S = ±20 V, $T_A = T_{high}$		–	1.2	2.5	–	–	–	
V_S = ±15 V, T_A = +25°C		–	–	–	–	1.8	3.0	
Large-Signal Voltage Gain	A_v							V/mV
V_S = ±15 V, V_O = ±10 V, $R_L > 2.0\ k\Omega$, T_A = +25°C		50	160	–	25	160	–	
V_S = ±15 V, V_O = ±10 V, $R_L \geq 2.0\ k\Omega$, $T_A = T_{low}$		25	–	–	15	–	–	
Average Temperature Coefficient of Input Offset Voltage $T_{low} \le T_A \le T_{high}$	$\|TC_{V_{IO}}\|$	–	3.0	15	–	6.0	30	μV/°C
Average Temperature Coefficient of Input Offset Current	$\|TC_{I_{IO}}\|$							nA/°C
+25°C $\le T_A \le T_{high}$		–	0.01	0.1	–	0.01	0.3	
$T_{low} \le T_A \le$ +25°C		–	0.02	0.2	–	0.02	0.6	
Output Voltage Swing ($T_A = T_{low}$ to T_{high})	V_O							V
V_S = ±15 V, R_L = 10 kΩ		±12	±14	–	±12	+14	–	
R_L = 2.0 kΩ		±10	±13	–	±10	±13	–	
Input Voltage Range ($T_A = T_{low}$ to T_{high})	$V_{in\ R}$							V
V_S = ±20 V		±15	–	–	–	–	–	
V_S = ±15 V		–	–	–	±12	–	–	
Common-Mode Rejection Ratio ($T_A = T_{low}$ to T_{high}) $R_S \leq 50\ k\Omega$	CMRR	80	96	–	70	90	–	dB
Supply-Voltage Rejection Ratio ($T_A = T_{low}$ to T_{high}) $R_S \leq 50\ k\Omega$	VSRR	80	96	–	70	96	–	dB

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. For operating at elevated temperatures, the device must be derated based on a maximum junction temperature of +150°C for the MLM107G, and 100°C for the MLM207G and MLM307G. The TO-99 package is derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3. Unless otherwise noted, these specifications apply for:

$\pm 5.0\ V \le V_S \le \pm 20\ V$, $-55°C \le T_A \le +125°C$, MLM107G (T_{low} = -55°C, T_{high} = +125°C)

$\pm 5.0\ V \le V_S \le \pm 20\ V$, $-25°C \le T_A \le +85°C$, MLM207G

$\pm 5.0\ V \le V_S \le \pm 15\ V$, $0°C \le T_A \le +70°C$, MLM307G

8

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 – MINIMUM INPUT VOLTAGE RANGE

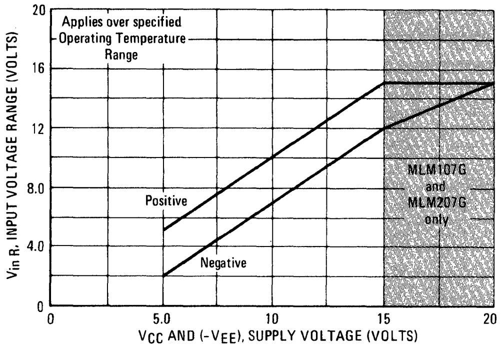


FIGURE 2 – MINIMUM OUTPUT VOLTAGE SWING

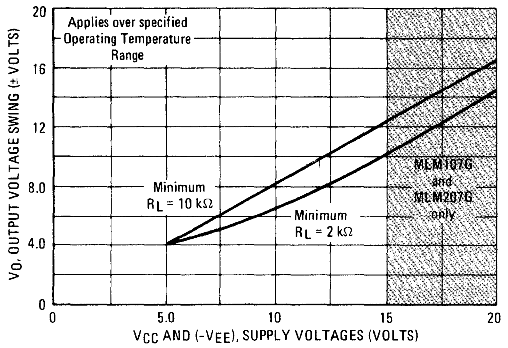


FIGURE 3 – MINIMUM VOLTAGE GAIN

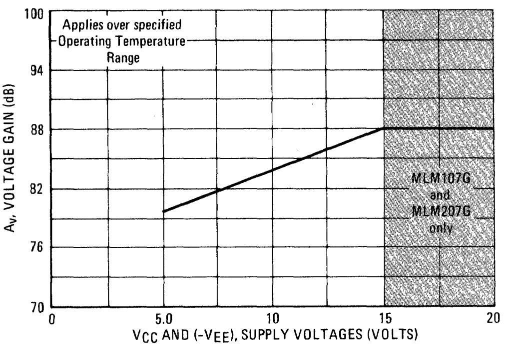


FIGURE 4 – TYPICAL SUPPLY CURRENTS

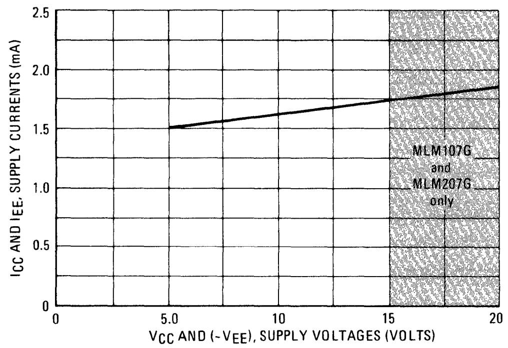


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

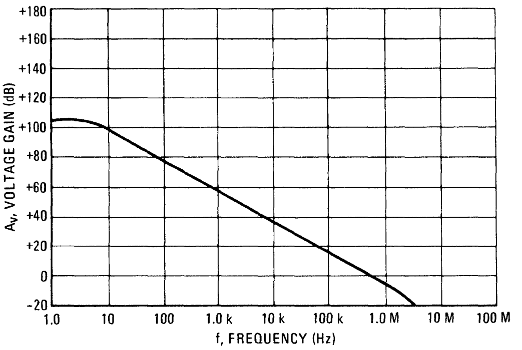
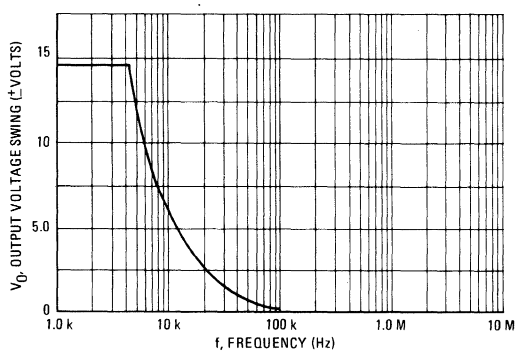


FIGURE 6 – LARGE-SIGNAL FREQUENCY RESPONSE



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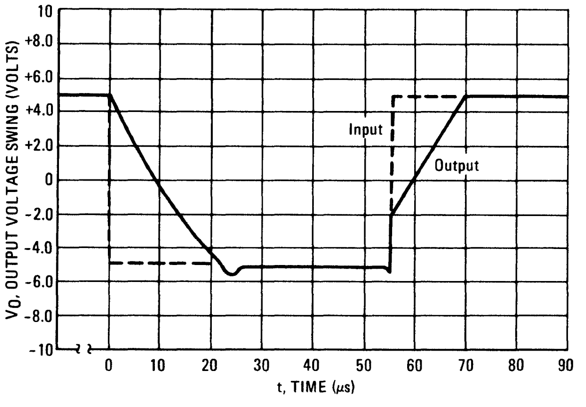
TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – VOLTAGE FOLLOWER PULSE RESPONSE



MLM109
MLM209
MLM309

VOLTAGE REGULATOR

MONOLITHIC POSITIVE THREE - TERMINAL FIXED VOLTAGE REGULATOR

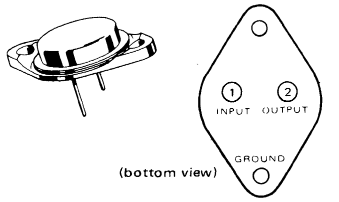
A versatile positive fixed +5.0-volt regulator designed for easy application as on on-card, local voltage regulator for digital logic systems. Current limiting and thermal shutdown are provided to make the units extremely rugged.

In most applications only one external component, a capacitor, is required in conjunction with the MLM109 Series devices. Even this component may be omitted if the power-supply filter is not located an appreciable distance from the regulator.

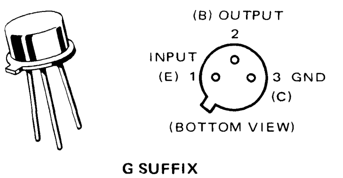
- High Maximum Output Current – Over 1.0 Ampere in TO-3 type Package – Over 200 mA in TO-39 Package
- Minimum External Components Required
- Internal Short-Circuit Protection
- Internal Thermal Overload Protection
- Excellent Line and Load Transient Rejection
- Designed for Use with Popular MDTL and MTTL Logic

POSITIVE VOLTAGE REGULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

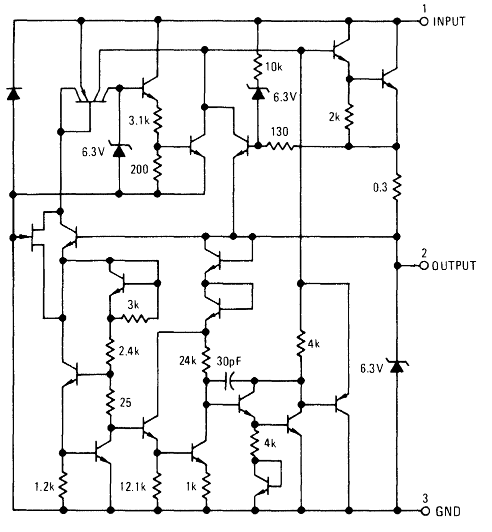


K SUFFIX
METAL PACKAGE
CASE 11
(TO-3 Type)

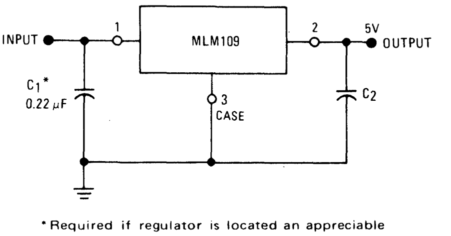


G SUFFIX
METAL PACKAGE
CASE 79
(TO-39)

CIRCUIT SCHEMATIC



FIXED 5.0 V REGULATOR



*Required if regulator is located an appreciable distance from power supply filter.
Although no output capacitor is needed for stability, it does improve transient response.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation	P_D	Internally Limited	
Junction Temperature Range	T_J		^{o}C
MLM109		-55 to +150	
MLM209		-55 to +150	
MLM309		0 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	^{o}C
Lead Temperature (soldering, t = 60 s)	T_S	300	^{o}C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MLM109 / MLM209 ①			MLM309 ②			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.7	5.05	5.3	4.8	5.05	5.2	Vdc
Input Regulation (T_J = +25°C) $7.0 \leqslant V_{in} \leqslant 25$ V	Reg_{in}	–	4.0	50	–	4.0	50	mV
Load Regulation (T_J = +25°C)	Reg_{load}							mV
Case 11-01 **(type TO-3)** 5.0 mA $\leqslant I_O \leqslant$ 1.5A		–	50	100	–	50	100	
Case 79-02 **(TO-39)** 5.0 mA $\leqslant I_O \leqslant$ 0.5A		–	20	50	–	20	50	
Output Voltage Range $7.0 V \leqslant V_{in} \leqslant 25$ V, 5.0 mA $\leqslant I_O \leqslant I_{max}$, $P \leqslant P_{max}$	V_O	4.6	–	5.4	4.75	–	5.25	Vdc
Quiescent Current (7.0 V $\leqslant V_{in} \leqslant$ 25 V)	I_B	–	5.2	10	–	5.2	10	mAdc
Quiescent Current Change (7.0 V $\leqslant V_{in} \leqslant$ 25 V)	I_B	–	–	0.5	–	–	0.5	
5.0 mA $\leqslant I_O \leqslant I_{max}$		–	–	0.8	–	–	0.8	
Output Noise Voltage (T_A = +25°C) 10 Hz $\leqslant f \leqslant$ 100 kHz	V_N	–	40	–	–	40	–	μV
Long Term Stability	S	–	–	10	–	–	20	mV
Thermal Resistance, Junction to Case ③	θJC							$^{o}C/W$
Case 11-01 (type TO-3)		–	3.0	–	–	3.0	–	
Case 79-02 (TO-39)		–	15	–	–	15	–	

NOTES:

① Unless otherwise specified, these specifications apply for -55°C $\leqslant T_J \leqslant$ +150° (-25°C $\leqslant T_J \leqslant$ +150°C for the MLM209). For Case 79-02 (TO-39) V_{in} = 10 V, I_O = 0.1 A, I_{max} = 0.2 A and P_{max} = 2.0 W. For Case 11-01 **(type TO-3)** V_{in} = 10 V, I_O = 0.5 A, I_{max} = 1.0 A and P_{max} = 20 W.

② Unless otherwise specified, these specifications apply for 0°C $\leqslant T_J \leqslant$ +125°C, V_{in} = 10V. For Case 79-02 (TO-39) I_O = 0.1A, I_{max} = 0.2A and P_{max} = 2.0 W. For Case 11-01 (type TO-3) I_O = 0.5 A, I_{max} = 1.0 A and P_{max} = 20 W.

③ Without a heat sink, the thermal resistance of the Case 79-02 **(TO-39)** package is about 150°C/W, while that of the Case 11-01 (type TO-3) package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the heat sink.

TYPICAL CHARACTERISTICS

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION (MLM109K, MLM209K)

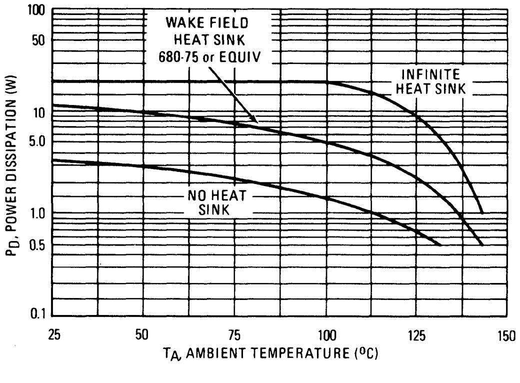
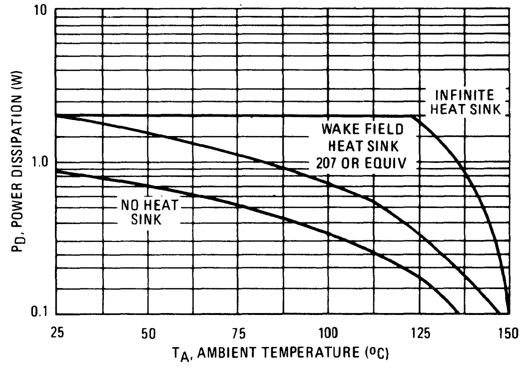


FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION (MLM109G, MLM209G)



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TYPICAL CHARACTERISTICS (continued)

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 3 – MAXIMUM AVERAGE POWER DISSIPATION (MLM309K)

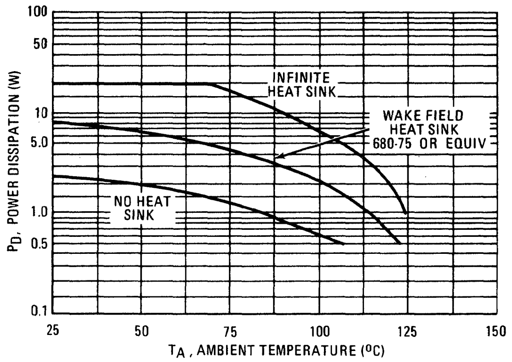


FIGURE 4 – MAXIMUM AVERAGE POWER DISSIPATION (MLM309G)

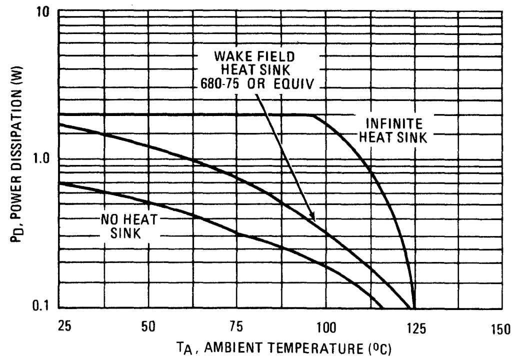


FIGURE 5 - OUTPUT IMPEDANCE versus FREQUENCY

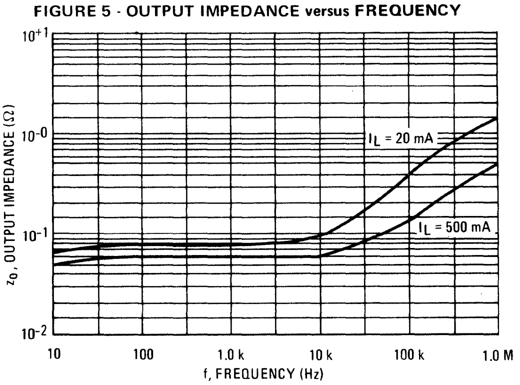


FIGURE 6 – PEAK OUTPUT CURRENT (K PACKAGE)

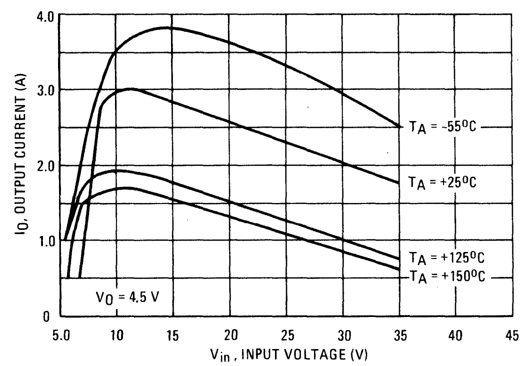


FIGURE 7 – PEAK OUTPUT CURRENT (G PACKAGE)

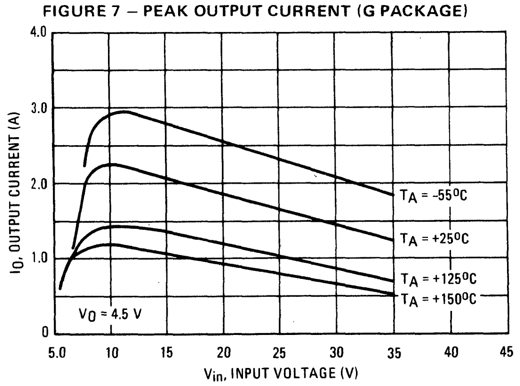
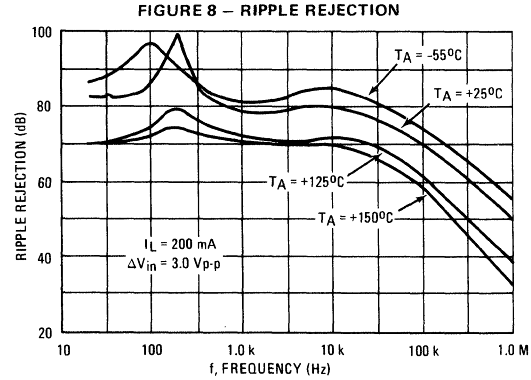


FIGURE 8 – RIPPLE REJECTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DROPOUT VOLTAGE

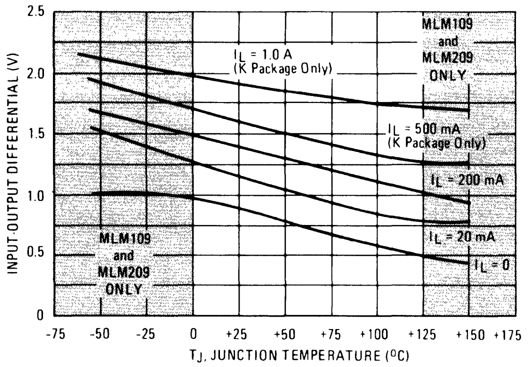


FIGURE 10 – DROPOUT CHARACTERISTIC (K PACKAGE)

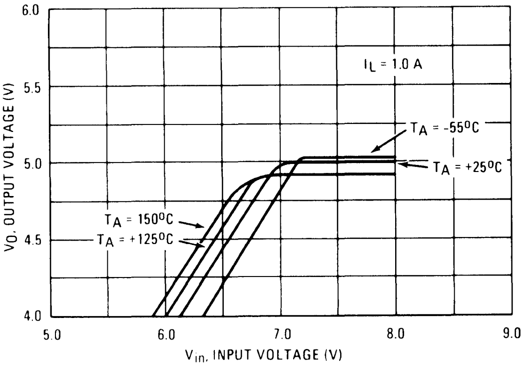


FIGURE 11 – OUTPUT VOLTAGE

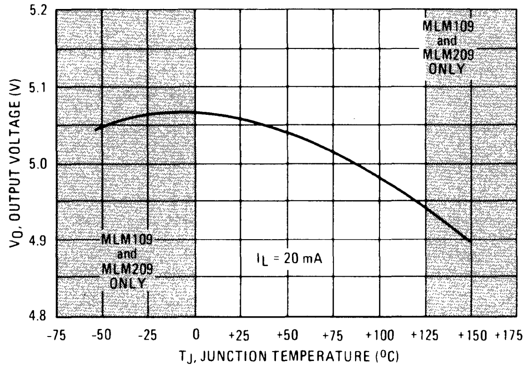


FIGURE 12 – OUTPUT NOISE VOLTAGE

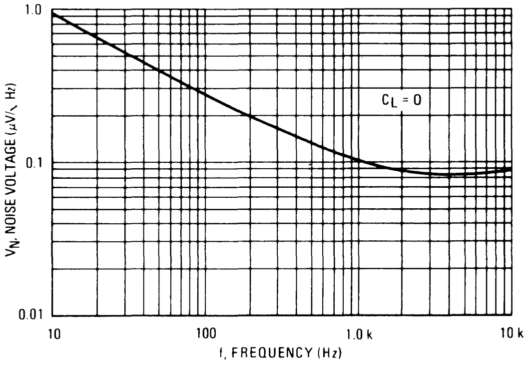


FIGURE 13 – QUIESCENT CURRENT

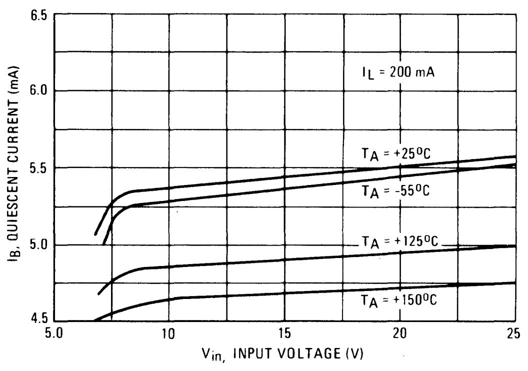
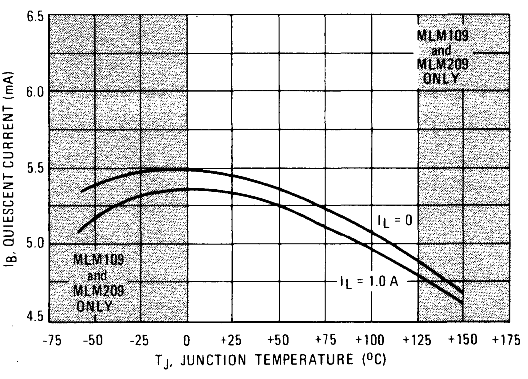


FIGURE 14 – QUIESCENT CURRENT



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TYPICAL APPLICATIONS

FIGURE 15 – ADJUSTABLE OUTPUT REGULATOR

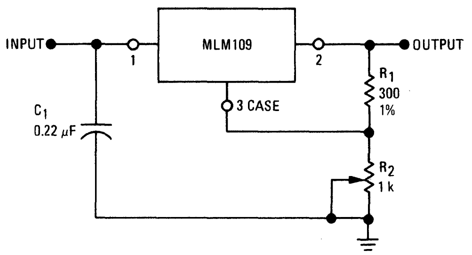
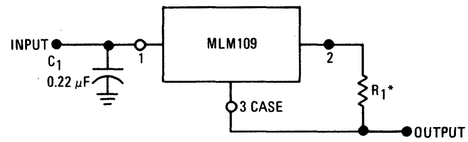


FIGURE 16 – CURRENT REGULATOR



*DETERMINES OUTPUT CURRENT.

FIGURE 17 – 5.0-VOLT, 3.0-AMPERE REGULATOR
(with plastic boost transistor)

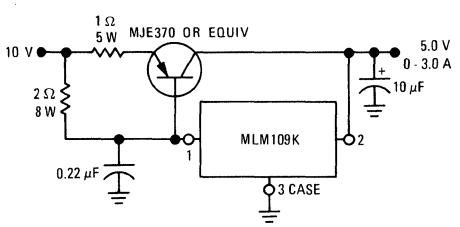


FIGURE 18 – 5.0 VOLT, 4.0-AMPERE TRANSISTOR
(with plastic Darlington boost transistor)

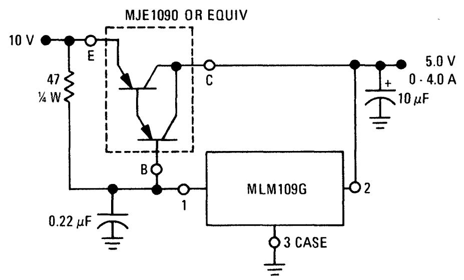


FIGURE 19 – 5.0-VOLT, 10-AMPERE REGULATOR

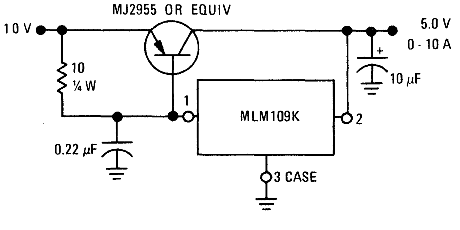
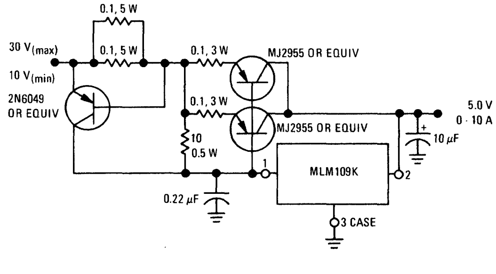


FIGURE 20 – 5.0-VOLT, 10-AMPERE REGULATOR
(with Short-Circuit Current Limiting for Safe-Area Protection of pass transistors)



OPERATIONAL AMPLIFIER

MLM110G
MLM210G
MLM310G

MONOLITHIC OPERATIONAL AMPLIFIER VOLTAGE FOLLOWER

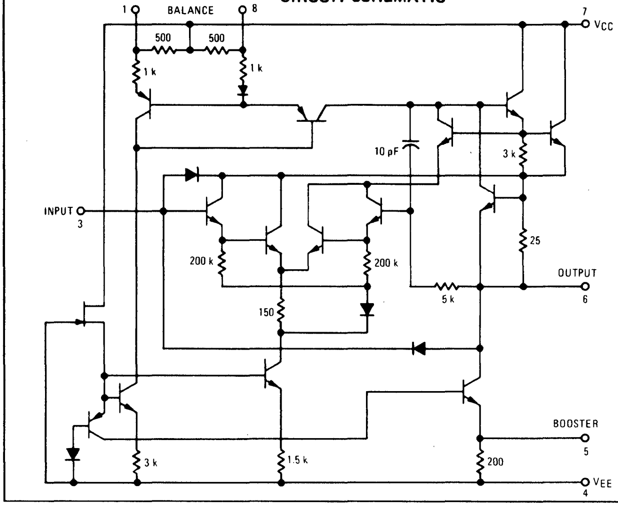
The MLM110G, MLM210G, and MLM310G are functionally, electrically, and pin-for-pin equivalent to the LM110, LM210, and LM310 respectively.

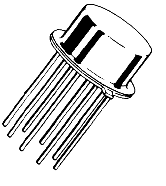
- Input Bias Current: 10 nA maximum over Temperature Range
- Small-Signal Bandwidth: 20 MHz typical
- Slew Rate: 30 Volts/μs typical
- Supply Voltage Range: ± 5.0 V to ± 18 V

OPERATIONAL AMPLIFIER VOLTAGE FOLLOWER INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED

CIRCUIT SCHEMATIC





METAL PACKAGE
CASE 601

TYPICAL APPLICATIONS

FIGURE 1 – OFFSET BALANCING CIRCUIT

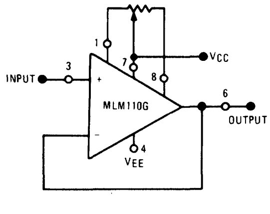
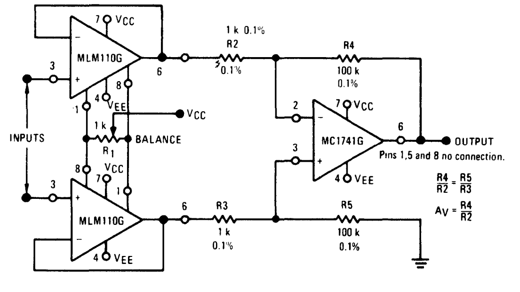


FIGURE 2 – DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MLM110G	MLM210G	MLM310G	Unit
Power Supply Voltage	V_{CC}(max) V_{EE}(max)	+18 -18	+18 -18	+18 -18	Vdc
Input Voltage (Note 1)	V_{IC}	± 15	± 15	± 15	Volts
Output Short Circuit Duration (Note 2)	T_{sc}		Indefinite		
Power Dissipation (Package Limitation) (Note 3)	P_D	500	500	500	mW
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C
Lead Temperature (soldering, t = 10 s)	T_S	300	300	300	°C

ELECTRICAL CHARACTERISTICS (See Note 4)

Characteristic	Symbol	MLM110G MLM210G			MLM310G			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}							mV
T_A = +25°C		–	1.5	4.0	–	2.5	7.5	
T_A = T_{low}* to T_{high}**		–	–	6.0	–	–	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	1.0	3.0	–	2.0	7.0	
T_A = T_{low} to T_{high}		–	–	10	–	–	10	
Input Resistance	r_i	10^{10}	10^{12}	–	10^{10}	10^{12}	–	ohms
Input Capacitance	C_i	–	1.5	–	–	1.5	–	pF
Large-Signal Voltage Gain (V_S = ± 15 V, V_O = +10 V)	A_{VS}							V/V
T_A = +25°C, R_L = 8.0 k ohms		0.999	0.9999	–	0.999	0.9999	–	
T_A = T_{low} to T_{high}, R_L = 10 k ohms		0.999	–	–	0.999	–	–	
Output Resistance	r_o							ohms
T_A = +25°C		–	0.75	2.5	–	0.75	2.5	
Small-Signal Bandwidth	BW	–	20	–	–	20	–	MHz
Slew Rate	SR	–	30	–	–	30	–	V/µs
Supply Current	I_D							mA
T_A = +25°C		–	3.9	5.5	–	3.9	5.5	
T_A = T_{high}		–	2.0	4.0	–	–	–	
Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$							µV/°C
-55°C ≤ T_A ≤ +85°C		–	6.0	–	–	–	–	
T_A = +125°C		–	12	–	–	–	–	
0°C ≤ T_A ≤ +70°C		–	–	–	–	10	–	
Output Voltage Swing	V_O							Volts
V_S = ± 15 V, R_L = 10 k ohms		± 10	–	–	± 10	–	–	
Supply Voltage Rejection Ratio	PSRR							dB
± 5/0 V ≤ V_S ≤ ± 18 V		70	80	–	70	80	–	

*T_{low} = -55°C for MLM110G
= -25°C for MLM210G
= 0°C for MLM310G

**T_{high} = +125°C for MLM110G
= +85°C for MLM210G
= +70°C for MLM310G

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Note 1. For supply voltages less than ± 15 volts, the absolute maximum input voltage is equal to the supply voltage.

Note 2. A continuous short-circuit duration capability is specified for MLM110G and MLM210G as follows: case temperatures up to +125°C and ambient temperatures up to +70°C; for the MLM310G up to +70°C case temperature and +55°C ambient temperature apply. A resistor (greater than 2.0 kilohms) must be inserted in series with the input when the amplifier is driven from a low impedance source, thus preventing damage when the output is shorted.

Note 3. The maximum junction temperature of the MLM110 is +150°C, for the MLM210G – +100°C, and for the MLM310G – +85°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance of 150°C/W – junction to ambient, or 45°C – junction to case.

Note 4. All listed specifications apply for ± 5.0 V ≤ V_S ≤ ±18 V and T_A = +25°C unless otherwise noted.

Note 5. Increased output swing under load can be obtained by connecting an external resistor between the booster and V_{EE} terminals (pins 4 and 5).

MLM111
MLM211
MLM311

VOLTAGE COMPARATORS

Product Preview

HIGHLY FLEXIBLE VOLTAGE COMPARATORS

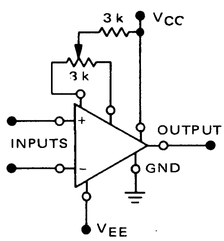
The ability to operate from a single power supply of 5.0 to 30 volts or ±15-volt split supplies, as commonly used with operational amplifiers, makes the MLM111/MLM211/MLM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the V_{CC} or the V_{EE} supply. This flexibility makes it possible to drive MDTL, MRTL, MTTL, or MOS logic. The output can also switch voltages to 50 volts at currents to 50 mA. Thus the MLM111/MLM211/MLM311 can be used to drive relays, lamps or solenoids.

HIGH PERFORMANCE VOLTAGE COMPARATORS

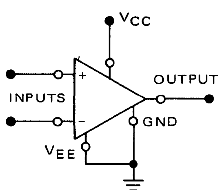
MONOLITHIC SILICON INTEGRATED CIRCUIT

SUGGESTED COMPARATOR DESIGN CONFIGURATIONS

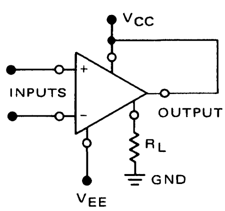
SPLIT POWER-SUPPLY with OFFSET BALANCE



SINGLE SUPPLY

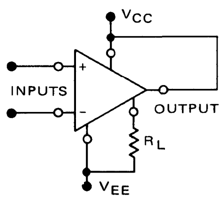


GROUND-REFERRED LOAD



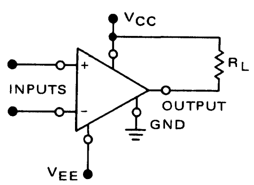
Input polarity is reversed when GND pin is used as an output.

LOAD REFERRED to NEGATIVE SUPPLY

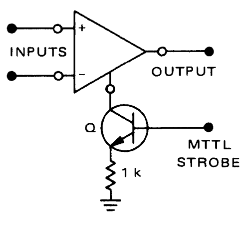


Input polarity is reversed when GND pin is used as an output.

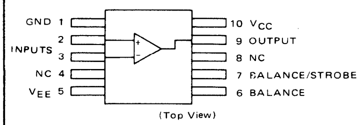
LOAD REFERRED to POSITIVE SUPPLY



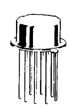
STROBE CAPABILITY

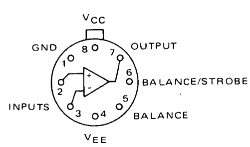


F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

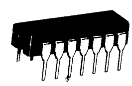


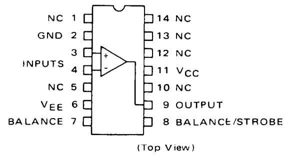
G SUFFIX
METAL PACKAGE
CASE 601



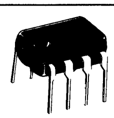


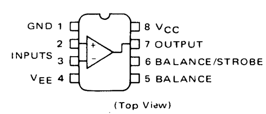
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116





P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MLM311 Only)





See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value MLM111 MLM211	Value MLM311	Unit
Total Supply Voltage	$V_{CC} + \lvert V_{EE} \rvert$	36	36	Vdc
Output to Negative Supply Voltage	$V_O - V_{EE}$	50	40	Vdc
Ground to Negative Supply Voltage	V_{EE}	30	30	Vdc
Differential Input Voltage	V_{ID}	±30	±30	Vdc
Input Voltage (See Note 1)	V_{in}	±15	±15	Vdc
Power Dissipation (Pkg. Limitation)	P_D			
Metal Package		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Flat Package		500		mW
Derate above T_A = +25°C		3.3		mW/°C
Plastic* and Ceramic Dual In-Line Packages		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Operating Temperatures Range	T_A			°C
MLM111		-55 to +125	–	
MLM211		-25 to +85	–	
MLM311		–	0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

*MLM311P1 only is available in the plastic dual in-line package.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MLM111 MLM211 Min	MLM111 MLM211 Typ	MLM111 MLM211 Max	MLM311 Min	MLM311 Typ	MLM311 Max	Unit
Input Offset Voltage (See Note 2.)	$\lvert V_{IO} \rvert$							mV
$R_S \leq 50$ kΩ, T_A = +25°C		–	0.7	3.0	–	2.0	7.5	
$R_S \leq 50$ kΩ, T_{low}* $\leq T_A \leq T_{high}$*		–	–	4.0	–	–	10	
Input Offset Current (See Note 2.)	$\lvert I_{IO} \rvert$							nA
T_A = +25°C		–	4.0	10	–	6.0	50	
$T_{low} \leq T_A \leq T_{high}$		–	–	20	–	–	70	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	60	100	–	100	250	
$T_{low} \leq T_A \leq T_{high}$		–	–	150	–	–	300	
Voltage Gain	A_V	–	200	–	–	200	–	V/mV
Response Time (See Note 3.)	t_{TLH}	–	200	–	–	200	–	ns
Saturation Voltage	V_{OL}							V
T_A = +25°C, $V_{ID} \leq -5.0$ mV, I_O = 50 mA		–	0.75	1.5	–	–	–	
$V_{ID} \leq -10$ mV, I_O = 50 mA		–	–	–	–	0.75	1.5	
$T_{low} \leq T_A \leq T_{high}$, $V_{CC} \geq 4.5$ V, V_{EE} = 0								
$V_{ID} \leq -6.0$ mV, $I_{sink} \leq 8.0$ mA		–	0.23	0.4	–	–	–	
$V_{ID} \leq -10$ mV, $I_{sink} \leq 8.0$ mA		–	–	–	–	0.23	0.4	
Strobe "On" Current	I_S	–	3.0	–	–	3.0	–	mA
Output Leakage Current	I_{OL}							
T_A = +25°C, $V_{ID} \geq 5.0$ mV, V_O = 35 V		–	0.2	10	–	–	–	nA
$V_{ID} \geq 10$ mV, V_O = 35 V		–	–	–	–	0.2	50	nA
$T_{low} \leq T_A \leq T_{high}$, $V_{ID} \geq 5.0$ mV, V_O = 35 V		–	0.1	0.5	–	–	–	μA
Input Voltage Range	V_{IR}							V
$T_{low} \leq T_A \leq T_{high}$		–	±14	–	–	±14	–	
Positive Supply Current	I_{CC}	–	+5.1	+6.0	–	+5.1	+7.5	mA
Negative Supply Current	I_{EE}	–	-4.1	-5.0	–	-4.1	-5.0	mA

*T_{low} = -55°C for MLM111
= -25°C for MLM211
= 0 for MLM311

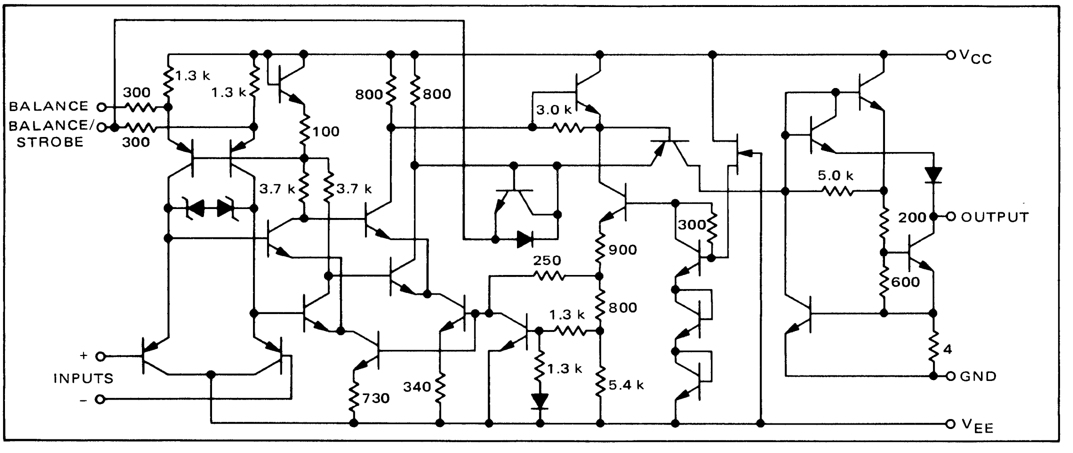
T_{high} = +125°C for MLM111
= +85°C for MLM211
= +70°C for MLM311

Note 1. This rating applies for ±15-volt supplies. The positive input voltage limit is 30 volts above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 volts below the positive supply, whichever is less.

Note 2. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0-mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.

Note 3. The response time specified is for a 100-mV input step with 5.0-mV overdrive.

FIGURE 1 – CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

FIGURE 2 – INPUT BIAS CURRENT and INPUT OFFSET CURRENT versus TEMPERATURE

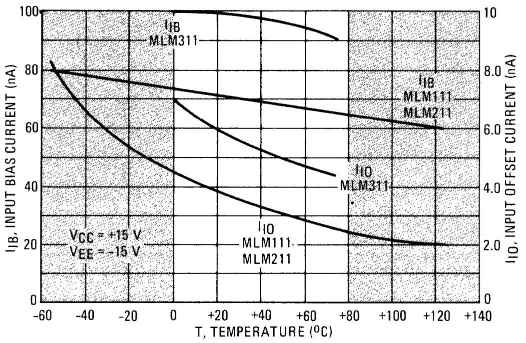


FIGURE 3 – COMMON-MODE LIMITS versus TEMPERATURE

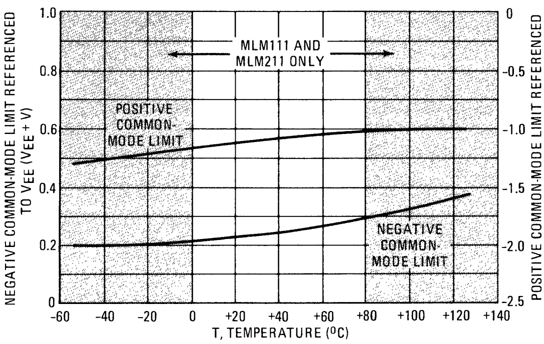


FIGURE 4 – OUTPUT SATURATION VOLTAGE versus OUTPUT CURRENT

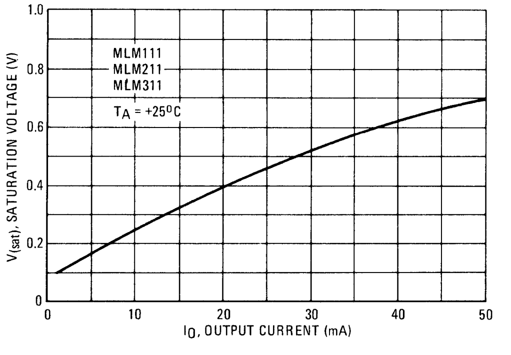
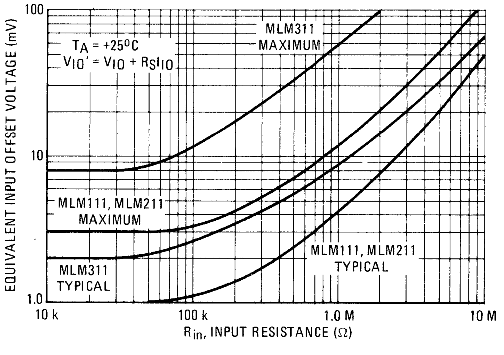


FIGURE 5 – EQUIVALENT OFFSET ERROR versus INPUT RESISTANCE



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APPLICATIONS INFORMATION

FIGURE 6 – ZERO-CROSSING DETECTOR DRIVING MOS LOGIC

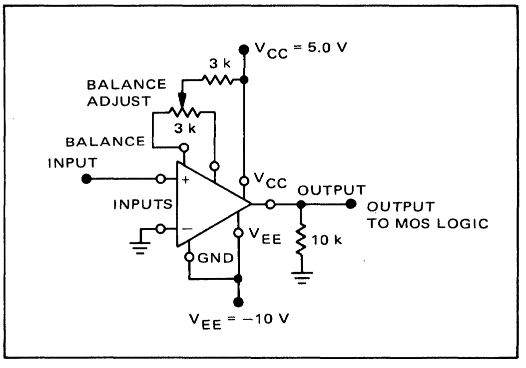
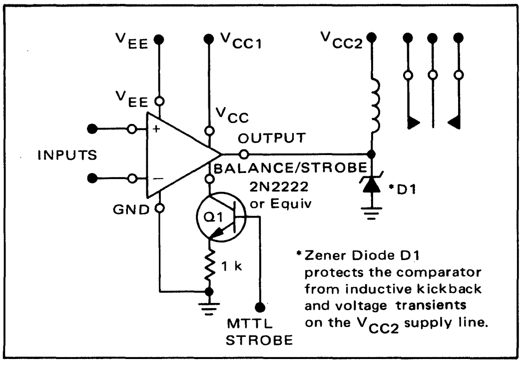


FIGURE 7 – RELAY DRIVER WITH STROBE CAPABILITY



MMH0026
MMH0026C

MOS CLOCK DRIVER

Specifications and Applications Information

DUAL MOS CLOCK DRIVER

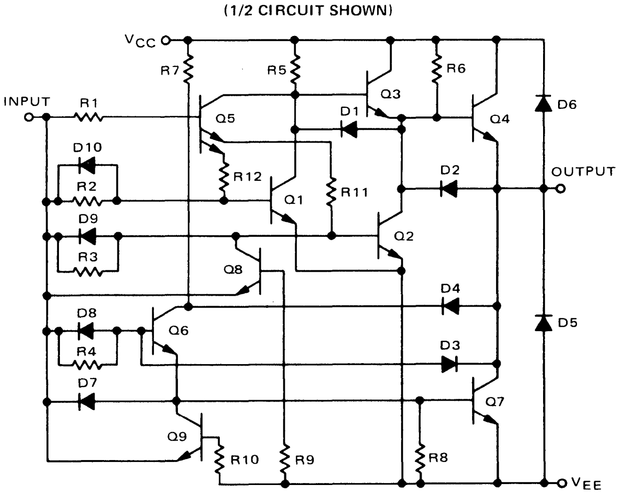
. . . designed for high-speed driving of highly capacitive loads in a MOS system.

- Fast Transition Times – 20 ns with 1000 pF Load
- High Output Swing – 20 Volts
- High Output Current Drive – ±1.5 Amperes
- High Repetition Rate – 5.0 to 10 MHz Depending on Load
- MTTL and MDTL Compatible Inputs
- Low Power Consumption when in MOS "0" State – 2.0 mW
- +5.0-Volt Operation for N-Channel MOS Compatibility

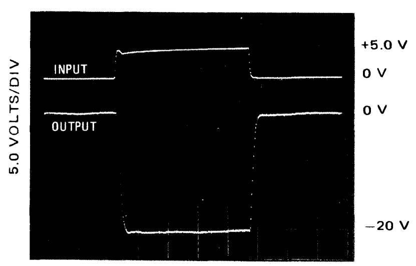
DUAL MOS CLOCK DRIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT

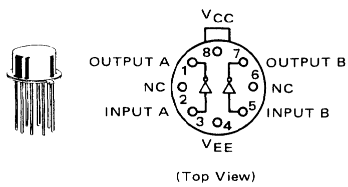
FIGURE 1 – CIRCUIT SCHEMATIC
(1/2 CIRCUIT SHOWN)



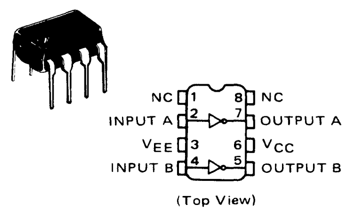
TYPICAL OPERATION
(R_S = 10 Ω, C_L = C_{in} = 1000 pF, f = 1.0 MHz,
PW = 500 ns, V_{CC} = 0 V, V_{EE} = –20 V)



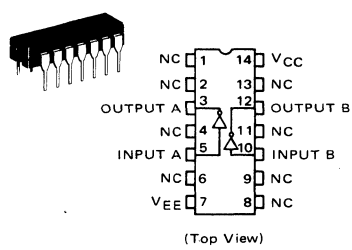
G SUFFIX
METAL PACKAGE
CASE 601
TO-99



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MMH0026C Only)



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



See Packaging Information Section for outline dimensions.

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
Differential Supply Voltage	$V_{CC}-V_{EE}$	+22			Vdc
Input Current	I_{in}	+100			mA
Input Voltage	V_{in}	V_{EE} + 5.5			Vdc
Peak Output Current	I_{Opk}	±1.5			A
		G Pkg.	L Pkg.	PI Pkg.	
Power Dissipation and Thermal Characteristics					
T_A = +25°C	P_D	680	1000	830	mW
Thermal Resistance, Junction to Air	θ_{JA}	220	150	150	°C/W
T_C = 25°C	P_D	2.1	3.0	1.8	W
Thermal Resistance, Junction to Case	θ_{JC}	70	50	70	°C/W
Junction Temperature	T_J	+175	+175	+150	°C
Operating Temperature Range	T_A				°C
MMH0026		-55 to +125	-55 to +125	–	
MMH0026C		0 to +85	0 to +85	0 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_{CC}-V_{EE}$ = 10 V to 20 V, C_L = 1000 pF, T_A = -55 to +125°C for MMH0026 and 0 to +85°C for MMH0026C for min and max values; T_A = +25°C for all typical values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Logic "1" Level Input Voltage $V_O = V_{EE}$ + 1.0 Vdc	V_{IH}	V_{EE} + 2.5	V_{EE} + 1.5	–	Vdc
Logic "1" Level Input Current $V_{in}-V_{EE}$ = 2.5 Vdc, $V_O = V_{EE}$ + 1.0 Vdc	I_{IH}	–	10	15	mA
Logic "0" Level Input Voltage $V_O = V_{CC}$ −1.0 Vdc	V_{IL}	–	V_{EE} + 0.6	V_{EE} + 0.4	Vdc
Logic "0" Level Input Current $V_{in}-V_{EE}$ = 0 Vdc, $V_O = V_{CC}$ -1.0 Vdc	I_{IL}	–	-0.005	-10	µA
Logic "0" Level Output Voltage	V_{OH}				Vdc
V_{CC} = +5.0 Vdc, V_{EE} = -12 Vdc, V_{in} = -11.6 Vdc		4.0	4.3	–	
$V_{in}-V_{EE}$ = 0.4 Vdc		V_{CC} -1.0	V_{CC} -0.7	–	
Logic "1" Level Output Voltage	V_{OL}				Vdc
V_{CC} = +5.0 Vdc, V_{EE} = -12 Vdc, V_{in} = -9.5 Vdc		–	-11.5	-11	
$V_{in}-V_{EE}$ = 2.5 Vdc		–	V_{EE} + 0.5	V_{EE} + 1.0	
"On" Supply Current $V_{CC}-V_{EE}$ = 20 Vdc, $V_{in}-V_{EE}$ = 2.5 Vdc	I_{CCL}	–	30	40	mA
"Off" Supply Current $V_{CC}-V_{EE}$ = 20 Vdc, $V_{in}-V_{EE}$ = 0 V	I_{CCH}	–	10	100	µA

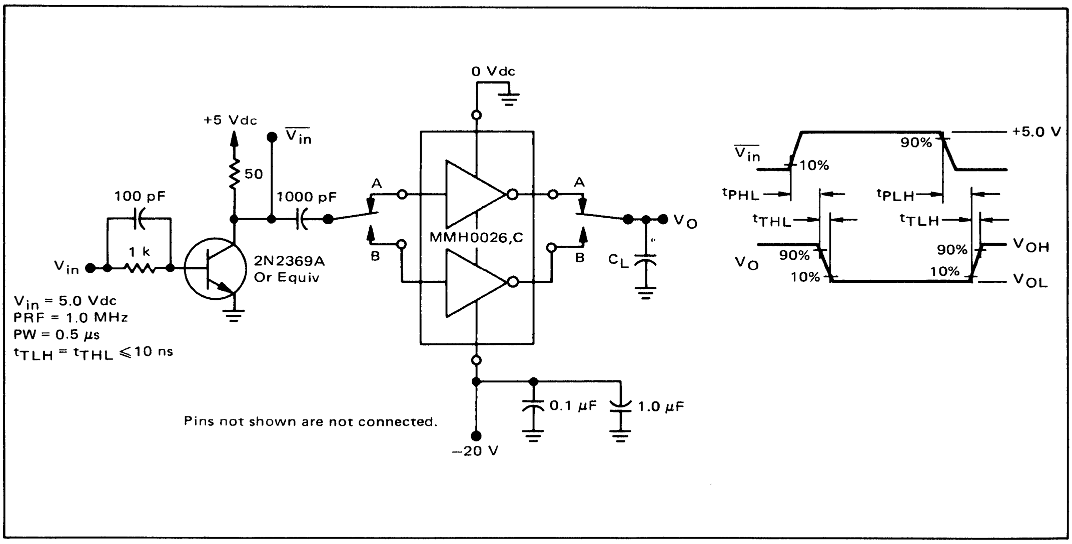
SWITCHING CHARACTERISTICS (See Figure 2.) ($V_{CC}-V_{EE}$ = 10 V to 20 V, C_L = 1000 pF, T_A = -55 to +125°C for MMH0026 and 0 to +85°C for MMH0026C for min and max values; T_A = +25°C for all typical values unless otherwise noted.)

Propagation Time					
High to Low	t_{PHL}	5.0	7.5	12	ns
Low to High	t_{PLH}	5.0	12	15	
Transition Time (High to Low)	t_{THL}				ns
$V_{CC}-V_{EE}$ = 17 Vdc, C_L = 250 pF		–	12	–	
$V_{CC}-V_{EE}$ = 17 Vdc, C_L = 500 pF		–	15	18	
$V_{CC}-V_{EE}$ = 20 Vdc, C_L = 1000 pF		–	20	35	
Transition Time (Low to High)	t_{TLH}				ns
$V_{CC}-V_{EE}$ = 17 Vdc, C_L = 250 pF		–	10	–	
$V_{CC}-V_{EE}$ = 17 Vdc, C_L = 500 pF		–	12	16	
$V_{CC}-V_{EE}$ = 20 Vdc, C_L = 1000 pF		–	17	25	

8

TEST CIRCUIT

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL APPLICATIONS

FIGURE 3 – AC-COUPLED MOS CLOCK DRIVER

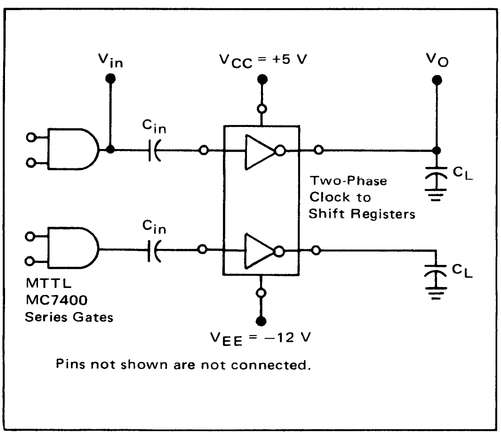
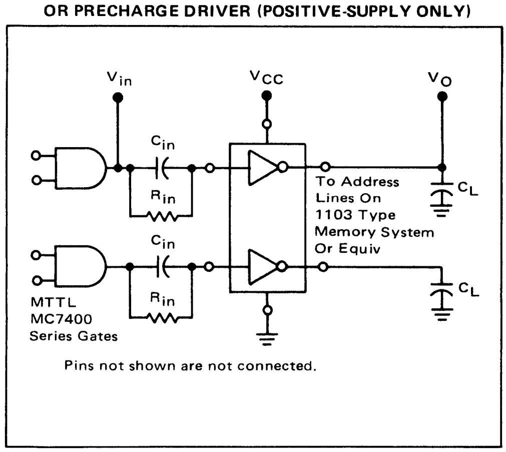


FIGURE 4 – DC-COUPLED RAM MEMORY ADDRESS OR PRECHARGE DRIVER (POSITIVE-SUPPLY ONLY)



8

TYPICAL CHARACTERISTICS

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 – INPUT CURRENT versus INPUT VOLTAGE

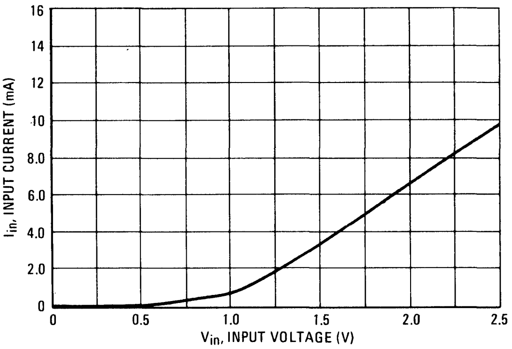


FIGURE 6 – SUPPLY CURRENT versus TEMPERATURE

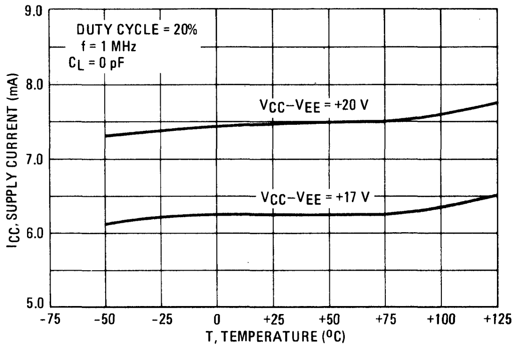


FIGURE 7 – OPTIMUM INPUT CAPACITANCE versus OUTPUT PULSE WIDTH

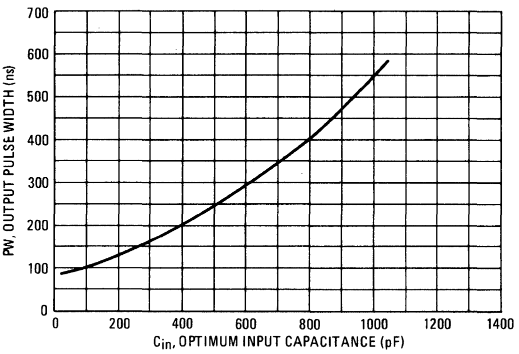


FIGURE 8 – TRANSITION TIMES versus LOAD CAPACITANCE

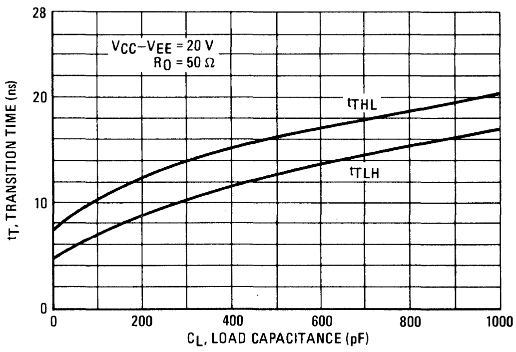


FIGURE 9 – PROPAGATION DELAY TIMES versus TEMPERATURE

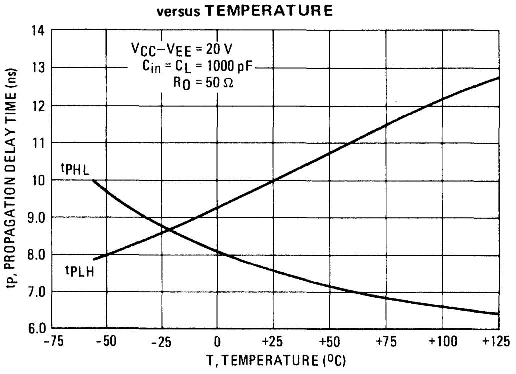
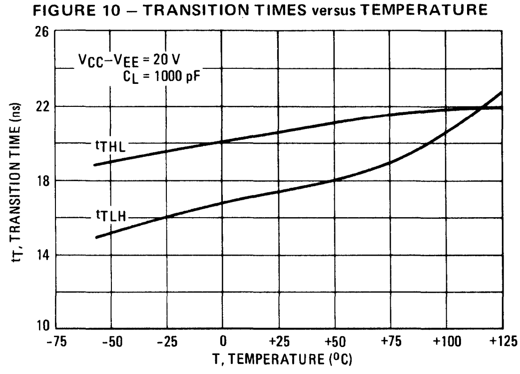


FIGURE 10 – TRANSITION TIMES versus TEMPERATURE



8

TYPICAL CHARACTISTICS (continued)

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 – TRANSITION TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

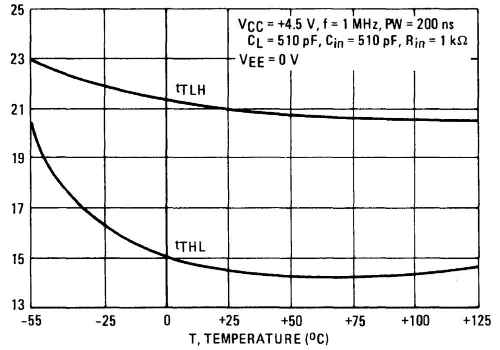


FIGURE 12 – PROPAGATION DELAY TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

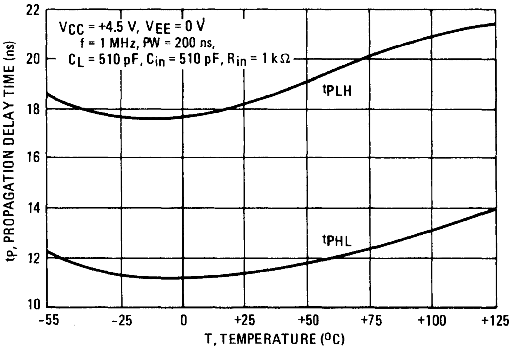


FIGURE 13 – DC-COUPLED SWITCHING RESPONSE versus R_{in} (See Figure 4.)

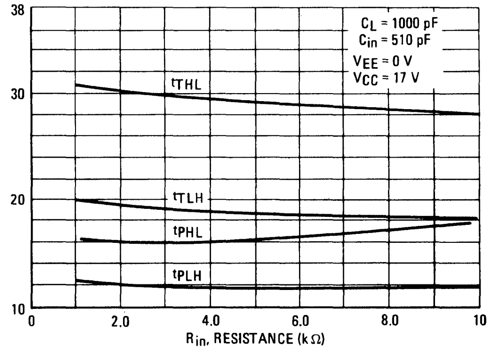


FIGURE 14 – DC-COUPLED SWITCHING versus C_{in} (See Figure 4.)

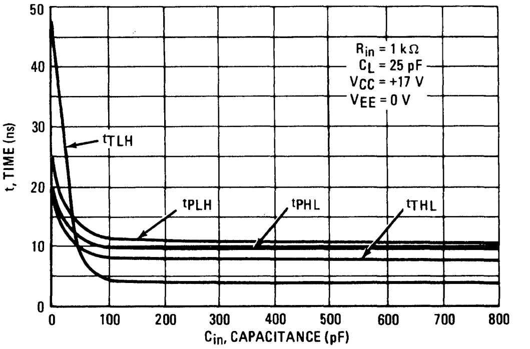


FIGURE 15 – MAXIMUM DC POWER DISSIPATION versus DUTY CYCLE (SINGLE DRIVER)

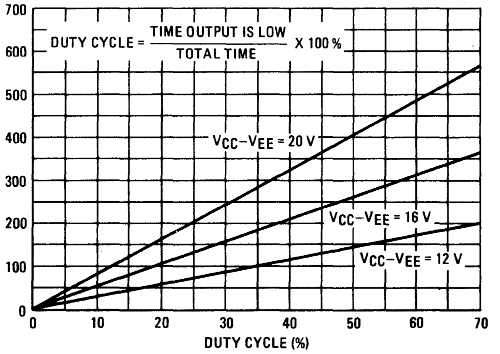
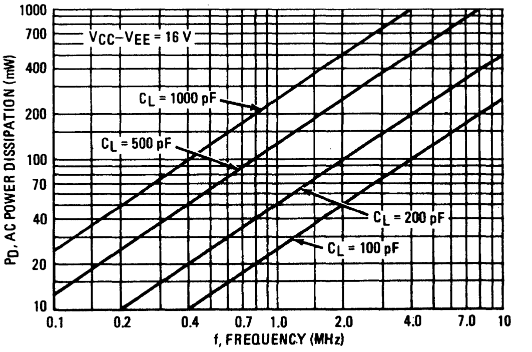


FIGURE 16 – AC POWER DISSIPATION versus FREQUENCY (SINGLE DRIVER)



8

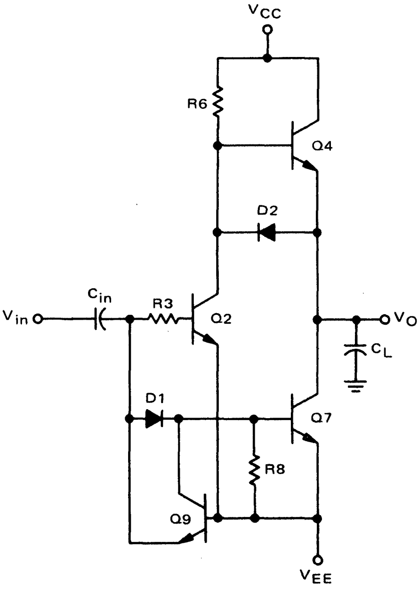
APPLICATIONS INFORMATION

OPERATION OF THE MMH0026

The simplified schematic diagram of MMH0026, shown in Figure 17, is useful in explaining the operation of the device. Figure 17 illustrates that as the input voltage level goes high, diode D1 provides an 0.7-volt "dead zone" thus ensuring that Q2 is turned "on" and Q4 is turned "off" before Q7 is turned "on". This prevents undesirable "current spiking" from the power supply, which would occur if Q7 and Q4 were allowed to be "on" simultaneously for an instant of time. Diode D2 prevents "zenering" of Q4 and provides an initial discharge path for the output capacitive load by way of Q2.

As the input voltage level goes low, the stored charge in Q2 is used advantageously to keep Q2 "on" and Q4 "off" until Q7 is "off". Again undesirable "current spiking" is prevented. Due to the external capacitor, the input side of C_{in} goes negative with respect to V_{EE} causing Q9 to conduct momentarily thus assuring rapid turn "off" of Q7.

FIGURE 17 – SIMPLIFIED SCHEMATIC DIAGRAM
(Ref.: Figure 1)



The complete circuit, Figure 1, basically creates Darlington devices of transistors Q7, Q4 and Q2 in the simplified circuit of Figure 17. Note in Figure 1 that when the input goes negative with respect to V_{EE}, diodes D7 through D10 turn "on" assuring faster turn "off" of transistors Q1, Q2, Q6 and Q7. Resistor R6 insures that the output will charge to within one V_{BE} voltage drop of the V_{CC} supply.

SYSTEM CONSIDERATIONS

Overshoot:

In most system applications the output waveform of the MMH0026 will "overshoot" to some degree. However, "overshoot" can be eliminated or reduced by placing a damping resistor in series with the output. The amount of resistance required is given by: $R_S = 2\sqrt{L/C_L}$ where L is the inductance of the line and C_L is the load capacitance. In most cases a series of damping resistor in the range of 10-to-50 ohms will be sufficient. The damping resistor also affects the transition times of the outputs. The speed reduction is given by the formula:

$t_{THL} \approx t_{TLH} = 2.2\ R_S\ C_L$ (R_S is the damping resistor).

Crosstalk:

The MMH0026 is sensitive to crosstalk when the output voltage level is high ($V_O \approx V_{CC}$). With the output in the high voltage level state, Q3 and Q4 are essentially turned "off". Therefore, negative-going crosstalk will pull the output down until Q4 turns "on" sufficiently to pull the output back towards V_{CC}. This problem can be minimized by placing a "bleeding" resistor from the output to ground. The "bleeding" resistor should be of sufficient size so that Q4 conducts only a few milliamperes. Thus, when noise is coupled, Q4 is already "on" and the line is quickly clamped by Q4. Also note that in Figure 1 D6 clamps the output one diode-voltage drop above V_{CC} for positive-going crosstalk.

Power Supply Decoupling:

The decoupling of V_{CC} and V_{EE} is essential in most systems. Sufficient capacitive decoupling is required to supply the peak surge currents during switching. At least a 0.1-μF to 1.0-μF low inductive capacitor should be placed as close to each driver package as the layout will permit.

Input Driving:

For those applications requiring split power supplies (V_{EE} < GND), ac coupling, as illustrated in Figure 3, should be employed. Selection of the input capacitor size is determined by the desired output pulse width. Maximum performance is attained when the voltage at

APPLICATIONS INFORMATION (continued)

the input of the MMH0026 discharges to just above the device's threshold voltage (about 1.5 V). Figure 7 shows optimum values for C_{in} versus the desired output pulse width. The value for C_{in} may be roughly predicted by:

$$C_{in} = (2 \times 10^{-3})\ (PW_O). \qquad (1)$$

For an output pulse width of 500 ns, the optimum value for C_{in} is:

$$C_{in} = (2 \times 10^{-3})\ (500 \times 10^{-9}) = 1000\ \text{pF}.$$

If single supply operation is required (V_{EE} = GND), then dc coupling as illustrated in Figure 4 can be employed. For maximum switching performance, a speed-up capacitor should be employed with dc coupling. Figures 13 and 14 show typical switching characteristics for various values of input resistance and capacitance.

POWER CONSIDERATIONS

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D\ (\theta_{JC} + \theta_{CA}) \qquad (2)$$

or

$$T_J = T_A + P_D\ (\theta_{JA}) \qquad (3)$$

where

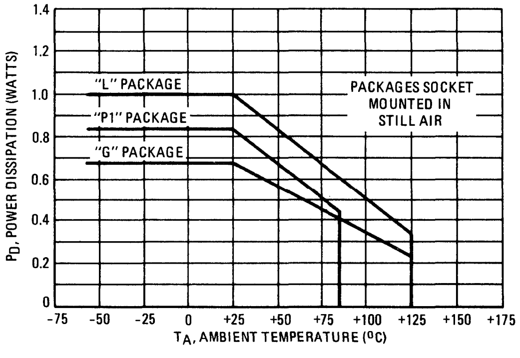
T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
θ_{JC} = thermal resistance, junction to case
θ_{CA} = thermal resistance, case to ambient
θ_{JA} = thermal resistance, junction to ambient.

Power Dissipation for the MMH0026 MOS Clock Driver: The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. This power dissipation, when substituted into equation (3), should not yield a junction temperature, T_J, greater than T_J(max) at the maximum encountered ambient temperature. T_J(max) is specified for three integrated circuit packages in the maximum ratings section of this data sheet.

TABLE 1 – THERMAL CHARACTERISTICS OF "G", "L" AND "P1" PACKAGES

PACKAGE TYPE (Mounted in Socket)	θ_{JA} (°C/W) Still Air		θ_{JC} (°C/W) Still Air	
	MAX	TYP	MAX	TYP
"G" (Metal Package)	220	175	70	40
"L" (Ceramic Package)	150	100	50	27
"P1" (Plastic Package)	150	100	70	40

FIGURE 18 – MAXIMUM POWER DISSIPATION versus AMBIENT TEMPERATURE (As related to package)



With these maximum junction temperature values, the maximum permissible power dissipation at a given ambient temperature may be determined. This can be done with equations (2) or (3) and the maximum thermal resistance values given in Table 1 or alternately, by using the curves plotted in Figure 18. If, however, the power dissipation determined by a given system produces a calculated junction temperature in excess of the recommended maximum rating for a given package type, something must be done to reduce the junction temperature.

There are two methods of lowering the junction temperature without changing the system requirements. First, the ambient temperature may be reduced sufficiently to bring T_J to an acceptable value. Secondly, the θ_{CA} term can be reduced. Lowering the θ_{CA} term can be accomplished by increasing the surface area of the package with the addition of a heat sink or by blowing air across the package to promote improved heat dissipation.

8

APPLICATIONS INFORMATION (continued)

The following examples illustrate the thermal considerations necessary to increase the power capability of the MMH0026.

Assume that the ceramic package is to be used at a maximum ambient temperature (T_A) of +70°C. From Table 1: $\theta_{JA}(max)$ = 150°C/watt, and from the maximum rating section of the data sheet: $T_J(max)$ = +175°C. Substituting the above values into equation (3) yields a maximum allowable power dissipation of 0.7 watts. Note that this same value may be read from Figure 18. Also note that this power dissipation value is for the device mounted in a socket.

Next, the maximum power consumed for a given system application must be determined. The power dissipation of the MOS clock driver is conveniently divided into dc and ac components. The dc power dissipation is given by:

$$P_{dc} = (V_{CC} - V_{EE}) \times (I_{CCL}) \times (\text{Duty Cycle}) \qquad (4)$$

$$\text{where } I_{CCL} = 40\text{ mA } \left(\frac{V_{CC} - V_{EE}}{20\text{ V}}\right).$$

Note that Figure 15 is a plot of equation (4) for three values of ($V_{CC}-V_{EE}$). For this example, suppose that the MOS clock driver is to be operated with V_{CC} = +16 V and V_{EE} = GND and with a 50% duty cycle. From equation (4) or Figure 15, the dc power dissipation (per driver) may be found to be 256 mW. If both drivers within the package are used in an identical way, the total dc power is 512 mW. Since the maximum total allowable power dissipation is 700 mW, the maximum ac power that can be dissipated for this example becomes:

$$P_{ac} = 0.7 - 0.512 = 188\text{ mW}$$

The ac power for each driver is given by:

$$P_{ac} = (V_{CC} - V_{EE})^2 \times f \times C_L \qquad (5)$$

where f = frequency of operation
C_L = load capacitance (including all strays and wiring).

Figure 16 gives the maximum ac power dissipation versus switching frequency for various capacitive loads with V_{CC} = 16 V and V_{EE} = GND. Under the above conditions, and with the aid of Figure 16, the safe operating area beneath Curve A of Figure 19 can be generated.

Since both drivers have a maximum ac power dissipation of 188 mW, the maximum ac power per driver becomes 94 mW. A horizontal line intersecting all the capacitance load lines at the 94 mW level of Figure 16 will yield the maximum frequency of operation for each of the capacitive loads at the specified power level. By using the previous formulas and constants, a new safe operating area can be generated for any output voltage swing and duty cycle desired.

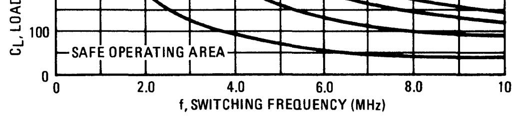
Note from Figure 19, that with highly capacitive loads, the maximum switching frequency is very low. The switching frequency can be increased by varying the following factors:

(a) decrease T_A
(b) decrease the duty cycle
(c) lower package thermal resistance θ_{JA}.

In most cases conditions (a) and (b) are fixed due to system requirements. This leaves only the thermal resistance θ_{JA} that can be varied.

Note from equation (2) that the thermal resistance is comprised of two parts. One is the junction-to-case thermal resistance (θ_{JC}) and the other is the case-to-ambient thermal resistance (θ_{CA}). Since the factor θ_{JC} is a function of the die size and type of bonding employed, it cannot be varied. However, the θ_{CA} term can be changed as previously discussed, see Page 7.

FIGURE 19 – LOAD CAPACITANCE versus FREQUENCY FOR "L" PACKAGE ONLY
(Both drivers used in identical way)



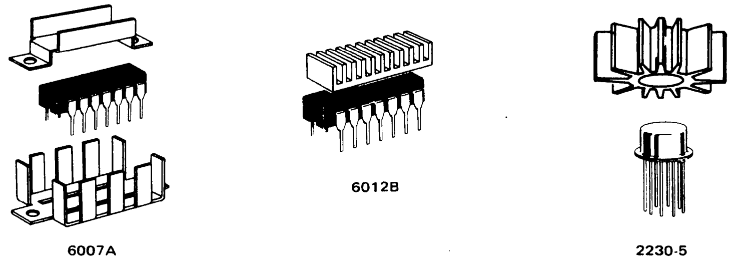
Heat Sink Considerations:

Heat sinks come in a wide variety of sizes and shapes that will accomodate almost any IC package made. Some of these heat sinks are illustrated in Figure 20. In the previous example, with the ceramic package, no heat sink and in a still air environment, $\theta_{JA}(max)$ was 150°C/W.

For the following example the Thermalloy 6012B type heat sink, or equivalent, is chosen. With this heat sink, the θ_{CA} for natural convection from Figure 21 is 44°C/W. From Table 1 $\theta_{JC}(max)$ = 50°C/W for the ceramic

APPLICATIONS INFORMATION (continued)

FIGURE 20 – THERMALLOY* HEAT SINKS



*Manufactured by Thermalloy Co. of Texas.

package. Therefore, the new θ_{JA}(max) with the 6012B heat sink added becomes:

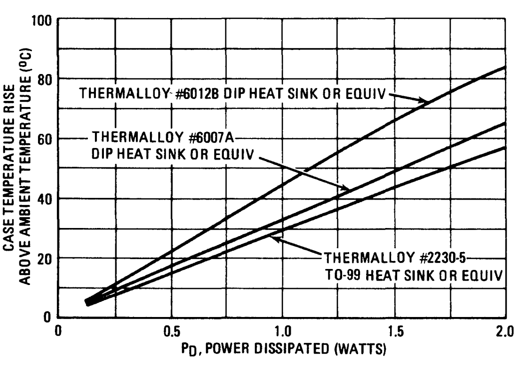
$$\theta_{JA}(\text{max}) = 50^{\circ}\text{C/W} + 44^{\circ}\text{C/W} = 94^{\circ}\text{C/W}.$$

Thus the addition of the heat sink has reduced θ_{JA}(max) from 150°C/W down to 94°C/W. With the heat sink, the maximum power dissipation by equation (3) at T_A = +70°C is:

$$P_D = \frac{175^{\circ}\text{C} - 70^{\circ}\text{C}}{94^{\circ}\text{C/W}} = 1.11 \text{ watts.}$$

This gives approximately a 58% increase in maximum power dissipation. The safe operating area under Curve C of Figure 19 can now be generated as before with the aid of Figure 16 and equation (5).

FIGURE 21 – CASE TEMPERATURE RISE ABOVE AMBIENT versus POWER DISSIPATED USING NATURAL CONVECTION



Forced Air Considerations:

As illustrated in Figure 22, forced air can be employed to reduce the θ_{JA} term. Note, however, that this curve is expressed in terms of typical θ_{JA} rather than maximum θ_{JA}. Maximum θ_{JA} can be determined in the following manner:

From Table 1 the following information is known:

(a) $\theta_{JA}(\text{typ}) = 100^{\circ}\text{C/W}$
(b) $\theta_{JC}(\text{typ}) = 27^{\circ}\text{C/W}$

Since:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \tag{6}$$

Then:

$$\theta_{CA} = \theta_{JA} - \theta_{JC} \tag{7}$$

Therefore, in still air

$$\theta_{CA}(\text{typ}) = 100^{\circ}\text{C/W} - 27^{\circ}\text{C/W} = 73^{\circ}\text{C/W}$$

From Curve 1 of Figure 22 at 500 LFPM and equation (7),

$$\theta_{CA}(\text{typ}) = 53^{\circ}\text{C/W} - 27^{\circ}\text{C/W} = 26^{\circ}\text{C/W}.$$

Thus θ_{CA}(typ) has changed from 73°C/W (still air) to 26°C/W (500 LFPM), which is a decrease in typical θ_{CA} by a ratio of 1:2.8. Since the typical value of θ_{CA} was reduced by a ratio of 1:2.8, θ_{CA}(max) of 100°C/W should also decrease by a ratio of 1:2.8.

This yields an θ_{CA}(max) at 500 LFPM of 36°C/W.

Therefore, from equation (6):

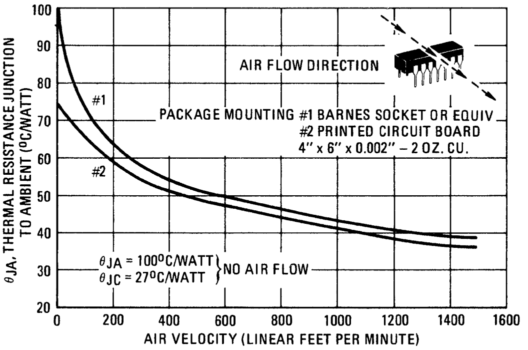
$$\theta_{JA}(\text{max}) = 50^{\circ}\text{C/W} + 36^{\circ}\text{C/W} = 86^{\circ}\text{C/W}.$$

Therefore the maximum allowable power dissipation at 500 LFPM and T_A = +70°C is from equation (3):

$$P_D = \frac{175^{\circ}\text{C} - 70^{\circ}\text{C}}{+86^{\circ}\text{C/W}} = 1.2 \text{ watts.}$$

APPLICATIONS INFORMATION (continued)

FIGURE 22 – TYPICAL THERMAL RESISTANCE (θ_{JA}) OF "L" PACKAGE versus AIR VELOCITY



As with the previous examples, the dc power at 50% duty cycle is subtracted from the maximum allowable device dissipation (P_D) to obtain a maximum P_{ac}. The safe operating area under Curve D of Figure 19 can now be generated from Figure 16 and equation (5).

Heat Sink and Forced Air Combined:

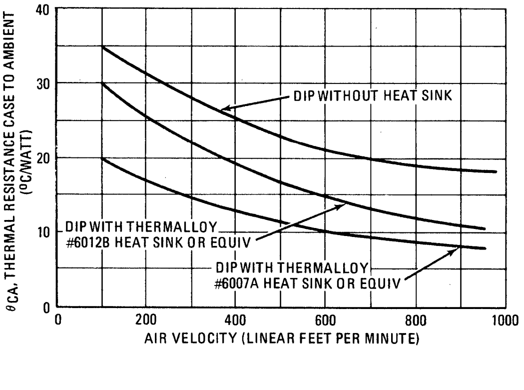
Some heat sink manufacturers provide data and curves of θ_{CA} for still air and forced air such as illustrated in Figure 23. For example the 6012B heat sink has an θ_{CA} = 17°C/W at 500 LFPM as noted in Figure 23. From equation (6):

$$\text{Max } \theta_{JA} = 50^{\circ}C/W + 17^{\circ}C/W = 67^{\circ}C/W$$

From equation (3) at T_A = +70°C

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{67^{\circ}C/W}\ 1.57 \text{ watts.}$$

FIGURE 23 – THERMAL RESISTANCE θ_{CA} versus AIR VELOCITY



As before this yields a safe operating area under Curve E in Figure 19.

Note from Table 1 and Figure 22 that if the 14-pin ceramic package is mounted directly to the PC board (2 oz. cu. underneath), that typical θ_{JA} is considerably less than for socket mount with still air and no heat sink. The following procedure can be employed to determine a safe operating area for this condition.

Given data from Table 1:

$$\text{typical } \theta_{JA} = 100^{\circ}C/W$$
$$\text{typical } \theta_{JC} = 27^{\circ}C/W$$

From Curve 2 of Figure 22, θ_{JA}(typ) is 75°C/W for a PC mount and no air flow. Then the typical θ_{CA} is 75°C/W – 27°C/W = 48°C/W. From Table 1 the typical value of θ_{CA} for socket mount is 100°C/W – 27°C/W = 73°C/W. This shows that the PC board mount results in a decrease in typical θ_{CA} by a ratio of 1:1.5 below the typical value of θ_{CA} in a socket mount. Therefore, the maximum value of socket mount θ_{CA} of 100°C/W should also decrease by a ratio of 1:1.5 when the device is mounted in a PC board. The maximum θ_{CA} becomes:

$$\theta_{CA} = \frac{100^{\circ}C/W}{1.5} = 66^{\circ}C/W \text{ for PC board mount}$$

Therefore the maximum θ_{JA} for a PC mount is from equation (6).

$$\theta_{JA} = 50^{\circ}C/W + 66^{\circ}C/W = 116^{\circ}C/W.$$

With maximum θ_{JA} known, the maximum power dissipation can be found and the safe operating area determined as before. See Curve B in Figure 19.

CONCLUSION

In most cases, heat sink manufacturer's publish only θ_{CA} socket mount data. Although θ_{CA} data for PC mounting is generally not available, this should present no problem. Note in Figure 22 that an air flow greater than 250 LFPM yields a socket mount θ_{JA} approximately 6% greater than for a PC mount. Therefore, the socket mount data can be used for a PC mount with a slightly greater safety factor. Also it should be noted that thermal resistance measurements can vary widely. These measurement variations are due to the dependency of θ_{CA} on the type environment and measurement techniques employed. For example, θ_{CA} would be greater for an integrated circuit mounted on a PC board with little or no ground plane versus one with a substantial ground plane. Therefore, if the maximum calculated junction temperature is on the border line of being too high for a given system application, then thermal resistance measurements should be done on the system to be absolutely certain that the maximum junction temperature is not exceeded.

LINEAR

INTEGRATED CIRCUITS

PACKAGING

9

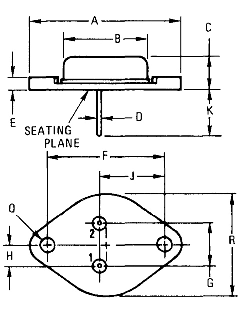
CASE OUTLINE DIMENSIONS

The packaging availability for each device type is indicated on the individual data sheets and the Linear Selector Guide. All of the outline dimensions for the packages are given in this section. Outline dimensions for non-encapsulated standard linear device chips, flip-chips, and beam-lead devices are found on the individual data sheets (see MCC, MCCF, or MCBC prefix followed by type number).

CASE 11 (TO-3)

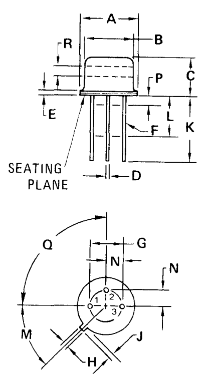
K Suffix
Metal Package
Weight ≈ 7.4 grams

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	--	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050



CASE 79 (TO-39)

G Suffix
Metal Package
Weight ≈ 0.96 gram

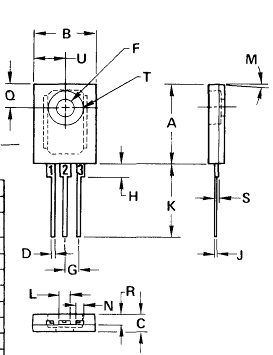


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC notes and dimensions apply.

CASE 199-04

P Suffix
Plastic Package
Weight ≈ 2.48 grams

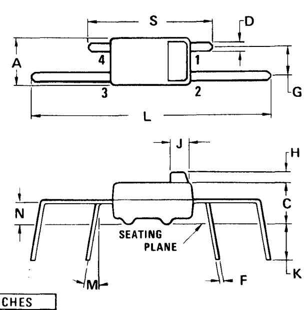


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0.152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

1. DIM "G" IS TO CENTER LINE OF LEADS.

CASE 206A

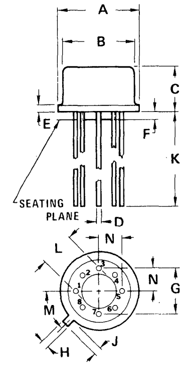
No Suffix
Plastic Package
Weight ≈ 0.2 gram



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.30	3.81	0.130	0.150
C	3.43	3.94	0.135	0.155
D	0.64	0.89	0.025	0.035
F	0.20	0.30	0.008	0.012
G	1.88	2.18	0.074	0.086
H	0.64	0.89	0.025	0.035
J	1.50	1.75	0.059	0.069
K	2.92	3.18	0.115	0.125
L	15.75	16.76	0.620	0.660
M	–	10°	–	10°
N	1.78	2.03	0.070	0.080
S	8.64	9.65	0.340	0.380

9

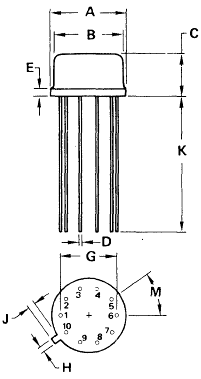
CASE 601
G Suffix
Metal Package
Weight ≈ 0.92 gram



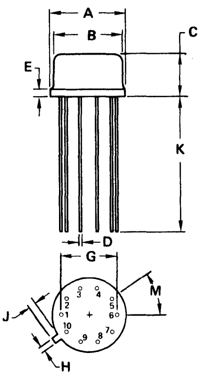
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.41	0.48	0.016	0.019
E	0.25	1.02	0.010	0.040
F	0.25	1.02	0.010	0.040
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
L	3.56	4.06	0.140	0.160
M	45° BSC		45° BSC	
N	2.41	2.67	0.095	0.105

CASE 602A
G Suffix
Metal Package
Weight ≈ 0.918 gram

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	–	4.57	–	0.180
D	0.41	0.48	0.016	0.019
E	–	1.02	–	0.040
G	5.84 BSC		0.230 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
M	36° BSC		36° BSC	



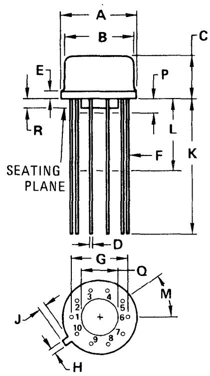
CASE 602B
G Suffix
Metal Package
Weight ≈ 0.918 gram



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	–	4.57	–	0.180
D	0.41	0.48	0.016	0.019
E	–	1.02	–	0.040
G	5.84 BSC		0.230 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	19.05	–	0.750	–
M	36° BSC		36° BSC	

NOTE:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

CASE 603 (TO-100)
G Suffix
Metal Package
Weight ≈ 0.918 gram



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.407	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	–	0.500	–
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	–	1.27	–	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

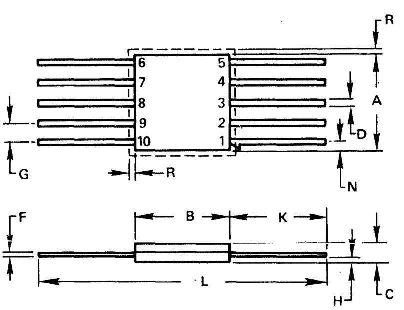
All JEDEC dimensions and notes apply

CASE 606 (TO-91)
F Suffix
Ceramic Package
Weight ≈ 0.127 gram

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	7.36	0.240	0.290
B	6.10	6.60	0.240	0.260
C	0.762	1.77	0.030	0.070
D	0.254	0.482	0.010	0.019
F	0.077	0.152	0.003	0.006
G	1.15	1.39	0.045	0.055
H	0.127	0.889	0.005	0.035
K	1.78	–	0.070	–
R	–	0.381	–	0.015

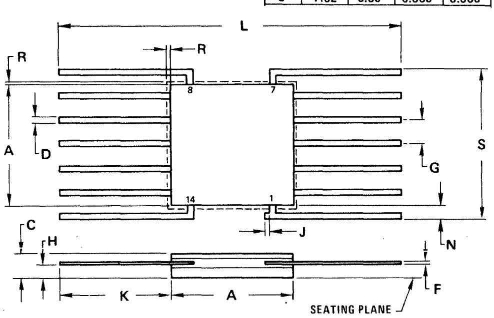
NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION (AT BODY)

All JEDEC dimensions and notes apply



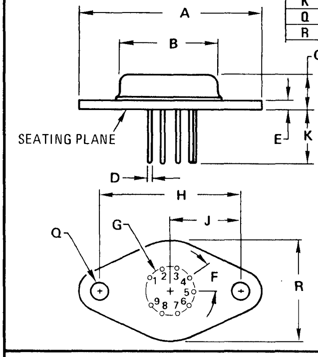
CASE 607
F Suffix
Ceramic Package
Weight ≈ 0.218 gram

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	6.60	0.240	0.260
C	0.76	1.78	0.030	0.070
D	0.33	0.48	0.013	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.30	0.89	0.012	0.035
J	–	0.38	–	0.015
K	6.35	9.40	0.250	0.370
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330



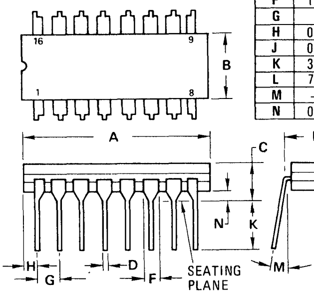
CASE 614
R Suffix
Metal Package
Weight ≈ 6.315 grams

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	31.80	–	1.252
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.81	0.028	0.032
E	1.27	1.90	0.050	0.075
F	36° BSC		36° BSC	
G	8.26 BSC		0.325 BSC	
H	24.33	24.43	0.958	0.962
J	12.17	12.22	0.479	0.481
K	9.14	–	0.360	–
Q	3.61	3.86	0.142	0.152
R	–	17.78	–	0.700



CASE 620
L Suffix
Ceramic Package
Weight ≈ 1.97 grams

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.99	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

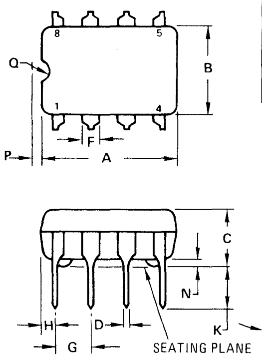


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION'
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT'
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL'

CASE 626
P or P1 Suffix
(See Data Sheet)
Plastic Package
Weight ≈ 0.446 gram

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51 NOM		0.020 NOM	
P	0.13	0.38	0.005	0.015
Q	0.76	1.02	0.030	0.040

DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

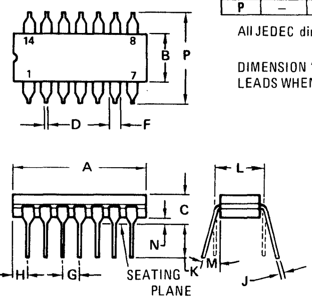


CASE 632 (TO-116)
L Suffix
Ceramic Package
Weight ≈ 1.954 grams

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

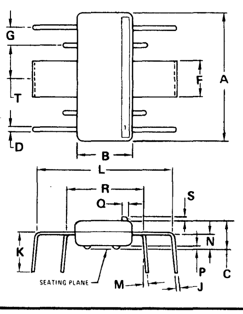
All JEDEC dimensions and notes apply.

DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



CASE 641A
No Suffix
Plastic Package
Weight ≈ 1.85 grams

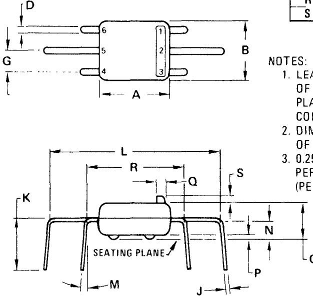
NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSIONS "L" AND "R" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. 0.25 mm (0.010) MAX FLASH PERMITTED AT PARTING LINE (PERIMETER).



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.92	19.18	0.745	0.755
B	7.49	7.75	0.295	0.305
C	4.06	4.57	0.160	0.180
D	0.76	1.27	0.030	0.050
F	5.84	6.35	0.230	0.250
G	2.03 BSC		0.080 BSC	
J	0.33	0.43	0.013	0.017
K	4.45	5.33	0.175	0.210
L	18.80	19.30	0.740	0.760
M	–	10°	–	10°
N	2.16	2.67	0.085	0.105
P	0.38	0.64	0.015	0.025
Q	1.52	1.78	0.060	0.070
R	11.68	12.19	0.460	0.480
S	0.64	0.89	0.025	0.035
T	5.08 BSC		0.200 BSC	

CASE 643A
No Suffix
Plastic Package
Weight ≈ 0.31 gram

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.60	7.11	0.260	0.280
B	5.33	5.84	0.210	0.230
C	3.43	4.06	0.135	0.160
D	0.64	0.89	0.025	0.035
G	2.03 BSC		0.080 BSC	
J	0.20	0.30	0.008	0.012
K	4.45	5.33	0.175	0.210
L	16.00	16.51	0.630	0.650
M	–	10°	–	10°
N	1.65	2.03	0.065	0.080
P	0.51	0.76	0.020	0.030
Q	1.50	1.75	0.059	0.069
R	8.89	9.40	0.350	0.370
S	0.64	0.89	0.025	0.035



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSIONS "L" AND "R" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. 0.25 mm (0.010) MAX FLASH PERMITTED AT PARTING LINE (PERIMETER)

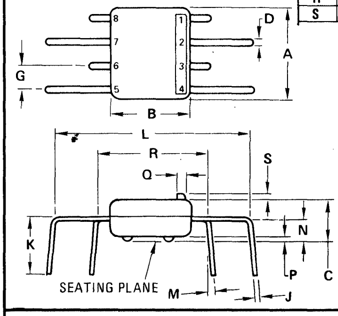
CASE 644A

No Suffix

Plastic Package

Weight ≈ 0.45 gram

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.37	7.87	0.290	0.310
B	6.60	6.86	0.260	0.270
C	3.43	4.06	0.135	0.160
D	0.64	0.89	0.025	0.035
G	2.03 BSC		0.080 BSC	
J	0.20	0.31	0.008	0.012
K	4.45	5.33	0.175	0.210
L	16.00	16.51	0.630	0.650
M	–	10°	–	10°
N	1.65	2.03	0.065	0.080
P	0.51	0.76	0.020	0.030
Q	1.50	1.75	0.059	0.069
R	8.89	9.40	0.350	0.370
S	0.64	0.89	0.025	0.035



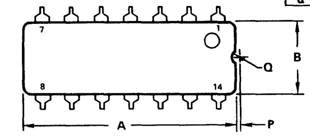
CASE 646

P Suffix

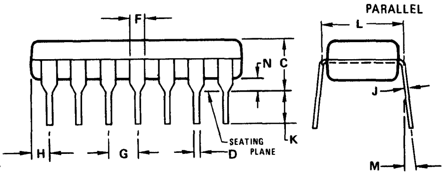
Plastic Package

Weight ≈ 0.911 gram

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



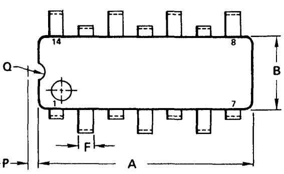
CASE 647

PQ Suffix

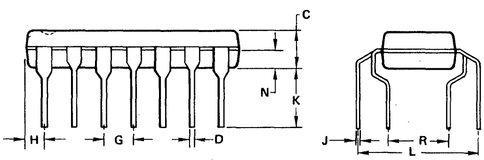
Plastic Package

Weight ≈ 0.911 gram

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	3.30	3.81	0.130	0.150
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	3.81	–	0.150	–
L	9.91	10.67	0.390	0.420
N	1.02	1.52	0.040	0.060
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030
R	4.83	5.59	0.190	0.220



NOTE:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION



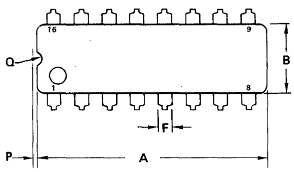
CASE 648

P Suffix

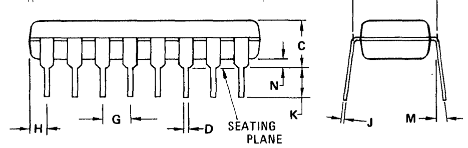
Plastic Package

Weight ≈ 0.93 gram

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC.	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030



NOTE:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

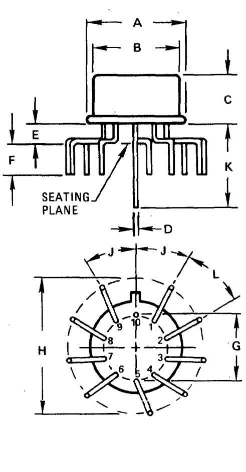


CASE 686

G Suffix

Metal Package

Weight ≈ 0.918 gram.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	–	4.57	–	0.180
D	0.406	0.483	0.016	0.019
E	1.78	2.54	0.070	0.100
F	3.05	3.81	0.120	0.150
G	5.84 TP		0.230 TP	
H	12.19 TP		0.480 TP	
J	31° TP		31° TP	
K	5.97	6.73	0.235	0.265
L	34° TP		34° TP	

*Seven places; (between all leads except 5 & 6, 9 & 10, 10 & 1)

LINEAR

INTEGRATED CIRCUITS

APPLICATION NOTES

10

APPLICATION NOTE ABSTRACTS

The application notes listed in this section have been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the AN number or numbers and send your request on your company letterhead to: Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

AN-204A The MC1530, MC1531 Integrated Operational Amplifiers

Two new high performance monolithic operational amplifiers feature exceptionally high input impedance and high open loop gain. This note describes the function of each stage in the circuit, methods of frequency compensating and DC biasing. Four applications are discussed: a summing circuit, an integrator, a DC comparator, and transfer function simulation.

AN-226 Thermal Measurements on Semiconductors

This note describes the techniques used by Motorola to obtain the thermal resistance of transistors, rectifiers, and thyristors.

AN-245A An Integrated Core Memory Sense Amplifier

This application note discusses core memories and related design considerations for a sense amplifier. Performance and environmental specifications for the amplifier design are carefully established so that the circuit will work with any computer using core memories. The final circuit design is then analyzed and measured performance is discussed. The amplifier features a small uncertainty region (6 mV max), adjustable voltage gain, and fast cycle time (0.5 μs).

AN-247A An Integrated Circuit RF-IF Amplifier

A new, versatile integrated circuit for RF-IF applications is introduced which offers high gain, extremely low internal feedback and wide AGC range. The circuit is a common-emitter, common-base pair (the cascade connection) with an AGC transistor and associated biasing circuitry. The amplifier is built on a very small die and is economically comparable to a single transistor, yet it offers performance advantages unobtainable with a single device. This application note describes the AC and DC operation of the circuit, a discussion of Y-parameters for calculating optimum power and voltage gain, and a variety of applications as an IF single-tuned amplifier, IF stagger-tuned amplifier, oscillator, video-audio amplifier and modulator. A discussion of noise figure is also included.

AN-248 The MC1533 Monolithic Operational Amplifier

This note introduces a high voltage monolithic operational amplifier featuring high open loop gain, large common mode input signal, and low drift. The function of each stage in the circuit is analyzed, and methods for frequency compensating the amplifier are discussed. DC biasing parameters are also examined. Four applications using the amplifier are discussed: a source follower, a twin tee filter and oscillator, a voltage regulator, and a high input impedance voltmeter.

AN-261A Transistor Logaritmic Conversion Using an Operational Amplifier

The design of a log amplifier using a common base transistor configuration as the feedback element of an integrated circuit operational amplifier circuit is discussed in this application note. Six decades of logarithmic conversion are obtained with less than 1% error of output voltage. The possible causes of error are discussed followed by two applications: direct multiplication of two numbers, and solution of the equation $Z = X^n$.

AN-273A More Value out of Integrated Operational Amplifier Data Sheets

The operational amplifier is rapidly becoming a basic building block in present day solid state electronic systems. The purpose of this application note is to provide a better understanding of the open loop characteristics of the amplifier and their significance to overall circuit operation. Also, each parameter is defined and reviewed with respect to closed loop considerations. The importance of loop gain stability and bandwidth is discussed at length. Input offset circuits are also reviewed with respect to closed loop operation.

AN-290B Mounting Procedure for, and Thermal Aspects of, Thermopad Plastic Power Devices

Many Motorola power devices are now available in the Plastic Thermopad packages. Three package types are presently available. This application note provides information concerning the handling and mounting of these packages, as well as information on some thermal aspects.

AN-299 An IC Wideband Video Amplifier with AGC

This application describes the use of the MC1550 as a wideband video amplifier with AGC. The analysis of a single stage amplifier with 28 dB of gain and 22 MHz bandwidth is given with the results extended to a 78 dB video amplifier with 10 MHz bandwidth.

AN-401 The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier

This application note discusses four different applications for the MC1554, along with a circuit description including DC characteristics, frequency response, and distortion. A section of the note is also devoted to package power dissipation calculations including the use of the curves on the power amplifier data sheet.

AN-403 Single Power Supply Operation of IC Op Amps

A split zener biasing technique that permits use of the MC1530/1531, MC1533, and MC1709 operational amplifiers and their restricted temperature counterparts MC1430/1431, MC1433 and MC1709C from a single power supply voltage is discussed in detail. General circuit considerations as well as specific AC and DC device considerations are outlined to minimize operating and design problems.

AN-404 A Wideband Monolithic Video Amplifier

This note describes the basic principles of AC and DC operation of the MC1552G and MC1553G, characteristics obtained as a function of the device operating modes, and typical circuit applications.

AN-407 A General Purpose IC Differential Output Operational Amplifier

This application note discusses four different applications for the MC1520 and a complete description of the device itself. The final sections of the note discuss such topics as operation from single and split power supplies, frequency compensation, and various feedback schemes.

AN-411 The MC1535 Monolithic Dual Op Amp

This note discusses two dual operational amplifier applications and an input compensation scheme for fast slew rate for the MC1535. A complete AC and DC circuit analysis is presented in addition to many of the pertinent electrical characteristics and how they might affect the system performance.

AN-421 Semiconductor Noise Figure Considerations

A summary of many of the important noise figure considerations related with the design of low noise amplifiers is presented. The basic fundamentals involving noise, noise figure, and noise figure-frequency characteristics are then discussed with the emphasis on characteristics common to all semiconductors. A brief introduction is made to various methods of data sheet presentation of noise figure and a summary is given for the various methods of measurement. A discussion of low noise circuit design, utilizing many of the previously discussed considerations, is included.

AN-432B A Monolithic Integrated FM Stereo Decoder System

This application note discusses the circuit approach that has been taken in the realization of the first monolithic integrated stereo multiplex decoder built for consumer usage, as well as some of the details concerning its incorporation in an FM stereo receiver.

AN-439 MC1539 Op Amp and its Applications

This application note discusses the MC1539, a second generation operational amplifier. The general use and operation of the amplifier is discussed with special mention made of improved operation over that of its first generation predecessor—the 709 type amplifier.

In addition to the detailed discussion on the DC and AC operation of the device, considerable emphasis is placed on operational performance. Many applications are offered to demonstrate the device capability, including a high frequency feed-forward scheme, and a source follower application.

AN-453 Zero Point Switching Techniques

This note discusses two unique pulse-type thyristor triggering circuits which meet the exact timing requirements of zero-point switching. They dissipate very little power and can be used with either sensitive or "shorted" gate devices.

AN-459 A Simple Technique for Extending Op Amp Power Bandwidth

The design of fast response amplifiers is presented without the use of "tricky" compensation procedures.

AN-460 Using Transient Response to Determine Operational Amplifier Stability

Analysis and an example are given for a technique that evaluates the stability of any particular feedback amplifier configuration by analyzing its response to a step-function input.

AN-471 Analog-to-Digital Conversion Techniques

The subject of analog-to-digital conversion and many of the techniques that can be used to accomplish it are discussed. The paper is written in general terms from a system point of view and is intended to assist the reader in determining which conversion technique is best suited for a given application.

AN-473 A Monolithic High-Power Series Voltage Regulator

This note discusses MC1560/MC1561 voltage regulator in terms of internal operation, development of these circuits, and how they are advantageously used in supply fabrication.

AN-474 The MC1541–A Gated Dual-Channel Sense Amplifier for Core Memories

The MC1541 sense amplifier can provide many magnetic core memory systems with lower system cycle times and a lower package count than with previous sense amplifiers. Circuit operation, design considerations, interface problems and typical applications are discussed.

AN-475 Using the MC1545–A Monolithic, Gated-Video Amplifier

Because of the unique design of the MC1545, this amplifier can be used as a gated video amplifier, sense amplifier, amplitude modulator, frequency shift keyer, balanced modulator, pulse amplifier, and many other applications. This note describes the AC and DC operation of the circuit and presents applications of the device as a video switch, amplitude modulator, balanced modulator, pulse amplifier, and others.

AN-480 Regulators Using Operational Amplifiers

The theory of op amp voltage regulator design is discussed. The problem areas associated with such designs are also detailed. The MC1560 is used as a OTC voltage reference in the op amp regulator designs that are shown. It is shown that regulation from 0.01% to 0.001% is possible.

AN-489 Analysis and Basic Operation of the MC1595

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance that is characteristic of the device. A few basic applications are given to assist the designer in system design.

AN-491 Gated Video Amplifier Applications The MC1545

This application note reviews the basic operation of the MC1545 and discusses some of the more popular applications for the MC1545. Included are several modulator types, temperature compensation of the active gate, AGC, gated oscillators, FSK systems, and single supply operation.

AN-498 Voltage and Current Boost Techniques Using The MC1560-61

The stability requirements for the current boosted MC1560-61 are discussed. Both internal and external compensation techniques are shown, along with heat-sink design information and typical circuits, including a self-oscillating switching regulator, and a voltage boost circuit.

AN-499 Shutdown Techniques for the MC1560-61/69 Monolithic Voltage Regulators

This note discusses the many ways one can use the shutdown control for the MC1560 Monolithic Voltage Regulator. These include logic control, short circuit detection, over voltage detection, junction temperature control, and thermal feedback. Also discussed, are current foldback and methods of restarting automatically from the shutdown state. The techniques discussed apply equally to the MC1560, MC1561, and MC1569 positive voltage regulators.

AN-500 Development, Analysis, and Basic Operation of the MC1560-61 Monolithic Voltage Regulators

In this note, the anlysis and basic operation of the MC1560 and the MC1561 voltage regulators are discussed. The tests and parameters used on the data sheet are considered, and the problems of specifying a monolithic voltage regulator are identified. The basic circuit configurations are shown with some insight for the typical performance one can expect.

AN-513 A High Gain Integrated Circuit RF-IF Amplifier with Wide Range AGC

This note describes the operation and application of the MC1590G, a monolithic RF-IF amplifier. Included are several applications for IF amplifiers, a mixer, video amplifiers, single and two-stage RF amplifiers.

AN-522 The MC1556 Operational Amplifier and its Applications

This application note discusses the MC1556, a second generation, internally compensated monolithic operational amplifier. Particular emphasis is placed on its distinct advantages over the early 709-type amplifier and the more recent 741-type amplifier.

Along with a description of its operation this note presents a discussion on various applications of the MC1556, highlighting its capabilities, and points out its characteristics so the reader may make effective use of the device.

AN-531 MC1596 Balanced Modulator

The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators for AM, SSB, and suppressed carrier AM; demodulators for the previously mentioned modulation forms; frequency doublers and HF/VHF double balanced mixers.

AN-533 Semiconductors for Plated-Wire Memories

An introduction to the operation and electrical characteristics of plated-wire memories is provided in conjunction with the applications of semiconductors that interface with the plated-wire memories.

Devices discussed include drivers, sense amplifiers, and decoders. Memory organization and memory-related semiconductor applications are also mentioned.

AN-543 Integrated Circuit IF Amplifiers for AM/FM and FM Radios

This application note discusses the design and performance of four IF amplifiers using integrated circuits. The IF amplifiers discussed include a high performance circuit, a circuit utilizing a quadrature detector, a composite AM/FM circuit, and an economy model for use with an external discriminator.

AN-545 Television Video IF Amplifier Using Integrated Circuits

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, MC1353 and the MC1330.

AN-547 A High-Speed Dual Differential Comparator, The MC1514

This application note discusses a few of the many uses for the MC1514 dual comparator. Many applications such as sense amplifiers, multivibrators, and peak level detectors are presented.

AN-552 The Control Engineer's Guide to IC Applications

This report is a guide to the use of integrated circuits, and as such provides practical solutions to a number of common problems encountered in circuits used for sensing and control which must operate in an industrial environment. The report is divided into two parts—digital ICs and linear ICs.

AN-553 A New Generation of Integrated Avionic Synthesizers

The need to generate signals of a multitude of different frequencies for avionic systems has resulted in complex solutions in the past. With the introduction of certain standard product integrated circuits, frequency synthesis using digital phase locked loop techniques presents a more practical solution. Several different types of servo phase locked loop systems are discussed and a practical design example is given. Results of design examples are presented along with possible applications.

AN-557 Analog-to-Digital Cyclic Converter

The A/D cyclic converter discussed in this note provides medium speed (1-5μs/ bit) and medium accuracy (7 or 8 bits) operation. A Cyclic converter uses the successive approximation technique in which an unknown analog input voltage is successively compared to a reference voltage to determine each bit of the digital output.

AN-559 Simple RAMP A/D Converter

A simple single ramp A/D converter which incorporates a calibration cycle to insure an accuracy of 12 bits is discussed. The circuit uses standard ICs and requires only one precision part—the reference voltage used in the calibration. This converter is useful in a number of instrumentation and measurement applications.

AN-564 An ADF Frequency Synthesizer Utilizing Phase Locked-Loop Integrated Circuits

This application note describes an IC phase locked-loop frequency synthesizer suitable for the local osciallator function in aircraft Automatic Direction Finder (ADF) equipment.

AN-587 Analysis and Design of the Op Amp Current Source

A voltage controlled current source utilizing an operational amplifier is discussed. Expressions for the transfer function and output impedances are developed using both the ideal and non-ideal op amp models. A section on analysis of the effects of op amp parameters and temperature variations on circuit performance is presented.

AN-588 A 20 kHz, 1kW Line Operated Inverter

This report describes a 1 kilowatt ultrasonic inverter for use in 208-volt, line-operated, computer main-frame power supply systems. This particular design has an output capability of 5 Volts at 200 Amperes.

AN-589 Generate Custom Waveforms Digitally

A method of generating custom waveforms using IC counters, a read-only memory, and a new monolithic D/A Converter is described. Performance of a prototype model is noted as well as possible applications.

AN-590 Servo Motor Drive Amplifiers

The design of transformerless, AC servo amplifiers using power darlington transistors and IC op amps are discussed. Two types of power amplifiers are illustrated, one using single +28 Volt power supply, the second using high voltage transistors in complementary configuration for operating directly off the line.

Four different op amp preamplifiers and 90 phase shifters are also described.

AN-594 A Frequency Synthesizer for Aircraft Automatic Direction Finding Systems

This report describes a phase locked loop frequency synthesizer suitable as the local oscillator in an ADF system. The synthesizer is designed for receivers using a 455 kHz IF system. Motorola application note AN-564 describes a similar system for receivers using a 10.7 MHz IF.

AN-597 Power Control Using the Zero Voltage Switch

This application note discusses the advantages of zero-voltage switching using the Motorola MFC8070. A temperature control circuit is shown which demonstrates the design flexibility of CMOS and optical-coupler combinations.

AN-599 Mounting Techniques For Metal Packaged Power Semiconductors

For cooler, more reliable operation, proper mounting procedures must be followed if the interface thermal resistance between the semiconductor package and heat sink is to be minimized. Discussed are aspects of preparing the mounting surface, using thermal compounds, and fastening techniques. Typical interface thermal resistance is given for a number of packages.

AN-702 High Speed Digital-To-Analog and Analog-To-Digital Techniques

A brief overview of some of the more popular techniques for accomplishing D/A and A/D techniques. In particular those techniques which lead themselves to high speed conversion.

AN-703 Designing Digitally-Controlled Power Supplies

This application note shows two design approaches; a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in any application.

AN-705 Pulse Width Modulation for Small DC Motor Control

This application note explains the use of modern pulse width modulation techniques as an efficient and economical solution to small DC motor control. Several practical circuit design approaches using discrete, operational amplifier and integrated circuit devices are described and illustrated.

AN-708 Line Driver and Receiver Considerations

This report discusses many line driver and receiver design considerations such as system description, definition of terms, important parameter measurements, design procedures and applications examples. An extensive line of devices is available from Motorola to provide the designer with the tools to implement the data transmission requirements necessary for almost every type of transmission system.

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