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MECL INTEGRATED CIRCUITS
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TECHNICAL DATA

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MECL INTEGRATED CIRCUITS

This book presents technical data for a broad line of MECL integrated circuits. Complete specifications for the individual monolithic circuits in the most popular MECL families are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent right of any manufacturer.

Series A

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GENERAL INFORMATION

SECTION I: HIGH SPEED LOGICS

For the purposes of this discussion, high speed logic has either or both of two characteristics:

a) toggle rates over 50 MHz

b) gate propagation delays under 6 ns

Only two types of standard high speed logic integrated circuits are commonly available in the marketplace: Schottky-clamped TTL logic (TTL-S), and non-saturating emitter-coupled logic (ECL).

Schottky-clamped TTL logic is similar to conventional TTL logic in its circuit configuration and operating characteristics. Conventional TTL is a saturated form of logic; that is, during turn-on, both the emitter-base and collector-base junctions of a transistor are forward biased, causing an accumulation of charged carriers in the base regions. Then, when the transistor is turned off, this charge must discharge through the collector. The finite time required for this charge to dissipate causes a delay in turning the transistor off. This "storage time" delay is an integral part of all saturated logic forms. Schottky-clamped TTL logic reduces storage time by means of Schottky-diodes between base-collector junctions. These diodes tend to keep the transistor out of saturation, but they also tend to increase the input capacitance of the Schottky-clamped transistor. Thus, while the speed of TTL-S is greater than that of TTL, due to a reduction in storage time, it is limited by the RC time constant of the transistor input.

Emitter-Coupled Logic, being non-saturating by design, completely avoids transistor storage time and its attendent speed limitation without the tradeoffs inherent in TTL-S. Gate delays of less than a nanosecond and operating frequencies approaching a gigahertz are currently feasible, and even these are not ultimate limits.

MECL PRODUCTS

Motorola offers four ECL logic families under its MECL trademark: MECL I, MECL II, MECL III, and MECL 10,000.

The MECL I family, introduced by Motorola in 1962, was the first monolithic integrated circuit line of emitter-coupled logic. Its propagation delay time of 8 ns and toggle rate of 30 MHz, though no longer considered state of the art, still places it above the speed capabilities of most saturated logic lines. It is still being produced in quantity for use in existing equipment designs, but several features of the more advanced MECL II, III, and MECL 10,000 families favor the use of these families in new designs.

In 1966, Motorola introduced MECL II with gate propagation delays of 4 ns, and flip-flop toggle rates of over 70 MHz. Speeds were later increased first to 120 MHz (typical) for the MC1027/MC1227 J-K flip-flop circuit, and then to 180 MHz (min.) for the MC1034 type D flip-flop.

Complex functions became available in MECL II when production capabilities shifted toward more complicated circuits. The family now has adders, data selectors, multiplexers, decoders, and a gas display tube decoder/driver.

Continuing development of MECL made possible an even faster logic family. As a result, MECL III was introduced in 1968. Its 1 ns gate propagation delays and greater than 500 MHz flip-flop toggle rates remain the industry leaders. For the moment, the very high speed capabilities of MECL III appear to have outstripped the general speed requirements of today's computer systems, however they are being utilized extensively in special high-speed sections of computers and high speed test and communication equipment. Motorola is continuing to develop and expand this product line.

For general purpose computer applications, trends in large high-speed systems showed the need for an easy-to-use logic family with propagation delays on the order of 2 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of MECL 10,000 is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy – MECL 10,000 gates use less than one-half the power of MECL III or high speed MECL II gates. Finally, low gate power and advanced circuit design techniques have permitted a new level of complexity for MECL circuits. For example, complexity of the MC10181 four bit arithmetic unit compares favorably to that of any bipolar integrated circuit on the market.

The basic MECL 10,000 Series has recently been expanded by a subset of devices with even greater speed. This additional series provides a selection of MECL 10,000 logic functions with flip-flop repetition rates up to 200 MHz min. The MECL 10,200 Series is meant for use in critical timing chains, and for clock distribution circuits. MECL 10,200 parts are otherwise identical to their 10,000 Series counterparts (subtract 100 from the MECL 10,200 part number to obtain the equivalent standard MECL 10,000 part number).

Although the basic design of all MECL families is the same, there are differences other than the speed and power capabilities. Comparisons of the key characteristics of each family are given in the tables of Figure 1.

MECL FAMILY COMPARISONS

Feature	MECL I	MECL II	MECL 10,000		MECL III
			10,100 Series 10,500 Series	10,200 Series 10,600 Series	
1. Gate Propagation Delay	8 ns	4 ns	2 ns	1.5 ns	1 ns
2. Gate Edge Speed	8.5 ns	4 ns	3.5 ns	2.5 ns	1 ns
3. Flip-Flop Toggle Speed (min)	30 MHz	165 MHz	125 MHz	200 MHz	500 MHz
4. Gate Power	31 mW	22 mW	25 mW	25 mW	60 mW
5. Speed-Power Product	250 pJ	88 pJ	50 pJ	37 pJ	60 pJ
6. Transmission Line Capability	No	On Some Devices	Yes	Yes	Yes
7. Wire-Wrap Capability	Yes	Yes	Yes	Yes	No
8. Output Pulldown Resistors	Yes	Optional	No	No	No
9. Input Pulldown Resistors	No	No	50 kΩ	50 kΩ	2 kΩ & 50 kΩ

FIGURE 1a – GENERAL CHARACTERISTICS

Ambient Temperature Range	MECL I	MECL II	MECL III	MECL 10,000
0°C to +75°C (commercial)	MC350	MC1000	–	–
-30°C to +85°C (industrial)	–	–	MC1600F,L	MECL 10,100 MECL 10,200
-55°C to +125°C (military)	MC300	MC1200	*	MECL 10,500 MECL 10,600

FIGURE 1b – OPERATING TEMPERATURE RANGE

*Planned for selected devices.

Package Style	MECL III	MECL 10,000
 Ceramic Flat Package (Hermetic)	Yes	Yes
 Plastic DIP	Yes (selected types)	Yes
 Ceramic DIP (Hermetic)	Yes	Yes

(For package dimensions see page 32)

FIGURE 1c – PACKAGE STYLES

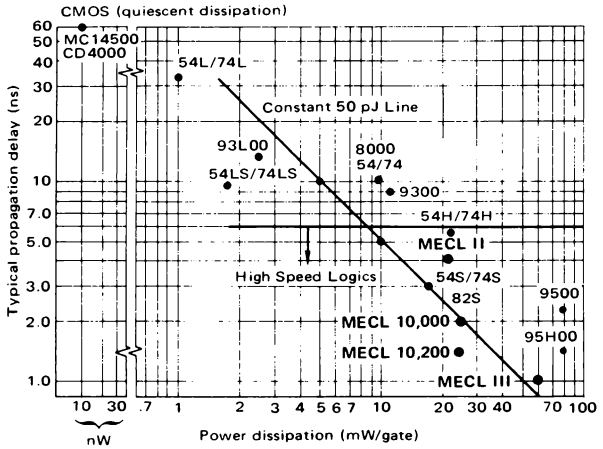


FIGURE 2a – SPEED-POWER CHARACTERISTICS OF MAJOR LOGIC LINES

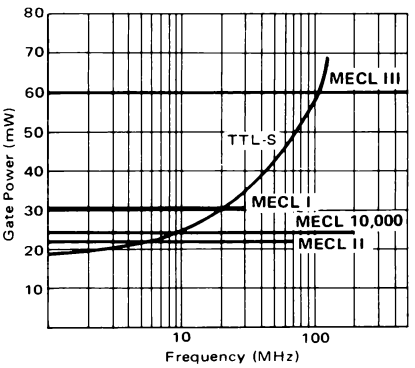


FIGURE 2b – POWER DISSIPATION versus FREQUENCY (MECL versus TTL-S)

MECL IN PERSPECTIVE

In evaluating a logic line, speed and power requirements are the obvious primary considerations. In Figure 2, today's major logic families are compared on the basis of these characteristics. But these are only the start of any comparative analysis. While the chart clearly shows that MECL and other ECL-type families are without peer in the speed category, with low power levels that rival some of the TTL lines, there are a number of other characteristics that make MECL highly desirable for systems implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power-supply design and reduces costs.

Low Cross-Talk due to low-current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10,000 series). A basic MECL 10,000 gate consumes less than 8 mW in on-chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No "Line Drivers" are listed in MECL families, because *every* device is a line driver.

Wire-ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted-pair transmission lines as long as 1000 feet.

MECL APPLICATIONS

The graduated speed ranges of the various MECL Families satisfy a great many digital system requirements. MECL 10,000 is a general-purpose, high-speed logic family specifically designed for smaller digital systems and peripherals as well as large computers. MECL III is recommended where its exceptionally high speed can buy needed system performance. It is used frequently in counter pre-scalers, high-speed digital communication systems, VHF phase-locked loops, high-speed digital processors, and high-speed timing chains in computers.

The compatibility among MECL families provides a bridge between system performance and system cost. Thus, the many functions and complex circuit members of the MECL 10,000 Line can be conveniently mixed with the very-high-speed functions of MECL III, in judicious combinations for system optimization.

BASIC CONSIDERATIONS FOR HIGH SPEED LOGIC DESIGN

High-speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium-speed systems, become highly important at state-of-the-art speeds.
2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.
3. The possibility of "crosstalk" between adjacent signal leads is proportionately increased in high speed systems.
4. Electrical noise generation and pick-up are more detrimental at higher speeds.

In general, these four characteristics are speed- and frequency-dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect-wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent "gate delay" is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10,000 Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state-of-the-art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At extreme speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 3). The solution, as in RF technology, is to employ "transmission-line" practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low-impedance, emitter-follower outputs of MECL circuits facilitate transmission-line practices without upsetting the voltage levels of the system.*

The increased affinity for crosstalk in high-speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high-speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. *In the design of MECL 10,000, the rise and fall times of the gate waveforms have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.*

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high-speed operation.

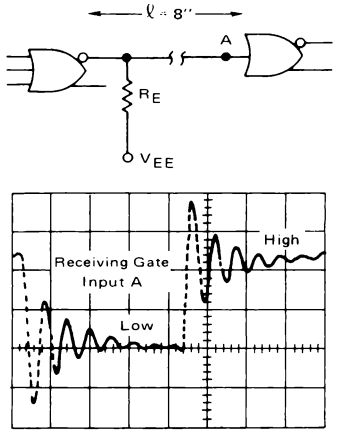


FIGURE 3a – UNTERMINATED TRANSMISSION LINE
(No Ground Plane Used)

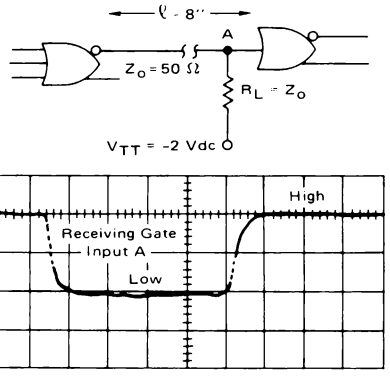


FIGURE 3b – PROPERLY TERMINATED TRANSMISSION LINE
(Ground Plane Added)

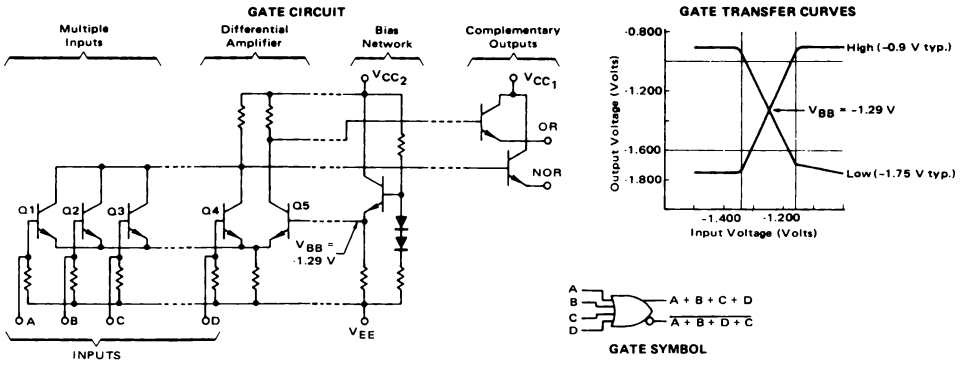


FIGURE 4 – MECL GATE STRUCTURE AND SWITCHING BEHAVIOR

CIRCUIT DESCRIPTION

The typical MECL circuit, Figure 4, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function.

Power-Supply Connections – Any of the power supply levels, V_{BB}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: V_{CC} = 0, V_{BB} = -1.15 to -1.3 V (depending on the specific MECL family), V_{EE} = -5.2 V.

System Logic Specifications – The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of V_L = -1.75 V to a HIGH state of V_H = -0.9 V with respect to ground. (These logic levels are valid for the MECL 10,000 and MECL III families. MECL I and II logic levels differ slightly.)

Positive logic is used when reference is made to logical "0's" or "1's." Then

"0" = -1.75 V = LOW

typical

"1" = -0.9 V = HIGH

Circuit Operation – Beginning with all logic inputs LOW (nominal -1.75 V), assume that Q1 through Q4 are cut off because their P-N base-emitter junctions are not conducting, and the forward-biased Q5 is conducting. Under these conditions, with the base of Q5 held at -1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than its base, or -2.09 V. (The 0.8 V differential is a characteristic of this P-N junction.) The base-to-emitter differential across Q1 - Q4 is then the difference between the common emitter voltage (-2.09 V) and the LOW logic level (-1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upward from the -1.75 V LOW state to the -0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common-emitter point rises from -2.09 V to -1.7 (one diode drop below the -0.9 V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at -1.29 V, the base-emitter voltage of Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 - Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 - Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

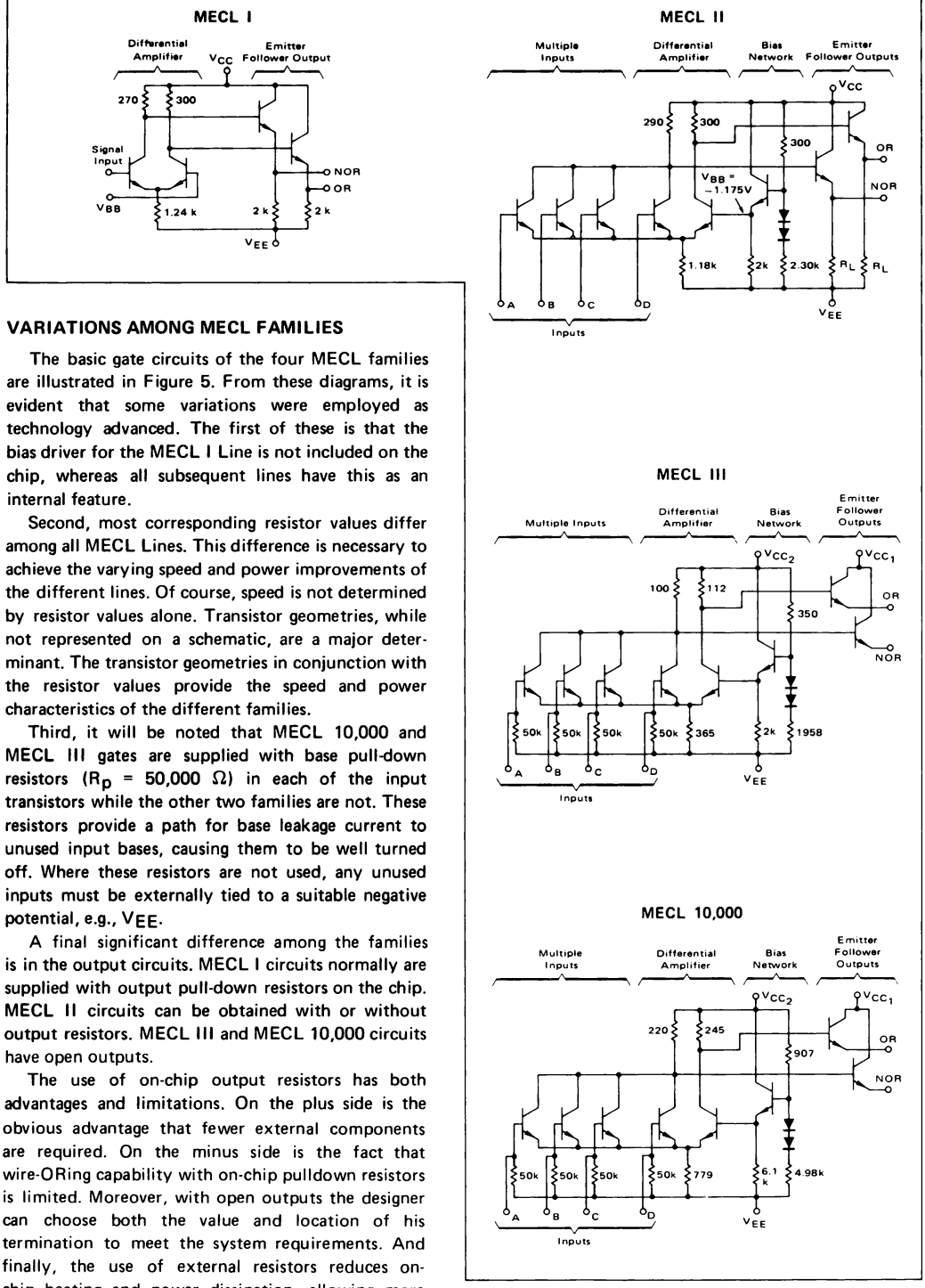


FIGURE 5 – BASIC GATE DIAGRAMS FOR THE MECL FAMILIES

VARIATIONS AMONG MECL FAMILIES

The basic gate circuits of the four MECL families are illustrated in Figure 5. From these diagrams, it is evident that some variations were employed as technology advanced. The first of these is that the bias driver for the MECL I Line is not included on the chip, whereas all subsequent lines have this as an internal feature.

Second, most corresponding resistor values differ among all MECL Lines. This difference is necessary to achieve the varying speed and power improvements of the different lines. Of course, speed is not determined by resistor values alone. Transistor geometries, while not represented on a schematic, are a major determinant. The transistor geometries in conjunction with the resistor values provide the speed and power characteristics of the different families.

Third, it will be noted that MECL 10,000 and MECL III gates are supplied with base pull-down resistors (R_D = 50,000 Ω) in each of the input transistors while the other two families are not. These resistors provide a path for base leakage current to unused input bases, causing them to be well turned off. Where these resistors are not used, any unused inputs must be externally tied to a suitable negative potential, e.g., V_{EE}.

A final significant difference among the families is in the output circuits. MECL I circuits normally are supplied with output pull-down resistors on the chip. MECL II circuits can be obtained with or without output resistors. MECL III and MECL 10,000 circuits have open outputs.

The use of on-chip output resistors has both advantages and limitations. On the plus side is the obvious advantage that fewer external components are required. On the minus side is the fact that wire-ORing capability with on-chip pulldown resistors is limited. Moreover, with open outputs the designer can choose both the value and location of his termination to meet the system requirements. And finally, the use of external resistors reduces on-chip heating and power dissipation, allowing more complex LSI and increasing chip life and reliability.

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

Current:

I_{BL} Base leakage current of a MECL expander input when at V_{EE}.

I_{CC} Total power supply current drawn from the positive supply by a MECL unit under test (I_C on older data sheets).

I_{CBO} Leakage current from input transistor on MECL devices without pulldown resistors when test voltage is applied.

I_{CCH} Current drain from V_{CC} power supply with all inputs at logic HIGH level.

I_{CCL} Current drain from V_{CC} power supply with all inputs at logic LOW level.

I_{CEX} Collector cut-off current (V_{CE} and $V_{BE(off)}$ as specified). For a MECL gate expander, this term signifies the total collector leakage current when all inputs are at the negative supply potential.

I_E Total power supply current drawn from a MECL test unit by the negative power supply.

I_F Forward diode current drawn from an input of a saturated logic-to-MECL translator when that input is at ground potential.

I_{in} Current into the input of the test unit when a maximum logic HIGH ($V_{IH\ max}$) is applied at that input.

$^*I_{INH}$ HIGH level node input current into an input node with a specified HIGH level ($V_{IH\ max}$) logic voltage applied to that node. (Same as I_{in} for positive logic.)

$^*I_{INL}$ LOW level node input current. The current flowing into an input node with a specified LOW level ($V_{IL\ min}$) logic voltage applied to that node.

I_L Load current that is drawn from a MECL circuit output when measuring the output HIGH level voltage.

$^*I_{OH}$ HIGH level output current: the current flowing into the output, at a specified HIGH level output voltage.

$^*I_{OL}$ LOW level output current: the current flowing into the output, at a specified LOW level output voltage.

I_{OS} Output short circuit current.

I_{out} Output current (from a device or circuit, under such conditions mentioned in context).

I_R Reverse current drawn from a transistor input of a test unit when V_{EE} is applied at that input.

I_{SC} Short-circuit current drawn from a translator saturating output when that output is at ground potential.

Voltage:

V_{BB} Reference bias supply voltage.

V_{BE} Base-to-emitter voltage drop of a transistor at specified collector and base currents.

V_{CB} Collector-to-base voltage drop of a transistor at specified collector and base currents.

V_{CC} General term for the most positive power supply voltage to a MECL device (usually ground, except for translator and interface circuits).

V_{CC1} Most positive power supply voltage (output devices). (Usually ground for MECL devices.)

V_{CC2} Most positive power supply voltage (current switches and bias driver)(usually ground for MECL devices).

V_{EE} Most negative power supply voltage for a circuit (usually -5.2 V for MECL devices).

V_F Input voltage for measuring I_F on TTL interface circuits.

V_{IH} Input logic HIGH voltage level (nominal value).

$^*V_{IH\ max}$ Maximum HIGH level input voltage: The most positive (least negative) value of high-level input voltage, for which operation of the logic element within specification limits is guaranteed.

V_{IHA} Input logic HIGH threshold voltage level.

$V_{IHA\ min}$ Minimum input logic HIGH level (threshold) voltage for which performance is specified.

$^*V_{IH\ min}$ Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Input logic LOW voltage level (nominal value).

$^*V_{IL\ max}$ Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{ILA} Input logic LOW threshold voltage level.

$V_{ILA\ max}$ Maximum input logic LOW level (threshold) voltage for which performance is specified.

$^*V_{IL\ min}$ Minimum LOW level input voltage: The least positive (most negative) value of LOW level input voltage for which opera-

*JEDEC, EIA, NEMA standard definition

tion of the logic element within specification limits is guaranteed.

V_{in} Input voltage (to a circuit or device).

V_{max} Maximum (most positive) supply voltage, permitted under a specified set of conditions.

$^*V_{OH}$ Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output.

V_{OHA} Output logic HIGH threshold voltage level.

$V_{OHA\ min}$ Minimum output HIGH threshold voltage level for which performance is specified.

$V_{OH\ max}$ Maximum output HIGH or high-level voltage for given inputs.

$V_{OH\ min}$ Minimum output HIGH or high-level voltage for given inputs.

$^*V_{OL}$ Output logic LOW voltage level: The voltage level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output.

V_{OLA} Output logic LOW threshold voltage level.

$V_{OLA\ max}$ Maximum output LOW threshold voltage level for which performance is specified.

$V_{OL\ max}$ Maximum output LOW level voltage for given inputs.

$V_{OL\ min}$ Minimum output LOW level voltage for given inputs.

V_{TT} Line load-resistor terminating voltage for outputs from a MECL device.

V_{OLS1} Output logic LOW level on MECL 10,000 line receiver devices with all inputs at V_{EE} voltage level. (This parameter is only valid for devices on whose data sheets it is specified).

V_{OLS2} Output logic LOW level on MECL 10,000 line receiver devices with all inputs open. (This parameter is only valid for devices on whose data sheets it is specified).

Time Parameters:

t+ Waveform rise time (LOW to HIGH), 10% to 90%, or 20% to 80%, as specified.

t- Waveform fall time (HIGH to LOW), 90% to 10%, or 80% to 20%, as specified.

t_r Same as t+

t_f Same as t-

t+- Propagation Delay, see Figure 12.

t-+ Propagation Delay, see Figure 12.

t_{pd} Propagation delay, input to output from the 50% point of the input waveform at

$t_{x\pm y\pm}$ pin x (falling edge noted by - or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by -, or rising edge noted by +). (Cf Figure 12.)

t_{x+} Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x with input conditions as specified.

t_{x-} Output waveform fall time as measured from 90% to 10% or 80% to 20% points on waveform (whichever is specified) at pin x, with input conditions as specified.

f_{tog} Toggle frequency of a flip-flop or counter device.

f_{shift} Shift rate for a shift register.

Temperature:

t_{stg} Maximum temperature at which device may be stored without damage or performance degradation.

T_J Junction (or die) temperature of an integrated circuit device.

T_A Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.

θ_{JA} Thermal resistance of an IC package, junction to ambient.

θ_{JC} Thermal resistance of an IC package, junction to case.

LFPM Linear feet per minute.

θ_{CA} Thermal resistance of an IC package, case to ambient.

Miscellaneous:

e_g Signal generator inputs to a test circuit.

TP_{in} Test point at input of unit under test.

TP_{out} Test point at output of unit under test.

D.U.T. Device under test.

Z_{out} Output impedance.

$^*P_D$ The total dc power applied to a device, not including any power delivered from the device to a load.

R_L Load Resistance.

R_T Terminating (load) resistor.

R_p An input pull-down resistor (i.e., connected to the most negative voltage).

*JEDEC, EIA, NEMA standard definition

GENERAL CHARACTERISTICS and SPECIFICATIONS

(See pages 7 and 8 for definitions of symbols and abbreviations)

In subsequent sections of this Data Book, the functional blocks of all four MECL lines are identified and characterized. Complete data sheets are provided for each of the functions in the MECL II, MECL III, and MECL 10,000 families*. To make these data sheets as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed in this section.

In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

LETTER SYMBOLS AND ABBREVIATIONS

Throughout this section, and in the subsequent data sheets, letter symbols and abbreviations will be used in discussing electrical characteristics and specifications. Recently, these symbols have been under scrutiny by various industry organizations, resulting in a number of additions and changes. The symbols used in this book, and their definitions, are listed on the preceeding two pages.

MAXIMUM RATINGS

The dc limit parameters beyond which the life of the devices may be impaired are given in the following table in Figure 6 for all MECL families. In addition, the table provides certain ac parameter limits which, if exceeded, will not destroy the devices, but could degrade the performance below that of the guaranteed specifications.

*Complete data sheets for MECL I functions are not included because this line is recommended only for replacement purposes. However, such data sheets are available and can be obtained by contacting your nearest Motorola representative.

MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. A typical transfer curve and associated data for all MECL families is shown in Figure 7a.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

The first set is obtained by applying test voltages, $V_{IL\ min}$ and $V_{IH\ max}$ (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between $V_{OL\ max}$ and $V_{OL\ min}$, and V_{OHmax} and V_{OHmin} specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, $V_{ILA\ max}$, is applied to the gate and the NOR and OR outputs are measured to see that they are above the $V_{OHA\ min}$ and below the $V_{OLA\ max}$ levels, respectively. Similar checks are made using the test input voltage $V_{IHA\ min}$.

The result of these specifications insures that:

a) The switching threshold ($\approx V_{BB}$) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;

b) Quiescent logic levels fall in the lightest shaded ranges;

c) Guaranteed noise immunity is met.

Figure 7b shows guaranteed 25°C logic level limits and switching thresholds for each of the MECL families, along with typical HIGH and LOW logic levels.

Of additional interest are the variations of these parameters at limit temperatures. These are given in the tables of Figure 8, for the MECL II, III, and 10,000 families.

All of these specifications assume -5.2 V power supply operation. Operation at other power-supply voltages is possible, but will result in further transfer curve changes. Transfer characteristic data obtained for a variety of supply voltages are shown in Figure 9. The table accompanying these graphs indicates the change rates of output voltages as a function of power supply voltages.

Variations in logic swing amplitude for MECL II, III, and 10,000 are shown in Figure 10.

NOISE MARGIN

"Noise margin" is a measure of a logic circuit's resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with

A. Limits beyond which device life may be impaired:

Characteristic		Symbol	Unit	Family: MECL I	MECL II	MECL III	MECL 10,000
Power Supply Voltage (V_{CC} = 0)		V_{EE}	Vdc	-10 to 0 V	-10 to 0 V	-8 to 0 V	-8 to 0 V
Base Input Voltage (V_{CC} = 0)		V_{in}	Vdc	0 to V_{EE}	0 to V_{EE}	0 to V_{EE}	0 to V_{EE}
Output Source Current	Continuous	I_o	mAdc	<20	<20	<40	<50
	Surge			–	–	–	<100
Storage Temperature		T_{stg}	°C	-55 to +150	MC1000 -55 to +150 MC1200 -55 to +150	-55 to +150	-55 to +150* -55 to +150**
Junction Operating Temperature[1]		T_J	°C	–	MC1000 < 150 MC1200 < 175	< 165†	< 165††

B. Limits beyond which performance may be degraded:

Operating Temperature Range	T_A	°C	MC300 -55 to +125 MC350 0 to +75	MC1000 0 to +75 MC1200 -55 to +125	MC1600 -30 to +85	-30 to +85* -55 to +125**
AC Fan-in (Expandable gates)	m	–	≤18	≤20	–	–
AC Fan-out	n	–	≤15	≤15	–	–
DC Fan-out	–	–	–	–	≤70	≤70
Power Supply Regulation	–	–	–	–	±10%	±10%

[1] Case must be < 150°C.

*MC10,100, MC10,200 **MC10,500, MC10,600

† Except MC1666-MC1671 < 145°C

†† Plastic Package < 150°C

FIGURE 6 – MAXIMUM RATINGS

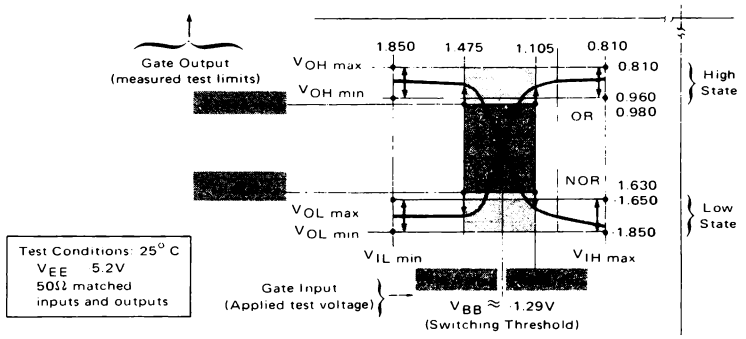


FIGURE 7a – MECL TRANSFER CURVES (MECL 10,000 example) and SPECIFICATION TEST POINTS

Inputs	Outputs	MECL I	MECL II	①② MECL III	MECL 10,000: 10,100 ① 10,200 ③	MECL 10,000: 10,500 ⑤ 10,600
V_{IL} min		V_{EE}	④	-1.850	-1.850	-1.850
V_{IH} max		0	-0.700	-0.810	-0.810	-0.720
	V_{OL} min	-1.750	-1.800	-1.850	-1.850	-1.850
	V_{OL} max	-1.465	-1.500	-1.620	-1.650	-1.620
	V_{OH} min	-0.795	-0.850 ⑥	-0.960	-0.960	-0.930
	V_{OH} max	-0.690	-0.700	-0.810	-0.810	-0.720
V_{ILA} max		–	-1.350	-1.485	-1.475	-1.475
V_{IHA} min		–	-1.025	-1.095	-1.105	-1.105
	V_{OLA} max	–	–	-1.600	-1.630	-1.600
	V_{OHA} min	–	-	-0.980	-0.980	-0.950
With suitable inputs:						
Typical Output HIGH State		-0.75	-0.75	-0.900	-0.900	-0.825
Typical Output LOW State		-1.55	-1.58	-1.750	-1.750	-1.725
Nominal V_{BB} (Switching Threshold)		-1.15	-1.175	-1.290	-1.290	-1.290

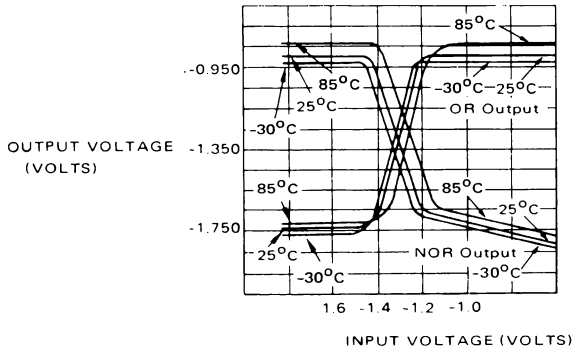
① Stabilized temperature, with ≥500 lfpm air flow. DIL package outputs terminated through 50 Ω resistor to -2.0 V.
② MC1660 DIL package.
③ MC10101 example.
④ See individual data sheets for V_{IL} min.
⑤ 100 Ω load to -2.0 V, stabilized temperature with ≥500 lfpm air flow.

General Conditions:
V_{EE} = -5.2 V
V_{CC} = ground
T_A = 25°C

FIGURE 7b – MECL LOGIC LEVEL SPECIFICATIONS (volts) 25°C

TRANSFER DATA FOR TEMPERATURE VARIATIONS

FIGURE 8 – TYPICAL TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE (see tables below for data)



MECL 10,000 FAMILY

Parameter (volts)	Series* (MC10101) 10,100 / 10,200		Series** (MC10501) 10,500 / 10,600	
	-30°C	+85°C	-55°C	+125°C
$V_{IH\ max}$ & $V_{OH\ max}$	-0.890	-0.700	-0.830	-0.580
$V_{OH\ min}$	-1.060	-0.890	-1.080	-0.825
$V_{OHA\ min}$	-1.080	-0.910	-1.100	-0.845
$V_{IHA\ min}$	-1.205	-1.035	-1.255	-1.000
$V_{ILA\ max}$	-1.500	-1.440	-1.510	-1.400
$V_{OLA\ max}$	-1.655	-1.595	-1.635	-1.525
$V_{OL\ max}$	-1.675	-1.615	-1.655	-1.545
$V_{IL\ min}$ & $V_{OL\ min}$	-1.890	-1.825	-1.920	-1.820

*Outputs loaded 50 Ω to -2.0 V. **Outputs loaded 100 Ω to -2.0 V.

MECL III (e.g. MC1660) FAMILY
Compatible with MECL 10,000

Parameter (volts)	DIP and Flat Package	
	-30°C	+85°C
$V_{IH\ max}$	-0.875	-0.700
$V_{OH\ max}$	-0.875	-0.700
$V_{OH\ min}$	-1.045	-0.890
$V_{OHA\ min}$	-1.065	-0.910
$V_{IHA\ min}$	-1.180	-1.025
$V_{ILA\ max}$	-1.515	-1.440
$V_{OLA\ max}$	-1.630	-1.555
$V_{OL\ max}$	-1.650	-1.575
$V_{IL\ min}$ & $V_{OL\ min}$	-1.890	-1.830

Note: Outputs loaded 50 Ω to - 2.0 V.

MECL II FAMILY

Parameter (Volts)	-55°C	0°C	+75°C	+125°C
$V_{IH\ max}$	-0.825	-0.740	-0.615	-0.530
$V_{OH\ max}$	-0.825	-0.735	-0.615	-0.530
$V_{OH\ min}$	-0.990	-0.895	-0.775	-0.700
$V_{IH\ min}$	-1.165	-1.070	-0.950	-0.875
$V_{IL\ max}$	-1.405	-1.350	-1.260	-1.205
$V_{OL\ max}$	-1.580	-1.525	-1.435	-1.380
$V_{OL\ min}$	-1.890	-1.830	-1.760	-1.720
$V_{IL\ min}$	$<V_{EE}$	$<V_{EE}$	$<V_{EE}$	$<V_{EE}$

Note: Noise margin = 175 mV.

TRANSFER DATA FOR POWER SUPPLY VARIATIONS

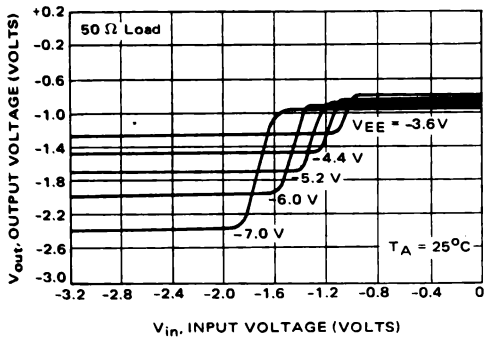


FIGURE 9a – MECL III/10,000 "OR"

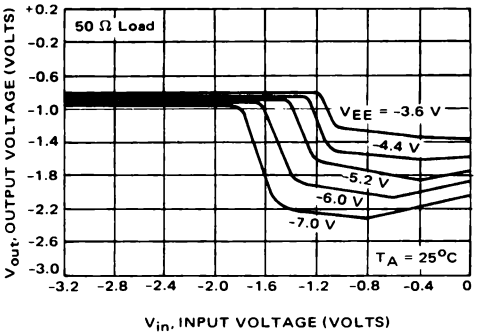


FIGURE 9b – MECL III/10,000 "NOR"

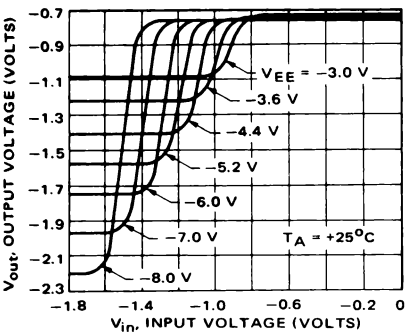


FIGURE 9c – MECL II "OR"

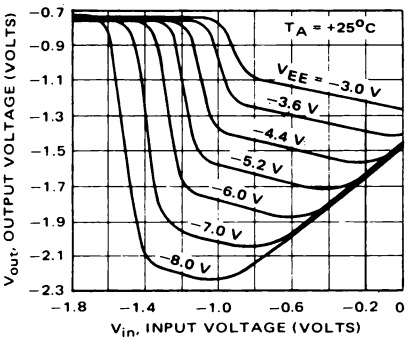


FIGURE 9d – MECL II "NOR"

Voltage	MECL II	MECL 10,000*	MECL III
$\Delta V_{OH}/\Delta V_{EE}$	0.015	0.016	0.033
$\Delta V_{OL}/\Delta V_{EE}$	0.230	0.250	0.27
$\Delta V_{BB}/\Delta V_{EE}$	0.115	0.148	0.14

*and subsets: 10,200; 10,500; 10,600.

FIGURE 9e – LEVEL CHANGE RATES

LOGIC SWING VARIATIONS WITH TEMPERATURE AND SUPPLY VOLTAGE

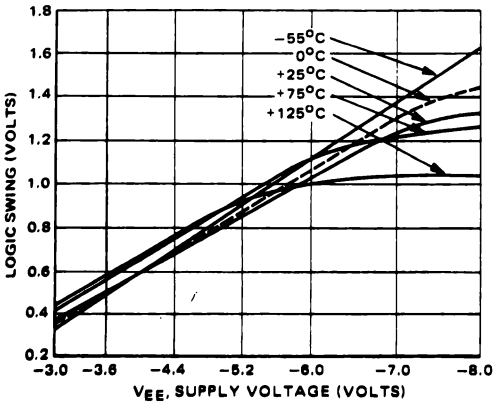


FIGURE 10a – MECL II

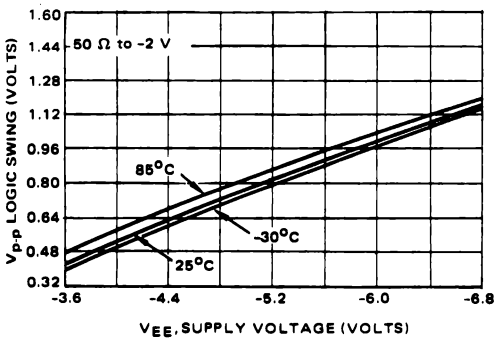
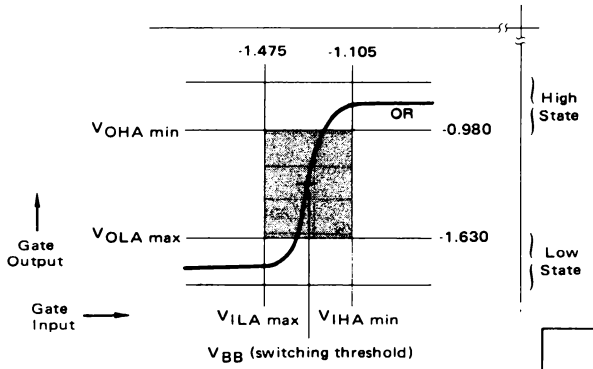
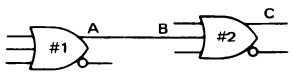


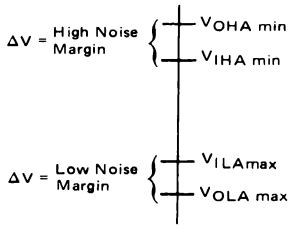
FIGURE 10b – MECL III/10,000



SPECIFICATION POINTS FOR DETERMINING NOISE MARGIN



ELEMENT 2 NOISE MARGIN MEASUREMENT POINTS FOR MECL GATES



NOISE MARGIN COMPUTATIONS

Family	Guaranteed Worst-Case dc Noise Margin	Typical dc Noise Margin
MECL II	0.175/0.150*	0.250/0.200*
All MECL 10,000	0.125	0.210
MECL III DIL and Flat Package	0.115	0.200

*Depending on part type. See selector guide or data sheet.

MECL NOISE MARGIN DATA

FIGURE 11

the "A" subscript (V_{OHA} min, V_{OLA} max, V_{IHA} min, V_{ILA} max) in the transfer characteristic curves.

Guaranteed noise margin (NM) is defined as follows:

$$NM_{HIGH\ LEVEL} = V_{OHA}\ min - V_{IHA}\ min$$

$$NM_{LOW\ LEVEL} = V_{ILA}\ max - V_{OLA}\ max.$$

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 11.

At a gate input (point B) equal to V_{ILA} max, MECL gate #2 can begin to enter the shaded transition region.

This is a "worst case" condition, since the V_{OLA} max specification point guarantees that no gate can enter the transition region before an input equal to V_{ILA} max is reached. Clearly then, V_{ILA} max is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case gate specifications)? From Figure 11 it can be observed that the V_{OLA} max specification insures that the LOW state OR output from gate 1 can be no greater than V_{OLA} max.

Note that V_{OLA} max is more negative than V_{ILA} max. Thus, with V_{OLA} max at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of V_{ILA} max on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from V_{OLA} max to V_{ILA} max. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10,000 levels shown:

$$NM_{LOW} = V_{ILA}\ max - V_{OLA}\ max$$
$$= -1.475\ V - (-1.630\ V)$$
$$= 155\ mV.$$

Similarly, for the HIGH state:

$$NM_{HIGH} = V_{OHA}\ min - V_{IHA}\ min$$
$$= -0.980\ V - (-1.105\ V)$$
$$= 125\ mV$$

Analogous results are obtained when considering the "NOR" transfer data.

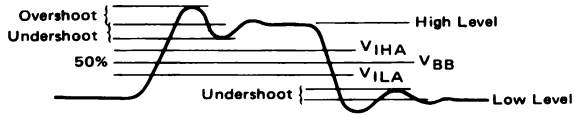
Note that these noise margins are absolute worst case conditions. The lesser of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

As shown in the table, typical noise margins are usually better than guaranteed – by about 75 mV.

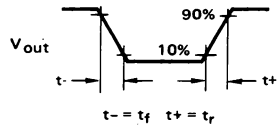
Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise-margin specifications, but also other circuit-related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise-margin specifications. This subject is discussed in greater detail in Application Notes AN-298 and AN-592.

AC OR TIME PARAMETERS

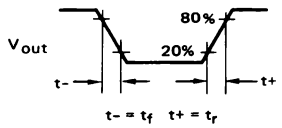
Time dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another (t+; t-). In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay. Since this terminology has varied over the years, and because the "conditions" associated with a particular parameter may differ among logic families, the common MECL waveform and propagation delay terminology are depicted in Figure 12. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for the MECL families are given in the curves of Figure 13.



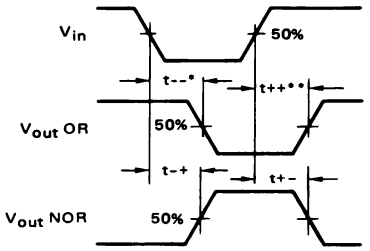
MECL WAVEFORM TERMINOLOGY



MECL II, III RISE AND FALL TIMES



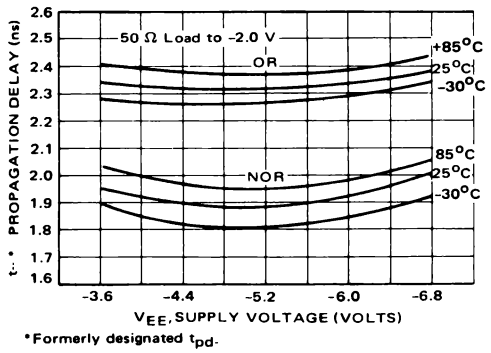
MECL 10,000 RISE AND FALL TIMES



*Designated t_{pd}- on older data sheets
**Designated t_{pd}+ on older data sheets

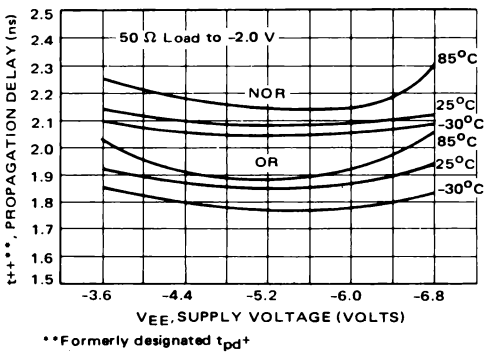
MECL PROPAGATION DELAY

FIGURE 12



*Formerly designated t_{pd}-

FIGURE 13a – TYPICAL PROPAGATION DELAY t--* versus V_{EE} and TEMPERATURE (MECL 10,000)



**Formerly designated t_{pd}+

FIGURE 13b – TYPICAL PROPAGATION DELAY t++** versus V_{EE} and TEMPERATURE (MECL 10,000)

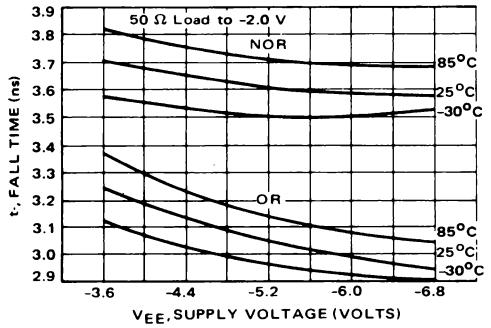


FIGURE 13c – TYPICAL FALL TIME (90% to 10%) versus TEMPERATURE and SUPPLY VOLTAGE (MECL 10,100)

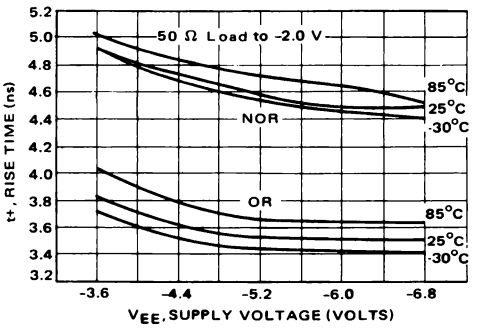


FIGURE 13d – TYPICAL RISE TIME (10% to 90%) versus TEMPERATURE and SUPPLY VOLTAGE (MECL 10,100)

TYPICAL DELAY TIMES FOR MECL II FAMILY

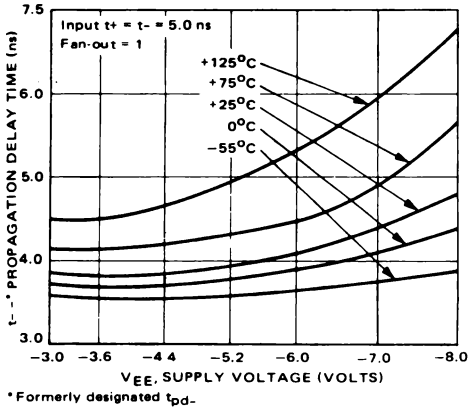


FIGURE 13e – TYPICAL PROPAGATION DELAY t- -* versus TEMPERATURE and SUPPLY VOLTAGE (MECL II)

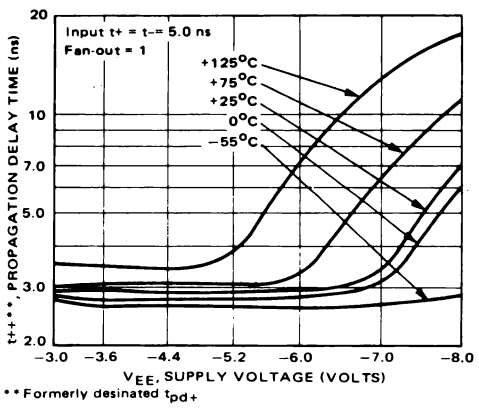


FIGURE 13f – TYPICAL PROPAGATION DELAY t++** versus TEMPERATURE and SUPPLY VOLTAGE (MECL II)

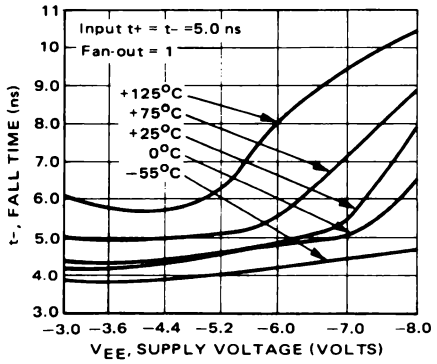


FIGURE 13g – TYPICAL FALL TIME (90% to 10%) versus TEMPERATURE and SUPPLY VOLTAGE (MECL II)

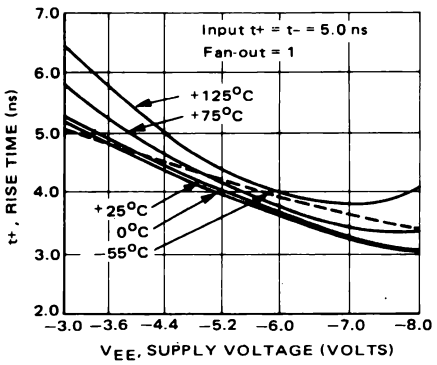


FIGURE 13h – TYPICAL RISE TIME (10% to 90%) versus TEMPERATURE and SUPPLY VOLTAGE (MECL II)

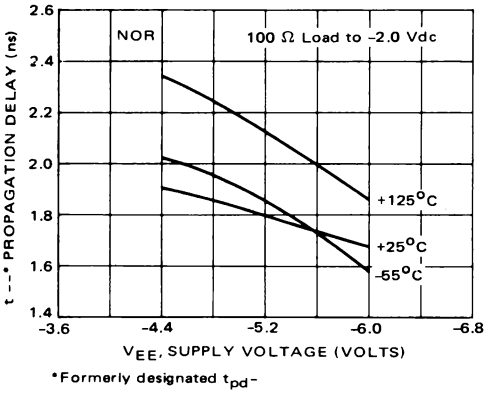


FIGURE 13i – TYPICAL PROPAGATION DELAY
t--* versus V_{EE} and TEMPERATURE
(MECL 10,500)

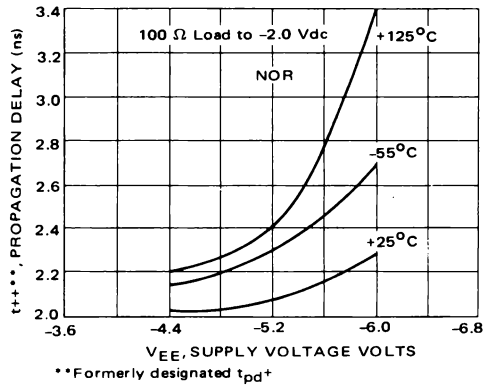


FIGURE 13j – TYPICAL PROPAGATION DELAY
t++** versus V_{EE} and TEMPERATURE
(MECL 10,500)

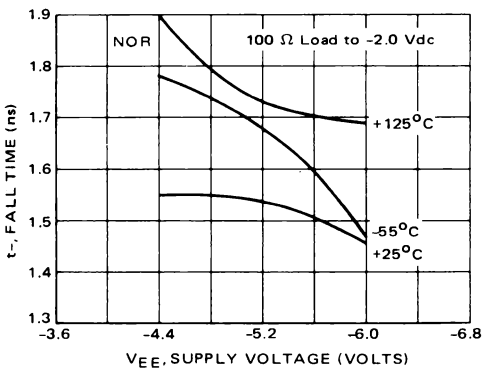


FIGURE 13k – TYPICAL FALL TIME
(80% to 20%) versus TEMPERATURE and
(MECL 10,500)

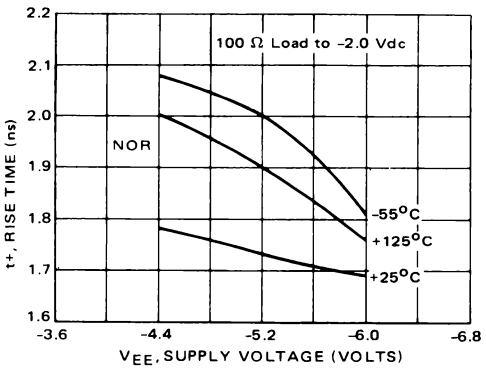
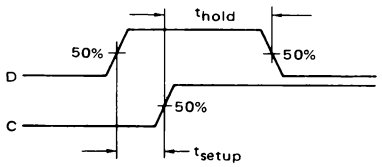


FIGURE 13l – TYPICAL RISE TIME (20% to 80%) versus
TEMPERATURE and SUPPLY VOLTAGE
(MECL 10,500)

SETUP AND HOLD TIMES

The t_{setup} and t_{hold} times are two ac specifications which can be confused unless clearly defined. For MECL devices, t_{setup} is defined as the time (50% – 50%) before a Clock transition that Data must be present for a bistable circuit to "recognize" the incoming Data.



The t_{hold} is similarly defined to be the time after the Clock transition that Data must remain to insure that bistable outputs retain their state.

In specifying devices, Motorola establishes and guarantees values for t_{setup} and t_{hold}. The limits for t_{setup} and t_{hold} insure proper logical function of bistable circuits, but do not guarantee that propagation delay or noise specifications will be met under all conditions when operating near the limits. For MECL bistable circuits, proper device operation usually occurs with Data present for somewhat less time than that specified for t_{setup} and t_{hold}.

POWER SUPPLY CONSIDERATIONS

MECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at -5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common-mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity.

Power supply regulation of 10% or better is recommended. The -5.2 V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect.

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 μF and a 100 pF capacitor at the power entrance to the board, and a 0.01 μF low-inductance capacitor between ground and the -5.2 V line every four to six packages, are recommended.

Most MECL 10,000 and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross-coupling between individual circuits within a package even when the outputs are driving heavy loads. Circuits with large drive capability, similar to the MC10110, have two V_{CC1} pins. The V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

All MECL II, MECL III, and MECL 10,000 devices have their own internal temperature and power-voltage-compensated bias voltage sources.

For further discussion of MECL power supply considerations to be made in system designing, see MECL System Design Handbook, Ch. 5.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The system designer can compute total package power for his particular termination technique by adding, I_E x 5.2 + Output Device Power. Some of the devices in the MECL I, II, and III Lines include on-chip output pulldown resistors, so that adding termination power has already been accomplished. None of the devices in the MECL 10,000 Series incorporate internal output pulldown resistors.

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to -2.0 Vdc	5.0	4.3
100 ohms to -2.0 Vdc	7.5	6.5
75 ohms to -2.0 Vdc	10	8.7
50 ohms to -2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohm to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

FIGURE 14 – TYPICAL POWER DISSIPATION IN OUTPUT CIRCUIT WITH EXTERNAL TERMINATING RESISTORS

The omission of these resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the specified power dissipation of those circuits without internal termination.

The table in Figure 14 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output-transistor power-dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

The power dissipation of MECL functional blocks varies with both temperature and V_{EE}. Typical variations are shown in Figure 15. The graph is normalized so that it applies to all MECL lines. The reference temperature is 25°C and the reference power is obtained by multiplying the typical I_E value (total power supply drain current specified on the

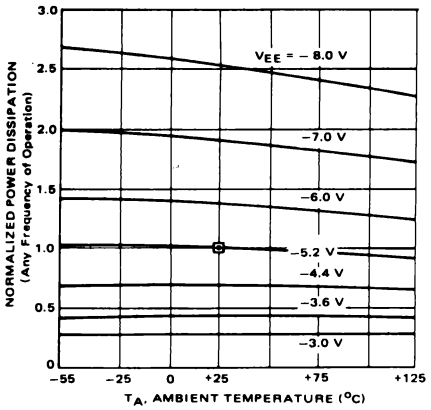


FIGURE 15 – NORMALIZED POWER DISSIPATION versus TEMPERATURE and SUPPLY VOLTAGE

data sheet) by V_{EE} (5.2 V). For those devices where only the maximum value of I_E is specified on the data sheet, nominal power dissipation is approximately 80% of that calculated with the I_E (max) specification.

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common-mode-rejection feature offers immunity against power-supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of gate inputs without deterioration of the guaranteed noise margin. Hence, dc fan-out with MECL circuits does not normally present a design problem.

The specified dc loading factors (the number of gate inputs of the same family that can be driven by a circuit output) for MECL I and MECL II families is 25. For MECL 10,000, it is 90; and for MECL III, it is 70 or 7, depending on the input impedance of the circuit (whether the system is implemented with high-impedance or low-impedance devices).

Graphs showing typical output voltage levels as a function of load current for MECL II, III, and 10,000 are shown in Figure 16. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit and, therefore, affects circuit speed. The effect of fan-out on MECL II speed is shown in the graphs of Figure 17.

For MECL 10,000 and MECL III, best performance at fan-outs greater than 10 and 6, respectively, will occur with the use of transmission lines.

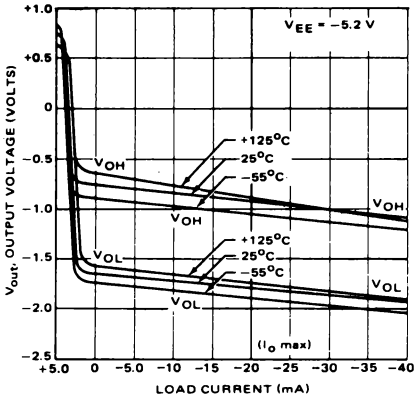


FIGURE 16a – MECL II TYPICAL OUTPUT VOLTAGES versus LOAD CURRENT and TEMPERATURE

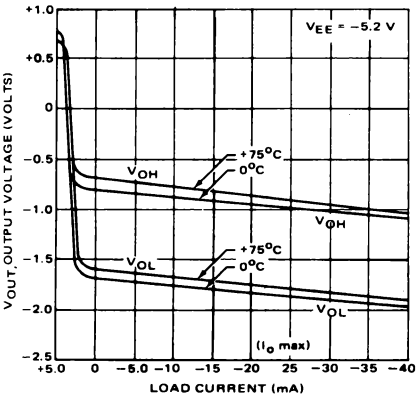


FIGURE 16b – MECL II TYPICAL OUTPUT VOLTAGES versus LOAD CURRENT and TEMPERATURE – 0°C & +75°C

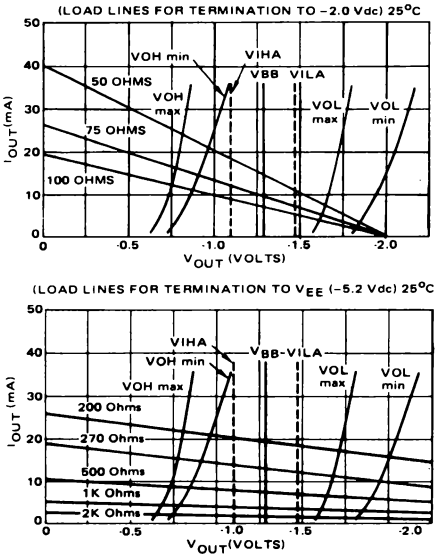


FIGURE 16c – OUTPUT VOLTAGE LEVELS versus DC LOADING, MECL III and MECL 10,000

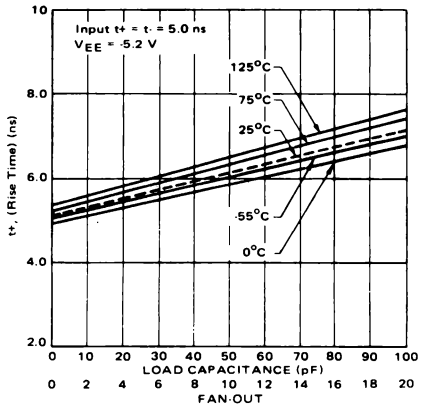


FIGURE 17a – MECL II RISE TIME versus LOADING and TEMPERATURE

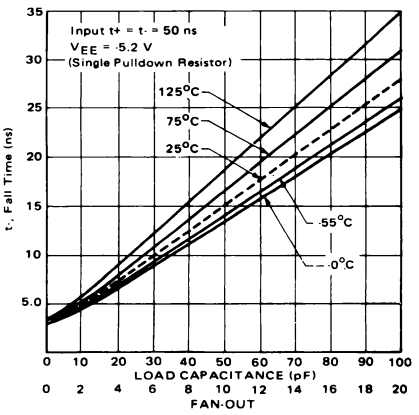


FIGURE 17b – MECL II FALL TIME versus LOADING and TEMPERATURE, (Single Pull-down Resistor)

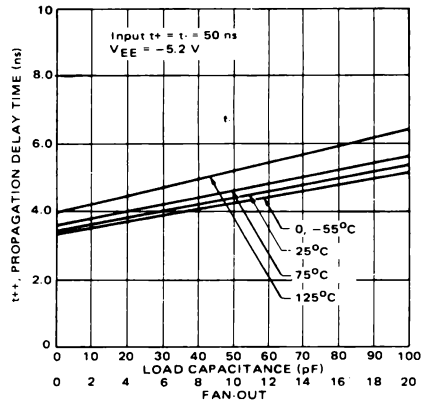


FIGURE 17c – MECL II PROPAGATION DELAY t++ versus LOADING and TEMPERATURE

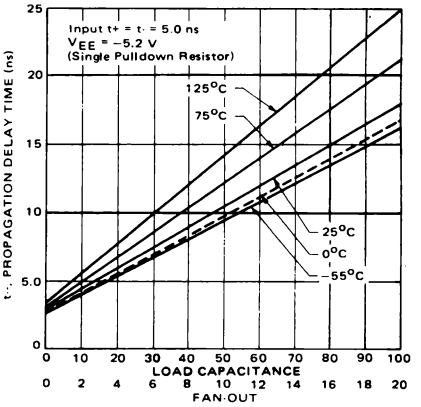


FIGURE 17d – MECL II PROPAGATION DELAY t-- versus LOADING and TEMPERATURE

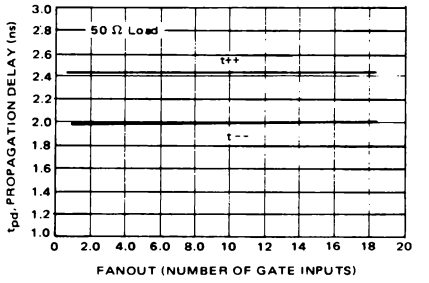


FIGURE 18a – MECL 10,000 GATE PROPAGATION DELAY TIME versus FANOUT (Fanout-at End of 14" 50 Ω Matched Transmission Line)

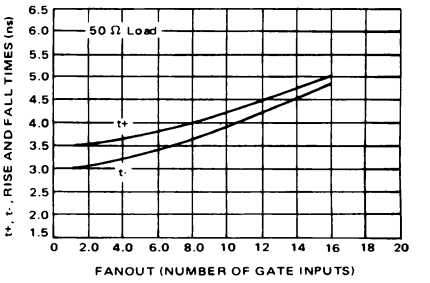


FIGURE 18b – MECL 10,000 RISE and FALL TIME (10% to 90%) versus FANOUT (Fanout at End of 14" 50 Ω Matched Transmission Line)

The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1 + C_d/C_o}$. Here C_o is the normal line capacitance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10,000 transmission line vary with line impedance. For example, with Z_o = 50 ohms, maximum stub length would be 4.5 inches (1.8 in. for

MECL III). But when Z_o = 100 ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10,000 device is 2.9 pF (e.g. MC10109). Therefore it is recommended that non-transmission-line environment fanout be limited to a maximum of 10 loads, due to line delay increases which limit system speed.

The input loading capacitance of a MECL III logic function is 3.3 pF. Therefore it is recommended that non-transmission-line environment fanout be limited to a maximum of 6 loads.

Shown in Figure 18 are the effects of fanout on MECL 10,000 time parameters.

UNUSED MECL INPUTS

The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low-signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual build-up of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

For MECL I and MECL II circuits, the gate inputs are essentially open. In use, therefore, any unused inputs should be tied to a negative potential for reliable system operation. Most devices can use V_{EE} as the input return, but control inputs of series reliable system operation. Most devices can use V_{EE} as the input return, but control inputs of series gated devices such as the MC1019, MC1021, MC1028, MC1035, MC1038, MC1045, and MC1066 should be returned to the V_{OL} level. This protects against voltage buildup on the unused inputs and assures that noise immunity depends only on those inputs actively used.

All single-ended input MECL 10,000 and MECL III circuits contain input pull-down resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected (the resistor provides a sink for I_{CBO} leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs).

Input pull-down resistor values for the MECL III high-impedance circuits and all MECL 10,000 devices are typically 50 kΩ and are not to be used as pull-down resistors for preceding open-emitter outputs.

Several MECL 10,000 devices don't contain input pull-downs. Examples are the differential line receivers, MC10115 and MC10116. If a single differential receiver of either device type is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE}.

SECTION IV — SYSTEM DESIGN CONSIDERATIONS

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The average temperature at the junction is a function of the system's ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D (\theta_{JA}) \quad (2)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = calculated power dissipation
θ_{JC} = thermal resistance, junction to case
θ_{CA} = thermal resistance, case to ambient
θ_{JA} = thermal resistance, junction to ambient

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case-to-ambient thermal resistance, θ_{CA}. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Hence, both system air flow and the MECL package mounting technique affect the thermal resistance term.

Package	θ_{JA} – °C/Watt (Still Air)		θ_{JC} – °C/Watt
	Worst Case	Typical	Worst Case
Ceramic Flat Pack (Cerflat) 1/4x1/4 (Gold Eutectic Die Bond)	210	166	60
Plastic Dual-In-Line, 14 lead or 16 lead (Gold Eutectic Die Bond)	150	100	70
Ceramic Dual-In-Line 14 or 16 lead (Gold Eutectic Die Bond)	150	100	50
Ceramic Dual-In-Line 24 Lead	–	45*	10*
Plastic Dual-In-Line 24 Lead	–	65**	–

*Data for 8200 sq. mil die size
**500 lfpm air flow

FIGURE 19 – WORST CASE AND TYPICAL THERMAL RESISTANCE RATINGS FOR SELECTED IC PACKAGES

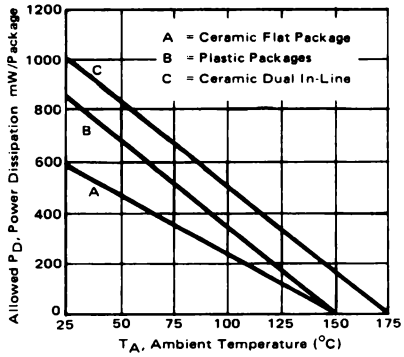
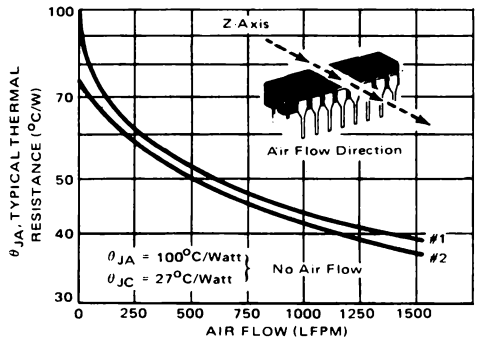


FIGURE 20 – AMBIENT TEMPERATURE DERATING CURVE



Package Type – 16-Lead Black Ceramic
Dissipation Level – 200 mW
Air Flow – Z-Axis 25°C*
Method – Calibrated Diode
Package Mounting #1 Barnes Socket
#2 Printed Circuit Board
4" x 6" x 0.062" – 2 oz. Cu.

*x-axis air flow lowers θ_{JA} by 5°C per watt.

FIGURE 21 – TYPICAL THERMAL RESISTANCES FOR 16-PIN BLACK CERAMIC DUAL IN-LINE PACKAGES

Package	Ambient Condition	θ_{JA}
Stud	Copper heat sink	37°C/W typ
Dual In-Line Low Power	⩾500 linear fpm blown air	50°C/W typ
Dual In-Line High Power (P_D > 500 mW)	Mounted in heat sink and 500 linear fpm blown air or Mounted in heat sink and on printed circuit ground plane using termal paste	35°C/W max

FIGURE 22 – THERMAL CONDITIONS FOR DC SPECIFICATIONS – MECL III

Internally, thermal resistance of an integrated circuit is a function of the package material and size, and of the method used in bonding the IC die to the package. For some standard IC packages, the worst-case and typical thermal resistance values are given in the table in Figure 19. In Figure 20, this basic data is converted into a graph showing the maximum power dissipation allowable at various ambient temperatures for circuits mounted in the various packages, taking into account the maximum permissible junction temperature for devices packaged in plastic or ceramic. These measurements are taken in still air.

The effect of air flow over the packages on θ_{JA} is illustrated in the graph of Figure 21 for two different mounting methods. This driven air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible junction temperature.

As an example of the use of the information above, the junction temperature for a quad MECL 10,000 gate loaded with four 50 ohm loads can be calculated. Typical total power dissipation (including a load) for this quad gate is 164 mW. Assume for this thermal study that air flow is 500 linear feet per minute and that the device is soldered into a printed circuit board. From Figure 21, curve #2, θ_{JA} is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following junction temperature results:

$$T_J = P_D \theta_{JA} + T_A$$
$$T_J = (0.164\ W)\ (50°C/W) + 25°C = 33.2\ °C$$

Under the above operating conditions the MECL 10,000 quad gate has its junction elevated above ambient temperature by only 8.2°C.

Even though devices on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperature as the air passes over the devices, or differences in ambient temperature between two devices.

MOUNTING and HEAT SINK SUGGESTIONS for MECL III

With large subnanosecond logic systems, the use of multilayer printed circuit boards is recommended. Such boards permit better ground planes and shorter interconnection runs than single-layer boards and also allow better use of stripline techniques.

MECL III circuits have an average power dissipation of approximately 60 mW per logic gate. Adequate cooling should be provided to insure that device junction temperatures do not exceed 110°C.

The dc data sheet specifications for MECL III are given for an operating temperature range from -30°C

to +85°C for the conditions described in the table of Figure 22.

The designer may want to use MECL III under conditions that vary from those given. The main restriction facing the designer is that a few high power dual in-line parts* dissipating typically 900 mW under load require heat sinking to assure a $\theta_{JA} \leq 35°C/W$ which will keep junction temperature below 110°C.

The low-power dual in-line parts may be used without air and with higher θ_{JA}. However, the designer must bear in mind that junction temperatures will be higher for higher θ_{JA}, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 450 mW device operated at θ_{JA} = 80°C/W shows a HIGH logic level shift of about 17.5 mV above the HIGH logic level when operated with a θ_{JA} = 50°C/W (level shift = $\Delta T_J \times 1.3$ mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and θ_{JA}), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and thermal characteristics are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL III system use.

Ceramic Dual In-Line Package, Case 620

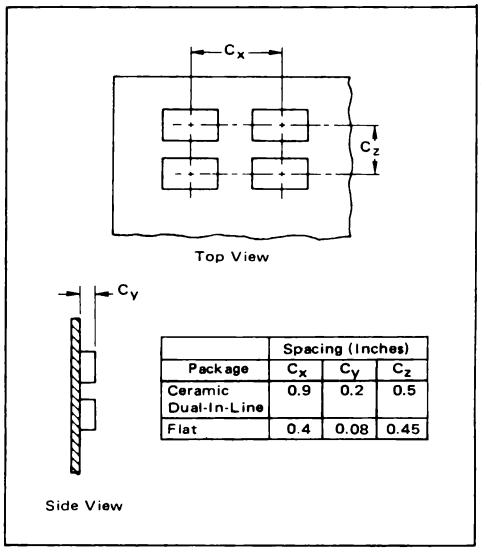
MECL III low-power devices are specified with θ_{JA} typically 50°C/W, and the high-power units (P_D > 500 mW) with θ_{JA} equal to 35°C/W maximum. To aid the designer in using the "L" (ceramic dual in-line) package, curves and data showing thermal characteristics of the package are provided in Figure 21.

The use of multi-layer printed circuit boards is recommended to provide both a ground plane and a good thermal path for heat dissipation. Also, a multi-layer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two-sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two-ounce copper board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be counter sunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

Printed channeling is a useful technique for conduction of heat away from the MECL dual in-line package when the device is soldered into a printed circuit board. As illustrated in Figure 23, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug-in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.



	Spacing (Inches)		
Package	C_x	C_y	C_z
Ceramic Dual-In-Line	0.9	0.2	0.5
Flat	0.4	0.08	0.45

FIGURE 23a – TYPICAL MECL III/MECL 10,000 CIRCUIT BOARD SPACING

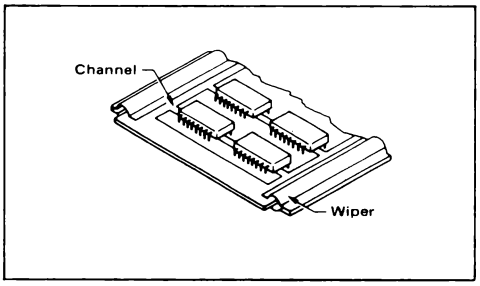


FIGURE 23b – CHANNEL/WIPER HEAT SINKING ON DOUBLE LAYER BOARD USED WITH MECL III

*i.e. MC1654, MC1678, MC1694, etc.

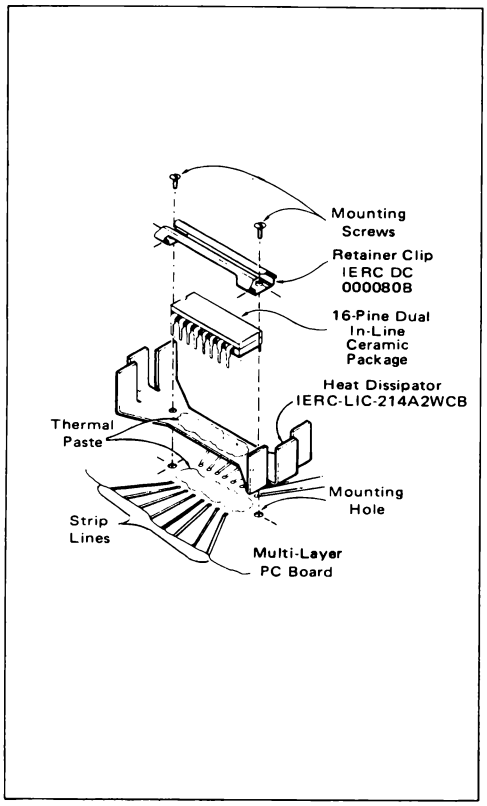


FIGURE 24 – MECL III HIGH-POWER DUAL IN-LINE PACKAGE MOUNTING (With Heat Sink, in 500 lfpm of Air)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5". Air flow is 500 lfpm along the Z axis.

FIGURE 25 – THERMAL GRADIENT OF JUNCTION TEMPERATURE (16-Pin MECL Dual In-Line Package)

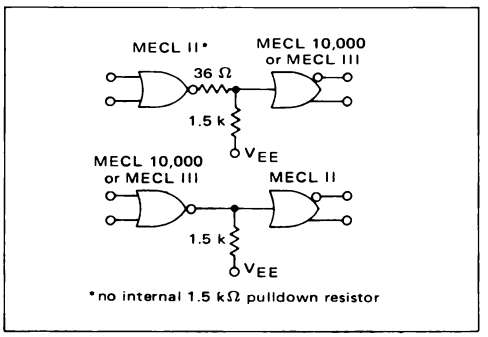


FIGURE 26 – INTERFACING MECL II TO MECL III OR MECL 10,000

For the high-power devices requiring θ_{JA} of less than 35°C/W, a suitable heat sink is the IERC-LIC-214A2WCB shown in Figure 24. The heat sink should have a minimum of 500 lfpm blown air or be mounted directly on the copper ground plane (using silicone paste) if used in still air, to meet the 35°C/W maximum rating. (See IERC Data Sheet for LIC-214A2WCB.) The heat sink shown allows easy access to the dual in-line IC pins for connection to Microstrip line.

Air Flow

The majority of MECL III users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Figure 25 provides gradient data at power levels of 200 mW. 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the air stream will be lower due to greater cooling.

(For further discussion of Thermal Management in MECL systems, see MECL System Design Handbook, Ch. 6.)

COMPATIBILITY AMONG MECL FAMILIES

MECL circuits are designed to interface with each other over a power supply voltage range of ±10% from the nominal -5.2 V without loss of noise margin (other than that due to reduced signal swing at low voltage). However, if two circuits are at different supply voltages or on the same power supply with a voltage offset between circuits, there will be a predictable loss of noise margin.

The MECL 10,000 logic family was designed to be directly level compatible with the MECL III logic family in dual in-line packages. The MECL II family has somewhat higher output levels but is compatible with the faster MECL 10,000 and MECL III inputs when MECL II is loaded with the resistor pair, shown in Figure 26. The resistor combination insures full noise margin in the logic LOW level. An alternate approach is to use a single 510 ohm resistor to V_{EE} on the MECL II output, but some loss of noise margin takes place. Conversely, lightly loading the MECL 10,000 or MECL III outputs with a 1.5 kΩ resistor raises the output logic levels to meet MECL II requirements. MECL II will operate directly with MECL 10,000 and MECL III, but there is a loss of noise margin (at the interface point only).

INTERFACING MECL to SLOWER LOGIC TYPES

MECL circuits are interfaceable with most other logic forms. For MECL/MTTL/MDTL interfaces, when MECL is operated at the recommended -5.2 volts and TTL/DTL at +5 V supply, currently available translator circuits, such as MC10124 and MC10125, may be used.

For systems where a dual supply (-5.2 V and + 5 V) is not practical, a discrete-component translator can be designed. For details, see MECL System Design Handbook, Ch. 8. Such circuits can easily be made fast enough for any available TTL.

MECL also interfaces readily with MOS. With CMOS operating at +5 V, any of the MECL to TTL translators works very well. On the other hand, CMOS will drive MECL directly when using a common -5.2 V supply. P-channel MOS, operating with a negative supply, requires simple translators to equalize the differing logic levels.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in Chapter 8 of the MECL System Design Handbook. Complex MECL 10,000 functions are presently available to interface MECL 10,000 with MOS logic, MOS memories, TTL tri-state circuits, and IBM bus logic levels.

CIRCUIT INTERCONNECTIONS

Though not necessarily essential, the use of multi-layer printed circuit boards offers a number of advantages in the development of high-speed logic cards. Not only do multi-layer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multi-layer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multi-layer boards are recommended for MECL III layouts and are justified when operating MECL 10,000 at top circuit speed, when high-density packaging is a requirement, or when transmission line interconnects are used.

Point-to-point back-plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL II speeds, this applies to line runs up to 12 inches, for MECL 10,000 up to 8 inches, and for MECL III up to 1 inch (maximum open wire lengths for less than 100 mV undershoot). But, because of the open-emitter outputs of MECL 10,000 and MECL III circuits, pull-down resistors are always required. Several ways of connecting such pull-down resistors are shown in Figure 27.

Resistor values for the connection in Figure 27(a) may range from 270 ohms to 2 kΩ depending on

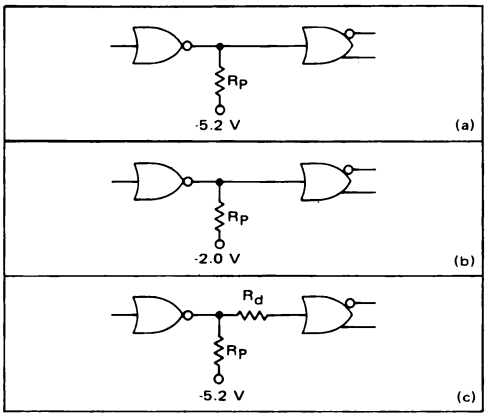


FIGURE 27 – PULL-DOWN RESISTOR TECHNIQUES

power and load requirements (see MECL System Design Handbook, Ch. 3). Power may be saved by connecting pull-down resistors in the range of 50 ohms (100 ohm minimum for MC10,500 and MC10,600 Series parts) to 150 ohms, to -2.0 Vdc, as shown in Figure 27(b). Use of a series damping resistor, Figure 27(c), will extend permissible lengths of unmatched-impedance interconnections, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length*, while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 150 ohms, depending on the line length, fanout, and impedance. The open emitter-follower outputs of MECL III and MECL 10,000 give the system designer all possible line driving options.

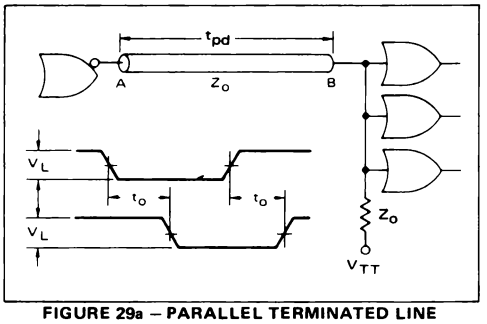


FIGURE 29a – PARALLEL TERMINATED LINE

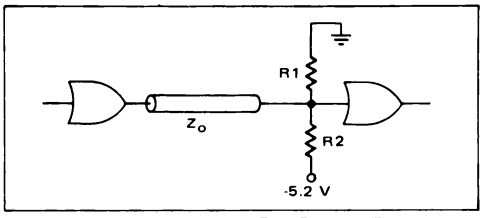


FIGURE 29b – PARALLEL TERMINATION – THEVENIN EQUIVALENT

*Limited only by line attenuation and bandwidth characteristics.

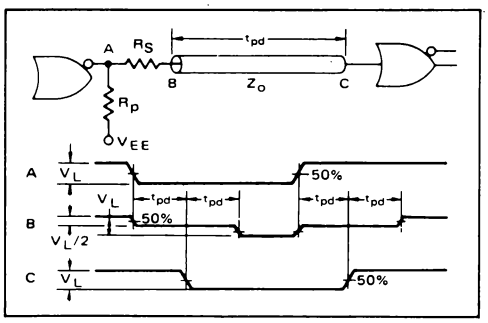


FIGURE 30 – SERIES TERMINATED LINE

One major advantage of MECL over saturated logic is its capability for driving matched-impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The MECL III and MECL 10,000 emitter-follower output transistors will drive a 50-ohm transmission line (100 ohms or greater for MECL 10,500 and MC10,600 Series) terminated to -2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6 mA in the LOW state.

Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 28(a), uses a single resistor whose value is equal to the impedance (Z_o) of the line. A terminating voltage (V_{TT}) of -2.0 Vdc must be supplied to the terminating resistor.

Another method of parallel termination uses a pair of resistors, R1 and R2. Figure 28(b) illustrates this method. The following two equations are used to calculate the values of R1 and R2:

$$R1 = 1.6\,Z_o$$

$$R2 = \frac{R1 \cdot Z_o}{R1 + Z_o}$$

Another popular approach is the series-terminated transmission line (see Figure 29). This differs from parallel termination in that only one-half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (R_S) at point A (Figure 29), the reflections in the transmission line will be terminated.

The advantages of series termination include ease of driving multiple series-terminated lines, low power consumption, and low cross-talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing present at intermediate points.

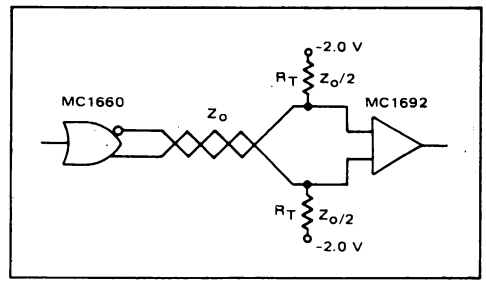


FIGURE 31 – TWISTED PAIR LINE DRIVER/RECEIVER

For board to board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies. No significant performance degradation occurs for lengths up to 20 feet for MECL III, and up to 50 feet for MECL 10,000.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. MECL complementary outputs are connected to one end of the twisted-pair line, and a differential line receiver to the other as shown in Figure 30. R_T is used to terminate the twisted pair line. The 1 to 1.5 V common-mode noise rejection of the line receiver ignores common-mode cross-talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

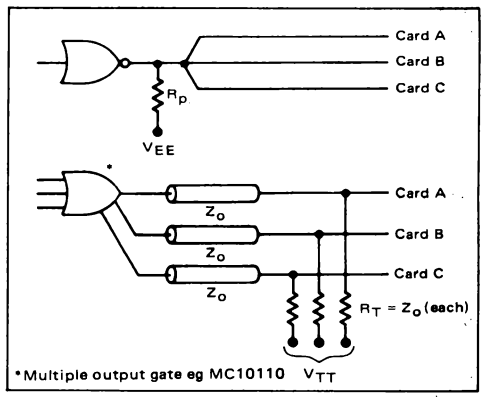


FIGURE 32 – PARALLEL FAN-OUT TECHNIQUES

If timing is critical, parallel signal paths (shown in Figure 31) should be used when fanout to several cards is required. This will eliminate distortion caused by long stub lengths off a signal path.

Wirewrapped connections can be used with both MECL II and MECL 10,000. For MECL III, the fast edge speeds (1 ns) create a mismatch at the wirewrap

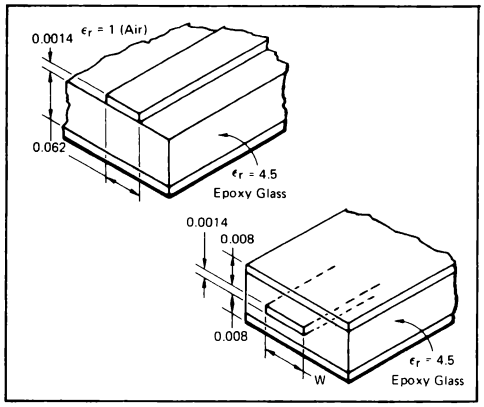


FIGURE 32 – PC INTERCONNECTION LINES FOR USE WITH MECL

connections which can cause reflections, thus reducing noise immunity. The mismatch occurs also with MECL II and MECL 10,000, but the distance between the wire-wrap connection and the end of the line is generally short enough so the reflections cause no problem.

Series damping resistors may be used with wire-wrapped lines for both MECL II and MECL 10,000 to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wirewrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single-ended, or differentially using a line receiver.

The recommended wirewrapped circuit cards have a ground plane on one side and a voltage plane on the other, to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wirewrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize crosstalk between parallel paths in the signal lines. Point-to-point wire routing is recommended because crosstalk will be minimized and line lengths will be shortest. Commercial wire-wrap boards designed for MECL 10,000 are available from Augat Inc.

Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant-width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 32.) The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

Stripline is used with multilayer circuit boards as shown in Figure 32. Stripline consists of a constant-width conductor between two ground planes.

Refer to MECL System Design Handbook, Ch. 3 for a full discussion of the properties and use of these lines.

CLOCK DISTRIBUTION

Clock distribution can be a system problem. Where large high-speed clock networks are required, a balanced twisted-pair line is recommended for clock distribution. A gate such as the MC1001/MC1201, together with the MC1020/MC1220 Quad Line Receiver make an excellent combination for distributing the clocking throughout a system. (See the MC1020/MC1220 data sheet for further detail.) This method allows control of clock skew time and offers 1.0 V, or better, noise immunity regardless of line length.

At MECL 10,000 speeds, either coaxial cable or twisted-pair line (using the MC10101 and MC10115) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large-fanouts at high frequency. An example of the application of this technique is shown in Figure 33.

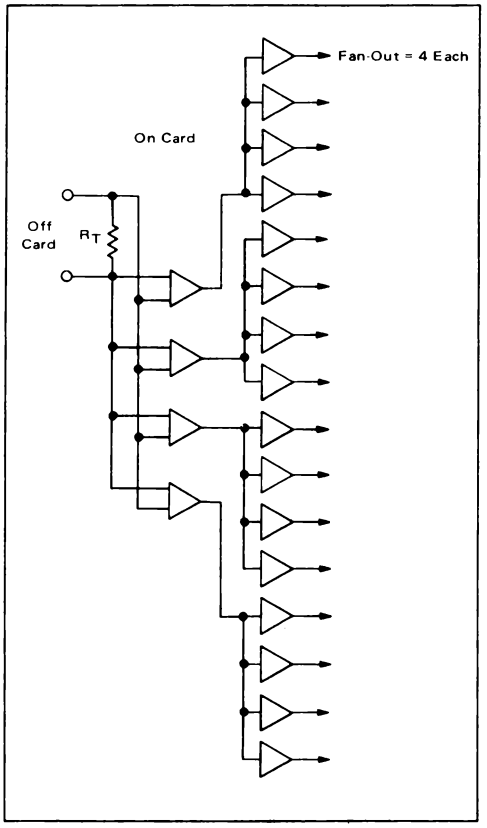


FIGURE 33 – 64 FANOUT CLOCK DISTRIBUTION

Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results:

A. On-card Synchronous Clock Distribution via Transmission Line
   1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
   2. Use balanced fanouts on the clock drivers.
   3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.
   4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.
   5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.
   6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.
   7. For Wire-OR (emitter dotting), two-way lines (a bus) are recommended. To produce such lines, both ends of a transmission line are terminated with 100-ohms impedance. This method should be used when Wire-OR connections exceed 1 inch apart on a drive line.

B. Off-Card Clock Distribution
   1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines or into flat, fixed-impedance ribbon cable. At the far end of the twisted pair an MC1692 differential line receiver is used. The line should be terminated with two $Z_O/2$ ohm resistors as shown in Figure 31. This method not only provides high speed, board-to-board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the V_{BB} reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.
   2. MECL III clock distribution to MECL II logic elements can be done one of two ways:
      a. Use the OR/NOR outputs or Q/$\overline{Q}$ outputs to drive the twisted pair as previously discussed. Receive differentially with the MECL II *line receivers (MC1020, MC1035,* or MC1066).
      b. Use any MECL III single-rail output to drive MECL II logic, but lightly load the MECL III element (1.5 kΩ to -5.2 volts) and maintain the interface lead length under 1 inch total (see Figure 26).

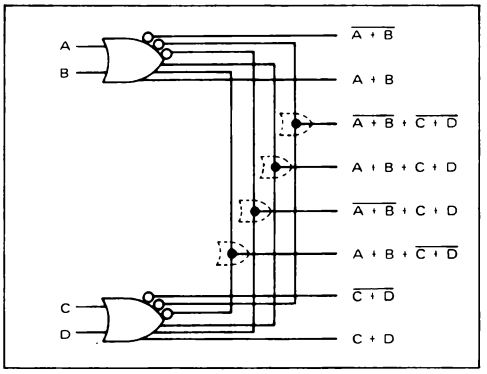


FIGURE 34a – USE OF WIRE-OR AND COMPLEMENTARY OUTPUTS

Family	Number **
MECL II*	15
MECL 10,000	10
MECL III	6

*Devices without internal pull-down resistors.
**DC limiting case; not AC recommended.

FIGURE 34b – RECOMMENDED MAXIMUM NUMBER OF GATES TO BE WIRE-ORed

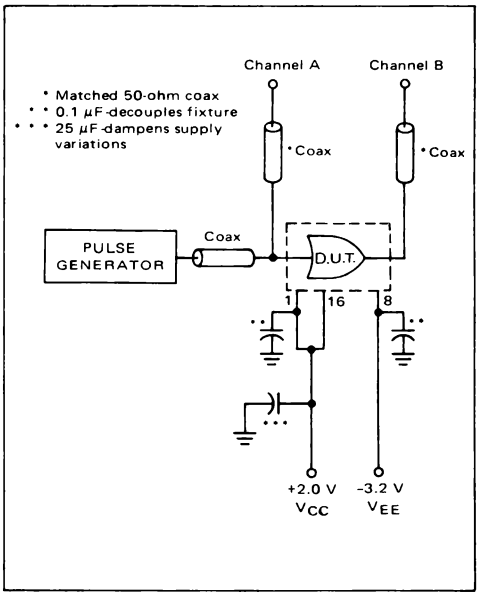


FIGURE 35 – MECL TEST SETUP

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. **Wire-OR** (can be produced by wiring MECL output emitters together outside packages).

2. **Complementary Logic Outputs** (both OR and NOR are brought out to package pins in most cases).

An example of the use of these two features to reduce gate and package count is shown in Figure 34a. The connection shown saves four 2-input gates and two inverters over non-ECL type logic designs. Wire-ORing also permits direct connection of MECL gates to busses (MECL System Design Handbook, Ch. 4).

Propagation delay is increased approximately 50 ps per wire-OR gate. The table in Figure 34b lists maximum numbers of gates possible for wire-OR without materially affecting system performance.

The use of a single output pulldown resistor is recommended per wired-OR, to economize on power dissipation. However, the use of two pulldown resistors per wired-OR can improve fall times and be used for double termination or busses.

Wire-OR should be done between gates on the same board, but the output of a wire-OR combination may go off board. Short on-card interconnects are recommended.

TESTING MECL 10,000 and MECL III

To obtain results correlating with Motorola circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 35.

A solid ground plane is used in the test set up, and capacitors bypass V_{CC1}, V_{CC2}, and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

The sampling 'scope interface runs directly to the 50-ohm inputs of Channel A and B via 50-ohm coaxial cable. Equal-length coaxial cables must be used between the test set and the A and B 'scope inputs. A 50-ohm coax cable such as RG58/U or RG188A/U, is recommended.

Interconnect fittings should be 50 ohm GR, BNC, Sealectro Conhex, or equivalent.

The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10,000 and 1.5 ns for MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of ±400 mV about a threshold of +0.7 V when V_{CC} = +2.0 V and V_{EE} = -3.2 V. (T_A = 25°C.)

The power supplies are shifted +2.0 V, so that the device under test has only one resistor value to load into — the precision 50-ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Motorola and customer testing. The positive supply (V_{CC}) should be decoupled from the test board by R.F. type 25 μF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1 μF, as is the V_{EE} pin.

SYSTEM CONSIDERATIONS, A SUMMARY OF RECOMMENDATIONS

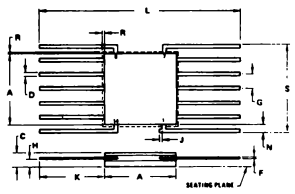
	MECL II	MECL 10,000	MECL III
Power Supply Regulation	10% or better	10% or better	10% or better
On-Card Temperature Gradient	Less Than 25°C	Less Than 25°C	Less Than 25°C
Maximum Non-Transmission Line Length (No Damping Resistor)	12"	8"	1"
Unused Inputs	Connect to V_{EE}*	Leave Open	Leave Open
PC Board	Standard 2-Sided or Multilayer	Standard 2-Sided or Multilayer	Multilayer
Special Cooling Requirements	No	No	No
Bus Connection Capability	Yes (Wire-OR)	Yes (Wire-OR)	Yes (Wire-OR)
MSI/LSI Parts	Yes	Yes	Yes (MSI)
Maximum Twisted Pair Length (Differential Drive)	Limited by Cable Response Only, Usually > 1000'	Limited by Cable Response Only, Usually > 1000'	Limited by Cable Response Only, Usually > 1000'
The Ground Plane to Occupy Percent Area of Card	> 25%	> 50%	> 75%
Wirewrap may be used	Yes	Yes	Not recommended
Compatible with MECL 10,000	With proper Interface	–	Yes

*Some devices may not be connected to V_{EE}; see specific data sheet information.

PACKAGE OUTLINE DIMENSIONS

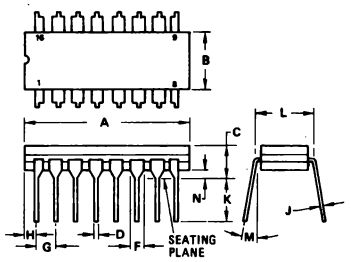
A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.

F SUFFIX
CERAMIC PACKAGE
CASE 607-04



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.10	6.99	0.240	0.275
C	0.76	2.03	0.030	0.080
D	0.25	0.48	0.010	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
J	–	0.38		0.015
K	6.35	–	0.250	–
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330

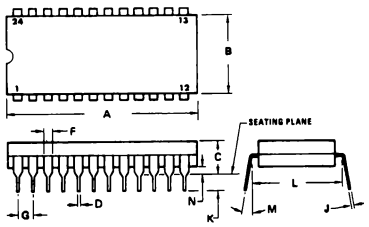
L SUFFIX
CERAMIC PACKAGE
CASE 620



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE
2 AT MAXIMUM MATERIAL CONDITION' PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT'
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL'

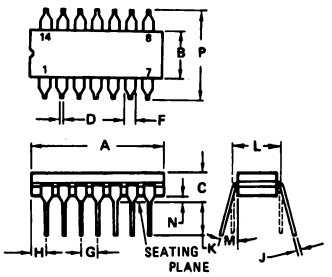
L SUFFIX
CERAMIC PACKAGE
CASE 623



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.08	0.160	0.200
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

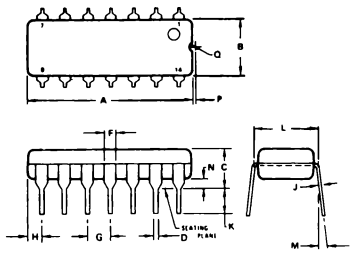
L SUFFIX
CERAMIC PACKAGE
CASE 632-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

NOTE: DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

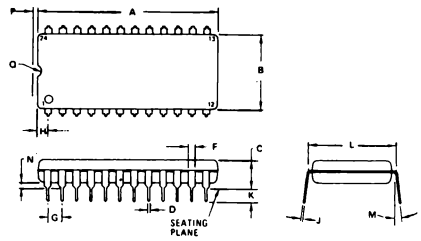
P SUFFIX
PLASTIC PACKAGE
CASE 646



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

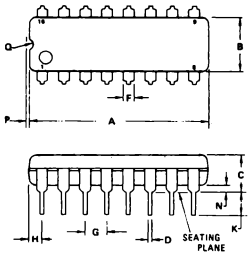
P SUFFIX
PLASTIC PACKAGE
CASE 649



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

Dimension "L" to lead centerline when formed parallel

P SUFFIX
PLASTIC PACKAGE
CASE 648

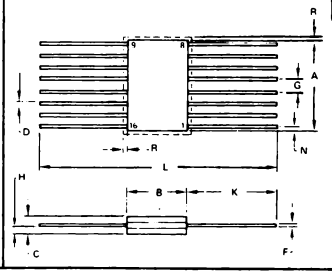


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

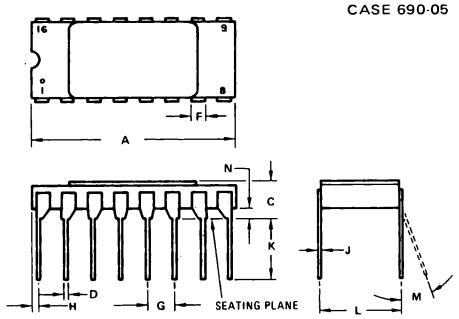
F SUFFIX
CERAMIC PACKAGE
CASE 650

NOTES
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER
2. LEADS WITHIN 0.13 mm (0.005") TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	6.60	0.245	0.260
C	1.52	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

L SUFFIX
CERAMIC PACKAGE
CASE 690-05



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.23	0.740	0.757
C	2.79	3.81	0.110	0.150
D	0.41	0.51	0.016	0.020
F	1.14	1.52	0.045	0.060
G	2.54 BSC		0.100 BSC	
H	0.33	0.89	0.013	0.035
J	0.20	0.30	0.008	0.012
K	3.56	4.06	0.140	0.160
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.76	1.14	0.030	0.045

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

Application Note Abstracts

(Application notes are available from Motorola Inc. at P.O. Box 20924, Phoenix, Arizona 85036)

AN-417A
"ICCrystal Controlled Oscillators"

Crystal controlled square wave oscillators can be used as clock drivers, harmonic sources for frequency markers, in frequency synthesizers, frequency comparators, etc. It is difficult to obtain high frequency square waves due to the long propagation delays of most integrated circuits. MECL 10,000 circuits with 2 ns propagation delays eliminate this problem. This note describes square wave oscillator circuits with crystal control that are capable of output frequencies, inverted and non-inverted, up to 200 MHz.

AN-418
"High Speed Monostable Multivibrators Design with MECL Integrated Circuits"

This note describes two configurations of monostable multivibrators using the MC1023 clock driver and a delay element. Operating frequencies in excess of 70 MHz and pulse widths of 4 nanoseconds are possible. Methods of obtaining the predetermined delay are also discussed.

AN-487
"A High-Speed Ripple-Through Arithmetic Processor"

A simple, systematic building block approach for designing a high-speed, ripple-through arithmetic processor is described. Using only gates and full adders, ultra-high speed multiplication, division, square root extraction, addition, and subtraction may be performed. Several variations of an arithmetic processor design are detailed and comparisons of speed and package count using the MECL and MDTL logic in 14-pin, 16-pin, 24-pin, 32-pin, and 64-pin packages are given.

AN-488
"High-Speed Addition Using Lookahead Carry Techniques"

The use of the lookahead carry principle to increase the operating speed of adder systems is described. Several adders of different sizes using variations of lookahead carry are developed and the logical implementation of these using the MTTL III and MECL II logic families is given.

AN-496-A
"Error Detection and Correction Using Exclusive-OR Gates and Parity Trees"

The availability of Exclusive-OR gates and parity trees allows digital system designers to use error detection and correction codes to improve their system reliability and maintainability without the major cost penalty that has existed in the past. Use of Exclusive-OR gates and parity trees available in the MRTL, MTTL, MDTL, and MECL families to design simple parity and single error Hamming parity detection and correction circuits is discussed.

AN-504
"The MC1600 Series MECL III Gates"

This application note explains the basic operation of the various gates available in the MECL III logic family. Typical operating characteristics are included as an aid to the designer of high-speed logic along with recommended layout, breadboarding, and testing procedures. This note will also provide the designer with some insight into the overall capabilities of this logic line as they apply to this application.

AN-532-A
"MTTL and MECL Avionics Digital Frequency Synthesizer"

This application note discusses several approaches that illustrate applications of complex digital integrated circuits directed toward avionics frequency synthesizers. The techniques presented point out the simplicity with which both MTTL and MECL digital integrated circuits can be used to produce frequency synthesis for avionic communications.

AN-534
"Commutating Filter Techniques"

This note describes the design and construction of commutating (digital) filters using Motorola MECL II, MTTL III and MC7400 digital integrated circuits. A short section on commuting filter theory is included along with examples of filters and their responses.

AN-536
"Micro-T Packaged Transistors for High Speed Logic Systems"

Integrated circuits have become the first thought of most designers faced with a digital problem. For specialized needs such as extremely high speed, high speed with minimum power dissipation, or unusual logic functions, however, discrete transistors in the ultra-small Micro-T package may prove advantageous.

AN-553
"A New Generation of Integrated Avionic Synthesizers"

The need to generate signals of a multitude of different frequencies for avionic systems has resulted in complex solutions in the past. With the introduction of certain standard product integrated circuits, frequency synthesis using digital phase locked loop techniques presents a more practical solution. Several different types of servo phase locked loop systems are

(Application notes are available from Motorola Inc. at P.O. Box 20924, Phoenix, Arizona 85036)

discussed and a practical design example is given. Results of design examples are presented along with possible applications.

AN-556
"Interconnection Techniques for Motorola's MECL 10,000 Series ECL"

This application note describes some of the characteristics of high speed digital signal lines and gives wiring rules for MECL 10,000 emitter coupled logic. The note includes discussions of printed circuit board interconnects, board-to-board interconnects, and wirewrapping techniques.

AN-565
"Using Shift Registers as Pulse Delay Networks"

This note discusses a high-speed clocked shift register using MECL 10,000 flip-flops and employed as a digitial incremental delay. The register may be clocked with a frequency division counter to accomplish delay with increments as small as 7.5 ns. The circuit, as developed, may be used for timing basic computer decisions or as an adjustable digital delay fine for pulses.

AN-566
"High Speed Binary Multiplication Using the MC10181"

With a MECL 4-bit arithmetic unit you can reduce both package count and interconnections in a ripple multiplier and achieve very fast multiply times.

AN-567
"MECL Positive and Negative Logic"

Either positive or negative logic assignments may prove convenient to the MECL system designer. This note describes the equivalences between the two approaches and providing guides for converting between them.

AN-579
"Testing MECL 10,000 Integrated Logic Circuits"

Circuit testing techniques become increasingly important as circuit speeds approach and exceed the 2 ns range. With MECL 10,000 and MECL III circuits it is possible to exploit their 50-ohm output drive capability to obtain highly accurate test data. This application note describes techniques for testing MECL 10,000 circuits for laboratory evaluation, and discusses key parameters which should be measured during incoming inspection rapid testing.

AN-581
"An MSI 500 MHz Frequency Counter Using MECL & MTTL"

The design of an MSI 8-digit LED readout 500 MHz counter using MECL III, MECL 10,000 and TTL is discussed. Described are two prescalers using MECL, along with the designs for two input amplifiers. A unique time-base controller is also shown for providing a multiphase clock to the counter.

AN-583
"A MECL 10,000 Main Frame Memory System Employing Dynamic MMOS RAMS"

This application note describes the construction of a dynamic MOS random access memory system that employs MECL 10,000 for the memory control logic. Considered in detail are the memory organization, layout rules, interfacing, and generation of the needed control signals.

AN-584
"Programmable Counters Using the MC10136 and MC10137 MECL 10,000 Universal Counters"

This application note describes operation of two MECL 10,000 Universal counters, and their use in high speed programmable counters. Circuit diagrams and waveform traces are included.

AN-592
"AC Noise Immunity of MECL 10,000 Integrated Circuits"

This application note discusses ac noise immunity as it relates to MECL systems. Test circuits for measuring ac noise immunity are shown, and results to be expected for typical MECL 10,000 circuits are presented.

AN-700
"Simulate MECL System Interconnections With A Computer Program

Circuit interconnections are an important part of system design when using high speed logic circuits. The design of interconnecting paths affects both system speed and system accuracy. This application note describes the use of a computer program to simulate interconnections for high speed digital systems.

AN-701
"Understanding MECL 10,000 DC and AC Data Sheet Specifications"

The dc and ac specifications for emitter-coupled logic are somewhat different than those for saturated logic. This application note describes the specifications found on a MECL 10,000 data sheet and provides information for understanding these specifications for persons unfamiliar with emitter-coupled logic.

(Application notes are available from Motorola at P.O. Box 20924, Phoenix, Arizona 85036)

AN-709
"MECL 10,000 Arithmetic Elements MC10179, MC10180, MC10181"

The MECL 10,000 arithmetic functions include a 4-bit arithmetic unit, a dual adder/subtractor, and a lookahead carry block. This application note describes the devices and shows their operation in large system configurations.

AN-720
"Interfacing With MECL 10,000"

This article describes some of the MECL circuits used to interface with signals not meeting MECL input or output requirements. The characteristics of these circuits such as; input impedance, output drive, gain, and bandwidth allow the system designer to use these parts to optimize his system. MECL interface circuits overcome a problem area of many system designs, which is the efficient coupling on non-compatible signals.

AN-726
"Bussing With MECL 10,000 Integrated Circuits"

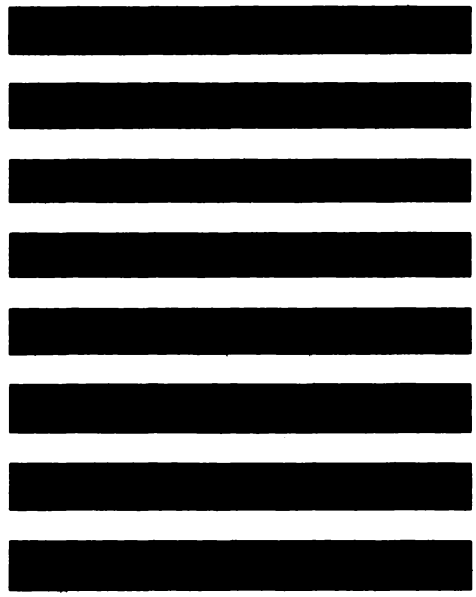
High speed data bus lines are an important part of modern computer systems. Features of the MECL 10,000 family allow construction of data busses in a transmission line environment. This application note describes some of the guidelines to consider when designing high speed bus lines and shows how the MC10123 can be used for maximum bus performance.

SUPPLEMENTARY LITERATURE

1. "The Case for Emitter-Coupled Logic," by Anthony A. Vacca, ELECTRONICS, April 26, 1971.
2. "Low Power ECL Bids for TTL Applications," by Ed Tynan, ELECTRONIC PRODUCTS, May 17, 1971.
3. "High-Speed Translators Simplify ECL/TTL Interface," by Bill Blood, COMPUTER HARDWARE, July 15, 1971.
4. "Speedup in ECL," by John Rhea, ELECTRONIC NEWS, September 13, 1971.
5. "Generate Stable High-Frequency Signals With Digital Mixers and Phase Locked Loops," by R. Treadway and L. J. Reed, ELECTRONIC DESIGN, January 6, 1972.
6. "ECL vs. Schottky," Special Report by John Rhea, ELECTRONIC NEWS, March 13, 1972.
7. "ECL Gates Stretch Oscillator Range," by W. Blood, ELECTRONICS, March 13, 1972.
8. "ECL – Who's Leading the Band?" by Sheldon Edelman, THE ELECTRONIC ENGINEER, April 1972.
9. "ECL Arithmetic Unit Performs High-Speed Binary Multiplication," by Tom Balph, EDN, May 1, 1972.
10. "Measure Frequency and Propagation Delay with High Speed ECL Circuits," by William R. Blood, Jr., EDN, July 1, 1972.
11. "Use ECL 10,000 Layout Rules to Help Solve PC Board Interconnections, Part I," by Tom Balph, ELECTRONIC DESIGN, August 17, 1972.
12. ibid, Part II, ELECTRONIC DESIGN, September 2, 1972.
13. "ECL/MOS for Optimum Minicomputer Systems," by P. Breedlove, COMPUTER DESIGN, August 1972.
14. "Testing MECL 10,000 – What it Takes to Get High on Speed", by Bill Blood, ELECTRONIC PRODUCTS, November 20, 1972.
15. "Boost Counting Speed to 110 MHz with ECL Universal Counters", by Tom Balph and Howard Gnauden, ELECTRONIC DESIGN, April 1, 1973.
16. "Digital Alphabet Spells Change in IC Usage" by Ed Tynan, ELECTRONIC BUYERS NEWS, October 2, 1972.
17. "ECL Shift Registers make Versatile Pulse Delay Networks", by Jon DeLaune, EDN, October15, 1972.
18. "Testing MECL 10,000 – What it Takes to Get High on Speed," by Bill Blood, ELECTRONIC PRODUCTS, November 20, 1972. (AN-579)
19. "Blend ECL and TTL ICs to Obtain High Frequency Counter Circuits," by Jon DeLaune, ELECTRONIC DESIGN, March 15, 1973, page 112.
20. "Leapfrog Ahead with Standard Family MSI/LSI," by Bob Cushman, Special Features Editor, EDN, April 5, 1972, page 30.
21. "Positive versus Negative Logic," by Tom Balph, Electronic Products Magazine, August 21, 1972.
22. "Improve Fast-Logic Designs," by Bill Blood, Electronic Design, May 10, 1973.
23. "Use ECL for Your High-Speed Design – Part I," by Lloyd Maul, EDN, July 20, 1973.
24. "ECL 10,000 Layout and Loading Rules – Part II," by Lloyd Maul, EDN, August 5, 1973.
25. "Interface TTL Systems With ECL Circuits," by George Adams, EDN, September 5, 1973.
26. "MECL 10 K Reliability Evaluation," by Paul Greer, Electronic Buyers' News, November 26, 1973.
27. "Make Sure Your Logic Keeps Pace With Memory Cycle Times" by Dick Brunner, EDN, January 20, 1973.
28. "Increasing Minicomputer Speed With Emitter-Coupled Logic" by Jon DeLaune, COMPUTER DESIGN, February 1974.

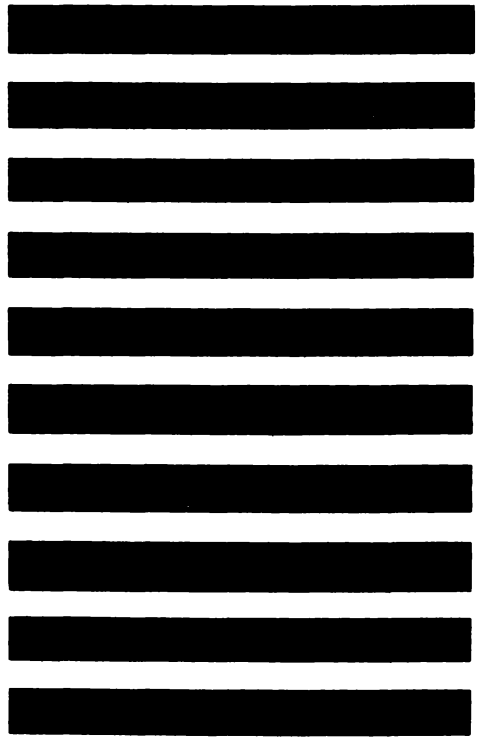
Contents of the MECL SYSTEM DESIGN HANDBOOK (206 pages):

Motorola's MECL System Design Handbook may be purchased for $2.50 per copy. Copies may be obtained by sending check or money order payable to Motorola Inc., at P. O. Box 20924, Phoenix, Arizona 85036.



MECL

INTEGRATED CIRCUITS
SELECTOR GUIDES



MC1000 Series (0 to +75°C)
MC1200 Series (−55 to +125°C)

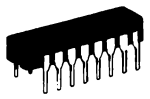
The MECL II series of monolithic integrated logic circuits presents the system design engineer with an integrated circuit family designed to permit system implementation with the fewest possible number of individual units. This approach offers cost savings, reduced power supply requirements, smaller physical size and high reliability.

MECL II circuits feature the fastest propagation delay times with commensurate rise and fall times of any family of integrated circuits. This feature plus the constant current feature of MECL imposes fewer restrictions on design, layout and system fabrication than any other high-speed family.

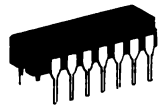
FEATURES

- Propagation typically 4 ns per logic decision
- Excellent noise immunity characteristics
- Simultaneous OR/NOR outputs
- High fan-in and fan-out capabilities
- Internally temperature compensated

F SUFFIX
CERAMIC PACKAGE
CASE 607



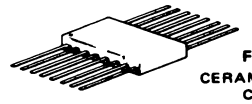
L SUFFIX
CERAMIC PACKAGE
CASE 620



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646

P SUFFIX
PLASTIC PACKAGE
CASE 648



F SUFFIX
CERAMIC PACKAGE
CASE 650

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C)

Function	Type ①		Loading Factor Each Output	Propagation Delay ns typ	Power Dissipation mW typ/pkg	Case
	-55 to +125°C	0 to +75°C				
Single 6-Input Gate, 3 OR Outputs w/Pulldowns 3 NOR Outputs w/Pulldowns	MC1201F,L	MC1001P	25	4.0	115	607,632,646
Dual 4-Input Gate, 2 OR Outputs w/Pulldowns 2 NOR Outputs w/Pulldowns	MC1204F,L	MC1004P	25	4.0	95	607,632,646
Dual 4-Input Gate, 2 OR Outputs w/o Pulldowns 2 NOR Outputs w/o Pulldowns	MC1206F,L	MC1006P	25	4.0	45	607,632,646
Triple 3-Input Gate, 3 NOR Outputs w/Pulldowns	MC1207F,L	MC1007P	25	4.0	110	607,632,646
Quad 2-Input Gate, 4 NOR Outputs w/Pulldowns	MC1210F,L	MC1010P	25	4.5	115	607,632,646
Quad 2-Input Gate, 2 NOR Outputs w/Pulldowns 2 NOR Outputs w/o Pulldowns	MC1211F,L	MC1011P	25	4.5	95	607,632,646

① Type numbers with F suffix use Case 607 or 650, Type numbers with L suffix use Case 632 or 620 as indicated.
Type numbers with P suffix use Case 646 or 648 as indicated.

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C)

Function	Type ①		Loading Factor Each Output	Propagation Delay ns typ	Power Dissipation mW typ/pkg	Case
	-55 to + 125°C	0 to + 75°C				
Quad 2-Input Gate, 4 NOR Outputs w/o Pulldowns	MC1212F,L	MC1012P	25	4.5	65	607, 632, 646
AC Coupled J-K Flip-Flop (85 MHz typ)	MC1213F,L	MC1013P	25	6.0	125	607, 632, 646
Dual R-S Flip-Flop (Positive Clock)	MC1214F,L	MC1014P	25	6.0	140	607, 632, 646
Dual R-S Flip-Flop (Negative Clock)	MC1215F,L	MC1015P	25	6.0	140	607, 632, 646
Dual R-S Flip-Flop (Single Rail)	MC1216F,L	MC1016P	25	6.0	140	607, 632, 646
Level Translator (Saturated Logic to MECL)	MC1217F,L	MC1017P	25 (MECL)	15	105	607, 632, 646
Level Translator (MECL to Saturated Logic)	MC1218F,L	MC1018P	7 (DTL)	19	55	607, 632, 646
Full Adder	MC1219F,L	MC1019P	25	3.0 to 8.0**	145	607, 632, 646
Quad Line Receiver	MC1220F,L	MC1020P	25	4.0	115	607, 632, 646
Full Subtractor	MC1221F,L	MC1021P	25	4.0 to 11**	145	607, 632, 646
Type D Flip-Flop	MC1222F,L	MC1022P	25	8.0	110	607, 632, 646
Dual 4-Input OR/NOR Clock Driver •	MC1223F,L	MC1023P	25	2.0	250	607, 632, 646
Dual 2-Input Expandable Gate	MC1224L	MC1024P	25	4.0	95	632, 646
Dual 4 and 5-Input Expander	MC1225F,L	MC1025P	–	–	–	607, 632, 646
Dual 3-4-Input Transmission Line and Clock Driver •	MC1226F,L	MC1026P	25	2.0	140	607, 632, 646
AC Coupled J-K Flip-Flop (120 MHz typ)	MC1227F,L	MC1027P	25	4.0	250	607, 632, 646
Dual 4-Channel Data Selector •	MC1228F,L	MC1028P	25	5.0	170	620, 648, 650
Quad Exclusive OR Gate	MC1230F,L	MC1030P	25	5.0	130	607, 632, 646
Quad Exclusive NOR Gate	MC1231F,L	MC1031P	25	5.0	130	607, 632, 646
100-MHz AC Coupled Dual J-K Flip-Flop •	MC1232F,L	MC1032P	25	4.5	180	620, 648, 650
Dual R-S Flip-Flop (Single Rail, Negative Clock)	MC1233F,L	MC1033P	25	6.0	140	607, 632, 646
Type D Flip-Flop •	MC1234F,L	MC1034P	25	4.0	185	607, 632, 646
Triple Line Receiver	MC1235F,L	MC1035P	25	5.0	140	607, 632, 646
16-Bit Coincident Memory •	MC1236F,L	MC1036P	5	17	250	607, 632, 646
16-Bit Coincident Memory w/o Pulldowns •	MC1237F,L	MC1037P	5	17	250	607, 632, 646
Quad Level Translator (MECL to Saturated Logic)	MC1239F,L	MC1039P	7 (DTL)	12	200	620, 648, 650
Quad Latch	MC1240F,L	MC1040P	25	8.0	250	607, 632, 646
Decoder - Display Driver •	MC1245F,L	MC1045P	–	–	178	620, 648, 650
Quad 2-Input AND Gates	MC1247F,L	MC1047P	25	5.0	130	607, 632, 646
Quad 2-Input NAND Gates	MC1248F,L	MC1048P	25	5.0	130	607, 632, 646
Dual Full Adder •	MC1259F,L	MC1059P	25	9.0	375	620, 648, 650
Quad 2-Input NOR Gate •	MC1262F,L	MC1062P	25	2.0	320	620, 648, 650
Quad 2-Input NOR Gate •	MC1263L	MC1063P	25	2.0	320	632, 646
Triple Line Receiver •	MC1266F,L	MC1066P	25	2.0	350	607, 632, 646
Quad MTTL to MECL Translator With Strobe	MC1267F,L	MC1067P	1	5.0	300	620, 648, 650
Quad MECL to MTTL Translator With Totem-Pole Outputs •	MC1268F,L	MC1068P	10 (MTTL)	5.0	340	620, 648, 650
Quad Latch	MC1270F,L	MC1070P	25	8.0	200	607, 632, 646

① Type numbers with F suffix use Case 607 or 650, Type numbers with L suffix use Case 632 or 620 as indicated.
Type numbers with P suffix use Case 646 or 648 as indicated.

†Not recommended for new designs

•Noise Margin = 150 mV

••Propagation delay time is dependent on data path, see data sheet for details.

MC1600 Series (-30°C to +85°C)

The requirement for digital systems with ever higher performance has increased the need for high-speed integrated circuits. The industry has recognized that the only economical way to obtain high operating system speed is through the use of emitter-coupled logic. Motorola offers a state-of-the-art, emitter-coupled logic family with sub-nanosecond propagation delays – MECL III.

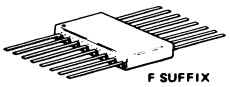
MECL III circuit design is similar to that used in the popular MECL 10,000 family. In the MECL III line, as well as MECL 10,000, advanced processing techniques are employed and the capability for driving low-impedance terminated lines is provided. MECL III is recommended for new designs.

GENERAL FEATURES

- Gate Switching Speeds of 1.0 ns typical
- Capability of Driving Terminated Lines with Impedance as Low as 50 Ohms
- Flip-Flop Toggle Rate Greater Than 500 MHz
- Operation with Unused Inputs Left Open
- Multilayer Metalization for economy
- New Packages with Improved Electrical and Thermal Characteristics
- Compatibility with MECL 10,000 Series
- Counting Speeds to above 1 GHz

P SUFFIX
PLASTIC PACKAGE
CASE 646

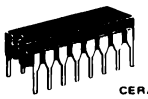
L SUFFIX
CERAMIC PACKAGE
CASE 632



F SUFFIX
CERAMIC PACKAGE
CASE 650

P SUFFIX
PLASTIC PACKAGE
CASE 648

F SUFFIX
CERAMIC PACKAGE
CASE 607



L SUFFIX
CERAMIC PACKAGE
CASE 620

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C unless otherwise noted.)

Function	Type ① -30° to +85°C	Loading Factor # Each Output	Propagation Delay 50-ohm Load ns typ	Power Dissipation (No Load) mW typ/pkg	Case
Voltage Controlled Oscillator	MC1648	–	*225 MHz typ	150	607,632,646
Dual A/D Comparator	MC1650	70	3.5	275	620,650
Dual A/D Comparator	MC1651	70	3.0	275	620,650
Binary Counter	MC1654	70	*325 MHz typ	750 ⌇⌇	620
Voltage-Controlled Multivibrator	MC1658	70	*150 MHz typ	125	620,648,650
Dual 4-Input OR/NOR Gate	MC1660	70	1.1	120	620,650
Quad 2-Input NOR Gate	MC1662	70	1.1	240	620,650
Quad 2-Input OR Gate	MC1664	70	1.1	240	620,650
Dual Clocked R-S Flip-Flop	MC1666	70	1.8	220	620,650
Dual Clocked Latch	MC1668	70	1.8	220	620,650
Master-Slave Type D Flip-Flop	MC1670	70	*350 MHz typ	220	620,650
Triple 2-Input Exclusive OR Gate	MC1672	70	1.3	220	620,650
Triple 2-Input Exclusive NOR Gate	MC1674	70	1.3	220	620,650
Bi-Quinary Counter	MC1678	70	*350 MHz typ	750 ⌇⌇	620
Dual 4-5-Input OR/NOR Gate	MC1688	70	0.8	125	650
UHF Prescaler Type D Flip-Flop	MC1690	70	*500 MHz min	200	620,650
Quad Line Receiver	MC1692	70	1.1	220	620,650
4-Bit Shift Register	MC1694	70	*325 MHz typ	750 ⌇⌇	620
1 GHz Divide-By-Ten Counter	MC1696	–	*1 GHz min	650	650

① L suffix denotes Dual In-Line Ceramic Package, F suffix denotes Ceramic Flat Package, P suffix denotes Dual In-Line Plastic Package. (i.e., MC1600L = Ceramic Dual In-Line Package, MC1600F = Ceramic Flat Package, MC1600P = Plastic Dual In-Line Package).

⌇⌇ Requires Heat Sink – IERC-LIC-214A2WCB or equivalent.

*Toggle Frequency

#DC Loading Factors are based on:

1. Full load output current, I_L = -25 mAdc max
2. Maximum input current, I_{in} = 350 μAdc

MECL III LOGIC DIAGRAMS

Numbers at ends of terminals denote pin numbers for L package (Case 620 unless noted as Case 632) and P package (Case 646 unless noted as Case 648).

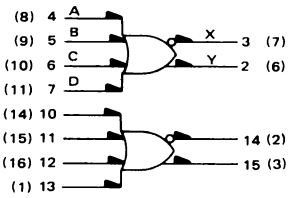
Numbers in parenthesis denote pin numbers for F package (Case 650 unless noted as Case 607).

CASE	V_{CC}	V_{EE}
	Pin No.	Pin No.
650	4,5	12
620	1, 16	8

See individual drawing for devices with other Cases.

GATES

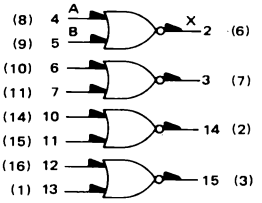
MC1660
Dual 4-Input OR/NOR Gate



$X = \overline{A+B+C+D}$
$Y = A+B+C+D$

t_{pd} = 0.9 ns typ (510-ohm load)
1.1 ns typ (50-ohm load)
P_D = 120 mW typ/pkg (no load)

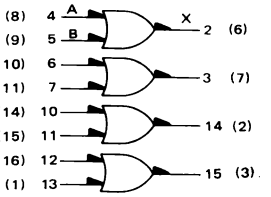
MC1662
Quad 2-Input NOR Gate



$X = \overline{A+B}$

t_{pd} = 0.9 ns typ (510-ohm load)
1.1 ns typ (50-ohm load)
P_D = 240 mW typ/pkg (no load)

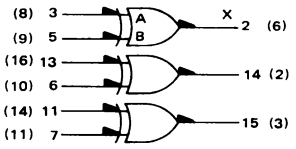
MC1664
Quad 2-Input OR Gate



X = A+B

t_{pd} = 0.9 ns typ (510-ohm load)
1.1 ns typ (50-ohm load)
P_D = 240 mW typ/pkg (no load)

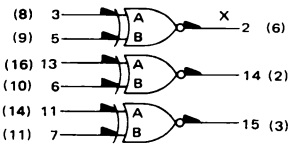
MC1672
Triple 2-Input Exclusive OR Gate



$X = A \bullet \overline{B} + \overline{A} \bullet B$

t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg

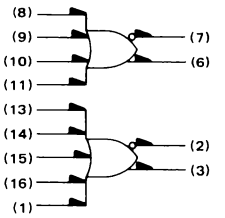
MC1674
Triple 2-Input Exclusive NOR Gate



$X = A \bullet B + \overline{A} \bullet \overline{B}$

t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns type (50-ohm load)
P_D = 220 mW typ/pkg

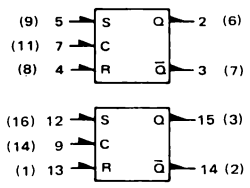
MC1688
Dual 4-5-Input OR/NOR Gate



t_{pd} = 0.8 ns typ
P_D = 125 mW typ/pkg (No Load)

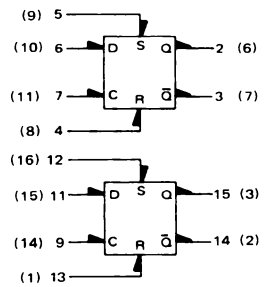
FLIP-FLOPS

MC1666
Dual Clocked R-S Flip-Flop



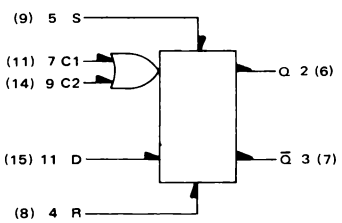
t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (no-load)

MC1668
Dual Clocked Latch



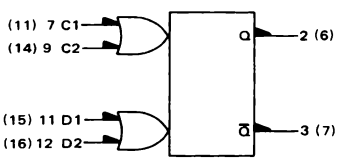
t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (no-load)

MC1670
Master-Slave Type D Flip-Flop



f_{Tog} = 350 MHz typ
P_D = 220 mW typ/pkg (no load)

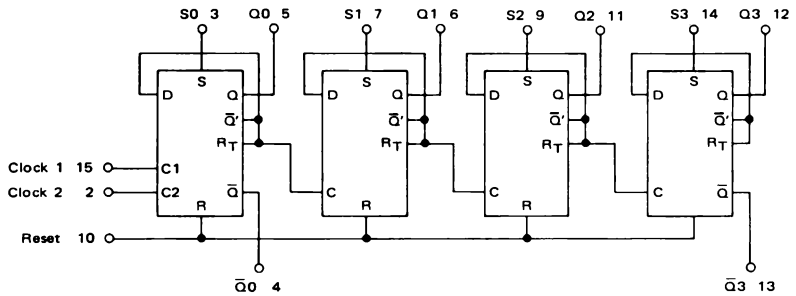
MC1690
UHF Prescaler Type D Flip-Flop



f_{Tog} = 500 MHz min
P_D = 200 mW typ/pkg (No Load)

COUNTERS

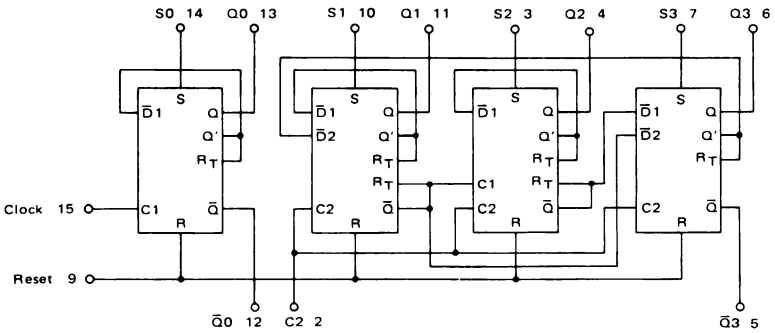
MC1654
Binary Counter



*P_D = 750 mW typ/pkg
Operating Frequency = 325 MHz typ

*Requires special heat sink IERC LIC 214A2WCB or equivalent.

MC1678
Bi-Quinary Counter

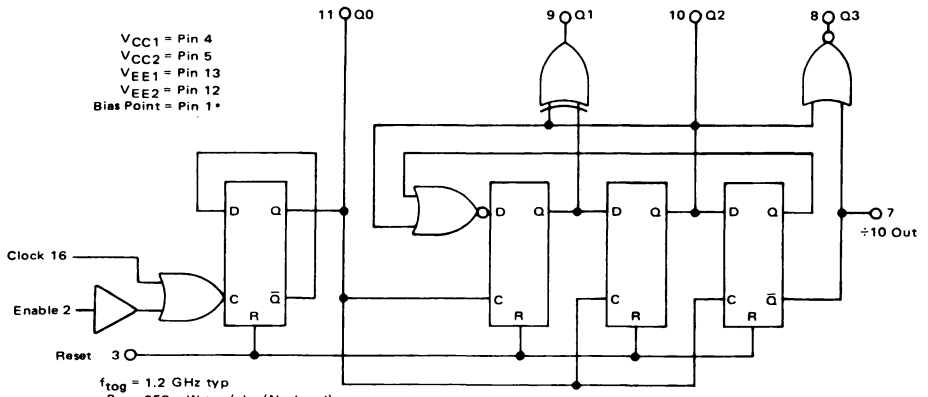


*P_D = 750 mW typ
Toggle Frequency = 350 MHz typ

*Requires special heat sink IERC LIC 214A2WCB or equivalent.

COUNTERS *(cont.)*

MC1696
1-GHz Divide-By-Ten
Counter



f_{tog} = 1.2 GHz typ
P_D = 650 mW typ/pkg (No Load)
Output Rise and Fall Times = 1.0 ns (20% to 80%)

*This bias point permits capacitive decoupling for a c performance enhancement.

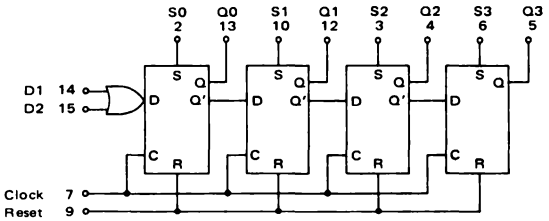
SHIFT REGISTER

MC1694
4-Bit Shift Register

FLIP-FLOP TRUTH TABLE

INPUTS				OUTPUT
D	C	R	S	Q_n
0	0	0	0	Q_{n-1}
0	0	0	0	1
0	0	1	0	0
0	0	1	1	*
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	*
1	0	0	0	Q_{n-1}
1	0	0	1	1
1	0	1	0	0
1	0	1	1	*
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	*

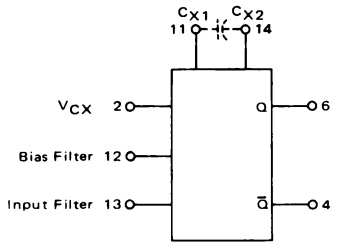
*Output State Undefined



Total Power Dissipation = 750 mW typ/pkg
Shift Frequency = 325 MHz typ

MULTIVIBRATOR

MC1658
Voltage-Controlled Multivibrator

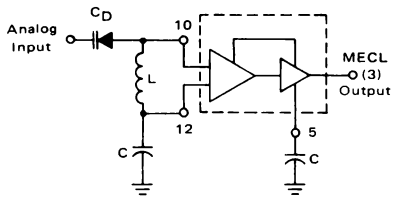


V_{CC1} = Pin 1
V_{CC2} = Pin 5
V_{EE} = Pin 6

Operating Frequency = 150 MHz typ
P_D = 125 mW typ/pkg

OSCILLATOR

MC1648
Emitter Coupled Oscillator

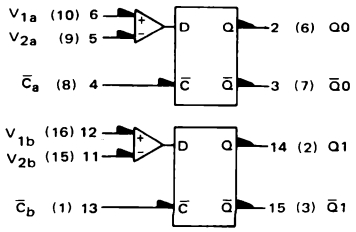


V_{CC} = Pins 1, 14
V_{EE} = Pins 7, 8

Operating Frequency = 225 MHz typ
P_D = 150 mW typ/pkg
(+5.0 Vdc Supply)
L, C, C_D are external components.
C_D is a varactor diode.

COMPARATOR

MC1650
MC1651
Dual A/D Comparator

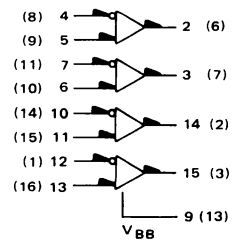


t_{pd} = 3.5 ns typ (MC1650)
3.0 ns typ (MC1651)
P_D = 330 mW typ/pkg (No load)

V_{CC} = +5.0 V = Pin 7,10 · (11), (14)
V_{EE} = -5.2 V = Pin 8 (12)
Gnd = Pin 1, 16 (4) (5)

RECEIVER

MC1692
Quad Line Receiver

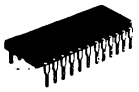


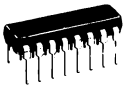
t_{pd} = 0.9 ns typ (510-ohm load)
1.1 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No load)

MC10,100/10,200 Series (-30 to +85°C)
MC10,500/10,600 Series (-55 to +125°C)

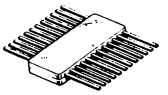
MECL 10,000 has an excellent speed-power product, has relatively slow rise and fall times, and transmission-line drive capability. The combination of versatile logic functions and the 2.0 ns propagation delay make MECL 10,000 a versatile family for data handling and processing systems.

Circuit design with MECL 10,000 is unusually convenient. The differential amplifier input and emitter-follower output permit high fanout, the wired-OR option, and complementary outputs. MECL III is directly compatible with MECL 10,000, and can be used to extend the speed capability of the MECL 10,000 series.

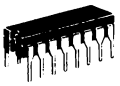

L SUFFIX
CERAMIC PACKAGE
CASE 623

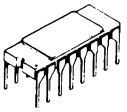

P SUFFIX
PLASTIC PACKAGE
CASE 648


F SUFFIX
CERAMIC PACKAGE
CASE 650


F SUFFIX
CERAMIC PACKAGE
CASE 652


P SUFFIX
PLASTIC PACKAGE
CASE 649


L SUFFIX
CERAMIC PACKAGE
CASE 620


AL SUFFIX
CERAMIC PACKAGE
CASE 690

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C)

Function	Type① -30 to +85°C	Type① -55 to +125°C	Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
Quad 2-Input NOR Gate With Strobe	MC10100	–	2.0	100	620
Quad OR/NOR Gate	MC10101	MC10501	2.0	100	620,648,650
Quad 2-Input NOR Gate	MC10102	MC10502	2.0	100	620,648,650
Quad 2-Input OR Gate	MC10103	–	2.0	100	620
Quad 2-Input AND Gate	MC10104	MC10504	2.7	140	620,648,650
Triple 2-3-2-Input OR/NOR Gate	MC10105	MC10505	2.0	90	620,648,650
Triple 4-3-3-Input NOR Gate	MC10106	MC10506	2.0	90	620,648,650
Triple 2-Input Exclusive OR/Exclusive NOR	MC10107	MC10507	2.5	110	620,648,650
Dual 4-5-Input OR/NOR Gate	MC10109	MC10509	2.0	60	620,648,650
Dual 3-Input 3-Output OR Gate	MC10110	–	2.4	160	620,648
Dual 3-Input 3-Output NOR Gate	MC10111	–	2.4	160	620,648
Quad Exclusive OR Gate	MC10113	–	2.5	175	620
Triple Line Receiver	MC10114	MC10514	2.4	145	620,648,650
Quad Line Receiver	MC10115	MC10515	2.0	110	620,648,650
Triple Line Receiver	MC10116	MC10516	2.0	85	620,648,650
Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate	MC10117	MC10517	2.3	100	620,648,650
Dual 2-Wide 3-Input OR-AND Gate	MC10118	MC10518	2.3	100	620,648,650
4-Wide 4-3-3-3-Input OR-AND Gate	MC10119	MC10519	2.3	100	620,648,650
4-Wide OR-AND/OR-AND-INVERT Gate	MC10121	MC10521	2.3	100	620,648,650
Triple 4-3-3-Input Bus Driver	MC10123	–	3.0	310	620
Quad MTTL to MECL Translator	MC10124	MC10524	3.5	380	620,648,650
Quad MECL to MTTL Translator	MC10125	MC10525	4.5	380	620,648,650
Dual MECL to MOS Translator	MC10127	–	–	–	620
Bus Driver	MC10128	–	12.0	700	620
Quad Bus Receiver	MC10129	–	10.0	750	620
Dual Latch	MC10130	MC10530	2.5	155	620,648,650
Dual Type D Master-Slave Flip-Flop	MC10131	MC10531	f = 160 MHz	235	620,648,650
Dual Multiplexer With Latch and Common Reset	MC10132	–	3.0	225	620,648
Quad Latch	MC10133	MC10533	4.0	310	620,648,650
Multiplexer with Latch	MC10134	–	3.0	225	620,648
Dual J-K Master-Slave Flip-Flop	MC10135	MC10535	f = 140 MHz	280	620,648,650
Universal Hexadecimal Counter	MC10136	MC10536	f = 150 MHz	625	620,650

① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*External Load Power not included.

Numbers in parenthesis denote pin numbers for F package (Case 650).

FUNCTIONS AND CHARACTERISTICS (continued)

Function	Type ①		Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
	-30 to +85°C	-55 to +125°C			
Universal Decade Counter	MC10137	MC10537	f = 150 MHz	625	620,650
Bi-Quinary Counter	MC10138	–	f = 150 MHz	370	620
64-Bit Random Access Memory (90 Ω)	MCM10140	–	t_{Access} = 15 (max)	420	620,690
Four-Bit Universal Shift Register	MC10141	MC10541	f = 200 MHz	425	620,648,650
64-Bit Random Access Memory (50 Ω)	MCM10142	–	t_{Access} = 10 (max)	420	620
8 x 2 Multiport Register File (RAM)	MCM10143	–	t_{Access} = 10	610	623
256-Bit Random Access Memory	MCM10144	–	t_{Access} = 30 (max)	420	620,690
64-Bit Register File (RAM)	MCM10145	–	t_{Access} = 10	625	620
128-Bit Random Access Memory	MCM10147	–	t_{Access} = 12 (max)	420	620
64-Bit Random Access Memory (50 Ω)	MCM10148	–	t_{Access} = 15 (max)	420	620
1024-Bit Programmable Read Only Memory	MCM10150	–	t_{Access} = 20	–	690
Quad Latch	MC10153	–	4.0	310	620
12-Bit Parity Generator-Checker	MC10160	MC10560	5.0	320	620,648,650
Binary to 1-8 Decoder (Low)	MC10161	MC10561	4.0	315	620,648,650
Binary to 1-8 Decoder (High)	MC10162	MC10562	4.0	315	620,648,650
Error Detection-Correction Circuit	MC10163	–	5.0	520	620
8-Line Multiplexer	MC10164	MC10564	3.0	310	620,648,650
8-Input Priority Encoder	MC10165	–	7.0	545	620,648
5-Bit Magnitude Comparator	MC10166	–	6.0	440	620
Quad Latch	MC10168	–	3.0	310	620
Dual Binary To 1-4 Decoder (Low)	MC10171	MC10571	4.0	325	620,648,650
Dual Binary To 1-4 Decoder (High)	MC10172	MC10572	4.0	325	620,648,650
Quad 2-Input Multiplexer/Latch	MC10173	–	2.5	275	620,648
Dual 4 To 1 Multiplexer	MC10174	MC10574	3.5	305	620,650
Quint Latch	MC10175	MC10575	2.5	400	620
Hex "D" Master-Slave Flip-Flop	MC10176	–	f = 250 MHz	460	620
Triple MECL to NMOS Translator	MC10177	–	–	1.0 W	620
Binary Counter	MC10178	–	f = 150 MHz	370	620
Look-Ahead Carry Block	MC10179	MC10579	3.0 (Cn,P) 4.0 (G)	300	620,648,650
Dual High Speed Adder/Subtractor	MC10180	MC10580	4.5	360	620,648,650
4-Bit Arithmetic Logic Unit/Function Generator	MC10181	MC10581	See Logic Diag.	600	623,649,652
2-Bit Arithmetic Logic Unit/Function Generator	MC10182	–	See Logic Diag.	575	620
Error Detection-Correction Circuit	MC10193	–	7.5	520	620
Hex Inverter/Buffer	MC10195	–	2.0	200	620
Hex "AND" Gate	MC10197	–	2.8	200	620
High Speed Dual 3-Input 3-Output OR Gate	MC10210	–	1.5	160	620
High Speed Dual 3-Input 3-Output NOR Gate	MC10211	–	1.5	160	620
High Speed Dual 3-Input 3-Output OR/NOR Gate	MC10212	–	1.5	160	620
High Speed Triple Line Receiver	MC10216	MC10616	1.8	100	620,648,650
High Speed Dual Type D Master-Slave Flip-Flop	MC10231	MC10631	f = 225 MHz	270	620,648,650
High Speed 2 x 1 Bit Array Multiplier Block	MC10287	–	–	400	620

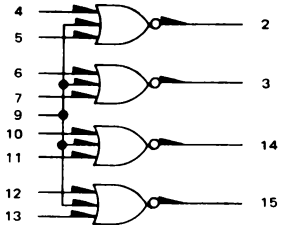
① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*Load Power not included

CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

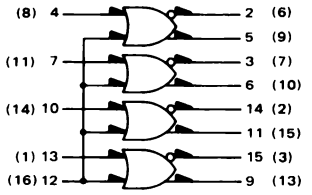
GATES

MC10100
Quad 2-Input NOR Gate With Strobe



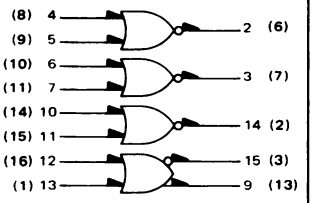
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

MC10101
MC10501
Quad OR/NOR Gate



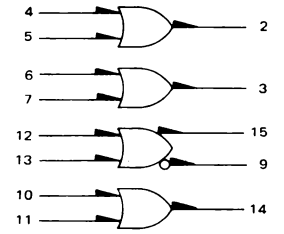
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

MC10102
MC10502
Quad 2-Input NOR Gate



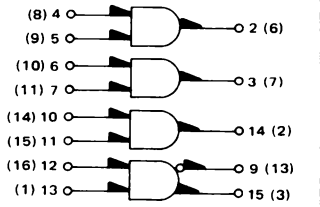
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

MC10103
Quad 2-Input OR Gate



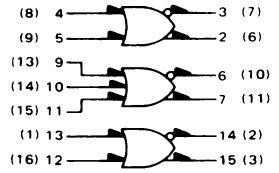
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

MC10104
MC10504
Quad 2-Input AND Gate



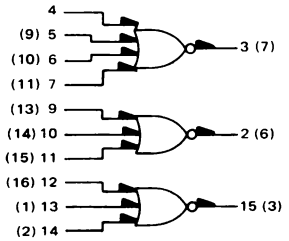
P_D = 35 mW typ/gate (No Load)
t_{pd} = 2.7 ns typ

MC10105
MC10505
Triple 2-3-2 Input OR/NOR Gate



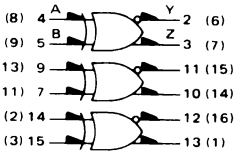
P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

MC10106
MC10506
Triple 4-3-3-Input NOR Gate



P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

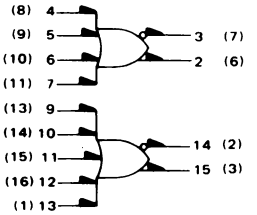
MC10107
MC10507
Triple 2-Input Exclusive OR/Exclusive NOR



$Z = (A \bullet \bar{B}) + (\bar{A} \bullet B)$
$Y = (\bar{A} \bullet \bar{B}) + (A \bullet B)$

P_D = 110 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

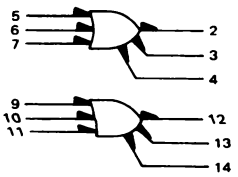
MC10109
MC10509
Dual 4-5-Input OR/NOR Gate



P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

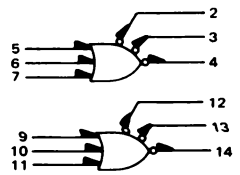
GATES (continued)

MC10110
MC10210
Dual 3-Input 3-Output
OR Gate



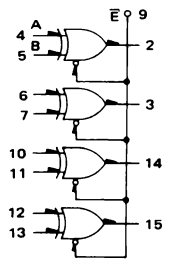
P_D = 160 mW typ/pkg (No Load)
MC10110
t_{pd} = 2.4 ns typ
MC10210
t_{pd} = 1.5 ns typ

MC10111
MC10211
Dual 3-Input 3-Output
NOR Gate



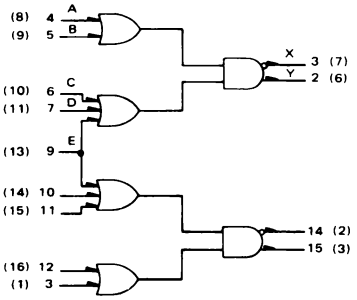
P_D = 160 mW typ/pkg (No Load)
MC10111
t_{pd} = 2.4 ns typ
MC10211
t_{pd} = 1.5 ns typ

MC10113
Quad Exclusive
OR Gate



P_D = 175 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

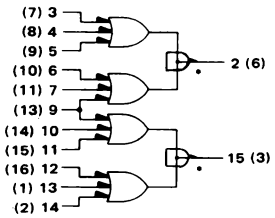
MC10117
MC10517
Dual 2-Wide 2-3-Input
OR-AND/OR-AND-INVERT
Gate



$Y = (A + B) \bullet (C + D + E)$
$\overline{X} = (A + B) \bullet (C + D + E)$

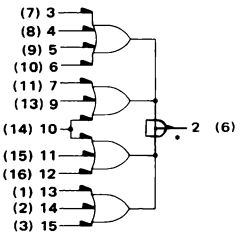
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ

MC10118
MC10518
Dual 2-Wide 3-Input
OR-AND Gate



*Collector Dot
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ

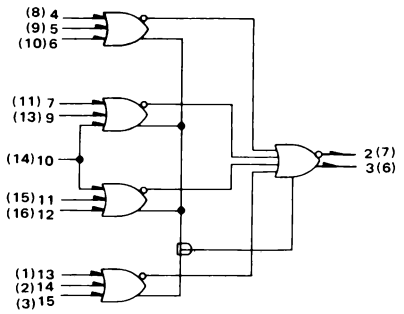
MC10119
MC10519
4-Wide 4-3-3-3 Input
OR-AND-Gate



*Collector Dot
P_D = 100 mV type/pkg (No Load)
t_{pd} = 2.3 ns typ

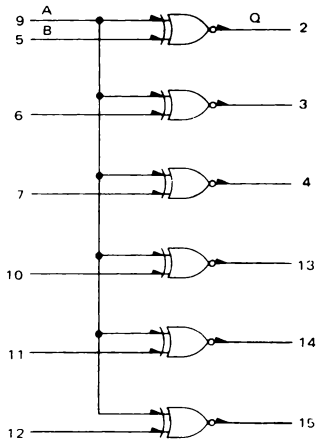
GATES (continued)

MC10121
MC10521
4-Wide
OR-AND/OR-AND-INVERT
Gate



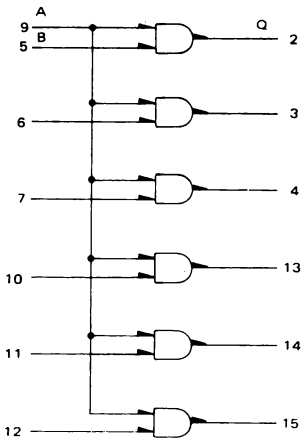
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ

MC10195
Hex Inverter/Buffer



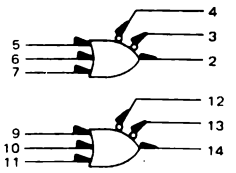
P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ

MC10197
Hex AND Gate



P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ

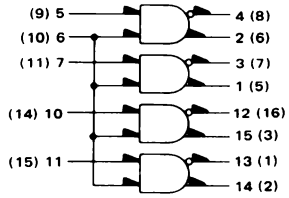
MC10212
High Speed Dual 3-Input
3-Output OR/NOR Gate



V_{CC1} = 1,15
V_{CC2} = 16
V_{EE} = 8
P_D = 160 mW typ/pkg (No Load)
t_{pd} = 1.5 ns typ (All Outputs Loaded)

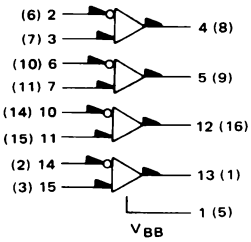
TRANSLATORS

MC10124
MC10525
Quad MTTL to MECL Translator



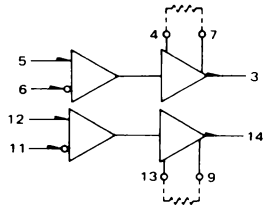
P_D = 380 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ

MC10125
MC10525
Quad MECL to MTTL Translator



P_D = 380 mW typ/pkg (No Load)
t_{pd} = 4.5 ns typ (50% to +1.5 Vdc out)

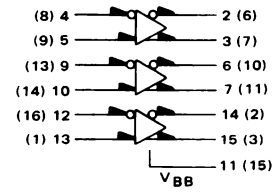
MC10127
Dual MECL to MOS Translator



V_{CC} = Gnd = Pins 1, 2, 15, 16
V_{EE} = Pin 8
V_{SS} = Pins 7, 9

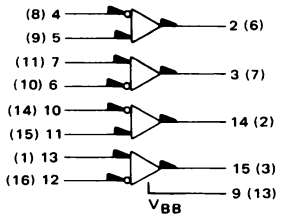
RECEIVERS

MC10114
MC10514
Triple Line Receiver



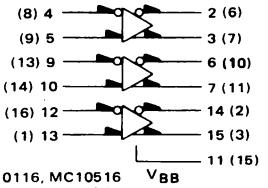
t_{pd} = 2.4 ns typ (Single Ended Input)
t_{pd} = 2.0 ns typ (Differential Input)
P_D = 145 mW typ/pkg (No Load)

MC10115
MC10515
Quad Line Receiver



P_D = 110 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ

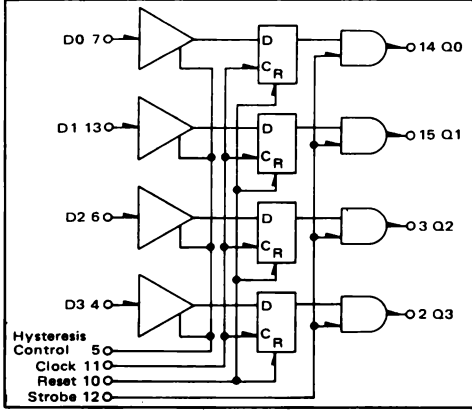
MC10116, MC10516
MC10216, MC10616
Triple Line Receiver



MC10116, MC10516 V_{BB}
P_D = 85 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ

MC10216, MC10616
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 1.8 ns typ

MC10129
Quad Bus Receiver

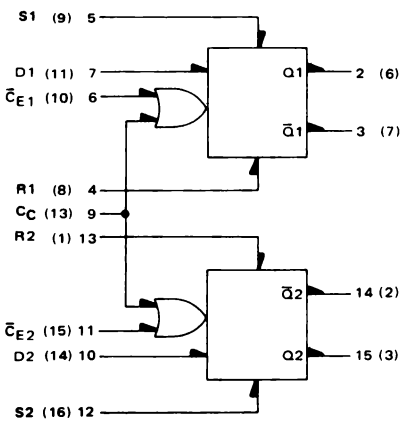


P_D = 750 mW typ/pkg (No Load)
t_{pd} = 10 ns typ

FLIP-FLOPS

MC10131,MC10531
MC10231,MC10631

Dual Type D Master-Slave Flip-Flop



MC10131, MC10531
P_D = 235 mW typ/pkg (No Load)
f = 160 MHz typ

MC10231, MC10631
P_D = 270 mW typ/pkg (No Load)
f = 225 MHz typ

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

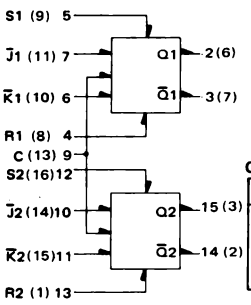
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care
$C = \bar{C}_E + C_C$

MC10135
MC10535

Dual J-K Master-Slave Flip-Flop



R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCK J-K TRUTH TABLE*

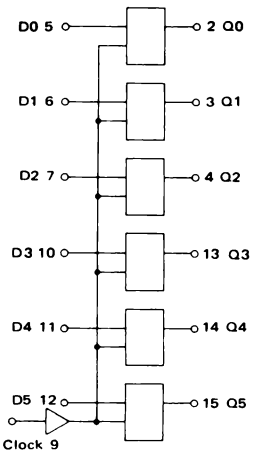
$\bar{J}$	$\bar{K}$	Q_{n+1}
L	L	$\bar{Q}_n$
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\bar{J}$-$\bar{K}$ input-condition present.

P_D = 280 mW typ/pkg (No Load)
f_{tog} = 140 MHz typ

MC10176

Hex "D" Master-Slave Flip-Flop



CLOCKED TRUTH TABLE

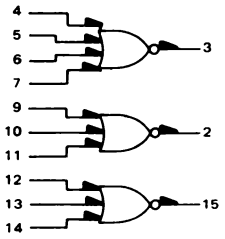
C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ = Don't Care.
*A clock H is a clock transition from a low to a high state.

P_D = 460 mW typ/pkg (No Load)
f_{tog} = 150 MHz typ

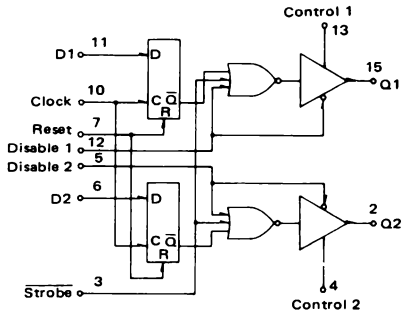
DRIVER

MC10123
Triple 4-3-3 Input Bus Driver



P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

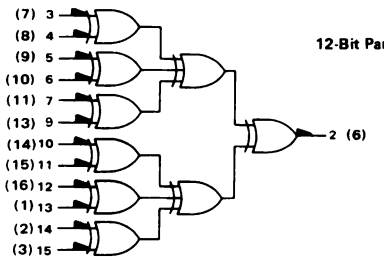
MC10128
Bus Driver



P_D = 700 mW typ/pkg (No Load)
t_{pd} = 12 ns typ

PARITY CHECKER

MC10160
MC10560
12-Bit Parity Generator-Checker

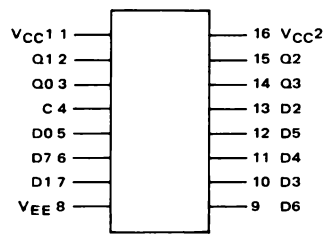


INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

P_D = 320 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ

ENCODER

MC10165
8-Input
Priority Encoder



TRUTH TABLE

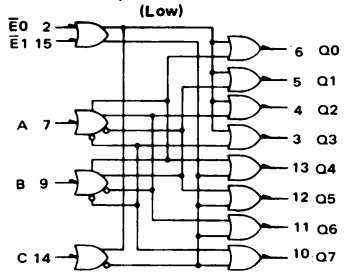
DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	L
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	H
L	L	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	H	L
L	L	L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H
L	L	L	L	H	ϕ	ϕ	ϕ	H	H	L	L
L	L	L	L	L	H	ϕ	ϕ	H	H	L	H
L	L	L	L	L	L	H	ϕ	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

ϕ = Don't Care

P_D = 545 mW typ/pkg
t_{pd} = 7.0 ns typ (Data to Output)

DECODERS

MC10161
MC10561
Binary To 1-8 Decoder
(Low)



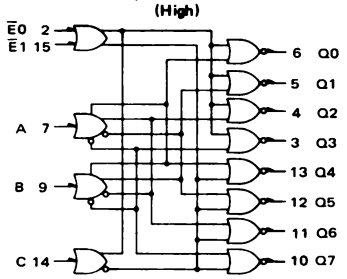
TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E}1$	$\overline{E}0$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H
ϕ	H	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

ϕ = Don't Care

P_D = 315 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

MC10162
MC10562
Binary To 1-8 Decoder
(High)



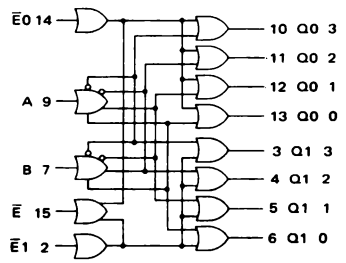
TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{E}0$	$\overline{E}1$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L
ϕ	H	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

ϕ Don't Care

P_D = 315 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

MC10171
Dual Binary To 1-4 Decoder
(Low)



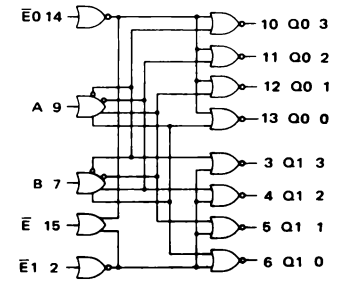
TRUTH TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
$\overline{E}$	$\overline{E}0$	$\overline{E}1$	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	H	L	H	L	H	H	H	L	H	H
L	L	L	L	H	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	ϕ	ϕ	H	H	H	H	L	L	L	L
L	H	L	ϕ	ϕ	H	H	H	H	L	L	L	L
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

ϕ = Don't Care

P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

MC10172
Dual Binary To 1-4 Decoder
(High)



TRUTH TABLE

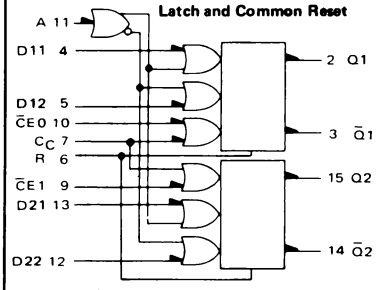
$\overline{E}$	$\overline{E}1$	$\overline{E}0$	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	H	L	L	H	L	L	L	H	L	L
L	H	H	L	H	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	ϕ	L	L	L	L	H	L	L	L
L	H	L	ϕ	L	L	L	L	L	L	H	L	L
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

ϕ = Don't Care

P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

DATA SELECTORS/MULTIPLEXERS

MC10132
Dual Multiplexer With Latch and Common Reset



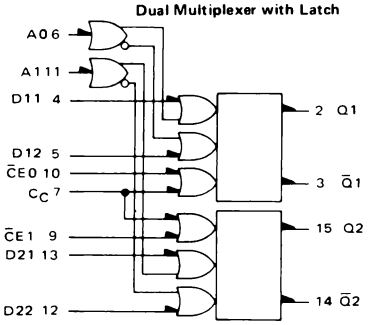
TRUTH TABLE

R	D	C	CE	Q_n†1
ϕ	L	L	L	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
ϕ	H	L	L	H
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	ϕ	ϕ	H	L

ϕ = Don't Care

P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

MC10134
Dual Multiplexer with Latch



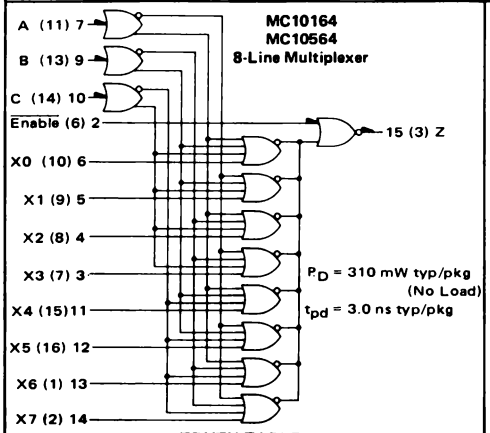
TRUTH TABLE

C	A0	D11	D12	Q_n+1
L	L	L	ϕ	L
L	L	H	ϕ	H
L	H	ϕ	L	L
L	H	ϕ	H	H
H	ϕ	ϕ	ϕ	Q_n

ϕ = Don't Care
C = $\overline{C_E}$ + C_C

P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

MC10164
MC10564
8-Line Multiplexer



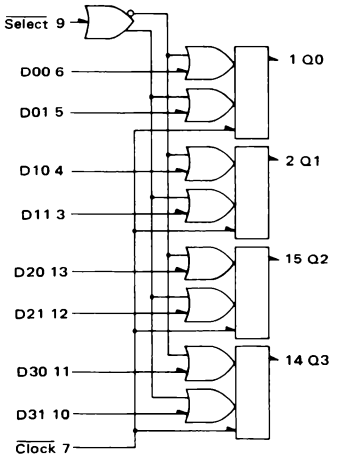
TRUTH TABLE

ENABLE	ADDRESS INPUTS C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ/pkg

MC10173
Quad 2-Input Multiplexer/Latch



TRUTH TABLE

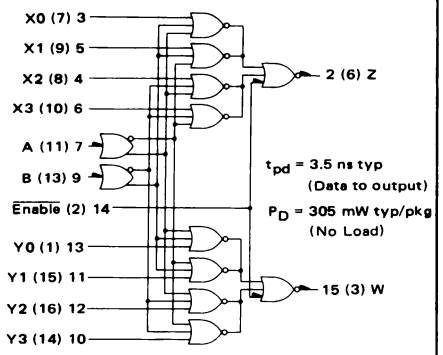
SELECT	CLOCK	$Q0_{n+1}$
H	L	D00
L	L	D01
ϕ	H	$Q0_n$

ϕ = Don't Care

P_D = 275 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

DATA SELECTORS/MULTIPLEXERS (continued)

MC10174 / MC10574
Dual 4 to 1 Multiplexer

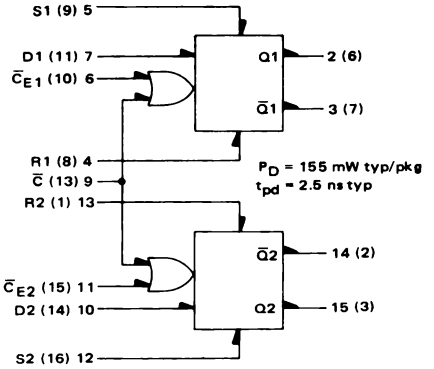


TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Z	W
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ϕ = Don't Care

MC10130 / MC10530
Quad Latch



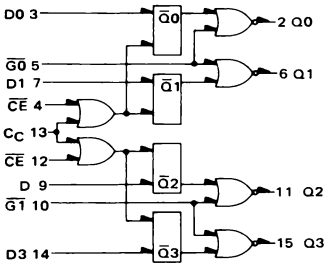
TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
ϕ	L	H	Q_n
ϕ	H	L	Q_n
ϕ	H	H	Q_n

ϕ = Don't Care.

LATCHES

MC10133 / MC10533
Quad Latch



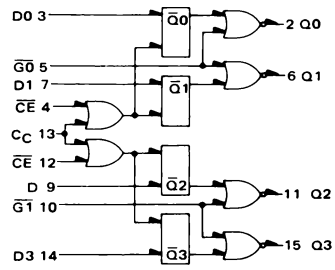
P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

ϕ = Don't Care
$C = \overline{C}_C + CE$

MC10153
Quad Latch



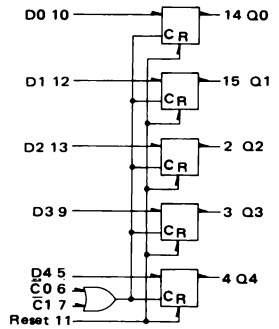
P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	L	H	H

ϕ = Don't Care
$C = \overline{C}_C + CE$

MC10175 / MC10575
Quint Latch



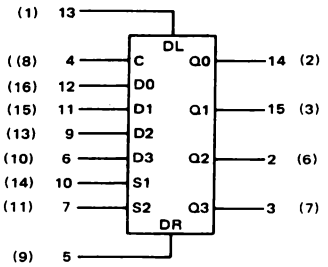
P_D = 400 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

TRUTH TABLE

D	C0	C1	Reset	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
ϕ	H	ϕ	L	Q_n
ϕ	ϕ	H	L	Q_n
ϕ	H	ϕ	H	L
ϕ	ϕ	H	H	L

SHIFT REGISTERS

MC10141
MC10541
Four-Bit Universal Shift Register



TRUTH TABLE

SELECT			OUTPUTS			
S1	S2	OPERATING MODE	$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

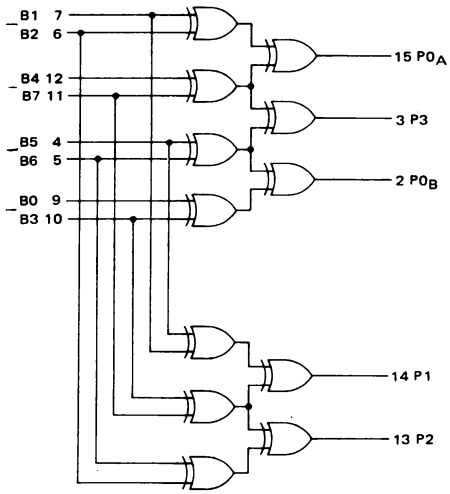
*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).

P_D = 425 mW typ/pkg
f_{shift} = 200 MHz typ

ERROR DETECTION-CORRECTION

MC10163 • MC10193
Error Detection-Correction Circuit

MC10163 LOGIC DIAGRAM

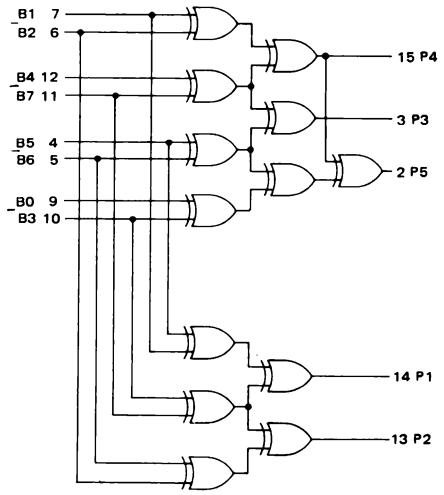


IBM CODE

$P0_A$ = B1, B2, B4, B7
$P0_B$ = B0, B3, B5, B6
P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7

P_D = 520 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ

MC10193 LOGIC DIAGRAM



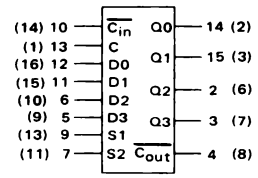
MOTOROLA CODE

P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7
P4 = B1, B2, B4, B7
P5 = Byte (B0, 1, 2, 3, 4, 5, 6, 7)

P_D = 520 mW typ/pkg (No Load)
t_{pd} = 7.5 ns typ (Pin 7 to Pin 2)

COUNTERS

MC10136
MC10536
Universal Hexadecimal Counter



FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

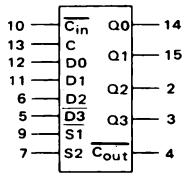
P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	L	H	ϕ	ϕ	ϕ	L	H	H	H	H	H	H
L	L	ϕ	ϕ	ϕ	ϕ	H	H	L	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	ϕ	H	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	L	H
L	L	ϕ	ϕ	ϕ	ϕ	ϕ	L	H	H	H	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
H	L	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	H	H	H	L
H	L	ϕ	ϕ	ϕ	ϕ	H	ϕ	L	H	H	L	H
H	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L
H	H	ϕ	ϕ	ϕ	ϕ	H	ϕ	H	L	L	L	L

ϕ = Don't care.
*Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

MC10137
Universal Decade Counter



FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

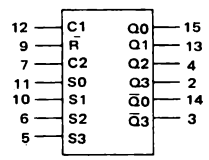
P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	ϕ	H	H	H	H	L	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	L	L	H	H
L	L	H	ϕ	ϕ	ϕ	L	H	L	H	L	H	H
L	L	H	ϕ	ϕ	ϕ	H	H	H	H	L	H	H
L	L	H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	H
L	L	H	ϕ	ϕ	ϕ	ϕ	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	H	H
H	L	ϕ	ϕ	ϕ	ϕ	H	L	H	H	L	H	L
H	L	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	L	L	H

ϕ = Don't care.
*Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

MC10138
Bi-Quinary Counter



COUNTER TRUTH TABLES

BI-QUINARY
(Clock connected to C2 and Q3 connected to C1)

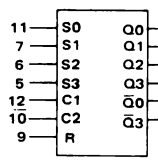
COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	H	L	L	H
9	L	H	L	H

BCD
(Clock connected to C1 and Q0 connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

P_D = 370 mW typ/pkg (No Load)
f_{tog} = 150 MHz typ

MC10178
Binary Counter



P_D = 370 mW typ/pkg (No Load)
f_{tog} = 150 MHz (Typ)

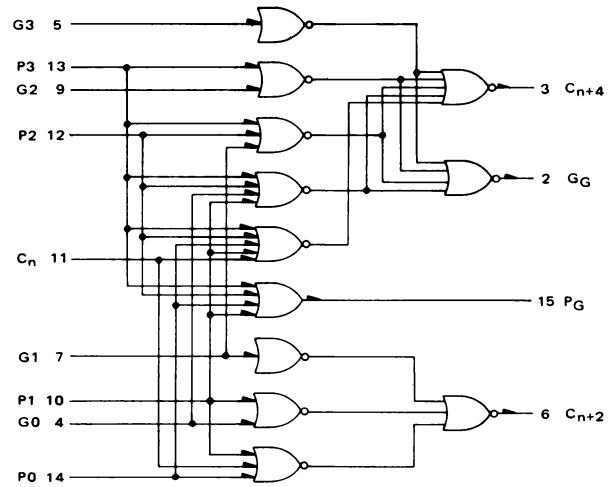
TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	ϕ	ϕ	L	L	L	L
L	H	L	L	H	ϕ	ϕ	H	No Count		
L	L	H	L	L	H	ϕ	L	H	L	H
L	L	L	H	L	ϕ	H	No Count			
L	L	L	L	L	↓	↓	L	L	L	L
L	L	L	L	L	↓	↓	H	L	L	L
L	L	L	L	L	↓	↓	L	H	L	L
L	L	L	L	L	↓	↓	H	H	L	L
L	L	L	L	L	↓	↓	L	L	H	L
L	L	L	L	L	↓	↓	H	L	H	L
L	L	L	L	L	↓	↓	L	H	H	L
L	L	L	L	L	↓	↓	H	H	H	L
L	L	L	L	L	↓	↓	L	L	L	H
L	L	L	L	L	↓	↓	H	L	L	H
L	L	L	L	L	↓	↓	L	H	L	H
L	L	L	L	L	↓	↓	H	H	L	H
L	L	L	L	L	↓	↓	L	L	H	H
L	L	L	L	L	↓	↓	H	L	H	H
L	L	L	L	L	↓	↓	L	H	H	H
L	L	L	L	L	↓	↓	H	H	H	H

** ϕ = Don't Care
Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

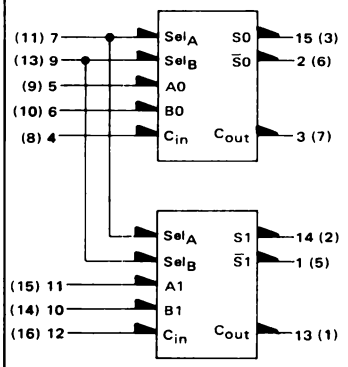
ADDER AND ARITHMETIC FUNCTIONS

MC10179
Look-Ahead Carry Block



P_D = 300 mW typ/pkg
t_{pd} = 3.0 ns typ (Carry, Propagate)
4.0 ns typ (Generate)

MC10180
MC10580
Dual High Speed Adder/Subtractor



P_D = 360 mW typ/pkg

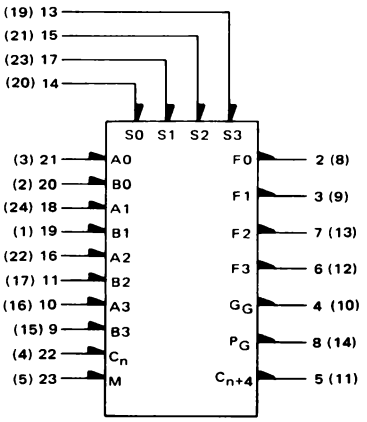
t_{pd} (typ)
C_{in} to C_{out} = 2.2 ns
A0 to S0 = 4.5 ns
A0 to C_{out} = 4.5 ns

Positive Logic Only
$A' = A \oplus \overline{Sel_A} = A \odot Sel_A$
$B' = B \oplus \overline{Sel_B} = B \odot Sel_B$

FUNCTION SELECT TABLE

Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

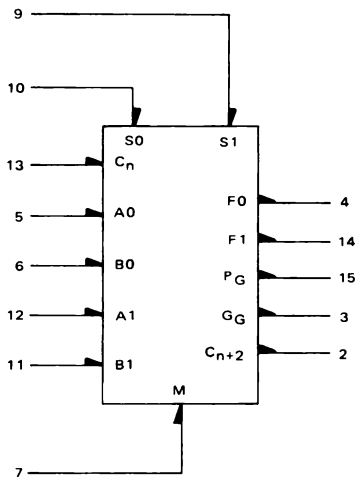
MC10181
MC10581
4-Bit Arithmetic Logic Unit/Function Generator



P_D = 600 mW typ/pkg (No Load)
t_{pd} (typ): A1 to F = 6.5 ns
C_n to C_{n+4} = 3.1 ns
A1 to P_G = 5.0 ns
A1 to G_G = 4.5 ns
A1 to C_{n+4} = 5.0 ns

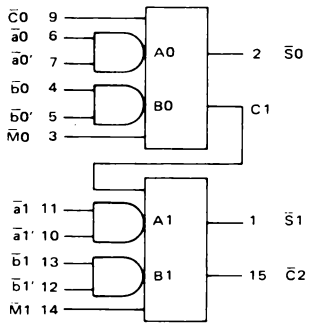
ADDER AND ARITHMETIC FUNCTIONS (continued)

MC10182
2-Bit Arithmetic Logic
Unit/Function Generator



P_D = 575 mW typ/pkg (No Load)
t_{pd} (typ): A1 to F = 7.5 ns
C_n to C_{n+2} = 2.7 ns
A1 to P_G = 6.5 ns
A1 to G_G = 5.5 ns
A1 to C_{n+2} = 7.0 ns

MC10287
High Speed
2 x 1 Bit Array Multiplier

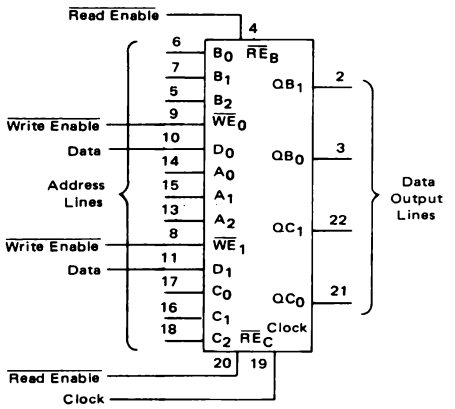


P_D = 400 mW typ/pkg (No Load)
t_{pd}: (Outputs loaded 1 kΩ to V_{EE})
C0 to C2 1.7 ns typ
a0 to C2 2.8
a0 to S0 2.7
b0 to S0 3.1
a0 to S1 3.9
b0 to S1 4.4
M0 to S1 8.7

V_{CC} = Pin 16
V_{EE} = Pin 8

MEMORIES

MCM10143
8 x 2 Multiport Register File (RAM)

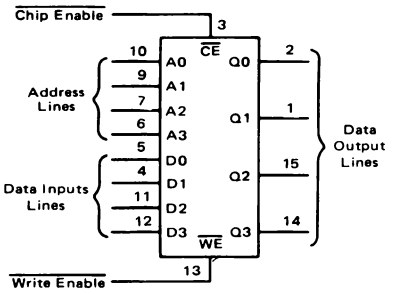


t_{pd}:
- Clock to Data out = 5 ns (typ) (Read Selected)
- Address to Data out = 10 ns (typ) (Clock High)
- Read Enable to Data out = 3.5 ns (typ) (Clock high, Addresses present)

P_D = 610 mW typ/pkg (No Load)

V_{CC0} = Pin 1
V_{CC1} = Pin 23
V_{CC} = Pin 24
V_{EE} = Pin 12

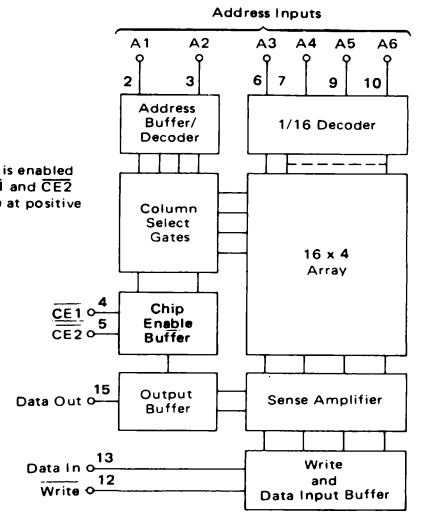
MCM10145
64-Bit Register File (RAM)



V_{CC} = Pin 16
V_{EE} = Pin 8

P_D = 625 mW typ/pkg (No Load)
Access Time = 10 ns typ

MCM10140 (90 Ω)
MCM10142 (50 Ω)
MCM10148 (50 Ω)
64-Bit Random Access Memory

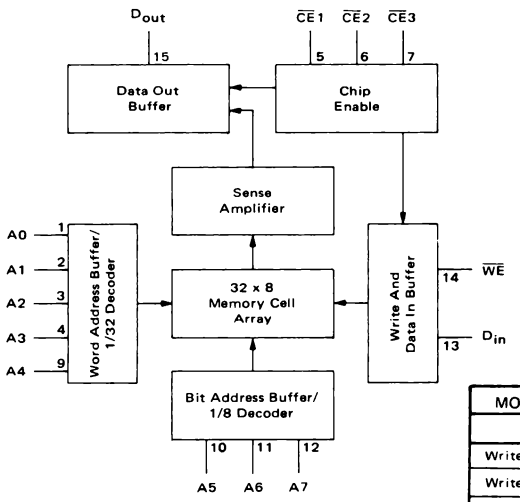


The Chip is enabled when $\overline{CE1}$ and $\overline{CE2}$ inputs are at positive logic "0"

P_D = 420 mW typ/pkg
t_{Access} = 15 ns (max) MCM10140, MCM10148
= 10 ns (max) MCM10142

MEMORIES (continued)

MCM10144
256 Bit Random Access Memory



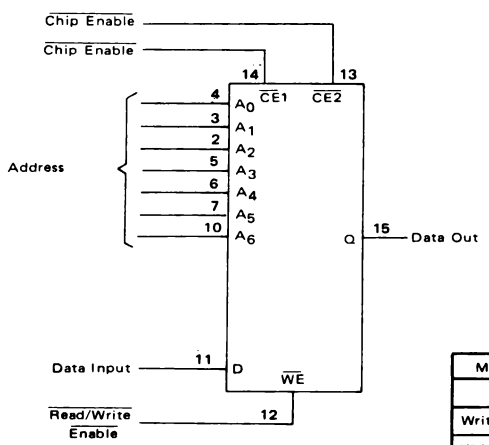
V_{CC} = Pin 16
V_{EE} = Pin 8
t_{Access} = 30 ns (max) (Address Inputs)

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CE}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care

MCM10147
128 Bit Random Access Memory



P_D = 415 mW typ/pkg (No Load)
t_{Access} = 10 ns typ (Address Inputs)

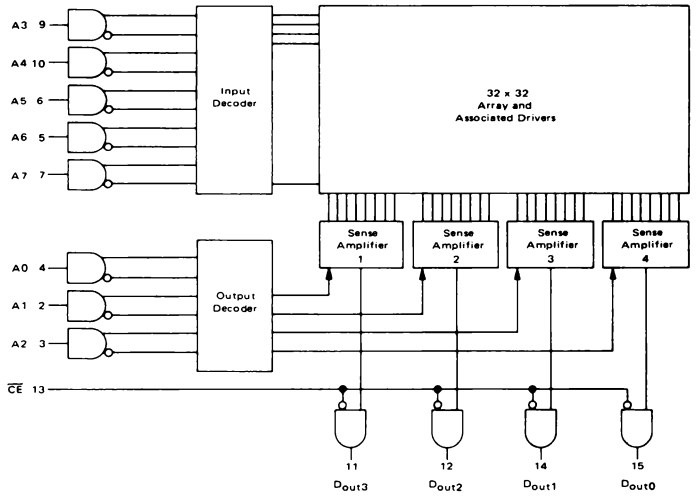
TRUTH TABLE

MODE	INPUT				OUTPUT
	$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	D	Q
Write "0"	L	L	L	L	L
Write "1"	L	L	L	H	L
Read	L	L	H	ϕ	Q
Disabled	H	L	ϕ	ϕ	L
	L	H	ϕ	ϕ	L

ϕ = Don't Care

MEMORIES (continued)

MCM10150
1024-Bit Programmable
Read Only Memory

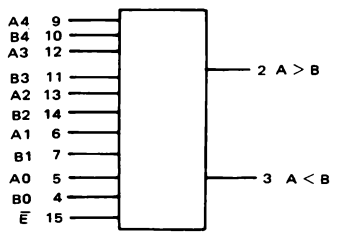


COMPARATOR

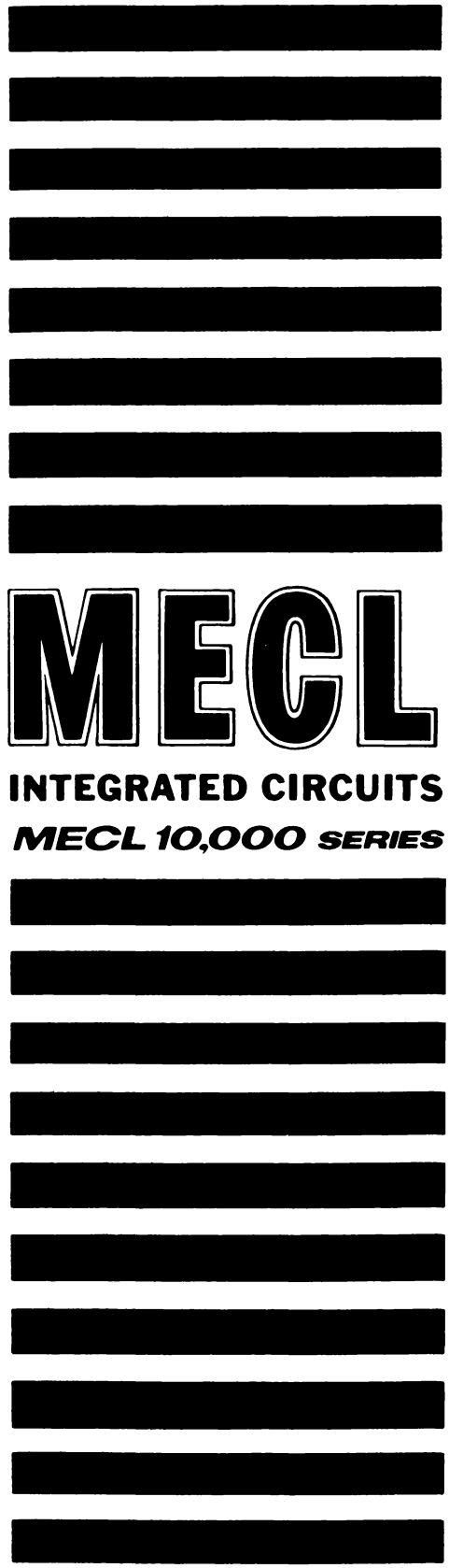
MC10166
5-Bit Magnitude
Comparator

TRUTH TABLE

Inputs			Outputs	
E	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L



P_D = 440 mW typ/pkg (No Load)
t_{pd} = Data to output 6.0 ns typ
E to output 2.5 ns typ


MECL
INTEGRATED CIRCUITS
MECL 10,000 SERIES

QUAD 2-INPUT NOR GATE
WITH STROBE

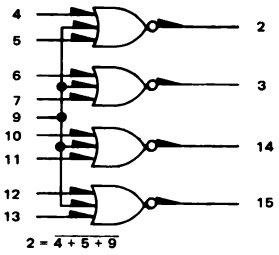
MC10100

Advance Information

The MC10100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates. Input pulldown resistors eliminate the need to tie unused inputs to a voltage supply. Open emitter outputs permit wire-ORing and direct connection to busses.

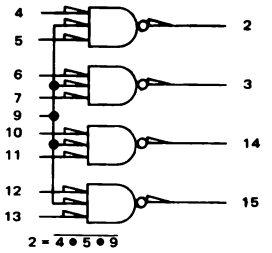
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

POSITIVE LOGIC

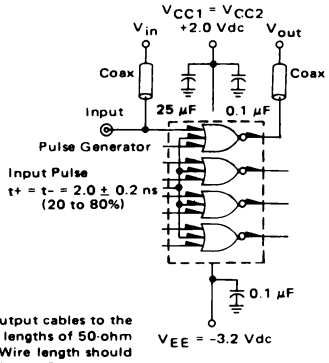


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

NEGATIVE LOGIC



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

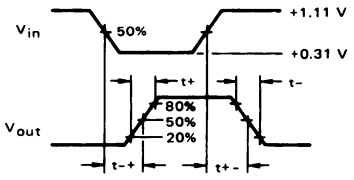


All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs connected to a 50-ohm resistor to ground.

50-ohm termination to ground located in each scope channel input.

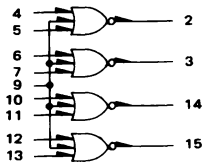
PROPAGATION DELAY

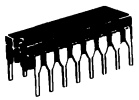


See General Information Section for packaging and maximum ratings.
This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





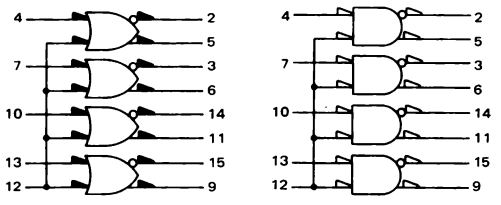
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10100L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	21	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4*	–	–	–	–	245	–	–	μAdc	4*	–	–	–	8	1,16
		9	–	–	–	–	470	–	–	μAdc	9	–	–	–	8	1,16
	I_{inL}	4*	–	–	0.5	–	–	–	–	μAdc	–	4*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,5,9	–	–	–	8	1,16
		14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,10,11	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.090	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	9	8	1,16
		3	-1.090	–	-0.980	–	–	-0.910	–	↓	–	–	–	9	↓	↓
		14	-1.090	–	-0.980	–	–	-0.910	–	↓	–	–	–	9	↓	↓
		15	-1.090	–	-0.980	–	–	-0.910	–	↓	–	–	–	9	↓	↓
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	9	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	9	–	↓	↓
		14	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	9	–	↓	↓
		15	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	9	–	↓	↓
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2-}	2	–	–	–	2.0	–	–	–	ns	–	–	4	2	8	1,16
	t_{4-2+}	2	–	–	–	↓	–	–	–	↓	–	–	↓	↓	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	–	–	–	↓	–	–	–	↓	–	–	↓	↓	↓	↓
Fall Time (20% to 80%)	t_{2-}	2	–	–	–	↓	–	–	–	↓	–	–	↓	↓	↓	↓

*Individually test each input applying V_{IH} or V_{IL} to input under test.

MC10101

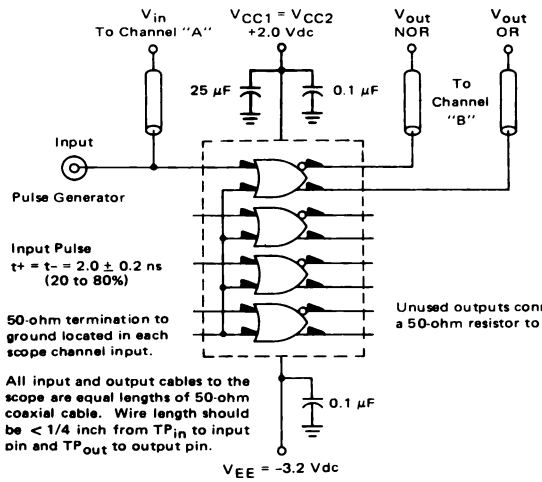


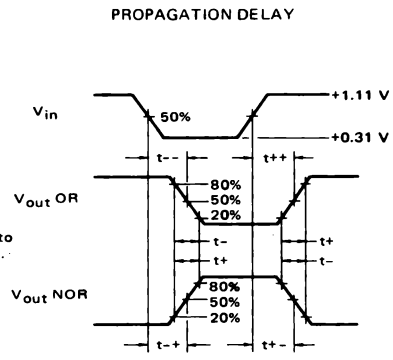
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

The MC10101 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

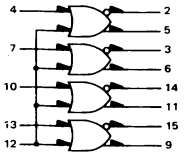


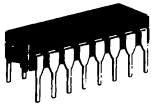


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





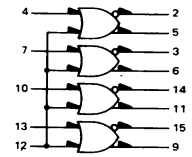
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10101L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	µAdc	4	–	–	–	8	1,16
		12	–	–	–	–	535	–	–	µAdc	12	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	µAdc	–	4	–	–	8	1,16
		12	–	–	0.5	–	–	–	–	µAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	5	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	–	–		8	1,16
		5	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		4	–		–		
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		–	–	–	–		
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		–	–	–	–		
Logic "0" Output Voltage	V_{OL}	5	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		5	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–	–	–	–		
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		12	–	–			
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		4	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	5	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–		12	–	8	1,16
		5	-1.080		-0.980	–	–	-0.910	–		–	–	4	–		
		2	-1.080	–	-0.980	–	–	-0.910	–		–	–	–	12		
		2	-1.080	–	-0.980	–	–	-0.910	–		–	–	–	4		
Logic "0" Threshold Voltage	V_{OLA}	5	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	12	8	1,16
		5	–	-1.655		–	-1.630	–	-1.595		–	–	–	4		
		2	–	-1.655	–	–	-1.630	–	-1.595		–	–	12	–		
		2	–	-1.655	–	–	-1.630	–	-1.595		–	–	4	–		
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2-}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–		4	2	8	1,16
	t_{4-2+}	2									–			2		
	t_{4+5+}	5									–			5		
	t_{4-5-}	5									–	–		5		
Rise Time	t_{2+}	2	1.1	3.6	1.1		3.3	1.1	3.7		–			2		
(20 to 80%)	t_{5+}	5									–			5		
Fall Time	t_{2-}	2									–	–		2		
(20 to 80%)	t_{5-}	5									–	–		5		

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.



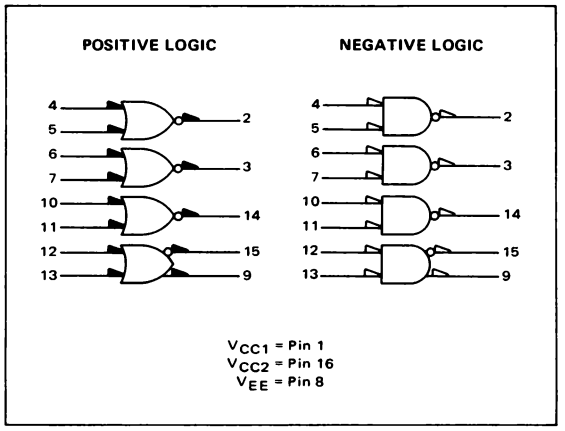
P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10101P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
		12	–	–	–	–	535	–	–	μAdc	12	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
		12	–	–	0.5	–	–	–	–	μAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	5	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	–	–	–	8	1,16
		5	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		4	–	–	–		
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		–	–	–	–		
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		–	–	–	–		
Logic "0" Output Voltage	V_{OL}	5	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		5	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–	–	–	–		
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		12	–	–	–		
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		4	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	5	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	12	–	8	1,16
		5	-1.080	–	-0.980	–	–	-0.910	–		–	–	4	–		
		2	-1.080	–	-0.980	–	–	-0.910	–		–	–	–	12		
		2	-1.080	–	-0.980	–	–	-0.910	–		–	–	–	4		
Logic "0" Threshold Voltage	V_{OLA}	5	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	12	8	1,16
		5	–	-1.655	–	–	-1.630	–	-1.595		–	–	–	4		
		2	–	-1.655	–	–	-1.630	–	-1.595		–	–	12	–		
		2	–	-1.655	–	–	-1.630	–	-1.595		–	–	4	–		
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2-}	2	–	–	1.0	2.0	2.9	–	–	ns	–	–	4	2	8	1,16
	t_{4-2+}	2	–	–				–	–		–	–		2		
	t_{4+5+}	5	–	–				–	–		–	–		5		
	t_{4-5-}	5	–	–				–	–		–	–		5		
Rise Time (20 to 80%)	t_{2+}	2	–	–	1.1		3.3	–	–		–	–		2		
	t_{5+}	5	–	–				–	–		–	–		5		
Fall Time (20 to 80%)	t_{2-}	2	–	–				–	–		–	–		2		
	t_{5-}	5	–	–				–	–		–	–		5		

QUAD 2-INPUT NOR GATE

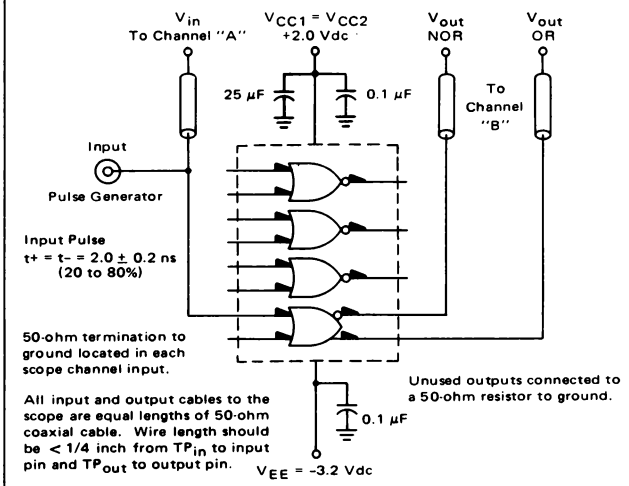
MC10102

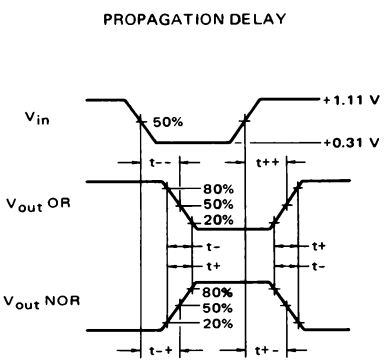


The MC10102 is a quad 2-input NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

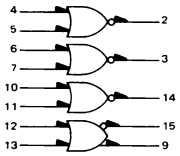


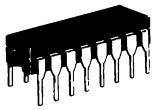


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





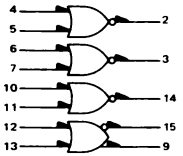
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10102L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8				20	26			mAdc	–				8	1,16
Input Current	I_{inH}	12		–			265		–	μAdc	12				8	1,16
	I_{inL}	12			0.5	–		–		μAdc		12			8	1,16
Logic "1" Output Voltage	V_{OH}	9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12				8	1,16
		9	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		13	–				
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700			–				
		15	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		–	–				
Logic "0" Output Voltage	V_{OL}	9	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	–	–			8	1,16
		9	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615			–				
		15	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		12					
		15	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		13					
Logic "1" Threshold Voltage	V_{OHA}	9	-1.080		-0.980			-0.910		Vdc			12		8	1,16
		9	-1.080		-0.980			-0.910					13			
		15	-1.080		-0.980			-0.910						12		
		15	-1.080	–	-0.980			-0.910	–					13		
Logic "0" Threshold Voltage	V_{OLA}	9		-1.655			-1.630		-1.595	Vdc				12	8	1,16
		9	–	-1.655			-1.630		-1.595					13		
		15	–	-1.655			-1.630	–	-1.595				12			
		15	–	-1.655		–	-1.630	–	-1.595				13			
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{12+15-}	15	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	12	15	8	1,16
	t_{12-15+}	15									–	–		15		
	t_{12+9+}	9									–	–		9		
	t_{12-9-}	9									–	–		9		
Rise Time (20 to 80%)	t_{15+}	15	1.1	3.6	1.1		3.3	1.1	3.7		–	–		15		
	t_{9+}	9									–	–		9		
Fall Time (20 to 80%)	t_{15-}	15									–	–		15		
	t_{9-}	9									–	–		9		

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.



P SUFFIX
PLASTIC PACKAGE
CASE 648

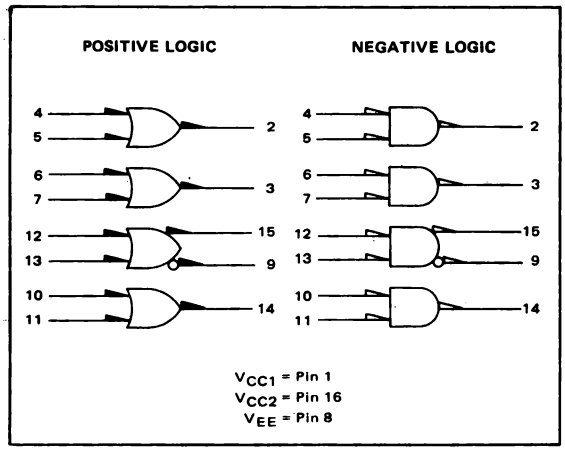
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10102P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8			–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	12			–	–	265	–	–	μAdc	12	–	–	–	8	1,16
	I_{inL}	12			0.5	–	–	–	–	μAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	–	–	–	8	1,16
		9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		13	–	–	–		
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		–	–	–	–		
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		–	–	–	–		
Logic "0" Output Voltage	V_{OL}	9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–	–	–	–		
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		12		–	–		
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		13	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	9	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	12	—	8	1,16
		9	-1.080	–	-0.980	–	–	-0.910	–		–	–	13	–		
		15	-1.080	–	-0.980	–	–	-0.910	–		–		–	12		
		15	-1.080	–	-0.980	–	–	-0.910	–		–	–	–	13		
Logic "0" Threshold Voltage	V_{OLA}	9	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	12	8	1,16
		9	–	-1.655	–	–	-1.630		-1.595		–	–	–	13		
		15	–	-1.655	–	–	-1.630	–	-1.595		–	–	12	–		
		15	–	-1.655	–	–	-1.630	–	-1.595		–	–	13	–		
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{12+15-}	15	–	–	1.0	2.0	2.9	–	–	ns	–	–	12	15	8	1,16
	t_{12-15+}	15	–	–				–	–		–	–		15		
	t_{12+9+}	9	–	–				–	–		–	–		9		
	t_{12-9-}	9	–	–				–	–		–	–		9		
Rise Time	t_{15+}	15	–	–	1.1		3.3	–	–		–	–		15		
(20 to 80%)	t_{9+}	9	–	–				–	–		–	–		9		
Fall Time	t_{15-}	15	–	–				–	–		–	–		15		
(20 to 80%)	t_{9-}	9	–	–				–	–		–	–		9		

MC10103

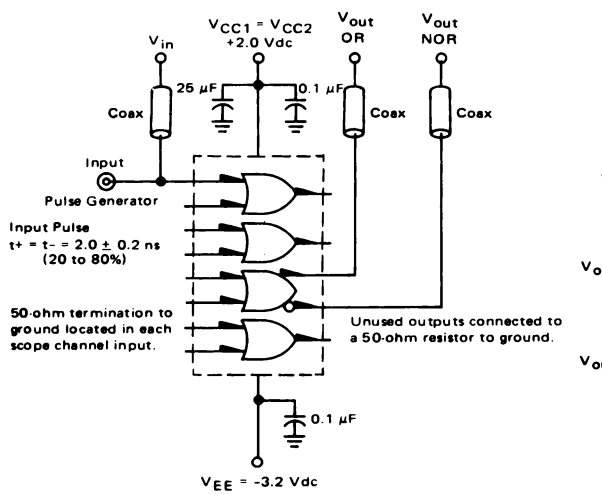
Advance Information

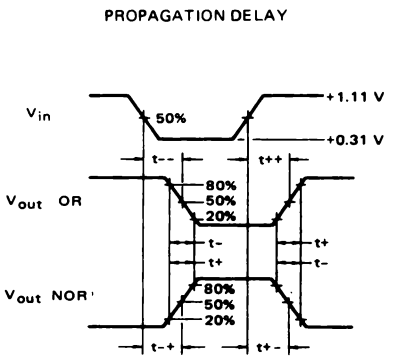
The MC10103 is a high-speed, low-power quad 2-input OR gate. One of the gates has both OR and NOR outputs. Input pulldown resistors eliminate the need to tie down unused inputs.



P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



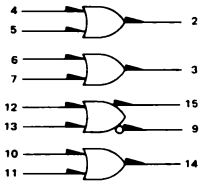


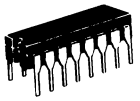
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.
Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

See General Information section for packaging and maximum ratings.
This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10103L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	21	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4*	–	–	–	–	245	–	–	μAdc	4*	–	–	–	8	1,16
	I_{inL}	4*	–	–	0.5	–	–	–	–	μAdc	–	4*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,5	–	–	–	8	1,16
		9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	12,13	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4,5	–	8	1,16
		9	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	12,13	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4,5	8	1,16
		9	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	12,13	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	–	–	2.0	–	–	–	ns	–	–	4	2	8	1,16
	t_{12+9-}	9	–	–	–	↓	–	–	–	↓	–	–	12	9	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	–	–	–		–	–	–		–	–	4	2		
Fall Time (20% to 80%)	t_{2-}	2	–	–	–		–	–	–		–	–	4	2		

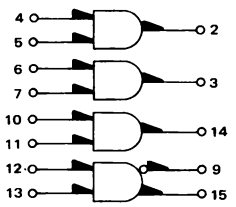
*Individually test each input applying V_{IH} or V_{IL} to input under test.

MC10104

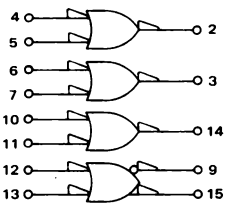
P_D = 35 mW typ/gate (No load)
t_{pd} = 2.7 ns typ
Output Rise and Fall Times:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

The MC10104 provides a very useful low power, high speed logic AND function. High Z input pulldown resistors allow high dc and ac fanouts and eliminate the need to tie unused inputs to an external supply. The open emitter outputs allow maximum flexibility in the selection of termination techniques and minimize the power requirements when driving transmission lines. Open emitter outputs also allow wire-ORing capability, which is very useful in control, bussing, and communications in high speed central processors, high speed peripherals, digital communications systems, minicomputers and instrumentation.

POSITIVE LOGIC

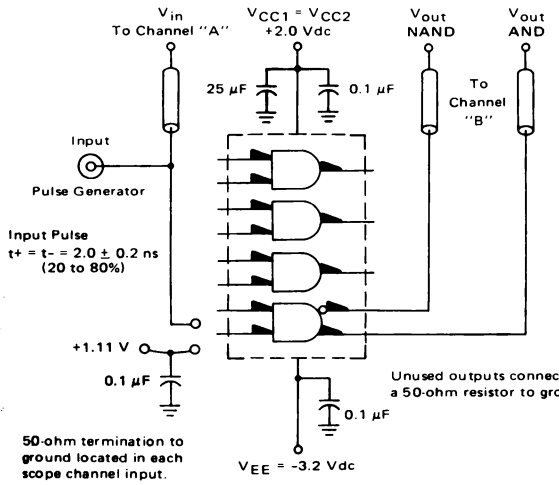


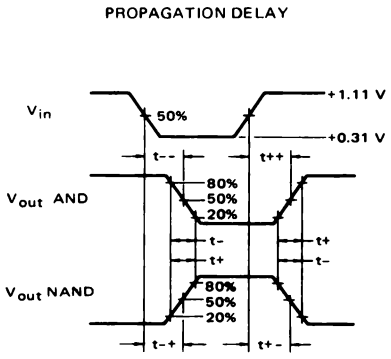
NEGATIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



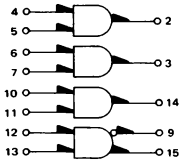


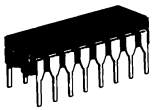
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.
Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

See General Information Section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

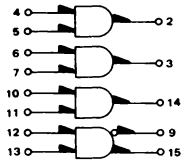
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

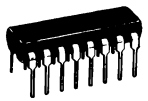
Characteristic	Symbol	Test	MC10104L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BLEOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	35	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}*	12	–	–	–	–	265	–	–	µAdc	12,13	–	–	–	8	1,16
		13	–	–	–	–	220	–	–	µAdc	13	–	–	–	8	1,16
	I_{inL}	12	–	–	0.5	–	–	–	–	µAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12,13	–	–	–	8	1,16
		9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	12,13	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	9	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	12	8	1,16
		9	-1.080	–	-0.980	–	–	-0.910	–	↓	–	–	–	13	↓	↓
		15	-1.080	–	-0.980	–	–	-0.910	–	↓	12	–	13	–	↓	↓
		15	-1.080	–	-0.980	–	–	-0.910	–	↓	13	–	12	–	↓	↓
Lgoic "0" Threshold Voltage	V_{OLA}	9	–	-1.655	–	–	-1.630	–	-1.595	Vdc	12	–	13	–	8	1,16
		9	–	-1.655	–	–	-1.630	–	-1.595	↓	13	–	12	–	↓	↓
		15	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	–	12	↓	↓
		15	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	–	13	↓	↓
Switching Times* (50-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{12+15+}	15	1.0	4.3	1.0	2.2	4.0	1.0	4.2	ns	13	–	12	15	8	1,16
	t_{12-15-}	15	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	15	↓	↓
	t_{12+9-}	9	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	9	↓	↓
	t_{12-9+}	9	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	9	↓	↓
	t_{13+15+}	15	↓	↓	↓	2.7	↓	↓	↓	↓	12	–	13	15	↓	↓
	t_{13+9-}	9	↓	↓	↓	2.7	↓	↓	↓	↓	12	–	13	9	↓	↓
Rise Time (20 to 80%)	t_{15+}	15	1.5	3.7	1.5	2.0	3.5	1.5	3.6	↓	↓	–	↓	15	↓	↓
	t_{9+}	9	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	9	↓	↓
Fall Time (20 to 80%)	t_{15-}	15	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	15	↓	↓
	t_{9-}	9	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	9	↓	↓

*Inputs 4, 7, 10, and 13 will behave similarly for ac and I_{inH} values.
Inputs 5, 6, 11, and 12 will behave similarly for ac and I_{inH} values.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





P SUFFIX
PLASTIC PACKAGE
CASE 648

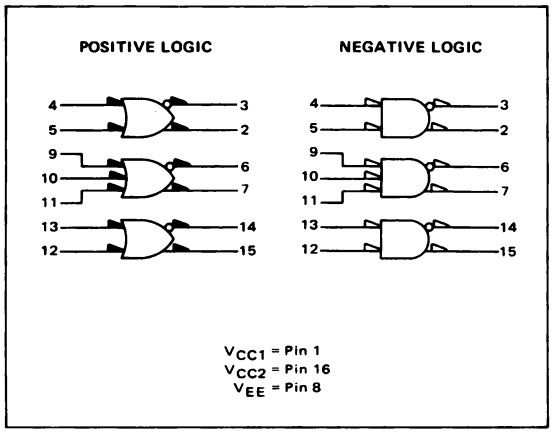
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Test	MC10104P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BLEOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	35	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}*	12	–	–	–	–	265	–	–	μAdc	12,13	–	–	–	8	1,16
		13	–	–	–	–	220	–	–	μAdc	13	–	–	–	8	1,16
	I_{inL}	12	–	–	0.5	–	–	–	–	μAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12,13	–	–	–	8	1,16
		9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	12,13	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	9	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	12	8	1,16
		9	-1.080	–	-0.980	–	–	-0.910	–		–	–	–	13		
		15	-1.080	–	-0.980	–	–	-0.910	–		12	–	13	–		
		15	-1.080	–	-0.980	–	–	-0.910	–		13	–	12	–		
Lgoic "0" Threshold Voltage	V_{OLA}	9	–	-1.655	–	–	-1.630	–	-1.595	Vdc	12	–	13	–	8	1,16
		9	–	-1.655	–	–	-1.630	–	-1.595		13	–	12	–		
		15	–	-1.655	–	–	-1.630	–	-1.595		–	–	–	12		
		15	–	-1.655	–	–	-1.630	–	-1.595		–	–	–	13		
Switching Times* (50-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{12+15+}	15	–	–	1.0	2.2	4.0	–	–	ns	13	–	12	15	8	1,16
	t_{12-15-}	15	–	–				–	–			–		15		
	t_{12+9-}	9	–	–				–	–			–		9		
	t_{12-9+}	9	–	–				–	–			–		9		
	t_{13+15+}	15	–	–		2.7		–	–		12	–	13	15		
	t_{13+9-}	9	–	–		2.7		–	–		12	–	13	9		
Rise Time (20 to 80%)	t_{15+}	15	–	–	1.5	2.0	3.5	–	–			–		15		
	t_{9+}	9	–	–				–	–			–		9		
Fall Time (20 to 80%)	t_{15-}	15	–	–				–	–			–		15		
	t_{9-}	9	–	–				–	–			–		9		

*Inputs 4, 7, 10, and 13 will behave similarly for ac and I_{inH} values.
Inputs 5, 6, 11, and 12 will behave similarly for ac and I_{inH} values.

TRIPLE 2-3-2 INPUT
OR/NOR GATE

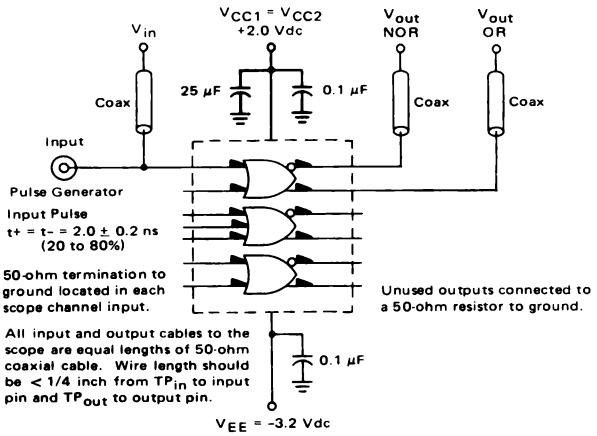
MC10105

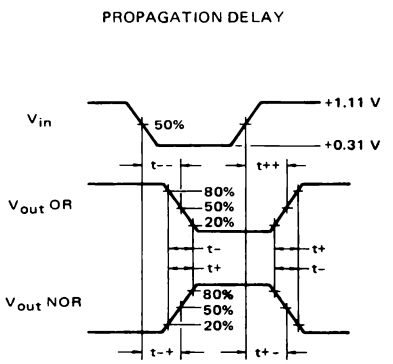


The MC10105 is a triple 2-3-2 input OR/NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time
= 3.5 ns typ (10%-90%)
= 2.0 ns typ (20%-80%)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

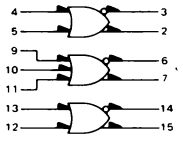


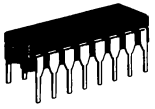


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





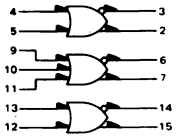
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10105L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	17	21	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	3	8	1,16
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
	t_{4+2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
Rise Time	t_{3+}	3	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	3	↓	↓
(20 to 80%)	t_{2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
Fall Time	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
(20 to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.



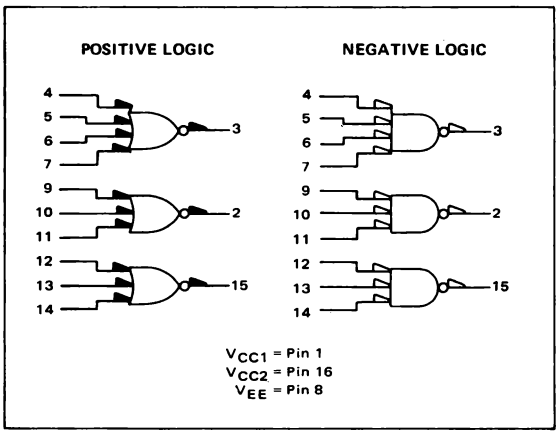
P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10105P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	17	21	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	–	–	1.0	2.0	2.9	–	–	ns	–	–	4	3	8	1,16
	t_{4-3+}	3	–	–	↓	↓	↓	–	–	↓	–	–	↓	3	↓	↓
	t_{4+2+}	2	–	–				–	–		–	–		2		
	t_{4-2-}	2	–	–				–	–		–	–		2		
Rise Time	t_{3+}	3	–	–	1.1		3.3	–	–		–	–		3		
(20 to 80%)	t_{2+}	2	–	–				–	–		–	–		2		
Fall Time	t_{3-}	3	–	–				–	–		–	–		3		
(20 to 80%)	t_{2-}	2	–	–	↓	↓	↓	–	–	↓	–	–	↓	2	↓	↓

TRIPLE 4-3-3 INPUT
NOR GATE

MC10106



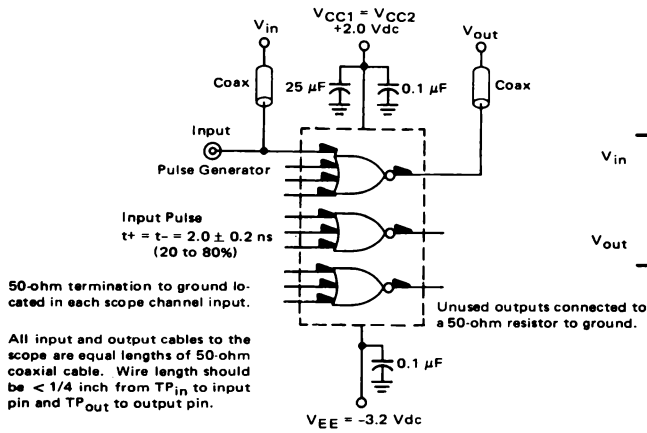
The MC10106 is a triple 4-3-3 input NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

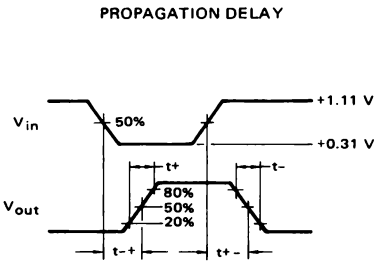
P_D = 30 mW typ/gate (No Load)

t_{pd} = 2.0 ns typ

Output Rise and Fall Time
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

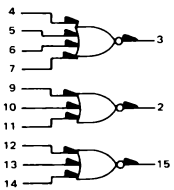


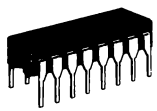


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





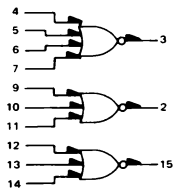
L SUFFIX
CERAMIC PACKAGE
CASE 620

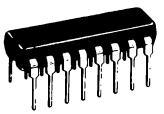
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10106L Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	17	21	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	9	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	3	8	1,16
	t_{4-3+}	↓	1.0	3.1	1.0	↓	2.9	1.0	3.3	↓	–	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_{3+}		1.1	3.6	1.1		3.3	1.1	3.7		–	–				
Fall Time (20 to 80%)	t_{3-}	↓	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	↓	↓	↓

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.



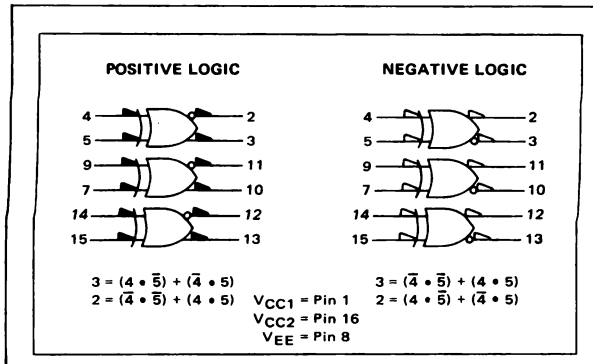


P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10106P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	17	21	–	–	mAdc				–	8	1,16
Input Current	$I_{in}H$	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	9	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	–	–	1.0	2.0	2.9	–	–	ns			4	3	8	1,16
	t_{4-3+}	↓	–	–	1.0	↓	2.9	–	–	↓			↓	↓	↓	↓
Rise Time (20 to 80%)	t_{3+}		–	–	1.1		3.3	–	–							
Fall Time (20 to 80%)	t_{3-}		–	–	1.1		3.3	–	–							

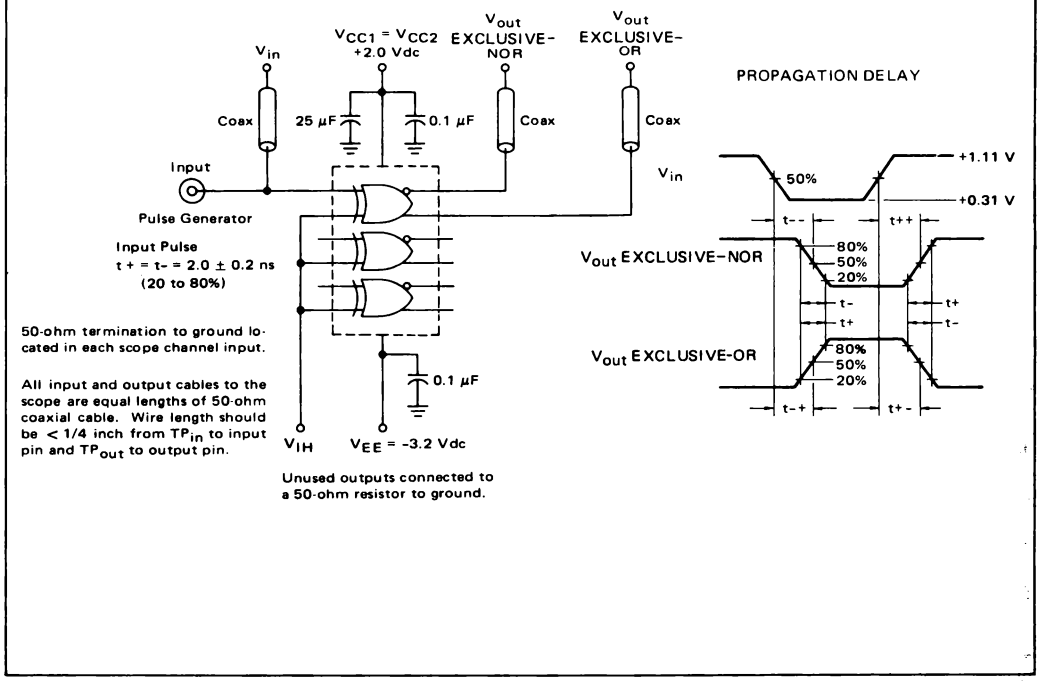
MC10107



This three gate array is designed to provide the positive logic Exclusive OR and Exclusive NOR functions in high speed applications. Input pulldown resistors eliminate the need to *tie unused inputs to* V_{EE}.

P_D = 40 mW typ/gate (No Load)
t_{pd} = 2.5 ns typ
Output Rise and Fall Times
= 2.5 ns typ (20% to 80%)
= 3.5 ns typ (10% to 90%)

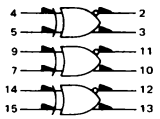
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

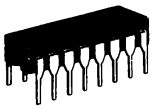


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

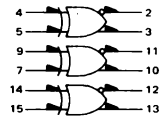
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

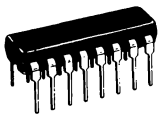
Characteristic	Symbol	Pin Under Test	MC10107L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–		28	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4,9,14	–	–	–		265	–	–	µAdc	*	–	–	–	8	1,16
		5,7,15	–	–	–		220	–	–	µAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5		–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	4,5	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		–	–	–	–		
		3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		4	–	–	–		
		3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		5	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		5	–	–	–		
		3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		4,5	–	–	–		
		3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		–	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980		–	-0.910	–	Vdc	5	–	4	–	8	1,16
		2	-1.080	–	-0.980		–	-0.910	–		–	–	–	4		
		3	-1.080	–	-0.980		–	-0.910	–		–	–	4	–		
		3	-1.080	–	-0.980		–	-0.910	–		–	–	5	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–		-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–		-1.630	–	-1.595		–	–	5	–		
		3	–	-1.655	–		-1.630	–	-1.595		5	–	4	–		
		3	–	-1.655	–		-1.630	–	-1.595		–	–	–	4		
Switching Times (50 Ω Load)					Min	Typ	Max			Unit	+1.1 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t++	Inputs	1.1	3.8	1.1	2.0	3.7	1.1	4.0	ns	5,7,15	–	Input	Corresponding	8	1,16
	t+-	4, 9 or 14										–	4, 9, or	Ex-OR/Ex-NOR		
	t-+	to either										–	14	Outputs		
	t--	Output										–				
	t++	Inputs				2.8					4,9,14	–	Input	Corresponding		
	t+-	5,7, or 15										–	5, 7, or	Ex-OR/Ex-NOR		
	t-+	to either										–	15	Outputs		
	t--	Output										–				
Rise Time (20 to 80%)	t+	**	1.1	3.5		2.5	3.5		3.8		4,9,14	–	Any Input	Corresponding		
Fall Time (20 to 80%)	t-	**	1.1	3.5		2.5	3.5		3.8		4,9,14	–	Any Input	Ex-OR/Ex NOR Outputs		

*Individually test each input applying V_{IH} or V_{IL} to input under test.
**Any Output

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





P SUFFIX
CERAMIC PACKAGE
CASE 648

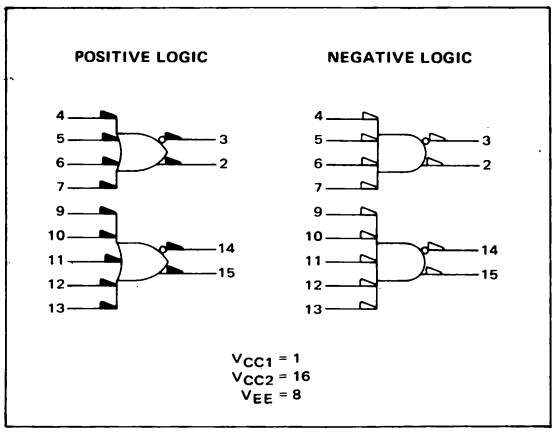
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10107P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–		28	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4,9,14	–	–	–		265	–	–	µAdc	*	–	–	–	8	1,16
		5,7,15	–	–	–		220	–	–	µAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5		–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	4,5	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		–	–	–	–		
		3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		4	–	–	–		
		3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		5	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		5	–	–	–		
		3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		4,5	–	–	–		
		3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		–	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980		–	-0.910	–	Vdc	5	–	4	–	8	1,16
		2	-1.080	–	-0.980		–	-0.910	–		–	–	–	4		
		3	-1.080	–	-0.980		–	-0.910	–		–	–	4	–		
		3	-1.080	–	-0.980		–	-0.910	–		–	–	5	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–		-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–		-1.630	–	-1.595		–	–	5	–		
		3	–	-1.655	–		-1.630	–	-1.595		5	–	4	–		
		3	–	-1.655	–		-1.630	–	-1.595		–	–	–	4		
Switching Times (50 Ω Load)					Min	Typ	Max			Unit	+1.1 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t++	Inputs	–	–	1.1	2.0	3.7	–	–	ns	5,7,15	–	Input	Corresponding	8	1,16
	t+-	4, 9 or 14	–	–				–	–			–	4, 9, or	Ex-OR/Ex-NOR		
	t-+	to either	–	–				–	–			–	14	Outputs		
	t--	Output	–	–				–	–			–				
	t++	Inputs	–	–		2.8		–	–		4,9,14	–	Input	Corresponding		
	t+-	5,7, or 15	–	–				–	–			–	5, 7, or	Ex-OR/Ex-NOR		
	t-+	to either	–	–				–	–			–	15	Outputs		
	t--	Output	–	–				–	–			–				
Rise Time (20 to 80%)	t+	**	–	–		2.5	3.5	–	–		4,9,14	–	Any Input	Corresponding Ex-OR/Ex NOR Outputs		
Fall Time (20 to 80%)	t-	**	–	–		2.5	3.5	–	–		4,9,14	–	Any Input			

*Individually test each input applying V_{IH} or V_{IL} to input under test.
**Any Output

DUAL 4-5-INPUT
"OR/NOR" GATE

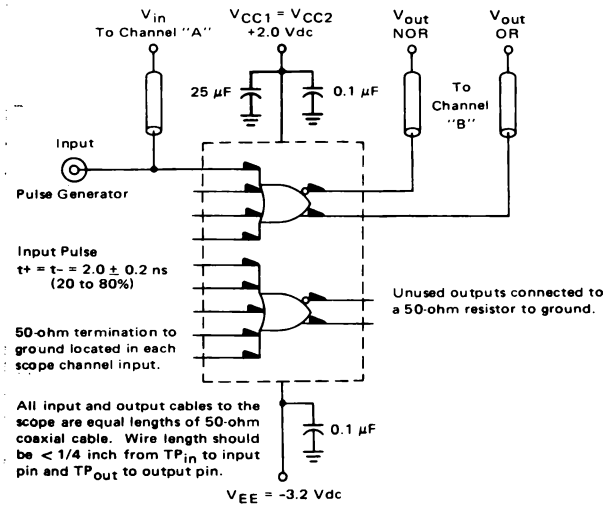
MC10109

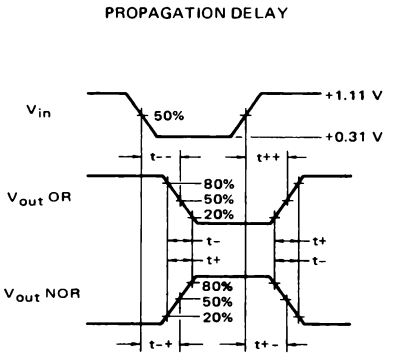


The MC10109 is a dual 4-5 input OR-NOR gate which is pin compatible with the MECL III MC1660L dual OR-NOR gate. All inputs are terminated by a 50 k ohm resistor to V_{EE} eliminating the need to tie unused inputs low.

t_{pd} = 2.0 ns typ
P_D = 30 mW typ/gate (No Load)
Output Rise and Fall Times
(10% to 90%) 3.5 ns
(20% to 80%) 2.0 ns

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

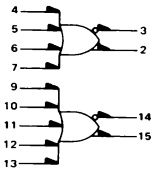


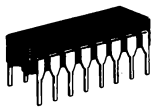


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





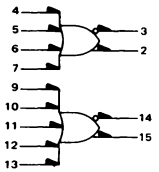
L SUFFIX
CERAMIC PACKAGE
CASE 620

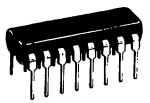
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10109L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	11	14	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	8	1,16
	t_{4-2-}	2									–	–		2		
	t_{4+3-}	3									–	–		3		
	t_{4-3+}	3									–	–		3		
Rise Time (20 to 80%)	t_{2+}	2	1.1	3.6	1.1		3.3	1.1	3.7		–	–		2		
	t_{3+}	3									–	–		3		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





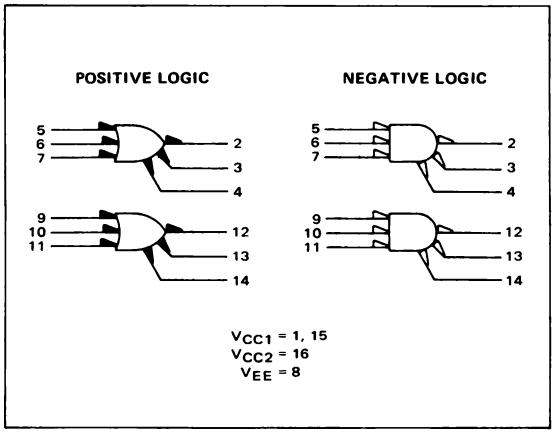
P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10109P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	11	14	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	–	1.0	2.0	2.9	–	–	ns	–	–	4	2	8	1,16
	t_{4-2-}	2	–	–	↓	↓	↓	–	–	↓	–	–	↓	2	↓	↓
	t_{4+3-}	3	–	–	↓	↓	↓	–	–	↓	–	–	↓	3	↓	↓
	t_{4-3+}	3	–	–	↓	↓	↓	–	–	↓	–	–	↓	3	↓	↓
Rise Time (20 to 80%)	t_{2+}	2	–	–	1.1	↓	3.3	–	–	↓	–	–	↓	2	↓	↓
	t_{3+}	3	–	–	↓	↓	↓	–	–	↓	–	–	↓	3	↓	↓
Fall Time (20 to 80%)	t_{2-}	2	–	–	↓	↓	↓	–	–	↓	–	–	↓	2	↓	↓
	t_{3-}	3	–	–	↓	↓	↓	–	–	↓	–	–	↓	3	↓	↓

DUAL 3-INPUT 3-OUTPUT
"OR" GATE

MC10110



The MC10110 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire-"OR"-ing of several levels of gating for minimization of gate and package count.

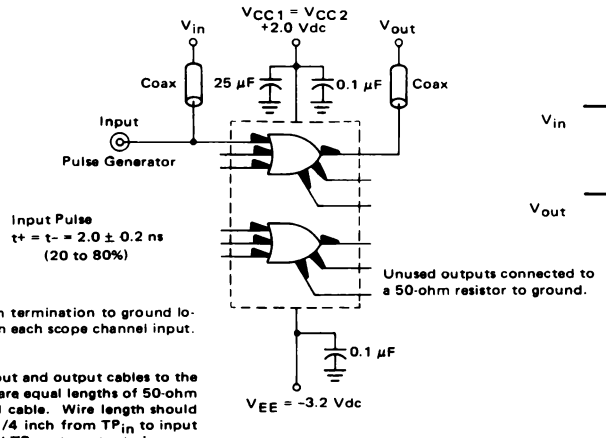
The ability to control three parallel lines from a single point makes the MC10110 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.

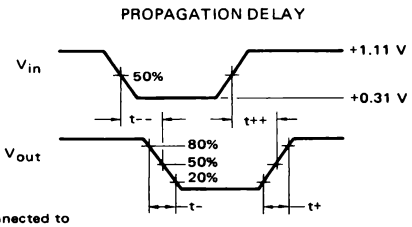
P_D = 80 mW typ/gate (No Load)

t_{pd} = 2.4 ns typ (All Outputs Loaded)

Output Rise and Fall Time: (All Outputs Loaded)
= 2.2 ns typ (20% to 80%)
= 4.0 ns typ (10% to 90%)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

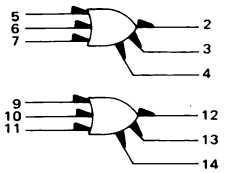


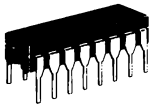


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

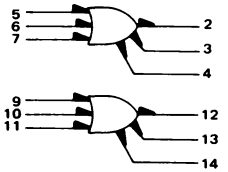
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10110L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	30	38	–	–	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	–	–	–	425	–	–	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	–	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	7	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2+}	2	1.4	3.5	1.4	2.4	3.5	1.5	3.8	ns	–	–	5	2	8	1,15,16
	t_{5-2-}	2									–	–		2		
	t_{5+3+}	3									–	–		3		
	t_{5-3-}	3									–	–		3		
	t_{5+4+}	4									–	–		4		
	t_{5-4-}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2	1.0		1.1	2.2		1.2			–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4									–	–		4		

*Individually test each input using the pin connections shown.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.



P SUFFIX
PLASTIC PACKAGE
CASE 648

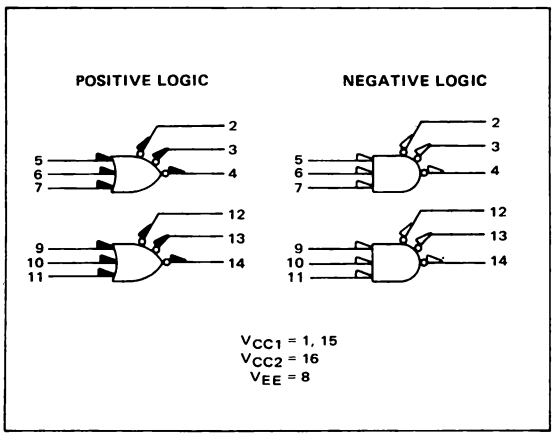
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10110P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	38	–	–	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	–	–	–	425	–	–	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	–	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	7	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2+}	2	–	–	1.4	2.4	3.5	–	–	ns	–	–	5	2	8	1,15,16
	t_{5-2-}	2	–	–				–	–		–	–		2		
	t_{5+3+}	3	–	–				–	–		–	–		3		
	t_{5-3-}	3	–	–				–	–		–	–		3		
	t_{5+4+}	4	–	–				–	–		–	–		4		
	t_{5-4-}	4	–	–				–	–		–	–		4		
Rise Time (20 to 80%)	t_{2+}	2	–	–	1.1	2.2		–	–		–	–		2		
	t_{3+}	3	–	–				–	–		–	–		3		
	t_{4+}	4	–	–				–	–		–	–		4		
Fall Time (20 to 80%)	t_{2-}	2	–	–				–	–		–	–		2		
	t_{3-}	3	–	–				–	–		–	–		3		
	t_{4-}	4	–	–				–	–		–	–		4		

*Individually test each input using the pin connections shown.

DUAL 3-INPUT 3-OUTPUT
"NOR" GATE

MC10111

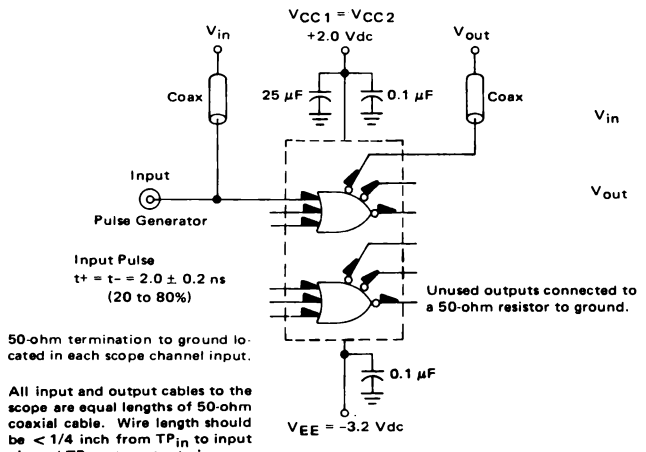


The MC10111 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire-"OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10111 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.

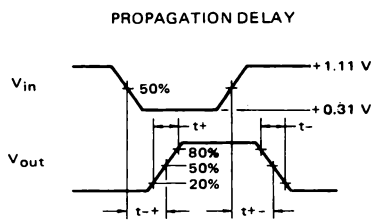
P_D = 80 mW typ/gate (No Load)
t_{pd} = 2.4 ns typ (All Outputs Loaded)
Output Rise and Fall Time: (All Outputs Loaded)
= 2.2 ns typ (20% to 80%)
= 4.0 ns typ (10% to 90%)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

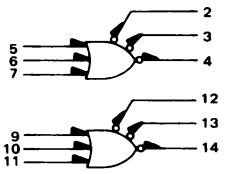
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

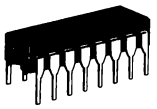


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

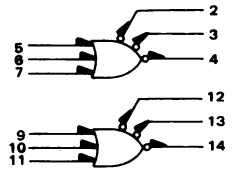
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

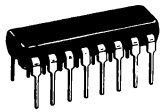
Characteristic	Symbol	Pin Under Test	MC10111L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+85°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	38	–	–	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	–	–	–	425	–	–	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc		–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	6		–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	6	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	7	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
		3	–	-1.655	–	–	-1.630		-1.595	Vdc	–	–	6	–	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	–	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2-}	2	1.4	3.5	1.4	2.4	3.5	1.5	3.8	ns	–	–	5	2	8	1,15,16
	t_{5-2+}	2									–	–		2		
	t_{5+3-}	3									–	–		3		
	t_{5-3+}	3									–	–		3		
	t_{5+4-}	4									–	–		4		
	t_{5-4+}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2	1.0		1.1	2.2	3.5	1.2	3.8		–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4									–	–		4		

*Individually test each input using the pin connections shown.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

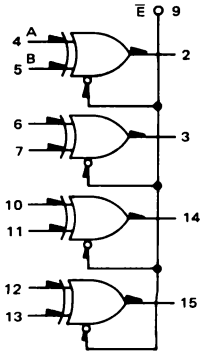
Characteristic	Symbol	Pin Under Test	MC10111P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	-	-	-	-	38	-	-	mAdc	-	-	-	-	8	1,15,16
Input Current	I_{inH}	5,6,7	-	-	-	-	425	-	-	µAdc	*	-	-	-	8	1,15,16
	I_{inL}	5,6,7	-	-	0.5	-	-	-	-	µAdc	-	*	-	-	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	-	-	-	-	8	1,15,16
		3	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	-	-	-	-	8	1,15,16
		4	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	-	-	-	-	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	5	-	-	-	8	1,15,16
		3	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	6	-	-	-	8	1,15,16
		4	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	7	-	-	-	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	-	-0.980	-	-	-0.910	-	Vdc	-	-	-	5	8	1,15,16
		3	-1.080	-	-0.980	-	-	-0.910	-	Vdc	-	-	-	6	8	1,15,16
		4	-1.080	-	-0.980	-	-	-0.910	-	Vdc	-	-	-	7	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	-	5	-	8	1,15,16
		3	-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	-	6	-	8	1,15,16
		4	-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	-	7	-	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2-}	-	-	-	-	1.4	2.4	3.5	-	-	ns	-	-	5	2	8	1,15,16
	t_{5-2+}	-	-	-	-	↓	↓	↓	-	-	↓	-	-	↓	2	↓	↓
	t_{5+3-}	-	-	-	-	↓	↓	↓	-	-	↓	-	-	↓	3	↓	↓
	t_{5-3+}	-	-	-	-	↓	↓	↓	-	-	↓	-	-	↓	3	↓	↓
	t_{5+4-}	-	-	-	-	↓	↓	↓	-	-	↓	-	-	↓	4	↓	↓
	t_{5-4+}	-	-	-	-	↓	↓	↓	-	-	↓	-	-	↓	4	↓	↓
Rise Time (20 to 80%)	t_{2+}	-	-	-	-	1.1	2.2	↓	-	-	↓	-	-	↓	2	↓	↓
	t_{3+}	-	-	-	-	↓	↓	↓	-	-	↓	-	-	↓	3	↓	↓
	t_{4+}	-	-	-	-	↓	↓	↓	-	-	↓	-	-	↓	4	↓	↓
Fall Time (20 to 80%)	t_{2-}	-	-	-	-	↓	↓	↓	-	-	↓	-	-	↓	2	↓	↓
	t_{3-}	-	-	-	-	↓	↓	↓	-	-	↓	-	-	↓	3	↓	↓
	t_{4-}	-	-	-	-	↓	↓	↓	-	-	↓	-	-	↓	4	↓	↓

*Individually test each input using the pin connections shown.

MC10113

Advance Information

POSITIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

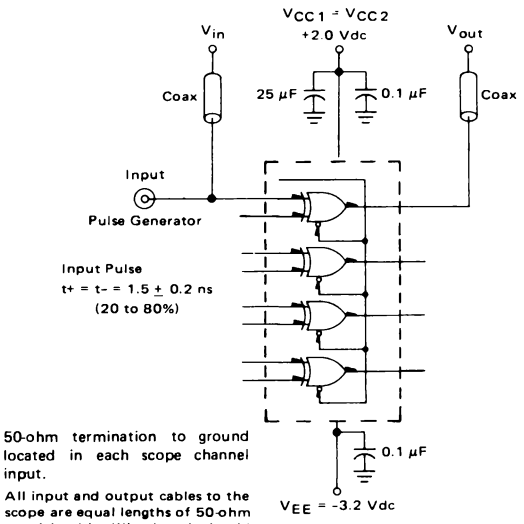
A	B	Ē	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
ϕ	ϕ	H	L

ϕ = Don't Care

The MC10113 is a quad Exclusive OR gate, with an enable common to all four gates. All four outputs may be wire-ORed together to perform a 4-bit comparison function (A = B). The enable is active low. Input pulldown resistors included in the circuit make it unnecessary to tie down unused inputs. Open emitter outputs permit direct connection of outputs to busses.

P_D = 175 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
Output Rise and Fall Times
= 2.0 ns typ (20% to 80%)

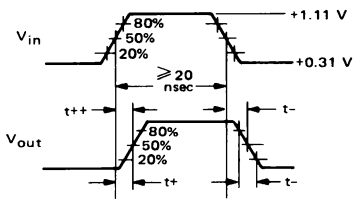
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

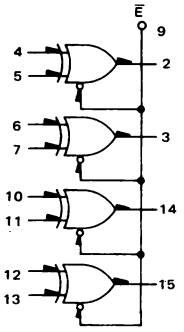
Unused outputs connected to a 50-ohm resistor to ground.

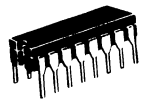


This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





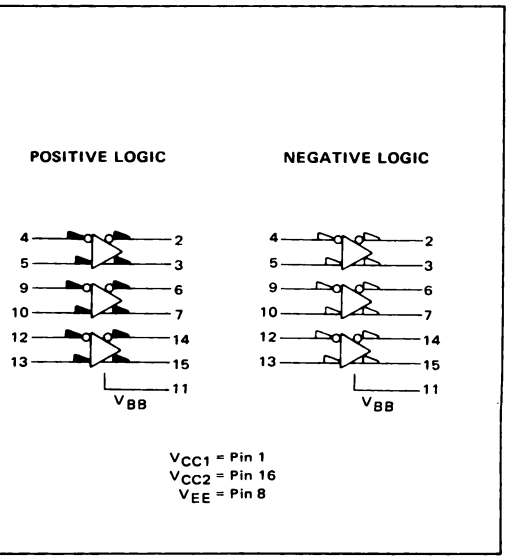
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10113L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	42	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4,7,10,13	–	–	–	265	–	–	μAdc	*	–	–	–	8	1,16
		5,6,11,12	–	–	–	220	–	–	μAdc	*	–	–	–	8	1,16
		9	–	–	–	545	–	–	μAdc	9	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	–	0.5	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		7	–	–	–		
		14	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		11	–	–	–		
		15	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		13	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	–	4	–	–	8	1,16
		3	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	7	–	–		
		14	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	11	–	–		
		15	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	13	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	-0.910	–		–	–	6	–		
		14	-1.080	–	-0.980	–	-0.910	–		–	–	10	–		
		15	-1.080	–	-0.980	–	-0.910	–		–	–	12	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		3	–	-1.655	–	-1.630	–	-1.595		–	–	–	7		
		14	–	-1.655	–	-1.630	–	-1.595		–	–	–	11		
		15	–	-1.655	–	-1.630	–	-1.595		–	–	–	13		
Switching Times (50 Ω Load)					Min	Typ	Max		Unit	+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	–	–	3.0	–	–	–	ns	–	–	4	2	8	1,16
	t_{4-2-}	2	–	–	–	3.0	–	–	–		–	–	4			
	t_{9+2-}	2	–	–	–	3.4	–	–	–		4	–	9			
	t_{9-2+}	2	–	–	–	3.4	–	–	–		4	–	9			
Rise Time (20 to 80%)	t_{2+}	2	–	–	–	2.0	–	–	–		–	–	4			
Fall Time (20 to 80%)	t_{2-}	2	–	–	–	2.0	–	–	–		–	–	4			

*Individually test each input applying V_{IH} or V_{IL} to input under test.

MC10114



The MC10114 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

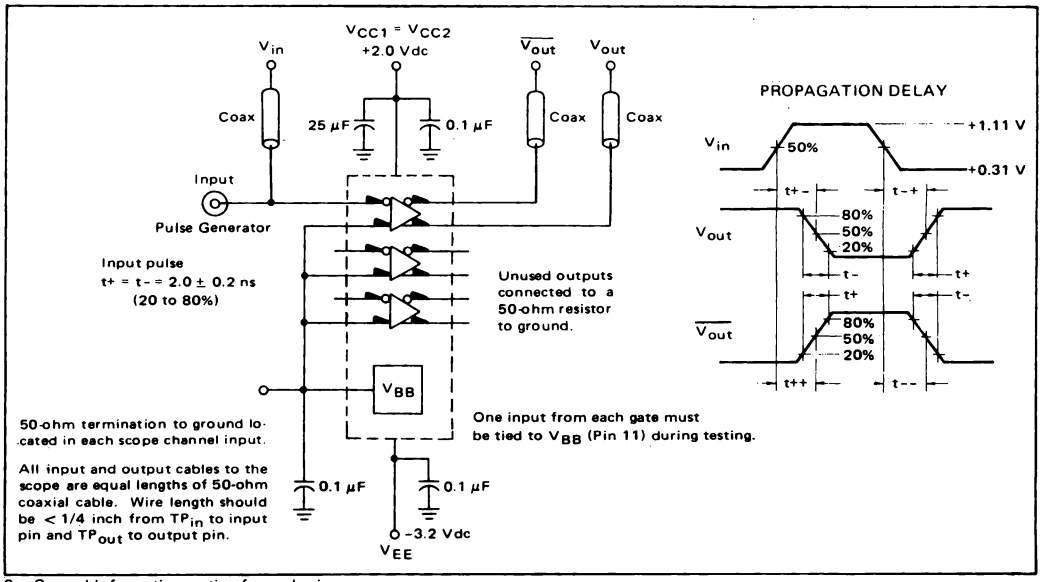
Another feature of the MC10114 is that the OR outputs (pins 3, 7, 15) go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 50 ohm transmission lines.

This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumentation systems. The MC10114 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A V_{BB} reference is provided which is useful in making the MC10114 a Schmitt trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary.

t_{pd} = 2.4 ns typ (Single Ended Input)
t_{pd} = 2.0 ns typ (Differential Input)
P_D = 145 mW typ/pkg

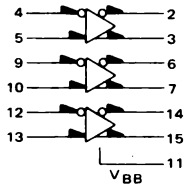
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

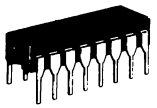


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

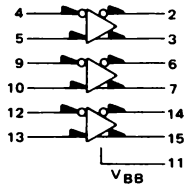
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From	+0.110	-0.890	-1.890	-2.890	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	+0.190	-0.850	-1.810	-2.850	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	+0.300	-0.825	-1.700	-2.825	-5.2

Characteristic	Symbol	Pin Under Test	MC10114L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	35	–	–	mAdc	–	4,9,12	–	–	5,10,13	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	45	–	–	μAdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
	I_{CBO}	4	–	–	–	–	1.0	–	–	μAdc	–	9,12	–	–	5,10,13	–	–	–	–	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–		5,10,13	–	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4		–	5,10,13	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	–	–	–	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	–	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	–	4	5,10,13	–	–	–	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	4	–	5,10,13	–	–	–	–	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	–	–	–	–	8	1,16
Common Mode Rejection Test	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	4	5	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	–	–	5	4	8	1,16
	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	–	–	5	4	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	4	5	–	–	8	1,16
Switching Times (50-ohm Load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out						-3.2 V	+2.0 V
Propagation Delay**	t_{4+2+}	2	1.0	4.4	1.0	2.4	4.0	0.9	4.3	ns	–	–	4	2	5,10,13	–	–	–	–	8	1,16
	t_{4-2-}	2									–	–		2		–	–	–	–		
	t_{4+3-}	3									–	–		3		–	–	–	–		
	t_{4-3+}	3									–	–		3		–	–	–	–		
Rise Time (20% to 80%)	t_{2+}	2	1.5	3.8	1.5	2.1	3.5	1.5	3.7		–	–		2		–	–	–	–		
	t_{3+}	3									–	–		3		–	–	–	–		
Fall Time (20% to 80%)	t_{2-}	2									–	–		2		–	–	–	–		
	t_{3-}	3									–	–		3		–	–	–	–		

*V_{IHH} = Input logic "1" level shifted positive one volt for common mode rejection tests.
V_{ILH} = Input logic "0" level shifted positive one volt for common mode rejection tests.
V_{IHL} = Input logic "1" level shifted negative one volt for common mode rejection tests.
V_{ILL} = Input logic "0" level shifted negative one volt for common mode rejection tests.
**Delay is 2.0 ns with differential input.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.



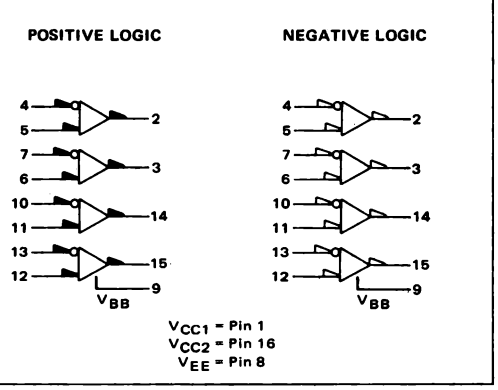
P SUFFIX
PLASTIC PACKAGE
CASE 648

● Test Temperature	TEST VOLTAGE VALUES (Volts)									
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From	+0.110	-0.890	-1.890	-2.890	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	+0.190	-0.850	-1.810	-2.850	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	+0.300	-0.825	-1.700	-2.825	-5.2

Characteristic	Symbol	Pin Under Test	MC10114P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	35	–	–	mAdc	–	4,9,12	–	–	5,10,13	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	45	–	–	μAdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
	I_{CBO}	4	–	–	–	–	1.0	–	–	μAdc	–	9,12	–	–	5,10,13	–	–	–	–	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4	–	–	5,10,13	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	–	–	–	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	–	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	–	4	5,10,13	–	–	–	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	4	–	5,10,13	–	–	–	–	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	–	–	–	–	8	1,16
Common Mode Rejection Test	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	4	5	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	–	–	5	4	8	1,16
	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	–	–	5	4	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	4	5	–	–	8	1,16
Switching Times (50-ohm Load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out						-3.2 V	+2.0 V
Propagation Delay**	t_{4+2+}	2	–	–	1.0	2.4	4.0	–	–	ns	–	–	4	2	5,10,13	–	–	–	–	8	1,16
	t_{4-2-}	2	–	–	↓	↓	↓	–	–	↓	–	–	↓	2	↓	–	–	–	–	↓	↓
	t_{4+3-}	3	–	–				–	–		–	–		3		–	–	–	–		
	t_{4-3+}	3	–	–				–	–		–	–		3		–	–	–	–		
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.5	2.1	3.5	–	–		–	–		2		–	–	–	–		
	t_{3+}	3	–	–				–	–		–	–		3		–	–	–	–		
Fall Time (20% to 80%)	t_{2-}	2	–	–				–	–		–	–		2		–	–	–	–		
	t_{3-}	3	–	–	↓	↓	↓	–	–	↓	–	–	↓	3	↓	–	–	–	–	↓	↓

*V_{IHH} = Input logic "1" level shifted positive one volt for common mode rejection tests.
V_{ILH} = Input logic "0" level shifted positive one volt for common mode rejection tests.
V_{IHL} = Input logic "1" level shifted negative one volt for common mode rejection tests.
V_{ILL} = Input logic "0" level shifted negative one volt for common mode rejection tests.
**Delay is 2.0 ns with differential input.

MC10115

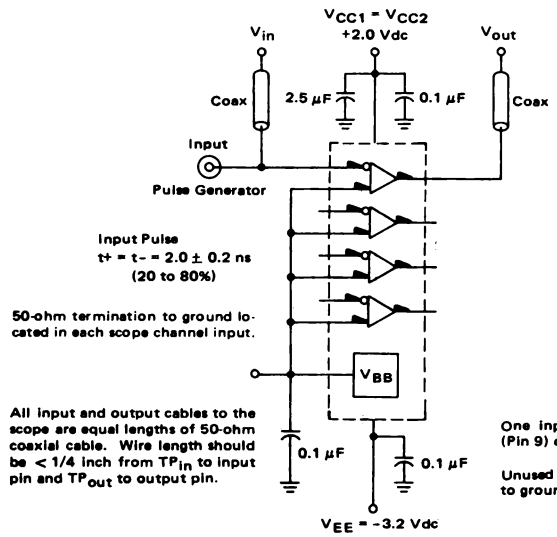


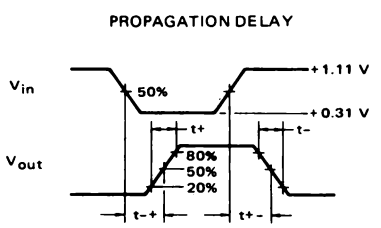
The MC10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

t_{pd} = 2.0 ns typ
P_D = 110 mW typ/pkg (No Load)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C





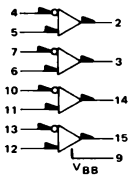
One input from each gate must be tied to V_{BB} (Pin 9) during testing.

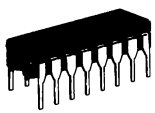
Unused outputs connected to a 50-ohm resistor to ground.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





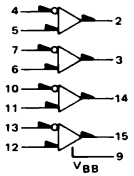
L SUFFIX
CERAMIC PACKAGE
CASE 620

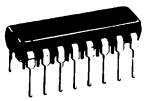
@ Test Temperature	TEST VOLTAGE VALUES					
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From Pin 9	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475		-5.2
+85°C	-0.700	-1.825	-1.035	-1.440		-5.2

Characteristic	Symbol	Pin Under Test	MC10115L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	26	–	–	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	$I_{in\ H}$	4	–	–	–	95	–	–	μAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
	I_{CBO}	4	–	–	–	1.0	–	–	μAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	1.420	1.280	-1.350	-1.230	1.295	-1.150	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50 Ω Load)										Pulse In		Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4-2+}	2	1.0	3.1	1.0	2.9	1.0	3.3	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	1.0	3.1	1.0	2.9	1.0	3.3								
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1	3.3	1.1	3.7								
Fall Time (20% to 80%)	t_{2-}	2	1.1	3.6	1.1	3.3	1.1	3.7								

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





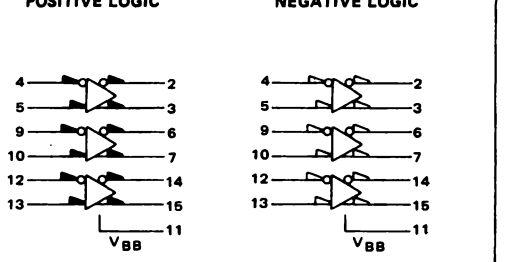
P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES					
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From Pin 9	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475		-5.2
+85°C	-0.700	-1.825	-1.035	-1.440		-5.2

Characteristic	Symbol	Pin Under Test	MC10115P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	26	–	–	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	$I_{in\,H}$	4	–	–	–	95	–	–	μAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
	I_{CBO}	4	–	–	–	1.0	–	–	μAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	1.420	1.280	-1.350	-1.230	1.295	-1.150	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50 Ω Load)										Pulse In		Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4-2+}	2	–	–	1.0	2.9	–	–	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	–	–	1.0	2.9	–	–		↓		↓		↓	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.1	3.3	–	–								
Fall Time (20% to 80%)	t_{2-}	2	–	–	1.1	3.3	–	–	↓							

TRIPLE LINE RECEIVER

MC10116



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

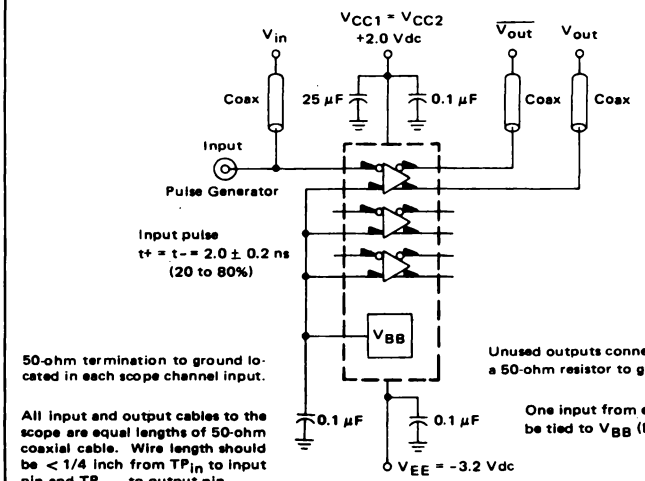
The MC10116 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

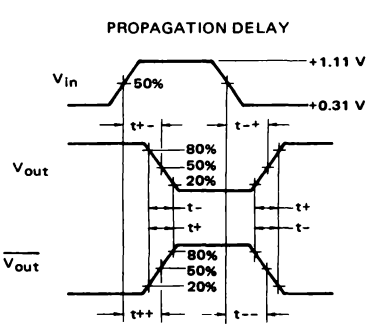
Active current sources provide the MC10116 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

t_{pd} = 2.0 ns typ
P_D = 85 mW typ/pkg (No Load)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

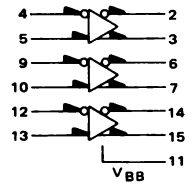


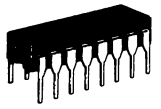


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





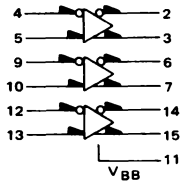
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2

Characteristic	Symbol	Pin Under Test	MC10116L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	17	21	–	–	mAdc	–	4,9,12	–	–	5,10,13	8	1,16
Input Current	I_{inH}	4	–	–	–	–	95	–	–	μAdc	4	9,12	–	–	5,10,13	8	1,16
	I_{CBO}	4	–	–	–	–	1.0	–	–	μAdc	–	9,12	–	–	5,10,13	8,4	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–	–	5,10,13	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4	–	–	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	–	4	5,10,13	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	4	–	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out		-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.1	1.0	2.0	2.9	1.1	3.3	ns	–	–	4	2	5,10,13	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓	↓
	t_{4+3-}	3									–	–		3			
	t_{4-3+}	3									–	–		3			
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1		3.3	1.1	3.7		–	–		2			
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓	↓
Fall Time (20% to 80%)	t_{2-}	2									–	–		2			
	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓	↓

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.



P SUFFIX
PLASTIC PACKAGE
CASE 648

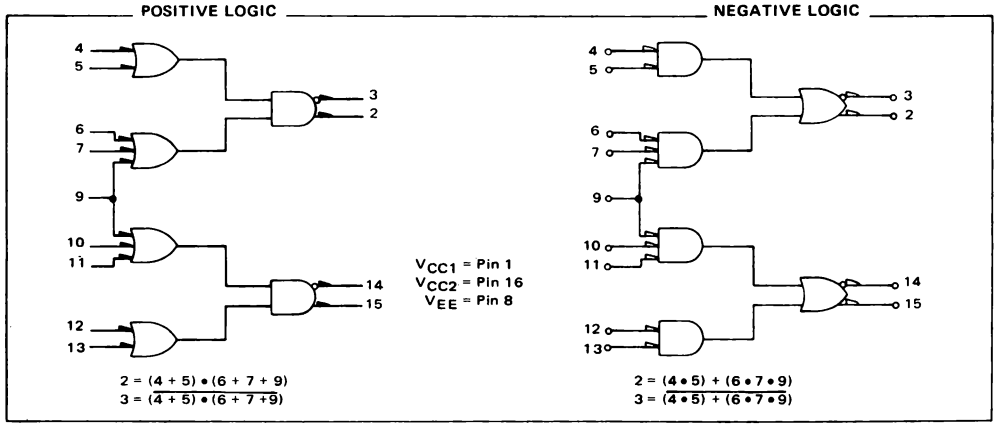
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2

Characteristic	Symbol	Pin Under Test	MC10116P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	—	—	—	17	21	—	—	mAdc	—	4,9,12	—	—	5,10,13	8	1,16
Input Current	I_{inH}	4	—	—	—	—	95	—	—	μAdc	4	9,12	—	—	5,10,13	8	1,16
	I_{CBO}	4	—	—	—	—	1.0	—	—	μAdc	—	9,12	—	—	5,10,13	8,4	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	—	-0.810	-0.890	-0.700	Vdc	4	9,12	—	—	5,10,13	8	1,16
		3	-1.060	-0.890	-0.960	—	-0.810	-0.890	-0.700	Vdc	9,12	4	—	—	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	—	-1.650	-1.825	-1.615	Vdc	9,12	4	—	—	5,10,13	8	1,16
		3	-1.890	-1.675	-1.850	—	-1.650	-1.825	-1.615	Vdc	4	9,12	—	—	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	—	-0.980	—	—	-0.910	—	Vdc	—	9,12	4	—	5,10,13	8	1,16
		3	-1.080	—	-0.980	—	—	-0.910	—	Vdc	9,12	—	—	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	—	-1.655	—	—	-1.630	—	-1.595	Vdc	—	9,12	—	4	5,10,13	8	1,16
		3	—	-1.655	—	—	-1.630	—	-1.595	Vdc	9,12	—	4	—	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	—	-1.230	-1.295	-1.150	Vdc	—	—	—	—	5,10,13	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out		-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	—	—	1.0	2.0	2.9	—	—	ns	—	—	4	2	5,10,13	8	1,16
	t_{4-2-}	2	—	—	↓	↓	↓	—	—	↓	—	—	↓	2	↓	↓	↓
	t_{4+3-}	3	—	—				—	—		—	—		3			
	t_{4-3+}	3	—	—				—	—		—	—		3			
Rise Time	t_{2+}	2	—	—	1.1		3.3	—	—		—	—		2			
(20% to 80%)	t_{3+}	3	—	—	↓		↓	—	—		—	—		3			
Fall Time	t_{2-}	2	—	—				—	—		—	—		2			
(20% to 80%)	t_{3-}	3	—	—	↓	↓	↓	—	—	↓	—	—	↓	3	↓	↓	↓

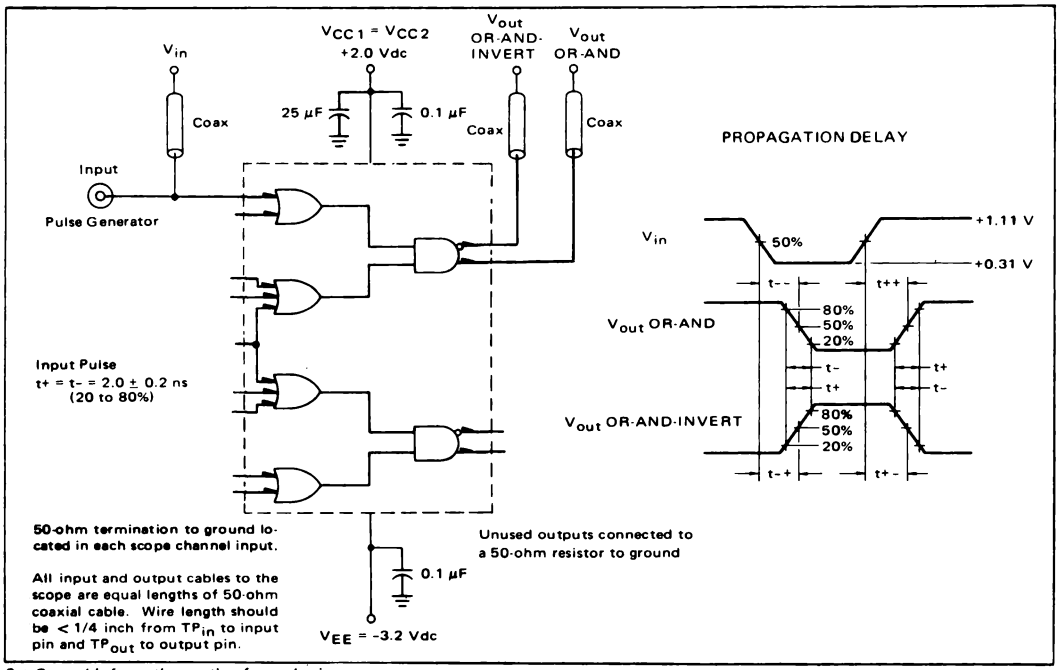
MC10117

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
Output Rise and Fall Times:
= 3.5 ns (10% to 90%)
= 2.2 ns (20% to 80%)

The MC10117 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.



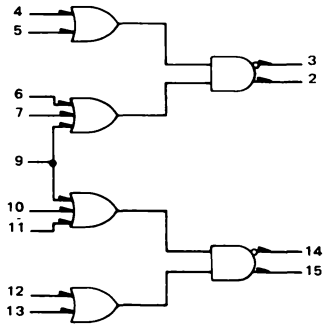
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

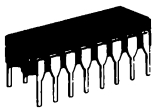


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





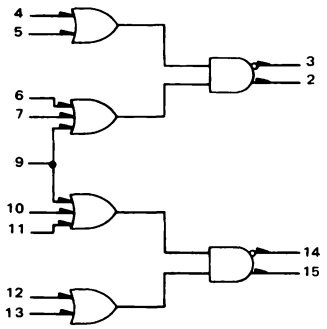
L SUFFIX
CERAMIC PACKAGE
CASE 620

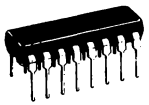
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10117L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	–	–	–	265	–	–	µAdc	4	–	–	–	8	1,16
		9	–	–	–	–	350	–	–	µAdc	9	–	–	–	8	1,16
	$I_{in\ L}$	4	–	–	0.5	–	–	–	–	µAdc	–	4	–	–	8	1,16
		9	–	–	0.5	–	–	–	–	µAdc	–	9	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,9	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	4	–	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	9	–	4	2	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓
	t_{4+3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
Rise Time (20 to 80%)	t_{2+}	2	0.9	4.1	1.1	2.2	4.0	1.1	4.6	↓	↓	–	↓	2	↓	↓
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
Fall Time (20 to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓
	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

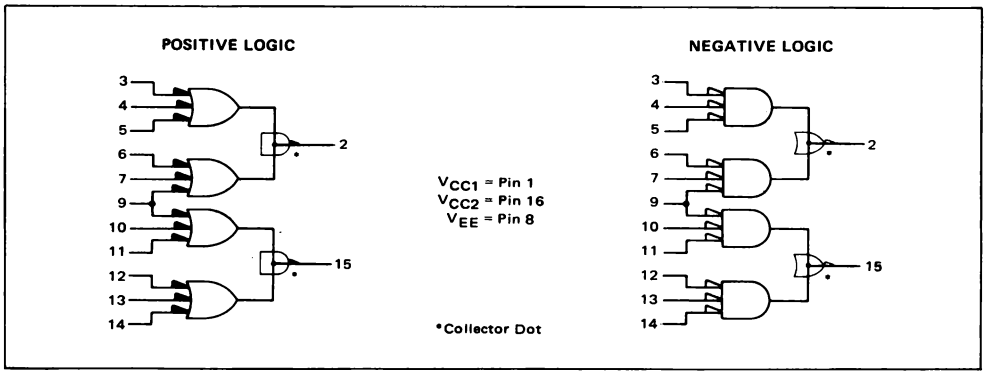
Characteristic	Symbol	Pin Under Test	MC10117P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
		9	–	–	–	–	350	–	–	μAdc	9	–	–	–	8	1,16
	$I_{in\ L}$	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
		9	–	–	0.5	–	–	–	–	μAdc	–	9	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,9	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	4	–	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	–	1.4	2.3	3.4	–	–	ns	9	–	4	2	8	1,16
	t_{4-2-}	2	–	–	↓	↓	↓	–	–	↓	↓	–	↓	2	↓	↓
	t_{4+3-}	3	–	–	↓	↓	↓	–	–	↓	↓	–	↓	3	↓	↓
	t_{4-3+}	3	–	–	↓	↓	↓	–	–	↓	↓	–	↓	3	↓	↓
Rise Time (20 to 80%)	t_{2+}	2	–	–	1.1	2.2	4.0	–	–	↓	↓	–	↓	2	↓	↓
	t_{3+}	3	–	–	↓	↓	↓	–	–	↓	↓	–	↓	3	↓	↓
Fall Time (20 to 80%)	t_{2-}	2	–	–	↓	↓	↓	–	–	↓	↓	–	↓	2	↓	↓
	t_{3-}	3	–	–	↓	↓	↓	–	–	↓	↓	–	↓	3	↓	↓

DUAL 2-WIDE 3-INPUT
"OR-AND" GATE

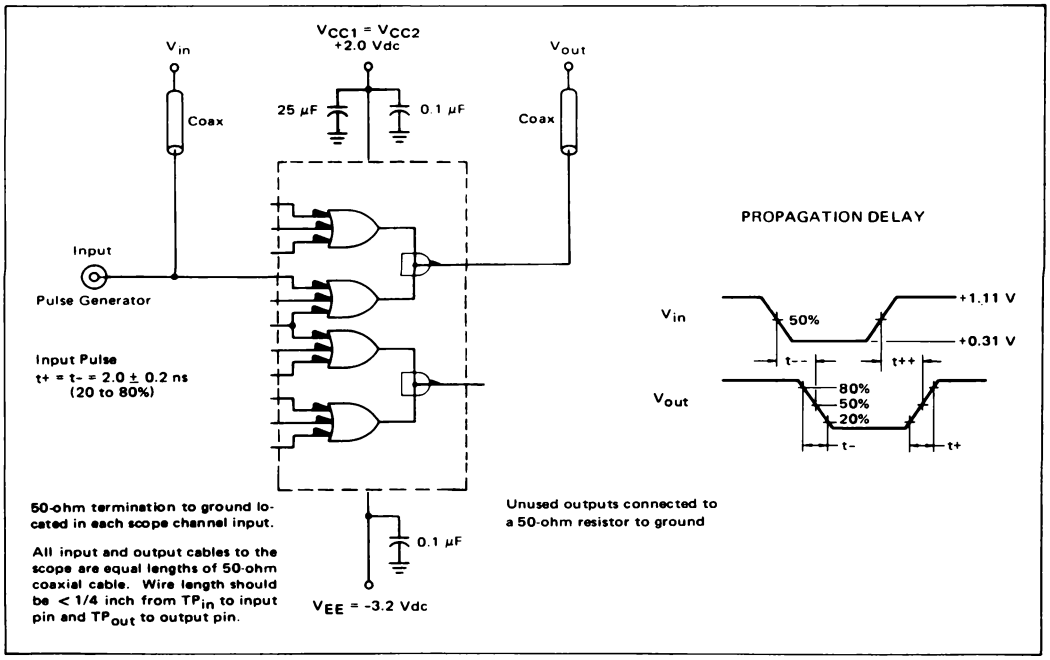
MC10118

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
Output Rise and Fall Times:
= 3.5 ns (10% to 90%)
= 2.5 ns (20% to 80%)

The MC10118 is a basic logic building block providing the OR-AND function, useful in data control and digital multiplexing applications.



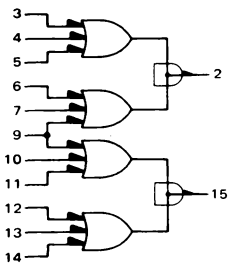
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

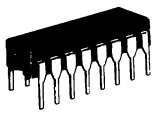


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





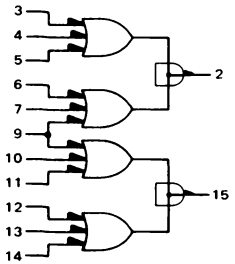
L SUFFIX
CERAMIC PACKAGE
CASE 620

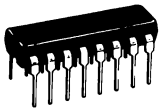
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10118L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–			8	1,16
Input Current	$I_{in\ H}$	6	–	–	–	–	265	–	–	μAdc	6	–	–	–	8	1,16
		7	–	–	–	–	265	–	–	↓	7	–	–	–	↓	↓
		9	–	–	–	–	370	–	–		9	–	–	–		
	$I_{in\ L}$	6	–	–	0.5	–	–	–	–	μAdc	–	6	–	–	8	1,16
		7	–	–	↓	–	–	–	–	↓	–	7	–	–	↓	↓
		9	–	–		–	–	–	–		–	9	–	–		
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-2.000	-1.675	-1.990	–	-1.650	-1.920	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	...	-0.910	–	Vdc	9	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	3	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{6+2+}	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	3	–	6	2	8	1,16
	t_{6-2-}	↓	1.4	3.9	1.4	2.3	3.4	1.4	3.8	↓	↓	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_+		0.8	4.1	1.5	2.5	4.0	1.5	4.6			–				
Fall Time (20 to 80%)	t_-		0.8	4.1	1.5	2.5	4.0	1.5	4.6			–				

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





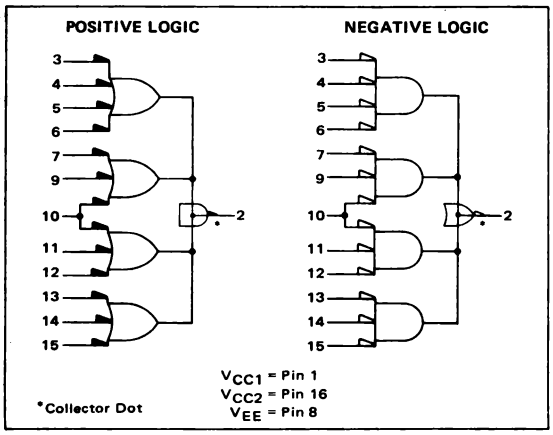
P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10118P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	6	–	–	–	–	265	–	–	μAdc	6	–	–	–	8	1,16
		7	–	–	–	–	265	–	–	↓	7	–	–	–	↓	↓
		9	–	–	–	–	370	–	–		9	–	–	–		
	$I_{in\ L}$	6	–	–	0.5	–	–	–	–	μAdc	–	6	–	–	8	1,16
		7	–	–	↓	–	–	–	–	↓	–	7	–	–	↓	↓
		9	–	–		–	–	–	–		–	9	–	–		
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-2.000	-1.675	-1.990	–	-1.650	-1.920	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	3	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{6+2+}	2	–	–	1.4	2.3	3.4	–	–	ns	3	–	6	2	8	1,16
	t_{6-2-}	↓	–	–	1.4	2.3	3.4	–	–	↓	↓	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_+		–	–	1.5	2.5	4.0	–	–			–				
Fall Time (20 to 80%)	t_-		–	–	1.5	2.5	4.0	–	–			–				

4-WIDE 4-3-3-3 INPUT
"OR-AND" GATE

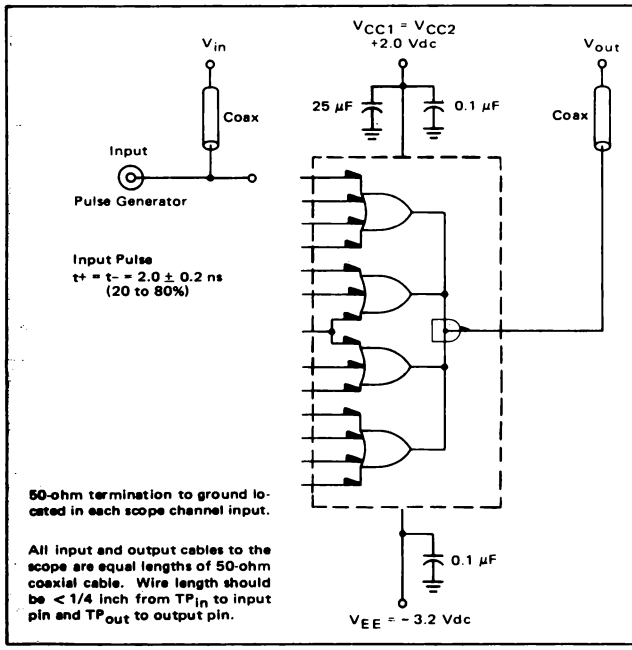
MC10119

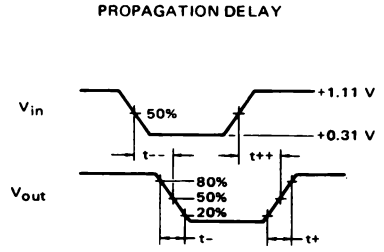


The MC10119 is a 4-Wide 4-3-3-3 Input OR-AND gate with one input from two gates common to pin 10. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.5 ns typ (20% - 80%)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

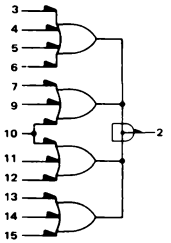


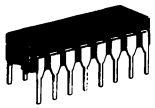


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





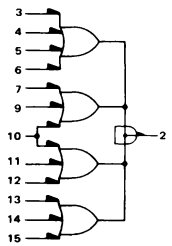
L SUFFIX
CERAMIC PACKAGE
CASE 620

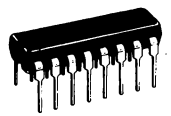
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10119L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	7	–	–	–	–	265	–	–	μAdc	7	–	–	–	8	1,16
		9	–	–	–	–	265	–	–	↓	9	–	–	–	↓	↓
		10	–	–	–	–	370	–	–		10	–	–	–		
	$I_{in\ L}$	7	–	–	0.5	–	–	–	–	μAdc	–	7	–	–	8	1,16
		9	–	–	↓	–	–	–	–	↓	–	9	–	–	↓	↓
		10	–	–		–	–	–	–		–	10	–	–		
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,10,15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-2.000	-1.675	-1.990	–	-1.650	-1.920	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	10,15	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	3	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	10,13	–	3	2	8	1,16
	t_{3-2-}	↓	1.4	3.9	1.4	2.3	3.4	1.4	3.8	↓	↓	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_+		0.8	4.1	1.5	2.5	4.0	1.5	4.6			–				
Fall Time (20 to 80%)	t_-		0.8	4.1	1.5	2.5	4.0	1.5	4.6			–				

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

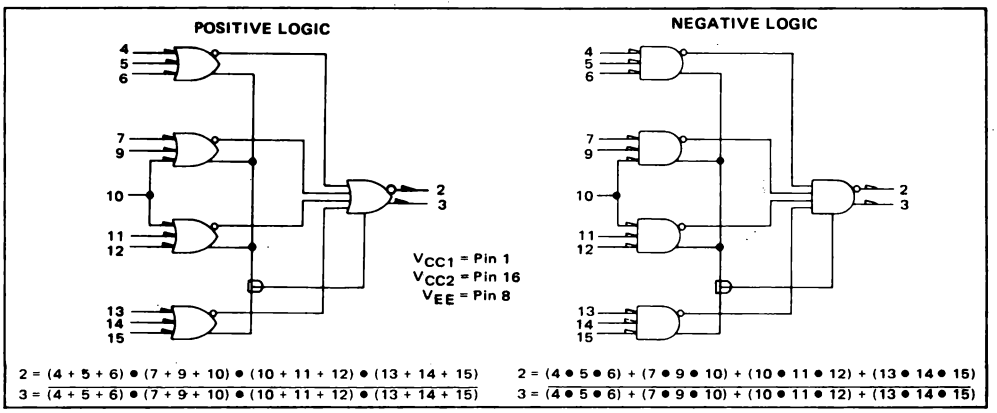
Characteristic	Symbol	Pin Under Test	MC10119P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	7	–	–	–	–	265	–	–	μAdc	7	–	–	–	8	1,16
		9	–	–	–	–	265	–	–		9	–	–	–	↓	↓
		10	–	–	–	–	370	–	–	↓	10	–	–	–		
	$I_{in\ L}$	7	–	–	0.5	–	–	–	–	μAdc	–	7	–	–	8	1,16
		9	–	–	↓	–	–	–	–		–	9	–	–	↓	↓
		10	–	–		–	–	–	–	↓	–	10	–	–		
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,10,15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-2.000	-1.675	-1.990	–	-1.650	-1.920	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	10,15	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	3	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–	–	1.4	2.3	3.4	–	–	ns	10,13	–	3	2	8	1,16
	t_{3-2-}		–	–	1.4	2.3	3.4	–	–			–				
Rise Time (20 to 80%)	t_+		–	–	1.5	2.5	4.0	–	–			–				
Fall Time (20 to 80%)	t_-	↓	–	–	1.5	2.5	4.0	–	–	↓	↓	–	↓	↓	↓	↓

4-WIDE
"OR-AND/OR-AND-INVERT"
GATE

MC10121

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
Output Rise and Fall Times:
= 3.5 ns (10% to 90%)
= 2.5 ns (20% to 80%)

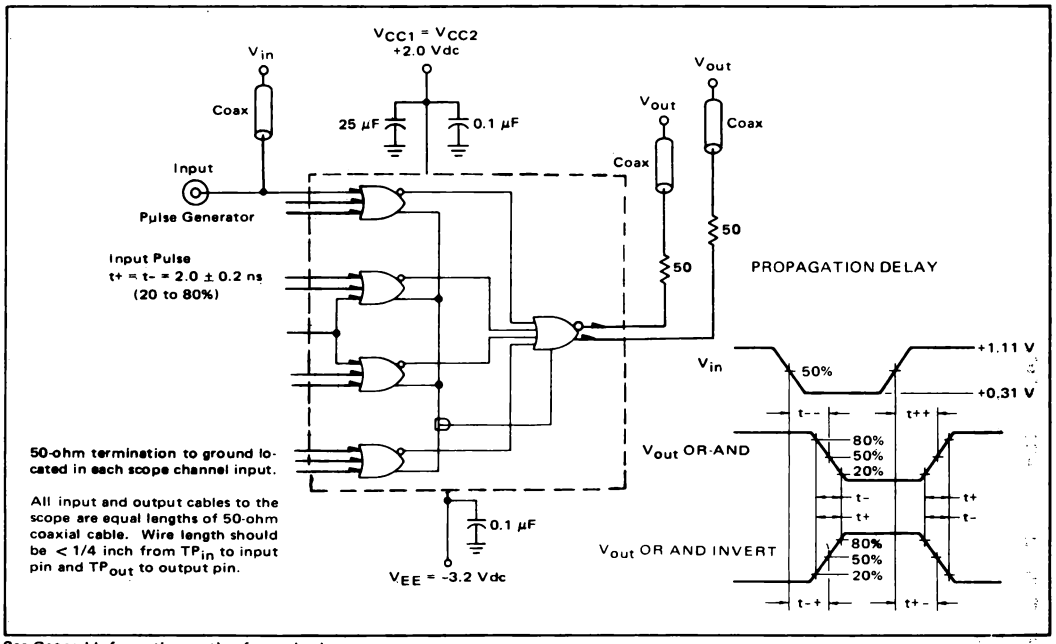
The MC10121 is a basic logic building block providing the simultaneous OR-AND/OR-AND-INVERT function, useful in data control and digital multiplexing applications.



2 = (4 + 5 + 6) • (7 + 9 + 10) • (10 + 11 + 12) • (13 + 14 + 15)
3 = $\overline{(4 + 5 + 6) • (7 + 9 + 10) • (10 + 11 + 12) • (13 + 14 + 15)}$

2 = (4 • 5 • 6) + (7 • 9 • 10) + (10 • 11 • 12) + (13 • 14 • 15)
3 = $\overline{(4 • 5 • 6) + (7 • 9 • 10) + (10 • 11 • 12) + (13 • 14 • 15)}$

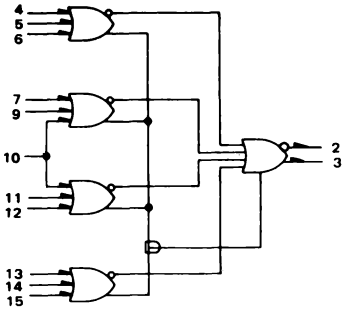
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

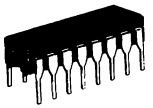


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





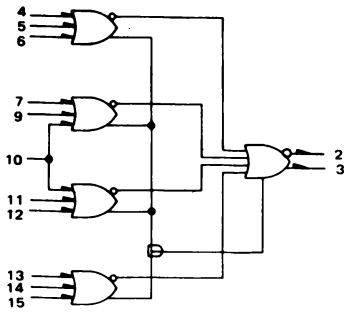
L SUFFIX
CERAMIC PACKAGE
CASE 620

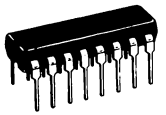
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10121L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	7	–	–	–	–	265	–	–	μAdc	7	–	–	–	8	1,16
		9	–	–	–	–	265	–	–	↓	9	–	–	–	↓	↓
		10	–	–	–	–	370	–	–	↓	10	–	–	–	↓	↓
	$I_{in\ L}$	7	–	–	0.5	–	–	–	–	μAdc	–	7	–	–	8	1,16
		9	–	–	↓	–	–	–	–	↓	–	9	–	–	↓	↓
		10	–	–	↓	–	–	–	–	↓	–	10	–	–	↓	↓
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,10,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,10,13	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	10,13	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	10,13	–	–	4	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	10,13	–	4	3	8	1,16
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓		–		3		
	t_{4+2+}	2	↓	↓	↓	↓	↓	↓	↓	↓		–		2		
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓		–		2		
Rise Time (20 to 80%)	t_{3+}	3	0.9	4.1	1.1	2.5	4.0	1.1	4.6	↓		–	↓	3	↓	↓
	t_{2+}	2	↓	↓	↓	↓	↓	↓	↓	↓		–		2		
Fall Time (20 to 80%)	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





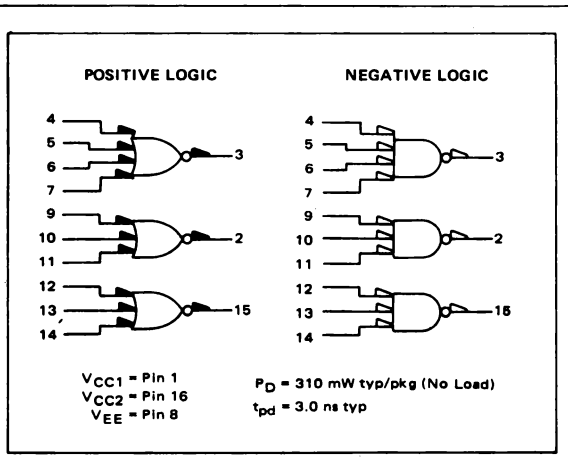
P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10121P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	7	–	–	–	–	265	–	–	μAdc	7	–	–	–	8	1,16
		9	–	–	–	–	265	–	–	↓	9	–	–	–	↓	↓
		10	–	–	–	–	370	–	–		10	–	–	–		
	$I_{in\ L}$	7	–	–	0.5	–	–	–	–	μAdc	–	7	–	–	8	1,16
		9	–	–	↓	–	–	–	–	↓	–	9	–	–	↓	↓
		10	–	–		–	–	–	–		–	10	–	–		
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,10,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,10,13	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	10,13	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	10,13	–	–	4	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	–	–	1.4	2.3	3.4	–	–	ns	10,13	–	4	3	8	1,16
	t_{4-3+}	3	–	–	↓	↓	↓	–	–			–		3		
	t_{4+2+}	2	–	–				–	–			–		2		
	t_{4-2-}	2	–	–				–	–			–		2		
Rise Time (20 to 80%)	t_{3+}	3	–	–	1.1	2.5	4.0	–	–			–		3		
	t_{2+}	2	–	–	↓	↓	↓	–	–			–		2		
Fall Time (20 to 80%)	t_{3-}	3	–	–				–	–			–		3		
	t_{2-}	2	–	–				–	–			–		2		

TRIPLE 4-3-3 INPUT
BUS DRIVER

MC10123



The MC10123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} \leq -2.0$ Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10123 are "turned-off". This elimimates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

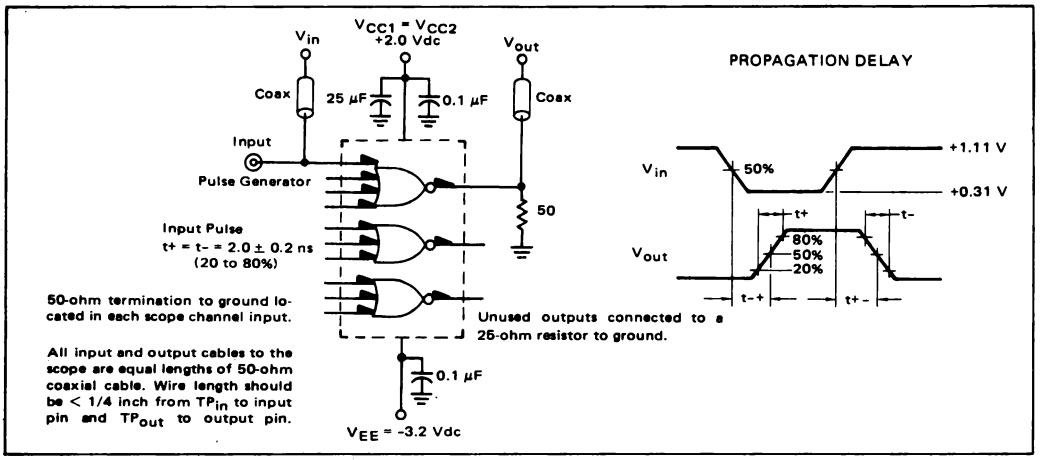
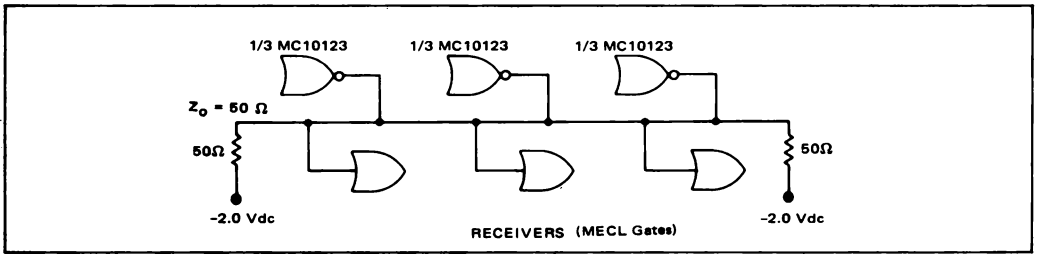


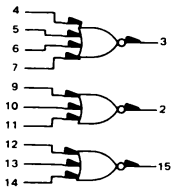
FIGURE 1 – 50-OHM BUS DRIVER

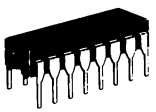


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 25-ohm resistor to -2.1 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





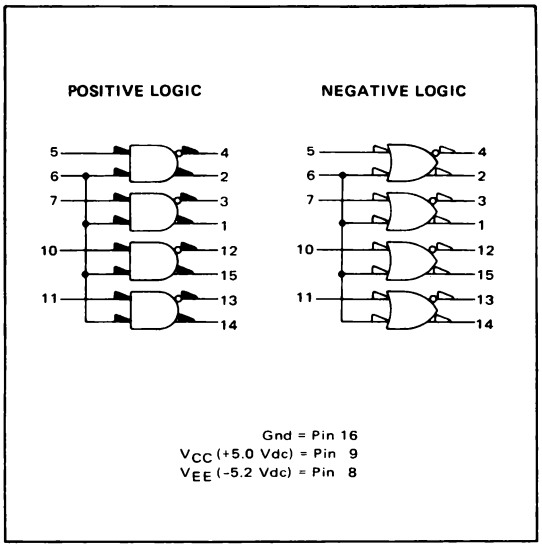
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10123 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	17	21	–	–	mAdc	4,5,6,7,9,10 11,12,13,14	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	µAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	µAdc	–	4			8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-2.100	-2.030	-2.100	–	-2.030	-2.100	-2.030	Vdc	4,5,6,7,9,12	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4,5,6,7	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-2.010	–	–	-2.010	–	-2.010	Vdc	9,12	–	4,5,6,7	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.2	4.6	1.2	3.0	4.4	1.2	4.8	ns	–	–	4	3	8	1,16
	t_{4-3+}	↓	↓	↓	↓	3.0	↓	↓	↓	↓	–	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_{3+}	↓	1.0	3.7	1.0	2.5	3.5	1.0	3.9	↓	–	–	↓	↓	↓	↓
Fall Time (20 to 80%)	t_{3-}	↓	↓	↓	↓	2.5	↓	↓	↓	↓	–	–	↓	↓	↓	↓

QUAD MTTL TO MECL TRANSLATOR

MC10124



The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has MTTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

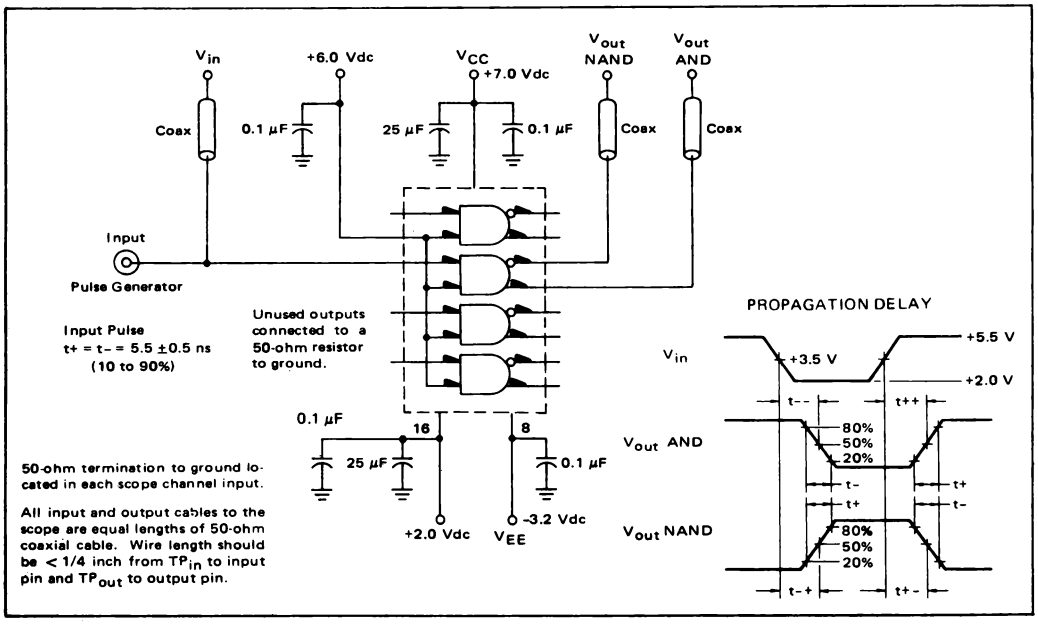
An advantage of this device is that MTTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

P_D = 380 mW typ/pkg (No Load)

t_{pd} = 3.5 ns typ (+1.5 Vdc in to 50% out)

Output Rise, Fall Times;
2.5 ns typ (20% to 80%)

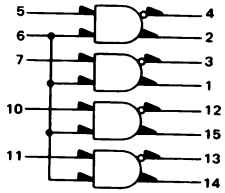
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

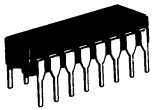


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one translator. The other translators are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

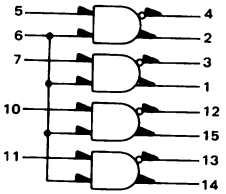
@ Test Temperature	V_{IH}	$V_{IL\ max}$	V_{IHA}	V_{ILA}	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}
	Volts								mA	
-30°C	+4.0	+0.40	+2.00	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+25°C	+4.0	+0.40	+1.80	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+85°C	+4.0	+0.40	+1.80	+0.90	+0.40	+2.40	+5.00	-5.2	-10	+1.0

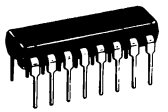
Characteristic	Symbol	Pin Under Test	MC10124L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH}	$V_{IL\ max}$	V_{IHA}	V_{ILA}	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}	Gnd
Negative Power Supply Drain Current	I_E	8	–	–	–	–	-66		–	mAdc							9	8			16
Positive Power Supply Drain Current	I_{CCH}	9	–	–	–	–	16	–	–	mAdc	5,6,7,10,11		–				9	8		–	16
	I_{CCL}	9	–	–	–	–	25	–	–	mAdc							9	8	–		5,6,7,10,11,16
Reverse Current	I_R	6	–	–	–	–	200	–	–	μAdc	–	–	–	–	5,7,10,11	6	9	8			16
		7	–	–	–	–	50	–	–	μAdc	–	–	–	–	6	7	9	8			16
Forward Current	I_F	6	–	–	–	–	-12.8	–	–	mAdc	5,7,10,11	–	–	–	6	–	9	8	–	-	16
		7	–	–	–	–	-3.2	–	–	mAdc	6	–	–	–	7	–	9	8	–	–	16
Input Breakdown Voltage	BV_{in}	6			5.5	–				Vdc							9	8		6	5,7,10,11,16
		7	–	–	5.5	–	–	–	–	Vdc		–	–			–	9	8	–	7	6,16
Clamp Input Voltage	V_I	6				–	-1.5			Vdc		–					9	8	6	–	16
		7				–	-1.5			Vdc		–		–		–	9	8	7		16
High Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6,7		–				9	8	–		16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc		6,7		–			9	8			16
Low Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc		6,7	–	–		–	9	8	–	–	16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6,7	–	–			–	9	8	–	–	16
High Threshold Voltage	V_{OHA}	1	-1.080		-0.980		–	-0.910		Vdc	6	–	7				9	8	–	–	16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6			7		–	9	8	–		16
Low Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	–	7		–	9	8			16
		3		-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	7	–	–	–	9	8		–	16
Switching Time (50-Ω load)											+6.0 Vdc	Pulse In	Pulse Out				+7.0 Vdc	-3.2 Vdc			+2.0 Vdc
Propagation Delay (+3.5 Vdc to 50%)①	t_{6+1+}	1	1.5	6.8	1.5	3.5	6.0	1.0	6.0	ns	7	6	1			–	9	8			16
	t_{6-1-}		1.0	6.0				1.5	6.8		7	6									
	t_{7+1+}		1.5	6.8				1.0	6.0		6	7									
	t_{7-1-}		1.0	6.0				1.5	6.8							–				–	
	t_{7+3-}	3	1.5	6.8				1.0	6.0				3			–			–	–	
	t_{7-3+}	3	1.0	6.0				1.5	6.8				3			–			–	–	
Rise Time (20% to 80%)	t_{1+}	1	1.0	4.2	1.1	2.5	3.9	1.1	4.3				1			–			–	–	
Fall Time (80% to 20%)	t_{1-}	1	1.0	4.2	1.1	2.5	3.9	1.1	4.3				1	–	–	–			–	–	

① See switching time test circuit. Propagation delay for this circuit is specified from +1.5 Vdc in to the 50% point on the output waveform. The +3.5 Vdc is shown here because all logic and supply levels are shifted 2 volts positive.)

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one translator. The other translators are tested in the same manner.





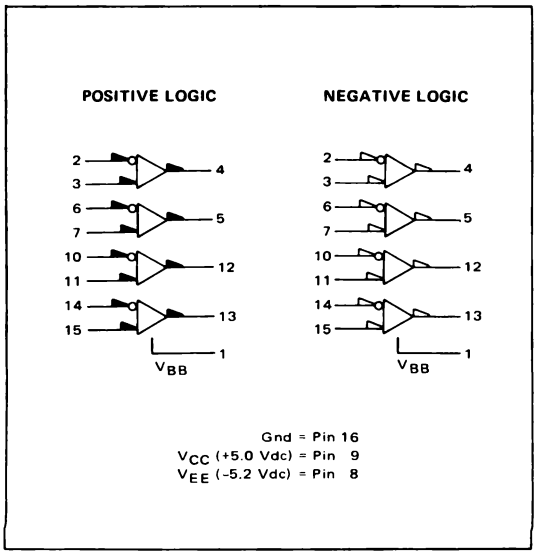
P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	V_{IH}	$V_{IL\ max}$	V_{IHA}	V_{ILA}	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}
	Volts								mA	
−30°C	+4.0	+0.40	+2.00	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+25°C	+4.0	+0.40	+1.80	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+85°C	+4.0	+0.40	+1.80	+0.90	+0.40	+2.40	+5.00	-5.2	-10	+1.0

Characteristic	Symbol	Pin Under Test	MC10124P Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH}	$V_{IL\ max}$	V_{IHA}	V_{ILA}	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}	Gnd
Negative Power Supply Drain Current	I_E	8	–	–	–	–	-66	–	–	mAdc	–	–	–	–	–	–	9	8	–	–	16
Positive Power Supply Drain Current	I_{CCH}	9	–	–	–	–	16	–	–	mAdc	5,6,7,10,11	–	–	–	–	–	9	8	–	–	16
	I_{CCL}	9	–	–	–	–	25	–	–	mAdc	–	–	–	–	–	–	9	8	–	–	5,6,7,10,11,16
Reverse Current	I_R	6	–	–	–	–	200	–	–	µAdc	–	–	–	–	5,7,10,11	6	9	8	–	–	16
		7	–	–	–	–	50	–	–	µAdc	–	–	–	–	6	7	9	8	–	–	16
Forward Current	I_F	6	–	–	–	–	-12.8	–	–	mAdc	5,7,10,11	–	–	–	6	–	9	8	–	–	16
		7	–	–	–	–	-3.2	–	–	mAdc	6	–	–	–	7	–	9	8	–	–	16
Input Breakdown Voltage	BV_{in}	6	–	–	5.5	–	–	–	–	Vdc	–	–	–	–	–	–	9	8	–	6	5,7,10,11,16
		7	–	–	5.5	–	–	–	–	Vdc	–	–	–	–	–	–	9	8	–	7	6,16
Clamp Input Voltage	V_I	6	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	–	9	8	6	–	16
		7	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	–	9	8	7	–	16
High Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6,7	–	–	–	–	–	9	8	–	–	16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	6,7	–	–	–	–	9	8	–	–	16
Low Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,7	–	–	–	–	9	8	–	–	16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6,7	–	–	–	–	–	9	8	–	–	16
High Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	7	–	–	–	9	8	–	–	16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	–	7	–	–	9	8	–	–	16
Low Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	–	7	–	–	9	8	–	–	16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	7	–	–	–	9	8	–	–	16
Switching Time (50-Ω load)											+6.0 Vdc	Pulse In	Pulse Out				+7.0 Vdc	-3.2 Vdc			+2.0 Vdc
Propagation Delay (+3.5 Vdc to 50%)①	t_{6+1+}	1	–	–	1.0	3.5	6.0	–	–	ns	7	6	1	–	–	–	9	8	–	–	16
	t_{6-1-}		–	–				–	–		7	6		–	–	–			–	–	
	t_{7+1+}		–	–				–	–		6	7		–	–	–			–	–	
	t_{7-1-}		–	–				–	–					–	–	–			–	–	
	t_{7+3-}	3	–	–				–	–				3	–	–	–			–	–	
	t_{7-3+}	3	–	–				–	–				3	–	–	–			–	–	
Rise Time (20% to 80%)	t_{1+}	1	–	–	1.1	2.5	3.9	–	–				1	–	–	–			–	–	
Fall Time (80% to 20%)	t_{1-}	1	–	–	1.1	2.5	3.9	–	–				1	–	–	–			–	–	

① See switching time test circuit. Propagation delay for this circuit is specified from +1.5 Vdc in to the 50% point on the output waveform. The +3.5 Vdc is shown here because all logic and supply levels are shifted 2 volts positive.)

MC10125



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (-5.2 Vdc) = Pin 8

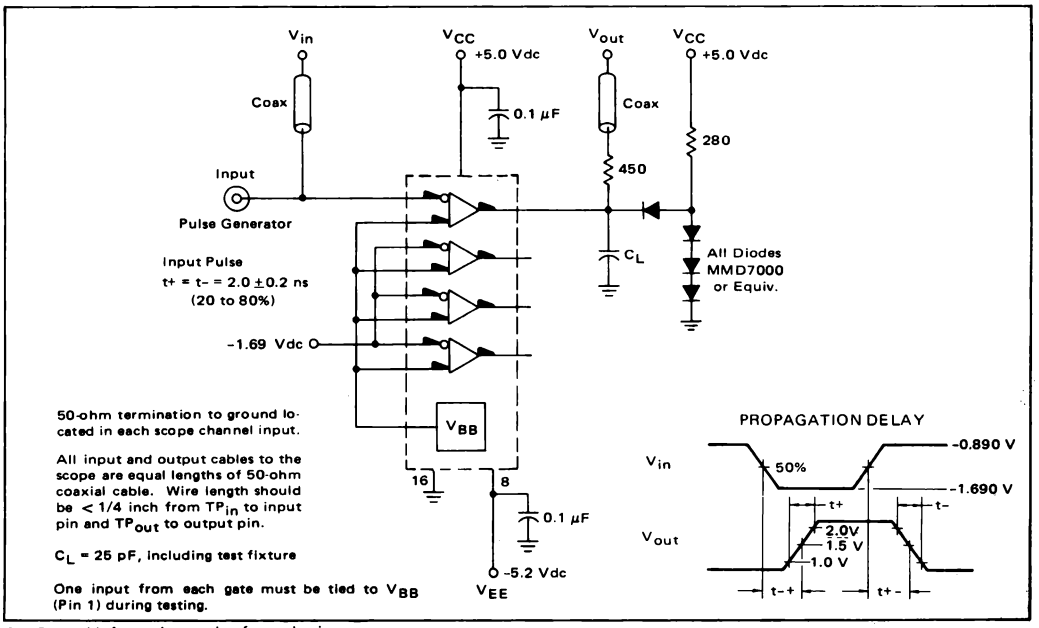
The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky MTTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and -5.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 MTTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or MTTL out. This device has an input common mode noise rejection of ±1.0 Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the MTTL equipment. This isolates the MECL logic from the noisy MTTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

P_D = 380 mW typ/pkg (No Load)
t_{pd} = 4.5 ns typ (50% to +1.5 Vdc out)
Output Rise, Fall Times;
2.5 ns typ (20% to 80%)
V_{CCmax} = +7.00 Vdc

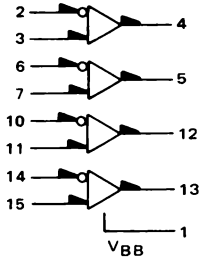
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

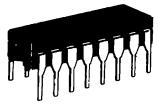


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one translator. The other translators are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

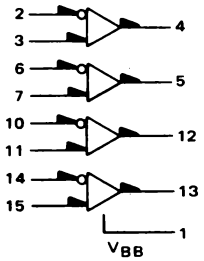
@ Test Temperature	TEST VOLTAGE VALUES (Volts)											Gnd	Output Condition
	$V_{IH\ max}$	$V_{IL\ min}$	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}		
-30°C	-0.890	-1.890	-1.205	-1.500	+0.110	-0.890	-1.890	-2.890	From Pin 1	+5.0	-5.2		
+25°C	-0.810	-1.850	-1.105	-1.475	+0.190	-0.850	-1.810	-2.850		+5.0	-5.2		
+85°C	-0.700	-1.825	-1.035	-1.440	+0.300	-0.825	-1.700	-2.825		+5.0	-5.2		

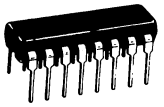
Characteristic	Symbol	Pin Under Test	MC10125L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_E	8	–	–	–	–	40	–	–	mAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Positive Power Supply Drain Current	I_{CCH}	9	–	–	–	–	52	–	–	mAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
	I_{CCL}	9	–	–	–	–	39	–	–	mAdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Input Current	$I_{in}H$ ①	2	–	–	–	–	115	–	–	µAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	
Input Leakage Current	I_{CBO}	2	–	–	–	–	1.0	–	–	µAdc	–	–	–	–		–	–	–	3,7,11,15	9	2,6,8,10,14	16	
High Output Voltage	V_{OH}	4	2.5	–	2.5	–	–	2.5		Vdc	–	2,6,10,14	–	–		–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Output Voltage	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	2,6,10,14	–	–	–	–	–		–	3,7,11,15	9	8	16	20 mA
High Threshold Voltage	V_{OHA}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	6,10,14	–	2	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Threshold Voltage	V_{OLA}	4	–	0.5	–	–	0.5	–	0.5	Vdc	6,10,14	–	2	–	–	–	–	–	3,7,11,15	9	8	16	20 mA
Indeterminate Input Protection Tests	V_{OLS1}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–		9	2,3,6,7,8, 10,11,14,15	16	20 mA
	V_{OLS2}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–		–	–	–	–	–	–	9	8	16	20 mA
Short-Circuit Current	I_{OS}	4	–	–	40	–	100	–	–	mA	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	4,16	
Reference Voltage	V_{BB}	1	-1.420	-1.28	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	2,6,10,14		–	–	–	–	–	3,7,11,15	–		–	
Common Mode Rejection Tests	V_{OH}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	–	–	–	3	2	–	–	–	9	8	16	-2.0 mA
		4	2.5	–	2.5	–	–	2.5	–		–	–	–	–	–	–	3	2	–	9	8	16	-2.0 mA
	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	2	3	–	–	–	9	8	16	20 mA
		4	–	0.5	–	–	0.5	–	0.5		–	–	–	–	–	–	2	3	–	9	8	16	20 mA
Switching Times											**Pulse In**	**Pulse Out**	**C_L (pF)**										
Propagation Delay (50% to +1.5 Vdc)	t_{6+5-}	5	1.0	6.0	1.0	4.5	6.0	1.0	6.0	ns	6	5	25	–	–		–	–	3,7,11,15	9	8	16	–
	t_{6-5+}	5	↓	↓	↓	↓	↓	↓	↓	↓	6	5	↓	–			–		↓	↓	↓	↓	
	t_{2+4-}	4									2	4		–	–	–		–					
	t_{2-4+}	↓									↓	↓	↓	–	–	–	–	–					
Rise Time (+1.0 Vdc to 2.0 Vdc)	t_{4+}		–	3.3	–	–	3.3	–	3.3						–	–							–
Fall Time (+1.0 Vdc to 2.0 Vdc)	t_{4-}	↓	–	3.3	–	–	3.3	–	3.3	↓	↓	↓	↓	–			–	–	↓	↓	↓	↓	–

① Individually test each input, apply $V_{IH\ max}$ to pin under test.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one translator. The other translators are tested in the same manner.





P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts)										
	$V_{IH\ max}$	$V_{IL\ min}$	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	+0.110	-0.890	-1.890	-2.890	From Pin 1	+5.0	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	+0.190	-0.850	-1.810	-2.850		+5.0	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	+0.300	-0.825	-1.700	-2.825		+5.0	-5.2

Characteristic	Symbol	Pin Under Test	MC10125P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_E	8	–	–	–	–	40	–	–	mAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Positive Power Supply Drain Current	I_{CCH}	9	–	–	–	–	52	–	–	mAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
	I_{CCL}	9	–	–	–	–	39	–	–	mAdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Input Current	I_{in} H ①	2	–	–	–	–	115	–	–	µAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	
Input Leakage Current	I_{CBO}	2	–	–	–	–	1.0	–	–	µAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	2,6,8,10,14	16	
High Output Voltage	V_{OH}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Output Voltage	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	20 mA
High Threshold Voltage	V_{OHA}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	6,10,14	–	2	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Threshold Voltage	V_{OLA}	4	–	0.5	–	–	0.5	–	0.5	Vdc	6,10,14	–	2	–	–	–	–	–	3,7,11,15	9	8	16	20 mA
Indeterminate Input Protection Tests	V_{OLS1}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–	–	9	2,3,6,7,8, 10,11,14,15	16	20 mA
	V_{OLS2}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–	–	9	8	16	20 mA
Short-Circuit Current	I_{OS}	4	–	–	40	–	100	–	–	mA	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	4,16	
Reference Voltage	V_{BB}	1	-1.420	-1.28	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	2,6,10,14							3,7,11,15	9	8	16	
Common Mode Rejection Tests	V_{OH}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	–	–	–	3	2	–	–	–	9	8	16	-2.0 mA
		4	2.5	–	2.5	–	–	2.5	–		–	–	–	–	–	–	3	2	–	9	8	16	-2.0 mA
	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	2	3	–	–	–	9	8	16	20 mA
		4	–	0.5	–	–	0.5	–	0.5		–	–	–	–	–	–	2	3	–	9	8	16	20 mA
Switching Times											Pulse In	Pulse Out	C_L (pF)										
Propagation Delay (50% to +1.5 Vdc)	t_{6+5-}	5	–	–	1.0	4.5	6.0	–	–	ns	6	5	25	–	–	–	–	–	3,7,11,15	9	8	16	–
	t_{6-5+}	5	–	–	↓	↓	↓	–	–		6	5	↓	–	–	–	–	–	↓	↓	↓	↓	–
	t_{2+4-}	4	–	–				–	–		2	4		–	–	–	–	–					–
	t_{2-4+}	↓	–	–				–	–		↓	↓		–	–	–	–	–					–
Rise Time (+1.0 Vdc to 2.0 Vdc)	t_{4+}		–	–	–	–	3.3	–	–					–	–	–	–	–					–
Fall Time (+1.0 Vdc to 2.0 Vdc)	t_{4-}	↓	–	–	–	–	3.3	–	–		↓	↓	↓	–	–	–	–	–	↓	↓	↓	↓	–

① Individually test each input, apply $V_{IH\ max}$ to pin under test.

MC10128

Advance Information

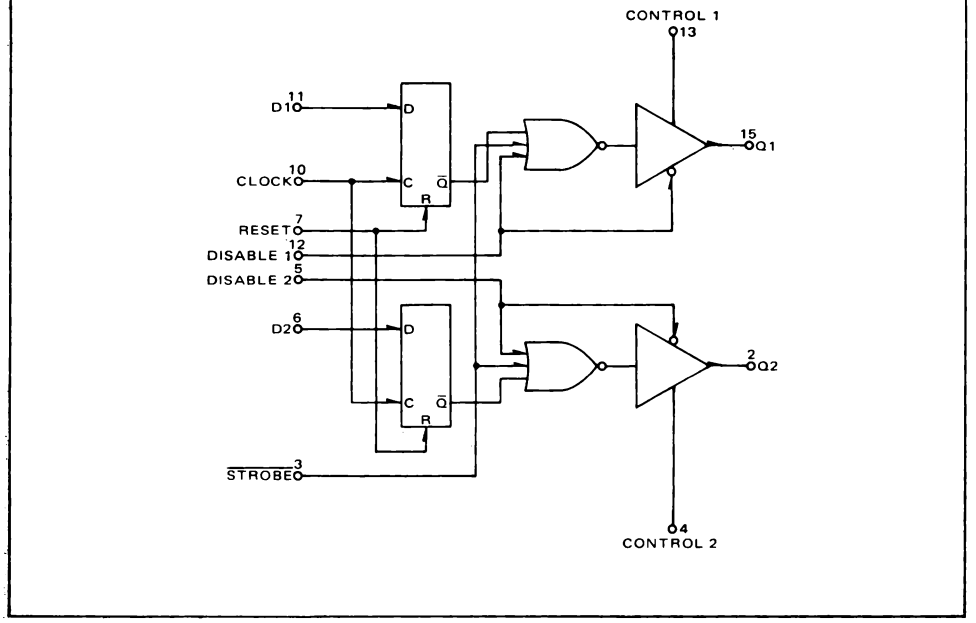
The MC10128 is designed to provide outputs which are compatible with IBM-type bus levels; or, if desired, it will drive TTL type loads and/or provide TTL three-state outputs. The inputs accept MECL 10,000 levels. The MC10128 output levels can be accepted by the MC10129 Bus Receiver.

The operating mode IBM or TTL is selected by tying the external control pins to ground or leaving them open. Leaving a control pin open selects the TTL mode, and tying a control pin to ground selects the IBM mode.

The TTL mode will drive a 25-ohm load, terminated to +1.5 Vdc or a 50-ohm load, terminated to ground. The device has totem-pole type outputs, but it also has a disable input for three-state logic operation when the circuit is used in the TTL mode. When in the high state the disable input causes the output to exhibit a high impedance state when it would normally be a positive logic "1" state. When the strobe is in the high state it inhibits the output data to the low state.

Latches are provided on each data input for temporary storage. When the clock input is in the low logic state, information present at the data inputs D1 and D2 will be fed directly to the latch output. When the clock goes high, the input data is latched. The outputs are gated to allow full bus driving and strobing capability.

The MC10128 is useful in interfacing and bus applications in central processors, mini-computers, and peripheral equipment.



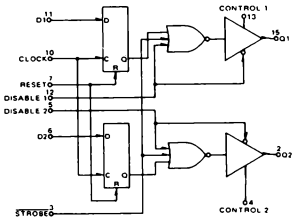
V_{CC} = Pin 14
Gnd 1 = Pin 16
Gnd 2 = Pin 1
Gnd 3 = Pin 9
V_{EE} = Pin 8

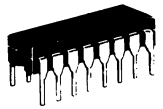
P_D = 700 mW pkg/typ (No Load)
t_{pd} = 12 ns typ

This is advance information and specifications are subject to change without notice.
See General Information section for packaging, and maximum ratings.

ELECTRICAL CHARACTERISTICS – MTTL MODE

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.





L SUFFIX
CERAMIC PACKAGE
CASE 620

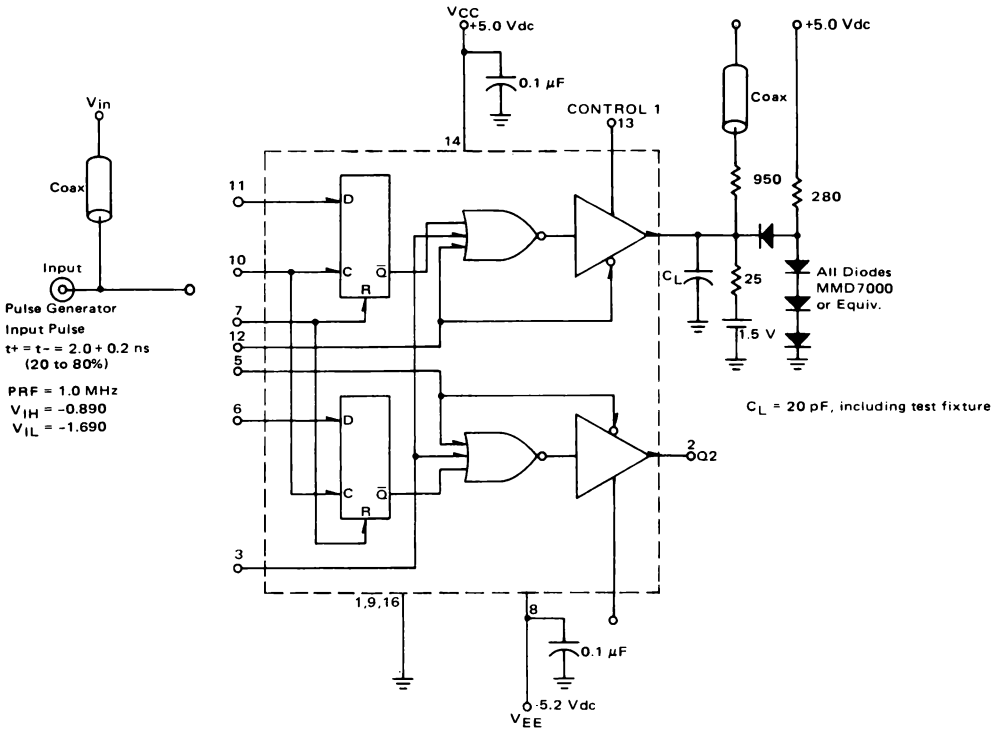
@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}
	Volts						mAdc	µAdc	mAdc
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+5.00	-50	-100	+56
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+5.00	-50	-100	+56
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+5.00	-50	-100	+56

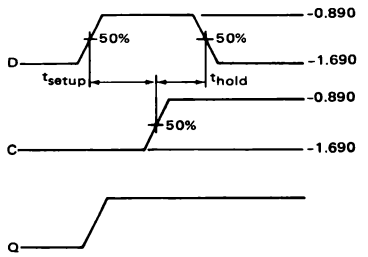
Characteristic	Symbol	Pin Under Test	MC10128L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}	Gnd
										TEST VOLTAGE APPLIED TO PINS LISTED BELOW:									
Negative Power Supply Drain Current	I_E	8	–	–	–	97	–	–	mAdc	6,11	–	–	–	8	14	–	–	–	1, 9,16
Positive Power Supply Drain Current	I_{CC}	14	–	–	–	73	–	–	mAdc	6,11	–	–	–	8	14	–	–	–	1, 9,16
Input Leakage Current	I_{inH}	3	–	–	–	620	–	–	µAdc	3	–	–	–	8	14	–	–	–	1, 9,16
		7	–	–	–	350	–	–		7	–	–	–			–	–	–	
		10	–	–	–	265	–	–		10	–	–	–			–	–	–	
		11	–	–	–	265	–	–		11	–	–	–			–	–	–	
		12	–	–	–	500	–	–		12	–	–	–			–	–	–	
	I_{inL}	All	–	–	0.5	–	–	–	µAdc	–		–	–	8	14	–	–	–	1, ,9,16
Logic "1" Output Voltage	V_{OH}	15	–	–	2.5	–	–	–	Vdc	11	–	–	–	8	14	2,15	–	–	1, ,9,16
		15	–	–	2.7	–	–	–	Vdc	11	–	–	–	8	14	–	2,15	–	1, ,9,16
Logic "0" Output Voltage	V_{OL}	15	–	–	–	0.5	–	–	Vdc	3	–	–	–	8	14	–	–	2,15	1, ,9,16
		2	–	–	–	0.5	–	–	Vdc	3	–	–	–	8	14	–	–	2,15	1, ,9,16
Logic "1" Threshold Voltage	V_{OHA}	15	–	–	2.5	–	–	–	Vdc	11	7	–	10 ③	8	14	2,15	–	–	1, ,9,16
		2	–	–	2.5	–	–	–	Vdc	6	7	–	10 ③	8	14	2,15	–	–	1, ,9,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	–	–	0.5	–	–	Vdc	11	7,10	3	–	8	14	–	–	2,15	1, ,9,16
		2	–	–	–	0.5	–	–	Vdc	6	7,10	3	–	8	14	–	–	2,15	1, ,9,16
Output Short Circuit Current	I_{SC}	15	–	–	–	260	–	–	mAdc	11	–	–	–	8	14	–	–	–	1,2, ,9 ,15,16
		2	–	–	–	260	–	–	mAdc	6	–	–	–	8	14	–	–	–	1,2, ,9 ,15,16
Switching Times † Propagation Delay										-0.890 V	-1.690 V	Pulse In	Pulse Out						
Data Input	t_{11+15+}	,5	–	–	3.5	18	–	–	ns	–	10	11	15	8	14	–	–	–	1, 9 ,16
	t_{11-15-}	15	–	–		18	–	–		–	10	11				–	–	–	
Clock Input	t_{10-15+}	15 ①	–	–		20	–	–		–	–	10,11				–	–	–	
	t_{10-15-}	15 ②	–	–			–	–		–	–	10,11				–	–	–	
Reset Input	t_{7+15-}	15 ②	–	–			–	–		11	–	7,10				–	–	–	
	t_{7+2-}	2 ②	–	–			–	–		6		7,10	2			–	–	–	
STROBE Input	t_{3+15-}	15	–	–	2.5	18	–	–		11	10	3	15			–	–	–	
	t_{3-15+}	15	–	–			–	–		–			15			–	–	–	
	t_{3+2-}	2	–	–			–	–		6			2			–	–	–	
	t_{3-2+}	2	–	–			–	–		–			2			–	–	–	
Setup Time	t_{setupH}	15	–	–	–	–	–	–		–	–	10,11	15			–	–	–	
	t_{setupL}	15	–	–	–	–	–	–		–	–					–	–	–	
Hold Time	t_{holdH}	15	–	–	–	–	–	–		–	–					–	–	–	
	t_{holdL}	15	–	–	–	–	–	–		–	–					–	–	–	
Rise Time (20% to 80%)	t_{15+}	15	–	–	1.0	8.0	–	–		–	10	11				–	–	–	
Fall Time (20% to 80%)	t_{15-}	15	–	–	1.0	8.0	–	–		–	10	11				–	–	–	

* Apply V_{ILmin} individually to pin under test.
① Output latched to logic Low state prior to test.
② Output latched to logic High state prior to test.
† See waveforms

③ A pulse is applied to pin 10.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – MTTL MODE



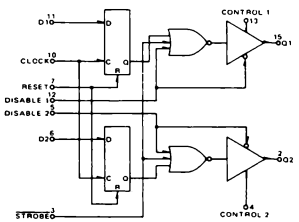


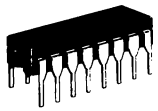
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

ELECTRICAL CHARACTERISTICS — IBM MODE

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.



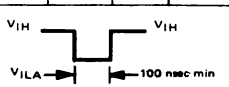


L SUFFIX
CERAMIC PACKAGE
CASE 620

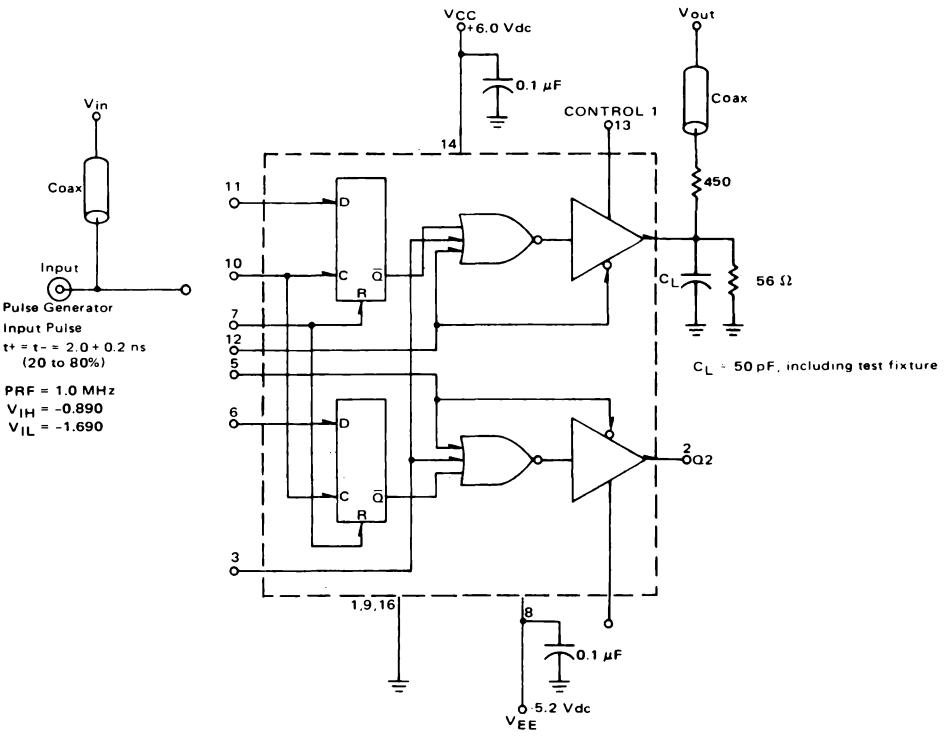
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES: TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	mAdc I_{OH1}	μAdc I_{OH2}	μAdc I_{OL}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+6.00	-59.3	-30	-240
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+6.00	-59.3	-30	-240
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+6.00	-59.3	-30	-240

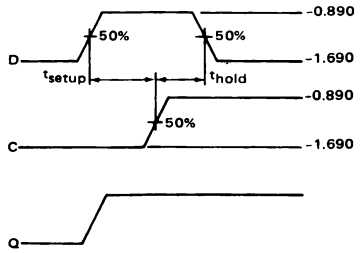
Characteristic	Symbol	Pin Under Test	MC10128L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}	Gnd
Negative Power Supply Drain Current	I_E	8	–	–	–	97	–	–	mAdc	6,11	–	–	–	8	14	–	–	–	1,4,9,13,16
Positive Power Supply Drain Current	I_{CC}	14	–	–	–	73	–	–	mAdc	6,11	–	–	–	8	14	–	–	–	1,4,9,13,16
Input Leakage Current	I_{inH}	3	–	–	–	620	–	–	μAdc	3	–	–	–	8	14	–	–	–	1,4,9,13,16
		7	–	–	–	350	–	–	↓	7	–	–	–	↓	↓	–	–	–	↓
		10	–	–	–	265	–	–		10	–	–	–			–	–	–	
		11	–	–	–	265	–	–		11	–	–	–			–	–	–	
		12	–	–	–	500	–	–		12	–	–	–			–	–	–	
	I_{inL}	All	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	14	–	–	–	1,4,9,13,16
Logic "1" Output Voltage	V_{OH}	15	–	–	3.11	–	–	–	Vdc	11	–	–	–	8	14	2,15	–	–	1,4,9,13,16
		15	–	–	–	5.85	–	–	Vdc	11	–	–	–	8	14	–	2,15	–	1,4,9,13,16
Logic "0" Output Voltage	V_{OL}	15	–	–	-0.5	0.15	–	–	Vdc	3	–	–	–	8	14	–	–	2,15	1,4,9,13,16
		2	–	–	-0.5	0.15	–	–	Vdc	3	–	–	–	8	14	–	–	2,15	1,4,9,13,16
Logic "1" Threshold Voltage	V_{OHA}	15	–	–		2.9	–	–	Vdc	11	7	–	10 ③	8	14	2,15	–	–	1,4,9,13,16
		2	–	–		2.9	–	–	Vdc	6	7	–	10 ③	8	14	2,15	–	–	1,4,9,13,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	–	-0.5	0.25	–	–	Vdc	11	7,10	3	–	8	14	–	–	2,15	1,4,9,13,16
		2	–	–	-0.5	0.25	–	–	Vdc	6	7,10	3	–	8	14	–	–	2,15	1,4,9,13,16
Output Short Circuit Current	I_{SC}	15	–	–	–	320	–	–	mAdc	11	–	–	–	8	14	–	–	–	1,2,4,9,13,15,16
		2	–	–	–	320	–	–	mAdc	6	–	–	–	8	14	–	–	–	1,2,4,9,13,15,16
Switching Times † Propagation Delay										-0.890 V	-1.690 V	Pulse In	Pulse Out						
Data Input	t_{11+15+}	15	–	–	3.5	23	–	–	ns	–	10	11	15	8	14	–	–	–	1,4,9,13,16
	t_{11-15-}	15	–	–	↓	↓	–	–	↓	–	10	11	↓	↓	↓	–	–	–	↓
Clock Input	t_{10-15+}	15 ①	–	–			–	–			–	10,11				–	–	–	
	t_{10-15-}	15 ②	–	–			–	–		–	–	10,11				–	–	–	
Reset Input	t_{7+15-}	15 ②	–	–			–	–		11	–	7,10	↓			–	–	–	
	t_{7+2-}	2 ②	–	–			–	–		6	–	7,10	2			–	–	–	
$\overline{\text{STROBE}}$ Input	t_{3+15-}	15	–	–	2.5		–	–		11	10	3	15			–	–	–	
	t_{3-15+}	15	–	–	↓		–	–		–	↓	↓	15			–	–	–	
	t_{3+2-}	2	–	–			–	–		6			2			–	–	–	
	t_{3-2+}	2	–	–			–	–		–			2			–	–	–	
Setup Time	t_{setupH}	15	–	–	–	–	–	–		–	–	10,11	15			–	–	–	
	t_{setupL}	15	–	–	–	–	–	–		–	–					–	–	–	
Hold Time	t_{holdH}	15	–	–	–	–	–	–		–	–					–	–	–	
	t_{holdL}	15	–	–	–	–	–	–		–	–					–	–	–	
Rise Time (20% to 80%)	t_{15+}	15	–	–	1.0	8.0	–	–		–	10	11				–	–	–	
Fall Time (20% to 80%)	t_{15-}	15	–	–	1.0	8.0	–	–	↓	–	10	11	↓	↓	↓	–	–	–	↓

* Apply V_{ILmin} individually to pin under test.
① Output latched to logic Low state prior to test.
② Output latched to logic High state prior to test.
† See waveforms
③ A pulse is applied to pin 10.



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – IBM MODE



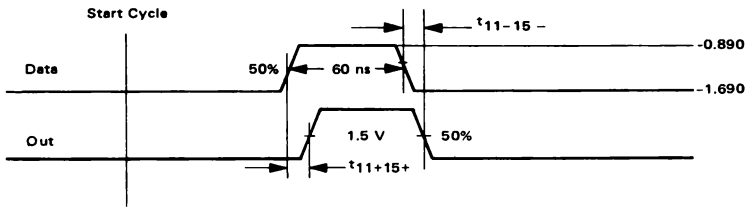


50-ohm termination to ground located in each scope channel input.

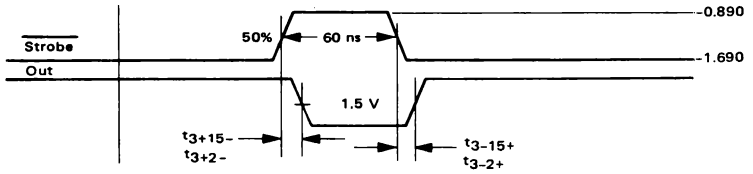
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

VOLTAGE WAVEFORMS

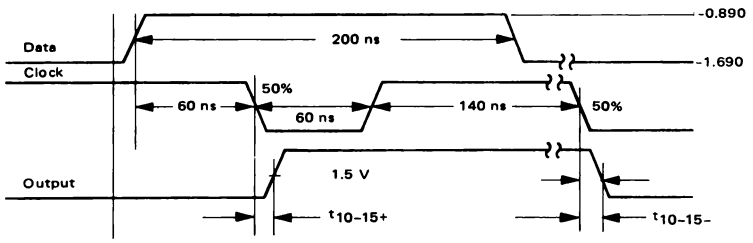
DATA INPUT



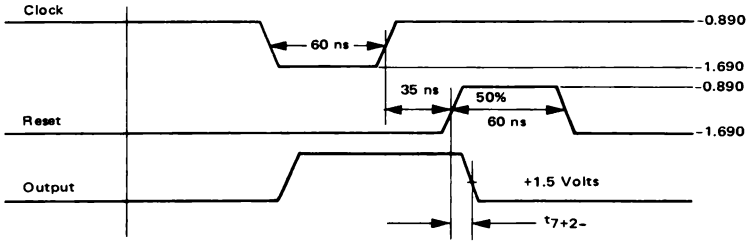
STROBE INPUT



CLOCK INPUT



RESET INPUT



TTL – MODE
V_{OL} = 0.5 Volts Max
V_{OH} = 2.5 Volts Min

IBM – MODE
V_{OL} = 0.25 Volts Max
V_{OH} = 5.85 Volts Min

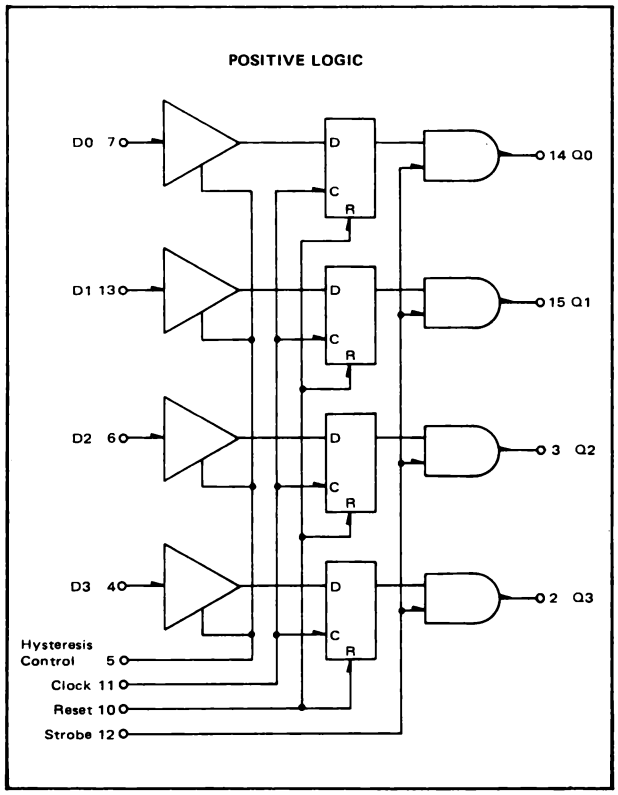
MC10129

The MC10129 bus receiver works in conjunction with the MC10128 to allow interfacing of MECL 10,000 to other forms of logic and logic buses. The data inputs are compatible with, and accept MTTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, the outputs will follow the D inputs, and the reset input is disabled. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to V_{CC} or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pulldown resistors to V_{EE}. They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to V_{EE}. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The other input pins are unaffected by the mode of operation used.

The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipment.



TRUTH TABLE

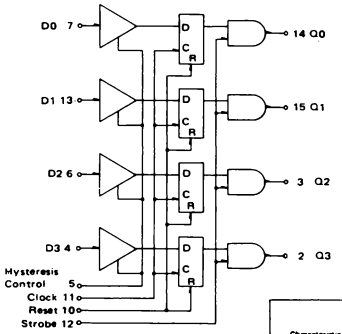
D	C	STROBE	RESET	Q_{n+1}
ϕ	ϕ	L	ϕ	L
ϕ	H	ϕ	H	L
L	L	H	ϕ	L
ϕ	H	H	L	Q_n
H	L	H	ϕ	H

ϕ = Don't Care

P_D = 750 mW typ/pkg (No Load)
t_{pd} = 10 ns typ

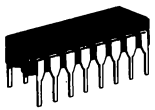
V_{CC} = Pin 9
Gnd = Pins 1 and 16
V_{EE} = Pin 8

See General Information section for packaging and maximum ratings information.



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input/output combination. Other combinations are tested in the same manner.



L SUFFIX
CERAMIC PACKAGE
CASE 620

⊕ Test Temperature	MECL 10,000 INPUT LEVELS V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	* MTTL INPUT LEVELS V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	*IBM INPUT LEVELS V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	HYSTERESIS MODE $V_{IHA''}$	$V_{ILA''}$	$V_{IHA'''}$	$V_{ILA'''}$	V_{CC} ①	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	3.000	0.400	2.000	0.800	3.11	0.150	–	–	2.80	2.00	2.20	1.30	+5.0	−5.2
+25°C	0.810	−1.850	−1.105	−1.475	3.000	0.400	2.000	0.800	3.11	0.150	1.700	0.70	2.600	1.700	1.900	1.000	+5.0	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	3.000	0.400	2.000	0.800	3.11	0.150	–	–	2.30	1.400	1.60		+5.0	−5.2

TEST VOLTAGE VALUES (Volts)

Characteristic	Symbol	Pin Under Test	MC10129 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	$V_{IHA''}$	$V_{ILA''}$	$V_{IHA'''}$	$V_{ILA'''}$	V_{CC} ①	V_{EE}	Gnd
Negative Power Supply Drain Current	I_E	8	–	–	–	–	152	–	–	mAdc	11	12	–														9	8	1,5,16
		8	–	–	–	–	172	–	–	mAdc	11	12															9	5,8	1,16
Positive Power Supply Drain Current	I_{CC}	9	–	–	–	–	80	–	–	mAdc	–	–	–	–	–	4,6,7,13	–	–	–	4,6,7,13	–	–	–	–	–	–	9	8	1,16
Input Current	I_{inH}	4					95			µAdc			–	–	4				4	–							9	8	1,16
		6					↓						–	–	6				6	–									
		7													7				7	–									
		10					450				10,11		–	–															
		11					245				11		–	–															
		12					245				12		–	–															
		13					95						–	–	13														
	I_{inL}	4			–		−1.0		–	µAdc			–	–		4	–	–		4	–	–					9	8	1,16
		6			–		↓		–				–	–		6	–	–		6	–	–							
		7			–				–		–	–	–	–		7	–	–		7	–	–							
		10		–	0.5							10	–	–															
		11		–	↓							11	–	–															
		12		–								12	–	–															
		13		–	–		−1.0		–		–	–	–	–		13	–	–		13	–	–							
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	12	10,11		–	4			–	4			–					9	5,8	1,16
		3	↓	↓	↓		↓	↓	↓		↓	↓		–	6			–	6			–						5,8	1,16
		2												–	4		–	–	4			–						8	1,5,16
		3												–	6		–	–	6			–						8	1,5,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	12	10,11		–		4		–		4		–					9	5,8	1,16
		3	↓	↓	↓		↓	↓	↓		↓	↓		–		6		–		6		–						5,8	1,16
		2												–		4		–		4		–						8	1,5,16
		3												–		6		–		6		–						8	1,5,16
Logic "1" Threshold Voltage	V_{OHA}	2 ④	-1.060	–	-0.980			-0.910	–	Vdc	11,12	–	–	10	4	–			4	–							9	5,8	1,16
		2									–	10,11	12	–	4	–			4	–									
		2									10,12	–		11	4				4	–									
		2									12	10,11			–		4		–		4								
		2 ②									↓	↓			–				–										
		2 ③													–				–				4				8	1,5,16
																											8	1,5,16
Logic "0" Threshold Voltage	V_{OLA}	2 ④	–	-1.655			-1.630	–	-1.595	Vdc	11,12	–	10		4	–			4	–							9	5,8	1,16
		2									–	10,11	–	12	4	–			4	–									
		2									10,12	–	11		4	–			4	–									
		2									12	10,11						4	–			4							
		2 ②																	–										
		2 ③	–		–	–											–	–	–				4				8	1,5,16
																											8	1,5,16
Switching Times Propagation Delay											+1.11 V	+0.31 V	Pulse In	Pulse Out	+5.0 V	+2.40 V	Figure		+5.0 V	+2.40 V	Figure						+7.0 V	−3.2 V	+2.0 V
Data Input	t_{7+14+}	14			6.6	–	27.0		–	ns	12	10,11	7	14	–	–	1		–	–	1		–	–	–	–	9	5,8	1,16
	t_{7-14-}	14			3.7	–	15.0		–		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–			
Clock Input	t_{11+14+}	14	–		2.7	–	11.0		–		12	10	7,11	14	–	–	4		–	–	4		–	–	–	–			
	t_{11-14-}	14	–	–	2.7	–	11.0	–	–		12	10	7,11	14	–	–	4		–	–	4		–	–	–	–			
Strobe Input	t_{12+14+}	14	–	–	1.6		7.0		–		–	10,11	12	14	7	–	2		7	–	2		–	–	–	–			
	t_{12-14-}	14	–		1.6		7.0				–	10,11	12	14	7	–	2		7	–	2		–	–	–	–			
Reset Input	t_{10+14-}	14	–		2.0	–	8.0				12	–	10,11	14	7	7	3		7	–	3		–	–	–	–			
Hysteresis Mode	t_{7+14+}	14	–		–	18.0	–		–		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–		8	1,5,16
	t_{7-14-}	14	–		–	10.0	–		–		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–		8	1,5,16
Setup Time	t_{setup}	14	–		25	–	–		–		12	10	7,11	14	–	–	5		–	–	5		–	–	–	–		5,8	1,16
Hold Time	t_{hold}	14	–		0	–	–		–		12	10	7,11	14	–	–	5		–	–	5		–	–	–	–			
Rise Time	t_+	14	–		1.5	–	4.3				12	10,11	7	14	–	–	1		–	–	1		–	–	–	–			
Fall Time	t_-	14	–	–	1.5	–	4.3	–	–		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–			

*When testing choose either MTTL or IBM Input Levels.

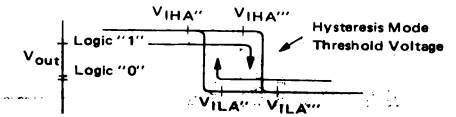
① Operation and limits shown also apply for V_{CC} = +5.0 V

② Input level on data input taken from +0.4 V up to voltage level given.

③ Input level on data input taken from +4.0 V down to voltage level given

④ Output latched to logic high state prior to test.

$V_{IHA'}$, $V_{ILA'}$ are standard logic "1" and logic "0" MTTL threshold voltages.
$V_{IHA''}$, $V_{ILA''}$, $V_{IHA'''}$ and $V_{ILA'''}$ are logic "1" and logic "0" threshold voltages in the hysteresis mode as shown in diagram.



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

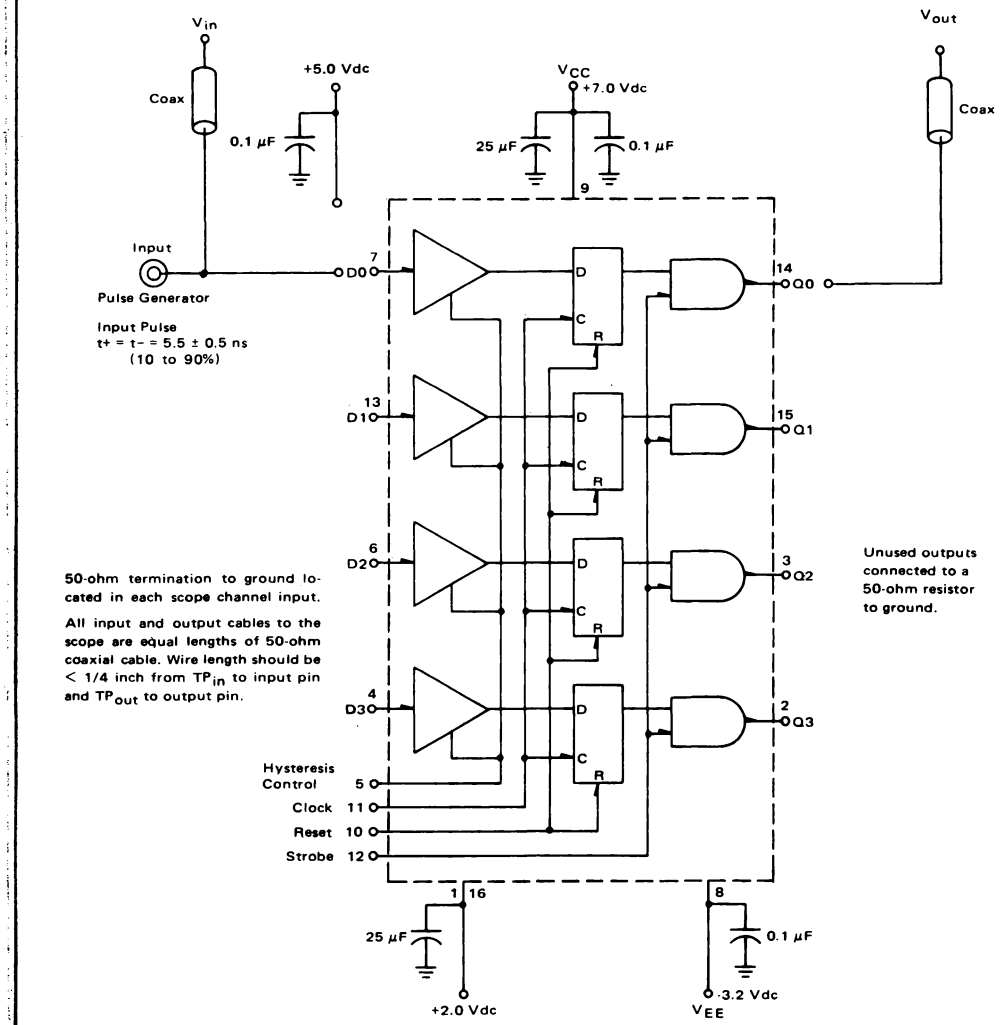


FIGURE 1 – DATA to OUTPUT
(Clock and Reset are low, Strobe is high)

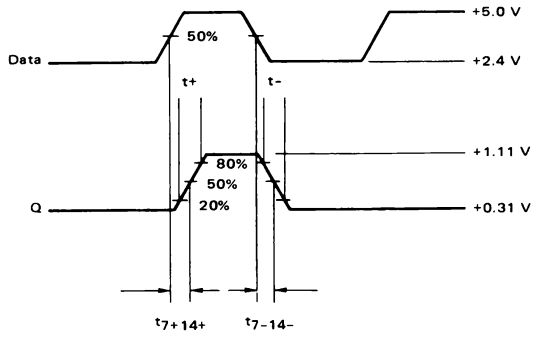


FIGURE 2 – STROBE to OUTPUT
(Data is high, Clock and Reset are low)

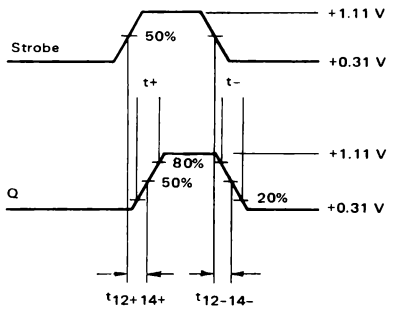


FIGURE 3 – RESET to OUTPUT
(Data and Strobe are high)

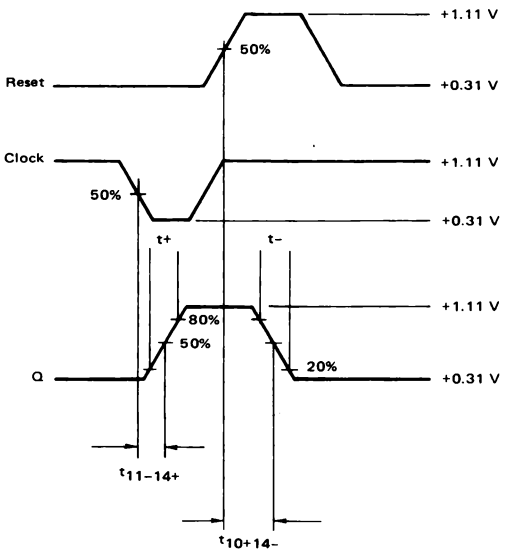


FIGURE 4 – CLOCK to OUTPUT
(Reset is low, Strobe is high)

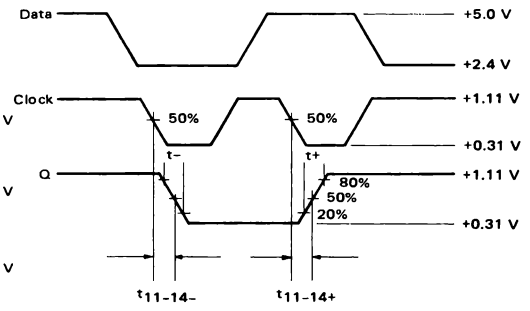
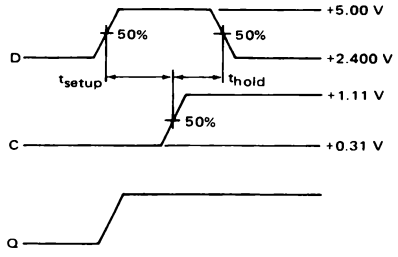


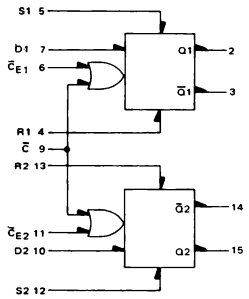
FIGURE 5 – $T_{SET\ UP}$ AND T_{HOLD} WAVEFORMS



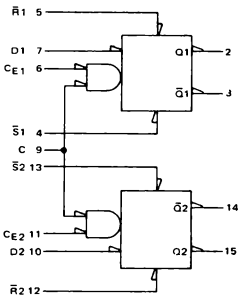
DUAL LATCH

MC10130

POSITIVE LOGIC



NEGATIVE LOGIC



TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
ϕ	L	H	Q_n
ϕ	H	L	Q_n
ϕ	H	H	Q_n

ϕ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 155 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

The MC10130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{C}_E$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

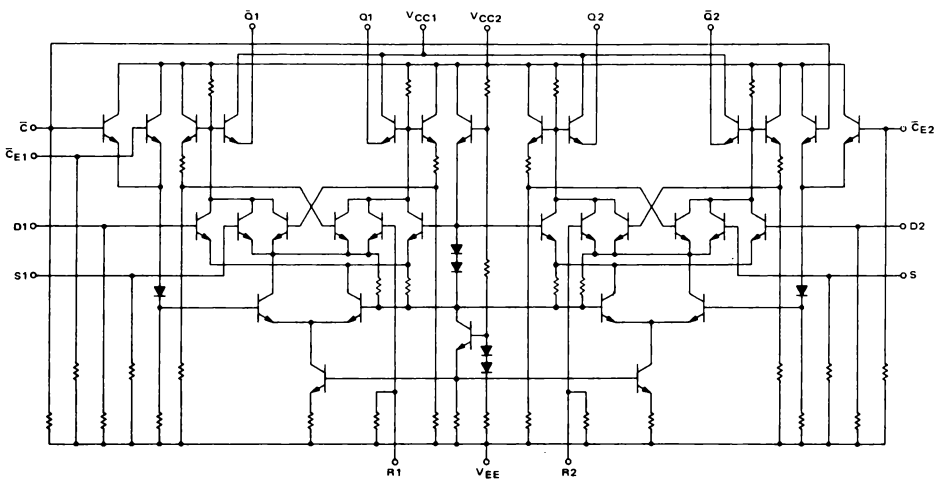
Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

Output rise and fall times have been optimized to provide relaxation of system layout and design criteria.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

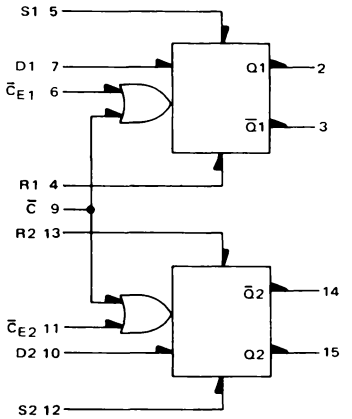
CIRCUIT SCHEMATIC

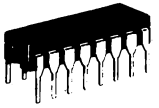


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one latch. The other latch is tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

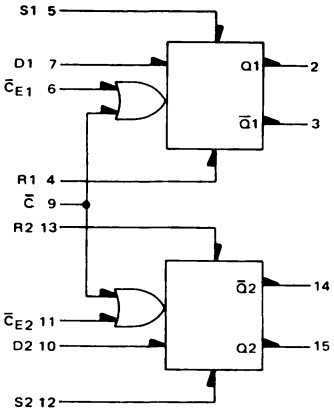
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

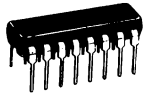
Characteristic	Symbol	Pin Under Test	MC10130L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	30	35	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6,11	–	–	–	–	220	–	–	μAdc	6,11	–	–	–	8	1,16
		9	–	–	–	–	265	–	–	↓	9	–	–	–	↓	↓
		4,5,9	–	–	–	–	285	–	–		4,5,9	–	–	–		
		7,10,12,13	–	–	–	–	285	–	–		7,10,12,13	9	–	–		
	I_{inL}	4*	–	–	0.50	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9	–	–	8	1,16
Switching Times (50 Ω Load) (See Figure 1)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+2+}	2	1.0	3.6	1.0	2.5	3.5	1.0	3.8	ns	–	–	7	2	8	1,16
	t_{5+2+}	↓	↓	3.6	↓	2.7	↓	1.1	3.9	↓	6	–	5	↓	↓	↓
	t_{4+2-}			3.6		2.7		1.1	3.9		6	–	4			
	t_{6-2+}			4.3		–	4.0	1.0	4.1		–	–	6			
Rise Time (20% to 80%)	t_{2+}			3.6	1.1	2.7	3.5	1.1	3.8		–		7			
Fall Time (20% to 80%)	t_{2-}	↓	↓	3.6	1.1	2.7	3.5	1.1	3.8	↓	–	–	7	↓	↓	↓
Setup Time	t_{setup}	2	–	–	2.5	–	–	–	–	ns	①	–	6,7	2	8	1,16
Hold Time	t_{hold}	2	–	–	1.5	–	–	–	–	ns	①	–	6,7	2	8	1,16

*All other inputs are tested in the same manner

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one latch. The other latch is tested in the same manner.





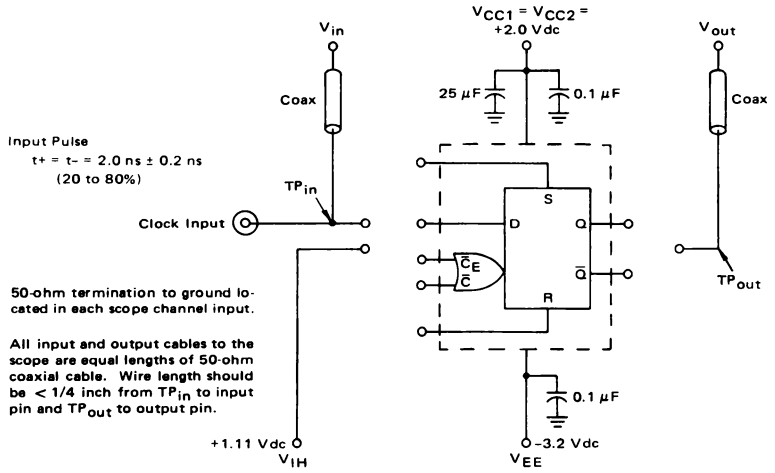
P SUFFIX
PLASTIC PACKAGE
CASE 648

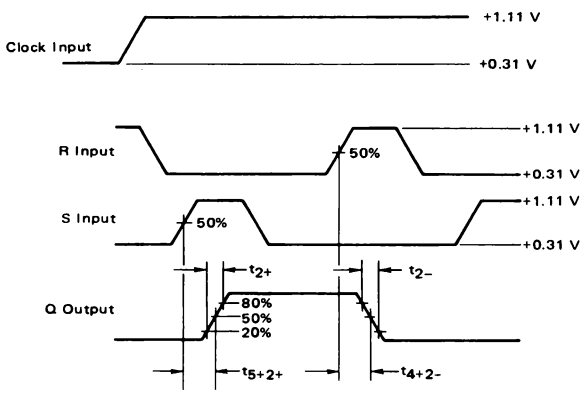
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

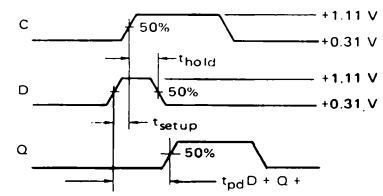
Characteristic	Symbol	Pin Under Test	MC10130P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	30	35	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6,11	–	–	–	–	220	–	–	μAdc	6,11	–	–	–	8	1,16
		9	–	–	–	–	265	–	–	↓	9	–	–	–	↓	↓
		4,5,9	–	–	–	–	285	–	–		4,5,9	–	–	–		
		7,10,12,13	–	–	–	–	285	–	–	↓	7,10,12,13	9	–	–		
	I_{inL}	4*	–	–	0.50	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9	–	–	8	1,16
Switching Times (50 Ω Load) (See Figure 1)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+2+}	2	–	–	1.0	2.5	3.5	–	–	ns	–	–	7	2	8	1,16
	t_{5+2+}		–	–	↓	2.7	↓	–	–	↓	6	–	5	↓	↓	↓
	t_{4+2-}		–	–		2.7		–	–		6	–	4			
	t_{6-2+}		–	–		–	4.0	–	–		–	–	6			
Rise Time (20% to 80%)	t_{2+}	↓	–	–	1.1	2.7	3.5	–	–		–	–	7	↓		
Fall Time (20% to 80%)	t_{2-}		–	–	1.1	2.7	3.5	–	–	↓	–	–	7		↓	↓
Setup Time	t_{setup}	2	–	–	2.5	–	–	–	–	ns	①	–	6,7	2	8	1,16
Hold Time	t_{hold}	2	–	–	1.5	–	–	–	–	ns	①	–	6,7	2	8	1,16

*All other inputs are tested in the same manner

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25° C







NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

DUAL TYPE D MASTER-SLAVE FLIP-FLOP

MC10131

The MC10131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\bar{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

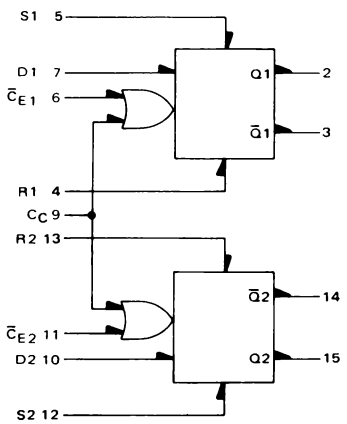
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

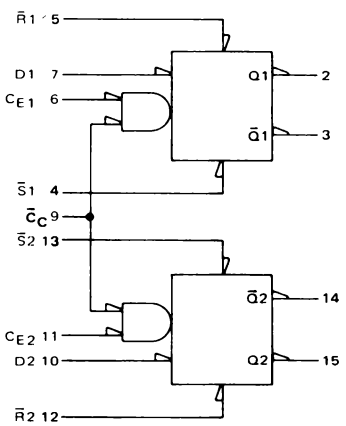
ϕ = Don't Care
$C = \bar{C}_E + C_C$.
A clock H is a clock transition from a low to a high state.

P_D = 235 mW typ/pkg (No Load)
f_{Tog} = 160 MHz typ

POSITIVE LOGIC



NEGATIVE LOGIC

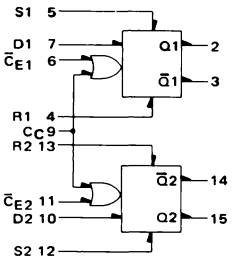


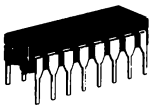
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

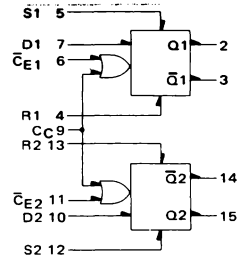
Characteristic	Symbol	Pin Under Test	MC10131L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	45	56	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	330	–	–	μAdc	4	–	–	–	8	1, 16
		5	–	–	–	–	330	–	–		5	–	–	–		
		6	–	–	–	–	220	–	–		6	–	–	–		
		7	–	–	–	–	245	–	–		7	–	–	–		
		9	–	–	–	–	265	–	–		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1, 16
		6,7,9*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1, 16
		2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1, 16
		3†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1, 16
		2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1, 16
		3†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	9	8	1, 16
Switching Times											+1.11 Vdc		Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{9+2-}	2	1.4	4.6	1.5	3.0	4.5	1.5	5.0	ns	–	–	9	2	8	1, 16
	t_{9+2+}	2									7	–	9	2		
	t_{6+2+}	2									7	–	6	2		
	t_{6+2-}	2									–	–	6	2		
Rise Time (20 to 80%)	t_{2+}	2	1.0		1.1	2.5		1.1	4.9		7	–	9	2		
Fall Time (20 to 80%)	t_{2-}	2	1.0		1.1	2.5		1.1	4.9		–	–	9	2		
Set Input Propagation Delay	t_{5+2+}	2	1.1	4.4	1.2	2.8	4.3	1.2	4.8	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15									6	–	12	15		
	t_{5+3-}	3									–	–	5	3		
	t_{12+14-}	14									9	–	12	14		
Reset Input Propagation Delay	t_{4+2-}	2	1.1	4.4	1.2	2.8	4.3	1.2	4.8	ns	–	–	4	2	8	1, 16
	t_{13+15-}	15									6	–	13	15		
	t_{4+3-}	3									–	–	4	3		
	t_{13+14+}	14									9	–	13	14		
Setup Time	t_{setup}	7	–	–	2.5	–	–	–	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{hold}	7	–	–	1.5	–	–	–	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	125	–	125	160	–	125	–	MHz	–	–	6	2	8	1, 16

*Individually test each input; apply V_{IL} min to pin under test.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6).

ELECTRICAL CHARACTERISTICS — ADVANCE INFORMATION*

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.



P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10131P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	45	56	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	330	–	–	μAdc	4	–	–	–	8	1, 16
		5	–	–	–	–	330	–	–		5	–	–	–		
		6	–	–	–	–	220	–	–		6	–	–	–		
		7	–	–	–	–	245	–	–		7	–	–	–		
		9	–	–	–	–	265	–	–		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1, 16
		6,7,9*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1, 16
		2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1, 16
		3†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1, 16
		2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1, 16
		3†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	9	8	1, 16
Switching Times											+1.11 Vdc		Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{9+2-}	2	–	–	1.5	3.0	4.5	–	–	ns	–	–	9	2	8	1, 16
	t_{9+2+}	2	–	–				–	–		7	–	9	2		
	t_{6+2+}	2	–	–				–	–		7	–	6	2		
	t_{6+2-}	2	–	–				–	–		–	–	6	2		
Rise Time (20 to 80%)	t_{2+}	2	–	–	1.1	2.5		–	–		7	–	9	2		
Fall Time (20 to 80%)	t_{2-}	2	–	–	1.1	2.5		–	–		–	–	9	2		
Set Input Propagation Delay	t_{5+2+}	2	–	–	1.2	2.8	4.3	–	–	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15	–	–				–	–		6	–	12	15		
	t_{5+3-}	3	–	–				–	–		–	–	5	3		
	t_{12+14-}	14	–	–				–	–		9	–	12	14		
Reset Input Propagation Delay	t_{4+2-}	2	–	–	1.2	2.8	4.3	–	–	ns	–	–	4	2	8	1, 16
	t_{13+15-}	15	–	–				–	–		6	–	13	15		
	t_{4+3-}	3	–	–				–	–		–	–	4	3		
	t_{13+14+}	14	–	–				–	–		9	–	13	14		
Setup Time	t_{setup}	7	–	–	2.5	–	–	–	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{hold}	7	–	–	1.5	–	–	–	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	–	–	125	160	–	–	–	MHz	–	–	6	2	8	1, 16

*Individually test each input; apply $V_{IL\ min}$ to pin under test.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6) — $V_{IH\ max}$, $V_{IL\ min}$

*This is advance information and specifications are subject to change without notice.

FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT

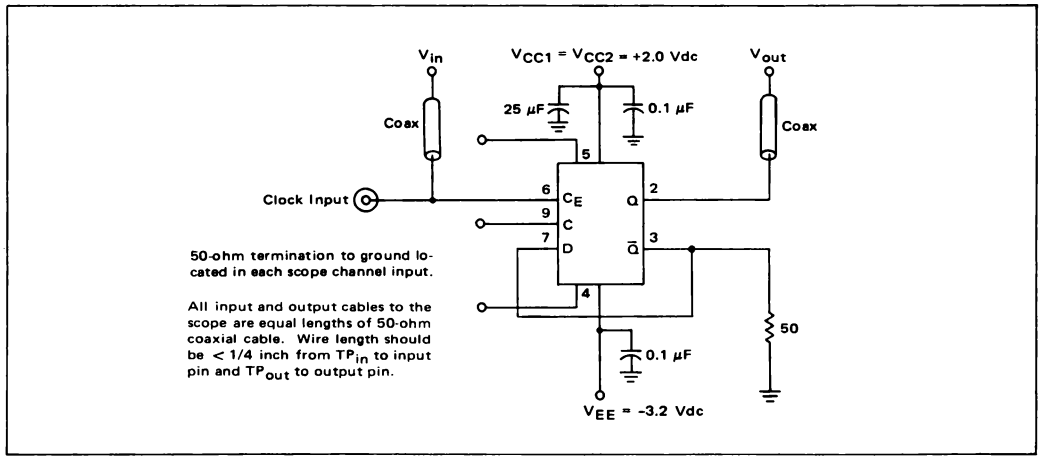
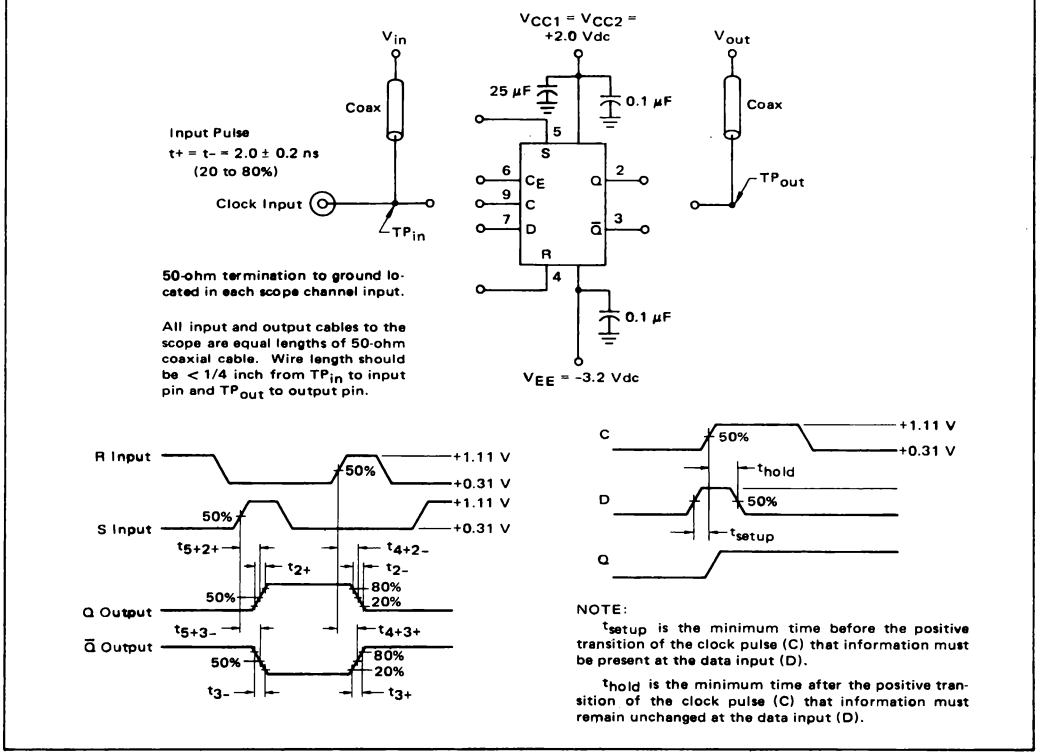


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE:

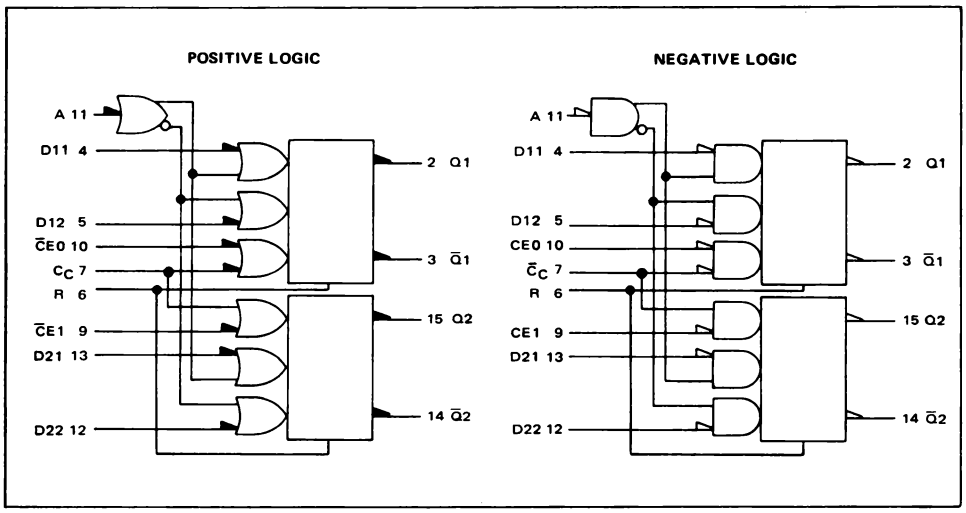
t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

MC10132

The MC10132 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select (A) input determines which data input is enabled. A high (H) level enables data inputs D12 and D22 and a low (L) level enables data inputs D11 and D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled when the clock is in the high state, and disabled when the clock is low.



TRUTH TABLE

R	D	C_C	$\overline{CE}$	Q_{n+1}
ϕ	L	L	L	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
ϕ	H	L	L	H
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	ϕ	ϕ	H	L

ϕ = Don't Care

$D = (\overline{A} \bullet D11) + (A \bullet D12)$

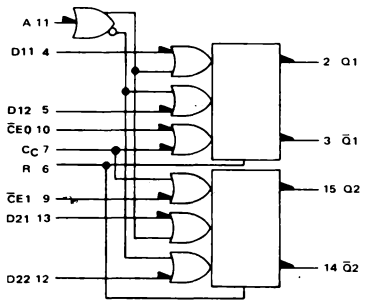
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

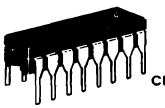
P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one latch. The other latches are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

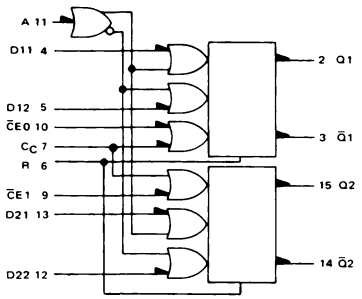
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

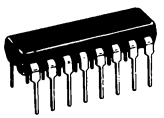
Characteristic	Symbol	Pin Under Test	MC10132L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Current	I_E	8	–	–	–	44	55	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	–	–	–	290	–	–	μAdc	4	–	–	–	8	1,16
		5	–	–	–	–	290	–	–		5	–	–	–		
		6	–	–	–	–	390	–	–		6	–	–	–		
		7	–	–	–	–	290	–	–		7	–	–	–		
		10	–	–	–	–	265	–	–		10	–	–	–		
		11	–	–	–	–	265	–	–		11	–	–	–		
	$I_{in\ L}$	4*	–	–	0.50	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	7,9,10	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,11	7,9,10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	7,9,10	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,11	7,9,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	7,9,10	4	–	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	11	7,9,10	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	7,9,10	4	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	11	7,9,10	5	–	8	1,16
Switching Times (50-ohm load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data	t_{4+2+}	2	–	–	1.0	–	3.3	–	–	ns	–	7,9,10	4	2	8	1,16
Reset	t_{6+2-}		–	–	1.0	–	3.8	–	–		7	–	6			
Clock	t_{7-2+}		–	–	1.0	–	5.7	–	–		4	–	7			
Select	t_{11+2+}		–	–	1.0	–	4.6	–	–		5	7	11			
Setup Time Data	t_{setup}	2	–	–	2.5	–	–	–	–	ns	–	11	4,10	2	8	1,16
Select	t_{setup}	2	–	–	3.5	–	–	–	–	ns	5	7	10,11	2	8	1,16
Hold Time Data	t_{hold}	2	–	–	1.5	–	–	–	–	ns	–	11	4,10	2	8	1,16
Select	t_{hold}	2	–	–	1.0	–	–	–	–	ns	5	7	10,11	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.5	–	3.5	–	–	ns	–	7,9,10	4	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	–	–	1.5	–	3.5	–	–	ns	–	7,9,10	4	2	8	1,16

*All other inputs tested in the same manner.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one latch. The other latches are tested in the same manner.





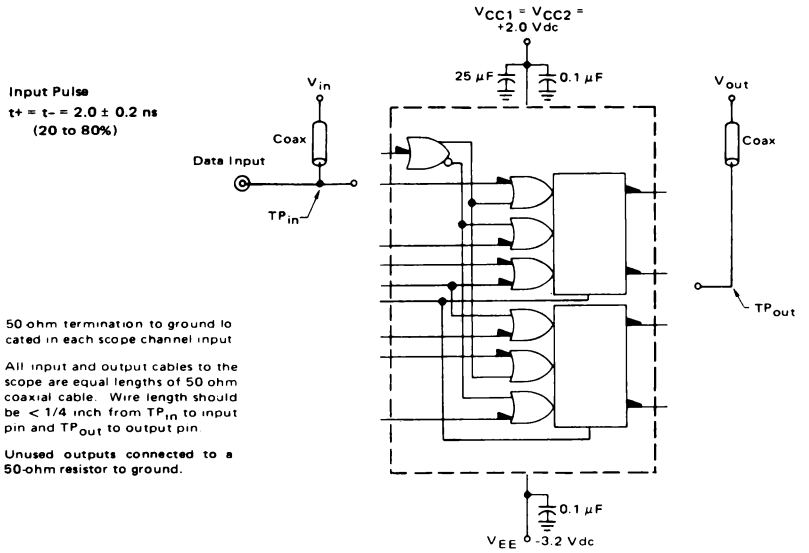
P SUFFIX
PLASTIC PACKAGE
CASE 648

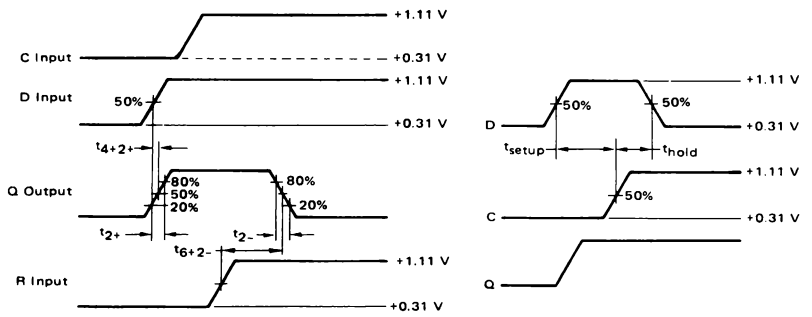
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10132P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Current	I_E	8	–	–	–	44	55	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	–	–	–	290	–	–	μAdc	4	–	–	–	8	1,16
		5	–	–	–	–	290	–	–		5	–	–	–		
		6	–	–	–	–	390	–	–		6	–	–	–		
		7	–	–	–	–	290	–	–		7	–	–	–		
		10	–	–	–	–	265	–	–		10	–	–	–		
		11	–	–	–	–	265	–	–		11	–	–	–		
	$I_{in\ L}$	4*	–	–	0.50	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	7,9,10	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,11	7,9,10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	7,9,10	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,11	7,9,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	7,9,10	4	–	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	11	7,9,10	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	7,9,10	4	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	11	7,9,10	5	–	8	1,16
Switching Times (50-ohm load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data	t_{4+2+}	2	–	–	1.0	–	3.3	–		ns	–	7,9,10	4	2	8	1,16
Reset	t_{6+2-}		–		1.0	–	3.8	–	–		7	–	6			
Clock	t_{7-2+}		–	–	1.0	–	5.7	–	–		4	–	7			
Select	t_{11+2+}		–	–	1.0	–	4.6	–	–		5	7	11			
Setup Time Data	t_{setup}	2	–	–	2.5	–	–	–	–	ns	–	11	4,10	2	8	1,16
Select	t_{setup}	2	–	–	3.5	–	–	–	–	ns	5	7	10,11	2	8	1,16
Hold Time Data	t_{hold}	2	–	–	1.5	–	–	–	–	ns	–	11	4,10	2	8	1,16
Select	t_{hold}	2	–	–	1.0	–	–	–	–	ns	5	7	10,11	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.5	–	3.5	–	–	ns	–	7,9,10	4	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	–	–	1.5	–	3.5	–	–	ns	–	7,9,10	4	2	8	1,16

*All other inputs tested in the same manner.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

APPLICATION INFORMATION

A typical application of the MC10132 is temporary storage in a minicomputer. The arithmetic section of a minicomputer might have a configuration similar to that illustrated in Figure 1. Data may be entered into the "B" register from either the register file or the input bus, requiring a multiplexed input to the register.

Figure 2 shows the MC10132 as the elements in the "B" register. Eight packages of the dual latch is necessary to construct a 16-bit register. Note that reset is available on the MC10132 if this capability is required.

FIGURE 1

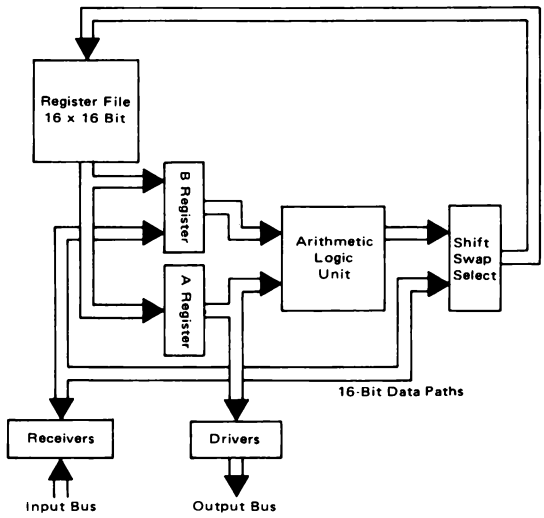
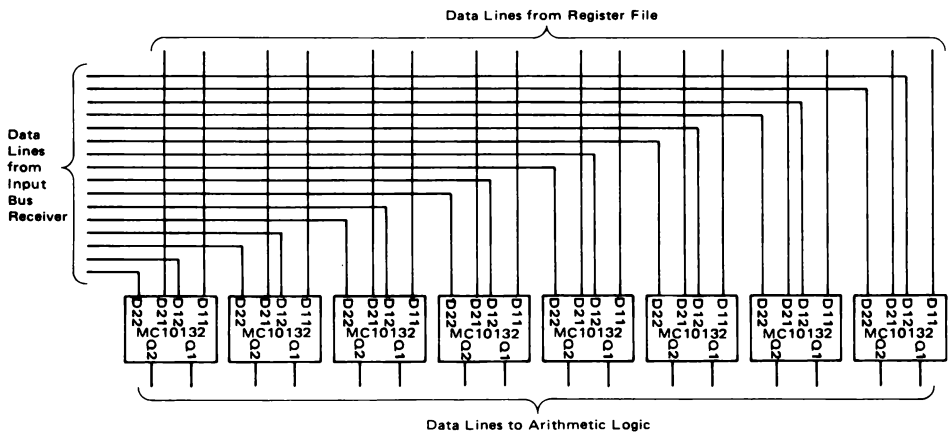


FIGURE 2



MC10133

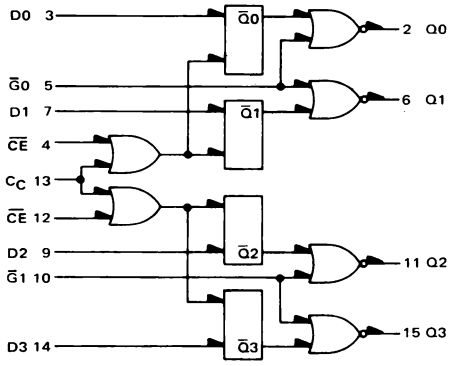
TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

ϕ = Don't Care
$C = C_C + C_E$

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

The MC10133 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on negative going transition of the clock.

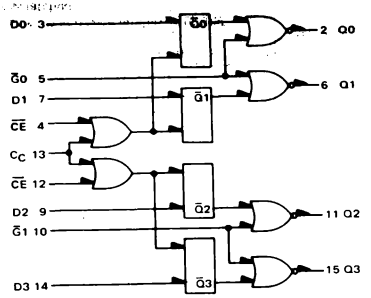


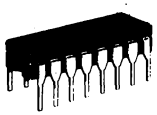
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10133L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	60	75	–	–	mAdc	–	13	–	–	8	1,16
Input Current	I_{inH}	3	–	–	–	–	245	–	–	μAdc	3	–	–	–	8	1,16
		4	–	–	–	–	265	–	–	↓	4	–	–	–	↓	↓
		5	–	–	–	–	350	–	–		5	–	–	–		
		13	–	–	–	–	350	–	–		13	–	–	–		
	I_{inL}	3	–	–	0.5	–	–	–	–	μAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,4	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	13	3	–	–	8	1,16
		2	↓	↓	↓		↓	↓	↓	↓	3,5,13	–	–	–	↓	↓
		2				–					4	3	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	3,4	–	–	5	8	1,16
		2	↓	–	↓	–	–	↓	–	↓	4	–	3	–	↓	↓
		2		–		–	–		–		3,4	–	–	–		
		2†		–		–	–		–		3	–	–	–		
		2††		–		–	–		–		–	–	–	–		
		2††		–		–	–		–		–	–	–	4		
		2		–		–	–		–		3	–	4	–		
		2	↓	–	↓	–	–	↓	–	↓	3	–	13	–	↓	↓
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	3,4	–	5	–	8	1,16
		2	–	↓	–	–	↓	–	↓	↓	4	–	–	3	↓	↓
		2	–		–	–		–			4	–	–	–		
		2†	–		–	–		–			–	–	–	–		
		2††	–		–	–		–			3	–	–	–		
		2††	–	↓	–	–	↓	–	↓	↓	3	–	–	13	↓	↓
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	1.0	5.6	1.0	–	5.4	1.1	5.9	ns	4	–	3	2	8	1,16
	t_{4+2+}	2	1.0	5.4	↓	–	5.4	1.2	6.0	↓	3 *	–	4	2	↓	↓
	t_{5-2+}	2	1.0	3.2		–	3.1	1.0	3.4		–	–	5	2		
	t_{Setup}	3	–	–	2.5	–	–	–	–		–	–	3	2		
	t_{Hold}	3	–	–	1.5	–	–	–	–		–	–	3	2		
Rise Time (20% to 80%)	t_{2+}	2	1.0	3.6	1.1	–	3.5	1.1	3.8		4	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	1.0	3.6	1.1	–	3.5	1.1	3.8	↓	4	–	3	2	↓	↓

†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

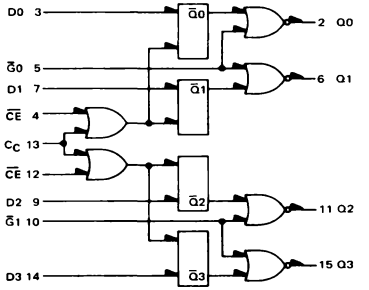
††Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

V_{IH} max
V_{IL} min

*Latch set to zero state before test.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.



P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10133P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	60	75	–	–	mAdc	–	13	–	–	8	1,16
Input Current	I_{inH}	3	–	–	–	–	245	–	–	μAdc	3	–	–	–	8	1,16
		4	–	–	–	–	265	–	–		4	–	–	–		
		5	–	–	–	–	350	–	–		5	–	–	–		
		13	–	–	–	–	350	–	–		13	–	–	–		
	I_{inL}	3	–	–	0.5	–	–	–	–	μAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,4	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	13	3	–	–	8	1,16
		2				–					3,5,13	–	–	–		
		2				–					4	3	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	3,4	–	–	5	8	1,16
		2		–		–	–		–		4	–	3	–		
		2		–		–	–		–		3,4	–	–	–		
		2†		–		–	–		–		3	–		–		
		2††		–		–					–	–	–	–		
		2††		–		–	–		–		–	–	–	4		
		2		–		–	–				3	–	4	–		
		2		–		–	–		–		3	–	13	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	3,4	–	–	5	8	1,16
		2	–		–			–			4	–		3		
		2	–		–	–		–			4	–	–	–		
		2†	–		–	–		–			–	–	–	–		
		2††	–		–	–					3	–	–	–		
		2††	–		–	–					3	–	–	13		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–	–	1.0	–	5.4	–	–	ns	4	–	3	2	8	1,16
	t_{4+2+}	2	–			–	5.4	–	–		3 *	–	4	2		
	t_{5-2+}	2	–	–		–	3.1	–	–		–	–	5	2		
	t_{Setup}	3	–	–	2.5	–	–	–	–		–	–	3	2		
	t_{Hold}	3	–	–	1.5	–	–	–	–		–	–	3	2		
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.1	–	3.5	–	–		4	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	–	–	1.1	–	3.5	–	–		4	–	3	2		

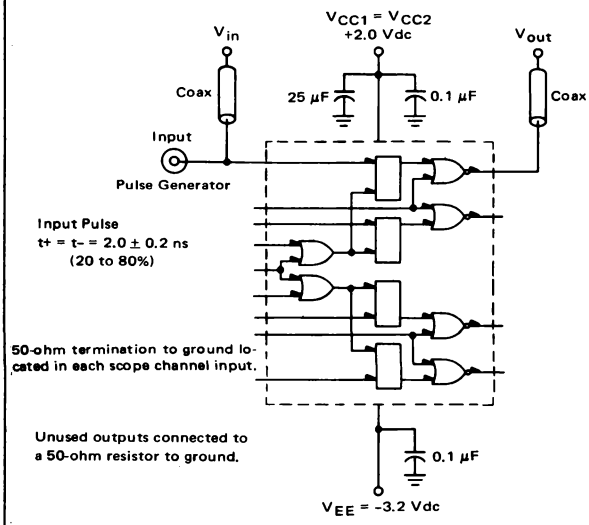
†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

V_{IH} max
V_{IL} min

*Latch set to zero state before test.

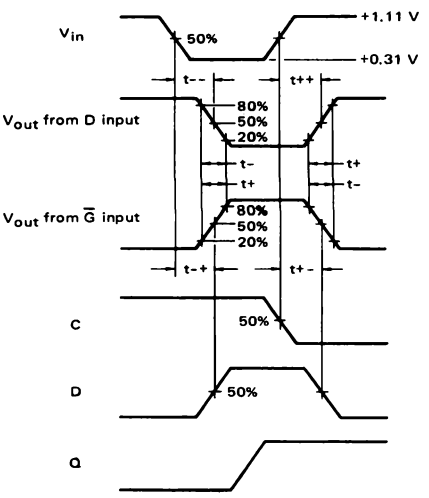
††Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

PROPAGATION DELAY



t_{Setup} is minimum time before the negative transition of the clock pulse (C) that information must be present at the data input (D).

t_{Hold} is the minimum time after the negative transition of the clock pulse (C) that information must remain unchanged at the data input (D).

APPLICATION INFORMATION

The MC10133 device consists of four bistable latch circuits with D type inputs and gated Q outputs. When the clock is high the outputs will follow the D inputs. The latch will store the data on the falling edge of the clock. The outputs are gated when the output enable is low. All four latches may be clocked at one time with the common clock, or each half may be clocked separately with its clock. This device is useful as a temporary storage element in high speed central processors, accumulators, register files, digital communication systems, instrumentation and test equipment.

DUAL MULTIPLEXER
WITH LATCH

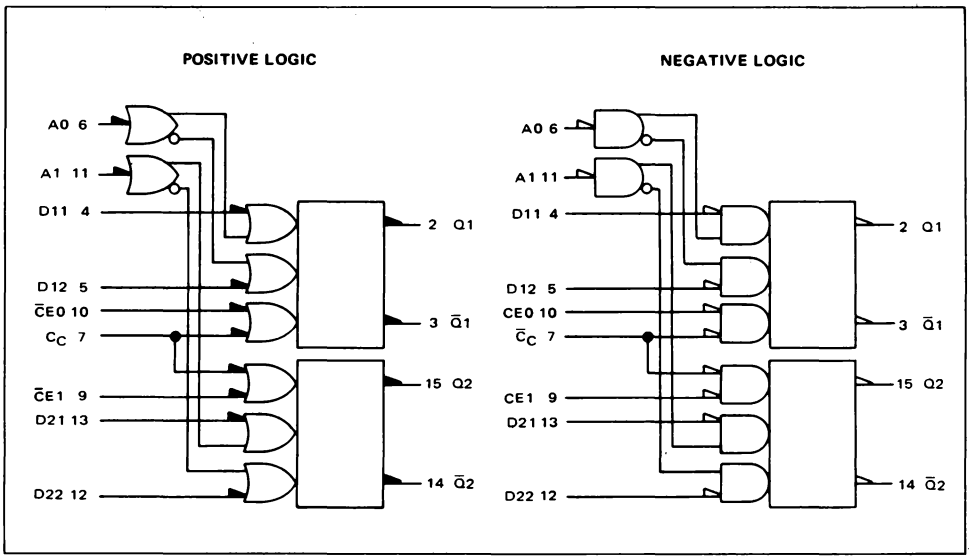
MC10134

The MC10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

Output rise and fall times have been optimized to provide relaxation of system layout and design criteria.



TRUTH TABLE

C	A0	D11	D12	Q_{n+1}
L	L	L	ϕ	L
L	L	H	ϕ	H
L	H	ϕ	L	L
L	H	ϕ	H	H
H	ϕ	ϕ	ϕ	Q_n

ϕ = Don't Care
$C = \overline{CE} + C_C$

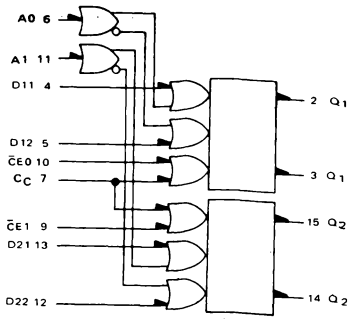
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

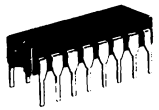
P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one latch. The other latches are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

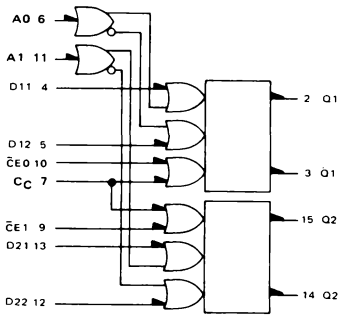
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.625	-1.035	-1.440	-5.2

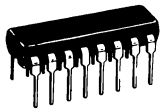
Characteristic	Symbol	Pin Under Test	MC10134L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	–	–	290	–	–	μAdc	4	–	–	–	8	1,16
		5	–	–	–	290	–	–		5	–	–	–		
		6	–	–	–	265	–	–		6	–	–	–		
		7	–	–	–	290	–	–		7	–	–	–		
		10	–	–	–	265	–	–		10	–	–	–		
	$I_{in\ L}$	4*	–	–	0.50	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	4	6,7,10,	–	–	8	1,16
		2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	5,6	7,10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	–	4,6,7,10,	–	–	8	1,16
		2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	6	5,7,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	6,7,10	4	–	8	1,16
		2	-1.080	–	-0.980	–	-0.910	–	Vdc	6	7,10	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	6,7,10	–	4	8	1,16
		2	–	-1.655	–	-1.630	–	-1.595	Vdc	6	7,10	–	5	8	1,16
Switching Times (50-ohm load)					Min	Max				+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data	t_{4+2+}	2	–	–	1.0	3.3	–	–	ns	–	6,7,10	4	2	8	1,16
Clock	t_{10-2+}		–	–	1.0	5.7	–	–		4	7	10			
Select	t_{6+2+}		–	–	1.0	4.6	–	–		5	7,10	6			
Setup Time Data	t_{setup}	2	–	–	2.5	–	–	–	ns	–	6,7	4,10	2	8	1,16
Select	t_{setup}	2	–	–	3.5	–	–	–	ns	5	7,11	6,10	2	8	1,16
Hold Time Data	t_{hold}	2	–	–	1.5	–	–	–	ns	–	6,7	4,10	2	8	1,16
Select	t_{hold}	2	–	–	1.0	–	–	–	ns	5	7,11	6,10	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.5	3.5	–	–	ns	–	6,7,10	4	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	–	–	1.5	3.5	–	–	ns	–	6,7,10	4	2	8	1,16

*All other inputs tested in the same manner.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one latch. The other latches are tested in the same manner.





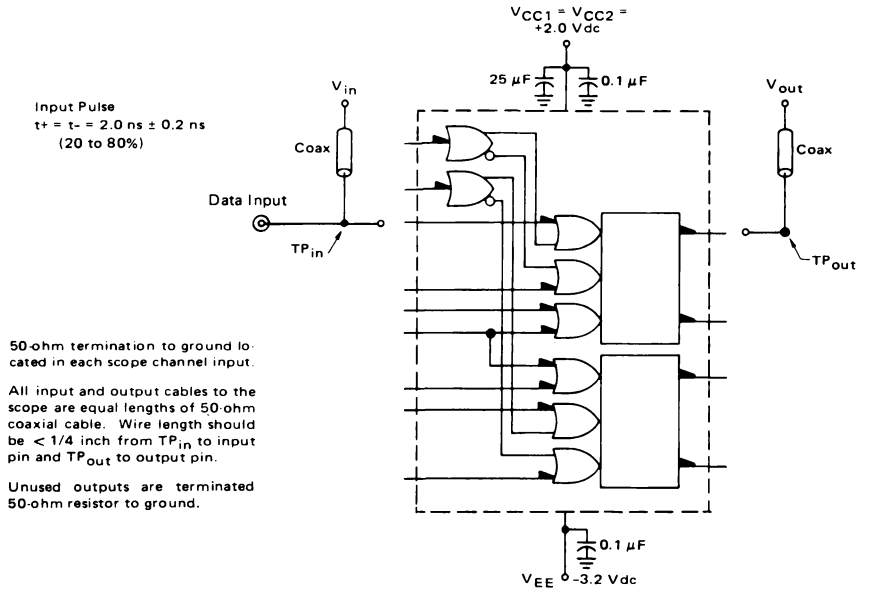
P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.625	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10134P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	–	–	290	–	–	μAdc	4	–	–	–	8	1,16
		5	–	–	–	290	–	–		5	–	–	–		
		6	–	–	–	265	–	–		6	–	–	–		
		7	–	–	–	290	–	–		7	–	–	–		
		10	–	–	–	265	–	–		10	–	–	–		
	$I_{in\ L}$	4*	–	–	0.50	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	4	6,7,10,	–	–	8	1,16
		2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	5,6	7,10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	–	4,6,7,10,	–	–	8	1,16
		2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	6	5,7,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	6,7,10	4	–	8	1,16
		2	-1.080	–	-0.980	–	-0.910	–	Vdc	6	7,10	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	6,7,10	–	4	8	1,16
		2	–	-1.655	–	-1.630	–	-1.595	Vdc	6	7,10	–	5	8	1,16
Switching Times (50-ohm load)					Min	Max				+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data	t_{4+2+}	2	–	–	1.0	3.3	–	–	ns	–	6,7,10	4	2	8	1,16
Clock	t_{10-2+}		–	–	1.0	5.7	–	–		4	7	10			
Select	t_{6+2+}		–	–	1.0	4.6	–	–		5	7,10	6			
Setup Time Data	t_{setup}	2	–	–	2.5	–	–	–	ns	–	6,7	4,10	2	8	1,16
Select	t_{setup}	2	–	–	3.5	–	–	–	ns	5	7,11	6,10	2	8	1,16
Hold Time Data	t_{hold}	2	–	–	1.5	–	–	–	ns	–	6,7	4,10	2	8	1,16
Select	t_{hold}	2	–	–	1.0	–	–	–	ns	5	7,11	6,10	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.5	3.5	–	–	ns	–	6,7,10	4	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	–	–	1.5	3.5	–	–	ns	–	6,7,10	4	2	8	1,16

*All other inputs tested in the same manner.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

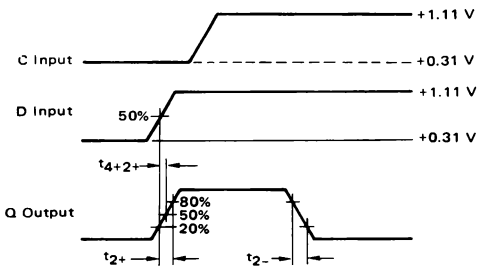


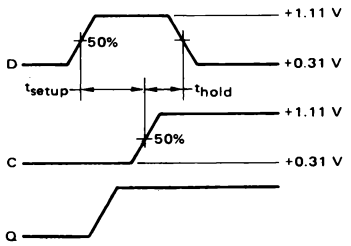
Input Pulse
t+ = t- = 2.0 ns ± 0.2 ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are terminated 50-ohm resistor to ground.





NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

APPLICATION INFORMATION

A typical application of the MC10134 is temporary storage in a minicomputer. The arithmetic section of a minicomputer might have a configuration similar to that illustrated in Figure 1. Data may be entered into the "B" register from either the register file or the input bus, requiring a multiplexed input to the register.

Figure 2 shows the MC10134 as the elements in the "B" register. Eight dual latch packages are necessary to construct a 16-bit register.

FIGURE 1

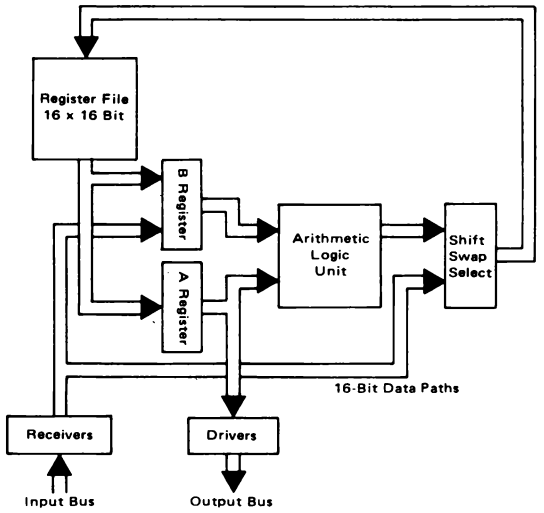
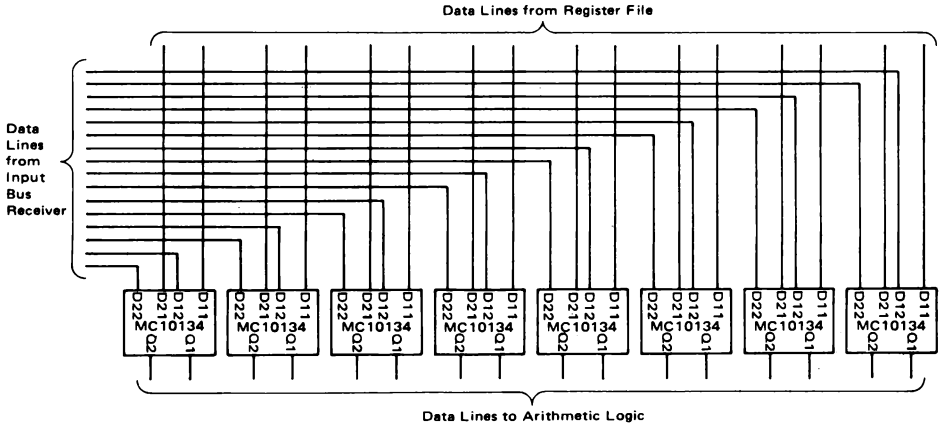
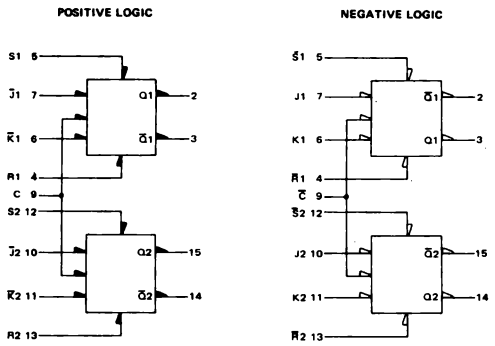


FIGURE 2



MC10135



R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCK J-K TRUTH TABLE*

$\bar{J}$	$\bar{K}$	Q_{n+1}
L	L	$\bar{Q}_n$
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\bar{J}$-$\bar{K}$ input condition present.

The MC10135 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate $\bar{J}$-$\bar{K}$ inputs. When the clock is static, the $\bar{J}$-$\bar{K}$ inputs do not effect the output.

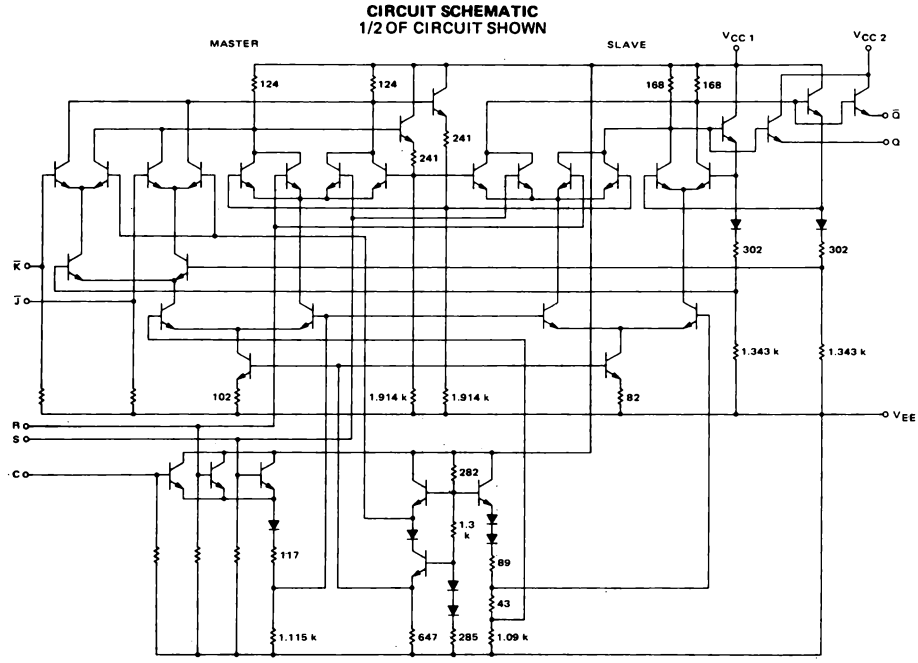
The output states of the flip-flop change on the positive transition of the clock.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 280 mW typ/pkg (No Load)
f_{Tog} = 140 MHz typ

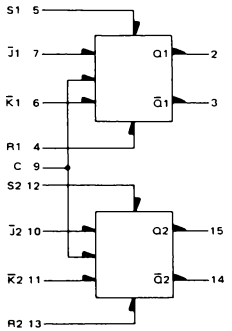
CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN

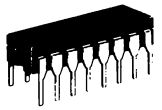


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES Vdc ± 1% $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10135L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	54	68	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	6,7,9,10,11	–	–	–	–	265	–	–	μAdc	①	–	–	–	8	1,16
		4,5,12,13	–	–	–	–	390	–	–	μAdc	①	–	–	–	8	1,16
Input Leakage Current	$I_{in\ L}$	4,5,6,7,9,	–	–	0.5	–	–	–	–	μAdc	–	②	–	–	8	1,16
		10,11,12,13	–	–	0.5	–	–	–	–	μAdc	–	②	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
		2 ③	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,16
		3 ③	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		2 ④	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,16
		3 ④	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	–	–	8	1,16
Switching Times													**Pulse In**	**Pulse Out**	**-3.2 Vdc**	**+2.0 Vdc**
Clock Input																
Propagation Delay	t_{9+2+}	2	1.0	5.0	1.0	3.0	4.5	1.0	4.6	ns	–	–	9	2	8	1,16
	t_{9+2-}	2	↓	↓	1.0	3.0	↓	↓	↓		–	–	9	2	↓	↓
Rise Time (20 to 80%)	$t_{2+,t3+}$	2,3	1.1	4.8	1.1	2.0	↓	1.1	4.7	↓	–	–	9	2,3	↓	↓
Fall Time (20 to 80%)	$t_{2-,t3-}$	2,3	↓	↓	1.1	2.0	↓	↓	↓	↓	–	–	9	2,3	↓	↓
Set Input																
Propagation Delay	t_{5+2+}	2	1.2	5.6	1.0	3.0	5.0	1.0	5.2	ns	–	–	5	2	8	1,16
	t_{12+15+}	15	↓	↓	↓	↓	↓	↓	↓	↓	–	–	12	15	↓	↓
	t_{5+3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	5	3	↓	↓
	t_{12+14-}	14	↓	↓	↓	↓	↓	↓	↓	↓	–	–	12	14	↓	↓
Reset Input																
Propagation Delay	t_{4+2-}	2	–	–	1.0	3.0	5.0	–	–	ns	–	–	4	2	8	1,16
	t_{4+3+}	3	–	–	↓	↓	↓	–	–	↓	–	–	4	3	↓	↓
	t_{13+15-}	15	–	–	↓	↓	↓	–	–	↓	–	–	13	15	↓	↓
	t_{13+14+}	14	–	–	↓	↓	↓	–	–	↓	–	–	13	14	↓	↓
Setup Time	t_{setup}	7	–	–	2.5		–	–	–	ns	–	–	6,9 ⑤	2	8	1,16
Hold Time	t_{hold}	7	–	–	1.5		–	–	–	ns	–	–	6,9 ⑤	2	8	1,16
Toggle Frequency	f_{Tog}	2	–	–	125	140	–	–	–	MHz	–	–	9	2	9	1,16

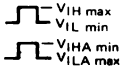
NOTES:

① Individually test each input; apply $V_{IH\ max}$ to pin under test.

② Individually test each input; apply $V_{IL\ min}$ to pin under test.

③ Output level to be measured after a clock pulse has been applied to the C input (pin 9)

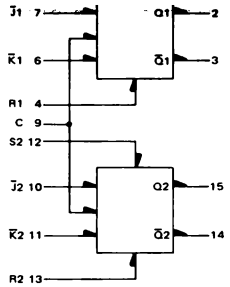
④ Output level to be measured after a clock pulse has been applied to the C input (pin 9)



⑤ See Figure 2 for timing test diagram.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.



P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES Vdc ± 1% $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10135P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	54	68	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	6,7,9,10,11	–	–	–	–	265	–	–	μAdc	①	–	–	–	8	1,16
		4,5,12,13	–	–	–	–	390	–	–	μAdc	①	–	–	–	8	1,16
Input Leakage Current	$I_{in\ L}$	4,5,6,7,9,	–	–	0.5	–	–	–	–	μAdc	–	②	–	–	8	1,16
		10,11,12,13	–	–	0.5	–	–	–	–	μAdc	–	②	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
		2 ③	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,16
		3 ③	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		2 ④	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,16
		3 ④	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	–	–	8	1,16
Switching Times													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input																
Propagation Delay	t_{9+2+}	2	–	–	1.0	3.0	4.5	–	–	ns	–	–	9	2	8	1,16
	t_{9+2-}	2	–	–	1.0	3.0	↓	–	–	↓	–	–	9	2	↓	↓
Rise Time (20 to 80%)	$t_{2+,t3+}$	2,3	–	–	1.1	2.0	↓	–	–	↓	–	–	9	2,3	↓	↓
Fall Time (20 to 80%)	$t_{2-,t3-}$	2,3	–	–	1.1	2.0	↓	–	–	↓	–	–	9	2,3	↓	↓
Set Input																
Propagation Delay	t_{5+2+}	2	–	–	1.0	3.0	5.0	–	–	ns	–	–	5	2	8	1,16
	t_{12+15+}	15	–	–	↓	↓	↓	–	–	↓	–	–	12	15	↓	↓
	t_{5+3-}	3	–	–	↓	↓	↓	–	–	↓	–	–	5	3	↓	↓
	t_{12+14-}	14	–	–	↓	↓	↓	–	–	↓	–	–	12	14	↓	↓
Reset Input																
Propagation Delay	t_{4+2-}	2	–	–	1.0	3.0	5.0	–	-	ns	–	–	4	2	8	1,16
	t_{4+3+}	3	–	–	↓	↓	↓	–	–	↓	–	–	4	3	↓	↓
	t_{13+15-}	15	–	–	↓	↓	↓	–	–	↓	–	–	13	15	↓	↓
	t_{13+14+}	14	–	–	↓	↓	↓	–	–	↓	–	–	13	14	↓	↓
Setup Time	t_{setup}	7	–	–	2.5	–	–	–	–	ns	–	–	6,9 ⑤	2	8	1,16
Hold Time	t_{hold}	7	–	–	1.5	–	–	–	–	ns	–	–	6,9 ⑤	2	8	1,16
Toggle Frequency	f_{Tog}	2	–	–	125	140	–	–	–	MHz	–	–	9	2	9	1,16

NOTES:

① Individually test each input; apply $V_{IH\ max}$ to pin under test.

② Individually test each input; apply $V_{IL\ min}$ to pin under test.

③ Output level to be measured after a clock pulse has been applied to the C input (pin 9) $V_{IH\ max}$ / $V_{IL\ min}$

④ Output level to be measured after a clock pulse has been applied to the C input (pin 9) $V_{IHA\ min}$ / $V_{ILA\ max}$

⑤ See Figure 2 for timing test diagram.

FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT

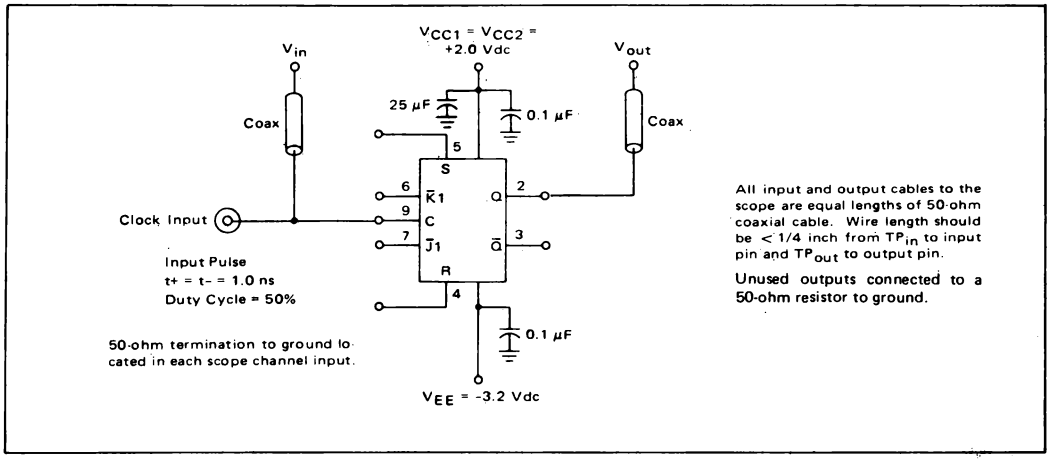
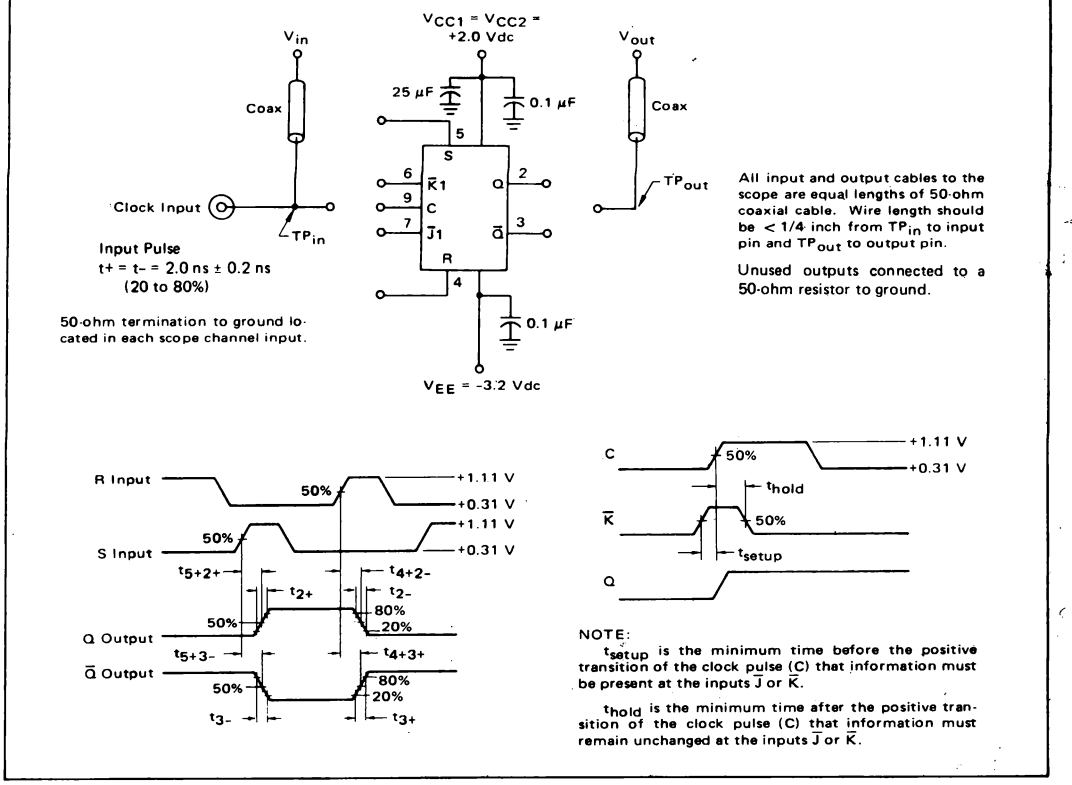


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the inputs $\overline{J}$ or $\overline{K}$.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the inputs $\overline{J}$ or $\overline{K}$.

UNIVERSAL HEXADECIMAL COUNTER

MC10136

The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. This binary counter is useful in high speed central processors and peripheral controllers, minicomputers, high speed digital communications equipment and instrumentation. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

A prescaler can be constructed using the MC10136 in conjunction with the MC10231 which will operate at over 200 MHz input frequency. A 500 MHz prescaler is possible using an MC1690 500 MHz D Flip-Flop, an MC1670 300 MHz D Flip-Flop, and the MC10136.

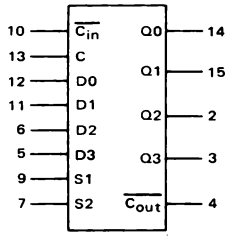
SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H

ϕ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

FUNCTION SELECT TABLE

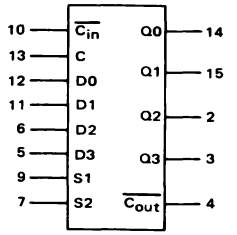
S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

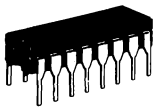
P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one output. The other outputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10136L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	120	150	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	$I_{in\ H}$	5,6,11,12	–	–	–	–	220	–	–	μAdc	5,6,11,12	–	–	–	8	1, 16
		7	–	–	–	–	265	–	–	↓	7	–	–	–	↓	↓
		9,10	–	–	–	–	245	–	–		9,10	–	–	–		
		13	–	–	–	–	290	–	–		13	–	–	–		
	$I_{in\ L}$	All	–	–	0.5	–	–	–	–	μAdc	–	①	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	14 ②	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	7, 9	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	14 ②	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	7, 9	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	14 ②	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	7, 9	12	–	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	14 ②	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	7, 9	–	12	8	1, 16
Switching Times (50-ohm Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Input	t_{13+14+}	14	0.8	4.8	1.0	3.3	4.5	1.4	5.0	ns	12	–	13	14	8	1, 16
	t_{13+14-}	14	0.8	4.8	1.0	3.3	4.5	1.4	5.0	↓	–	–	↓	14	↓	↓
	t_{13+4+}	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5		7	–		4		
	t_{13+4-}	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5		7	–		4		
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$	t_{10-4-}	4 ③	1.6	7.4	1.6	5.0	6.9	1.9	7.5		7	13	10	4		
	t_{10+4+}	4	1.6	7.4	1.6	5.0	6.9	1.9	7.5		7	13	10	4		
Set Up Time																
Data Inputs	t_{12+13+}	14	–	–	3.5	–	–	–	–		–	7, 9	12, 13	14		
	t_{12-13+}	14	–	–	3.5	–	–	–	–		–	7, 9	12, 13	↓		
Select Inputs	t_{9+13+}	14	–	–	7.5	–	–	–			–	–	9, 13			
	t_{7+13+}	14	–	–	7.5	–	–	–	–		–	–	7, 13			
$\overline{\text{Carry In}}$ Input	t_{10-13+}	14	–	–	3.7	–	–	–	–		7	9	10, 13	14		
	t_{13+10+}	14	–	–	-1.0	–	–	–			7	–	10, 13	14		
Hold Time																
Data Inputs	t_{13+12+}	14	–	–	-1.0	–	–	–	–		–	7, 9	12, 13	14		
	t_{13+12-}	14	–	–	-1.0	–	–	–	–		–	7, 9	12, 13	↓		
Select Inputs	t_{13+9+}	14	–	–	-2.5	–	–		–		–	–	9, 13			
	t_{13+7+}	14	–	–	-2.5	–	–	–	–		–	–	7, 13			
$\overline{\text{Carry In}}$ Input	t_{13+10-}	14	–	–	-1.6	–	–	–	–		7	9	10, 13			
	t_{10+13+}	14		–	3.1	–	–	–	–		7	9	10, 13			
Counting Frequency	$f_{countup}$	14	125	–	125	150	–	125	–	MHz	7	–	13			
	$f_{countdown}$	14	125	–	125	150	–	125	–	MHz	9	–	↓	↓		
Rise Time (20% to 80%)	t_{4+}	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	ns	7	–		4		
	t_{14+}	14	↓	↓	↓	2.0	↓	↓	↓	↓	↓	–		14		
Fall Time (20% to 80%)	t_{4-}	4				2.0						–		4		
	t_{14-}	14				2.0						–		14		

① Individually apply $V_{IL\ min}$ to pin under test. ② Measure output after clock pulse V_{IL} ⌐ V_{IH} appears at clock input (pin 13) ③ Before test set all Q outputs to a logic high.

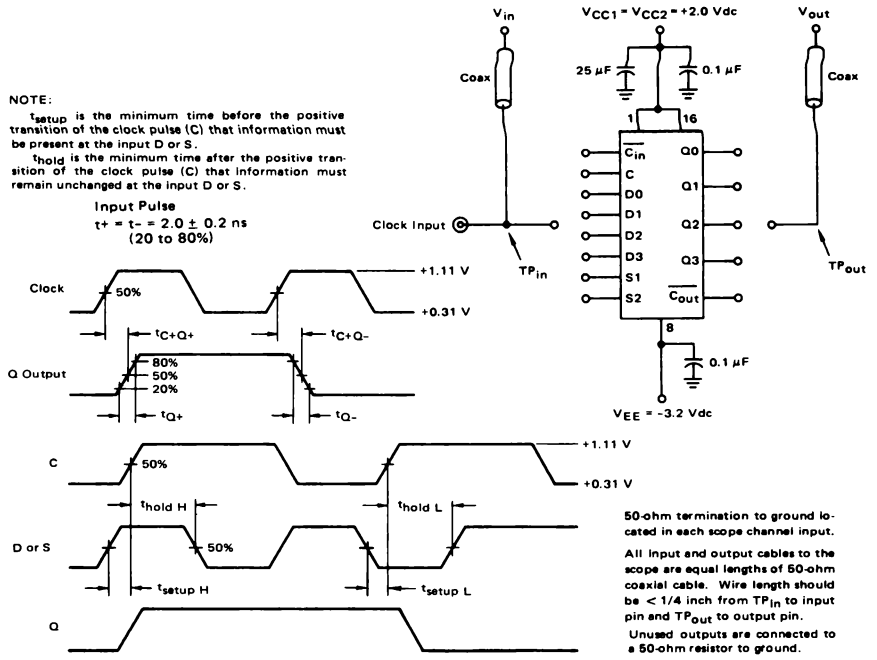
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

Input Pulse
$t+ = t- = 2.0 \pm 0.2$ ns
(20 to 80%)



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

SET UP AND HOLD TIMES

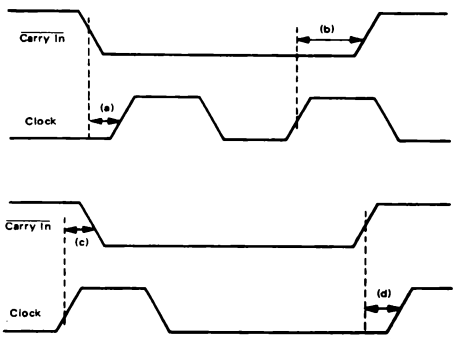
(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

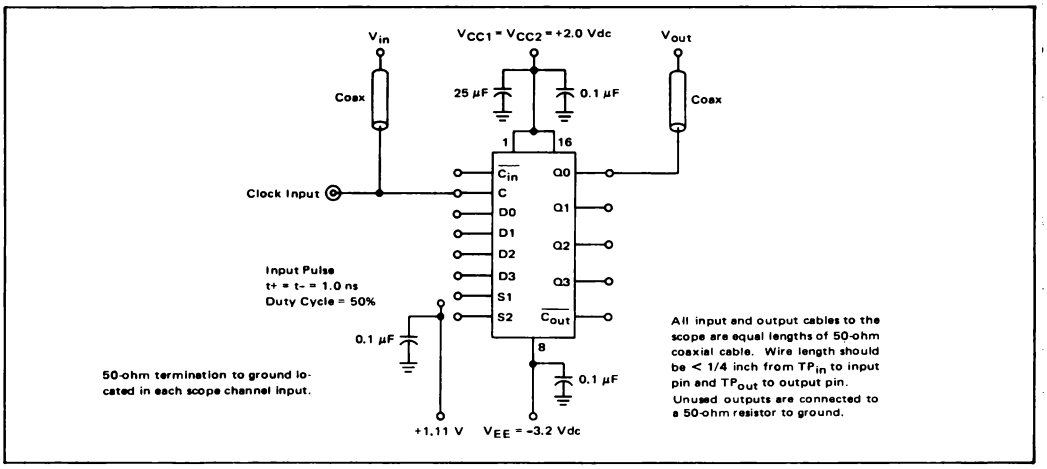
(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

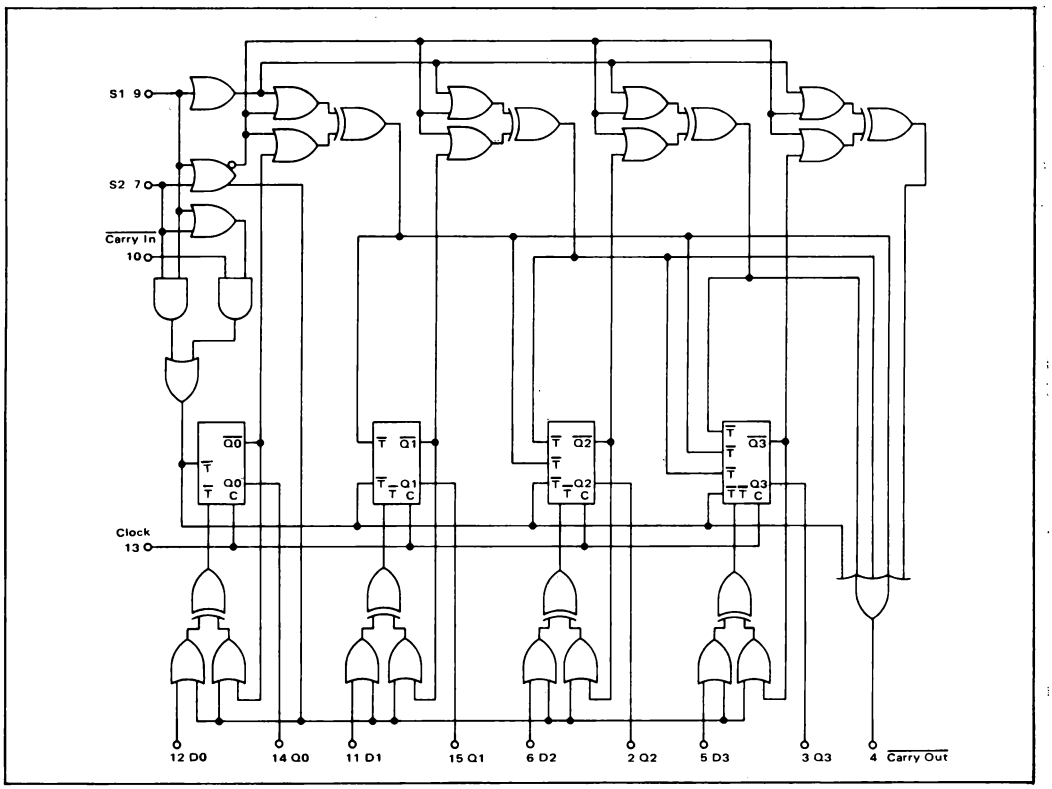
(b) and (c) may be negative numbers.



COUNT FREQUENCY TEST CIRCUIT



UNIVERSAL BINARY UP/DOWN COUNTER



APPLICATIONS INFORMATION

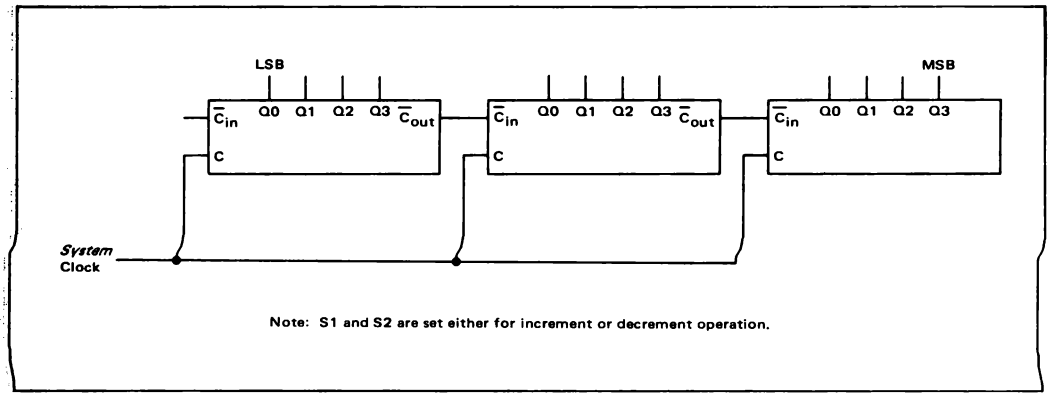
To provide more than four bits of counting capability several MC10136 counters may be cascaded. The $\overline{\text{Carry In}}$ input overrides the clock when the counter is either in the increment mode or the decrement mode of operation. This input allows several devices to be cascaded in a fully synchronous multistage counter as illustrated in Figure 1. The carry is advanced between stages as shown with no external gating. The $\overline{\text{Carry In}}$ of the first device may be left open. The system clock is common to all devices.

The various operational modes of the counter make it useful for a wide variety of applications. If used with MECL III devices, prescalers with input toggle frequencies in excess of 300 MHz are possible. Figure 2 shows such a prescaler using the MC10136 and MC1670. Use of the MC10231 in place of the MC1670 permits 200 MHz operation.

The MC10136 may also be used as a programmable counter. The configuration of Figure 3 requires no additional gates, although maximum frequency is limited to about 50 MHz. The divider modulus is equal to the program input plus one (M = N + 1), there fore, the counter will divide by a modulus varying from 1 to 16.

A second programmable configuration is also illustrated in Figure 4. A pulse swallowing technique is used to speed the counter operation up to 110 MHz typically. The divider modulus for this figure is equal to the program input (M = N). The minimum modulus is 2 because of the pulse swallowing technique, and the modulus may vary from 2 to 15. This programmable configuration requires an additional gate, such as ½MC10109 and a flip-flop such as ½MC10131.

FIGURE 1 – 12 BIT SYNCHRONOUS COUNTER



Note: S1 and S2 are set either for increment or decrement operation.

FIGURE 2 – 300 MHz PRESCALER

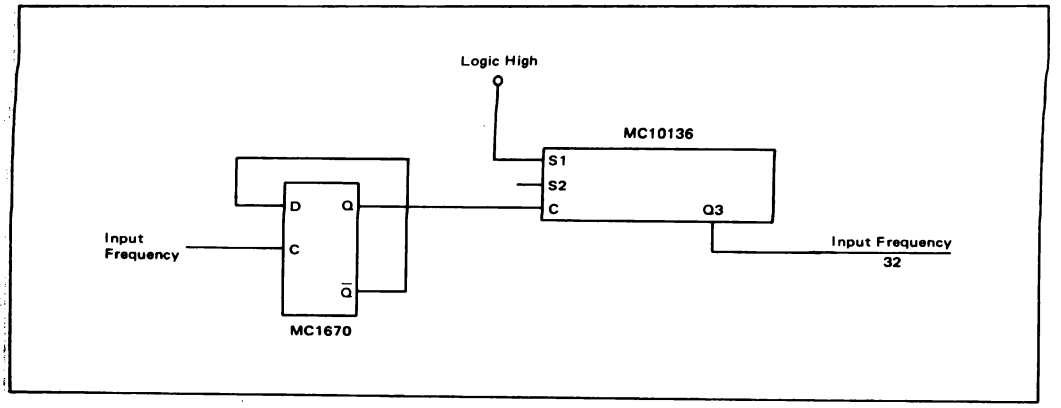
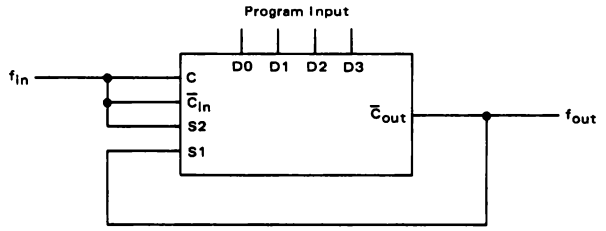


FIGURE 3 – 50 MHz PROGRAMMABLE COUNTER

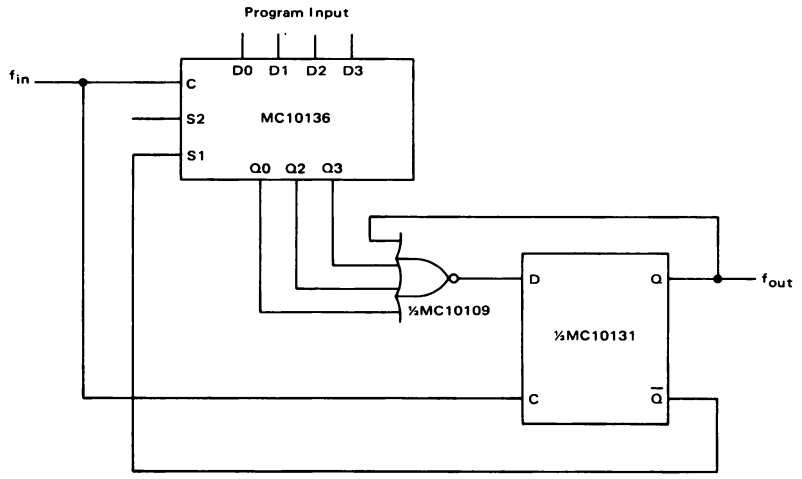


1 $f_{out} = \frac{f_{in}}{\text{Program Input} + 1}$

2 $f_{max} \cong 50$ MHz Typ.

3 Divide Ratio is from 1 to 16.

FIGURE 4 – 100 MHz PROGRAMMABLE COUNTER



1 $f_{out} = \frac{f_{in}}{\text{Program Input}}$

2 $f_{max} \cong 110$ MHz Typ.

3 Divide Ratio is from 2 to 15.

UNIVERSAL DECADE COUNTER

MC10137

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	ϕ	H	H	H	H	L	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	L	L	L	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	L	L	L	H
L	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	H	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L

ϕ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

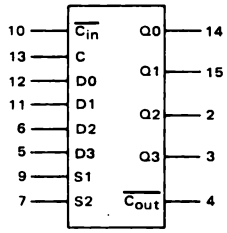
** A clock H is defined as a clock input transition from a low to a high logic level.

The MC10137 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. This decade counter is useful in high speed central processors and peripheral controllers, minicomputers, high speed digital communications equipment and instrumentation. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10137 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count. The $\overline{\text{Carry Out}}$ on the MC10137 is partially decoded from Q1 and Q2 directly, so in the preset mode the condition of the $\overline{\text{Carry Out}}$ after the Clock's positive excursion will depend on the condition of Q1 and/or Q2.

When an output is not needed, it can be left open to conserve system power. (The open emitter output will require no power if left open.) The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.

A prescaler can be constructed using the MC10137 in conjunction with the MC10231 which will operate at over 200 MHz input frequency. A 500 MHz prescaler is possible using an MC1690 500 MHz D Flip-Flop, an MC1670 300 MHz D Flip-Flop, and the MC10137.



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

FUNCTION SELECT TABLE

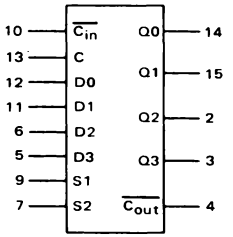
S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

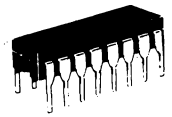
P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test Procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

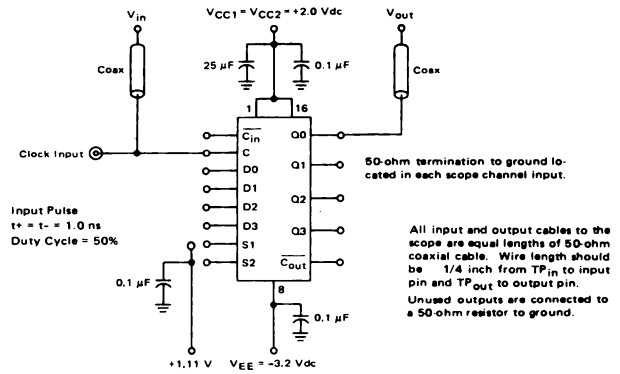
Characteristic	Symbol	Pin Under Test	MC10137L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	120	150	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{in} H	5,6,11,12	–	–	–	–	220	–	–	μAdc	5,6,11,12	–	–	–	8	1, 16
		7	–	–	–	–	265	–	–		7	–	–	–		
		9,10	–	–	–	–	245	–	–		9,10	–	–	–		
		13	–	–	–	–	290	–	–		13	–	–	–		
	I_{in} L	All	–	–	0.5	–	–	–	–	μAdc	–	①	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	14 ②	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	7, 9	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	14 ②	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	7, 9	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	14 ②	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	7, 9	12	–	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	14 ②	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	7, 9	–	12	8	1, 16
Switching Times (50-ohm Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Input	t_{13+14+}	14	0.8	4.8	1.0	3.3	4.5	1.1	5.0	ns	12	–	13	14	8	1, 16
	t_{13+14-}	14	0.8	4.8	1.0	3.3	4.5	1.1	5.0		–	–		14		
	t_{13+4+}	4	2.0	10.9	2.5	7.0	10.5	2.5	11.5		7	–		4		
	t_{13+4-}	4	2.0	10.9	2.5	7.0	10.5	2.5	11.5		7	–		4		
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$	t_{10-4-}	4 ③	1.4	7.4	1.6	5.0	6.9	1.5	7.5		7	13	10	4		
	t_{10+4+}	4	1.4	7.4	1.6	5.0	6.9	1.5	7.5		7	13	10	4		
Set Up Time																
Data Inputs	t_{12+13+}	14			3.5	–	–				–	7, 9	12, 13	14		
	t_{12-13+}	14		–	3.5	–					–	7, 9	12, 13			
Select Inputs	t_{9+13+}	14	–	–	7.5	–		–			–	–	9, 13			
	t_{7+13+}	14	–		7.5	–					–	–	7, 13			
$\overline{\text{Carry In}}$ Input	t_{10-13+}	14			3.7	–		–	–		7	9	10, 13	14		
	t_{13+10+}	14			-1.0	–					7	9	10, 13	14		
Hold Time																
Data Inputs	t_{13+12+}	14			-1.0	–		–	–		–	7, 9	12, 13	14		
	t_{13+12-}	14		–	-1.0	–			–		–	7, 9	12, 13			
Select Inputs	t_{13+9+}	14			-2.5	–					–	–	9, 13			
	t_{13+7+}	14	–		-2.5	–					–	–	7, 13			
$\overline{\text{Carry In}}$ Input	t_{13+10-}	14		–	-1.6	–					7	9	10, 13			
	t_{10+13+}	14	–	–	3.1	–					7	9	10, 13			
Counting Frequency	$f_{countup}$	14	125	–	125	150	–	125		MHz	7	–	13			
	$f_{countdown}$	14	125	–	125	150	–	125	–	MHz	9	–				
Rise Time (20% to 80%)	t_{4+}	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	ns	7	–		4		
	t_{14+}	14				2.0						–		14		
Fall Time (20% to 80%)	t_{4-}	4				2.0						–		4		
	t_{14-}	14				2.0						–		14		

① Individually apply $V_{IL\ min}$ to pin under test.

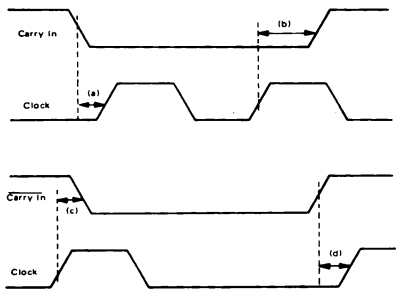
② Measure output after clock pulse V_{IL} ⌐ V_{IH} appears at clock input (pin 13)

③ Before test set Q1 and Q2 outputs to a logic low.

COUNT FREQUENCY TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

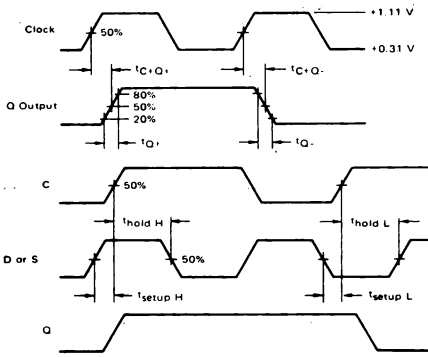
(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect on the state of the counter.

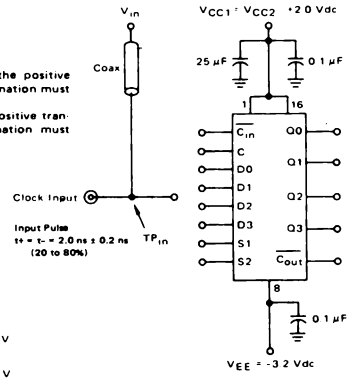
(b) and (c) may be negative numbers.

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.



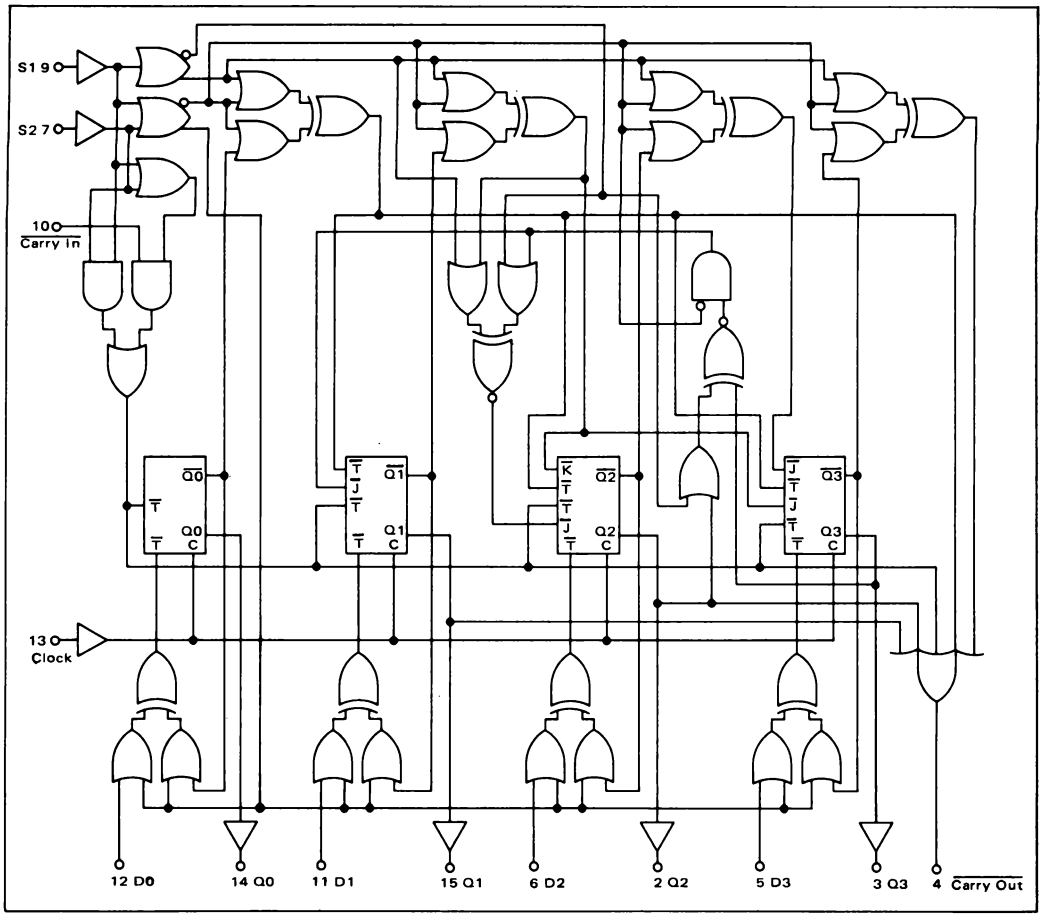


50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

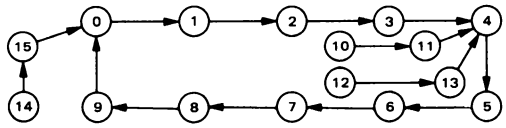
Unused outputs are connected to a 50-ohm resistor to ground.

UNIVERSAL DECADE UP/DOWN COUNTER

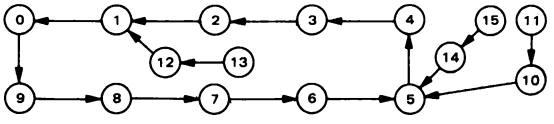


STATE DIAGRAMS

COUNT UP



COUNT DOWN



BI-QUINARY
COUNTER

MC10138

Advance Information

The MC10138 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set-reset master-slave flip-flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or reset input override the clock, allowing asynchronous "set" or "clear". Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

COUNTER TRUTH TABLES

BI-QUINARY
(Clock connected to C2
and Q3 connected to C1)

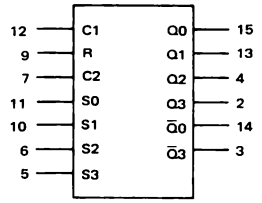
COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	L	H	H
9	L	L	H	H

BCD
(Clock connected to C1
and Q0 connected to C2)

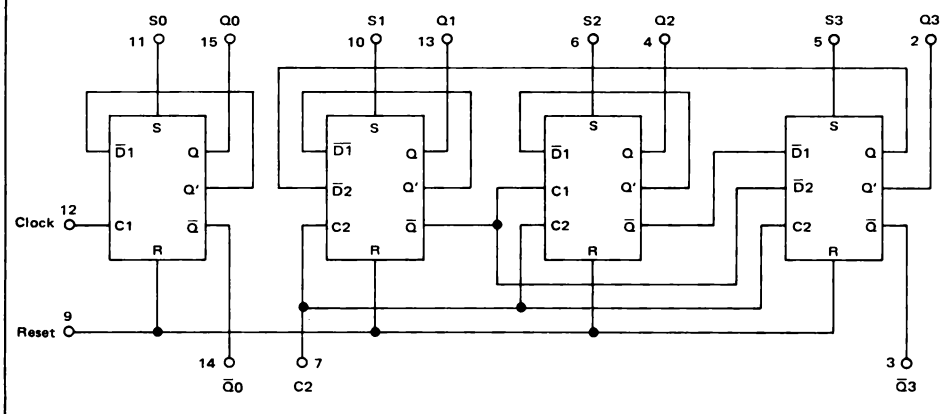
COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

P_D = 370 mW typ/pkg (No Load)
f_{tog} = 150 MHz typ

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8



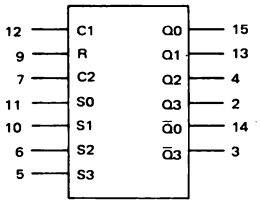
BLOCK DIAGRAM

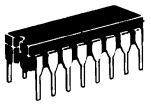


This is advance information and specifications are subject to change without notice.
See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.





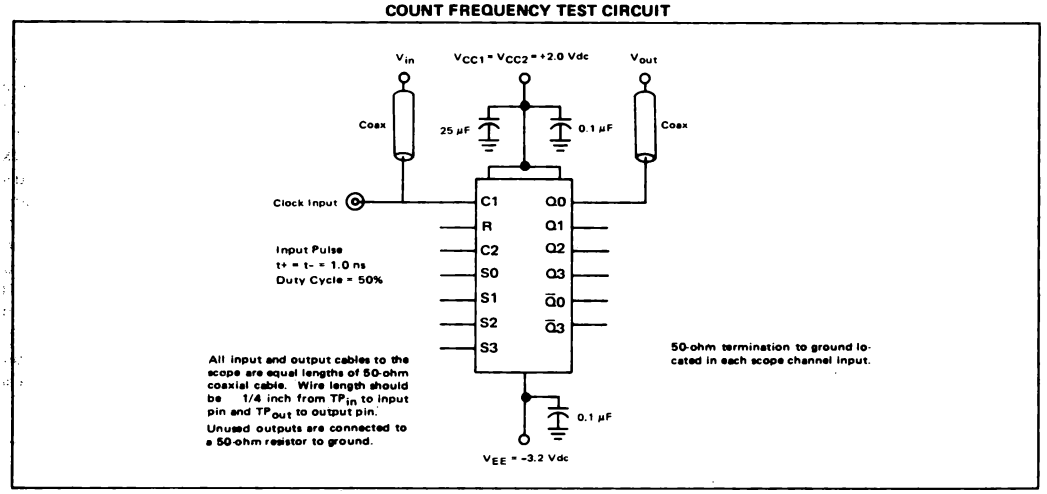
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

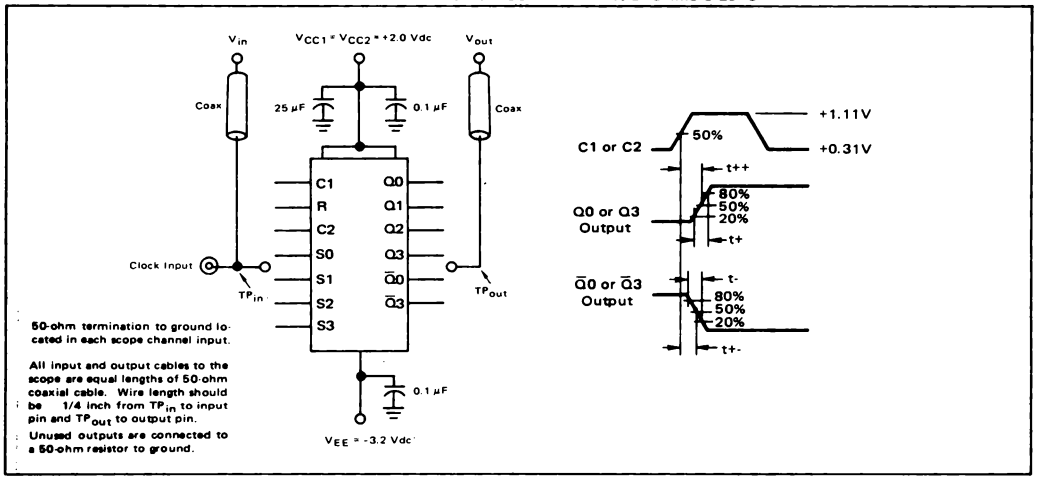
Characteristic	Symbol	Pin Under Test	MC10138L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	70	88	–	–	mAdc	9	–	–	–	8	1,16
Input Current	I_{in} H	12	–	–	–	–	220	–	–		12	–	–	–		
		5,6,10,11	–	–	–	–	245	–	–		5,6,10,11	–	–	–		
		7	–	–	–	–	290	–	–		7	–	–	–		
		9	–	–	–	–	410	–	–		9	–	–	–		
	I_{in} L	All	–	–	0.5	–		–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3,14② ①	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
		2,4,13,15 ①	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,6,10,11	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3,14 ①	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,6,10,11	–	–	–	8	1,16
		2,4,13,15 ②	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2,4,13,15 ①	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5,6,10,11	–	8	1,16
		3,14 ②	↓	–	↓	–	–	↓	–	↓	–	–	9	–	↓	↓
		13,15 ①		–		–	–		–		–	–	7,12	–		
Logic "0" Threshold Voltage	V_{OLA}	2,4,13,15 ②		-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5,6,10,11	8	1,16
		3,14 ①		↓		–	↓	–	↓	↓	–	–	–	9	↓	↓
		13,15 ②			–	–		–			–	–	–	7,12		
Switching Times (50-ohm Load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Delays 50 Ω Loads	t_{12+15+}	15				3.5		–	–	ns	–	–	12	15	8	1,16
	t_{12+14+}	14						–	–		–	–	12	14		
	t_{7+13+}	13			–			–	–		–	–	7	13		
	t_{7+4+}	4			–		–	–	–		–	–		4		
	t_{7+2+}	2	–		–		–	–	–		–	–		2		
	t_{7+3+}	3			–		–	–	–		–	–		3		
	t_{12+15-}	15	–	–	–		–	–	–		–	–	12	15		
	t_{12+14-}	14	–	–	–		–	–	–		–	–	12	14		
	t_{7+13-}	13	–	–	–		–	–	–		–	–	7	13		
	t_{7+4-}	4	–	–	–		–	–	–		–	–		4		
	t_{7+2-}	2	–	–	–		–	–	–		–	–		2		
	t_{7+3-}	3		–	–		–	–	–		–	–		3		
Set Delay	t_{11+15+}	15	–	–	–	5.2	–	–	–		–	–	11	15		
	t_{11+14-}	14	–	–	–		–	–	–		–	–	11	14		
Reset Delay	t_{9+14+}	14	–	–	–		–	–	–		–	–	9	14		
	t_{9+15-}	15	–	–	–		–	–	–		–	–	9	15		
Rise Time (20% to 80%)	t_{14+}	14	–	–	–	2.6	–	–	–	ns	–	–	11	14		
	t_{15+}	15	–	–	–		–	–	–		–	–	11	15		
Fall Time (20% to 80%)	t_{14-}	14	–	–	–			–	–		–	–	9	14		
	t_{15-}	15	–	–	–		–	–	–		–	–	9	15		
Counting Frequency	f_{count}	2	–	–	–	150	–	–	–	MHz	–	–	7	2		
		15	–	–	–	150	–	–	–	MHz	–	–	12	15		

*Individually apply V_{ILmin} to pin under test.
① Set all four flip-flops by applying pulse V_{IHmax} / V_{ILmin} to pins 5,6,10,11 prior to applying test voltage indicated.
② Reset all four flip-flops by applying pulse V_{IHmax} / V_{ILmin} to pin 9 prior to applying test voltage indicated.

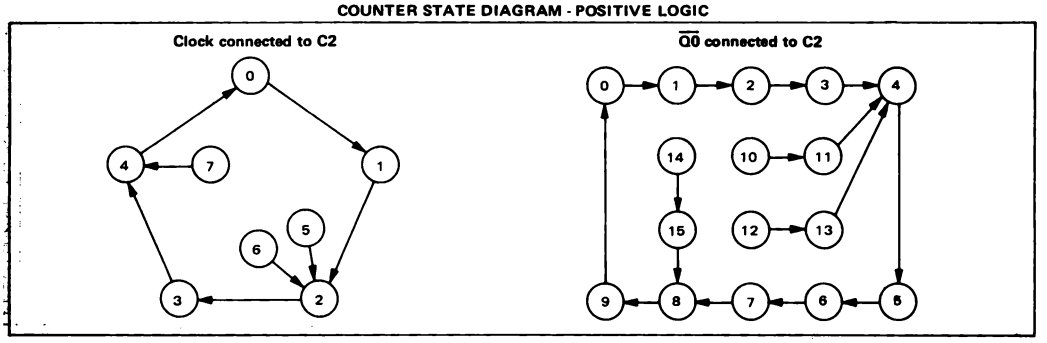
COUNT FREQUENCY TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

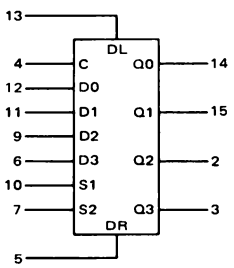


COUNTER STATE DIAGRAM - POSITIVE LOGIC



FOUR-BIT UNIVERSAL
SHIFT REGISTER

MC10141



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

The MC10141 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR). All four outputs are capable of driving 50 ohm lines.

When the register is used for serial output only, the unused emitter follower outputs can be left open.

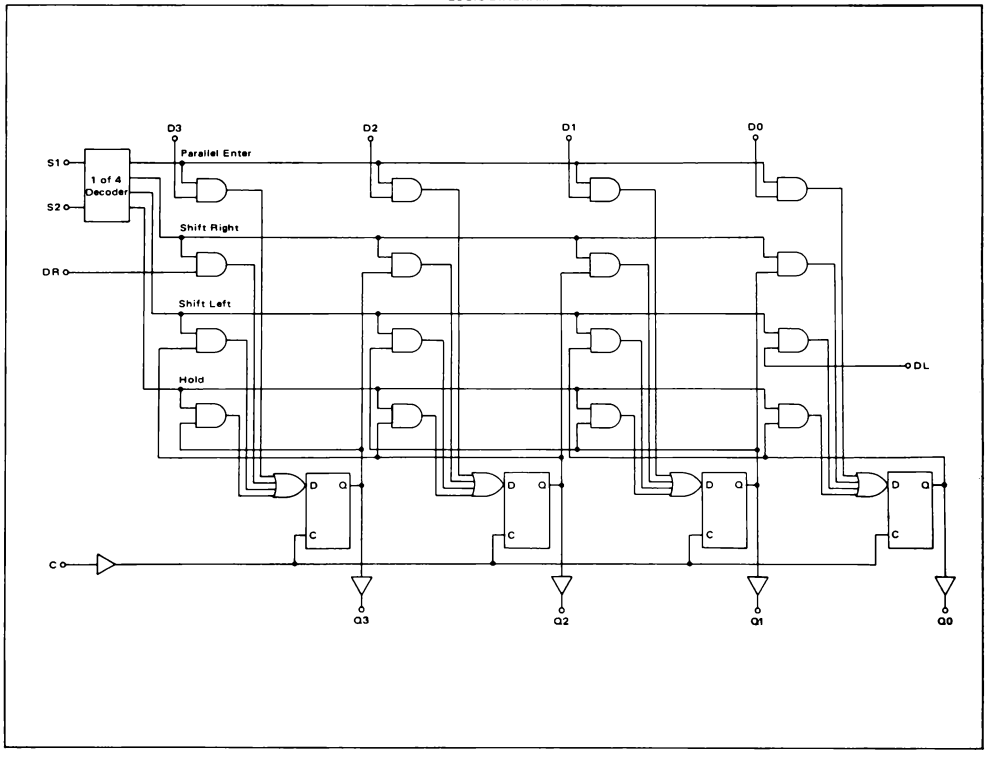
TRUTH TABLE

SELECT			OUTPUTS			
S1	S2	OPERATING MODE	$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).

P_D = 425 mW typ/pkg (No Load)
f_{Shift} = 200 MHz typ

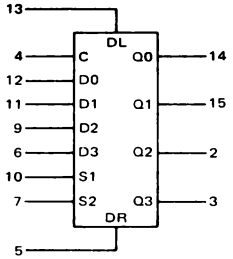
LOGIC DIAGRAM



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

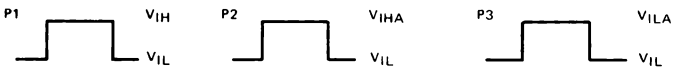
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.



L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

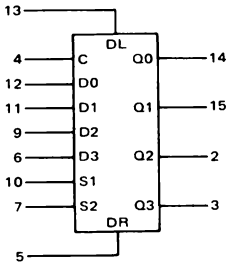
Characteristic	Symbol	Pin Under Test	MC10141L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	P1	P2	P3	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	82	102	–	–	mAdc	–	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\,H}$	5	–	–	–	–	220	–	–	μAdc	5	–	–	–	8	–	–	–	1,16
		6	–	–	–	–	220	–	–		6	–	–	–		–	–	–	
		7	–	–	–	–	245	–	–		7	–	–	–		–	–	–	
		4	–	–	–	–	265	–	–		4	–	–	–		–	–	–	
	$I_{in\,L}$	12	–	–	0.5	–	–	–	–	μAdc	4,5,6,7,9, 10,11,13	12	–	–	8	–	–		1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	4	–	–	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	4	–	–	1,16
Logic "1" Threshold Voltage ①	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	4	–	–	1,16
				–		–	–		–		6	④	–	7		4	–	–	
				–		–	–		–		6	④	–	–		–	4	–	
				–		–	–		–		–	–	–	–		–	–	4	
Logic "0" Threshold Voltage ①	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	4	–	–	1,16
			–		–	–		–			–	⑤	–	7		4	–	–	
			–		–	–		–			–	⑤	–	–		–	4	–	
			–		–	–		–			6	–	–	–		–	–	4	
Switching Times (50 Ω Load)															-3.2 V				+2.0 V
Propagation Delay	t_{4+3+}	3	0.9	3.9	1.0	2.9	3.8	1.2	4.2	ns	②	–	–	–	8	–	–	–	1,16
Setup Time (t_{setup})	t_{12+4+}	14	–	–	2.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{12-4+}		–	–	2.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{10+4+}		–	–	5.0	–	–	–	–		–	–	–	–		–	–	–	
	t_{10-4+}		–	–	5.0	–	–	–	–		–	–	–	–		–	–	–	
Hold Time (t_{hold})	t_{4+12+}		–	–	1.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{4+12-}		–	–	1.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{4+10+}		–	–	1.0	–	–	–	–		–	–	–	–		–	–	–	
	t_{4+10-}		–	–	1.0	–	–	–	–		–	–	–	–		–	–	–	
Rise Time (20% to 80%)	t_{3+}	3	1.0	3.4	1.1	1.7	3.3	1.1	3.6		②	–	–	–		–	–	–	
Fall Time (20% to 80%)	t_{3-}	3	1.0	3.4	1.1	1.7	3.3	1.1	3.6		②	–	–	–		–	–	–	
Shift Frequency	f_{Shift}	–	150	–	150	200	–	150	–	MHz	③	–	–	–		–	–	–	

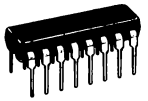


① These tests to be performed in sequence as shown.
② See switching time test circuit for test procedures.
③ See shift frequency test circuit for test procedures.
④ Reset to zero before performing test
⑤ Reset to one before performing test.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

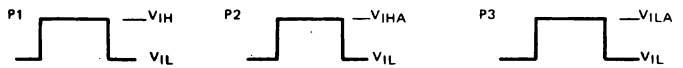




P SUFFIX
PLASTIC PACKAGE
CASE 648

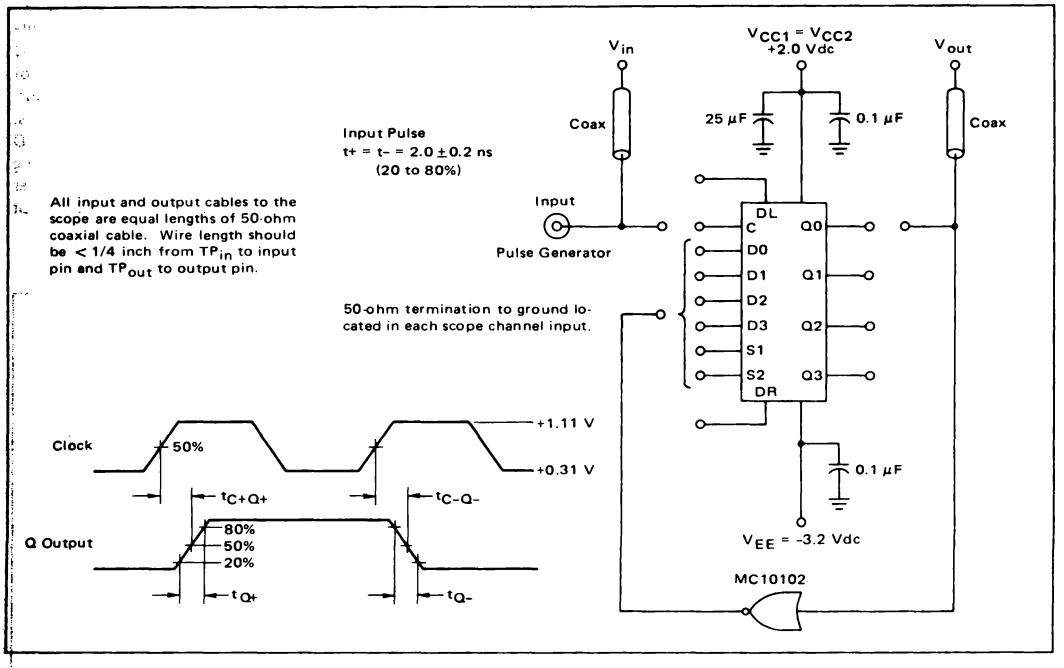
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\,max}$	$V_{IL\,min}$	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10141P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	P1	P2	P3	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	82	102	–	–	mAdc	–	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\,H}$	5	–	–	–	–	220	–	–	μAdc	5	–	–	–	8	–	–	–	1,16
		6	–	–	–	–	220	–	–	↓	6	–	–	–	↓	–	–		↓
		7	–	–	–	–	245	–	–		7	–	–	–		–	–	–	
		4	–	–	–	–	265	–	–		4	–	–	–		–	–	–	
	$I_{in\,L}$	12	–	–	0.5	–	–	–	–	μAdc	4,5,6,7,9, 10,11,13	12	–	–	8	–	–		1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–		8	4	–	–	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	4	–	–	1,16
Logic "1" Threshold Voltage	V_{OHA} ①	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	4	–	–	1,16
		↓	↓	–	↓	–	–	↓	–	↓	6	④	–	7	↓	4	–	–	↓
				–		–	–		–		6	④	–	–		–	4	–	
				–		–	–		–		–	–	–	–		–	–	4	
Logic "0" Threshold Voltage	V_{OLA} ①	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	4	–	–	1,16
		↓	–	↓	–	–	↓	–	↓	↓	–	⑤	–	7	↓	4	–	–	↓
			–		–	–		–			–	⑤	–	–			4	–	
			–		–	–		–			6	–	–	–		–	–	4	
Switching Times (50 Ω Load)															-3.2 V				+2.0 V
Propagation Delay	t_{4+3+}	3	–	–	1.0	2.9	3.8	–	–	ns	②	–	–	–	8	–	–	–	1,16
Setup Time (t_{setup})	t_{12-4+}	14	–	–	2.5	–	–	–	–	↓		–	–	–	↓	–	–	–	↓
	t_{12-4+}		–	–	2.5	–	–	–	–			–	–	–		–	–	–	
	t_{10+4+}		–	–	5.0	–	–	–	–			–	–	–		–	–	–	
	t_{10-4+}		–	–	5.0	–	–	–	–			–	–	–		–	–	–	
Hold Time (t_{hold})	t_{4+12+}		–	–	1.5	–	–	–	–			–	–	–		–	–	–	
	t_{4+12-}		–	–	1.5	–	–	–	–			–		–		–	–	–	
	t_{4+10+}		–	–	1.0	–	–	–	–				–	–		–	–	–	
	t_{4+10-}		–	–	1.0	–	–	–	–			–	–	–		–	–		
Rise Time (20% to 80%)	t_{3+}	3	–	–	1.1	1.7	3.3	–	–		②		–	–		–	–	–	
Fall Time (20% to 80%)	t_{3-}	3	–	–	1.1	1.7	3.3	–	–		②	–	–	–		–	–		
Shift Frequency	f_{Shift}	–	–	–	150	200	–	–	–	MHz	③	–	–	–	↓	–	–	–	↓

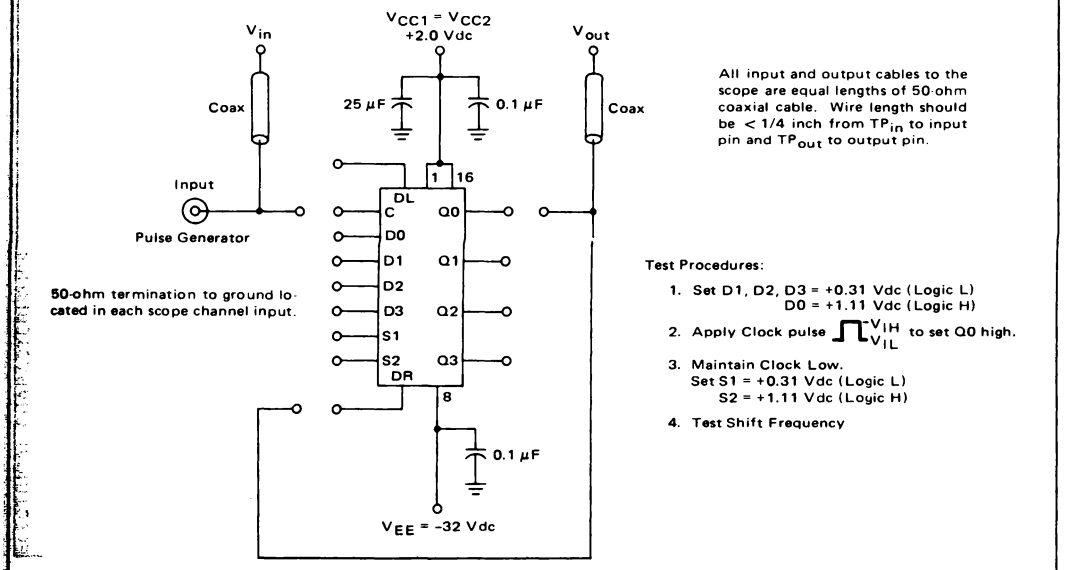


① These tests to be performed in sequence as shown.
② See switching time test circuit for test procedures.
③ See shift frequency test circuit for test procedures.
④ Reset to zero before performing test.
⑤ Reset to one before performing test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



SHIFT FREQUENCY TEST CIRCUIT



QUAD LATCH

MC10153

Advance Information

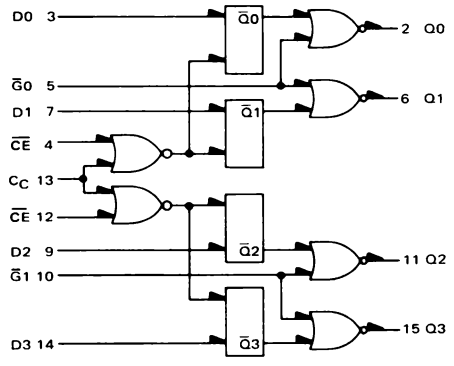
The MC10153 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on positive going transition of the clock. The MC10153 provides the same logic function as the MC10133, except for inversion of the clock.

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	L	H	H

ϕ = Don't Care
$C = C_C + \overline{CE}$

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

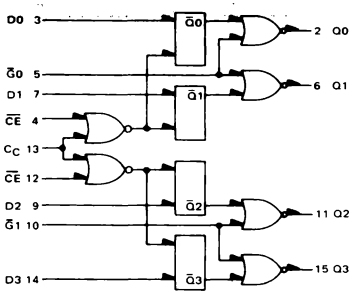


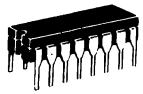
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10153L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	75	–	–	mAdc	–	13	–	–	8	1,16
Input Current	I_{inH}	3	–	–	–	–	245	–	–	μAdc	3	–	–	–	8	1,16
		4	–	–	–	–	290	–	–		4	–	–	–		
		5	–	–	–	–	350	–	–		5	–	–	–		
		13	–	–	–	–	350	–	–		13	–	–	–		
	I_{inL}	3	–	–	0.5	–	–	–	–	μAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3	4	–	–	8	1,16
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	3	13	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	3,13	–	–	8	1,16
		2									3,5	13	–	–		
		2				–					–	3,4	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980			-0.910	–	Vdc	3	4	–	5	8	1,16
		2		–		–	–				–	4	3	–		
		2		–		–					3	4	–	–		
		2†				–					3	–	–	–		
		2††		–			–				–	–	–	–		
		2††		–					–		–	–	–	–		
		2		–							3	–	–	4		
		2		–		–			–		3	–	–	13		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	3	4	5	–	8	1,16
		2	–								–	4	–	3		
		2	–		–	–					–	4	–	–		
		2†	–								–	–	–	–		
		2††	–								3	–	–	–		
		2††	–		–	–		–			3	–	–	13		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–	–	–	3.0	–		–	ns	–	–	3	2	8	1,16
	t_{13+2+}	2	–	–	–	4.0	–				3 *	–	4	2		
	t_{5-2+}	2		–	–	2.0	–		–		–		5	2		
	t_{Setup}	3	–	–	–	0.7	–				–	–	3	2		
	t_{Hold}	3		–	–	0.7	–				–		3	2		
Rise Time (20% to 80%)	t_{2+}	2			–	2.0	–				–	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2			–	2.0	–				–	–	3	2		

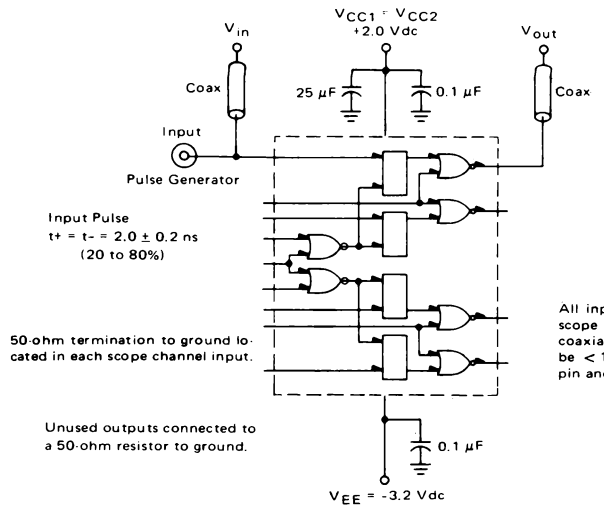
†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

††Data input at proper high/low level while clock pulse is low so that device latches at proper high/low level for test. Levels are measured after device has latched.

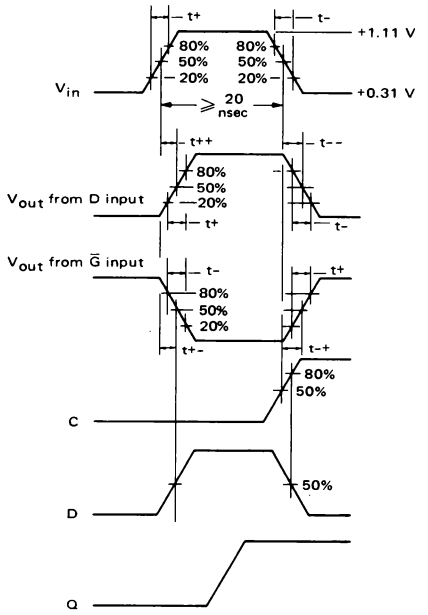
V_{IH} max
V_{IL} min

*Latch set to zero state before test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



PROPAGATION DELAY

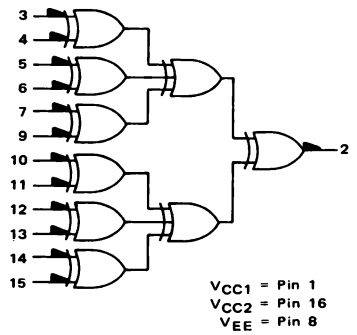


t_{setup} is minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

12-BIT PARITY
GENERATOR-CHECKER

MC10160



The MC10160 consists of nine EXCLUSIVE-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

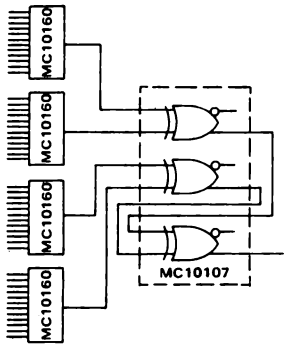
P_D = 320 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ

APPLICATIONS INFORMATION

The MC10160 is useful in any system requiring high speed detection or generation of parity. The MC10160 can generate parity for twelve bits in 4 ns. A large number of functions on one chip reduces package count and saves system power. As shown in Figure 1, by using four MC10160's and one MC10107 parity can be checked or generated on 48 bits in 9.5 ns, or 7.5 ns if the MC10107 is replaced by a MECL III MC1672 or MC1674.

If parity detection or generation is required for less than twelve bits, the unnecessary inputs can be left open. Input pulldown resistors will insure that the unused inputs are pulled to the low logic level.

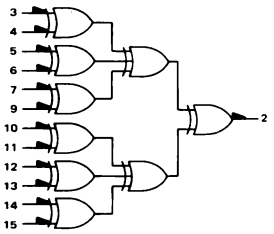
FIGURE 1 – 48-BIT PARITY CHECKER

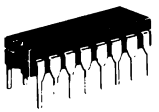


See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.





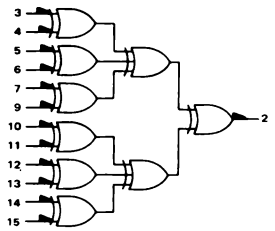
L SUFFIX
CERAMIC PACKAGE
CASE 620

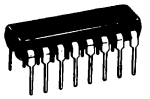
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10160L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	62	78	–	–	mAdc	4,5,9,10,13,14	–	–	–	8	1,16
Input Current	I_{inH}	3	–	–	–	–	265	–	–	μAdc	3	–	–	–	8	1,16
		4	–	–	–	–	220	–	–	μAdc	4	–	–	–	8	1,16
	I_{inL}	3	–	–	0.5	–	–	–	–	μAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3	4,5,6,7,9,10, 11,12,13,14,15	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	3,4,5,6,7,9,10, 11,12,13,14,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	4,5,6,7,9,10,11, 12,13,14,15	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	3,5,6,7,9,10,11 12,13,14,15	–	4	8	1,16
Switching Times (50 Ω Load)																
Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
	t_{3+2+}	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	ns	–	–	3	2	8	1,16
	t_{3+2-}										4	–				
	t_{3-2-}										–	–				
	t_{3-2+}										4	–				
	t_{4+2+}										–	–	4			
	t_{4+2-}										3	–				
	t_{4-2-}										–	–				
	t_{4-2+}										3	–				
Rise Time (20% to 80%)	t_{2+}		1.1	3.5	1.1	2.0	3.3	1.0	3.5		–	–	3			
Fall Time (20% to 80%)	t_{2-}		1.1	3.5	1.1	2.0	3.3	1.0	3.5		–	–	3			

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.



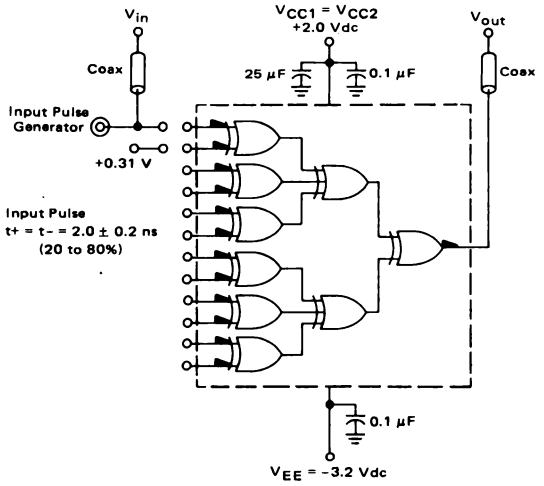


P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10160P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	62	78	–	–	mAdc	4,5,9,10,13,14	–	–	–	8	1,16
Input Current	I_{inH}	3	–	–	–	–	265	–	–	µAdc	3	–	–	–	8	1,16
		4	–	–	–	–	220	–	–	µAdc	4	–	–	–	8	1,16
	I_{inL}	3	–	–	0.5	–	–	–	–	µAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3	4,5,6,7,9,10, 11,12,13,14,15	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	3,4,5,6,7,9,10, 11,12,13,14,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	4,5,6,7,9,10,11, 12,13,14,15	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	3,5,6,7,9,10,11 12,13,14,15	–	4	8	1,16
Switching Times (50 Ω Load)																
Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
	t_{3+2+}	2	–	–	2.0	5.0	7.5	–	–	ns	–	–	3	2	8	1,16
	t_{3+2-}		–	–				–	–		4	–				
	t_{3-2-}		–	–				–	–		–	–				
	t_{3-2+}		–	–				–	–		4	–				
	t_{4+2+}		–	–				–	–		–	–	4			
	t_{4+2-}		–	–				–	–		3	–				
	t_{4-2-}		–	–				–	–		–	–				
	t_{4-2+}		–	–				–	–		3	–				
Rise Time (20% to 80%)	t_{2+}		–	–	1.1	2.0	3.3	–	–		–	–	3			
Fall Time (20% to 80%)	t_{2-}		–	–	1.1	2.0	3.3	–	–		–	–	3			

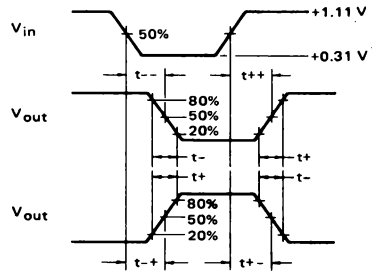
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

PROPAGATION DELAY

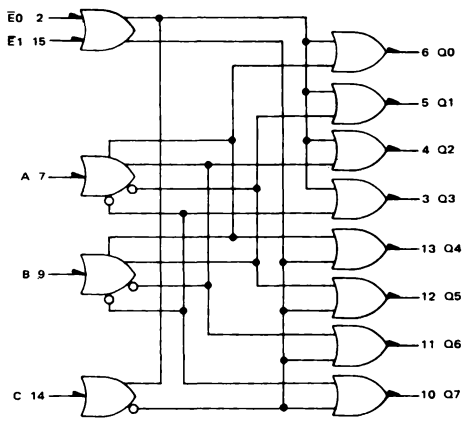


BINARY TO 1-8 DECODER
(LOW)

MC10161

The MC10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high. This device has high Z input pulldown resistors and open emitter outputs.

POSITIVE LOGIC



P_D = 315 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

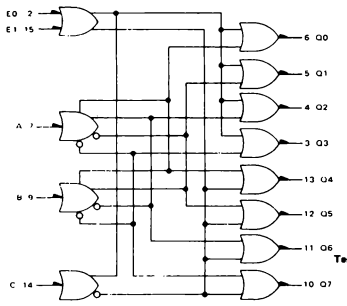
ENABLE INPUTS		INPUTS			OUTPUTS							
Ē1	Ē0	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H
ϕ	H	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

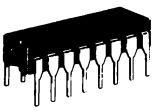
ϕ = Don't Care

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input/output combination. Other combinations are tested according to the truth table.



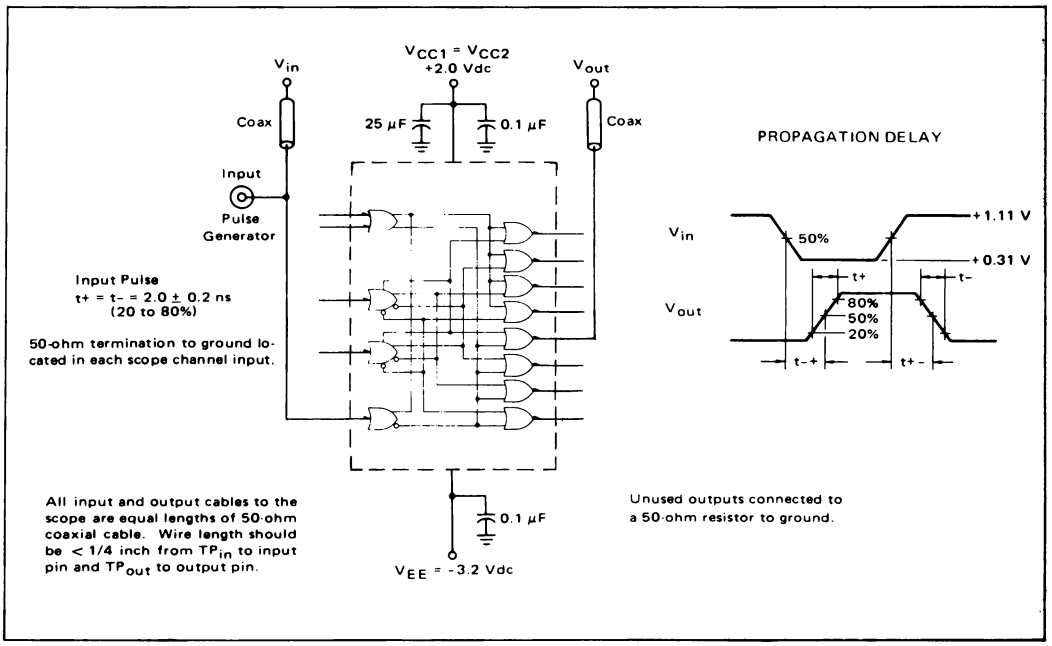


L SUFFIX
CERAMIC PACKAGE
CASE 620

● Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

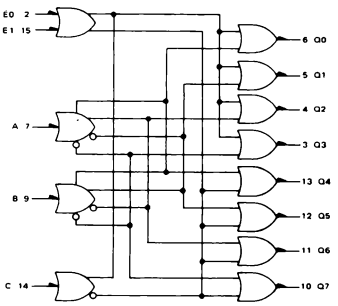
Characteristic	Symbol	Pin Under Test	MC10161L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	61	76	–	–	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	220	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	2	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	2	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	14	–	8	1,16
Switching Times (50 Ω Load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13-}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	–	–	14	13	8	1,16
	t_{14-13+}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4		–	–				
Rise Time (20% to 80%)	t_{13+}	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–	–				
Fall Time (20% to 80%)	t_{13-}	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–	–				

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input/output combination. Other combinations are tested according to the truth table.



P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

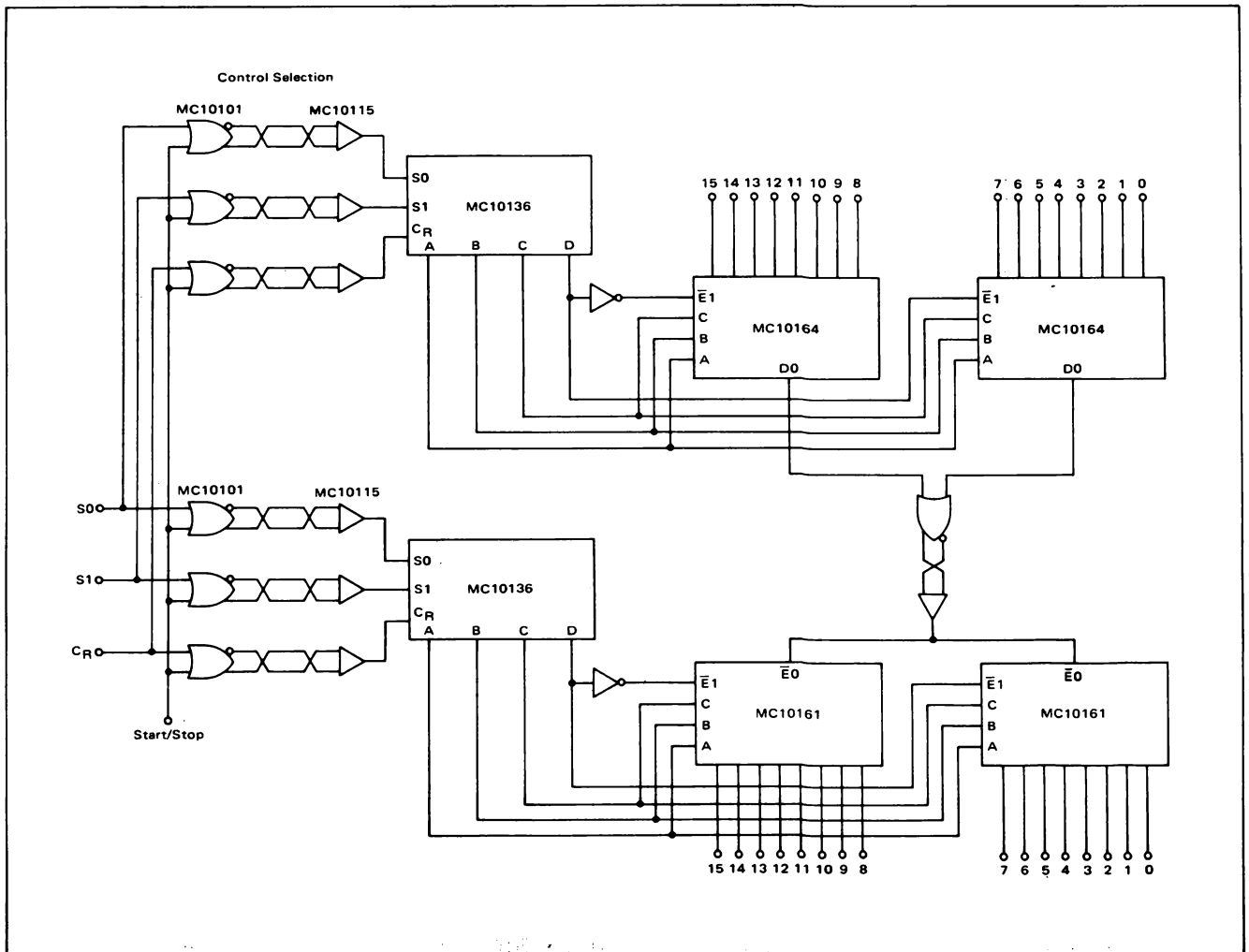
Characteristic	Symbol	Pin Under Test	MC10161P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	61	76	–	–	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	220	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	2	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	2	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	14	–	8	1,16
Switching Times (50 Ω Load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13-}	13	–	–	1.5	4.0	6.0	–	–	ns	–	–	14	13	8	1,16
	t_{14-13+}	13	–	–	1.5	4.0	6.0	–	–		–	–				
Rise Time (20% to 80%)	t_{13+}	13	–	–	1.1	2.0	3.3	–	–		–	–				
Fall Time (20% to 80%)	t_{13-}	13	–	–	1.1	2.0	3.3	–	–		–	–				

APPLICATION INFORMATION

The MC10161 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4 ns delay from any address or enable input to any output.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both *S0* and *S1* are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the MC10101s to send twisted-pair select data to the multiplexer/demultiplexer units.

FIGURE 1 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

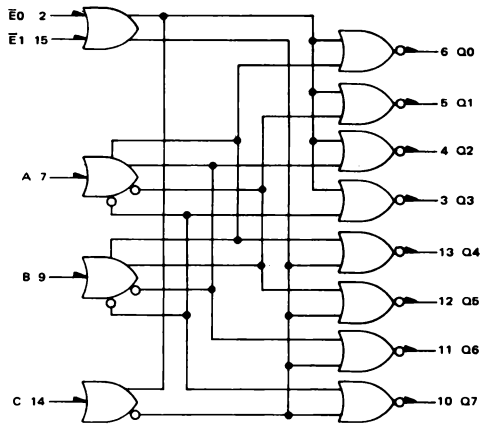


BINARY TO 1-8 DECODER
(HIGH)

MC10162

The MC10162 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

POSITIVE LOGIC



P_D = 315 ns typ/pkg (No Load)
t_{pd} = 4.0 ns typ

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

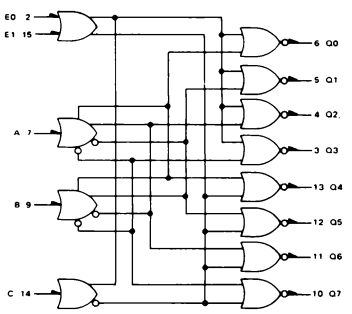
INPUTS					OUTPUTS							
Ē0	Ē1	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L
ϕ	H	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

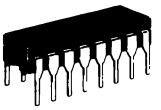
ϕ = Don't Care

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only input/output combination. Other combinations are tested according to the truth table.



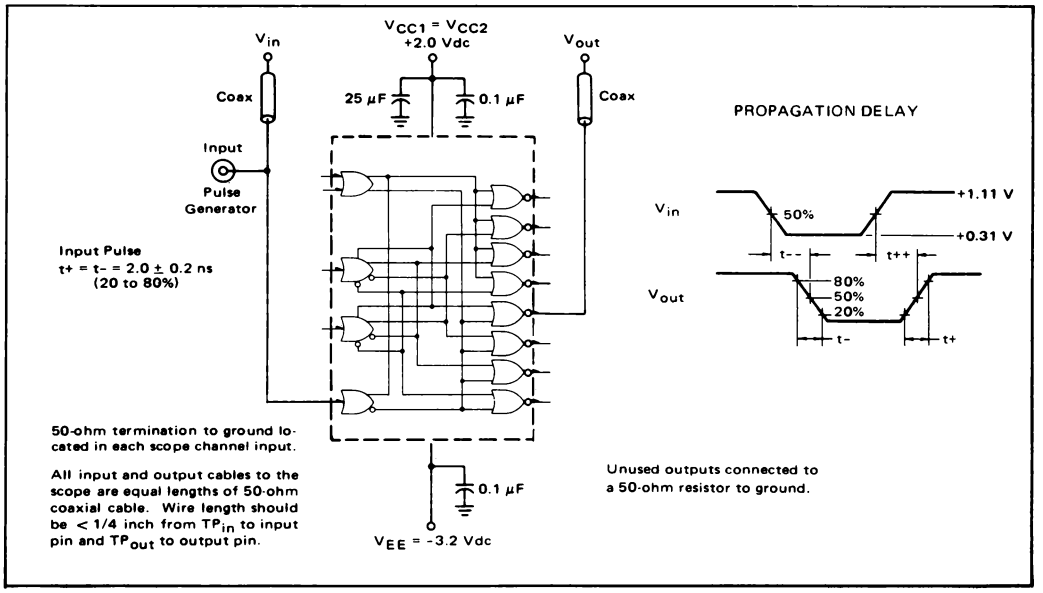


L SUFFIX
CERAMIC PACKAGE
CASE 620

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

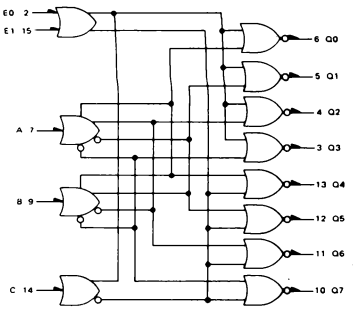
Characteristic	Symbol	Pin Under Test	MC10162L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	-		-	61	76	-		mAdc	-	-	-	-	8	1,16
Input Current	I_{inH}	14	-	-	-		220			µAdc	14	-	-	-	8	1,16
	I_{inL}	14	-	-	0.5	-		-	-	µAdc	-	14		-	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	14	-	-	-	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	2	-	-	-	8	1,16
		13	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	15	-	-	-	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.080		-0.980			-0.910		Vdc	-	-	14	-	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	-	-1.655			-1.630		-1.595	Vdc			2	-	8	1,16
		13	-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	-	15	-	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13+}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	-	-	14	13	8	1,16
	t_{14-13-}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4		-	-				
Rise Time (20% to 80%)	t_+	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		-	-				
Fall Time (20% to 80%)	t_-	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		-	-				

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only input/output combination. Other combinations are tested according to the truth table.



P SUFFIX
PLASTIC PACKAGE
CASE 648

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10162P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	61	76	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	220	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	2	–	–	–	8	1,16
		13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	15	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	2	–	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	15	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13+}	13	–	–	1.5	4.0	6.0	–	–	ns	–	–	14	13	8	1,16
	t_{14-13-}	13	–	–	1.5	4.0	6.0	–	–		–	–				
Rise Time (20% to 80%)	t_+	13	–	–	1.1	2.0	3.3	–	–		–	–				
Fall Time (20% to 80%)	t_-	13	–	–	1.1	2.0	3.3	–	–		–	–				

APPLICATION INFORMATION

The MC10162 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders.

This device is ideally suited for demultiplexer applications as shown in Figure 1. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 2. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. Control information via twisted pair lines is sent through MC10101 gates to the MC10115 line receivers to provide select data to the multiplexer/demultiplexer units.

FIGURE 1 – DEMULTIPLEXER (1 OF-8 LOCATIONS)

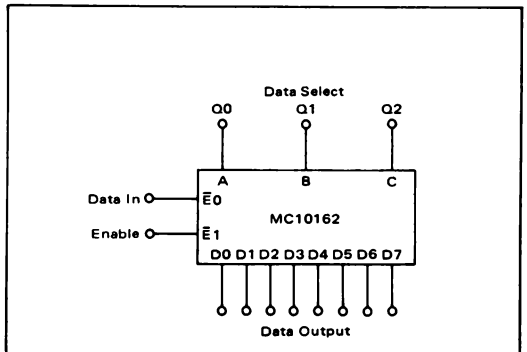
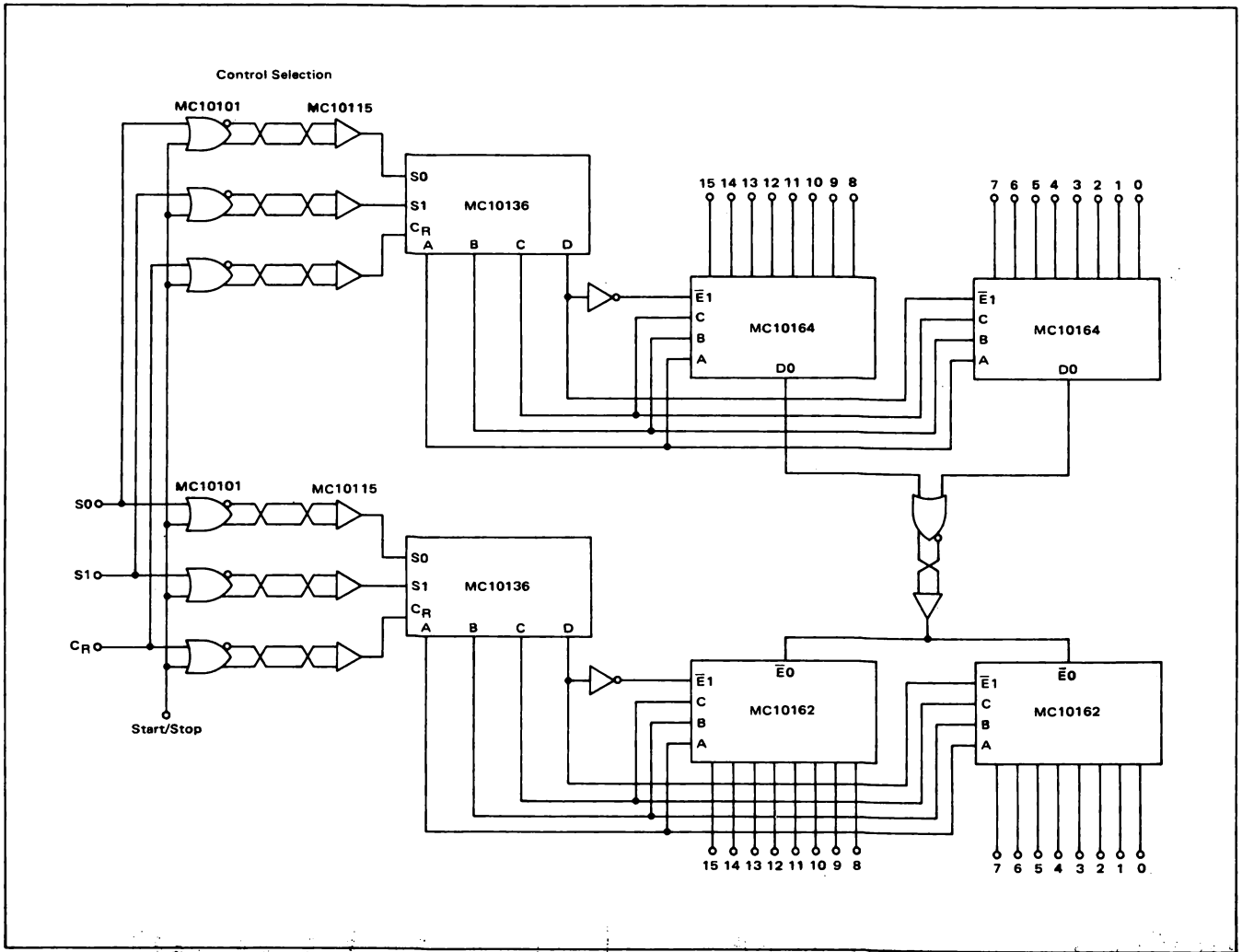


FIGURE 2 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

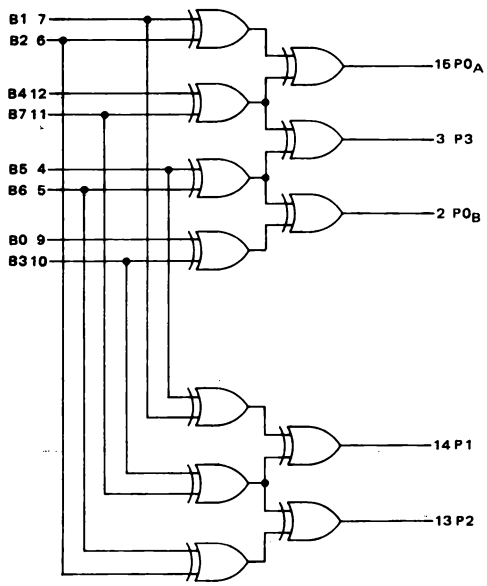


MC10163 • MC10193

Advance Information

The MC10163 and the MC10193 are error detection and correction circuits. They are building blocks designed for use with memory systems. They offer economy in the design of error detection/correction subsystems for mainframe and add-on memory systems. For example, using eight MC10163's together with eight 12-bit parity checkers (MC10160), single-bit error detection/correction and double-bit error detection can be done on a word of 64-bit length. Only eight check bits (B0-B7) need be added to the word. A useful feature of this building block is that the MC10193 option generates the parity of all inputs to the block. Thus, if the MC10193 is applied in a byte sequence, individual byte parity is automatically available.

MC10163 LOGIC DIAGRAM



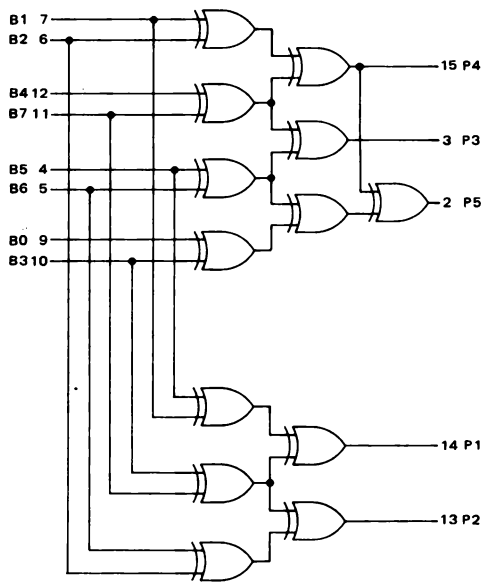
IBM CODE

$P0_A$ = B1, B2, B4, B7
$P0_B$ = B0, B3, B5, B6
P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 520 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ

MC10193 LOGIC DIAGRAM



MOTOROLA CODE

P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7
P4 = B1, B2, B4, B7
P5 = Byte (B0, 1, 2, 3, 4, 5, 6, 7)

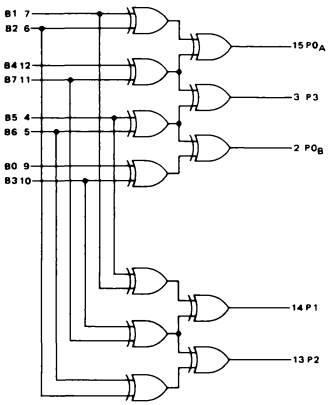
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

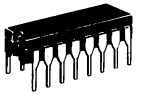
P_D = 520 mW typ/pkg (No Load)
t_{pd} = 7.5 ns typ (pin 7 to pin 2)

This is advance information and specifications are subject to change without notice.
See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

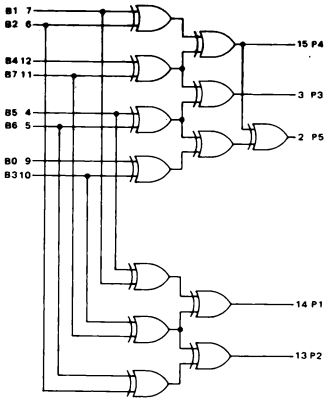
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

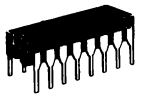
Characteristic	Symbol	Pin Under Test	MC10163L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	125	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4,6,10	–	–	–	–	220	–	–	µAdc	4,6,10	–	–	–	8	1,16
		5,7,9,11,12	–	–	–	–	265	–	–	µAdc	5,7,9,11,12	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	↓	↓	↓	–	↓	↓	↓	↓	4	–	–	–	↓	↓
		13				–					11	–	–	–		
		14				–					11	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	4	–	–	8	1,16
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11	–	–	↓	↓
		13				–					–	11	–	–		
		14				–					–	11	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		3	↓	–	↓	–	–	↓	–	↓	–	–	11	–	↓	↓
		13		–		–	–		–		–	–	5	–		
		14		–		–	–		–		–	–	4	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		3	–	↓	–	–	↓	–	↓	↓	–	–	–	11	↓	↓
		13	–		–	–		–			–	–	–	5		
		14	–		–	–		–			–	–	–	4		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+15+}	15	–	–	–	5.0	–	–	–	ns	–	–	7	15	8	1,16
	t_{4+14+}	14	–	–	–	5.0	–	–	–	↓	–	–	4	14	↓	↓
Rise Time (20% to 80%)	t_{15+}	15	–	–	–	2.0	–	–	–		–	–	7	15		
Fall Time (20% to 80%)	t_{15-}	15	–	–	–	2.0	–	–	–	↓	–	–	7	15	↓	↓

*Individually test each input, apply V_{ILmin} to pin under test.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





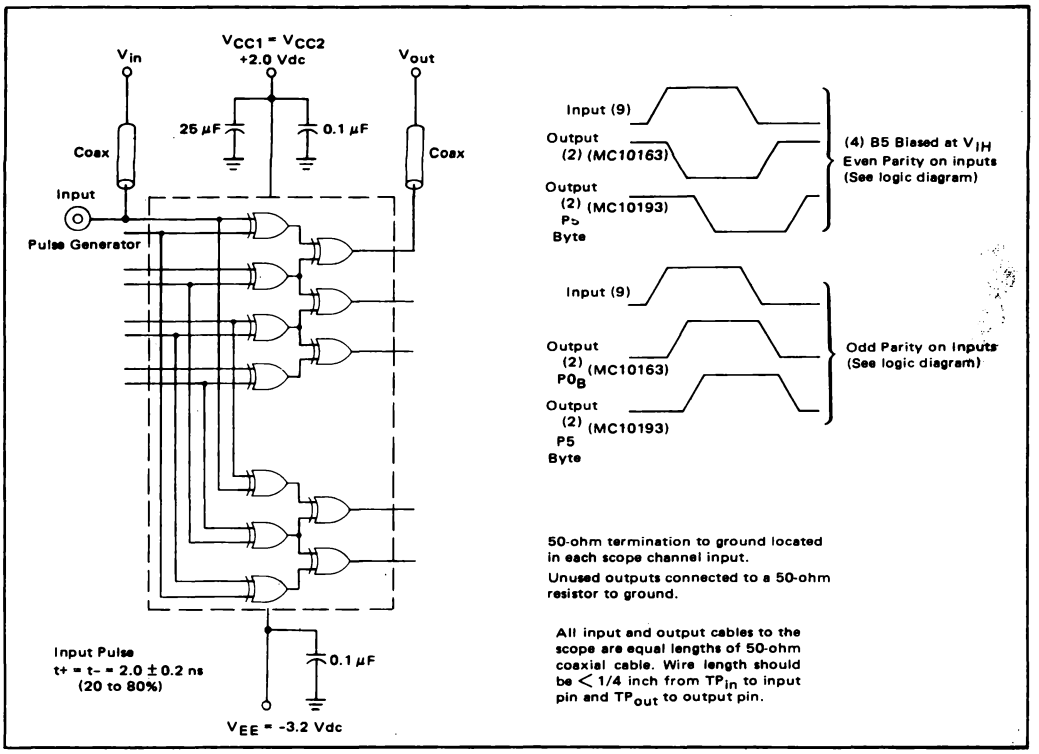
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10193L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	125	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4,6,10	–	–	–	–	220	–	–	µAdc	4,6,10	–	–	–	8	1,16
		5,7,9,11,12	–	–	–	–	265	–	–	µAdc	5,7,9,11,12	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	↓	↓	↓	–	↓	↓	↓	↓	4	–	–	–	↓	↓
		13				–					11	–	–	–		
		14				–					11	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	4	–	–	8	1,16
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11	–	–	↓	↓
		13				–					–	11	–	–		
		14				–					–	11	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		3	↓	–	↓	–	–	↓	–	↓	–	–	11	–	↓	↓
		13		–		–	–		–		–	–	5	–		
		14		–		–	–		–		–	–	4	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		3	–	↓	–	–	↓	–	↓	↓	–	–	–	11	↓	↓
		13	–		–	–		–			–	–	–	5		
		14	–		–	–		–			–	–	–	4		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+15+}	15	–	–	–	5.0	–	–	–	ns	–	–	7	15	8	1,16
	t_{4+14+}	14	–	–	–	5.0	–	–	–	↓	–	–	4	14	↓	↓
	t_{7+2+}	2	–	–	–	7.5	–	–	–		–	–	7	2		
	t_{4+2+}	2	–	–	–	7.5	–	–	–		–	–	4	2		
Rise Time (20% to 80%)	t_{15+}	15	–	–	–	2.5	–	–	–		–	–	7	15		
Fall Time (20% to 80%)	t_{15-}	15	–	–	–	2.5	–	–	–	↓	–	–	7	15	↓	↓

*Individually test each input, apply V_{ILmin} to pin under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C (MC10163)



MC10163 APPLICATIONS INFORMATION

The MC10163 is a building block for generating the modified Hamming single-error-correction, double-error-detection (SEC-DED) code used in the IBM 370/145 memory. While the MC10163 can also be used for generating other patterns, it is optimized for generating the pattern shown in the H matrix of Figure 1.

When writing into a memory, the MC10163 is used to generate the eight check bits (C0-C32, CT) which are stored with the 65 data bits (B0-B63). These check bits are generated by taking the parity of all data bits marked with an X in the appropriate row of the H matrix. (C0, C1, C32, CT, are even parity; C2, C4, C8, C17, are odd parity.) To generate these check bits with the building blocks, eight MC10163's and eight MC10160 parity checkers are used. One MC10163 is connected to each byte of data and the outputs of these building blocks are connected to the eight MC10160 parity checkers, one for each check bit. Figure 2 shows which connections are required (i.e., C0 is the even parity of output $P0_A$ of the MC10163 on the "zero" byte of data, output $P0_B$ of the "zero" byte, $P0_A$ of the "one" byte, ---, $P0_B$ of the "three" byte and data bit 32.)

During the memory read operation, the fetched check bits previously generated (as described) are exclusive-ORed with newly generated C0-C32 to generate syndrome bits S0-S32. Syndrome ST is a special case where ST is the even parity of all eight fetched check bits and all 64 fetched data bits. For determining the type and location of an error:

1. If all syndromes (S0-S32 and ST) are false, there is no error.
2. If ST is true and S0-S32 are false, the CT is in error.
3. If ST is false and one or more of S0-S32 is true, an uncorrectable error has occurred.
4. If ST is true and one or more of S0-S32 is true, simply add the S1-S32 bits to get the binary location of the error (S1 has weight 1, S2 weight 2, S4 weight 4, etc.)

Data bits B0 and B32 are special cases of this location technique: B0 is in error if ST, S0, and S32 are true; B32 is in error if ST, S0, S1, and S32 are true.

FIGURE 1 – 370/145 PATTERN

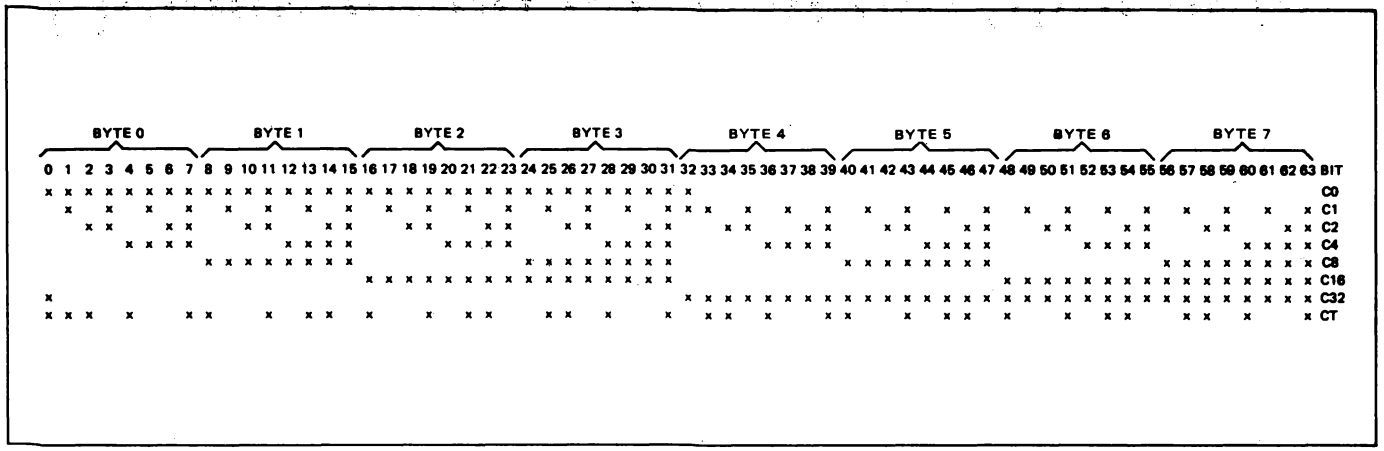


FIGURE 2 – 370/145 PATTERN GENERATION

C0 = $P0_{A0}$	$P0_{B0}$	$P0_{A1}$	$P0_{B1}$	$P0_{A2}$	$P0_{B2}$	$P0_{A3}$	$P0_{B3}$	B(32)
C1 = P10	P11	P12	P13	P14	P15	P16	P17	B(32)
C2 = P20	P21	P22	P23	P24	P25	P26	P27	
C4 = P30	P31	P32	P33	P34	P35	P36	P37	
C8 = $P0_{A1}$	$P0_{B1}$	$P0_{A3}$	$P0_{B3}$	$P0_{A5}$	$P0_{B5}$	$P0_{A7}$	$P0_{B7}$	
C16 = $P0_{A2}$	$P0_{A2}$	$P0_{A3}$	$P0_{B3}$	$P0_{A6}$	$P0_{B6}$	$P0_{A7}$	$P0_{B7}$	
C32 = $P0_{A4}$	$P0_{B4}$	$P0_{A5}$	$P0_{B5}$	$P0_{A6}$	$P0_{B6}$	$P0_{A7}$	$P0_{B7}$	B(0)
CT = $P0_{A0}$	$P0_{B1}$	$P0_{B2}$	$P0_{A3}$	$P0_{A4}$	$P0_{B5}$	$P0_{B6}$	$P0_{A7}$	B(0)

Where for P_{NM}: N = MC10163 Output
M = Byte Number

MC10193 APPLICATIONS INFORMATION

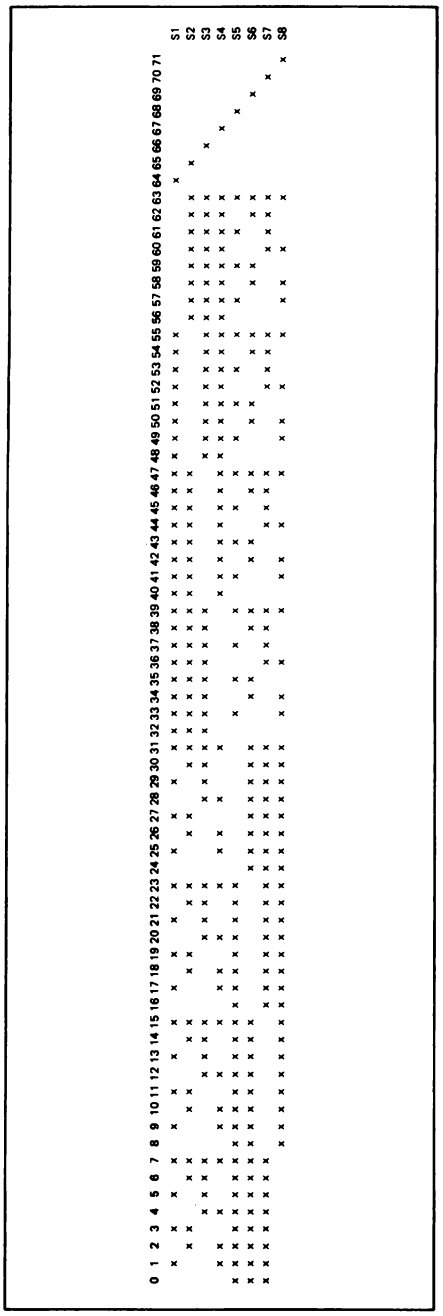


FIGURE 3 – MOTOROLA PATTERN EXAMPLE

The MC10193 is a building block for generating modified Hamming SEC-DED codes. It can be used for any length data word and for a variety of codes. The MC10193 is optimized for codes organized on a byte repetitive basis and has the advantage of automatically supplying whole byte parity (P5 output). While it is possible to use a number of criteria for choosing a pattern, the pattern of Figure 3 was chosen on the basis of speed and ease of error location decode. As can be seen in the H matrix of Figure 3, the pattern is repetitive by byte with the various rows generated by only five combinations of bit parities within the bytes. For the 64 bit data word in the example of Figure 3, the eight check bits (B64 to B71) are generated by the odd parity of all data bits indicated by an X in the appropriate row. The syndromes S1 to S8 are generated by including the fetched check bits in the same generator that originally generated the check bits.

The pattern of Figure 3 is easily generated by using eight MC10193 devices, one for each data byte and eight MC10160 parity checkers, one for each syndrome/check bit. The connections of building blocks and parity checkers are shown in tabular form in Figure 4 and in schematic form in Figure 6.

Once the syndrome bits (S1 to S8) have been formed from fetched data (B0 to B63) and fetched check bits (B64 to B71), the determination of type and location of error is simply done:

1. If all syndromes are false, there is no error.
2. If one syndrome is true, the corresponding check bit is in error.
3. If more than one syndrome is true, and the parity of all syndromes is even, a multiple (uncorrectable) error has occurred.
4. If more than one syndrome is true, and the parity of all syndromes is odd, a single error has occurred and is easily located by the circuit of Figure 5.

Figure 5 gives the error location circuit for the example pattern. The outputs EB0 to EB7 are a one-of-eight-high code giving the byte in error. Outputs EC0 to EC3 give the binary location of the bit in error within the located byte. Since this location process can occur simultaneously with the determination of error type described, the entire error correction sequence (using a toggling fetched data latch) takes less than 20 ns. This is because an error occurrance detector is a simple ORing of S1 to S8. The error locator has simultaneously located the error which is then corrected as though the error was a single (and therefore correctable) error. The parity of syndromes then determines if the error was indeed single, and interrupts the CPU if the error was an uncorrectable (multiple) error. Since uncorrectable data is unusable without special handling, the CPU would be interrupted anyway; therefore this automatic correction of any error as if it were single does not create any problems. This fast error correction technique allows single error correction on a non-interrupt basis with only a 20 ns memory system access time penalty.

These techniques can, of course, be extended to large or smaller data words.

FIGURE 4 – M2 PATTERN BUILDING BLOCK

S1 =	P10	P11	P12	P13	P54	P55	P56	B(64)
S2 =	P20	P21	P22	P23	P54	P55	P57	B(65)
S3 =	P30	P31	P32	P33	P54	P56	P57	B(66)
S4 =	P40	P41	P42	P43	P55	P56	P57	B(67)
S5 =	P14	P15	P16	P17	P50	P51	P52	B(68)
S6 =	P24	P25	P26	P27	P50	P51	P53	B(69)
S7 =	P34	P35	P36	P37	P50	P52	P53	B(70)
S8 =	P44	P45	P46	P47	P51	P52	P53	B(71)

Where for P_{NM}: N = MC10193 Output
M = Byte Number

FIGURE 5 – M2 PATTERN CORRECTION MATRIX

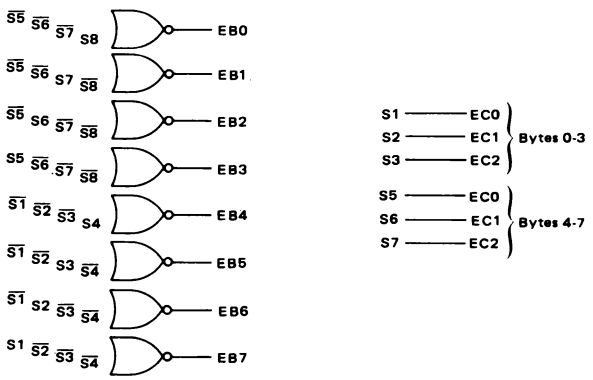
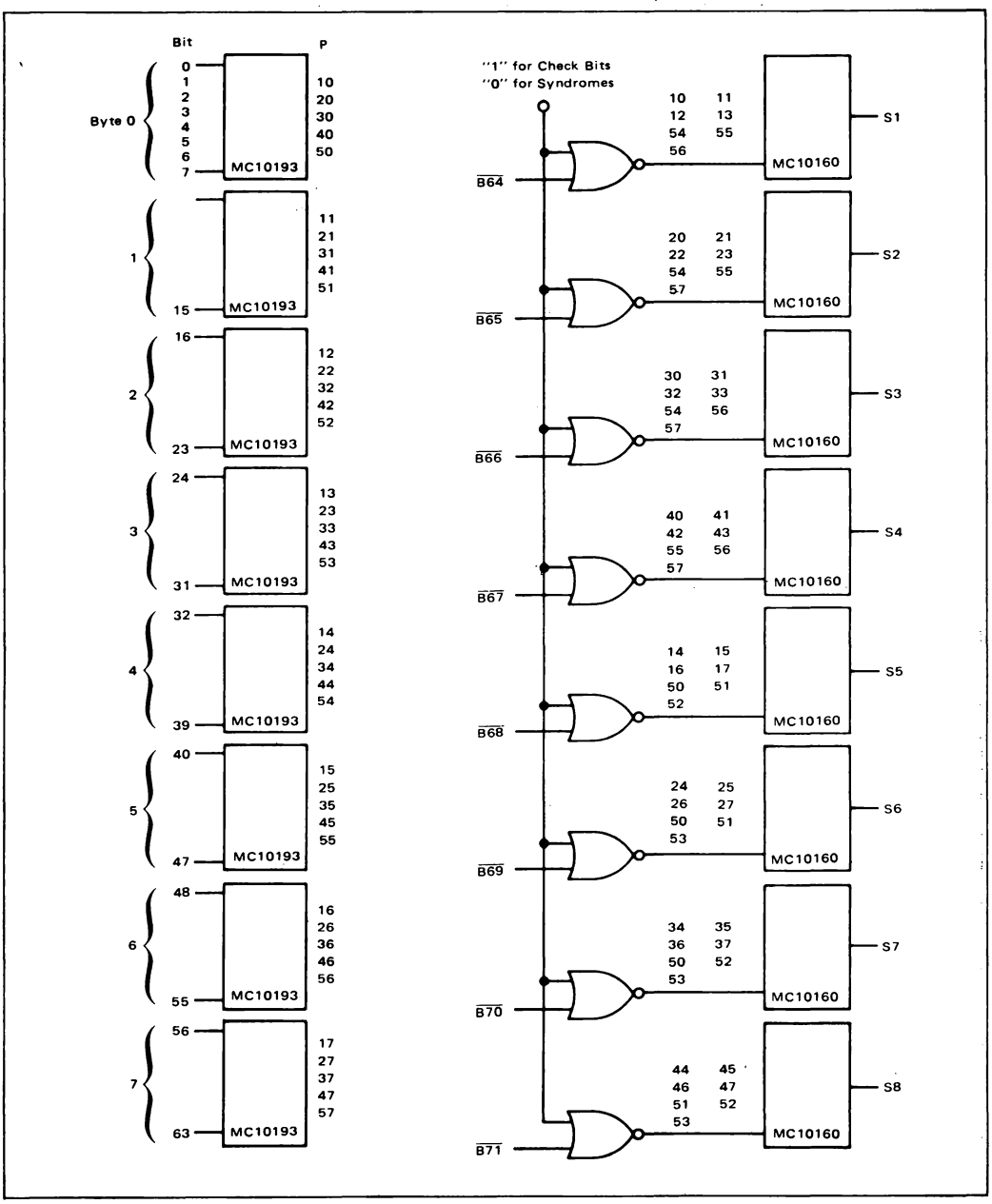


FIGURE 6 – SYNDROME AND CHECK BIT GENERATOR, M2 PATTERN



MC10164

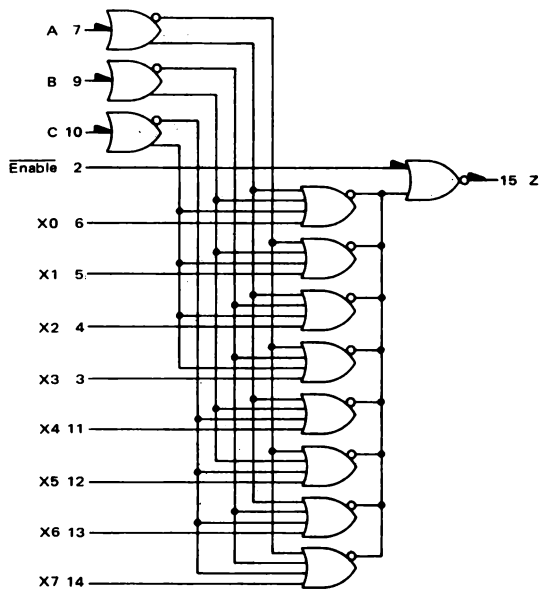
The MC10164 is a high speed, low power eight-channel data selector which routes data present at one-of-eight inputs to the output. The data is routed according to the three bit code present on the address inputs. An enable input is provided for easy bit expansion.

TRUTH TABLE

ENABLE	ADDRESS INPUTS C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ (Data to output)

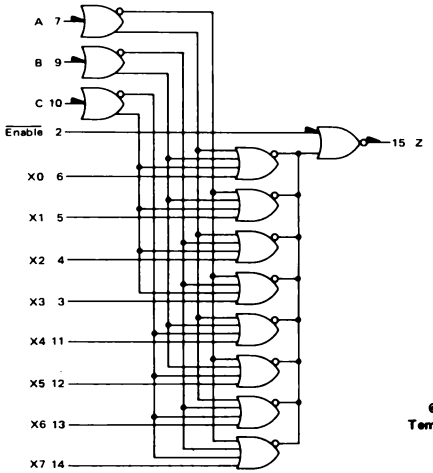


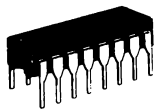
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.





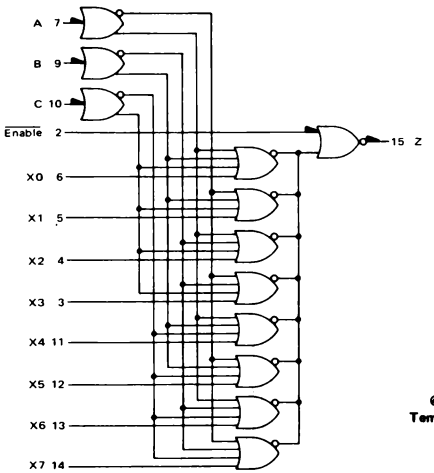
L SUFFIX
CERAMIC PACKAGE
CASE 620

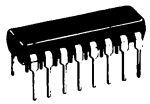
@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10164L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	60	75	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	2	–	–	–	–	265	–	–	μAdc	2	–	–	–	8	1,16
	$I_{in\ L}$	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	4,9	–	–	2	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	–	2	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+15+}	15	1.5	4.7	1.5	3.0	4.5	1.6	4.8	ns	9	–	4	15	8	1,16
	t_{4-15-}	15	1.5	4.7	1.5	3.0	4.5	1.6	4.8		9	–	4			
	t_{7+15+}	15	1.9	6.3	2.0	4.0	6.0	2.2	6.5		5	–	7			
	t_{7-15-}	15	1.9	6.3	2.0	4.0	6.0	2.2	6.5		5	–	7			
	t_{2+15+}	15	0.9	3.3	1.0	2.0	2.9	1.0	3.1		7,5	–	2			
	t_{2-15+}	15	0.9	3.3	1.0		2.9	1.0	3.1		7,5	–	2			
Rise Time (20% to 80%)	t_+	15	0.9	3.3	1.1		3.3	1.2	3.6		9	–	4			
Fall Time (20% to 80%)	t_-	15	0.9	3.3	1.1		3.3	1.2	3.6		9	–	4			

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.



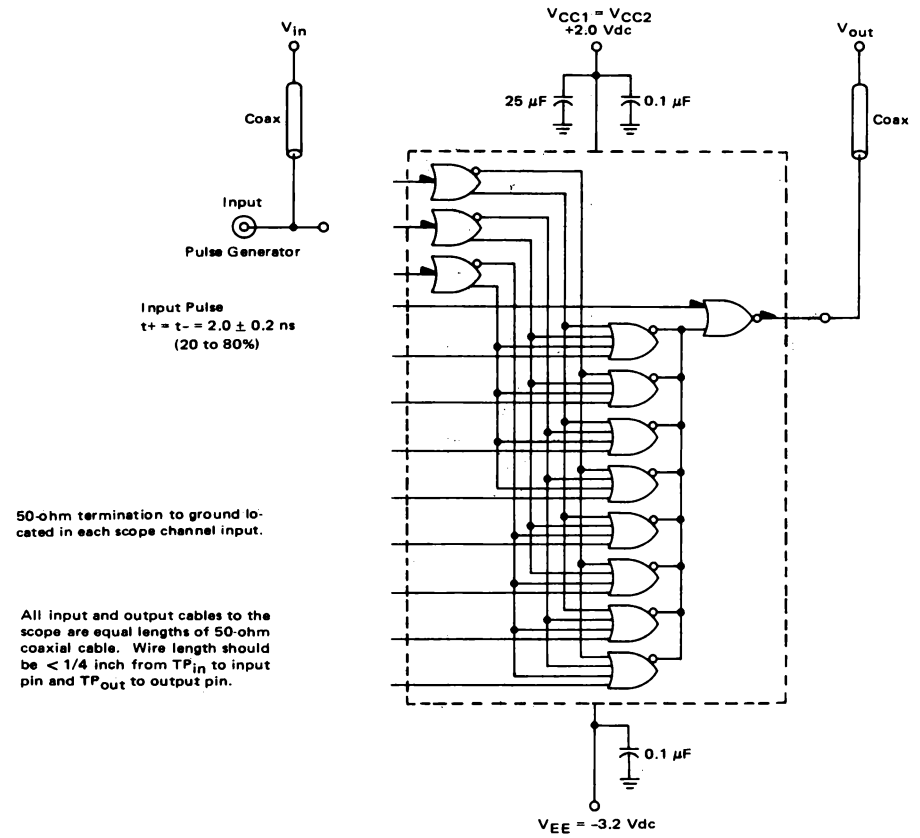


P SUFFIX
PLASTIC PACKAGE
CASE 648

@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10164P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	60	75	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	2	–	–	–	–	265	–	–	μAdc	2	–	–	–	8	1,16
	$I_{in\ L}$	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	4,9	–	–	2	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	–	2	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+15+}	15	–	–	1.5	3.0	4.5	–	–	ns	9	–	4	15	8	1,16
	t_{4-15-}	15	–	–	1.5	3.0	4.5	–	–		9	–	4			
	t_{7+15+}	15	–	–	2.0	4.0	6.0	–	–		5	–	7			
	t_{7-15-}	15	–	–	2.0	4.0	6.0	–	–		5	–	7			
	t_{2+15+}	15	–	–	1.0	2.0	2.9	–	–		7,5	–	2			
	t_{2-15+}	15	–	–	1.0		2.9	–	–		7,5	–	2			
Rise Time (20% to 80%)	t+	15	–	–	1.1		3.3	–	–		9	–	4			
Fall Time (20% to 80%)	t-	15	–	–	1,1		3.3	–	–		9	–	4			

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

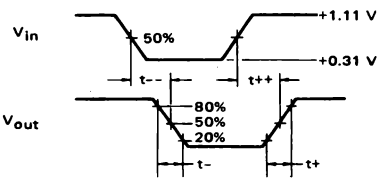


Input Pulse
$t+ = t- = 2.0 \pm 0.2$ ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

PROPAGATION DELAY

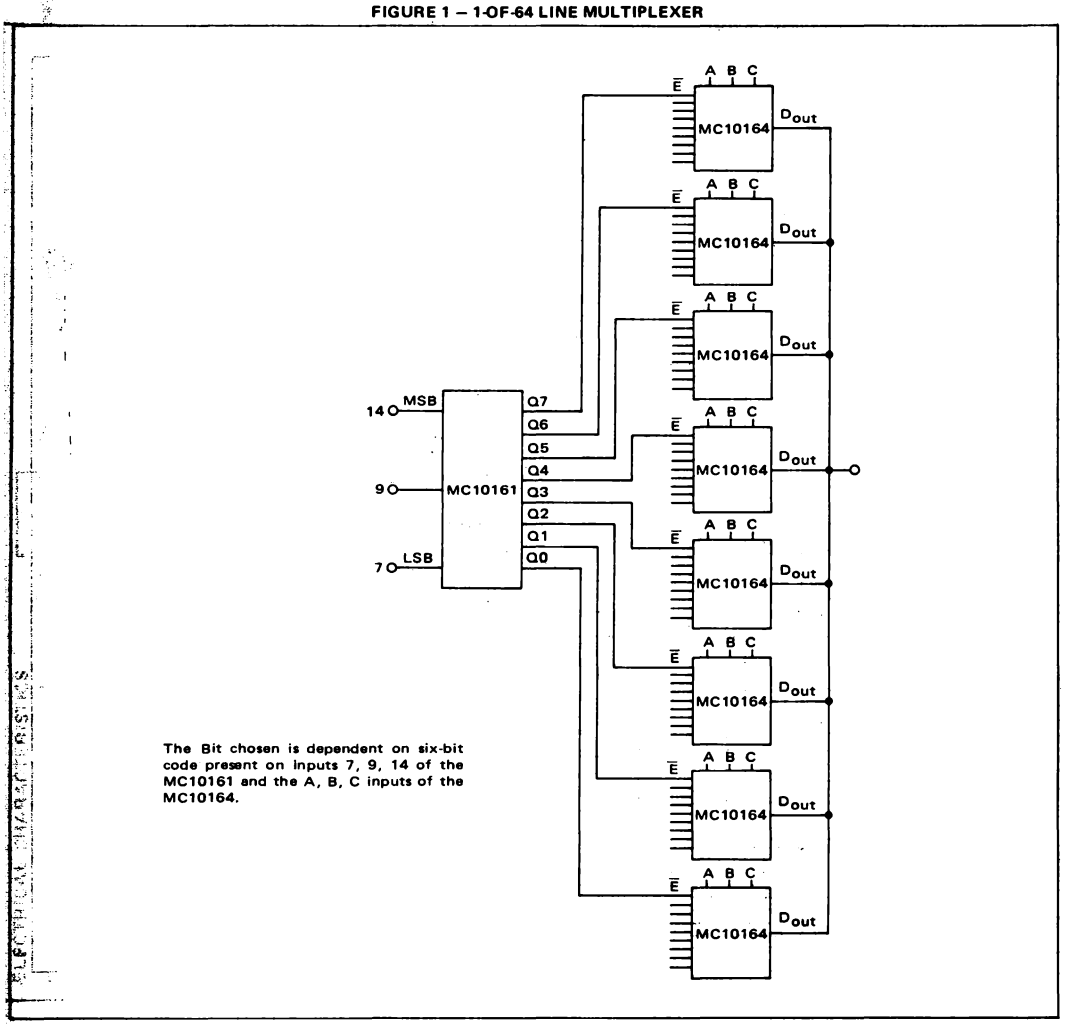


APPLICATION INFORMATION

The MC10164 can be used wherever data multiplexing and parallel to serial conversion is desirable. Full parallel clocking permits equal delays through any data path. The output of the MC10164 incorporates a buffer gate with eight data inputs and an enable. A high level on the enable forces the output low. The MC10164 can be connected directly to a data bus, due to its open emitter output and output enable.

Figure one illustrates how a 1-of-64 line multiplexer can be built with eight MC10164's wire ORed at their outputs and one MC10161 to drive the enables on each multiplexer, without speed degradation over a single MC10164 being experienced.

FIGURE 1 – 1-OF-64 LINE MULTIPLEXER



8-INPUT
PRIORITY ENCODER

MC10165

Advance Information

TRUTH TABLE

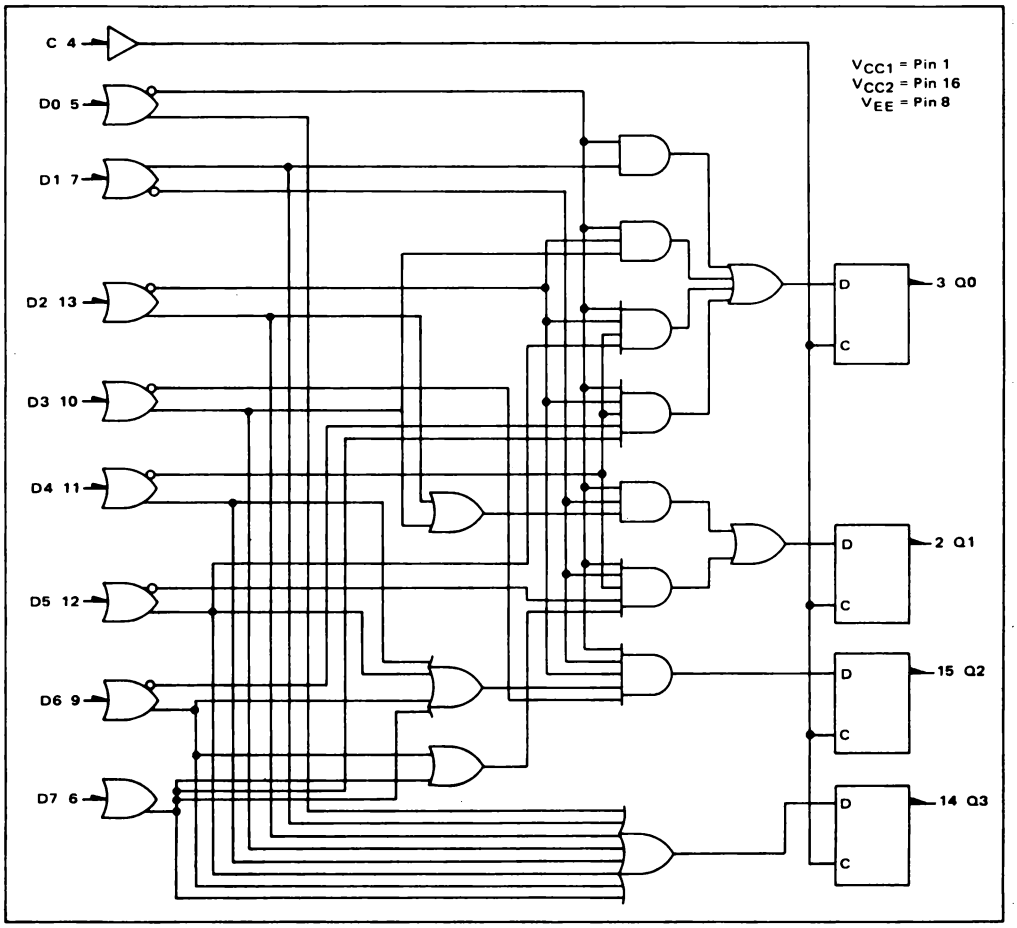
DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	L
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	H
L	L	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	H	L
L	L	L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H
L	L	L	L	H	ϕ	ϕ	ϕ	H	H	L	L
L	L	L	L	L	H	ϕ	ϕ	H	H	L	H
L	L	L	L	L	L	H	ϕ	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

ϕ = Don't Care

P_D = 545 mW typ/pkg (No Load)
t_{pd} = 7.0 ns typ (Data to Output)

The MC10165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

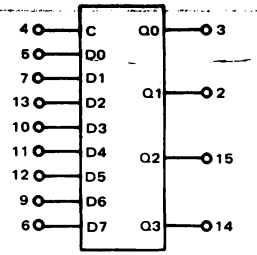
The input is active when high, (e.g. the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

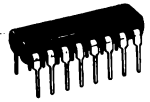


This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.





*** P SUFFIX**
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

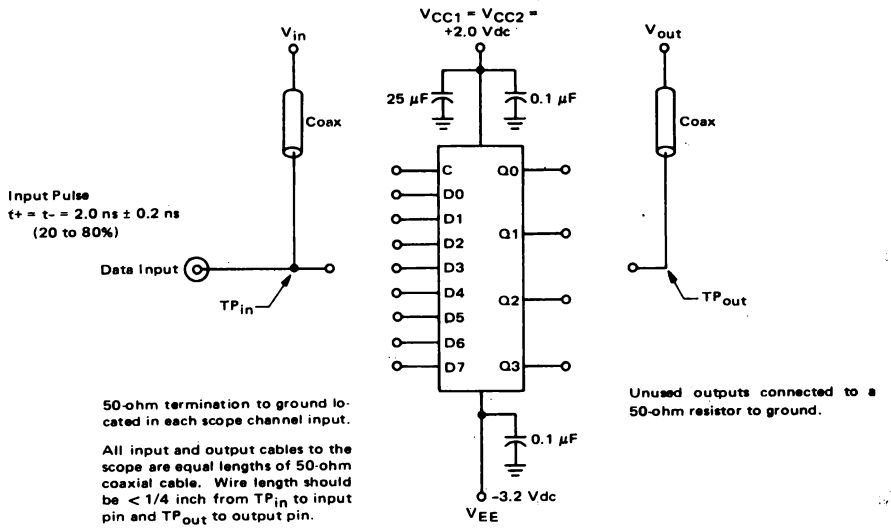
Characteristic	Symbol	Pin Under Test	MC10165 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	105	131	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	–	–	–	245	–	–	µAdc	4	–	–	–	8	1,16
		5	–	–	–	–	220	–	–	µAdc	5 ①	–	–	–	8	1,16
	$I_{in\ L}$	4	–	–	0.5	–	–	–	–	µAdc	–	4	–	–	8	1,16
		5	–	–	0.5	–	–	–	–	µAdc	–	5①	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	4	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700				–	–		
		14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700				–	–		
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700				–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	4	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–		–	–		
		14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–		–	–		
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–		–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	4	6	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–		–			–		
		14	-1.080	–	-0.980	–	–	-0.910	–		–			–		
		15	-1.080	–	-0.980	–	–	-0.910	–		–			–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	4	–	6	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595		–		–			
		14	–	-1.655	–	–	-1.630	–	-1.595		–		–			
		15	–	-1.655	–	–	-1.630	–	-1.595		–		–			
Switching Times (50-ohm Load)										Unit	+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data Input	t_{7+14+}	14	–	–	–	4.4	–	–	–	ns	–	4	7	14	8	1,16
	t_{11+15+}	15	–	–	–	6.5	–	–	–		–		11	15		
	t_{7+3+}	3	–	–	–	11.0	–	–	–		–		7	3		
	t_{13-2-}	2	–	–	–	7.0	–	–	–		–		13	2		
	t_{13+2+}	2	–	–	–	7.0	–	–	–		–		13	2		
Clock Input	t_{4+2+}	2 ②	–	–	–	3.5	–	–	–		7	–	4	3		
Setup Time	$t_{setup\ H}$	3	–	–	–	3.4	–	–	–		–	–	4,7	3		
	$t_{setup\ L}$		–	–	–	3.0	–	–	–		–	–				
Hold Time	$t_{hold\ H}$		–	–	–	-2.3	–	–	–		–	–				
	$t_{hold\ L}$		–	–	–	-2.7	–	–	–		–	–				
Rise Time (20% to 80%)	t_{3+}		–	–	–	2.0	–	–	–		–	4	7			
Fall Time (20% to 80%)	t_{3-}		–	–	–	2.0	–	–	–		–	4	7			

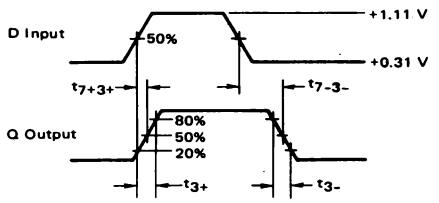
① The same limit applies for all D type input pins. To test input currents for other D inputs, individually apply proper voltage to pin under test.

② Output latched to low state prior to test.

* To preserve reliable performance, the MC10165P (plastic-packaged device only) is to be operated in ambient temperatures above 75°C only when 500 lfpm blown air or equivalent heat sinking is provided.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

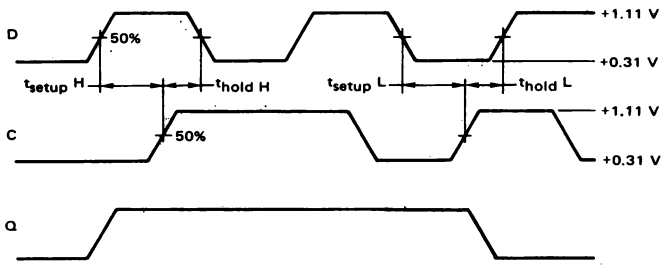




NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

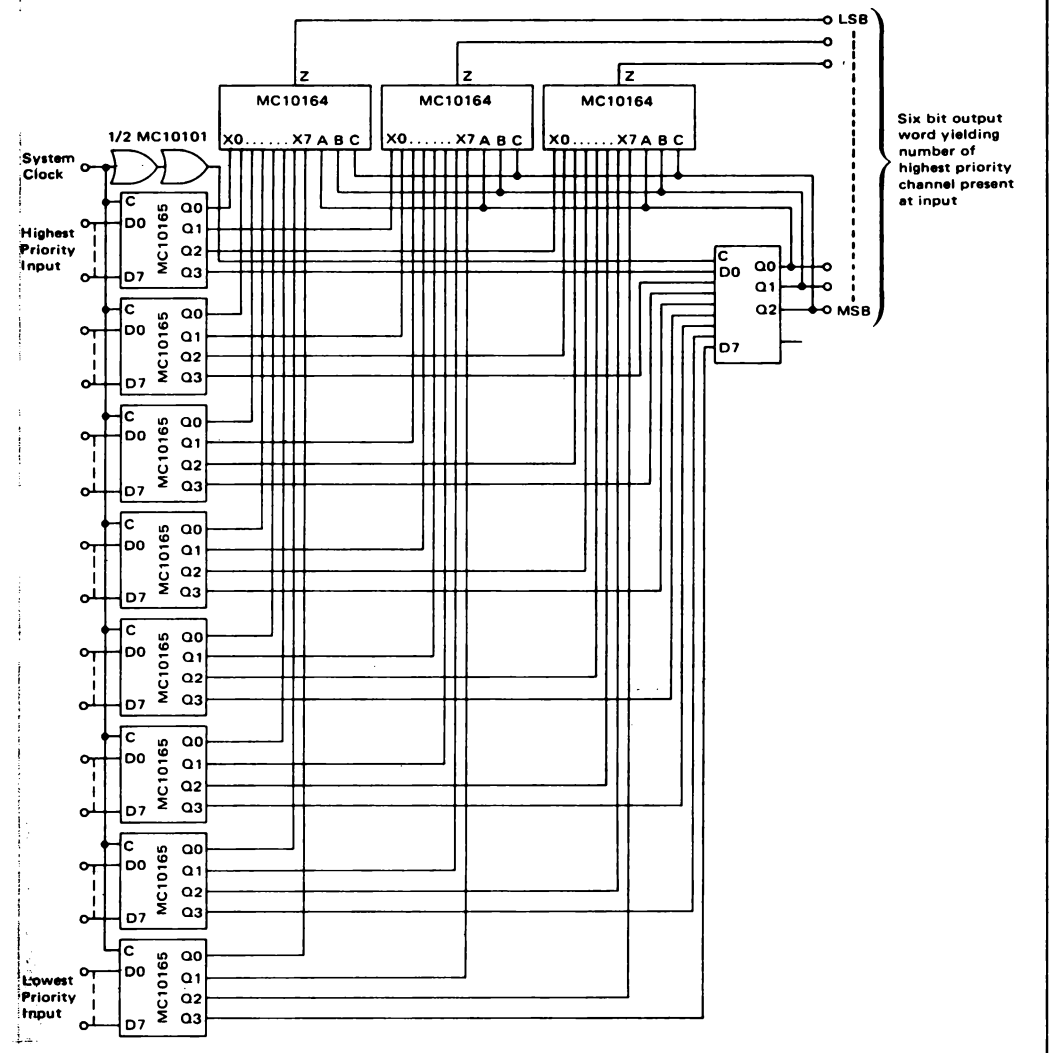
t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).



APPLICATION INFORMATION

A typical application of the MC10165 is the decoding of stem status on a priority basis. A 64 line priority encoder shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64-LINE PRIORITY ENCODER



5-BIT MAGNITUDE COMPARATOR

MC10166

Advance Information

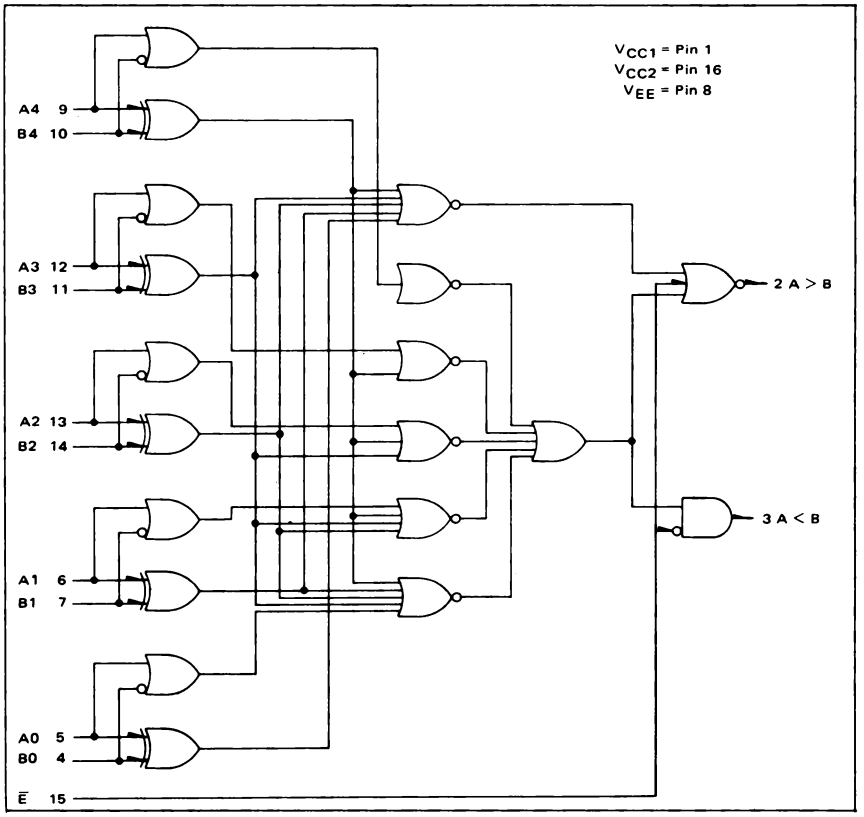
The MC10166 is a high speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A < B and A > B. A = B can be obtained by NORing the two outputs with an additional gate. A high level on the enable function forces both outputs low. Multiple MC10166s may be used for larger word comparisons.

TRUTH TABLE

Inputs			Outputs	
$\overline{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

P_D = 440 mW typ/pkg (No Load)
t_{pd} = Data to output 6.0 ns typ
$\overline{E}$ to output 2.5 ns typ

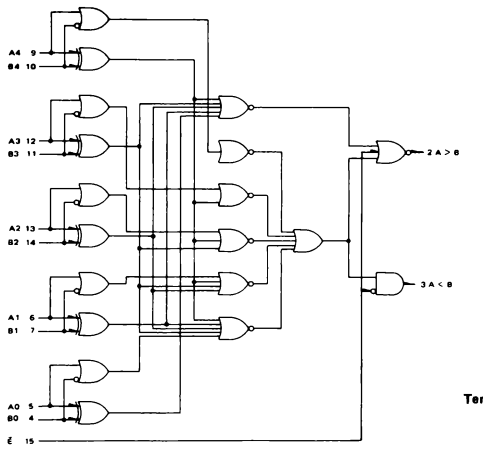
LOGIC DIAGRAM

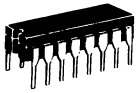


This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.



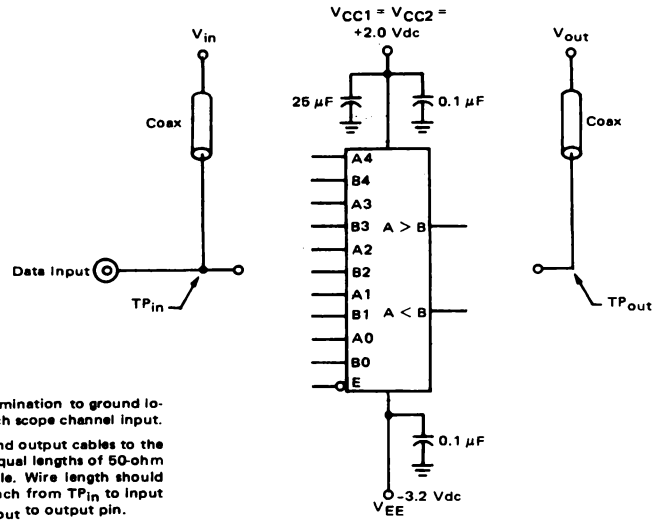


L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10166L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	85	106	–	–	mAdc	–	4,7,10,11,14	–	–	8	1,16
Input Current	I_{inH}	5	–	–	–	–	220	–	–	µAdc	5	–	–	–	8	1,16
	I_{inL}	5	–	–	0.5	–	–	–	–	µAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,15	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,15	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	5	–	–	15	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	4	–	–	15	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	5	–	15	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	4	–	15	–	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data to Output	t_{9+2+}	2	–	–	–	6.0	–	–	–	ns	–	–	9	2	8	1,16
	t_{9-2-}	2	–	–	–	↓	–	–	–	↓	–	–	9	2	↓	↓
	t_{11-2+}	2	–	–	–		–	–	–		12	–	11	2		
	t_{11+2-}	2	–	–	–		–	–	–		12	–	11	2		
	t_{7+3+}	3	–	–	–		–	–	–		6	–	7	3		
	t_{7-3-}	3	–	–	–		–	–	–		6	–	7	3		
Enable to Output	t_{15-3+}	3	–	–	–	2.5	–	–	–		10	–	15	3		
	t_{15+3-}	3	–	–	–	2.5	–	–	–		10	–	15	3		
Rise Time (20% to 80%)	t_{2+}	2	–	–	–	2.0	–	–	–		–	–	9	2		
Fall Time (20% to 80%)	t_{2-}	2	–	–	–	2.0	–	–	–	↓	–	–	9	2	↓	↓

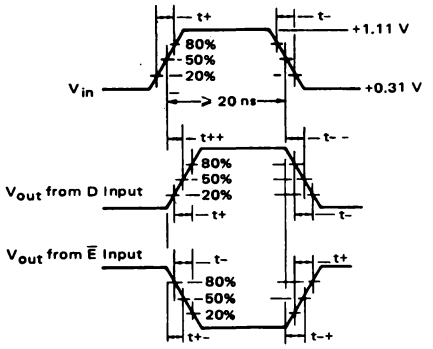
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

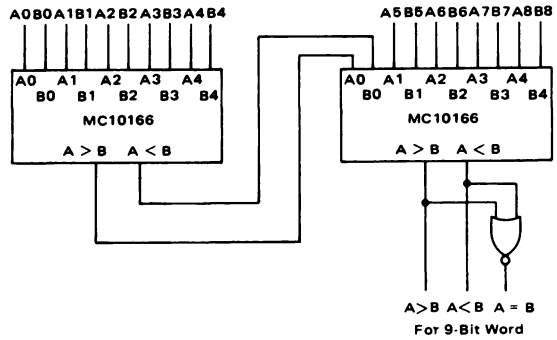
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs tied through a 50-ohm resistor to ground.



APPLICATION INFORMATION

FIGURE 1 – 9-BIT MAGNITUDE COMPARATOR



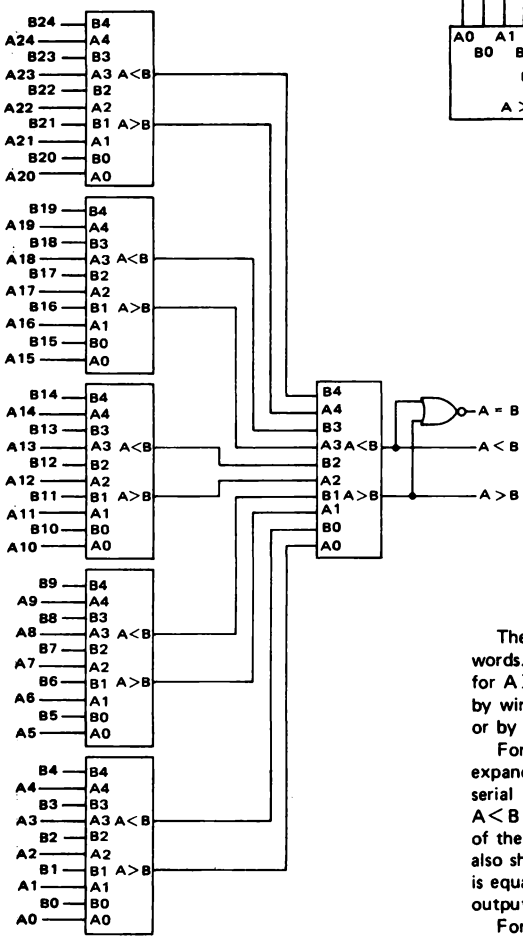


FIGURE 2 – 25-BIT MAGNITUDE COMPARATOR

The MC10166 compares the magnitude of two 5-bit words. Two outputs are provided which give a high level for A > B and A < B. The A = B function can be obtained by wire-ORing these outputs (a low level indicates A = B) or by NORing the outputs (a high level indicates A = B).

For longer word lengths, the MC10166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9-bit word length. The A > B and A < B outputs are fed to the A0 and B0 inputs respectively of the next device. The connection for an A = B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data-to-output delay.

For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25-bit cascaded comparator whose worst case delay is two data-to-output delays. The cascaded scheme can be extended to longer word lengths.

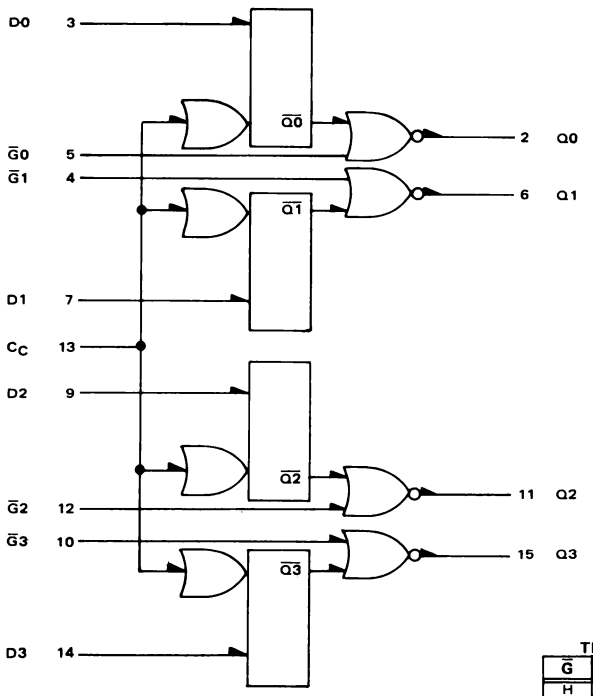
QUAD LATCH

MC10168

Advance Information

P_D = 310 mW typ/pkg (No Load)
t_{pd}: $\overline{G}$ to Q = 2 ns typ
D to Q = 3 ns typ
C to Q = 4 ns typ

The MC10168 is a Quad Latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative-going transition of the clock.



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

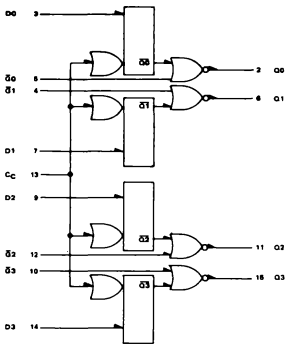
$\overline{G}$	C	D	Q_n+1
H	Ø	Ø	L
L	L	Ø	Q_n
L	H	L	L
L	H	H	H

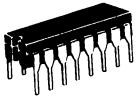
Ø = don't care

This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. The other inputs and outputs are tested in the same manner.





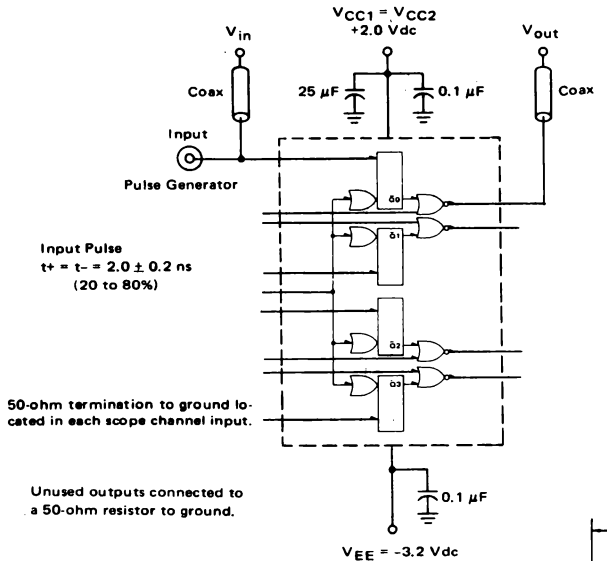
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-1.890	-1.890	-1.205	-1.500	-5.2
+25°C	-1.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

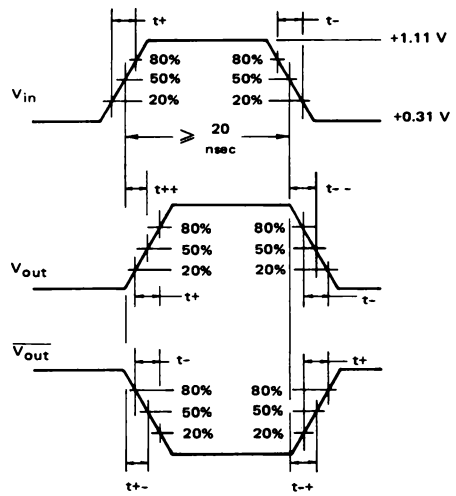
Characteristic	Symbol	Pin Under Test	MC10168L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	60	75	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	3,7,9,14	–	–	–	–	245	–	–	μAdc	*	–	–	–	8	1,16
		4,5,10,12	–	–	–	–	265	–	–	↓	*	–	–	–	↓	↓
		13	–	–	–	–	290	–	–		13	–	–	–		
	I_{inL}	*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,13	–	–	–	8	1,16
		6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	3,5	–	–	–	8	1,16
		6	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,7	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13	–	3	–	8	1,16
		6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13	–	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13	–	–	3	8	1,16
		6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13	–	–	7	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–	–	–	3.0	–	–	–	ns	–	–	3	2	8	1,16
	t_{5-2+}	2	–	–	–	2.0	–	–	–	↓	–	–	5	2	↓	↓
	t_{13+2+}	2	–	–	–	4.0	–	–	–		–	–	13	2		
Rise Time (20% to 80%)	t_{2+}	2	–	–	–	2.0	–	–	–		–	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	–	–	–	2.0	–	–	–		–	–	3	2		

*Individually test each input applying V_{IH} or V_{IL} to input under test.

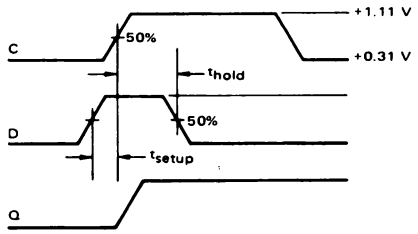
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



PROPAGATION DELAY



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.



t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D). Note that t_{hold} may be a negative number.

DUAL
BINARY TO 1-4-DECODER
(LOW)

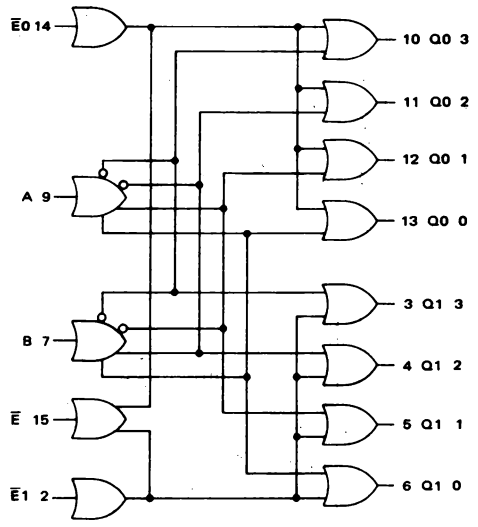
MC10171

The MC10171 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E}0$ or $\overline{E}1$ high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$, when high, forces all outputs high.

All propagation delay times are equal due to the internal emitter dotting techniques used. High impedance 50 k ohm resistors on all inputs eliminate the need to tie unused inputs to V_{EE}.

P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

POSITIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

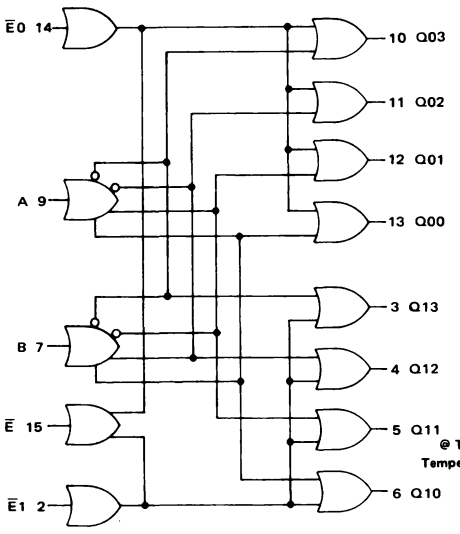
ENABLE INPUTS			INPUTS		OUTPUTS							
Ē	Ē0	Ē1	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

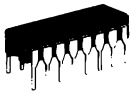
ϕ = Don't Care

See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test Procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





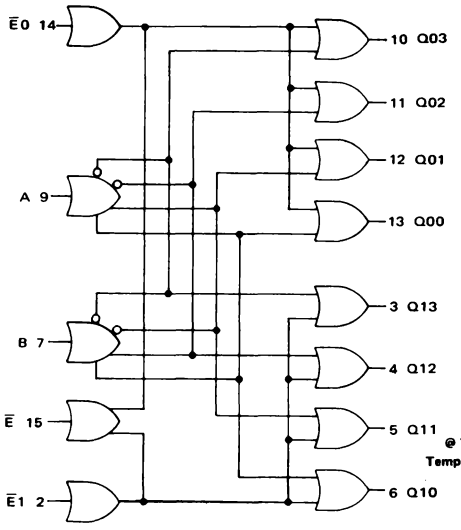
L SUFFIX
CERAMIC PACKAGE
CASE 620

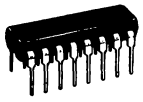
TEST VOLTAGE VALUES (Volts)				
V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-0.890	-1.890	-1.205	-1.500	-5.2
-0.810	-1.850	-1.105	-1.475	-5.2
-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10171L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	65	77	–	–	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	220	–	–	µAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	µAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	2,7,9,14,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,9,14,15	–	7	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,7,14,15	–	9	8	1,16
Switching Times (50 Ω Load)												+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6+}	6	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	–	2,9,14,15	7	6	8	1,16
	t_{7-6-}	6	↓	↓	↓	↓	↓	↓	↓		–	↓	↓	6	↓	↓
	t_{7+13+}	13												13		
	t_{7-13-}	13									–			13		
Rise Time (20% to 80%)	t_{6+}	6	1.0	3.3	1.1	2.0	3.3	1.1	3.4		–	–		6		
	t_{13+}	13									–	–		13		
Fall Time (20% to 80%)	t_{6-}	6									–	–		6		
	t_{13-}	13	↓	↓	↓	↓	↓	↓	↓		–	–	↓	13	↓	↓

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.



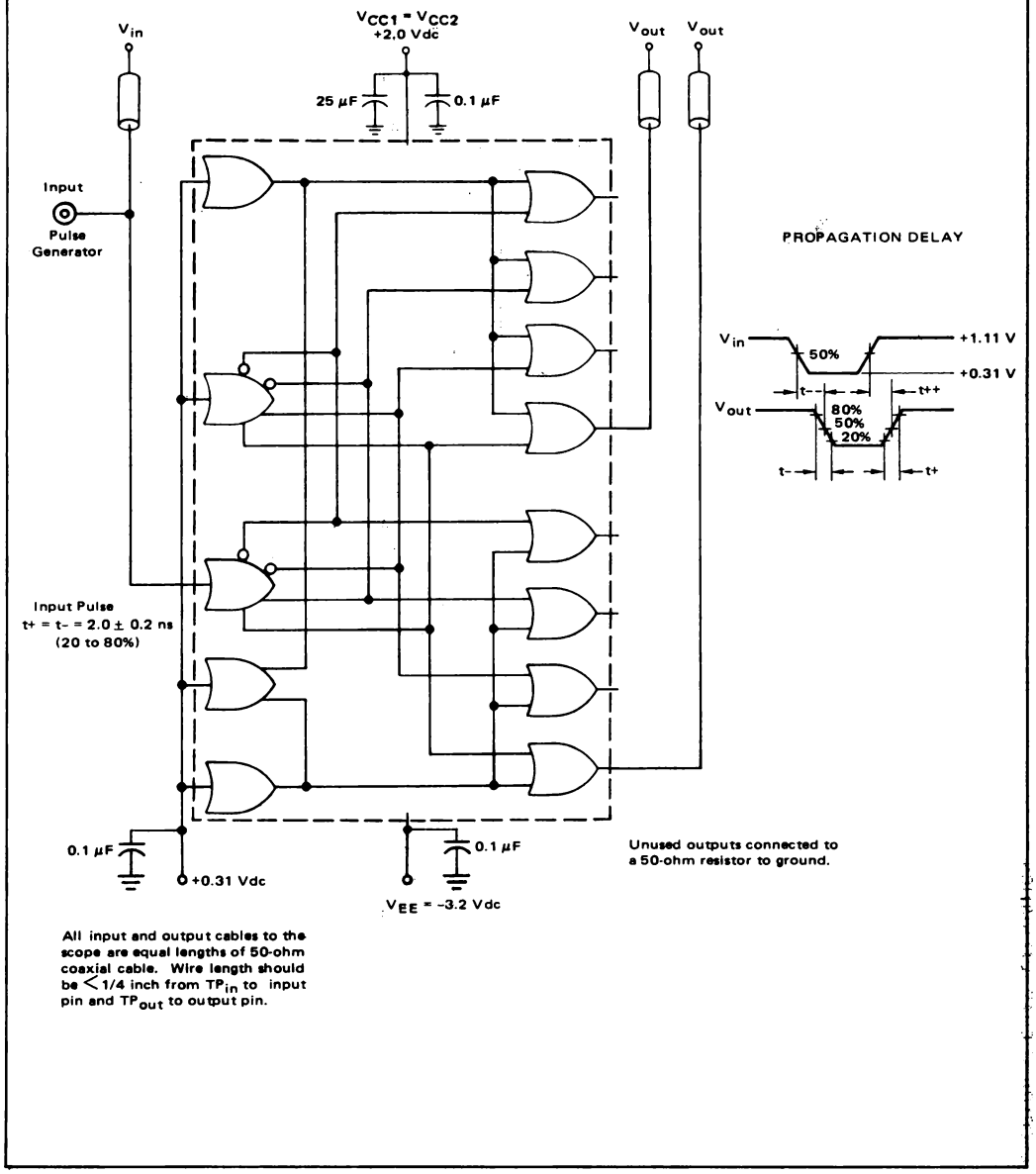


P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

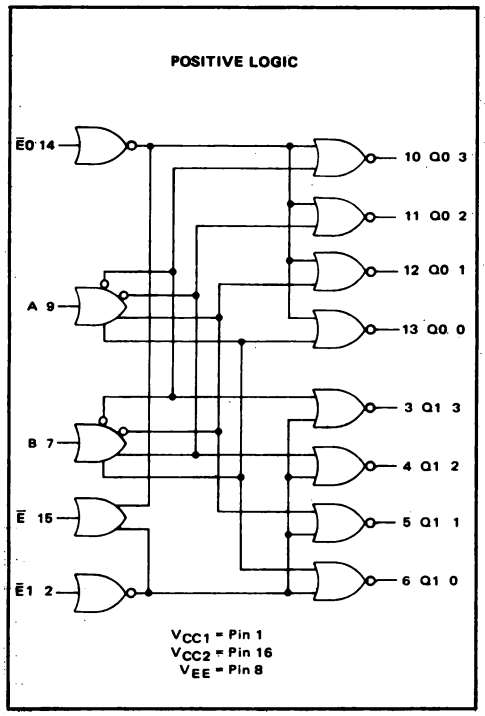
Characteristic	Symbol	Pin Under Test	MC10171P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	65	77	–	–	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	220	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	2,7,9,14,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,9,14,15	–	7	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,7,14,15	–	9	8	1,16
Switching Times (50 Ω Load)												+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6+}	6	–	–	1.5	4.0	6.0	–	–	ns	–	2,9,14,15	7	6	8	1,16
	t_{7-6-}	6	–	–	↓	↓	↓	–	–	↓	–	↓	↓	6	↓	↓
	t_{7+13+}	13	–	–	↓	↓	↓	–	–	↓	–	↓	↓	13	↓	↓
	t_{7-13-}	13	–	–	↓	↓	↓	–	–	↓	–	↓	↓	13	↓	↓
Rise Time (20% to 80%)	t_{6+}	6	–	–	1.1	2.0	3.3	–	–	↓	–	–	↓	6	↓	↓
	t_{13+}	13	–	–	↓	↓	↓	–	–	↓	–	–	↓	13	↓	↓
Fall Time (20% to 80%)	t_{6-}	6	–	–	↓	↓	↓	–	–	↓	–	–	↓	6	↓	↓
	t_{13-}	13	–	–	↓	↓	↓	–	–	↓	–	–	↓	13	↓	↓

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



DUAL
BINARY TO 1-4-DECODER
(HIGH)

MC10172



The MC10172 is a binary-coded 2 line to dual 4 line decoder with selected outputs high. With either $\overline{E}0$ or $\overline{E}1$ low, the corresponding selected 4 outputs are low. The common enable $\overline{E}$, when high, forces all outputs low.

All propagation delay times are equal. High impedance 50 k ohm resistors on all inputs eliminate the need to tie unused inputs to V_{EE}.

P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

TRUTH TABLE

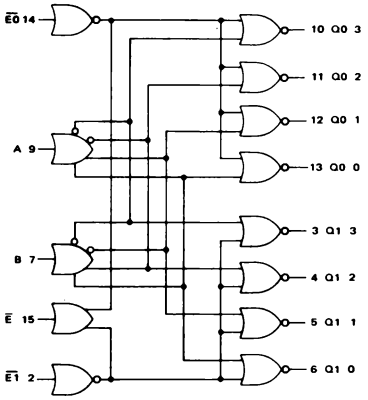
$\overline{E}$	$\overline{E}1$	$\overline{E}0$	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

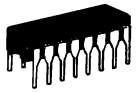
ϕ = Don't Care

See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





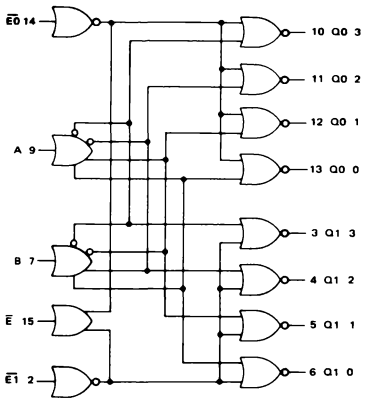
L SUFFIX
CERAMIC PACKAGE
CASE 620

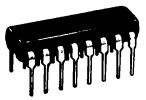
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10172L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	62	77	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	220	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	2	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	15	2,7,9,14	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	2	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,9,14	–	7	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,7,14	–	9	8	1,16
Switching Times (50 Ω Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6-}	6	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	2	9,14	7	6	8	1,16
	t_{7-6+}	6	↓	↓	↓	↓	↓	↓	↓	↓	2	9,14	↓	6	↓	↓
	t_{7+13-}	13	↓	↓	↓	↓	↓	↓	↓	↓	14	2,9	↓	13	↓	↓
	t_{7-13+}	13	↓	↓	↓	↓	↓	↓	↓	↓	14	2,9	↓	13	↓	↓
Rise Time (20% to 80%)	t_{6+}	6	1.0	3.3	1.1	2.0	3.3	1.1	3.4	↓	2	9,14	↓	6	↓	↓
	t_{13+}	13	↓	↓	↓	↓	↓	↓	↓	↓	14	2,9	↓	13	↓	↓
Fall Time (20% to 80%)	t_{6-}	6	↓	↓	↓	↓	↓	↓	↓	↓	2	9,14	↓	6	↓	↓
	t_{13-}	13	↓	↓	↓	↓	↓	↓	↓	↓	14	2,9	↓	13	↓	↓

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.



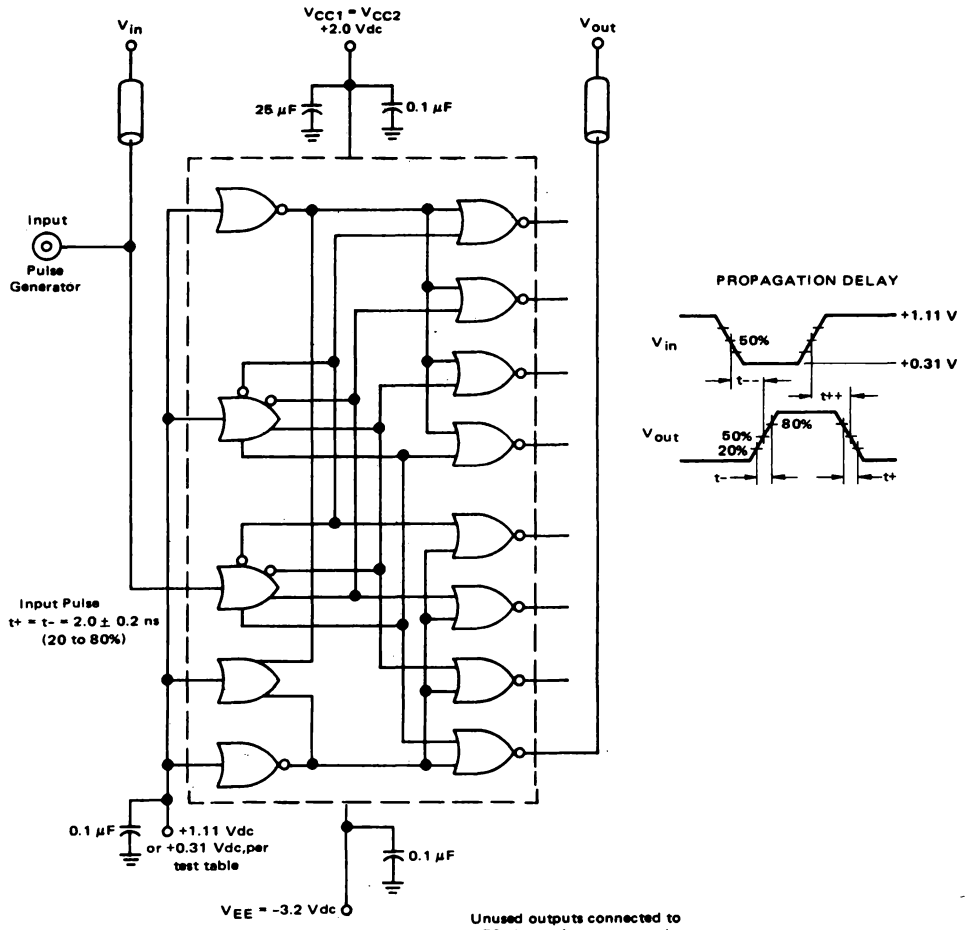


P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10172P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	62	77	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	220	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	2	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	15	2,7,9,14	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	2	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,9,14	–	7	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	-	2,7,14	–	9	8	1,16
Switching Times (50 Ω Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6-}	6	–	–	1.5	4.0	6.0	–	–	ns	2	9,14	7	6	8	1,16
	t_{7-6+}	6	–	–	↓	↓	↓	–	–	↓	2	9,14	↓	6	↓	↓
	t_{7+13-}	13	–	–	↓	↓	↓	–	–	↓	14	2,9	↓	13	↓	↓
	t_{7-13+}	13	–	–	↓	↓	↓	–	–	↓	14	2,9	↓	13	↓	↓
	t_{6+}	6	–	–	1.1	2.0	3.3	–	–	↓	2	9,14	↓	6	↓	↓
Rise Time (20% to 80%)	t_{13+}	13	–	–	↓	↓	↓	–	–	↓	14	2,9	↓	13	↓	↓
	t_{6-}	6	–	–	↓	↓	↓	–	–	↓	2	9,14	↓	6	↓	↓
Fall Time (20% to 80%)	t_{13-}	13	–	–	↓	↓	↓	–	–	↓	14	2,9	↓	13	↓	↓

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

MC10173

Advance Information

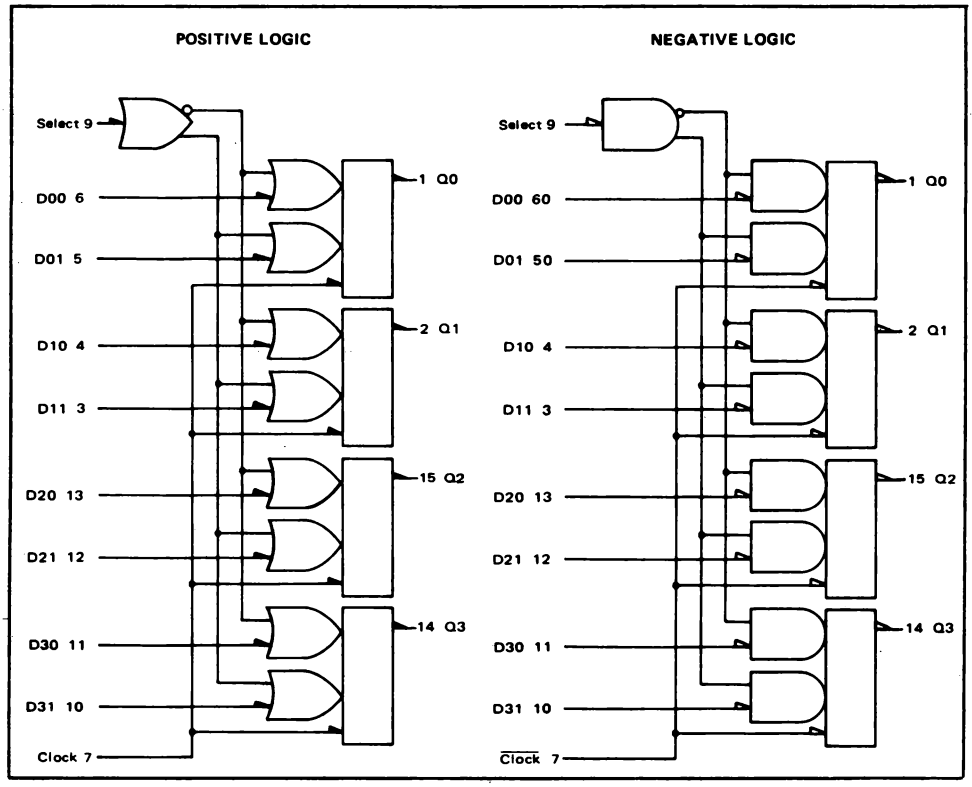
The MC10173 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

TRUTH TABLE

SELECT	CLOCK	$Q0_{n+1}$
H	L	D00
L	L	D01
ϕ	H	$Q0_n$

ϕ = Don't Care

P_D = 275 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

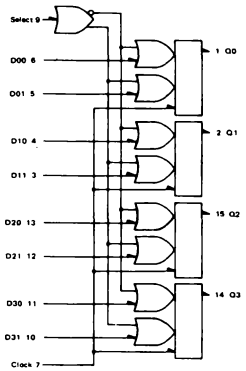


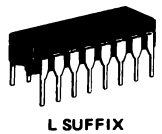
V_{CC} = Pin 16
V_{EE} = Pin 8

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.





L SUFFIX
CERAMIC PACKAGE
CASE 620

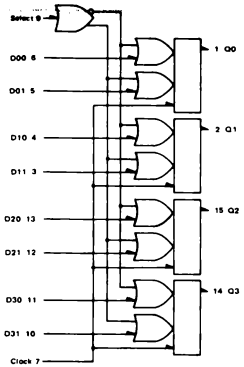
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

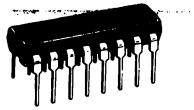
Characteristic	Symbol	Pin Under Test	MC10173L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	66	–	–	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	5	–	–	–	–	295	–	–	μAdc	5	–	–	–	8	16
		6	–	–	–	–	295	–	–		6	–	–	–		
		7	–	–	–	–	250	–	–		7	–	–	–		
		9	–	–	–	–	250	–	–		9	–	–	–		
Input Leakage Current	I_{inL}	All	–	–	0.5	–	–	–	–	μAdc	–	•	–	–	8	16
Logic "1" Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6,9	7	–	–	8	16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	7	–	–	8	16
Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	7	–	–	8	16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	7	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	7	6	–	8	16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	7	5	–	8	16
Logic "0" Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	7	–	6	8	16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	7	–	5	8	16
Switching Times											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay																
Data Input	t_{6+1+}	1	0.8	3.7	1.0		3.5	1.1	5.3	ns	9	7	6	1	8	16
	t_{6-1-}										9		6			
	t_{5+1+}										–		5			
	t_{5-1-}										–		5			
Clock Input	t_{7-1+}		1.6	7.2	1.6		6.8	1.4	6.8		–	–	5,7			
	t_{7-1-}		1.6	7.2	1.6		6.8	1.4	6.8		–	–	5,7			
Select Input	t_{9+1+}		1.1	6.2	1.3		5.7	1.2	6.7		6	7	9			
	t_{9+1-}										5					
	t_{9-1+}										5					
	t_{9-1-}										6					
Setup Time																
Data Input	t_{setup}		–	–	2.0		–	–	–		–	–	5,7			
Select Input	t_{setup}		–	–	3.0		–	–	–		6	–	7,9			
Hold Time																
Data Input	t_{hold}		–	–	2.5		–	–	–		–	–	5,7			
Select Input	t_{hold}		–	–	1.5		–	–	–		6	–	7,9			
Rise Time (20 to 80%)	t_+		1.2	4.0	1.5		3.5	1.4	4.0		5	–	7			
Fall Time (20 to 80%)	t_-		1.2	4.0	1.5		3.5	1.4	4.0		–	–	7			

*V_{ILmin} applied to each input pin, one at a time.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.





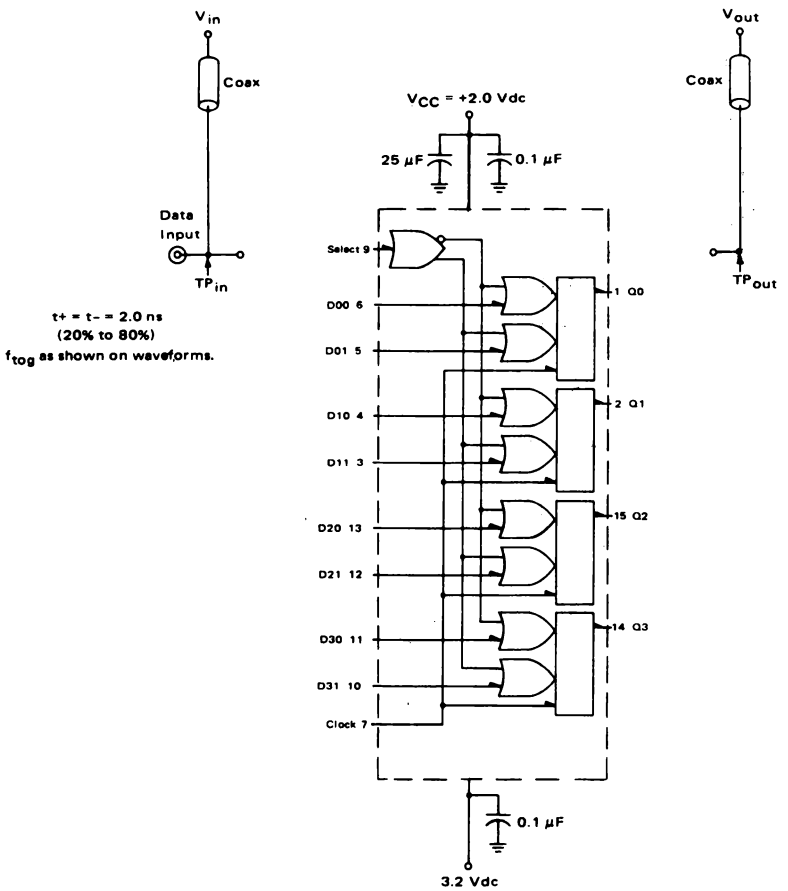
P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10173P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	66	–	–	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	5	–	–	–	–	295	–	–	μAdc	5	–	–	–	8	16
		6	–	–	–	–	295	–	–		6	–	–	–		
		7	–	–	–	–	250	–	–		7	–	–	–		
		9	–	–	–	–	250	–	–		9	–	–	–		
Input Leakage Current	I_{inL}	All	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	16
Logic "1" Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6,9	7	–	–	8	16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	7	–	–	8	16
Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	7	–	–	8	16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	7	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	7	6	–	8	16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	7	5	–	8	16
Logic "0" Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	7	–	6	8	16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	7	–	5	8	16
Switching Times											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay																
Data Input	t_{6+1+}	1	–	–	–	2.5	–	–	–	ns	9	7	6	1	8	16
	t_{6-1-}		–	–	–		–	–	–		9		6			
	t_{5+1+}		–	–	–		–	–	–		–		5			
	t_{5-1-}		–	–	–		–	–	–		–		5			
Clock Input	t_{7-1+}		–	–	–	4.5	–	–	–		–	–	5,7			
	t_{7-1-}		–	–	–	4.5	–	–	–		–	–	5,7			
Select Input	t_{9+1+}		–	–	–	3.5	–	–	–		6	7	9			
	t_{9+1-}		–	–	–		-	–	–		5					
	t_{9-1+}		–	–	–		–	–	–		5					
	t_{9-1-}		–	–	–		–	–	–		6					
Setup Time																
Data Input	t_{setup}		–	–	–	1.5	–	–	–		–	–	5,7			
Select Input	t_{setup}		–	–	–	2.5	–	–	–		6	–	7,9			
Hold Time																
Data Input	t_{hold}		–	–	–	0.0	–	–	–		–	–	5,7			
Select Input	t_{hold}		–	–	–	-0.5	–	–	–		6	–	7,9			
Rise Time (20 to 80%)	t+		–	–	–	2.0	–	–	–		5	–	7			
Fall Time (20 to 80%)	t-		–	–	–	2.0	–	–	–		–	–	7			

*V_{ILmin} applied to each input pin, one at a time.

SWITCHING TIMES TEST CIRCUIT



t+ = t- = 2.0 ns
(20% to 80%)
f_{tog} as shown on waveforms.

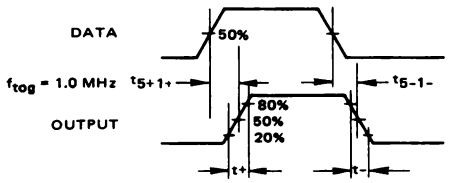
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

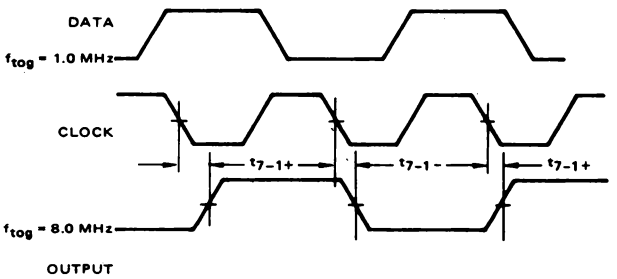
Unused outputs are connected to 50-ohm resistor to ground.

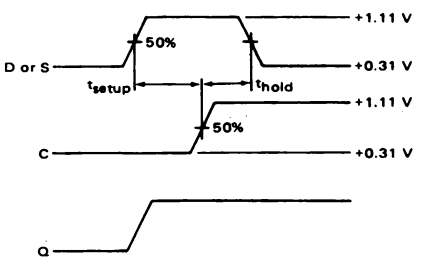
WAVEFORMS @ 25°C

DATA TO OUTPUT WITH CLOCK AT V_{IL}



CLOCK TO OUTPUT





NOTE:

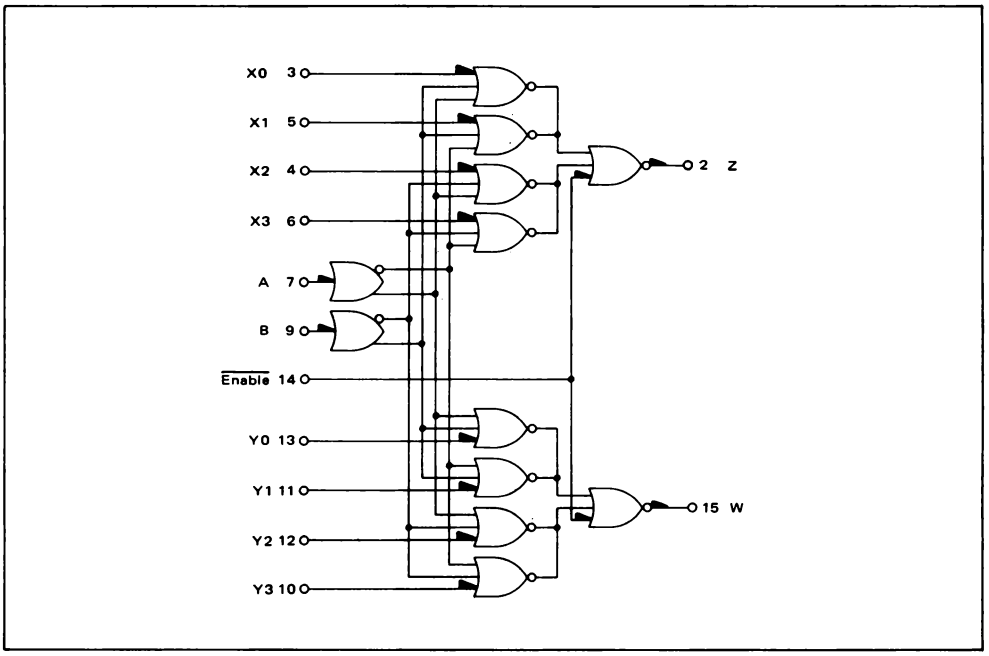
t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input (D) or (S).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D) or (S).

MC10174

The MC10174 is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state. The enable is also useful in wire-ORing several multiplexers to achieve additional channel capability. Delay from data input to output is typically 3.5 nanoseconds.

P_D = 305 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (Data to output)



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

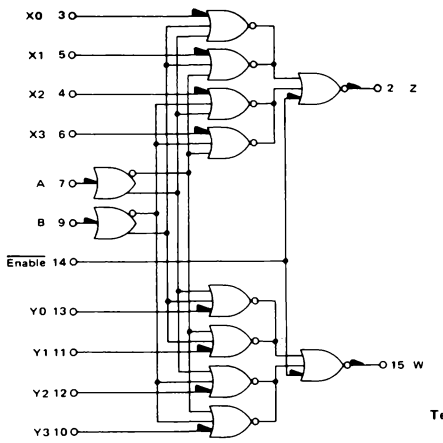
ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Z	W
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

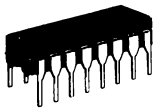
ϕ = Don't Care

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.



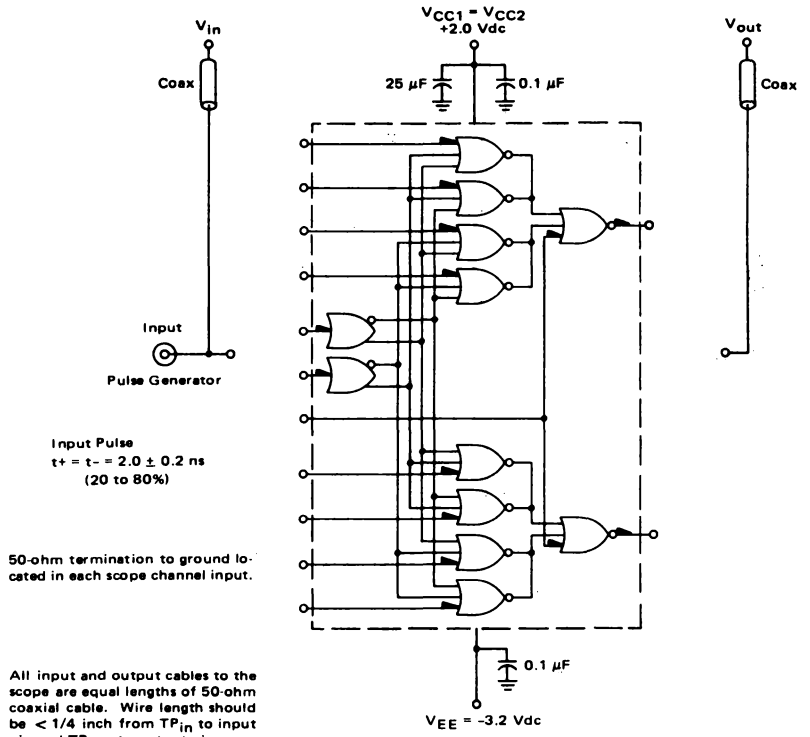


L SUFFIX
CERAMIC PACKAGE
CASE 620

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10174L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	58	73	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	–	–	–	220	–	–	μAdc	4	–	–	–	8	1,16
		14	–	–	–	–	330	–	–		14	–	–	–	8	1,16
	$I_{in\ L}$	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	13	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630		-1.595	Vdc	–	–	14	–	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{13+15+}	15	1.4	4.8	1.5	3.5	4.5	1.4	4.8	ns	–	–	13	15	8	1,16
	t_{13-15-}	15	1.4	4.8	1.5	3.5	4.5	1.4	4.8		–	–	13			
	t_{7+15-}	15	1.9	6.4	2.0	5.0	6.0	2.1	6.4		11	–	7			
	t_{7-15+}	15	1.9	6.4	2.0	5.0	6.0	2.1	6.4		11	–	7			
	t_{14+15-}	15	1.0	3.1	1.0	2.0	2.9	0.9	3.2		13	–	14			
	t_{14-15+}	15		3.1	1.0	2.0	2.9	0.9	3.2			–	14			
Rise Time (20% to 80%)	t+	15		3.4	1.1	2.0	3.3	1.1	3.6			–	14			
Fall Time (20% to 80%)	t-	15		3.4	1.1	2.0	3.3	1.1	3.6			–	14			

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



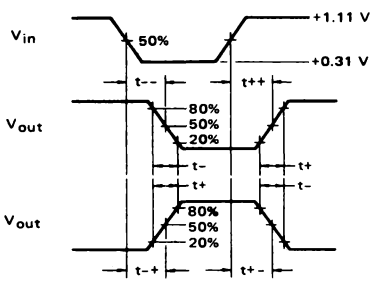
Input Pulse
$t+ = t- = 2.0 \pm 0.2$ ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused output connected to a 50-ohm resistor to ground.

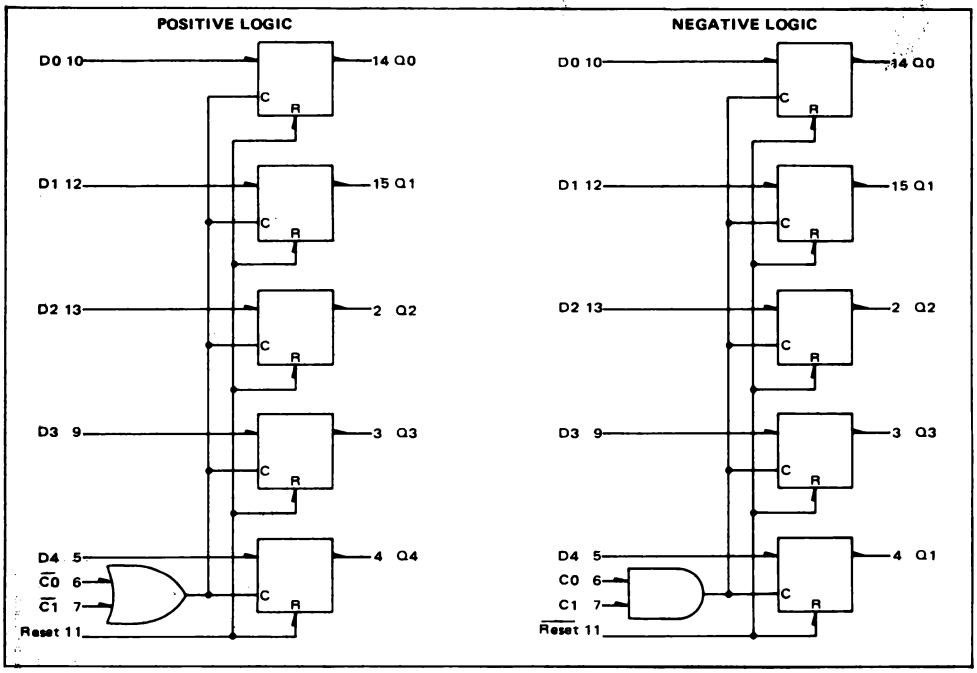
PROPAGATION DELAY



The MC10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together. Propagation delays are typically 2.5 nanoseconds from each data input to the output.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

The MC10175 allows storage of five bits of information, and it is useful in temporary storage applications in high speed central processors, accumulators, register files, digital communication systems, instrumentation, and test equipment.



TRUTH TABLE

D	C0	C1	Reset	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Q n
X	X	H	L	Q n
X	H	X	H	L
X	X	H	H	L

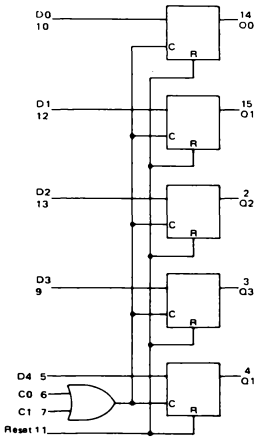
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

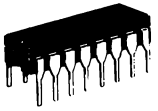
P_D = 400 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Output)

See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





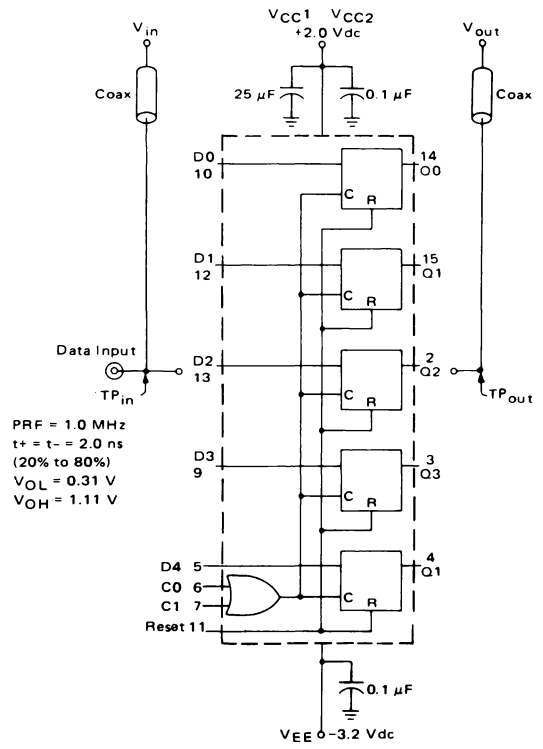
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10175L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	78	97	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6	–	–	–	–	290	–	–	μAdc	6	–	–	–		
		7	–	–	–	–	290	–	–	↓	7	–	–	–		
		10	–	–	–	–	290	–	–		10	–	–	–	↓	↓
		11	–	–	–	–	650	–	–		11	–	–	–		
Input Leakage Current	I_{inL}	All	–	–	0.5	–	–	–	–	μAdc	–	①	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	10	6	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	6	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,10	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,12	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	14	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	6	10	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	6	12	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	14	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	6	–	10	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	6	–	12	8	1,16
Switching Times											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Data Input	t_{10+14+}	14	1.0	3.6	1.0	–	3.5	1.0	3.6	ns	–	6,7	10	14	8	1,16
	t_{10-14-}			3.6		–	3.5		3.6		–	6,7	10			
Clock Input	t_{6-14+}	↓	↓	4.7	↓	–	4.3	↓	4.4	↓	–	7	10,6	↓	↓	↓
	t_{6-14-}			4.7		–	4.3		4.4		–	7	10,6			
Reset Input	t_{11+4-}	4	0.9	4.0	1.0	–	3.9	1.0	4.2	ns	5	6	7,11	4 ②	8	1,16
	t_{11+14-}	14	0.9	4.0	1.0	–	3.9	1.0	4.2	↓	10	6	7,11	14 ②	8	1,16
Setup Time	t_{setup}	14	–	–	2.5	–	–	–	–	ns	–	7	6,10	14	8	1,16
Hold Time	t_{hold}	14	–	–	1.5	–	–	–	–		–	7	6,10			
Rise Time (20 to 80%)	t+	14	1.0	3.6	1.1	–	3.5	1.1	3.7	↓	–	6,7	10	↓	↓	↓
Fall Time (20 to 80%)	t-	14	1.0	3.6	1.1	–	3.5	1.1	3.7		–	6,7	10			

① Individually test each input; apply $V_{IL\ min}$ to pin under test.
② Output latched to high logic state prior to test.

SWITCHING TIME TEST CIRCUIT

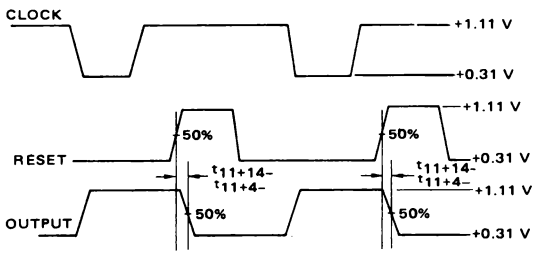


50-ohm termination to ground located in each scope channel input.

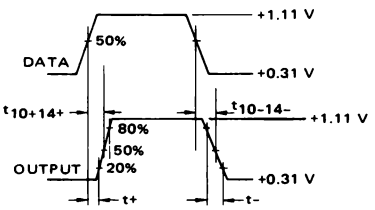
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

VOLTAGE WAVEFORMS

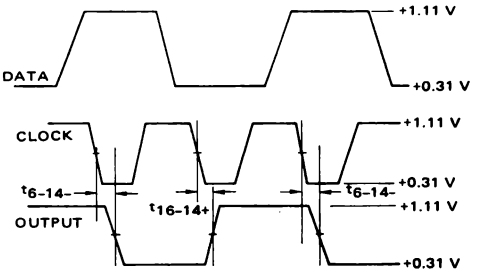
RESET INPUT

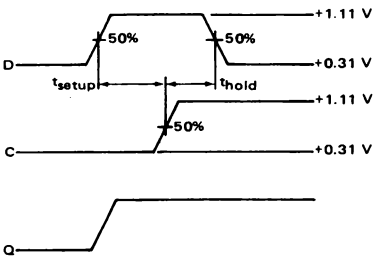


DATA INPUT



CLOCK INPUT





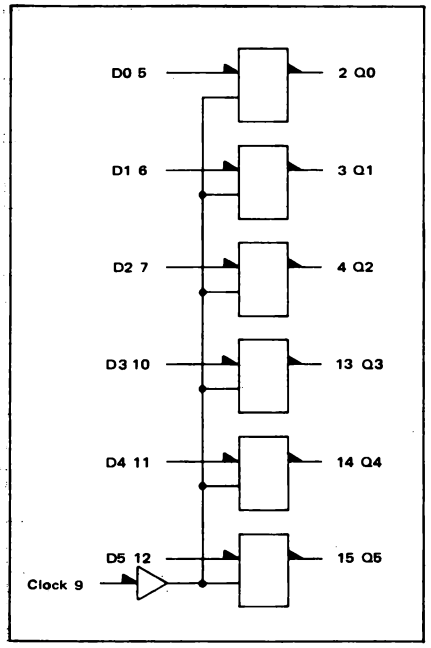
NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

P_D = 460 mW typ/pkg (No Load)
f_{toggle} 150 MHz (typ)

The MC10176 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a postive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

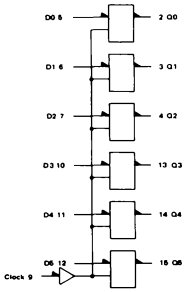
ϕ = Don't Care

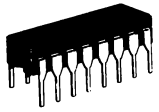
*A clock H is a clock transition from a low to a high state.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one data input, and the clock input, and for one output. Other inputs and outputs tested in the same manner.





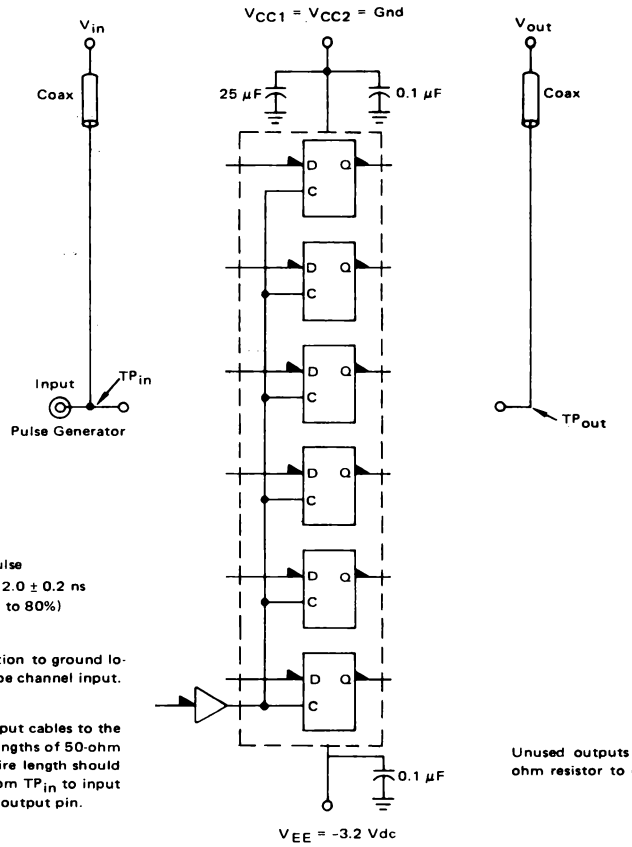
L SUFFIX
CERAMIC PACKAGE
CASE 620

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10176L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	88	110	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	5	–	–	–	–	220	–	–	µAdc	5	–	–	–	8	1,16
		9	–	–	–	–	310	–	–		9	–	–	–	8	1,16
Input Leakage Current	I_{inL}	5	–	–	0.5	–	–	–	–	µAdc	–	5	–	–	8	1,16
		9	–	–	0.5	–	–	–	–	µAdc	–	9	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
		15†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	5	–	–	8	1,16
		15†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	12	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		15†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	12	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		15†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	12	8	1,16
Switching Times											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{9+2+}	2	1.4	4.6	1.5	–	4.5	1.5	5.0	ns	–	–	5,9	2	8	1,16
	t_{9+2-}	2	1.4	4.6	1.5	–	4.5	1.5	5.0		–	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.1	1.1	–	4.0	1.1	4.4		–	–				
Fall Time (20 to 80%)	t_{2-}	2	1.0	4.1	1.1	–	4.0	1.1	4.4		–	–				
Setup Time	t_{setup}	2	–	–	2.5	–	–	–	–	ns	–	–	5.9	2	8	1,16
Hold Time	t_{hold}	2	–	–	1.5	–	–	–	–	ns	–	–	5,9	2	8	1,16
Toggle Frequency	f_{tog}	2	–	–	125	150	–	–	–	MHz	–	–	–	–	8	1,16

† Output level to be measured after a clock pulse has been applied to C input (pin 9). $V_{IH\ max}$ $V_{IL\ min}$

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



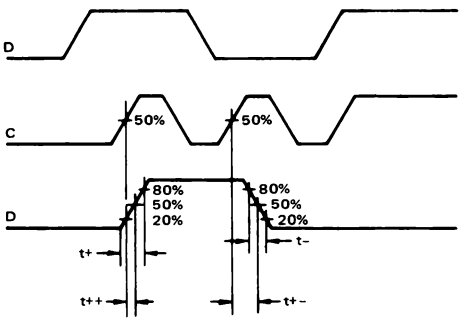
Input Pulse
t+ = t-= 2.0 ± 0.2 ns
(20 to 80%)

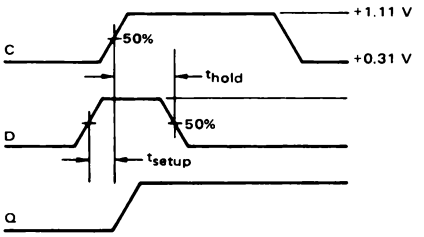
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are tied to a 50-ohm resistor to ground.

PROPAGATION DELAY





t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D). Note that t_{hold} may be a negative number.

TRIPLE MECL TO
NMOS TRANSLATOR

MC10177

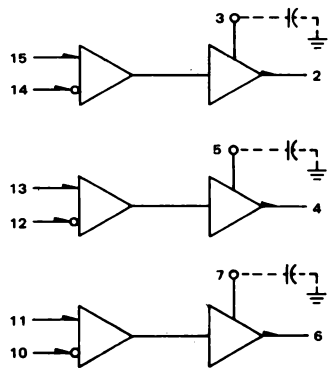
Advance Information

- Max Load: 350 pF
- P_D = 1.0 W typ/pkg @ 5.0 MHz
- Operating Rate: 5.0 MHz typ.
  (all 3 translators in use simultaneously)
- INPUT: MECL 10,000 (differential)
- OUTPUT: NMOS + 0.5 V V_{OLmax}
  + 3.0 V V_{OHmin}*

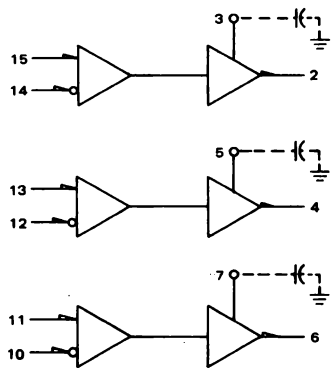
*May be raised by increasing V_{SS}.

The MC10177 consists of three MECL to MOS translators which convert MECL 10,000 logic levels to NMOS levels. It is designed for use in N-channel memory systems as a Read/Write, Data/Address driver. It may also be used as a high fanout (30) MECL to TTL translator, or in other applications requiring the capability to drive high capacitive loads. A separate lead from each of the three translators is brought out of the package. These leads may be connected to V_{SS} or to an external capacitor (0.01 to 0.05 μF to ground), for waveform improvement, and short circuit protection. When connection is made to an external capacitor, V_{SS} line fluctuations due to transient currents are also reduced.

POSITIVE LOGIC



NEGATIVE LOGIC



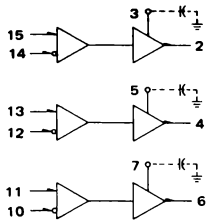
V_{CC} = Gnd = Pins 1,16
V_{EE} = Pin 8 = -5.2 Vdc ±5%
V_{SS} = Pin 9 (+5.0 Vdc or +6.0 Vdc ± 10%)

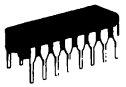
This is advance information and specifications are subject to change without notice.
See General Information section of packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

In general test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner.





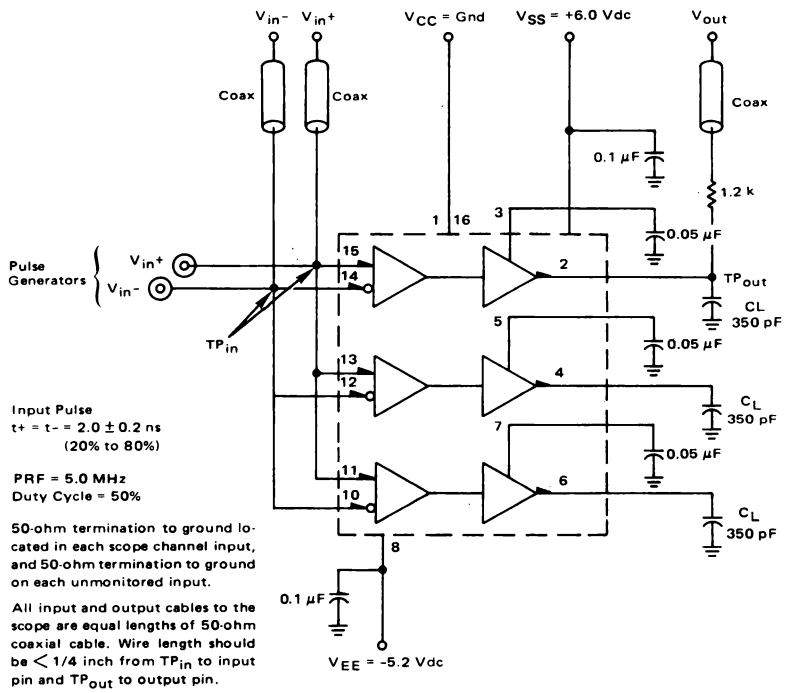
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES: Volts V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{SC}	V_{SS}	mAdc ±1% I_{OL1}	I_{OL2}	I_{OH}	µF ±5% C#
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+5.0	+6.0	+1.0	+20	-15	0.05
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+5.0	+6.0	+1.0	+20	-15	0.05
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+5.0	+6.0	+1.0	+20	-15	0.05

Characteristic	Symbol	Pin Under Test	MC10177L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{SC}	V_{SS}	I_{OL1}	I_{OL2}	I_{OH}	C#	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	–	–	–	96	–	–	mAdc	–	–	–	–	8	–	–	–	–	–	–	1,16
Negative Output Low	I_{SSO}	9	–	–	–	–	88	–	–	mAdc	–	–	–	–	8	9	–	–	–	–	–	1,16
Positive Output Low	I_{SSL}	9	–	–	–	–	88	–	–	↓	10,12,14	11,13,15	–	–	↓	↓	–	–	–	–	–	↓
Positive Output High	I_{SSH}	9	–	–	–	–	44	–	–		11,13,15	10,12,14	–	–			–	–	–	–	–	
Input Current	I_{inH}	10	–	–	–	–	1.0	–	–	µAdc	10	11	–	–	8	9	–	–	–	–	–	1,16
		11	–	–	–	–	↓	–	–	↓	11	10	–	–	↓	↓	–	–	–	–	–	↓
		12	–	–	–	–		–	–		12	13	–	–			–	–	–	–	–	
		13	–	–	–	–		–	–		13	12	–	–			–	–	–	–	–	
		14	–	–	–	–		–	–		14	15	–	–			–	–	–	–	–	
		15	–	–	–	–		–	–		15	14	–	–			–	–	–	–	–	
Input Leakage Current	I_{CBO}	11	–	–	-1.0	–	–	–	–	µAdc	10	–	–	–	8,11	9	–	–	–	–	–	1,16
		13	–	–	↓	–	–	–	–	↓	12	–	–	–	8,13	↓	–	–	–	–	–	↓
		15	–	–		–	–	–	–		14	–	–	–	8,15		–	–	–	–	–	
Logic "1" Output Voltage	V_{OH}	2	3.0	–	3.0	–	–	3.0	–	Vdc	15	14	–	–	8	9	–	–	–	2	–	1,16
		2	4.0	–	4.0	–	–	4.0	–	Vdc	15	14	–	–	8	–	9	–	–	2	–	1,16
Logic "0" Output Voltage	V_{OL}	2	–	0.5	–	–	0.5	–	0.5	Vdc	14	15	–	–	8	9	–	2	–	–	–	1,16
		2	–	0.6	–	–	0.6	–	0.6	Vdc	14	15	–	–	8	9	–	–	2	–	–	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	3.0	–	3.0	–	–	3.0	–	Vdc	–	14	15	–	8	9	–	–	–	2	–	1,16
		2	4.0	–	4.0	–	–	4.0	–	Vdc	–	14	15	–	8	–	9	–	–	2	–	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	0.5	–	–	0.5	–	0.5	Vdc	14	–	–	15	8	9	–	2	–	–	–	1,16
		2	–	0.6	–	–	0.6	–	0.6	Vdc	14	–	–	15	8	9	–	–	2	–	–	1,16
Output Short-Circuit Current	I_{SC}	2	-50	-90	-50	–	-90	-50	-90	mAdc	15	14	–	–	8	9	–	–	–	–	–	1,2,16
											-1.29 V	-1.69 V	Pulse In	Pulse Out	-5.2 V							
Switching Times (350 pF Load)	t_{15+2+}	2	–	–	–	6.0	–	–	–	ns	14	11,13	15	2	8	9	–	–	–	–	3,5,7	1,16
	t_{15-2-}	2	–	–	–	↓	–	–	–	↓	14	↓	15	↓	↓	↓	–	–	–	–	↓	↓
Propagation Delay	t_{14+2-}	2	–	–	–		–	–	–		15		14				–	–	–	–		
	t_{14-2+}	2	–	–	–		–	–	–		15		14				–	–	–	–		
Rise Time (10% to 90%)	t_{2+}	2	–	–	–	12	–	–	–		14		15				–	–	–	–		
Fall Time (10% to 90%)	t_{2-}	2	–	–	–	12	–	–	–		14		15				–	–	–	–		
Supply Source Current (@ 5.0 MHz) (350 pF Load)	I_{SS}	9	–	–	–	83	–	–	–	mA	10,12,14	–	11,13,15	–	8	–	9	–	–	–	3,5,7	1,16

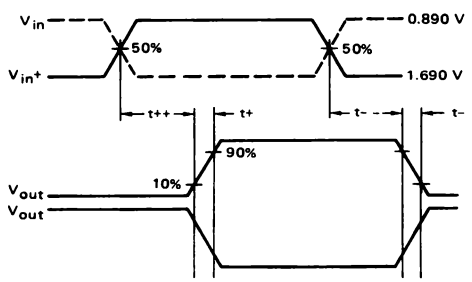
#See test circuit.

SWITCHING TIME TEST CIRCUIT



SWITCHING WAVEFORMS @ 25°C

Switching times are measured after the device under test reaches a stabilized temperature (air flow ≥ 500 lfpm)



Advance Information

P_D = 370 mW typ/pkg (No Load)
f_{toggle} 150 MHz (typ)

The MC10178 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

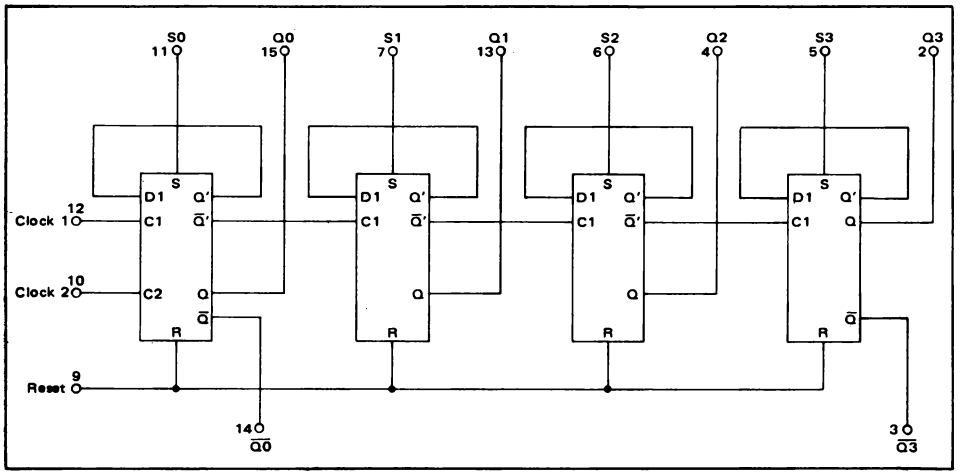
TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	ϕ	ϕ	L	L	L	L
L	H	H	H	H	ϕ	ϕ	H	H	H	H
L	L	L	L	L	H	ϕ	No Count			
L	L	L	L	L	ϕ	H	No Count			
L	L	L	L	L	••		L	L	L	L
L	L	L	L	L	••		H	L	L	L
L	L	L	L	L	••		L	H	L	L
L	L	L	L	L	••		H	H	L	L
L	L	L	L	L	••		L	L	H	L
L	L	L	L	L	••		H	L	H	L
L	L	L	L	L	••		L	H	H	L
L	L	L	L	L	••		H	H	H	L
L	L	L	L	L	••		L	L	L	H
L	L	L	L	L	••		H	L	L	H
L	L	L	L	L	••		L	H	L	H
L	L	L	L	L	••		H	H	L	H
L	L	L	L	L	••		L	L	H	H
L	L	L	L	L	••		H	L	H	H
L	L	L	L	L	••		L	H	H	H
L	L	L	L	L	••		H	H	H	H

ϕ = Don't Care

•• V_{IL} ⌐ V_{IH} Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

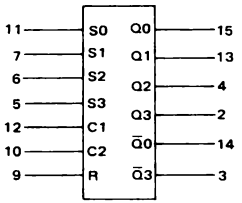


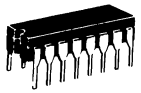
This is advance information on a new introduction and specifications are subject to change without notice.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.





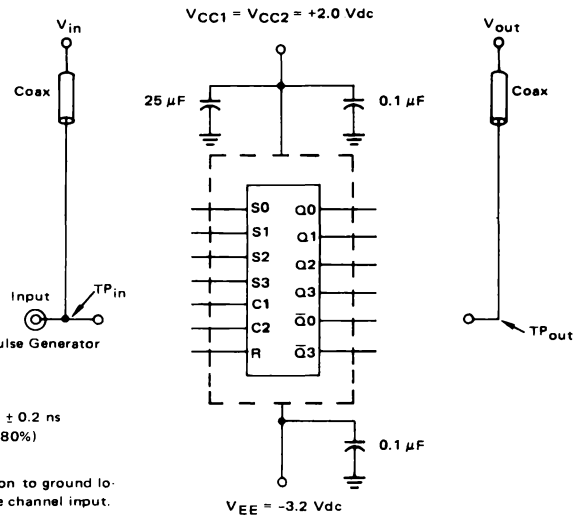
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10178L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	88.5	–	–	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	12	–	–	–	–	245	–	–	µAdc	12	–	–	–	8	1,16
		11	–	–	–	–	220	–	–	µAdc	11	–	–	–	8	1,16
		9	–	–	–	–	410	–	–	µAdc	9	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	11	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	11	–	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		14	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	11	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	9	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		14	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	11	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	9	8	1,16
Switching Times													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input** Propagation Delay	t_{12+15+}	15	–	–	–	3.5	–	–	–	ns	–	–	12	15	8	1,16
	t_{12-13-}	13	–	–	–	6.0	–	–	–		–	–		13		
	t_{12+4-}	4	–	–	–	8.5	–	–	–		–	–		4		
	t_{12-3+}	3	–	–	–	11	–	–	–		–	–		3		
Rise Time (20 to 80%)	t_{15+}	15	–	–	–	2.5	–	–	–		–	–		15		
Fall Time (20 to 80%)	t_{15-}	15	–	–	–	2.5	–	–	–		–	–		15		
Set Input	t_{11-15+}	15	–	–	–	5.2	–	–	–	ns	–	–	11	15	8	1,16
Reset Input	t_{9-15+}	15	–	–	–	5.2	–	–	–	ns	–	–	9	15	8	1,16
Counting Frequency	f_{count}	15	–	–	–	150	–	–	–	MHz	–	–	12	15	8	1,16

*Individually test each input applying V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



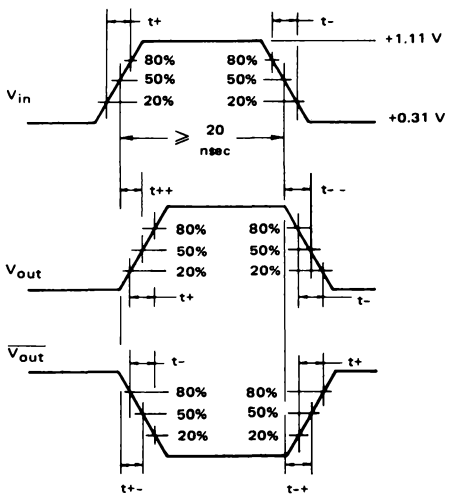
Input Pulse
$t+ = t- = 2.0 \pm 0.2$ ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are tied to a 50-ohm resistor to ground.

PROPAGATION DELAY



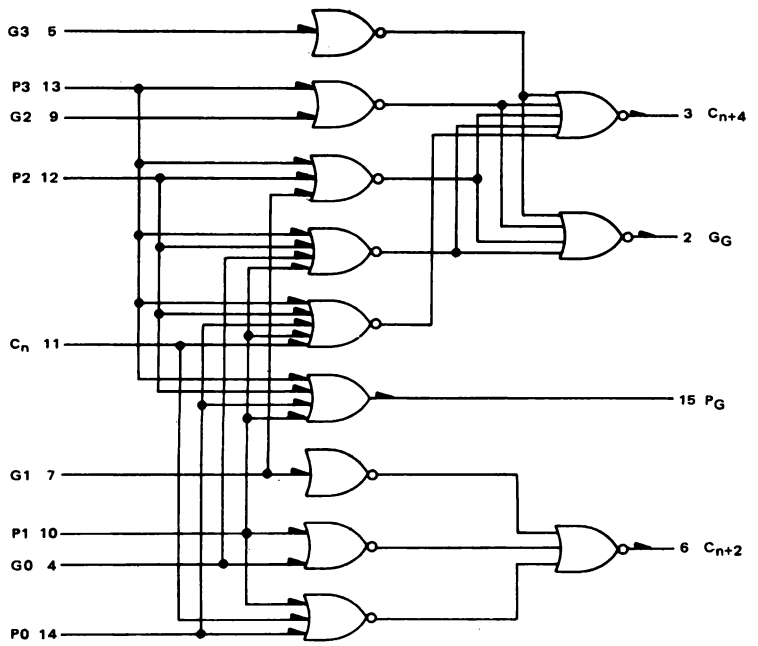
LOOK-AHEAD CARRY BLOCK

MC10179

P_D = 300 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ (Carry, Propagate)
4.0 ns typ (Generate)

The MC10179 device has 12 low power gates internally connected to perform the look-ahead carry function. This device has high Z input pulldown resistors and open emitter outputs. This device has applications in fast look-ahead adders such as with the MC10181. It can be used also as a boolean function generator.

POSITIVE LOGIC

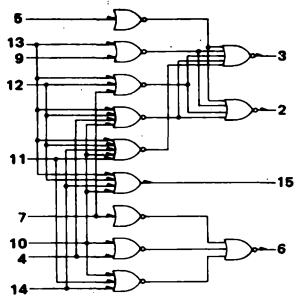


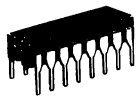
$P_G = P0 + P1 + P2 + P3$
$G_G = (G0 + P1 + P2 + P3)\ (G1 + P2 + P3)\ (G2 + P3)\ G3$
$C_{n+2} = (C_n + P0 + P1)\ (G0 + P1)\ G1$
$C_{n+4} = (C_n + P0 + P1 + P2 + P3)\ (G0 + P1 + P2 + P3)\ (G1 + P2 + P3)\ (G2 + P3)\ G3$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





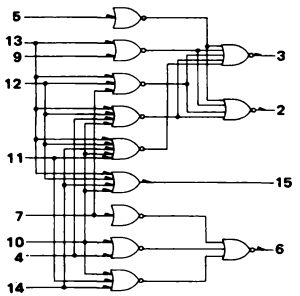
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10179L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	58	72	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4,7,11	–	–	–	–	270	–	–	µAdc	4,7,11	–	–	–	8	1,16
		5,9	–	–	–	–	225	–	–		5,9	–	–	–		
		10,13	–	–	–	–	440	–	–		10,13	–	–	–		
		12	–	–	–	–	395	–	–		12	–	–	–		
		14	–	–	–	–	355	–	–		14	–	–	–		
	I_{inL}	4	–	–	0.5	–	–	–	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,5,7,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13	–	5	–	8	1,16
		2		–		–	–		–		5,12	–	9	–		
		2		–		–	–		–		5,9	–	12	–		
		2		–		–	–		–		5	–	13	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13	–	–	5	8	1,16
		2	–		–	–		–			5	–	–	13		
		2	–		–	–		–			5	–	–	9		
		2	–		–	–		–			5,9	–	–	12		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+3+}	3	–	–	1.0	–	5.5	–	–	ns	4,7,9	–	5	3	8	1,16
	t_{5-3-}	3	–	–		–		–	–		4,7,9	–	5	3		
	t_{11+6+}	6	–	–		–		–	–		4,7	–	11	6		
	t_{11-6-}	6	–	–		–		–	–		4,7	–	11	6		
	t_{5+2+}	2	–	–		–		–	–		4,7,9	–	5	2		
	t_{5-2-}	2	–	–		–		–	–		4,7,9	–	5	2		
	t_{10+6+}	6	–	–		–		–	–		4,7	–	10	6		
	t_{10-6-}	6	–	–		–		–	–		4,7	–	10	6		
	t_{10+15+}	15	–	–		–	3.5	–	–		12,13,14	–	10	15		
	t_{10-15-}	15	–	–		–		–	–		12,13,14	–	10	15		
Rise Time (20% to 80%)	t_{6+}	6	–	–	1.1	–		–	–		4,7	–	11	6		
Fall Time (20% to 80%)	t_{6-}	6	–	–	1.1	–		–	–		4,7	–	11	6		

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

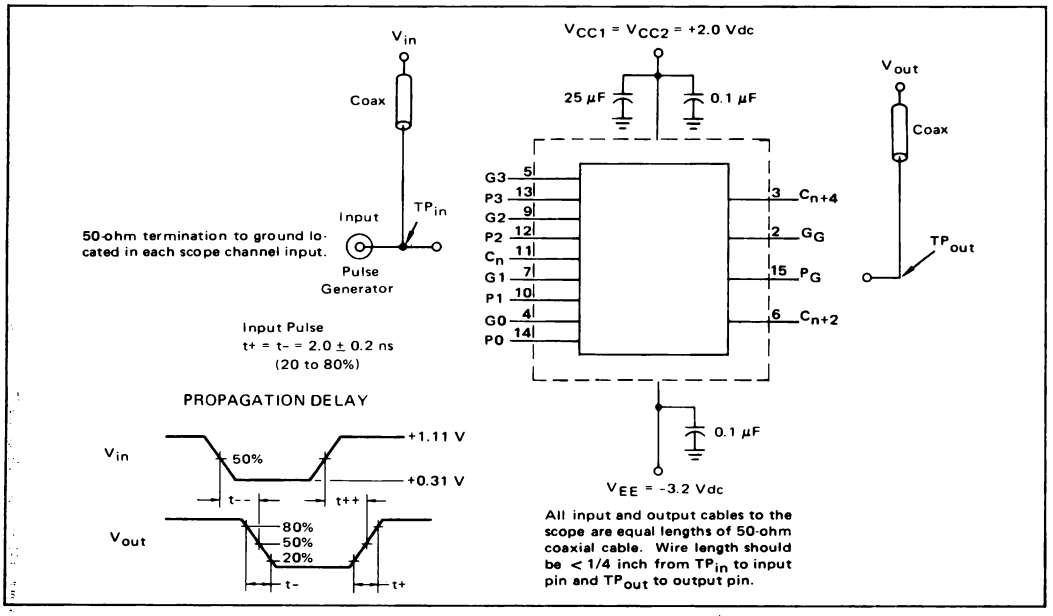


P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10179P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	58	72	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4,7,11	–	–	–	–	270	–	–	µAdc	4,7,11	–	–	–	8	1,16
		5,9	–	–	–	–	225	–	–		5,9	–	–	–		
		10,13	–	–	–	–	440	–	–		10,13	–	–	–		
		12	–	–	–	–	395	–	–		12	–	–	–		
		14	–	–	–	–	355	–	–		14	–	–	–		
	I_{inL}	4	–	–	0.5	–	–	–	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,5,7,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13	–	5	–	8	1,16
		2		–		–	–		–		5,12	–	9	–		
		2		–		–	–		–		5,9	–	12	–		
		2		–		–	–		–		5	–	13	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13	–	–	5	8	1,16
		2	–		–	–		–			5	–	–	13		
		2	–		–	–		–			5	–	–	9		
		2	–		–	–		–			5,9	–	–	12		
											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Switching Times (50 Ω Load) Propagation Delay	t_{5+3+}	3	–	–	1.0	–	5.5	–	–	ns	4,7,9	–	5	3	8	1,16
	t_{5-3-}	3	–	–		–		–	–		4,7,9	–	5	3		
	t_{11+6+}	6	–	–		–		–	–		4,7	–	11	6		
	t_{11-6-}	6	–	–		–		–	–		4,7	–	11	6		
	t_{5+2+}	2	–	–		–		–	–		4,7,9	–	5	2		
	t_{5-2-}	2	–	–		–		–	–		4,7,9	–	5	2		
	t_{10+6+}	6	–	–		–		–	–		4,7	–	10	6		
	t_{10-6-}	6	–	–		–		–	–		4,7	–	10	6		
	t_{10+15+}	15	–	–		–	3.5	–	–		12,13,14	–	10	15		
	t_{10-15-}	15	–	–		–		–	–		12,13,14	–	10	15		
Rise Time (20% to 80%)	t_{6+}	6	–	–	1.1	–		–	–		4,7	–	11	6		
Fall Time (20% to 80%)	t_{6-}	6	–	–	1.1	–		–	–		4,7	–	11	6		

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

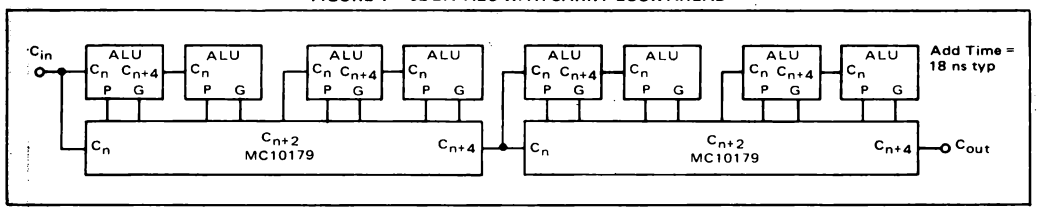


APPLICATION INFORMATION

The MC10179 is a high speed, low power, standard MECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10181 4-bit ALU directly, or with the MC10180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

When used with the MC10181, the MC10179 performs a second order or higher look-ahead. Figure 2 shows a 16-bit look-ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques, to 18 nanoseconds with carry look-ahead techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10179 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

FIGURE 1 – 32-BIT ALU WITH CARRY LOOK-AHEAD



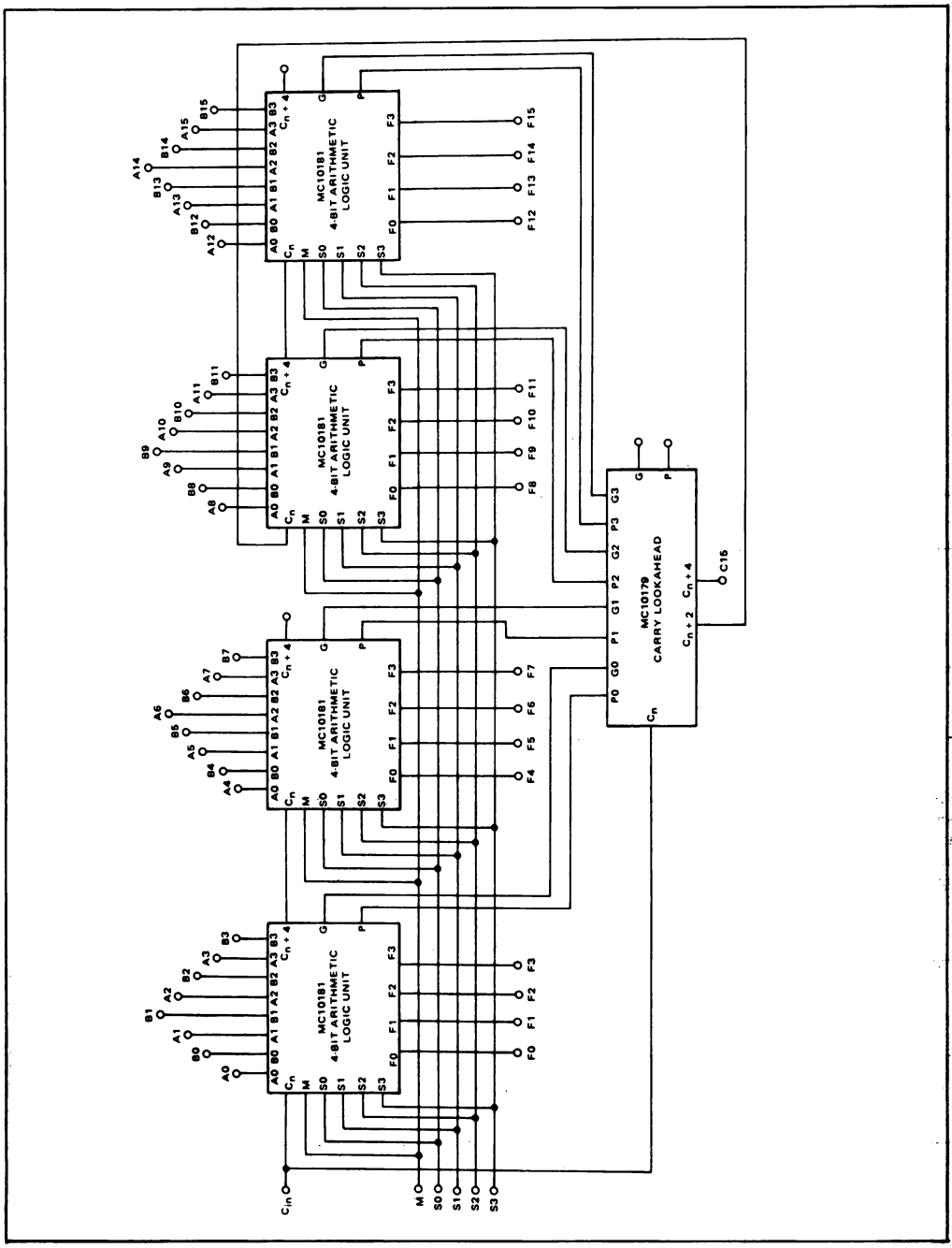


FIGURE 2 – 16-BIT FULL LOOK-AHEAD CARRY ARITHMETIC LOGIC UNIT

MC10180

P_D = 360 mW typ/pkg (No Load)

t_{pd} (typ)

C_{in} to C_{out} = 2.2 ns

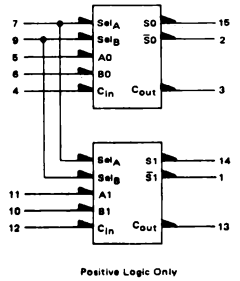
A0 to S0 = 4.5 ns

A0 to C_{out} = 4.5 ns

The MC10180 is a high speed, low power general-purpose adder/subtractor. It is designed to be used in special purpose adders/subtractors or in high speed multiplier arrays. The MC10180 can be used in any piece of equipment where these operations are necessary.

Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, $\overline{\text{Sum}}$, and Carry-out. The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B. The speed is very fast, with Carry-in to Carry-out propagation delay of 2.2 ns and Operand in to Sum or Carry-out propagation delay of 4.5 ns.

POSITIVE LOGIC



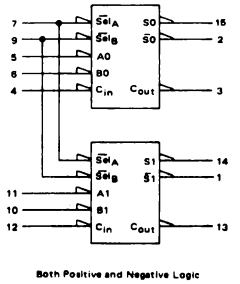
Positive Logic Only

$A' = A \odot \overline{Sel_A} = A \odot Sel_A$

$B' = B \odot \overline{Sel_B} = B \oplus Sel_B$

V_{CC} = Pin 16
V_{EE} = Pin 8

NEGATIVE LOGIC



Both Positive and Negative Logic

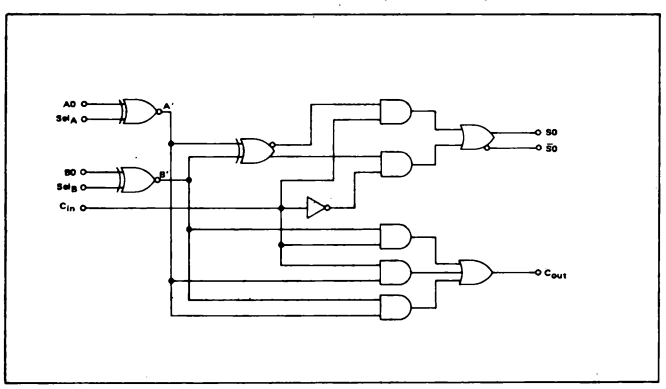
$S = \bar{C}_{in}(\bar{A}' B' + A' \bar{B}') + C_{in}(A' B' + \bar{A}' \bar{B}')$

$C_{out} = C_{in} A' + C_{in} B' + A' B'$

FUNCTION SELECT TABLE

Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

POSTIVE LOGIC DIAGRAM — 1/2 Of Circuit Shown



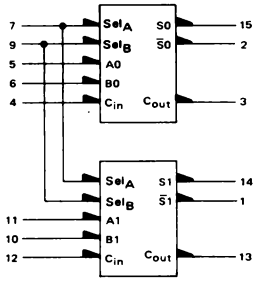
TRUTH TABLE

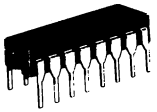
FUNCTION	INPUTS					OUTPUTS		
	Sel_A	Sel_B	A0	B0	C_{in}	S0	$\overline{S0}$	C_{out}
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	H
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	L
	H	H	H	H	H	H	L	H
	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	H
	H	L	H	L	L	L	H	L
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	L
	H	L	H	H	H	L	H	H
	L	H	L	L	L	L	H	L
	L	H	L	L	H	H	L	H
	L	H	L	H	L	H	L	L
	L	H	L	H	H	L	H	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	H
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
	L	L	L	L	L	H	L	L
	L	L	L	L	H	L	H	H
	L	L	L	H	L	L	H	L
	L	L	L	H	H	H	L	H
	L	L	H	L	L	L	H	L
	L	L	H	L	H	H	L	H
	L	L	H	H	L	H	L	L
	L	L	H	H	H	L	H	H
SUBTRACT	H	H	L	L	L	H	L	L
	H	H	L	L	H	L	H	H
	H	H	L	H	L	L	H	L
	H	H	L	H	H	H	L	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	L
	H	H	H	H	H	H	L	H
	H	L	L	L	L	L	H	L
	H	L	L	L	H	H	L	H
	H	L	L	H	L	H	L	L
	H	L	L	H	H	L	H	H
	H	L	H	L	L	H	L	L
	H	L	H	L	H	L	H	H
	H	L	H	H	L	L	H	L
	H	L	H	H	H	H	L	H
	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	H	L	L
	L	H	L	H	H	L	H	H
	L	H	H	L	L	H	L	L
	L	H	H	L	H	L	H	H
	L	H	H	H	L	L	H	L
	L	H	H	H	H	H	L	H
	L	L	L	L	L	H	L	L
	L	L	L	L	H	L	H	H
	L	L	L	H	L	L	H	L
	L	L	L	H	H	H	L	H
	L	L	H	L	L	L	H	L
	L	L	H	L	H	H	L	H
	L	L	H	H	L	H	L	L
	L	L	H	H	H	L	H	H
REVERSE SUBTRACT	L	H	L	L	L	L	H	L
	L	H	L	L	H	H	L	H
	L	H	L	H	L	H	L	L
	L	H	L	H	H	L	H	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	H
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
	H	H	L	L	L	H	L	L
	H	H	L	L	H	L	H	H
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	L	H	L
	H	H	H	L	H	H	L	H
	H	H	H	H	L	H	L	L
	H	H	H	H	H	L	H	H
	H	L	L	L	L	L	H	L
	H	L	L	L	H	H	L	H
	H	L	L	H	L	H	L	L
	H	L	L	H	H	L	H	H
	H	L	H	L	L	H	L	L
	H	L	H	L	H	L	H	H
	H	L	H	H	L	L	H	L
	H	L	H	H	H	H	L	H
	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	L	H	L
	L	H	L	H	H	H	L	H
	L	H	H	L	L	H	L	L
	L	H	H	L	H	L	H	H
	L	H	H	H	L	L	H	L
	L	H	H	H	H	H	L	H
	L	L	L	L	L	H	L	L
	L	L	L	L	H	L	H	H
	L	L	L	H	L	L	H	L
	L	L	L	H	H	H	L	H
	L	L	H	L	L	L	H	L
	L	L	H	L	H	H	L	H
	L	L	H	H	L	H	L	L
	L	L	H	H	H	L	H	H

See General Information section for packaging and maximum ratings information.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10180 L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	70	86	–	–	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	4	–	–	–	–	370	–	–	μAdc	4	–	–	–	8	16
		5	–	–	–	–	220	–	–		5	–	–	–		
		6	–	–	–	–	220	–	–		6	–	–	–		
		7	–	–	–	–	290	–	–		7	–	–	–		
		9	–	–	–	–	290	–	–		9	–	–	–		
		10	–	–	–	–	220	–	–		10	–	–	–		
		11	–	–	–	–	220	–	–		11	–	–	–		
		12	–	–	–	–	370	–	–		12	–	–	–		
	I_{inL}	All	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7,9	–	–	–	8	16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		4,5,7,9	–	–	–		
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		4,7,9	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,7,9	–	–	–	8	16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		7,9	–	–	–		
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		7,9	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	7,9	–	–	4	8	16
		3	-1.080	–	-0.980	–	–	-0.910	–		4,7,9	–	5	–		
		15	-1.080	–	-0.980	–	–	-0.910	–		7,9	–	4	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	7,9	–	4	–	8	16
		3	–	-1.655	–	–	-1.630	–	-1.595		7,9	–	–	4		
		15	–	-1.655	–	–	-1.630	–	-1.595		4,7,9	–	5	–		
Switching Times Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Operand Input	t_{5+15+}	15	1.3	5.8	1.3	–	5.4	1.1	5.8	ns	7,9	–	5	15	8	16
	t_{6+15+}	15	1.3	5.8	1.3	–	5.4	1.1	5.8		7,9	–	6	15		
Carry-in Input	t_{4+15+}	15	1.0	3.4	1.0	–	3.3	0.9	3.6		7,9	–	4	15		
	t_{4+3+}	3	1.0	3.4	1.0	–	3.3	0.9	3.6		5,7,9	–	4	3		
Select Input	t_{7+15+}	15	1.3	5.8	1.3	–	5.4	1.1	5.8		4,9	–	7	15		
	t_{9+15+}	15	1.3	5.8	1.3	–	5.4	1.1	5.8		7,4	–	9			
Rise Time (20 to 80%)	t_{15+}	15	1.0	3.8	1.1	–	3.7	1.1	3.9		7,9	–	5			
Fall Time	t_{15-}	15	1.0	3.8	1.1	–	3.7	1.1	3.9		7,9	–	5			

*Individually apply $V_{IL\ min}$ to pin under test.

ELECTRICAL CHARACTERISTICS

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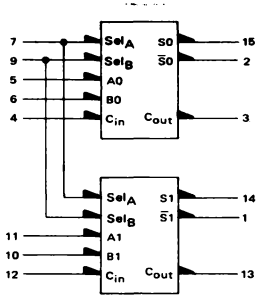

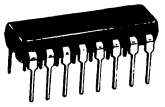

P SUFFIX
PLASTIC PACKAGE
CASE 648

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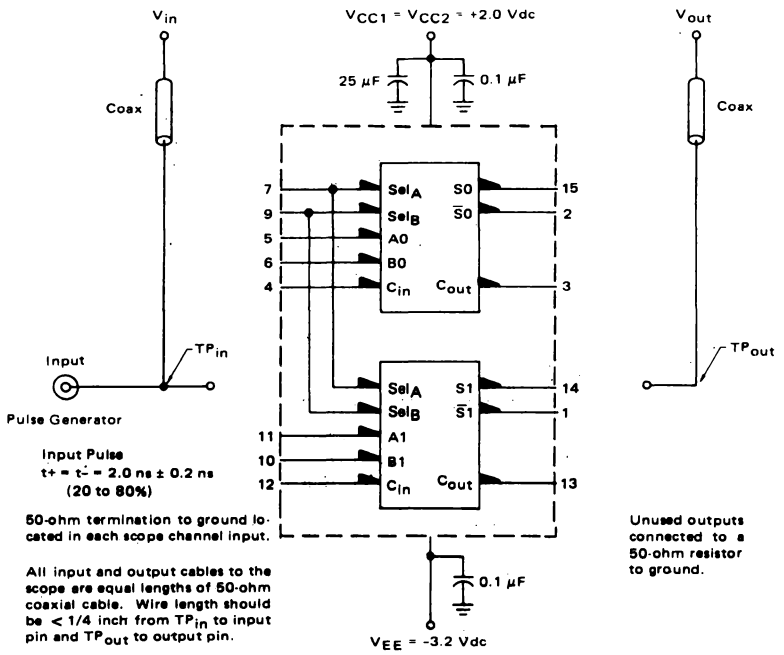
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

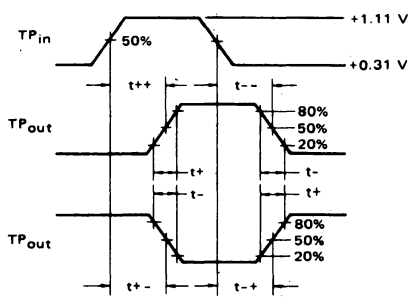
Characteristic	Symbol	Pin Under Test	MC10180P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	70	86	–	–	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	4	–	–	–	–	370	–	–	μAdc	4	–	–	–	8	16
		5	–	–	–	–	220	–	–		5	–	–	–		
		6	–	–	–	–	220	–	–		6	–	–	–		
		7	–	–	–	–	290	–	–		7	–	–	–		
		9	–	–	–	–	290	–	–		9	–	–	–		
		10	–	–	–	–	220	–	–		10	–	–	–		
		11	–	–	–	–	220	–	–		11	–	–	–		
		12	–	–	–	–	370	–	–		12	–	–	–		
	I_{inL}	All	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7,9	–	–	–	8	16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		4,5,7,9	–	–	–		
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		4,7,9	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,7,9	–	–	–	8	16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		7,9	–	–	–		
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		7,9	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	7,9	–	–	4	8	16
		3	-1.080	–	-0.980	–	–	-0.910	–		4,7,9	–	5	–		
		15	-1.080	–	-0.980	–	–	-0.910	–		7,9	–	4	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	7,9	–	4	–	8	16
		3	–	-1.655	–	–	-1.630	–	-1.595		7,9	–	–	4		
		15	–	-1.655	–	–	-1.630	–	-1.595		4,7,9	–	5	–		
Switching Times Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Operand Input	t_{5+15+}	15	–	–	1.3	–	5.4	–	–	ns	7,9	–	5	15	8	16
	t_{6+15+}	15	–	–	1.3	–	5.4	–	–		7,9	–	6	15		
Carry-in Input	t_{4+15+}	15	–	–	1.0	–	3.3	–	–		7,9	–	4	15		
	t_{4+3+}	3	–	–	1.0	–	3.3	–	–		5,7,9	–	4	3		
Select Input	t_{7+15+}	15	–	–	1.3	–	5.4	–	–		4,9	–	7	15		
	t_{9+15+}	15	–	–	1.3	–	5.4	–	–		7,4	–	9			
Rise Time (20 to 80%)	t_{15+}	15	–	–	1.1	–	3.7	–	–		7,9	–	5			
Fall Time	t_{15-}	15	–	–	1.1	–	3.7	–	–		7,9	–	5			

*Individually apply $V_{IL\ min}$ to pin under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



PROPAGATION DELAY



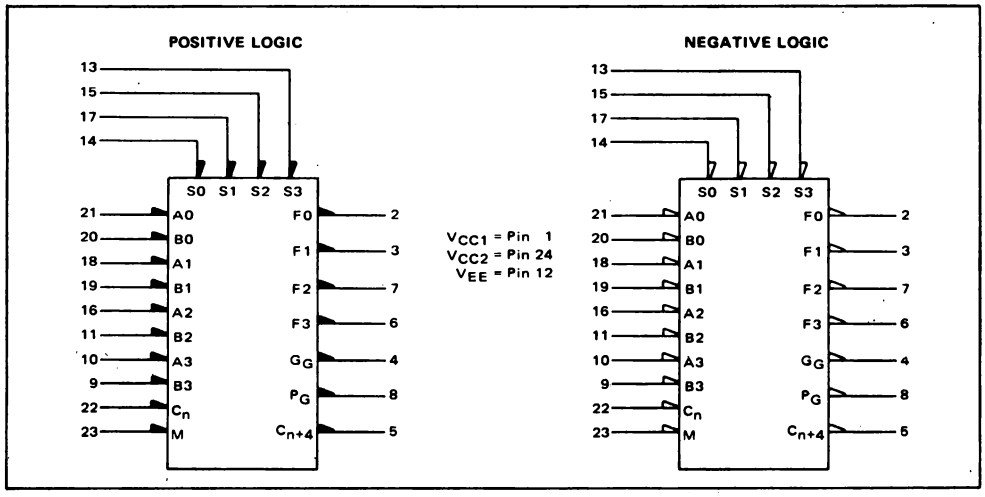
MC10181

The MC10181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions.

Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10179, full-carry look-ahead, as a second order look ahead block, the MC10181 provides high speed arithmetic operations on very long words.



P_D = 600 mW typ/pkg (No Load)
t_{pd} (typ): A1 to F = 6.5 ns
C_n to C_{n+4} = 3.1 ns
A1 to P_G = 5.0 ns
A1 to G_G = 4.5 ns
A1 to C_{n+4} = 5.0

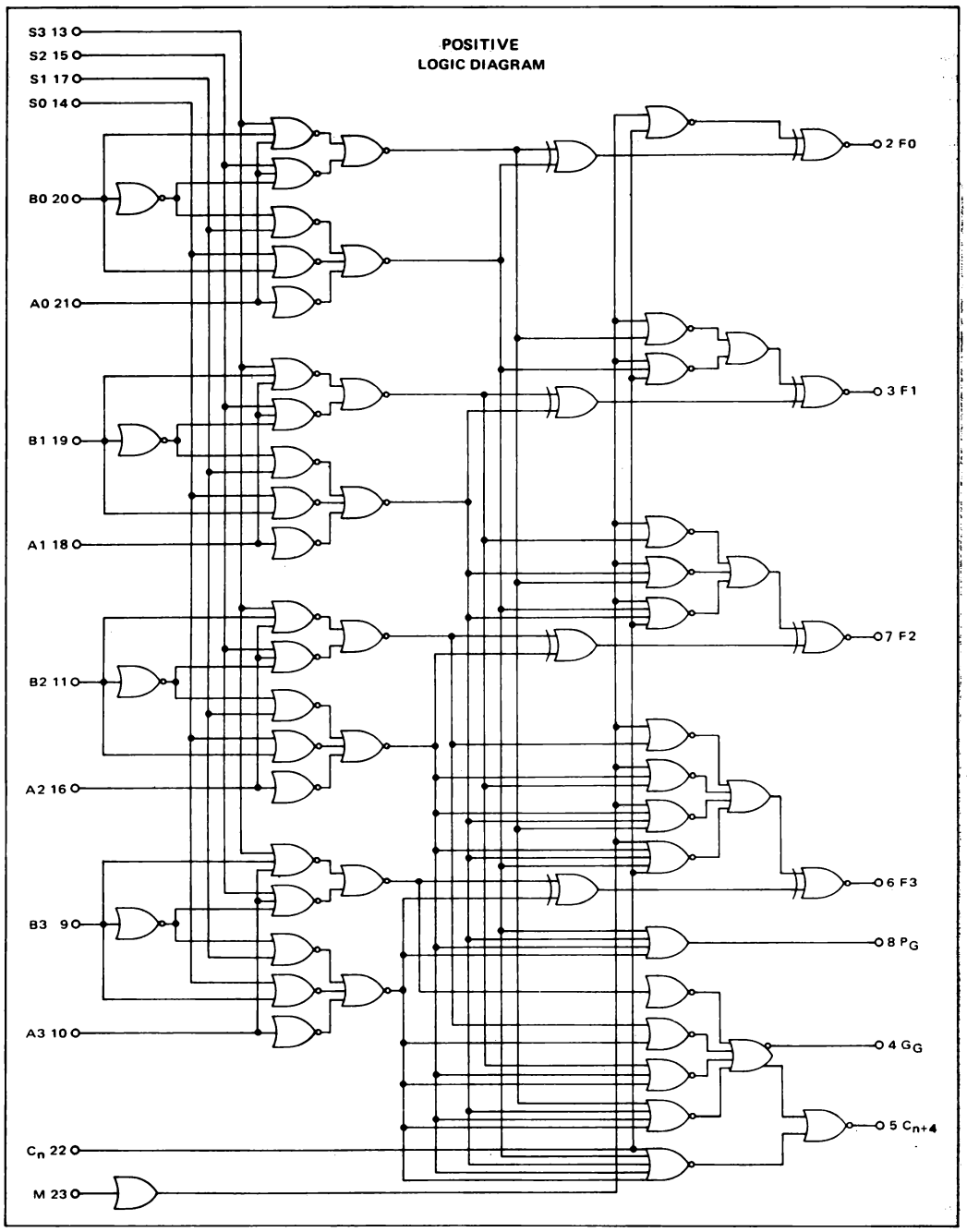
POSITIVE LOGIC

Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	$F = \overline{A}$	F = A plus 0
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus (A • $\overline{B}$)
L	L	H	L	$F = \overline{A} + B$	F = A plus (A • B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A} \bullet \overline{B}$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus (A • $\overline{B}$)
L	H	H	L	F = A ● B	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \bullet \overline{B}$	F = (A + $\overline{B}$) plus 0
H	L	L	H	F = A ⊙ B	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus (A • B)
H	L	H	H	F = A + B	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \bullet \overline{B}$	F = (A • $\overline{B}$) minus 1
H	H	H	L	F = A • B	F = (A • B) minus 1
H	H	H	H	F = A	F = A minus 1

NEGATIVE LOGIC

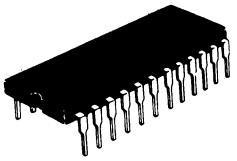
Function Select S3	S2	S1	S0	Logic Functions M is High F	Arithmetic Operation M is Low C_n of LSB must be High F
L	L	L	L	$F = \overline{A}$	F = A minus 1
L	L	L	H	$F = \overline{A + B}$	F = A plus (A + $\overline{B}$)
L	L	H	L	$F = \overline{A} \bullet B$	F = A plus (A + B)
L	L	H	H	F = Logical "0"	F = A times 2
L	H	L	L	$F = \overline{A \bullet B}$	F = (A • B) minus 1
L	H	L	H	$F = \overline{B}$	F = (A • B) plus (A + $\overline{B}$)
L	H	H	L	$F = A \oplus B$	F = A plus B
L	H	H	H	$F = A \bullet \overline{B}$	F = A plus (A • B)
H	L	L	L	$F = \overline{A} + B$	F = (A • $\overline{B}$) minus 1
H	L	L	H	$F = A \odot B$	F = A minus B minus 1
H	L	H	L	F = B	F = (A • $\overline{B}$) plus (A + B)
H	L	H	H	F = A • B	F = (A • $\overline{B}$) plus A
H	H	L	L	F = Logical "1"	F = minus 1 (two's complement)
H	H	L	H	F = A + $\overline{B}$	F = (A + $\overline{B}$) plus 0
H	H	H	L	F = A + B	F = (A + B) plus 0
H	H	H	H	F = A	F = A plus 0

See General Information section for packaging.

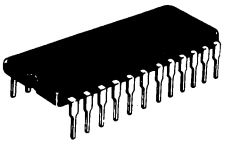

POSITIVE
LOGIC DIAGRAM
S3 13
S2 15
S1 17
S0 14
B0 20
A0 21
B1 19
A1 18
B2 11
A2 16
B3 9
A3 10
C_n 22
M 23
2 F0
3 F1
7 F2
6 F3
8 P_G
4 G_G
5 C_{n+4}

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10181 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	12	–	–	–	–	145	–	–	mAdc	–	–	–	–	12	1,24
Input Current	I_{inH}	9	–	–	–	–	245	–	–	µAdc	9	–	–	–	12	1,24
		10	–	–	–	–	220	–	–		10	–	–	–		
		11	–	–	–	–	245	–	–		11	–	–	–		
		13	–	–	–	–	200	–	–		13	–	–	–		
		14	–	–	–	–	265	–	–		14	–	–	–		
		15	–	–	–	–	265	–	–		15	–	–	–		
		16	–	–	–	–	220	–	–		16	–	–	–		
		17	–	–	–	–	265	–	–		17	–	–	–		
		18	–	–	–	–	220	–	–		18	–	–	–		
		19	–	–	–	–	245	–	–		19	–	–	–		
		20	–	–	–	–	245	–	–		20	–	–	–		
		21	–	–	–	–	220	–	–		21	–	–	–		
		22	–	–	–	–	290	–	–		22	–	–	–		
		23	–	–	–	–	200	–	–		23	–	–	–		
Input Leakage Current	I_{inL}	9	–	–	0.5	–	–	–	–	µAdc	–	9	–	–	12	1,24
		10	–	–		–	–	–	–		–	10	–	–		
		11	–	–		–	–	–	–		–	11	–	–		
		13	–	–		–	–	–	–		–	13	–	–		
		14	–	–		–	–	–	–		–	14	–	–		
		15	–	–		–	–	–	–		–	15	–	–		
		16	–	–		–	–	–	–		–	16	–	–		
		17	–	–		–	–	–	–		–	17	–	–		
		18	–	–		–	–	–	–		–	18	–	–		
		19	–	–		–	–	–	–		–	19	–	–		
		20	–	–		–	–	–	–		–	20	–	–		
		21	–	–		–	–	–	–		–	21	–	–		
		22	–	–		–	–	–	–		–	22	–	–		
		23	–	–		–	–	–	–		–	23	–	–		
High Output Voltage	V_{OH}	*	-1.060	-0.890	-0.980	–	-0.810	-0.890	-0.700	Vdc	*	*	–	–	12	1,24
Low Output Voltage	V_{OL}	*	-2.000	-1.675	-1.990	–	-1.650	-1.920	-1.615	Vdc	*	*	–	–	12	1,24
High Threshold Voltage	V_{OHA}	*	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	**	**	12	1,24
Low Threshold Voltage	V_{OLA}	*	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	**	**	12	1,24

*Test all input-output combinations according to Function Table.
**For threshold level test, apply threshold input level to only one input pin at a time

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics -30°C * Min	-30°C * Max	+25°C Min	+25°C Typ	+25°C Max	+85°C * Min	+85°C * Max	Unit
Propagation Delay	t++, t--	C_n	C_{n+4}	A0,A1,A2,A3	1.0	5.1	1.1	3.1	5.0	1.1	5.4	ns
Rise Time, Fall Time	t+,t-	C_n	C_{n+4}	A0,A1,A2,A3	1.0	3.2	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++, t+-	C_n	F1	A0	1.7	7.2	2.0	4.5	7.0	2.0	7.5	ns
	t-+, t--				1.7	7.2	2.0	4.5	7.0	2.0	7.5	
Rise Time, Fall Time	t+, t-				1.3	5.3	1.5	3.0	5.0	1.5	5.3	
Propagation Delay	t++, t+-	A1	F1	–	2.6	10.4	3.0	6.5	10	3.0	10.8	ns
	t-+, t- -				2.6	10.4	3.0	6.5	10	3.0	10.8	
Rise Time, Fall Time	t+, t-			–	1.3	5.4	1.5	3.0	5.0	1.5	5.3	
Propagation Delay	t++, t--	A1	P_G	S0,S3	1.6	7.0	2.0	5.0	6.5	2.0	7.0	ns
Rise Time, Fall Time	t+, t-	A1	P_G	S0,S3	0.8	3.7	1.1	2.0	3.5	1.1	3.8	ns
Propagation Delay	t++, t--	A1	G_G	A0,A2,A3,C_n	1.1	7.4	2.0	4.5	7.0	1.3	7.7	ns
Rise Time, Fall Time	t+, t-	A1	G_G	A0,A2,A3,C_n	1.2	5.1	1.5	4.0	5.0	1.2	5.3	ns
Propagation Delay	t+-, t-+	A1	C_{n+4}	A0,A2,A3,C_n	1.7	7.3	2.0	5.0	7.0	2.0	7.8	ns
Rise Time, Fall Time	t+, t-	A1	C_{n+4}	A0,A2,A3,C_n	1.0	3.1	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++, t-+	B1	F1	S3, C_n	2.7	11.3	3.0	8.0	11	3.0	11.9	ns
Rise Time, Fall Time	t+, t-	B1	F1	S3,C_n	1.2	5.3	1.5	3.5	5.0	1.5	5.3	ns

†Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
$V_{CC1} = V_{CC2} = +2.0$ Vdc, $V_{EE} = -3.2$ Vdc

*L Suffix Only

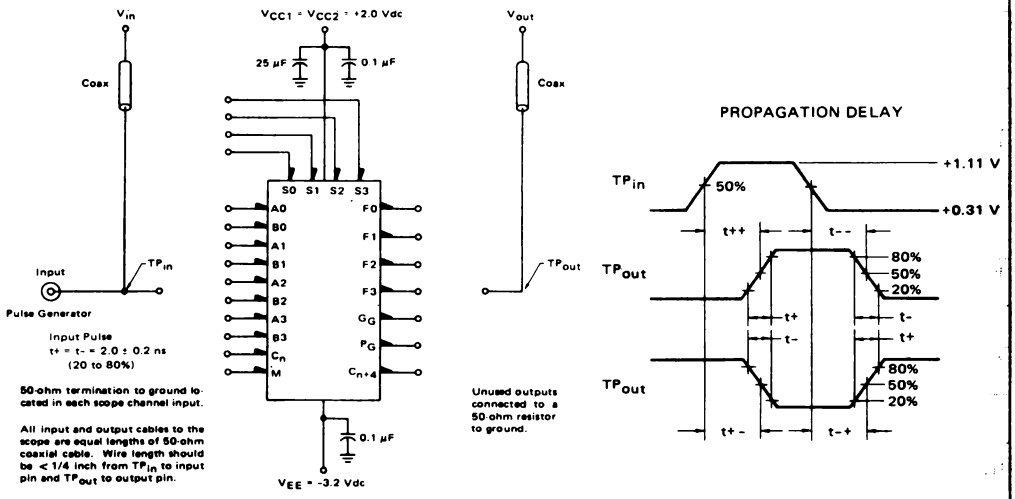
ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics							
					-30°C*		+25°C			+85°C*		
					Min	Max	Min	Typ	Max	Min	Max	Unit
Propagation Delay	t++, t--	B1	P_G	S0, S3	1.6	7.7	2.0	6.0	7.5	2.0	8.0	ns
Rise Time, Fall Time	t+, t-	B1	P_G	S0,S3	1.0	3.6	1.1	2.0	3.5	1.1	3.9	ns
Propagation Delay	t++, t--	B1	G_G	S3, C_n	1.7	8.2	2.0	6.0	8.0	2.0	8.6	ns
Rise Time, Fall Time	t+, t-	B1	G_G	S3,C_n	1.4	5.2	1.5	3.0	5.0	1.2	5.4	ns
Propagation Delay	t+-, t-+	B1	C_{n+4}	S3, C_n	1.8	8.2	2.0	6.0	8.0	2.0	8.7	ns
Rise Time, Fall Time	t+, t-	B1	C_{n+4}	S3,C_n	0.9	3.1	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++, t+-	M	F1	–	2.4	10.3	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+, t-	M	F1	–	1.1	5.1	1.5	4.0	5.0	1.5	5.3	ns
Propagation Delay	t+-, t-+	S1	F1	A1, B1	2.5	10.7	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+, t-	S1	F1	A1, B1	1.0	5.4	1.5	3.0	5.0	1.5	5.4	ns
Propagation Delay	t-+, t+-	S1	P_G	A3, B3	1.7	8.3	2.0	6.0	8.0	2.0	8.4	ns
Rise Time, Fall Time	t+, t-	S1	P_G	A3, B3	0.8	5.1	1.1	3.0	5.0	1.1	5.2	ns
Propagation Delay	t+-, t-+	S1	C_{n+4}	A3, B3	1.6	9.3	2.0	6.0	9.0	2.0	9.9	ns
Rise Time, Fall Time	t+, t-	S1	C_{n+4}	A3, B3	0.9	5.3	1.1	3.0	5.0	1.0	5.2	ns
Propagation Delay	t+-, t-+	S1	G_G	A3, B3	1.5	9.6	2.0	6.0	9.0	1.9	9.7	ns
Rise Time, Fall Time	t+, t-	S1	G_G	A3, B3	0.8	6.2	0.8	3.0	6.0	0.8	6.5	ns

†Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
$V_{CC1} = V_{CC2} = +2.0$ Vdc, $V_{EE} = -3.2$ Vdc

*L Suffix Only

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



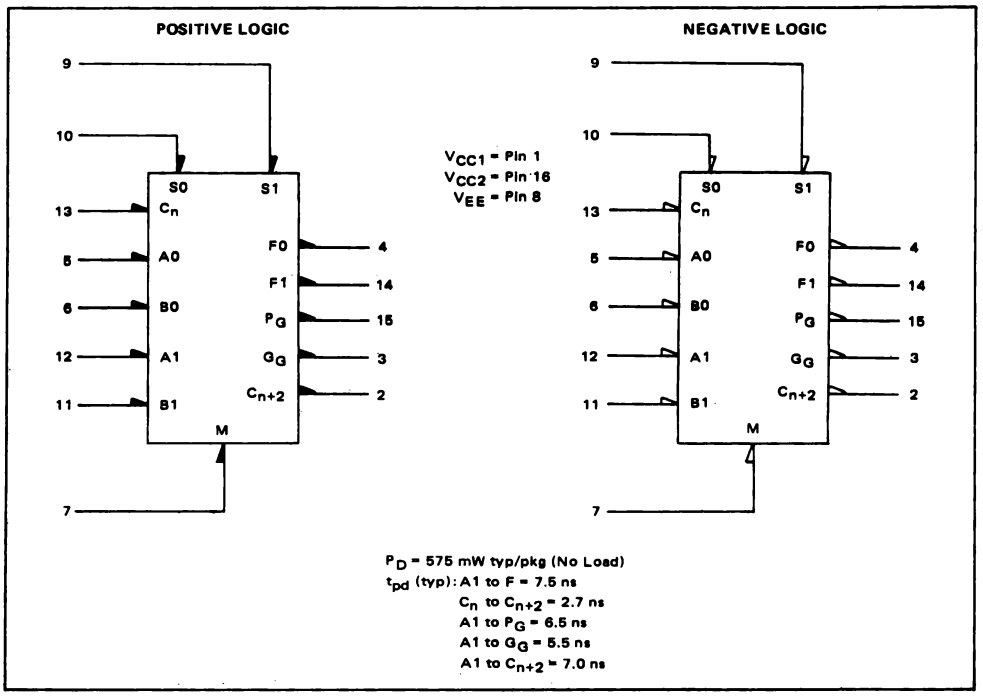
MC10182

Advance Information

The MC10182 is a high-speed arithmetic logic unit capable of performing 4 logic operations and 4 arithmetic operations on two 2-bit words. Full internal carry is incorporated for arithmetic operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 and S1) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided for a second order look ahead carry using the MC10179. The internal carry is enabled by applying a low level voltage to the mode control input (M).

The MC10182 provides an alternate to the MC10181 four-bit ALU for applications not requiring the extended functions of the MC10181 or for applications requiring a 16-pin package. The MC10182 also differs from the MC10181 in that Word A and Word B are treated equally for addition and subtraction (A plus B, A minus B, B minus A).

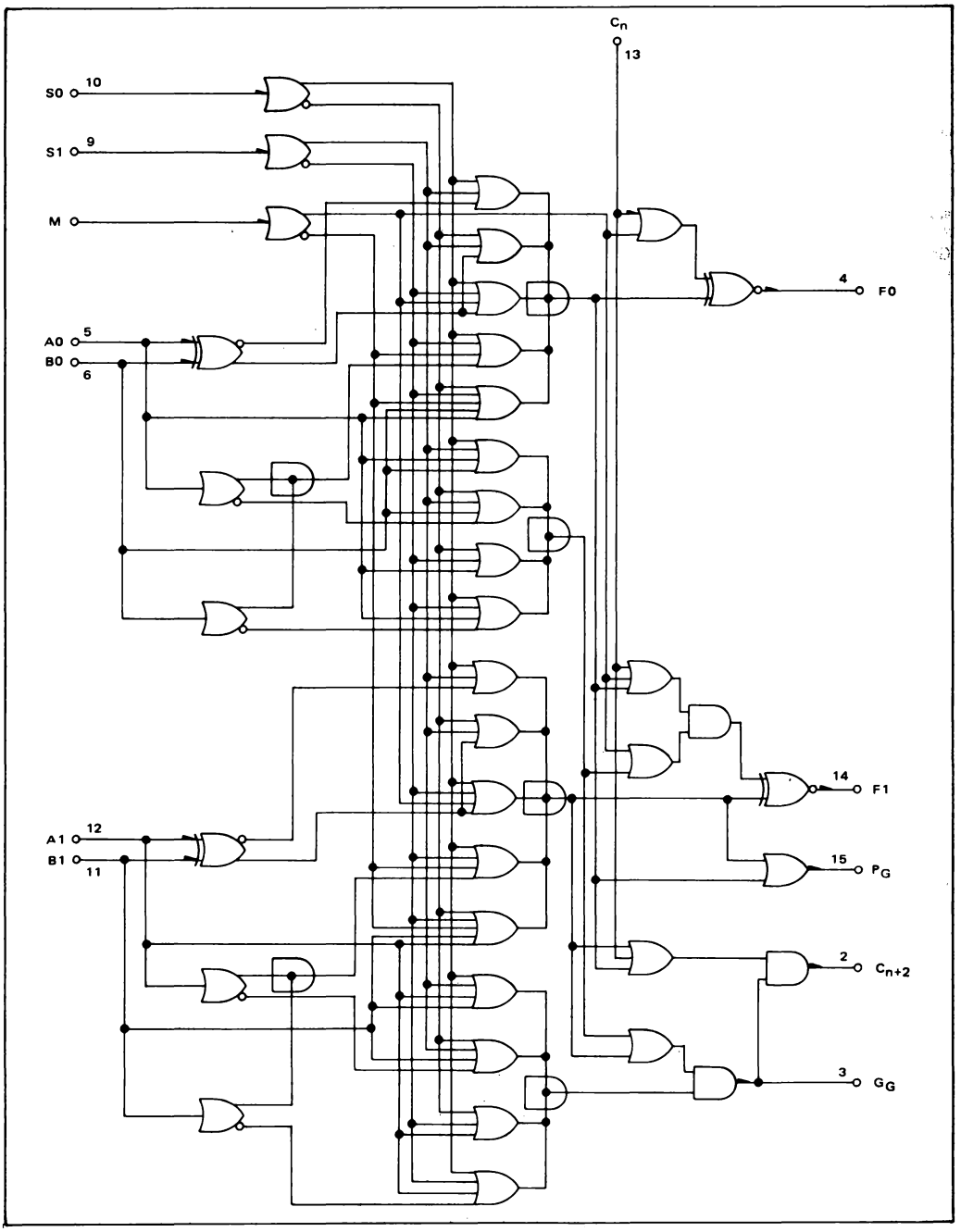


P_D = 575 mW typ/pkg (No Load)
t_{pd} (typ): A1 to F = 7.5 ns
C_n to C_{n+2} = 2.7 ns
A1 to P_G = 6.5 ns
A1 to G_G = 5.5 ns
A1 to C_{n+2} = 7.0 ns

Function Select		POSITIVE LOGIC		NEGATIVE LOGIC	
		Logic Function M is High	Arithmetic Operation M is Low	Logic Function M is High	Arithmetic Operation M is Low
S1	S0	F	F	F	F
L	L	F = A ⊙ B	F = A plus B plus Carry	F = A ⊕ B	F = A plus B plus Carry
L	H	F = A ⊕ B	F = $\overline{A}$ plus B plus Carry	F = A ⊙ B	F = $\overline{A}$ plus B plus Carry
H	L	F = A • B	F = A plus $\overline{B}$ plus Carry	F = A + B	F = A plus $\overline{B}$ plus Carry
H	H	F = A + B	F = A times 2	F = A • B	F = A times 2

See General Information section for packaging and maximum ratings information.
This is advance information and specifications are subject to change without notice.

POSITIVE LOGIC DIAGRAM



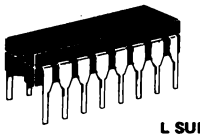
TRUTH TABLE

Input	M	L																															
	S1	L										H																					
	S0	L							H							L								H								
A1	B1	A0	B0	C_n	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}
L	L	L	L	L	L	L	H	L	L	H	H	L	H	H	H	H	L	H	H	L	L	L	H	L	L	L	L	H	L	L	L	L	L
L	L	L	L	H	L	H	H	L	L	L	L	L	H	H	L	H	H	L	L	H	H	H	L	L	L	L	L	H	H	L	L	L	L
L	L	L	H	L	L	H	H	L	L	L	L	H	H	H	H	L	H	L	L	L	L	H	L	L	H	H	H	H	L	L	L	L	L
L	L	L	H	H	H	L	H	L	L	L	H	H	H	H	H	H	H	L	L	L	H	H	L	L	H	H	H	H	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	H	L	H	H	H	H	L	H	L	L	H	L	H	L	L	H	H	H	H	L	L	L	L	L
L	L	H	L	H	H	L	H	L	L	H	H	H	L	L	L	H	H	H	H	H	L	H	L	L	H	H	H	H	L	L	L	L	L
L	L	H	H	L	H	L	H	L	L	H	H	L	H	L	H	H	L	H	L	H	L	H	L	L	H	H	H	H	L	L	L	L	L
L	L	H	H	H	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	H	H	L	L	H	H	H	H	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	H	H	H	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	L	L	L	L	L
L	H	L	L	H	H	L	H	L	L	H	L	H	L	L	L	H	H	L	L	L	L	H	L	L	H	H	H	H	L	L	L	L	L
L	H	L	H	L	H	H	H	L	L	H	L	H	H	H	H	L	H	L	L	H	L	H	L	L	H	H	H	H	L	L	L	L	L
L	H	L	H	H	L	L	L	H	H	H	H	H	H	H	L	H	H	L	L	L	L	H	L	L	H	H	H	H	L	L	L	L	L
L	H	H	L	L	H	H	L	H	H	H	L	H	H	H	H	L	H	L	L	L	L	H	L	L	H	H	H	H	L	L	L	L	L
L	H	H	L	H	L	L	L	H	H	L	H	H	H	H	L	H	H	L	L	L	L	H	L	L	H	H	H	H	L	L	L	L	L
L	H	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	L	L	L	L	H	L	L	H	H	H	H	L	L	L	L	L
L	H	H	H	H	L	H	H	H	L	L	H	L	H	H	H	L	H	L	L	L	L	H	L	L	H	H	H	H	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	H	H	L	L	L	L	H	H	H	L	H	H	L	L	L	L	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	L	H	L	H	H	H	L	H	H	H	H	L	H	H	L	L	L	L	H	H	H	L	H	H	H
H	L	L	H	L	H	H	L	H	L	H	L	L	H	H	L	L	H	H	H	L	H	H	L	L	L	L	L	L	H	H	H	H	H
H	L	L	H	H	L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H	L	L	L	L	L	L	H	H	H	H	H
H	L	H	L	L	H	H	L	H	L	H	L	H	L	L	H	L	H	H	H	L	H	H	L	L	L	L	H	H	H	H	H	H	H
H	L	H	L	H	L	H	L	H	L	L	L	H	L	L	L	L	H	H	H	L	H	H	L	L	L	L	L	L	H	H	H	H	H
H	L	H	H	L	L	H	L	H	L	L	L	H	H	H	L	H	H	H	H	L	H	H	L	L	L	L	H	H	H	H	H	H	H
H	L	H	H	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	L	H	H	L	L	L	L	L	L	H	H	H	H	H
H	H	L	L	L	L	L	H	H	H	H	H	L	H	L	H	H	L	H	H	H	H	H	H	L	L	L	H	L	H	L	H	H	H
H	H	L	L	H	H	H	H	L	L	L	L	L	H	H	L	H	H	L	L	H	H	H	L	L	L	L	L	L	H	L	H	H	H
H	H	L	H	L	H	L	H	H	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	L	L	L	H	H	H	H	L	L	H	H	H	H	H	H	L	L	L	L	L	L	H	H	H	H	H
H	H	H	L	L	L	H	H	H	H	H	L	H	L	L	L	L	H	H	H	H	H	H	L	L	L	L	H	L	H	H	H	H	H
H	H	H	L	H	H	H	H	L	L	L	H	H	L	L	H	L	H	H	H	H	H	H	L	L	L	L	L	L	H	H	H	H	H
H	H	H	H	L	H	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	H	H	H	H	H

These outputs are not normally used during logic operation.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

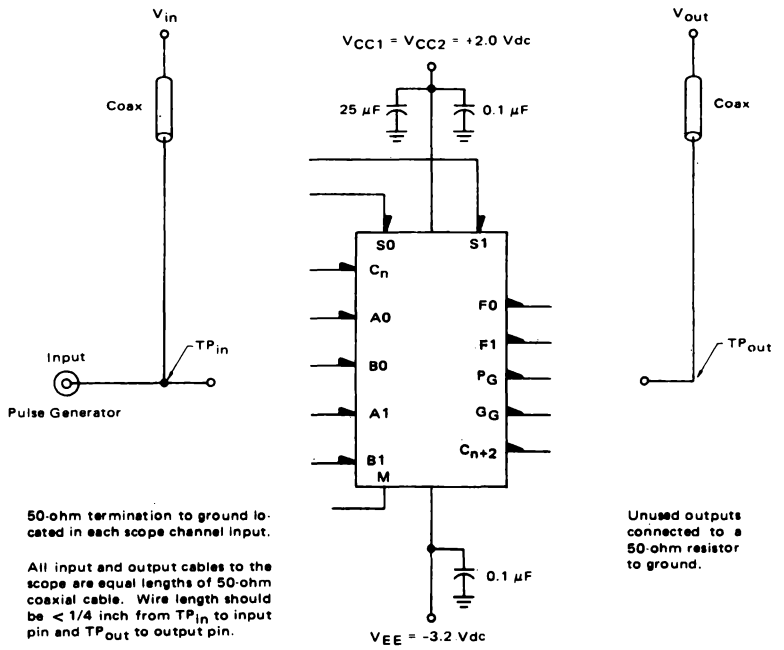


L SUFFIX
CERAMIC PACKAGE
CASE 620

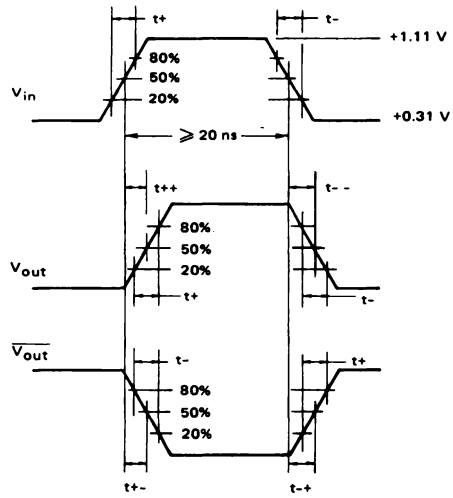
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10182L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	110	138	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	7	–	–	–	–	220	–	–	μAdc	7	–	–	–	8	1,16
		5	–	–	–	–	390	–	–		5	–	–	–		
		6	–	–	–	–	290	–	–		6	–	–	–		
		13	–	–	–	–	350	–	–		13	–	–	–		
	I_{inL}	5	–	–	0.5	–	–	–	–	μAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,6,11	–	–	–	8	1,16
		3				–					12,13	–	–	–		
		4				–						–	–	–		
		14				–						–	–	–		
		15				–						–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7,9,10	–	–	–	8	1,16
		3				–						–	–	–		
		4				–						–	–	–		
		14				–						–	–	–		
		15				–						–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6,7,9	–	5	–	8	1,15
		3		–		–	–		–		5,10,13	–	6	–		
		4		–		–	–		–		7,9,10	–	5	–		
		14		–		–	–		–		9,10	–	5	–		
		15		–		–	–		–		6,7,9	–	5	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6,7,9	–	–	5	8	1,16
		3	–		–	–		–			5,10,13	–	–	6		
		4	–		–	–		–			7,9,10	–	–	5		
		14	–		–	–		–			9,10	–	–	5		
		15	–		–	–		–			6,7,9	–	–	5		
Switching Times												+1.11 V	Pulse In	Pulse Out	-3.2V	+2.0 V
(50 Ω Load)		2	–	–	–	2.7	–	–	–	ns	–	10	13	2	8	1,16
Propagation Delay	t_{13+2+}	4	–	–	–	2.7	–	–	–		–	5	13	4		
	t_{13+4-}	4	–	–	–	7.0	–	–	–		–	7	5	4		
	t_{5+4-}	4	–	–	–	7.0	–	–	–		–	9,10	6	4		
	t_{6-4-}	14	–	–	–	7.0	–	–	–		–	–	12	14		
	t_{12-14+}	14	–	–	–	7.0	–	–	–		–	–	11	14		
	t_{11-14-}	2	–	–	–	7.0	–	–	–		–	9	5	2		
	t_{5+2+}	2	–	–	–	7.0	–	–	–		–	9,10	12	2		
	t_{12-2-}	2	–	–	–	7.0	–	–	–		–	10	6	2		
	t_{6-2-}	2	–	–	–	7.0	–	–	–		–	12	11	2		
	t_{11+2+}	15	–	–	–	6.5	–	–	–		–	10	5	15		
	t_{5-15-}	15	–	–	–	6.5	–	–	–		–	10	6	15		
	t_{6+15+}	3	–	–	–	5.5	–	–	–		–	10	5	3		
	t_{5+3-}	3	–	–	–	5.5	–	–	–		–	9	6	3		
	t_{6-3+}	4	–	–	–	4.0	–	–	–		–	9,10	7	4		
	t_{7-4+}	4	–	–	–	6.0	–	–	–		–	6,11,13	10	4		
	t_{10-4-}															
Rise Time (20% to 80%)	t_{4+}	4	–	–	–	2.5	–	–	–	ns	–	–	5	4	8	1,16
Fall Time (20% to 80%)	t_{4-}	4	–	–	–	2.5	–	–	–	ns	–	–	5	4	8	1,16

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



PROPAGATION DELAY



MC10195

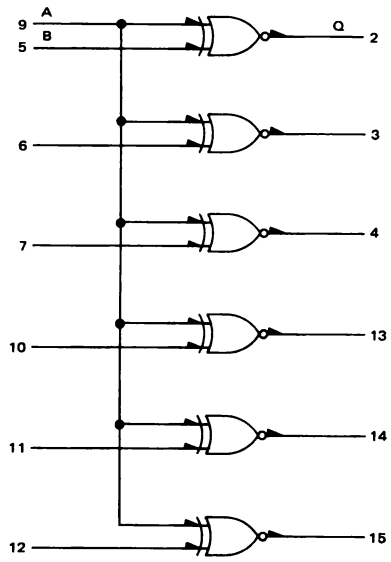
Advance Information

The MC10195 is a Hex Buffer Inverter which is built using six EXCLUSIVE NOR gates. There is a common input to these gates which when placed low or left open allows them to act as inverters. With the common input connected to a high logic level the MC10195 is a hex buffer, useful for high fanout clock driving and reducing stub lengths on long bus lines.

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

POSITIVE LOGIC



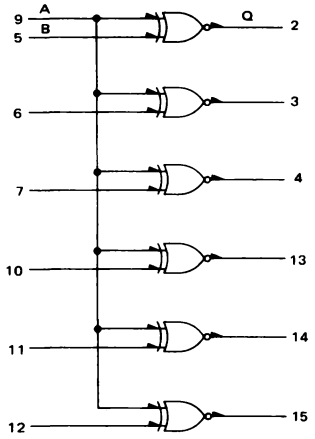
P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ

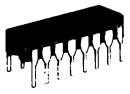
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.



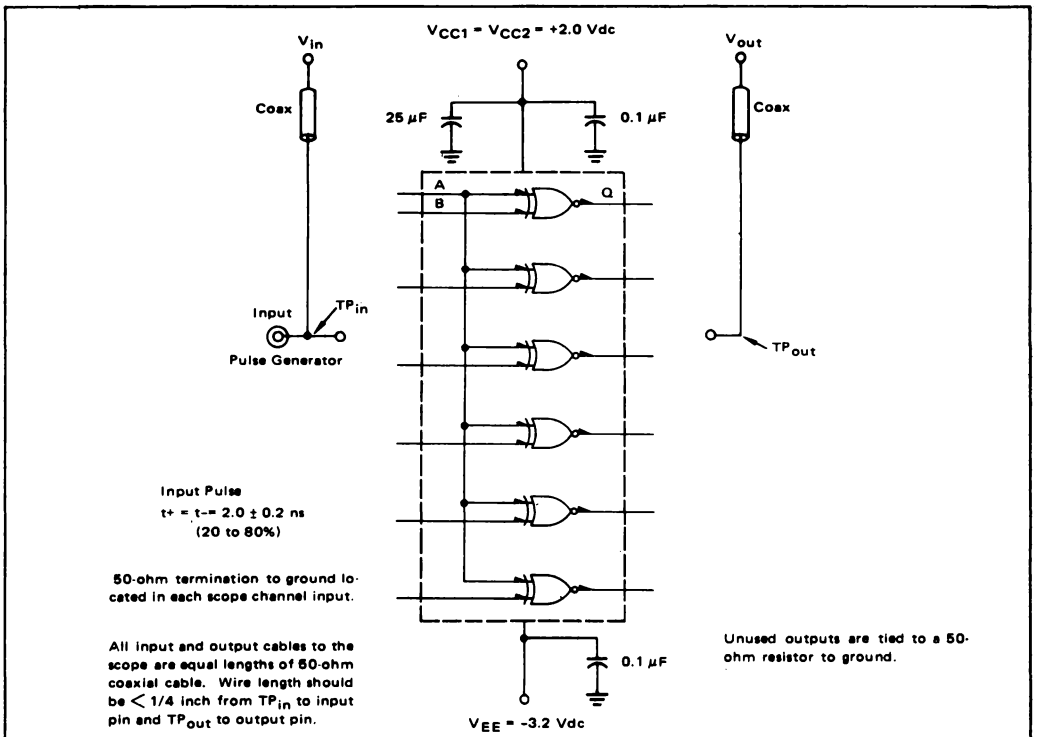


L SUFFIX
CERAMIC PACKAGE
CASE 620

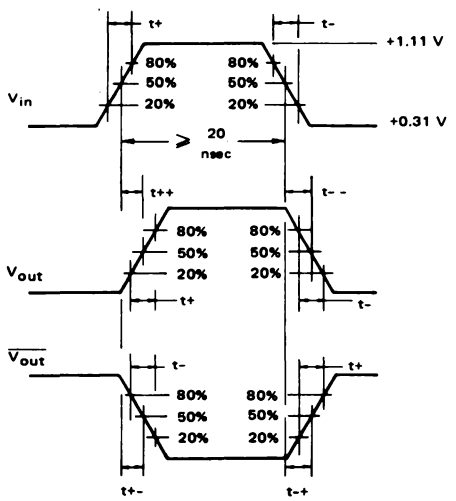
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10195L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	39	49	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	5	–	–	–	–	265	–	–	µAdc	5	–	–	–	8	1,16
		9	–	–	–	–	290	–	–	µAdc	9	–	–	–	8	1,16
	I_{inL}	5	–	–	0.5	–	–	–	–	µAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,16
Switching Time (50 ohm load)													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{5+2-}	2	–	–	–	2.8	–	–	–	ns	–	–	5	2	8	1,16
	t_{7-4+}	4	–	–	–	↓	–	–	–	↓	–	–	7	4	↓	↓
	t_{10+13+}	13	–	–	–		–	–	–		–	–	10	13		
	t_{11-14-}	14	–	–	–		–	–	–		–	–	11	14		
Rise Time (20% to 80%)	t_{2+}	2	–	–	–	2.0	–	–	–		–	–	5	2		
Fall Time (20% to 80%)	t_{2-}	2	–	–	–	2.0	–	–	–	↓	–	–	5	2	↓	↓

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



PROPAGATION DELAY



MC10197

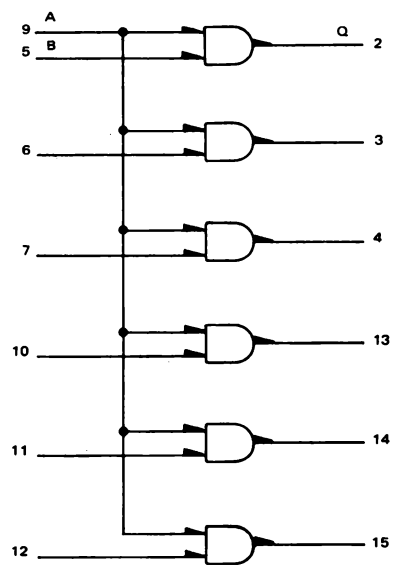
Advance Information

The MC10197 provides a high speed hex AND function with strobe capability. Open emitter outputs allow wire ORing. This high density function is useful in control, bussing, communications in high speed central processors, high speed peripherals, digital communications systems, minicomputers, and instrumentation.

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

POSITIVE LOGIC



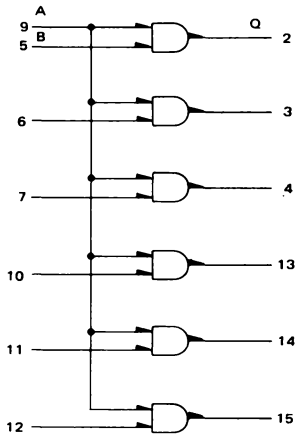
P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ

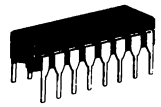
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.



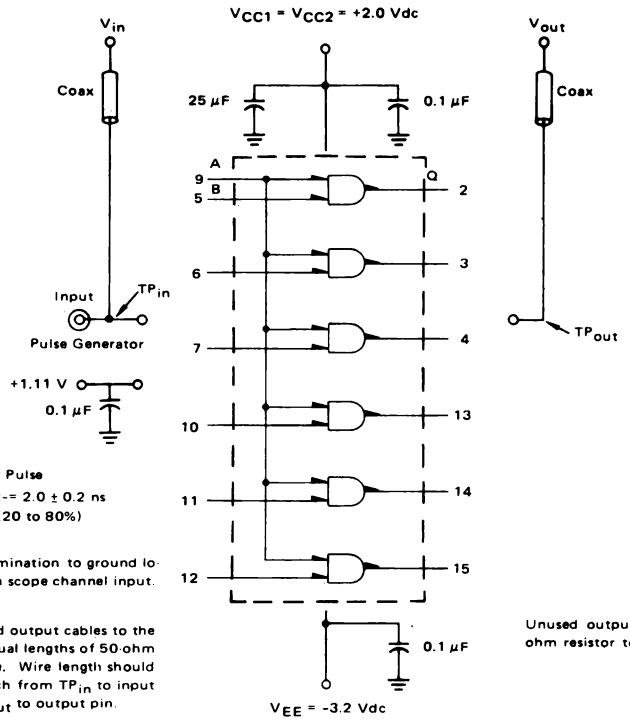


L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10197L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	39	49	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	5	–	–	–	–	265	–	–	µAdc	5	–	–	–	8	1,16
		9	–	–	–	–	290	–	–	µAdc	9	–	–	–	8	1,16
	I_{inL}	5	–	–	0.5	–	–	–	–	µAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	–	5	8	1,16
Switching Time (50 ohm load)												+1.11Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{5+2+}	2	–	–	–	2.8	–	–	–	ns	–	9	5	2	8	1,16
	t_{9+2+}	2	–	–	–	3.5	–	–	–	↓	–	5	9	↓	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	–	–	–	2.0	–	–	–		–	9	5			
Fall Time (20% to 80%)	t_{2-}	2	–	–	–	2.0	–	–	–		–	9	5			

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



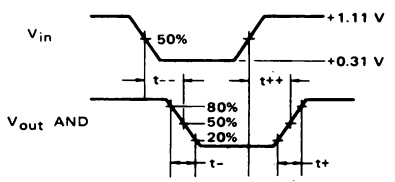
Input Pulse
t+ = t-= 2.0 ± 0.2 ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

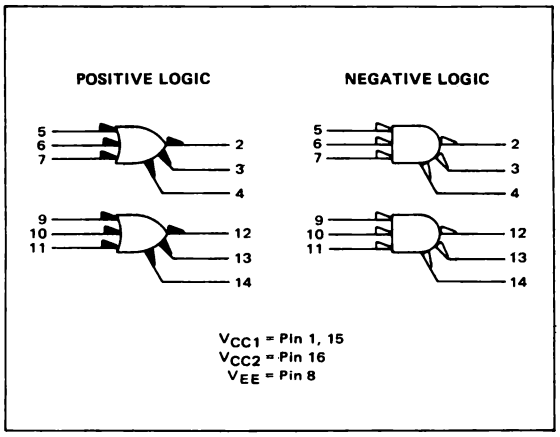
Unused outputs are tied to a 50-ohm resistor to ground.

PROPAGATION DELAY



HIGH SPEED DUAL 3-INPUT
3-OUTPUT "OR" GATE

MC10210



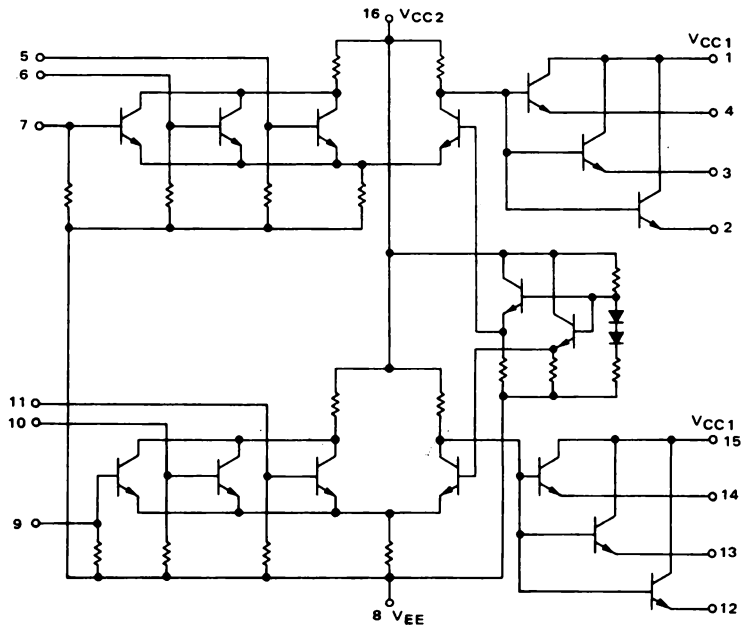
The MC10210 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10210 particularly useful in clock distribution applications where minimum clock skew is desired.

The MC10210 is a higher speed version of the MC10110. It is a pin-for-pin replacement for the device. Three V_{CC} pins are provided and each one should be used.

P_D = 160 mW typ/pkg (No Load)
t_{pd} = 1.5 ns typ (All Output Loaded)
Output Rise and Fall Time: (All Outputs Loaded)
= 1.5 ns typ (20% to 80%)

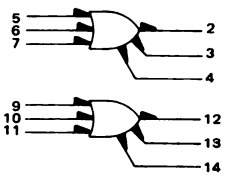
CIRCUIT SCHEMATIC



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.



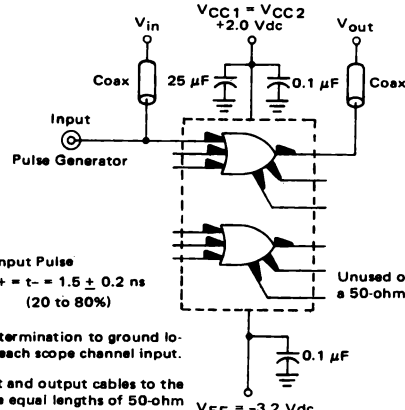
L SUFFIX
CERAMIC PACKAGE
CASE 620

● Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10210L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$ *	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	38	–	–	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	–	–	–	410	–	–	μAdc	•	–	–	–	8	1,15,16
	I_{inL}	5,6,7	–	–	0.5	–	–	–	–	μAdc	–	•	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	–	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	7	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2+}	2	–	–	1.0	1.5	2.5	–	–	ns	–	–	5	2	8	1,15,16
	t_{6-2-}	2	–	–				–	–		–	–		2		
	t_{5+3+}	3	–	–				–	–		–	–		3		
	t_{5-3-}	3	–	–				–	–		–	–		3		
	t_{5+4+}	4	–	–				–	–		–	–		4		
	t_{5-4-}	4	–	–				–	–		–	–		4		
Rise Time (20 to 80%)	t_{2+}	2	–	–				–	–		–	–		2		
	t_{3+}	3	–	–				–	–		–	–		3		
	t_{4+}	4	–	–				–	–		–	–		4		
Fall Time (20 to 80%)	t_{2-}	2	–	–				–	–		–	–		2		
	t_{3-}	3	–	–				–	–		–	–		3		
	t_{4-}	4	–	–				–	–		–	–		4		

*Individually test each input using the pin connections shown.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

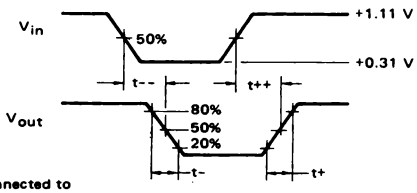


Input Pulse
t+ = t- = 1.5 ± 0.2 ns
(20 to 80%)

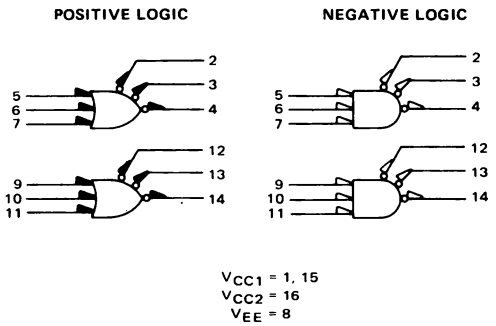
Unused outputs connected to a 50-ohm resistor to ground.

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.



MC10211

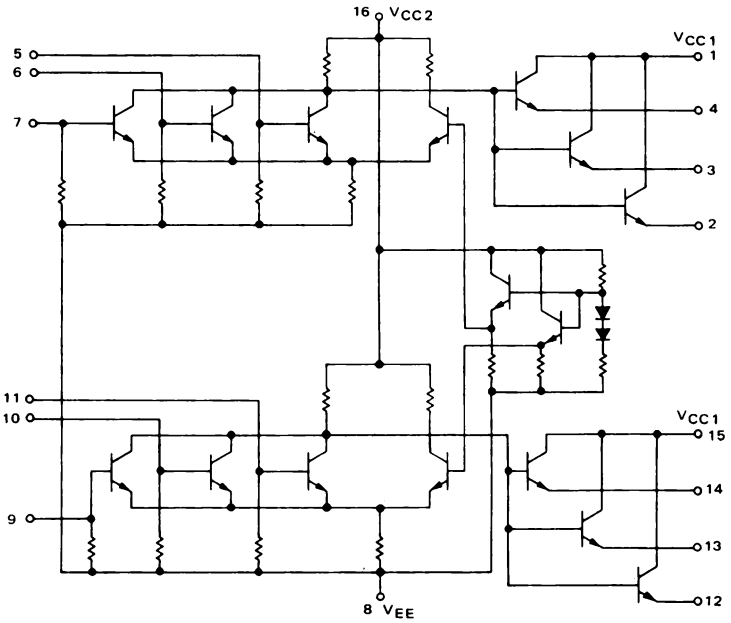


The MC10211 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10211 particularly useful in clock distribution applications where minimum clock skew is desired.

P_D = 75 mW typ/gate (Outputs Open)
t_{pd} = 1.5 ns typ (All Outputs Loaded)
Output Rise and Fall Time: (All Outputs Loaded)
= 1.5 ns typ (20% to 80%)

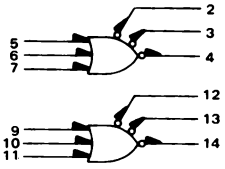
CIRCUIT SCHEMATIC

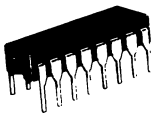


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.





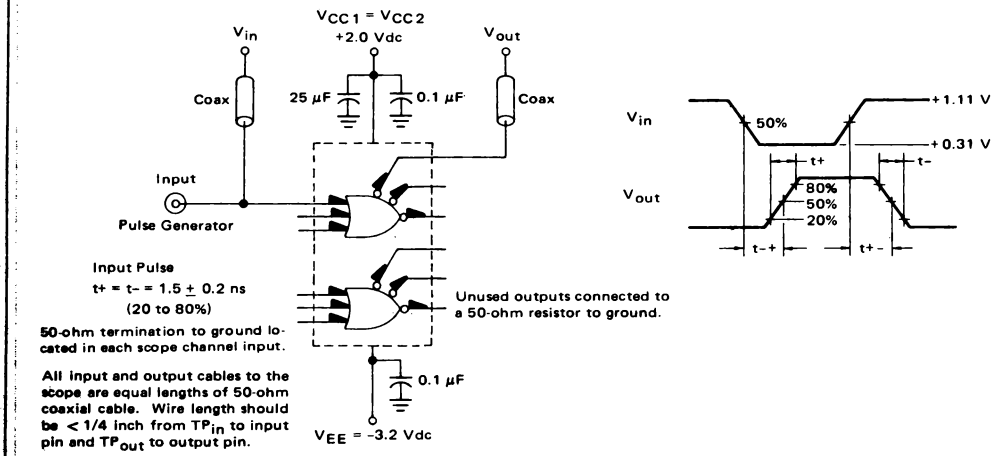
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10211L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	30	38	–	–	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	–	–	–	410	–	–	μAdc	*	*	–	–	8	1,15,16
	I_{inL}	5,6,7	*	–	0.5	–	–	–	*	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	6	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	7	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	6	–	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	–	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2-}	2	–	–	1.0	1.5	2.5	–	–	ns	–	–	5	2	8	1,15,16
	t_{5-2+}	2	–	–	↓	↓	↓	–	–	↓	–	–	↓	2	↓	↓
	t_{5+3-}	3	–	–				–	–		–	–		3		
	t_{5-3+}	3	–	–				–	–		–	–		3		
	t_{5+4-}	4	–	–				–	–		–	–		4		
	t_{5-4+}	4	–	–				–	–		–	–		4		
Rise Time (20 to 80%)	t_{2+}	2	–	–				–	–		–	–		2		
	t_{3+}	3	–	–				–	–			–		3		
	t_{4+}	4	–	–				–	–			–		4		
Fall Time (20 to 80%)	t_{2-}	2	–	–				–	–			–		2		
	t_{3-}	3	–	–				–	–		–	–		3		
	t_{4-}	4	–	–	↓	↓	↓	–	–	↓	–	–	↓	4	↓	↓

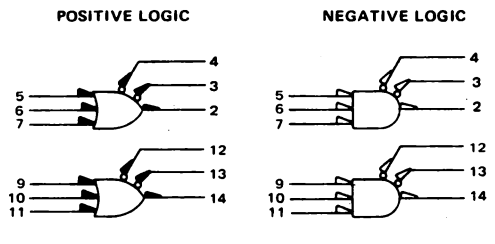
*Individually test each input using the pin connections shown.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



MC10212

Advance Information



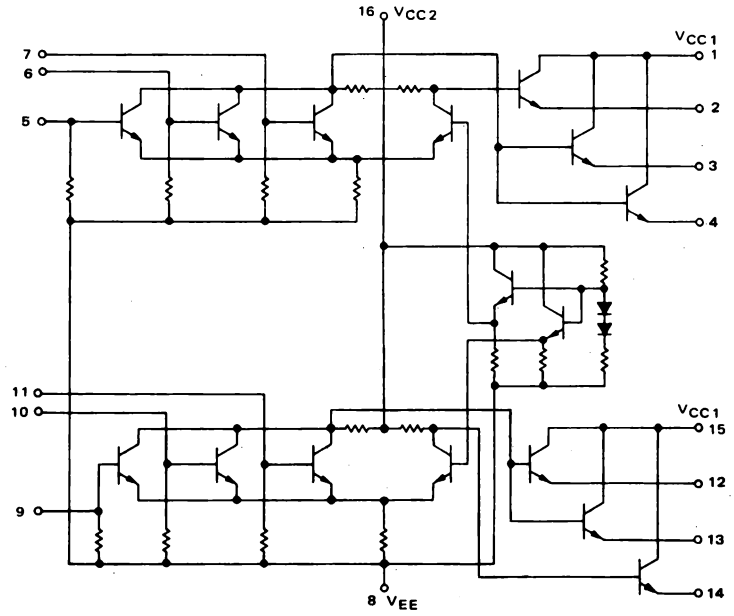
V_{CC1} = 1, 15
V_{CC2} = 16
V_{EE} = 8

The MC10212 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10212 particularly useful in clock distribution applications where minimum clock skew is desired.

P_D = 160 mW typ/pkg (No Load)
t_{pd} = 1.5 ns typ (All Outputs Loaded)
Output Rise and Fall Time: (All Outputs Loaded)
= 1.5 ns typ (20% to 80%)

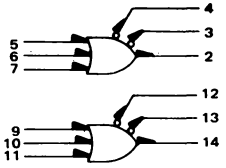
CIRCUIT SCHEMATIC

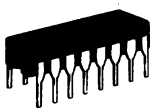


This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.





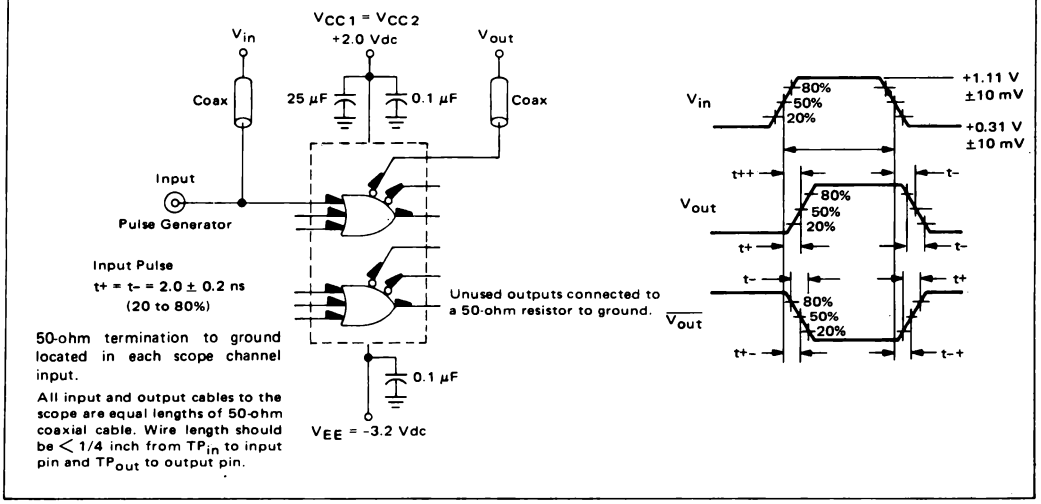
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10212L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	30	38	–	–	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	–	–	–	405	–	–	μAdc	5,6,7*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	–	–	0.5	–	–	–	–	μAdc	–	5,6,7*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2+}	2	–	–	–	1.5	–	–	–	ns	–	–	5	2	8	1,15,16
	t_{5-2-}	2	–	–	–		–	–	–		–	–		2		
	t_{5+3-}	3	–	–	–		–	–	–		–	–		3		
	t_{5-3+}	3	–	–	–		–	–	–		–	–		3		
	t_{5+4-}	4	–	–	–		–	–	–		–	–		4		
	t_{5-4+}	4	–	–	–		–	–	–		–	–		4		
Rise Time (20 to 80%)	t_{2+}	2	–	–	–		–	–	–		–	–		2		
	t_{3+}	3	–	–	–		–	–	–		–	–		3		
	t_{4+}	4	–	–	–		–	–	–		–	–		4		
Fall Time (20 to 80%)	t_{2-}	2	–	–	–		–	–	–		–	–		2		
	t_{3-}	3	–	–	–		–	–	–		–	–		3		
	t_{4-}	4	–	–	–		–	–	–		–	–		4		

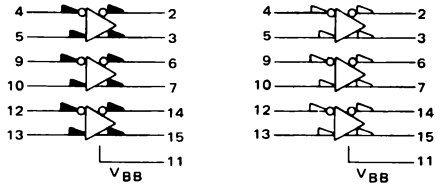
*Individually test each input using the pin connections shown.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



HIGH SPEED TRIPLE
LINE RECEIVER

MC10216



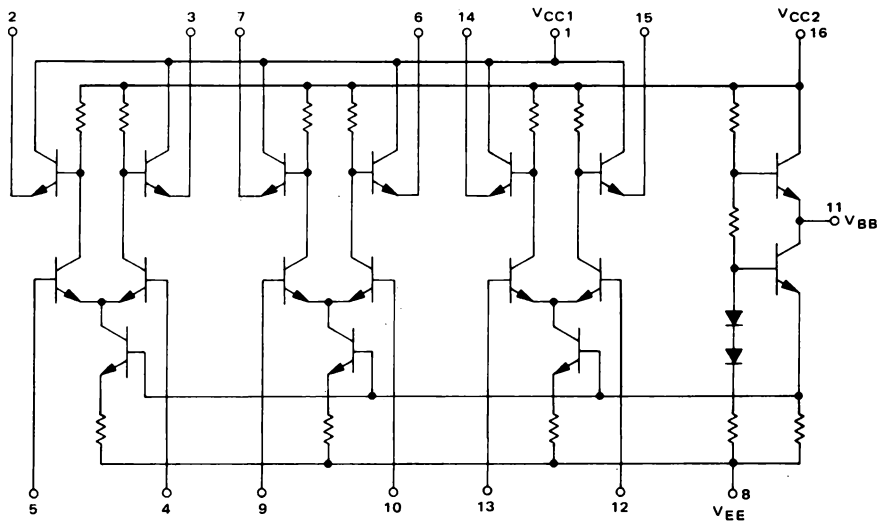
The MC10216 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 1.8 ns typ (Single ended)
= 1.5 ns typ (Differential)

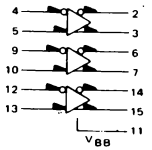
CIRCUIT SCHEMATIC

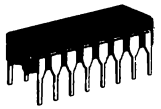


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

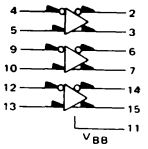
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2

Characteristic	Symbol	Pin Under Test	MC10216L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	25	–	–	mAdc	4,9,12	–	–	–	5,10,13	8	1,16
Input Current	I_{inH}	4	–	–	–	–	115	–	–	μAdc	4	9,12	–	–	5,10,13	8	1,16
	I_{CBO}	4	–	–	–	–	1.0	–	–	μAdc	–	9,12	–	–	5,10,13	8,4	1,16
		9	–	–	–	–	1.0	–	–	μAdc	–	4,12	–	–	5,10,13	8,9	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–	–	5,10,13	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4	–	–	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	–	4	5,10,13	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	4	–	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	8	1,16
Switching Times (50-ohm Load)													Pulse In	Pulse Out		-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{4+2+}	2	–	–	1.0	1.8*	2.5	–	–	ns	–	–	4	2	5,10,13	8	1,16
	t_{4-2-}	2	–	–	↓	↓	↓	–	–	↓	–	–	↓	2	↓	↓	↓
	t_{4+3-}	3	–	–				–	–		–	–		3			
	t_{4-3+}	3	–	–				–	–		–	–		3			
Rise Time	t_{2+}	2	–	–		1.5		–	–		–	–		2			
(20% to 80%)	t_{3+}	3	–	–		↓		–	–		–	–		3			
Fall Time	t_{2-}	2	–	–				–	–		–	–		2			
(20% to 80%)	t_{3-}	3	–	–	↓	↓	↓	–	–	↓	–	–	↓	3	↓	↓	↓

*Delay is 1.5 ns when inputs are driven differentially
Delay is 1.8 ns when inputs are driven single ended.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.



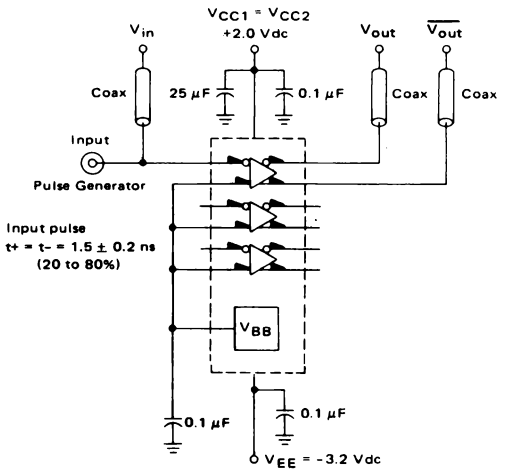
P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2

Characteristic	Symbol	Pin Under Test	MC10216P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	25	–	-	mAdc	4,9,12	–	–	–	5,10,13	8	1,16
Input Current	I_{inH}	4	–	–	–	–	115	–	–	μAdc	4	9,12	–	–	5,10,13	8	1,16
	I_{CBO}	4	–	–	–	–	1.0	–	–	μAdc	–	9,12	–	–	5,10,13	8,4	1,16
		9	–	–	–	–	1.0	–	–	μAdc	–	4,12	–	–	5,10,13	8,9	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–	–	5,10,13	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4	–	–	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	–	4	5,10,13	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	4	–	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	8	1,16
Switching Times (50-ohm Load)													Pulse In	Pulse Out		-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{4+2+}	2	–	–	1.0	1.8*	2.5	–	–	ns	–	–	4	2	5,10,13	8	1,16
	t_{4-2-}	2	–	–				–	–		–	–		2			
	t_{4+3-}	3	–	–				–	–		–	–		3			
	t_{4-3+}	3	–	–				–	–		–	–		3			
Rise Time (20% to 80%)	t_{2+}	2	–	–		1.5		–	–		–	–		2			
	t_{3+}	3	–	–				–	–		–	–		3			
Fall Time (20% to 80%)	t_{2-}	2	–	–				–	–		–	–		2			
	t_{3-}	3	–	–				–	–		–	–		3			

*Delay is 1.5 ns when inputs are driven differentially
Delay is 1.8 ns when inputs are driven single ended

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



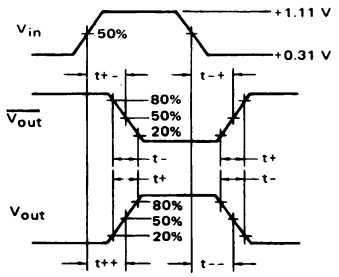
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs connected to a 50-ohm resistor to ground.

One input from each gate must be tied to V_{BB} (Pin 11) during testing.

PROPAGATION DELAY



MC10231

The MC10231 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock(C_C) and Clock Enable ($\overline{C_E}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times allow high frequency operation over 200 MHz.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

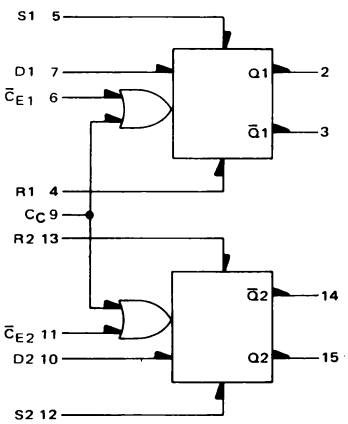
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

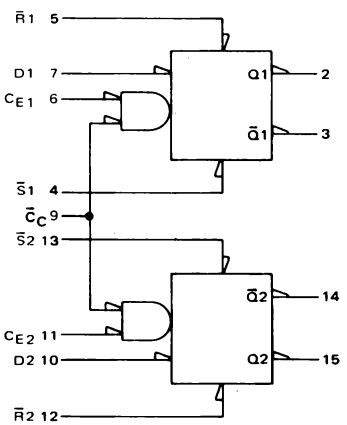
ϕ = Don't Care
$C = \overline{C}_E + C_C$.
A clock H is a clock transition from a low to a high state.

P_D = 270 mW typ/pkg (No Load)
f_{Tog} = 225 MHz typ

POSITIVE LOGIC



NEGATIVE LOGIC

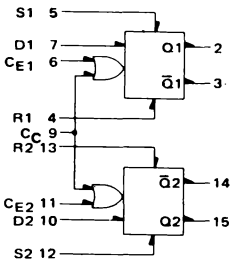


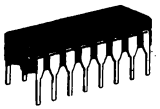
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

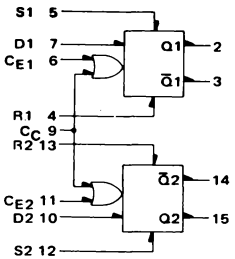
Characteristic	Symbol	Pin Under Test	MC10231L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}†) Gnd
Power Supply Drain Current	I_E	8	–	–	–	52	65	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	410	–	–	μAdc	4	–	–	–	8	1, 16
		5	–	–	–	–	410	–	–	↓	5	–	–	–	↓	↓
		6	–	–	–	–	220	–	–		6	–	–	–		
		7	–	–	–	–	220	–	–		7	–	–	–		
		9	–	–	–	–	290	–	–		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1, 16
		6,7,9*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1, 16
		2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1, 16
		3†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1, 16
		2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1, 16
		3†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	9	8	1, 16
Switching Times Clock Input											+1.11 Vdc		Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{9+2-}	2	1.4	3.4	1.5	–	3.3	1.5	3.7	ns	–	–	9	2	8	1, 16
	t_{6+2+}	2	1.4	3.4	1.5	–	3.3	1.5	3.7		7	–	6	2		
Rise Time (20 to 80%)	t_{2+}	2	0.9	3.3	1.0	–	3.1	1.0	3.5	↓	7	–	9	2	↓	↓
Fall Time (20 to 80%)	t_{2-}	2	0.9	3.3	1.0	–	3.1	1.0	3.5		–	–	9	2		
Set Input Propagation Delay	t_{5+2+}	2	1.0	3.4	1.1	–	3.3	1.1	3.7	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15				–					6	–	12	15		
	t_{5+3+}	3				–					–	–	5	3		
	t_{12+14-}	14	↓	↓	↓	–	↓	↓	↓	↓	9	–	12	14	↓	↓
Reset Input Propagation Delay	t_{4+2-}	2			1.1	–	3.3			ns	–	–	4	2	8	1, 16
	t_{13+15-}	15				–					6	–	13	15		
	t_{4+3-}	3				–					–	–	4	3		
	t_{13+14+}	14	↓	↓	↓	–	↓	↓	↓	↓	9	–	13	14	↓	↓
Setup Time	t_{Setup}	7	–	–	1.0	–	–	–	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{Hold}	7	–	–	0.75	–	–	–	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	200	–	200	250	–	200	–	MHz	• •	–	6	2	8	1, 16

†Individually test each input; apply V_{IL} min to pin under test.

‡Output level to be measured after a clock pulse has been applied to the $\bar{C}_E$ input (pin 6)

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.



P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10231P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	52	65	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	410	–	–	μAdc	4	–	–	–	8	1, 16
		5	–	–	–	–	410	–	–		5	–	–	–		
		6	–	–	–	–	220	–	–		6	–	–	–		
		7	–	–	–	–	220	–	–		7	–	–	–		
		9	–	–	–	–	220	–	–		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1, 16
		6,7,9*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1, 16
		2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1, 16
		3†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1, 16
		2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1, 16
		3†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	9	8	1, 16
Switching Times											+1.11 Vdc		Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input																
Propagation Delay	t_{9+2-}	2	–	–	–	2.0	–	–	–	ns	–	–	9	2	8	1, 16
	t_{6+2+}	2	–	–	–	2.0	–	–	–		7	–	6	2		
Rise Time (20 to 80%)	t_{2+}	2	–	–	–	1.3	–	–	–		7	–	9	2		
Fall Time (20 to 80%)	t_{2-}	2	–	–	–	1.3	–	–	–		–	–	9	2		
Set Input Propagation Delay	t_{5+2+}	2	–	–	–	2.0	–	–	–	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15	–	–	–		–	–	–		6	–	12	15		
	t_{5+3+}	3	–	–	–		–	–	–		–	–	5	3		
	t_{12+14-}	14	–	–	–		–	–	–		9	–	12	14		
Reset Input Propagation Delay	t_{4+2-}	2	–	–	–	2.0	–	–	–	ns	–	–	4	2	8	1, 16
	t_{13+15-}	15	–	–	–		–	–	–		6	–	13	15		
	t_{4+3-}	3	–	–	–		–	–	–		–	–	4	3		
	t_{13+14+}	14	–	–	–		–	–	–		9	–	13	14		
Setup Time	t_{Setup}	7	–	–	1.0	–	–	–	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{Hold}	7	–	–	0.75	–	–	–	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	–	–	200	2.25	–	–	–	MHz	• •	–	6	2	8	1, 16

*Individually test each input; apply $V_{IL\ min}$ to pin under test.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6)  V_{IH} max, V_{IL} min

FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT

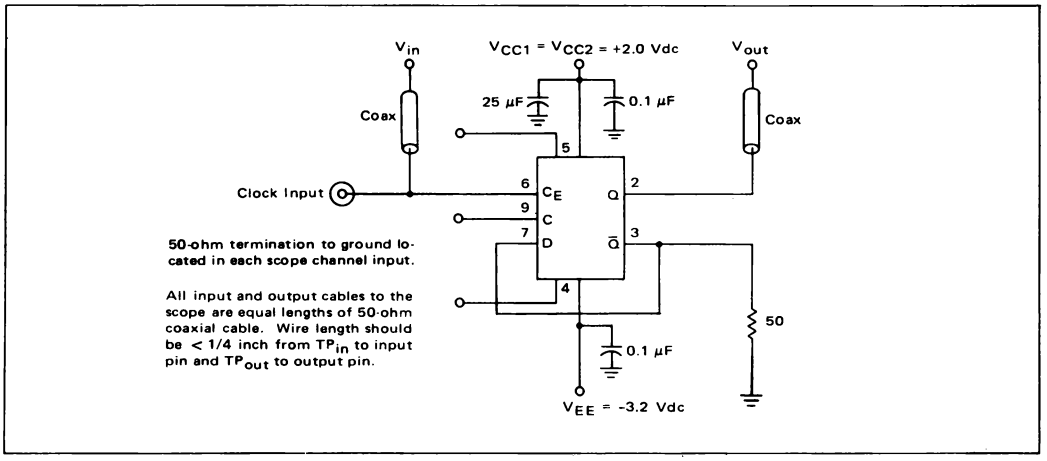
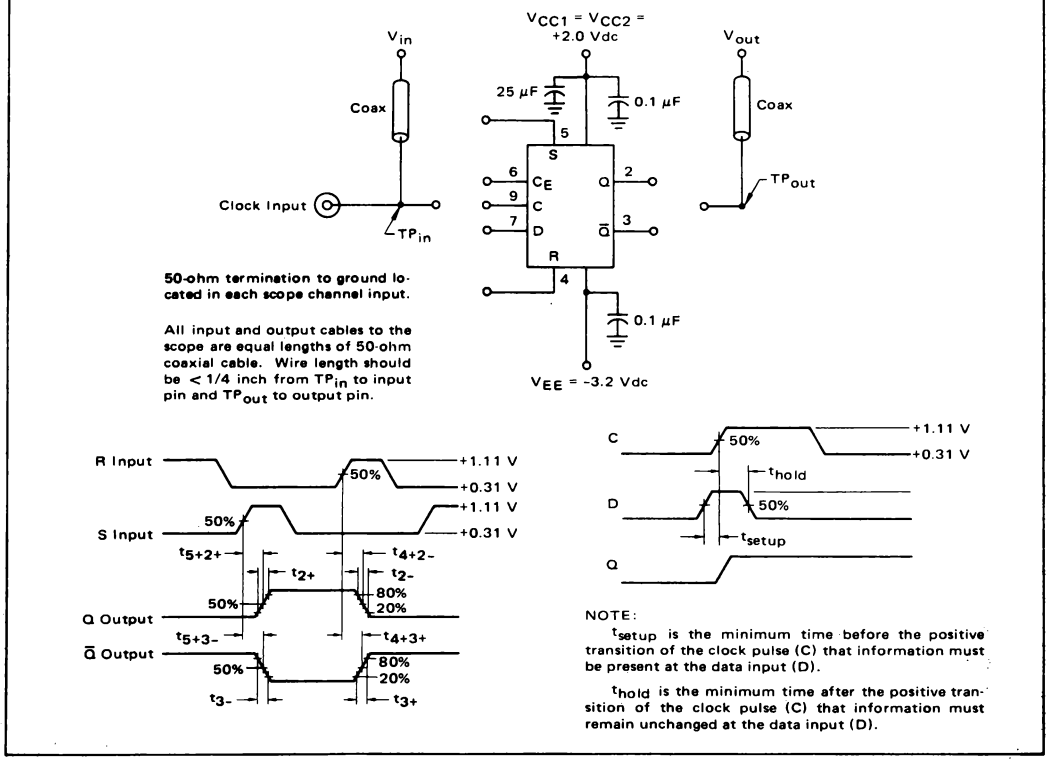


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

MC10287

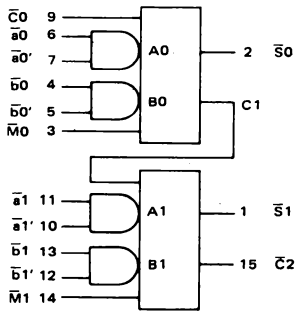
Advance Information

P_D = 400 mW typ/pkg (No Load)
t_{pd}: (Outputs loaded 1 kΩ to V_{EE})
C0 to C2 1.7 ns typ
a0 to C2 2.8
a0 to S0 2.7
b0 to S0 3.1
a0 to S1 3.9
b0 to S1 4.4
M0 to S1 8.7

The MC10287 is a dual high speed iterative multiplier. It is designed for use as an array multiplier block. Each device is a modified full adder/subtractor that forms a single-bit binary product at each operand input of the adder. Internal carry lookahead is employed for high speed operation.

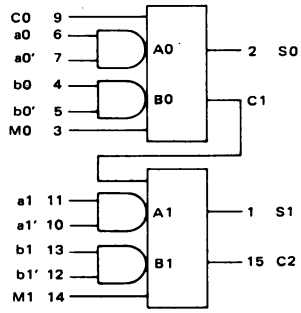
An addition or subtraction is selected by mode controls (M0, M1). The mode controls are buffered such that they can be grounded or taken to a standard high logic level to accomplish subtraction. When left open or taken to a low logic level, M0 and M1 cause addition.

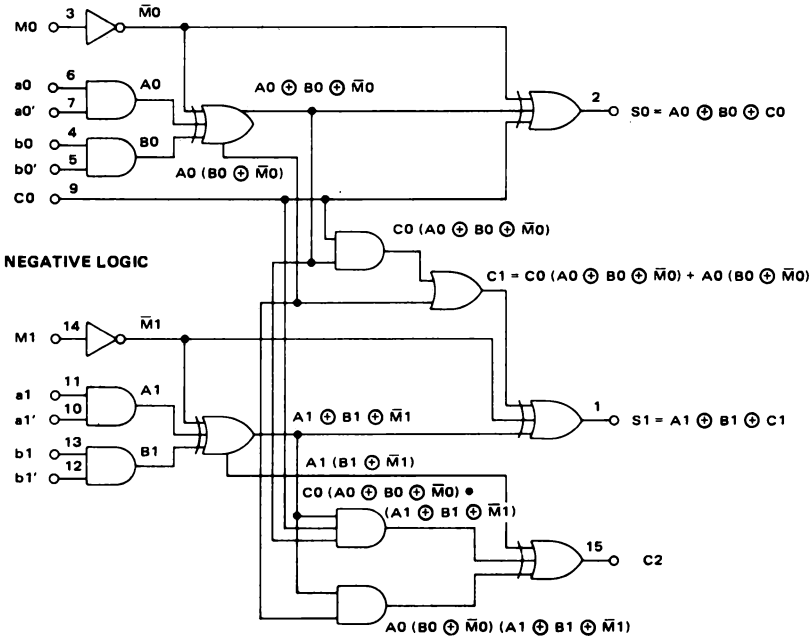
POSITIVE LOGIC



V_{CC} = Pin 16
V_{EE} = Pin 8

NEGATIVE LOGIC





This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

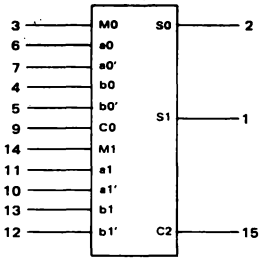
MC10287 FUNCTIONAL TRUTH TABLE

M1	M0	b1	b1'	a1	a1'	b0	b0'	a0	a0'	C0	S0	S1	C2	
14	3	13	12	11	10	4	5	6	7	9	2	1	15	Word
H	H	H	H	H	H	H	H	H	H	H	H	H	H	0
H	H	H	H	H	H	H	H	H	H	L	L	L	L	1
H	H	H	H	H	H	H	H	L	L	H	L	L	L	2
H	H	H	H	H	H	H	H	L	L	L	H	L	L	3
H	H	H	H	H	H	L	L	H	H	H	L	H	H	4
H	H	H	H	H	H	L	L	H	H	L	H	H	H	5
H	H	H	H	H	H	L	L	L	L	H	H	H	H	6
H	H	H	H	H	H	L	L	L	L	L	L	L	L	7
H	H	H	H	L	L	H	H	H	H	H	H	L	L	8
H	H	H	H	L	L	H	H	H	H	L	L	H	L	9
H	H	H	H	L	L	H	H	L	L	H	L	H	L	10
H	H	H	H	L	L	H	H	L	L	L	H	H	L	11
H	H	H	H	L	L	L	L	H	H	H	L	L	L	12
H	H	H	H	L	L	L	L	H	H	L	H	L	L	13
H	H	H	H	L	L	L	L	L	L	H	H	L	L	14
H	H	H	H	L	L	L	L	L	L	L	L	H	L	15
H	H	L	L	H	H	H	H	H	H	H	H	L	H	16
H	H	L	L	H	H	H	H	H	H	L	L	H	H	17
H	H	L	L	H	H	H	H	L	L	H	L	H	H	18
H	H	L	L	H	H	H	H	L	L	L	H	H	H	19
H	H	L	L	H	H	L	L	H	H	H	L	L	H	20
H	H	L	L	H	H	L	L	H	H	L	H	L	H	21
H	H	L	L	H	H	L	L	L	L	H	H	L	H	22
H	H	L	L	H	H	L	L	L	L	L	L	H	H	23
H	H	L	L	L	L	H	H	H	H	H	H	H	H	24
H	H	L	L	L	L	H	H	H	H	L	L	L	L	25
H	H	L	L	L	L	H	H	L	L	H	L	L	L	26
H	H	L	L	L	L	H	H	L	L	L	H	L	L	27
H	H	L	L	L	L	L	L	H	H	H	L	H	H	28
H	H	L	L	L	L	L	L	H	H	L	H	H	H	29
H	H	L	L	L	L	L	L	L	L	H	H	H	H	30
H	H	L	L	L	L	L	L	L	L	L	L	L	L	31
H	L	H	H	H	H	H	H	H	H	H	H	H	H	32
H	L	H	H	H	H	H	H	H	H	L	L	H	H	33
H	L	H	H	H	H	H	H	L	L	H	L	H	H	34
H	L	H	H	H	H	H	H	L	L	L	H	L	L	35
H	L	H	H	H	H	L	L	H	H	H	L	H	H	36
H	L	H	H	H	H	L	L	H	H	L	H	L	L	37
H	L	H	H	H	H	L	L	L	L	H	H	L	L	38
H	L	H	H	H	H	L	L	L	L	L	L	L	L	39
H	L	H	H	L	L	H	H	H	H	H	H	L	L	40
H	L	H	H	L	L	H	H	H	H	L	L	L	L	41
H	L	H	H	L	L	H	H	L	L	H	L	L	L	42
H	L	H	H	L	L	H	H	L	L	L	H	L	L	43
H	L	H	H	L	L	L	L	H	H	H	L	H	L	44
H	L	H	H	L	L	L	L	H	H	L	H	H	L	45
H	L	H	H	L	L	L	L	L	L	H	H	H	L	46
H	L	H	H	L	L	L	L	L	L	L	L	H	L	47
H	L	L	L	H	H	H	H	H	H	H	H	L	H	48
H	L	L	L	H	H	H	H	H	H	L	L	L	H	49
H	L	L	L	H	H	H	H	L	L	H	L	L	H	50
H	L	L	L	H	H	H	H	L	L	L	H	H	H	51
H	L	L	L	H	H	L	L	H	H	H	L	L	H	52
H	L	L	L	H	H	L	L	H	H	L	H	H	H	53
H	L	L	L	H	H	L	L	L	L	H	H	H	H	54
H	L	L	L	H	H	L	L	L	L	L	L	H	H	55
H	L	L	L	L	L	H	H	H	H	H	H	H	H	56
H	L	L	L	L	L	H	H	H	H	L	L	H	H	57
H	L	L	L	L	L	H	H	L	L	H	L	H	H	58
H	L	L	L	L	L	H	H	L	L	L	H	L	L	59
H	L	L	L	L	L	L	L	H	H	H	L	H	H	60
H	L	L	L	L	L	L	L	H	H	L	H	L	L	61
H	L	L	L	L	L	L	L	L	L	H	H	L	L	62
H	L	L	L	L	L	L	L	L	L	L	L	L	L	63
L	H	H	H	H	H	H	H	H	H	H	H	H	H	64
L	H	H	H	H	H	H	H	H	H	L	L	L	H	65
L	H	H	H	H	H	H	H	L	L	H	L	L	H	66
L	H	H	H	H	H	H	H	L	L	L	H	L	H	67

M1	M0	b1	b1'	a1	a1'	b0	b0'	a0	a0'	C0	S0	S1	C2	
14	3	13	12	11	10	4	5	6	7	9	2	1	15	Word
L	H	H	H	H	H	L	L	H	H	H	L	H	H	68
L	H	H	H	H	H	L	L	H	H	L	H	H	H	69
L	H	H	H	H	H	L	L	L	L	H	H	H	H	70
L	H	H	H	H	H	L	L	L	L	L	L	L	H	71
L	H	H	H	L	L	H	H	H	H	H	H	L	H	72
L	H	H	H	L	L	H	H	H	H	L	L	H	L	73
L	H	H	H	L	L	H	H	L	L	H	L	H	L	74
L	H	H	H	L	L	H	H	L	L	L	H	H	L	75
L	H	H	H	L	L	L	L	H	H	H	L	L	H	76
L	H	H	H	L	L	L	L	H	H	L	H	L	H	77
L	H	H	H	L	L	L	L	L	L	H	H	L	H	78
L	H	H	H	L	L	L	L	L	L	L	L	H	L	79
L	H	L	L	H	H	H	H	H	H	H	H	L	H	80
L	H	L	L	H	H	H	H	H	H	L	L	H	L	81
L	H	L	L	H	H	H	H	L	L	H	L	H	L	82
L	H	L	L	H	H	H	H	L	L	L	H	H	L	83
L	H	L	L	H	H	L	L	H	H	H	L	L	H	84
L	H	L	L	H	H	L	L	H	H	L	H	L	H	85
L	H	L	L	H	H	L	L	L	L	H	H	L	H	86
L	H	L	L	H	H	L	L	L	L	L	L	H	L	87
L	H	L	L	L	L	H	H	H	H	H	H	H	L	88
L	H	L	L	L	L	H	H	H	H	L	L	L	L	89
L	H	L	L	L	L	H	H	L	L	H	L	L	L	90
L	H	L	L	L	L	H	H	L	L	L	H	L	L	91
L	H	L	L	L	L	L	L	H	H	H	L	H	H	92
L	H	L	L	L	L	L	L	H	H	L	H	H	L	93
L	H	L	L	L	L	L	L	L	L	H	H	H	L	94
L	H	L	L	L	L	L	L	L	L	L	L	L	L	95
L	L	H	H	H	H	H	H	H	H	H	H	H	H	96
L	L	H	H	H	H	H	H	H	H	L	L	H	H	97
L	L	H	H	H	H	H	H	L	L	H	L	H	H	98
L	L	H	H	H	H	H	H	L	L	L	H	L	H	99
L	L	H	H	H	H	L	L	H	H	H	L	H	H	100
L	L	H	H	H	H	L	L	H	H	L	H	L	H	101
L	L	H	H	H	H	L	L	L	L	H	H	L	H	102
L	L	H	H	H	H	L	L	L	L	L	L	L	H	103
L	L	H	H	L	L	H	H	H	H	H	H	L	H	104
L	L	H	H	L	L	H	H	H	H	L	L	L	H	105
L	L	H	H	L	L	H	H	L	L	H	L	L	H	106
L	L	H	H	L	L	H	H	L	L	L	H	H	L	107
L	L	H	H	L	L	H	H	L	L	H	L	L	H	108
L	L	H	H	L	L	L	L	H	H	L	H	H	L	109
L	L	H	H	L	L	L	L	L	L	H	H	H	L	110
L	L	H	H	L	L	L	L	L	L	L	L	H	L	111
L	L	L	L	H	H	H	H	H	H	H	H	L	H	112
L	L	L	L	H	H	H	H	H	H	L	L	L	H	113
L	L	L	L	H	H	H	H	L	L	H	L	L	H	114
L	L	L	L	H	H	H	H	L	L	L	H	H	L	115
L	L	L	L	H	H	L	L	H	H	H	L	L	H	116
L	L	L	L	H	H	L	L	H	H	L	H	H	L	117
L	L	L	L	H	H	L	L	L	L	H	H	H	L	118
L	L	L	L	H	H	L	L	L	L	L	L	H	L	119
L	L	L	L	L	L	H	H	H	H	H	H	H	L	120
L	L	L	L	L	L	H	H	H	H	L	L	H	L	121
L	L	L	L	L	L	H	H	L	L	H	L	H	L	122
L	L	L	L	L	L	H	H	L	L	L	H	L	L	123
L	L	L	L	L	L	L	L	H	H	H	L	H	L	124
L	L	L	L	L	L	L	L	H	H	L	H	L	L	125
L	L	L	L	L	L	L	L	L	L	H	H	L	L	126
L	L	L	L	L	L	L	L	L	L	L	L	L	L	127
L	L	H	L	L	L	L	L	L	L	L	L	H	L	128
L	L	L	H	L	L	L	L	L	L	L	L	H	L	129
L	L	L	L	H	L	L	L	L	L	L	L	H	L	130
L	L	L	L	L	H	L	L	L	L	L	L	H	L	131
L	L	L	L	L	L	H	L	L	L	L	H	L	L	132
L	L	L	L	L	L	L	H	L	L	L	H	L	L	133
L	L	L	L	L	L	L	L	H	L	L	H	L	L	134
L	L	L	L	L	L	L	L	L	H	L	H	L	L	135

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.



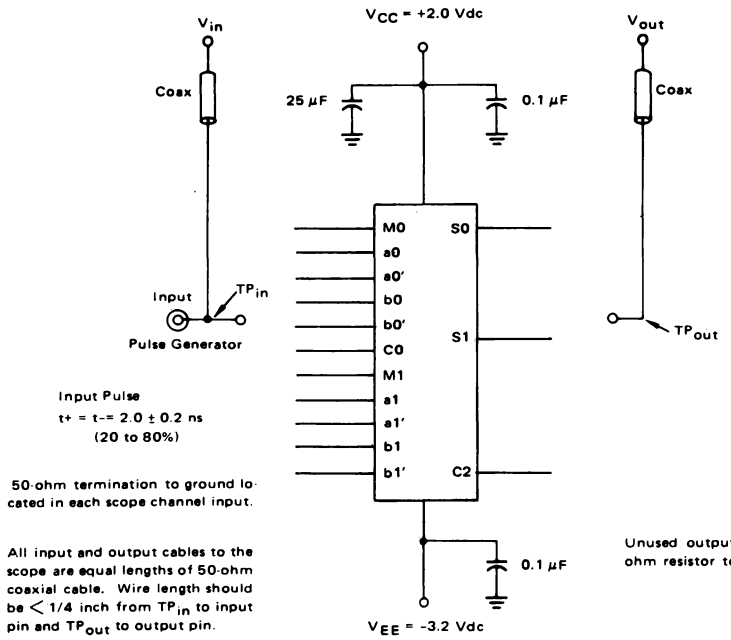
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10287 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	77	96	–	–	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	3	–	–	–	–	200	–	–	μAdc	3	–	–	–	8	16
		4	–	–	–	–	220	–	–		4	–	–	–		
		6	–	–	–	–	265	–	–		6	–	–	–		
		9	–	–	–	–	410	–	–		9	–	–	–		
	I_{inL}	3	–	–	0.5	–	–	–	–	μAdc	–	3	–	–	8	16
Logic "1" Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,9	–	–	–	8	16
		2				–					9	–	–	–		
		15				–					6,9,10	–	–	–		
Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	16
		2				–					–	–	–	–		
		15				–					–	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6,7	–	9	–	8	16
		2		–		–	–		–		–	–	4	–		
		15		–		–	–		–		6,7,10,11	–	9	–		
Logic "0" Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6,7	–	–	9	8	16
		2	–		–	–		–			–	–	–	4		
		15	–		–	–		–			6,7,10,11	–	–	9		
Switching Times											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay (50 ohm load)	t_{9+15+}	15	–	–	–	2.0	–	–	–	ns	3	•	9	15	8	16
	t_{6-1-}	1	–	–	–	4.5	–	–	–		3		6	1		
	t_{4+2-}	2	–	–	–	3.5	–	–	–		6		4	2		
	t_{4-1+}	1	–	–	–	4.5	–	–	–		6		4	1		
	t_{11+1-}	1	–	–	–	3.0	–	–	–		13		11	1		
	t_{13+1-}	1	–	–	–	3.5	–	–	–		3,9		13	1		
	t_{3+1+}	1	–	–	–	8.5	–	–	–		9		3	1		
	t_{3+15+}	15	–	–	–	8.0	–	–	–		9,14		3	15		
	t_{14+15+}	15	–	–	–	8.0	–	–	–		11		14	15		
Rise Time (20% to 80%)	t_{15+}	15	–	–	–	2.0	–	–	–		–		3	15		
Fall Time (20% to 80%)	t_{15-}	15	–	–	–	2.0	–	–	–		–		3	15		

*Apply +0.31 V to all other inputs.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



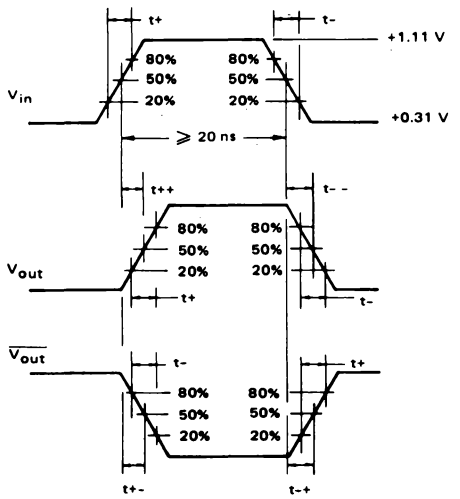
Input Pulse
t+ = t- = 2.0 ± 0.2 ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are tied to a 50-ohm resistor to ground.

PROPAGATION DELAY



APPLICATION INFORMATION

The MC10287 is a stand alone fully iterative dual multiplier cell. It is intended for use in parallel multiplier arrays where maximum speed is desired. Each cell is a modified gated adder/subtractor individually controlled by a mode select line. Internal carry lookahead (also called anticipated carry) is used to minimize sum and carry out delay times.

The mode controls are specifically buffered such that they can be grounded. Normally, MECL 10,000 device inputs should not be placed at ground to establish a high logic level. However, M0 and M1 can be used at ground potential for ease of layout in large arrays.

An array multiplier is defined as a multi-input, multi-output combinational logic circuit that forms the product of two binary numbers. Binary multiplication can be treated in two categories, that is, simple magnitude multiplication and 4-quadrant multiplication (requiring both positive and negative numbers).

MAGNITUDE BINARY MULTIPLICATION

Magnitude multiplication consists of the product of two binary numbers in which all digits are number bits (no sign bit). Magnitude representation then includes only positive numbers.

Thus, for a 4-bit number X the representation is:

$$X = x_3\ x_2\ x_1\ x_0$$

A 4-bit by 4-bit product becomes:

$$Z = X \bullet Y = (x_3\ x_2\ x_1\ x_0) \bullet (y_3\ y_2\ y_1\ y_0)$$

The product consists of the sum of the single-bit products formed by this expression. The standard "parallelogram" matrix of the single-bit products (or summands) can be written:

$$\begin{array}{cccccccc} & & & & x_3y_0 & x_2y_0 & x_1y_0 & x_0y_0 \\ & & & x_3y_1 & x_2y_1 & x_1y_1 & x_0y_1 & \\ & & x_3y_2 & x_2y_2 & x_1y_2 & x_0y_2 & & \\ & x_3y_3 & x_2y_3 & x_1y_3 & x_0y_3 & & & \\ \hline z_7 & z_6 & z_5 & z_4 & z_3 & z_2 & z_1 & z_0 \end{array}$$

The MC10287 is used in an array summing the single-bit products to form the final result. It is observed that the arithmetic product of binary digits x_j and y_i is also the logical product (x_j times y_i = x_j AND y_i. The AND function on the operand inputs of the MC10287 forms the single-bit products of the matrix directly and sums them internally. For magnitude binary multiplication, the MC10287 functions as a dual full adder (M0, M1 are both low).

The partial product array can be summed using a number of different techniques. The fastest technique is some form of matrix reduction scheme that prevents carry propagation until the final level of summation. Several of these schemes are discussed in detail in Reference 1.

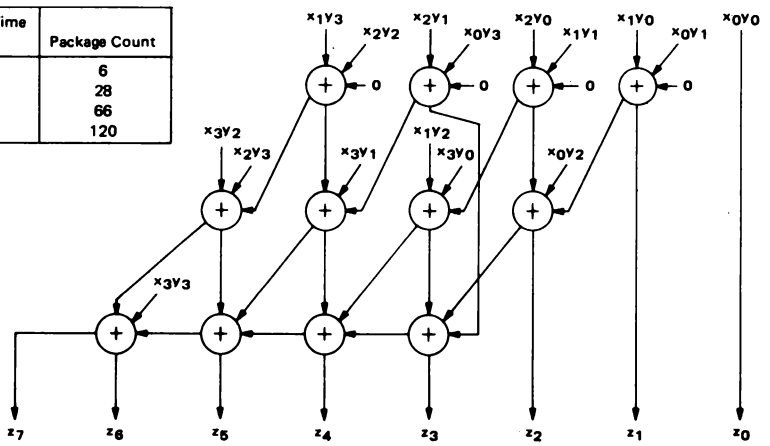
As an example, if the matrix is rearranged and written in a different form:

$$\begin{array}{cccccccc} & & & & x_0y_3 & & & \\ & & & x_1y_3 & x_3y_0 & x_2y_0 & x_1y_0 & x_0y_0 \\ & & x_2y_3 & x_3y_1 & x_2y_1 & x_1y_1 & x_0y_1 & \\ & x_3y_3 & x_3y_2 & x_2y_2 & x_1y_2 & x_0y_2 & & \\ \hline z_7 & z_6 & z_5 & z_4 & z_3 & z_2 & z_1 & z_0 \end{array}$$

TABLE 1 – TYPICAL MULTIPLY TIME FOR AN n-BIT BY n-BIT BINARY MAGNITUDE ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120

FIGURE 1 – 4-BIT BY 4-BIT MAGNITUDE ARRAY MULTIPLIER



The summation of the partial products for this configuration is shown in Figure 1. The number of MC10287's for an n-bit by n-bit array is n(n-1)/2. Note also that the least significant product bit ($z_0 = x_0y_0$) is formed by an individual AND gate (negative logic).

Table 1 gives package count and typical multiplication times for n-bit by n-bit magnitude multiplier arrays. The multiply times do not include wiring delays, and the package count does not include the gate for the least significant product bit.

FOUR-QUADRANT MULTIPLICATION

Sign-magnitude and 2's complement representations are commonly used for 4-quadrant multiplication. For sign-magnitude representation, the binary word consists of a sign bit and magnitude bits which indicate the absolute value of the number. For a 4-bit example:

$$X = x_s\ x_2\ x_1\ x_0$$

For $X \bullet Y = Z$

$$Z = X \bullet Y = (x_s\ x_2\ x_1\ x_0) \bullet (y_s\ y_2\ y_1\ y_0)$$

An array multiplier for this representation consists of an (n-1)-bit by (n-1)-bit magnitude multiplier that produces the product of the magnitude bits of X and Y and of logic that produces the proper product sign bit ($z_s = x_s \oplus y_s$).

2's complement representation also includes a sign bit which is a negative bit. That is:

$$X = -x_3\ x_2\ x_1\ x_0$$

where x_3 is the sign bit. The product of two 4-bit 2's complement numbers becomes:

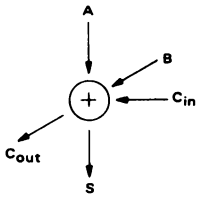
$$Z = X \bullet Y = (-x_3\ x_2\ x_1\ x_0) \bullet (-y_3\ y_2\ y_1\ y_0)$$

The matrix for this expression is:

			$-x_3y_0$	x_2y_0	x_1y_0	x_0y_0	
		$-x_3y_1$	x_2y_1	x_1y_1	x_0y_1		
	$-x_3y_2$	x_2y_2	x_1y_2	x_0y_2			
x_3y_3	$-x_2y_3$	$-x_1y_3$	$-x_0y_3$				
$-z_7$	z_6	z_5	z_4	z_3	z_2	z_1	z_0

The product is the sum of this array of single-bit products. However, notice that several summands are negative quantities. Therefore, they can not be simply added as is the magnitude binary multiplier. The subtraction capability of the MC10287 is utilized when considering these negative quantities.

A standard full adder is symbolized as:



in which all inputs are positive quantities. If one input is negative (such as B), the outputs C_{out} and S must be coded such that they can represent the 4 possible output conditions. If B can be a negative one or zero, the net output can then be:

$$\text{net output} = \begin{cases} -1 \\ 0 \\ +1 \\ +2 \end{cases}$$

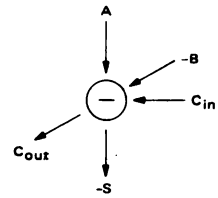
If C_{out}, whose weight is twice that of S, is assigned a positive value and S is a negative value, the above values can be represented:

$$\text{net output} = 2 \bullet C_{out} - S$$

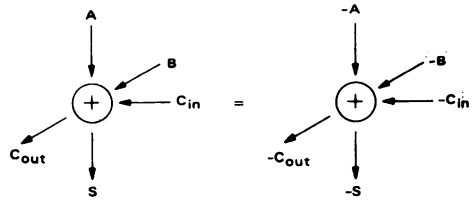
where:

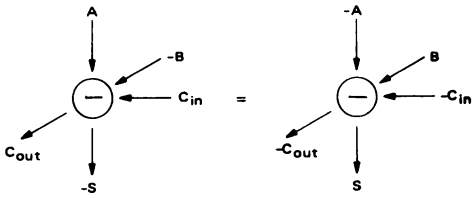
$$-1 = 0 - 1$$
$$0 = 0 - 0$$
$$+1 = 2 - 1$$
$$+2 = 2 - 0$$

If the truth table is written and logic equations generated, the result is a subtractor. That is, a subtractor used in place of a full adder produces the proper outputs. The symbol for the subtractor is:



Also, if the input variables are multiplied by -1, the outputs also are multiplied by -1. Thus, the following devices are equivalent:





A basic adder/subtractor can then handle all the varying situations that appear in the multiplication matrix.

If the 2's complement matrix is rearranged:

			$-x_0y_3$				
		$-x_1y_3$	$-x_3y_0$	x_2y_0	x_1y_0	x_0y_0	
	$-x_2y_3$	$-x_3y_1$	x_2y_1	x_1y_1	x_0y_1		
x_3y_3	$-x_3y_2$	x_2y_2	x_1y_2	x_0y_2			
$-z_7$ z_6	z_5	z_4	z_3	z_2	z_1	z_0	

The adder/subtractor array for this configuration is shown in Figure 2. Care must be taken to insure that the proper mode of operation (add or subtract) appears at each summing node as a function of the positive and negative weighted inputs.

The summand matrix can be altered different ways to speed up the multiplier array. Reference 2 discusses the algorithm used with the MC10287 in detail. Also, the techniques of Reference 1 also apply to 2's complement arrays using the MC10287.

Table 2 gives typical multiply times for 2's complement arrays for n-bit by n-bit multipliers.

TABLE 2 – TYPICAL MULTIPLY TIME FOR AN n-BIT BY n-BIT 2's COMPLEMENT ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120

IMPROVED SWITCHING DELAYS

The specified ac switching delays are given for output loading of 50 Ω to -2 volts. With lower output current, propagation delays will be improved and decreased multiply times can result. For output loading of 1 kΩ to V_{EE}, the following delays are typical.

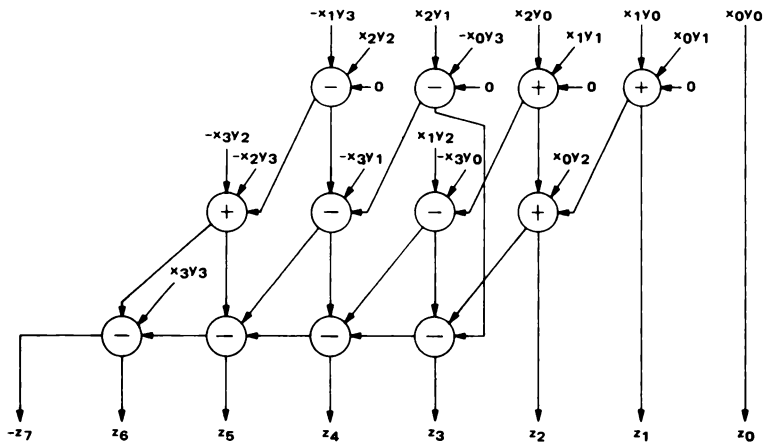
Input	Output	Delay (ns)
C0	C2	1.7
A0	C2	2.8
A0	S0	2.8
B0	S0	3.1
A0	S1	3.9
B0	S1	4.4
M0	S1	8.7

REFERENCE AND ACKNOWLEDGEMENT

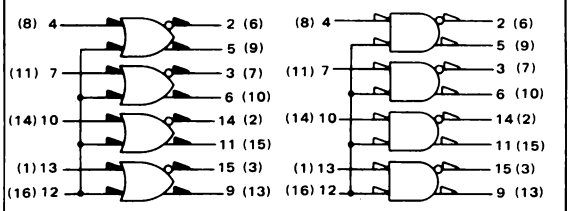
The techniques for implementing the MC10287 in multiplier arrays resulted from work done originally at M.I.T. Lincoln Laboratories. Also, applications information presented here developed in part from personal correspondence with P. Blankenship of Lincoln Labs. The following references are useful in developing multipliers using the MC10287:

1. A. Habibi and P.A. Wintz, "Fast Multipliers," *IEEE Trans. Computers* (Short Notes), Vol. C-19, Feb. 1970, pp. 153-157.
2. S.D. Pezaris, "A 40-ns 17-Bit by 17-Bit Array Multiplier", *IEEE Trans. Computers*, Vol. C-20, Number 4, April, 1971, pp. 442-447.

FIGURE 2 – 4-BIT BY 4-BIT 2's COMPLEMENT ARRAY MULTIPLIER



MC10501



Numbers at ends of terminals denote pin numbers for L package (Case 620).

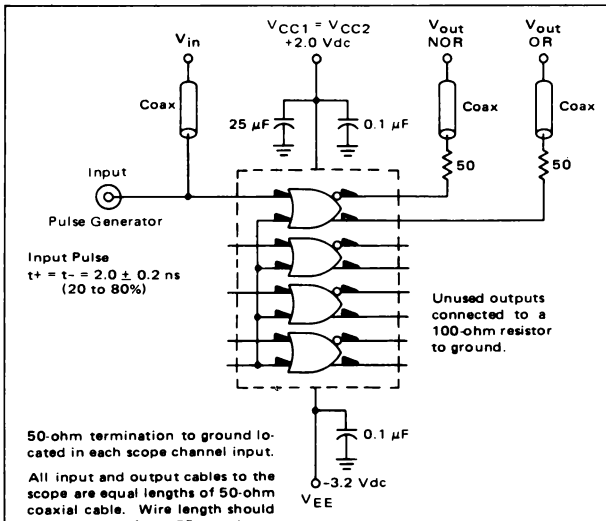
Numbers in parenthesis denote pin numbers for F package (Case 650).

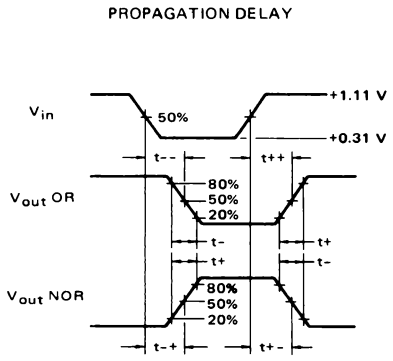
CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

The MC10501 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12 in the L package and pin 16 in the F package. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

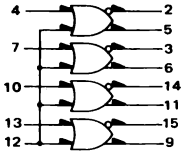


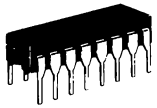


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





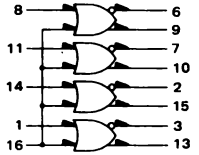
L SUFFIX
CERAMIC PACKAGE
CASE 620

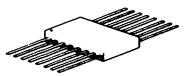
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10501L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	450	–	–	265	–	265	µAdc	4	–	–	–	8	1,16
		12	–	910	–	–	535	–	535	µAdc	12	–	–	–	8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3	–	µAdc	–	4	–	–	8	1,16
		12	0.5	–	0.5	–	–	0.3	–	µAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	5	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	12	–	–	–	8	1,16
		5	↓	↓	↓	–	↓	↓	↓	↓	4	–	–	–	↓	↓
		2				–					–	–	–	–		
		2				–					–	–	–	–		
Logic "0" Output Voltage	V_{OL}	5	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	8	1,16
		5	↓	↓	↓	–	↓	↓	↓	↓	–	–	–	–	↓	↓
		2				–					12	–	–	–		
		2				–					4	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	5	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	12	–	8	1,16
		5	↓	–	↓	–	–	↓	–	↓	–	–	4	–	↓	↓
		2		–		–	–		–		–	–	–	12		
		2		–		–	–		–		–	–	–	4		
Logic "0" Threshold Voltage	V_{OLA}	5	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	12	8	1,16
		5	–	↓	–	–	↓	–	↓	↓	–	–	–	4	↓	↓
		2	–		–	–		–			–	–	12	–		
		2	–		–	–		–			–	–	4	–		
Switching Times (100-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2-}	2	1.0	3.7	1.0	2.0	2.9	1.0	3.7	ns	–	–	4	2	8	1,16
	t_{4-2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{4+5+}	5									–	–		5		
	t_{4-5-}	5									–	–		5		
Rise Time (20 to 80%)	t_{2+}	2		4.0	1.1		3.3		4.0		–	–		2		
	t_{5+}	5									–	–		5		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{5-}	5									–	–		5		

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

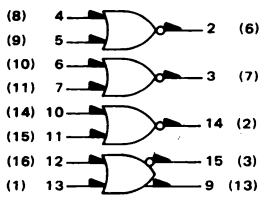
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.830	-1.920	-1.255	-1.510	-5.2
+25°C	-0.720	-1.850	-1.105	-1.475	-5.2
+125°C	-0.580	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10501F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	29	–	20	26	–	29	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	8	–	450	–	–	265	–	265	µAdc	8	–	–	–	12	4,5
		16	–	910	–	–	535	–	535	µAdc	16	–	–	–	12	4,5
	I_{inL}	8	0.5	–	0.5	–	–	0.3	–	µAdc	–	8	–	–	12	4,5
		16	0.5	–	0.5	–	–	0.3	–	µAdc	–	16	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	9	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	16	–	–	–	12	4,5
		9	↓	↓	↓	–	↓	↓	↓	↓	8	–	–	–	↓	↓
		6				–					–	–	–	–		
		6				–					–	–	–	–		
Logic "0" Output Voltage	V_{OL}	9	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	12	4,5
		9	↓	↓	↓	–	↓	↓	↓	↓	–	–	–	–	↓	↓
		6				–					16	–	–	–		
		6				–					8	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	9	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	16	–	12	4,5
		9	↓	–	↓	–	–	↓	–	↓	–	–	8	–	↓	↓
		6		–		–	–		–		–	–	–	16		
		6		–		–	–		–		–	–	–	8		
Logic "0" Threshold Voltage	V_{OLA}	9	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	16	12	4,5
		9	–	↓	–	–	↓	–	↓	↓	–	–	–	8	↓	↓
		6	–		–	–		–			–	–	16	–		
		6	–		–	–		–			–	–	8	–		
Switching Times (100-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{8+6-}	6	–	–	1.0	2.0	2.9	–	–	ns	–	–	8	6	12	4,5
	t_{8-6+}	6	–	–	↓	↓	↓	–	–	↓	–	–	↓	6	↓	↓
	t_{8+9+}	9	–	–				–	–		–	–		9		
	t_{8-9-}	9	–	–				–	–		–	–		9		
Rise Time (20 to 80%)	t_{6+}	6	–	–	1.1		3.3	–	–		–	–		6		
	t_{9+}	9	–	–				–	–		–	–		9		
Fall Time (20 to 80%)	t_{6-}	6	–	–	↓	↓	↓	–	–	↓	–	–	↓	6	↓	↓
	t_{9-}	9	–	–				–	–		–	–		9		

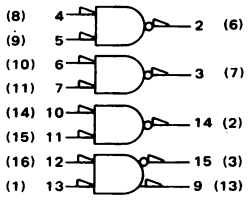
MC10502

The MC10502 is a quad 2-input NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

POSITIVE LOGIC



NEGATIVE LOGIC



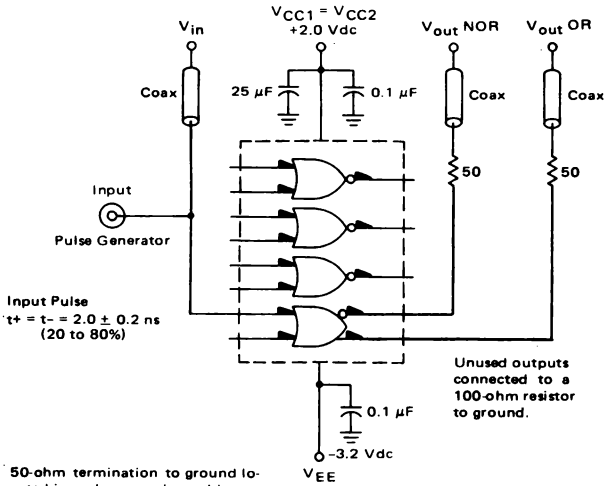
Numbers at ends of terminals denote pin numbers for L package (Case 620).

Numbers in parenthesis denote pin numbers for F package (Case 650).

CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

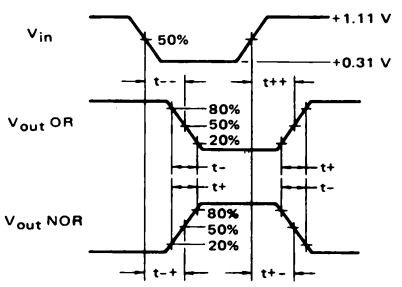
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

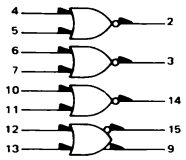
PROPAGATION DELAY

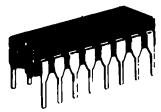


See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





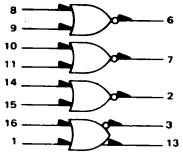
L SUFFIX
CERAMIC PACKAGE
CASE 620

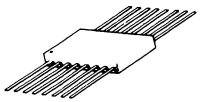
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.830	-1.920	-1.255	-1.510	-5.2
+25°C	-0.720	-1.850	-1.105	-1.475	-5.2
+125°C	-0.580	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10502L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	12	–	450	–	–	265	–	265	µAdc	12	–	–	–	8	1,16
	I_{inL}	12	0.5	–	0.5	–	–	0.3	–	µAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	9	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	12	–	–	–	8	1,16
		9	↓	↓	↓	–	↓	↓	↓	↓	13	–	–	–	↓	↓
		15				–					–	–	–	–		
		15				–					–	–	–	–		
Logic "0" Output Voltage	V_{OL}	9	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	8	1,16
		9	↓	↓	↓	–	↓	↓	↓	↓	–	–	–	–	↓	↓
		15				–					12	–	–	–		
		15				–					13	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	9	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	12	–	8	1,16
		9	↓	–	↓	–	–	↓	–	↓	–	–	13	–	↓	↓
		15		–		–	–		–		–	–	–	12		
		15		–		–	–		–		–	–	–	13		
Logic "0" Threshold Voltage	V_{OLA}	9	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	12	8	1,16
		9	–	↓	–	–	↓	–	↓	↓	–	–	–	13	↓	↓
		15	–		–	–		–			–	–	12	–		
		15	–		–	–		–			–	–	13	–		
Switching Times (100-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{12+15-}	15	1.0	3.7	1.0	2.0	2.9	1.0	3.7	ns	–	–	12	15	8	1,16
	t_{12-15+}	15	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	15	↓	↓
	t_{12+9+}	9									–	–		9		
	t_{12-9-}	9									–	–		9		
Rise Time	t_{15+}	15		4.0	1.1		3.3		4.0		–	–		15		
(20 to 80%)	t_{9+}	9									–	–		9		
Fall Time	t_{15-}	15									–	–		15		
(20 to 80%)	t_{9-}	9									–	–		9		

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

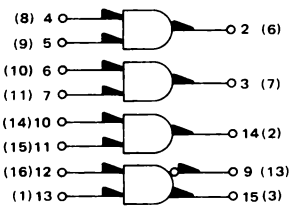
Characteristic	Symbol	Pin Under Test	MC10502F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	29	–	20	26	–	29	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	16	–	450	–	–	265	–	265	µAdc	16	–	–	–	12	4,5
	I_{inL}	16	0.5	–	0.5	–		0.3	–	µAdc	–	16	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	13	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	16	–	–	–	12	4,5
		13	↓	↓	↓	–	↓	↓	↓	↓	1	–	–	–	↓	↓
		3				–					–	–	–	–		
		3				–					–	–	–	–		
Logic "0" Output Voltage	V_{OL}	13	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	12	4,5
		13	↓	↓	↓	–	↓	↓	↓	↓	–	–	–	–	↓	↓
		3				–					16	–	–	–		
		3				–					1	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	13	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	16	–	12	4,5
		13	↓	–	↓	–	–	↓	–	↓	–	–	1	–	↓	↓
		3		–		–	–		–		–	–	–	16		
		3		–		–	–		–		–	–	–	1		
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	16	12	4,5
		13	–	↓	–	–	↓	–	↓	↓	–	–	–	1	↓	↓
		3	–		–	–		–			–	–	16	–		
		3	–		–	–		–			–	–	1	–		
Switching Times (100-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{16+3-}	3	–	–	1.0	2.0	2.9	–	–	ns	–	–	16	3	12	4,5
	t_{16+3+}	3	–	–	↓	↓	↓	–	–	↓	–	–	↓	3	↓	↓
	t_{16+13+}	13	–	–				–	–		–	–		13		
	t_{16+13-}	13	–	–				–	–		–	–		13		
Rise Time	t_{3+}	3	–	–	1.1		3.3	–	–		–	–		3		
(20 to 80%)	t_{13+}	13	–	–				–	–		–	–		13		
Fall Time	t_{3-}	3	–	–	↓	↓	↓	–	–	↓	–	–	↓	3	↓	↓
(20 to 80%)	t_{13-}	13	–	–				–	–		–	–		13		

MC10504

P_D = 35 mW typ/gate (No load)
t_{pd} = 2.7 ns typ
Output Rise and Fall Times:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

The MC10504 provides a very useful low power, high speed logic AND function. High Z input pulldown resistors allow high dc and ac fanouts and eliminate the need to tie unused inputs to an external supply. The open emitter outputs allow maximum flexibility in the selection of termination techniques and minimize the power requirements when driving transmission lines. Open emitter outputs also allow wire-ORing capability, which is very useful in control, bussing, and communications in high speed central processors, high speed peripherals, digital communication systems, minicomputers and instrumentation.

POSITIVE LOGIC

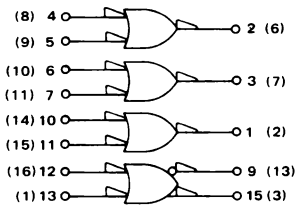


Numbers at ends of terminals denote pin numbers for L package (Case 620).

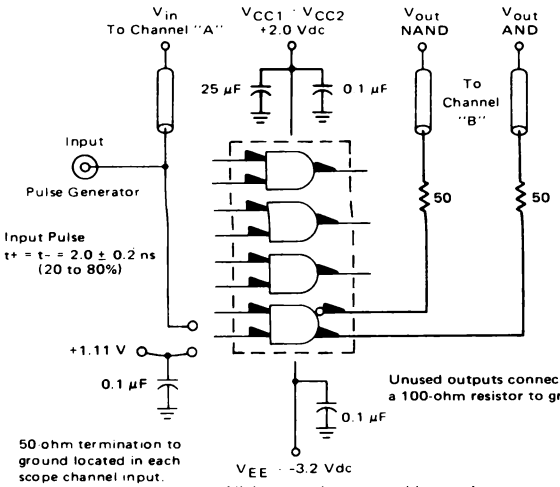
Numbers in parenthesis denote pin numbers for F package (Case 650).

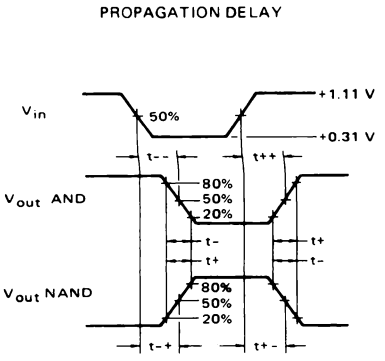
CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

NEGATIVE LOGIC



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



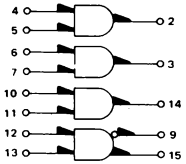


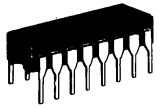
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.
V_{out} is 2:1 attenuated.

See General Information Section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

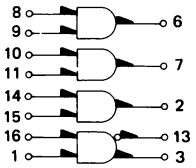
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

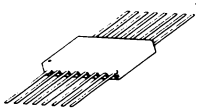
Characteristic	Symbol	Pin Under Test	MC10504L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	39	–	28	35	–	39	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	13	–	450	–	–	265	–	265	µAdc	13	–	–	–	8	1,16
		12	–	375	–	–	220	–	220	µAdc	12,13	–	–	–	8	1,16
	I_{inL}	12	0.5	–	0.5	–	–	0.3	–	µAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	9	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	–	–	–	–	8	1,16
		9	↓	↓	↓	–	↓	↓	↓	↓	12	–	–	–	↓	↓
		9				–					13	–	–	–		
		15				–					12,13	–	–	–		
Logic "0" Output Voltage	V_{OL}	9	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	12,13	–	–	–	8	1,16
		15	↓	↓	↓	–	↓	↓	↓	↓	–	–	–	–	↓	↓
		15				–					13	–	–	–		
		15				–					12	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	9	-1.100	–	-0.950	–	–	-0.845	–	Vdc	12	–	–	13	8	1,16
		9	↓	–	↓	–	–	↓	–	↓	13	–	–	12	↓	↓
		15		–		–	–		–		12	–	13	–		
		15		–		–	–		–		13	–	12	–		
Logic "0" Threshold Voltage	V_{OLA}	9	–	-1.635	–	–	-1.600	–	-1.525	Vdc	12	–	13	–	8	1,16
		9	–	↓	–	–	↓	–	↓	↓	13	–	12	–	↓	↓
		15	–		–	–		–			12	–	–	13		
		15	–		–	–		–			13	–	–	12		
Switching Times* (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{12+9-}	9	–	–	1.0	2.2	4.0	–	–	ns	13	–	12	9	8	1,16
	t_{12-9+}	9	–	–	↓	↓	↓	–	–	↓	↓	–	↓	9	↓	↓
	t_{12+15+}	15	–	–				–	–			–		15		
	t_{12-15-}	15	–	–				–	–		↓	–	↓	15		
	t_{13+9+}	9	–	–		2.7		–	–		12	–	13	9		
	t_{13+15-}	15	–	–	↓	2.7	↓	–	–	↓	↓	–	↓	15	↓	↓
Rise Time (20% to 80%)	t_{9+}	9	–	–	1.5	2.0	3.5	–	–			–		9		
	t_{15+}	15	–	–	↓	↓	↓	–	–			–		15		
Fall Time (20% to 80%)	t_{9-}	9	–	–				–	–			–		9		
	t_{15-}	15	–	–	↓	↓	↓	–	–	↓	↓	–	↓	15	↓	↓

*Inputs 4, 7, 10, and 13 will behave similarly for ac and I_{inH} values.
Inputs 5, 6, 11, and 12 will behave similarly for ac and I_{inH} values.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10504F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	-	39	–	28	35	–	39	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	1	–	450	–	-	265	–	265	µAdc	1	–	–	–	12	4,5
		16	–	375	–	–	220	–	220	µAdc	1,16	–	–	–	12	4,5
	I_{inL}	16	0.5	–	0.5	-	–	0.3	–	µAdc	–	16	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	1,16	–	–	–	12	4,5
		13	↓	↓	↓	–	↓	↓	↓	↓	–	–	–	–	↓	↓
		13				–					1	–	–	–		
		13				–					16	–	–	–		
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	12	4,5
		3	↓	↓	↓	–	↓	↓	↓	↓	1	–	–	–	↓	↓
		3				–					16	–	–	–		
		13				–					1,16	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	1	–	16	–	12	4,5
		3	↓	–	↓	–	–	↓	–	↓	16	–	1	–	↓	↓
		13				–	–		–		1	–	–	16		
		13		–		–	–		–		16	–	–	1		
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	16	–	–	1	12	4,5
		3	–	↓	–	–	↓	–	↓	↓	1	–	–	16	↓	↓
		13	–		–	–		–			16	–	1	–		
		13	–		–	–		–			1	–	16	–		
Switching Times* (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{16+3+}	3	–	–	1.0	2.2	4.0	–	–	ns	1	–	16	3	12	4,5
	t_{16-3-}	3	–	–				–	–			–		3		
	t_{16+13-}	13	–	–		↓		–	–		↓	–	↓	13		
	t_{16-13+}	13	–	–				–	–			–		13		
	t_{1+3-}	3	–	–		2.7		–	–		16	–	1	3		
	t_{1+13+}	13	–	–	↓	2.7	↓	–	–	↓	↓	–	↓	13	↓	↓
Rise Time (20% to 80%)	t_{3+}	3	–	–	1.5	2.0	3.5	–	–			–		3		
	t_{13+}	13	–	–	↓	↓	↓	–	–			–		13		
Fall Time (20% to 80%)	t_{3-}	3	–	–				–	–			–		3		
	t_{13-}	13	–	–	↓	↓	↓	–	–	↓	↓	–	↓	13	↓	↓

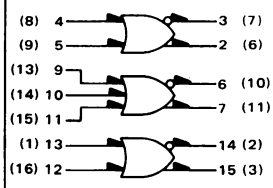
*Inputs 1, 8, 11 and 14 will behave similarly for ac and I_{inH} values.
Inputs 9, 10, 15 and 16 will behave similarly for ac and I_{inH} values.

TRIPLE 2-3-2 INPUT
OR/NOR GATE

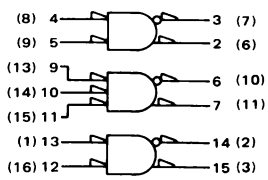
MC10505

The MC10505 is a triple 2-3-2 input gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

POSITIVE LOGIC



NEGATIVE LOGIC

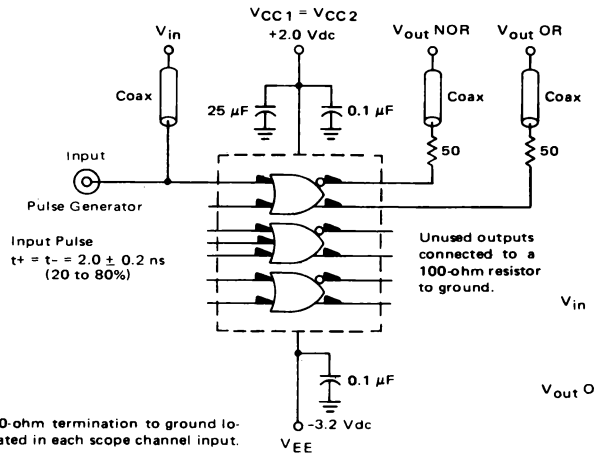


Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

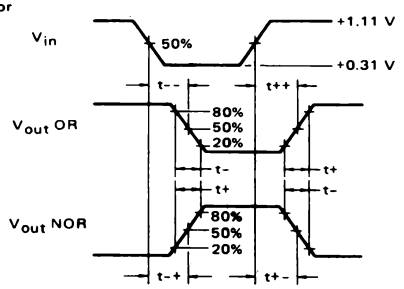
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

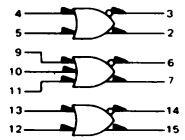
PROPAGATION DELAY

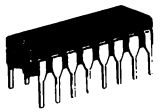


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





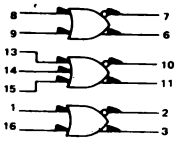
L SUFFIX
CERAMIC PACKAGE
CASE 620

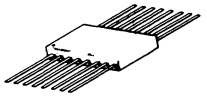
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10505L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	24	–	17	21	–	24	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	450	–	–	265	–	265	µAdc	4	–	–	–	8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	–	–	–	–	8	1,16
		2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	4	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	4	–	–	–	8	1,16
		2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	–	4	8	1,16
		2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	4	–	8	1,16
		2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	4	8	1,16
Switching Times (100-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.0	3.7	1.0	2.0	2.9	1.0	3.7	ns	–	–	4	3	8	1,16
	t_{4-3+}	3									–	–		3		
	t_{4+2+}	2									–	–		2		
	t_{4-2-}	2									–	–		2		
Rise Time	t_{3+}	3		4.0	1.1		3.3		4.0		–	–		3		
(20 to 80%)	t_{2+}	2									–	–		2		
Fall Time	t_{3-}	3									–	–		3		
(20 to 80%)	t_{2-}	2									–	–		2		

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

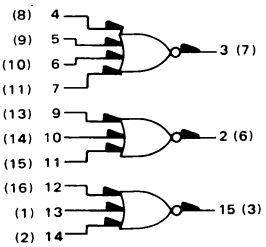
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10505F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	24	–	17	21	–	24	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	8	–	450	–	–	265	–	265	µAdc	8	–	–	–	12	4,5
	I_{inL}	8	0.5	–	0.5	–	–	0.3	–	µAdc	–	8	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	7	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	–	–	–	–	12	4,5
		6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	8	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	8	–	–	–	12	4,5
		6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	7	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	–	8	12	4,5
		6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	8	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	8	–	12	4,5
		6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	8	12	4,5
Switching Times (100-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{8+7-}	7	–	–	1.0	2.0	2.9	–	–	ns	–	–	8	7	12	4,5
	t_{8-7+}	7	–	–	↓	↓	↓	–	–	↓	–	–	↓	7	↓	↓
	t_{8+6+}	6	–	–				–	–		–	–		6		
	t_{8-6-}	6	–	–				–	–		–	–		6		
Rise Time (20 to 80%)	t_{7+}	7	–	–	1.1		3.3	–	–		–	–		7		
	t_{6+}	6	–	–	↓		↓	–	–		–	–		6		
Fall Time (20 to 80%)	t_{7-}	7	–	–	↓	↓	↓	–	–	↓	–	–	↓	7	↓	↓
	t_{6-}	6	–	–	↓	↓	↓	–	–	↓	–	–	↓	6	↓	↓

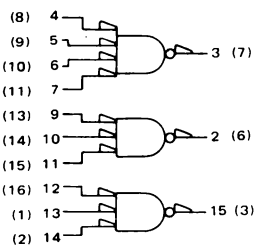
MC10506

The MC10506 is a triple 4-3-3 input NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

POSITIVE LOGIC



NEGATIVE LOGIC



Numbers at ends of terminals denote pin numbers for L package (Case 620).

Numbers in parenthesis denote pin numbers for F package (Case 650).

CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

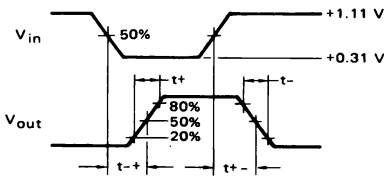
P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

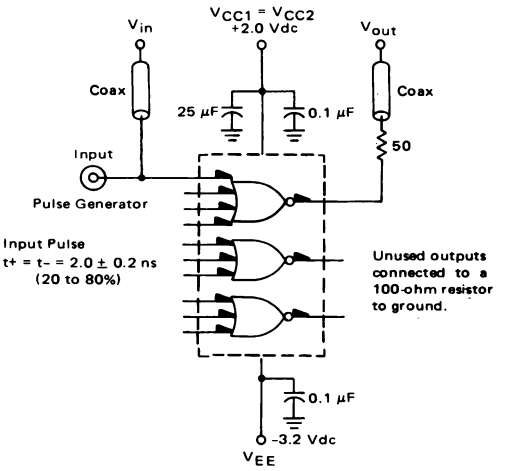
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

PROPAGATION DELAY

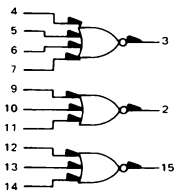


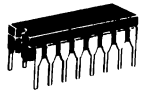


See General Information section for packaging.

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





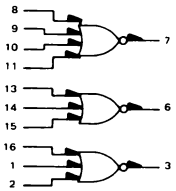
L SUFFIX
CERAMIC PACKAGE
CASE 620

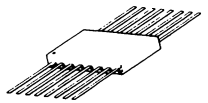
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10506L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	24	–	17	21	–	24	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	450	–	–	265	–	265	µAdc	4		–	–	8	1,16
	I_{inL}	4	0.5		0.5	–		0.3		µAdc		4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc		–	–	–	8	1,16
		2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	4		–		8	1,16
		2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.100	–	-0.950	–		-0.845		Vdc			–	4	8	1,16
		2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	–	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–		-1.600	–	-1.525	Vdc			4		8	1,16
		2	–	-1.635	–	–	-1.600	–	-1.525	Vdc		–	9	–	8	1,16
Switching Times (100-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.0	3.7	1.0	2.0	2.9	1.0	3.7	ns			4	3	8	1,16
	t_{4-3+}			3.7	1.0		2.9		3.7		–	–				
Rise Time (20 to 80%)	t_{3+}			4.0	1.1		3.3		4.0							
Fall Time (20 to 80%)	t_{3-}			4.0	1.1		3.3		4.0			–				

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





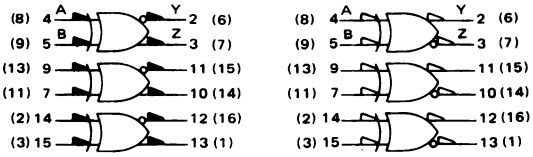
F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.830	-1.920	-1.255	-1.510	-5.2
+25°C	-0.720	-1.850	-1.105	-1.475	-5.2
+125°C	-0.580	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10506F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	24	–	17	21	–	24	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	8	–	450	–	–	265	–	265	µAdc	8	–	–	–	12	4,5
	I_{inL}	8	0.5	–	0.5	–	–	0.3	–	µAdc	–	8	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	7	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	–	–	–	–	12	4,5
		6	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	–	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	8	–	–	–	12	4,5
		6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	13	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	7	-1.100	–	-0.950	–	–	-0.845	–	Vdc			–	8	12	4,5
		6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	–	13	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	8	–	12	4,5
		6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	13	–	12	4,5
Switching Times (100-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{g+7-}	7	–	–	1.0	2.0	2.9	–	–	ns	–		8	7	12	4,5
	t_{g-7+}	↓	–	–	1.0	↓	2.9	–	–	↓	–	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_{7+}	↓	–	–	1.1	↓	3.3	–	–	↓	–	–	↓	↓	↓	↓
Fall Time (20 to 80%)	t_{7-}	↓	–	–	1.1	↓	3.3	–	–	↓			↓	↓	↓	↓

TRIPLE 2-INPUT EXCLUSIVE "OR"/EXCLUSIVE "NOR"

MC10507



$Z = (A \bullet \overline{B}) + (\overline{A} \bullet B)$
$Y = (\overline{A} \bullet \overline{B}) + (A \bullet B)$

$Z = (\overline{A} \bullet \overline{B}) + (A \bullet B)$
$Y = (A \bullet \overline{B}) + (\overline{A} \bullet B)$

Numbers at ends of terminals denote pin numbers for L package (Case 620).

Numbers in parenthesis denote pin numbers for F package (Case 650).

CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

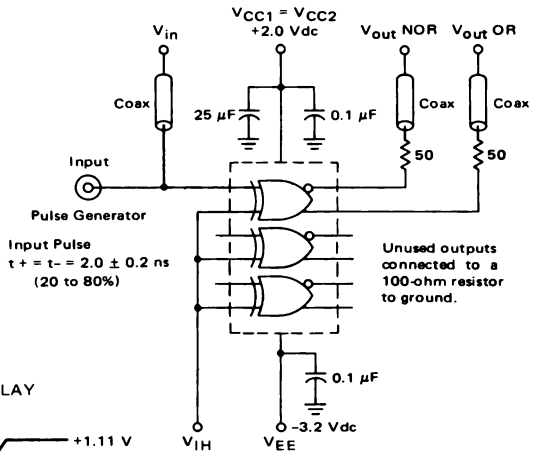
The MC10507 provides three positive logic Exclusive OR and Exclusive NOR functions for high speed applications. Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

P_D = 40 mW typ/gate (No Load)
t_{pd} = 2.5 ns typ
Output Rise and Fall Times
= 2.0 ns typ (20% to 80%)
= 3.5 ns typ (10% to 90%)

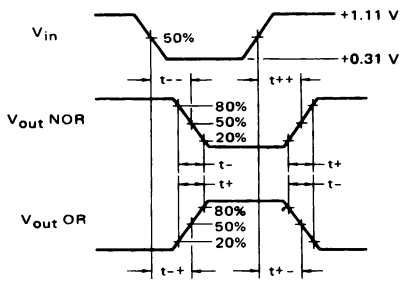
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.



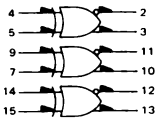
PROPAGATION DELAY

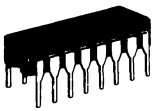


See General Information section for packaging.

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

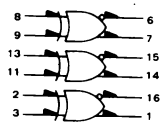
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

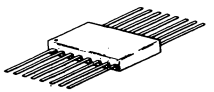
Characteristic	Symbol	Pin Under Test	MC10507L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	31	–	28	–	31	mAdc	All Inputs	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4,9,14	–	450	–	265	–	265	μAdc	*	–	–	–	8	1,16
		5,7,15	–	375	–	220	–	220	μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	0.5	–	0.5	–	0.3	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	-0.780	-0.825	-0.630	Vdc	4,5	–	–	–	8	1,16
		2	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	↓	↓
		3								4	–	–	–		
		3								5	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	-1.620	-1.820	-1.545	Vdc	4	–	–	–	8	1,16
		2	↓	↓	↓	↓	↓	↓	↓	5	–	–	–	↓	↓
		3								4,5	–	–	–		
		3								–	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	-0.845	–	Vdc	5	–	–	4	8	1,16
		2	↓	–	↓	–	↓	–	↓	–	–	–	–	↓	↓
		3		–		–		–		–	–	–	4		
		3		–		–		–		–	–	5	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	-1.600	–	-1.525	Vdc	–	–	4	–	8	1,16
		2	–	↓	–	↓	–	↓	↓	–	–	5	–	↓	↓
		3	–		–		–			5	–	4	–		
		3	–		–		–			–	–	–	4		
Switching Times (100 Ω load)					Min	Typ	Max		Unit	+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t++	Inputs	1.0	4.5	1.1	2.0	3.7	1.0	4.5	ns	5,7,15	–	Input	Corresponding	8	1,16
	t+-	4, 9 or 14										–	4, 9, or	Ex-OR/Ex-NOR		
	t-+	to either										–	14	Outputs		
	t--	Output				↓					↓	–				
	t++	Inputs				2.8					4,9,14	–	Input	Corresponding		
	t+-	5,7, or 15										–	5, 7, or	Ex-OR/Ex-NOR		
	t-+	to either										–	15	Outputs		
	t--	Output										–				
Rise Time (20 to 80%)	t+	**		4.3		2.5	3.5		4.3			–	Any Input	Corresponding Ex-OR/Ex-NOR Outputs		
Fall Time (20 to 80%)	t-	**		4.3		2.5	3.5		4.3			–	Any Input			

*Individually test each input applying V_{IH} or V_{IL} to input under test.
**Any Output

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

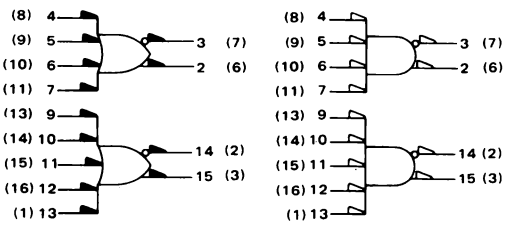
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10507F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	-	31	-	28		31	mAdc	All Inputs	-	-	-	12	4,5
Input Current	$I_{in\ H}$	2,8,13	-	450	-	265	-	265	µAdc	*	-	-	-	12	4,5
		3,9,11	-	375	-	220		220	µAdc	*	-	-	-	12	4,5
	$I_{in\ L}$	*	0.5	-	0.5	-	0.3	-	µAdc	-	*	-	-	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	-0.780	-0.825	-0.630	Vdc	8,9	-	-	-	12	4,5
		6	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
		7								8	-	-	-		
		7								9	-	-	-		
Logic "0" Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	-1.620	-1.820	-1.545	Vdc	8	-	-	-	12	4,5
		6	↓	↓	↓	↓	↓	↓	↓	9	-	-	-	↓	↓
		7								8,9	-	-	-		
		7								-	-	-	-		
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	-	-0.950	-	-0.845	-	Vdc	9	-	8	-	12	4,5
		6	↓	-	↓	-	↓	-	↓	-	-	-	8	↓	↓
		7		-		-		-		-	-	8	-		
		7		-		-		-		-	-	9	-		
Logic "0" Threshold Voltage	V_{OLA}	6	-	-1.635	-	-1.600		-1.525	Vdc	-	-	8	-	12	4,5
		6	-	↓	-	↓		↓	↓	-	-	9	-	↓	↓
		7	-		-		-			-	-	8	-		
		7	-		-		-			-	-	-	8		
Switching Times (100 Ω load)					Min	Typ	Max		Unit	+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t++	Inputs	-	-	1.1	2.0	3.7	-	ns	3,9,11	-	Input 2,8 or 13	Corresponding Ex-OR/Ex-NOR Outputs	12	4,5
	t+-	2,8 or 13	-	-		↓	↓	-		↓	-			↓	↓
	t-+	to either	-	-				-			-				
	t--	Output	-	-				-			-				
	t++	Inputs	-	-		2.8		-		2,8,13	-	Input 3,9 or 11	Corresponding Ex-OR/Ex-NOR Outputs		
	t+-	3,9 or 11	-	-				-			-				
	t-+	to either	-	-				-			-				
	t--	Output	-	-		↓	↓	-		↓	-				
Rise Time (20 to 80%)	t+	**	-	-		2.5	3.5	-				Any Input	Corresponding Ex-OR/Ex-NOR Outputs		
Fall Time (20 to 80%)	t-	**	-	-	↓	2.5	3.5	-	↓	↓	-	Any Input	↓	↓	↓

*Individually test each input applying V_{IH} or V_{IL} to input under test.
**Any Output

DUAL 4-5-INPUT
"OR/NOR" GATE

MC10509



Numbers at ends of terminals denote pin numbers for L package (Case 620).

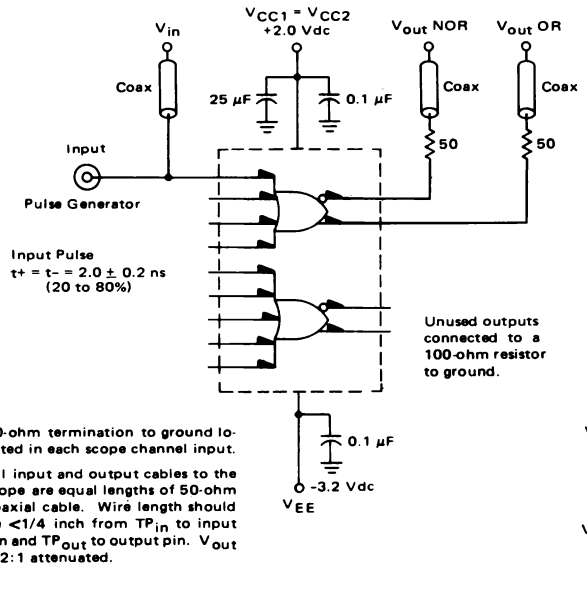
Numbers in parenthesis denote pin numbers for F package (Case 650).

CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

The MC10509 is a dual 4-5 input OR-NOR gate which is pin compatible with the MECL III MC1660L dual OR-NOR gate. All inputs are terminated by a 50 k ohm resistor to V_{EE} eliminating the need to tie unused inputs low.

t_{pd} = 2.0 ns typ
P_D = 30 mW typ/gate (No Load)
Output Rise and Fall Times
(10% to 90%) 3.5 ns
(20% to 80%) 2.0 ns

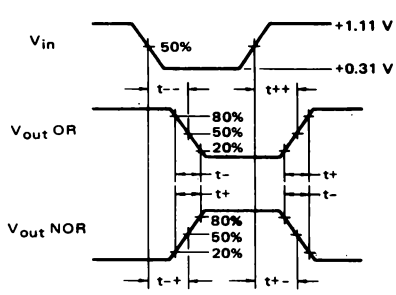
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

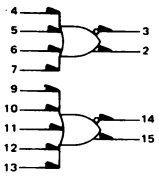
PROPAGATION DELAY

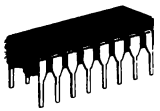


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





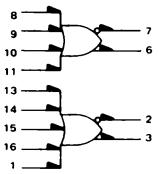
L SUFFIX
CERAMIC PACKAGE
CASE 620

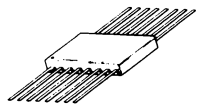
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10509L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	16	–	11	14	–	16	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	450	–	–	265	–	265	µAdc	4	–	–	–	8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3		µAdc	–	4	–	–	8	1,16
High Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	4	–	–	–	8	1,16
		3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	–	–	–	–	8	1,16
Low Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	8	1,16
		3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	4	–	–	–	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	4	–	8	1,16
		3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	–	4	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	4	8	1,16
		3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	4	–	8	1,16
Switching Times (100 ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.7	1.0	2.0	2.9	1.0	3.7	ns	–	–	4	2	8	1,16
	t_{4-2-}	2									–	–		2		
	t_{4+3-}	3									–	–		3		
	t_{4-3+}	3									–	–		3		
Rise Time (20 to 80%)	t_{2+}	2		4.0	1.1		3.3		4.0		–	–		2		
	t_{3+}	3									–	–		3		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





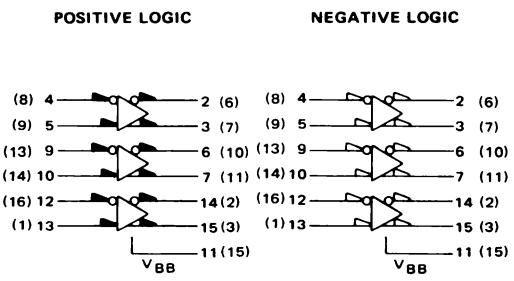
F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.830	-1.920	-1.255	-1.510	-5.2
+25°C	-0.720	-1.850	-1.105	-1.475	-5.2
+125°C	-0.580	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10509F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	16	–	11	14	–	16	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	8	–	450	–	–	265	–	265	µAdc	8	–	–	–	12	4,5
	I_{inL}	8	0.5	–	0.5	–	–	0.3	–	µAdc	–	8	–	–	12	4,5
High Output Voltage	V_{OH}	6	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	8	–	–	–	12	4,5
		7	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	–	–	–	–	12	4,5
Low Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	12	4,5
		7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	8	–	–	–	12	4,5
High Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	8	–	12	4,5
		7	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	–	8	12	4,5
Low Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	8	12	4,5
		7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	8	–	12	4,5
Switching Times (100 ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{9+6+}	6	–	–	1.0	2.0	2.9	–	–	ns	–	–	8	6	12	4,5
	t_{9-6-}	6	–	–	↓	↓	↓	–	–	↓	–	–	↓	6	↓	↓
	t_{9+7-}	7	–	–				–	–		–	–		7		
	t_{9-7+}	7	–	–				–	–		–	–		7		
Rise Time (20 to 80%)	t_{6+}	6	–	–	1.1		3.3	–	–		–	–		6		
	t_{7+}	7	–	–	↓		↓	–	–		–	–		7		
Fall Time (20 to 80%)	t_{6-}	6	–	–				–	–		–	–	↓	6	↓	↓
	t_{7-}	7	–	–				–	–		–	–		7		

TRIPLE LINE RECEIVER
(HIGH COMMON MODE)

MC10514



CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

The MC10514 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

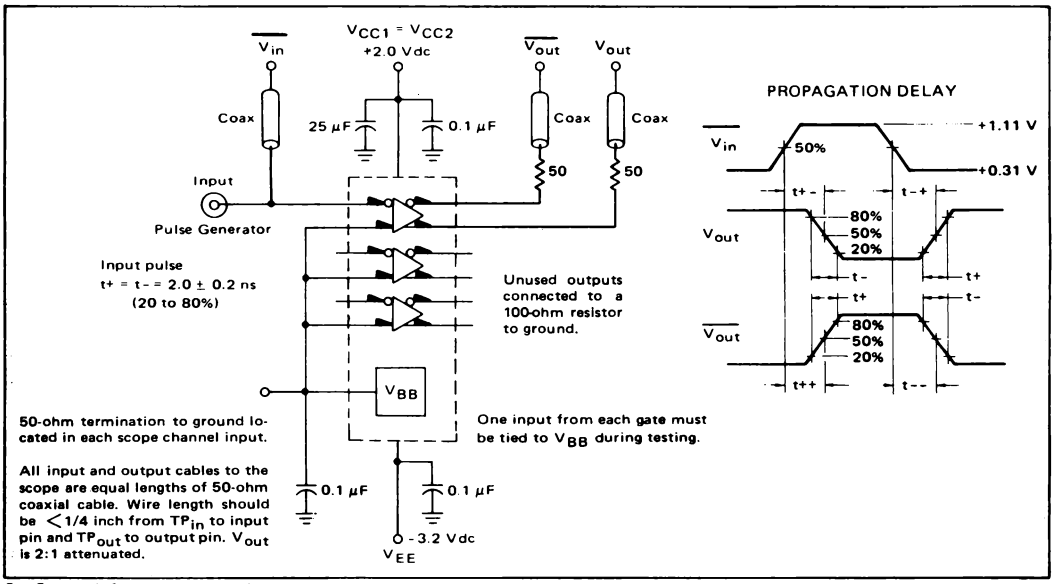
Another feature of the MC10514 is that the OR outputs go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 100-ohm transmission lines.

This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumentation systems. The MC10514 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A V_{BB} reference is provided which is useful in making the MC10514 a Schmitt trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary.

t_{pd} = 2.4 ns typ (Single Ended Input)
t_{pd} = 2.0 ns typ (Differential Input)
P_D = 145 mW typ/pkg (No Load)

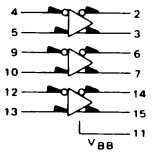
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.



L SUFFIX
CERAMIC PACKAGE
CASE 620

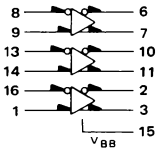
@ Test Temperature	TEST VOLTAGE VALUES (Volts)									
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	From	+0.170	-0.920	-1.830	-2.920	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	Pin	+0.280	-0.850	-1.720	-2.850	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	11	+0.420	-0.820	-1.580	-2.820	-5.2

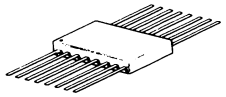
Characteristic	Symbol	Pin Under Test	MC10514L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	39	–	28	35	–	39	mAdc	–	4,9,12	–	–	5,10,13	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	80	–	–	45	–	45	μAdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
	I_{CBO}	4	–	1.5		–	1.0	–	1.0	μAdc	–	9,12	–	–	5,10,13	–	–	–	–	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
		3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	9,12	4	–	–	5,10,13	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	9,12	4	–	–	5,10,13	–	–	–	–	8	1,16
		3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	9,12	4	–	5,10,13	–	–	–	–	8	1,16
		3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	9,12	–	–	4	5,10,13	–	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	9,12	–	–	4	5,10,13	–	–	–	–	8	1,16
		3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	9,12	4	–	5,10,13	–	–	–	–	8	1,16
Reference Voltage	V_{BB}	11	-1.440	-1.320	-1.350	–	-1.230	-1.240	-1.120	Vdc	–	–	–	–	5,10,13	–	–	–	–	8	1,16
Common Mode Rejection Test	V_{OH}	2	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	–	–	–	–	–	4	5	–	–	8	1,16
		3	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	–	–	–	–	–	–	–	5	4	8	1,16
	V_{OL}	2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	–	–	–	5	4	8	1,16
		3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	–	4	5	–	–	8	1,16
Switching Times (100-ohm Load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out						-3.2 V	+2.0 V
Propagation Delay**	t_{4+2+}	2	–	–	1.0	2.5	4.0	–	–	ns	–	–	4	2	5,10,13	–	–	–	–	8	1,16
	t_{4-2-}	2	–	–				–	–		–	–		2		–	–	–	–		
	t_{4+3-}	3	–	–				–	–		–	–		3		–	–	–	–		
	t_{4-3+}	3	–	–				–	–		–	–		3		–	–	–	–		
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.5	2.1	3.5	–	–		–	–		2		–	–	–	–		
	t_{3+}	3	–	–				–			–	–		3		–	–	–	–		
Fall Time (20% to 80%)	t_{2-}	2	–	–				–	–		–	–		2		–	–	–	–		
	t_{3-}	3	–	–				–	–		–	–		3		–	–	–	–		

*V_{IHH} = Input logic "1" level shifted positive one volt for common mode rejection tests.
V_{ILH} = Input logic "0" level shifted positive one volt for common mode rejection tests.
V_{IHL} = Input logic "1" level shifted negative one volt for common mode rejection tests.
V_{ILL} = Input logic "0" level shifted negative one volt for common mode rejection tests.
**Delay is 2.0 ns with differential input.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.



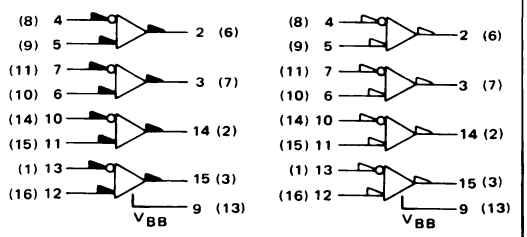


F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	From	+0.170	-0.920	-1.830	-2.920	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	Pin	+0.280	-0.850	-1.720	-2.850	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	15	+0.420	-0.820	-1.580	-2.820	-5.2

Characteristic	Symbol	Pin Under Test	MC10514F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	39	–	28	35	–	39	mAdc	–	8,13,16	–	–	1,9,14	–	–	–	–	12	4,5
Input Current	I_{inH}	8	–	80	–	–	45	–	45	μAdc	8	13,16	–	–	1,9,14	–	–	–	–	12	4,5
	I_{CBO}	8	–	1.5		–	1.0	–	1.0	μAdc	–	13,16	–	–	1,9,14	–	–	–	–	8,12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930		-0.780	-0.825	-0.630	Vdc	8	13,16	–	–	1,9,14	–	–	–	–	12	4,5
		7	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	13,16	8	–	–	1,9,14	–	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	13,16	8	–	–	1,9,14	–	–	–	–	12	
		7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	8	13,16	–	–	1,9,14	–	–	–	–	12	
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	13,16	8	–	1,9,14	–	–	–	–	12	
		7	-1.100	–	-0.950	–	–	-0.845	–	Vdc	13,16	–	–	8	1,9,14	–	–	–	–	12	
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635		–	-1.600	–	-1.525	Vdc	13,16	–	–	8	1,9,14	–	–	–	–	12	
		7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	13,16	8	–	1,9,14	–	–	–	–	12	
Reference Voltage	V_{BB}	15	-1.440	-1.320	-1.350	–	-1.230	-1.240	-1.120	Vdc	–	–	–	–	1,9,14	–	–	–	–	12	
Common Mode Rejection Test	V_{OH}	6	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	–	–	–	–	–	8	9	–	–	12	
		7	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	–	–	–	–	–	–	–	9	8	12	
	V_{OL}	6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	–	–	–	9	8	12	
		7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	–	8	9	–	–	12	
Switching Times (100-ohm Load)			**Min**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Max**				**Pulse In**	**Pulse Out**						**-3.2 V**	**+2.0 V**
Propagation Delay**	t_{8+6+}	6	–	–	1.0	2.5	4.0	–	–	ns		–	8	6	1,9,14	–	–	–	–	12	4.5
	t_{8-6-}	6	–	–				–	–			–		6		–	–	–	–		
	t_{8+7-}	7	–	–				–	–			–		7		–	–	–	–		
	t_{8-7+}	7	–	–				–	–			–		7		–	–	–	–		
Rise Time (20% to 80%)	t_{6+}	6	–	–	1.5	2.1	3.5	–				–		6		–	–	–	–		
	t_{7+}	7	–	–				–				–		7		–	–	–	–		
Fall Time (20% to 80%)	t_{6-}	6	–	–				–			–	–		6		–	–	–	–		
	t_{7-}	7	–	–				–	–		–	–		7		–	–	–	–		

*V_{IHH} = Input logic "1" level shifted positive one volt for common mode rejection tests.
V_{ILH} = Input logic "0" level shifted positive one volt for common mode rejection tests.
V_{IHL} = Input logic "1" level shifted negative one volt for common mode rejection tests.
V_{ILL} = Input logic "0" level shifted negative one volt for common mode rejection tests.
**Delay is 2.0 ns with differential input.



Numbers at ends of terminals denote pin numbers for L package (Case 620).

Numbers in parenthesis denote pin numbers for F package (Case 650).

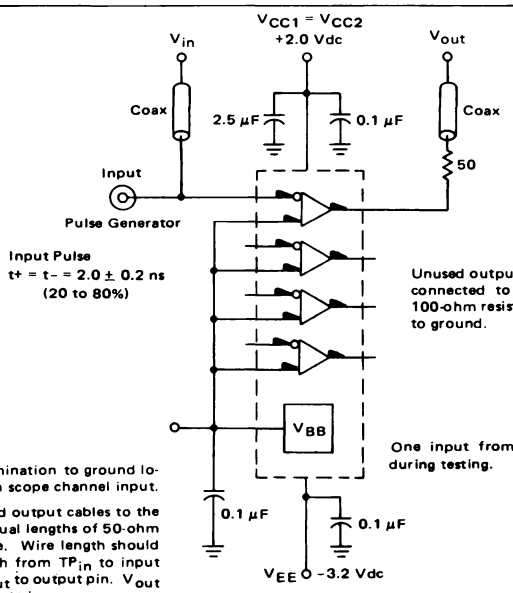
CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

The MC10515 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10515 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent upsetting the current source bias network.

t_{pd} = 2.0 ns typ
P_D = 110 mW typ/pkg (No Load)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input Pulse
$t_+ = t_- = 2.0 \pm 0.2$ ns
(20 to 80%)

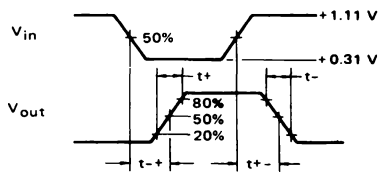
Unused outputs connected to a 100-ohm resistor to ground.

One input from each gate must be tied to V_{BB} during testing.

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

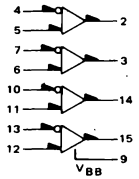
PROPAGATION DELAY

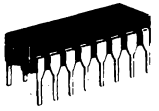


See General Information section for packaging.

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





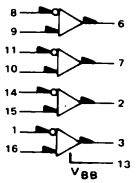
L SUFFIX
CERAMIC PACKAGE
CASE 620

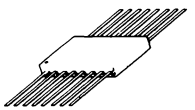
@ Test Temperature	TEST VOLTAGE VALUES					
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	From Pin 9	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475		-5.2
+125°C	-0.630	-1.820	-1.000	-1.400		-5.2

Characteristic	Symbol	Pin Under Test	MC10515L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	26	–	29	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	$I_{in\,H}$	4	–	165	–	95	–	95	μAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
	I_{CBO}	4	–	1.5	–	1.0	–	1.0	μAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	-0.780	-0.825	-0.630	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	-1.620	-1.820	-1.545	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	-0.845	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	-1.600	–	-1.525	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	-1.440	-1.320	-1.350	-1.230	-1.240	-1.120	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (100 ohm load)			Min	Max	Min	Max	Min	Max		Pulse In		Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4-2+}	2	1.0	3.5	1.0	2.9	1.0	4.0	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	↓	3.5	1.0	2.9	↓	4.0	↓	↓		↓		↓	↓	↓
Rise Time (20% to 80%)	t_{2+}	2		3.9	1.1	3.3		4.4								
Fall Time (20% to 80%)	t_{2-}	2		3.9	1.1	3.3		4.4								

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

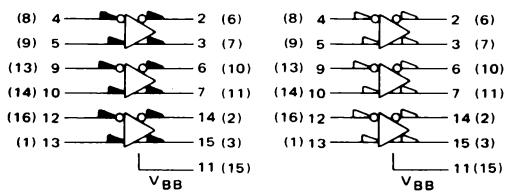




F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	From Pin 13	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475		-5.2
+125°C	-0.630	-1.820	-1.000	-1.400		-5.2

Characteristic	Symbol	Pin Under Test	MC10515F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	29	–	26	–	29	mAdc	–	1,8,11,14	–	–	9,10,15,16	12	4,5
Input Current	$I_{in\ H}$	8	–	165	–	95	–	95	μAdc	8	1,11,14	–	–	9,10,15,16	12	4,5
	I_{CBO}	8	–	1.5	–	1.0	–	1.0	μAdc	–	1,11,14	–	–	9,10,15,16	8,12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	-0.780	-0.825	-0.630	Vdc	1,11,14	8	–	–	9,10,15,16	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	-1.620	-1.820	-1.545	Vdc	8	1,11,14	–	–	9,10,15,16	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	-0.845	–	Vdc	–	1,11,14	–	8	9,10,15,16	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635	–	-1.600	–	-1.525	Vdc	–	1,11,14	8	–	9,10,15,16	12	4,5
Reference Voltage	V_{BB}	13	-1.440	-1.320	-1.350	-1.230	-1.240	-1.120	Vdc	–	–	–	–	9,10,15,16	12	4,5
Switching Times (100 ohm load)			Min	Max	Min	Max	Min	Max		Pulse In		Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{8-6+}	6	–	–	1.0	2.9	–	–	ns	8		6		9,10,15,16	12	4,5
	t_{8-6-}	6	–	–	1.0	2.9	–	–								
Rise Time (20% to 80%)	t_{6+}	6	–	–	1.1	3.3	–	–								
Fall Time (20% to 80%)	t_{6-}	6	–	–	1.1	3.3	–	–								



Numbers at ends of terminals denote pin numbers for L package (Case 620).

Numbers in parenthesis denote pin numbers for F package (Case 650).

CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

The MC10516 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10516 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent upsetting the current source bias network.

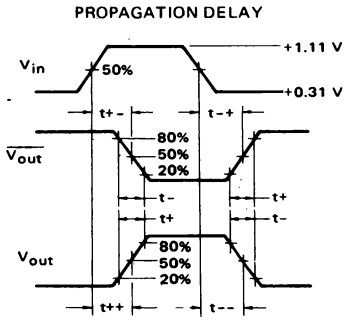
Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

t_{pd} = 2.0 ns typ
P_D = 85 mW typ/pkg (No Load)

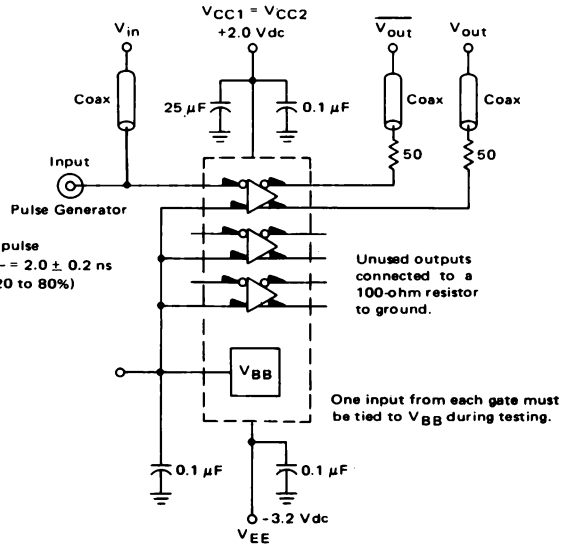
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.



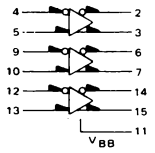
Input pulse
t+ = t- = 2.0 ± 0.2 ns
(20 to 80%)

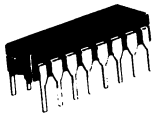


See General Information section for packaging.

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





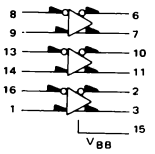
L SUFFIX
CERAMIC PACKAGE
CASE 620

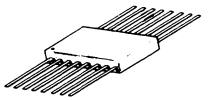
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	From	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	Pin	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	11	-5.2

Characteristic	Symbol	Pin Under Test	MC10516L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	--	24	--	14	21	--	24	mAdc	--	4,9,12	--	--	5,10,13	8	1,16
Input Current	I_{inH}	4	--	165	--	--	95	--	95	µAdc	4	9,12	--	--	5,10,13	8	1,16
	I_{CBO}	4	--	1.5	--	--	1.0	--	1.0	µAdc	--	9,12	--	--	5,10,13	8,4	1,16
High Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	--	-0.780	-0.825	-0.630	Vdc	4	9,12	--	--	5,10,13	8	1,16
		3	-1.080	-0.880	-0.930	--	-0.780	-0.825	-0.630	Vdc	9,12	4	--	--	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	--	-1.620	-1.820	-1.545	Vdc	9,12	4	--	--	5,10,13	8	1,16
		3	-1.920	-1.655	-1.850	--	-1.620	-1.820	-1.545	Vdc	4	9,12	--	--	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.100	--	-0.950	--	--	-0.845	--	Vdc	--	9,12	4	--	5,10,13	8	1,16
		3	-1.100	--	-0.950	--	--	-0.845	--	Vdc	9,12	--	--	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	--	-1.635	--	--	-1.600	--	-1.525	Vdc	--	9,12	--	4	5,10,13	8	1,16
		3	--	-1.635	--	--	-1.600	--	-1.525	Vdc	9,12	--	4	--	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	-1.440	-1.320	-1.350	--	-1.230	-1.240	-1.120	Vdc	--	--	--	--	5,10,13	8	1,16
Switching Times (100-ohm load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out		-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.5	1.0	2.0	2.9	1.0	4.0	ns	--	--	4	2	5,10,13	8	1,16
	t_{4-2-}	2									--	--		2			
	t_{4+3-}	3									--	--		3			
	t_{4-3+}	3									--	--		3			
Rise Time (20% to 80%)	t_{2+}	2		3.9	1.1		3.3		4.4		--	--		2			
	t_{3+}	3									--	--		3			
Fall Time (20% to 80%)	t_{2-}	2									--	--		2			
	t_{3-}	3									--	--		3			

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	From	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	Pin	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	15	-5.2

Characteristic	Symbol	Pin Under Test	MC10516F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12		24		17	21		24	mAdc		8,13,16	–	–	1,9,14	12	4,5
Input Current	I_{inH}	8		165			95		95	μAdc	8	13,16	–	–	1,9,14	12	4,5
	I_{CBO}	8		1.5	–	–	1.0		1.0	μAdc	–	13,16	–	–	1,9,14	8,12	4,5
High Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930		-0.780	-0.825	-0.630	Vdc	8	13,16	–	–	1,9,14	12	4,5
		7	-1.080	-0.880	-0.930		-0.780	-0.825	-0.630	Vdc	13,16	8	–	–	1,9,14	12	4,5
Low Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850		-1.620	-1.820	-1.545	Vdc	13,16	8	–	–	1,9,14	12	4,5
		7	-1.920	-1.655	-1.850		-1.620	-1.820	-1.545	Vdc	9	13,16	–	–	1,9,14	12	4,5
High Threshold Voltage	V_{OHA}	6	-1.100		-0.950			-0.845		Vdc		13,16	8	–	1,9,14	12	4,5
		7	-1.100	–	-0.950	–	–	-0.845		Vdc	13,16	–	–	8	1,9,14	12	4,5
Low Threshold Voltage	V_{OLA}	6		-1.635			-1.600		-1.525	Vdc	–	13,16	–	8	1,9,14	12	4,5
		7	–	-1.635	–		-1.600		-1.525	Vdc	13,16	–	8	–	1,9,14	12	4,5
Reference Voltage	V_{BB}	15	-1.440	-1.320	-1.350	–	-1.230	-1.240	-1.120	Vdc	–	–	–	–	1,9,14	12	4,5
Switching Times (100-ohm load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out		-3.2 V	+2.0 V
Propagation Delay	t_{8+6+}	6	–	–	1.0	2.0	2.9	–	–	ns			8	6	1,9,14	12	4,5
	t_{8-6-}	6	–	–				–	–					6			
	t_{8+7-}	7	–	–				–	–					7			
	t_{8-7+}	7	–	–				–	–					7			
Rise Time	t_{6+}	6	–	–	1.1		3.3	–	–					6			
(20% to 80%)	t_{7+}	7	–	–				–	–			–		7			
Fall Time	t_{6-}	6	–	–				–	–			–		6			
(20% to 80%)	t_{7-}	7	–	–				–	–		–	–		7			

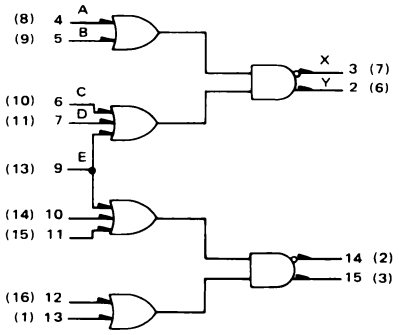
DUAL 2-WIDE 2-3-INPUT "OR-AND/OR-AND-INVERT" GATE

MC10517

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
Output Rise and Fall Times:
= 3.5 ns (10% to 90%)
= 2.2 ns (20% to 80%)

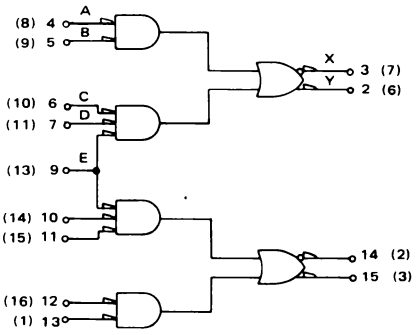
The MC10517 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Input E is common to both gates.

POSITIVE LOGIC



$Y = (A + B) \bullet (C + D + E)$
$X = (A + B) \bullet (C + D + E)$

NEGATIVE LOGIC

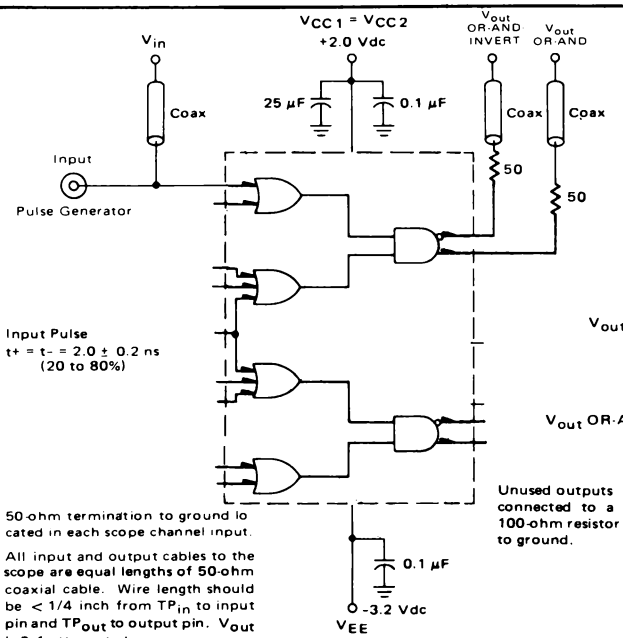


$Y = (A \bullet B) + (C \bullet D \bullet E)$
$X = (A \bullet B) + (C \bullet D \bullet E)$

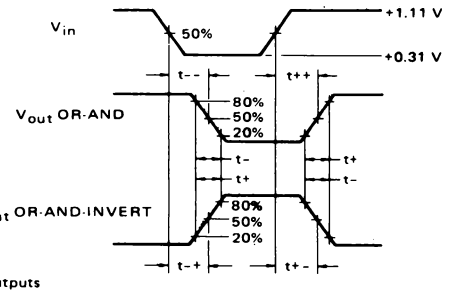
Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



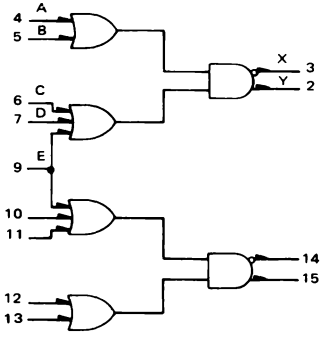
PROPAGATION DELAY

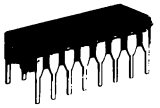


See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





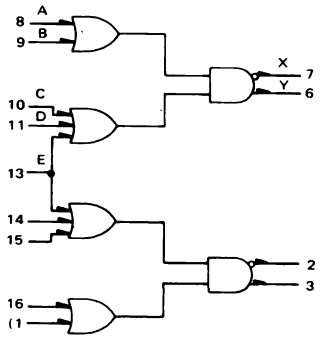
L SUFFIX
CERAMIC PACKAGE
CASE 620

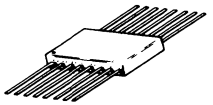
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.830	-1.920	-1.255	-1.510	-5.2
+25°C	-0.720	-1.850	-1.105	-1.475	-5.2
+125°C	-0.580	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10517L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	-	29	–	20	26	–	29	mAdc	-	–	-	-	8	1,16
Input Current	$I_{in\ H}$	4	–	450	–	–	265	–	265	µAdc	4	-	-	-	8	1,16
		9	–	630	–	–	370	–	370	µAdc	9	–	-	-	8	1,16
	$I_{in\ L}$	4	–	–	0.5	–	–	–	–	µAdc	–	4	-	–	8	1,16
		9	–	–	0.5	–	–	–	–	µAdc	–	9	-	-	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	4,9	–	-		8	1,16
		3	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	–	4,9	-	-	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	4,9	-	-	8	1,16
		3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	4,9	–	-	-	8	1 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	4,9	–	8	1,16
		3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	-	-	4,9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	-	-1.600	–	-1.525	Vdc	–	–	–	4,9	8	1,16
		3	–	-1.635	-	-	-1.600	–	-1.525	Vdc	–	–	4,9	–	8	1,16
Switching Times (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.1	3.5	1.4	2.3	3.4	1.2	3.5	ns	9	–	4	2	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓
	t_{4+3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	↓	3	↓	↓
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	↓	3	↓	↓
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.1	1.1	2.2	4.0	0.9	4.1	↓	↓	–	↓	2	↓	↓
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	↓	3	↓	↓
Fall Time (20 to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	↓	2	↓	↓
	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.830	-1.920	-1.255	-1.510	-5.2
+25°C	-0.720	-1.850	-1.105	-1.475	-5.2
+125°C	-0.580	-1.820	-1.000	-1.400	-5.2

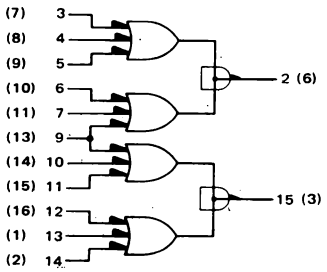
Characteristic	Symbol	Pin Under Test	MC10517F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	29	–	20	26	–	29	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\ H}$	8	–	450	–	–	265	–	265	µAdc	8	–	–	–	12	4,5
		13	–	630	–	–	370	–	370	µAdc	13	–	–	–	12	4,5
	$I_{in\ L}$	8	–	–	0.5	–	–	–	–	µAdc	–	8	–	–	12	4,5
		13	–	–	0.5	–	–	–	–	µAdc	–	13	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	8,13	–	–	–	12	4,5
		7	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	–	8,13	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	8,13	–	–	12	4,5
		7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	8,13	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	8,13	–	12	4,5
		7	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	–	8,13	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	8,13	12	4,5
		7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	8,13	–	12	4,5
Switching Times (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	6	–	–	1.4	2.3	3.4	–	–	ns	13	–	8	6		
	t_{4-2-}	6	–	–	↓	↓	↓	–	–	↓	↓	–	↓	6	↓	↓
	t_{4+3-}	7	–	–	↓	↓	↓	–	–	↓	↓	–	↓	7	↓	↓
	t_{4-3+}	7	–	–	↓	↓	↓	–	–	↓	↓	–	↓	7	↓	↓
Rise Time (20 to 80%)	t_{2+}	6	–	–	1.1	2.2	4.0	–	–	↓	↓	–	↓	6	↓	↓
	t_{3+}	7	–	–	↓	↓	↓	–	–	↓	↓	–	↓	7	↓	↓
Fall Time (20 to 80%)	t_{2-}	6	–	–	↓	↓	↓	–	–	↓	↓	–	↓	6	↓	↓
	t_{3-}	7	–	–	↓	↓	↓	–	–	↓	↓	–	↓	7	↓	↓

MC10518

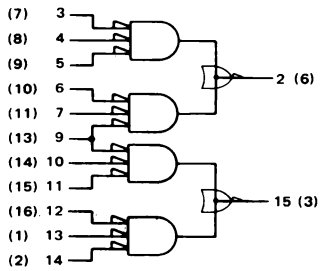
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
Output Rise and Fall Times:
= 3.5 ns (10% to 90%)
= 2.5 ns (20% to 80%)

The MC10518 is a basic logic building block providing the OR-AND function, useful in data control and digital multiplexing applications.

POSITIVE LOGIC



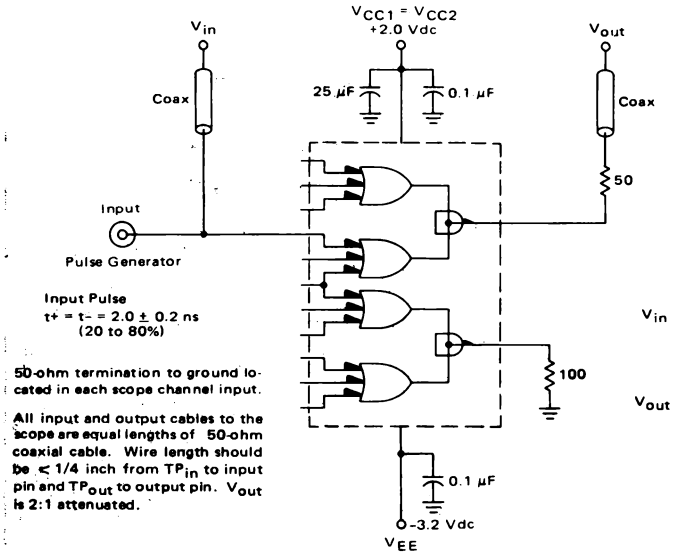
NEGATIVE LOGIC



Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

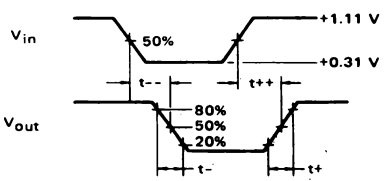


Input Pulse
$t_+ = t_- = 2.0 \pm 0.2$ ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

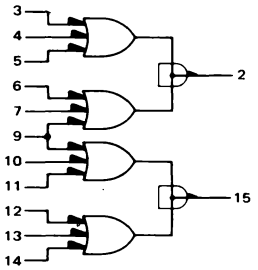
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

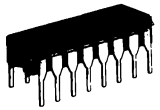
PROPAGATION DELAY



ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





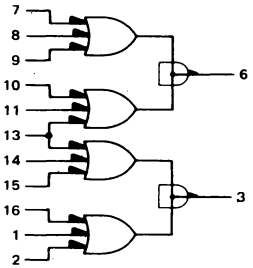
L SUFFIX
CERAMIC PACKAGE
CASE 620

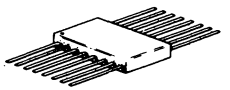
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10518L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	6	–	450	–	–	265	–	265	µAdc	6	–	–	–	8	1,16
		7	–	450	–	–	265	–	265	↓	7	–	–	–	↓	↓
		9	–	630	–	–	370	–	370		9	–	–	–		
	$I_{in\ L}$	6	0.5	–	0.5	–	–	0.3	–	µAdc	–	6	–	–	8	1,16
		7	↓	–	↓	–	–	↓	–	↓	–	7	–	–	↓	↓
		9		–		–	–		–		–	9	–	–		
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	3,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	3,9	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	9	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	9	–	3	8	1,16
Switching Times (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{6+2+}	2	1.1	3.5	1.4	2.3	3.4	1.2	3.9	ns	3	–	6	2	8	1,16
	t_{6-2-}	↓	1.1	3.5	1.4	2.3	3.4	1.2	3.9	↓	↓	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_{2+}		1.3	4.1	1.5	2.5	4.0	1.2	4.0			–				
Fall Time (20 to 80%)	t_{2-}		1.3	4.1	1.5	2.5	4.0	1.2	4.0			–				

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





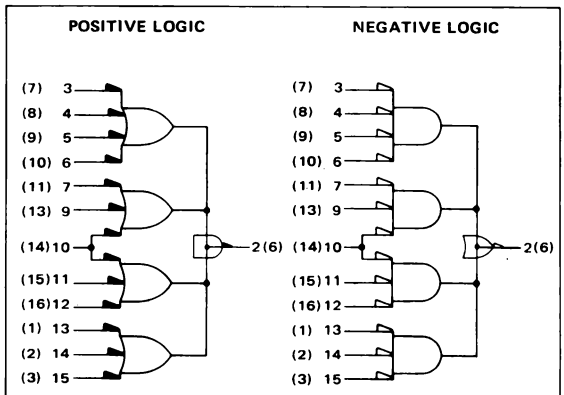
F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.830	-1.920	-1.255	-1.510	-5.2
+25°C	-0.720	-1.850	-1.105	-1.475	-5.2
+125°C	-0.580	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10518F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	29	–	20	26	–	29	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\ H}$	10	–	450	–	–	265	–	265	μAdc	10	–	–	–	12	4,5
		11	–	450	–	–	265	–	265		11	–	–	–		
		13	–	630	–	–	370	–	370		13	–	–	–		
	$I_{in\ L}$	10	0.5	–	0.5	–	–	0.3	–	μAdc	–	10	–	–	12	4,5
		11		–		–	–		–		–	11	–	–		
		13		–		–	–		–		–	13	–	–		
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	7,13	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	7,13	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	13	–	7	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	13	–	7	12	4,5
Switching Times (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{10+6+}	6	–	–	1.4	2.3	3.4	–	–	ns	7	–	10	6	12	4,5
	t_{10-6-}		–	–	1.4	2.3	3.4	–	–			–				
Rise Time (20 to 80%)	t_{6+}		–	–	1.5	2.5	4.0	–	–			–				
Fall Time (20 to 80%)	t_{6-}		–	–	1.5	2.5	4.0	–	–			–				

4-WIDE 4-3-3-3 INPUT
"OR-AND" GATE

MC10519



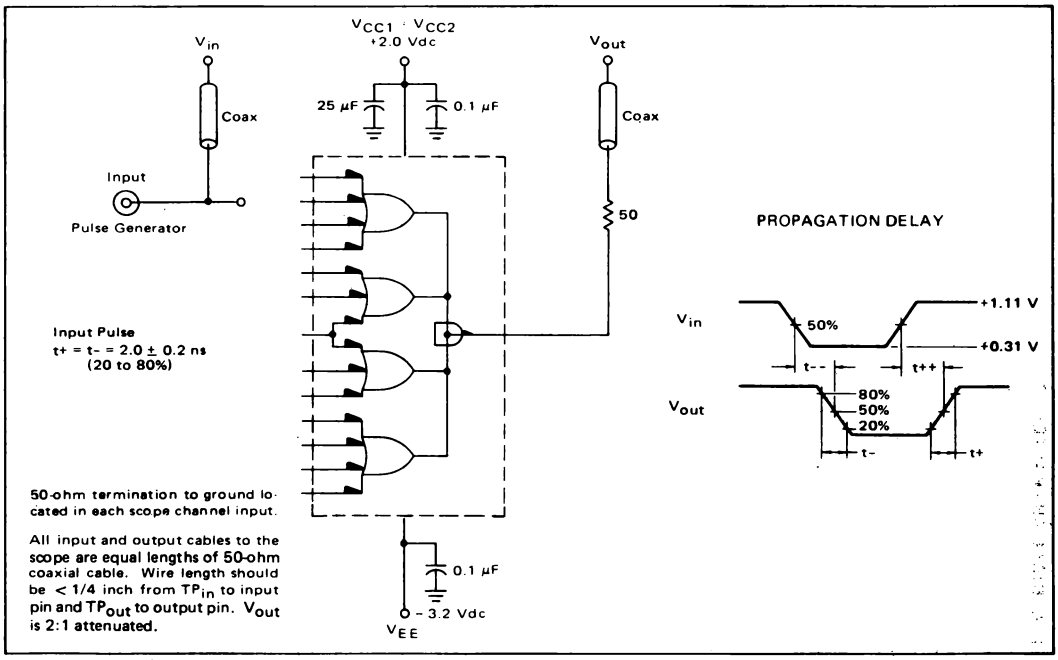
Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

The MC10519 is a 4-Wide 4-3-3-3 Input OR-AND gate with one input for two gates common to pin 10 (14). Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.5 ns typ (20% - 80%)

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

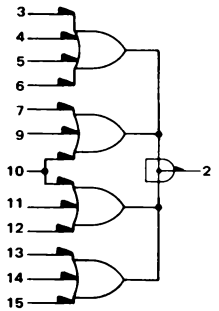
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

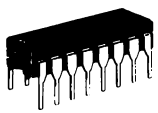


See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





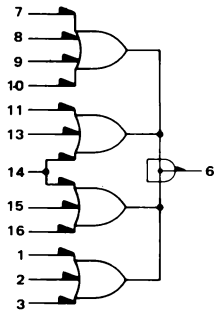
L SUFFIX
CERAMIC PACKAGE
CASE 620

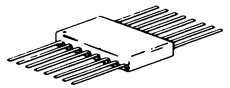
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10519L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc		–	–		8	1,16
Input Current	$I_{in\ H}$	7	–	450	–		265	–	265	μAdc	7	–	–	–	8	1,16
		9	–	450	–	–	265	–	265		9	–	–			
		10	–	630	–	–	370		370		10	–	–	–		
	$I_{in\ L}$	7	0.5	–	0.5	–	–	0.3	–	μAdc		7	–	–	8	1,16
		9		–		–	–		–		–	9	–	–		
		10		–		–	–		–		–	10	–	–		
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	3,10,15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850		-1.620	-1.820	-1.545	Vdc	–	3,10,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	10,15	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	10,15	–	3	8	1,16
Switching Times (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.1	3.5	1.4	2.3	3.4	1.2	3.5	ns	10,13		4	2	8	1,16
	t_{4-2-}		1.1	3.5	1.4	2.3	3.4	1.2	3.5		10,13					
Rise Time (20 to 80%)	t_+		1.3	4.1	1.5	2.5	4.0	1.2	4.3		–					
Fall Time (20 to 80%)	t_-		1.3	4.1	1.5	2.5	4.0	1.2	4.3		–					

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

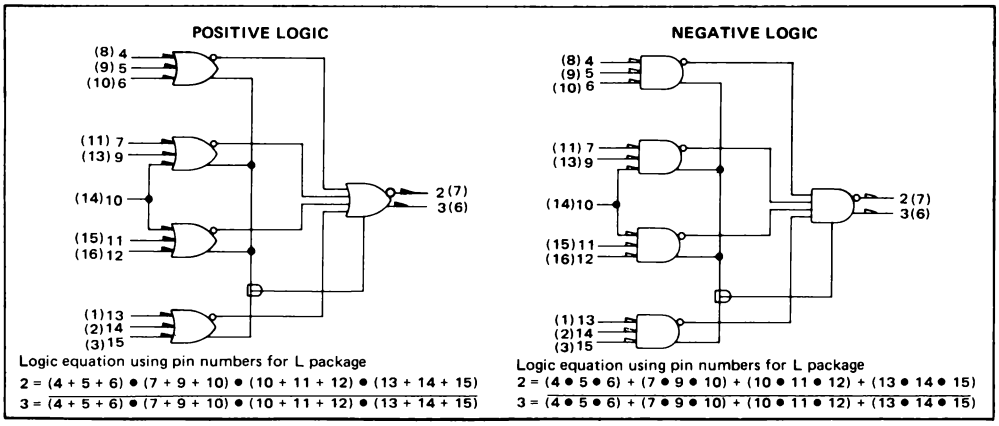
Characteristic	Symbol	Pin Under Test	MC10519F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	11	–	450	–	–	265	–	265	µAdc	11	–	–	–	8	1,16
		13	–	450	–	–	265	–	265	↓	13	–	–	–	↓	↓
		14	–	630	–	–	370	–	370		14	–	–	–		
	$I_{in\ L}$	11	0.5	–	0.5	–	–	0.3	–	µAdc	–	11	–	–	8	1,16
		13	↓	–	↓	–	–	↓	–	↓	–	13	–	–	↓	↓
		14		–		–	–		–		–	14	–	–		
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	3,7,14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	3,7,14	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	3,14	–	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	3,14	–	7	8	1,16
Switching Times (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6+}	6	–	–	1.4	2.3	3.4	–	–	ns	1,14	–	7	6	12	4,5
	t_{7-6-}	↓	–	–	1.4	2.3	3.4	–	–	↓	1,14	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_{6+}		–	–	1.5	2.5	4.0	–	–		–	–				
Fall Time (20 to 80%)	t_{6-}		–	–	1.5	2.5	4.0	–	–		–	–				

4-WIDE
"OR-AND/OR-AND-INVERT"
GATE

MC10521

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
Output Rise and Fall Times:
= 3.5 ns (10% to 90%)
= 2.5 ns (20% to 80%)

The MC10521 is a basic logic building block providing the simultaneous OR-AND/OR-AND-INVERT function, useful in data control and digital multiplexing applications.



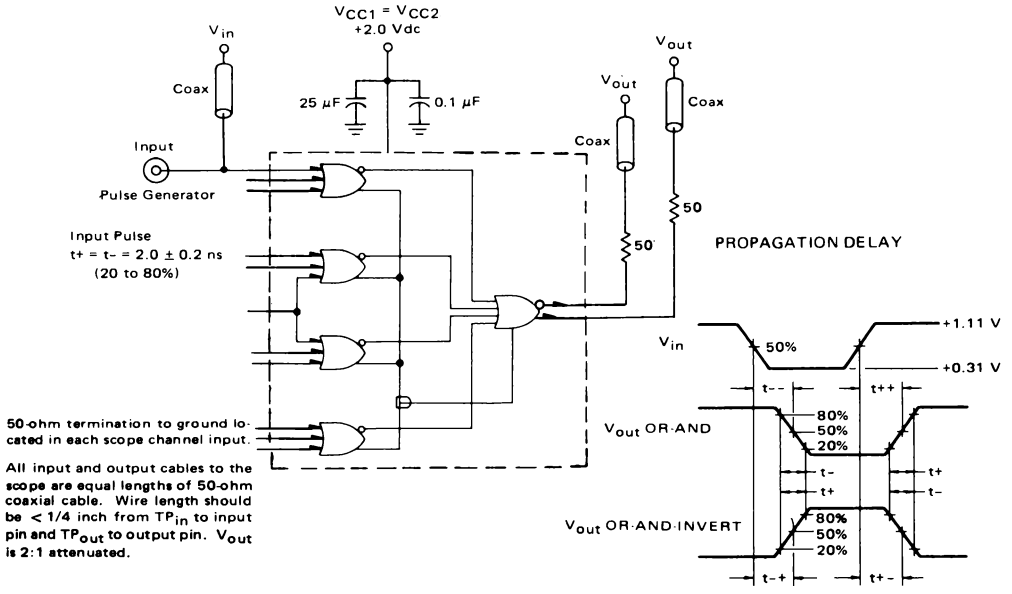
Logic equation using pin numbers for L package
2 = (4 + 5 + 6) • (7 + 9 + 10) • (10 + 11 + 12) • (13 + 14 + 15)
3 = (4 + 5 + 6) • (7 + 9 + 10) • (10 + 11 + 12) • (13 + 14 + 15)

Logic equation using pin numbers for L package
2 = (4 • 5 • 6) + (7 • 9 • 10) + (10 • 11 • 12) + (13 • 14 • 15)
3 = (4 • 5 • 6) + (7 • 9 • 10) + (10 • 11 • 12) + (13 • 14 • 15)

Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



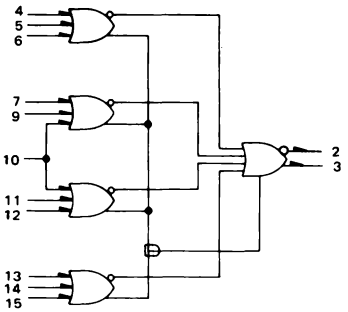
50-ohm termination to ground located in each scope channel input.

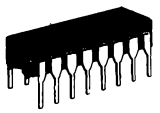
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





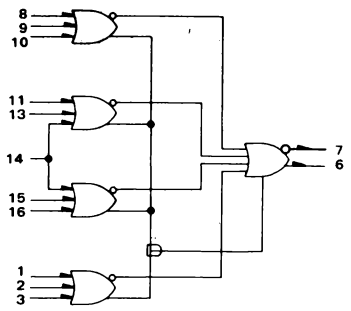
L SUFFIX
CERAMIC PACKAGE
CASE 620

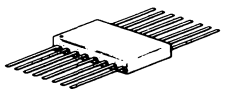
@ Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.830	-1.920	-1.255	-1.510	-5.2
+25°C	-0.720	-1.850	-1.105	-1.475	-5.2
+125°C	-0.580	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10521L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	7	–	450	–	–	265	–	265	μAdc	7	–	–	–	8	1,16
		9	–	450	–	–	265	–	265		9	–	–	–		
		10	–	630	–	–	370	–	370		10	–	–	–		
	$I_{in\ L}$	7	0.5	–	0.5	–	–	0.3	–	μAdc	–	7	–	–	8	1,16
		9		–		–	–		–		–	9	–	–		
		10		–		–	–		–		–	10	–	–		
Logic "1" Output Voltage	V_{OH}	3	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	10,13	4	–	–	8	1,16
		2	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	4,10,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	4,10,13	–	–	–	8	1,16
		2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	10,13	4	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	10,13	–	–	4	8	1,16
		2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	10,13	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	10,13	–	4	–	8	1,16
		2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	10,13	–	–	4	8	1,16
Switching Times (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.2	3.6	1.4	2.3	3.4	1.1	3.5	ns	10,13	–	4	3	8	1,16
	t_{4-3+}	3										–		3		
	t_{4+2+}	2										–		2		
	t_{4-2-}	2										–		2		
Rise Time (20 to 80%)	t_{3+}	3	1.0	4.5	1.1	2.5	4.0	0.9	4.4			–		3		
	t_{2+}	2										–		2		
Fall Time (20 to 80%)	t_{3-}	3										–		3		
	t_{2-}	2										–		2		

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.





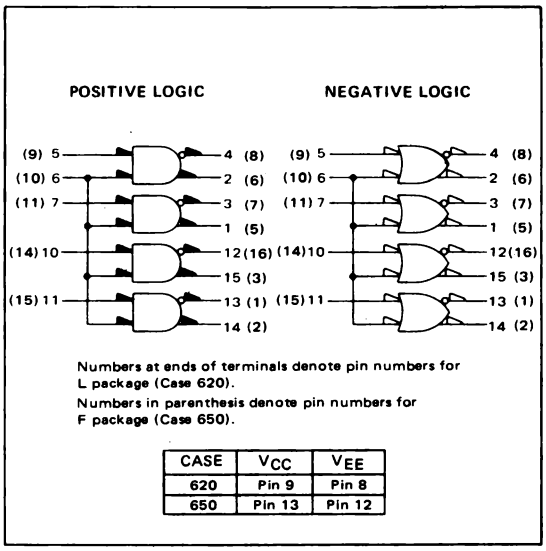
F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.830	-1.920	-1.255	-1.510	-5.2
+25°C	-0.720	-1.850	-1.105	-1.475	-5.2
+125°C	-0.580	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10521F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	29	–	20	26	–	29	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\,H}$	11	–	450	–	–	265	–	265	μAdc	11	–	–	–	12	4,5
		13	–	450	–	–	265	–	265	↓	13	–	–	–	↓	↓
		14	–	630	–	–	370	–	370		14	–	–	–		
	$I_{in\,L}$	11	0.5	–	0.5	–	–	0.3	–	μAdc	–	11	–	–	12	4,5
		13	↓	–	↓	–	–	↓	–	↓	–	13	–	–	↓	↓
		14		–		–	–		–		–	14	–	–		
Logic "1" Output Voltage	V_{OH}	7	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	1,14	8	–	–	12	4,5
		6	-1.080	-0.830	-0.930	–	-0.720	-0.825	-0.580	Vdc	1,8,14	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	1,8,14	–	–	–	12	4,5
		6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	1,14	8	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	7	-1.100	–	-0.950	–	–	-0.845	–	Vdc	1,14	–	–	8	12	4,5
		6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	1,14	–	8	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	1,14	–	8	–	12	4,5
		6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	1,14	–	–	8	12	4,5
Switching Times (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{8+7-}	7	–	–	1.4	2.3	3.4	–	–	ns	1,14	–	8	7	12	4,5
	t_{8-7+}	7	–	–	↓	↓	↓	–	–	↓	↓	–	↓	7	↓	↓
	t_{8+6+}	6	–	–				–	–			–		6		
	t_{8-6-}	6	–	–				–	–			–		6		
Rise Time (20 to 80%)	t_{7+}	7	–	–	1.1	2.5	4.0	–	–			–		7		
	t_{6+}	6	–	–				–	–			–		6		
Fall Time (20 to 80%)	t_{7-}	7	–	–				–	–			–		7		
	t_{6-}	6	–	–	↓	↓	↓	–	–	↓	↓	–	↓	6	↓	↓

MC10524

Advance Information



Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

CASE	V_{CC}	V_{EE}
620	Pin 9	Pin 8
650	Pin 13	Pin 12

The MC10524 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10524 has MTTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. Propagation delay of the MC10524 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

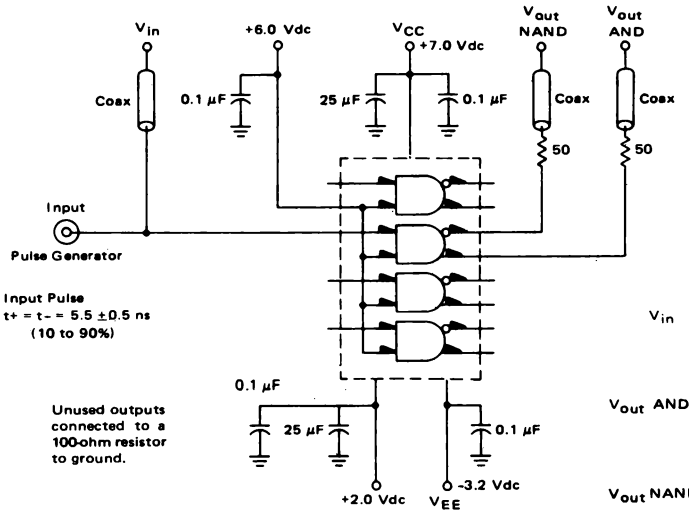
An advantage of this device is that MTTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10515 or MC10516 differential line receivers. The MC10524 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

P_D = 380 mW typ/pkg (No Load)

t_{pd} = 3.5 ns typ (+1.5 Vdc in to 50% out)

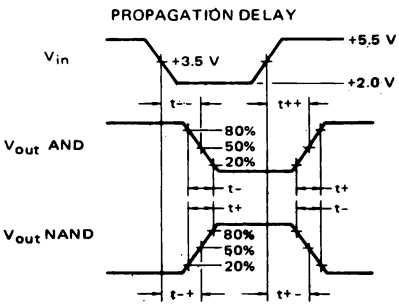
Output Rise, Fall Times;
2.5 ns typ (20% to 80%)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

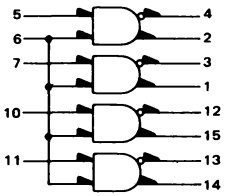
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

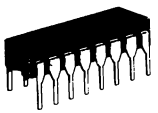


This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

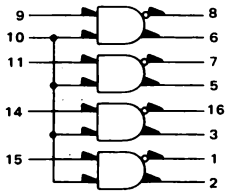
● Test Temperature	V_{IH} min	V_{IL} max	V_{RH}	V_F	V_R	V_{CC}	V_{EE}	I_{I1}	I_{I2}	I_{in}
	Volts							mA		
-55°C	+2.00	+1.10	+4.0	+0.40	+2.40	+5.00	-5.2	-10	-20	+1.0
+25°C	+1.80	+1.10	+4.0	+0.40	+2.40	+5.00	-5.2	-10	-20	+1.0
+125°C	+1.80	+0.80	+4.0	+0.40	+2.40	+5.00	-5.2	-10	-20	+1.0

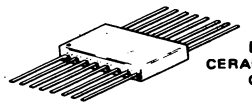
Characteristic	Symbol	Pin Under Test	MC10524L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH} min	V_{IL} max	V_{RH}	V_F	V_R	V_{CC}	V_{EE}	I_{I1}	I_{I2}	I_{in}	Gnd
Negative Power Supply Drain Current	I_E	8	–	–	–	–	-66	–	–	mAdc	–	–	–	–	–	9	8	–	–	–	16
Positive Power Supply Drain Current	I_{CCH}	9	–	–	–	–	16	–	–	mAdc	–	–	5,6,7,10,11	–	–	9	8	–	–	–	16
	I_{CCL}	9	–	–	–	–	25	–	–	mAdc	–	–	–	–	–	–	8	–	–	–	5,6,7,10,11,16
Reverse Current	I_R	6	–	–	–	–	200	–	–	µAdc	–	–	–	5,7,10,11	6	9	8	–	–	–	16
		7	–	–	–	–	50	–	–	µAdc	–	–	–	6	7	9	8	–	–	–	16
Forward Current	I_F	6	–	–	–	–	-12.8	–	–	mAdc	–	–	–	6	5,7,10,11	9	8	–	–	–	16
		7	–	–	–	–	-3.2	–	–	mAdc	–	–	–	7	6	9	8	–	–	–	16
Input Breakdown Voltage	BV_{in}	6	5.5	–	5.5	–	–	5.5	–	Vdc	–	–	–	–	–	9	8	–	–	6	16
		7	5.5	–	5.5		–	5.5	–	Vdc	–	–	–	6	–	9	8	–	–	7	16
Clamp Input Voltage	V_I	6	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	9	8	–	6	–	16
		7	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	9	8	7	–	–	16
High Output Voltage	V_{OH}	1	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	–	–	–	–	6,7	9	8	–	–	–	16
		3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	–	–	–	6	7	9	8	–	–	–	16
Low Output Voltage	V_{OL}	1	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	7	6	9	8	–	–	–	16
		3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	6,7	9	8	–	–	–	16
High Threshold Voltage	V_{OHA}	1	-1.000	–	-0.950	–	–	-0.845	–	Vdc	7	–	–	–	6	9	8	–	–	–	16
		3	-1.000	–	-0.950	–	–	-0.845	–	Vdc	–	7	–	–	6	9	8	–	–	–	16
Low Threshold Voltage	V_{OLA}	1	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	7	–	–	6	9	8	–	–	–	16
		3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	7	–	–	–	6	9	8	–	–	–	16
Switching Time (50 Ω load)											+6.0 Vdc	Pulse In	Pulse Out			+7.0 Vdc	-3.2 Vdc				+2.0 Vdc
Propagation Delay (+3.5 Vdc to 50%)①	t_{10+5+}	1	–	–	1.0	3.5	6.0	–	–	ns	7	6	5			9	8	–	–	–	16
	t_{10-5-}	↓	–	–	↓	↓	↓	–	–	↓	7	6	↓	–	–	↓	↓	–	–	–	↓
	t_{11+5+}		–	–				–	–		6	7		–	–			–	–	–	
	t_{11-5-}		–	–				–	–		↓	↓		–	–			–	–	–	
	t_{11+7-}	3	–	–				–	–				7	–	–			–	–	–	
	t_{11-7+}	3	–	–	↓	↓	↓	–	–				7	–	–			–	–	–	
Rise Time (20% to 80%)	t_{5+}	1	–	–	1.1	2.5	3.9	–	–				5	–	–			–	–	–	
Fall Time (80% to 20%)	t_{5-}	1	–	–	1.1	2.5	3.9	–	–	↓	↓	↓	5	–	–	↓	↓	–	–	–	↓

① See switching time test circuit. Propagation delay for this circuit is specified from +1.5 Vdc in to the 50% point on the output waveform. The +3.5 Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

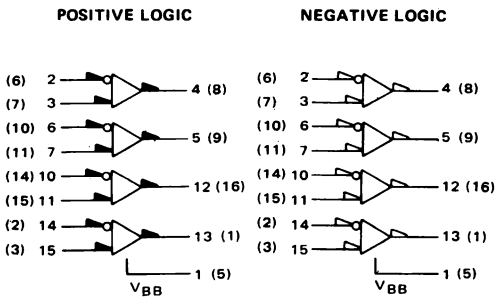
@ Test Temperature	$V_{IH\ min}$	$V_{IL\ max}$	V_{RH}	V_F	V_R	V_{CC}	V_{EE}	I_{I1}	I_{I2}	I_{in}
	TEST VOLTAGE/CURRENT VALUES									
	Volts							mA		
-55°C	+2.00	+1.10	+4.0	+0.40	+2.40	+5.00	-5.2	-10	-12	+1.0
+25°C	+1.80	+1.10	+4.0	+0.40	+2.40	+5.00	-5.2	-10	-12	+1.0
+125°C	+1.80	+0.80	+4.0	+0.40	+2.40	+5.00	-5.2	-10	-12	+1.0

Characteristic	Symbol	Pin Under Test	MC10524F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IH\ min}$	$V_{IL\ max}$	V_{RH}	V_F	V_R	V_{CC}	V_{EE}	I_{I1}	I_{I2}	I_{in}	Gnd
Negative Power Supply Drain Current	I_E	12	–	–	–	–	-66	–	–	mAdc	–	–	–	–	–	13	12	–	–	–	4
Positive Power Supply Drain Current	I_{CCH}	13	–	–	–	–	16	–	–	mAdc	–	–	9,10,11,14,15	–	–	13	12	–	–	–	4
	I_{CCL}	13	–	–	–	–	25	–	–	mAdc	–	–	–	–	–	–	12	–	–	–	4,9,10,11,14,15
Reverse Current	I_R	10	–	–	–	–	200	–	–	µAdc	–	–	–	9,11,14,15	10	13	12	–	–	–	4
		11	–	–	–	–	50	–	–	µAdc	–	–	–	10	11	13	12	–	–	–	4
Forward Current	I_F	10	–	–	–	–	-12.8	–	–	mAdc	–	–	–	10	9,11,14,15	13	12	–	–	–	4
		11	–	–	–	–	-3.2	–	–	mAdc	–	–	–	11	10	13	12	–	–	–	4
Input Breakdown Voltage	BV_{in}	10	5.5	–	5.5	–	–	5.5	–	Vdc	–	–	–	–	–	13	12	–	–	10	4
		11	5.5	–	5.5	–	–	5.5	–	Vdc	–	–	–	10	–	13	12	–	–	11	4
Clamp Input Voltage	V_I	10	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	13	12	–	10	–	4
		11	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	13	12	11	–	–	4
High Output Voltage	V_{OH}	5	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	–	–	–	–	10,11	13	12	–	–	–	4
		8	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	–	–	–	10	11	13	12	–	–	–	4
Low Output Voltage	V_{OL}	5	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	11	10	13	12	–	–	–	4
		8	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	10,11	13	12	–	–	–	4
High Threshold Voltage	V_{OHA}	5	-1.000	–	-0.950	–	–	-0.845	–	Vdc	11	–	–	–	10	13	12	–	–	–	4
		8	-1.000	–	-0.950	–	–	-0.845	–	Vdc	–	11	–	–	10	13	12	–	–	–	4
Low Threshold Voltage	V_{OLA}	5	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	11	–	–	10	13	12	–	–	–	4
		8	–	-1.635	–	–	-1.600	–	-1.525	Vdc	11	–	–	–	10	13	12	–	–	–	4
Switching Time (50-Ω load)											+6.0 Vdc	Pulse In	Pulse Out			+7.0 Vdc	-3.2 Vdc				+2.0 Vdc
Propagation Delay (+3.5 Vdc to 50%) ①	t_{10+5+}	5	–	–	1.0	3.5	6.0	–	–	ns	11	10	5	–	–	13	12	–	–	–	4
	t_{10-5-}		–	–				–	–		11	10		–	–			–	–	–	
	t_{11+5+}		–	–				–	–		10	11		–	–			–	–	–	
	t_{11-5-}		–	–				–	–					–	–			–	–	–	
	t_{11+7-}	7	–	–				–	–				7	–	–			–	–	–	
	t_{11-7+}	7	–	–				–	–				7	–	–			–	–	–	
Rise Time (20% to 80%)	t_{5+}	5	–	–	1.1	2.5	3.9	–	–				5	–	–			–	–	–	
Fall Time (80% to 20%)	t_{5-}	5	–	–	1.1	2.5	3.9	–	–				5	–	–			–	–	–	

① See switching time test circuit. Propagation delay for this circuit is specified from +1.5 Vdc in to the 50% point on the output waveform. The +3.5 Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

MC10525

Advance Information



Numbers at end of terminals denote pin numbers for L package (Case 620).

Numbers in parenthesis denote pin numbers for F package (Case 650).

CASE	V_{CC}	V_{EE}
620	Pin 9	Pin 8
650	Pin 13	Pin 12

The MC10525 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10525 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available for use in single-ended input biasing. The outputs of the MC10525 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and -5.2 Volts. Propagation delay of the MC10525 is typically 4.5 ns. The MC10525 has fanout of 6 MTTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or MTTL out. This device has an input common mode noise rejection of ±1.0 Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the MTTL equipment. This isolates the MECL logic from the noisy MTTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

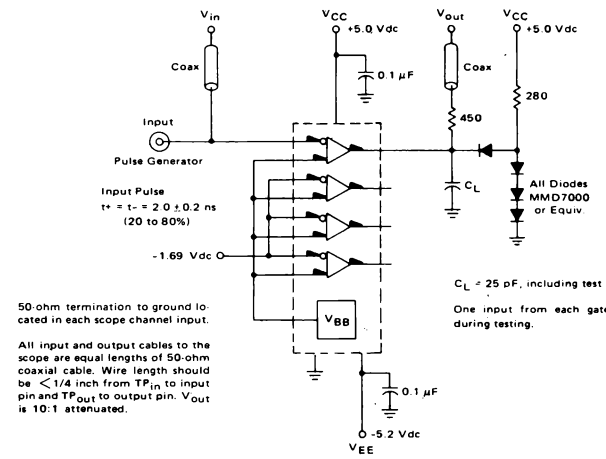
P_D = 380 mW typ/pkg (No Load)

t_{pd} = 4.5 ns typ (50% to +1.5 Vdc out)

Output Rise, Fall Times;
2.5 ns typ (20% to 80%)

V_{CCmax} = +7.00 Vdc

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



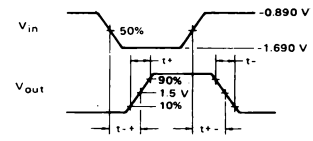
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 10:1 attenuated.

C_L = 25 pF, including test fixture

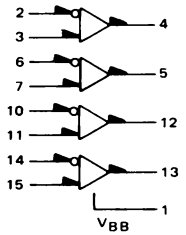
One input from each gate must be tied to V_{BB} during testing.

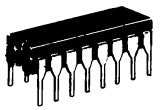
PROPAGATION DELAY



ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

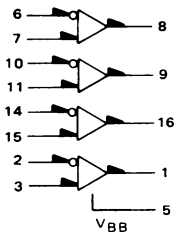
@ Test Temperature	TEST VOLTAGE VALUES (Volts)										
	$V_{IH\ max}$	$V_{IL\ min}$	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	+0.170	-0.920	-1.830	-2.920	From Pin 1	+5.0	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	+0.280	-0.850	-1.720	-2.850		+5.0	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	+0.420	-0.820	-1.580	-2.820		+5.0	-5.2

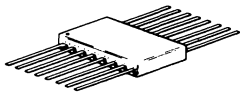
Characteristic	Symbol	Pin Under Test	MC10525L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_E	8	–	–	–	–	40	–	–	mAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Positive Power Supply Drain Current	I_{CCH}	9	–	–	–	–	52	–	–	mAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
	I_{CCL}	9	–	–	–	–	39	–	–	mAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Input Current	I_{in} H ①	2	–	–	–	–	115	–	–	µAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
		3	–	–	–	–	115	–	–	µAdc	3,7,11,15	–	–	–	–	–	–	–	2,6,10,14	9	8	16	–
Input Leakage Current	I_{CBO} ②	2	–	–	–	–	1.0	–	–	µAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	2,6,8,10,14	16	–
		3	–	–	–	–	1.0	–	–	µAdc	–	–	–	–	–	–	–	–	2,6,10,14	9	3,7,8,11,15	16	–
Short-Circuit Current	I_{OS}	4	–	–	40	–	100	–	–	mA	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	4,16	–
High Output Voltage	V_{OH} ③	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Output Voltage	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	12.0 mA
High Threshold Voltage	V_{OHA}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	6,10,14	–	2	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Threshold Voltage	V_{OLA}	4	–	0.5	–	–	0.5	–	0.5	Vdc	6,10,14	–	2	–	–	–	–	–	3,7,11,15	9	8	16	12.0 mA
Indeterminate Input Protection Tests	V_{OLS1}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–	–	9	2,3,6,7,8, 10,11,14,15	16	12.0 mA
	V_{OLS2}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–	–	9	8	16	12.0 mA
Reference Voltage	V_{BB}	1	-1.440	-1.320	-1.350	–	-1.230	-1.240	-1.120	Vdc	–	–	–	–	–	–	–	–	3,7,11,15	–	–	–	–
Common Mode Rejection Tests	V_{OH}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	–	–	–	3	2	–	–	–	9	8	16	-2.0 mA
		4	2.5	–	2.5	–	–	2.5	–		–	–	–	–	–	–	3	2	–	9	8	16	-2.0 mA
	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	2	3	–	–	–	9	8	16	12.0 mA
		4	–	0.5	–	–	0.5	–	0.5		–	–	–	–	–	–	2	3	–	9	8	16	12.0 mA
Switching Times											Pulse In	Pulse Out	C_L (pF)										
Propagation Delay (50% to +1.5 Vdc)	t_{6+5-}	5	–	–	1.0	4.5	6.0	–	–	ns	6	5	25	–	–	–	–	–	3,7,11,15	9	8	16	–
	t_{6-5+}	5	–	–				–	–		6	5		–	–	–	–	–					–
	t_{2+4-}	4	–	–				–	–		2	4		–	–	–	–	–					–
	t_{2-4+}		–	–				–	–					–	–	–	–	–					–
Rise Time (+1.0 Vdc to 2.0 Vdc)	t_{4+}		–	–	–	–	3.3	–	–					–	–	–	–	–					–
Fall Time (+1.0 Vdc to 2.0 Vdc)	t_{4-}		–	–	–	–	3.3	–	–					–	–	–	–	–					–

① Individually test each input, apply $V_{IH\ max}$ to pin under test.
② Individually test each input, apply V_{EE} to pin under test.
③ Individually test each output, following example shown for pin 4.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	$V_{IH\ max}$	$V_{IL\ min}$	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	+0.170	-0.920	-1.830	-2.920	From Pin 5	+5.0	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	+0.280	-0.850	-1.720	-2.850		+5.0	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	+0.420	-0.820	-1.580	-2.820		+5.0	-5.2

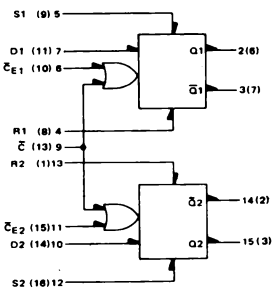
Characteristic	Symbol	Pin Under Test	MC10525F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_E	12	—	—	—	—	40	—	—	mAdc	—	—	—	—	—	—	—	—	3,7,11,15	13	12	4	—
Positive Power Supply Drain Current	I_{CCH}	13	—	—	—	—	52	—	—	mAdc	2,6,10,14	—	—	—	—	—	—	—	3,7,11,15	13	12	4	—
	I_{CCL}	13	—	—	—	—	39	—	—	mAdc	—	—	—	—	—	—	—	—	3,7,11,15	13	12	4	—
Input Current	$I_{in}H$ ①	6	—	—	—	—	115	—	—	μAdc	2,6,10,14	—	—	—	—	—	—	—	3,7,11,15	13	12	4	—
		7	—	—	—	—	115	—	—	μAdc	3,7,11,15	—	—	—	—	—	—	—	2,6,10,14	13	12	4	—
Input Leakage Current	I_{CBO} ②	6	—	—	—	—	1.0	—	—	μAdc	—	—	—	—	—	—	—	—	3,7,11,15	13	2,6,10,12,14	4	—
		7	—	—	—	—	1.0	—	—	μAdc	—	—	—	—	—	—	—	—	2,6,10,14	13	3,7,11,12,15	4	—
Short-Circuit Current	I_{OS}	8	—	—	40	—	100	—	—	mA	—	2,6,10,14	—	—	—	—	—	—	3,7,11,15	13	12	4,8	—
High Output Voltage	V_{OH} ③	8	2.5		2.5	—	—	2.5	—	Vdc	—	2,6,10,14	—	—	—	—	—	—	3,7,11,15	13	12	4	2.0 mA
Low Output Voltage	V_{OL}	8	—	0.5	—	—	0.5	—	0.5	Vdc	2,6,10,14	—	—	—	—	—	—	—	3,7,11,15	13	12	4	12.0 mA
High Threshold Voltage	V_{OHA}	8	2.5	—	2.5	—	—	2.5	—	Vdc	—	2,10,14	—	6	—	—	—	—	3,7,11,15	13	12	4	2.0 mA
Low Threshold Voltage	V_{OLA}	8	—	0.5	—	—	0.5	—	0.5	Vdc	2,10,14	—	6	—	—	—	—	—	3,7,11,15	13	12	4	12.0 mA
Indeterminate Input Protection Tests	V_{OLS1}	8	—	0.5	—	—	0.5	—	0.5	Vdc	—	—	—	—	—	—	—	—	—	13	2,3,6,7,10, 11,12,14,15	4	12.0 mA
	V_{OLS2}	8	—	0.5	—	—	0.5	—	0.5	Vdc	—	—	—	—	—	—	—	—	—	13	12	4	12.0 mA
Reference Voltage	V_{BB}	5	-1.440	-1.320	-1.350	—	-1.230	-1.240	-1.120	Vdc	—	—	—	—	—	—	—	—	3,7,11,15	—	—	—	—
Common Mode Rejection Tests	V_{OH}	8	2.5		2.5	—	—	2.5	—	Vdc	—	—	—	—	7	6	—	—	—	13	12	4	2.0 mA
		8	2.5		2.5	—	—	2.5	—	—	—	—	—	—			7	6	—	13	12	4	2.0 mA
	V_{OL}	8	—	0.5	—	—	0.5	—	0.5	Vdc	—	—	—	—	6	7	—		—	13	12	4	12.0 mA
		8	—	0.5	—	—	0.5	—	0.5	—	—	—	—	—	—	—	6	7	—	13	12	4	12.0 mA
Switching Times											Pulse In	Pulse Out	C_L (pF)										
Propagation Delay (50% to +1.5 Vdc)	t_{10+9-}	9	—	—	1.0	4.5	6.0	—	—	ns	10	9	25	—	—	—	—	—	3,7,11,15	13	12	4	—
	t_{10-9+}	9	—	—				—	—		10	9		—	—	—	—	—					—
	t_{6+8-}	8	—	—				—	—		6	8		—	—	—	—	—					—
	t_{6-8+}		—	—				—	—					—	—	—	—	—					—
Rise Time (+1.0 Vdc to 2.0 Vdc)	t_{8+}		—	—	—	—	3.3	—	—					—	—	—	—	—					—
Fall Time (+1.0 Vdc to 2.0 Vdc)	t_{8-}		—	—	—	—	3.3	—	—					—	—	—	—	—					—

① Individually test each input, apply $V_{IH\ max}$ to pin under test.
② Individually test each input, apply V_{EE} to pin under test.
③ Individually test each output, following example shown for pin 8.

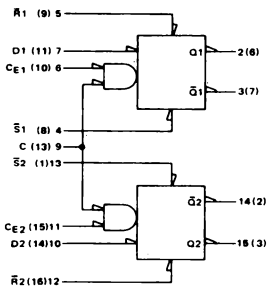
MC10530

Advance Information

POSITIVE LOGIC



NEGATIVE LOGIC



TRUTH TABLE

D	$\bar{C}$	$\bar{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
φ	L	H	Q_n
φ	H	L	Q_n
φ	H	H	Q_n

φ = Don't Care

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

P_D = 145 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

The MC10530 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\bar{C}_E$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\bar{C}$).

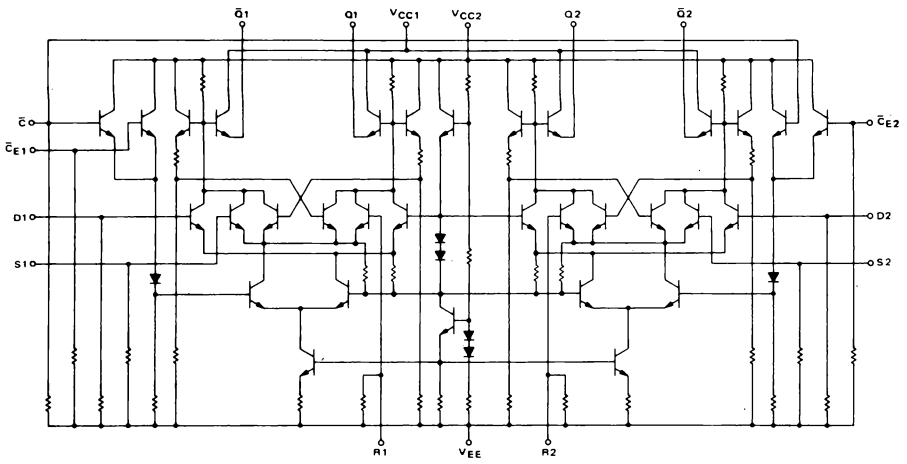
Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

Output rise and fall times have been optimized to provide relaxation of system layout and design criteria.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\bar{C}$ or $\bar{CE}$ or both are high.

CIRCUIT SCHEMATIC

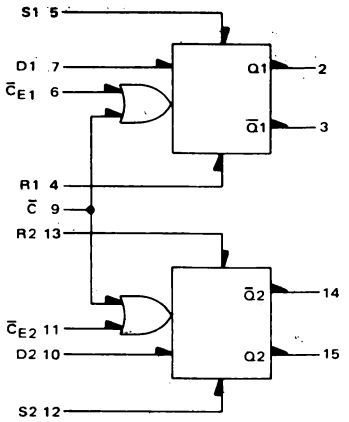


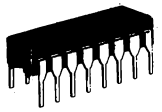
This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

(1) See test circuit for test procedures.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

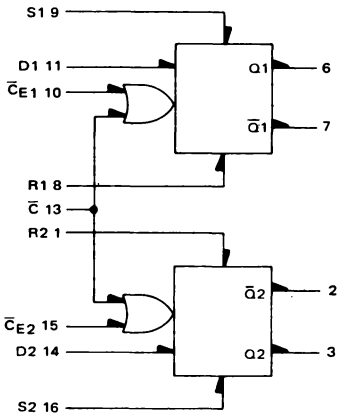
Characteristic	Symbol	Pin Under Test	MC10530L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	39	–	28	35	–	39	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	6	–	375	–	–	220	–	220	μAdc	6	–	–	–	8	1,16
		9	–	450	–	–	265	–	265		9	–	–	–		
		4	–	485	–	–	285	–	285		4,9	–	–	–		
		7	–	485	–	–	285	–	285		7,9	9	–	–		
	I_{inL}	4*	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	7	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	7	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	7	8	1,16
Switching Times (50 Ω Load) (See Figure 1)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+2+}	2	–	–	1.0	2.7	3.5	–	–	ns	–	–	7	2	8	1,16
	t_{5+2+}		–	–		2.7		–	–		6	–	5			
	t_{4+2-}		–	–		2.7		–	–		6	–	4			
	t_{6-2-}		–	–		–	4.0	–	–		–	–	6			
Rise Time (20% to 80%)	t_{2+}		–	–	1.1	2.7	3.5	–	–		–	–	7			
Fall Time (20% to 80%)	t_{2-}		–	–	1.1	2.7	3.5	–	–		–	–	7			
Setup Time	t_{setup}	2	–	–	2.5	–	–	–	–	ns	(1)	–	6,7	2	8	1,16
Hold Time	t_{hold}	2	–	–	1.5	–	–	–	–	ns	(1)	–	6,7	2	8	1,16

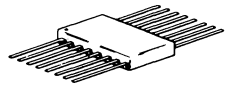
*All other inputs are tested in the same manner

(1) See test circuit for test procedures.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

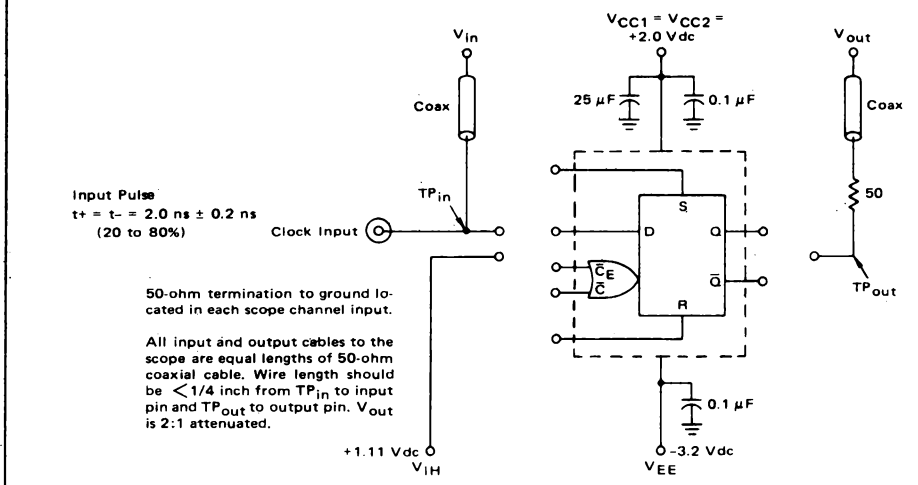
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

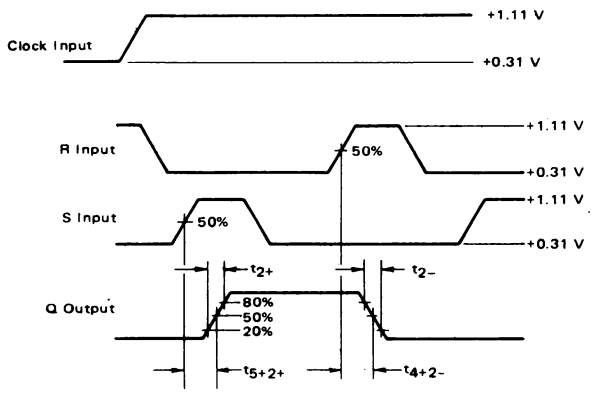
Characteristic	Symbol	Pin Under Test	MC10530F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	39	–	28	35	–	39	mAdc	13	–	–	–	12	4,5
Input Current	I_{inH}	10	–	375	–	–	220	–	220	μAdc	10	–	–	–	12	4,5
		13	–	450	–	–	265	–	265	↓	13	–	–	–	↓	↓
		8	–	485	–	–	285	–	285		8,13	–	–	–		
		11	–	485	–	–	285	–	285		11,13	–	–	–		
	I_{inL}	8*	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	11	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	11	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	11	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	11	12	4,5
Switching Times (50 Ω Load) (See Figure 1)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{11+6+}	6	–	–	1.0	2.7	3.5	–	–	ns	–	–	11	6	12	4,5
	t_{9+6+}	↓	–	–	↓	2.7	↓	–	–	↓	10	–	9	↓	↓	↓
	t_{8+6-}		–	–		2.7		–	–		10	–	8			
	t_{10-6-}		–	–	↓	–	4.0	–	–		–	–	10			
Rise Time (20% to 80%)	t_{6+}		–	–	1.1	2.7	3.5	–	–		–	–	11	↓	↓	↓
Fall Time (20% to 80%)	t_{6-}	↓	–	–	1.1	2.7	3.5	–	–	↓	–	–	11			
Setup Time	t_{setup}	6	–	–	2.5	–	–	–	–	ns	①	–	10,11	6	12	4,5
Hold Time	t_{hold}	6	–	–	1.5	–	–	–	–	ns	①	–	10,11	6	12	4,5

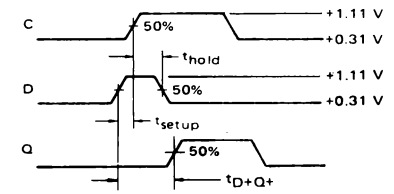
*All other inputs are tested in the same manner

① See test circuit for test procedures.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25° C







NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

MC10531

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care

$C = \bar{C}_E + C_C$

A clock H is a clock transition from a low to a high state.

CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

The MC10531 is a dual master-slave type D flip-flop. Asynchronous inputs Set (S) and Reset (R) override the Clock (C_C) and Clock Enable ($\bar{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

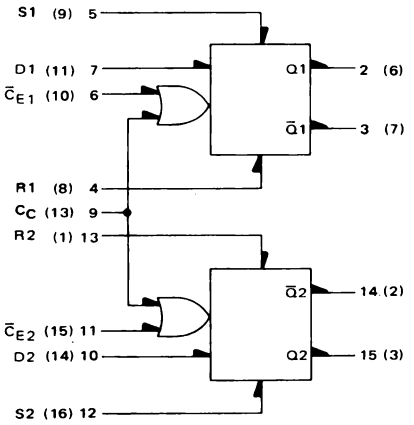
The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

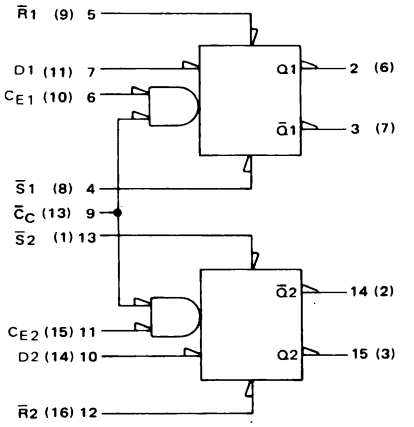
P_D = 235 mW typ/pkg

f_{Tog} = 160 MHz typ

POSITIVE LOGIC



NEGATIVE LOGIC

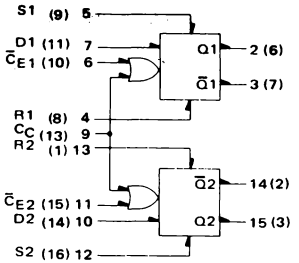


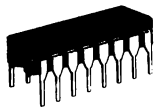
Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

See General Information section for packaging.

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Vdc ± 1%) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.500	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10531L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	62	–	45	56	–	62	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	565	–	–	330	–	330	μAdc	4	–	–	–	8	1, 16
		5	–	565	–	–	330	–	330		5	–	–	–		
		6	–	375	–	–	220	–	220		6	–	–	–		
		7	–	420	–	–	245	–	245		7	–	–	–		
		9	–	450	–	–	265	–	265		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1, 16
		6,7,9*	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	5	–	–	–	8	1, 16
		2†	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	5	–	–	–	8	1, 16
		3†	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	5	–	8	-1, 16
		2†	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	5	–	8	1, 16
		3†	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	7	9	8	1, 16
Switching Times (100-ohm load) Clock Input											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{9+2-}	2	1.4	4.6	1.5	3.0	4.5	1.5	5.0	ns	–	–	9	2	8	1, 16
	t_{9+2+}	2									7	–	9	2		
	t_{6+2+}	2									7	–	6	2		
	t_{6+2-}	2									–	–	6	2		
Rise Time (20 to 80%)	t_{2+}	2	1.0		1.1	2.5		1.1	4.9		–	–	9	2		
Fall Time (20 to 80%)	t_{2-}	2	1.0		1.1	2.5		1.1	4.9		–	–	9	2		
Set Input Propagation Delay	t_{5+2+}	2	1.1	4.5	1.2	2.8	4.3	1.2	4.9	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15									–	–	12	15		
	t_{5+3-}	3									–	–	5	3		
	t_{12+14-}	14									–	–	12	14		
Reset Input Propagation Delay	t_{4+2-}	2	1.1	4.5	1.2	2.8	4.3	1.2	4.9	ns	–	–	4	2	8	1, 16
	t_{13+15-}	15									–	–	13	15		
	t_{4+3+}	3									–	–	4	3		
	t_{13+14+}	14									–	–	13	14		
Setup Time	t_{setup}	7	–	–	2.5	1.5	–	–	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{hold}	7	–	–	1.5	-0.5	–	–	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	115	–	125	160	–	125	–	MHz	**	–	6	2	8	1, 16

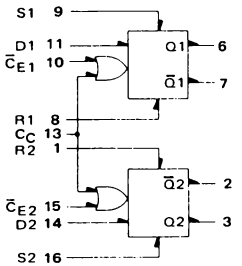
*Individually test each input; apply V_{IL} min to pin under test.

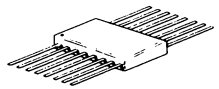
**Pin 3 is tied to pin 7 for these tests.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6)

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES Vdc ± 1% V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.500	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10531F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	62	–	45	56	–	62	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	8	–	565	–	–	330	–	330	µAdc	8	–	–	–	12	4,5
		9	–	565	–	–	330	–	330		9	–	–	–		
		10	–	375	–	–	220	–	220		10	–	–	–		
		11	–	420	–	–	245	–	245		11	–	–	–		
		13	–	450	–	–	265	–	265		13	–	–	–		
Input Leakage Current	I_{inL}	8,9*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	12	4,5
		10,11,13*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	9	–	–	–	12	4,5
		6†	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	11	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	9	–	–	–	12	4,5
		7†	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	11	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	9	–	12	4,5
		6†	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	1	13	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	9	–	12	4,5
		7†	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	1	13	12	4,5
Switching Times (100-ohm load) Clock Input											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{13+6-}	6	–	–	1.5	3.0	4.5	–	–	ns	–	–	13	6	12	4,5
	t_{13+6+}	6	–	–				–	–		11	–	13	6		
	t_{10+6+}	6	–	–				–	–		11	–	10	6		
	t_{10+6-}	6	–	–				–	–		–	–	10	6		
Rise Time (20 to 80%)	t_{6+}	6	–	–	1.1	2.5		–	–		–	–	13	6		
Fall Time (20 to 80%)	t_{6-}	6	–	–	1.1	2.5		–	–		–	–	13	6		
Set Input Propagation Delay	t_{9+6+}	6	–	–	1.2	2.8	4.3	–	–	ns	–	–	9	6	12	4,5
	t_{16+3+}	3	–	–				–	–		–	–	16	3		
	t_{9+7-}	7	–	–				–	–		–	–	9	7		
	t_{16+2-}	2	–	–				–	–		–	–	16	2		
Reset Input Propagation Delay	t_{8+6-}	6	–	–	1.2	2.8	4.3	–	–	ns	–	–	8	6	12	4,5
	t_{1+3-}	3	–	–				–	–		–	–	1	3		
	t_{8+2+}	7	–	–				–	–		–	–	8	7		
	t_{1+2+}	2	–	–				–	–		–	–	1	2		
Setup Time	t_{setup}	11	–	–	–	1.5	2.5	–	–	ns	–	–	10,11	6	12	4,5
Hold Time	t_{hold}	11	–	–	1.5	-0.5	–	–	–	ns	–	–	10,11	6	12	4,5
Toggle Frequency (Max)	f_{Tog}	6	–	–	125	160	–	–	–	MHz	**	–	10	6	12	4,5

*Individually test each input; apply V_{IL} min to pin under test.

**Pin 3 is tied to pin 7 for these tests.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 10)

FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT

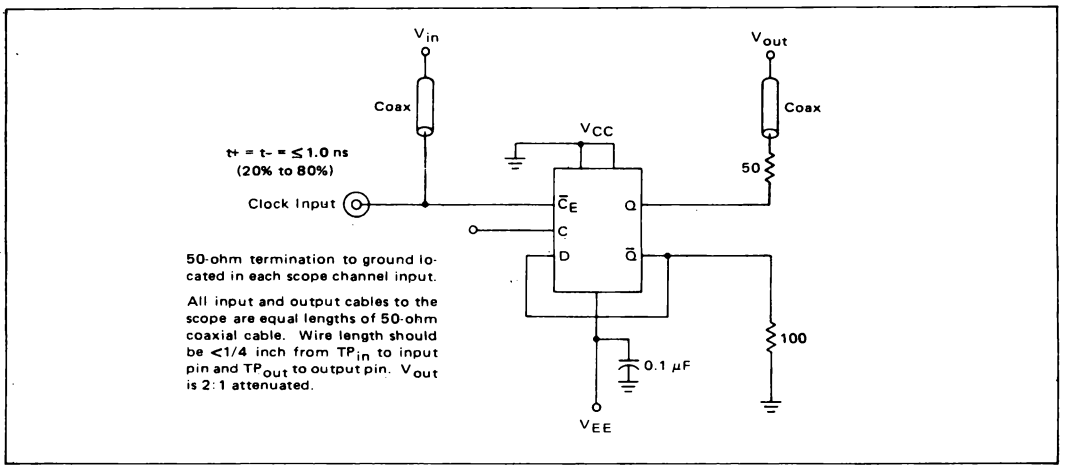
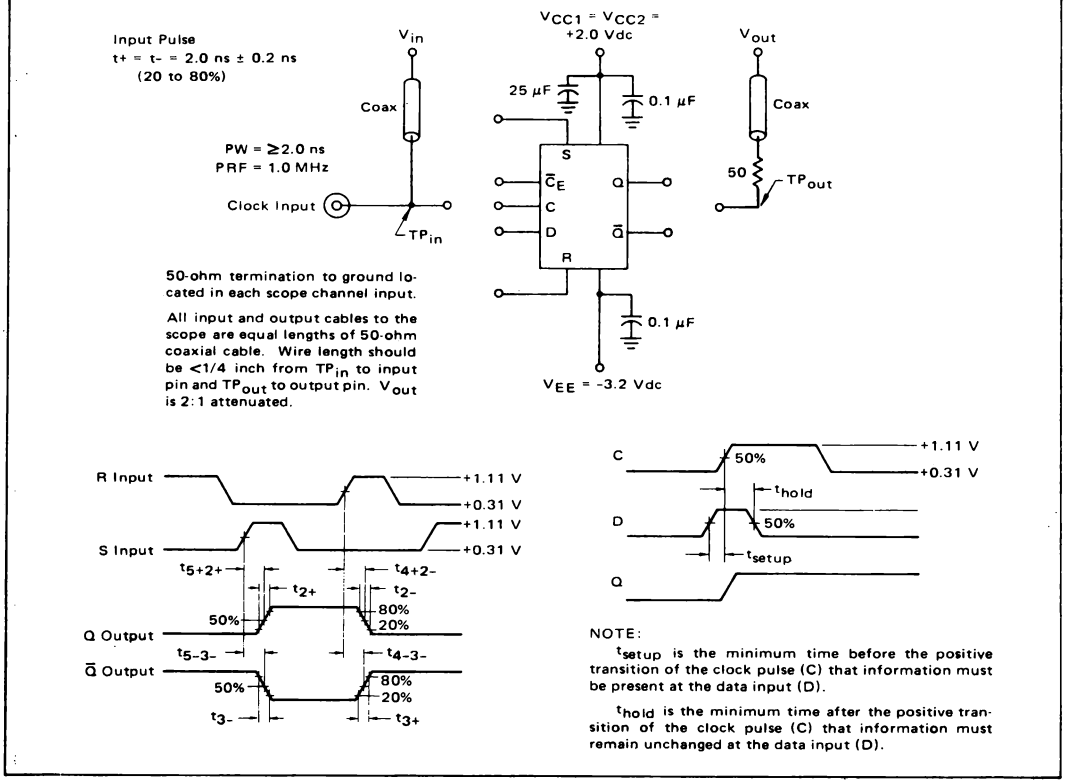


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

QUAD LATCH

MC10533

The MC10533 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on negative going transition of the clock.

TRUTH TABLE

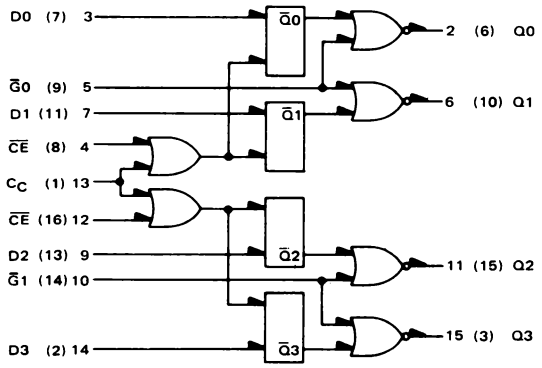
$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

ϕ = Don't Care

$C = C_C + \overline{CE}$

P_D = 310 mW typ
t_{pd} = 4.0 ns typ

POSITIVE LOGIC



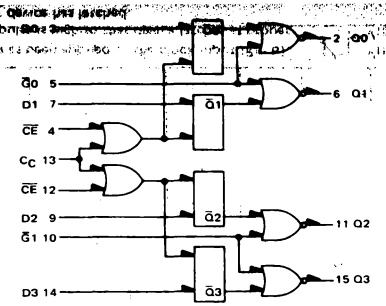
Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

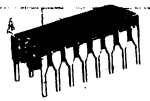
Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

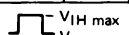
@ Test Temperature	†TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{IHAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10533L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{IHAmax}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	60	75	–	–	mAdc	–	13	–	–	8	1,16
Input Current	$I_{in\ H}$	3	–	–	–	–	245	–	–	μAdc	3	–	–	–	8	1,16
		4	–	–	–	–	265	–	–		4	–	–	–		
		5	–	–	–	–	350	–	–		5	–	–	–		
		13	–	–	–	–	350	–	–		13	–	–	–		
	$I_{in\ L}$	3	–	–	0.5	–	–	–	–	μAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	3,4	–	–	–	8	1,16
		2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	3,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	13	3	–	–	8	1,16
		2				–					3,5,13	–	–	–		
		2				–					4	3	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	3,4	–	–	5	8	1,16
		2		–		–	–		–		4	–	3	–		
		2		–		–	–		–		3,4	–	–	–		
		2†		–		–	–		–		3	–	–	–		
		2††		–		–	–		–		–	–	–	–		
		2††		–		–	–		–		–	–	–	4		
		2		–		–	–		–		3	–	4	–		
		2		–		–	–		–		3	–	13	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	3,4	–	5	–	8	1,16
		2	–		–	–		–			4	–	–	3		
		2	–		–	–		–			4	–	–	–		
		2†	–		–	–		–			–	–	–	–		
		2††	–		–	–		–			3	–	–	–		
		2††	–		–	–		–			3	–	–	13		
Switching Times (100-ohm Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–	–	1.0	–	5.4	–	–	ns	4	–	3	2	8	1,16
	t_{4-2+}	2	–	–		–	5.4	–	–		3*	–	4	2		
	t_{5-2+}	2	–	–		–	3.1	–	–		–	–	5	2		
	t_{setup}	3	–	–	2.5	–	–	–	–		–	–	3	2		
	t_{hold}	3	–	–	1.5	–	–	–	–		–	–	3	2		
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.1	–	3.5	–	–		4	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	–	–	1.1	–	3.5	–	–		4	–	3	2		

†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

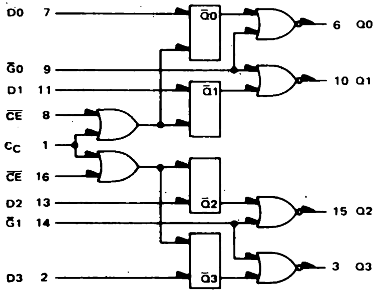
††Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

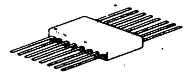
*Latch set to zero state before test.



ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

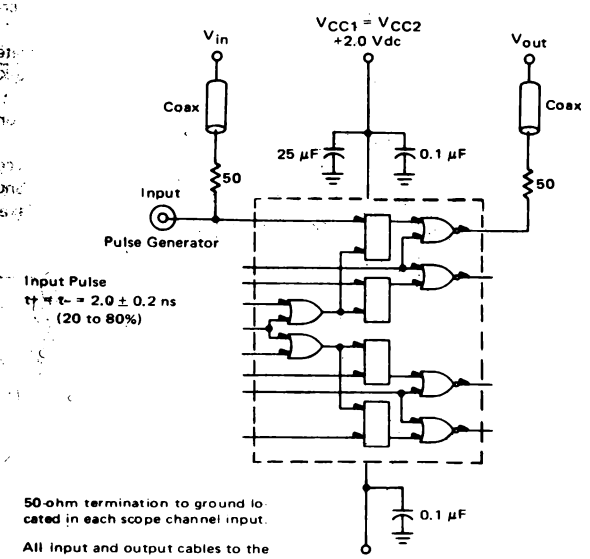
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{IHAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

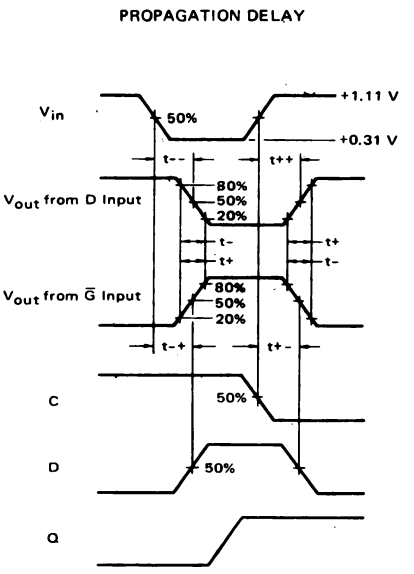
Characteristic	Symbol	Pin Under Test	MC10533F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{IHAmax}	V_{EE}	Gnd
Power Supply Drain Current	I_E	12	–	–	–	60	75	–	–	mAdc	–	1	–	–	12	4,5
Input Current	$I_{in H}$	7	–	–	–	–	245	–	–	µAdc	7	–	–	–	12	4,5
		8	–	–	–	–	265	–	–	↓	8	–	–	–	↓	↓
		9	–	–	–	–	350	–	–	↓	9	–	–	–	↓	↓
		1	–	–	–	–	350	–	–	↓	1	–	–	–	↓	↓
	$I_{in L}$	7	–	–	0.5	–	–	–	–	µAdc	–	7	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	7,8	–	–	–	12	4,5
		6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	1,7	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	1	7	–	–	12	4,5
		6	↓	↓	↓	–	↓	↓	↓	↓	1,7,9	–	–	–	↓	↓
		6	↓	↓	↓	–	↓	↓	↓	↓	8	7	–	–	↓	↓
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	7,8	–	–	9	12	4,5
		6	↓	–	↓	–	–	↓	–	↓	8	–	7	–	↓	↓
		6	↓	–	↓	–	–	↓	–	↓	7,8	–	–	–	↓	↓
		6†	↓	–	↓	–	–	↓	–	↓	7	–	–	–	↓	↓
		6††	↓	–	↓	–	–	↓	–	↓	–	–	–	–	↓	↓
		6††	↓	–	↓	–	–	↓	–	↓	–	–	–	8	↓	↓
		6	↓	–	↓	–	–	↓	–	↓	7	–	7	–	↓	↓
		6	↓	–	↓	–	–	↓	–	↓	7	–	1	–	↓	↓
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	7,8	–	9	–	12	4,5
		6	–	↓	–	–	↓	–	↓	↓	8	–	–	7	↓	↓
		6	–	↓	–	–	↓	–	↓	↓	8	–	–	–	↓	↓
		6†	–	↓	–	–	↓	–	↓	↓	–	–	–	–	↓	↓
		6††	–	↓	–	–	↓	–	↓	↓	7	–	–	–	↓	↓
		6††	–	↓	–	–	↓	–	↓	↓	7	–	–	1	↓	↓
Switching Times (100-ohm Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	6	–	–	1.0	–	5.4	–	–	ns	8	–	7	6	12	4,5
	t_{4-2+}	6	–	–	↓	–	5.4	–	–	↓	7*	–	8	6	↓	↓
	t_{5-2+}	6	–	–	↓	–	3.1	–	–	↓	–	–	9	6	↓	↓
	t_{setup}	7	–	–	2.5	–	–	–	–	↓	–	–	7	6	↓	↓
	t_{hold}	7	–	–	1.5	–	–	–	–	↓	–	–	7	6	↓	↓
Rise Time (20% to 80%)	t_{2+}	6	–	–	1.1	–	3.5	–	–	↓	8	–	7	6	↓	↓
Fall Time (20% to 80%)	t_{2-}	6	–	–	1.1	–	3.5	–	–	↓	8	–	7	6	↓	↓

†Output level to be measured after a clock pulse has been applied to the clock input (Pin 8). $V_{IH\,max}$ / $V_{IL\,min}$

††Data input at proper high/low level while clock pulse is high so that device latches at proper

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C





t_{setup} is minimum time before the negative transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

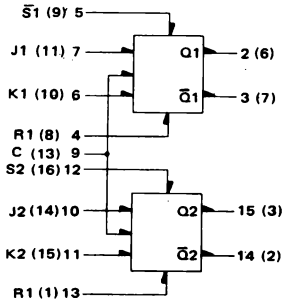
APPLICATION INFORMATION

The MC10533 device consists of four bistable latch circuits with D type inputs and gated Q outputs. When the clock is high the outputs will follow the D inputs. The latch will store the data on the falling edge of the clock. The outputs are gated when the output enable is low. All four latches may be clocked at one time with the common clock, or each half may be clocked separately with its clock. This device is useful as a temporary storage element in high speed central processors, accumulators, register files, digital communication systems, instrumentation and test equipment.

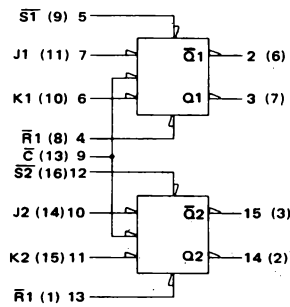
MC10535

Advance Information

POSITIVE LOGIC



NEGATIVE LOGIC



Numbers at ends of terminals denote pin numbers for L package (Case 620).

Numbers in parenthesis denote pin numbers for F package (Case 650).

CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

The MC10535 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{J}$-$\overline{K}$ inputs do not effect the output.

The output states of the flip-flop change on the positive transition of the clock.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

ϕ = Not Defined

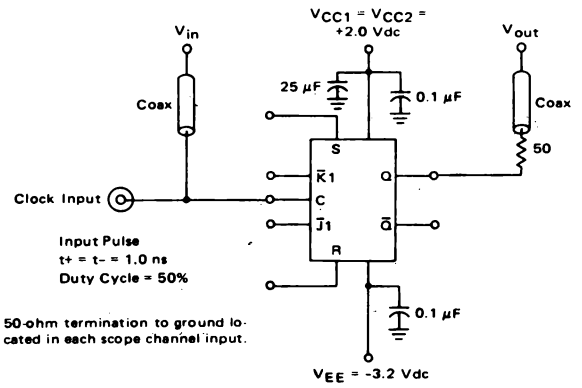
CLOCK J-K TRUTH TABLE*

J	K	Q_{n+1}
L	L	$\bar{Q}_n$
H	L	L
L	H	H
H	H	ϕ

*Output states change on positive transition of clock for J-K input condition present.

P_D = 280 mW typ/pkg (No Load)
f_{Tog} = 140 MHz typ

FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

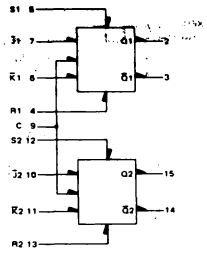
Unused outputs connected to a 50-ohm resistor to ground.

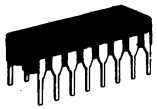
See General Information section for packaging.

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (VOLTS) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10535L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	75	–	54	68	–	75	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	6,7,9,10,11	–	450	–	–	265	–	265	µAdc	①	–	–	–	8	1,16
		4,5,12,13	–	665	–	–	390	–	390	µAdc	①	–	–	–	8	1,16
Input Leakage Current	$I_{in\ L}$	4,5,6,7,9,	0.5	–	0.5	–	–	0.3	–	µAdc	–	②	–	–	8	1,16
		10,11,12,13	0.5	–	0.5	–	–	0.3	–	µAdc	–	②	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	5	–	–	–	8	1,16
		2 ③	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	6	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	5	–	–	–	8	1,16
		3 ③	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	6	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	5	–	8	1,16
		2 ④	-1.100	–	-0.950	–	–	-0.845	–	Vdc	6	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	5	–	8	1,16
		3 ④	–	-1.635	–	–	-1.600	–	-1.525	Vdc	6	–	–	–	8	1,16
Switching Times													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{9+2+}	2	–	–	1.0	3.0	4.5	–	–	ns	–	–	9	2	8	1,16
	t_{9+2-}	2	–	–	1.0	3.0	↓	–	–	↓	–	–	9	2	↓	↓
Rise Time (20 to 80%)	$t_{2+,t3+}$	2,3	–	–	1.1	2.0	↓	–	–	↓	–	–	9	2,3	↓	↓
Fall Time (20 to 80%)	$t_{2-,t3-}$	2,3	–	–	1.1	2.0	↓	–	–	↓	–	–	9	2,3	↓	↓
Set Input Propagation Delay	t_{5+2+}	2	–	–	1.0	3.0	5.0	–	–	ns	–	–	5	2	8	1,16
	t_{12+15+}	15	–	–	↓	↓	↓	–	–	↓	–	–	12	15	↓	↓
	t_{5+3-}	3	–	–	↓	↓	↓	–	–	↓	–	–	5	3	↓	↓
	t_{12+14-}	14	–	–	↓	↓	↓	–	–	↓	–	–	12	14	↓	↓
Reset Input Propagation Delay	t_{4+2-}	2	–	–	1.0	3.0	5.0	–	–	ns	–	–	4	2	8	1,16
	t_{4+3+}	3	–	–	↓	↓	↓	–	–	↓	–	–	4	3	↓	↓
	t_{13+15-}	15	–	–	↓	↓	↓	–	–	↓	–	–	13	15	↓	↓
	t_{13+14+}	14	–	–	↓	↓	↓	–	–	↓	–	–	13	14	↓	↓
Setup Time	t_{setup}	7	–	–	1.5	–	–	–	–	ns	–	–	6,9 ⑤	2	8	1,16
Hold Time	t_{hold}	7	–	–	2.5	–	–	–	–	ns	–	–	6,9 ⑤	2	8	1,16
Toggle Frequency	f_{Tog}	2	–	–	125	140	–	–	–	MHz	–	–	9	2	9	1,16

NOTES:

① Individually test each input; apply $V_{IH\ max}$ to pin under test.

② Individually test each input; apply $V_{IL\ min}$ to pin under test.

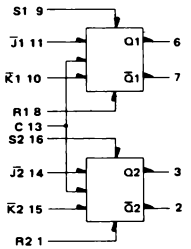
③ Output level to be measured after a clock pulse has been applied to the C input (pin 9) — $V_{IH\ max}$ / $V_{IL\ min}$

④ Output level to be measured after a clock pulse has been applied to the C input (pin 9) — $V_{IHA\ min}$ / $V_{ILA\ max}$

⑤ See Figure 2 for timing test diagram.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.



F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (VOLTS) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10535F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	75	–	54	68	–	75	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\ H}$	10,11,13,14,15	–	450	–	–	265	–	265	µAdc	①	–	–	–	12	4,5
		1,8,9,16	–	665	–	–	390	–	390	µAdc	①	–	–	–	12	4,5
Input Leakage Current	$I_{in\ L}$	8,9,10,11,13	0.5	–	0.5	–	–	0.3	–	µAdc	–	②	–	–	12	4,5
		1,14,15,16	0.5	–	0.5	–	–	0.3	–	µAdc	–	②	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	9	–	–	–	12	4,5
		6 ③	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	10	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	9	–	–	–	12	4,5
		7 ③	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	10	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	9	–	12	4,5
		6 ④	-1.100	–	-0.950	–	–	-0.845	–	Vdc	10	–	–	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	9	–	12	4,5
		7 ④	–	-1.635	–	–	-1.600	–	-1.525	Vdc	10	–	–	–	12	4,5
Switching Times													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{13+6+}	6	–	–	1.0	3.0	4.5	–	–	ns	–	–	13	6	12	4,5
	t_{13+6-}	6	–	–	1.0	3.0	↓	–	–	↓	–	–	13	6	↓	↓
Rise Time (20 to 80%)	t_{6+7+}	6,7	–	–	1.1	2.0	↓	–	–	↓	–	–	13	6,7	↓	↓
Fall Time (20 to 80%)	t_{6-7-}	6,7	–	–	1.1	2.0	↓	–	–	↓	–	–	13	6,7	↓	↓
Set Input Propagation Delay	t_{9+6+}	6	–	–	1.0	3.0	5.0	–	–	ns	–	–	9	6	12	4,5
	t_{16+3+}	3	–	–	↓	↓	↓	–	–	↓	–	–	16	3	↓	↓
	t_{9-7-}	7	–	–	↓	↓	↓	–	–	↓	–	–	9	7	↓	↓
	t_{16+2-}	2	–	–	↓	↓	↓	–	–	↓	–	–	16	2	↓	↓
Reset Input Propagation Delay	t_{8+6-}	6	–	–	1.0	3.0	5.0	–	–	ns	–	–	8	6	12	4,5
	t_{8+7+}	7	–	–	↓	↓	↓	–	–	↓	–	–	8	7	↓	↓
	t_{1+3-}	3	–	–	↓	↓	↓	–	–	↓	–	–	1	3	↓	↓
	t_{1+2+}	2	–	–	↓	↓	↓	–	–	↓	–	–	1	2	↓	↓
Setup Time	t_{setup}	11	–	–	1.5	–	–	–	–	ns	–	–	10,13 ⑤	6	12	4,5
Hold Time	t_{hold}	11	–	–	2.5	–	–	–	–	ns	–	–	10,13 ⑤	6	12	4,5
Toggle Frequency	f_{Tog}	6	–	–	125	140	–	–	–	MHz	–	–	13	6	12	4,5

NOTES:

① Individually test each input; apply $V_{IH\ max}$ to pin under test.

② Individually test each input; apply $V_{IL\ min}$ to pin under test.

③ Output level to be measured after a clock pulse has been applied to the C input (pin 9)

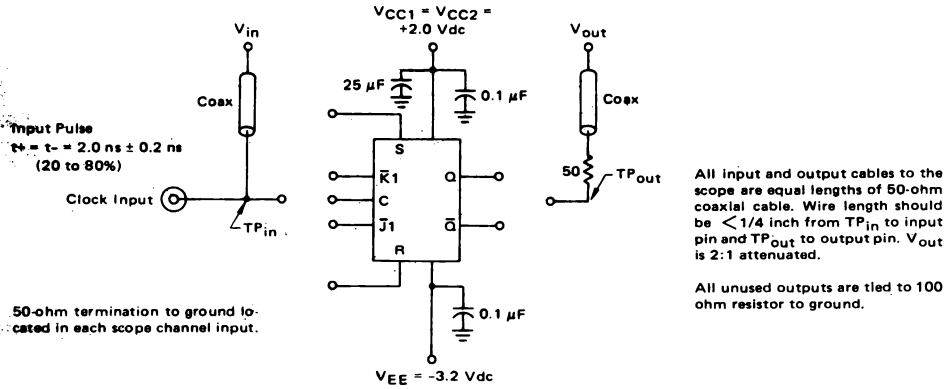
④ Output level to be measured after a clock pulse has been applied to the C input (pin 9)

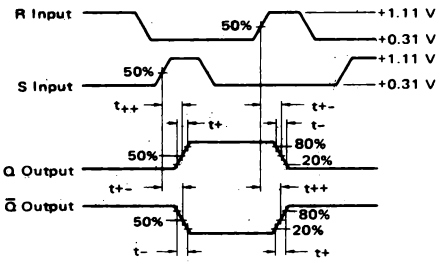
⑤ See Figure 2 for timing test diagram.

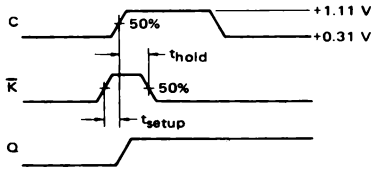
$V_{IH\ max}$ / $V_{IL\ min}$

$V_{IHA\ min}$ / $V_{ILA\ max}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C







NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the inputs $\overline{J}$ or $\overline{K}$.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the inputs $\overline{J}$ or $\overline{K}$.

UNIVERSAL HEXADECIMAL COUNTER

MC10536

The MC10536 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. This binary counter is useful in high speed central processors and peripheral controllers, minicomputers, high speed digital communications equipment and instrumentation. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10536 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

When an output is not needed, it can be left open to conserve system power. (The open emitter output will require no power if left open). The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock.

This device is not designed for use with gated clocks. Control is via S1 and S2.

A prescaler can be constructed using the MC10536 in conjunction with the MC10631 which will operate at over 200 MHz input frequency. A 500 MHz prescaler is possible using an MC1690 500 MHz D Flip-Flop, an MC1670 300 MHz D Flip-Flop, and the MC10536.

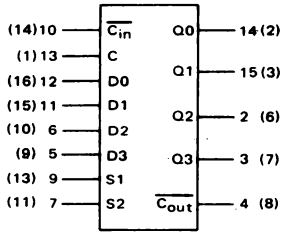
SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	H

ϕ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.



FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ

Numbers at ends of terminals denote pin numbers for L package (Case 620).

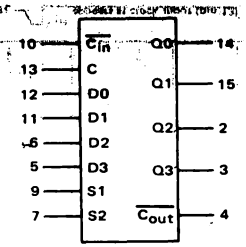
Numbers in parenthesis denote pin numbers for F package (Case 650).

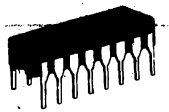
Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

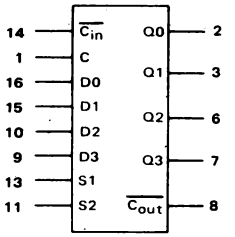
● Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

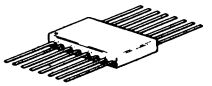
Characteristic	Symbol	Pin Under Test	MC10536L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	165	–	120	150	–	165	mAdc	–	–	–	–	8	1, 16
Input Current	$I_{in\ H}$	5,6,11,12	–	375	–	–	220	–	220	µAdc	5,6,11,12	–	–	–	8	1, 16
		7	–	450	–	–	265	–	265		7	–	–	–		
		9,10	–	415	–	–	245	–	245		9,10	–	–	–		
		13	–	495	–	–	290	–	290		13	–	–	–		
	$I_{in\ L}$	All	0.5	–	0.5	–	–	0.3	–	µAdc	–	①	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	14 ②	-1.080	-0.890	-0.930	–	-0.780	-0.825	-0.630	Vdc	12	7, 9	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	14 ②	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	7, 9	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	14 ②	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	7, 9	12	–	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	14 ②	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	7, 9	–	12	8	1, 16
Switching Times (100-ohm Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Input	t_{13+14+}	14	0.8	4.6	1.0	3.3	4.5	1.4	5.2	ns	12	–	13	14	8	1, 16
	t_{13+14-}	14	0.8	4.6	1.0	3.3	4.5	1.4	5.2		–	–		14		
	t_{13+4+}	4	2.0	11.0	2.5	7.0	10.5	2.4	12.6		7	–		4		
	t_{13+4-}	4	2.0	11.0	2.5	7.0	10.5	2.4	12.6		7	–				
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$	t_{10-4-}	4 ③	1.6	7.1	1.6	5.0	6.9	1.9	7.6		7	13	10			
	t_{10+4+}	4	1.6	7.1	1.6	5.0	6.9	1.9	7.6		7	13	10			
Set Up Time																
Data Inputs	t_{12+13+}	14	–	–	3.5	–	–	–	–		–	7, 9	12, 13	14		
	t_{12-13+}	14	–	–	3.5	–	–	–	–		–	7, 9	12, 13			
Select Inputs	t_{9+13+}	14	–	–	7.5	–	–	–	–		–	–	9, 13			
	t_{7+13+}	14	–	–	7.5	–	–	–	–		–	–	7, 13			
$\overline{\text{Carry In}}$ Input	t_{10-13+}	14	–	–	3.7	–	–	–	–		7	9	10, 13			
	t_{13+10+}	14	–	–	-1.0	–	–	–	–		7	9	10, 13			
Hold Time																
Data Inputs	t_{13+12+}	14	–	–	-1.0	–	–	–	–		–	7, 9	12, 13			
	t_{13+12-}	14	–	–	-1.0	–	–	–	–		–	7, 9	12, 13			
Select Inputs	t_{13+9+}	14	–	–	-2.5	–	–	–	–		–	–	9, 13			
	t_{13+7+}	14	–	–	-2.5	–	–	–	–		–	–	7, 13			
$\overline{\text{Carry In}}$ Input	t_{13+10-}	14	–	–	-1.6	–	–	–	–		7	9	10, 13			
	t_{10+13+}	14	–	–	3.1	–	–	–	–		7	9	10, 13			
Counting Frequency	$f_{countup}$	4	115	–	125	150	–	115	–	MHz	7	–	13			
	$f_{countdown}$	4	115	–	125	150	–	115	–	MHz	9	–				
Rise Time (20% to 80%)	t_{4+}	4	0.9	3.3	1.1	2.0	3.3	1.2	3.7	ns	7	–		4		
	t_{14+}	14										–		14		
Fall Time (20% to 80%)	t_{4-}	4										–		4		
	t_{14-}	14										–		14		

① Individually apply $V_{IL\ min}$ to pin under test. ② Measure output after clock pulse V_{IL} ⌐ V_{IH} appears at clock input (pin 13) ③ Before test set all Q outputs to a logic high.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

● Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10536F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	165	–	120	150	–	165	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\ H}$	9,10,15,16	–	365	–	–	215	–	215	μAdc	9,10,15,16	–	–	–	12	4,5
		11	–	445	–	–	260	–	260		11	–	–	–		
		13,14	–	410	–	–	240	–	240		13,14	–	–	–		
		1	–	485	–	–	285	–	285		1	–	–	–		
	$I_{in\ L}$	All	0.5	–	0.5	–	–	0.3	–	μAdc	–	①	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	2 ②	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	16	11,13	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	2 ②	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	11,13	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	2 ②	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	11,13	16	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	2 ②	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	11,13	–	16	12	4,5
Switching Times (100-ohm Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Input	t_{1+2+}	2	–	–	1.0	3.3	4.5	–	–	ns	16	–	1	2	12	4,5
	t_{1+2-}	2	–	–	1.0	3.3	4.5	–	–		–	–		2		
	t_{1+8+}	8	–	–	2.5	7.0	10.5	–	–		11	–		8		
	t_{1+8-}	8	–	–	2.5	7.0	10.5	–	–		11	–				
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$	t_{14-8-}	8 ③	–	–	1.6	5.0	6.9	–	–		11	1	14			
	t_{14+8+}	8	–	–	1.6	5.0	6.9	–	–		11	1	14			
Set Up Time																
Data Inputs	t_{16+1+}	2	–	–	3.5	–	–	–	–		–	11,13	1,16	2		
	t_{16-1+}	2	–	–	3.5	–	–	–	–		–	11,13	1,16			
Select Inputs	t_{13+1+}	2	–	–	7.5	–	–	–	–		–	–	1,13			
	t_{11+1+}	2	–	–	7.5	–	–	–	–		–	–	1,11			
$\overline{\text{Carry In}}$ Input	t_{14-1+}	2	–	–	3.7	–	–	–	–		11	13	1,14			
	t_{14+14+}	2	–	–	-1.0	–	–	–	–		11	13	1,14			
Hold Time																
Data Inputs	t_{1+16+}	2	–	–	-1.0	–	–	–	–		–	11,13	1,16			
	t_{1+16-}	2	–	–	-1.0	–	–	–	–		–	11,13	1,16			
Select Inputs	t_{1+13+}	2	–	–	-2.5	–	–	–	–		–	–	1,13			
	t_{1+11-}	2	–	–	-2.5	–	–	–	–		–	–	1,11			
$\overline{\text{Carry In}}$ Input	t_{1+14-}	2	–	–	-1.6	–	–	–	–		11	13	1,14			
	t_{14+1+}	2	–	–	3.1	–	–	–	–		11	13	1,14			
Counting Frequency	$f_{countup}$	8	–	–	125	150	–	–	–	MHz	11	–	1			
	$f_{countdown}$	8	–	–	125	150	–	–	–	MHz	13	–				
Rise Time (20% to 80%)	t_{8+}	8	–	–	1.1	2.0	3.3	–	–	ns	11	–		8		
	t_{2+}	2	–	–				–	–			–		2		
Fall Time (80% to 20%)	t_{8-}	8	–	–				–	–			–		8		
	t_{2-}	2	–	–				–	–			–		2		

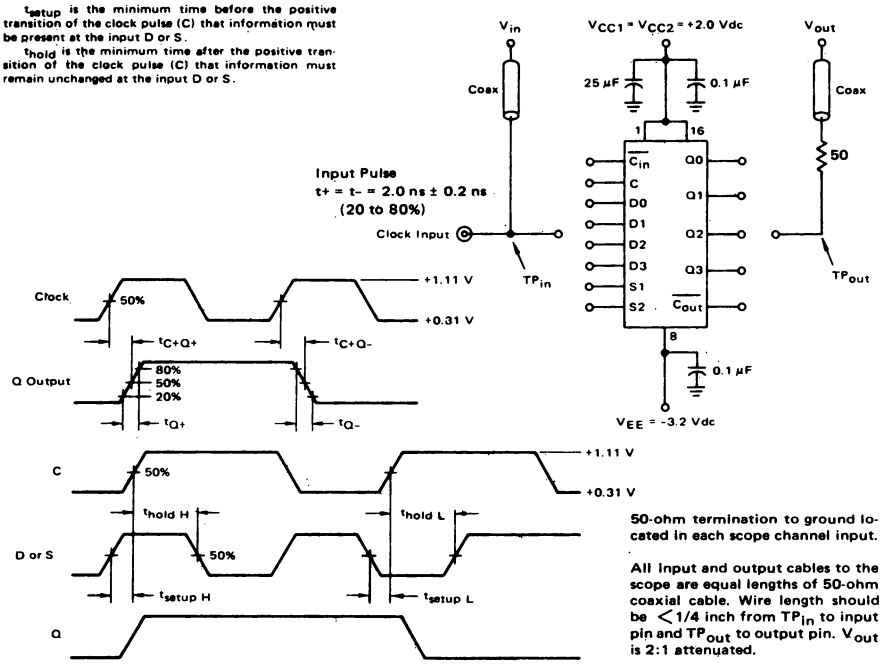
① Individually apply $V_{IL\ min}$ to pin under test. ② Measure output after clock pulse V_{IL} ⎍ V_{IH} appears at clock input (pin 13). ③ Before test set all Q outputs to a logic high.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<$1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

Unused outputs are connected to a 100-ohm resistor to ground.

SET UP AND HOLD TIMES

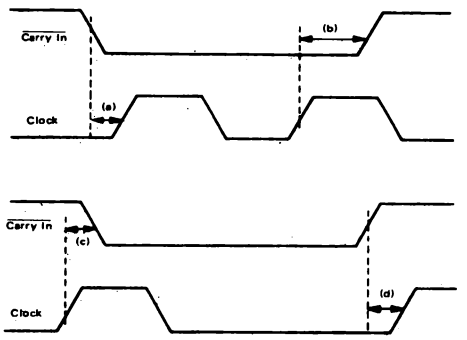
(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

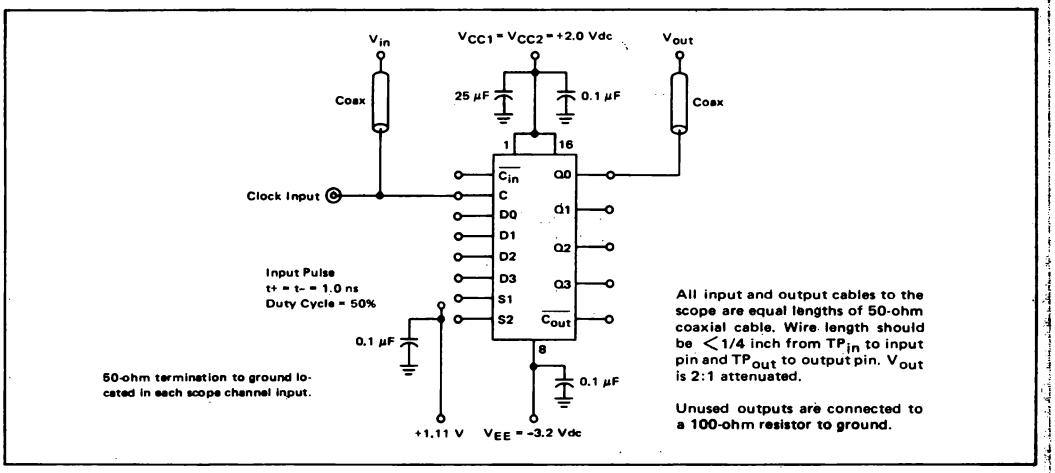
(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

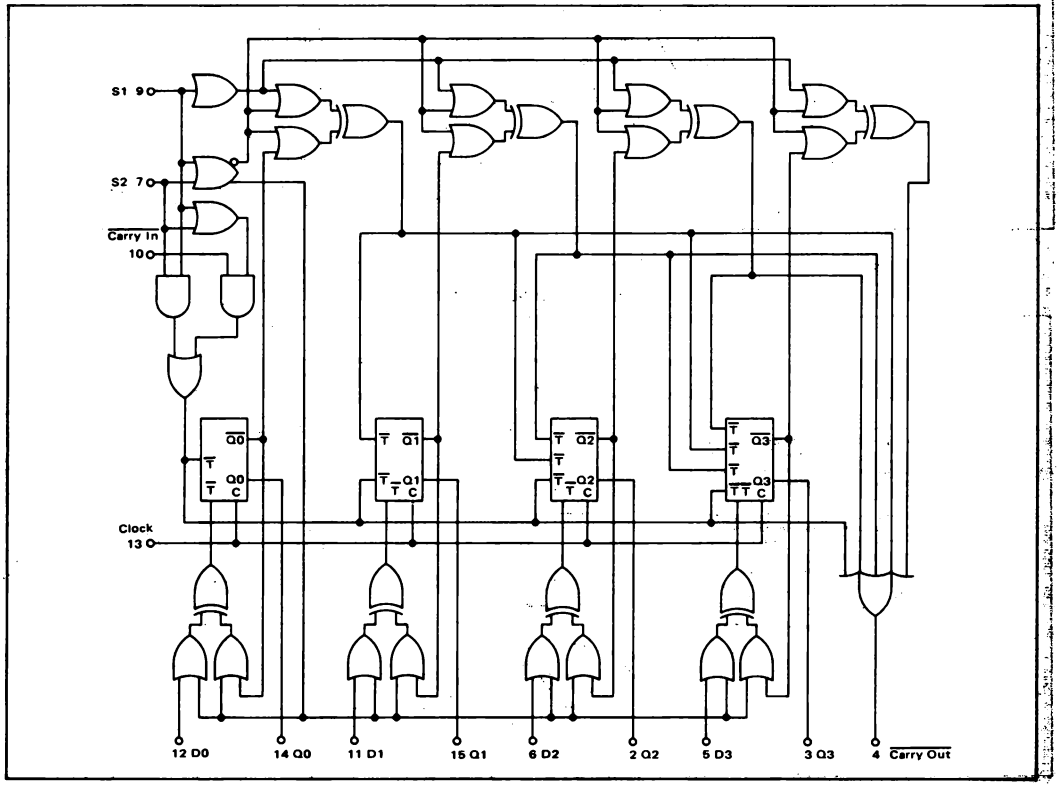
(b) and (c) may be negative numbers



COUNT FREQUENCY TEST CIRCUIT



UNIVERSAL BINARY UP/DOWN COUNTER



APPLICATIONS INFORMATION

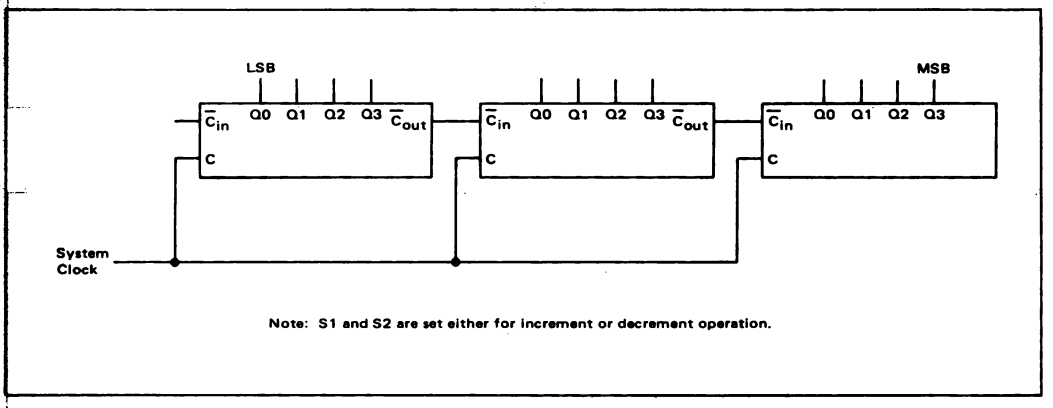
To provide more than four bits of counting capability several MC10536 counters may be cascaded. The Carry In input overrides the clock when the counter is either in the increment mode or the decrement mode of operation. This input allows several devices to be cascaded in a fully synchronous multistage counter as illustrated in Figure 1. The carry is advanced between stages as shown with no external gating. The $\overline{\text{Carry In}}$ of the first device may be left open. The system clock is common to all devices.

The various operational modes of the counter make it useful for a wide variety of applications. If used with MECL III devices, prescalers with input toggle frequencies in excess of 300 MHz are possible. Figure 2 shows such a prescaler using the MC10536 and MC1670. Use of the MC10631 in place of the MC1670 permits 200 MHz operation.

The MC10536 may also be used as a programmable counter. The configuration of Figure 3 requires no additional gates, although maximum frequency is limited to about 50 MHz. The divider modulus is equal to the program input plus one (M = N + 1), therefore, the counter will divide by a modulus varying from 1 to 16.

A second programmable configuration is also illustrated in Figure 4. A pulse swallowing technique is used to speed the counter operation up to 110 MHz typically. The divider modulus for this figure is equal to the program input (M = N). The minimum modulus is 2 because of the pulse swallowing technique, and the modulus may vary from 2 to 15. This programmable configuration requires an additional gate, such as ½MC10509 and a flip-flop such as ½MC10531.

FIGURE 1 – 12 BIT SYNCHRONOUS COUNTER



Note: S1 and S2 are set either for increment or decrement operation.

FIGURE 2 – 300 MHz PRESCALER

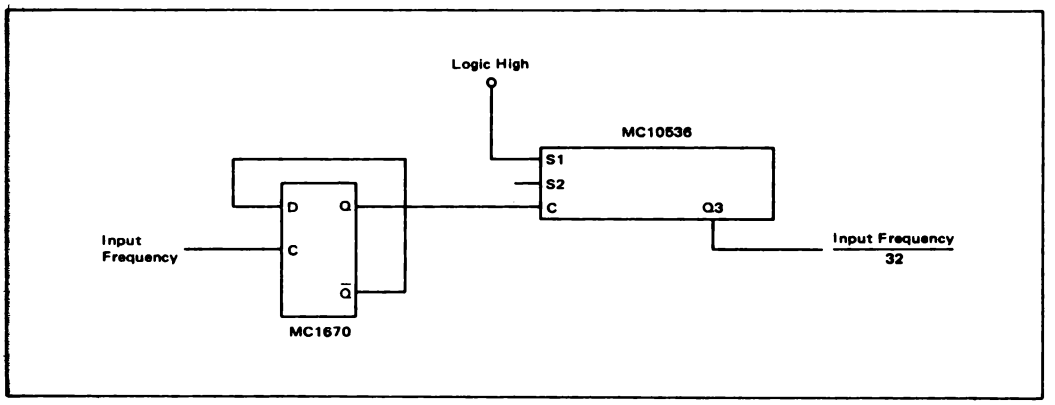
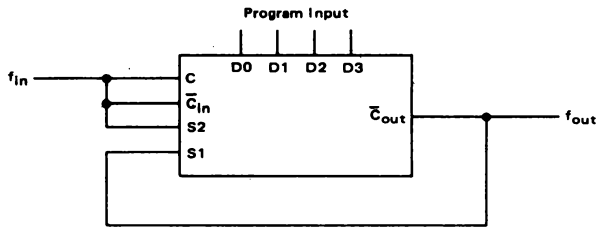


FIGURE 3 – 50 MHz PROGRAMMABLE COUNTER

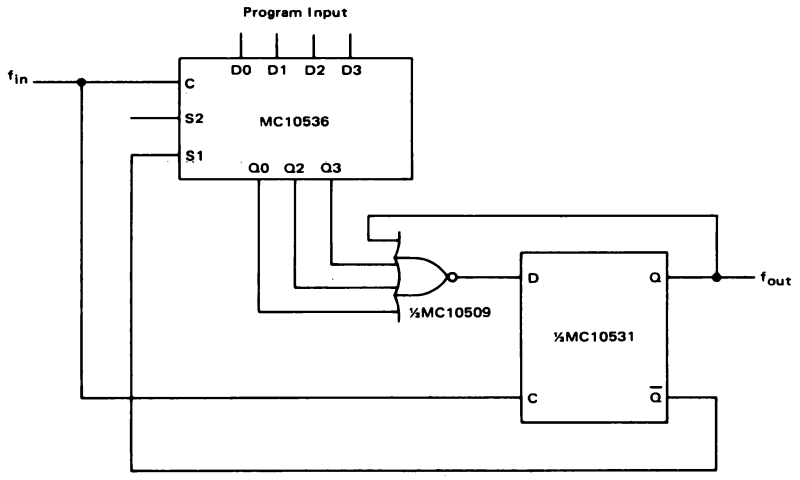


1 $f_{out} = \frac{f_{in}}{\text{Program Input} + 1}$

2 $f_{max} \cong 50$ MHz Typ.

3 Divide Ratio is from 1 to 16.

FIGURE 4 – 100 MHz PROGRAMMABLE COUNTER



1 $f_{out} = \frac{f_{in}}{\text{Program Input}}$

2 $f_{max} \cong 110$ MHz Typ.

3 Divide Ratio is from 2 to 15.

UNIVERSAL DECADE COUNTER

MC10537

The MC10537 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. This decade counter is useful in high speed central processors and peripheral controllers, minicomputers, high speed digital communications equipment and instrumentation. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10537 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count. The $\overline{\text{Carry Out}}$ on the MC10537 is partially decoded from Q1 and Q2 directly, so in the preset mode the condition of the $\overline{\text{Carry Out}}$ after the Clock's positive excursion will depend on the condition of Q1 and/or Q2.

When an output is not needed, it can be left open to conserve system power. (The open emitter output will require no power if left open.) The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.

A prescaler can be constructed using the MC10537 in conjunction with the MC10631 which will operate at over 200 MHz input freuqency. A 500 MHz prescaler is possible using an MC1690 500 MHz D Flip-Flop, an MC1670 300 MHz D Flip-Flop, and the MC10537.

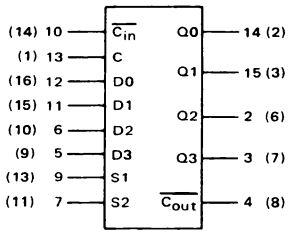
SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	ϕ	H	H	H	H	L	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	L	L	L	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	L	L	L	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L

ϕ = Don't care.

*Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.



Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

FUNCTION SELECT TABLE

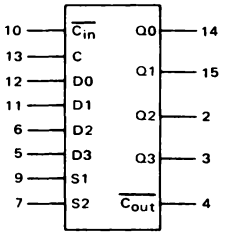
S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

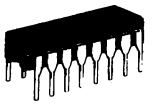
P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





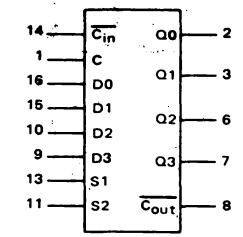
L SUFFIX
CERAMIC PACKAGE
CASE 620

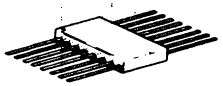
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10637L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	165	–	120	150	–	165	mAdc	–	–	–	–	8	1, 16
Input Current	$I_{in\ H}$	5,6,11,12	–	375	–	–	220	–	220	µAdc	5,6,11,12	–	–	–	8	1, 16
		7	–	450	–	–	265	–	265		7	–	–	–		
		9,10	–	415	–	–	245	–	245		9,10	–	–	–		
		13	–	495	–	–	290	–	290		13	–	–	–		
	$I_{in\ L}$	All	0.5	–	0.5	–	–	0.3	–	µAdc	–	①	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	14 ②	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	12	7, 9	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	14 ②	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	7, 9	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	14 ②	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	7, 9	12	–	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	14 ②	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	7, 9	–	12	8	1, 16
Switching Times (100-ohm Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Input	t_{13+14+}	14	0.8	4.6	1.0	3.3	4.5	1.4	5.2	ns	12	–	13	14	8	1, 16
	t_{13+14-}	14	0.8	4.6	1.0	3.3	4.5	1.4	5.2		–	–		14		
	t_{13+4+}	4	2.0	11	2.5	7.0	10.5	2.4	12.6		7	–		4		
	t_{13+4-}	4	2.0	11	2.5	7.0	10.5	2.4	12.6		7	–		4		
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$	t_{10-4-}	4 ③	1.6	7.1	1.6	5.0	6.9	1.9	7.6		7	13	10	4		
	t_{10+4+}	4 ③	1.6	7.1	1.6	5.0	6.9	1.9	7.6		7	13	10	4		
Set Up Time																
Data Inputs	t_{12+13+}	14	–	–	3.5	–	–		–		–	7, 9	12, 13	14		
	t_{12-13+}	14	–	–	3.5	–	–		–		–	7, 9	12, 13			
Select Inputs	t_{9+13+}	14	–	–	7.5	–	–	–	–		–	–	9, 13			
	t_{7+13+}	14	–	–	7.5	–	–	–	–		–	–	7, 13			
$\overline{\text{Carry In}}$ Input	t_{10-13+}	14	–	–	3.7	–	–	–	–		7	9	10, 13			
	t_{13+10+}	14	–	–	-1.0	–	–	–	–		7	–	10, 13			
Hold Time																
Data Inputs	t_{13+12+}	14	–	–	-1.0	–	–	–	–		–	7, 9	12, 13			
	t_{13+12-}	14	–	–	-1.0	–	–	–	–		–	7, 9	12, 13			
Select Inputs	t_{13+9+}	14	–	–	-2.5	–	–	–	–		–	–	9, 13			
	t_{13+7+}	14	–	–	-2.5	–	–	–	–		–	–	7, 13			
$\overline{\text{Carry In}}$ Input	t_{13+10-}	14	–	–	-1.6	–	–	–	–		7	9	10, 13			
	t_{10+13+}	14	–	–	3.1	–	–	–	–		7	9	10, 13			
Counting Frequency	$f_{countup}$	4	115	–	125	150	–	115	–	MHz	7	–	13			
	$f_{countdown}$	4	115	–	125	150	–	115	–	MHz	9	–				
Rise Time (20% to 80%)	t_{4+}	4	0.9	3.3	1.1	2.0	3.3	1.2	3.7	ns	7	–		4		
	t_{14+}	14										–		14		
Fall Time (20% to 80%)	t_{4-}	4										–		4		
	t_{14-}	14										–		14		

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





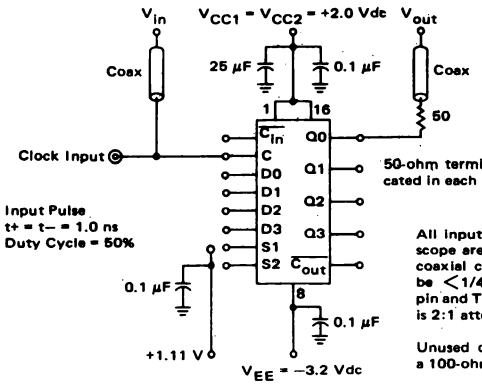
F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−55°C	−0.880	−1.920	−1.255	−1.510	−5.2
+25°C	−0.780	−1.850	−1.105	−1.475	−5.2
+125°C	−0.830	−1.820	−1.000	−1.400	−5.2

Characteristic	Symbol	Pin Under Test	MC10537F Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	165	–	120	150	–	165	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\ H}$	9,10,15,16	–	375	–	–	220	–	220	μAdc	9,10,15,16	–	–	–	12	4,5
		11	–	450	–	–	265	–	265		11	–	–	–		
		13,14	–	415	–	–	245	–	245		13,14	–	–	–		
		1	–	495	–	–	290	–	290		1	–	–	–		
	$I_{in\ L}$	All	0.5	–	0.5	–	–	0.3	–	μAdc	–	①	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	2 ②	−1.080	−0.880	−0.930	–	−0.780	−0.825	−0.630	Vdc	16	11,13	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	2 ②	−1.920	−1.655	−1.850	–	−1.620	−1.820	−1.545	Vdc	–	11,13	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	2 ②	−1.100	–	−0.950	–	–	−0.845	–	Vdc	–	11,13	16	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	2 ②	–	−1.635	–	–	−1.600	–	−1.525	Vdc	–	11,13	–	18	12	4,5
Switching Times (100-ohm Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay																
Clock Input	t_{1+2+}	2	–	–	1.0	3.3	4.5	–	–	ns	16	–	1	2	12	4,5
	t_{1+2-}	2	–	–	1.0	3.3	4.5	–	–		–	–		2		
	t_{1+8+}	8	–	–	2.5	7.0	10.5	–	–		11	–		8		
	t_{1+8-}	8	–	–	2.5	7.0	10.5	–	–		11	–				
$\overline{CI}$ To $\overline{CO}$	t_{14-8-}	8 ③	–	–	1.6	5.0	6.9	–	–		11	1	14			
	t_{14+8+}	8 ③	–	–	1.6	5.0	6.9	–	–		11	1	14			
Set Up Time																
Data Inputs	t_{16+1+}	2	–	–	3.5	–	–	–	–		–	11,13	1,16	2		
	t_{16-1+}	2	–	–	3.5	–	–	–	–		–	11,13	1,16			
Select Inputs	t_{13+1+}	2	–	–	7.5	–	–	–	–		–	–	1,13			
	t_{11+1+}	2	–	–	7.5	–	–	–	–		–	–	1,11			
$\overline{CI}$ Input	t_{14-1+}	2	–	–	3.7	–	–	–	–		11	13	1,14			
	t_{1+14+}	2	–	–	−1.0	–	–	–	–		11	–	1,14			
Hold Time																
Data Inputs	t_{1+16+}	2	–	–	−1.0	–	–	–	–		–	11,13	1,16			
	t_{1+16-}	2	–	–	−1.0	–	–	–	–		–	11,13	1,16			
Select Inputs	t_{1+13+}	2	–	–	−2.5	–	–	–	–		–	–	1,13			
	t_{1+11+}	2	–	–	−2.5	–	–	–	–		–	–	1,11			
$\overline{CI}$ Input	t_{1+14-}	2	–	–	−1.6	–	–	–	–		11	13	1,14			
	t_{14+1+}	2	–	–	3.1	–	–	–	–		11	13	1,14			
Counting Frequency	$f_{countup}$	8	–	–	125	150	–	–	–	MHz	11	–	1			
	$f_{countdown}$	8	–	–	125	150	–	–	–	MHz	13	–				
Rise Time (20% to 80%)	t_{8+}	8	–	–	1.1	2.0	3.3	–	–	ns	11	–		8		
	t_{2+}	2	–	–				–	–			–		2		
Fall Time (20% to 80%)	t_{8-}	8	–	–				–	–			–		8		
	t_{2-}	2	–	–				–	–			–		2		

① Individually apply $V_{IL\ min}$ to pin under test. ② Measure output after clock pulse V_{IL} ⌐ V_{IH} appears at clock input (pin 1) ③ Before test counter must be set to a zero count condition (all outputs low)

COUNT FREQUENCY TEST CIRCUIT



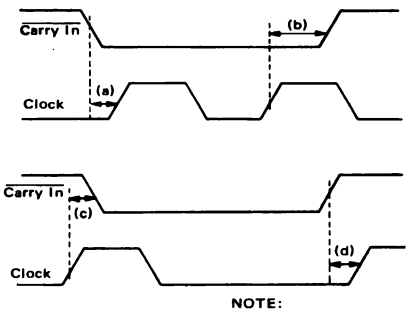
Input Pulse
$t_+ = t_- = 1.0$ ns
Duty Cycle = 50%

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

Unused outputs are connected to a 100-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter hasbeen disabled that it may be clocked.

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

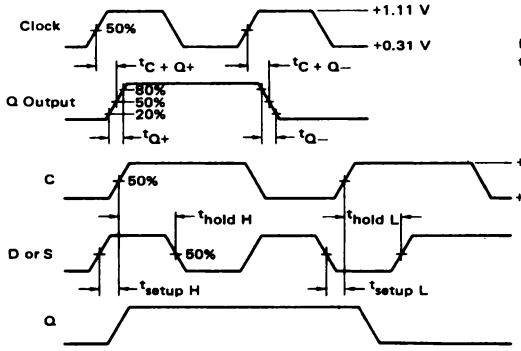
(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

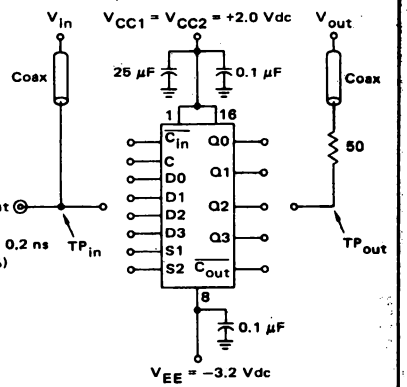
(b) and (c) may be negative numbers.

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.





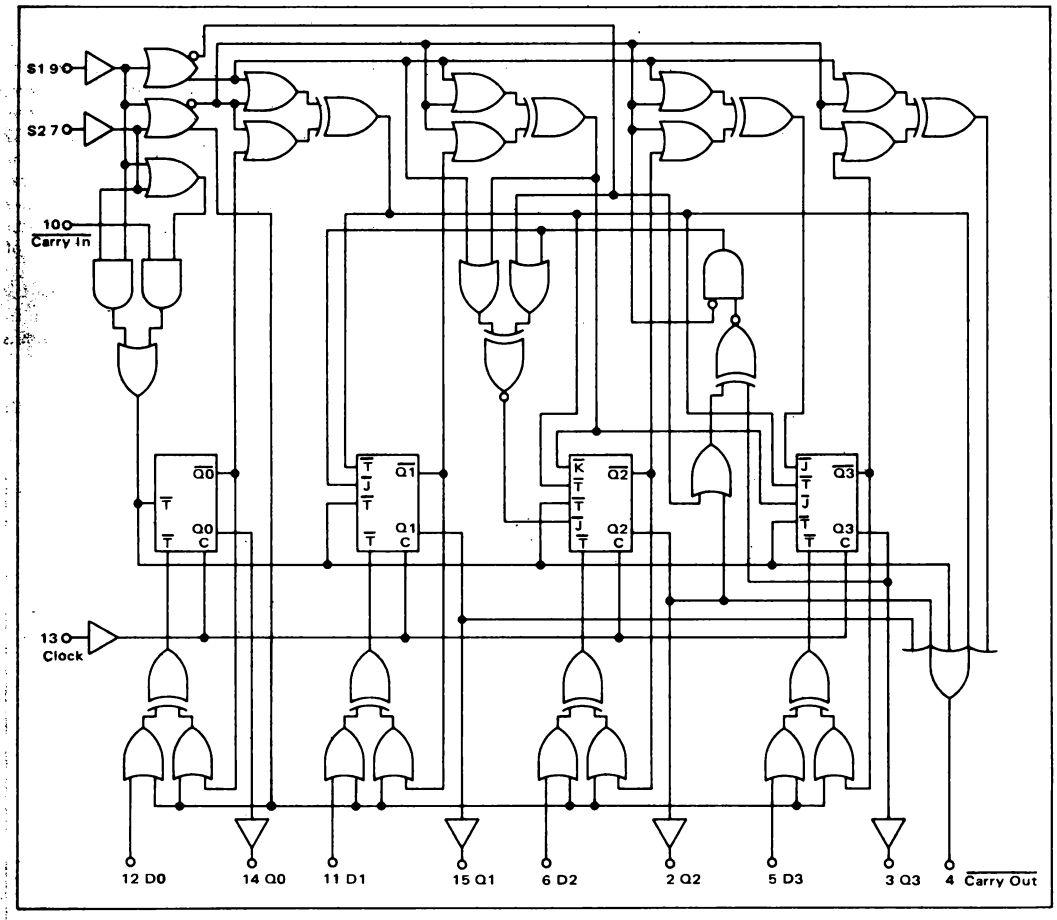
Input Pulse
$t_+ = t_- = 2.0 \pm 0.2$ ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

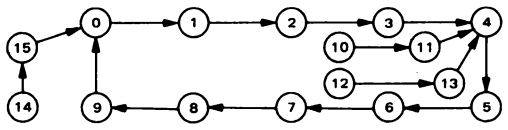
Unused outputs are connected to a 100-ohm resistor to ground.

UNIVERSAL DECADE UP/DOWN COUNTER

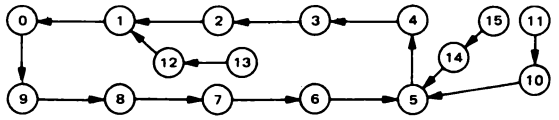


STATE DIAGRAMS

COUNT UP

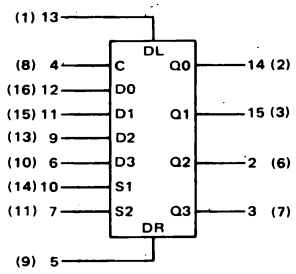


COUNT DOWN



FOUR-BIT UNIVERSAL
SHIFT REGISTER

MC10541



The MC10541 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR). All four outputs are capable of driving 100 ohm lines.

When the register is used for serial output only, the unused emitter follower outputs can be left open.

TRUTH TABLE

SELECT			OUTPUTS			
S1	S2	OPERATING MODE	$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

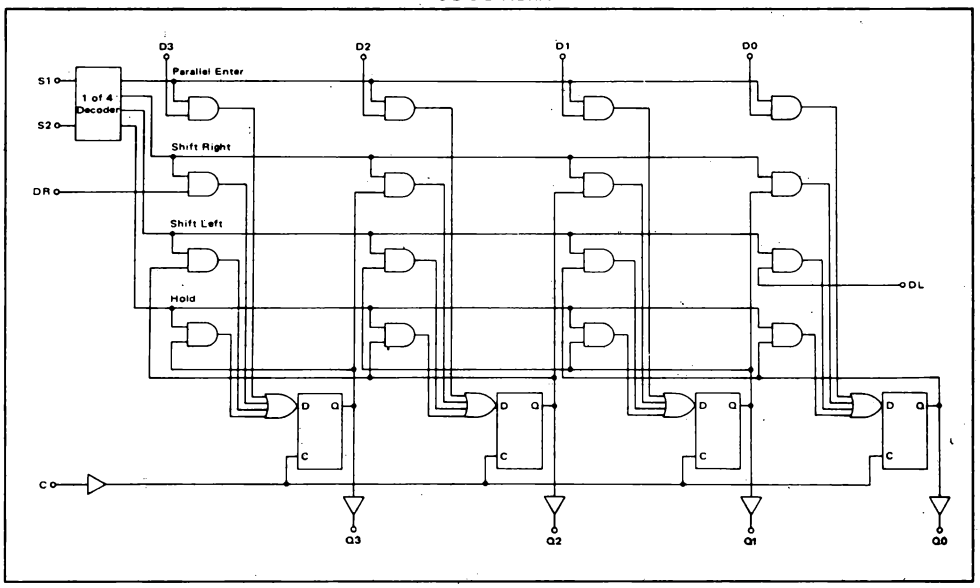
*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).

P_D = 425 mW typ/pkg (No Load)
f_{Shift} = 150 MHz typ

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

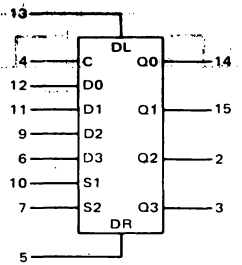
LOGIC DIAGRAM



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

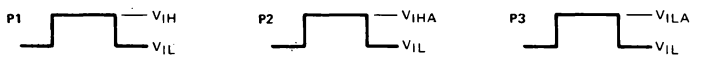
Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.



L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

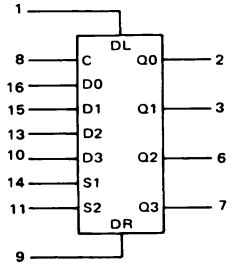
Characteristic	Symbol	Pin Under Test	MC10541L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	P1	P2	P3	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	110	–	–	100	–	110	mAdc	–	–	–	–	8	–	–	–	1,16
Input Current	I_{inH}	5	–	375	–	–	220	–	220	μAdc	5	–	–	–	8	–	–	–	1,16
		6	–	375	–	–	220	–	220		6	–	–	–		–	–	–	
		7	–	415	–	–	245	–	245		7	–	–	–		–	–	–	
		4	–	450	–	–	265	–	265		4	–	–	–		–	–	–	
	I_{inL}	12	0.5	–	0.5	–	–	0.3	–	μAdc	4,5,6,7,9, 10,11,13	12	–	–	8	–	–	–	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	6	–	–	–	8	4	–	–	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	8	4	–	–	1,16
Logic "1" Threshold Voltage	V_{OHA} ①	3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	6	–	8	4	–	–	1,16
				–		–	–		–		6	④	–	7		4	–	–	
				–		–	–		–		6	④	–	–		–	4	–	
				–		–	–		–		–	–	–	–		–	–	4	
Logic "0" Threshold Voltage	V_{OLA} ①	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	6	8	4	–	–	1,16
			–		–	–		–			–	⑤	–	7		4	–	–	
			–		–	–		–			–	⑤	–	–		–	4	–	
			–		–	–		–			6	–	–	–		–	–	4	
Switching Times (100 Ω Load)															-3.2 V				+2.0 V
Propagation Delay	t_{4+3+}	3	–	–	1.0	2.9	3.8	–	–	ns	②	–	–	–	8	–	–	–	1,16
Setup Time (t_{setup})	t_{12+4+}	14	–	–	2.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{12-4+}		–	–	2.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{10+4+}		–	–	5.0	–	–	–	–		–	–	–	–		–	–	–	
	t_{10-4+}		–	–	5.0	–	–	–	–		–	–	–	–		–	–	–	
Hold Time (t_{hold})	t_{4+12+}		–	–	1.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{4+12-}		–	–	1.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{4+10+}		–	–	1.0	–	–	–	–		–	–	–	–		–	–	–	
	t_{4+10-}		–	–	1.0	–	–	–	–		–	–	–	–		–	–	–	
Rise Time (20% to 80%)	t_{3+}	3	–	–	1.1	1.7	3.3	–	–		②	–	–	–		–	–	–	
Fall Time (20% to 80%)	t_{3-}	3	–	–	1.1	1.7	3.3	–	–		②	–	–	–		–	–	–	
Shift Frequency	f_{Shift}	–	–	–	150	–	–	–	–	MHz	③	–	–	–		–	–	–	

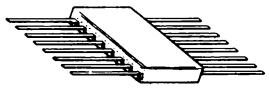


① These tests to be performed in sequence as shown.
② See switching time test circuit for test procedures.
③ See shift frequency test circuit for test procedures.
④ Reset to zero before performing test.
⑤ Reset to one before performing test.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





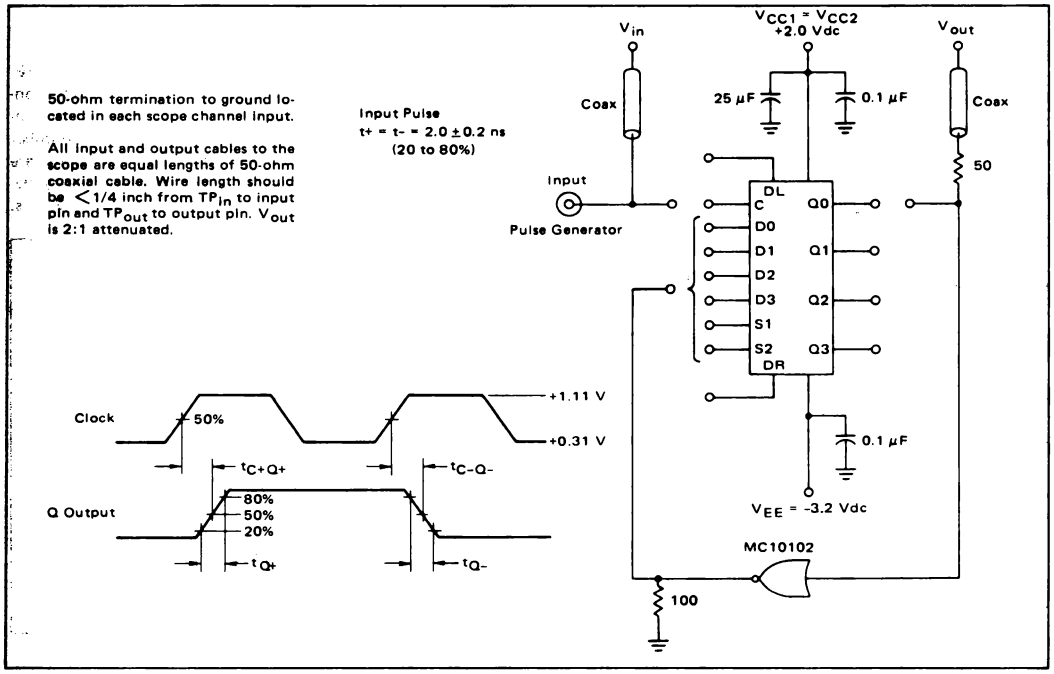
F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

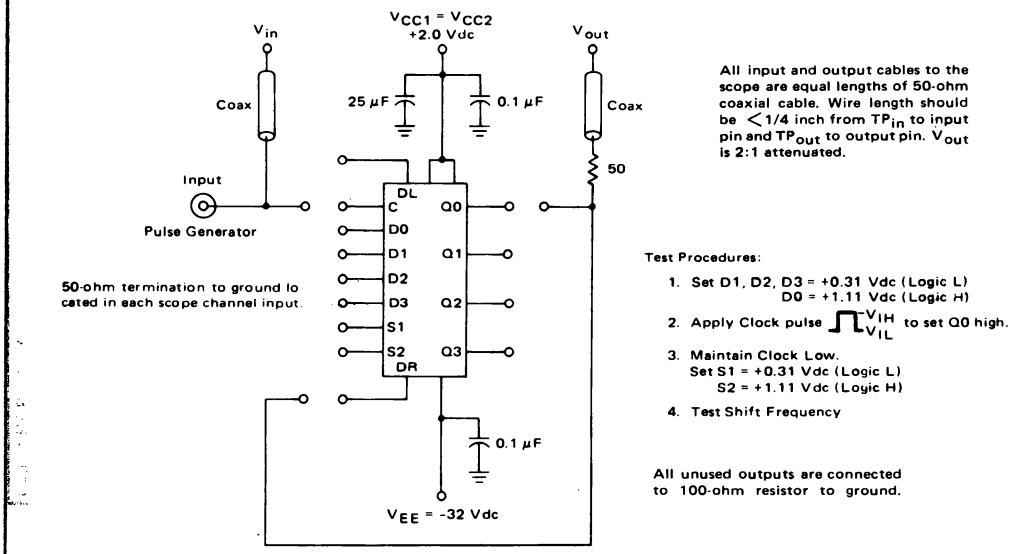
Characteristic	Symbol	Pin Under Test	MC10541F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	P1	P2	P3	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	110	–	–	100	–	110	mAdc	–	–	–	–	12	–	–	–	4,5
Input Current	I_{inH}	9	–	365	–	–	220	–	220	µAdc	9	–	–	–	12	–	–	–	4,5
		10	–	365	–	–	220	–	220		10	–	–	–		–	–	–	
		11	–	420	–	–	245	–	245		11	–	–	–		–	–	–	
		8	–	455	–	–	265	–	265		8	–	–	–		–	–	–	
	I_{inL}	16	0.5	–	0.5	–	–	0.3	–	µAdc	8,9,10,11, 13,14,15,1	16	–	–	12	–	–	–	4,5
Logic "1" Output Voltage	V_{OH}	7	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	10	–	–	–	12	8	–	–	4,5
Logic "0" Output Voltage	V_{OL}	7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	12	8	–	–	4,5
Logic "1" Threshold Voltage	V_{OHA} ①	7	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	10	–	12	8	–	–	4,5
				–		–	–		–		10	④	–	11		8	–	–	
				–		–	–		–		10	④	–	–		–	8	–	
				–		–	–		–		–	–	–	–		–	–	8	
Logic "0" Threshold Voltage	V_{OLA} ①	7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	10	12	8	–	–	4,5
			–		–	–		–			–	⑤	–	11		8	–	–	
			–		–	–		–			–	⑤	–	–		–	8	–	
			–		–	–		–			10	–	–	–		–	–	8	
Switching Times (100 Ω Load)															-3.2 V				+2.0 V
Propagation Delay	t_{8+7+}	7	–	–	1.0	2.9	3.8	–	–	ns	②	–	–	–	12	–	–	–	4,5
Setup Time (t_{setup})	t_{16-8+}	2	–	–	2.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{16-8+}		–	–	2.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{14+8+}		–	–	5.0	–	–	–	–		–	–	–	–		–	–	–	
	t_{14-8+}		–	–	5.0	–	–	–	–		–	–	–	–		–	–	–	
Hold Time (t_{hold})	t_{8+16+}		–	–	1.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{8+16-}		–	–	1.5	–	–	–	–		–	–	–	–		–	–	–	
	t_{8+14+}		–	–	1.0	–	–	–	–		–	–	–	–		–	–	–	
	t_{8+14-}		–	–	1.0	–	–	–	–		–	–	–	–		–	–	–	
Rise Time (20% to 80%)	t_{7+}	7	–	–	1.1	1.7	3.3	–	–		②	–	–	–		–	–	–	
Fall Time (20% to 80%)	t_{7-}	7	–	–	1.1	1.7	3.3	–	–		②	–	–	–		–	–	–	
Shift Frequency	f_{Shift}	–	–	–	150	–	–	–	–	MHz	③	–	–	–		–	–	–	

① These tests to be performed in sequence as shown.
② See switching time test circuit for test procedures.
③ See shift frequency test circuit for test procedures.
④ Reset to zero before performing test.
⑤ Reset to one before performing test.

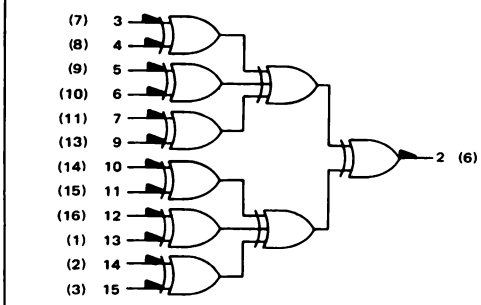
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



SHIFT FREQUENCY TEST CIRCUIT



MC10560



Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

The MC10560 consists of nine EXCLUSIVE-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2(6)
Even	Low
Odd	High

P_D = 320 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

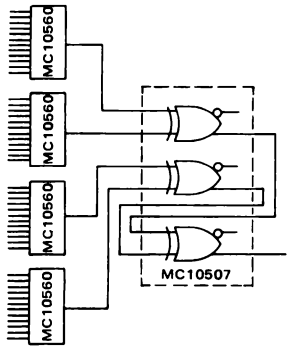
Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

APPLICATION INFORMATION

The MC10560 is useful in any system requiring high speed detection or generation of parity. The MC10560 can generate parity for twelve bits in four ns. A large number of functions on one chip reduces package count and saves system power. As shown in Figure 1, by using the MC10560's and one MC10507 parity can be checked or generated on 48 bits in 9.5 ns, or 7.5 ns if the MC10507 is replaced by a MECL III MC1672 or MC1674, although these MECL III parts are not guaranteed over the full temperature range.

If parity detection or generation is required for less than twelve bits, the unnecessary inputs can be left open. Input pulldown resistors will insure that the unused inputs are pulled to the low logic level.

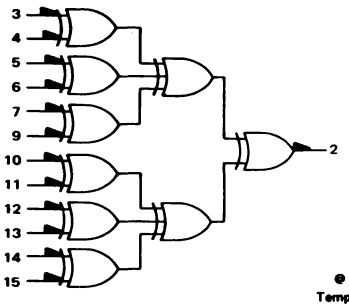
FIGURE 1 – 48-BIT PARITY CHECKER

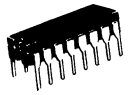


See General Information section for packaging and maximum ratings

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions.





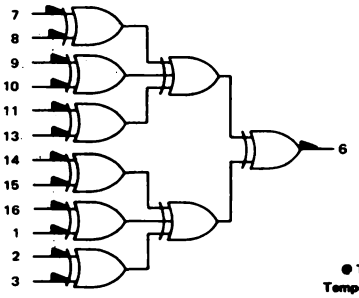
L SUFFIX
CERAMIC PACKAGE
CASE 620

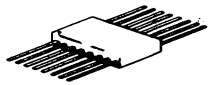
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10560L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	86	–	62	78	–	86	mAdc	4,5,9,10,13,14	–	–	–	8	1,16
Input Current	I_{inH}	3	–	450	–	–	265	–	265	µAdc	3	–	–	–	8	1,16
		4	–	375	–	–	220	–	220	µAdc	4	–	–	–	8	1,16
	I_{inL}	3	0.5	–	0.5	–	–	0.3	–	µAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	3	4,5,6,7,9,10, 11,12,13,14,15	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	3,4,5,6,7,9,10, 11,12,13,14,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	4,5,6,7,9,10,11, 12,13,14,15	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	3,5,6,7,9,10,11 12,13,14,15	–	4	8	1,16
Switching Times (100-ohm load) Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
	t_{3+2+}	2	1.6	7.5	2.0	4.0	7.5	1.4	7.5	ns	–	–	3	2	8	1,16
	t_{3+2-}										4	–				
	t_{3-2-}										–	–				
	t_{3-2+}										4	–				
	t_{4+2+}										–	–	4			
	t_{4+2-}										3	–				
	t_{4-2-}										–	–				
	t_{4-2+}										3	–				
Rise Time (20% to 80%)	t_{2+}		1.0	3.4	1.1	2.0	3.3	0.9	3.4		–	–	3			
Fall Time (20% to 80%)	t_{2-}		1.0	3.4	1.1	2.0	3.3	0.9	3.4		–	–	3			

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions.



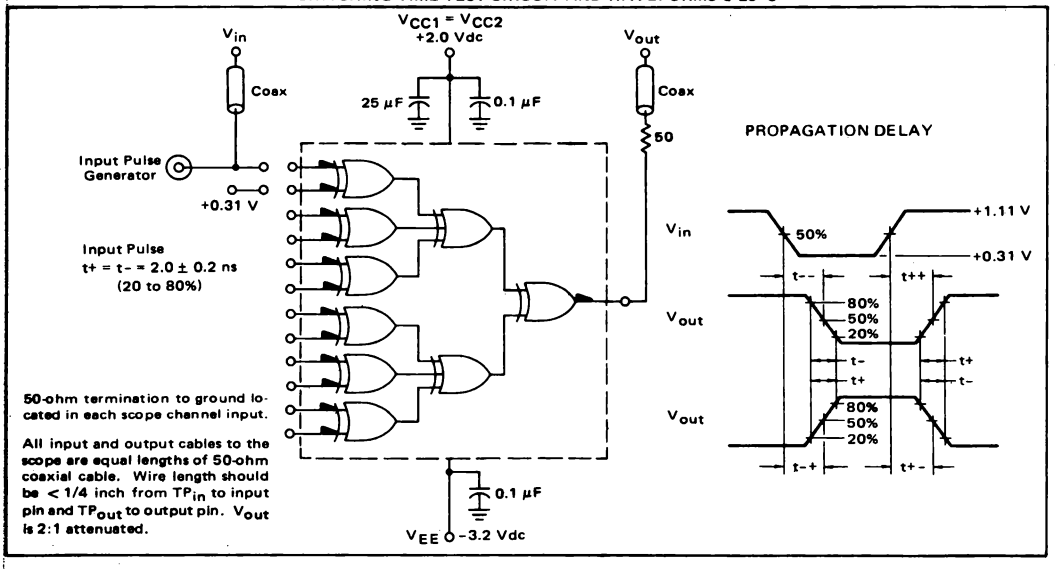


F SUFFIX
CERAMIC PACKAGE
CASE 650

● Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10560F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	86	–	62	78	–	86	mAdc	1,2,8,9,13,14	–	–	–	12	4,5
Input Current	I_{inH}	7	–	450	–	–	265	–	265	µAdc	7	–	–	–	12	4,5
		8	–	375	–	–	220	–	220	µAdc	8	–	–	–	12	4,5
	I_{inL}	7	0.5	–	0.5	–	–	0.3	–	µAdc	–	7	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	7	1,2,3,8,9,10, 11,13,14,15,16	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	1,2,3,7,8,9,10, 11,13,14,15,16	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	1,2,3,8,9,10, 11,13,14,15,16	7	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	1,2,3,7,9,10, 11,13,14,15,16	–	8	12	4,5
Switching Times (100-ohm load) Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
	t_{7+6+}	6	–	–	2.0	4.0	7.5	–	–	ns	–	–	7	6	12	4,5
	t_{7+6-}		–	–				–	–		8	–				
	t_{7-6-}		–	–				–	–		–	–				
	t_{7-6+}		–	–				–	–		8	–				
	t_{8+6+}		–	–				–	–		–	–	8			
	t_{8+6-}		–	–				–	–		7	–				
	t_{8-6-}		–	–				–	–		–	–				
	t_{8-6+}		–	–				–	–		7	–				
Rise Time (20% to 80%)	t_{6+}		–	–	1.1	2.0	3.3	–	–		–	–	7			
Fall Time (80% to 20%)	t_{6-}		–	–	1.1	2.0	3.3	–	–		–	–	7			

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

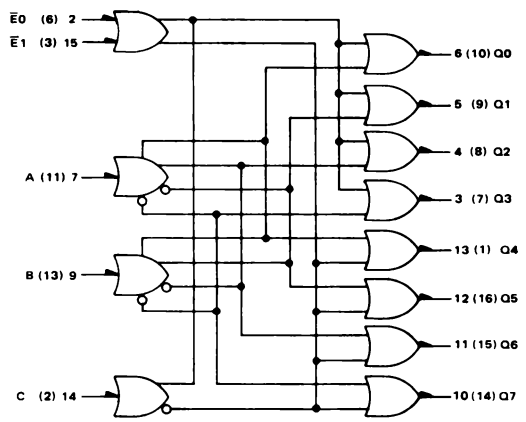


BINARY TO 1-8 DECODER
(LOW)

MC10561

The MC10561 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

POSITIVE LOGIC



Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

P_D = 315 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

TRUTH TABLE

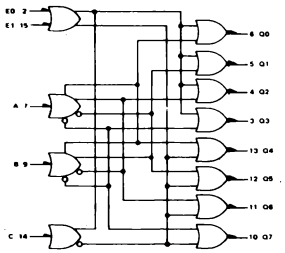
ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E}1$	$\overline{E}0$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H
ϕ	H	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

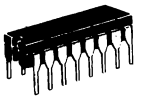
ϕ = Don't Care

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





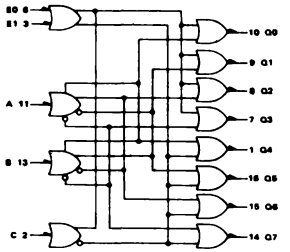
L SUFFIX
CERAMIC PACKAGE
CASE 620

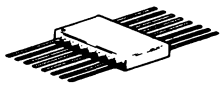
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10561L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	84	–	61	76	–	84	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14	–	374	–	–	220	–	220	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	0.5	–	0.5	–	–	0.3	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	2	–	–	–	8	1,16
		13	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	2	–	8	1,16
		13	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	14	–	8	1,16
Switching Times (100 Ω Load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13-}	13	–	–	1.5	4.0	6.0	–	–	ns	–	–	14	13	8	1,16
	t_{14-13+}	13	–	–	1.5	4.0	6.0	–	–	↓	–	–	↓	↓	↓	↓
Rise Time (20% to 80%)	t_{13+}	13	–	–	1.1	2.0	3.3	–	–	↓	–	–	↓	↓	↓	↓
Fall Time (20% to 80%)	t_{13-}	13	–	–	1.1	2.0	3.3	–	–	↓	–	–	↓	↓	↓	↓

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.



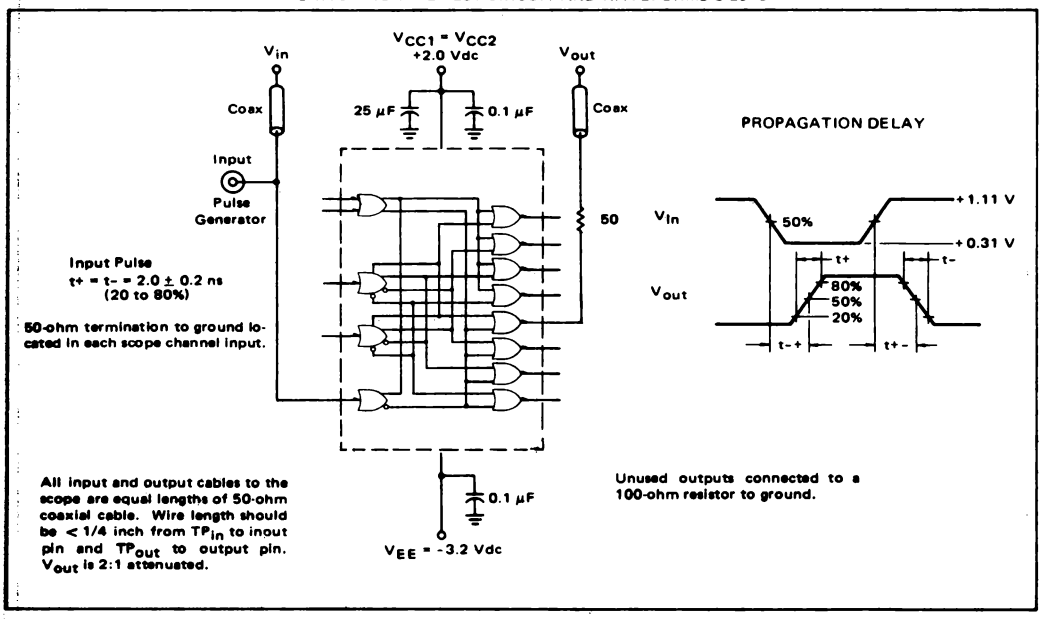


F SUFFIX
CERAMIC PACKAGE
CASE 650

● Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10561F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	84	–	61	76	–	84	mAdc	2,3,6,11,13	–	–	–	12	4,5
Input Current	I_{inH}	2	–	374	–	–	220	–	220	µAdc	2	–	–	–	12	4,5
	I_{inL}	2	0.5	–	0.5	–	–	0.3	–	µAdc	–	2	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	1	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	6	–	–	–	12	4,5
		1	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	3	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	1	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	2	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	1	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	6	–	12	4,5
		1	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	3	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	1	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	2	–	12	4,5
Switching Times (100 Ω Load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{2+1-}	1	–	–	1.5	4.0	6.0	–	–	ns	–	–	2	1	12	4,5
	t_{2-1+}	1	–	–	1.5	4.0	6.0	–	–		–	–				
Rise Time (20% to 80%)	t_{1+}	1	–	–	1.1	2.0	3.3	–	–		–	–				
Fall Time (20% to 80%)	t_{1-}	1	–	–	1.1	2.0	3.3	–	–		–	–				

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

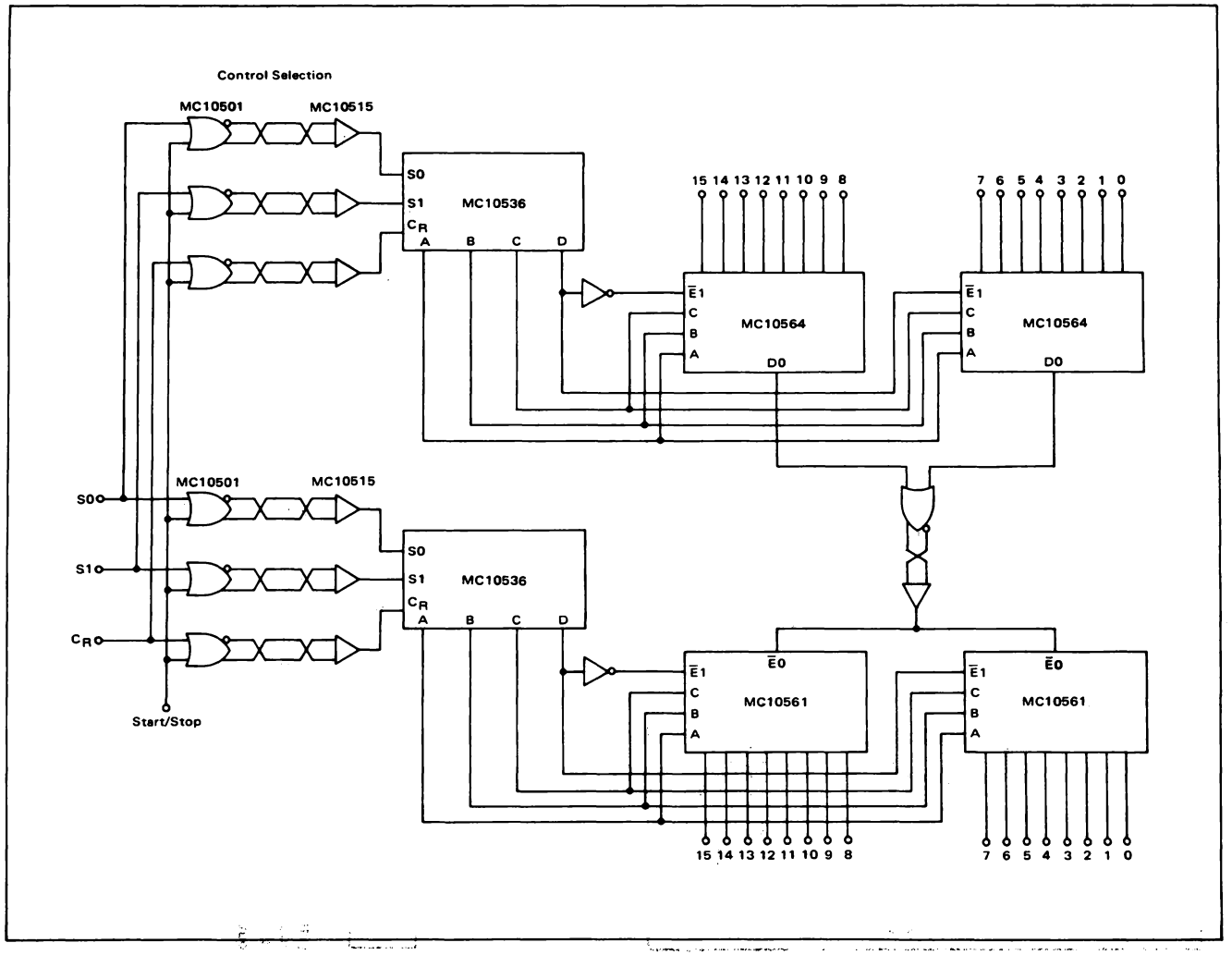


APPLICATION INFORMATION

The MC10561 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4 ns delay from any address or enable input to any output.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the MC10536 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the MC10501s to send twisted-pair select data to the multiplexer/demultiplexer units.

FIGURE 1 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

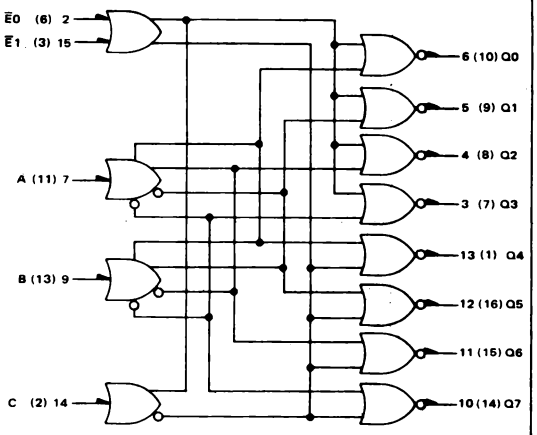


BINARY TO 1-8 DECODER
(HIGH)

MC10562

The MC10562 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

POSITIVE LOGIC



Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (case 650).

P_D = 315 ns typ/pkg (No Load)
t_{pd} = 4.0 ns typ

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

TRUTH TABLE

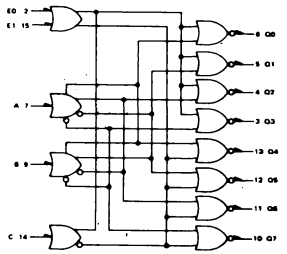
INPUTS					OUTPUTS							
Ē0	Ē1	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L
ϕ	H	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

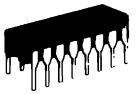
ϕ = Don't Care

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





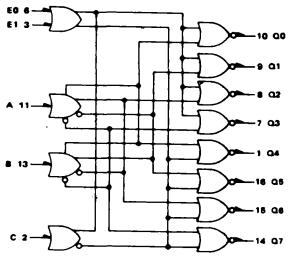
L SUFFIX
CERAMIC PACKAGE
CASE 620

@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10562L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	84	–	61	76	–	84	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	220	–	–	µAdc	14	–	–	–	8	1,16
	I_{inL}	14	0.5	–	0.5	–	–	0.3	–	µAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	2	–	–	–	8	1,16
		13	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	15	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	2	–	8	1,16
		13	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	15	–	8	1,16
Switching Times (100-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13+}	13	–	–	1.5	4.0	6.0	–	–	ns	–	–	14	13	8	1,16
	t_{14-13-}	13	–	–	1.5	4.0	6.0	–	–	↓	–	–	↓	↓	↓	↓
Rise Time (20% to 80%)	t_+	13	–	–	1.1	2.0	3.3	–	–		–	–				
Fall Time (20% to 80%)	t_-	13	–	–	1.1	2.0	3.3	–	–		–	–				

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

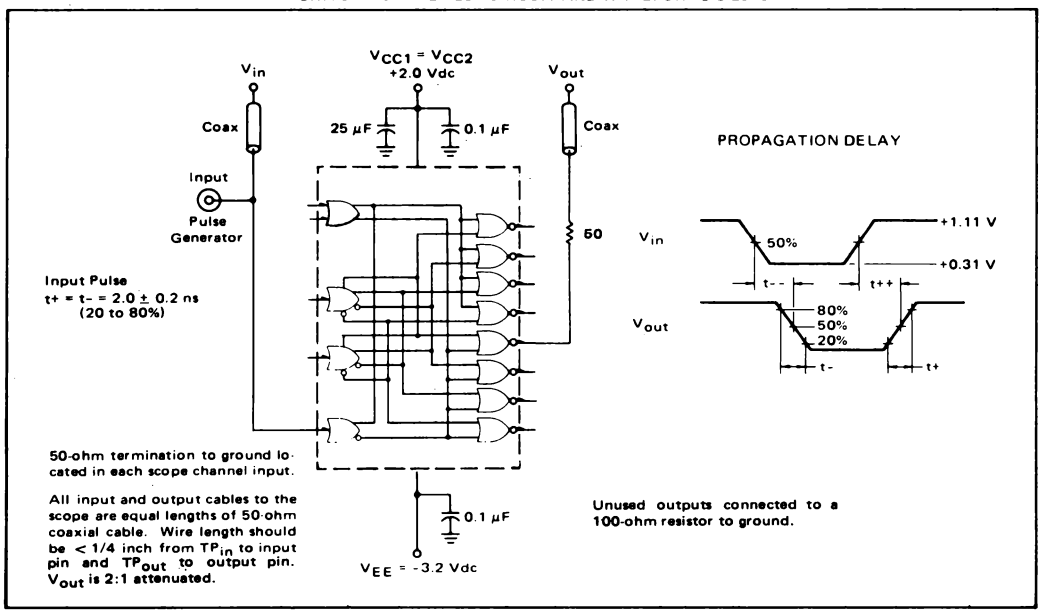


F SUFFIX
CERAMIC PACKAGE
CASE 650

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10562F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	84	–	61	76	–	84	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	2	–	–	–	–	220	–	–	µAdc	2	–	–	–	12	4,5
	I_{inL}	2	0.5	–	0.5	–	–	0.3	–	µAdc	–	2	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	1	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	2	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	1	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	6	–	–	–	12	4,5
		1	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	3	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	1	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	2	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	1	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	6	–	12	4,5
		1	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	3	–	12	4,5
Switching Times (100-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{2+1+}	1	–	–	1.5	4.0	6.0	–	–	ns	–	–	2	1	12	4,5
	t_{2-1-}	1	–	–	1.5	4.0	6.0	–	–		–	–				
Rise Time (20% to 80%)	t_+	1	–	–	1.1	2.0	3.3	–	–		–	–				
Fall Time (20% to 80%)	t_-	1	–	–	1.1	2.0	3.3	–	–		–	–				

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



APPLICATION INFORMATION

The MC10562 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders.

This device is ideally suited for demultiplexer applications as shown in Figure 1. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 2. This system, using the MC10536 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. Control information via twisted pair lines is sent through MC10501 gates to the MC10515 line receivers to provide select data to the multiplexer/demultiplexer units.

FIGURE 1 – DEMULTIPLEXER (1 OF 8 LOCATIONS)

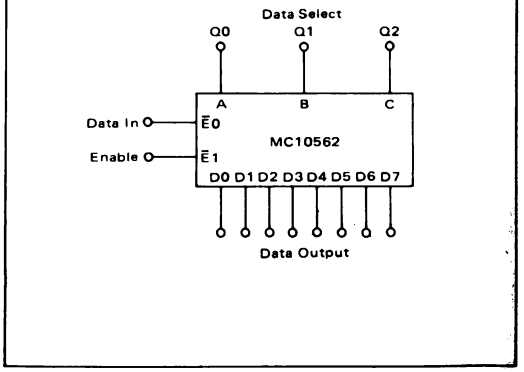
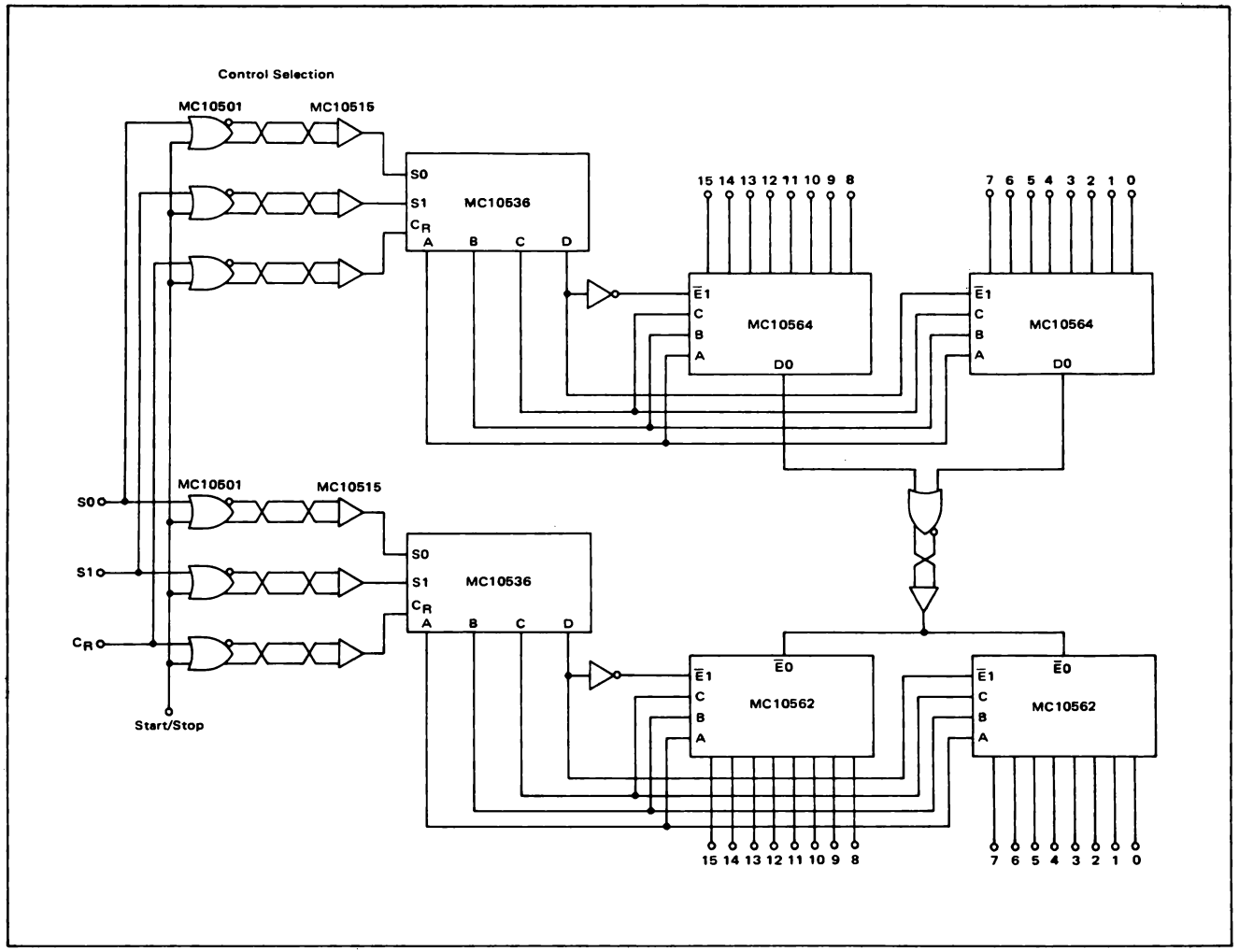


FIGURE 2 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER



MC10564

The MC10564 is a high speed, low power MECL eight-channel data selector which routes data present at one-of-eight inputs to the output. The data is routed according to the three bit code present on the address inputs. An enable input is provided for easy bit expansion.

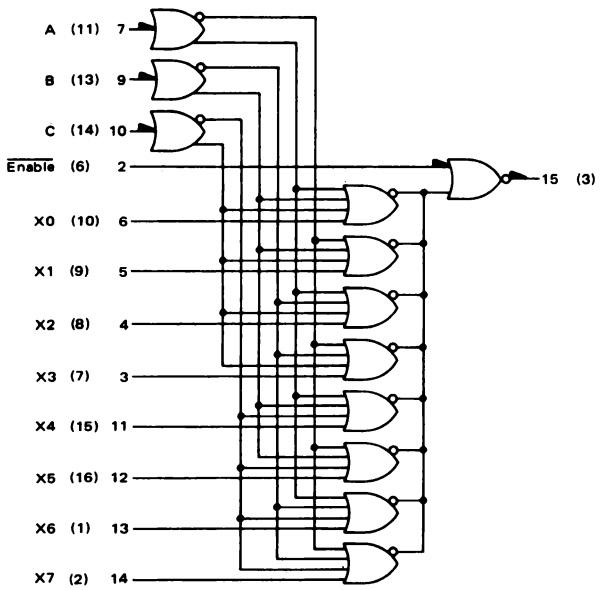
TRUTH TABLE

ENABLE	ADDRESS INPUTS C	B	A	DATA ROUTED FROM:
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

POSITIVE LOGIC



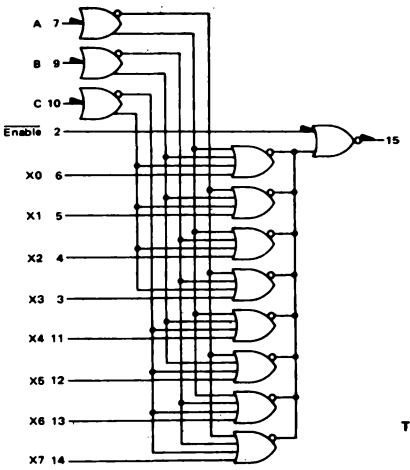
Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

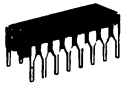
Numbers at end of terminals are pin numbers for L package (Case 620)
Numbers in parenthesis denotes pin numbers for F package (Case 650)

See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





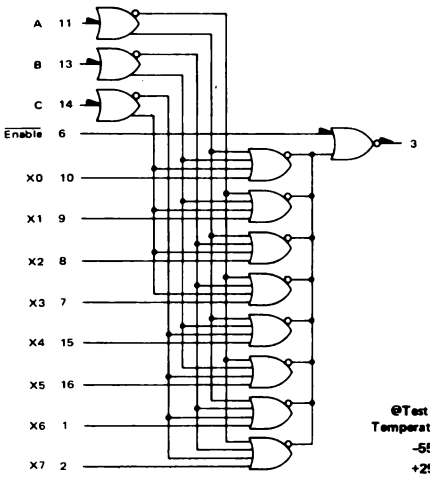
L SUFFIX
CERAMIC PACKAGE
CASE 620

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10564L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	83	–	60	75	–	83	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	455	–	–	265	–	265	µAdc	2	–	–	–	8	1,16
	$I_{in\ L}$	4	0.5	–	0.5	–	–	0.3	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	4,9	2,7,10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	9	2,4,7,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.100	–	-0.950	–	–	-0.845	–	Vdc	9	7,10	4	2	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	4,7,10	9	2	8	1,16
Switching Times (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+15+}	15	1.3	4.6	1.5	3.0	4.5	1.2	4.5	ns	9	–	4	15	8	1,16
	t_{4-15-}	15	1.3	4.6	1.5	3.0	4.5	1.2	4.5		9	–	4			
	t_{7+15+}	15	1.8	6.1	2.0	4.0	6.0	1.9	6.0		5	–	7			
	t_{7-15-}	15	1.8	6.1	2.0	4.0	6.0	1.9	6.0		5	–	7			
	t_{2+15-}	15	0.9	3.0	1.0	2.0	2.9	0.9	2.9		7,5	–	2			
	t_{2-15+}	15		3.0	1.0		2.9		2.9		7,5	–	2			
Rise Time (20% to 80%)	t+	15		3.3	1.1		3.3		3.4		9	–	4			
Fall Time (20% to 80%)	t-	15		3.3	1.1		3.3		3.4		9	–	4			

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.

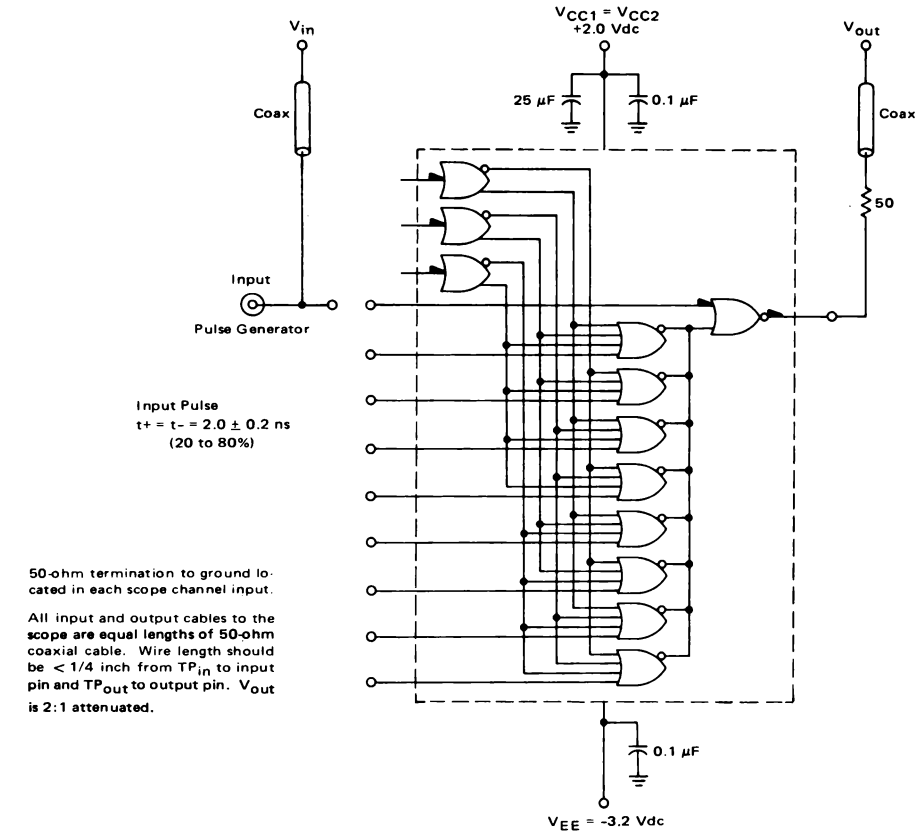


F SUFFIX
CERAMIC PACKAGE
CASE 650

@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10564F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	83	–	60	75	–	83	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\ H}$	8	–	455	–	–	265	–	265	μAdc	6	–	–	–	12	4,5
	$I_{in\ L}$	8	0.5	–	0.5	–	–	0.3	–	μAdc	–	8	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	8,13	6, 11, 14	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	13	6, 8, 11, 14	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	13	11, 14	8	6	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	8, 11, 14	13	6	12	4,5
Switching Times (100-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{8+3+}	3	–	–	1.5	3.0	4.5	–	–	ns	13	–	8	15	12	4,5
	t_{8-3-}		–	–	1.5	3.0	4.5	–	–		13	–	8			
	t_{11+3+}		–	–	2.0	4.0	6.0	–	–		9	–	11			
	t_{11-3-}		–	–	2.0	4.0	6.0	–	–		9	–	11			
	t_{6+3-}		–	–	1.0	2.0	2.9	–	–		9,11	–	6			
	t_{6-3+}		–	–	1.0		2.9	–	–		9,11	–	6			
Rise Time (20% to 80%)	t_{3+}		–	–	1.1		3.3	–	–		13	–	8			
Fall Time (20% to 80%)	t_{3+}		–	–	1.1		3.3	–	–		13	–	8			

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

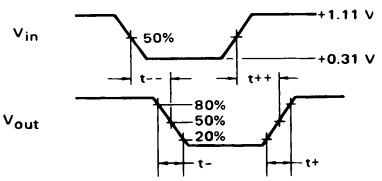


Input Pulse
$t+ = t- = 2.0 \pm 0.2$ ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

PROPAGATION DELAY

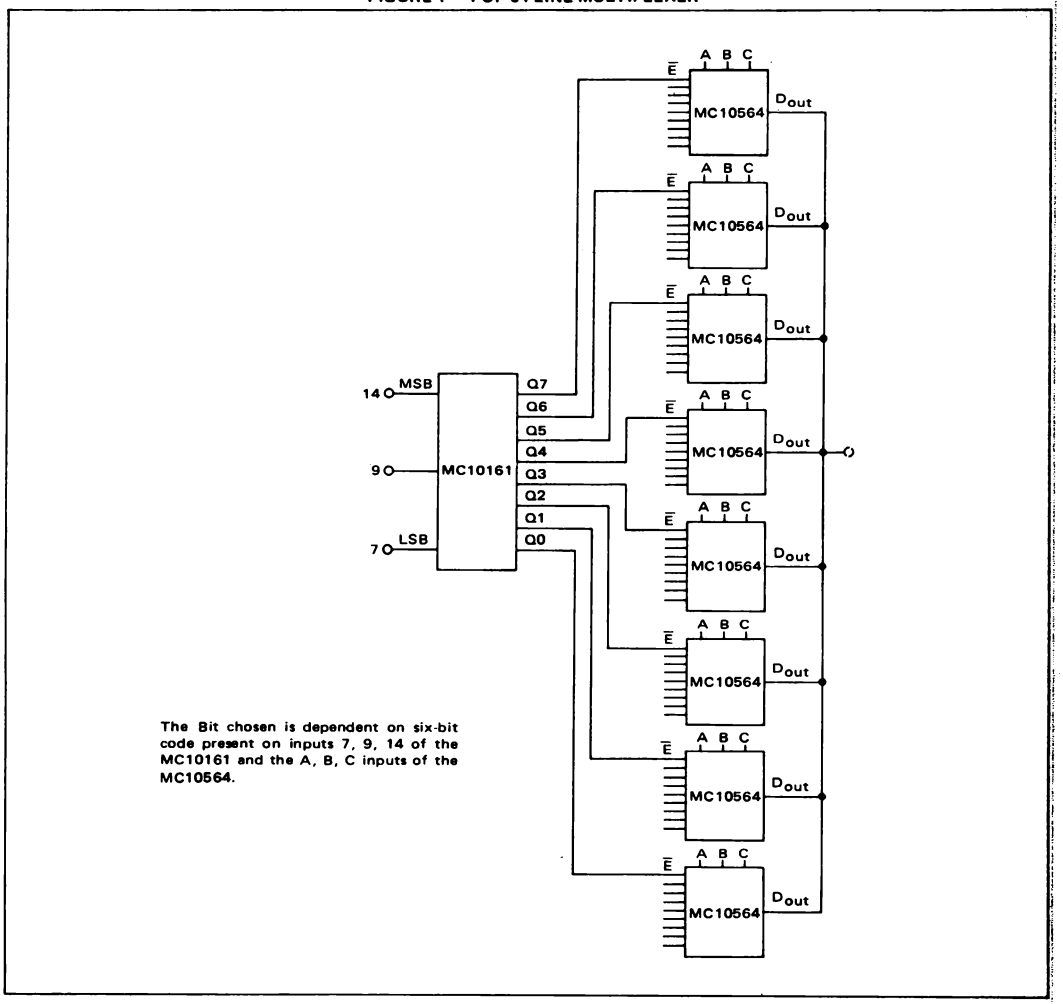


APPLICATION INFORMATION

The MC10564 can be used wherever data multiplexing or parallel to serial conversion is desirable. Full parallel gating permits equal delays through any data path. The output of the MC10564 incorporates a buffer gate with eight data inputs and an enable. A high level on the enable forces the output low. The MC10564 can be connected directly to a data bus, due to its open emitter output and output enable.

Figure one illustrates how a 1-of-64 line multiplexer can be built with eight MC10564's wire ORed at their outputs and one MC10161 to drive the enables on each multiplexer, without speed degradation over a single MC10564 being experienced.

FIGURE 1 – 1-OF-64 LINE MULTIPLEXER



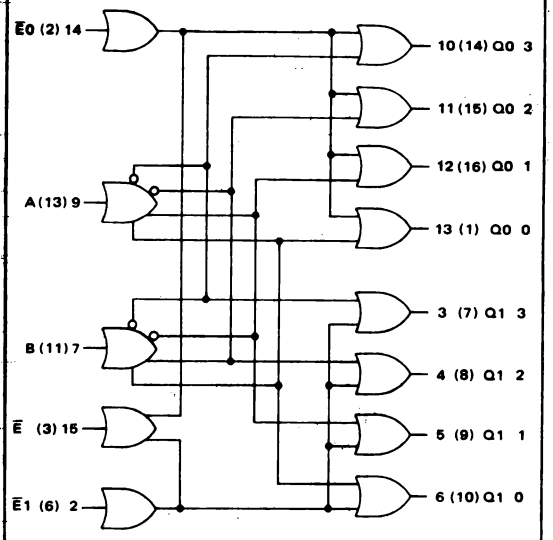
DUAL BINARY TO
1-4 DECODER
(LOW)

MC10571

The MC10571 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E}0$ or $\overline{E}1$ high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$ forces all outputs high.

All propagation delay times are equal due to the internal emitter dotting techniques used. High impedance 50 k ohm resistors on all inputs eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (case 650).

P_D = 330 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

TRUTH TABLE

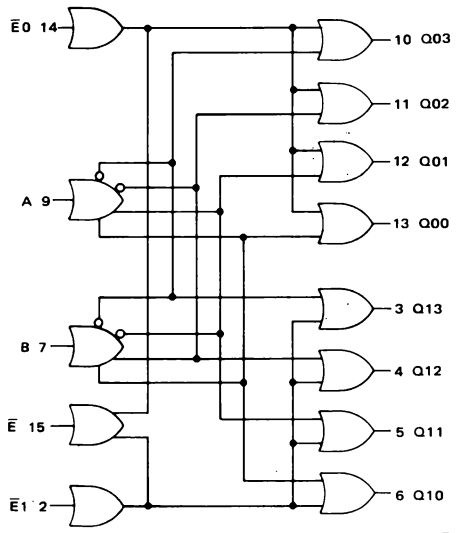
ENABLE INPUTS			INPUTS		OUTPUTS							
$\overline{E}$	$\overline{E}0$	$\overline{E}1$	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

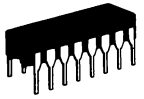
ϕ = Don't Care

See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





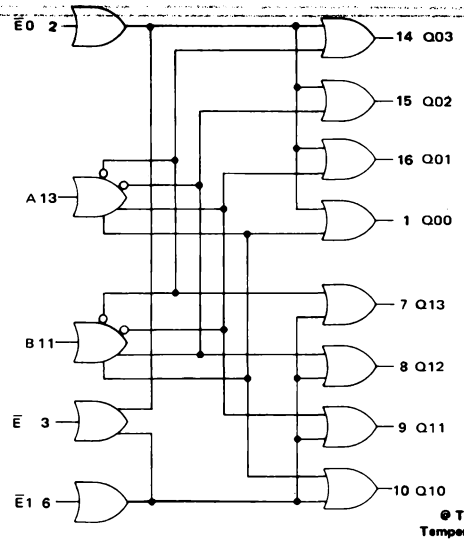
L SUFFIX
CERAMIC PACKAGE
CASE 620

● Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10571L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	64	77	–	–	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	220	–	–	µAdc	14	–	–	–	8	1,16
	I_{inL}	14	0.5	–	0.5	–	–	0.3	–	µAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	15	–	–	–	8	1,16
		13	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	2,7,9,14,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	15	–	8	1,16
		13	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	2,9,14,15	–	7	8	1,16
		13	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	2,7,14,15	–	9	8	1,16
Switching Times (100Ω Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6+}	6	–	–	1.5	4.0	6.0	–	–	ns	14	2,9,15	7	6	8	1,16
	t_{7-6-}	6	–	–	↓	↓	↓	–	–	↓	14	2,9,15	↓	6	↓	↓
	t_{7+13+}	13	–	–	↓	↓	↓	–	–	↓	2	9,14,15	↓	13	↓	↓
	t_{7-13-}	13	–	–	↓	↓	↓	–	–	↓	2	9,14,15	↓	13	↓	↓
	t_{6+}	6	–	–	1.1	2.0	3.3	–	–	↓	14	2,9,15	↓	6	↓	↓
Rise Time (20% to 80%)	t_{13+}	13	–	–	↓	↓	↓	–	–	↓	2	9,14,15	↓	13	↓	↓
	t_{6-}	6	–	–	↓	↓	↓	–	–	↓	14	2,9,15	↓	6	↓	↓
Fall Time (20% to 80%)	t_{13-}	13	–	–	↓	↓	↓	–	–	↓	2	9,14,15	↓	13	↓	↓

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

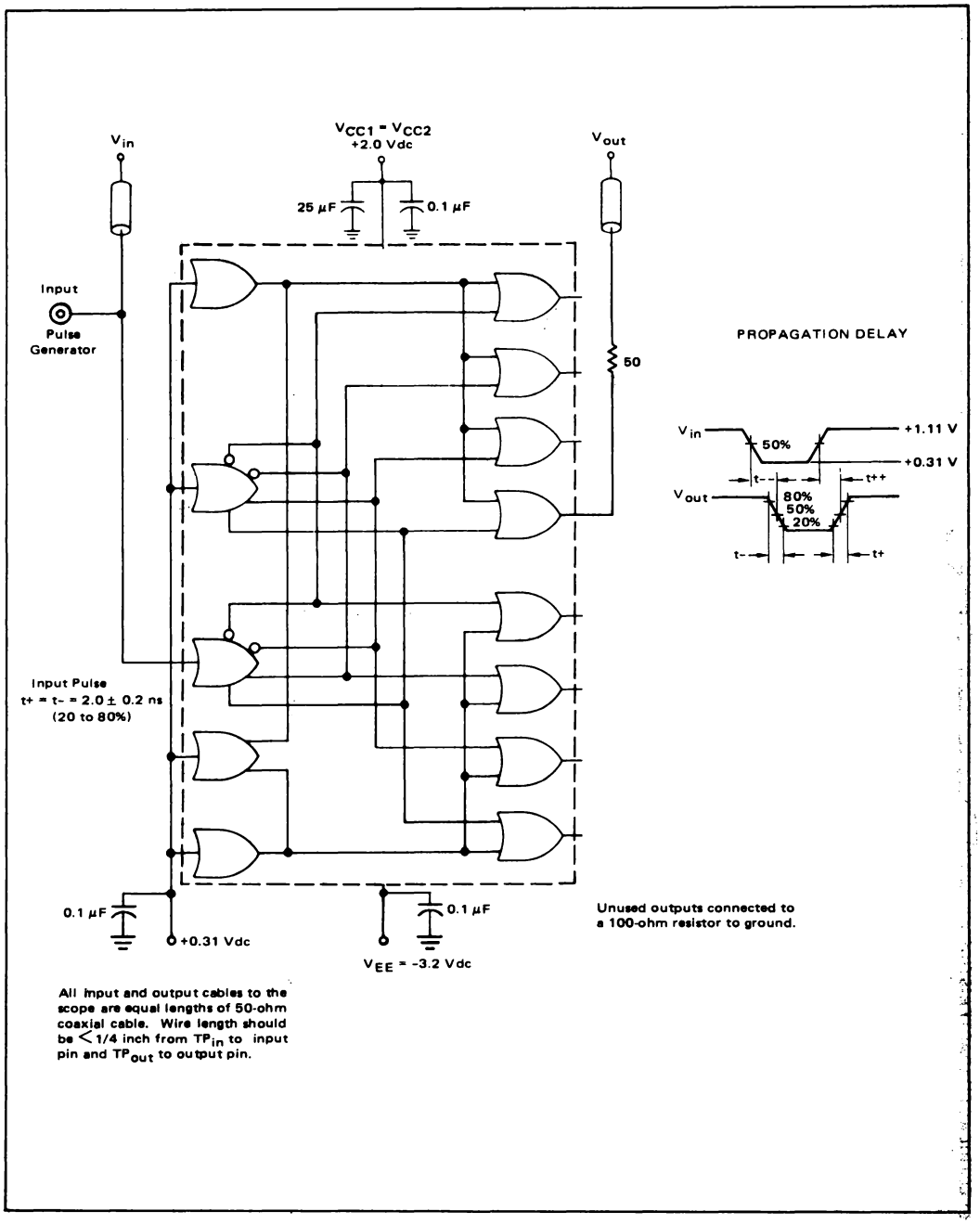


F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

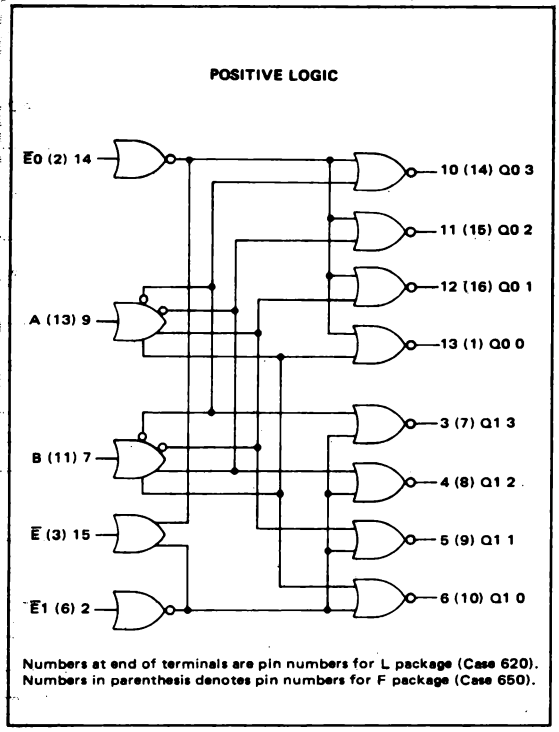
Characteristic	Symbol	Pin Under Test	MC10571F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–	64	77	–	–	mAdc	2,3,6,11,13	–	–	–	12	4,5
Input Current	I_{inH}	2	–	–	–	–	220	–	–	µAdc	2	–	–	–	12	4,5
	I_{inL}	2	0.5	–	0.5	–	–	0.3	–	µAdc	–	2	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	10	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	3	–	–	–	12	4,5
		1	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	3	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	1	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	2,7,9,14,15	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	10	-1.100	–	-0.950	–	–	-0.845	–	Vdc	3	–	3	–	12	4,5
		1	-1.100	–	-0.950	–	–	-0.845	–	Vdc	3	–	3	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	10	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	2,9,14,15	–	11	12	4,5
		1	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	2,7,14,15	–	13	12	4,5
Switching Times (100 Ω Load)											+1.110 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{11+10+}	10	–	–	1.5	4.0	6.0	–	–	ns	2	3,6,13	11	10	12	4,5
	t_{11-10-}	10	–	–	↓	↓	↓	–	–	↓	2	3,6,13	↓	10	↓	↓
	t_{11+1+}	1	–	–	↓	↓	↓	–	–	↓	6	2,3,13	↓	1	↓	↓
	t_{11-1-}	1	–	–	↓	↓	↓	–	–	↓	6	2,3,13	↓	1	↓	↓
	t_{10+}	10	–	–	1.1	2.0	3.3	–	–	↓	2	3,6,13	↓	10	↓	↓
Rise Time (20% to 80%)	t_{1+}	1	–	–	↓	↓	↓	–	–	↓	6	2,3,13	↓	1	↓	↓
	t_{10-}	10	–	–	↓	↓	↓	–	–	↓	2	3,6,13	↓	10	↓	↓
Fall Time (20% to 80%)	t_{1-}	1	–	–	↓	↓	↓	–	–	↓	6	2,3,13	↓	1	↓	↓

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



DUAL
BINARY TO 1-4-DECODER
(HIGH)

MC10572



Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

The MC10572 is a binary-coded 2 line to dual 4 line decoder with selected outputs high. With either $\overline{E}0$ or $\overline{E}1$ low, the corresponding selected 4 outputs are low. The common enable $\overline{E}$, when high, forces all outputs low.

All propagation delay times are equal. High impedance 50 k ohm resistors on all inputs eliminate the need to tie unused inputs to V_{EE}.

P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

TRUTH TABLE

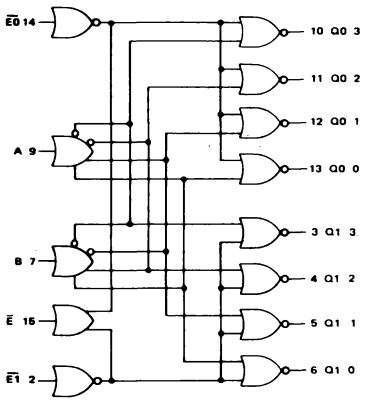
$\overline{E}$	$\overline{E}1$	$\overline{E}0$	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

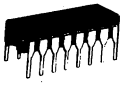
ϕ = Don't Care

See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





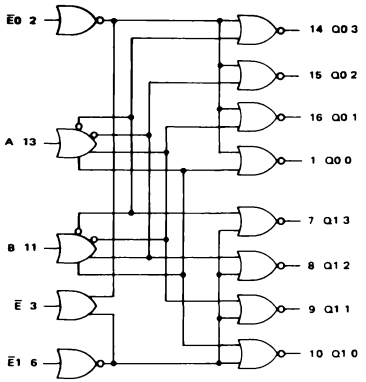
L SUFFIX
CERAMIC PACKAGE
CASE 620

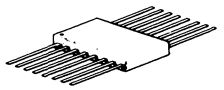
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10572L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	62	77	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	220	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	0.5	–	0.5	–	–	0.3	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	2	–	–	–	8	1,16
		13	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	15	2,7,9,14	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	2	–	8	1,16
		13	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	2,9,14	–	7	8	1,16
		13	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	2,7,14	–	9	8	1,16
Switching Times (100 Ω Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6-}	6	–	–	1.5	4.0	6.0	–	–	ns	2	9,14	7	6	8	1,16
	t_{7-6+}	6	–	–	↓	↓	↓	–	–	↓	2	9,14	↓	6	↓	↓
	t_{7+13-}	13	–	–	↓	↓	↓	–	–	↓	14	2,9	↓	13	↓	↓
	t_{7-13+}	13	–	–	↓	↓	↓	–	–	↓	14	2,9	↓	13	↓	↓
Rise Time (20% to 80%)	t_{6+}	6	–	–	1.1	2.0	3.3	–	–	↓	2	9,14	↓	6	↓	↓
	t_{13+}	13	–	–	↓	↓	↓	–	–	↓	14	2,9	↓	13	↓	↓
Fall Time (20% to 80%)	t_{6-}	6	–	–	↓	↓	↓	–	–	↓	2	9,14	↓	6	↓	↓
	t_{13-}	13	–	–	↓	↓	↓	–	–	↓	14	2,9	↓	13	↓	↓

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.



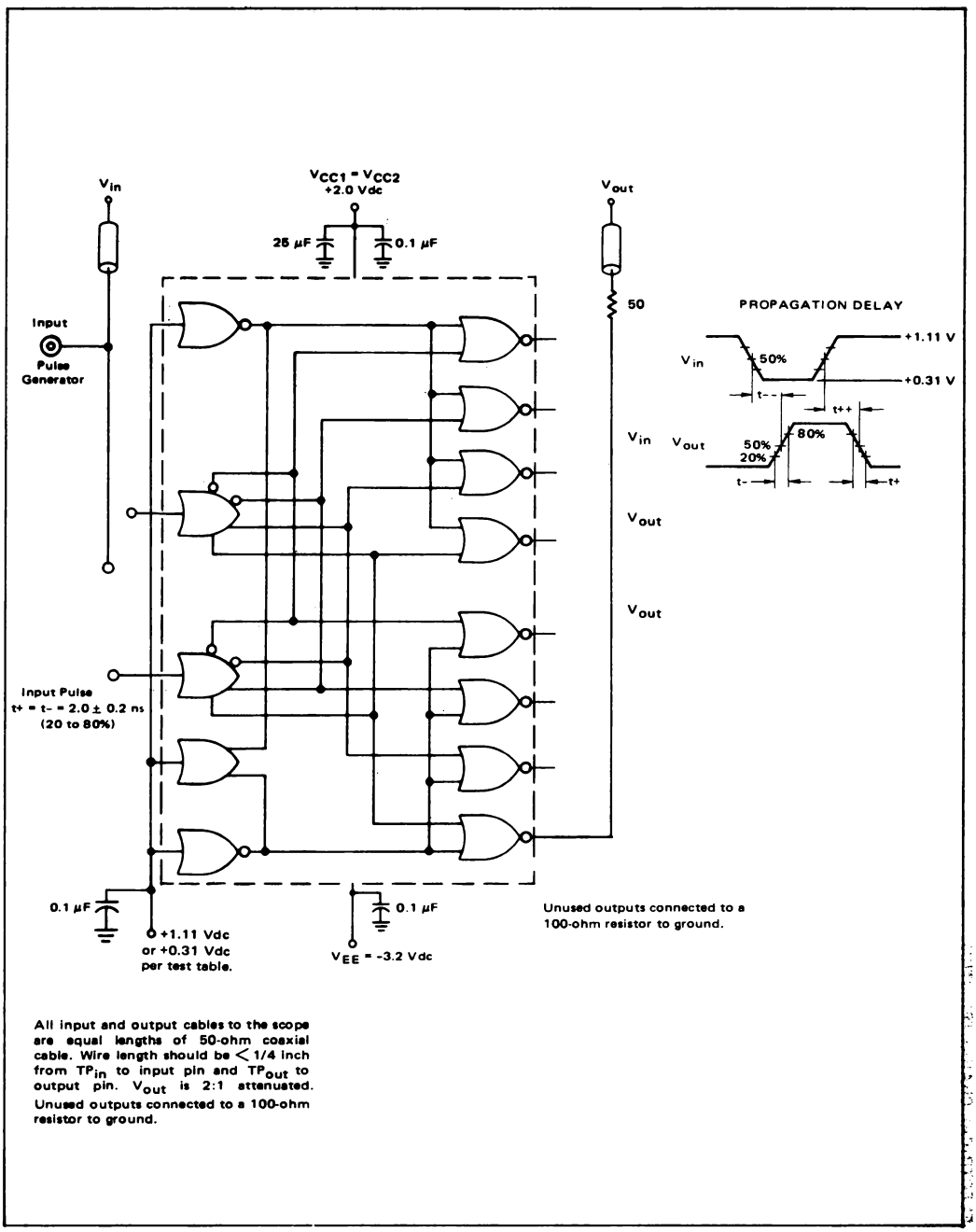


F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10572F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–	62	77	–	–	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	2	–	–	–	–	220	–	–	μAdc	2	–	–	–	12	4,5
	I_{inL}	2	0.5	–	0.5	–	–	0.3	–	μAdc	–	12	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	10	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	6	–	–	–	12	4,5
		1	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	2	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	1	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	3	2,6,11,13	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	10	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	6	–	12	4,5
		1	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	2	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	10	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	2,6,13	–	11	12	4,5
		1	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	2,6,11	–	13	12	4,5
Switching Times (100 Ω Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{11+6-}	10	–	–	1.5	4.0	6.0	–	–	ns	6	2,13	11	10	12	4,5
	t_{11-6+}	10	–	–	↓	↓	↓	–	–	↓	6	2,13	↓	10	↓	↓
	t_{11+1-}	1	–	–	↓	↓	↓	–	–	↓	2	6,13	↓	1	↓	↓
	t_{11-1+}	1	–	–	↓	↓	↓	–	–	↓	2	6,13	↓	1	↓	↓
Rise Time (20% to 80%)	t_{10+}	10	–	–	1.1	2.0	3.3	–	–	↓	6	2,13	↓	10	↓	↓
	t_{1+}	1	–	–	↓	↓	↓	–	–	↓	2	6,13	↓	1	↓	↓
Fall Time (20% to 80%)	t_{10-}	10	–	–	↓	↓	↓	–	–	↓	2	2,13	↓	10	↓	↓
	t_{1-}	1	–	–	↓	↓	↓	–	–	↓	14	6,13	↓	1	↓	↓

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

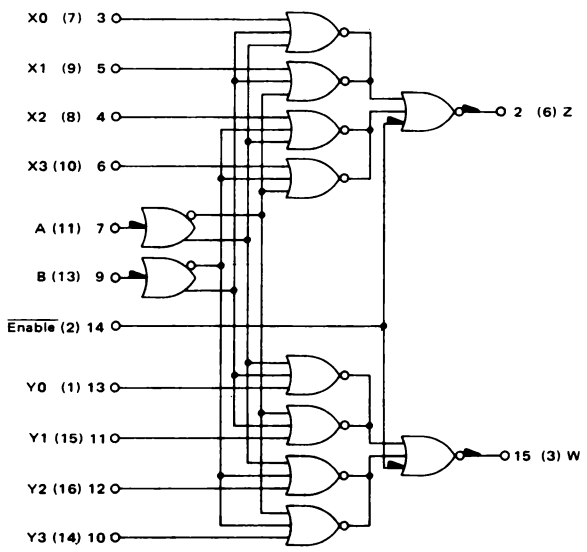


All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated. Unused outputs connected to a 100-ohm resistor to ground.

MC10574

P_D = 305 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (Data to output)

The MC10574 is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state. The enable is also useful in wire-ORing several multiplexers to achieve additional channel capability. Delay from data input to output is typically 3.5 nanoseconds.



Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Z	W
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

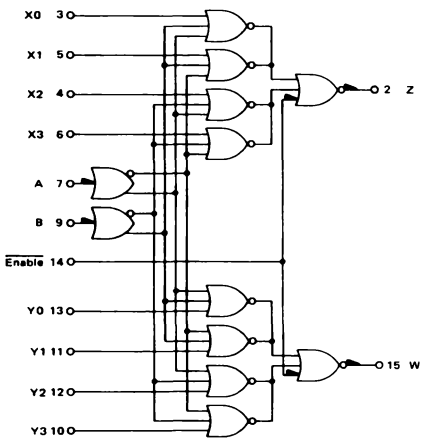
ϕ = Don't Care

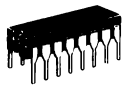
Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

See General Information section for packaging, and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.





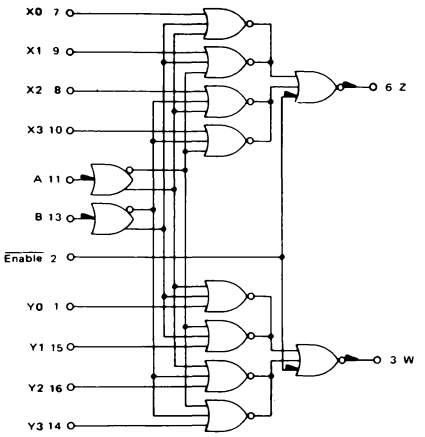
L SUFFIX
CERAMIC PACKAGE
CASE 620

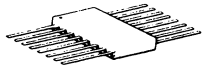
@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10574L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	80	–	58	73	–	80	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	375	–	–	220	–	220	µAdc	4	–	–	–	8	1,16
		14	–	565	–	–	330	–	330		14	–	–	–	8	1,16
	$I_{in\ L}$	4	0.5	–	0.5	–	–	0.3	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	13	14	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	14	–	8	1,16
Switching Times (100 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{13+15+}	15	1.3	4.6	1.5	3.5	4.5	1.2	4.5	ns	–	–	13	15	8	1,16
	t_{13-15-}	15	1.3	4.6	1.5	3.5	4.5	1.2	4.5		–	–	13			
	t_{7+15-}	15	1.8	6.1	2.0	5.0	6.0	1.9	6.0		13	–	7			
	t_{7-15+}	15	1.8	6.1	2.0	5.0	6.0	1.9	6.0		13	–	7			
	t_{14+15-}	15	0.9	3.0	1.0	2.0	2.9	0.9	2.9		13	–	14			
	t_{14-15+}	15		3.0	1.0	2.0	2.9		2.9		13	–	14			
Rise Time (20% to 80%)	t+	15		3.3	1.1	2.0	3.3		3.4		13	–	14			
Fall Time (20% to 80%)	t-	15		3.3	1.1	2.0	3.3		3.4		13	–	14			

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.



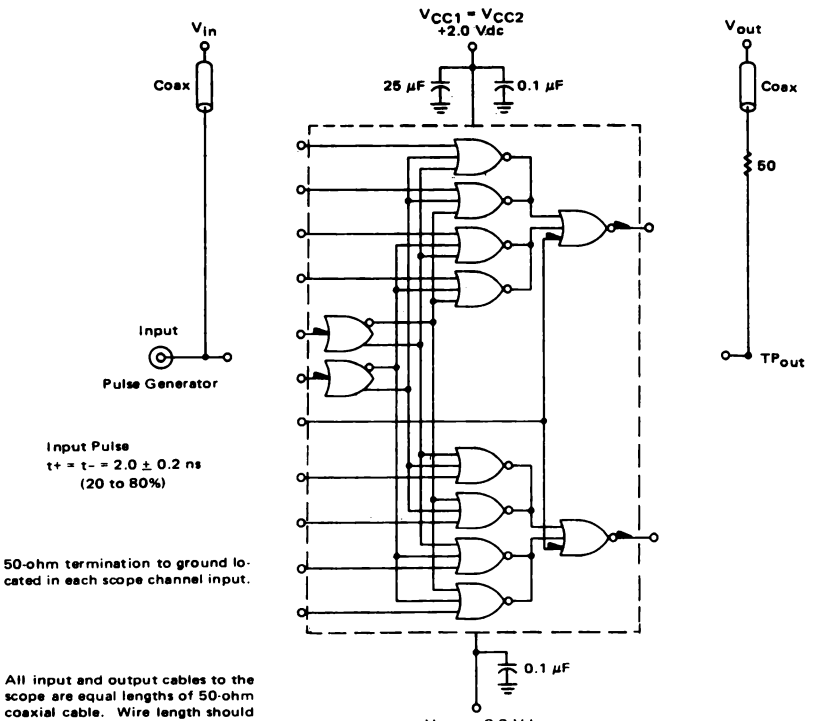


F SUFFIX
CERAMIC PACKAGE
CASE 650

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10574F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	80	–	58	73	–	80	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\ H}$	8	–	375	–	–	220	–	220	µAdc	8	–	–	–	12	4,5
		2	–	565	–	–	330	–	330		2	–	–	–	12	4,5
	$I_{in\ L}$	8	0.5	–	0.5	–	–	0.3	–	µAdc	–	8	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	1	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	2	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	–	2	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	2	–	12	4,5
Switching Times (100 Ω Lead)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{1+3+}	3	–	–	1.5	3.5	4.5	–	–	ns	–	–	1	3	12	4,5
	t_{1-3-}	3	–	–	1.5	3.5	4.5	–	–		–	–	1			
	t_{11+3-}	3	–	–	2.0	5.0	6.0	–	–		1	–	11			
	t_{11-3+}	3	–	–	2.0	5.0	6.0	–	–			–	11			
	t_{2+3-}	3	–	–	1.0	2.0	2.9	–	–			–	2			
	t_{2-3+}	3	–	–	1.0	2.0	2.9	–	–			–				
Rise Time (20% to 80%)	t+	3	–	–	1.1	2.0	3.3	–	–			–				
Fall Time (20% to 80%)	t-	3	–	–	1.1	2.0	3.3	–	–			–				

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

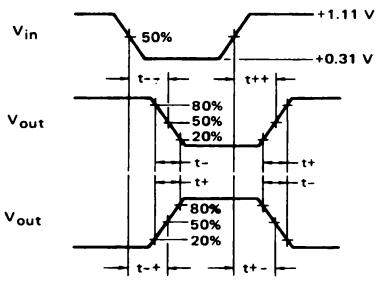


Input Pulse
$t+ = t- = 2.0 \pm 0.2$ ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

PROPAGATION DELAY



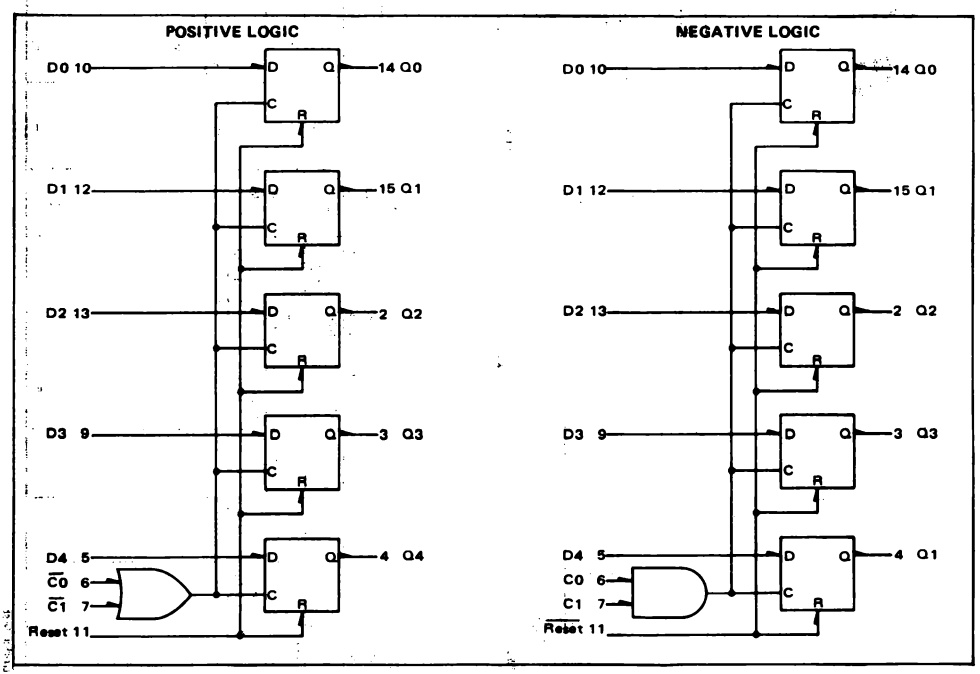
QUINT LATCH

MC10575

The MC10575 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together. Propagation delays are typically 2.1 nanoseconds from each data input to the output.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

The MC10575 allows storage of five bits of information, and it is useful in temporary storage applications in high speed central processors, accumulators, register files, digital communication systems, instrumentation, and test equipment.



TRUTH TABLE

D	$\overline{C0}$	$\overline{C1}$	Reset	Q_{n+1}
L	L	L	ϕ	L
H	L	L	ϕ	H
ϕ	H	ϕ	L	Q_n
ϕ	ϕ	H	L	Q_n
ϕ	H	ϕ	H	L
ϕ	ϕ	H	H	L

ϕ = don't care

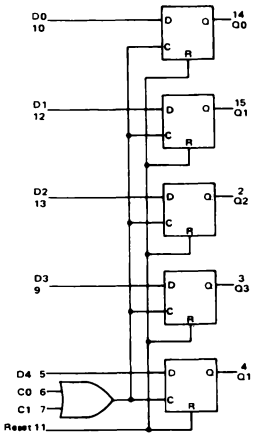
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

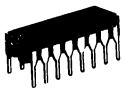
P_D = 400 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Output)

See General Information section for packaging and maximum ratings.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test Procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in the same manner.





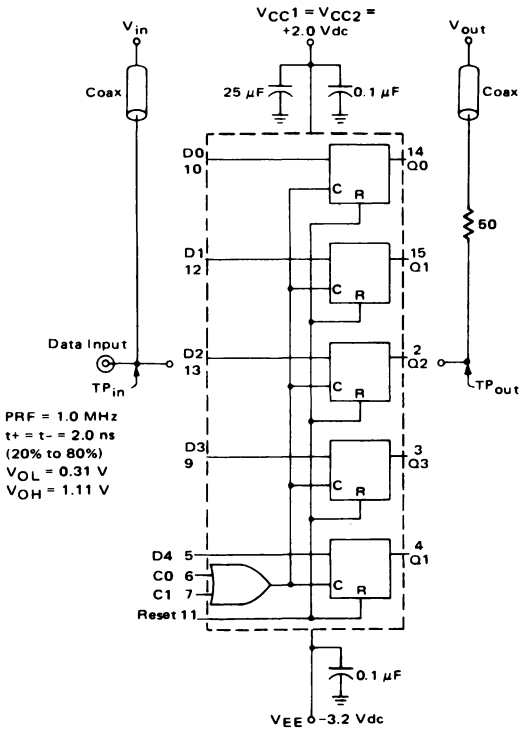
L SUFFIX
CERAMIC PACKAGE
CASE 620

● Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.500	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10575L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	78	97	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6	–	–	–	–	290	–	–	μAdc	6	–	–	–	8	1,16
		7	–	–	–	–	290	–	–	↓	7	–	–	–	↓	↓
		10	–	–	–	–	290	–	–		10	–	–	–		
		11	–	–	–	–	645	–	–		11	–	–	–		
Input Leakage Current	I_{inL}	All	0.5	–	0.5	–	–	0.3	–	μAdc	–	①	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	10	6	–	–	8	1,16
		15	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	12	6	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	6,10	–	–	8	1,16
		15	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	6,12	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	14	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	6	10	–	8	1,16
		15	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	6	12	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	14	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	6	–	10	8	1,16
		15	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	6	–	12	8	1,16
Switching Times											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Data Input	t_{10+14+}	14	–	–	1.0	2.1	3.5	–	–	ns	–	6,7	10	14	8	1,16
	t_{10-14-}	↓	–	–	1.0	2.1	3.5	–	–	↓	–	6,7	10	↓	↓	↓
Clock Input	t_{6-14+}		–	–	1.0	2.6	4.3	–	–		–	7	6,10			
	t_{6-14-}		–	–	1.0	2.6	4.3	–	–		–	7	6,10			
Reset Input	t_{11+4-}	4	–	–	1.0	2.8	3.9	–	–		5	6	7,11	4 ②		
	t_{11+14-}	14	–	–	1.0	2.8	3.9	–	–		10	6	7,11	14 ②		
Setup Time	t_{setup}	14	–	–	2.5	–	–	–	–		–	7	6,10	14		
Hold Time	t_{hold}	14	–	–	1.5	–	–	–	–		–	7	6,10			
Rise Time (20 to 80%)	t+	14	–	–	1.1	2.0	3.5	–	–		–	6,7	10	↓	↓	↓
Fall Time (20 to 80%)	t-	14	–	–	1.1	2.0	3.5	–	–	↓	–	6,7	10			

① Individually test each input; apply $V_{IL\ min}$ to pin under test.
② Output latched to high logic state prior to test.

SWITCHING TIME TEST CIRCUIT



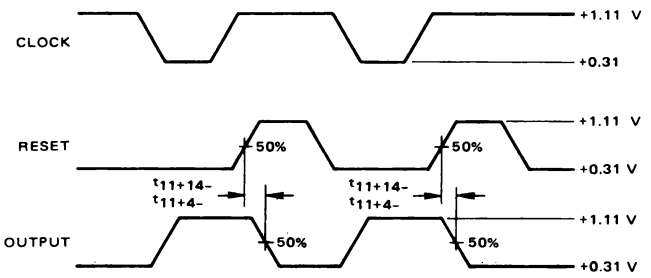
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

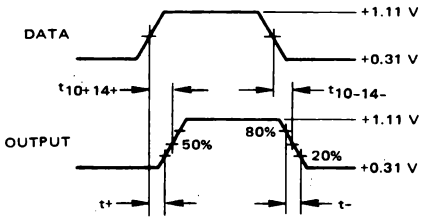
Unused outputs connected to a 100 Ω resistor to ground.

VOLTAGE WAVEFORMS

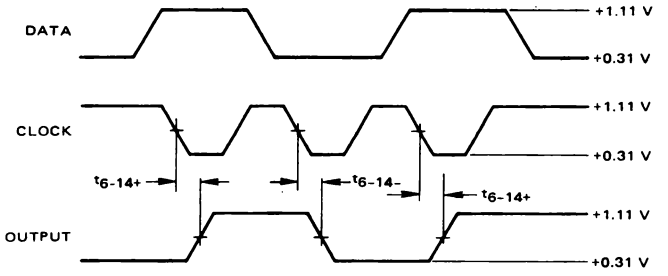
RESET INPUT

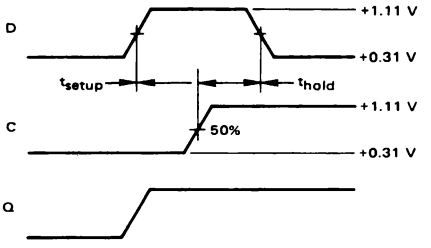


DATA INPUT



CLOCK INPUT





NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

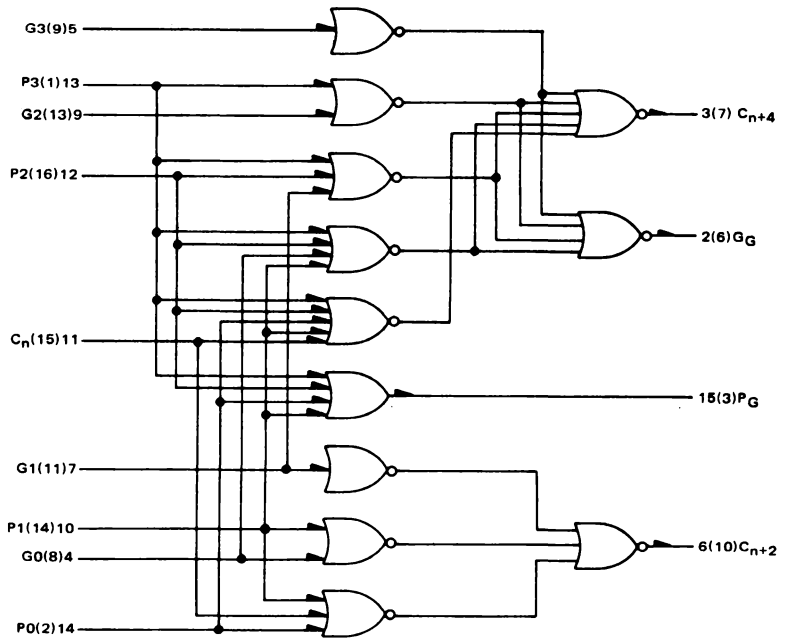
LOOK-AHEAD CARRY BLOCK

MC10579

P_D = 300 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ (Carry, Propagate)
4.0 ns typ (Generate)

The MC10579 device has 12 low power gates internally connected to perform the look-ahead carry function. This device has high Z input pulldown resistors and open emitter outputs. This device has applications in fast look-ahead adders such as with the MC10581. It can be used also as a boolean function generator.

POSITIVE LOGIC



P_G = P0 + P1 + P2 + P3
G_G = (G0 + P1 + P2 + P3) (G1 + P2 + P3) (G2 + P3) G3
C_{n+2} = (C_n + P0 + P1) (G0 + P1) G1
C_{n+4} = (C_n + P0 + P1 + P2 + P3) (G0 + P1 + P2 + P3) (G1 + P2 + P3) (G2 + P3) G3

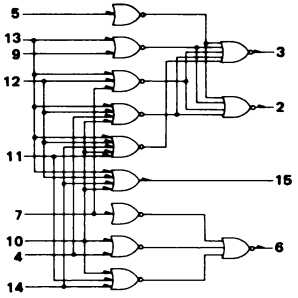
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

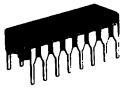
Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





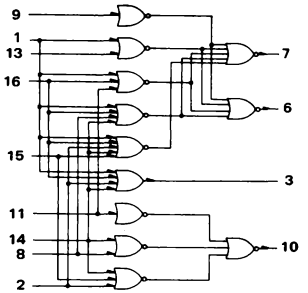
L SUFFIX
CERAMIC PACKAGE
CASE 620

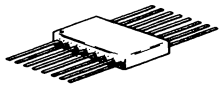
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10579L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	58	72	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4,7,11	–	–	–	–	270	–	–	μAdc	4,7,11	–	–	–	8	1,16
		5,9	–	–	–	–	225	–	–		5,9	–	–	–		
		10,13	–	–	–	–	440	–	–		10,13	–	–	–		
		12	–	–	–	–	395	–	–		12	–	–	–		
		14	–	–	–	–	355	–	–		14	–	–	–		
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	4,5,7,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	13	–	5	–	8	1,16
		2		–		–	–		–		5,12	–	9	–		
		2		–		–	–		–		5,9	–	12	–		
		2		–		–	–		–		5	–	13	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	13	–	–	5	8	1,16
		2	–		–	–		–			5	–	–	13		
		2	–		–	–		–			5	–	–	9		
		2	–		–	–		–			5,9	–	–	12		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{11+6+}	6	–	–	1.0	–	4.5	–	–	ns	4,7	–	11	6	8	1,16
	t_{11-6-}	6	–	–		–	4.5	–	–		4,7	–	11	6		
	t_{5+2+}	2	–	–		–	5.5	–	–		4,7,9	–	5	2		
	t_{5-2-}	2	–	–		–	5.5	–	–		4,7,9	–	5	2		
Rise Time (20% to 80%)	t_{6+}	6	–	–	1.1	–	3.5	–	–		4,7	–	11	6		
Fall Time (20% to 80%)	t_{6-}	6	–	–	1.1	–	3.5	–	–		4,7	–	11	6		

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.



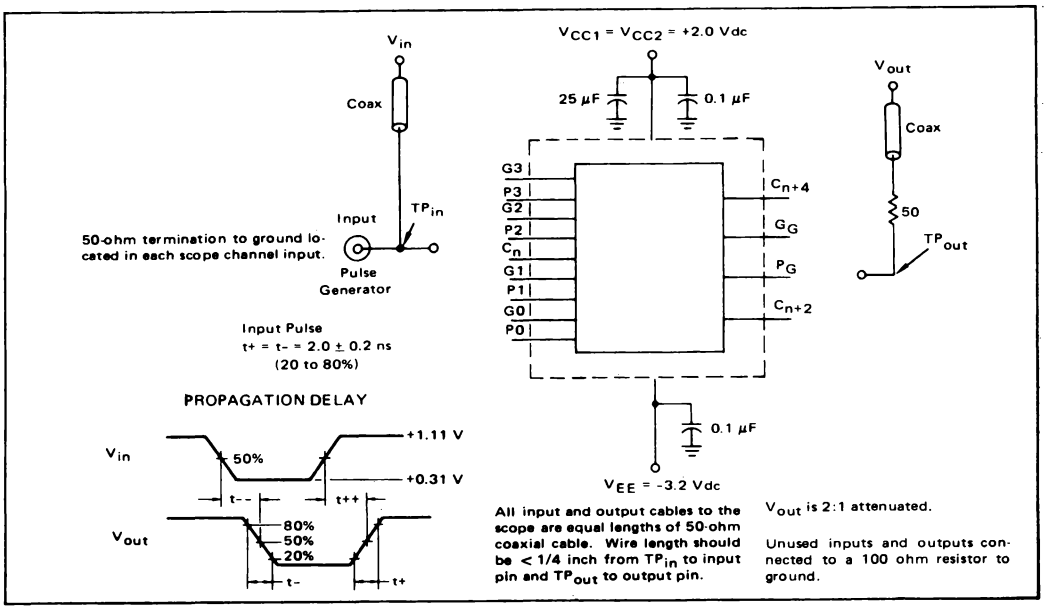


F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10579F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–	58	72	–	–	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	8,11,15	–	–	–	–	270	–	–	μAdc	8,11,15	–	–	–	12	4,5
		9,13	–	–	–	–	225	–	–		9,13	–	–	–		
		1,14	–	–	–	–	440	–	–		1,14	–	–	–		
		16	–	–	–	–	395	–	–		16	–	–	–		
		2	–	–	–	–	355	–	–		2	–	–	–		
	I_{inL}	8	–	–	0.5	–	–	–	–	μAdc	–	8	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	8,9,11,13	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	–	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	1	–	9	–	12	4,5
		6		–		–	–		–		9,16	–	13	–		
		6		–		–	–		–		9,13	–	16	–		
		6		–		–	–		–		9	–	17	–		
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	1	–	–	9	12	4,5
		6	–		–	–		–			9	–	–	17		
		6	–		–	–		–			9	–	–	13		
		6	–		–	–		–			9,13	–	–	16		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{15+10+}	10	–	–	1.0	–	4.5	–	–	ns	8,11	–	15	10	12	4,5
	t_{15-10-}	10	–	–		–	4.5	–	–		8,11	–	15	10		
	t_{9+6+}	6	–	–		–	5.5	–	–		8,11,13	–	9	6		
	t_{9-6-}	6	–	–		–	5.5	–	–		8,11,13	–	9	6		
Rise Time (20% to 80%)	t_{10+}	10	–	–	1.1	–	3.5	–	–		8,11	–	15	10		
Fall Time (20% to 80%)	t_{10-}	10	–	–	1.1	–	3.5	–	–		8,11	–	15	10		

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

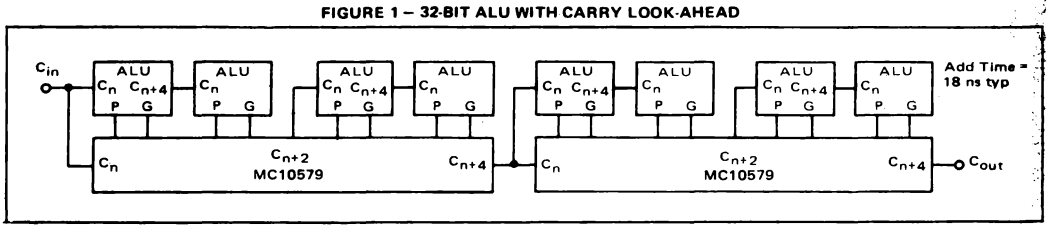


APPLICATION INFORMATION

The MC10579 is a high speed, low power, standard MECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10581 4-bit ALU directly, or with the MC10580 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

When used with the MC10581, the MC10579 performs a second order or higher look-ahead. Figure 2 shows a 16-bit look-ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques, to 18 nanoseconds with carry look-ahead techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10579 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

FIGURE 1 – 32-BIT ALU WITH CARRY LOOK-AHEAD



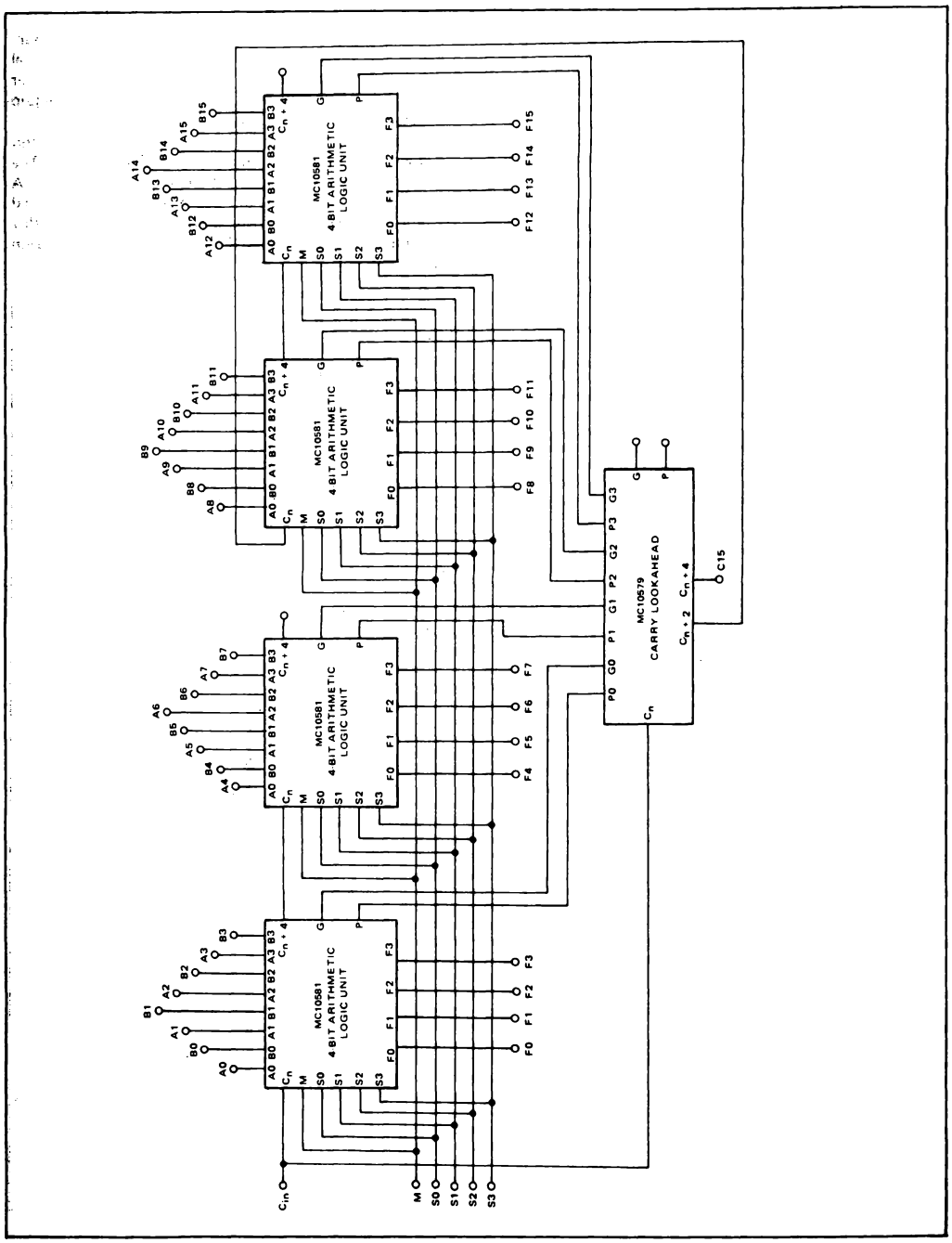


FIGURE 2 – 16-BIT FULL LOOK-AHEAD CARRY ARITHMETIC LOGIC UNIT

MC10580

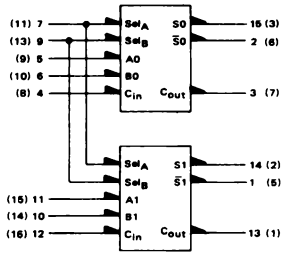
P_D = 360 mW typ/pkg (No Load)

t_{pd}(typ): C_{in} to C_{out} = 2.2 ns
A0 to S0 = 4.5 ns
A0 to C_{out} = 4.5 ns

The MC10580 is a high speed, low power general-purpose adder/subtractor. It is designed to be used in special purpose adders/subtractors or in high speed multiplier arrays. The MC10580 can be used in any piece of equipment where these operations are necessary.

Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, $\overline{\text{Sum}}$, and Carry-out. The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B. The speed is very fast, with Carry-in to Carry-out propagation delay of 2.2 ns and Operand in to Sum or Carry-out propagation delay of 4.5 ns.

POSITIVE LOGIC

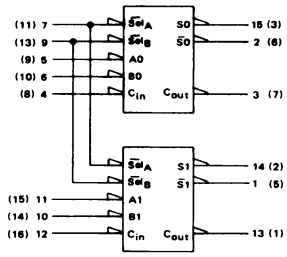


Positive Logic Only

$A' = \overline{A \oplus Sel_A} = A \odot Sel_A$

$B' = \overline{B \oplus Sel_B} = B \odot Sel_B$

NEGATIVE LOGIC



Both Positive and Negative Logic

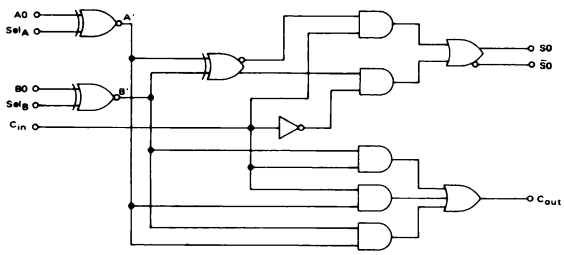
$S = \bar{C}_{in}(\bar{A}'B' + A'\bar{B}') + C_{in}(A'B' + \bar{A}'\bar{B}')$

$C_{out} = C_{in}A' + C_{in}B' + A'B'$

CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

POSTIVE LOGIC DIAGRAM — 1/2 Of Circuit Shown



FUNCTION SELECT TABLE

Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

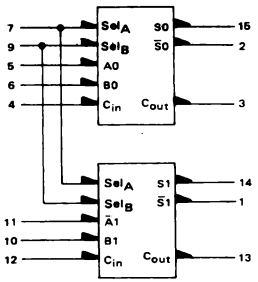
TRUTH TABLE

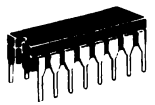
FUNCTION	INPUTS					OUTPUTS		
	Sel_A	Sel_B	A0	B0	C_{in}	S0	S̄0	C_{out}
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	H
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	L
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	H
	H	L	H	H	H	L	H	H
REVERSE SUBTRACT	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	H	L	H
	L	H	L	H	H	L	H	L
	L	H	H	L	L	H	L	L
	L	H	H	L	H	L	H	H
	L	H	H	H	L	L	H	H
	L	H	H	H	H	H	L	L
	L	L	L	L	L	H	L	H
	L	L	L	L	H	L	H	L
	L	L	L	H	L	H	L	L
	L	L	L	H	H	L	H	H
	L	L	H	L	L	H	L	H
	L	L	H	L	H	L	H	L
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

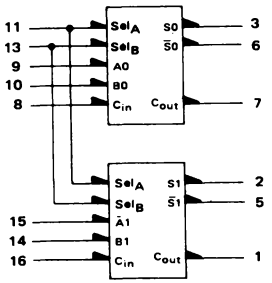
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

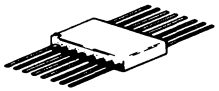
Characteristic	Symbol	Pin Under Test	MC10580L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	95	–	70	86	–	95	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	4	–	630	–	–	370	–	370	μAdc	–	–	–	–	8	16
		5	–	374	–	–	220	–	220		–	–	–	–		
		6	–	374	–	–	220	–	220		–	–	–	–		
		7	–	493	–	–	290	–	290		–	–	–	–		
		9	–	493	–	–	290	–	290		–	–	–	–		
		10	–	374	–	–	220	–	220		–	–	–	–		
		11	–	374	–	–	220	–	220		–	–	–	–		
		12	–	630	–	–	370	–	370		–	–	–	–		
	I_{inL}	All	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	7,9	–	–	–	8	16
		3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630		4,5,7,9	–	–	–		
		15	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630		4,7,9	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	5,7,9	–	–	–	8	16
		3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545		7,9	–	–	–		
		15	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545		7,9	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	7,9	–	–	4	8	16
		3	-1.100	–	-0.950	–	–	-0.845	–		4,7,9	–	5	–		
		15	-1.100	–	-0.950	–	–	-0.845	–		7,9	–	4	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	7,9	–	4	–	8	16
		3	–	-1.635	–	–	-1.600	–	-1.525		7,9	–	–	4		
		15	–	-1.635	–	–	-1.600	–	-1.525		4,7,9	–	5	–		
Switching Times Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Operand Input	t_{5+15+}	15	–	–	1.0	4.5	5.4	–	–	ns	7,9	–	5	15	8	16
	t_{6+15+}	15	–	–		4.5	5.4	–	–		7,9	–	6	15		
Carry-in Input	t_{4+15+}	15	–	–		2.2	3.3	–	–		7,9	–	4	15		
	t_{4+3+}	3	–	–		2.2	3.3	–	–		5,7,9	–	4	3		
Select Input	t_{7+15+}	15	–	–		4.5	5.4	–	–		4,9	–	7	15		
	t_{9+15+}	15	–	–		4.5	5.4	–	–		7,4	–	9			
Rise Time (20 to 80%)	t_{15+}	15	–	–	1.1	2.0	3.7	–	–		7,9	–	5			
Fall Time	t_{15-}	15	–	–	1.1	2.0	3.7	–	–		7,9	–	5			

*Individually apply $V_{IL\ min}$ to pin under test.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





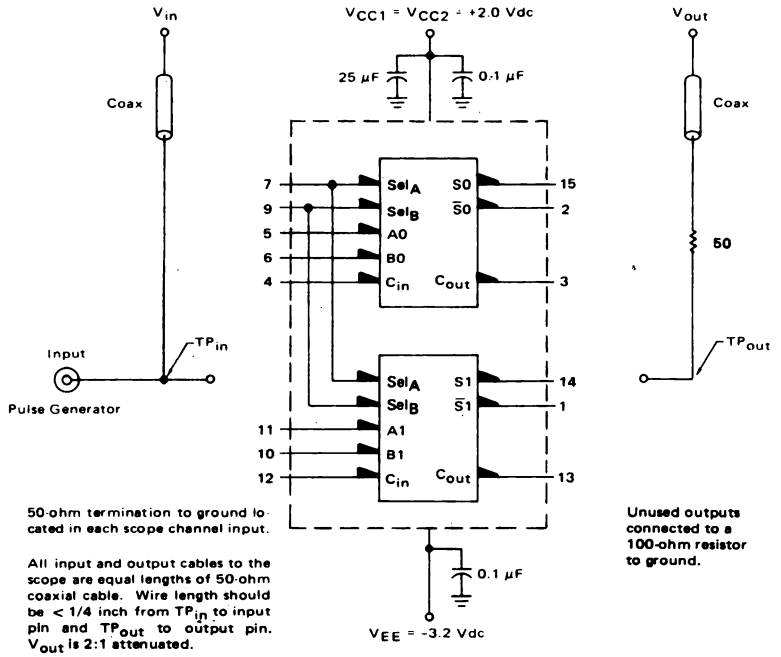
F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

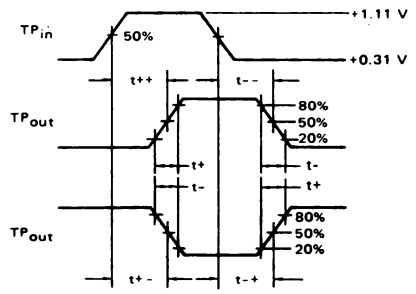
Characteristic	Symbol	Pin Under Test	MC10580F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	96	–	70	86	–	95	mAdc	–	–	–	–	12	4
Input Current	I_{inH}	8	–	630	–	–	370	–	370	µAdc	–	–	–	–	12	4
		9	–	374	–	–	220	–	220		–	–	–	–		
		10	–	374	–	–	220	–	220		–	–	–	–		
		11	–	493	–	–	290	–	290		–	–	–	–		
		13	–	493	–	–	290	–	290		–	–	–	–		
		14	–	374	–	–	220	–	220		–	–	–	–		
		15	–	374	–	–	220	–	220		–	–	–	–		
		16	–	630	–	–	370	–	370		–	–	–	–		
	I_{inL}	All	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	12	4
Logic "1" Output Voltage	V_{OH}	3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	8,11,13	–	–	–	12	4
		6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630		11,13	–	–	–		
		7	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630		8,9,11,13	–	–	–		
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	11,13	–	–	–	12	4
		6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545		9,11,13	–	–	–		
		7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545		11,13	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	11,13	–	8	–	12	4
		6	-1.100	–	-0.950	–	–	-0.845	–		11,13	–	–	8		
		7	-1.100	–	-0.950	–	–	-0.845	–		8,11,13	–	9	–		
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	8,11,13	–	9	–	12	4
		6	–	-1.635	–	–	-1.600	–	-1.525		11,13	–	8	–		
		7	–	-1.635	–	–	-1.600	–	-1.525		11,13	–	–	8		
Switching Times Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Operand Input	t_{9+3+}	3	–	–	1.0	4.5	5.4	–	–	ns	11,13	–	9	3	12	4
	t_{10+3+}	3	–	–		4.5	5.4	–	–		11,13	–	10	3		
Carry-in Input	t_{8+3+}	3	–	–		2.2	3.3	–	–		11,13	–	8	3		
	t_{8+7+}	7	–	–		2.2	3.3	–	–		9,11,13	–	8	7		
Select Input	t_{11+3+}	3	–	–		4.5	5.4	–	–		8,13	–	11	3		
	t_{13+3+}	3	–	–		4.5	5.4	–	–		8,11	–	13			
Rise Time (20 to 80%)	t_{3+}	3	–	–	1.1	2.0	3.7	–	–		11,13	–	9			
Fall Time	t_{3-}	3	–	–	1.1	2.0	3.7	–	–		11,13	–	9			

*Individually apply $V_{IL\ min}$ to pin under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



PROPAGATION DELAY



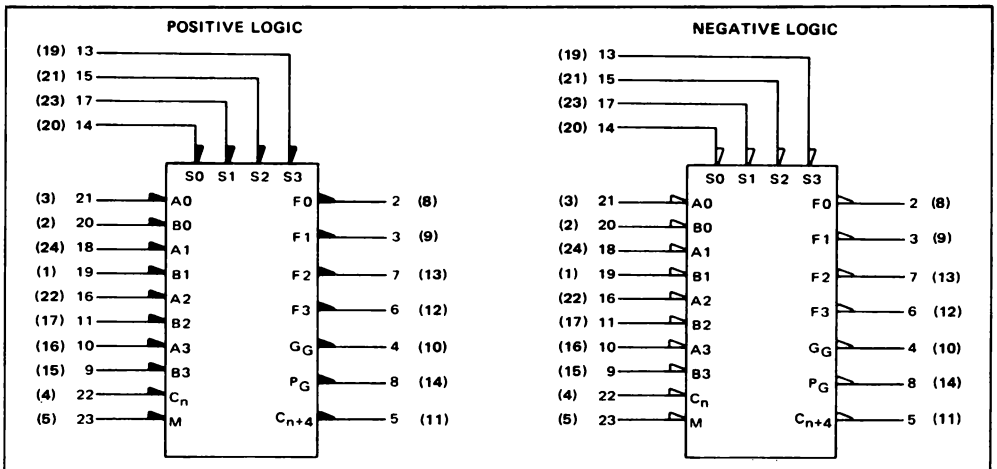
MC10581

The MC10581 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions.

Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast addition of very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10579, full-carry look-ahead, as a second order look ahead block, the MC10581 provides high speed arithmetic operations on very long words.



Numbers at end of terminals are pin numbers for L package (Case 620)
Numbers in parenthesis denotes pin numbers for F package (Case 650)

Case	V_{CC1}	V_{CC2}	V_{EE}
623	Pin 1	Pin 24	Pin 12
667	Pin 7	Pin 6	Pin 18

P_D = 600 mW typ/pkg (No Load)

t_{pd} (typ): A1 to F = 6.5 ns; C_n to C_{n+4} = 3.1 ns; A1 to P_G = 5.0 ns; A1 to G_G = 4.5 ns; A1 to C_{n+4} = 5.0 ns

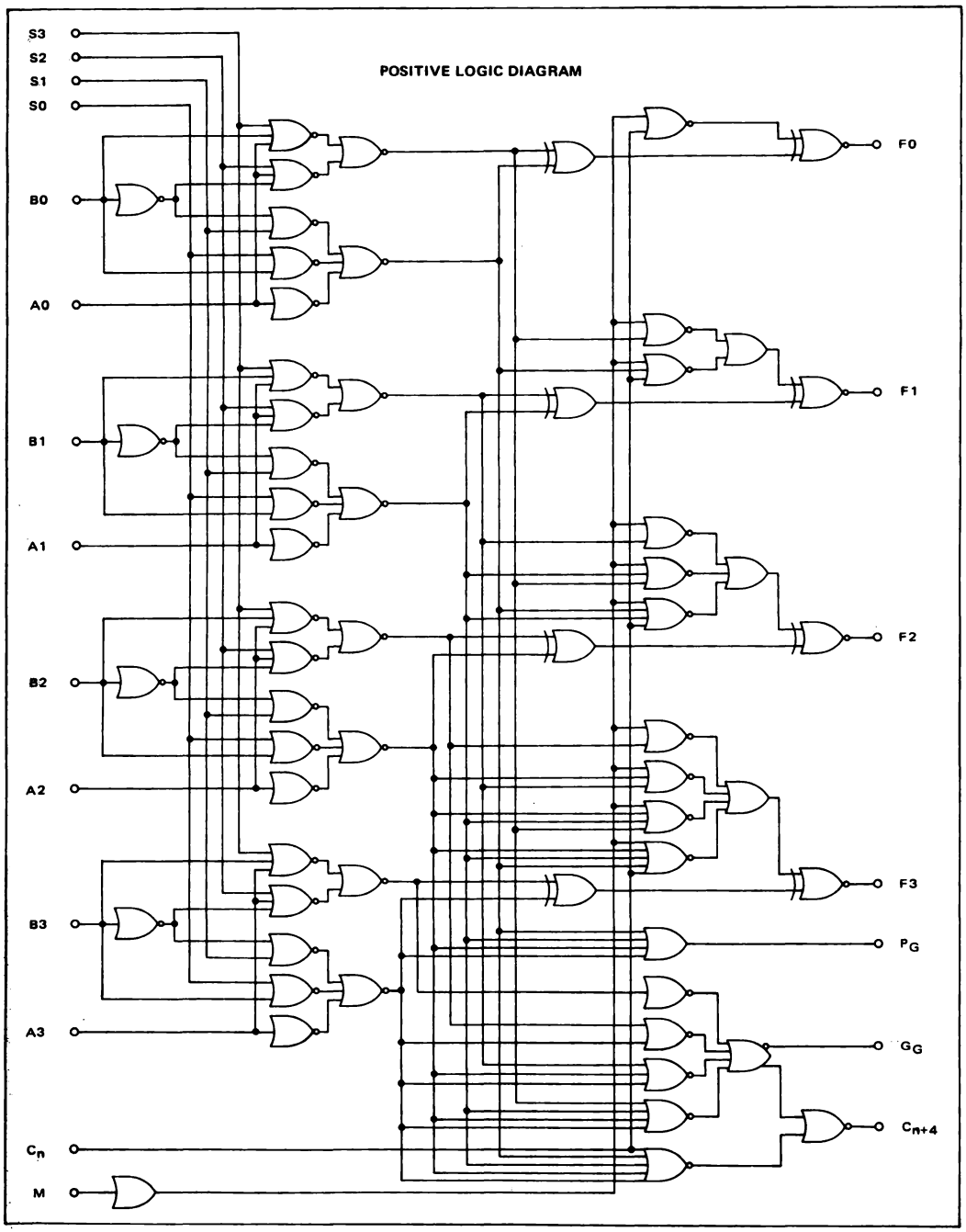
POSITIVE LOGIC

Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	F = $\bar{A}$	F = A plus 0
L	L	L	H	F = $\bar{A} + \bar{B}$	F = A plus (A • $\bar{B}$)
L	L	H	L	F = $\bar{A} + B$	F = A plus (A • B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	F = $\bar{A} \bullet \bar{B}$	F = (A + B) plus 0
L	H	L	H	F = $\bar{B}$	F = (A + B) plus (A • $\bar{B}$)
L	H	H	L	F = A ⊕ B	F = A plus B
L	H	H	H	F = A + $\bar{B}$	F = A plus (A + $\bar{B}$)
H	L	L	L	F = $\bar{A} \bullet B$	F = (A + $\bar{B}$) plus 0
H	L	L	H	F = A ⊙ B	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\bar{B}$) plus (A • B)
H	L	H	H	F = A + B	F = A plus (A + $\bar{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	F = A • $\bar{B}$	F = (A • $\bar{B}$) minus 1
H	H	H	L	F = A • B	F = (A • B) minus 1
H	H	H	H	F = A	F = A minus 1

NEGATIVE LOGIC

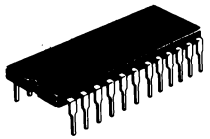
Function Select S3	S2	S1	S0	Logic Functions M is High F	Arithmetic Operation M is Low C_n of LSB must be High F
L	L	L	L	F = $\bar{A}$	F = A minus 1
L	L	L	H	F = $\overline{\bar{A} + \bar{B}}$	F = A plus (A + $\bar{B}$)
L	L	H	L	F = $\bar{A} \bullet B$	F = A plus (A + B)
L	L	H	H	F = Logical "0"	F = A times 2
L	H	L	L	F = $\overline{\bar{A} \bullet \bar{B}}$	F = (A + B) minus 1
L	H	L	H	F = $\bar{B}$	F = (A + B) plus (A + $\bar{B}$)
L	H	H	L	F = A ⊙ B	F = A plus B
L	H	H	H	F = A • $\bar{B}$	F = A plus (A • B)
H	L	L	L	F = $\bar{A}$ + B	F = (A • $\bar{B}$) minus 1
H	L	L	H	F = A ⊙ B	F = A minus B minus 1
H	L	H	L	F = B	F = (A • $\bar{B}$) plus (A + B)
H	L	H	H	F = A • B	F = (A • $\bar{B}$) plus A
H	H	L	L	F = Logical "1"	F = minus 1 (two's complement)
H	H	L	H	F = A + $\bar{B}$	F = (A + $\bar{B}$) plus 0
H	H	H	L	F = A + B	F = (A + B) plus 0
H	H	H	H	F = A	F = A plus 0

See General Information section for packaging and maximum ratings.


POSITIVE LOGIC DIAGRAM
S3
S2
S1
S0
B0
A0
B1
A1
B2
A2
B3
A3
Cn
M
F0
F1
F2
F3
PG
GG
Cn+4

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.



L SUFFIX
CERAMIC PACKAGE
CASE 623

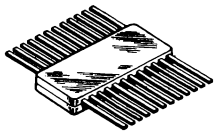
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10581L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	160	–	–	145	–	160	mAdc	–	–	–	–	12	1,24
Input Current	I_{inH}	9	–	420	–	–	245	–	245	µAdc	9	–	–	–	12	1,24
		10	–	375	–	–	220	–	220		10	–	–	–		
		11	–	420	–	–	245	–	245		11	–	–	–		
		13	–	340	–	–	200	–	200		13	–	–	–		
		14	–	450	–	–	265	–	265		14	–	–	–		
		15	–	450	–	–	265	–	265		15	–	–	–		
		16	–	375	–	–	220	–	220		16	–	–	–		
		17	–	450	–	–	265	–	265		17	–	–	–		
		18	–	375	–	–	220	–	220		18	–	–	–		
		19	–	420	–	–	245	–	245		19	–	–	–		
		20	–	420	–	–	245	–	245		20	–	–	–		
		21	–	375	–	–	220	–	220		21	–	–	–		
		22	–	495	–	–	290	–	290		22	–	–	–		
		23	–	340	–	–	200	–	200		23	–	–	–		
Input Leakage Current	I_{inL}	9	0.5	–	0.5	–	–	0.3	–	µAdc	–	9	–	–	12	1,24
		10		–		–	–		–		–	10	–	–		
		11		–		–	–		–		–	11	–	–		
		13		–		–	–		–		–	13	–	–		
		14		–		–	–		–		–	14	–	–		
		15		–		–	–		–		–	15	–	–		
		16		–		–	–		–		–	16	–	–		
		17		–		–	–		–		–	17	–	–		
		18		–		–	–		–		–	18	–	–		
		19		–		–	–		–		–	19	–	–		
		20		–		–	–		–		–	20	–	–		
		21		–		–	–		–		–	21	–	–		
		22		–		–	–		–		–	22	–	–		
		23		–		–	–		–		–	23	–	–		
High Output Voltage	V_{OH}	*	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	*	*	–	–	12	1,24
Low Output Voltage	V_{OL}	*	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	*	*	–	–	12	1,24
High Threshold Voltage	V_{OHA}	*	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	**	**	12	1,24
Low Threshold Voltage	V_{OLA}	*	–	-1.635	–	–	-1.660	–	-1.525	Vdc	–	–	**	**	12	1,24

*Test all input-output combinations according to Function Table.
**For threshold level test, apply threshold input level to only one input pin at a time.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts.



F SUFFIX
CERAMIC PACKAGE
CASE 652

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10581F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	18	–	160	–	116	145	–	160	mAdc	–	–	–	–	18	6,7
Input Current	I_{inH}	15	–	420	–	–	245	–	245	µAdc	15	–	–	–	18	6,7
		16	–	375	–	–	220	–	220		16	–	–	–		
		17	–	420	–	–	245	–	245		17	–	–	–		
		19	–	340	–	–	200	–	200		19	–	–	–		
		20	–	450	–	–	265	–	265		20		–	–		
		21	–	450	–	–	265	–	265		21	–	–	–		
		22	–	375	–	–	220	–	220		22	–	–	–		
		23	–	450	–	–	265	–	265		23	–	–	–		
		24	–	375	–	–	220	–	220		24		–	–		
		1	–	420	–	–	245		245		1	–	–	–		
		2	–	420	–	–	245	–	245		2	–	–	–		
		3	–	375	–	–	220	–	220		3	–	–	–		
		4	–	495	–	–	290	–	290		4	–	–	–		
		5	–	340	–	–	200	–	200		5	–	–	–		
Input Leakage Current	I_{inL}	15	0.5	–	0.5	–	–	0.3	–	µAdc	–	15	–	–	18	6,7
		16		–		–	–		–		–	16	–	–		
		17		–		–	–		–		–	17	–	–		
		19		–		–	–		–		–	19	–	–		
		20				–	–		–		–	20	–	–		
		21		–		–	–		–		–	21	–	–		
		22		–		–	–		–		–	22	–	–		
		23		–		–	–		–		–	23	–	–		
		24		–		–	–		–		–	24	–	–		
		1		–		–	–		–		–	1	–	–		
		2				–	–		–		–	2	–	–		
		3		–		–	–		–		–	3	–	–		
		4		–		–	–		–		–	4	–	–		
		5		–		–	–		–		–	5	–	–		
High Output Voltage	V_{OH}	*	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	*	*	–	–	18	6,7
Low Output Voltage	V_{OL}	*	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	*	*	–	–	18	6,7
High Threshold Voltage	V_{OHA}	*	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	**	**	18	6,7
Low Threshold Voltage	V_{OLA}	*	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	**	**	18	6,7

*Test all input-output combinations according to Function Table.
**For threshold level test, apply threshold input level to only one input pin at a time.

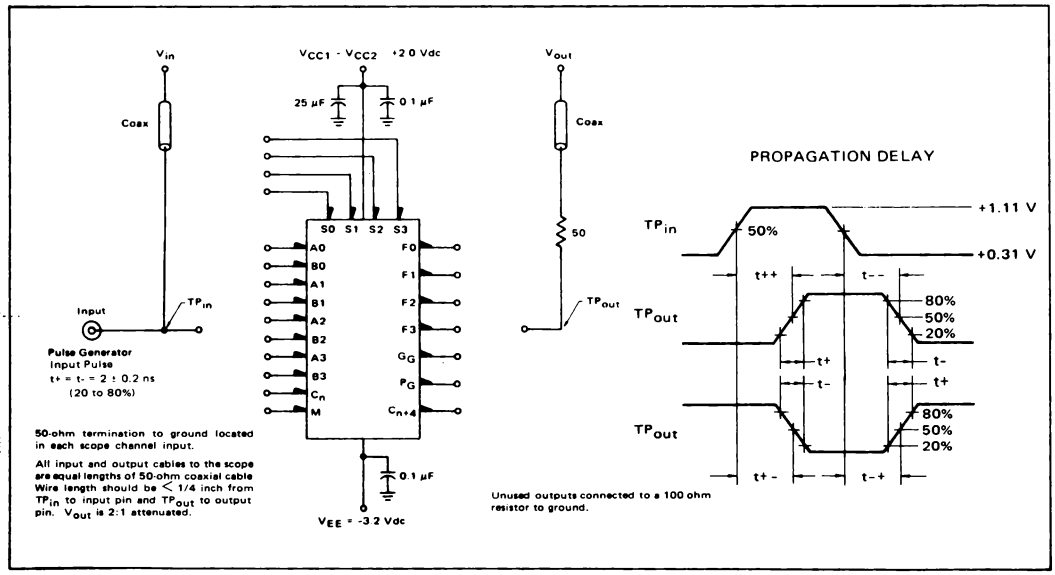
ELECTRICAL CHARACTERISTICS (CONT')

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics							
					-55°C *		+25°C			+125°C *		
					Min	Max	Min	Typ	Max	Min	Max	Unit
Propagation Delay	t++, t--	B1	P_G	S0, S3	1.8	7.6	2.0	6.0	7.5	1.6	7.6	ns
Rise Time, Fall Time	t+, t-	B1	P_G	S0,S3	1.0	3.5	1.1	2.0	3.5	0.9	3.5	ns
Propagation Delay	t++, t--	B1	G_G	S3, C_n	1.9	8.1	2.0	6.0	8.0	2.0	8.1	ns
Rise Time, Fall Time	t+, t-	B1	G_G	S3.C_n	1.3	5.0	1.5	3.0	5.0	1.3	5.0	ns
Propagation Delay	t+-, t-+	B1	C_{n+4}	S3, C_n	1.9	8.1	2.0	6.0	8.0	1.9	8.1	ns
Rise Time, Fall Time	t+, t-	B1	C_{n+4}	S3.C_n	0.9	3.0	1.0	2.0	3.0	0.9	3.0	ns
Propagation Delay	t++, t+-	M	F1	–	2.8	10.3	3.0	6.5	10	2.8	10.2	ns
Rise Time, Fall Time	t+, t-	M	F1	–	1.3	5.2	1.5	4.0	5.0	1.3	5.2	ns
Propagation Delay	t+-, t-+	S1	F1	A1, B1	2.7	10.2	3.0	6.5	10	2.6	10.2	ns
Rise Time, Fall Time	t+, t-	S1	F1	A1, B1	1.3	5.2	1.5	3.0	5.0	1.3	5.2	ns
Propagation Delay	t-+, t+-	S1	P_G	A3, B3	1.9	8.1	2.0	6.0	8.0	1.8	8.1	ns
Rise Time, Fall Time	t+, t-	S1	P_G	A3, B3	1.0	5.1	1.1	3.0	5.0	1.0	5.1	ns
Propagation Delay	t+-, t-+	S1	C_{n+4}	A3, B3	1.9	9.1	2.0	6.0	9.0	1.8	9.1	ns
Rise Time, Fall Time	t+, t-	S1	C_{n+4}	A3, B3	1.0	5.1	1.1	3.0	5.0	1.0	5.1	ns
Propagation Delay	t+-, t-+	S1	G_G	A3, B3	1.7	9.2	2.0	6.0	9.0	1.7	9.1	ns
Rise Time, Fall Time	t+, t-	S1	G_G	A3, B3	0.8	6.2	0.8	3.0	6.0	0.8	6.2	ns
Propagation Delay	t++, t--	C_n	C_{n+4}	A0,A1,A2,A3	1.0	5.1	1.1	3.1	5.0	0.9	5.1	ns
Rise Time, Fall Time	t+,t-	C_n	C_{n+4}	A0,A1,A2,A3	0.9	3.1	1.0	2.0	3.0	0.3	3.1	ns
Propagation Delay	t++, t+-	C_n	F1	A0	1.9	7.1	2.0	4.5	7.0	2.0	7.1	ns
	t-+, t--	↓	↓	↓	1.9	7.1	2.0	4.5	7.0	2.0	7.1	↓
Rise Time, Fall Time	t+, t-	↓	↓	↓	1.3	5.2	1.5	3.0	5.0	1.3	5.2	↓
Propagation Delay	t++, t+-	A1	F1	–	2.9	10.1	3.0	6.5	10	2.8	10.2	ns
	t-+, t- -	↓	↓		2.9	10.1	3.0	6.5	10	2.8	10.2	↓
Rise Time, Fall Time	t+, t-	↓	↓	–	1.3	5.2	1.5	3.0	5.0	1.3	5.2	↓
Propagation Delay	t++, t--	A1	P_G	S0,S3	1.8	6.6	2.0	5.0	6.5	1.8	6.5	ns
Rise Time, Fall Time	t+, t-	A1	P_G	S0,S3	0.9	3.5	1.1	2.0	3.5	1.0	3.6	ns
Propagation Delay	t++, t--	A1	G_G	A0,A2,A3,C_n	1.9	7.1	2.0	4.5	7.0	2.0	7.1	ns
Rise Time, Fall Time	t+, t-	A1	G_G	A0,A2,A3,C_n	1.3	5.2	1.5	4.0	5.0	1.3	5.2	ns
Propagation Delay	t+-, t-+	A1	C_{n+4}	A0,A2,A3,C_n	2.0	7.1	2.0	5.0	7.0	1.9	7.1	ns
Rise Time, Fall Time	t+, t-	A1	C_{n+4}	A0,A2,A3,C_n	0.9	3.0	1.0	2.0	3.0	0.9	3.1	ns
Propagation Delay	t++, t-+	B1	F1	S3, C_n	2.9	11.1	3.0	8.0	11	2.7	11.2	ns
Rise Time, Fall Time	t+, t-	B1	F1	S3,C_n	1.3	5.2	1.5	3.5	5.0	1.3	5.2	ns

†Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
$V_{CC1} = V_{CC2} = +2.0$ Vdc, $V_{EE} = -3.2$ Vdc

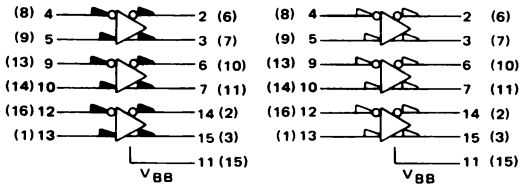
*For L Suffix only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



HIGH SPEED TRIPLE
LINE RECEIVER

MC10616



Numbers at end of terminals are pin numbers for L package (Case 620).
Numbers in parenthesis denotes pin numbers for F package (Case 650).

Case	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

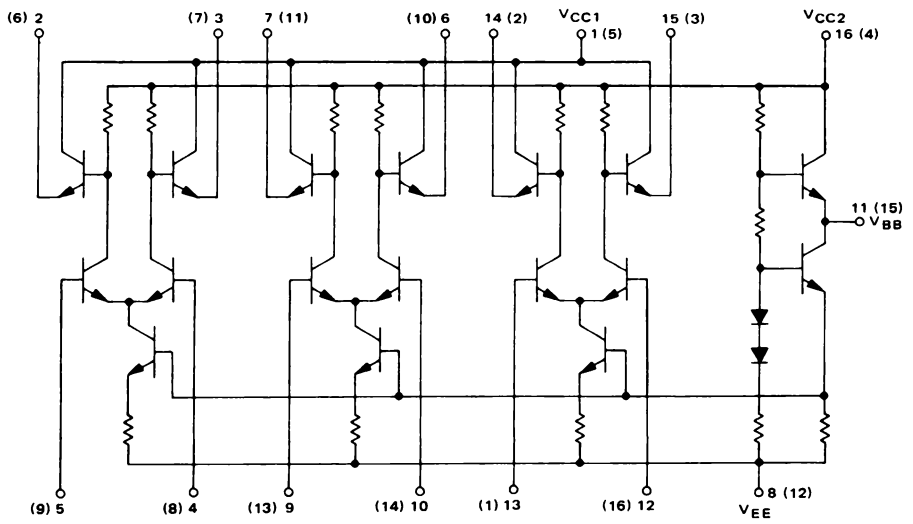
The MC10616 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10616 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 1.8 ns typ (Single ended)
= 1.5 ns typ (Differential)

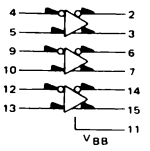
CIRCUIT SCHEMATIC

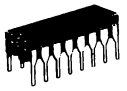


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner





L SUFFIX
CERAMIC PACKAGE
CASE 620

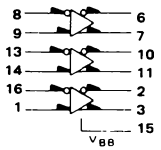
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	From	-5.2
+25°C	-0.780	-1.850	-1.106	-1.475	Pin	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	11	-5.2

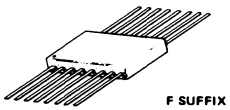
Characteristic	Symbol	Pin Under Test	MC10616L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	28	–	20	25	–	28	mAdc	–	4,9,12	–	–	5,10,13	8	1,16
Input Current	I_{inH}	4	–	195	–	–	115	–	115	µAdc	4	9,12	–	–	5,10,13	8	1,16
	I_{CBO}	4	–	1.5	–	–	1.0	–	1.0	µAdc	–	9,12	–	–	5,10,13	8,4	1,16
		9	–	1.5	–	–	1.0	–	1.0	µAdc	–	4,12	–	–	5,10,13	8,9	1,16
High Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	4	9,12	–	–	5,10,13	8	1,16
		3	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	9,12	4	–	–	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	9,12	4	–	–	5,10,13	8	1,16
		3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	4	9,12	–	–	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	9,12	4	–	5,10,13	8	1,16
		3	-1.100	–	-0.950	–	–	-0.845	–	Vdc	9,12	–	–	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	9,12	–	4	5,10,13	8	1,16
		3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	9,12	–	4	–	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	-1.440	-1.320	-1.350	–	-1.230	-1.240	-1.120	Vdc	–	–	–	–	5,10,13	8	1,16
Switching Times (50-ohm Load)													Pulse In	Pulse Out		-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{4+2+}	2	–	–	1.0	1.8*	2.5	–		ns	–	–	4	2	5,10,13	8	1,16
	t_{4-2-}	2	–	–				–	–		–	–		2			
	t_{4+3-}	3	–	–				–	–		–	–		3			
	t_{4-3+}	3	–	–				–	–		–	–		3			
Rise Time (20% to 80%)	t_{2+}	2	–	–		1.5		–	–		–	–		2			
	t_{3+}	3	–	–				–	–		–	–		3			
Fall Time (20% to 80%)	t_{2-}	2	–	–				–	–		–	–		2			
	t_{3-}	3	–	–				–	–		–	–		3			

*Delay is 1.5 ns when inputs are driven differentially
Delay is 1.8 ns when inputs are driven single ended

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner





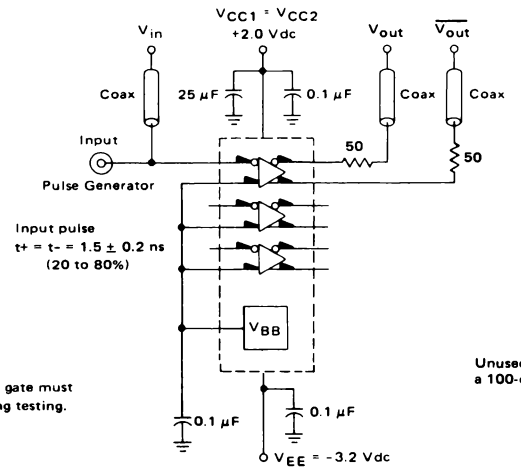
F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	From	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	Pin	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	15	-5.2

Characteristic	Symbol	Pin Under Test	MC10616F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	28	–	20	25	–	28	mAdc	–	8, 13, 16	–	–	1,9,14	12	4,5
Input Current	I_{inH}	8	–	195	–	–	115	–	115	µAdc	8	13,16	–	–	1,9,14	12	4,5
	I_{CBO}	8	–	1.5	–	–	1.0	–	1.0	µAdc	–	13,16	–	–	1,9,14	8,12	4,5
		13	–	1.5	–	–	1.0	–	1.0	µAdc	–	8,13	–	–	1,9,14	12,13	4,5
High Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	8	13,16	–	–	1,9,14	12	4,5
		7	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	13,16	8	–	–	1,9,14	12	4,5
Low Output Voltage	V_{OL}	6	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	13,16	8	–	–	1,9,14	12	4,5
		7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	8	13,16	–	–	1,9,14	12	4,5
High Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845		Vdc	–	13,16	8	–	1,9,14	12	4,5
		7	-1.100	–	-0.950	–	–	-0.845	–	Vdc	13,16	–	–	8	1,9,14	12	4,5
Low Threshold Voltage	V_{OLA}	6	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	13,16	–	8	1,9,14	12	4,5
		7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	13,16	–	8	–	1,9,14	12	4,5
Reference Voltage	V_{BB}	15	-1.440	-1.320	-1.350	–	-1.230	-1.240	-1.120	Vdc	–	–	–	–	1,9,14	8	4,5
Switching Times (50-ohm Load)													Pulse In	Pulse Out		-3.2 Vdc	+2.0 Vdc
Propagation Delay	$t_{8^+6^+}$	6	–	–	1.0	1.8*	2.5	–		ns		–	8	6	1,9,14	12	4,5
	t_{8-6-}	6	–	–				–	–		–	–		6			
	t_{8+7-}	7	–	–				–	–			–		7			
	t_{8-7+}	7	–	–				–	–		–	–		7			
Rise Time (20% to 80%)	t_{6+}	6	–	–		1.5		–			–	–		6			
	t_{7+}	7	–	–				–				–		7			
Fall Time (20% to 80%)	t_{6-}	6	–	–				–	–		–	–		6			
	t_{7-}	7	–	–				–	–			–		7			

*Delay is 1.5 ns when inputs are driven differentially
Delay is 1.8 ns when inputs are driven single ended

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



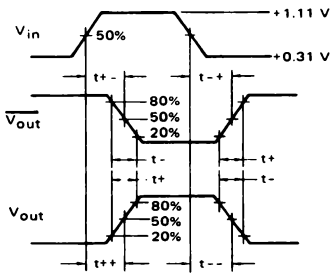
One input from each gate must be tied to V_{BB} during testing.

Unused outputs connected to a 100-ohm resistor to ground.

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<$1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

PROPAGATION DELAY



HIGH SPEED DUAL TYPE D
MASTER-SLAVE
FLIP-FLOP

MC10631

The MC10631 is a dual master-slave type D flip-flop. Asynchronous inputs Set (S) and Reset (R) override the Clock (C_C) and Clock Enable ($\overline{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

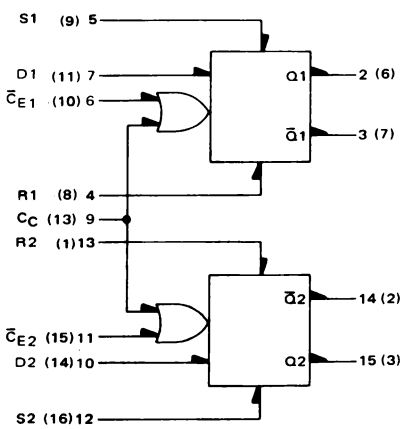
C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care
$C = \overline{C}_E + C_C$
A clock H is a clock transition from a low to a high state.

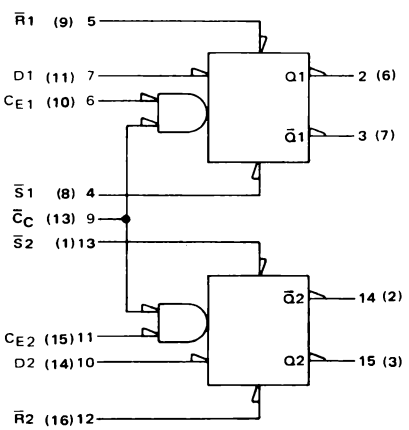
CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

P_D = 270 mW typ/pkg (No Load)
f_{Tog} = 225 MHz typ

POSITIVE LOGIC



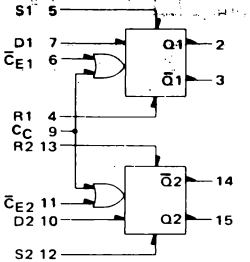
NEGATIVE LOGIC

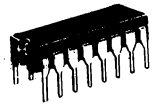


Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

● Test Temperature

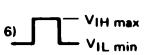
Ter	
	-55°C
	+25°C
	+125°C

TEST VOLTAGE VALUES (Vdc ± 1%)				
V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-0.880	-1.920	-1.255	-1.510	-5.2
-0.780	-1.850	-1.105	-1.475	-5.2
-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10631L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	72	–	92	65	–	72	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	700	–	–	410	–	410	µAdc	4	–	–	–	8	1, 16
		5	–	700	–	–	410	–	410		5	–	–	–		
		6	–	375	–	–	220	–	220		6	–	–	–		
		7	–	375	–	–	220	–	220		7	–	–	–		
		9	–	495	–	–	290	–	290		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	8	1, 16
		6,7,9*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	5	–	–	–	8	1, 16
		2†	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	5	–	–	–	8	1, 16
		3†	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	5	–	8	1, 16
		2†	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	5	–	8	1, 16
		3†	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	7	9	8	1, 16
Switching Times (100-ohm load)											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input																
Propagation Delay	t_{9+2-}	2	–	–	1.5	2.0	3.3	–	–	ns	–	–	9	2	8	1, 16
	t_{6+2+}		–	–	1.5	2.0	3.3	–	–		7	–	6			
Rise Time (20 to 80%)	t_{2+}		–	–	1.0	1.3	3.1	–	–		7	–	9			
Fall Time (20 to 80%)	t_{2-}		–	–	1.0	1.3	3.1	–	–		–	–	9			
Set Input																
Propagation Delay	t_{5+2+}	2	–	–	1.1	2.0	3.3	–	–	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15	–	–				–	–		–	–	12	15		
	t_{5+3-}	3	–	–				–	–		–	–	6	3		
	t_{12+14-}	14	–	–				–	–		–	–	12	14		
Reset Input																
Propagation Delay	t_{4+2-}	2	–	–	1.1	2.0	3.3	–	–	ns	–	–	4	2	8	1, 16
	t_{13+15-}	15	–	–				–	–		–	–	13	15		
	t_{4+3+}	3	–	–				–	–		–	–	4	3		
	t_{13+14+}	14	–	–				–	–		–	–	13	14		
Setup Time	t_{setup}	7	–	–	1.0	0.75	–	–	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{hold}	7	–	–	0.75	-0.5	–	–	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	200	–	200	225	–	200	–	MHz	••	–	6	2	8	1, 16

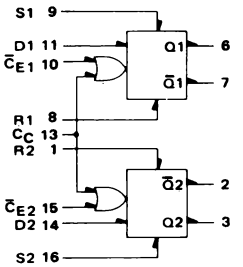
*Individually test each input; apply $V_{IL\ min}$ to pin under test.

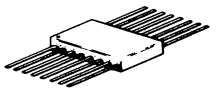
**Pin 3 is tied to pin 7 for these tests.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6) 

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

● Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
	TEST VOLTAGE VALUES Vdc ± 1%				
-55°C	-0.880	-1.920	-1.255	-1.610	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10631F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	62	–	45	65	–	62	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	8	–	700	–	–	410	–	410	µAdc	8	–	–	–	12	4,5
		9	–	700	–	–	410	–	410		9	–	–	–		
		10	–	375	–	–	220	–	220		10	–	–	–		
		11	–	375	–	–	220	–	220		11	–	–	–		
		13	–	495	–	–	290	–	290		13	–	–	–		
Input Leakage Current	I_{inL}	8,9*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	12	4,5
		10,11,13*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	9	–	–	–	12	4,5
		6†	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	11	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	9	–	–	–	12	4,5
		7†	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	11	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	9	–	12	4,5
		6†	-1.100	–	-0.960	–	–	-0.845	–	Vdc	–	–	11	13	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	9	–	12	4,5
		7†	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	11	13	12	4,5
											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse In	-3.2 Vdc	+2.0 Vdc
Switching Times (100-ohm load)	t_{13+6-}	6	–	–	1.5	2.0	3.3	–	–	ns	–	–	13	6	12	4,5
Clock Input Propagation Delay	t_{13+6+}	6	–	–				–	–		11	–	13			
	t_{10+6+}	6	–	–				–	–		11	–	10			
	t_{10+6-}	6	–	–				–	–		–	–	10			
Rise Time (20 to 80%)	t_{6+}	6	–	–	1.0	1.3	3.1	–	–		–	–	13			
Fall Time (20 to 80%)	t_{6-}	6	–	–	1.0	1.3	3.1	–	–		–	–	13			
Set Input Propagation Delay	t_{9+6+}	6	–	–	1.1	2.0	3.0	–	–	ns	–	–	9	6	12	4,5
	t_{16+3+}	3	–	–				–	–		–	–	16	3		
	t_{9+7-}	7	–	–				–	–		–	–	9	7		
	t_{16+2-}	2	–	–				–	–		–	–	16	2		
Reset Input Propagation Delay	t_{8+6-}	6	–	–	1.1	2.0	3.3	–	–	ns	–	–	8	6	12	4,5
	t_{1+3-}	3	–	–				–	–		–	–	1	3		
	t_{8+7+}	7	–	–				–	–		–	–	8	7		
	t_{1+2+}	2	–	–				–	–		–	–	1	2		
Setup Time	t_{setup}	11	–	–	1.0	0.75	–	–	–	ns	–	–	10,11	6	12	4,5
Hold Time	t_{hold}	11	–	–	0.75	-0.5	–	–	–	ns	–	–	10,11	6	12	4,5
Toggle Frequency (Max)	f_{Tog}	6	–	–	200	250	–	–	–	MHz	**	–	10	6	12	4,5

*Individually test each input; apply V_{IL} min to pin under test.

**Pin 7 is tied to pin 11 for these tests.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 10)

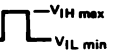


FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT

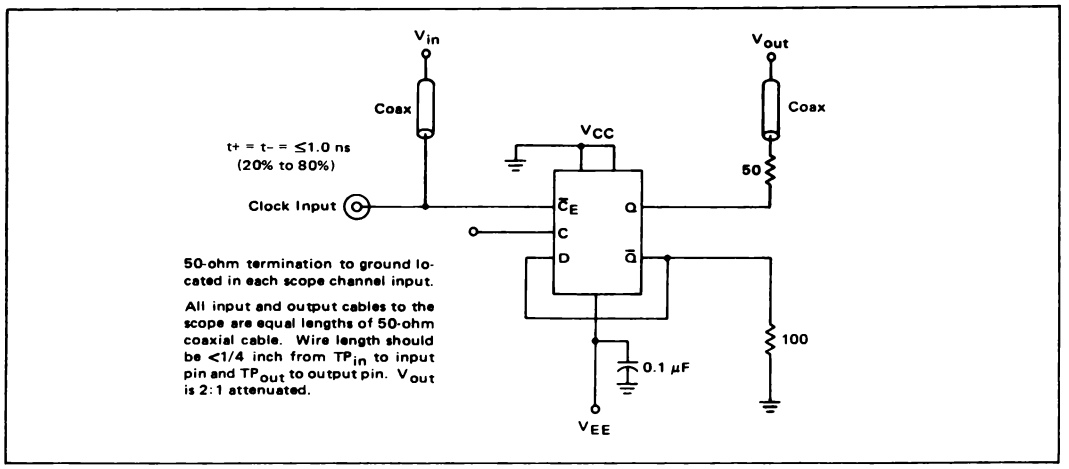
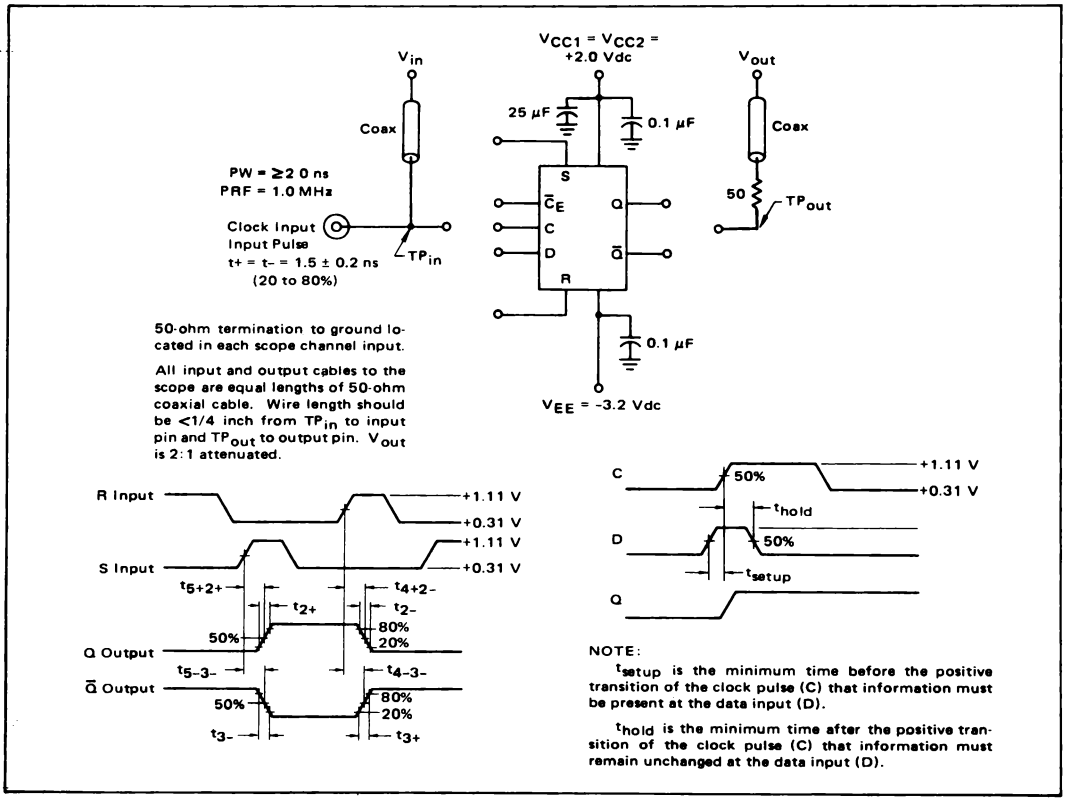


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

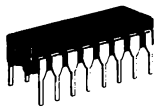
MCM10140
MCM10142
MCM10148

64-BIT RANDOM ACCESS MEMORY

The MCM10140, MCM10142 and MCM10148 are 64-Bit Random Access Memories (RAMs). They offer very high speed, full binary decoding, two chip enable inputs for easy memory expansion, and separate data input and data output pins.

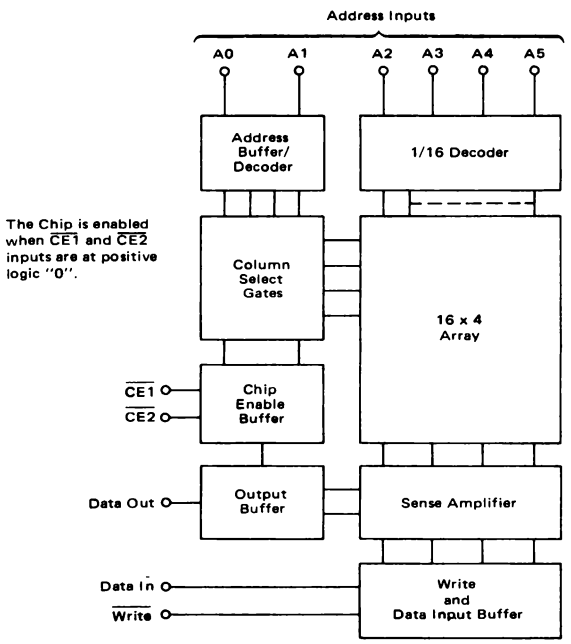
Organization of these memories is 64 one-bit words and they are packaged in standard 16-pin hermetic dual in-line packages.

MCM10142 and MCM10148 logic levels are fully compatible with the MECL 10,000 logic family and are specified for driving a 50 ohm load. The MCM10140 logic levels are compatible with the MECL 10,000 logic family except they are specified for driving a 90 ohm load.

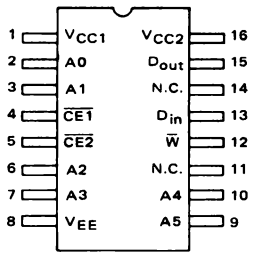


L SUFFIX
CERAMIC PACKAGE
CASE 620

BLOCK DIAGRAM



PIN ASSIGNMENT



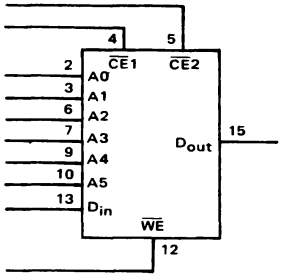
TRUTH TABLE

MODE	INPUT			OUTPUT
	CE	WE	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

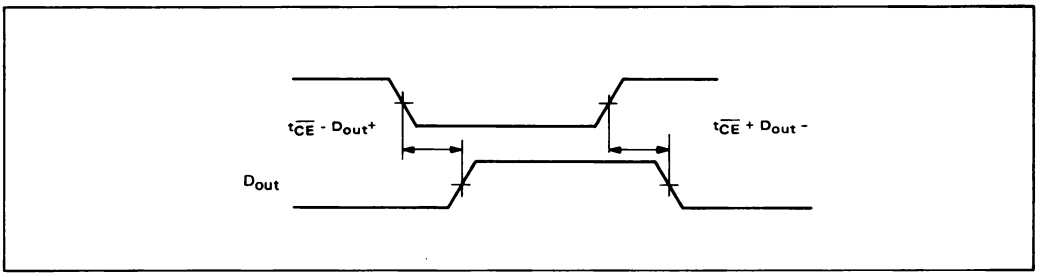


@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

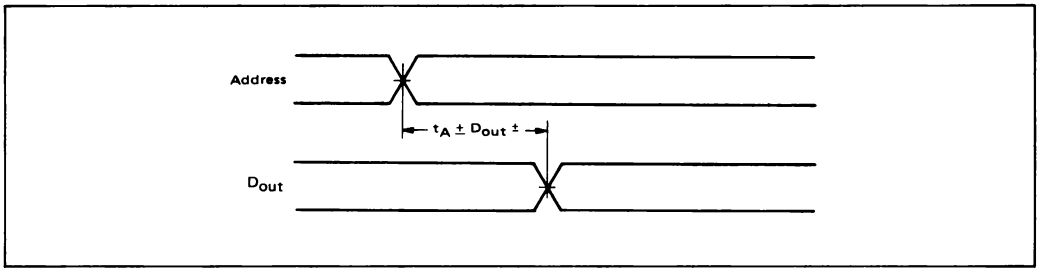
Characteristic		Pin Under Test	MCM10140, MCM10142, MCM10148 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	80	100	–	–	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	6	–	–	–	–	265	–	–	μAdc	6	–	–	–	8	16
		4	–	–	–	–	50	–	–		4	–	–	–		
	I_{inL}	6	–	–	0.5	–	–	–	–		–	6	–	–		
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-1.980	–	–	-0.910	–	Vdc	–	–	3,14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	3,14	8	1,16
Switching Times													Pulse In	Pulse Out	-3.2 V	+2.0 V
Access Times	$t_{\overline{CE}-D+}$	15	–	–	–	–	12	–	–	ns	–	–	4	15	8	1,16
Chip Enable	$t_{\overline{CE}+D-}$	15	–	–	–	–	12	–	–		–	–	4	15		
Address Inputs	t_{A+D+}	15	–	–	–	–	10*,15**	–	–		–	–	2	15		
	t_{A+D-}	15	–	–	–	–	10*,15**	–	–		–	–	2	15		
	t_{A-D+}	15	–	–	–	–	10*,15**	–	–		–	–	2	15		
	t_{A-D-}	15	–	–	–	–	10*,15**	–	–		–	–	2	15		
Write Pulse Width	$t_{W(\overline{WE})}$	12	–	–	–	–	10	–	–		–	–	13	12		
Chip Enable Pulse Width	$t_{W(CE)}$	4	–	–	–	–	13	–	–		–	–	13	4		
Write Strobe Mode Times Setup																
Data	$t_{setup(D\pm\overline{W}-)}$	12	–	–	–	–	0	–	–		–	–	2	12		
Chip Enable	$t_{setup(\overline{CE}-\overline{W}-)}$	12	–	–	–	–	3	–	–		–	–	4	12		
Address	$t_{setup(A\pm\overline{W}-)}$	12	–	–	–	–	5	–	–		–	–	4	12		
Hold																
Data	$t_{hold(\overline{W}+D\pm)}$	15	–	–	–	–	3	–	–		–	–	12	15		
Chip Enable	$t_{hold(\overline{W}+\overline{CE}+)}$	4	–	–	–	–	0	–	–		–	–	12	4		
Address	$t_{hold(\overline{W}+A\pm)}$	2	–	–	–	–	3	–	–		–	–	12	2		

*MCM10142
**MCM10140, MCM10148

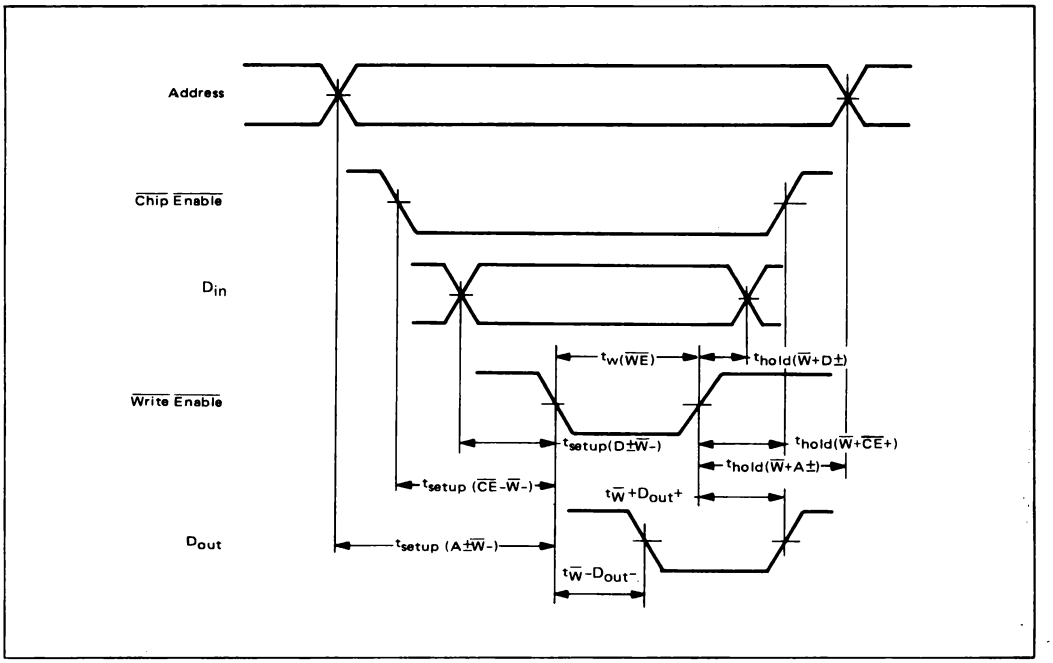
CHIP ENABLE ACCESS TIME



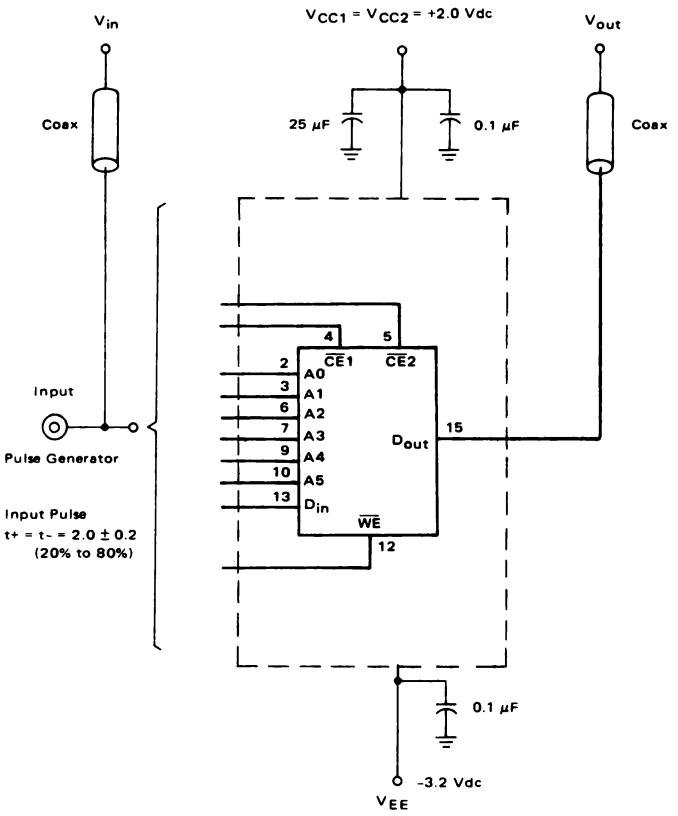
ADDRESS ACCESS TIME



WRITE STROBE MODE



SWITCHING TIME TEST CIRCUIT @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<$ 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

MCM10143

8 x 2 MULTIPORT REGISTER FILE (RAM)

The MC10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE

The word to be written is selected by addresses A_0–A_2. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by A_0–A_2.

READ

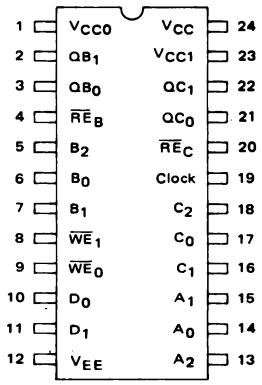
When the clock is high any two words may be read out simultaneously, as selected by addresses B_0–B_2 and C_0–C_2, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B_0–B_1), (C_0–C_1).

t_{pd}:
- Clock to Data out = 5 ns (typ) (Read Selected)
- Address to Data out = 10 ns (typ) (Clock High)
- $\overline{\text{Read Enable}}$ to Data out = 2.8 ns (typ) (Clock high, Addresses present)

P_D = 610 mW/pkg (typ no load)

L SUFFIX
CERAMIC PACKAGE
CASE 623

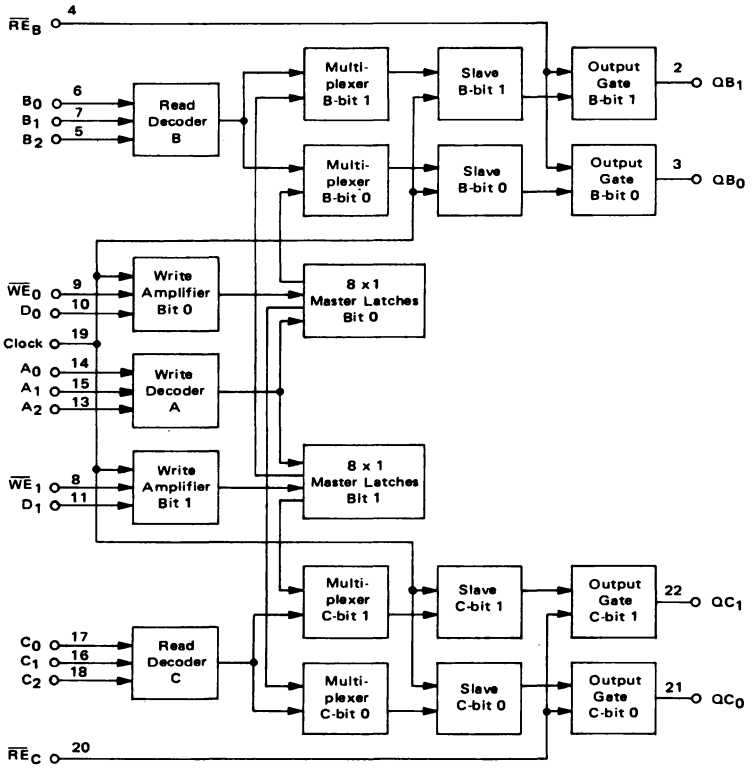
PIN ASSIGNMENT



V_{CC0} = Pin 1
V_{CC1} = Pin 23
V_{CC} = Pin 24
V_{EE} = Pin 12

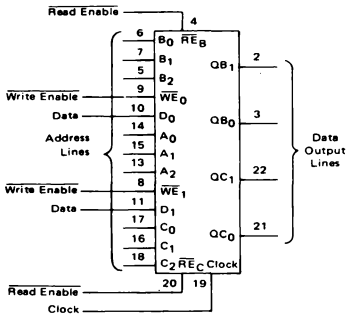
See General Information section for packaging.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.



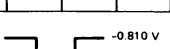
@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MCM10143L Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC} Gnd)
Power Supply Drain Current	I_E	12	–	–	–	118	147	–	–	mAdc	4,5,6,7,8, 9,13,14, 15,16,17, 18,19,20	–	–	–	12	1,23
Input Current	$I_{in\ H}$	4	–	–	–	–	200	–	–	µAdc	4	–	–	–	12	1,23
		5	–	–	–	–		–	–		5	–	–	–		
		6	–	–	–	–		–	–		6	–	–	–		
		7	–	–	–	–		–	–		7	–	–	–		
		8	–	–	–	–		–	–		8	–	–	–		
		9	–	–	–	–		–	–		9	–	–	–		
		13	–	–	–	–		–	–		13	–	–	–		
		14	–	–	–	–		–	–		14	–	–	–		
		15	–	–	–	–		–	–		15	–	–	–		
		16	–	–	–	–		–	–		16	–	–	–		
		17	–	–	–	–		–	–		17	–	–	–		
		18	–	–	–	–		–	–		18	–	–	–		
		20	–	–	–	–		–	–		20	–	–	–		
		10	–	–	–	–	245	–	–		10	–	–	–		
		11	–	–	–	–	245	–	–		11	–	–	–		
		19	–	–	–	–	245	–	–		19	–	–	–		
	$I_{in\ L}$	*	–	–	0.5	–	–	–	–	µAdc	–	*	–	–	12	1,23
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	10,11 ①	–	–	–	12	1,23
		3	↓	↓	↓	–	↓	↓	↓	↓	↓ ↓	–	–	–	↓	↓
		21				–						–	–	–		
		22				–						–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,20 ①	–	–	–	12	1,23
		3	↓	↓	↓	–	↓	↓	↓	↓	↓ ↓	–	–	–	↓	↓
		21				–						–	–	–		
		22				–						–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	11 ①	–	–	4	12	1,23
		3	↓	–	↓	–	–	↓	–	↓	10	–	–	4		↓
		21		–		–	–		–		10 ↓	–	–	20		
		22		–		–	–		–		11	–	–	20		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	11 ①	–	4	–	12	1,23
		3	–	↓	–	–	↓	–	↓	↓	10	–	4	–		↓
		21	–		–	–		–			10 ↓	–	20	–		
		22	–		–	–		–			11	–	20	–		
Switching Times ②												Figure	Pulse In	Pulse Out	-3.2 V	+2.0
Access Time																
Address Input	t_{B-QB-}	2	–	–	–	10	–	–	–	ns	–	1	5	2	12	1,23
	t_{B+QB+}	2	–	–	–	10	–	–	–		–	1	5	2		
Read Enable	$t_{\overline{RE}-QB+}$	2	–	–	–	2.8	–	–	–		–	2	4	2		
Data	$t_{Clock+QB-}$	2	–	–	–	5.0	–	–	–		–	3	19	2		
Setup																
Address	$t_{setup(B-Clock-)}$	19			–	5.5	–	–	–			4	5	19		
Hold																
Address	$t_{hold(Clock-B+)}$	5				-4.5	–		–		–	4	19	5		
Write Time ②																
Setup																
Write Enable	$t_{setup(\overline{WE}-Clock+)}$	19	–	–	–	2.0	–	–	–		–	5	8	19		
	$t_{setup(\overline{WE}+Clock-)}$	19	–	–	–	2.0	–	–	–		–	6	8	19		
Address	$t_{setup(A-Clock+)}$	19	–	–	–	3.0	–	–	–		–	8	14	19		
Data	$t_{setup(D-Clock+)}$	19	–	–	–	2.0	–	–	–		–	8	10	19		
Hold																
Write Enable	$t_{hold(Clock+\overline{WE}+)}$	8	–	–	–	-2.0	–	–	–		–	5	19	8		
	$t_{hold(Clock+\overline{WE}-)}$	8	–	–	–	-2.0	–	–	–		–	6	19	8		
Address	$t_{hold(Clock+A+)}$	5	–	–	–	-3.0	–	–	–		–	8	19	14		
Data	$t_{hold(Clock+D+)}$	10	–	–	–	+2.6	–	–	–		–	8	19	10		
Write Pulse Width	$PW_{\overline{WE}}$	19	–	–	–	5.0	–	–	–		–	7	8	19		
Rise Time (20% to 80%)	t_+	2	–		–	2.0	–	–	–		–	–	5	2		
Fall Time (20% to 80%)	t_-	2	–	–		2.0	–	–	–	↓	–		5	2	↓	↓

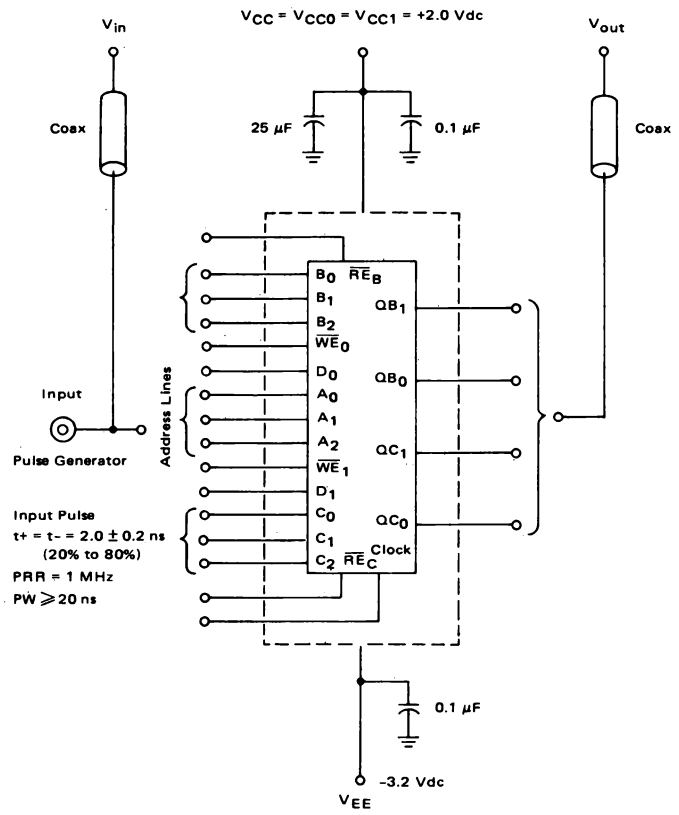
*Limit applies for all inputs, individually apply V_{ILmin} to pin under test

① Data has to be clocked in.

② AC timing figures do not show all the necessary pre-setting conditions



SWITCHING TIME TEST CIRCUIT @ 25°C

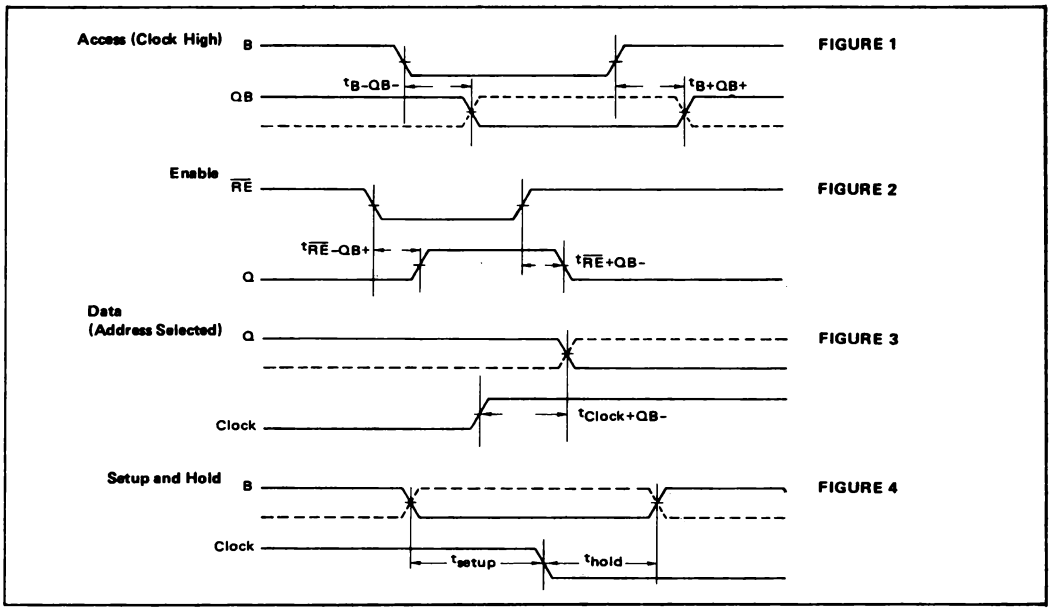


50-ohm termination to ground located in each scope channel input.

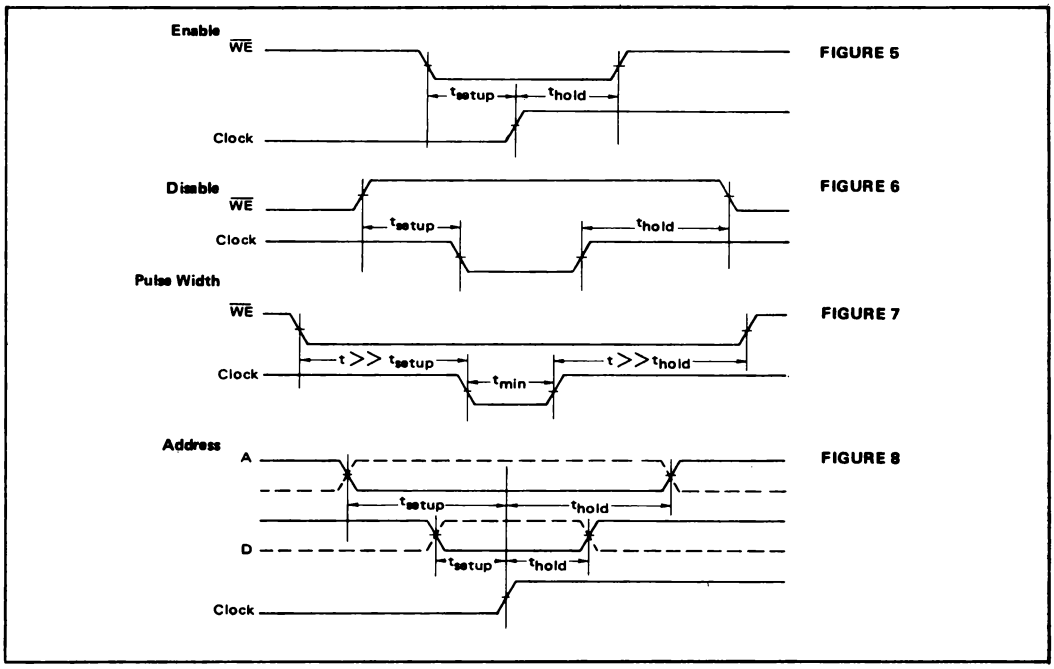
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs connected to a 50-ohm resistor to ground.

READ TIMING DIAGRAMS



WRITE TIMING DIAGRAMS



256 BIT RANDOM
ACCESS MEMORY

MCM10144

256 x 1 BIT RANDOM ACCESS MEMORY

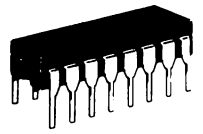
The MCM10144 is a fully decoded 256-bit Random Access Read/Write Memory organized as 256 one bit words. Stored data is selected by means of an eight bit address, consisting of inputs A0 through A7.

The MCM10144 has three active-low chip enable inputs for increased logic flexibility permitting memory expansion up to 2048 words without additional decoding. For larger memories, the upper address words are selected by using one of the $\overline{CE}$ inputs for enabling 1024 word segments.

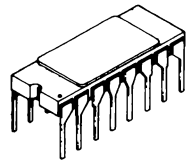
The MCM10144 operating mode (all $\overline{CE}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the WRITE mode, the output, D_{out}, is tow and the data state present at the data input (pin 13) is stored at the selected address. With the $\overline{WE}$ high the chip is in the READ mode and the data state at the selected memory location will be presented, noninverted at the data output (pin 15).

Open emitter outputs permit full *wire-ORing* to data buses, with Q low when the chip is disabled.

The device is fully compatible with the MECL 10,000 logic family. It is designed for use in high speed scratch pad, control, cache, and buffer storage applications.

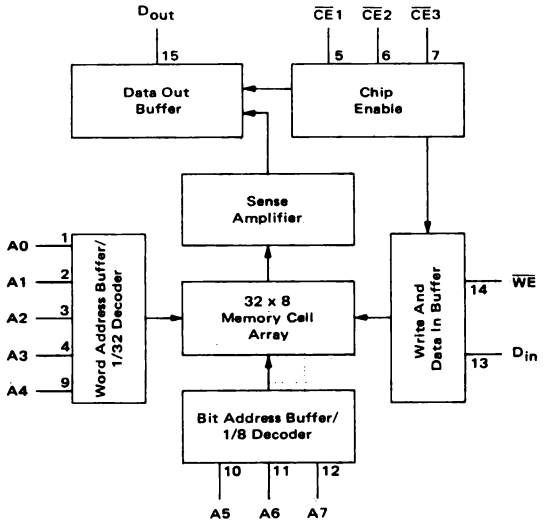


L SUFFIX
CERAMIC PACKAGE
CASE 620

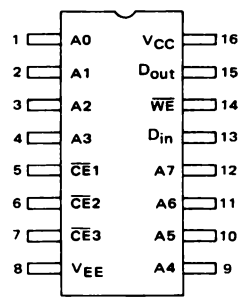


MCM10144AL
CERAMIC PACKAGE
CASE 690

BLOCK DIAGRAM



PIN ASSIGNMENT



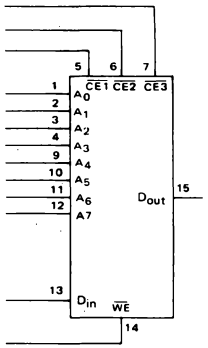
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CE}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

ELECTRICAL CHARACTERISTICS

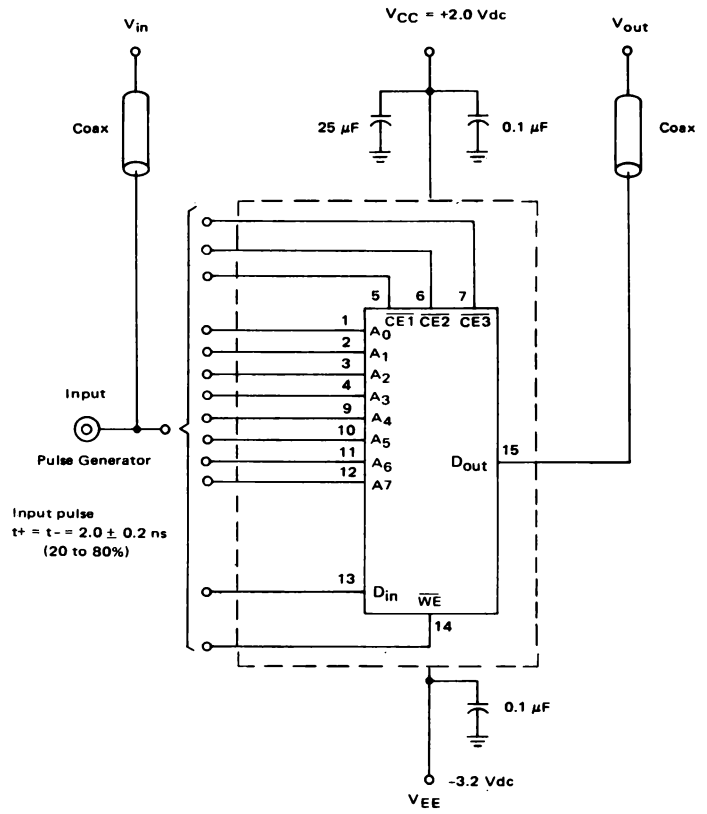
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for selected inputs; other inputs are tested in the same manner.



@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

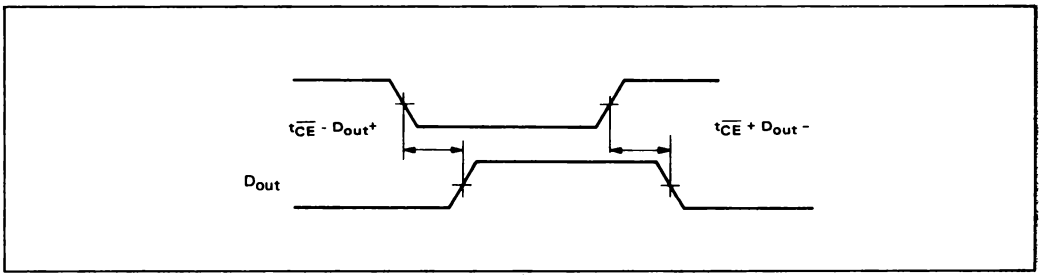
Characteristic	Symbol	Pin Under Test	MCM10144 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC} Gnd
Power Supply Drain Current	I_E	8	–	–	–	80	100	–	–	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	5	–	–	–	–	265	–	–	µAdc	5	–	–	–	8	16
		1	–	–	–	–	50	–	–		1	–	–	–		
		12	–	–	–	–	50	–	–		12	–	–	–		
		14	–	–	–	–	50	–	–		14	–	–	–		
	I_{inL}	5	–	–	0.5	–	–	–	–	µAdc	–	5	–	–	8	16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	13,14	1,2,3,4,5,6, 7,9,10,11,12	–	–	8	16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	14	1,2,3,4,5,6,7, 9,10,11,12,13	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13,14	1,2,3,4,5,6, 7,9,10,11,12	–	5,6,7	8	16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13,14	1,2,3,4,5,6, 7,9,10,11,12	5,6,7	–	8	16
Switching Times													**Pulse In**	**Pulse Out**		
Access Times																
Chip Enable	$t_{\overline{CE}-D_{out}+}$	15	–	–	–	5	10	–	–	ns	–	–	6,7	15	8	16
	$t_{\overline{CE}+D_{out}-}$		–	–	–	5	10	–	–		–	–	5			
Address Inputs	$t_{A\pm D_{out}+}$		–	–	–	18	30	–	–		–	–	1			
	$t_{A\pm D_{out}-}$		–	–	–	18	30	–	–		–	–	1			
Write Strobe Mode Times																
Setup																
Data	$t_{setup(D\pm\overline{W}-}$	15	–	–	2.0	–	–	–	–		–	–	13,14			
Chip Enable	$t_{setup(\overline{CE}-\overline{W}-)}$		–	–	2.0	–	–	–	–		–	–	5,14			
Address	$t_{setup(A\pm\overline{W}-)}$		–	–	10	–	–	–	–		–	–	1,14			
Hold																
Data	$t_{hold(\overline{W}+D\pm)}$		–	–	2.0	–	–	–	–		–	–	13,14			
Chip Enable	$t_{hold(\overline{W}+\overline{CE}+)}$		–	–	2.0	–	–	–	–		–	–	7,14			
Address	$t_{hold(\overline{W}+A\pm)}$		–	–	0	–	–	–	–		–	–	1,14			
Recovery After Write Time	$t_{\overline{W}+D_{out}+}$		–	–	–	–	17	–	–		–	–	14			
	$t_{\overline{W}-D_{out}-}$		–	–	–	–	17	–	–		–	–	14			
Write Pulse Width	$t_{w(\overline{WE})}$	12	–	–	30	–	–	–	–		–	–	14			

SWITCHING TIME TEST CIRCUIT @ 25°C

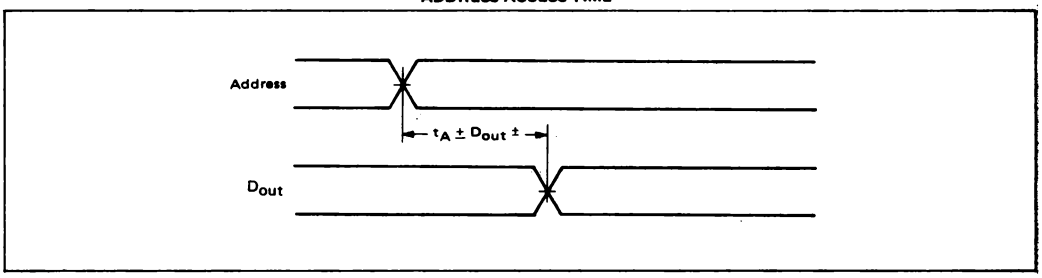


50-ohm termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

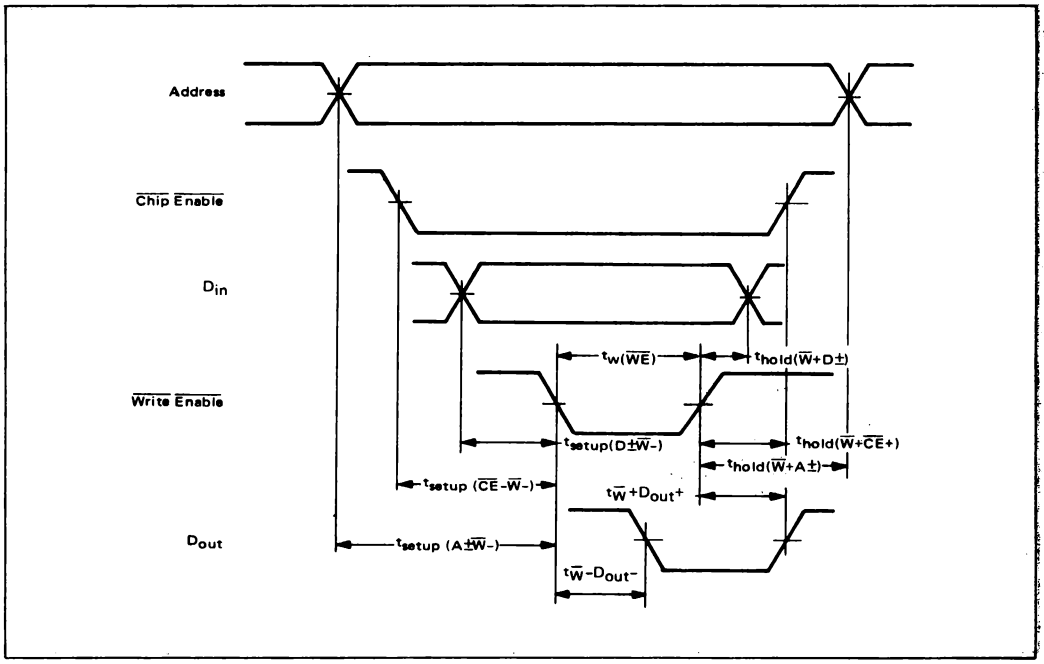
CHIP ENABLE ACCESS TIME



ADDRESS ACCESS TIME



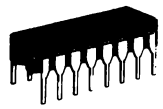
WRITE STROBE MODE



MCM10145

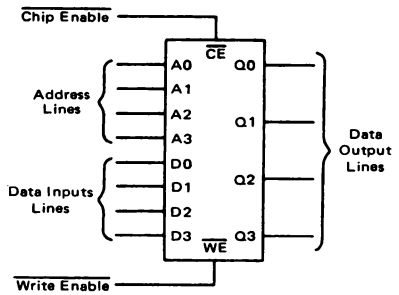
64-BIT REGISTER FILE (RAM)

The MC10145 is a 64-Bit RAM organized as a 16x4 array. This organization and the high speed make the MC10145 particularly useful in register file or small scratch pad applications. Fully decoded inputs, together with a chip enable, provide expansion of memory capacity. The Write Enable input, when low, allows data to be entered; when high, disables the data inputs. The Chip Enable input when low, allows full functional operation of the device; when high, all outputs go to a low logic state. The Chip Enable, together with open emitter outputs allow full wire-ORing and data bussing capability. On-chip input pulldown resistors allow unused inputs to remain open.



L SUFFIX
CERAMIC PACKAGE
CASE 620

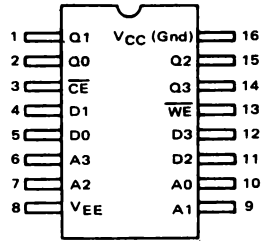
BLOCK DIAGRAM



V_{CC} = Gnd
V_{EE} = -5.2 Vdc

P_D = 625 mW typ/pkg (No Load)
t_{Access} = 10 ns typ (Address Inputs)

PIN ASSIGNMENT



TRUTH TABLE

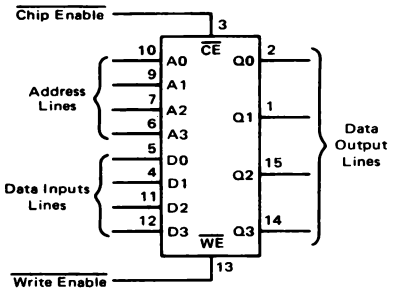
MODE	INPUT			OUTPUT
	CE	WE	D	Q
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.



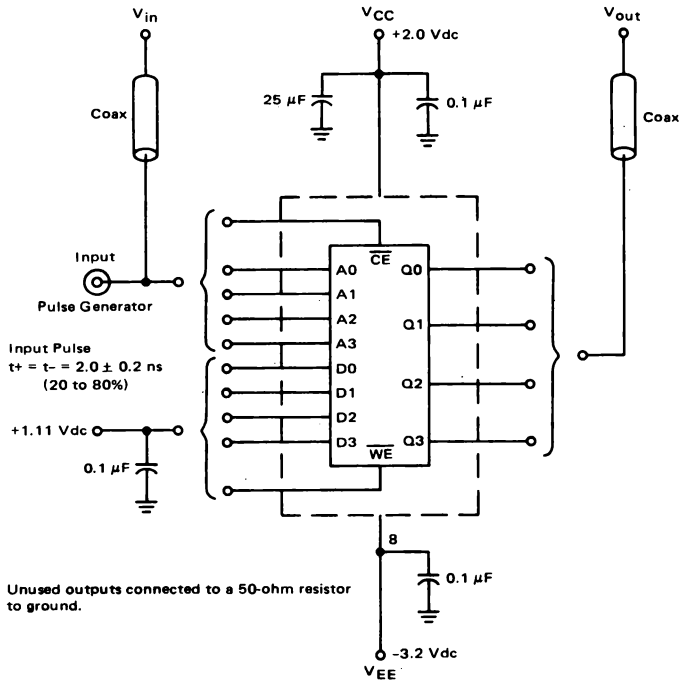
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MCM10145L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
Power Supply Drain Current	I_E	8	–	–	–	120	150	–	–	mAdc	–	–	–	–	8
Input Current	$I_{in\ H}$	3	–	–	–	–	200	–	–	µAdc	3	–	–	–	8
		4	–	–	–	–	220	–	–		4	–	–	–	
		5	–	–	–	–	220	–	–		5	–	–	–	
		6	–	–	–	–	200	–	–		6	–	–	–	
		7	–	–	–	–	200	–	–		7	–	–	–	
		9	–	–	–	–	200	–	–		9	–	–	–	
		10	–	–	–	–	200	–	–		10	–	–	–	
		11	–	–	–	–	220	–	–		11	–	–	–	
		12	–	–	–	–	220	–	–		12	–	–	–	
		13	–	–	–	–	470	–	–		13	–	–	–	
	$I_{in\ L}$	*	–	–	0.5	–	–	–	–	µAdc	–	*	–	–	8
Logic "1" Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4 ②	–	–	–	8
		2				–					5 ②	–	–	–	
		14				–					12 ②	–	–	–	
		15				–					11 ②	–	–	–	
Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	②	–	–	–	8
		2				–					②	–	–	–	
		14				–					②	–	–	–	
		15				–					②	–	–	–	
Logic "1" Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	②	–	4	–	8
		2		–		–	–		–			–	5	–	
		14		–		–	–		–			–	12	–	
		15		–		–	–		–			–	11	–	
Logic "0"	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	②	–	–	4	8
		2	–		–	–		–				–	–	5	
		14	–		–	–		–				–	–	12	
		15	–		–	–		–				–	–	11	
Switching Times ③											+1.11 V		Pulse In	Pulse Out	-3.2 V
Access Times															
Chip Enable	$t_{\overline{CE}-Q+}$	2	–	–	–	7.0	–	–	–	ns	–	①	3	2	8
	$t_{\overline{CE}+Q-}$	2	–	–	–	7.0	–	–	–		–		3	2	
Address Inputs	t_{A+Q+}	1,2,14,15	–	–	–	10.0	–	–	–		–		6,7,9,10	1,2,14,15	
	t_{A-Q+}		–	–	–		–	–	–		–				
	t_{A+Q-}		–	–	–		–	–	–		–				
	t_{A-Q-}		–	–	–		–	–	–		–				
Write Strobe Mode Times															
Setup															
Data	$t_{setup\ (D-\overline{W})}$	2	–	–	–	0	–	–	–		–	–	5,13	2	
Chip Enable	$t_{setup\ (\overline{CE}-\overline{W})}$	2	–	–	–	3.5	–	–	–		–	–	3,13	2	
Address	$t_{setup\ (A-\overline{W})}$	1,2,14,15	–	–	–	3.5	–	–	–		–	–	6,7,9,10,13	1,2,14,15	
Hold															
Data	$t_{hold\ (\overline{W}-D)}$	2	–	–	–	3.0	–	–	–		–	–	5,13	2	
Chip Enable	$t_{hold\ (\overline{W}-\overline{CE})}$	2	–	–	–	3.0	–	–	–		–	–	3,13	2	
Address	$t_{hold\ (\overline{W}-A)}$	1,2,14,15	–	–	–	3.5	–	–	–		–	–	6,7,9,10,13	1,2,14,15	
Recovery After Write Time	$t_{\overline{W}+Q+}$	2	–	–	–	7.5	–	–	–		5	①	13	2	
	$t_{\overline{W}+Q-}$		–	–	–	7.5	–	–	–		–	①	13	2	
Write Pulse Width	$PW_{\overline{W}}$		–	–	–	7.5	–	–	–		–	–	13	2	
Chip Enable Strobe Mode Times															
Setup															
Data	$t_{setup\ (D-\overline{CE})}$		–	–	–	7.5	–	–	–		–	–	3,5	2	
Write Enable	$t_{setup\ (\overline{W}-\overline{CE})}$		–	–	–	11.0	–	–	–		–	–	3,13	2	
Address	$t_{setup\ (A-\overline{CE})}$	1,2,14,15	–	–	–	3.0	–	–	–		–	–	3,6,7,9,10	1,2,14,15	
Hold															
Data	$t_{hold\ (\overline{CE}-D)}$	2	–	–	–	3.0	–	–	–		–	–	3,5	2	
Write Enable	$t_{hold\ (\overline{CE}-\overline{W})}$	2	–	–	–	3.0	–	–	–		–	–	3,13	2	
Address	$t_{hold\ (\overline{CE}-A)}$	1,2,14,15	–	–	–	3.0	–	–	–		–	–	3,6,7,9,10	1,2,14,15	
Chip Enable Pulse Width	$PW_{\overline{CE}}$	2	–	–	–	7.5	–	–	–		–		3	2	
Rise Time (20% to 80%)	t_+		–	–	–	3.0	–	–	–		–	①	–		
Fall Time (20% to 80%)	t_-		–	–	–	3.0	–	–	–		–	①	–		

*Limit applies for all inputs, individually apply $V_{IL\ min}$ to pin under test.
**For definition of timing parameters, see Figure.

① Proper high/low logic levels are written into addressed location prior to test.
② Pulse is applied to pin 13 (Write Enable) with input conditions as shown before measuring output conditions.
③ For definition of symbols see timing diagrams.

SWITCHING TIME TEST CIRCUIT

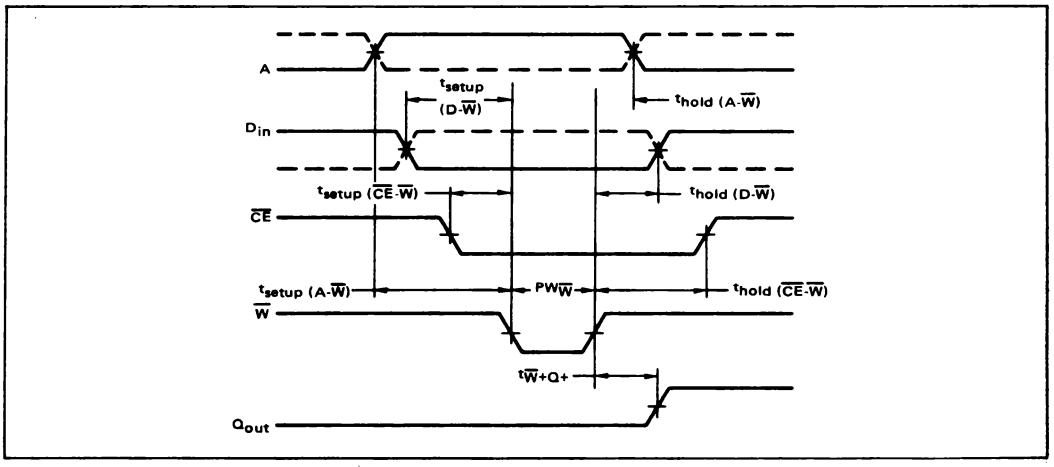


50-ohm termination to ground located in each scope channel input.

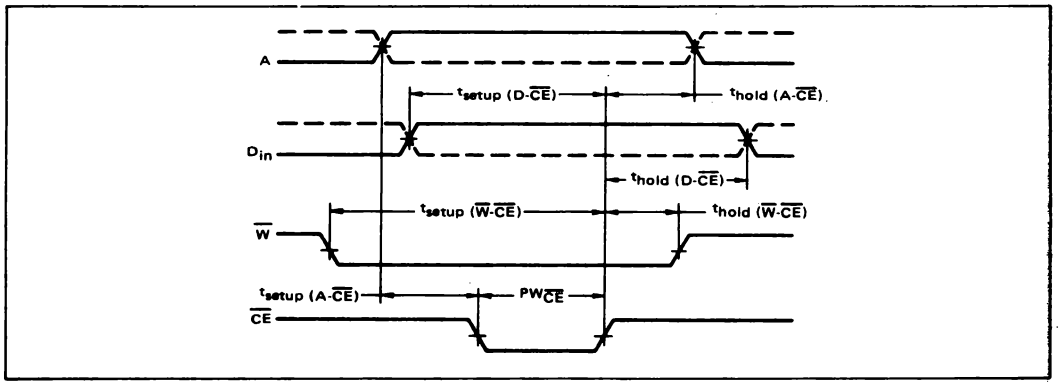
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs connected to a 50-ohm resistor to ground.

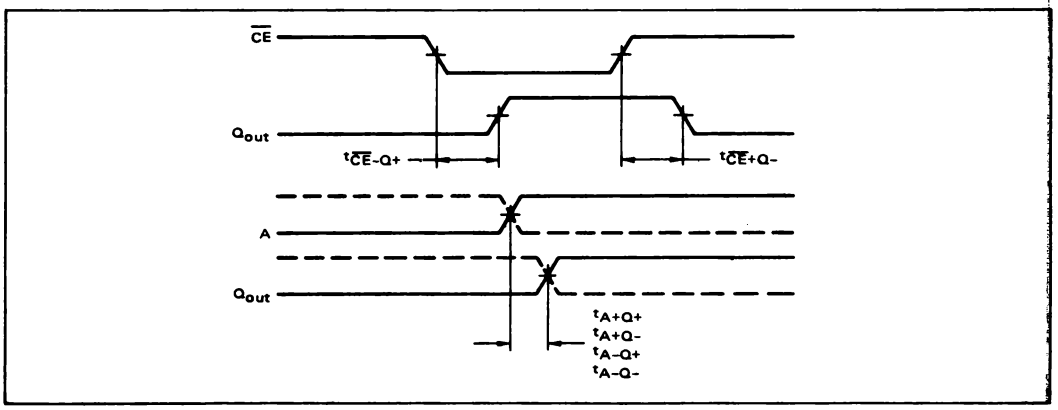
WRITE TIMING DIAGRAMS—WRITE STROBE MODE



CHIP ENABLE STROBE MODE



READ TIMING DIAGRAM



MCM10147

128 x 1 BIT RANDOM ACCESS MEMORY

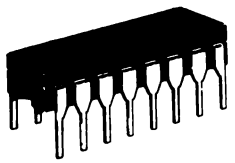
The MCM10147 is a 128-bit RAM organized as a 128-word by 1-bit array. This organization and the high speed of this MECL 10,000 device make the MCM10147 particularly useful in fast scratch pad, register file, and buffer memory applications. Full address decoding, and two Chip Enables ($\overline{CE}$) are included in this device to permit simple memory expansion.

For writing Data (D) into this memory, both Chip Enables $\overline{CE1}$ and $\overline{CE2}$ are brought low, the address is presented at A0-A6, and the Read/Write Enable ($\overline{WE}$) is taken low while Data is valid. To read a particular address, both Chip Enable inputs must again be low, but the Read/Write input is high (Data input disabled) while the location is addressed.

The two Chip Enables are provided for row or column selection of device packages in an expanded memory system. Either input can be used to select a particular row or column of stored data bits.

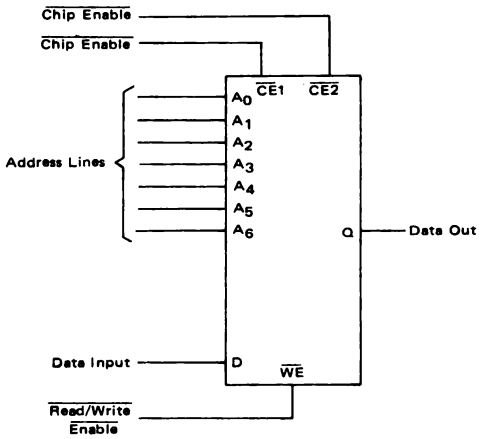
Open emitter outputs permit full wire-ORing to data buses, with the output being held low when either Chip Enable is high.

Internal input pulldown resistors are not used on this device. Unused inputs should be tied to V_{EE}.



L SUFFIX
CERAMIC PACKAGE
CASE 620

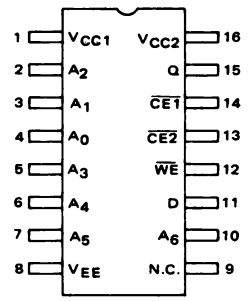
BLOCK DIAGRAM



$V_{CC1} = V_{CC2} = Gnd$
$V_{EE} = -5.2\ V$

$P_D = 415$ mW typ/pkg (No Load)
$t_{Access} = 10$ ns typ (Address Inputs)

PIN ASSIGNMENT



TRUTH TABLE

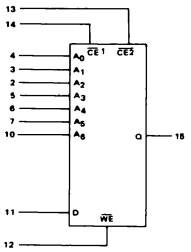
MODE	INPUT				OUTPUT
	$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L	L
Write "1"	L	L	L	H	L
Read	L	L	H	ϕ	Q
Disabled	H	L	ϕ	ϕ	L
	L	H	ϕ	ϕ	L

ϕ = don't care

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

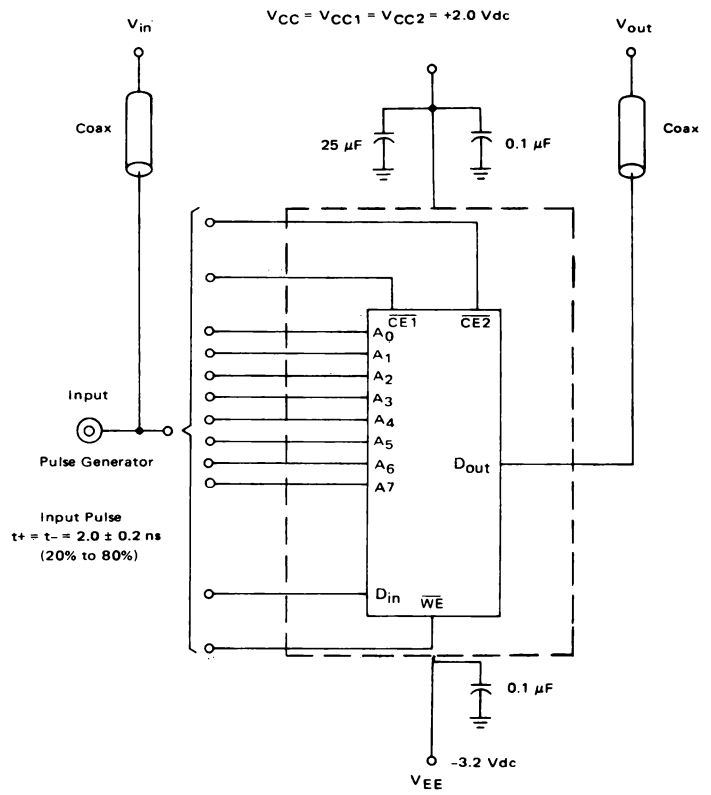
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for selected inputs; other inputs are tested in the same manner.



@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10147AL Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–		80	100	–	–	mAdc	–	–	–	–	8	16
Input Current	I_{in} H	2	–	–	–	–	35	–	–	μAdc	2	–	–	–	8	1,16
		11	–	–	–	–		–	–	↓	11	–	–	–	↓	↓
		13	–	–	–	–		–	–		13	–	–	–		
		12	–	–	–	–	75	–	–		12	–	–	–		
	I_{in} L	2	–	–	-6.0	–	+6.0	–	–	μAdc	–	2	–	–	8	1,16
		11	–	–	–	–	↓	–	–	↓	–	11	–	–	↓	↓
		13	–	–	–	–		–	–		–	13	–	–		
		12	–	–	-6.0	–		–	–		–	12	–	–		
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	– –	-0.810	-0.890	-0.700	Vdc	–	2,3,4,5, 6,7,10,11	12	13,14	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.920	-1.675	-1.880	– –	-1.650	-1.855	-1.615	Vdc	–	2,3,4,5 6,7,10,11	12	13,14	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-0.980	– –	–	-0.910	–	Vdc	–	2,3,4,5, 6,7,10,11	12	13,14	8	1,16
Logic "0"	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,3,4,5,	13	–	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	6,7,10,11	14	–	8	1,16
Switching Times													Pulse In	Pulse Out		
Access Times																
Chip Enable	$t_{\overline{CE}-Q+}$	15	–	–	–	–	8.0	–	–	ns	–	–	13	15	8	1,16
	$t_{\overline{CE}+Q-}$		–	–	–	–	8.0	–	–	↓	–	–	14	↓	↓	↓
Address Inputs	t_{A+Q+}		–	–	–	10	12	–	–		–	–	7			
	t_{A-Q+}		–	–	–	10	12	–	–		–	–	7			
	t_{A+Q+}		–	–	–	9	10	–	–		–	–	4			
	t_{A-Q-}	↓	–	–	–	9	10	–	–		–	–	4			
Write Strobe Mode Times																
Setup																
Data	$t_{setup(D-\overline{W})}$	15	–	–	1.0	–	–	–	–		–	–	11,12			
Chip Enable	$t_{setup(\overline{CE}-\overline{W})}$		–	–	1.0	–	–	–	–		–	–	12,13			
Address	$t_{setup(A-\overline{W})}$		–	–	3.0	–	–	–	–		–	–	2,12			
	$t_{setup(A-\overline{W})}$		–	–	4.0	–	–	–	–		–	–	7,12			
Hold																
Data	$t_{hold(D-\overline{W})}$		–	–	1.0	–	–	–	–		–	–	11,12			
Chip Enable	$t_{hold(\overline{CE}-\overline{W})}$		–	–	1.0	–	–	–	–		–	–	12,13			
Address	$t_{hold(A-\overline{W})}$		–	–	3.0	–	–	–	–		–	–	2,12			
Recovery After Write Time	$t_{\overline{W}+Q+}$		–	–	–	–	8.0	–	–		–	–	12			
	$t_{\overline{W}+Q-}$	↓	–	–	–	–	8.0	–	–		–	–	12			
Write Pulse Width	$t_{w(\overline{WE})}$	12	–	–	–	–	8.0	–	–		–	–	12	↓	↓	↓
Rise Time (20% to 80%)	t+	11	–	–	–	2.0	–	–	–		–	–	–	11	8	1,16
Fall Time (20% to 80%)	t−	11	–	–	–	1.0	–	–	–	↓	–	–	–	11	8	1,16

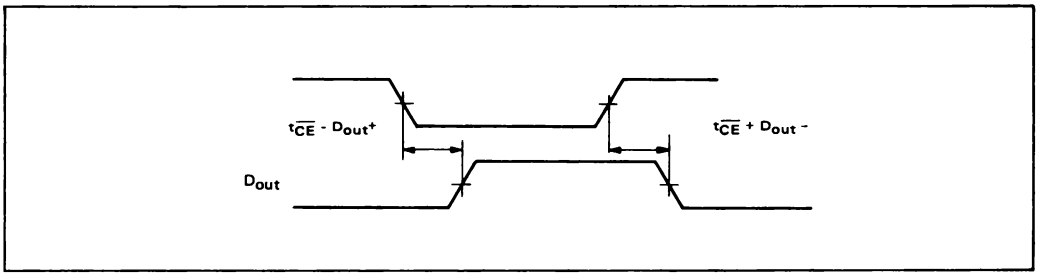
SWITCHING TIME TEST CIRCUIT @ 25°C



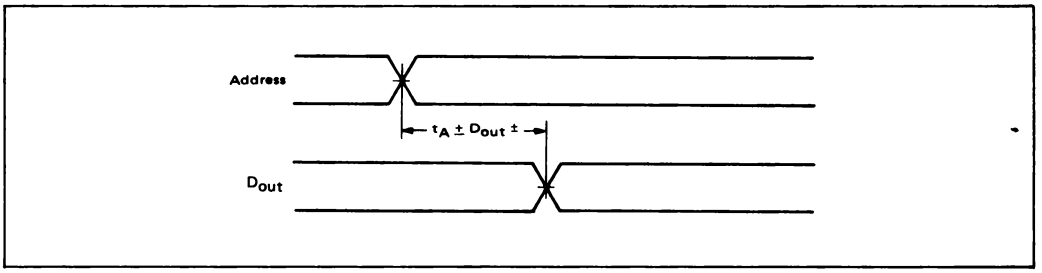
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

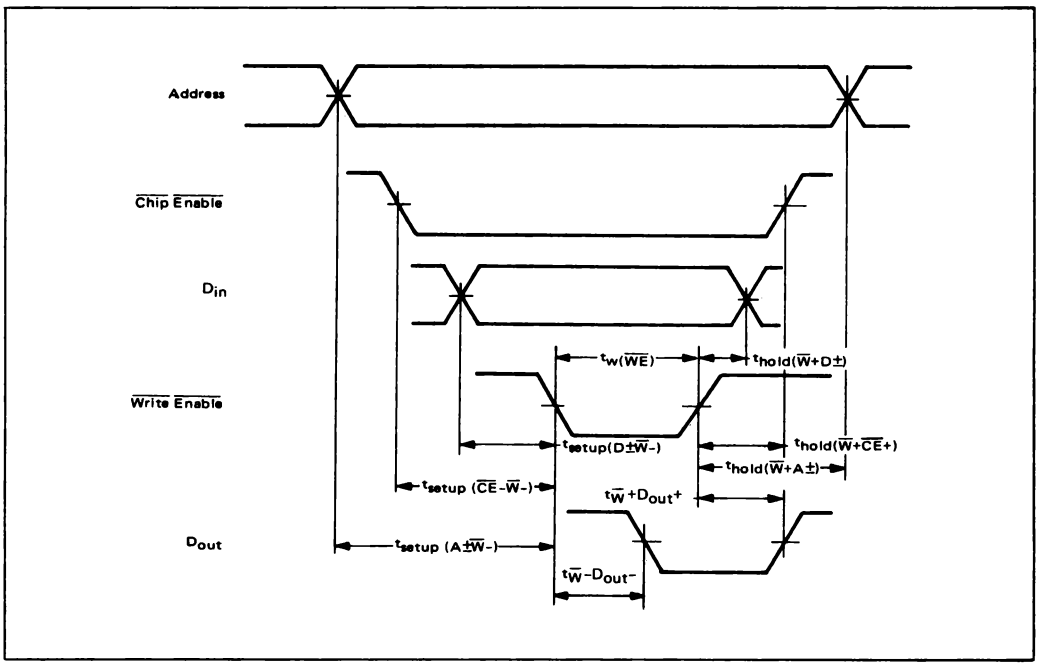
CHIP ENABLE ACCESS TIME



ADDRESS ACCESS TIME



WRITE STROBE MODE



MCM10150

Advance Information

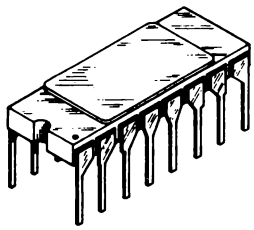
256 x 4 BIT PROGRAMMABLE READ ONLY MEMORY

The MCM10150AL is a monolithic 1024-bit programmable read only memory (ROM) that can be factory programmed for custom requirements. The basic organization of the memory is 256 four-bit words. This organization and the high speed of this MECL 10,000 device make the MCM10150AL particularly useful in fast micro programs, look up tables, decode functions, code conversion, number conversion, and random logic.

Metal interconnections establish each bit initially in the logic "1" state. By "blowing" appropriate nichrome resistors and thus breaking metallization links these bits can be changed to the logic "0" state to meet specific custom program requirements.

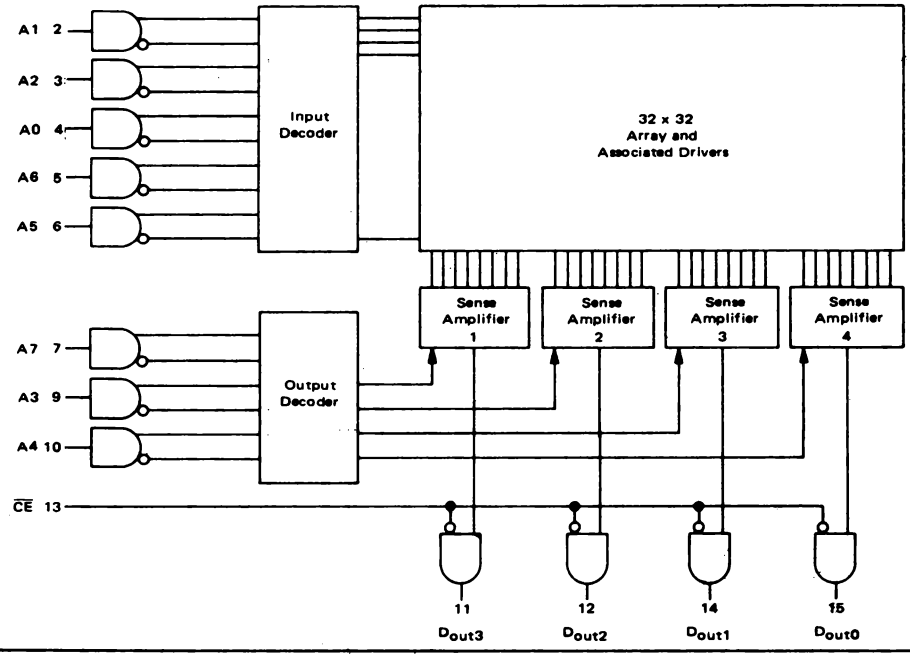
The MCM10150AL has eight address inputs to select the proper word and one chip enable input as well as outputs for each of the four bits. The MCM10150AL is specified over an operating temperature range of -30°C to +85°C.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8



MCM10150AL
CERAMIC PACKAGE
CASE 690

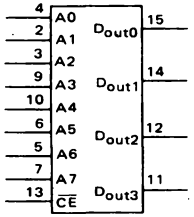
BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.



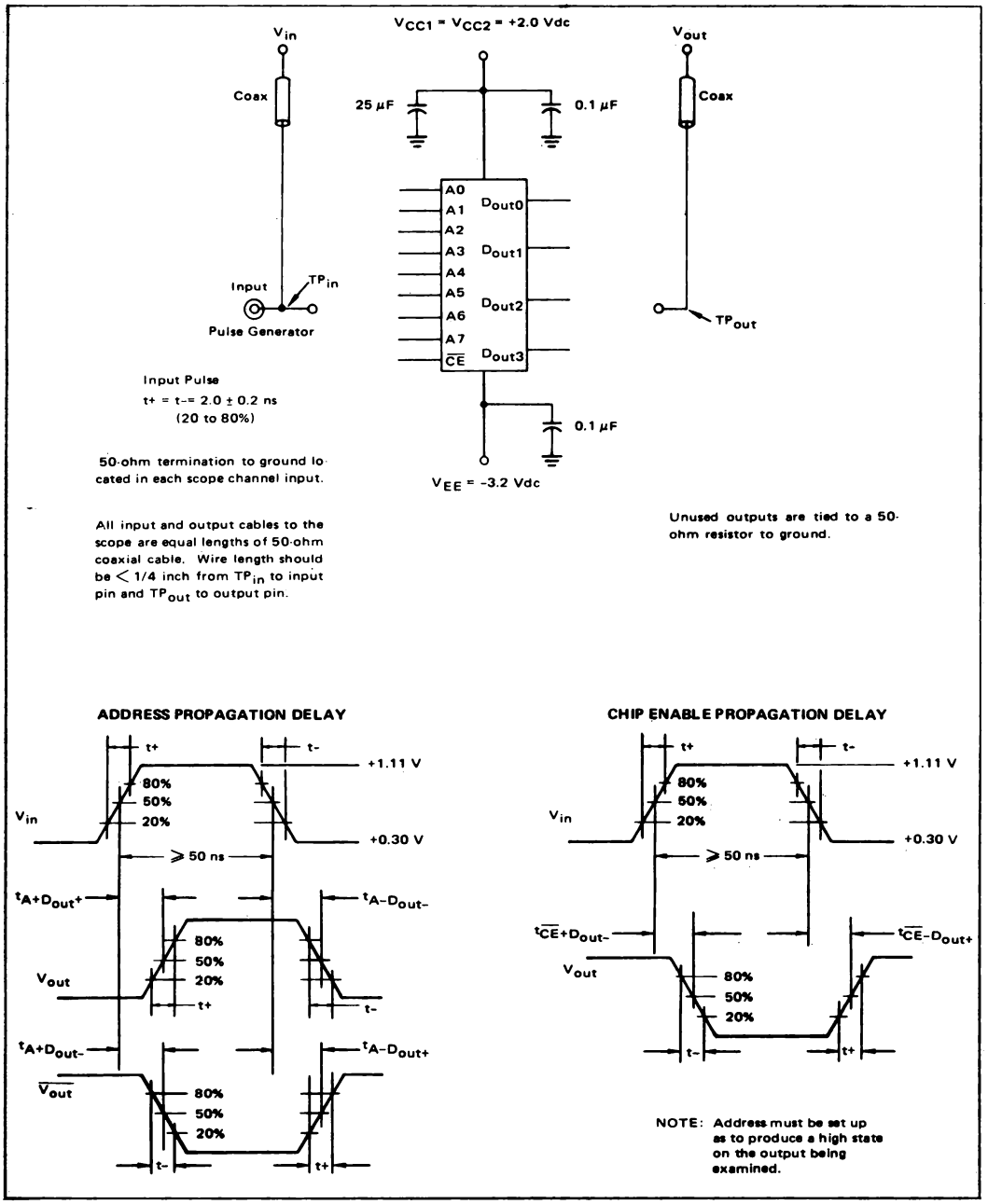
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MCM10150AL Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC} Gnd
Power Supply Drain Current	I_E	8	–	–	–	110	150	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	2	–	–	–	–	265	–	–	μAdc	2	–	–	–	8	1,16
	I_{inL}	2	–	–	0.5	–	–	–	–	μAdc	–	2	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}*	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	*	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	13	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}*	15	-0.080	–	-0.980	–	–	-0.910	–	Vdc	–	*	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	13	–	8	1,16
Switching Times (50 Ω Load)													**Pulse In**	**Pulse Out**	**-3.2 V**	**+2.0 V**
Access Time																
Chip Enable	$t_{\overline{CE}-D_{out}+}$	15	–	–	–	7.0	–	–	–	ns	–	–	13	15	8	1,16
	$t_{\overline{CE}+D_{out}-}$		–	–	–	7.0	–	–	–		–	–	13			
Address Inputs**	$t_{A+D_{out}+}$		–	–	–	20	–	–	–		–	–	7			
	$t_{A-D_{out}+}$		–	–	–	20	–	–	–		–	–	7			
Rise Time (20% to 80%)	t_{15+}		–	–	–	4.0	–	–	–		–	–	7			
Fall Time (20% to 80%)	t_{15-}		–	–	–	4.0	–	–	–		–	–	7			

*V_{OH} measurement pattern dependent.

**AC tests shown for only one address line and one output (times are pattern dependent).

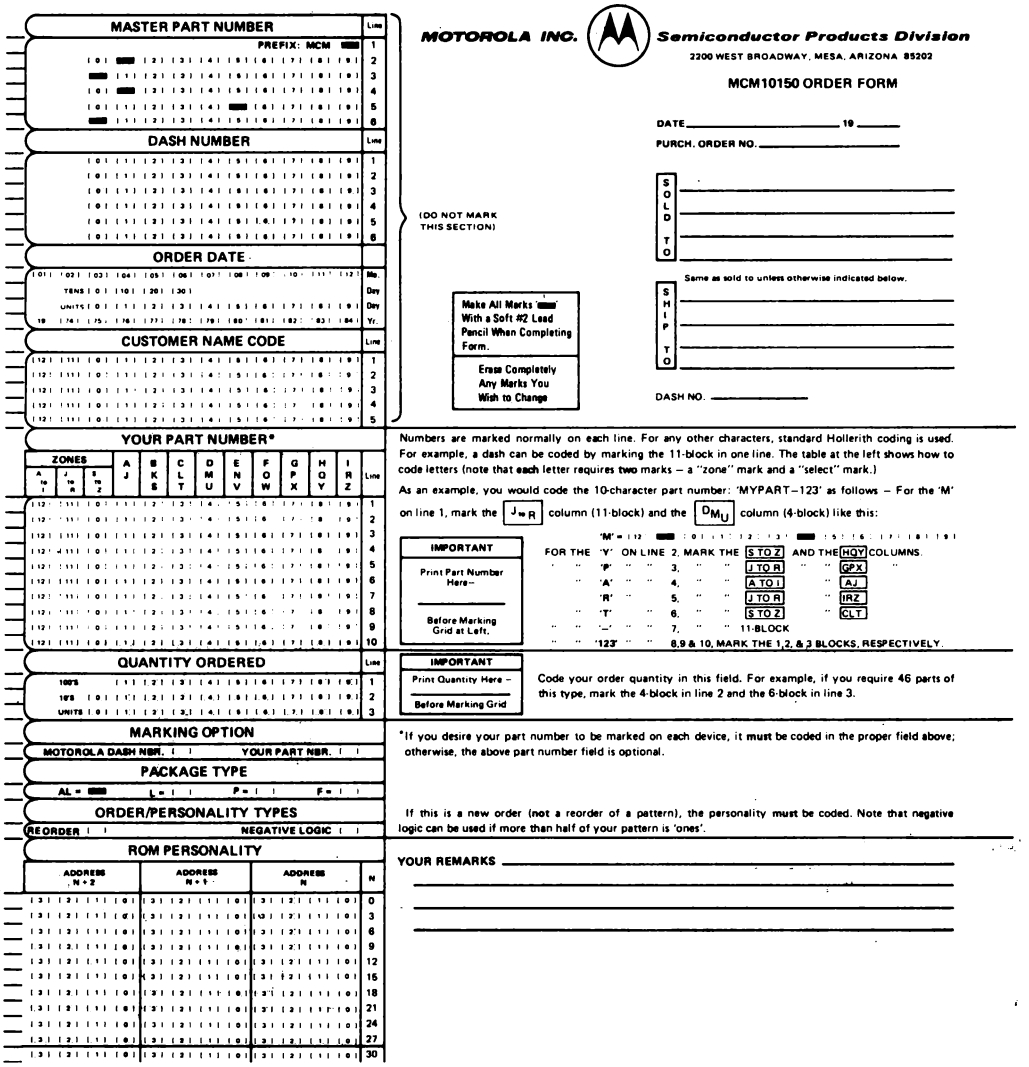
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



ADDRESS PROPAGATION DELAY

CHIP ENABLE PROPAGATION DELAY

NOTE: Address must be set up as to produce a high state on the output being examined.



MASTER PART NUMBER — PREFIX: MCM

DASH NUMBER

ORDER DATE

CUSTOMER NAME CODE

YOUR PART NUMBER*

ZONES

QUANTITY ORDERED

MARKING OPTION

MOTOROLA DASH NBR. YOUR PART NBR.

PACKAGE TYPE

AL = L = P = F =

ORDER/PERSONALITY TYPES

REORDER NEGATIVE LOGIC

ROM PERSONALITY

ADDRESS N+2 | ADDRESS N+1 | ADDRESS N

MOTOROLA INC. Semiconductor Products Division

2200 WEST BROADWAY, MESA, ARIZONA 85202

MCM10150 ORDER FORM

DATE _____ 19 ____

PURCH. ORDER NO. _____

SOLD TO

Same as sold to unless otherwise indicated below.

SHIP TO

DASH NO. _____

(DO NOT MARK THIS SECTION)

Make All Marks With a Soft #2 Lead Pencil When Completing Form.

Erase Completely Any Marks You Wish to Change

Numbers are marked normally on each line. For any other characters, standard Hollerith coding is used. For example, a dash can be coded by marking the 11-block in one line. The table at the left shows how to code letters (note that each letter requires two marks – a "zone" mark and a "select" mark.)

As an example, you would code the 10-character part number: 'MYPART–123' as follows – For the 'M' on line 1, mark the J=R column (11-block) and the D_{MU} column (4-block) like this:

'M' = 12 0 1 2 3 5 6 7 8 9

IMPORTANT — Print Part Number Here — _____ Before Marking Grid at Left.

FOR THE	'Y'	ON LINE	2,	MARK THE	S TO Z AND THE HQY COLUMNS.
"	'P'	"	3,	"	J TO R GPX
"	'A'	"	4,	"	A TO I AJ
"	'R'	"	5,	"	J TO R IRZ
"	'T'	"	6,	"	S TO Z CLT
"	'–'	"	7,	"	11-BLOCK
"	'123'	"	8,9 & 10,	MARK THE 1,2, & 3 BLOCKS, RESPECTIVELY.	

IMPORTANT — Print Quantity Here — _____ Before Marking Grid

Code your order quantity in this field. For example, if you require 46 parts of this type, mark the 4-block in line 2 and the 6-block in line 3.

*If you desire your part number to be marked on each device, it must be coded in the proper field above; otherwise, the above part number field is optional.

If this is a new order (not a reorder of a pattern), the personality must be coded. Note that negative logic can be used if more than half of your pattern is 'ones'.

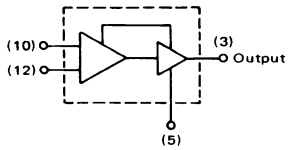
YOUR REMARKS _____

Request your order forms from your Motorola representative.

MECL III

INTEGRATED CIRCUITS
MC1600 SERIES

MC1648



Numbers in parenthesis denote pin number for F package (Case 607) L package (Case 632), and P package (Case 646).

Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

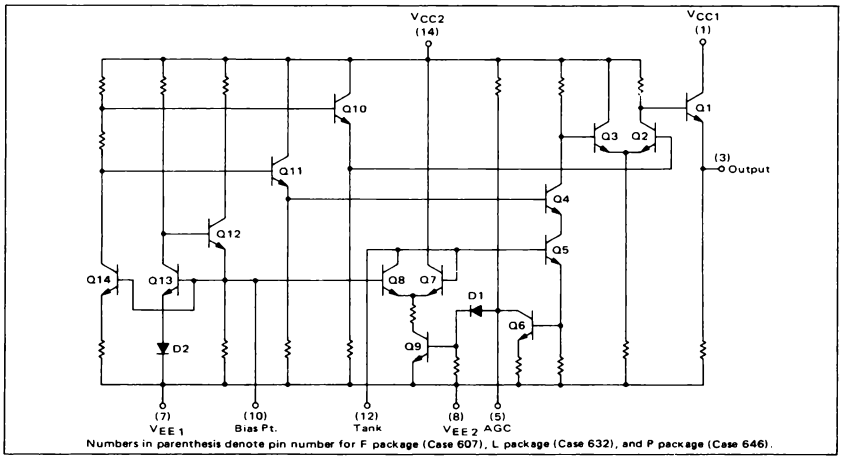
The MC1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with MECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity (See Figure 2).

The MC1648 may be operated from a +5.0 Vdc supply or a -5.2 Vdc supply, depending upon system requirements.

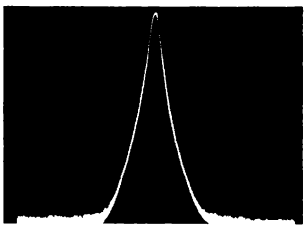
SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

FIGURE 1 – CIRCUIT SCHEMATIC

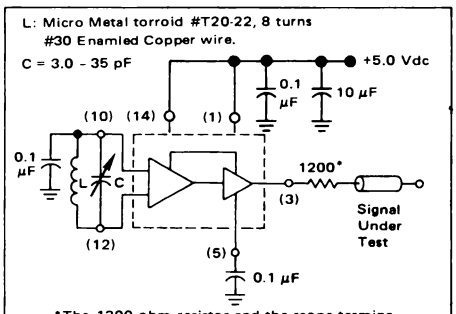


Numbers in parenthesis denote pin number for F package (Case 607), L package (Case 632), and P package (Case 646).

FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT



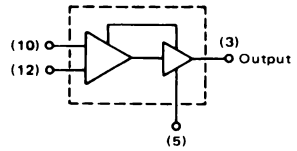
B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



*The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts



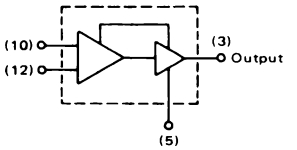
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	mAdc I_L
-30°C	+1.960	+1.410	5.0	-5.0
+25°C	+1.800	+1.300	5.0	-5.0
+85°C	+1.680	+1.180	5.0	-5.0

Characteristic	Symbol	Pin Under Test	MC1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	I_L	V_{EE} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	40	—	—	mAdc	—	—	1, 14	—	7, 8
Logic "1" Output Voltage	V_{OH}	3	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	—	12	1, 14	3	7, 8
Logic "0" Output Voltage	V_{OL}	3	3.16	3.40	3.20	3.43	3.23	3.46	Vdc	12	—	1, 14	3	7, 8
Bias Voltage	V_{Bias}*	10	1.51	1.86	1.40	1.70	1.28	1.58	Vdc	—	—	1, 14	—	7, 8
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max							
Peak-to-Peak Tank Voltage	V_{p-p}	12	—	—	—	—	500	—	—	—	—	mV	See Figure 3	—	1, 14	3	7, 8
Output Duty Cycle	V_{DC}	3	—	—	—	—	50	—	—	—	—	%	See Figure 3	—	1, 14	3	7, 8
Oscillation Frequency	f_{max}	—	—	—	—	200	225	—	—	—	—	MHz	See Figure 3	—	1, 14	3	7, 8

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 volts

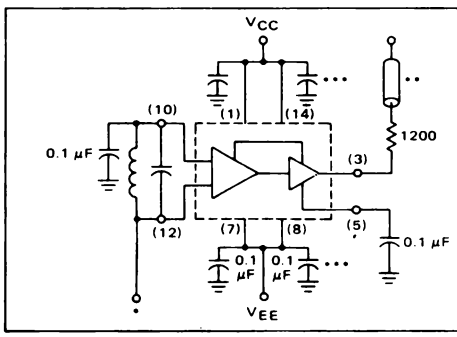


@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	mAdc I_L
-30°C	-3.300	-3.800	-5.2	-5.0
+25°C	-3.400	-3.900	-5.2	-5.0
+85°C	-3.500	-4.000	-5.2	-5.0

Characteristic	Symbol	Pin Under Test	MC1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	41	—	—	mAdc	—	—	7, 8	—	1, 14
Logic "1" Output Voltage	V_{OH}	3	-1.045	-0.815	-0.960	-0.750	-0.890	-0.650	Vdc	—	12	7, 8	3	1, 14
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	12	—	7, 8	3	1, 14
Bias Voltage	V_{Bias}*	10	-3.690	-3.340	-3.800	-3.500	-3.920	-3.620	Vdc	—	—	7, 8	—	7, 14
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max							
Peak-to-Peak Tank Voltage	V_{p-p}	12	—	—	—	—	500	—	—	—	—	mV	See Figure 3	—	7, 8	3	1, 14
Output Duty Cycle	V_{DC}	3	—	—	—	—	50	—	—	—	—	%	See Figure 3	—	7, 8	3	1, 14
Oscillation Frequency	f_{max}	—	—	—	—	200	225	—	—	—	—	MHz	See Figure 3	—	7, 8	3	1, 14

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

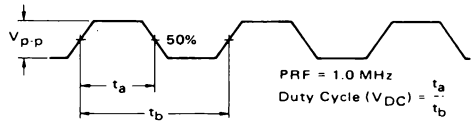
FIGURE 3 – TEST CIRCUIT AND WAVEFORMS



*Use high impedance probe (>1.0 Megohm must be used).

**The 1200-ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

***Bypass only that supply opposite ground.



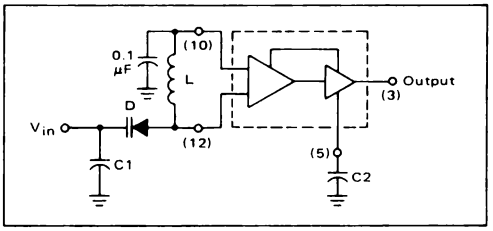
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q7 to the collector of Q8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (Q4) is used to translate from the emitter follower (Q5) to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provide a highly buffered output which produces a square wave. Transistors Q10 thru Q14 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

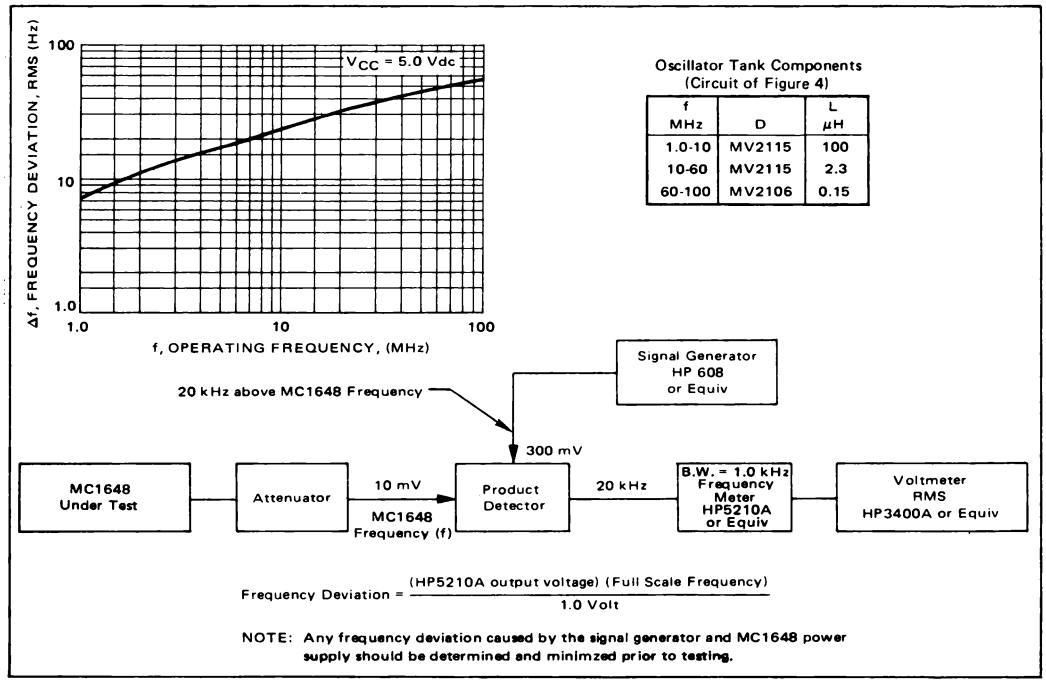
When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

FIGURE 4 – THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 5 – NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



NOTE: Any frequency deviation caused by the signal generator and MC1648 power supply should be determined and minimzed prior to testing.

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^oC$

FIGURE 6

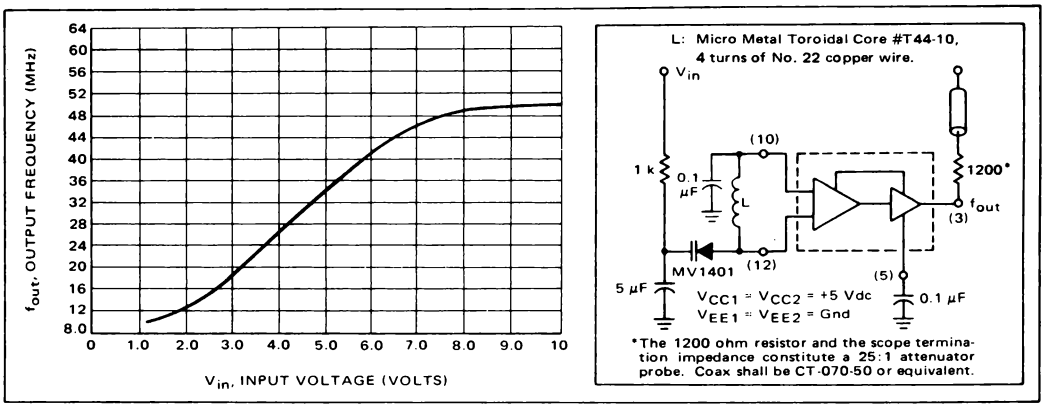


FIGURE 7

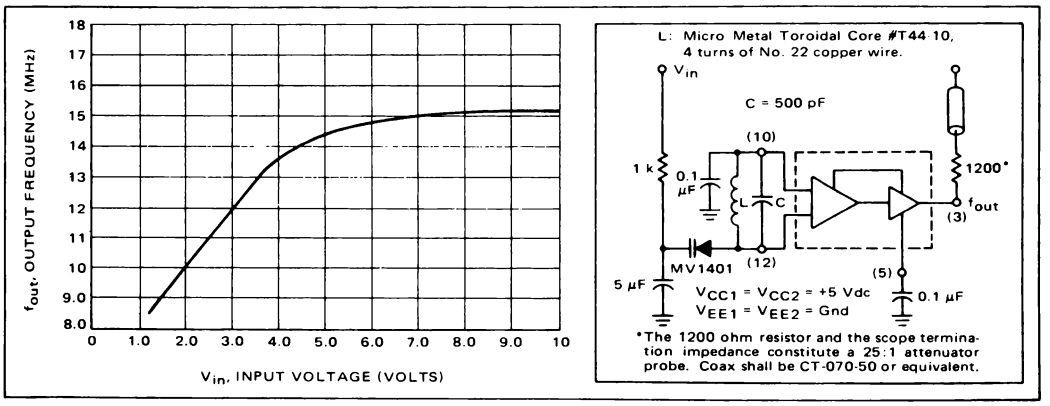
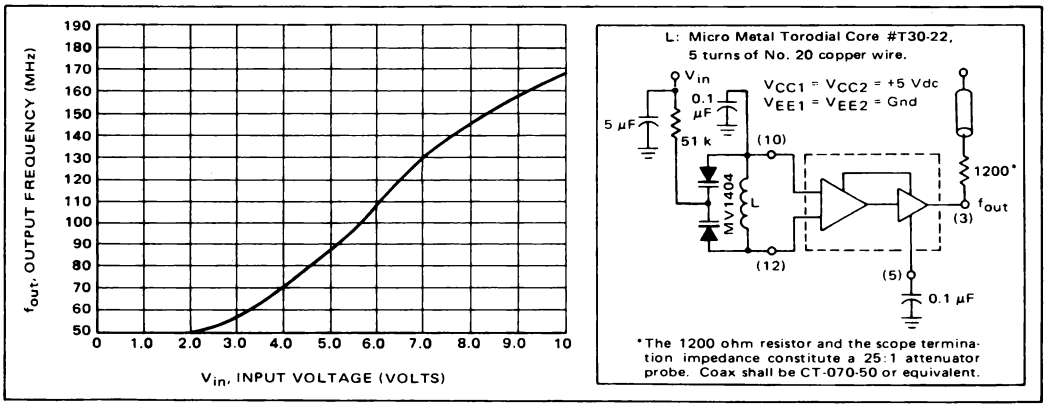


FIGURE 8



Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7 and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (pluse the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\ (max) + C_S}}{\sqrt{C_D\ (min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi \sqrt{L\ (C_D\ (max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins (see Figure 2).

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the MC1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and land-mobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translation, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lock-up. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked-loops and digital frequency synthesizers, see Motorola Application Notes AN-532A, AN-535, AN-553, AN-564, AN-594, or Phase-Locked Loop Systems Data Book.

FIGURE 9 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION

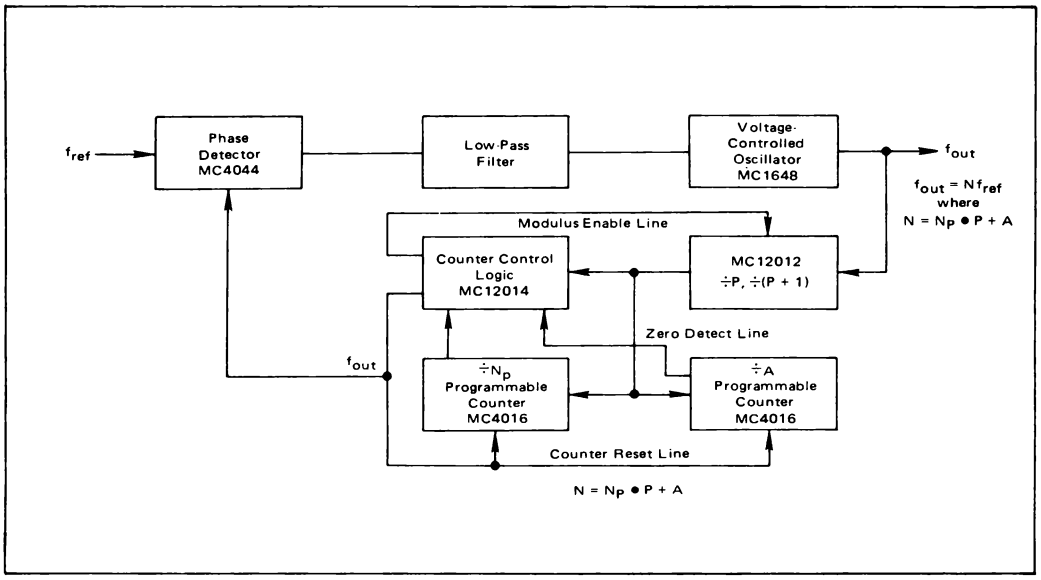


Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

Figure 12 shows the MC1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 – METHOD OF OBTAINING A SINE-WAVE OUTPUT

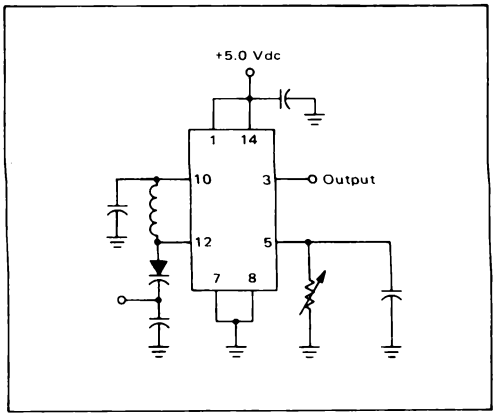


FIGURE 11 – METHOD OF EXTENDING THE USEFUL RANGE OF THE MC1648 (SQUARE WAVE OUTPUT)

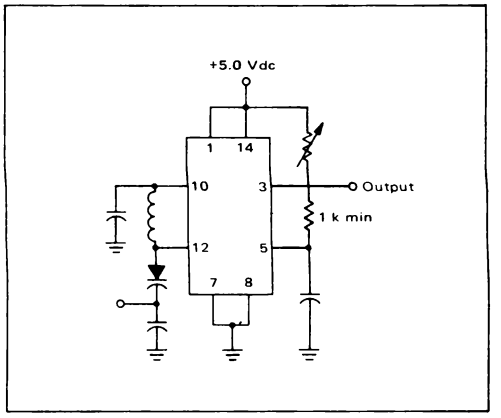


FIGURE 12 — CIRCUIT SCHEMATIC USED FOR COLLECTOR OUTPUT OPERATION

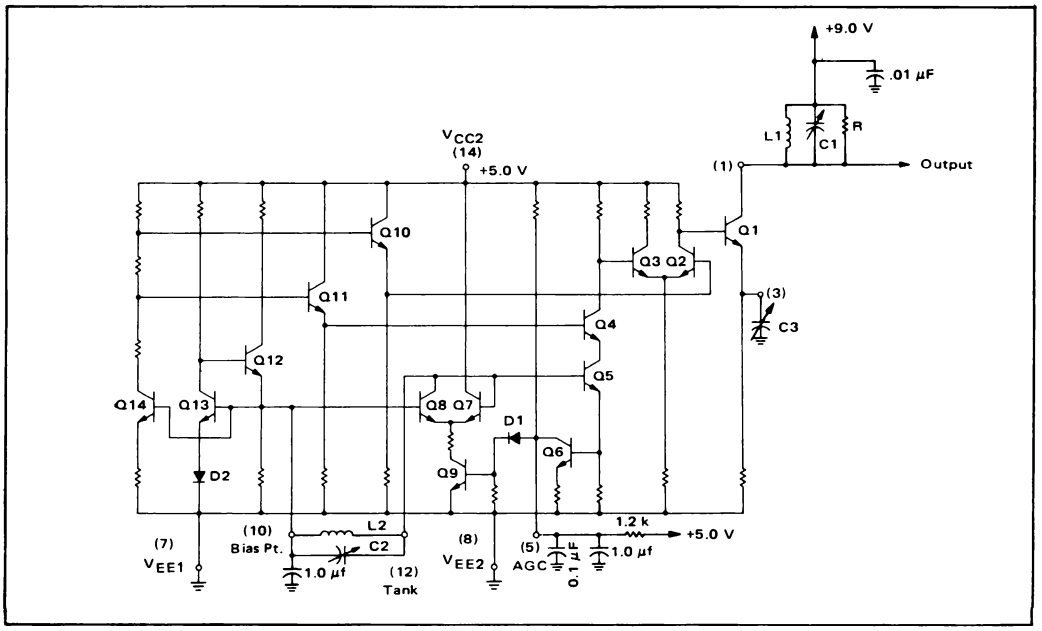


FIGURE 13 — POWER OUTPUT versus COLLECTOR LOAD

See test circuit, Figure 12, f = 100 MHz
C3 = 3.0 - 35 pF
Collector Tank
L1 = 0.22 μH C1 = 1.0 - 7.0 pF
R = 50 Ω - 10 kΩ
Rp of L1 and C1 = 11 kΩ @ 100 MHz Resonance
Oscillator Tank
L2 = 4 turns #20 AWG 3/16" ID
C2 = 1.0 - 7.0 pF

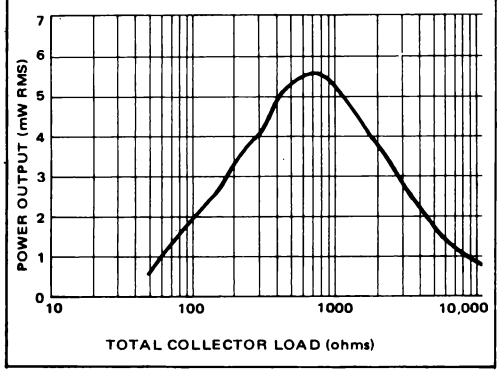
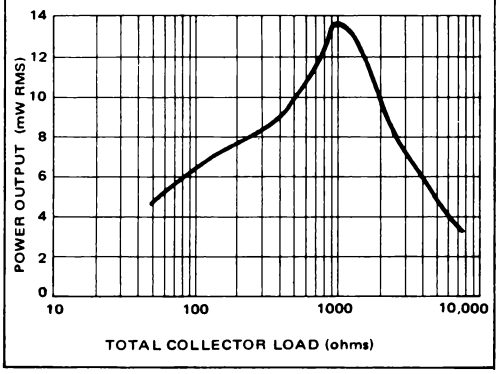
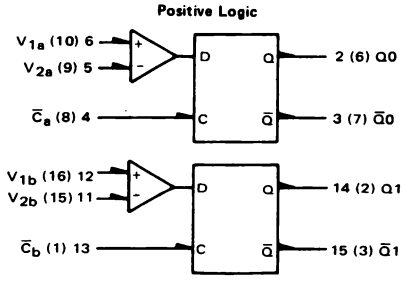


FIGURE 14 — POWER OUTPUT versus COLLECTOR LOAD

See test circuit, Figure 12, f = 10 MHz
C3 = 470 pF
Collector Tank
L1 = 2.7 μH C1 = 24 - 200 pF
R = 50 Ω - 10 kΩ
Rp of L1 and C1 = 6.8 kΩ @ 10 MHz Resonance
Oscillator Tank
L2 = 2.7 μH
C2 = 16 - 150 pF



MC1650 • MC1651



V_{CC} = +5.0 V = Pin 7,10 - (11), (14)
V_{EE} = -5.2 V = Pin 8 (12)
Gnd = Pin 1,16 (4) (5)

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (MC1650)
  = 3.0 ns typ (MC1651)
- Input Slew Rate = 350 V/μs (MC1650)
  = 500 V/μs (MC1651)
- Differential Input Voltage:
  -5.0 V to +5.0 V (-30°C to +85°C)
- Common Mode Range:
  -3.0 V to +2.5 V (-30°C to +85°C) (MC1651)
  -2.5 V to +3.0 V (-30°C to +85°C) (MC1650)
- Resolution: ≤20 mV (-30°C to +85°C)
- Drives 50 Ω lines

Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

The MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC-1651 is a lower impedance option, with higher input slew rate and higher speed capability.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock inputs ($\overline{C}_a$ and $\overline{C}_b$) operate from MECL III or MECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}0$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

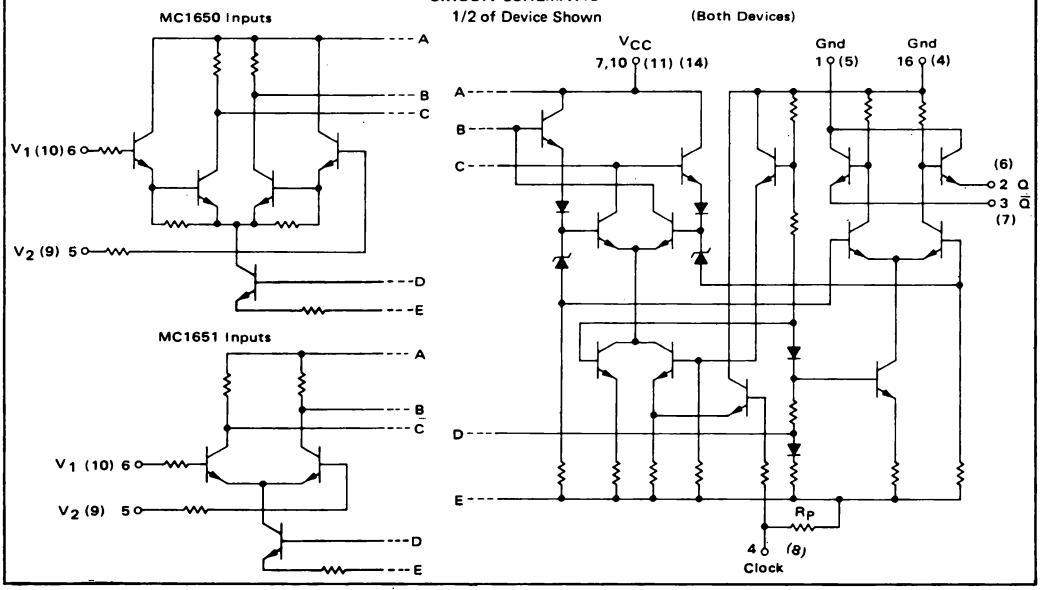
Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the relative behaviors shown in Figures 3 and 6.

TRUTH TABLE

$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

ϕ = Don't Care

CIRCUIT SCHEMATIC

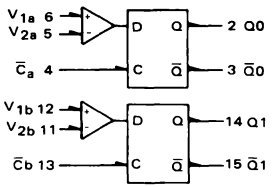


See General Information section for packaging information.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

POSITIVE LOGIC



L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

Characteristic	Symbol	Pin Under Test	MC1650L/1651L Test Limits ① -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
Power Supply Drain Current																						
Positive	I_{CC}	7,10	–	–	–	25*	–	–	mAdc	–	4,13	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
Negative	I_E	8	–	–	–	55*	–	–	mAdc	4,13	–	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
Input Current	I_{in}																					
MC1650		6	–	–	–	10	–	–	μAdc	4	13	–	–	12	–	6	–	–	–	7,10	8	1,5,11,16
MC1651		6	–	–	–	40	–	–	μAdc	4	13	–	–	12	–	6	–	–	–	7,10	8	1,5,11,16
Input Leakage Current	I_R																					
MC1650		6	–	–	–	7	–	–	μAdc	4	13	–	–	12	–	–	–	6	–	7,10	8	1,5,11,16
MC1651		6	–	–	–	10	–	–	μAdc	4	13	–	–	12	–	–	–	6	–	7,10	8	1,5,11,16
Input Clock Current	$I_{in}H$	4	–	–	–	350	–	–	μAdc	4	13	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
	$I_{in}L$	4	–	–	0.5	–	–	–	μAdc	–	13	–	–	6,12	–	–	–	–	–	7,10	4,8	1,5,11,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13	–	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
		2									–	–	–	–	5,11	–	–	–	–			1,6,12,16
		2									–	–	–	–	–	6,12	5,11	–	–			1,16
		2									–	–	–	–	–	–	–	5,11	6,12			1,16
		3									–	–	–	–	6,12	–	–	–	–			1,5,11,16
		3									–	–	–	5,11	–	–	–	–	–			1,6,12,16
		3									–	–	–	–	–	5,11	6,12	–	–			1,16
		3									–	–	–	–	–	–	–	6,12	5,11			1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13	–	–	–	–	6,12	–	–	–	–	7,10	8	1,5,11,16
		2									–	–	–	5,11	–	–	–	–	–			1,6,12,16
		2									–	–	–	–	–	5,11	6,12	–	–			1,16
		2									–	–	–	–	–	–	–	6,12	5,11			1,16
		3									–	–	–	6,12	–	–	–	–	–			1,5,11,16
		3									–	–	–	–	5,11	–	–	–	–			1,6,12,16
		3									–	–	–	–	–	6,12	5,11	–	–			1,16
		3									–	–	–	–	–	–	–	5,11	6,12			1,16
Logic "1" Threshold Voltage ②	V_{OHA}	1	-1.065	–	-0.980	–	-0.910	–	Vdc	–	13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
		2								–	–	–	4	–	6	–	–	–	–			
		3								–		4	–	–	6	–	–	–	–			
		4								–		–	4	6	–	–	–	–	–			
Logic "0" Threshold Voltage ②	V_{OLA}	1	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
		2								–	–	–	4	–	6	–	–	–	–			
		3								–		4	–	–	6	–	–	–	–			
		4								–		–	4	6	–	–	–	–	–			

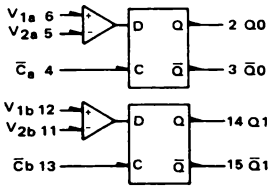
NOTES: ① All data is for ½ MC1650 or MC1651, except data marked (*) which refers to the entire package.
② These tests done in order indicated. See Figure 4.
③ Maximum Power Supply Voltages (beyond which device life may be impaired):
$|V_{EE}| + |V_{CC}| \leq 12$ Vdc.

④

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
MC1650	+3.000	+2.980	-2.500	-2.480
MC1651	+2.500	+2.480	-3.000	-2.980

SWITCHING TIMES

POSITIVE LOGIC



L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	See Figure 2
-30°C	+2.000	See Note ④		+1.040	+2.00	+7.00	-3.20	
+25°C	+2.000			+1.110	+2.00	+7.00	-3.20	
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20	

Characteristic	Symbol	Pin Under Test	MC1650L/1651L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	P1	P2	P3	P4
Switching Times																				
Propagation Delay	t_{6+2+}	2	2.0	5.0	2.0	5.0	2.0	5.7	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
(50% to 50%)	t_{6+2+}	2								–	5	–					–	6	–	–
	t_{6+2+}	2								–	–	5					–	–	6	–
V-Input to Output	t_{6+3-}	3								5	–	–					6	–	–	–
	t_{6+3-}	3								–	5	–					–	6	–	–
	t_{6+3-}	3								–	–	5					–	–	6	–
	t_{6-2-}	2								5	–	–					6	–	–	–
	t_{6-2-}	2								–	5	–					–	6	–	–
	t_{6-2-}	2								–	–	5					–	–	6	–
	t_{6-3+}	3								5	–	–					6	–	–	–
	t_{6-3+}	3								–	5	–					–	6	–	–
	t_{6-3+}	3								–	–	5					–	–	6	–
Clock to Output ②	t_{4+2+}	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
	t_{4+2-}	2								6	–	–	–				5	–	–	
	t_{4+3+}	3								6	–	–	–				5	–	–	
	t_{4+3-}	3								5	–	–	–				6	–	–	
Clock Enable Time ③	t_{setup}	6	–	–	2.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Clock Aperture Time ③	t_{ap}	6	–	–	1.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Rise Time																				
(10% to 90%)	t_{2+}	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3+}	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
Fall Time																				
(10% to 90%)	t_{2-}	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3-}	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–

NOTES: ① Maximum Power Supply Voltages (beyond which device life may be impaired:
$|V_{CC}| + |V_{EE}| \leq 12$ Vdc.

② Unused clock inputs may be tied to ground.

③ See Figure 8.

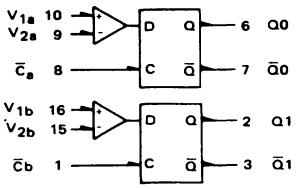
④

All Temperatures	V_{R2}	V_{R3}
MC1650	+4.900	-0.400
MC1651	+4.400	-0.900

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

POSITIVE LOGIC



F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts)											
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

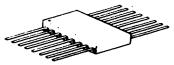
Characteristic	Symbol	Pin Under Test	MC1650F/1651F Test Limits ① -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
Power Supply Drain Current																						
Positive	I_{CC}	11,14	–	–	–	25*	–	–	mAdc	–	1,8	–	–	10,16	–	–	–	–	–	11,14	12	4,5,9,15
Negative	I_E	12	–	–	–	55*	–	–	mAdc	1,8	–	–	–	10,16	–	–	–	–	–	11,14	12	4,5,9,15
Input Current	I_{in}																					
MC1650		10	–	–	–	10	–	–	μAdc	8	1	–	–	16	–	10	–	–	–	11,14	12	4,5,9,15
MC1651		10	–	–	–	40	–	–	μAdc	8	1	–	–	16	–	10	–	–	–	11,14	12	4,5,9,15
Input Leakage Current	I_R																					
MC1650		10	–	–	–	7	–	–	μAdc	8	1	–	–	16	–	–	–	10	–	11,14	12	4,5,9,15
MC1651		10	–	–	–	10	–	–	μAdc	8	1	–	–	16	–	–	–	10	–	11,14	12	4,5,9,15
Input Clock Current	$I_{in}H$	8	–	–	–	350	–	–	μAdc	8	1	–	–	10,16	–	–	–	–	–	11,14	12	4,5,9,15
	$I_{in}L$	8	–	–	0.5	-	–	–	μAdc	–	1	–	–	10,16	–	–	–	–	–	11,14	8,12	4,5,9,15
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	1,8	–	–	–	10,16	–	–	–	–	–	11,14	12	4,5,9,15
		6									–	–	–	–	9,15	–	–	–	–			4,5,10,16
		6									–	–	–	–	–	10,16	9,15	–	–			4,5
		6									–	–	–	–	–	–	–	9,15	10,16			4,5
		7									–	–	–	–	10,16	–	–	–	–			4,5,9,15
		7									–	–	–	9,15	–	–	–	–	–			4,5,10,16
		7									–	–	–	–	–	9,15	10,16	–	–			4,5
		7									–	–	–	–	–	–	–	10,16	9,15			4,5
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	1,8	–	–	–	–	10,16	–	–	–	–	11,14	12	4,5,9,15
		6									–	–	–	9,15	–	–	–	–	–			4,5,10,16
		6									–	–	–	–	–	9,15	10,16	–	–			4,5
		6									–	–	–	–	–	–	–	10,16	9,15			4,5
		7									–	–	–	10,16	–	–	–	–	–			1,5,11,16
		7									–	–	–	–	9,15	–	–	–	–			1,6,12,16
		7									–	–	–	–	–	10,16	9,15	–	–			1,16
		7									–	–	–	–	–	–	–	9,11	10,16			1,16
Logic "1" Threshold Voltage ②	V_{OHA}	6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	1	8	–	10	–	–	–	–	–	11,14	12	4,5,9
		6		–		–		–		–		–	8	–	10	–	–	–	–			
		7		–		–		–		–		8	–	–	10	–	–	–	–			
		7		–		–		–		–		–	8	10	–	–	–	–	–			
Logic "0" Threshold Voltage ②	V_{OLA}	7	–	-1.630	–	-1.600	–	-1.555	Vdc	–	1	8	–	10	–	–	–	–	–	11,14	12	4,5,9
		7	–		–		–			–		–	8	–	10	–	–	–	–			
		6	–		–		–			–		8	–	–	10	–	–	–	–			
		6	–		–		–			–		–	8	10	–	–	–	–	–			

NOTES: ① All data is for ½ MC1650 or MC1651, except data marked (*) which refers to the entire package.
② These tests done in order indicated. See Figure 4.
③ Maximum Power Supply Voltages (beyond which device life may be impaired):
$|V_{EE}| + |V_{CC}| \leq 12$ Vdc.

④

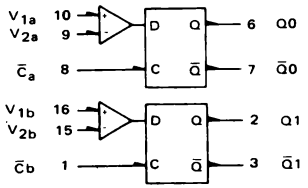
All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
MC1650	+3.000	+2.980	-2.500	-2.480
MC1651	+2.500	+2.480	-3.000	-2.980

SWITCHING TIMES (continued)



F SUFFIX
CERAMIC PACKAGE
CASE 650

POSITIVE LOGIC



@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①
-30°C	+2.000	See Note ④		+1.040	+2.00	+7.00	-3.20
+25°C	+2.000			+1.110	+2.00	+7.00	-3.20
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20

Characteristic	Symbol	Pin Under Test	MC1650F/1651F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	P1	P2	P3	P4
Switching Times	t_{10+6+}	6	2.0	5.0	2.0	5.0	2.0	5.7	ns	9	–	–	8	4,5,16	11,14	12	10	–	–	–
Propagation Delay	t_{10+6+}	6								–	9	–					–	10	–	–
(50% to 50%)	t_{10+6+}	6								–	–	9					–	–	10	–
V-Input to Output	t_{10+7-}	7								9	–	–					10	–	–	–
	t_{10+7-}	7								–	9	–					–	10	–	–
	t_{10+7-}	7								–	–	9					–	–	10	–
	t_{10-6-}	6								9	–	–					10	–	–	–
	t_{10-6-}	6								–	9	–					–	10	–	–
	t_{10-6-}	6								–	–	9					–	–	10	–
	t_{10-7+}	7								9	–	–					10	–	–	–
	t_{10-7+}	7								–	9	–					–	10	–	–
	t_{10-7+}	7								–	–	9					–	–	10	–
Clock to Output ②	t_{8+6+}	6	2.0	4.7	2.0	4.7	2.0	5.2	ns	9	–	–	–	4,5,16	11,14	12	10	–	–	8
	t_{8+6-}	6								10	–	–	–				9	–	–	
	t_{8+7+}	7								10	–	–	–				9	–	–	
	t_{8+7-}	7								9	–	–	–				10	–	–	
Clock Enable Time ③	t_{setup}	10	–	–	2.5	–	–	–	ns	9	–	–	–	4,5,16	11,14	12	10	–	–	8
Clock Aperture Time ③	t_{ap}	10	–	–	1.5	–	–	–	ns	9	–	–	–	4,5,16	11,14	12	10	–	–	8
Rise Time	t_{6+}	6	1.0	3.5	1.0	3.5	1.0	3.8	ns	9	–	–	8	4,5,16	11,14	12	10	–	–	–
(10% to 90%)	t_{7+}	7	1.0	3.5	1.0	3.5	1.0	3.8	ns	9	–	–	8	4,5,16	11,14	12	10	–	–	–
Fall Time	t_{6-}	6	1.0	3.0	1.0	3.0	1.0	3.3	ns	9	–	–	8	4,5,16	11,14	12	10	–	–	–
(10% to 90%)	t_{7-}	7	1.0	3.0	1.0	3.0	1.0	3.3	ns	9	–	–	8	4,5,16	11,14	12	10	–	–	–

See Figure 2

NOTES: ① Maximum Power Supply Voltages (beyond which device life may be impaired: $|V_{CC}| + |V_{EE}| \leq 12$ Vdc.

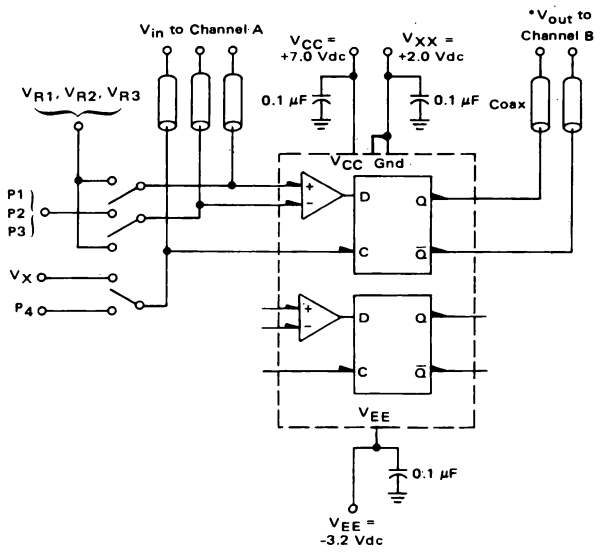
② Unused clock inputs may be tied to ground.

③ See Figure 8.

④

All Temperatures	V_{R2}	V_{R3}
MC1650	+4.900	-0.400
MC1651	+4.400	-0.900

FIGURE 1 – SWITCHING TIME TEST CIRCUIT @ 25°C



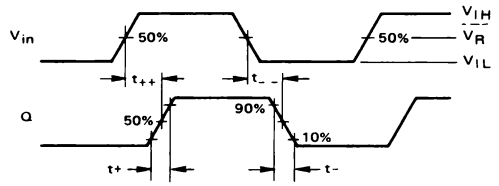
50-ohm termination to ground located in each scope channel input
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

*Complement of output under test should always be loaded with 50-ohms to ground.

FIGURE 2 – SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output

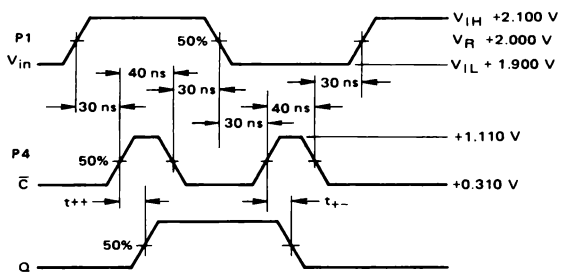


Test pulses: $t_+, t_- = 1.5 \pm 0.2$ ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle
V_{IH} is applied to $\overline{C}$ during tests.

TEST PULSE LEVELS

	Pulse 1		Pulse 2		Pulse 3	
	MC1650	MC1651	MC1650	MC1651	MC1650	MC1651
V_{IH}	+2.100 V	+2.100 V	+5.000 V	+4.500 V	-0.300 V	-0.800 V
V_R	+2.000 V	+2.000 V	+4.900 V	+4.400 V	-0.400 V	-0.900 V
V_{IL}	+1.900 V	+1.900 V	+4.800 V	+4.300 V	-0.500 V	-1.000 V

Clock to Output



P4: $t_+, t_- = 1.5 \pm 0.2$ ns.

FIGURE 3 – PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE

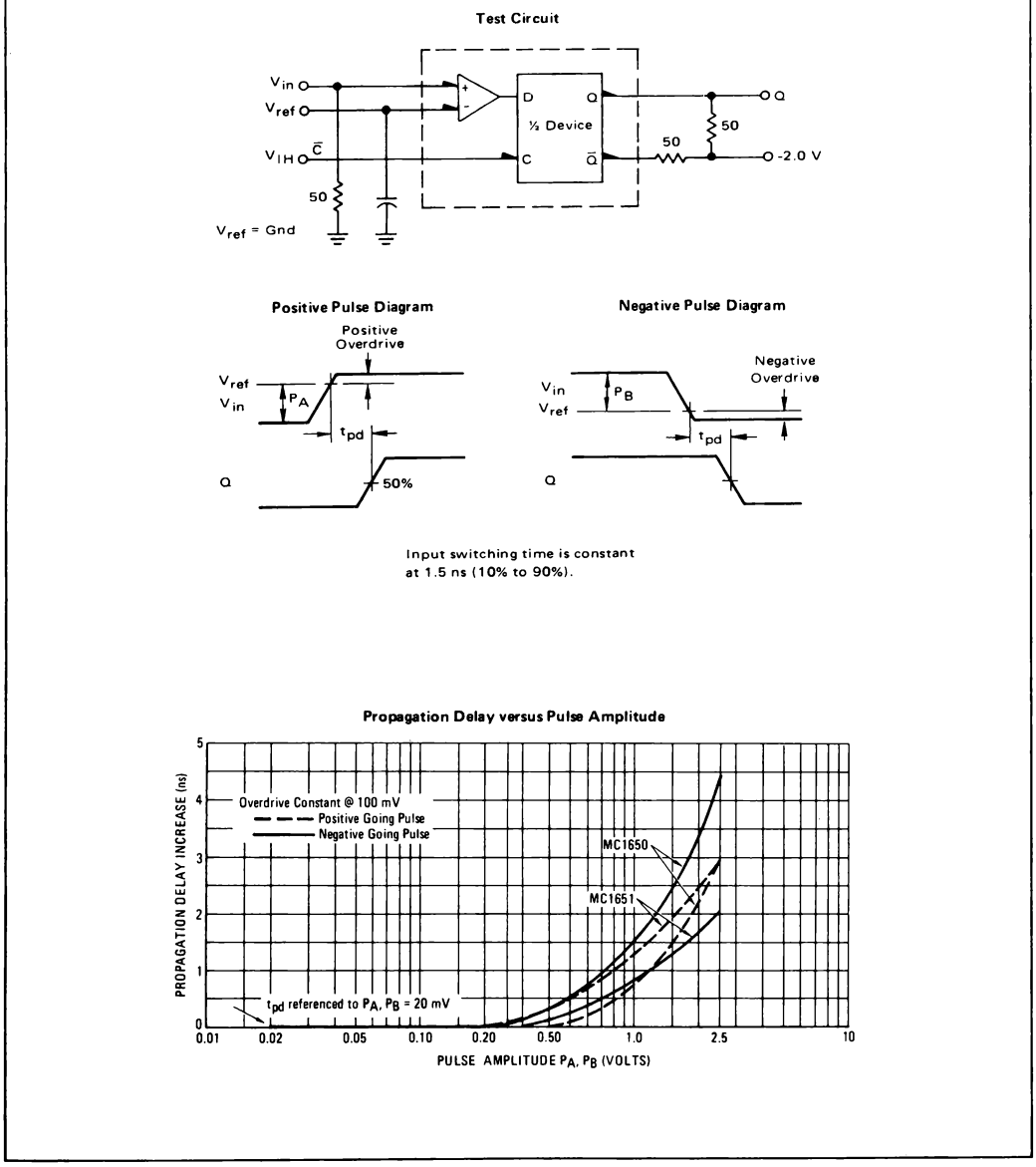


FIGURE 3 (continued)

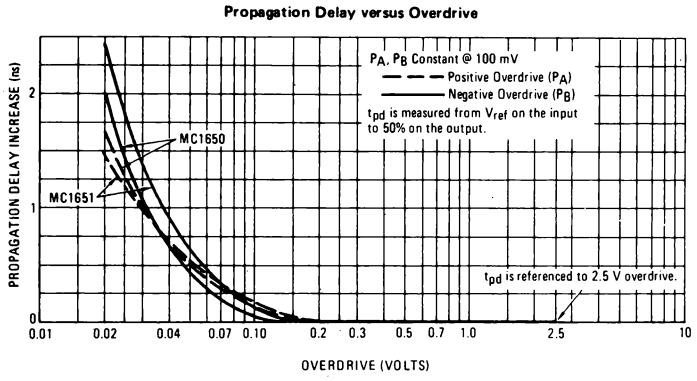


FIGURE 4 – LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

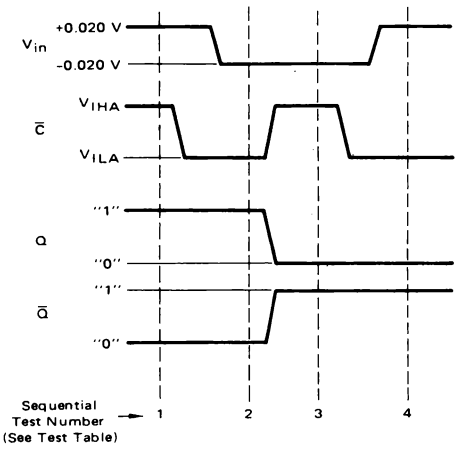
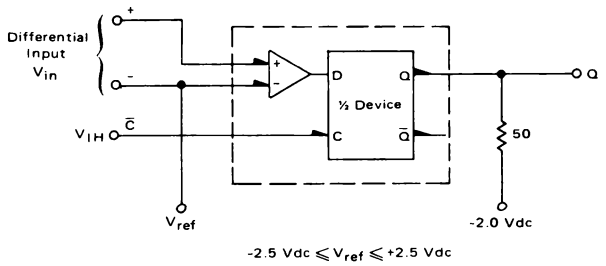


FIGURE 5 – TRANSFER CHARACTERISTICS (Q versus V_{in})

Test Configuration



$-2.5\ Vdc \leqslant V_{ref} \leqslant +2.5\ Vdc$

Typical Transfer Curves

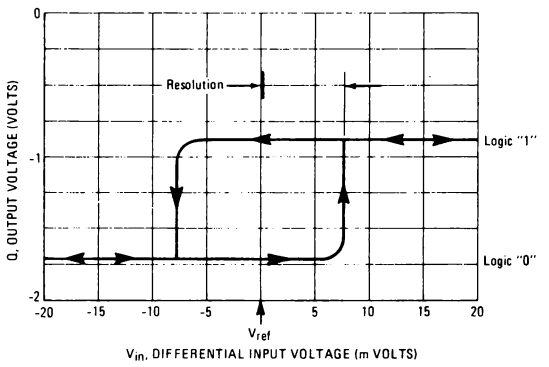
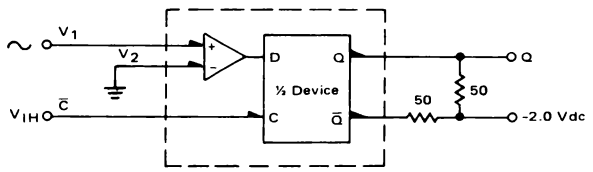
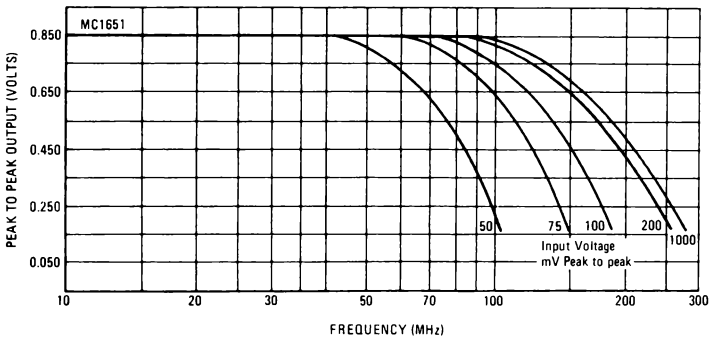


FIGURE 6 – OUTPUT VOLTAGE SWING versus FREQUENCY

(A) Test Circuit



(B) Typical Output Logic Swing versus Frequency



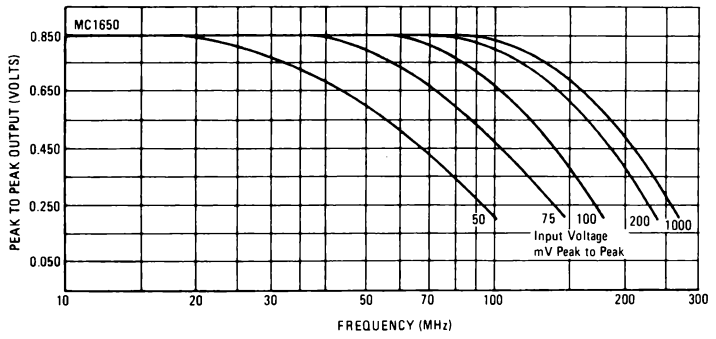
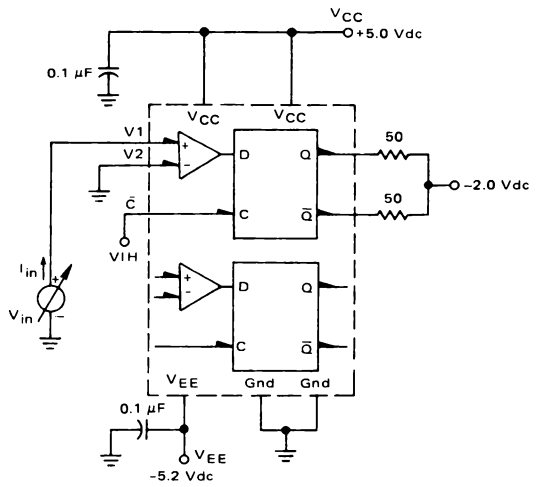
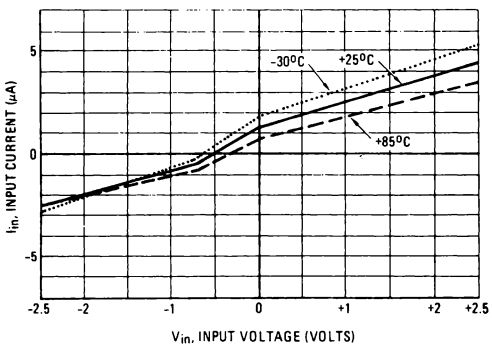


FIGURE 7 – INPUT CURRENT versus INPUT VOLTAGE

TEST CIRCUIT



Typical MC1650 (Complementary Input Grounded)



Typical MC1651 (Complementary Input Grounded)

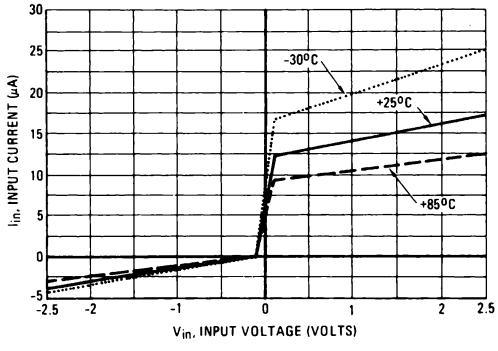
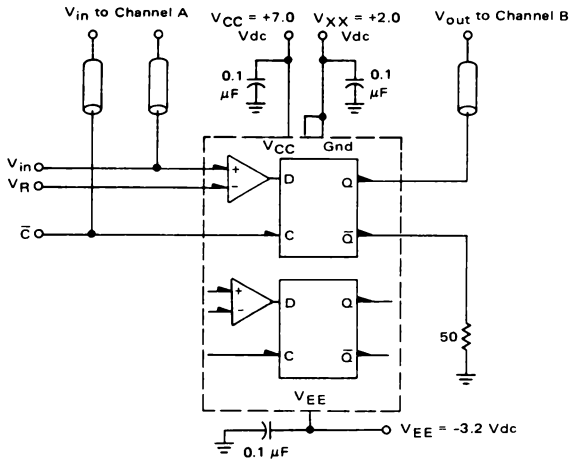


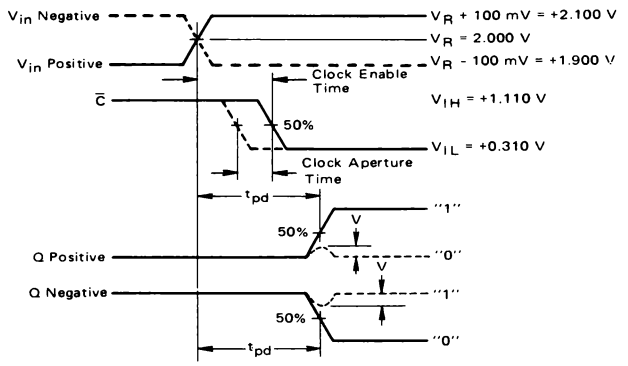
FIGURE 8 – CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Analog Signal Positive and Negative Slew Case



Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

MC1654

The MC1654 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight, or a divide-by-16 functions. When used independently, the divide-by-16 section will toggle at 325 MHz typically. Clock inputs trigger on the positive going edge of the Clock pulse.

Set and Reset inputs override the Clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

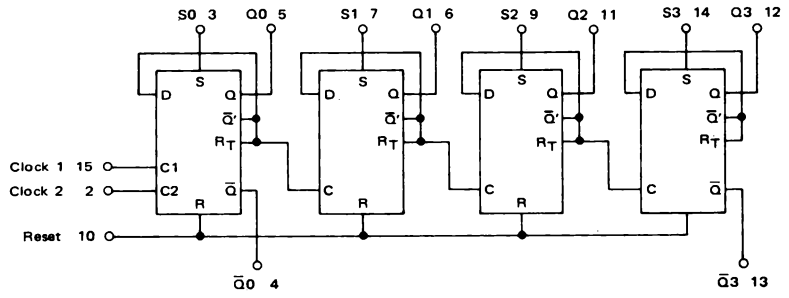
TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
1	0	0	0	0	ϕ	ϕ	0	0	0	0
0	1	1	1	1	ϕ	ϕ	1	1	1	1
0	0	0	0	0	1	ϕ	No Count			
0	0	0	0	0	ϕ	1	No Count			
0	0	0	0	0	••		0	0	0	0
0	0	0	0	0	••		1	0	0	0
0	0	0	0	0	••		0	1	0	0
0	0	0	0	0	••		1	1	0	0
0	0	0	0	0	••		0	0	1	0
0	0	0	0	0	••		1	0	1	0
0	0	0	0	0	••		0	1	1	0
0	0	0	0	0	••		1	1	1	0
0	0	0	0	0	••		0	0	0	1
0	0	0	0	0	••		1	0	0	1
0	0	0	0	0	••		0	1	0	1
0	0	0	0	0	••		1	1	0	1
0	0	0	0	0	••		0	0	1	1
0	0	0	0	0	••		1	0	1	1
0	0	0	0	0	••		0	1	1	1
0	0	0	0	0	••		1	1	1	1

ϕ = Don't Care

•• V_{IL} ⌐ V_{IH} Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

Power Dissipation = 750 mW typ
f_{Tog} = 325 MHz typ



V_{CC} = 1, 16
V_{EE} = 8

See General Information section for packaging.

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN

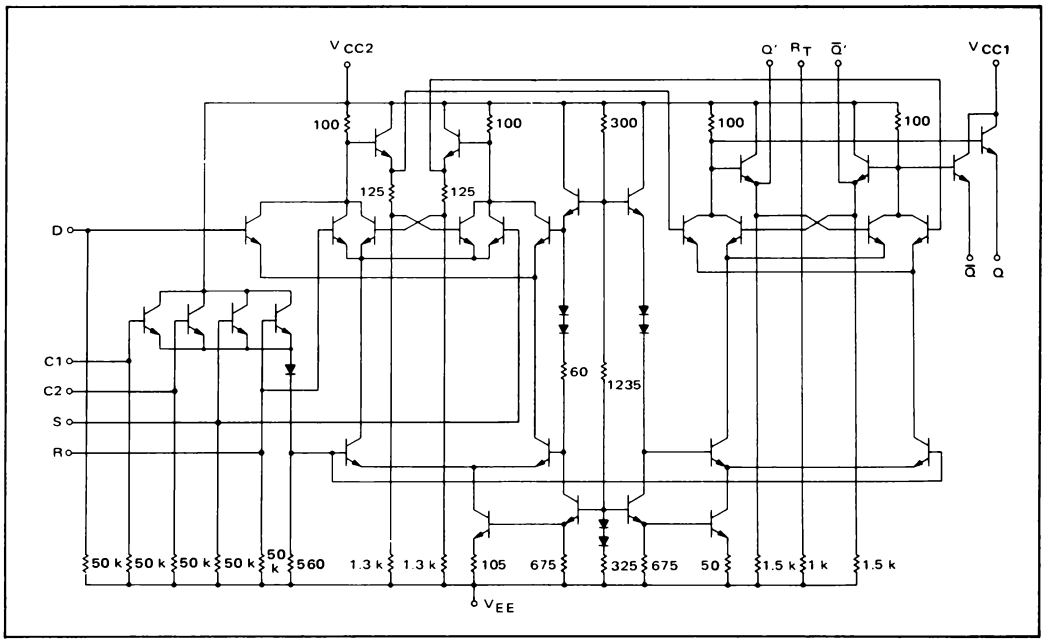
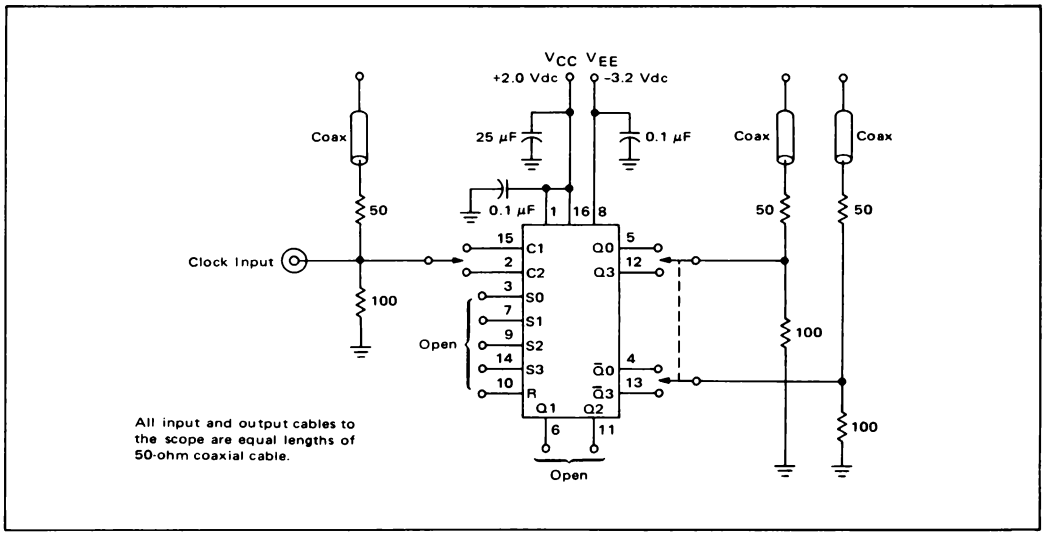
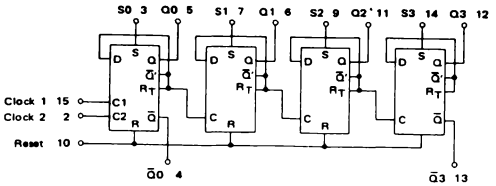


FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package requires a heat sink (IERC LIC214A2 or equivalent). Outputs are tested with a 50-ohm resistor to -2.0 V. See general information section of the MECL III series for complete thermal data.



L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

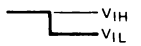
Characteristic	Symbol	Pin Under Test	MC1654 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	200	–	–	mAdc	10	–	–	–	8	1,16
Input Current	$I_{in\ H}$	10	–	–	–	1.00	–	–	mAdc	10	–	–	–	8	1,16
		2,3,7,9,14,15	–	–	–	0.60	–	–	mAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	10	–	–	0.5	–	–	–	µAdc	–	10	–	–	8	1,16
		2,3,7,9,14,15	–	–	0.5	–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	4,13 ①	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	3,7,9,14	–	–	8	1,16
		5,6,11,12 ②	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	4,13 ②	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	10	–	–	8	1,16
		5,6,11,12 ①	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	3,7,9,14	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	4,13 ③	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	3,7,9,14	8	1,16
		5,6,11,12 ④	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	10	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	4,13 ④	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	10	8	1,16
		5,6,11,12 ③	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	3,7,9,14	8	1,16
AC Characteristics												**Pulse In**	**Pulse Out**	**-3.2 Vdc**	**+2.0 Vdc**
Clock Delays (50 Ω Load)	t_{15+4+}	4	1.0	2.9	1.0	2.7	1.0	3.1	ns	–	–	15	4	8	1,16
	t_{15+5+}	5	↓	↓	↓	↓	↓	↓	↓	–	–	15	5	↓	↓
	t_{2+4+}	4	↓	↓	↓	↓	↓	↓	↓	–	–	2	4	↓	↓
	t_{2+5+}	5	↓	↓	↓	↓	↓	↓	↓	–	–	2	5	↓	↓
	t_{15+4-}	4	1.0	2.9	1.0	2.7	1.0	3.1	ns	–	–	15	4	8	1,16
	t_{15+5-}	5	↓	↓	↓	↓	↓	↓	↓	–	–	15	5	↓	↓
	t_{2+4-}	4	↓	↓	↓	↓	↓	↓	↓	–	–	2	4	↓	↓
	t_{2+5-}	5	↓	↓	↓	↓	↓	↓	↓	–	–	2	5	↓	↓
Set Delay	t_{3+4+}	4	2.0	3.9	2.0	3.7	2.0	4.1	ns	–	–	3	4	8	1,16
	t_{3+5-}	5	2.0	3.9	2.0	3.7	2.0	4.1	ns	–	–	3	5	8	1,16
Reset Delay	t_{10+4+}	4	2.0	3.9	2.0	3.7	2.0	4.1	ns	–	–	10	4	8	1,16
	t_{10+5-}	5	2.0	3.9	2.0	3.7	2.0	4.1	ns	–	–	10	5	8	1,16
Rise Time	t_{4+}	4	1.0	2.9	1.0	2.7	1.0	3.1	ns	–	–	15	4	8	1,16
	t_{5+}	5	1.0	2.9	1.0	2.7	1.0	3.1	ns	–	–	15	5	8	1,16
Fall Time	t_{4-}	4	1.0	2.8	1.0	2.6	1.0	3.0	ns	–	–	15	4	8	1,16
	t_{5-}	5	1.0	2.8	1.0	2.6	1.0	3.0	ns	–	–	15	5	8	1,16
Maximum Toggle Frequency	f_t	3 ⑤	260	–	300	–	260	–	MHz	–	–	–	–	8	1,16

*Individually apply V_{IH} or V_{IL} to input under test.

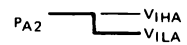
① Reset all four flip-flops by applying P_{A1} to pin 10

② Set all four flip-flops by applying P_{A1} to pins 3, 7, 9, and 14 simultaneously.

③ Reset all four flip-flops by applying P_{A2} to pin 10



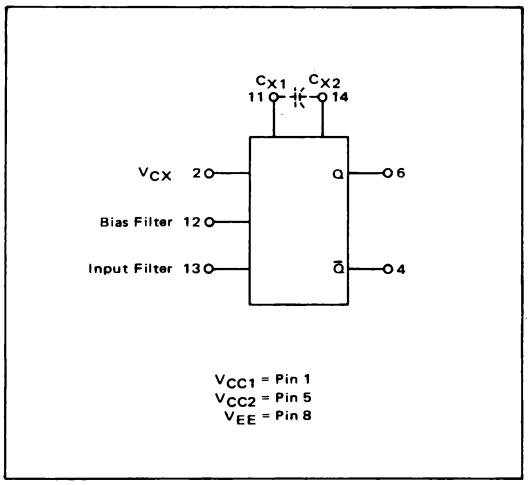
④ Set all four flip-flops by applying P_{A2} to pins 3, 7, 9, and 14 simultaneously.



⑤ See Figure 1 for toggle test circuit

VOLTAGE-CONTROLLED MULTIVIBRATOR

MC1658

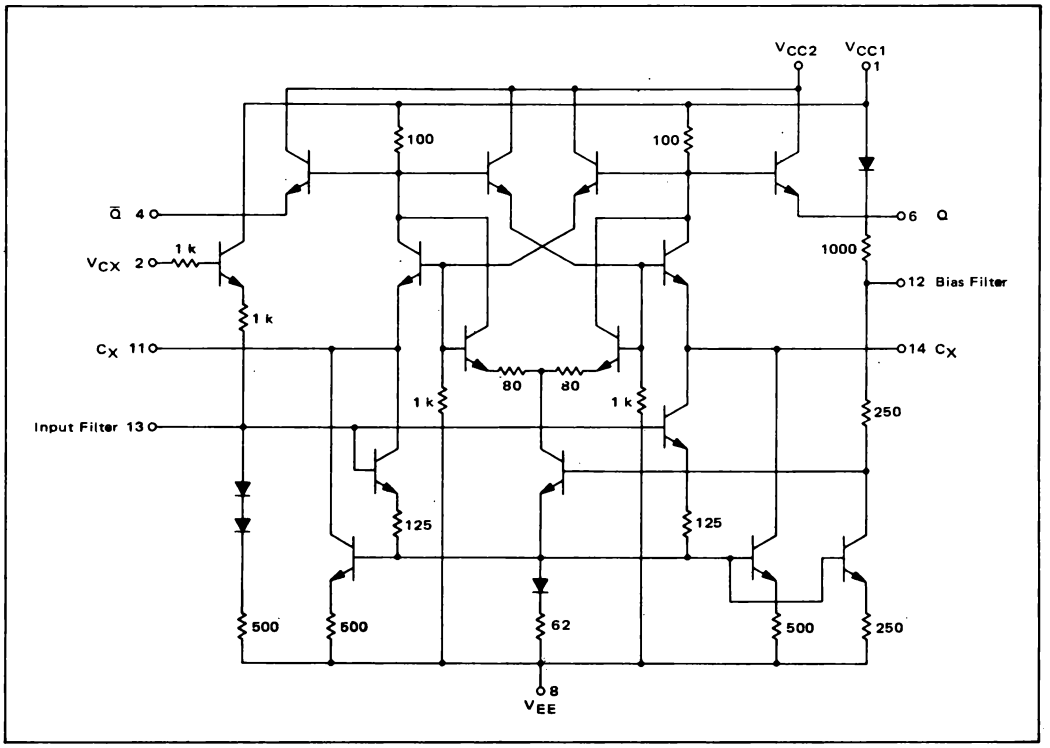


The MC1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with MECL III and MECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The MC1658 is useful in phase-locked loops, frequency synthesizer and clock signal generation applications for instrumentation, communication, and computer systems.

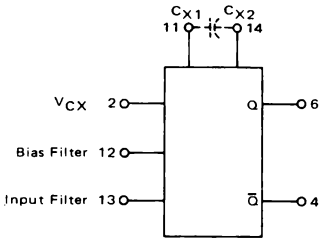
FIGURE 1 – CIRCUIT SCHEMATIC

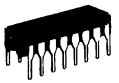


See General Information Section for packaging.

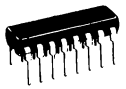
ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

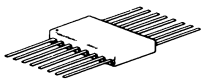




L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Vdc ±1%) V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}
-30°C	0.0	-2.0	-1.0	+2.0	-5.2
+25°C	0.0	-2.0	-1.0	+2.0	-5.2
+85°C	0.0	-2.0	-1.0	+2.0	-5.2

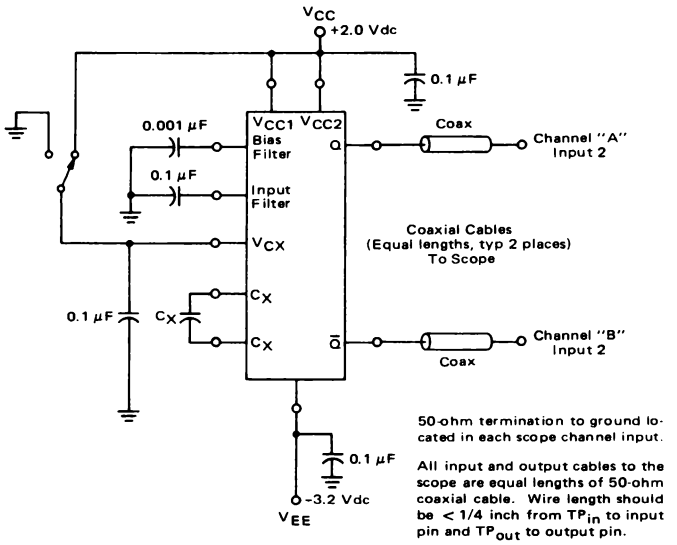
Characteristic	Symbol	Pin Under Test	MC1658 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8*	–	–	–	–	32	–	–	mAdc	2	–	–	–	8	1,5
		8**	–	–	–	–	32	–	–	mAdc	2	–	–	–	8	1,5
Input Current	I_{inH}	2*	–	–	–	–	350	–	–	μAdc	2	–	–	–	8	1,5
Input Leakage Current	I_{inL}	2*	–	–	0.5	–	–	–	–	μAdc	–	2	–	–	8	1,5
"Q" High Output Voltage	V_{OH}	4*	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	–	8	1,5
		6**	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	–	8	1,5
"Q̄" Low Output Voltage	V_{OL}	4*	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	–	8	1,5
		6**	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	–	8	1,5
AC Characteristics (Figure 2) (Tests shown for one output, but checked on both)											C_{X1}	C_{X2}	Gnd		V_{EE} -3.2 V	V_{CC} +2.0 V
Rise Time (10% to 90%)	t+	6	–	2.7	–	1.6	2.7	–	3.0	ns	–	11,14	–	2	8	1,15
Fall Time (10% to 90%)	t-	6	–	2.7	–	1.4	2.7	–	3.0	ns	–	11,14	–	2	2	1,15
Oscillator Frequency	f_{osc1}	–	130	–	130	155	175	110	–	MHz	–	11,14	–		8	1,5
	f_{osc2}	–	–	–	78	90	100	–	–	MHz	11,14	–	–		8	1,5
Tuning Ratio Test †	TR	–	–	–	3.1	4.5	–	–	–	–	11,14	–	–		8	1,5

*Germanium diode (0.4 drop) forward biased from 11 to 14 (11 ⟶|⟵ 14).
**Germanium diode (0.4 drop) forward biased from 14 to 11 (11 ⟶|⟵ 14).

$$\dagger TR = \frac{\text{Output frequency at } V_{CX} = \text{Gnd}}{\text{Output frequency at } V_{CX} = -2.0\ V}$$

C1 = 0.01 μF connected from pin 12 to Gnd.
C2 = 0.001 μF connected from pin 13 to Gnd.
C_{X1} = 10 pF connected from pin 11 to pin 14.
C_{X2} = 5 pF connected from pin 11 to pin 14.

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



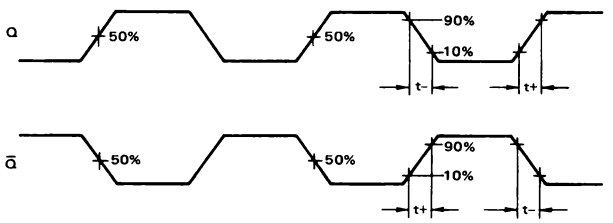


FIGURE 3 – OUTPUT FREQUENCY versus CAPACITANCE FOR VARIOUS VALUES OF INPUT VOLTAGE

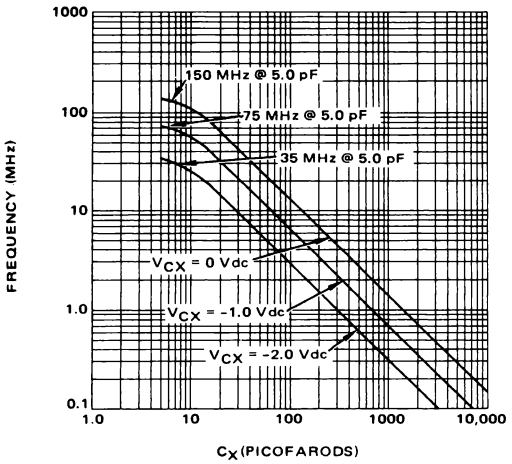


FIGURE 4 – RMS NOISE DEVIATION versus OPERATING FREQUENCY

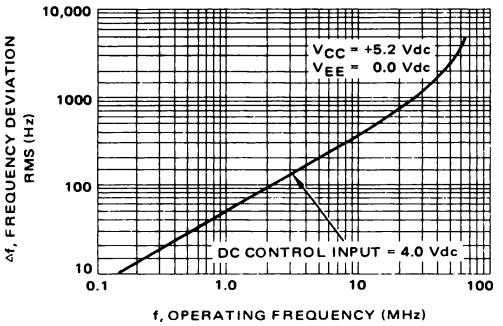
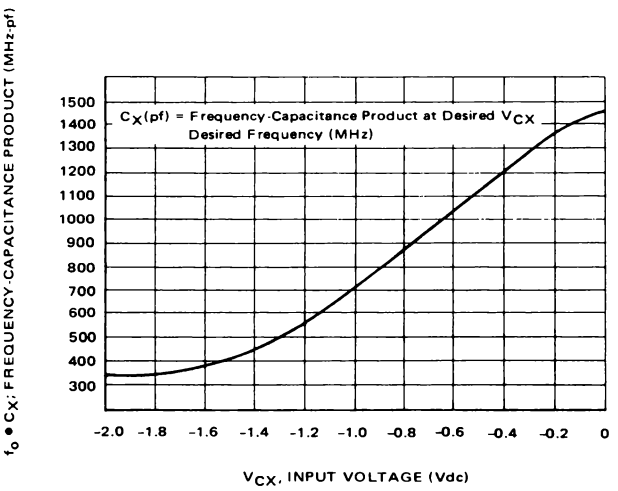


FIGURE 5 – FREQUENCY-CAPACITANCE PRODUCT versus CONTROL VOLTAGE (V_{CX})

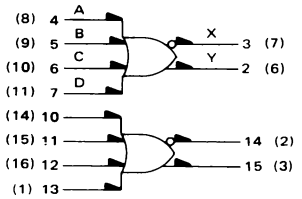


DUAL 4-INPUT GATE

MC1660

MC1660 provides simultaneous OR-NOR or AND-NAND output functions with the capability of driving 50-ohm lines. These devices contain an internal bias reference voltage insuring that the threshold point is always in the center of the transition region over the temperature range (-30° to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

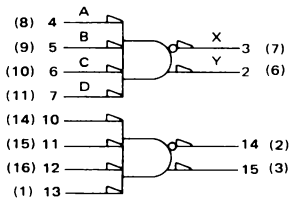
POSITIVE LOGIC



$X = \overline{A + B + C + D}$

$Y = A + B + C + D$

NEGATIVE LOGIC



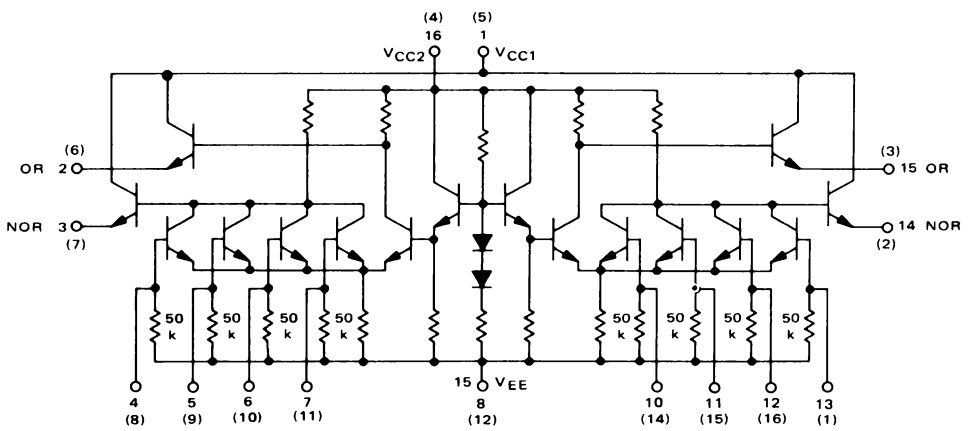
$X = \overline{A \bullet B \bullet C \bullet D}$

$Y = A \bullet B \bullet C \bullet D$

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 120 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

CIRCUIT SCHEMATIC

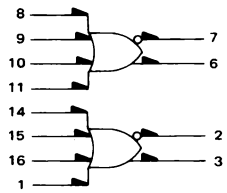


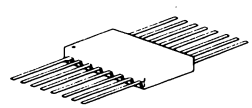
Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





F SUFFIX
CERAMIC PACKAGE
CASE 650

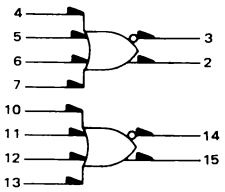
@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

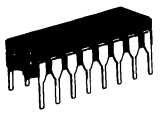
Characteristic	Symbol	Pin Under Test	MC1660F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–	28	–	–	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	*	–	–	–	350	–	–	μAdc	*	–	–	–	12	4,5
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	12	4,5
NOR Logic "1" Output Voltage	V_{OH}	7	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	– – – –	8 9 10 11	– – – –	– – – –	12	4,5
NOR Logic "0" Output Voltage	V_{OL}	7	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	8 9 10 11	– – – –	– – – –	– – – –	12	4,5
OR Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	8 9 10 11	– – – –	– – – –	– – – –	12	4,5
OR Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	– – – –	8 9 10 11	– – – –	– – – –	12	4,5
NOR Logic "1" Threshold Voltage	V_{OHA}	7	-1.065	– – – –	-0.980	– – – –	-0.910	– – – –	Vdc	– – – –	– – – –	– – – –	8 9 10 11	12	4,5
NOR Logic "0" Threshold Voltage	V_{OLA}	7	– – – –	-1.630	– – – –	-1.600	– – – –	-1.555	Vdc	– – – –	– – – –	8 9 10 11	– – – –	12	4,5
OR Logic "1" Threshold Voltage	V_{OHA}	6	-1.065	– – – –	-0.980	– – – –	-0.910	– – – –	Vdc	– – – –	– – – –	8 9 10 11	– – – –	12	4,5
OR Logic "0" Threshold Voltage	V_{OLA}	6	– – – –	-1.630	– – – –	-1.600	– – – –	-1.555	Vdc	– – – –	– – – –	– – – –	8 9 10 11	12	4,5
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{8+7-}	7	–	1.8	–	1.7	–	1.9	ns	8	7	–	–	12	4,5
	t_{8-6-}	6	–	1.8	–	1.7	–	1.9			6	–	–		
	t_{8+6+}	6	–	1.6	–	1.5	–	1.7			6	–	–		
	t_{8-7+}	7	–	1.6	–	1.5	–	1.7			7	–	–		
Rise Time	t_{7+}	7	–	2.2	–	2.1	–	2.3	ns	8	7	–	–	12	4,5
	t_{6+}	6	–	2.2	–	2.1	–	2.3	ns	8	6	–	–	12	4,5
Fall Time	t_{7-}	7	–	2.2	–	2.1	–	2.3	ns	8	7	–	–	12	4,5
	t_{6-}	6	–	2.2	–	2.1	–	2.3	ns	8	6	–	–	12	4,5

*Individually test each input applying V_{IH} or V_{IL} to the input under test.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1660L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
NOR Logic "1" Output Voltage	$V_{OH}\phi$	3	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	– – –	4 5 6 7	– – –	– – –	8	1,16
NOR Logic "0" Output Voltage	$V_{OL}\phi$	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4 5 6 7	– – – –	– – – –	– – – –	8	1,16
OR Logic "1" Output Voltage	$V_{OH}\phi$	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4 5 6 7	– – – –	– – – –	– – – –	8	1,16
OR Logic "0" Output Voltage	$V_{OL}\phi$	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	– – – –	4 5 6 7	– – – –	– – – –	8	1,16
NOR Logic "1" Threshold Voltage	$V_{OHA}\phi$	3	-1.065	– – – –	-0.980	– – – –	-0.910	– – – –	Vdc	– – – –	– – – –	– – – –	4 5 6 7	8	1,16
NOR Logic "0" Threshold Voltage	$V_{OLA}\phi$	3	–	-1.630	–	-1.600	–	-1.555	Vdc	– – – –	– – – –	4 5 6 7	– – – –	8	1,16
OR Logic "1" Threshold Voltage	$V_{OHA}\phi$	2	-1.065	– – – –	-0.980	– – – –	-0.910	– – – –	Vdc	– – – –	– – – –	4 5 6 7	– – – –	8	1,16
OR Logic "0" Threshold Voltage	$V_{OLA}\phi$	2	–	-1.630	–	-1.600	–	-1.555	Vdc	– – – –	– – – –	– – – –	4 5 6 7	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	–	1.8	–	1.7	–	1.9	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9			2	–	–		
	t_{4+2+}	2	–	1.6	–	1.5	–	1.7			2	–	–		
	t_{4-3+}	3	–	1.6	–	1.5	–	1.7			3	–	–		
Rise Time	t_{3+}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{3-}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to the input under test.

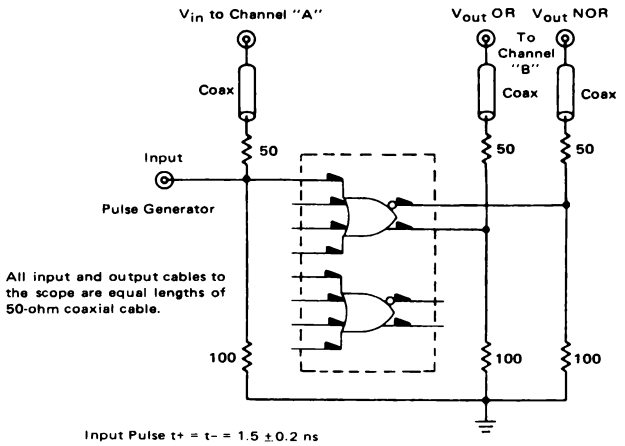
φ NOTES

The electrical specifications shown above apply to the MC1660 under the following conditions:

1. The package is housed in a suitable heat sink.†
   or
2. Air is blown transversely over the package. See general information section for more details.

†A suitable heat sink is an IERC LIC14A2U or equivalent.

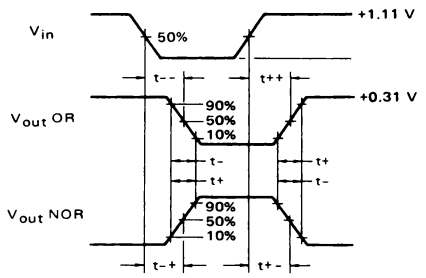
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input Pulse t+ = t- = 1.5 ±0.2 ns

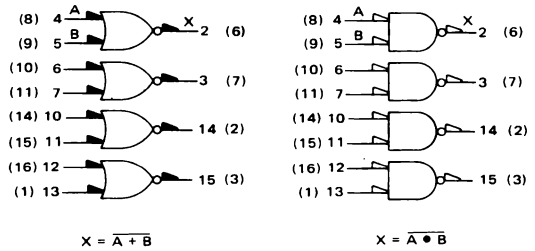
Unused outputs connected to a 50-ohm resistor to ground

PROPAGATION DELAY



QUAD 2-INPUT "NOR" GATE

MC1662



Four 2-input NOR or NAND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range (-30 to +85°C).

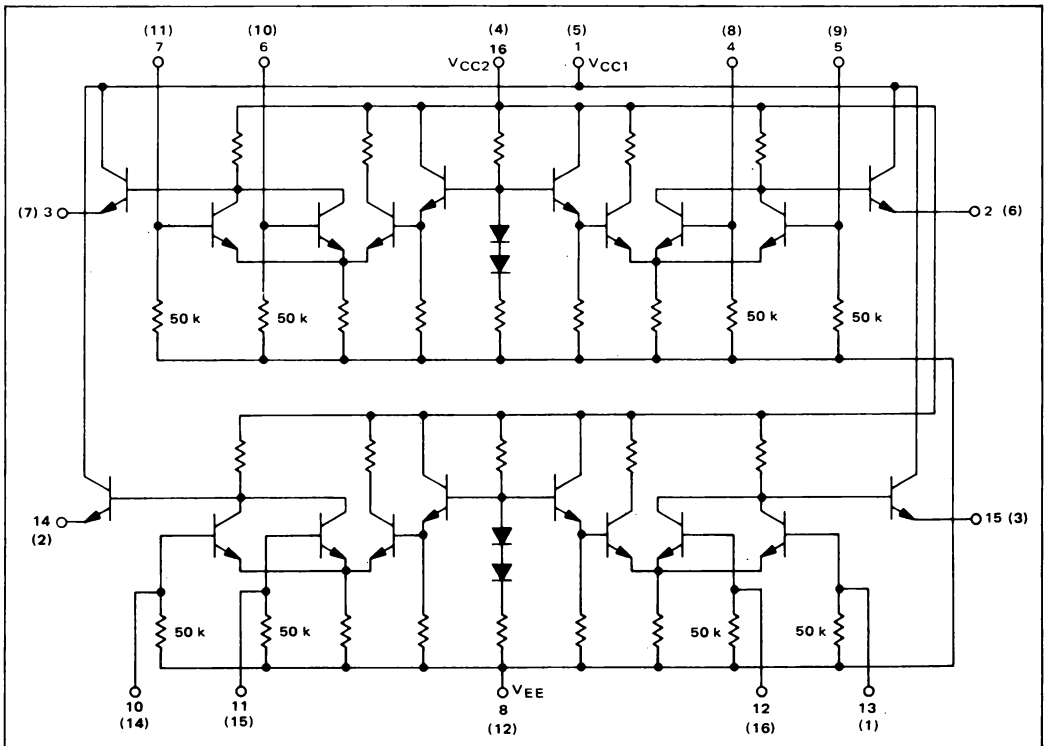
Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

Number at end of terminals denotes pin number of L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

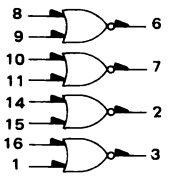
CIRCUIT SCHEMATIC

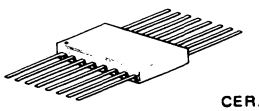


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





F SUFFIX
CERAMIC PACKAGE
CASE 650

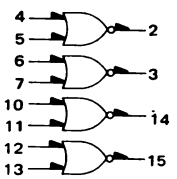
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

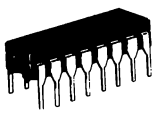
Characteristic	Symbol	Pin Under Test	MC1662F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	12	–	–	–	56	–	–	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	12	4,5
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	8	–	–	12	4,5
		6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	9	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	8	–	–	–	12	4,5
		6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	8	12	4,5
		6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	9	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	8	–	12	4,5
		6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	9	–	12	4,5
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{8-6+}	6	–	1.6	–	1.5	–	1.7	ns	8	6	–	–	12	4,5
	t_{8+6-}	6	–	1.8	–	1.7	–	1.9	ns	8	6	–	–	12	4,5
Rise Time	t_{6+}	6	–	2.2	–	2.1	–	2.3	ns	8	6	–	–	12	4,5
Fall Time	t_{6-}	6	–	2.2	–	2.1	–	2.3	ns	8	6	–	–	12	4,5

*Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





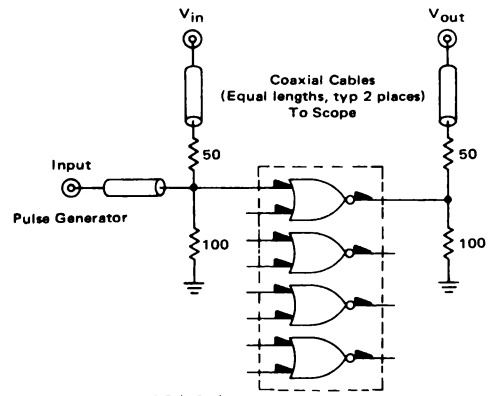
L SUFFIX
CERAMIC PACKAGE
CASE 620

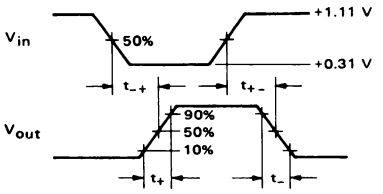
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1662L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	5	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	5	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	4	–	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	5	–	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	1.6	1.0	1.5	–	1.7	ns	4	2	–	–	8	1,16
	t_{4-2-}	2	–	1.8	1.1	1.7	–	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	–	2.2	1.4	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	–	2.2	1.2	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



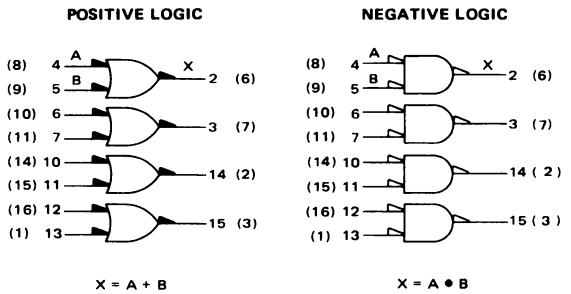


Input Pulse $t_+ = t_- = 1.5\ (\pm 0.2)$ ns

Unused outputs connected to a 50-ohm resistor to ground.

QUAD 2-INPUT "OR" GATE

MC1664



X = A + B X = A • B

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

Number at end of terminals denotes pin number of L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

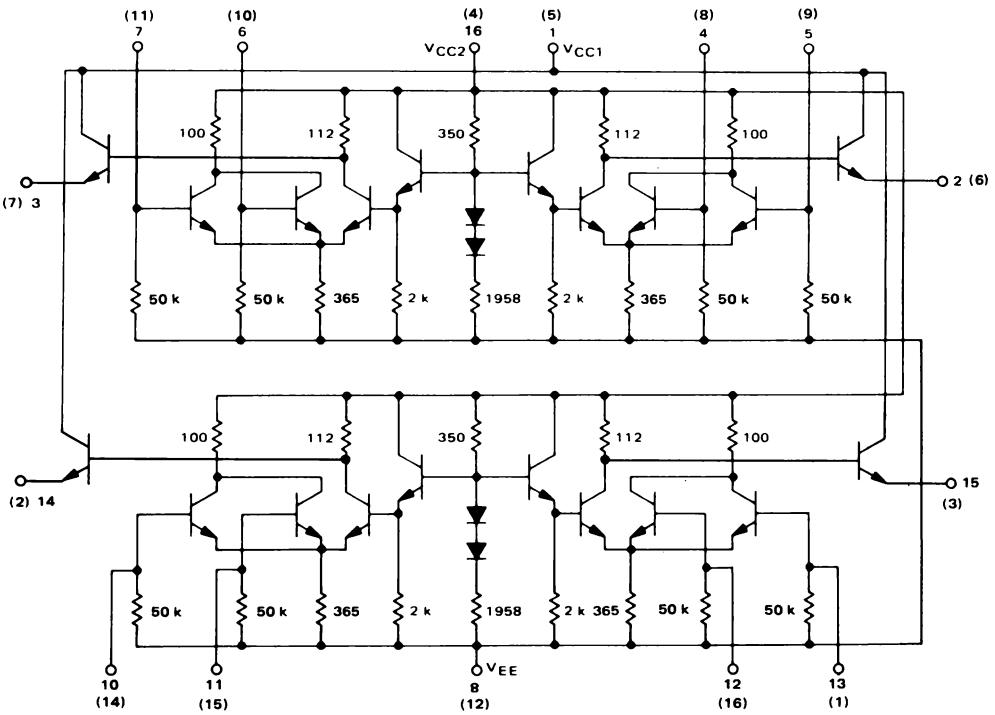
Four 2-input OR or AND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range -30 to +85°C.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

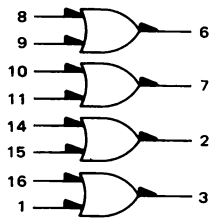
CIRCUIT SCHEMATIC

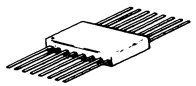


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





F SUFFIX
CERAMIC PACKAGE
CASE 650

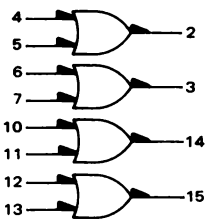
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

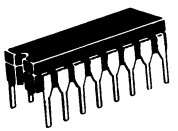
Characteristic	Symbol	Pin Under Test	MC1664F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–	56	–	–	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	12	4,5
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	8	–	–	–	12	4,5
		6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	8	–	–	12	4,5
		6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	9	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	8	–	12	4,5
		6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	9	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	8	12	4,5
		6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	9	12	4,5
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{8+6+}	6	–	1.6	–	1.5	–	1.7	ns	8	6	–	–	12	4,5
	t_{8-6-}	6	–	1.8	–	1.7	–	1.9	ns	8	6	–	–	12	4,5
Rise Time	t_{6+}	6	–	2.2	–	2.1	–	2.3	ns	8	6	–	–	12	4,5
Fall Time	t_{6-}	6	–	2.2	–	2.1	–	2.3	ns	8	6	–	–	12	4,5

*Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





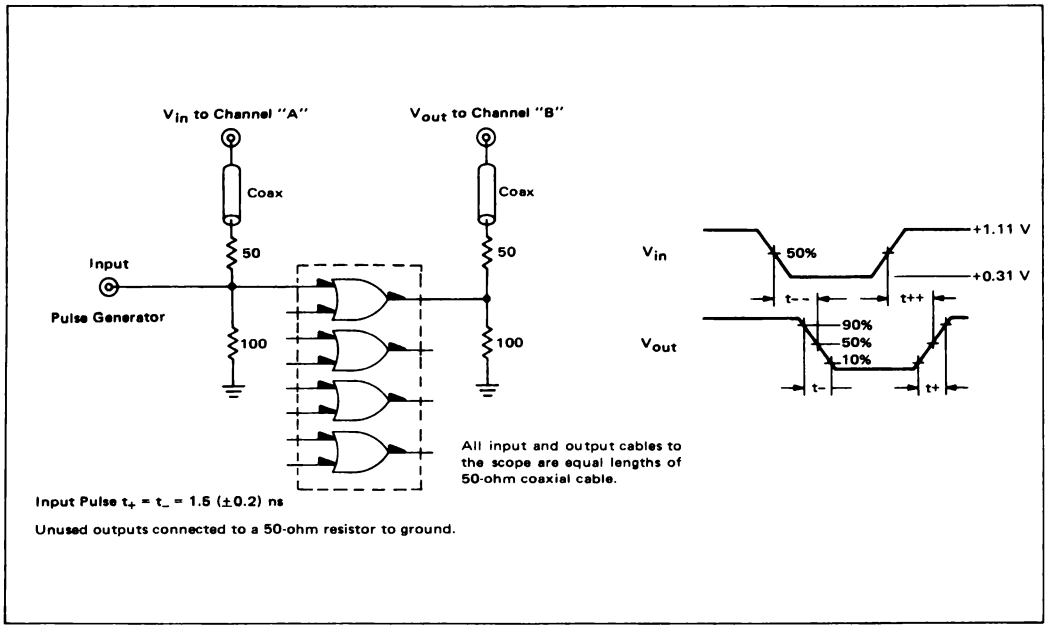
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1664L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	4	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	4	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	5	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	1.6	–	1.5	–	1.7	ns	4	2	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input Pulse $t_+ = t_- = 1.5\ (\pm 0.2)$ ns

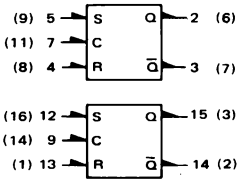
Unused outputs connected to a 50-ohm resistor to ground.

DUAL CLOCKED R-S FLIP-FLOP

MC1666

This device consists of two Set-Reset flip-flops in a single package which require a clock input to enable the set-reset inputs. Internal input pull-down resistors eliminate the need to return unused inputs to a negative voltage. The device is useful as a high-speed dual storage element.

POSITIVE LOGIC



t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No Load)

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

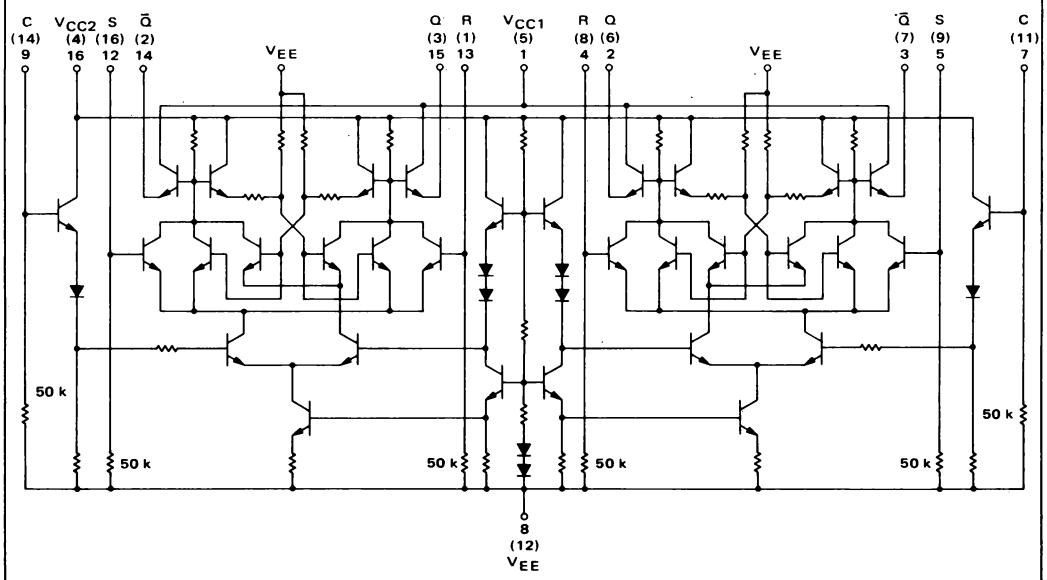
TRUTH TABLE

S	R	C	Q_{n+1}
ϕ	ϕ	0	Q_n
0	0	1	Q_n
1	0	1	1
0	1	1	0
1	1	1	N.D.

ϕ = Don't Care
N.D. = Not Defined

Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

CIRCUIT SCHEMATIC

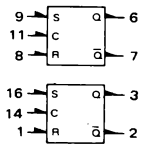


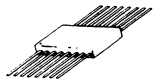
Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





F SUFFIX
CERAMIC PACKAGE
CASE 650

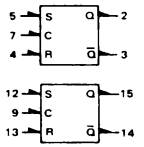
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

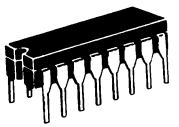
Characteristic	Symbol	Pin Under Test	MC1666F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85 Min	+85 Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E ①	12	--	--	--	55	--		mAdc	11,14	--	--	--	12	4,5
Input Current	I_{inH}	1	--	--	--	0.370	--	--	mAdc	1,14	--			12	4,5
		16	--	--	--	0.370	--	--	mAdc	14,16				12	4,5
		14	--	--	--	0.225	--	--	mAdc	14	--	--	--	12	4,5
	I_{inL}	16	--	--	0.5	--	--	--	µAdc		16			12	4,5
		1,14	--	--	0.5	--	--	--	µAdc		1,14			12	4,5
"Q" Logic "1" Output Voltage	V_{OH}	3 ②	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	--	1			12	4,5
		3 ③	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	14	--			12	4,5
"Q" Logic "0" Output Voltage	V_{OL}	3 ④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	--	16		--	12	4,5
		3 ⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	14	--			12	4,5
"Q̄" Logic "1" Output Voltage	V_{OH}	2 ④	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	--	16			12	4,5
		2 ⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	14	--			12	4,5
"Q̄" Logic "0" Output Voltage	V_{OL}	2 ②	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	--	1		--	12	4,5
		2 ③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	14	--	--	--	12	4,5
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	3 ⑥	-1.065		-0.980	--	-0.910		Vdc	--	--	16	1	12	4,5
		3 ⑦	-1.065	--	-0.980	--	-0.910	--	Vdc		1	14	--	12	4,5
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	3 ⑥	--	-1.630	--	-1.600	--	-1.555	Vdc			1	16	12	4,5
"Q̄" Logic "1" Output Threshold Voltage	V_{OHA}	2 ⑥	-1.065	--	-0.980	--	-0.910		Vdc	--	--	1	16	12	4,5
"Q̄" Logic "0" Output Threshold Voltage	V_{OLA}	2 ⑥	--	-1.630	--	-1.600		-1.555	Vdc	--	--	16	1	12	4,5
		2 ⑦	--	-1.630	--	-1.600		-1.555	Vdc	--	14	14	--	12	4,5
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Clock Input	t_{14+3+}	3	1.0	2.7	1.0	2.5	1.1	2.8	ns	14	3		--	12	4,5
	t_{14+3-}	3									3		--		
	t_{14+2-}	2									2				
	t_{14+2+}	2									2	--	--		
Set Input	t_{16+3+}	3	1.0	2.5	1.0	2.3	1.1	2.7	ns	16	3	--	--	12	4,5
	t_{16+2-}	2							ns	16	2			12	4,5
Reset Input	t_{1+2+}	3							ns	1	2		--	12	4,5
	t_{1+3-}	2							ns	1	3		--	12	4,5
Rise Time	t_+	2,3	0.8	2.8	0.8	2.5	0.9	2.9	ns	14	2,3		--	12	4,5
Fall Time	t_-	2,3	0.5	2.4	0.5	2.2	0.5	2.6	ns	14	2,3	--	--	12	4,5

○ Notes appear on page following Electrical Characteristics tables

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





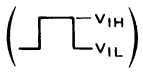
L SUFFIX
CERAMIC PACKAGE
CASE 620

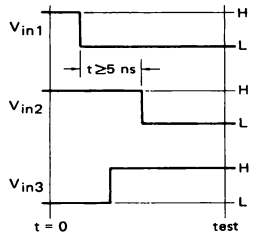
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1666L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85 Min	+85 Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E ①	8	–	–	–	55	–	–	mAdc	7,9	–	–	–	8	1,16
Input Current	I_{inH}	12	–	–	–	0.370	–	–	mAdc	9,12	–	–	–	8	1,16
		13	–	–	–	0.370	–	–	mAdc	9,13	–	–	–	8	1,16
		9	–	–	–	0.225	–	–	mAdc	9	–	–	–	8	1,16
	I_{inL}	12	–	–	0.500	–	–	–	µAdc	–	12	–	–	8	1,16
		9,13	–	–	0.500	–	–	–	µAdc	–	9,13	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15 ②	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	13	–	–	8	1,16
		15 ③	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Voltage	V_{OL}	15 ④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	12	–	–	8	1,16
		15 ⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"$\overline{Q}$" Logic "1" Output Voltage	V_{OH}	14 ④	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	12	–	–	8	1,16
		14 ⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"$\overline{Q}$" Logic "0" Output Voltage	V_{OL}	14 ②	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	13	–	–	8	1,16
		14 ③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15 ⑥	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	12	13	8	1,16
		15 ⑦	-1.065	–	-0.980	–	-0.910	–	Vdc	–	13	9	–	8	1,16
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15 ⑥	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	13	12	8	1,16
"$\overline{Q}$" Logic "1" Output Threshold Voltage	V_{OHA}	14 ⑥	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	13	12	8	1,16
"$\overline{Q}$" Logic "0" Output Threshold Voltage	V_{OLA}	14 ⑥	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	12	13	8	1,16
		14 ⑦	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	9	–	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Clock Input	t_{9+15+}	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15	–	–	8	1,16
	t_{9+15-}	15									15	–	–		
	t_{9+14-}	14									14	–	–		
	t_{9+14+}	14									14	–	–		
Set Input	t_{12+15+}	15	1.0	2.5	1.0	2.3	1.1	2.7	ns	12	15	–	–	8	1,16
	t_{12+14-}	14							ns	12	14	–	–	8	1,16
Reset Input	t_{13+14-}	14							ns	13	14	–	–	8	1,16
	t_{13+15+}	15							ns	13	15	–	–	8	1,16
Rise Time	t+	14,15	0.8	2.8	0.8	2.5	0.9	2.9	ns	9	14,15	–	–	8	1,16
Fall Time	t-	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15	–	–	8	1,16

○ Notes appear on page following Electrical Characteristics tables.

NOTES





① I_E is measured with no output pull-down resistors.

② Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to S (V_{IH} to V_{IL})

③ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to S (V_{IH} to V_{IL})

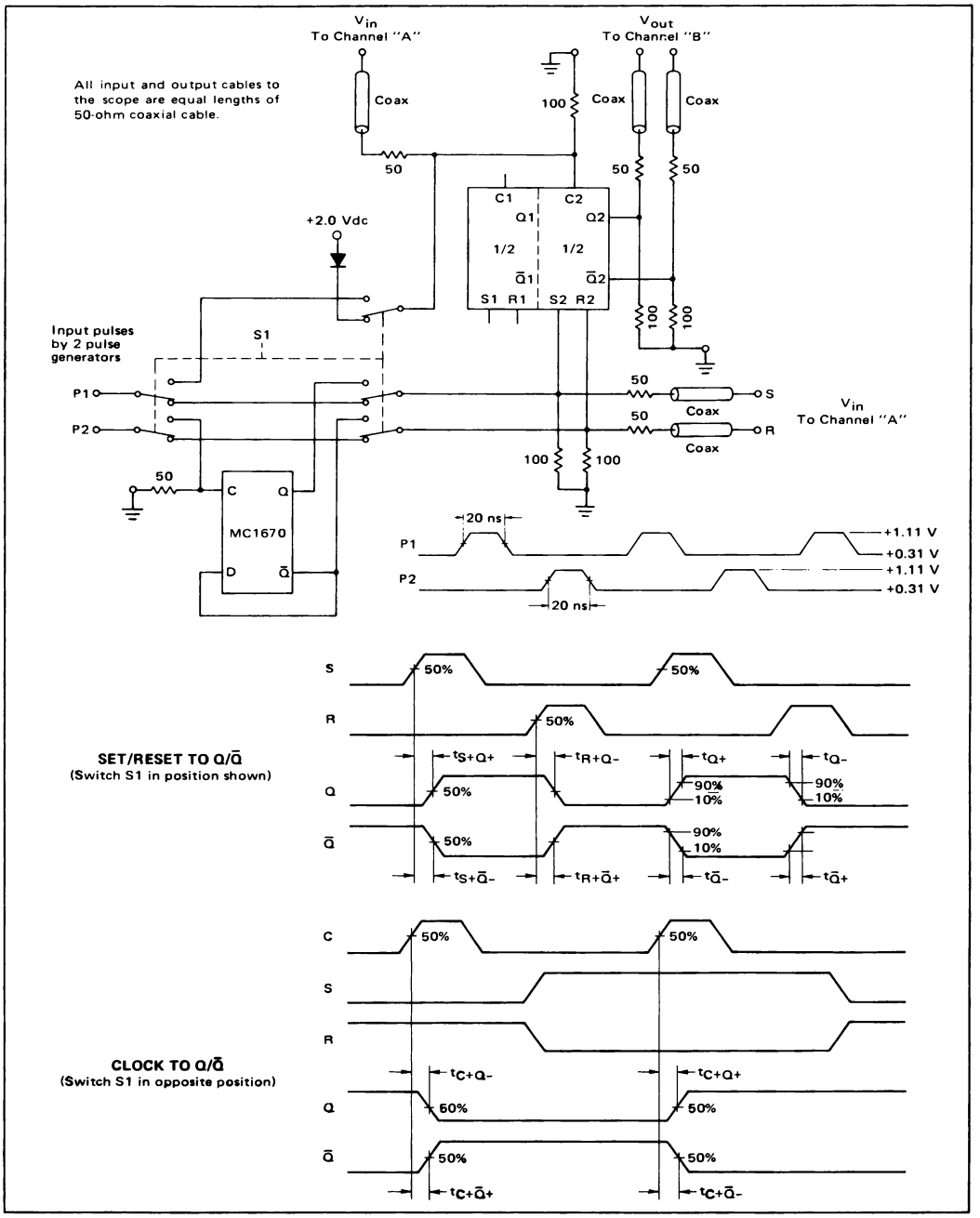
④ Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

⑤ Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

⑥ Apply V_{in3} to C (V_{IH} to V_{IL})

⑦ Apply V_{in3} to S (V_{IH} to V_{IL})

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

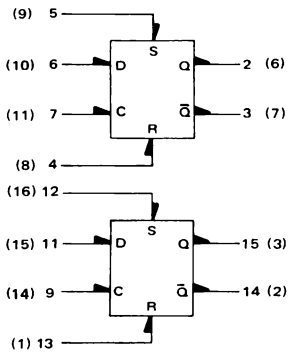


DUAL CLOCKED LATCH

MC1668

This device is a Dual Clocked Latch/R-S Flip-Flop. Whenever the Clock is low, the R-S inputs control the output state. Whenever the Clock is high, the output follows the data (D) input.

POSITIVE LOGIC



Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

TRUTH TABLE

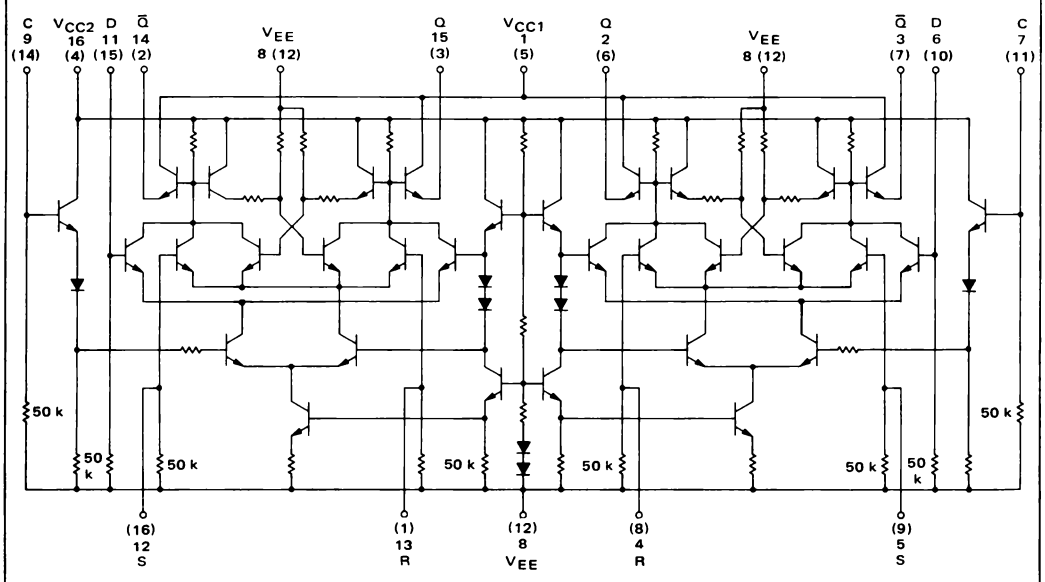
S	R	D	C	Q_{n+1}
0	0	ϕ	0	Q_n
1	0	ϕ	0	1
0	1	ϕ	0	0
1	1	ϕ	0	••
ϕ	ϕ	0	1	0
ϕ	ϕ	1	1	1

••Output state not defined ϕ = Don't Care

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No load)

CIRCUIT SCHEMATIC

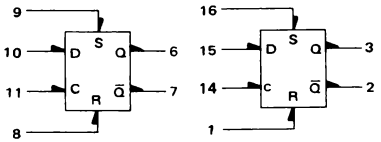


Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



F SUFFIX
CERAMIC PACKAGE
CASE 650

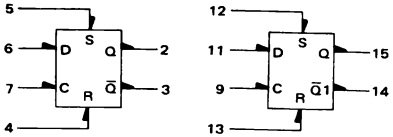
@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

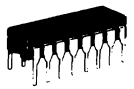
Characteristic	Symbol	Pin Under Test	MC1668F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12 ①	–	–	–	55	–	–	mAdc	11,14	–	–	–	12	4,5
Input Current	I_{in} H	1,15,16②	–	–	–	0.370	–	–	mAdc	1,15,16	–	–	–	12	4,5
		13	–	–	–	0.225	–	–	mAdc	14	–	–	–	12	4,5
	I_{in} L	1,15,16②	–	–	0.500	–	–	–	μAdc	–	1,15,16	–	–	12	4,5
		13	–	–	0.500	–	–	–	μAdc	–	14	–	–	12	4,5
"Q" Logic "1" Output Voltage	V_{OH}	3③	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc	–	1	–	–	12	4,5
		3④	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc	14	–	–	–	12	4,5
"Q" Logic "0" Output Logic	V_{OL}	3⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	16	–	–	12	4,5
		3⑥	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	14	–	–	–	12	4,5
"Q̄" Logic "1" Output Voltage	V_{OH}	2⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	16	–	–	12	4,5
		2⑥	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	14	–	–	–	12	4,5
"Q̄" Logic "0" Output Voltage	V_{OL}	2③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	1	–	–	12	4,5
		2④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	14	–	–	–	12	4,5
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	3	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	16	1	12	4,5
		3⑦	↓	–	↓	–	↓	–	↓	–	–	15	–	↓	↓
		3⑤	–	–	–	–	–	–		15	–	14	–		
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	1	16	12	4,5
		3⑥	–	↓	–	↓	–	↓	↓	–	–	–	15	↓	↓
		3③	–		–		–			–	15	14	–		
"Q̄" Logic "1" Output Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	1	16	12	4,5
		2⑥	↓	–	↓	–	↓	–	↓	–	–	–	15	↓	↓
		2③		–		–		–		–	15	14	–		
"Q̄" Logic "0" Output Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	16	1	12	4,5
		2⑦	–	↓	–	↓	–	↓	↓	–	–	15	–	↓	↓
		2⑤	–		–		–			–	–	14	–		
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Clock Input	t_{13+3+}	3	1.0	2.7	1.0	2.5	1.1	2.8	ns	14	3	–	–	12	4,5
	t_{13+3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	3	–	–	↓	↓
	t_{13+2-}	2									2	–	–		
	t_{13+2+}	2									2	–	–		
Rise Time	t_+	2,3	0.8	2.8	0.9	2.5	0.9	2.9	ns	14	2,3	–	–	12	4,5
Fall Time	t_-	2,3	0.5	2.4	0.5	2.2	0.5	2.6	ns	14	2,3	–	–	12	4,5
Set Input	t_{16+3+}	3	1.0	2.5	1.1	2.3	1.1	2.7	ns	16	3	–	–	12	4,5
	t_{16+2-}	2	1.0	2.5	1.1	2.3	1.1	2.7	ns	16	2	–	–	12	4,5
Reset Input	t_{1+2+}	2	1.0	2.5	1.1	2.3	1.1	2.7	ns	1	2	–	–	12	4,5
	t_{1+3-}	3	1.0	2.5	1.1	2.3	1.1	2.7	ns	1	3	–	–	12	4,5

○Notes appear on page following Electrical Characteristics tables.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

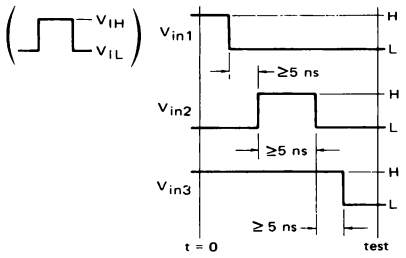
Characteristic	Symbol	Pin Under Test	MC1668L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E (Hi-Z) 1	8	–	–	–	55	–	–	mAdc	7,9	–	–	–	8	1,16
Input Current	$I_{in\ H}$	11,12,13②	–	–	–	0.370	–	–	mAdc	11,12,13	–	–	–	8	1,16
		9	–	–	–	0.225	–	–	mAdc	9	–	–	–	8	1,16
	$I_{in\ L}$	11,12,13②	–	–	0.500	–	–	–	μAdc	–	11,12,13	–	–	8	1,16
		9	–	–	0.500	–	–	–	μAdc	–	9	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15③	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc	–	13	–	–	8	1,16
		15④	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Logic	V_{OL}	15⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	12	–	–	8	1,16
		15⑥	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"$\bar{Q}$" Logic "1" Output Voltage	V_{OH}	14⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	12	–	–	8	1,16
		14⑥	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"$\bar{Q}$" Logic "0" Output Voltage	V_{OL}	14③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	13	–	–	8	1,16
		14④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	12	13	8	1,16
		15⑦	↓	–	↓	–	↓	–	↓	–	–	11	–	↓	↓
		15⑤		–		–				11		9	–		
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	13	12	8	1,16
		15⑥	–	↓	–	↓	–	↓	↓	–	–	–	11	↓	↓
		15③	–		–		–				11	9	–		
"$\bar{Q}$" Logic "1" Output Threshold Voltage	V_{OLA}	14	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	13	12	8	1,16
		14⑥	↓	–		–	↓	–	↓	–	–	–	11	↓	↓
		14③		–		–		–		–	11	9	–		
"$\bar{Q}$" Logic "0" Output Threshold Voltage	V_{OLA}	14	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	12	13	8	1,16
		14⑦	–	↓	–	↓	–	↓	↓	–	–	11	–	↓	↓
		14⑤	–		–		–			–	–	9	–		
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Clock Input	t_{g+15+}	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15	–	–	8	1,16
	t_{g+15-}	15	↓	↓	↓	↓	↓	↓	↓	↓	15	–	–	↓	↓
	t_{g+14-}	14									14	–	–		
	t_{g+14+}	14									14	–	–		
Rise Time	t_+	14,15	0.8	2.8	0.9	2.5	0.9	2.9	ns	9	14,15	–	–	8	1,16
Fall Time	t_-	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15	–	–	8	1,16
Set Input	t_{12+15+}	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	15	–	–	8	1,16
	t_{12+14-}	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	14	–	–	8	1,16
Reset Input	t_{13+14+}	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	14	–	–	8	1,16
	t_{13+15-}	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	15	–	–	8	1,16

○Notes appear on page following Electrical Characteristics tables.

NOTES

① I_E is measured with no output pulldown resistors.

② Test voltage applied to pin under test.



③ Apply V_{in1} to S (V_{IH} to V_{IL}).

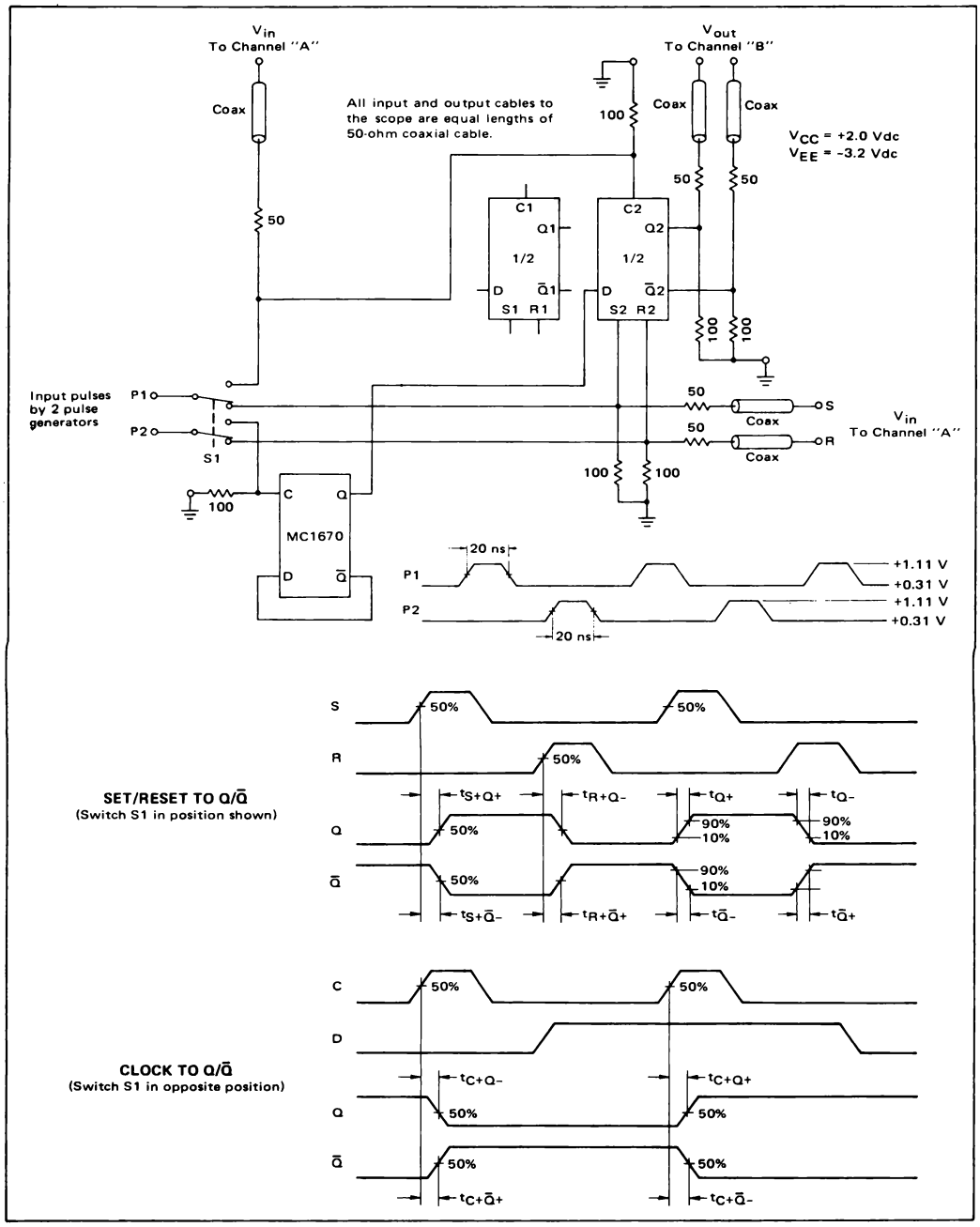
④ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})
V_{in3} to D (V_{IH} to V_{IL})

⑤ Apply V_{in1} to R (V_{IH} to V_{IL})

⑥ Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})

⑦ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS @ 25°C



The MC1670 is a Type D Master-Slave Flip-Flop designed for use in high speed digital applications. Master slave construction renders the MC1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

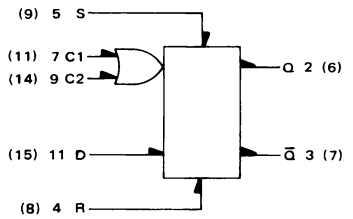
When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

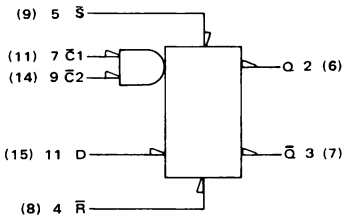
Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



NEGATIVE LOGIC



Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

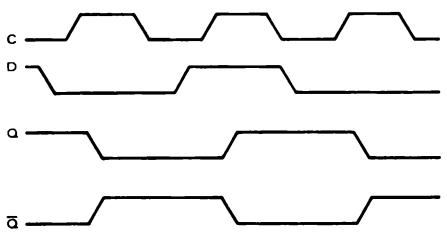
Power Dissipation = 220 mW typical (No Load)
f_{tog} = 350 MHz typ

TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↗	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↗	H
L	L	H	H	Q_n

ϕ = Don't Care
ND = Not Defined
C = C1 + C2

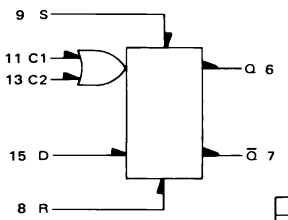
TIMING DIAGRAM

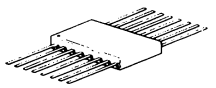


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

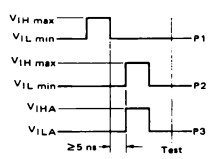




F SUFFIX
CERAMIC PACKAGE
CASE 650

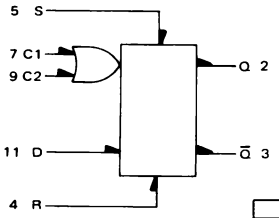
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

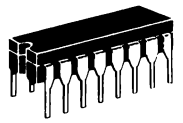
Characteristic	Symbol	Pin Under Test	MC1670F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	12	–	–	–	48	–	–	mAdc	–	–	–	–	12	–	–	–	4,5
Input Current	$I_{in\ H}$	8	–	–	–	550	–	–	μAdc	8				12	–	–	–	4,5
		9	–	–	–	550		–		9			–		–		–	
		14	–	–	–	250	–			14					–		–	
		11	–	–		250	–			11						–	–	
		15	–	–	–	270	–	–		15	–	–			–	–	–	
	$I_{in\ L}$	8	–	–	0.5	–	–	–	μAdc	14	8	–	–	12	–	–	–	4,5
		9	–	–		–	–	–		14	9	–	–		–	–	–	
		14	–			–	–			11	14		–		–	–	–	
		11	–	–		–	–	–		14	11	–	–		–		–	
		15	–	–		–	–	–		14	15	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	8,11,15	–	–	12	14	9	–	4,5
		7								15	9,14	–			11	8	–	
		6								15	9,11		–		8	14		
		7									8,14,15	–	–		9	11		
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	15	9,11	–	–	12	14	8	–	4,5
		7									8,14,15	–	–		11	9		
		6								–	8,11,15	–	–		9	14	–	
		7								15	9,14	–	–		8	11	–	
Logic "1" Threshold Voltage	V_{OHA}	6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	8,11,15	–	–	12	14	–	9	4,5
		7		–		–		–		15	9,14	–			11	–	8	
		6		–		–		–		15	9,11	–	–		8	–	14	
		7		–		–		–		–	8,14,15	–	–		9	–	11	
		6		–		–		–		–	9,11	15	–		8	14		
		7		–		–		–		–	8,14	–	15		9	11	–	
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.630	–	-1.600	–	-1.555	Vdc	15	9,11	–	–	12	14	–	8	4,5
		7	–		–		–				8,14,15				11	–	9	
		6	–		–					–	8,11,15	–			9	–	14	
		7	–		–					15	9,14	–	–		8		11	
		6	–		–		–			–	8,11		15		9	14	–	
		7	–		–		–			–	9,14	15	–		8	11	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						-3.2 Vdc				+2.0 Vdc
Clock to Output Delay	t_{11+6+}	14,6	1.0	2.7	1.1	2.5	1.1	2.9	ns					12	–	–	–	4,5
(See Figure 1)	t_{11-6-}	14,6									–	–	–		–	–	–	
	t_{11+7-}	14,7									–		–		–	–	–	
	t_{11-7+}	14,7								–	–	–	–		–	–	–	
Set to Output Delay	t_{9+6+}	9,6								–		–	–		–	–	–	
(See Figure 2)	t_{9+6-}	9,7								–			–		–	–	–	
Reset to Output Delay	t_{8+6-}	8,6									–		–			–	–	
(See Figure 2)	t_{8+7+}	8,7								–	–		–		–	–		
Output Rise Time	t_{6+7+}	6,7	0.9	2.7	1.0	2.5	1.0	2.9		–	–	–	–		–	–	–	
Fall Time (See Figure 2)	t_{6-7-}	6,7	0.5	2.1	0.6	1.9	0.6	2.3		–	–	–	–		–	–	–	
Set Up Time	$t_{s"1"}$	6	–	–	–	0.4	–	–		–	6	–	–		–	–	–	
(See Figure 3)	$t_{s"0"}$	6	–	–	–	0.5	–	–		–	6		–		–	–		
Hold Time	$t_{H"1"}$	6	–	–	–	0.3	–	–		–	6	–	–			–		
(See Figure 3)	$t_{H"0"}$	6	–	–	–	0.5	–	–		–	6	–	–			–	–	
Toggle Frequency (See Figure 4)	f_{Tog}	6	270	–	300	–	270	–	MHz	–	–	–	–		–		–	–



ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.005	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1670L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	8	-		-	48	-	--	mAdc	7,9	--	-	-	8	-	-	-	1,16
Input Current	$I_{in\ H}$	4		-		550	-	--	μAdc	4	-	-	--	8	--	-	-	1,16
		5		-		550		-		5		--	-				--	
		9				250				9								
		7	-			250				7					--		-	
		11	-			270				11	--		-			-		
	$I_{in\ L}$	4			0.5				μAdc	9	4	-		8			-	1,16
		5								9	5				-			
		9					-			7	9					-		
		7					--			9	7		-					
		11	-	--			-			9	11	-	--			-		
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	-	4,7,11	-		8	9	5	--	1,16
		3								11	5,9				7	4	-	
		2								11	5,7				4	9		
		3									4,9,11	-	-		5	7	-	
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	11	5,7	-	-	8	9	4		1,16
		3									4,9,11		-		7	5		
		2									4,7,11				5	9		
		3								11	5,9	-	-		4	7	-	
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065		-0.980		-0.910		Vdc	--	4,7,11	-	--	8	9	-	5	1,16
		3								11	5,9				7		4	
		2								11	5,7				4		9	
		3									4,9,11	-			5		7	
		2						-			5,7	11	--		4	9		
		3		-				-		-	4,9		11		5	7	-	
Logic "0" Threshold Voltage	V_{OLA}	2		-1.630		-1.600		-1.555	Vdc	11	5,7		-	8	9		4	1,16
		3									4,9,11				7	--	5	
		2								-	4,7,11				5		9	
		3								11	5,9				4		7	
		2								-	4,7		11		5	9		
		3								-	5,9	11	-		4	7	-	
Switching Parameters			Min	Max	Min	Max	Min	Max						-3.2 Vdc				+2.0 Vdc
Clock to Output Delay	t_{7+2+}	9,2	1.0	2.7	1.1	2.5	1.1	2.9	ns					8		-	-	1,16
(See Figure 1)	t_{7-2-}	9,2																
	t_{7+3-}	9,3											-		-			
	t_{7-3+}	9,3											-					
Set to Output Delay	t_{5+2+}	5,2										-	-		-		-	
(See Figure 2)	t_{5+3-}	5,3											-		-		--	
Reset to Output Delay	t_{4+2-}	4,2									-		-			-	-	
(See Figure 2)	t_{4+3+}	4,3									-		-		--	-	-	
Output Rise Time	$t_{2+,3+}$	2,3	0.9	2.7	1.0	2.5	1.0	2.9				-			-	-	-	
Fall Time (See Figure 2)	$t_{2-,3-}$	2,3	0.5	2.1	0.6	1.9	0.6	2.3		--		-			-	--	-	
Set Up Time	t_{S}"1"	2				0.4		-			6		-		-	-	-	
(See Figure 3)	t_{S}"0"	2				0.5		-			6		-		-	-	-	
Hold Time	t_{H}"1"	2				0.3		-		-	6	-	-		-		-	
(See Figure 3)	t_{H}"0"	2				0.5					6	-	-			-	-	
Toggle Frequency (See Figure 4)	f_{Tog}	2	270		300	-	270	-	MHz	-	-				-	-	-	-

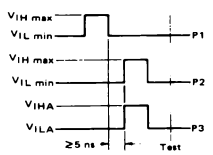


FIGURE 1 – PROPAGATION DELAY TEST CIRCUIT

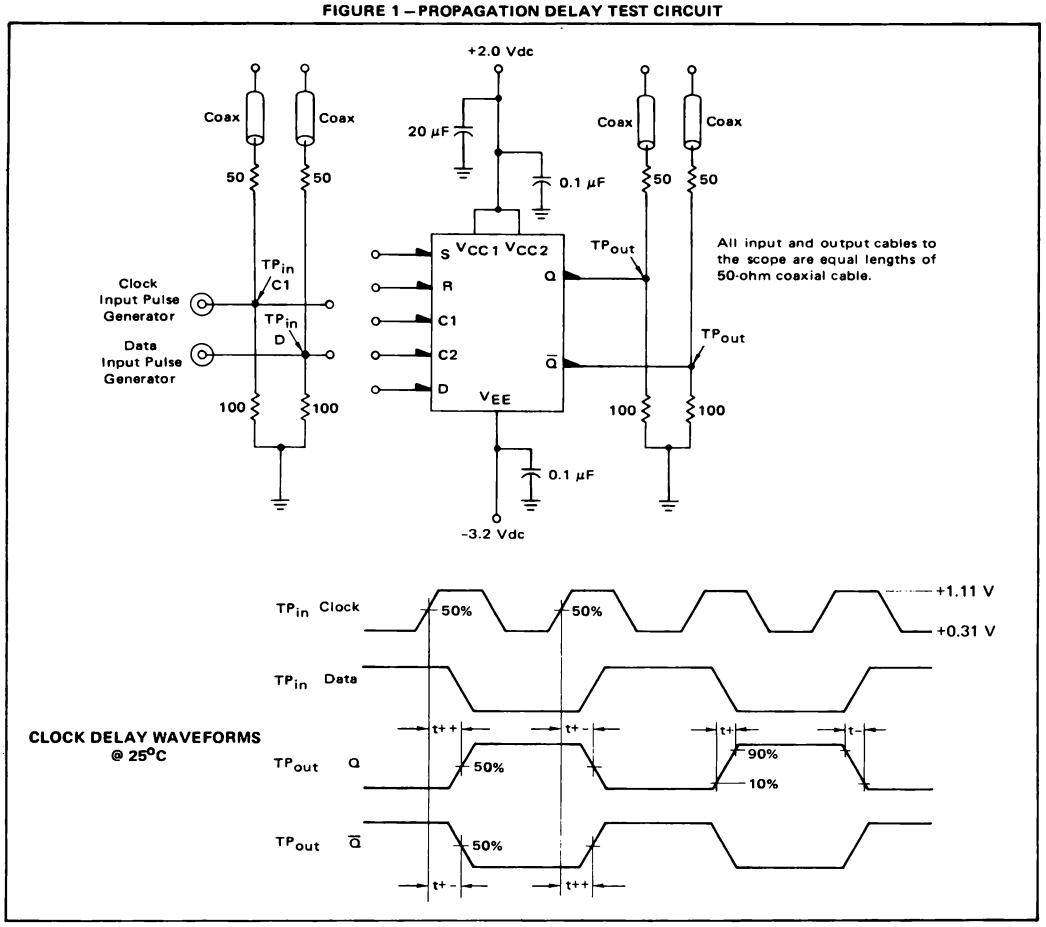


FIGURE 2 – SET-RESET DELAY WAVEFORMS @ 25°C

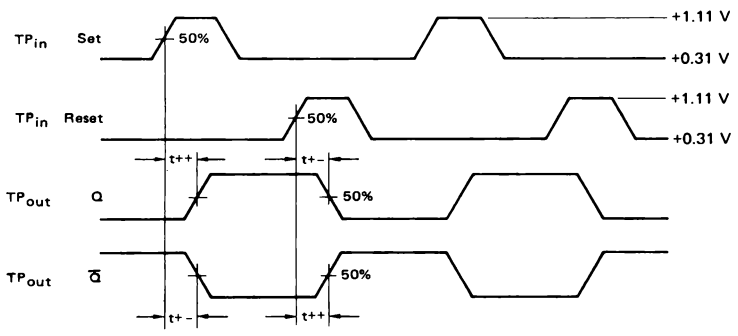
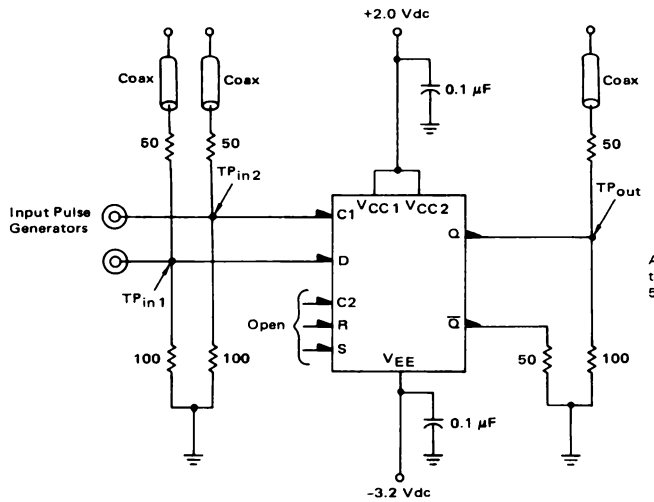
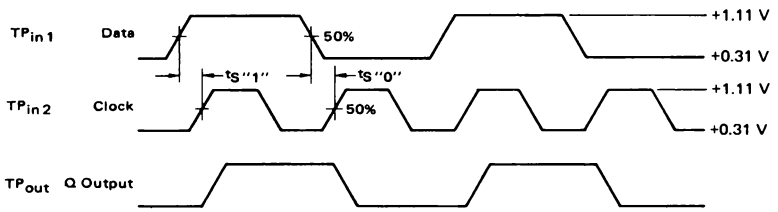


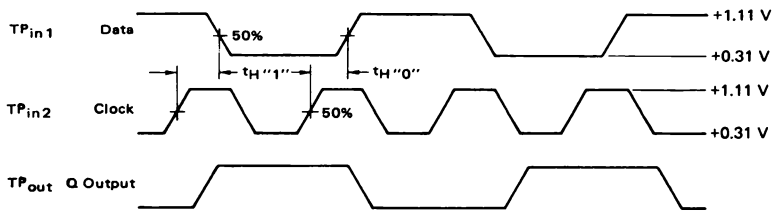
FIGURE 3 – SET UP AND HOLD TIME TEST CIRCUIT



SET UP TIME WAVEFORMS @ 25°C



HOLD TIME WAVEFORMS @ 25°C



Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data (D) input.

FIGURE 4 – TOGGLE FREQUENCY TEST CIRCUIT

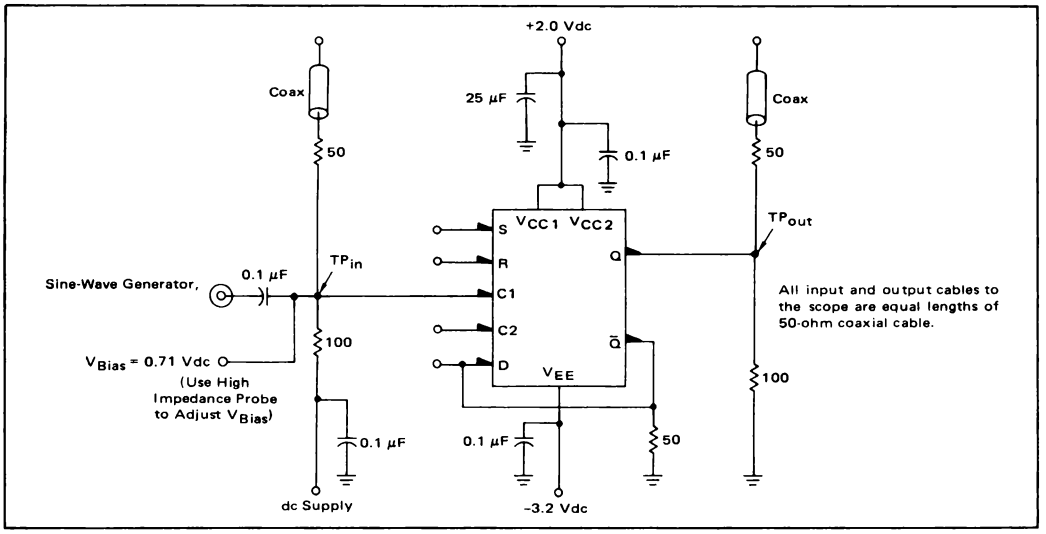


FIGURE 5 – TOGGLE FREQUENCY WAVEFORMS

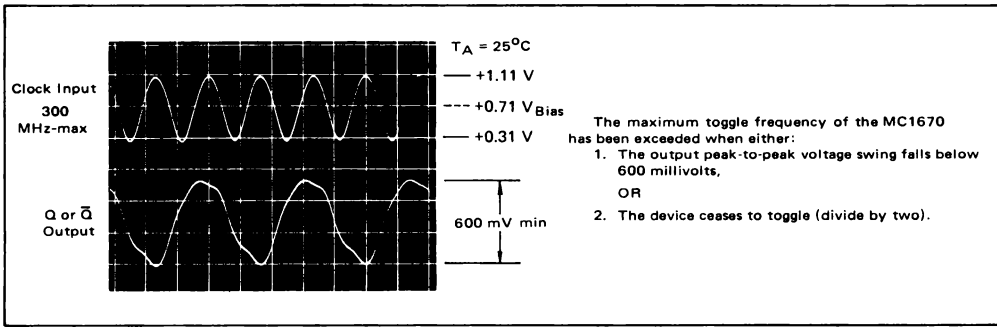


FIGURE 6 – MAXIMUM TOGGLE FREQUENCY (TYPICAL)

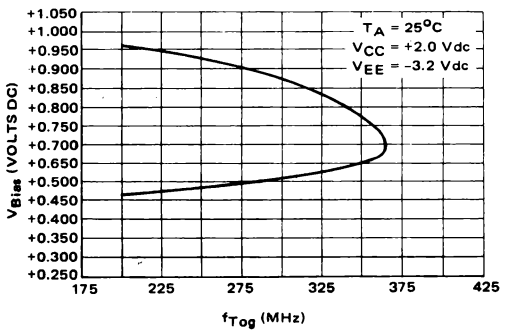
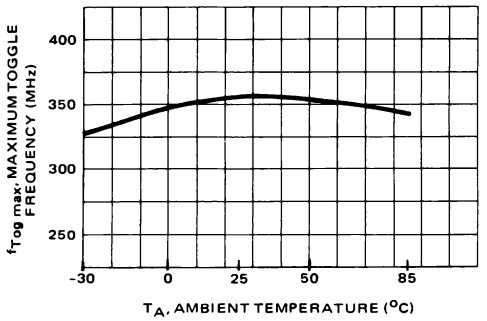


Figure 6 illustrates the variation in toggle frequency with the dc offset voltage (V_{Bias}) of the input clock signal. V_{Bias} is defined by the test circuit in Figure 4, and waveform Figure 5.

Figures 8 and 9 illustrate minimum clock pulse width recommended for reliable operation of the MC1670.

FIGURE 7 – TYPICAL MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE



Temperature	-30°C	+25°C	+85°C
V_{Bias}	+0.660 Vdc	+0.710 Vdc	+0.765 Vdc

FIGURE 8 – MINIMUM "DOWN TIME" TO CLOCK OUTPUT LOAD = 50 Ω

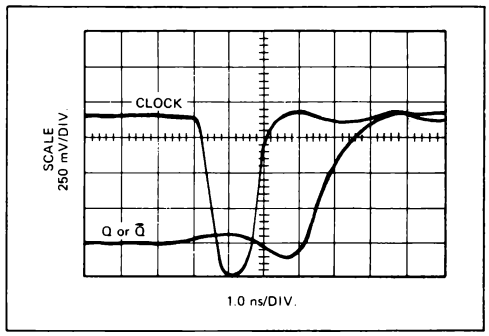
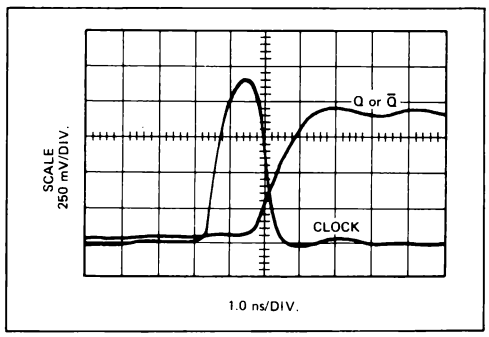


FIGURE 9 – MINIMUM "UP TIME" TO CLOCK OUTPUT LOAD = 50 Ω



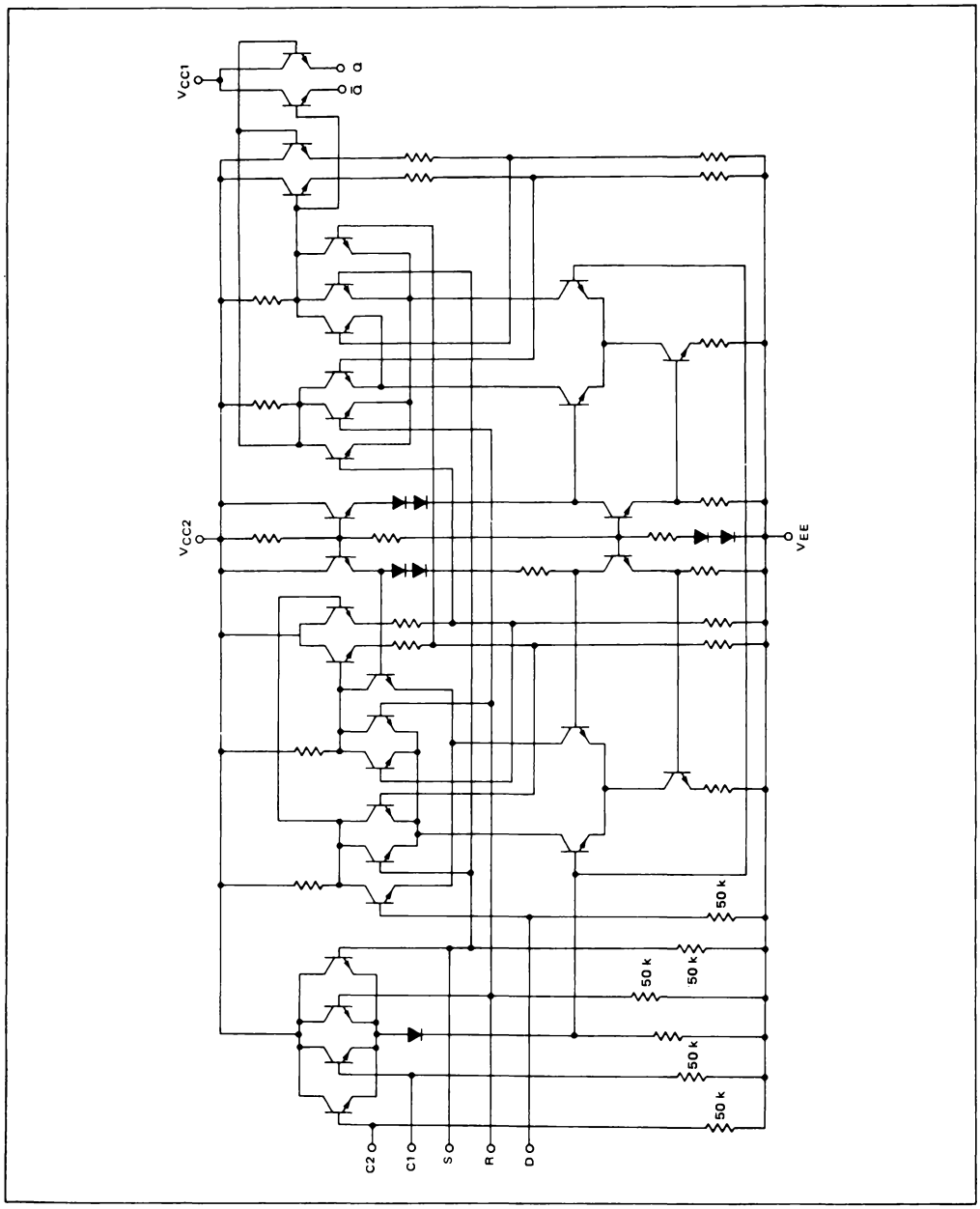


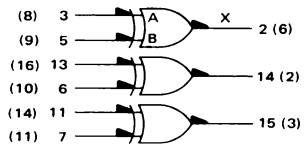
FIGURE 10 – MC1670 CIRCUIT SCHEMATIC

TRIPLE 2-INPUT
EXCLUSIVE-OR GATE

MC1672

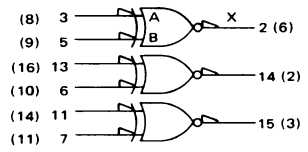
This three gate array is designed to provide the positive logic Exclusive-OR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (-30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



$X = A \bullet \overline{B} + \overline{A} \bullet B$

NEGATIVE LOGIC



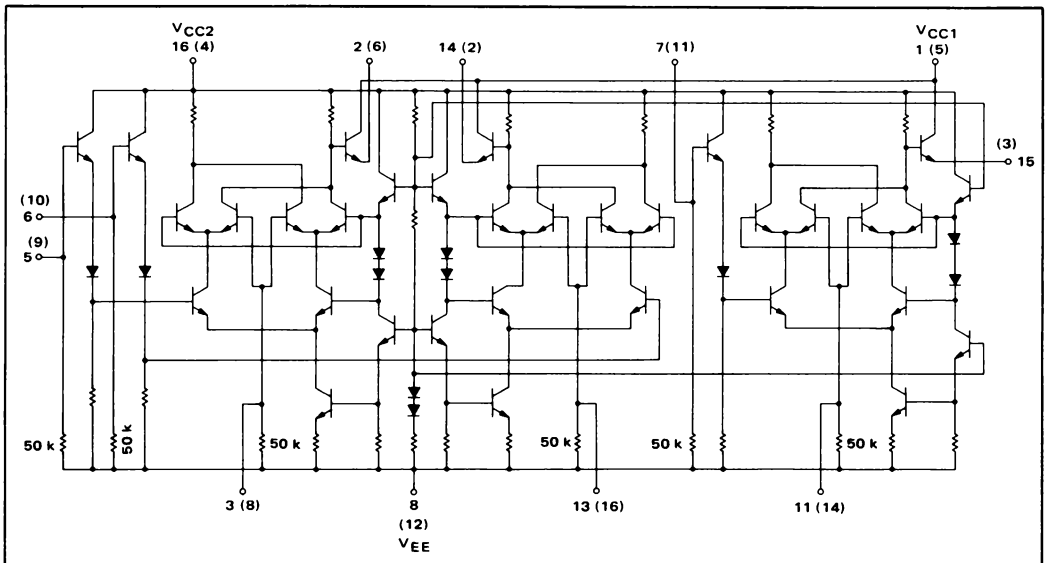
$X = A \bullet B + \overline{A} \bullet \overline{B}$

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = -25 mAdc max

Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

CIRCUIT SCHEMATIC

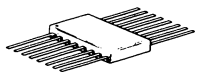


Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

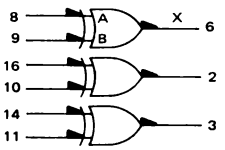
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



F SUFFIX
CERAMIC PACKAGE
CASE 650



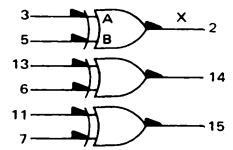
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

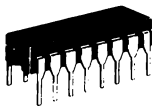
Characteristic	Symbol	Pin Under Test	MC1672F Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	12	4,5
Input Current	I_{inH}	8,14,16	–	–	–	350	–	–	μAdc	*	–	–	–	12	4,5
	0.75 I_{inH}	9,10,11	–	–	–	270	–	–	μAdc	*	–	–	–	12	4,5
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	8	9	–	–	12	4,5
		6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	8	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	8,9	–	–	–	12	4,5
		6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	8,9	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	8	9	12	4,5
		6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	9	8	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	8,9	–	12	4,5
		6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	8,9	12	4,5
Switching Times (50 Ω Load)												Pulse In	Pulse Out		
Propagation Delay	t_{8+6+}	6	–	2.0	–	1.8	–	2.3	ns	–	–	8	6	12	4,5
	t_{8-6+}		–	2.0	–	1.8	–	2.3		–	–				
	t_{8+6-}		–	2.1	–	1.9	–	2.4		–	–				
	t_{8-6-}		–	2.1	–	1.9	–	2.4		–	–				
	t_{9+6+}		–	2.5	–	2.3	–	2.8		–	–	9			
	t_{9-6+}		–		–		–			–	–				
	t_{9+6-}		–		–		–			–	–				
	t_{9-6-}		–		–		–			–	–				
Rise Time	t_{6+}	6	–	2.7	–	2.5	–	2.9	ns	–	–	8	6	12	4,5
Fall Time	t_{6-}	6	–	2.4	–	2.2	–	2.6	ns	–	–	8	6	12	4,5

*Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





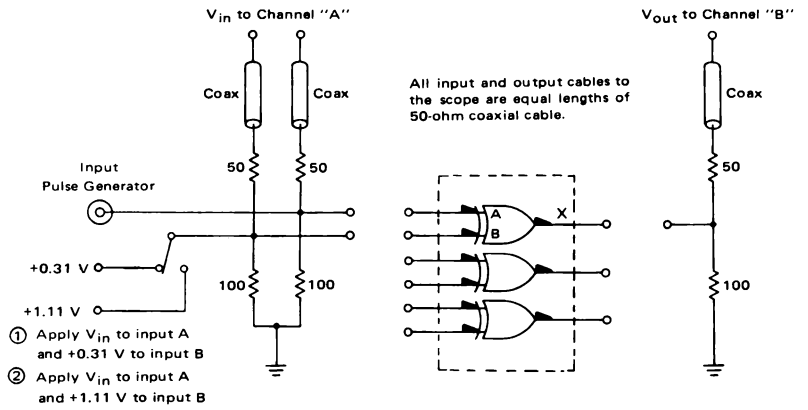
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1672L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	--	--		55	--	--	mAdc	All Inputs	--	--	--	8	1,16
Input Current	$I_{in\ H}$	3,11,13	--	--	--	350	--	--	µAdc	*	--	--	--	8	1,16
	0.75 $I_{in\ H}$	5,6,7	--	--	--	270	--	--	µAdc	*	--	--	--	8	1,16
	$I_{in\ L}$	*	--	--	0.5	--	--	--	µAdc	--	*	--	--	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	3	5	--	--	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5	3	--	--	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	3,5	--	--	--	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	--	3,5	--	--	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	--	-0.980	--	-0.910	--	Vdc	--	--	3	5	8	1,16
		2	-1.065	--	-0.980	--	-0.910	--	Vdc	--	--	5	3	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	--	-1.630	--	-1.600	--	-1.555	Vdc	--	--	3,5	--	8	1,16
		2	--	-1.630	--	-1.600	--	-1.555	Vdc	--	--	--	3,5	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max				Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	--	2.0	--	1.8	--	2.3	ns	--	--	3	2	8	1,16
	t_{3-2+}	2	--	2.0	--	1.8	--	2.3		--	--				
	t_{3+2-}	2	--	2.1	--	1.9	--	2.4		--	--				
	t_{3-2-}	2	--	2.1	--	1.9	--	2.4		--	--				
	t_{5+2+}	2	--	2.5	--	2.3	--	2.8		--	--	5			
	t_{5-2+}	2	--		--		--			--	--				
	t_{5+2-}	2	--		--		--			--	--				
	t_{5-2-}	2	--		--		--			--	--				
Rise Time	t_{2+}	2	--	2.7	--	2.5	--	2.9	ns	--	--	3	2	8	1,16
Fall Time	t_{2-}	2	--	2.4	--	2.2	--	2.6	ns	--	--	3	2	8	1,16

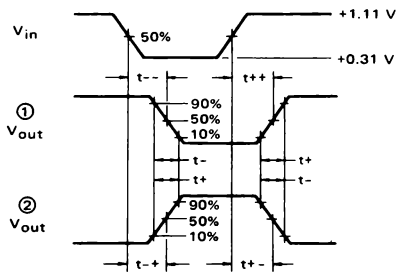
*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Unused outputs connected to a 50-ohm resistor to ground.

PROPAGATION DELAY

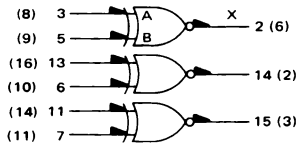


TRIPLE 2-INPUT
EXCLUSIVE-NOR GATE

MC1674

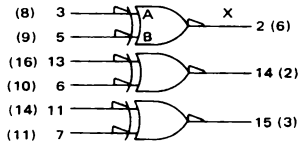
This three gate array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (-30° to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



$X = A \bullet B + \bar{A} \bullet \bar{B}$

NEGATIVE LOGIC

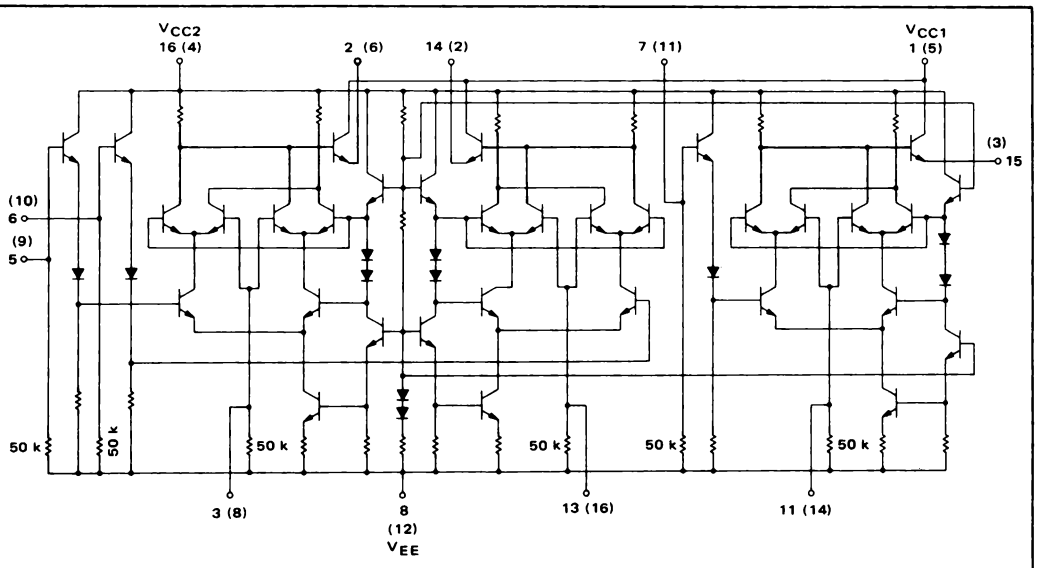


$X = \bar{A} \bullet B + A \bullet \bar{B}$

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = -25 mAdc max

Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

CIRCUIT SCHEMATIC

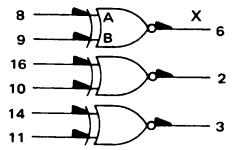


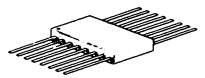
Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





F SUFFIX
CERAMIC PACKAGE
CASE 650

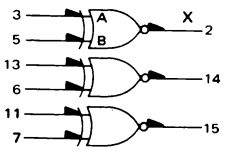
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1674F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	12	4,5
Input Current	I_{inH}	8,14,16	–	–	–	350	–	–	μAdc	*	–	–	–	12	4,5
	0.75 I_{inH}	9,10,11	–	–	–	270	–	–	μAdc	*	–	–	–	12	4,5
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	8,9	–	–	–	12	4,5
		6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	8,9	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	8	9	–	–	12	4,5
		6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	8	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	8,9	–	12	4,5
		6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	8,9	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	8	9	12	4,5
		6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	9	8	12	4,5
Switching Times (50 Ω Load)												Pulse In	Pulse Out		
Propagation Delay	t_{8+6+}	6	–	2.0	–	1.8	–	2.3	ns	–	–	8	6	12	4,5
	t_{8-6+}		–	2.0	–	1.8	–	2.3		–	–				
	t_{8+6-}		–	2.1	–	1.9	–	2.4		–	–				
	t_{8-6-}		–	2.1	–	1.9	–	2.4		–	–				
	t_{9+6+}		–	2.5	–	2.3	–	2.8		–	–	9			
	t_{9-6+}		–		–		–			–	–				
	t_{9+6-}		–		–		–			–	–				
	t_{9-6-}		–		–		–			–	–				
Rise Time	t_{6+}	6	–	2.7	–	2.5	–	2.9	ns	–	–	8	6	12	4,5
Fall Time	t_{6-}	6	–	2.4	–	2.2	–	2.6	ns	–	–	8	6	12	4,5

*Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



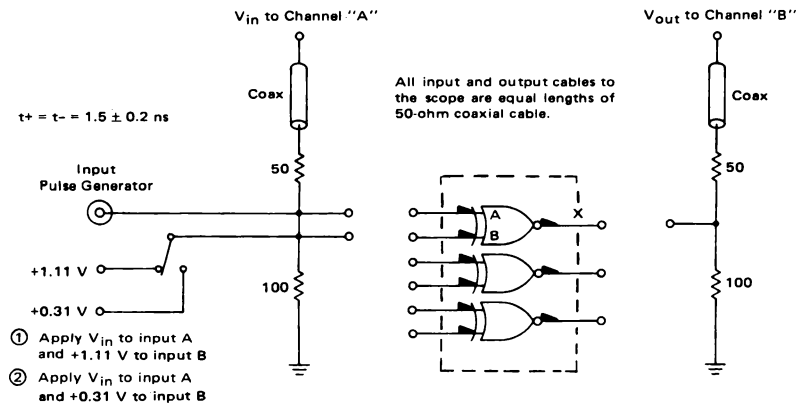
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1674L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current	I_{inH}	3,11,13	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	0.75 I_{inH}	5,6,7	–	–	–	270	–	–	μAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	$V_{OH\phi}$	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	3,5	–	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	3,5	–	–	8	1,16
Logic "0" Output Voltage	$V_{OL\phi}$	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	3	5	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	5	3	–	–	8	1,16
Logic "1" Threshold Voltage	$V_{OHA\phi}$	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	3,5	–	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	3,5	8	1,16
Logic "0" Threshold Voltage	$V_{OLA\phi}$	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	3	5	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	5	3	8	1,16
Switching Times (50 Ω Load)												Pulse In	Pulse Out		
Propagation Delay	t_{3+2+}	2	–	2.0	–	1.8	–	2.3	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	–	2.0	–	1.8	–	2.3		–	–				
	t_{3+2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{3-2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{5+2+}	2	–	2.5	–	2.3	–	2.8		–	–	5			
	t_{5-2+}	2	–		–		–			–	–				
	t_{5+2-}	2	–		–		–			–	–				
	t_{5-2-}	2	–		–		–			–	–				
Rise Time	t_{6+}	2	–	2.7	–	2.5	–	2.9	ns	–	–	3	2	8	1,16
Fall Time	t_{6-}	2	–	2.4	–	2.2	–	2.6	ns	–	–	3	2	8	1,16

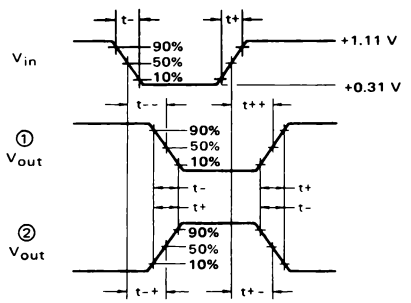
*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Unused outputs connected to a 50-ohm resistor to ground.

PROPAGATION DELAY



MC1678

DC Input Loading Factor
R = 2.40
C1 = 0.77
C2 = 1.23
S = 1.00

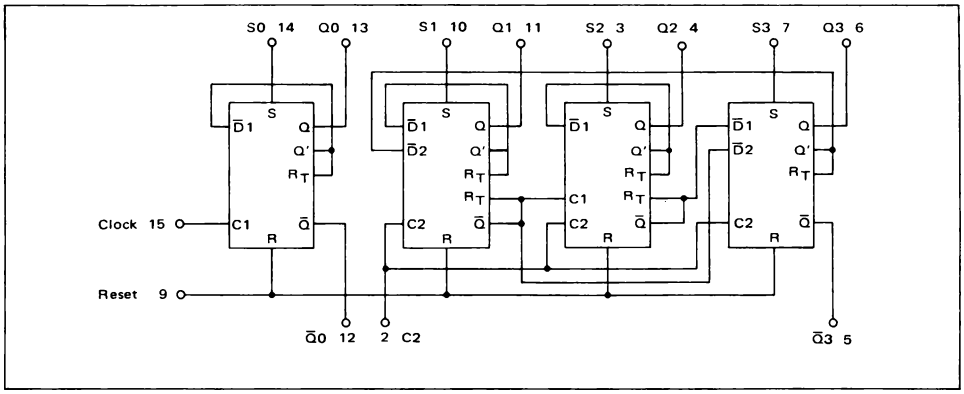
DC Output Loading Factor = 70

Power Dissipation = 750 mW typ

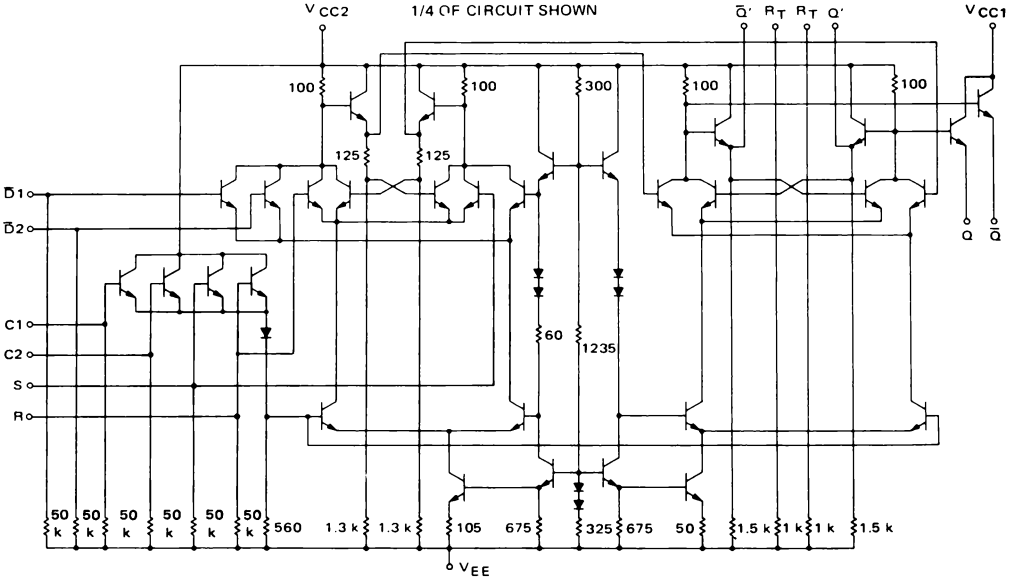
f_{Tog} = 350 MHz typ

The MC1678 is a four-bit counter capable of divide-by-two, divide-by-five, or divide-by-10 functions. When used independently, the divide-by-two section will toggle at 350 MHz typically, while the divide-by-five section will toggle at 325 MHz typically. Clock inputs trigger on the positive going edge of the clock pulse.

Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.



CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



See General Information section for packaging.

COUNTER TRUTH TABLES

BCD
(Clock connected to C1 and $\overline{Q0}$ connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

BI-QUINARY
(Clock connected to C2 and $\overline{Q3}$ connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

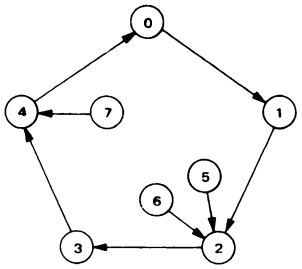
R-S

C	R	S	Q_{n+1}
ϕ	L	L	Q_n
ϕ	H	L	H
ϕ	L	H	H
ϕ	H	H	ND

ϕ = Don't Care
ND = Not Defined

COUNTER STATE DIAGRAM - POSITIVE LOGIC

Clock connected to C2



Q0 connected to C2

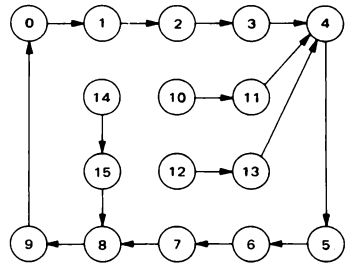
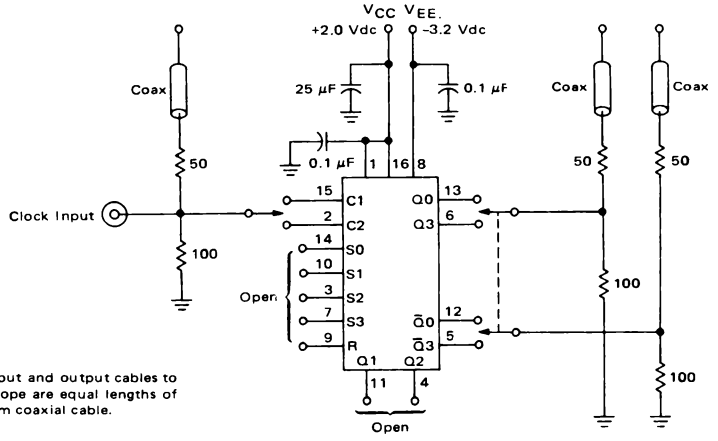


FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1678L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	200	–	–	mAdc	9		–	–	8	1,16
Input Current	$I_{in\ H}$	9	–	–	–	1.00	–	–	mAdc	9	–	–	–	8	1,16
		2	–	–	–	0.70	–	–	↓	2	–	–	–	↓	↓
		15	–	–	–	0.45	–	–		15	–	–	–		
		3,7,10,14	–	–	–	0.45	–	–		*	–	–	–		
	$I_{in\ L}$	9	–	–	0.5	–	–	–	μAdc	–	9	–	–	8	1,16
		2	–	–	0.5	–	–	–	↓	–	2	–	–	↓	↓
		3,7,10,14,15	–	–	0.5	–	–	–		–	*	–	–		
Logic "1" Output Voltage	V_{OH}	5,12 ①	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	3,7,10,14	–	–	8	1,16
		4,6,11,13 ②	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	9	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	5,12 ②	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	9	–	–	8	1,16
		4,6,11,13 ①	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	3,7,10,14	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	5,12 ③	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	3,7,10,14	8	1,16
		6,8,11,13 ④	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	5,12 ④	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	9	8	1,16
		4,6,13,16 ③	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	3,7,10,14	8	1,16
AC Characteristics												Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Delays 50 Ω Loads	t_{15+12+}	12	1.0	2.9	1.0	2.7	1.0	3.1	ns	–	–	15	12	8	1,16
	t_{15+13+}	13	↓	2.9	↓	2.7	↓	3.1	↓	–	–	15	13	↓	↓
	t_{2+11+}	11		3.2		3.0		3.4		–	–	2	11		
	t_{2+4+}	4		↓		↓		↓		–	–	2	4		
	t_{2+6+}	6								–	–	2	6		
	t_{2+5+}	5								–	–	2	5		
	t_{15+12-}	12	1.0	2.9	1.0	2.7	1.0	3.1	ns	–	–	15	12	8	1,16
	t_{15+13-}	13	↓	2.9	↓	2.7	↓	3.1	↓	–	–	15	13	↓	↓
	t_{3+11-}	11		3.2		3.0		3.4		–	–	2	11		
	t_{2+4-}	4		↓		↓		↓		–	–	2	4		
	t_{2+6-}	6								–	–	2	6		
	t_{2+5-}	5								–	–	2	5		
Set Delay	t_{14+13+}	13	2.0	3.9	2.0	3.7	2.0	4.1	ns	–	–	14	13	8	1,16
	t_{14+12-}	12	2.0	3.9	2.0	3.7	2.0	4.1	ns	–	–	14	12	8	1,16
Reset Delay	t_{9+12+}	12	2.0	3.9	2.0	3.7	2.0	4.1	ns	–	–	9	12	8	1,16
	t_{9+13-}	13	2.0	3.9	2.0	3.7	2.0	4.1	ns	–	–	9	13	8	1,16
Rise Time	t_{13+}	13	1.0	2.9	1.0	2.7	1.0	3.1	ns	–	–	15	13	8	1,16
	t_{12+}	12	1.0	2.9	1.0	2.7	1.0	3.1	ns	–	–	15	12	8	1,16
Fall Time	t_{13-}	13	1.0	2.8	1.0	2.6	1.0	3.0	ns	–	–	15	13	8	1,16
	t_{12-}	12	1.0	2.8	1.0	2.6	1.0	3.0	ns	–	–	15	12	8	1,16
Maximum Toggle Frequency 50 Ω Load	f_t	13 ⑤	260	–	300	–	260	–	MHz	–	–	–	–	8	1,16
	f_t	6 ⑤	250	–	275	–	250	–	MHz	–	–	–	–	8	1,16

*Individually apply V_{IH} or V_{IL} to input under test.

① Reset all four flip-flops by applying P_A to pin 9.

② Set all four flip-flops by applying P_A to pins 3, 7, 10, and 14 simultaneously.

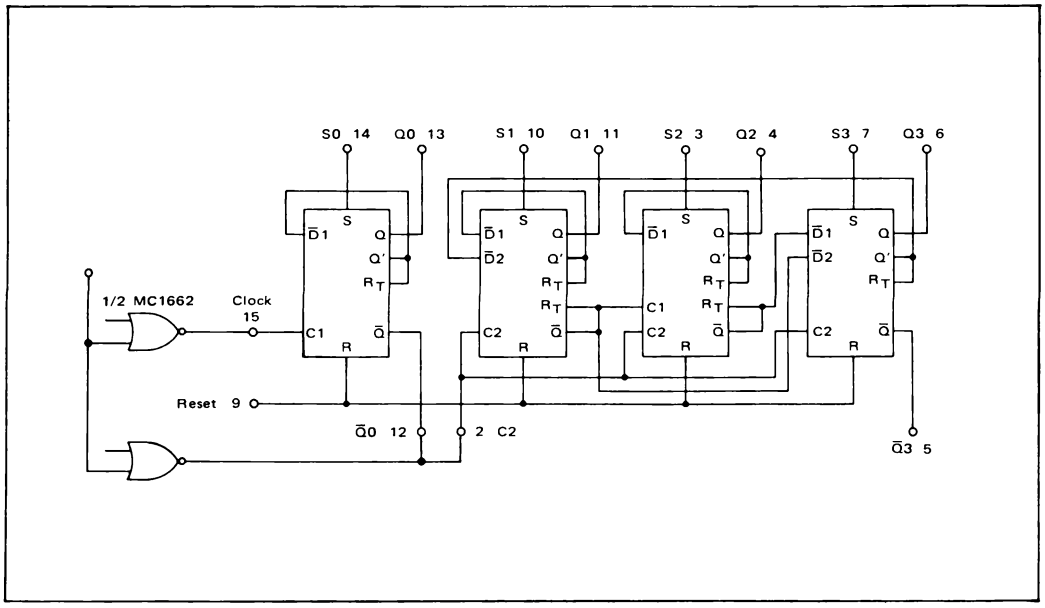
③ Reset all four flip-flops by applying P_A to pin 9.

④ Set all four flip-flops by applying P_A to pins 3, 7, 10, and 14 simultaneously. P_A ┐ V_{IH} ┘ V_{IL}

⑤ See Figure 1 for toggle test circuit

APPLICATIONS INFORMATION

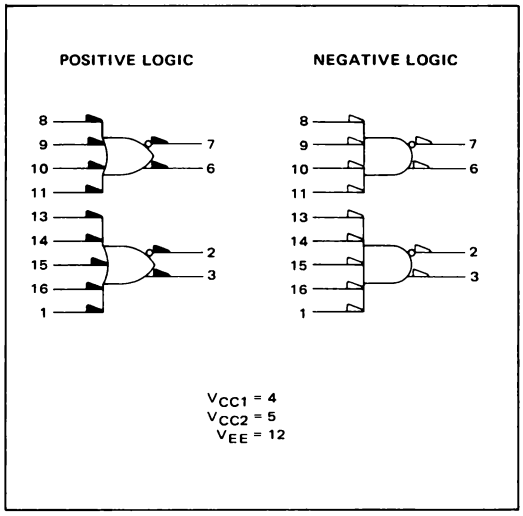
With the addition of a single gate package, the MC1678 will count in a fully synchronous mode, as shown below.



DUAL 4-5-INPUT
OR/NOR GATE

MC1688

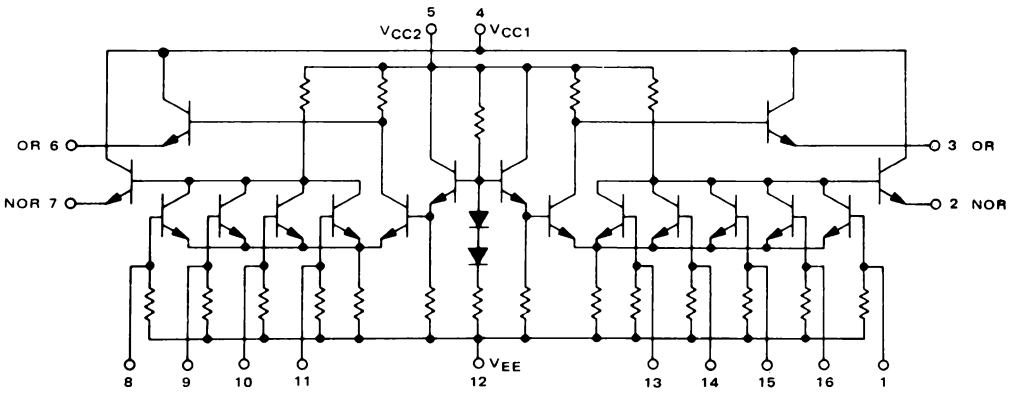
Advance Information



The MC1688 is a dual 4-5 input OR-NOR gate. All inputs are terminated by a 50 k ohm resistor to V_{EE} eliminating the need to tie unused inputs low.

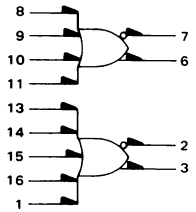
t_{pd} = 0.8 ns typ
P_D = 125 mW typ/pkg (No Load)
Output Rise and Fall Times
(10% to 90%) 1.7 ns
(20% to 80%) 1.1 ns

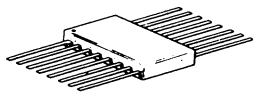
CIRCUIT SCHEMATIC



This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

Each MECL III series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.



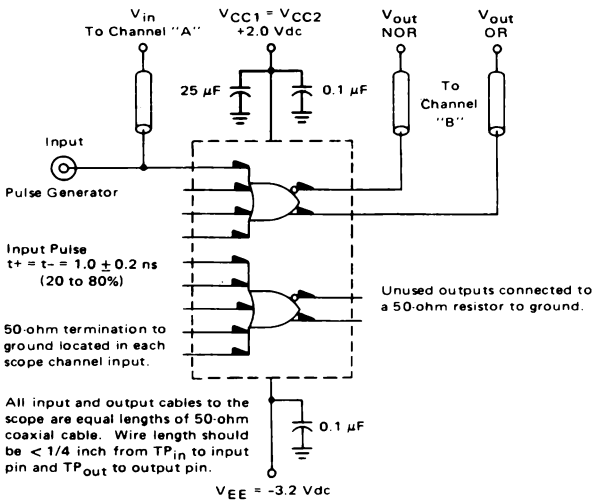


F SUFFIX
CERAMIC PACKAGE
CASE 650

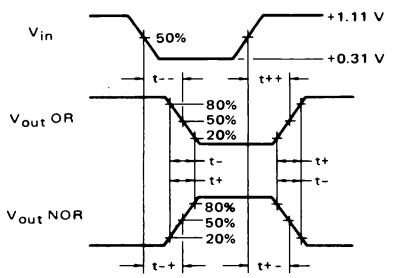
@ Test Temperature	$V_{IH\ max}$	$V_{IL\ min}$	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1688F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–	24	30	–	–	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	8	–	–	–	–	350	–	–	μAdc	8	–	–	–	12	4,5
	I_{inL}	8	–	–	0.5	–	–	–	–	μAdc	–	8	–	–	12	4,5
High Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	8	–	–	–	12	4,5
		7	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	8	–	–	12	4,5
Low Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	8	–	–	12	4,5
		7	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	8	–	–	–	12	4,5
High Threshold Voltage	V_{OHA}	6	-1.065	–	-0.980	–	–	-0.910	–	Vdc	–	–	8	–	12	4,5
		7	-1.065	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	8	12	4,5
Low Threshold Voltage	V_{OLA}	6	–	-1.630	–	–	-1.600	–	-1.555	Vdc	–	–	–	8	12	4,5
		7	–	-1.630	–	–	-1.600	–	-1.555	Vdc	–	–	8	–	12	4,5
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{8+7-}	7	–	–	–	0.8	–	–	–	ns	–	–	8	7	12	4,5
	t_{8-7+}	7	–	–	–	↓	–	–	–	↓	–	–	↓	7	↓	↓
	t_{8+6+}	6	–	–	–	↓	–	–	–	↓	–	–	↓	6	↓	↓
	t_{8-6-}	6	–	–	–	↓	–	–	–	↓	–	–	↓	6	↓	↓
Rise Time (20 to 80%)/(10 to 90%)	t_{7+}	7	–	–	–	1.1/1.7	–	–	–	↓	–	–	↓	7	↓	↓
	t_{6+}	6	–	–	–	↓	–	–	–	↓	–	–	↓	6	↓	↓
Fall Time (20 to 80%)/(10 to 90%)	t_{7-}	7	–	–	–	↓	–	–	–	↓	–	–	↓	7	↓	↓
	t_{6-}	6	–	–	–	↓	–	–	–	↓	–	–	↓	6	↓	↓

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



PROPAGATION DELAY



UHF PRESCALER
TYPE D FLIP-FLOP

MC1690

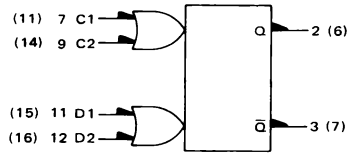
Advance Information

P_D = 200 mW typ/pkg (No Load)
f_{tog} = 500 MHz min

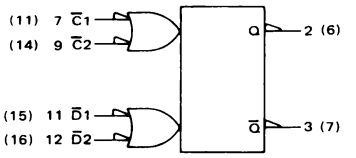
The MC1690 is a high speed D master-slave flip-flop capable of toggle rates over 500 MHz. Designed primarily for high speed prescaling applications in communications and instrumentation, this device employs two data inputs, two clock inputs and complementary Q and $\overline{Q}$ outputs. It is a higher frequency replacement for the MC1670 (350 MHz) D flip-flop. There are no set or reset inputs and an extra data input is provided.

When used with the MC1678, the MC1690 provides a decade counter capable of 500 MHz operation.

POSITIVE LOGIC



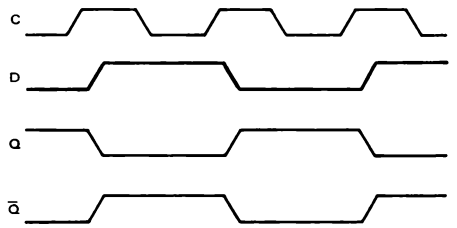
NEGATIVE LOGIC



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

TIMING DIAGRAM



TRUTH TABLE

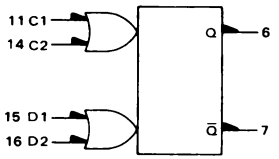
C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
⎍	L	L
⎍	H	H

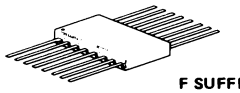
C = C1 + C2
D = D1 + D2
ϕ = Don't Care

This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

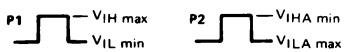




F SUFFIX
CERAMIC PACKAGE
CASE 650

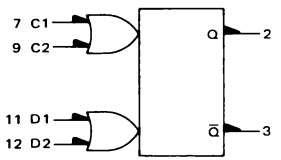
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

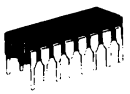
Characteristic	Symbol	Pin Under Test	MC1690F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} max	V_{IHA} min	V_{ILA} max	V_{EE}	P1	P2	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–		59	–	–	mAdc	11,14,15,16	–	–	–	12	–	–	4,5
Input Current	I_{inH}	11	–	–	–		250	–	–	μAdc	11	–	–	–	12	–	–	4,5
		15	–	–	–		270	–	–	μAdc	15	–	–	–	12	–	–	4,5
	I_{inL}	11	–	–	0.5		–	–	–	μAdc	–	11	–	–	12	–	–	4,5
		15	–	–	0.5		–	–	–	μAdc	–	15	–	–	12	–	–	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960		-0.810	-0.890	-0.700	Vdc	15	–	–	–	12	11	–	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850		-1.620	-1.830	-1.575	Vdc	–	15	–	–	12	11	–	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.065	–	-0.980		–	-0.910	–	Vdc	15	–	–	–	12	–	11	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.630	–		-1.600	–	-1.555	Vdc	–	15	–	–	12	–	11	4,5
Switching Parameters					Min	Typ	Max								-3.2 Vdc			+2.0 Vdc
Clock to Output Delay (See Figure 1)	t_{11+6+}	6	–		–	1.5	–	–		ns	–	–	–	–	12	–	–	4,5
	t_{14+6+}		–	–	–	1.5	–	–	–		–	–	–	–		–	–	
Output Rise Time	t_+		–	–	–	1.3	–				–	–	–	–		–	–	
Output Fall Time	t_-		–		–	1.3		–	–		–	–	–	–		–	–	
Setup Time (See Figure 2)	$t_{setup\ H}$		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
	$t_{setup\ L}$		–	–	–	0.3	–		–		–	–	–	–		–	–	
Hold Time (See Figure 2)	$t_{hold\ H}$		–	–	–	0.2	–		–		–	–	–	–		–	–	
	$t_{hold\ L}$		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
Toggle Frequency (See Figure 3)	f_{tog}	6	500	–	500	550	–	500	–	MHz	–	–	–	–	12	–	–	4,5



ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1690L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P1	P2	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–		59	–	–	mAdc	7,9,11,12	–	–	–	8	–	–	1,16
Input Current	$I_{in\ H}$	7	–	–	–		250	–	–	µAdc	7	–	–	–	8	–	–	1,16
		11	–	–	–		270	–	–	µAdc	11	–	–	–	8	–	–	1,16
	$I_{in\ L}$	7	–	–	0.5		–	–	–	µAdc	–	7	–	–	8	–	–	1,16
		11	–	–	0.5		–	–	–	µAdc	–	11	–	–	8	–	–	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960		-0.810	-0.890	-0.700	Vdc	11	–	–	–	8	7	–	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850		-1.620	-1.830	-1.575	Vdc	–	11	–	–	8	7	–	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980		–	-0.910	–	Vdc	11	–	–	–	8	–	7	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–		-1.600	–	-1.555	Vdc	–	11	–	–	8	–	7	1,16
Switching Parameters					Min	Typ	Max								-3.2 Vdc			+2.0 Vdc
Clock to Output Delay (See Figure 1)	t_{7+2+}	2	–	–	–	1.5	–	–	–	ns	–	–	–	–	8	–	–	1,16
	t_{9+2+}		–	–	–	1.5	–	–	–		–	–	–	–		–	–	
Output Rise Time	t_+		–	–	–	1.3	–	–	–		–	–	–	–		–	–	
Fall Time	t_-		–	–	–	1.3	–	–	–		–	–	–	–		–	–	
Setup Time (See Figure 2)	$t_{setup\ H}$		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
	$t_{setup\ L}$		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
Hold Time (See Figure 2)	$t_{hold\ H}$		–	–	–	0.2	–	–	–		–	–	–	–		–	–	
	$t_{hold\ L}$		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
Toggle Frequency (See Figure 3)	f_{tog}	2	500	–	500	540	–	500	–	MHz	–	–	–	–	8	–	–	1,16

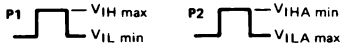
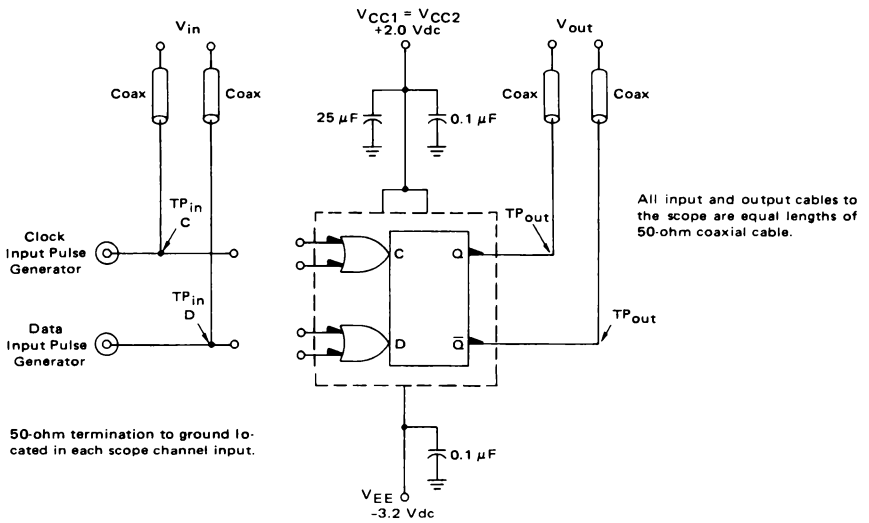


FIGURE 1 – PROPAGATION DELAY TEST CIRCUIT



CLOCK DELAY WAVEFORMS @ 25°C

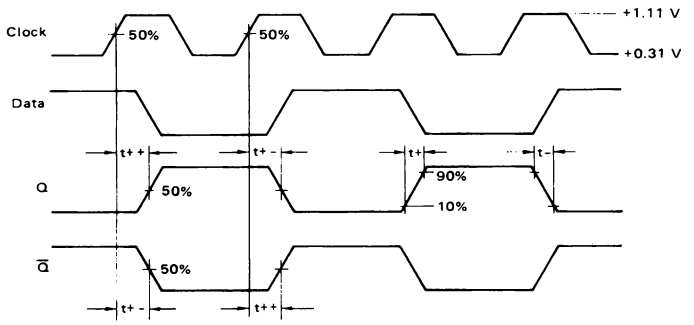
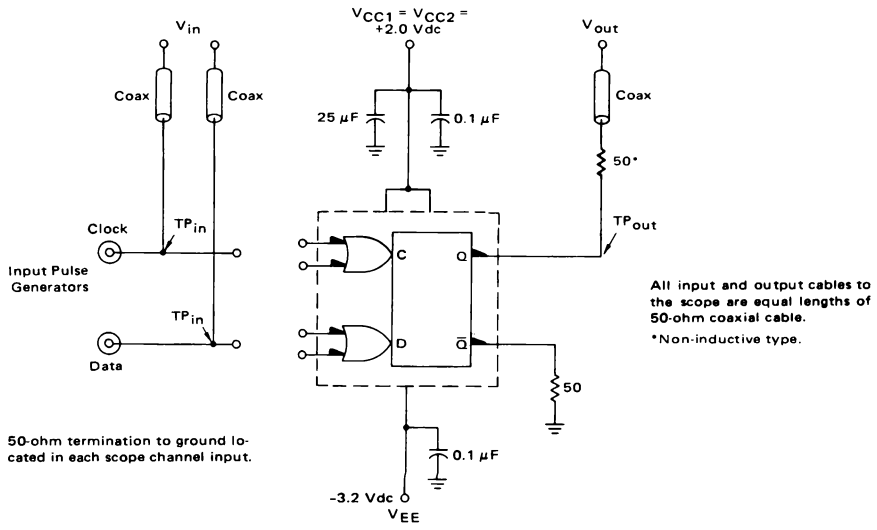
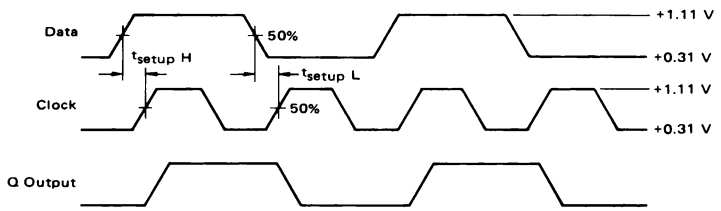


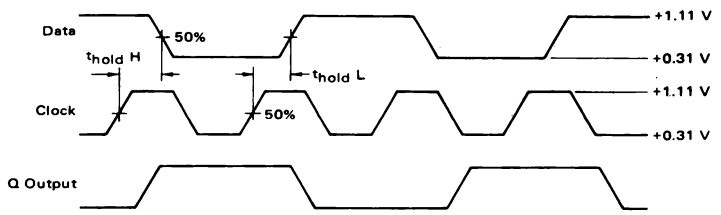
FIGURE 2 – SETUP AND HOLD TIME TEST CIRCUIT



SETUP TIME WAVEFORMS @ 25°C



HOLD TIME WAVEFORMS @ 25°C



Setup time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data (D) input.

FIGURE 3 – TOGGLE FREQUENCY TEST CIRCUIT

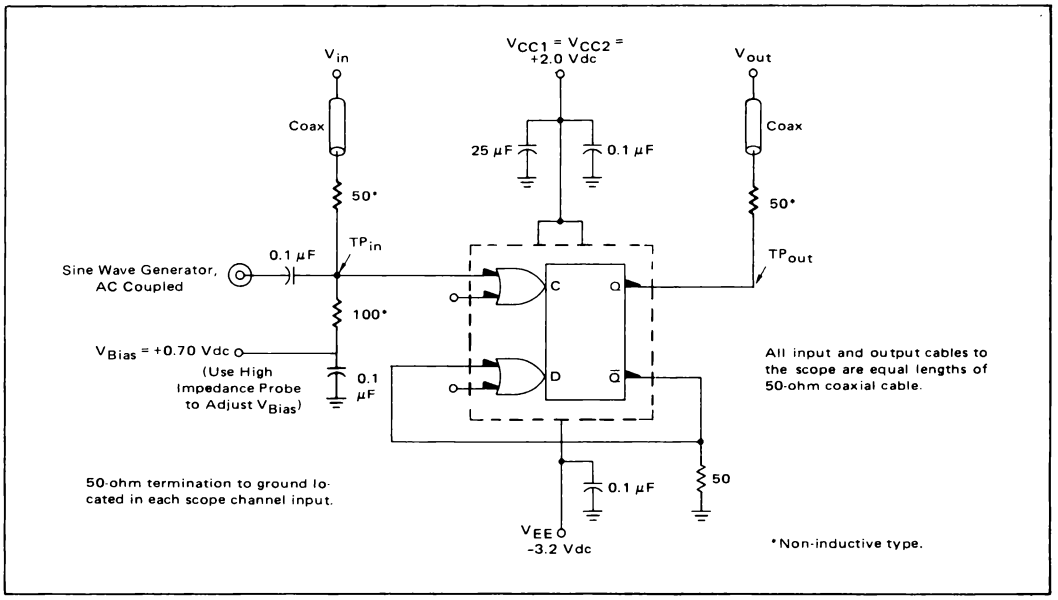
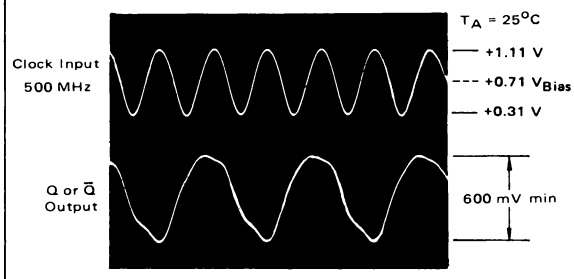


FIGURE 4 – TOGGLE FREQUENCY WAVEFORMS



The maximum toggle frequency of the MC1690 has been exceeded when either:

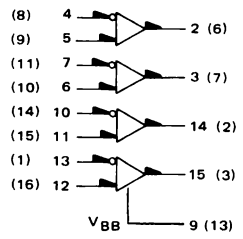
1. The output peak-to-peak voltage swing falls below 600 millivolts,

   OR

2. The device ceases to toggle (divide by two).

MC1692

Four differential amplifiers with emitter followers intended for use in sensing differential signals over long lines.



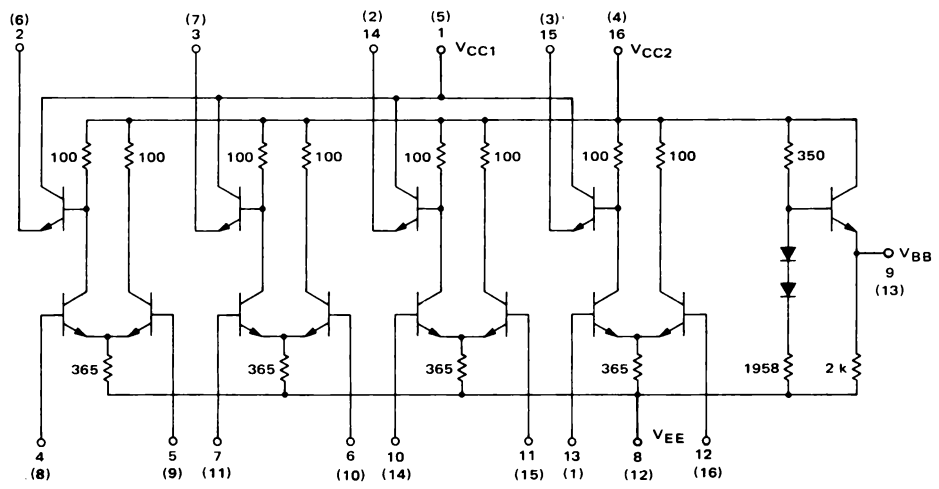
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 220 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

Number at end of terminals denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

CIRCUIT SCHEMATIC

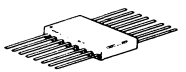


Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

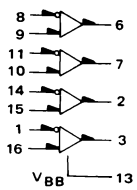
See General Information section for packaging information.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



F SUFFIX
CERAMIC PACKAGE
CASE 650

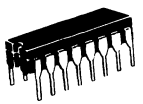


@ Test Temperature	TEST VOLTAGE VALUES						
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	
-30°C	-0.875	-1.890	-1.180	-1.515	From Pin 13	-5.2	
+25°C	-0.810	-1.850	-1.095	-1.485		-5.2	
+85°C	-0.700	-1.830	-1.025	-1.440		-5.2	

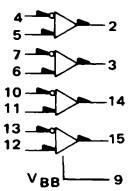
Characteristic	Symbol	Pin Under Test	MC1692F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–	50	–	–	mAdc	–	1,8,11,14	–	–	9,10,15,16	12	4,5
Input Current	I_{in}	8	–	–	–	250	–	–	μAdc	8	1,11,14	–	–	9,10,15,16	12	4,5
Input Leakage Current	I_R	8	–	–	–	100	–	–	μAdc	–	1,11,14	–	–	9,10,15,16	8,12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	1,11,14	8	–	–	9,10,15,16	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	8	1,11,14	–	–	9,10,15,16	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	1,11,14	–	8	9,10,15,16	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	1,11,14	8	–	9,10,15,16	12	4,5
Reference Voltage	V_{BB}	13	1.375	1.275	-1.35	-1.25	1.30	1.20	Vdc	–	–	–	–	9,10,15,16	12	4,5
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max		Pulse In		Pulse Out				
Propagation Delay	t_{8-6+}	6	–	1.6	–	1.5	–	1.7	ns	8		6		9,10,15,16	12	4,5
	t_{8+6-}	6	–	1.8	–	1.7	–	1.9								
Rise Time	t_{6+}	6	–	2.2	–	2.1	–	2.3								
Fall Time	t_{6-}	6	–	2.2	–	2.1	–	2.3								

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



L SUFFIX
CERAMIC PACKAGE
CASE 620



@ Test Temperature	TEST VOLTAGE VALUES					
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	From Pin 9	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485		-5.2
+85°C	-0.700	-1.830	-1.025	-1.440		-5.2

Characteristic	Symbol	Pin Under Test	MC1692L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	50	–	–	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	I_{in}	4	–	–	–	250	–	–	μAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Input Leakage Current	I_R	4	–	–	–	100	–	–	μAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	1.375	1.275	-1.35	-1.25	1.30	1.20	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max		Pulse In		Pulse Out				
Propagation Delay	t_{4-2+}	2	–	1.6	–	1.5	–	1.7	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	–	1.8	–	1.7	–	1.9								
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3								
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3								

APPLICATIONS INFORMATION

The MC1692 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. The line is driven with a MC1660 OR/NOR gate. The MC1660 is terminated with 50 ohm resistors to -2.0 volts. At the end of the twisted pair a 100 ohm termination resistor is placed across the differential line receiver inputs of the MC1692. Illustrated in Figure 2 is the sending and receiving waveforms at a data rate of 400 megabits per second over an 18 foot twisted pair cable. The waveform picture of Figure 3 shows a 5 nanosecond pulse being propagated down the 18 foot line. The delay time for the line is 1.68 ns/foot.

The MC1692 may also be applied as a high frequency schmitt trigger as illustrated in Figure 4. This circuit has been used in excess of 200 MHz. The MC1692 when loaded into 50 ohms will produce an output rising edge of about 1.5 nanoseconds.

FIGURE 1 – LINE DRIVER/RECEIVER

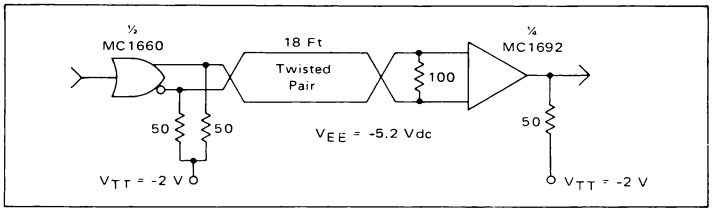


FIGURE 2 – 400 MBS WAVEFORMS

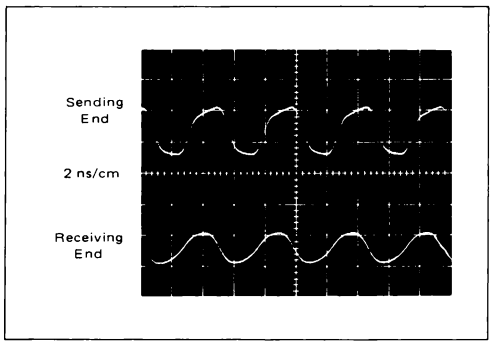
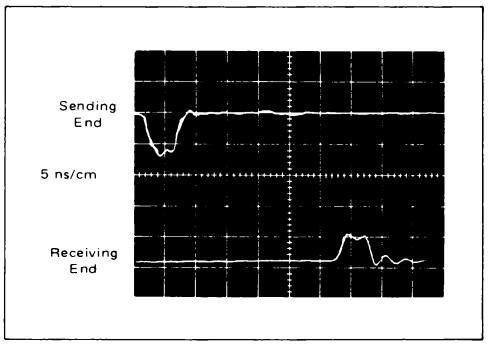


FIGURE 3 – PULSE PROPAGATION WAVEFORMS



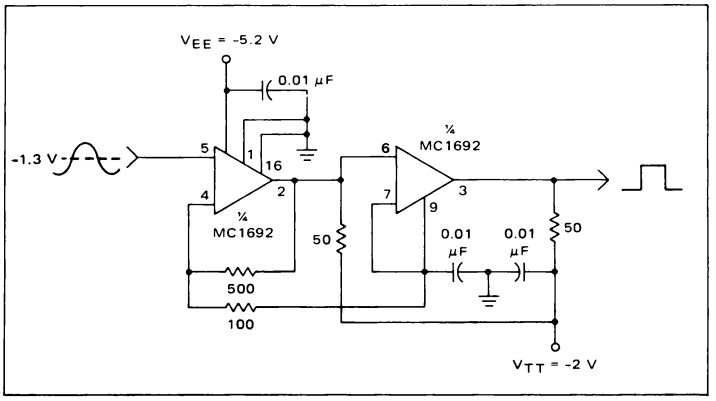


FIGURE 4 – 200 MHz SCHMITT TRIGGER

MC1694

The MC1694 is a 4-Bit register capable of shift rates up to 325 MHz (typical). This shift register operates in the shift-right mode, accepting serial data at either data input D1 or D2. A master reset and individual set inputs override the clock allowing asynchronous entry of information.

FLIP-FLOP TRUTH TABLE

Inputs				Output
D	C	R	S	Q_n
0	0	0	0	Q_{n-1}
0	0	0	1	1
0	0	1	0	0
0	0	1	1	*
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	*
1	0	0	0	Q_{n-1}
1	0	0	1	1
1	0	1	0	0
1	0	1	1	*
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	*

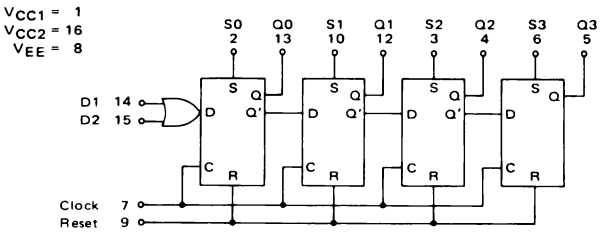
*Output State Undefined

DC Input Loading Factors
Reset = 2.5 Set = 1.0
Clock = 1.6 Data = 0.9

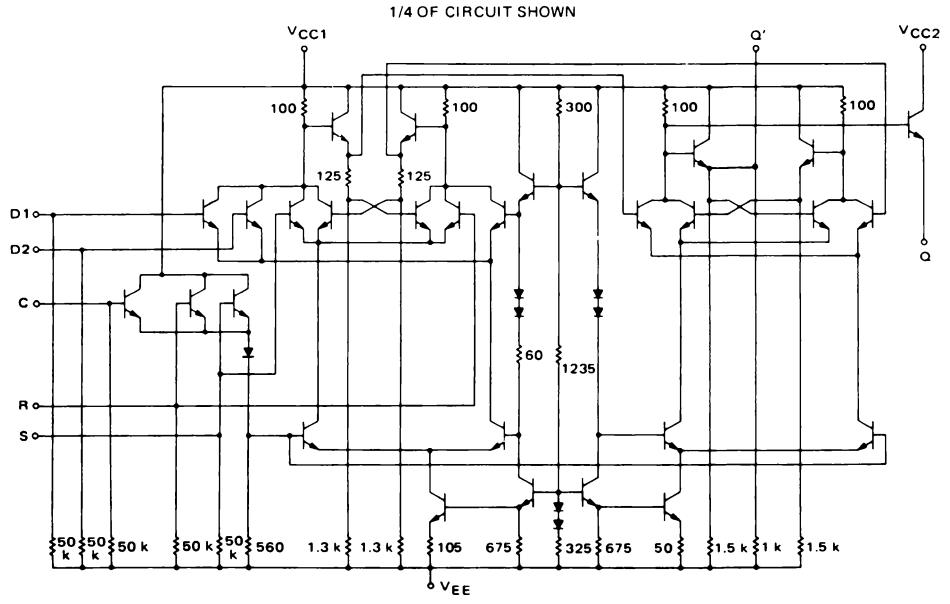
DC Output Loading Factor = 70

Total Power Dissipation = 750 mW typ/pkg
Shift Frequency = 325 MHz typ

LOGIC DIAGRAM



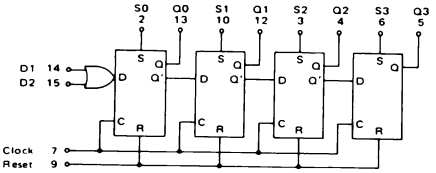
FLIP-FLOP ELEMENT CIRCUIT SCHEMATIC

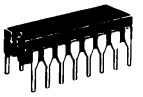


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





L SUFFIX
CERAMIC PACKAGE
CASE 620

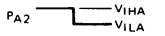
@ Test Temperature	TEST VOLTAGE VALUES V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1694L -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	200	–	–	mAdc	9	–	–	–	8	1,16
Input Current	$I_{in\ H}$	9	–	–	–	1.0	–	–	mAdc	9	–	–	–	8	1,16
		7	–	–	–	0.750		–		7	–	–	–		
		2,3,6,10	–	–	–	0.6	–			*	–	–	–		
		14,15	–	–	–	0.5	–	–		*	–	–	–		
	$I_{in\ L}$	7,9	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
		2,3,6,10	–	–	0.5	–	–	–		–	*	–	–		
		14,15	–	–	0.5	–		–		–	*	–	–		
Logic "1" Output Voltage	V_{OH}	4,5,12,13	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	①	9	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	4,5,12,13	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	②	2,3,6,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	4,5,12,13	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	③	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	4,5,12,13	–	-1.630	–	-1.600	–	-1.555	Vdc	–	2,3,6,10	④	–	8	1,16
AC Characteristics												Pulse In	Pulse Out	-3.2 V	+2.0 V
Clock Delays (50 Ω Loads)	t_{7+X+}	4,5,12,13	1.0	3.2	1.0	3.0	1.0	3.4	ns	–	–	7	X	8	1,16
	t_{7+X-}	4,5,12,13	1.0	3.2	1.0	3.0	1.0	3.4	ns		–	7	X	8	1,16
Set Delay	t_{Y+X+}	4,5,12,13	2.0	3.9	2.0	3.7	2.0	4.1	ns	–	–	Y	X	8	1,16
Reset Delay	t_{9+X-}	4,5,12,13	2.0	3.9	2.0	3.7	2.0	4.1	ns	–	–	9	X	8	1,16
Rise Time	t_{X+}	4,5,12,13	1.0	2.9	1.0	2.7	1.0	3.1	ns	–	–	X	X	8	1,16
Fall Time	t_{X-}	4,5,12,13	1.0	2.8	1.0	2.6	1.0	3.0	ns	–	–	9	X	8	1,16
Shift Rate		⑤	240	–	275	–	250	–	MHz	–	–	–	–	–	–

*Individually apply V_{IH} or V_{IL} to input under test.
X = Pin 4,5,12 or 13
Y = Pin 2,3,6 or 10

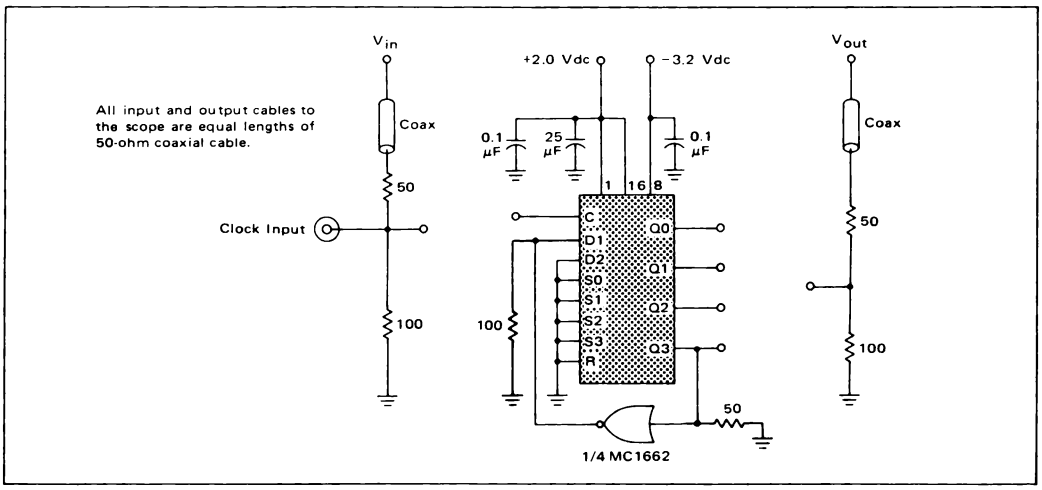
① Reset all four flip-flops by applying P_{A1} to pin 9
② Set all four flip-flops by applying P_{A1} to pins 2,3,6, and 10 simultaneously
③ Reset all four flip-flops by applying P_{A2} to pin 10

④ Set all four flip-flops by applying P_{A2} to pins 2,3,6, and 14 simultaneously.



⑤ See Figure 1 for shift frequency test circuit.

FIGURE 1 – SHIFT FREQUENCY TEST CIRCUIT



COMPATIBLE
INTEGRATED CIRCUITS

MC1543L

DUAL SENSE AMPLIFIER

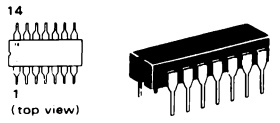
MONOLITHIC DUAL MECL CORE MEMORY SENSE AMPLIFIER

. . . a dual dc coupled sense amplifier providing output levels compatible with emitter-coupled logic levels. The MC1543L offers adjustable threshold and excellent threshold stability over a wide range of power-supply voltage variation.

- Input Threshold – Adjustable from 10 to 40 mV (Positive or Negative Signals)
- Both OR and NOR Outputs Available
- Low Power Dissipation
- Threshold Insensitive V_{CC} or V_{EE} Voltage Variation
- Each Amplifier is Separately Strobed

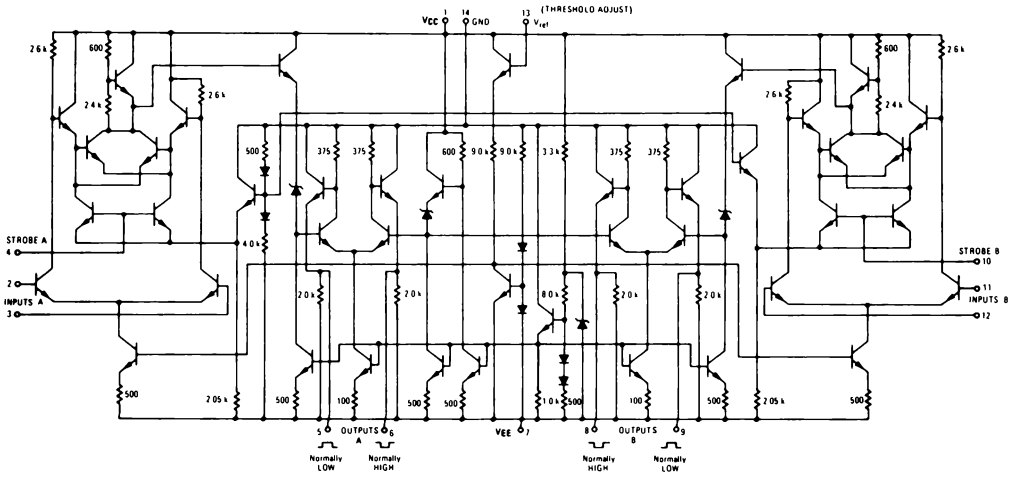
DUAL MECL CORE MEMORY SENSE AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 632
TO-116

CIRCUIT SCHEMATIC



See General Information section for packaging

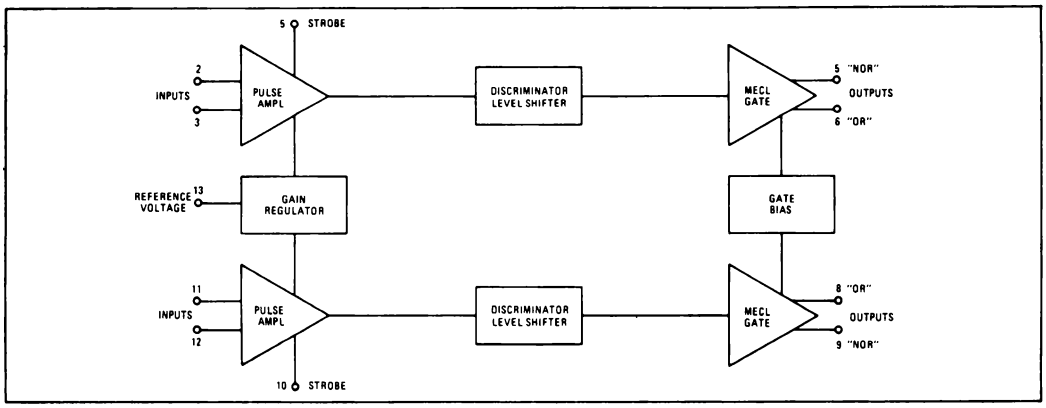
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+10 -10	Vdc Vdc
Differential Input Voltage	V_{ID}	±5.0	Vdc
Common-Mode Input Voltage	V_{ICM}	±5.0	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Ceramic Dual-In-Line Package Derate above T_A = +25°C	P_D	 1000 6.7	 mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Each Amplifier) (V_{CC} = +5.0 Vdc ±5%, V_{EE} = -5.2 Vdc ±5%, V_{ref} = 0.54 V ±1%, T_A = +25°C unless otherwise noted.)

Characteristic	Fig.No.	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage	8	V_{TH}	17	20	23	mV
Power Supply Currents (V_2 = V_3 = V_{11} = V_{12} = V_{14} = 0)	6 6	I_{CC} I_{EE}	– –	9.5 26.5	12 33	mAdc mAdc
Input Bias Current	7	I_{IB}	–	3.5	10	µAdc
Input Offset Current	7	I_{IO}	–	0.05	0.5	µAdc
Output Voltage High	9	V_{OH}	-0.85	-0.8	-0.67	Vdc
Output Voltage Low	9	V_{OL}	–	-1.7	-1.46	Vdc
Strobe Threshold Level	10	V_{ST}	–	-1.30	–	Vdc
Strobe Input Current High	10	I_{SH}	–	25	50	µAdc
Strobe Input Current Low	10	I_{SL}	–	0.01	0.1	µAdc
Input Common Mode Range	14	V_{CMR}	3.0	4.0	–	Vdc
Input Threshold Range (by varying V_{ref})	8	V_{THR}	–	10-40	–	mV
Power Dissipation	6	P_D	–	185	230	mW
Reference Supply Input Current (Pin 13)	6	I_{ref}	–	10	40	µA
SWITCHING CHARACTERISTICS						
Propagation Delay (Input to Output)	1	t_{IO}	–	28	35	ns
Propagation Delay (Strobe to Output)	12	t_{SO}	–	16	20	ns
Strobe Release Time	12	t_{SR}	–	18	30	ns
Recovery Time (Differential-Mode) (e_{in} = 400 mVdc)	13	t_{DR}	–	10	15	ns
Recovery Time (Common-Mode) (e_{in} = 3.0 Vdc)	14	t_{CMR}	–	3.0	15	ns
Strobe Width Minimum	12	t_S	–	8.0	–	ns
TEMPERATURE TESTS (-55°C to +125°C)						
Input Threshold Voltage T_A = -55°C T_A = +125°C	8	V_{TH}	 18 15	 21.5 18.5	 25 22	mV
Input Bias Current	7	I_{IB}	2.2	7.0	20	µAdc
Input Offset Current	7	I_{IO}	0.02	0.1	1.0	µAdc

EQUIVALENT CIRCUIT



TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 Vdc, V_{EE} = -5.2 Vdc, V_{ref} set for 20 mV Threshold, T_A = +25°C unless otherwise noted.)

FIGURE 1 – TYPICAL INPUT THRESHOLD versus TEMPERATURE

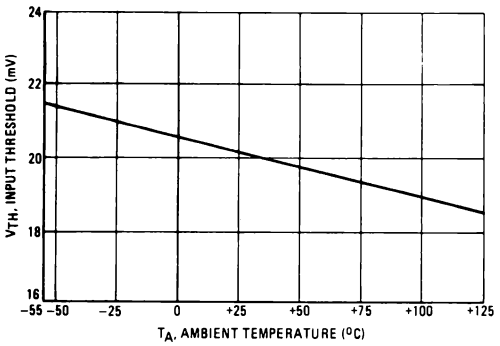


FIGURE 2 – TYPICAL INPUT THRESHOLD versus REFERENCE VOLTAGE

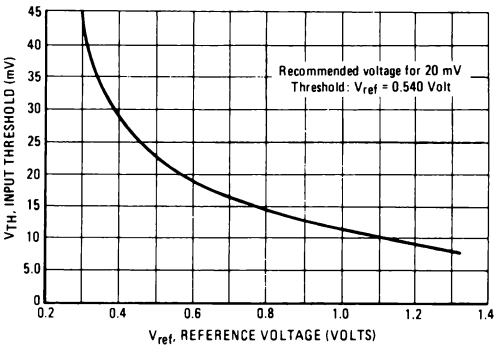


FIGURE 3A – TYPICAL INPUT THRESHOLD versus V_{CC}

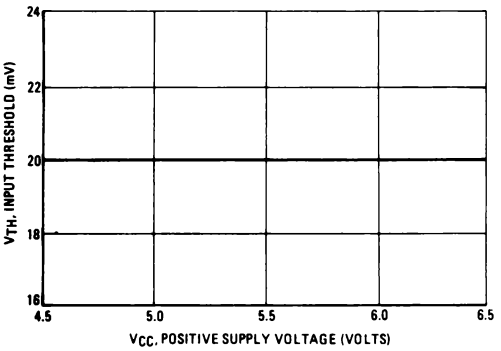
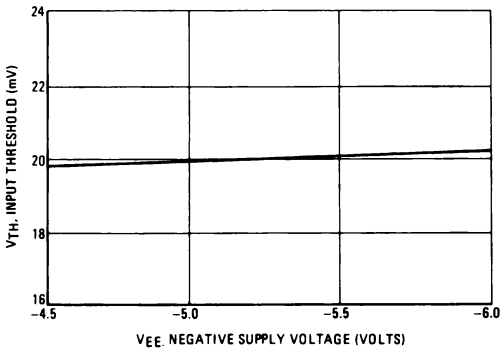


FIGURE 3B – TYPICAL INPUT THRESHOLD versus V_{EE}



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 Vdc, V_{EE} = -5.2 Vdc, V_{ref} set for 20 mV Threshold, T_A = +25°C unless otherwise noted.)

FIGURE 4 – TYPICAL INPUT THRESHOLD versus INPUT PULSE WIDTH

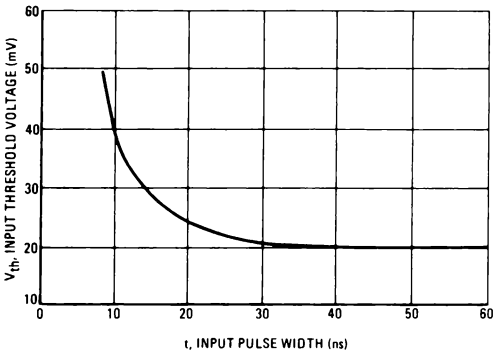
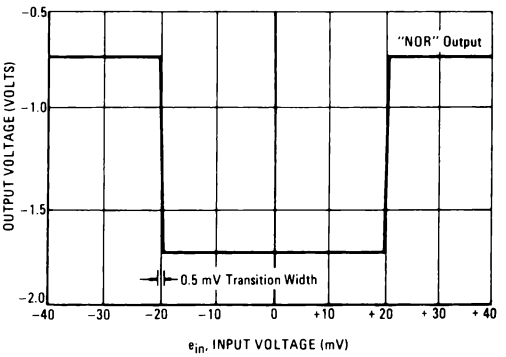


FIGURE 5 – INPUT-OUTPUT TRANSFER CHARACTERISTICS (one output)



TEST CIRCUITS

(V_{CC} = +5.0 Vdc, V_{EE} = -5.2 Vdc, V_{ref} = 0.54 V, T_A = +25°C unless otherwise noted.)

FIGURE 6 – POWER SUPPLY CURRENT DRAIN

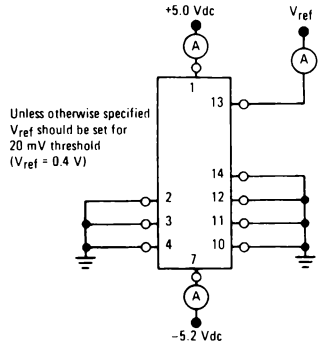


FIGURE 7 – INPUT BIAS CURRENT INPUT OFFSET CURRENT

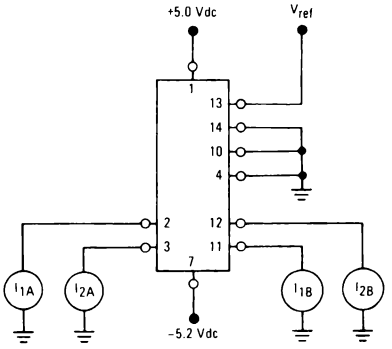


FIGURE 8 – INPUT THRESHOLD LEVEL

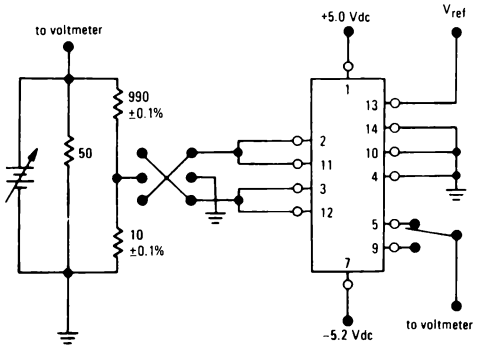
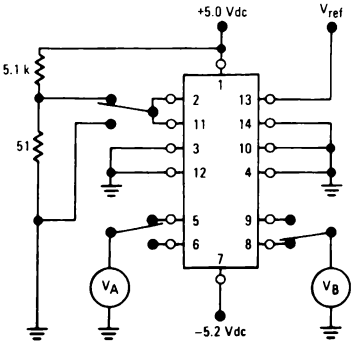


FIGURE 9 – OUTPUT VOLTAGE LEVELS



TEST CIRCUITS (continued)

FIGURE 10 – STROBE THRESHOLD LEVEL
STROBE INPUT CURRENTS

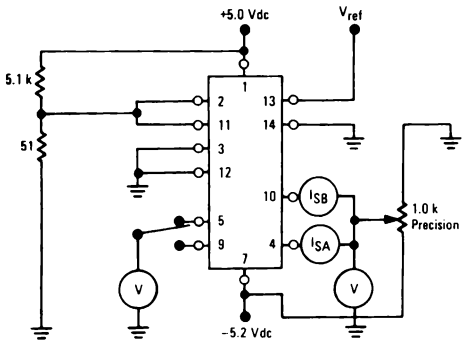


FIGURE 11 – PROPAGATION DELAY –
INPUT TO OUTPUT

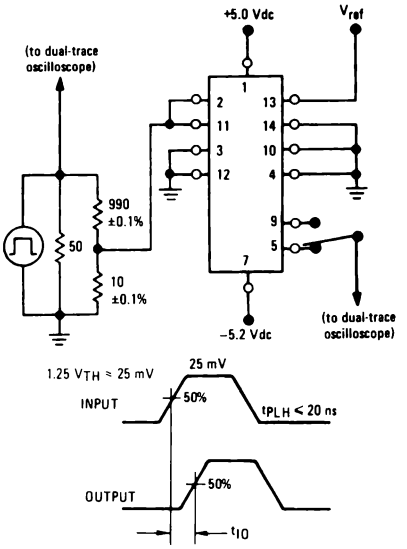


FIGURE 12 – PROPAGATION DELAY – STROBE TO
OUTPUT and STROBE RELEASE TIME

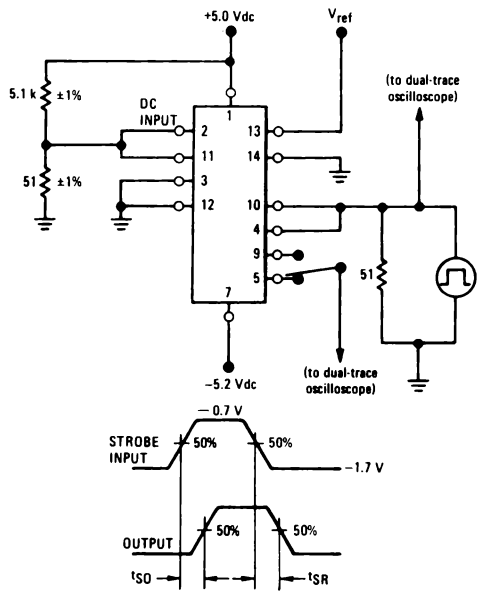
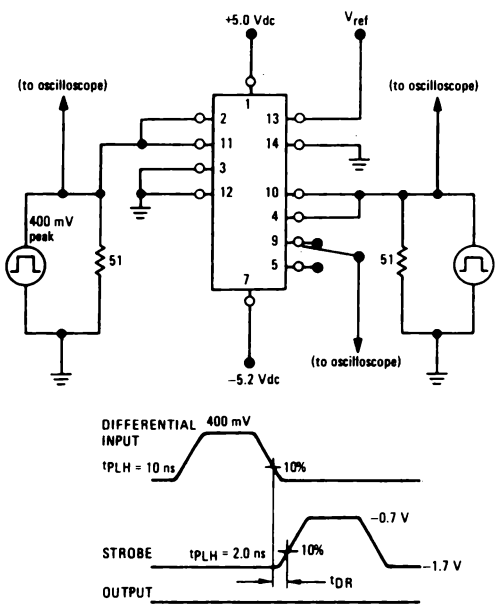
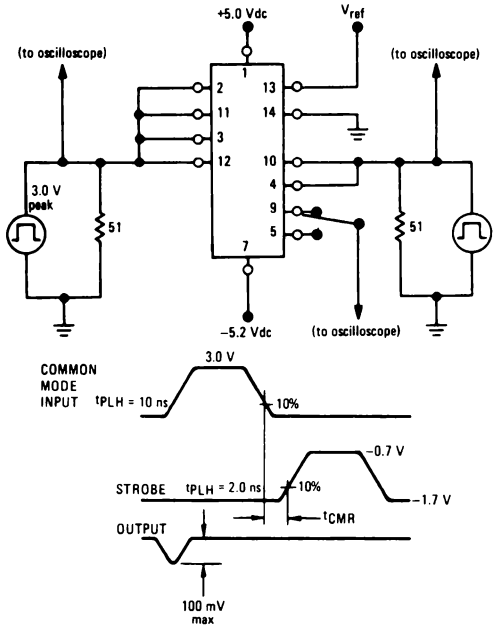


FIGURE 13 – DIFFERENTIAL MODE RECOVERY TIME
(See definition section)



TEST CIRCUITS (continued)

FIGURE 14 – COMMON MODE RECOVERY TIME
COMMON MODE INPUT RANGE
(See definition section)



DEFINITIONS

I_{IO} Input Offset Current – The difference between amplifier input current values $|I_{1A} - I_{2A}|$ or $|I_{1B} - I_{2B}|$.

I_{SH} Strobe High Current – The amount of input current when the strobe pin is grounded.

I_{SL} Strobe Low Current – The leakage current when the strobe input is tied to the negative supply.

P_D Power Dissipation – The amount of power dissipated in the unit.

t_{CMR} Common-Mode Recovery Time – The minimum time by which the strobe input may follow the high level common mode input signal without causing a signal to appear at the amplifier output.

t_{DR} Differential-Mode Recovery Time – Differential recovery time, the minimum time by which the strobe input may follow the high level differential input signal without causing a signal to appear at the amplifier output.

t_{IO} Propagation Delay, Amplifier Input to Amplifier Output – The time required for the amplifier output to reach 50% of its final value as referenced to 50% of the level of the pulse input. (Amplifier input = 25% over set threshold or approximately 25 mVdc.)

t_S Strobe Width – The amount of time the strobe must be high to obtain a given output. Minimum strobe width is that minimum time required to cause the output to complete a full swing V_{OL} to V_{OH} or V_{OH} to V_{OL}.

t_{SO} Propagation Delay, Strobe Input to Amplifier Output – The time required for the amplifier output pulse to achieve 50% of its final value referenced to 50% of the strobe input pulse at pins 4 or 10.

t_{SR} Strobe Release Time – The time required for the output to change to 50% of its swing after the strobe reaches 50% of its level going low. A dc level of 50 mV is the input signal.

V_{CMR} Maximum Common-Mode Input Range – The common-mode input voltage which causes the output voltage level of the amplifier to change by 100 mV (strobe high).

V_{OH} Output Voltage High – The high-level output voltage at pins 6 and 8 with no input – or at pins 5 and 9 with input above threshold.

V_{OL} Output Voltage Low – The low-level output voltage at pins 5 and 9 with no input – or at pins 6 and 8 with input above threshold.

V_{ST} Strobe Threshold Level – The voltage at which the strobe turns the amplifier to the ON state.

V_{TH} Input Threshold – Input pulse amplitude at pins 2, 3, 11, or 12 that causes the output gate to just reach its new value, V_{OL} or V_{OH}.

V_{THR} Input Threshold Range – The maximum spread of input threshold level that can be attained by varying the threshold voltage reference, V_{ref}.

MC7900C Series

NEGATIVE VOLTAGE REGULATORS

MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

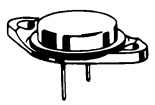
The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation – making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

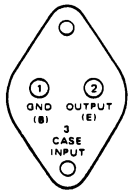
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 199-04
  (Pin Compatible with the VERSAWATT† or TO-220)
  Or Hermetic TO-3 Type Metal Power Package

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

MONOLITHIC SILICON INTEGRATED CIRCUITS

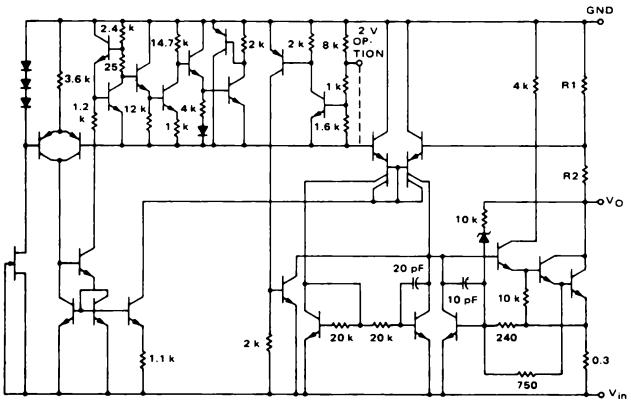


K SUFFIX
METAL PACKAGE
CASE 11
(TO-3 TYPE)



(bottom view)

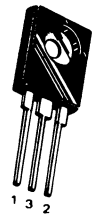
SCHEMATIC DIAGRAM



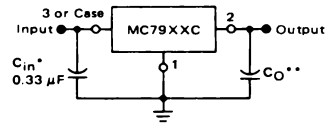
P SUFFIX
PLASTIC PACKAGE
CASE 199-04

Pin 1 GND (B)
Pin 2 Output (E)
Pin 3 Input (C)

Heat sink surface connected to pin 3.



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C - 2.0 Volts	MC7906C - 6.0 Volts	MC7915C - 15 Volts
MC7905C - 5.0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C - 5.2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

†Trademark of Radio Corporation of America.

MC7900C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.0 V – 18 V) (24 V)	V_{in}	-35 -40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	2.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	20	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	50	°C/W
T_C = +25°C	P_D	15	Watts
Derate above T_C = +95°C (See Figure 1)	$1/\theta_{JC}$	500	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	2.0	°C/W
Metal Package			
T_A = +25°C	P_D	2.5	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	28.6	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	35	°C/W
T_C = +25°C	P_D	15	Watts
Derate above T_C = +65°C	$1/\theta_{JC}$	250	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	4.0	°C/W
Storage Junction Temperature Range	T_{stg}	-20 to +150	°C
Operating Junction Temperature Range	T_J	0 to +125	°C

MC7902C ELECTRICAL CHARACTERISTICS (V_{in} = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-1.92	-2.00	-2.08	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	8.0	20	
-8.0 Vdc ≥ V_{in} ≥ -12 Vdc		–	4.0	10	
(T_J = +25°C, I_O = 500 mA)					
-7.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	18	40	
-8.0 Vdc ≥ V_{in} ≥ -12 Vdc		–	8.0	20	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	70	120	
250 mA ≤ I_O ≤ 750 mA		–	20	60	
Output Voltage -7.0 Vdc ≥ V_{in} ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-1.90	–	-2.10	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
-7.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_{in}-V_O \rvert$	–	3.5	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7905C ELECTRICAL CHARACTERISTICS (V_{in} = -10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.8	-5.0	-5.2	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	7.0	50	
-8.0 Vdc ≥ V_{in} ≥ -12 Vdc		–	2.0	25	
(T_J = +25°C, I_O = 500 mA)					
-7.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	35	100	
-8.0 Vdc ≥ V_{in} ≥ -12 Vdc		–	8.0	50	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	11	100	
250 mA ≤ I_O ≤ 750 mA		–	4.0	50	
Output Voltage	V_O	-4.75	–	-5.25	Vdc
-7.0 Vdc ≥ V_{in} ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
-7.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential	$\lvert V_{in}-V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	TCV_O	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7905.2C ELECTRICAL CHARACTERISTICS (V_{in} = -10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.0	-5.2	-5.4	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.2 Vdc ≥ V_{in} ≥ -25 Vdc		–	8.0	52	
-8.0 Vdc ≥ V_{in} ≥ -12 Vdc		–	2.2	27	
(T_J = +25°C, I_O = 500 mA)					
-7.2 Vdc ≥ V_{in} ≥ -25 Vdc		–	37	105	
-8.0 Vdc ≥ V_{in} ≥ -12 Vdc		–	8.5	52	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	12	105	
250 mA ≤ I_O ≤ 750 mA		–	4.5	52	
Output Voltage	V_O	-4.94	–	-5.46	Vdc
-7.2 Vdc ≥ V_{in} ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
-7.2 Vdc ≥ V_{in} ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	42	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	68	–	dB
Input-Output Voltage Differential	$\lvert V_{in}-V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	TCV_O	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7906C ELECTRICAL CHARACTERISTICS (V_{in} = -11 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.75	-6.0	-6.25	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-8.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	9.0	60	
-9.0 Vdc ≥ V_{in} ≥ -13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 500 mA)					
-8.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	43	120	
-9.0 Vdc ≥ V_{in} ≥ -13 Vdc		–	10	60	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	13	120	
250 mA ≤ I_O ≤ 750 mA		–	5.0	60	
Output Voltage	V_O	-5.7	–	-6.3	Vdc
-8.0 Vdc ≥ V_{in} ≥ -21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)					
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
-8.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	45	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential	$\lvert V_{in}-V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	TCV_O	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$					

MC7908C ELECTRICAL CHARACTERISTICS (V_{in} = -14 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-7.7	-8.0	-8.3	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-10.5 Vdc ≥ V_{in} ≥ -25 Vdc		–	12	80	
-11 Vdc ≥ V_{in} ≥ -17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 500 mA)					
-10.5 Vdc ≥ V_{in} ≥ -25 Vdc		–	50	160	
-11 Vdc ≥ V_{in} ≥ -17 Vdc		–	22	80	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	26	160	
250 mA ≤ I_O ≤ 750 mA		–	9.0	80	
Output Voltage	V_O	-7.6	–	-8.4	Vdc
-10.5 Vdc ≥ V_{in} ≥ -23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
-10.5 Vdc ≥ V_{in} ≥ -25 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	52	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential	$\lvert V_{in}-V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	TCV_O	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$					

MC7912C ELECTRICAL CHARACTERISTICS (V_{in} = -19 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.5	-12	-12.5	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-14.5 Vdc ≥ V_{in} ≥ -30 Vdc		–	13	120	
-16 Vdc ≥ V_{in} ≥ -22 Vdc		–	6.0	60	
(T_J = +25°C, I_O = 500 mA)					
-14.5 Vdc ≥ V_{in} ≥ -30 Vdc		–	55	240	
-16 Vdc ≥ V_{in} ≥ -22 Vdc		–	24	120	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	46	240	
250 mA ≤ I_O ≤ 750 mA		–	17	120	
Output Voltage	V_O	-11.4	–	-12.6	Vdc
-14.5 Vdc ≥ V_{in} ≥ -27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change	ΔI_B				mA
-14.5 Vdc ≥ V_{in} ≥ -30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	75	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential	$\lvert V_{in}-V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	TCV_O	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7915C ELECTRICAL CHARACTERISTICS (V_{in} = -23 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.4	-15	-15.6	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-17.5 Vdc ≥ V_{in} ≥ -30 Vdc		–	14	150	
-20 Vdc ≥ V_{in} ≥ -26 Vdc		–	6.0	75	
(T_J = +25°C, I_O = 500 mA)					
-17.5 Vdc ≥ V_{in} ≥ -30 Vdc		–	57	300	
-20 Vdc ≥ V_{in} ≥ -26 Vdc		–	27	150	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	68	300	
250 mA ≤ I_O ≤ 750 mA		–	25	150	
Output Voltage	V_O	-14.25	–	-15.75	Vdc
-17.5 Vdc ≥ V_{in} ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change	ΔI_B				mA
-17.5 Vdc ≥ V_{in} ≥ -30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential	$\lvert V_{in}-V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	TCV_O	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7918C ELECTRICAL CHARACTERISTICS (V_{in} = -27 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-17.3	-18	-18.7	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-21 Vdc ≥ V_{in} ≥ -33 Vdc		–	25	180	
-24 Vdc ≥ V_{in} ≥ -30 Vdc		–	10	90	
(T_J = +25°C, I_O = 500 mA)					
-21 Vdc ≥ V_{in} ≥ -33 Vdc		–	90	360	
-24 Vdc ≥ V_{in} ≥ -30 Vdc		–	50	180	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A		–	110	360	
250 mA ≤ I_O ≤ 750 mA		–	55	180	
Output Voltage	V_O	-17.1	–	-18.9	Vdc
-21 Vdc ≥ V_{in} ≥ -33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Quiescent Current (T_J = +25°C)	I_B	–	4.5	8.0	mA
Quiescent Current Change	ΔI_B				mA
-21 Vdc ≥ V_{in} ≥ -33 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	110	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential	$\lvert V_{in}-V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	TCV_O	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7924C ELECTRICAL CHARACTERISTICS (V_{in} = -33 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-23	-24	-25	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
-27 Vdc ≥ V_{in} ≥ -38 Vdc		–	31	240	
-30 Vdc ≥ V_{in} ≥ -36 Vdc		–	14	120	
(T_J = +25°C, I_O = 500 mA)					
-27 Vdc ≥ V_{in} ≥ -38 Vdc		–	118	480	
-30 Vdc ≥ V_{in} ≥ -36 Vdc		–	70	240	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A		–	150	480	
250 mA ≤ I_O ≤ 750 mA		–	85	240	
Output Voltage	V_O	-22.8	–	-25.2	Vdc
-27 Vdc ≥ V_{in} ≥ -38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Quiescent Current (T_J = +25°C)	I_B	–	4.6	8.0	mA
Quiescent Current Change	ΔI_B				mA
-27 Vdc ≥ V_{in} ≥ -38 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	170	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential	$\lvert V_{in}-V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	TCV_O	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (CASE 199-04)

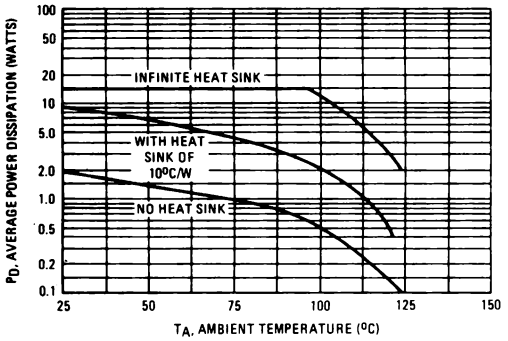


FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3 TYPE PACKAGE)

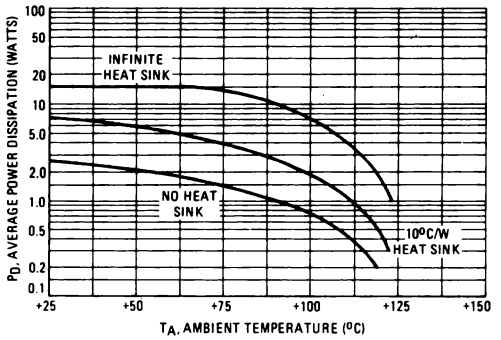


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

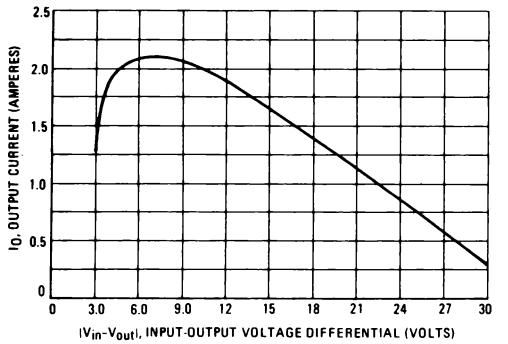


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

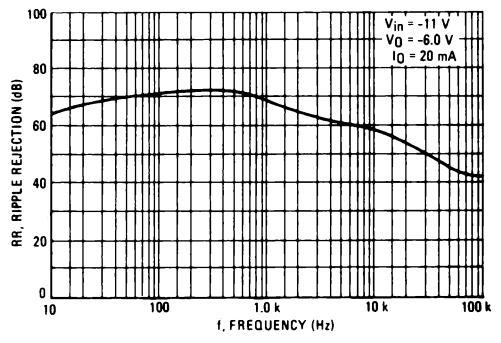


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

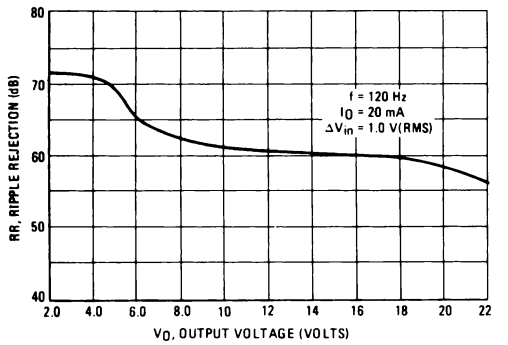
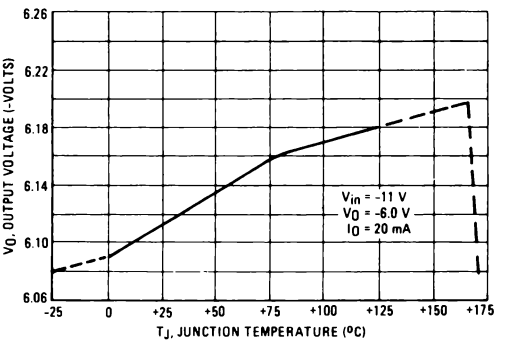
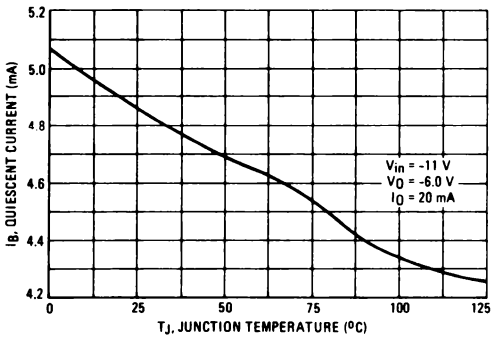


FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

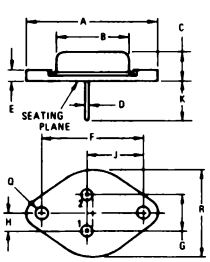
Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

OUTLINE DIMENSIONS



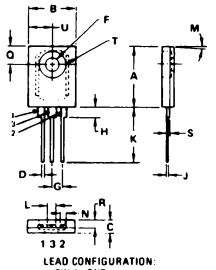
LEAD CONFIGURATION:
PIN 1. GND
2. OUTPUT
CASE: INPUT

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Weight = 5.9 grams

Leads are gold plated copper cored Kovar*
*Trademark of Westinghouse Electric Corporation
Ground connected to case.
Metal Package
CASE 11-01
K SUFFIX



LEAD CONFIGURATION:
PIN 1. GND
PIN 2. OUTPUT
PIN 3. INPUT

Heat sink surface connected to pin 3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0.152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

NOTES
1. DIM "G" IS TO CENTER OF LEADS
PLASTIC PACKAGE
CASE 199-04
P SUFFIX
Weight = 2.48 grams

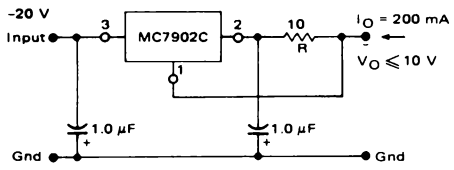
APPLICATIONS INFORMATION

Design Considerations

The MC7900C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. If an aluminum electrolytic capacitor is used, its value should be 1.0 μF or larger. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 – CURRENT REGULATOR

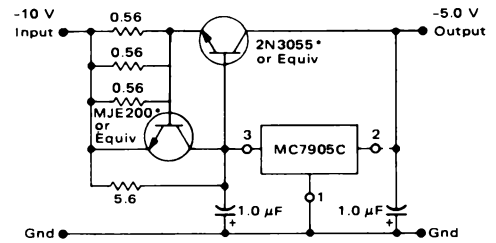


The MC7902, -2.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{2\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 2.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

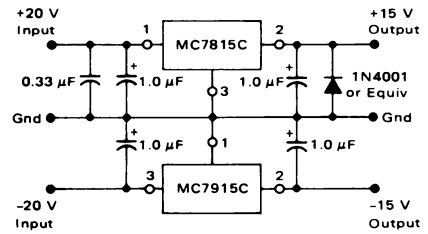
FIGURE 9 – CURRENT BOOST REGULATOR
(-5.0 V @ 4.0 A, with 5.0 A current limiting)



*Mounted on common heat sink, Motorola MS-10 or equivalent.

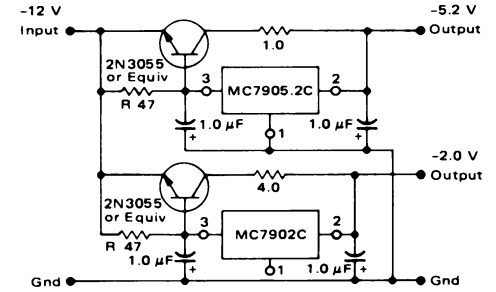
When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

FIGURE 10 – OPERATIONAL AMPLIFIER SUPPLY
(±15 V @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems.

FIGURE 11 – TYPICAL MECL SYSTEM POWER SUPPLY
(-5.2 V @ 4.0 A and -2.0 V @ 2.0 A; for PC Board)



When current-boost power transistors are used, 47-ohm base-to-emitter resistors (R) must be used to bypass the quiescent current at no load. These resistors, in conjunction with the V_{BE} of the NPN transistors, determine when the pass transistors begin conducting. The 1-ohm and 4-ohm dropping resistors were chosen to reduce the power dissipated in the boost transistors but still leave at least 2.0 V across these devices for good regulation.

Advance Information

1024-BIT STATIC RANDOM ACCESS MEMORY

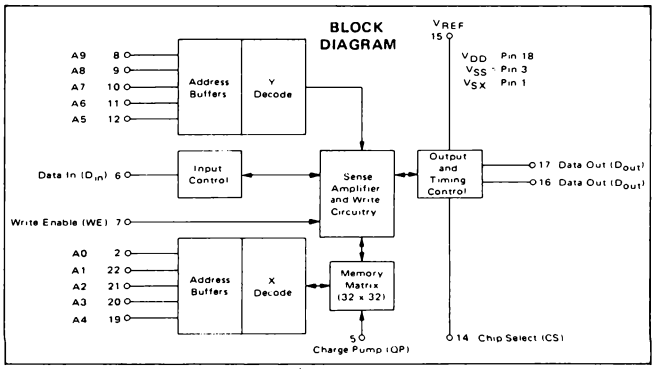
The MCM7001 memory is fabricated with high-density, highly-reliable, N-channel, metal-gate MOS technology. The device utilizes low-voltage inputs (except Chip Select) and on-chip address registers, and has low power consumption. Low output capacitance and a Chip Select input allow memory expansion without speed degradation. The charge pump technique is used to automatically refresh all memory cells without affecting memory access.

- Organized as 1024 Words of 1 Bit
- Access Time = 55 ns Maximum (MCM7001L)
  = 75 ns Maximum (MCM7001L-1)
- Cycle Time = 180 ns Minimum
- Static Operation
- Low Power Dissipation
  640 μW/Bit Maximum Active
  60 μW/Bit Maximum Standby
- Differential Current Sinking Outputs
- On-Chip Address Registers
- Low-Voltage Inputs (Except Chip Select)
- Chip Select for Memory Expansion
- MCM7001L Direct Replacement for AMS7001

ABSOLUTE MAXIMUM RATINGS (See Note 1)
(Referenced to most negative supply voltage, V_{SX}.)

Rating	Symbol	Value	Unit
Supply Voltages	V_{DD}	-0.5 to +25	Vdc
	V_{REF}	-0.5 to +25	Vdc
	V_{SS}	-0.5 to +10	Vdc
Input and Output Voltages	V_{in},V_{out}	-0.5 to +25	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

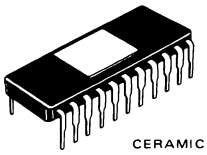


This is advance information and specifications are subject to change without notice.

MOS

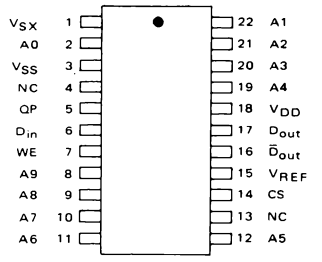
(N-CHANNEL, METAL GATE)

1024-BIT STATIC RANDOM ACCESS MEMORY



CERAMIC PACKAGE
CASE 694

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Full Temperature Range)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltages	V_{DD}	14.7	15.5	16.3	V
	V_{REF}	7.0	7.5	8.0	V
	V_{SS}	0	0	0	V
	V_{SX}	-2.7	-3.0	-3.3	V
Logic Levels					
Input High Voltage (A_n, D_{in}, WE)	V_{IH}	4.0	–	5.5	V
Input Low Voltage (A_n, D_{in}, WE)	V_{IL}	-1.0	–	0.8	V
Chip Select High Voltage	V_{CSH}	V_{DD} -1.0	–	V_{DD} + 1.0	V
Chip Select Low Voltage	V_{CSL}	-1.0	–	1.0	V
Charge Pump High Voltage	V_{PH}	8.0	–	12	V
Charge Pump Low Voltage	V_{PL}	V_{SX} - 2.0	–	V_{SX} - 5.0	V
Timing (t_{CSr} and t_{CSf} = 10 ns)					
Chip Select On Time	T_{CS}	80	–	500	ns
Chip Select Off Time	$T_{\overline{CS}}$	100	–	–	ns
Chip Select Rise Time	t_{CSr}	5.0	–	40	ns
Chip Select Fall Time	t_{CSf}	5.0	–	40	ns
Cycle Time (Read or Write)	T_{cyc}	180	–	–	ns
Setup Time (A_n, D_{in}, WE)	T_{IS}	0	–	–	ns
Address Hold Time	T_{Ah}	40	–	–	ns
Write Valid Time	T_{Wv}	T_{CS} + T_{IS}	–	–	ns
Data In Valid Time	T_{Dv}	T_{CS} + T_{IS}	–	–	ns
Charge Pump Input Frequency (See Figure 1 for waveform characteristics)	f_{pump}	200	–	1000	kHz

DC ELECTRICAL CHARACTERISTICS (Full operating voltage and temperature range unless otherwise noted.)

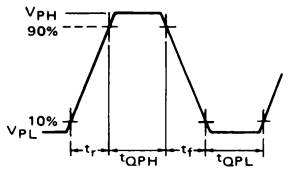
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (A_n, D_{in}) (V_I = 4.0 V, V_{CS} = 0)	I_{IH}	–	0.4	1.0	mA
Write Enable Input Current (V_I = 4.0 V, V_{CS} = 0)	I_{WH}	–	–	10	μA
Chip Select Input Current, Average Over Operating Mode (V_A = V_{IL}, T_{cyc} = 180 ns)	I_{CSH}	–	–	10	mA
Chip Select Low Input Current (V_A = 4.0 V, V_{CS} = 0)	I_{CSL}	–	–	-11	mA
Differential Output Sink Current	I_{DO}	0.2	–	–	mA
Supply Current, Unselected Mode (V_{CS} = 0)	I_{SXU}	–	–	-100	μA
	I_{DDU}	–	2.5	3.0	mA
	I_{REFU}	–	–	60	μA
Supply Current, Operating Mode (T_{cyc} = 180 ns)	I_{SX}	–	–	-400	μA
	I_{DD}	–	25	35	mA
	I_{REF}	–	6.0	10	mA

AC ELECTRICAL CHARACTERISTICS (Full operating voltage and temperature range unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Access Time (I_{DO} = 0.2 mA, t_{CSr} = 10 ns, R_L = 100 ohms, C_L = 50 pF, Figure 2)	MCM7001L	T_{acc}	–	45	55	ns
	MCM7001L-1		–	–	75	ns
Address Capacitance*	V_I = V_{SS}, f = 1.0 MHz	C_A	–	5.0	6.0	pF
Write Enable Capacitance*		C_{WE}	–	5.0	6.0	pF
Data In Capacitance*		C_{DI}	–	5.0	6.0	pF
Charge Pump Input Capacitance*		C_{QP}	–	65	80	pF
Data Output Capacitance* (V_{CS} = V_{SS}, f = 1.0 MHz)		C_{DO}	–	–	6.0	pF
Effective Chip Select Capacitance (Figure 3)*		$C_{CS(EFF)}$	–	65	80	pF

*Capacitances are periodically sampled rather than 100% tested.

FIGURE 1 – CHARGE PUMP OSCILLATOR WAVEFORM REQUIREMENTS



Characteristic	Symbol	Min	Max	Unit
Rise Time	t_r	100	–	ns
High Level Dwell Time	t_{QPH}	100	–	ns
Fall Time	t_f	100	500	ns
Low Level Dwell Time	t_{QPL}	100	–	ns

FIGURE 2 – MEMORY TIMING DIAGRAM

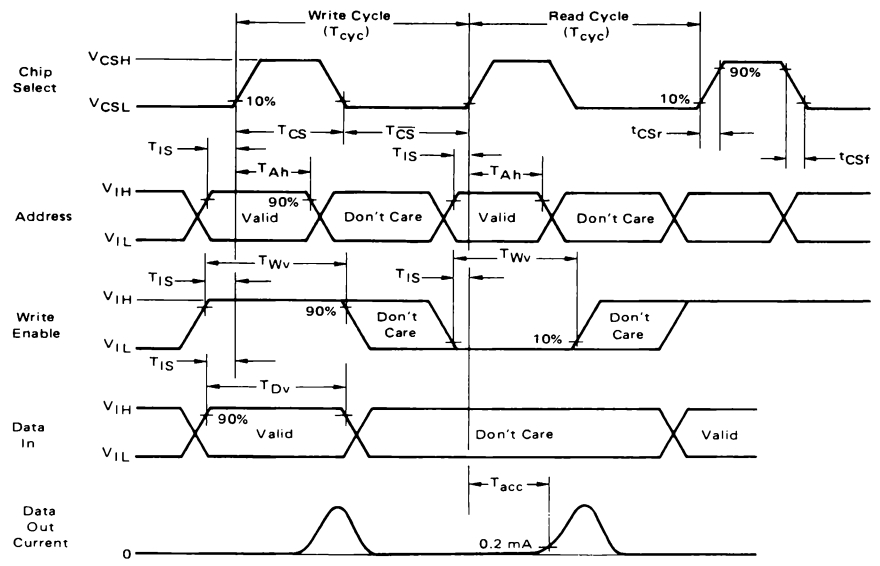
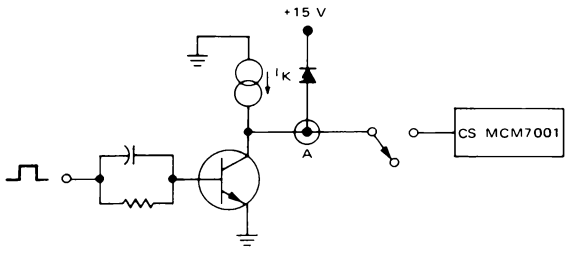


FIGURE 3 – MEASUREMENT OF EFFECTIVE CHIP SELECT CAPACITANCE



The effective capacitance of the Chip Select input terminal $C_{CS(EFF)}$ is determined by measuring the difference in rise times of the voltage waveforms at point A with and without the Chip Select terminal connected.

$C_{CS(EFF)} \approx K \Delta t_r$

where $K = I_K/V$ (15 V)

$I_K \geqslant 100$ mA.

APPLICATIONS INFORMATION

The MCM7001 static random access memory provides the high speed and low power required for large memory systems. Only a single clock input is required with this memory. Data Output and its complement can be detected using a differential amplifier for sensing. The outputs of several devices can be wire-ORed with no significant degradation in speed.

Operation of the Charge Pump input is shown by the basic memory cell in Figure 4. Assume the arbitrary state of Q3 "on" and Q4 "off". In this state, C1 is charged and C2 discharged. Over a period of time, C1 will lose its charge due to leakage unless the charge is replenished. By driving the charge pump devices with an oscillator of the correct frequency, the memory will be refreshed.

The Charge Pump oscillator must operate within the frequency and amplitude limits listed under Recommended Operating Conditions. These frequencies and voltages provide low power consumption and static operation. The Charge Pump input does not need to be operated synchronously with any other input signal and has no effect on access time.

The Charge Pump oscillator of Figure 5 uses the Charge Pump input capacitance of the MCM7001 as part of a Colpitts-type oscillator. The oscillator can drive from 8 to 64 devices in a push-pull manner by connecting half of the RAM charge pump inputs to each end of the inductor. The zener and resistor are used to control the oscillator amplitude. The positive peak of the swing is determined by the zener voltage and the negative swing is 0.6 V below the V_{SS} voltage (-5.2 V). It is important that the maximum voltage rating of the MC14049 feedback buffer be observed.

Frequency of oscillation is dependent on the number of RAMs to be driven. The inductance is determined as

$$L \approx \frac{1}{10\, n\, C_{QP}\, f^2}$$

where n = total number of RAMs,
C_{QP} = charge pump capacitance, and
f = frequency.

Typical values will therefore be

Frequency	Number of RAMs	Inductance (L)
800 kHz	8	300 μH
	16	150 μH
	32	75 μH
	64	37 μH

Figures 6 and 7 show possible interface circuits for driving the address and data inputs of the MCM7001. The MC10125 MECL-to-MTTL translator is used if ECL logic is being interfaced to the memory card; if TTL is being used, an MTTL gate such as the MC3000 can be used. The pullup resistor at the output is needed to meet the required "1" level. The extra drive circuitry shown in Figure 6 is required to drive the normally heavy load of the address inputs (approximately 400 pF for a 32 k x 2 or 4 k x 16 memory board). This will maintain a fast access measured from the address input. The circuit of Figure 6 should also be used to drive the write enable input. The circuit of Figure 7 is capable of driving the four data inputs required in a 4 k x 16 memory board, but the circuit of Figure 6 should be used if more than four devices are being driven. Interface circuits MC3459 (Quad TTL-to-N channel) and MC10177 (triple ECL-to-N channel) will be available in 1974 for system use.

The Chip Select driver must charge its capacitive load with the specified rise time to maintain the fast access time. In addition, it must supply a small dc current in both the High and Low states. Figure 8 shows a MECL interface circuit which will drive a load of eight devices (one byte) to the required level of V_{DD} ± 1.0 volt. MECL level translation is first made through a differential amplifier. The amplifier turns on a switch which in turn drives the output transistors. In order to minimize rise time and overshoot, proper line integrity and termination must be used. Some rules for achieving this are found in the **MECL System Design Handbook.**

Another approach for driving the Chip Select inputs, although slower, is to use the MC10127 dual clock driver for MECL systems or the MMH0026 for TTL systems.

The data outputs, D_{out} and $\overline{D}_{out}$, are current sinking terminals and require pullup resistors. If a logic "1" exists in the addressed location, $\overline{D}_{out}$ will sink a minimum current of 200 μA toward ground, while D_{out} is a high impedance. If a logic "0" exists, $\overline{D}_{out}$ will be a high impedance and D_{out} sinks current. The output data from the memory then is referenced around the supply voltage connected to the pullup resistors.

A simple, fast, and reliable output sensing circuit is shown in Figure 9. The PNP transistors are used to translate the memory outputs to a voltage that can be detected by the differential amplifier. The 3.6 k-ohm resistors are used as 2.0 mA current sources that produce a 1.0-volt drop across the 510 ohm resistors. The voltage at the data outputs (D_{out} and $\overline{D}_{out}$) is fixed at one diode drop above V_{REF}. When one data output sinks current, less current is available across the 510 ohm resistor and a lesser voltage appears at that terminal of the differential amplifier (e.g., Δ200 μA = Δ100 mV; Δ400 μA = Δ200 mV). For a fast MECL system the MC1650 dual comparator should be used (propagation delay = 3.5 ns). It requires a low overdrive, low input switching current and has a latch for data storage. If desired, the MC10115 quad line receiver could also be used for the differential amplifier. The MC10125 quad MECL-to-MTTL translator, which has a propagation delay of 5.0 ns can be used as the differential amplifier with TTL systems. If longer delays are tolerable, the MC1514, MC3450 or MC75107 can be used.

A major advantage of the technique used in Figure 9 is that up to 16 memory outputs can be tied together without appreciably affecting the access time.

FIGURE 4 – BASIC MEMORY CELL

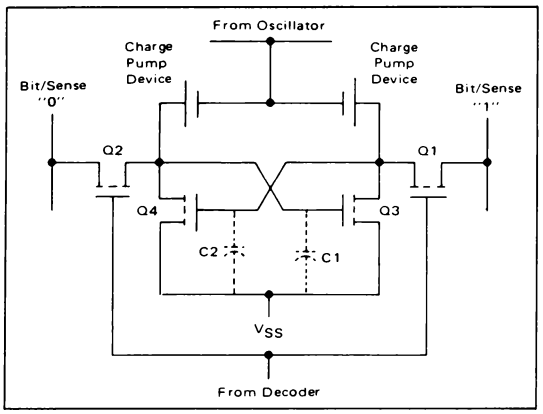


FIGURE 5 – CHARGE PUMP OSCILLATOR

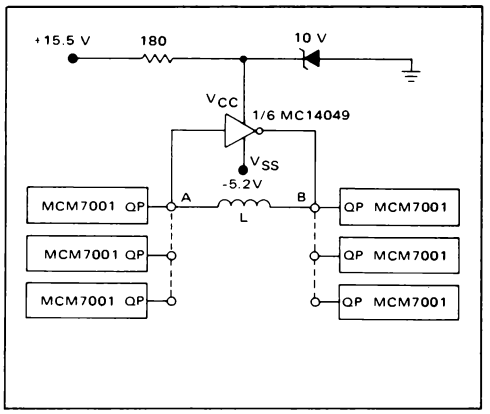
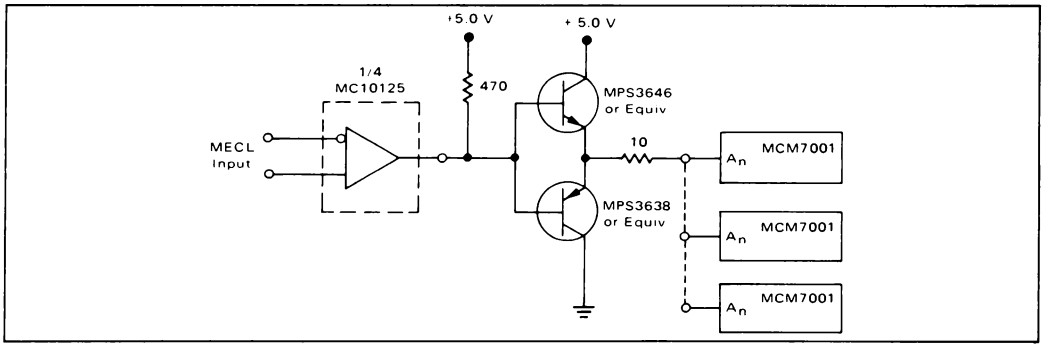


FIGURE 6 – ADDRESS INPUT DRIVER

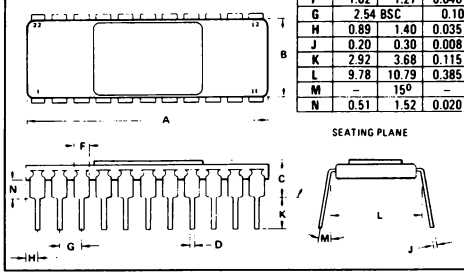


PACKAGE DIMENSIONS

CASE 694

NOTES
1. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) FROM PACKAGE BASE)
2. LEADS WITHIN 0.005 RADIUM OF TRUE POSITION (TP) AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
3. LEAD No. 1 IDENTIFIED BY NOTCH ON TOP

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	26.54	27.94	1.045	1.100
B	9.02	9.40	0.355	0.370
C	3.30	4.06	0.130	0.160
D	0.38	0.53	0.015	0.021
F	1.02	1.27	0.040	0.050
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	9.78	10.79	0.385	0.425
M	–	15°	–	15°
N	0.51	1.52	0.020	0.060



CASE 677

The MCM7001 may be packaged in Case 677 (white ceramic) rather than in Case 694. If your application requires precise tolerances, consult the factory.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	27.05	27.94	1.065	1.100
C	2.16	3.68	0.085	0.145
D	0.43	0.58	0.017	0.023
F	1.02 REF		0.040 REF	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	9.65	10.67	0.380	0.420
M	–	7°	–	7°
N	0.64	1.27	0.025	0.050

NOTES
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

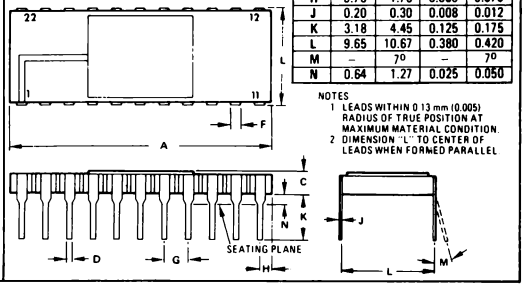


FIGURE 7 – DATA INPUT DRIVER

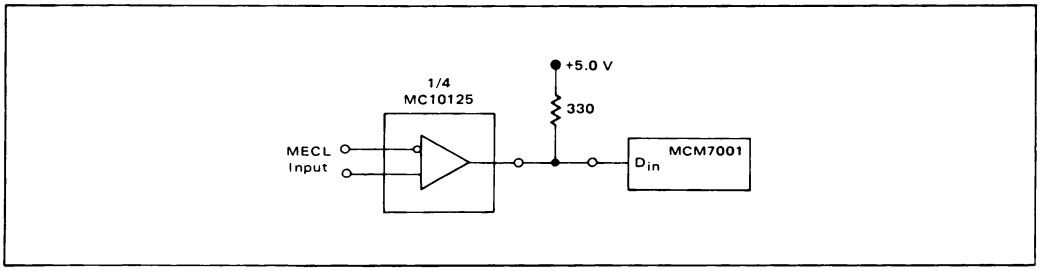


FIGURE 8 – CHIP SELECT DRIVER

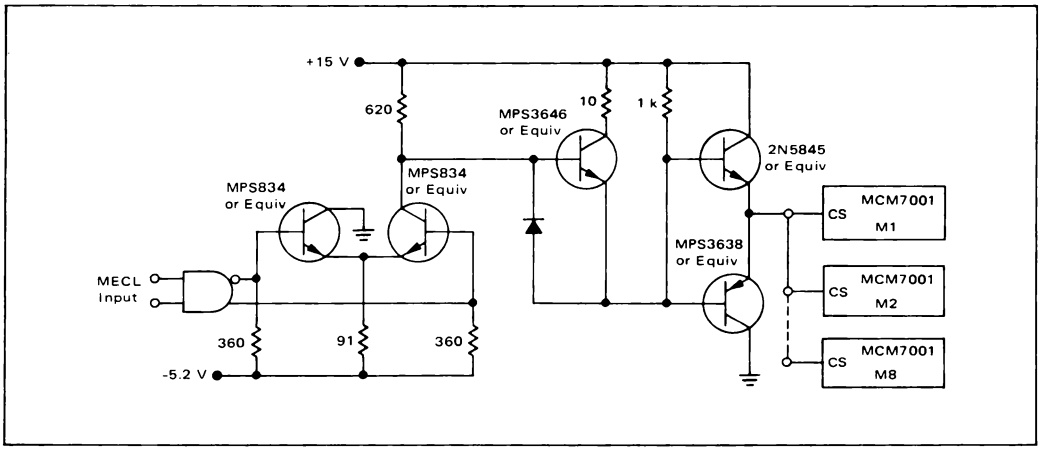
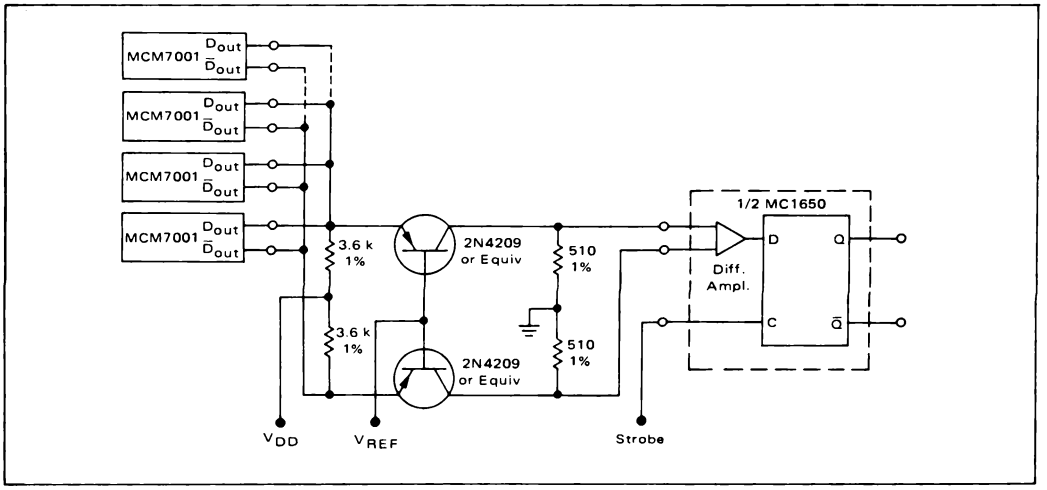


FIGURE 9 – OUTPUT SENSE CIRCUIT



MECL

PHASE-LOCKED LOOP COMPONENTS

LOGIC PRODUCTS
for
PHASE-LOCKED LOOP APPLICATIONS

Motorola offers the designer a choice of specially designed integrated circuits for performing phase-locked loop functions: phase detection, frequency division, filtering, and voltage-controlled signal generation. In addition, the choice of circuits permits the designer to select TTL circuits *where speed is not critical (<25 MHz), or ECL circuits where high speed is required. The MC12000* series circuits will operate at either +5.0 V or -5.2 V, and translators are included where needed so that all functions are compatible.

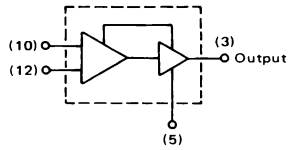
FUNCTION	DEVICE NUMBER	LOGIC FAMILY	SPEED (TYP) MHz	CHARACTERISTICS
Phase-Frequency Detector	MC4044	MTTL	10	Consists of two digital phase detectors, charge pump, and amplifier
Phase-Frequency Detector	MC12040	MECL	80	Operation similar to MC4044
Voltage-Controlled Multivibrator	MC4024	MTTL	25	Contains two independent voltage-controlled multivibrators with output buffers
Voltage-Controlled Oscillator	MC1648	MECL	200	Emitter-coupled oscillator with output levels compatible with MECL III
Digital Mixer/Translator	MC12000	MECL	250	A "D" flip-flop with MTTL to MECL and MECL to MTTL translators
Two-Modulus Prescaler	MC12012	MECL	200	÷2, ÷5/÷6, ÷10/÷11, ÷10/÷12
Two-Modulus Prescaler	MC12013*	MECL	400	÷10/11, ÷10/12
Counter Control Logic	MC12014	MTTL	25	Used with MC12012 and MC74416 to accomplish direct high-frequency programming
Crystal Oscillator	MC12060	MECL	100 kHz to 2 MHz	Provide complementary sine wave, complementary ECL logic levels, and single ended TTL logic level outputs.
Crystal Oscillator	MC12061	MECL	2 MHz to 20 MHz	Frequency stability provided by external crystal (fundamental, series mode).
COUNTER OPTIONS				
Programmable Divide By N Decade Counter	MC74416 (MC4016)	MTTL	10**	÷0 through 9
Two Programmable Divide By N Counters	MC74417	MTTL	10**	÷0-1, ÷0 through 4
Programmable Divide By N Hexadecimal Counter	MC74418 (MC4018)	MTTL	10**	÷0 through 15
Two Programmable Divide By N Counters	MC74419	MTTL	10**	÷0 through 3
Universal Counter	MC4023	MTTL	30	÷2 through 12 except 7 and 11
Decade Counter	MC7490	MTTL	20	÷2, ÷5, ÷10
Bi-Quinary Counter	MC1678	MECL	325	÷2, ÷5, ÷10
UHF Prescaler Type D Flip-Flop	MC1690	MECL	500	÷2
Universal Hexadecimal Counter	MC10136	MECL	150***	0 to 15
Universal BCD Decade Counter	MC10137	MECL	150***	÷10
Decade Counter-Divider	MC14017	McMOS	5	÷10
Binary Counter	MC14040	McMOS	10	$\div(2^{12})$
BCD Presettable Up/Down Counter	MC14510	McMOS	6	÷10
Binary Up/Down Counter	MC14516	McMOS	6	÷16
Dual BCD Up Counter	MC14518	McMOS	6	÷10 or ÷100
Dual Binary Up Counter	MC14520	McMOS	6	÷16 or ÷256
BCD Programmable Divide By N	MC14522	McMOS	5	÷0 through 9
Binary Programmable Divide By N	MC14526	McMOS	5	÷0 through 15

(*) To be announced.
(**) Speed can be increased to 25 MHz (typ) when used with MC12014
(***) When used as a prescaler, it is possible to extend the input frequency to over 200 MHz with the MC10231; to 300 MHz with the MC1670; or to over 500 MHz with the MC1690

CONTENTS

NOTE: For individual data sheets on other products listed in the selector guide write –
Motorola Semiconductor Products Inc.
P.O. Box 20924
Phoenix, Arizona 85036

MC1648



Numbers in parenthesis denote pin number for F package (Case 607) L package (Case 632), and P package (Case 646).

Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

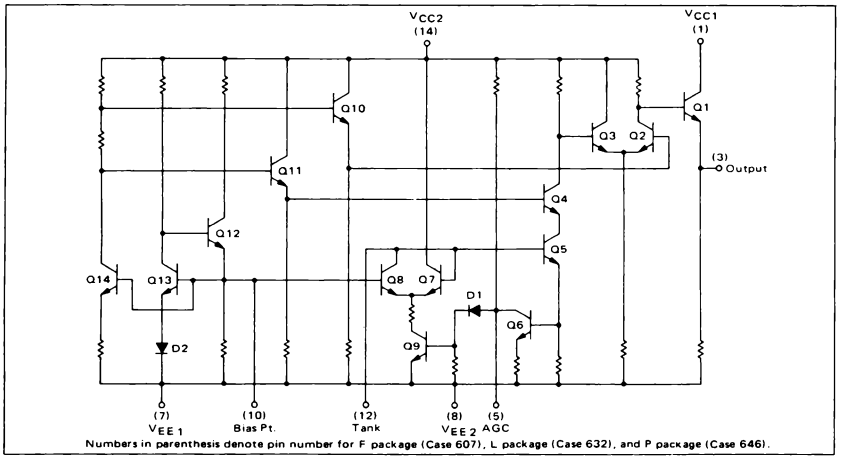
The MC1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with MECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity (See Figure 2).

The MC1648 may be operated from a +5.0 Vdc supply or a -5.2 Vdc supply, depending upon system requirements.

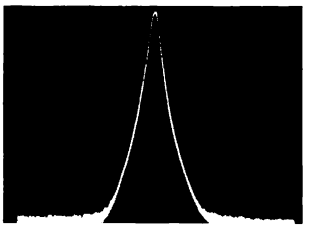
SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

FIGURE 1 – CIRCUIT SCHEMATIC

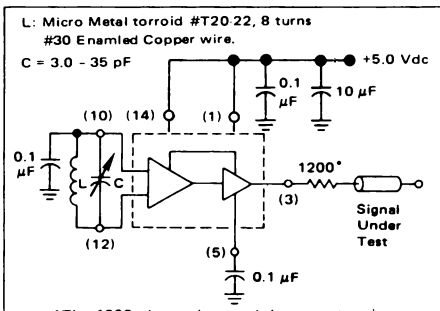


Numbers in parenthesis denote pin number for F package (Case 607), L package (Case 632), and P package (Case 646).

FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT



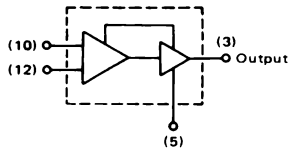
B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



*The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts



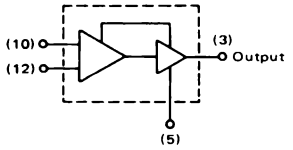
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	mAdc I_L
-30°C	+1.960	+1.410	5.0	-5.0
+25°C	+1.800	+1.300	5.0	-5.0
+85°C	+1.680	+1.180	5.0	-5.0

Characteristic	Symbol	Pin Under Test	MC1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	I_L	V_{EE} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	40	—	—	mAdc	—	—	1, 14	—	7, 8
Logic "1" Output Voltage	$V_{O:H}$	3	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	—	12	1, 14	3	7, 8
Logic "0" Output Voltage	V_{OL}	3	3.16	3.40	3.20	3.43	3.23	3.46	Vdc	12	—	1, 14	3	7, 8
Bias Voltage	V_{Bias}*	10	1.51	1.86	1.40	1.70	1.28	1.58	Vdc	—	—	1, 14	—	7, 8
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	—	— —	—	500 —	—	— —	mV	See Figure 3	—	1, 14	3	7, 8
Output Duty Cycle	V_{DC}	3	—	— —	—	50 —	—	— —	%	See Figure 3	—	1, 14	3	7, 8
Oscillation Frequency	f_{max}	—	—	— —	200	225 —	—	— —	MHz	See Figure 3	—	1, 14	3	7, 8

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 volts

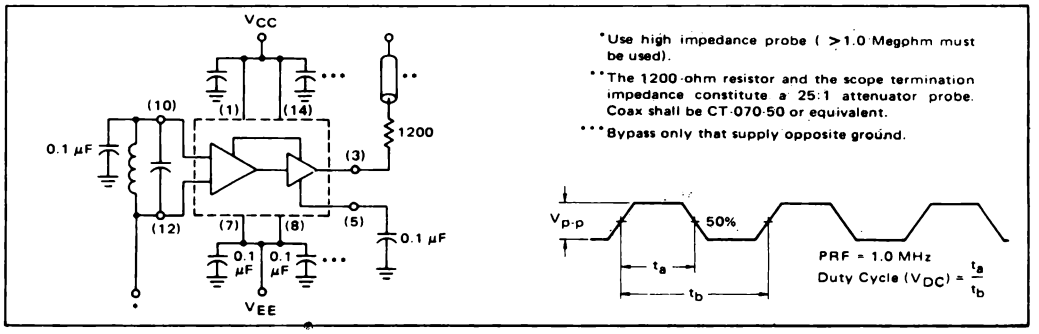


@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	mAdc I_L
-30°C	-3.300	-3.800	-5.2	-5.0
+25°C	-3.400	-3.900	-5.2	-5.0
+85°C	-3.500	-4.000	-5.2	-5.0

Characteristic	Symbol	Pin Under Test	MC1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	41	—	—	mAdc	—	—	7, 8	—	1, 14
Logic "1" Output Voltage	V_{OH}	3	-1.045	-0.815	-0.960	-0.750	-0.890	-0.650	Vdc	—	12	7, 8	3	1, 14
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	12	—	7, 8	3	1, 14
Bias Voltage	V_{Bias}*	10	-3.690	-3.340	-3.800	-3.500	-3.920	-3.620	Vdc	—	—	7, 8	—	1, 14
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	—	— —	—	500 —	—	— —	mV	See Figure 3	—	7, 8	3	1, 14
Output Duty Cycle	V_{DC}	3	—	— —	—	50 —	—	— —	%	See Figure 3	—	7, 8	3	1, 14
Oscillation Frequency	f_{max}	—	—	— —	200	225 —	—	— —	MHz	See Figure 3	—	7, 8	3	1, 14

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS



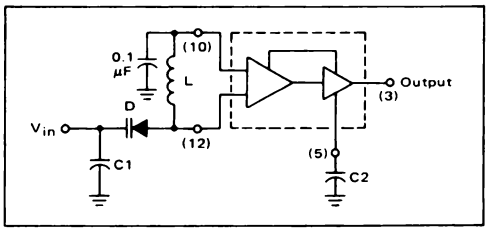
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q7 to the collector of Q8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (Q4) is used to translate from the emitter follower (Q5) to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provide a highly buffered output which produces a square wave. Transistors Q10 thru Q14 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

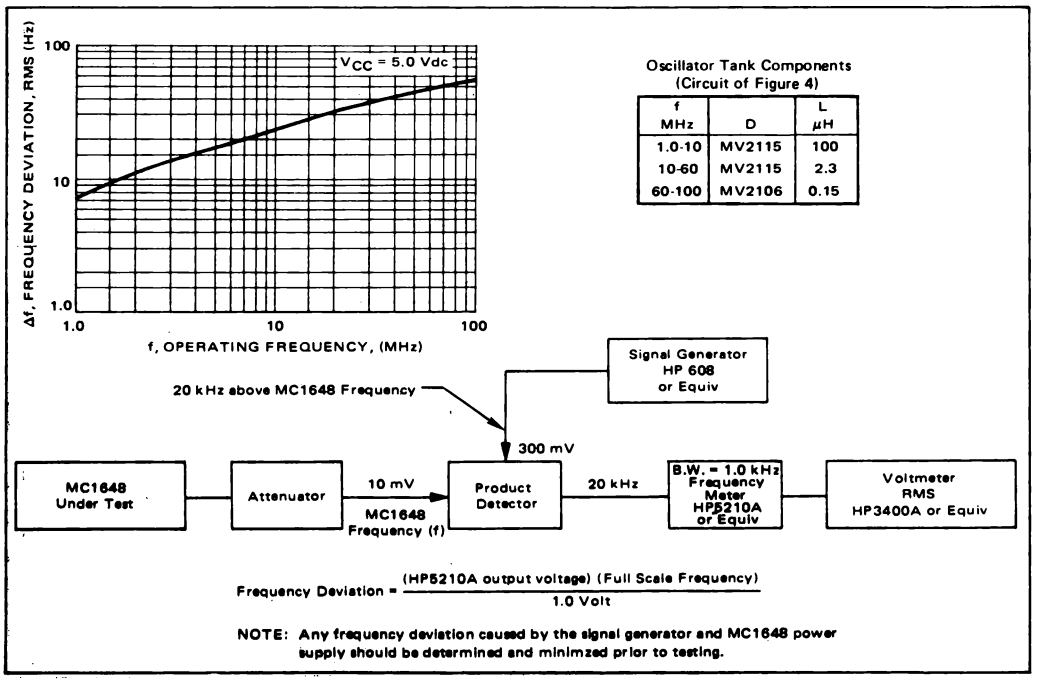
When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

FIGURE 4 – THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 5 – NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



NOTE: Any frequency deviation caused by the signal generator and MC1648 power supply should be determined and minimzed prior to testing.

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^oC$

FIGURE 6

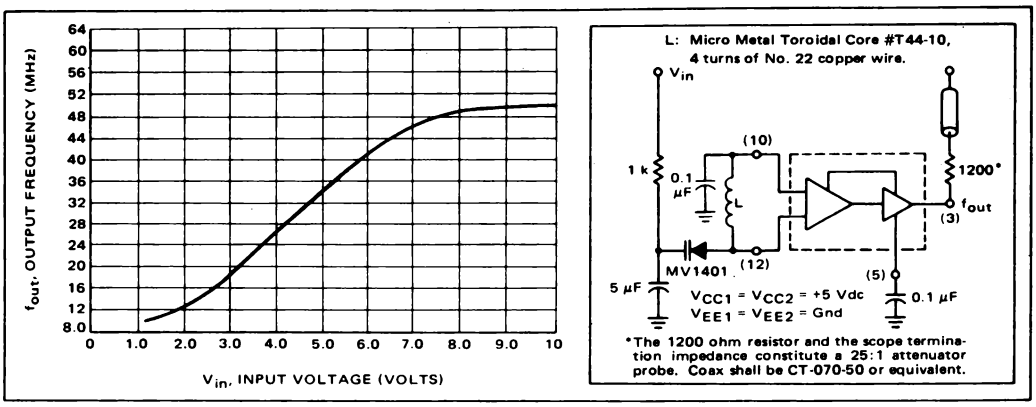


FIGURE 7

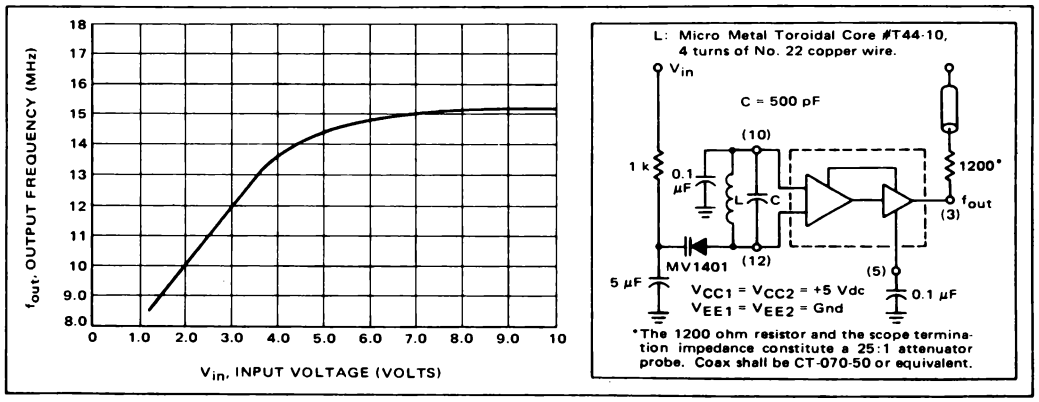
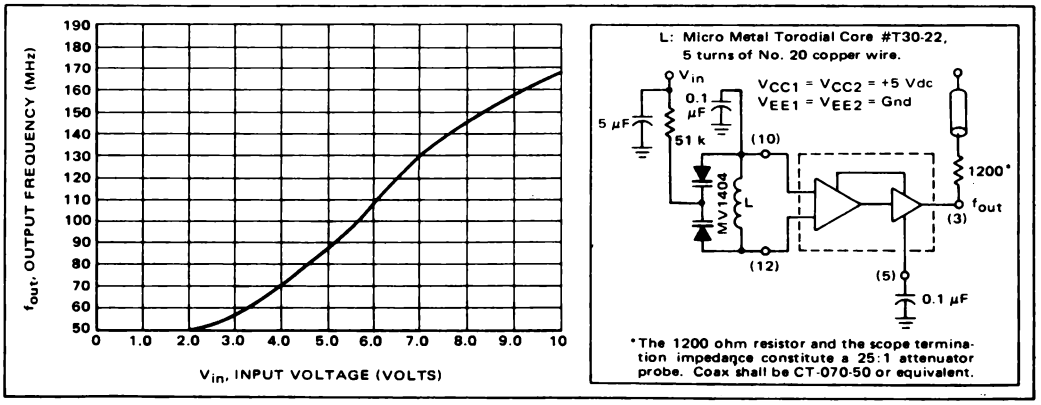


FIGURE 8



Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7 and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (pluse the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\ (max) + C_S}}{\sqrt{C_D\ (min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L\ (C_D\ (max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins (see Figure 2).

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the MC1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and land-mobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translation, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lock-up. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked-loops and digital frequency synthesizers, see Motorola Application Notes AN-532A, AN-535, AN-553, AN-564, and AN-594.

FIGURE 9 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION

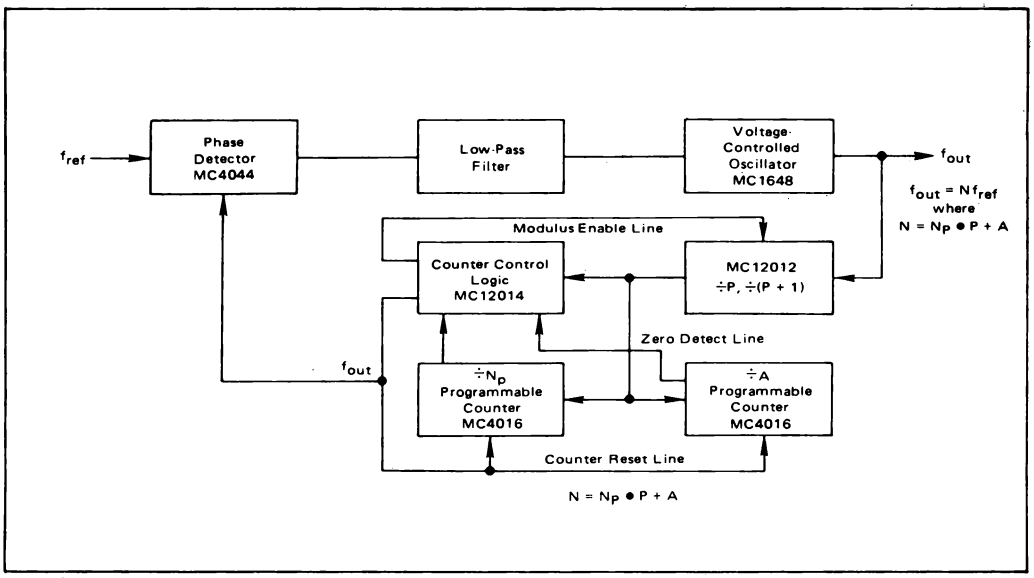


Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

Figure 12 shows the MC1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 – METHOD OF OBTAINING A SINE-WAVE OUTPUT

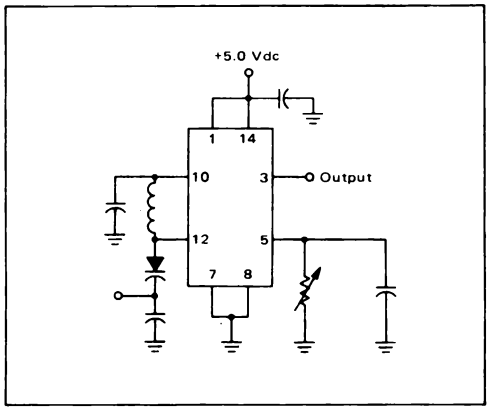


FIGURE 11 – METHOD OF EXTENDING THE USEFUL RANGE OF THE MC1648 (SQUARE WAVE OUTPUT)

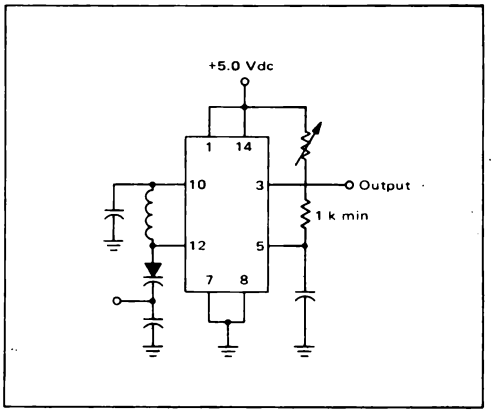


FIGURE 12 — CIRCUIT SCHEMATIC USED FOR COLLECTOR OUTPUT OPERATION

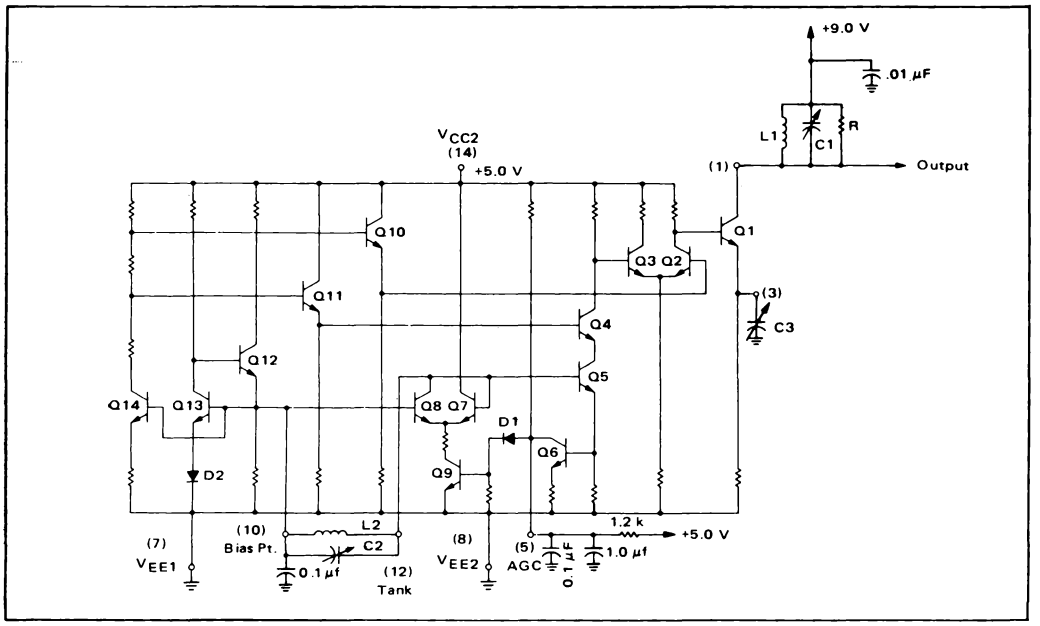


FIGURE 13 – POWER OUTPUT versus COLLECTOR LOAD

See test circuit, Figure 12, f = 100 MHz
C3 = 3.0 - 35 pF
Collector Tank
L1 = 0.22 μH C1 = 1.0 - 7.0 pF
R = 50 Ω - 10 kΩ
Rp of L1 and C1 = 11 kΩ @ 100 MHz Resonance
Oscillator Tank
L2 = 4 turns #20 AWG 3/16" ID
C2 = 1.0 - 7.0 pF

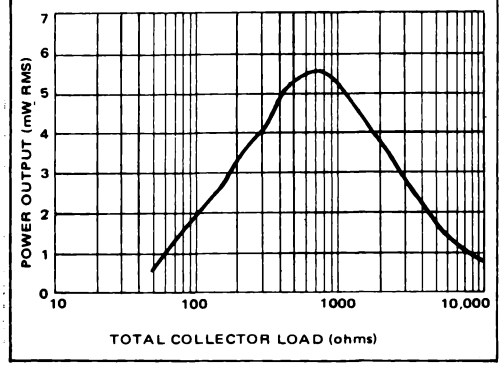
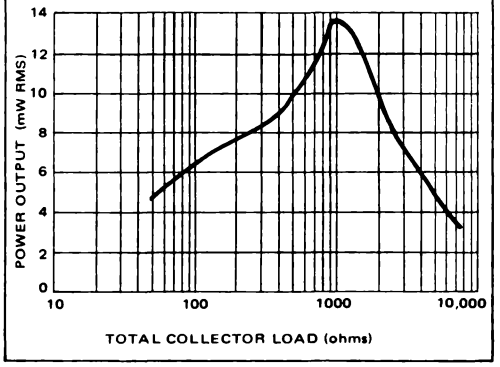


FIGURE 14 – POWER OUTPUT versus COLLECTOR LOAD

See test circuit, Figure 12, f = 10 MHz
C3 = 470 pF
Collector Tank
L1 = 2.7 μH C1 = 24 - 200 pF
R = 50 Ω - 10 kΩ
Rp of L1 and C1 = 6.8 kΩ @ 10 MHz Resonance
Oscillator Tank
L2 = 2.7 μH
C2 = 16 - 150 pF



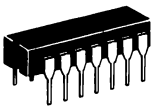
DIGITAL
MIXER/TRANSLATOR

MC12000

DIGITAL MIXER/TRANSLATOR
(D Flip-Flop w/Translator)

The MC12000 is intended for use as a digital mixer in phase-locked loop frequency synthesizers and other applications where a MECL "D" flip-flop with translators is required. Toggle frequency is typically 250 MHz. MTTL to MECL and MECL to MTTL translators are provided to facilitate interfacing with MECL or MTTL circuits.

The MC12000 is designed to operate from a single power supply of either +5.0 Vdc or -5.2 Vdc.



CERAMIC PACKAGE
CASE 632

Pin Assignment

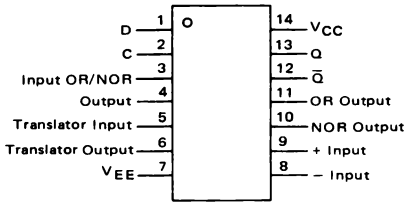
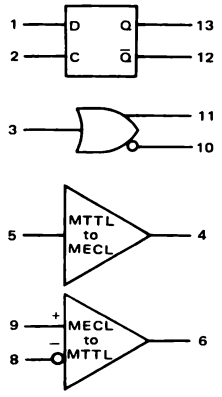
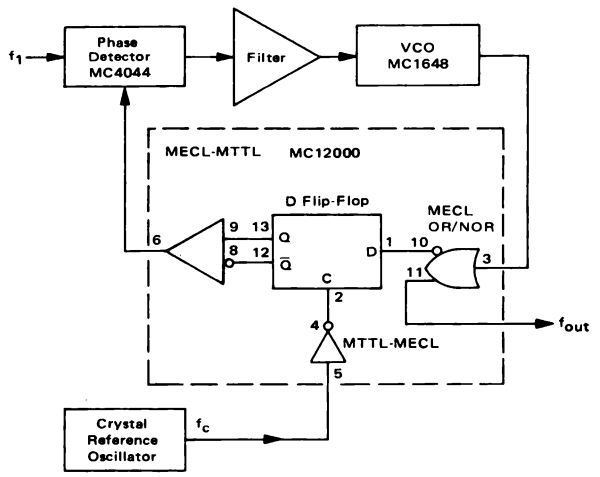


FIGURE 1 – LOGIC DIAGRAM



D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

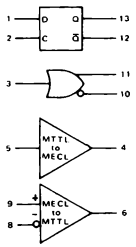
FIGURE 2 – TYPICAL DIGITAL MIXER



Note: All MECL outputs have 510-ohm internal pulldown resistors.

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 V



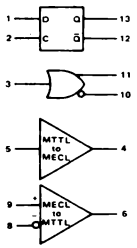
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES													
	Volts											mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHA}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
0°C	+4.160	+3.130	+3.855	+3.510	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
25°C	+4.190	+3.150	+3.895	+3.525	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
75°C	+4.280	+3.170	+3.955	+3.550	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	MC12000 0°C Max	MC12000 +25°C Min	MC12000 +25°C Typ	MC12000 +25°C Max	MC12000 +75°C Min	MC12000 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7	–	–	–	85	–	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	14	–	–	–	7
Input Current	I_{INH1}	1	–	–	–	–	200	–	–	μAdc	1	2	–	–	–	–	–	–	–	–	14	–	–	–	7
		2	–	–	–	–	200	–	–		2	1	–	–	–	–	–	–	–	–		–	–	–	
		3	–	–	–	–	200	–	–		3	–	–	–	–	–	–	–	–	–		–	–	–	
	I_{INH2}	5	–	4.0	–	–	40	–	40		–	–	–	–	–	–	5	–	–	–		–	–	–	
	I_{INH3}	8	–	–	3.8	–	6.5	–	–	mAdc	9	8	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	3.8	–	6.5	–	–		9	8	–	–	–	–	–	–	–	–		–	–	–	
	I_{INL1} (Leakage Current)	1	–	–	–	–	2.0	–	–	μAdc	–	–	–	–	–	–	–	–	–	–	14	–	–	–	1,7
		2	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–		–	–	–	2,7
		3	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–		–	–	–	3,7
	I_{INL2}	5	–	-1.6	–	–	-1.6	–	-1.6	mAdc	–	–	–	–	5	–	–	–	–	–		–	–	–	7
	I_{INL3}	8	–	–	3.8	–	6.5	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	2.0	–	4.0	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH1}	4	4.000	4.160	4.040	–	4.190	4.100	4.280	Vdc	–	–	–	–	–	5	–	–	–	–	14	4	–	–	7
		10				–					–	3	–	–	–	–	–	–	–	–		10	–	–	
		11				–					3	–	–	–	–	–	–	–	–	–		11	–	–	
		12†				–					–	1	–	–	–	–	–	–	–	–		12	–	–	
		13†				–					1	–	–	–	–	–	–	–	–	–		13	–	–	
	V_{OH2}	6	2.400	–	2.400	–	–	2.400	–	Vdc	9	8	–	–	–	–	–	–	–	–	14	–	–	6	7
Logic "0" Output Voltage	V_{OL1}	4	3.130	3.370	3.150	–	3.380	3.170	3.410	Vdc	–	–	–	–	5	–	–	–	–	–	14	4	–	–	7
		10				–					3	–	–	–	–	–	–	–	–	–		10	–	–	
		11				–					–	3	–	–	–	–	–	–	–	–		11	–	–	
		12†				–					1	–	–	–	–	–	–	–	–	–		12	–	–	
		13†				–					–	1	–	–	–	–	–	–	–	–		13	–	–	
	V_{OL2}	6	–	0.500	–	–	0.500	–	0.500	Vdc	8	9	–	–	–	–	–	–	–	–	14	–	6	–	7
Logic "1" Threshold Voltage	V_{OHA}	4	3.980	–	4.020	–	–	4.080	–	Vdc	–	–	–	–	–	–	–	–	–	5	14	4	–	–	7
		10		–		–	–		–		–	–	–	3	–	–	–	–	–	–		10	–	–	
		11		–		–	–		–		–	–	3	–	–	–	–	–	–	–		11	–	–	
		12†		–		–	–		–		–	–	–	1	–	–	–	–	–	–		12	–	–	
		13†		–		–	–		–		–	–	1	–	–	–	–	–	–	–		13	–	–	
Logic "0" Threshold Voltage	V_{OLA}	4	–	3.390	–	–	3.400	–	3.430	Vdc	–	–	–	–	–	–	–	–	–	5	14	4	–	–	7
		10	–		–	–		–			–	–	3	–	–	–	–	–	–	–		10	–	–	
		11	–		–	–		–			–	–	–	3	–	–	–	–	–	–		11	–	–	
		12†	–		–	–		–			–	–	1	–	–	–	–	–	–	–		12	–	–	
		13†	–		–	–		–			–	–	–	1	–	–	–	–	–	–		13	–	–	
Short Circuit Current	I_{SC}	6	-20	-65	-20	–	-65	-20	-65	mAdc	9	8	–	–	–	–	–	–	–	–	14	–	–	–	6,7

†Output Level to be measured after a clock pulse has been applied to the C input (pin 2) V_{IHmax} / V_{ILmin}

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 V



@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	(mA) I_L	I_{OL}	I_{OH}
0°C	-0.840	-1.870	-1.145	-1.490	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6
25°C	-0.810	-1.850	-1.105	-1.475	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6
75°C	-0.720	-1.830	-1.045	-1.450	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6

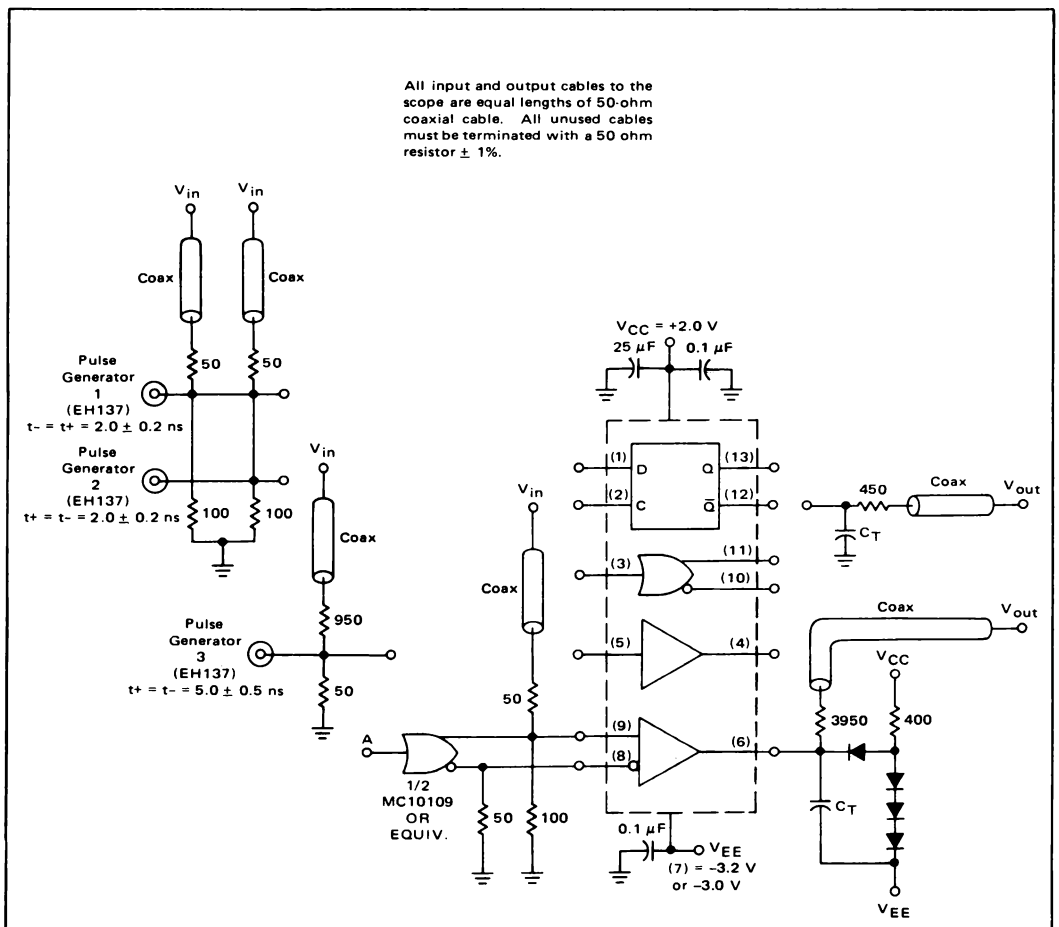
Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	0°C Max	25°C Min	25°C Typ	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	V_{CC} Gnd
Power Supply Drain Current	I_E	7	–	–	–	90	–	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	7	–	–	–	14
Input Current	I_{INH1}	1	–	–	–	–	200	–	–	µAdc	1	2	–	–	–	–	–	–	–	–	7	–	–	–	14
		2	–	–	–	–	200	–	–		2	1	–	–	–	–	–	–	–	–		–	–	–	
		3	–	–	–	–	200	–	–		3	–	–	–	–	–	–	–	–	–		–	–	–	
	I_{INH2}	5	–	40	–	–	40	–	40		–	–	–	–	–	–	5	–	–	–		–	–	–	
	I_{INH3}	8	–	–	3.8	–	6.5	–	–	mAdc	9	8	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	3.8	–	6.5	–	–		9	8	–	–	–	–	–	–	–	–		–	–	–	
	I_{INL1}	1	–	–	–	–	2.0	–	–	µAdc	–	–	–	–	–	–	–	–	–	–	1,7	–	–	–	14
	(Leakage	2	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–	2,7	–	–	–	
	Current)	3	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–	3,7	–	–	–	
	I_{INL2}	5	–	-1.6	–	–	-1.6	–	-1.6	mAdc	–	–	–	–	5	–	–	–	–	–	7	–	–	–	
	I_{INL3}	8	–	–	3.8	–	6.5	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	2.0	–	4.0	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH1}	4	-1.000	-0.840	-0.960	–	-0.810	-0.900	-0.720	Vdc	–	–	–	–	–	5	–	–	–	–	7	4	–	–	14
		10				–					–	3	–	–	–	–	–	–	–	–		10	–	–	
		11				–					3	–	–	–	–	–	–	–	–	–		11	–	–	
		12†				–					–	1	–	–	–	–	–	–	–	–		12	–	–	
		13†				–					1	–	–	–	–	–	–	–	–	–		13	–	–	
	V_{OH2}	6	-2.800	–	-2.800	–	–	-2.800	–	Vdc	9	8	–	–	–	–	–	–	–	–	7	–	–	6	14
Logic "0" Output Voltage	V_{OL1}	4	-1.870	-1.635	-1.850	–	-1.620	-1.830	-1.595	Vdc	–	–	–	–	5	–	–	–	–	–	7	4	–	–	14
		10				–					3	–	–	–	–	–	–	–	–	–		10	–	–	
		11				–					–	3	–	–	–	–	–	–	–	–		11	–	–	
		12†				–					1	–	–	–	–	–	–	–	–	–		12	–	–	
		13†				–					–	1	–	–	–	–	–	–	–	–		13	–	–	
	V_{OL2}	6	–	-4.700	–	–	-4.700	–	-4.700	Vdc	8	9	–	–	–	–	–	–	–	–	7	–	6	–	14
Logic "1" Threshold Voltage	V_{OHA}	4	-1.020	–	-0.980	–	–	-0.920	–	Vdc	–	–	–	–	–	–	–	–	5	–	7	4	–	–	14
		10		–		–	–		–		–	–	–	3	–	–	–	–	–	–		10	–	–	
		11		–		–	–		–		–	–	3	–	–	–	–	–	–	–		11	–	–	
		12†		–		–	–		–		–	–	–	1	–	–	–	–	–	–		12	–	–	
		13†		–		–	–		–		–	–	1	–	–	–	–	–	–	–		13	–	–	
Logic "0" Threshold Voltage	V_{OLA}	4	–	-1.615	–	–	-1.600	–	-1.575	Vdc	–	–	–	–	–	–	–	–	–	5	7	4	–	–	14
		10	–		–	–		–			–	–	3	–	–	–	–	–	–	–		10	–	–	
		11	–		–	–		–			–	–	–	3	–	–	–	–	–	–		11	–	–	
		12†	–		–	–		–			–	–	1	–	–	–	–	–	–	–		12	–	–	
		13†	–		–	–		–			–	–	–	1	–	–	–	–	–	–		13	–	–	
Short Circuit Current	I_{SC}	6	-20	-65	-20	–	-65	-20	-65	mAdc	9	8	–	–	–	–	–	–	–	–	6,7	–	–	–	14

†Output Level to be measured after a clock pulse has been applied to the C input (pin 2) V_{IHmax} V_{ILmin}

AC ELECTRICAL CHARACTERISTICS

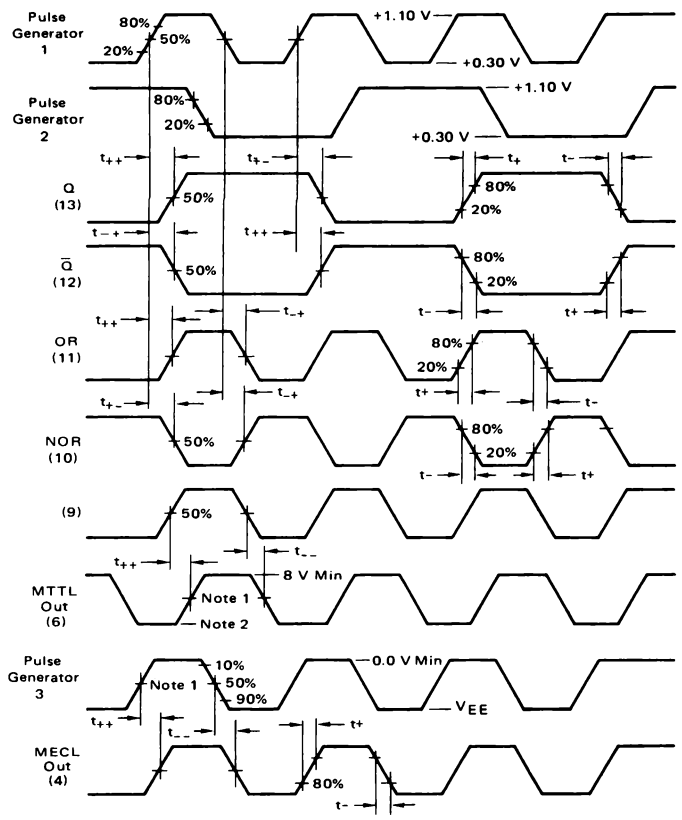
Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	Pulse Out	V_{EE} -3.2 V or -3.0 V	V_{CC} +2.0 V
Propagation Delay (See Figure 4)	t_{2+13+}	2,13	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	13	7	14
	t_{2+13-}	2,13	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	13	7	14
	t_{2+12+}	2,12	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	12	7	14
	t_{2+12-}	2,12	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	12	7	14
	t_{3+11+}	3,11	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	11	7	14
	t_{3-11-}	3,11	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	11	7	14
	t_{3+10-}	3,10	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	10	7	14
	t_{3-10+}	3,10	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	10	7	14
	t_{5+4+}	5,4	–	–	2.0	3	5.0	–	–	ns	–	–	5	4	7	14
	t_{5-4-}	5,4	–	–	1.0	1.5	3.0	–	–	ns	–	–	5	4	7	14
	t_{9+6+}	9,6	–	–	4.0	8.0	12.0	–	–	ns	A	–	–	6	7	14
	t_{9-6-}	9,6	–	–	3.0	5.0	10.0	–	–	ns	A	–	–	6	7	14
Output Rise Time (See Figure 4)	t_{13+}	13	–	–	–	2.8	–	–	–	ns	2	1	–	13	7	14
	t_{12+}	12	–	–	–	2.8	–	–	–	ns	2	1	–	12	7	14
	t_{11+}	11	–	–	–	2.0	–	–	–	ns	3	–	–	11	7	14
	t_{10+}	10	–	–	–	2.0	–	–	–	ns	3	–	–	10	7	14
	t_{4+}	4	–	–	–	2.4	–	–	–	ns	–	–	5	4	7	14
Output Fall Time (See Figure 4)	t_{13-}	13	–	–	–	2.8	–	–	–	ns	2	1	–	13	7	14
	t_{12-}	12	–	–	–	2.8	–	–	–	ns	2	1	–	12	7	14
	t_{11-}	11	–	–	–	2.0	–	–	–	ns	3	–	–	11	7	14
	t_{10-}	10	–	–	–	2.0	–	–	–	ns	3	–	–	10	7	14
	t_{4-}	4	–	–	–	2.4	–	–	–	ns	–	–	5	4	7	14
Setup Time (See Figure 5)	$t_{setup"1"}$	13	–	–	–	0.2	–	–	–	ns	2	1	–	–	7	14
	$t_{setup"0"}$	13	–	–	–	0.7	–	–	–	ns	2	1	–	–	7	14
Hold Time (See Figure 5)	$t_{hold"1"}$	13	–	–	–	0.0	–	–	–	ns	2	1	–	–	7	14
	$t_{hold"0"}$	13	–	–	–	1.0	–	–	–	ns	2	1	–	–	7	14
Toggle Frequency (See Figure 6)	f_{tog}	13	–	–	–	250	–	–	–	MHz	–	–	–	–	7	14

FIGURE 3 – SWITCHING TIME TEST CIRCUIT



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 – AC TEST VOLTAGE WAVEFORMS



NOTES:
1. V_{EE} + 1.5 V
2. V_{EE} + 0.5 V max

FIGURE 5 – SETUP AND HOLD TIME WAVEFORMS (See Figure 3)

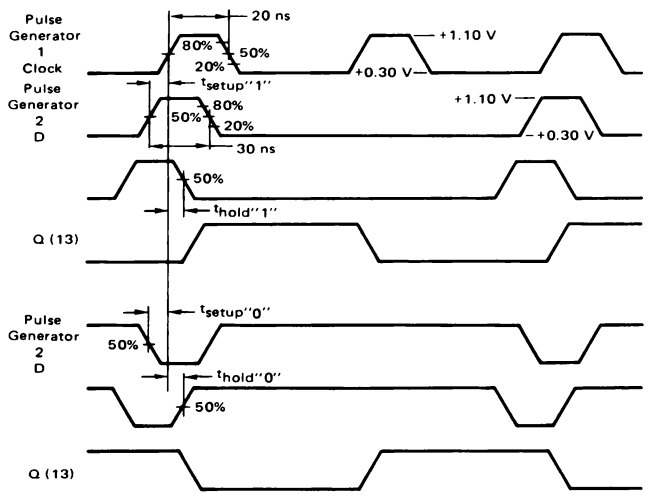
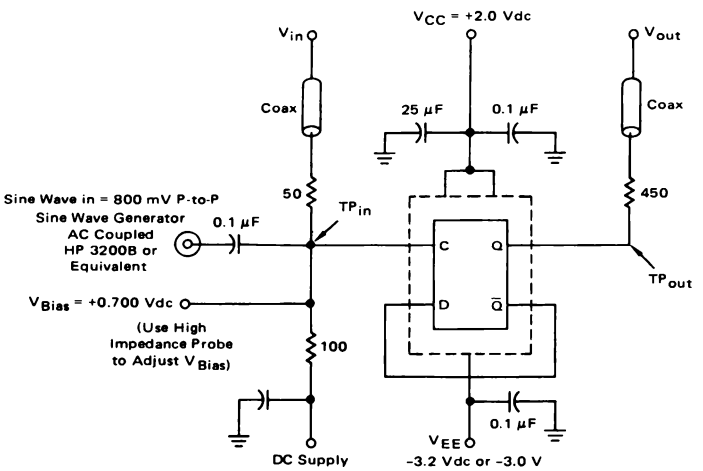


FIGURE 6 – TOGGLE FREQUENCY TEST CIRCUIT



The maximum Toggle Frequency of MC12000 has been exceeded when either:

1. The output Peak-to-Peak voltage swing falls below 600 mV

   or

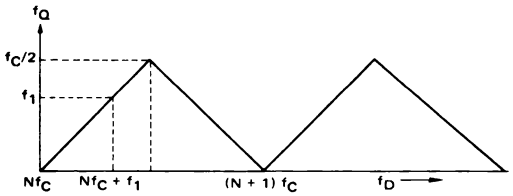
2. The devices cease to Toggle (divide by 2).

MC12000 DIGITAL MIXER

This device is a digital mixer designed to operate with logic levels at its input and output ports. In operation it is an MECL type "D" flip-flop with level translators to and from MTTL to accomodate most interfacing demands. Output frequency (f_Q) as a function of "D" and clock inputs is shown in Figure 7. It can be seen that either direct or harmonic mixing may be employed, that is, f_Q may be either the difference between f_D and f_C or the difference between f_D and the Nth harmonic of f_C.

One particular advantage of mixing in phase locked loops (PLL) is that lower frequencies may be generated for use in portions of the circuit where digital processing is done (with divide-by-P network and/or phase detector). Lower frequency operation often reduces overall system cost since a less expensive logic form may be utilized. However use of the mixing technique is not a panacea for all VHF applications and the design of such synthesizer systems must be approached with care.

FIGURE 7



Use of the MC12000 in a non-harmonic PLL is straightforward (Figure 8). Output frequency is the sum of both input quantities ($f_1 + f_C$) as long as f_1 is less than $f_C/2$ (See Figure 7), since f_Q can go no higher than that. Unless VCO output range is restricted somewhat there is a chance also that the loop may operate at the second harmonic of f_C. This problem is minimal in the loop of Figure 8, however, since the output frequency would have to vary more than 2:1.

Mixing is used because the digital phase detector has an upper frequency limit of about 10 MHz and many loops require direct locks at 20 MHz or more. Direct down-mixing does not change any loop characteristics except the sampling rate which restricts loop natural frequency to about $f_C/10$ in practical circuits. Although output frequency may be changed by varying either f_1 or f_C, the clock input is usually crystal controlled since it is of the same magnitude as f_D and more difficult to stabilize.

FIGURE 8

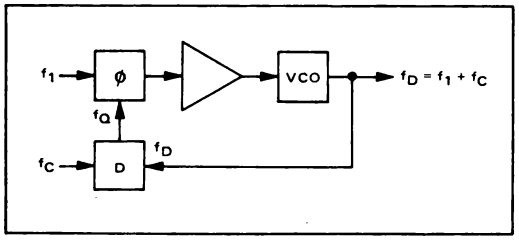
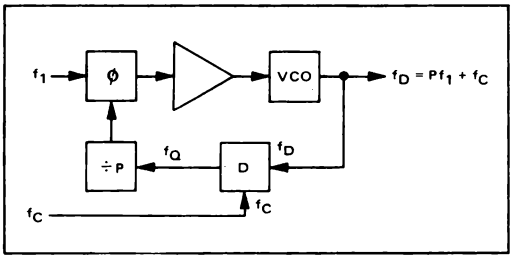


FIGURE 9



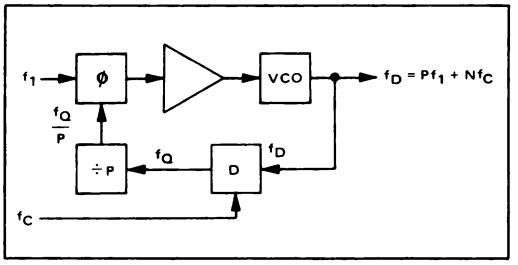
Combining a standard synthesis configuration with the mixer yields a circuit capable of high frequency operation at low cost (Figure 9), if the output frequency range is relatively small ($P_{max} - P_{min}$) $f_1 < f_C/2$. In fact the choice of harmonic or non-harmonic mixing is largely based on the availability of a suitable crystal or other reference source for f_C versus the needed frequency coverage. Considering all the restrictions on f_C, its value (and the maximum harmonic number N) are dictated by the following expressions:

$$N < \frac{f_{D(min)} - f_1}{2\,\Delta f_D} \qquad (1)$$

$$Nf_C = f_{D(min)} - f_1 \qquad (2)$$

where Δf_D = change in output frequency.

FIGURE 10



Using Equations (1) and (2) above the minimum value of f_C may be found for the circuit of Figure 10 and still get adequate frequency coverage. In this minimum configuration all necessary output frequencies may be generated by programming the "P" count string. But the divide number might bear no obvious relation to the output frequency such as often happens with non-mixing synthesizers.

DESIGN EXAMPLES

Example #1

Output Frequency: 48-54 MHz
Frequency Increments: 10 kHz
Using Equations (1) and (2), a minimum frequency (f_C) version can be designed:

$$f_1 = \text{increment} = 10\ \text{kHz}$$

$$N < \frac{48\ \text{MHz} - 10\ \text{kHz}}{2\ (54\text{-}48)\ \text{MHz}}$$

$$N < 4$$

Let N = 3

$$Nf_C = 47.99\ \text{MHz}$$

$$f_C = \frac{Nf_C}{N} = \frac{47.99}{3} = 15.99666\ \text{MHz}$$

$$f_C = 15.996666\ \text{MHz}$$

$$P_{min} = 1$$

$$P_{max} = \frac{\Delta f_D}{10\ \text{kHz}} + P_{min} \qquad (3)$$

$$P_{max} = \frac{6\ \text{MHz}}{10\ \text{kHz}} + P_{min}$$

$$P_{max} = 601$$

$$f_{Q(max)} = P_{max}\, f_1$$
$$= 6.01\ \text{MHz} \qquad (4)$$

Equation (4) above puts the divider string (divide-by-P) into a medium frequency situation where devices such as the MC4016/4316 may be utilized. Note that the divider number now indicates the channel selected rather than output frequency. That is, at f_D = 48.000 MHz, P = 1; at f_D = 54.000 MHz, P = 601.

If "proper" divide-by-P readings are desired for direct frequency readout a slight circuit modification is necessary. To enable a division at 48.000 MHz the first divide-by-P must be 100 rather than 1, and P_{max} would then be 700 to cover all 6 MHz. Recalculating $f_{Q(max)}$ from Equation 4 we still find that the 7 MHz maximum value allows use of the same components. The next question concerns the allowable range of f_Q in relation to f_C ($f_Q < f_C/2$). Since f_C is nearly 16 MHz, the range of f_Q can be contained. A cosmetic change to the most significant digit switch completes the design. Instead of reading 1 through 7 it must be modified to display 48 through 54.

Example #2

Output Frequency: 144-148 MHz
Frequency Increments: 10 kHz

$$f_1 = \text{increment} = 10\ \text{kHz}$$

$$N < \frac{144.00 - 0.01}{2\ (4)}$$

$$N < 18$$

Let N = 17

$$Nf_C = 144.00 - 0.01\ \text{MHz}$$
$$= 143.99$$

$$f_C = \frac{Nf_C}{N} = 8.470\ \text{MHz}$$

$$P_{min} = 1$$

$$P_{max} = \frac{4\ \text{MHz}}{10\ \text{kHz}} + 1$$
$$= 401$$

$$f_{Q(max)} = P_{max}\, f_1 = 4.01\ \text{MHz}$$

Maximum frequency seen by the divide-by-P chain is still well within the MC4016 rating.

When converting this synthesizer to one that reads frequency directly, a "1" is again added to the most significant digit (MSD). This results in a P_{min} of 100 to P_{max} of 500. In this example, however, $f_{Q(max)}$ is 5 MHz which easily exceeds $f_C/2$. To alleviate this difficulty, the "N" factor must be decreased in order to raise f_C to at least 10 MHz.

$$N < \frac{f_{D(min)} - f_1}{f_C}$$

Let f_C = 10 MHz

$$N < \sim 14.4$$

Let N = 14

$$Nf_C = 143.99\ \text{(from above)}$$

$$f_C = \frac{Nf_C}{N} = \frac{143.99}{14}$$

$$f_C = 10.28500\ \text{MHz} \qquad (5)$$

VCO RANGE RESTRICTIONS

As in all harmonically locked PLL's, it is possible for the loop to lock on the wrong harmonic if there is too wide a range in the VCO. This situation is shown in Figure 11 where the possible false lock areas are indicated near the (N - 1) and (N + 1) harmonic points. The problem of VCO restraint however is more than just making sure that output frequency f_D isn't able to go to B or A' (the closest false lock points). Actual operating limits are C and C', symmetrically placed frequencies corresponding to $f_{D(min)}$ about Nf_C and $f_{D(max)}$ about $(Nf+1/2)\ f_C$. If the VCO drops below C while the feedback counter is at P_{min} the phase detector will try to push f_D even lower, toward the stable condition at A (Figure 12). Likewise, at C' (when $P = P_{max}$) the tendency is for the loop to accelerate toward lockup at B' (Figure 13). When C or C' are exceeded the loop will "hang up" and not attain the proper lock.

FIGURE 11

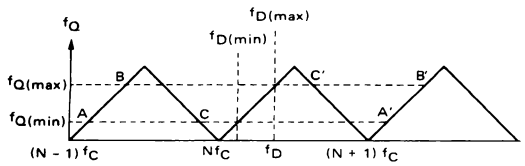


FIGURE 12

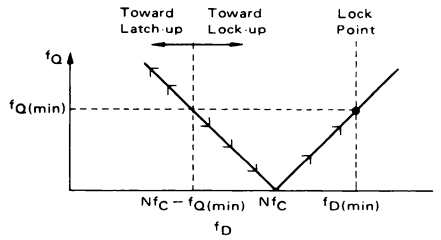
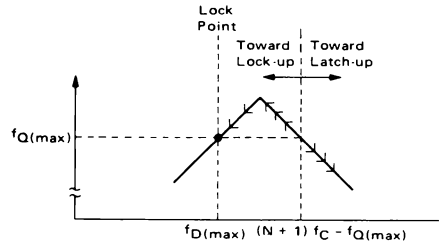
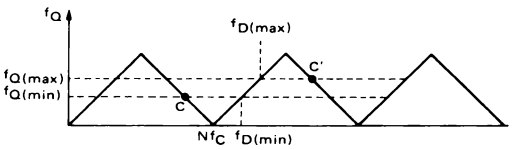


FIGURE 13



The VCO frequency constraints may be quite severe if the minimum f_C formulation is followed and the Nth harmonic is quite high. Where VCO constraint may pose a problem, decrease N below the maximum indicated by Equation (1) until sufficient room is generated by placing the operating range of f_Q on only a small part of the f_D slope (Figure 14). Note that f_C goes up as we approach the more idealized case (Equation 5).

FIGURE 14



The most likely reasons for a "latched up" state in a harmonic loop are turn-on transients and loop overshoot when changing frequency abruptly from one end of the range to the other.

SUMMARY OF SYNTHESIS PROCEDURE

1. Compute harmonic number N

$$N < \frac{f_{D(min)} - f_1}{2\,\Delta f_D}$$

where Δf_D = change in output frequency
f_1 = channel spacing

2. Compute minimum mixing frequency f_C

$$f_C = \frac{f_{D(min)} - f_1}{N}$$

3. Calculate feedback divider's maximum value

$$P_{max} = \frac{\Delta f_D}{f_1} + P_{min}$$

where $P_{min} = 1$ for minimum f_C.

4. Find maximum divide-by-P frequency

$$f_{Q(max)} = \Delta f_D + f_1$$

5. Calculate allowable VCO swing

$$Nf_C - f_1 < f_{VCO} < (N + 1)\ f_C - f_{Q(max)}$$

6. If the above constraints are too tight choose the next lower number for N and repeat steps 2 and 5 until satisfied.

SKIP-LOCK TUNING

Harmonic mixing provides an alternate means to frequency synthesis without the feedback divide-by-P network. In this instance the design objective is to provide a large frequency coverage with a set (and relatively wide) channel spacing. The configuration is identical to a single frequency PLL (Figure 15) except it operates in the harmonic mode and tuning is accomplished at the VCO. Output frequency is fixed as being f_1 above all harmonics of f_C. As the VCO is tuned through its range, the loop will acquire and lose signals spaced f_C apart. Since these must be some frequency for the phase detector to operate with, the output frequency cannot be a direct harmonic of f_C. This facet of the circuit often causes users to refer to f_1 as the "offset" frequency.

The value of f_1 is often dictated by output frequency and channel spacing requirements. However the relationship of f_1 to f_C has a large effect on the tunability both up and down the frequency range. If, for example, the loop were locked at point A (Figure 16) and B were the next desired point, then the VCO must be "dragged" from A to A′ before lock can be achieved. This frequency adjustment may be quite critical since the frequency difference between A′ and B is only $2f_1$. If the VCO is tuned past B the opportunity for lock has been passed.

On the other hand, in going from B to A, the upper end of the VCO control range must only cross A′ before the loop acquires frequency A. In either case it's apparent that the loop will not "jump" from one lock point to another and some indication of loop lock should be added. This is normally done by monitoring the VCO dc control line with a pair of comparators and noting when the line reaches its limits.

FIGURE 15

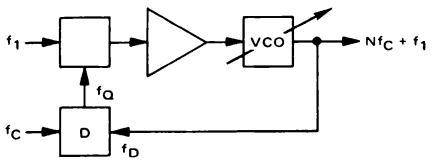
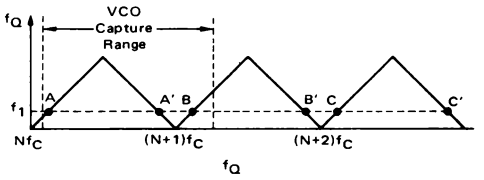


FIGURE 16



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{IL} min	Vdc
Output Source Current	I_o	40	mAdc
Storage Temperature Range	T_{stg}	-55 to +125	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	–

*AC fan-out is limited by desired system performance.

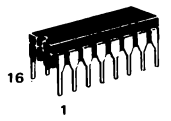
TWO-MODULUS PRESCALER

MC12012

The MC12012 is a two-modulus prescaler which consists of three functional blocks: 1) a controllable divide by 5/divide by 6 prescaler; 2) a divide by 2 prescaler; and 3) a MECL to MTTL translator. When used with the MC12014 Counter Control Logic function and the MC4016 programmable counter, a divide by N programmable counter can be constructed for operation to 200 MHz. This arrangement is especially useful in frequency synthesizer applications.

- ÷2, ÷5/÷6, ÷10/÷11, ÷10/÷12
- MECL to MTTL Translator on Chip
- +5.0 or -5.2 V Operation*
- 200 MHz (typ) Toggle Frequency

*When using +5.0 V supply, apply +5.0 V to pin 16 (V_{CC}) and ground pin 8 (V_{EE}). When using -5.2 V supply, ground pin 16 (V_{CC}) and apply -5.2 V to pin 8 (V_{EE}).



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT

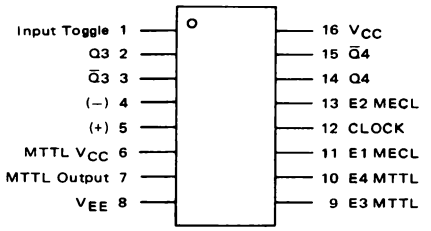


FIGURE 1 – LOGIC DIAGRAM

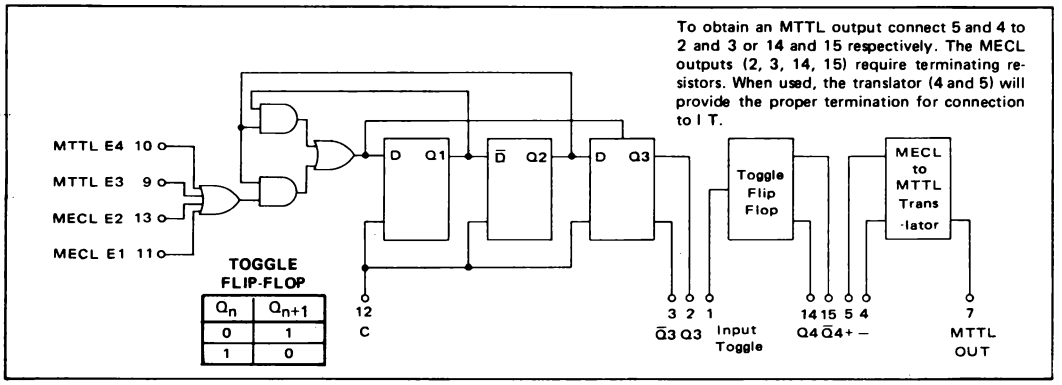
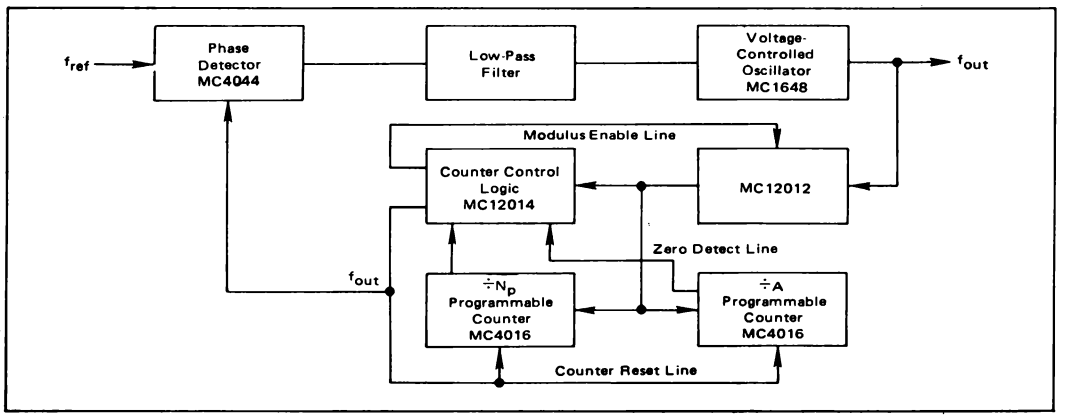


FIGURE 2 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to $V_{IL\ min}$	Vdc
Output Source Current	I_o	20	mAdc
Storage Temperature Range	T_{stg}	-55 to +125	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	–

*AC fan-out is limited by desired system performance.

ELECTRICAL CHARACTERISTICS

Supply Voltage -5.2 V

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts)									TEST VOLTAGE/CURRENT VALUES (mA)		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}
0°C	-0.840	-1.870	-1.145	-1.490	-4.7	+0.3	-3.2	-4.4	-5.2	-2.5	16	-1.6
25°C	-0.810	-1.850	-1.105	-1.475	-4.7	+0.3	-3.2	-4.4	-5.2	-2.5	16	-1.6
75°C	-0.720	-1.880	-1.045	-1.450	-4.7	+0.3	-3.2	-4.4	-5.2	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	100	–	–	–	mAdc	–	–	–	–	–	–	–	–	8	–	–	–	6,16
Input Current	I_{INH1}	12	–	–	–	100	200	–	–	µAdc	12	–	–	–	–	–	–	–	8	–	–	–	16
	I_{INH2}	1	–	–	–	40	100	–	–	µAdc	1	–	–	–	–	–	–	–	8	–	–	–	16
		11	–	–	–	40	100	–	–		11	–	–	–	–	–	–	–	8	–	–	–	16
		13	–	–	–	40	100	–	–		13	–	–	–	–	–	–	–	8	–	–	–	16
	I_{INH3}	9	–	–	–	–	40	–	–	µAdc	–	–	–	–	–	9	–	–	8	–	–	–	16
		10	–	–	–	–	40	–	–		–	–	–	–	–	10	–	–	8	–	–	–	16
	I_{INH4}	4	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
		5	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
Leakage Current	I_{INL1}	1	–	–	–	–	2.0	–	–	µAdc	–	–	–	–	–	–	–	–	1,8	–	–	–	16
		11	–	–	–	–	↓	–	–	↓	–	–	–	–	–	–	–	–	8,11	–	–	–	↓
		12	–	–	–	–		–	–		–	–	–	–	–	–	–	–	8,12	–	–	–	
		13	–	–	–	–		–	–		–	–	–	–	–	–	–	–	8,13	–	–	–	
	I_{INL2}	9	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	9	–	–	–	8	–	–	–	16
		10	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	10	–	–	–	8	–	–	–	16
	I_{INL3}	4	–	–	3.8	–	6.5	–	–	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	16
		5	–	–	2.0	–	4.0	–	–	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	16
Logic "1" Output Voltage ②	V_{OH1}	2	-1.000	-0.840	-0.960	–	-0.810	-0.900	-0.720	Vdc	–	11,13	–	–	9,10	–	–	–	8	2	–	–	16
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–		3	–	–	↓
		14				–					–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–	↓	15	–	–	
	V_{OH2}	7	-2.800	–	-2.800	–	–	-2.800	–	Vdc	5	4	–	–	–	–	–	–	8	–	–	7	6
Logic "0" Output Voltage ②	V_{OL1}	2	-1.870	-1.635	-1.850	–	-1.620	-1.830	-1.595	Vdc	–	11,13	–	–	9,10	–	–	–	8	2	–	–	16
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–		3	–	–	↓
		14				–					–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–	↓	15	–	–	
	V_{OL2}	7	–	-4.700	–	–	-4.700	–	-4.700	Vdc	4	5	–	–	–	–	–	–	8	–	7	–	6
Logic "1" Threshold Voltage	V_{OHA}	2 ④	-1.020	–	-0.980	–	–	-0.920	–	Vdc	–	–	11,13	–	–	–	9,10	–	8	2	–	–	16
		3 ③	↓	–	↓	–	–	↓	–	↓	–	–	11,13	–	–	–	9,10	–		3	–	–	↓
		14 ④		–		–	–		–		–	–	–	–	–	–	–	–		14	–	–	
		15 ④		–		–	–		–		–	–	–	–	–	–	–	–	↓	15	–	–	
Logic "0" Threshold Voltage	V_{OLA}	2 ⑤	–	-1.615	–	–	-1.600	–	-1.575	Vdc	–	–	–	11,13	–	–	–	9,10	8	2	–	–	16
		3 ⑤	–	↓	–	–	↓	–	↓	↓	–	–	–	11,13	–	–	–	9,10		3	–	–	↓
		14 ④	–		–	–		–			–	–	–	–	–	–	–	–		14	–	–	
		15 ④	–		–	–		–			–	–	–	–	–	–	–	–	↓	15	–	–	
Short Circuit Current	I_{OS}	7	-20	-65	-20	–	-65	-20	-65	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6

ELECTRICAL CHARACTERISTICS

Supply Voltage +5.0 V

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IHT}	V_{ILT}	V_{CC}	I_L (mA)	I_{OL} (mA)	I_{OH} (mA)
0°C	+4.160	+3.130	+3.855	+3.510	+0.5	+5.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
25°C	+4.190	+3.150	+3.895	+3.525	+0.5	+5.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
75°C	+4.280	+3.170	+3.955	+3.550	+0.5	+5.5	+2.0	+0.8	+5.0	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	MC12012 0°C Max	MC12012 +25°C Min	MC12012 +25°C Typ	MC12012 +25°C Max	MC12012 +75°C Min	MC12012 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IHT}	V_{ILT}	V_{CC}	I_L (mA)	I_{OL} (mA)	I_{OH} (mA)	(V_{EE}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	95	–	–	–	mAdc	–	–	–	–	–	–	–	–	6,16	–	–	–	8
Input Current	I_{INH1}	12	–	–	–	100	200	–	–	µAdc	12	–	–	–	–	–	–	–	16	–	–	–	8
	I_{INH2}	1	–	–	–	40	100	–	–	µAdc	1	–	–	–	–	–	–	–	16	–	–	–	8
		11	–	–	–	40	100	–	–		11	–	–	–	–	–	–	–	16	–	–	–	8
		13	–	–	–	40	100	–	–		13	–	–	–	–	–	–	–	16	–	–	–	8
	I_{INH3}	9	–	–	–	–	40	–	–	µAdc	–	–	–	–	–	9	–	–	16	–	–	–	8
		10	–	–	–	–	40	–	–		–	–	–	–	–	10	–	–	16	–	–	–	8
	I_{INH4}	4	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	6	–	–	–	8
		5	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	6	–	–	–	8
Leakage Current	I_{INL1}	1	–	–	–	–	2.0	–	–	µAdc	–	–	–	–	–	–	–	–	16	–	–	–	1,8
		11	–	–	–	–	↓	–	–	↓	–	–	–	–	–	–	–	–	↓	–	–	–	8,11
		12	–	–	–	–		–	–		–	–	–	–	–	–	–	–		–	–	–	8,12
		13	–	–	–	–		–	–		–	–	–	–	–	–	–	–		–	–	–	8,13
	I_{INL2}	9	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	9	–	–	–	16	–	–	–	8
		10	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	10	–	–	–	16	–	–	–	8
	I_{INL3}	4	–	–	3.8	–	6.5	–	–	mAdc	4	5	–	–	–	–	–	–	6	–	–	–	8
		5	–	–	2.0	–	4.0	–	–	mAdc	4	5	–	–	–	–	–	–	6	–	–	–	8
Logic "1" Output Voltage	V_{OH1} ②	2	4.000	4.160	4.040	–	4.190	4.100	4.280	Vdc	–	11,13	–	–	9,10	–	–	–	16	2	–	–	8
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–		3	–	–	
		14				–					–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–		15	–	–	↓
	V_{OH2}	7	2.400	–	2.400	–	–	2.400	–	Vdc	5	4	–	–	–	–	–	–	6	–	–	7	8
Logic "0" Output Voltage	V_{OL1} ②	2	3.190	3.430	3.210	–	3.440	3.230	3.470	Vdc	–	11,13	–	–	9,10	–	–	–	16	2	–	–	8
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–		3	–	–	
		14				–					–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–		15	–	–	↓
	V_{OL2}	7		0.500	–	–	0.500	–	0.500	Vdc	4	5	–	–	–	–	–	–	6	–	7	–	8
Logic "1" Threshold Voltage	V_{OHA}	2 ③	3.980	–	4.020	–	–	4.080	–	Vdc	–	–	11,13	–	–	–	9,10	–	16	2	–	–	8
		3 ④	↓	–	↓	–	–	↓	–	↓	–	–	11,13	–	–	–	9,10	–		3	–	–	
		14 ④		–		–	–		–		–	–	–	–	–	–	–	–		14	–	–	
		15 ④		–		–	–		–		–	–	–	–	–	–	–	–		15	–	–	↓
Logic "0" Threshold Voltage	V_{OLA}	2 ⑤	–	3.450	–	–	3.460	–	3.490	Vdc	–	–	–	11,13	–	–	–	9,10	16	2	–	–	8
		3 ⑤	–	↓	–	–	↓	–	↓	↓	–	–	–	11,13	–	–	–	9,10		3	–	–	
		14 ④	–		–	–		–			–	–	–	–	–	–	–	–		14	–	–	
		15 ④	–		–	–		–			–	–	–	–	–	–	–	–		15	–	–	↓
Short Circuit Current	I_{OS}	7	-20	-65	-20	–	-65	-20	-65	mAdc	5	4	–	–	–	–	–	–	6	–	–	–	8

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} +1.100	V_{ILmin} +0.130	V_F -3.0 V	V_{EE} -3.0 or -3.2	V_{CC} +2.0
Propagation Delay (See Figures 3 and 4)	t_{12+2+}	12,2	–	–	2.0	3.0	4.0	–	–	ns	12	–	–	–	11,13	9,10	8	6,16
	t_{12+3+}	12,3	–	–		3.0		–	–			–	–	–	11,13	9,10		
	t_{12+}	12,2	–	–		2.8		–	–			–	–	–	11,13	9,10		
	t_{12+3-}	12,3	–	–		2.8		–	–			–	–	–	11,13	9,10		
	t_{1+14+}	1,14	–	–		3.0		–	–		1	–	–	–	–	–		
	t_{1+15+}	1,15	–	–		3.0		–	–			–	–	–	–	–		
	t_{1+14-}	1,14	–	–		2.8		–	–			–	–	–	–	–		
	t_{1+15-}	1,15	–	–		2.8		–	–			–	–	–	–	–		
	t_{5+7+}	5,7	–	–		8.0	12.0	–	–		A	–	–	–	–	–		
	t_{5-7-}	5,7	–	–		5.0	10.0	–	–		A	–	–	–	–	–		
Output Rise Time (See Figure 4)	t_{2+}	2	–	–	–	2.0	–	–	–	ns	12	–	–	–	11,13	9,10	8	6,16
	t_{3+}	3	–	–	–	2.0	–	–	–		12	–	–	–	11,13	9,10		
	t_{14+}	14	–	–	–	2.0	–	–	–		1	–	–	–	–	–		
	t_{15+}	15	–	–	–	2.0	–	–	–		1	–	–	–	–	–		
Output Fall Time (See Figure 4)	t_{2-}	2	–	–	–	2.0	–	–	–	ns	12	–	–	–	11,13	9,10	8	6,16
	t_{3-}	3	–	–	–	2.0	–	–	–		12	–	–	–	11,13	9,10		
	t_{14-}	14	–	–	–	2.0	–	–	–		1	–	–	–	–	–		
	t_{15-}	15	–	–	–	2.0	–	–	–		1	–	–	–	–	–		
Setup Time (See Figure 5)	t_{setup1}	11,13	–	4.0	–	2.4	3.0	–	4.0	ns	12	11/13	–	–	13/11	9,10	8	6,16
	t_{setup2}	9,10	–	7.0	–	5.0	7.0	–	8.5	ns	12	–	9/10	–	11,13	10/9	8	6,16
Release Time (See Figure 5)	t_{rel1}	11,13	–	2.5	–	1.2	2.0	–	2.0	ns	12	11/13	–	–	13/11	9,10	8	6,16
	t_{rel2}	9,10	–	4.0	–	2.5	3.5	–	2.0	ns	12	–	9/10	–	11,13	10/9	8	6,16
Toggle Frequency	f_{max}									MHz								
Figure 6 (÷5)		2	–	–	175	200	–	–	–		–	–	–	11	13	9,10	8	16
(÷6)		2	–	–			–	–	–		–	–	–	–	11,13	9,10		
(÷2)		14	–	–			–	–	–		–	–	–	–	–	–		
Figure 7 (÷10 or 11)		14	–	–			–	–	–		–	–	–	–	–	–		

① All MECL outputs (2,3,14,15) are terminated to V_{EE} through an external 510 Ω resistor during the DC tests.

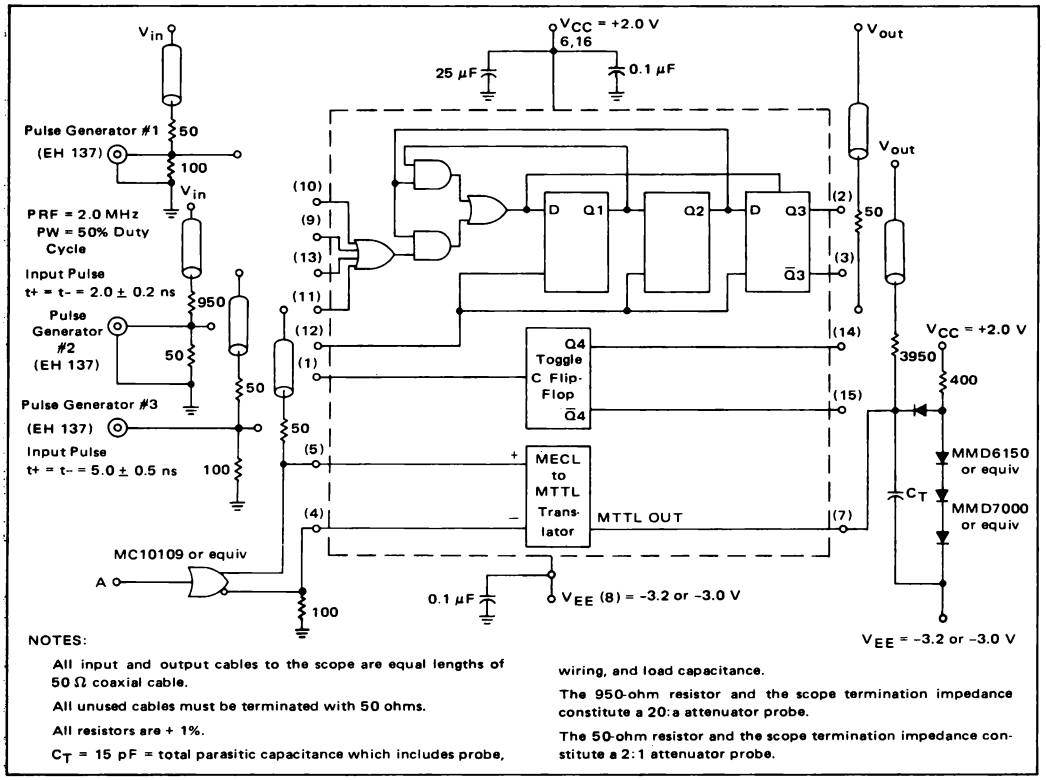
② Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is

③ In addition to meeting the output levels specified, the device must divide by 5 during this test. The clock input is

④ In addition to meeting the output levels specified the device must divide by 2 with a clock input of

⑤ In addition to meeting the output levels specified, the device must divide by 6 during this test. The clock input is

FIGURE 3 – AC TEST CIRCUIT



NOTES:

All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

All unused cables must be terminated with 50 ohms.

All resistors are ± 1%.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.

The 950-ohm resistor and the scope termination impedance constitute a 20:a attenuator probe.

The 50-ohm resistor and the scope termination impedance constitute a 2:1 attenuator probe.

FIGURE 4 – AC VOLTAGE WAVEFORMS

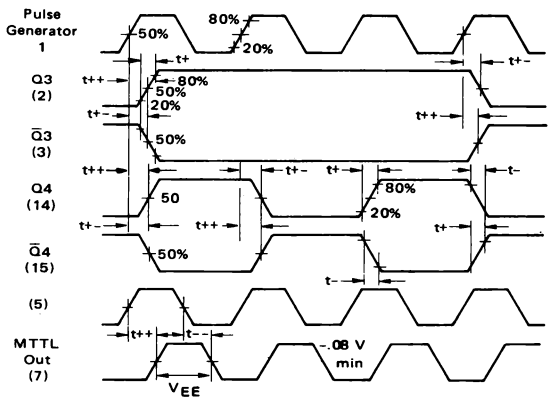


FIGURE 5 – SETUP AND RELEASE TIME WAVEFORMS

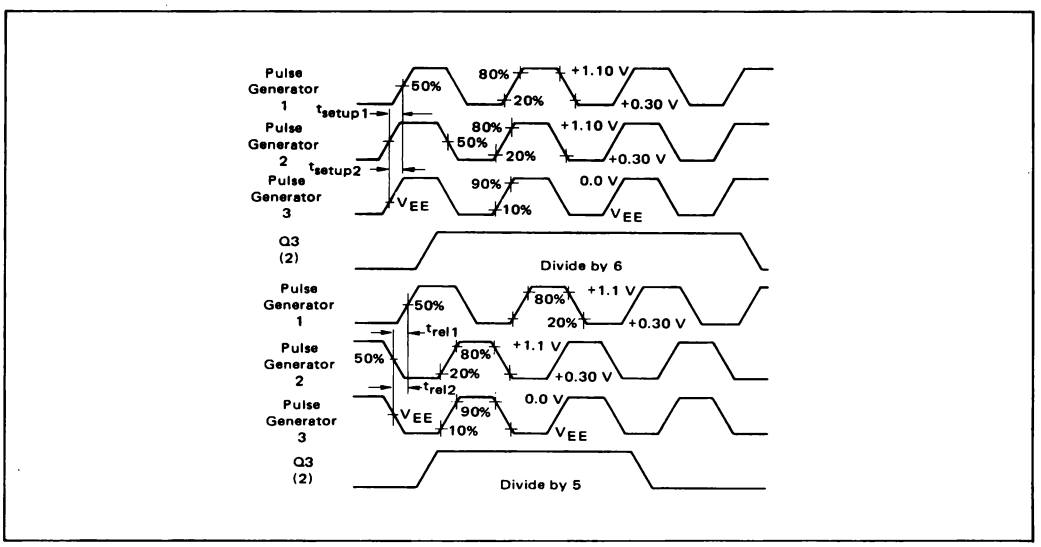
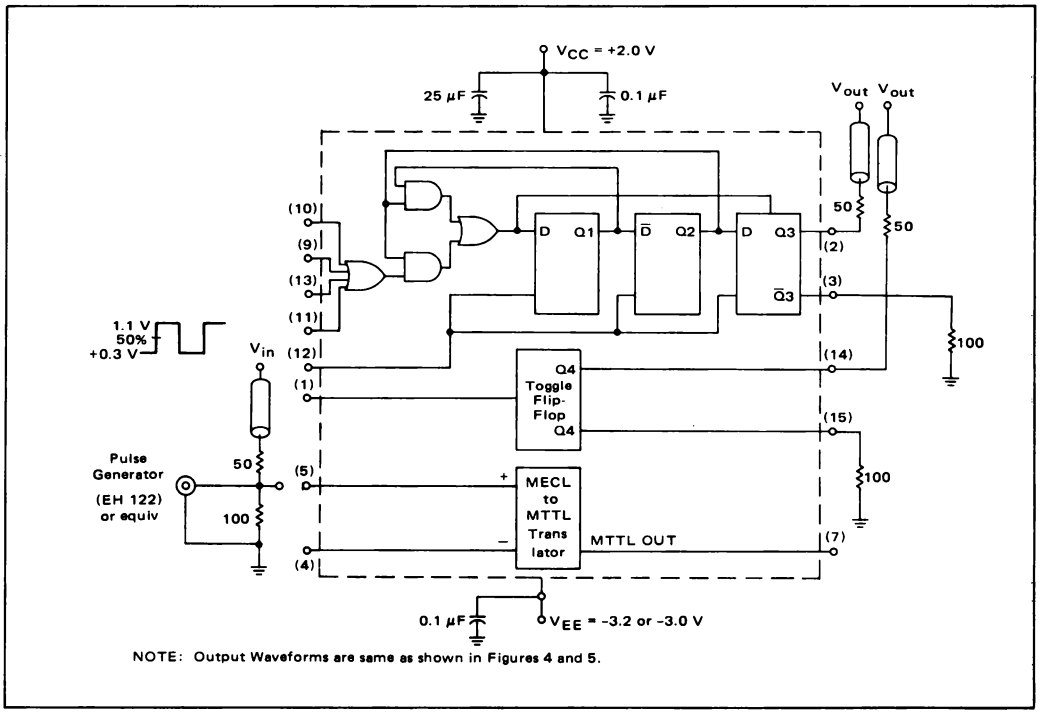
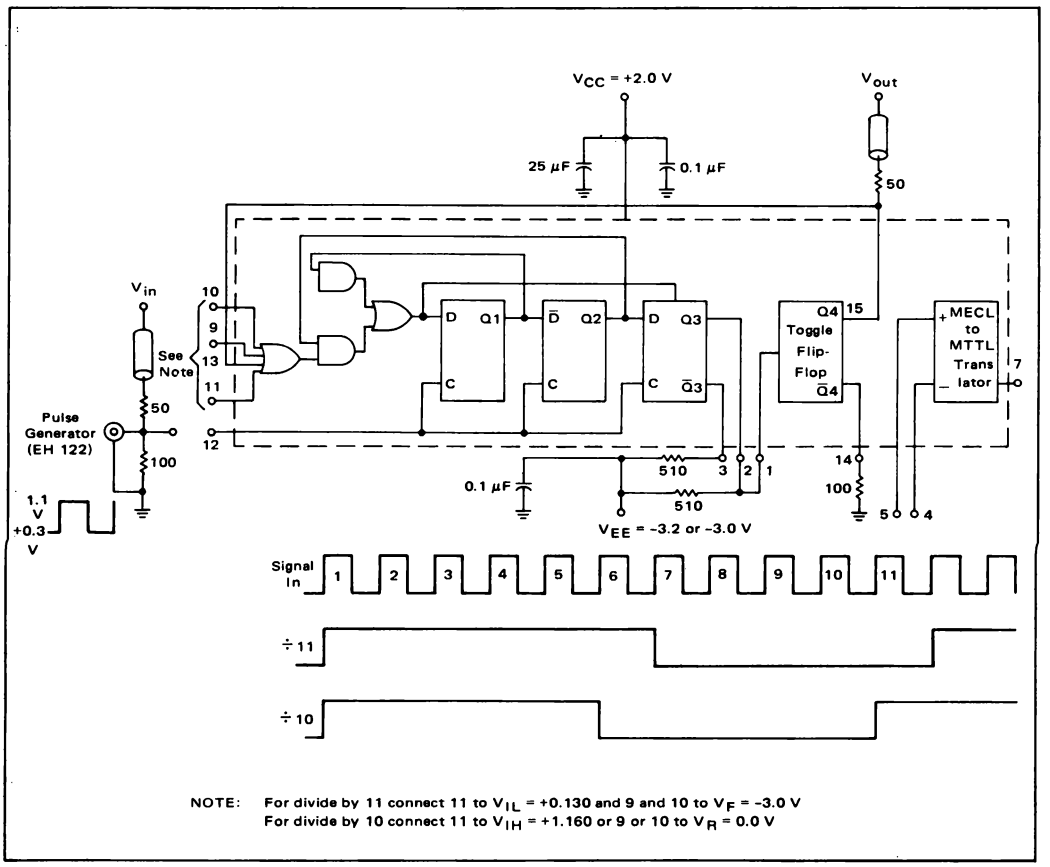


FIGURE 6 – MAXIMUM FREQUENCY TEST CIRCUIT



NOTE: Output Waveforms are same as shown in Figures 4 and 5.

FIGURE 7 – MAXIMUM FREQUENCY TEST CIRCUIT



NOTE: For divide by 11 connect 11 to V_{IL} = +0.130 and 9 and 10 to V_F = -3.0 V
For divide by 10 connect 11 to V_{IH} = +1.160 or 9 or 10 to V_R = 0.0 V

FIGURE 8 – STATE DIAGRAMS

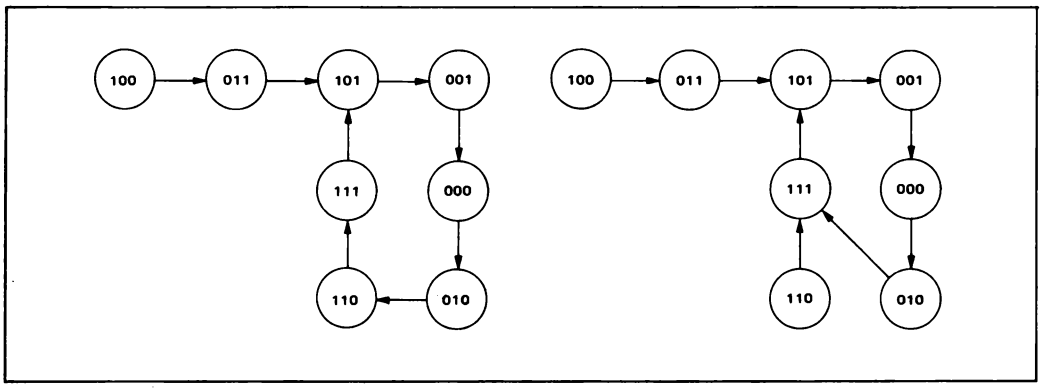
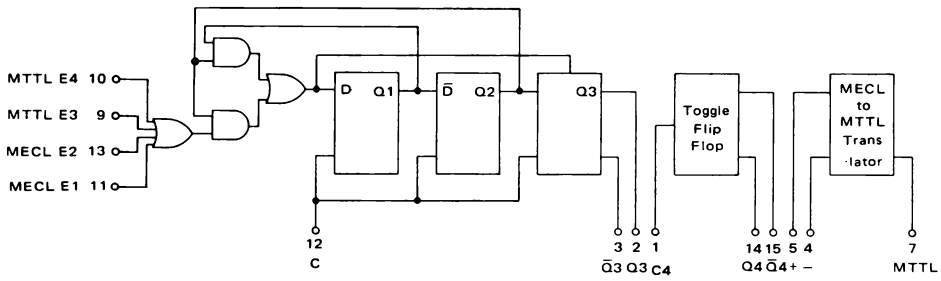


FIGURE 9 – ÷5/6



Divide by 2 use Toggle Flip-Flop

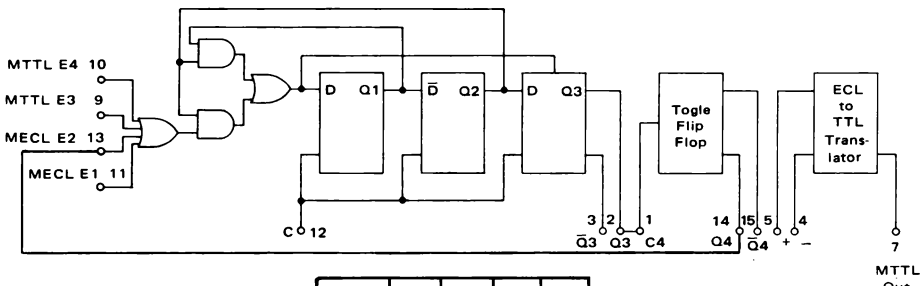
E1 + E2 + E3 + E4 = 1

E1 + E2 + E3 + E4 = 0

COUNT	Q1	Q2	Q3
6	0	1	1
7	1	1	1
5	1	0	1
1	1	0	0
0	0	0	0
2	0	1	0

To obtain a MTTL output connect 5 and 4 to 2 and 3 or 14 and 15 respectively.

FIGURE 10 – ÷10/11



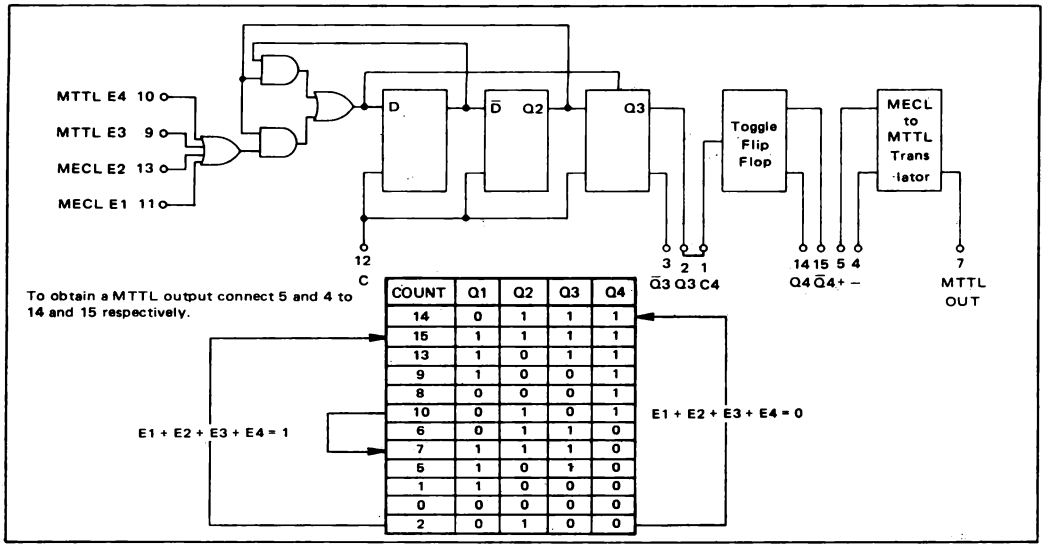
E1 + E3 + E4 = 1

E1 + E3 + E4 = 0

COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

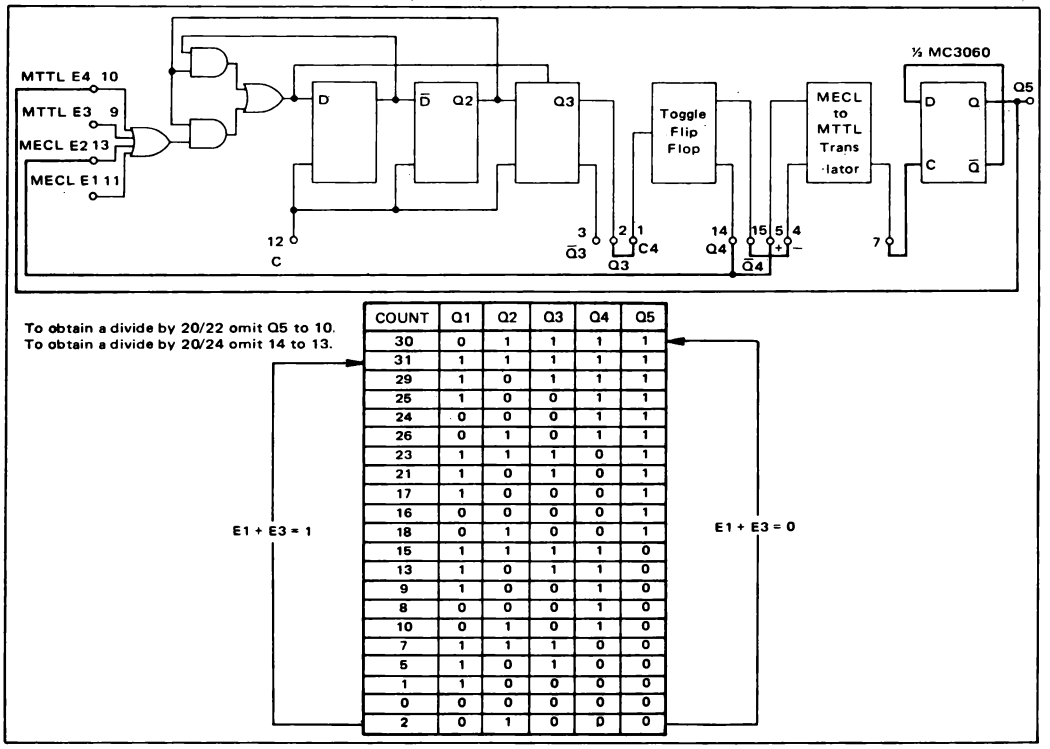
To obtain a MTTL output connect 5 and 4 to 14 and 15 respectively.

FIGURE 11 – - - 10/12



COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
6	0	1	1	0
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

FIGURE 12 - - 20/21



COUNT	Q1	Q2	Q3	Q4	Q5
30	0	1	1	1	1
31	1	1	1	1	1
29	1	0	1	1	1
25	1	0	0	1	1
24	0	0	0	1	1
26	0	1	0	1	1
23	1	1	1	0	1
21	1	0	1	0	1
17	1	0	0	0	1
16	0	0	0	0	1
18	0	1	0	0	1
15	1	1	1	1	0
13	1	0	1	1	0
9	1	0	0	1	0
8	0	0	0	1	0
10	0	1	0	1	0
7	1	1	1	0	0
5	1	0	1	0	0
1	1	0	0	0	0
0	0	0	0	0	0
2	0	1	0	0	0

FUNCTION DESCRIPTION

INTRODUCTION

The MC12012 is one part of a variable modulus (divisor) prescaling subsystem used in certain Digital Phase-Locked Loops (PLL).

More often than not, the feedback loop of any PLL contains a counter-divider. Many methods are available for building a divider, but not all are simple, economical, or convenient in a particular application.

The technique and system described here offer a new approach to the construction of a phase-locked loop divider. In addition to using the MC12012 variable modulus prescaler, this system requires an MC12014 Counter Control Logic function, together with suitable programmable counters (e.g. MC4016s). Data sheets for these additional devices should be consulted for their particular functional descriptions.

THE MC12012 TWO MODULUS PRESCALER

Three functional blocks are contained in the MC12012 variable modulus prescaler: 1) a controllable ÷5/÷6 prescaler; 2) a ÷ 2 prescaler; and 3) an ECL to TTL translator (for single power supply operation).

Selection of division by 5 or by 6 is made by inputs to E1 through E4. If all E inputs are low before the transition of the clock pulse driving Q3 high, Q3 will stay high for 3 clock pulses, then will go low for 3 clock pulses. This provides a divide by 6 function.

On the other hand, if any one or all of the E inputs are high prior to the positive transition of the clock pulse driving Q3 high, Q3 will stay high for only 2 clock pulses, then will go low for 3 clock pulses. The result is division by 5.

For the ÷5 operation, at least one of the E inputs must go high sometime before the clock pulse. This time is referred to as the "setup time." Specifications for setup time are given in the electrical characteristics table: t_{setup1} and t_{setup2} for E1 and E2 (MECL inputs), and E3 and E4 (MTTL inputs).

For the divide by 6 operation all E inputs must be low for some time prior to the clock pulse. This time is referred to as the "release time." Data for release time is given in the electrical characteristics table; t_{re1} and t_{re2} for E1, E2, E3, E4.

The data given in the tables for setup and release times are referenced to the positive transition of the clock pulse causing Q3 to go high. If it is necessary to reference the setup and release times to the positive transition of Q3, add t++ (specified for Q3) to the setup/release times given. It should be noted that the logic states for the enable inputs are important only for only one clock pulse which causes Q3 to go high (within the limits specified by setup and release times).

The ÷ 5/÷ 6 prescaler may be connected externally to the ÷ 2 prescaler to form a ÷ 10/÷ 11 prescaler (Figure 10) or a ÷ 10/÷ 12 prescaler (Figure 11).

By way of an example showing how a ÷ 10/÷ 11 prescaler operates, note that if E1, E3, and E4 (Figure 10) are held in a low state, the counter divides by 11. To do this, a feedback connection is established from Q4 to E2 (or to E1). With this feedback, the ÷ 5/÷ 6 prescaler divides by 5 when Q4 is high, and by 6 when Q4 is low.

Since Q4 changes state with each positive transition of Q3, the prescaler alternates between ÷ 5 and ÷ 6 resulting in a ÷ 11 at Q4.

If any one or all of the E inputs are high (Figure 10), the 5/6 prescaler always divides by 5 and a divide by 10 results at Q4.

With the addition of external flip-flops and counters (MECL or MTTL) various other modulus prescalers may be produced (20/21, 20/22, 20/24, 40/41, 50/51, 100/101, etc.).

THE TECHNIQUE OF DIRECT PROGRAMMING BY UTILIZING A TWO MODULUS PRESCALER (MC12012)

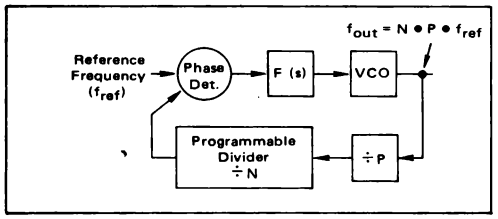
The disadvantage of using a fixed modulus (÷ P) for frequency division in high frequency phase-locked loops (PLL) is that it requires dividing the desired reference frequency by P also (desired reference frequency equals channel spacing.)

The MC12012 is specially designed for use with a technique called "variable modulus prescaling". This technique allows a simple MECL two-modulus prescaler (MC12012) to be controlled by a relatively slow MTTL programmable counter. The use of this technique permits direct high-frequency prescaling without any sacrifice in resolution since it is no longer necessary to divide the reference frequency by the modulus of the high frequency prescaler.

The theory of "variable modulus prescaling" may be explained by considering the system shown in Figure 13. For the loop shown:

$$f_{out} = N \bullet P \bullet f_{ref} \quad (1)$$

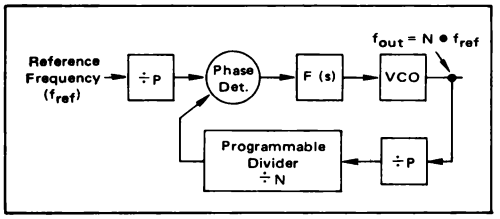
FIGURE 13 – FREQUENCY SYNTHESIS BY PRESCALING



where P is fixed and N is variable. For a change of 1 in N, the output frequency changes by $P \bullet f_{ref}$. If f_{ref} equals the desired channel spacing, then only every P channel may be programmed using this method. A problem remains: how to program intermediate channels.

One solution to this problem is shown in Figure 14.

FIGURE 14 – FREQUENCY SYNTHESIS BY PRESCALING



A ÷ P is placed in series with the desired channel spacing (frequency) to give a new reference frequency: channel spacing/P.

Another solution is found by considering the defining equation (1) for f_{out} of Figure 13. From the equation it may be seen that only every P channel can be programmed simply, because N is always an integer. To obtain intermediate channels, P must be multiplied by an integer plus a fraction. This fraction would be of the form: A/P. If N is defined to be an integer number, Np, plus a fraction, A/P, N may be expressed as:

$$N = Np + A/P.$$

Substituting this expression for N in equation 1 gives:

$$f_{out} = (Np + A/P) \bullet P \bullet f_{ref} \quad (2)$$

or:

$$f_{out} = (Np\ P + A) \bullet f_{ref} \quad (3)$$

$$f_{out} = Np \bullet P \bullet f_{ref} + A \bullet f_{ref}. \quad (4)$$

Equation 4 shows that all channels can be obtained directly if N can take on fractional values. Since it is difficult to multiply by a fractional number, equation 4 must be synthesized by some other means.

Taking equation 3 and adding ±AP to the coefficient of f_{ref}, the equation becomes:

$$f_{out} = (Np \bullet P + A + A \bullet P - A \bullet P)\ f_{ref}. \quad (5)$$

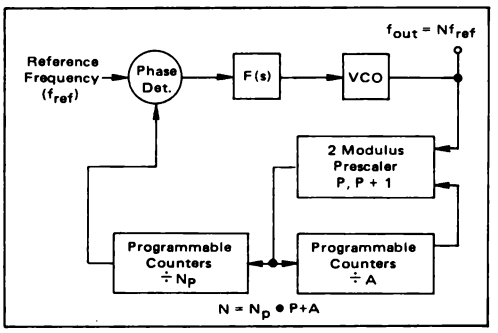
Collecting terms and factoring gives:

$$f_{out} = [(Np - A)\ P + A\ (P + 1)]\ f_{ref} \quad (6)$$

From equation 6 it becomes apparent that the fractional part of N can be synthesized by using a two-modulus counter (P and P + 1) and dividing by the upper modulus, A times, and the lower modulus (Np - A) times.

This equation (6) suggests the circuit configuration in Figure 15. The A counter shown must be the type that

FIGURE 15 – FREQUENCY SYNTHESIS BY TWO MODULUS PRESCALING



counts from the programmed state (A) to the enable state, and remains in this state until divide by Np is completed in the programmable counter.

In operation, the prescaler divides by P + 1, A times. For every P + 1 pulse into the prescaler, both the A counter and Np counter are decremented by 1. The prescaler divides by P + 1 until the A counter reaches the zero state. At the end of (P + 1) • A pulses, the state of the Np counter equals (Np - A). The modulus of the prescaler then changes to P. The variable modulus counter divides by P until the remaining count, (Np - A) in the Np counter, is decremented to zero. Finally, when this is completed, the A and Np counters are reset and the cycle repeats.

To further understand this prescaling technique, consider the case with P = 10. Equation 6 becomes:

$$f_{out} = (A + 10\ Np) \bullet f_{ref} \quad (7)$$

If Np consists of 2 decades of counters then:

$$Np = 10\ Np_1 + Np_0$$

(Np_1 is the most significant digit),

and equation 7 becomes:

FIGURE 16 – DIRECT PROGRAMMING UTILIZING TWO-MODULUS PRESCALER

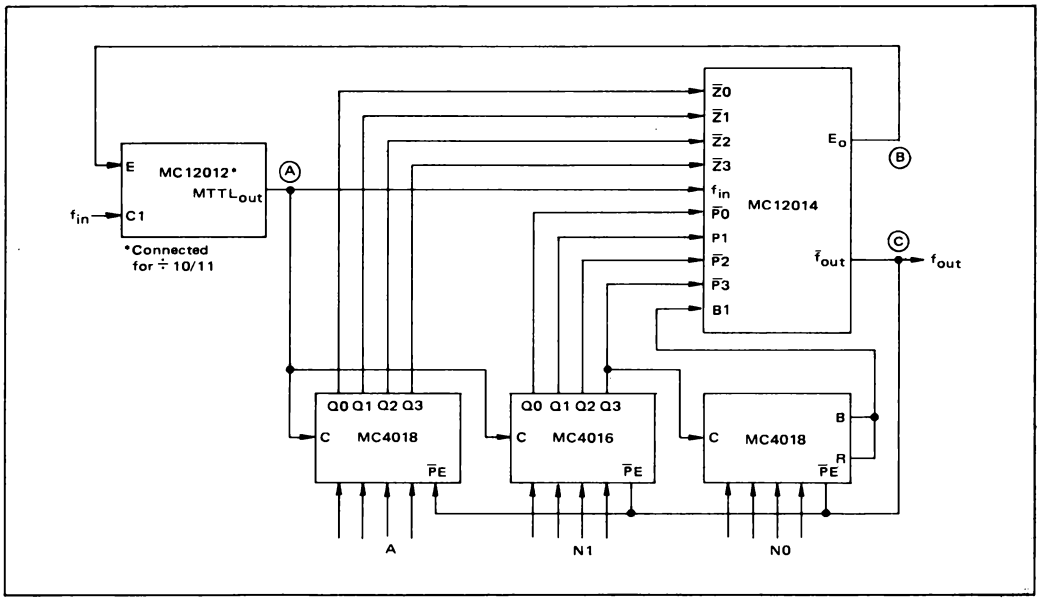


FIGURE 17 – WAVEFORMS FOR DIVIDE BY 43

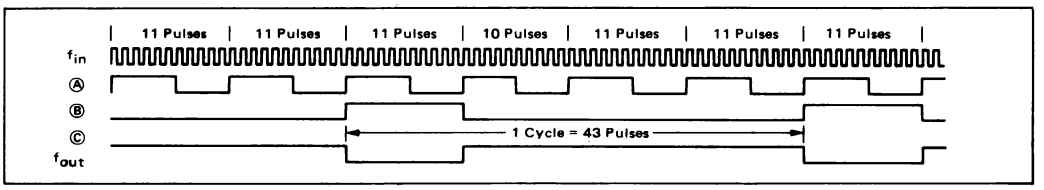


FIGURE 18 – WAVEFORMS FOR DIVIDE BY 42

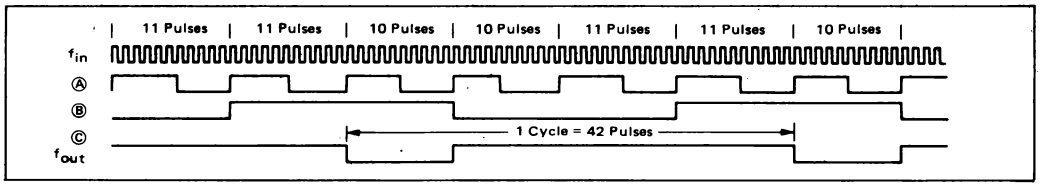
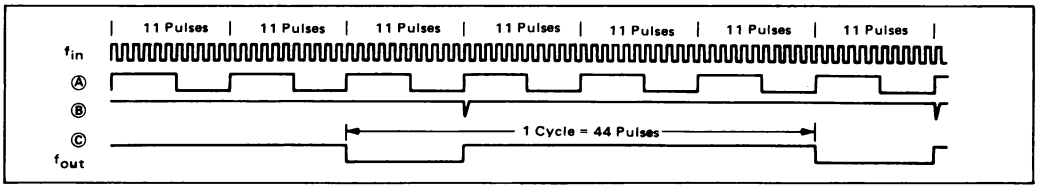


FIGURE 19 – WAVEFORMS FOR DIVIDE BY 44



$$f_{out} = (100\,N_{P1} + 10\,N_{P0} + A)\,f_{ref}.$$

To do variable modulus prescaling using the MC12012 and programmable divide by N counters (MC4016, MC4018, one additional part is required: the MC12014 (Counter Control Logic).

In variable modulus prescaling the MC12014 serves a dual purpose: it detects the terminal (zero) count of the A counter, to switch the modulus of the MC12012; and it extends the maximum operating frequency of the programmable counters to above 25 MHz. (See the MC12014 data sheet for a detailed description of the Counter Control Logic).

Figure 16 shows the method of interconnecting the MC12012, MC12014, and MC4016 (or MC4018) for variable modulus prescaling. To understand the operation of the circuit shown in Figure 16, consider division by 43. Division by 43 is done by programming $N_{P1} = 0$, $N_{P0} = 4$, and $A = 3$.

Waveforms for various points in the circuit are shown in Figure 17 for this division. From the waveforms it may be seen that the two-modulus prescaler starts in the divide by 11 mode, and the first input pulse causes point A to go high. This positive transition decrements the Np counter to 3, and counter A to 2.

After 11 pulses, point Ⓐ again goes high; the Np counter decrements to 2 and the A counter to 1. The "2" contained in the Np counter enables the inputs to the frequency extender portion of the MC12014. After 11 more pulses point Ⓐ goes high again.

With this position transition at Ⓐ, the output (f_{out}) of the MC12014 goes low, the Np counter goes to 1, and the A counter goes to 0. The zero state of the A counter is detected by the MC12014, causing point Ⓑ to go to 1 and changing the modulus of the MC12012 to 10 at the start of the cycle.

When f_{out} goes low, the programmable counters are reset to the programmed number. After 11 pulses (the enable went high after the start of the cycle and therefore doesn't change the modulus until the next cycle), point Ⓐ makes another positive transition. This positive transition causes f_{out} to return high, release the preset on the counter, and generates a pulse to clear the latch (return point Ⓑ to 0).

After 10 pulses the cycle begins again (point Ⓑ was high prior to point Ⓐ going high). The number of input pulses that have occured during this entire operation is: 11 + 11 + 11 + 10 = 43. Figures 18 and 19 show the waveforms for divide by 42 and divide by 44 respectively.

The variable modulus prescaling technique may be used in any application as long as the number in the Np counter is greater than or equal to the number in the A counter. Failure to observe this rule will result in erroneous results. (For example, for the system shown in Figure 16 if the number 45 is programmed, the circuit actually will divide by 44. This is not a serious restriction since Np is greater than A in most applications).

It is important to note that the A counter has been composed of only one counter for discussion only; where required, the A counter may be made as large as needed by cascading several programmable counters. Figure 20 shows the method of interconnecting counters. Operation is previously described. The number of stages in the A counter should not exceed the number of stages for the

FIGURE 20 – METHOD OF INTERCONNECTING COUNTERS

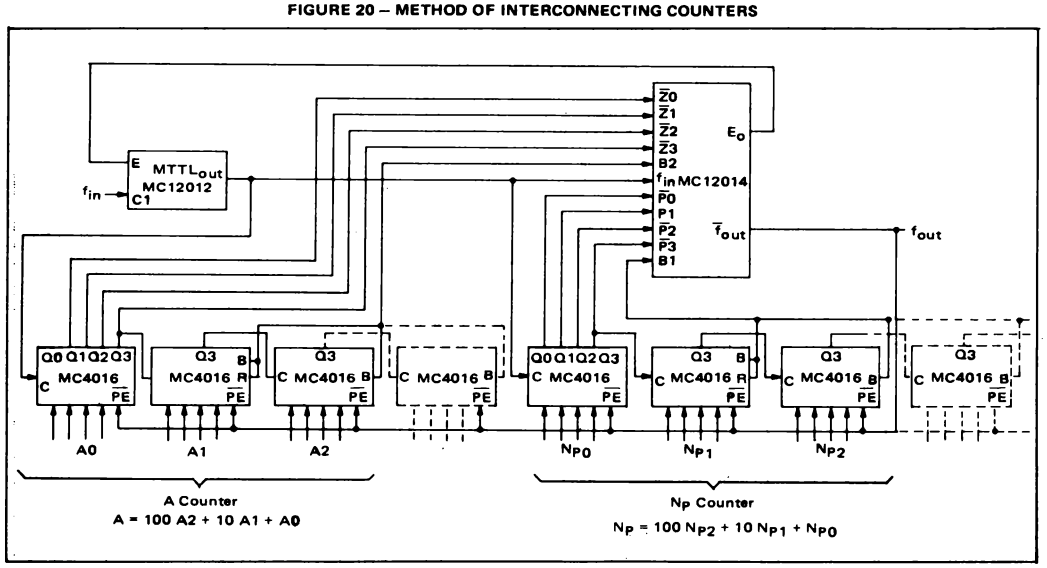


FIGURE 21 – DIRECT PROGRAMMING 100-200 MHz SYNTHESIZER IN 50 kHz STEPS

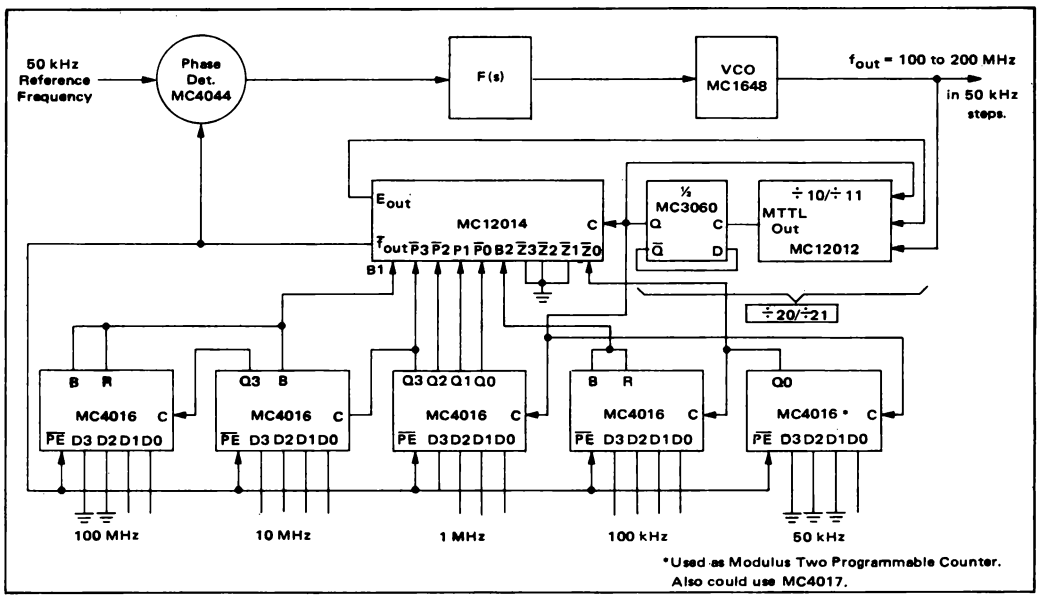
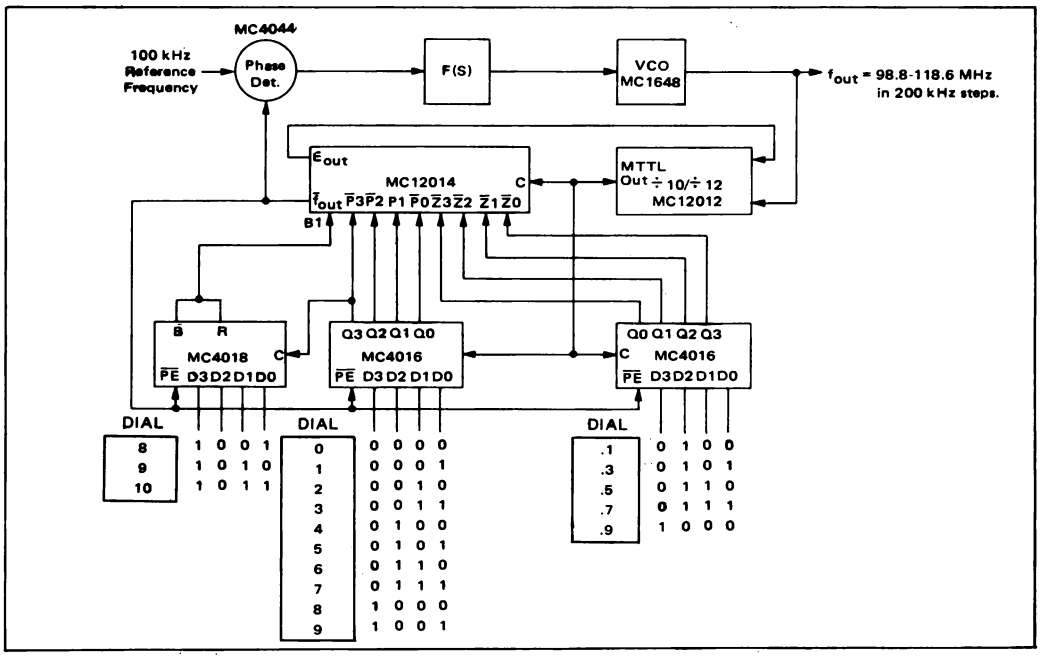


FIGURE 22 – FM BAND SYNTHESIZER WITH 10.7 MHz I.F. OFFSET



Np counters. As many counters as desired may be cascaded, as long as fan-in and fan-out rules for each part are observed.

The theory of "variable modulus prescaling" developed above, examined a case in which the upper modulus of the two-modulus prescaler was 1 greater than the lower modulus. However, the technique described is by no means limited to this one special case. There are applications in which it is desirable to use moduli other than P/(P + 1).

It can be shown that for a general case in which the moduli of the two-modulus prescaler are P and P + M, equation 6 becomes:

$$f_{out} = [(Np - A)\,P + A\,(P + M)] \bullet f_{ref}$$

or

$$f_{out} = [Np \bullet P + M \bullet A] \bullet f_{ref}. \qquad (8)$$

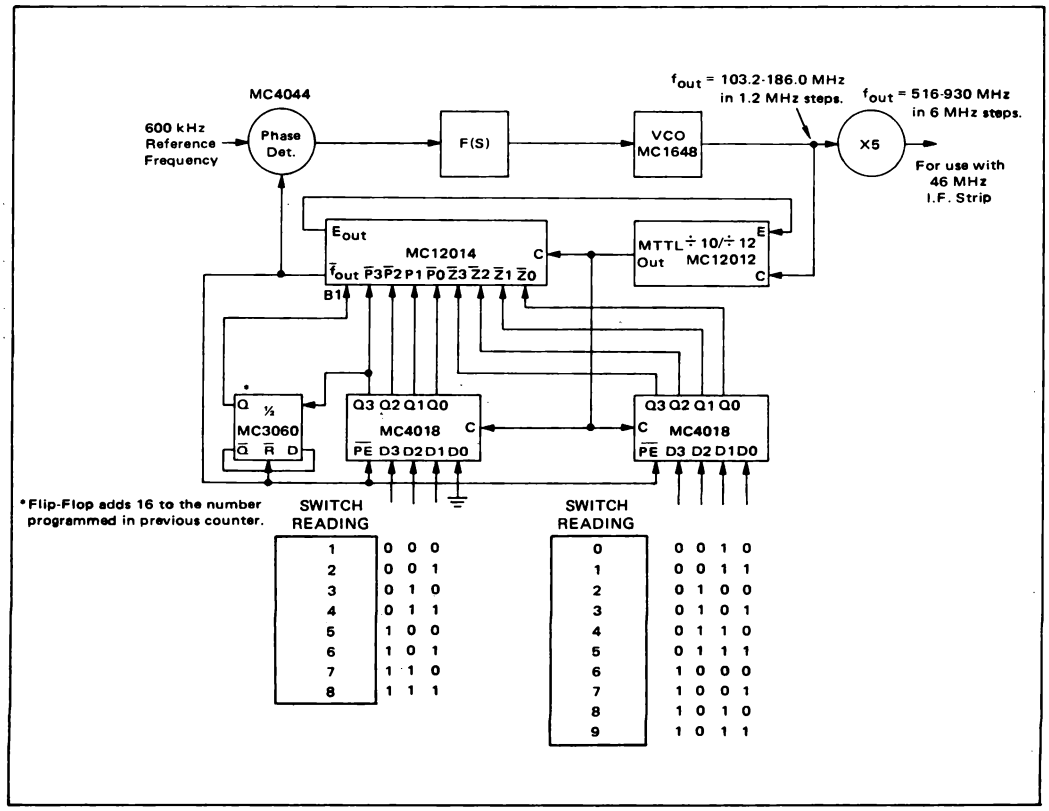
From equation 8 it may be seen that the upper modulus of the two-modulus prescaler has no effect on the Np counter, and that the number programmed in the A counter is simply multiplied by M.

APPLICATIONS

There is no one procedure which will always yield the best counter configuration for all possible MC12012 applications. Each designer will develop his own special design for the counter portion of his PLL system.

An insight into some of the various possible counter schemes may be obtained by considering the various PLL systems shown in Figures 21, 22, and 23. These examples were chosen to show some of the moduli that may be obtained by using the MC12012.

FIGURE 23 – UHF SYNTHESIZER USING 10/12 COUNTER

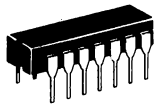


PHASE-FREQUENCY DETECTOR

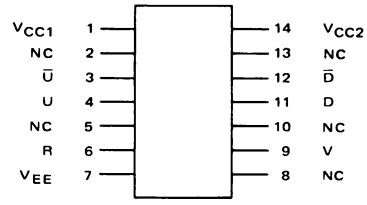
MC12040

The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

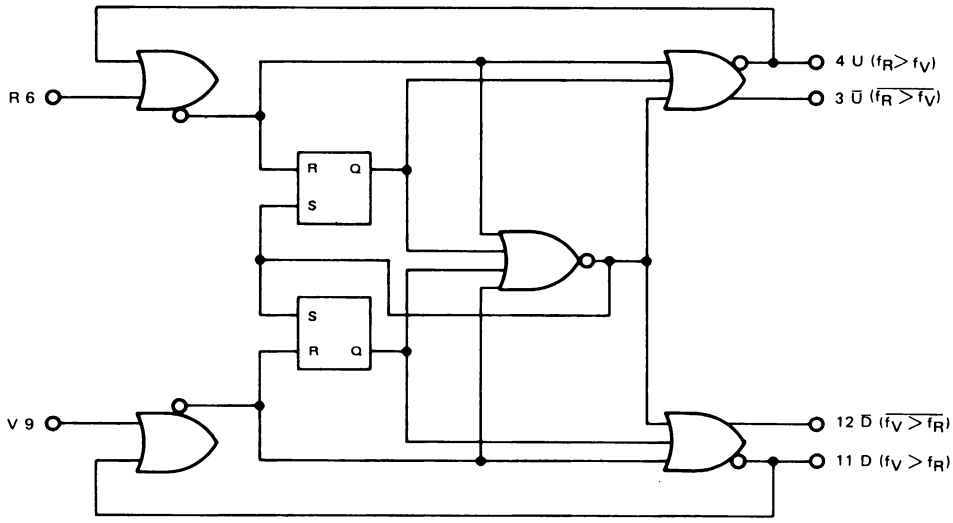
- Operating Frequency = 80 MHz typical



CERAMIC PACKAGE
CASE 632-02



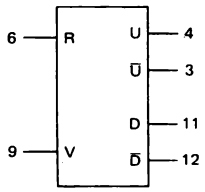
NC – No Connection



V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{CC3} = Pin 7

ELECTRICAL CHARACTERISTICS

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to -2.0 V for -5.2 V tests.



INPUT		OUTPUT			
R	V	U	D	Ū	D̄
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	0

X = Don't Care

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possibile modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

Supply Voltage = -5.2V

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
25°C	-0.810	-1.850	-1.105	-1.475	-5.2
75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Typ	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7	–	–	-60	-90	-120	–	–	mAdc		–	–	–	7	1,14
Input Current	I_{INH}	6				–	350			µAdc	6	–	–	–	7	1,14
		9	–	–		–	350	–	–	µAdc	9	–	–	–	7	1,14
	I_{INL}	6	–	–	0.5	–	–	–	–	µAdc	–	6			7	1,14
		9	–	–	0.5	–	–	–	–	µAdc		9		–	7	1,14
Logic "1" Output Voltage	V_{OH}①	3	-1.000	-0.840	-0.960	–	-0.810	-0.900	-0.720	Vdc			–	–	7	1,14
		4				–								–		
		11				–										
		12				–					–	–	–	–		
Logic "0" Output Voltage	V_{OL}①	3	-1.870	-1.635	-1.850		-1.620	-1.830	-1.595	Vdc	–	–	–		7	1,14
		4				–					–	–	–			
		11				–										
		12				–										
Logic "1" Threshold Voltage	V_{OHA}②	3	-1.020		-0.980	–		-0.920		Vdc			6,9		7	1,14
		4										–				
		11		–		–										
		12		–		–			–							
Logic "0" Threshold Voltage	V_{OLA}②	3	–	-1.615	–		-1.600		-1.575	Vdc		–	9	6	7	1,14
		4	–		–							–	6	9		
		11										–	9	6		
		12	–			–		–			–	–	6	9		

Supply Voltage = +5.0V

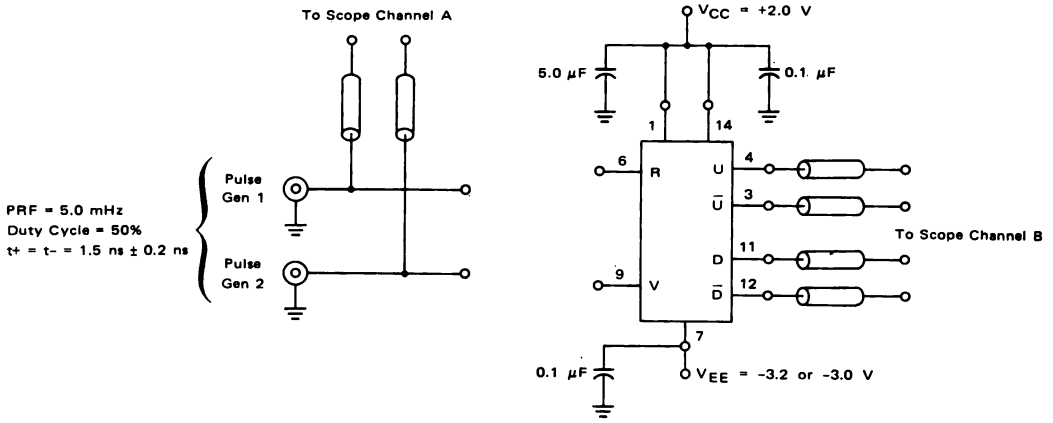
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}
0°C	+4.160	+3.130	+3.855	+3.510	+5.0
25°C	+4.190	+3.150	+3.895	+3.525	+5.0
75°C	+4.280	+3.170	+3.955	+3.550	+5.0

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Typ	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7			-60	-85	-115			mAdc					1,14	7
Input Current	I_{INH}	6					350			µAdc	6				1,14	7
		9					350			µAdc	9				1,14	7
	I_{INL}	6	–	–	0.5	–	–			µAdc		6			1,14	7
		9			0.5					µAdc		9			1,14	7
Logic "1" Output Voltage	V_{OH}①	3	4.000	4.160	4.040	–	4.190	4.100	4.280	Vdc					1,14	7
		4														
		11				–										
		12				–										
Logic "0" Output Voltage	V_{OL}①	3	3.190	3.430	3.210		3.440	3.230	3.470	Vdc					1,14	7
		4														
		11														
		12														
Logic "1" Threshold Voltage	V_{OHA}②	3	3.980		4.020			4.080		Vdc			6,9		1,14	7
		4		–												
		11														
		12							–							
Logic "0" Threshold Voltage	V_{OLA}②	3	–	3.450		–	3.460	–	3.490	Vdc			9	6	1,14	7
		4	–										6	9		
		11						–					9	6		
		12	–										6	9		

① Outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests.

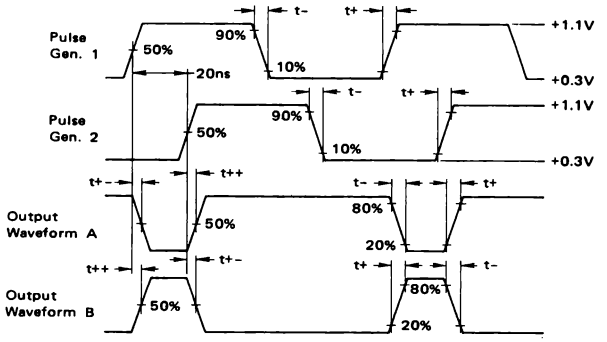
② The device must also function according to the truth table during these tests.

AC TESTS



NOTES:

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. Unused input and outputs are connected to a 50 Ω resistor to ground.
3. The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 6 and 9 are interchanged. The same technique applies.



Characteristic	Symbol	Pin Under Test	Output Waveform	MC12040 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	V_{EE} -3.0 or -3.2 V	V_{CC} +2.0 V
Propagation Delay	t_{6+4+}	6,4	B	–	2.8	1.6	–	2.8	–	3.8	ns	6	9	7	1,14
	t_{6+12+}	6,12	A	–	4.5	2.6	–	4.5	–	5.7		9	6		
	t_{6+3-}	6,3	A	–	2.8	1.6	–	2.8	–	3.8		6	9		
	t_{6+11-}	6,11	B	–	4.8	2.8	–	4.8	–	6.1		9	6		
	t_{9+11+}	9.11	B	–	2.8	1.6	–	2.8	–	3.8		9	6		
	t_{9+3+}	9,3	A	–	4.5	2.6	–	4.5	–	5.7		6	9		
	t_{9+12-}	9.12	A	–	2.8	1.6	–	2.8	–	3.8		9	6		
	t_{9+4-}	9,4	B	–	4.8	2.8	–	4.8	–	6.1		6	9		
Output Rise Time	t_{3+}	3	A	–	2.4	0.8	1.5	2.4	–	3.1	ns	6	9	7	1,14
	t_{4+}	4	B	–					–			6	9		
	t_{11+}	11	B	–					–			9	6		
	t_{12+}	12	A	–					–			9	6		
Output Fall Time	t_{3-}	3	A	–	2.4	0.8	1.5	2.4	–	3.1	ns	6	9	7	1,14
	t_{4-}	4	B	–					–			6	9		
	t_{11-}	11	B	–					–			9	6		
	t_{12-}	12	A	–					–			9	6		

APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle – that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

Proper level shifting is acomplished by differentially driving the operational amplifier from the normally high outputs of the phase detector ($\overline{U}$ and $\overline{D}$). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The $\overline{U}$ and $\overline{D}$ outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering imbedded within the input network (Figure 2) may be very beneficial since the very narrow correctional pulses of the MC12040 would not normally be integrated by the amplifier. General design guides for calculating R1, R2, and C are included in the MC4044 data sheet. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of 0.016/0.16 = 0.1 radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 2). Phase error over temperature depends on how much the offending parameters drift. If better performance were desired, the "charge pump" concept of the MC4044 could be implemented and subsequent errors could be reduced considerably since offsets no longer enter the picture.

FIGURE 1 – TIMING DIAGRAM

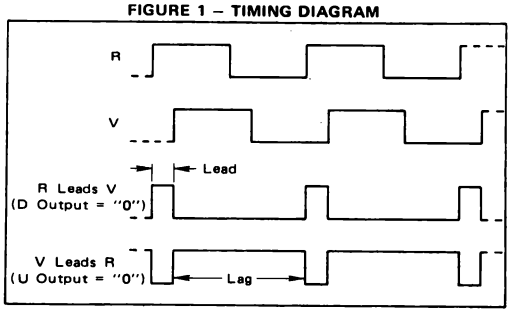
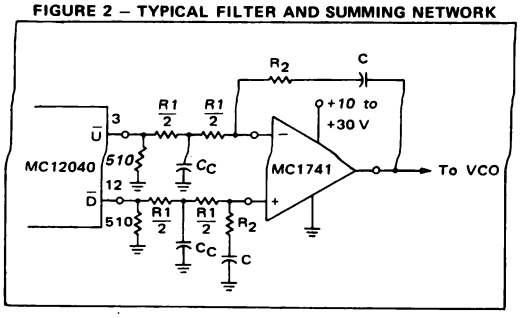


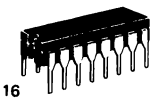
FIGURE 2 – TYPICAL FILTER AND SUMMING NETWORK



MC12060 • MC12560
MC12061 • MC12561

The MC12060/12560 and MC12061/12561 are designed for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and MTTL outputs.

- Frequency Range = 100 kHz to 2.0 MHz for MC12060/12560
  = 2.0 MHz to 20 MHz for MC12061/12561
- Temperature Range = -55°C to +125°C for MC12560, 61
  = 0°C to +70°C for MC12060, 61
- Single Supply Operation: +5.0 Vdc or -5.2 Vdc
- Three Outputs Available:
  1. Complementary Sine Wave (600 mVp-p typ)
  2. Complementary MECL
  3. Single Ended MTTL



16 1

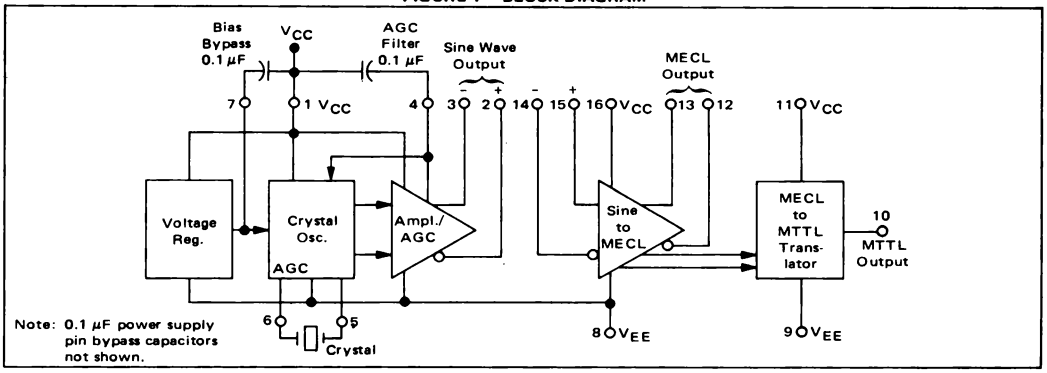
L SUFFIX
CERAMIC PACKAGE
CASE 620

16 1

P SUFFIX
PLASTIC PACKAGE
CASE 648

MC12060/MC12061 only.

FIGURE 1 – BLOCK DIAGRAM



TYPICAL CIRCUIT CONFIGURATIONS Note: 0.1 μF power supply pin bypass capacitors not shown.

FIGURE 2 – SINE WAVE OUTPUT

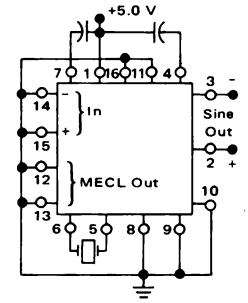


FIGURE 3 – MTTL OUTPUT

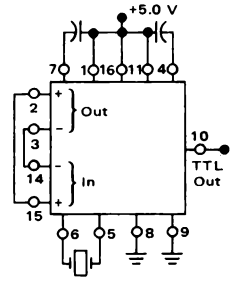


FIGURE 4 – MECL OUTPUT (+5.0 V Supply)

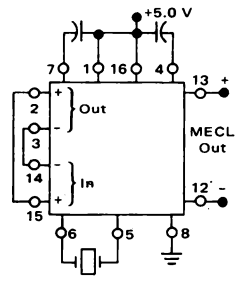
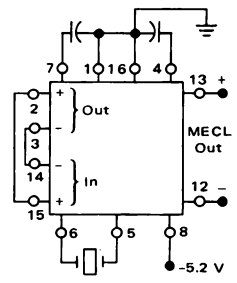


FIGURE 5 – MECL OUTPUT (-5.2 V Supply)

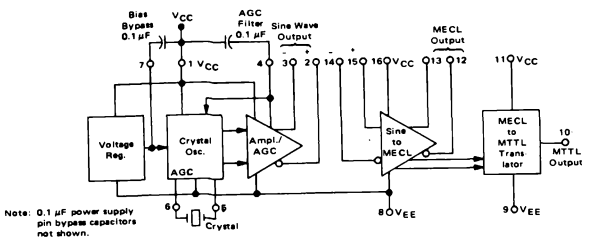


CRYSTAL REQUIREMENTS

Note: Start-up stabilization time is a function of crystal series resistance. The lower the resistance, the faster the circuit stabilizes.

Characteristic	MC12060/12560	MC12061/12561
Mode of Operation	Fundamental Series Resonance	
Frequency Range	100 kHz – 2.0 MHz	2.0 MHz – 20 MHz
Series Resistance, R1	Minimum at Fundamental	
Maximum Effective Resistance, $R_{E(max)}$	4 k ohms	155 ohms

ELECTRICAL CHARACTERISTICS

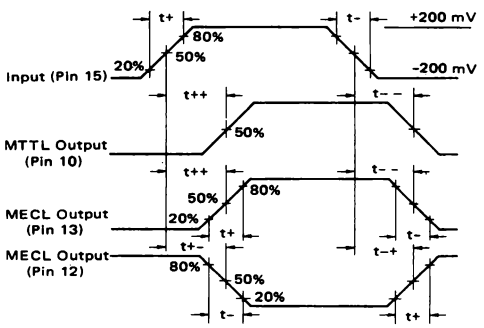


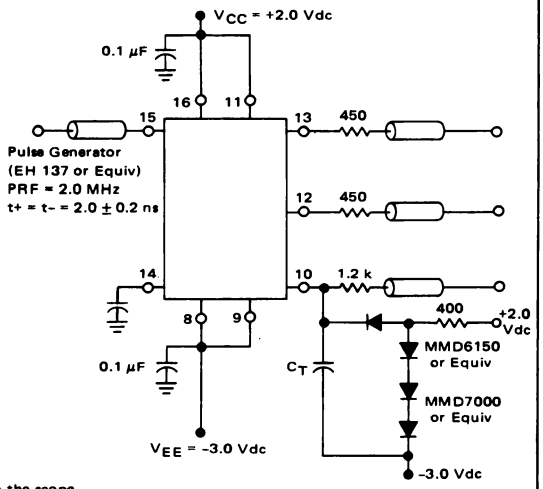
	@ Test Temperature	TEST VOLTAGE/CURRENT VALUES											
		Volts								mA			
		V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	V_{CC}	V_{CCH}	I_{OL}	I_{OH}	I_L
MC12560, MC12561	-55°C	4.07	3.18	3.72	3.49	4.0	4.5	5.0	5.5	16	-0.4	-2.5
	+25°C	4.19	3.21	3.90	3.52	4.0	4.5	5.0	5.5	16	-0.4	-2.5
	+125°C	4.37	3.25	4.03	3.60	4.0	4.5	5.0	5.5	16	-0.4	-2.5
MC12060, MC12061	0°C	4.16	3.19	3.86	3.51	4.0	4.75	5.0	5.25	16	-0.4	-2.5
	+25°C	4.19	3.21	3.90	3.52	4.0	4.75	5.0	5.25	16	-0.4	-2.5
	+75°C	4.28	3.23	3.96	3.55	4.0	4.75	5.0	5.25	16	-0.4	-2.5

Characteristic	Symbol	Pin Under Test	MC12560, MC12561 -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	MC12060, MC12061 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	V_{CC}	V_{CCH}	I_{OL}	I_{OH}	I_L	Gnd
Power Supply Drain Current – MC12060/12560	I_{CC}	1	–	–	13	16	19	–	–	–	–	13	16	19	–	–	mAdc	–	–	–	–	–	–	1	–	–	–	–	8
– MC12061/12561		1	–	–	18	23	28	–	–	–	–	18	23	28	–	–		–	–	–	–	–	–	1	–	–	–	–	8
		11	–	–	–	3.0	4.0	–	–	–	–	–	3.0	4.0	–	–		14	15	–	–	–	–	11,16	–	–	–	–	8,9
		16	–	–	13	16	19	–	–	–	–	13	16	19	–	–		–	–	–	–	–	–	16	–	–	–	–	8
Input Current	I_{INH}	14	–	–	–	–	250	–	–	–	–	–	–	250	–	–	μAdc	14	15	–	–	–	–	16	–	–	–	–	8
		15	–	–	–	–	250	–	–	–	–	–	–	250	–	–	μAdc	15	14	–	–	–	–	16	–	–	–	–	8
	I_{INL}	14	–	–	–	–	1.0	–	–	–	–	–	–	1.0	–	–	μAdc	15	–	–	–	–	–	16	–	–	–	–	8,14
		15	–	–	–	–	1.0	–	–	–	–	–	–	1.0	–	–	μAdc	14	–	–	–	–	–	16	–	–	–	–	8,15
Differential Offset Voltage	ΔV	4 to 7	–	–	40	–	325	–	–	–	–	40	–	325	–	–	mVdc	–	–	–	–	5,6	–	1	–	–	–	–	8
MC12060/12560		2 to 3	–	–	-220	0	+220	–	–	–	–	-300	0	+300	–	–		–	–	–	–	4	–		–	–	–	–	
MC12061/12561		2 to 3	–	–	-100	0	+100	–	–	–	–	-200	0	+200	–	–		–	–	–	–	4	–		–	–	–	–	
Output Voltage Level	V_{out}	2	–	–	–	3.5	–	–	–	–	–	–	3.5	–	–	–	Vdc	–	–	–	–	4	–	1	–	–	–	–	8
		3	–	–	–	3.5	–	–	–	–	–	–	3.5	–	–	–	Vdc	–	–	–	–	4	–	1	–	–	–	–	8
Logic "1" Output Voltage	V_{OH1}*	12	3.92	4.07	4.04	–	4.19	4.17	4.37	4.00	4.16	4.04	–	4.19	4.10	4.28	Vdc	14	15	–	–	–	16	–	–	–	–	12	8
		13	3.92	4.07	4.04	–	4.19	4.17	4.37	4.00	4.16	4.04	–	4.19	4.10	4.28	Vdc	15	14	–	–	–	16	–	–	–	–	13	8
	V_{OH2}	10	2.4	–	2.4	–	–	2.4	–	2.4	–	2.4	–	–	2.4	–	Vdc	15	14	–	–	–	11,16	–	–	–	10	–	8,9
Logic "0" Output Voltage	V_{OL1}*	12	2.97	3.39	3.00	–	3.44	3.04	3.50	2.98	3.43	3.00	–	3.44	3.02	3.47	Vdc	15	14	–	–	–	–	16	–	–	–	12	8
		13	2.97	3.39	3.00	–	3.44	3.04	3.50	2.98	3.43	3.00	–	3.44	3.02	3.47	Vdc	14	15	–	–	–	–	16	–	–	–	13	8
	V_{OL2}	10	–	0.5	–	–	0.5	–	0.5	–	0.5	–	–	0.5	–	0.5	Vdc	14	15	–	–	–	11,16	–	–	10	–	–	8,9
		10	–	0.5	–	–	0.5	–	0.5	–	0.5	–	–	0.5	–	0.5	Vdc	14	15	–	–	–	–	–	11,16	10	–	–	8,9
Logic "1" Threshold Voltage	V_{OHA}	12	3.90	–	4.02	–	–	4.15	–	3.98	–	4.02	–	–	4.08	–	Vdc	–	–	14	15	–	–	16	–	–	–	12	8
		13	3.90	–	4.02	–	–	4.15	–	3.98	–	4.02	–	–	4.08	–	Vdc	–	–	15	14	–	–	16	–	–	–	13	8
Logic "0" Threshold Voltage	V_{OLA}	12	–	3.41	–	–	3.46	–	3.52	–	3.45	–	–	3.46	–	3.49	Vdc	–	–	15	14	–	–	16	–	–	–	12	8
		13	–	3.41	–	–	3.46	–	3.52	–	3.45	–	–	3.46	–	3.49	Vdc	–	–	14	15	–	–	16	–	–	–	13	8
Output Short-Circuit Current	I_{OS}	10	20	60	20	–	60	20	60	20	60	20	–	60	20	60	mAdc	15	14	–	–	–	11,16	–	–	–	–	–	8,9,10

*Devices will meet standard MECL logic levels using V_{EE} = -5.2 Vdc and V_{CC} = 0.

FIGURE 6 – AC CHARACTERISTICS – MECL AND MTTL OUTPUTS





All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

Unused outputs are connected to a 50 Ω ±1% resistor to ground.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.

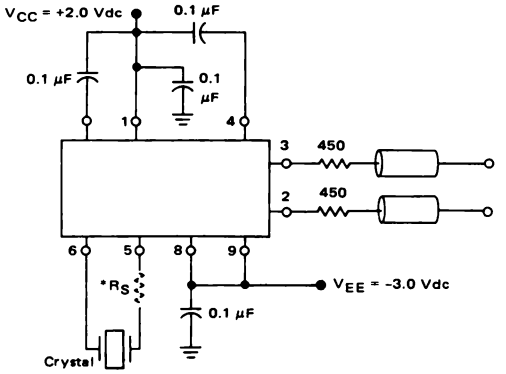
Characteristic	Symbol	Pin Under Test	MC12560, MC12561 -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	MC12060, MC12061 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse In	Pulse Out	+2.0 Vdc	-3.0 Vdc	Gnd
Propagation Delay	t_{15+10+}	10	–	30	–	17	25	–	30	–	22	–	17	25	–	27	ns	15	10	11,16	8,9	14
	t_{15-10-}	10	–	22	–	12	18	–	22	–	19	–	12	18	–	18			10			
	t_{15+12-}	12	–	5.0	–	4.3	5.5	–	6.0	–	5.2	–	4.3	5.5	–	5.8			12			
	t_{15-12+}	12	–	4.8	–	3.7	5.2	–	5.5	–	5.0	–	3.7	5.2	–	5.2			12			
	t_{15+13+}	13	–	4.6	–	4.0	5.0	–	5.4	–	4.8	–	4.0	5.0	–	5.2			13			
	t_{15-13-}	13	–	5.0	–	4.0	5.0	–	5.2	–	5.0	–	4.0	5.0	–	5.1			13			
Rise Time	t_{12+}	12	–	3.8	–	3.0	4.0	–	5.0	–	4.0	–	3.0	4.0	–	4.4	ns	15	12	11,16	8,9	14
	t_{13+}	13	–	3.8	–	3.0	4.0	–	5.0	–	4.0	–	3.0	4.0	–	4.4	ns	15	13	11,16	8,9	14
Fall Time	t_{12-}	12	–	3.8	–	3.0	4.0	–	4.5	–	4.0	–	3.0	4.0	–	4.0	ns	15	12	11,16	8,9	14
	t_{13-}	13	–	3.8	–	3.0	4.0	–	4.5	–	4.0	–	3.0	4.0	–	4.0	ns	15	13	11,16	8,9	14

FIGURE 7 – AC TEST CIRCUIT – SINE WAVE OUTPUT

Crystal – Reeves Hoffman Series Mode, Series Resistance Minimum at Fundamental
MC12060/12560:
f = 500 kHz
R_E = 1 k Ω
MC12061/12561:
f = 10 MHz
R_E = 5 Ω

*R_S – MC12060/12560 = 3 kΩ
MC12061/12561 = 150 Ω
R_S is inserted only for test purposes. When used with the above specified crystal, it guarantees oscillation with any crystal which has an equivalent series resistance ≤4 kΩ for MC12060/12560 and 155 Ω for MC12061/12561.

All output cables to the scope are equal lengths of 50 Ω coaxial cable. All unused cables must be terminated with a 50 Ω ±1% resistor to ground.
450 Ω resistor and the scope termination impedance constitute a 10:1 attenuator probe.



Characteristic	Pin Under Test	MC12560 MC12561 +25°C Min	MC12560 MC12561 +25°C Typ	MC12060 MC12061 +25°C Min	MC12060 MC12061 +25°C Typ	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW +2.0 Vdc	TEST VOLTAGE APPLIED TO PINS LISTED BELOW -3.0 Vdc
Sine Wave Amplitude								
MC12060/12560	2	600	675	500	650	mVp-p	1	8,9
	3	600	675	500	650			
MC12061/12561	2	700	750	650	750			
	3	700	750	650	750			

OPERATING CHARACTERISTICS

The MC12060/12560 and MC12061/12561 consist of three basic sections: an oscillator with AGC and two translators (Figure 1). Buffered complementary sine wave outputs are available from the oscillator section. The translators convert these sine wave outputs to levels compatible with MECL and/or MTTL.

Series mode crystals should be used with the oscillator. If it is necessary or desirable to adjust the crystal frequency, a reactive element can be inserted in series with the crystal – an inductor to lower the frequency or a capacitor to raise it. When such an adjustment is necessary, it is recommended that the crystal be specified slightly lower in frequency and a series trimmer capacitor be added to bring the oscillator back on frequency. As the oscillator frequency is changed from the natural resonance of the crystal, more and more dependence is placed on the external reactance, and temperature drift of the trimming components then affects overall oscillator performance.

The MC12060/12560 and MC12061/12561 are designed to operate from a single supply – either +5.0 Vdc or -5.2 Vdc. Although each translator has separate V_{CC} and V_{EE} supply pins, the circuit is NOT designed to operate from both voltage levels at the same time. The separate V_{EE} pin from the MTTL translator helps minimize transient disturbance. If neither translator is being used, all unused pins (9 thru 16) should be connected to V_{EE} (pin 8). With the translators not powered, supply current drain is typically reduced from 35 mA to 16 mA for the MC12060/12560, and from 42 mA to 23 mA for the MC12061/12561.

Frequency Stability

Output frequency of different oscillator circuits (of a given device type number) will vary somewhat when used with a given test setup, however the variation should be within approximately ±0.001% from unit to unit.

Frequency variations with temperature (independent of the crystal, which is held at 25°C) are small – about -0.08 ppm/°C for MC12061/12561 operating at 8.0 MHz, and about -0.16 ppm/°C for MC12060/12560 operating at 1.0 MHz (see Figure 8).

Signal Characteristics

The sine wave outputs at either pin 2 or pin 3 will typically range from 800 mVp-p (no load) to 500 mVp-p (120 ohm ac load). Approximately 500 mVp-p can be provided across 50 ohms by slightly increasing the dc current in the output buffer by the addition of an external resistor (680 ohms) from pin 2 or 3 to ground, as shown in Figure 9. Frequency drift is typically less than 0.0003% when going from a high-impedance load (1 megohm, 15 pF) to the 50-ohm load of Figure 9. The dc voltage level at pin 2 or 3 is nominally 3.5 Vdc with V_{CC} = +5.0 Vdc.

Harmonic distortion content in the sine wave outputs is crystal as well as circuit dependent. The largest harmonic (third) will usually be at least 15 dB down from the fundamental. The harmonic content is approximately load independent except that the higher harmonic levels (greater than the fifth) are increased when the MECL translator is being driven.

Typically, the MECL outputs (pins 12 and 13) will drive up to five gates, as defined in Figure 10, and the MTTL output (pin 10) will drive up to ten gates, as defined in Figure 11.

Noise Characteristics

Noise level evaluation of the sine wave outputs using the circuit of Figure 12, with operation at 1.0 MHz for MC12060/12560 or 9.0 MHz for MC12061/12561, indicates the following characteristics:

1. Noise floor (200 kHz from oscillator center frequency) is approximately -122 dB when referenced to a 1.0 Hz bandwidth. Noise floor is not sensitive to load conditions and/or translator operation.
2. Close-in noise (100 Hz from oscillator center frequency) is approximately -88 dB when referenced to a 1.0 Hz bandwidth.

FIGURE 8 – FREQUENCY SHIFT versus TEMPERATURE

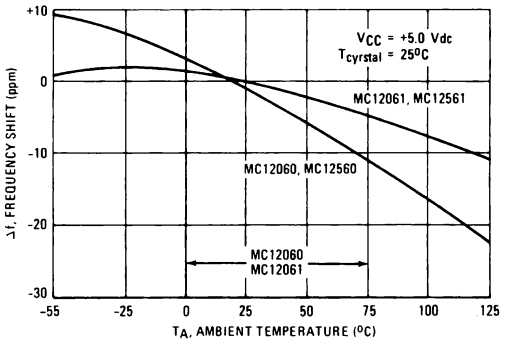
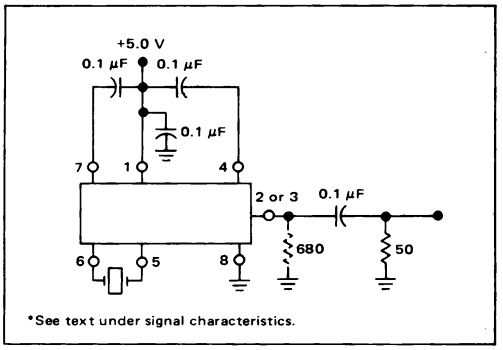


FIGURE 9 – DRIVING LOW-IMPEDANCE LOADS



*See text under signal characteristics.

FIGURE 10 – MECL TRANSLATOR LOAD CAPABILITY

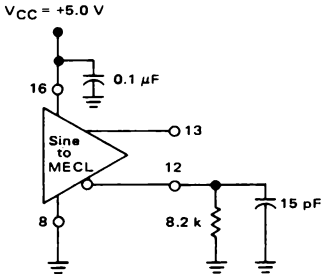


FIGURE 11 – MTTL TRANSLATOR LOAD CAPABILITY

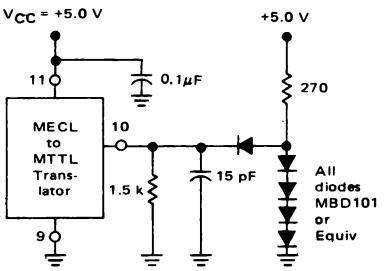
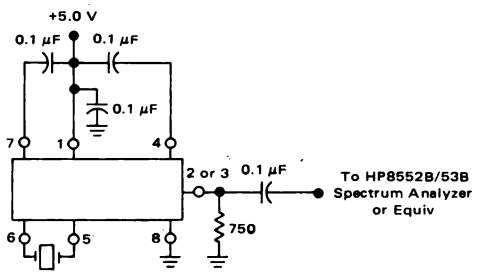


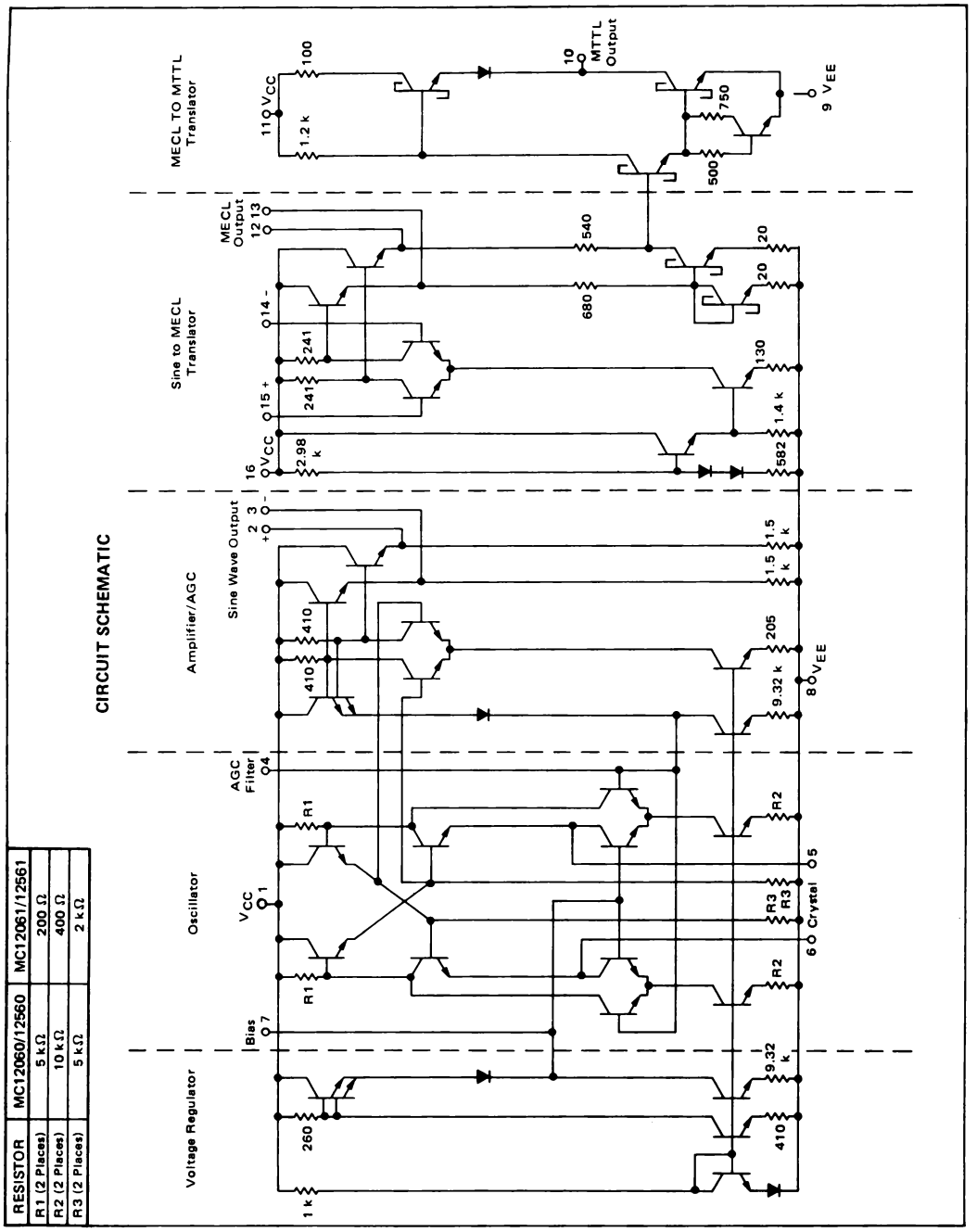
FIGURE 12 – NOISE MEASUREMENT TEST CIRCUIT



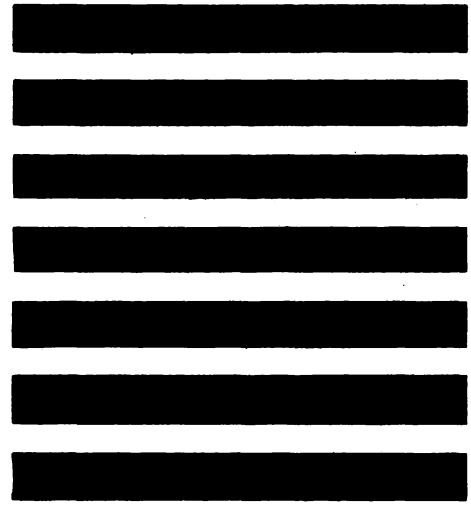
ANALYZER SETTING

Measurement	Sweep	Bandwidth	Video Filter
Noise Floor	50 kHz/div	10 kHz	10 Hz
Close-In Noise	20 kHz/div	10 Hz	10 Hz

CIRCUIT SCHEMATIC



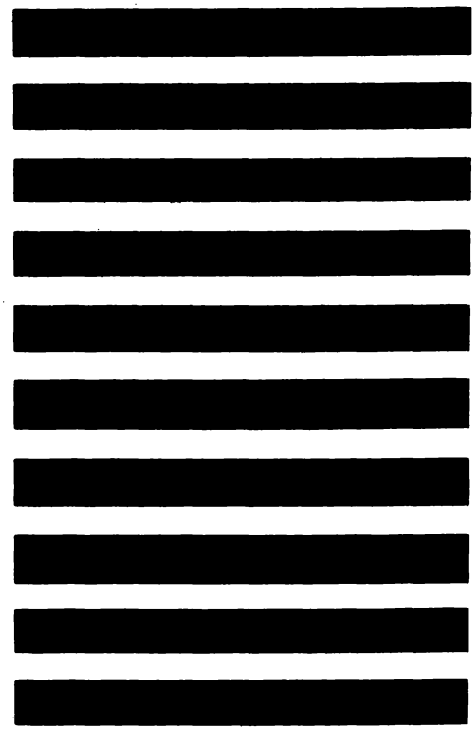
RESISTOR	MC12060/12560	MC12061/12561
R1 (2 Places)	5 kΩ	200 Ω
R2 (2 Places)	10 kΩ	400 Ω
R3 (2 Places)	5 kΩ	2 kΩ



MECL

INTEGRATED CIRCUITS

MIL-M-38510 PROGRAM



MOTOROLA MIL-M-38510 PROGRAM

— the ultimate in quality assurance for integrated circuits

Motorola is the industry's pioneer manufacturer of high-reliability integrated circuits, having been the first company to be qualified as a MIL-M-38510 approved facility by the Defense Electronics Supply Center of the Department of Defense early in 1971. Motorola's extensive experience in high-reliability military and manned spacecraft programs such as Apollo, Minuteman and Safeguard, coupled with an investment of millions of dollars for research and development, has resulted in the ultimate in quality assurance for integrated circuits: the MOTOROLA MIL-M-38510 PROGRAM.

This comprehensive program is structured to provide an environment in which proven methods of manufacturing, quality assurance, monitoring, screening and testing can thrive — to give you **the most reliable product on the market today** — and to give it to you **fast!**

The MOTOROLA MIL-M-38510 PROGRAM is designed to support a broad base of test and evaluation programs for micro-electronic devices: materials, workmanship, performance capabilities, identification and processing — applied to all Motorola standard integrated circuit product, with appropriate levels of reliability. This product can be ordered in accordance with MIL-M-38510 JAN-**Qualified** standards or to the lower-cost, but similar hi-rel specifications designated as MIL-M-38510 JAN-**Processing.** (See ordering information.)

The MOTOROLA MIL-M-38510 PROGRAM is designed to facilitate delivery and to minimize specification preparation time. Beginning with a nucleus of popular IC types from our high-volume lines, the program is continually adding more devices to the list of MIL-M-38510 JAN-**Qualified** products.

Because it is a "standard" hi-rel program, the MOTOROLA MIL-M-38510 PROGRAM aids in reducing the high costs and delivery delays normally associated with "custom" hi-rel programs in the past.

It is a functional, operating program, based on the Military's own long-range objective to improve and demonstrate integrated circuit reliability, and is designed to provide hi-rel customers with the finest in quality, reliability and performance — fast!

THE MOTOROLA MIL-M-38510 PROGRAM OFFERS YOU THESE BENEFITS:

1. Standardization of environmental and electrical test procedures
2. Less specification writing required
3. Less time required in negotiating specifications
4. Fast delivery
5. Lower costs

MIL-M-38510 *processed* devices are offered by Motorola in the MECL 10,000 family for both commercial and military temperature range use. Hermetically-sealed ceramic dual in line and flat packages are available. Industry-wide "slash-specs" are being issued, and when available, will permit Motorola to provide MIL-M-38510 *qualified* MECL 10,000 devices.

Most devices in the MECL II and MECL III families can also be processed to meet MIL-M-38510 requirements.

Motorola's MIL-M-38510 Program supplants our former high reliability "Checkmate" program. You are invited to inquire directly to Motorola for price and delivery quotations on your MIL-M-38510 MECL device requirements.

MECL MIL-M-38510 SELECTOR

MECL 10,000	Rated Temperature Range	Package Styles Available
MC10,0XX	-30°C/+85°C	–
MC10,1XX		L
MC10,2XX		L
MC10,3XX		–
MC10,4XX	-55°C/+125°C	–
MC10,5XX		L,F
MC10,6XX		L,F
MC10,7XX		
MECL III		
MC16XX	-30°C/+85°C	L,F

THE MOTOROLA MIL-M-38510 PROGRAM

Under this program, Motorola integrated circuits may be procured to the specifications of MIL-M-38510 and to four levels of processing which meet the screening requirements of MIL-STD-883.

MIL-M-38510 JAN-QUALIFIED PRODUCT

Class A	Class B	Class C

JAN-QUALIFIED DEVICE MARKINGS

JM38510/XXXXXAXX	JM38510/XXXXXBXX	JM38510/XXXXXCXX

JAN QUALIFIED

1. **G.S.I. (Government Source Inspection) provided upon request.**
2. **Must be manufactured in a Government-approved facility.**
3. **Product inventoried in distributor and OEM warehouses.**

Examples of MIL-M-38510 JAN-**Qualified** markings:

	Linear	Digital
DEVICE:	MC1741BCBJ	MC5400BCBJ
ORDER:	MC1741BCBJ	MC5400BCBJ
MARKING:	JM38510/10101BCB	JM38510/00104BCB

HOW TO ORDER MIL-M-38510 JAN-QUALIFIED PRODUCT

Basic Numbering Parameters — Example: JM38510/XXXXXBCB

J	M38510	/XXX	XX	B	C	B
(1)	(2)	(3)	(4)	(5)	(6)	(7)

(1) = J — This indicates a qualified device.
(2) = M38510 — The military designator.
(3) = /XXX — This three-digit number signifies the detail specification in which the device type is found. The detail specifications, also referred to as "slash specs," generally contain more than one device type and are written for various generic groupings (i.e., TTL NAND Gates, TTL NAND Buffers, TTL Flip-Flops, Op Amps, Voltage Regulators, etc.)
(4) = XX — This two-digit number identifies the device type within the detail specification.
(5) = B — This is a single letter and specifies the device class per MIL-M-38510 and will be class A, B or C.
(6) = Case Outline. (See listings in adjacent column).
(7) = Lead finish. (See listings in adjacent column).

The Motorola equivalent of the JAN M38510 part number is as shown in the following example and should be referenced when ordering your specific device requirement.

MCXXXX	BCB	J
(1)	(2)	(3)

1. The MCXXXX designates the Motorola source device type.
2. The first three letters after the part type have the same meaning and order as in the JAN part numbering system. This will simplify your cross-referencing.
3. J, which is the last letter in the part number, designates a JAN-qualified device.

Case outline and lead finish designations are common to both JAN Qualified and JAN Processed devices:

QUALIFIED # (6) PROCESSED # (3)

C — This is a single letter and specifies the package or case outline. A list of the currently-defined package types (the letters define the same case outline for all detail specifications) is shown below:

CASE OUTLINE DESIGNATOR	CASE OUTLINE
*A	— ¼" x ¼" flat pack, 14-pin
B	— ⅛" x ¼" flat pack, 14-pin
C	— ¼" x ¾" dual-in-line, 14-pin
*D	— ¼" x ⅜" flat pack, 14-pin
E	— ¼" x ¾" dual-in-line, 16-pin
F	— ¼" x ⅜" flat pack, 16-pin
G	— 8-lead can
H	— ¼" x ¼" flat pack, 10-lead
I	— 10-lead can
J	— ½" x 1¼" dual-in-line, 24-pin
K	— ⅜" x ½" flat pack, 24-pin
Z	— ¼" x ½" flat pack, 24-pin

— A and D outlines are interchangeable

MIL-M-38510 JAN-PROCESSED PRODUCT

Class A **Class B** **Class C** **Class D**

JAN-PROCESSED DEVICE MARKINGS

MC38510/XXXXAXXM MC38510/XXXXBXXM MC38510/XXXXCXXM MC38510/XXXXDXXM
MC38510/XXXXAXXS MC38510/XXXXBXXS MC38510/XXXXCXXS MC38510/XXXXDXXS

JAN PROCESSED

1. **No G.S.I. provided.**
2. **Government-approved facility not required.**
3. **Product supplied with MIL-M-38510 electricals will be designated by an "M" suffix.**
4. **Product supplied with Motorola standard data sheet electricals will be designated by an "S" suffix.**
5. **Devices will be manufactured using design and processing guidelines contained in MIL-M-38510.**
6. **Inventories will be maintained prior to burn-in and final electrical tests.**

Examples of MIL-M-38510 JAN-**Processed** markings:

Linear

DEVICE:	MC1741BCB (M or S)
ORDER:	MC1741BCB (M or S)
MARKINGS:	MC38510/1741BCB (M or S)

Digital

DEVICE:	MC5400BCB (M or S)
ORDER:	MC5400BCB (M or S)
MARKINGS:	MC38510/5400BCB (M or S)

QUALIFIED #(7) PROCESSED #(4)

B — This is a single letter and specifies the finish to be used on the package leads. There are three types of lead finishes which are acceptable for JAN product. They are:

LEAD FINISH SYMBOL	LEAD FINISH
A	**— Kovar or Alloy 42, with hot solder dip**
B	**— Kovar or Alloy 42, with bright acid tin plate**
C	**— Kovar or Alloy 42, with gold plate**

Note: For other Motorola standard packaging, not currently identified in MIL-M-38510, contact your Motorola representative.

HOW TO ORDER MIL-M-38510 JAN-PROCESSED PRODUCT

EXAMPLE: If you wish to enter an order for an MCXXXX Class B device in a 14-pin, dual-in-line ceramic package with the lead finish to be tin plate and electrically tested to Motorola's standard data sheet electricals, the order would be entered as follows:

MCXXXX	**B**	**C**	**B**	**S**
(1)	(2)	(3)	(4)	(5)

(1) = Motorola device type.
(2) = B — This is a single letter and specifies the device class per MIL-M-38510 for Classes A, B and C. Class D is an added Motorola JAN processing class and is the same as the MIL-M-38510 Class B except for the differences shown in the following screening procedures table.
(3) = Case Outline. (See listings in adjacent column).
(4) = Lead finish. (See listings in adjacent column).
(5) = S — This is a single letter and specifies the electrical specifications to which the device is to be screened during electrical test and will be either an S or M. "S" specifies the use of Motorola standard data sheet electricals. "M" specifies the use of JAN slash-sheet electricals where they exist.

Electrical Test Symbols	Test Level
S	**— Motorola standard data sheet electricals**
M	**— JAN slash-sheet electricals**

SCREENING PROCEDURES

(To MIL-STD-883 Requirements)

This program establishes screening procedures for total lot screening of integrated circuits to assist in achieving levels of quality and reliability commensurate with the intended application. In recognition of the fact that the level of screening has a direct impact on the cost of the product as well as its quality and reliability, four standard levels of screening are provided to coincide with four device classes or levels of product assurance.

Flexibility is provided in the choice of conditions and stress levels to provide screens, tailored to a particular product or application. Selection of a level **better** than that required for the specific product and application will, of course, result in unnecessary expense. A level **less** than that required will result in an unwarranted risk that reliability and other requirements will not be met. For general hi-rel applications, the Class B screening level should be considered.

	CLASS A		CLASS B		CLASS C		CLASS D	
SCREEN	METHOD	RQMT	METHOD	RQMT	METHOD	RQMT	METHOD	RQMT
Internal Visual (Precap)	2010 Cond A and 38510	100%	2010 Cond B and 38510	100%	2010 Cond B and 38510	100%	2010 Cond B and 38510	100%
Stabilization Bake	1008 24 hrs min, test condition C	100%	1008, 24 hrs min, test condition C	100%	1008, 24 hrs min, test condition C	100%	1008, 24 hrs min, test condition C	100%
Thermal Shock	1011, Cond A	100%		—		—		—
Temperature Cycling	1010, Cond C	100%	1010, Cond C	100%	1010 Cond C	100%	1010, Cond C	100%
Mechanical Shock	2002 Cond F One Shock in Y_1 plane only **or** 5 shocks at Cond B in Y_1 plane	100%		—		—		—
Constant Acceleration	2001 Cond E (min) in Y_1 plane then Y_1 plane	100%	2001 Cond E (min) Y_1 plane	100%	2001 Cond E (min) Y_1 plane	100%	2001 Cond E (min) Y_1 plane	100%
Seal (a) Fine (b) Gross	1014	100%	1014	100%	1014	100%	1014	100%
Interim Electrical Parameters	JAN slash-sheet electrical specification unless otherwise designated	100%	JAN slash-sheet electrical specifications unless otherwise designated	100%		—	Motorola stand. data sheet electrical specs unless otherwise indicated	100%
Burn-in test	1015 240 hrs @ 125°C min	100%	1015 168 hrs @ 125°C min	100%		—	1015 168 hrs @ 125°C min	100%
Interim Electricals	JAN slash-sheet electrical specifications unless otherwise designated	100%						
Reverse Bias Burn-in	1015 Cond A or C 72 hrs at 150°C min	100%						
Final Electrical tests (a) Static tests (1) 25°C (Subgroup 1 table 1 5005)	JAN slash-sheet electrical specifications unless otherwise designated	100%	JAN slash-sheet electrical specifications unless otherwise designated	100%	JAN slash-sheet electrical specifications unless otherwise designated	100%	Motorola stand. data sheet electrical specs unless otherwise indicated	100%
(2) Max and min rated op. temperature (subgroups 2 and 3 table 1, 5005)		100%		100%		—		—
(b) Dynamic tests and/or switching tests 25°C (subgroup 4 and 9 table 1, 5005)		100%		100%		—		—
(C) Functional test 25°C (subgroup 7 table 1, 5005)		100%		100%		100%		100%
Radiographic	2012	100%		—		—		—
Qualification or quality conformance inspection	5005 Class A	per 38510 *	5005 Class B	per 38510 *	5005 Class C	per 38510 *	5005 Class B	*
External Visual	2009	100%	2009	100%	2009	100%	2009	100%

* Group A per 5005. Generic data available for groups B & C on devices produced to Class B, C, D for JAN processed (from JAN program)