Volume 2

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- EIA Registered Type Numbers
  1N5000 and 2N5000 and up
  3N . . . and 4N . . . Type Numbers

MOTOROLA Semiconductor Products Inc.

THE SEMICONDUCTOR DATA LIBRARY

SERIES A
VOLUME II

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VOLUME II

This volume contains complete data sheets for Motorola-manufactured devices with EIA registered type numbers from 1N5000 and 2N5000 and up, as well as those with 3N . . . and 4N . . . type numbers. Data sheets are in numerical sequence according to device type number except for those data sheets that cover several devices with different type numbers. The numerical index in front of the book permits the user to quickly locate the page number of the data sheet for any device characterized in the book.

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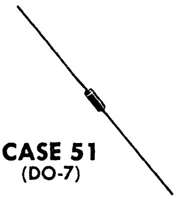
3N126		2-634
3N128		2-638
3N140		2-642
3N155,A		2-644
3N156,A		2-644
3N157,A		2-648
3N158,A		2-648
3N169		2-652
3N170		2-652
3N171		2-652
3N209		2-656
3N210		2-656
4N25		2-662
4N26		↓
4N27		↓
4N28		2-662
4N29		2-666
4N30		↓
4N31		↓
4N32		↓
4N33		2-666

1N... JEDEC REGISTERED DEVICE SPECIFICATIONS

1N5139,A thru 1N5148,A (SILICON)



CASE 51
(DO-7)

Polarity band on
cathode end

Silicon voltage-variable capacitance diodes, designed for electronic tuning and harmonic-generation applications, and providing solid-state reliability to replace mechanical tuning methods.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	60	Vdc
Forward Current	I_F	250	mAdc
RF Power Input†	P_{in}†	5.0	Watts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Device Dissipation @ T_C = 25°C Derate above 25°C	P_C	2.0 13.3	Watts mW/°C
Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

† The RF power input rating assumes that an adequate heat sink is provided.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic – All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	B_{VR}	60	70	—	Vdc
Reverse Voltage Leakage Current	V_R = 55 Vdc, T_A = 25°C V_R = 55 Vdc, T_A = 150°C	I_R	— —	— —	0.02 20	μAdc
Series Inductance	f = 250 MHz, L ≈ 1/16"	L_S	—	5.0	—	nH
Case Capacitance	f = 1 MHz, L ≈ 1/16"	C_C	—	0.25	—	pF
Diode Capacitance Temperature Coefficient	V_R = 4 Vdc, f = 1 MHz	TC_C	—	200	300	ppm/°C

	C_T, Diode Capacitance V_R = 4 Vdc, f = 1 MHz pF			Q, Figure of Merit V_R = 4 Vdc, f = 50 MHz	α V_R = 4 Vdc, f = 1 MHz		TR, Tuning Ratio C_4/C_{60} f = 1 MHz	
Device	Min	Typ	Max	Min	Min	Typ	Min	Typ
1N5139	6.1	6.8	7.5	350	0.37	0.40	2.7	2.9
1N5139A	6.5	6.8	7.1	350	0.37	0.40	2.7	2.9
1N5140	9.0	10.0	11.0	300	0.38	0.41	2.8	3.0
1N5140A	9.5	10.0	10.5	300	0.38	0.41	2.8	3.0
1N5141	10.8	12.0	13.2	300	0.38	0.41	2.8	3.0
1N5141A	11.4	12.0	12.6	300	0.38	0.41	2.8	3.0
1N5142	13.5	15.0	16.5	250	0.38	0.41	2.8	3.0
1N5142A	14.3	15.0	15.7	250	0.38	0.41	2.8	3.0
1N5143	16.2	18.0	19.8	250	0.38	0.41	2.8	3.0
1N5143A	17.1	18.0	18.9	250	0.38	0.41	2.8	3.0
1N5144	19.8	22.0	24.2	200	0.43	0.45	3.2	3.4
1N5144A	20.9	22.0	23.1	200	0.43	0.45	3.2	3.4
1N5145	24.3	27.0	29.7	200	0.43	0.45	3.2	3.4
1N5145A	25.7	27.0	28.3	200	0.43	0.45	3.2	3.4
1N5146	29.7	33.0	36.3	200	0.43	0.45	3.2	3.4
1N5146A	31.4	33.0	34.6	200	0.43	0.45	3.2	3.4
1N5147	36.1	39.0	42.9	200	0.43	0.45	3.2	3.4
1N5147A	37.1	39.0	40.9	200	0.43	0.45	3.2	3.4
1N5148	42.3	47.0	51.7	200	0.43	0.45	3.2	3.4
1N5148A	44.7	47.0	49.3	200	0.43	0.45	3.2	3.4

FIGURE 1 — DIODE CAPACITANCE versus REVERSE VOLTAGE

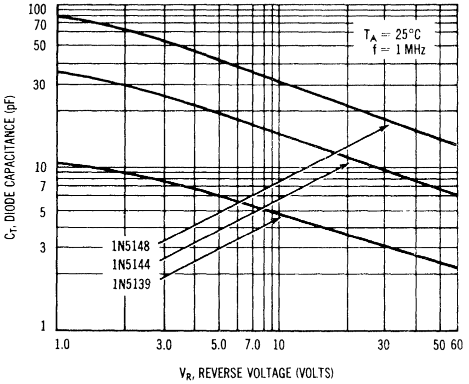


FIGURE 2 — FIGURE OF MERIT versus REVERSE VOLTAGE

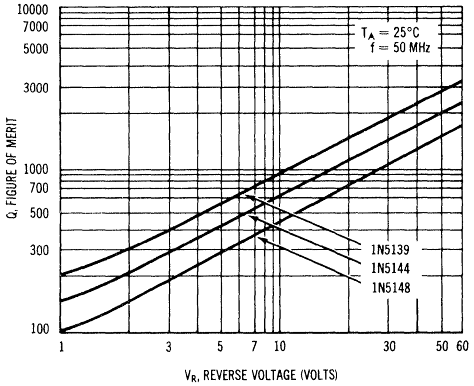


FIGURE 3 — NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE

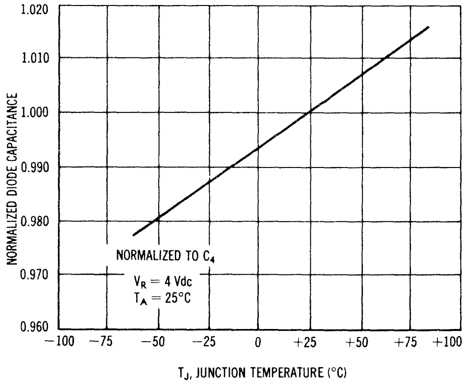


FIGURE 4 — NORMALIZED FIGURE OF MERIT versus JUNCTION TEMPERATURE

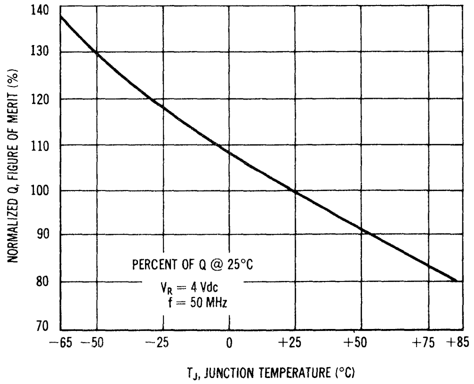


FIGURE 5 — REVERSE CURRENT versus REVERSE BIAS VOLTAGE

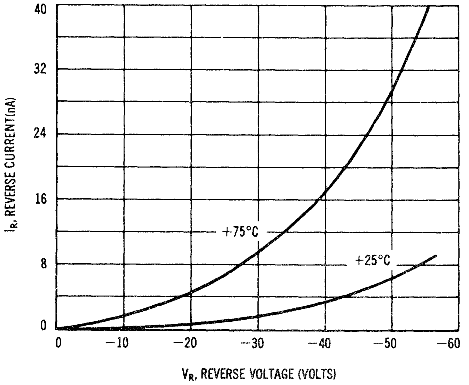
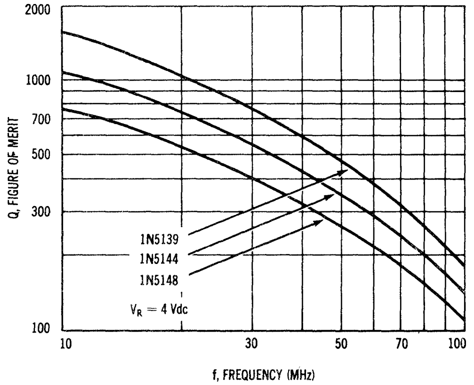


FIGURE 6 — FIGURE OF MERIT versus FREQUENCY



1N5149 (SILICON)
1N5150

The RF Line

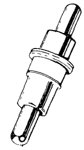
SILICON HIGH FREQUENCY STEP-RECOVERY POWER VARACTORS

. . . designed for 100 MHz to 2 GHz harmonic-generation applications with output power to 25 Watts at 1 GHz.

- Specified f_{in} = 0.5 GHz, f_{out} = 1.0 GHz Characteristics –
  Input Power = 20 W – 1N5149
  = 37 W – 1N5150
  Output Power = 11 W – 1N5149
  = 24 W – 1N5150
  Efficiency = 55% – 1N5149
  = 65% – 1N5150
- Characterized with Doubling, Tripling and Quadrupling Curves
- 100% Functionally Tested as a Doubler @ 1.0 GHz

24 W – 1 GHz – 1N5150
11 W – 1 GHz – 1N5149

STEP-RECOVERY POWER VARACTOR DIODES



MAXIMUM RATINGS

Rating	Symbol	1N5149	1N5150	Unit
Reverse Voltage	V_R	80		Volts
Forward Current	I_F	1.0		Amp
RF Power Input	P_{in}	25	40	Watts
Total Device Dissipation @ T_A = 75°C Derate above 75°C	P_D	10 0.08	14 0.11	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

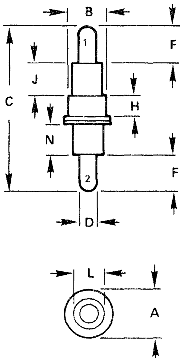
Characteristic	Symbol	1N5150 Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	9.0	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	BV_R	80	90	–	Vdc
Reverse Current	I_R				μAdc
(V_R = 70 Vdc)		–	–	2.0	
(V_R = 70 Vdc, T_A = 150°C)		–	–	100	
Diode Capacitance (V_R = 6.0 Vdc, f = 1.0 MHz)	C_T	5.0	11.5	20	pF
Figure of Merit (V_R = 6.0 Vdc, f = 50 MHz)	Q	–	800	–	–

FUNCTIONAL TEST (Figure 3)

Characteristic	Symbol	Min	Typ	Max	Unit
RF Power Output	P_{out}				Watts
(P_{in} = 20 W, f_{in} = 0.5 GHz, f_{out} = 1.0 GHz) 1N5149		11	–	–	
(P_{in} = 37 W, f_{in} = 0.5 GHz, f_{out} = 1.0 GHz) 1N5150		24	25	–	
Doubler Efficiency	η				%
(P_{in} = 20 W, f_{in} = 0.5 GHz, f_{out} = 1.0 GHz) 1N5149		55	–	–	
(P_{in} = 37 W, f_{in} = 0.5 GHz, f_{out} = 1.0 GHz) 1N5150		65	68	–	



STYLE 1:
PIN 1 CATHODE
2. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.72	6.22	0.225	0.245
B	4.70	4.95	0.185	0.195
C	19.18	20.19	0.755	0.795
D	2.24	2.49	0.088	0.098
F	4.57	4.83	0.180	0.190
H	2.29	2.54	0.090	0.100
J	3.68	4.06	0.145	0.160
L	3.94	4.19	0.155	0.165
N	3.18	3.43	0.125	0.135

CASE 47-01

OUTPUT POWER versus OUTPUT FREQUENCY

1N5149

FIGURE 1A – DOUBLING (X2)

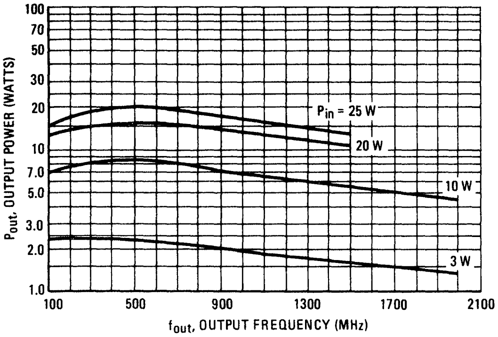


FIGURE 1B – TRIPLING (X3)

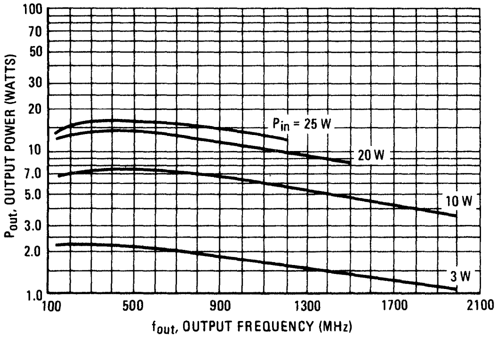
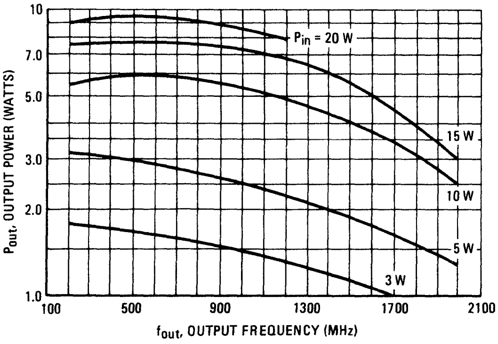


FIGURE 1C – QUADRUPLING (X4)



1N5150

FIGURE 2A – DOUBLING (X2)

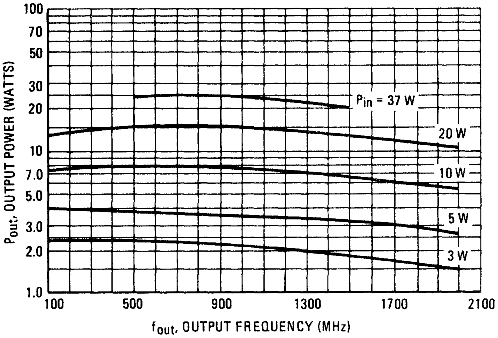


FIGURE 2B – TRIPLING (X3)

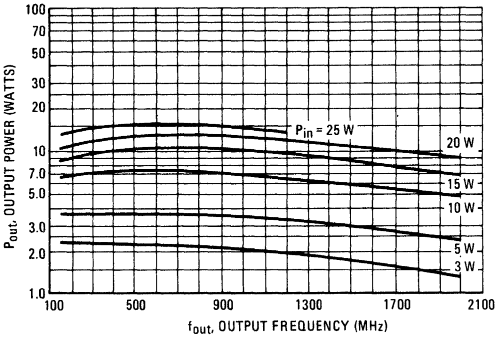


FIGURE 2C – QUADRUPLING (X4)

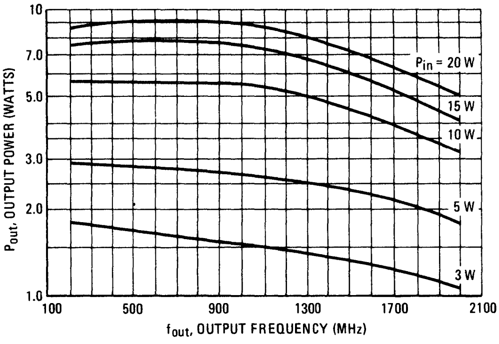
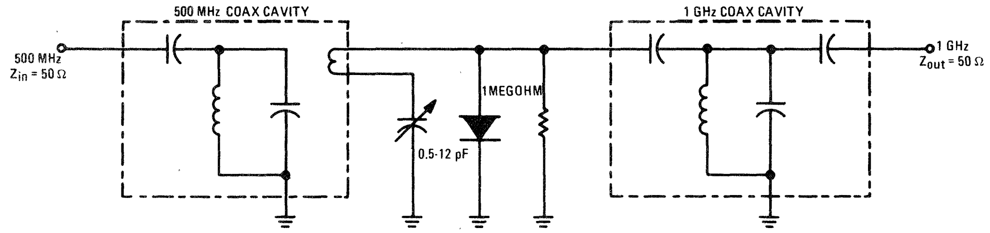
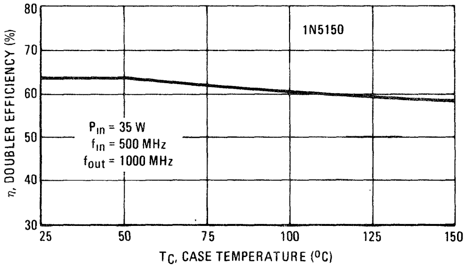
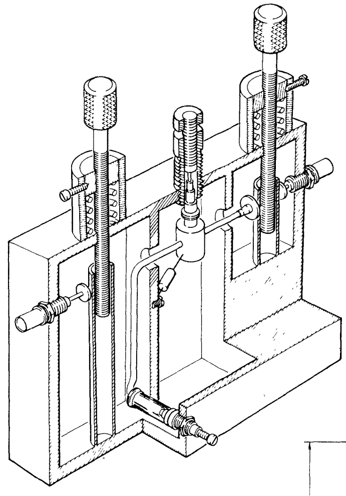
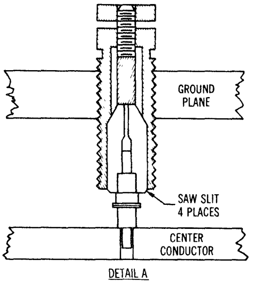


FIGURE 3 – HARMONIC DOUBLER EFFICIENCY TEST CIRCUIT









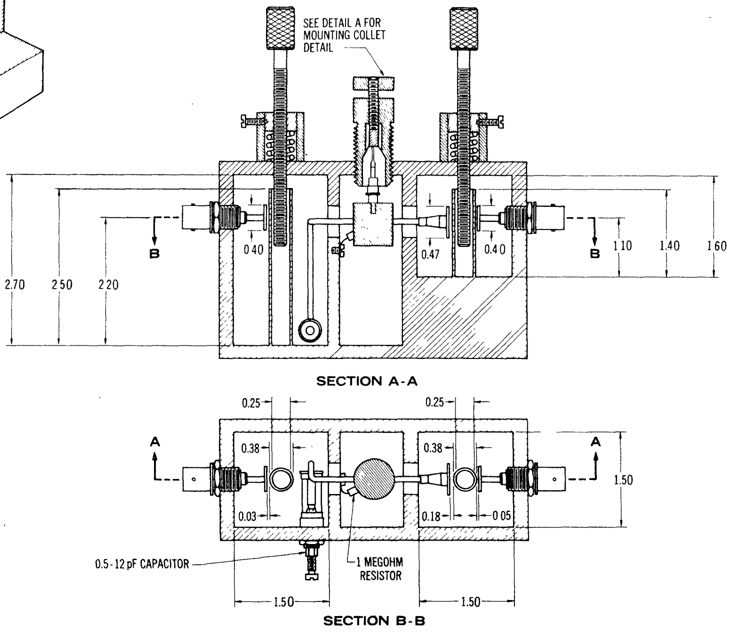


FIGURE 4 – LINEARITY CHARACTERISTIC WITHOUT RETUNING

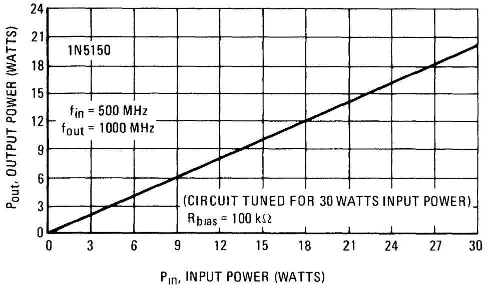
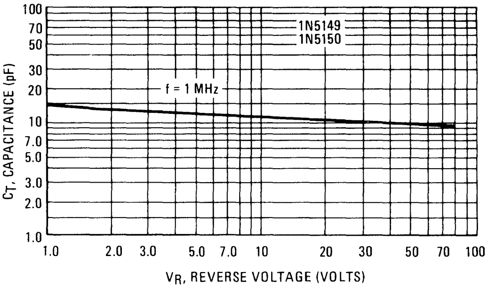


FIGURE 5 – CAPACITANCE versus REVERSE VOLTAGE



APPLICATION NOTE

VARACTOR CHARACTERISTICS

The 1N5149 and 1N5150 varactors are designed for RF power inputs up to 25 watts and 40 watts respectively. These devices exhibit high multiplication efficiency at output frequencies as low as 0.1 GHz and as high as 2.0 GHz. Power handling capability is stressed in device construction, but high efficiency is maintained with power inputs as low as 3 watts. At output frequencies below 600 MHz, where input power beyond the capability of these devices is needed, the 1N4386 and 1N4387 varactors are recommended.

The 1N5149 and 1N5150 power varactors are epitaxial-passivated, diffused-junction varactors with a unique impurity profile. The significance of the impurity profile is the enhancement of snap-off in the current waveform, due to the fast recovery of stored minority carriers after a forward-voltage surge. Dependence upon nonlinearity rather than capacity variation with reverse voltage results in high efficiency at high power levels and considerably less distortion of multiplied amplitude-modulated signals.

The approximate input and output impedances of the varactors, when operated as doublers, triplers (with idler), and quadruplers (with idler), are predicted from the formulas below. These equations are based on computer-determined approximations and tables.[1]

Doubler (High Level Drive)

$$R_{in} \approx \frac{42}{C_{-6}f_{in}} \qquad C_{eff\,in} \approx \frac{C_{min}}{0.5}$$

$$R_{out} \approx \frac{41.5}{C_{-6}f_{in}} \qquad C_{eff\,out} \approx \frac{C_{min}}{0.5}$$

where: R_{in} = the input resistance in ohms
C_{-6} = varactor capacitance in pF at −6 volts
f_{in} = input frequency in GHz
R_{out} = output resistance in ohms
$C_{eff\,in}$ = effective input capacitance in pF
$C_{eff\,out}$ = effective output capacitance in pF
C_{min} = capacitance at voltage breakdown, in pF

Tripler (High Level Drive)

$$R_{in} \approx \frac{55}{C_{-6}f_{in}} \qquad C_{eff\,in} \approx \frac{C_{min}}{0.5}$$

$$R_{out} \approx \frac{20}{C_{-6}f_{in}} \qquad C_{eff\,out} \approx \frac{C_{min}}{0.5}$$

Quadrupler (High Level Drive)

$$R_{in} \approx \frac{55}{C_{-6}f_{in}} \qquad C_{eff\,in} \approx \frac{C_{min}}{0.5}$$

$$R_{out} \approx \frac{20}{C_{-6}f_{in}} \qquad C_{eff\,out} \approx \frac{C_{min}}{0.5}$$

These formulas show values useful for initial circuit design, but they differ from final optimum values in some cases.

GENERAL DESIGN CONSIDERATIONS

In the design of varactor harmonic multipliers, lumped-circuit techniques are useful to the 450-600 MHz range with little performance degradation, provided coil and capacitor unloaded "Q" values of 200 to 300 are maintained.

Coaxial, stripline, or helical-coil resonators are recommended for higher frequencies. Both cavity and broadband filters can be used. Component values are not critical, but excessive inductance or insufficient coupling can reduce efficiency, and insufficient inductance or excessive coupling can cause poor filtering. Simple experimentation with well-constructed, shielded breadboards is generally sufficient to optimize the circuit. An adequate tuning range must be provided to insure input matching over normal varactor parameter variations. Spurious signals between stages should be kept below 30 dB by suitable filter circuits.

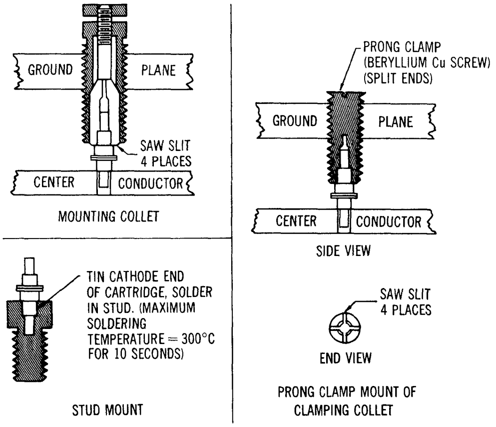
Bias resistors in 500 kohm range give optimum efficiency under self bias. For a linear input-power to output-power relationship, a lower-value bias resistor should be used (approximately 80 kohms). Amplitude-modulated signals can be linearly multiplied with negligible distortion at power-input levels to 30 watts. Figure 4 shows the linearity of the power-output versus power-input relationship without circuit retuning.

For frequency multiplication other than doubling, idler circuits should be used for best efficiencies. One-step, high-order frequency multiplications are possible because of the step-recovery characteristics of these varactors.

VARACTOR MOUNTING

The 1N5149 and 1N5150 varactors are in the cartridge package (designated by the suffix C). This package is well suited for both shunt and series-mounted varactor circuits. Figure 6 shows cross-sectional views of typical mountings. These mountings combine high power-dissipation characteristics with low parasitic impedance.

FIGURE 6 – SUGGESTED MOUNTINGS



MOUNTING COLLET

SIDE VIEW

END VIEW

STUD MOUNT

PRONG CLAMP MOUNT OF CLAMPING COLLET

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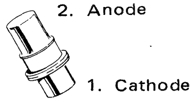
[1] C. B. Burckhardt, "Analysis of Varactor Frequency Multipliers for Arbitrary Capacitance Variation and Drive Level", THE BELL SYSTEM TECHNICAL JOURNAL, April, 1965, pp 675-692.

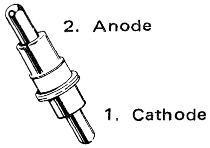
1N5150A (SILICON)
1N5153A
1N5155A

Silicon high-frequency step-recovery power varactor devices optimized for critical multiplier applications requiring tight control of junction capacitance and power dissipation.



CASE 46

1N5155A



CASE 47

1N5150A
1N5153A

MAXIMUM RATINGS

Rating	Symbol	1N5150A	1N5153A	1N5155A	Unit
Reverse Voltage	V_R	80	75	35	Vdc
Forward Current	I_F	1000	250	200	mAdc
RF Power Input	P_{in}	40	15	7.0	Watts
Total Device Dissipation @ T_C = 25°C	P_D	29.2	11.7	8.75	Watts
Derate above 25°C		167	66.7	50	mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	1N5150A	BV_R	80	-	-	Vdc
	1N5153A		75	-	-	
	1N5155A		35	-	-	
Reverse Current (V_R = 70 Vdc)	1N5150A	I_R	-	-	2.0	μAdc
(V_R = 70 Vdc, T_A = 150°C)	1N5150A		-	-	100	
(V_R = 60 Vdc)	1N5153A		-	-	1.0	
(V_R = 60 Vdc, T_A = 150°C)	1N5153A		-	-	100	
(V_R = 26 Vdc)	1N5155A		-	-	1.0	
(V_R = 26 Vdc, T_A = 150°C)	1N5155A		-	-	100	
Series Resistance (V_R = 6.0 Vdc, f = self-resonant frequency)	1N5150A	R_S	-	0.25	-	Ohms
	1N5153A		-	0.5	-	
	1N5155A		-	0.9	-	
Series Inductance	1N5150A	L_S	-	1.5	-	nH
	1N5153A		-	1.7	-	
	1N5155A		-	0.9	-	
Diode Capacitance ($C_J + C_C$) (V_R = 6.0 Vdc, f = 1.0 MHz)	1N5150A	C_T	10.8	-	13.2	pF
	1N5153A		5.8	-	7.0	
	1N5155A		1.71	-	2.09	
Figure of Merit (V_R = 6.0 Vdc, f = 50 MHz)	1N5150A	Q	-	800	-	-
	1N5153A		-	1100	-	
	1N5155A		-	1700	-	
Thermal Resistance	1N5150A	θ_{JC}	-	-	6.0	°C/W
	1N5153A		-	-	15	
	1N5155A		-	-	20	

FUNCTIONAL TEST

1N5150A

RF Power Output	P_{in} = 37 W, f_{in} = 500 MHz,	P_{out}	25.1	-	-	Watts
Doubling Efficiency	f_{out} = 1.0 GHz	η	68	-	-	%

1N5153A

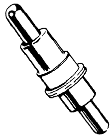
RF Power Output	P_{in} = 12 W, f_{in} = 1.0 GHz,	P_{out}	7.2	-	-	Watts
Doubling Efficiency	f_{out} = 2.0 GHz	η	60	-	-	%

1N5155A

RF Power Output	P_{in} = 5.0 W, f_{in} = 2.0 GHz,	P_{out}	2.0	-	-	Watts
Tripling Efficiency	f_{out} = 6.0 GHz	η	40	-	-	%

For typical curves and test circuits, see the following data sheets: 1N5149-1N5150, 1N5153, and 1N5155.

1N5153 (SILICON)



CASE 47

Silicon high-frequency step-recovery power varactor, designed for high-power, high-frequency harmonic generation applications.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	75	Vdc
Forward Current	I_F	0.25	Adc
RF Power Input	P_{in}	15	Watts
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	5.5 45	Watts mW/°C
Junction Temperature	T_J	+200	°C
Storage Temperature	T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	BV_R	75	80	–	Vdc
Reverse Current	V_R = 60 Vdc V_R = 60 Vdc, T_A = 150°C	I_R	– –	0.5 –	1.0 100	μAdc
Series Resistance	V_R = 6 Vdc, f = 50 MHz	R_S	–	0.5	–	Ohms
Diode Capacitance	V_R = 6 Vdc, f = 1.0MHz V_R = 70 Vdc, f = 1.0MHz	C_T*	5.0 –	5.8 4.0	7.5 –	pF
Figure of Merit	V_R = 6 Vdc, f = 50 MHz	Q	–	1100	–	–
Power Output	DOUBLER TEST CIRCUIT (Figure 1)	P_{out}	6.0	7.2	–	Watts
Efficiency	P_{in} = 12 W, f_{in} = 1GHz f_{out} = 2 GHz	η	50	60	–	%
Thermal Resistance		θ_J	–	19	23	°C/Watt

*$C_T = C_J + C_C$

FIGURE 1 – HARMONIC DOUBLER EFFICIENCY TEST CIRCUIT

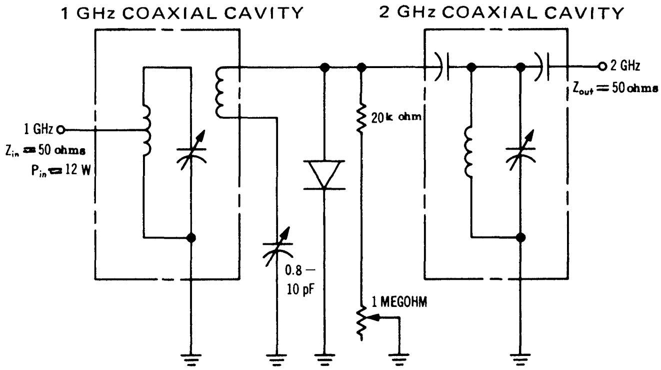
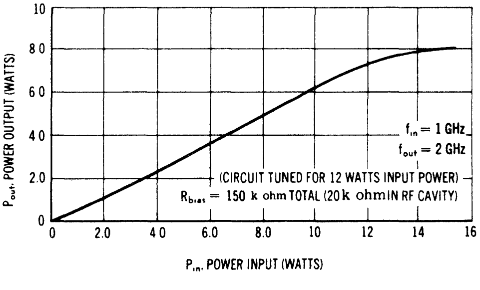


FIGURE 2 – LINEARITY CHARACTERISTIC WITHOUT RETUNING



1N5153 (continued)

POWER OUTPUT versus OUTPUT FREQUENCY

FIGURE 3A — DOUBLING (X2)

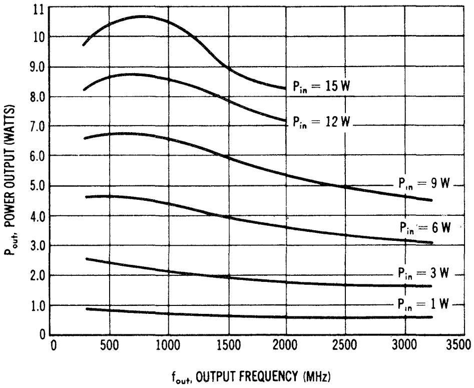


FIGURE 3B — TRIPLING (X3)

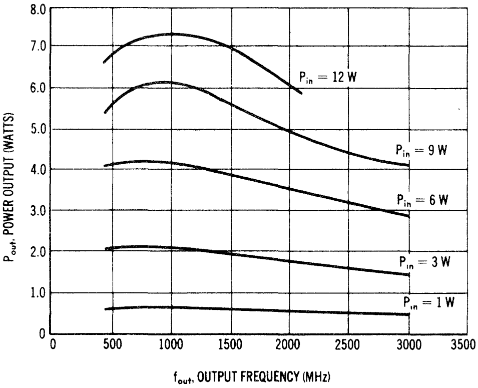
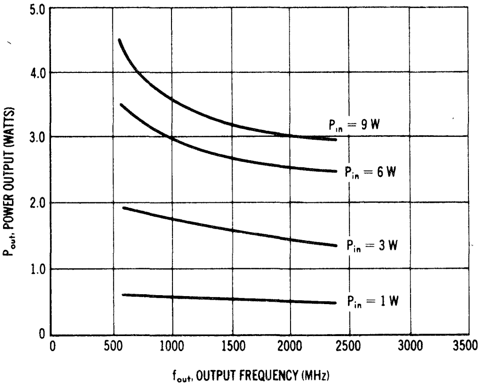


FIGURE 3C — QUADRUPLING (X4)



TYPICAL CHARACTERISTICS at 25°C

FIGURE 4 — FIGURE OF MERIT versus REVERSE VOLTAGE

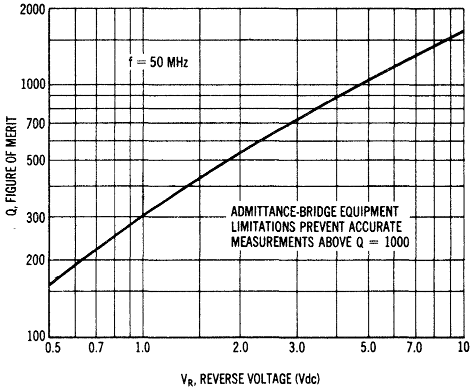


FIGURE 5 — VARACTOR CAPACITANCE versus REVERSE VOLTAGE

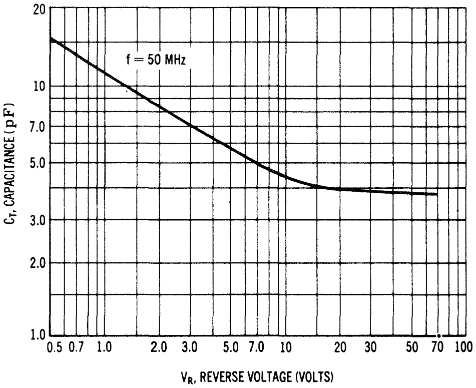
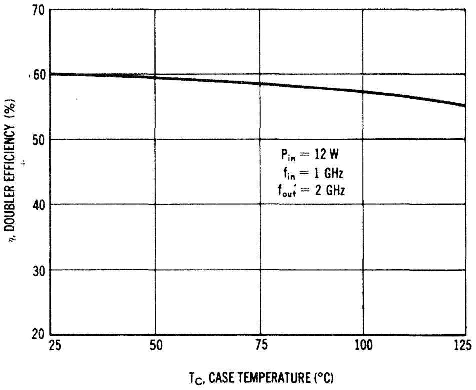


FIGURE 6 — DOUBLER EFFICIENCY versus CASE TEMPERATURE



1N5153A

For Specifications, See 1N5150A Data

1N5155 (SILICON)

CASE 46

Silicon high-frequency step-recovery power varactor, for multiplier applications from 2 to 8.5 GHz with 2 watts minimum power output guaranteed at 6 GHz.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	35	Vdc
Forward Current	I_F	200	mAdc
RF Power Input	P_{in}	7.0	Watts
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	3.5 30	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to + 200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	BV_R	35	45	—	Vdc
Reverse Current	V_R = 26 Vdc V_R = 26 Vdc, T_A = 150°C	I_R	— —	— —	1.0 100	μAdc
Series Resistance	V_R = 6 Vdc, f = 50 MHz	R_S	—	0.9	—	Ohms
Diode Capacitance	V_R = 6 Vdc, f = 1 MHz	C_T	1.0	2.1	3.0	pF
Figure of Merit	V_R = 6 Vdc, f = 50 MHz	Q	—	1700	—	—
Thermal Resistance		θ_{JC}	—	—	35	°C/W

FUNCTIONAL TEST

RF Power Output	Test Circuit Figure 5 P_{in} = 5 watts, f_{in} = 2 GHz, f_{out} = 6 GHz	P_{out}	2.0	—	—	Watts
Tripling Efficiency		η	40	—	—	%

POWER OUTPUT versus OUTPUT FREQUENCY

FIGURE 1A — DOUBLING (X2)

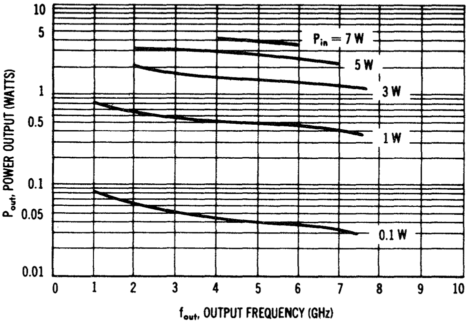


FIGURE 1B — TRIPLING (X3)

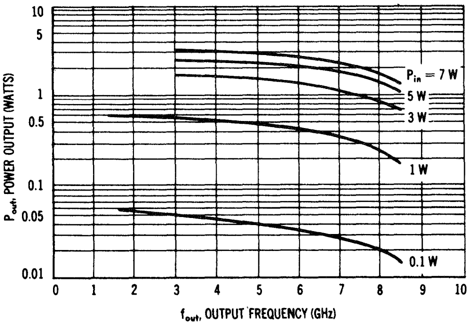
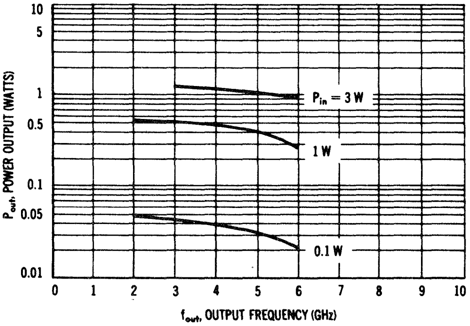


FIGURE 1C — QUADRUPLING (X4)



TYPICAL CHARACTERISTICS
$T_C = 25°C$

FIGURE 2 — VARACTOR CAPACITANCE versus REVERSE VOLTAGE

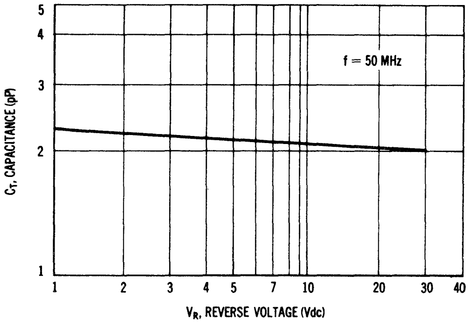


FIGURE 3 — TRIPLER POWER OUTPUT versus TEMPERATURE 2 GHz to 6 GHz

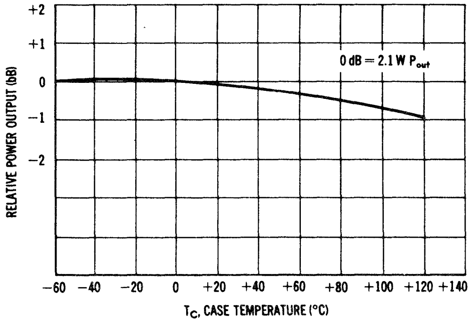


FIGURE 4 — TRIPLER LINEARITY CHARACTERISTIC

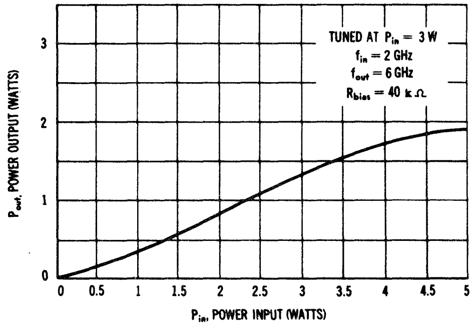


FIGURE 5 — HARMONIC TRIPLER — 2 GHz to 6 GHz

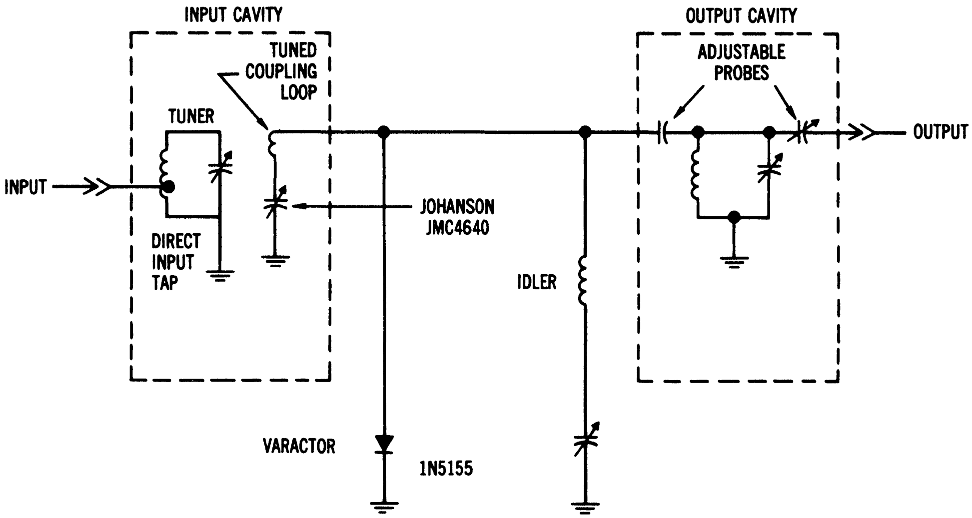
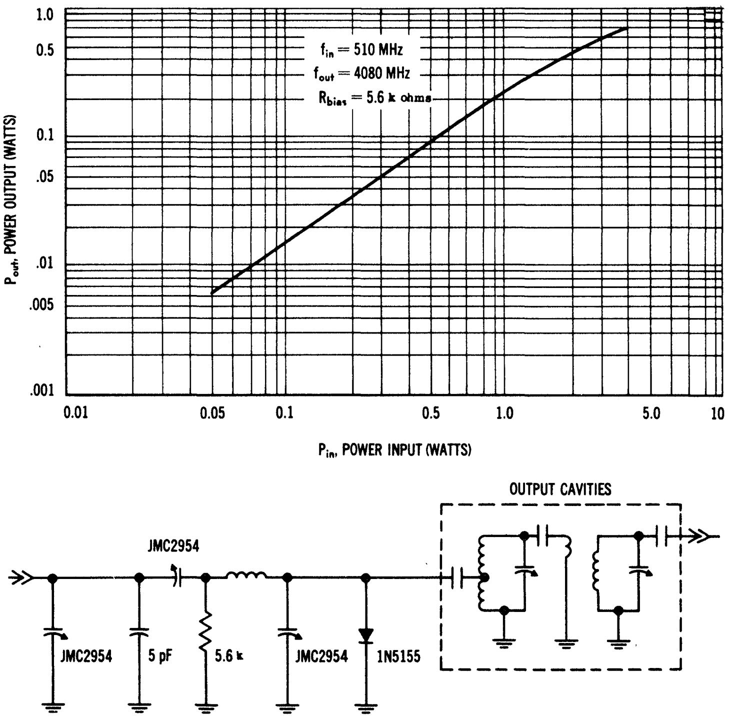


FIGURE 6 — HARMONIC OCTUPLER — 510 MHz to 4080 MHz



1N5155A

For Specifications, See 1N5150A Data

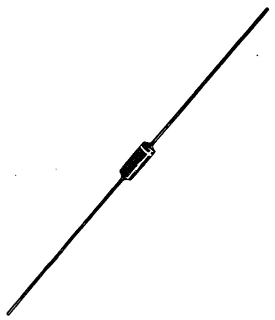
1N5158 thru 1N5160
1N5779 thru 1N5793

PNPN 4-LAYER DIODES

. . . two terminal, fast-switching devices specifically designed for low voltage applications such as logic circuits, pulse generators, memory and relay drivers, relay replacements, alarm circuits, multivibrators, ring counters, and telephone switching circuits. These devices feature:

- Low Breakover (Switching) Voltage – 10 to 15-Volt Ratings
- Fast Switching Speeds – t_{on} = 75 ns (Typ)
  t_{off} = 250 ns (Typ)
- Low Junction Capacitance – 45 pF (Typ)
- Low Breakover Currents
- Subminiature Glass Package

EPITAXIAL
4-LAYER DIODES
10-15 VOLTS
150 mW

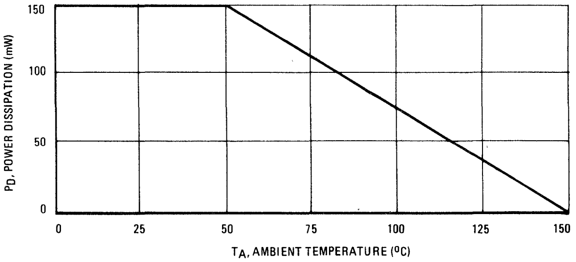


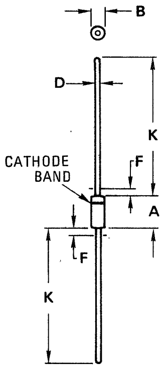
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
*Reverse Voltage 1N5158, 1N5782, 1N5788	V_{RM}	10	Volts
1N5159, 1N5783, 1N5789		11	
1N5160, 1N5784, 1N5790		12	
1N5779, 1N5785, 1N5791		13	
1N5780, 1N5786, 1N5792		14	
1N5781, 1N5787, 1N5793		15	
*Continuous Forward Current	I_F	150	mA
*Steady State Power Dissipation @ T_A = 50°C Derate above 50°C	P_D	150 1.5	mW mW/°C
*Peak Pulse Current (50 μs maximum pulse width)	I_{pulse}	10	Amps
*Operating Junction Temperature Range	T_J	-65 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	–	1.000	–

All JEDEC dimensions and notes apply

CASE 51-02
DO-7

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
*Forward Switching Voltage	1N5158, 1N5782, 1N5788	V_S	8.0	–	10	Volts
	1N5159, 1N5783, 1N5789		9.0	–	11	
	1N5160, 1N5784, 1N5790		10	–	12	
	1N5779, 1N5785, 1N5791		11	–	13	
	1N5780, 1N5786, 1N5792		12	–	14	
	1N5781, 1N5787, 1N5793		13	–	15	
*Forward Switching Current	1N5158 thru 1N5160, 1N5779 thru 1N5781	I_S	–	5.0	50	μA
	1N5782 thru 1N5793		–	10	100	
*Forward Off-State Current (V_F = 0.75 x V_S)		I_{FM}	–	1.0	5.0	μA
*Reverse Current (V_R = V_{RM})		I_{RM}	–	2.0	10	μA
*Holding Current	1N5158 thru 1N5160, 1N5779 thru 1N5781	I_H	1.0	4.0	20	mA
	1N5782 thru 1N5787		10	–	50	
	1N5788 thru 1N5793		0.1	–	2.0	
*Forward On Voltage (I_F = 150 mAdc)		V_F	–	1.0	1.5	Volts
*Critical Rate of Rise of Applied Forward Voltage		dv/dt				V/μs
(V_S = 6.0 Vdc)	1N5158, 1N5782, 1N5788		–	–	0.1	
(V_S = 6.75 Vdc)	1N5159, 1N5783, 1N5789		–	–	0.1	
(V_S = 7.5 Vdc)	1N5160, 1N5784, 1N5790		–	–	0.1	
(V_S = 8.25 Vdc)	1N5779, 1N5785, 1N5791		–	–	0.1	
(V_S = 9.0 Vdc)	1N5780, 1N5786, 1N5792		–	–	0.1	
(V_S = 9.75 Vdc)	1N5781, 1N5787, 1N5793		–	–	0.1	
Junction Capacitance (AC Voltage = 10 mV, V_F = 0, f = 100 kHz)		C_J	–	45	–	pF
Turn-On Time (Figure 2)		t_{on}	–	75(1)	–	ns
Turn-Off Time (Figure 3)		t_{off}	–	250(1)	–	ns

*Indicates JEDEC Registered Data. (1) Time depends on a wide variety of circuit conditions. Consult manufacturer for further information.

FIGURE 2 – TURN-ON TIME TEST CIRCUIT

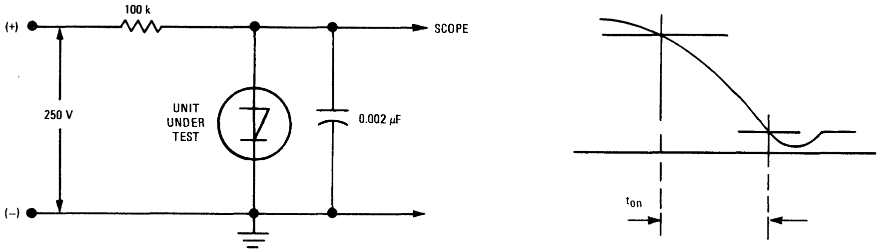
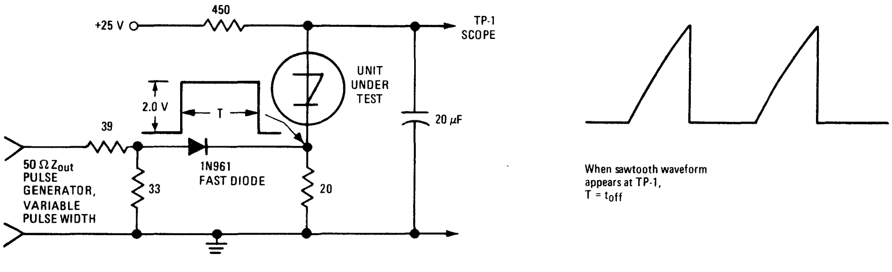


FIGURE 3 – TURN-OFF TIME TEST CIRCUIT



When sawtooth waveform appears at TP-1, T = t_{off}

FIGURE 4 – TYPICAL FORWARD CONDUCTION CHARACTERISTICS

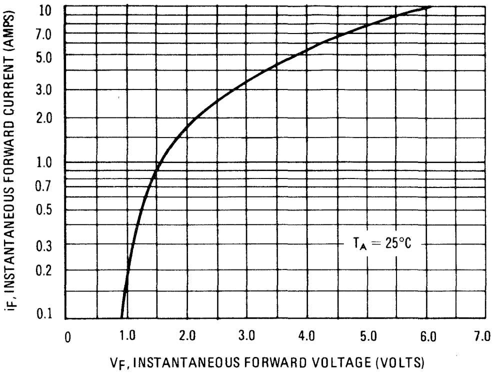
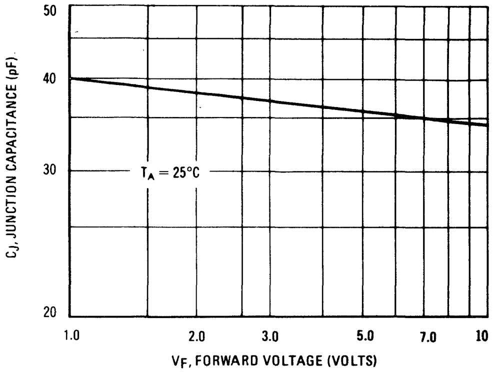


FIGURE 5 – TYPICAL CAPACITANCE



TYPICAL DC CHARACTERISTICS versus TEMPERATURE

(NORMALIZED to 25°C VALUE)

FIGURE 6 – FORWARD BREAKOVER VOLTAGE

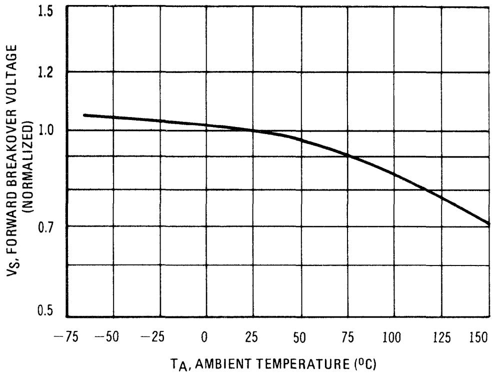


FIGURE 7 – REVERSE BLOCKING VOLTAGE

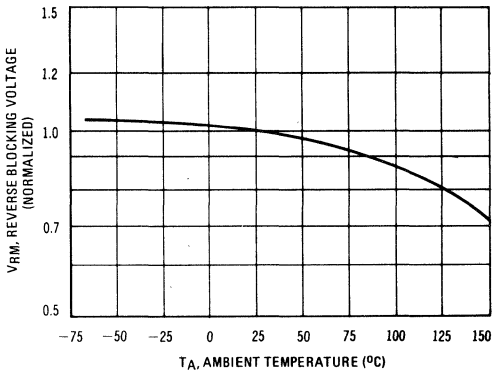


FIGURE 8 – FORWARD BREAKOVER CURRENT

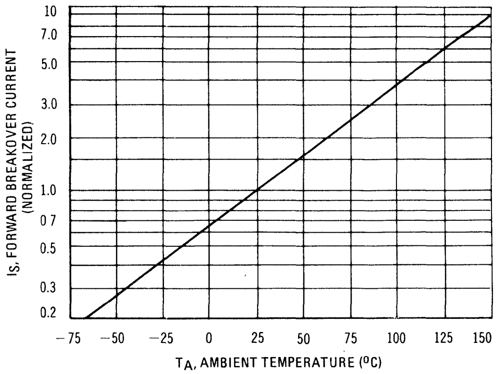
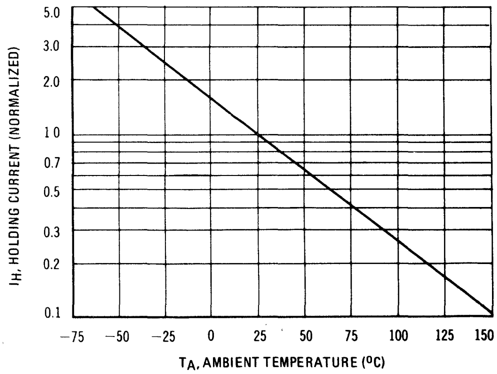
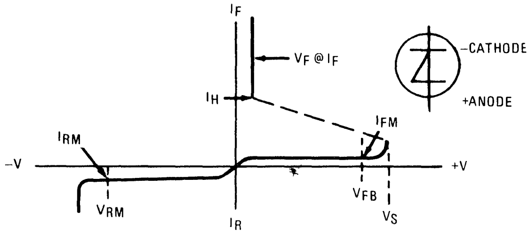


FIGURE 9 – HOLDING CURRENT



4-LAYER DIODE SYMBOLS AND DEFINITIONS



dv/dt	**FORWARD VOLTAGE APPLICATION RATE (V/μs)** – The rate of rise of forward voltage.
I_S	**FORWARD BREAKOVER (SWITCHING) CURRENT** – The value of anode current at the instant the device switches from the blocking to the "on" state, specified at a particular junction temperature.
I_F	**FORWARD CURRENT** – The continuous or DC value of forward current during the "on" state.
I_{FM}	**PEAK FORWARD BLOCKING CURRENT** – The peak anode current when the 4-layer diode is in the "off" state for a stated anode-to-cathode voltage and junction temperature.
I_H	**HOLDING CURRENT** – That value of forward anode current below which the 4-layer diode switches from the conducting state to the forward blocking condition.
I_{pulse}	**PEAK PULSE CURRENT** – The peak repetitive current that can flow through the device for the time duration stated.
I_{RM}	**PEAK REVERSE BLOCKING CURRENT** – The peak current when the 4-layer diode is in the reverse blocking state for a stated anode-to-cathode voltage and junction temperature.
P_D	**STEADY-STATE POWER DISSIPATION**
T_A	**AMBIENT TEMPERATURE**
T_J	**JUNCTION TEMPERATURE**
T_{stg}	**STORAGE TEMPERATURE**
t_{on}	**TURN-ON TIME** – The time interval between the 90% point (90% of forward blocking voltage) and the point 10% above the "on" voltage under stated conditions.
t_{off}	**TURN-OFF TIME** – The time interval required for the device to regain control of its forward blocking characteristic after interruption of forward anode current.
V_S	**FORWARD BREAKOVER (SWITCHING) VOLTAGE** – The positive anode voltage with respect to cathode required to switch the device from the high impedance blocking state to the low impedance "on" state, specified at a particular junction temperature.
V_F	**FORWARD VOLTAGE** – The forward voltage across the device in the "on" state under stated conditions of current and temperature.
V_{FB}	**FORWARD BLOCKING VOLTAGE** – The anode-to-cathode voltage when the 4-layer diode is in the "off" state.
V_{RM}	**PEAK REVERSE VOLTAGE** – The maximum allowable instantaneous value of reverse voltage (repetitive or continuous DC) which can be applied to the device at a stated temperature without damage to the device.

MECHANICAL CHARACTERISTICS

CASE: Hermetically sealed all glass case
DIMENSIONS: JEDEC DO-7 Outline
FINISH: All external surfaces are corrosion resistant with readily solderable leads.
POLARITY: Cathode end indicated by color band.
WEIGHT: 0.2 grams (approx.)
MOUNTING POSITION: Any

1N5221 (SILICON)
thru
1N5281
series

500 MILLIWATT SURMETIC 20 SILICON ZENER DIODES (SILICON OXIDE PASSIVATED)

. . .in answer to the Circuit Design and Component Engineers' many requests — A complete new series of Zener Diodes in the popular DO-204AA case with higher ratings, tighter limits, better operating characteristics and a full set of designers' curves that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial-lead, transfer-molded plastic package offering protection in all common environmental conditions.

- Proven Capability to MIL-S-19500 Specifications
- 10 Watt Surge Rating
- Weldable Leads
- Maximum Limits Guaranteed on Six Electrical Parameters

MAXIMUM RATINGS

Junction and Storage Temperature: —65 to +200°C

Lead Temperature not less than 1/16" from the case for 10 seconds: 230°C

DC Power Dissipation: 500 mW @ T_L = 75°C, Lead Length = 3/8"
(Derate 4.0 mW/°C above 75°C)

Surge Power: 10 Watts (Non-recurrent square wave @ PW = 8.3 ms, T_J = 55°C, Figure 16)

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded, thermosetting plastic.

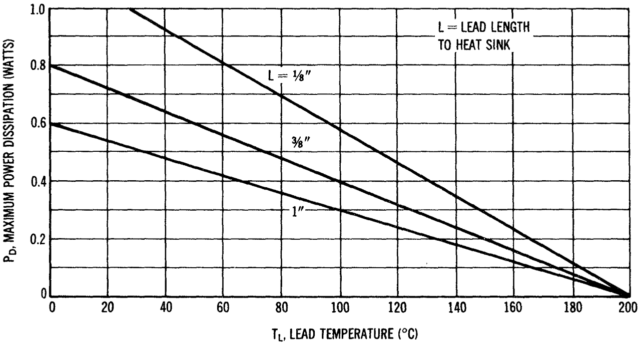
FINISH: All external surfaces are corrosion resistant. Leads are readily solderable and weldable.

POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.

MOUNTING POSITION: Any.

WEIGHT: 0.18 gram (approximately).

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE

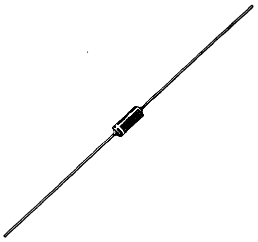


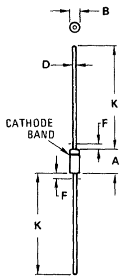
.5M2.4ZS10 thru .5M200ZS10
1N5221A thru 1N5281A

.5M2.4ZS5 thru .5M200ZS5
1N5221B thru 1N5281B

500 MILLIWATT ZENER REGULATOR DIODES

2.4 — 200 VOLTS





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.84	7 62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F		1 27		0.050
K	25 40		1 000	

All JEDEC dimensions and notes apply

CASE 51-02
DO-7

1N5221 thru 1N5281 series (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted). Based on dc measurements at thermal equilibrium; lead length = 3/8"; thermal resistance of heat sink = 30°C/W) V_F = **1.1 Max @ I_F = 200 mA for all types.**

JEDEC Type No. (Note 1)	Nominal Zener Voltage V_Z @ I_{ZT} Volts (Note 2)	Test Current I_{ZT} mA	Max Zener Impedance A & B Suffix Only		Max Reverse Leakage Current				Max Zener Voltage Temp. Coeff. (A & B Suffix Only) θ_{VZ} (%/°C) (Note 3)
					A & B Suffix Only			Non-Suffix	
			Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} @ I_{ZK} = 0.25 mA Ohms	I_R µA	@ V_R Volts A	B	I_R @ V_R Used For Suffix A µA	
1N5221	2.4	20	30	1200	100	0.95	1.0	200	-0.085
1N5222	2.5	20	30	1250	100	0.95	1.0	200	-0.085
1N5223	2.7	20	30	1300	75	0.95	1.0	150	-0.080
1N5224	2.8	20	30	1400	75	0.95	1.0	150	-0.080
1N5225	3.0	20	29	1600	50	0.95	1.0	100	-0.075
1N5226	3.3	20	28	1600	25	0.95	1.0	100	-0.070
1N5227	3.6	20	24	1700	15	0.95	1.0	100	-0.065
1N5228	3.9	20	23	1900	10	0.95	1.0	75	-0.060
1N5229	4.3	20	22	2000	5.0	0.95	1.0	50	±0.055
1N5230	4.7	20	19	1900	5.0	1.9	2.0	50	±0.030
1N5231	5.1	20	17	1600	5.0	1.9	2.0	50	±0.030
1N5232	5.6	20	11	1600	5.0	2.9	3.0	50	+0.038
1N5233	6.0	20	7.0	1600	5.0	3.3	3.5	50	+0.038
1N5234	6.2	20	7.0	1000	5.0	3.8	4.0	50	+0.045
1N5235	6.8	20	5.0	750	3.0	4.8	5.0	30	+0.050
1N5236	7.5	20	6.0	500	3.0	5.7	6.0	30	+0.058
1N5237	8.2	20	8.0	500	3.0	6.2	6.5	30	+0.062
1N5238	8.7	20	8.0	600	3.0	6.2	6.5	30	+0.065
1N5239	9.1	20	10	600	3.0	6.7	7.0	30	+0.068
1N5240	10	20	17	600	3.0	7.6	8.0	30	+0.075
1N5241	11	20	22	600	2.0	8.0	8.4	30	+0.076
1N5242	12	20	30	600	1.0	8.7	9.1	10	+0.077
1N5243	13	9.5	13	600	0.5	9.4	9.9	10	+0.079
1N5244	14	9.0	15	600	0.1	9.5	10	10	+0.082
1N5245	15	8.5	16	600	0.1	10.5	11	10	+0.082
1N5246	16	7.8	17	600	0.1	11.4	12	10	+0.083
1N5247	17	7.4	19	600	0.1	12.4	13	10	+0.084
1N5248	18	7.0	21	600	0.1	13.3	14	10	+0.085
1N5249	19	6.6	23	600	0.1	13.3	14	10	+0.086
1N5250	20	6.2	25	600	0.1	14.3	15	10	+0.086
1N5251	22	5.6	29	600	0.1	16.2	17	10	+0.087
1N5252	24	5.2	33	600	0.1	17.1	18	10	+0.088
1N5253	25	5.0	35	600	0.1	18.1	19	10	+0.089
1N5254	27	4.6	41	600	0.1	20	21	10	+0.090
1N5255	28	4.5	44	600	0.1	20	21	10	+0.091
1N5256	30	4.2	49	600	0.1	22	23	10	+0.091
1N5257	33	3.8	58	700	0.1	24	25	10	+0.092
1N5258	36	3.4	70	700	0.1	26	27	10	+0.093
1N5259	39	3.2	80	800	0.1	29	30	10	+0.094
1N5260	43	3.0	93	900	0.1	31	33	10	+0.095
1N5261	47	2.7	105	1000	0.1	34	36	10	+0.095
1N5262	51	2.5	125	1100	0.1	37	39	10	+0.096
1N5263	56	2.2	150	1300	0.1	41	43	10	+0.096
1N5264	60	2.1	170	1400	0.1	44	46	10	+0.097
1N5265	62	2.0	185	1400	0.1	45	47	10	+0.097
1N5266	68	1.8	230	1600	0.1	49	52	10	+0.097
1N5267	75	1.7	270	1700	0.1	53	56	10	+0.098
1N5268	82	1.5	330	2000	0.1	59	62	10	+0.098
1N5269	87	1.4	370	2200	0.1	65	68	10	+0.099
1N5270	91	1.4	400	2300	0.1	66	69	10	+0.099
1N5271	100	1.3	500	2600	0.1	72	76	10	+0.110
1N5272	110	1.1	750	3000	0.1	80	84	10	+0.110
1N5273	120	1.0	900	4000	0.1	86	91	10	+0.110
1N5274	130	0.95	1100	4500	0.1	94	99	10	+0.110
1N5275	140	0.90	1300	4500	0.1	101	106	10	+0.110
1N5276	150	0.85	1500	5000	0.1	108	114	10	+0.110
1N5277	160	0.80	1700	5500	0.1	116	122	10	+0.110
1N5278	170	0.74	1900	5500	0.1	123	129	10	+0.110
1N5279	180	0.68	2200	6000	0.1	130	137	10	+0.110
1N5280	190	0.66	2400	6500	0.1	137	144	10	+0.110
1N5281	200	0.65	2500	7000	0.1	144	152	10	+0.110

NOTE 1 — TOLERANCE AND VOLTAGE DESIGNATION

Tolerance designation — The JEDEC type numbers shown indicate a tolerance of ±10% with guaranteed limits on only V_Z, I_R and V_F as shown in the above table. Units with guaranteed limits on all six parameters are indicated by suffix "A" for ±10% tolerance and suffix "B" for ±5.0% units.

Non-Standard voltage designation — To designate units with zener voltages other than those assigned JEDEC numbers, the type number should be used.

EXAMPLE:

0.5 M 90 Z S 5

0.5 Watt

Manufacturer

Nominal Voltage

Zener Diodes

Surmetic

Tolerance (±%)

NOTE 2 — SPECIAL SELECTIONS AVAILABLE INCLUDE:

1 — Nominal zener voltages between those shown.

2 — **Matched sets: (Standard Tolerances are ±5.0%, ±3.0%, ±2.0%, ±1.0%) depending on voltage per device.**

a. Two or more units for series connection with specified tolerance on total voltage. Series matched sets make zener voltages in excess of 200 volts possible as well as providing lower temperature coefficients, lower dynamic impedance and greater power handling ability.

b. Two or more units matched to one another with any specified tolerance.

3 — Tight voltage tolerances: 1.0%, 2.0%, 3.0%.

NOTE 3 — TEMPERATURE COEFFICIENT (θ_{VZ})

Test conditions for temperature coefficient are as follows:

a. I_{ZT} = 7.5 mA, T_1 = 25°C,
T_2 = 125°C (1N5221A, B thru 1N5242A, B.)

b. I_{ZT} = Rated I_{ZT}, T_1 = 25°C,
T_2 = 125°C (1N5243A, B thru 1N5281A, B.)

Device to be temperature stabilized with current applied prior to reading breakdown voltage at the specified ambient temperature.

TYPICAL REVERSE CHARACTERISTICS FOR SELECTED ZENER DIODES

Curves marked T_A were obtained from dc measurements at thermal equilibrium; lead length = ⅜"; thermal resistance of heat sink = 30°C/W.
Curves marked T_J were obtained from pulse tests; mounting conditions are not a factor

$V_{Z(Nominal)}$ = 3.3 Volts

FIGURE 2

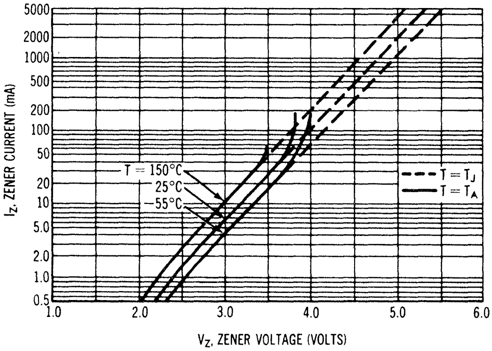
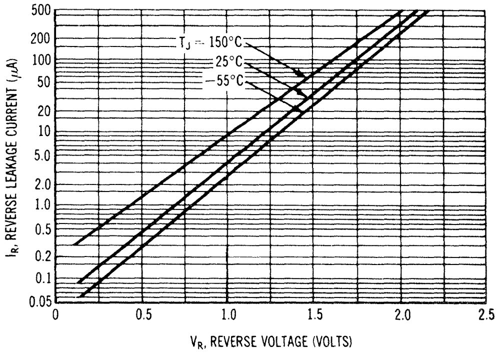


FIGURE 3



$V_{Z(Nominal)}$ = 5.1 Volts

FIGURE 4

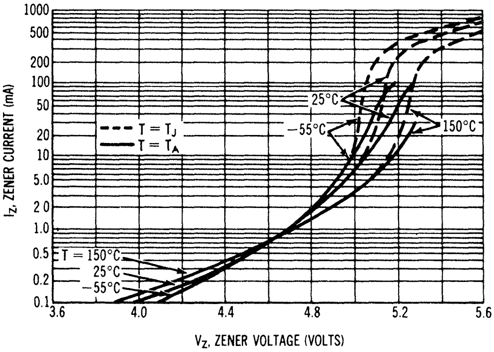
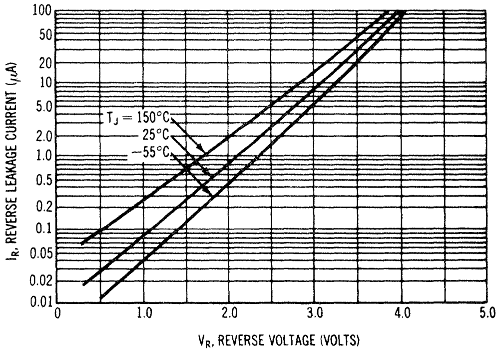


FIGURE 5



$V_{Z(Nominal)}$ = 27 Volts

FIGURE 6

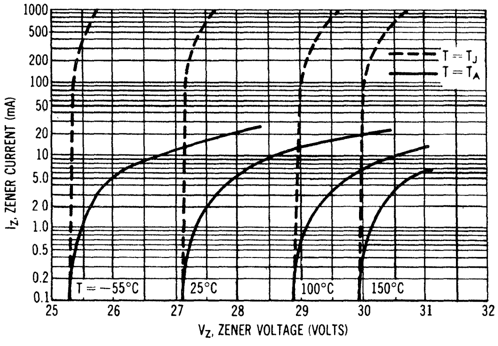
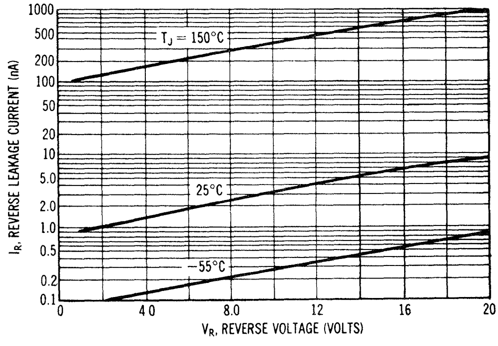


FIGURE 7



TEMPERATURE COEFFICIENTS AND VOLTAGE REGULATION

(90% of the units are in the ranges indicated)

FIGURE 8 — RANGE FOR UNITS TO 12 VOLTS

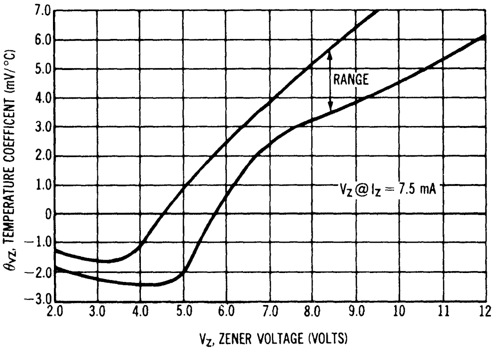


FIGURE 9 — RANGE FOR UNITS 12 TO 200 VOLTS

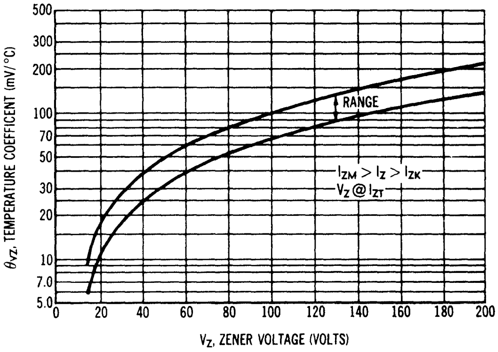


FIGURE 10 — EFFECT OF ZENER CURRENT

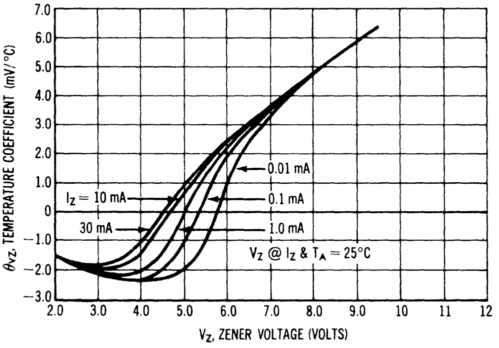
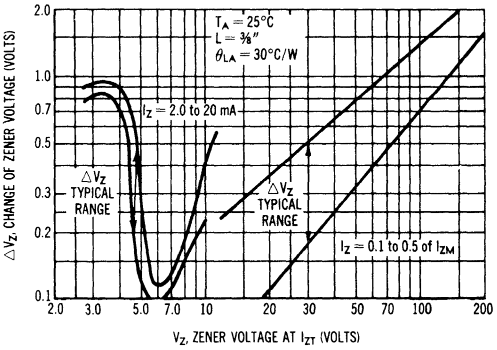


FIGURE 11 — VOLTAGE REGULATION



TYPICAL ZENER IMPEDANCE

FIGURE 12 — EFFECT OF ZENER CURRENT

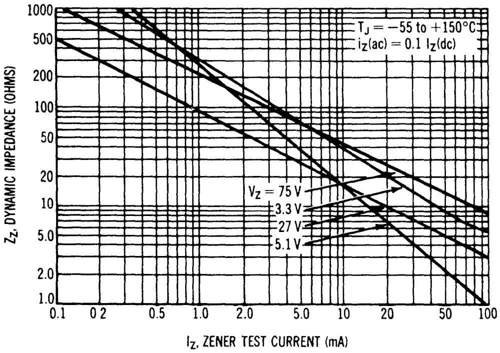


FIGURE 13 — EFFECT OF ZENER VOLTAGE

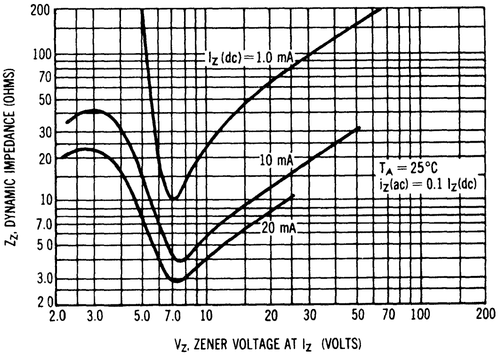


FIGURE 14 — TYPICAL THERMAL RESPONSE

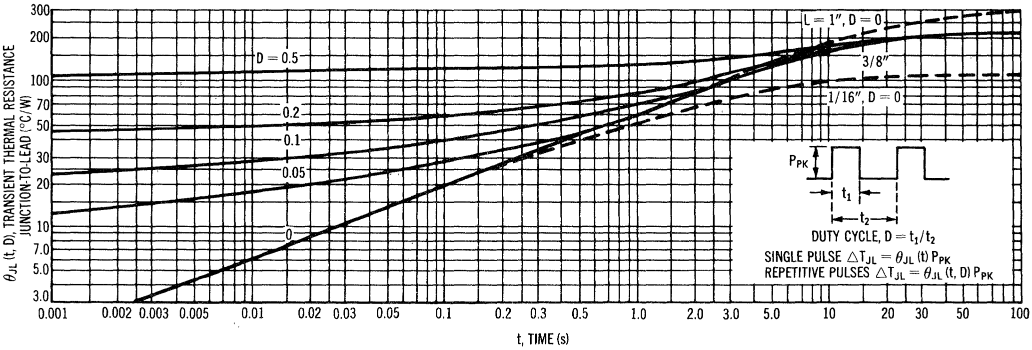


FIGURE 15 — TYPICAL THERMAL RESISTANCE

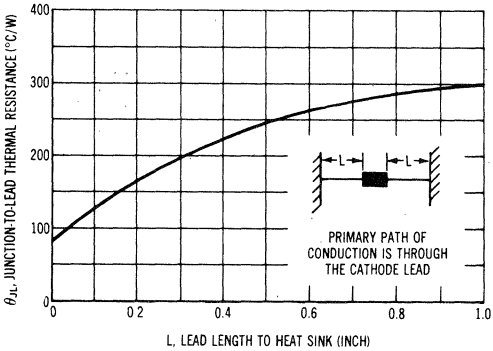
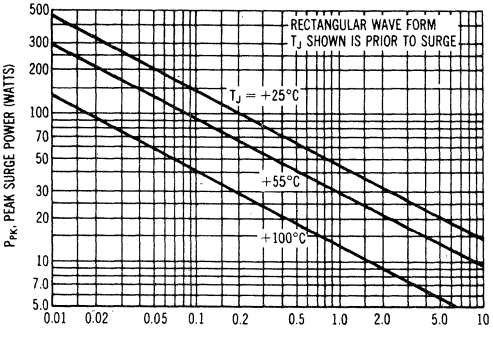


FIGURE 16 — MAXIMUM NON-REPETITIVE SURGE POWER — Note 4



APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions, in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L, should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

θ_{LA} is the lead-to-ambient thermal resistance and P_D is the power dissipation. θ_{LA} is generally 30-40°C/W for the various clips and tie points in common use and for printed circuit board wiring.

Junction Temperature, T_J, may be found from:

$$T_J = T_L + \Delta T_{JL}$$

ΔT_{JL} is the increase in junction temperature above the lead temperature and may be found from Figure 14 for a train of power pulses or from Figure 15 for dc power.

For worst-case design, using expected limits of I_Z, limits of P_D and the extremes of T_J (ΔT_J) may be estimated. Changes in voltage, V_Z, can then be found from:

$$\Delta V = \theta_{VZ} \Delta T_J$$

θ_{VZ}, the zener voltage temperature coefficient, is found from Figures 8, 9, and 10.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, use short leads, especially to the cathode, and keep current excursions as low as possible.

Data of Figure 14 should not be used to compute surge capability. Surge limitations are given in Figure 16. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 16 be exceeded.

Note 4.

This curve is directly readable when applied to devices with nominal voltages in the 11 to 200 Volt range. For devices with nominal voltages in the 2.4 to 10 Volt range, multiply the appropriate peak surge power reading by 0.4.

FIGURE 17 — TYPICAL CAPACITANCE

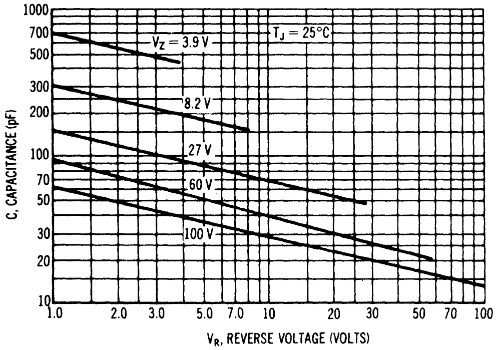


FIGURE 18 — TYPICAL FORWARD CHARACTERISTICS

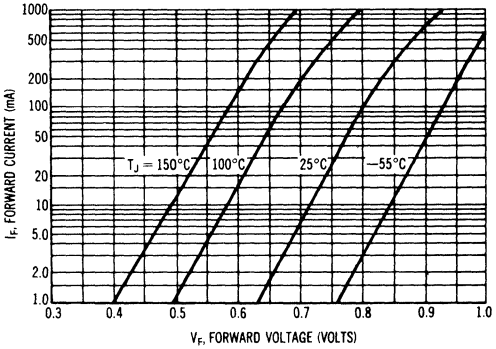


FIGURE 19 — TYPICAL NOISE DENSITY

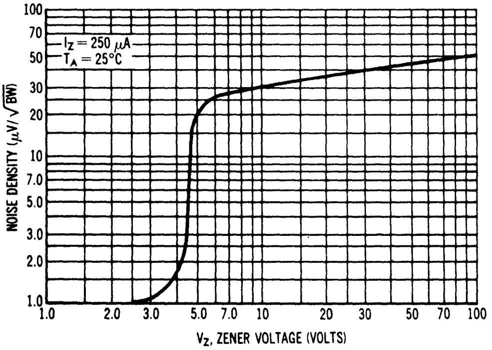
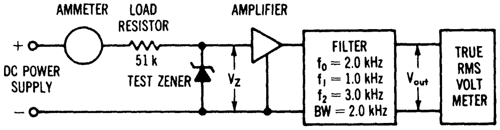


FIGURE 20 — NOISE DENSITY MEASUREMENT METHOD

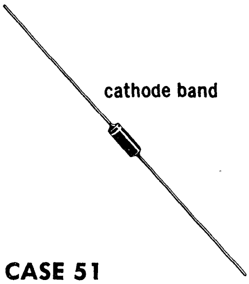


NOISE DENSITY (VOLTS PER SQUARE ROOT BANDWIDTH) = $\dfrac{V_{out}}{\text{OVERALL GAIN } \sqrt{BW}}$

WHERE: BW = FILTER BANDWIDTH (Hz)
V_{out} = OUTPUT NOISE (VOLTS RMS)

The input voltage and load resistance are high so that the zener diode is driven from a constant current source. The amplifier is low noise so that the amplifier noise is negligible compared to that of the test zener. The filter bandpass is known so that the noise density can be calculated from the formula shown. The data of Figure 19 and the formula can also be used to find noise for any system bandwidth.

1N5283 thru 1N5314



CASE 51
(DO-7)

Field-effect current regulator diodes are circuit elements that provide a current essentially independent of voltage. These diodes are especially designed for maximum impedance over the operating range. These devices may be used in parallel to obtain higher currents.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Operating Voltage (T_J = -55°C to +200°C)	POV	100	Volts
Steady State Power Dissipation @ T_L = 75°C Derate above T_L = 75°C Lead Length = 3/8" (Forward or Reverse Bias)	P_D	600 4.8	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200	°C

1N5283 thru 1N5314 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

	Regulator Current I_P (mA) @ V_T = 25 V			Minimum Dynamic Impedance @V_T = 25 V Z_T (MΩ)	Minimum Knee Impedance @V_K = 6.0 V Z_K (MΩ)	Maximum Limiting Voltage @I_L = 0.8 I_P (min) V_L (Volts)
Type No.	nom	min	max			
1N5283	0.22	0.198	0.242	25.0	2.75	1.00
1N5284	0.24	0.216	0.264	19.0	2.35	1.00
1N5285	0.27	0.243	0.297	14.0	1.95	1.00
1N5286	0.30	0.270	0.330	9.0	1.60	1.00
1N5287	0.33	0.297	0.363	6.6	1.35	1.00
1N5288	0.39	0.351	0.429	4.10	1.00	1.05
1N5289	0.43	0.387	0.473	3.30	0.870	1.05
1N5290	0.47	0.423	0.517	2.70	0.750	1.05
1N5291	0.56	0.504	0.616	1.90	0.560	1.10
1N5292	0.62	0.558	0.682	1.55	0.470	1.13
1N5293	0.68	0.612	0.748	1.35	0.400	1.15
1N5294	0.75	0.675	0.825	1.15	0.335	1.20
1N5295	0.82	0.738	0.902	1.00	0.290	1.25
1N5296	0.91	0.819	1.001	0.880	0.240	1.29
1N5297	1.00	0.900	1.100	0.800	0.205	1.35
1N5298	1.10	0.990	1.210	0.700	0.180	1.40
1N5299	1.20	1.08	1.32	0.640	0.155	1.45
1N5300	1.30	1.17	1.43	0.580	0.135	1.50
1N5301	1.40	1.26	1.54	0.540	0.115	1.55
1N5302	1.50	1.35	1.65	0.510	0.105	1.60
1N5303	1.60	1.44	1.76	0.475	0.092	1.65
1N5304	1.80	1.62	1.98	0.420	0.074	1.75
1N5305	2.00	1.80	2.20	0.395	0.061	1.85
1N5306	2.20	1.98	2.42	0.370	0.052	1.95
1N5307	2.40	2.16	2.64	0.345	0.044	2.00
1N5308	2.70	2.43	2.97	0.320	0.035	2.15
1N5309	3.00	2.70	3.30	0.300	0.029	2.25
1N5310	3.30	2.97	3.63	0.280	0.024	2.35
1N5311	3.60	3.24	3.96	0.265	0.020	2.50
1N5312	3.90	3.51	4.29	0.255	0.017	2.60
1N5313	4.30	3.87	4.73	0.245	0.014	2.75
1N5314	4.70	4.23	5.17	0.235	0.012	2.90

FIGURE 1 — TYPICAL CURRENT REGULATOR CHARACTERISTICS

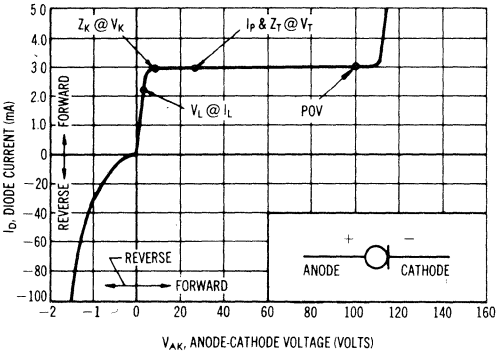
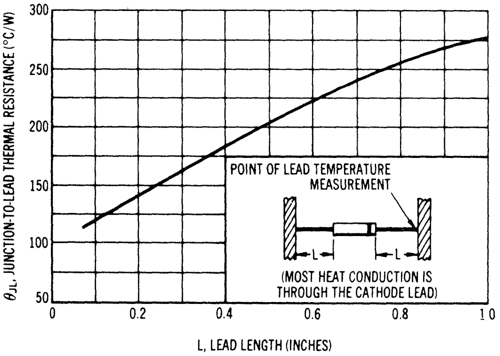


FIGURE 2 — TYPICAL THERMAL RESISTANCE



SYMBOLS AND DEFINITIONS

I_D — Diode Current.

I_L — Limiting Current: 80% of I_P minimum used to determine Limiting voltage, V_L.

I_P — Pinch-off Current: Regulator current at specified Test Voltage, V_T.

POV — Peak Operating Voltage· Maximum voltage to be applied to device.

θ_I — Current Temperature Coefficient

V_{AK} — Anode-to-cathode Voltage

V_K — Knee Impedance Test Voltage: Specified voltage used to establish Knee Impedance, Z_K.

V_L — Limiting Voltage: Measured at I_L. V_L, together with Knee AC Impedance, Z_K, indicates the Knee characteristics of the device.

V_T — Test Voltage: Voltage at which I_P and Z_T are specified.

Z_K — Knee AC Impedance at Test Voltage To test for Z_K, a 90 Hz signal v_K with RMS value equal to 10% of test voltage, V_K, is superimposed on V_K:

$$Z_K = v_K / i_K$$

where i_K is the resultant ac current due to v_K

To provide the most constant current from the diode, Z_K should be as high as possible, therefore, a minimum value of Z_K is specified.

Z_T — AC Impedance at Test Voltage: Specified as a minimum value. To test for Z_T, a 90 Hz signal with RMS value equal to 10% of Test Voltage, V_T, is superimposed on V_T.

APPLICATION NOTE

As the current available from the diode is temperature dependent, it is necessary to determine junction temperature, T_J, under specific operating conditions to calculate the value of the diode current. The following procedure is recommended:

Lead Temperature, T_L, shall be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

where θ_{LA} is lead-to-ambient thermal resistance
and P_D is power dissipation.

θ_{LA} is generally 30-40°C/W for the various clips and tie points in common use, and for printed circuit-board wiring.

Junction Temperature, T_J, shall be calculated from:

$$T_J = T_L + \theta_{JL} P_D$$

where θ_{JL} is taken from Figure 2.

For circuit design limits of V_{AK}, limits of P_D may be estimated and extremes of T_J may be computed. Using the information on Figures 4 and 5, changes in current may be found. To improve current regulation, keep V_{AK} low to reduce P_D and keep the leads short, especially the cathode lead, to reduce θ_{JL}.

FIGURE 3 — TYPICAL FORWARD CHARACTERISTICS

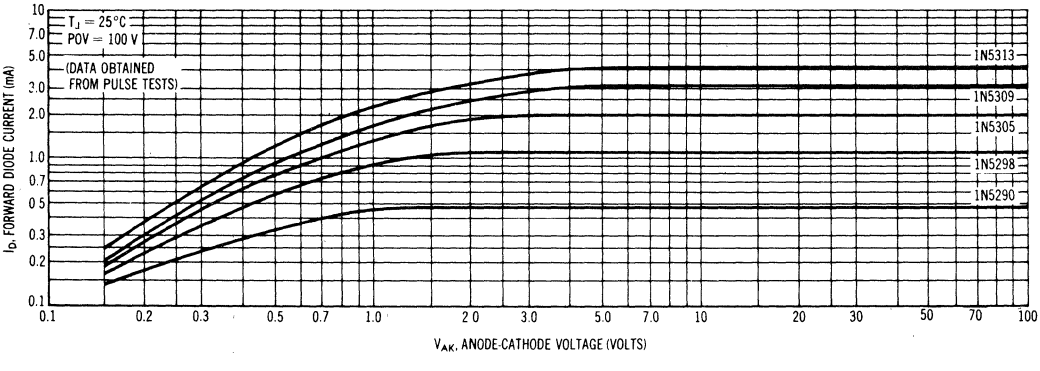


FIGURE 4 — TEMPERATURE COEFFICIENT

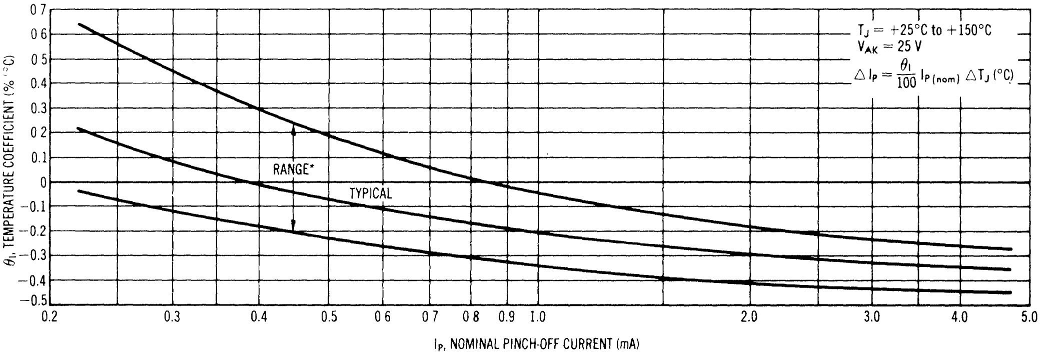


FIGURE 5 — TEMPERATURE COEFFICIENT

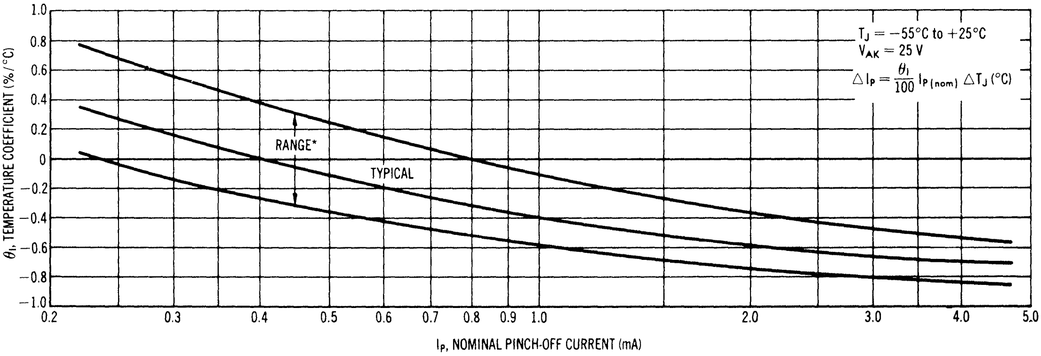
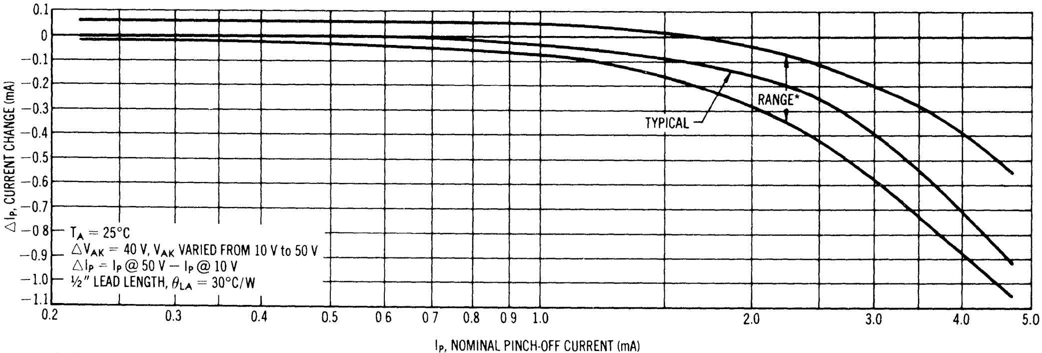


FIGURE 6 — CURRENT REGULATION FACTOR



*90% of the units will be in the ranges shown.

1N5333 (SILICON)
thru
1N5388

5.0 WATT SURMETIC 40 SILICON ZENER DIODES (SILICON OXIDE PASSIVATED)

. . . a complete new series of 5.0 Watt Zener Diodes with tight limits and better operating characteristics that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial-lead, transfer-molded plastic package offering protection in all common environmental conditions.

- Up to 180 Watt Surge Rating @ 8.3 ms
- Maximum Limits Guaranteed on Seven Electrical Parameters

(5M3.3ZS10 thru 5M200ZS10 1N5333A thru 1N5388A)
(5M3.3ZS5 thru 5M200ZS5 1N5333B thru 1N5388B)

5.0 WATT ZENER REGULATOR DIODES

3.3 – 200 VOLTS

MAXIMUM RATINGS

Junction and Storage Temperature: -65 to +200°C

Lead Temperature not less than 1/16" from the case for 10 seconds: 230°C

DC Power Dissipation: 5.0 W @ T_L = 75°C, Lead Length = 3/8"
(Derate 40 mW/°C above 75°C)

MECHANICAL CHARACTERISTICS

CASE: Void-free, transfer-molded, thermosetting plastic

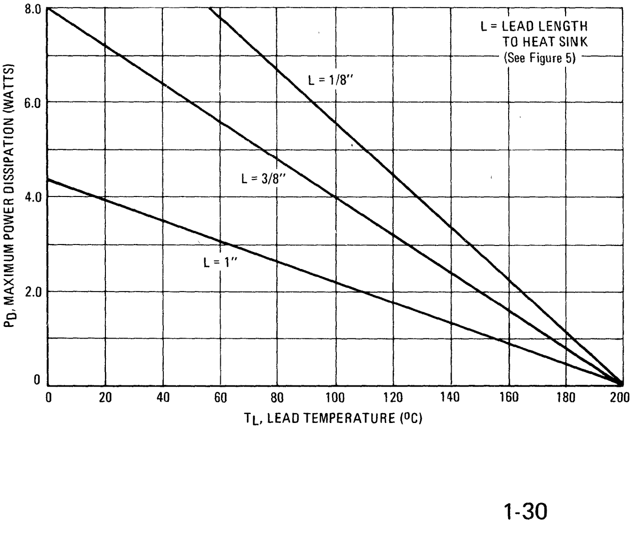
FINISH: All external surfaces are corrosion resistant. Leads are readily solderable

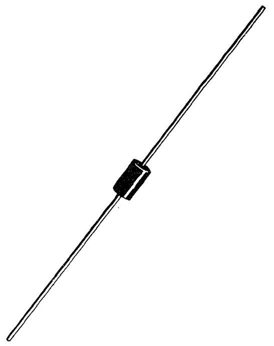
POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.

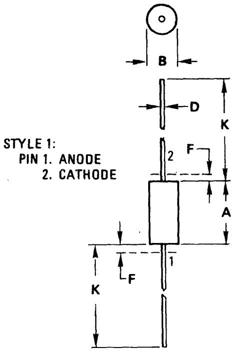
MOUNTING POSITION: Any

WEIGHT: 0.7 gram (approx)

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE







DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	3.30	3.68	0.130	0.145
D	0.94	1.09	0.037	0.043
F	–	1.27	–	0.050
K	25.40	31.75	1.000	1.250

CASE 17

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 1.2 Max @ I_F = 1.0 A for all types

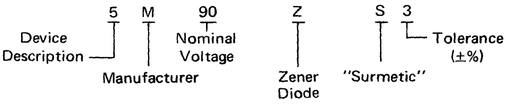
JEDEC Type No. (Note 1 & 2)	Nominal Zener Voltage V_Z @ I_{ZT} Volts (Note 3)	Test Current I_{ZT} mA	Max Zener Impedance A & B Suffix Only		Max Reverse Leakage Current			Applies to all Suffix	A & B Suffix Only	Maximum Regulator Current I_{ZM} mA (Note 6)
			Z_{ZT} @ I_{ZT} Ohms (Note 3)	Z_{ZK} @ I_{ZK} = 1.0 mA Ohms (Note 3)	I_R µA	@ V_R Volts Non & A Suffix	B-Suffix	Max Surge Current i_r, Amps (Note 4)	Max Voltage Regulation △ V_Z, Volts (Note 5)	
1N5333	3.3	380	3.0	400	300	1.0	1.0	20.0	0.85	1440
1N5334	3.6	350	2.5	500	150	1.0	1.0	18.7	0.80	1320
1N5335	3.9	320	2.0	500	50	1.0	1.0	17.6	0.54	1220
1N5336	4.3	290	2.0	500	10	1.0	1.0	16.4	0.49	1100
1N5337	4.7	260	2.0	450	5.0	1.0	1.0	15.3	0.44	1010
1N5338	5.1	240	1.5	400	1.0	1.0	1.0	14.4	0.39	930
1N5339	5.6	220	1.0	400	1.0	2.0	2.0	13.4	0.25	865
1N5340	6.0	200	1.0	300	1.0	3.0	3.0	12.7	0.19	790
1N5341	6.2	200	1.0	200	1.0	3.0	3.0	12.4	0.10	765
1N5342	6.8	175	1.0	200	10	4.9	5.2	11.5	0.15	700
1N5343	7.5	175	1.5	200	10	5.4	5.7	10.7	0.15	630
1N5344	8.2	150	1.5	200	10	5.9	6.2	10.0	0.20	580
1N5345	8.7	150	2.0	200	10	6.3	6.6	9.5	0.20	545
1N5346	9.1	150	2.0	150	7.5	6.6	6.9	9.2	0.22	520
1N5347	10	125	2.0	125	5.0	7.2	7.6	8.6	0.22	475
1N5348	11	125	2.5	125	5.0	8.0	8.4	8.0	0.25	430
1N5349	12	100	2.5	125	2.0	8.6	9.1	7.5	0.25	395
1N5350	13	100	2.5	100	1.0	9.4	9.9	7.0	0.25	365
1N5351	14	100	2.5	75	1.0	10.1	10.6	6.7	0.25	340
1N5352	15	75	2.5	75	1.0	10.8	11.5	6.3	0.25	315
1N5353	16	75	2.5	75	1.0	11.5	12.2	6.0	0.30	295
1N5354	17	70	2.5	75	0.5	12.2	12.9	5.8	0.35	280
1N5355	18	65	2.5	75	0.5	13.0	13.7	5.5	0.40	264
1N5356	19	65	3.0	75	0.5	13.7	14.4	5.3	0.40	250
1N5357	20	65	3.0	75	0.5	14.4	15.2	5.1	0.40	237
1N5358	22	50	3.5	75	0.5	15.8	16.7	4.7	0.45	216
1N5359	24	50	3.5	100	0.5	17.3	18.2	4.4	0.55	198
1N5360	25	50	4.0	110	0.5	18.0	19.0	4.3	0.55	190
1N5361	27	50	5.0	120	0.5	19.4	20.6	4.1	0.60	176
1N5362	28	50	6.0	130	0.5	20.1	21.2	3.9	0.60	170
1N5363	30	40	8.0	140	0.5	21.6	22.8	3.7	0.60	158
1N5364	33	40	10	150	0.5	23.8	25.1	3.5	0.60	144
1N5365	36	30	11	160	0.5	25.9	27.4	3.3	0.65	132
1N5366	39	30	14	170	0.5	28.1	29.7	3.1	0.65	122
1N5367	43	30	20	190	0.5	31.0	32.7	2.8	0.70	110
1N5368	47	25	25	210	0.5	33.8	35.8	2.7	0.80	100
1N5369	51	25	27	230	0.5	36.7	38.8	2.5	0.90	93.0
1N5370	56	20	35	280	0.5	40.3	42.6	2.3	1.00	86.0
1N5371	60	20	40	350	0.5	43.0	45.5	2.2	1.20	79.0
1N5372	62	20	42	400	0.5	44.6	47.1	2.1	1.35	76.0
1N5373	68	20	44	500	0.5	49.0	51.7	2.0	1.50	70.0
1N5374	75	20	45	620	0.5	54.0	56.0	1.9	1.60	63.0
1N5375	82	15	65	720	0.5	59.0	62.2	1.8	1.80	58.0
1N5376	87	15	75	760	0.5	63.0	66.0	1.7	2.00	54.5
1N5377	91	15	75	760	0.5	65.5	69.2	1.6	2.20	52.5
1N5378	100	12	90	800	0.5	72.0	76.0	1.5	2.50	47.5
1N5379	110	12	125	1000	0.5	79.2	83.6	1.4	2.50	43.0
1N5380	120	10	170	1150	0.5	86.4	91.2	1.3	2.50	39.5
1N5381	130	10	190	1250	0.5	93.6	98.8	1.2	2.50	36.6
1N5382	140	8.0	230	1500	0.5	101	106	1.2	2.50	34.0
1N5383	150	8.0	330	1500	0.5	108	114	1.1	3.00	31.6
1N5384	160	8.0	350	1650	0.5	115	122	1.1	3.00	29.4
1N5385	170	8.0	380	1750	0.5	122	129	1.0	3.00	28.0
1N5386	180	5.0	430	1750	0.5	130	137	1.0	4.00	26.4
1N5387	190	5.0	450	1850	0.5	137	144	0.9	5.00	25.0
1N5388	200	5.0	480	1850	0.5	144	152	0.9	5.00	23.6

NOTE 1 – TOLERANCE AND VOLTAGE DESIGNATION

TOLERANCE DESIGNATION – The JEDEC type numbers shown indicate a tolerance of ±20% with guaranteed limits on only V_Z, I_R, i_r, and V_F as shown in the electrical characteristics table. Units with guaranteed limits on all seven parameters are indicated by suffix "A" for ±10% tolerance and suffix "B" for ±5.0% units.

NOTE 2 – SPECIALS AVAILABLE INCLUDE:

(A) NOMINAL ZENER VOLTAGES BETWEEN THE VOLTAGES SHOWN AND TIGHTER VOLTAGE TOLERANCES: To designate units with zener voltages other than those assigned JEDEC numbers and/or tight voltage tolerances (±3%, ±2%, ±1%), the Mfg. type number should be used.



Example: 5M90ZS3

(B) MATCHED SETS: (Standard Tolerances are ±5.0%, ±2.0%, ±1.0%).

Zener diodes can be obtained in sets consisting of two or more matched devices. The method for specifying such matched sets is similar to the one described in (A) for specifying units with a special voltage and/or tolerance except that two extra suffixes are added to the code number described.

These units are marked with code letters to identify the matched sets and, in addition, each unit in a set is marked with the same serial number, which is different for each set being ordered.

5	Device Description
M	Manufacturer
5 1	51 Volts (each device)
Z	Zener Diodes
S	"Surmetic"
5	Tolerance per device (±5%) (omit for ±20% units)
B	Code* (A-Not used)
1	Overall Tolerance of set (±1%)

*Code:
B – Two devices in series
C – Three devices in series
D – Four devices in series

Example: **5M51ZS5B1**

(C) ZENER CLIPPERS: (Standard Tolerance ±10% and ±5%).

Special clipper diodes with opposing Zener junctions built into the device are available by using the following nomenclature:

5	Device Description
M	Manufacturer
20,	Nominal Voltage
Z	Zener Diodes
Z	Clipper
10	Tolerance for each of the two Zener voltages (not a matching requirement)

Example: **5M20ZZ10**

NOTE 3 – ZENER VOLTAGE (V_Z) AND IMPEDANCE (Z_{ZT} & Z_{ZK})

Test conditions for Zener voltage and impedance are as follows: I_Z is applied 40 ± 10 ms prior to reading. Mounting contacts are located 3/8" to 1/2" from the inside edge of mounting clips to the body of the diode. ($T_A = 25°C \,^{+8}_{-2}°C$).

NOTE 4 – SURGE CURRENT (i_r)

Surge current is specified as the maximum allowable peak, non-recurrent square-wave current with a pulse width, PW, of 8.3 ms. The data given in Figure 6 may be used to find the maximum surge current for a square wave of any pulse width between 1.0 ms and 1000 ms by plotting the applicable points on logarithmic paper. Examples of this, using the 3.3 V and 200 V zeners, are shown in Figure 7. Mounting contact located as specified in Note 3. ($T_A = 25°C \,^{+8}_{-2}°C$).

NOTE 5 – VOLTAGE REGULATION (ΔV_Z)

Test conditions for voltage regulation are as follows: V_Z measurements are made at 10% and then at 50% of the I_Z max value listed in the electrical characteristics table. The test currents are the same for the 5% and 10% tolerance devices. The test current time duration for each V_Z measurement is 40 ± 10 ms. ($T_A = 25°C \,^{+8}_{-2}C$). Mounting contact located as specified in Note 3.

NOTE 6 – MAXIMUM REGULATOR CURRENT (I_{ZM})

The maximum current shown is based on the maximum voltage of a 5% type unit, therefore, it applies only to the B-suffix device. The actual I_{ZM} for any device may not exceed the value of 5.0 watts divided by the actual V_Z of the device. $T_L = 75°C$ at 3/8" maximum from the device body.

TEMPERATURE COEFFICIENTS

FIGURE 2 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS 3.0 TO 10 VOLTS

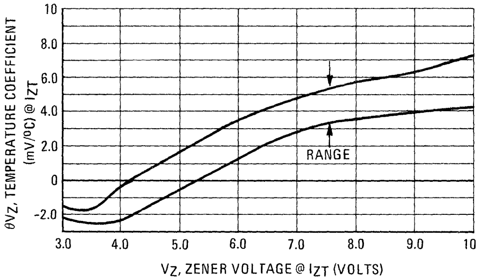


FIGURE 3 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS 10 TO 220 VOLTS

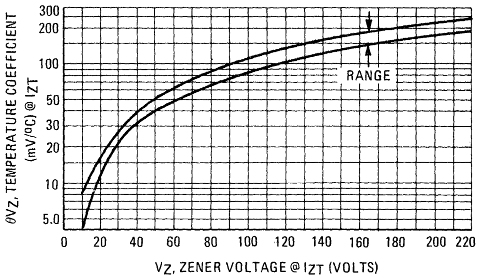
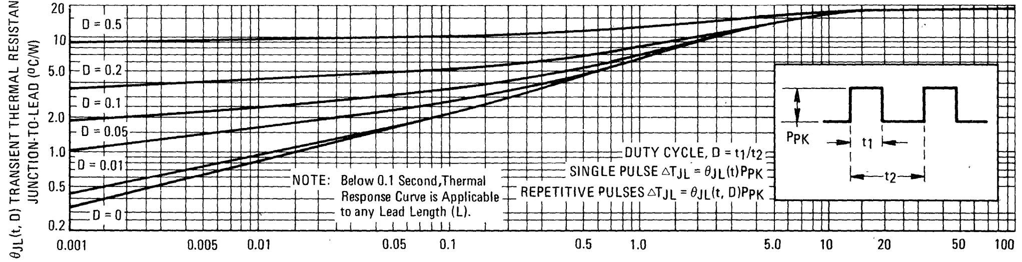


FIGURE 4 – TYPICAL THERMAL RESPONSE

L, LEAD LENGTH = 3/8 INCH



NOTE: Below 0.1 Second, Thermal Response Curve is Applicable to any Lead Length (L).

FIGURE 5 — TYPICAL THERMAL RESISTANCE

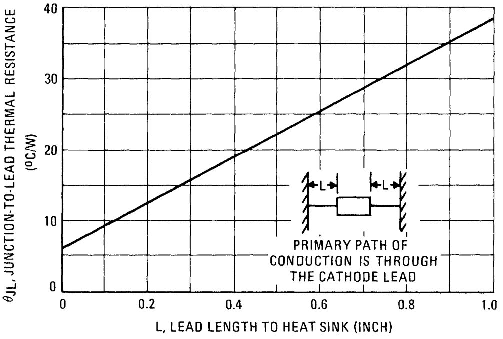


FIGURE 6 — MAXIMUM NON-REPETITIVE SURGE CURRENT versus NOMINAL ZENER VOLTAGE

(See Note 4)

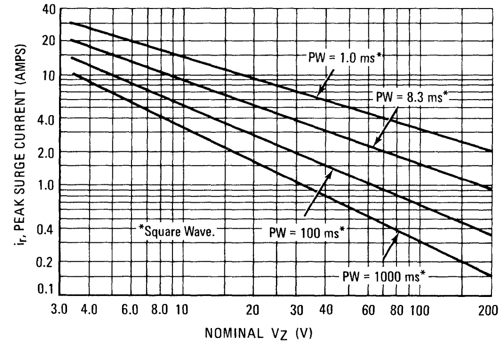
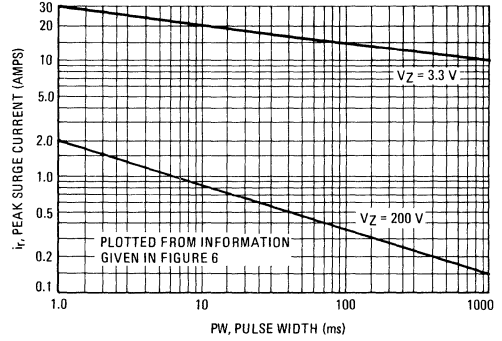


FIGURE 7 — PEAK SURGE CURRENT versus PULSE WIDTH

(See Note 4)



APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions, in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L, should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

θ_{LA} is the lead-to-ambient thermal resistance and P_D is the power dissipation.

Junction Temperature, T_J, may be found from:

$$T_J = T_L + \Delta T_{JL}$$

ΔT_{JL} is the increase in junction temperature above the lead temperature and may be found from Figure 4 for a train of power pulses or from Figure 5 for dc power.

$$\Delta T_{JL} = \theta_{JL} P_D$$

For worst-case design, using expected limits of I_Z, limits of P_D and the extremes of $T_J(\Delta T_J)$ may be estimated. Changes in voltage, V_Z, can then be found from:

$$\Delta V = \theta_{VZ} \Delta T_J$$

θ_{VZ}, the zener voltage temperature coefficient, is found from Figures 2 and 3.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, keep current excursions as low as possible.

Data of Figure 4 should not be used to compute surge capability. Surge limitations are given in Figure 6. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 6 be exceeded.

1N5441A,B,C (SILICON)
thru
1N5456A,B,C

VVC

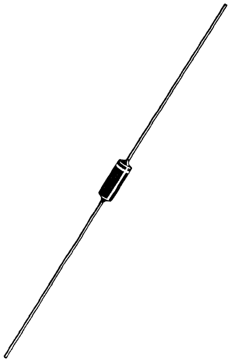
VOLTAGE-VARIABLE CAPACITANCE DIODES

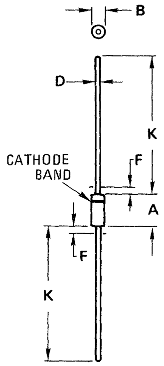
6.8 – 100 pF
30 VOLTS

SILICON EPICAP DIODES

. . . epitaxial passivated abrupt junction tuning diodes designed for electronic tuning, FM, AFC and harmonic-generation applications in AM through UHF ranges, providing solid-state reliability to replace mechanical tuning methods.

- Excellent Q Factor at High Frequencies
- Guaranteed Capacitance Change – 2.0 to 30 V
- Guaranteed Temperature Coefficient
- Capacitance Tolerance – 10%, 5.0%, and 2.0%
- Complete Typical Design Curves





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	–	1.000	–

All JEDEC dimensions and notes apply

CASE 51-02
DO-7

** MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Operating Junction Temperature Range	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

**Indicates JEDEC Registered Data.

**ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic—All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	BV_R	30	–	–	Vdc
Reverse Voltage Leakage Current	V_R = 25 Vdc, T_A = 25°C V_R = 25 Vdc, T_A = 150°C	I_R	– –	– –	0.02 20	μAdc
Series Inductance	f = 250 MHz, lead length≈1/16"	L_S	–	4.0	10	nH
Case Capacitance	f = 1.0 MHz, lead length≈1/16"	C_C	0.1	0.17	0.25	pF
Diode Capacitance Temperature Coefficient (Note 6)	V_R = 4.0 Vdc, f = 1.0 MHz	TC_c	–	300	400	ppm/°C

Device	C_T, Diode Capacitance* V_R = 4.0 Vdc, f = 1.0 MHz pF			TR, Tuning Ratio C_2/C_{30} f = 1.0 MHz		Q, Figure of Merit V_R = 4.0 Vdc f = 50 MHz
	Min (Nom -10%)	Nom	Max (Nom +10%)	Min	Max	Min
1N5441A	6.1	6.8	7.5	2.5	3.1	450
1N5442A	7.4	8.2	9.0	2.5	3.1	450
1N5443A	9.0	10.0	11.0	2.6	3.1	400
1N5444A	10.8	12.0	13.2	2.6	3.1	400
1N5445A	13.5	15.0	16.5	2.6	3.1	400
1N5446A	16.2	18.0	19.8	2.6	3.1	350
1N5447A	18.0	20.0	22.0	2.6	3.1	350
1N5448A	19.8	22.0	24.2	2.6	3.2	350
1N5449A	24.3	27.0	29.7	2.6	3.2	350
1N5450A	29.7	33.0	36.3	2.6	3.2	350
1N5451A	35.1	39.0	42.9	2.6	3.2	300
1N5452A	42.3	47.0	51.7	2.6	3.2	250
1N5453A	50.4	56.0	61.6	2.6	3.3	200
1N5454A	61.2	68.0	74.8	2.7	3.3	175
1N5455A	73.8	82.0	90.2	2.7	3.3	175
1N5456A	90.0	100.0	110.0	2.7	3.3	175

*To order devices with C_T Nom ±5.0% or ±2.0% add Suffix B or C respectively.

**Indicates JEDEC Registered Data.

PARAMETER TEST METHODS

1. **L_S, Series Inductance**
   L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter or equivalent).
2. **C_C, Case Capacitance**
   C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. **C_T, Diode Capacitance**
   ($C_T = C_C + C_J$). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
4. **TR, Tuning Ratio**
   TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.
5. **Q, Figure of Merit**
   Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

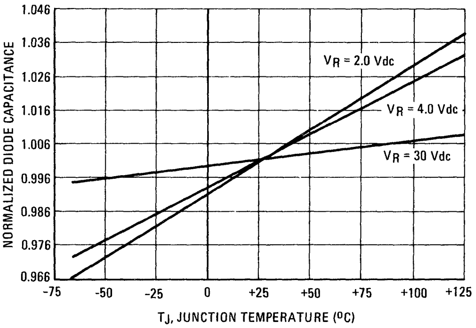
   $$Q = \frac{2\pi fC}{G}$$

   (Boonton Electronics Model 33AS8 or equivalent).
6. **TC_c, Diode Capacitance Temperature Coefficient**
   TC_c is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = -65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation, which defines TC_c:

   $$TC_c = \left| \frac{C_T(+85^\circ C) - C_T(-65^\circ C)}{85 + 65} \right| \frac{10^6}{C_T(25^\circ C)}$$

   Accuracy limited by C_T measurement to ±0.1 pF.

FIGURE 1 — NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE



TYPICAL DEVICE PERFORMANCE

FIGURE 2 – DIODE CAPACITANCE versus REVERSE VOLTAGE

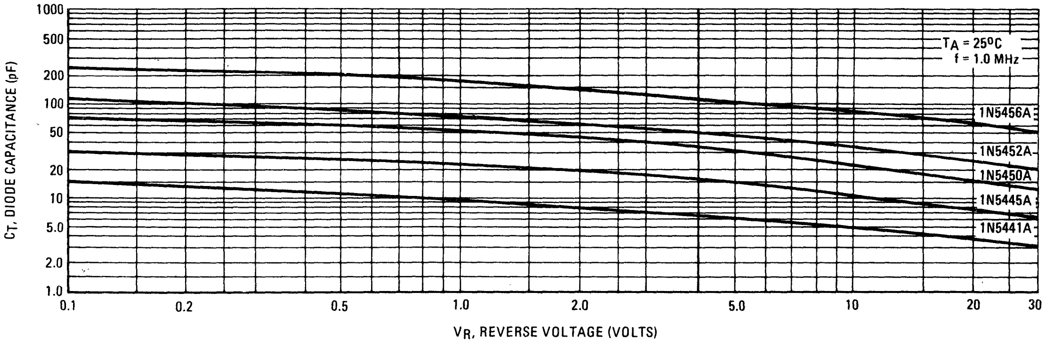


FIGURE 3 – FIGURE OF MERIT versus REVERSE VOLTAGE

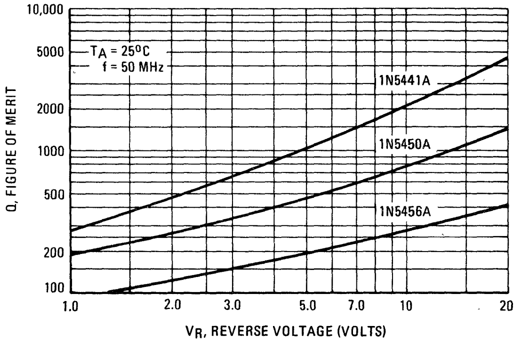


FIGURE 4 – FIGURE OF MERIT versus FREQUENCY

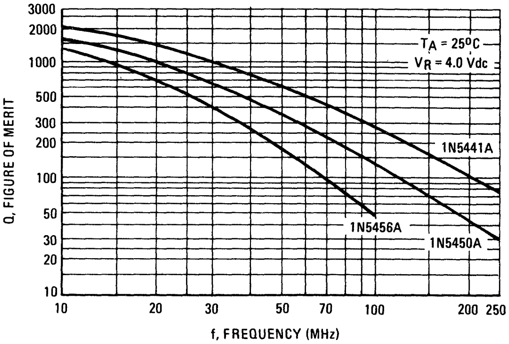


FIGURE 5 – REVERSE CURRENT versus REVERSE BIAS VOLTAGE

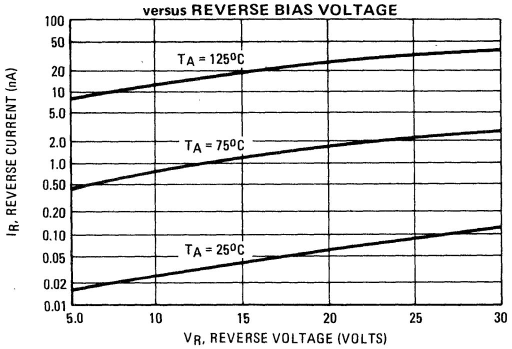
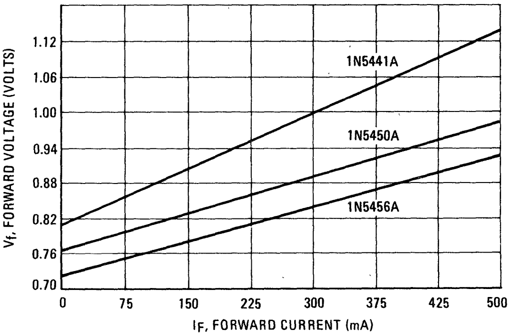


FIGURE 6 – FORWARD VOLTAGE versus FORWARD CURRENT



1N5461A,B,C (SILICON)
thru
1N5476A,B,C

VVC

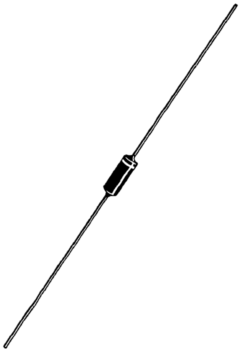
VOLTAGE-VARIABLE CAPACITANCE DIODES

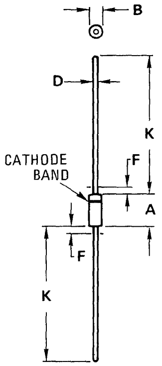
6.8 – 100 pF
30 VOLTS

SILICON EPICAP DIODES

. . . a PREMIUM line of epitaxial, passivated, abrupt-junction tuning diodes for critical and sophisticated frequency control applications through the UHF range.

- High Q at High Frequencies
- Guaranteed High Capacitance Tuning Range
- Excellent Unit-to-Unit Uniformity
- Guaranteed Temperature Coefficient
- Capacitance Tolerances – 10%, 5.0%, and 2.0%
- Complete Typical Design Curves





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	–	1.000	–

All JEDEC dimensions and notes apply

CASE 51-02
DO-7

**MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Device Dissipation @ $T_A = 25^{\circ}C$ Derate above 25°C	P_D	400 2.67	mW mW/°C
Operating Junction Temperature Range	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

**Indicates JEDEC Registered Data.

**ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic—All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 µAdc	BV_R	30	—	—	Vdc
Reverse Voltage Leakage Current	V_R = 25 Vdc, T_A = 25°C V_R = 25 Vdc, T_A = 150°C	I_R	— —	— —	0.02 20	µAdc
Series Inductance	f = 250 MHz, lead length ≈1/16"	L_S	—	4.0	10	nH
Case Capacitance	f = 1.0 MHz, lead length ≈ 1/16"	C_C	0.1	0.17	0.25	pF
Diode Capacitance Temperature Coefficient (Note 6)	V_R = 4.0 Vdc, f = 1.0 MHz	TC_c	—	300	400	ppm/°C

Device	C_T, Diode Capacitance* V_R = 4.0 Vdc, f = 1.0 MHz pF			TR, Tuning Ratio C_2/C_{30} f = 1.0 MHz		Q, Figure of Merit V_R = 4.0 Vdc f = 50 MHz
	Min (Nom −10%)	Nom	Max (Nom +10%)	Min	Max	Min
1N5461A	6.1	6.8	7.5	2.7	3.1	600
1N5462A	7.4	8.2	9.0	2.8	3.1	600
1N5463A	9.0	10.0	11.0	2.8	3.1	550
1N5464A	10.8	12.0	13.2	2.8	3.1	550
1N5465A	13.5	15.0	16.5	2.8	3.1	550
1N5466A	16.2	18.0	19.8	2.9	3.1	500
1N5467A	18.0	20.0	22.0	2.9	3.1	500
1N5468A	19.8	22.0	24.2	2.9	3.2	500
1N5469A	24.3	27.0	29.7	2.9	3.2	500
1N5470A	29.7	33.0	36.3	2.9	3.2	500
1N5471A	35.1	39.0	42.9	2.9	3.2	450
1N5472A	42.3	47.0	51.7	2.9	3.2	400
1N5473A	50.4	56.0	61.6	2.9	3.3	300
1N5474A	61.2	68.0	74.8	2.9	3.3	250
1N5475A	73.8	82.0	90.2	2.9	3.3	225
1N5476A	90.0	100.0	110.0	2.9	3.3	200

*To order devices with C_T Nom ±5.0% or ±2.0% add Suffix B or C respectively.

**Indicates JEDEC Registered Data.

PARAMETER TEST METHODS

1. **L_S, Series Inductance**
   L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter or equivalent).
2. **C_C, Case Capacitance**
   C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. **C_T, Diode Capacitance**
   (C_T = C_C + C_J). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
4. **TR, Tuning Ratio**
   TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.
5. **Q, Figure of Merit**
   Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

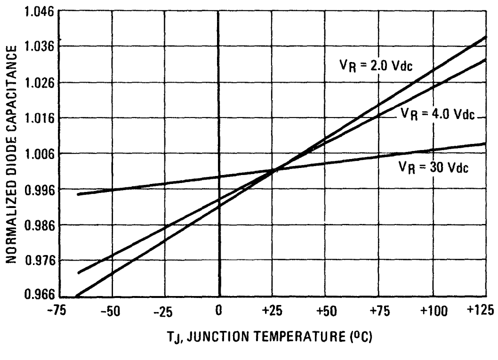
   $$Q = \frac{2\pi fC}{G}$$

   (Boonton Electronics Model 33AS8 or equivalent).
6. **TC_c, Diode Capacitance Temperature Coefficient**
   TC_c is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = −65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation, which defines TC_c:

$$TC_c = \left|\frac{C_T(+85^{\circ}C) - C_T(-65^{\circ}C)}{85 + 65}\right| \frac{10^6}{C_T(25^{\circ}C)}$$

Accuracy limited by C_T measurement to ±0.1 pF.

FIGURE 1 — NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE



TYPICAL DEVICE PERFORMANCE

FIGURE 2 – DIODE CAPACITANCE versus REVERSE VOLTAGE

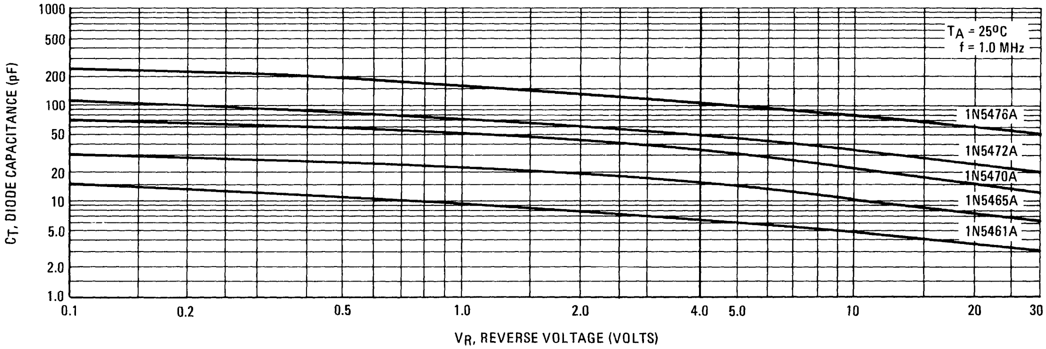


FIGURE 3 – FIGURE OF MERIT versus REVERSE VOLTAGE

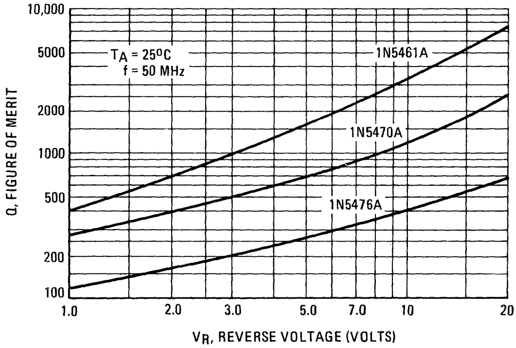


FIGURE 4 – FIGURE OF MERIT versus FREQUENCY

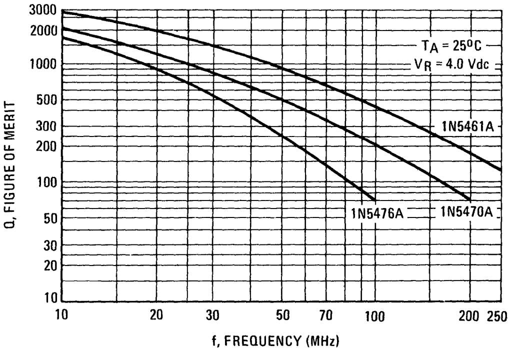


FIGURE 5 – REVERSE CURRENT versus REVERSE BIAS VOLTAGE

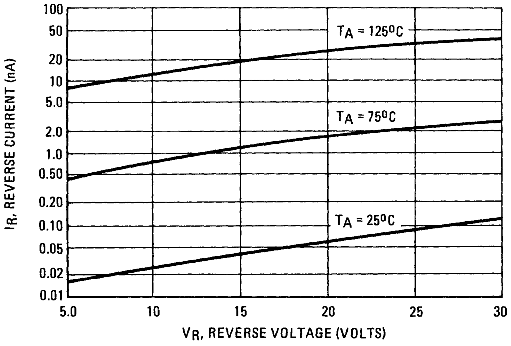
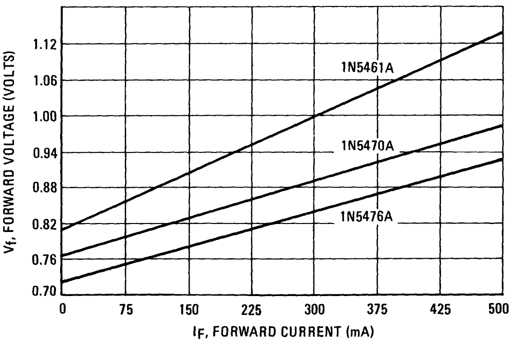


FIGURE 6 – FORWARD VOLTAGE versus FORWARD CURRENT



EPICAP VOLTAGE-VARIABLE CAPACITANCE DIODE DEVICE CONSIDERATIONS

A. Epicap Network Presentation

The equivalent circuit in Figure 7 shows the voltage capacitance and parasitic elements of an EPICAP diode. For design purposes at all but very high and very low frequencies, L_S, R_J, and C_C can be neglected. The simplified equivalent circuit of Figure 8 represents the diode under these conditions.

Definitions:

C_J – Voltage-Variable Junction Capacitance
R_S – Series Resistance (semiconductor bulk, contact, and lead resistance)
C_C – Case Capacitance
L_S – Series Inductance
R_J – Voltage-Variable Junction Resistance (negligible above 100 kHz)

FIGURE 7

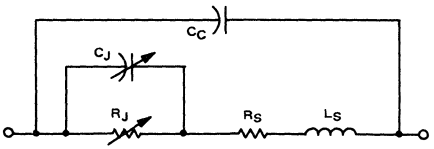


FIGURE 8

B. Epicap Capacitance versus Reverse Bias Voltage

The most important design characteristic of an EPICAP diode is the C_T versus V_R variation as shown in equations 1 and 2. Tuning Ratio, TR, between any two voltage points on curve of equation (2) is determined from equations (3) and (4).

$$C_T = C_C + C_J \qquad (1)$$

$$C_T = C_C + \frac{C_o}{\left(1 + \frac{V_R}{\phi}\right)^{\gamma}} \qquad (2)$$

C. Epicap Capacitance versus Frequency

Variations in EPICAP effective capacitance, as a function of operating frequency, can be derived from a simplified equivalent circuit similar to that of Figure 7, but neglecting R_S and R_J. The admittance expression for such a circuit is given in equation 5. Examination of equation 5 yields the following information:

At low frequencies, $C_{eq} \approx C_J$; at very high frequencies ($f \approx \infty$) $C_{eq} \approx C_C$.

As frequency is increased from 1.0 MHz, C_{eq} increases until it is maximum at $\omega^2 = 1/L_SC_J$; and as ω^2 is increased from $1/L_SC_J$ toward infinity, C_{eq} increases from a very negative capacitance (inductance) toward $C_{eq} = C_C$, a positive capacitance.

Very simple calculations for C_{eq} at higher frequencies indicate the problems encountered when capacity measurements are made above 1.0 MHz. As ω approaches $\omega_o = 1/\sqrt{L_SC_J}$, small variations in L_S cause extreme variations in measured diode capacitance.

$$\text{TR Junction} = \frac{C_{J1}}{C_{J2}} = \left(\frac{V_{R2} + \phi}{V_{R1} + \phi}\right)^{\gamma} \qquad (3)$$

$$\text{TR Diode} = \frac{C_{T1}}{C_{T2}} = \frac{C_{J1} + C_C}{C_{J2} + C_C} \qquad (4)$$

$C_o = C_J$ at $V_R = 0$
V_R = Reverse Bias (Volts)
γ, Diode Power Law, ≈ 0.44
ϕ, Contact Potential, ≈ 0.6 Volt
$C_c \approx 0.17$ pF

$$Y = j\omega C_{eq} = j\omega C_C + \frac{j\omega C_J}{1 - \omega^2 L_S C_J} \qquad (5)$$

D. EPICAP Figure of Merit (Q) and Cutoff Frequency (f_{co})

The efficiency of EPICAP response to an input frequency is related to the Figure of Merit of the device as defined in equation 6. For very low frequencies, equation 7 applies whereas at high frequencies, where R_J can be neglected, equation 6 may be rewritten into the familiar form of equation 8.

Another useful parameter for EPICAP devices is the cutoff frequency (f_{co}), and is the frequency point where Q is equal to 1. Equation 9 gives this relationship.

$$Q = \frac{X_{Seq}}{R_{Seq}} \qquad (6)$$

$$Q_{Lf} = \frac{\omega C_J R_J^2}{R_J + R_S(1 + \omega^2 C_J^2 R_J^2} \qquad (7)$$

$$Q_{hf} = \frac{1}{\omega R_S C_{eq}} \qquad (8)$$

$$f_{co} = Qf_{max} \quad \frac{1}{2\pi R_S C_{BVR}} \qquad (9)$$

E. Harmonic Generation Using EPICAPS

Efficient harmonic generation is possible with EPICAPS because of their high cutoff frequency and breakdown voltage. Since EPICAP junction capacitance varies inversely with the square root of the breakdown voltage, harmonic generator performance can be accurately predicted from various idealized models. Equation 10 gives the level of maximum input power for the EPICAP and equation 11 gives the relationships governing EPICAP circuit efficiency. In these equations, adequate heat sinking has been assumed.

$$P_{in(max)} = \frac{M(BV_R + \phi)^2}{R_S} \; \frac{f_{in}}{f_{co}} \qquad (10)$$

$M(x2) = 0.0285$; $M(x3) = 0.0241$; $M(x4) = 0.196$

$$Eff = 1 - N \frac{f_{out}}{f_{co}} \qquad (11)$$

$N(x2) = 20.8$; $N(x3) = 34.8$; $N(x4) = 62.5$

M and N are Constants

1N5518, A, B (SILICON)
thru
1N5546, A, B

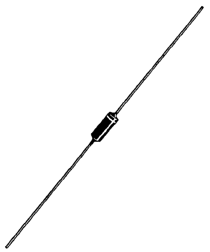
LOW VOLTAGE AVALANCHE SILICON OXIDE PASSIVATED ZENER REGULATOR DIODES

Highly reliable silicon regulators utilizing an oxide-passivated junction for long-term voltage stability. RamRod construction provides a rugged, glass-enclosed, hermetically sealed structure.

- Low Zener Noise Specified
- Low Maximum Regulation Factor
- Low Zener Impedance
- Low Leakage Current
- Controlled Forward Characteristics
- Temperature Range: -65 to + 200°C

LOW VOLTAGE AVALANCHE ZENER DIODES

400 MILLIWATTS
3.3 THRU 33 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Power Dissipation @ T_A = 50°C Derate above 50°C	P_D	400 2.66	mW mW/°C
DC Power Dissipation @ T_L = 50°C Lead Length = 1/8" Derate above 50°C (Figure 1)	P_D	500 3.3	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

MECHANICAL CHARACTERISTICS

CASE: Hermetically sealed, all-glass

DIMENSIONS: See outline drawing.

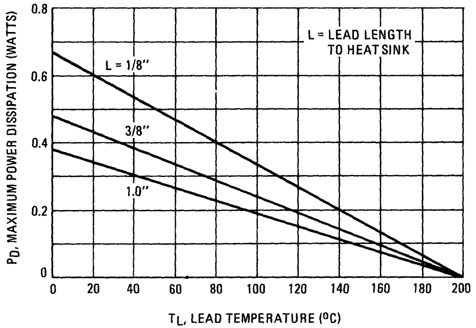
FINISH: All external surfaces are corrosion resistant and leads are readily solderable and weldable.

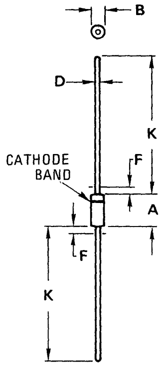
POLARITY: Cathode indicated by polarity band.

WEIGHT: 0.2 Gram (approx)

MOUNTING POSITION: Any

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	–	1.000	–

All JEDEC dimensions and notes apply

CASE 51-02
DO-7

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted. Based on dc measurements at thermal equilibrium; V_F = 1.1 Max @ I_F = 200 mA for all types)

JEDEC Type No. (Note 1)	Nominal Zener Voltage V_Z @ I_{ZT} Volts (Note 2)	Test Current I_{ZT} mAdc	Max Zener Impedance B-C-D Suffix Z_{ZT} @ I_{ZT} Ohms (Note 3)	Max Reverse Leakage Current			B-C-D Suffix Maximum DC Zener Current I_{ZM} mAdc (Note 5)	B-C-D Suffix Max Noise Density at I_Z = 250 µA N_D (Figure 1) (micro-volts per square root cycle)	Regulation Factor ΔV_Z Volts (Note 6)	Low V_Z Current I_{ZL} mAdc
				I_R µAdc (Note 4)	V_R – Volts Non & A-Suffix	V_R – Volts B-C-D Suffix				
1N5518	3.3	20	26	5.0	0.90	1.0	115	0.5	0.90	2.0
1N5519	3.6	20	24	3.0	0.90	1.0	105	0.5	0.90	2.0
1N5520	3.9	20	22	1.0	0.90	1.0	98	0.5	0.85	2.0
1N5521	4.3	20	18	3.0	1.0	1.5	88	0.5	0.75	2.0
1N5522	4.7	10	22	2.0	1.5	2.0	81	0.5	0.60	1.0
1N5523	5.1	5.0	26	2.0	2.0	2.5	75	0.5	0.65	0.25
1N5524	5.6	3.0	30	2.0	3.0	3.5	68	1.0	0.30	0.25
1N5525	6.2	1.0	30	1.0	4.5	5.0	61	1.0	0.20	0.01
1N5526	6.8	1.0	30	1.0	5.5	6.2	56	1.0	0.10	0.01
1N5527	7.5	1.0	35	0.5	6.0	6.8	51	2.0	0.05	0.01
1N5528	8.2	1.0	40	0.5	6.5	7.5	46	4.0	0.05	0.01
1N5529	9.1	1.0	45	0.1	7.0	8.2	42	4.0	0.05	0.01
1N5530	10.0	1.0	60	0.05	8.0	9.1	38	4.0	0.10	0.01
1N5531	11.0	1.0	80	0.05	9.0	9.9	35	5.0	0.20	0.01
1N5532	12.0	1.0	90	0.05	9.5	10.8	32	10	0.20	0.01
1N5533	13.0	1.0	90	0.01	10.5	11.7	29	15	0.20	0.01
1N5534	14.0	1.0	100	0.01	11.5	12.6	27	20	0.20	0.01
1N5535	15.0	1.0	100	0.01	12.5	13.5	25	20	0.20	0.01
1N5536	16.0	1.0	100	0.01	13.0	14.4	24	20	0.20	0.01
1N5537	17.0	1.0	100	0.01	14.0	15.3	22	20	0.20	0.01
1N5538	18.0	1.0	100	0.01	15.0	16.2	21	20	0.20	0.01
1N5539	19.0	1.0	100	0.01	16.0	17.1	20	20	0.20	0.01
1N5540	20.0	1.0	100	0.01	17.0	18.0	19	20	0.20	0.01
1N5541	22.0	1.0	100	0.01	18.0	19.8	17	20	0.25	0.01
1N5542	24.0	1.0	100	0.01	20.0	21.6	16	20	0.30	0.01
1N5543	25.0	1.0	100	0.01	21.0	22.4	15	20	0.35	0.01
1N5544	28.0	1.0	100	0.01	23.0	25.2	14	20	0.40	0.01
1N5545	30.0	1.0	100	0.01	24.0	27.0	13	20	0.45	0.01
1N5546	33.0	1.0	100	0.01	28.0	29.7	12	20	0.50	0.01

NOTE 1 – TOLERANCE AND VOLTAGE DESIGNATION

The JEDEC type numbers shown are ±20% with guaranteed limits for only V_Z, I_R, and V_F. Units with "A" suffix are ±10% with guaranteed limits for V_Z, I_R, and V_F. Units with guaranteed limits for all six parameters are indicated by a "B" suffix for ±5.0% units, "C" suffix for ±2.0% and "D" suffix for ±1.0%.

NOTE 2 – ZENER VOLTAGE (V_Z) MEASUREMENT

Nominal zener voltage is measured with the device junction in thermal equilibrium with ambient temperature of 25°C.

NOTE 3 – ZENER IMPEDANCE (Z_Z) DERIVATION

The zener impedance is derived from the 60 Hz ac voltage, which results when an ac current having an rms value equal to 10% of the dc zener current (I_{ZT}) is superimposed on I_{ZT}.

NOTE 4 – REVERSE LEAKAGE CURRENT (I_R)

Reverse leakage currents are guaranteed and are measured at V_R as shown on the table.

NOTE 5 – MAXIMUM REGULATOR CURRENT (I_{ZM})

The maximum current shown is based on the maximum voltage of a 5.0% type unit, therefore, it applies only to the "B" suffix device. The actual I_{ZM} for any device may not exceed the value of 400 milliwatts divided by the actual V_Z of the device.

NOTE 6 – MAXIMUM REGULATION FACTOR (ΔV_Z)

ΔV_Z is the maximum difference between V_Z at I_{ZT} and V_Z at I_{ZL} measured with the device junction in thermal equilibrium.

ZENER NOISE DENSITY

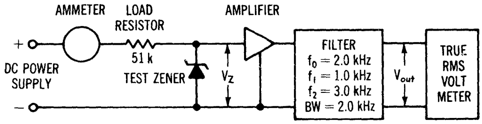
A zener diode generates noise when it is biased in the zener direction. A small part of this noise is due to the internal resistance associated with the device. A larger part of zener noise is a result of the zener breakdown phenomenon and is called microplasma noise. To eliminate the higher frequency components of noise a small shunting capacitor can be used. The lower frequency noise generally must be tolerated since a capacitor required to eliminate the lower frequencies would degrade the regulation properties of the zener in many applications.

Motorola is rating this series with a maximum noise density at 250 microamperes, a bandwidth of 2.0 kHz and a center frequency of 2.0 kHz.

Noise density decreases as zener current increases. The junction temperature will also change the zener noise levels, thus the noise rating must indicate frequency, bandwidth, current level and temperature.

The block diagram shown in Figure 2 represents the method used to measure noise density. The input voltage and load resistance is high so that the zener is driven from a constant current source. The amplifier must be low noise so that the amplifier noise is negligible compared to the test zener. The filter frequency and bandpass is known so that the noise density in volts RMS per square root cycle can be calculated.

FIGURE 2 — NOISE DENSITY MEASUREMENT METHOD



NOISE DENSITY (VOLTS PER SQUARE ROOT BANDWIDTH) = $\dfrac{V_{out}}{\text{OVERALL GAIN}\ \sqrt{BW}}$

WHERE: BW = FILTER BANDWIDTH (Hz)
V_{out} = OUTPUT NOISE (VOLTS RMS)

FIGURE 3 — TYPICAL CAPACITANCE

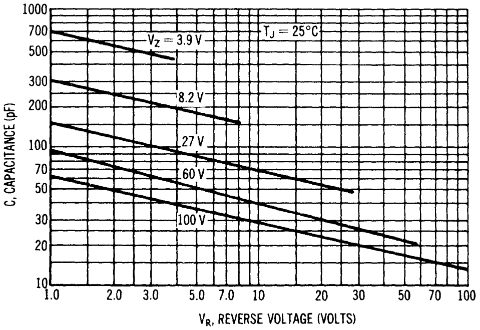
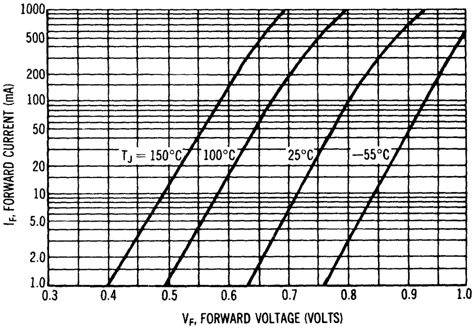


FIGURE 4 — TYPICAL FORWARD CHARACTERISTICS



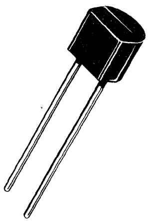
1N5758,A thru 1N5762,A (SILICON)

SILICON 3-LAYER BILATERAL TRIGGERS

. . . Annular , two terminal devices that exhibit bi-directional negative resistance switching characteristics. These economical, durable devices have been developed for use in thyristor triggering circuits for lamp drivers and universal motor speed controls.

- Switching Voltage Range – 20 to 36 Volts Nominal
- Symmetrical Characteristics
- Passivated Surface for Reliability and Uniformity

SILICON BILATERAL TRIGGERS



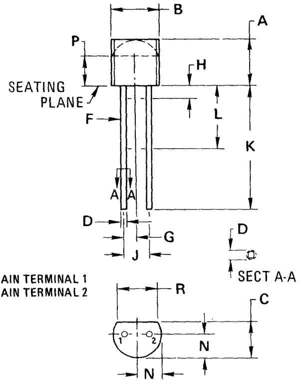
***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Pulse Current (30 μs duration, 120 Hz repetition rate)	I_{pulse}	2.0	Amp
Power Dissipation @ T_A = -40 to +25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Switching Voltage (Both Directions)	1N5758	V_S	16	24	Volts
	1N5759		20	28	
	1N5760		24	32	
	1N5761		28	36	
	1N5762		32	40	
	1N5758A		18	22	
	1N5759A		22	26	
	1N5760A		26	30	
	1N5761A		30	34	
	1N5762A		34	38	
Switching Current (Both Directions) (T_A = -40 to +75°C)	1N5758/5762	I_S	–	100	μA
	1N5758A/5762A		–	25	
Switching Voltage Change (Both Directions) (ΔI = I_S to I = 10 mA)	1N5758,A,1N5759,A	ΔV	5.0	–	Volts
	1N5760,A,61,A,62,A		7.0	–	
Leakage Current (Both Directions), (Applied Voltage = 14 Volts)		I_B	–	10	μA
Switching Voltage Symmetry	1N5758/5762	$(V_S+)-(V_S-)$	–	± 4.0	Volts
	1N5758A/5762A		–	± 2.0	
Peak Pulse Amplitude (Figure 1) (Both Polarities)	1N5758,A,1N5759,A		3.0	–	Volts
	1N5760,A,61,A,62,A		5.0	–	

*Indicates JEDEC Registered Data.



STYLE 3:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

CASE 182-02

TYPICAL ELECTRICAL CHARACTERISTICS

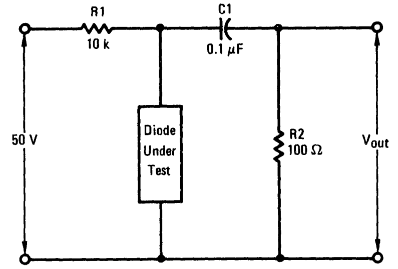


FIGURE 1 – PEAK PULSE AMPLITUDE TEST CIRCUIT

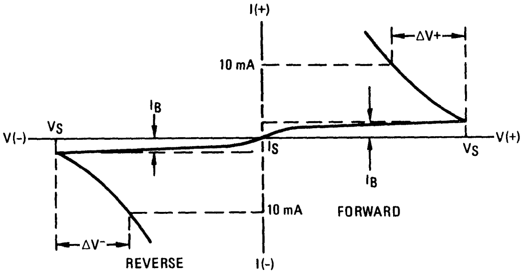


FIGURE 2 – VOLT-AMPERE CHARACTERISTICS

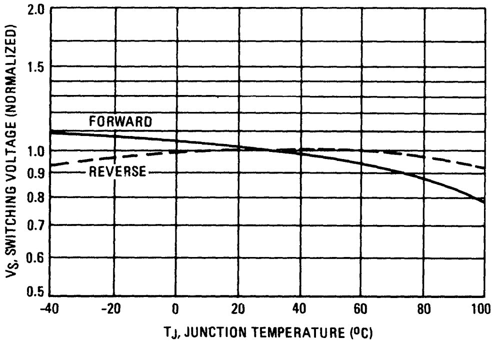


FIGURE 3 – BREAKOVER VOLTAGE BEHAVIOR

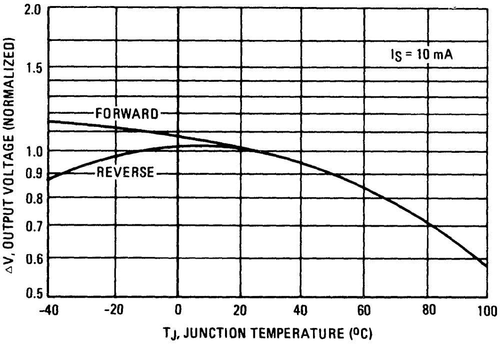


FIGURE 4 – NORMALIZED OUTPUT VOLTAGE BEHAVIOR

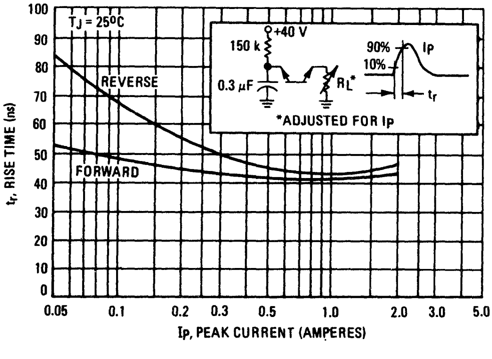


FIGURE 5 – SWITCHING TIMES

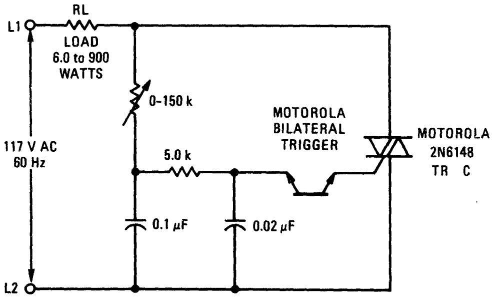


FIGURE 6 – CONTROL CIRCUIT

1N5779 thru 1N5793 For Specifications, See 1N5158 Data.

1N5820
1N5821

Designers Data Sheet

HOT CARRIER POWER RECTIFIERS

. . . employing the Schottky Barrier principle in a large area metal-to-silicon power diode. State of the art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high-frequency inverters, free wheeling diodes, and polarity protection diodes.

- Extremely Low v_F
- Low Stored Charge, Majority Carrier Conduction
- Low Power Loss/High Efficiency
- High Surge Capacity

Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

SCHOTTKY BARRIER RECTIFIERS

3.0 AMPERE
20, 30 VOLTS

*MAXIMUM RATINGS

Rating	Symbol	1N5820	1N5821	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	24	36	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	14	21	Volts
Average Rectified Forward Current (2) $V_{R(equiv)} \leqslant 0.2\,V_R(dc)$, $T_L = 95^{\circ}C$ ($R_{\theta JA} = 28^{\circ}C/W$, P.C. Board Mounting, See Note 2)	I_O	3.0		Amp
Ambient Temperature Rated V_R (dc), $P_{F(AV)} = 0$ $R_{\theta JA} = 28^{\circ}C/W$	T_A	90	85	°C
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, halfwave, single phase 60 Hz, $T_L = 75^{\circ}C$)	I_{FSM}	250 (for 1 cycle)		Amp
Operating and Storage Junction Temperature Range (Reverse Voltage applied)	T_J, T_{stg}	-65 to +125		°C
Peak Operating Junction Temperature (Forward Current Applied)	$T_{J(pk)}$	150		°C

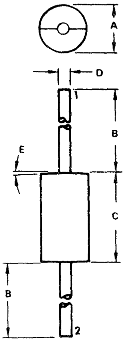
*THERMAL CHARACTERISTICS (Note 2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	28	°C/W

*ELECTRICAL CHARACTERISTICS ($T_L = 25^{\circ}C$ unless otherwise noted.) (2)

Characteristic	Symbol	1N5820	1N5821	Unit
Maximum Instantaneous Forward Voltage (1)	v_F			Volts
(i_F = 1.0 Amp)		0.370	0.380	
(i_F = 3.0 Amp)		0.475	0.500	
(i_F = 9.4 Amp)		0.850	0.900	
Maximum Instantaneous Reverse Current @ rated dc Voltage (1)	I_R			mA
$T_L = 25^{\circ}C$		2.0	2.0	
$T_L = 100^{\circ}C$		20	20	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
(2) Lead Temperature reference is cathode lead 1/32" from Case.
*Indicates JEDEC Registered Data.



	MILLIMETERS		INCHES	
A	4.83	5.33	0.190	0.210
B	26.97	27.23	1.062	1.072
C	9.40	9.65	0.370	0.380
D	1.22	1.32	0.048	0.052
E	2°		2°	

CASE 267

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded

FINISH: All external surfaces corrosion-resistant and the terminal leads are readily solderable.

POLARITY: Cathode indicated by polarity band

MOUNTING POSITIONS: Any

SOLDERING: 220°C 1/16" from case for 10 s.

NOTE 1: DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 0.1 V_{RWM}. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA}\,P_{F(AV)} - R_{\theta JA}\,P_{R(AV)} \qquad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest).

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figures 1 and 2 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA}\,P_{R(AV)} \qquad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA}\,P_{F(AV)} \qquad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figures 1 and 2 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1 and 2 is based upon dc conditions. For use in common rectifier circuits, Table I indicates suggested factors for an equivalent dc voltage to use for conservative design; i.e.:

$$V_{R(equiv)} = V_{(FM)} \times F \qquad (4)$$

The Factor F is derived by considaring the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

Example: Find $T_{A(max)}$ for 1N5821 operated in a 12-Volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 2.0 A ($I_{F(AV)}$ = 1.0 A), $I_{(FM)}/I_{(AV)}$ = 10, Input Voltage = 10 $V_{(rms)}$, $R_{\theta JA}$ = 40°C/W.

Step 1: Find $V_{R(equiv)}$. Read F = 0.65 from Table I ∴
$V_{R(equiv)} = (1.41)(10)(0.65) = 9.2$ V

Step 2 Find T_R from Figure 2. Read T_R = 108°C @ V_R = 9.2 V & $R_{\theta JA}$ = 40°C/W.

Step 3 Find $P_{F(AV)}$ from Figure 3. **Read $P_{F(AV)}$ = 0.85 W @ $\frac{I_{(FM)}}{I_{(AV)}} = 10$ & $I_{F(AV)}$ = 1.0 A

Step 4: Find $T_{A(max)}$ from equation (3).
$T_{A(max)} = 108 - (0.85)(40) = 74$°C

**Values given are for the 1N5821. Power is slightly lower for the 1N5820 because of its lower forward voltage.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped *†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

*Note that $V_{R(PK)} \approx 2\,V_{in(PK)}$. †Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE – 1N5820

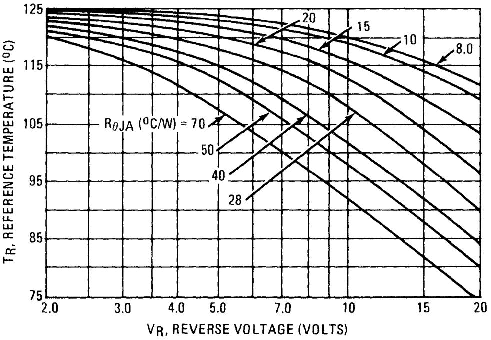


FIGURE 2 – MAXIMUM REFERENCE TEMPERATURE – 1N5821

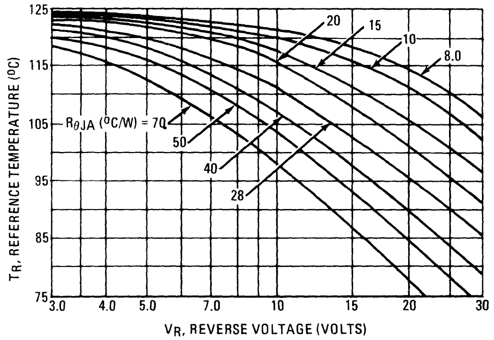
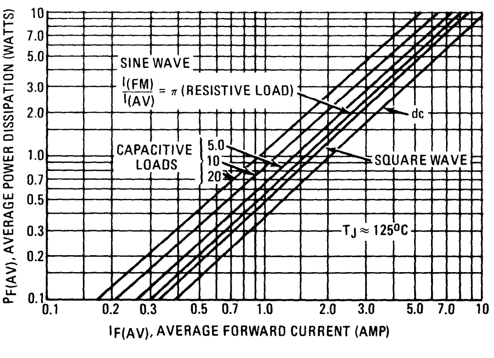
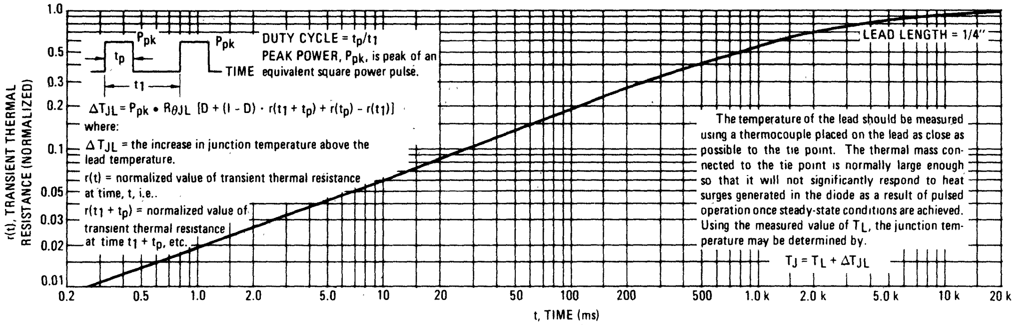


FIGURE 3 – FORWARD POWER DISSIPATION



THERMAL CHARACTERISTICS

FIGURE 4 – THERMAL RESPONSE



DUTY CYCLE = t_p/t_1

PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

$\Delta T_{JL} = P_{pk} \bullet R_{\theta JL}\ [D + (I - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$

where:

ΔT_{JL} = the increase in junction temperature above the lead temperature.

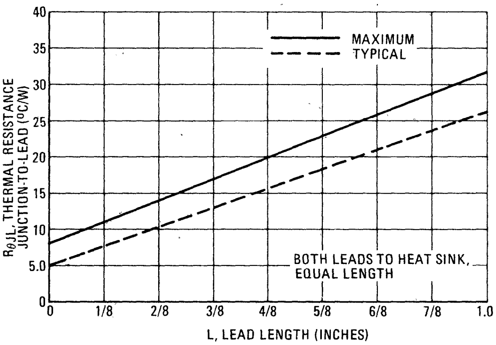
r(t) = normalized value of transient thermal resistance at time, t, i.e..

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$, etc.

The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by.

$T_J = T_L + \Delta T_{JL}$

FIGURE 5 – STEADY – STATE THERMAL RESISTANCE



NOTE 2 – MOUNTING DATA

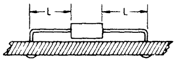
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering, or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

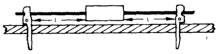
MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.



MOUNTING METHOD 2

Vector Push-In Terminals T-28



MOUNTING METHOD 3

P.C. Board with 2-1/2″ x 2-1/2″ Copper Surface

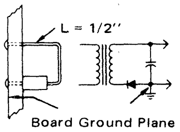
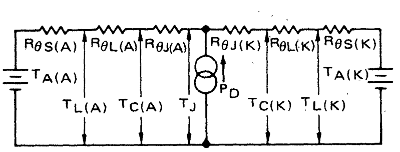


FIGURE 6 – APPROXIMATE THERMAL CIRCUIT MODEL



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts (A) and (K) refer to anode and cathode sides respectively.) Values for thermal resistance components are:

$R_{\theta L}$ = 42°C/W/IN. Typically and 48°C/W/IN. Maximum.
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum.

The maximum lead temperature may be found as follows:

$$T_L = T_{J(max)} - \Delta T_{JL}$$

Where: $\Delta T_{JL} \approx R_{\theta JL} \bullet P_D$

FIGURE 7 – TYPICAL FORWARD VOLTAGE

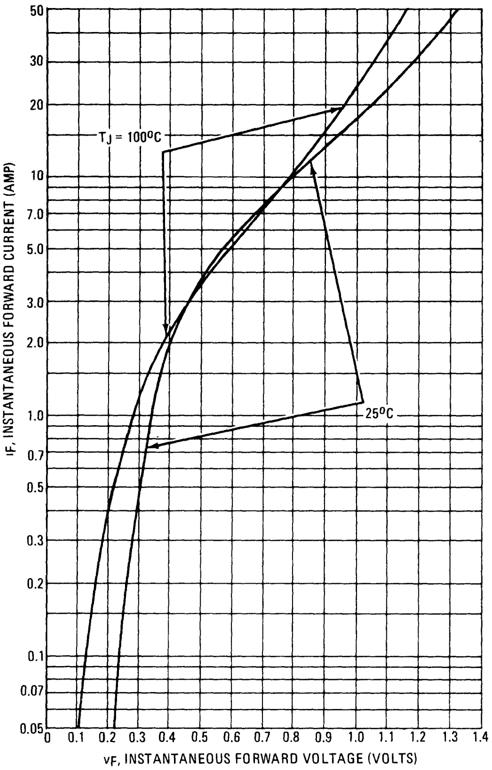


FIGURE 8 – MAXIMUM NON-REPETITIVE SURGE CURRENT

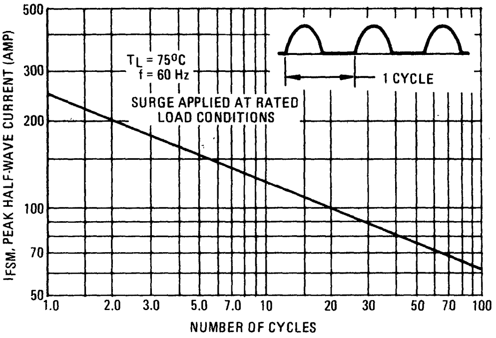


FIGURE 9 – TYPICAL REVERSE CURRENT

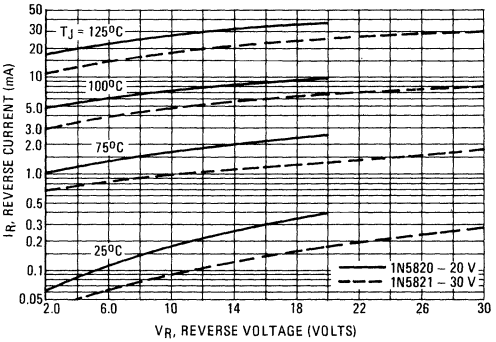
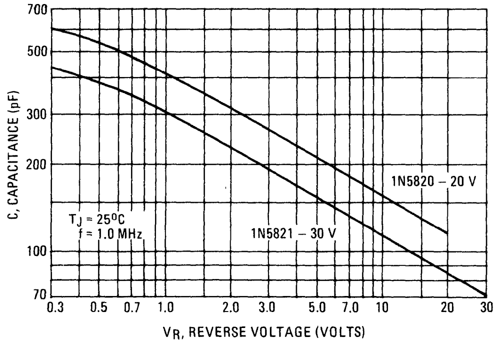


FIGURE 10 – CAPACITANCE



NOTE 3 – HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 10.)

1N5823, 1N5824, 1N5825 (SILICON)

Designers Data Sheet

HOT CARRIER POWER RECTIFIERS

. . . employing the Schottky Barrier principle in a large area metal-to-silicon power diode. State of the art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high-frequency inverters, free wheeling diodes, and polarity protection diodes.

- Extremely Low v_F
- Low Stored Charge, Majority Carrier Conduction
- Low Power Loss/High Efficiency
- High Surge Capacity

Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

*MAXIMUM RATINGS

Rating	Symbol	1N5823	1N5824	1N5825	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	40	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	24	36	48	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	14	21	28	Volts
Average Rectified Forward Current $V_{R(equiv)} \leq 0.2\ V_R$ (dc), $T_C = 75°C$ $V_{R(equiv)} \leq 0.2\ V_R$ (dc), $T_L = 80°C$ ($R_{\theta JA} = 25°C/W$, P.C. Board Mounting, See Note 3)	I_O	← 15 → ← 5.0 →			Amp
Ambient Temperature Rated V_R (dc), $P_{F(AV)} = 0$ $R_{\theta JA} = 25°C/W$	T_A	65	60	55	°C
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, halfwave, single phase 60 Hz)	I_{FSM}	← 500 (for 1 cycle) →			Amp
Operating and Storage Junction Temperature Range (Reverse Voltage applied)	T_J, T_{stg}	← -65 to +125 →			°C
Peak Operating Junction Temperature (Forward Current Applied)	$T_{J(pk)}$	← 150 →			°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.0	°C/W

*ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted.)

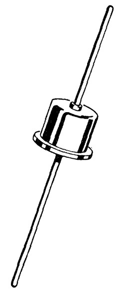
Characteristic	Symbol	1N5823	1N5824	1N5825	Unit
Maximum Instantanous Forward Voltage (1)	v_F				Volts
($i_F = 3.0$ Amp)		0.330	0.340	0.350	
($i_F = 5.0$ Amp)		0.360	0.370	0.380	
($i_F = 15.7$ Amp)		0.470	0.490	0.520	
Maximum Instantanous Reverse Current @ rated dc Voltage	I_R				mA
$T_C = 25°C$		10	10	10	
$T_C = 100°C$		75	75	75	

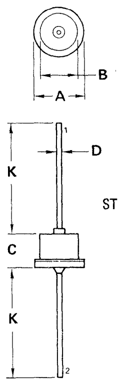
(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2.0%.

*Indicates JEDEC Registered Data.

SCHOTTKY BARRIER RECTIFIERS

5 AMPERE
20, 30, 40 VOLTS





STYLE 1:
PIN 1. CATHODE
2. ANODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	11.43	–	0.450
B	–	8.89	–	0.350
C	–	7.62	–	0.300
D	1.17	1.42	0.046	0.056
K	24.89	–	0.980	–

CASE 60

MECHANICAL CHARACTERISTICS

CASE: Welded, hermetically sealed construction.

FINISH: All external surfaces corrosion-resistant and the terminal leads are readily solderable.

POLARITY: Cathode to case.

MOUNTING POSITIONS: Any

NOTE 1: DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 0.1 V_{RWM}. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} P_{F(AV)} - R_{\theta JA} P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest).

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figures 1, 2 and 3 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA} P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA} P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figures 1, 2 and 3 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1, 2 and 3 is based upon dc conditions. For use in common rectifier circuits, Table I indicates suggested factors for an equivalent dc voltage to use for conservative design; i.e.:

$$V_{R(equiv)} = V_{IN(PK)} \times F \quad (4)$$

The Factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

Example: Find $T_{A(max)}$ for 1N5825 operated in a 12-Volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 10 A ($I_{F(AV)}$ = 5 A), $I_{(PK)}/I_{(AV)}$ = 10, Input Voltage = 10 V(rms), $R_{\theta JA}$ = 10°C/W.

Step 1: Find $V_{R(equiv)}$. Read F = 0.65 from Table I ∴ $V_{R(equiv)}$ = (1.41)(10)(0.65) = 9.2 V

Step 2: Find T_R from Figure 3. Read T_R = 118°C @ V_R = 9.2 V & $R_{\theta JA}$ = 10°C/W.

Step 3: Find $P_{F(AV)}$ from Figure 4. †Read $P_{F(AV)}$ = 5.5 W @ $\frac{I_{(PK)}}{I_{(AV)}}$ = 10 & $I_{F(AV)}$ = 5 A

Step 4: Find $T_{A(max)}$ from equation (3). $T_{A(max)}$ = 118-(10)(5.5) = 63°C.

†Values given are for the 1N5825. Power is slightly lower for the other units because of their lower forward voltage.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped (1),(2)	
Load	**Resistive**	**Capacitive (1)**	**Resistive**	**Capacitive**	**Resistive**	**Capacitive**
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

(1) Note that $V_{R(PK)} \approx 2\ V_{in(PK)}$ (2) Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE – 1N5823

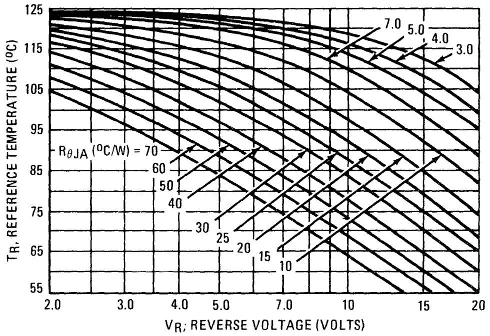


FIGURE 2 – MAXIMUM REFERENCE TEMPERATURE – 1N5824

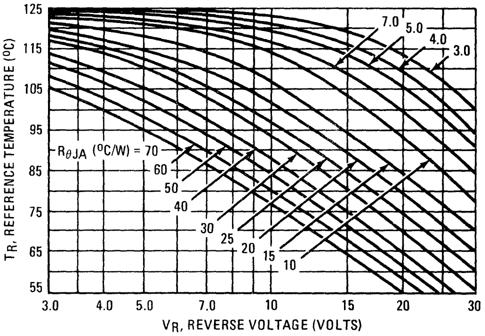


FIGURE 3 – MAXIMUM REFERENCE TEMPERATURE – 1N5825

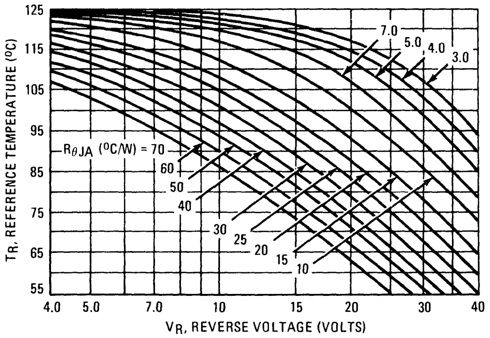
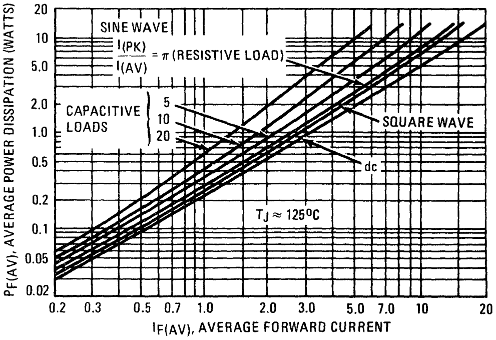
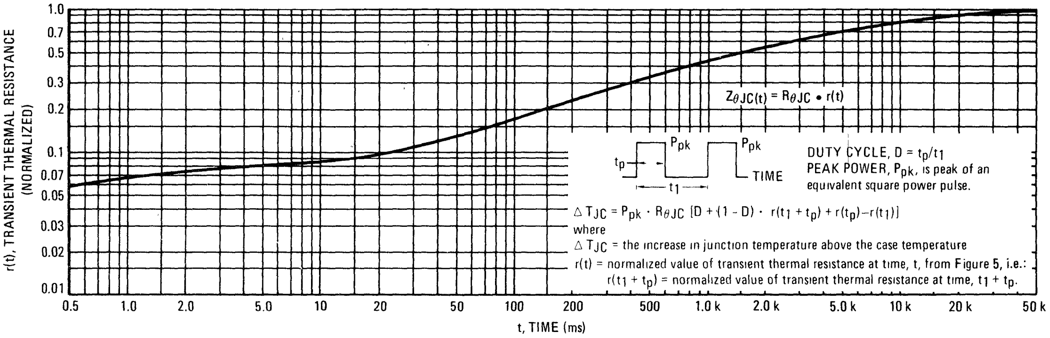


FIGURE 4 – FORWARD POWER DISSIPATION

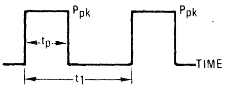


THERMAL CHARACTERISTICS

FIGURE 5 – THERMAL RESPONSE



NOTE 2 – FINDING JUNCTION TEMPERATURE



DUTY CYCLE, D = t_p/t_1
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended

The temperature of the case should be measured using a thermocouple placed on the case at the temperature reference point (see Note 3) The thermal mass connected to the case is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved Using the measured value of T_C, the junction temperature may be determined by

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by

$$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC} [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where

$r(t)$ = normalized value of transient thermal resistance at time, t, from Figure 5. i.e.

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$

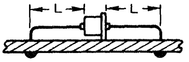
NOTE 3 – MOUNTING DATA

Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering.

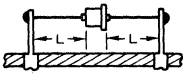
TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN) 1/4	1	$R_{\theta JA}$
1	55	60	°C/W
2	65	70	°C/W
3	25		°C/W

MOUNTING METHOD 1



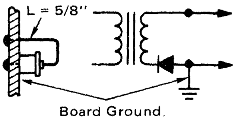
MOUNTING METHOD 2



Vector pin mounting

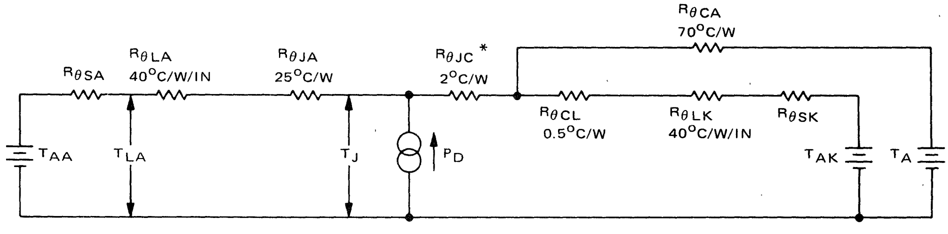
MOUNTING METHOD 3

P. C. Board with
2 1/2" x 2 1/2" copper surface



Board Ground Plane

FIGURE 6 – APPROXIMATE THERMAL CIRCUIT MODEL



Use of the above model permits calculation of average junction temperature for any mounting situation. Lowest values of thermal resistance will occur when the cathode lead is brought as close as possible to a heat dissipator; as heat conduction through the anode lead is small. Terms in the model are defined as follows:

*Case temperature reference is at cathode end.

TEMPERATURES

T_A = Ambient
T_{AA} = Anode Heat Sink Ambient
T_{AK} = Cathode Heat Sink Ambient
T_{LA} = Anode Lead
T_{LK} = Cathode Lead
T_J = Junction

THERMAL RESISTANCES

$R_{\theta CA}$ = Case to Ambient
$R_{\theta SA}$ = Anode Lead Heat Sink to Ambient
$R_{\theta SK}$ = Cathode Lead Heat Sink to Ambient
$R_{\theta LA}$ = Anode Lead
$R_{\theta LK}$ = Cathode Lead
$R_{\theta CL}$ = Case to Cathode Lead
$R_{\theta JC}$ = Junction to Case
$R_{\theta JA}$ = Junction to Anode Lead (S bend)

FIGURE 7 – TYPICAL FORWARD VOLTAGE

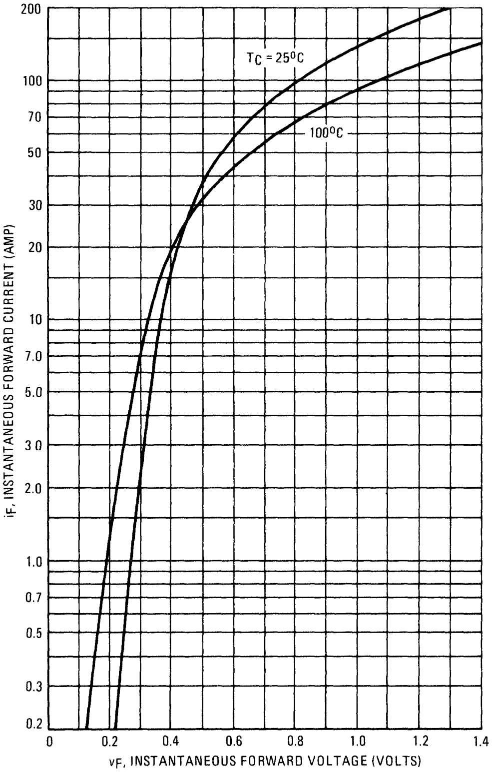


FIGURE 8 – MAXIMUM SURGE CAPABILITY

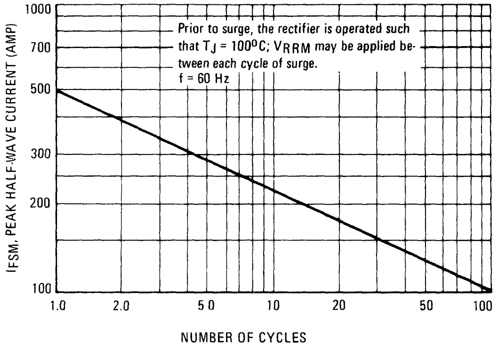

Prior to surge, the rectifier is operated such that $T_J = 100^{\circ}C$; V_{RRM} may be applied between each cycle of surge.
f = 60 Hz

FIGURE 9 – TYPICAL REVERSE CURRENT

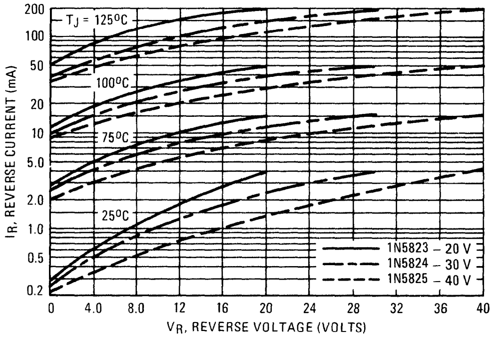
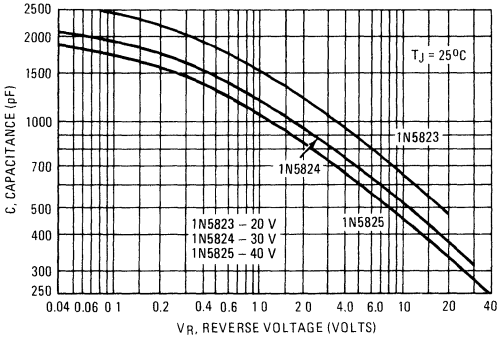


FIGURE 10 – CAPACITANCE



NOTE 4 – HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 10).

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, whereas perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss; it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

1N5826, 1N5827, 1N5828 (SILICON)

Designers Data Sheet

HOT CARRIER POWER RECTIFIER

. . . employing the Schottky Barrier principle in a large area metal-to-silicon power diode. State of the art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high-frequency inverters, free wheeling diodes, and polarity protection diodes.

- Extremely Low v_F
- Low Stored Charge, Majority Carrier Conduction
- Low Power Loss/High Efficiency
- High Surge Capacity

Designer's Data for "Worst Case" Conditions

The Designers▲ Data sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

*MAXIMUM RATINGS

Rating	Symbol	1N5826	1N5827	1N5828	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	40	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	24	36	48	Volts
Average Rectified Forward Current $V_{R(equiv)} \leq 0.2\ V_{R(dc)}, T_C = 85^\circ C$	I_O	← 15 →			Amp
Ambient Temperature Rated $V_{R(dc)}, P_{F(AV)} = 0$, $R_{\theta JA} = 5.0^\circ C/W$	T_A	95	90	85	°C
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, halfwave, single phase, 60 Hz)	I_{FSM}	← 500 (for 1 cycle) →			Amp
Operating and Storage Junction Temperature Range (Reverse voltage applied)	T_J, T_{stg}	← -65 to +125 →			°C
Peak Operating Junction Temperature (Forward Current Applied)	$T_{J(pk)}$	← 150 →			°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ C$ unless otherwise noted.)

Characteristic	Symbol	1N5826	1N5827	1N5828	Unit
Maximum Instantaneous Forward Voltage (1)	v_F				Volts
(i_F = 8.0 Amp)		0.380	0.400	0.420	
(i_F = 15 Amp)		0.440	0.470	0.500	
(i_F = 47.1 Amp)		0.670	0.770	0.870	
Maximum Instantaneous Reverse Current @ rated dc Voltage (1)	i_R	10	10	10	mA
$T_C = 100^\circ C$		75	75	75	

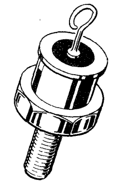
*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

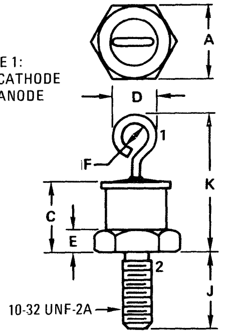
▲ Trademark of Motorola Inc.

SCHOTTKY BARRIER RECTIFIERS

15 AMPERE
20,30,40 VOLTS



STYLE 1:
1. CATHODE
2. ANODE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.77	11.10	0.424	0.437
C	–	10.29	–	0.405
D	–	6.35	–	0.250
E	1.91	4.45	0.075	0.175
F	1.52	–	0.060	–
J	10.72	11.51	0.422	0.453
K	–	20.32	–	0.800

CASE 245-01

MECHANICAL CHARACTERISTICS

CASE: Welded, hermetically sealed

FINISH: All external surfaces corrosion resistant and terminal lead is readily solderable.

POLARITY: Cathode to Case

MOUNTING POSITION: Any

STUD TORQUE: 15 in. lb. max

NOTE 1: DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 0.2 V_{RWM}. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} P_{F(AV)} - R_{\theta JA} P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest).

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figures 1, 2 and 3 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA} P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA} P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figures 1, 2 and 3 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1, 2 and 3 is based upon dc conditions. For use in common rectifier circuits, Table I indicates suggested factors for an equivalent dc voltage to use for conservative design; i.e.:

$$V_{R(equiv)} = V_{in(PK)} \times F \quad (4)$$

The Factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

Example: Find $T_{A(max)}$ for 1N5828 operated in a 12-Volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 10 A ($I_{F(AV)}$ = 5 A), $I_{(PK)}/I_{(AV)}$ = 20, Input Voltage = 10 V(rms), $R_{\theta JA}$ = 5°C/W.

Step 1: Find $V_{R(equiv)}$. Read F = 0.65 from Table I ∴ $V_{R(equiv)} = (1.41)(10)(0.65) = 9.18$ V

Step 2: Find T_R from Figure 3. Read T_R = 121°C @ V_R = 9.18 & $R_{\theta JA}$ = 5°C/W

Step 3: Find $P_{F(AV)}$ from Figure 4. †Read $P_{F(AV)}$ = 10 W @ $\frac{I_{(PK)}}{I_{(AV)}} = 20$ & $I_{F(AV)} = 5$ A

Step 4: Find $T_{A(max)}$ from equation (3). $T_{A(max)} = 121-(5)(10) = 71$°C

†Values given are for the 1N5828. Power is slightly lower for the other units because of their lower forward voltage.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped (1),(2)	
Load	Resistive	Capacitive (1)	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

(1) Note that $V_{R(PK)} \approx 2 V_{in(PK)}$

(2) Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE – 1N5826

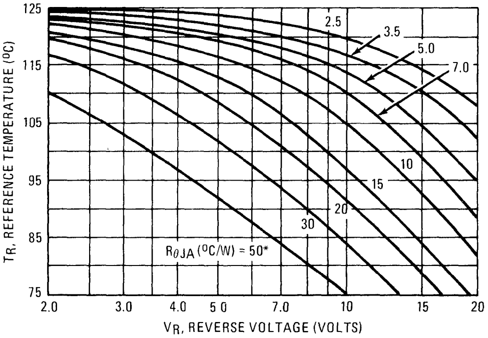


FIGURE 2 – MAXIMUM REFERENCE TEMPERATURE – 1N5827

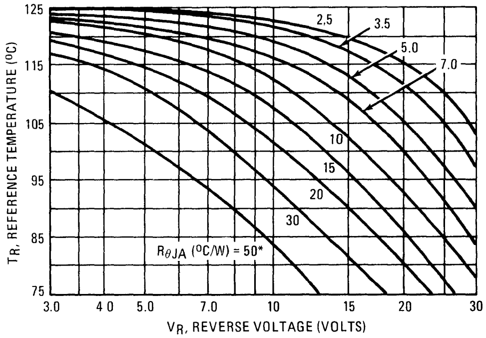


FIGURE 3 – MAXIMUM REFERENCE TEMPERATURE – 1N5828

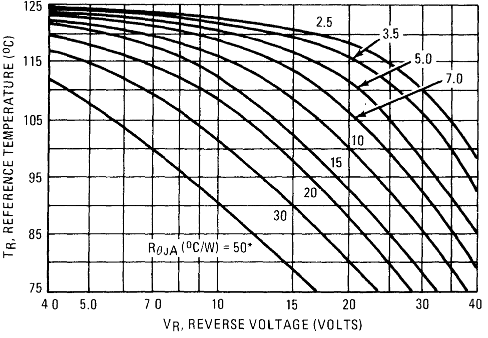


FIGURE 4 – FORWARD POWER DISSIPATION

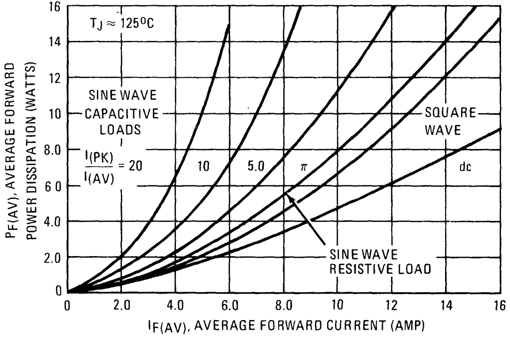


FIGURE 5 – TYPICAL FORWARD VOLTAGE

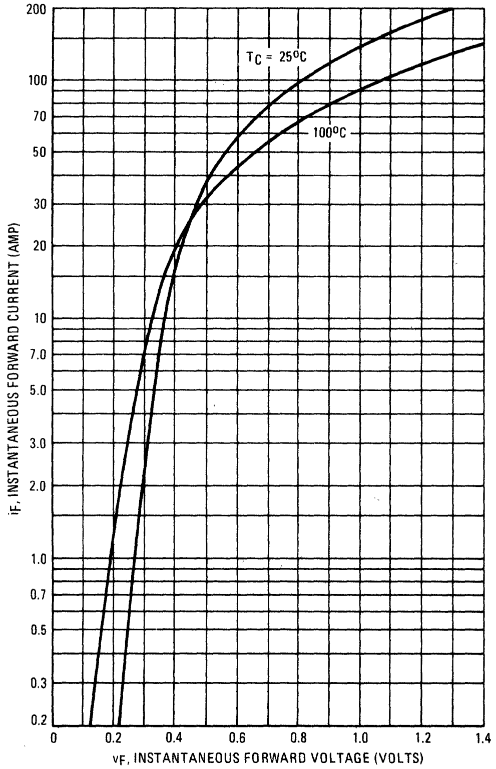
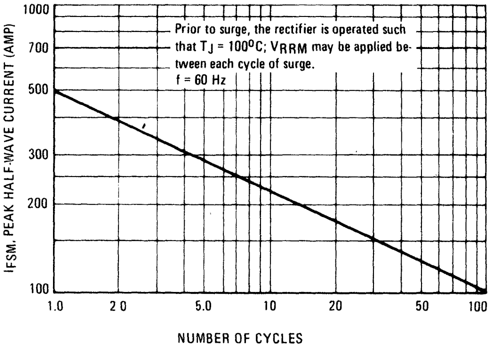
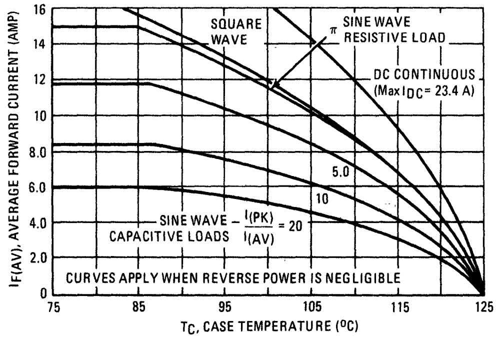


FIGURE 6 – MAXIMUM SURGE CAPABILITY



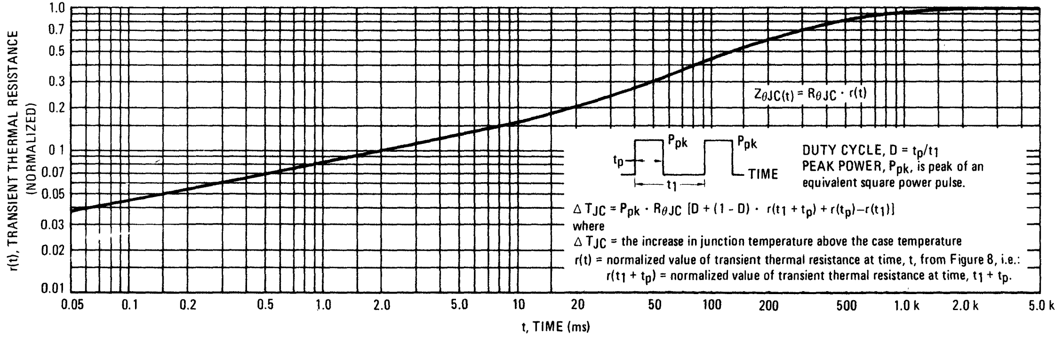
Prior to surge, the rectifier is operated such that $T_J = 100°C$; V_{RRM} may be applied between each cycle of surge.
f = 60 Hz

FIGURE 7 – CURRENT DERATING



CURVES APPLY WHEN REVERSE POWER IS NEGLIGIBLE

FIGURE 8 – THERMAL RESPONSE



$Z_{\theta JC}(t) = R_{\theta JC} \cdot r(t)$

DUTY CYCLE, $D = t_p/t_1$
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC}\ [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$

where

ΔT_{JC} = the increase in junction temperature above the case temperature

r(t) = normalized value of transient thermal resistance at time, t, from Figure 8, i.e.:
$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time, $t_1 + t_p$.

FIGURE 9 – NORMALIZED REVERSE CURRENT

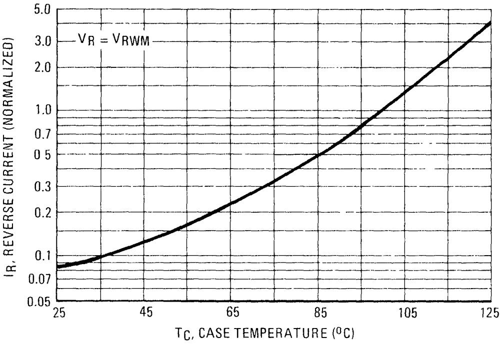


FIGURE 10 – TYPICAL REVERSE CURRENT

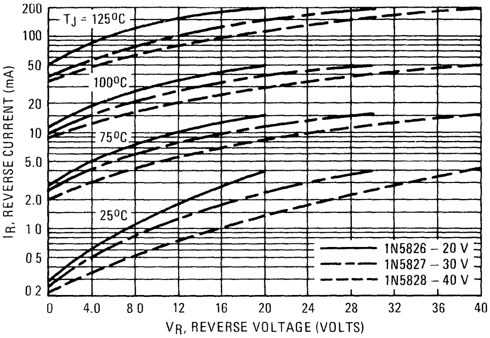
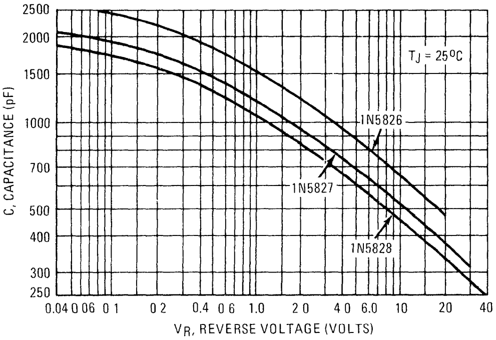


FIGURE 11 – CAPACITANCE



NOTE 2 – HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 11).

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, whereas perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss; it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

1N5829, 1N5830, 1N5831 (SILICON)

Designers Data Sheet

HOT CARRIER POWER RECTIFIER

. . . employing the Schottky Barrier principle in a large area metal-to-silicon power diode. State of the art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high-frequency inverters, free wheeling diodes, and polarity protection diodes.

- Extremely Low v_F
- Low Stored Charge, Majority Carrier Conduction
- Low Power Loss/High Efficiency
- High Surge Capacity

Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

***MAXIMUM RATINGS**

Rating	Symbol	1N5829	1N5830	1N5831	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	40	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	24	36	48	Volts
Average Rectified Forward Current $V_{R(equiv.)} \leqslant 0.2\ V_{R(dc)}, T_C = 85^oC$	I_O	← 25 →			Amp
Ambient Temperature Rated $V_{R(dc)}, P_{F(AV)} = 0$ $R_{\theta JA} = 3.5^oC/W$	T_A	90	85	80	^oC
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, halfwave, single phase, 60 Hz)	I_{FSM}	800 (for 1 cycle)			Amp
Operating and Storage Junction Temperature Range (Reverse voltage applied)	T_J, T_{stg}	← -65 to +125 →			^oC
Peak Operating Junction Temperature (Forward Current Applied)	$T_{J\ (pk)}$	← 150 →			^oC

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^oC/W$

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^oC$ unless otherwise noted)

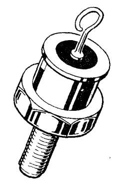
Characteristic	Symbol	1N5829	1N5830	1N5831	Unit
Maximum Instantaneous Forward Voltage(1) (i_F = 10 Amp) (i_F = 25 Amp) (i_F = 78.5 Amp)	v_F	 0.360 0.440 0.720	 0.370 0.460 0.770	 0.380 0.480 0.820	Volts
Maximum Instantaneous Reverse Current @Rated dc Voltage)(1) ($T_C = 100^oC$)	I_R	20 150	20 150	20 150	mA

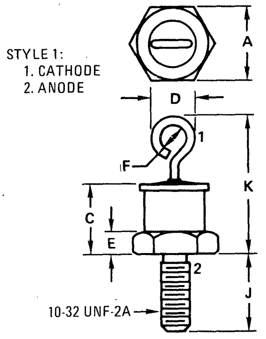
*Indicates JEDEC Registered Data

(1)Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%

SCHOTTKY BARRIER RECTIFIERS

25 AMPERE
20, 30, 40 VOLTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.77	11.10	0.424	0.437
C	–	10.29	–	0.405
D	–	6.35	–	0.250
E	1.91	4.45	0.075	0.175
F	1.52	–	0.060	–
J	10.72	11.51	0.422	0.453
K	–	20.32	–	0.800

CASE 245-01

MECHANICAL CHARACTERISTICS

CASE: Welded, hermetically sealed

FINISH: All external surfaces corrosion resistant and terminal lead is readily solderable.

POLARITY: Cathode to Case

MOUNTING POSITIONS: Any

STUD TORQUE: 15 in. lb. Max

NOTE 1: DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 0.2 V_{RWM}. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} P_{F(AV)} - R_{\theta JA} P_{R(AV)} \qquad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest).

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JC}$ = Junction-to-ambient thermal resistance

Figures 1, 2 and 3 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA} P_{R(AV)} \qquad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA} P_{F(AV)} \qquad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figures 1, 2 and 3 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1, 2 and 3 is based upon dc conditions. For use in common rectifier circuits, Table I indicates suggested factors for an equivalent dc voltage to use for conservative design; i.e.:

$$V_{R(equiv)} = V_{in(PK)} \times F \qquad (4)$$

The Factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

Example: Find $T_{A(max)}$ for 1N5831 operated in a 12-Volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 16 A ($I_{F(AV)}$ = 8 A), $I_{(PK)}/I_{(AV)}$ = 20, Input Voltage = 10 V(rms), $R_{\theta JA}$ = 5°C/W.

Step 1: Find $V_{R(equiv)}$. Read F = 0.65 from Table I ∴
$V_{R(equiv)} = (1.41)(10)(0.65) = 9.18$ V

Step 2: Find T_R from Figure 3. Read T_R = 113°C @ V_R = 9.18 & $R_{\theta JA}$ = 5°C/W

Step 3. Find $P_{F(AV)}$ from Figure 4. †Read $P_{F(AV)}$ = 12.8 W @ $\frac{I_{(PK)}}{I_{(AV)}} = 20$ & $I_{F(AV)}$ = 8 A

Step 4. Find $T_{A(max)}$ from equation (3). $T_{A(max)}$ = 113-(5)(12.8) = 49°C

†Values given are for the 1N5831. Power is slightly lower for the other units because of their lower forward voltage.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped (1),(2)	
Load	Resistive	Capacitive (1)	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

(1) Note that $V_{R(PK)} \approx 2 V_{in(PK)}$

(2) Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE – 1N5829

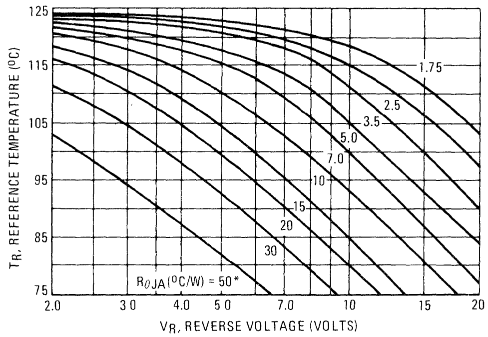


FIGURE 2 – MAXIMUM REFERENCE TEMPERATURE – 1N5830

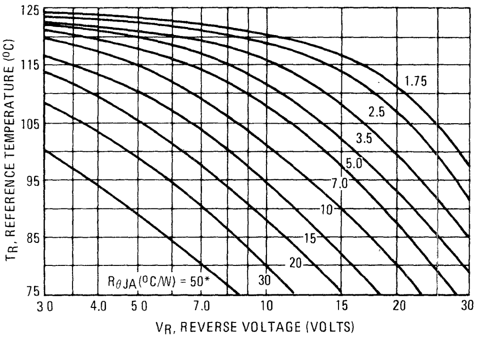
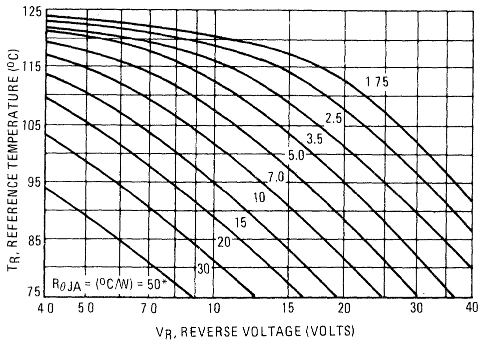


FIGURE 3 – MAXIMUM REFERENCE TEMPERATURE – 1N5831



*No external heat sink.

FIGURE 4 – FORWARD POWER DISSIPATION

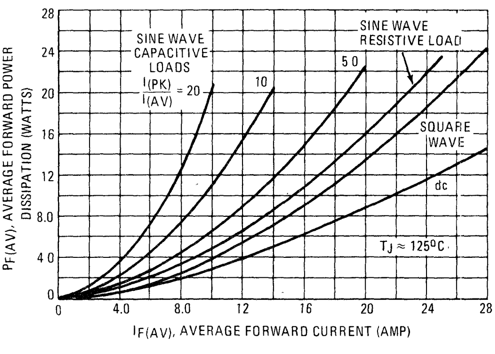


FIGURE 5 – TYPICAL FORWARD VOLTAGE

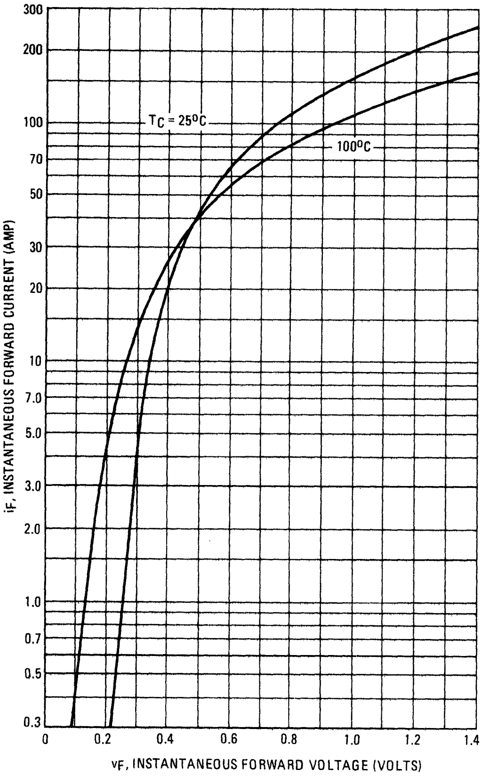
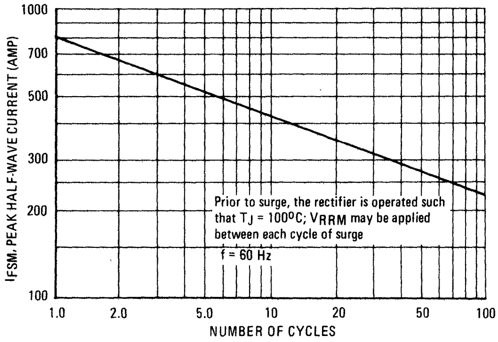


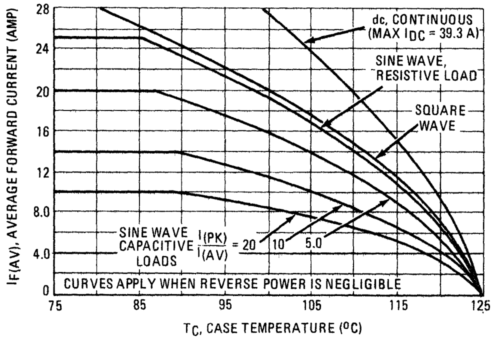
FIGURE 6 – MAXIMUM SURGE CAPABILITY



Prior to surge, the rectifier is operated such that $T_J = 100^{\circ}C$; V_{RRM} may be applied between each cycle of surge

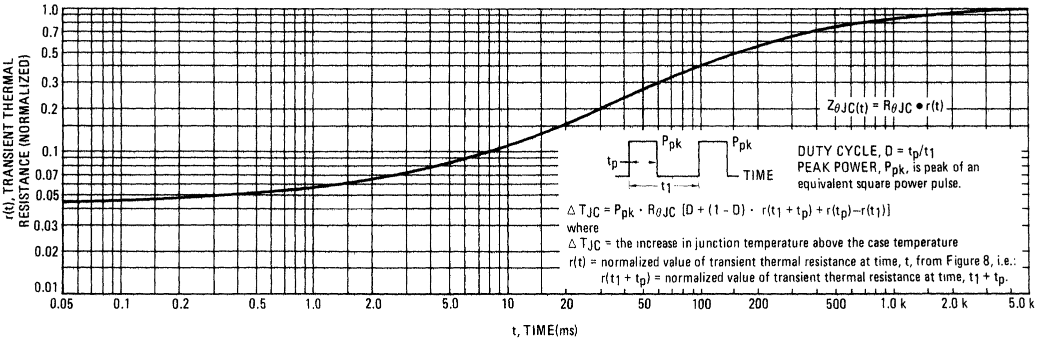
f = 60 Hz

FIGURE 7 – CURRENT DERATING



CURVES APPLY WHEN REVERSE POWER IS NEGLIGIBLE

FIGURE 8 – THERMAL RESPONSE



$Z_{\theta JC(t)} = R_{\theta JC} \bullet r(t)$

DUTY CYCLE, $D = t_p/t_1$

PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC} \, [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$

where

ΔT_{JC} = the increase in junction temperature above the case temperature

r(t) = normalized value of transient thermal resistance at time, t, from Figure 8, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time, $t_1 + t_p$.

FIGURE 9 – NORMALIZED REVERSE CURRENT

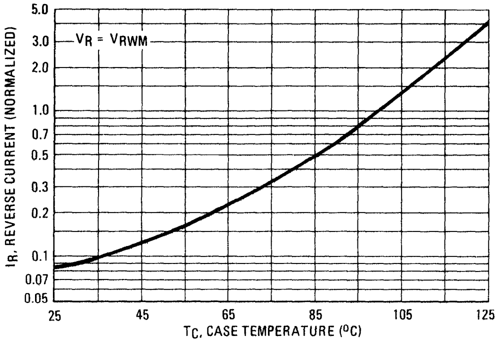


FIGURE 10 – TYPICAL REVERSE CURRENT

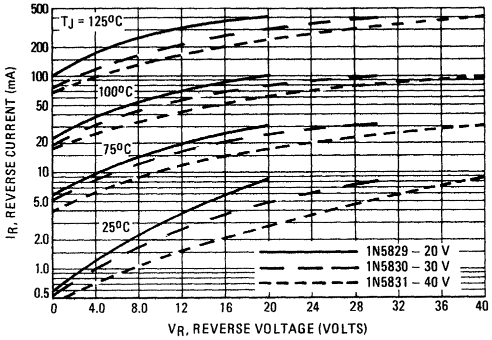
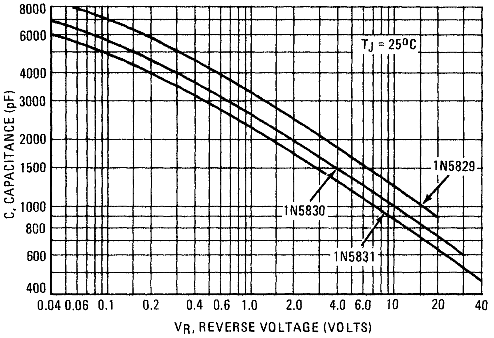


FIGURE 11 – CAPACITANCE



NOTE 2 – HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 11).

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, whereas perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss; it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

1N5832, 1N5833, 1N5834 (SILICON)

Designers Data Sheet

HOT CARRIER POWER RECTIFIER

. . . employing the Schottky Barrier principle in a large area metal-to-silicon power diode. State of the art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high-frequency inverters, free wheeling diodes, and polarity protection diodes

- Extremely Low v_F
- Low Stored Charge, Majority Carrier Conduction
- Low Power Loss/High Efficiency
- High Surge Capacity

Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

*MAXIMUM RATINGS

Rating	Symbol	1N5832	1N5833	1N5834	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	40	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	24	36	48	Volts
Average Rectified Forward Current $V_{R(equiv)} \le 0.2\ V_{R(dc)}, T_C = 75^oC$	I_O	← 40 →			Amp
Ambient Temperature Rated $V_{R(dc)}, P_{F(AV)} = 0$, $R_{\theta JA} = 2.0^oC/W$	T_A	100	95	90	^oC
Non-Repetitive Peak Surge Current (surge applied at rated load conditions halfwave, single phase, 60 Hz)	I_{FSM}	← 800 (for 1 cycle) →			Amp
Operating and Storage Junction Temperature Range (Reverse voltage applied)	T_J, T_{stg}	← -65 to +125 →			^oC
Peak Operating Junction Temperature (Forward Current Applied)	$T_{J(pk)}$	← 150 →			^oC

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

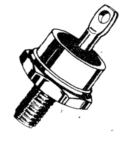
Characteristic	Symbol	1N5832	1N5833	1N5834	Unit
Maximum Instantaneous Forward Voltage (1)	v_F				Volts
(i_F = 10 Amp)		0.360	0.370	0.380	
(i_F = 40 Amp)		0.520	0.550	0.590	
(i_F = 125 Amp)		0.980	1.080	1.180	
Maximum Instantaneous Reverse Current @ rated dc Voltage (1)	i_R	20	20	20	mA
$T_C = 100^oC$		150	150	150	

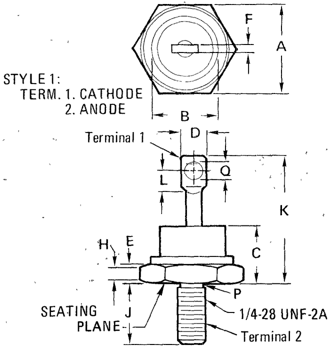
*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

SCHOTTKY BARRIER RECTIFIERS

40 AMPERE
20,30,40 VOLTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.94	17.45	0.667	0.687
B	–	16.94	–	0.667
C	–	11.43	–	0.450
D	–	9.53	–	0.375
E	2.92	5.08	0.115	0.200
F	–	2.03	–	0.080
H	1.52	–	0.060	–
J	10.72	11.51	0.422	0.453
K	–	25.40	–	1.000
L	3.86	–	0.152	–
P	5.59	6.32	0.220	0.249
Q	3.56	4.45	0.140	0.175

NOTES:
1. Dimension "P" is diameter.
2. All JEDEC dimensions and notes apply.

CASE 257-01
DO-203AB

MECHANICAL CHARACTERISTICS

CASE: Welded, hermetically sealed

FINISH: All external surfaces corrosion resistant and terminal lead is readily solderable.

POLARITY: Cathode to Case

MOUNTING POSITION: Any

STUD TORQUE: 25 in. lb. Max

NOTE 1: DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 0.2 V_{RWM}. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} P_{F(AV)} - R_{\theta JA} P_{R(AV)} \qquad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest).

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JC}$ = Junction-to-ambient thermal resistance

Figures 1, 2 and 3 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA} P_{R(AV)} \qquad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA} P_{F(AV)} \qquad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figures 1, 2 and 3 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1, 2 and 3 is based upon dc conditions. For use in common rectifier circuits, Table I indicates suggested factors for an equivalent dc voltage to use for conservative design; i.e.:

$$V_{R(equiv)} = V_{in(PK)} \times F \qquad (4)$$

The Factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

Example: Find $T_{A(max)}$ for 1N5834 operated in a 12-Volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 30 A ($I_{F(AV)}$ = 15 A), $I_{(PK)}/I_{(AV)}$ = 10, Input Voltage = 10 V(rms), $R_{\theta JA}$ = 3°C/W.

Step 1: Find $V_{R(equiv)}$. Read F = 0.65 from Table I ∴
$V_{R(equiv)}$ = (10)(1.41)(0.65) = 9.18 V

Step 2: Find T_R from Figure 3. Read T_R = 118°C @ V_R = 9.18 V & $R_{\theta JA}$ = 3°C/W

Step 3: Find $P_{F(AV)}$ from Figure 4.†Read $P_{F(AV)}$ = 20 W
@ $\frac{I_{(PK)}}{I_{(AV)}}$ = 10 & $I_{F(AV)}$ = 15 A

Step 4: Find $T_{A(max)}$ from equation (3). $T_{A(max)}$ = 118-(3)(20) = 58°C

†Values given are for the 1N5834. Power is slightly lower for the other units because of their lower forward voltage.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped (1),(2)	
Load	Resistive	Capacitive (1)	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

(1) Note that $V_{R(PK)} \approx 2\, V_{in(PK)}$

(2) Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE – 1N5832

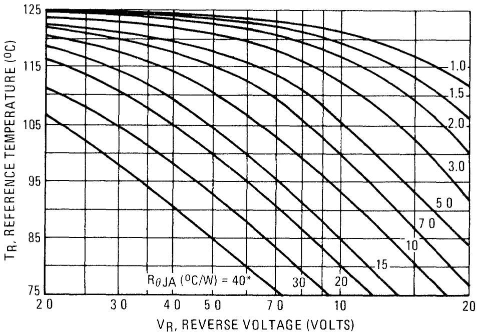


FIGURE 2 – MAXIMUM REFERENCE TEMPERATURE – 1N5833

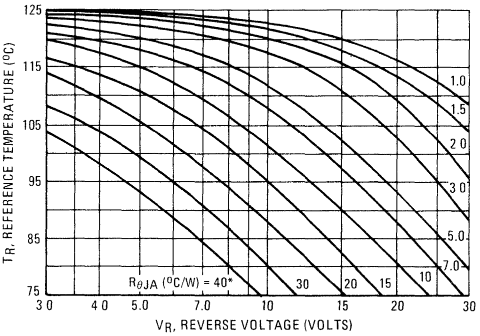


FIGURE 3 – MAXIMUM REFERENCE TEMPERATURE – 1N5834

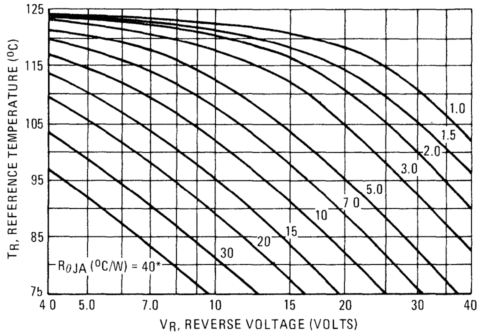
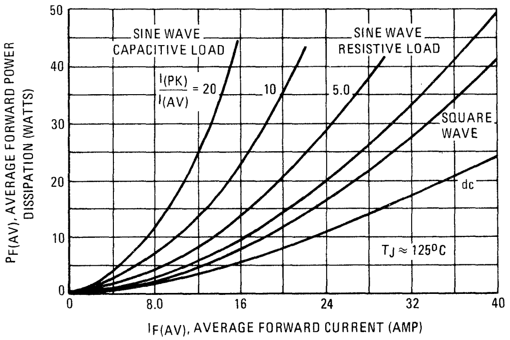


FIGURE 4 – FORWARD POWER DISSIPATION



*No external heat sink.

FIGURE 5 – TYPICAL FORWARD VOLTAGE

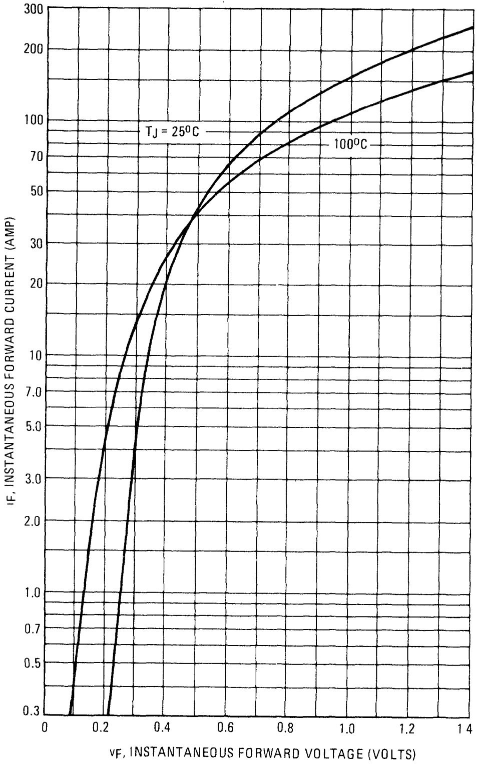


FIGURE 6 – MAXIMUM SURGE CAPABILITY

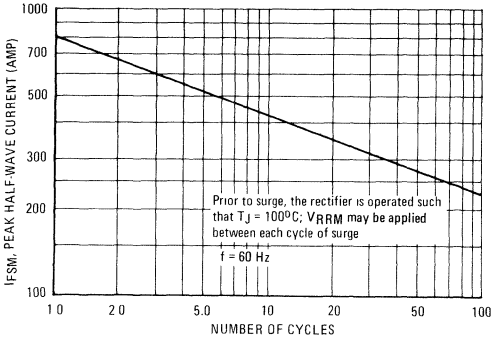


FIGURE 7 – CURRENT DERATING

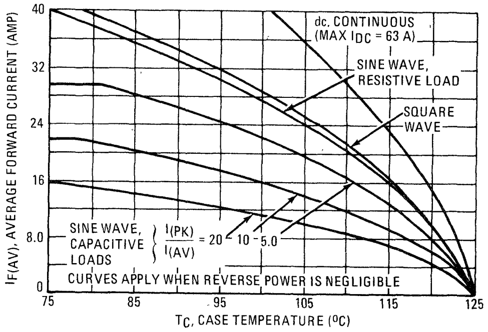
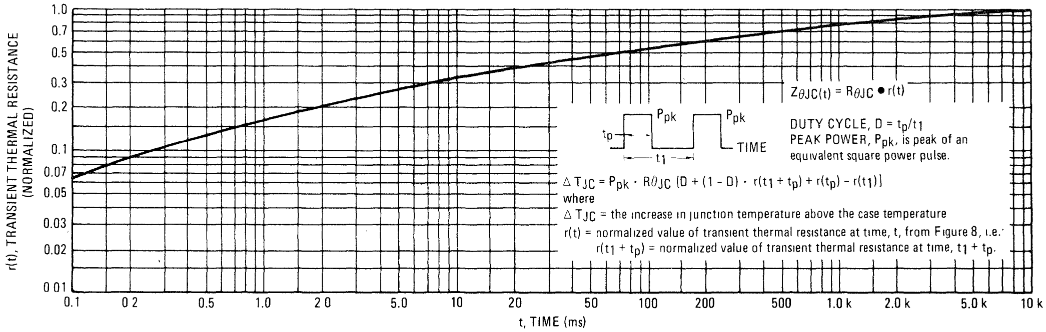


FIGURE 8 – THERMAL RESPONSE



$Z_{\theta JC}(t) = R_{\theta JC} \bullet r(t)$

DUTY CYCLE, $D = t_p/t_1$

PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC} [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$

where

ΔT_{JC} = the increase in junction temperature above the case temperature

$r(t)$ = normalized value of transient thermal resistance at time, t, from Figure 8, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time, $t_1 + t_p$.

FIGURE 9 – NORMALIZED REVERSE CURRENT

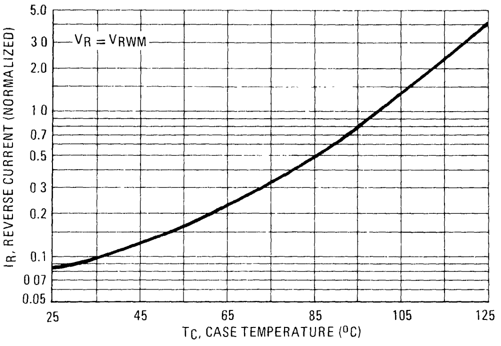


FIGURE 10 – TYPICAL REVERSE CURRENT

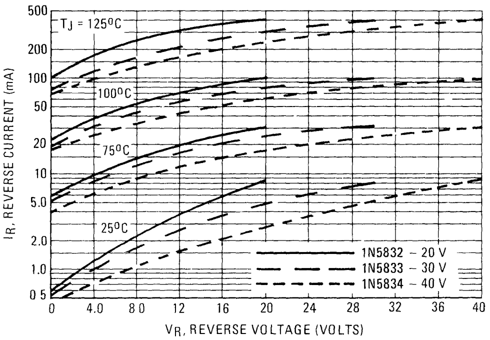
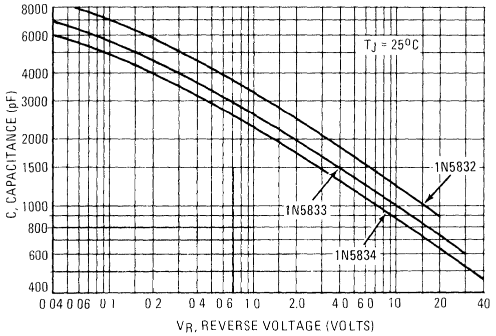


FIGURE 11 – CAPACITANCE



NOTE 2 HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 11).

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, whereas perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss; it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

1N5837A
thru
1N5897A

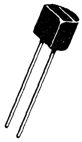
500 mW UNIBLOC SILICON OXIDE-PASSIVATED ZENER REGULATOR DIODES

Highly reliable silicon regulators utilizing an oxide-passivated junction for long-term voltage stability. Supplied in the popular TO-92 plastic package for the high volume requirements of the consumer industry.

- In-Line Leads for Easy Insertion
- Lower Cost in High Volume
- Electrically Similar to the Popular Surmetic 20 Series "1N5221 – 1N5281"
- Wide Voltage Selection – 2.4-200 V

UNIBLOC
ZENER REGULATOR DIODES

500 MILLIWATTS
2.4 thru 200 VOLTS



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Power Dissipation @ T_L = 55°C Lead Length = 1/4" Derate above 55°C (Figure 1)	P_D	500 5.26	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

*Indicates JEDEC Registered Data.

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded, thermosetting plastic

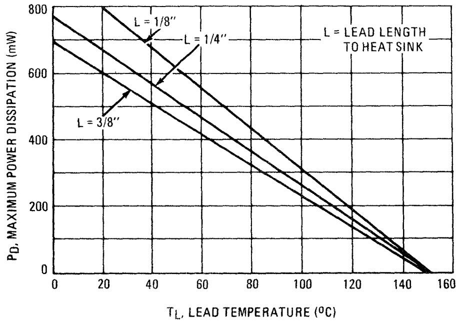
FINISH: All external surfaces are corrosion resistant. Leads are readily solderable and weldable

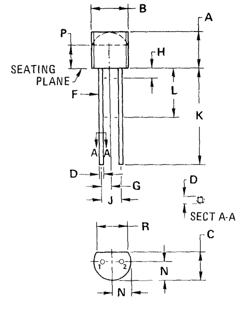
POLARITY: Cathode indicated by color dot. (When operated in zener mode, cathode will be positive with respect to anode.)

MOUNTING POSITION: Any

WEIGHT: 0.18 gram (approx)

FIGURE 1 – POWER-DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

CASE 182-02

ELECTRICAL CHARACTERISTICS Guaranteed when measured at 90 seconds while maintaining the lead temperature $T_L = 30 \pm 1^oC$, 3/8" from the diode body (V_F = 1.5 Volts Max at I_F = 200 mAdc for all types.)

Motorola Type Number (Note 1)	Nominal Zener Voltage* V_Z @ I_{ZT} Volts (Note 2)	Test Current* I_{ZT} mA	Max. Zener Impedance *		Max. Reverse * Leakage Current		Maximum DC Zener Current I_{ZM}* mAdc	Maximum Surge Current $I_{Z(surge)}$* mAdc (Note 4)	Typical Zener Voltage Temp. Coeff. θ_{VZ} (%/°C) (Note 3)
			Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} @ I_{ZK} = 0.25 mA Ohms	I_R µA	at V_R volts			
1N5837A	2.4	20	50	2100	100	1.0	210	1041.7	-1.03
1N5838A	2.5	20	50	2100	100	1.0	200	1000.0	-1.03
1N5839A	2.7	20	50	2200	75	1.0	185	925.9	-1.01
1N5840A	2.8	20	50	2200	75	1.0	179	892.9	-1.00
1N5841A	3.0	20	50	2300	50	1.0	167	833.3	-0.09
1N5842A	3.3	20	50	2500	25	1.0	151	757.6	-0.068
1N5843A	3.6	20	48	2700	15	1.0	139	694.4	-0.051
1N5844A	3.9	20	40	2800	10	1.0	129	641.0	-0.034
1N5845A	4.3	20	25	2900	5.0	1.0	116	581.4	-0.010
1N5846A	4.7	20	19	2600	5.0	2.0	106	531.9	+0.012
1N5847A	5.1	20	17	2400	5.0	2.0	98	490.2	+0.025
1N5848A	5.6	20	15	2100	5.0	3.0	89	446.4	+0.035
1N5849A	6.0	20	13	1900	5.0	3.5	83	416.7	+0.041
1N5850A	6.2	20	14	1500	5.0	4.0	80	403.2	+0.043
1N5851A	6.8	20	17	780	3.0	5.0	74	367.6	+0.050
1N5852A	7.5	20	23	700	3.0	6.0	67	333.3	+0.055
1N5853A	8.2	20	34	700	3.0	6.5	61	304.9	+0.059
1N5854A	8.7	20	44	700	3.0	6.5	57	287.4	+0.061
1N5855A	9.1	20	50	700	3.0	7.0	55	274.7	+0.062
1N5856A	10	20	62	700	3.0	8.0	50	250.0	+0.066
1N5857A	11	20	68	700	2.0	8.4	45	227.3	+0.068
1N5858A	12	20	70	700	1.0	9.1	41.5	208.3	+0.070
1N5859A	13	9.5	70	700	0.5	9.9	38.5	538.5	+0.072
1N5860A	14	9.0	70	700	0.1	10	35.5	500.0	+0.074
1N5861A	15	8.5	34	700	0.1	11	33	466.7	+0.076
1N5862A	16	7.8	38	700	0.1	12	31	437.5	+0.077
1N5863A	17	7.4	42	700	0.1	13	29	411.8	+0.078
1N5864A	18	7.0	48	700	0.1	14	28	388.9	+0.079
1N5865A	19	6.6	52	700	0.1	14	26	368.4	+0.080
1N5866A	20	6.2	57	700	0.1	15	25	350.0	+0.080
1N5867A	22	5.6	68	700	0.1	17	22.6	318.2	+0.082
1N5868A	24	5.2	78	700	0.1	18	21.7	291.7	+0.083
1N5869A	25	5.0	85	700	0.1	19	20	280.0	+0.083
1N5870A	27	4.6	98	700	0.1	21	18.5	259.3	+0.084
1N5871A	28	4.5	105	700	0.1	21	17.9	250.0	+0.084
1N5872A	30	4.2	117	700	0.1	23	16.7	233.3	+0.085
1N5873A	33	3.8	140	700	0.1	25	15.1	212.1	+0.086
1N5874A	36	3.4	160	700	0.1	27	13.9	194.4	+0.087
1N5875A	39	3.2	190	800	0.1	30	12.9	179.5	+0.087
1N5876A	43	3.0	225	900	0.1	33	11.6	162.8	+0.088
1N5877A	47	2.7	260	1000	0.1	36	10.6	148.9	+0.088
1N5878A	51	2.5	300	1100	0.1	39	9.8	137.3	+0.089
1N5879A	56	2.2	360	1300	0.1	43	8.9	125.0	+0.089
1N5880A	60	2.1	410	1500	0.1	46	8.3	116.7	+0.090
1N5881A	62	2.0	430	1600	0.1	47	8.0	112.9	+0.090
1N5882A	68	1.8	520	1900	0.1	52	7.4	102.9	+0.090
1N5883A	75	1.7	600	2300	0.1	56	6.7	93.3	+0.090
1N5884A	82	1.5	700	2700	0.1	62	6.1	85.4	+0.090
1N5885A	87	1.4	780	3100	0.1	68	5.7	80.5	+0.091
1N5886A	91	1.4	840	3400	0.1	69	5.5	76.9	+0.091
1N5887A	100	1.3	1000	4000	0.1	76	5.0	50.0	+0.091
1N5888A	110	1.1	1200	5000	0.1	84	4.5	45.5	+0.091
1N5889A	120	1.0	1400	5100	0.1	91	4.1	41.7	+0.092
1N5890A	130	0.95	1600	5200	0.1	99	3.8	38.5	+0.092
1N5891A	140	0.90	1800	5300	0.1	106	3.5	35.7	+0.092
1N5892A	150	0.85	2100	5400	0.1	114	3.3	33.3	+0.092
1N5893A	160	0.80	2300	5500	0.1	122	3.1	31.2	+0.092
1N5894A	170	0.74	2600	5600	0.1	129	2.9	29.4	+0.092
1N5895A	180	0.68	2900	6000	0.1	137	2.8	27.8	+0.092
1N5896A	190	0.66	3200	6500	0.1	144	2.6	26.3	+0.093
1N5897A	200	0.65	3500	7000	0.1	152	2.5	25.0	+0.093

*Indicates JEDEC Registered Data.

NOTE 1 – TOLERANCE AND VOLTAGE DESIGNATION

Tolerance designation – The type numbers listed indicate a tolerance of ±10%. Device tolerances of ±5% are indicated by a "B" suffix; ±2% by a "C" suffix, ±1% by a "D" suffix. ±20% tolerance should be designated as below with no suffix.

Non-Standard voltage designation – To designate units with zener voltages other than those assigned the Motorola type number should be used.

EXAMPLE:

M	Z	92	–	65	A
Motorola	Zener Diode	Series		Nominal Voltage	Tolerance (±%)

NOTE 2 – SPECIAL SELECTIONS AVAILABLE INCLUDE:

(a) Nominal zener voltages between those shown.

(b) Matched sets: (Standard Tolerances are ±5.0%, ±2.0%, ±1.0%)

- a. Two or more units for series connection with specified tolerance on total voltage. Series matched sets make zener voltages in excess of 200 volts possible as well as providing lower temperature coefficients, lower dynamic impedance and greater power handling ability.
- b. Two or more units matched to one another with any specified tolerance.

NOTE 3 – TYPICAL TEMPERATURE COEFFICIENT (θ_{VZ})

Test conditions for temperature coefficient are as follows:

a. I_{ZT} = 7.5 mA, T_1 = 25°C
T_2 = 125°C (MZ92-2,4A,B thru MZ92-12A,B).

b. I_{ZT} = Rated I_{ZT}, T_1 = 25°C
T_2 = 125°C (MZ92-13A,B thru MZ92-200A,B)

Device to be temperature stabilized with current applied prior to reading breakdown voltage at the specified ambient temperature.

NOTE 4 – $I_{Z(surge)}$ NON-REPETITIVE

The rating listed in the electrical characteristics table is maximum peak, non-repetitive, reverse surge current of 1/2 square wave or equivalent sine wave pulse of 1/120 second duration superimposed on the test current, I_{ZT}, per JEDEC registration.

1N5909

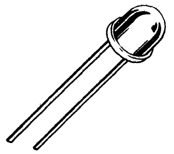
(Formerly MLED455)

VISIBLE RED LIGHT-EMITTING DIODE

. . . designed for panel mount applications where small size and plug-in package are desirable.

- JEDEC Registered for Guaranteed Mechanical and Electrical Conformity
- High Luminous Intensity
- Economical Plastic Package
- Solid-State Reliability
- Red Diffusing Lens
- IC Compatible – Low Power Consumption
- Wide Viewing Angle – 75°

MINIATURE
LIGHT EMITTING DIODE
VISIBLE RED
PN GALLIUM
ARSENIDE PHOSPHIDE



MAXIMUM RATINGS

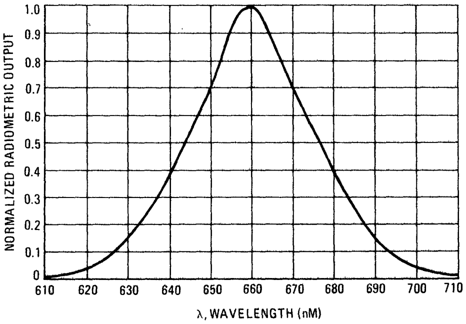
Rating	Symbol	Value	Unit
Reverse Voltage	V_R	4.0	Volts
*Forward Current – T_A = 25°C	I_F	35	mA
*Peak Pulse Current (Pulse Width = 1.0 μs, f = 10 kHz)	i_F	1000	mA
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	75 1.0	mW mW/°C
*Operating and Storage Temperature Range	T_A,T_{stg}	-40 to +100	°C

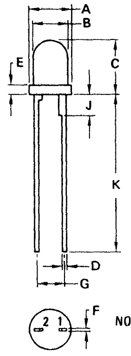
*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Soldering Temperature 1/16" from Case for 10 seconds	–	240	°C

*Indicates JEDEC Registered Data.

FIGURE 1 – NORMALIZED RADIOMETRIC OUTPUT versus WAVELENGTH





NOTE:
1. CATHODE
2. ANODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.68	3.94	0.145	0.155
B	2.92	3.18	0.115	0.125
C	4.95	5.21	0.195	0.205
D	0.38	0.48	0.015	0.019
E	0.76	1.02	0.030	0.040
F	0.20	0.30	0.008	0.012
G	2.41	2.67	0.095	0.105
J	1.78	2.03	0.070	0.080
K	12.70	–	0.500	–

CASE 292-01

1N5909 (continued)

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 100 μA)	–	BV_R	4.0	–	–	Volts
Forward Voltage (I_F = 20 mA)	2	V_F	–	1.6	2.0	Volts

OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted).

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
*Axial Luminous Intensity(1) (IF = 20 mA)	3,4,5	I_o	0.3	1.2	–	mcd
Effective Luminous Area	–	–	–	0.01	–	Square-Inch Circle
Peak Emission Wavelength	–	λp	–	660	–	nM
Spectral Line Half Width	–	$\Delta\lambda$	–	30	–	nM

(1) Axial Luminous Intensity (I_o) is measured using an International Commission on Illumination corrected Photometer and a measurement solid angle of 0.003 Steradian.

* Indicates JEDEC Registered Data.

TYPICAL CHARACTERISTICS

FIGURE 2 – FORWARD CHARACTERISTICS

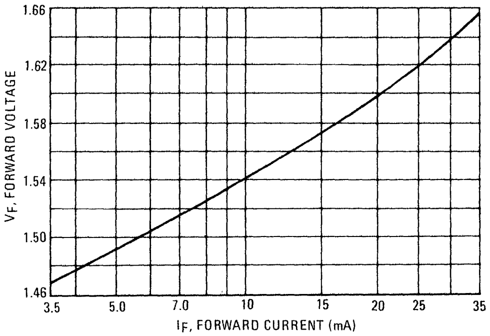


FIGURE 3 – AXIAL LUMINOUS INTENSITY versus JUNCTION TEMPERATURE

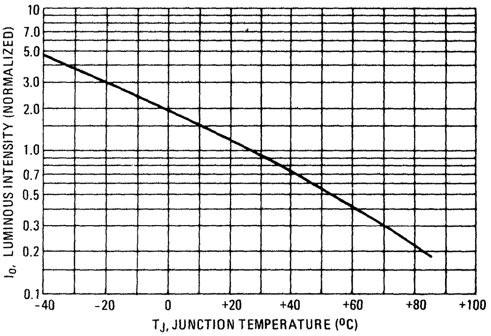


FIGURE 4 – AXIAL LUMINOUS INTENSITY versus FORWARD CURRENT

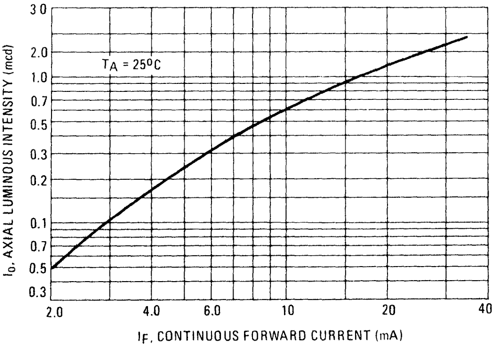
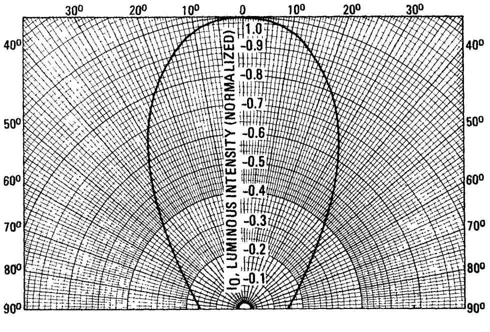


FIGURE 5 – SPATIAL RADIATION PATTERN



1N5910

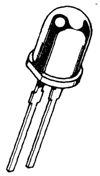
(Formerly MLED650)

VISIBLE RED LIGHT-EMITTING DIODE

. . . ideally suited for panel mount indicator applications in panels up to 0.125 inches thick.

- JEDEC Registered for Guaranteed Mechanical and Electrical Conformity
- High Luminous Intensity
- Economical Plastic Package
- Solid State Reliability
- Wide Viewing Angle
- Red Diffusing Lens

PANEL MOUNT
LIGHT EMITTING DIODE
VISIBLE RED
PN GALLIUM
ARSENIDE PHOSPHIDE



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	4.0	Volts
*Forward Current — $T_A = 25^\circ C$	I_F	60	mA
*Peak Pulse Current (Pulse Width = 1.0 µs, f = 10 kHz)	i_F	1000	mA
*Total Power Dissipation @ $T_A = 25^\circ C$ Derate above 25°C	P_D(1)	125 1.67	mW mW/°C
*Operating and Storage Temperature Range	T_A, T_{stg}	-40 to +100	°C

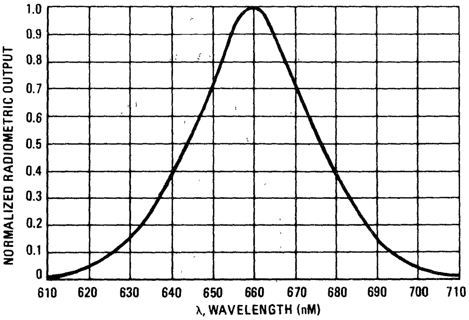
THERMAL CHARACTERISTICS

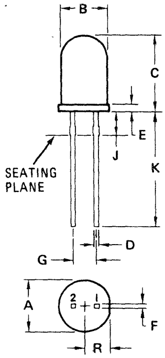
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	600	°C/W
*Soldering Temperature — 1/16″ From Case for 10 Seconds	—	240	°C

(1) Mounted in metal panel

*Indicates JEDEC Registered Data.

FIGURE 1 — NORMALIZED RADIOMETRIC OUTPUT versus WAVELENGTH





STYLE 1.
PIN 1. CATHODE
2 ANODE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.72	5.97	0.225	0.235
B	4.95	5.21	0.195	0.205
C	8.38	8.89	0.330	0.350
D	0.41	0.51	0.016	0.020
E	0.64	0.89	0.025	0.035
F	0.30	0.46	0.012	0.018
G	2.44	2.64	0.096	0.104
J	2.44	2.54	0.096	0.100
K	12.57	13.21	0.495	0.520
R	2.54	2.79	0.100	0.110

CASE 279-01

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 100 μA)	–	BV_R	4.0	–	–	Volts
Forward Voltage (I_F = 20 mA)	2	V_F	–	1.6	2.0	Volts

OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Fig. No.	Symbol	Min	Typ	Max	Unit
Axial Luminous Intensity (1)	3,4	I_o				mcd
*(I_F = 20 mA)			0.3	0.8	–	
(IF = 50 mA)			–	1.4	–	
Effective Luminous Area	–	–	–	0.03		Square-Inch Circle
Peak Emission Wavelength	–	λp	–	660	–	nM
Spectral Line Half Width	–	Δλ	–	30	–	nM

(1) Axial Luminous Intensity (I_o) is measured using an International Commission on Illumination corrected Photometer and a measurement solid angle of 0.003 Steradian.

*Indicates JEDEC Registered Data.

TYPICAL CHARACTERISTICS

FIGURE 2 – FORWARD CHARACTERISTICS

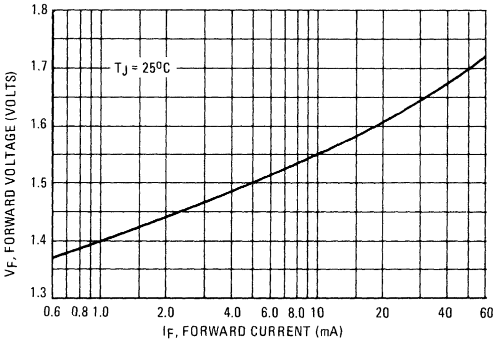


FIGURE 3 – AXIAL LUMINOUS INTENSITY versus JUNCTION TEMPERATURE

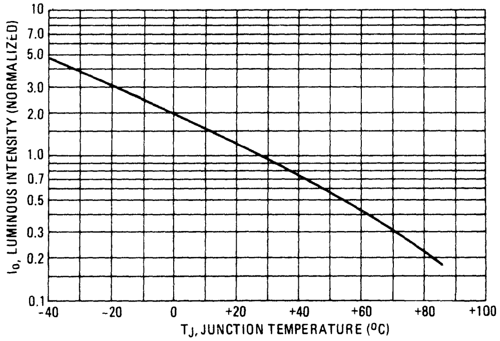


FIGURE 4 – AXIAL LUMINOUS INTENSITY versus CONTINUOUS FORWARD CURRENT

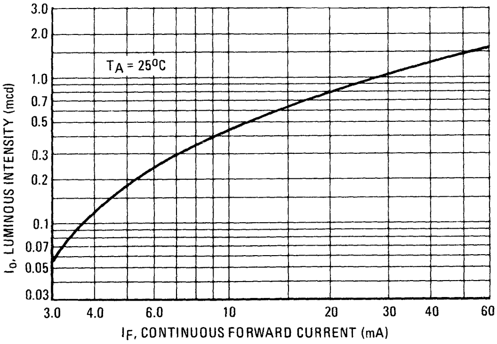
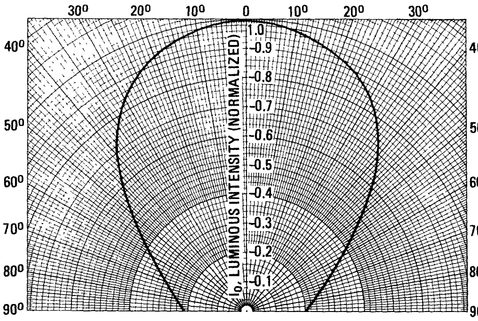


FIGURE 5 – SPATIAL RADIATION PATTERN



1N5911
(Formerly MLED750)

VISIBLE GREEN LIGHT-EMITTING DIODE

. . . ideally suited for panel mount indicator applications in panels up to 0.125 inches thick.

- JEDEC Registered for Guaranteed Mechanical and Electrical Conformity.
- High Luminous Intensity
- Economical Plastic Package
- Solid State Reliability
- Wide Viewing Angle – 90°
- Green Diffusing Lens

MAXIMUM RATINGS

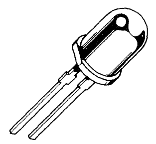
Rating	Symbol	Value	Unit
Reverse Voltage	V_R	4.0	Volts
*Forward Current – $T_A = 25^oC$	I_F	35	mA
*Peak Pulse Current (Pulse Width = 1.0 μs, f = 10 kHz)	i_F	1000	mA
*Total Power Dissipation @ $T_A = 25^oC$ Derate above 25°C	P_D(1)	125 1.67	mW mW/°C
*Operating and Storage Temperature Range	T_A, T_{stg}	-40 to +100	°C

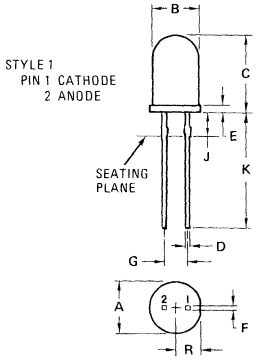
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	600	°C/W
*Soldering Temperature – 1/16" from Case for 10 Seconds	–	240	°C

(1) Mounted in metal panel
*Indicates JEDEC Registered Data.

PANEL MOUNT
LIGHT EMITTING DIODE
VISIBLE GREEN
PN GALLIUM PHOSPHIDE

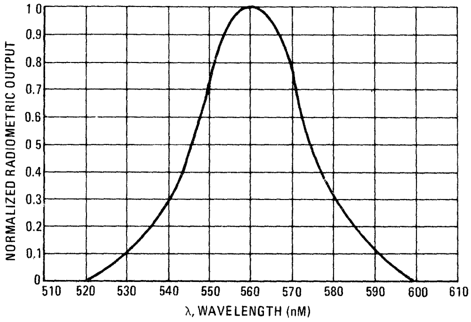




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.72	5.97	0.225	0.235
B	4.95	5.21	0.195	0.205
C	8.38	8.89	0.330	0.350
D	0.41	0.51	0.016	0.020
E	0.64	0.89	0.025	0.035
F	0.30	0.46	0.012	0.018
G	2.44	2.64	0.096	0.104
J	2.44	2.54	0.096	0.100
K	12.57	13.21	0.495	0.520
R	2.54	2.79	0.100	0.110

CASE 279-01

FIGURE 1 – NORMALIZED RADIOMETRIC OUTPUT versus WAVELENGTH



***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic	Figure No.	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 100 μA)	–	BV_R	4.0	–	–	Volts
Forward Voltage (I_F = 25 mA)	2	V_F	–	2.1	3.0	Volts

OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Figure No.	Symbol	Min	Typ	Max	Unit
*Axial Luminous Intensity (1) (I_F = 25 mA)	3,4,5	I_o	0.3	0.5	–	mcd
Effective Luminous Area	–	–	–	0.03	–	Square-Inch Circle
Peak Emission Wavelength	–	λp	–	560	–	nM
Spectral Line Half Width	–	Δλ	–	30	–	nM

*Indicates JEDEC Registered Data.

(1) Axial Luminous Intensity (I_o) is measured using an International Commission on Illumination corrected Photometer and a measurement solid angle of 0.003 Steradian.

TYPICAL CHARACTERISTICS

FIGURE 2 – FORWARD CHARACTERISTICS

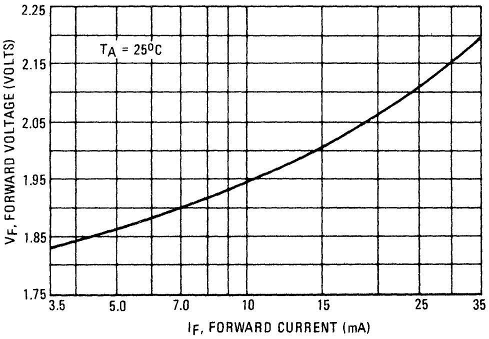


FIGURE 3 – AXIAL LUMINOUS INTENSITY versus JUNCTION TEMPERATURE

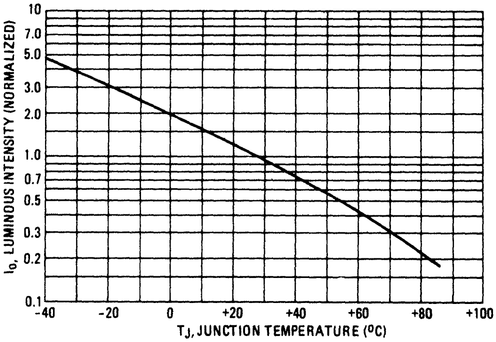


FIGURE 4 – AXIAL LUMINOUS INTENSITY versus FORWARD CURRENT

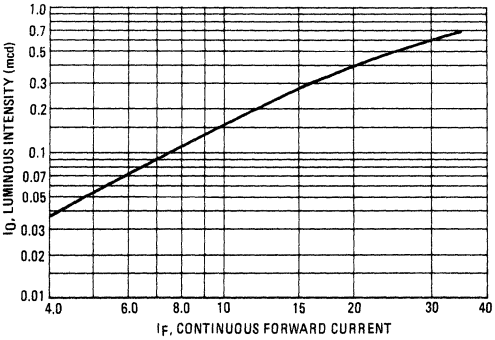
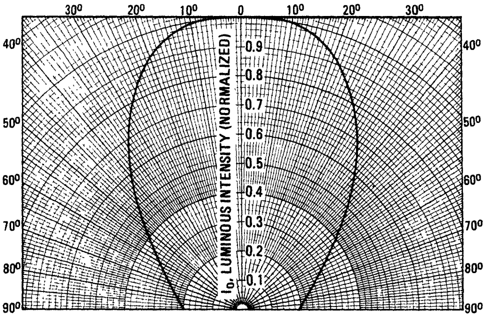


FIGURE 5 – SPATIAL RADIATION PATTERN



1N5912

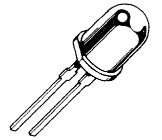
(Formerly MLED850)

VISIBLE YELLOW LIGHT-EMITTING DIODE

. . . ideally suited for panel mount indicator applications in panels up to 0.125 inches thick.

- JEDEC Registered for Guaranteed Mechanical and Electrical Conformity.
- High Luminous Intensity
- Economical Plastic Package
- Solid State Reliability
- Wide Viewing Angle – 90°
- Yellow Diffusing Lens

PANEL MOUNT
LIGHT EMITTING DIODE
VISIBLE YELLOW
PN GALLIUM PHOSPHIDE



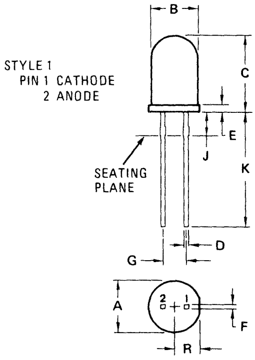
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	4.0	Volts
*Forward Current – T_A = 25°C	I_F	35	mA
*Peak Pulse Current (Pulse Width = 1.0 μs, f = 10 kHz)	i_F	1000	mA
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D(1)	125 1.67	mW mW/°C
*Operating and Storage Junction Temperature Range	T_A, T_{stg}	-40 to +100	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	600	°C/W
*Soldering Temperature – 1/16" from Case for 10 Seconds	–	240	°C

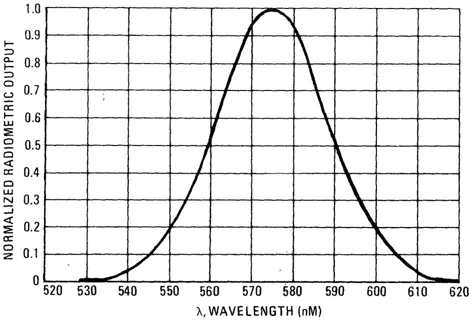
(1) Mounted in metal panel
*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.72	5.97	0.225	0.235
B	4.95	5.21	0.195	0.205
C	8.38	8.89	0.330	0.350
D	0.41	0.51	0.016	0.020
E	0.64	0.89	0.025	0.035
F	0.30	0.46	0.012	0.018
G	2.44	2.64	0.096	0.104
J	2.44	2.54	0.096	0.100
K	12.57	13.21	0.495	0.520
R	2.54	2.79	0.100	0.110

CASE 279-01

FIGURE 1 – RELATIVE INTENSITY versus WAVELENGTH



***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic	Figure No.	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 100 μA)	–	BV_R	4.0	–	–	Volts
Forward Voltage (I_F = 25 mA)	2	V_F	–	2.1	3.0	Volts

OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Figure No.	Symbol	Min	Typ	Max	Unit
*Axial Luminous Intensity (1) (I_F = 25 mA)	3,4,5	I_o	0.3	0.8	–	mcd
Effective Luminous Area	–	–	–	0.03	–	Square-Inch Circle
Peak Emission Wavelength	–	λp	–	575	–	nM
Spectral Line Half Width	–	Δλ	–	30	–	nM

*Indicates JEDEC Registered Data.

(1) Axial Luminous Intensity (I_o) is measured using an International Commission on Illumination corrected Photometer and a measurement solid angle of 0.003 Steradian.

TYPICAL CHARACTERISTICS

FIGURE 2 – FORWARD CHARACTERISTICS

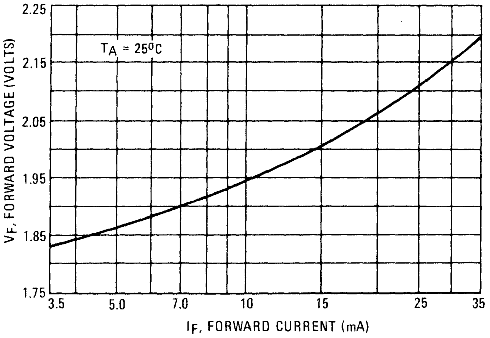


FIGURE 3 – AXIAL LUMINOUS INTENSITY versus JUNCTION TEMPERATURE

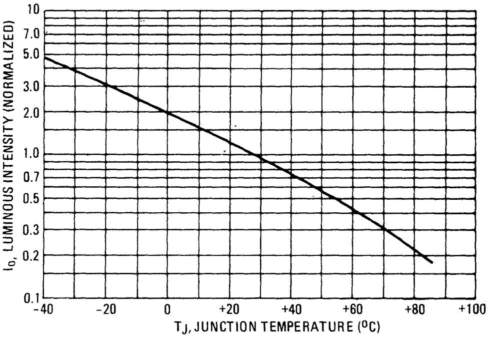


FIGURE 4 – AXIAL LUMINOUS INTENSITY versus FORWARD CURRENT

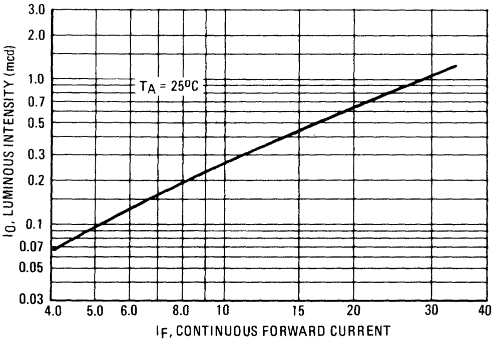
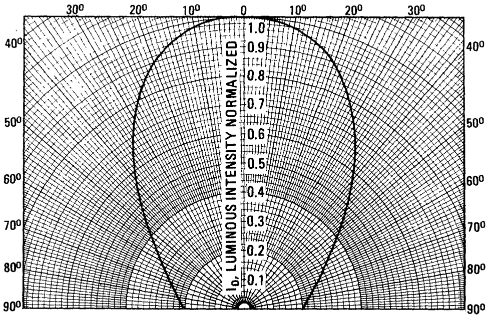


FIGURE 5 – SPATIAL RADIATION PATTERN



1N5913 (SILICON)
thru
1N5956

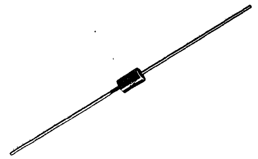
1.5 WATT HERMETICALLY SEALED GLASS SILICON ZENER DIODES

. . . A completely new line of 1.5-Watt Zener Diodes offering the following advantages:

- Complete Voltage Range – 3.3 to 200 Volts
- DO-41 Package – Smaller than Conventional Metal Devices
- Double Slug Type Construction – Mobile Particle Problem Eliminated
- Metallurgically Bonded Construction
- JEDEC Registered Parameters
- Oxide Passivated Diode

GLASS ZENER DIODES

1.5 WATTS
3.3 – 200 VOLTS



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Power Dissipation @ T_L = 75°C, Lead Length = 3/8" Derate above 75°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200	°C

*Indicates JEDEC Registered Data.

MECHANICAL CHARACTERISTICS

CASE: Double slug type, hermetically sealed glass

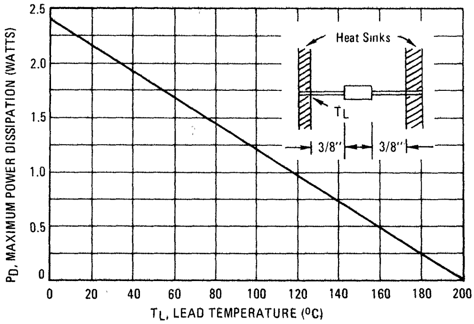
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 230°C, 1/16" from case for 10 seconds

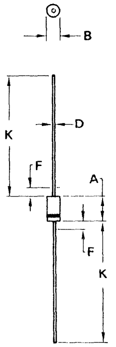
FINISH: All external surfaces are corrosion resistant with readily solderable leads

POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.

MOUNTING POSITION: Any

FIGURE 1 – STEADY STATE POWER DERATING





NOTE
1 POLARITY DENOTED BY CATHODE BAND

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.07	5.20	0.160	0.205
B	2.04	2.71	0.080	0.107
D	0.71	0.86	0.028	0.034
F	–	1.27	–	0.050
K	27.94	–	1.100	–

All JEDEC dimensions and notes apply

CASE 59-03
DO-41

1N5913 thru 1N5956 (continued)

***ELECTRICAL CHARACTERISTICS** (T_L = 30°C unless otherwise noted.) (V_F = 1.5 Volts Max @ I_F = 200 mAdc for all types.)

Motorola Type Number (Note 1)	Nominal Zener Voltage V_Z @ I_{ZT} Volts (Note 2)	Test Current I_{ZT} mA	Max. Zener Impedance			Max. Reverse Leakage Current		Maximum DC Zener Current I_{ZM} mAdc
			Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} Ohms	@ I_{ZK} mA	I_R µA	@ V_R Volts	
1N5913	3.3	113.6	10	500	1.0	100	1.0	454
1N5914	3.6	104.2	9.0	500	1.0	75	1.0	416
1N5915	3.9	96.1	7.5	500	1.0	25	1.0	384
1N5916	4.3	87.2	6.0	500	1.0	5.0	1.0	348
1N5917	4.7	79.8	5.0	500	1.0	5.0	1.5	319
1N5918	5.1	73.5	4.0	350	1.0	5.0	2.0	294
1N5919	5.6	66.9	2.0	250	1.0	5.0	3.0	267
1N5920	6.2	60.5	2.0	200	1.0	5.0	4.0	241
1N5921	6.8	55.1	2.5	200	1.0	5.0	5.2	220
1N5922	7.5	50.0	3.0	400	0.5	5.0	6.0	200
1N5923	8.2	45.7	3.5	400	0.5	5.0	6.5	182
1N5924	9.1	41.2	4.0	500	0.5	5.0	7.0	164
1N5925	10	37.5	4.5	500	0.25	5.0	8.0	150
1N5926	11	34.1	5.5	550	0.25	1.0	8.4	136
1N5927	12	31.2	6.5	550	0.25	1.0	9.1	125
1N5928	13	28.8	7.0	550	0.25	1.0	9.9	115
1N5929	15	25.0	9.0	600	0.25	1.0	11.4	100
1N5930	16	23.4	10	600	0.25	1.0	12.2	93
1N5931	18	20.8	12	650	0.25	1.0	13.7	83
1N5932	20	18.7	14	650	0.25	1.0	15.2	75
1N5933	22	17.0	17.5	650	0.25	1.0	16.7	68
1N5934	24	15.6	19	700	0.25	1.0	18.2	62
1N5935	27	13.9	23	700	0.25	1.0	20.6	55
1N5936	30	12.5	28	750	0.25	1.0	22.8	50
1N5937	33	11.4	33	800	0.25	1.0	25.1	45
1N5938	36	10.4	38	850	0.25	1.0	27.4	41
1N5939	39	9.6	45	900	0.25	1.0	29.7	38
1N5940	43	8.7	53	950	0.25	1.0	32.7	34
1N5941	47	8.0	67	1000	0.25	1.0	35.8	31
1N5942	51	7.3	70	1100	0.25	1.0	38.8	29
1N5943	56	6.7	86	1300	0.25	1.0	42.6	26
1N5944	62	6.0	100	1500	0.25	1.0	47.1	24
1N5945	68	5.5	120	1700	0.25	1.0	51.7	22
1N5946	75	5.0	140	2000	0.25	1.0	56.0	20
1N5947	82	4.6	160	2500	0.25	1.0	62.2	18
1N5948	91	4.1	200	3000	0.25	1.0	69.2	16
1N5949	100	3.7	250	3100	0.25	1.0	76.0	15
1N5950	110	3.4	300	4000	0.25	1.0	83.6	13
1N5951	120	3.1	380	4500	0.25	1.0	91.2	12
1N5952	130	2.9	450	5000	0.25	1.0	98.8	11
1N5953	150	2.5	600	6000	0.25	1.0	114	10
1N5954	160	2.3	700	6500	0.25	1.0	121.6	9.0
1N5955	180	2.1	900	7000	0.25	1.0	136.8	8.0
1N5956	200	1.9	1200	8000	0.25	1.0	152	7.0

*Indicates JEDEC Registered Data.

NOTE 1 – TOLERANCE AND VOLTAGE DESIGNATION

Tolerance designation – The type numbers listed indicate a tolerance of ±20%. Device tolerances of ±10% are indicated by an "A" suffix, ±5% by a "B" suffix, ±2% by a "C" suffix, ±1% by a "D" suffix.

Non-Standard voltage designation – To designate units with zener voltages other than those assigned the Motorola type number should be used.

EXAMPLE:

M	Z	G	41	–	6.0	A
Motorola	Zener	Glass	Series		Nominal Voltage	Tolerance (±%)

NOTE 2 – SPECIAL SELECTIONS AVAILABLE INCLUDE:

(a) Nominal zener voltages between those shown.

(b) Matched sets (Standard Tolerances are ±5.0%, ±2.0%, ±1.0%)

a. Two or more units for series connection with specified tolerance on total voltage. Series matched sets make zener voltages in excess of 200 volts possible as well as providing lower temperature coefficients, lower dynamic impedance and greater power handling ability

b. Two or more units matched to one another with any specified tolerance.

TYPICAL CHARACTERISTICS

TEMPERATURE COEFFICIENTS (-55°C to +150°C temperature range)

FIGURE 2 – ZENER VOLTAGE – TO 12 VOLTS

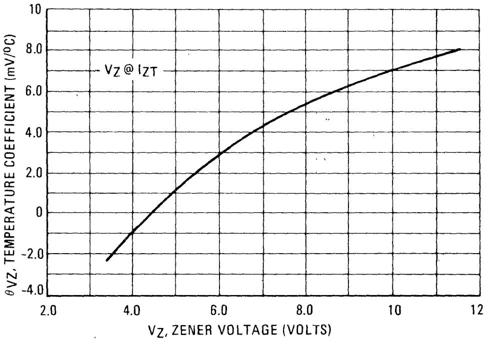
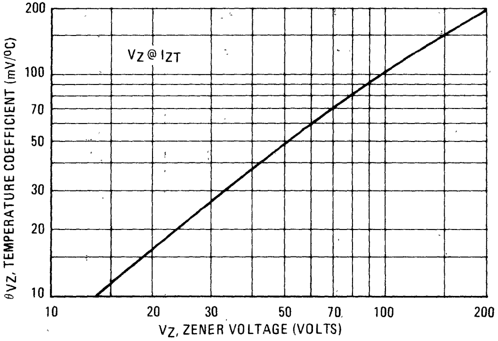


FIGURE 3 – ZENER VOLTAGE – 14 TO 200 VOLTS



ZENER IMPEDANCE

FIGURE 4 – EFFECT OF ZENER CURRENT

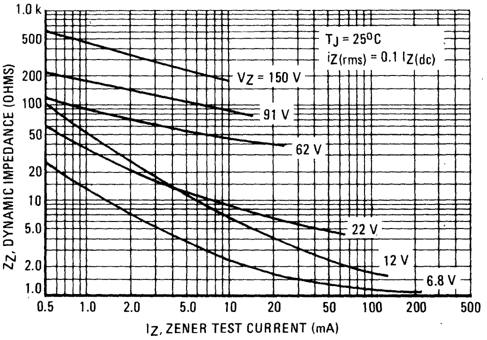
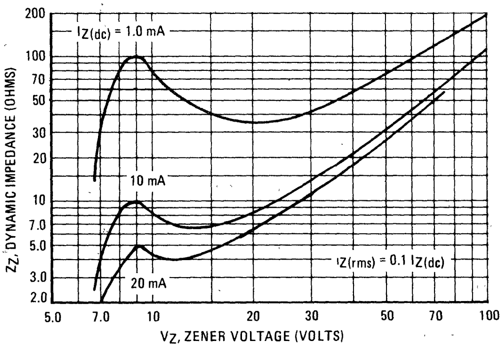


FIGURE 5 – EFFECT OF ZENER VOLTAGE



2N... 3N... & 4N... JEDEC REGISTERED DEVICE SPECIFICATIONS

2N5016 (SILICON)

The RF Line

NPN SILICON RF POWER TRANSISTOR

. . . designed for VHF and UHF power amplifier applications in military and industrial equipment. Suited for use in Class B or C amplifier applications to 600 MHz.

- High Power Output –
  P_{out} = 15 W (Min) @ f = 400 MHz
- Balanced Emitter Construction to Assure Ruggedness and Resist Transistor Damage Due to Load Mismatch
- Large-Signal Impedance Data Provided to Simplify Matching Network Design

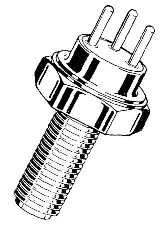
*MAXIMUM RATINGS

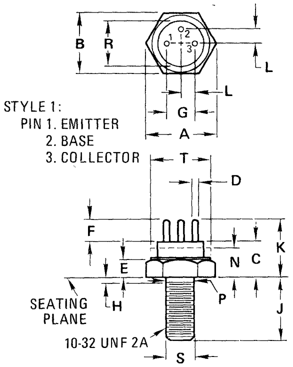
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	65	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current - Continuous	I_C	4.5	Adc
Base Current-Continuous	I_B	1.5	Adc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	30 0.2	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

15 W–400 MHz
RF POWER TRANSISTOR

NPN SILICON





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.57	13.08	0.495	0.515
B	10.77	11.10	0.424	0.437
C	5.46	8.13	0.215	0.320
D	0.762	1.17	0.030	0.046
E	2.29	3.43	0.090	0.135
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	9.53	11.56	0.375	0.455
K	9.02	12.19	0.355	0.480
L	2.29	2.79	0.090	0.110
N	–	4.19	–	0.165
P	4.14	4.80	0.163	0.189
R	8.13	9.14	0.320	0.360
T	9.14	11.10	0.360	0.437

All JEDEC dimensions and notes apply

CASE 36
TO-60

2N5016 (continued)

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	–	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, R_{BE} = 30 ohms)	$V_{CER(sus)}$	40	–	–	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)		–	–	10	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		–	–	10	
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				
(I_C = 500 mAdc, V_{CE} = 4.0 Vdc)		10	–	200	
(I_C = 4.5 Adc, V_{CE} = 4.0 Vdc)		3.0	–	–	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 15 Vdc, f = 400 MHz)	f_T	500	–	–	MHz
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f - 1.0 MHz)	C_{ob}	–	20	25	pF
FUNCTIONAL TEST					
Power Input (P_{out} = 15 W, V_{CC} = 28 Vdc, f = 400 MHz)	P_{in}	–	–	5.0	Watt
Collector Efficiency (P_{in} = 5.0 W, P_{out} = 15 W, V_{CC} = 28 Vdc, f = 400 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data.

(1) Pulsed thru 25 mH Inductor @ 50% Duty Cycle.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 — 400 MHz POWER OUTPUT TEST CIRCUIT

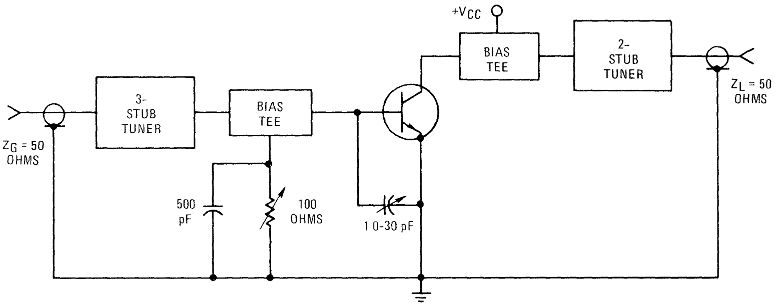


FIGURE 2 – POWER OUTPUT versus FREQUENCY

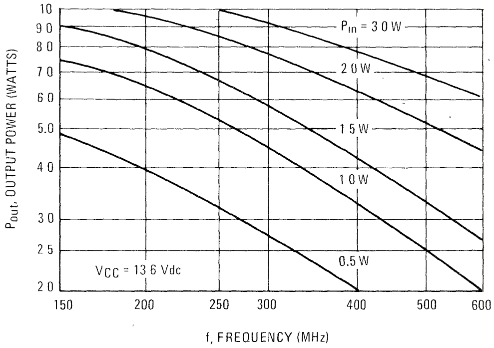


FIGURE 3 – POWER OUTPUT versus FREQUENCY

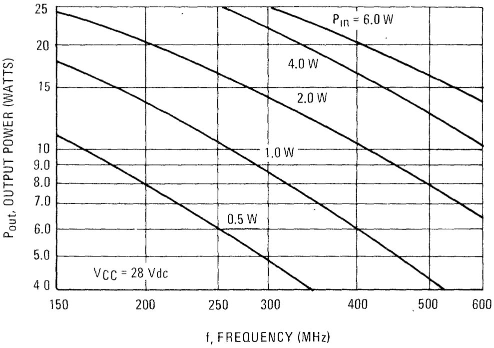


FIGURE 4 – POWER OUTPUT versus POWER INPUT

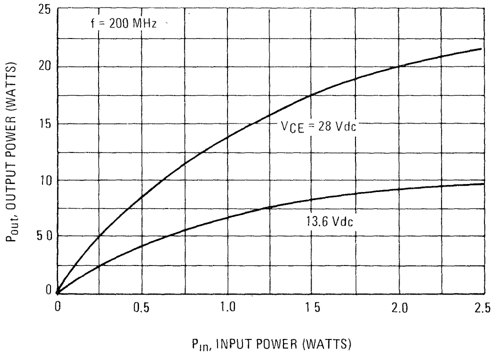


FIGURE 5 – POWER OUTPUT versus POWER INPUT

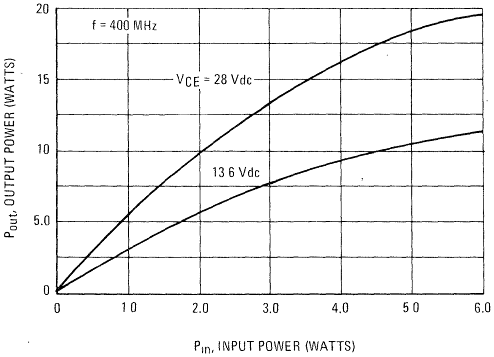


FIGURE 6 – POWER OUTPUT versus POWER INPUT

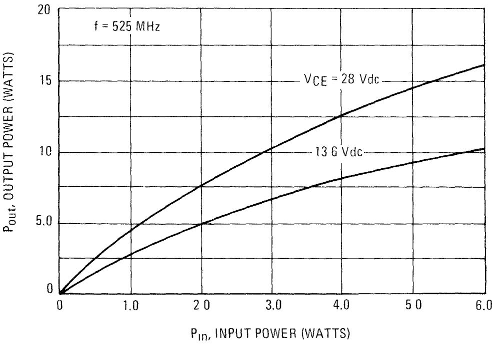
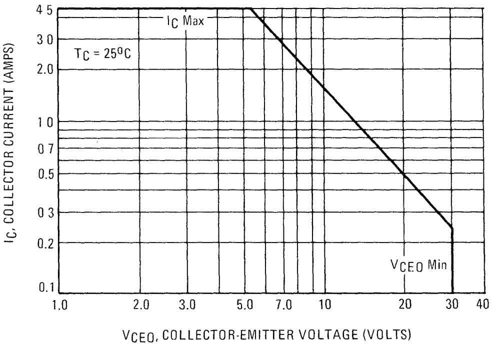


FIGURE 7 – DC SAFE OPERATING AREA



PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

FIGURE 8 – V_{CC} = 13.6 Vdc

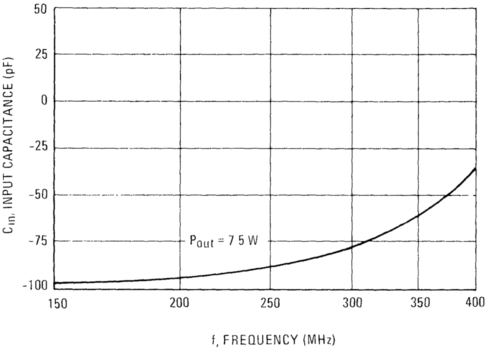
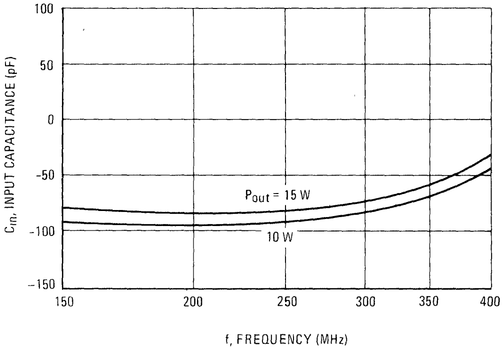


FIGURE 9 – V_{CC} = 28 Vdc



PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

FIGURE 10 – V_{CC} = 13.6 Vdc

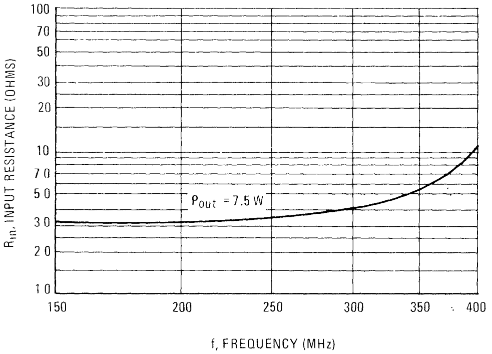
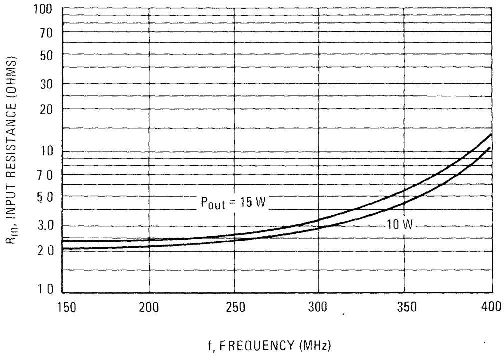


FIGURE 11 – V_{CC} = 28 Vdc



PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

FIGURE 12 – V_{CC} = 13.6 Vdc

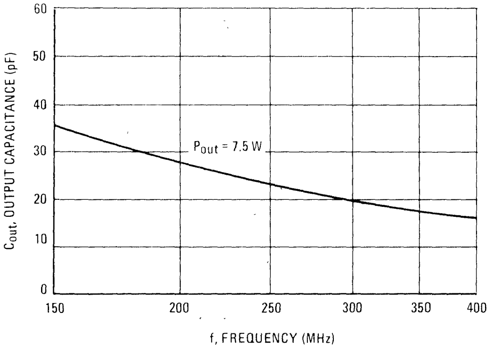
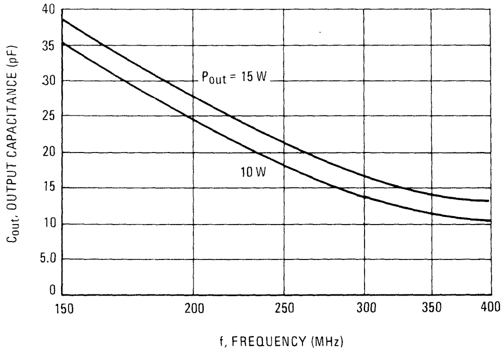


FIGURE 13 – V_{CC} = 28 Vdc



2N5031 (SILICON)
2N5032

NPN SILICON RF SMALL-SIGNAL TRANSISTORS

. . . designed primarily for use in high-gain, low-noise, small-signal amplifiers in military and industrial equipment. Suitable for use in video wideband and general high-frequency amplifier applications of 50 to 1000 MHz.

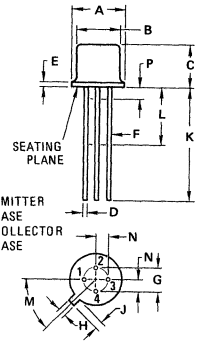
- Low Noise Figure –
  NF = 2.5 dB (Max) @ f = 450 MHz (2N5031)
- High Power Gain –
  G_{pe} = 17 dB (Typ) @ f = 450 MHz
- High Current-Gain–Bandwidth Product –
  f_T = 1000 MHz (Min) @ I_C = 5.0 mAdc

NPN SILICON
RF SMALL-SIGNAL
TRANSISTORS

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	10	Vdc
Collector-Base Voltage	V_{CB}	15	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	20	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	200 1.14	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



STYLE 10
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45°BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

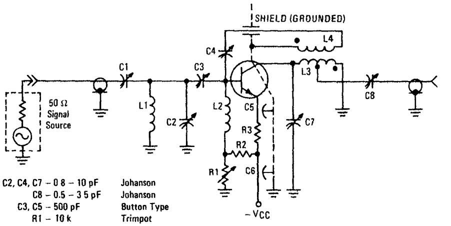
CASE 20-03
TO-72

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	10	–	–	Vdc
*Collector-Base Breakdown Voltage (I_C = 0.01 mAdc, I_E = 0)	BV_{CBO}	15	–	–	Vdc
*Emitter-Base Breakdown Voltage (I_E = 0.01 mAdc, I_C = 0)	BV_{EBO}	3.0	–	–	Vdc
*Collector Cutoff Current (V_{CB} = 6.0 Vdc, I_E = 0)	I_{CBO}	–	1.0	10	nAdc
ON CHARACTERISTICS					
*DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc)	h_{FE}	25	–	300	–
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	–	0.35	–	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 5.0 mAdc)	$V_{BE(sat)}$	–	1.0	–	Vdc
DYNAMIC CHARACTERISTICS					
*Current-Gain—Bandwidth Product (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	1000	–	3500	MHz
*Output Capacitance (V_{CE} = 6.0 Vdc, I_E = 0, f = 0.1 MHz)	C_{cb}	–	1.3	1.5	pF
Collector-Base Time Constant (I_C = 6.0 mAdc, V_{CE} = 6.0 Vdc, f = 31.8 MHz)	$r_b'C_c$	–	5.0	–	ps
*Noise Figure† (Figure 1) (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz) 2N5031 2N5032	NF	 – –	 – –	 2.5 3.0	dB
FUNCTIONAL TEST					
*Common-Emitter Amplifier Power Gain† (Figure 1) (V_{CE} = 6.0 Vdc, I_C = 1.0 mAdc, f = 450 MHz)	G_{pe}	14	17	25	dB

*Indicates JEDEC Registered Data.
†Tuned for Minimum Noise.

FIGURE 1 – POWER GAIN AND NOISE FIGURE TEST CIRCUIT



C1, C2, C4, C7	– 0.8 – 10 pF	Johanson
C8	– 0.5 – 3.5 pF	Johanson
C3, C5	– 500 pF	Button Type
R1	– 10 k	Trimpot
R2	– 2.7 k	1/4 watt 5%
R3	– 1.0 k	1/4 watt 5%

L1 – 1/4" Brass Rod, Solder Plated, 1-1/8" long. Placed 5/8" from the socket and in parallel with the shield, which bisects the socket. The ungrounded side is soldered directly to the ungrounded side of C2.

L2 – 0.22 μH

L3 – 1/4" Brass Rod, Solder Plated, 1-1/2" long. Placed 1/2" from the socket and in parallel with shield, which bisects the socket. The ungrounded side is soldered directly to the ungrounded side of C7. Output tap is 15/16" from ground.

L4 – 1/2 Turn #16, 5/16" above L3 and 5/8" long, (over L3).

FIGURE 2 – COLLECTOR-BASE CAPACITANCE versus VOLTAGE

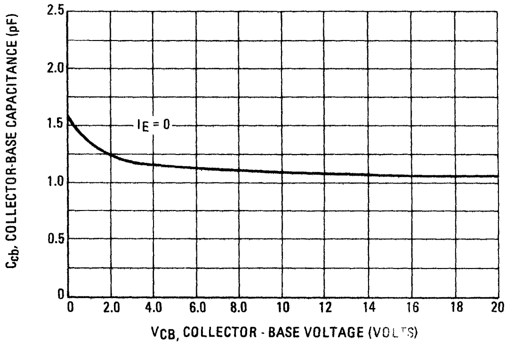


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

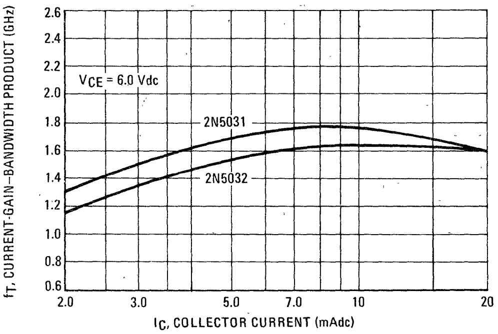


FIGURE 4 – S_{11} AND S_{22}

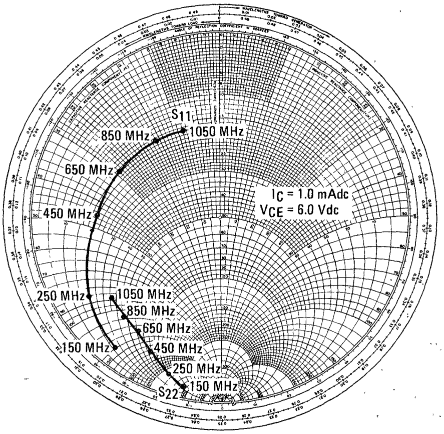


FIGURE 5 – S_{12}

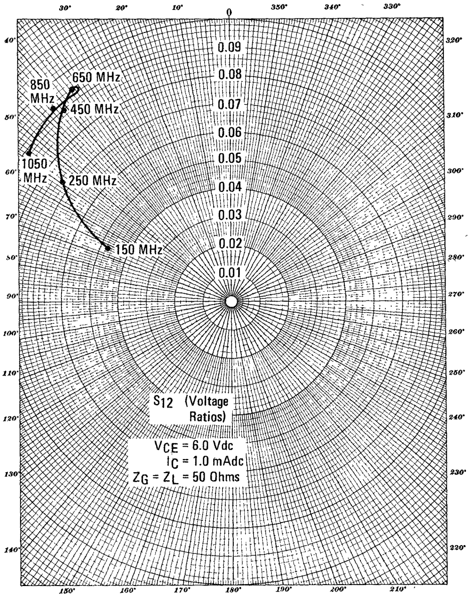


FIGURE 6 – S_{21}

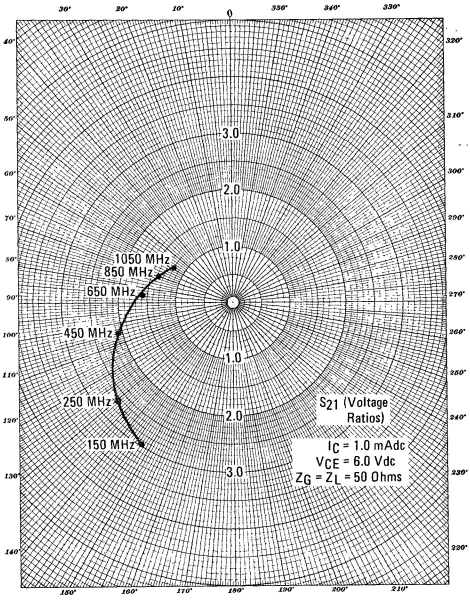


FIGURE 7 – NOISE FIGURE versus FREQUENCY

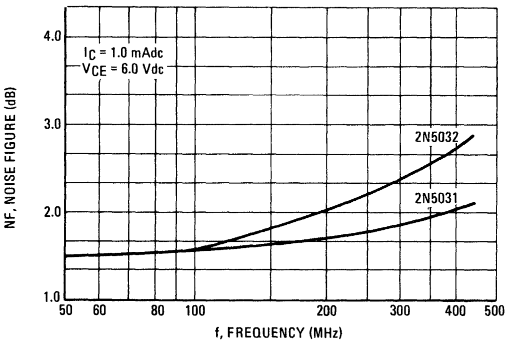


FIGURE 8 – POWER GAIN versus FREQUENCY

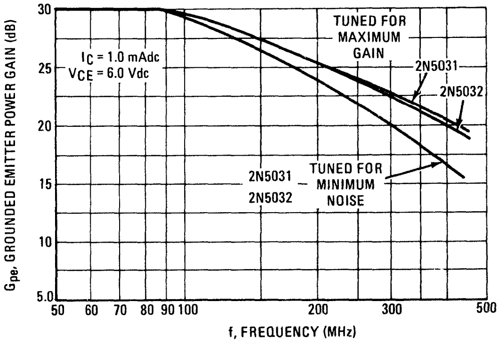


FIGURE 9 – INPUT ADMITTANCE versus FREQUENCY

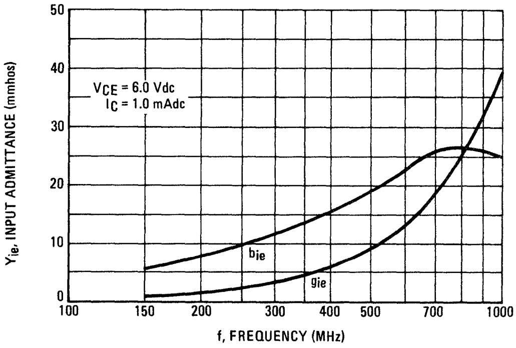


FIGURE 10 – OUTPUT ADMITTANCE versus FREQUENCY

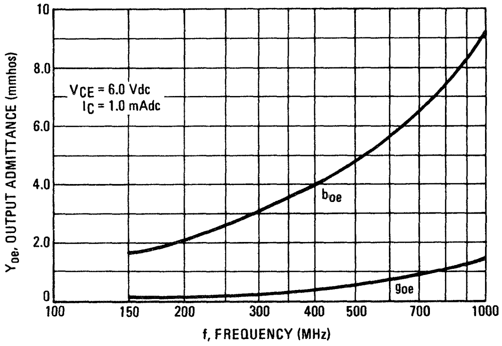


FIGURE 11 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

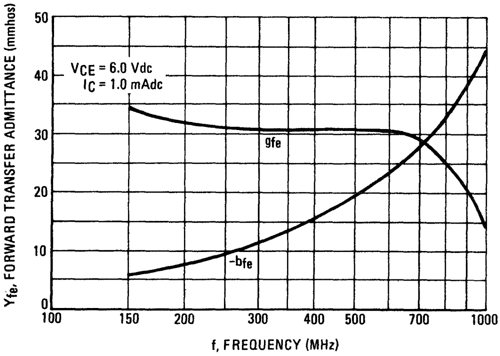
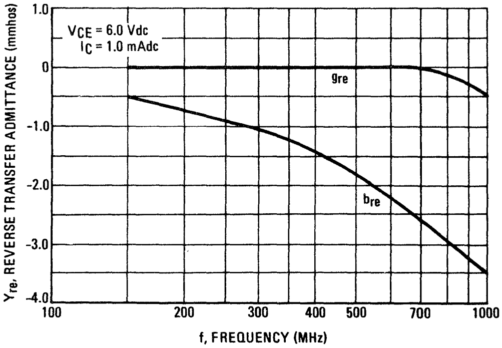


FIGURE 12 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY



2N5050 (SILICON)
2N5051
2N5052

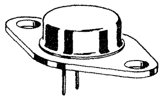
MEDIUM-POWER NPN SILICON TRANSISTORS

. . . designed for untuned amplifier and switching applications.

- High Voltage Ratings – V_{CEO} = 125, 150 and 200 Vdc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 0.75 Adc
- Packaged in the Compact, High Efficiency TO-66 Case

2 AMPERE
POWER TRANSISTORS
NPN SILICON

125-200 VOLTS
40 WATTS



*MAXIMUM RATINGS

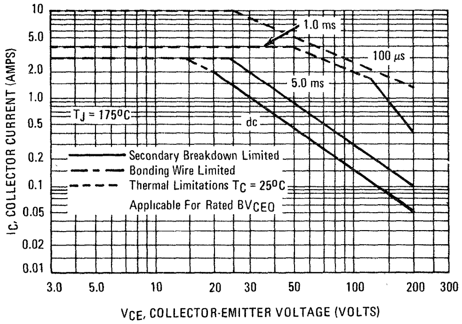
Rating	Symbol	2N5050	2N5051	2N5052	Unit
Collector-Emitter Voltage	V_{CEO}	125	150	200	Vdc
Collector-Base Voltage	V_{CB}	125	150	200	Vdc
Emitter-Base Voltage	V_{EB}	6.0			Vdc
Collector Current – Continuous	I_C	2.0			Adc
Base Current	I_B	1.0			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.266			Watts W/°C
Operating Junction Temperature Range	T_J	-65 to +175			°C
Storage Temperature Range	T_{stg}	-65 to +200			°C

*THERMAL CHARACTERISTICS

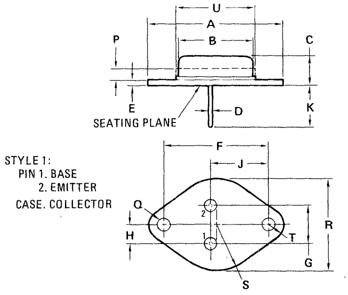
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.76	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

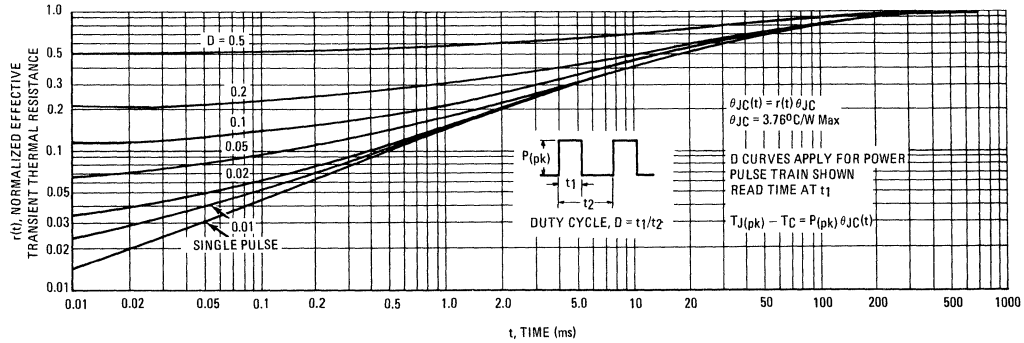
CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (Note 1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5050		125	–	
	2N5051		150	–	
	2N5052		200	–	
Collector-Emitter Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 62.5 Vdc, I_B = 0)	2N5050		–	0.1	
(V_{CE} = 75 Vdc, I_B = 0)	2N5051		–	0.1	
(V_{CE} = 100 Vdc, I_B = 0)	2N5052		–	0.1	
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Emitter-Base Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	mAdc
***ON CHARACTERISTICS**					
DC Current Gain (Note 1)		h_{FE}			–
(I_C = 0.75 Adc, V_{CE} = 5.0 Vdc)			25	100	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			25	–	
(I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage (Note 1)		$V_{CE(sat)}$			Vdc
(I_C = 0.75 Adc, I_B = 0.1 Adc)			–	1.0	
(I_C = 2.0 Adc, I_B = 0.4 Adc)			–	5.0	
Base-Emitter On Voltage (Note 1) (I_C = 0.75 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
***DYNAMIC CHARACTERISTICS**					
Current-Gain—Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 5.0 MHz)		f_T	10	–	MHz
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–
Common Base Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	250	pF
***SWITCHING CHARACTERISTICS**					
Rise Time	(V_{CC} = 120 Vdc, I_C = 750 mAdc, R_L = 150 Ohms, I_{B1} = I_{B2} = 100 mAdc)	t_r	–	300	ns
Storage Time		t_s	–	3.5	μs
Fall Time		t_f	–	1.2	μs

*Indicates JEDEC Registered Data. Note 1: Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 2 – THERMAL RESPONSE



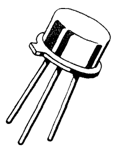
2N5058S (SILICON)

NPN SILICON ANNULAR TRANSISTORS

. . . designed for high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 300 Vdc (Min) – 2N5058S
- DC Current Gain Specified –
  5.0 mAdc to 100 mAdc
- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 30 mAdc

NPN SILICON
AMPLIFIER/DRIVER
TRANSISTORS



*MAXIMUM RATINGS

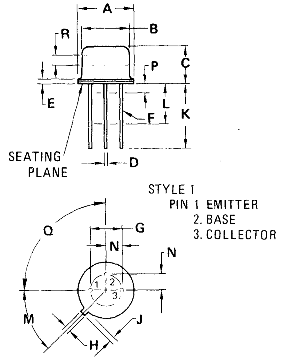
Rating	Symbol	2N5058S	2N5059S	Unit
Collector-Emitter Voltage	V_{CEO}	300	250	Vdc
Collector-Base Voltage	V_{CB}	300	250	Vdc
Emitter-Base Voltage	V_{EB}	7.0	6.0	Vdc
Collector Current – Continuous	I_C	150		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 6.67		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 33.3		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction To Ambient	$R_{\theta JA}$(1)	150	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	30	°C/W

*Indicates JEDEC Registered Data

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 1
PIN 1 EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

CASE 79-02
TO-39

All JEDEC notes and dimensions apply.

*ELECTRICAL CHARACTERISTICS (T_A 25°C unless otherwise noted)

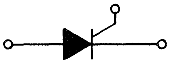
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1)	BV_{CEO}			Vdc
(I_C = 30 mAdc, I_B = 0) 2N5058S		300	—	
2N5059S		250	—	
Collector-Base Breakdown Voltage	BV_{CBO}			Vdc
(I_C = 100 µAdc, I_E = 0) 2N5058S		300	—	
2N5059S		250	—	
Emitter-Base Breakdown Voltage	BV_{EBO}			Vdc
(I_E = 100 µAdc, I_C = 0) 2N5058S		7.0	—	
2N5059S		6.0	—	
Collector Cutoff Current	I_{CBO}			µAdc
(V_{CB} = 100 Vdc, I_E = 0)		—	0.05	
(V_{CB} = 100 Vdc, I_E = 0, T_A = +125°C)		—	20	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	10	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			—
(I_C = 5.0 mAdc, V_{CE} = 25 Vdc) 2N5058S		10	—	
2N5059S		10	—	
(I_C = 30 mAdc, V_{CE} = 25 Vdc) 2N5058S		35	150	
2N5059S		30	150	
(I_C = 30 mAdc, V_{CE} = 25 Vdc, T_A = -55°C) 2N5058S		10	—	
(I_C = 100 mAdc, V_{CE} = 25 Vdc) 2N5058S		35	—	
2N5059S		30		
Collector-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{BE(sat)}$	—	0.85	Vdc
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 25 Vdc)	$V_{BE(on)}$	—	0.82	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (2) (I_C = 10 mAdc, V_{CE} = 25 Vdc, f = 20 MHz)	f_T	30	160	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	10	pF
Emitter-Base Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{eb}	—	75	pF

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width $\leqslant$300 µs, Duty Cycle $\leqslant$2.0%

(2) f_T is defined as the frequency at which $|h_{fe}|$ extropolates to unity.

2N5060 (SILICON)
thru
2N5064



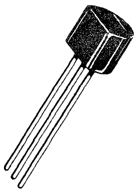
PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
30 thru 200 VOLTS

PLASTIC THYRISTORS

. . . Annular PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 50 μA Maximum, $T_C = 125^\circ C$
- Low Holding Current – 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity

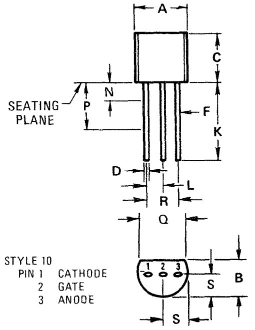


MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage	V_{RRM}		Volts
2N5060		30*	
2N5061		60*	
2N5062		100*	
2N5063		150*	
2N5064		200*	
Forward Current RMS (See Figures 4 & 5) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, $T_A = 25^\circ C$ (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	6.0*	Amp
Circuit Fusing Considerations, $T_A = 25^\circ C$ (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
Peak Gate Power – Forward, $T_A = 25^\circ C$	P_{GM}	0.1*	Watt
Average Gate Power – Forward, $T_A = 25^\circ C$	$P_{GF(AV)}$	0.01*	Watt
Peak Gate Current – Forward, $T_A = 25^\circ C$ (300 μs, 120 PPS)	I_{GFM}	1.0*	Amp
Peak Gate Voltage – Reverse	V_{GRM}	5.0*	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +125*	°C
Storage Temperature Range	T_{stg}	-65 to +150*	°C
Lead Solder Temperature (<1/16″ from case, 10 s max)	–	+230*	°C

*Indicates JEDEC Registered Data.

(1) Temperature reference point for all case temperatures in center of flat portion of package. ($T_C = +125^\circ C$ unless otherwise noted.)



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (Note 1)		V_{DRM}			Volts
(T_C = 125°C)	2N5060		30*	–	
	2N5061		60*	–	
	2N5062		100*	–	
	2N5063		150*	–	
	2N5064		200*	–	
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C)		I_{DRM}	–	50*	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C)		I_{RRM}	–	50*	μA
Forward "On" Voltage (Note 2) (I_{TM} = 1.2 A peak @ T_A = 25°C)		V_{TM}	–	1.7*	Volts
Gate Trigger Current (Continuous dc) (Note 3)	T_C = 25°C	I_{GT}	–	200	μA
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C		–	350*	
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	–	0.8	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C		–	1.2*	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C	V_{GD}	0.1	–	
Holding Current	T_C = 25°C	I_H	–	5.0	mA
(Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = -65°C		–	10*	
Thermal Resistance, Junction to Case (Note 4)		θ_{JC}	–	75*	°C/W
Thermal Resistance, Junction to Ambient		θ_{JA}	–	200	°C/W

*Indicates JEDEC Registered Data.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
3. R_{GK} current is not included in measurement.
4. This measurement is made with the case mounted "flat side down" on a heat sink and held in position by means of a metal clamp over the curved surface.

FIGURE 1 — SURGE RATINGS

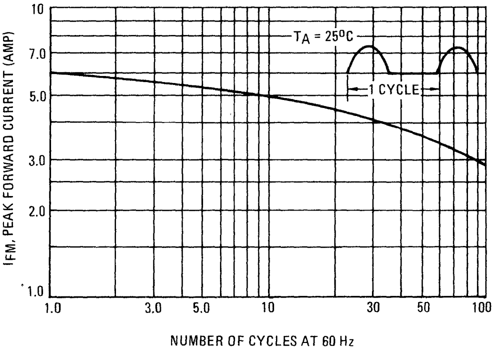


FIGURE 2 — POWER DISSIPATION

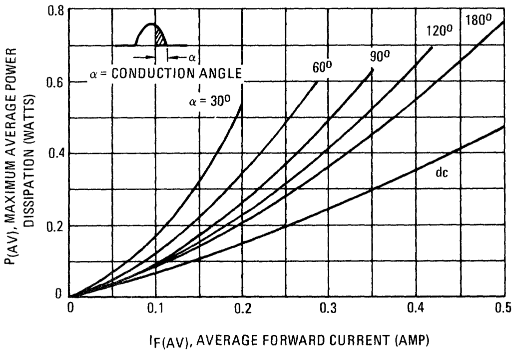


FIGURE 3 – FORWARD VOLTAGE

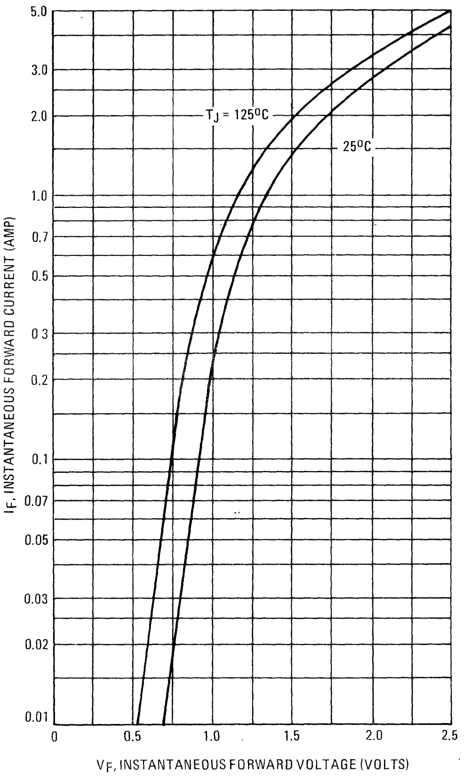


FIGURE 4 – CURRENT DERATING (REFERENCE: CASE TEMPERATURE)

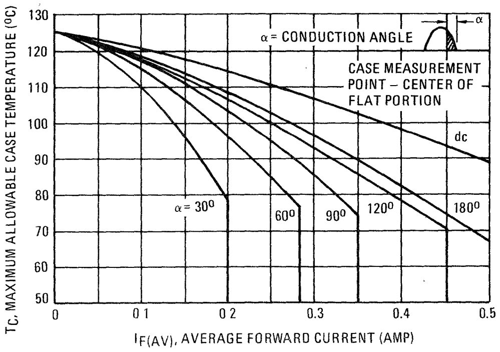


FIGURE 5 – CURRENT DERATING (REFERENCE: AMBIENT TEMPERATURE)

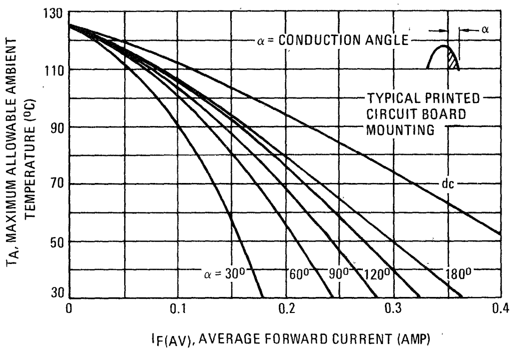
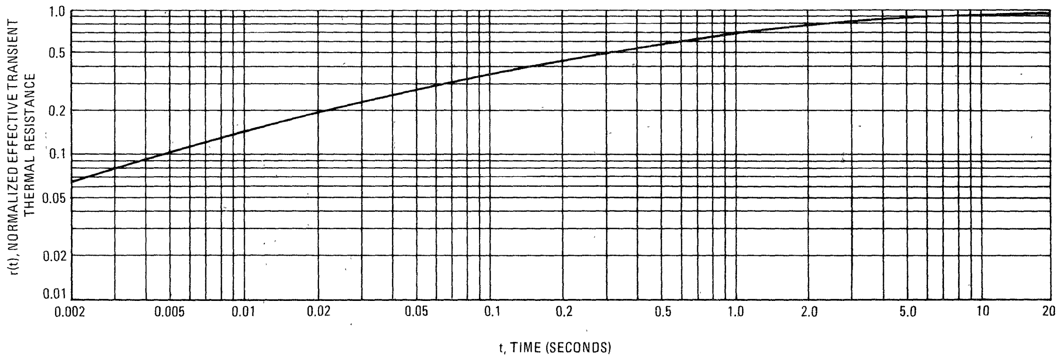


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 7 – GATE TRIGGER VOLTAGE

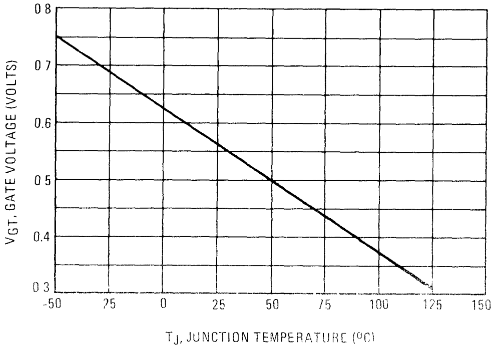


FIGURE 8 – GATE TRIGGER CURRENT

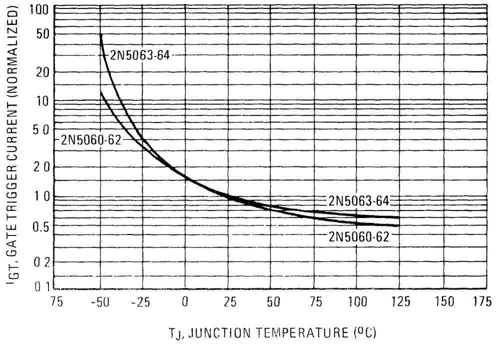


FIGURE 9 – HOLDING CURRENT

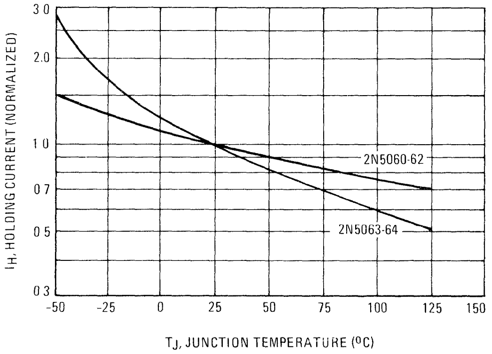
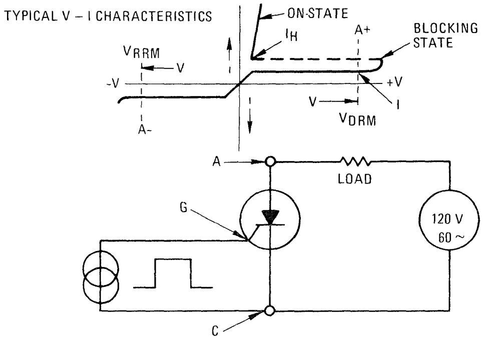


FIGURE 10 – CHARACTERISTICS AND SYMBOLS



SELECTED THYRISTOR-TRIGGER APPLICATION NOTES

AN-240 – SCR Power Control Fundamentals
AN-290B – Mounting Procedure for, and Thermal Aspects of, Thermopad Plastic Power Devices
AN-295 – Suppressing RFI in Thyristor Circuits
AN-422 – Testers for Thyristors and Trigger Diodes
AN-453 – Zero Point Switching Techniques

To obtain copies of these notes list the AN number(s) on your company letterhead and send your request to:

Technical Information Center
Motorola Semiconductor Products, Inc.
P.O. Box 20924
Phoenix, Arizona 85036

2N5067 (SILICON)
2N5068
2N5069

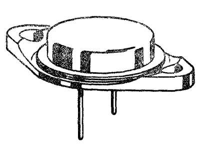
SILICON NPN POWER TRANSISTORS

. . . for use in power amplifier and switching circuits.

- Low Saturation Voltage — $V_{CE(sat)} = 0.4$ Vdc @ $I_C = 1.0$ Amp
- Excellent Safe Area Limits (Figure 11)
- Power Dissipation — $P_D = 87.5$ W @ $T_C = 25°C$
- Complement to PNP 2N4901, 2N4902, 2N4903

5 AMPERE POWER TRANSISTORS SILICON NPN

40-80 VOLTS
87.5 WATTS



MAXIMUM RATINGS

Rating	Symbol	2N5067	2N5068	2N5069	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous	I_C	5.0			Adc
Base Current - Continuous	I_B	1.0			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	87.5 0.5			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

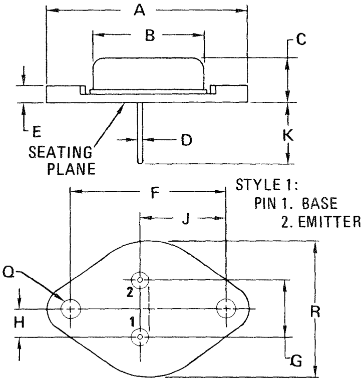
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 0.2 Adc, I_B = 0) 2N5067 2N5068 2N5069	11	$V_{CEO(sus)}$*	40 60 80	- - -	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}	-	1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	5, 6	I_{CEX}	- -	1.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	5, 6	I_{CBO}	-	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	-	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	1	h_{FE}*	20 7.0	80 -	-
Collector-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc)	2, 3, 4	$V_{CE(sat)}$*	- -	0.4 1.5	Vdc
Base-Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	3, 4	$V_{BE(on)}$*	-	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	4.0	-	MHz
Small-Signal Current Gain (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	-	-

* Pulse Test, PW ≈ 300 μs, Duty Cycle ≈ 2.0%



STYLE 1:
PIN 1. BASE
2. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector Connected to Case

CASE 11-03

FIGURE 1 — NORMALIZED DC CURRENT GAIN

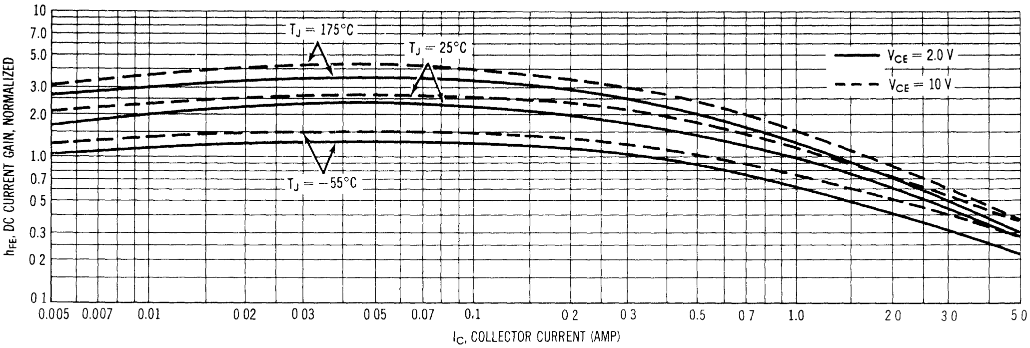


FIGURE 2 — COLLECTOR SATURATION REGION

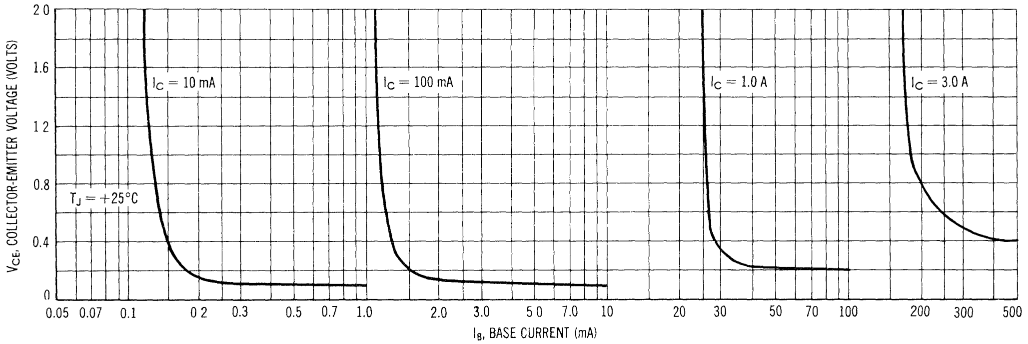


FIGURE 3 — "ON" VOLTAGES

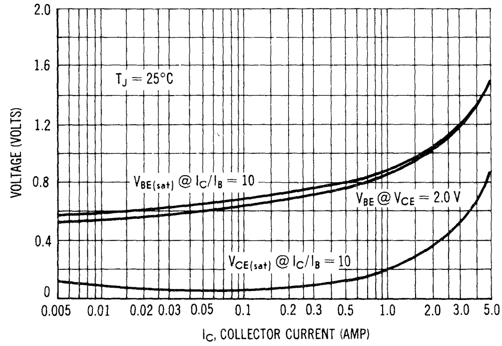
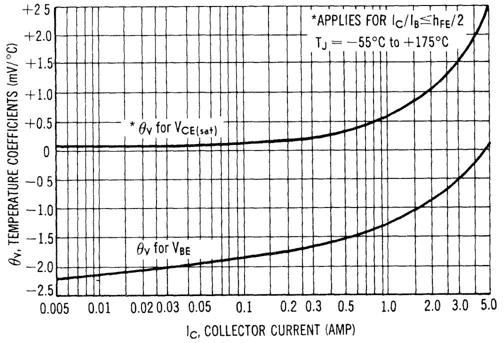


FIGURE 4 — TEMPERATURE COEFFICIENTS



TYPICAL "OFF" REGION CHARACTERISTICS

FIGURE 5 — CUT-OFF REGION

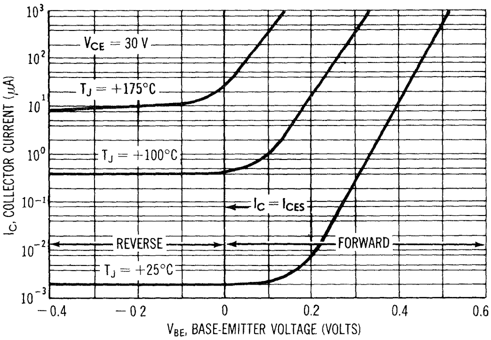


FIGURE 6 — EFFECTS OF BASE-EMITTER RESISTANCE

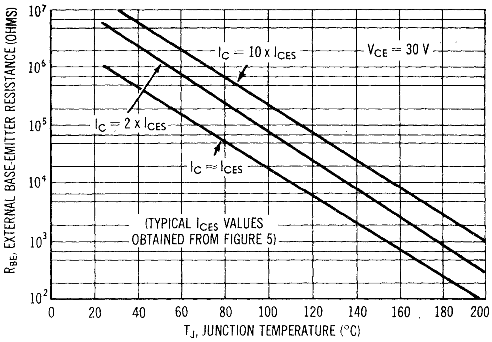


FIGURE 7 — SWITCHING TIME EQUIVALENT CIRCUIT

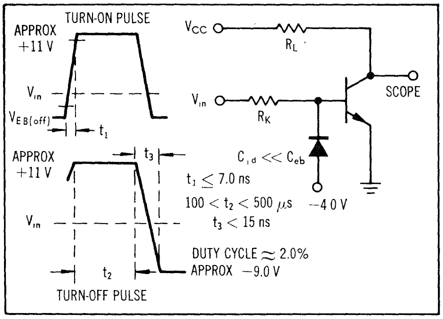


FIGURE 8 — CAPACITANCE

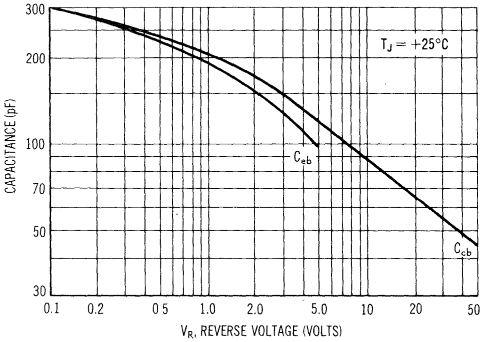


FIGURE 9 — TURN-ON TIME

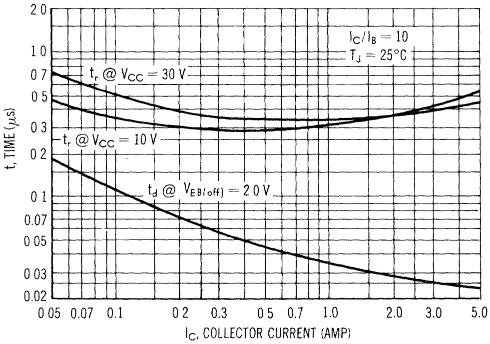
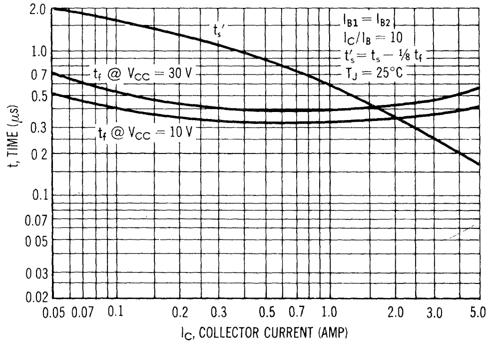
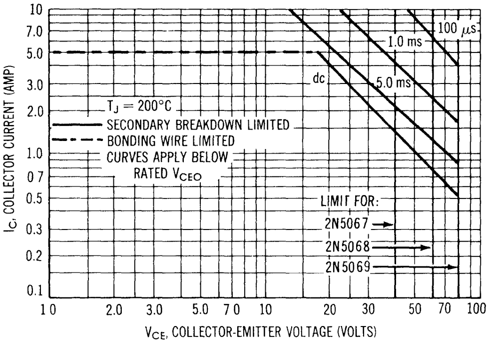


FIGURE 10 — TURN-OFF TIME



RATING AND THERMAL DATA

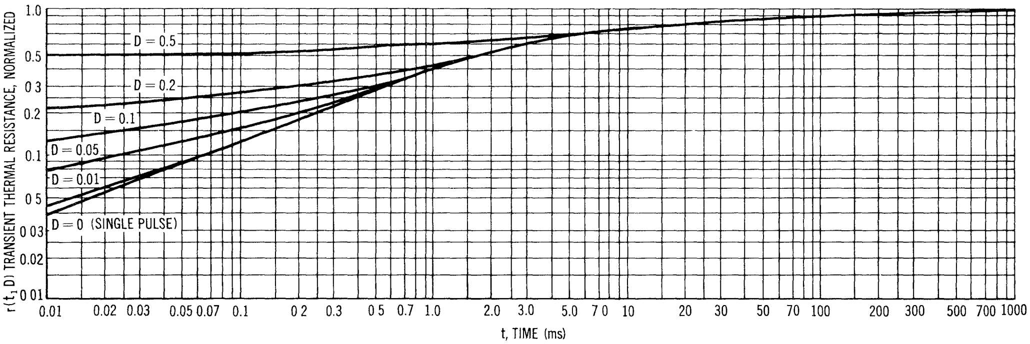
FIGURE 11 — ACTIVE-REGION SAFE OPERATING AREAS



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

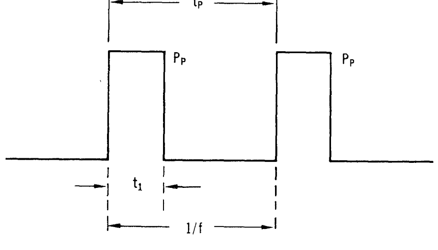
The data of Figure 11 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 12 — TRANSIENT THERMAL RESISTANCE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



DUTY CYCLE $D = t_1 \cdot f = \frac{t_1}{t_P}$

PEAK PULSE POWER = P_P

A train of periodical power pulses can be represented by the model as shown in Figure A. Using the model and the device thermal reponse, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5067 is dissipating 100 watts under the following conditions:
t_1 = 0.1 ms, t_P = 0.5 ms. (D = 0.2)

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of r (t_1, D) is 0.28.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.28 \times 100 \times 2.0 = 56°C$$

2N5070 (SILICON)

The RF Line

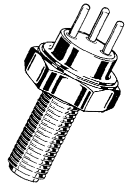
NPN SILICON RF POWER TRANSISTORS

. . . designed primarily for applications as a high-power linear amplifier from 2.0 to 75 MHz.

- Optimized for Operation from a 28-Volt Supply
- Power Out @ 28 Vdc, 30 MHz – 25 W (PEP)
- Intermodulation Distortion at 25 W (PEP)
  IMD = 30 dB (Max)
- Isothermal-Resistor Design Results in Rugged Device

25 W (PEP) – 30 MHz

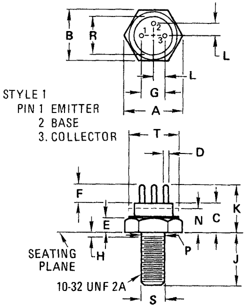
**RF POWER
TRANSISTOR
NPN SILICON**



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous Peak	I_C	3.3 10	Adc
Base Current – Continuous	I_B	1.0	Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	70 400	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



STYLE 1
PIN 1 EMITTER
2 BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.57	13.08	0.495	0.515
B	10.77	11.10	0.424	0.437
C	5.46	8.13	0.215	0.320
D	0.762	1.17	0.030	0.046
E	2.29	3.43	0.090	0.135
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	9.53	11.56	0.375	0.455
K	9.02	12.19	0.355	0.480
L	2.29	2.79	0.090	0.110
N	–	4.19	–	0.165
P	4.14	4.80	0.163	0.189
R	8.13	9.14	0.320	0.360
T	9.14	11.10	0.360	0.437

All JEDEC dimensions and notes apply

Emitter connected to case

**CASE 36
TO-60**

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

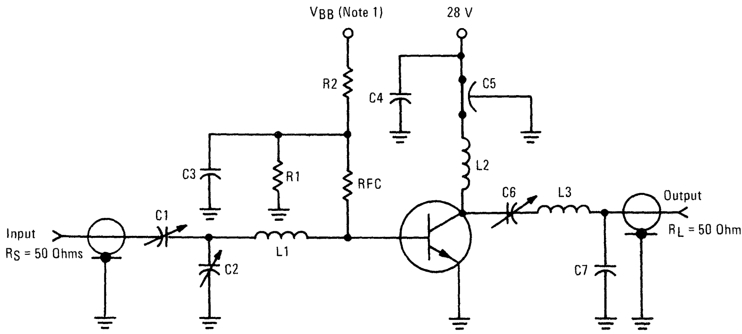
— Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage(1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	–	Vdc
Collector-Emitter Sustaining Voltage(1) (I_C = 200 mAdc, R_{BE} = 5.0 ohms)	$V_{CER(sus)}$	40	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	5.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, V_{BE} = −1.5 Vdc) (V_{CE} = 60 Vdc, V_{BE} = −1.5 Vdc, T_C = 150°C)	I_{CEX}	 – –	 10 10	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	I_{CBO}	–	10	mAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	10	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 10 10	 100 100	–
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product(2) (I_C = 1.0 Adc, V_{CE} = 15 Vdc, f = 50 MHz)	f_T	100	–	MHz
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	85	pF
FUNCTIONAL TEST (Figure 1)				
Power Input (P_{out} = 25 W (PEP), Z_G = 50 Ohms, V_{CE} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	P_{in}	–	1.25	Watt (PEP)
Collector Efficiency (P_{out} = 25 W (PEP), Z_G = 50 Ohms, V_{CE} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	η	40	-	%
Intermodulation Distortion (P_{out} = 25 W (PEP), Z_G = 50 Ohms, V_{CE} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	IMD	–	-30	dB

*Indicates JEDEC Registered Data.

(1)Pulsed thru 25 mH Inductor, Duty Cycle = 50%, Repetition Rate = 60 Hz.

(2)f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – 30 MHz LINEAR TEST CIRCUIT



L1: 3 Turns No. 12 AWG, 1/4″ I.D., 1/2″ Long
L2: 6 Turns No. 14 AWG, 3/8″ I.D., 3/4″ Long
L3: 5 Turns No. 10 AWG, 3/4″ I.D., 3/4″ Long
C1: 140-680 pF, ARCO 468 or Equivalent
C2: 170-780 pF, ARCO 469 or Equivalent
C3: 0.05 μF, Ceramic Capacitor
C4: 0.1 μF, Ceramic Capacitor
C5: 1000 pF, Feedthrough Capacitor
C6: 24-200 pF, ARCO 425, or Equivalent
C7: 32-250 pF, ARCO 426, or Equivalent
Q: 2N5070
R1: 1.0 Ω, 5.0 W
R2: 50 Ohms, 25 W
RFC: 350 Ferrite Choke, Ferroxcube* #VK200 01-03B, or Equivalent

*Ferroxcube Corp. of America, Saugerties, N. Y.

Note 1: Adjust V_{BB} for a collector quiescent current of 20 mA with no RF input signal.

FIGURE 2 – LINEAR OUTPUT POWER versus FREQUENCY

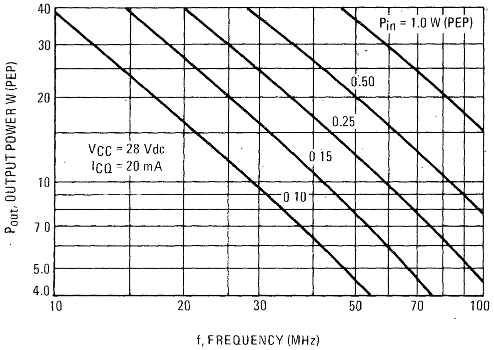


FIGURE 3 – TYPICAL OUTPUT POWER versus INPUT POWER

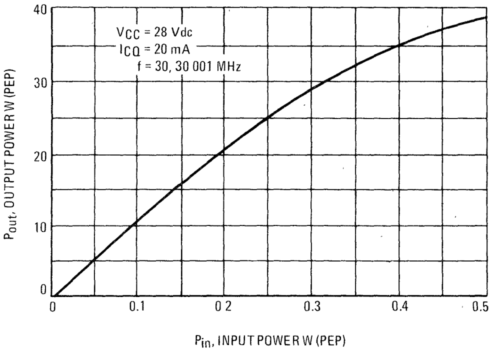


FIGURE 4 – TYPICAL OUTPUT POWER versus INPUT POWER

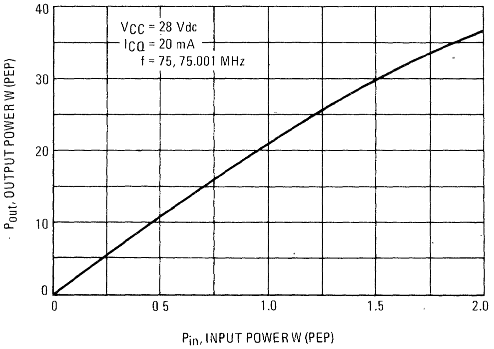
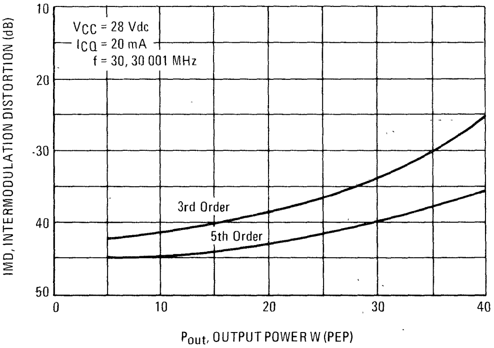


FIGURE 5 – TYPICAL INTERMODULATION DISTORTION versus OUTPUT POWER



LINEAR OUTPUT POWER versus SUPPLY VOLTAGE

FIGURE 6 – f = 30 MHz

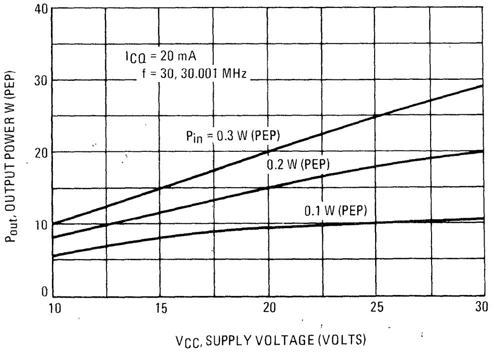


FIGURE 7 – IMD = -30 dB

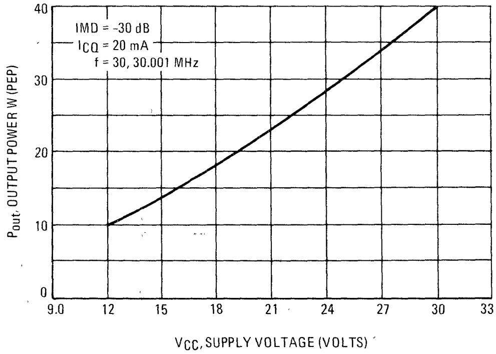


FIGURE 8 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

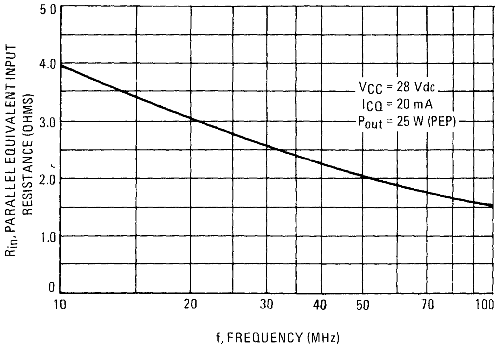


FIGURE 9 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

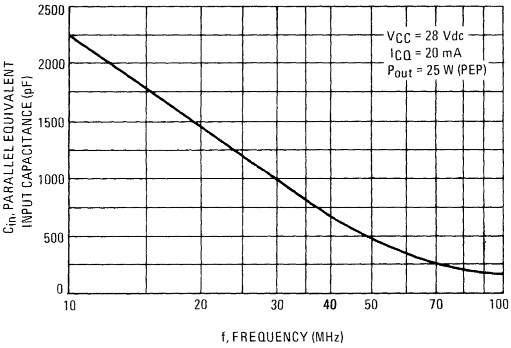


FIGURE 10 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

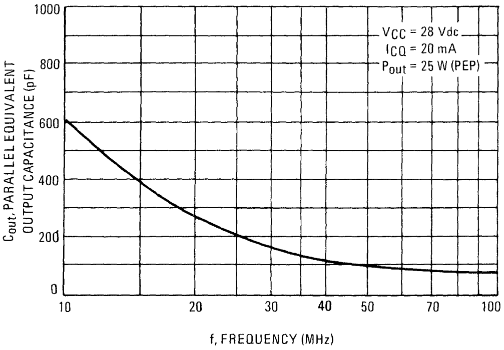
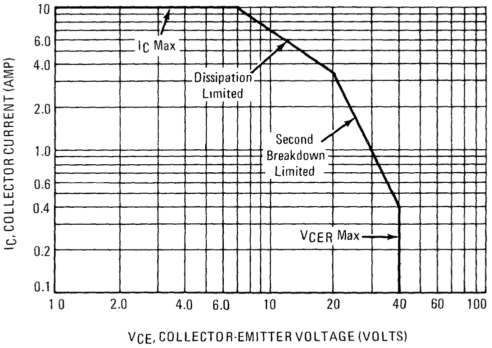


FIGURE 11 – DC SAFE OPERATING AREA



APPLICATIONS INFORMATION

The 2N5070 transistor is designed for linear power amplifier operation in the HF/VHF region (2 to 75 MHz). It features guaranteed linear amplifier performance rather than the conventional performance demonstrated in a class C* amplifier.

Class C operation is inherently non-linear, but in many power amplifier applications non-linear operation does not present major problems. With a single frequency driving signal, the only spurious signals generated are harmonics and these can be suppressed in the amplifier tuned networks and output filter.

For single sideband (SSB), low level amplitude modulation (AM), and other types of complex signals, class C operation is generally not satisfactory. For instance, when a signal contains multiple frequencies at close spacings, odd-order non-linearities will generate spurious outputs which are within the passband of the tuned circuits and filters; therefore, the spurious outputs are not suppressed before they reach the antenna or other load. As a result, such complex signals require linear amplification if the amplified signal is to be free of spurious outputs.

A detailed analysis of spurious signals generated by non-linearities and linearity requirements of various applications is described in Chapter 12 of Reference 1.

The following discussion concerns itself with a detailed description of the 2N5070 characterization curves and general information on solid state linear power amplifier design.

The Two-Tone Test

The 2N5070 functional test specification consists of a linear power amplifier test with guaranteed limits on power output, gain, efficiency, and intermodulation distortion (IMD) output levels. A two-tone test signal is used with the test amplifier as shown in Figure 1.

The two-tone test is one of many methods commonly used for testing linear amplifier performance. This test involves driving the amplifier with two RF signals, of equal amplitude, separated in frequency from each other by approximately 1 kHz.

When a two-tone test signal consisting of frequencies f_1 and f_2 is passed through a non-linear amplifier, odd order non-linearities generate spurious signals near the desired carrier. The level of these spurious signals provides a measure of the degree of non-linearity of the amplifier. This type of non-linearity is called intermodulation distortion (IMD). The spurious signals generated by IMD are further classified according to the exponential order of the amplifier non-linearity, i.e., 3rd order IMD products, 5th order IMD products, etc. The 3rd and 5th order IMD products are usually the most significant encountered with linear power amplifiers. Data on both 3rd and 5th order IMD are included in the 2N5070 characterization.

Third order IMD generates spurious signals near the operating frequency at frequencies $2f_1 - f_2$ and $2f_2 - f_1$; and 5th order IMD spurious signals are at frequencies $3f_1 - 2f_2$ and $3f_2 - 2f_1$.

Specifications and Characterization

The two-tone functional amplifier test is performed in a manner identical to the conventional class C functional test with two exceptions: a two-frequency signal is used in place of a single frequency, and amplifier linearity is added to the items tested and specified.

The functional test procedure for the 2N5070 requires driving the test amplifier with a two frequency signal and measuring power output, gain, efficiency, and linearity.

Power output, gain, and efficiency measurement methods are the same for both linear and class C amplifiers.

Since a multiple frequency test signal has an instantaneous power level which varies with time, power levels are normally expressed in peak envelope power (PEP). This is the average power level of the envelope at its greatest amplitude point.

When the test signal consists of multiple signals with equal amplitudes and different frequencies, the relationship of average power and PEP is given by the following expression:

$$\text{Average power} = \frac{\text{PEP}}{N}$$

where N = the number of input frequencies.

Therefore, when measuring the power level of a standard two-tone test signal, a true average reading power meter will indicate 1/2 the PEP of the signal.

Linearity is tested by measuring the amplitudes of the 3rd and 5th order IMD products. The ratio of one of the 3rd order products to one of the two desired frequencies is then expressed as a power ratio in decibels (dB). This is repeated for the 5th order products. The smaller of these two ratios (usually the 3rd order) is then included in the electrical characteristics specification as intermodulation distortion ratio (IMD).

2N5070 Performance Curves

Figures 2 through 4 show typical power output and gain characteristics versus frequency and/or input power. These curves are similar to those found on other RF power transistor data sheets with one exception, a two-frequency test signal was used rather than a single frequency signal.

The curves shown in Figure 5 are unique to transistors characterized for linear power amplifier service and show the typical IMD levels versus power output.

The 2N5070 features guaranteed IMD performance at the -30 dB level. However, the designer may desire IMD greater or less than -30 dB for a particular application. Figure 5 provides data on IMD levels that can be expected as a function of output power.

Figure 6 shows the variation in gain with dc supply voltage and provide data on gain only. It does not include information on IMD ratio.

Figure 7 reflects the power output that can be obtained at a fixed IMD ratio for operation with dc supply voltages other than 28 Vdc.

Figures 8 through 10 show the large signal impedance characteristics of the 2N5070. These are similar to curves shown on other Motorola data sheets except a two-frequency test signal was used rather than a single frequency signal.

It must be stressed that the data shown in Figures 8 through 10 do not represent y, z, h, s, or any standard two-port parameter set. The actual transistor impedance levels during normal operation in an amplifier are given. For a detailed discussion of RF power transistor large signal impedance, see Reference 2.

Linear Amplifier Design

The following is a discussion of some general design considerations for solid-state linear power amplifiers. While this is not a detailed analysis of linear amplifier design, some general guidelines are provided.

The major difference between linear power amplifiers and class C power amplifiers is in the dc bias circuitry. As stated in the introduction, class C operation usually involves a collector dc supply as

APPLICATIONS INFORMATION (continued)

the only bias voltage with $V_E = V_B = 0$. The collector current is zero until the input RF signal turns the transistor "on".

In contrast, a linear amplifier is normally operated with forward bias and some collector current flowing when no signal is present.

The magnitude of no-signal collector current and the bias circuitry may vary with the application. Optimum no-signal collector current for the 2N5070 was found to be approximately 20 mA.

The key to bias circuitry for good linearity lies in maintaining the base-emitter dc voltage relatively constant as the RF signal amplitude varies. The inherent nature of a forward-biased RF power transistor is to bias itself "off" with increasing RF drive signal. Therefore, a constant voltage source is required for base voltage.

Temperature effects also complicate the situation, since V_{BE} decreases with increasing temperature.

A simple solution to the bias problem involves the use of a forward-biased diode mounted on the transistor heat sink for thermal coupling to the transistor. A large capacitor (several hundred microfarads) in parallel with the diode helps maintain a constant V_{BE} with RF drive and improves linearity, while the diode provides temperature compensation to prevent thermal runaway. It is also possible to use complex active circuitry for biasing, and some rather exotic schemes have been developed to provide the same results.

Another important consideration is the collector-output network. Normally, a network with low impedance to ground for harmonics provides better linearity than a network with high harmonic impedances; therefore, some experimentation with network configuration is in order. Proper impedance matching remains the primary factor in both input and output network design. Further, it must also be stressed that the collector load impedance should be designed for the PEP, not the average power output. See Chapter 13 of Reference 1 for a detailed discussion of network design considerations.

Feedback may also be employed to improve linearity and may take the form of either neutralization or negative RF feedback. The possibilities here are limited only by the designer's imagination. Of course, negative RF feedback involves a decrease in gain to improve linearity.

REFERENCES

1. Pappenfus, Bruene, Schoenike, "Single Sideband Principles and Circuits", McGraw-Hill.
2. Hejhall, "Systemizing RF Power Amplifier Design", Motorola Semiconductor Products Inc., Application Note AN-282A.

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*"Class C", as used here refers to operation with the no signal conditions $I_C = 0$, and $V_{BE} = 0$, and a theoretical conduction angle of less than 180°, even though the actual conduction angle may be more than 180°.

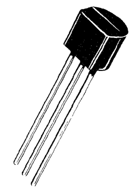
2N5086 (SILICON)
2N5087

PNP SILICON ANNULAR TRANSISTORS

. . . PNP silicon annular transistors designed for low-level, low-noise amplifier applications.

- Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 50 V (Min)
- Low 1.0 kHz Noise Figure —
  2N5086 — 3.0 dB (Max)
  2N5087 — 2.0 dB (Max)
- High Gain at Low Current —
  2N5087 — 250 @ 100 μAdc
- Low Current-Gain—Bandwidth Product to Facilitate Audio Frequency Design — f_T = 40 MHz (Min)
- Low Leakage Current — I_{CBO} = 10 nAdc (Max) @ 10 V
- Low Collector-Base Capacitance — C_{cb} = 4.0 pF (Max)

PNP SILICON
AMPLIFIER TRANSISTORS



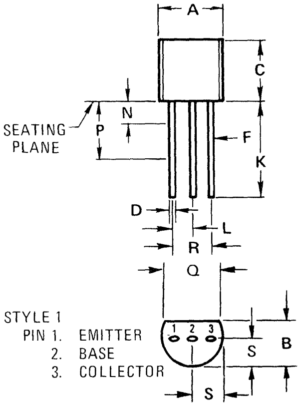
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.
(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

*ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_B = 0)		BV_{CEO}	50	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	50	-	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0) (V_{CB} = 35 Vdc, I_E = 0)		I_{CBO}	- -	10 50	nAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)		I_{EBO}	-	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 μAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)(1)	2N5086 2N5087 2N5086 2N5087 2N5086 2N5087	h_{FE}	150 250 150 250 150 250	500 800 - - - -	-
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)		$V_{CE(sat)}$	-	0.3	Vdc
Base-Emitter On Voltage (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc		$V_{BE(on)}$	-	0.85	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain - Bandwidth Product (I_C = 500 μAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)		f_T	40	-	MHz
Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 100 kHz)		C_{cb}	-	4.0	pF
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	2N5086 2N5087	h_{fe}	150 250	600 900	-
Noise Figure (I_C = 20 μAdc, V_{CE} = 5.0 Vdc, R_S = 10 k ohms, f = 10 Hz to 15.7 kHz) (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 3.0 k ohms, f = 1.0 kHz)	2N5086 2N5087 2N5086 2N5087	NF,	- - - -	3.0 2.0 3.0 2.0	dB

* Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

NOISE FIGURE

V_{CE} = 5.0 Vdc, T_A = 25

FIGURE 1 — FREQUENCY EFFECTS

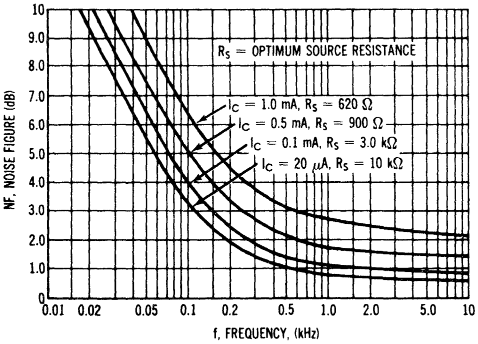


FIGURE 2 — SOURCE RESISTANCE EFFECTS

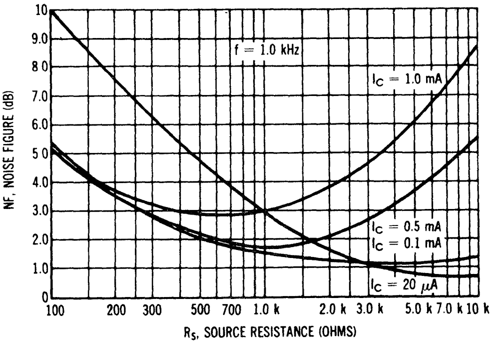


FIGURE 3 — DC CURRENT-GAIN

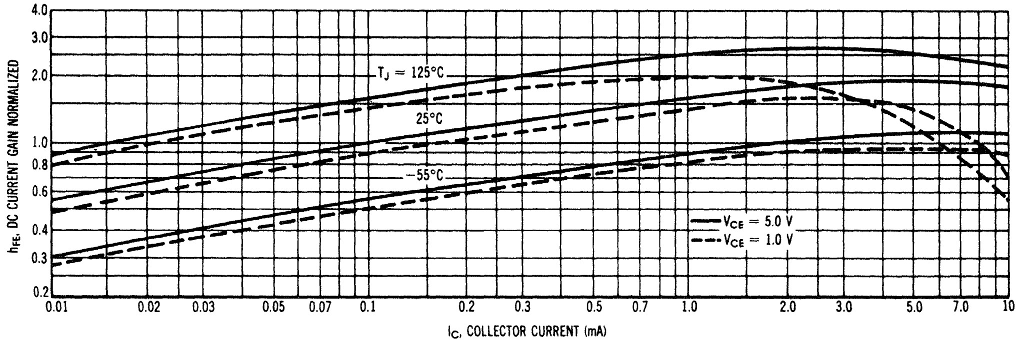


FIGURE 4 — COLLECTOR SATURATION REGION

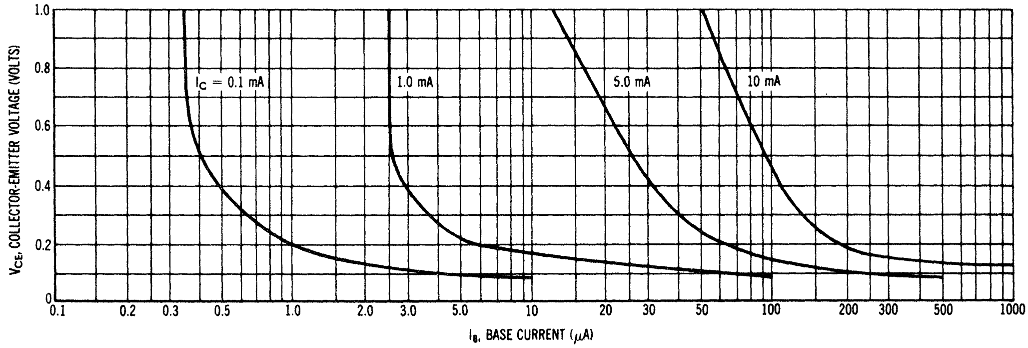


FIGURE 5 — CURRENT GAIN — BANDWIDTH PRODUCT

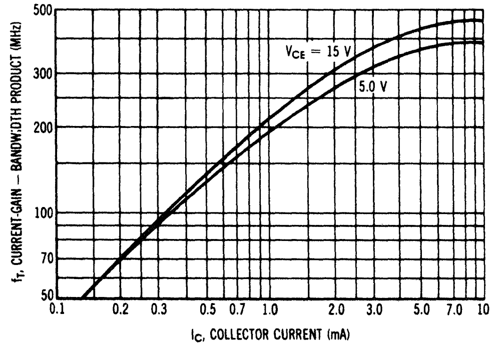
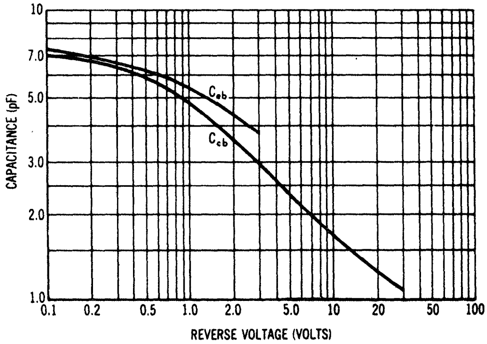


FIGURE 6 — CAPACITANCES



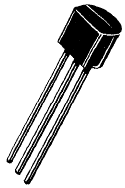
2N5088 (SILICON)
2N5089

NPN SILICON ANNULAR TRANSISTORS

. . . NPN silicon annular transistors designed for low-level, low- noise amplifier applications.

- High Gain at Low Current —
  2N5088 — 300 min at 100 μAdc
  2N5089 — 400 min at 100 μAdc
- Low 100 μAdc Noise Figure —
  1.2 dB typ at 100 Hz
  1.0 dB typ at 1.0 kHz
- Excellent Gain Linearity from 20 μAdc to 2.0 mAdc
  (See Figure 9)

NPN SILICON AMPLIFIER TRANSISTORS



*MAXIMUM RATINGS

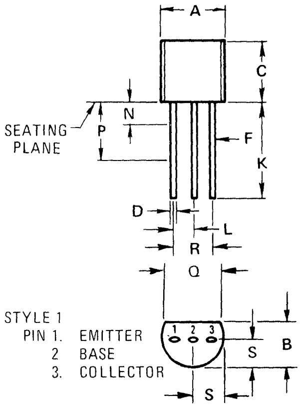
Rating	Symbol	2N5088	2N5089	Unit
Collector-Emitter Voltage	V_{CEO}	30	25	Vdc
Collector-Base Voltage	V_{CB}	35	30	Vdc
Emitter-Base Voltage	V_{EB}	4.5		Vdc
Collector Current — Continuous	I_C	50		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8		mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

2N5088, 2N5089 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_B = 0)	2N5088 2N5089	BV_{CEO}	30 25	- -	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	2N5088 2N5089	BV_{CBO}	35 30	- -	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0) (V_{CB} = 15 Vdc, I_E = 0)	2N5088 2N5089	I_{CBO}	- -	50 50	nAdc
Emitter Cutoff Current ($V_{EB(off)}$ = 3.0 Vdc, I_C = 0) ($V_{EB(off)}$ = 4.5 Vdc, I_C = 0)		I_{EBO}	- -	50 100	nAdc
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 100 μAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)(1)	2N5088 2N5089 2N5088 2N5089 2N5088 2N5089	h_{FE}	300 400 350 450 300 400	900 1200 - - - -	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)		$V_{CE(sat)}$	-	0.5	Vdc
Base-Emitter On Voltage (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)(1)		$V_{BE(on)}$	-	0.8	Vdc
DYNAMIC CHARACTERISTICS					
*Current-Gain – Bandwidth Product (I_C = 500 μAdc, V_{CE} = 5.0 Vdc, f = 20 MHz		f_T	50	-	MHz
*Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 100 kHz)		C_{cb}	-	4.0	pF
Emitter-Base Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)		C_{eb}	-	10	pF
*Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	2N5088 2N5089	h_{fe}	350 450	1400 1800	-
*Noise Figure (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 10 k ohms, f = 10 Hz to 15.7 kHz	2N5088 2N5089	NF	- -	3.0 2.0	dB

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

NOISE FIGURE

V_{CE} = 5.0 Vdc, T_A = 25 °C

FIGURE 1 – FREQUENCY EFFECTS

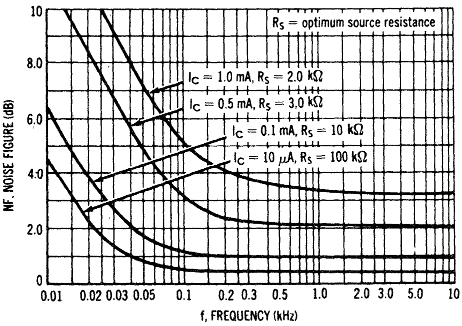


FIGURE 2 – SOURCE RESISTANCE EFFECTS

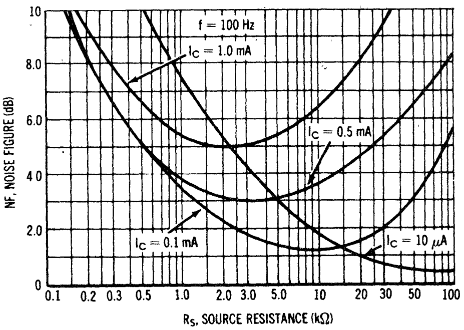


FIGURE 3 – DC CURRENT GAIN

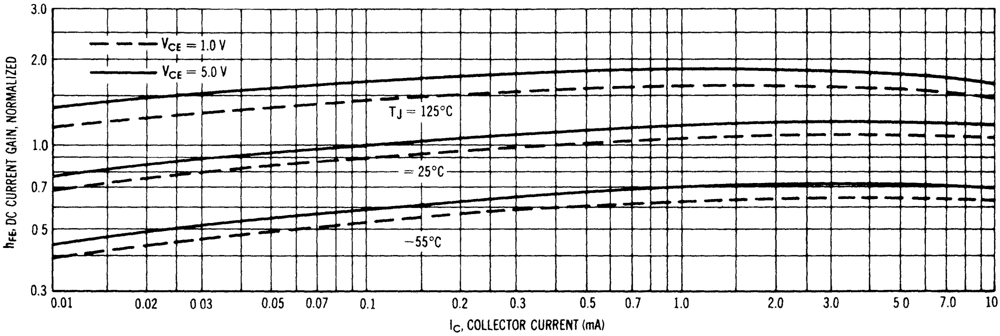


FIGURE 4 – COLLECTOR SATURATION REGION

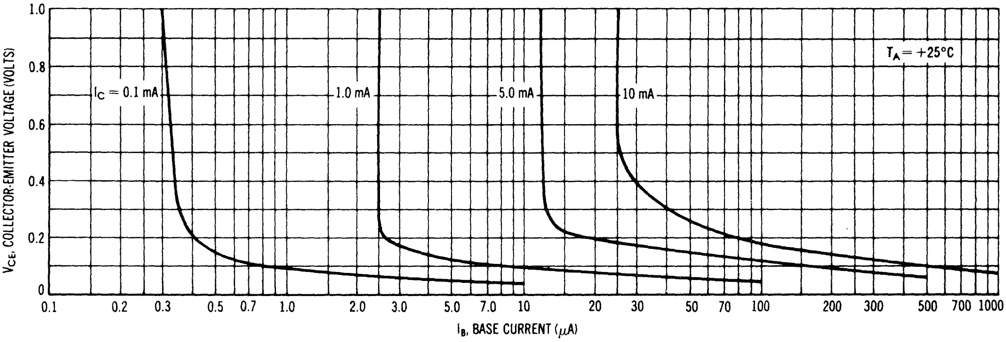


FIGURE 5 – CURRENT-GAIN–BANDWIDTH PRODUCT

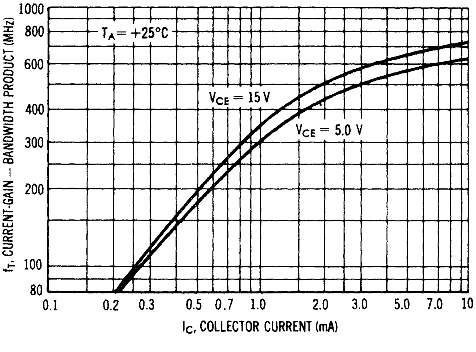
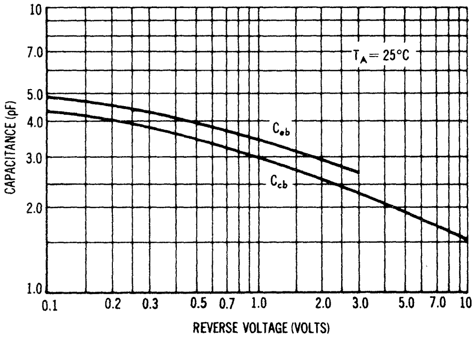


FIGURE 6 – CAPACITANCE



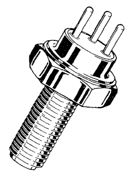
2N5090 (SILICON)

NPN SILICON RF POWER TRANSISTOR

. . . designed for amplifier, frequency-multiplier or oscillator circuits in Military or Industrial equipment. Suitable for use as output, driver or pre-driver stages in VHF and UHF equipment.

- 1.2 Watts Output Minimum at 400 MHz (7.8 dB Gain)
- 2.0 Watts Output Typical at 150 MHz (13 dB Gain)
- Multiple-Emitter Overlay Construction for Excellent High-Frequency Performance

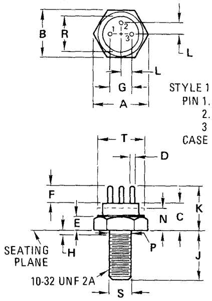
NPN SILICON
RF POWER
TRANSISTOR



*MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	55	Vdc
Emitter-Base Voltage	V_{EB}	3.5	Vdc
Collector Current - Continuous	I_C	0.4	Adc
Total Device Dissipation @ $T_C = 75^\circ C$ Derate above 75°C	P_D	5.0 0.04	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



STYLE 1
PIN 1. EMITTER
2. BASE
3 COLLECTOR
CASE ISOLATED

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.57	13.08	0.495	0.515
B	10.77	11.10	0.424	0.437
C	5.46	8.13	0.215	0.320
D	0.762	1.17	0.030	0.046
E	2.29	3.43	0.090	0.135
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	9.53	11.56	0.375	0.455
K	9.02	12.19	0.355	0.480
L	2.29	2.79	0.090	0.110
N	–	4.19	–	0.165
P	4.14	4.80	0.163	0.189
R	8.13	9.14	0.320	0.360
T	9.14	11.10	0.360	0.437

All JEDEC dimensions and notes apply

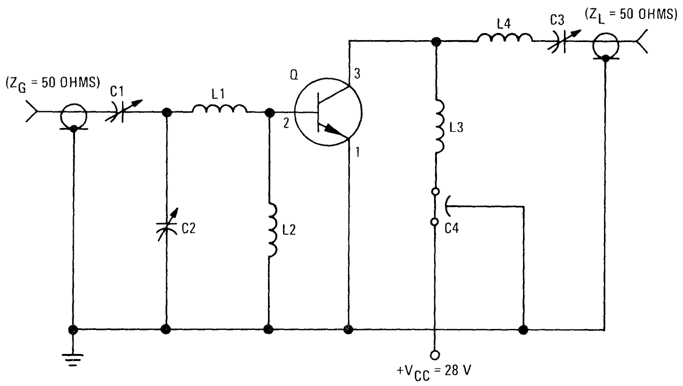
CASE 36
TO-60

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	–	Vdc
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, R_{BE} = 10 Ohms)	$V_{CER(sus)}$	55	–	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, I_B = 0)	I_{CEO}	–	20	µAdc
Collector Cutoff Current (V_{CE} = 55 Vdc, V_{BE} = -1.5 Vdc) (V_{CE} = 30 Vdc, V_{BE} = -1.5 Vdc, T_C = 200°C)	I_{CEX}	 – –	 0.1 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 3.5 Vdc, I_C = 0)	I_{EBO}	–	0.1	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc) (I_C = 360 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	 10 5.0	 200 –	–
Collector-Emitter Saturation Voltage (I_C = 0.1 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	500	–	MHz
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	3.5	pF
FUNCTIONAL TEST				
Power Input (Figure 1) (P_{out} = 1.2 Watts, R_L = 50 Ohms, f = 400 MHz)	P_{in}	–	0.2	Watt
Collector Efficiency (Figure 1) (P_{out} = 1.2 Watts, R_L = 50 Ohms, f = 400 MHz)	η	45	–	%

*Indicates JEDEC Registered Data.

FIGURE 1 – 400 MHz TEST CIRCUIT



C1 = 0.9–7.0 pF, ARCO 400 or equivalent
C2 = 1.5–20 pF, ARCO 402 or equivalent
C3 = 1.5–20 pF, ARCO 402 or equivalent
C4 = 1000 pF
L1 = 2 turns No. 18 AWG wire, 1/4″ ID, 1/8″ Long
L2 = RF Choke, 0.1 µH
L3 = 2 turns No. 18 AWG wire, 1/8″ ID, 1/8″ Long
L4 = 3 turns No. 16 AWG wire, 1/4″ ID, 3/8″ Long

FIGURE 2 – POWER OUTPUT versus FREQUENCY

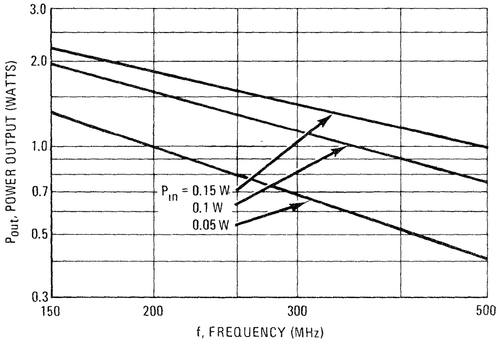


FIGURE 3 – POWER OUTPUT versus POWER INPUT

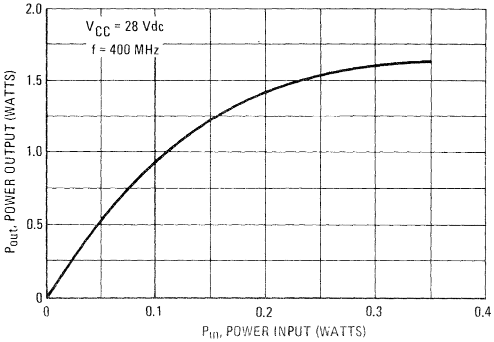


FIGURE 4 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

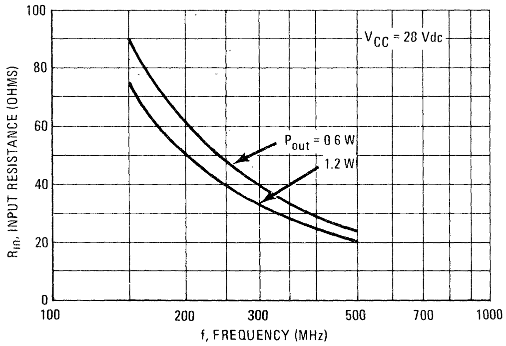


FIGURE 5 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

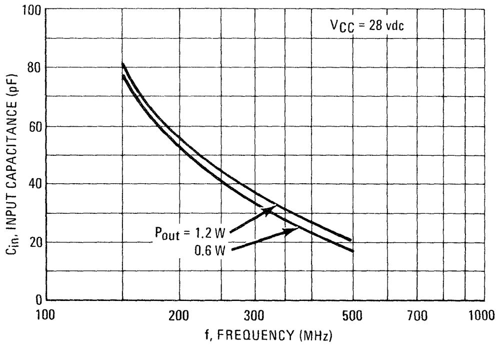
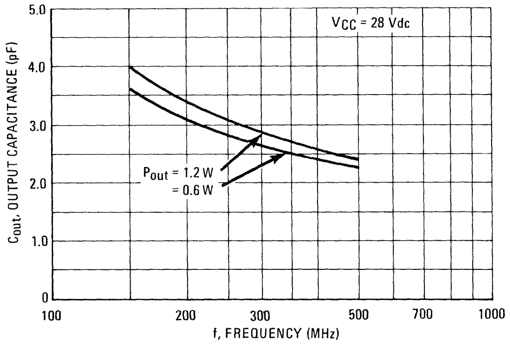


FIGURE 6 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY



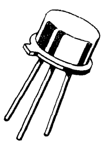
2N5108 (SILICON)

NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed for amplifier, frequency multiplier, or oscillator applications in military and industrial equipment. Suitable for use as output, driver, or pre-driver stages in UHF equipment and as a fundamental frequency oscillator at 1.68 GHz.

- High Power Output – P_{out} = 1.0 W (Min) @ f = 1.0 GHz
- High Current-Gain–Bandwidth Product – f_T = 1200 MHz (Min) @ I_C = 50 mAdc
- Ideal for Radio Sonde Applications – P_{out} (oscillator) = 300 mW (Typ) @ f = 1.68 GHz

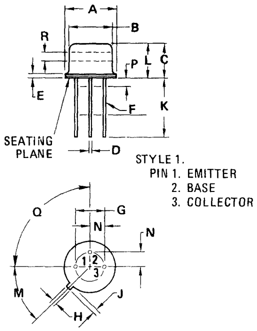
NPN SILICON AMPLIFIER TRANSISTOR



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
*Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	55	Vdc
*Collector-Base Voltage	V_{CB}	55	Vdc
*Emitter-Base Voltage	V_{EB}	3.0	Vdc
*Collector Current – Continuous	I_C	0.4	Adc
*Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.5 0.02	Watts W/°C
*Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



STYLE 1.
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

CASE 79-02

Note: All JEDEC notes and dimensions apply.

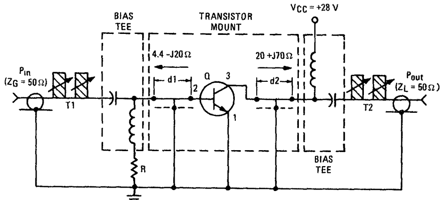
TO-39

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, R_{BE} = 10 ohms)	$V_{CER(sus)}$	55	–	–	Vdc
*Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	BV_{EBO}	3.0	–	–	Vdc
*Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	–	–	20	μAdc
*Collector Cutoff Current (V_{CE} = 50 Vdc, V_{BE} = 0) (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 150°C)	I_{CES}	 – –	 – –	 1.0 10	 μAdc mAdc
DYNAMIC CHARACTERISTICS					
*Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	1200	–	–	MHz
*Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	1.3	3.0	pF
FUNCTIONAL TEST					
*Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 1.0 W, V_{CC} = 28 Vdc, I_C = 102 mAdc, f = 1.0 GHz)	G_{PE}	5.0	–	–	dB
Power Output (Figure 1) (P_{in} = 316 mW, V_{CE} = 28 Vdc, f = 1.0 GHz)	P_{out}	1.0	–	–	Watt
*Collector Efficiency (P_{in} = 316 mW, V_{CE} = 28 Vdc, f = 1.0 GHz)	η	35	–	–	%
Power Output (Oscillator) (Figure 2) (V_{CE} = 20 Vdc, V_{EB} = 1.5 Vdc, f = 1.68 GHz) (Minimum Efficiency = 15%)	P_{out}	–	0.3	–	Watt

***Indicates JEDEC Registered Data.**

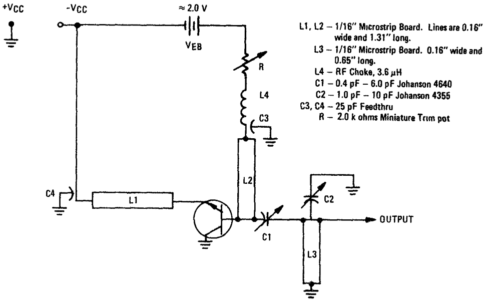
FIGURE 1 — 1 GHz RF AMPLIFIER POWER OUTPUT TEST CIRCUIT



d1.	1" Input line, center conductor width = 0.280"
d2	1" Output line, center conductor width = 0.125"
Q	2N5108
R	3 9 ohms
T1, T2	Microlab Double Stub Tuner, or Equivalent
Bias Tee.	Microlab 08N, or Equivalent
Transistor Mount	1/32" Microstrip board

Note. Impedance measurements are made at transistor socket pins.

FIGURE 2 — 1.68 GHz RF OSCILLATOR POWER OUTPUT TEST CIRCUIT



L1, L2 – 1/16" Microstrip Board. Lines are 0.16" wide and 1.31" long.
L3 – 1/16" Microstrip Board. 0.16" wide and 0.65" long.
L4 – RF Choke, 3.6 μH
C1 – 0.4 pF – 6.0 pF Johanson 4640
C2 – 1.0 pF – 10 pF Johanson 4355
C3, C4 – 25 pF Feedthru
R – 2.0 k ohms Miniature Trim pot

FIGURE 3 – POWER OUTPUT versus POWER INPUT

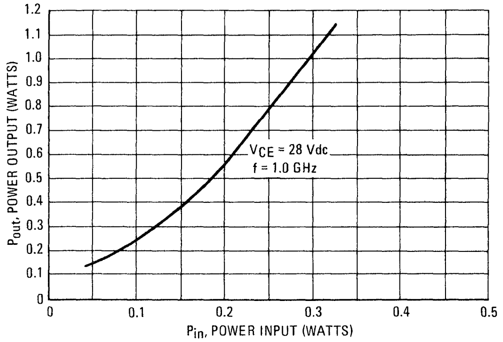


FIGURE 4 – POWER OUTPUT versus FREQUENCY

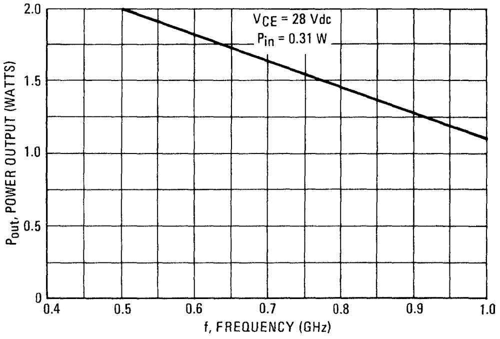


FIGURE 5 – POWER OUTPUT versus COLLECTOR-EMITTER VOLTAGE

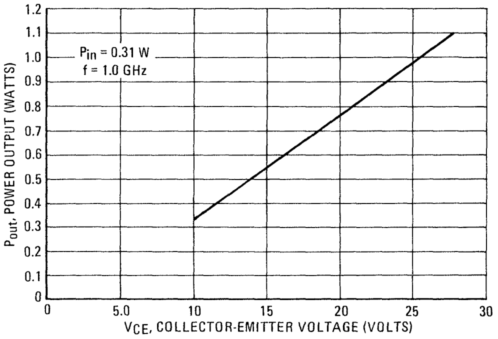


FIGURE 6 – OSCILLATOR POWER OUTPUT versus COLLECTOR CURRENT

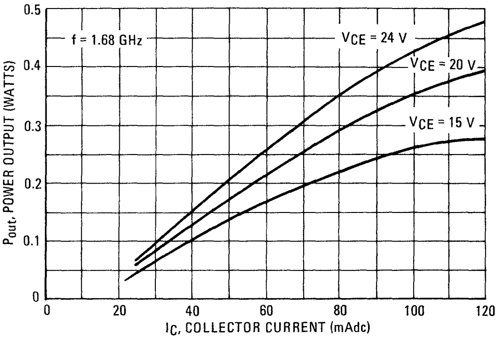


FIGURE 7—CURRENT-GAIN—BANDWIDTH PRODUCT versus CURRENT

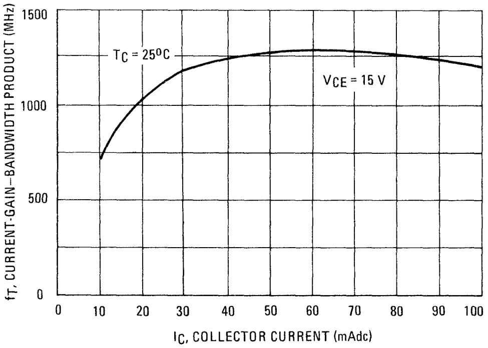
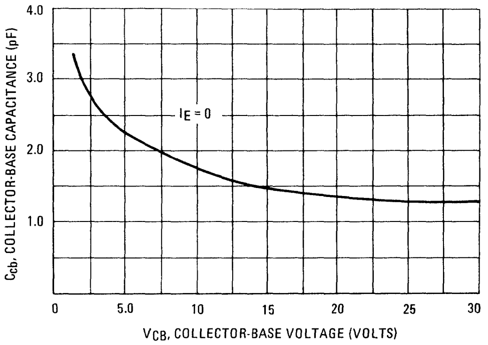


FIGURE 8—COLLECTOR BASE CAPACITANCE versus VOLTAGE



The RF Line

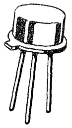
NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed specifically for broadband applications requiring low cross-modulation distortion and low-noise figure. Characterized for use in CATV amplifiers.

- Low Noise Figure — @ f = 200 MHz
  NF = 3.0 dB (Typ)
- High Current-Gain — Bandwidth Product —
  f_T = 1200 MHz (Min) @ I_C = 50 mAdc

WIDE BAND AMPLIFIER

NPN SILICON
HIGH-FREQUENCY
TRANSISTOR

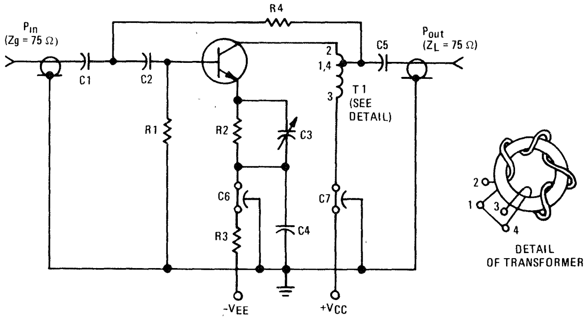


*MAXIMUM RATINGS

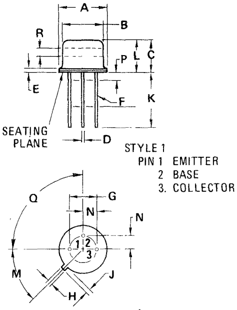
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Base Current — Continuous	I_B	400	mAdc
Collector Current — Continuous	I_C	400	mAdc
Total Device Dissipation @ T_C = 75°C (1) Derate above 25°C	P_D	2.5 20	Watt mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

(1) Total Device Dissipation at T_A = 25°C is 1.0 Watt.
* Indicates JEDEC Registered Data.

FIGURE 1 — VOLTAGE GAIN TEST CIRCUIT



C1, C2, C5 0.002 μF
C3 8 – 60 pF, ARCO 404 or Equivalent
C4 0.03 μF
C6, C7 1,500 pF
R1 390 OHMS, 1/2 WATT
R2 6.8 OHMS, 1/2 WATT
R3 330 OHMS, 1 WATT
R4 270 OHMS, 1/2 WATT
T_1 4 turns, Bifilar winding, 3/16" I.D., #30 AWG CORE MATERIAL: Indiana General CF 102-Q1



STYLE 1
PIN 1 EMITTER
2 BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0 350	0 370
B	8 00	8.51	0.315	0.335
C	6 10	6.60	0.240	0.260
D	0.406	0 533	0.016	0.021
E	0 229	3.18	0 009	0 125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0 210
H	0 711	0 864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

Note. All JEDEC notes and dimensions apply

CASE 79-02
TO-39

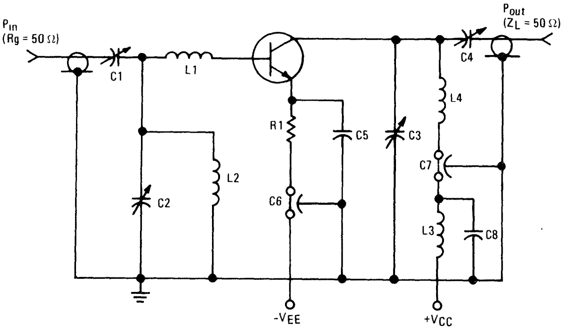
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO\ (sus)}$	20	–	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 5.0 mAdc, R_{BE} = 10 Ω)	$V_{CER\ (sus)}$	40	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	–	–	20	μAdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = −1.5 V, T_C = 150°C)	I_{CEX}	–	–	5.0	mAdc
(V_{CE} = 35 Vdc, V_{BE} = −1.5 V)		–	–	5.0	mAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc
***ON CHARACTERISTICS**					
DC Current Gain	h_{FE}				
(I_C = 360 mAdc, V_{CE} = 5.0 Vdc)		5.0	–	–	–
(I_C = 50 mAdc, V_{CE} = 15 Vdc)		40	–	120	–
DYNAMIC CHARACTERISTICS					
*Current-Gain – Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	1200	–	–	MHz
*Collector-Base Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	1.8	3.5	pF
Noise Figure (I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 200 MHz) (Figure 2)	NF	–	3.0	–	dB
FUNCTIONAL TEST					
*Common-Emitter Amplifier Voltage Gain (Figure 1) (I_C = 50 mAdc, V_{CC} = 15 Vdc, f = 50 to 216 MHz)	G_{ve}	11	–	–	dB
Cross-Modulation Distortion (Figure 3) (I_C = 50 mAdc, V_{CE} = 15 Vdc, V_{out} = 54 dBmV)	XM	–	-70	–	dB
*Power Input (Figure 2) (I_C = 50 mAdc, V_{CC} = 15 Vdc, R_S = 50 ohms, P_{out} = 1.26 mW, f = 200 MHz)	P_{in}	–	–	0.1	mW

*Indicates JEDEC Registered Data.

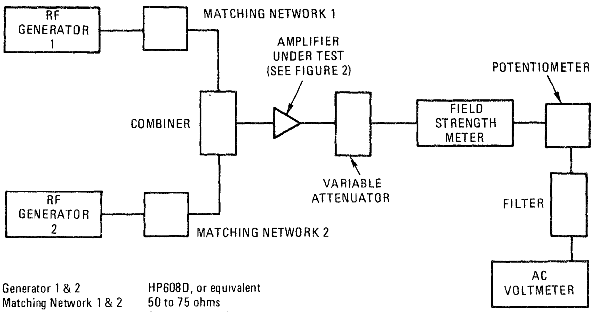
(1) Pulsed thru a 25 mH Inductor; 50% Duty Cycle

FIGURE 2 – 200 MHz POWER GAIN TEST CIRCUIT



C1, C2, C3	10 – 30 pF	L1	4-1/2 turns, No 22 wire, 3/16″ I.D
C4	10 – 20 pF	L4	3-1/2 turns, No. 22 wire, 3/16″ I.D.
C5	10,000 pF	L2, L3	0.82 μH RFC
C6, C7	1,000 pF	R1	240 OHMS, 2 WATTS
C8	0.01 μF		

FIGURE 3 – CROSS MODULATION TEST SETUP



Generator 1 & 2	HP608D, or equivalent
Matching Network 1 & 2	50 to 75 ohms
Combiner	20 dB isolation between generators
Variable Attenuator	As required
Field Strength Meter, with Detector Output	50 – 220 MHz
Filter	1000 Hz
AC Voltmeter	Ballantine 861, or equivalent

OPERATING INSTRUCTIONS FOR CROSS MODULATION TEST

1. Set up equipment as shown in Fig. 3
2. Set generator 1 to 150 MHz modulated 30% by 1,000 hertz, and tune field strength meter to 150 MHz.
3. Adjust output level of generator 1 to give rated output from the amplifier under test.
4. Adjust potentiometer and AC voltmeter for a convenient level. This level then corresponds to 100% cross modulation.
5. Remove modulation. Readjust output level of generator 1 if necessary to obtain the AC voltmeter "100% level". Do not readjust generator 1 during the following steps.
6. Set generator 2 to 210 MHz modulated 30% by 1,000 hertz and tune field strength meter to 210 MHz.
7. Adjust output level of generator 2 to give rated output of the amplifier, i e The AC voltmeter indicates the "100% level".
8. Tune field strength meter to 150 MHz CW and read the AC voltmeter (a change of the AC voltmeter scale may be necessary).
9. Calculate percentage of cross modulation by comparing the reading of step 8 to the "100% level"

FIGURE 4 – CURRENT-GAIN – BANDWIDTH PRODUCT

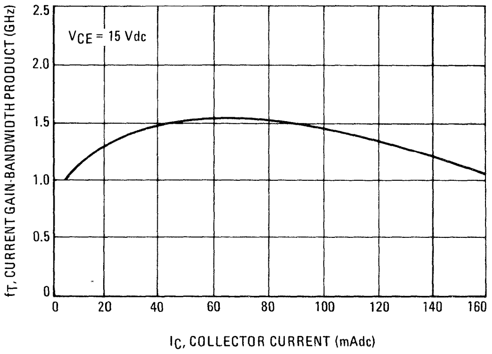


FIGURE 5 – COLLECTOR-BASE TIME CONSTANT

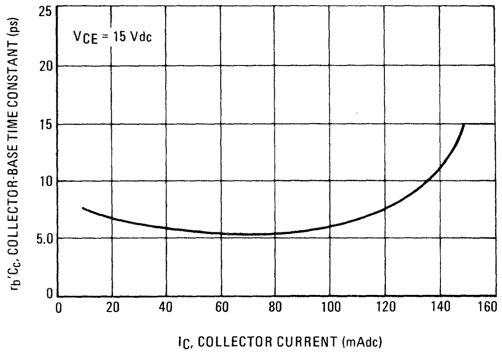


FIGURE 6 – SATURATION VOLTAGES

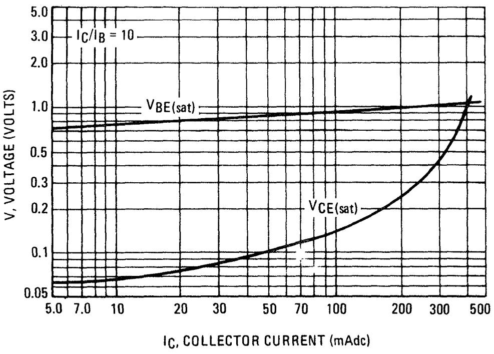


FIGURE 7 – CAPACITANCES versus REVERSE VOLTAGE

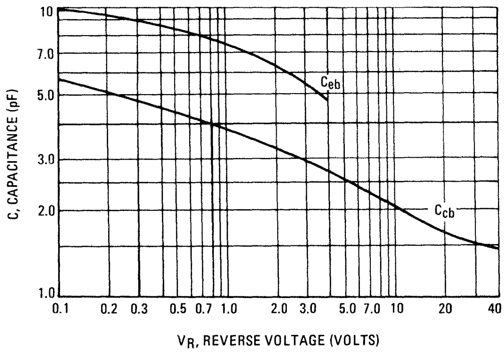


FIGURE 8 – INPUT ADMITTANCE versus FREQUENCY

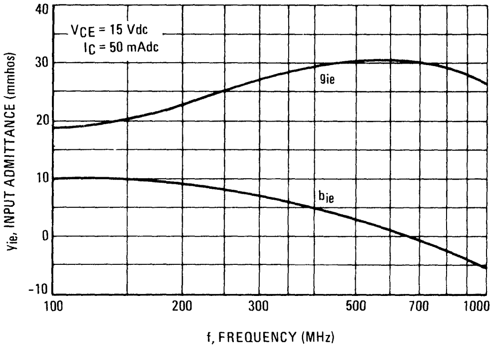


FIGURE 9 – INPUT ADMITTANCE versus COLLECTOR CURRENT

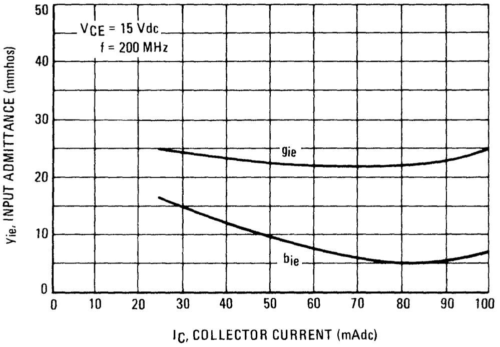


FIGURE 10 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY

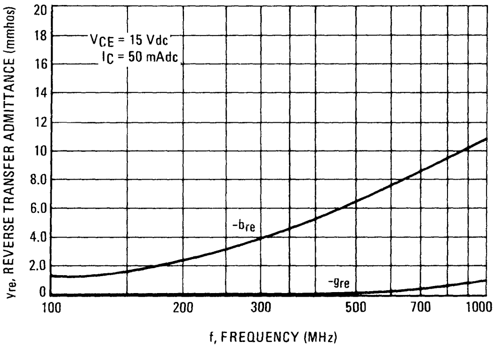


FIGURE 11 – REVERSE TRANSFER ADMITTANCE versus COLLECTOR CURRENT

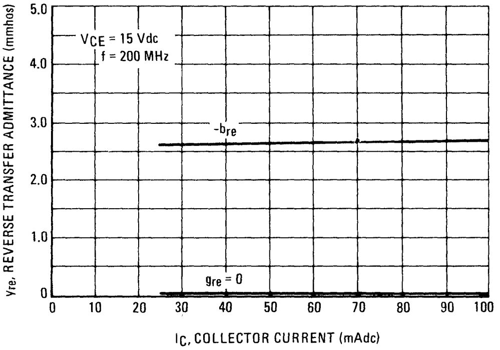


FIGURE 12 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

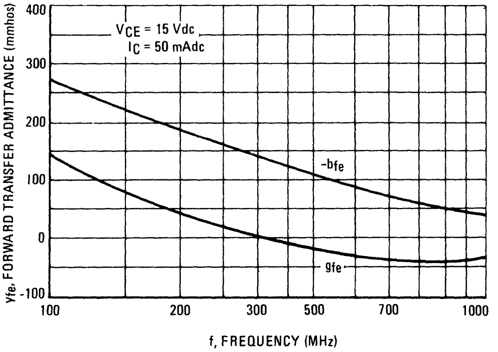


FIGURE 13 – FORWARD TRANSFER ADMITTANCE versus COLLECTOR CURRENT

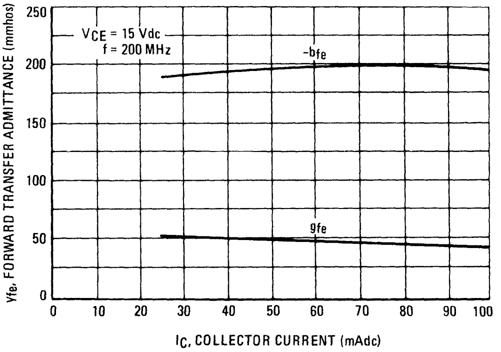


FIGURE 14 – OUTPUT ADMITTANCE versus FREQUENCY

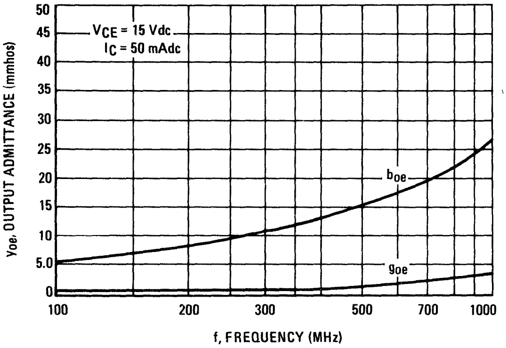


FIGURE 15 – OUTPUT ADMITTANCE versus COLLECTOR CURRENT

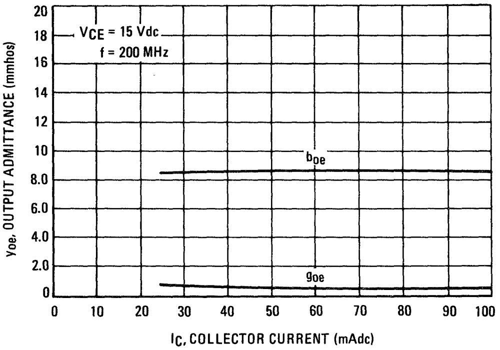


FIGURE 16 – INPUT REFLECTION COEFFICIENT versus FREQUENCY

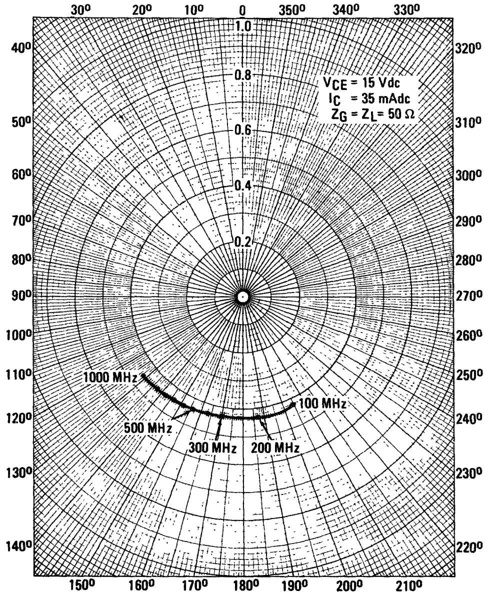


FIGURE 17 – OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

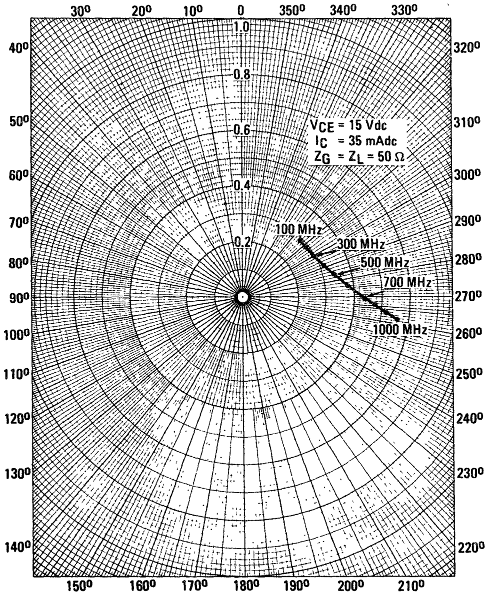


FIGURE 18 – REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY

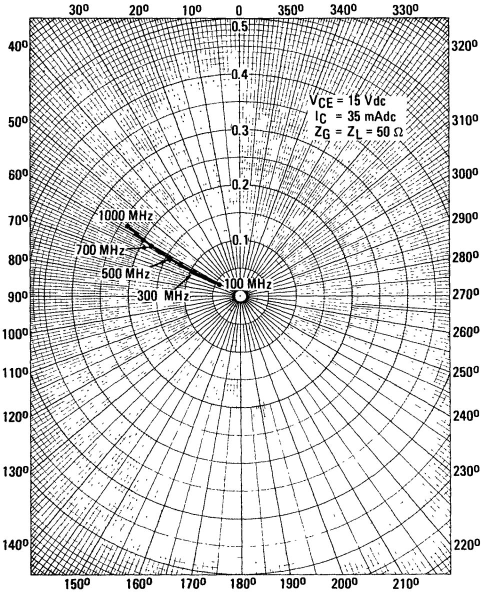


FIGURE 19 – FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY

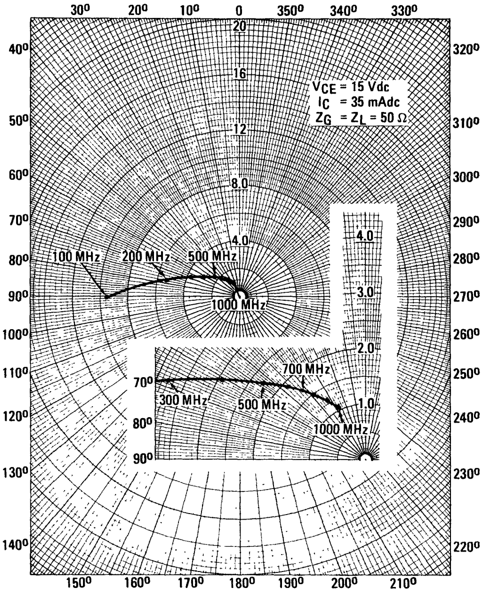
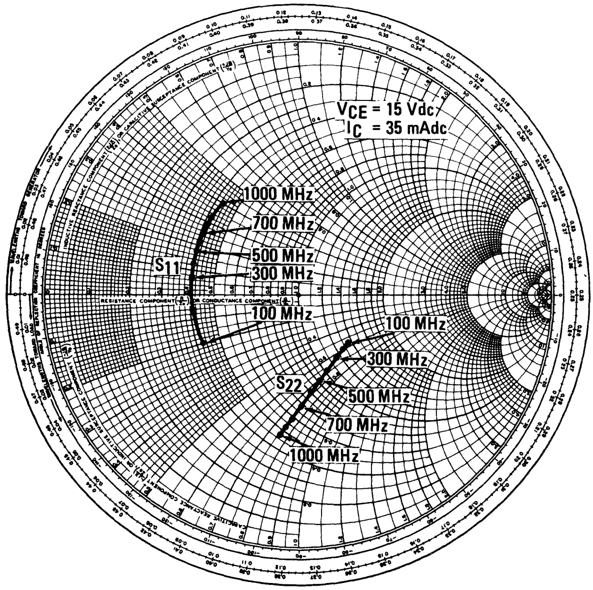


FIGURE 20 – INPUT REFLECTION COEFFICIENT AND OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

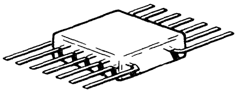


PNP SILICON ANNULAR MULTIPLE TRANSISTORS

. . . designed for use in high current, high speed switching applications.

- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)} = 1.0$ Vdc (Max) @ $I_C = 1.0$ Adc
- DC Current Gain Specified — 20 (Min) @ $I_C = 1.0$ Adc
- High Current-Gain—Bandwidth Product —
  $f_T = 150$ MHz (Min) @ $I_C = 50$ mAdc
- Fast Turn-On Time
  $t_{on} = 40$ ns, $t_{off} = 110$ ns

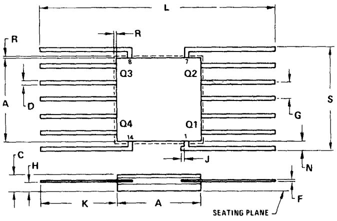
PNP SILICON
MULTIPLE TRANSISTORS



*MAXIMUM RATINGS

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	40		Vdc
Collector-Base Voltage	V_{CB}	40		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	1.5		Adc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
		One Die	All Die Equal Power	
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	400 2.28	600 3.42	mW mW/°C
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	0.9 5.13	3.6 20.5	Watts mW/°C

*Indicates JEDEC Registered Data.



STYLE 1
PIN 1 COLLECTOR
2 BASE
3 EMITTER
4 NOT CONNECTED
5 EMITTER
6 BASE
7 COLLECTOR
8 COLLECTOR
9 BASE
10 EMITTER
11 NOT CONNECTED
12 EMITTER
13 BASE
14 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.99	0.240	0.275
C	0.76	2.03	0.030	0.080
D	0.25	0.48	0.010	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
J	–	0.38	–	0.015
K	6.35	–	0.250	–
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330

CASE 607-04

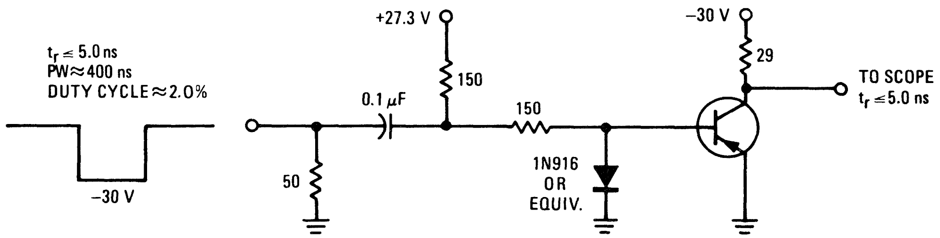
*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	40	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc)	I_{CEV}	-	100	nAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	-	100	nAdc
Base Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc)	I_{BEV}	-	200	nAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	20	-	-
Collector-Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	-	1.0	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	-	1.4	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	150	-	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	-	20	pF
Emitter-Base Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	-	80	pF
SWITCHING CHARACTERISTICS (See Figure 1)				
Delay Time (V_{CC} = 30 Vdc, $V_{BE(off)}$ = 0.5 Vdc, I_C = 1.0 Adc, I_{B1} = 0.1 Adc)	t_d	-	10	ns
Rise Time	t_r	-	30	ns
Storage Time (V_{CC} = 30 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)	t_s	-	80	ns
Fall Time	t_f	-	30	ns

* Indicates JEDEC Registered Data

(1) **Pulse test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%**

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



2N5155 (GERMANIUM)

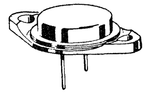
PNP GERMANIUM POWER TRANSISTORS

. . . designed for high-current switching applications requiring low saturation voltages, fast switching times and above average Collector-Emitter Sustaining capability.

- Alloy Diffused Epitaxial Construction
- Low Saturation Voltages –
  $V_{CE(sat)}$ = 0.9 Vdc (Max) @ I_C = 25 Adc
  $V_{BE(sat)}$ = 1.4 Vdc (Max) @ I_C = 25 Adc
- DC Current Gain –
  h_{FE} = 25 (Min) @ I_C = 8.0 Adc

25 AMPERE
PNP ADE GERMANIUM
POWER TRANSISTOR

140 VOLTS
106 WATTS



*MAXIMUM RATINGS

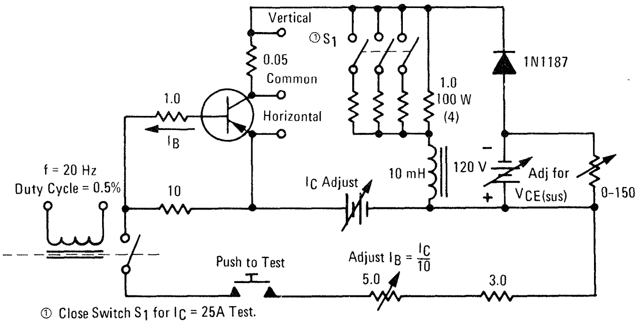
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	120	Vdc
Collector-Base Voltage	V_{CB}	140	Vdc
Emitter-Base Voltage	V_{EB}	1.5	Vdc
Collector Current - Continuous ** - Continuous - Peak	I_C	15 25 25	Adc
Base Current - Continuous	I_B	5.0	Adc
**Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	106 1.25	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +110	°C

THERMAL CHARACTERISTICS

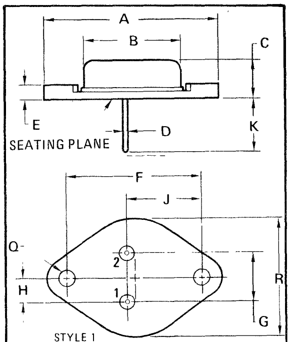
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.8	°C/W

*Indicates JEDEC Registered Data.
**Motorola guarantees this data in addition to the JEDEC Registered data shown.

FIGURE 1 – SUSTAINING VOLTAGE TEST CIRCUIT



① Close Switch S_1 for I_C = 25A Test.



STYLE 1
PIN 1 BASE
2 EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	–	7.62	–	0.300
D	1.22	1.32	0.048	0.052
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	8.13	10.67	0.320	0.420
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
*Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	BV_{CEO}	120	-	Vdc
*Collector-Emitter Sustaining Voltage (See Figure 1) (I_C = 8.0 Adc, R_{EB} = 10 Ohms) (I_C = 25 Adc, R_{EB} = 10 Ohms)	$V_{CEO(sus)}$	120 80	- -	Vdc
*Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 0.2 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 0.2 Vdc, T_C = 85°C)	I_{CEX}	- -	10 25	mAdc
Collector Cutoff Current (V_{CB} = 2.0 Vdc, I_E = 0)	I_{CBO}	-	200	μAdc
*Emitter Cutoff Current (V_{EB} = 1.5 Vdc, I_C = 0)	I_{EBO}	-	500	mAdc
ON CHARACTERISTICS				
*DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	-
*Collector-Emitter Saturation Voltage (I_C = 25 Adc, I_B = 2.5 Adc)	$V_{CE(sat)}$	-	0.9	Vdc
*Base-Emitter Saturation Voltage (I_C = 25 Adc, I_B = 2.5 Adc)	$V_{BE(sat)}$	-	1.4	Vdc
Pulse Energy Test (Note 1) (See Figure 2) (I_C = 4.2 Adc, V_{CE} = 30 Vdc)	PET	1.26	-	Joule
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc, f = 50 kHz)	f_T	100	-	kHz

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Rise Time	(V_{CC} = -12 Vdc, I_C = 10 Adc, I_{B1} = 1.0 Adc, I_{B2} = 1.0 Adc) (See Figure 3)	t_r	-	18	μs
Storage Time		t_s	-	12	μs
Fall Time		t_f	-	18	μs

*Indicates JEDEC Registered Data.

Note 1: Pulse Test: Pulse Width = 10 ms, Duty Cycle = 2.5%.

FIGURE 2 – PULSE ENERGY TEST CIRCUIT

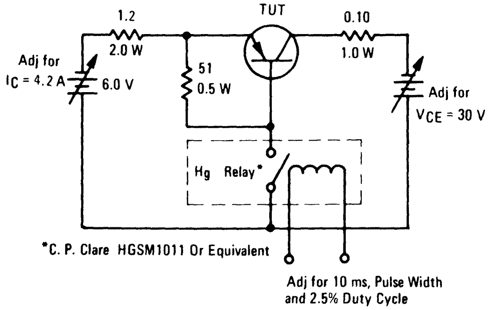
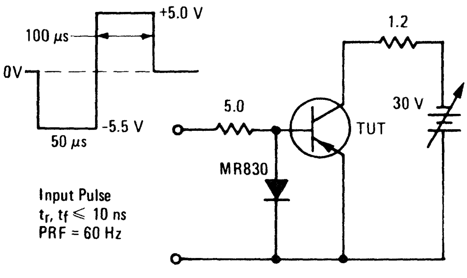


FIGURE 3 – SWITCHING TIME TEST CIRCUIT

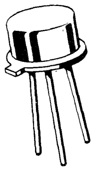


2N5157

For Specifications, See 2N3902 Data, Volume I.

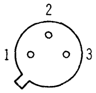
2N5160 (SILICON)

PNP silicon RF power transistors designed for amplifier, frequency multiplier or oscillator applications in military and industrial equipment. Suitable for use as Class A, B, or C output driver, or pre-driver stages in VHF and UHF.



CASE 79
(TO-39)

Collector connected to case



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	0.4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	-	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	BV_{EBO}	4.0	-	-	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, I_B = 0)	I_{CEO}	-	-	20	μAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, V_{BE} = 0)	I_{CES}	-	-	0.1	mAdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	-	-	1.0	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	-	-	-
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	500	900	-	MHz
Collector-Base Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{cb}	-	2.5	4.0	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CE} = 28 Vdc, P_{in} = 0.16 Watt, f = 400 MHz) (V_{CE} = 28 Vdc, P_{in} = 50 mW, f = 175 MHz)	G_{PE}	8.0 -	8.8 14.5	- -	dB
Power Output (V_{CE} = 28 Vdc, P_{in} = 0.16 Watt, f = 400 MHz) (V_{CE} = 28 Vdc, P_{in} = 50 mW, f = 175 MHz)	P_{out}	1.0 -	1.2 1.4	- -	Watt
Collector Efficiency (V_{CE} = 28 Vdc, P_{in} = 0.16 Watt, f = 400 MHz)	η	45	55	-	%

FIGURE 1 – 400-MHz TEST CIRCUIT

C_1 – 10 pF
C_2, C_3, C_4, C_5 – 1.0 – 10 pF variable
C_6 – 2400 pF feed through
C_7 – 0.004 μF

C_8 – 0.01 μF
L_1 – 30 nH, 1 turn, No. 20 AWG
L_2 – 75 nH, 3 turns, No. 20 AWG
L_3 – 0.33 μH, R.F.C.

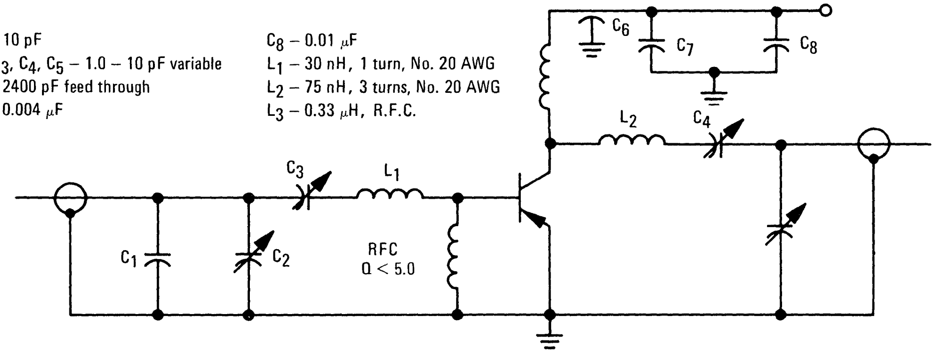


FIGURE 2 – POWER OUTPUT versus FREQUENCY

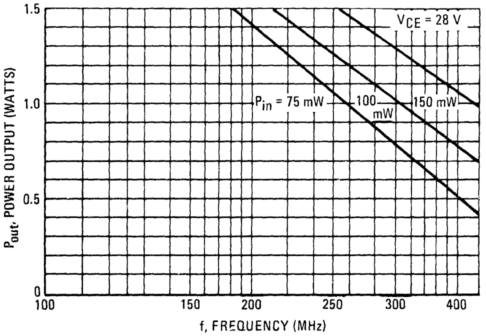


FIGURE 3 – POWER OUTPUT versus POWER INPUT

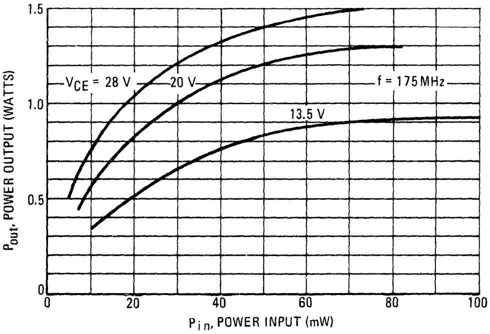


FIGURE 4 – PARALLEL INPUT IMPEDANCE versus FREQUENCY

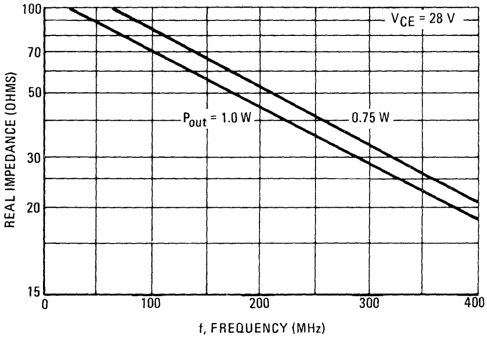


FIGURE 5 – PARALLEL INPUT IMPEDANCE versus FREQUENCY

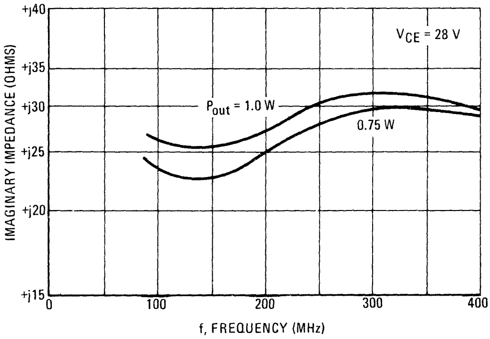


FIGURE 6 – PARALLEL OUTPUT CAPACITANCE versus FREQUENCY

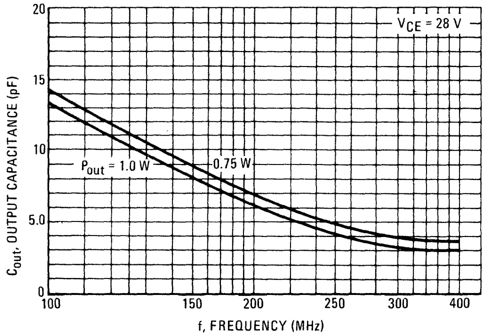


FIGURE 7 – CURRENT-GAIN–BANDWIDTH PRODUCT versus COLLECTOR CURRENT

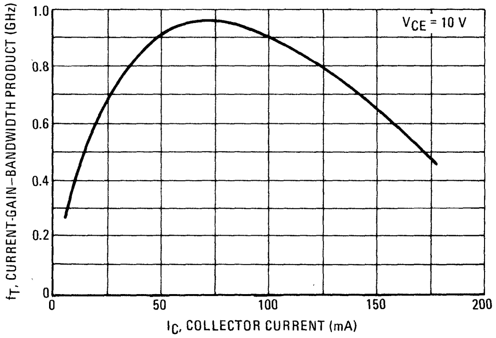


FIGURE 8 – 2N5160 300-MHz COMPLEMENTARY POWER OUTPUT CIRCUIT

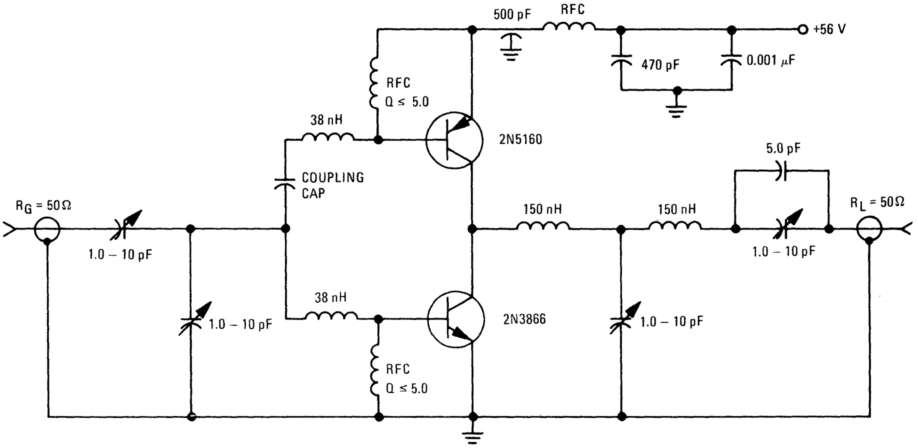
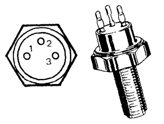


FIGURE 9 – COMPLEMENTARY CIRCUIT – POWER OUTPUT versus POWER INPUT

2N5161 (SILICON)
2N5162



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

CASE 36
(TO-60)

Case common to emitter

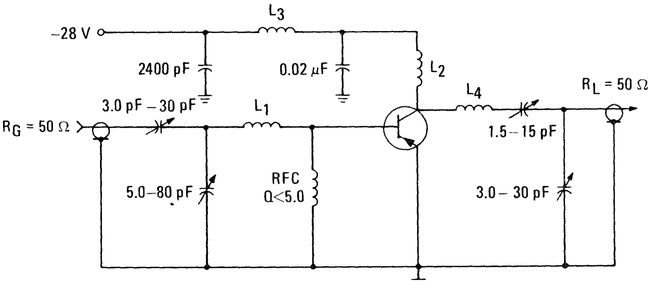
PNP silicon RF power transistors designed for amplifier or oscillator applications in military and industrial equipment. Suitable for use as Class B or C output or power oscillator in VHF applications

MAXIMUM RATINGS

Rating	Symbol	2N5161	2N5162	Unit
Collector-Emitter Voltage	V_{CEO}	40		Vdc
Collector-Base Voltage	V_{CB}	60		Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current	I_C	1.5	5.0	Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	20 0.114	50 0.286	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

FIGURE 1 – 175 MHz TEST CIRCUITS

1a – 2N5161

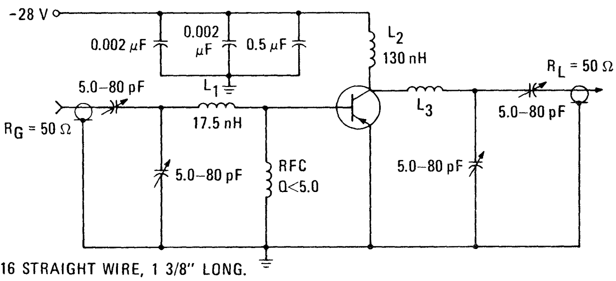


L_1 – 1 TURN, #18 AWG (21 nH)

L_2, L_3 – 0.33 µH RFC

L_4 – 4 TURNS, #16 AWG, ½" I.D. (200 nH)

1b – 2N5162



L_1 – #16 STRAIGHT WIRE, 1 3/8" LONG.

L_2 – 5 TURNS #20 AWG, 1/2" LONG.

L_3 – 1 TURN #18 AWG WIRE.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage* (I_C = 200 mAdc, I_B = 0)		$V_{CEO(sus)}$*	40	-	-	Vdc
Emitter-Base Breakdown Voltage		BV_{EBO}				Vdc
(I_E = 1.0 mAdc, I_C = 0)	2N5161		4.0	-	-	
(I_E = 5.0 mAdc, I_C = 0)	2N5162		4.0	-	-	
Collector Cutoff Current		I_{CES}				mAdc
(V_{CE} = 60 Vdc, V_{BE} = 0)	2N5161		-	-	0.5	
	2N5162		-	-	1.0	
(V_{CE} = 28 Vdc, V_{BE} = 0, T_C = 200°C)	2N5161		-	-	5.0	
	2N5162		-	-	10	
Collector Cutoff Current		I_{CBO}				mAdc
(V_{CB} = 28 Vdc, I_E = 0)	2N5161		-	-	0.1	
	2N5162		-	-	0.2	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				-
(I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	2N5161		10	-	-	
(I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	2N5162		10	-	-	
DYNAMIC CHARACTERISTICS						
Current-Gain-Bandwidth Product		f_T				MHz
(I_C = 200 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N5161		-	500	-	
(I_C = 500 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N5162		-	500	-	
Collector-Base Capacitance		C_{cb}				pF
(V_{CB} = 28 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	2N5161		-	10	15	
	2N5162		-	45	60	
FUNCTIONAL TEST						
Common-Emitter Amplifier Power Gain		G_{PE}				dB
(V_{CC} = 28 Vdc, P_{out} = 7.5 Watts, f = 175 MHz)	2N5161		8.75	10.3	-	
(V_{CC} = 28 Vdc, P_{out} = 30 Watts, f = 175 MHz)	2N5162		6.0	7.0	-	
Power Output		P_{out}				Watts
(V_{CC} = 28 Vdc, P_{in} = 1.0 Watt, f = 175 MHz)	2N5161		7.5	8.5	-	
(V_{CC} = 28 Vdc, P_{in} = 7.5 Watts, f = 175 MHz)	2N5162		30	35	-	
Collector Efficiency		η				%
(V_{CC} = 28 Vdc, P_{out} = 7.5 Watts, f = 175 MHz)	2N5161		45	-	-	
(V_{CC} = 28 Vdc, P_{out} = 30 Watts, f = 175 MHz)	2N5162		55	-	-	

* Pulsed through 25 mH inductor

2N5161 DESIGN DATA

FIGURE 2 — POWER OUTPUT versus FREQUENCY

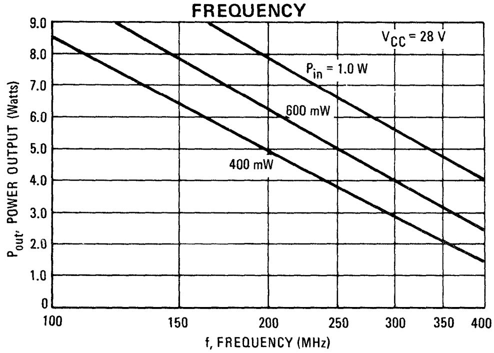
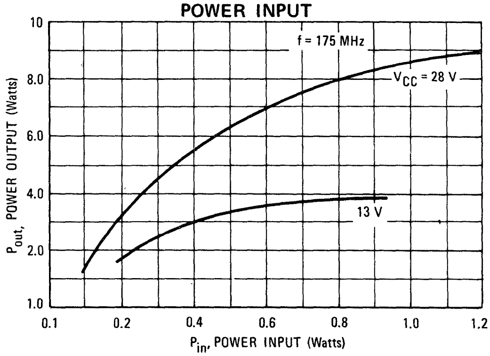


FIGURE 3 — POWER OUTPUT versus POWER INPUT



LARGE SIGNAL IMPEDANCE DATA

FIGURE 4 – REAL SERIES INPUT RESISTANCE versus FREQUENCY

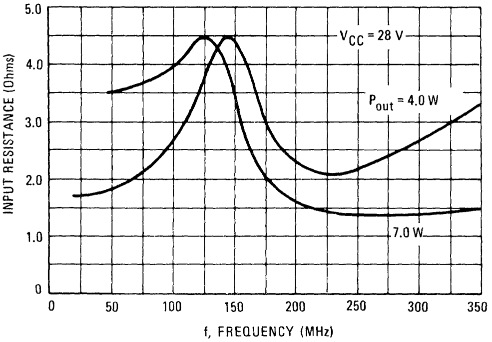


FIGURE 5 – IMAGINARY SERIES INPUT REACTANCE versus FREQUENCY

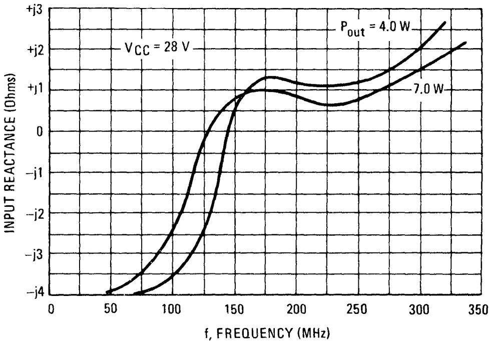
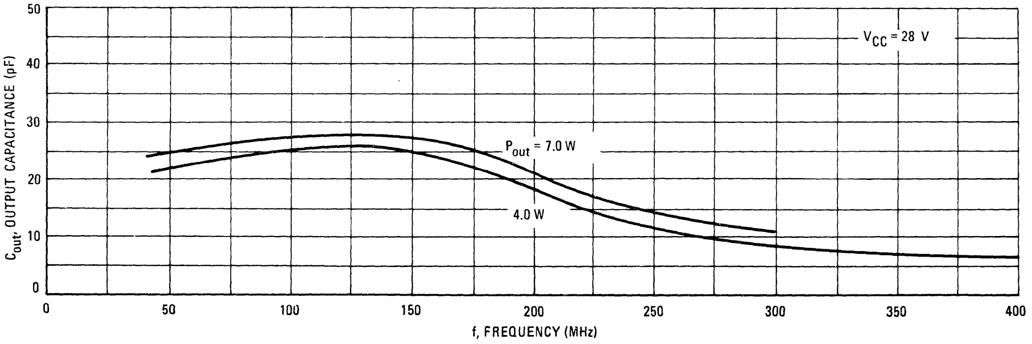


FIGURE 6 – OUTPUT CAPACITANCE versus FREQUENCY



2N5162 DESIGN DATA

FIGURE 7 – POWER OUTPUT versus FREQUENCY

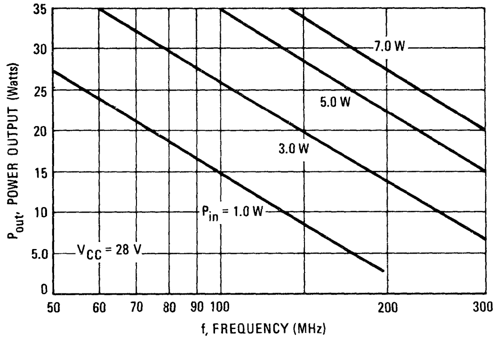
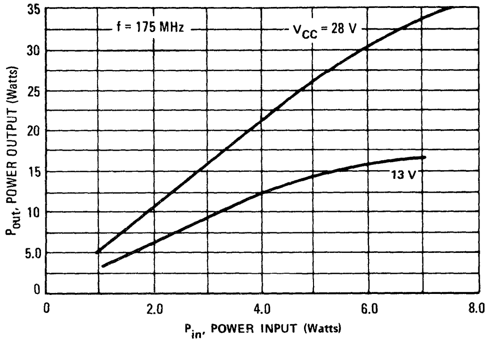


FIGURE 8 – POWER OUTPUT versus POWER INPUT



LARGE SIGNAL IMPEDANCE DATA

FIGURE 9 – REAL SERIES INPUT RESISTANCE versus FREQUENCY

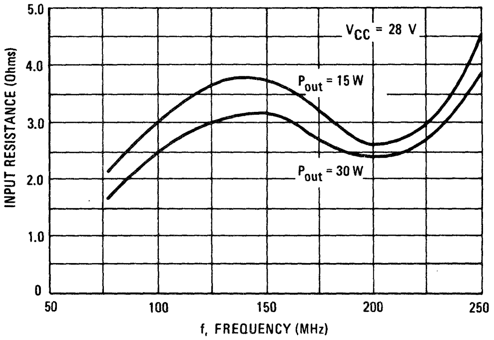


FIGURE 10 – IMAGINARY SERIES INPUT REACTANCE versus FREQUENCY

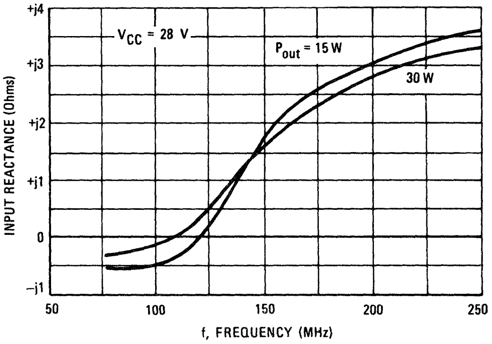
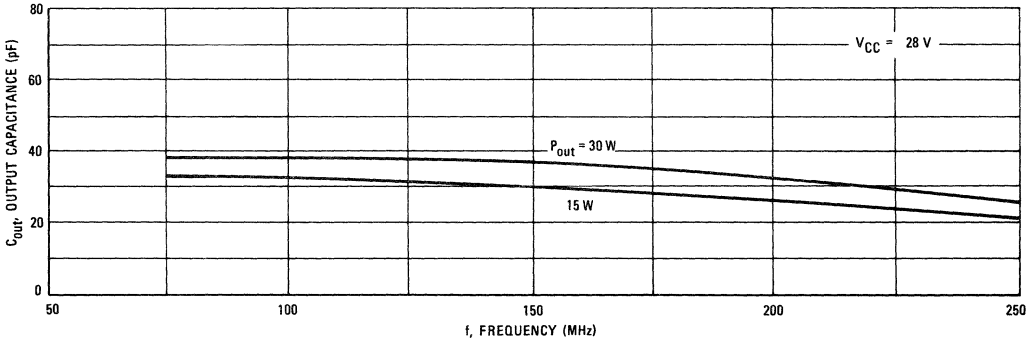


FIGURE 11 – OUTPUT CAPACITANCE versus FREQUENCY



2N5164 thru 2N5171 (SILICON)
2N5164R thru 2N5171R

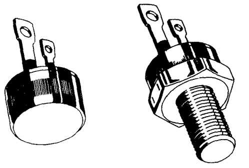
THYRISTORS
SILICON CONTROLLED RECTIFIERS

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Supplied in Either Pressfit or Stud Package
- High Surge Current Rating – I_{TSM} = 240 Amp
- Low On-State Voltage – 1.2 V (Typ) @ I_{TM} = 20 Amp
- Practical Level Triggering and Holding Characteristics – 10 mA (Typ) @ $T_C = 25^\circ C$

THYRISTORS
PNPN

50-600 VOLTS
20 AMPERES RMS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Reverse Blocking Voltage (1) 2N5164,2N5168 2N5165,2N5169 2N5166,2N5170 2N5167,2N5171	V_{RRM}	 50 200 400 600	Volts
*Non-repetitive Peak Reverse Blocking Voltage 2N5164,2N5168 2N5165,2N5169 2N5166,2N5170 2N5167,2N5171	V_{RSM}	 75 300 500 700	Volts
Forward Current RMS	$I_{T(RMS)}$	20	Amp
Circuit Fusing Considerations (T_J = -40 to +100°C, t ≤8.3 ms)	I^2t	235	A^2s
*Peak Forward Surge Current (One cycle, 60 Hz, T_J = -40 to +100°C)	I_{TSM}	240	Amp
*Peak Forward Gate Power	P_{GFM}	5.0	Watts
*Average Forward Gate Power	$P_{GF(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GFM}	2.0	Amp
Peak Gate Voltage – Forward (2) Reverse	V_{GFM} V_{GRM}	10 10	Volts
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque (3) 2N5168-2N5171		30	in. lb.

THERMAL CHARACTERISTICS

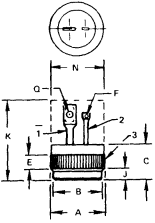
Characteristic	Symbol	Typ	Max	Unit
*Thermal Resistance, Junction to Case 2N5164,65,66,67 2N5168,69,70,71	θ_{JC}	 1.0 1.1	 1.5 1.6	°C/W

*Indicates JEDEC Registered Data.

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.

(2) Devices should not be operated with a positive bias applied to the gate concurrent with a negative potential applied to the anode.

(3) Reliable operation can be impaired if torque rating is exceeded, terminal tubes bent, or glass seal broken.



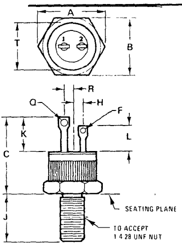
2N5164
2N5165
2N5166
2N5167

All JEDEC dimensions and notes apply

CASE 174-02
TO-203AA

STYLE 1
TERM. 1. GATE
2. CATHODE
3 ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.726	12.827	0.501	0.505
B	11.811	12.065	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	1.72	0.035	0.068
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.66	2.28	0.065	0.090



2N5168
2N5169
2N5170
2N5171

CASE 175

STYLE 1:
TERM 1. CATHODE
2. GATE
STUD : ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	1.40	1.65	0.055	0.065
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	2.03	2.41	0.080	0.095
R	1 65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
*Peak Forward Blocking Voltage (T_J = 100°C) 2N5164, 2N5168	V_{DRM}(1)	50	–	Volts
2N5165, 2N5169		200	–	
2N5166, 2N5170		400	–	
2N5167, 2N5171		600	–	
*Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 100°C, gate open)	I_{DRM}	–	5.0	mA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 100°C, gate open)	I_{RRM}	–	5.0	mA
Gate Trigger Current (Continuous dc)	I_{GT}(2)			mA
(Anode Voltage = 7.0 Vdc, R_L = 100 Ω)		–	40	
*(Anode Voltage = 7.0 Vdc, R_L = 100 Ω, T_C = -40°C)		–	75	
Gate Trigger Voltage (Continuous dc)	V_{GT}			Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ω)		–	1.5	
*(Anode Voltage = 7.0 Vdc, R_L = 100 Ω, T_C = -40°C)		–	2.5	
*(Anode Voltage = Rated V_{DRM}, R_L = 100 Ω, T_J = 100°C)	V_{GD}	0.2	–	
Forward "ON" Voltage (pulsed, 1.0 ms max, duty cycle ≤1%)	V_{TM}			Volts
(I_{TM} = 20 A)		–	1.5	
(I_{TM} = 41 A)		–	1.7	
Holding Current	I_H			mA
(Anode Voltage = 7.0 Vdc, gate open)		–	50	
*(Anode Voltage = 7.0 Vdc, gate open, T_C = -40°C)		–	90	
		TYPICAL		
Turn-On Time ($t_d + t_r$) (I_{TM} = 20 A, I_{GT} = 40 mAdc)	t_{on}	1.0		μs
Turn-Off Time	t_{off}			μs
(I_{TM} = 10 A, I_R = 10 A)		20		
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C) (V_{DRM} = rated voltage) (dv/dt = 30 V/μs)		30		
Forward Voltage Application Rate (Gate open, T_J = 100°C)	dv/dt	50		V/μs

*Indicates JEDEC Registered Data.

(1) V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. These devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

(2) For optimum operation, i.e. faster turn-on, lower switching losses, best di/dt capability, recommended I_{GT} = 200 mA.

EFFECT OF TEMPERATURE UPON TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 – GATE TRIGGER CURRENT

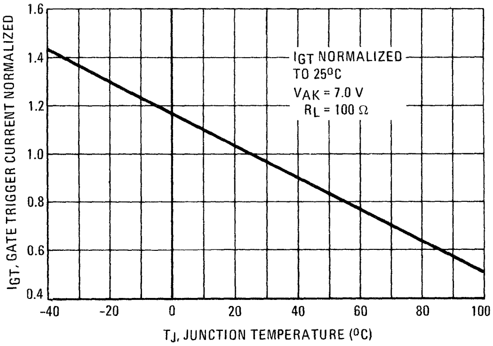
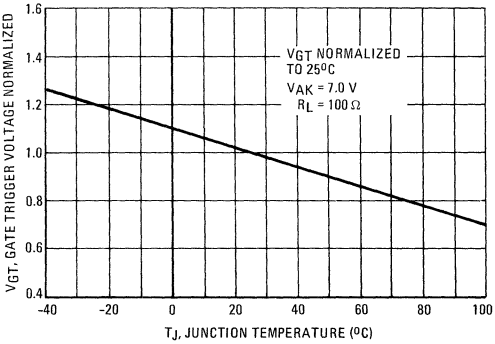


FIGURE 2 – GATE TRIGGER VOLTAGE



MAXIMUM ALLOWABLE NON-RECURRENT SURGE CURRENT

FIGURE 3 – 60 Hz SURGES

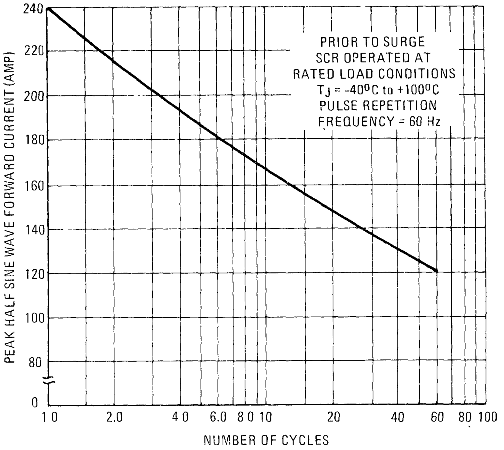


FIGURE 4 – SUB-CYCLE SURGES

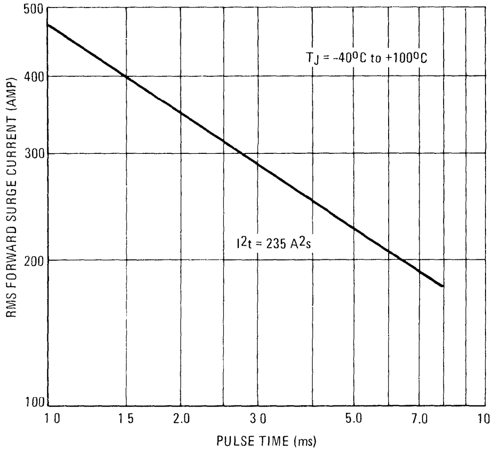


FIGURE 5 – GATE TRIGGER CHARACTERISTICS

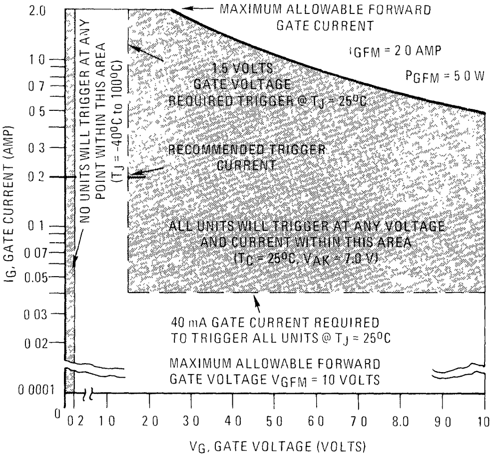
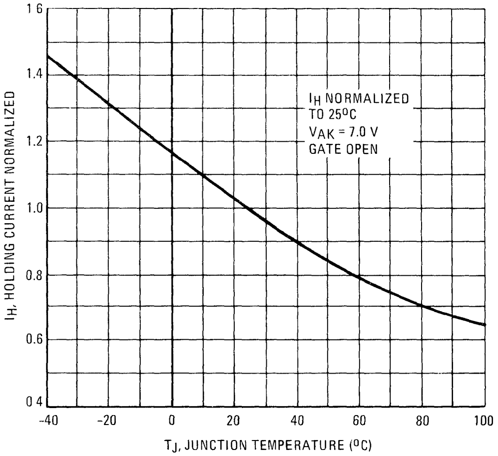


FIGURE 6 – EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT



DERATING AND DISSIPATION FOR RESISTIVE AND INDUCTIVE LOADS (f = 60 to 400 Hz, SINE WAVE)

FIGURE 7 – CURRENT DERATING(1)

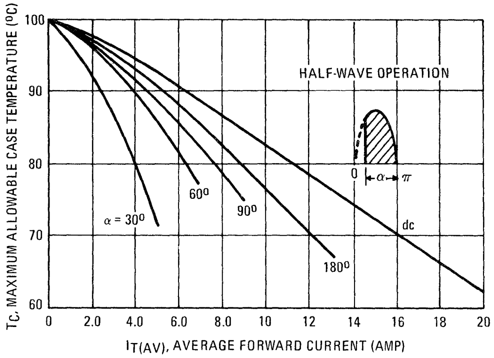


FIGURE 8 – FORWARD POWER DISSIPATION

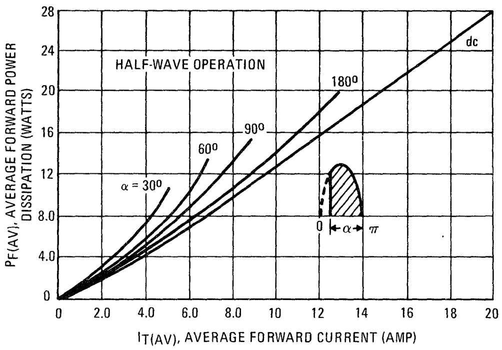


FIGURE 9 – FORWARD CONDUCTION CHARACTERISTICS

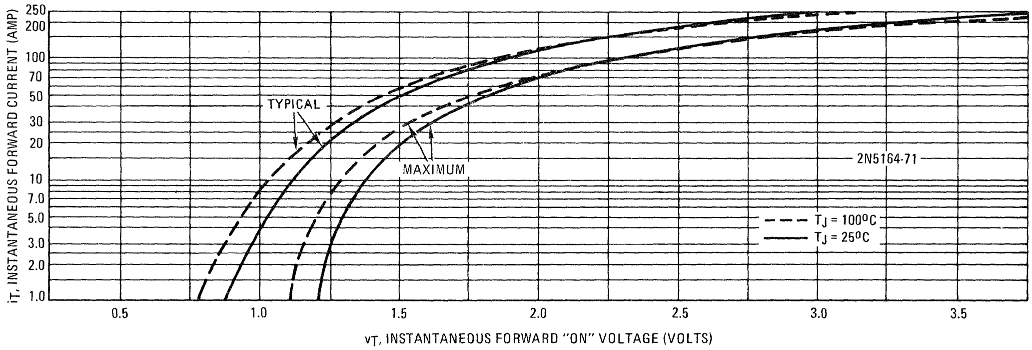
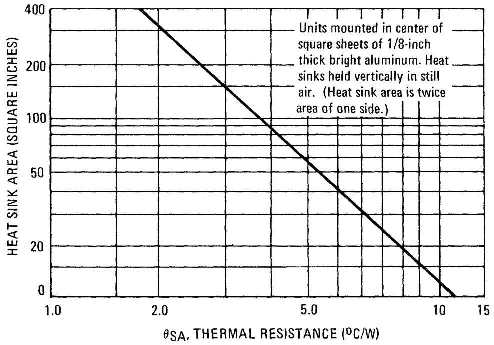


FIGURE 10 – TYPICAL THERMAL RESISTANCE OF PLATES



(1) Reverse polarity units must be derated an additional 10%; i.e., in Figure 7 the maximum allowable case temperature of the 2N5164 at 16 Adc is 70°C, a derating of 30°C below the maximum junction temperature. For the 2N5164R the derating would be an additional 10% or 3.0°C, making the allowable case temperature 67°C.

For additional mounting information, refer to the Motorola brochure "Mounting Techniques for Pressfit Silicon Rectifiers and Silicon Controlled Rectifiers".

2N5179 (SILICON)

The RF Line

4.5 dB @ 200 MHz

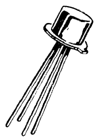
HIGH FREQUENCY TRANSISTOR

NPN SILICON

NPN SILICON RF HIGH FREQUENCY TRANSISTOR

. . . designed primarily for use in high-gain, low-noise amplifier, oscillator, and mixer applications. Can also be used in UHF converter applications.

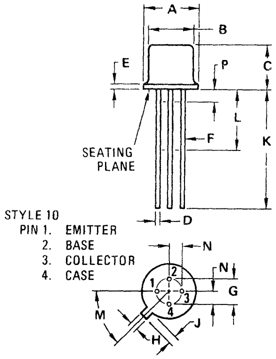
- High Current-Gain – Bandwidth Product –
  f_T = 1.4 GHz (Typ) @ I_C = 10 mAdc
- Low Collector-Base Time Constant –
  $r_b'C_c$ = 14 ps (Max) @ I_E = 2.0 mAdc
- Characterized with Scattering Parameters
- Low Noise Figure –
  NF = 4.5 dB (Max) @ f = 200 MHz



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage Applicable 1.0 to 20 mAdc	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CB}	20	Vdc
Emitter-Base Voltage	V_{EB}	2.5	Vdc
Collector Current	I_C	50	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



STYLE 10
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

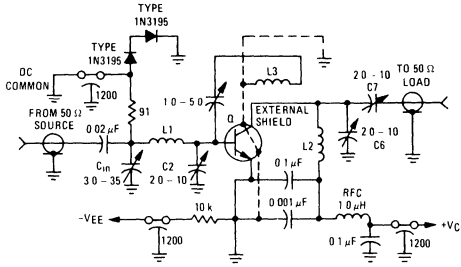
*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 3.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	12	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.001 mAdc, I_E = 0)	BV_{CBO}	20	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.01 mAdc, I_C = 0)	BV_{EBO}	2.5	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0) (V_{CB} = 15 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	– –	0.02 1.0	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 3.0 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	25	250	–
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	–	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product ① (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	900	2000	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{cb}	–	1.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 kHz)	h_{fe}	25	300	–
Collector-Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 6.0 Vdc, f = 31.9 MHz)	$r_b C_c$	3.0	14	ps
Noise Figure (See Figure 1) (I_C = 1.5 mAdc, V_{CE} = 6.0 Vdc, R_S = 50 ohms, f = 200 MHz)	NF	–	4.5	dB
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (See Figure 1) (V_{CE} = 6.0 Vdc, I_C = 5.0 mAdc, f = 200 MHz)	G_{pe}	15	–	dB
Power Output (See Figure 2) (V_{CB} = 10 Vdc, I_E = 12 mAdc, f≥500 MHz)	P_{out}	20	–	mW

*Indicates JEDEC Registered Values.

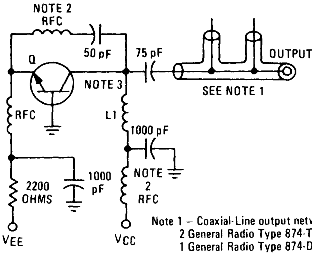
① f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – 200 MHz AMPLIFIER POWER GAIN AND NOISE FIGURE CIRCUIT



L1 1-3/4 Turns, #18 AWG, 0 5" L, 0 5" Diameter
L2 2 Turns, #16 AWG, 0 5" L, 0.5" Diameter
L3 2 Turns, #13 AWG, 0 25" L, 0.5" Diameter (Position 1/4" from L2)

FIGURE 2 – 500 MHz OSCILLATOR CIRCUIT



Note 1 – Coaxial-Line output network consisting of
2 General Radio Type 874-TEE or equivalent
1 General Radio Type 874-D20 Adjustable Stub or equivalent
1 General Radio Type 874-LA Adjustable Line or equivalent
1 General Radio Type 874-WN3 Short-circuit termination or equivalent

Note 2 – RFC = 0.2 μH Ohmite #2-460 or equivalent

Note 3 – Lead Number 4 (case) floating

L1 – 2 turns #16 AWG wire, 3/8 inch OD, 1-1/4 inch long

Q = 2N5179

FIGURE 3 – NOISE FIGURE versus FREQUENCY

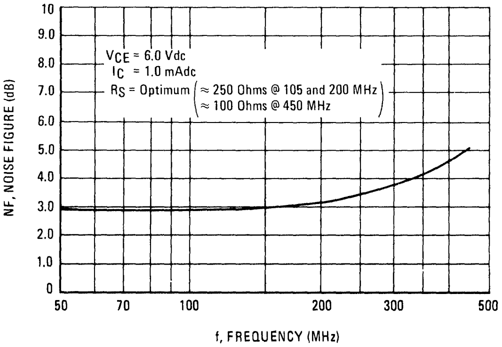


FIGURE 4 – NOISE FIGURE versus SOURCE RESISTANCE and COLLECTOR CURRENT

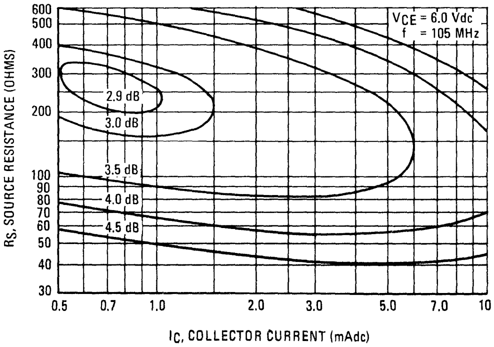


FIGURE 5 – NOISE FIGURE versus SOURCE RESISTANCE and COLLECTOR CURRENT

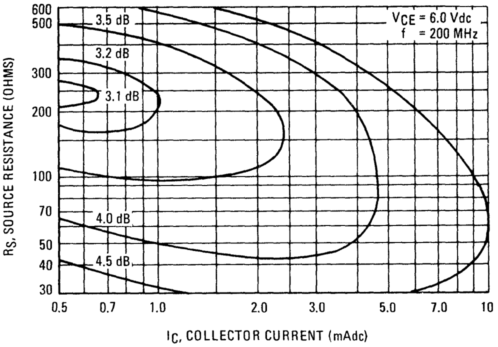


FIGURE 6 — CURRENT-GAIN-BANDWIDTH PRODUCT

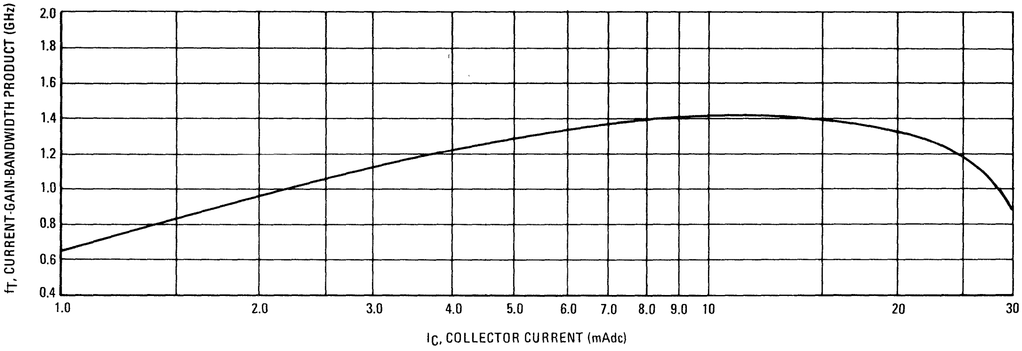


FIGURE 7 — INPUT ADMITTANCE versus FREQUENCY

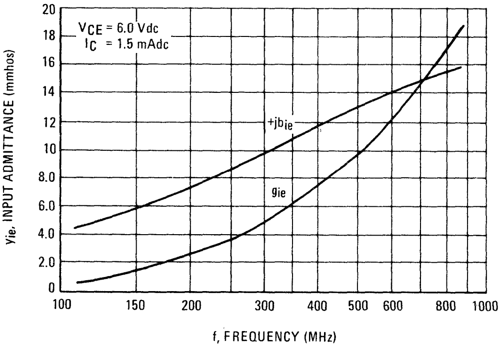


FIGURE 8 — OUTPUT ADMITTANCE versus FREQUENCY

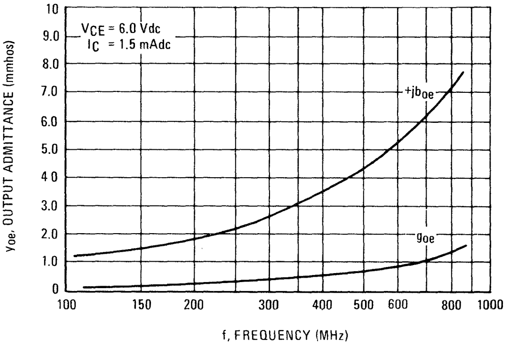


FIGURE 9 — FORWARD TRANSFER ADMITTANCE versus FREQUENCY

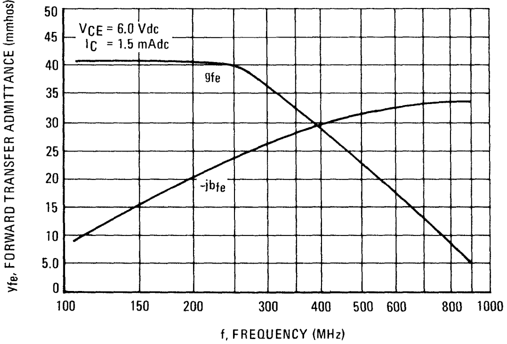


FIGURE 10 — REVERSE TRANSFER ADMITTANCE versus FREQUENCY

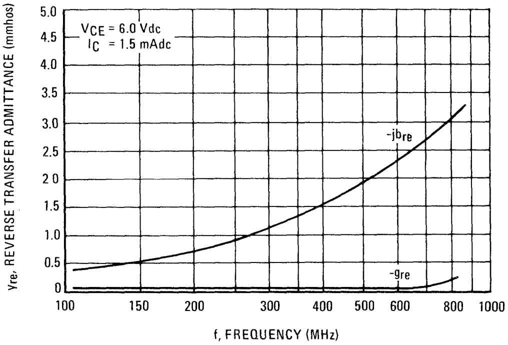


FIGURE 11— S_{11}, INPUT REFLECTION COEFFICIENT

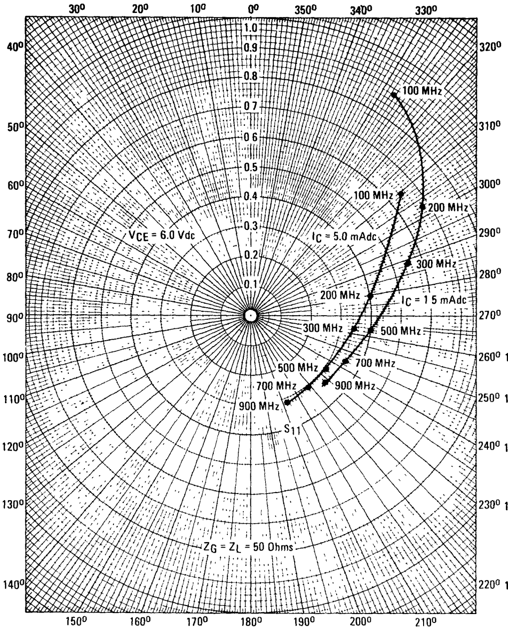


FIGURE 12—S_{22}, OUTPUT REFLECTION COEFFICIENT

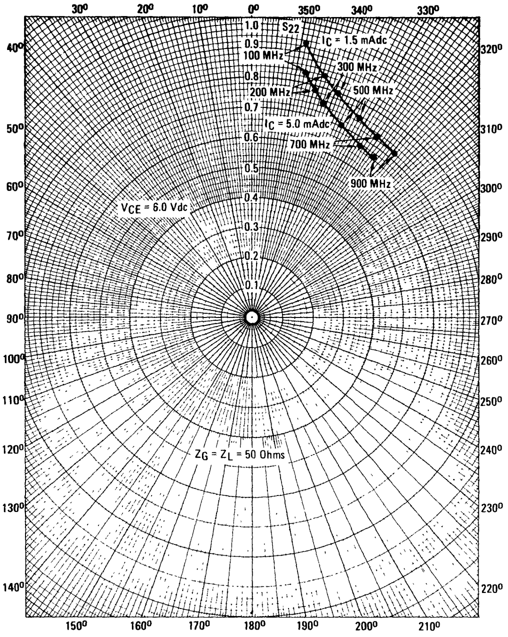


FIGURE 13 — S_{12}, REVERSE TRANSMISSION COEFFICIENT

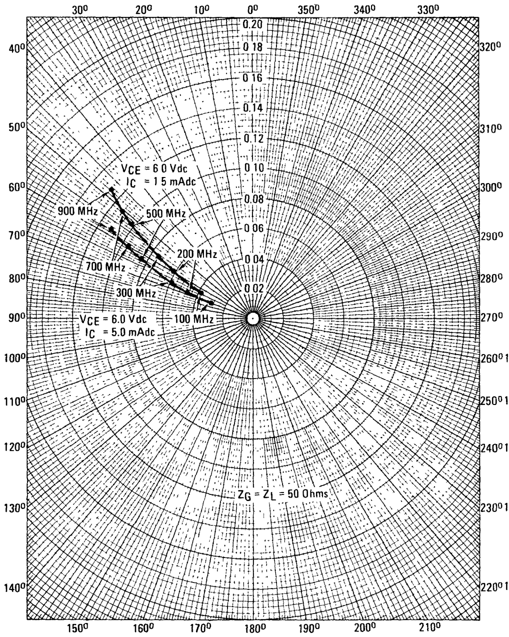


FIGURE 14 — S_{21}, FORWARD TRANSMISSION COEFFICIENT

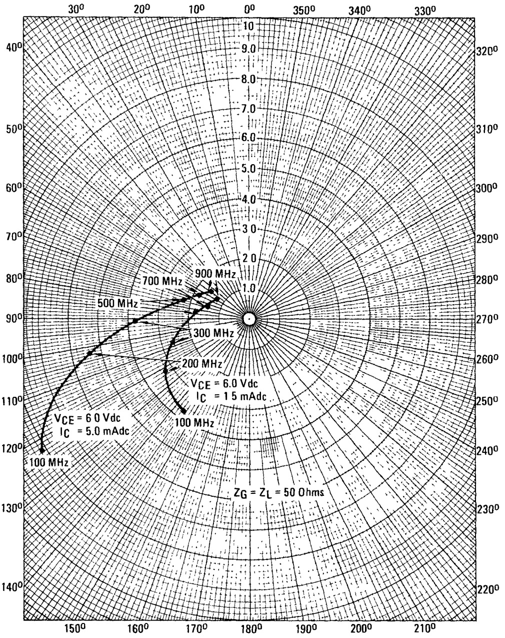
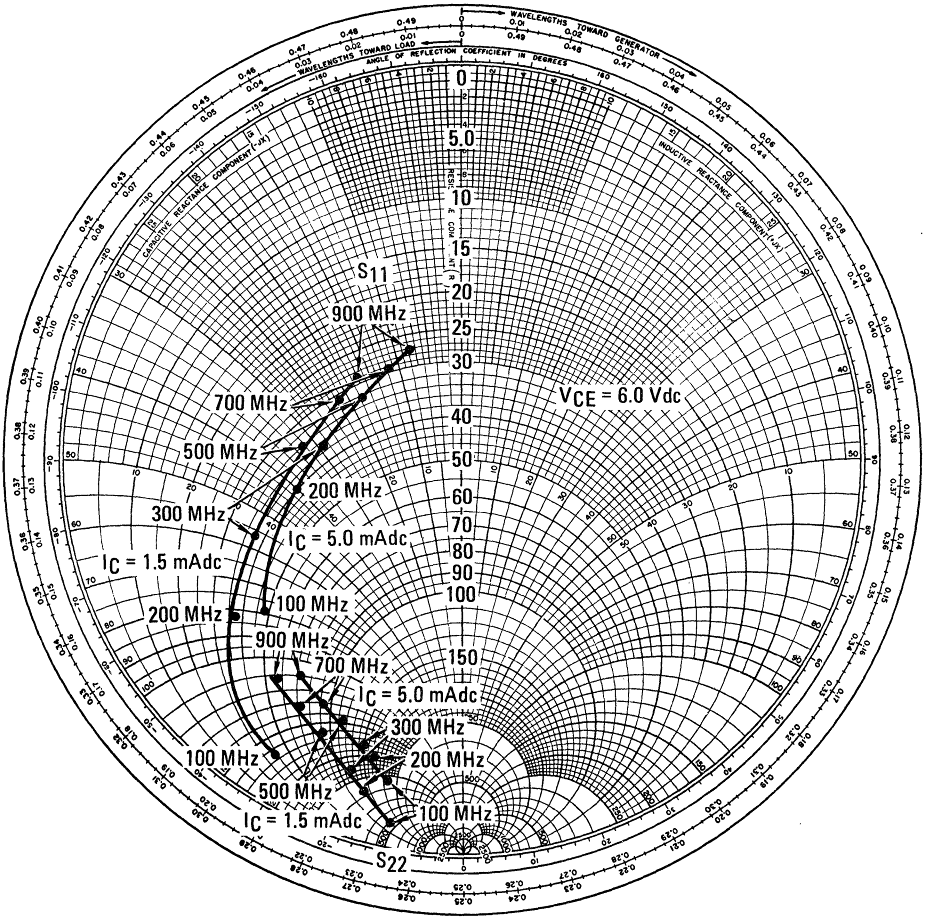


FIGURE 15—S_{11}, INPUT REFLECTION COEFFICIENT AND S_{22}, OUTPUT REFLECTION COEFFICIENT



2N5190 thru 2N5192 (SILICON)
MJE5190 thru MJE5192

SILICON NPN POWER TRANSISTORS

. . . for use in power amplifier and switching circuits, — excellent safe area limits. Complement to PNP 2N5193, 2N5194, 2N5195 and MJE5193, MJE5194, MJE5195.

4 AMPERE
POWER TRANSISTORS
SILICON NPN

40-80 VOLTS
40 and 60 WATTS

*MAXIMUM RATINGS

Rating	Symbol	2N5190 MJE5190	2N5191 MJE5191	2N5192 MJE5192	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current	I_C	← 4.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
		2N5190 Series	MJE5190 Series		
Total Device Dissipation @ $T_C = 25^{\circ}C$ Derate above 25°C	P_D	40 320	60 480		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

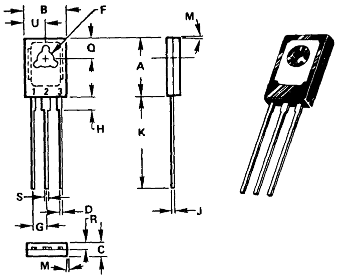
THERMAL CHARACTERISTICS

Characteristic	Symbol	2N5190 Series	MJE5190 Series	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	2.08	°C/W

*ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 0.1$ Adc, $I_B = 0$) 2N5190,MJE5190 2N5191,MJE5191 2N5192,MJE5192	$V_{CEO(sus)}$	 40 60 80	 – – –	Vdc
Collector Cutoff Current ($V_{CE} = 40$ Vdc, $I_B = 0$) 2N5190,MJE5190 ($V_{CE} = 60$ Vdc, $I_B = 0$) 2N5191,MJE5191 ($V_{CE} = 80$ Vdc, $I_B = 0$) 2N5192,MJE5192	I_{CEO}	 – – –	 1.0 1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 40$ Vdc, $V_{EB(off)} = 1.5$ Vdc) 2N5190,MJE5190 ($V_{CE} = 60$ Vdc, $V_{EB(off)} = 1.5$ Vdc) 2N5191,MJE5191 ($V_{CE} = 80$ Vdc, $V_{EB(off)} = 1.5$ Vdc) 2N5192,MJE5192 ($V_{CE} = 40$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^{\circ}C$) 2N5190,MJE5190 ($V_{CE} = 60$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^{\circ}C$) 2N5191,MJE5191 ($V_{CE} = 80$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^{\circ}C$) 2N5192,MJE5192	I_{CEX}	 – – – – – –	 0.1 0.1 0.1 2.0 2.0 2.0	mAdc
Collector Cutoff Current ($V_{CB} = 40$ Vdc, $I_E = 0$) 2N5190,MJE5190 ($V_{CB} = 60$ Vdc, $I_E = 0$) 2N5191,MJE5191 ($V_{CB} = 80$ Vdc, $I_E = 0$) 2N5192,MJE5192	I_{CBO}	 – – –	 0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}	 –	 1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain(1) ($I_C = 1.5$ Adc, $V_{CE} = 2.0$ Vdc) 2N5190,MJE5190 2N5191,MJE5191 2N5192,MJE5192 ($I_C = 4.0$ Adc, $V_{CE} = 2.0$ Vdc) 2N5190,MJE5190 2N5191,MJE5191 2N5192,MJE5192	h_{FE}	 25 25 20 10 10 7.0	 100 100 80 – –	–
Collector-Emitter Saturation Voltage(1) ($I_C = 1.5$ Adc, $I_B = 0.15$ Adc) ($I_C = 4.0$ Adc, $I_B = 1.0$ Adc)	$V_{CE(sat)}$	 – –	 0.6 1.4	Vdc
Base-Emitter On Voltage (1) ($I_C = 1.5$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$	 –	 1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, f = 1.0 MHz)	f_T	 2.0	 –	MHz

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.
*Indicates JEDEC Registered Data for 2N5190 Series.

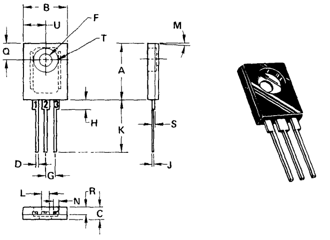


STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

2N5190
2N5191
2N5192

CASE 77-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.36 BSC		0.093 BSC	
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.38	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155



STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER

MJE5190
MJE5191
MJE5192

CASE 199-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0.152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

NOTES
1 DIM "G" IS TO CENTER OF LEADS

FIGURE 1 – DC CURRENT GAIN

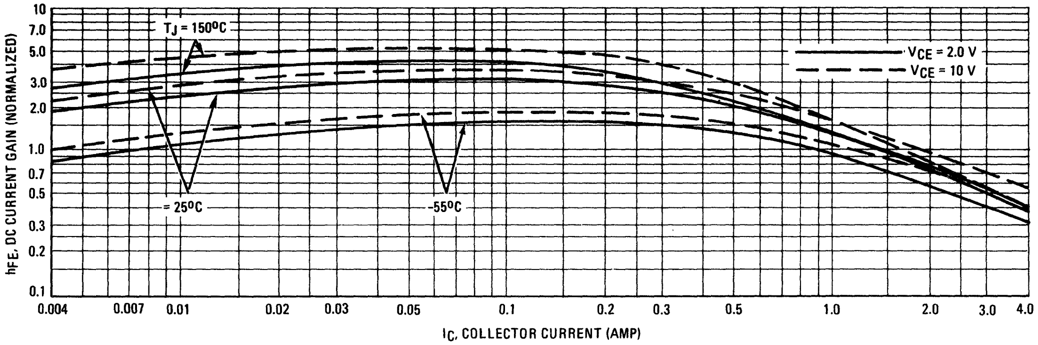


FIGURE 2 – COLLECTOR SATURATION REGION

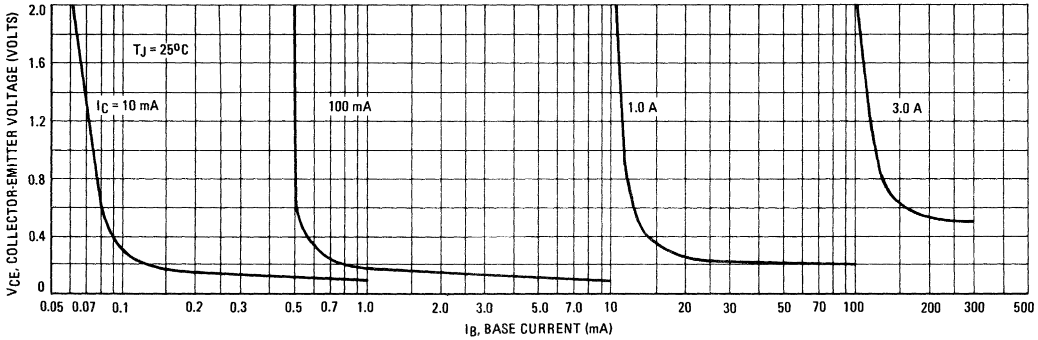


FIGURE 3 – "ON" VOLTAGES

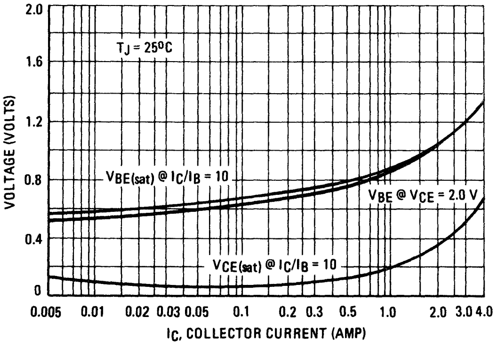


FIGURE 4 – TEMPERATURE COEFFICIENTS

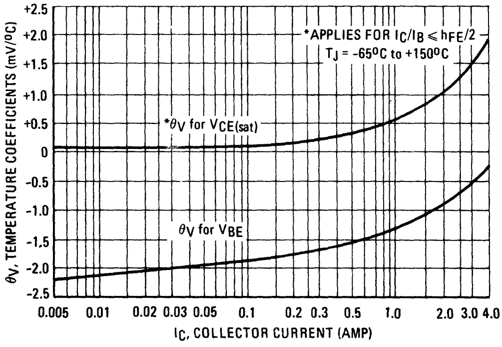


FIGURE 5 – COLLECTOR CUT-OFF REGION

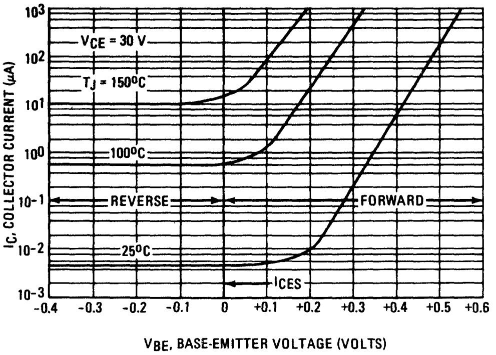


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

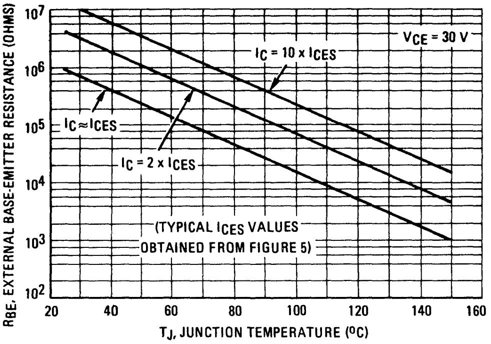


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

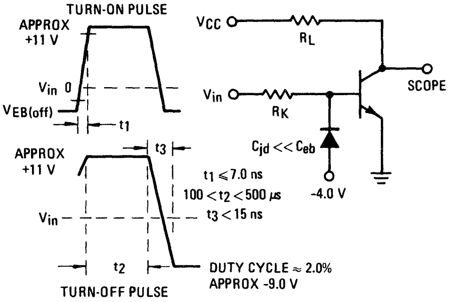


FIGURE 8 – CAPACITANCE

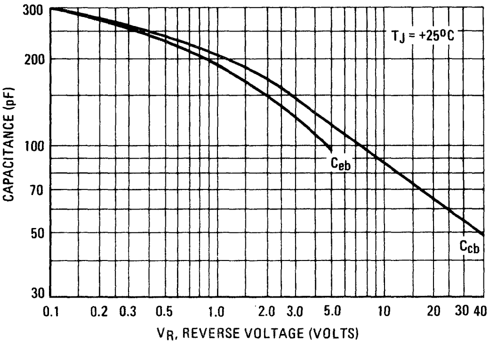


FIGURE 9 – TURN-ON TIME

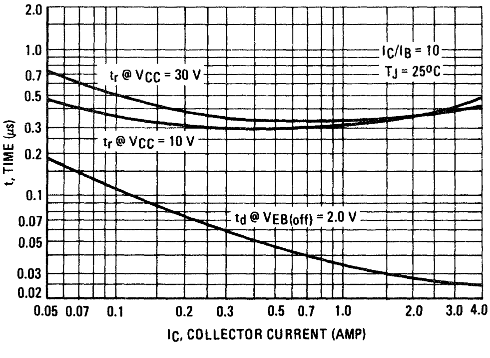
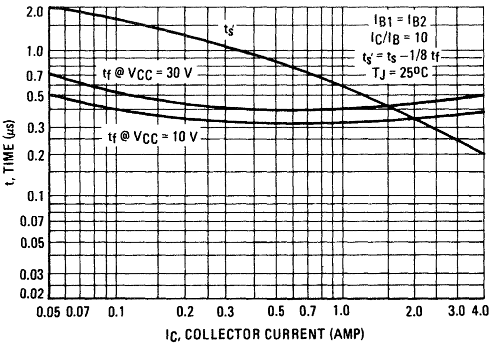


FIGURE 10 – TURN-OFF TIME



RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA

FIGURE 11 – 2N5190,2N5191,2N5192

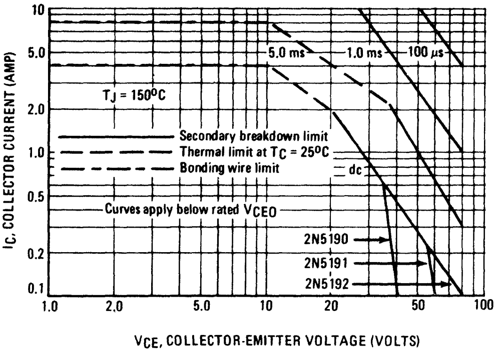
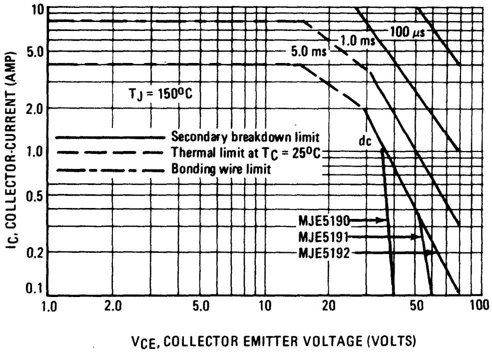


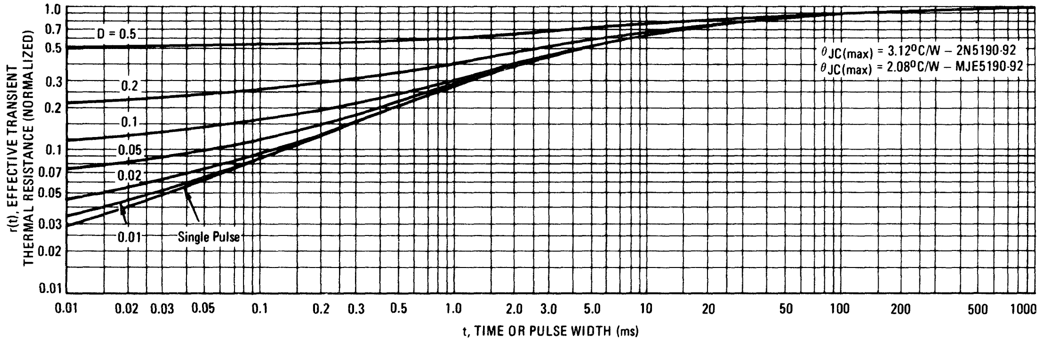
FIGURE 12 – MJE5190, MJE5191, MJE5192



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

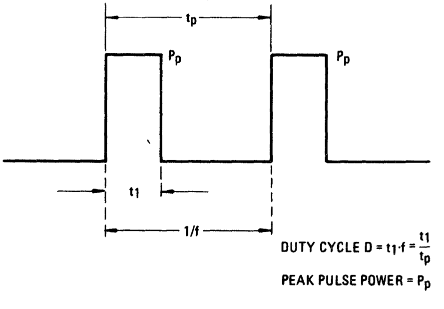
The data of Figures 11 and 12 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 13 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 13 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 13 by the steady state value θ_{JC}.

Example:

The 2N5190 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, tp = 0.5 ms. (D = 0.2).

Using Figure 13, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$

2N5193 thru 2N5195 (SILICON)
MJE5193 thru MJE5195

SILICON PNP POWER TRANSISTORS

. . . for use in power amplifier and switching circuits, – excellent safe area limits. Complement to NPN 2N5190, 2N5191, 2N5192 and MJE5190, MJE5191, MJE5192.

4 AMPERE
POWER TRANSISTORS
SILICON PNP

40-80 VOLTS
40 and 60 WATTS

*MAXIMUM RATINGS

Rating	Symbol	2N5193 MJE5193	2N5194 MJE5194	2N5195 MJE5195	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current	I_C	← 4 0 →			Adc
Base Current	I_B	← 1 0 →			Adc
		2N5193 Series	MJE5193 Series		
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	60 480		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C/W

THERMAL CHARACTERISTICS

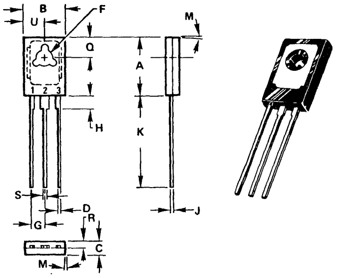
Characteristic	Symbol	2N5193 Series	MJE5193 Series	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3 12	2.08	°C/W

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 0 1 Adc, I_B = 0)	2N5193, MJE5193		40	–	
	2N5194, MJE5194		60	–	
	2N5195, MJE5195		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5193, MJE5193		–	1 0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5194, MJE5194		–	1 0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5195, MJE5195		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1 5 Vdc)	2N5193, MJE5193		–	0 1	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5194, MJE5194		–	0 1	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1 5 Vdc)	2N5195, MJE5195		–	0 1	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1 5 Vdc, T_C = 125°C)	2N5193, MJE5193		–	2 0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1 5 Vdc, T_C = 125°C)	2N5194, MJE5194		–	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1 5 Vdc, T_C = 125°C)	2N5195, MJE5195		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N5193, MJE5193		–	0 1	
(V_{CB} = 60 Vdc, I_E = 0)	2N5194, MJE5194		–	0 1	
(V_{CB} = 80 Vdc, I_E = 0)	2N5195, MJE5195		–	0.1	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1 0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5193, MJE5193, 2N5194, MJE5194,		25	100	
	2N5195, MJE5195		20	80	
(I_C = 4 0 Adc, V_{CE} = 2 0 Vdc)	2N5193, MJE5193, 2N5194, MJE5194,		10	–	
	2N5195, MJE5195		7.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0 15 Adc)			–	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			–	1 2	
Base-Emitter On Voltage (1) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1 2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz

*Indicates JEDEC Registered Data for 2N5193 Series.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

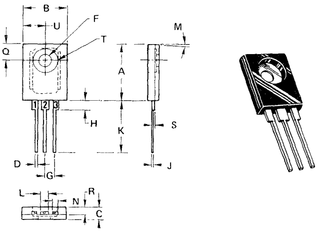


STYLE 1
PIN 1 EMITTER
2. COLLECTOR
3. BASE

2N5193
2N5194
2N5195

CASE 77-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.36 BSC		0.093 BSC	
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.38	16.64	0 605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155



STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER

MJE5193
MJE5194
MJE5195

CASE 199-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16 08	16 33	0 633	G 643
B	12 57	12 83	0 495	0 505
C	3 18	3 43	0 125	0 135
D	0 51	0 76	0 020	0 030
F	3 61	3 86	0 142	0 152
G	2 54 BSC		0 100 BSC	
H	2 67	2 92	0 105	0 115
J	0 43	0 69	0 017	0 027
K	14 73	14 99	0 580	0 590
L	2 16	2 41	0 085	0 095
M	3° TYP		3° TYP	
N	1 47	1 73	0 058	0 068
Q	4 78	5 03	0 188	0 198
R	1 91	2 16	0 075	0 085
S	0 81	0 86	0 032	0 034
T	6 99	7 24	0 275	0 285
U	6 22	6 48	0 245	0 255

NOTES
1 DIM "G" IS TO CENTER OF LEADS

FIGURE 1 – DC CURRENT GAIN

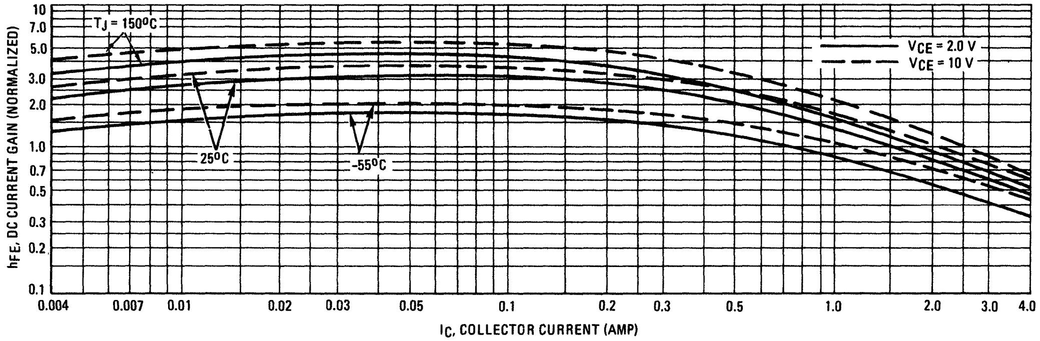


FIGURE 2 – COLLECTOR SATURATION REGION

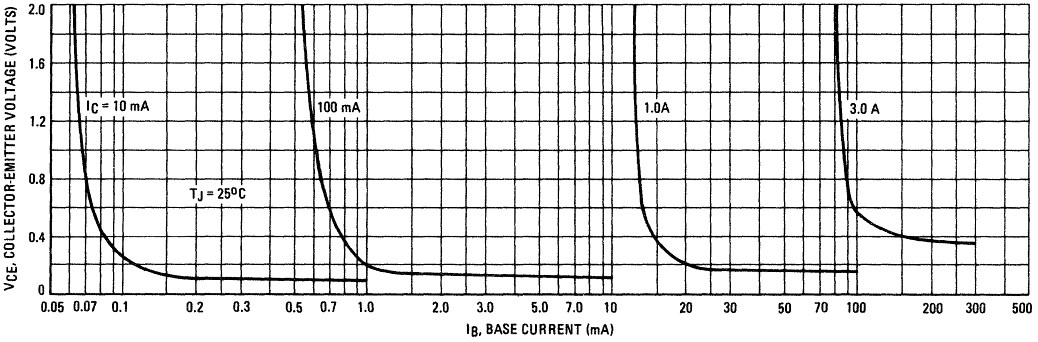


FIGURE 3 – "ON" VOLTAGE

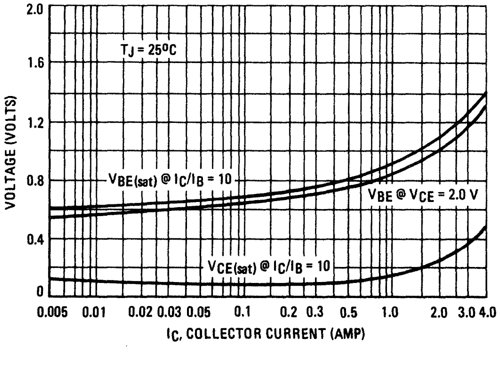


FIGURE 4 – TEMPERATURE COEFFICIENTS

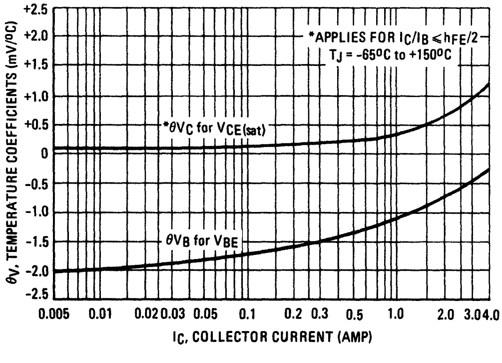


FIGURE 5 – COLLECTOR CUT-OFF REGION

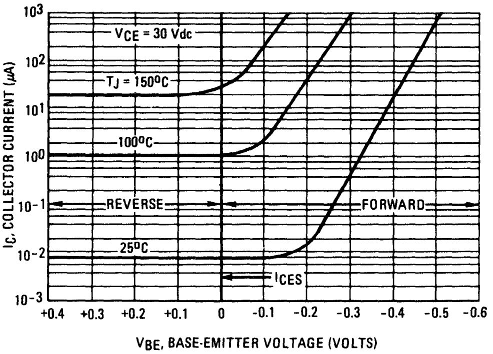


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

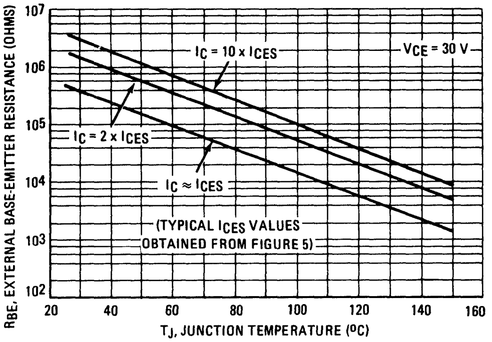


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

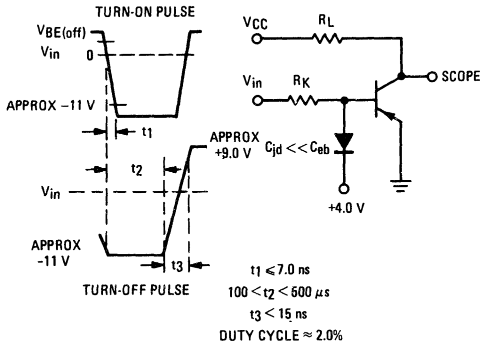


FIGURE 8 – CAPACITANCE

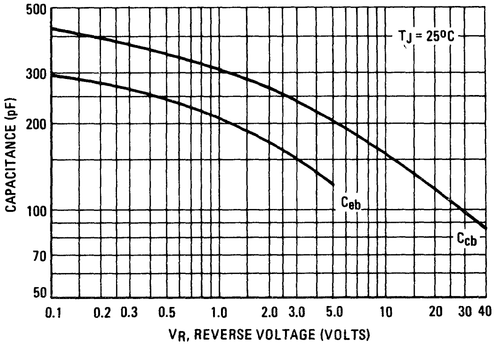


FIGURE 9 – TURN-ON TIME

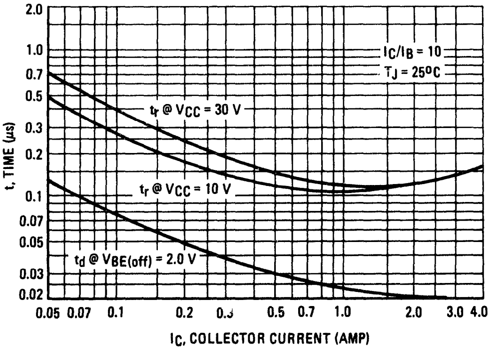
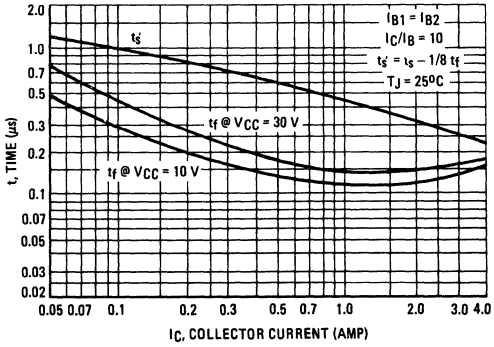
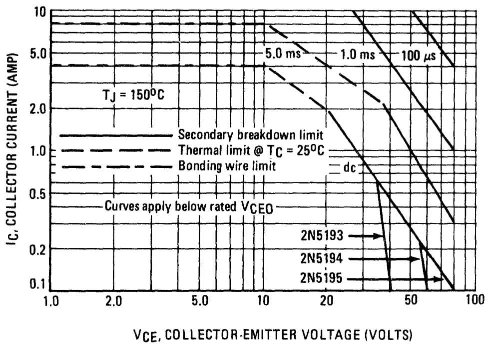


FIGURE 10 – TURN-OFF TIME



RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA

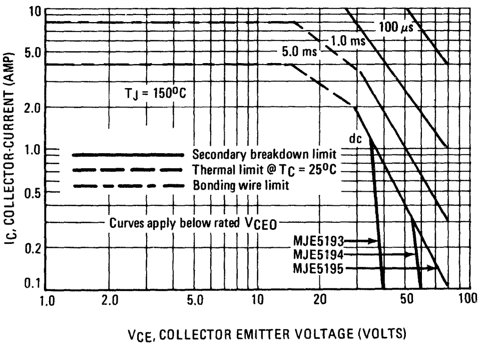
FIGURE 11 – 2N5193, 2N5194, 2N5195



Note 1:

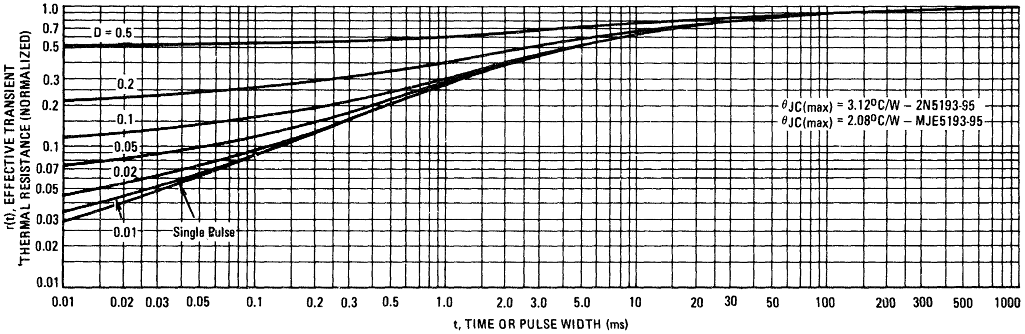
There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

FIGURE 12 – MJE5193, MJE5194, MJE5195



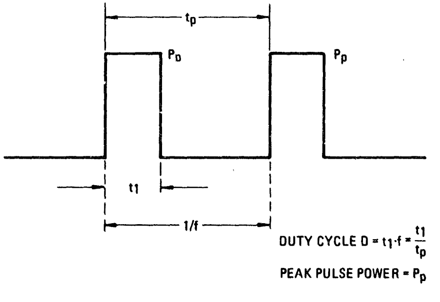
The data of Figures 11 and 12 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 13 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 13 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 13 by the steady state value θ_{JC}.

Example:

The 2N5193 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, tp = 0.5 ms. (D = 0.2).

Using Figure 13, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$

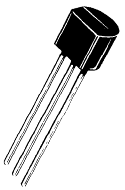
2N5208 (SILICON)

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general purpose RF amplifier applications in the frequency range up to 300 MHz.

- Low Collector-Base Time Constant – $r_b{}'C_c < 10$ ps
- Low Noise Figure N.F. = 3.0 dB max @ 100 MHz
- High Power Gain – G_{pe} = 22 dB min @ 100 MHz
- Complete Y-Parameter Curves
- Low Leakage Current – $I_{CBO} < 10$ nAdc @ V_{CB} = 10 V
- Stability Factor Curves - For Direct Circuit Design

PNP SILICON SWITCHING AND AMPLIFIER TRANSISTOR



*MAXIMUM RATINGS

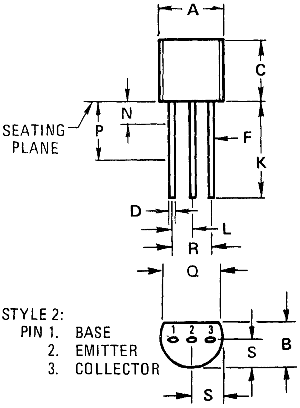
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

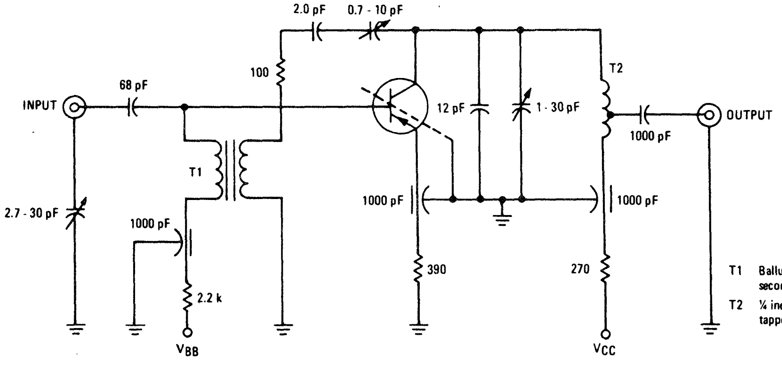
CASE 29-02
TO-92

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	25	-	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	BV_{CBO}	30	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	3.0	-	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	-	10	nAdc
Emitter Cutoff Current (V_{BE} = 2.0 Vdc, I_C = 0)	I_{EBO}	-	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	120	-
Base-Emitter On Voltage (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	-	0.85	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	300	1200	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	-	1.0	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	-	4.0	pF
Collector-Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 10 Vdc, f = 31.8 MHz)	$r_b'C_c$	-	10	ps
Noise Figure (See Figure 1) (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, R_S = 75 ohms, f = 100 MHz, BW = 1.0 MHz)	NF	-	3.0	dB
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (See Figure 1) (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	G_{pe}	22	-	dB

* Indicates JEDEC Registered Data

FIGURE 1 - 100 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT



T1 Ballun Core, 5 turns primary, 5 turns secondary, No. 24 bifilar wound.
T2 ¼ inch inner diameter, 5½ turns tapped up ½ turn, No. 16 buss wire.

COMMON-EMITTER Y PARAMETERS (Polar Plots)

V_{CE} = 10 Vdc, T_A = 25°C

FIGURE 2 - INPUT ADMITTANCE

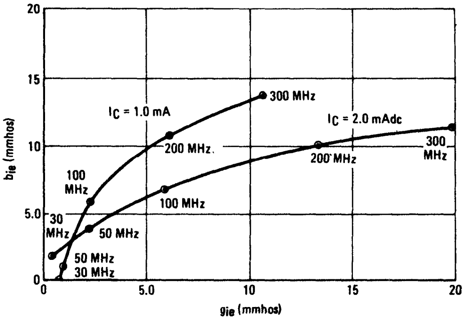


FIGURE 3 - OUTPUT ADMITTANCE

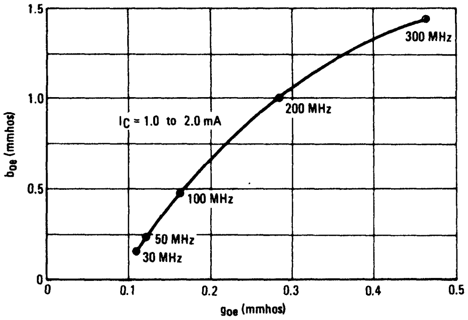


FIGURE 4 - FORWARD TRANSFER ADMITTANCE

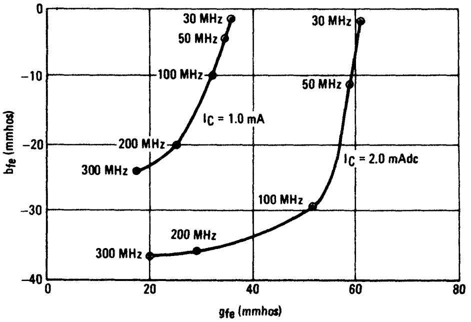
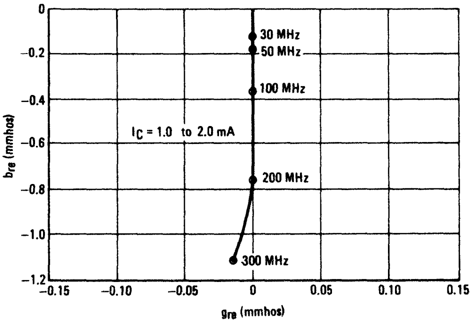


FIGURE 5 - REVERSE TRANSFER ADMITTANCE



STABILITY FACTOR CURVE

FIGURE 6 - POWER GAIN AND NOISE FIGURE

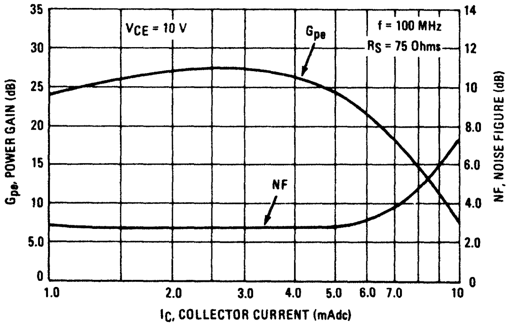
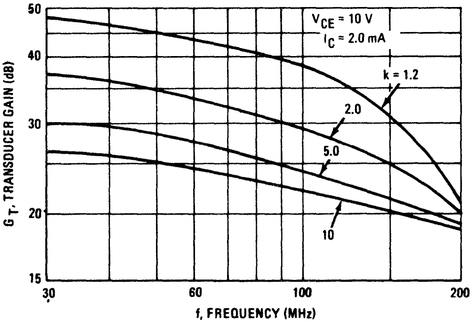


FIGURE 7 - MAXIMUM TRANSDUCER GAIN



COMMON-EMITTER Y PARAMETERS vs FREQUENCY

V_{CE} = 10 Vdc, T_A = 25°C

FIGURE 8 - INPUT ADMITTANCE

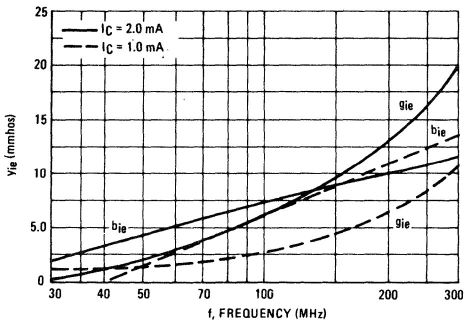


FIGURE 9 - OUTPUT ADMITTANCE

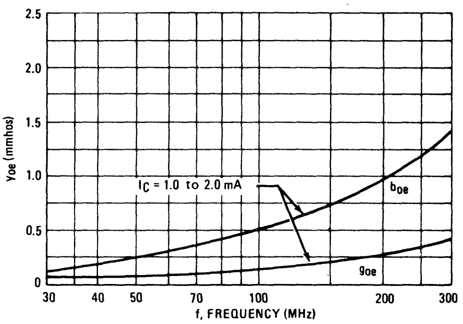


FIGURE 10 - FORWARD TRANSFER ADMITTANCE

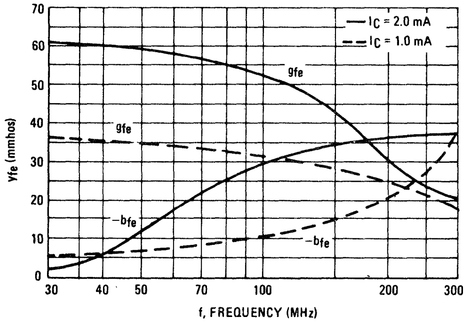
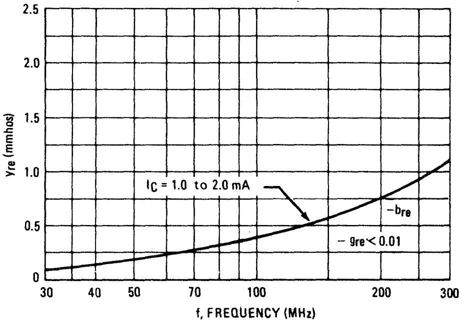


FIGURE 11 - REVERSE TRANSFER ADMITTANCE



STABILITY FACTOR CURVES

FIGURE 12 - OPTIMUM SOURCE ADMITTANCE

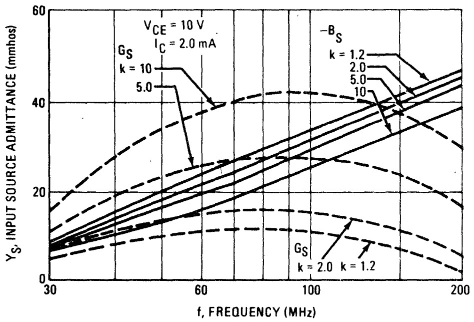
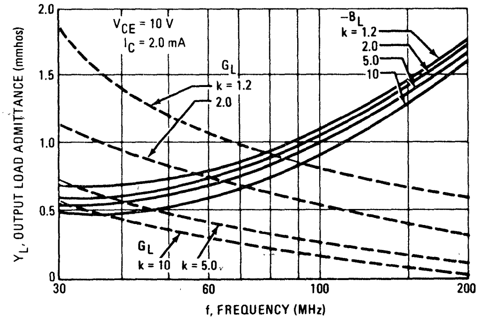


FIGURE 13 - OPTIMUM LOAD ADMITTANCE



When a potentially unstable device is operated without feedback, there is an infinite number of combinations of source and load admittance associated with any given circuit stability factor (k). Equations have been developed for determining the optimum source and load admittance for maximum gain. Figures 7, 12 and 13 provide a solution to the equations for the 2N5208.

NOISE FIGURE

FIGURE 14 - FREQUENCY EFFECTS

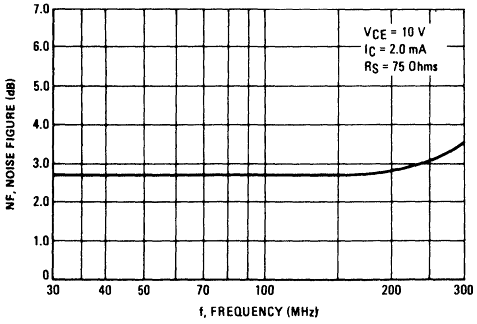


FIGURE 15 - SOURCE RESISTANCE EFFECTS

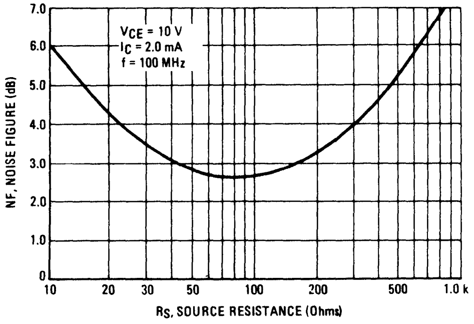


FIGURE 16 - CURRENT-GAIN — BANDWIDTH PRODUCT

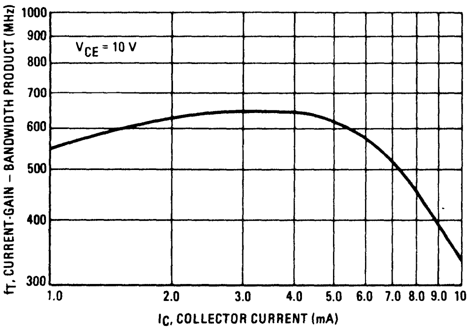


FIGURE 17 - CAPACITANCES

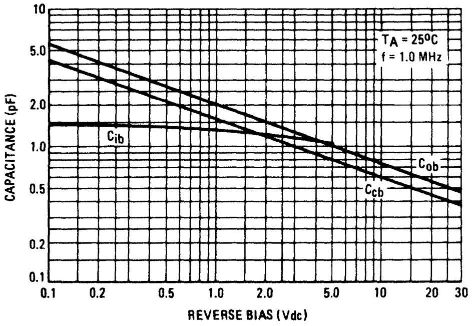
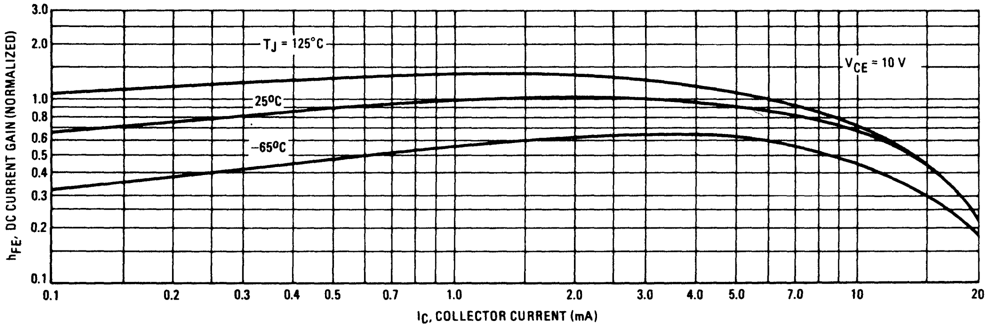


FIGURE 18 - DC CURRENT GAIN



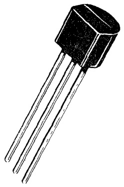
2N5209 (SILICON)
2N5210

NPN SILICON ANNULAR TRANSISTORS

. . . designed for general-purpose amplifier applications and for complementary circuitry with PNP types 2N5086 and 2N5087.

- Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 50 Vdc (Min) @ I_C = 1.0 mAdc
- Current Gain Specified From 100 μA to 10 mA
- Low Collector-Base Capacitance —
  C_{cb} = 4.0 pF (Max) @ V_{CB} = 5.0 Vdc

NPN SILICON
AMPLIFIER TRANSISTORS



*MAXIMUM RATINGS

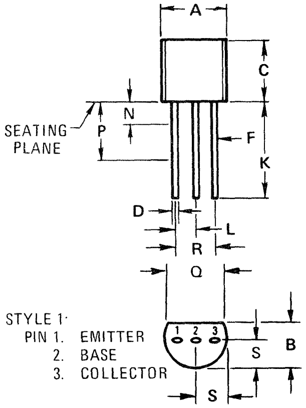
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	4.5	Vdc
Collector Current — Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

2N5209, 2N5210 (continued)

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	50	-	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	BV_{CBO}	50	-	Vdc
Collector Cutoff Current (V_{CB} = 35 Vdc, I_E = 0)	I_{CBO}	-	50	nAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	-	50	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 100 µAdc, V_{CE} = 5.0 Vdc) 2N5209 2N5210	h_{FE}	100 200	300 600	-
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc) 2N5209 2N5210		150 250	- -	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)(1) 2N5209 2N5210		150 250	- -	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	-	0.7	Vdc
Base-Emitter On Voltage (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	-	0.85	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 500 µAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)	f_T	30	-	MHz
Collector Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	-	4.0	pF
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz) 2N5209 2N5210	h_{fe}	150 250	600 900	-
Noise Figure (I_C = 20 µAdc, V_{CE} = 5.0 Vdc, R_S = 22 k ohms, f = 10 Hz to 15.7 kHz) 2N5209 2N5210	NF	- -	3.0 2.0	dB
(I_C = 20 µAdc, V_{CE} = 5.0 Vdc, R_S = 10 k ohms, f = 1.0 kHz) 2N5209 2N5210		- -	4.0 3.0	

*** Indicates JEDEC Registered Data**

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2.0%.

NOISE FIGURE
(V_{CE} = 5.0 Vdc, T_A = 25°C)

FIGURE 1 — NOISE FIGURE versus FREQUENCY

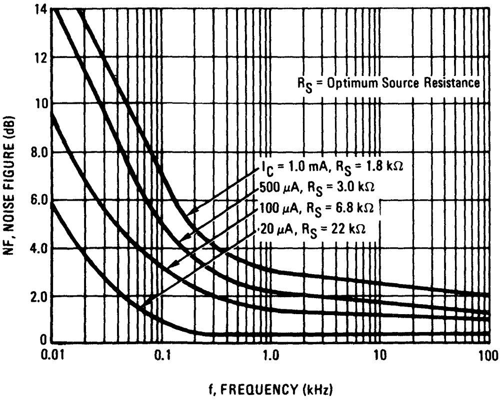


FIGURE 2 — NOISE FIGURE versus SOURCE RESISTANCE

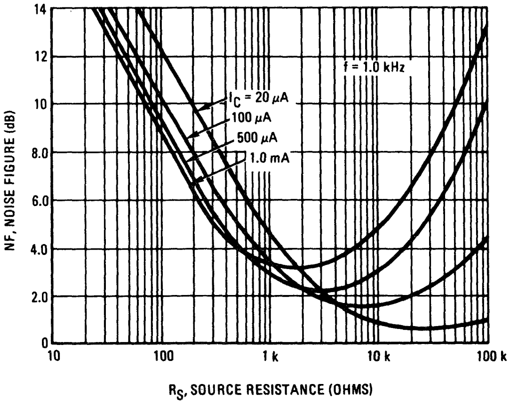


FIGURE 3 – DC CURRENT-GAIN

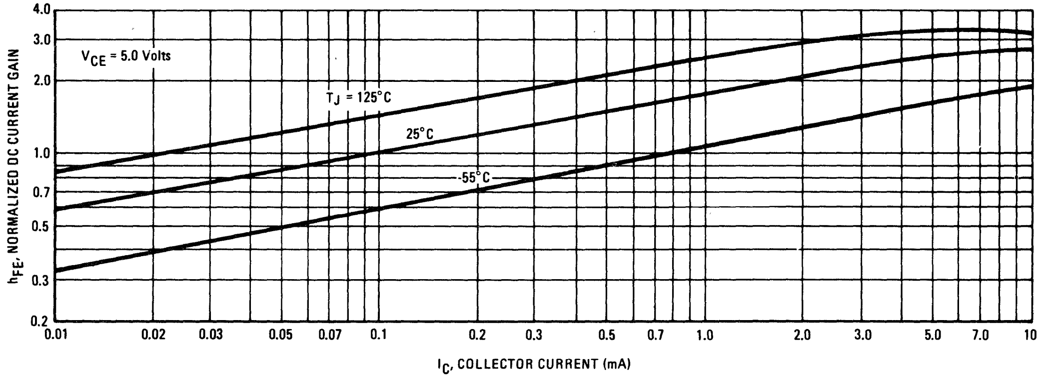


FIGURE 4 – COLLECTOR SATURATION REGION

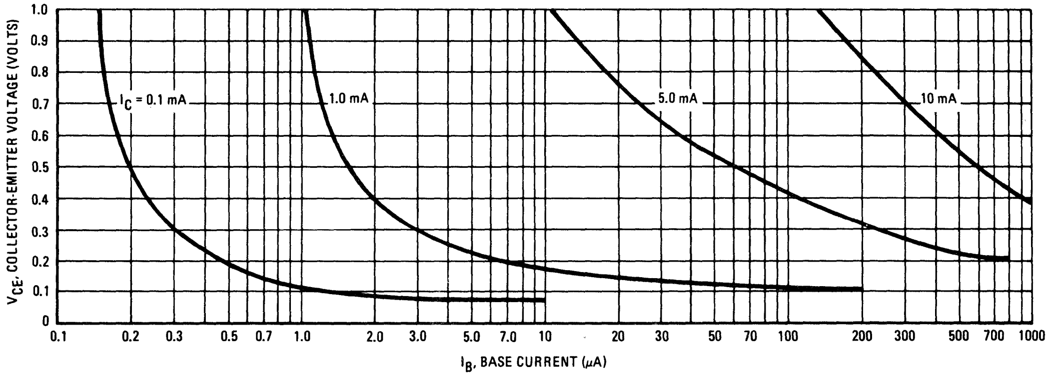


FIGURE 5 – CURRENT-GAIN–BANDWIDTH PRODUCT

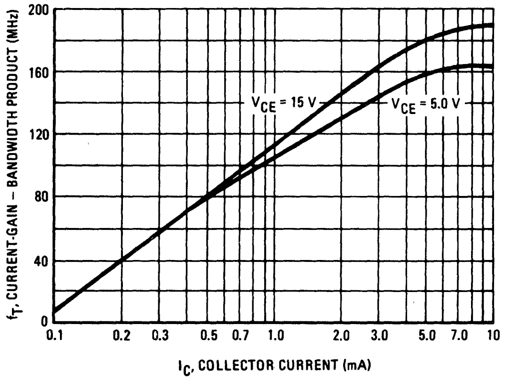
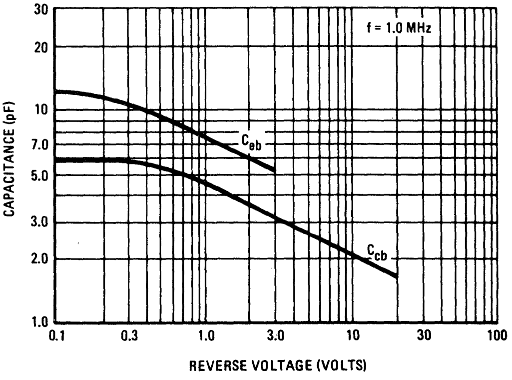


FIGURE 6 – CAPACITANCES



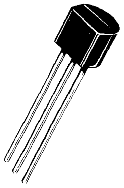
2N5219 (SILICON)

NPN SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose amplifier applications.

- Low Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$ = 0.4 Vdc (Max) @ I_C = 10 mAdc
- High Current-Gain—Bandwidth Product
  f_T = 150 MHz (Min) @ I_C = 10 mAdc
- Low Collector-Base Capacitance
  C_{cb} = 4.0 pF (Max) @ V_{CE} = 10 Vdc

NPN SILICON AMPLIFIER TRANSISTOR



*MAXIMUM RATINGS

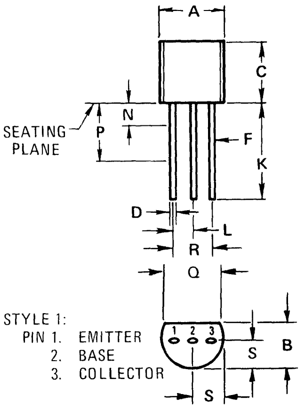
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	20	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	100	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	15	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	20	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.0	-	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	-	100	nAdc
Emitter Cutoff Current (V_{BE} = 2.0 Vdc, I_C = 0)	I_{EBO}	-	500	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	35	500	-
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	-	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	150	-	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	-	4.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	35	1500	-

* Indicates JEDEC Registered Data

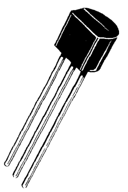
2N5220 (SILICON)

NPN SILICON ANNULAR TRANSISTOR

. . . designed for low-power, large signal audio and general-purpose amplifier applications. Complements PNP type 2N5221.

- Low Saturation Voltage – $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 150 mAdc, I_B = 15 mAdc

NPN SILICON AMPLIFIER TRANSISTOR



*MAXIMUM RATINGS

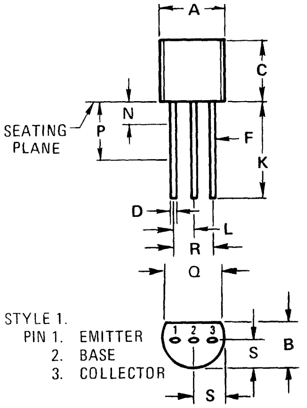
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	15	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 1.
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	15	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	15	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.0	-	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	-	100	nAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	-	100	nAdc
ON CHARACTERISTICS(1)				
DC Current Gain	h_{FE}			-
(I_C = 10 mAdc, V_{CE} = 10 Vdc)		25	-	
(I_C = 50 mAdc, V_{CE} = 10 Vdc)		30	600	
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$	-	0.5	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$	-	1.1	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	100	-	MHz
Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	-	10	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	30	1800	-

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

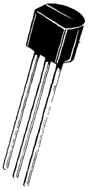
2N5221 (SILICON)

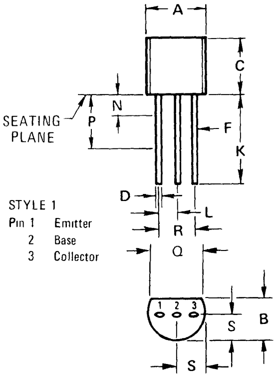
PNP SILICON ANNULAR TRANSISTOR

. . . designed for low-power, large signal audio and general-purpose amplifier applications. Complements NPN type 2N5220.

- Low Saturation Voltage – $V_{CE(sat)}$ = 0.5 Vdc (Max)
  @ I_C = 150 mAdc, I_B = 15 mAdc

PNP SILICON AMPLIFIER TRANSISTOR





STYLE 1
Pin 1 Emitter
2 Base
3 Collector

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	15	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 350 2.8 2.73	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +135 -55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	15	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	15	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.0	–	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	100	nAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 25 30	 – 600	–
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$	–	1.1	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	100	–	MHz
Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	15	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	30	1800	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leqslant$300 μs, Duty Cycle $\leqslant$2.0%.

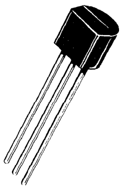
2N5222 (SILICON)

NPN SILICON ANNULAR TRANSISTOR

. . . designed for RF amplifier, mixer, and video IF applications.

- High Current-Gain—Bandwidth Product – f_T = 450 MHz (Min) @ I_C = 4.0 mAdc
- Collector-Emitter Saturation Voltage – V_{CE} = 1.0 Vdc (Max) @ I_C = 4.0 mAdc
- Low Collector-Base Capacitance – C_{cb} = 1.3 pF (Max) @ V_{CB} = 10 Vdc

NPN SILICON
AMPLIFIER TRANSISTOR



*MAXIMUM RATINGS

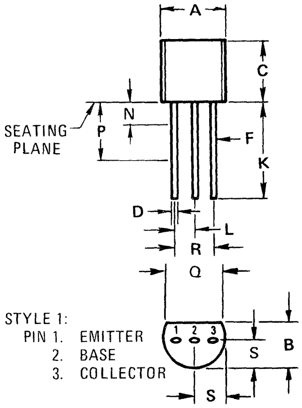
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	20	Vdc
Emitter-Base Voltage	V_{EB}	2.0	Vdc
Collector Current – Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

* ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	15	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	20	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	2.0	-	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	-	100	nAdc
Emitter Cutoff Current (V_{BE} = 2.0 Vdc, I_C = 0)	I_{EBO}	-	100	nAdc
ON CHARACTERISTICS				
DC Current Gain(1) (I_C = 4.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	1500	-
Collector-Emitter Saturation Voltage (I_C = 4.0 mAdc, I_B = 400 μAdc)	$V_{CE(sat)}$	-	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 4.0 mAdc, I_B = 400 μAdc)	$V_{BE(sat)}$	-	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 4.0 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	450	-	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	-	1.3	pF
Small-Signal Current Gain (I_C = 4.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	20	3000	-

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

COMMON-BASE y PARAMETERS versus FREQUENCY

(V_{CB} = 10 Vdc, I_C = 4.0 mAdc, T_A = 25°C)

y_{ib}, INPUT ADMITTANCE

FIGURE 1 – RECTANGULAR FORM

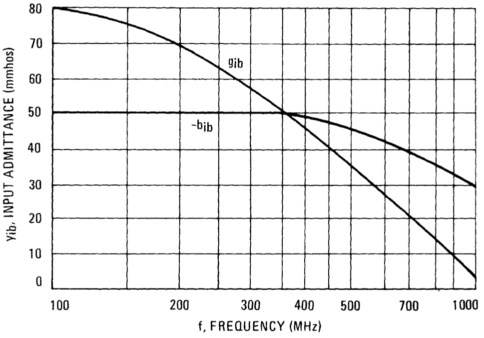
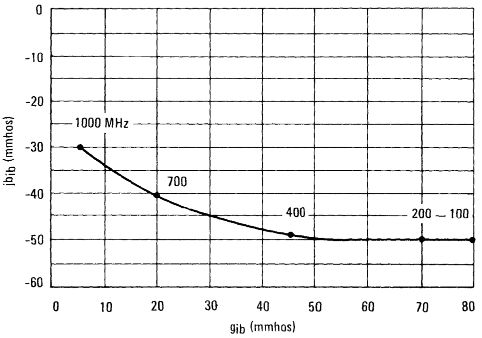


FIGURE 2 – POLAR FORM



y_{fb}, FORWARD TRANSFER ADMITTANCE

FIGURE 3 – RECTANGULAR FORM

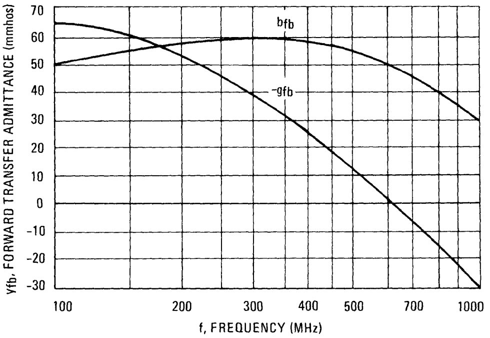
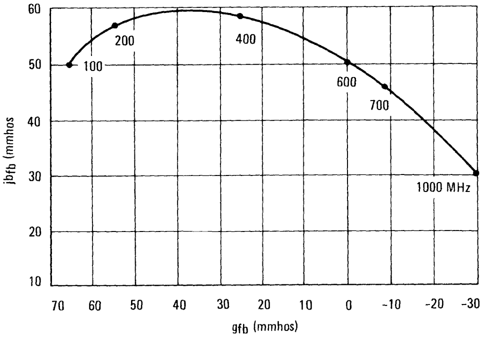


FIGURE 4 – POLAR FORM



COMMON-BASE y PARAMETERS versus FREQUENCY

(V_{CB} = 10 Vdc, I_C = 4.0 mAdc, T_A = 25°C)

y_{rb}, REVERSE TRANSFER ADMITTANCE

FIGURE 5 – RECTANGULAR FORM

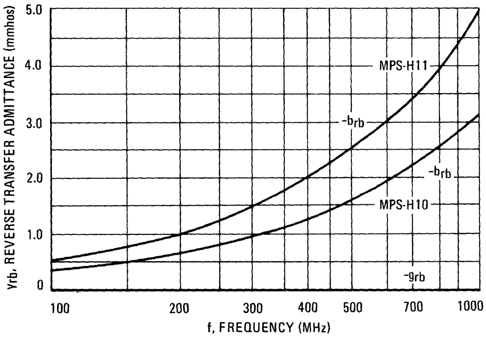
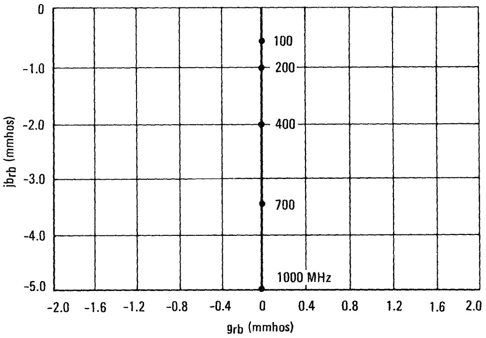


FIGURE 6 – POLAR FORM



y_{ob}, OUTPUT ADMITTANCE

FIGURE 7 – RECTANGULAR FORM

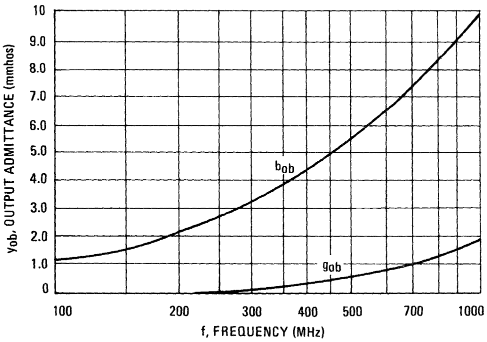
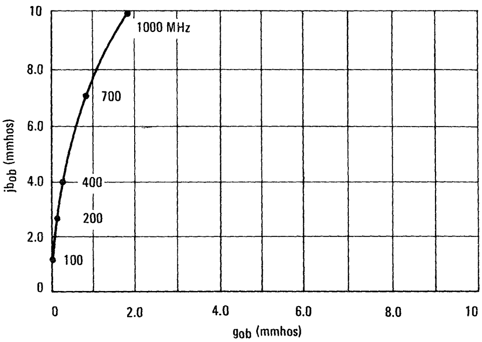


FIGURE 8 – POLAR FORM



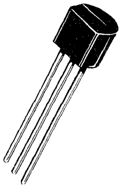
2N5223 (SILICON)

NPN SILICON AMPLIFIER TRANSISTOR

. . . designed for low-level, small-signal, general-purpose amplifier applications.

- High Current-Gain—Bandwidth Product
  f_T = 150 MHz (Min) @ I_C = 10 mAdc –
- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 10 mAdc
- Collector-Base Capacitance –
  C_{cb} = 4.0 pF (Max) @ V_{CB} = 10 Vdc

NPN SILICON AMPLIFIER TRANSISTOR



*MAXIMUM RATINGS

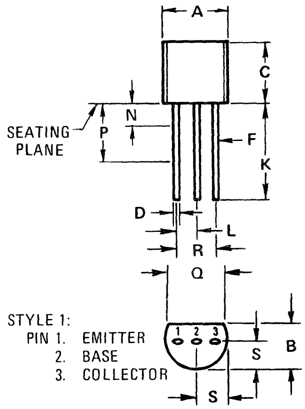
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CB}	25	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	100	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	20	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	25	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.0	-	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	-	100	nAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	-	500	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	50	800	-
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	-	0.7	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	-	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	150	-	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	-	4.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	50	1600	-

* Indicates JEDEC Registered Data

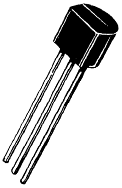
2N5224 (SILICON)

NPN SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose, low-level switching applications.

- Current Gain Specified at 10 mAdc and 100 mAdc
- Complete Switching Specification
- Low Collector-Base Capacitance —
  C_{cb} = 4.0 pF (Max) @ V_{CB} = 5.0 Vdc

NPN SILICON
SWITCHING
TRANSISTOR



***MAXIMUM RATINGS**

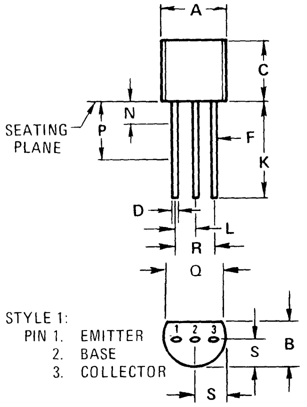
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CB}	25	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

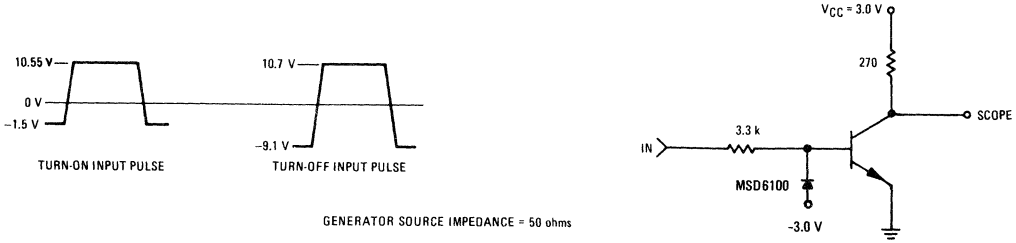
* ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)		BV_{CEO}	12	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	25	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)		I_{CBO}	-	500	nAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)		I_{EBO}	-	100	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			-
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			40	400	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)(1)			15	-	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 3.0 mAdc)		$V_{CE(sat)}$	-	0.35	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 3.0 mAdc)		$V_{BE(sat)}$	-	0.9	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)		f_T	250	-	MHz
Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	-	4.0	pF
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 3.0 Vdc, $V_{BE(off)}$ = 1.5 Vdc I_C = 10 mAdc, I_{B1} = 3.0 mAdc)	t_d	-	25	ns
Rise Time		t_r	-	20	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mA, I_{B1} = I_{B2} = 3.0 mAdc)	t_s	-	35	ns
Fall Time		t_f	-	25	ns

(1)Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

* Indicates JEDEC Registered Data.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT



GENERATOR SOURCE IMPEDANCE = 50 ohms

INPUT PULSE:
RISE TIME ⩽ 2.0 ns
FALL TIME ⩽ 2.0 ns
NOMINAL PULSEWIDTH = 300 ns
NOMINAL DUTY CYCLE = 2.0%

OSCILLOSCOPE:
RISE TIME ⩽ 0.4 ns
INPUT RESISTANCE ⩾ 50 ohms
INPUT CAPACITANCE ⩽ 4.0 pF

For t_d and t_r, diode is disconnected.

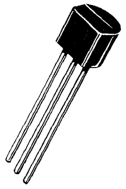
2N5225 (SILICON)

NPN SILICON ANNULAR TRANSISTOR

. . . designed for general purpose amplifier applications and for complementary circuitry with types 2N5226.

- Collector-Emitter Breakdown Voltage — BV_{CEO} = 25 Volts (Min)
- Current Gain Specified at 10 mA and 50 mA
- Collector-Base Capacitance — C_{cb} = 20 pF (Max)

NPN SILICON AMPLIFIER TRANSISTOR



*MAXIMUM RATINGS

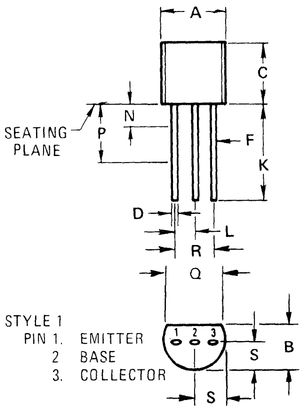
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CB}	25	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Power Dissipation @ $T_A = 25^\circ C$ Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	25	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	25	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	4.0	-	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	-	300	nAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	-	500	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			-
(I_C = 10 mAdc, V_{CE} = 10 Vdc)		25	-	
(I_C = 50 mAdc, V_{CE} = 10 Vdc)		30	600	
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	-	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{BE(sat)}$	-	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	50	-	MHz
Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	-	20	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	30	1800	-

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

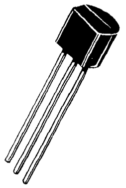
2N5226 (SILICON)

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general purpose amplifier applications and for complementary circuitry with the 2N5225.

- Collector-Emitter Breakdown Voltage — BV_{CEO} = 25 Volts (Min) @ I_C = 10 mAdc
- Current Gain Specified at 10 mA and 50 mA
- Collector-Base Capacitance — C_{cb} = 20 pF (Max) @ V_{CB} = 5.0 Vdc

PNP SILICON
AMPLIFIER
TRANSISTOR



*MAXIMUM RATINGS

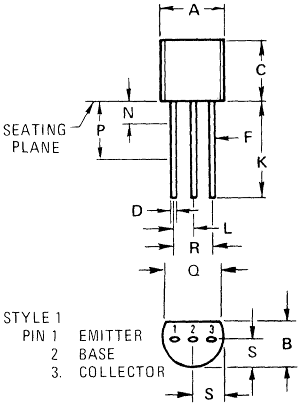
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CB}	25	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	25	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	25	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	4.0	-	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	-	300	nAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	-	500	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 25 30	 - 600	-
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	-	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{BE(sat)}$	-	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	50	-	MHz
Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	-	20	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	30	1800	-

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

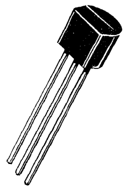
2N5227 (SILICON)

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose amplifier applications.

- Current Gain Specified at 100 μAdc and 2.0 mAdc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.4 Vdc (Max) @ I_C = 10 mAdc
- Collector-Base Capacitance —
  C_{cb} = 5.0 pF (Max) @ V_{CB} = 10 Vdc

PNP SILICON
AMPLIFIER
TRANSISTOR



*MAXIMUM RATINGS

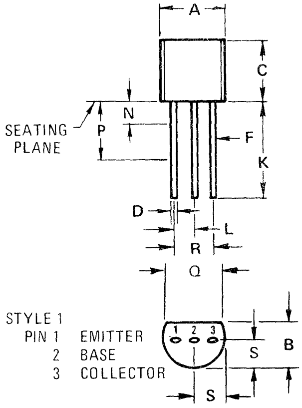
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	30	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	30	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.0	-	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	-	100	nAdc
Emitter Cutoff Current (V_{BE} = 2.0 Vdc, I_C = 0)	I_{EBO}	-	500	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 100 μAdc, V_{CE} = 10 Vdc) (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30 50	- 700	-
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	-	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	100	-	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	-	5.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	50	1500	-

*Indicates JEDEC Registered Data

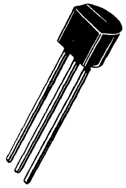
2N5228 (SILICON)

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general purpose switching applications.

- Current Gain Specified at 10 mA and 50 mA
- Collector-Base Capacitance — C_{cb} = 5.0 pF (Max)

PNP SILICON SWITCHING TRANSISTOR



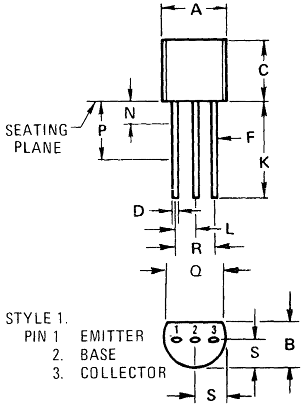
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	5.0	Vdc
Collector-Base Voltage	V_{CB}	5.0	Vdc
Collector-Emitter Voltage	V_{CES}	6.0	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.
*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

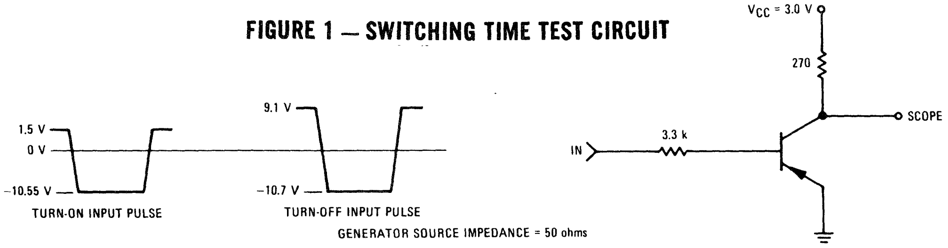
*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	5.0	-	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)	BV_{CES}	6.0	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	5.0	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.0	-	Vdc
Collector Cutoff Current (V_{CE} = 4.0 Vdc, V_{BE} = 0)	I_{CES}	-	100	nAdc
Emitter Cutoff Current (V_{BE} = 2.5 Vdc, I_C = 0)	I_{EBO}	-	100	μAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			-
(I_C = 10 mAdc, V_{CE} = 0.3 Vdc)		30	-	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (1)		15	-	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 3.0 mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 3.0 mAdc)	$V_{BE(sat)}$	0.65	1.25	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	300	-	MHz
Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	-	5.0	pF
SWITCHING CHARACTERISTICS				
Delay Time (V_{CC} = 3.0 Vdc, $V_{BE(off)}$ = 1.5 Vdc I_C = 10 mAdc, I_{B1} = 3.0 mAdc)	t_d	-	25	ns
Rise Time	t_r	-	50	ns
Storage Time (V_{CC} = 3.0 Vdc, I_C = 10 mA, I_{B1} = I_{B2} = 3.0 mAdc)	t_s	-	90	ns
Fall Time	t_f	-	50	ns

(1)Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

* Indicates JEDEC Registered Data.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT



GENERATOR SOURCE IMPEDANCE = 50 ohms

INPUT PULSE:
RISE TIME ≤ 2.0 ns
FALL TIME ≤ 2.0 ns
NOMINAL PULSEWIDTH = 300 ns
NOMINAL DUTY CYCLE = 2.0%

OSCILLOSCOPE:
RISE TIME ≤ 0.4 ns
INPUT RESISTANCE ≥ 50 ohms
INPUT CAPACITANCE ≤ 4.0 pF

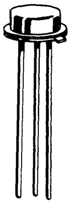
2N5229 (SILICON)
2N5230
2N5231

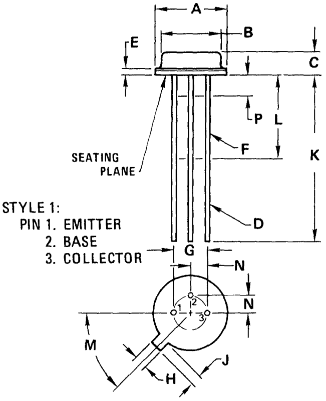
PNP SILICON ANNULAR TRANSISTORS

. . . designed for low-level, chopper applications requiring high speed operation. This series of devices offers excellent characteristics for use in servo-loop, sensing instrumentation and control amplifier for motor drive systems. These transistors can also be used as replacement devices for alloy-type transistors where high BV_{EBO} is required.

- Low Offset Voltage – $V_{EC(off)}$ = 0.5 mVdc (Max) @ I_B = 100 μAdc
- Low Dynamic "ON" Series Resistance – $r_{ec\,(ON)}$ = 6.0 Ohms (Max) @ I_B = 1.0 mAdc
- Space Saving TO-46 Package

PNP SILICON CHOPPER TRANSISTORS





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	1.65	2.16	0.065	0.085
D	0.406	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.305	0.483	0.012	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC dimensions and notes apply

CASE 26-03
TO-46

MAXIMUM RATINGS

Rating	Symbol	2N5229	2N5230	2N5231	Unit
*Collector-Emitter Voltage	V_{CEO}	10	20	30	Vdc
*Collector-Base Voltage	V_{CB}	15	30	50	Vdc
*Emitter-Base Voltage	V_{EB}	15	30	50	Vdc
*Collector Current – Continuous	I_C	← 50 →			mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 0.5 → ← 2.86 →			Watt mW/°C
*Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 2.0 → ← 12 →			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

*Indicates JEDEC Registered Data.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Emitter-Collector Breakdown Voltage		BV_{ECO}			Vdc
(I_E = 10 µAdc, I_B = 0)	2N5229		10	–	
	2N5230		20	–	
	2N5231		30	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 10 µAdc, I_E = 0)	2N5229		15	–	
	2N5230		30	–	
	2N5231		50	–	
Emitter-Base Breakdown Voltage		BV_{EBO}			Vdc
(I_E = 10 µAdc, I_C = 0)	2N5229		15	–	
	2N5230		30	–	
	2N5231		50	–	
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 12 Vdc, I_E = 0)	2N5229		–	1.0	
(V_{CB} = 25 Vdc, I_E = 0)	2N5230		–	1.0	
(V_{CB} = 40 Vdc, I_E = 0)	2N5231		–	1.0	
Emitter Cutoff Current		I_{EBO}			nAdc
(V_{EB} = 12 Vdc, I_C = 0)	2N5229		–	1.0	
(V_{EB} = 25 Vdc, I_C = 0)	2N5230		–	1.0	
(V_{EB} = 40 Vdc, I_C = 0)	2N5231		–	1.0	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 100 µAdc, V_{CE} = 1.0 Vdc)			50	–	
(I_C = 200 µAdc, V_{CE} = 0.5 Vdc) (Inverted Connection)			15	–	
Offset Voltage		$V_{EC\,(off)}$			mVdc
(I_B = 100 µAdc, I_E = 0)	2N5229,2N5230		–	0.5	
	2N5231		–	0.8	
(I_B = 1.0 mAdc, I_E = 0)	2N5229		–	0.8	
	2N5230,2N5231		–	1.0	
DYNAMIC CHARACTERISTICS					
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz)		C_{cb}	–	5.0	pF
Emitter-Base Capacitance (V_{EB} = 10 Vdc, I_C = 0, f = 140 kHz)		C_{eb}	–	4.0	pF
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 4.0 MHz)		h_{fe}	2.0	–	–
"ON" Series Resistance		$r_{ec\,(on)}$			Ohms
(I_B = 1.0 mAdc, I_E = 0, I_e = 100 µA (RMS), f = 1.0 kHz)	2N5229		1.0	6.0	
	2N5230		2.0	8.0	
	2N5231		2.0	10	

*Indicates JEDEC Registered Data.

TYPICAL CHARACTERISTICS

FIGURE 1 – EMITTER-COLLECTOR VOLTAGE versus BASE CURRENT

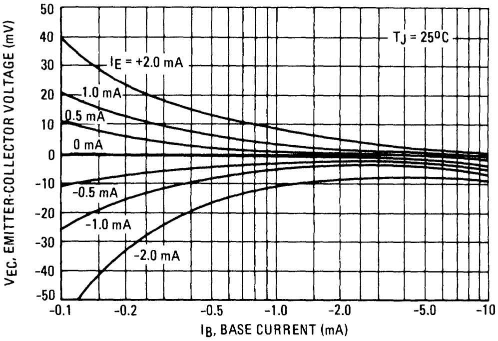


FIGURE 2 – EMITTER-COLLECTOR VOLTAGE versus JUNCTION TEMPERATURE

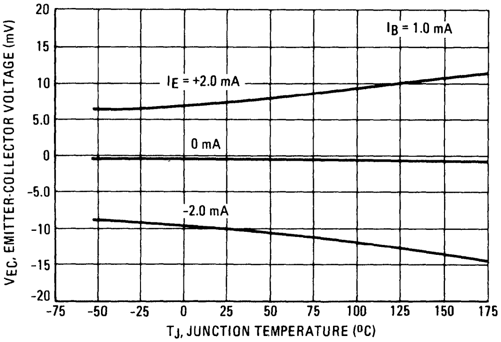


FIGURE 3 – EMITTER-COLLECTOR "ON" RESISTANCE versus BASE CURRENT

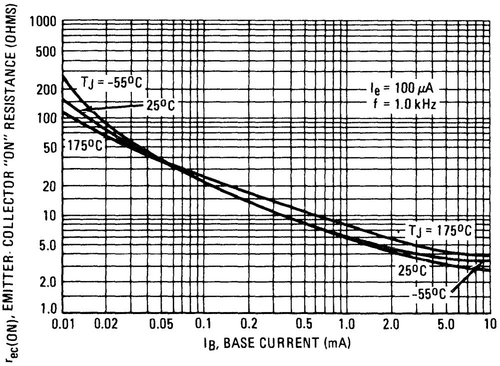


FIGURE 4 – EMITTER-COLLECTOR "ON" RESISTANCE TEMPERATURE COEFFICIENT versus BASE CURRENT

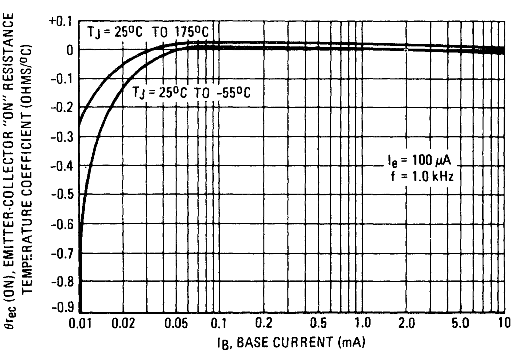


FIGURE 5 – CURRENT GAIN versus COLLECTOR CURRENT

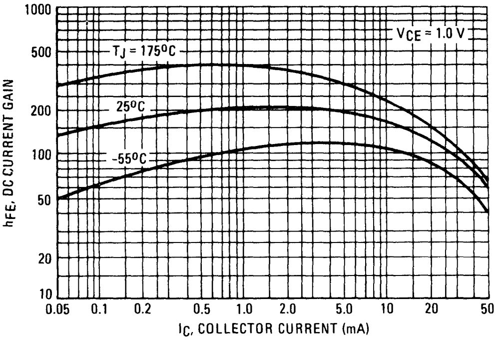


FIGURE 6 – CURRENT GAIN (Inverted Connection) versus EMITTER CURRENT

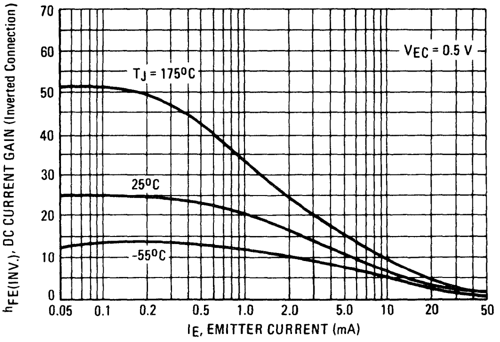


FIGURE 7 – COLLECTOR CUTOFF CURRENT versus JUNCTION TEMPERATURE

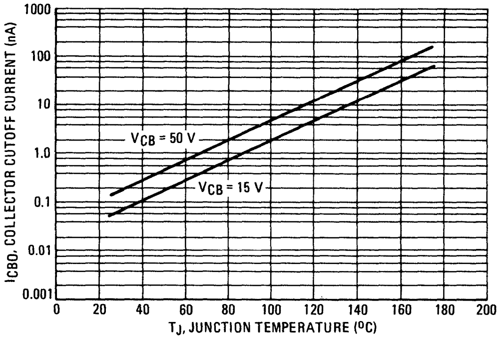


FIGURE 8 – EMITTER CUTOFF CURRENT versus JUNCTION TEMPERATURE

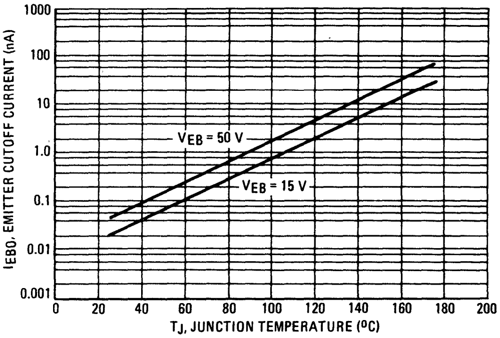


FIGURE 9 – COLLECTOR-EMITTER SATURATION VOLTAGE versus COLLECTOR CURRENT

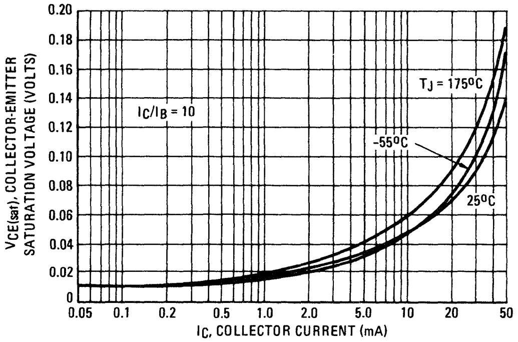
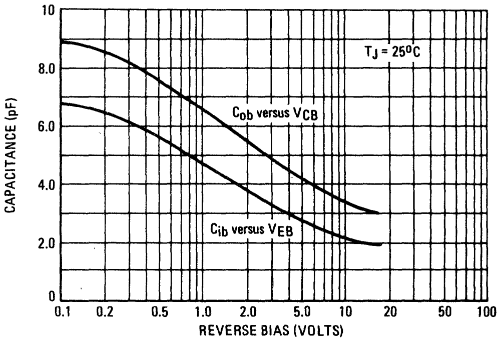


FIGURE 10 – JUNCTION CAPACITANCE versus REVERSE BIAS VOLTAGE



2N5241 (SILICON)

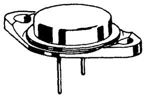
HIGH VOLTAGE NPN SILICON TRANSISTOR

. . . designed for use in high-voltage switching regulators, inverters, converters and line operated amplifiers.

- High Collector-Emitter Voltage – 400 Volts
- DC Current Gain –
  h_{FE} = 10 (Min) @ I_C = 3.5 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 2.5 Adc
- Switching Times – @ I_C = 2.5 Adc
  t_{on} = 0.8 μs (Max)
  t_{off} = 1.7 μs (Max)

5.0 AMPERE
POWER TRANSISTOR
NPN SILICON

400 VOLTS
125 WATTS



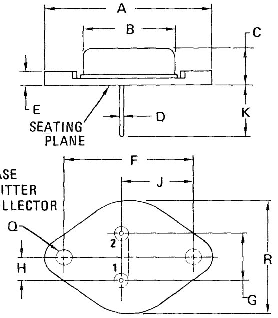
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Base Voltage	V_{CB}	400	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 62.5°C Derate above 62.5°C	P_D	125 1.43	Watts W/°C
Operating Junction Temperature Range	T_J	-65 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

*Indicates JEDEC Registered Data



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$BV_{CEO(sus)}$	325	–	Vdc
Collector Cutoff Current (V_{CE} = 400 Vdc, I_B = 0)	I_{CEO}	–	2.5	mAdc
Collector Cutoff Current	I_{CEX}			mAdc
(V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc)		–	0.5	
(V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)		15	35	
(I_C = 3.5 Adc, V_{CE} = 5.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 2.5 Adc, I_B = 0.5 Adc)		–	0.7	
(I_C = 5.0 Adc, I_B = 1.0 Adc)		–	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 2.5 Adc, I_B = 0.5 Adc)		–	1.5	
(I_C = 5.0 Adc, I_B = 1.0 Adc)		–	2.0	
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 12 Vdc, f = 1.0 MHz)	f_T	2.5	–	MHz
SWITCHING CHARACTERISTICS				
Turn-On Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = 0.25 Adc)	t_{on}	–	0.8	μs
Turn-Off Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = 0.25 Adc, I_{B2} = 0.5 Adc)	t_{off}	–	1.7	μs
Pulse Energy Test (V_{CC} = 200 Vdc, I_C = 0.3 Adc, t_p = 5.0 ms, Duty Cycle = 1.0%)	–	300	–	mJ

FIGURE 1 – COLLECTOR-EMITTER SUSTAINING VOLTAGE TEST CIRCUIT AND WAVEFORM

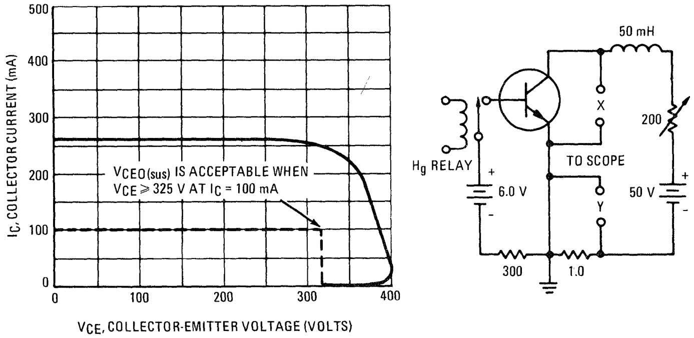
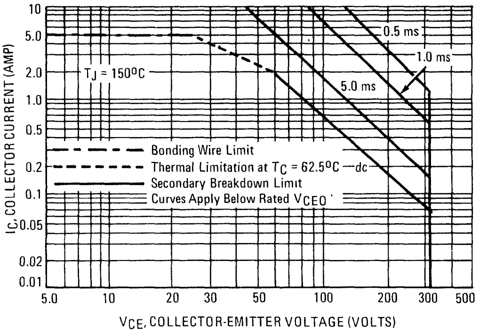


FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 3 – DC CURRENT GAIN

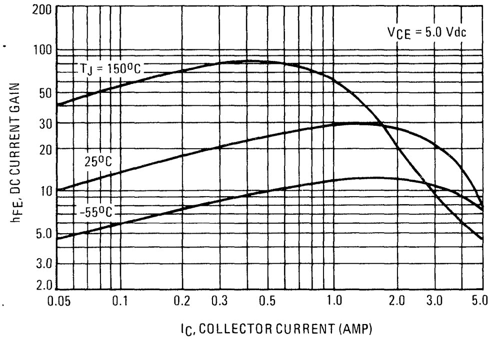


FIGURE 4 – "ON" VOLTAGES

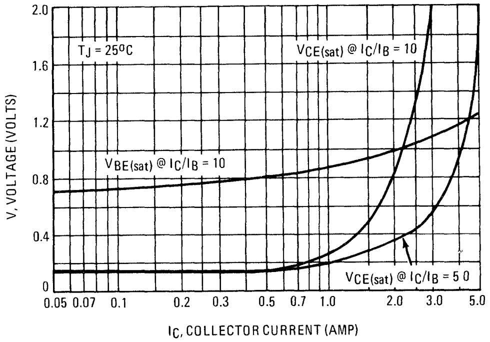
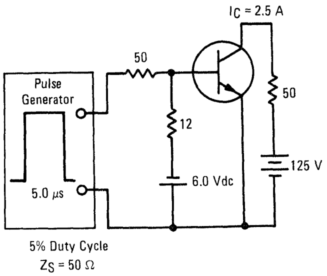


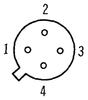
FIGURE 5 – SWITCHING CIRCUIT



2N5265 thru 2N5270 (SILICON)

P-Channel junction depletion mode (Type A) field-effect transistors designed for general-purpose amplifier applications.

CASE 20(5)
(TO-72)



STYLE 5
PIN 1. SOURCE
2. GATE 1
3. DRAIN
4. CASE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	Vdc
Drain-Gate Voltage	V_{DG}	60	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	60	Vdc
Drain Current	I_D	20	mAdc
Gate Current-forward	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 2.0	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C
Operating Junction Temperature Range	T_J	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	60	-	Vdc
Gate-Source Cutoff Voltage	$V_{GS(off)}$			Vdc
(V_{DS} = 15 Vdc, I_D = 1.0 μAdc) 2N5265, 2N5266		-	3.0	
2N5267, 2N5268		-	6.0	
2N5269, 2N5270		-	8.0	
Gate Reverse Current	I_{GSS}			
(V_{GS} = 30 Vdc, V_{DS} = 0)		-	2.0	nAdc
(V_{GS} = 30 Vdc, V_{DS} = 0, T_A = 150°C)		-	2.0	μAdc
ON CHARACTERISTICS				
Zero-Gate Voltage Drain Current	I_{DSS}			mAdc
(V_{DS} = 15 Vdc, V_{GS} = 0) 2N5265		0.5	1.0	
2N5266		0.8	1.6	
2N5267		1.5	3.0	
2N5268		2.5	5.0	
2N5269		4.0	8.0	
2N5270		7.0	14	
Gate-Source Voltage	V_{GS}			Vdc
(V_{DS} = 15 Vdc, I_D = 0.05 mAdc) 2N5265		0.3	1.5	
(V_{DS} = 15 Vdc, I_D = 0.08 mAdc) 2N5266		0.4	2.0	
(V_{DS} = 15 Vdc, I_D = 0.15 mAdc) 2N5267		1.0	4.0	
(V_{DS} = 15 Vdc, I_D = 0.25 mAdc) 2N5268		1.0	4.0	
(V_{DS} = 15 Vdc, I_D = 0.4 mAdc) 2N5269		2.0	6.0	
(V_{DS} = 15 Vdc, I_D = 0.7 mAdc) 2N5270		2.0	6.0	
SMALL-SIGNAL CHARACTERISTICS				
Forward Transadmittance	$\|y_{fs}\|$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz) 2N5265		900	2700	
2N5266		1000	3000	
2N5267		1500	3500	
2N5268		2000	4000	
2N5269		2200	4500	
2N5270		2500	5000	
Forward Transconductance	$Re(y_{fs})$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz) 2N5265		800	-	
2N5266		900	-	
2N5267		1400	-	
2N5268		1700	-	
2N5269		1900	-	
2N5270		2100	-	
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{os}\|$	-	75	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	-	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	-	2.0	pF
Common-Source Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 M ohm, f = 100 Hz, BW = 1.0 Hz)	NF	-	2.5	dB
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)	e_n	-	115	nV/$\sqrt{Hz}$

FIGURE 1–6 TRANSFER CHARACTERISTIC CURVES
FOR MIN/MAX I_{DSS} LIMITS

FIGURE 1

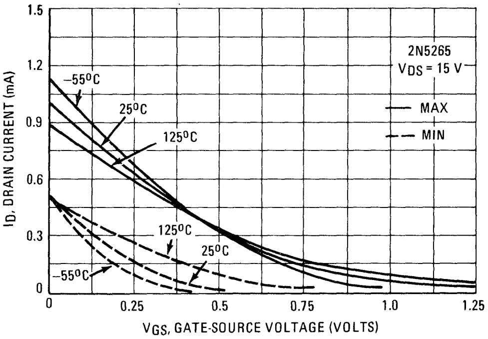


FIGURE 2

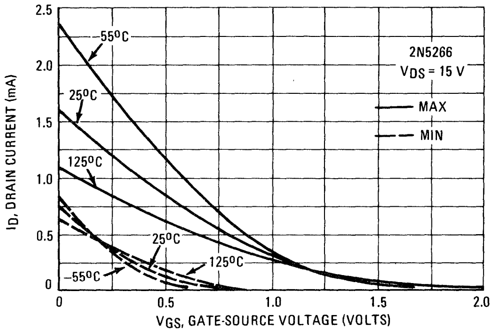


FIGURE 3

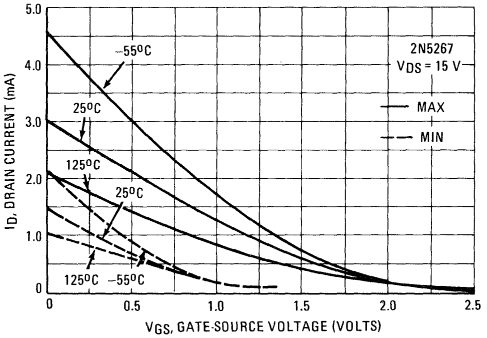


FIGURE 4

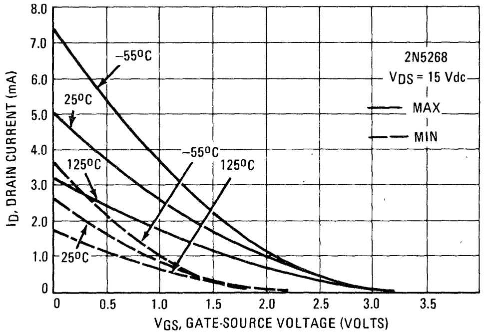


FIGURE 5

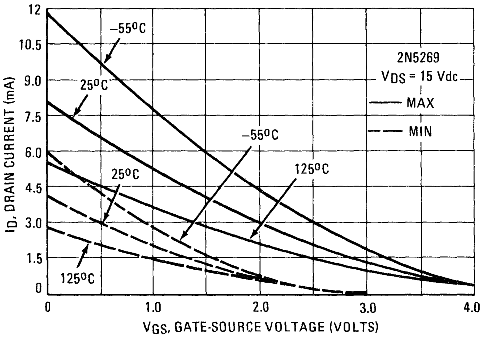
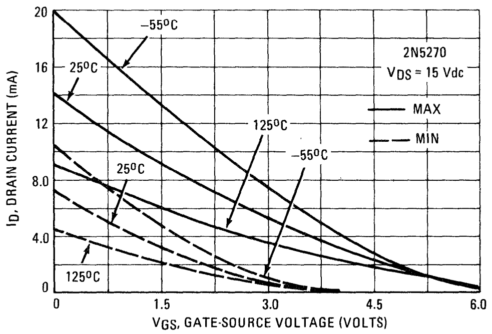


FIGURE 6



FIGURES 7-12 – TYPICAL AND MINIMUM FORWARD TRANSFER ADMITTANCE

FIGURE 7

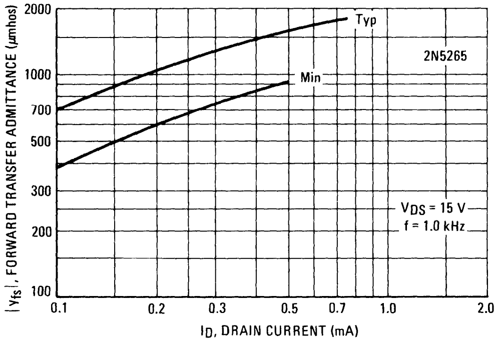


FIGURE 8

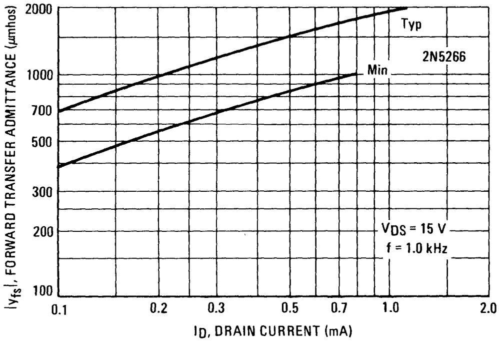


FIGURE 9

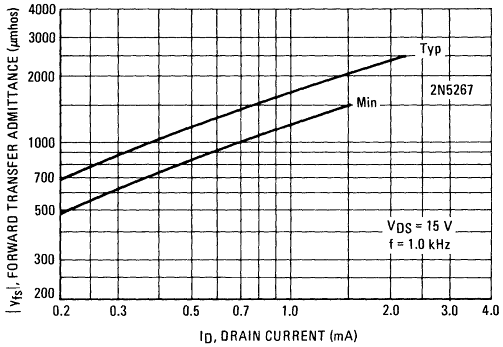


FIGURE 10

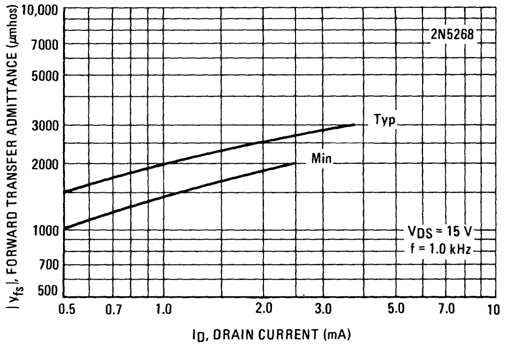


FIGURE 11

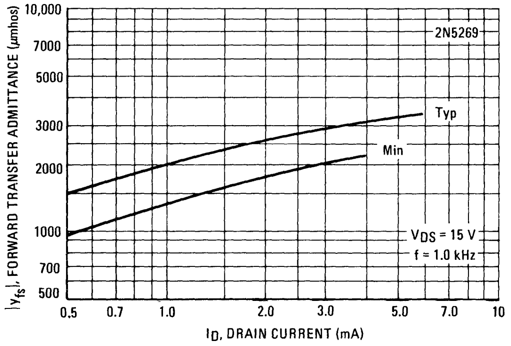
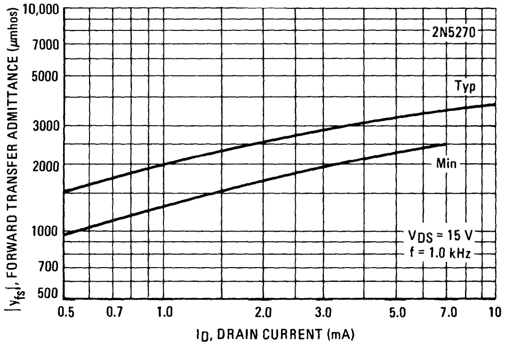


FIGURE 12



TYPICAL CURVES

FIGURE 13 – OUTPUT RESISTANCE versus DRAIN CURRENT

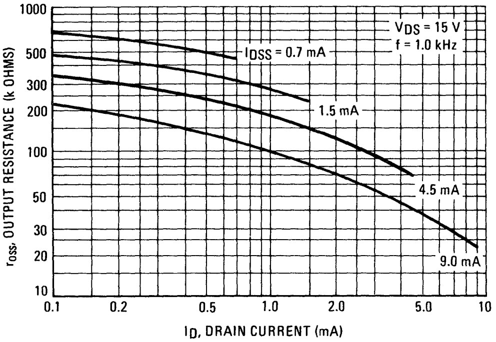


FIGURE 14 – CAPACITANCE versus DRAIN-SOURCE VOLTAGE

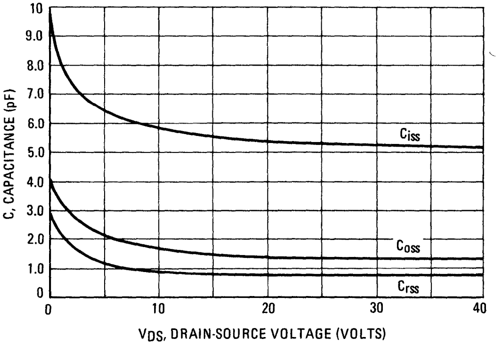


FIGURE 15 – NOISE FIGURE versus FREQUENCY

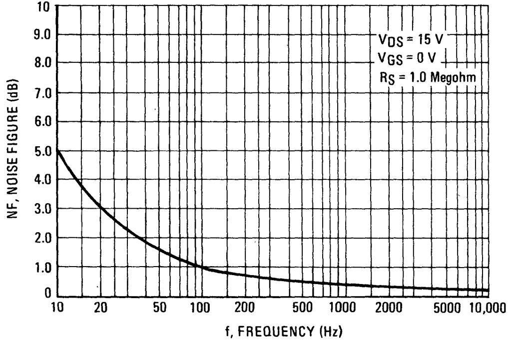


FIGURE 16 – NOISE FIGURE versus SOURCE RESISTANCE

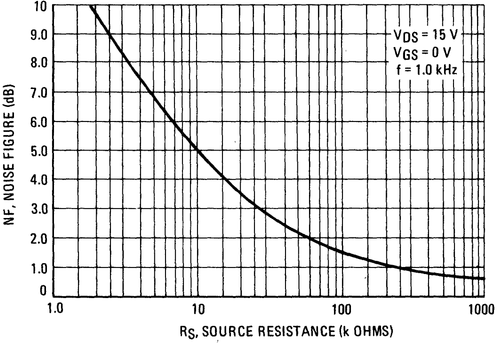


FIGURE 17 – DRAIN CURRENT TEMPERATURE COEFFICIENT versus DRAIN CURRENT

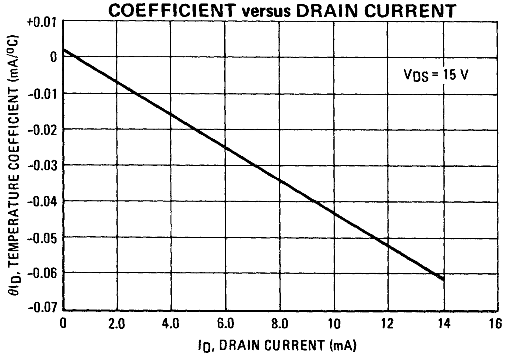


FIGURE 18 – FORWARD TRANSADMITTANCE COEFFICIENT versus DRAIN CURRENT

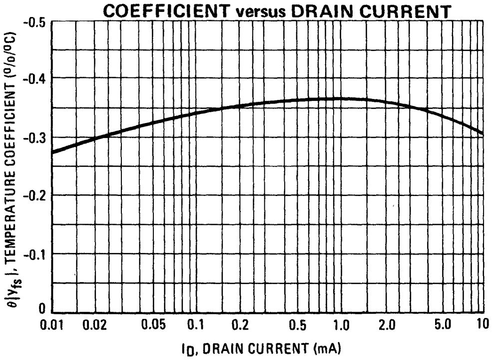
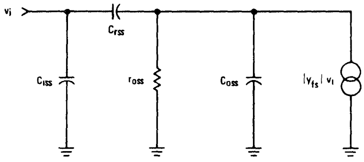


FIGURE 19 – EQUIVALENT LOW FREQUENCY CIRCUIT



Common Source
y Parameters for Frequencies
Below 30 MHz

$y_{is} = j\omega C_{iss}$
$y_{os} = j\omega C_{osp}^{*} + 1/r_{oss}$
$y_{fs} = |y_{fs}|$
$y_{rs} = -j\omega C_{rss}$

$^{*}C_{osp}$ is C_{oss} in parallel with Series Combination of C_{iss} and C_{rss}

BIAS NETWORK DESIGN FOR WORST CASE I_{DSS} VARIANCE

This Designers Data Sheet has been published to assist the circuit designer in optimizing his "worst case" design. The following example illustrates the use of the forward transfer characteristics curves (Pigures 1 thru 6) in the design of a typical bias network.

Given: V_{DD} = -30 Vdc, I_D = 1.0 ± 0.25 mAdc from -55°C to +125°C

Procedure: The 2N5268 "worst case" bias conditions across the temperature range (from Figure 4) are reproduced in Figure A. The first step in the bias network design is to determine the value of the source resistance (R_S) necessary to hold the ± 0.25 mAdc I_D bias tolerance. To solve R_S, plot $I_{D(max)}$ and $I_{D(min)}$ on Figure A and calculate R_S, and V_G.

$$R_S = \frac{V_{GS(max)} - V_{GS(min)}}{I_{D(max)} - I_{D(min)}} = \frac{1.9\text{ Vdc} - 0.8\text{ Vdc}}{(1.25\text{ mA} - 0.75\text{ mA})} = 2.2\text{ k Ohms}$$

$$V_G = \frac{I_{D(max)}\, V_{GS(min)} - I_{D(min)}\, V_{GS(max)}}{I_{D(max)} - I_{D(min)}}$$

$$= \frac{1.25 \times 0.80 - 0.75 \times 1.9}{0.5} = -0.9\text{ Vdc}$$

In Figure B the maximum allowable value for R_1 will be determined by loading due to gate reverse current. Gate reverse current variations with temperature follow the pattern of all silicon devices, and, as a rule, we can assume that it will double with each 15°C temperature rise. Therefore, we can assume a maximum reverse current of approximately 0.5 µAdc at 125°C, based on the specified maximum 2.0 µAdc reverse at 150°C. The variation in V_G bias versus temperature will not be too great if we chose a value for R_1 which results in a bias network current (I_1 in Figure B) greater than 5 times the maximum reverse current. Assuming a value for R_1 of 9.1 Megohms, R_2 can be solved from the equation:

$$V_G = -0.9\text{ Vdc} \approx \frac{-30\, R_2}{9.1 + R_2} \quad (\text{Ignoring } I_G)$$

$$R_2 \approx 300\text{ k Ohms}$$

Using the above values of R_1 and R_2, the variation in V_G can be computed for I_G = 0 to I_G = 0.5 µAdc. V_G will vary from 0.81 Vdc at I_G = 0.5 µAdc to 0.96 Vdc @ I_G = 0. This variation will have a minimal effect on I_D, as can be seen from Figure A by plotting load lines with a slope equal to $1/R_S$ from V_G = 0.81 Vdc and 0.96 Vdc respectively.

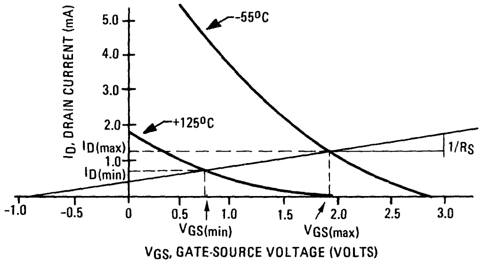


FIGURE A

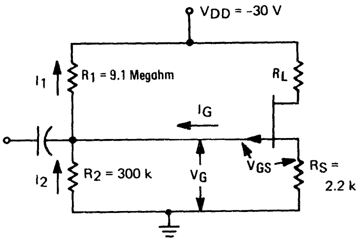


FIGURE B

2N5271 (SILICON)

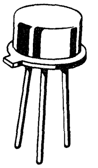
NPN SILICON ANNULAR AVALANCHE TRANSISTOR

. . . designed for AVALANCHE mode operation for the generation of high-current pulses with nanosecond rise times. Ideal for applications such as laser diodes, high-current pulse generators, vacuum tube driver and other applications requiring ultra high-speed, high-voltage or high-current pulses.

- Rise Time — t_r = 1.0 ns (Max)
- Delay Time — t_d = 5.0 ns (Max)
- Output Pulse Amplitude —
  V_O = 130 Vdc (Typ) @ R_L = 50 Ohms

NPN SILICON AVALANCHE SWITCHING TRANSISTOR

$t_r < 1.0$ ns

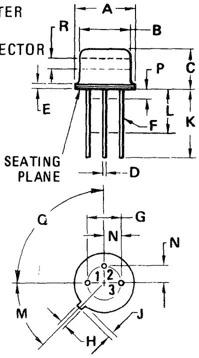


*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Peak	I_C	5.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	600 3.43	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02

TO-39

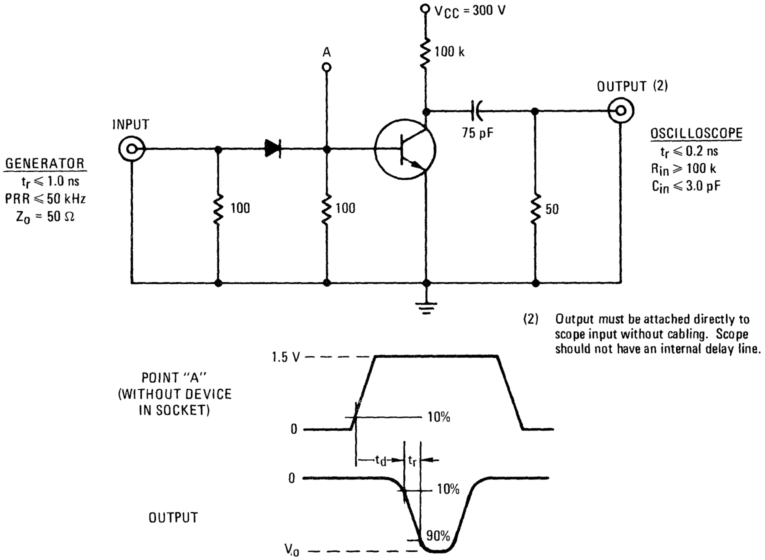
*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 500 μAdc, R_{BE} = 100 Ohms)	BV_{CER}	200	280	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	7.0	–	Vdc
Collector Cutoff Current (V_{CE} = 160 Vdc, R_{BE} = 100 Ohms)	I_{CER}	–	20	nAdc
Collector Holdoff Current(1) (R_{BE} = 100 Ohms, T_A = +55°C)	$I_{CER(H)}$	0.5	–	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	10	nAdc
DYNAMIC CHARACTERISTICS				
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 140 kHz)	C_{cb}	–	6.0	pF
Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 140 kHz)	C_{eb}	–	16	pF
SWITCHING CHARACTERISTICS (Figure 1)				
Delay Time	t_d	–	5.0	ns
Rise Time	t_r	–	1.0	ns
Output Pulse Amplitude (Figure 1)	V_o	100	–	Vdc

*Indicates JEDEC Registered Data.

(1)Collector Holdoff Current is that value of collector cutoff current above which the reverse voltage-current characteristic exhibits negative resistance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



(2) Output must be attached directly to scope input without cabling. Scope should not have an internal delay line.

2N5301 (SILICON)
2N5302
2N5303

HIGH-POWER NPN SILICON TRANSISTORS

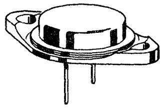
. . . for use in power amplifier and switching circuits applications.

- High Collector-Emitter Sustaining Voltage –
  $BV_{CEO(sus)}$ = 80 Vdc (Min) @ I_C = 200 mAdc (2N5303)
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 10 Adc (2N5301, 2N5302)
  1.0 Vdc (Max) @ I_C = 10 Adc (2N5303)
- Excellent Safe Operating Area –
  200 Watt dc Power Rating to 30 Vdc (2N5303)
- Complements to PNP 2N4398, 2N4399 and 2N5745

20 AND 30 AMPERE
POWER TRANSISTORS

NPN SILICON

40-60-80 VOLTS
200 WATTS



*MAXIMUM RATINGS

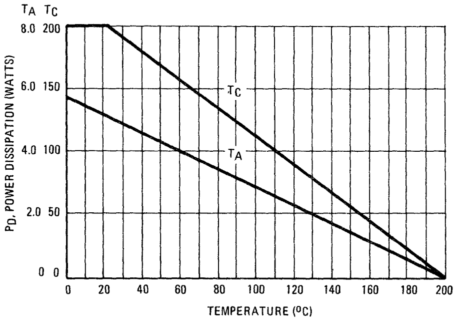
Rating	Symbol	2N5301	2N5302	2N5303	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Collector Current – Continuous	I_C	30	30	20	Adc
Base Current	I_B	← 7.5 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 200 → ← 1.14 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← –65 to +200 →			°C

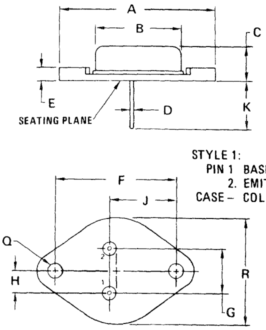
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Case to Ambient	θ_{CA}	34	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1 BASE
2. EMITTER
CASE – COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	–	7.62	–	0.300
D	1.22	1.32	0.048	0.052
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 12-01

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (Note 1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5301		40	–	
	2N5302		60	–	
	2N5303		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5301		–	5.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5302		–	5.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5303		–	5.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5301		–	1.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5302		–	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5303		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5301		–	10	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5302		–	10	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5303		–	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N5301		–	1.0	
(V_{CB} = 60 Vdc, I_E = 0)	2N5302		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5303		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1)		h_{FE}			–
*(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	ALL TYPES		40	–	
*(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5303		15	60	
*(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N5301,2N5302		15	60	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5303		5.0	–	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N5301,2N5302		5.0	–	
*Collector-Emitter Saturation Voltage (Note 1)		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	2N5301,2N5302		–	0.75	
(I_C = 10 Adc, I_B = 1.0 Adc)	2N5303		–	1.0	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5303		–	1.5	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N5301,2N5302		–	2.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5303		–	2.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N5301,2N5302		–	3.0	
*Base-Emitter Saturation Voltage (Note 1)		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	ALL TYPES		–	1.7	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5301,2N5302		–	1.8	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5303		–	2.0	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N5301,2N5302		–	2.5	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5303		–	2.5	
*Base-Emitter On Voltage (Note 1)		$V_{BE(on)}$			Vdc
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5303		–	1.5	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N5301,2N5302		–	1.7	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5303		–	2.5	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N5301,2N5302		–	3.0	
***DYNAMIC CHARACTERISTICS**					
Current-Gain—Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	–	–

***SWITCHING CHARACTERISTICS**

Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	–	1.0	μs
Storage Time		t_s	–	2.0	μs
Fall Time		t_f	–	1.0	μs

*Indicates JEDEC Registered Data.

Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 2 – TURN-ON TIME

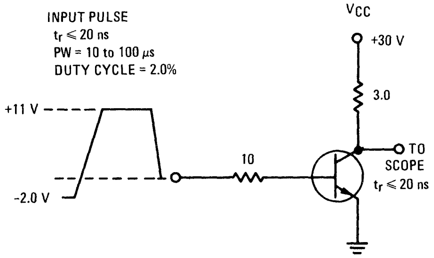


FIGURE 3 – TURN-OFF TIME

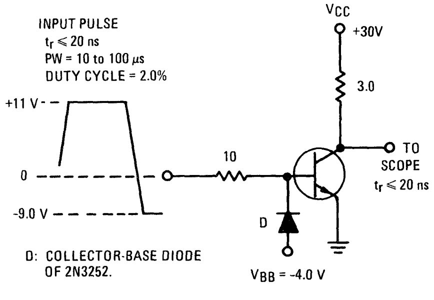


FIGURE 4 – THERMAL RESPONSE

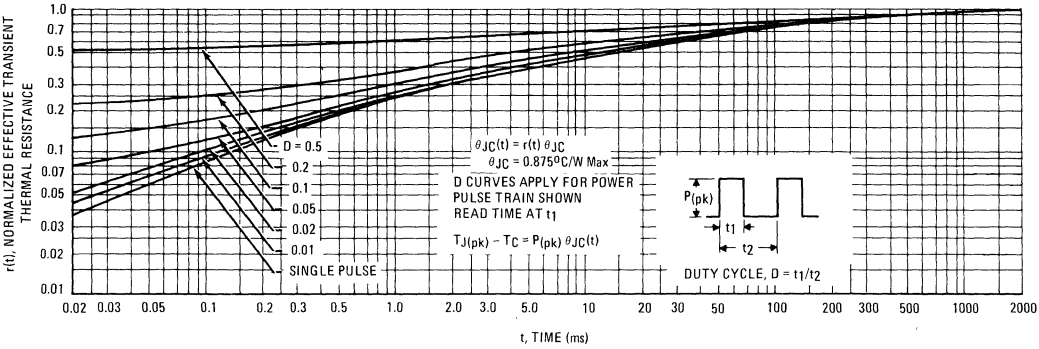


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA

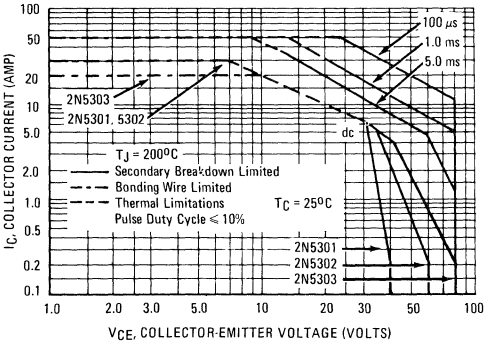


FIGURE 6 – CAPACITANCE versus VOLTAGE

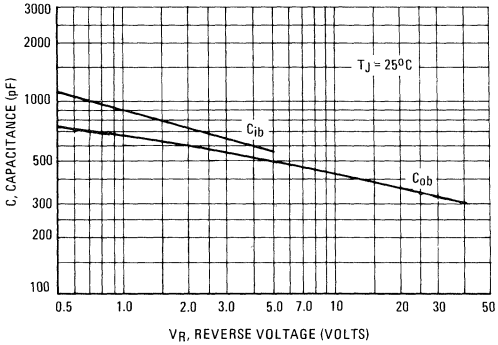


FIGURE 7 – TURN-ON TIME

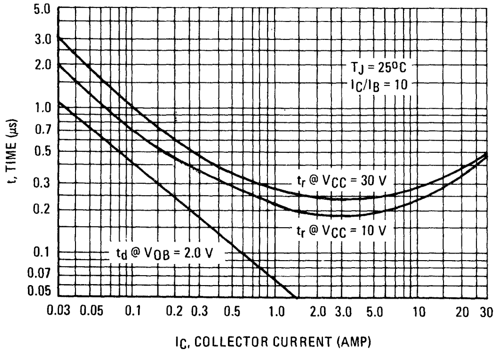


FIGURE 8 – TURN-OFF TIME

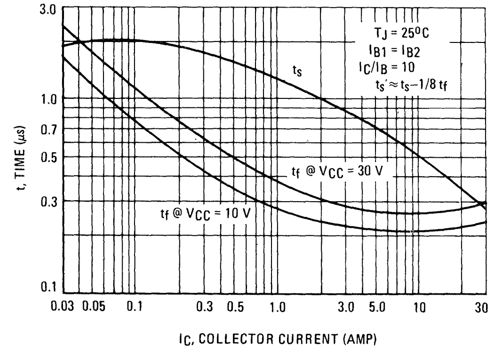


FIGURE 9 – DC CURRENT GAIN

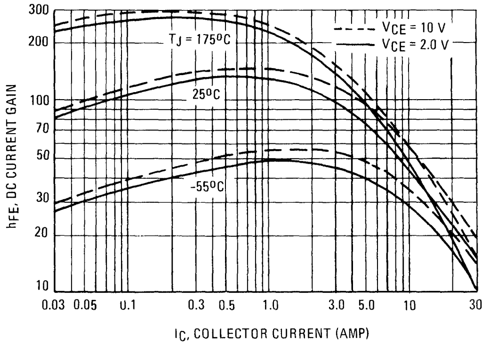


FIGURE 10 – COLLECTOR SATURATION REGION

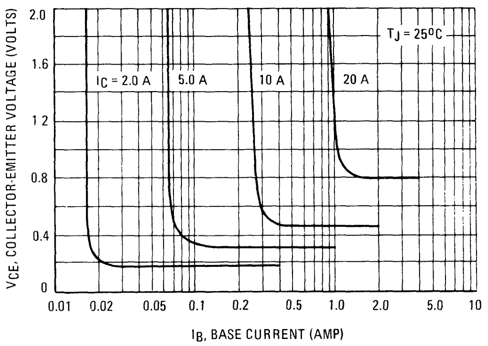


FIGURE 11 – EFFECTS OF BASE-EMITTER RESISTANCE

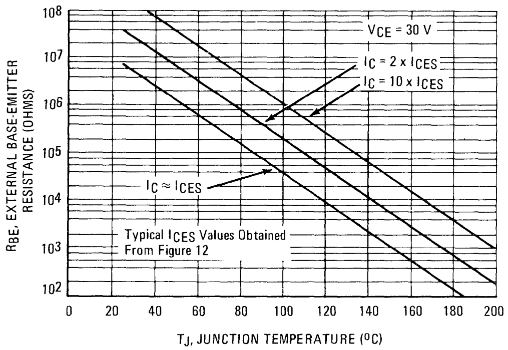


FIGURE 12 – "ON" VOLTAGES

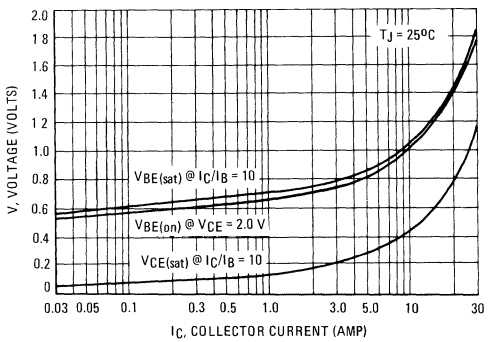


FIGURE 13 – COLLECTOR CUT-OFF REGION

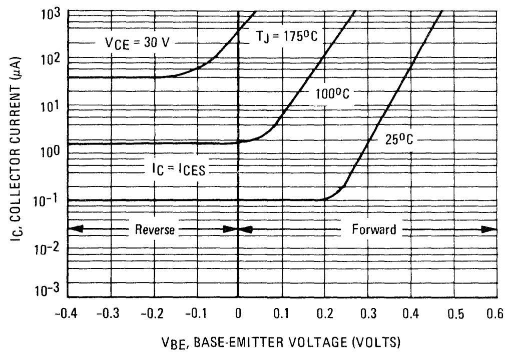
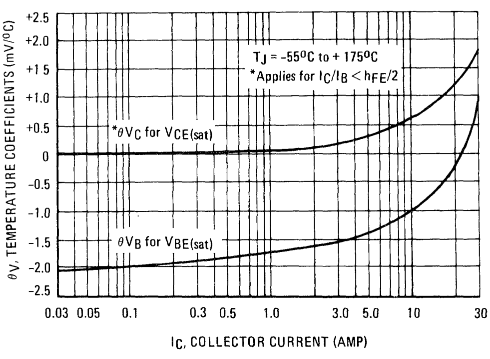


FIGURE 14 – TEMPERATURE COEFFICIENTS



2N5304 (SILICON)

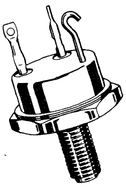
RADIATION-RESISTANT NPN SILICON POWER TRANSISTOR

. . . designed for high-speed switching and wide-band amplifier applications in radiation environments.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc (Min) @ I_C = 100 mAdc
- DC Current Gain —
  h_{FE} = 30-120 @ I_C = 2.0 Adc
  = 25 (Min) @ I_C = 5.0 Adc
  = 12 (Min) @ I_C = 10 Adc
- Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.4 Vdc (Max) @ I_C = 2.0 Adc
  = 0.8 Vdc (Max) @ I_C = 5.0 Adc
  = 1.2 Vdc (Max) @ I_C = 10 Adc
- Current-Gain — Bandwidth Product—
  f_T = 100 MHz (Min) @ I_C = 0.5 Adc
- Collector Cutoff Current, DC Current Gain and Collector-Emitter Saturation Voltage Limits Guaranteed After Exposure to 1 x 10^{14} Fast Neutron/cm^2.

10 AMPERE
POWER TRANSISTOR
NPN SILICON

40 VOLTS
25 WATTS



GUARANTEED RADIATION RESISTANCE CAPABILITIES

After 1 x 10^{14} n/cm^2 Fast Neutron (E > 10 keV) Exposure (Fission Spectrum)

Characteristic	Symbol	Min	Max	Unit
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	5.0	–	–
Collector Cutoff Current (V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc	I_{CEX}	–	50	μAdc
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	1.5	Vdc

MAXIMUM RATINGS

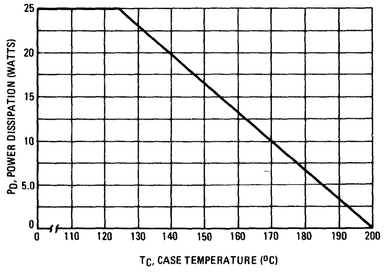
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @T_C = 125°C Derate above 125°C	P_D	25 0.333	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C
Fast Neutron Radiation Level	–	1×10^{14}	n/cm^2

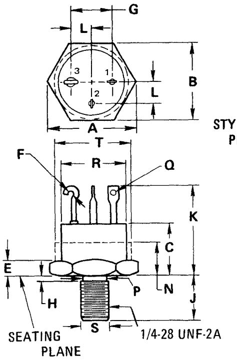
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.0	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.30	20.07	0.760	0.790
B	16.94	17.45	0.667	0.687
C	8.26	11.68	0.325	0.460
E	2.29	3.81	0.090	0.150
F	1.17	1.96	0.046	0.077
G	8.64	10.54	0.340	0.415
H	–	2.29	–	0.090
J	10.72	11.56	0.422	0.455
K	16.26	22.23	0.640	0.875
L	4.32	5.41	0.170	0.213
N	–	6.86	–	0.270
P	5.59	6.32	0.220	0.249
Q	1.19	1.83	0.047	0.072
R	14.48	15.49	0.570	0.610
S	5.651	5.761	0.2225	0.2268
T	15.49	17.45	0.610	0.687

Collector connected to case
All JEDEC dimensions and notes apply
CASE 9
TO-61

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	–	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, I_B = 0)	I_{CEO}	–	200	μAdc
Collector Cutoff Current (V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 25 Vdc, $V_{EB(off)}$ = 1.5 Vdc T_C = 150°C)	I_{CEX}	– –	10 5.0	μAdc mAdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	25	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 10 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	30 25 12	120 – –	–
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 5.0 Adc, I_B = 500 mAdc) (I_C = 10 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	– – –	0.4 0.8 1.2	Vdc
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 10 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	– –	1.2 1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	100	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	300	pF
SWITCHING CHARACTERISTICS				
Rise Time (V_{CC} ≈ 20 Vdc, I_C = 2.0 Adc, I_{B1} = 200 mAdc)	t_r	–	100	ns
Storage Time (V_{CC} ≈ 20 Vdc, I_C = 2.0 Adc, I_{B1} = 200 mAdc, I_{B2} = 100 mAdc)	t_s	–	700	ns
Fall Time (V_{CC} ≈ 20 Vdc, I_C = 2.0 Adc, I_{B1} = 200 mAdc, I_{B2} = 100 mAdc)	t_f	–	100	ns

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

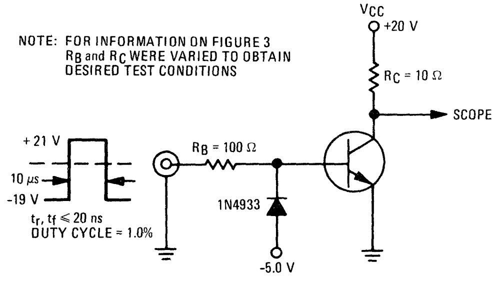


FIGURE 3 – SWITCHING TIMES

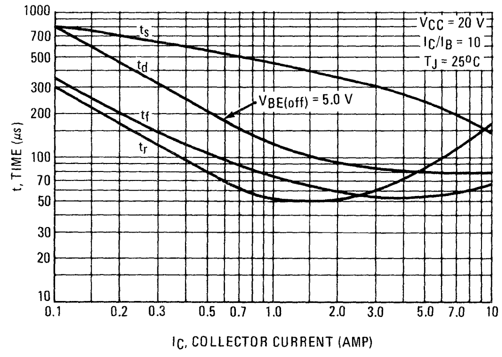


FIGURE 4 – THERMAL RESPONSE

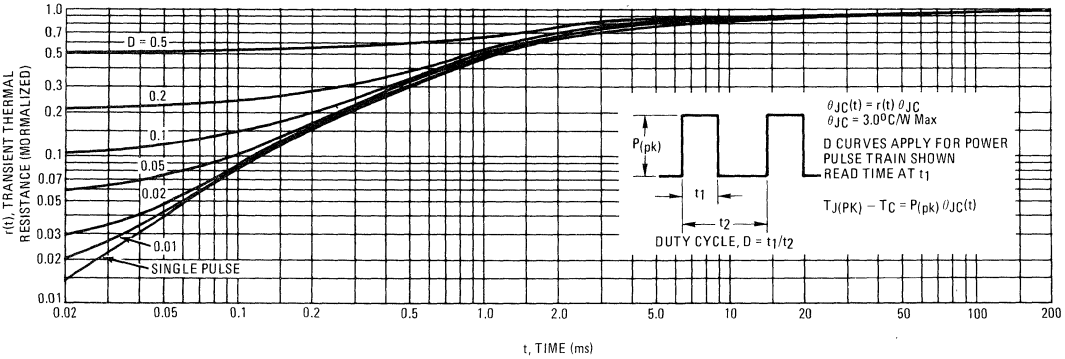
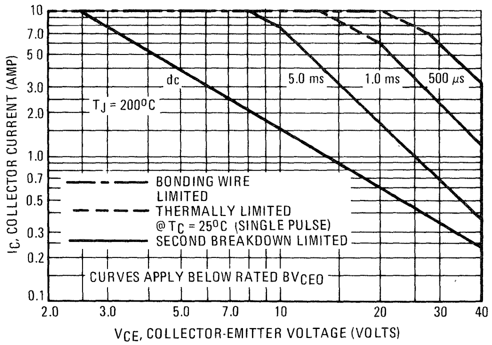


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

FIGURE 7 – CAPACITANCE

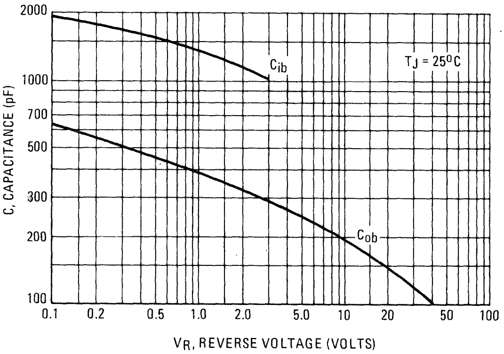
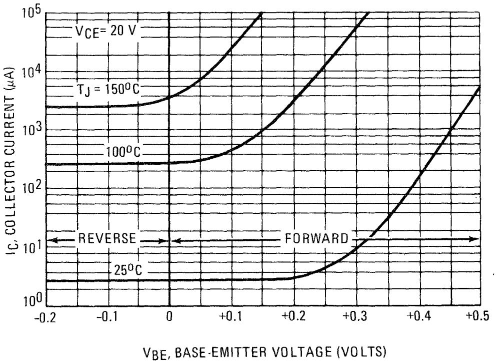
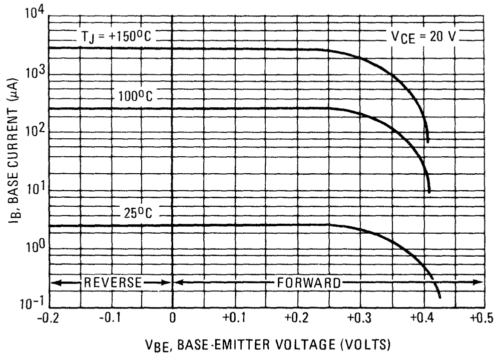


FIGURE 6 – COLLECTOR CUTOFF REGION



The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 8 – BASE CUTOFF REGION



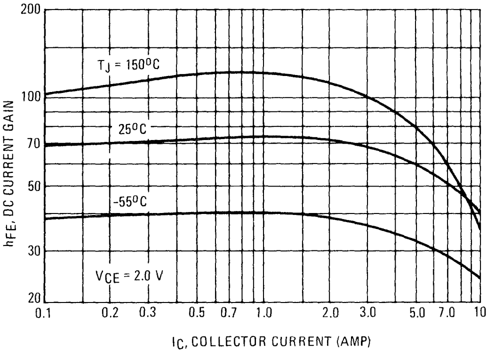


FIGURE 9 – DC CURRENT GAIN

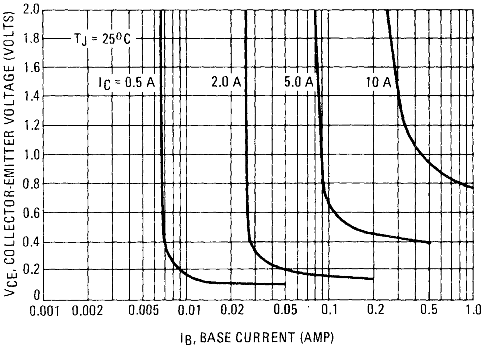


FIGURE 10 – COLLECTOR SATURATION REGION

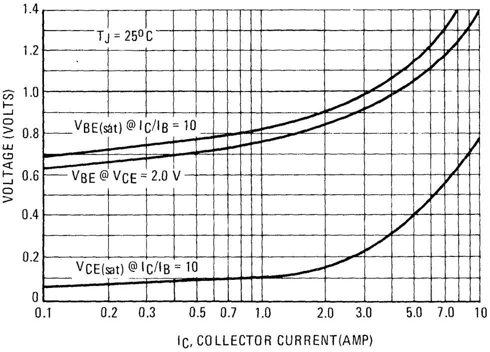


FIGURE 11 – "ON" VOLTAGES

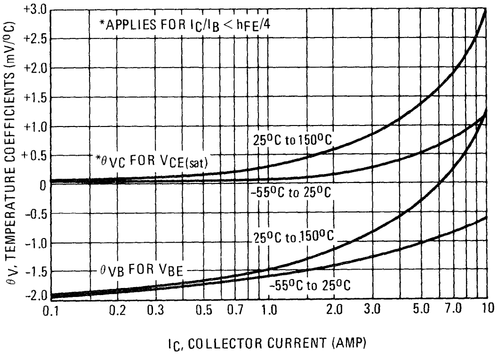


FIGURE 12 – TEMPERATURE COEFFICIENTS

EFFECTS OF FAST NEUTRON DOSAGE

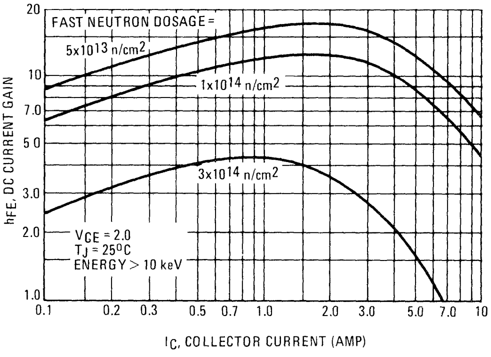


FIGURE 13 – DC CURRENT GAIN

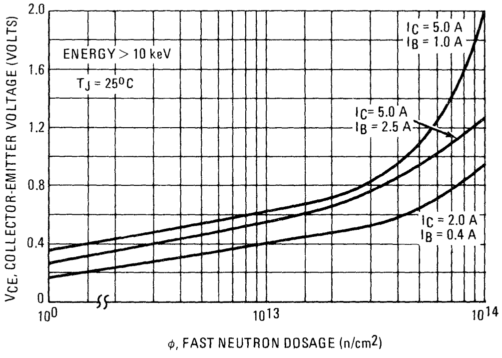


FIGURE 14 – COLLECTOR-EMITTER SATURATION VOLTAGE

2N5324 (GERMANIUM)
2N5325

PNP GERMANIUM POWER TRANSISTORS

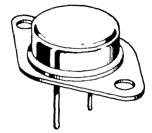
. . . designed primarily for switching, inverter, and industrial power supply applications.

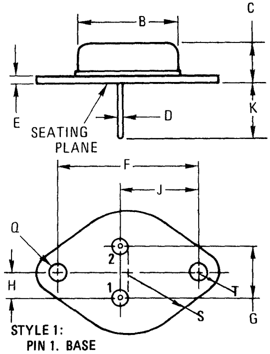
- Low Collector Cutoff Current –
  I_{CEX} = 7.0 mAdc (Max) @ V_{CEX} = 250 Vdc (2N5324)
  7.0 mAdc (Max) @ V_{CEX} = 325 Vdc (2N5325)
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 10 Adc
- Low Base-Emitter Saturation Voltage –
  $V_{BE(sat)}$ = 0.75 Vdc (Max) @ I_C = 10 Adc
- Guaranteed Excellent Safe Operating Area ($V_{CER(sus)}$)
  Specified at 3.0 Amps and 10 Amps
- 100% Stabilization Bake at 125°C for 100 Hours

10 AMPERE
POWER TRANSISTORS
PNP GERMANIUM

EPITAXIAL BASE

250-325 VOLTS
56 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply
CASE 1-03
(TO-3)

*MAXIMUM RATINGS

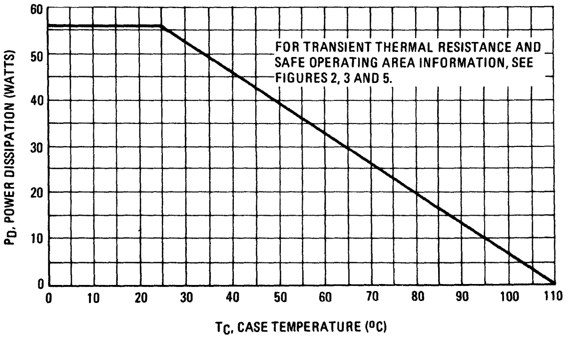
Rating	Symbol	2N5324	2N5325	Unit
Collector-Emitter Voltage	V_{CEO}	150	200	Vdc
Collector-Base Voltage	V_{CB}	250	325	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current - Continuous	I_C	10		Adc
Base Current - Continuous	I_B	3.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	56 0.67		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +110		°C

*Indicates JEDEC Registered Data.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.5	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
†Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N5324		150	–	
	2N5325		200	–	
Collector-Emitter Sustaining Voltage		$V_{CER(sus)}$			Vdc
(I_C = 3.0 Adc, R_{BE} = 10 Ohms) (Figure 4, Test Condition 1)	2N5324		165	–	
	2N5325		200	–	
(I_C = 10 Adc, R_{BE} = 10 Ohms) (Figure 4, Test Condition 2)	2N5324		100	–	
	2N5325		115	–	
*Collector Cutoff Current (See Note 1)		I_{CEV}			mAdc
(V_{CE} = 250 Vdc, V_{BE} (off) = 0.2 Vdc)	2N5324		–	7.0	
(V_{CE} = 250 Vdc, V_{BE} (off) = 0.2 Vdc, T_C = 85°C)			–	35	
(V_{CE} = 325 Vdc, V_{BE} (off) = 0.2 Vdc)	2N5325		–	7.0	
(V_{CE} = 325 Vdc, V_{BE} (off) = 0.2 Vdc, T_C = 85°C)			–	35	
*Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)		I_{EBO}	–	100	mAdc
ON CHARACTERISTICS					
*DC Current Gain (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	20	60	–
*Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	–	0.5	Vdc
*Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	0.75	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc, f = 0.5 MHz)		f_T	2.0	–	MHz
SWITCHING CHARACTERISTICS					
*Rise Time	(I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc) (See Figure 6)	t_r	–	15	μs
*Storage Time		t_s	–	10	μs
*Fall Time		t_f	–	7.0	μs

Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

***Indicates JEDEC Registered Data.**

†JEDEC Registration Defined as $V_{(BR)CEO}$

FIGURE 2 – TRANSIENT THERMAL RESPONSE

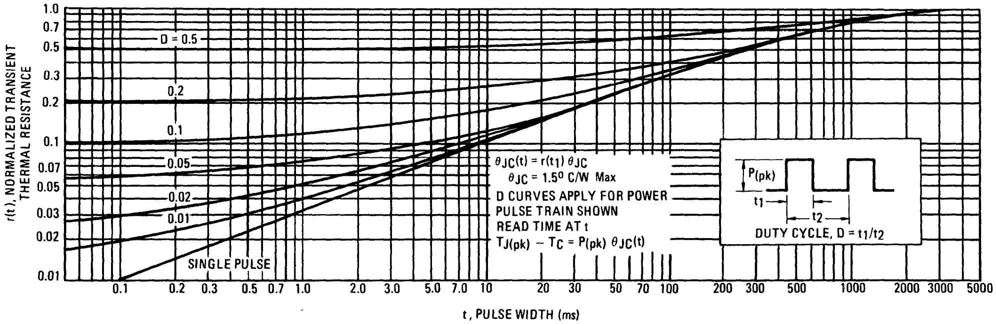


FIGURE 3 – COLLECTOR-EMITTER SUSTAINING VOLTAGE

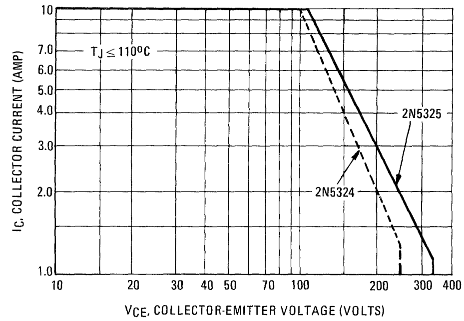
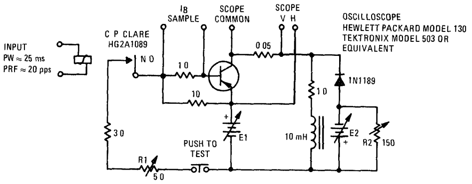


FIGURE 4 – COLLECTOR-EMITTER SUSTAINING VOLTAGE TEST CIRCUIT



TEST CONDITION 1
ADJUST E1 FOR I_C = 3 0 Adc
ADJUST E2 – 2N5324, V_{CE} = 165 Vdc
2N5325, V_{CE} = 200 Vdc
ADJUST R1 FOR I_B = 0 3 Adc

TEST CONDITION 2
ADJUST E1 FOR I_C = 10 Adc
ADJUST E2 – 2N5324, V_{CE} = 100 Vdc
2N5325, V_{CE} = 115 Vdc
ADJUST R1 FOR I_B = 1 0 Adc

R2 SET TO ALLOW REVERSE SURGE CURRENT TO BYPASS E2 POWER SUPPLY NOT NEEDED FOR POWER SUPPLY WITH LOW REVERSE IMPEDANCE

FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA

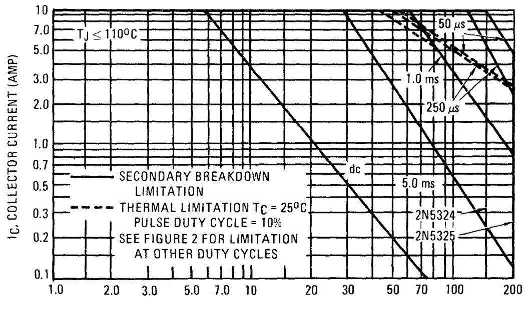


FIGURE 6 – SWITCHING TIME TEST CIRCUIT

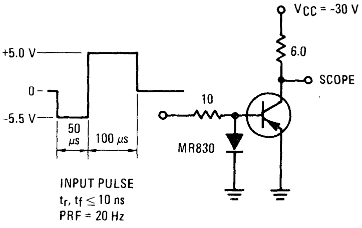


FIGURE 7 – SWITCHING TIMES

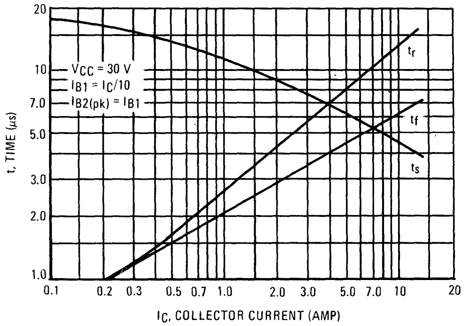


FIGURE 8 - CURRENT GAIN BANDWITH PRODUCT

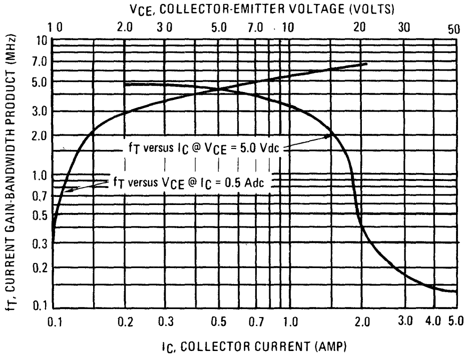


FIGURE 9 – DC CURRENT GAIN

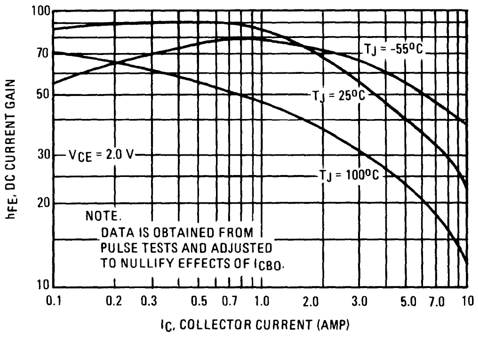


FIGURE 10 – COLLECTOR SATURATION REGION

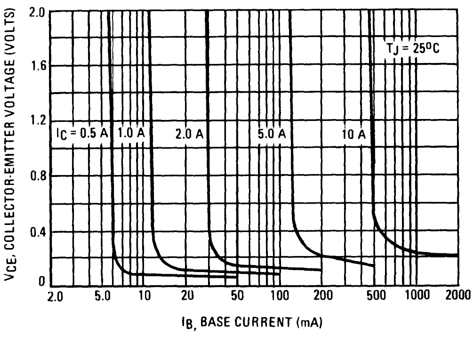


FIGURE 11 – EFFECTS OF EMITTER-BASE RESISTANCE

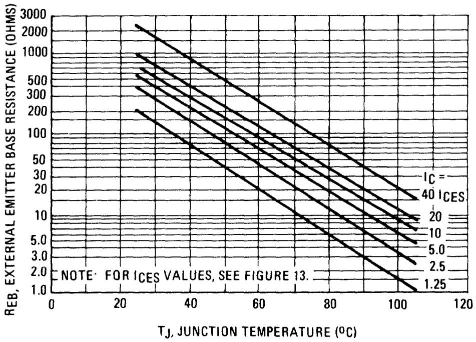


FIGURE 12 – "ON" VOLTAGES

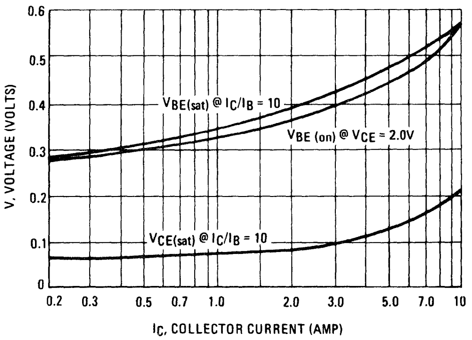


FIGURE 13 – COLLECTOR CUTOFF REGION

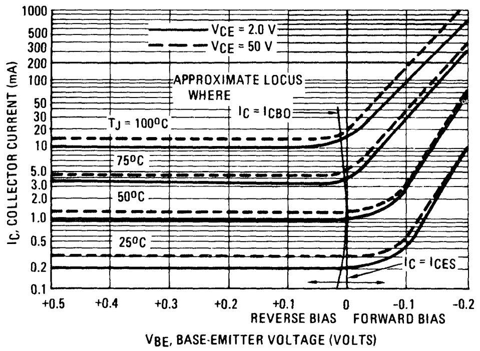
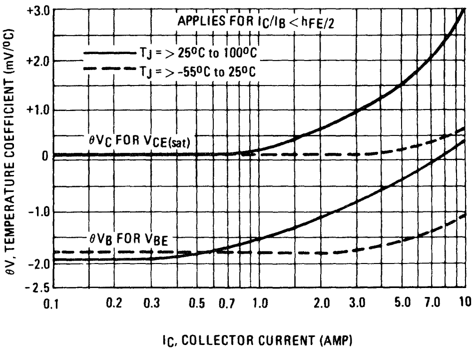
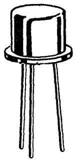


FIGURE 14 – TEMPERATURE COEFFICIENTS

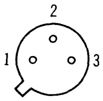


2N5336 (SILICON)
thru
2N5339



Medium-power NPN silicon transistors designed for switching and wide band amplifier applications.

CASE 79
(TO-39)



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

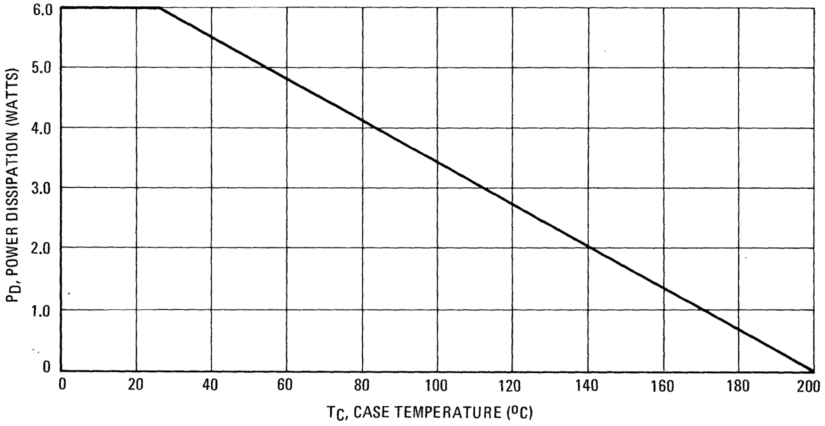
MAXIMUM RATINGS

Rating	Symbol	2N5336 2N5337	2N5338 2N5339	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	6.0 34.3		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	29.2	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		-	$BV_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N5336, 2N5337			80	-	
	2N5338, 2N5339			100	-	
Collector Cutoff Current		-	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N5336, 2N5337			-	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N5338, 2N5339			-	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5336, 2N5337			-	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5338, 2N5339			-	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5336, 2N5337			-	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5338, 2N5339			-	1.0	
Collector Cutoff Current		-	I_{CBO}			μAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N5336, 2N5337			-	10	
(V_{CB} = 100 Vdc, I_E = 0)	2N5338, 2N5339			-	10	
Emitter Cutoff Current		-	I_{EBO}			μAdc
(V_{BE} = 6.0 Vdc, I_C = 0)				-	100	
ON CHARACTERISTICS						
DC Current Gain (1)		8	h_{FE}			-
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			30	-	
	2N5337, 2N5339			60	-	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			30	120	
	2N5337, 2N5339			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			20	-	
	2N5337, 2N5339			40	-	
Collector-Emitter Saturation Voltage (1)		9, 11, 13	$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				-	0.7	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				-	1.2	
Base-Emitter Saturation Voltage (1)		11, 13	$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				-	1.2	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				-	1.8	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product		-	f_T			MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 10 MHz)				30	-	
Output Capacitance		7	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)				-	250	
Input Capacitance		7	C_{ib}			pF
(V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)				-	1,000	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc, I_C = 2.0 Adc, I_{B1} = 0.2 Adc)	2,3	t_d	-	100	ns
Rise Time			t_r	-	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.2 Adc)	2,6	t_s	-	2.0	μs
Fall Time			t_f	-	200	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

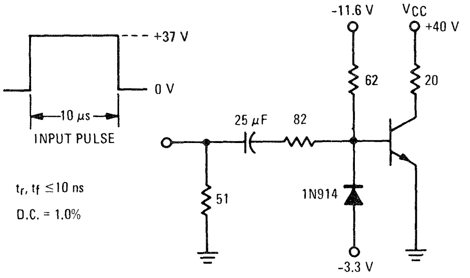


FIGURE 3 – TURN ON TIME

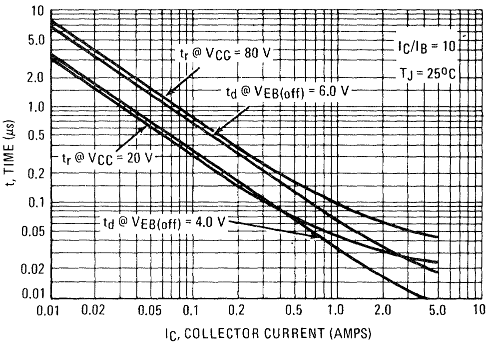


FIGURE 4 – THERMAL RESPONSE

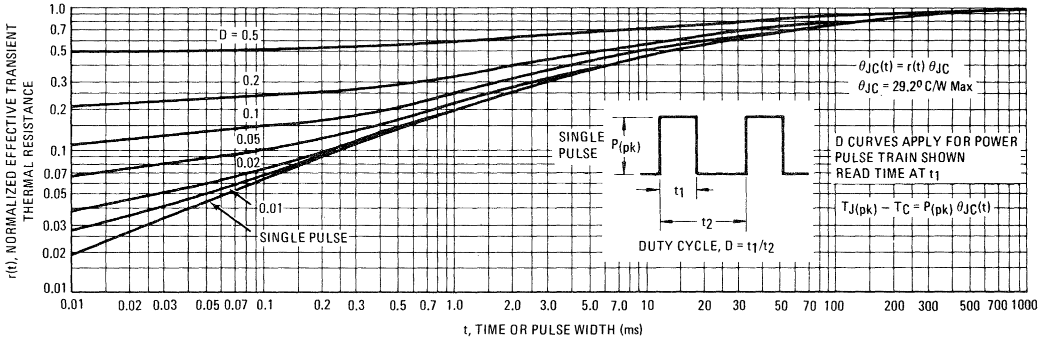
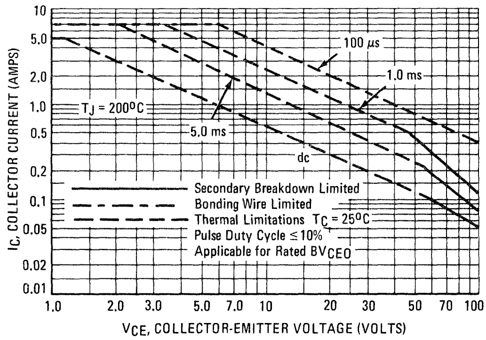


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

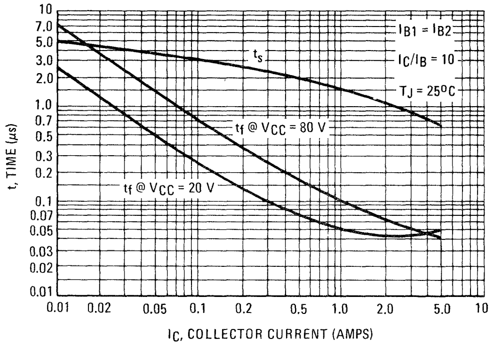


FIGURE 7 – CAPACITANCE versus VOLTAGE

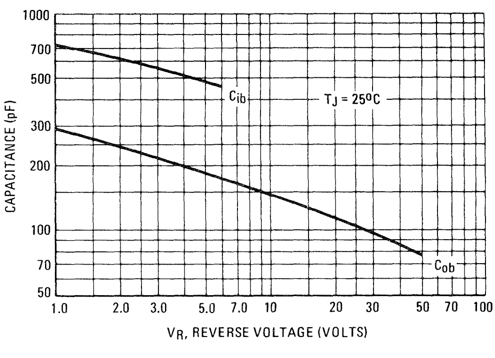


FIGURE 8 – DC CURRENT GAIN

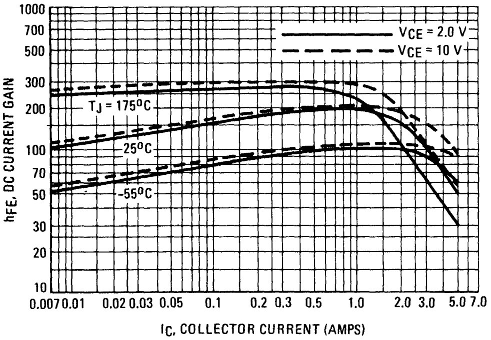


FIGURE 9 – COLLECTOR SATURATION REGION

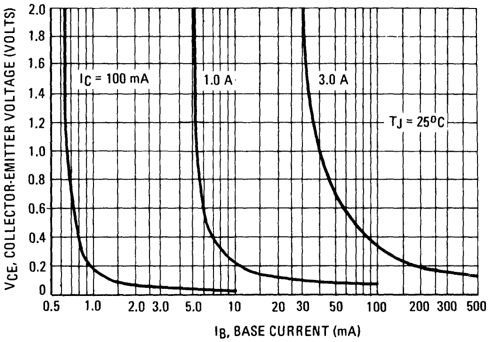


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

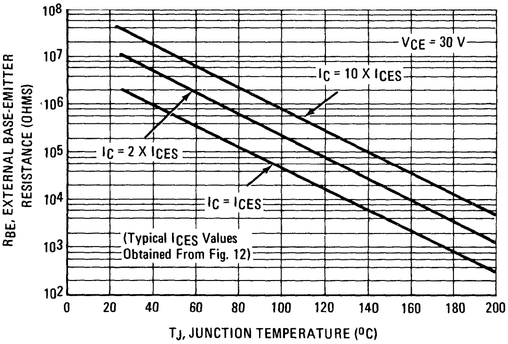


FIGURE 11 – ON VOLTAGES

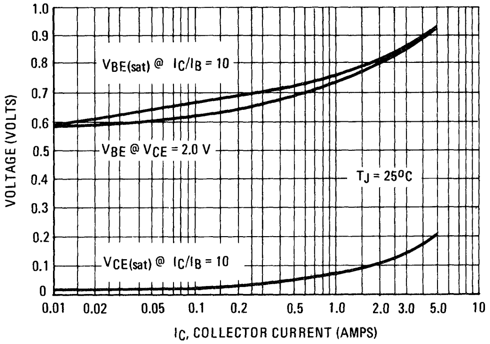


FIGURE 12 – COLLECTOR CUT-OFF REGION

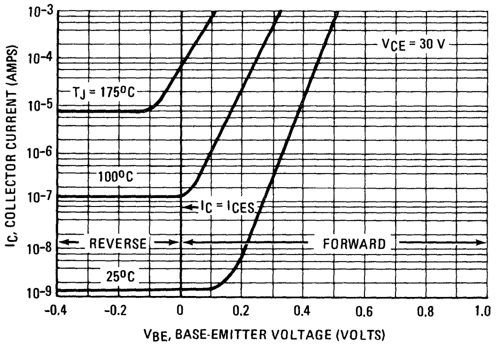
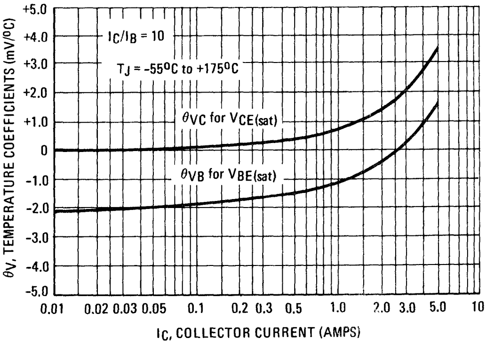
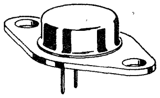


FIGURE 13 – TEMPERATURE COEFFICIENTS



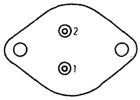
2N5344 (SILICON)
2N5345

High voltage power PNP silicon transistors designed for high-voltage switching and amplifier applications.



CASE 80
(TO-66)

Collector connected to case



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

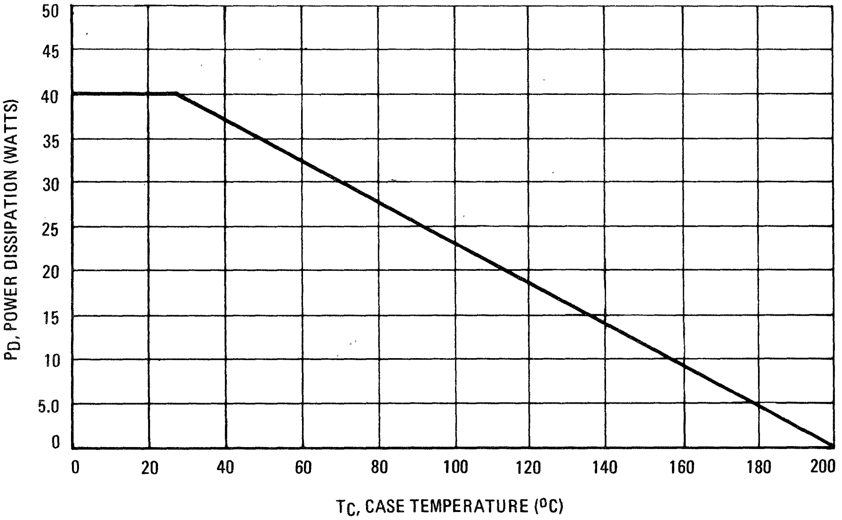
MAXIMUM RATINGS

Rating	Symbol	2N5344	2N5345	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	Vdc
Collector-Base Voltage	V_{CB}	250	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	1.0		Adc
Base Current — Continuous	I_B	0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 228		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.38	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves Are Indicated By Figure 5. All Limits Are Applicable And Must Be Observed

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0) 2N5344 2N5345	5	$V_{CEO(sus)}$	250 300	- -	Vdc
Collector Cutoff Current (V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5344 (V_{CE} = 270 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5345 (V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) 2N5344 (V_{CE} = 270 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) 2N5345	10, 12	I_{CEX}	- - - -	100 100 1.0 1.0	μAdc mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	-	I_{CBO}	-	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	-	I_{EBO}	-	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	8	h_{FE}	25 7.0	100 -	-
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)	9, 11, 13	$V_{CE(sat)}$	-	3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)	11, 13	$V_{BE(sat)}$	-	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 100 mAdc, V_{CE} = 20 Vdc, f = 10 MHz)	-	f_T	60	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0)	7	C_{ob}	-	200	pF
SWITCHING CHARACTERISTICS					
Delay Time (V_{CC} = 100 Vdc, $V_{BE(off)}$ = 0.85 Vdc, I_C = 500 mAdc, I_{B1} = 50 mAdc)	2, 3	t_d	-	100	ns
Rise Time	2, 3	t_r	-	100	ns
Storage Time (V_{CC} = 100 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc)	2, 6	t_s	-	600	ns
Fall Time	2, 6	t_f	-	100	ns

(1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

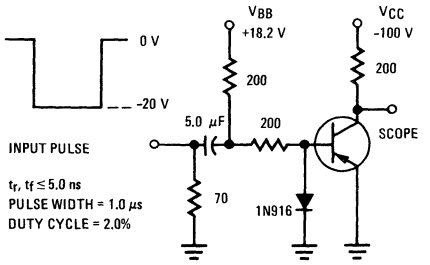


FIGURE 3 — TURN-ON TIME

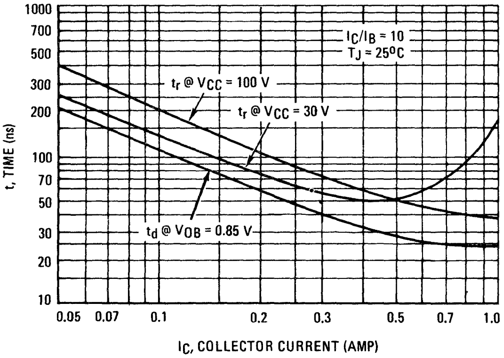


FIGURE 4 – THERMAL RESPONSE

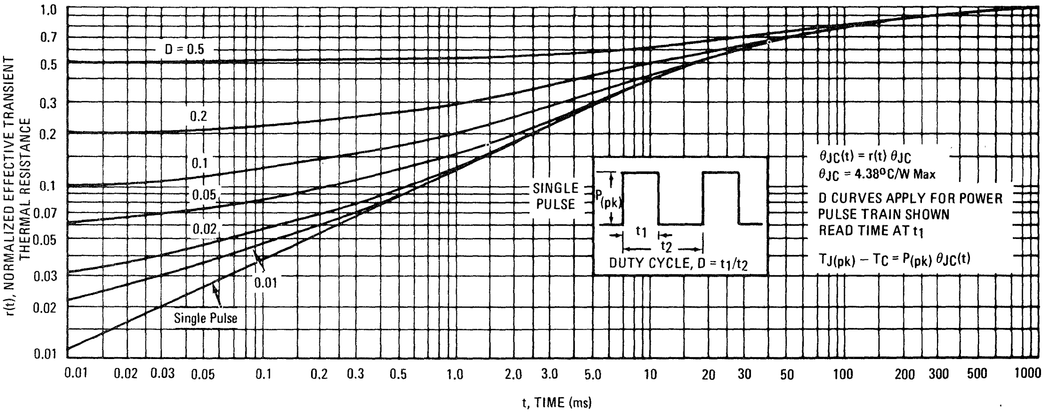
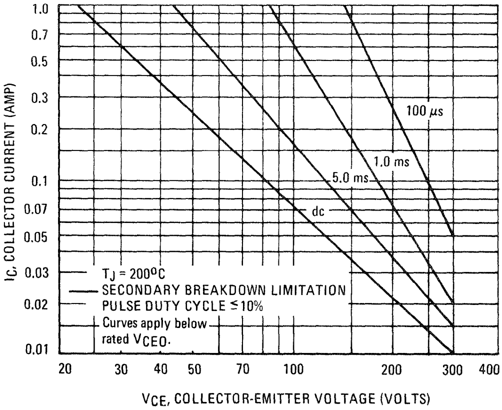


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

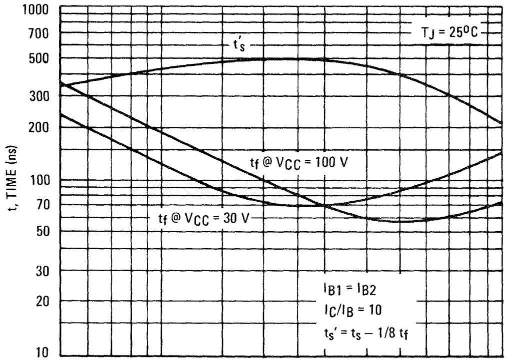
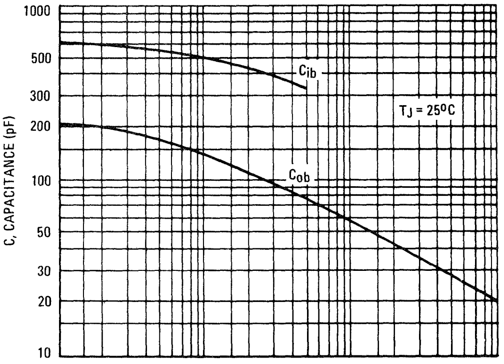


FIGURE 7 – CAPACITANCES



TYPICAL DC CHARACTERISTICS

FIGURE 8 – DC CURRENT GAIN

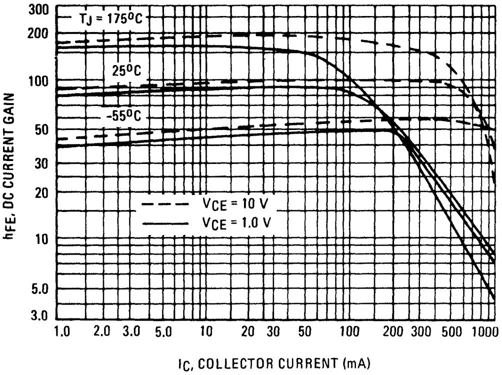


FIGURE 9 – COLLECTOR SATURATION REGION

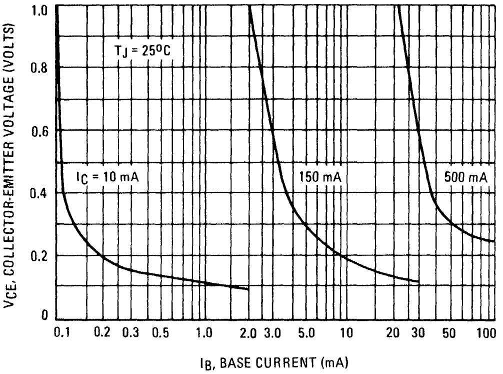


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

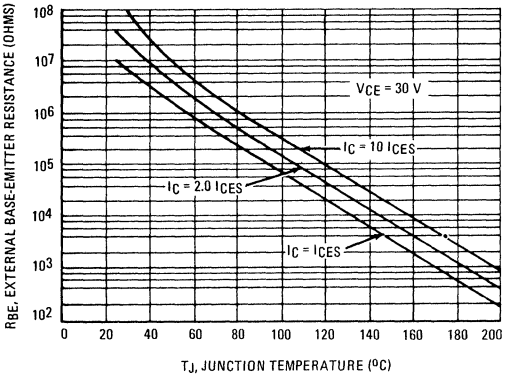


FIGURE 11 – "ON" VOLTAGES

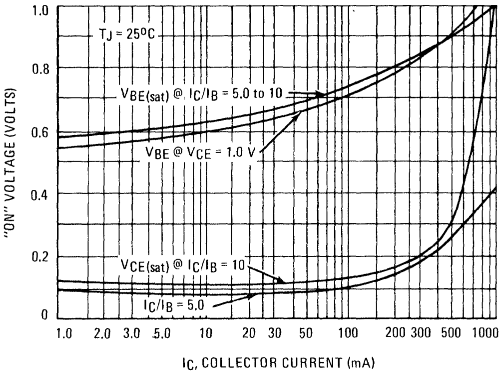


FIGURE 12 – COLLECTOR CUT-OFF REGION

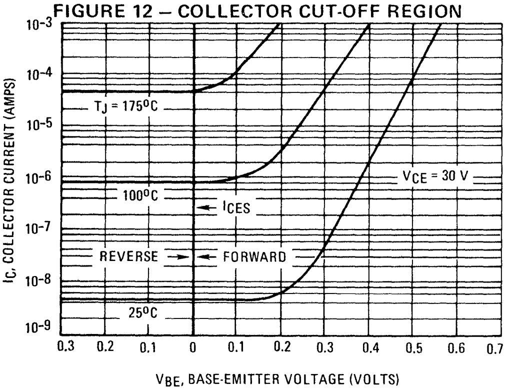
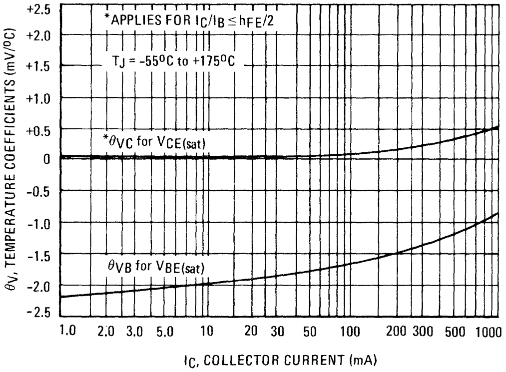


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5346 (SILICON)
thru
2N5349

MEDIUM-POWER NPN SILICON TRANSISTORS

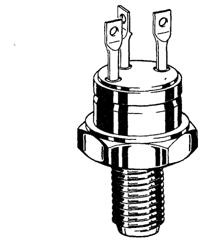
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 7.0 Adc
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact, High Dissipation TO-59 Case
- Isolated Collector Configuration

7 AMPERE
POWER TRANSISTORS

NPN SILICON

80-100 VOLTS
60 WATTS



*MAXIMUM RATINGS

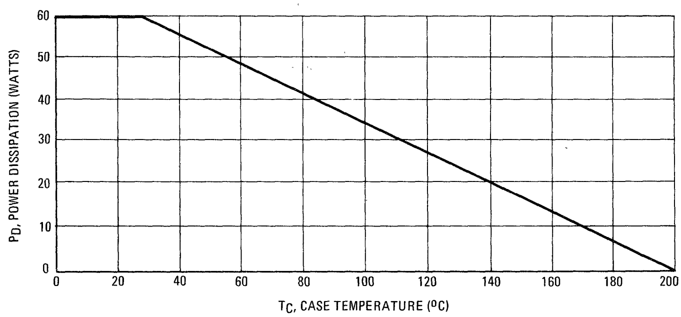
Rating	Symbol	2N5346 2N5347	2N5348 2N5349	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	7.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 343		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

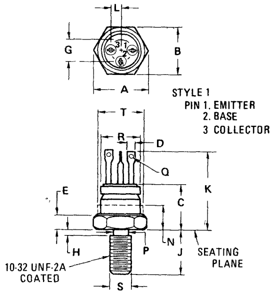
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.91	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	8.13	11.89	0.320	0.468
E	2.29	3.81	0.090	0.150
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	10.16	11.56	0.400	0.455
K	14.48	19.38	0.570	0.763
L	2.29	2.79	0.090	0.110
N	–	6.35	–	0.250
P	4.14	4.80	0.163	0.189
Q	1.02	1.65	0.040	0.065
R	8.08	9.65	0.318	0.380
S	4.212	4.310	0.1658	0.1697
T	9.65	11.10	0.380	0.437

All JEDEC dimensions and notes apply
Collector isolated from case.

CASE 160-03
TO-59

ISOLATED COLLECTOR

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	 2N5346, 2N5347 2N5348, 2N5349	-	$V_{CEO(sus)}$	 80 100	 - -	Vdc
Collector Cutoff Current (V_{CE} = 75 Vdc, I_B = 0) (V_{CE} = 90 Vdc, I_B = 0)	 2N5346, 2N5347 2N5348, 2N5349	-	I_{CEO}	 - -	 100 100	μAdc
Collector Cutoff Current (V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N5346, 2N5347 2N5348, 2N5349 2N5346, 2N5347 2N5348, 2N5349	12	I_{CEX}	 - - - -	 10 10 1.0 1.0	μAdc mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		-	I_{CBO}	-	10	μAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		-	I_{EBO}	-	100	μAdc
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 500 mAdc, V_{CE} = 2.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	 2N5346, 2N5348 2N5347, 2N5349 2N5346, 2N5348 2N5347, 2N5349 2N5346, 2N5348 2N5347, 2N5349	8	h_{FE}	 30 60 30 60 20 40	 - - 120 240 - -	-
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc) (I_C = 7.0 Adc, I_B = 0.7 Adc)		9,11,13	$V_{CE(sat)}$	 - -	 0.7 1.2	Vdc
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc) (I_C = 7.0 Adc, I_B = 0.7 Adc)		11, 13	$V_{BE(sat)}$	 - -	 1.2 2.0	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		-	f_T	30	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		7	C_{ob}	-	250	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		7	C_{ib}	-	1,000	pF
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc, I_C = 2.0 Adc, I_{B1} = 200 mAdc)	2,3	t_d	-	100	ns
Rise Time			t_r	-	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc, I_{B1} = I_{B2} = 200 mAdc)	2,6	t_s	-	2.0	μs
Fall Time			t_f	-	200	ns

*Indicates JEDEC Registered Data.
(1)Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

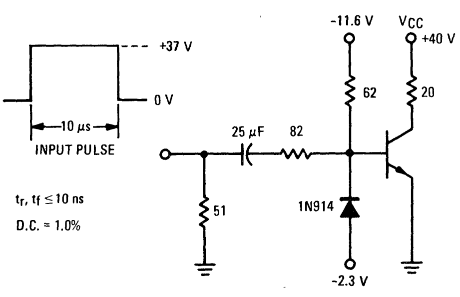


FIGURE 3 – TURN-ON TIME

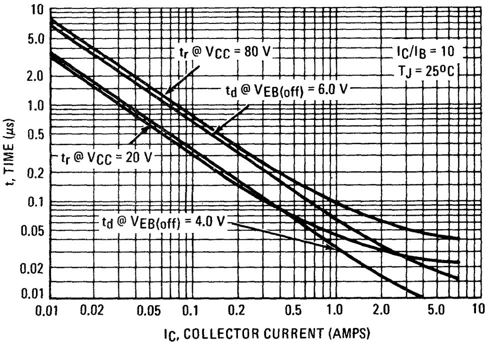


FIGURE 4 – THERMAL RESPONSE

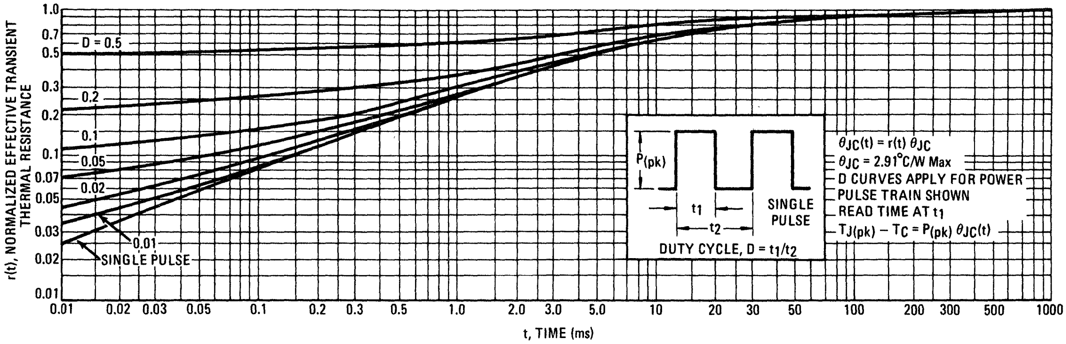
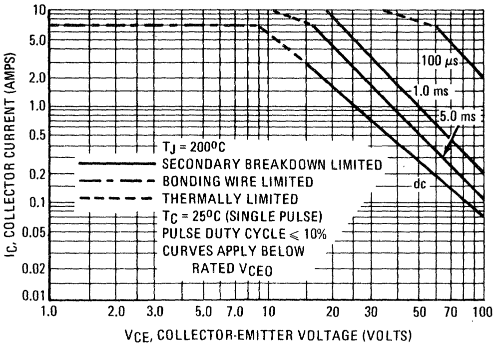


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

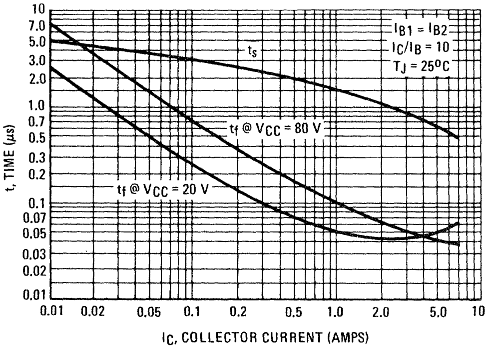


FIGURE 7 – CAPACITANCE versus VOLTAGE

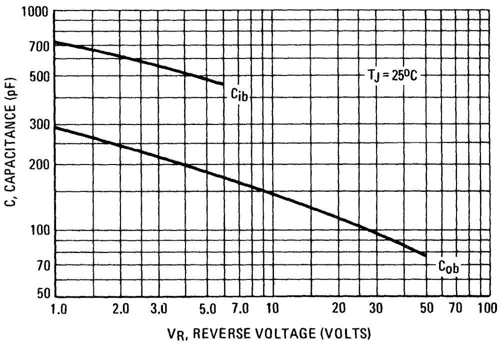


FIGURE 8 – DC CURRENT GAIN

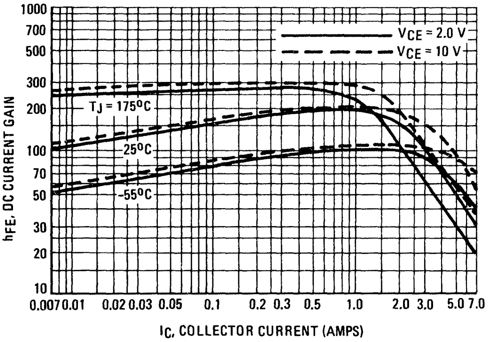


FIGURE 9 – COLLECTOR SATURATION REGION

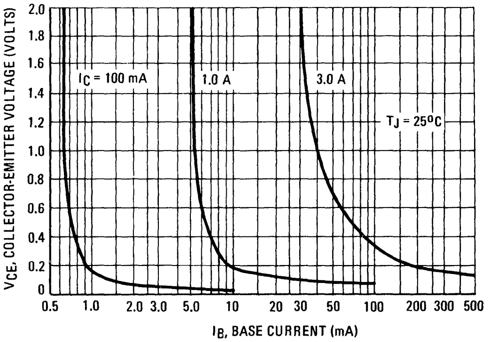


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

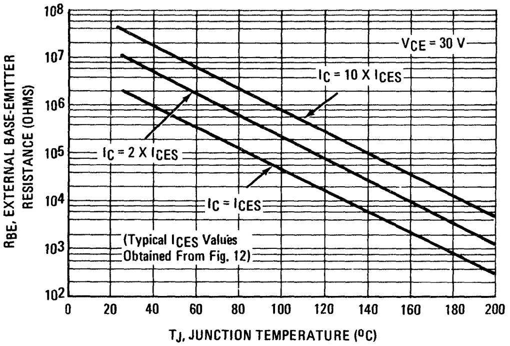


FIGURE 11 – "ON" VOLTAGES

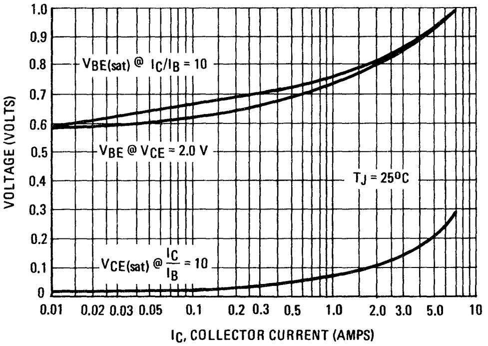


FIGURE 12 – COLLECTOR CUT-OFF REGION

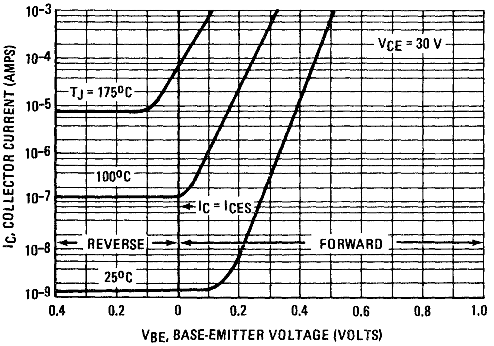
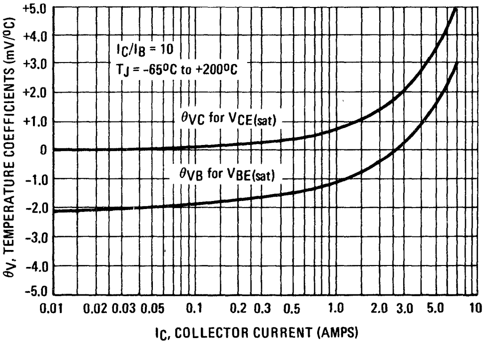


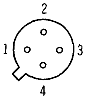
FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5358 (SILICON)
thru
2N5364

Silicon N-channel junction field-effect transistors depletion mode (Type A) devices designed primarily for general-purpose amplifier applications.

CASE 20
(TO-72)



STYLE 3
PIN 1. DRAIN
2. SOURCE
3. GATE
4. CASE LEAD

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Forward Gate Current	$I_{G(f)}$	10	mAdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	40	Vdc
Drain-Gate Voltage	V_{DG}	40	Vdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 2.0	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C
Operating Junction Temperature Range	T_J	-65 to +175	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage ($I_G = 10\ \mu$Adc, $V_{DS} = 0$)		$V_{(BR)GSS}$	40	-	Vdc
Gate-Source Cutoff Voltage ($V_{DS} = 15$ Vdc, $I_D = 100$ nAdc)	2N5358	$V_{GS(off)}$	0.5	3.0	Vdc
	2N5359		0.8	4.0	
	2N5360		0.8	4.0	
	2N5361		1.0	6.0	
	2N5362		2.0	7.0	
	2N5363		2.5	8.0	
	2N5364		2.5	8.0	
Gate Reverse Current ($V_{GS} = 20$ Vdc, $V_{DS} = 0$)		I_{GSS}	-	0.1	nAdc
($V_{GS} = 20$ Vdc, $V_{DS} = 0$, $T_A = 150°C$)			-	0.1	μAdc

ELECTRICAL CHARACTERISTICS (continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5358	I_{DSS}	0.5	1.0	mAdc
	2N5359		0.8	1.6	
	2N5360		1.5	3.0	
	2N5361		2.5	5.0	
	2N5362		4.0	8.0	
	2N5363		7.0	14	
	2N5364		9.0	18	
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 50 μAdc)	2N5358	V_{GS}	0.3	1.5	Vdc
(V_{DS} = 15 Vdc, I_D = 80 μAdc)	2N5359		0.4	2.0	
(V_{DS} = 15 Vdc, I_D = 150 μAdc)	2N5360		0.5	2.5	
(V_{DS} = 15 Vdc, I_D = 250 μAdc)	2N5361		1.0	5.0	
(V_{DS} = 15 Vdc, I_D = 400 μAdc)	2N5362		1.3	5.0	
(V_{DS} = 15 Vdc, I_D = 700 μAdc)	2N5363		2.0	6.0	
(V_{DS} = 15 Vdc, I_D = 900 μAdc)	2N5364		2.0	6.0	
SMALL-SIGNAL CHARACTERISTICS					
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5358	$\|y_{fs}\|$	1000	3000	μmhos
	2N5359		1200	3600	
	2N5360		1400	4200	
	2N5361		1500	4500	
	2N5362		2000	5500	
	2N5363		2500	6000	
	2N5364		2700	6500	
Forward Transconductance (V_{DS} = 15 Vdc, V_{GS} = 0 Vdc, f = 100 MHz)	2N5358	$Re(y_{fs})$	800	-	μmhos
	2N5359		900	-	
	2N5360		1400	-	
	2N5361		1700	-	
	2N5362		1900	-	
	2N5363		2100	-	
	2N5364		2200	-	
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5358, 2N5359	$\|y_{os}\|$	-	10	μmhos
	2N5360, 2N5361			20	
	2N5362, 2N5363			40	
	2N5364			60	
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	-	6.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	-	2.0	pF
Common-Source Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 100 Hz, BW = 1.0 Hz)		NF	-	2.5	dB
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)		e_n	-	115	nV/$\sqrt{Hz}$

DRAIN CURRENT versus GATE SOURCE VOLTAGE

FIGURE 1 – 2N5358

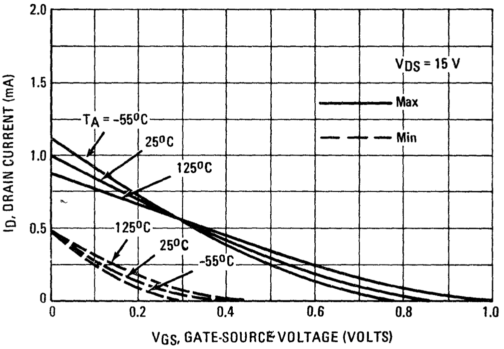


FIGURE 3 – 2N5359

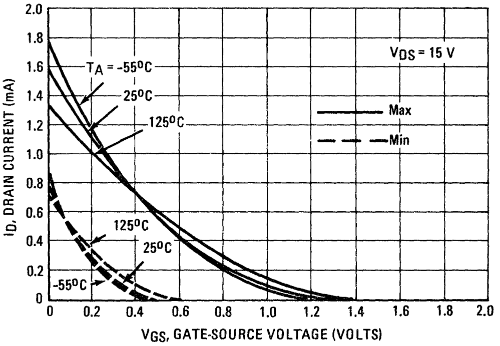
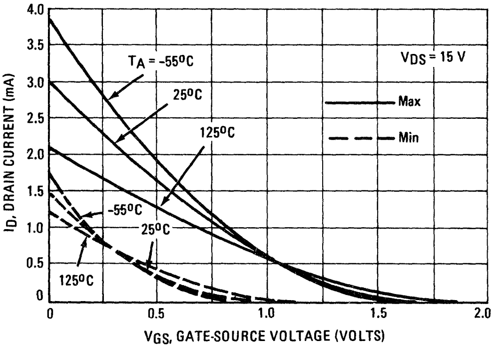


FIGURE 5 – 2N5360



FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

FIGURE 2 – 2N5358

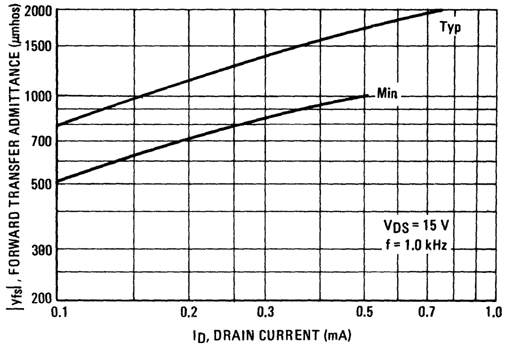


FIGURE 4 – 2N5359

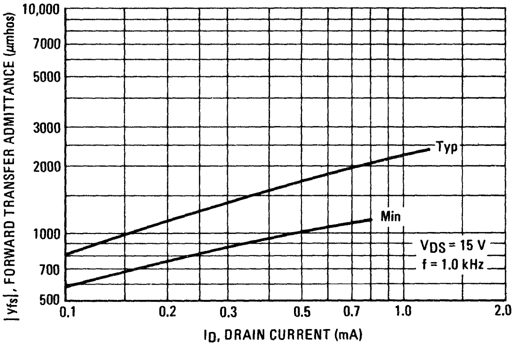
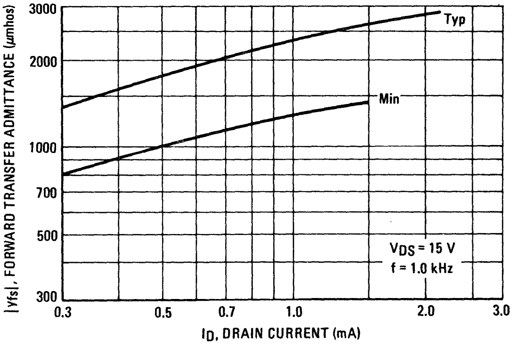


FIGURE 6 – 2N5360



DRAIN CURRENT versus GATE SOURCE VOLTAGE

FIGURE 7 – 2N5361

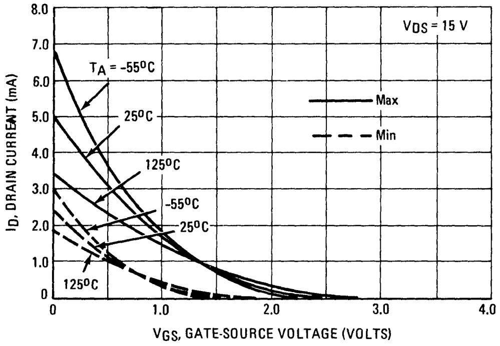


FIGURE 9 – 2N5362

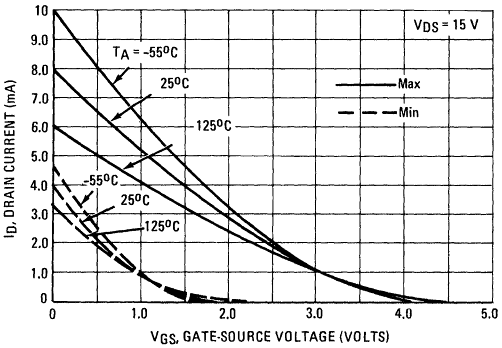
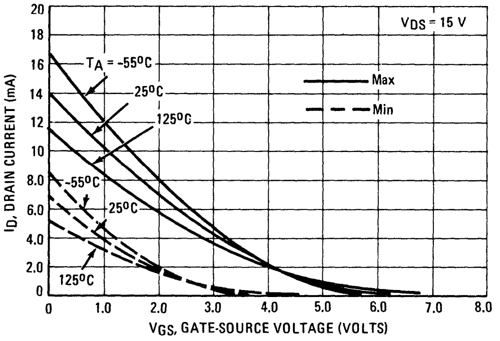


FIGURE 11 – 2N5363



FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

FIGURE 8 – 2N5361

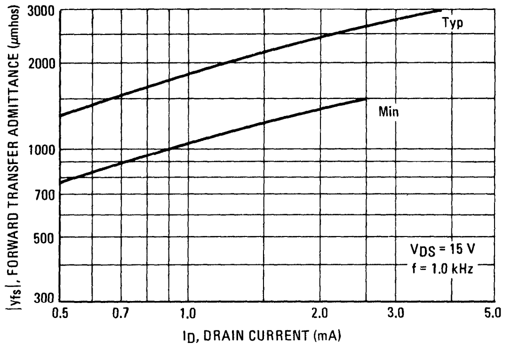


FIGURE 10 – 2N5362

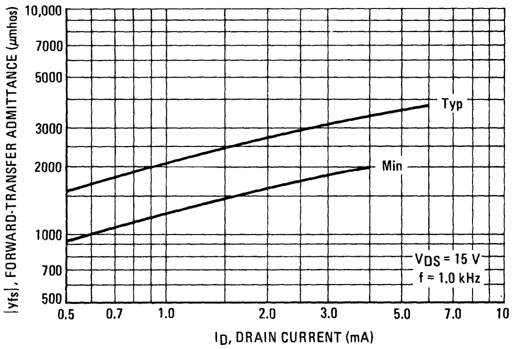
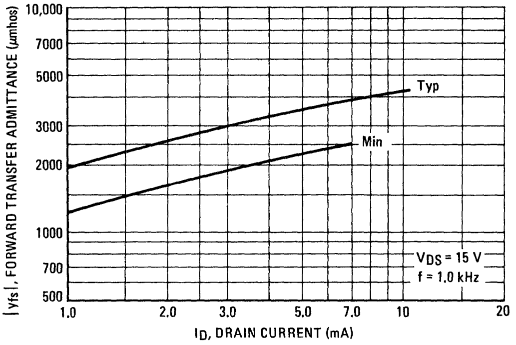
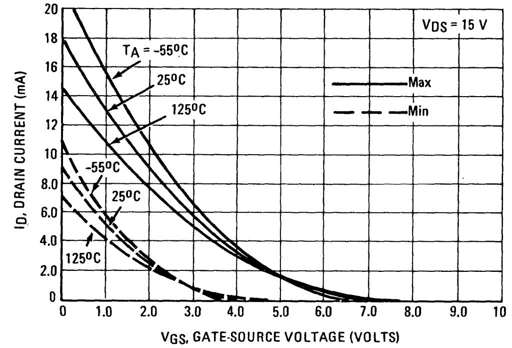


FIGURE 12 – 2N5363



DRAIN CURRENT versus GATE-SOURCE VOLTAGE

FIGURE 13 – 2N5364



FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

FIGURE 14 – 2N5364

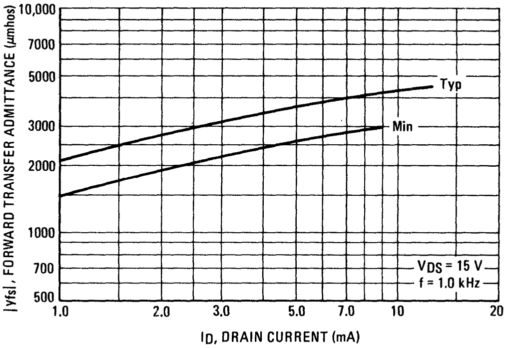


FIGURE 15 – TYPICAL DRAIN CURRENT TEMPERATURE COEFFICIENT versus DRAIN CURRENT

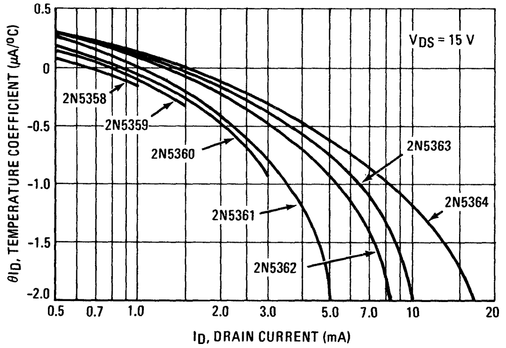


FIGURE 16 – TYPICAL FORWARD TRANSADMITTANCE TEMPERATURE COEFFICIENT versus DRAIN CURRENT

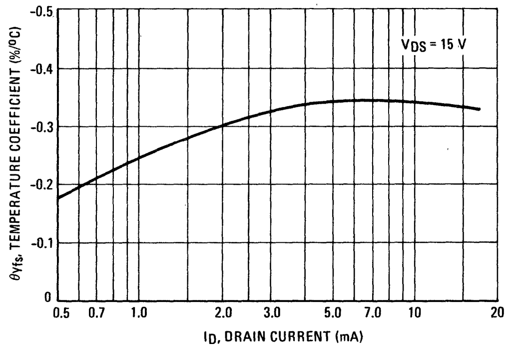


FIGURE 17 – TYPICAL OUTPUT RESISTANCE versus DRAIN CURRENT

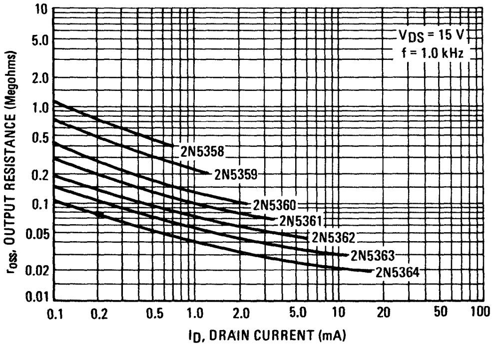


FIGURE 18 – TYPICAL CAPACITANCE versus VOLTAGE

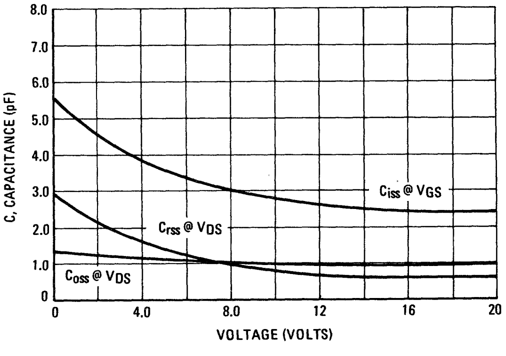


FIGURE 19 – TYPICAL NOISE FIGURE versus FREQUENCY

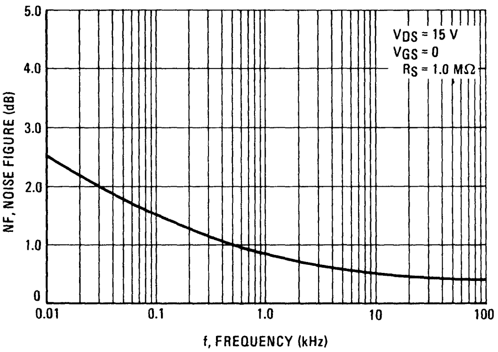


FIGURE 20 – TYPICAL NOISE FIGURE versus SOURCE RESISTANCE

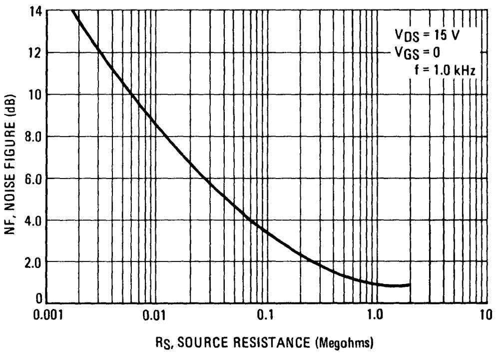
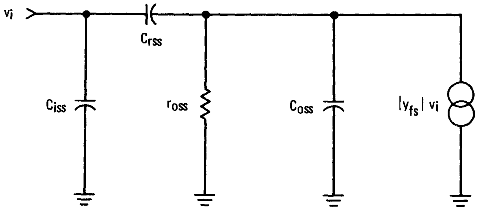


FIGURE 21 – EQUIVALENT LOW FREQUENCY CIRCUIT



Common Source
y Parameters for Frequencies
Below 30 MHz

$y_{is} = j\omega C_{iss}$
$y_{os} = j\omega C_{osp}{}^{*} + 1/r_{oss}$
$y_{fs} = |y_{fs}|$
$y_{rs} = -j\omega C_{rss}$

*C_{osp} is C_{oss} in parallel with Series Combination of C_{iss} and C_{rss}.

NOTE: Graphical data is presented for dc conditions. Tabular data is given for pulsed conditions (Pulse Width = 630 ms, Duty Cycle = 10%).

2N5400 (SILICON)
2N5401

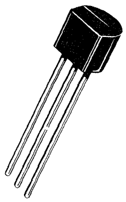
PNP SILICON ANNULAR TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier applications.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 120 and 150 Vdc (Min)
- Low Saturation Voltage $V_{CE(sat)}$ = 0.5 V (Max) @ I_C = 50 mA
- Current Gain Specified from 1.0 mAdc to 50 mAdc
- Excellent for Nixie® Driver Applications

HIGH VOLTAGE

PNP SILICON AMPLIFIER TRANSISTORS



MAXIMUM RATINGS

Rating	Symbol	2N5400	2N5401	Unit
*Collector-Emitter Voltage	V_{CEO}	120	150	Vdc
*Collector-Base Voltage	V_{CB}	130	160	Vdc
*Emitter-Base Voltage	V_{EB}	5.0		Vdc
*Collector Current — Continuous	I_C	600		mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8		mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

*Indicates JEDEC Registered Data

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

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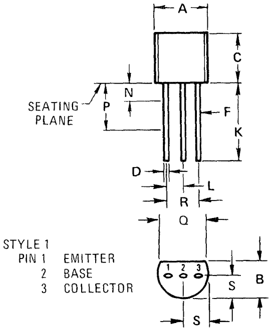


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0 016	0.021
F	0.407	0.482	0.016	0 019
K	12.700	–	0.500	–
L	1 150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2 670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
($I_C = 1.0$ mAdc, $I_B = 0$)	2N5400		120	–	
	2N5401		150	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
($I_C = 100\ \mu$Adc, $I_E = 0$)	2N5400		130	–	
	2N5401		160	–	
Emitter-Base Breakdown Voltage		BV_{EBO}			Vdc
($I_E = 10\ \mu$Adc, $I_C = 0$)			5.0	–	
Collector Cutoff Current		I_{CBO}			nAdc
($V_{CB} = 100$ Vdc, $I_E = 0$)	2N5400		–	100	
($V_{CB} = 120$ Vdc, $I_E = 0$)	2N5401		–	50	
($V_{CB} = 100$ Vdc, $I_E = 0$, $T_A = 100^{\circ}C$)	2N5400		–	100	μAdc
($V_{CB} = 120$ Vdc, $I_E = 0$, $T_A = 100^{\circ}C$)	2N5401		–	50	
Emitter Cutoff Current		I_{EBO}			nAdc
($V_{EB} = 3.0$ Vdc, $I_C = 0$)			–	50	
ON CHARACTERISTICS (1)					
*DC Current Gain		h_{FE}			–
($I_C = 1.0$ mAdc, $V_{CE} = 5.0$ Vdc)	2N5400		30	–	
	2N5401		50	–	
($I_C = 10$ mAdc, $V_{CE} = 5.0$ Vdc)	2N5400		40	180	
	2N5401		60	240	
($I_C = 50$ mAdc, $V_{CE} = 5.0$ Vdc)	2N5400		40	–	
	2N5401		50	–	
*Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
($I_C = 10$ mAdc, $I_B = 1.0$ mAdc)			–	0.20	
($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)			–	0.5	
*Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
($I_C = 10$ mAdc, $I_B = 1.0$ mAdc)			–	1.0	
($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)			–	1.0	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product		f_T			MHz
($I_C = 10$ mAdc, $V_{CE} = 10$ Vdc, f = 100 MHz)	2N5400		100	400	
	2N5401		100	300	
Output Capacitance		C_{ob}			pF
($V_{CB} = 10$ Vdc, $I_E = 0$, f = 1.0 MHz)			–	6.0	
Small-Signal Current Gain		h_{fe}			–
($I_C = 1.0$ mAdc, $V_{CE} = 10$ Vdc, f = 1.0 kHz)	2N5400		30	200	
	2N5401		40	200	
Noise Figure		NF			dB
($I_C = 250\ \mu$Adc, $V_{CE} = 5.0$ Vdc, $R_S = 1.0$ k ohm, f = 10 Hz to 15.7 kHz)			–	8.0	

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 1 – DC CURRENT GAIN

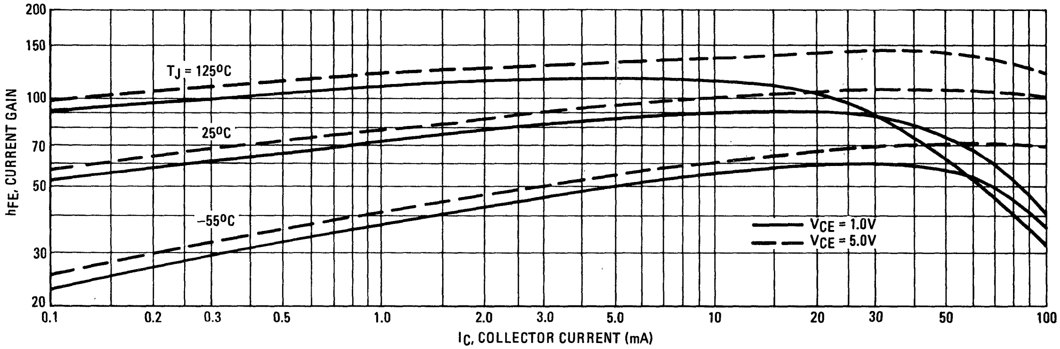


FIGURE 2 – COLLECTOR SATURATION REGION

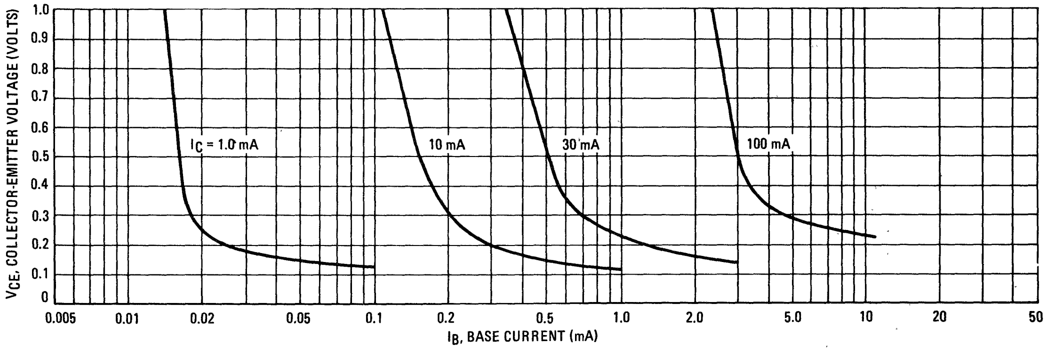


FIGURE 3 – COLLECTOR CUT-OFF REGION

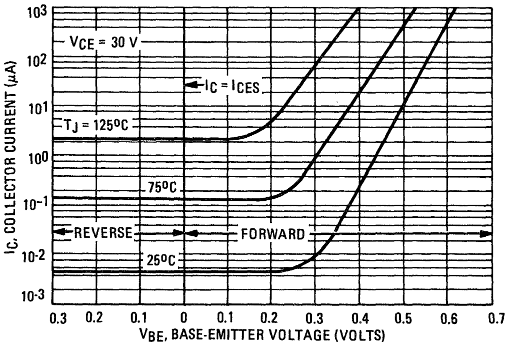


FIGURE 4 – "ON" VOLTAGES

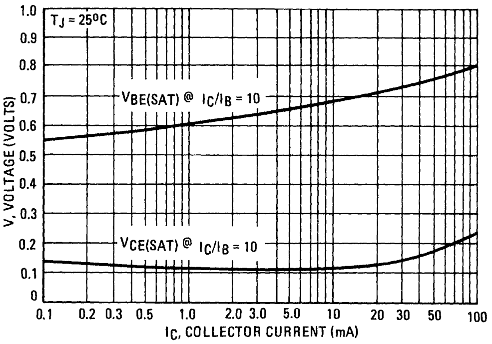


FIGURE 5 – TEMPERATURE COEFFICIENTS

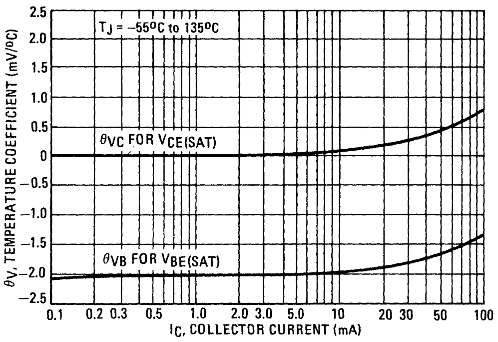


FIGURE 6 – SWITCHING TIME TEST CIRCUIT

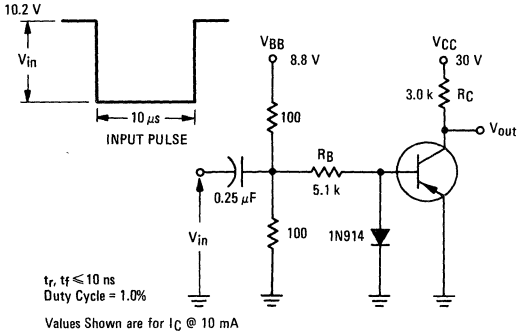


FIGURE 7 – CAPACITANCES

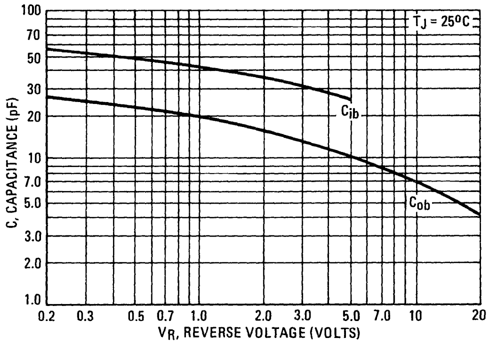


FIGURE 8 – TURN-ON TIME

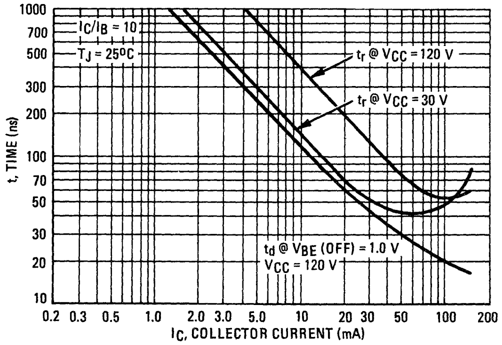
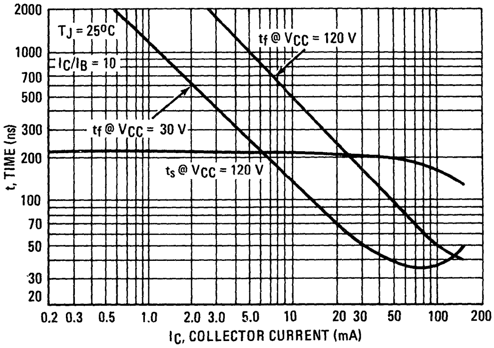
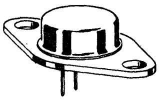


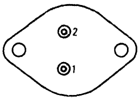
FIGURE 9 – TURN-OFF TIME



2N5427 (SILICON)
thru
2N5430



CASE 80
(TO-66)
Collector connected to case



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

Medium-power NPN silicon transistors designed for switching and wide-band amplifier applications.

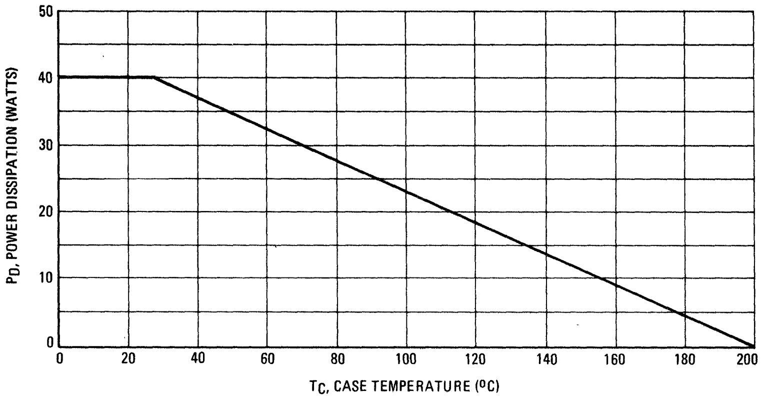
MAXIMUM RATINGS

Rating	Symbol	2N5427 2N5428	2N5429 2N5430	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	7.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	40 228		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.37	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

2N5427 thru 2N5430 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N5427, 2N5428	-	$BV_{CEO(sus)}$	80	-	Vdc
	2N5429, 2N5430			100	-	
Collector Cutoff Current (V_{CE} = 75 Vdc, I_B = 0)	2N5427, 2N5428		I_{CEO}	-	100	μAdc
(V_{CE} = 90 Vdc, I_B = 0)	2N5429, 2N5430			-	100	
Collector Cutoff Current (V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5427, 2N5428	12	I_{CEX}	-	10	μAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5429, 2N5430			-	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5427, 2N5428			-	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5429, 2N5430			-	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		-	I_{CBO}	-	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		-	I_{EBO}	-	100	μAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5427, 2N5429	8	h_{FE}	30	-	-
	2N5428, 2N5430			60	-	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5427, 2N5429			30	120	
	2N5428, 2N5430			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5427, 2N5429			20	-	
	2N5428, 2N5430			40	-	
Collector-Emitter Saturation Voltage (1) (I_C = 2.0 Adc, I_B = 0.2 Adc)		9, 11, 13	$V_{CE(sat)}$	-	0.7	Vdc
(I_C = 7.0 Adc, I_B = 0.7 Adc)				-	1.2	
Base-Emitter Saturation Voltage (1) (I_C = 2.0 Adc, I_B = 0.2 Adc)		11, 13	$V_{BE(sat)}$	-	1.2	Vdc
(I_C = 7.0 Adc, I_B = 0.7 Adc)				-	2.0	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		-	f_T	30	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		7	C_{ob}	-	250	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		7	C_{ib}	-	1,000	pF
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc, I_C = 2.0 Adc, I_{B1} = 200 mAdc)	2,3	t_d	-	100	ns
Rise Time			t_r	-	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc, I_{B1} = I_{B2} = 200 mAdc)	2,6	t_s	-	2.0	μs
Fall Time			t_f	-	200	ns

(1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

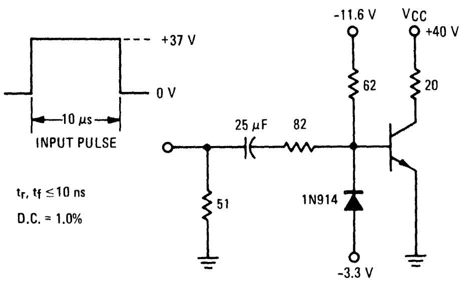


FIGURE 3 – TURN-ON TIME

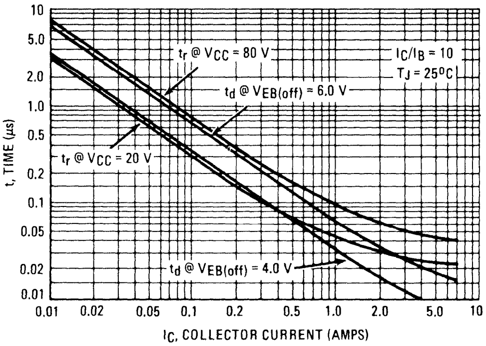


FIGURE 4 — THERMAL RESPONSE

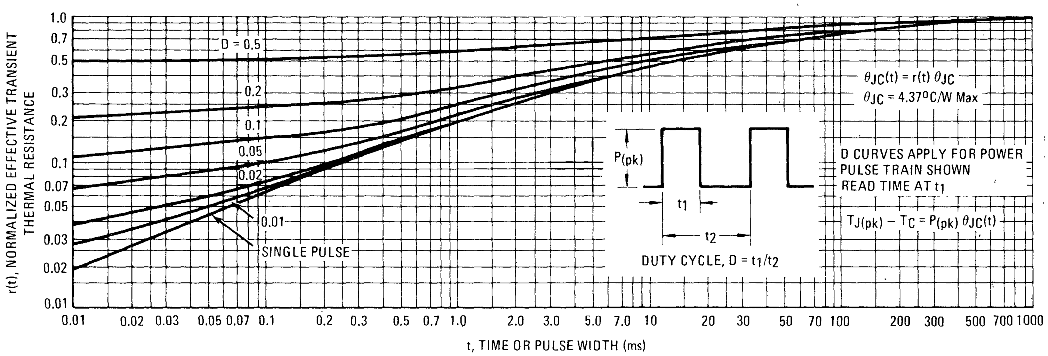
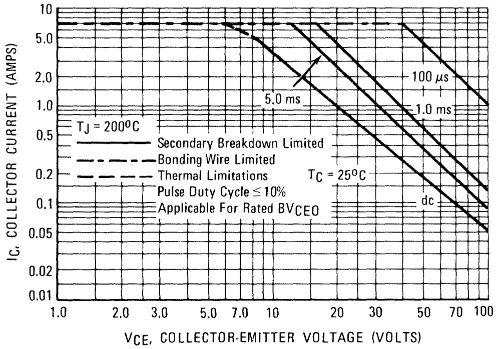


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — TURN-OFF TIME

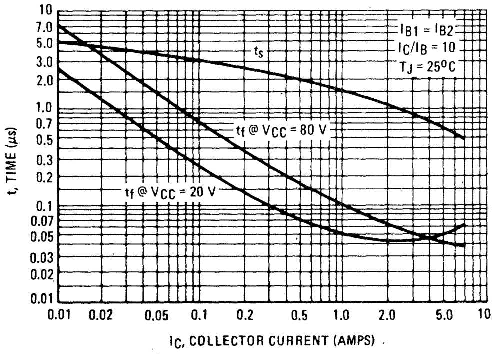


FIGURE 7 — CAPACITANCE versus VOLTAGE

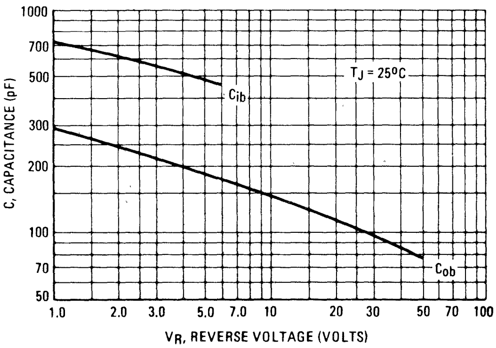


FIGURE 8 – DC CURRENT GAIN

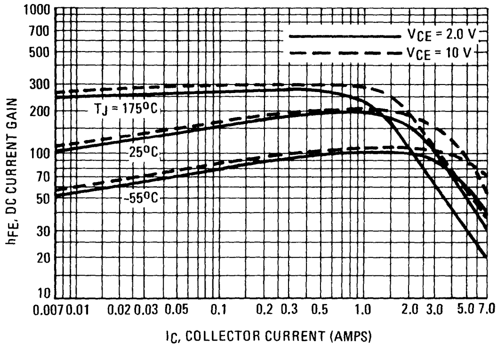


FIGURE 9 – COLLECTOR SATURATION REGION

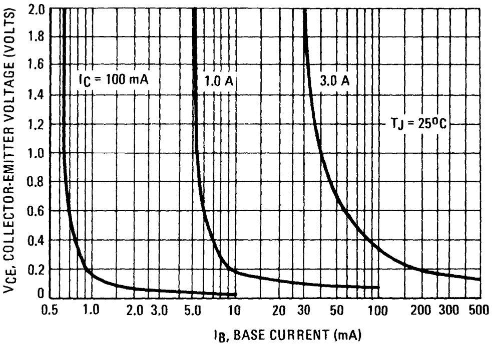


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

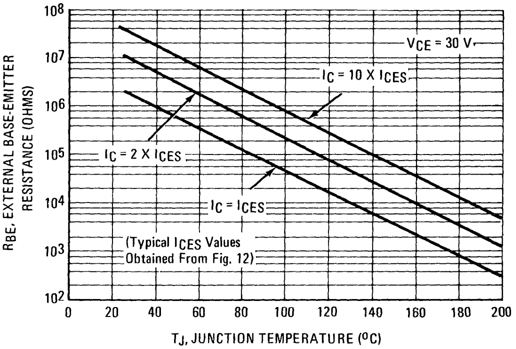


FIGURE 11 – "ON" VOLTAGES

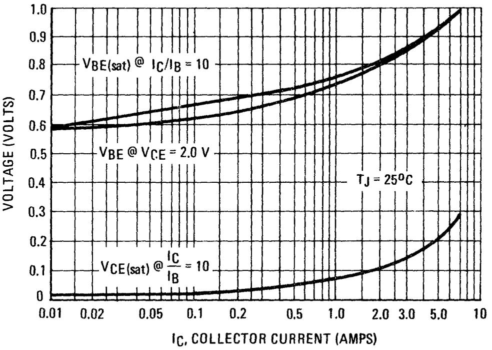


FIGURE 12 – COLLECTOR CUT-OFF REGION

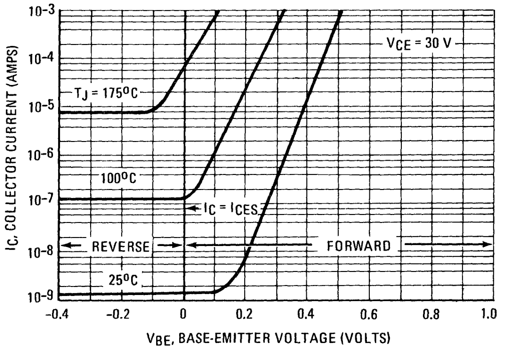
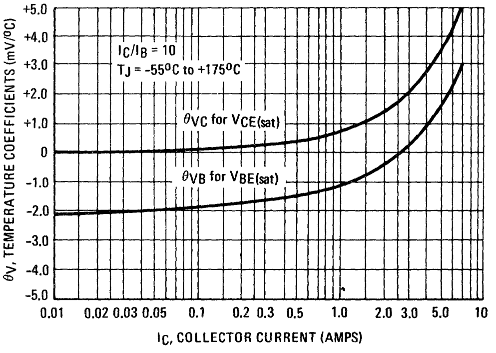
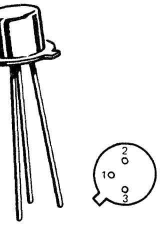


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5431 (SILICON)



STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

CASE 22A
(TO-18 Modified)
Lead 3 connected to case

Silicon annular unijunction transistors characterized primarily for low interbase-voltage operation in sensing, pulse triggering, and timing circuits.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D*	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current **	i_e**	1.5	A
Emitter Reverse Voltage	V_{B2E}	30	V
Interbase Voltage ‡	V_{B2B10}‡	35	V
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Derate 3.0 mW/°C increase in ambient temperature.
**Duty Cycle ≤ 1.0%, PRR = 10 PPS (see figure 5).
‡Based upon power dissipation at T_A = 25°C.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

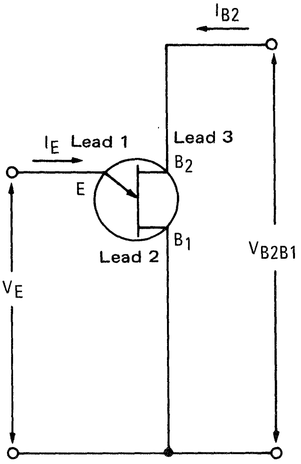
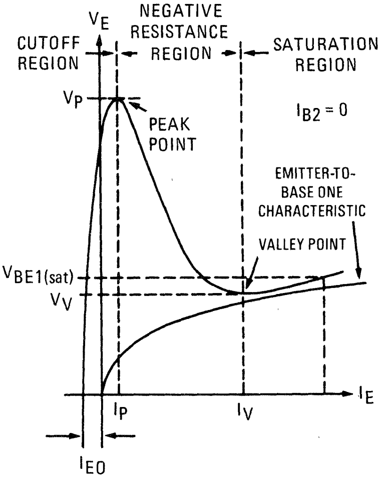


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
Intrinsic Standoff Ratio① (V_{B2B1} = 10 V)	4	η①	0.72	0.80	-
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		R_{BB}	6.0	8.5	kΩ
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = 0 to 100°C)		αR_{BB}	0.4	0.8	%/°C
Emitter Saturation Voltage ② (V_{B2B1} = 10 V, I_E = 50 mA)		$V_{EB1(sat)}$②	-	3.0	V
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	5.0	30	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		I_{EB2O}	-	10	nA
Peak-Point Emitter Current (V_{B2B1} = 25 V) (V_{B2B1} = 4.0 V)		I_P	- -	0.4 4.0	μA
Valley-Point Current② (V_{B2B1} = 20 V, R_{B2} = 100 ohms)		I_V ②	2.0	-	mA
Base-One Peak Pulse Voltage (V_{BB} = 4.0 volts)	3	V_{OB1}	1.0	-	V

①η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B10} + V_F$, where V_F is about 0.49 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

② Use pulse techniques: PW ≈ 300 μs, Duty Cycle ≤ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 — V_{OB1} TEST CIRCUIT

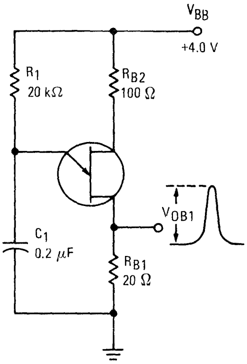
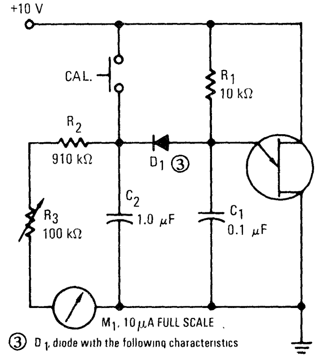


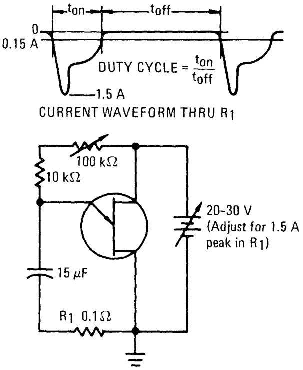
FIGURE 4 — η TEST CIRCUIT



③ D_1, diode with the following characteristics
V_F = 0.49 V @ I_F = 10 μA
I_R ≤ 2.0 μA @ V_R = 20 V

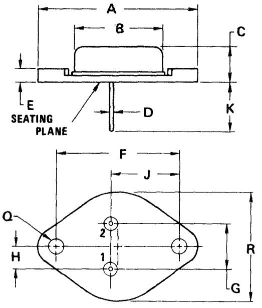
FIGURE 5 — PRR TEST CIRCUIT AND WAVEFORM

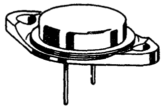
DUTY CYCLE ≤ 1.0%, PRR ≤ 10 PPS



2N5435 (GERMANIUM)
thru
2N5440

PNP germanium power switching transistors designed for high-current, fast-switching applications requiring low saturation voltage and excellent safe operating area.

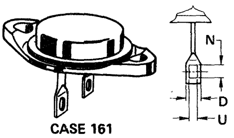




CASE 3-04

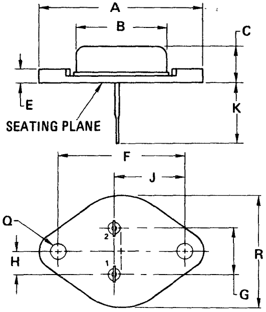
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	–	9.14	–	0.360
D	1.52	1.65	0.060	0.065
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	15.49	18.03	0.610	0.710
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050



CASE 161

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	–	9.14	–	0.360
D	–	3.56	–	0.140
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	15.49	17.27	0.610	0.680
N	3.05	3.30	0.120	0.130
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
U	1.83	–	0.072	–



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

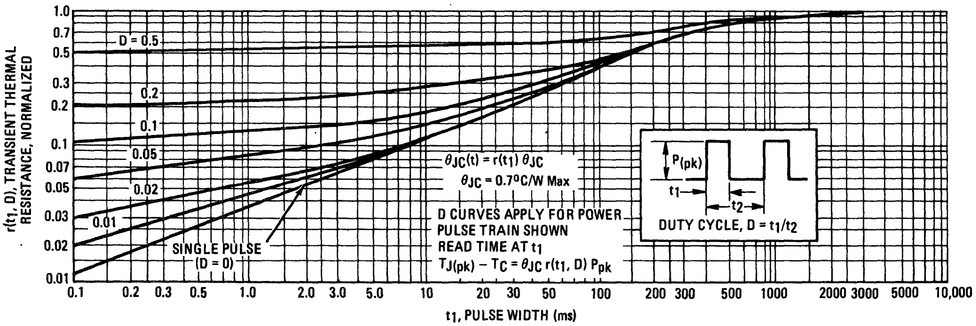
MAXIMUM RATINGS **

Rating	Symbol	2N5435 2N5438	2N5436 2N5439	2N5437 2N5440	Unit
Collector-Emitter Voltage	V_{CEO}	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	80	110	140	Vdc
Emitter-Base Voltage	V_{EB}	2.5			Vdc
Collector Current — Continuous	I_C	60			Adc
Base Current — Continuous	I_B	12			Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	120 1.43			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +110			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

FIGURE 1 – THERMAL RESPONSE



**Maximum Ratings for MP5435 Series are the Same as the 2N5435 Series.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)**

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 0.1 Adc, I_B = 0) 2N5435, 2N5438	BV_{CEO}	60	-	Vdc
2N5436, 2N5439		90	-	
2N5437, 2N5440		120	-	
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 0.2 Vdc) 2N5435, 2N5438	I_{CEX}	-	10	mAdc
(V_{CE} = 110 Vdc, $V_{BE(off)}$ = 0.2 Vdc) 2N5436, 2N5439		-	10	
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 0.2 Vdc) 2N5437, 2N5440		-	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 0.2 Vdc, T_C = +85°C) 2N5435, 2N5438		-	30	
(V_{CE} = 110 Vdc, $V_{BE(off)}$ = 0.2 Vdc, T_C = +85°C) 2N5436, 2N5439		-	30	
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 0.2 Vdc, T_C = +85°C) 2N5437, 2N5440		-	30	
Collector Cutoff Current (V_{CB} = 2.0 Vdc, I_E = 0)	I_{CBO}	-	200	µAdc
Emitter Cutoff Current (V_{BE} = 2.5 Vdc, I_C = 0)	I_{EBO}	-	500	mAdc
ON CHARACTERISTICS				
DC Current Gain* (I_C = 25 Adc, V_{CE} = 2.0 Vdc) 2N5435, 2N5436, 2N5437	h_{FE}*	20	60	
2N5438, 2N5439, 2N5440		40	120	
(I_C = 60 Adc, V_{CE} = 2.0 Vdc) 2N5435, 2N5436, 2N5437		10	-	
2N5438, 2N5439, 2N5440		15	-	
Collector-Emitter Saturation Voltage* (I_C = 60 Adc, I_B = 6.0 Adc) 2N5435, 2N5436, 2N5437	$V_{CE(sat)}$*	-	0.75	Vdc
2N5438, 2N5439, 2N5440		-	0.50	
Base-Emitter Saturation Voltage* (I_C = 60 Adc, I_B = 6.0 Adc) 2N5435, 2N5436, 2N5437	$V_{BE(sat)}$*	-	1.2	Vdc
2N5438, 2N5439, 2N5440		-	0.9	
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain–Bandwidth Product (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc, f = 100 kHz)	f_T	350	-	kHz
SWITCHING CHARACTERISTICS				
Rise Time (I_C = 25 Adc, I_{B1} = 2.5 Adc, I_{B2} = 2.5 Adc) (See Figure 4)	t_r	-	12	µs
Storage Time	t_s	-	10	µs
Fall Time	t_f	-	8.0	µs

**Electrical Characteristics for MP5435 series are the same as the 2N5435 series.
* To avoid excessive heating of the collector junction, perform test with pulse method.

FIGURE 2 – POWER-TEMPERATURE DERATING CURVE

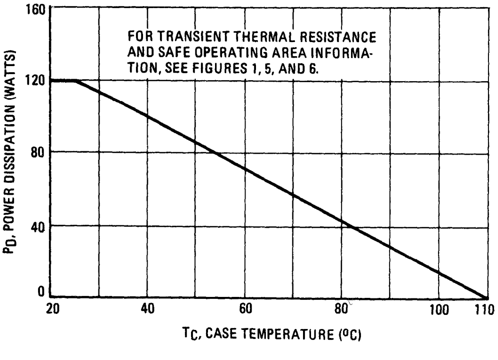


FIGURE 3 – SWITCHING TIMES

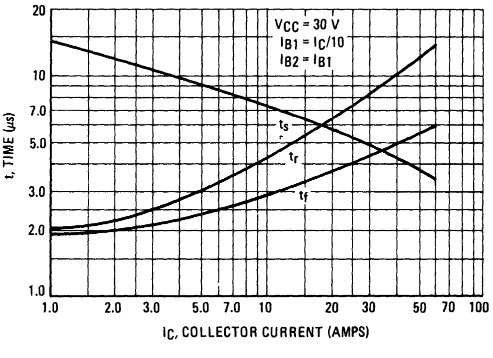


FIGURE 4 – SWITCHING TIME TEST CIRCUIT

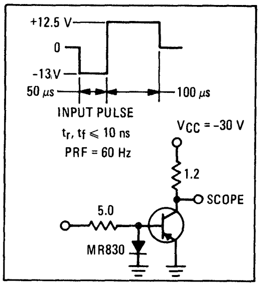
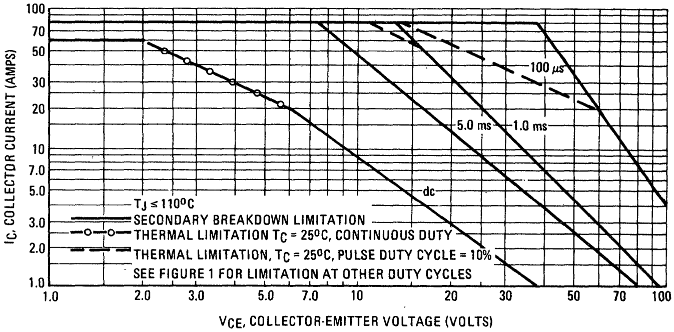


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 110°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} < 110°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – CLAMPED INDUCTIVE SAFE OPERATING AREA

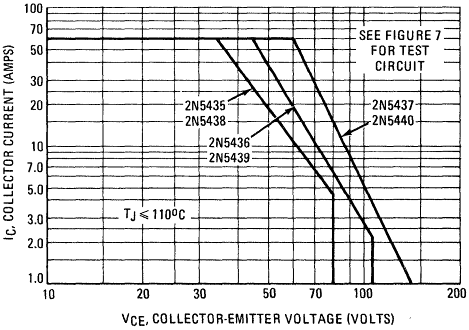
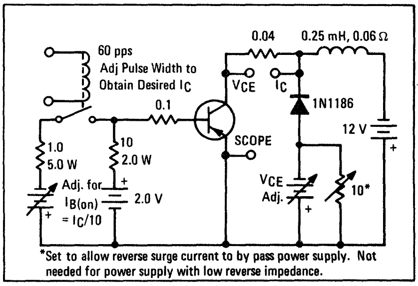


FIGURE 7 – CLAMPED INDUCTIVE SAFE OPERATING AREA TEST CIRCUIT



*Set to allow reverse surge current to by pass power supply. Not needed for power supply with low reverse impedance.

FIGURE 8 – DC CURRENT GAIN

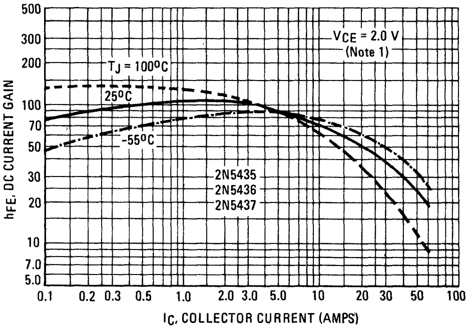
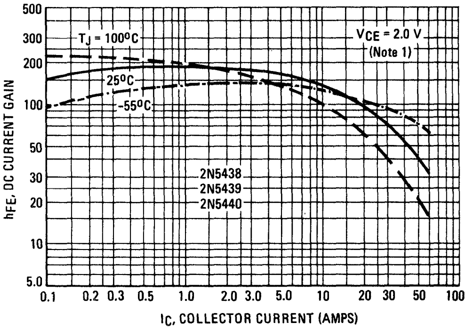


FIGURE 9 – DC CURRENT GAIN



NOTE 1: Data is obtained from pulse tests and adjusted to nullify the effect of I_{CBO}.

FIGURE 10 – COLLECTOR SATURATION REGION

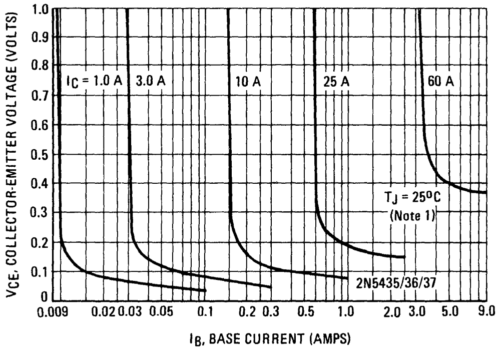


FIGURE 11 – COLLECTOR SATURATION REGION

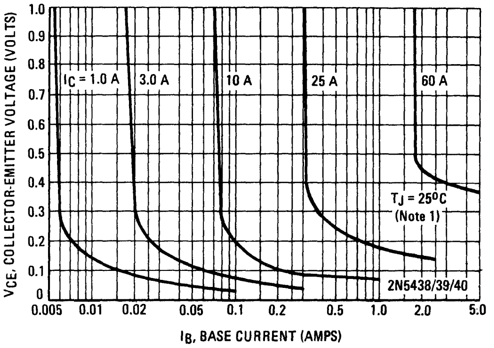


FIGURE 12 – EFFECTS OF BASE-EMITTER RESISTANCE

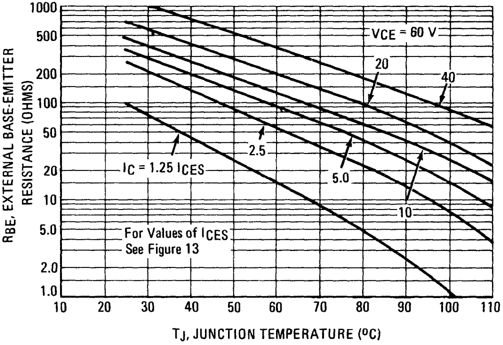


FIGURE 13 – COLLECTOR CUTOFF REGION

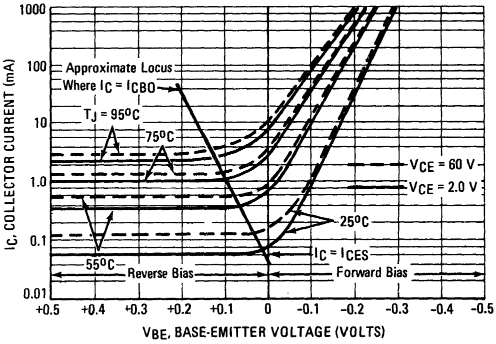


FIGURE 14 – "ON" VOLTAGES

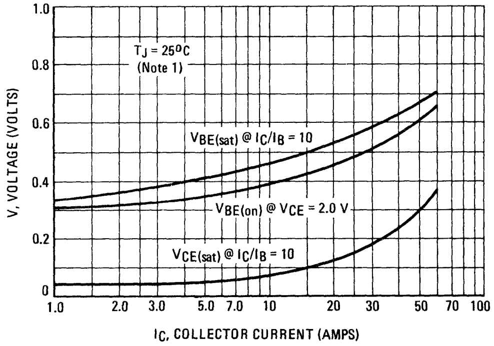
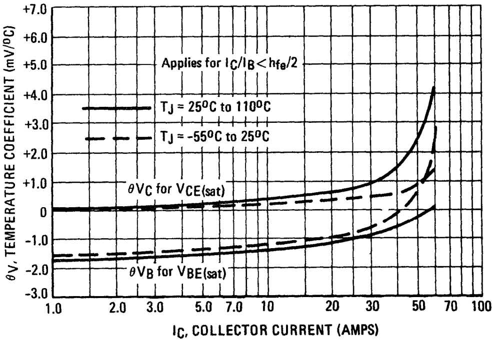
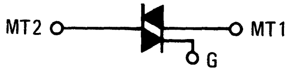


FIGURE 15 – TEMPERATURE COEFFICIENTS



2N5441 thru 2N5446 (SILICON)
MAC40688 thru MAC40690



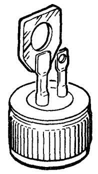
TRIACS
(THYRISTORS)

40 AMPERES RMS

SILICON BIDIRECTIONAL THYRISTORS

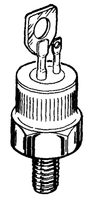
. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants



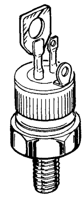
2N5441
2N5442
2N5443

CASE 237



2N5444
2N5445
2N5446

CASE 238



MAC40688
MAC40689
MAC40690

CASE 239

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage (1) (T_J = -65 to +110°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open *Peak Principal Voltage 2N5441, 2N5444, MAC40688 2N5442, 2N5445, MAC40689 2N5443, 2N5446, MAC40690	V_{DRM}	 200 400 600	Volts
*Peak Gate Voltage	V_{GM}	30	Volts
*On-State Current RMS (T_C = -65 to +70°C) (T_C = +100°C) Full Sine Wave, 50 to 60 Hz	$I_{T(RMS)}$	 40 20	Amp
*Peak Surge Current (One Full Cycle of surge current at 60 Hz, preceeded and followed by a 40 A RMS current, T_J = +110°C)	I_{TSM}	300	Amp
*Peak Gate Power (Pulse Width = 10 µs Max)	P_{GM}	40	Watts
*Average Gate Power	$P_{G(AV)}$	0.75	Watt
*Peak Gate Current (10 µs Max)	I_{GM}	4.0	Amp
*Operating Junction Temperature Range	T_J	-65 to +110	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case 2N5441, 2N5442, 2N5443 2N5444, 2N5445, 2N5446 MAC40688, MAC40689, MAC40690	$R_{\theta JC}$	 0.8 0.9 1.0	°C/W

*Indicates JEDEC Registered Data for 2N5441 thru 2N5446.

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

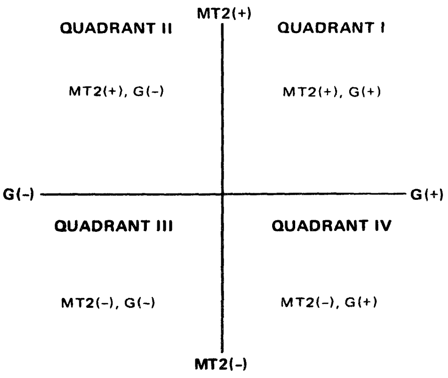
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C	I_{DRM}	–	0.5	4.0	mA
*On-State Voltage (Either Direction) I_{TM} = 56 A Peak, Pulse Width ≤1.0 ms, Duty Cycle ≤2.0%	V_{TM}	–	1.65	1.85	Volts
Gate Trigger Current (1) Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	I_{GT}				mA
MT2 (+), G(+)		–	15	70	
MT2 (+), G(–)		–	15	70	
MT2 (–), G(–)		–	15	70	
MT2 (–), G(+)		–	20	100	
*MT2 (+), G(+); MT2 (–), G (–) T_C = -65°C		–	–	125	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -65°C		–	–	240	
Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	V_{GT}				Volts
MT2 (+), G(+)		–	1.1	2.0	
MT2 (+), G(–)		–	1.1	2.0	
MT2 (–), G(–)		–	1.1	2.0	
MT2 (–), G(+)		–	1.3	2.5	
*All Quadrants, T_C = -65°C)		–	–	3.4	
*Main Terminal Voltage = Rated V_{DRM} = R_L = 10 k ohms, T_J = +110°C		0.2	–	–	
Holding Current Main Terminal Voltage = 12 Vdc, Gate Open Initiating Current = 150 mA	I_H				mA
MT2 (+)		–	10	70	
MT2 (–)		–	10	70	
*Either Direction, T_C = -65°C		–	–	100	
*Turn-On Time Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 56 A, Gate Source Voltage = 12 V, R_S = 12 Ohms, Rise Time = 0.1 µs, Pulse Width = 2.0 µs	t_{gt}	–	1.0	2.0	µs
*Critical Rate-of -Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 40 A, Commutating di/dt = 22 A/ms, gate energized	dv/dt				V/µs
T_C = 70°C 2N5441, 2N5442, 2N5443		5.0	30	–	
= 65°C 2N5444, 2N5445, 2N5446		5.0	30	–	
= 60°C MAC40688, MAC40689, MAC40690		5.0	30	–	
Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 110°C					
2N5441, 2N5444, MAC40688		50			
2N5442, 2N5445, MAC40689		30			
2N5443, 2N5446, MAC40690		20			

*Indicates JEDEC Registered Data for 2N5441 thru 2N5446.

(1) All voltage polarity referenced to Main Terminal 1.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 – 10 V	7.5 – 9.0 V	3.0 – 5.0 V
I_S	350 µA Max	120 µA Max	100 – 400 µA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – POWER DISSIPATION versus ON-STATE CURRENT

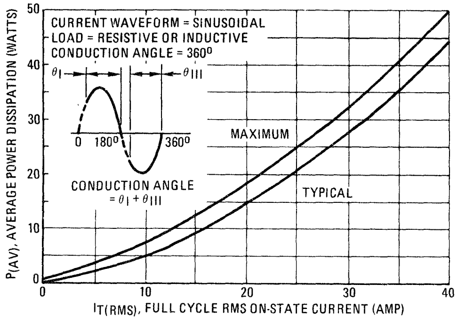


FIGURE 2 – CASE TEMPERATURE versus ON-STATE CURRENT

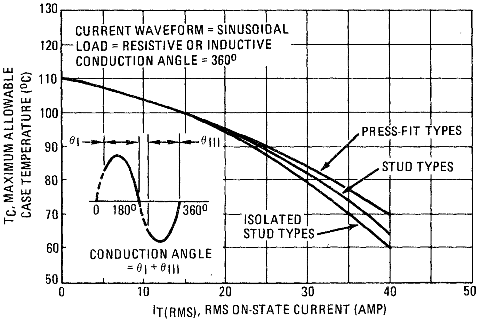


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

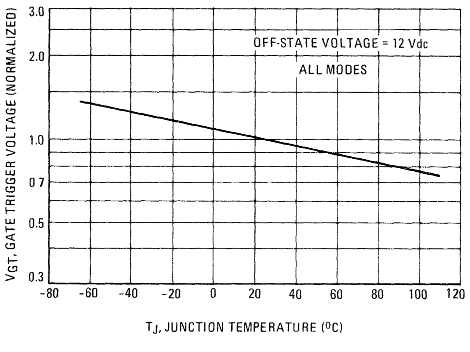


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

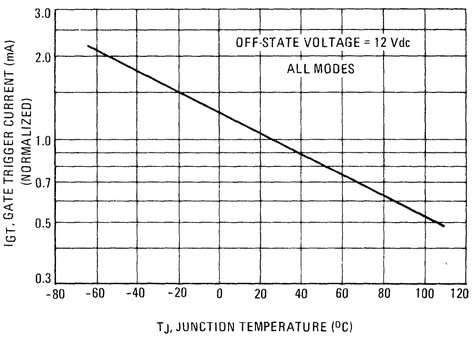


FIGURE 5 – TYPICAL THERMAL RESPONSE

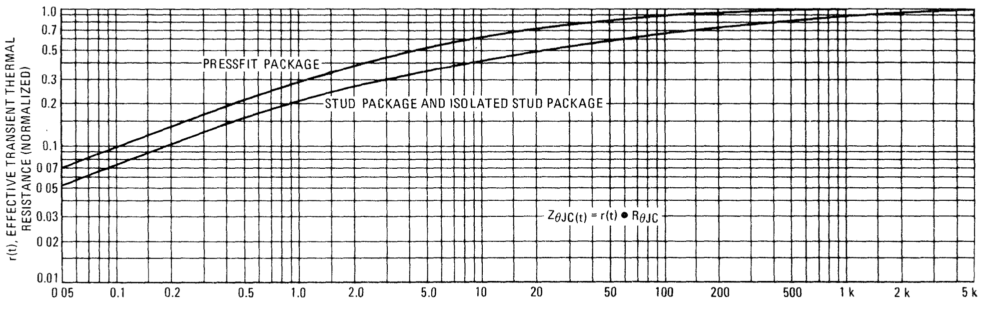


FIGURE 6 – MAXIMUM ON-STATE CHARACTERISTICS

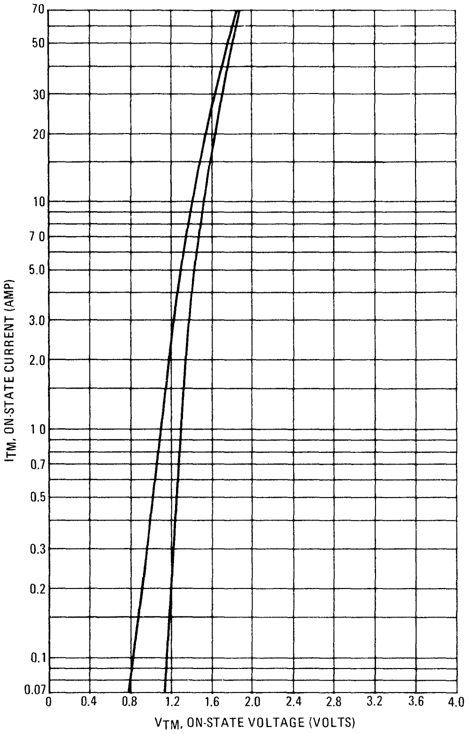


FIGURE 7 – TYPICAL HOLDING CURRENT

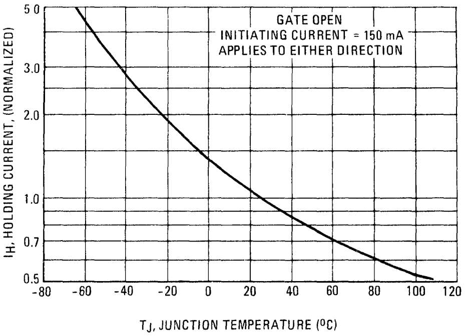
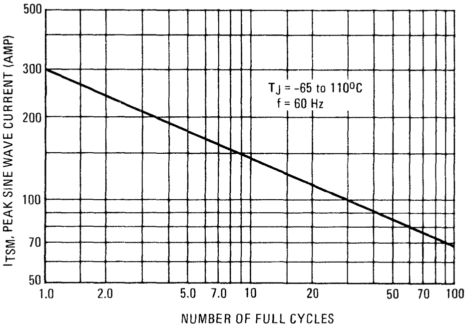
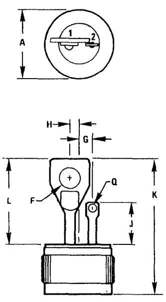


FIGURE 8 – MAXIMUM ALLOWABLE SURGE CURRENT



CASE 237

2N5441
2N5442
2N5443



Pin 1 MT1
2 Gate
Case MT2

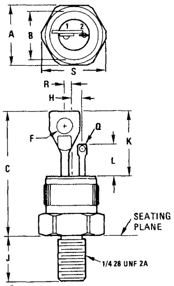
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12 73	12 83	0 501	0 505
F	–	4 06	–	0 160
G	2 16	2 41	0 085	0.095
H	1 52	1.78	0 060	0.070
J	6 99	7 75	0 275	0 305
K	–	26 67	–	1.050
L	–	17 02	–	0 670
Q	1 40	1 65	0 055	0 065

NOTE
1 DIM "G" & "H" TO BE MEASURED AT CAN

CASE 237-01

CASE 238

2N5444
2N5445
2N5446



Pin 1 MT1
2 Gate
Stud MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14 00	14.20	0 551	0 559
B	12 73	12.83	0 501	0 505
C	–	30.23	–	1 190
F	–	4.06	–	0 160
H	2 16	2 41	0 085	0 095
J	10 67	11 56	0 420	0 455
K	–	17 02	–	0.670
L	6 99	7 75	0 275	0 305
Q	1 40	1 65	0 055	0 065
R	1 52	1 78	0 060	0 070
S	15 34	15 60	0 604	0 614

NOTE
1 DIM "H" & "R" TO BE
MEASURED AT CAN

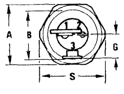
CASE 238-01

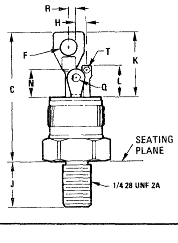
CASE 239

MAC40688
MAC40689
MAC40690

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14 00	14 20	0 551	0 559
B	12 73	12 83	0 501	0 505
C	–	32 51	–	1 280
F	–	4.06	–	0 160
G	–	6 48	–	0.255
H	2 16	2.41	0 085	0.095
J	10.67	11 56	0 420	0 455
K	–	17.02	–	0.670
L	6.99	7.75	0 275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3 81	0.135	0 150
R	1 52	1 78	0 060	0.070
S	15.34	15 60	0 604	0 614
T	1 40	1 65	0 055	0.065

NOTE
1 DIM "G", "H" & "R" TO BE MEASURED AT CAN

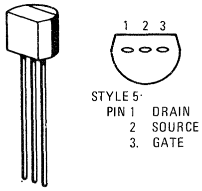




Pin 1 MT1
2 Gate
3. MT2
Stud Isolated

2N5457 (SILICON)
2N5458
2N5459

Silicon N-channel junction field-effect transistors depletion mode (Type A) designed for general-purpose audio and switching applications.



CASE 29
(TO-92)

Drain and source may be interchanged.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D (2)	310 2.82	mW mW/°C
Operating Junction Temperature	T_J (2)	135	°C
Storage Temperature Range	T_{stg} (2)	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage ($I_G = -10\mu Adc$, $V_{DS} = 0$)	BV_{GSS}	25	—	—	Vdc
Gate Reverse Current ($V_{GS} = -15$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	—	1.0	nAdc
($V_{GS} = -15$ Vdc, $V_{DS} = 0$, $T_A = 100°C$)		—	—	200	
Gate-Source Cutoff Voltage ($V_{DS} = 15$ Vdc, $I_D = 10$ nAdc) 2N5457	$V_{GS(off)}$	0.5	—	6.0	Vdc
2N5458		1.0	—	7.0	
2N5459		2.0	—	8.0	
Gate-Source Voltage ($V_{DS} = 15$ Vdc, $I_D = 100\mu Adc$) 2N5457	V_{GS}	—	2.5	—	Vdc
($V_{DS} = 15$ Vdc, $I_D = 200\ \mu Adc$) 2N5458		—	3.5	—	
($V_{DS} = 15$ Vdc, $I_D = 400\ \mu Adc$) 2N5459		—	4.5	—	
ON CHARACTERISTICS					
Zero-Gate-Voltage Drain Current (1) ($V_{DS} = 15$ Vdc, $V_{GS} = 0$) 2N5457	I_{DSS}	1.0	3.0	5.0	mAdc
2N5458		2.0	6.0	9.0	
2N5459		4.0	9.0	16	
DYNAMIC CHARACTERISTICS					
Forward Transfer Admittance (1) ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1 kHz) 2N5457	$\|y_{fs}\|$	1000	3000	5000	µmhos
2N5458		1500	4000	5500	
2N5459		2000	4500	6000	
Output Admittance (1) ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1 kHz)	$\|y_{os}\|$	—	10	50	µmhos
Input Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1 MHz)	C_{iss}	—	4.5	7.0	pF
Reverse Transfer Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1 MHz)	C_{rss}	—	1.5	3.0	pF

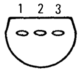
(1) Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

(2) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows. $P_D = 1.0$ W @ $T_C = 25°C$, Derate above 25°C – 8.0 mW/°C, $T_J = -65$ to +150°C, $\theta_{JC} = 125°$ C/W.

2N5460 (SILICON)
thru
2N5465

P-channel depletion mode (Type A) junction field-effect transistors designed for use in general-purpose amplifier applications.

CASE 29
(TO-92)



STYLE 7·
PIN 1 SOURCE
2 DRAIN
3. GATE

MAXIMUM RATINGS

Rating	Symbol	2N5460 2N5461 2N5462	2N5463 2N5464 2N5465	Unit
Drain-Gate Voltage	V_{DG}	40	60	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	40	60	Vdc
Forward Gate Current	$I_{G(f)}$	10		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D(1)	310 2.82		mW mW/°C
Storage Temperature Range	T_{stg}(1)	-65 to +150		°C
Operating Junction Temperature Range	T_J(1)	-65 to +135		°C

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows. P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125°C/W.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0) 2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465	$V_{(BR)GSS}$	40 60	- -	- -	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc) 2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	$V_{GS(off)}$	0.75 1.0 1.8	- - -	6.0 7.5 9.0	Vdc
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0) 2N5460, 2N5461, 2N5462	I_{GSS}	-	-	5.0	nAdc
(V_{GS} = 30 Vdc, V_{DS} = 0) 2N5463, 2N5464, 2N5465		-	-	5.0	
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C) 2N5460, 2N5461, 2N5462		-	-	1.0	μAdc
(V_{GS} = 30 Vdc, V_{DS} = 0, T_A = 100°C) 2N5463, 2N5464, 2N5465		-	-	1.0	
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0) 2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	I_{DSS}	1.0 2.0 4.0	- - -	5.0 9.0 16	mAdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 0.1 mAdc) 2N5460, 2N5463	V_{GS}	0.5	-	4.0	Vdc
(V_{DS} = 15 Vdc, I_D = 0.2 mAdc) 2N5461, 2N5464		0.8	-	4.5	
(V_{DS} = 15 Vdc, I_D = 0.4 mAdc) 2N5462, 2N5465		1.5	-	6.0	
SMALL-SIGNAL CHARACTERISTICS					
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz) 2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	$\|y_{fs}\|$	1000 1500 2000	- - -	4000 5000 6000	μmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{os}\|$	-	-	75	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	-	5.0	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	-	1.0	2.0	pF
Common-Source Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 100 Hz, BW = 1.0 Hz)	NF	-	1.0	2.5	dB
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)	e_n	-	60	115	nV/√Hz

DRAIN CURRENT versus GATE SOURCE VOLTAGE

FIGURE 1 – 2N5460 and 2N5463

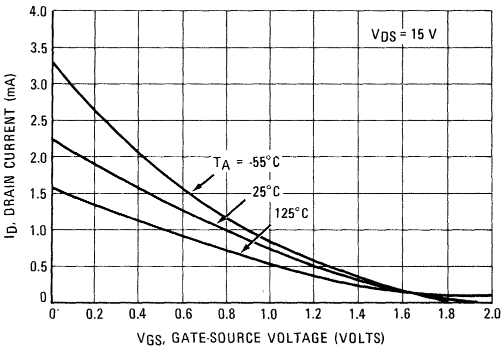


FIGURE 2 – 2N5461 and 2N5464

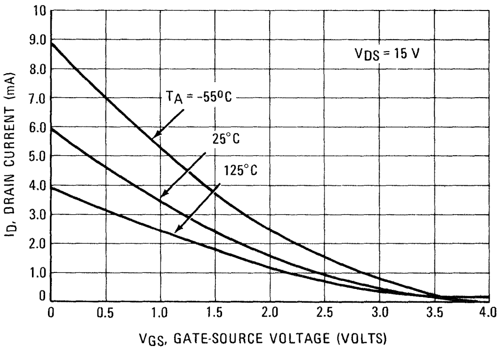
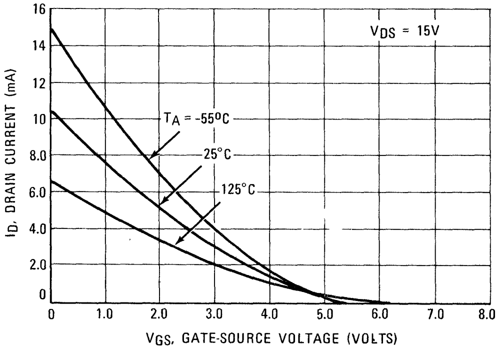


FIGURE 3 – 2N5462 and 2N5465



FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

FIGURE 4 – 2N5460 and 2N5463

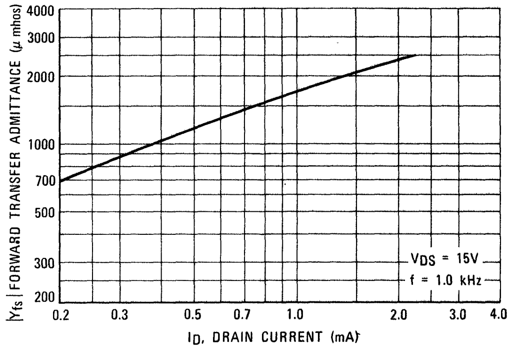


FIGURE 5 – 2N5461 and 2N5464

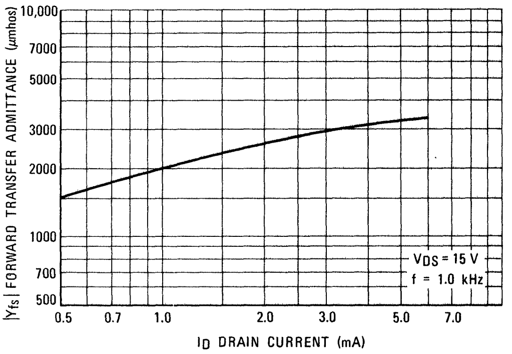


FIGURE 6 – 2N5462 and 2N5465

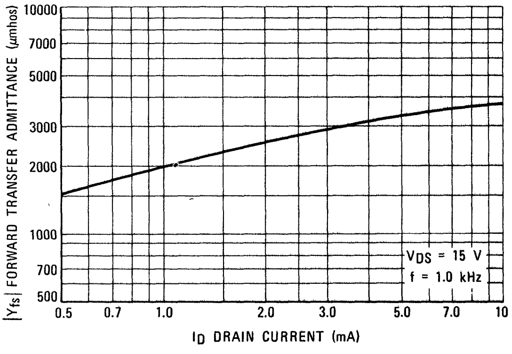


FIGURE 7 – OUTPUT RESISTANCE VERSUS DRAIN CURRENT

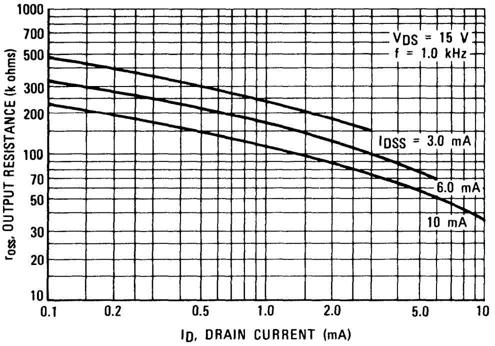


FIGURE 8 – CAPACITANCE VERSUS DRAIN-SOURCE VOLTAGE

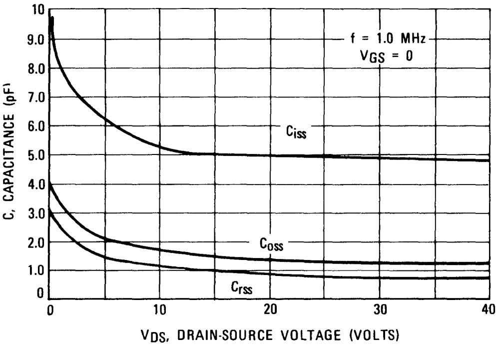


FIGURE 9 – NOISE FIGURE VERSUS FREQUENCY

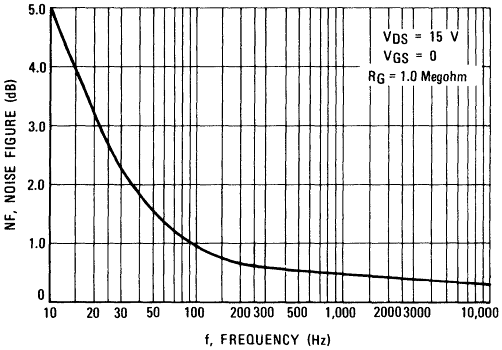


FIGURE 10 – NOISE FIGURE VERSUS SOURCE RESISTANCE

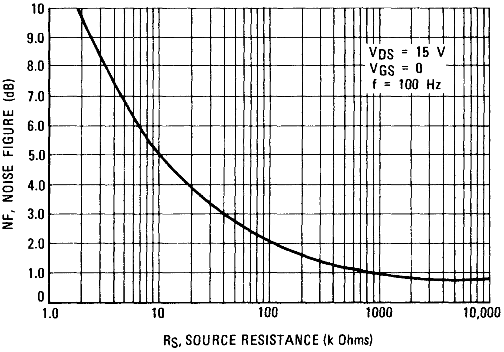
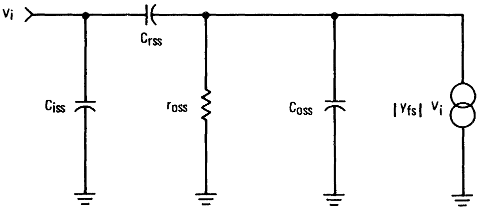


FIGURE 11 – EQUIVALENT LOW FREQUENCY CIRCUIT



Common Source
y Parameters for Frequencies
Below 30 MHz

$y_{is} = j\omega C_{iss}$

$y_{os} = j\omega C_{osp}{}^{*} + 1/r_{oss}$

$y_{fs} = |y_{fs}|$

$y_{rs} = -j\omega C_{rss}$

*C_{osp} is C_{oss} in parallel with Series Combination of C_{iss} and C_{rss}.

NOTE:

1. Graphical data is presented for dc conditions. Tabular data is given for pulsed conditions (Pulse Width = 630 ms, Duty Cycle = 10%).

2N5471 (SILICON)
thru
2N5476

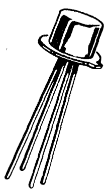
P-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

Depletion mode Junction Field-Effect Transistors designed for general-purpose amplifier and switching applications.

- High Gate-Source Breakdown Voltage — $V_{(BR)GSS}$ = 40 Vdc (Min) for All Types
- High DC Input Resistance — I_{GSS} = 100 pAdc (Max) @ V_{GS} = 10 Vdc
- Low Reverse Transfer Capacitance — C_{rss} = 1.0 pF (Max) @ V_{DS} = −15 Vdc
- Tight I_{DSS} Range for Easier Circuit Design
- Drain and Source Interchangeable

P-CHANNEL

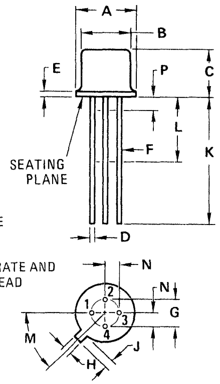
JUNCTION FIELD-EFFECT TRANSISTORS



***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	40	Vdc
Reverse Gate-Source Voltage	V_{GSR}	40	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 2.0	mW mW/°C
Operating Channel Temperature Range	$T_{channel}$	-65 to +175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



STYLE 2
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SUBSTRATE AND CASE LEAD

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45°BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = 10 µAdc, V_{DS} = 0)		$V_{(BR)GSS}$	40	–	Vdc
Gate-Source Cutoff Voltage		$V_{GS(off)}$			Vdc
(V_{DS} = -15 Vdc, I_D = -10 nAdc)	2N5471		0.5	4.0	
	2N5472		0.7	4.0	
	2N5473		0.9	6.0	
	2N5474		1.2	7.0	
	2N5475		1.5	8.0	
	2N5476		2.0	9.0	
Reverse Gate Current		I_{GSS}			nAdc
(V_{GS} = 10 Vdc, V_{DS} = 0)			–	0.1	
(V_{GS} = 20 Vdc, V_{DS} = 0)			–	0.5	
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 150°C)			–	1.0	µAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (1)		I_{DSS}			mAdc
(V_{DS} = -15 Vdc, V_{GS} = 0)	2N5471		0.02	0.06	
	2N5472		0.05	0.12	
	2N5473		0.10	0.25	
	2N5474		0.20	0.50	
	2N5475		0.40	1.0	
	2N5476		0.80	2.0	
Gate-Source Voltage		V_{GS}			Vdc
(V_{DS} = -15 Vdc, I_D = 2.0 µAdc)	2N5471		0.5	3.0	
(V_{DS} = -15 Vdc, I_D = 5.0 µAdc)	2N5472		0.7	3.5	
(V_{DS} = -15 Vdc, I_D = 10 µAdc)	2N5473		0.9	4.5	
(V_{DS} = -15 Vdc, I_D = 20 µAdc)	2N5474		1.2	6.0	
(V_{DS} = -15 Vdc, I_D = 40 µAdc)	2N5475		1.5	7.5	
(V_{DS} = -15 Vdc, I_D = 80 µAdc)	2N5476		2.0	8.0	
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance (1)		$\|y_{fs}\|$			µmhos
(V_{DS} = -15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5471		60	180	
	2N5472		90	225	
	2N5473		120	300	
	2N5474		160	400	
	2N5475		200	500	
	2N5476		260	650	
Output Admittance (1)		$\|y_{os}\|$			µmhos
(V_{DS} = -15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5471		–	1.0	
	2N5472		–	1.0	
	2N5473		–	2.5	
	2N5474		–	2.5	
	2N5475		–	5.0	
	2N5476		–	10	
Input Capacitance (V_{DS} = -15 Vdc, V_{GS} = 0, 140 kHz ≤ f ≤ 1.0 MHz)		C_{iss}	–	5.0	pF
Reverse Transfer Capacitance (V_{DS} = -15 Vdc, V_{GS} = 0, 140 kHz ≤ f ≤ 1.0 MHz)		C_{rss}	–	1.0	pF
Common-Source Noise Figure (V_{DS} = -15 Vdc, V_{GS} = 0, R_S = 1.0 Megohm, f = 1.0 kHz, BW = 1.0 Hz)		NF	–	2.5	dB
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = -15 Vdc, V_{GS} = 0, f = 1.0 kHz, BW = 1.0 Hz)		e_n	–	110	$nV/\sqrt{Hz}$

(1) Pulse Test: Pulse Width ≤630 ms, Duty Cycle ≤2.0%.

*Indicates JEDEC Registered Data.

TYPICAL SMALL-SIGNAL CHARACTERISTICS

($T_{channel} = 25^{\circ}C$)

FIGURE 1 – FORWARD TRANSFER ADMITTANCE

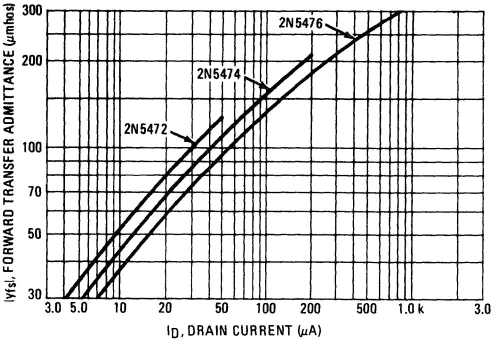
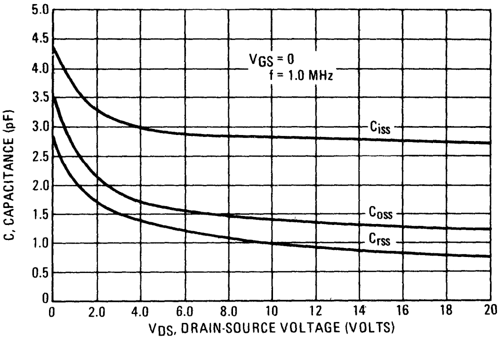


FIGURE 2 – CAPACITANCE



TYPICAL NOISE FIGURE

FIGURE 3 – EFFECTS OF FREQUENCY

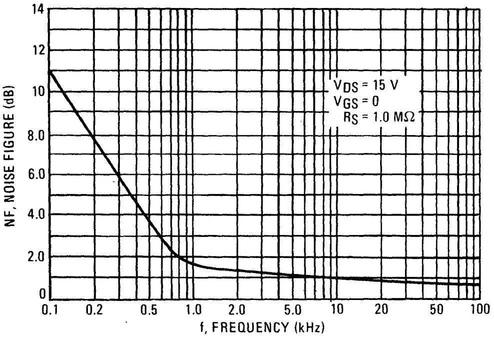


FIGURE 4 – EFFECTS OF SOURCE RESISTANCE

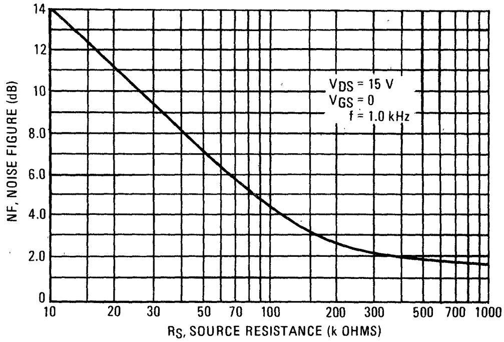
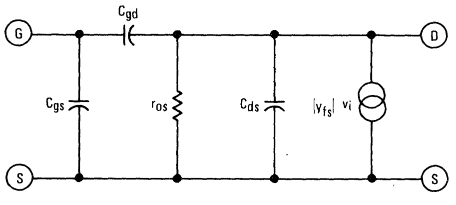


FIGURE 5 – LOW FREQUENCY CIRCUIT MODEL



$y_{is} = j\omega C_{iss}$
$y_{os} = 1/r_{oss} + j\omega C_{oss}$
$y_{fs} = |y_{fs}|$
$y_{rs} = -j\omega C_{rss}$

$C_{iss} = C_{gd} + C_{gs}$
$C_{rss} = C_{gd}$
$C_{oss} = C_{gd} + C_{ds}$

TYPICAL LIMIT TRANSFER CHARACTERISTICS

(TEMPERATURES NOTED ARE $T_{channel}$)

FIGURE 6 – 2N5471

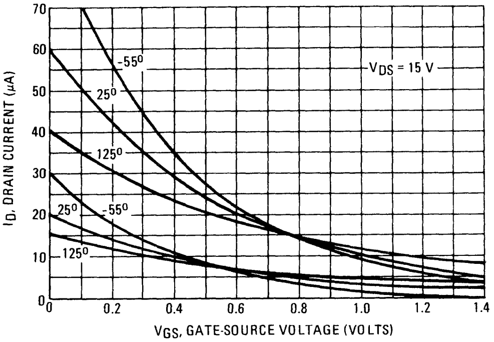


FIGURE 7 – 2N5472

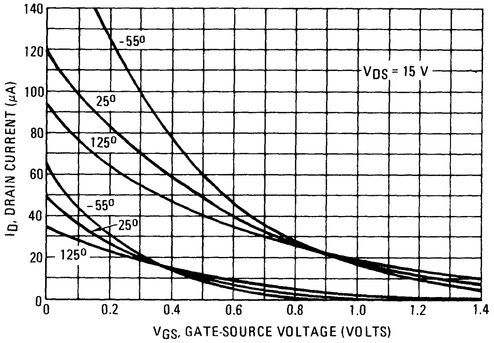


FIGURE 8 – 2N5473

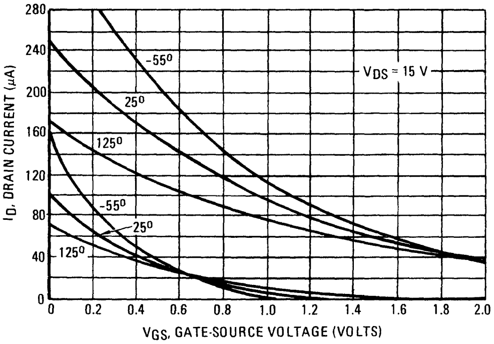


FIGURE 9 – 2N5474

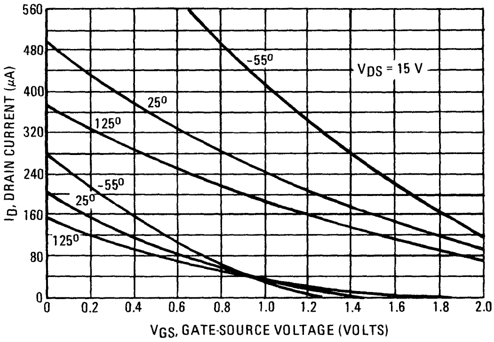


FIGURE 10 – 2N5475

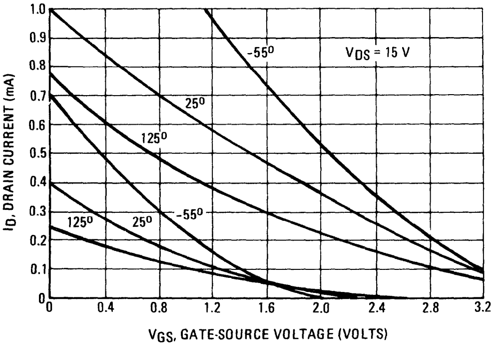
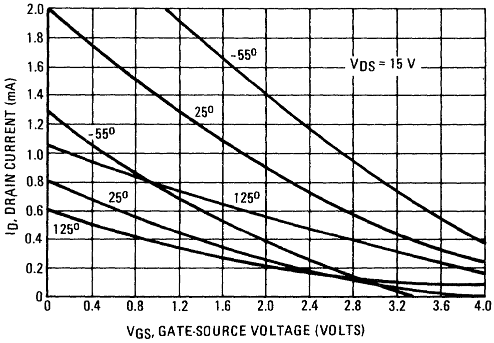


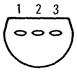
FIGURE 11 – 2N5476



2N5484 (SILICON)
thru
2N5486

N-channel depletion mode (Type A) junction field-effect transistors designed for VHF/UHF amplifier applications.

CASE 29
(TO-92)



STYLE 5
PIN 1. DRAIN
2 SOURCE
3. GATE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	25	Vdc
Drain Current	I_D	30	mAdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_C = 25° C Derate above 25° C	P_D (1)	310 2.82	mW mW/° C
Operating and Storage Junction Temperature Range	T_J, T_{stg} (1)	-65 to +150	° C

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125° C/W.

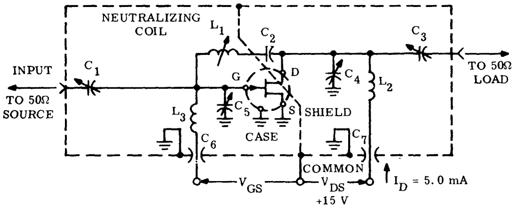
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	25	-	-	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5484	$V_{GS(off)}$	0.3	-	3.0	Vdc
	2N5485		0.5	-	4.0	
	2N5486		2.0	-	6.0	
Gate Reverse Current (V_{GS} = -20 Vdc, V_{DS} = 0)		I_{GSS}	-	-	1.0	nAdc
(V_{GS} = -20 Vdc, V_{DS} = 0, T_A = 100° C)			-	-	0.2	μAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5484	I_{DSS}	1.0	-	5.0	mAdc
	2N5485		4.0	-	10	
	2N5486		8.0	-	20	

ELECTRICAL CHARACTERISTICS (continued)

Characteristic		Symbol	Min	Typ	Max	Unit
SMALL-SIGNAL CHARACTERISTICS						
Forward Transadmittance		$\lvert y_{fs} \rvert$				µmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5484		3000	-	6000	
	2N5485		3500	-	7000	
	2N5486		4000	-	8000	
Forward Transconductance		$Re(y_{fs})$				µmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484		2500	-	-	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485		3000	-	-	
	2N5486		3500	-	-	
Output Admittance		$\lvert y_{os} \rvert$				µmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5484		-	-	50	
	2N5485		-	-	60	
	2N5486		-	-	75	
Output Conductance		$Re(y_{os})$				µmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484		-	-	75	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485, 2N5486		-	-	100	
Input Conductance		$Re(y_{is})$				µmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484		-	-	100	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485, 2N5486		-	-	1000	
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	-	-	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	-	-	1.0	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	-	-	2.0	pF
Common-Source Noise Figure		NF				dB
(V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 1.0 kHz)	All Types		-	-	2.5	
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, $R_G \approx$ 1.0 k ohm, f = 100 MHz)	2N5484		-	-	3.0	
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, $R_G \approx$ 1.0 k ohm, f = 200 MHz)	2N5484		-	4.0	-	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, $R_G \approx$ 1.0 k ohm, f = 100 MHz)	2N5485, 2N5486		-	-	2.0	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, $R_G \approx$ 1.0 k ohm, f = 400 MHz)	2N5485, 2N5486		-	-	4.0	
Insertion Power Gain		G_{ps}				dB
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, f = 100 MHz)	2N5484		16	-	25	
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, f = 200 MHz)	2N5484		-	14	-	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, f = 100 MHz)	2N5485, 2N5486		18	-	30	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, f = 400 MHz)	2N5485, 2N5486		10	-	20	

FIGURE 1 – 100 MHz AND 400 MHz NEUTRALIZED AMPLIFIER



ADJUST V_{GS} FOR
I_D = 5.0 mA
V_{GS} < 0 VOLTS

NOTE:

The noise source is a hot-cold body (AIL type 70 or equivalent) with a test receiver (AIL type 136 or equivalent).

Reference Designation	VALUE 100 MHz	VALUE 400 MHz
C_1	1-12 pF	0.8-8.0 pF
C_2	1000 pF	27 pF
C_3	1-12 pF	0.8-8.0 pF
C_4	1-12 pF	0.8-8.0 pF
C_5	1-12 pF	0.8-8.0 pF
C_6	0.0015 µF	0.001 µF
C_7	0.0015 µF	0.001 µF
L_1	3.0 µH*	0.2 µH**
L_2	0.25 µH*	0.03 µH**
L_3	0.14 µH*	0.022 µH**

* L_1 17 turns (approximately - depending upon circuit layout), AWG #28 enameled copper wire, close wound on 9/32" ceramic coil form. Tuning provided by a powdered iron slug.

L_2 4 1/2 turns, AWG #18 enameled copper wire, 5/16" long, 3/8" I. D. (AIR CORE).

L_3 3 1/2 turns, AWG #18 enameled copper wire, 1/4" long, 3/8" I. D. (AIR CORE).

** L_1 6 turns (approximately - depending upon circuit layout), AWG #24 enameled copper wire, close wound on 7/32" ceramic coil form. Tuning provided by an aluminum slug.

L_2 1 turn, AWG #16 enameled copper wire, 3/8" I. D. (AIR CORE).

L_3 1/2 turn, AWG #16 enameled copper wire, 1/4" I. D. (AIR CORE).

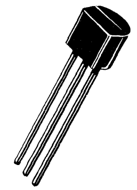
2N5550 (SILICON)
2N5551

NPN SILICON ANNULAR TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier applications.

- High Voltage Ratings –
  BV_{CEO} = 140 and 160 Vdc (Min)
- Low Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$ = 0.25 Vdc (Max) @ I_C = 50 mA – 2N5550
  = 0.20 Vdc (Max) @ I_C = 50 mA – 2N5551
- Current Gain Specified from 1.0 mAdc to 50 mAdc
- Excellent for Nixie® Driver Applications

HIGH VOLTAGE
NPN SILICON
AMPLIFIER TRANSISTORS



*MAXIMUM RATINGS

Rating	Symbol	2N5550	2N5551	Unit
Collector-Emitter Voltage	V_{CEO}	140	160	Vdc
Collector-Base Voltage	V_{CB}	160	180	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous	I_C	600		mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	350 2.8		mW mW/^oC
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	1.0 8.0		Watt mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	357	$^oC/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	$^oC/W$

*Indicates JEDEC Registered Data

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

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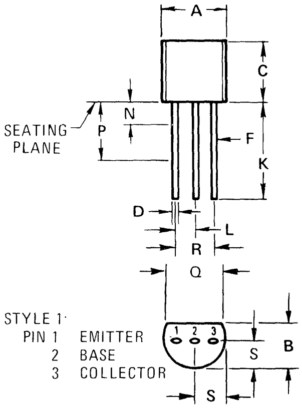


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

* **ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	2N5550		140	–	
	2N5551		160	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	2N5550		160	–	
	2N5551		180	–	
Emitter-Base Breakdown Voltage		BV_{EBO}			Vdc
(I_E = 10 μAdc, I_C = 0)			6.0	–	
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 100 Vdc, I_E = 0)	2N5550		–	100	
(V_{CB} = 120 Vdc, I_E = 0)	2N5551		–	50	
(V_{CB} = 100 Vdc, I_E = 0, T_A = 100°C)	2N5550		–	100	μAdc
(V_{CB} = 120 Vdc, I_E = 0, T_A = 100°C)	2N5551		–	50	
Emitter Cutoff Current		I_{EBO}			nAdc
(V_{EB} = 4.0 Vdc, I_C = 0)			–	50	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	2N5550		60	–	
	2N5551		80	–	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	2N5550		60	250	
	2N5551		80	250	
(I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	2N5550		20	–	
	2N5551		30	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)	Both Types		–	0.15	
(I_C = 50 mAdc, I_B = 5.0 mAdc)	2N5550		–	0.25	
	2N5551		–	0.20	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)	Both Types		–	1.0	
(I_C = 50 mAdc, I_B = 5.0 mAdc)	2N5550		–	1.2	
	2N5551		–	1.0	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)			100	300	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)			–	6.0	
Input Capacitance		C_{ib}			pF
(V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	2N5550		–	30	
	2N5551		–	20	
Small-Signal Current Gain		h_{fe}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)			50	200	
Noise Figure		NF			dB
(I_C = 250 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k ohm,	2N5550		–	10	
f = 10 Hz to 15.7 kHz)	2N5551		–	8.0	

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%

FIGURE 1 — DC CURRENT GAIN

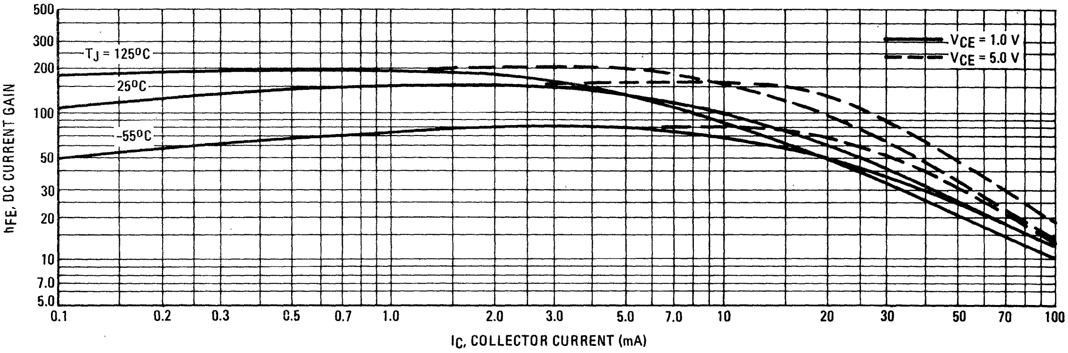


FIGURE 2 — COLLECTOR SATURATION REGION

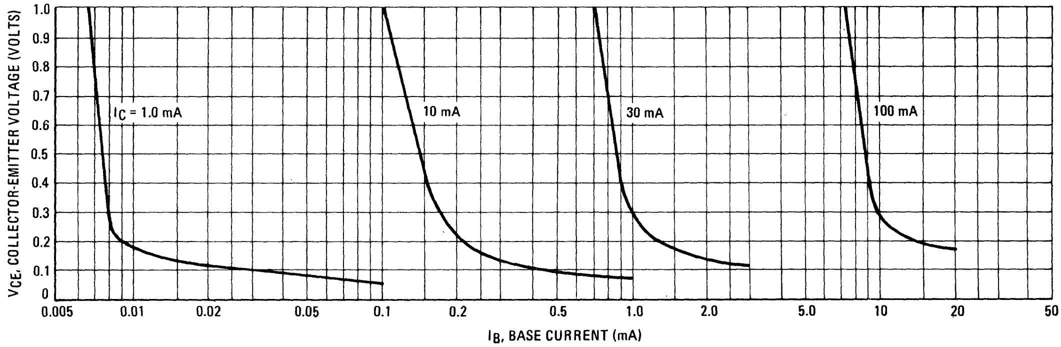


FIGURE 3 — COLLECTOR CUT-OFF REGION

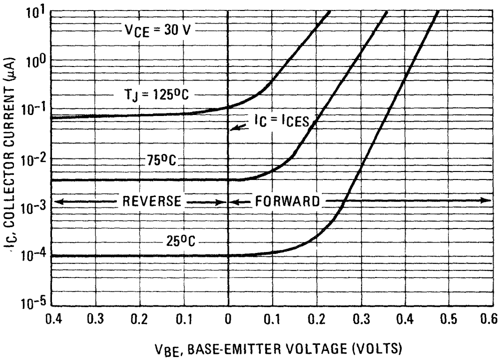


FIGURE 4 – "ON" VOLTAGES

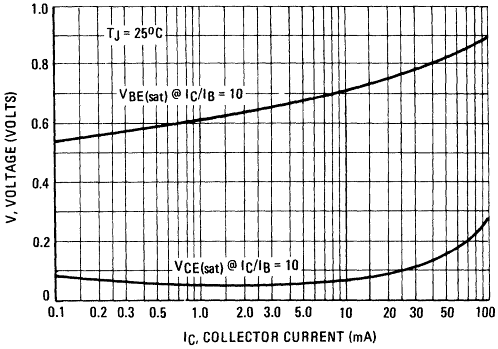


FIGURE 5 – TEMPERATURE COEFFICIENTS

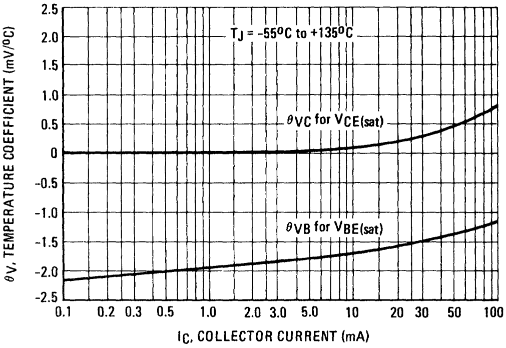


FIGURE 6 – SWITCHING TIME TEST CIRCUIT

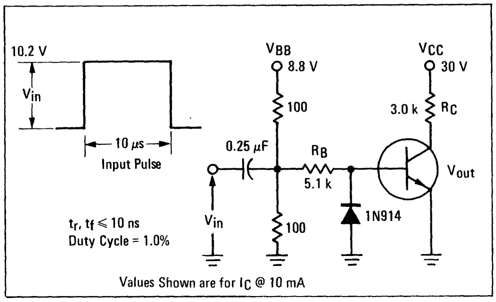


FIGURE 7 – CAPACITANCES

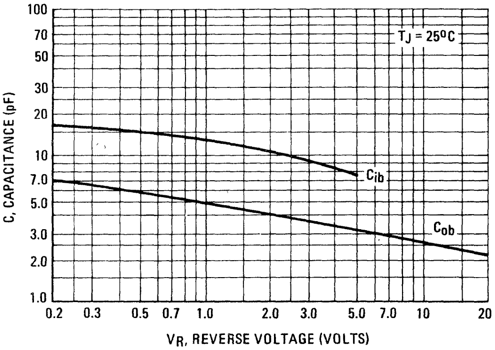


FIGURE 8 – TURN-ON TIME

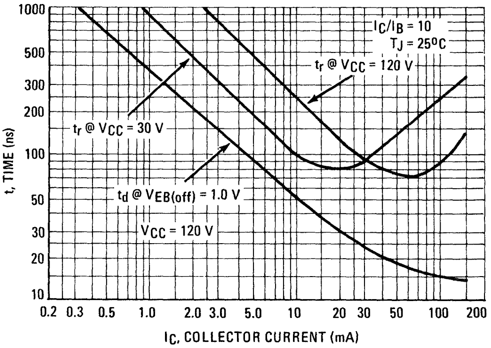
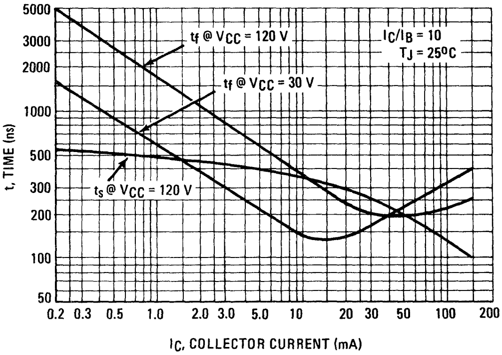


FIGURE 9 – TURN-OFF TIME



2N5555 (SILICON)

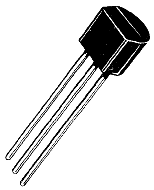
SILICON N-CHANNEL
JUNCTION FIELD-EFFECT TRANSISTOR

Depletion Mode (Type A) Junction Field-Effect Transistor designed for high-speed switching applications.

- Low Drain-Source "On" Resistance — $r_{ds(on)}$ = 150 Ohms (Max)
- Low Reverse Transfer Capacitance — C_{rss} = 1.2 pF (Max) @ f = 1.0 MHz
- Fast Turn-On Time — $t_{(on)}$ = 10 ns (Max)

N-CHANNEL
JUNCTION FIELD-EFFECT
TRANSISTOR

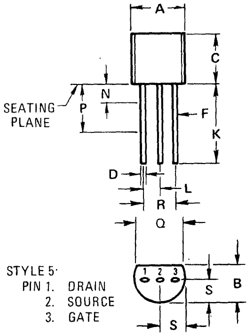
TYPE A



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Gate-Source Voltage	V_{GS}	25	Vdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @T_C = 25°C Derate above 25°C	$P_{(1)}$	310 2.82	mW mW/°C
Operating Junction Temperature Range	$T_{(1)}$	-65 to +175	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125°C/W.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

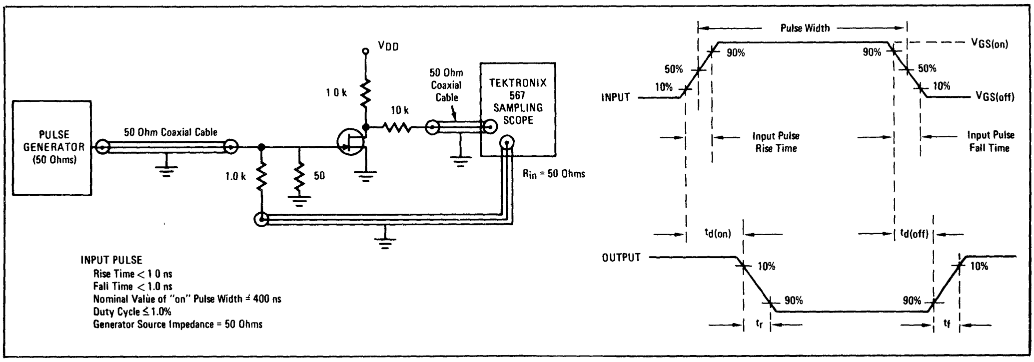
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	25	-	Vdc
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0)	I_{GSS}	-	1.0	nAdc
Drain Cutoff Current (V_{DS} = 12 Vdc, V_{GS} = 10 Vdc)	$I_{D(off)}$	-	10	nAdc
(V_{DS} = 12 Vdc, V_{GS} = 10 Vdc, T_A = 100°C)		-	2.0	μAdc
ON CHARACTERISTICS				
Zero-Gate Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	15	-	mAdc
Gate-Source Forward Voltage ($I_{G(f)}$ = 1.0 mAdc, V_{DS} = 0)	$V_{GS(f)}$	-	1.0	Vdc
Drain-Source "ON" Voltage (I_D = 7.0 mAdc, V_{GS} = 0)	$V_{DS(on)}$	-	1.5	Vdc
Static Drain-Source "ON" Resistance (I_D = 0.1 mAdc, V_{GS} = 0)	$r_{DS(on)}$	-	150	Ohms
SMALL-SIGNAL CHARACTERISTICS				
Small-Signal Drain-Source "ON" Resistance (V_{GS} = 0, I_D = 0, f = 1.0 kHz)	$r_{ds(on)}$	-	150	Ohms
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	-	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 10 Vdc, f = 1.0 MHz)	C_{rss}	-	1.2	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 10 Vdc, $I_{D(on)}$ = 7.0 mAdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -10 Vdc) (See Figure 1)	$t_{d(on)}$	-	5.0	ns
Rise Time		t_r	-	5.0	ns
Turn-Off Delay Time	(V_{DD} = 10 Vdc, $I_{D(on)}$ = 7.0 mAdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -10 Vdc) (See Figure 1)	$t_{d(off)}$	-	15	ns
Fall Time		t_f	-	10	ns

(1) Pulse Test: Pulse Width < 300 μs, Duty Cycle < 3.0%.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
Rise Time < 1.0 ns
Fall Time < 1.0 ns
Nominal Value of "on" Pulse Width ≈ 400 ns
Duty Cycle ≤ 1.0%
Generator Source Impedance = 50 Ohms

2N5556 (SILICON)
thru
2N5558

SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

Depletion Mode (Type A) devices designed for low-noise amplifier applications.

- Low Noise Figure – NF = 1.0 dB (Max) @ 100 Hz
- Low Gate Leakage Current – I_{GSS} = 0.1 nAdc (Max)
- Low Input Capacitance – C_{iss} = 6.0 pF (Max)

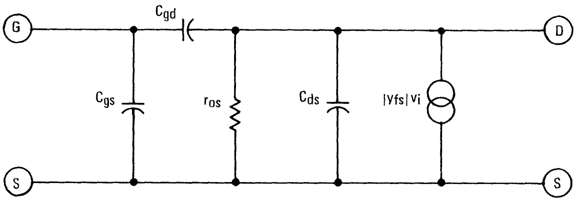
SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

TYPE A

MAXIMUM RATINGS

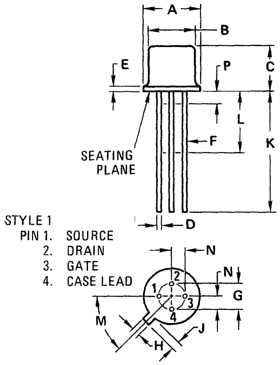
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 2.0	mW mW/°C
Operating Junction Temperature Range	T_J	-65 to +175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

FIGURE 1 – EQUIVALENT LOW FREQUENCY CIRCUIT



$y_{is} = j\omega C_{iss}$
$y_{os} = 1/r_{oss} + j\omega C_{oss}$
$y_{fs} = |y_{fs}|$
$y_{rs} = -j\omega C_{rss}$

$C_{iss} = C_{gd} + C_{gs}$
$C_{rss} = C_{gd}$
$C_{oss} = C_{gd} + C_{ds}$



STYLE 1
PIN 1. SOURCE
2. DRAIN
3. GATE
4. CASE LEAD

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

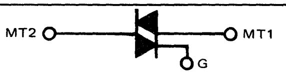
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	-	-	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 nAdc)	2N5556	$V_{GS(off)}$	0.2	-	4.0	Vdc
	2N5557		0.8	-	5.0	
	2N5558		1.5	-	6.0	
Gate Reverse Current (V_{GS} = -15 Vdc, V_{DS} = 0)		I_{GSS}	-	-	-0.1	nAdc
(V_{GS} = -15 Vdc, V_{DS} = 0, T_A = 150°C)			-	-	-100	
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5556	I_{DSS}	0.5	-	2.5	mAdc
	2N5557		2.0	-	5.0	
	2N5558		4.0		10	
DYNAMIC CHARACTERISTICS						
Forward Transadmittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\|y_{fs}\|$	1500	3500	6500	μmhos
Output Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\|y_{os}\|$	-	-	20	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	-	4.5	6.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	-	1.2	3.0	pF
Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_S = 500 k ohms, f = 10 Hz, BW = 1.0 Hz)		NF	-	-	1.0	dB
(V_{DS} = 15 Vdc, V_{GS} = 0, R_S = 100 k ohms, f = 100 Hz, BW = 1.0 Hz)			-	-	1.0	
Equivalent Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 10 Hz, BW = 1.0 Hz)		e_n	-	20	35	nV/√Hz
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)			-	10	20	

(1) Pulse Test: Pulse Width = 630 ms, Duty Cycle = 10%.

2N5571 thru 2N5574 (SILICON)
2N6145 thru 2N6147
MAC40797, MAC40798

**TRIACS
(THYRISTORS)**

**15 AMPERES RMS
200-600 VOLTS**



SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 4 Quadrants

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage (1) (T_J = -65 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM} and V_{RRM}		Volts
2N5571, 2N5573, 2N6145		200	
2N5572, 2N5574, 2N6146		400	
MAC40797, MAC40798, 2N6147		600	
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS	$I_{T(RMS)}$		Amp
(T_C = -65 to +80°C)		15	
(T_C = +85°C)		10	
*Peak Surge Current (One Full cycle of surge current at 60 Hz, preceeded and followed by 15 A current, T_C = +80°C)	I_{TSM}	100	Amp
Circuit Fusing Considerations (T_C = -65 to +80°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (2) (T_C = +80°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, Pulse Width = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-65 to +100	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Stud Torque 2N5573, 2N5574 2N6145, 2N6146, 2N6147	—	30	in.lb.

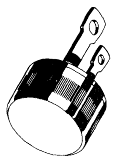
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

*Indicates JEDEC Registered Data.

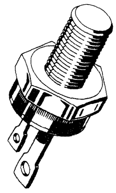
(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

(2) 2N5571 thru 2N5574, P_{GM} Rating = 16 Watts.



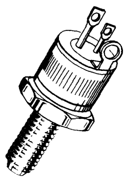
**2N5571
2N5572
MAC40797**

CASE 174
TO-203



**2N5573
2N5574
MAC40798**

CASE 175



**2N6145
2N6146
2N6147**

CASE 235

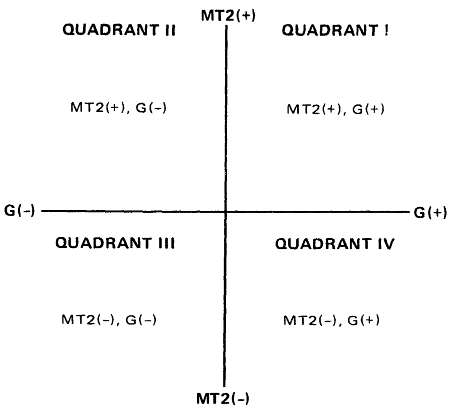
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_C = 100°C	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 21 A Peak, Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤2.0%	V_{TM}	–	1.3	1.8	Volts
Gate Trigger Current, Continuous dc (1) Main Terminal Voltage = 12 Vdc, R_L = 30 ohms	I_{GT}				mA
MT2 (+), G(+); MT2(-), G(-)		–	–	50	
MT2 (+), G(-); MT2(-), G(+)		–	–	80	
*MT2 (+), G(+); MT2(-), G(-) T_C = -65°C		–	–	150	
*MT2 (+), G(-); MT2(-), G(+) T_C = -65°C		–	–	200	
Gate Trigger Voltage, Continuous dc (All Quadrants) Main Terminal Voltage = 12 Vdc, R_L = 30 ohms	V_{GT}				Volts
T_C = 25°C		–	–	2.5	
*T_C = -65°C		–	–	4.0	
*Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_C = +100°C		0.2	–	–	
Holding Current Main Terminal Voltage = 12 Vdc, Gate Open Initiating Current = 500 mA	I_H				mA
T_C = 25°C		–	–	75	
*T_C = -65°C		–	–	300	
*Turn-On Time Rated V_{DRM}, I_{TM} = 21 A Peak, I_{GT} = 160 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	t_{gt}	–	1.0	2.0	μs
*Critical Rate-of-Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 21 A Peak, Commutating di/dt = 8 A/ms, gate unenergized	dv/dt				V/μs
T_C = 80°C 2N5571 thru 2N5574, MAC40797, MAC40798		2.0	10	–	
T_C = 75°C 2N6145 thru 2N6147		2.0	10	–	
*Critical Rate-of-Rise of Off-State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C:	dv/dt				V/μs
2N5571, 2N5573, 2N6145		30	150	–	
2N5572, 2N5574, 2N6146		20	100	–	
MAC40797, MAC40798, 2N6147		10	75	–	

*Indicates JEDEC Registered Data.

(1)All Voltage polarity reference to main terminal 1.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 – 10 V	7.5 – 9.0 V	3.0 – 5.0 V
I_S	350 μA Max	120 μA Max	100 – 400 μA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient = 0.02%/°C Typ			

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

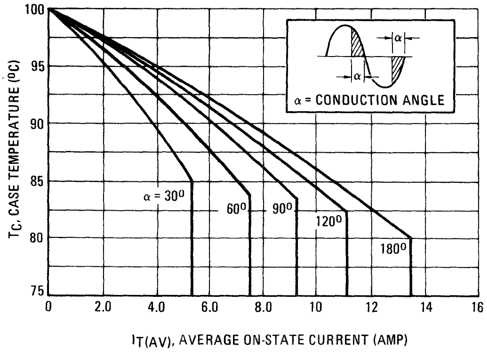


FIGURE 2 – RMS CURRENT DERATING

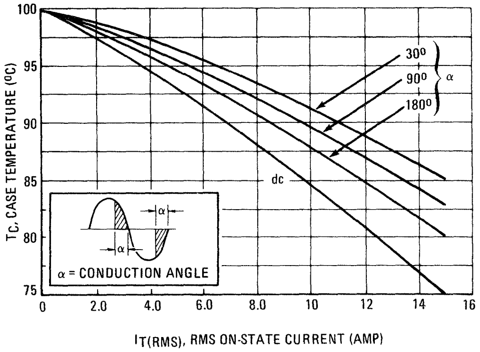


FIGURE 3 – ON-STATE POWER DISSIPATION

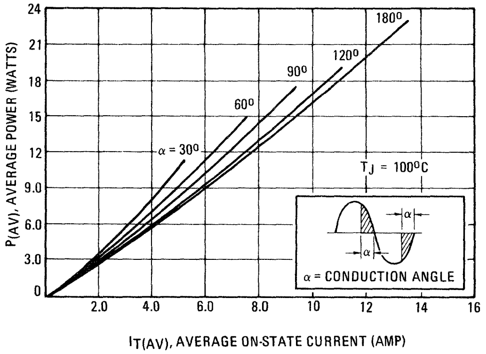


FIGURE 4 – ON-STATE POWER DISSIPATION

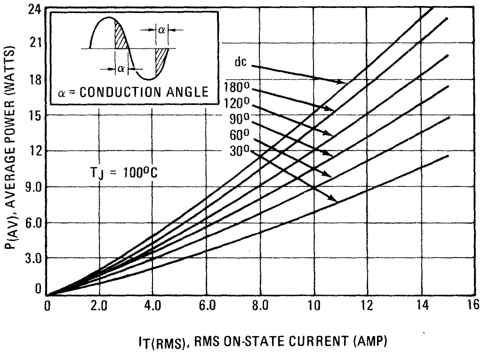


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

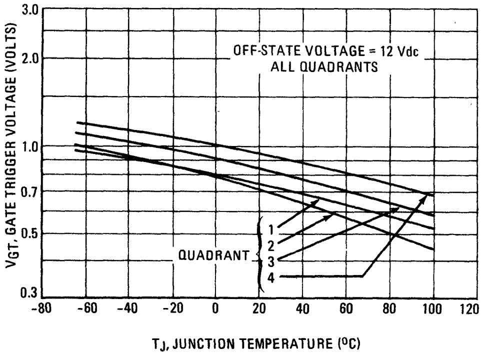


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

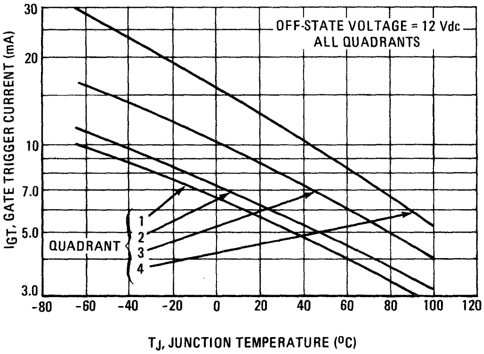


FIGURE 7 — MAXIMUM ON-STATE CHARACTERISTICS

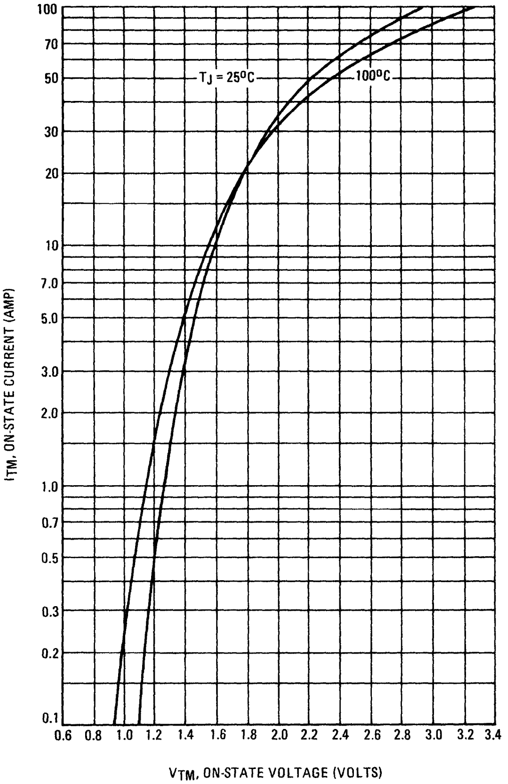


FIGURE 8 — TYPICAL HOLDING CURRENT

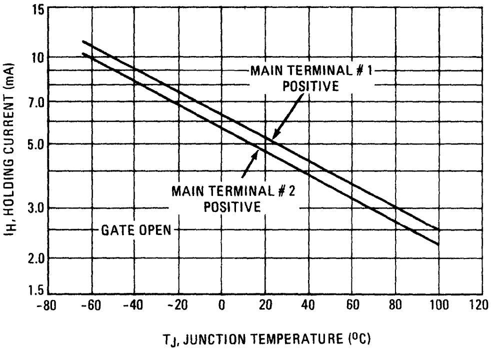


FIGURE 9 — MAXIMUM ALLOWABLE SURGE CURRENT

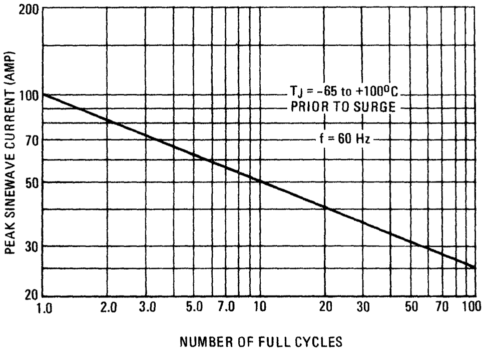
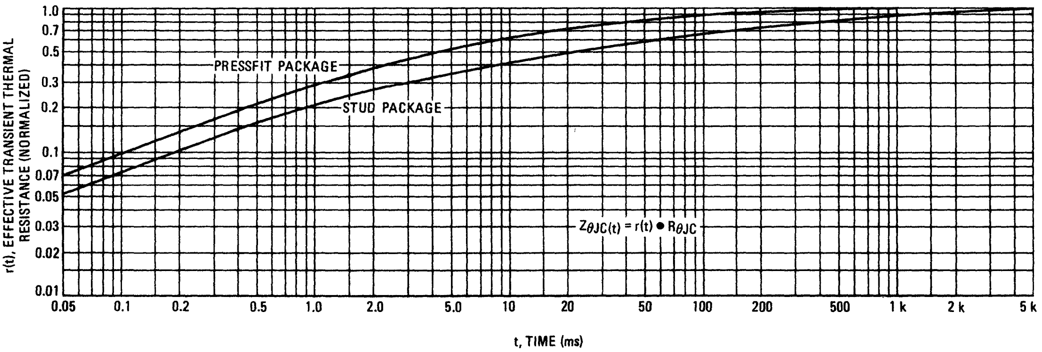
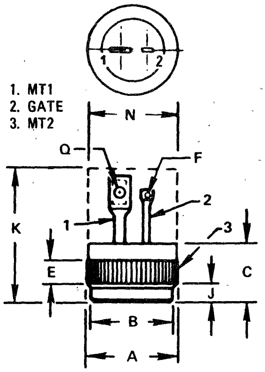


FIGURE 10 — TYPICAL THERMAL RESPONSE



TERM. 1. MT1
2. GATE
3. MT2



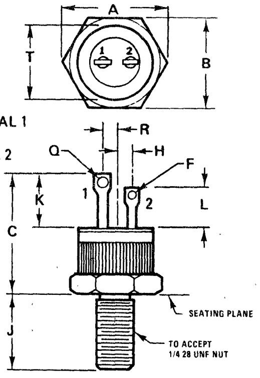
2N5571
2N5572
MAC40797

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.726	12.827	0.501	0.505
B	11.811	12.065	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	1.72	0.035	0.068
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.66	2.28	0.065	0.090

All JEDEC dimensions and notes apply

CASE 174-02
TO-203AA

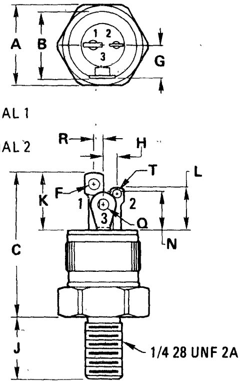
STYLE 3:
TERM. 1. MAIN TERMINAL 1
2. GATE
STUD: MAIN TERMINAL 2



2N5573
2N5574
MAC40798

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	1.40	1.65	0.055	0.065
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	2.03	2.41	0.080	0.095
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

CASE 175



STYLE 2:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2
STUD-ISOLATED

2N6145
2N6146
2N6147

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	2.03	2.41	0.080	0.095
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	1.40	1.65	0.055	0.065

CASE 235

2N 5581, 2N 5582 (SILICON)

For Specifications, See 2N2218S,AS Data, Volume I.

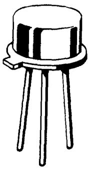
2N5583 (SILICON)

PNP SILICON ANNULAR TRANSISTOR

. . . designed for applications in high frequency amplifiers and non-saturated switching circuits. Large signal capabilities, low-noise and high gain-bandwidth product characteristics of the 2N5583 provide excellent performance in a variety of small signal and linear amplifier applications. Ideal for C A T V circuits.

- High Current-Gain—Bandwidth Product — f_T = 1300 (Min) @ I_C = 100 mAdc

PNP SILICON AMPLIFIER TRANSISTOR

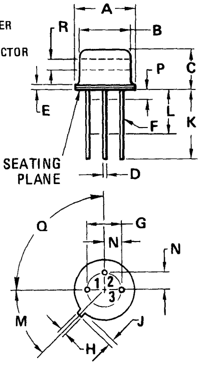


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	30	Vdc
*Collector-Base Voltage	V_{CB}	30	Vdc
*Emitter-Base Voltage	V_{EB}	3.0	Vdc
*Collector Current — Continuous	I_C	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 5.71	Watt mW/°C
*Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Figure No.	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	–	BV_{CEO}	30	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	–	BV_{CBO}	30	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	–	BV_{EBO}	3.0	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	4	I_{CBO}	–	50	nAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	–	I_{EBO}	–	0.5	μAdc
***ON CHARACTERISTICS** (1)					
DC Current Gain (I_C = 40 mAdc, V_{CE} = 2.0 Vdc) (I_C = 100 mAdc, V_{CE} = 2.0 Vdc) (I_C = 300 mAdc, V_{CE} = 5.0 Vdc)	1	h_{FE}	 20 25 15	 – 100 –	–
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	2,3	$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 2.0 Vdc)	3	$V_{BE(on)}$	–	1.8	Vdc
SMALL-SIGNAL CHARACTERISTICS					
*Current-Gain—Bandwidth Product (I_C = 40 mAdc, V_{CE} = 10 Vdc, f = 100 MHz) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	7	f_T	 1000 1300	 – –	MHz
*Collector-Base Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 100 kHz)	5	C_{cb}	–	5.0	pF
*Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	5	C_{eb}	–	35	pF

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

FIGURE 1 – DC CURRENT GAIN

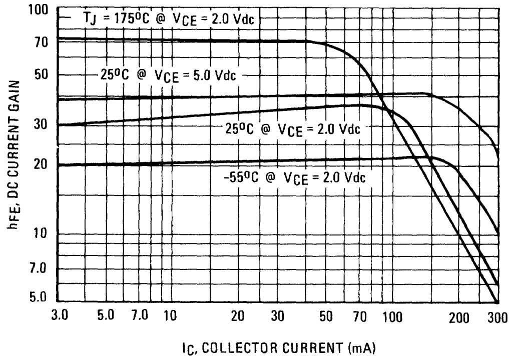


FIGURE 2 – COLLECTOR SATURATION REGION

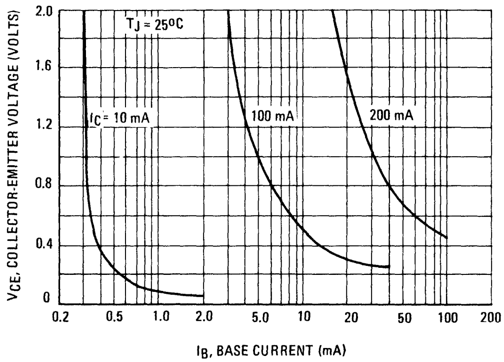


FIGURE 3 – "ON" VOLTAGES

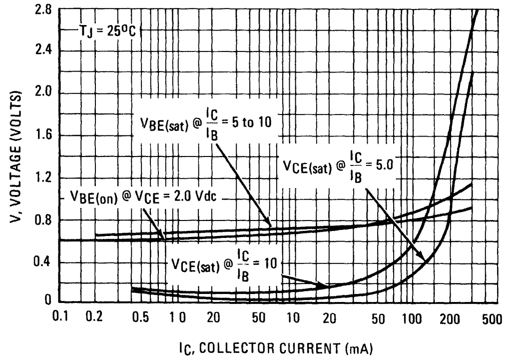


FIGURE 4 – COLLECTOR CURRENT versus BASE VOLTAGE

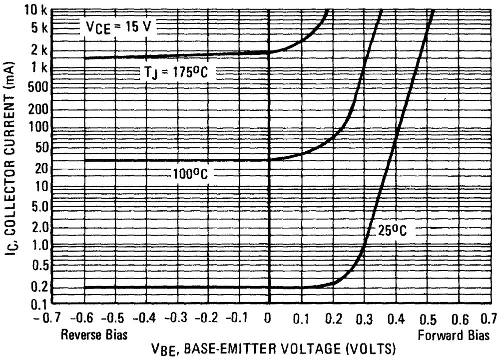


FIGURE 5 – CAPACITANCES

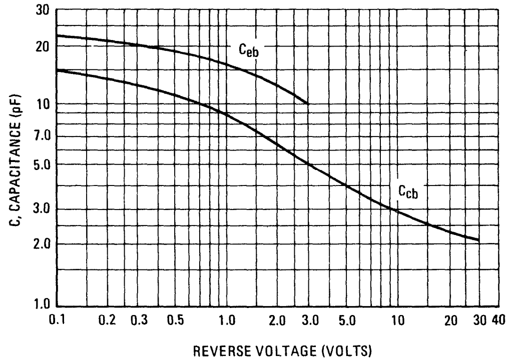


FIGURE 6 – TEMPERATURE COEFFICIENTS

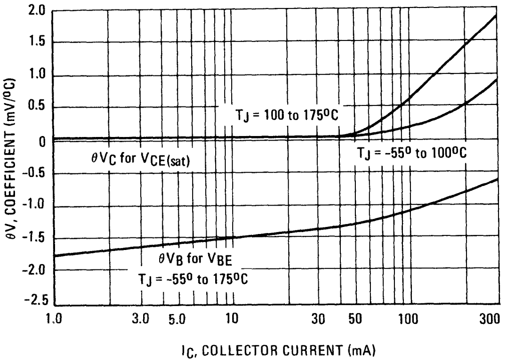


FIGURE 7 – CURRENT-GAIN–BANDWIDTH PRODUCT

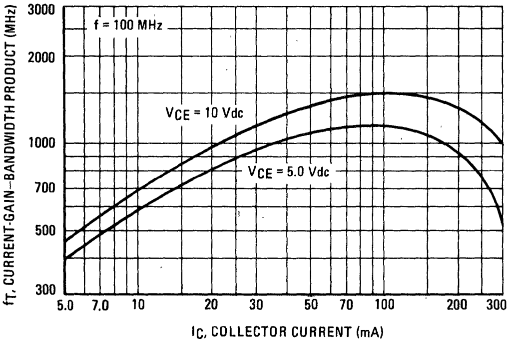


FIGURE 8 – COLLECTOR-BASE TIME CONSTANT

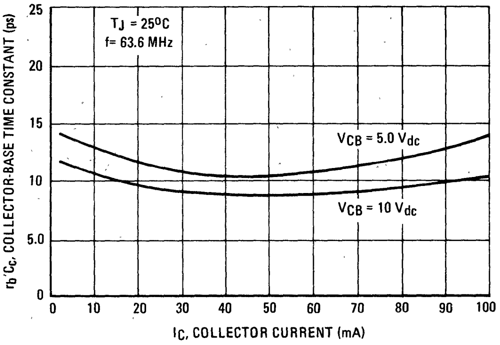


FIGURE 9 – SWITCHING TIME

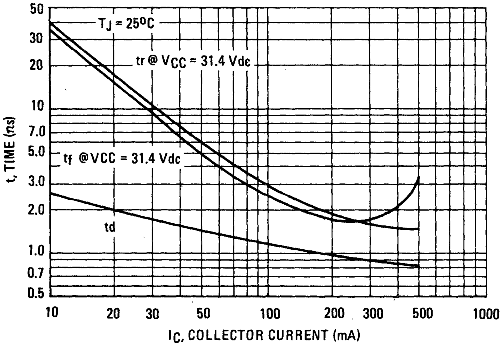
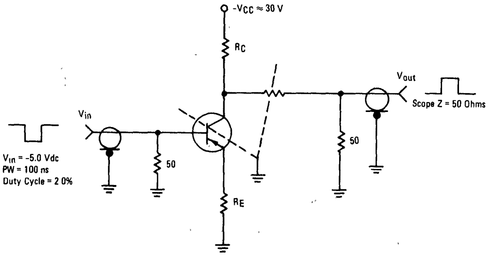


FIGURE 10 – SWITCHING TIME TEST CIRCUIT



I_C mA	R_C Ohms	R_E Ohms	V_{CC} Volts
50	526	80	34.4
150	160	26.6	31.4
300	78	13.3	30.6
500	46.5	8.0	30.3

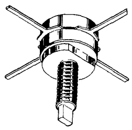
2N5589 (SILICON)

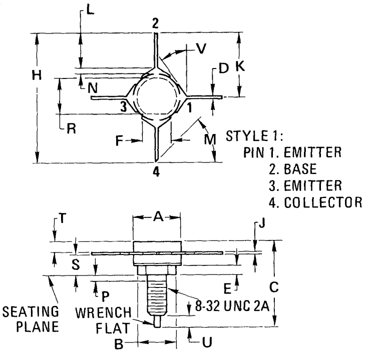
NPN SILICON RF POWER TRANSISTOR

. . . designed for 13.6 volt, VHF large signal power amplifier applications required in military and industrial equipment operating to 240 MHz.

- Low lead inductance stripline package for easier design and increased broadband capability.
- Balanced Emitter Construction for increased Safe Operating Area. The 2N5589 is designed to withstand an Open or Shorted Load at rated Output Power.
- Specified 13.6 Volt, 175 MHz Characteristics –
  Output Power = 3.0 Watts
  Minimum Gain = 8.2 dB
  Efficiency = 50%

NPN SILICON
RF POWER
TRANSISTOR





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.63	19.46	0.694	0.766
D	0.64	0.89	0.025	0.035
E	1.78	2.03	0.070	0.080
F	5.59	5.84	0.220	0.230
H	26.16	27.69	1.030	1.090
J	0.10	0.15	0.004	0.006
K	13.08	13.84	0.515	0.545
L	7.11	7.37	0.280	0.290
M	40°	50°	40°	50°
N	1.27	1.52	0.050	0.060
P		1.27		0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130
V	10°	20°	10°	20°

CASE 144B-03

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CB}	36	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	0.6	Adc
Total Device Dissipation @ $T_A = 25^{\circ}C$ Derate above 25°C	P_D	15 86	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

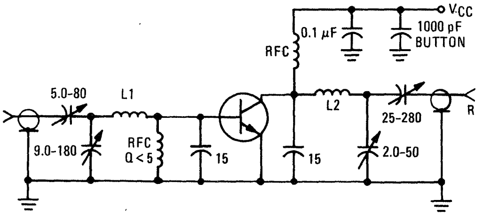
*Indicates JEDEC Registered Data.

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	BV_{CEO}	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 200 mAdc, V_{BE} = 0)	BV_{CES}	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{ob}	–	15	30	pF
FUNCTIONAL TEST					
Power Input (Figure 1) (P_{out} = 3.0 W, V_{CE} = 13.6 Vdc, f = 175 MHz)	P_{in}	–	0.35	0.45	Watt
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 3.0 W, V_{CE} = 13.6 Vdc, f = 175 MHz)	G_{PE}	8.2	–	–	dB
Collector Efficiency (Figure 1) (P_{out} = 3.0 W, V_{CE} = 13.6 Vdc, f = 175 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data.
Note 1: Pulsed through 25 mH inductor.

FIGURE 1 – 175 MHz TEST CIRCUIT



All capacitance values in pF unless otherwise indicated
L1 – 1-3/8" length of #14 AWG Wire
L2 – 2 Turns #16 AWG Wire, 1/4" Dia. 1-1/2" Long

POWER OUTPUT versus FREQUENCY

FIGURE 2

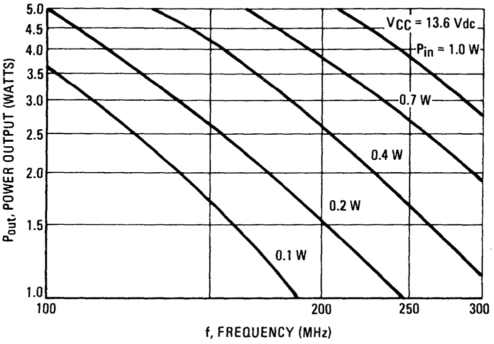


FIGURE 3

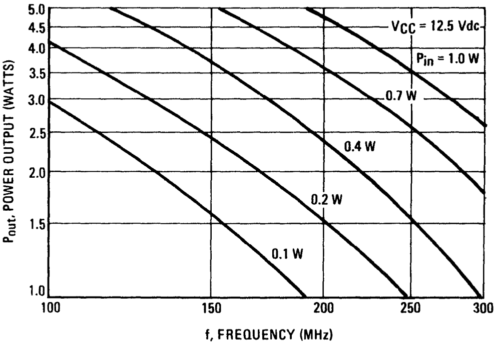


FIGURE 4 – POWER OUTPUT versus POWER INPUT

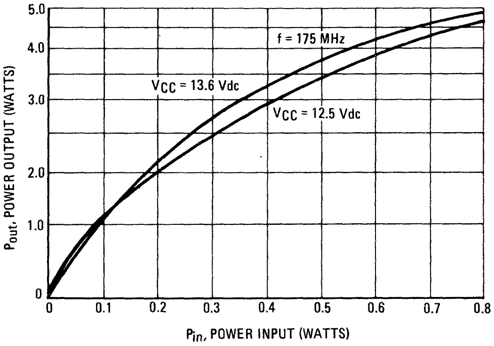
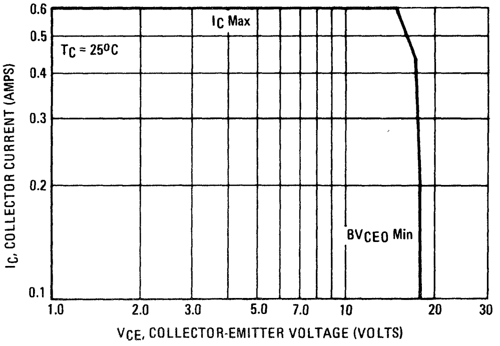


FIGURE 5 – DC SAFE OPERATING AREA



PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

FIGURE 6

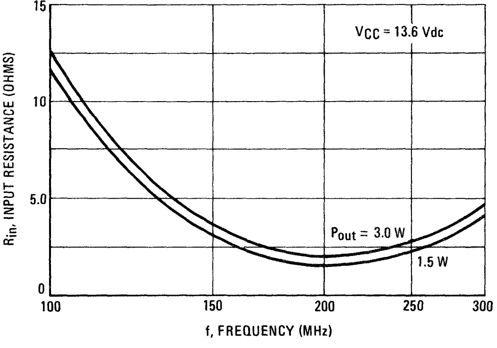
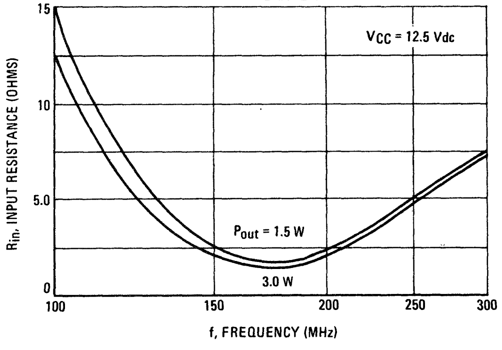


FIGURE 7



PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

FIGURE 8

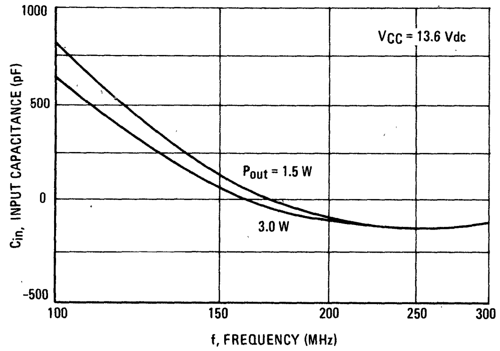
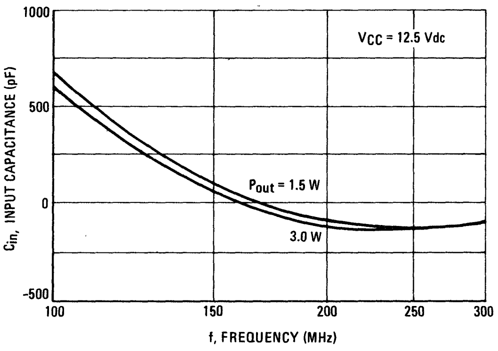


FIGURE 9



PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

FIGURE 10

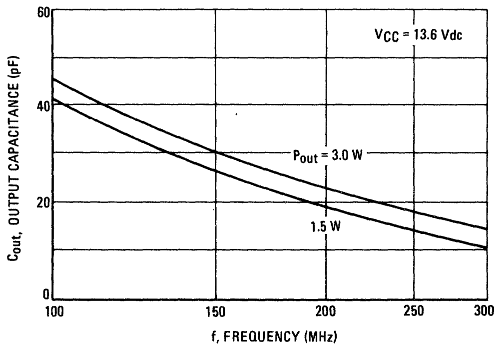
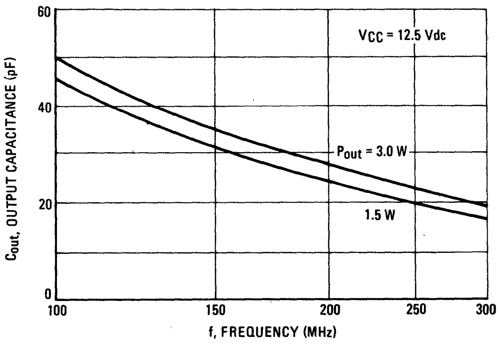


FIGURE 11



SERIES INPUT IMPEDANCE versus FREQUENCY

FIGURE 12

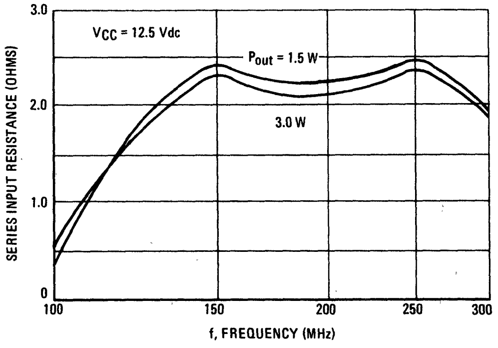
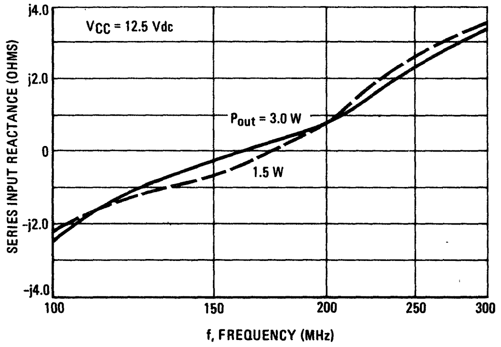


FIGURE 13



2N5590 (SILICON)

NPN SILICON RF POWER TRANSISTOR

. . . designed for 13.6 volt, VHF large signal power amplifier applications required in military and industrial equipment operating to 240 MHz.

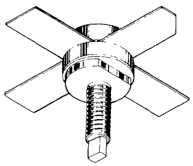
- Low lead inductance stripline package for easier design and increased broadband capability.
- Balanced Emitter Construction for increased Safe Operating Area. The 2N5590 is designed to withstand an Open or Shorted Load at rated Output Power.
- Specified 13.6 Volt, 175 MHz Characteristics –
  Output Power = 10 Watts
  Minimum Gain = 5.2 dB
  Efficiency = 50%

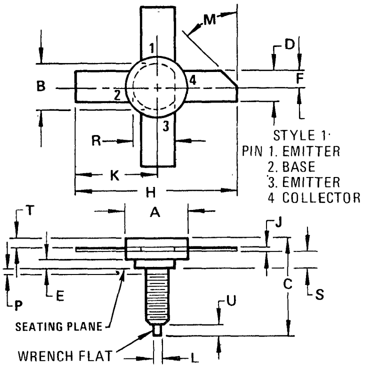
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CB}	36	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	2.0	Adc
Total Device Dissipation @ $T_A = 25^{\circ}C$ Derate above 25°C	P_D	30 171	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

NPN SILICON
RF POWER
TRANSISTOR





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	18.03	19.05	0.710	0.750
D	5.59	5.84	0.220	0.230
E	1.78	2.03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130

NOTE:
CASE 145A-01 USE 8-32NC2A STUD

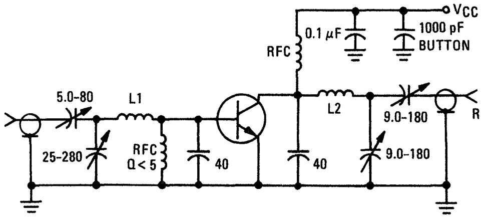
CASE 145A-01

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	18	–	–	Vdc
*Collector-Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, R_{BE} = 0)	$V_{CES(sus)}$	36	–	–	Vdc
*Emitter-Base Breakdown Voltage (I_E = 2.5 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
*DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
*Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{ob}	–	35	70	pF
FUNCTIONAL TEST					
*Power Input (Figure 1) (P_{out} = 10 W, V_{CE} = 13.6 Vdc, f = 175 MHz)	P_{in}	–	–	3.0	Watts
*Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 10 W, V_{CE} = 13.6 Vdc, f = 175 MHz)	G_{PE}	5.2	–	–	dB
Collector Efficiency (Figure 1) (P_{out} = 10 W, V_{CE} = 13.6 Vdc, f = 175 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data.
Note 1: Pulsed through 25 mH inductor.

FIGURE 1 — 175 MHz TEST CIRCUIT



All capacitance values in pF unless otherwise indicated
L1 – 1-3/8" length of #14 AWG Wire
L2 – 1 Turn #14 AWG Wire, 3/8" Dia. 1-1/2" Long

POWER OUTPUT versus FREQUENCY

FIGURE 2

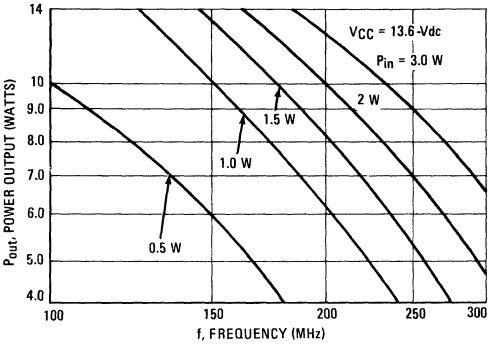


FIGURE 3

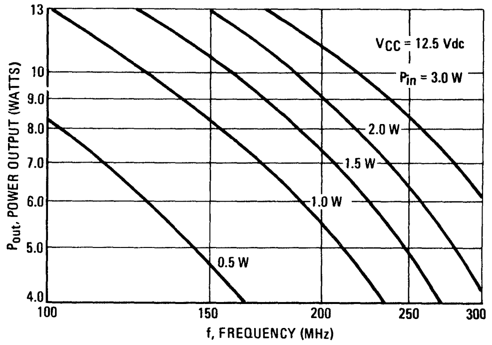


FIGURE 4 – POWER OUTPUT versus POWER INPUT

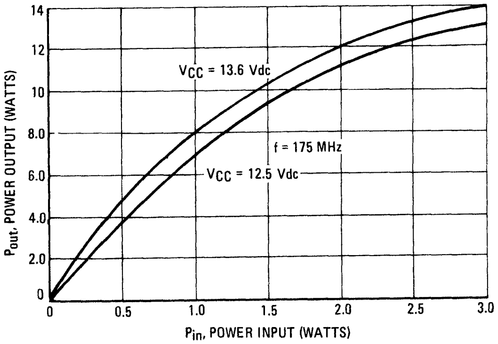
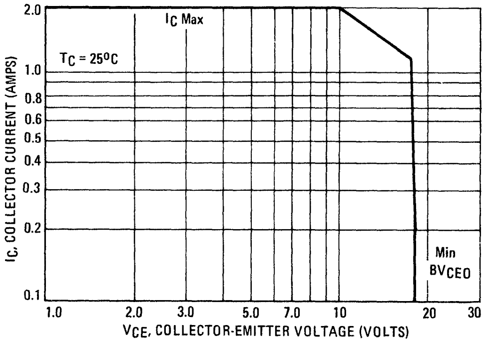


FIGURE 5 – DC SAFE OPERATING AREA



PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

FIGURE 6

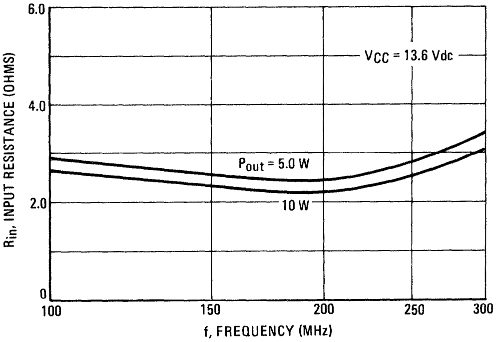
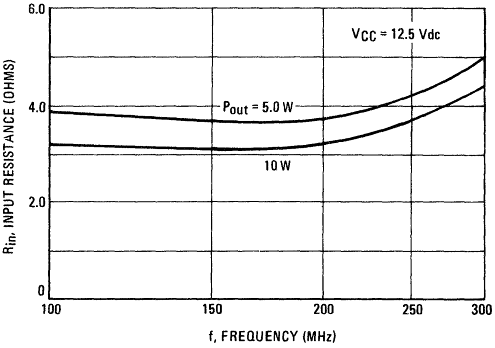


FIGURE 7



PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

FIGURE 8

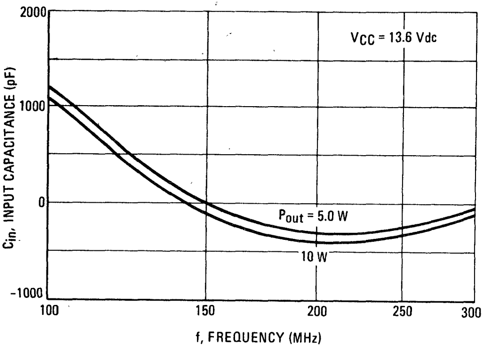
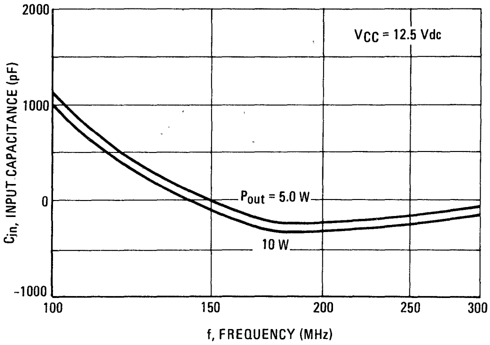


FIGURE 9



PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

FIGURE 10

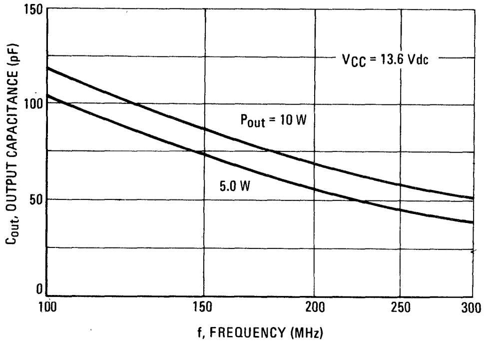
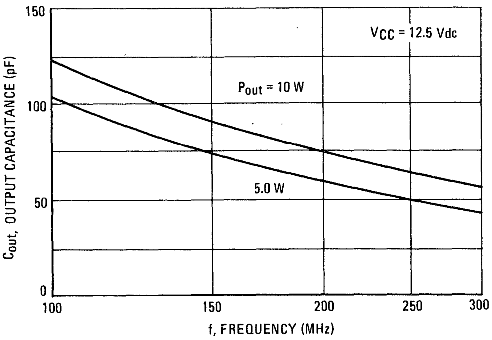


FIGURE 11



SERIES INPUT IMPEDANCE versus FREQUENCY

FIGURE 12

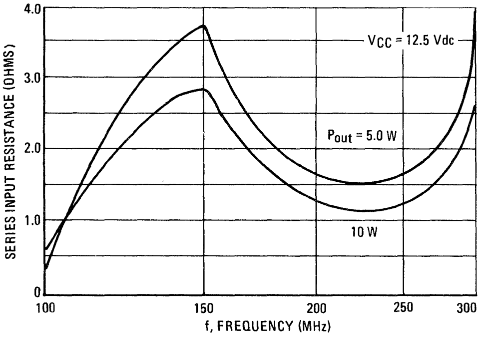
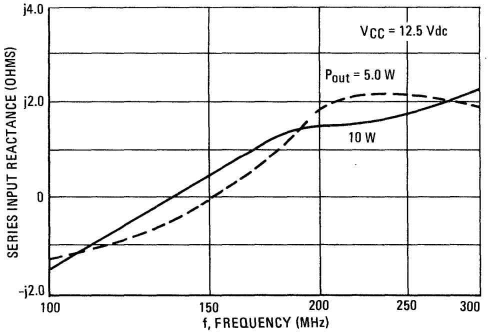


FIGURE 13



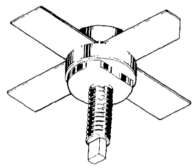
2N5591 (SILICON)

NPN SILICON RF POWER TRANSISTOR

. . . designed for 13.6 volt, VHF large signal power amplifier applications required in military and industrial equipment operating to 240 MHz.

- Low lead inductance stripline package for easier design and increased broadband capability.
- Balanced Emitter Construction for increased Safe Operating Area. The 2N5591 is designed to withstand an Open or Shorted Load at rated Output Power.
- Specified 13.6 Volt. 175 MHz Characteristics –
  Output Power = 25 Watts
  Minimum Gain = 4.4 dB
  Efficiency = 50%

**NPN SILICON
RF POWER
TRANSISTOR**

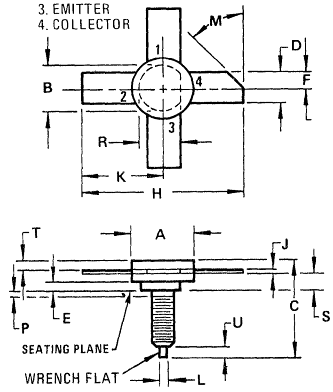


*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CB}	36	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	4.0	Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	70 400	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

STYLE 1.
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

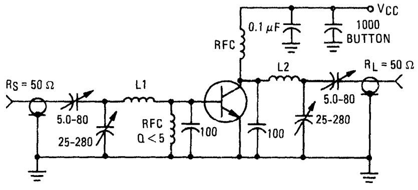


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	18.03	19.05	0.710	0.750
D	5.59	5.84	0.220	0.230
E	1.78	2.03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130

NOTE
CASE 145A-01 USE 8-32NC2A STUD

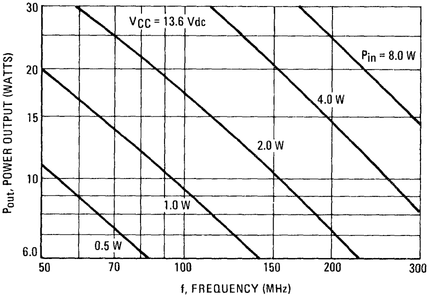
CASE 145A-01

FIGURE 1 – 175 MHz TEST CIRCUIT



ALL CAPACITORS IN pF UNLESS OTHERWISE INDICATED
L1 – #14 AWG STRAIGHT WIRE, 1–3/8″ LONG
L2 – 1 TURN #14 AWG WIRE, 3/8″ DIA. 1-1/2″ LONG

FIGURE 2 – POWER OUTPUT versus FREQUENCY



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	18	–	–	Vdc
*Collector-Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, V_{BE} = 0)	$V_{CES(sus)}$	36	–	–	Vdc
*Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
***DYNAMIC CHARACTERISTICS**					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{ob}	–	90	120	pF
***FUNCTIONAL TEST**					
Power Input (Figure 1) (P_{out} = 25 W, V_{CE} = 13.6 Vdc, f = 175 MHz)	P_{in}	–	–	9.0	Watts
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 25 W, V_{CE} = 13.6 Vdc, f = 175 MHz)	G_{PE}	4.4	–	–	dB
Collector Efficiency (Figure 1) (P_{out} = 25 W, V_{CE} = 13.6 Vdc, f = 175 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data.
Note 1: Pulsed through 25 mH inductor.

FIGURE 3 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

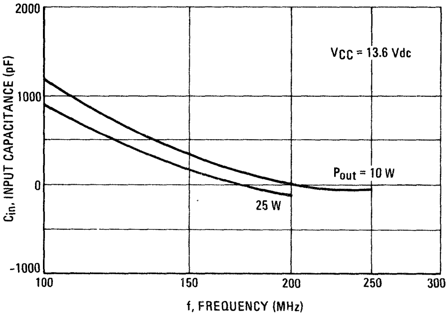


FIGURE 4 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

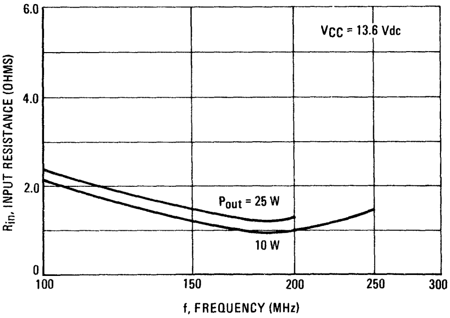


FIGURE 5 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

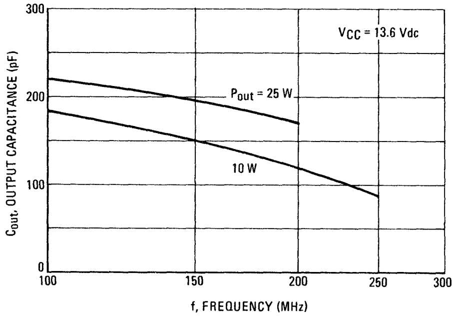
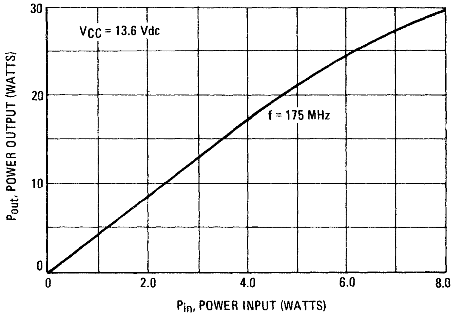


FIGURE 6 – POWER OUTPUT versus POWER INPUT



2N5629 (SILICON)
2N5630
2N5631

HIGH-VOLTAGE – HIGH POWER NPN TRANSISTORS

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc – 2N5629
  = 120 Vdc – 2N5630
  = 140 Vdc – 2N5631
- High DC Current Gain – @ I_C = 8.0 Adc
  h_{FE} = 25 (Min) – 2N5629
  = 20 (Min) – 2N5630
  = 15 (Min) – 2N5631
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Complement to PNP Transistor Series 2N6029, 2N6030, 2N6031

*MAXIMUM RATINGS

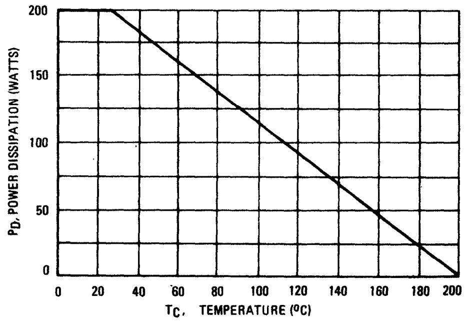
Rating	Symbol	2N5629	2N5630	2N5631	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 16 → ← 20 →			Adc
Base Current – Continuous	I_B	← 5.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 200 → ← 1.14 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

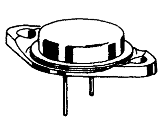
FIGURE 1 – POWER DERATING

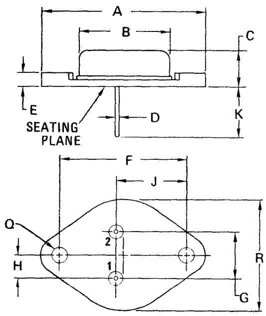


Safe Area Curves are indicated by Figure 5. All Limits are applicable and must be observed.

16 AMPERE
POWER TRANSISTORS
NPN SILICON

100-120-140 VOLTS
200 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

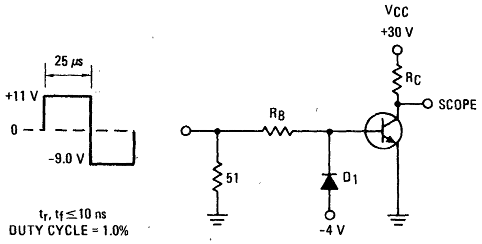
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5629		100	–	
	2N5630		120	–	
	2N5631		140	–	
Collector-Emitter Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N5629		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5630		–	1.0	
(V_{CE} = 70 Vdc, I_B = 0)	2N5631		–	1.0	
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			–	1.0	
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)	2N5629		25	100	
	2N5630		20	80	
	2N5631		15	60	
(I_C = 16 Adc, V_{CE} = 2.0 Vdc)	All Types		4.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	All Types		–	1.0	
(I_C = 16 Adc, I_B = 4.0 Adc)			–	2.0	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	500	pF
Small-Signal Current Gain (I_C = 4.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩾2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FIGURE 3 – TURN-ON TIME

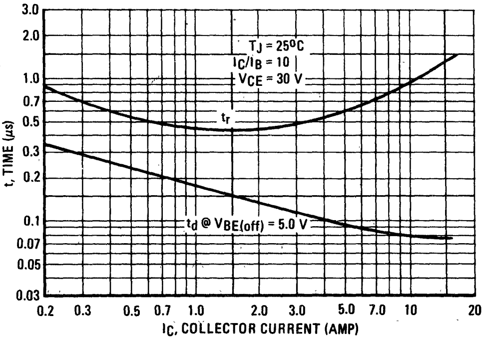


FIGURE 4 – THERMAL RESPONSE

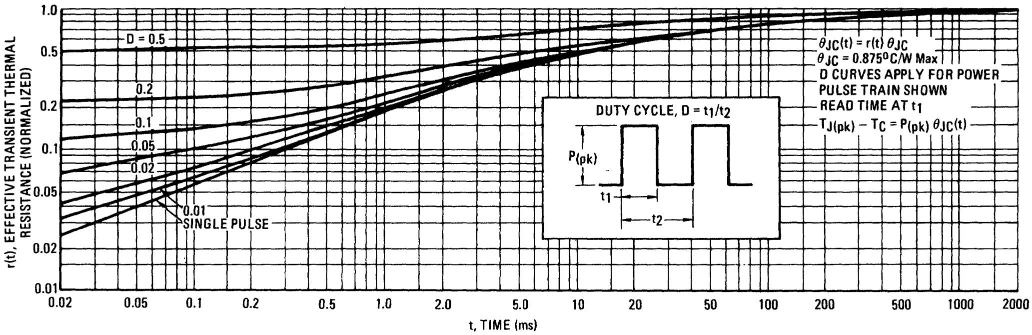
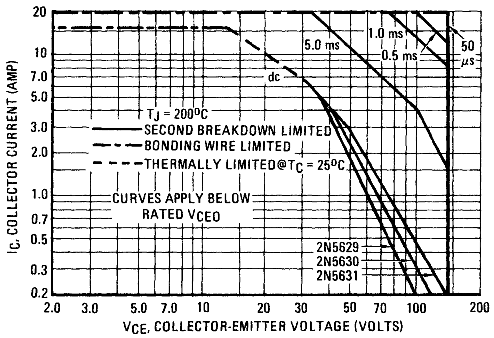


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

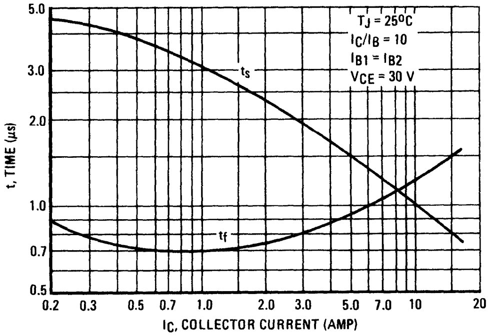


FIGURE 7 – CAPACITANCE

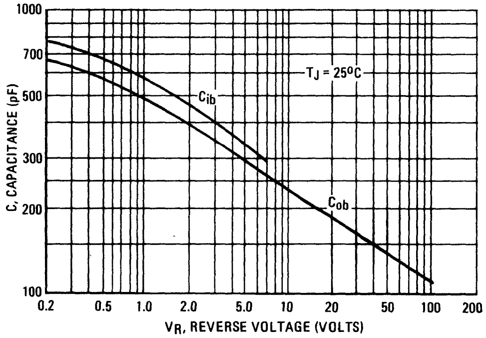


FIGURE 8 – DC CURRENT GAIN

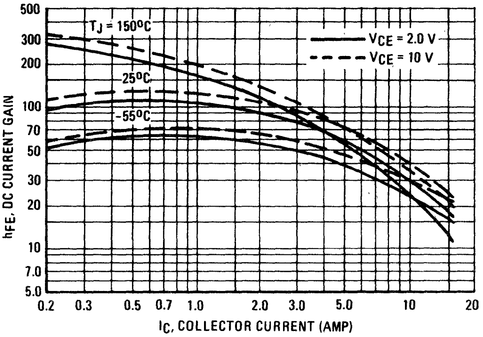


FIGURE 9 – COLLECTOR SATURATION REGION

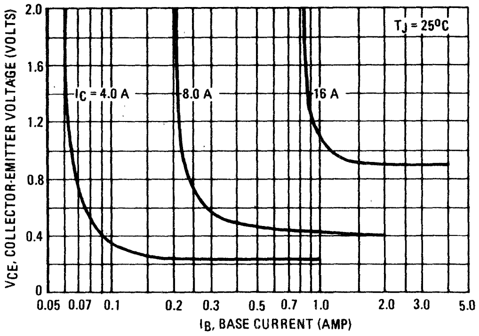


FIGURE 10 – ON VOLTAGES

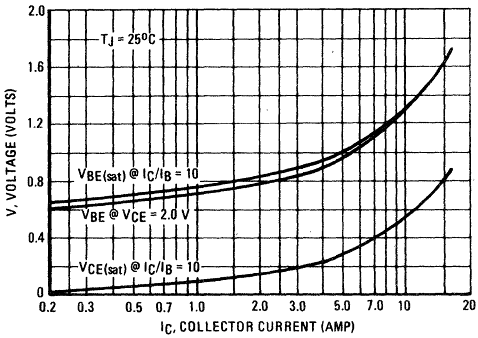


FIGURE 11 – TEMPERATURE COEFFICIENTS

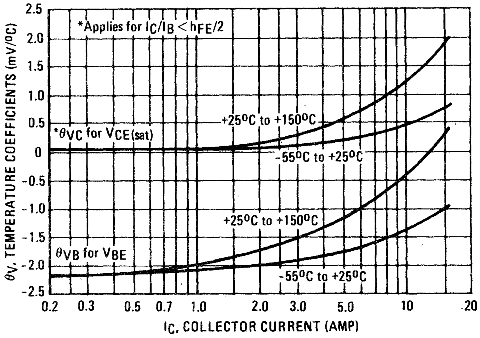


FIGURE 12 – COLLECTOR CUTOFF REGION

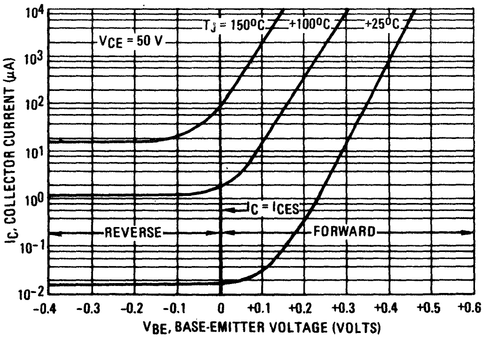
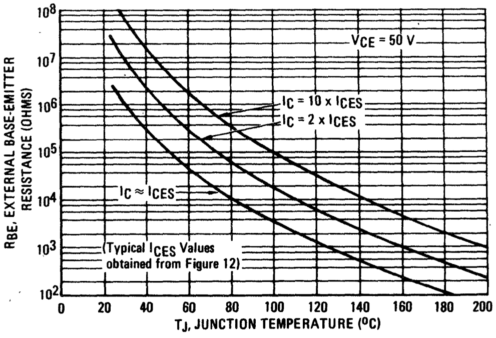


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N5632 (SILICON)
2N5633
2N5634

HIGH VOLTAGE-HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in high power audio amplifier applications and high-voltage switching regulator circuits.

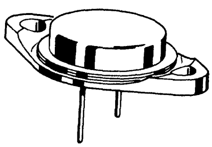
- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N5632
  = 120 Vdc (Min) – 2N5633
  = 140 Vdc (Min) – 2N5634
- High DC Current Gain @ I_C = 5.0 Adc –
  h_{FE} = 25 (Min) – 2N5632
  = 20 (Min) – 2N5633
  = 15 (Min) – 2N5634
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 7.5 Adc
- Complement to PNP Transistor Series
  2N6229, 2N6230, 2N6231

10 AMPERE

POWER TRANSISTOR

NPN SILICON

100-120-140 VOLTS
150 WATTS



*MAXIMUM RATINGS

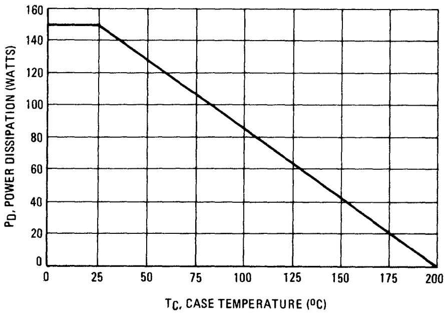
Rating	Symbol	2N5632	2N5633	2N5634	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	←	7.0	→	Vdc
Collector Current – Continuous – Peak	I_C	← ←	10 15	→ →	Adc
Base Current – Continuous	I_B	←	5.0	→	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	←	150 0.857	→	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	←	–65 to +200	→	°C

*THERMAL CHARACTERISTICS

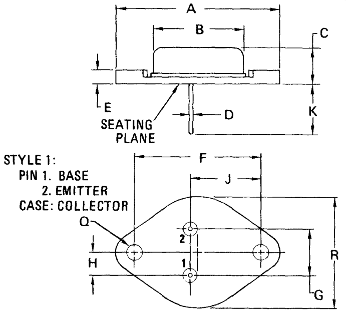
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



Safe area limits are indicated by Figure 5.
Both limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

Collector connected to case.

CASE 11-01

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

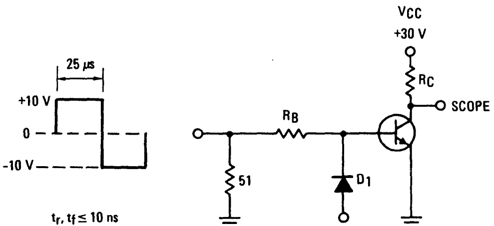
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage(1)	$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0) 2N5632		100	–	
2N5633		120	–	
2N5634		140	–	
Collector-Emitter Cutoff Current	I_{CEO}			mAdc
(V_{CE} = 50 Vdc, I_B = 0) 2N5632		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0) 2N5633		–	1.0	
(V_{CE} = 70 Vdc, I_B = 0) 2N5634		–	1.0	
Collector-Emitter Cutoff Current	I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)		–	1.0	
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		–	5.0	
Collector Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	–	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain(1)	h_{FE}			–
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc) 2N5632		25	100	
2N5633		20	80	
2N5634		15	60	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc) All Types		5.0	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 7.5 Adc, I_B = 0.75 Adc)		–	1.0	
(I_C = 10 Adc, I_B = 2.0 Adc)		–	2.0	
Base-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)	f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	300	pF
Small Signal Current Gain (V_{CE} = 10 Vdc, I_C = 2.0 Adc, f = 1.0 kHz)	h_{fe}	15	–	–

***Indicates JEDEC Registered Data.**

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



t_r, t_f ≤ 10 ns
DUTY CYCLE = 1.0%

R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FIGURE 3 – TURN-ON TIME

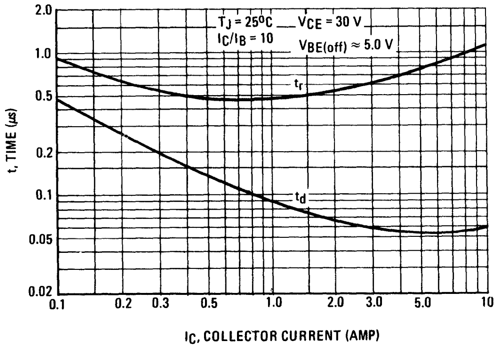


FIGURE 4 – THERMAL RESPONSE

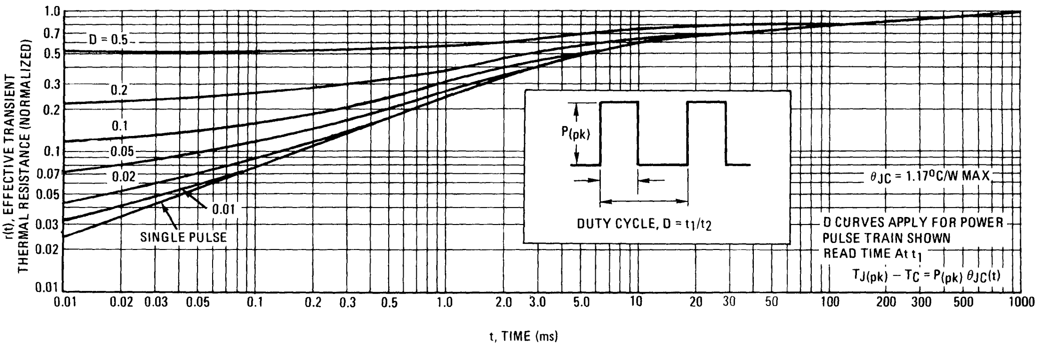
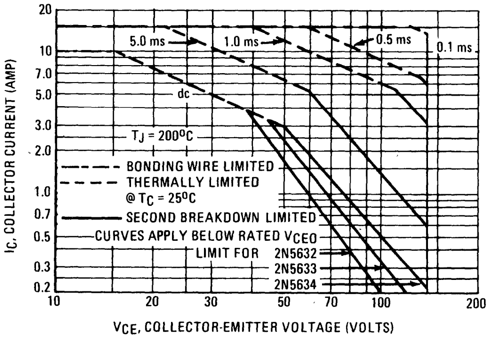


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

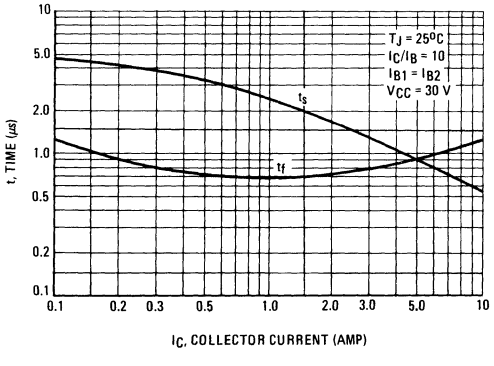


FIGURE 7 – CAPACITANCE

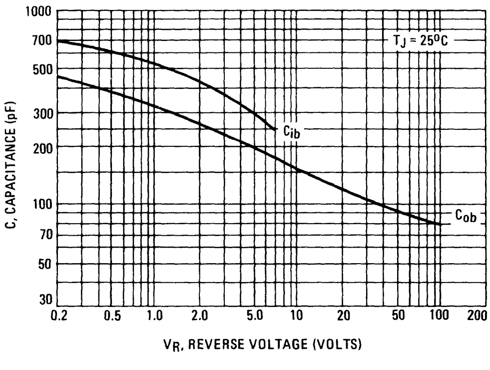


FIGURE 8 – DC CURRENT GAIN

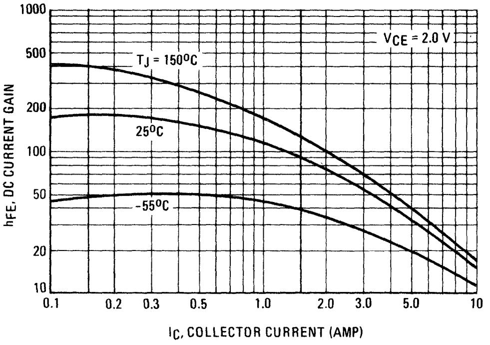


FIGURE 9 – COLLECTOR SATURATION REGION

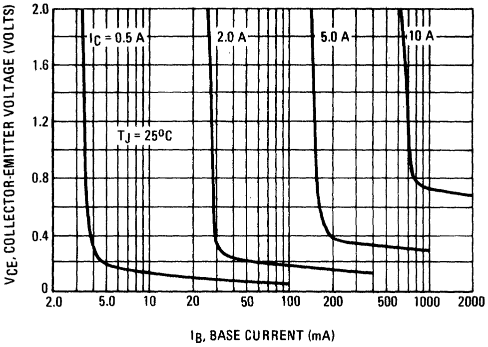


FIGURE 10 – "ON" VOLTAGES

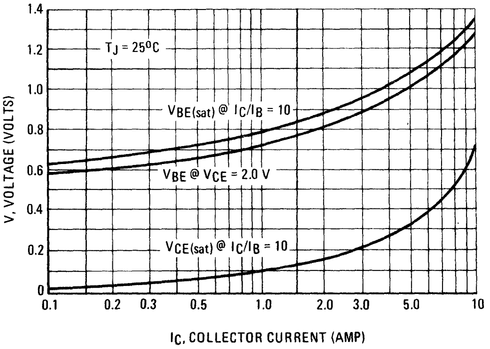


FIGURE 11 – TEMPERATURE COEFFICIENTS

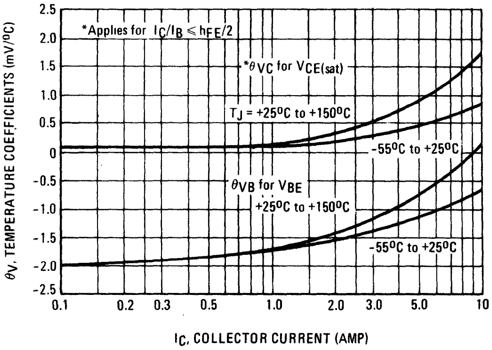


FIGURE 12 – COLLECTOR CUTOFF REGION

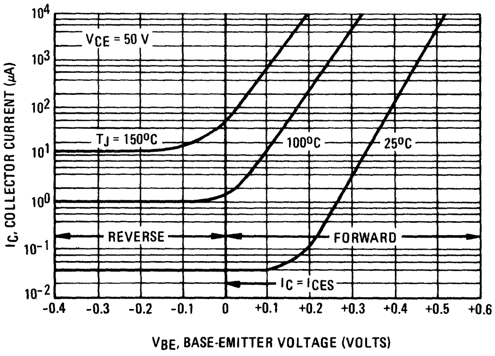
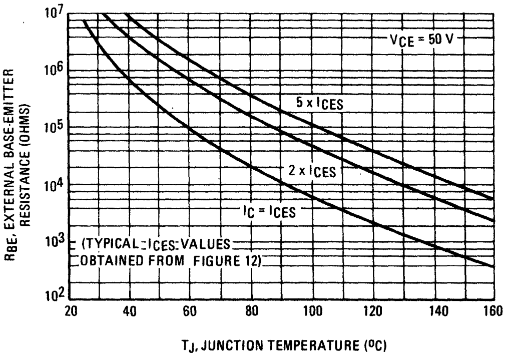


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



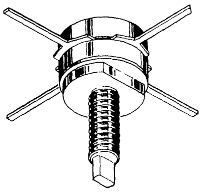
2N5635 (SILICON)
2N5636
2N5637

NPN SILICON RF POWER TRANSISTORS

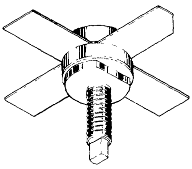
. . . designed for VHF/UHF amplifier applications. These devices are suitable for use in 28 volt systems to 470 MHz. These transistors are ideal for 225-400 MHz communications equipment.

- Balanced Emitter Construction to provide the designer with the device technology that assures ruggedness and resists transistor damage caused by load mismatch.
- Low inductance strip line packaging for easier and better broadband designs.
- Ceramic Package
- Choice of Power Levels at 400 MHz, 28 Vdc –
  2N5635 – 2.5 Watts – 6.2 dB (Min) Gain
  2N5636 – 7.5 Watts – 5.7 dB (Min) Gain
  2N5637 – 20 Watts – 4.6 dB (Min) Gain

NPN SILICON
RF POWER
TRANSISTORS



2N5635
2N5636

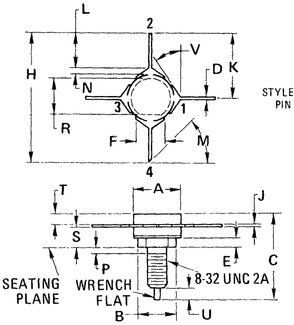


2N5637

*MAXIMUM RATINGS

Rating	Symbol	2N5635	2N5636	2N5637	Unit
Collector-Emitter Voltage	V_{CEO}	← 35 →			Vdc
Collector-Base Voltage	V_{CB}	← 60 →			Vdc
Emitter-Base Voltage	V_{EB}	← 4.0 →			Vdc
Collector Current	I_C	1.0	1.5	3.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	7.5 43	15 86	30 171	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200			°C

*Indicates JEDEC Registered Data.

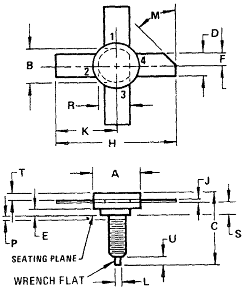


STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0 385
B	8.13	8.38	0 320	0.330
C	17.63	19.46	0.694	0.766
D	0 64	0.89	0.025	0.035
E	1.78	2.03	-0 070	0.080
F	5.59	5.84	0.220	0.230
H	26.16	27.69	1.030	1 090
J	0.10	0 15	0.004	0.006
K	13.08	13 84	0.515	0.545
L	7.11	7.37	0.280	0 290
M	40°	50°	40°	50°
N	1 27	1.52	0.050	0.060
P		1.27		0.050
R	7 59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2 16	2 41	0.085	0.095
U	2.54	3.30	0.100	0.130
V	10°	20°	10°	20°

CASE 144B-03

2N5635, 2N5636



STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

2N5637

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0 370	0.385
B	8.13	8.38	0.320	0.330
C	18.03	19.05	0.710	0 750
D	5.59	5.84	0.220	0.230
E	1.78	2.03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1 130
J	0.10	0.15	0 004	0.006
K	13.21	14 35	0.520	0 565
L	1.40	1.65	0 055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0 178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130

NOTE
CASE 145A-01 USE 8 32NC2A STUD

CASE 145A-01

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

OFF CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Collector-Emitter Breakdown Voltage (Note 1)		BV_{CEO}				Vdc
(I_C = 100 mAdc, I_B = 0)	2N5635		35	–	–	
(I_C = 200 mAdc, I_B = 0)	2N5636,2N5637		35	–	–	
Collector-Emitter Breakdown Voltage (Note 1)		BV_{CES}				Vdc
(I_C = 100 mAdc, V_{BE} = 0)	2N5635		60	–	–	
(I_C = 200 mAdc, V_{BE} = 0)	2N5636,2N5637		60	–	–	
Emitter-Base Breakdown Voltage		BV_{EBO}				Vdc
(I_E = 1.0 mAdc, I_C = 0)	2N5635		4.0	–	–	
(I_E = 5.0 mAdc, I_C = 0)	2N5636		4.0	–	–	
(I_E = 10 mAdc, I_C = 0)	2N5637		4.0	–	–	
Collector Cutoff Current		I_{CBO}				mAdc
(V_{CB} = 30 Vdc, I_E = 0)	2N5635		–	–	0.1	
	2N5636		–	–	1.0	
	2N5637		–	–	1.0	

ON CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
DC Current Gain		h_{FE}				–
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	2N5635		5.0	–	–	
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	2N5636		5.0	–	–	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	2N5637		5.0	–	–	

DYNAMIC CHARACTERISTICS

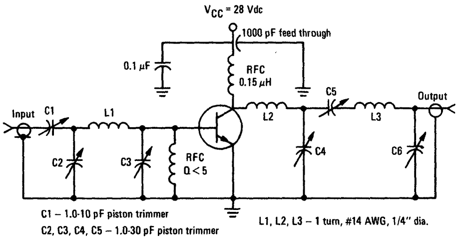
Characteristic		Symbol	Min	Typ	Max	Unit
Output Capacitance		C_{ob}				pF
(V_{CB} = 30 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	2N5635		–	5.0	10	
	2N5636		–	10	20	
	2N5637		–	20	30	

FUNCTIONAL TEST

Characteristic		Symbol	Min	Typ	Max	Unit
Common-Emitter Amplifier Power Gain		G_{PE}				dB
(P_{out} = 2.5 Watts, V_{CE} = 28 Vdc, f = 400 MHz)	2N5635		6.2	9.2	–	
(P_{out} = 7.5 Watts, V_{CE} = 28 Vdc, f = 400 MHz)	2N5636		5.7	7.0	–	
(P_{out} = 20 Watts, V_{CE} = 28 Vdc, f = 400 MHz)	2N5637		4.6	5.8	–	
Power Output		P_{out}				Watts
(P_{in} = 0.6 Watt, V_{CE} = 28 Vdc, f = 400 MHz)	2N5635		2.5	3.2	–	
(P_{in} = 2.0 Watts, V_{CE} = 28 Vdc, f = 400 MHz)	2N5636		7.5	8.4	–	
(P_{in} = 7.0 Watts, V_{CE} = 28 Vdc, f = 400 MHz)	2N5637		20	22	–	
Collector Efficiency		η				%
(P_{out} = 2.5 Watts, V_{CE} = 28 Vdc, f = 400 MHz)	2N5635		50	–	–	
(P_{out} = 7.5 Watts, V_{CE} = 28 Vdc, f = 400 MHz)	2N5636		50	–	–	
(P_{out} = 20 Watts, V_{CE} = 28 Vdc, f = 400 MHz)	2N5637		60	–	–	

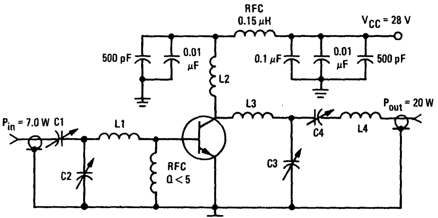
***Indicates JEDEC Registered Data.**
Note 1: Pulsed through 25 mH inductor.

FIGURE 1 – 400 MHz TEST CIRCUIT (2N5635,2N5636)



C1 – 1.0-10 pF piston trimmer
C2, C3, C4, C5 – 1.0-30 pF piston trimmer
C6 – 1.0-20 pF piston trimmer
L1, L2, L3 – 1 turn, #14 AWG, 1/4" dia.

FIGURE 2 – 400 MHz TEST CIRCUIT (2N5637)



C1 – 1.0-30 pF piston trimmer
C2, C3, C4 – 1.0-10 pF piston trimmer
L1 – 12 nH, #14 straight wire, 3/4" long
L2 – 30 nH, 3 Turns #16 AWG, ¼" O. D., ½" L.
L3 – 40 nH, 1 Turn #16 AWG, 3/8 O. D.
L4 – 10 nH, 1/4" wide, 3/8" long Cu Strap

TYPICAL PERFORMANCE DATA

POWER OUTPUT versus FREQUENCY

FIGURE 3

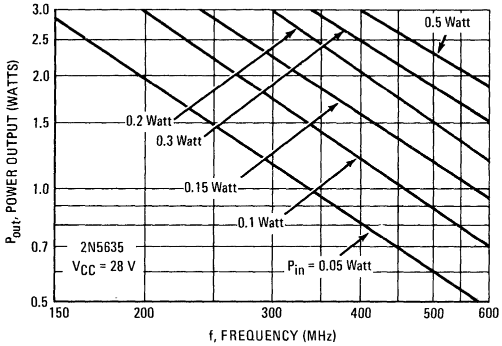


FIGURE 4

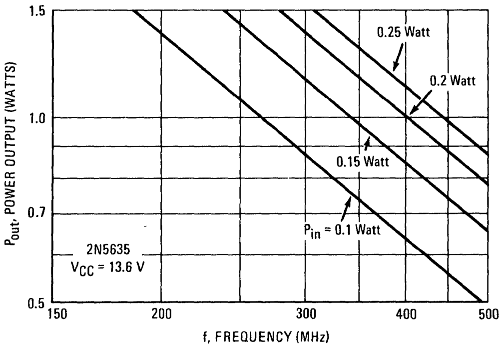


FIGURE 5

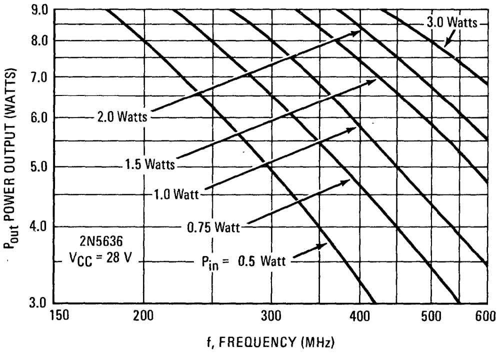


FIGURE 6

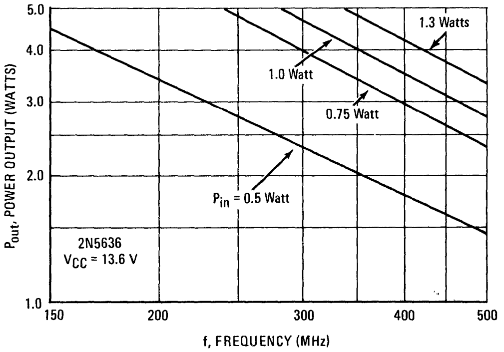


FIGURE 7

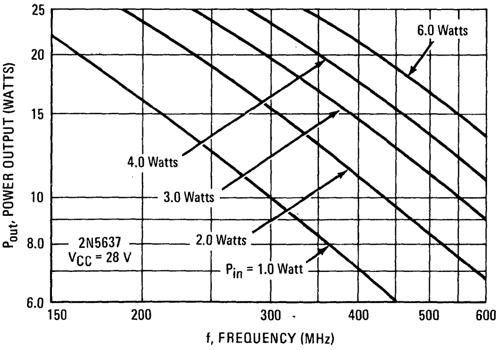
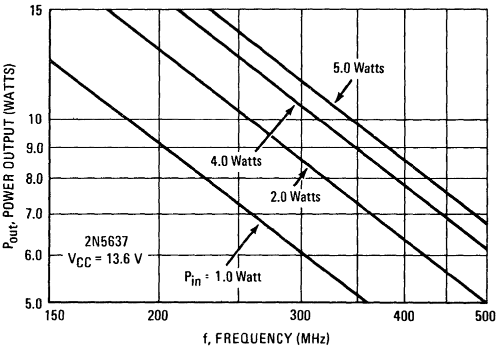


FIGURE 8



TYPICAL PERFORMANCE DATA

POWER OUTPUT versus POWER INPUT

FIGURE 9

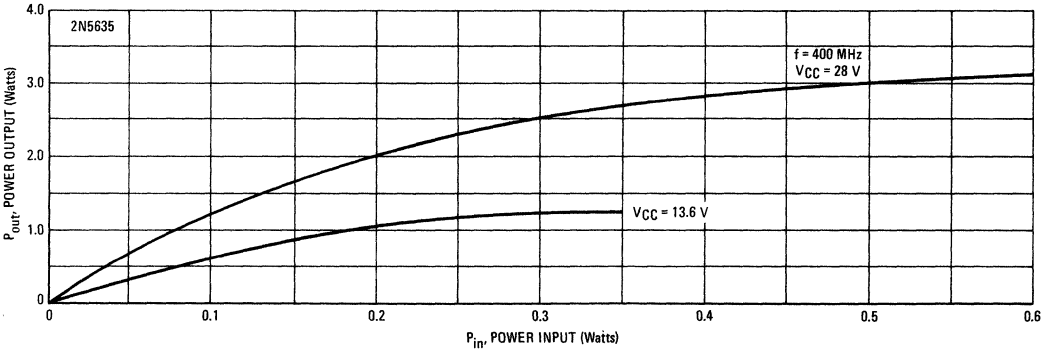


FIGURE 10

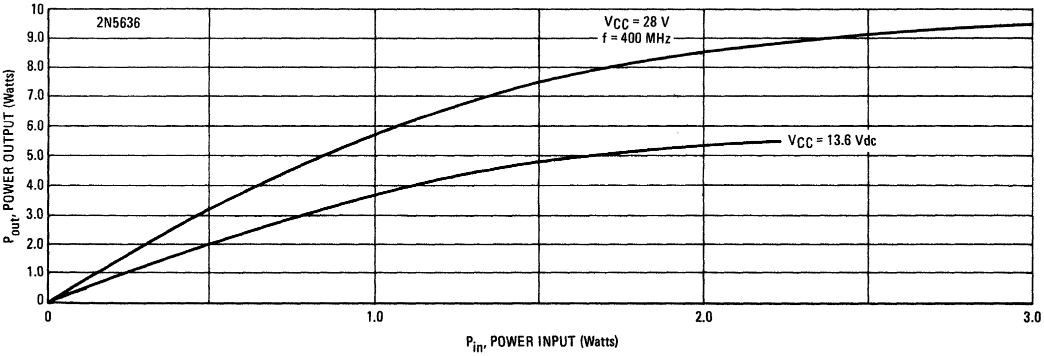
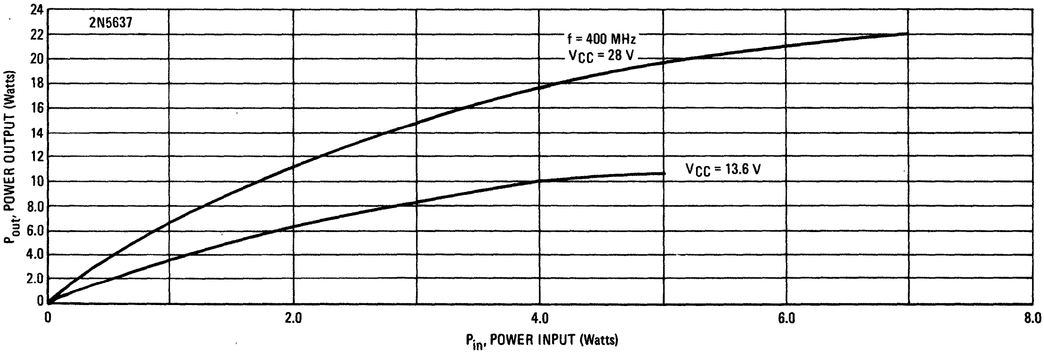


FIGURE 11



CIRCUIT DESIGN DATA

PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

FIGURE 12

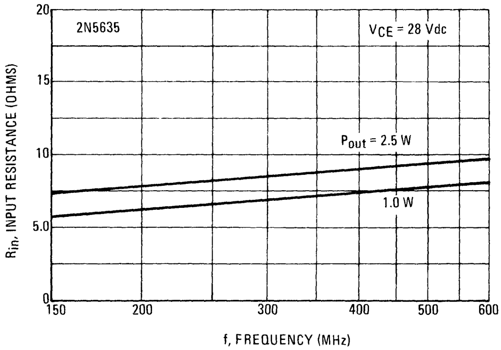


FIGURE 14

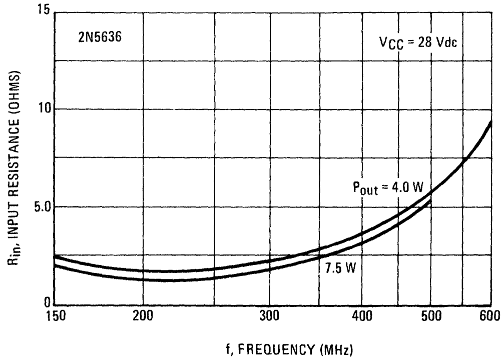
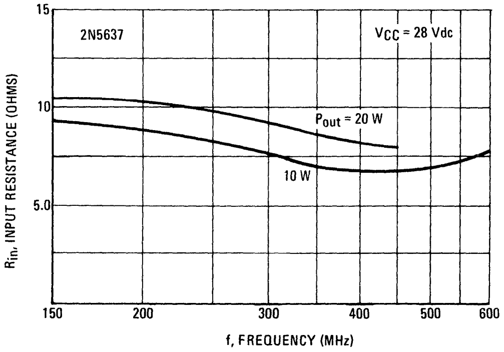


FIGURE 16



PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

FIGURE 13

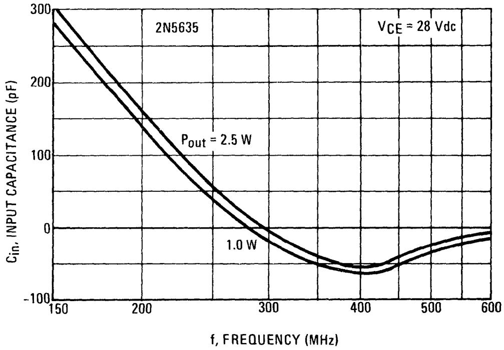


FIGURE 15

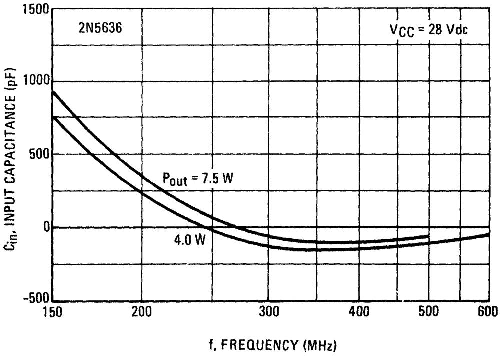
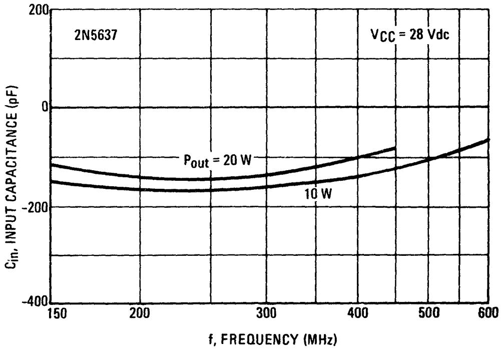


FIGURE 17



CIRCUIT DESIGN DATA

LARGE SIGNAL OUTPUT CAPACITANCE versus FREQUENCY

FIGURE 18

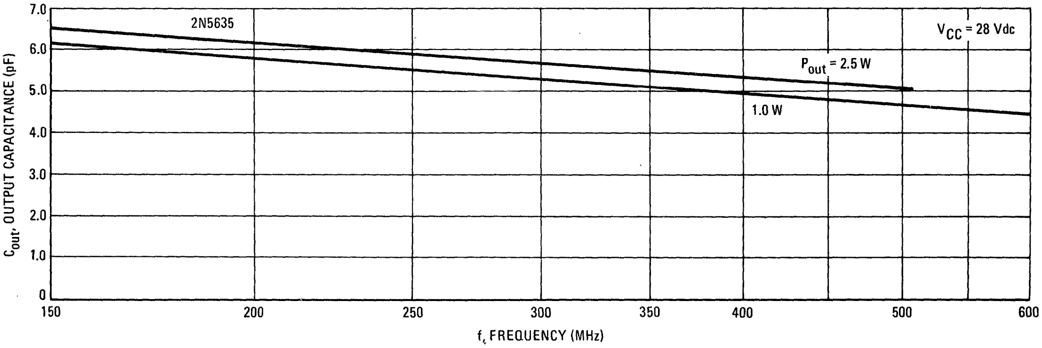


FIGURE 19

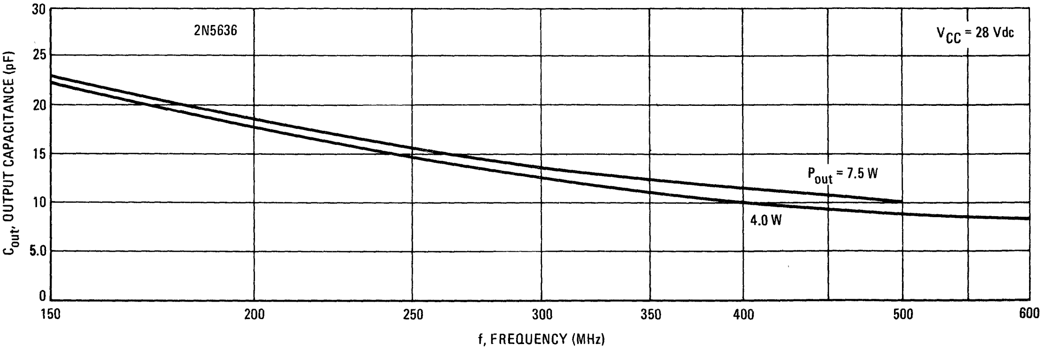
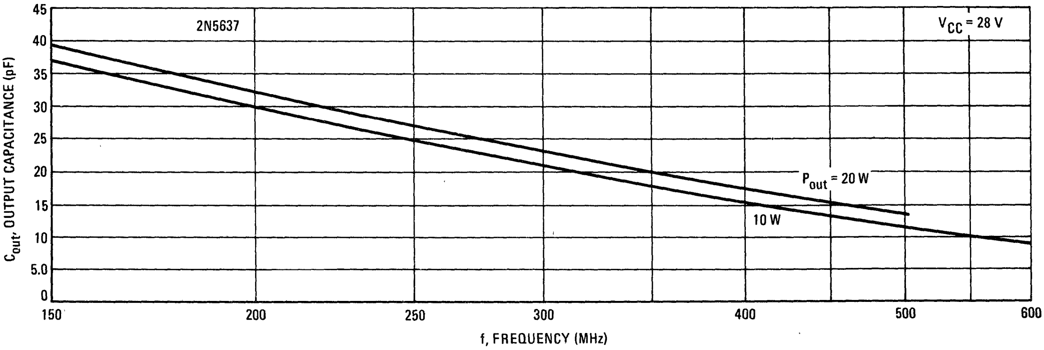


FIGURE 20



DC SAFE OPERATING AREA

FIGURE 21

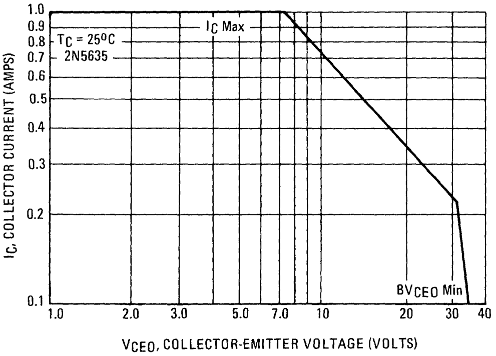


FIGURE 23

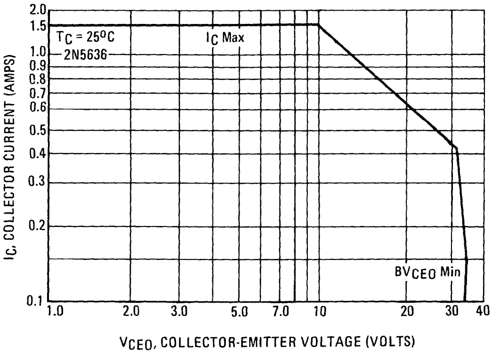
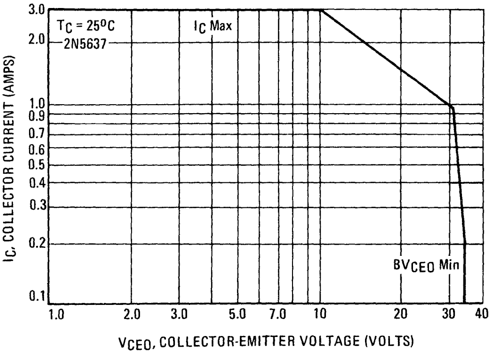


FIGURE 25



POWER DISSIPATION DERATING CURVE

FIGURE 22

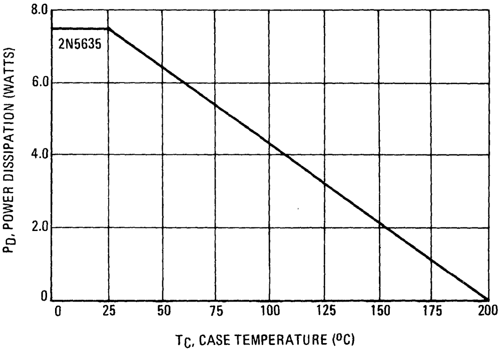


FIGURE 24

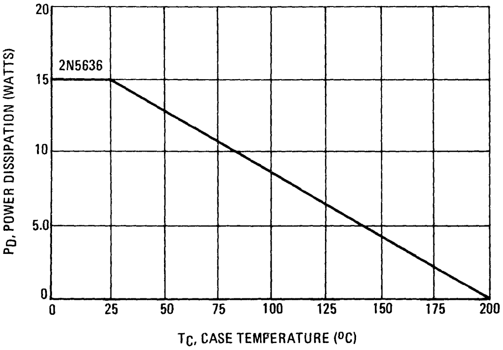
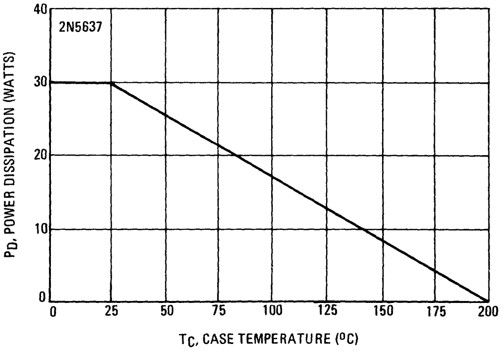


FIGURE 26



APPLICATION INFORMATION

In addition to a fine selection of quality RF Semiconductors, Motorola provides applications information in the form of Application Notes. Any of the notes listed on this page may be obtained by writing to the Technical Information Center, Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Arizona.

Small Signal RF Design

AN-139A- Understanding Transistor Response Parameters
AN-166 – Using Linvill Techniques for RF Amplifiers
AN-215A – RF Small Signal Design Using 2-Port Parameters
AN-238 – Transistor Mixer Design Using Admittance Parameters
AN-247A- An Integrated Circuit RF-IF Amplifier
AN-419 – UHF Amplifier Design Using Data Sheet Curves
AN-421 – Semiconductor Noise Figure Considerations
AN-423 – Field-Effect Transistor RF Amplifier Design Techniques

RF Power Transistor Circuit Design

AN-267 – Matching Network Designs with Computer Solutions
AN-282A – Systemizing RF Power Amplifier Design

2N5638 (SILICON)
2N5639
2N5640

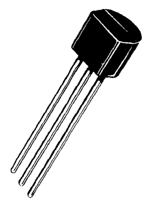
N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

. . . depletion mode (Type A) Junction Field-Effect Transistors designed for chopper and high-speed switching applications.

- Low Drain-Source "ON" Resistance –
  $r_{ds(on)}$ = 30 Ohms (2N5638)
  60 Ohms (2N5639)
  100 Ohms (2N5640)
- Low Reverse Transfer Capacitance –
  C_{rss} = 4.0 pF (Max) @ f = 1.0 MHz
- Fast Switching Characteristics –
  t_r = 5.0 ns (Max) (2N5638)

N-CHANNEL
JUNCTION
FIELD-EFFECT
TRANSISTORS

TYPE A

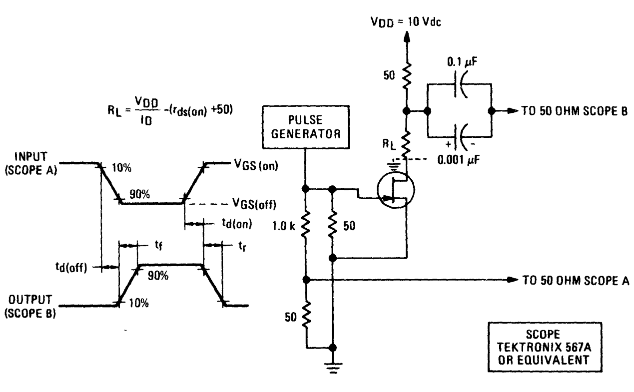


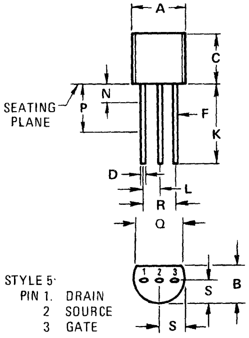
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
*Drain-Gate Voltage	V_{DG}	30	Vdc
*Reverse Gate-Source Voltage	V_{GSR}	30	Vdc
*Forward Gate Current	I_{GF}	10	mAdc
*Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D (1)	310 2.82	mW mW/°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Range	T_J (1)	-65 to +135	°C

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125°C/W.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

*Indicates JEDEC Registered Data.

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	–	Vdc
Gate Reverse Current		I_{GSS}			
(V_{GS} = –15 Vdc, V_{DS} = 0)			–	1.0	nAdc
(V_{GS} = –15 Vdc, V_{DS} = 0, T_A = 100°C)			–	1.0	μAdc
Drain Cutoff Current		$I_{D(off)}$			
(V_{DS} = 15 Vdc, V_{GS} = –12 Vdc)	2N5638		–	1.0	nAdc
(V_{DS} = 15 Vdc, V_{GS} = –8.0 Vdc)	2N5639		–	1.0	
(V_{DS} = 15 Vdc, V_{GS} = –6.0 Vdc)	2N5640		–	1.0	
(V_{DS} = 15 Vdc, V_{GS} = –12 Vdc, T_A = 100°C)	2N5638		–	1.0	μAdc
(V_{DS} = 15 Vdc, V_{GS} = –8.0 Vdc, T_A = 100°C)	2N5639		–	1.0	
(V_{DS} = 15 Vdc, V_{GS} = –6.0 Vdc, T_A = 100°C)	2N5640		–	1.0	
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (Note 1)		I_{DSS}			mAdc
(V_{DS} = 20 Vdc, V_{GS} = 0)	2N5638		50	–	
	2N5639		25	–	
	2N5640		5.0	–	
Drain-Source "ON" Voltage		$V_{DS(on)}$			Vdc
(I_D = 12 mAdc, V_{GS} = 0)	2N5638		–	0.5	
(I_D = 6.0 mAdc, V_{GS} = 0)	2N5639		–	0.5	
(I_D = 3.0 mAdc, V_{GS} = 0)	2N5640		–	0.5	
Static Drain-Source "ON" Resistance		$r_{DS(on)}$			Ohms
(I_D = 1.0 mAdc, V_{GS} = 0)	2N5638		–	30	
	2N5639		–	60	
	2N5640		–	100	
SMALL-SIGNAL CHARACTERISTICS					
Static Drain-Source "ON" Resistance		$r_{ds(on)}$			Ohms
(V_{GS} = 0, I_D = 0, f = 1.0 kHz)	2N5638		–	30	
	2N5639		–	60	
	2N5640		–	100	
Input Capacitance (V_{DS} = 0, V_{GS} = –12 Vdc, f = 1.0 MHz)		C_{iss}	–	10	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = –12 Vdc, f = 1.0 MHz)		C_{rss}	–	4.0	pF

SWITCHING CHARACTERISTICS (Figure 1)

Characteristic	Conditions			Symbol	Min	Max	Unit
Turn-On Delay Time	V_{DD} = 10 Vdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = –10 Vdc, R_G' = 50 ohms	$I_{D(on)}$ = 12 mAdc	2N5638	$t_{d(on)}$	–	4.0	ns
		6.0 mAdc	2N5639		–	6.0	
		3.0 mAdc	2N5640		–	8.0	
Rise Time		$I_{D(on)}$ = 12 mAdc	2N5638	t_r	–	5.0	ns
		6.0 mAdc	2N5639		–	8.0	
		3.0 mAdc	2N5640		–	10	
Turn-Off Delay Time		$I_{D(on)}$ = 12 mAdc	2N5638	$t_{d(off)}$	–	5.0	ns
		6.0 mAdc	2N5639		–	10	
		3.0 mAdc	2N5640		–	15	
Fall Time		$I_{D(on)}$ = 12 mAdc	2N5638	t_f	–	10	ns
		6.0 mAdc	2N5639		–	20	
		3.0 mAdc	2N5640		–	30	

*Indicates JEDEC Registered Data.

Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 3.0%.

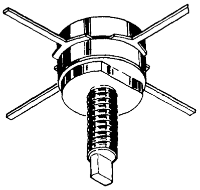
2N5641 (SILICON)
2N5642
2N5643

NPN SILICON RF POWER TRANSISTORS

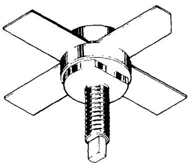
. . . designed for VHF power amplifier or oscillator applications in military and industrial equipment. These devices are particularly suited for use in Class AB, B, or C amplifier applications to 400 MHz.

- Balanced Emitter Construction to provide the designer with the device technology that assures ruggedness and resists transistor damage caused by load mismatch.
- Stripline packaging for lower lead inductance and better broadband capability.
- Ceramic Packaging
- Specified 28 Volt, 175 MHz Characteristics –
  - 2N5641 – 7.0 Watts Output Power at 8.4 dB Gain
  - 2N5642 – 20 Watts Output Power at 8.2 dB Gain
  - 2N5643 – 40 Watts Output Power at 7.6 dB Gain

NPN SILICON
RF POWER
TRANSISTORS



2N5641

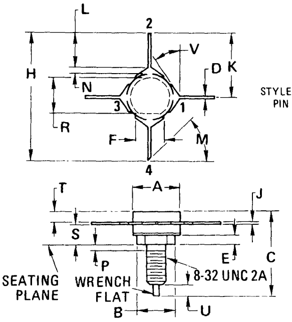


2N5642
2N5643

*MAXIMUM RATINGS

Rating	Symbol	2N5641	2N5642	2N5643	Unit
Collector-Emitter Voltage	V_{CEO}	←	35	→	Vdc
Collector-Base Voltage	V_{CB}	←	65	→	Vdc
Emitter-Base Voltage	V_{EB}	←	4.0	→	Vdc
Collector Current – Continuous	I_C	1.0	3.0	5.0	Adc
Total Device Dissipation @ $T_A = 25^oC$ Derate above 25°C	P_D	15 86	30 171	60 342	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

*Indicates JEDEC Registered Data.

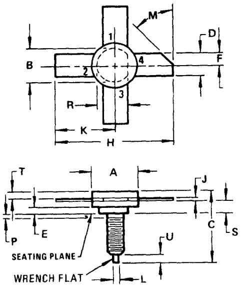


STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8 13	8.38	0 320	0.330
C	17.63	19.46	0.694	0.766
D	0.64	0.89	0.025	0.035
E	1.78	2.03	0 070	0.080
F	5.59	5.84	0.220	0.230
H	26.16	27.69	1 030	1.090
J	0.10	0.15	0.004	0.006
K	13.08	13.84	0.515	0.545
L	7.11	7.37	0.280	0.290
M	40°	50°	40°	50°
N	1.27	1 52	0 050	0.060
P		1.27		0.050
R	7 59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130
V	10°	20°	10°	20°

2N5641

CASE 144B-03



STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

2N5642
2N5643

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9 40	9.78	0 370	0.385
B	8.13	8.38	0.320	0 330
C	18.03	19 05	0.710	0.750
D	5.59	5.84	0.220	0.230
E	1.78	2 03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14 35	0.520	0.565
L	1.40	1 65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7 59	7 80	0.299	0.307
S	4 01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2 54	3.30	0 100	0 130

NOTE
CASE 145A 01 USE 8 32NC2A STUD

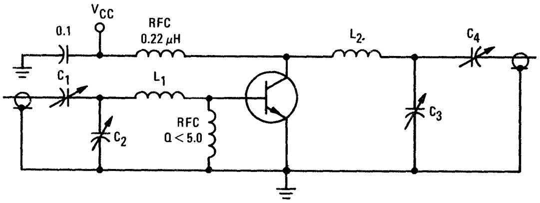
CASE 145A-01

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	BV_{CEO}	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	BV_{CES}	65	–	–	Vdc
Emitter-Base Breakdown Voltage	BV_{EBO}				Vdc
(I_E = 5.0 mAdc, I_C = 0) 2N5641		4.0	–	–	
(I_E = 10 mAdc, I_C = 0) 2N5642,2N5643		4.0	–	–	
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				–
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc) 2N5641		5.0	–	–	
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc) 2N5642		5.0	–	–	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc) 2N5643		5.0	–	–	
DYNAMIC CHARACTERISTICS					
Output Capacitance	C_{ob}				pF
(V_{CB} = 30 Vdc, I_E = 0, f = 0.1 to 1.0 MHz) 2N5641		–	8.5	15	
2N5642		–	22	35	
2N5643		–	45	65	
FUNCTIONAL TEST					
Power Input (Figure 1)	P_{in}				Watts
(P_{out} = 7.0 Watts, V_{CE} = 28 Vdc, f = 175 MHz) 2N5641		–	0.4	1.0	
(P_{out} = 20 Watts, V_{CE} = 28 Vdc, f = 175 MHz) 2N5642		–	1.9	3.0	
(P_{out} = 40 Watts, V_{CE} = 28 Vdc, f = 175 MHz) 2N5643		–	5.0	7.0	
Common-Emitter Amplifier Power Gain (Figure 1)	G_{PE}				dB
(P_{out} = 7.0 Watts, V_{CE} = 28 Vdc, f = 175 MHz) 2N5641		8.4	12.5	–	
(P_{out} = 20 Watts, V_{CE} = 28 Vdc, f = 175 MHz) 2N5642		8.2	10.2	–	
(P_{out} = 40 Watts, V_{CE} = 28 Vdc, f = 175 MHz) 2N5643		7.6	8.1		
Collector Efficiency (Figure 1)	η				%
(P_{out} = 7.0 Watts, V_{CE} = 28 Vdc, f = 175 MHz) 2N5641		60	–	–	
(P_{out} = 20 Watts, V_{CE} = 28 Vdc, f = 175 MHz) 2N5642		60	–	–	
(P_{out} = 40 Watts, V_{CE} = 28 Vdc, f = 175 MHz) 2N5643		60	–	–	

Note 1: Pulsed through 25 mH inductor.
***Indicates JEDEC Registered Data.**

FIGURE 1 – 175 MHz TEST CIRCUIT



2N5641

C_1, C_3, C_4 – 5.0 – 80 pF

C_2 – 9.0 – 180 pF

L_1 – 1¼" Straight #14 AWG

L_2 – 3 Turns #16 AWG, ¼" I.D.

2N5642

C_1 – 3.0 – 30 pF

C_2, C_3, C_4, – 9.0 – 180 pF

L_1 – 1" Straight #14 AWG

L_2 – 1 Turn #16 AWG, ¼" I.D.

2N5643

C_1, C_2, C_3, C_4, - ARCO 464 25-280 pF

L_1 – 1" Straight #14 AWG

L_2 – 1 Turn #16 AWG, ¼" I.D.

TYPICAL PERFORMANCE DATA

POWER OUTPUT versus FREQUENCY

FIGURE 2

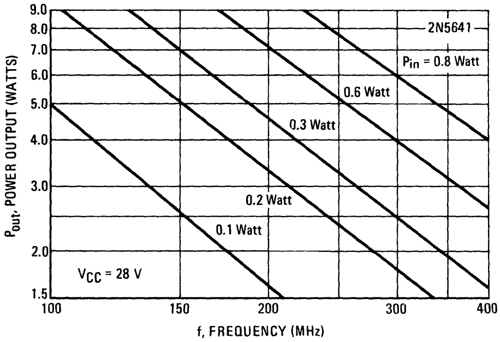


FIGURE 3

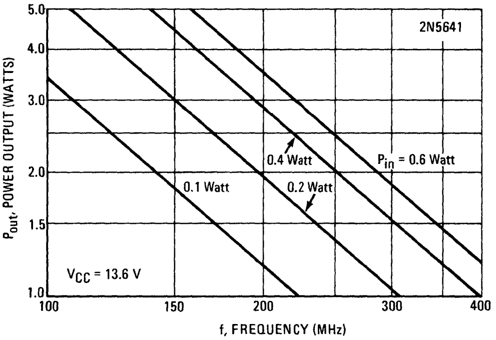


FIGURE 4

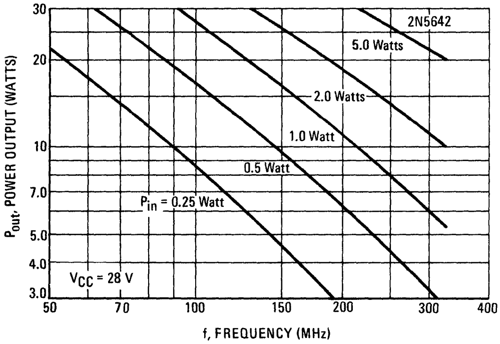


FIGURE 5

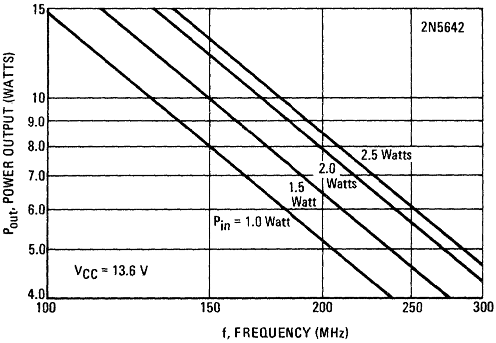


FIGURE 6

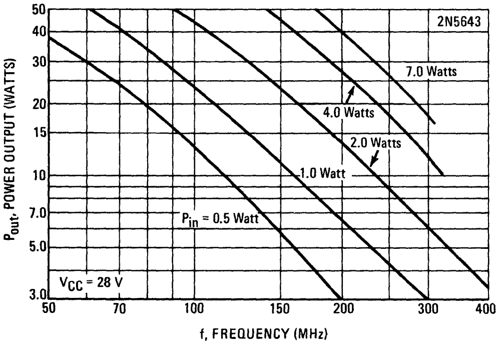
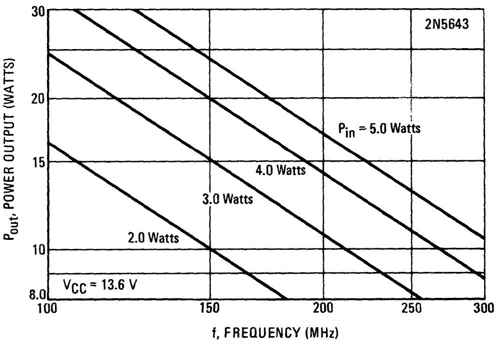


FIGURE 7



TYPICAL PERFORMANCE DATA
POWER OUTPUT versus POWER INPUT

FIGURE 8

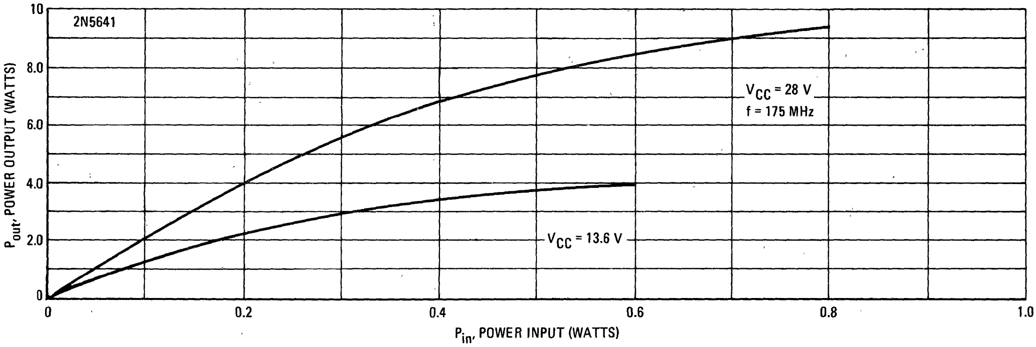


FIGURE 9

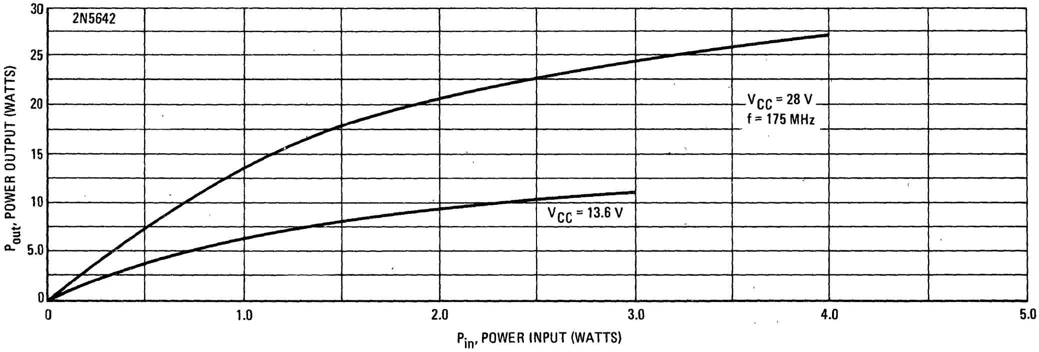
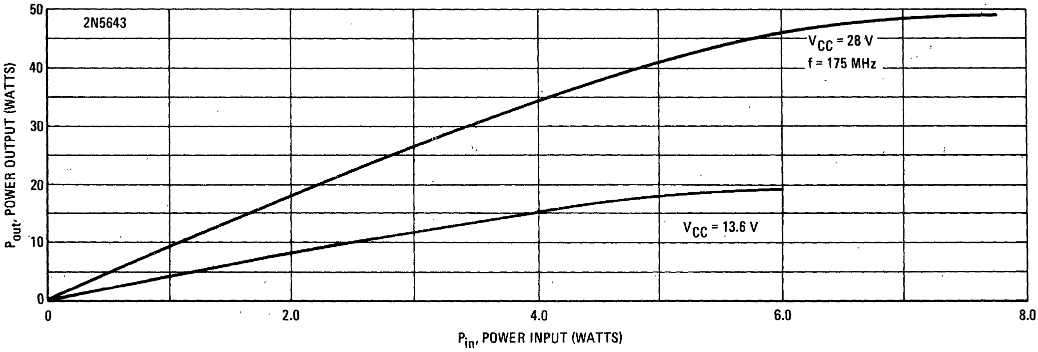


FIGURE 10



CIRCUIT DESIGN DATA

PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

FIGURE 11

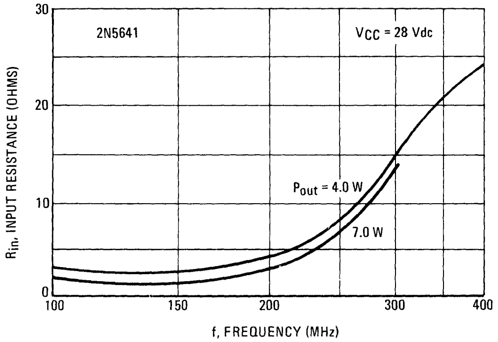


FIGURE 13

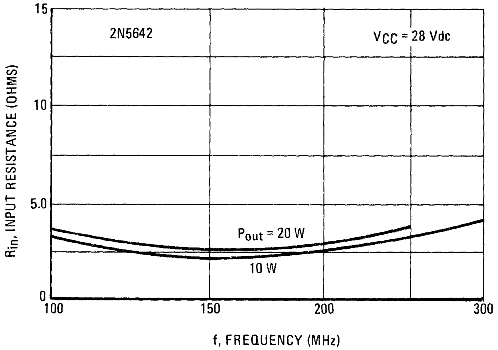
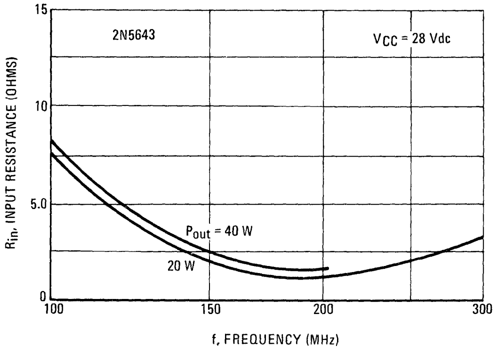


FIGURE 15



PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

FIGURE 12

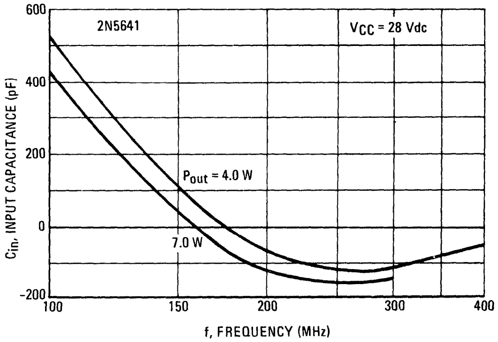


FIGURE 14

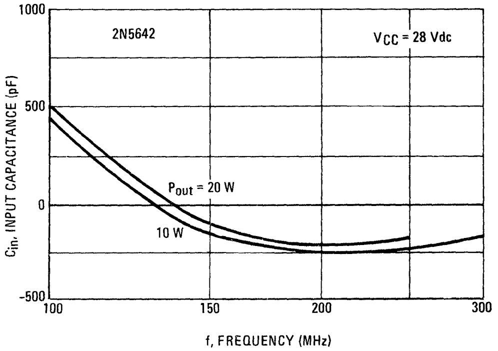
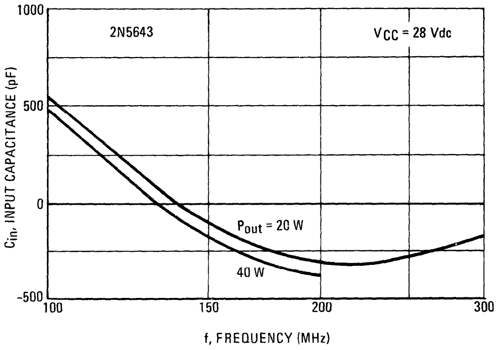


FIGURE 16



CIRCUIT DESIGN DATA

LARGE SIGNAL OUTPUT CAPACITANCE versus FREQUENCY

FIGURE 17

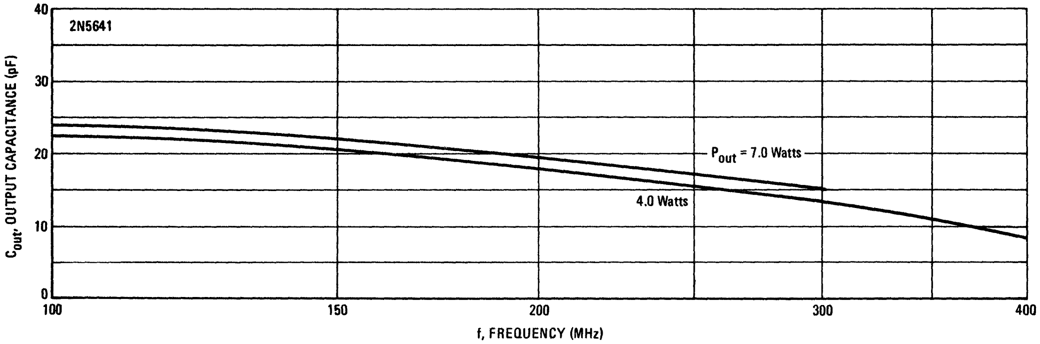


FIGURE 18

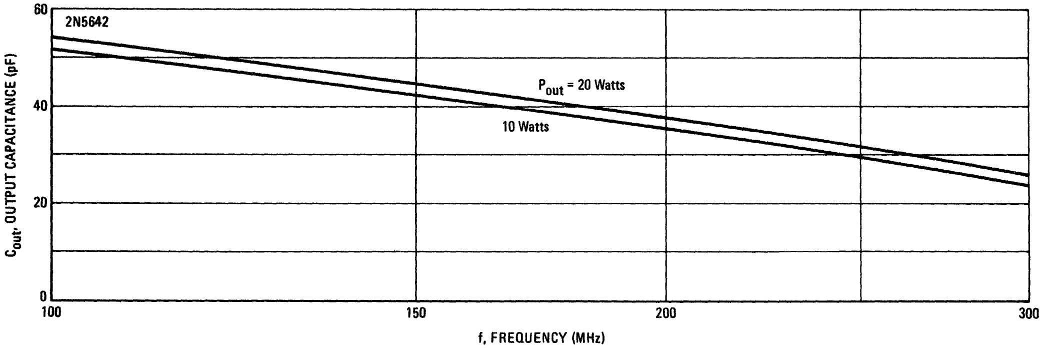
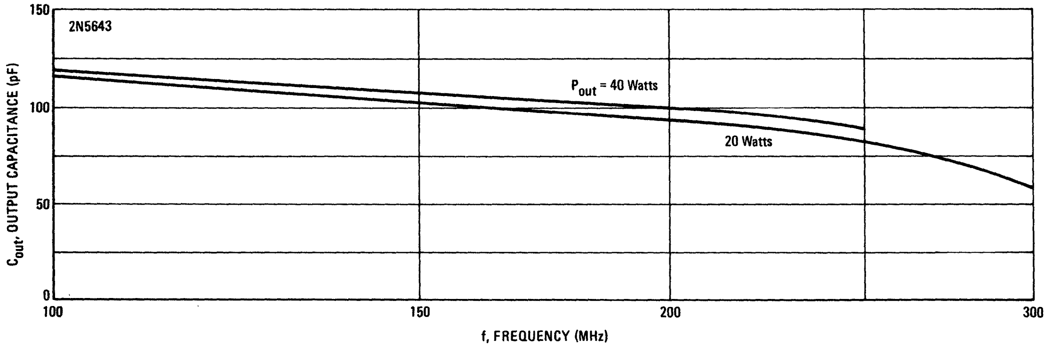


FIGURE 19



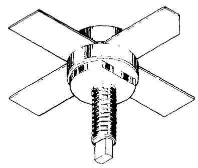
2N5644 (SILICON)

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt, UHF large signal amplifier applications required in industrial and consumer FM equipment operating to 520 MHz.

- Low lead inductance stripline package for ease of design and increased broadband capability
- Balanced Emitter Construction to protect against device damage due to load mismatch
- Specified 12.5 Volt, 470 MHz Characteristics –
  Output Power = 1.0 Watt
  Minimum Gain = 7.0 dB
  Efficiency = 60%

NPN SILICON
RF POWER
TRANSISTOR



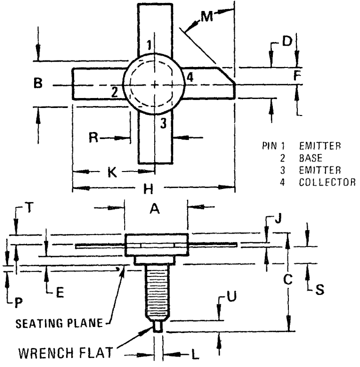
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CB}	36	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	0.25	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	3.5 0.02	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 50 mAdc, I_B = 0)	BV_{CEO}	18	–	Vdc
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 50 mAdc, V_{BE} = 0)	BV_{CES}	36	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, $T_A = 125^oC$)	I_{CES}	–	10	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	0.1	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	15	–	–
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (Note 2) (I_C = 50 mAdc, V_{CE} = 12 Vdc, f = 100 MHz)	f_T	400	–	MHz
Output Capacitance (V_{CB} = 12 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	8.0	pF
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 1.0 W, V_{CC} = 12.5 Vdc, I_C = 0.133 Adc, f = 470 MHz)	G_{PE}	7.0	–	dB
Collector Efficiency (P_{out} = 1.0 W, V_{CC} = 12.5 Vdc, I_C = 0.133 Adc, f = 470 MHz)	η	60	–	%

*Indicates JEDEC Registered Data.
Note 1: Pulsed through 25 mH inductor.
Note 2: f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.



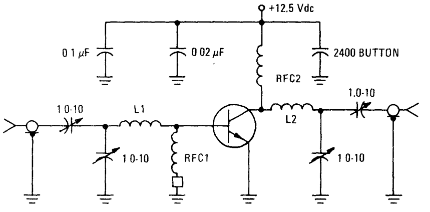
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	18.03	19.05	0.710	0.750
D	5.59	5.84	0.220	0.230
E	1.78	2.03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.40	1.65	0.055	0.065
M	45^0 NOM		45^0 NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130

NOTE·
CASE 145A-01 USE 8-32NC2A STUD

CASE 145A-01

DESIGN DATA

FIGURE 1 – 470 MHz TEST CIRCUIT



L1 = COPPER STRAP 1" Long, 5/32" Wide

L2 = 1 Turn #16 AWG WIRE, 3/32" I.D., Total Length
of Coil and Leads = 13/16"

RFC 1 = 0.15 µH MOLDED CHOKE with Ferrite Bead on Ground Lead

RFC 2 = 8 Turns #20 WIRE, 7/32" I.D., 3/8" Long

All Capacitance Values in pF Except As Noted

FIGURE 2 – POWER OUTPUT versus POWER INPUT

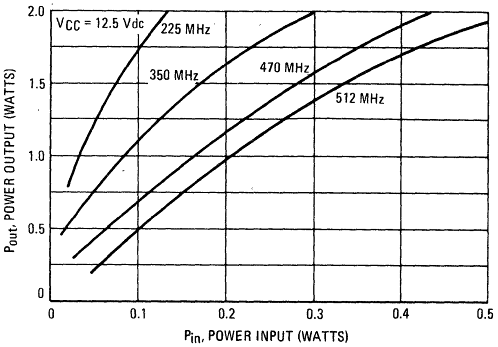


FIGURE 3 – POWER OUTPUT versus FREQUENCY

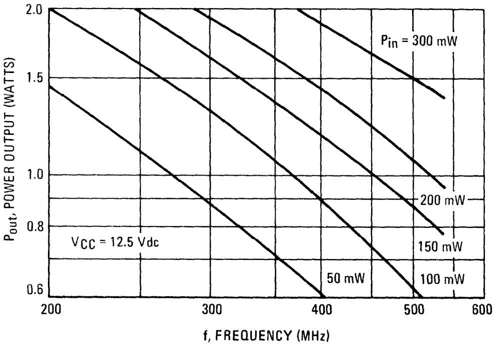


FIGURE 4 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

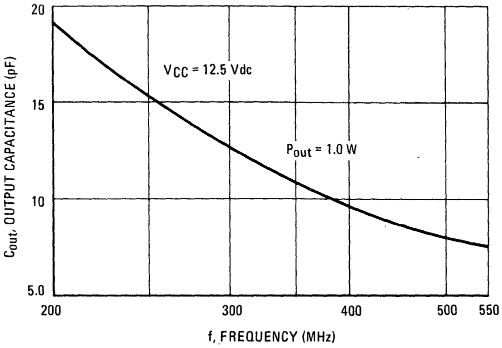


FIGURE 5 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

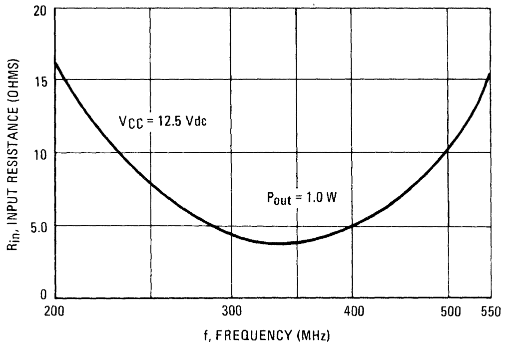
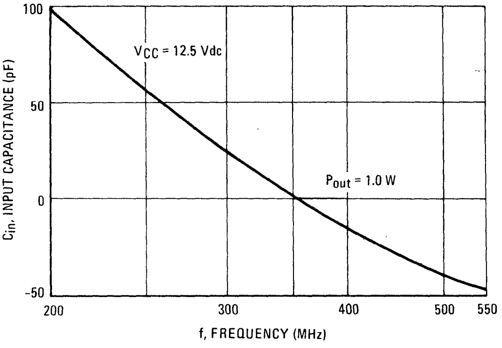


FIGURE 6 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY



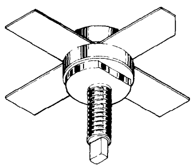
2N5645 (SILICON)

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt, UHF large signal amplifier applications required in industrial and consumer FM equipment operating to 520 MHz.

- Low lead inductance stripline package for ease of design and increased broadband capability
- Balanced Emitter Construction to protect against device damage due to load mismatch
- Specified 12.5 Volt, 470 MHz Characteristics –
  Output Power = 4.0 Watt
  Minimum Gain = 6.0 dB
  Efficiency = 60%

NPN SILICON
RF POWER
TRANSISTOR



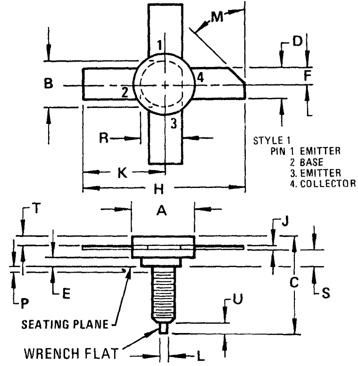
***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CB}	36	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25°C	P_D	12 0.068	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*** ELECTRICAL CHARACTERISTICS** ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (Note 1) ($I_C = 100$ mAdc, $I_B = 0$)	BV_{CEO}	18	–	Vdc
Collector-Emitter Breakdown Voltage (Note 1) ($I_C = 100$ mAdc, $V_{BE} = 0$)	BV_{CES}	36	–	Vdc
Emitter-Base Breakdown Voltage ($I_E = 1.0$ mAdc, $I_C = 0$)	BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current ($V_{CE} = 15$ Vdc, $V_{BE} = 0$, $T_A = 125^oC$)	I_{CES}	–	10	mAdc
Collector Cutoff Current ($V_{CB} = 15$ Vdc, $I_E = 0$)	I_{CBO}	–	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 0.5$ Adc, $V_{CE} = 5.0$ Vdc)	h_{FE}	15	–	–
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (Note 2) ($I_C = 100$ mAdc, $V_{CE} = 12$ Vdc, f = 100 MHz)	f_T	400	–	MHz
Output Capacitance ($V_{CB} = 12$ Vdc, $I_E = 0$, f = 1.0 MHz)	C_{ob}	–	20	pF
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (Figure 1) ($P_{out} = 4.0$ W, $V_{CC} = 12.5$ Vdc, $I_C = 0.53$ Adc, f = 470 MHz)	G_{PE}	6.0	–	dB
Collector Efficiency ($P_{out} = 4.0$ W, $V_{CC} = 12.5$ Vdc, $I_C = 0.53$ Adc, f = 470 MHz)	η	60	–	%

*Indicates JEDEC Registered Data.
Note 1: Pulsed through 25 mH inductor.
Note 2: f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	18.03	19.05	0.710	0.750
D	5.59	5.84	0.220	0.230
E	1.78	2.03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
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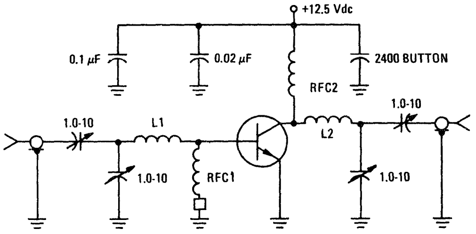
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130

NOTE
CASE 145A-01 USE 8-32NC2A STUD

CASE 145A-01

DESIGN DATA

FIGURE 1 – 470 MHz TEST CIRCUIT



L1 = COPPER STRAP 1" Long, 5/32" Wide

L2 = 1 Turn #16 AWG WIRE, 3/32" I.D., Total Length of Coil and Leads = 13/16"

RFC 1 = 0.15 μH MOLDED CHOKE with Ferrite Bead on Ground Lead

RFC 2 = 8 Turns #20 WIRE, 7/32" I.D., 3/8" Long

All Capacitance Values in pF Except As Noted.

FIGURE 2 – POWER OUTPUT versus POWER INPUT

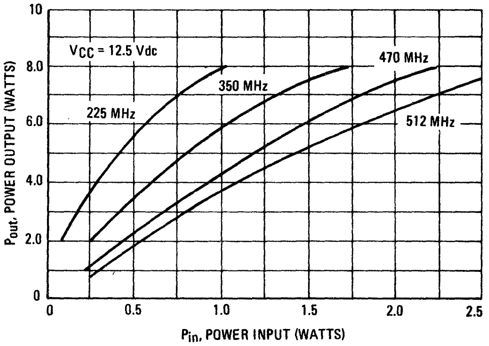


FIGURE 3 – POWER OUTPUT versus FREQUENCY

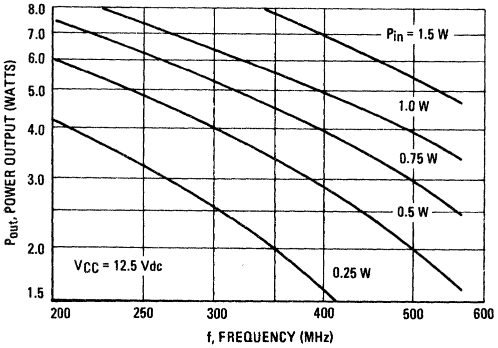


FIGURE 4 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

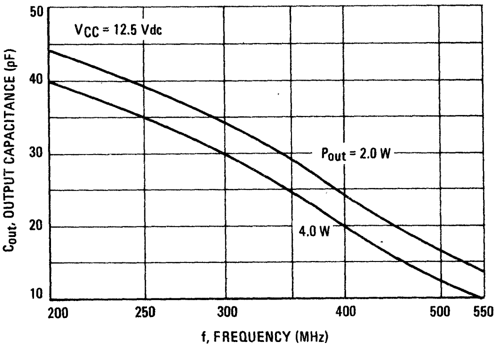


FIGURE 5 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

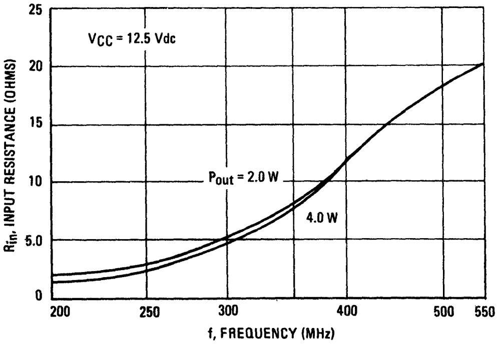
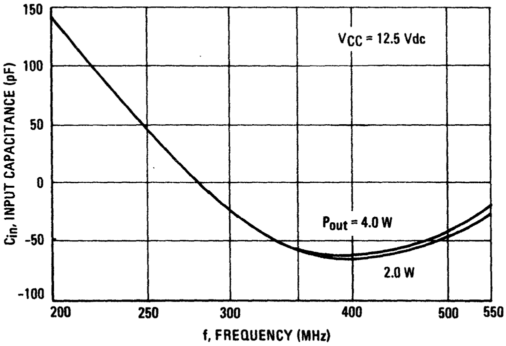


FIGURE 6 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY



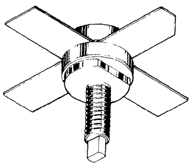
2N5646 (SILICON)

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt, UHF large signal amplifier applications required in industrial and consumer FM equipment operating to 520 MHz.

- Low lead inductance stripline package for ease of design and increased broadband capability
- Balanced Emitter Construction to protect against device damage due to load mismatch
- Specified 12.5 Volt, 470 MHz Characteristics –
  Output Power = 12 Watt
  Minimum Gain = 4.7 dB
  Efficiency = 60%

NPN SILICON
RF POWER
TRANSISTOR



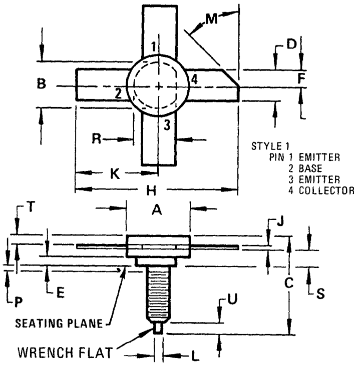
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CB}	36	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.171	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	BV_{CEO}	18	–	Vdc
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 200 mAdc, V_{BE} = 0)	BV_{CES}	36	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_A = 125°C)	I_{CES}	–	10	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	15	–	–
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (Note 2) (I_C = 250 mAdc, V_{CE} = 12 Vdc, f = 100 MHz)	f_T	400	–	MHz
Output Capacitance (V_{CB} = 12 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	40	pF
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 12 W, V_{CC} = 12.5 Vdc, I_C = 1.6 Adc, f = 470 MHz)	G_{PE}	4.7	–	dB
Collector Efficiency (P_{out} = 12 W, V_{CC} = 12.5 Vdc, I_C = 1.6 Adc, f = 470 MHz)	η	60	–	%

*Indicates JEDEC Registered Data.
Note 1: Pulsed through 25 mH inductor.
Note 2: f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.



STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

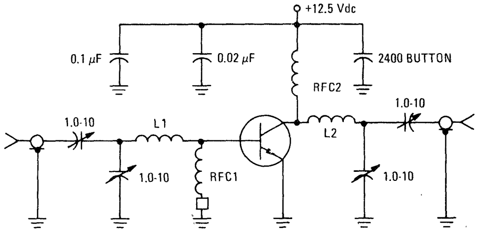
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	18.03	19.05	0.710	0.750
D	5.59	5.84	0.220	0.230
E	1.78	2.03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130

NOTE:
CASE 145A-01 USE 8-32NC2A STUD

CASE 145A-01

DESIGN DATA

FIGURE 1 – 470 MHz TEST CIRCUIT



L1 = COPPER STRAP 1″ Long, 5/32″ Wide

L2 = 1 Turn #16 AWG WIRE, 3/32″ I.D., Total Length of Coil and Leads = 13/16″

RFC 1 = 0.15 μH MOLDED CHOKE with Ferrite Bead on Ground Lead.

RFC 2 = 8 Turns #20 WIRE, 7/32″ I D., 3/8″ Long

All Capacitance Values in pF Except As Noted.

FIGURE 2 – POWER OUTPUT versus POWER INPUT

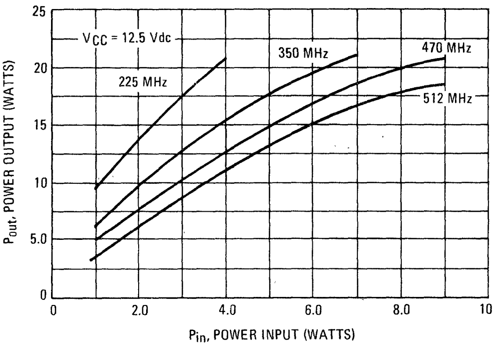


FIGURE 3 – POWER OUTPUT versus FREQUENCY

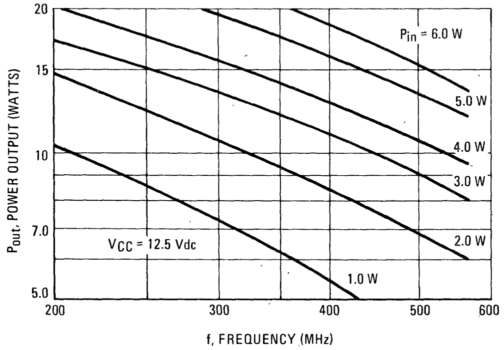


FIGURE 4 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

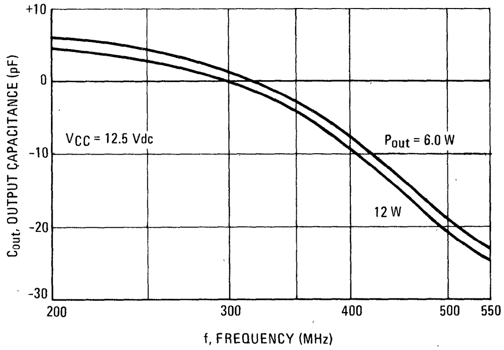


FIGURE 5 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

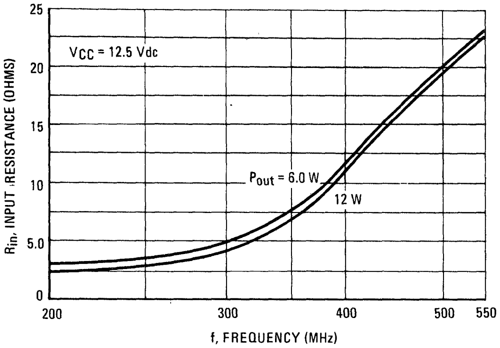
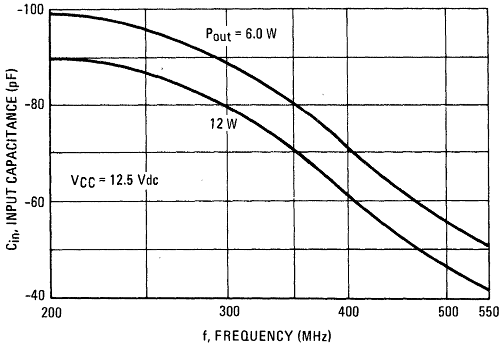


FIGURE 6 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY



2N5829 (SILICON)

For Specifications See 2N4957 Data, Volume I.

2N5653 (SILICON)
2N5654

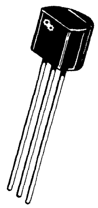
SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

Depletion Mode (Type A) Junction Field-Effect Transistors designed primarily for low-power, chopper and switching applications.

- Fast Switching Times – 2N5653
  $t_{d(on)}$ = 4.0 ns (Max)
  t_r = 5.0 ns (Max)
  $t_{d(off)}$ = 5.0 ns (Max)
  t_f = 10 ns (Max)
- Low Drain-Source "ON" Resistance –
  $r_{ds(on)}$ = 50 Ohms (Max) @ I_D = 1.0 mAdc - 2N5653
- Low Reverse Transfer Capacitance –
  C_{rss} = 3.5 pF (Max) @ V_{GS} = -12 Vdc

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

(Type A)

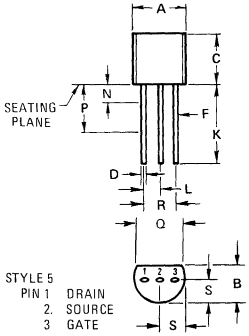


*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	30	Vdc
Reverse Gate-Source Voltage	V_{GSR}	30	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D (1)	310 2.82	mW mW/°C
Storage Temperature Range	T_{stg} (1)	-65 to +150	°C

*Indicates JEDEC Registered Data.

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125°C/W.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0 482	0.016	0.019
K	12.700	–	0.500	–
L	1 150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2 670	0.080	0.105

CASE 29-02
TO-92

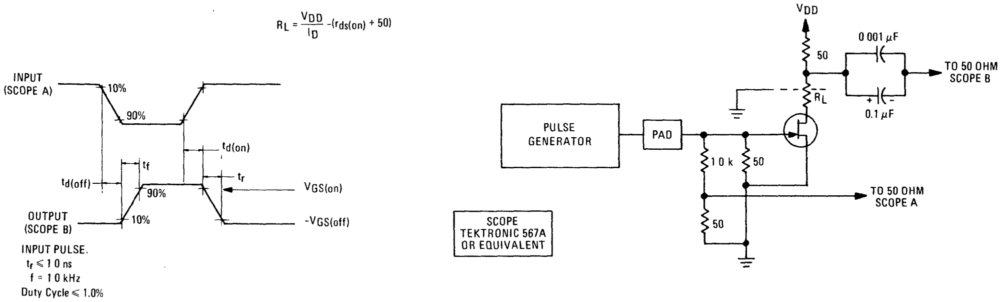
*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage	(I_G = 10 µAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	–	Vdc
Gate Reverse Current			I_{GSS}			
	(V_{GS} = -15 Vdc, V_{DS} = 0)			–	1.0	nAdc
	(V_{GS} = -15 Vdc, V_{DS} = 0, T_A = 100°C)			–	1.0	µAdc
Drain Cutoff Current			$I_{D(off)}$			
	(V_{DS} = 15 Vdc, V_{GS} = -12 Vdc)	2N5653		–	1.0	nAdc
	(V_{DS} = 15 Vdc, V_{GS} = -8.0 Vdc)	2N5654		–	1.0	
	(V_{DS} = 15 Vdc, V_{GS} = -12 Vdc, T_A = 100°C)	2N5653		–	1.0	µAdc
	(V_{DS} = 15 Vdc, V_{GS} = -8.0 Vdc, T_A = 100°C)	2N5654		–	1.0	
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (Note 1)			I_{DSS}			mAdc
	(V_{DS} = 20 Vdc, V_{GS} = 0)	2N5653		40	–	
		2N5654		15	–	
Drain-Source "ON" Voltage			$V_{DS(on)}$			Vdc
	(I_D = 10 mAdc, V_{GS} = 0)	2N5653		–	0.75	
	(I_D = 5.0 mAdc, V_{GS} = 0)	2N5654		–	0.75	
SMALL-SIGNAL CHARACTERISTICS						
Static Drain-Source "ON" Resistance			$r_{ds(on)}$			Ohms
	(V_{GS} = 0, I_D = 1.0 mAdc)	2N5653		–	50	
		2N5654		–	100	
	(V_{GS} = 0, I_D = 0, f = 1.0 kHz)	2N5653		–	50	
		2N5654		–	100	
Input Capacitance	(V_{DS} = 0, V_{GS} = -12 Vdc, f = 1.0 MHz)		C_{iss}	–	10	pF
Reverse Transfer Capacitance	(V_{DS} = 0, V_{GS} = -12 Vdc, f = 1.0 MHz)		C_{rss}	–	3.5	pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	Test Condition for 2N5653:					
	(V_{DD} = 10 Vdc, $V_{GS(on)}$ = 0,	2N5653	$t_{d(on)}$	–	4.0	ns
	$V_{GS(off)}$ = -12 Vdc,	2N5654		–	6.0	
Rise Time	$I_{D(on)}$ = 10 mAdc,	2N5653	t_r	–	5.0	ns
	R_G' = 50 Ohms)	2N5654		–	8.0	
Turn-Off Delay Time	Test Condition for 2N5654:					
	(V_{DD} = 10 Vdc, $V_{GS(on)}$ = 0,	2N5653	$t_{d(off)}$	–	5.0	ns
	$V_{GS(off)}$ = -12 Vdc,	2N5654		–	10	
Fall Time	$I_{D(on)}$ = 5.0 mAdc,	2N5653	t_f	–	10	ns
	R_G' = 50 Ohms)	2N5654		–	20	
	(Figure 1)					

*Indicates JEDEC Registered Data.

Note 1: Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 3.0%.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



$$R_L = \frac{V_{DD}}{I_D} - (r_{ds(on)} + 50)$$

2N5655 2N5656 2N5657 (SILICON)
MJE5655 MJE5656 MJE5657

PLASTIC NPN SILICON HIGH-VOLTAGE POWER TRANSISTORS

. . . designed for use in line-operated equipment such as audio output amplifiers; low-current, high-voltage converters; and AC line relays

- Excellent DC Current Gain – h_{FE} = 30-250 @ I_C = 100 mAdc
- Current-Gain – Bandwidth Product –
  f_T = 10 MHz (Min) @ I_C = 50 mAdc
- Packaged in Thermopad Case for Low Cost
- Choice of Packages – 2N5655, 2N5656, 2N5657 – Case 77
  MJE5655, MJE5656, MJE5657 – Case 199

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON

250-300-350 VOLTS
20 and 30 WATTS

*MAXIMUM RATINGS

Rating	Symbol	2N5655 MJE5655	2N5656 MJE5656	2N5657 MJE5657	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	325	375	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 0.5 → ← 1.0 →			Adc
Base Current	I_B	← 0.25 →			Adc
		2N5655 Series		MJE5655 Series	
Total Device Dissipation @ $T_C = 25^{\circ}C$ Derate above 25°C	P_D	20 0.16		30 0.24	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N5655 Series	MJE5655 Series	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	4.167	°C/W

*Indicates JEDEC Registered Data for 2N5655 Series.

FIGURE 1 – POWER DERATING

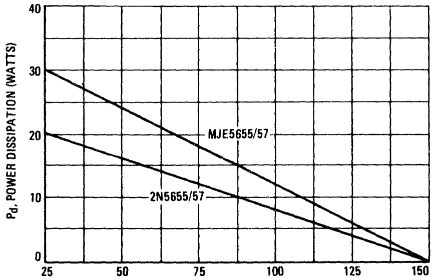
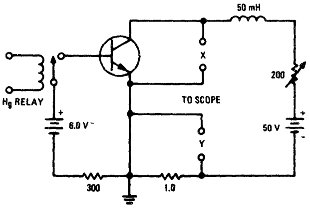
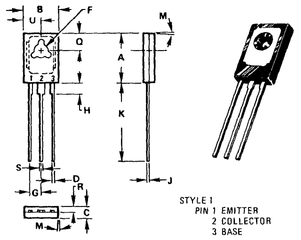


FIGURE 2 – SUSTAINING VOLTAGE TEST CIRCUIT



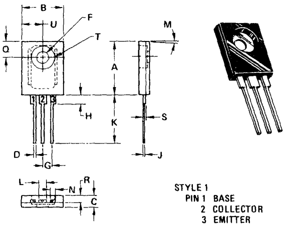


STYLE 1
PIN 1 EMITTER
2 COLLECTOR
3 BASE

2N5655
2N5656
2N5657

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.36 BSC		0.093 BSC	
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.38	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155

CASE 77-03



STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER

MJE5655
MJE5656
MJE5657

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0.152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

CASE 199-04

Safe Area Limits are indicated by Figures 3 and 4. Both limits are applicable and must be observed.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc (inductive), L = 50 mH)	2N5655, MJE5655	$V_{CEO(sus)}$	250	–	Vdc
	2N5656, MJE5656		300	–	
	2N5657, MJE5657		350	–	
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	2N5655, MJE5655	BV_{CEO}	250	–	Vdc
	2N5656, MJE5656		300	–	
	2N5657, MJE5657		350	–	
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	2N5655, MJE5655	I_{CEO}	–	0.1	mAdc
(V_{CE} = 200 Vdc, I_B = 0)	2N5656, MJE5656		–	0.1	
(V_{CE} = 250 Vdc, I_B = 0)	2N5657, MJE5657		–	0.1	
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5655, MJE5655	I_{CEX}	–	0.1	mAdc
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5656, MJE5656		–	0.1	
(V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5657, MJE5657		–	0.1	
(V_{CE} = 150 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5655, MJE5655		–	1.0	
(V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5656, MJE5656		–	1.0	
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5657, MJE5657		–	1.0	
Collector Cutoff Current (V_{CB} = 275 Vdc, I_E = 0)	2N5655, MJE5655	I_{CBO}	–	10	μAdc
(V_{CB} = 325 Vdc, I_E = 0)	2N5656, MJE5656		–	10	
(V_{CB} = 375 Vdc, I_E = 0)	2N5657, MJE5657		–	10	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}		10	μAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 10 Vdc)		h_{FE}	25	–	–
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			30	250	
(I_C = 250 mAdc, V_{CE} = 10 Vdc)			15	–	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage (1) (I_C = 100 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 250 mAdc, I_B = 25 mAdc)			–	2.5	
(I_C = 500 mAdc, I_B = 100 mAdc)			–	10	
Base-Emitter Voltage (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc)		V_{BE}	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	10	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	25	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data for 2N5655 Series

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity

ACTIVE-REGION SAFE OPERATING AREA

FIGURE 3 – 2N5655, 2N5656, 2N5657

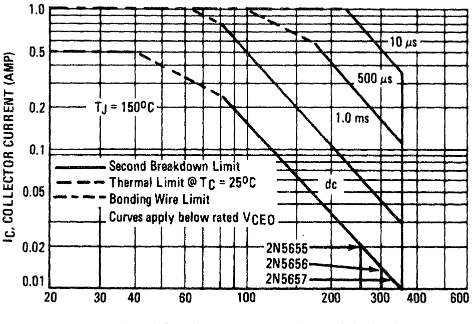
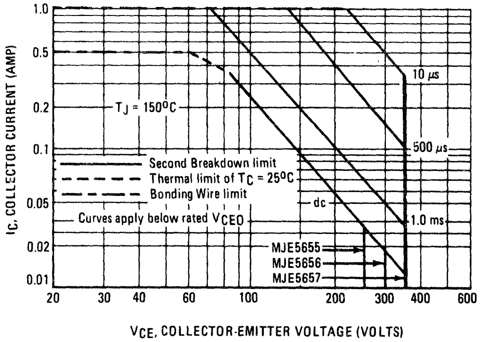


FIGURE 4 – MJE5655, MJE5656, MJE5657



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

LARGE SIGNAL CHARACTERISTICS

FIGURE 5 – TRANSCONDUCTANCE

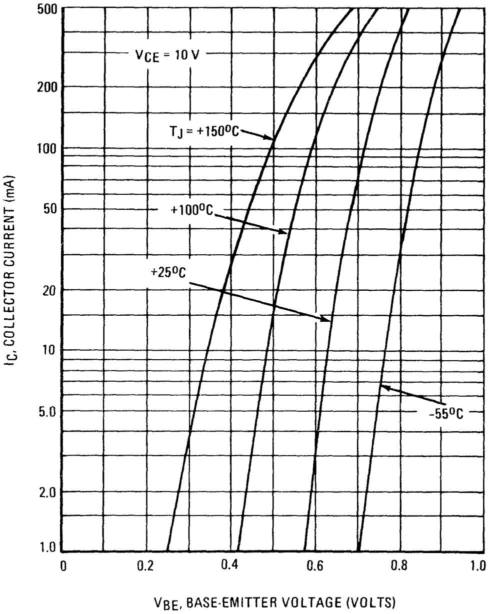
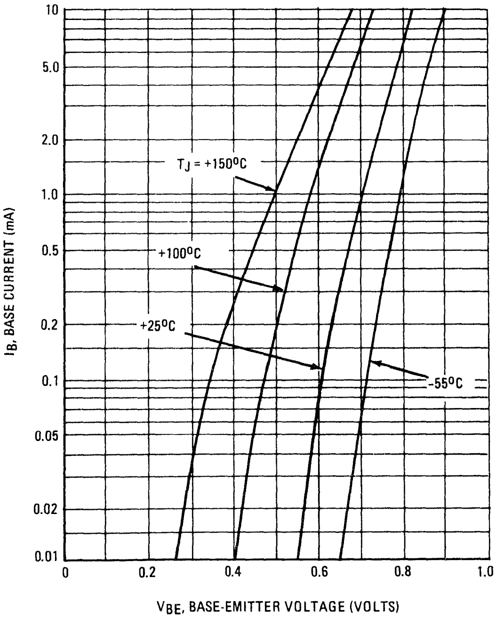


FIGURE 7 – INPUT ADMITTANCE



CUT-OFF CHARACTERISTICS

FIGURE 6 – TRANSCONDUCTANCE

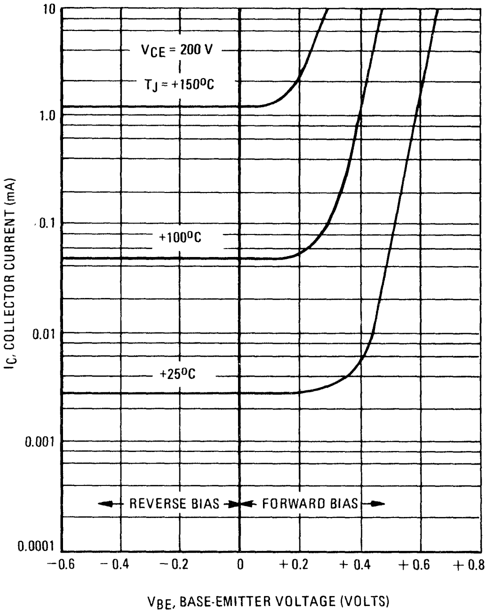


FIGURE 8 – EFFECT OF BASE-EMITTER RESISTANCE

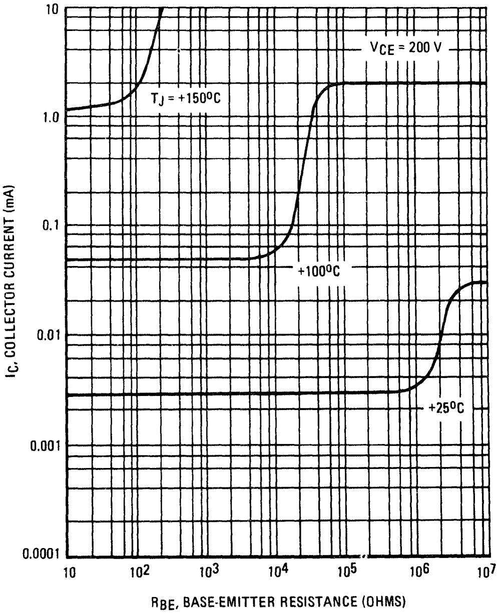


FIGURE 9 – CURRENT GAIN

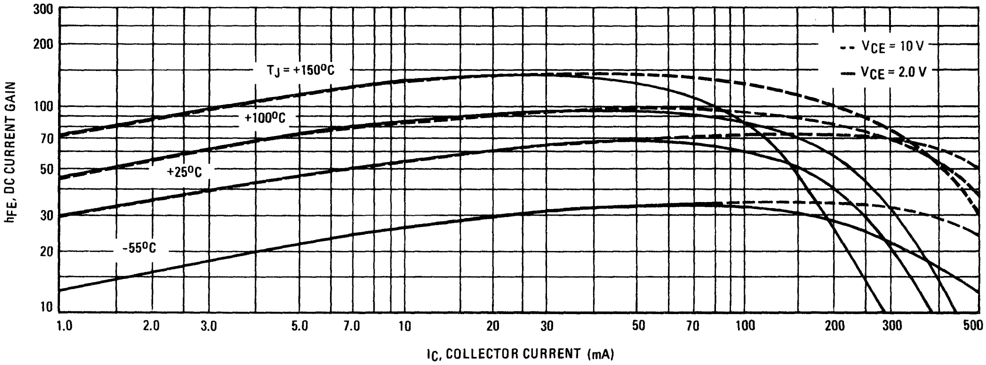


FIGURE 10 – "ON" VOLTAGES

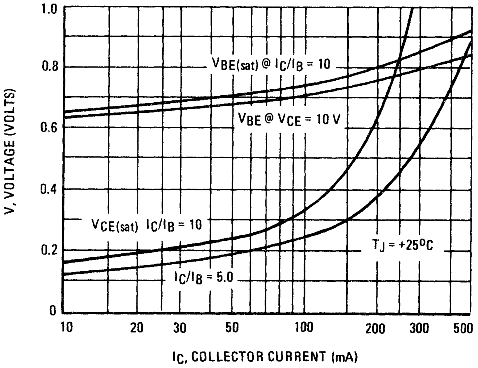


FIGURE 11 – CAPACITANCE

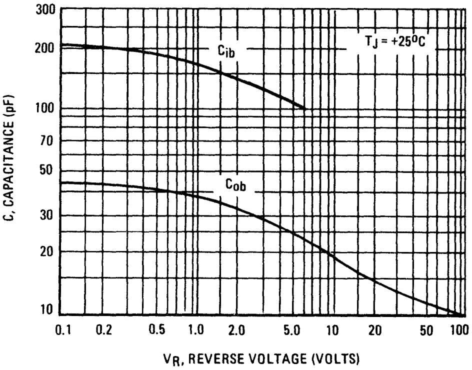


FIGURE 12 – TURN-ON TIME

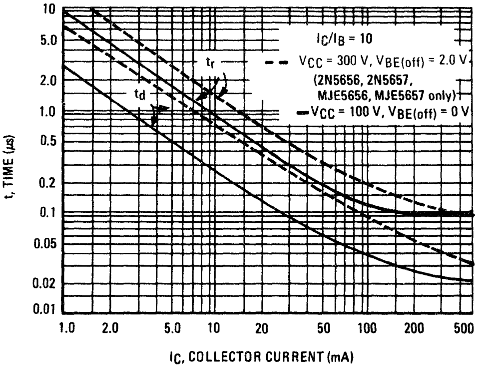
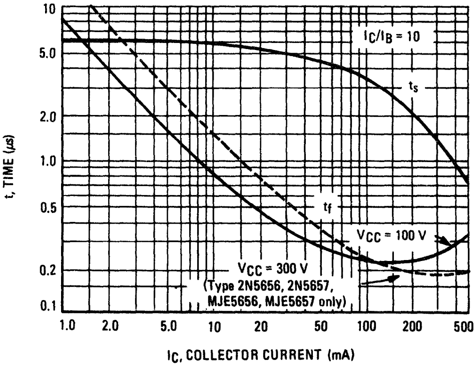


FIGURE 13 – TURN-OFF TIME



2N5668 (SILICON)
2N5669
2N5670

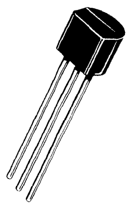
SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

Depletion Mode (Type A) Junction Field-Effect Transistors designed for VHF amplifier and mixer applications.

- Low Cross Modulation and Intermodulation Distortion
- Drain and Source Interchangeable
- Low 100-MHz Noise Figure –
  NF = 2.5 dB (Max)
- Low Reverse Transfer and Input Capcitances –
  C_{rss} = 1.0 pF (Typ); C_{iss} = 4.7 pF (Typ)
- High Maximum Stable Gain Due to Drain and Gate Lead Separation

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

(Type A)

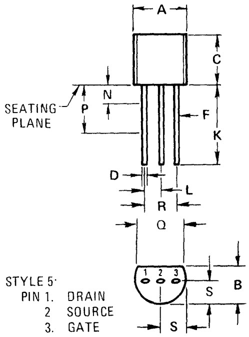


*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
*Drain-Gate Voltage	V_{DG}	25	Vdc
*Reverse Gate-Source Voltage	V_{GSR}	25	Vdc
*Forward Gate Current	I_{GF}	10	mAdc
Drain Current	I_D	20	mAdc
*Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D (1)	310 2.82	mW mW/°C
*Storage Temperature Range	T_{stg} (1)	-65 to +150	°C

*Indicates JEDEC Registered Data.

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125°C/W.



STYLE 5:
PIN 1. DRAIN
2 SOURCE
3. GATE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4 450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0 170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

2N5668, 2N5669, 2N5670 (continued)

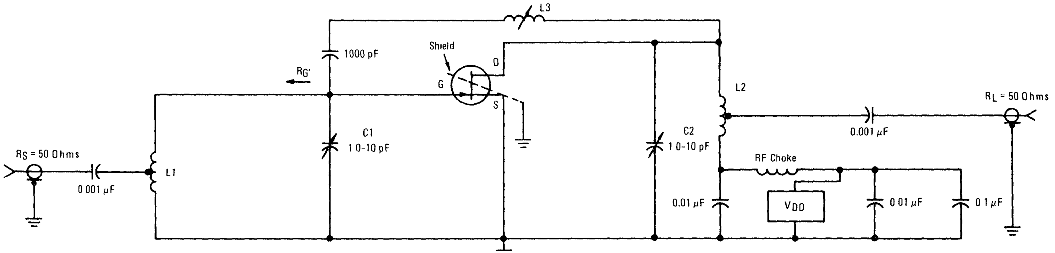
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**						
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	25	–	–	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5668	$V_{GS(off)}$	0.2	–	4.0	Vdc
	2N5669		1.0	–	6.0	
	2N5670		2.0	–	8.0	
Gate Reverse Current		I_{GSS}				
(V_{GS} = −15 Vdc, V_{DS} = 0)			–	–	2.0	nAdc
(V_{GS} = −15 Vdc, V_{DS} = 0, T_A = 100°C)			–	–	2.0	μAdc
***ON CHARACTERISTICS**						
Zero-Gate Voltage Drain Current (Note 1) (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5668	I_{DSS}	1.0	–	5.0	mAdc
	2N5669		4.0	–	10	
	2N5670		8.0	–	20	
SMALL-SIGNAL CHARACTERISTICS						
*Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5668	$\lvert y_{fs} \rvert$	1500	–	6500	μmhos
	2N5669		2000	–	6500	
	2N5670		3000	–	7500	
*Forward Transconductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5668	$Re(y_{fs})$	1000	–	–	μmhos
	2N5669		1600	–	–	
	2N5670		2500	–	–	
*Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5668	$\lvert y_{os} \rvert$	–	–	20	μmhos
	2N5669		–	–	50	
	2N5670		–	–	75	
*Output Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5668	$Re(y_{os})$	–	10	50	μmhos
	2N5669		–	25	100	
	2N5670		–	35	150	
*Input Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)		$Re(y_{is})$	–	125	800	μmhos
*Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	4.7	7.0	pF
*Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.0	3.0	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	–	1.4	4.0	pF
*Common Source Noise Figure (Figure 1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz, at $R_{G'}$ = 1.0 k ohm)		NF	–	–	2.5	dB
Power Gain (Figure 1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)		G_{ps}	16	–	–	dB

*Indicates JEDEC Registered Data, excluding typical values.

Note 1: Pulse Test: Pulse With = 100 ms, Duty Cycle ≤ 10%.

FIGURE 1 — 100 MHz, POWER GAIN AND NOISE FIGURE TEST CIRCUIT



L1 ≈ 8.5 Turns of #14 AWG Tinned Copper, Dia ≈ 3/8", ≈ 0.9" Long
Tapped at ≈ 2-1/2 Turns (adjust to give R_G = 1.0 k ohm),
Parallel Resistance = 40 k ohms, tunes at ≈ 8.0 pF

L2 ≈ 13.5 Turns #16 AWG Tinned Copper, Dia ≈ 3/8", ≈ 1.2" Long
Tapped at ≈ 5 Turns, Parallel Resistance = 40 k ohms,
tunes at ≈ 4.0 pF

L3 ≈ 17 Turns of #28 AWG Enameled
Copper Wire, Close Wound on 9/32"
Ceramic Form, Tuning Provided by a
Powdered Iron Slug

2N5679, 2N5680 PNP (SILICON)
2N5681, 2N5682 NPN

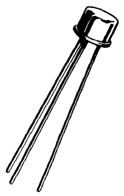
LOW-POWER COMPLEMENTARY SILICON TRANSISTORS

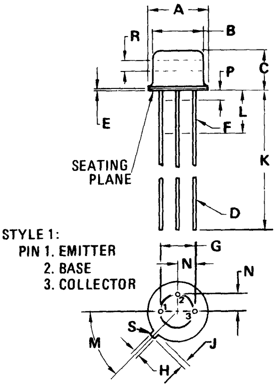
. . . designed for use as a driver for high-power transistors in general-purpose amplifier and switching circuit applications.

- High Current-Gain—Bandwidth Product — f_T = 30 MHz (Min) @ I_C = 100 mAdc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 0.25 Adc
- DC Current Gain Bracketed at 0.25 Adc — h_{FE} = 40 (Min) and 150 (Max)

1 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS

100-120 VOLTS
10 WATTS





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.711	0.864	0.028	0.034
J	0.734	1.14	0.029	0.045
K	38.10	–	1.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	
P	–	1.27	–	0.050
R	2.54	–	0.100	–
S	–	0.179	–	0.007

All JEDEC dimensions and notes apply.

CASE 31-03
TO-5

*MAXIMUM RATINGS

Rating	Symbol	2N5679 2N5681	2N5680 2N5682	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	Vdc
Collector-Base Voltage	V_{CB}	100	120	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current — Continuous	I_C	1.0		Adc
Base Current	I_B	0.5		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 5.7		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 57		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	17.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	175	°C/W

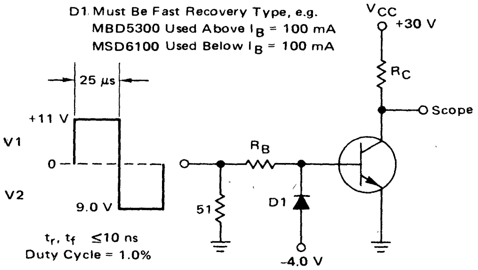
*Indicates JEDEC Registered Data.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	 2N5679, 2N5681 2N5680, 2N5682	$V_{CEO(sus)}$	 100 120	 – –	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)		I_{CEO}	 – –	 10 10	μAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 120 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 120 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N5679, 2N5681 2N5680, 2N5682 2N5679, 2N5681 2N5680, 2N5682	I_{CEX}	 – – – –	 1.0 1.0 1.0 1.0	 μAdc mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 120 Vdc, I_E = 0)	 2N5679, 2N5681 2N5680, 2N5682	I_{CBO}	 – –	 1.0 1.0	μAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 2.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	 40 5.0	 150 –	–
Collector-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 25 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	 – – –	 0.6 1.0 2.0	Vdc
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz		f_T	30	–	–
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	50	pF
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 1.5 Vdc, f = 1.0 kHz)		h_{fe}	40	–	–

*Indicates JEDEC Registered Data.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT



D1 Must Be Fast Recovery Type, e.g.
MBD5300 Used Above I_B = 100 mA
MSD6100 Used Below I_B = 100 mA

t_r, t_f ≤10 ns
Duty Cycle = 1.0%

R_B and R_C Varied to Obtain Desired Current Levels

For t_d and t_r, D1 is disconnected and V2 = 0
For PNP test circuit, reverse diode and voltage polarities.

PNP
2N5679, 2N5680

NPN
2N5681, 2N5682

FIGURE 2 — TURN-ON TIME

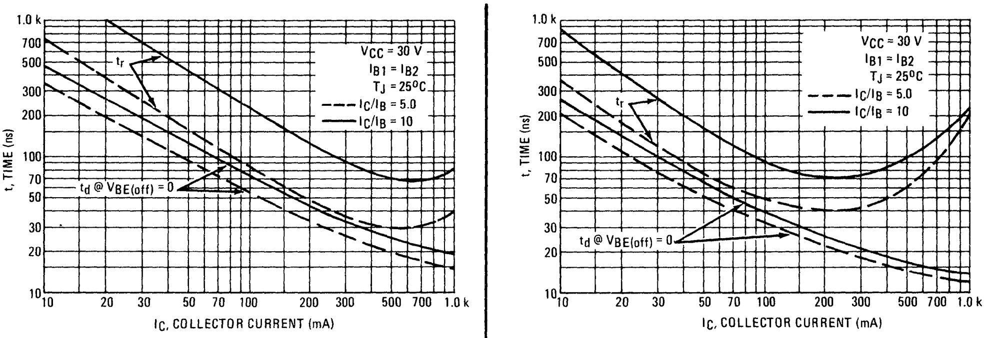


FIGURE 3 — TURN-OFF TIME

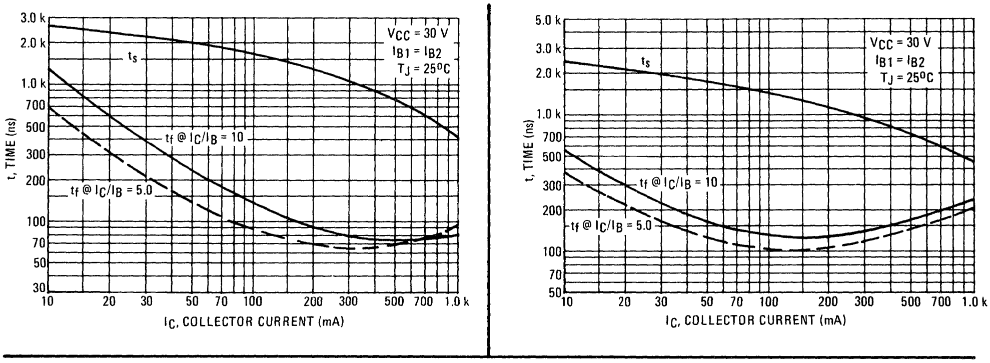


FIGURE 4 — CURRENT-GAIN — BANDWIDTH PRODUCT

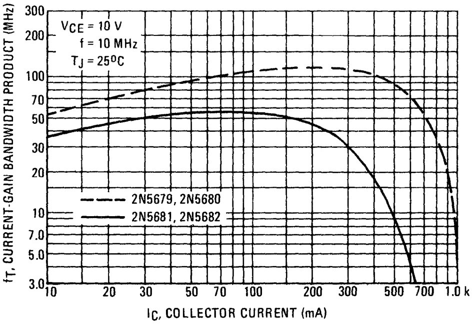


FIGURE 5 — CAPACITANCE

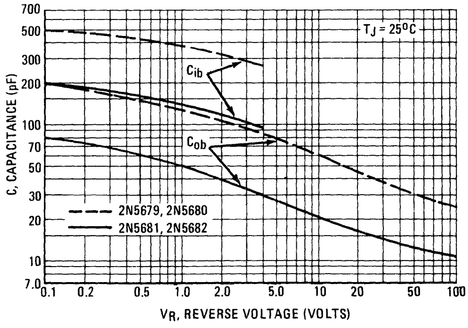


FIGURE 6 – THERMAL RESISTANCE

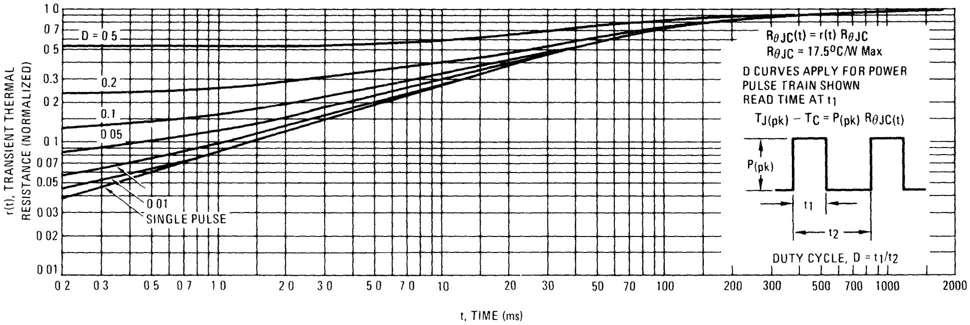


FIGURE 7 – ACTIVE-REGION SAFE OPERATING AREA

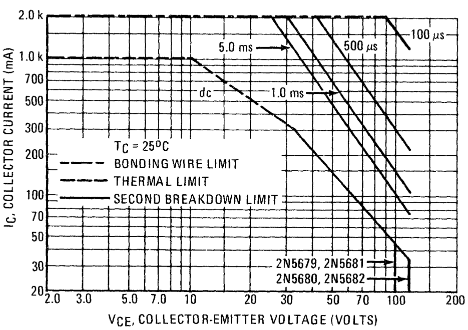
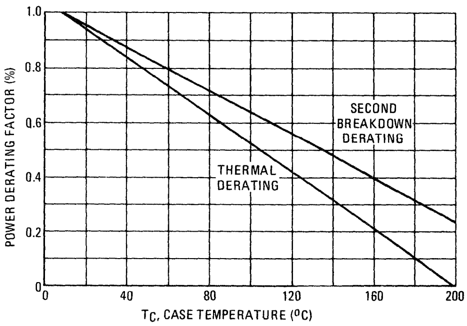


FIGURE 8 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 8.

PNP
2N5679, 2N5680

NPN
2N5681, 2N5682

FIGURE 9 – DC CURRENT GAIN

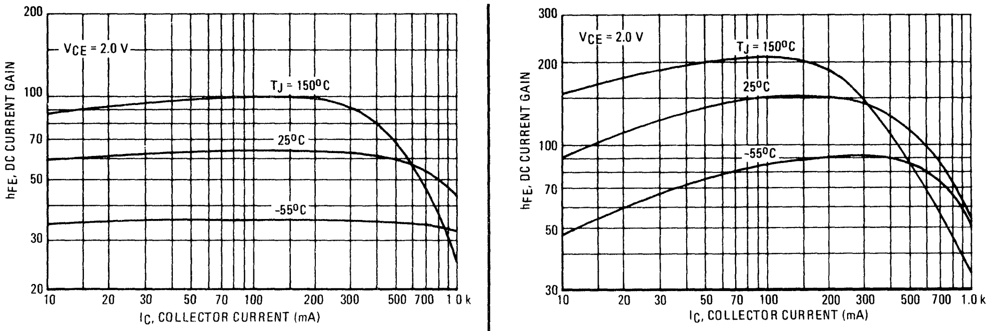


FIGURE 10 – COLLECTOR SATURATION REGION

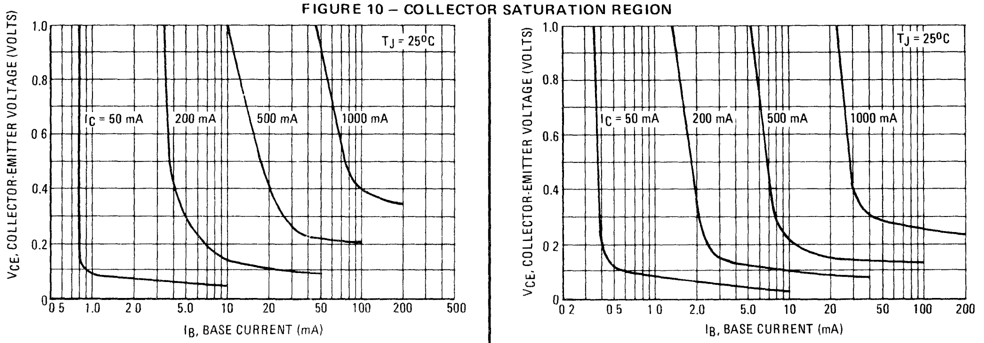
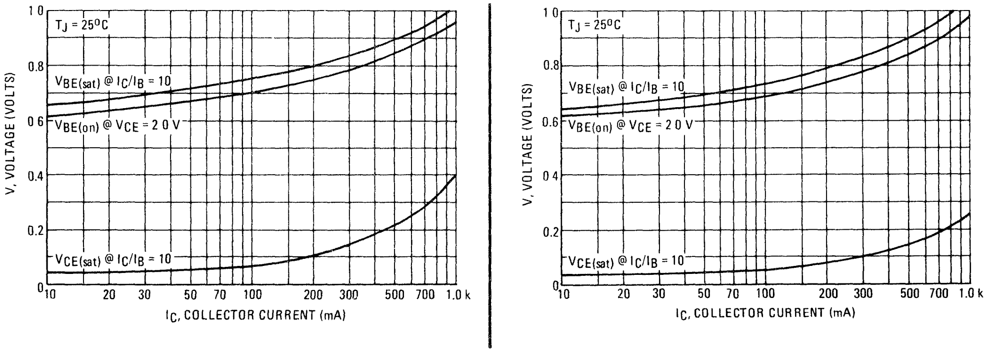


FIGURE 11 – "ON" VOLTAGES



PNP
2N5679, 2N5680

NPN
2N5681, 2N5682

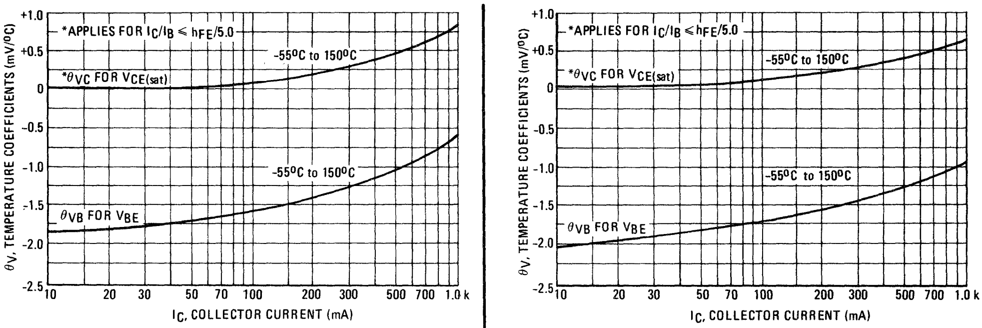


FIGURE 12 – TEMPERATURE COEFFICIENTS

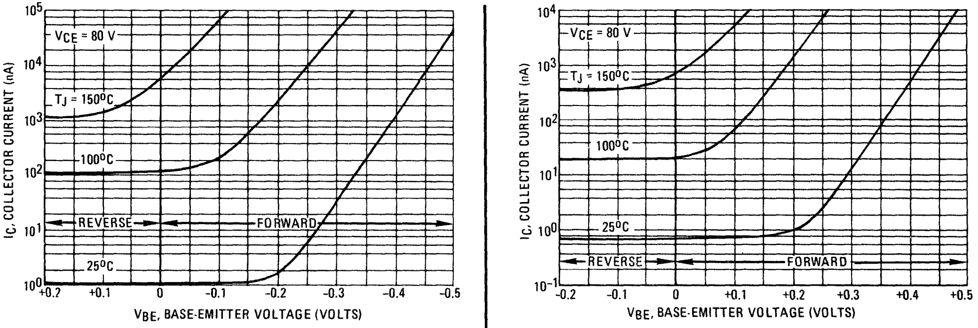


FIGURE 13 – COLLECTOR CUTOFF REGION

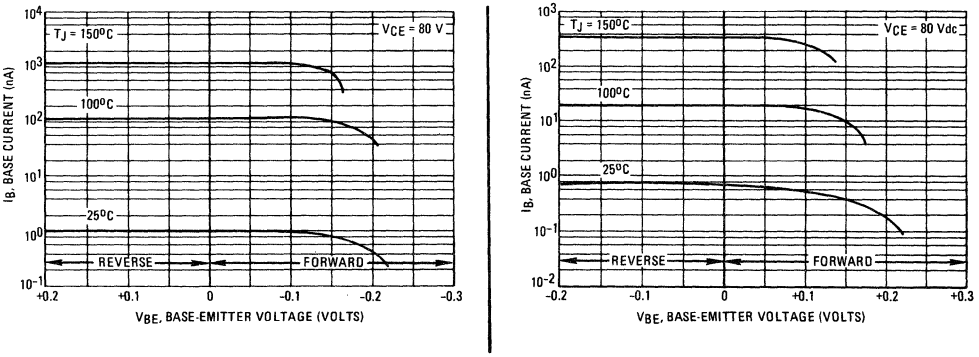


FIGURE 14 – BASE CUTOFF REGION

2N5683, 2N5684 PNP (SILICON)
2N5685, 2N5686 NPN

HIGH-CURRENT COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for use in high-power amplifier and switching circuit applications.

- High Current Capability – I_C Continuous = 50 Amperes.
- DC Current Gain –
  h_{FE} = 15 - 60 @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 25 Adc

*MAXIMUM RATINGS

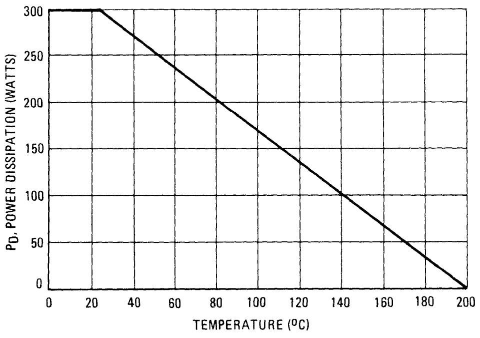
Rating	Symbol	2N5683 2N5685	2N5684 2N5686	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	50		Adc
Base Current	I_B	15		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.715		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.584	°C/W

*Indicates JEDEC Registered Data.

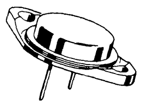
FIGURE 1 – POWER DERATING

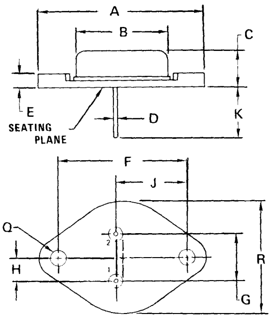


Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

50 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60–80 VOLTS
300 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

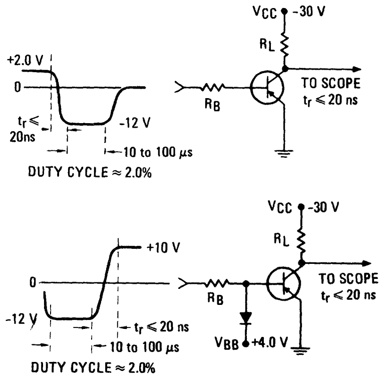
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Note 1)		$V_{CEO(sus)}$			Vdc
(I_C = 0.2 Adc, I_B = 0)	2N5683, 2N5685		60	–	
	2N5684, 2N5686		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5683, 2N5685		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5684, 2N5686		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5683, 2N5685		–	2.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5684, 2N5686		–	2.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5683, 2N5685		–	10	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5684, 2N5686		–	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5683, 2N5685		–	2.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5684, 2N5686		–	2.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1)		h_{FE}			–
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			15	60	
(I_C = 50 Adc, V_{CE} = 5.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage (Note 1)		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			–	1.0	
(I_C = 50 Adc, I_B = 10 Adc)			–	5.0	
Base-Emitter Saturation Voltage (Note 1) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage (Note 1) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 5.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz
Output Capacitance	2N5683, 2N5684	C_{ob}	–	2000	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5685, 2N5686		–	1200	
Small-Signal Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	15	–	

*Indicates JEDEC Registered Data

Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

FIGURE 3 – TURN-ON TIME

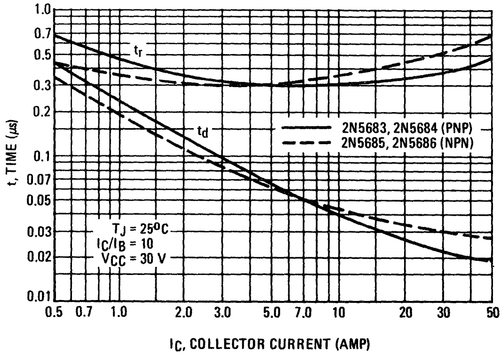


FIGURE 4 – THERMAL RESPONSE

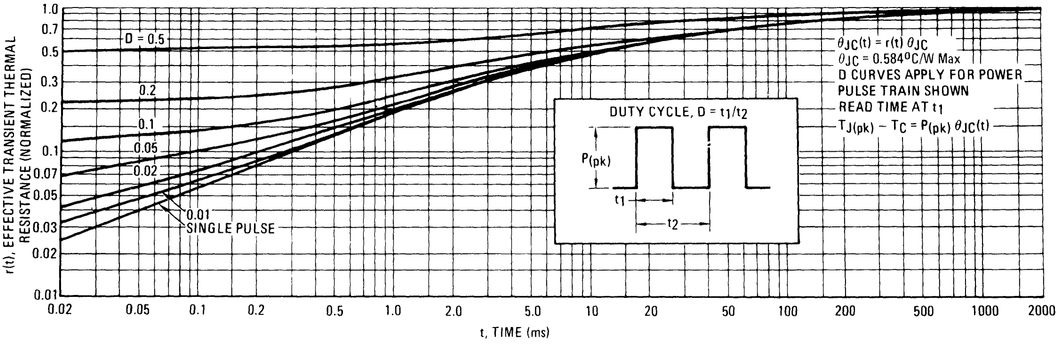
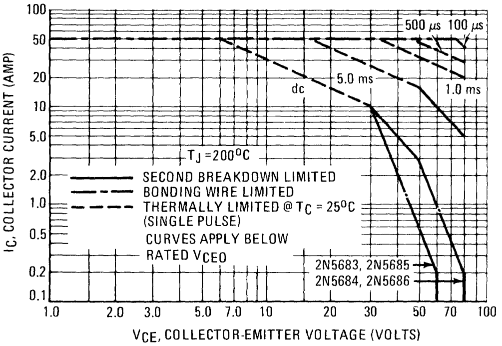


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

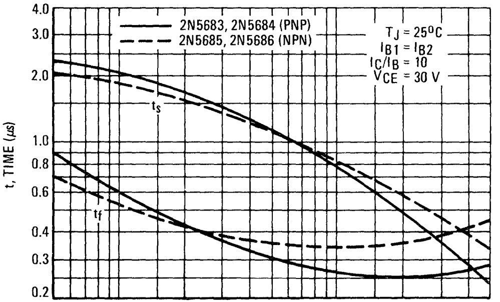
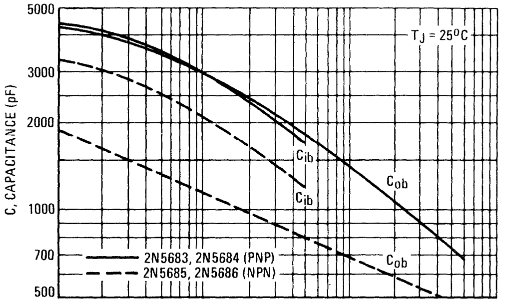


FIGURE 7 – CAPACITANCE



PNP
2N5683, 2N5684

NPN
2N5685, 2N5686

FIGURE 8 – DC CURRENT GAIN

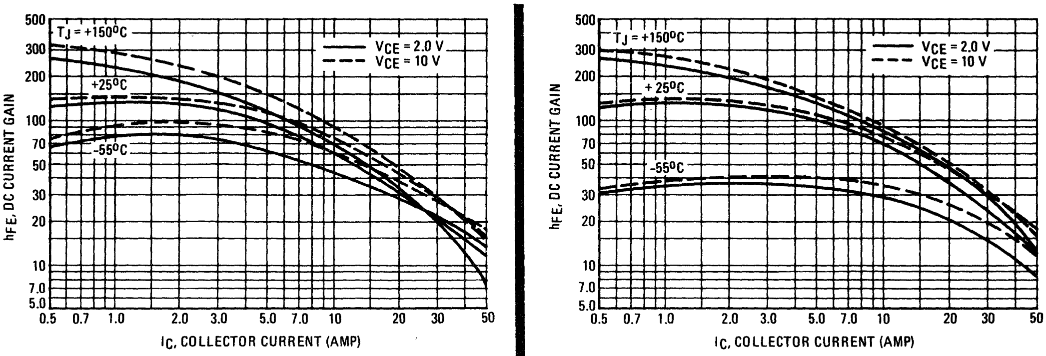


FIGURE 9 – COLLECTOR SATURATION REGION

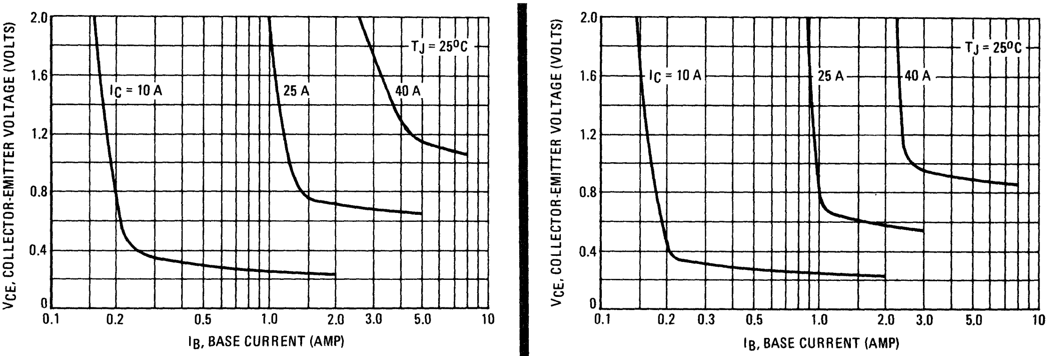
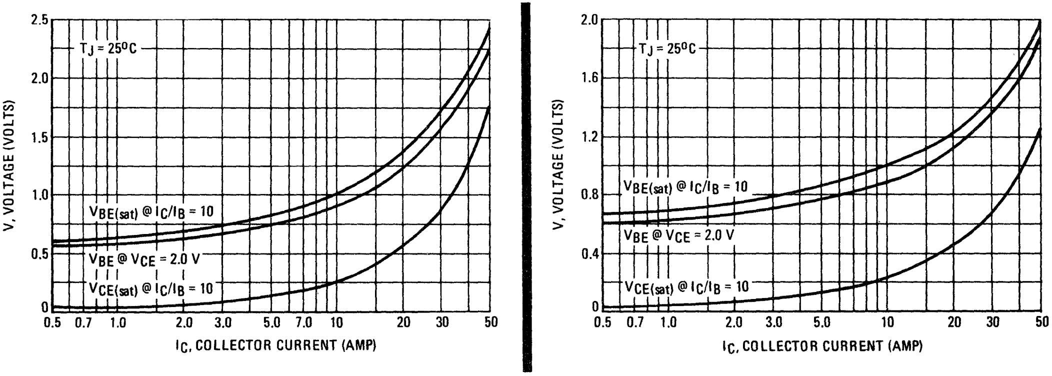


FIGURE 10 – "ON" VOLTAGES



PNP
2N5683, 2N5684

NPN
2N5685, 2N5686

FIGURE 11 – TEMPERATURE COEFFICIENTS

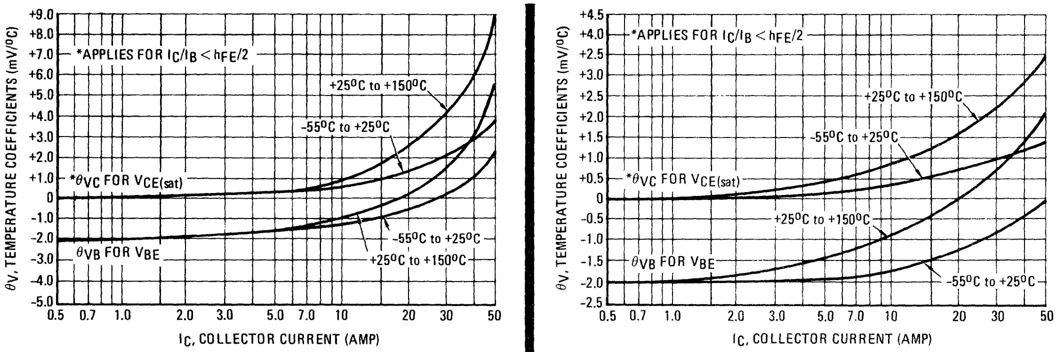


FIGURE 12 – COLLECTOR CUTOFF REGION

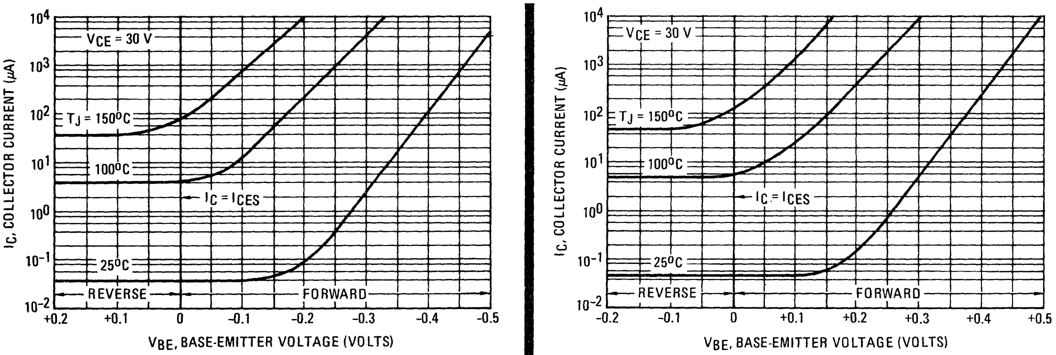
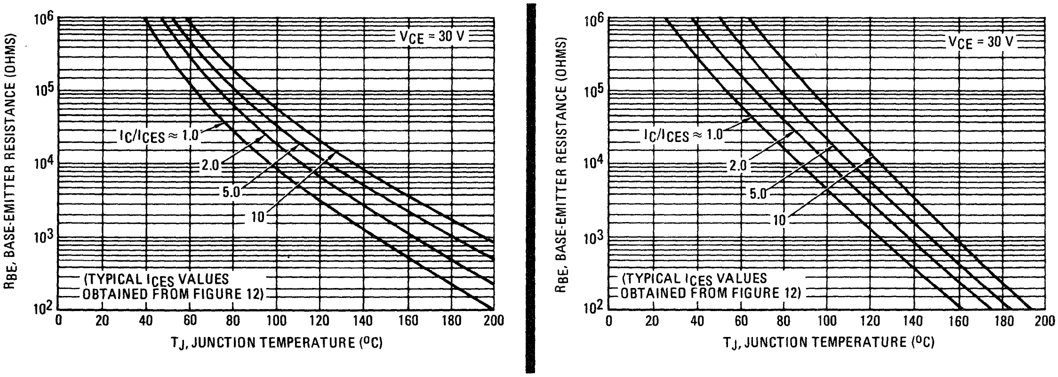


FIGURE 13 – EFFECT OF EXTERNAL BASE-EMITTER RESISTANCE

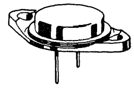


2N5692 thru 2N5696 (GERMANIUM)

PNP GERMANIUM POWER SWITCHING TRANSISTORS

. . . designed for high-current, fast-switching applications requiring low saturation voltage and excellent safe operating area.

40 AMPERE "ADE"
POWER TRANSISTORS
PNP GERMANIUM
50-140 VOLTS
120 WATTS



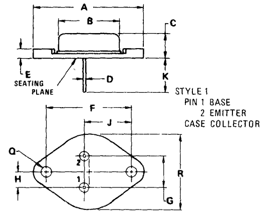
MAXIMUM RATINGS

Rating	Symbol	2N5692	2N5693	2N5694	2N5695	2N5696	Unit
*Collector-Emitter Voltage	V_{CEO}	30	60	80	100	120	Vdc
*Collector-Base Voltage	V_{CB}	50	80	100	120	140	Vdc
*Emitter-Base Voltage	V_{EB}	← 2.5 →					Vdc
*Collector Current — Continuous — Peak	I_C	← 40 → ← 60 →					Adc
*Base Current — Continuous	I_B	← 12 →					Adc
*Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 120 → ← 1.43 →					Watts W/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +110 →					°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

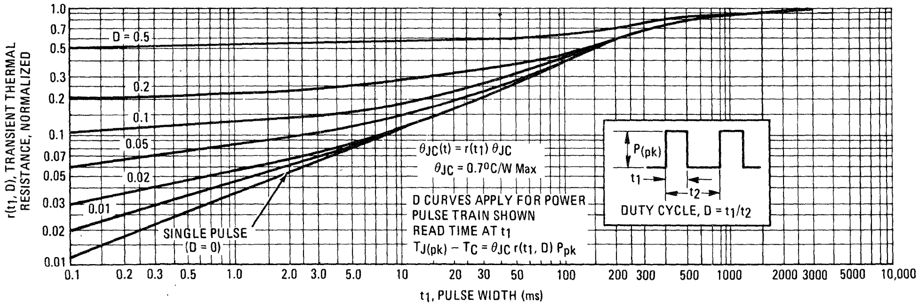
*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39 37	–	1 550
B	–	21 08	–	0 830
C	–	9 14	–	0 360
D	1 52	1 65	0.060	0 065
E	–	3 43	–	0.135
F	29.90	30.40	1.177	1 197
G	10 67	11 18	0 420	0 440
H	5 33	5 59	0 210	0 220
J	16.64	17 15	0 655	0 675
K	15 49	18 03	0 610	0 710
Q	3 84	4 09	0 151	0 161
R	–	26 67	–	1 050

CASE 3-04

FIGURE 1 — THERMAL RESPONSE



$\theta_{JC}(t) = r(t_1)\,\theta_{JC}$
θ_{JC} = 0.7°C/W Max

D CURVES APPLY FOR POWER PULSE TRAIN SHOWN
READ TIME AT t_1
$T_{J(pk)} - T_C = \theta_{JC}\, r(t_1, D)\, P_{pk}$

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
* Collector-Emitter Breakdown Voltage (I_C = 0.1 Adc, I_B = 0)	2N5692	BV_{CEO}	30	–	Vdc
	2N5693		60	–	
	2N5694		80	–	
	2N5695		100	–	
	2N5696		120	–	
* Collector Cutoff Current (V_{CE} = 50 Vdc) $V_{BE(off)}$ = 0.2 Vdc For All Types	2N5692	I_{CEX1}	–	10	mAdc
(V_{CE} = 80 Vdc)	2N5693		–	10	
(V_{CE} = 100 Vdc)	2N5694		–	10	
(V_{CE} = 120 Vdc)	2N5695		–	10	
(V_{CE} = 140 Vdc)	2N5696		–	10	
* Collector Cutoff Current (V_{CE} = 50 Vdc) $V_{BE(off)}$ = 0.2 Vdc, T_C = +85°C For All Types	2N5692	I_{CEX2}(1)	–	30	mAdc
(V_{CE} = 80 Vdc)	2N5693		–	30	
(V_{CE} = 100 Vdc)	2N5694		–	30	
(V_{CE} = 120 Vdc)	2N5695		–	30	
(V_{CE} = 140 Vdc)	2N5696		–	30	
* Collector-Emitter Sustaining Voltage (See Figure 3) (I_C = 10 Adc)	2N5692	$V_{CEX(sus)}$	50	–	Vdc
	2N5693		80	–	
	2N5694		100	–	
	2N5695		120	–	
	2N5696		140	–	
(I_C = 40 Adc)	2N5692		45	–	
	2N5693		50	–	
	2N5694		55	–	
	2N5695		60	–	
	2N5696		65	–	
* Collector Cutoff Current (V_{CB} = 2.0 Vdc, I_E = 0)		I_{CBO}	–	200	μAdc
* Emitter Cutoff Current (V_{BE} = 2.5 Vdc, I_C = 0)		I_{EBO}	–	500	mAdc
ON CHARACTERISTICS (1)					
* DC Current Gain (I_C = 25 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	20	65	–
(I_C = 40 Adc, V_{CE} = 2.0 Vdc)			10	–	
* Collector-Emitter Saturation Voltage (I_C = 60 Adc, I_B = 12 Adc)		$V_{CE(sat)}$	–	0.75	Vdc
* Base-Emitter Saturation Voltage (I_C = 60 Adc, I_B = 12 Adc)		$V_{BE(sat)}$	–	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
* Current-Gain—Bandwidth Product (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc, f = 100 kHz)		f_T	200	–	kHz
SWITCHING CHARACTERISTICS					
* Rise Time	(I_C = 25 Adc, I_{B1} = 2.5 Adc, I_{B2} = 2.5 Adc) (See Figure 2)	t_r	–	20	μs
* Storage Time		t_s	–	8.0	μs
* Fall Time		t_f	–	15	μs

*Indicates JEDEC Registered Data.

(1) To avoid excessive heating of the collector junction, perform test with pulse method. (PW ≤ 300 μs, DC ≤ 2.0%).

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

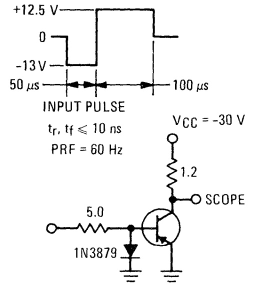
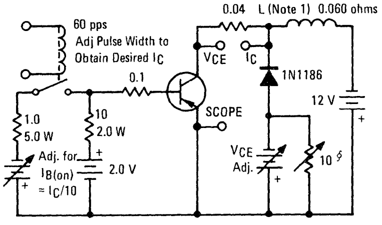


FIGURE 3 – CLAMPED INDUCTIVE SAFE OPERATING AREA TEST CIRCUIT



§ Set to allow reverse surge current to by pass power supply. Not needed for power supply with low reverse impedance.

NOTE 1. L = 10 mH at I_C = 10 A
L = 0.25 mH at I_C = 40 A

2N5716 (SILICON)
2N5717
2N5718

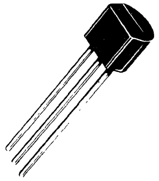
SILICON LOW NOISE N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

Depletion Mode Junction Field-Effect Transistors designed for audio amplifiers in low-power or battery operated applications.

- Low Zero-Gate-Voltage Drain Current @ V_{DS} = 15 Vdc –
  I_{DSS} = 50 µAdc to 250 µAdc – 2N5716
  200 µAdc to 1.0 mAdc – 2N5717
  800 µAdc to 4.0 mAdc – 2N5718
- High Forward Transadmittance @ V_{DS} = 15 Vdc, f = 1.0 kHz –
  $|y_{fs}|$ = 350 µmhos (Typ) @ I_D = 50 µAdc – 2N5716
  550 µmhos (Typ) @ I_D = 200 µAdc – 2N5717
  900 µmhos (Typ) @ I_D = 800 µAdc – 2N5718
- Low Noise Voltage –
  $e_n = 75\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ (Max) @ f = 1.0 kHz
- Drain and Source Interchangeable

LOW NOISE
N-CHANNEL
JUNCTION FIELD-EFFECT
TRANSISTORS

$e_n = 75\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$



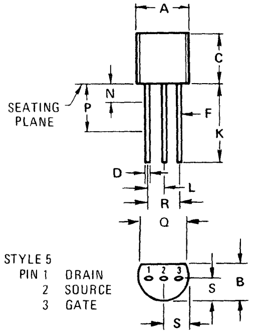
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	40	Vdc
Reverse Gate-Source Voltage	V_{GSR}	40	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Operating Channel Temperature	$T_{channel}$	150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Indicates JEDEC Registered Data.

MECHANICAL CHARACTERISTICS:

Maximum Lead Temperature for Soldering:
240°C, not less than 1/16" from case for 10 s.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Gate-Drain Breakdown Voltage (I_D = 1.0 μAdc, I_S = 0)		$V_{(BR)GSS}$	40	–	Vdc
Gate-Source Cutoff Voltage		$V_{GS(off)}$			Vdc
(V_{DS} = 15 Vdc, I_D = 1.0 nAdc)	2N5716		0.2	3.0	
	2N5717		0.5	5.0	
	2N5718		1.0	8.0	
Gate Reverse Current		I_{GSS}			
(V_{GS} = 20 Vdc, V_{DS} = 0)			–	1.0	nAdc
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C)			–	1.0	μAdc
***ON CHARACTERISTICS**					
Zero-Gate Voltage Drain Current (1)		I_{DSS}			mAdc
(V_{DS} = 15 Vdc, V_{GS} = 0)	2N5716		0.05	0.25	
	2N5717		0.2	1.0	
	2N5718		0.8	4.0	
SMALL-SIGNAL CHARACTERISTICS					
*Forward Transadmittance (1)		$\|y_{fs}\|$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5716		200	1000	
	2N5717		400	1600	
	2N5718		500	2000	
*Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		$\|y_{os}\|$	–	25	μmhos
*Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	5.0	pF
*Output Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	pF
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz, BW = 1.0 Hz)		e_n	–	75	nV/√Hz

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ⩽630 ms, Duty Cycle ≤ 10%

TYPICAL SMALL-SIGNAL CHARACTERISTICS

FIGURE 1 – FORWARD TRANSFER ADMITTANCE

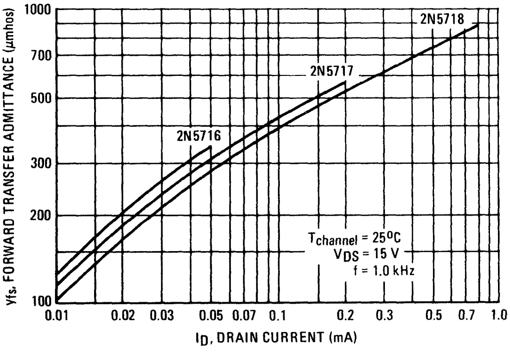
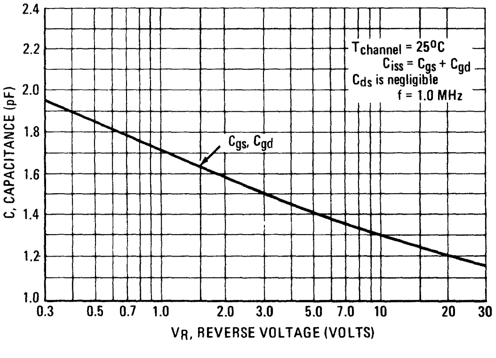
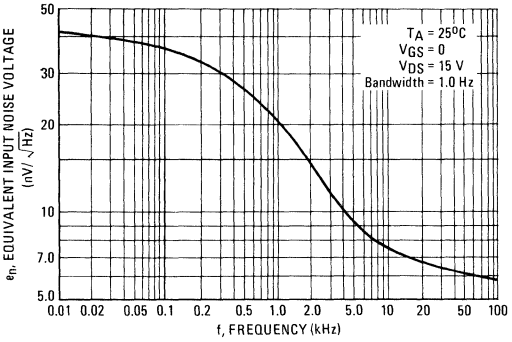


FIGURE 2 – CAPACITANCE



NOISE DATA

FIGURE 3 – TYPICAL NOISE VOLTAGE



In a junction field-effect transistor, the current flow is due to carrier drift, therefore total noise at the input may be expressed as

$$V_T = [e^2_n + 4\,KT\,R_S]^{1/2}$$

where V_T = total noise voltage at the FET input (volts/$\sqrt{Hz}$)
e_n = noise voltage of the FET referred to the input (Figure 3).
K = Boltzman's constant (1.38×10^{-23} j/°K)
T = temperature of the source resistance (°K)
R_S = source resistance (ohms)

Example:

Find the total noise at the input of a 2N5716 FET with a source impedance of 10 kilohms at a frequency of 1.0 kHz and at a temperature of 25°C.

Read e_n = 20.5 $nV/\sqrt{Hz}$ from Figure 3. (Note that this is for a one cycle bandwidth).

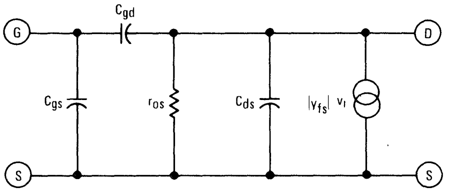
$$V_T = [(20.5\times10^{-9})^2 + (4)(1.38\times10^{-23}(300)(1\times10^4)]^{1/2}$$
$$= 24.2\ nV/\sqrt{Hz}$$

Noise over a frequency band can be handled in one of two ways depending upon whether FET noise is constant or variable over the bandwidth of interest.

1. For constant FET noise, multiply V_T by the square root of bandwidth, i.e., $V'_T = V_T \bullet \Delta f^{1/2}$
2. For variable FET noise, plot V'_T (where Δf = 1.0 Hz) versus frequency over the bandwidth and integrate the result.

Total noise voltage at the output of the FET stage can be found by multiplying V_T by the voltage gain of the stage.

FIGURE 4 – LOW FREQUENCY CIRCUIT MODEL



$y_{is} = j\omega C_{iss}$
$y_{os} = 1/r_{oss} + j\omega C_{oss}$
$y_{fs} = |y_{fs}|$
$y_{rs} = -j\omega C_{rss}$

$C_{iss} = C_{gd} + C_{gs}$
$C_{rss} = C_{gd}$
$C_{oss} = C_{gd} + C_{ds},\ C_{ds} \approx 0$

TYPICAL LIMIT TRANSFER CHARACTERISTICS

(Temperatures Noted are $T_{channel}$)

FIGURE 5 – 2N5716

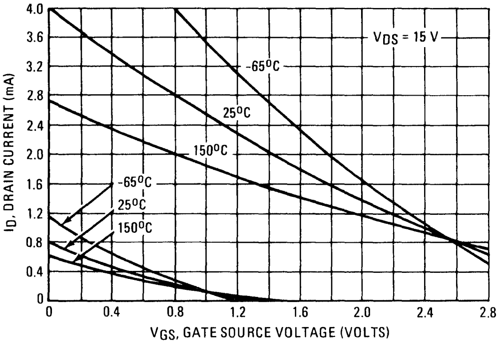


FIGURE 6 – 2N5717

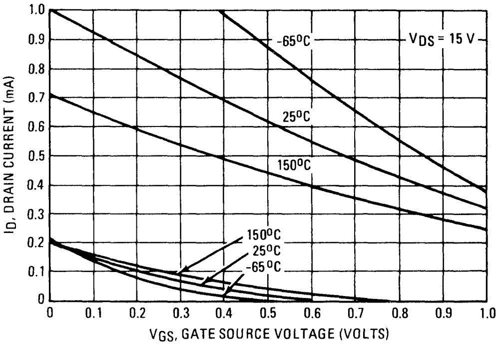


FIGURE 7 – 2N5718

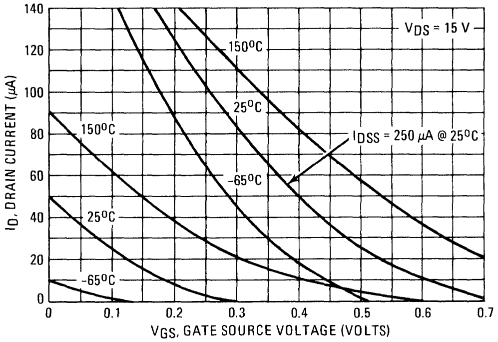
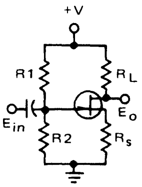
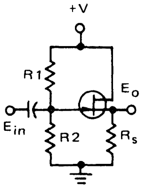
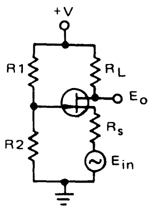


FIGURE 8 – AMPLIFIER EQUATIONS

Circuit Characteristic	Common Source	Source Follower	Common Gate
			
Voltage Gain	$A_v \approx \frac{-R_L}{\frac{1}{gm} + R_s}$	$A_v \approx \frac{R_s}{\frac{1}{gm} + R_s}$	$A_v \approx \frac{R_L}{\frac{1}{gm} + R_s}$
Input Impedance	$Z_{in} \approx R1 \| R2$	$Z_{in} \approx R1 \| R2$	$Z_{in} \approx R_s + \frac{1}{gm}$
Output Impedance	$Z_o \approx R_L$	$Z_o \approx R_s \| \frac{1}{gm}$	$Z_o \approx R_L$

2N5745 (SILICON)

For Specifications, See 2N4398, Volume I.

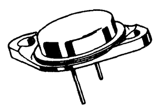
2N5758 (SILICON)
2N5759
2N5760

HIGH-VOLTAGE HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N5758
  = 120 Vdc (Min) – 2N5759
  = 140 Vdc (Min) – 2N5760
- DC Current Gain @ I_C = 3.0 Adc –
  h_{FE} = 25 (Min) – 2N5758
  = 20 (Min) – 2N5759
  = 15 (Min) – 2N5760
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 3.0 Adc
- Complement to PNP transistors 2N6226, 2N6227, 2N6228

6 AMPERE
POWER TRANSISTORS
NPN SILICON
100-120-140 VOLTS
150 WATTS



*MAXIMUM RATINGS

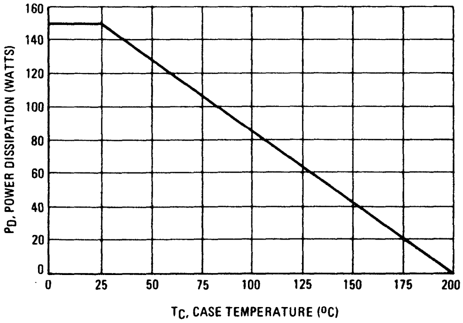
Rating	Symbol	2N5758	2N5759	2N5760	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	7.0			Vdc
Collector Current - Continuous Peak	I_C	6.0 10			Adc
Base Current	I_B	4.0			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857			Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200			°C

THERMAL CHARACTERISTICS

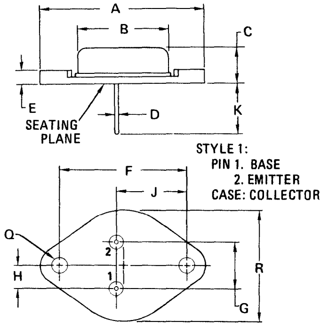
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING



Safe area limits are indicated by Figure 5.
Both limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01

Collector connected to case.

NOTE: 1. DIM "Q" IS DIA.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

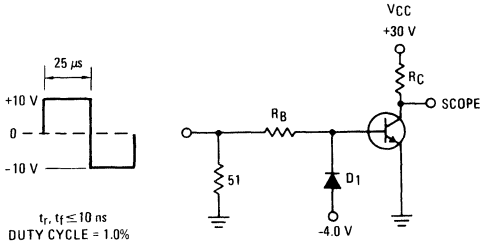
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0	2N5758 2N5759 2N5760	$V_{CEO(sus)}$	100 120 140	– – –	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 70 Vdc, I_B = 0)	2N5758 2N5759 2N5760	I_{CEO}	– – –	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	– –	1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)	2N5758 2N5759 2N5760 All Types	h_{FE}	25 20 15 5.0	100 80 60 –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc) (I_C = 6.0 Adc, I_B = 1.2 Adc)		$V_{CE(sat)}$	– –	1.0 2.0	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	300	pF
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	–	–

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

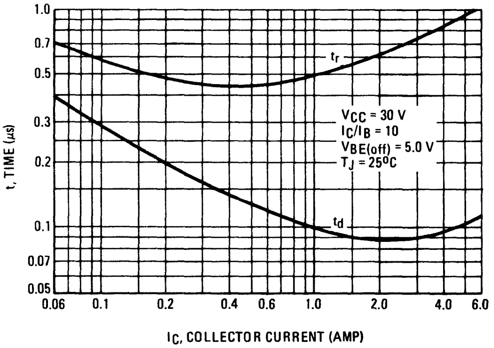


t_r, t_f ≤ 10 ns
DUTY CYCLE = 1.0%

R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

FIGURE 3 – TURN-ON TIME



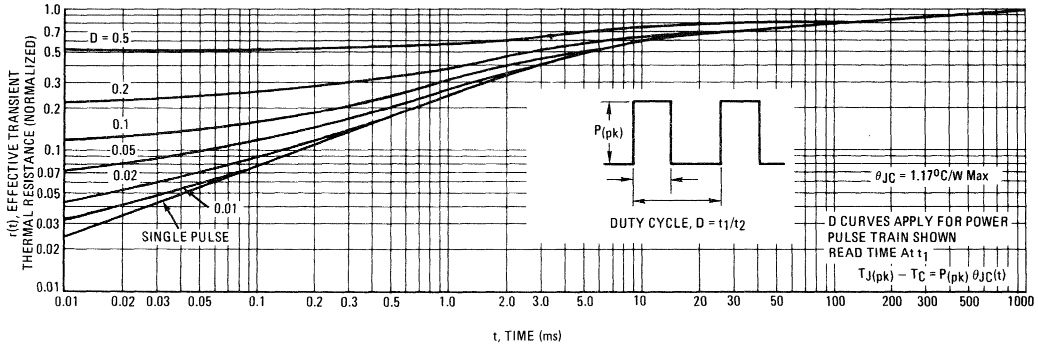


FIGURE 4 – THERMAL RESPONSE

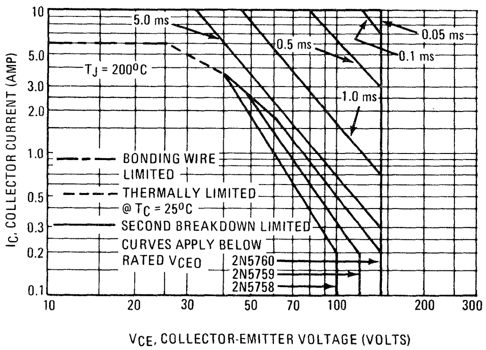


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

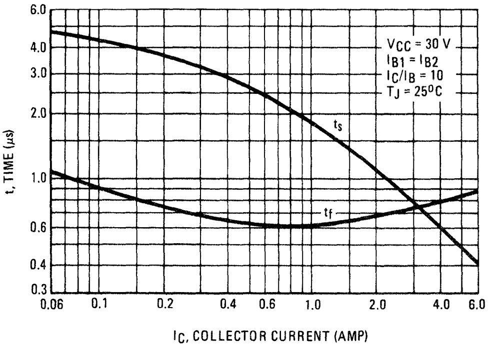


FIGURE 6 – TURN-OFF TIME

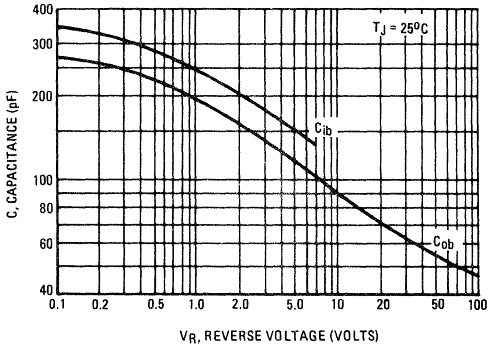


FIGURE 7 – CAPACITANCE

FIGURE 8 – DC CURRENT GAIN

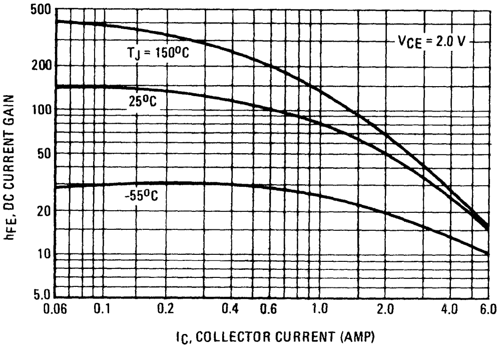


FIGURE 9 – COLLECTOR SATURATION REGION

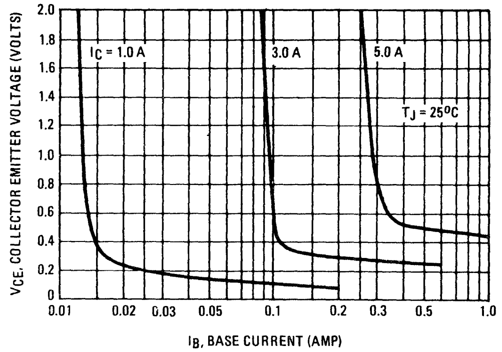


FIGURE 10 – "ON" VOLTAGE

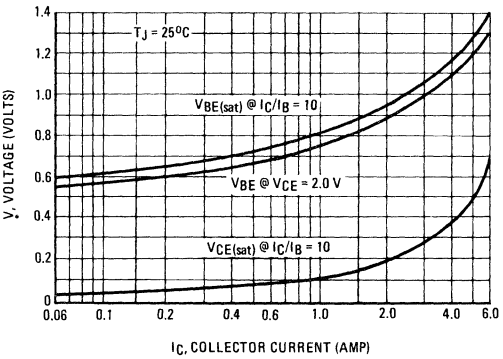


FIGURE 11 – TEMPERATURE COEFFICIENTS

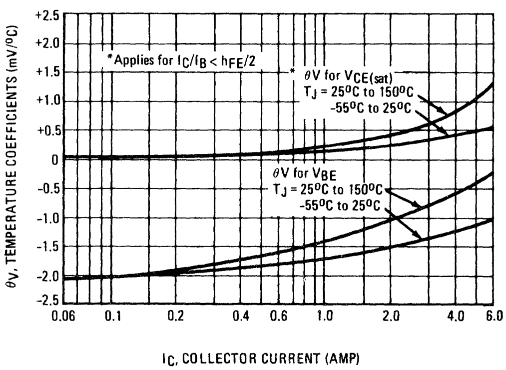


FIGURE 12 – COLLECTOR CUT OFF REGION

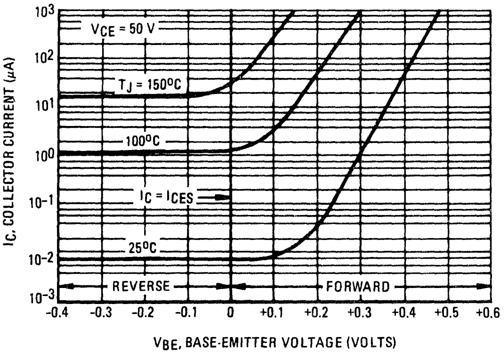
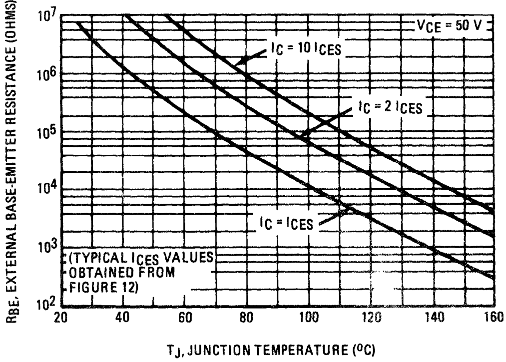


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N5777 thru 2N5780 (SILICON)
MRD14B

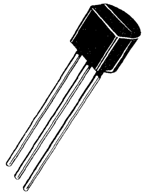
PLASTIC NPN SILICON PHOTO DARLINGTON AMPLIFIERS

. . . designed for applications in industrial inspection, processing and control, counters, sorters, switching and logic circuits or any design requiring extremely high radiation sensitivity, and stable characteristics.

- Economical Plastic Package
- Sensitive Throughout Visible and Near Infra-Red Spectral Range for Wide Application
- Range of Radiation Sensitivities and Voltages for Design Flexibility
- TO-92 Clear Plastic Package for Standard Mounting
- Annular Passivated Structure for Stability and Reliability
- Precision Die Placement

12, 25, 40 VOLT
PHOTO DARLINGTON AMPLIFIERS
NPN SILICON

200 MILLIWATTS



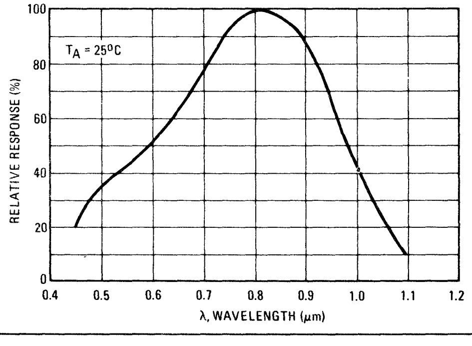
MAXIMUM RATINGS

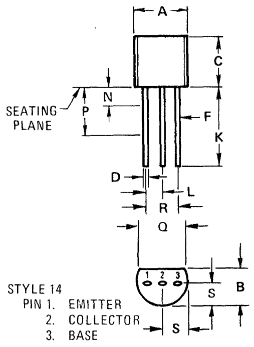
Rating	Symbol	MRD14B	2N5777* 2N5779	2N5778* 2N5780	Unit
Collector-Emitter Voltage	V_{CEO}	12	25	40	Volts
Collector-Base Voltage	V_{CBO}	18	25	40	Volts
Emitter-Base Voltage	V_{EBO}	8.0	8.0	12	Volts
Light Current	I_L	← 250 →			mA
Total Device Dissipation @ $T_A = 25^{\circ}C$ Derate above 25°C	P_D	← 200 → ← 2.67 →			mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}(1)	-65 to +100			°C

*Indicates JEDEC Registered Data.

(1) Heat Sink should be applied to leads during soldering to prevent case temperature from exceeding 100°C.

FIGURE 1 – CONSTANT ENERGY SPECTRAL RESPONSE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

* STATIC ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector Dark Current (Note 2) (V_{CE} = 12 V)		I_{CEO}	–	–	0.1	μA
Collector-Emitter Breakdown Voltage (Note 2)		BV_{CEO}				Volts
(I_C = 10 mA)	MRD14B		12	–	–	
	2N5777, 2N5779		25	–	–	
	2N5778, 2N5780		40	–	–	
Collector-Base Breakdown Voltage (Note 2)		BV_{CBO}				Volts
(I_C = 100 μA)	MRD14B		18	–	–	
	2N5777, 2N5779		25	–	–	
	2N5778, 2N5780		40	–	–	
Emitter-Base Breakdown Voltage (Note 2)		BV_{EBO}				Volts
(I_E = 100 μA)	MRD14B		8.0	–	–	
	2N5777, 2N5779		8.0	–	–	
	2N5778, 2N5780		12	–	–	

* OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
Collector Light Current (Notes 1,4,5)		–	I_L				mA
(V_{CE} = 5.0 V)	MRD14B			0.5	2.0	–	
	2N5777, 2N5778			0.5	4.0	–	
	2N5779, 2N5780			2.0	8.0	–	
DC Current Gain (Note 2)		–	h_{FE}				–
(V_{CE} = 5.0 V, I_C = 0.5 mA)	2N5777, 2N5778			2.5 k	–	–	
	2N5779, 2N5780			5.0 k	–	–	
Wave Length of Maximum Sensitivity		1	λ_s	0.7	0.8	1.0	μm
Turn-On Delay Time (Notes 3, 4)		2,3	t_{d1}	–	–	100	μs
Rise Time (Notes 3, 4)		2,3	t_r	–	–	250	μs
Turn-Off Delay Time (Notes 3, 4)		2,3	t_{d2}	–	–	5.0	μs
Fall Time (Notes 3, 4)		2,3	t_f	–	–	150	μs
Collector-Base Capacitance (V_{CB} = 10 V, f = 1.0 MHz, I_E = 0)	2N5777 thru 2N5780	–	C_{cb}	–	–	10	pF

*Indicates JEDEC Registered Data.

NOTES:

1. Radiation Flux Density (H) equal to 2.0 mW/cm^2 emitted from a tungsten source at a color temperature of 2870 K.
2. Measured under dark conditions. (H≈0).
3. For unsaturated rise time measurements, radiation is provided by a pulsed GaAs (gallium-arsenide) light-emitting diode ($\lambda \approx$ 0.9 μm) with a pulse width equal to or greater than 500 microseconds (see Figures 2 and 3).
4. Measurement mode with no electrical connection to the base lead.
5. Die faces curved side of package.

FIGURE 2 – PULSE RESPONSE TEST CIRCUIT

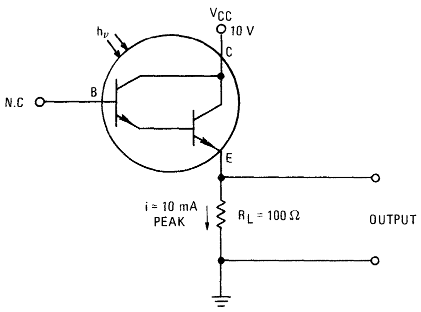
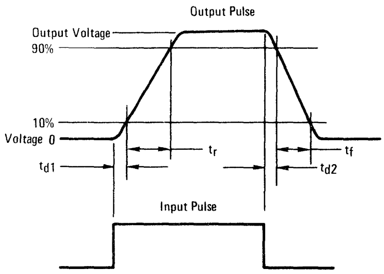


FIGURE 3 – PULSE RESPONSE TEST WAVEFORM



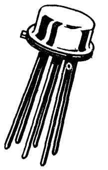
2N5793 (SILICON)
2N5794

DUAL NPN SILICON ANNULAR TRANSISTORS

. . . designed for high-speed switching circuits, dc to VHF amplifier applications and complementary circuitry to the PNP 2N5795 and 2N5796.

- DC Current Gain Specified – 0.1 mAdc to 300 mAdc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)} = 0.3$ Vdc (Max) @ $I_C = 150$ mAdc
- All Leads Electrically Isolated for Design Flexibility
- Each Transistor Similar to 2N2218A or 2N2219A

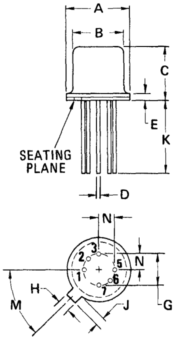
NPN SILICON DUAL TRANSISTORS



*MAXIMUM RATINGS

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	40		Vdc
Collector-Base Voltage	V_{CB}	75		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous	I_C	600		mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
		One Die	Both Die Equal Power	
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	500 2.9	600 3.4	mW mW/°C
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	1.2 6.9	2.0 11.43	Watts mW/°C

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. OMITTED
5. EMITTER
6. BASE
7. COLLECTOR
8. OMITTED

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.70	0.150	0.185
D	0.41	0.53	0.016	0.021
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	--	0.500	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

CASE 654-07

2N5793, 2N5794 (continued)

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	40	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	75	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	–	10	nAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	10	nAdc
Collector 1 to Collector 2 Leakage Current ($V_{1C\text{-}2C}$ = ±50 Vdc)	$I_{C1\text{-}C2}$	–	±1.0	nAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 100 μAdc, V_{CE} = 10 Vdc) 2N5793		20	–	
2N5794		35	–	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc) 2N5793		25	–	
2N5794		50	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)(1) 2N5793		35	–	
2N5794		75	–	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)(1) 2N5793		20	–	
2N5794		50	–	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)(1) 2N5793		40	120	
2N5794		100	300	
(I_C = 300 mAdc, V_{CE} = 10 Vdc)(1) 2N5793		25	–	
2N5794		40	–	
Collector-Emitter Saturation Voltage(1)	$V_{CE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)		–	0.3	
(I_C = 300 mAdc, I_B = 30 mAdc)		–	0.9	
Base-Emitter Saturation Voltage(1)	$V_{BE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)		0.6	1.2	
(I_C = 300 mAdc, I_B = 30 mAdc)		–	1.8	
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product(2) (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	250	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	–	8.0	pF
Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	25	pF
SWITCHING CHARACTERISTICS				
Delay Time (V_{CC} = 30 Vdc, $V_{BE(off)}$ = 0.5 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) (See Figure 1)	t_d	–	15	ns
Rise Time	t_r	–	30	ns
Storage Time (V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) (See Figure 2)	t_s	–	250	ns
Fall Time	t_f	–	60	ns

*Indicates JEDEC Registered Data.

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2)f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – TURN-ON TIME TEST

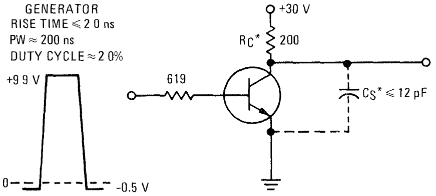
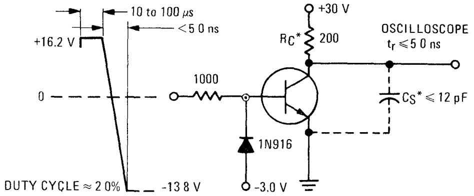


FIGURE 2 – TURN-OFF TIME TEST CIRCUIT



*C_S is total shunt capacitance of oscilloscope and test fixture
R_C includes oscilloscope resistance.

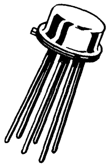
2N5795 (SILICON)
2N5796

DUAL PNP SILICON ANNULAR TRANSISTORS

. . . designed for high-speed switching circuits, dc to VHF amplifier applications and complementary circuits with the NPN 2N5793 and 2N5794.

- DC Current Gain Specified – 0.1 mAdc to 500 mAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.4 Vdc (Max) @ I_C = 150 mAdc
- All Leads Electrically Isolated for Design Flexibility
- Each Transistor Similar to 2N2904A or 2N2905A

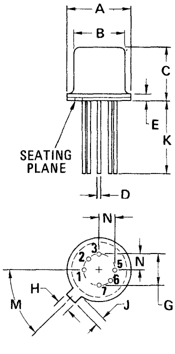
PNP SILICON
DUAL TRANSISTORS



*MAXIMUM RATINGS

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	60		Vdc
Collector-Base Voltage	V_{CB}	60		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	600		mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
		One Die	Both Die Equal Power	
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	500 2.9	600 3.4	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.2 6.9	2.0 11.43	Watts mW/°C

*Indicates JEDEC Registered Data.

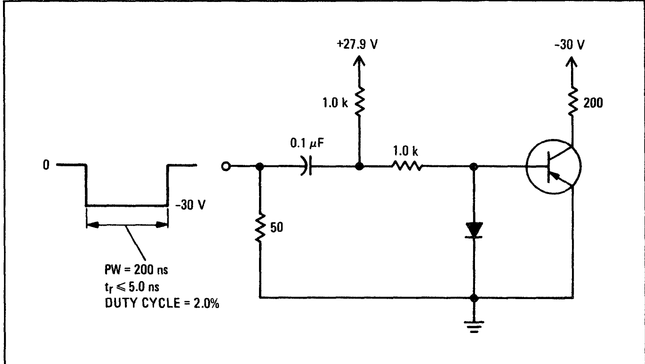


STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. OMITTED
5. EMITTER
6. BASE
7. COLLECTOR
8. OMITTED

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.70	0.150	0.185
D	0.41	0.53	0.016	0.021
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

CASE 654-07

FIGURE 1 – SATURATED SWITCHING TIMES TEST CIRCUIT



*__ELECTRICAL CHARACTERISTICS__ (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 10 mAdc, I_B = 0)		BV_{CEO}	60	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		BV_{CBO}	60	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)		I_{CBO}	–	20	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
Collector 1 to Collector 2 Leakage Current ($V_{1C\text{-}2C}$ = ±50 Vdc)		$I_{C1\text{-}C2}$	–	±1.0	nAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 100 μAdc, V_{CE} = 10 Vdc)	2N5795 2N5796		40 75	– –	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	2N5795 2N5796		40 100	– –	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)(1)	2N5795 2N5796		40 100	– –	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)(1)	2N5795 2N5796		20 50	– –	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)(1)	2N5795 2N5796		40 100	120 300	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)(1)	2N5795 2N5796		40 50	– –	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)			–	0.4	
(I_C = 500 mAdc, I_B = 50 mAdc)			–	1.6	
Base-Emitter Saturation Voltage(1)		$V_{BE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)			–	1.3	
(I_C = 500 mAdc, I_B = 50 mAdc)			–	2.6	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product(2) (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)		f_T	200	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{cb}	–	8.0	pF
Emitter-Base Capacitance (V_{EB} = 2.0 Vdc, I_C = 0, f = 100 kHz)		C_{eb}	–	30	pF
SWITCHING CHARACTERISTICS (See Figure 1)					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = 0.5 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc)	t_d	–	12	ns
Rise Time		t_r	–	35	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc)	t_s	–	100	ns
Fall Time		t_f	–	40	ns

*Indicates JEDEC Registered Data.

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%

(2)f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

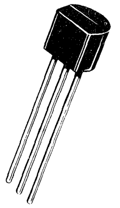
2N5797 (SILICON)
thru
2N5800

SILICON P-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

Symmetrical depletion mode Junction Field-Effect Transistors designed primarily for low-power, audio amplifier applications.

- Low Reverse Transfer Capacitance – C_{rss} = 1.0 pF (Max)
- Drain and Source Interchangeable
- Low Gate Reverse Current – I_{GSS} = 1.0 nAdc (Max)
- Unibloc Plastic Package Encapsulation

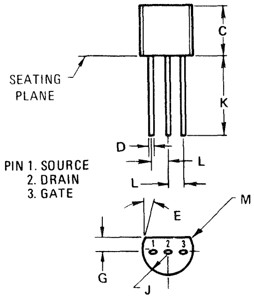
P-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	Vdc
Drain-Gate Voltage	V_{DG}	40	Vdc
Reverse Gate-Source Voltage	V_{GSR}	40	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

*Indicates JEDEC Registered Data.



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
C	0.175	0.185	4.450	4.700
D	0.016	0.019	0.407	0.482
E	5° NOM		5° NOM	
G	0.045	0.055	1.150	1.390
J	0.085	0.095	2.160	2.420
K	0.500	–	12.700	–
L	0.050 TP		1.270 TP	
M	0.003	0.013	0.076	0.330

CASE 29-01
TO-92

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTIC				
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	40	–	Vdc
Gate-Source Cutoff Voltage (V_{DS} = −15 Vdc, I_D = −10 μAdc) 2N5797	$V_{GS(off)}$	0.5	4.0	Vdc
2N5798		0.8	6.0	
2N5799		1.2	8.0	
2N5800		2.0	9.0	
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	–	1.0	nAdc
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C)		–	1.0	μAdc
ON CHARACTERISTICS				
Zero Gate Voltage Drain Current (V_{DS} = −15 Vdc, V_{GS} = 0) 2N5797	I_{DSS}	0.02	0.1	mAdc
2N5798		0.08	0.4	
2N5799		0.25	1.0	
2N5800		0.70	2.0	
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance (1) (V_{DS} = −15 Vdc, V_{GS} = 0, f = 1.0 kHz) 2N5797	$\lvert y_{fs} \rvert$	60	225	mmhos
2N5798		100	400	
2N5799		160	500	
2N5800		250	700	
Output Admittance (1) (V_{DS} = −15 Vdc, V_{GS} = 0, f = 1.0 kHz) 2N5797	$\lvert y_{os} \rvert$	–	1.0	μmhos
2N5798		–	2.5	
2N5799		–	5.0	
2N5800		–	10	
Input Capacitance (V_{DS} = −15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	–	5.0	pF
Reverse Transfer Capacitance (V_{DS} = −15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	–	1.0	pF
Common-Source Noise Figure (V_{DS} = −15 Vdc, V_{GS} = 0, R_S = 1.0 Megohm, f = 1.0 kHz, BW = 1.0 Hz)	NF	–	2.5	dB
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = −15 Vdc, V_{GS} = 0, f = 1.0 kHz, BW = 1.0 Hz)	e_n	–	110	$nV/\sqrt{Hz}$

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 360 ms, Duty Cycle = 2.0%.

TYPICAL SMALL-SIGNAL CHARACTERISTICS

FIGURE 1 – FORWARD TRANSFER ADMITTANCE

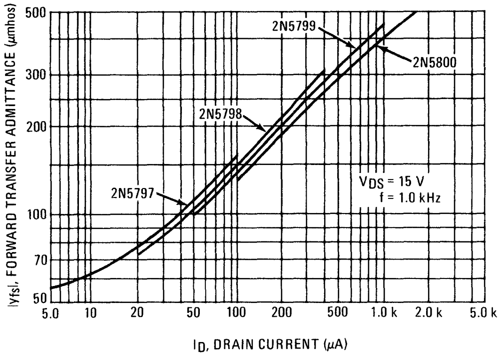
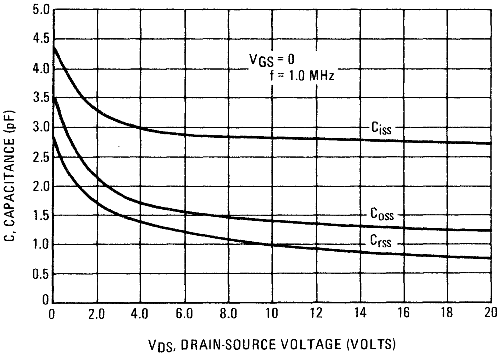


FIGURE 2 – CAPACITANCE



TYPICAL NOISE FIGURE

FIGURE 3 – EFFECTS OF FREQUENCY

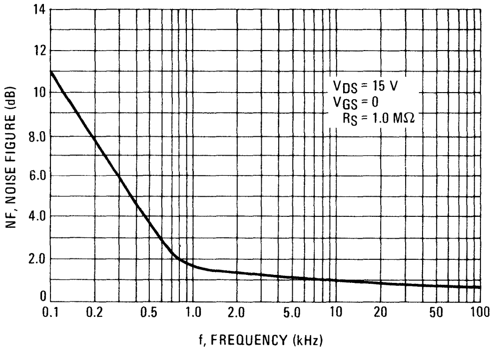


FIGURE 4 – EFFECTS OF SOURCE RESISTANCE

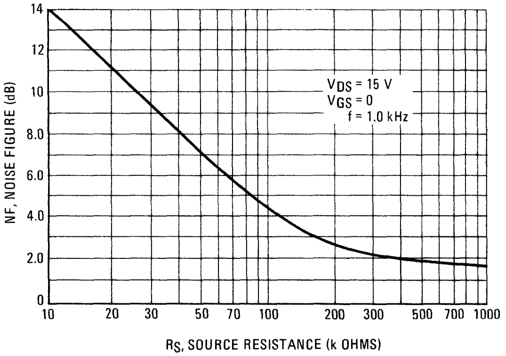
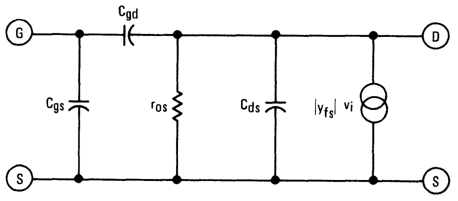


FIGURE 5 – LOW FREQUENCY CIRCUIT MODEL



$y_{is} = j\omega C_{iss}$
$y_{os} = 1/r_{oss} + j\omega C_{oss}$
$y_{fs} = |y_{fs}|$
$y_{rs} = -j\omega C_{rss}$

$C_{iss} = C_{gd} + C_{gs}$
$C_{rss} = C_{gd}$
$C_{oss} = C_{gd} + C_{ds}$

TYPICAL LIMIT TRANSFER CHARACTERISTICS
(TEMPERATURES NOTED ARE T_J)

FIGURE 6 – 2N5797

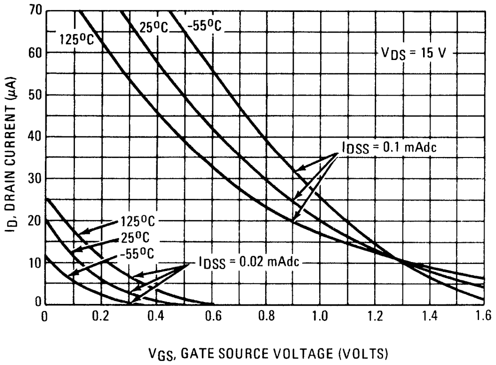


FIGURE 7 – 2N5798

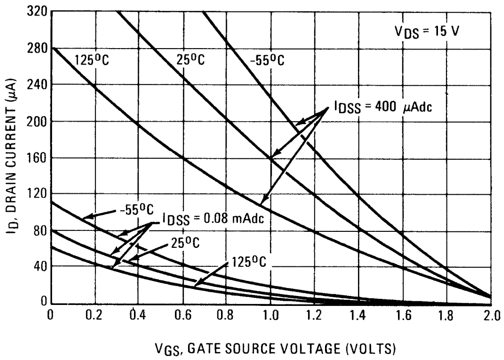


FIGURE 8 – 2N5799

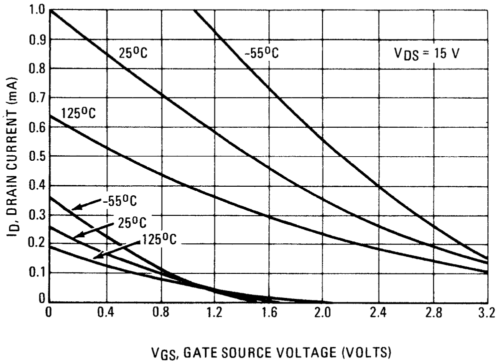
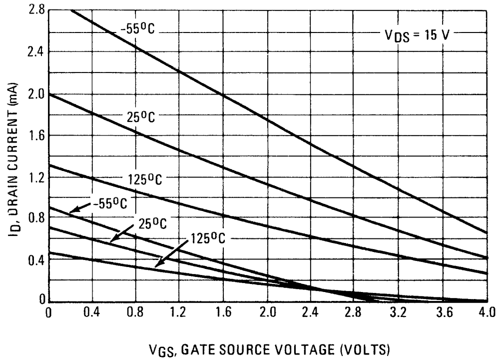


FIGURE 9 – 2N5800



2N5829

For Specifications, See 2N4957 Data, Volume I.

2N5835 (SILICON)
2N5836
2N5837

NPN SILICON HIGH-FREQUENCY TRANSISTORS

. . . designed primarily for use in fast current-mode switching circuits in military and industrial equipment. Suitable for use in general high-frequency amplifier applications to 1.5 GHz.

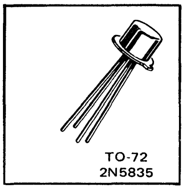
- High Current-Gain—Bandwidth Product —
  f_T = 2.5 GHz (Min) @ I_C = 10 mAdc – 2N5835
  2.0 GHz (Min) @ I_C = 50 mAdc – 2N5836
  1.7 GHz (Min) @ I_C = 100 mAdc – 2N5837
- Fast Non-Saturated Switching Times —
  t_r = 250 ps (Typ) @ I_C = 10 mAdc – 2N5835
  320 ps (Typ) @ I_C = 50 mAdc – 2N5836
  650 ps (Typ) @ I_C = 100 mAdc – 2N5837
- Characterized with Scattering Parameters

*MAXIMUM RATINGS

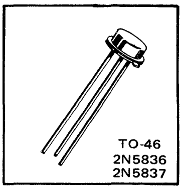
Rating	Symbol	2N5835	2N5836	2N5837	Unit
Collector-Emitter Voltage	V_{CEO}	10	10	5.0	Vdc
Collector-Base Voltage	V_{CB}	15	15	10	Vdc
Emitter-Base Voltage	V_{EB}	3.5	3.5	3.5	Vdc
Collector Current – Continuous	I_C	15	200	300	mAdc
Total Device Dissipation @ $T_A = 25^oC$ Derate above 25°C	P_D	200 1.14	– –	– –	mW mW/°C
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25°C	P_D	– –	2.0 11.43		Watts mW/°C
Storage Junction Temperature Range	T_{stg}	←—— -65 to +200 ——→			°C

*Indicates JEDEC Registered Data.

NPN SILICON HIGH-FREQUENCY TRANSISTORS

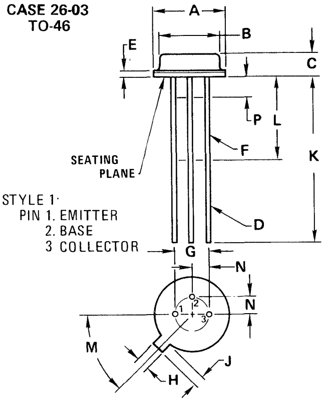


TO-72
2N5835



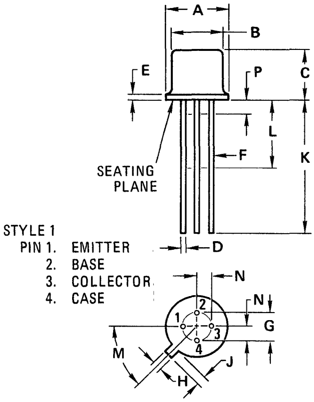
TO-46
2N5836
2N5837

CASE 26-03
TO-46



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	1.65	2.16	0.065	0.085
D	0.406	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.305	0.483	0.012	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC dimensions and notes apply



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45°BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

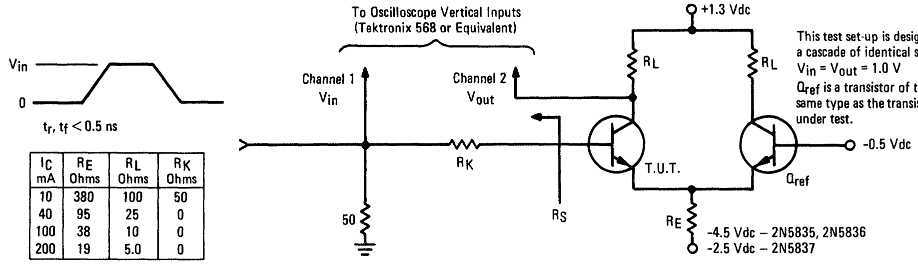
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Base Breakdown Voltage		BV_{CBO}				Vdc
(I_C = 10 μAdc, I_E = 0)	2N5835		15	–	–	
(I_C = 100 μAdc, I_E = 0)	2N5836		15	–	–	
	2N5837		10	–	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	3.5	–	–	Vdc
Collector Cutoff Current		I_{CBO}				μAdc
(V_{CB} = 7.5 Vdc, I_E = 0)	2N5835		–	–	0.01	
(V_{CB} = 10 Vdc, I_E = 0)	2N5836		–	–	10	
(V_{CB} = 5.0 Vdc, I_E = 0)	2N5837		–	–	10	
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)		I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				–
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc)	2N5835		25	–	–	
(I_C = 50 mAdc, V_{CE} = 6.0 Vdc)	2N5836		25	–	–	
(I_C = 100 mAdc, V_{CE} = 3.0 Vdc)	2N5837		25	–	–	
Base-Emitter On Voltage		$V_{BE(on)}$				Vdc
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc)	2N5835		–	–	0.9	
(I_C = 50 mAdc, V_{CE} = 6.0 Vdc)	2N5836		–	–	0.9	
(I_C = 100 mAdc, V_{CE} = 3.0 Vdc)	2N5837		–	–	0.9	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product ①		f_T				GHz
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc, f = 200 MHz)	2N5835		2.5	–	–	
(I_C = 50 mAdc, V_{CE} = 6.0 Vdc, f = 200 MHz)	2N5836		2.0	–	–	
(I_C = 100 mAdc, V_{CE} = 3.0 Vdc, f = 200 MHz)	2N5837		1.7	–	–	
Collector-Base Capacitance		C_{cb}				pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	2N5835		–	–	0.8	
	2N5836		–	–	3.5	
(V_{CB} = 5.0 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	2N5837		–	–	5.0	
Collector-Base Time Constant ②		$r_b'C_c$				ps
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc, f = 63.6 MHz)	2N5835		–	5.0	–	
(I_C = 50 mAdc, V_{CE} = 6.0 Vdc, f = 63.6 MHz)	2N5836		–	6.0	–	
(I_C = 100 mAdc, V_{CE} = 3.0 Vdc, f = 63.6 MHz)	2N5837		–	6.0	–	
SWITCHING CHARACTERISTICS ②						
Rise Time (See Figure 1) (I_C = 10 mAdc)	2N5835	t_r	–	250	–	ps
(I_C = 40 mAdc)	2N5836		–	320	–	
(I_C = 100 mAdc)	2N5837		–	650	–	

*Indicates JEDEC Registered Data

① f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

② Typical values shown in addition to JEDEC Registered Data.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



I_C mA	R_E Ohms	R_L Ohms	R_K Ohms
10	380	100	50
40	95	25	0
100	38	10	0
200	19	5.0	0

This test set-up is designed to simulate a cascade of identical stages. $R_S = R_L$
$V_{in} = V_{out}$ = 1.0 V
Q_{ref} is a transistor of the same type as the transistor under test.

FIGURE 2 – SWITCHING TIME

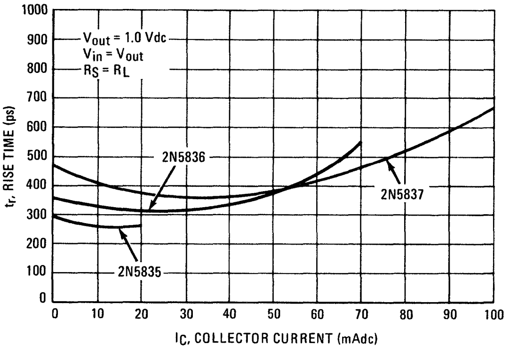


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

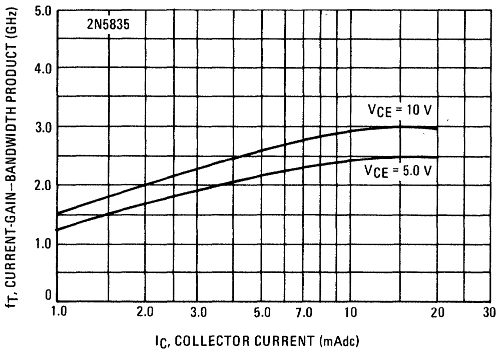


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT

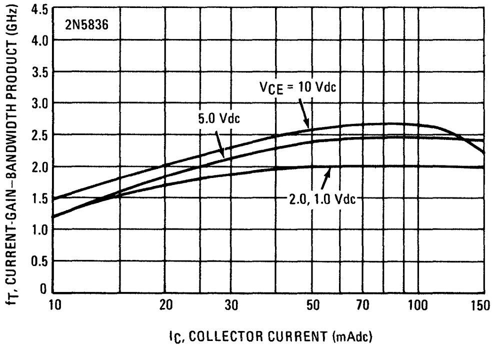


FIGURE 5 – CURRENT-GAIN–BANDWIDTH PRODUCT

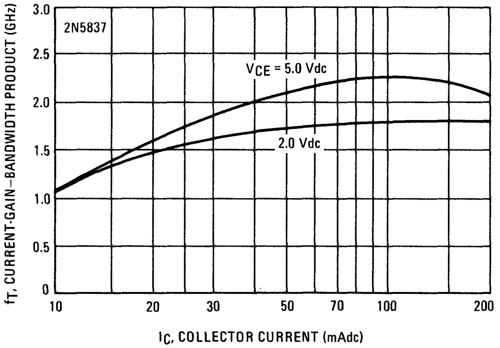


FIGURE 6 – COLLECTOR-BASE TIME CONSTANT

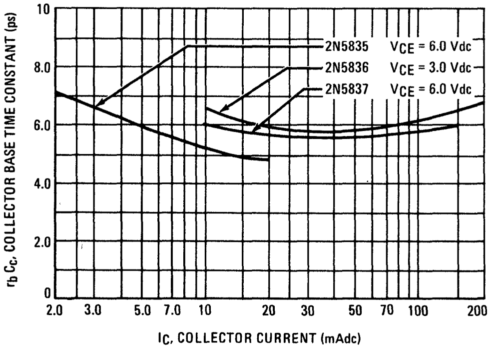
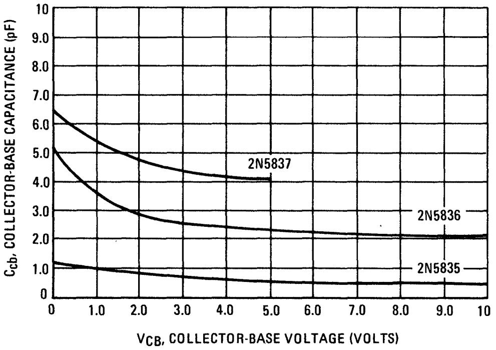


FIGURE 7 – COLLECTOR-BASE CAPACITANCE



2N5835 SCATTERING PARAMETERS

(I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, Z_G = Z_L = 50 Ohms)

FIGURE 8 – S_{11}, INPUT REFLECTION COEFFICIENT

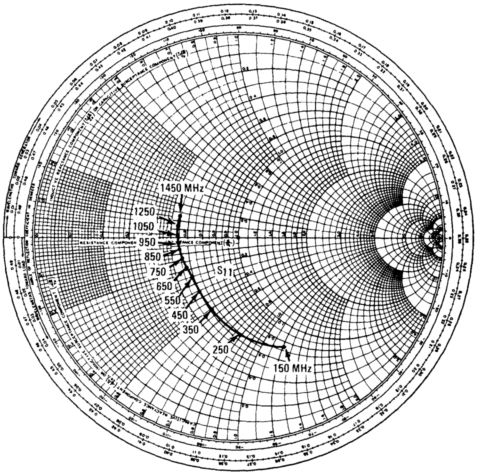


FIGURE 9 – S_{22}, OUTPUT REFLECTION COEFFICIENT

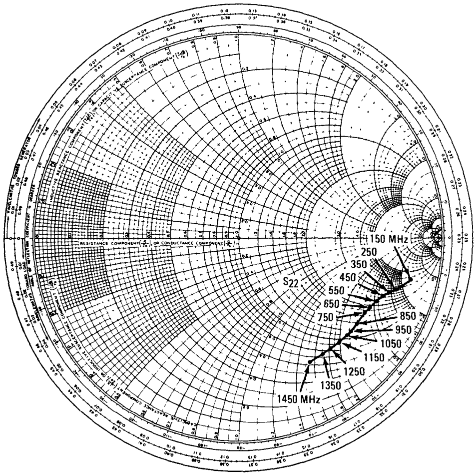


FIGURE 10 – S_{12}, REVERSE TRANSMISSION COEFFICIENT

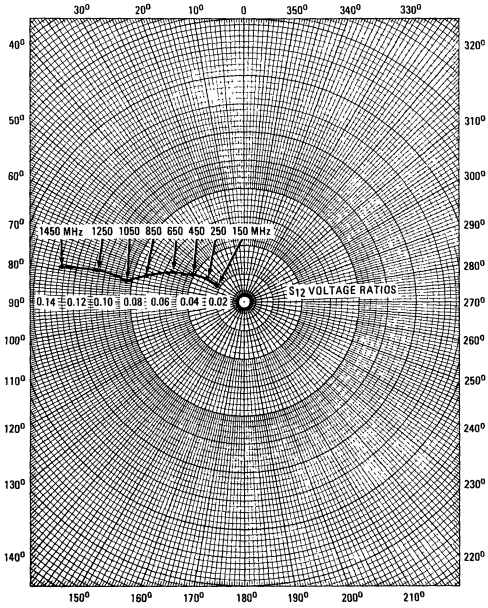
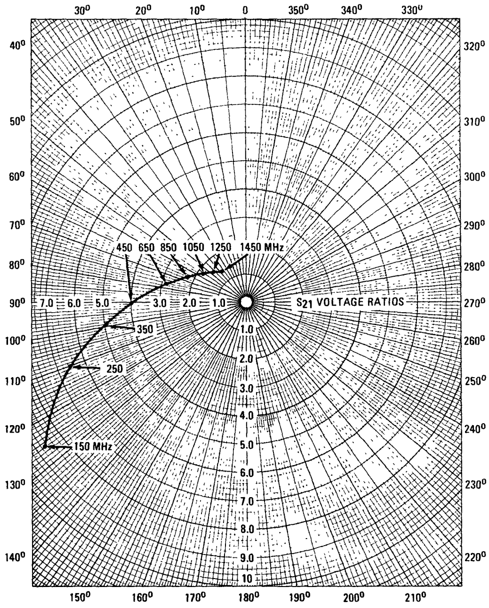


FIGURE 11 – S_{21}, FORWARD TRANSMISSION COEFFICIENT



2N5836 SCATTERING PARAMETERS

(I_C = 100 mAdc, V_{CE} = 10 Vdc, Z_G = Z_L = 50 Ohms)

FIGURE 12 – S_{11}, INPUT REFLECTION COEFFICIENT

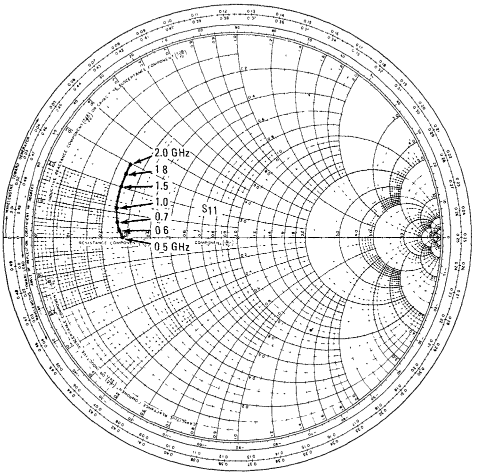


FIGURE 13 – S_{22}, OUTPUT REFLECTION COEFFICIENT

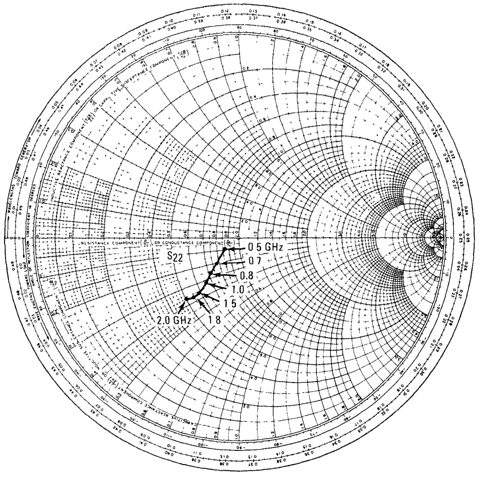


FIGURE 14 – S_{12}, REVERSE TRANSMISSION COEFFICIENT

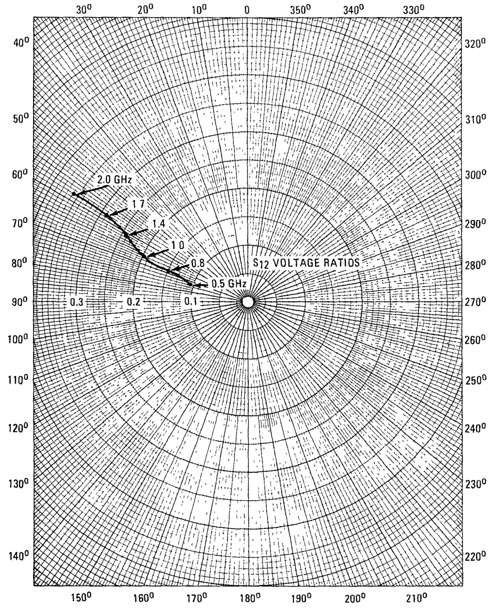
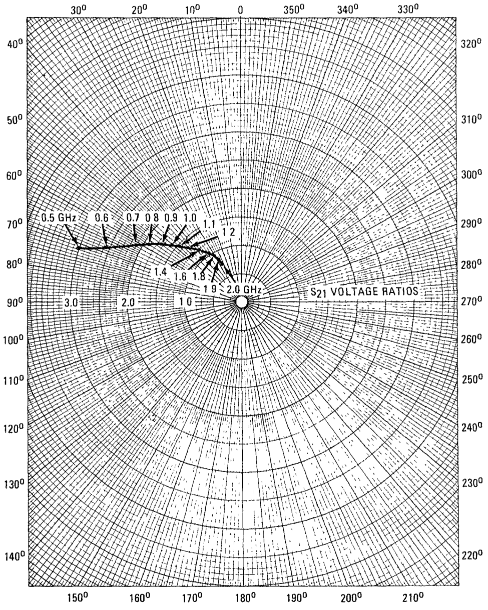


FIGURE 15 – S_{21}, FORWARD TRANSMISSION COEFFICIENT



2N5837 SCATTERING PARAMETERS

(I_C = 100 mAdc, V_{CE} = 3.0 Vdc, Z_G = Z_L = 50 Ohms)

FIGURE 16 – S_{11}, INPUT REFLECTION COEFFICIENT

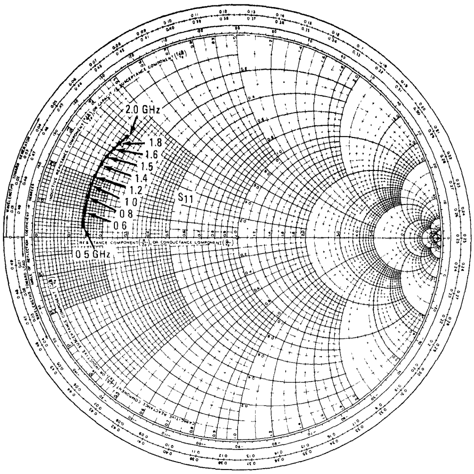


FIGURE 17 – S_{22}, OUTPUT REFLECTION COEFFICIENT

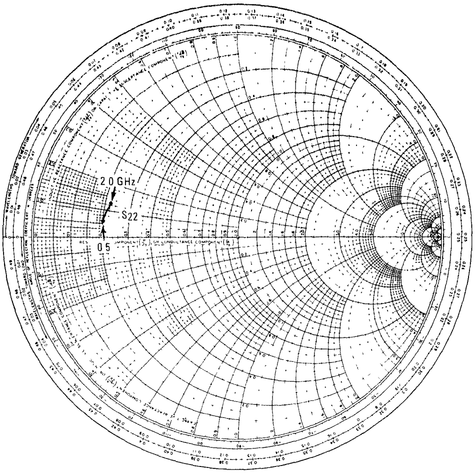


FIGURE 18 – S_{12}, REVERSE TRANSMISSION COEFFICIENT

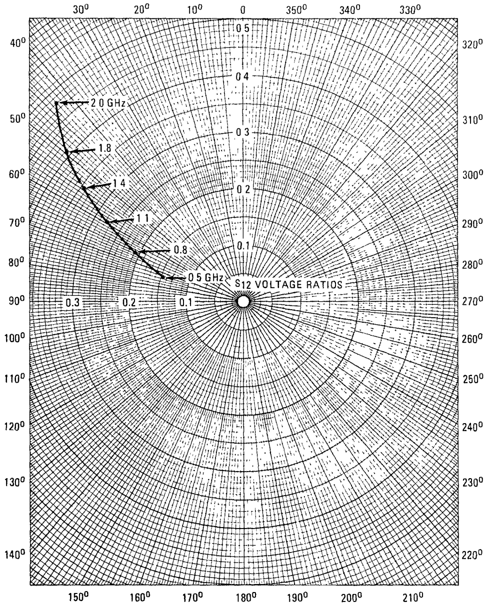
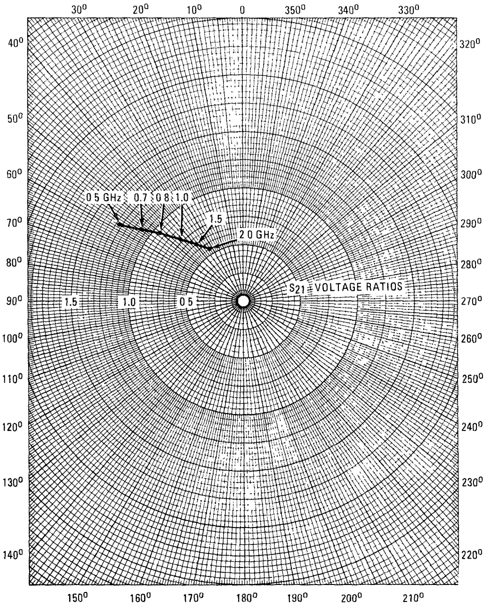


FIGURE 19 – S_{21}, FORWARD TRANSMISSION COEFFICIENT



2N5841 (SILICON)
2N5842

NPN SILICON RF TRANSISTORS

. . . designed to provide ultra-fast switching times in current-mode circuits at collector currents to 80 mAdc.

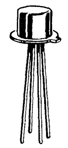
- High Current-Gain—Bandwidth Product — @ I_C = 25 mAdc
  f_T = 2.2 GHz (Min) 2N5841
  1.7 GHz (Min) 2N5842
- Low Collector-Base Capacitance —
  C_{cb} = 1.5 pF (Max) @ V_{CB} = 4.0 Vdc
- Fast Non-Saturated Switching Times — @ I_C = 30 mAdc
  Typical Values
  $t_{d(on)}$ = 0.4 ns
  t_r = 0.18 ns
  $t_{d(off)}$ = 0.3 ns
  t_f = 0.20 ns

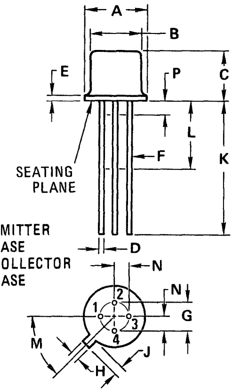
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	10	Vdc
Collector-Base Voltage	V_{CB}	20	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	100	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 2.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

NPN SILICON
RF TRANSISTORS





STYLE 10
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45°BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

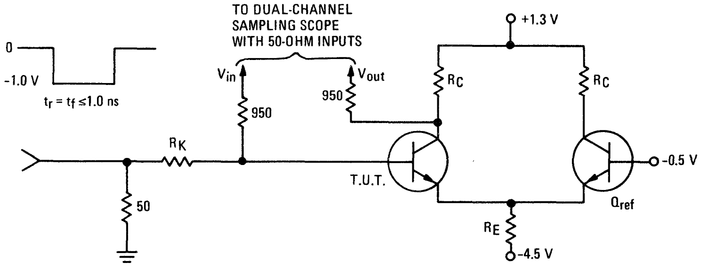
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	10	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	20	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	20	nAdc
Emitter Cutoff Current (V_{BE} = 2.5 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				–
(I_C = 25 mAdc, V_{CE} = 4.0 Vdc) 2N5841		25	–	200	
2N5842		25	–	250	
Base-Emitter On Voltage (I_C = 25 mAdc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product	f_T				GHz
(I_C = 10 mAdc, V_{CE} = 4.0 Vdc, f = 200 MHz) 2N5841		2.0	2.6	–	
2N5842		–	2.0	–	
(I_C = 25 mAdc, V_{CE} = 4.0 Vdc, f = 200 MHz) 2N5841		2.2	2.7	–	
2N5842		1.7	2.0	–	
(I_C = 50 mAdc, V_{CE} = 4.0 Vdc, f = 200 MHz) 2N5841		–	2.2	–	
2N5842		–	1.5	–	
Collector-Base Capacitance (V_{CB} = 4.0 Vdc, I_E = 0, f = 100 MHz)	C_{cb}	–	0.9	1.5	pF
Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 MHz)	C_{eb}	–	0.7	1.1	pF
Collector-Base Time Constant	$r_b'C_c$				ps
(I_C = 25 mAdc, V_{CE} = 4.0 Vdc, f = 31.8 MHz) 2N5841		–	18	25	
2N5842		–	25	40	

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Turn-On Delay Time	(I_C = 30 mAdc)	$t_{d(on)}$	–	0.40	–	ns
Rise Time		t_r	–	0.18	–	ns
Turn-Off Delay Time	(I_C = 30 mAdc)	$t_{d(off)}$	–	0.30	–	ns
Fall Time		t_f	–	0.20	–	ns

*Indicates JEDEC Registered Data

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT



I_C mA	R_E Ohms	R_C Ohms	R_K Ohms
1.0	3.8 k	1.0 k	950
2.0	1.9 k	500	450
4.0	950	250	200
6.0	635	167	117
8.0	475	125	75
10	380	100	50
20	190	50	0
40	95	25	0
60	64	16-17	0
80	48	12-13	0
100	38	10	0

V_{in} and V_{out} are attenuated 20:1 at scope inputs. Before attenuation, V_{in} = V_{out} = 1.0 V.
Q_{ref} is a transistor of the same type as the transistor under test.

FIGURE 2 – CURRENT GAIN BANDWIDTH PRODUCT

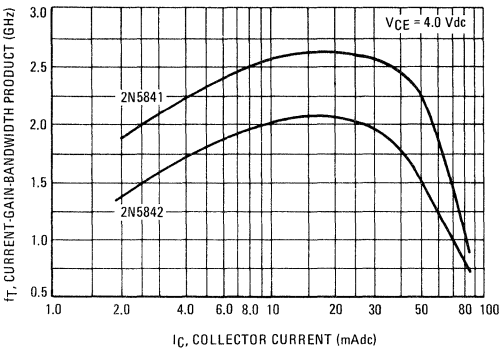


FIGURE 3 – COLLECTOR-BASE TIME CONSTANT

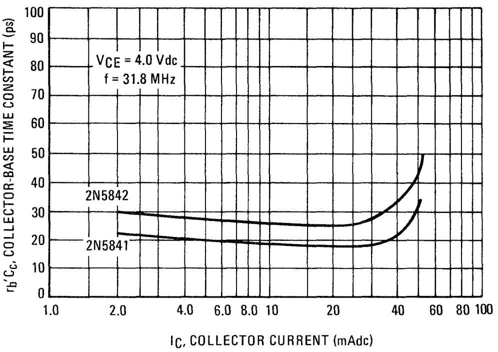


FIGURE 4 – SWITCHING TIMES

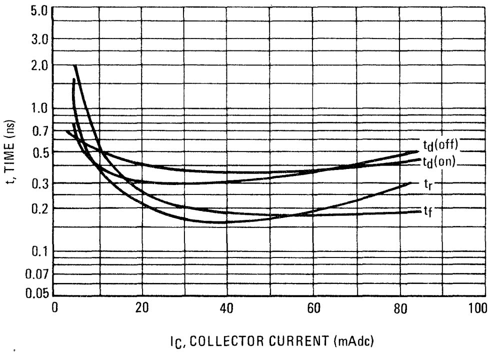


FIGURE 5 – CAPACITANCES

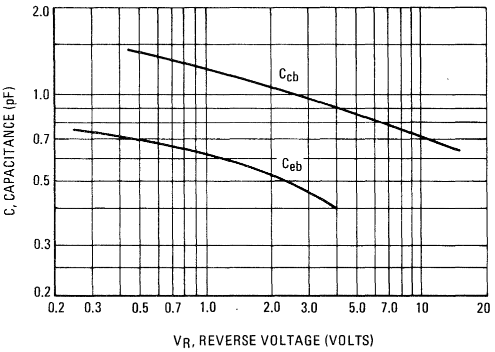


FIGURE 6 – BASE-EMITTER VOLTAGE versus CURRENT

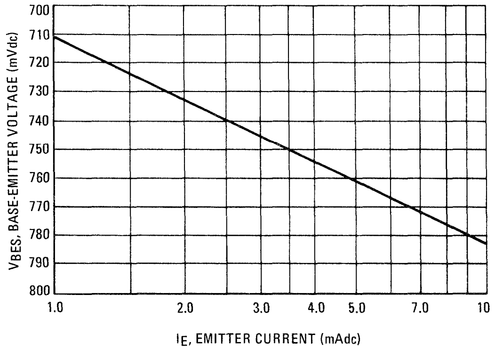
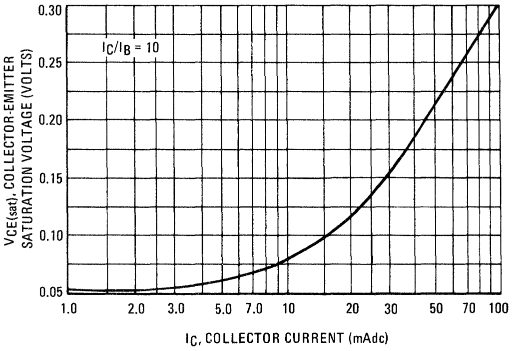


FIGURE 7 – COLLECTOR-EMITTER SATURATION VOLTAGE



V_{CE} = 4.0 Vdc, I_C = 10 mAdc

FIGURE 8 – INPUT ADMITTANCE versus FREQUENCY

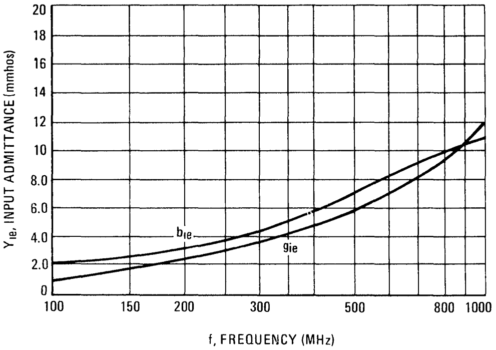


FIGURE 9 – OUTPUT ADMITTANCE versus FREQUENCY

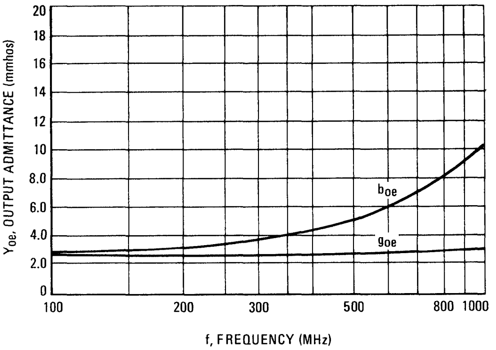


FIGURE 10 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

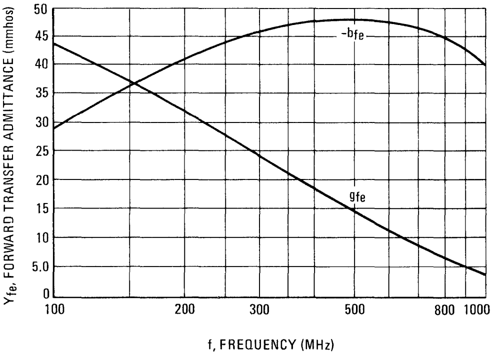
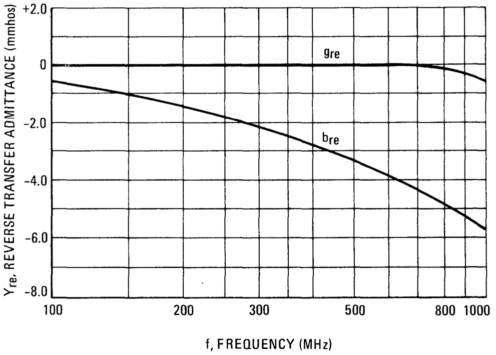
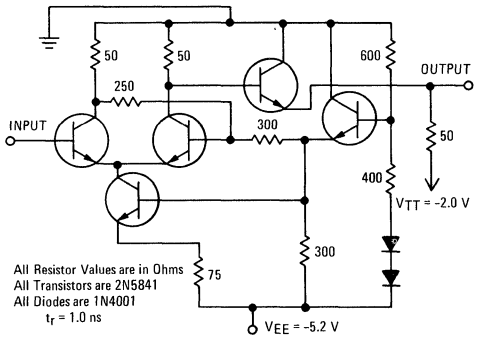


FIGURE 11 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY



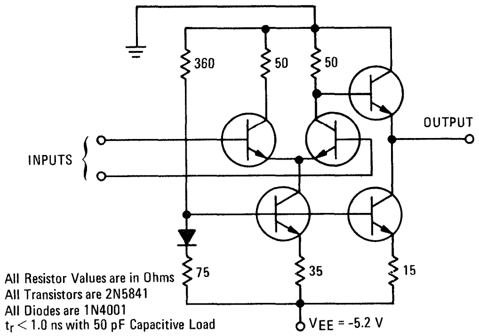
NON-SATURATED SWITCHING APPLICATIONS

SCHMITT TRIGGER



All Resistor Values are in Ohms
All Transistors are 2N5841
All Diodes are 1N4001
t_r = 1.0 ns

HIGH-SPEED CLOCK DRIVER



All Resistor Values are in Ohms
All Transistors are 2N5841
All Diodes are 1N4001
t_r < 1.0 ns with 50 pF Capacitive Load

V_{CE} = 4.0 Vdc, I_C = 10 mAdc

FIGURE 12 – S_{11}, INPUT REFLECTION COEFFICIENT

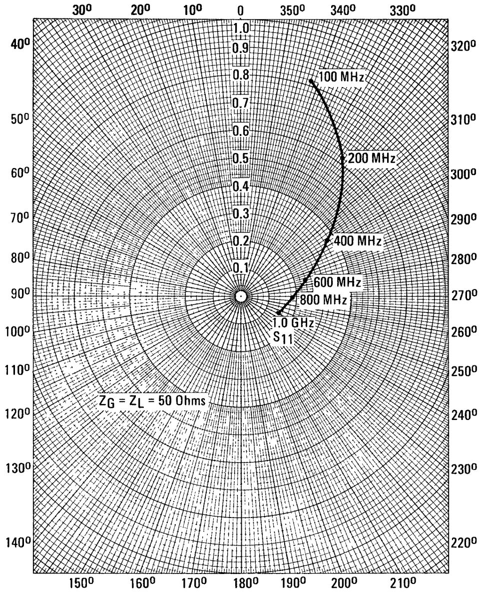


FIGURE 13 – S_{22}, OUTPUT REFLECTION COEFFICIENT

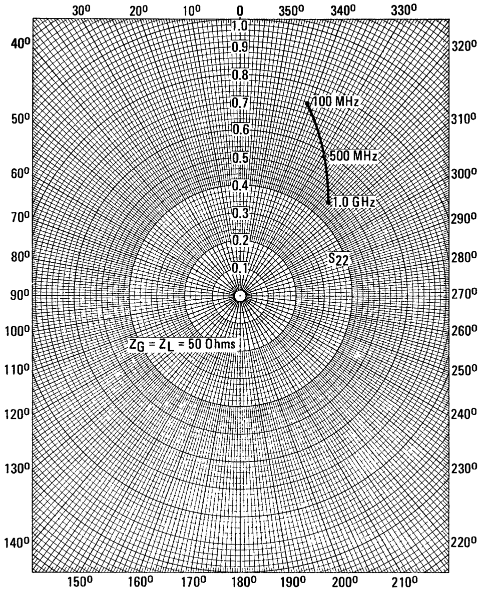


FIGURE 14 – S_{21}, FORWARD TRANSMISSION COEFFICIENT

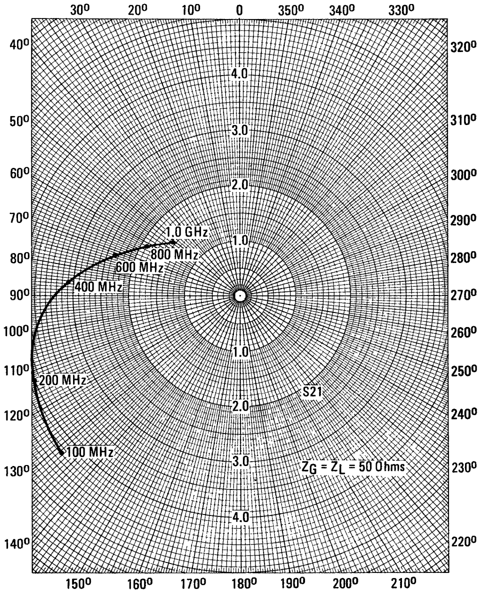
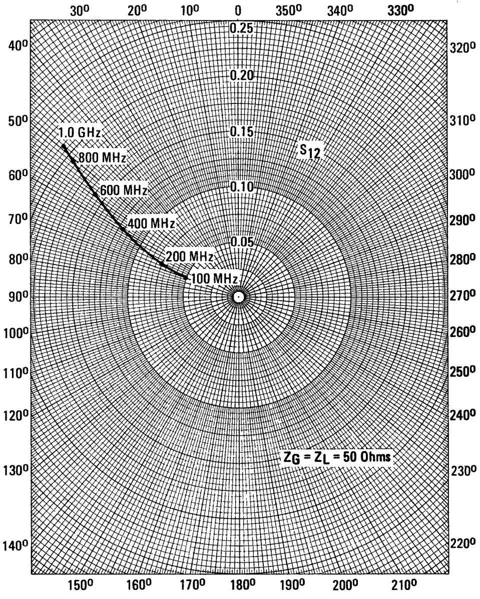


FIGURE 15 – S_{12}, REVERSE TRANSMISSION COEFFICIENT



V_{CE} = 4.0 Vdc, I_C = 10 mAdc

FIGURE 16 – S_{11}, INPUT REFLECTION COEFFICIENT

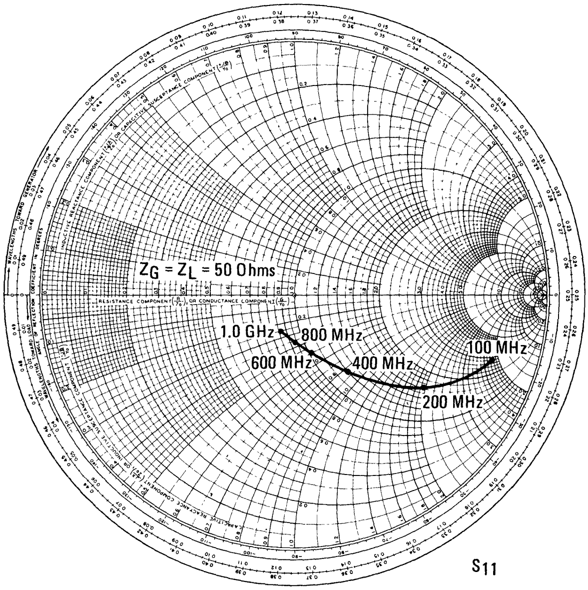
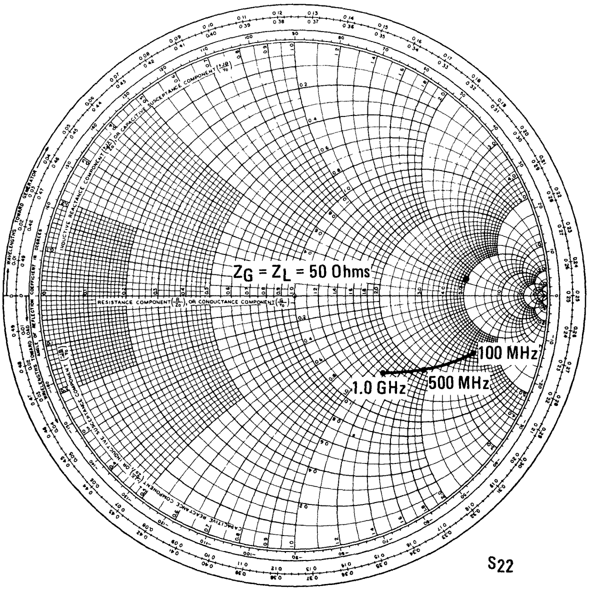


FIGURE 17 – S_{22}, OUTPUT REFLECTION COEFFICIENT



2N5845 (SILICON)
2N5845A

NPN SILICON ANNULAR TRANSISTORS

. . . designed for high-current saturated switching and core driver applications.

- Fast Switching Times @ I_C = 500 mAdc –
  t_{on} = 30 ns (Max) – 2N5845A
  40 ns (Max) – 2N5845
  t_{off} = 50 ns (Max) – 2N5845A
  60 ns (Max) – 2N5845
- High Current Gain – Bandwidth Product –
  f_T = 250 MHz (Min) – 2N5845A
  200 MHz (Min) – 2N5845
- Low Collector-Emitter Saturation Voltage – @ I_C = 500 mAdc –
  $V_{CE(sat)}$ = 0.5 Vdc (Max) – 2N5845A
  0.6 Vdc (Max) – 2N5845

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous	I_C	1.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

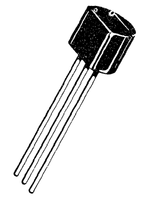
THERMAL CHARACTERISTICS

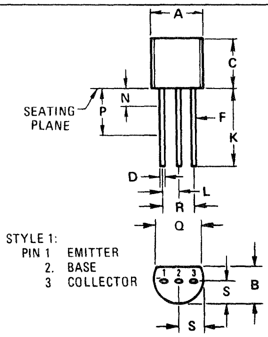
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	200	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

NPN SILICON SWITCHING TRANSISTORS





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ① (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	40	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	50	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	–	500	nAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	50	nAdc
ON CHARACTERISTICS				
DC Current Gain ①	h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		50	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)		50	200	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc) 2N5845		25	150	
2N5845A		35	150	
Collector-Emitter Saturation Voltage ①	$V_{CE(sat)}$			Vdc
(I_C = 100 mAdc, I_B = 10 mAdc)		–	0.25	
(I_C = 500 mAdc, I_B = 50 mAdc) 2N5845		–	0.6	
2N5845A		–	0.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 100 mAdc, I_B = 10 mAdc)		–	0.85	
(I_C = 500 mAdc, I_B = 50 mAdc)		0.8	1.1	
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product ②	f_T			MHz
(I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz) 2N5845		200	–	
2N5845A		250	–	
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	–	9.0	pF
Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	70	pF

SWITCHING CHARACTERISTICS

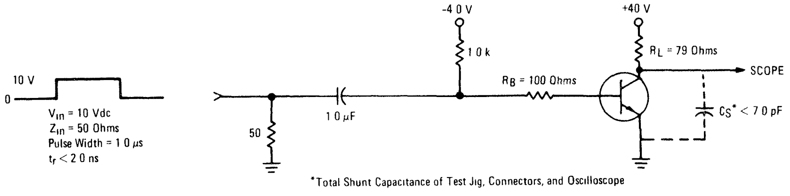
Characteristic	Conditions	Device	Symbol	Min	Max	Unit
Turn-On Time	(V_{CC} = 40 Vdc, I_C = 500 mAdc, I_{B1} = 50 mAdc, $V_{BE(off)}$ = 4.0 Vdc)	2N5845	t_{on}	–	40	ns
		2N5845A		–	30	
Delay Time		2N5845	t_d	–	17	ns
		2N5845A		–	15	
Rise Time		2N5845	t_r	–	28	ns
		2N5845A		–	25	
Turn-Off Time	(V_{CC} = 40 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc)	2N5845	t_{off}	–	60	ns
		2N5845A		–	50	
Storage Time		2N5845	t_s	–	40	ns
		2N5845A		–	38	
Fall Time		2N5845	t_f	–	30	ns
		2N5845A		–	27	

*Indicates JEDEC Registered Data.

①Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

② f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT



*Total Shunt Capacitance of Test Jig, Connectors, and Oscilloscope

TRANSIENT CHARACTERISTICS

FIGURE 2 — DELAY TIME

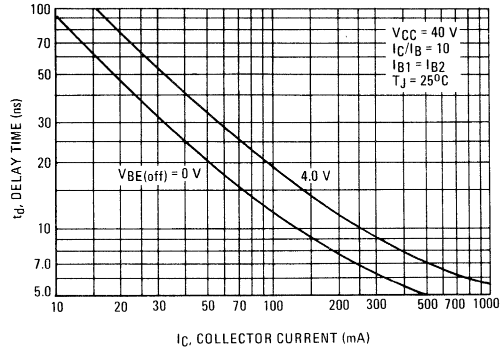


FIGURE 3 — RISE TIME

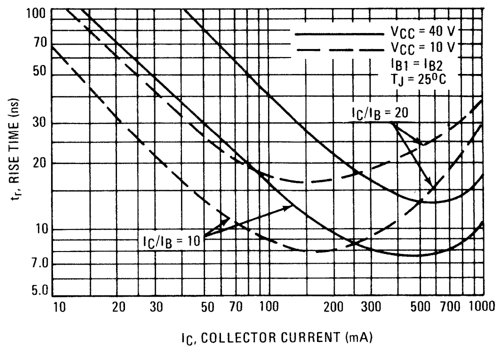


FIGURE 4 — STORAGE TIME

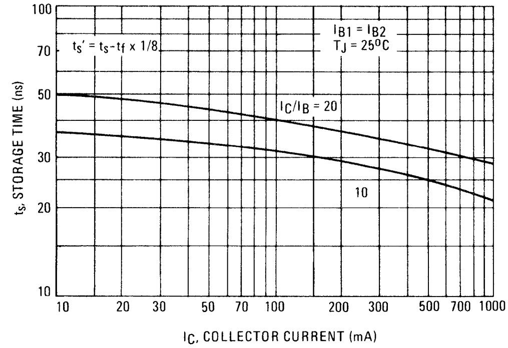


FIGURE 5 — STORAGE TIME CONTOURS

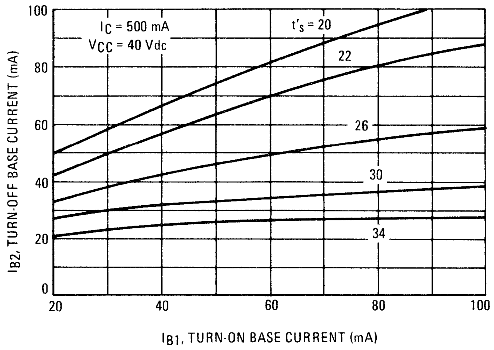


FIGURE 6 — FALL TIME

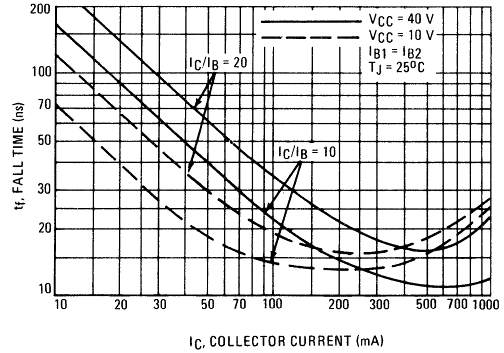
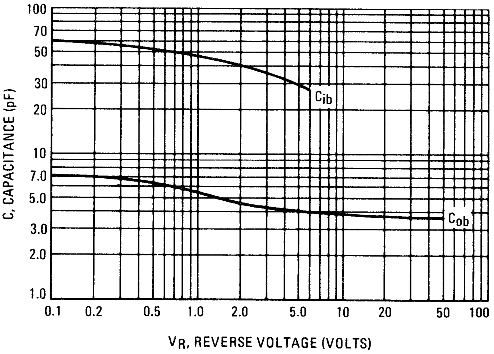


FIGURE 7 — CAPACITANCES



STATIC CHARACTERISTICS

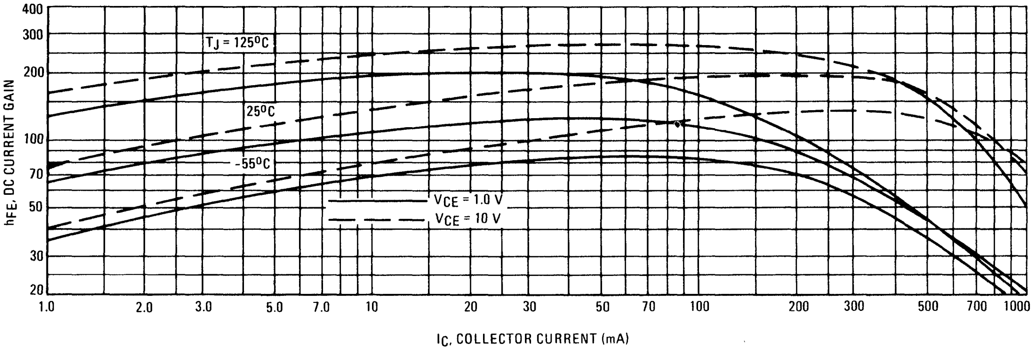


FIGURE 8 – DC CURRENT GAIN

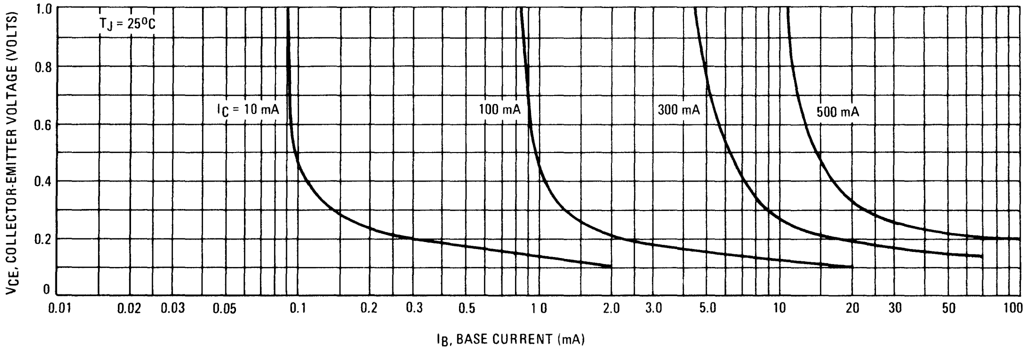


FIGURE 9 – SATURATION REGION

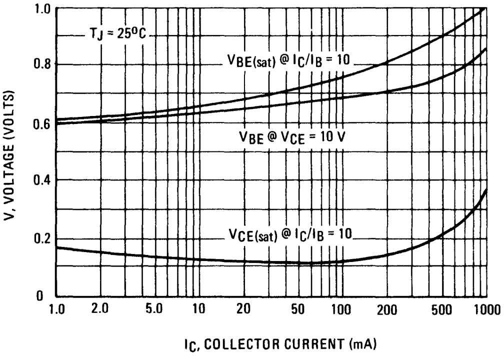


FIGURE 10 – "ON" VOLTAGES

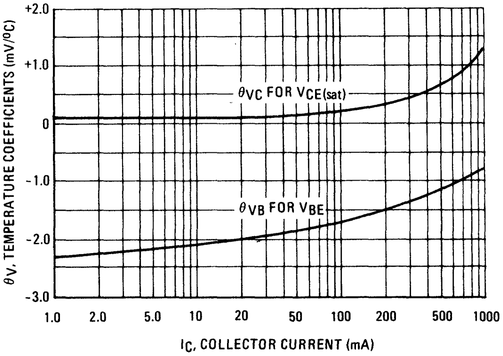
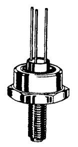


FIGURE 11 – TEMPERATURE COEFFICIENTS

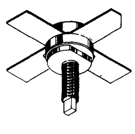
2N5846 (SILICON)
2N5847

The RF Line

3.5 W, 7.0 W – 50 MHz
RF POWER
TRANSISTORS
NPN SILICON



TO-102
CASE 24



CASE 145A-01

NPN SILICON RF POWER TRANSISTORS

. . . designed primarily for use in large-signal amplifier driver and pre-driver stages, these devices are intended for use in industrial communications equipment operating at frequencies to 80 MHz.

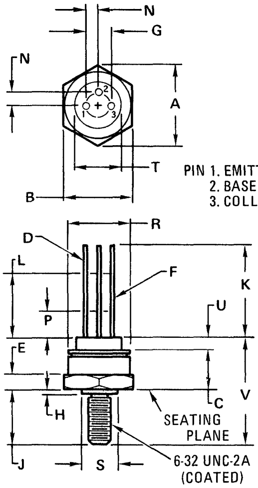
- Optimized for Operation from a 12.5 Volt Supply
- Power Output @ 12.5 Vdc, 50 MHz
  P_{out} = 3.5 W – 2N5846
  8.0 W – 2N5847
- Large-Signal Impedance Data Permit Convenient Matching Network Design

*MAXIMUM RATINGS

Rating	Symbol	2N5846	2N5847	Unit
Collector-Emitter Voltage	V_{CEO}	18		Vdc
Collector-Base Voltage	V_{CB}	36		Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	1.0	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 57.2	20 114	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

*Indicates JEDEC Registered Data.

2N5846



PIN 1. EMITTER
2. BASE
3. COLLECTOR

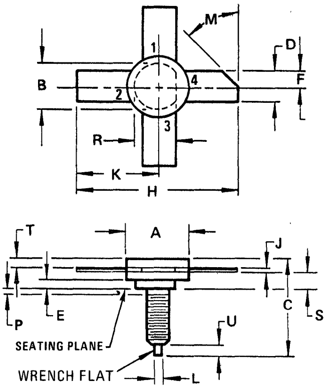
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.49	11.00	0.413	0.433
B	9.19	9.53	0.362	0.375
C	5.33	5.72	0.210	0.225
D	0.406	0.533	0.016	0.021
E	1.65	1.78	0.065	0.070
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.508	0.889	0.020	0.035
J	6.73	7.42	0.265	0.292
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050
R	8.89	9.14	0.350	0.360
S	4.45	4.83	0.175	0.190
T	4.11	4.29	0.162	0.169
U	1.14	1.52	0.045	0.060

CASE 24
TO-102

All JEDEC dimensions and notes apply

2N5847

CASE 145A-01



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	18.03	19.05	0.710	0.750
D	5.59	5.84	0.220	0.230
E	1.78	2.03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130

NOTE
CASE 145A-01 USE 8-32NC2A STUD

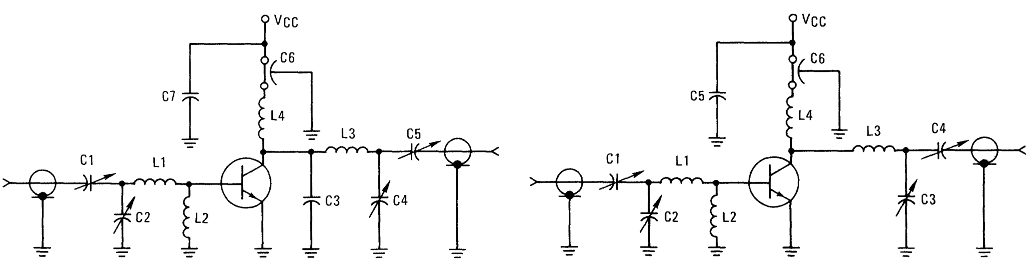
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, I_B = 0)	BV_{CEO}	18	–	Vdc
Collector-Emitter Breakdown Voltage (1) (I_C = 50 mAdc, V_{BE} = 0)	BV_{CES}	36	–	Vdc
Emitter-Base Breakdown Voltage	BV_{EBO}			Vdc
(I_E = 0.25 mAdc, I_C = 0) 2N5846		4.0	–	
(I_E = 5.0 mAdc, I_C = 0) 2N5847		4.0	–	
Collector Cutoff Current	I_{CES}			mAdc
(V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 125°C) 2N5846		–	5.0	
2N5847		–	10	
Collector Cutoff Current	I_{CBO}			mAdc
(V_{CB} = 15 Vdc, I_E = 0) 2N5846		–	0.5	
2N5847		–	1.0	
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 250 mAdc, V_{CE} = 5.0 Vdc) 2N5846		5.0	–	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc) 2N5847		5.0	–	
DYNAMIC CHARACTERISTICS				
Output Capacitance	C_{ob}			pF
(V_{CB} = 15 Vdc, I_E = 0, f = 0.1 to 1.0 MHz) 2N5846		–	25	
2N5847		–	90	
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain	G_{PE}			dB
(V_{CC} = 12.5 Vdc, P_{out} = 3.5 W, f = 50 MHz) 2N5846		10	–	
(V_{CC} = 12.5 Vdc, P_{out} = 8.0 W, f = 50 MHz) 2N5847		10	–	
Power Output	P_{out}			Watts
(V_{CC} = 12.5 Vdc, P_{in} = 350 mW, f = 50 MHz) 2N5846		3.5	–	
(V_{CC} = 12.5 Vdc, P_{in} = 800 mW, f = 50 MHz) 2N5847		8.0	–	
Collector Efficiency	η			%
(V_{CC} = 12.5 Vdc, P_{out} = 3.5 W, f = 50 MHz) 2N5846		50	–	
(V_{CC} = 12.5 Vdc, P_{out} = 8.0 W, f = 50 MHz) 2N5847		50	–	

*Indicates JEDEC Registered Data.

(1)Pulsed thru a 25 mH inductor.

FIGURE 1 – 50 MHz TEST CIRCUITS


2N5846 2N5847

C1, C2, C5	25-280 pF, Arco 464 or Equivalent
C3	40 pF, 500 Vdc, Unelco
C4	9.0 -180 pF, Arco 463 or Equivalent
C6	1000 pF Feedthru
C7	0.1 µF, 75 Vdc
L1	2 Turns, #18 AWG, 3/8" I.D.
L2	Small Ferrite Bead, 2½ Turns
L3	5 Turns, #18 AWG, 3/8" I.D.
L4	1.0 µH, RF Choke

C1, C3, C4	25-280 pF, Arco 464 or Equivalent
C2	80-480 pF, Arco 466 or Equivalent
C5	0.1 µF, 75 Vdc
C6	1000 pF Feedthru
L1	1 Turn, #14 AWG ½" I.D.
L2	Large Ferrite Bead 2½ Turns
L3	3 Turns, #14 AWG ½" I.D.
L4	20 Turns, #18 AWG NYCLAD Wire, 2 Layers (10 Turns Per Layer) ¼" I.D.

POWER OUTPUT versus POWER INPUT

FIGURE 2 – 2N5846

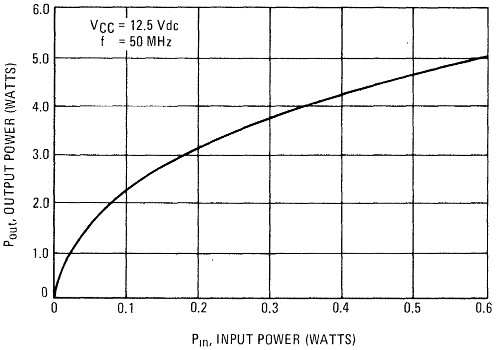
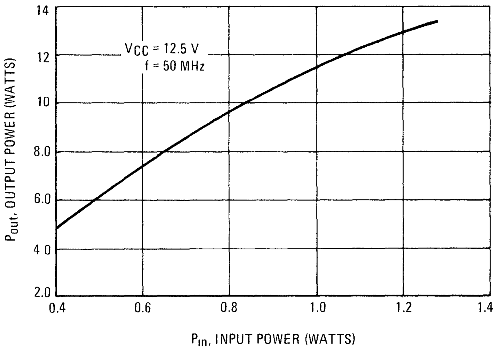


FIGURE 3 – 2N5847



POWER OUTPUT versus FREQUENCY

FIGURE 4 – 2N5846

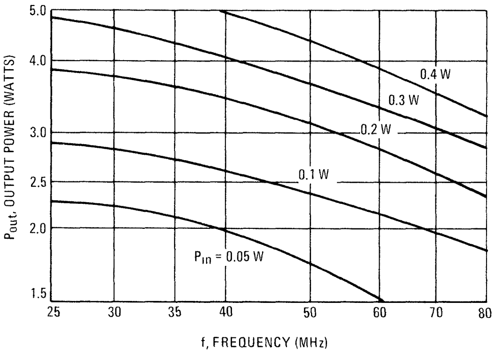
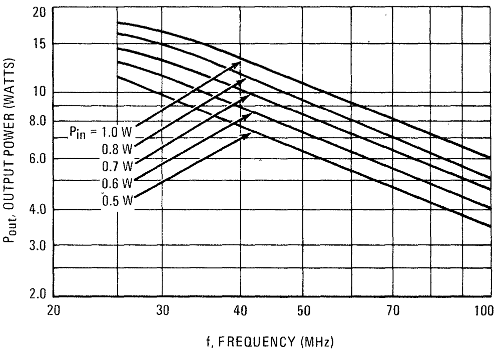


FIGURE 5 – 2N5847



POWER DISSIPATION DERATING CURVES

FIGURE 6 – 2N5846

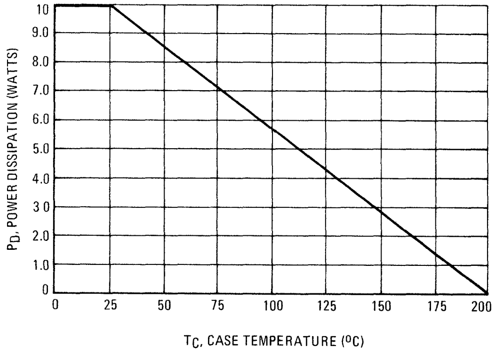
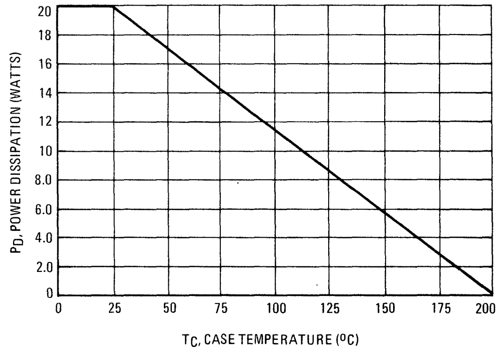


FIGURE 7 – 2N5847



PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

FIGURE 8 – 2N5846

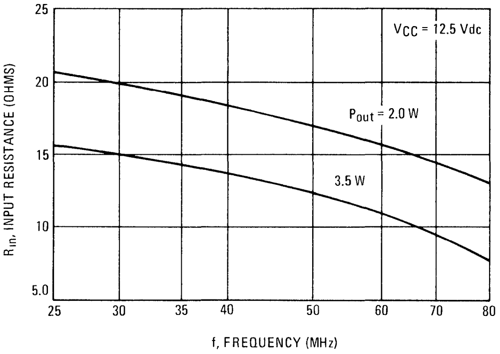
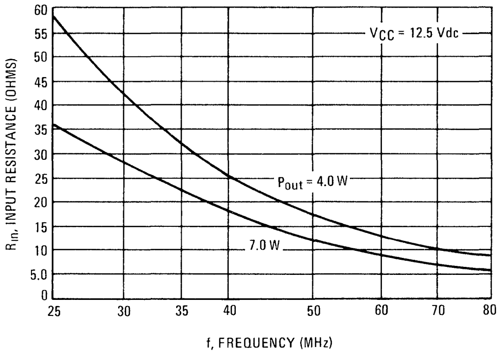


FIGURE 9 – 2N5847



PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

FIGURE 10 – 2N5846

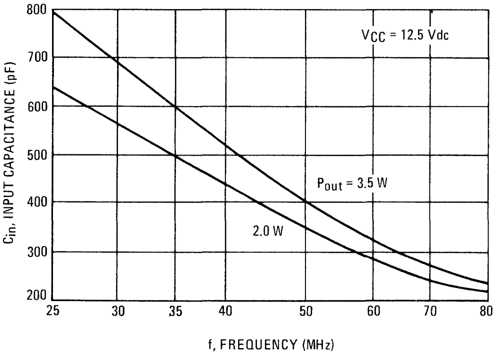
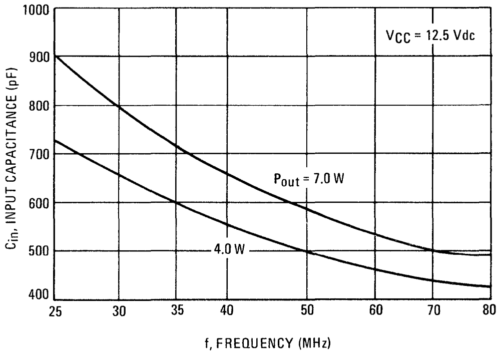


FIGURE 11 – 2N5847



PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

FIGURE 12 – 2N5846

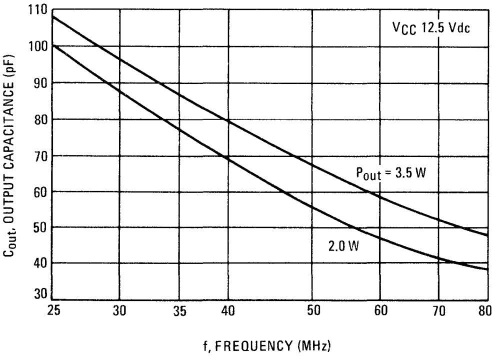
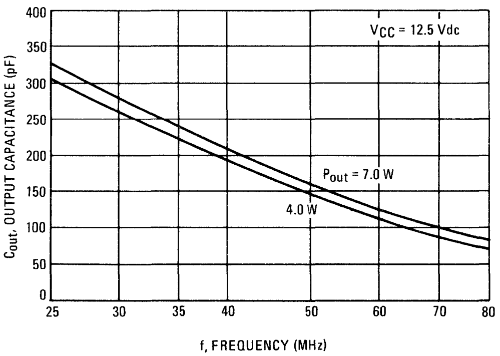


FIGURE 13 – 2N5847



2N5848 (SILICON)

The RF Line

NPN SILICON RF POWER TRANSISTOR

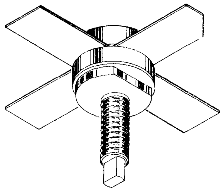
. . . designed primarily for use in large-signal amplifier driver and output stages, the 2N5848 is intended for use in industrial communications equipment operating at frequencies to 80 MHz.

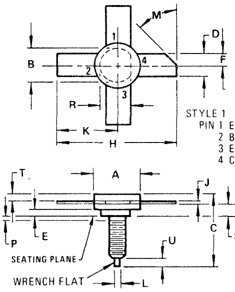
- Optimized for Operation from a 12.5 Volt Supply
- 20 Watts (Min) RF Power Output at 50 MHz
- Balanced Emitter Construction for Burn Out Protection

20 W-50 MHz

RF POWER TRANSISTOR

NPN SILICON





STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	18.03	19.05	0.710	0.750
D	5.59	5.84	0.220	0.230
E	1.78	2.03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130

NOTE
CASE 145A-01 USE 8-32NC2A STUD

CASE 145A-01

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	24	Vdc
Collector-Base Voltage	V_{CB}	48	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	3.5	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25°C	P_D	50 285	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C
Stud Torque (1)	–	6.5	in-lbs.

*Indicates JEDEC Registered Data.

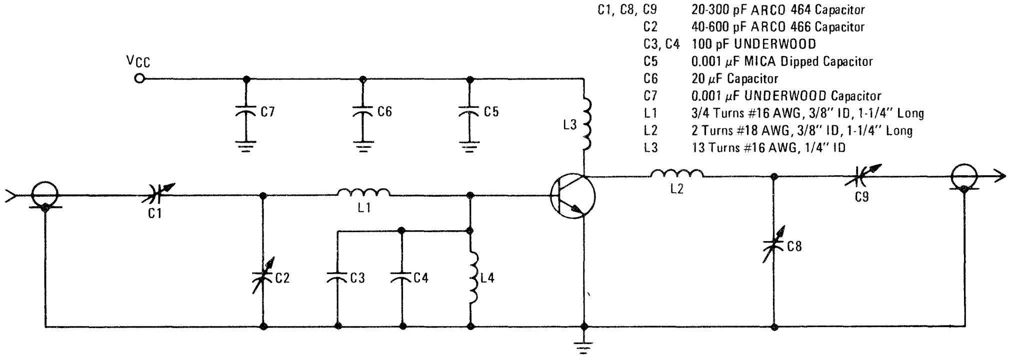
(1) For repeated assembly use 5 in-lbs.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	BV_{CEO}	24	–	–	Vdc
Collector-Emitter Breakdown Voltage(1) (I_C = 50 mAdc, V_{BE} = 0)	BV_{CES}	48	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_A = +125°C)	I_{CES}	–	–	10	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.2 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	3.0	15	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{ob}	–	100	125	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 20 W, V_{CC} = 12.5 Vdc, I_C = 3.2 Adc, f = 50 MHz)	G_{PE}	8.0	–	–	dB
Collector Efficiency (P_{out} = 20 W, V_{CC} = 12.5 Vdc, I_C = 3.2 Adc, f = 50 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data.
(1)Pulsed thru a 25 mH Inductor.

FIGURE 1 – 50 MHz POWER GAIN TEST CIRCUIT



C1, C8, C9	20-300 pF ARCO 464 Capacitor
C2	40-600 pF ARCO 466 Capacitor
C3, C4	100 pF UNDERWOOD
C5	0.001 μF MICA Dipped Capacitor
C6	20 μF Capacitor
C7	0.001 μF UNDERWOOD Capacitor
L1	3/4 Turns #16 AWG, 3/8" ID, 1-1/4" Long
L2	2 Turns #18 AWG, 3/8" ID, 1-1/4" Long
L3	13 Turns #16 AWG, 1/4" ID

FIGURE 2 – OUTPUT POWER versus INPUT POWER

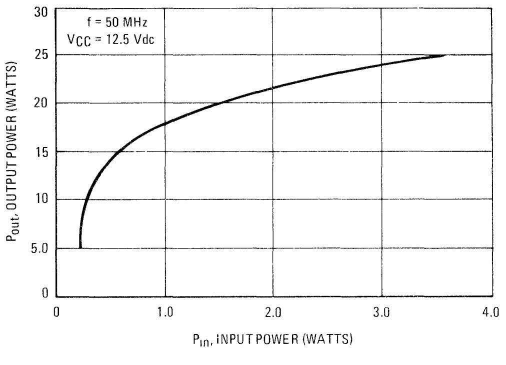


FIGURE 3 – OUTPUT POWER versus FREQUENCY

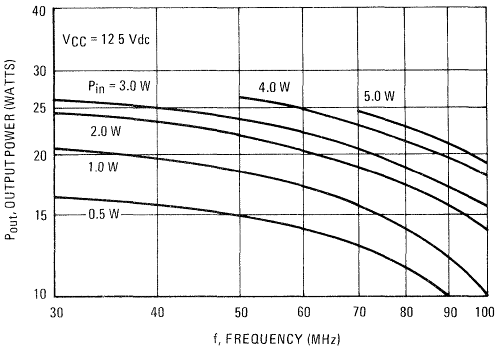


FIGURE 4 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

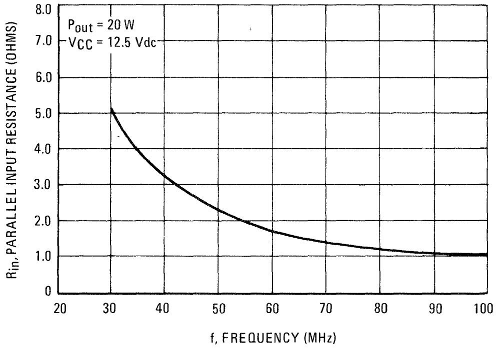


FIGURE 5 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

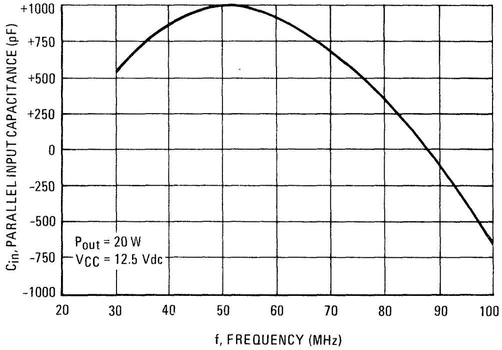


FIGURE 6 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

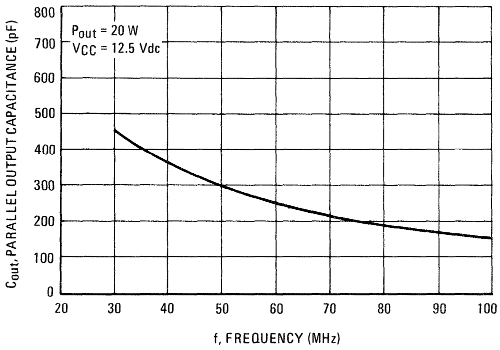
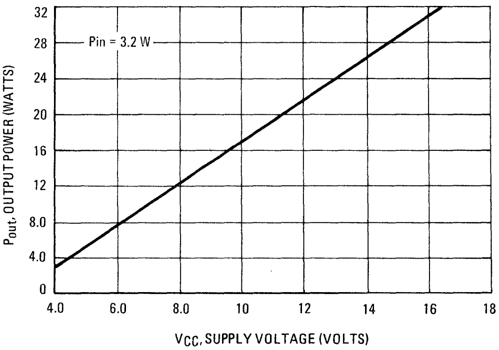
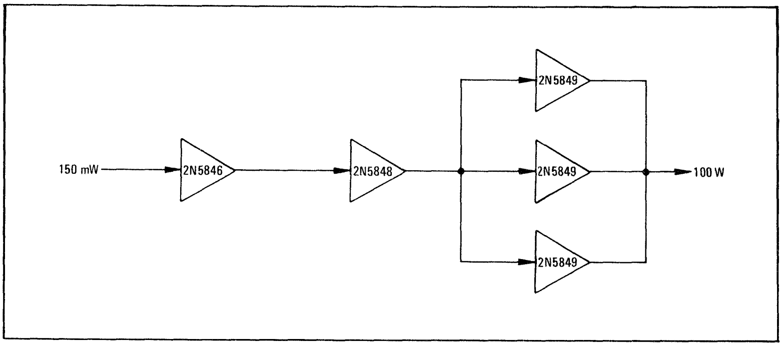


FIGURE 7 – OUTPUT POWER versus SUPPLY VOLTAGE



LOW-BAND FM (25-50 MHz) 12.5 Vdc, 100 WATT AMPLIFIER



2N5849 (SILICON)

NPN SILICON RF POWER TRANSISTOR

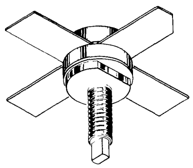
. . . designed primarily for use in large-signal amplifier output stages, the 2N5849 is intended for use in industrial communications equipment operating at frequencies to 80 MHz.

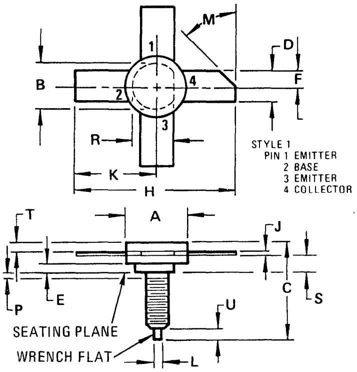
- Optimized for Operation from a 12.5 Volt Supply
- 40 Watts (Min) RF Power Output at 50 MHz
- Balanced Emitter Construction for Burn Out Protection

40 W-50 MHz

RF POWER TRANSISTOR

NPN SILICON





STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.57	12.90	0.459	0.508
B	10.54	10.80	0.415	0.425
C	21.21	21.46	0.835	0.845
D	5.59	5.84	0.220	0.230
E	1.83	1.98	0.072	0.078
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.65	1.90	0.065	0.075
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	9.78	10.01	0.385	0.394
S	3.89	4.45	0.153	0.175
T	2.03	2.29	0.080	0.090
U	2.54	3.30	0.100	0.130

NOTE: 145A-02 USES 10-32NF2A STUD.

CASE 145A-02

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	24	Vdc
Collector-Base Voltage	V_{CB}	48	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	7.0	Adc
Total Device Dissipation @ $T_C = 25^{\circ}C$ Derate above 25°C	P_D	100 571	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

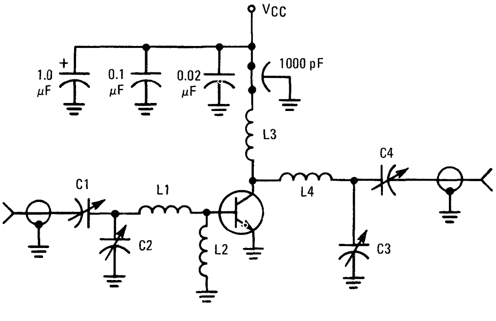
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 200 mAdc, I_B = 0)	BV_{CEO}	24	–	–	Vdc
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, V_{BE} = 0)	BV_{CES}	48	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_A = +125°C)	I_{CES}	–	–	10	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.4 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	3.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{ob}	–	180	230	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 50 MHz)	G_{PE}	7.5	–	–	dB
Collector Efficiency (P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 50 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data.

(1)Pulsed thru a 25 mH Inductor.

FIGURE 1 — 50 MHz POWER GAIN TEST CIRCUIT



C1	25-280 pF, Arco 464 or Equivalent
C2	80-480 pF, Arco 466 or Equivalent
C3	0-75 pF, Hammarlund MAPC 75 or Equivalent
C4	0-50 pF, Hammarlund MAPC 50 or Equivalent
L1	1 Turn #14 AWG 5/16" I.D.
L2	2-1/2 Turns #22 AWG on 3/8" Ferrite Bead
L3	18 Turns #18 AWG 3/8" I.D. 2 Layers, 9 Turns Each
L4	4 Turns #14 AWG 7/16" I.D. 7/16" Long

FIGURE 2 – POWER OUTPUT versus POWER INPUT

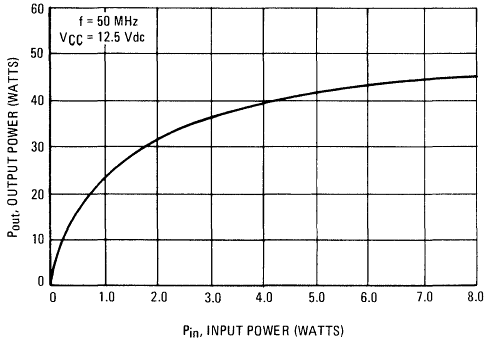


FIGURE 3 – POWER OUTPUT versus FREQUENCY

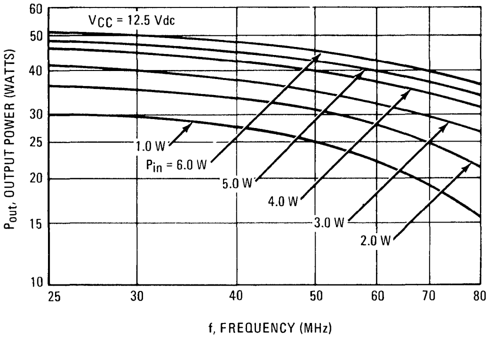


FIGURE 4 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

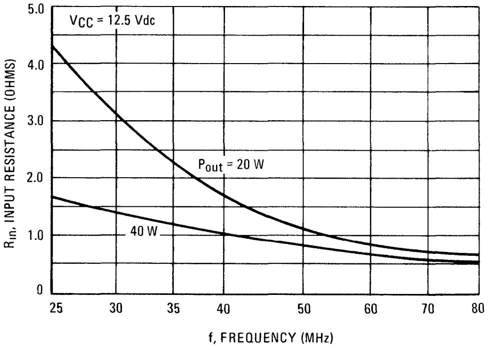


FIGURE 5 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

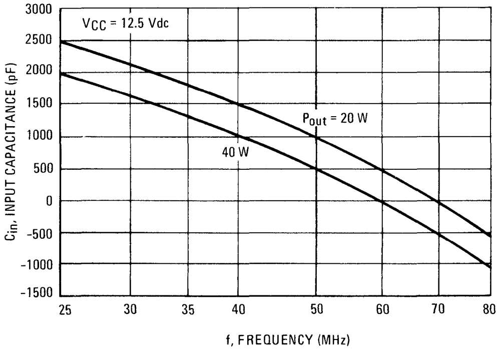


FIGURE 6 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

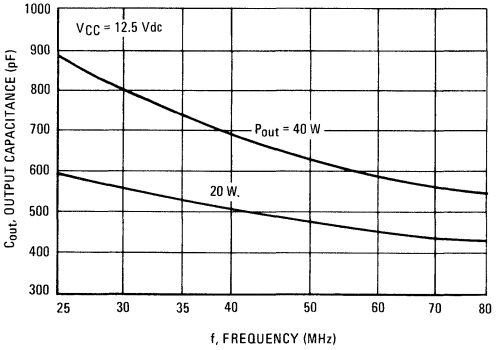
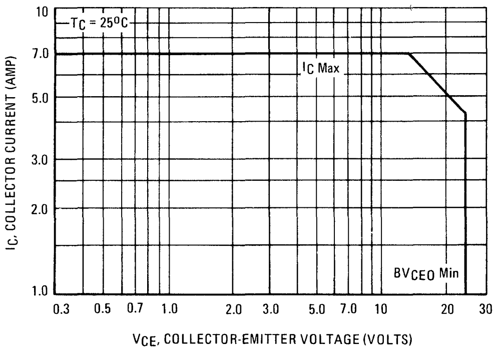
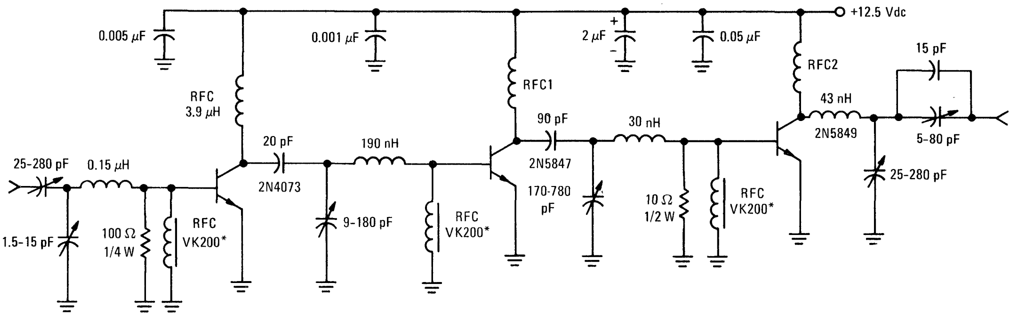


FIGURE 7 – DC SAFE OPERATING AREA



40 WATT, 50 MHz TRANSMITTER SCHEMATIC

(Information obtained from AN-502A)



P_o = 40 W
P_{in} = 20 mW
Overall Gain = 33 dB
Overall Efficiency = 59.2%

*Ferroxcube Part Number
RFC1 – 20 Turns #18 AWG, 3/16" I.D., 2 Layers, 10 Turns Each, Close Wound.
RFC2 – 18 Turns, #18 AWG, 3/16" I.D., 2 Layers, 9 Turns Each, Close Wound.

APPLICATION INFORMATION

In addition to a fine selection of quality RF Semiconductors, Motorola provides applications information in the form of Application Notes. Any of the notes listed on this page may be obtained by writing to the Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20924, Phoenix, Arizona 85036.

AN-267	Matching Network Designs with Computer Solutions
AN-282A	Systemizing RF Power Amplifier Design
AN-481	A Broadband 4-Watt Aircraft Transmitter
AN-495	A 25-Watt, 175-MHz Transmitter for 12.5-Volt Operation
AN-502A	A 40-Watt, 50-MHz Transmitter for 12.5-Volt Operation
AN-507	A 13-Watt Broadband AM Aircraft Transmitter

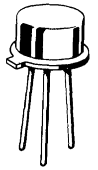
2N5859 (SILICON)

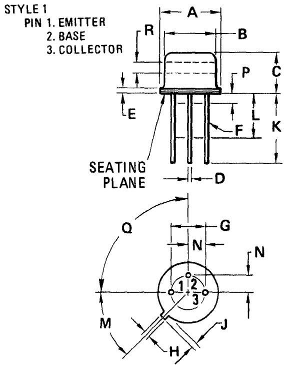
NPN SILICON ANNULAR SWITCHING TRANSISTOR

. . . designed for high-current, high-speed switching applications. Ideally suited for ferrite core and plated wire memory driver, hammer driver, or MOS translator applications.

- Excellent Current-Gain – Bandwidth Product –
  f_T = 250 MHz (Min) @ I_C = 50 mAdc
- Low Collector-Base Capacitance –
  C_{cb} = 7.0 pF (Max) @ V_{CB} = 10 Vdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.0 Adc
- Fast Switching Times @ I_C = 1.0 Adc
  t_{on} = 35 ns (Max)
  t_{off} = 60 ns (Max)

NPN SILICON
SWITCHING
TRANSISTOR





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 5.72	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	175	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	35	°C/W

*Indicates JEDEC Registered Data

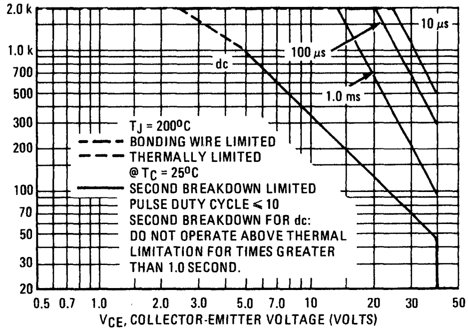
***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	40	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	80	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current	I_{CEX}			μAdc
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 2.0 Vdc)		–	0.2	
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_A = 75°C)		–	5.0	
Collector Cutoff Current	I_{CBO}			μAdc
(V_{CB} = 50 Vdc, I_E = 0)		–	0.25	
(V_{CB} = 50 Vdc, I_E = 0, T_A = 75°C)		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		30	120	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		15	100	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc, T_A = −55°C)		10	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)		–	0.4	
(I_C = 1.0 Adc, I_B = 100 mAdc)		–	0.7	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)		0.8	1.0	
(I_C = 1.0 Adc, I_B = 100 mAdc)		0.9	1.25	
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	250	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	–	7.0	pF
Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	60	pF
SWITCHING CHARACTERISTICS				
Turn-On Time (V_{CC} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, I_C = 1.0 Adc, I_{B1} = 100 mAdc) (Figures 8 and 10)	t_{on}	–	35	ns
Delay Time (V_{CC} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, I_C = 1.0 Adc, I_{B1} = 100 mAdc) (Figures 8 and 10)	t_d	–	6.0	ns
Rise Time (V_{CC} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, I_C = 1.0 Adc, I_{B1} = 100 mAdc) (Figures 8 and 10)	t_r	–	30	ns
Turn-Off Time (V_{CC} = 30 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc) (Figures 9 and 11)	t_{off}	–	60	ns
Storage Time (V_{CC} = 30 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc) (Figures 9 and 11)	t_s	–	35	ns
Fall Time (V_{CC} = 30 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc) (Figures 9 and 11)	t_f	–	35	ns

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2.0%.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL DC CHARACTERISTICS

FIGURE 2 – DC CURRENT GAIN

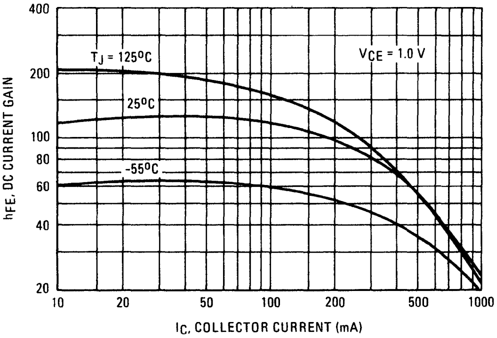


FIGURE 3 – "ON" VOLTAGES

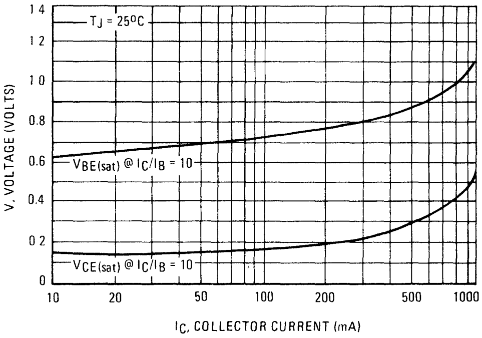


FIGURE 4 – COLLECTOR SATURATION REGION

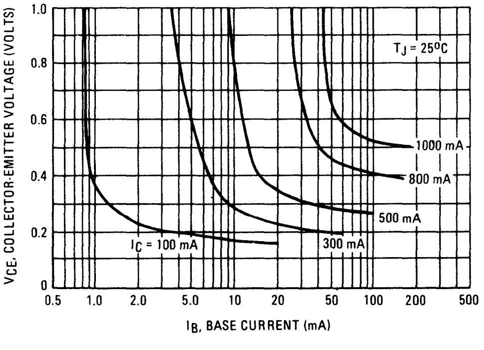
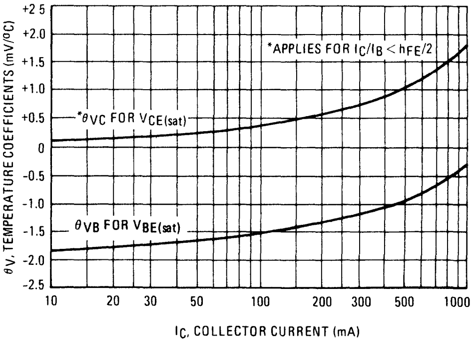


FIGURE 5 – TEMPERATURE COEFFICIENTS



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 6 – CURRENT-GAIN–BANDWIDTH PRODUCT

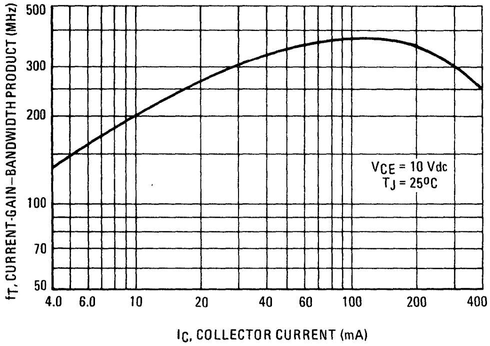


FIGURE 7 – CAPACITANCE

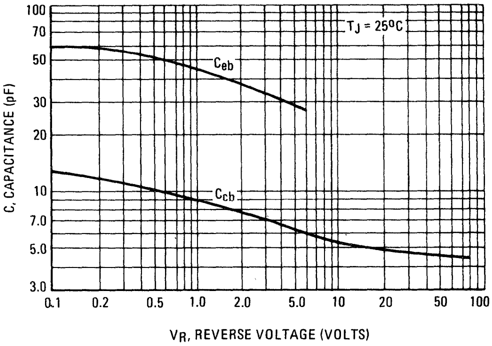


FIGURE 8 – TURN-ON TIME

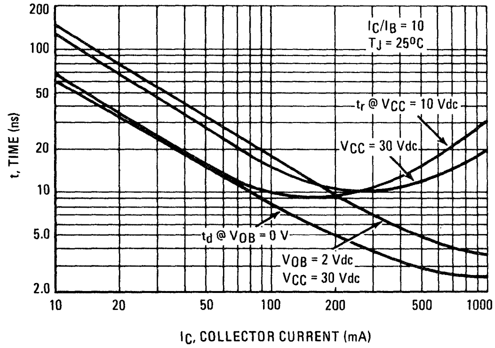


FIGURE 9 – TURN-OFF TIME

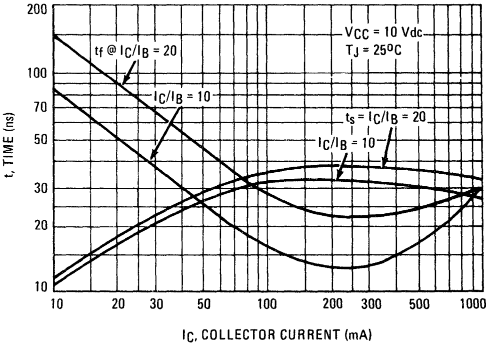
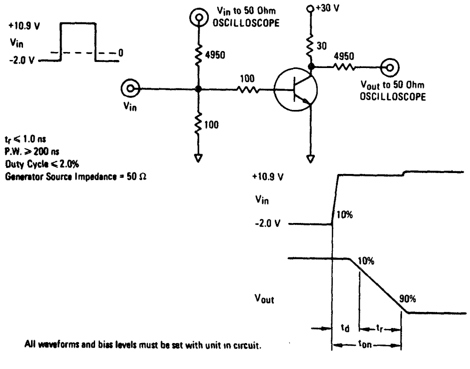
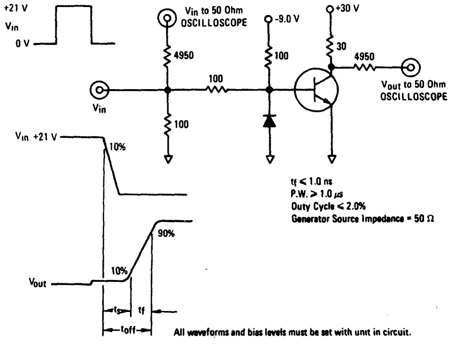


FIGURE 10 – TURN-ON TIME TEST CIRCUIT



All waveforms and bias levels must be set with unit in circuit.

FIGURE 11 – TURN-OFF TIME TEST CIRCUIT



All waveforms and bias levels must be set with unit in circuit.

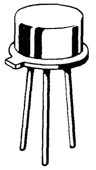
2N5861 (SILICON)

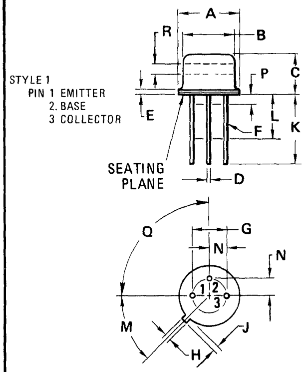
NPN SILICON ANNULAR MEMORY DRIVER

. . . designed for medium-current, high-speed switching applications. Ideally suited for ferrite core memory driver circuits.

- Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 50 Vdc (Min) @ I_C = 10 mAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 500 mAdc
- Low Collector-Base Capacitance –
  C_{cb} = 7.0 pF (Max) @ V_{CB} = 10 Vdc
- Fast Switching Times @ I_C = 500 mAdc –
  t_{on} = 25 ns (Max)
  t_{off} = 60 ns (Max)

NPN SILICON MEMORY DRIVER TRANSISTOR





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous	I_C	2.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 6.0	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	50	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	100	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current	I_{CEV}			μAdc
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 2.0 Vdc)		–	0.3	
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_A = 75°C)		–	10	
Collector Cutoff Current	I_{CBO}			μAdc
(V_{CB} = 50 Vdc, I_E = 0)		–	0.3	
(V_{CB} = 50 Vdc, I_E = 0, T_A = +75°C)		–	10	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		25	100	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc, T_A = -55°C)		10	–	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{BE(sat)}$	0.8	1.1	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	200	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	–	7.0	pF
Emitter-Base Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	60	pF
SWITCHING CHARACTERISTICS				
Turn-On Time (V_{CC} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, I_C = 500 mAdc, I_{B1} = 50 mAdc) (Figure 5)	t_{on}	–	25	ns
Delay Time	t_d	–	8.0	ns
Rise Time	t_r	–	18	ns
Turn-Off Time (V_{CC} = 30 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc) (Figure 6)	t_{off}	–	60	ns
Storage Time	t_s	–	35	ns
Fall Time	t_f	–	35	ns

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width≤300 μs, Duty Cycle≤2.0%.

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN–BANDWIDTH PRODUCT

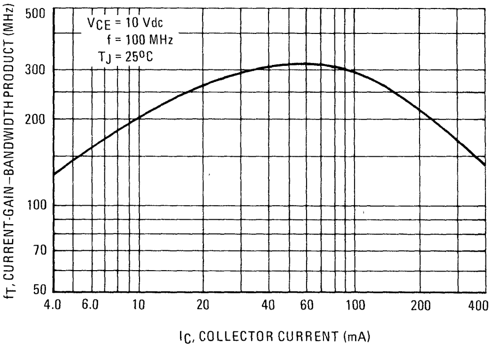
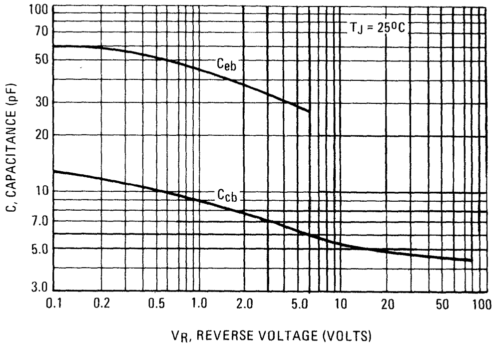


FIGURE 2 – CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 3 – TURN-ON TIME

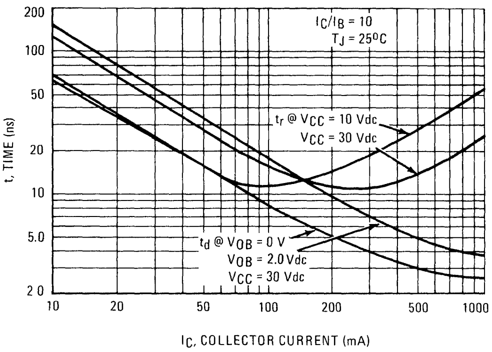


FIGURE 4 – TURN-OFF TIME

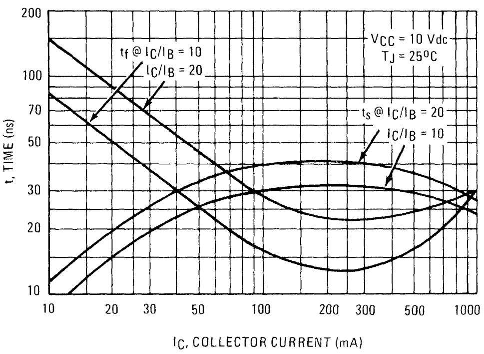
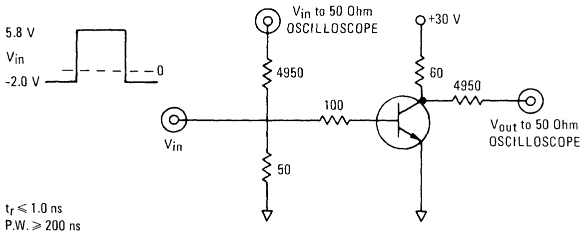
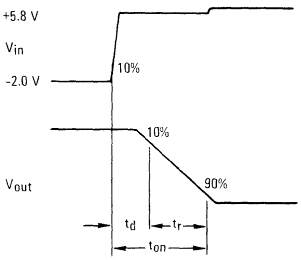


FIGURE 5 – TURN-ON TIME TEST CIRCUIT

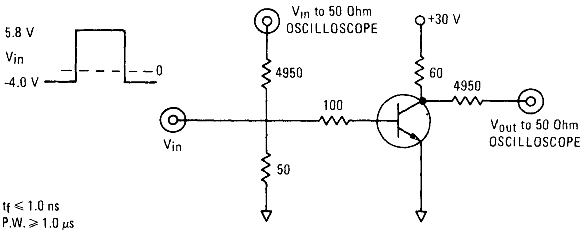


$t_r \leq 1.0$ ns
P.W. ≥ 200 ns
Duty Cycle ≤ 2.0%
Generator Source Impedance = 50 Ω
Pulse Generator: EH1421 Timing Unit and 1121 Pulse Driver
Oscilloscope: Tektronix 661 Sampling Scope

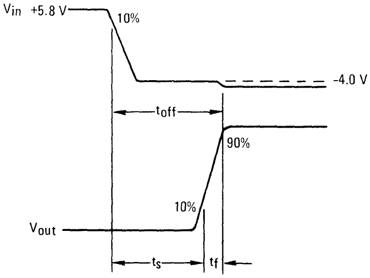


V_{in} during t_{on} interval must be +5 8 V.
All waveforms and bias levels must be set with unit in circuit.

FIGURE 6 – TURN-OFF TIME TEST CIRCUIT



$t_f \leq 1.0$ ns
P.W. ≥ 1.0 μs
Duty Cycle ≤ 2.0%
Generator Source Impedance = 50 Ω
Pulse Generator: EH1421 Timing Unit and 1121 Pulse Driver
Oscilloscope: Tektronix 661 Sampling Scope



V_{in} during t_{off} interval must be -4.0 V.
All waveforms and bias levels must be set with unit in circuit.

FIGURE 7 – DC CURRENT GAIN

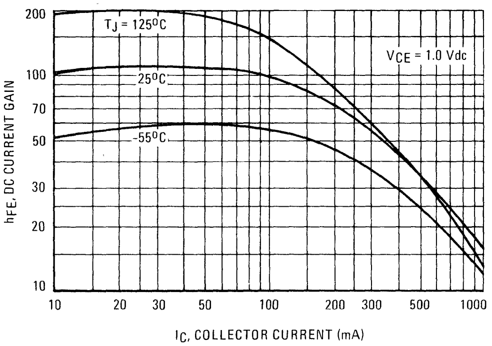


FIGURE 8 – "ON" VOLTAGES

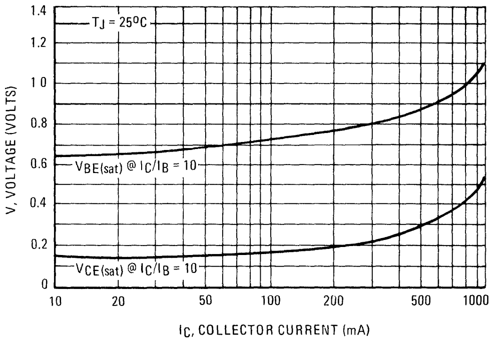
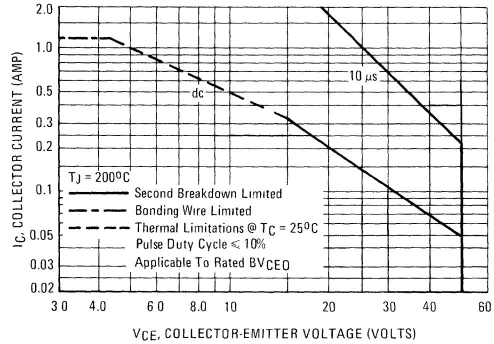


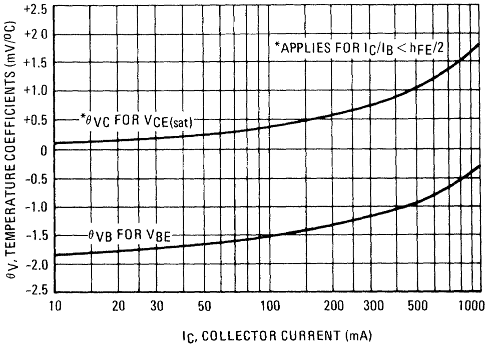
FIGURE 9 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 12 – TEMPERATURE COEFFICIENTS



2N5862 (SILICON)

The RF Line

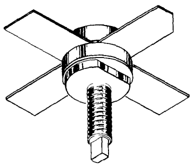
NPN SILICON RF POWER TRANSISTOR

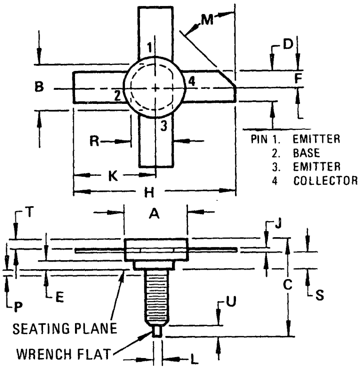
. . . designed for VHF power amplifier applications in military and industrial equipment. Particularly suited for use in Class AB, B, or C amplifier applications to 175 MHz.

- High Output Power Capability –
  90 Watts Peak Output for 15 Watts (Typ) Input @ f = 150 MHz
- Balanced Emitter Construction to Provide the Designer with the device Technology that Assures Ruggedness and Resists Transistor Damage Caused by Load Mismatch.
- Stripline Packaging for Lower Lead Inductance and Better Broadband Capability

90 WATTS PEAK - 150 MHz

**NPN SILICON
RF POWER
TRANSISTOR**





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.57	12.90	0.459	0.508
B	10.54	10.80	0.415	0.425
C	21.21	21.46	0.835	0.845
D	5.59	5.84	0.220	0.230
E	1.83	1.98	0.072	0.078
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.65	1.90	0.065	0.075
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	9.78	10.01	0.385	0.394
S	3.89	4.45	0.153	0.175
T	2.03	2.29	0.080	0.090
U	2.54	3.30	0.100	0.130

NOTE: 145A-02 USES 10-32NF2A STUD.

CASE 145A-02

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	65	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	8.0	Adc
Total Device Dissipation @ T_C=50°C Derate above 50°C	P_D	80 533	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data

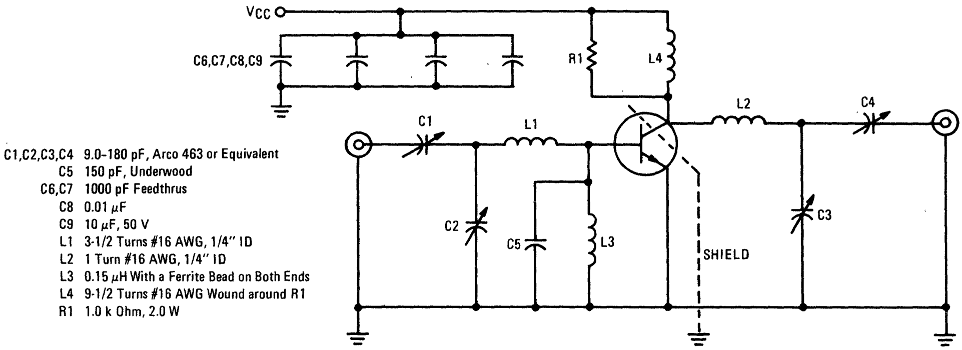
* ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ① (I_C = 200 mAdc, I_B = 0)	BV_{CEO}	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	BV_{CES}	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0, T_C = 125°C)	I_{CES}	–	–	10	mAdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{ob}	–	90	130	pF
FUNCTIONAL TEST (Circuit Tuned at 90 Watts Peak, V_{CC} = 27 Vdc and not retuned for 13.5 Vdc Carrier Power Test)					
Power Input (P_{out} = 90 W Peak, V_{CC} = 27 Vdc, f = 150 MHz, 33.3% Duty Cycle Square Wave, Power Source Modulated)	$P_{in(peak)}$	–	15	–	Watts
Power Gain CW (Carrier Power) (P_{out} = 24 W, V_{CC} = 13.5 Vdc, f = 150 MHz, Circuit Tuned at 90 W Peak, V_{CC} = 27 Vdc)	G_{PE}	5.0	–	–	dB
Power Gain (V_{CC} = 27 Vdc, f = 150 MHz, P_{out} = 75 W, I_C = 4.1 Adc, Circuit Tuned at 90 W Peak, V_{CC} = 27 Vdc)	G_{PE}	7.0	–	–	dB
Collector Efficiency (P_{out} = 75 W, V_{CC} = 27 Vdc, f = 150 MHz, I_C = 4.1 Adc)	η	60	–	–	%
Load Mismatch (P_{out} = 75 W, CW, V_{CC} = 27 Vdc, f = 150 MHz, 10% Duty Cycle, 10 ms Pulse, VSWR 10:1, all angles)	Less Than 5% Change in Power Readings Before and After Mismatch Tests.				

① **Pulsed through 25 mH Inductor.**

*Indicates JEDEC Registered Data

FIGURE 1 — 150 MHz TEST CIRCUIT



C1,C2,C3,C4	9.0-180 pF, Arco 463 or Equivalent
C5	150 pF, Underwood
C6,C7	1000 pF Feedthrus
C8	0.01 µF
C9	10 µF, 50 V
L1	3-1/2 Turns #16 AWG, 1/4" ID
L2	1 Turn #16 AWG, 1/4" ID
L3	0.15 µH With a Ferrite Bead on Both Ends
L4	9-1/2 Turns #16 AWG Wound around R1
R1	1.0 k Ohm, 2.0 W

OUTPUT POWER versus FREQUENCY

FIGURE 2 – V_{CC} = 13.5 Vdc

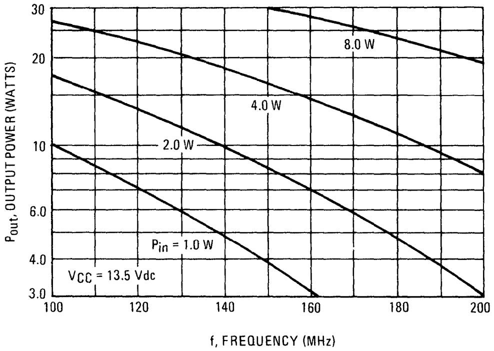


FIGURE 3 – V_{CC} = 27 Vdc

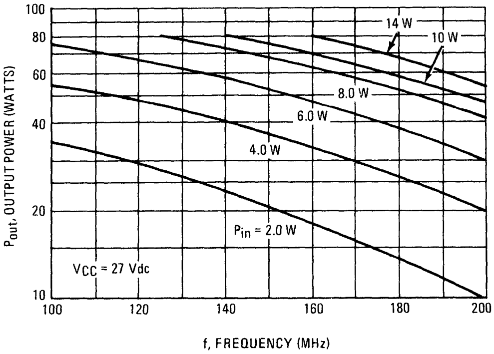


FIGURE 4 – OUTPUT POWER versus INPUT POWER

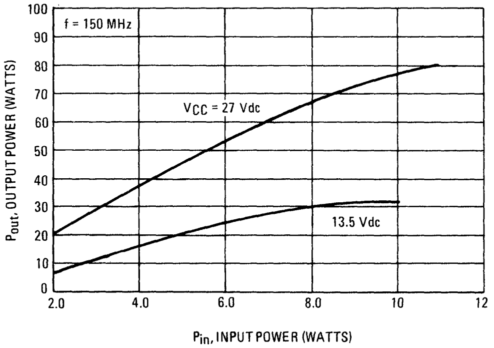
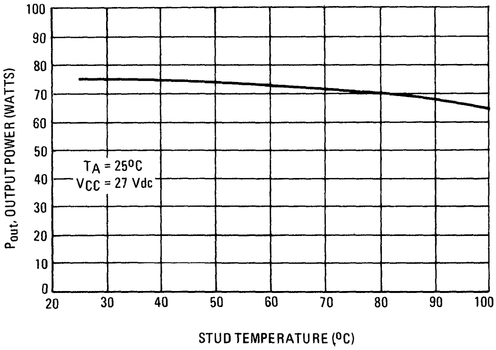


FIGURE 5 – OUTPUT POWER versus STUD TEMPERATURE



PARALLEL INPUT RESISTANCE versus FREQUENCY

FIGURE 6 – V_{CC} = 13.5 Vdc, P_{out} = 25 W

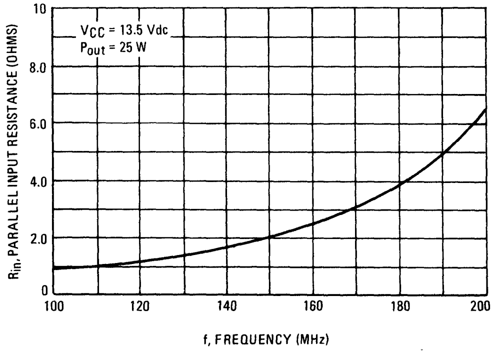
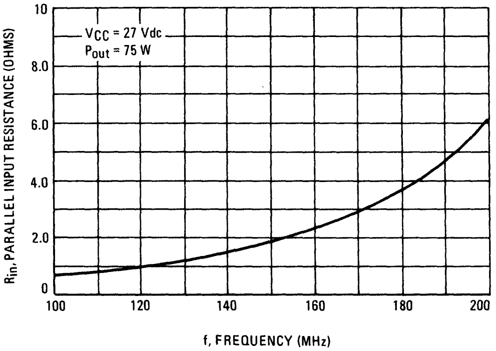


FIGURE 7 – V_{CC} = 27 Vdc, P_{out} = 75 W



PARALLEL INPUT CAPACITANCE versus FREQUENCY

FIGURE 8 – V_{CC} = 13.5 Vdc, P_{out} = 25 W

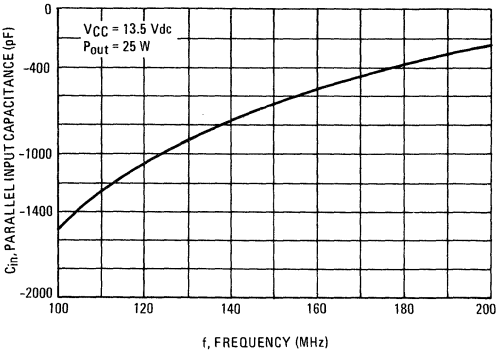
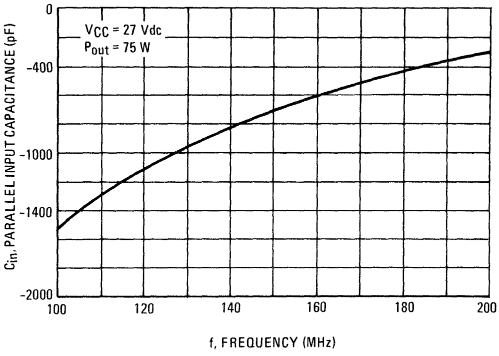


FIGURE 9 – V_{CC} = 27 Vdc, P_{out} = 75 W



PARALLEL OUTPUT CAPACITANCE versus FREQUENCY

FIGURE 10 – V_{CC} = 13.5 Vdc, P_{out} = 25 W

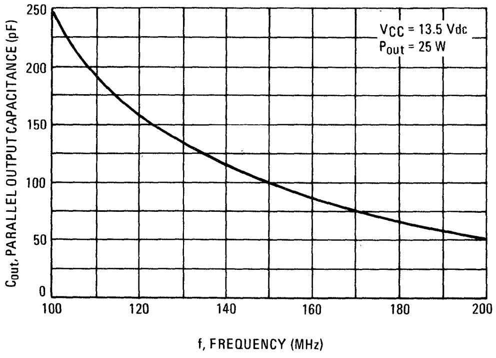


FIGURE 11 – V_{CC} = 27 Vdc, P_{out} = 75 W

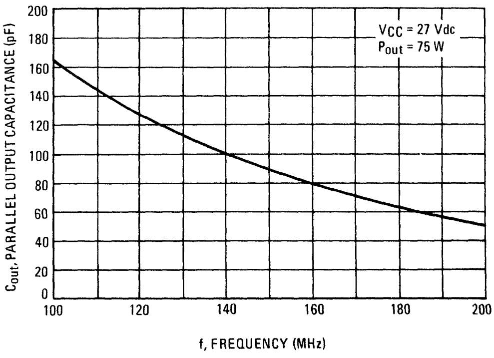
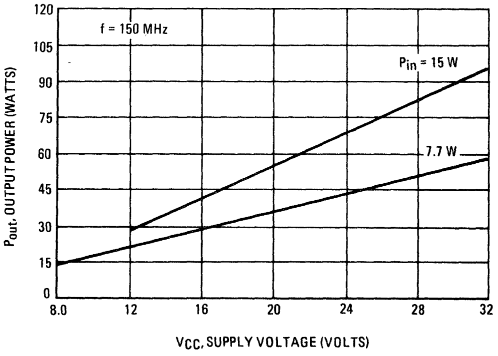


FIGURE 12 — OUTPUT POWER versus SUPPLY VOLTAGE



2N5864 (SILICON)

PNP SILICON ANNULAR TRANSISTOR

. . . designed for use in general-purpose amplifier and medium-speed switching applications.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 70 Vdc (Min) @ I_C = 10 mAdc
- DC Current Gain Specified — 10 mA to 500 mA
- High Collector Current — I_C = 1.5 Adc Continuous

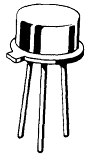
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	70	Vdc
Collector-Base Voltage	V_{CB}	90	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	1.5	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 7.15	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	8.75 50	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

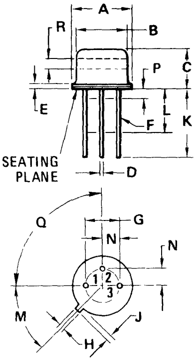
*Indicates JEDEC Registered Data

**Motorola Guarantees this data in addition to JEDEC Registered Data.

PNP SILICON GENERAL-PURPOSE TRANSISTOR



Pin 1. Emitter
2. Base
3. Collector



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02

TO-39

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	70	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	90	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0)	I_{CBO}	–	0.5	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	0.5	μAdc
ON CHARACTERISTICS				
*DC Current Gain	h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 10 Vdc)		50	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)		50	–	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)		50	500	
(I_C = 300 mAdc, V_{CE} = 10 Vdc)		35	–	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)		25	–	
*Collector-Emitter Saturation Voltage (I_C = 300 mAdc, I_B = 30 mAdc)	$V_{CE(sat)}$		0.9	Vdc
Base-Emitter Saturation Voltage (I_C = 300 mAdc, I_B = 30 mAdc)	$V_{BE(sat)}$	–	1.25	Vdc
*Base-Emitter On Voltage (I_C = 150 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	–	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS				
*Current-Gain—Bandwidth Product (1) (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)	f_T	50	–	MHz
*Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	–	25	pF
Emitter-Base Capacitance (V_{BE} = 1.0 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	150	pF
*Input Impedance (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{ie}	200	1500	Ohms
*Voltage Feedback Ratio (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{re}	–	5.0	$X10^{-4}$
*Small-Signal Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	50	500	–
*Output Admittance (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{oe}	10	200	μmhos

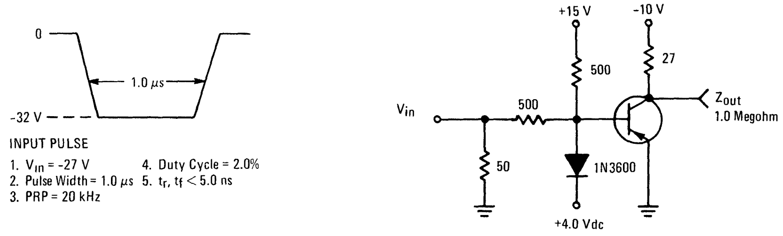
SWITCHING CHARACTERISTICS (See Figure 1)

Delay Time	(V_{CC} = 10 Vdc, I_C = 300 mAdc, I_{B1} = 30 mAdc)	t_d	–	30	ns
Rise Time		t_r	–	100	ns
Storage Time	(V_{CC} = 10 Vdc, I_C = 300 mAdc, I_{B1} = I_{B2} = 30 mAdc)	t_s	–	500	ns
Fall Time		t_f	–	250	ns

*Indicates JEDEC Registered Data.

(1) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



2N5865 (SILICON)

PNP SILICON ANNULAR TRANSISTOR

. . . designed where high-current, high-voltage conditions are requirements for general-purpose switching and amplifier applications.

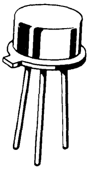
- Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 50 Vdc (Min) @ I_C = 10 mAdc
- DC Current Gain Specified – 1.0 mA to 500 mA
- Turn-On Time –
  t_{on} = 120 ns (Max) @ I_C = 500 mAdc

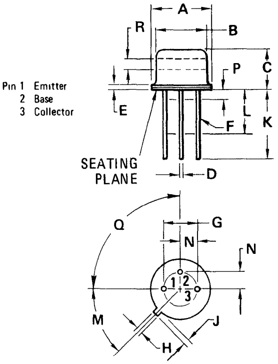
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	1.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 7.15	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	7.0 40	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

PNP SILICON GENERAL-PURPOSE TRANSISTOR





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (2) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	50	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	70	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 35 Vdc, I_E = 0)	I_{CBO}	–	200	nAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	200	nAdc
ON CHARACTERISTICS (2)				
DC Current Gain	h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)		40	–	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)		40	200	
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		20	–	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	–	1.25	Vdc
Base-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{BE(sat)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product(1) (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)	f_T	100	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	–	20	pF
Emitter-Base Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	150	pF

SWITCHING CHARACTERISTICS

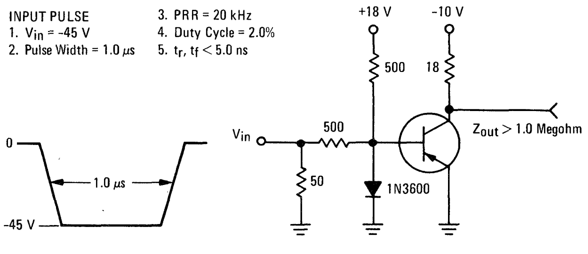
		Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 10 Vdc, I_C = 500 mAdc, I_{B1} = 50 mAdc)	t_d	–	30	ns
Rise Time		t_r	–	90	ns
Storage Time	(V_{CC} = 10 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc)	t_s	–	350	ns
Fall Time		t_f	–	150	ns

*Indicates JEDEC Registered Data.

(1) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates itself to unity.

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT



INPUT PULSE
1. V_{in} = -45 V
2. Pulse Width = 1.0 μs
3. PRR = 20 kHz
4. Duty Cycle = 2.0%
5. t_r, t_f < 5.0 ns

2N5867, 2N5868 PNP (SILICON)
2N5869, 2N5870 NPN

COMPLEMENTARY SILICON MEDIUM-POWER TRANSISTORS

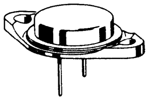
. . .designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 1.0$ Vdc (Max) @ $I_C = 2.0$ Adc
- Low Leakage Current — $I_{CEX} = 0.1$ mAdc (Max)
- Excellent DC Current Gain — $h_{FE} = 20$ (Min) @ $I_C = 1.5$ Adc
- High Current Gain — Bandwidth Product — $f_T = 4.0$ MHz at $I_C = 0.25$ Adc

5.0 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
87.5 WATTS



*MAXIMUM RATINGS

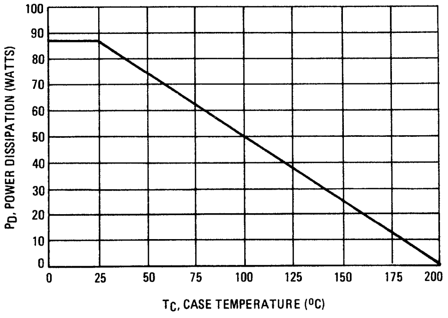
Rating	Symbol	2N5867 2N5869	2N5868 2N5870	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	5.0 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	87.5 0.5		Watts W/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

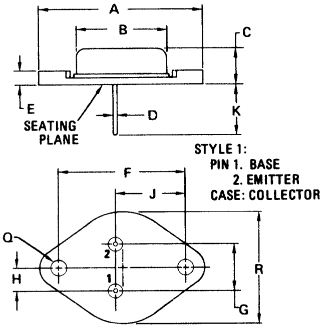
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.0	$^oC/W$

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 11-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

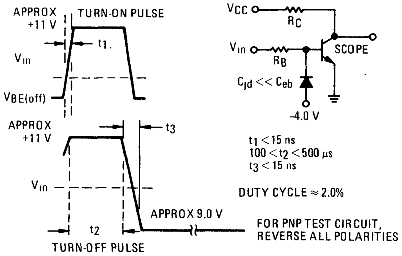
Collector connected to case.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N5867, 2N5869		60	–	
	2N5868, 2N5870		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5867, 2N5869		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N5868, 2N5870		–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5867, 2N5869		–	0.1	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5868, 2N5870		–	0.1	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5867, 2N5869		–	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5868, 2N5870		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5867, 2N5869		–	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	2N5868, 2N5870		–	0.1	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 0.3 Adc, V_{CE} = 4.0 Vdc)			35	–	
(I_C = 1.5 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)			–	1.0	
(I_C = 5.0 Adc, I_B = 1.25 Adc)			–	2.0	
Base-Emitter On Voltage (1) (I_C = 1.5 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 1.25 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5867, 2N5868		–	200	
	2N5869, 2N5870		–	150	
Small-Signal Current Gain (I_C = 0.25 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 1.5 Adc, I_{B1} = I_{B2} = 0.15 Adc)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 AND 6, R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

FIGURE 3 – TURN "ON" TIME

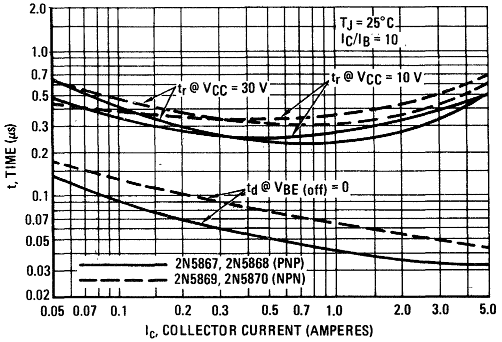


FIGURE 4 – THERMAL RESPONSE

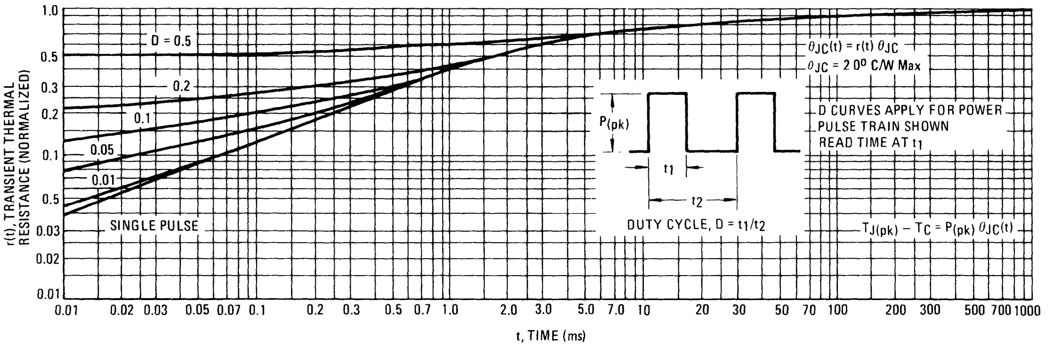
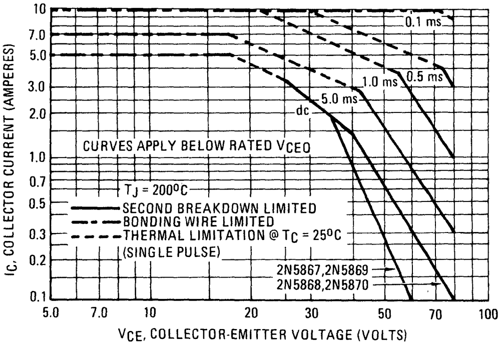


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown. (See Motorola Application Note AN-415).

FIGURE 6 – TURN "OFF" TIME

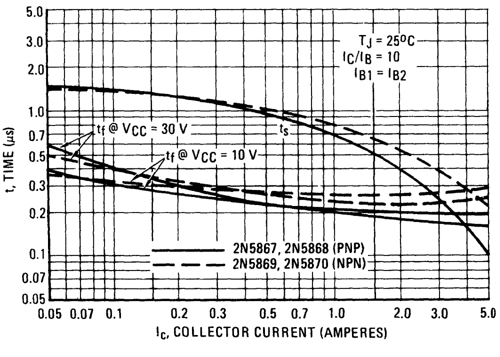
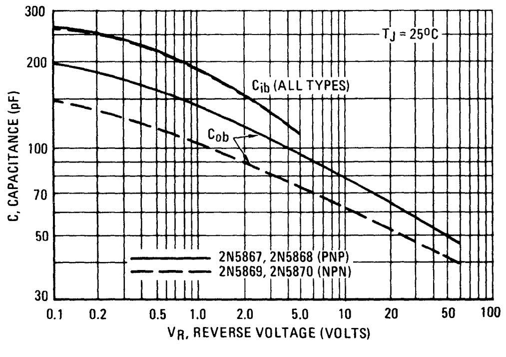


FIGURE 7 – CAPACITANCE



PNP
2N5867 and 2N5868

NPN
2N5869 and 2N5870

FIGURE 8 – DC CURRENT GAIN

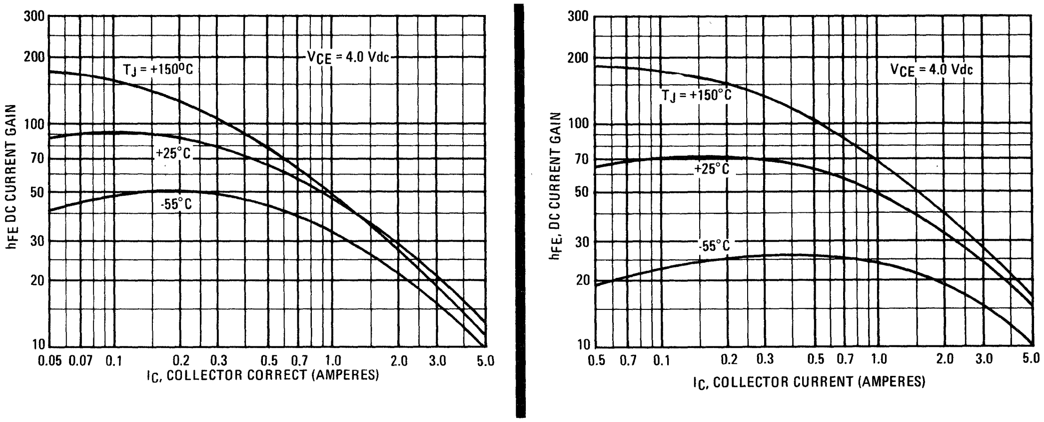


FIGURE 9 – COLLECTOR SATURATION REGION

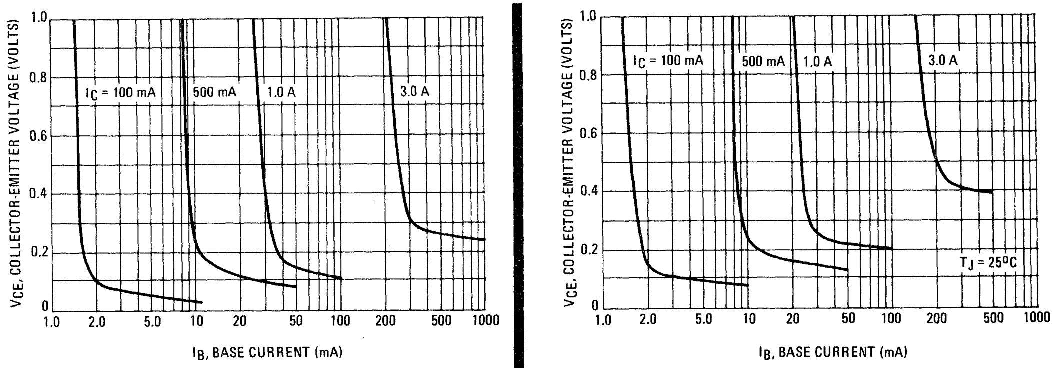
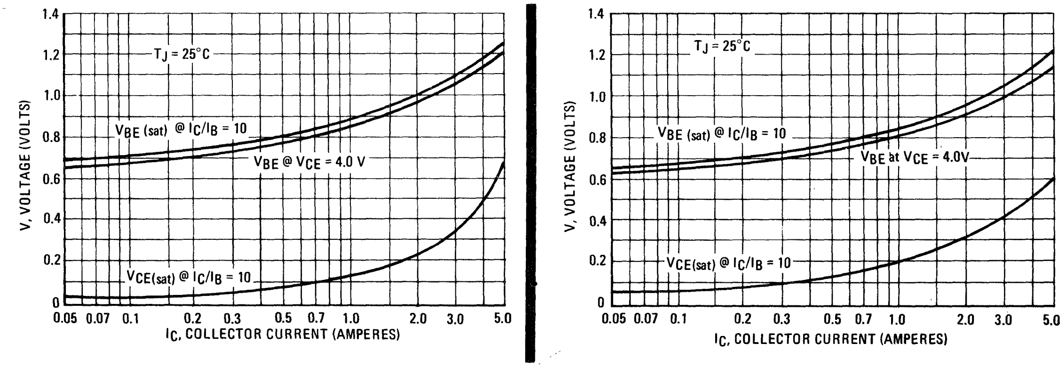


FIGURE 10 – "ON" VOLTAGES



PNP
2N5867 and 2N5868

NPN
2N5869 and 2N5870

FIGURE 11 – TEMPERATURE COEFFICIENTS

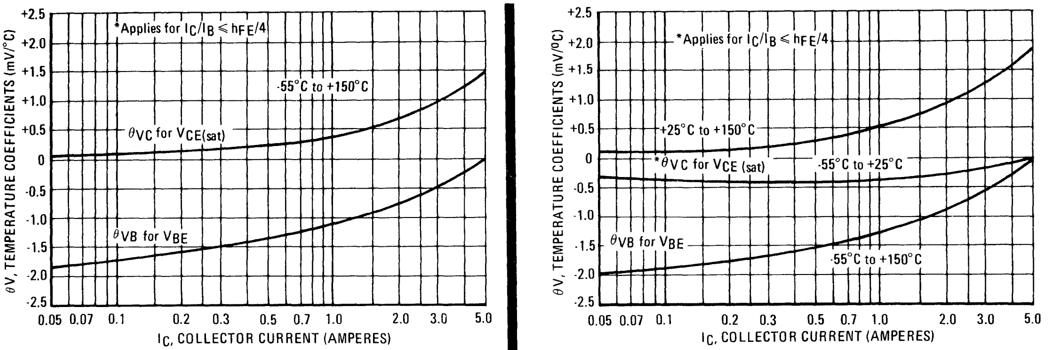


FIGURE 12 – COLLECTOR CUT-OFF REGION

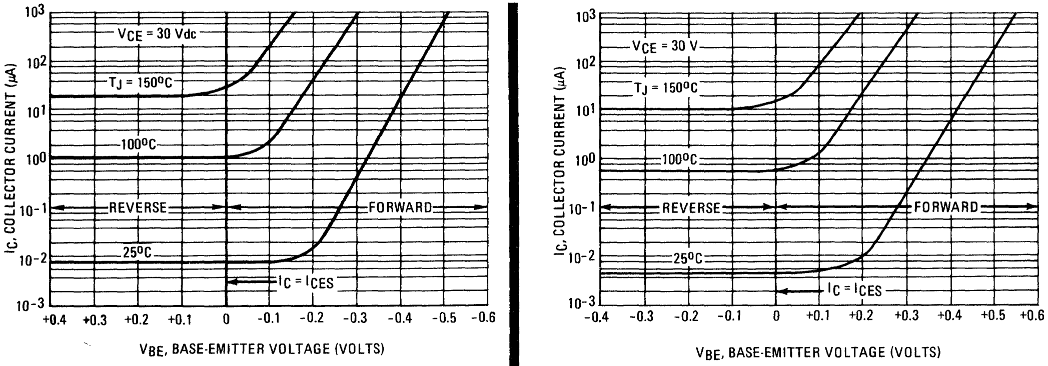
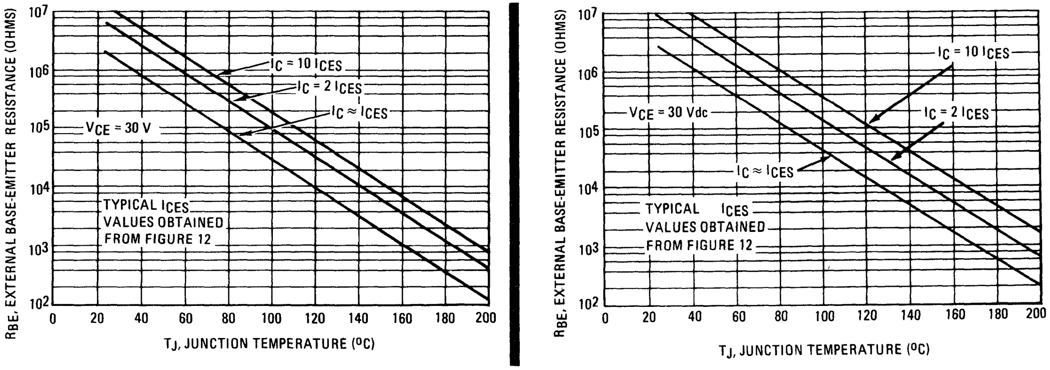


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N5871, 2N5872, 2N6317, 2N6318 PNP (SILICON)
2N5873, 2N5874, 2N6315, 2N6316 NPN

COMPLEMENTARY SILICON MEDIUM-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 1.0$ Vdc (Max) @ $I_C = 4.0$ Adc
- Low Leakage Current — $I_{CEX} = 0.25$ mAdc (Max)
- Excellent DC Current Gain — $h_{FE} = 20$ (Min) @ $I_C = 2.5$ Adc
- High Current Gain — Bandwidth Product — $f_T = 4.0$ MHz @ $I_C = 0.25$ Adc
- Choice of Packages — TO-3 — 2N5871/2N5874
  TO-66 — 2N6315/2N6318

7.0 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS

115 WATTS — TO-3
90 WATTS — TO-66

*MAXIMUM RATINGS

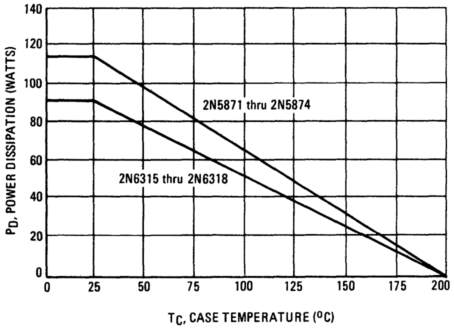
Rating	Symbol	2N5871 2N5873 2N6315 2N6317	2N5872 2N5874 2N6316 2N6318	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	7.0 15		Adc
Base Current	I_B	2.0		Adc
		2N5871 Series	2N6315 Series	
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	115 0.658	90 0.515	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N5871 2N5872 2N5873 2N5874	2N6315 2N6316 2N6317 2N6318	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.52	1.94	$^oC/W$

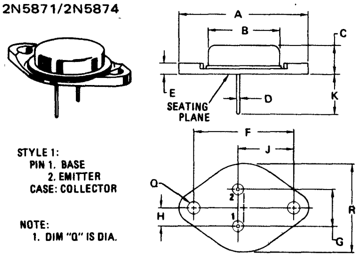
*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 — POWER DERATING



Safe Area Limits are indicated by Figures 5 and 6. Both limits are applicable and must be observed.

2N5871/2N5874



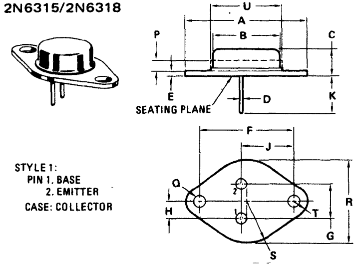
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

CASE 11-03

2N6315/2N6318



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

CASE 80-02
TO-66

2N5871, 2N5872, 2N6317, 2N6318 PNP (continued)
2N5873, 2N5874, 2N6315, 2N6316 NPN

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N5871,2N5873,2N6315,2N6317		60	–	
	2N6872,2N5874,2N6316,2N6318		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5871,2N5873,2N6315,2N6317		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N5872,2N5874,2N6316,2N6318		–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5871,2N5873,2N6315,2N6317		–	0.25	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5872,2N5874,2N6316,2N6318		–	0.25	
(V_{CE} = 60 Vdc $V_{BE(off)}$ =1.5 Vdc,T_C =150°C)	2N5871,2N5873,2N6315,2N6317		–	2.0	
(V_{CE} = 80 Vdc,$V_{BE(off)}$ =1.5 Vdc,T_C =150°C)	2N5872,2N5874,2N6316,2N6318		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5871,2N5873,2N6315,2N6317		–	0.25	
(V_{CB} = 80 Vdc, I_E = 0)	2N5872,2N5874,2N6316,2N6318		–	0.25	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 4.0 Vdc)			35	–	
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 0.4 Adc)			–	1.0	
(I_C = 7.0 Adc, I_B = 1.75 Adc)			–	2.0	
Base-Emitter Saturation Voltage (1) (I_C = 7.0 Adc, I_B = 1.75 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5871,2N5872,2N6317,2N6318		–	300	
	2N5873,2N5874,2N6315,2N6316		–	200	
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.25 Adc)	t_r	–	0.7	µs
Storage Time		t_s	–	1.0	µs
Fall Time		t_f	–	0.8	µs

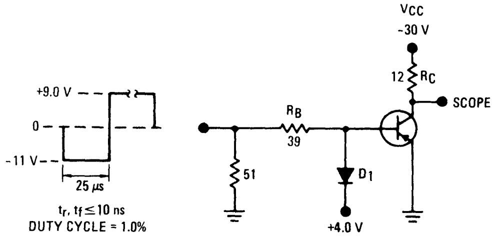
*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2 0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

TYPICAL CHARACTERISTICS

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 AND 7, R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS.

D_1 MUST BE FAST RECOVERY TYPE, e.g.

MBD5300 USED ABOVE I_B ≈ 100 mA

MSD6100 USED BELOW I_B ≈ 100 mA

FOR NPN TEST CIRCUIT, REVERSE ALL POLARITIES.

FIGURE 3 — TURN "ON" TIME

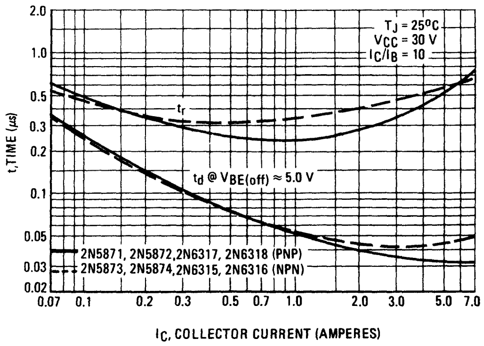
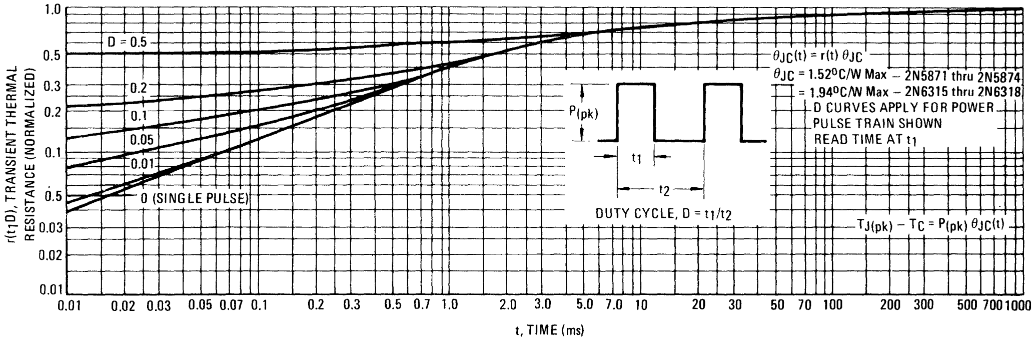


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N5871 thru 2N5874

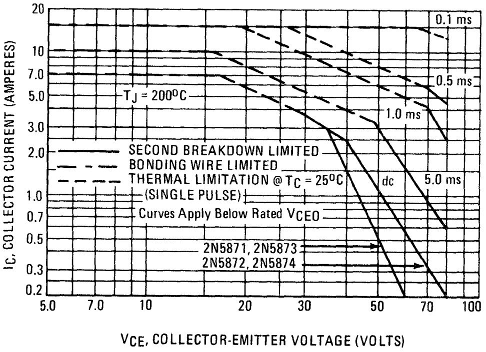
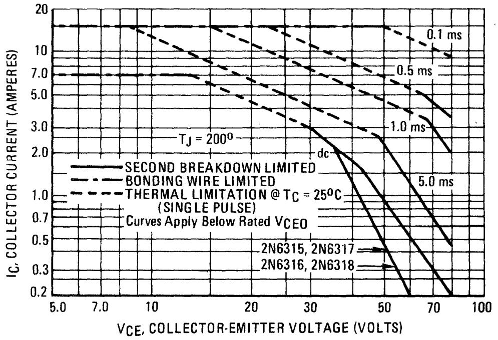


FIGURE 6 – 2N6315 thru 2N6318



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitaitons imposed by second breakdown.

FIGURE 7 – TURN "OFF" TIME

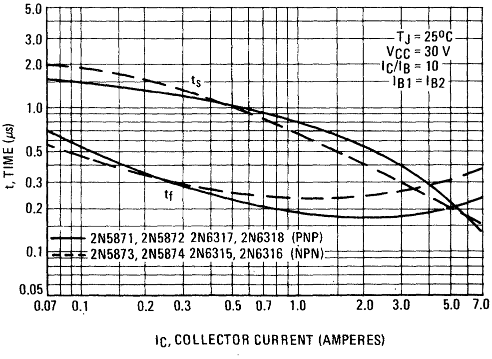


FIGURE 8 – CAPACITANCE

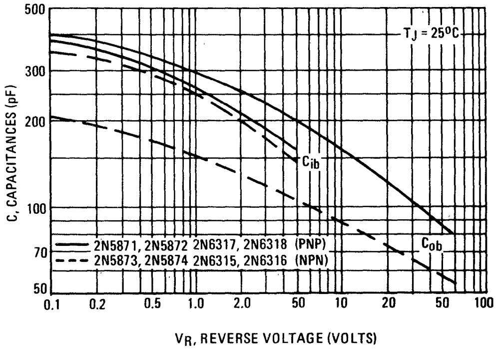


FIGURE 9 – DC CURRENT GAIN

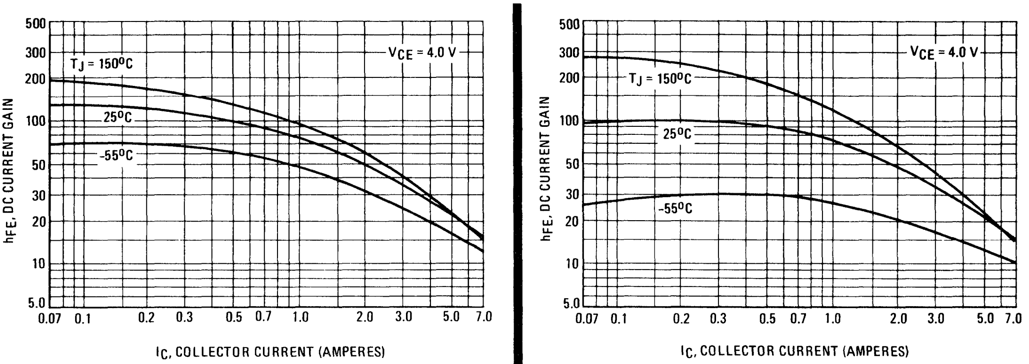


FIGURE 10 – COLLECTOR SATURATION REGION

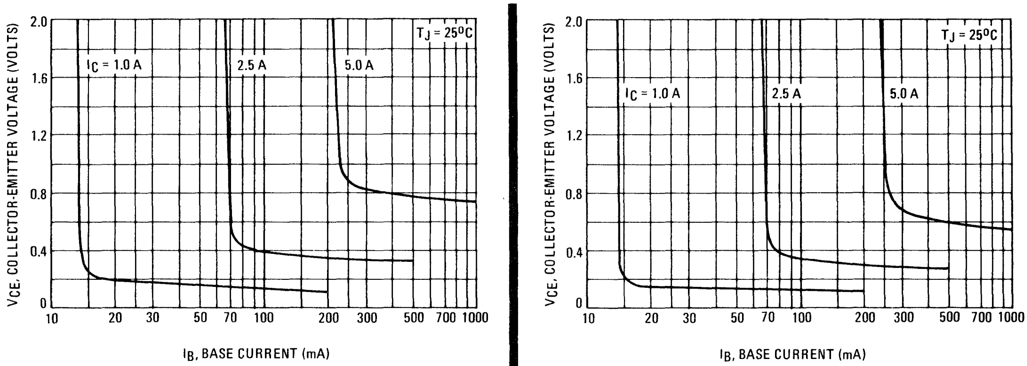
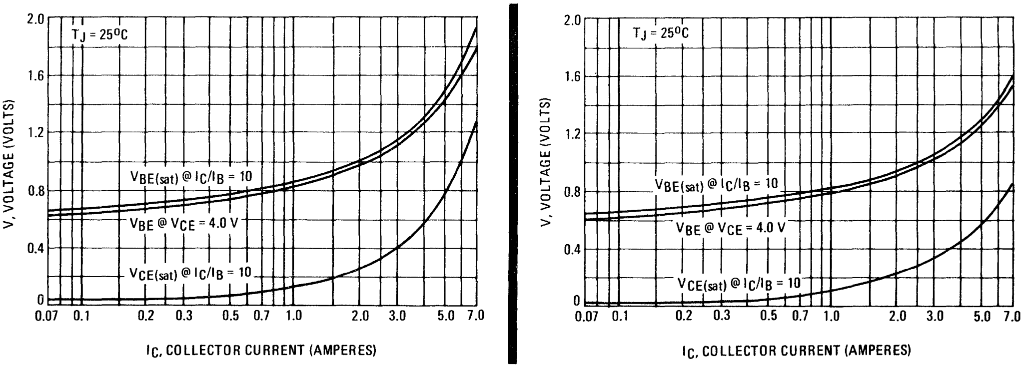


FIGURE 11 – "ON" VOLTAGES



PNP
2N5871 and 2N5872
2N6317 and 2N6318

NPN
2N5873 and 2N5874
2N6315 and 2N6316

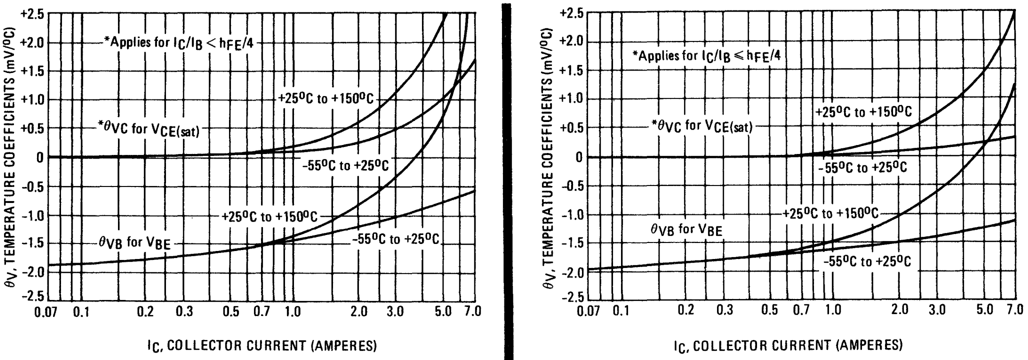


FIGURE 12 — TEMPERATURE COEFFICIENTS

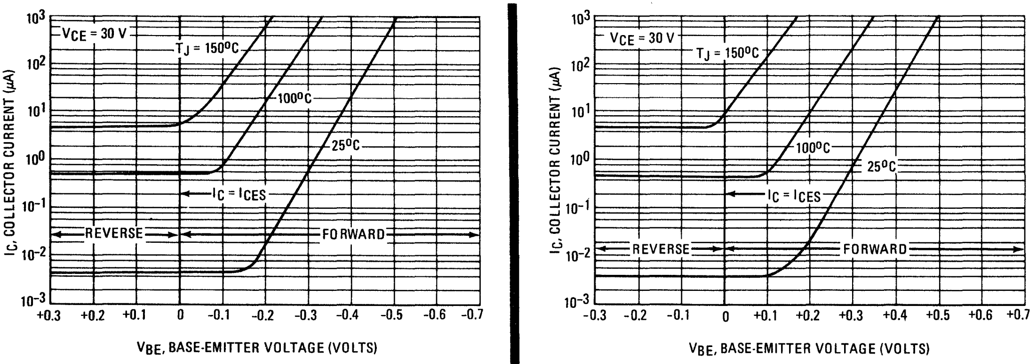


FIGURE 13 — COLLECTOR CUT-OFF REGION

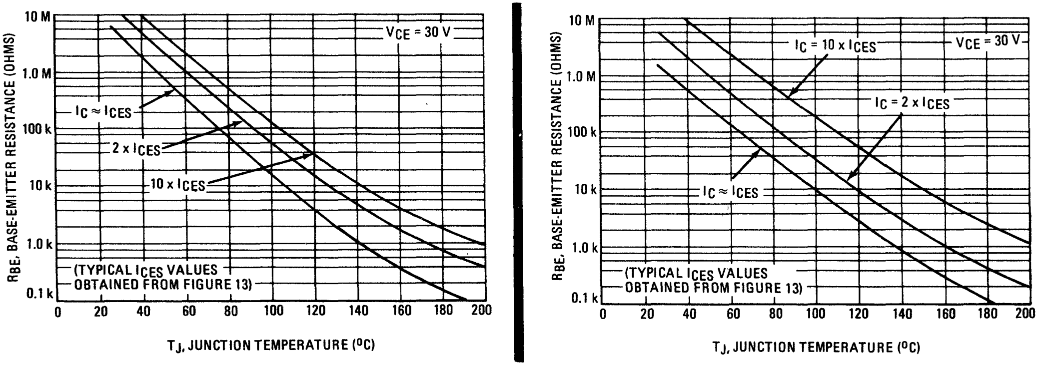


FIGURE 14 — EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE

2N5875, 2N5876 PNP (SILICON)
2N5877, 2N5878 NPN

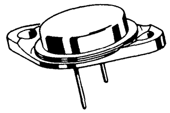
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 5.0 Adc
- Low Leakage Current —
  I_{CEX} = 0.5 mAdc (Max) @ Rated Voltage
- Excellent DC Current Gain —
  h_{FE} = 20 (Min) @ I_C = 4.0 Adc
- High Current Gain — Bandwidth Product —
  f_T = 4.0 MHz (Min) @ I_C = 0.5 A

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
150 WATTS

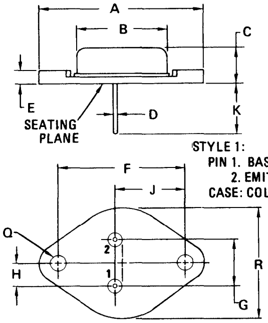


*MAXIMUM RATINGS

Rating	Symbol	2N5875 2N5877	2N5876 2N5878	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 20		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

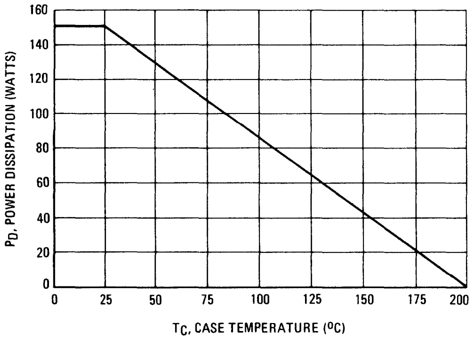
CASE 11-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

Collector connected to case.

FIGURE 1 — POWER DERATING

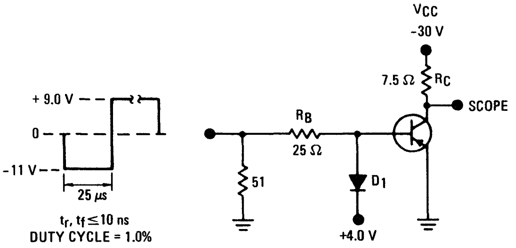


***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1)	$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0) 2N5875, 2N5877		60	–	
2N5876, 2N5878		80	–	
Collector Cutoff Current	I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0) 2N5875, 2N5877		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0) 2N5876, 2N5878		–	1.0	
Collector Cutoff Current	I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5875, 2N5877		–	0.5	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5876, 2N5878		–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) 2N5875, 2N5877		–	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) 2N5876, 2N5878		–	5.0	
Collector Cutoff Current	I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0) 2N5875, 2N5877		–	0.5	
(V_{CB} = 80 Vdc, I_E = 0) 2N5876, 2N5878		–	0.5	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_E = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1)	h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		35	–	
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		20	100	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)		4.0	–	
Collector-Emitter Saturation Voltage (1)	$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)		–	1.0	
(I_C = 10 Adc, I_B = 2.5 Adc)		–	3.0	
Base-Emitter Saturation Voltage (1) (I_C = 10 Adc, I_B = 2.5 Adc)	$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0	–	MHz
Output Capacitance	C_{ob}	–		pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz) 2N5875, 2N5876		–	500	
2N5877, 2N5878		–	300	
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	20	–	–
SWITCHING CHARACTERISTICS				
Rise Time (V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, See Figure 2)	t_r	–	0.7	µs
Storage Time	t_s	–	1.0	µs
Fall Time	t_f	–	0.8	µs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 and 6, R_B and R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g. MBD5300 USED ABOVE $I_B \approx$ 100 mA MSD6100 USED BELOW $I_B \approx$ 100 mA

For NPN test circuit, reverse all polarities.

FIGURE 3 — TURN-ON TIME

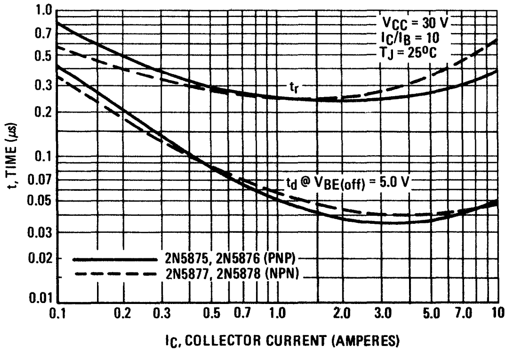


FIGURE 4 – THERMAL RESPONSE

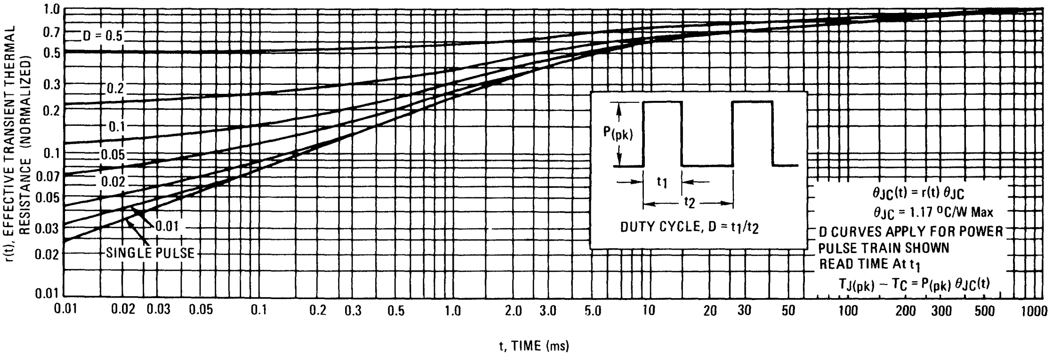
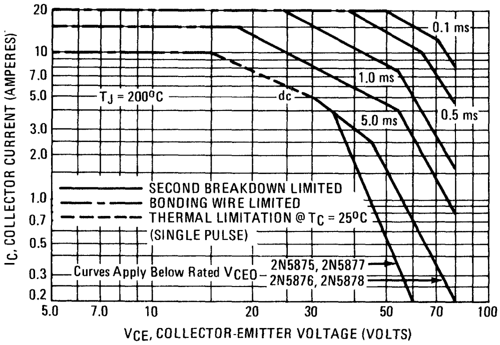


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 6 – TURN-OFF TIME

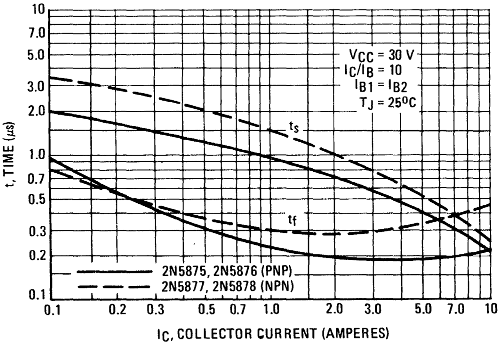
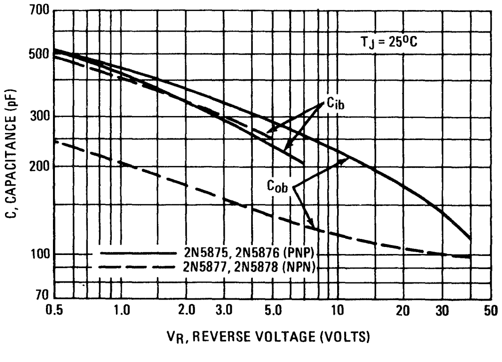


FIGURE 7 – CAPACITANCE



PNP DEVICES
2N5875 and 2N5876

NPN DEVICES
2N5877 and 2N5878

FIGURE 8 – DC CURRENT GAIN

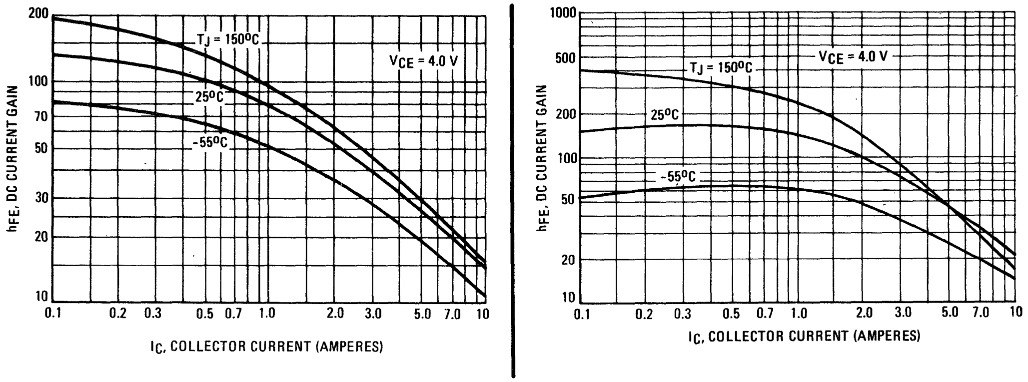


FIGURE 9 – COLLECTOR SATURATION REGION

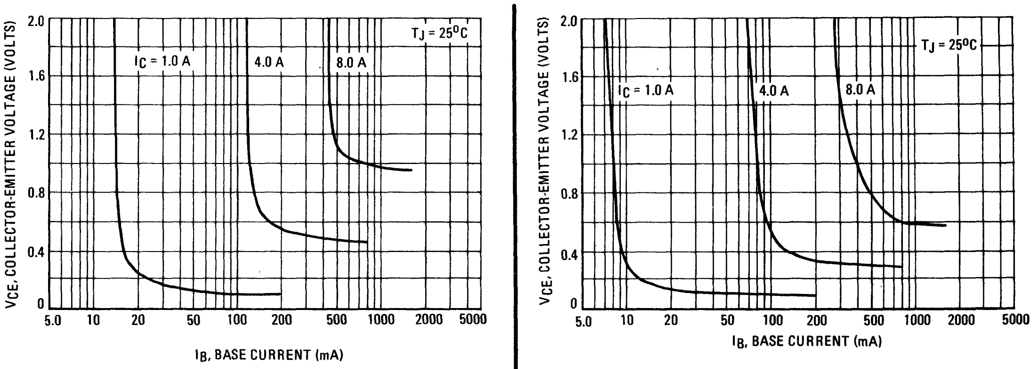
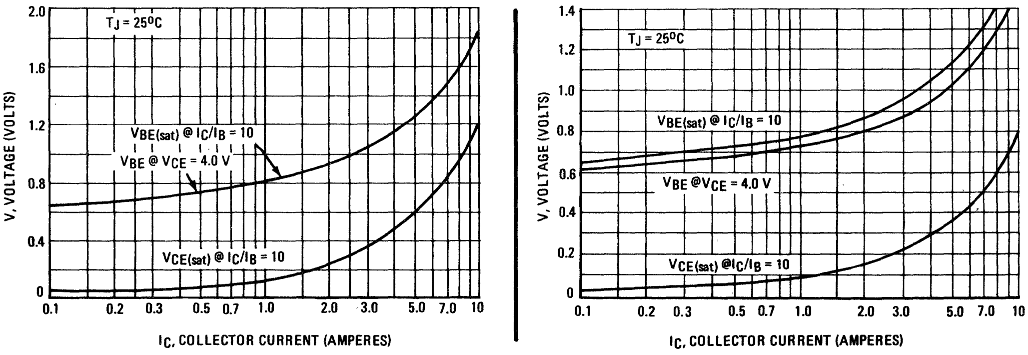


FIGURE 10 – "ON" VOLTAGES



PNP DEVICES
2N5875 and 2N5876

NPN DEVICES
2N5877 and 2N5878

FIGURE 11 – TEMPERATURE COEFFICIENTS

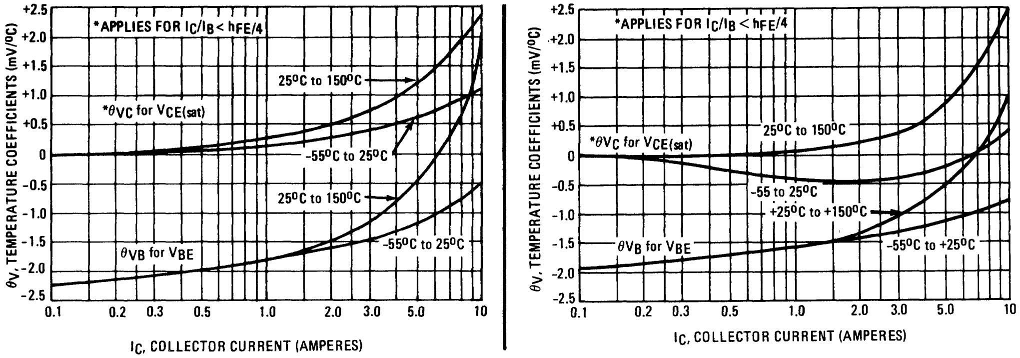


FIGURE 12 – COLLECTOR CUT-OFF REGION

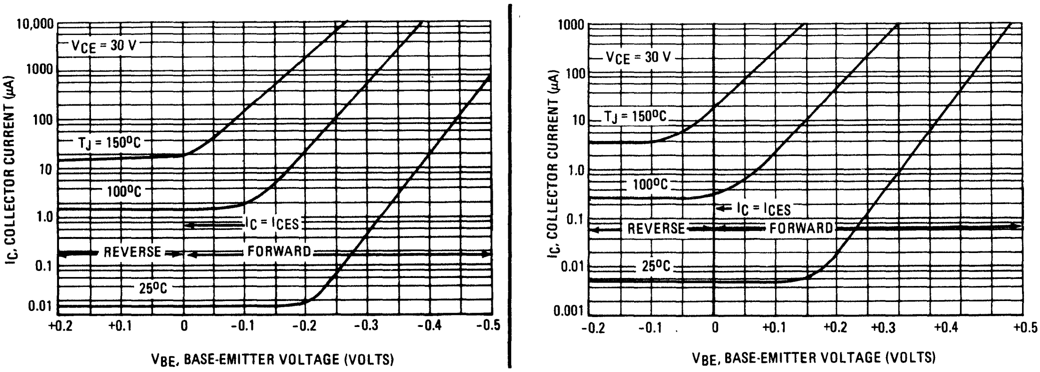
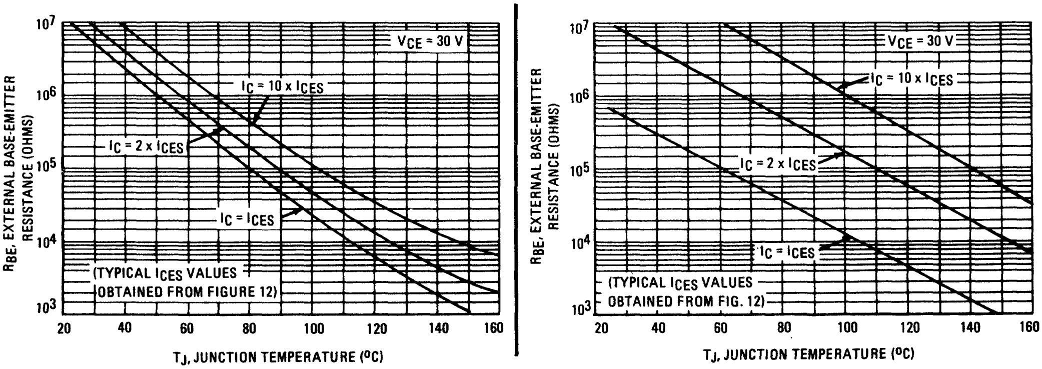


FIGURE 13 – EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE



2N5879, 2N5880 PNP (SILICON)
2N5881, 2N5882 NPN

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N5879, 2N5881
  = 80 Vdc (Min) — 2N5880, 2N5882
- DC Current Gain —
  h_{FE} = 20 (Min) @ I_C = 6.0 Adc
- Low Collector — Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 7.0 Adc
- High Current — Gain-Bandwidth Product —
  f_T = 4.0 MHz (Min) @ I_C = 1.0 Adc
- Recommended for New Circuit Designs

*MAXIMUM RATINGS

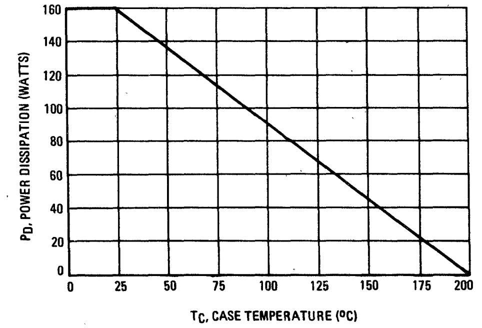
Rating	Symbol	2N5879 2N5881	2N5880 2N5882	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	15 30		Adc
Base Current	I_B	5.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.1	°C/W

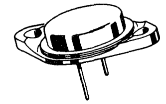
*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

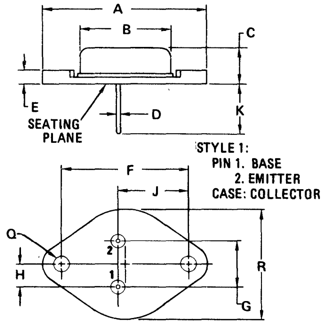
FIGURE 1 — POWER DERATING



15 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
160 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 11-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

Collector connected to case.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

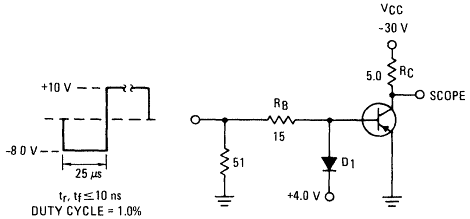
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5879, 2N5881		60	–	
	2N5880, 2N5882		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5879, 2N5881		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5880, 2N5882		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5879, 2N5881		–	0.5	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5880, 2N5882		–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5879, 2N5881		–	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5880, 2N5882		–	5.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5879, 2N5881		–	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N5880, 2N5882		–	0.5	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			35	–	
(I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 7.0 Adc, I_B = 0.7 Adc)			–	1.0	
(I_C = 15 Adc, I_B = 3.75 Adc)			–	4.0	
Base-Emitter Saturation Voltage (1) (I_C = 15 Adc, I_B = 3.75 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	2N5879, 2N5880		–	600	
	2N5881, 2N5882		–	400	
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.6 Adc See Figure 2)	t_r	–	0.7	µs
Storage Time		t_s	–	1.0	µs
Fall Time		t_f	–	0.8	µs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



FOR CURVES OF FIGURES 3 and 6, R_B and R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg.
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

For NPN test circuit, reverse all polarities.

FIGURE 3 – TURN-ON TIME

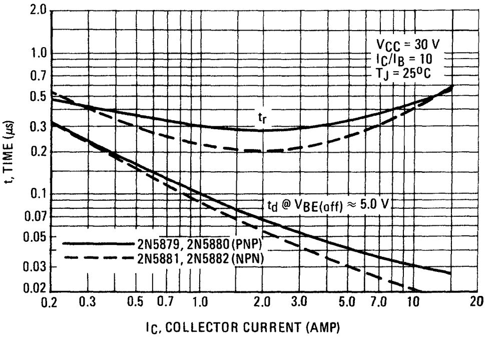


FIGURE 4 – THERMAL RESPONSE

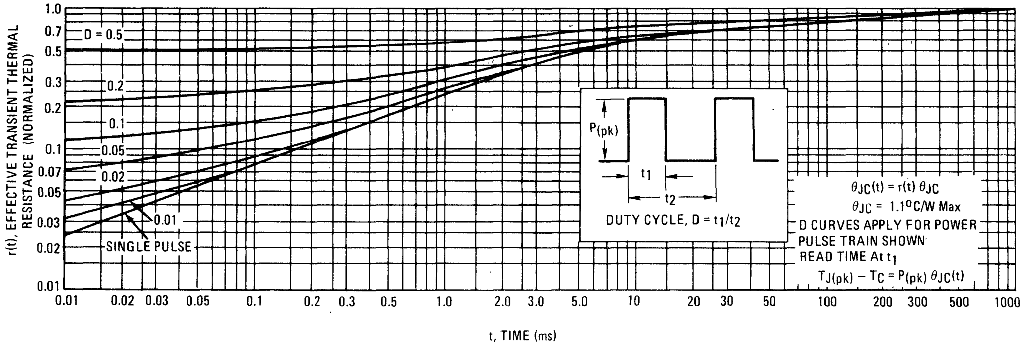
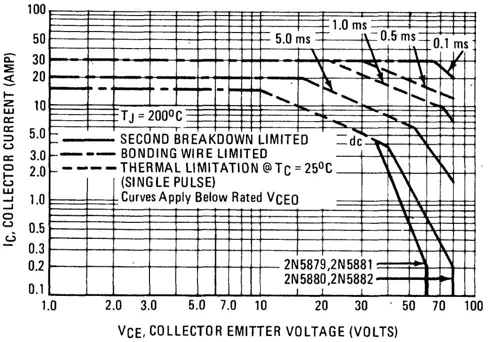


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 6 – TURN-OFF TIME

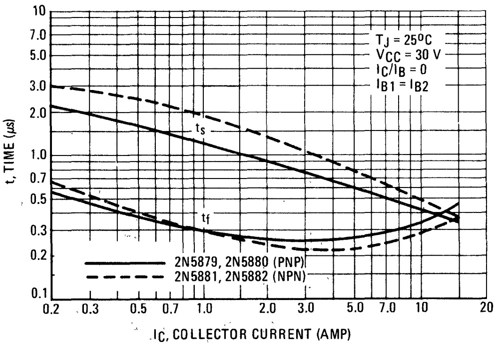
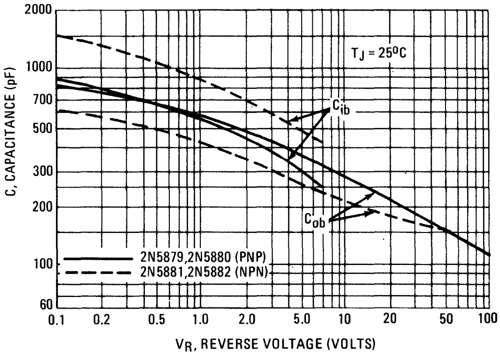


FIGURE 7 – CAPACITANCE



PNP
2N5879, 2N5880

NPN
2N5881, 2N5882

FIGURE 8 – DC CURRENT GAIN

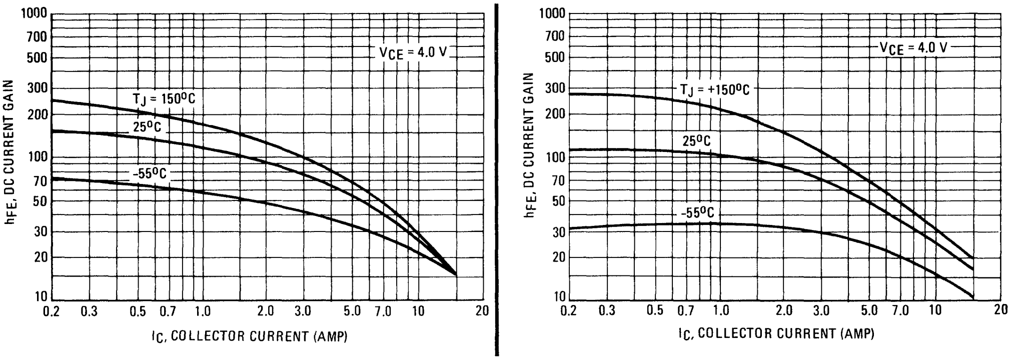


FIGURE 9 – COLLECTOR SATURATION REGION

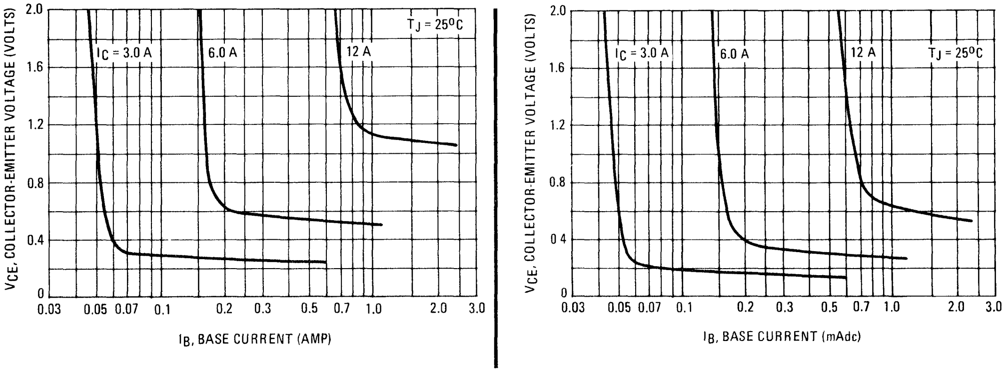
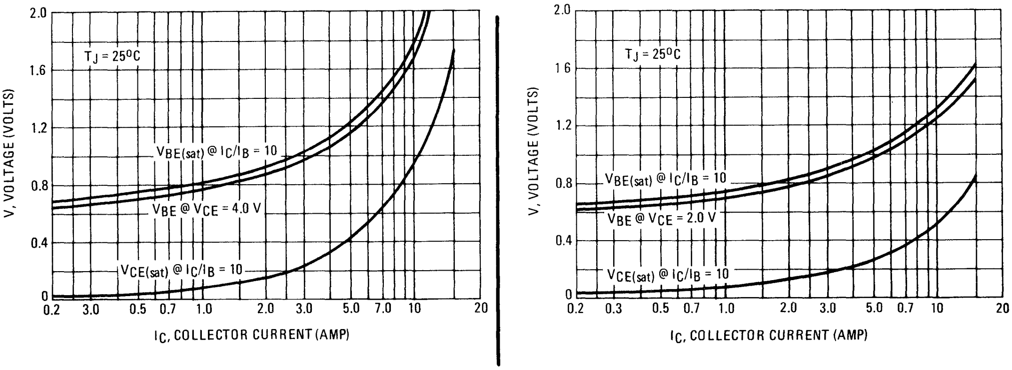


FIGURE 10 – "ON" VOLTAGES



PNP
2N5879, 2N5880

NPN
2N5881, 2N5882

FIGURE 11 – TEMPERATURE COEFFICIENTS

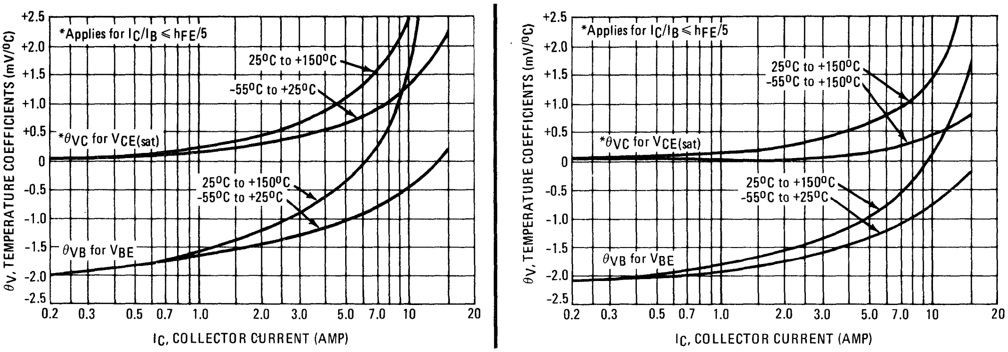


FIGURE 12 – COLLECTOR CUTOFF REGION

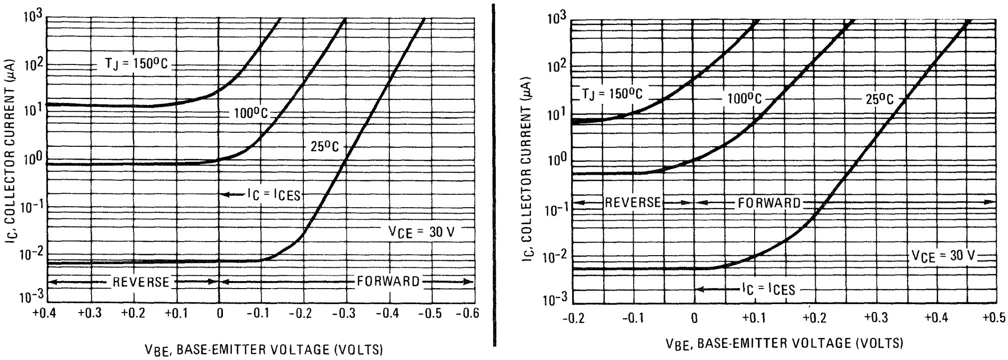
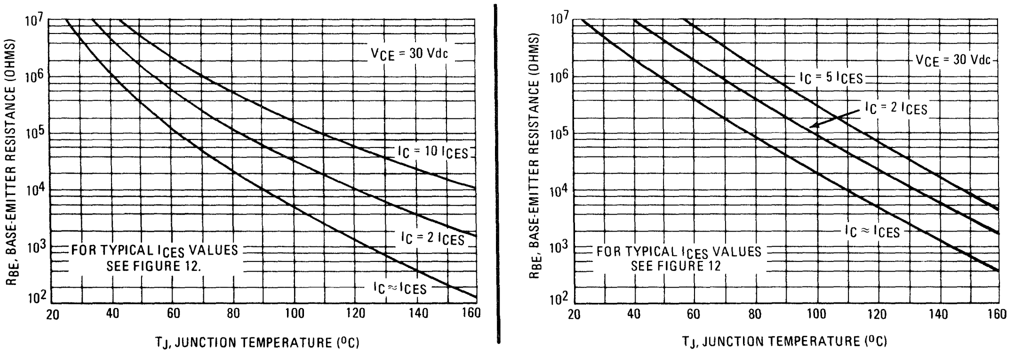


FIGURE 13 – EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE



2N5883, 2N5884 PNP (SILICON)
2N5885, 2N5886 NPN

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

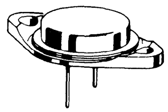
. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc, (max) at I_C = 15 Adc
- Low Leakage Current
  I_{CEX} = 1.0 mAdc (max) at Rated Voltage
- Excellent DC Current Gain –
  h_{FE} = 20 (min) at I_C = 10 Adc
- High Current Gain Bandwidth Product –
  f_T = 4.0 MHz (min) at I_C = 1.0 Adc

25 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
200 WATTS



*MAXIMUM RATINGS

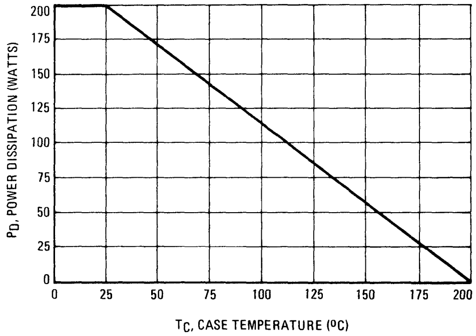
Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	25 50		Adc
Base Current	I_B	7.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.15		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

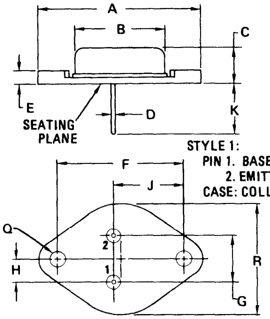
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE: Collector connected to case.
1. DIM "Q" IS DIA. CASE 11-01

2N5883, 2N5884 PNP, 2N5885, 2N5886 NPN (continued)

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	 2N5883, 2N5885 2N5884, 2N5886	$V_{CEO(sus)}$	 60 80	 – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	 2N5883, 2N5885 2N5884, 2N5886	I_{CEO}	 – –	 2.0 2.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N5883, 2N5885 2N5884, 2N5886 2N5883, 2N5885 2N5884, 2N5886	I_{CEX}	 – – – –	 1.0 1.0 10 10	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 2N5883, 2N5885 2N5884, 2N5886	I_{CBO}	 – –	 1.0 1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 25 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 35 20 4.0	 – 100 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 25 Adc, I_B = 6.25 Adc)		$V_{CE(sat)}$	 – –	 1.0 4.0	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 25 Adc, I_B = 6.25 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	 2N5883, 2N5884 2N5885, 2N5886	C_{ob}	 – –	 1000 500	pF
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	–	0.7	µs
Storage Time		t_s	–	1.0	µs
Fall Time		t_f	–	0.8	µs

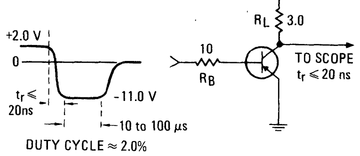
*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

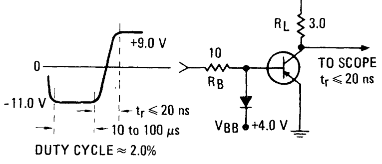
(2) $f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUITS

TURN-ON TIME



TURN-OFF TIME



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

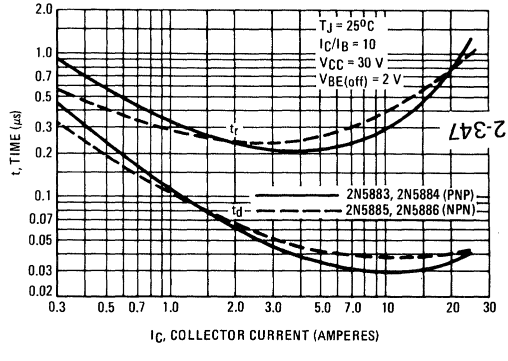


FIGURE 4 – THERMAL RESPONSE

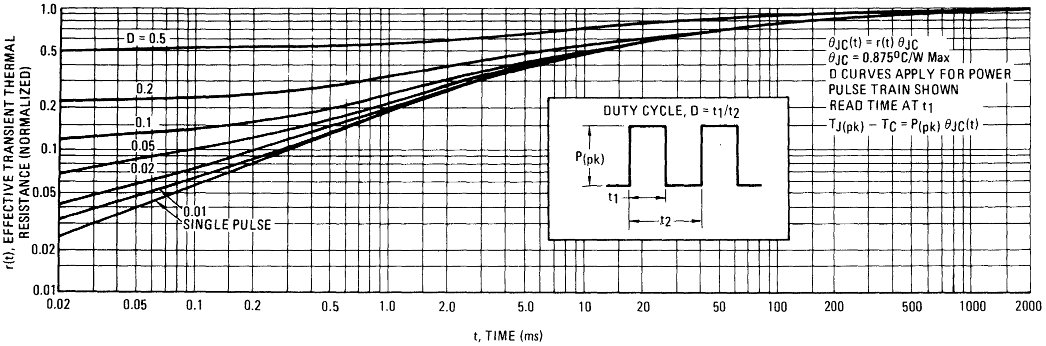
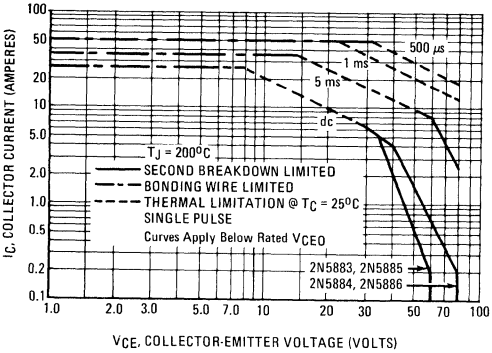


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See Motorola Application Note AN-415)

FIGURE 6 – TURN-OFF TIME

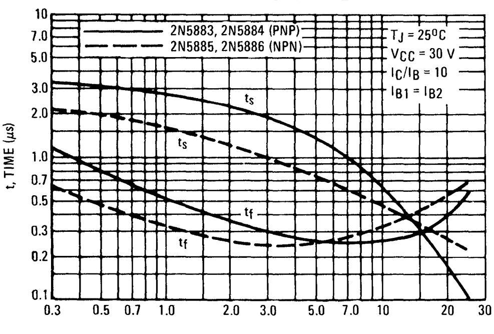
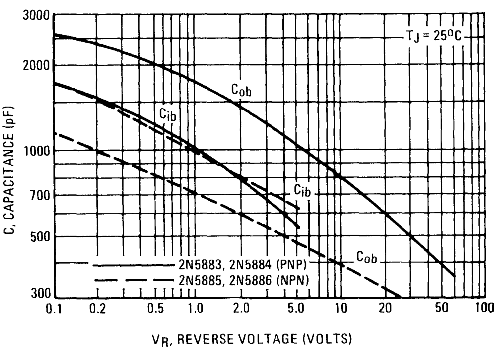


FIGURE 7 – CAPACITANCE



PNP DEVICES
2N5883 and 2N5884

NPN DEVICES
2N5885 and 2N5886

FIGURE 8 – DC CURRENT GAIN

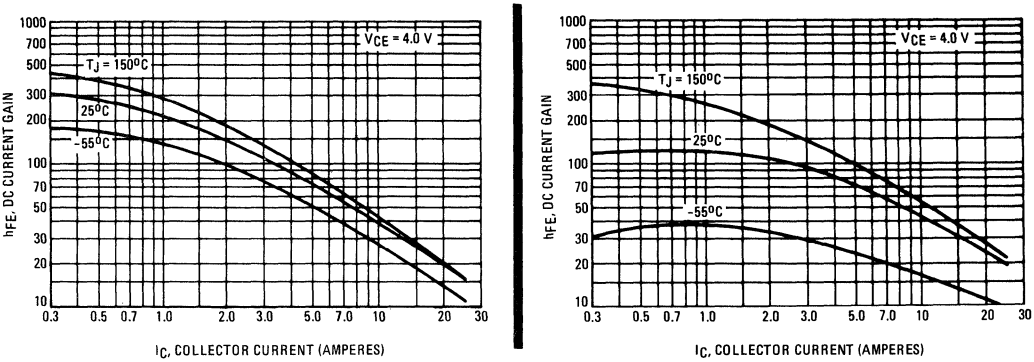


FIGURE 9 – COLLECTOR SATURATION REGION

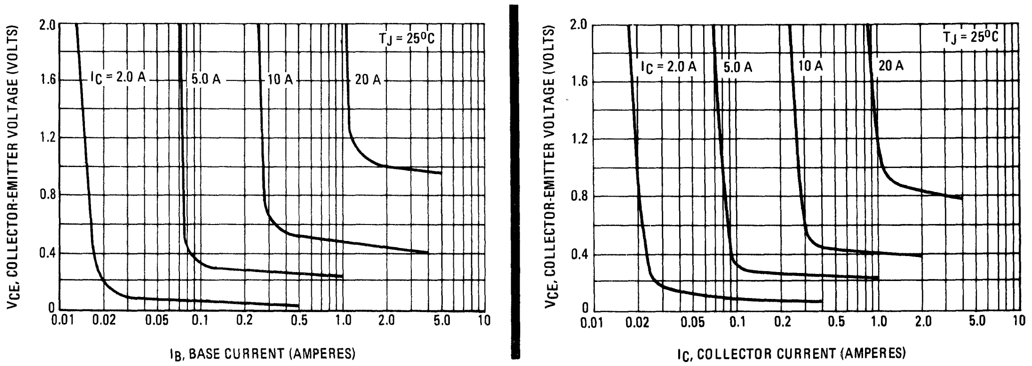
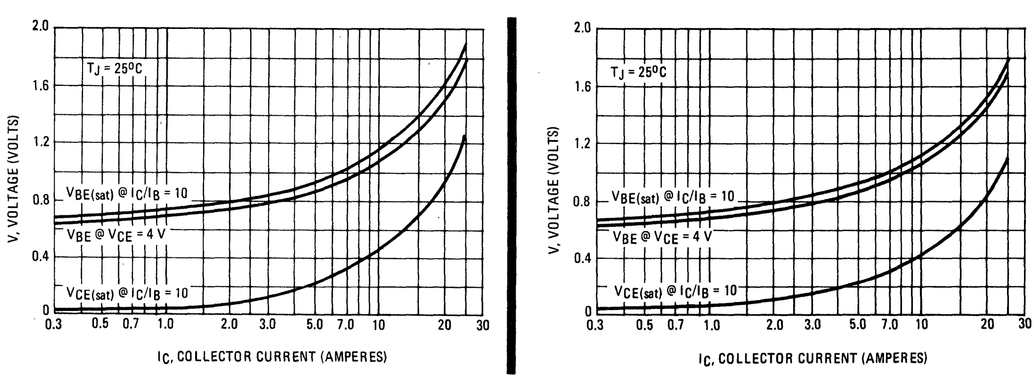


FIGURE 10 – "ON" VOLTAGES



PNP DEVICES
2N5883 and 2N5884

NPN DEVICES
2N5885 and 2N5886

FIGURE 11 – TEMPERATURE COEFFICIENTS

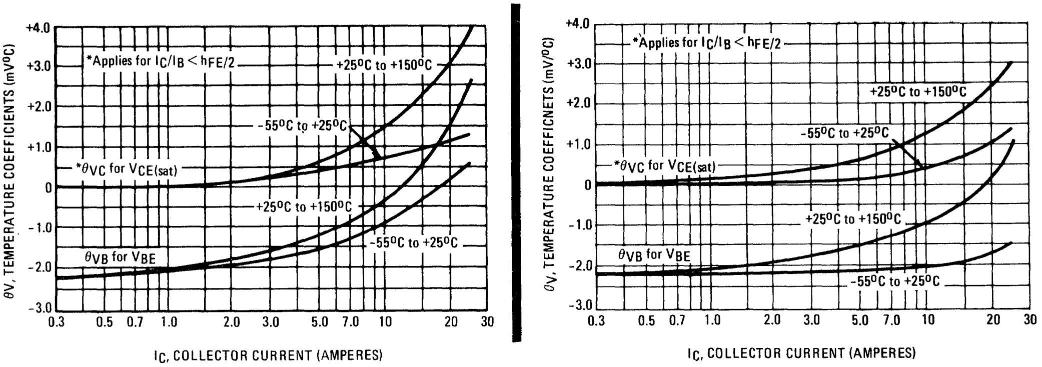


FIGURE 12 – COLLECTOR CUT-OFF REGION

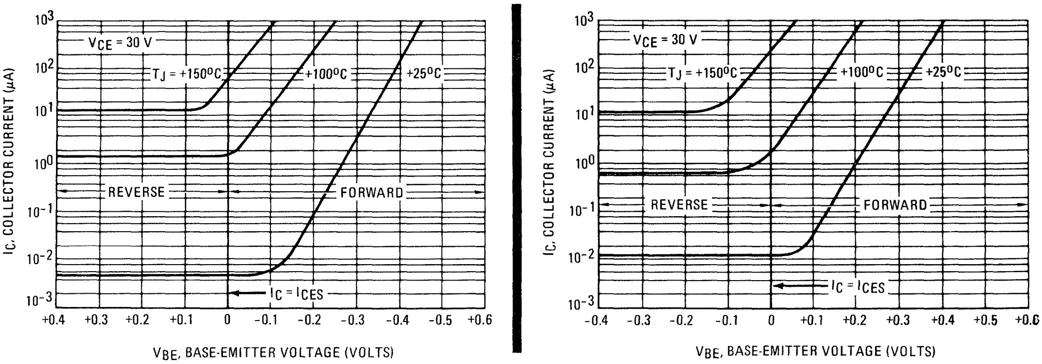
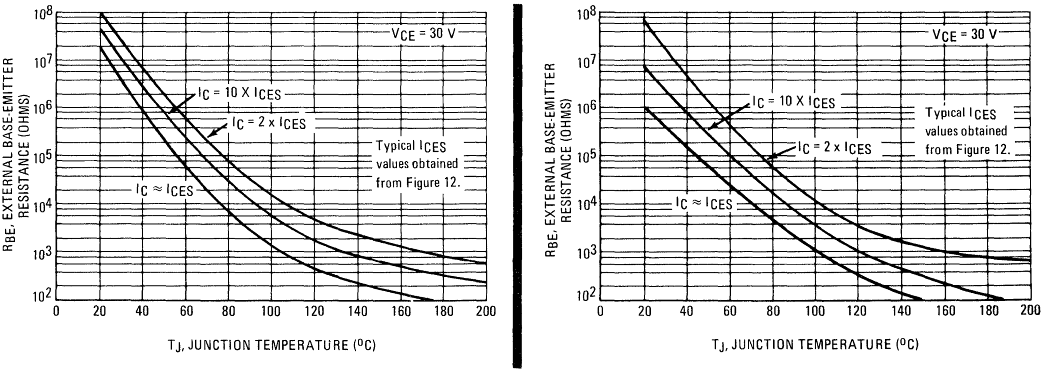


FIGURE 13 – EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE



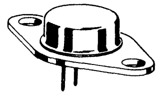
2N5887 thru 2N5901 (GERMANIUM)

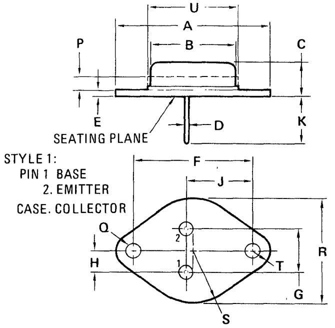
GERMANIUM PNP POWER TRANSISTORS

. . . designed for low frequency switching and amplifier applications requiring to 7.0 amperes collector current.

- Low Collector-Emitter Cutoff Current –
  I_{CEX} = 10 mA Max @ 100°C with V_{CE} to 75 V
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.4 V Max @ I_C = 7.0 A
- Broad Range of Current Gain Available
- TO-66 Cold Weld All Aluminum Package
- Electrically Similar to 2N3611 Series

7.0 AMPERE
POWER TRANSISTORS
PNP GERMANIUM
20–75 VOLTS
57 WATTS





STYLE 1:
PIN 1 BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

CASE 80-02
TO-66

*MAXIMUM RATINGS

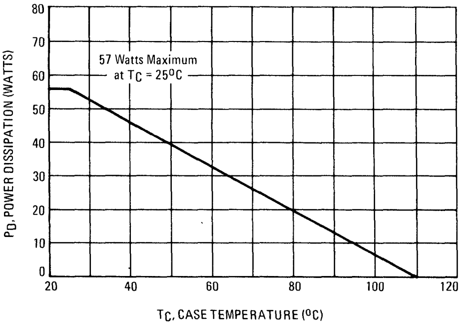
Rating	Symbol	2N5887	2N5888 2N5889 2N5893 2N5897 2N5901	2N5890 2N5894 2N5898	2N5891 2N5895 2N5899	2N5892 2N5896 2N5900	Unit
Collector-Emitter Voltage (Base Open)	V_{CEO}	15	25	35	45	60	Vdc
Collector-Emitter Voltage	V_{CES}	20	30	45	60	75	Vdc
Collector-Base Voltage	V_{CBO}	20	30	45	60	75	Vdc
Emitter-Base Voltage	V_{EBO}	← 20 →					Vdc
Collector Current – Continuous	I_C	← 7.0 →					Adc
Base Current – Continuous	I_B	← 2.0 →					Adc
Operating Case and Storage Temperature Range	T_C, T_{stg}	← -65 to +110 →					°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 57 → ← 0.67 →					Watts W/°C

*Indicates JEDEC Registered Data

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.5	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 500 mAdc, I_B = 0)	2N5887		15	–	
	2N5888,89,93,97,2N5901		25	–	
	2N5890,94,98		35	–	
	2N5891,95,99		45	–	
	2N5892,96,2N5900		60	–	
Collector-Emitter Breakdown Voltage (1)		BV_{CES}			Vdc
(I_C = 250 mAdc, V_{BE} = 0)	2N5887		20	–	
	2N5888,89,93,97,2N5901		30	–	
	2N5890,94,98		45	–	
	2N5891,95,99		60	–	
	2N5892,96,2N5900		75	–	
Collector Cutoff Current		I_{CEO}	–	30	mAdc
(V_{CE} = 1/2 V_{CEO} Max)	All Types				
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = V_{CES} Max, V_{BE} = 1.0 Vdc)	All Types		–	5.0	
(V_{CE} = V_{CES} Max, V_{BE} = 1.0 Vdc, T_C = 100°C)	All Types		–	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 2.0 Vdc)	All Types		–	0.06	
(V_{CB} = 15 Vdc)	2N5887		–	1.0	
(V_{CB} = 25 Vdc)	2N5888,89,93,97,2N5901		–	1.0	
(V_{CB} = 35 Vdc)	2N5890,94,98		–	1.0	
(V_{CB} = 45 Vdc)	2N5891,95,99		–	1.0	
(V_{CB} = 60 Vdc)	2N5892,96,2N5900		–	1.0	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{BE} = 20 Vdc, I_C = 0)	All Types				
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	2N5887,88		15	350	
	2N5889,90,91,92		30	70	
	2N5893,94,95,96		60	120	
	2N5897,98,99,2N5900		100	200	
	2N5901		175	350	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	2N5887,88		10	–	
	2N5889,90,91,92		15	–	
	2N5893,94,95,96		30	–	
	2N5897,98,99,2N5900		50	–	
	2N5901		75	–	
(I_C = 7.0 Adc, V_{CE} = 2.0 Vdc)	2N5887,88		5.0	–	
	2N5889 thru 2N5901		10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 7.0 Adc, I_B = 1.4 Adc)	2N5887,88		–	0.4	
(I_C = 7.0 Adc, I_B = 700 mAdc)	2N5889 thru 2N5901		–	0.4	
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.2	Vdc
(I_C = 7.0 Adc, V_{CE} = 2.0 Vdc)	All Types				
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product		f_T	250	–	kHz
(I_C = 0.5 Adc, V_{CE} = 12 Vdc)	All Types				

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

*Indicates JEDEC Registered Data.

FIGURE 2 – THERMAL RESPONSE

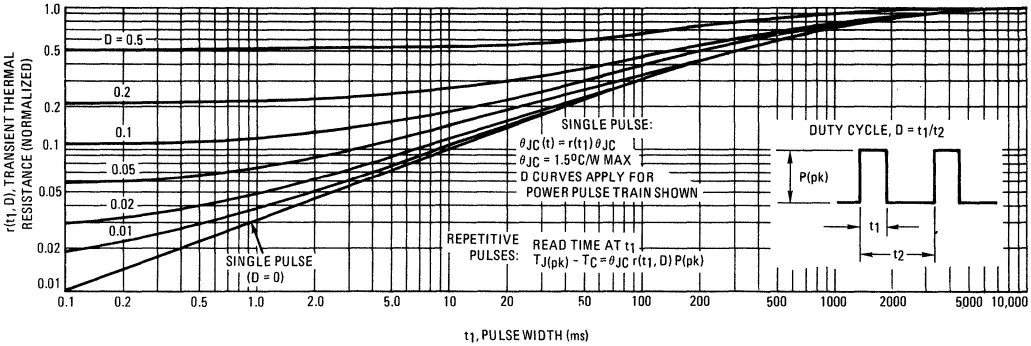


FIGURE 3 – CLAMPED INDUCTIVE SAFE OPERATING AREA

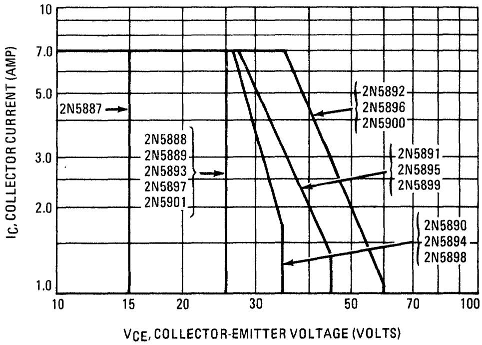


FIGURE 4 – CLAMPED INDUCTIVE SAFE OPERATING AREA TEST CIRCUIT

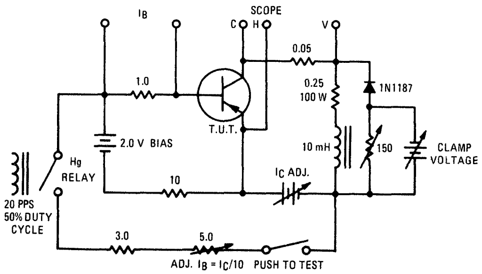


FIGURE 5 – SWITCHING TIMES

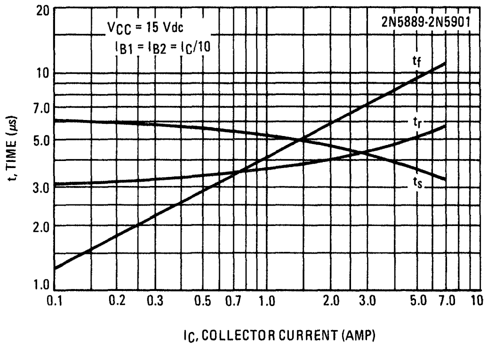


FIGURE 6 – SWITCHING TIME TEST CIRCUIT

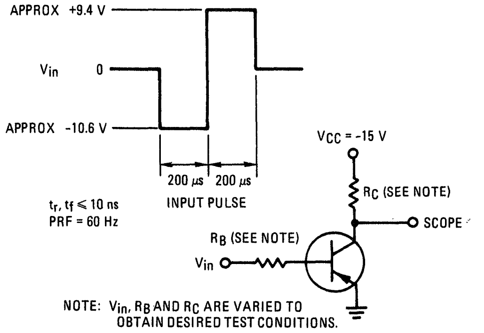


FIGURE 7 – ACTIVE-REGION SAFE-OPERATING AREA

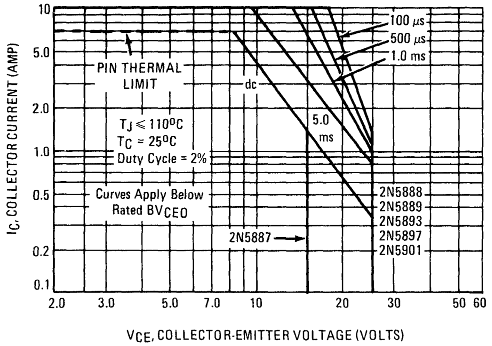


FIGURE 8 – ACTIVE-REGION SAFE-OPERATING AREA

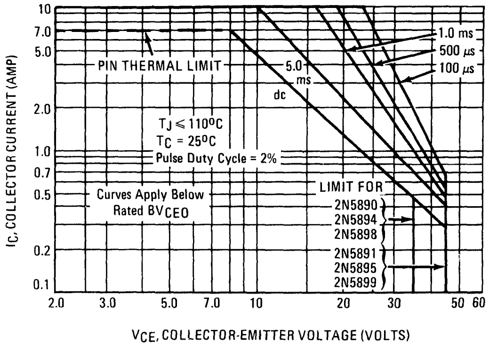


FIGURE 9 – ACTIVE-REGION SAFE-OPERATING AREA

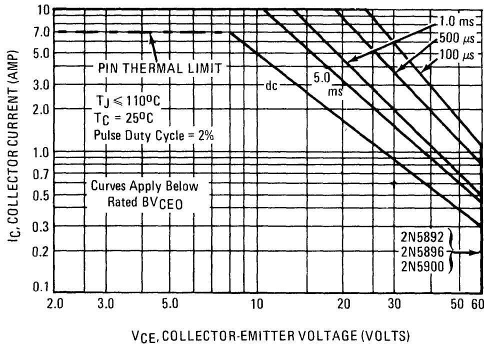


FIGURE 10 – CURRENT-GAIN–BANDWIDTH PRODUCT

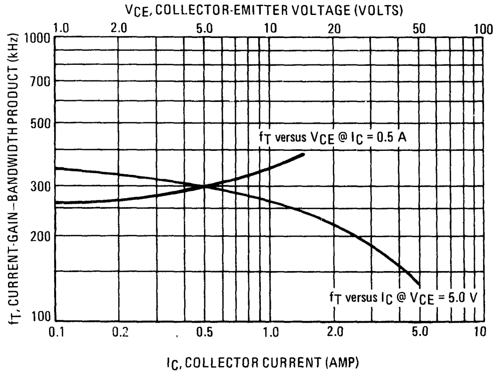


FIGURE 11 – EFFECTS OF BASE-EMITTER RESISTANCE

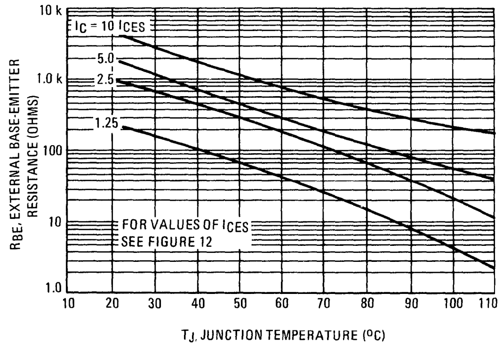


FIGURE 12 – COLLECTOR CUTOFF REGION

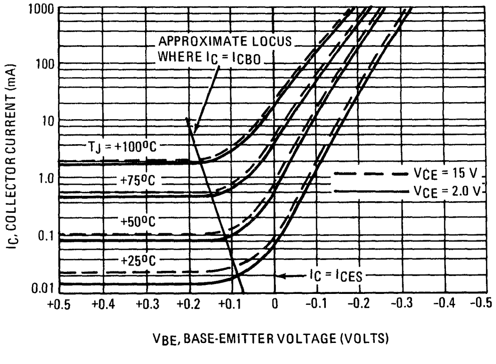


FIGURE 13 – DC CURRENT GAIN

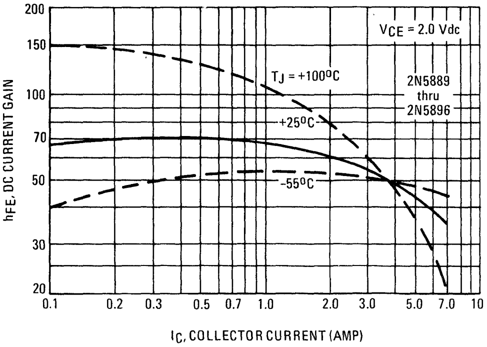


FIGURE 14 – DC CURRENT GAIN

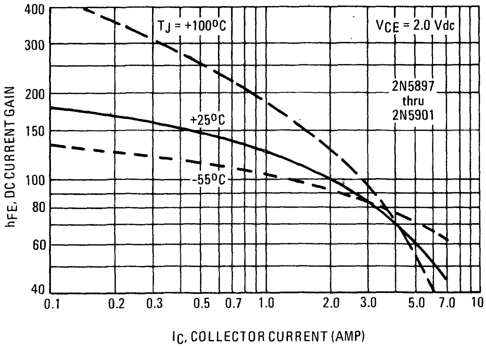


FIGURE 15 – COLLECTOR SATURATION REGION

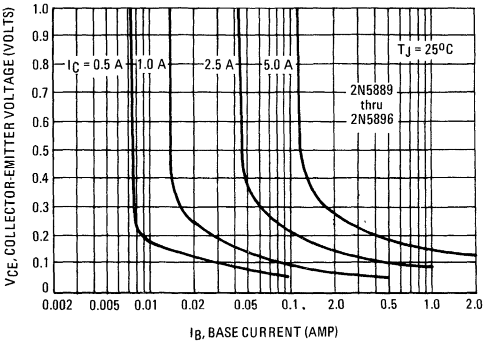


FIGURE 16 – COLLECTOR SATURATION REGION

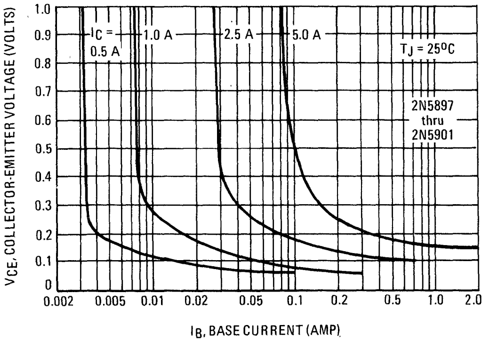


FIGURE 17 – "ON" VOLTAGES

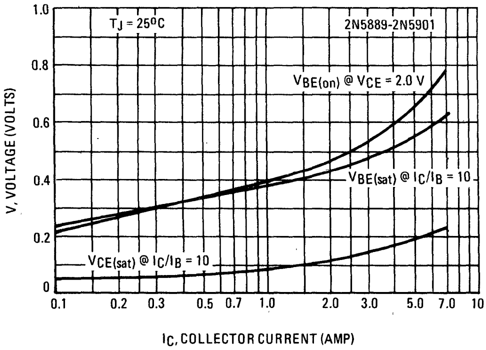
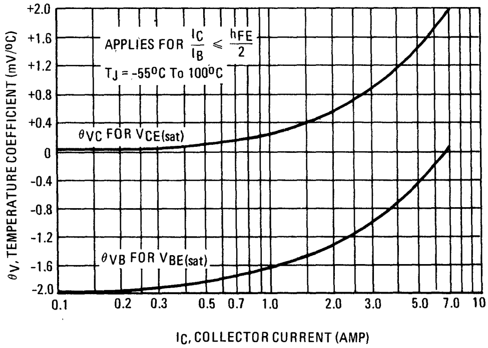


FIGURE 18 – TEMPERATURE COEFFICIENTS



2N5941 (SILICON)
2N5942

The RF Line

NPN SILICON RF POWER TRANSISTORS

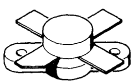
. . . designed primarily for applications as a high-power linear amplifier from 2.0 to 30 MHz, in single sideband mobile, marine and base station equipment.

- Specified 28 Volt, 30 MHz Characteristics –
  Output Power = 40 W (PEP) – 2N5941
  = 80 W (PEP) – 2N5942
  Minimum Gain = 13 dB
  Efficiency = 40%
  Intermodulation Distortion = –30 dB (Max)
- Isothermal-Resistor Design Results in Rugged Device
- 2N5942 Available as Matched Pairs for Push-Pull Amplifier Applications

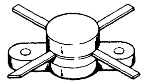
40 W (PEP)–30 MHz – 2N5941
80 W (PEP)–30 MHz – 2N5942

RF POWER TRANSISTORS

NPN SILICON



2N5941

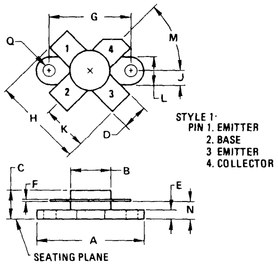


2N5942

MATCHING PROCEDURE

In the push-pull circuit configuration two device parameters are critical for optimum circuit performance. These parameters are $V_{BE(on)}$ and h_{FE}. Both parameters can be guaranteed by measuring I_{CQ} of the devices and selecting pairs with a $\Delta I_{CQ} \leqslant 10$ mAdc.

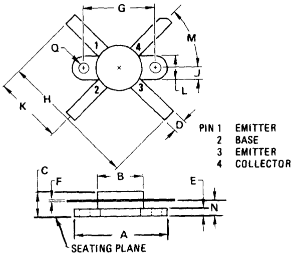
Actual I_{CQ} matching is performed in the 2N5942 test circuit with a V_{CE} equal to 28 Volts. The base bias supply is adjusted to set I_{CQ} equal to 40 mAdc using a reference standard 2N5942. The I_{CQ} of all production 2N5942 transistors is measured using this base bias supply setting. The production 2N5942's are tested and categorized in ranges of 10 mAdc. Finally, the devices are stocked as pairs with a guaranteed $\Delta I_{CQ} \leqslant 10$ mAdc.



2N5941

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.64	24.89	0.970	0.980
B	9.47	9.73	0.373	0.383
C	6.07	7.14	0.239	0 281
D	5.59	5.84	0.220	0.230
E	2 16	2.67	0 085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	21.59	22.10	0 850	0.870
J	3.12	3.23	0.123	0.127
K	10.80	11.05	0.425	0.435
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.97	3.12	0.117	0.123

CASE 211-01



2N5942

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.64	24.89	0.970	0.980
B	11.81	12.07	0.465	0.475
C	5.82	6.73	0.229	0.265
D	2.16	3.94	0.085	0.155
E	2.13	2.54	0.084	0.100
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	35.56	38.10	1.400	1.500
J	3.12	3.23	0.123	0.127
K	17.78	19.05	0.700	0.750
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.66	4.32	0 144	0.170
Q	2.97	3.12	0.117	0.123

CASE 211-02

*MAXIMUM RATINGS

Rating	Symbol	2N5941	2N5942	Unit
Collector-Emitter Voltage	V_{CEO}	35		Vdc
Collector-Base Voltage	V_{CBO}	65		Vdc
Emitter-Base Voltage	V_{EBO}	4.0		Vdc
Collector Current – Continuous	I_C	6.0	12	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.457	140 0.8	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +200		°C

*Indicates JEDEC Registered Data

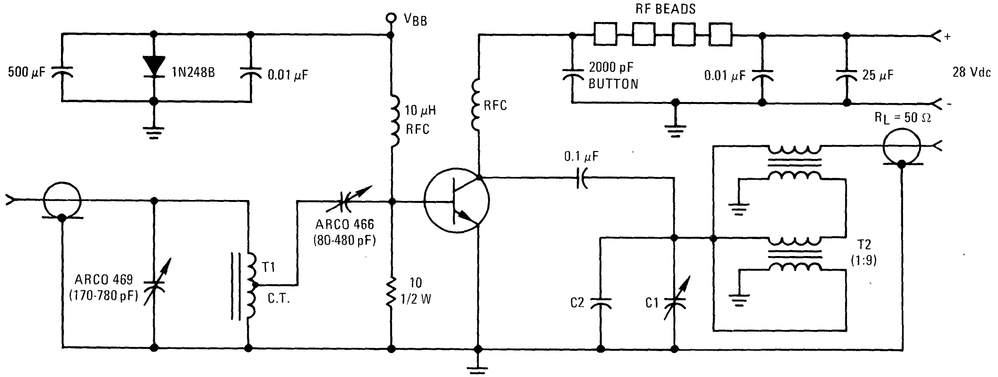
These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)		BV_{CEO}	35	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)		BV_{CES}	65	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)		BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0, T_C = +55°C)	2N5941 2N5942	I_{CES}	– –	5.0 10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	2N5941 2N5942	h_{FE}	10 10	– –	–
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 0.25 Adc, V_{CE} = 15 Vdc, f = 50 MHz) (I_C = 0.5 Adc, V_{CE} = 15 Vdc, f = 50 MHz)	2N5941 2N5942	f_T	50 50	– –	MHz
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	2N5941 2N5942	C_{ob}	– –	125 250	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 40 W (PEP), I_C = 1.78 Adc (Max), V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz) (P_{out} = 80 W (PEP), I_C = 3.575 Adc (Max), V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	2N5941 2N5942	G_{PE}	13 13	– –	dB
Intermodulation Distortion Ratio (Figure 1) (P_{out} = 40 W (PEP), I_C = 1.78 Adc (Max), V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz) (P_{out} = 80 W (PEP), I_C = 3.575 Adc (Max), V_{CC} = 28 Vdc f_1 = 30 MHz, f_2 = 30.001 MHz)	2N5941 2N5942	IMD	– –	-30 -30	dB
Collector Efficiency (P_{out} = 40 W (PEP), I_C = 1.78 Adc (Max), V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz) (P_{out} = 80 W (PEP), I_C = 3.575 Adc (Max), V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	2N5941 2N5942	η	40 40	– –	%

* Indicates JEDEC Registered Data.

FIGURE 1 — 30 MHz TEST CIRCUIT



RFC. 20 TURNS #12 AWG ENAMELED WIRE CLOSE WOUND IN 2 LAYERS, 1/4" I.D.

T1: 20 TURNS #24 AWG WIRE WOUND ON MICRO-METALS T37-7 TOROID CORE CENTER TAPPED.

T2: 1:9 XFMR; 6 TURNS OF 2 TWISTED PAIRS OF #28 AWG ENAMELED WIRE. (8 CRESTS PER INCH) BIFILAR WOUND ON EACH OF 2 SEPARATE BALUN CORES. (Stackpole #57-1503, No. 14 Material) Interconnected as shown

RF BEADS. FERROXCUBE #56-590-65/3B

V_{BB} adjusted for I_{CQ}. 2N5941 – 20 mAdc
2N5942 – 40 mAdc (I_{CQ} = Quiescent Collector Current)

C1 – 2N5941 – 80-480 pF, ARCO 466 or Equiv
2N5942 – 170-780 pF, ARCO 469 or Equiv
C2 – 2N5941 – 220 pF
2N5942 – 330 pF

LINEAR OUTPUT POWER versus FREQUENCY

FIGURE 2 – 2N5941

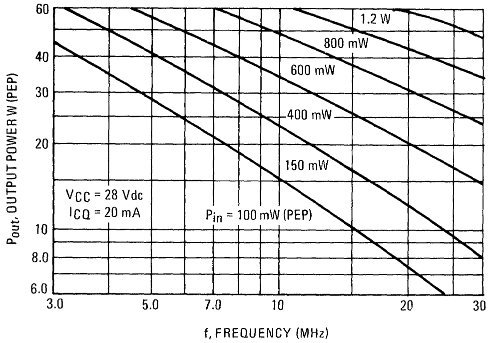
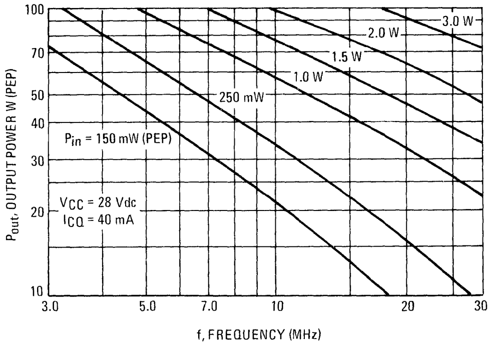


FIGURE 3 – 2N5942



OUTPUT POWER versus INPUT POWER

FIGURE 4 – 2N5941

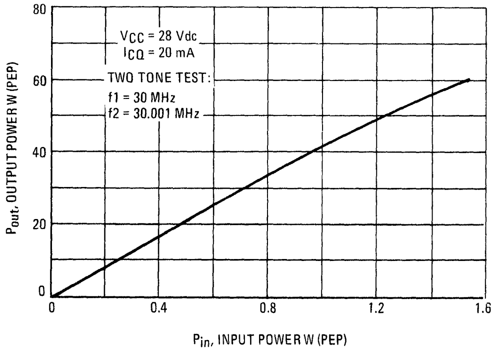


FIGURE 5 – 2N5942

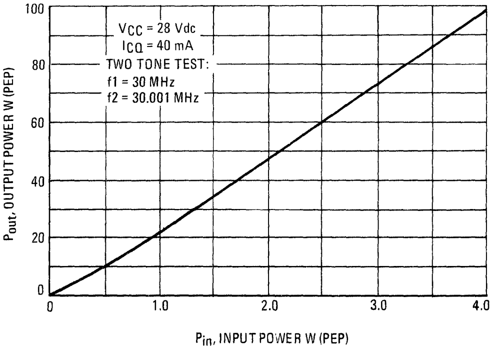


FIGURE 6 – 2N5941

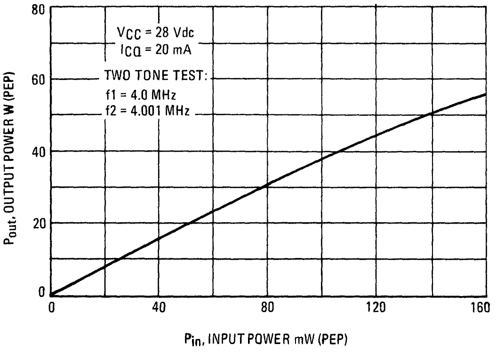
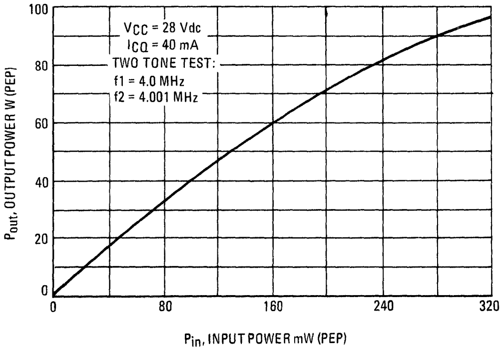


FIGURE 7 – 2N5942



INTERMODULATION DISTORTION versus OUTPUT POWER

(f1 = 30 MHz, f2 = 30.001 MHz)

FIGURE 8 – 2N5941

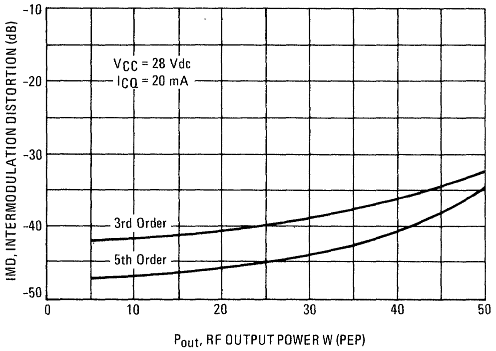
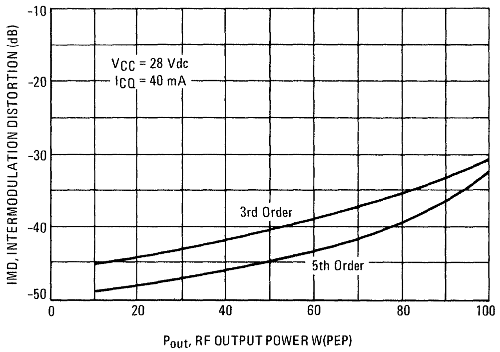


FIGURE 9 – 2N5942



LINEAR OUTPUT POWER versus SUPPLY VOLTAGE

(f1 = 30 MHz, f2 = 30.001 MHz)

FIGURE 10 – 2N5941

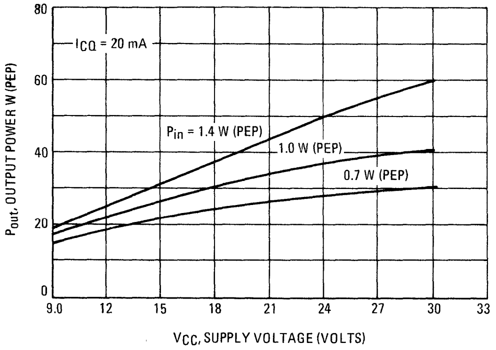


FIGURE 11 – 2N5942

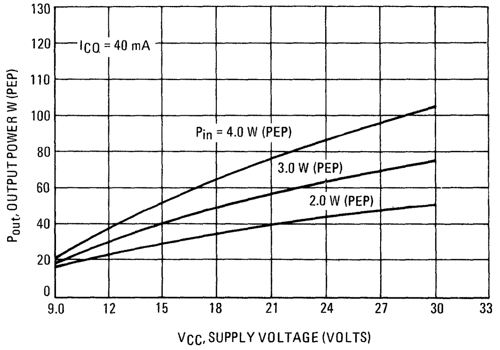


FIGURE 12 – 2N5941

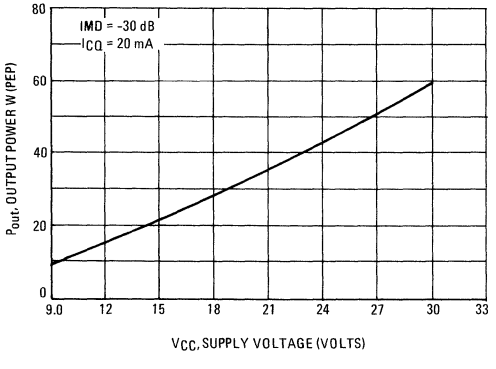
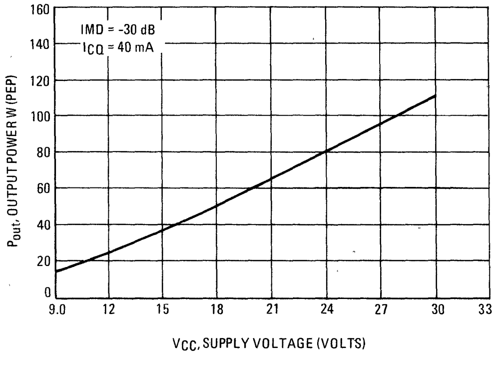


FIGURE 13 – 2N5942



PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

FIGURE 14 – 2N5941

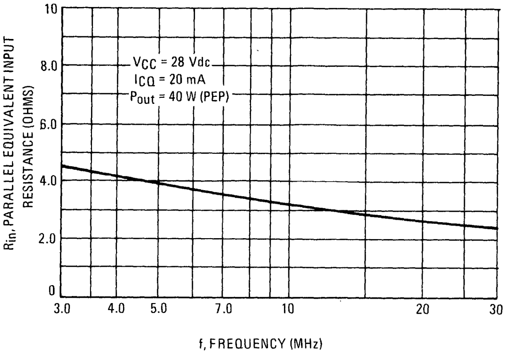
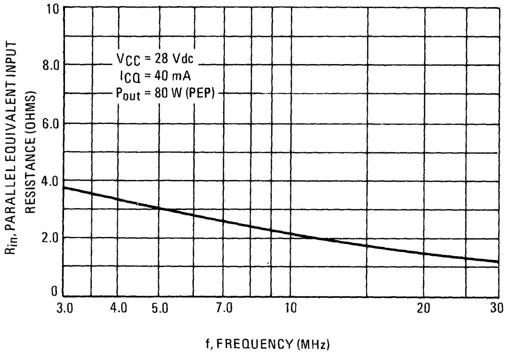


FIGURE 15 – 2N5942



PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

FIGURE 16 – 2N5941

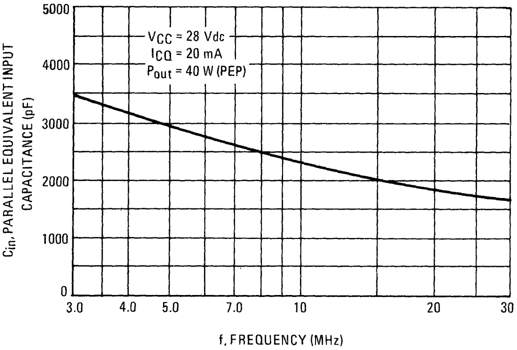
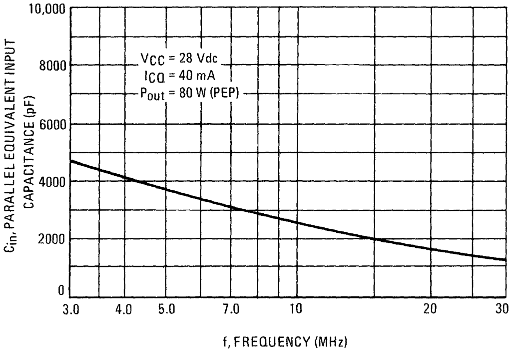


FIGURE 17 – 2N5942



PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

FIGURE 18 – 2N5941

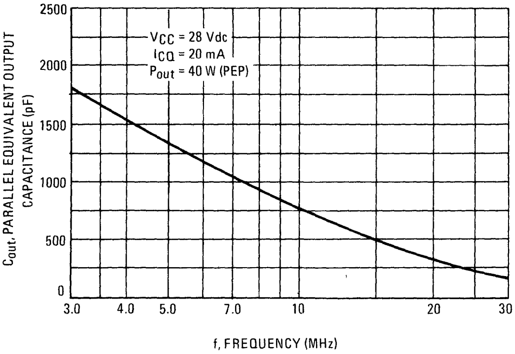
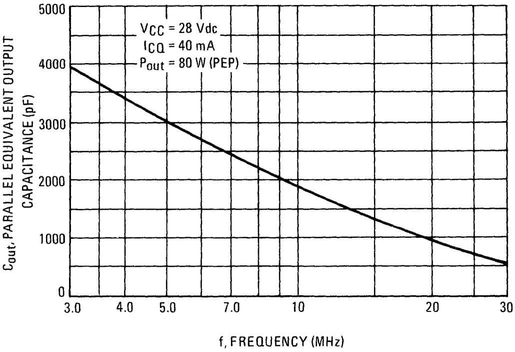


FIGURE 19 – 2N5942



COLLECTOR CURRENT versus BASE-EMITTER VOLTAGE

FIGURE 20 – 2N5941

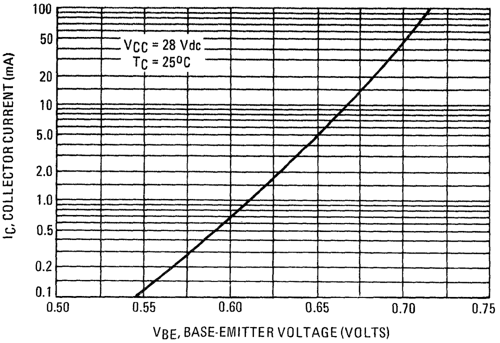
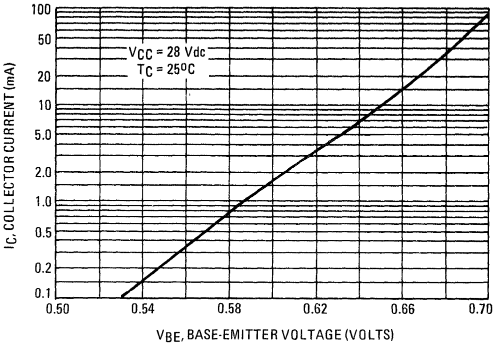


FIGURE 21 – 2N5942



SAFE OPERATING AREA

FIGURE 22 – 2N5941

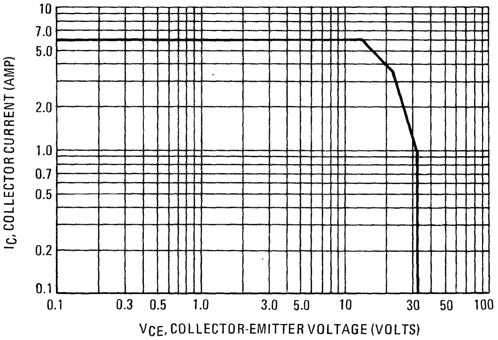


FIGURE 23 – 2N5942

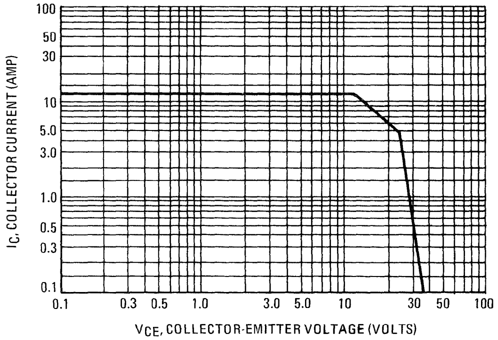
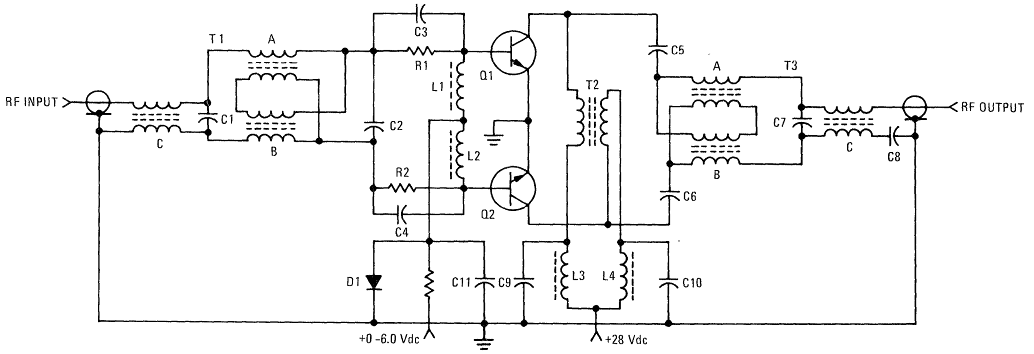


FIGURE 24 – PUSH-PULL 120-WATT PEP, 2-30 MHz LINEAR AMPLIFIER

G_{PE} = 13.5 dB, IMD = -31 dB (Typ)



C1	91 pF Dipped Mica
C2	680 pF Dipped Mica
C3,C4	3900 pF Ceramic (Total Lead Length to Bases Not to Exceed 3/4")
C5,C6	0.047 μF Polyester Film (Total Lead Length to Collectors Not to Exceed 1/2")
C7	27 pF Dipped Mica
C8	3300 pF Ceramic
C9,C10	0.33 μF Ceramic
C11	500 μF, 6.0 Volt Electrolytic
R1,R2	5.0 Ohm, (Two 10 Ohm, 1/2 Watt Carbon Resistors in Parrallel)
R3	20 Ohms, 10 Watts
L1,L2	10 μH Molded Chokes
L3,L4	FERROXCUBE VK200 19/4B (or 6 Ferrite Beads on #20 AWG)

D1	1N4997 (Mounted to Heat Sink Near Q1 and Q2)
Q1,Q2	2N5942 Matched Pair
T1	A and B Consist of 5 Turns of 4 Pairs of #32 AWG loosely twisted, Enameled Wires Wound on the Outer Toroids of INDIANA GENERAL TV Antenna Balum Core F684-1. C = 2 Pairs of #32 AWG Wound on the Inner Toroid of the Balum Core
T2	Collector Choke, 4 Turns, 2 Twisted Pairs of #22 AWG Enameled Wire (4 Twists Per Inch), Wound on INDIANA GENERAL F627-8Q1 or Equivalent Toroid.
T3	A and B Consist of 5 Turns, 2 Twisted Pairs of #24 AWG, C Consists of 10 Turns, 1 Twisted Pair of #24 AWG Enameled Wire. (All Winding 6 Twists Per Inch) Core = INDIANA GENERAL F624-19Q1 or Equivalent.

NOTE For more information on transformers, see AN-593, "Broadband Linear Power Amplifiers Using Push-Pull Transistors."

The maximum theoretical output from a 28 Volt push-pull amplifier, with a 1:4 output transformer, is 110-112 Watts, due to the limited voltage swing (assuming the transformer is a perfect 1:4). In most transmission line type transformers, the transformation ratio is usually higher, especially at the higher frequencies. Thus, depending on the amount of flat-topping that can be tolerated, and the compensation techniques of the transformer higher power outputs can be realized at reasonably low distortion. Ideally a 1:6 output transformer would be required for a power output of 150 Watt PEP.

APPLICATIONS INFORMATION

The 2N5941 and 2N5942 transistors are designed for linear power amplifier operation in the HF region (2 to 30 MHz). They feature guaranteed linear amplifier performance rather than the conventional performance demonstrated in a class C* amplifier.

Class C operation is inherently non-linear, but in many power amplifier applications non-linear operation does not present major problems. With a single frequency driving signal, the only spurious signals generated are harmonics and these can be suppressed in the amplifier tuned networks and output filter.

For single sideband (SSB), low level amplitude modulation (AM), and other types of complex signals, class C operation is generally not satisfactory. For instance, when a signal contains multiple frequencies at close spacings, odd-order non-linearities will generate spurious outputs which are within the passband of the tuned circuits and filters; therefore, the spurious outputs are not suppressed before they reach the antenna or other load. As a result, such complex signals require linear amplification if the amplified signal is to be free of spurious outputs.

A detailed analysis of spurious signals generated by non-linearities and linearity requirements of various applications is described in Chapter 12 of Reference 1.

The following discussion concerns itself with a detailed description of the 2N5941-2 characterization curves and general information on solid-state linear power amplifier design.

The Two-Tone Test

The 2N5941-42 functional test specification consists of a linear power amplifier test with guaranteed limits on power output, gain, efficiency, and intermodulation distortion (IMD) output levels. A two-tone test signal is used with the test amplifier as shown in Figure 1.

The two-tone test is one of many methods commonly used for testing linear amplifier performance. This test involves driving the amplifier with two RF signals, of equal amplitude, separated in frequency from each other by approximately 1 kHz.

When a two-tone test signal consisting of frequencies f_1 and f_2 is passed through a non-linear amplifier, odd order non-linearities generate spurious signals near the desired carrier. The level of these spurious signals provides a measure of the degree of non-linearity of the amplifier. This type of non-linearity is called intermodulation distortion (IMD). The spurious signals generated by IMD are further classified according to the exponential order of the amplifier non-linearity, i.e., 3rd order IMD products, 5th order IMD products, etc. The 3rd and 5th order IMD products are usually the most significant encountered with linear power amplifiers. Data on both 3rd and 5th order IMD are included in the 2N5941-42 characterization.

Third order IMD generates spurious signals near the operating frequency at frequencies $2f_1 - f_2$ and $2f_2 - f_1$; and 5th order IMD spurious signals are at frequencies $3f_1 - 2f_2$ and $3f_2 - 2f_1$.

Specifications and Characterization

The two-tone functional amplifier test is performed in a manner identical to the conventional class C functional test with two exceptions: a two-frequency signal is used in place of a single frequency, and amplifier linearity is added to the items tested and specified.

The functional test procedure for the 2N5941-42 requires driving the test amplifier with a two-frequency signal and measuring power output, gain, efficiency, and linearity.

Power output, gain, and efficiency measurement methods are the same for both linear and class C amplifiers.

Since a multiple frequency test signal has an instantaneous power level which varies with time, power levels are normally expressed in peak envelope power (PEP). This is the average power level of the envelope at its greatest amplitude point.

When the test signal consists of multiple signals with equal amplitudes and different frequencies, the relationship of average power and PEP is given by the following expression:

$$\text{Average power} = \frac{\text{PEP}}{N}$$

where N = the number of input frequencies.

Therefore, when measuring the power level of a standard two-tone test signal, a true average reading power meter will indicate 1/2 the PEP of the signal.

Linearity is tested by measuring the amplitudes of the 3rd and 5th order IMD products. The ratio of one of the 3rd order products to one of the two desired frequencies is then expressed as a power ratio in decibels (dB). This is repeated for the 5th order products. The smaller of these two ratios (usually the 3rd order) is then included in the electrical characteristics specification as intermodulation distortion ratio (IMD).

2N5941-42 Performance Curves

Figures 2 through 7 show typical power output and gain characteristics versus frequency and/or input power. These curves are similar to those found on other RF power transistor data sheets with one exception, a two-frequency test signal was used rather than a single frequency signal.

The curves shown in Figures 8 and 9 are unique to transistors characterized for linear power amplifier service and show the typical IMD levels versus power output.

The 2N5941-42 feature guaranteed IMD performance at the -30 dB level. However, the designer may desire IMD greater or less than -30 dB for a particular application. Figures 8 and 9 provide data on IMD levels that can be expected as a function of output power.

Figures 10 and 11 show the variation in gain with dc supply voltage and provide data on gain only. They do not include information on IMD ratio.

Figures 12 and 13 reflect the power output that can be obtained at a fixed IMD ratio for operation with dc supply voltages other than 28 Vdc.

Figures 14 through 19 show the large signal impedance characteristics of the 2N5941-42. These are similar to curves shown on other Motorola data sheets except a two-frequency test signal was used rather than a single frequency signal.

It must be stressed that the data shown in Figures 14 through 19 do not represent y, z, h, s, or any standard two-port parameter set. The actual transistor impedance levels during normal operation in an amplifier are given. For a detailed discussion of RF power transistor large signal impedance, see Reference 2.

Linear Amplifier Design

The following is a discussion of some general design considerations for solid-state linear power amplifiers. While this is not a detailed analysis of linear amplifier design, some general guidelines are provided.

The major difference between linear power amplifiers and class C power amplifiers is in the dc bias circuitry. As stated in the introduction, class C operation usually involves a collector dc supply as

APPLICATIONS INFORMATION (continued)

the only bias voltage with $V_E = V_B = 0$. The collector current is zero until the input RF signal turns the transistor "on".

In contrast, a linear amplifier is normally operated with forward bias and some collector current flowing when no signal is present.

The magnitude of no-signal collector current and the bias circuitry may vary with the application. Optimum no-signal collector currents for the 2N5941 and 2N5942 were found to be approximately 20 mA and 40 mA respectively.

The key to bias circuitry for good linearity lies in maintaining the base-emitter dc voltage relatively constant as the RF signal amplitude varies. The inherent nature of a forward-biased RF power transistor is to bias itself "off" with increasing RF drive signal. Therefore, a constant voltage source is required for base voltage.

Temperature effects also complicate the situation, since V_{BE} decreases with increasing temperature.

A simple solution to the bias problem involves the use of a forward-biased diode mounted on the transistor heat sink for thermal coupling to the transistor. A sample of this technique is shown in the test circuit of Figure 1. The capacitor in parallel with the diode helps maintain a constant V_{BE} with RF drive and improves linearity, while the diode provides temperature compensation to prevent thermal runaway. It is also possible to use complex active circuitry for biasing, and some rather exotic schemes have been developed to provide the same results.

Another important consideration is the collector-output network. Normally, a network with low impedance to ground for harmonics provides better linearity than a network with high harmonic impedances; therefore, some experimentation with network configuration is in order. Proper impedance matching remains the primary factor in both input and output network design. Further, it must also be stressed that the collector load impedance should be designed for the PEP, not the average power output. See Chapter 13 of Reference 1 for a detailed discussion of network design considerations.

Feedback may also be employed to improve linearity and may take the form of either neutralization or negative RF feedback. The possibilities here are limited only by the designer's imagination. Of course, negative RF feedback involves a decrease in gain to improve linearity.

REFERENCES

1. Pappenfus, Bruene, Schoenike, "Single Sideband Principles and Circuits", McGraw-Hill.
2. Hejhall, "Systemizing RF Power Amplifier Design", Motorola Semiconductor Products Inc., Application Note AN-282A.

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*"Class C", as used here refers to operation with the no signal conditions $I_C = 0$, and $V_{BE} = 0$, and a theoretical conduction angle of less than 180°, even though the actual conduction angle may be more than 180°.

2N5943 (SILICON)

The RF Line

NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed specifically for broadband applications requiring low cross-modulation distortion and low-noise figure. Characterized for use in CATV applications. The 2N5943 was formerly MM8002.

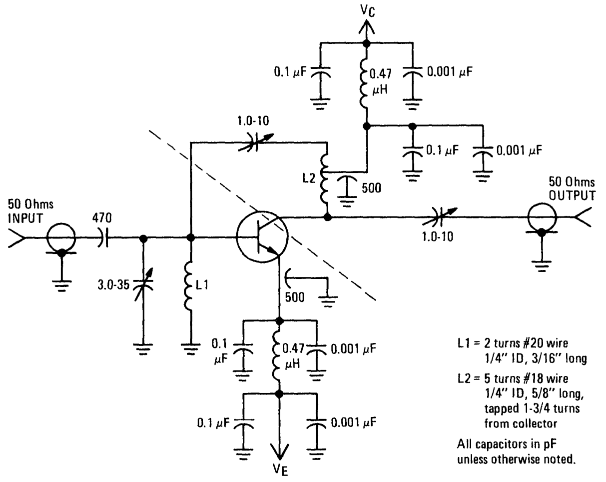
- Low Noise Figure — @ f = 200 MHz
  NF (Narrowband) = 3.4 dB (Typ)
  NF (Broadband) = 6.8 dB (Typ)
- High Current-Gain — Bandwidth Product —
  f_T = 1200 MHz (Min) @ I_C = 50 mAdc
- Completely Characterized with S and Y-Parameters

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	3.5	Vdc
Collector Current — Continuous	I_C	400	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 5.7	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.5 0.02	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

FIGURE 1 — NARROW-BAND TEST CIRCUIT

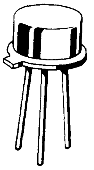


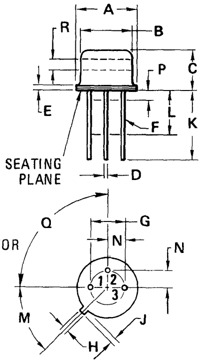
L1 = 2 turns #20 wire
1/4" ID, 3/16" long

L2 = 5 turns #18 wire
1/4" ID, 5/8" long,
tapped 1-3/4 turns
from collector

All capacitors in pF
unless otherwise noted.

NPN SILICON HIGH-FREQUENCY TRANSISTOR





STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.
CASE 79-02
TO-39

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	BV_{CEO}	30	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.5	–	–	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	I_{CEO}	–	–	50	μAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 15 Vdc)	h_{FE}	25	–	300	–
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	–	0.15	0.2	Vdc
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{BE(sat)}$	–	0.88	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (Figure 2)	f_T				MHz
(I_C = 25 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)		1000	1350	–	
(I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)		1200	1550	2400	
(I_C = 100 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)		1000	1425	–	
Collector-Base Capacitance (Figure 5) (V_{CB} = 30 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	1.0	1.6	2.5	pF
Emitter-Base Capacitance (Figure 5) (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	8.4	15	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 1.0 kHz)	h_{fe}	25	–	350	–
Collector-Base Time Constant (I_E = 50 mAdc, V_{CB} = 15 Vdc, f = 31.8 MHz)	$r_b'C_c$	2.0	5.5	20	ps
Noise Figure	NF				dB
(I_C = 30 mAdc, V_{CE} = 15 Vdc, f = 200 MHz) (Figure 1)		–	3.4	–	
(I_C = 35 mAdc, V_{CE} = 15 Vdc, f = 200 MHz) (Figures 6, 11, 14) (1)		–	6.8	8.0	
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain	G_{pe}				dB
(I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 200 MHz) (Figure 1)		–	11.4	–	
(I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 250 MHz) (Figure 6)		7.0	7.6	–	
Intermodulation Distortion (Figure 7) (I_C = 50 mAdc, V_{CE} = 15 Vdc, V_{out} = +50 dBmV)	IM	–	–	-50	dB
Cross Modulation Distortion (Figure 8)	XM				dB
(I_C = 50 mAdc, V_{CE} = 15 Vdc, V_{out} = +40 dBmV)		–	-67	–	
(I_C = 50 mAdc, V_{CE} = 15 Vdc, V_{out} = +50 dBmV)		–	-42	-45	

*Indicates JEDEC Registered Data.

(1) Includes noise figure of post-amplifier and matching pad.

FIGURE 2 – CURRENT-GAIN – BANDWIDTH PRODUCT

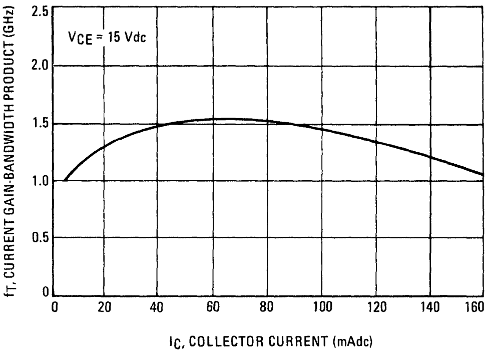


FIGURE 3 – COLLECTOR-BASE TIME CONSTANT

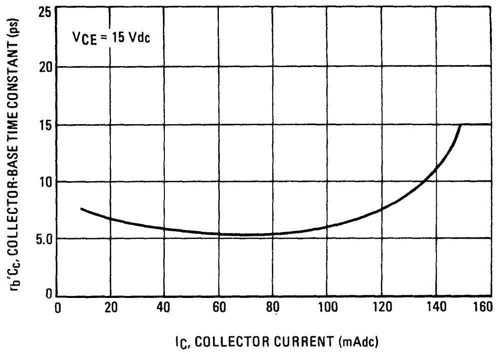


FIGURE 4 – SATURATION VOLTAGES

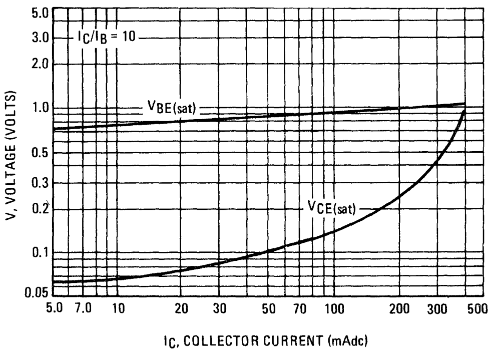


FIGURE 5 – CAPACITANCES versus REVERSE VOLTAGE

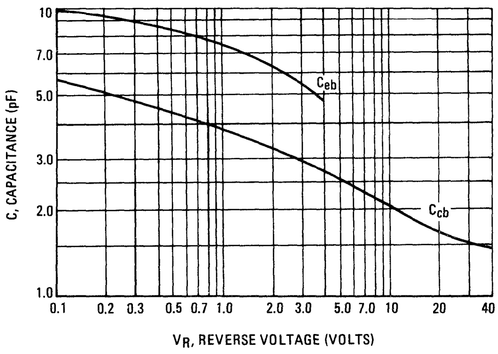
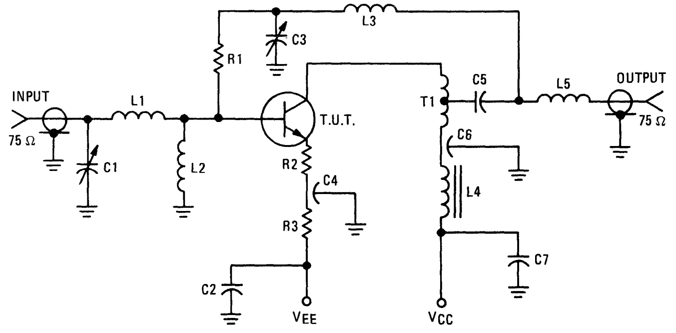


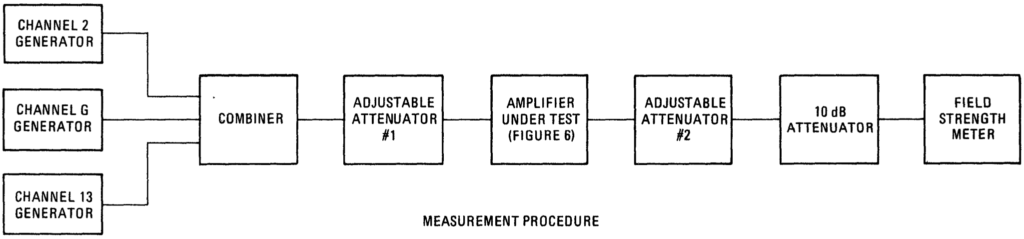
FIGURE 6 – BROADBAND TEST CIRCUIT



C1	1.0-10 pF	JOHANSON 2951 OR EQUIVALENT
C2, C7	0.01 μF	
C3	0.5-6.0 pF	JOHANSON 4642 OR EQUIVALENT
C4, C6	1500 pF	
C5	470 pF	
L1	2 TURNS AWG #26, 5/32" I.D.	
L2	1 μH MOLDED CHOKE	
L3	5 TURNS AWG #26, 3/32" I.D.	
L4	FERRITE CHOKE, 3 TURNS #30 ON STACKPOLE 57-0156 BEAD	
L5	2 TURNS AWG #26, 3/32" I.D.	
T1	AWG #30 TRIFILAR WOUND 1-9-9 ON STACKPOLE 57-0985, #11 TOROID	
R1	270 OHMS	
R2	18 OHMS	
R3	150 OHMS	

GARLOCK TEFLON SOCKET

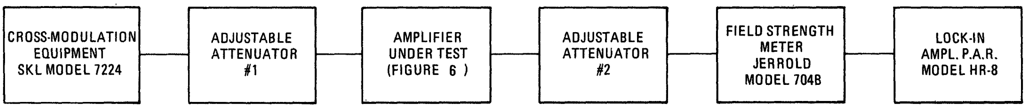
FIGURE 7 – INTERMODULATION DISTORTION TEST SETUP AND PROCEDURE



MEASUREMENT PROCEDURE

1. ADJUST CHANNEL 2 GENERATOR FOR RATED OUTPUT FROM TEST AMPLIFIER (CHANNELS G & 13 OFF).
2. REPEAT FOR CHANNEL G (2 & 13 OFF) AND CHANNEL 13 (2 & G OFF). NOTE FOR REFERENCE THE FIELD STRENGTH METER READING FOR CHANNEL 13 (2 & G OFF).
3. TURN CHANNEL 13 OFF AND DRIVE THE TEST AMPLIFIER WITH CHANNELS 2 & G. MEASURE THE LEVEL OF INTERMODULATION DISTORTION AT CHANNEL 13 RELATIVE TO THE REFERENCE LEVEL IN STEP 2.

FIGURE 8 – CROSS-MODULATION DISTORTION TEST SETUP AND PROCEDURE



MEASUREMENT PROCEDURE

1. ADJUST THE CROSSMODULATION EQUIPMENT FOR +40 dBmV OUTPUT FROM EACH CHANNEL.
2. ADJUST ATTENUATOR #1 FOR THE DESIRED OUTPUT LEVEL FROM THE TEST AMPLIFIER. ADJUST ATTENUATOR #2 TO MAINTAIN THE FIELD STRENGTH METER INPUT AT +10 dBmV.
3. WITH THE FIELD STRENGTH METER SELECT CHANNEL 13. USING THE WAVE ANALYZER MEASURE THE LEVEL OF THE MODULATION ON CHANNEL 13 DUE TO CROSS-MODULATION OF CHANNELS 2-12.

FIGURE 9 – CROSS-MODULATION DISTORTION versus COLLECTOR CURRENT

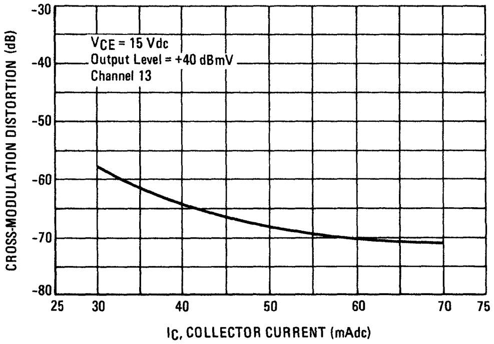


FIGURE 10 – CROSS-MODULATION DISTORTION versus OUTPUT LEVEL

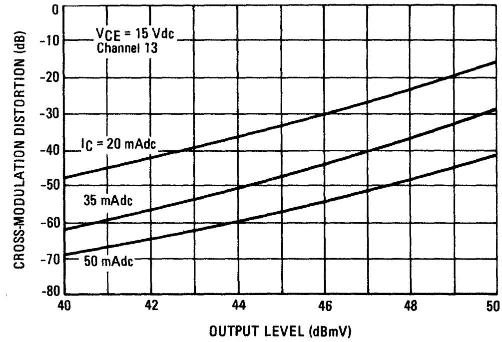
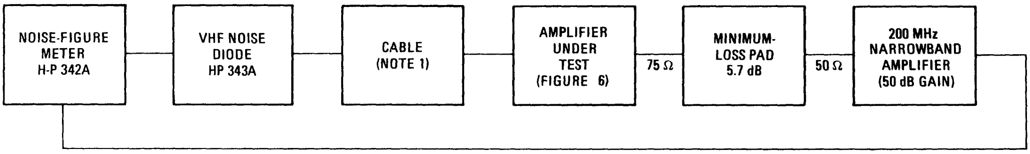


FIGURE 11 – NOISE FIGURE TEST SETUP



NOTE 1. RG-59 CABLE WITH ORIGINAL CENTER CONDUCTOR REPLACED WITH #30 WIRE. OVERALL LENGTH, INCLUDING BNC CONNECTORS, IS A QUARTER-WAVELENGTH AT 200 MHz (APPROX. 11 INCHES). USED TO MATCH IMPEDANCE OF NOISE DIODE TO AMPLIFIER UNDER TEST.

THE NOISE FIGURE OF THE POST-AMPLIFIER AND MINIMUM LOSS PAD IS 8.4 dB.

FIGURE 12 – NARROWBAND NOISE FIGURE versus COLLECTOR CURRENT

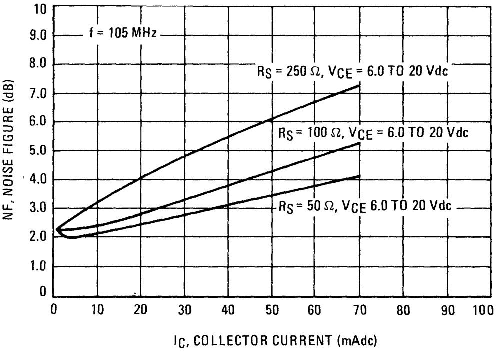


FIGURE 13 – NARROWBAND NOISE FIGURE versus COLLECTOR CURRENT

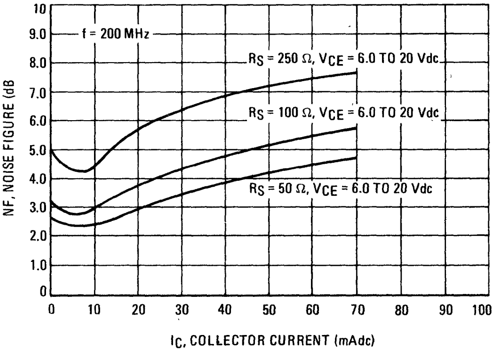


FIGURE 14 – BROADBAND NOISE FIGURE versus COLLECTOR CURRENT

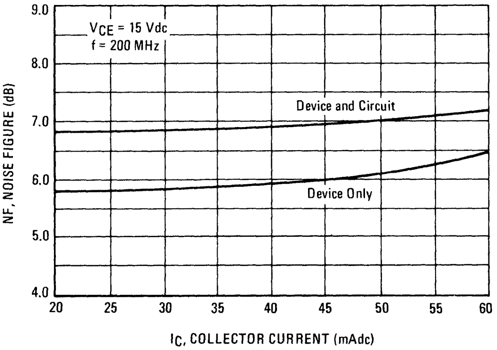


FIGURE 15 – NARROWBAND NOISE FIGURE versus FREQUENCY

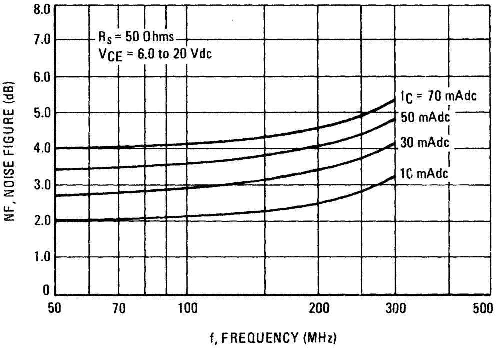


FIGURE 16 – INPUT ADMITTANCE versus FREQUENCY

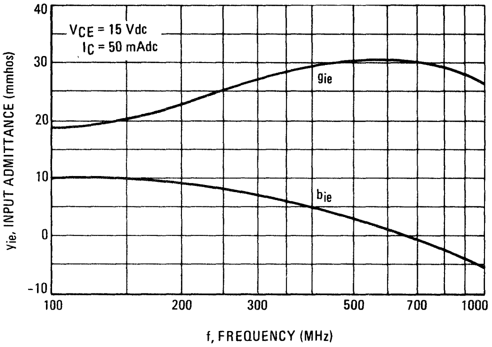


FIGURE 17 – INPUT ADMITTANCE versus COLLECTOR CURRENT

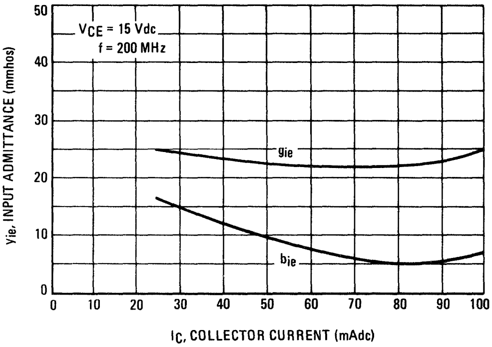


FIGURE 18 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY

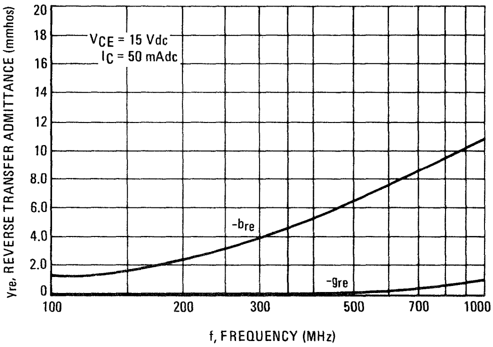


FIGURE 19 – REVERSE TRANSFER ADMITTANCE versus COLLECTOR CURRENT

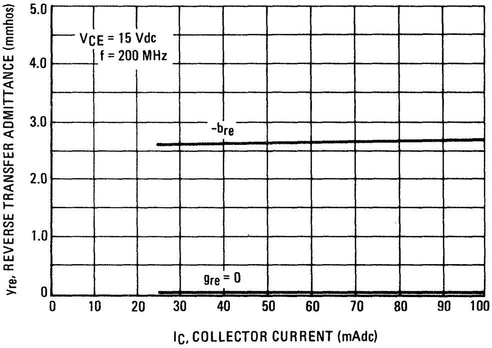


FIGURE 20 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

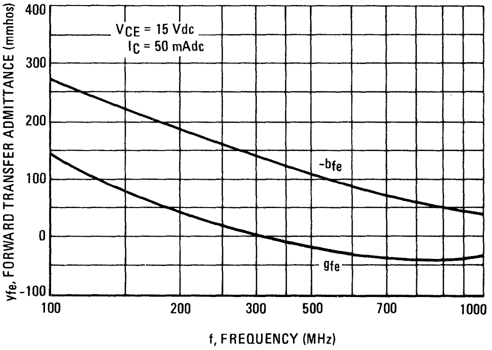


FIGURE 21 – FORWARD TRANSFER ADMITTANCE versus COLLECTOR CURRENT

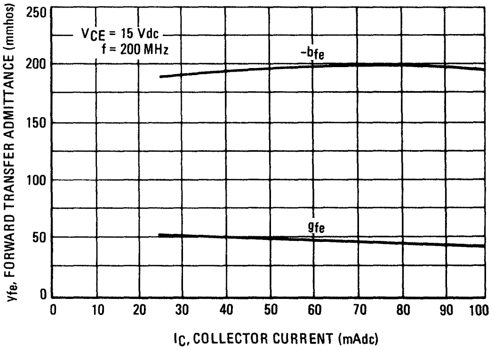


FIGURE 22 – OUTPUT ADMITTANCE versus FREQUENCY

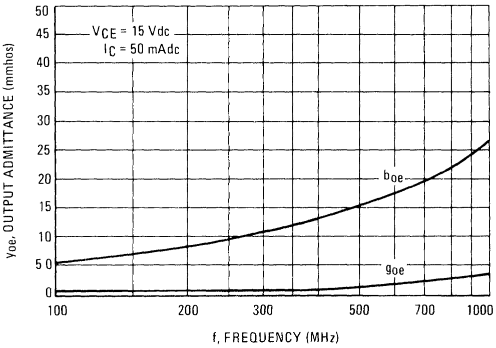


FIGURE 23 – OUTPUT ADMITTANCE versus COLLECTOR CURRENT

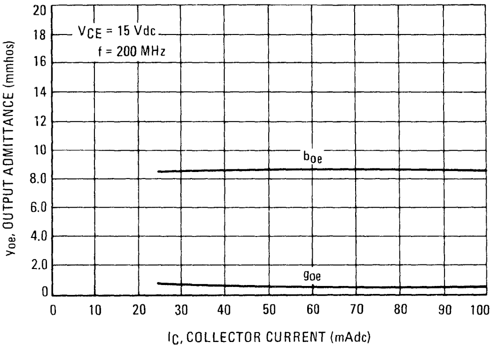


FIGURE 24 – INPUT REFLECTION COEFFICIENT versus FREQUENCY

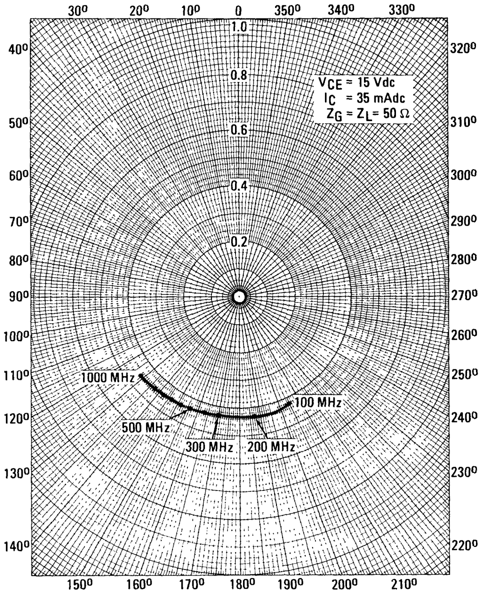


FIGURE 25 – OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

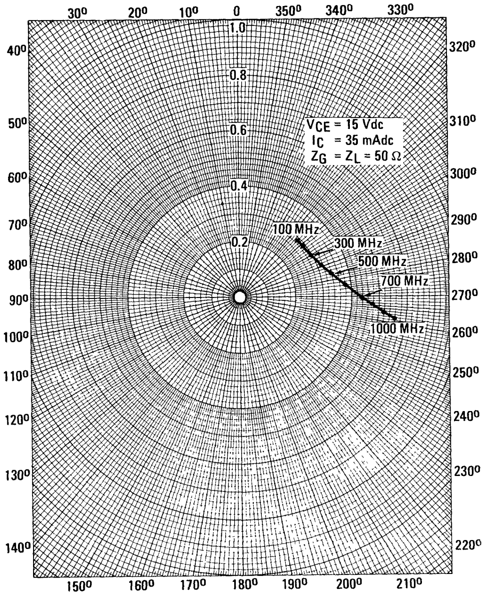


FIGURE 26 – REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY

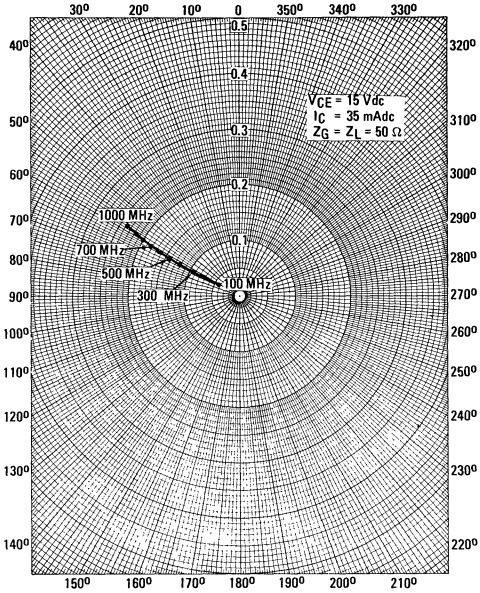


FIGURE 27 – FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY

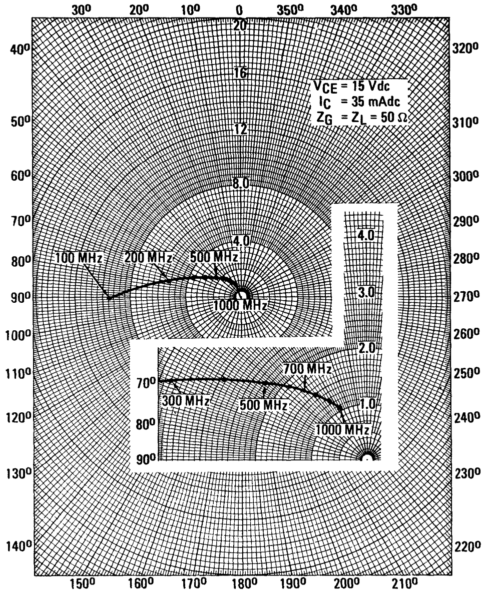
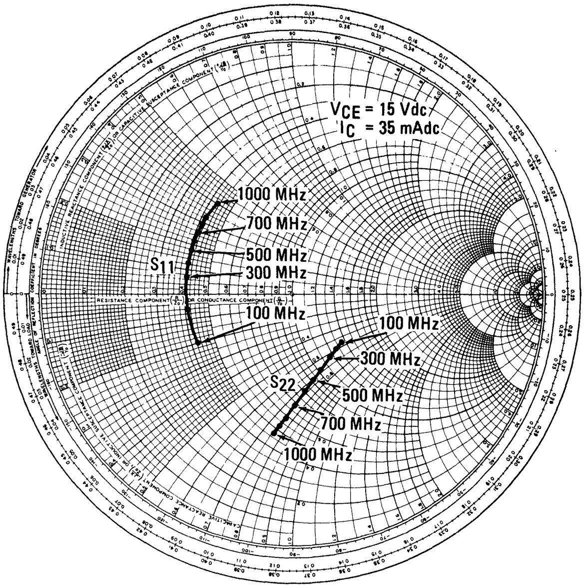


FIGURE 28 – INPUT REFLECTION COEFFICIENT AND OUTPUT REFLECTION COEFFICIENT versus FREQUENCY



2N5944 (SILICON)
2N5945
2N5946

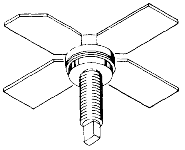
The RF Line

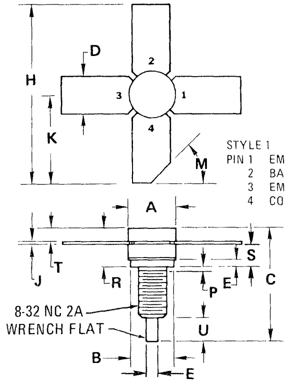
NPN SILICON RF POWER TRANSISTORS

. . . designed for 7.0 to 15 Volts, UHF large signal amplifier applications required in industrial and commercial FM equipment operating in the 400 to 960 MHz range.

- Specified 12.5 Volt, 470 MHz Characteristics –
  Power Output = 2 0 W - 2N5944
  4.0 W – 2N5945
  10 W – 2N5946
  Minimum Gain = 9.0 dB – 2N5944
  8.0 dB – 2N5945
  6.0 dB – 2N5946
  Efficiency = 60% Minimum
- RF ballasting provides protection against device damage due to load mismatch
- Characterized with series equivalent large-signal impedance parameters

2.0, 4.0, 10 W – 470 MHz
RF POWER
TRANSISTORS
NPN SILICON





STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.25	6.45	0.246	0.254
C	15.49	16.51	0.610	0.650
D	5.59	5.84	0.220	0.230
E	1.52 NOM		0.060 NOM	
H	26.80	27.05	1.055	1.065
J	0.127 NOM		0.005 NOM	
K	13.41	13.51	0.528	0.532
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	4.52	5.03	0.178	0.198
S	3.00	3.25	0.118	0.128
T	1.40	1.65	0.055	0.065
U	2.92	3.68	0.115	0.145

CASE 244

MAXIMUM RATINGS

Rating	Symbol	2N5944	2N5945	2N5946	Unit
*Collector-Emitter Voltage	V_{CEO}	← 16 →			Vdc
*Collector-Base Voltage	V_{CBO}	← 36 →			Vdc
*Emitter-Base Voltage	V_{EBO}	← 4 0 →			Vdc
*Collector Current – Continuous	I_C	0 4	0 8	2 0	Adc
*Total Device Dissipation @ $T_C = 25^oC$(1) Derate above 25°C	P_D	5 0 28 5	15 85.5	37 5 214	Watts mW/°C
*Storage Temperature Range	T_{stg}	← -65 to +200 →			°C
Stud Torque(2)	–	← 6 5 →			in-lbs.

*Indicates JEDEC Registered Data

(1) These devices are designed for RF operation The total device dissipation rating applies only when the devices are operated as RF amplifiers

(2) For repeated assembly use 5 in-lbs

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage		BV_{CEO}				Vdc
(I_C = 50 mAdc, I_B = 0)	2N5944		16	–	–	
(I_C = 100 mAdc, I_B = 0)	2N5945		16	–	–	
(I_C = 200 mAdc, I_B = 0)	2N5946		16	–	–	
Collector-Emitter Breakdown Voltage		BV_{CES}				Vdc
(I_C = 50 mAdc, V_{BE} = 0)	2N5944		36	–	–	
(I_C = 100 mAdc, V_{BE} = 0)	2N5945		36	–	–	
(I_C = 200 mAdc, V_{BE} = 0)	2N5946		36	–	–	
Emitter-Base Breakdown Voltage		BV_{EBO}				Vdc
(I_E = 1.0 mAdc, I_C = 0)	2N5944		4.0	–	–	
(I_E = 2.0 mAdc, I_C = 0)	2N5945		4.0	–	–	
(I_E = 4.0 mAdc, I_C = 0)	2N5946		4.0	–	–	
Collector Cutoff Current		I_{CES}				mAdc
(V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 55°C)	2N5944		–	0.2	10	
	2N5945,2N5946		–	0.5	20	
Collector Cutoff Current		I_{CBO}				mAdc
(V_{CB} = 15 Vdc, I_E = 0)	2N5944,2N5945		–	–	1.0	
	2N5946		–	–	2.0	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				–
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	2N5944		20	80	–	
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	2N5945		20	80	–	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	2N5946		20	80	–	
DYNAMIC CHARACTERISTICS						
Output Capacitance		C_{ob}				pF
(V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	2N5944		–	11	15	
	2N5945		–	18	25	
	2N5946		–	38	45	
FUNCTIONAL TEST (Figure 20)						
Common-Emitter Amplifier Power Gain		G_{PE}				dB
(V_{CC} = 12.5 Vdc, P_{out} = 2.0 W, I_C(max) = 267 mAdc, f = 470 MHz)	2N5944		9.0	10	–	
(V_{CC} = 12.5 Vdc, P_{out} = 4.0 W, I_C(max) = 533 mAdc, f = 470 MHz)	2N5945		8.0	9.0	–	
(V_{CC} = 12.5 Vdc, P_{out} = 10 W, I_C(max) = 1.33 Adc, f = 470 MHz)	2N5946		6.0	7.0	–	
Collector Efficiency		η				%
(V_{CC} = 12.5 Vdc, P_{out} = 2.0 W, I_C(max) = 240 mAdc, f = 470 MHz)	2N5944		60	–	–	
(V_{CC} = 12.5 Vdc, P_{out} = 4.0 W, I_C(max) = 500 mAdc, f = 470 MHz)	2N5945		60	–	–	
(V_{CC} = 12.5 Vdc, P_{out} = 10 W, I_C(max) = 1.3 Adc, f = 470 MHz)	2N5946		60	–	–	

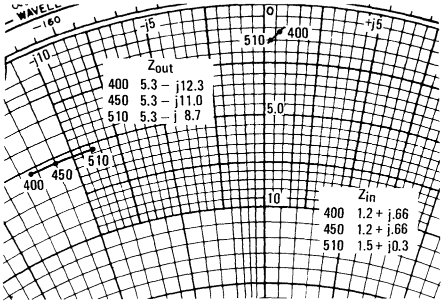
*Indicates JEDEC Registered Data

These devices are available in various packages, such as a studless stripline package, TO-39, and also in chip form on beryllium oxide carriers for hybrid assemblies.

For further information, contact your nearest Motorola representative or the factory representative.

2N5944
TYPICAL PERFORMANCE DATA

FIGURE 1 – SERIES EQUIVALENT IMPEDANCE



V_{CC} = 12.5 Vdc, P_{out} = 2.0 W

FIGURE 2 – OUTPUT POWER versus SUPPLY VOLTAGE

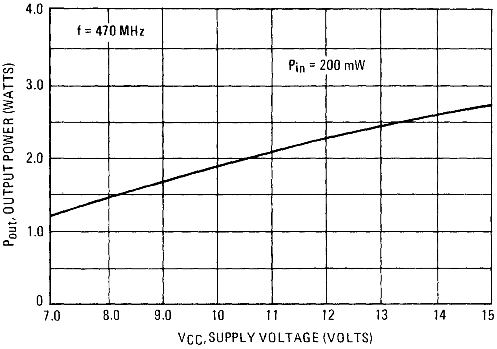


FIGURE 3 – OUTPUT POWER versus INPUT POWER

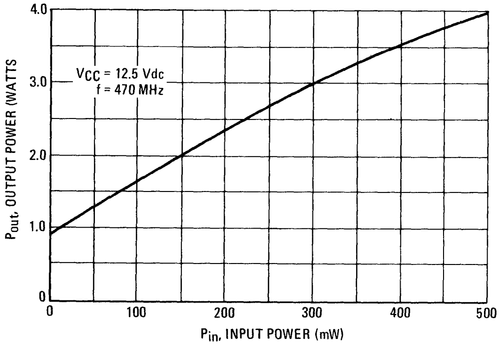


FIGURE 4 – OUTPUT POWER versus FREQUENCY

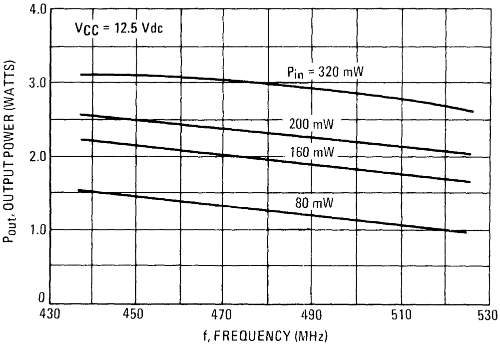


FIGURE 5 – OUTPUT POWER versus INPUT POWER

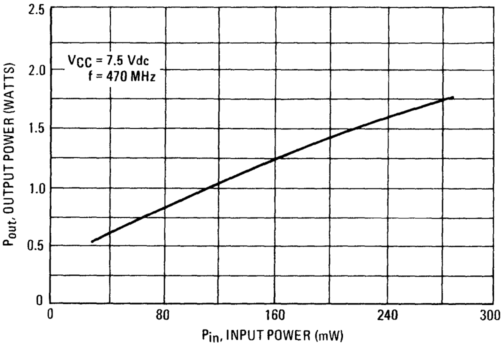
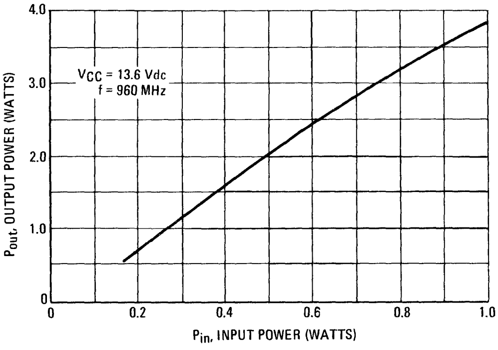
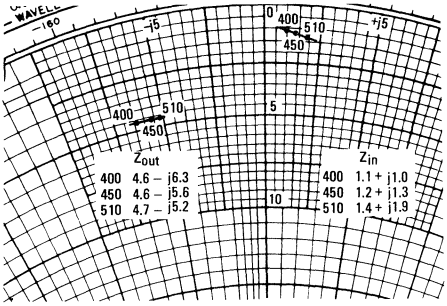


FIGURE 6 – OUTPUT POWER versus INPUT POWER



2N5945
TYPICAL PERFORMANCE DATA

FIGURE 7 – SERIES EQUIVALENT IMPEDANCE



V_{CC} = 12.5 Vdc, P_{out} = 4.0 W

FIGURE 8 – OUTPUT POWER versus SUPPLY VOLTAGE

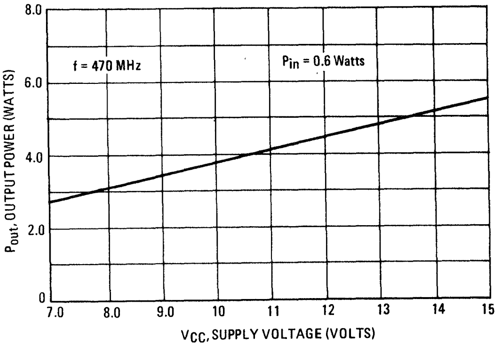


FIGURE 9 – OUTPUT POWER versus INPUT POWER

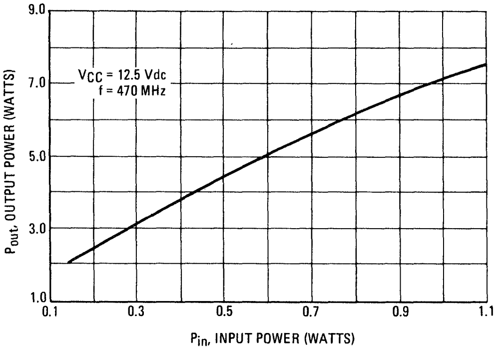


FIGURE 10 – OUTPUT POWER versus FREQUENCY

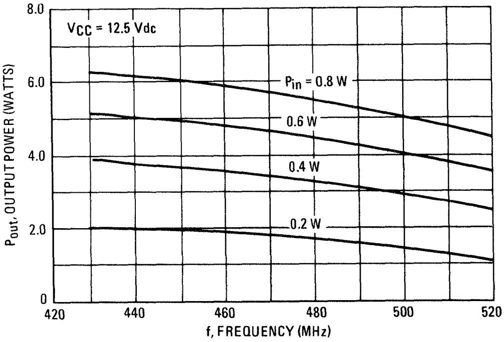


FIGURE 11 – OUTPUT POWER versus INPUT POWER

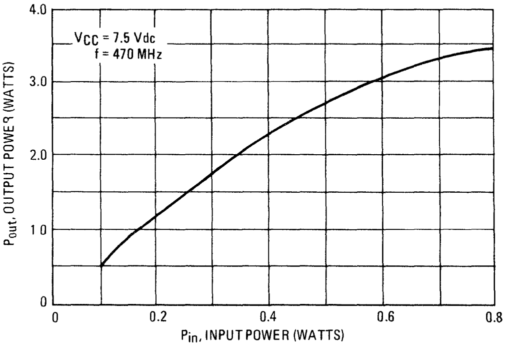
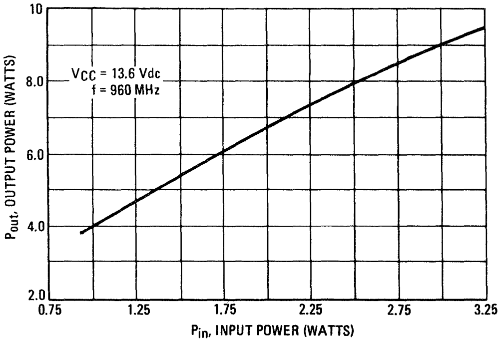
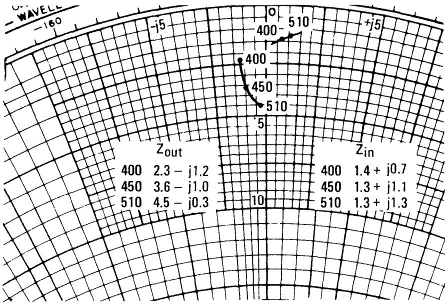


FIGURE 12 – OUTPUT POWER versus INPUT POWER



2N5946
TYPICAL PERFORMANCE DATA

FIGURE 13 – SERIES EQUIVALENT IMPEDANCE



V_{CC} = 12.5 Vdc, P_{out} = 12 W

FIGURE 14 – OUTPUT POWER versus SUPPLY VOLTAGE

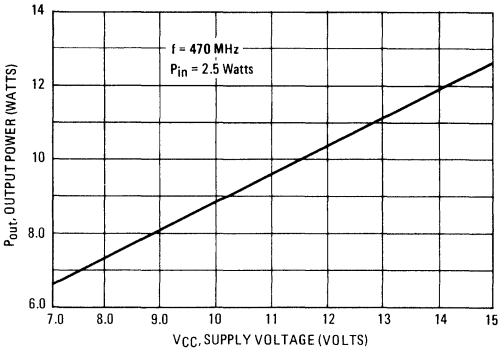


FIGURE 15 – OUTPUT POWER versus INPUT POWER

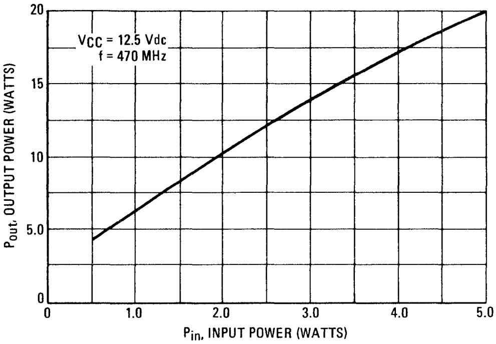


FIGURE 16 – OUTPUT POWER versus FREQUENCY

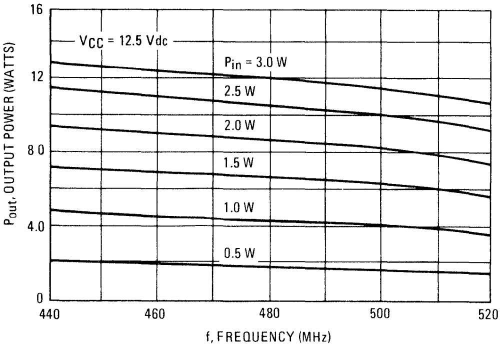


FIGURE 17 – OUTPUT POWER versus INPUT POWER

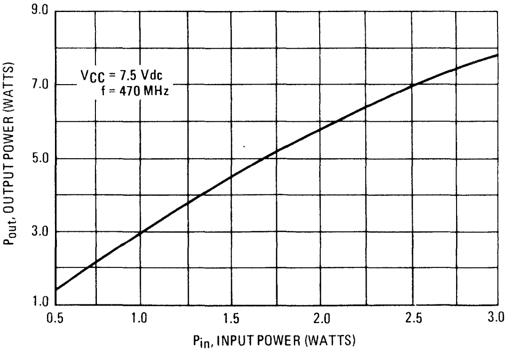
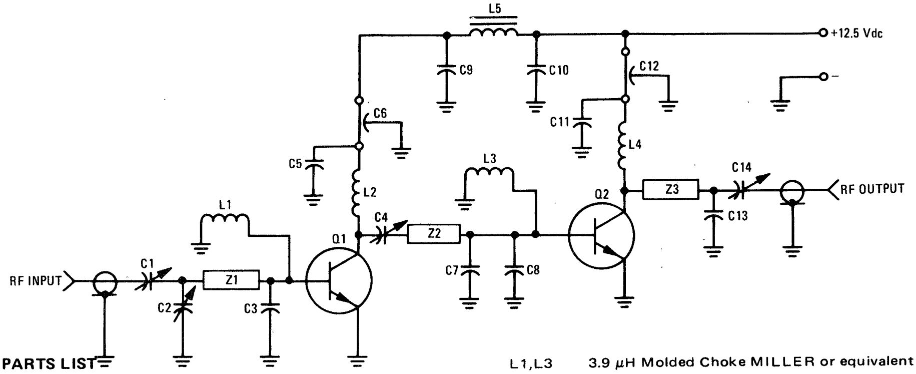


FIGURE 18



PARTS LIST

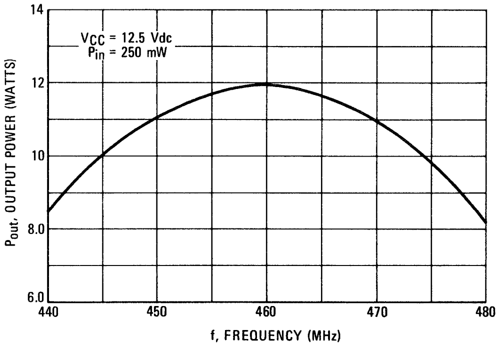
C1,C2,C4,C13,C14	0.9-7.0 pF ARCO 400 or equivalent
C3,C7,C8	25 pF UNELCO or equivalent
C5,C11	0.1 μF Ceramic 35 V
C6,C12	680 pF ALLEN BRADLEY Feedthru
C9,C10	1.0 μF, 35 V Tantalum
L1,L3	3.9 μH Molded Choke MILLER or equivalent
L2,L4	5 Turns #18 AWG Enameled 0.2" I.D.
L5	FERROXCUBE Ferrite Choke VK200 20/4B
Z1,Z2,Z3	Microstrip Lines (See Template Below)
Q1	2N5944
Q2	2N5946

10 W AMPLIFIER PERFORMANCE

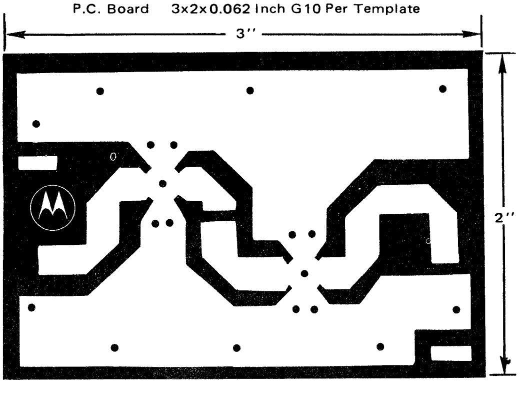
V_{CC} = 12.5 Vdc

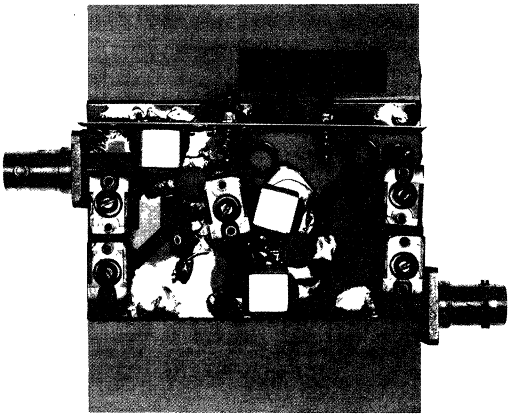
Frequency MHz	P_{in} mW	P_{out} W	I_C Amp
440	250	8.5	1.5
450	250	11	1.6
460	250	12	1.6
470	250	10.9	1.5
480	250	8.2	1.2

FIGURE 19 – OUTPUT POWER versus FREQUENCY



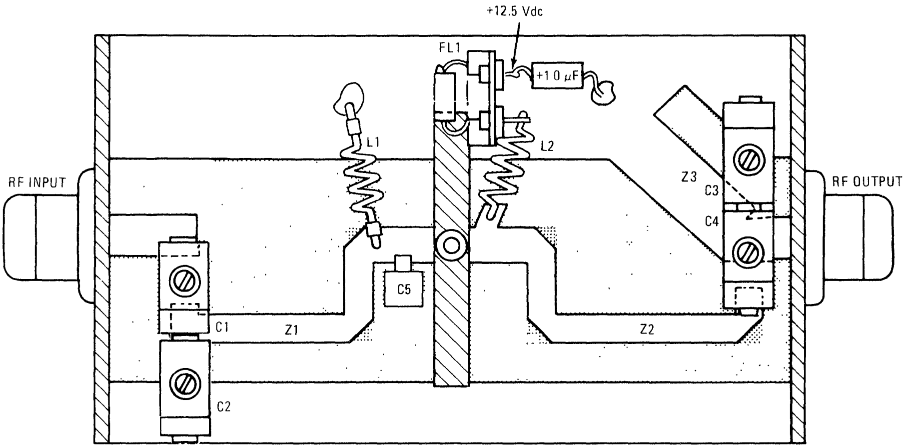
P.C. Board 3x2x0.062 Inch G10 Per Template





470 MHz TEST CIRCUIT

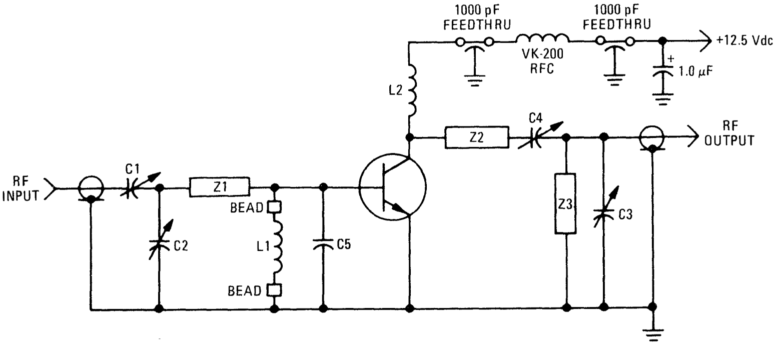
FIGURE 20



C1,2	1.0-25 pF ARCO 421 OR EQUIVALENT
C3,4	1 0-25 pF ARCO 421 OR EQUIVALENT
L1,2	7 TURNS #22 AWG, 0.2" I.D. FERRITE BEADS FERROXCUBE 56-590-65-3B AS SHOWN ON L1
FL1	DC SUPPLY FILTER 2-1000 pF FT CAPACITOR 1-1.0 μF, 35 V CAPACITOR 1-CHOKE FERROXCUBE VK 200-20-4B

CONNECTORS ARE TYPE "N"
BOARD IS GLASS TEFLON
3" x 5" x 0.060"
MOUNTING PLATE IS 3" x 5" x 0.75"

FIGURE 21



2N5947 (SILICON)

The RF Line

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed specifically for broadband applications requiring low cross-modulation distortion and low noise figure. Characterized for use in CATV applications. The 2N5947 was formerly the MM8012.

- Low Cross Modulation Distortion –
  XM = -57 dB (Max) @ +50 dBmV Output
- Low Noise Figure – @ f = 200 MHz
  NF (Narrowband) = 3.8 dB (Typ)
  NF (Broadband) = 8.5 dB (Max)
- High Broadband Power Gain –
  G_{pe} = 10 dB (Min) @ f = 250 MHz

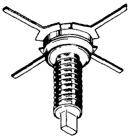
***MAXIMUM RATINGS**

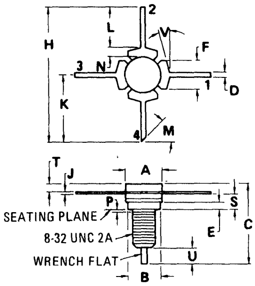
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	3.5	Vdc
Collector Current – Continuous	I_C	400	mAdc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	5.0 28.6	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	-65 to +200	^oC

*Indicates JEDEC Registered Data.

HIGH FREQUENCY TRANSISTOR

NPN SILICON





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.25	6.45	0.246	0.254
C	15.49	16.51	0.610	0.650
D	0.64	0.89	0.025	0.035
E	1.40	1.65	0.055	0.065
F	5.59	5.84	0.220	0.230
H	26.67	27.18	1.050	1.070
J	0.10	0.15	0.004	0.006
K	13.34	13.59	0.525	0.535
L	8.26	8.51	0.325	0.335
M	40^0	50^0	40^0	50^0
N	1.40	1.65	0.055	0.065
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.65	0.055	0.065
U	2.92	3.68	0.115	0.145
V	10^0	20^0	10^0	20^0

CASE 144D-04

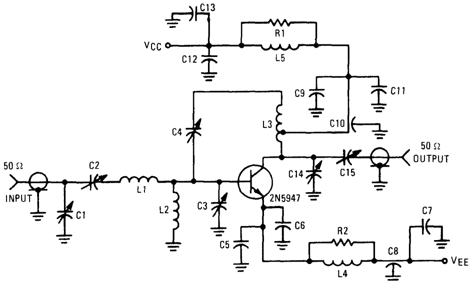
*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	BV_{CEO}	30	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.5	–	–	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, I_B = 0)	I_{CEO}	–	–	100	μAdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 3.5 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 75 mAdc, V_{CE} = 20 Vdc)	h_{FE}	25	–	250	–
Collector-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc)	$V_{CE(sat)}$	–	0.2	0.35	Vdc
Base-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc)	$V_{BE(sat)}$	–	1.0	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (Figure 3) (I_C = 75 mAdc, V_{CE} = 20 Vdc, f = 200 MHz)	f_T	1100	1500	–	MHz
Collector-Base Capacitance (Figure 4) (V_{CB} = 30 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	–	1.5	4.0	pF
Emitter-Base Capacitance (Figure 4) (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	8.2	12	pF
Small-Signal Current Gain (I_C = 75 mAdc, V_{CE} = 20 Vdc, f = 1.0 kHz)	h_{fe}	25	–	300	–
Collector-Base Time Constant (I_E = 75 mAdc, V_{CB} = 20 Vdc, f = 31.8 MHz)	$r_b'C_c$	2.0	–	20	ps
Noise Figure (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 200 MHz) (Figure 1) (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 200 MHz) (1) (Figure 2, 9) (I_C = 75 mAdc, V_{CE} = 20 Vdc, f = 200 MHz) (1) (Figure 2, 9)	NF	 – – –	 3.8 7.2 7.8	 – 8.5 –	dB
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Figure 2) (I_C = 75 mAdc, V_{CE} = 20 Vdc, f = 250 MHz)	G_{pe}	10	11	–	dB
Intermodulation Distortion (Figure 2, 10) (I_C = 75 mAdc, V_{CE} = 20 Vdc, V_{out} = +50 dBmv)	IM	–	-55	-50	dB
Cross Modulation Distortion (Figure 2, 11) (I_C = 75 mAdc, V_{CE} = 20 Vdc, V_{out} = +50 dBmV)	XM	–	-60	-57	dB

*Indicates JEDEC Registered Data.

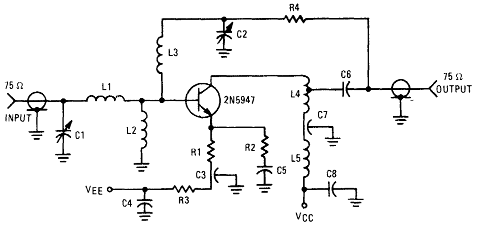
(1) Includes noise figure of post-amplifier and matching pad.

FIGURE 1 – NARROWBAND TEST CIRCUIT



C1, C2, C3	1.0–20 pF		
C4, C14, C15	1.0–10 pF	L2	1-1/2 Turns AWG #18, 1/4" I.D., 3/16" Long
C5, C8, C9	470 pF		
C6, C10, C11	0.001 μF	L3	9-3/4 Turns AWG #18, 3/16" I.D., 1" Long
C7, C13	0.01 μF		
C12	0.1 μF		Tapped 1 3/4 Turns from Collector End
L1	3 Turns AWG #18, 1/4" I.D., 5/16" Long	L4, L5	0.47 μH Molded Choke
		R1, R2	10 Ohms

FIGURE 2 – BROADBAND TEST CIRCUIT



C1, C2	0.5–6.0 pF	L4	#30 AWG Trifilar Wound 1 9 9 Stackpole 57-0985, #11 Toroid
C3, C7	1500 pF Underwood		
C4, C5, C8	0.01 μF		
C6	470 pF	L5	Ferrite Choke, 3 Turns #30 on Stackpole 57-0156 Bead
L1	3 Turns #20 AWG, 5/32" I.D.	R1	20 Ohms
L2	0.84 μH, Ohmite Z235	R2	68 Ohms
L3	5 Turns #26 AWG, 5/32" I.D.	R3	150 Ohms
		R4	360 Ohms

FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

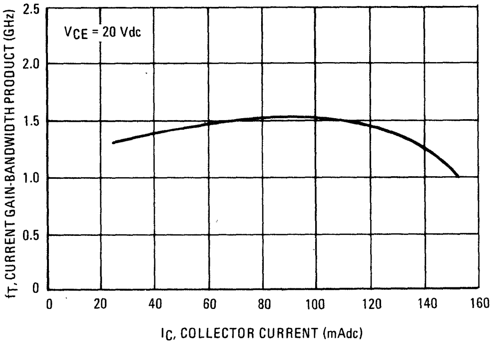


FIGURE 4 – CAPACITANCES

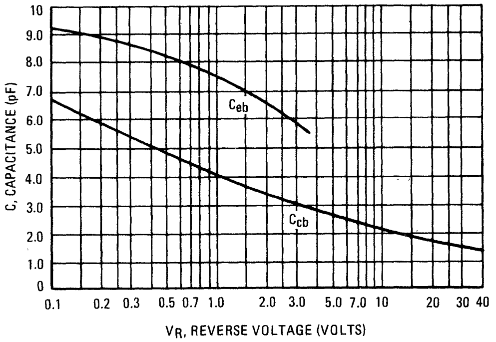


FIGURE 5 – COLLECTOR-EMITTER SATURATION VOLTAGE

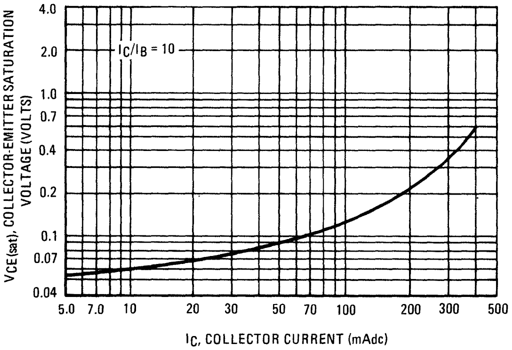


FIGURE 6 – BASE-EMITTER SATURATION VOLTAGE

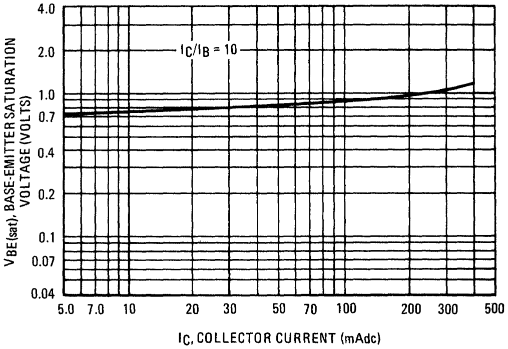


FIGURE 7 – NARROWBAND NOISE FIGURE versus CURRENT

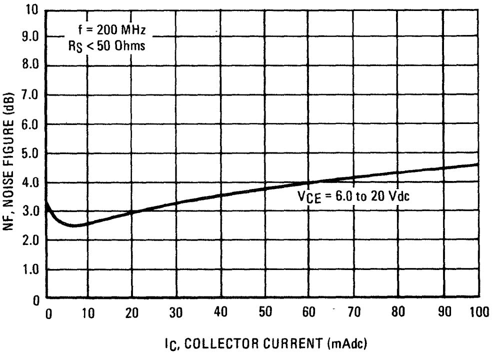


FIGURE 8 – BROADBAND NOISE FIGURE versus CURRENT

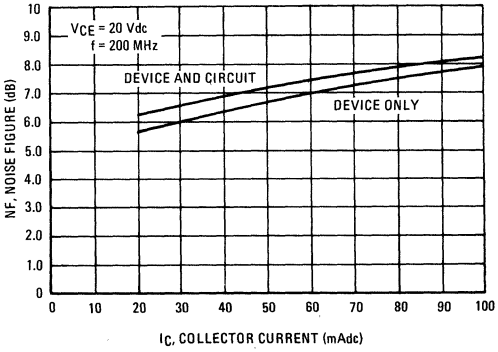
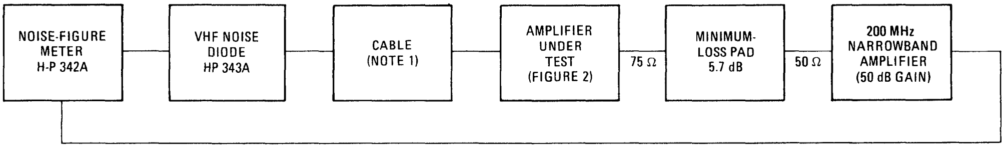


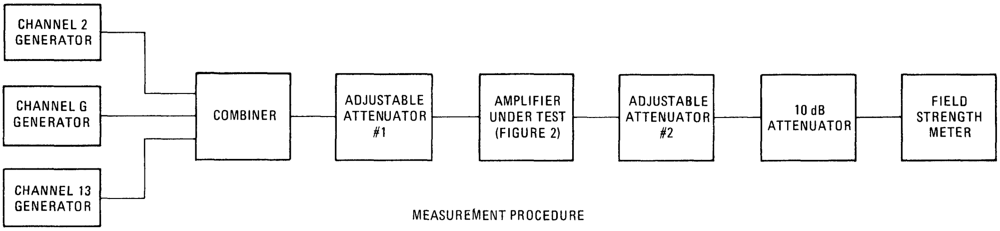
FIGURE 9 – NOISE FIGURE TEST SETUP



NOTE 1. RG-59 CABLE WITH ORIGINAL CENTER CONDUCTOR REPLACED WITH #30 WIRE. OVERALL LENGTH, INCLUDING BNC CONNECTORS, IS A QUARTER-WAVELENGTH AT 200 MHz (APPROX. 11 INCHES). USED TO MATCH IMPEDANCE OF NOISE DIODE TO AMPLIFIER UNDER TEST.

THE NOISE FIGURE OF THE POST-AMPLIFIERS AND MINIMUM LOSS PAD IS 8.4 dB.

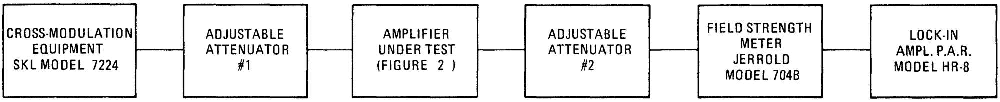
FIGURE 10 – INTERMODULATION DISTORTION TEST SETUP



MEASUREMENT PROCEDURE

1. ADJUST CHANNEL 2 GENERATOR FOR RATED OUTPUT FROM TEST AMPLIFIER (CHANNELS G & 13 OFF).
2. REPEAT FOR CHANNEL G (2 & 13 OFF) AND CHANNEL 13 (2 & G OFF). NOTE FOR REFERENCE THE FIELD STRENGTH METER READING FOR CHANNEL 13 (2 & G OFF).
3. TURN CHANNEL 13 OFF AND DRIVE THE TEST AMPLIFIER WITH CHANNELS 2 & G. MEASURE THE LEVEL OF INTERMODULATION DISTORTION AT CHANNEL 13 RELATIVE TO THE REFERENCE LEVEL IN STEP 2.

FIGURE 11 – CROSS MODULATION DISTORTION TEST SETUP



MEASUREMENT PROCEDURE

1. ADJUST THE CROSSMODULATION EQUIPMENT FOR +50 dBmV OUTPUT FROM EACH CHANNEL.
2. ADJUST ATTENUATOR #1 FOR THE DESIRED OUTPUT LEVEL FROM THE TEST AMPLIFIER. ADJUST ATTENUATOR #2 TO MAINTAIN THE FIELD STRENGTH METER INPUT AT +10 dBmV.
3. WITH THE FIELD STRENGTH METER SELECT CHANNEL 13. USING THE WAVE ANALYZER MEASURE THE LEVEL OF THE MODULATION ON CHANNEL 13 DUE TO CROSS-MODULATION OF CHANNELS 2-12.

FIGURE 12 – CROSS MODULATION DISTORTION *versus* OUTPUT LEVEL

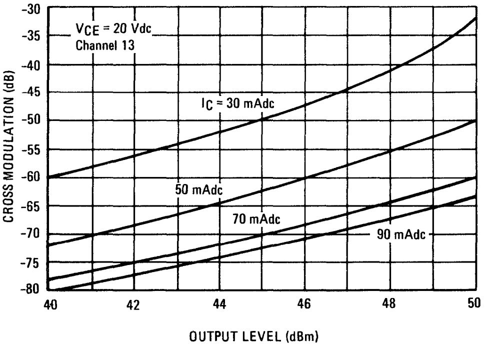
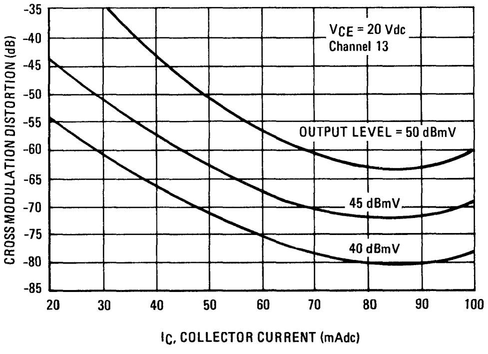


FIGURE 13 – CROSS MODULATION DISTORTION *versus* CURRENT



2N5974 2N5975 2N5976 (SILICON)
MJE5974 MJE5975 MJE5976

PNP SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- DC Current Gain Specified to 5 Amperes
  h_{FE} = 20-120 @ I_C = 2.5 Adc
  = 7.0 (Min) @ I_C = 5.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N5974, MJE5974
  = 60 Vdc (Min) – 2N5975, MJE5975
  = 80 Vdc (Min) – 2N5976, MJE5976
- High Current Gain – Bandwidth Product –
  f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Complements to NPN Transistors 2N5977, 2N5978, 2N5979 and MJE5977, MJE5978, MJE5979
- Choice of Packages – 2N5974 Series – Case 90
  MJE5974 Series – Case 199

5 AMPERE
POWER TRANSISTORS

PNP SILICON

40-60-80 VOLTS
75 WATTS

*MAXIMUM RATINGS

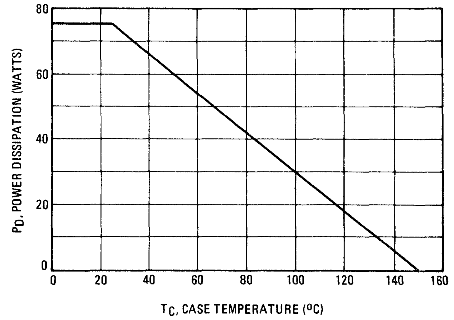
Rating	Symbol	2N5974 MJE5974	2N5975 MJE5975	2N5976 MJE5976	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current - Continuous Peak	I_C	← 5.0 → ← 10 →			Adc
Base Current	I_B	← 2.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 75 → ← 0.60 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS

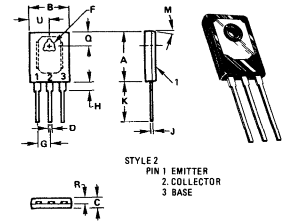
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

*Indicates JEDEC Registered Data for 2N5974 Series.

FIGURE 1 – POWER DERATING



2N5974
2N5975
2N5976



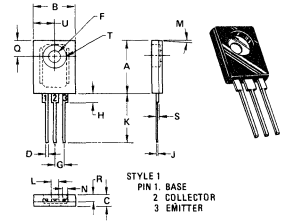
STYLE 2
PIN 1 EMITTER
2. COLLECTOR
3 BASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

NOTE
1 LEADS WITHIN .005" RAD OF TRUE POSITION (TP) AT MMC

CASE 90-05

MJE5974
MJE5975
MJE5976



STYLE 1
PIN 1. BASE
2 COLLECTOR
3 EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0.152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

1 DIM "G" IS TO CENTER LINE OF LEADS

CASE 199-04

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

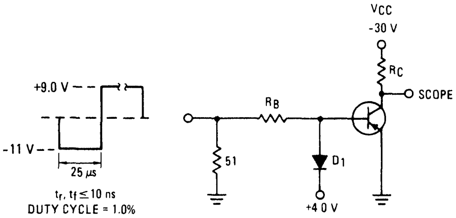
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N5974, MJE5974 2N5975, MJE5975 2N5976, MJE5976	$V_{CEO(sus)}$	40 60 80	– – 	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N5974, MJE5974 2N5975, MJE5975 2N5976, MJE5976	I_{CEO}	– – –	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5974, MJE5974 2N5975, MJE5975 2N5976, MJE5976 2N5974, MJE5974 2N5975, MJE5975 2N5976, MJE5976	I_{CEX}	– – – – – –	100 100 100 1.0 1.0 1.0	μAdc mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc) (I_C = 2.5 Adc, V_{CE} = 2.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	40 20 7.0	– 120 –	–
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 250 mAdc (I_C = 5.0 Adc, I_B = 750 mAdc		$V_{CE(sat)}$	– –	0.6 1.7	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 750 mAdc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.4	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	300	pF
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data for 2N5974 Series.

(1) Pulse Test: Pulse Width ≲ 300 μs, Duty Cycle ≲ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FIGURE 3 – TURN-ON TIME

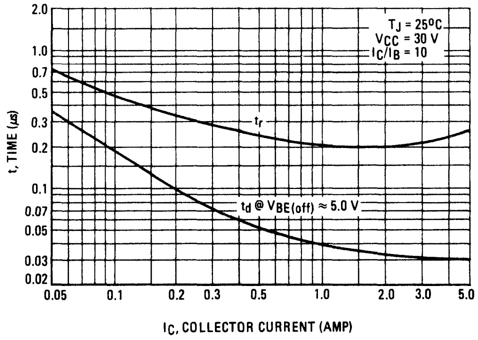


FIGURE 4 – THERMAL RESPONSE

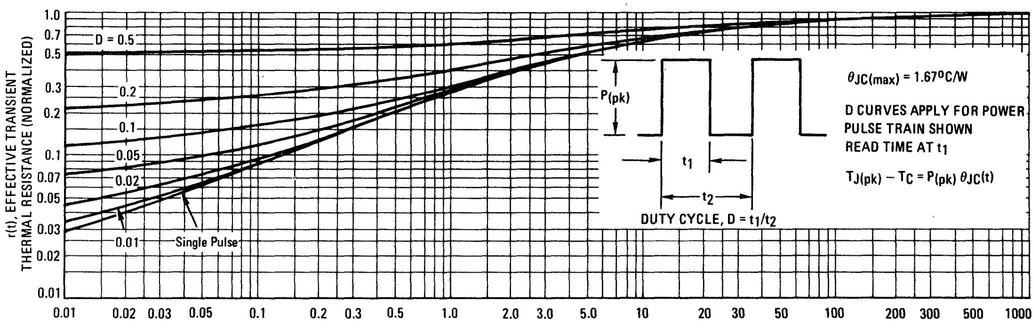
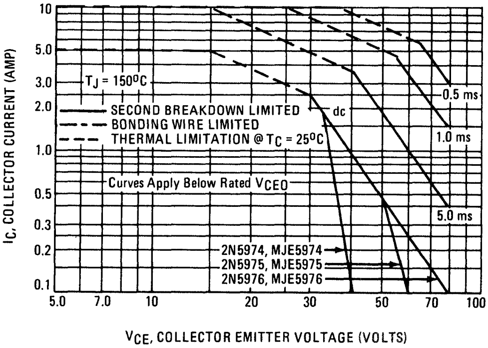


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

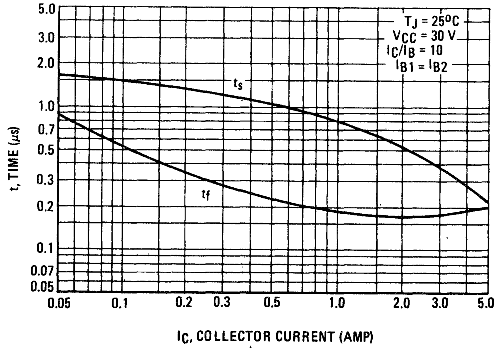


FIGURE 7 – CAPACITANCE

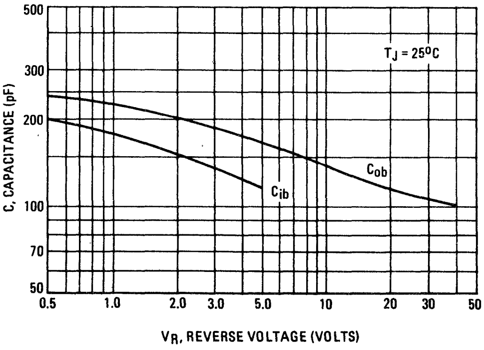


FIGURE 8 – DC CURRENT GAIN

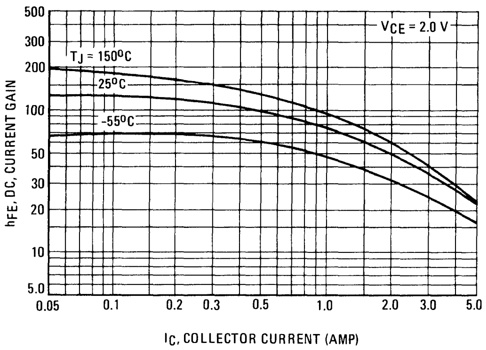


FIGURE 9 – COLLECTOR SATURATION REGION

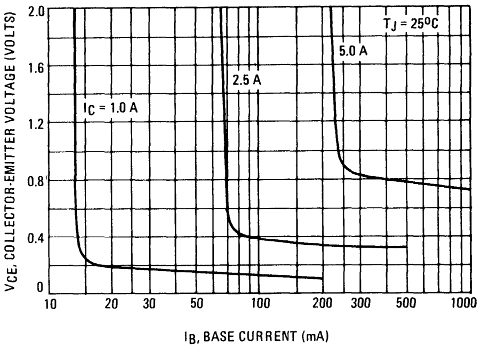


FIGURE 10 – "ON" VOLTAGES

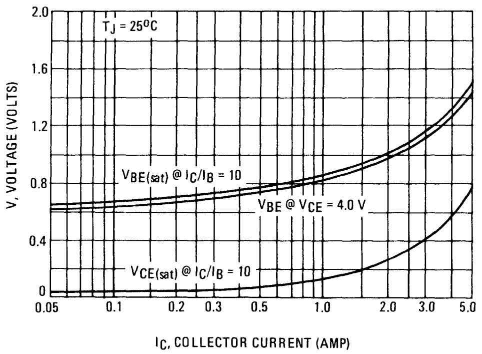


FIGURE 11 – TEMPERATURE COEFFICIENTS

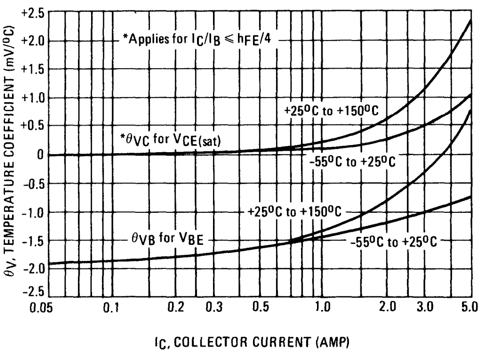


FIGURE 12 – COLLECTOR CUT-OFF REGION

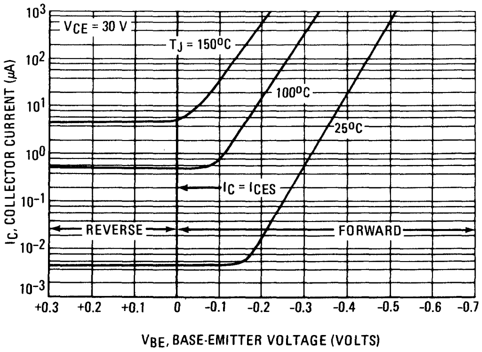
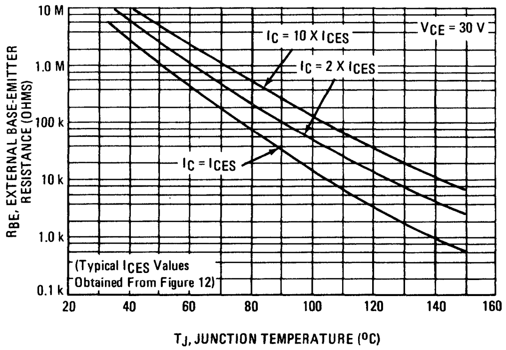


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N5977 2N5978 2N5979 (SILICON)
MJE5977 MJE5978 MJE5979

NPN SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- DC Current Gain Specified to 5 Amperes
  h_{FE} = 20-120 @ I_C = 2.5 Adc
  = 7.0 (Min) @ I_C = 5.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N5977, MJE5977
  = 60 Vdc (Min) – 2N5978, MJE5978
  = 80 Vdc (Min) – 2N5979, MJE5979
- High Current Gain — Bandwidth Product
  f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Complement to PNP Transistors —
  2N5974, 2N5975, 2N5976 and MJE5974, MJE5975, MJE5976
- Choice of Packages — 2N5977 Series — Case 90
  MJE5977 Series — Case 199

5 AMPERE
POWER TRANSISTORS

NPN SILICON

40-60-80 VOLTS
75 WATTS

*MAXIMUM RATINGS

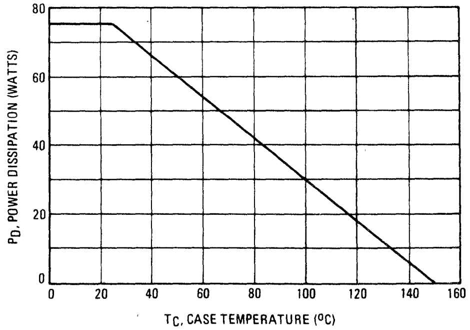
Rating	Symbol	2N5977 MJE5977	2N5978 MJE5978	2N5979 MJE5979	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current - Continuous Peak	I_C	← 5.0 → ← 10 →			Adc
Base Current	I_B	← 2.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 75 → ← 0.60 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS

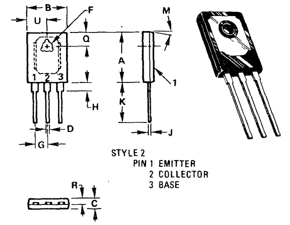
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

*Indicates JEDEC Registered Data for 2N5977 Series.

FIGURE 1 — POWER DERATING



2N5977
2N5978
2N5979



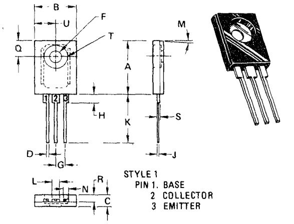
STYLE 2
PIN 1 EMITTER
2 COLLECTOR
3 BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

NOTE
1 LEADS WITHIN .005" RAD OF TRUE POSITION (TP) AT MMC

CASE 90-05

MJE5977
MJE5978
MJE5979



STYLE 1
PIN 1. BASE
2 COLLECTOR
3 EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0.152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

1 DIM "G" IS TO CENTER LINE OF LEADS

CASE 199-04

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

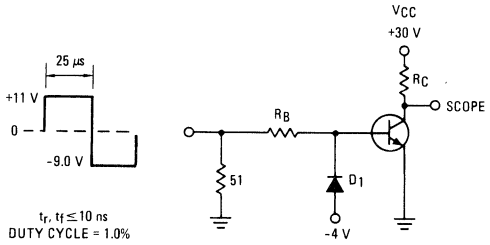
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N5977, MJE5977		40	–	
	2N5978, MJE5978		60	–	
	2N5979, MJE5979		80		
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N5977, MJE5977		–	1.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N5978, MJE5978		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5979, MJE5979		–	1.0	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5977, MJE5977		–	100	µAdc
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5978, MJE5978		–	100	
(V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5979, MJE5979		–	100	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5977, MJE5977		–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5978, MJE5978		–	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5979, MJE5979		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)			7.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.5 Adc, I_B = 250 mAdc)			–	0.6	
(I_C = 5.0 Adc, I_B = 750 mAdc)			–	1.7	
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 750 mAdc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.4	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	200	pF
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data for 2N5977 Series.

(1) Pulse Test: Pulse Width $\leq$ 300 µs, Duty Cycle $\leq$ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE IB ≈100 mA
MSD6100 USED BELOW IB ≈100 mA

FIGURE 3 – TURN-ON TIME

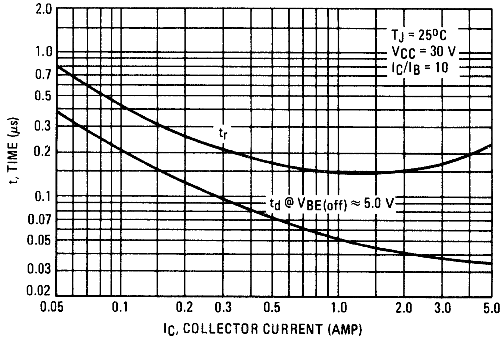


FIGURE 4 – THERMAL RESPONSE

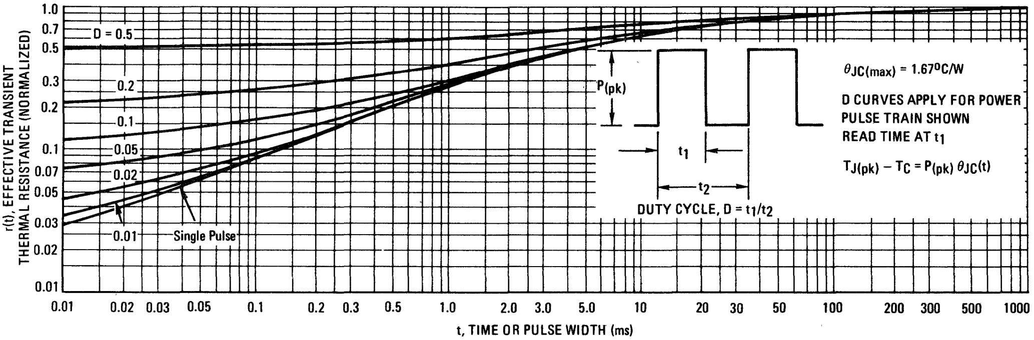
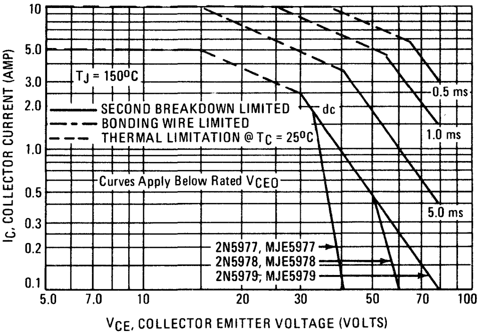


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

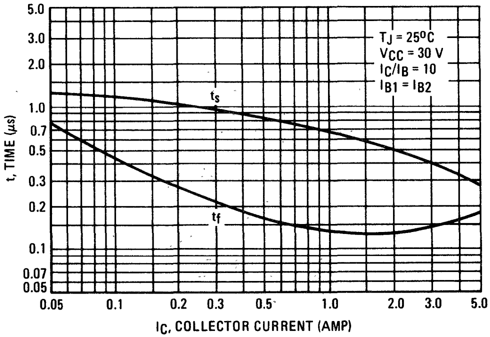


FIGURE 7 – CAPACITANCE

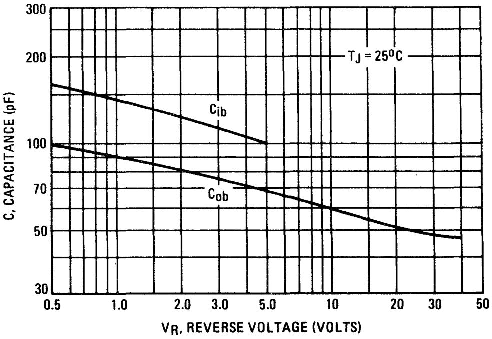


FIGURE 8 – DC CURRENT GAIN

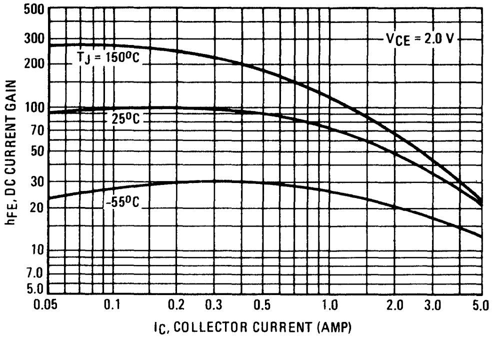


FIGURE 9 – COLLECTOR SATURATION REGION

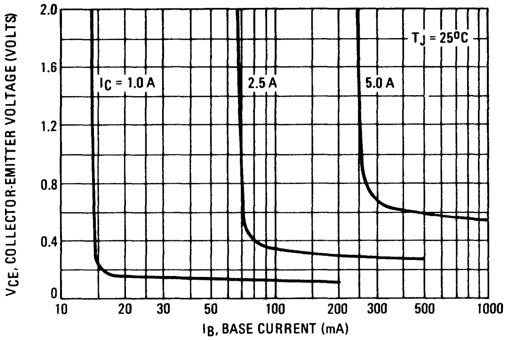


FIGURE 10 – "ON" VOLTAGES

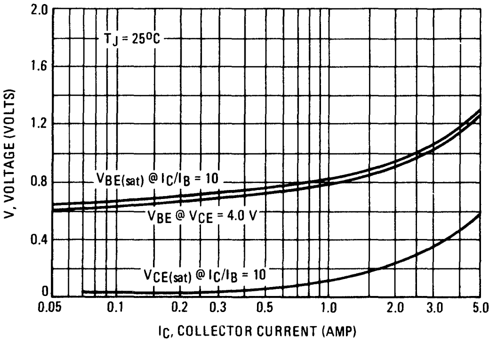


FIGURE 11 – TEMPERATURE COEFFICIENTS

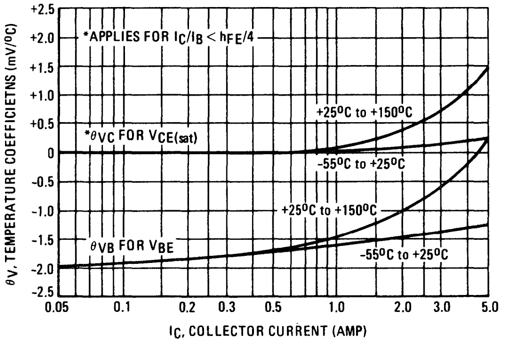


FIGURE 12 – COLLECTOR CUT-OFF REGION

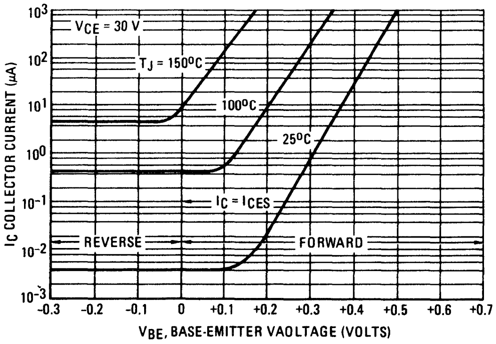
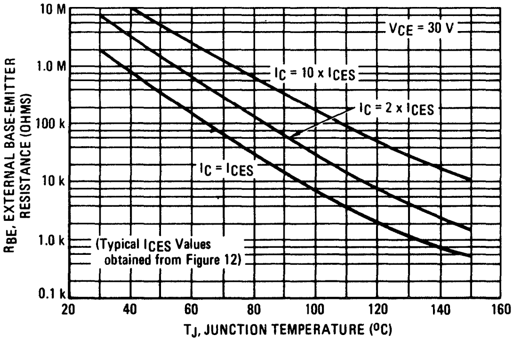


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N5980 2N5981 2N5982 (SILICON)
MJE5980 MJE5981 MJE5982

HIGH POWER PNP SILICON TRANSISTORS

. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 8 Amperes –
  h_{FE} = 20-120 @ I_C = 4.0 Adc
  = 7.0 (Min) @ I_C = 8.0 Adc
- Collector-Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N5980, MJE5980
  = 60 Vdc (Min) – 2N5981, MJE5981
  = 80 Vdc (Min) – 2N5982, MJE5982
- High Current Gain – Bandwidth Product –
  f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Complements to NPN Transistors – 2N5983, 2N5984, 2N5985 and MJE5983, MJE5984, MJE5985
- Choice of Packages – 2N5980 Series – Case 90
  MJE5980 Series – Case 199

8 AMPERE
POWER TRANSISTORS

PNP SILICON

40-60-80 VOLTS
90 WATTS

*MAXIMUM RATINGS

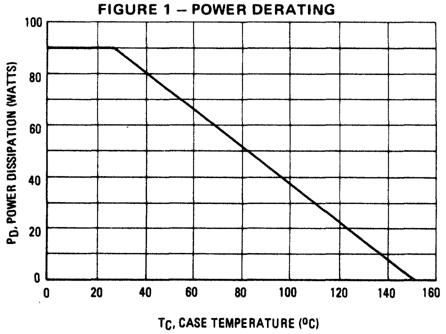
Rating	Symbol	2N5980 MJE5980	2N5981 MJE5981	2N5982 MJE5982	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 8.0 → ← 15 →			Adc
Base Current	I_B	← 3.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 90 → ← 0.72 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS

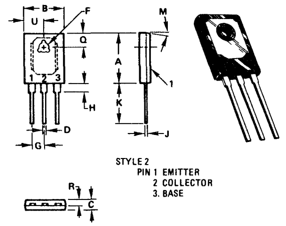
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

*Indicates JEDEC Registered Data for 2N5980 Series.

FIGURE 1 – POWER DERATING



2N5980
2N5981
2N5982



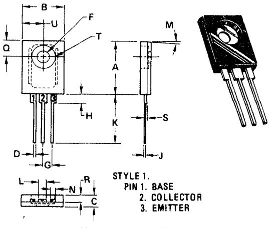
STYLE 2
PIN 1 EMITTER
2 COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16 13	16 38	0 635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0 125	0 135
D	1.09	1.24	0 043	0.049
F	3.51	3.76	0 138	0 148
G	4.22 BSC		0 166 BSC	
H	2.67	2.92	0.105	0 115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0 185	0.195
R	1.91	2.16	0.075	0 085
U	6 22	6 48	0.245	0.255

NOTE
1 LEADS WITHIN .005" RAD OF TRUE POSITION (TP) AT MMC

CASE 90-05

MJE5980
MJE5981
MJE5982



STYLE 1.
PIN 1. BASE
2. COLLECTOR
3. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16 08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0:152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

1. DIM "G" IS TO CENTER LINE OF LEADS

CASE 199-04

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

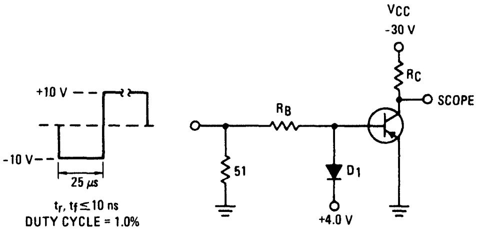
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5980, MJE5980		40	–	
	2N5981, MJE5981		60	–	
	2N5982, MJE5982		80	–	
Collector Cutoff Current		I_{CEO}			mA
(V_{CE} = 20 Vdc, I_B = 0)	2N5980, MJE5980		–	1.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N5981, MJE5981		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5982, MJE5982		–	1.0	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5980, MJE5980		–	100	µAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5981, MJE5981		–	100	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5982, MJE5982		–	100	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5980, MJE5980		–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5981, MJE5981		–	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5982, MJE5982		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)			7.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 400 mAdc)			–	0.6	
(I_C = 8.0 Adc, I_B = 1.2 Adc)			–	1.7	
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 1.2 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.4	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	350	pF
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data for 2N5980 Series.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FIGURE 3 – TURN-ON TIME

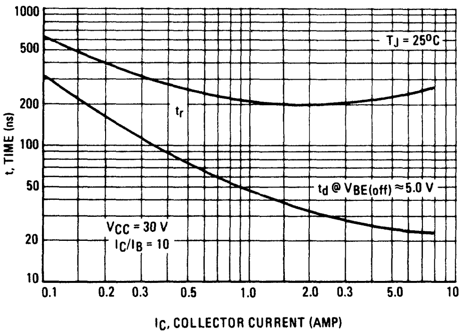


FIGURE 4 – THERMAL RESPONSE

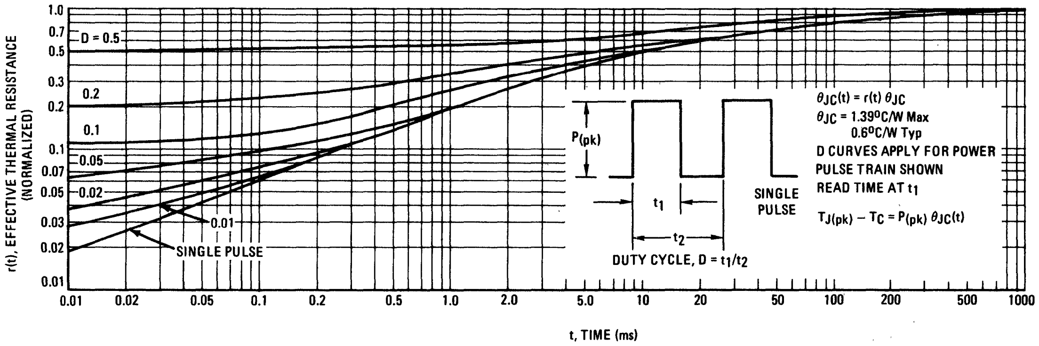
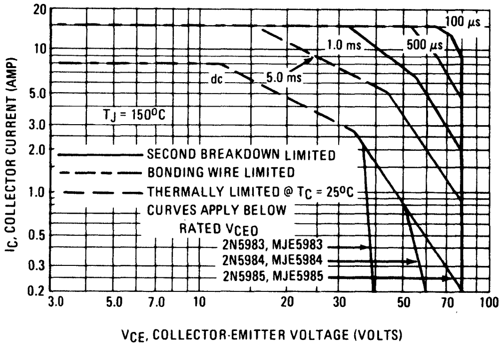


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

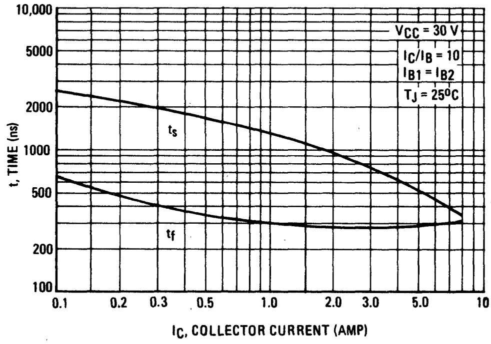


FIGURE 7 – CAPACITANCE

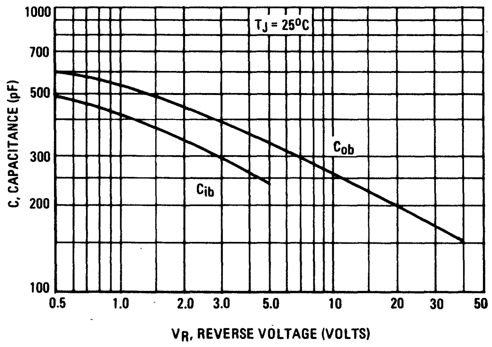


FIGURE 8 – DC CURRENT GAIN

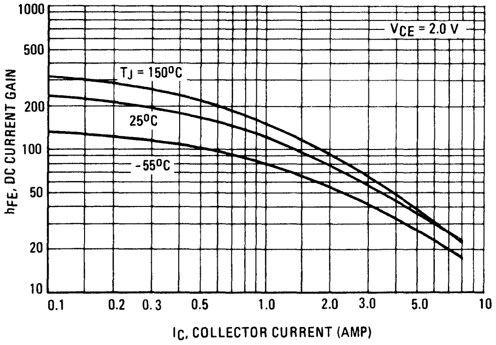


FIGURE 9 – COLLECTOR SATURATION REGION

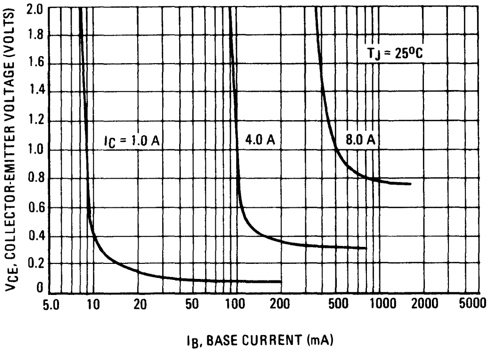


FIGURE 10 – "ON" VOLTAGES

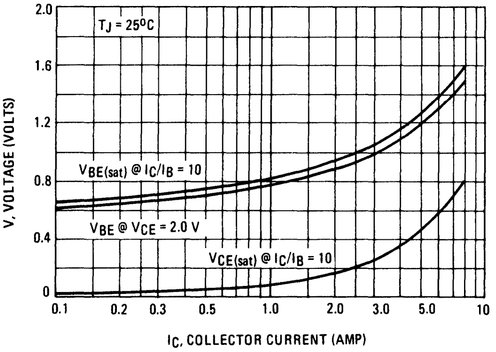


FIGURE 11 – TEMPERATURE COEFFICIENTS

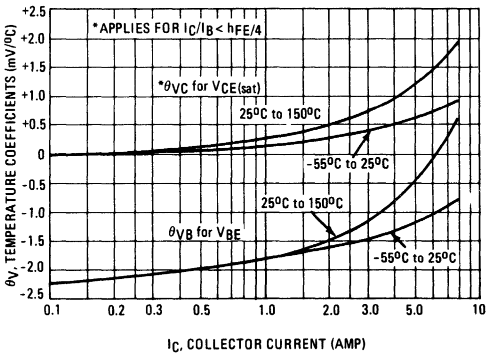


FIGURE 12 – COLLECTOR CUTOFF REGION

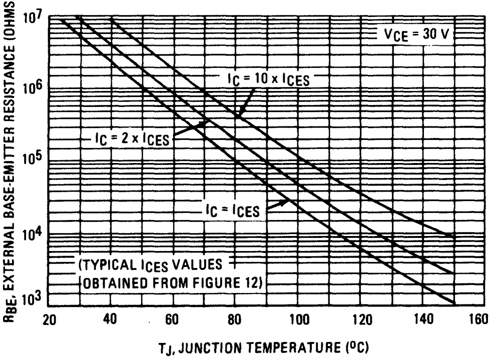
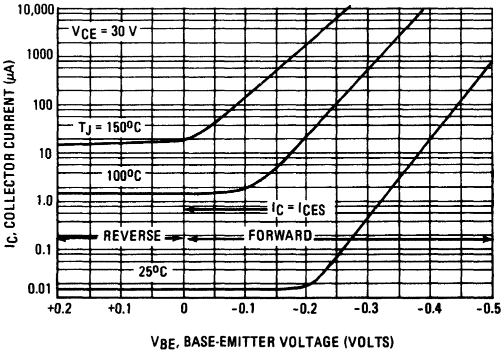


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N5983 2N5984 2N5985 (SILICON)
MJE5983 MJE5984 MJE5985

HIGH POWER NPN SILICON TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- DC Current Gain Specified to 8 Amperes
  h_{FE} = 20-120 @ I_C = 4.0 Adc
  = 7.0 (Min) @ I_C = 8.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc (Min) — 2N5983, MJE5983
  = 60 Vdc (Min) — 2N5984, MJE5984
  = 80 Vdc (Min) — 2N5985, MJE5985
- High Current Gain — Bandwidth Product —
  f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Complements to PNP Transistors —
  2N5980, 2N5981, 2N5982 and MJE5980, MJE5981, MJE5982
- Choice of Packages — 2N5983 Series — Case 90
  MJE5983 Series — Case 199

**8 AMPERE
POWER TRANSISTORS**

NPN SILICON

**40-60-80 VOLTS
90 WATTS**

*MAXIMUM RATINGS

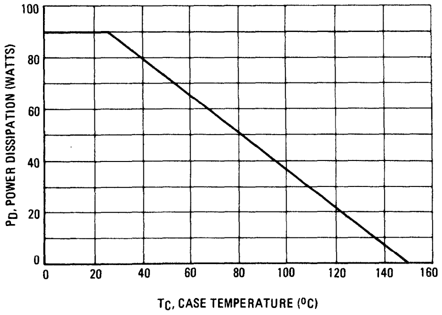
Rating	Symbol	2N5983 MJE5983	2N5984 MJE5984	2N5985 MJE5985	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current - Continuous Peak	I_C	← 8.0 → ← 15 →			Adc
Base Current	I_B	← 3.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 90 → ← 0.72 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS

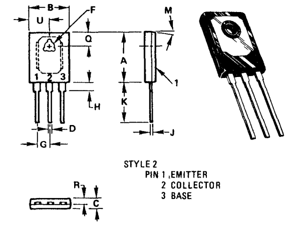
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

*Indicates JEDEC Registered Data for 2N5983 Series.

FIGURE 1 — POWER DERATING



2N5983
2N5984
2N5985



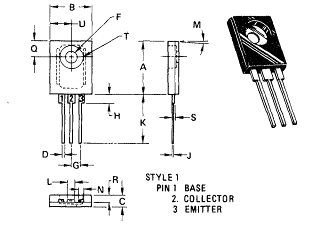
STYLE 2
PIN 1 EMITTER
2 COLLECTOR
3 BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

NOTE
1 LEADS WITHIN .005" RAD OF TRUE POSITION (TP) AT MMC

CASE 90-05

MJE5983
MJE5984
MJE5985



STYLE 1
PIN 1 BASE
2. COLLECTOR
3 EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0.152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

1 DIM "G" IS TO CENTER LINE OF LEADS

CASE 199-04

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

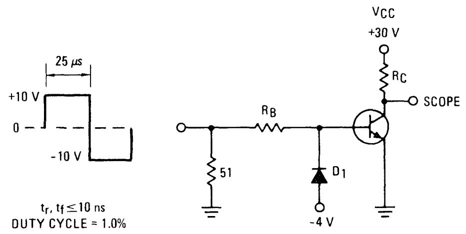
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5983, MJE5983		40	–	
	2N5984, MJE5984		60	–	
	2N5985, MJE5985		80		
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N5983, MJE5983		–	1.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N5984, MJE5984		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5985, MJE5985		–	1.0	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5983, MJE5983		–	100	μAdc
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5984, MJE5984		–	100	
(V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5985, MJE5985		–	100	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5983, MJE5983		–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5984, MJE5984		–	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5985, MJE5985		–	1.0	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)			7.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 400 mAdc)			–	0.6	
(I_C = 8.0 Adc, I_B = 1.2 Adc)			–	1.7	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 8.0 Adc, I_B = 1.2 Adc)			–	2.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			–	1.4	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2)		f_T			MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)			2.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	250	
Small-Signal Current Gain		h_{fe}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)			20	–	

*Indicates JEDEC Registered Data for 2N5983 Series.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

FIGURE 3 – TURN-ON TIME

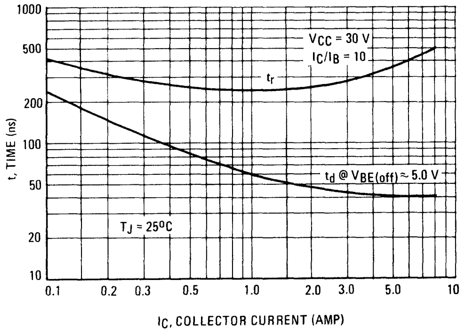


FIGURE 4 – THERMAL RESPONSE

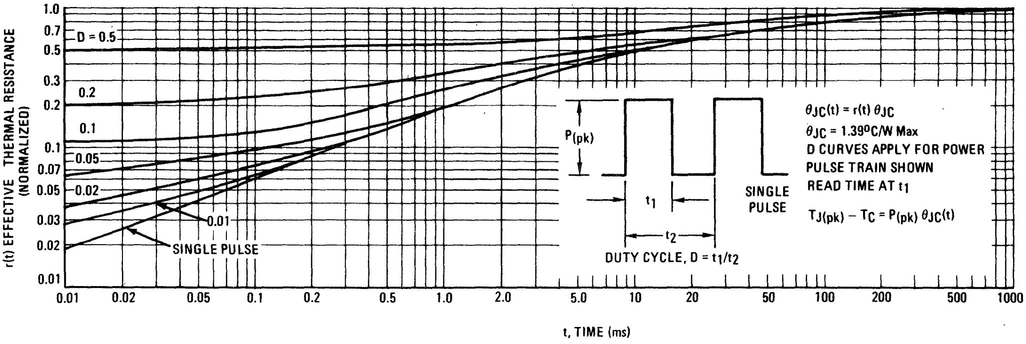
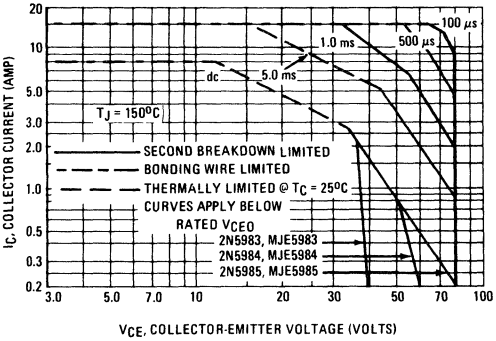


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

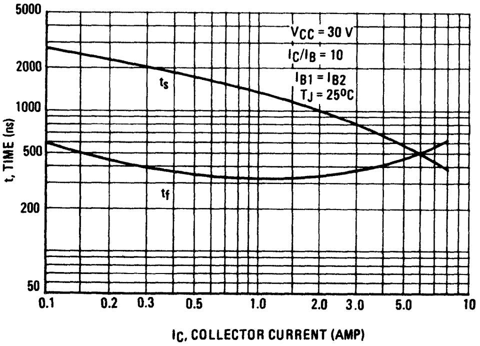


FIGURE 7 – CAPACITANCES

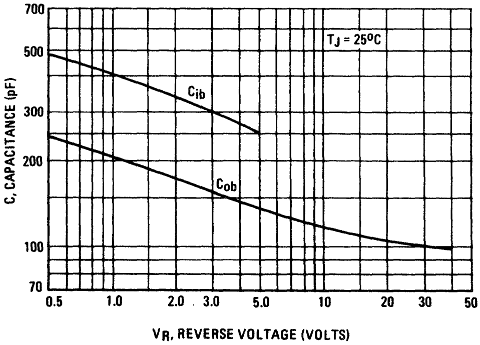


FIGURE 8 — DC CURRENT GAIN

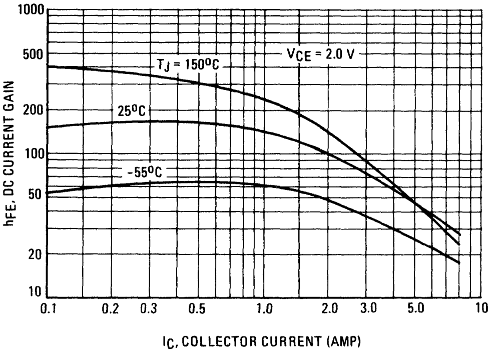


FIGURE 9 — COLLECTOR SATURATION REGION

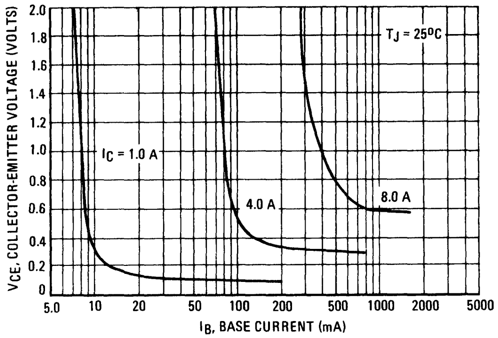


FIGURE 10 — "ON" VOLTAGES

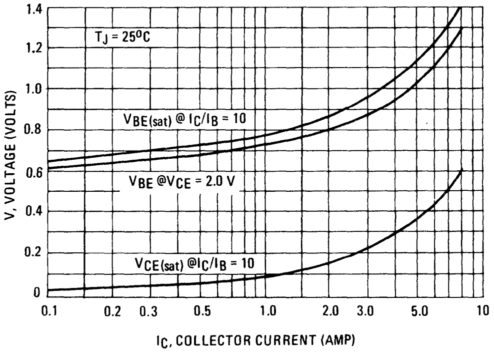


FIGURE 11 — TEMPERATURE COEFFICIENTS

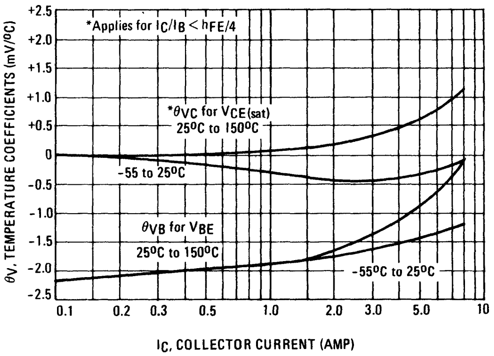


FIGURE 12 — COLLECTOR CUT-OFF REGION

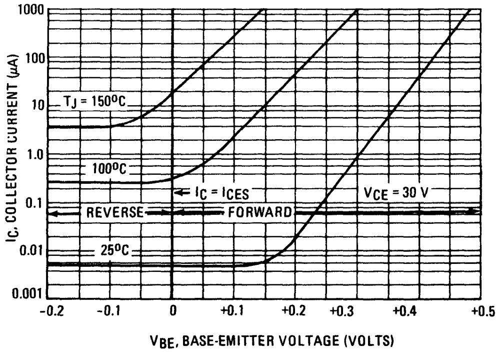
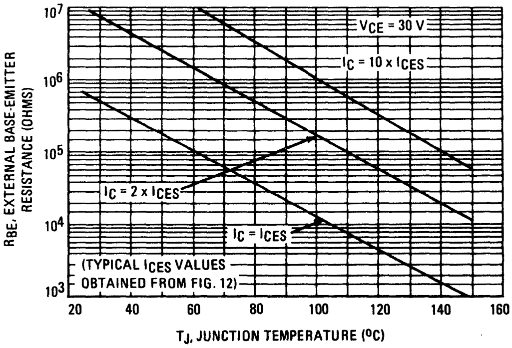


FIGURE 13 — EFFECTS OF BASE-EMITTER RESISTANCE



2N5986 2N5987 2N5988 PNP (SILICON)
2N5989 2N5990 2N5991 NPN

HIGH POWER PLASTIC COMPLEMENTARY SILICON POWER TRANSISTORS

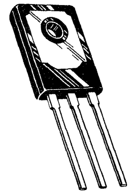
. . . designed for use in general-purpose amplifier and switching circuits.

- Collector-Base Voltage – V_{CBO} = 60 Vdc – 2N5986, 2N5989
  = 80 Vdc – 2N5987, 2N5990
  = 100 Vdc – 2N5988, 2N5991
- Collector-Emitter Voltage – V_{CEO} = 40 Vdc – 2N5986, 2N5989
  = 60 Vdc – 2N5987, 2N5990
  = 80 Vdc – 2N5988, 2N5991
- DC Current Gain –
  h_{FE} = 20-120 @ I_C = 6.0 Adc
  = 7.0 (Min) @ I_C = 12 Adc
- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 6.0 Adc

12 AMPERE

POWER TRANSISTORS
COMPLEMENTARY SILICON

40, 60, 80 VOLTS
100 WATTS



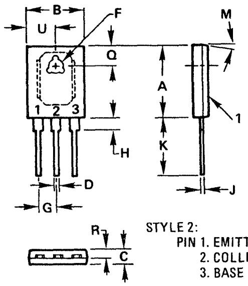
*MAXIMUM RATINGS

Rating	Symbol	2N5986 2N5989	2N5987 2N5990	2N5988 2N5991	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	12 20			Adc
Base Current	I_B	4.0			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.25	°C/W

*Indicates JEDEC Registered Data



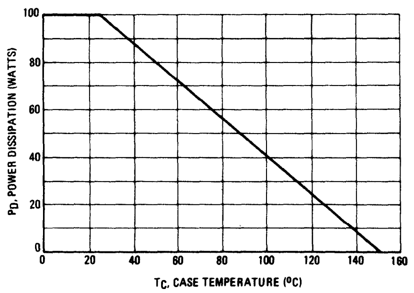
STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51.	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

NOTE:
1. LEADS WITHIN .005" RAD OF TRUE POSITION (TP) AT MMC

CASE 90-05

FIGURE 1 – POWER DERATING



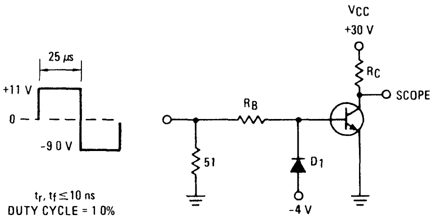
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 0.2 Adc, I_B = 0) 2N5986, 2N5989 2N5987, 2N5990 2N5988, 2N5991	$BV_{CEO(sus)}$	40 60 80	– – –	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) 2N5986, 2N5989 (V_{CE} = 30 Vdc, I_B = 0) 2N5987, 2N5990 (V_{CE} = 40 Vdc, I_B = 0) 2N5988, 2N5991	I_{CEO}	– – –	2.0 2.0 2.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5986, 2N5989 (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5987, 2N5990 (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5988, 2N5991 (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) 2N5986, 2N5989 (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) 2N5987, 2N5990 (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) 2N5988, 2N5991	I_{CEX}	– – – – – –	200 200 200 2.0 2.0 2.0	μAdc mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc) (I_C = 6.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 12 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	40 20 7.0	– 120 –	–
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 0.6 Adc) (I_C = 12 Adc, I_B = 1.8 Adc)	$V_{CE(sat)}$	– –	0.7 1.7	Vdc
Base-Emitter Saturation Voltage (I_C = 12 Adc, I_B = 1.8 Adc)	$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.4	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz) 2N5986 thru 2N5988 2N5989 thru 2N5991	C_{ob}	– –	500 300	pF
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	20	–	–

*Indicates JEDEC Registered Data.

(1) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg.
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

For PNP test circuit reverse diode and voltage polarities.

FIGURE 3 – TURN-ON TIME

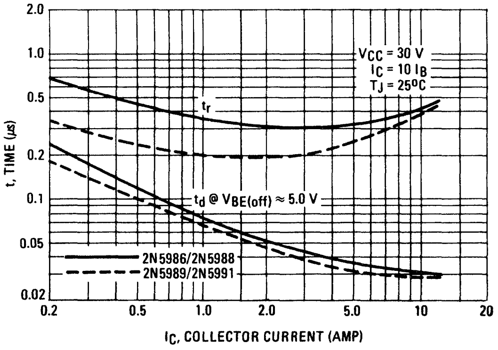


FIGURE 4 – THERMAL RESPONSE

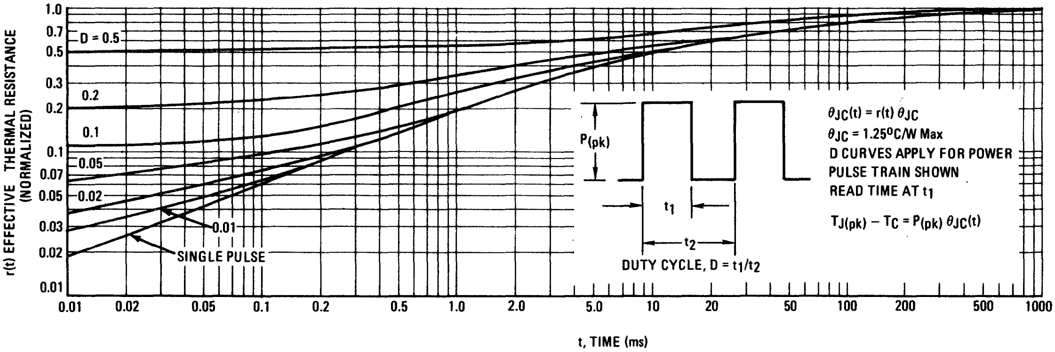
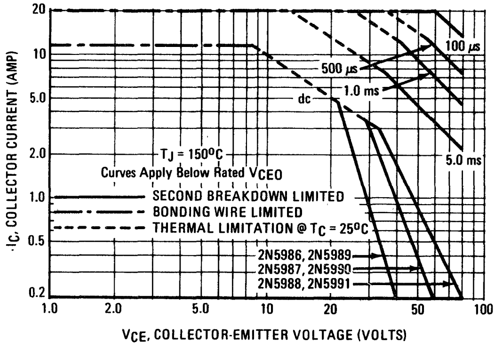


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$ $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

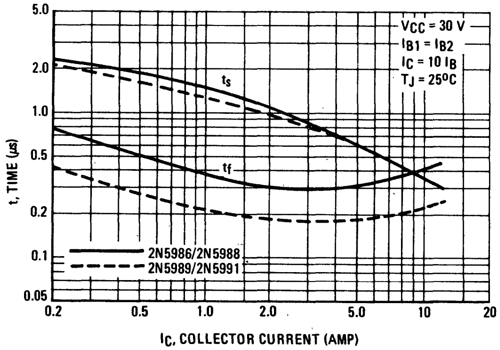
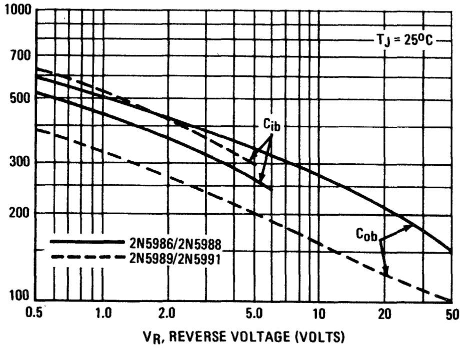


FIGURE 7 – CAPACITANCE



PNP
2N5986 thru 2N5988

NPN
2N5989 thru 2N5991

FIGURE 8 – DC CURRENT GAIN

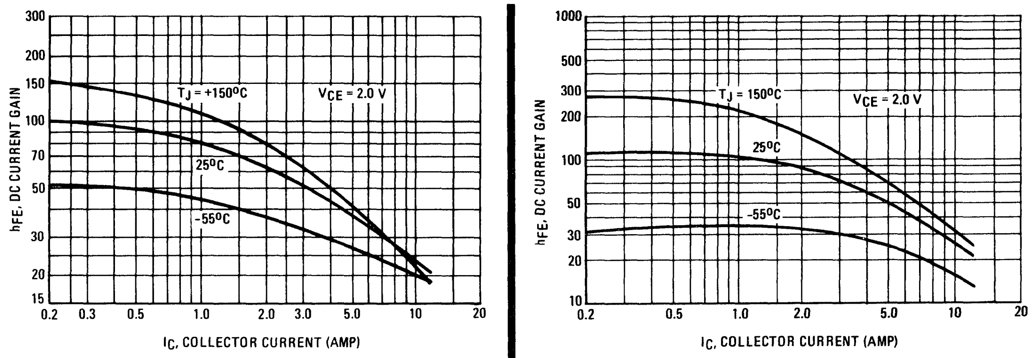


FIGURE 9 – COLLECTOR SATURATION REGION

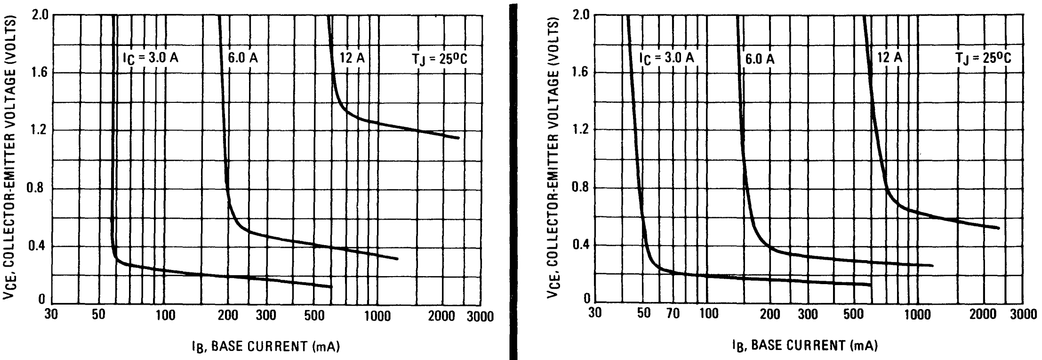
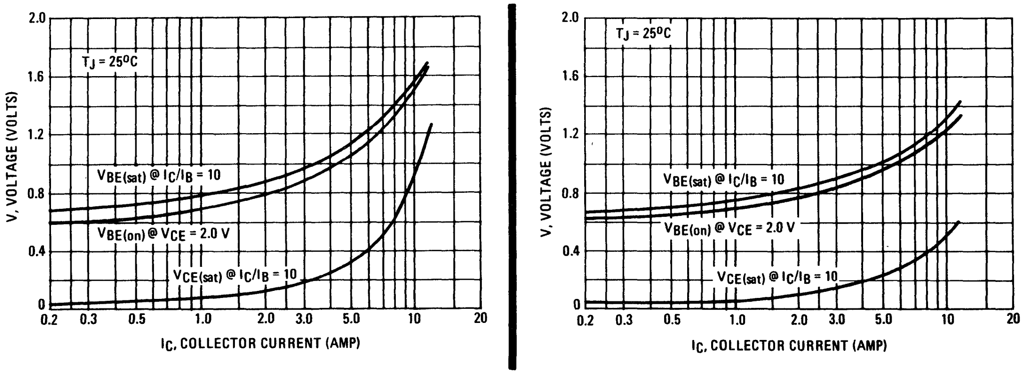


FIGURE 10 – "ON" VOLTAGES



PNP
2N5986 thru 2N5988

NPN
2N5989 thru 2N5991

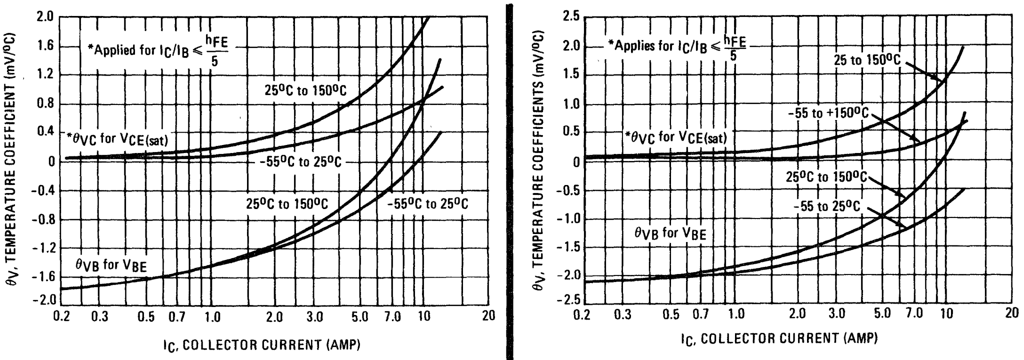


FIGURE 11 – TEMPERATURE COEFFICIENTS

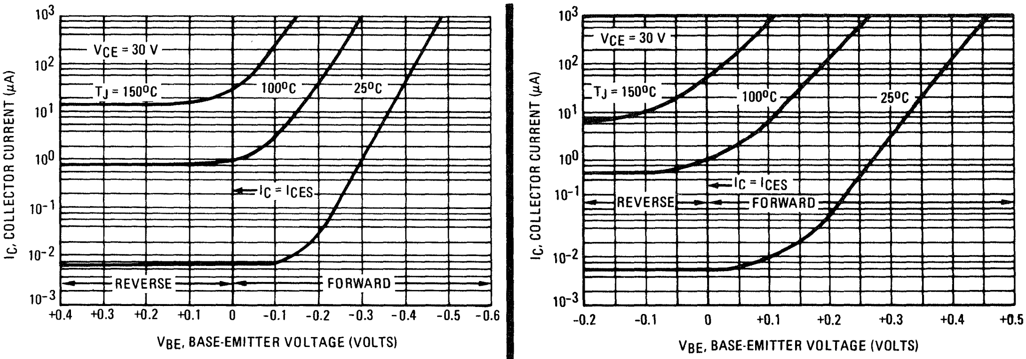


FIGURE 12 – COLLECTOR CUTOFF REGION

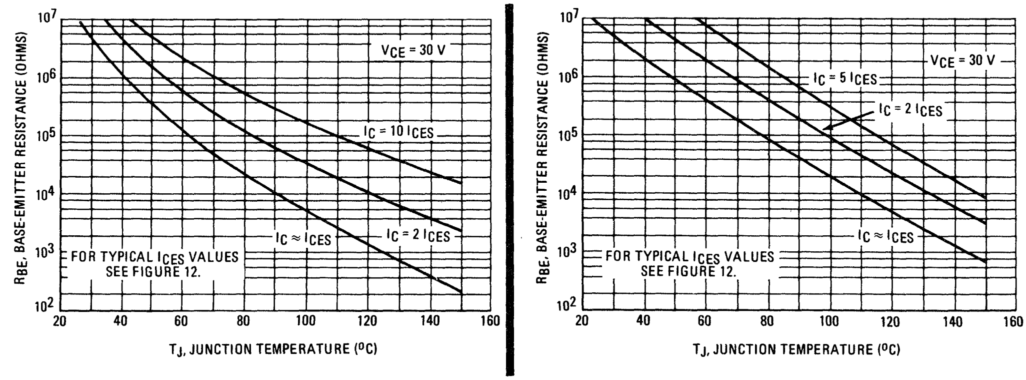
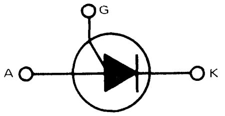


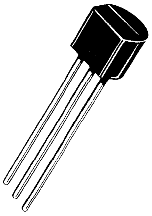
FIGURE 13 – EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE

2N6027 (SILICON)
2N6028



SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

40 VOLTS
375 mW



SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

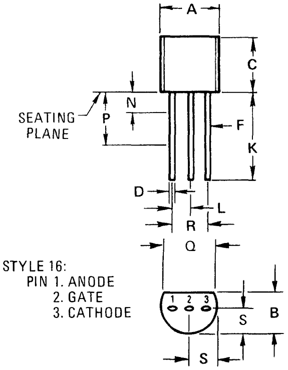
. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable – R_{BB}, η, I_V and I_P.
- Low On-State Voltage – 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 10 nA Maximum
- High Peak Output Voltage – 11 Volts Typical
- Low Offset Voltage – 0.35 Volt Typical (R_G = 10 k ohms)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation(1) Derate Above 25°C	P_F $1/\theta_{JA}$	375 5.0	mW mW/°C
DC Forward Anode Current(2) Derate Above 25°C	I_T	200 2.67	mA mA/°C
*DC Gate Current	I_G	±50	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle *20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
* Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
* Gate to Cathode Reverse Voltage	V_{GKR}	-5.0	Volt
* Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
* Anode to Cathode Voltage	V_{AK}	±40	Volt
Operating Junction Temperature Range	T_J	-50 to +100	°C
* Storage Temperature Range	T_{stg}	-55 to +150	°C

*Indicates JEDEC Registered Data
(1)JEDEC Registered Data is 300 mW, derating at 4.0 mW/°C.
(2)JEDEC Registered Data is 150 mA.



STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

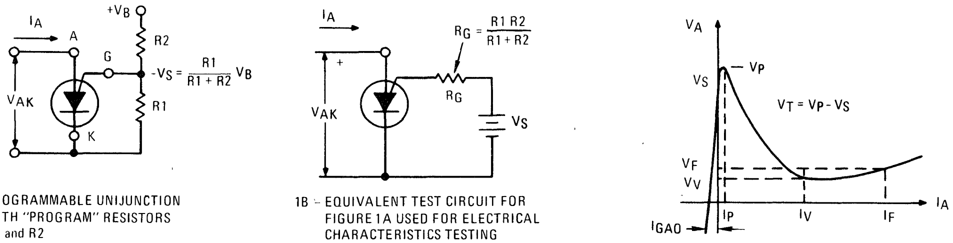
CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
*Peak Current		2,9,11	I_P				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			–	1.25	2.0	
	2N6028			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			–	4.0	5.0	
	2N6028			–	0.70	1.0	
*Offset Voltage		1	V_T				Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			0.2	0.70	1.6	
	2N6028			0.2	0.50	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	(Both Types)			0.2	0.35	0.6	
*Valley Current		1,4,5,	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			–	18	50	
	2N6028			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			70	270	–	
	2N6028			25	270	–	
(V_S = 10 Vdc, R_G = 200 Ohms)	2N6027			1.5	–	–	mA
	2N6028			1.0	–	–	
* Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	10	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	3.0	–	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
*Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0.8	1.5	Volts
* Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

*Indicates JEDEC Registered Data

FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – PROGRAMMABLE UNIJUNCTION WITH "PROGRAM" RESISTORS R1 and R2

1B – EQUIVALENT TEST CIRCUIT FOR FIGURE 1A USED FOR ELECTRICAL CHARACTERISTICS TESTING (ALSO SEE FIGURE 2)

1C – ELECTRICAL CHARACTERISTICS

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

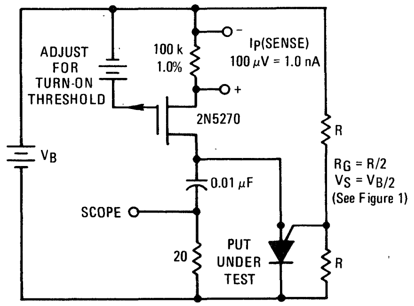
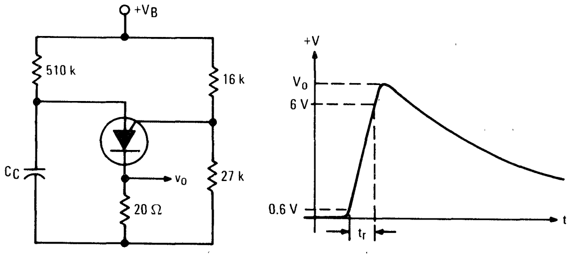


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

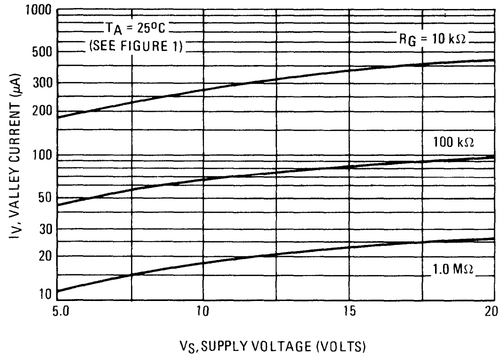


FIGURE 5 – EFFECT OF TEMPERATURE

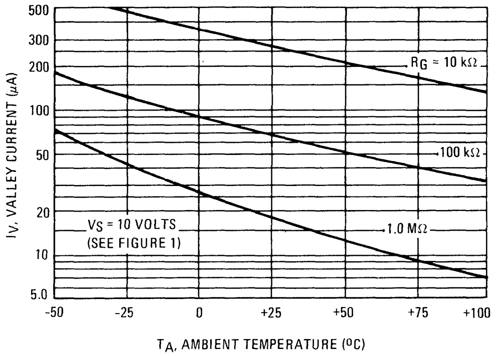


FIGURE 6 – FORWARD VOLTAGE

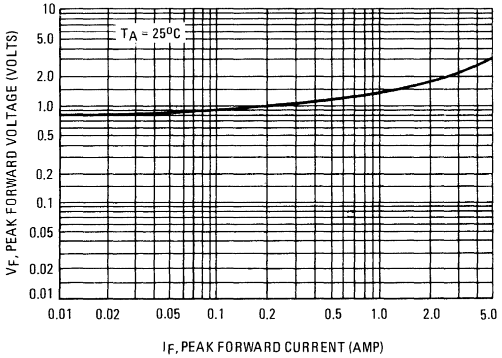


FIGURE 7 – PEAK OUTPUT VOLTAGE

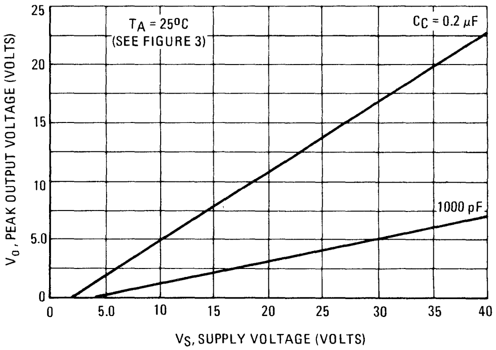
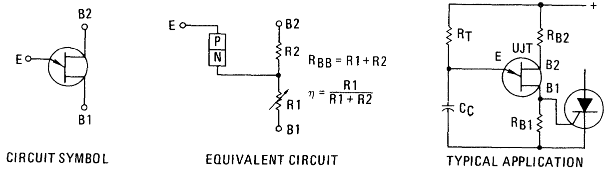


FIGURE 8 – STANDARD UNIJUNCTION COMPARED TO PROGRAMMABLE UNIJUNCTION

STANDARD UNIJUNCTION

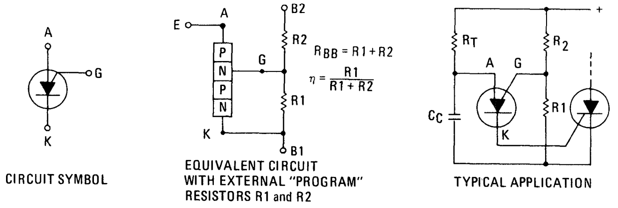


CIRCUIT SYMBOL

EQUIVALENT CIRCUIT

TYPICAL APPLICATION

PROGRAMMABLE UNIJUNCTION



CIRCUIT SYMBOL

EQUIVALENT CIRCUIT
WITH EXTERNAL "PROGRAM"
RESISTORS R1 and R2

TYPICAL APPLICATION

TYPICAL PEAK CURRENT BEHAVIOR

2N6027

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

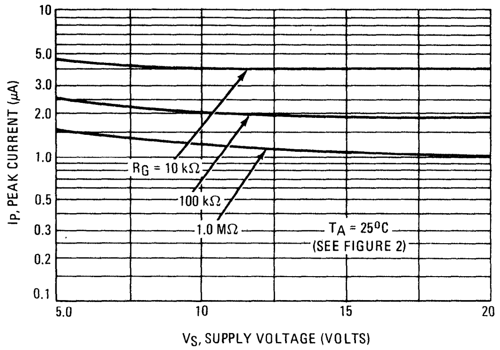
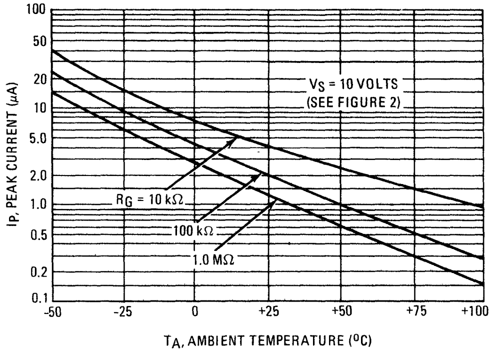


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



2N6028

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

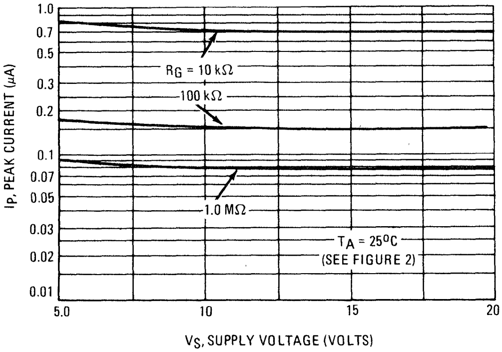
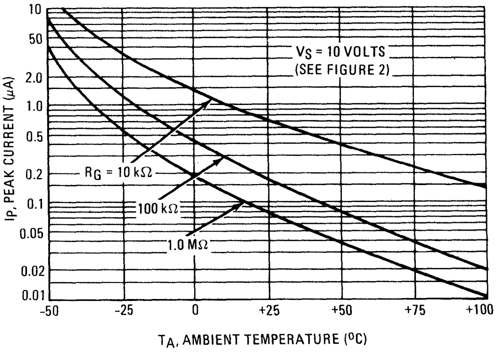


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



2N6029 (SILICON)
2N6030
2N6031

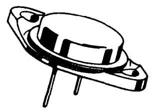
HIGH-VOLTAGE – HIGH POWER PNP TRANSISTORS

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc – 2N6029
  = 120 Vdc – 2N6030
  = 140 Vac – 2N6031
- High DC Current Gain – @ I_C = 8.0 Adc
  h_{FE} = 25 (Min) – 2N6029
  = 20 (Min) – 2N6030
  = 15 (Min) – 2N6031
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Complement to NPN Transistor Series – 2N5629, 2N5630, 2N5631

16 AMPERE
POWER TRANSISTORS
PNP SILICON

100-120-140 VOLTS
200 WATTS



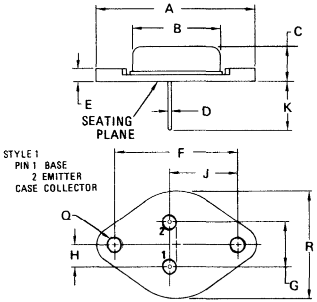
*MAXIMUM RATINGS

Rating	Symbol	2N6029	2N6030	2N6031	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 16 → ← 20 →			Adc
Base Current – Continuous	I_B	← 5.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 200 → ← 1.14 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J T_{stg}	← -65 to +200 →			°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.



STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

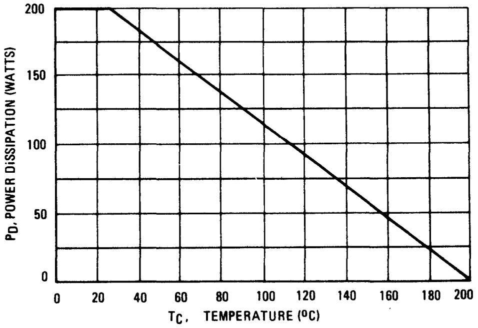
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

Collector connected to case.

CASE 11-01

FIGURE 1 – POWER DERATING



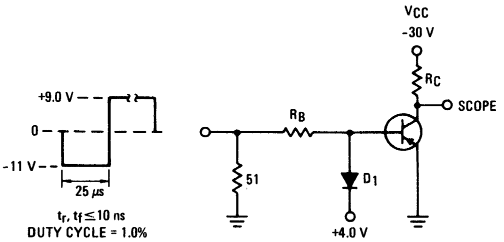
Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N6029 2N6030 2N6031	$V_{CEO(sus)}$	100 120 140	– – –	Vdc
Collector-Emitter Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 70 Vdc, I_B = 0)	2N6029 2N6030 2N6031	I_{CEO}	– – –	2.0 2.0 2.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	– –	2.0 7.0	mAdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	2.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 2.0 Vdc)	2N6029 2N6030 2N6031 All Types	h_{FE}	25 20 15 4.0	100 80 60 –	–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 16 Adc, I_B = 4.0 Adc)		$V_{CE(sat)}$	– –	1.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	1000	pF
Small-Signal Current Gain (I_C = 4.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	–	–

*Indicates JEDEC Registered Data. (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

FIGURE 3 — TURN-ON TIME

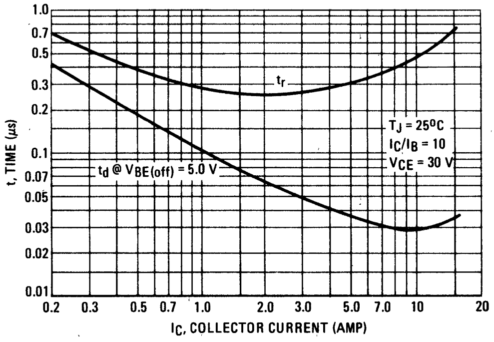


FIGURE 4 – THERMAL RESPONSE

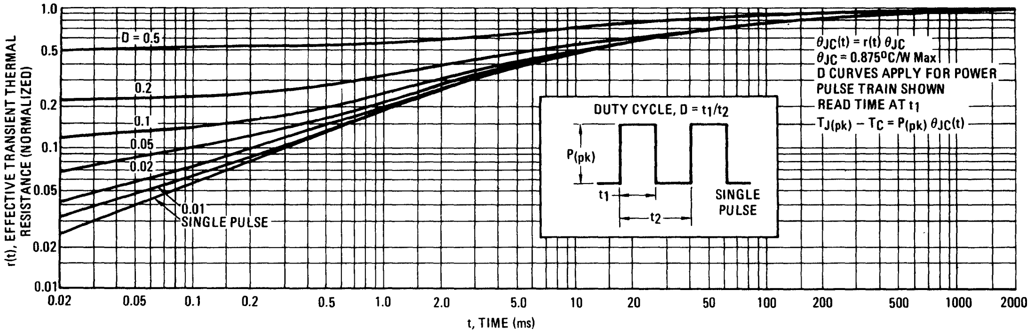
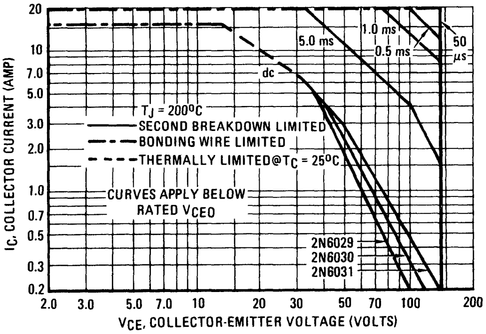


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

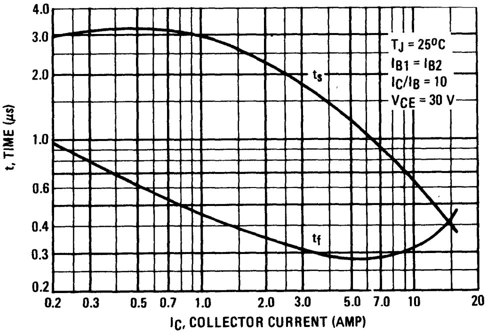
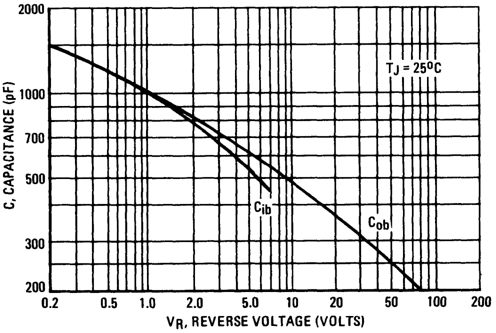


FIGURE 7 – CAPACITANCE



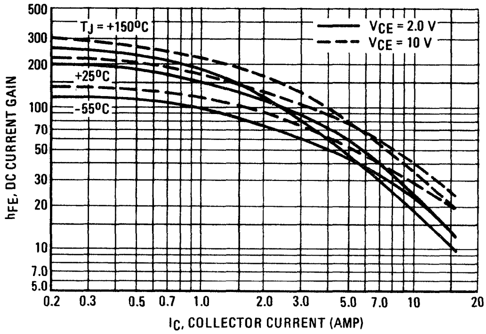


FIGURE 8 – DC CURRENT GAIN

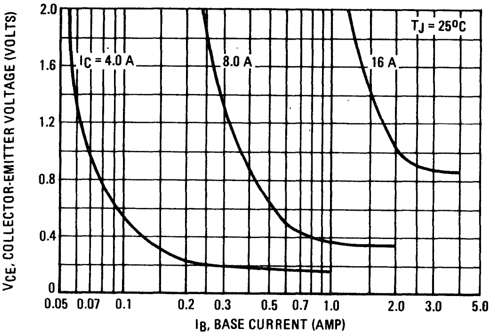


FIGURE 9 – COLLECTOR SATURATION REGION

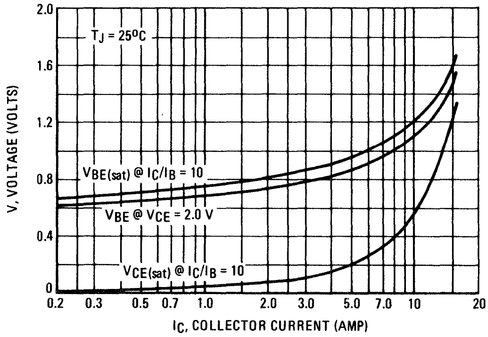


FIGURE 10 – "ON" VOLTAGES

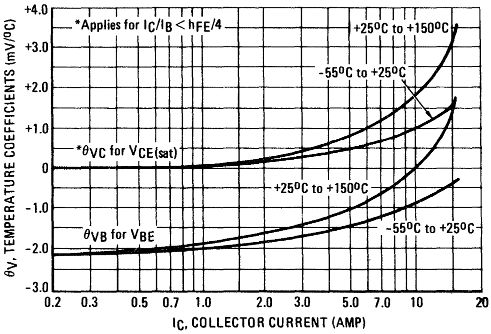


FIGURE 11 – TEMPERATURE COEFFICIENTS

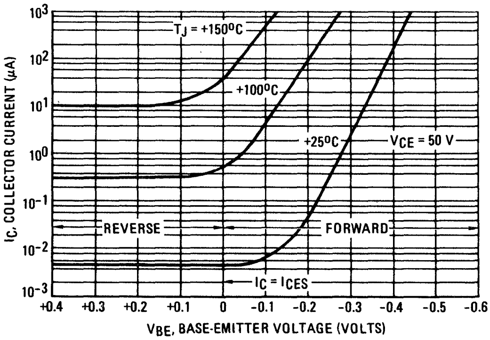


FIGURE 12 – COLLECTOR CUTOFF REGION

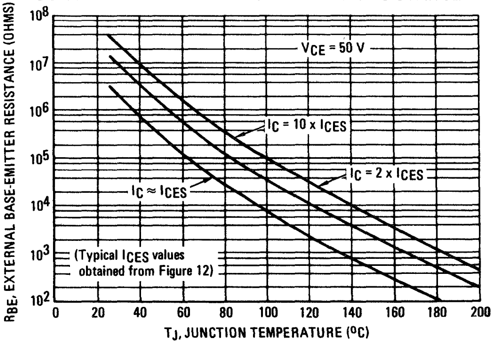


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE

2N6034, 2N6035, 2N6036 PNP (SILICON)
2N6037, 2N6038, 2N6039 NPN

PLASTIC DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

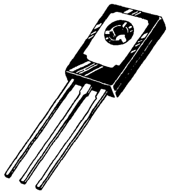
. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain — h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) — 2N6034, 2N6037
  = 60 Vdc (Min) — 2N6035, 2N6038
  = 80 Vdc (Min) — 2N6036, 2N6039
- Forward Biased Second Breakdown Current Capability $I_{S/b}$ = 1.5 Adc @ 25 Vdc
- Monolithic Construction with Built-In Base-Emitter Resistors to Limit Leakage Multiplication
- Space-Saving High Performance-to-Cost Ratio Case 77 Plastic Package

DARLINGTON
4-AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40, 60, 80 VOLTS
40 WATTS



*MAXIMUM RATINGS

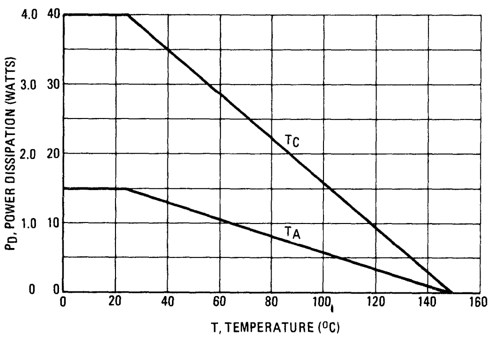
Rating	Symbol	2N6034 2N6037	2N6035 2N6038	2N6036 2N6039	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	4.0 8.0			Adc
Base Current	I_B	100			mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Watts W/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150			°C

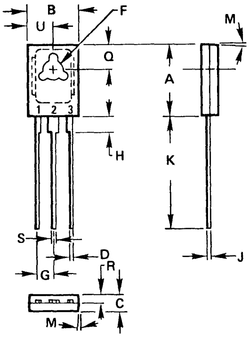
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.3	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.36 BSC		0.093 BSC	
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.38	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155

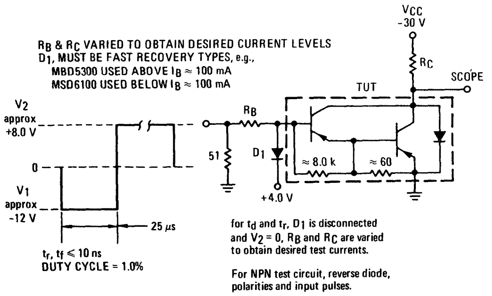
CASE 77-03

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6034, 2N6037		40	–	
	2N6035, 2N6038		60	–	
	2N6036, 2N6039		80	–	
Collector-Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N6034, 2N6037		–	0.5	
(V_{CE} = 30 Vdc, I_B = 0)	2N6035, 2N6038		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N6036, 2N6039		–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6034, 2N6037		–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6035, 2N6038		–	0.5	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6036, 2N6039		–	0.5	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6034, 2N6037		–	2.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6035, 2N6038		–	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6036, 2N6039		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N6034, 2N6037		–	0.5	
(V_{CB} = 60 Vdc, I_E = 0)	2N6035, 2N6038		–	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N6036, 2N6039		–	0.5	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			500	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			750	15,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)			–	2.0	
(I_C = 4.0 Adc, I_B = 40 mAdc)			–	3.0	
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Small-Signal Current-Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	25	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E =0, f = 0.1 MHz)	2N6034, 2N6035, 2N6036		–	200	
	2N6037, 2N6038, 2N6039		–	100	

*Indicates JEDEC Registered Data.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



R_B & R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1, MUST BE FAST RECOVERY TYPES, e.g.,
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

for t_d and t_r, D_1 is disconnected and V_2 = 0, R_B and R_C are varied to obtain desired test currents.

For NPN test circuit, reverse diode, polarities and input pulses.

FIGURE 3 – SWITCHING TIMES

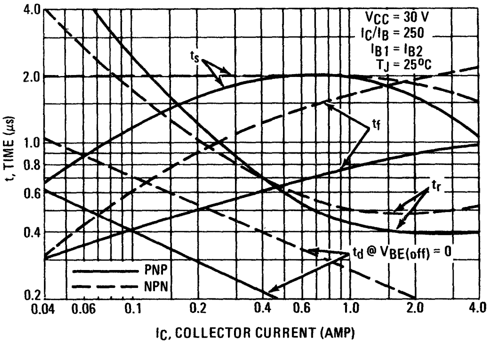
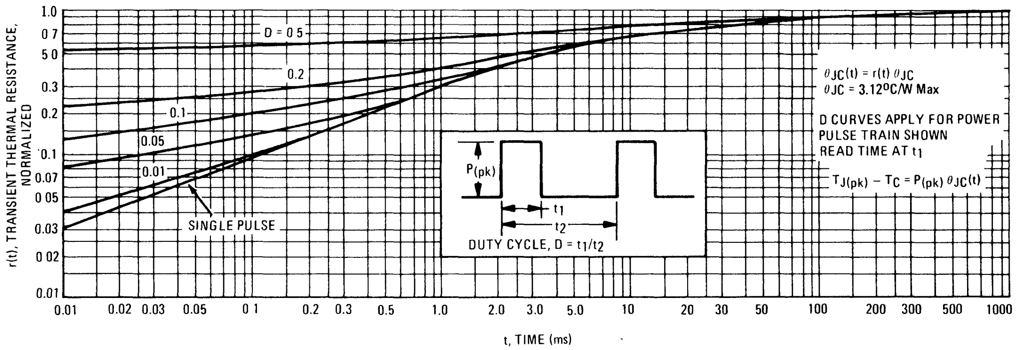


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 5 – 2N6034, 2N6035, 2N6036

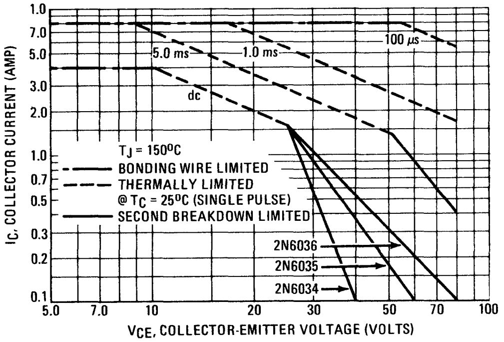


FIGURE 6 – 2N6037 2N6038, 2N6039

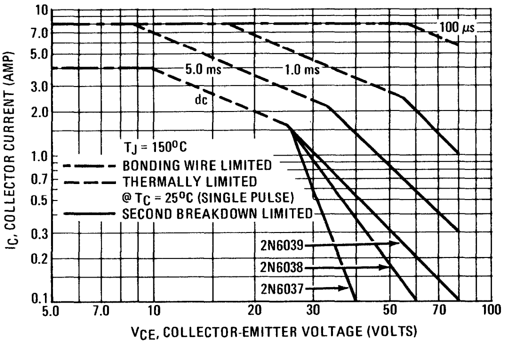
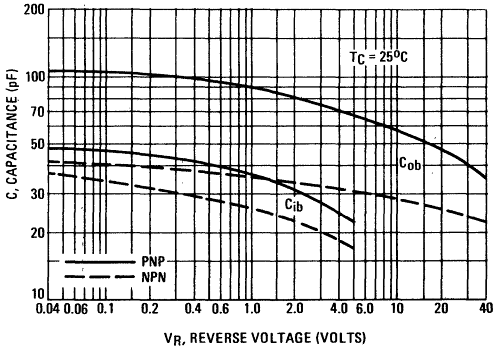


FIGURE 7 – CAPACITANCE



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

PNP
2N6034, 2N6035, 2N6036

NPN
2N6037, 2N6038, 2N6039

FIGURE 8 – DC CURRENT GAIN

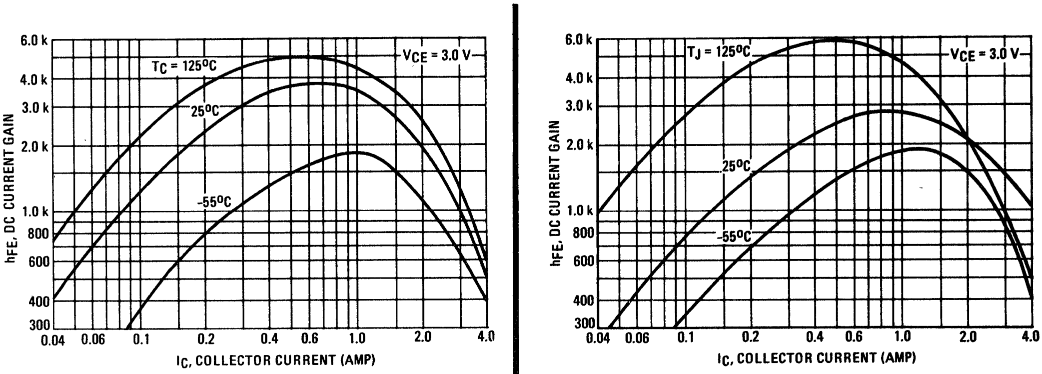


FIGURE 9 – COLLECTOR SATURATION REGION

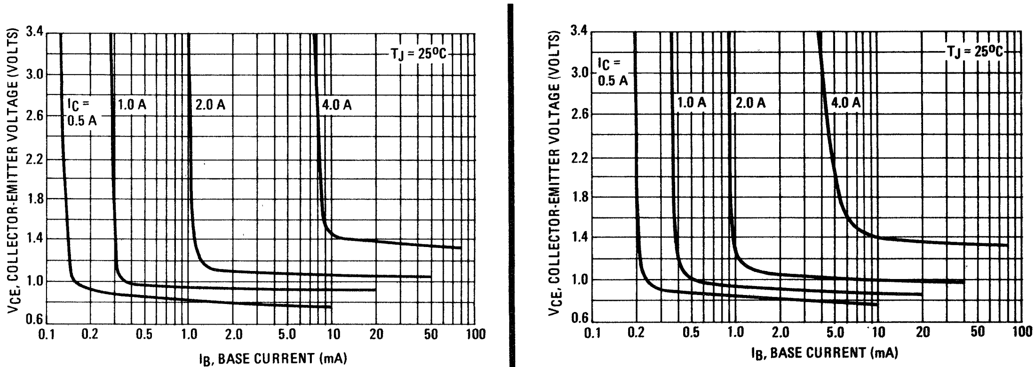
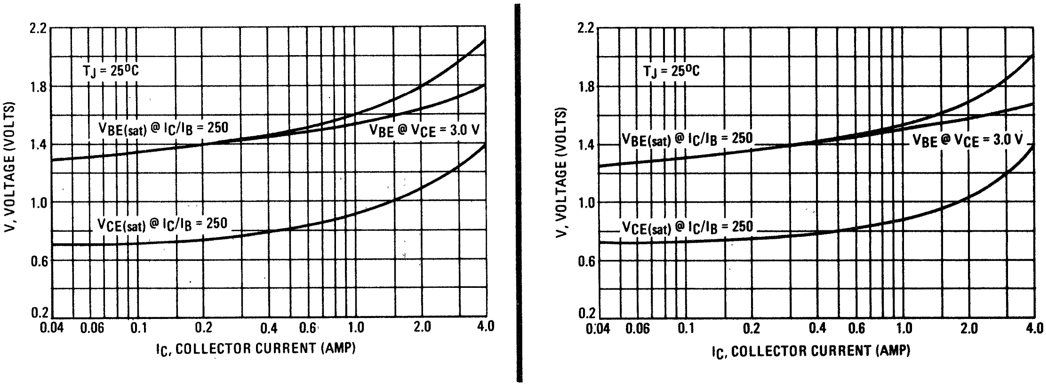


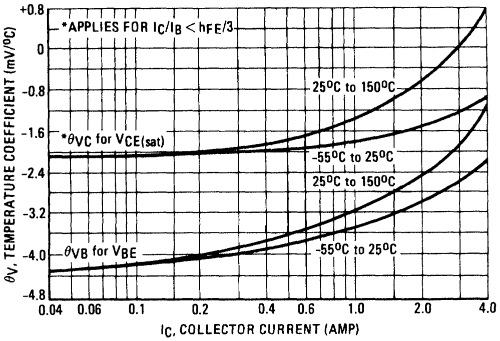
FIGURE 10 – "ON" VOLTAGES



PNP
2N6034, 2N6035, 2N6036

NPN
2N6037, 2N6038, 2N6039

FIGURE 11 – TEMPERATURE COEFFICIENCTS



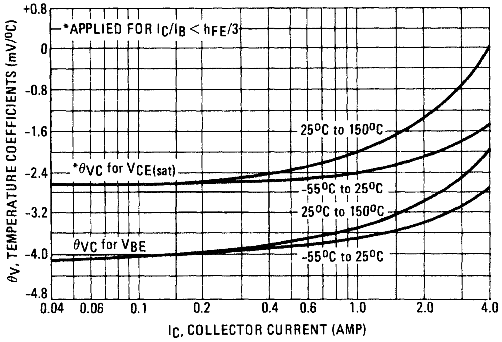
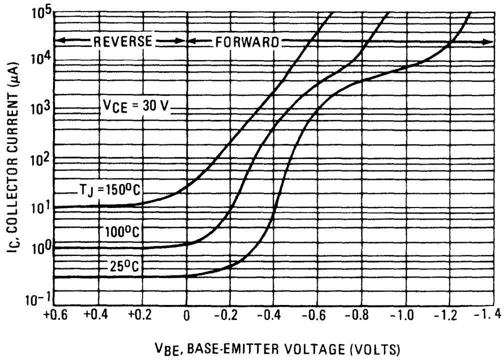


FIGURE 12 – COLLECTOR CUT-OFF REGION



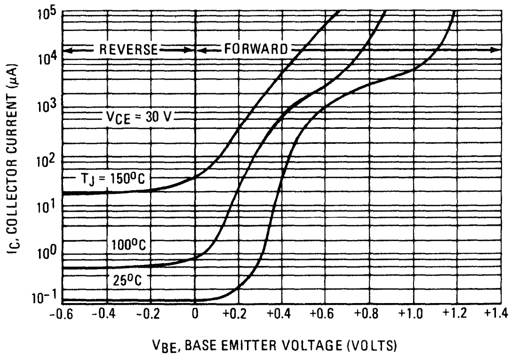
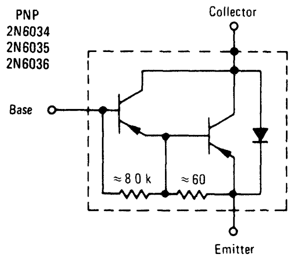
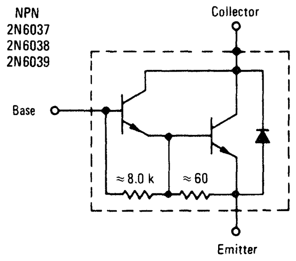


FIGURE 13 – DARLINGTON SCHEMATIC





2N6040 thru 2N6042 PNP (SILICON)
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6042 PNP
MJE6043 thru MJE6045 NPN

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc (1)
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6040, 2N6043
  = 80 Vdc (Min) – 2N6041, 2N6044
  = 100 Vdc (Min) – 2N6042, 2N6045
- Low Collector-Emitter Saturation Voltage – (1)
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc – 2N6040,41,2N6043,44
  = 2.0 Vdc (Max) @ I_C = 3.0 Adc – 2N6042, 2N6045
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- Thermopad High Efficiency Compact Package

(1) Applies to corresponding in-house part numbers also.

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
75 WATTS

*MAXIMUM RATINGS

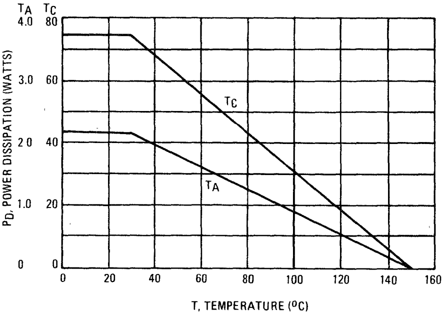
Rating	Symbol	2N6040 2N6043 MJE6040 MJE6043	2N6041 2N6044 MJE6041 MJE6044	2N6042 2N6045 MJE6042 MJE6045	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 8.0 → ← 16 →			Adc
Base Current	I_B	← 120 →			mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 75 → ← 0.60 →			Watts W/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.2 → ← 0.0175 →			Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← –65 to +150 →			°C

THERMAL CHARACTERISTICS

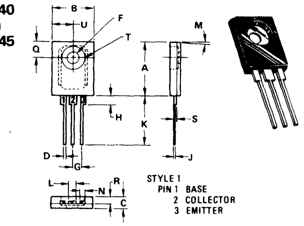
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	57	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



2N6040 thru 2N6045



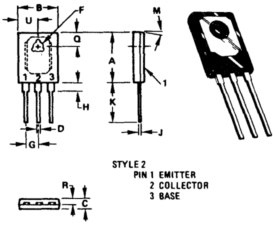
STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0.152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

1 DIM "G" IS TO CENTER LINE OF LEADS

CASE 199-04

MJE6040 thru MJE6045



STYLE 2
PIN 1 EMITTER
2 COLLECTOR
3 BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

NOTE
1 LEADS WITHIN .005" RAD OF TRUE POSITION (TP) AT MMC

CASE 90-05

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6040, 2N6043, MJE6040, MJE6043 2N6041, 2N6044, MJE6041, MJE6044 2N6042, 2N6045, MJE6042, MJE6045	$V_{CEO(sus)}$	60 80 100	– – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	2N6040, 2N6043, MJE6040, MJE6043 2N6041, 2N6044, MJE6041, MJE6044 2N6042, 2N6045, MJE6042, MJE6045	I_{CEO}	– – –	0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6040, 2N6043, MJE6040, MJE6043 2N6041, 2N6044, MJE6041, MJE6044 2N6042, 2N6045, MJE6042, MJE6045 2N6040, 2N6043, MJE6040, MJE6043 2N6041, 2N6044, MJE6041, MJE6044 2N6042, 2N6045, MJE6042, MJE6045	I_{CEX}	– – – – – –	0.5 0.5 0.5 5.0 5.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	2N6040, 2N6043, MJE6040, MJE6043 2N6041, 2N6044, MJE6041, MJE6044 2N6042, 2N6045, MJE6042, MJE6045	I_{CBO}	– – –	0.5 0.5 0.5	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	2N6040,41, 2N6043,44, MJE6040,41, MJE6043,44 2N6042, 2N6045, MJE6042, MJE6045 All Types	h_{FE}	1000 1000 100	20,000 20,000 –	–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 16 mAdc) (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 8.0 Adc, I_B = 80 mAdc)	2N6040,41,2N6043,44,MJE6040,41,MJE6043,44 2N6042,2N6045,MJE6042,MJE6045 All Types	$V_{CE(sat)}$	– – –	2.0 2.0 4.0	Vdc
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{BE(sat)}$	–	4.5	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6040/2N6042, MJE6040/MJE6042 2N6043/2N6045, MJE6043/MJE6045	C_{ob}	– –	300 200	pF
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

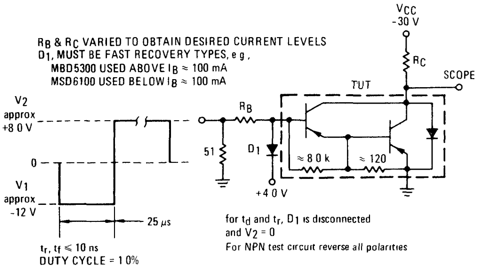


FIGURE 3 – SWITCHING TIMES

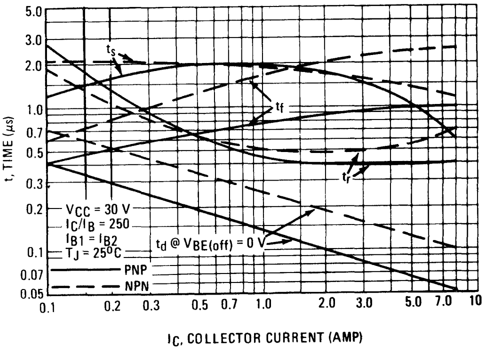


FIGURE 4 – THERMAL RESPONSE

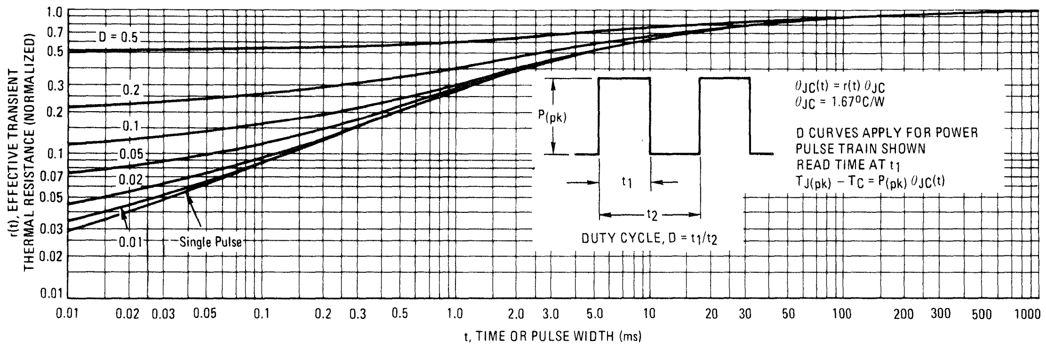
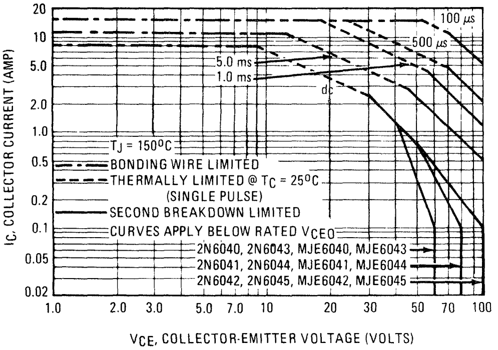


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

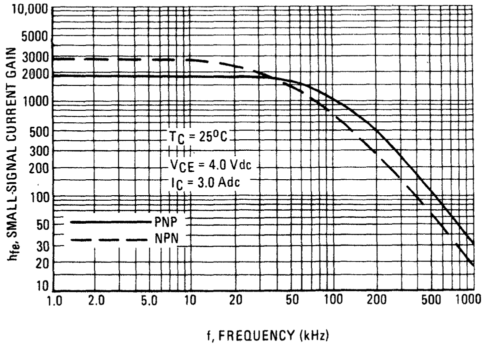
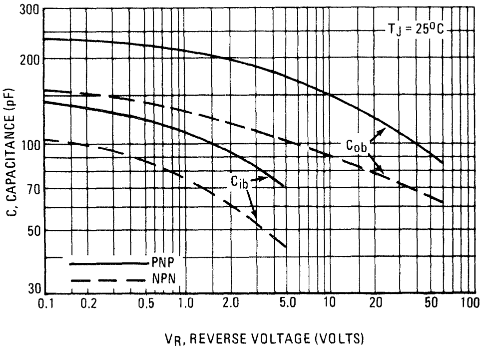


FIGURE 7 – CAPACITANCE



PNP
2N6040, 2N6041, 2N6042
MJE6040, MJE6041, MJE6042

NPN
2N6043, 2N6044, 2N6045
MJE6043, MJE6044, MJE6045

FIGURE 8 – DC CURRENT GAIN

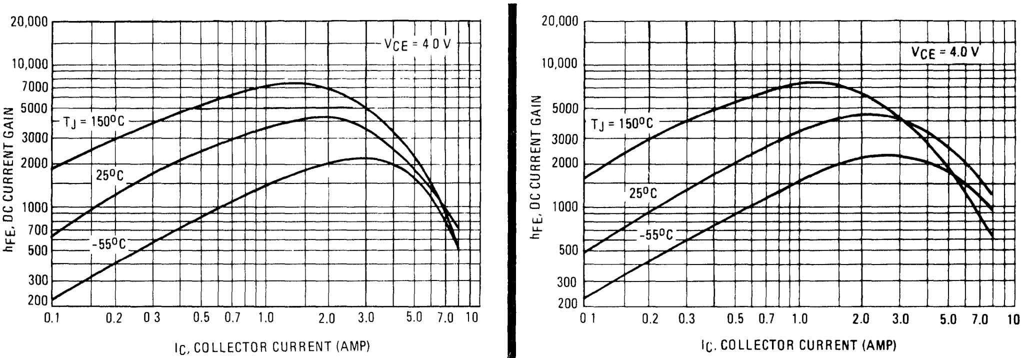


FIGURE 9 – COLLECTOR SATURATION REGION

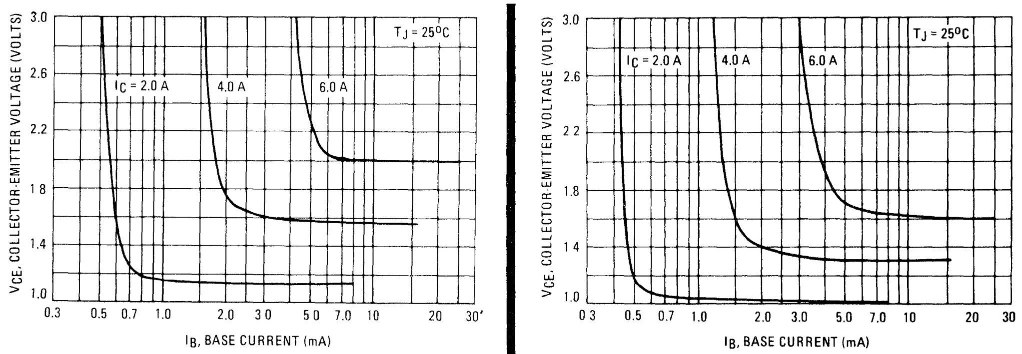
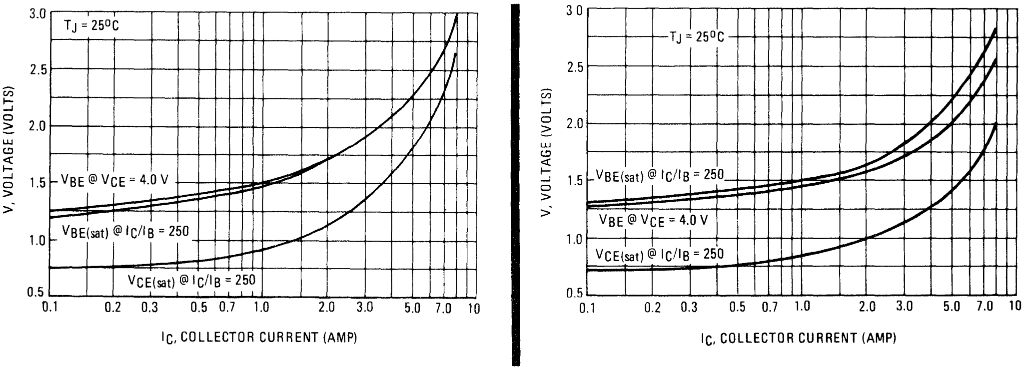


FIGURE 10 – "ON" VOLTAGES



PNP
2N6040, 2N6041, 2N6042
MJE6040, MJE6041, MJE6042

NPN
2N6043, 2N6044, 2N6045
MJE6043, MJE6044, MJE6045

FIGURE 11 – TEMPERATURE COEFFICIENTS

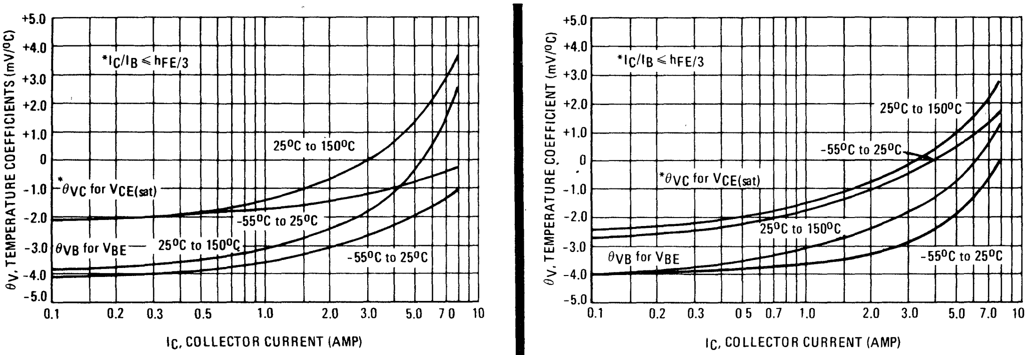


FIGURE 12 – COLLECTOR CUT-OFF REGION

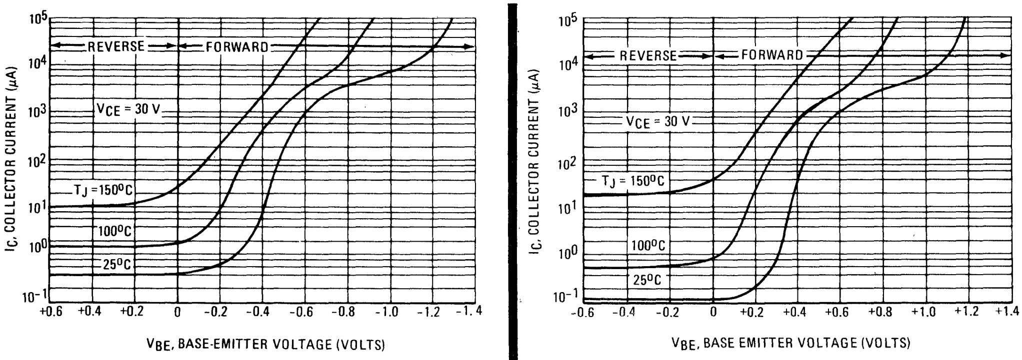
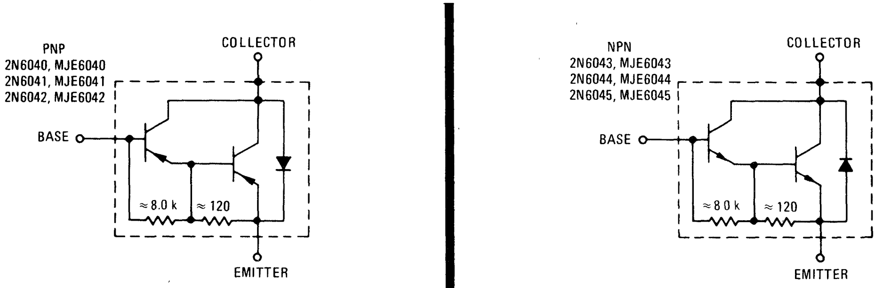


FIGURE 13 – DARLINGTON SCHEMATIC



2N6049 (SILICON)

MEDIUM-POWER PNP SILICON TRANSISTOR

. . . designed for general-purpose switching and amplifier applications

- Aluminum TO-66 Package for Better Power Handling Capability — 75 Watts @ T_C = 25°C
- Excellent Safe Operating Area
- DC Current Gain Specified to 4.0 Amperes
- Complement to NPN Type 2N3054A

4 AMPERE
POWER TRANSISTOR
PNP SILICON
55 VOLTS
75 WATTS

*MAXIMUM RATINGS

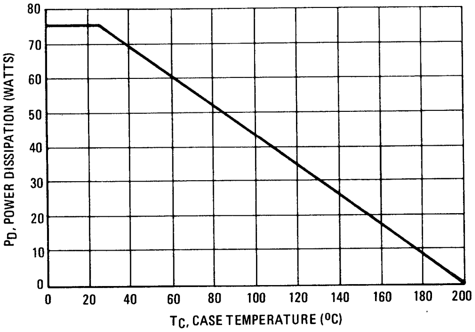
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	55	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	60	Vdc
Collector-Base Voltage	V_{CB}	90	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	4.0 10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°	P_D	75 0.43	Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200	°C

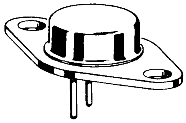
*Indicates JEDEC Registered Data

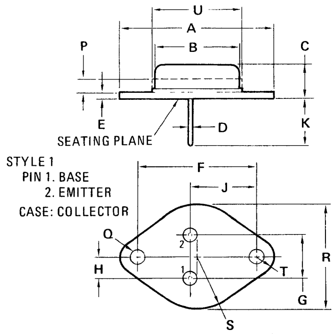
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.33	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING







STYLE 1
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	55	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, R_{BE} = 100 Ω	$V_{CER(sus)}$	60	–	Vdc
Collector Cuttoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	500	µAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 6.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	25 6.0	100	–
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 4.0 Adc, I_B = 800 mAdc)	$V_{CE(sat)}$	– –	0.5 2.0	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc)	f_T	3.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	200	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	25	180	

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUIT

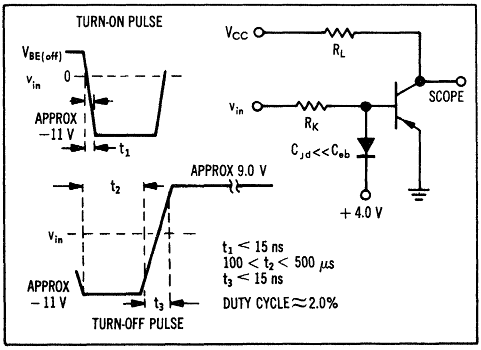


FIGURE 3 – TURN-ON TIME

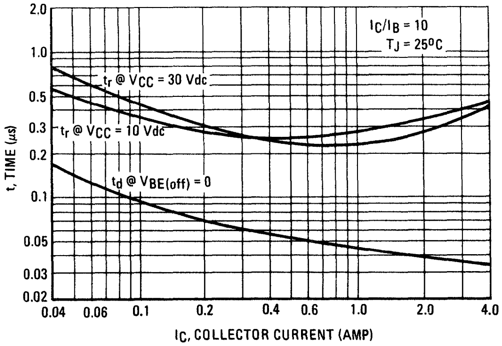


FIGURE 4 – THERMAL RESPONSE

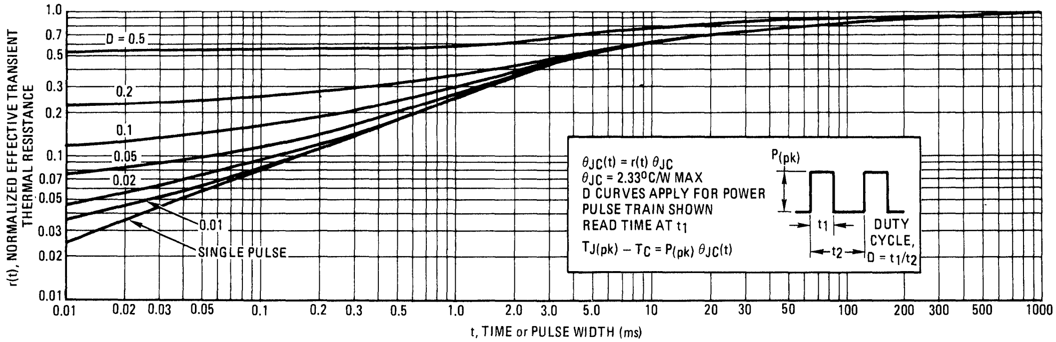
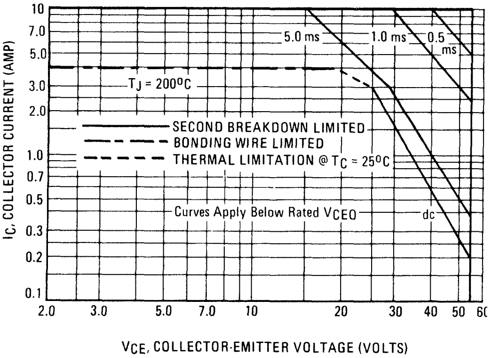


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 6 – TURN-OFF TIME

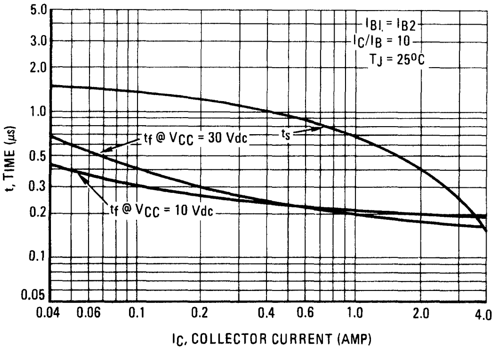


FIGURE 7 – CAPACITANCE

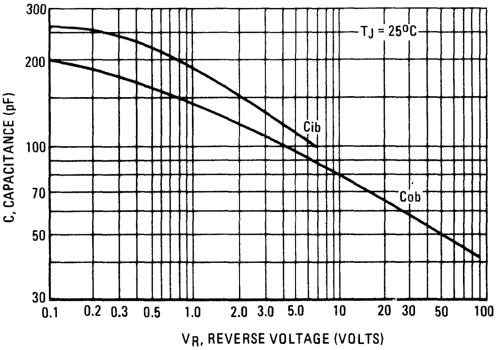


FIGURE 8 – DC CURRENT GAIN

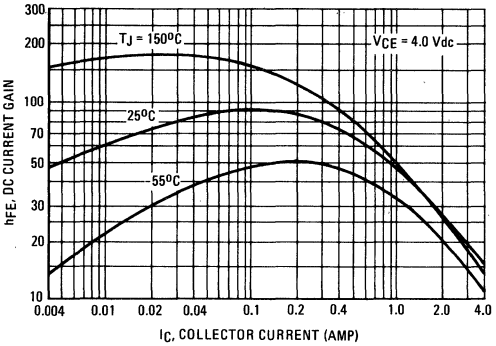


FIGURE 9 – COLLECTOR SATURATION REGION

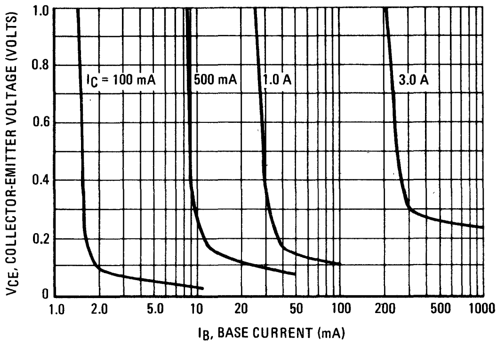


FIGURE 10 – TEMPERATURE COEFFICIENT

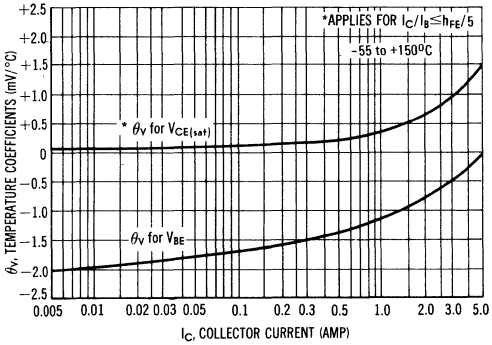


FIGURE 11 – "ON" VOLTAGES

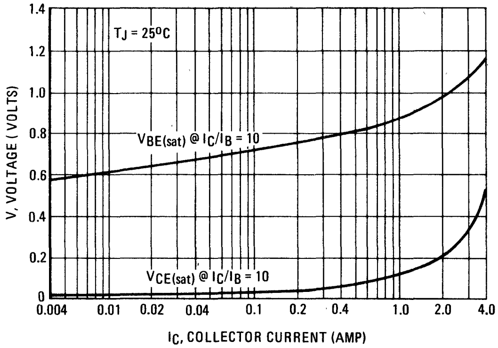


FIGURE 12 – COLLECTOR CUT-OFF REGION

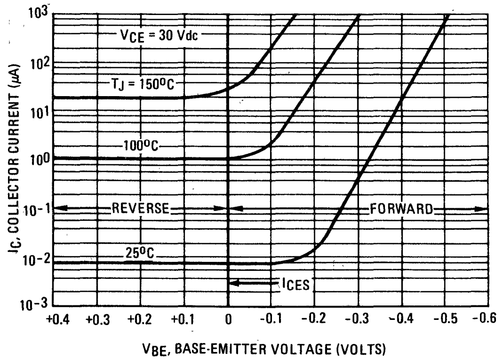
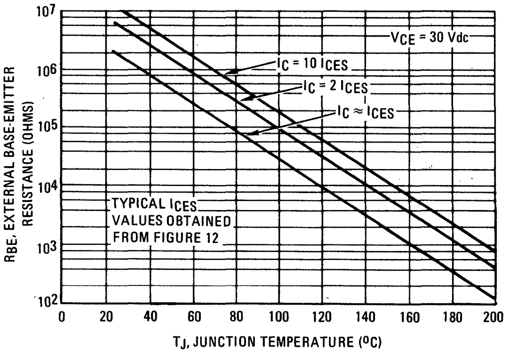


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



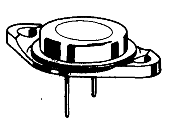
2N6050 thru 2N6052 PNP (SILICON)
2N6057 thru 2N6059 NPN

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
  h_{FE} = 3500 (Typ) @ I_C = 5.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6050, 2N6057
  80 Vdc (Min) – 2N6051, 2N6058
  100 Vdc (Min) – 2N6052, 2N6059
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
12 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
150 WATTS



*MAXIMUM RATINGS

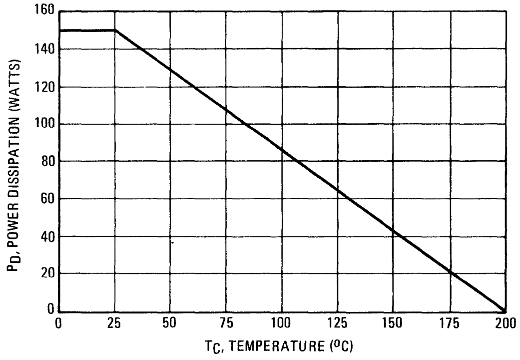
Rating	Symbol	2N6050 2N6057	2N6051 2N6058	2N6052 2N6059	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 12 → ← 20 →			Adc
Base Current	I_B	← 0.2 →			Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	← 150 → ← 0.857 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200°C →			°C

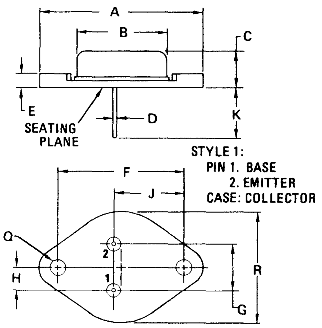
THERMAL CHARACTERISTICS

Characteristic	Symbol	Rating	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01

NOTE:
1. DIM "Q" IS DIA.

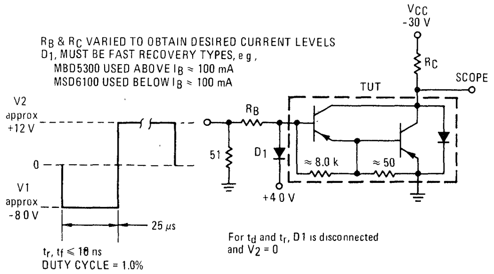
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	 2N6050, 2N6057 2N6051, 2N6058 2N6052, 2N6059	$V_{CEO(sus)}$	 60 80 100	 – – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 2N6050, 2N6057 2N6051, 2N6058 2N6052, 2N6059	I_{CEO}	 – – –	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 –	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 12 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 750 100	 18,000 –	–
Collector-Emitter Saturation Volatage (I_C = 6.0 Adc, I_B = 24 mAdc) (I_C = 12 Adc, I_B = 120 mAdc)		$V_{CE(sat)}$	 – –	 2.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 12 Adc, I_B = 120 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6050/2N6052 2N6057/2N6059	C_{ob}	– –	500 300	pF
Small-Signal Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data

(1)Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 – SWITCHING TIMES

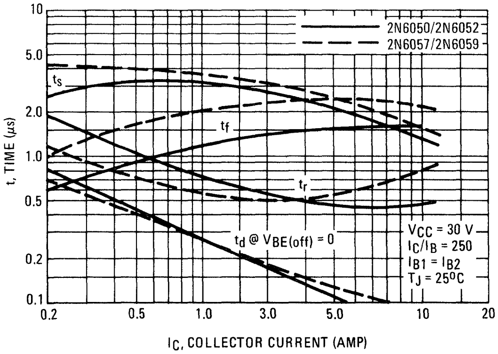
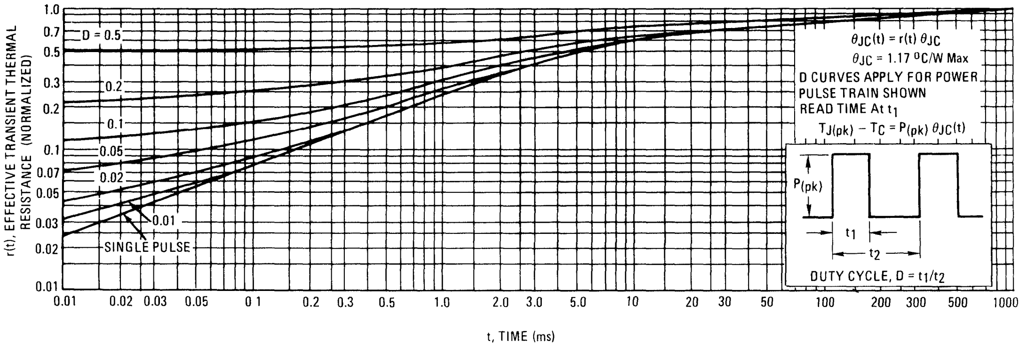


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6050, 2N6057

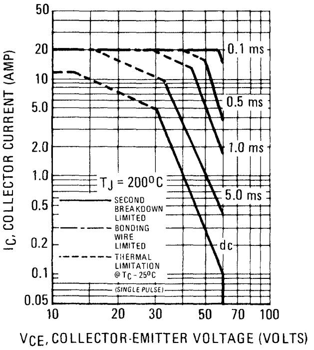


FIGURE 6 – 2N6051, 2N6058

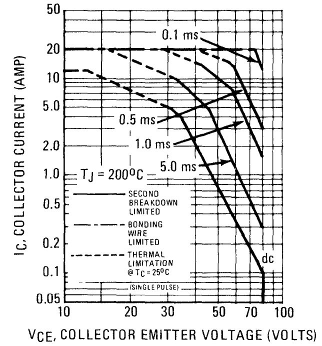
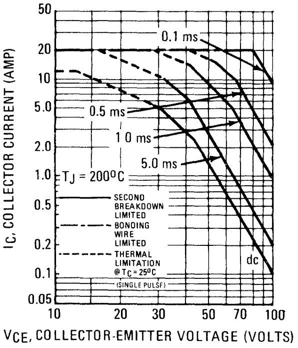


FIGURE 7 – 2N6052, 2N6059



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$ $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 8 – SMALL-SIGNAL CURRENT GAIN

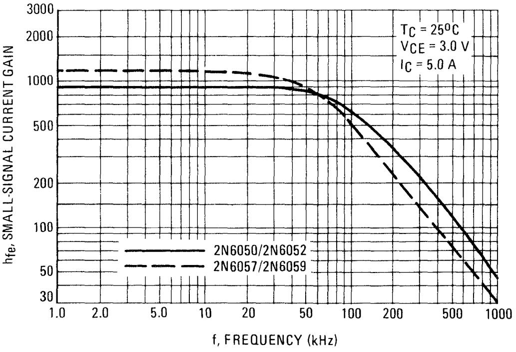
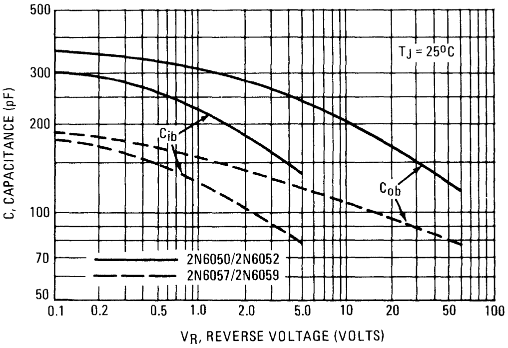


FIGURE 9 – CAPACITANCE



PNP
2N6050, 2N6051, 2N6052

NPN
2N6057, 2N6058, 2N6059

FIGURE 10 – DC CURRENT GAIN

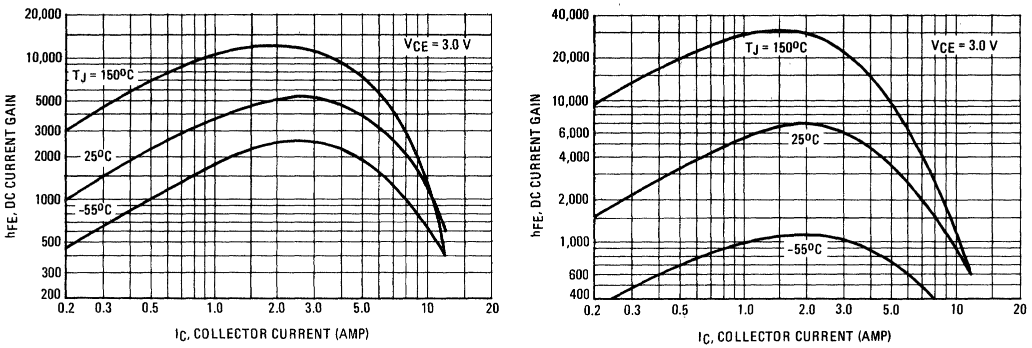


FIGURE 11 – COLLECTOR SATURATION REGION

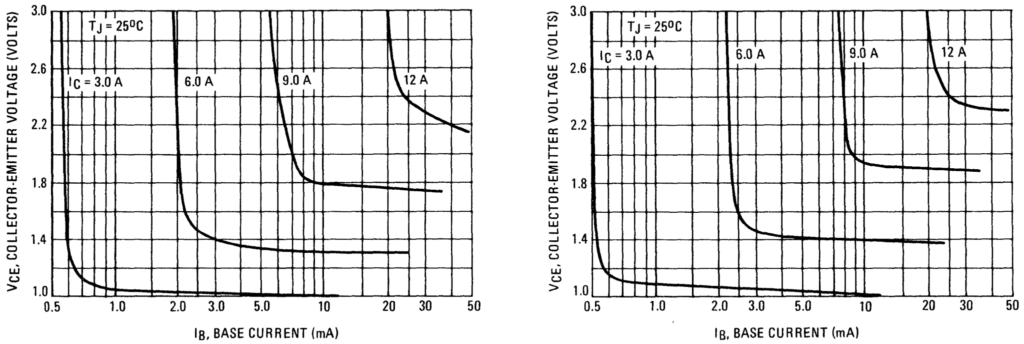
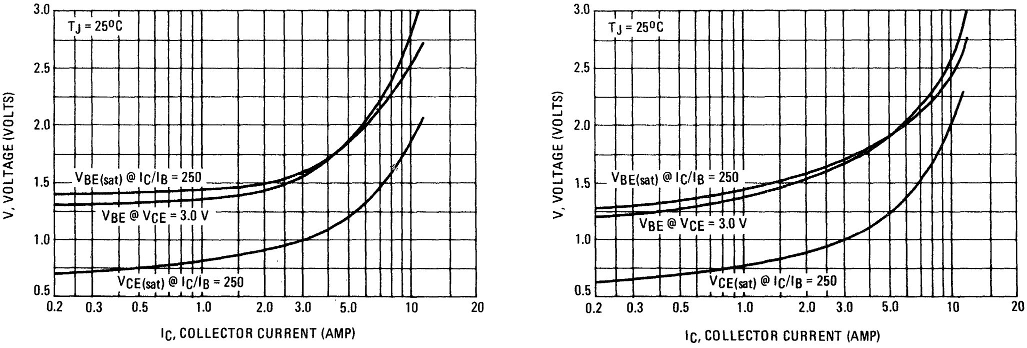


FIGURE 12 – "ON" VOLTAGES



PNP
2N6050, 2N6051, 2N6052

NPN
2N6057, 2N6058, 2N6059

FIGURE 13 – TEMPERATURE COEFFICIENTS

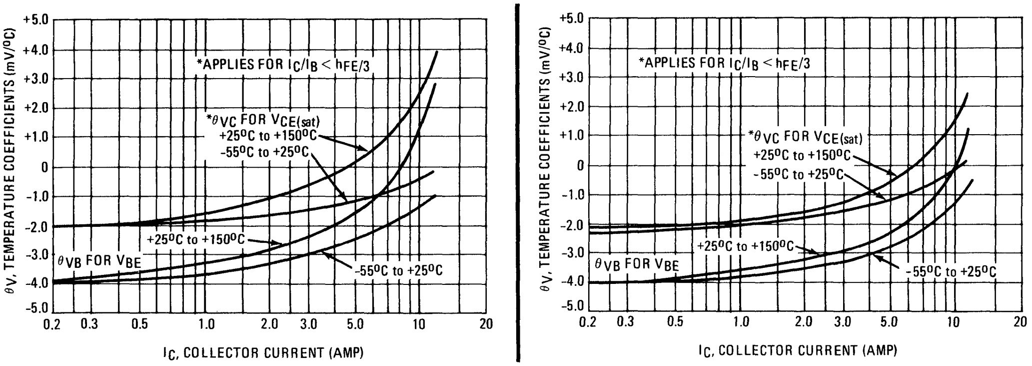


FIGURE 14 – COLLECTOR CUT-OFF REGION

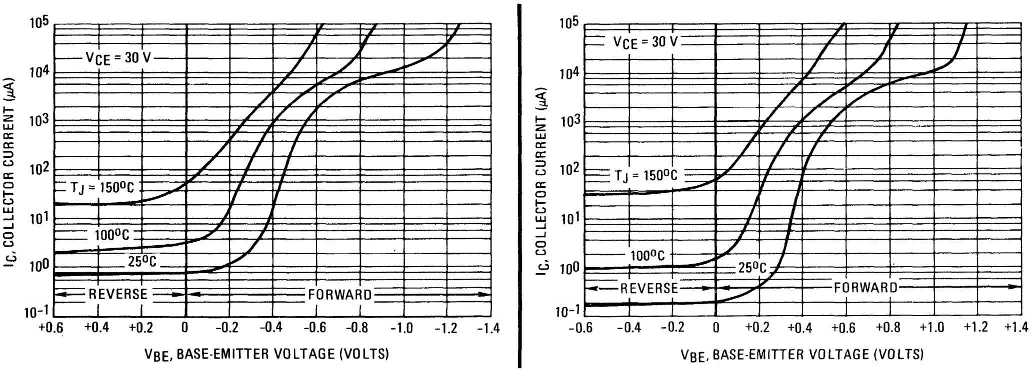
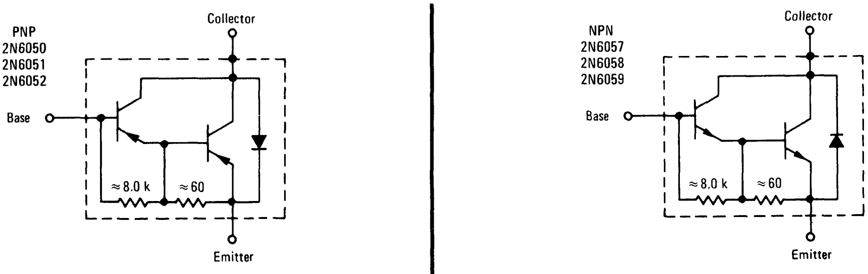


FIGURE 15 – DARLINGTON SCHEMATICS



2N6053, 2N6054, 2N6298, 2N6299 PNP (SILICON)
2N6055, 2N6056, 2N6300, 2N6301 NPN

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
  h_{FE} = 3000 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6053, 2N6055, 2N6298, 2N6300
  = 80 Vdc (Min) — 2N6054, 2N6056, 2N6299, 2N6301
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc
  = 3.0 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

*MAXIMUM RATINGS

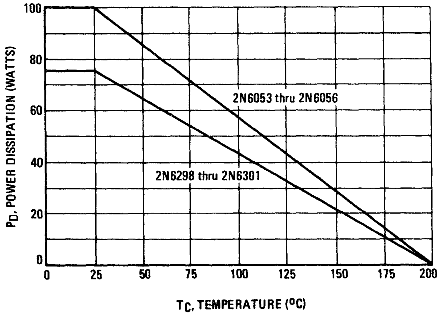
Rating	Symbol	2N6053 2N6055 2N6298 2N6300	2N6054 2N6056 2N6299 2N6301	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	8.0 16		Adc
Base Current	I_B	120		mAdc
		2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.571	75 0.428	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.75	2.33	°C/W

*Indicates JEDEC Registered Data.

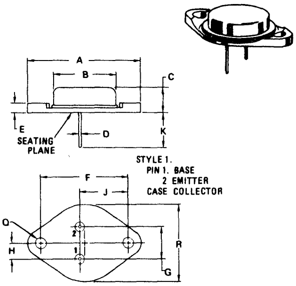
FIGURE 1 — POWER DERATING



DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
75,100 WATTS

2N6053
2N6054
2N6055
2N6056



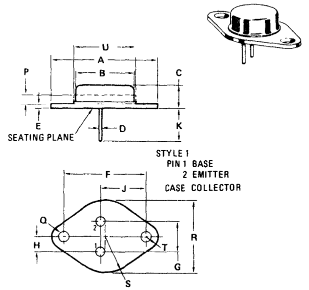
STYLE 1.
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE.
1. DIM "Q" IS DIA

CASE 11-03

2N6298
2N6299
2N6300
2N6301



STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.368	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply

CASE 80-02
TO-66

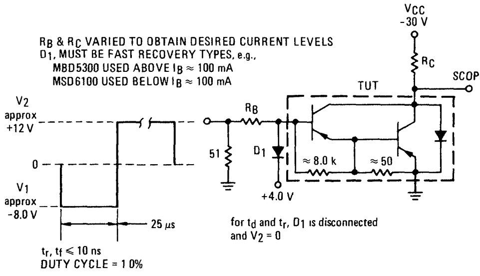
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0) 2N6053, 2N6055, 2N6298, 2N6300 2N6054, 2N6056, 2N6299, 2N6301	$V_{CEO(sus)}$	 60 80	 – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) 2N6053, 2N6055, 2N6298, 2N6300 (V_{CE} = 40 Vdc, I_B = 0) 2N6054, 2N6056, 2N6299, 2N6301	I_{CEO}	 – –	 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C	I_{CEX}	 – –	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	 750 100	 18000 –	–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 16 mAdc) (I_C = 8.0 Adc, I_B = 80 mAdc)	$V_{CE(sat)}$	 – –	 2.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common Emitter Small-Signal Short Circuit Current Transfer Ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$\lvert h_{fe} \rvert$	4.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) 2N6053, 2N6054, 2N6298, 2N6299 2N6055, 2N6056, 2N6300, 2N6301	C_{ob}	 – –	 300 200	pF
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)	h_{fe}	300	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0 %.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode, polarities and input pulses.

FIGURE 3 – SWITCHING TIMES

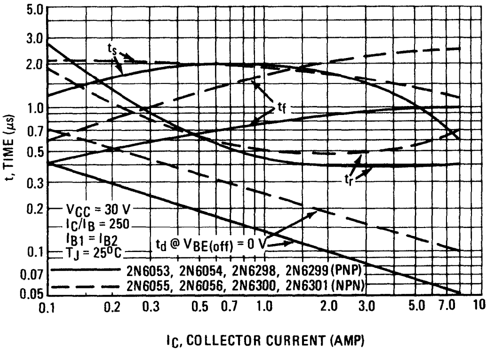
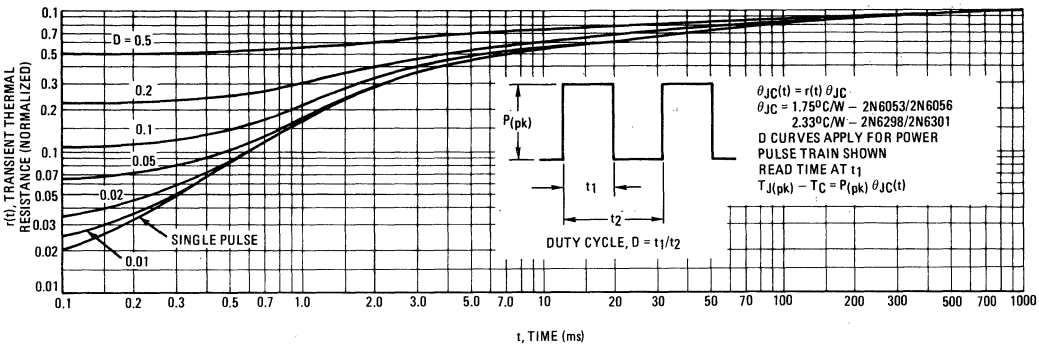


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6053 thru 2N6056

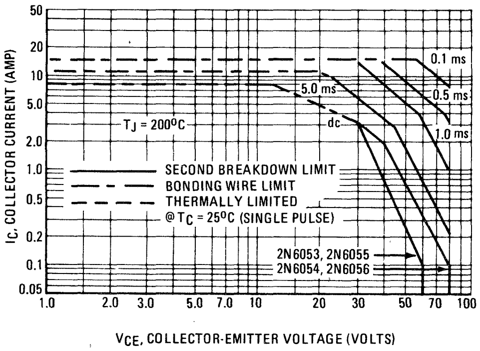
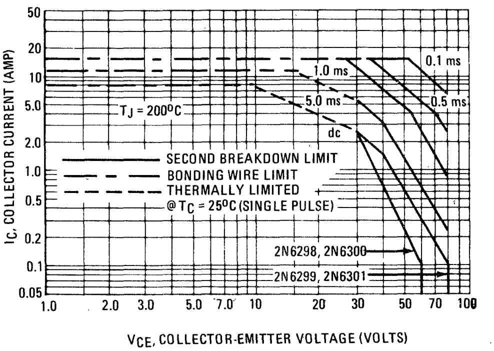


FIGURE 6 – 2N6298 thru 2N6301



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 7 – SMALL-SIGNAL CURRENT GAIN

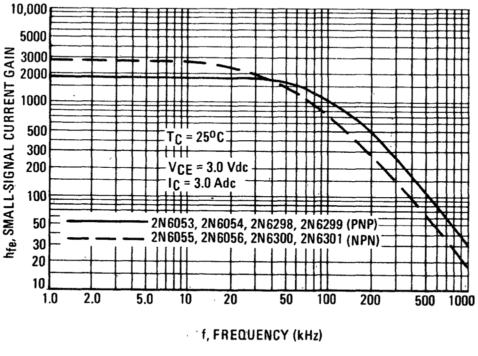
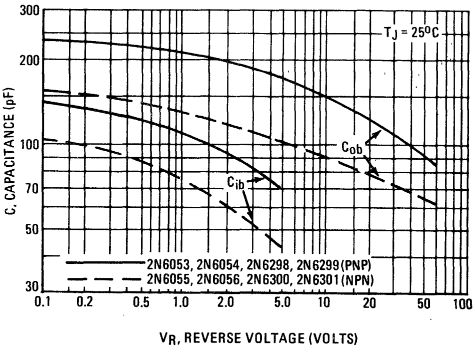


FIGURE 8 – CAPACITANCE



PNP **NPN**

2N6053, 2N6054, 2N6298, 2N6299 **2N6055, 2N6056, 2N6300, 2N6301**

FIGURE 9 – DC CURRENT GAIN

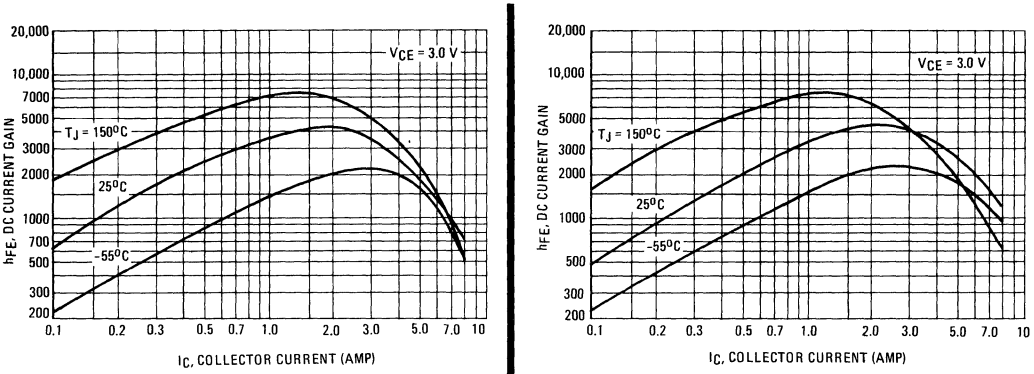


FIGURE 10 – COLLECTOR SATURATION REGION

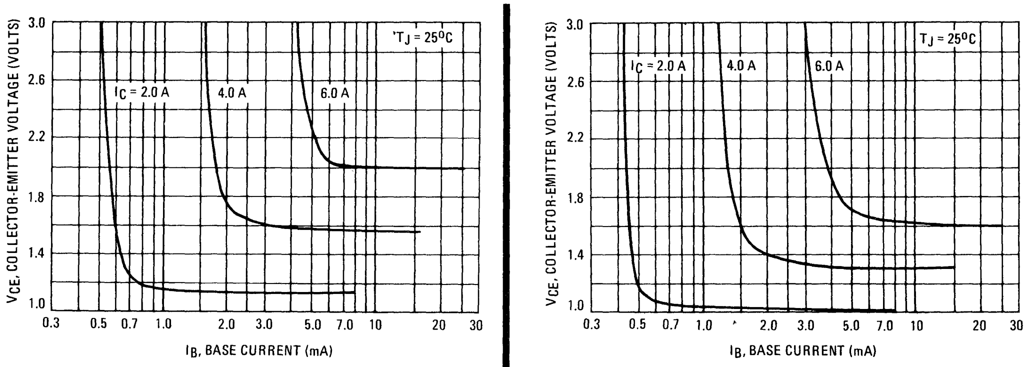
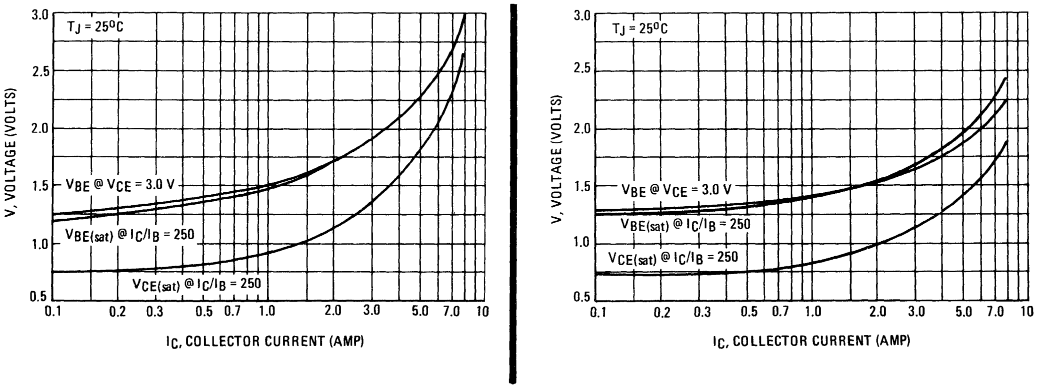


FIGURE 11 – "ON" VOLTAGES



PNP

2N6053, 2N6054, 2N6298, 2N6299

NPN

2N6055, 2N6056, 2N6300, 2N6301

FIGURE 12 – TEMPERATURE COEFFICIENTS

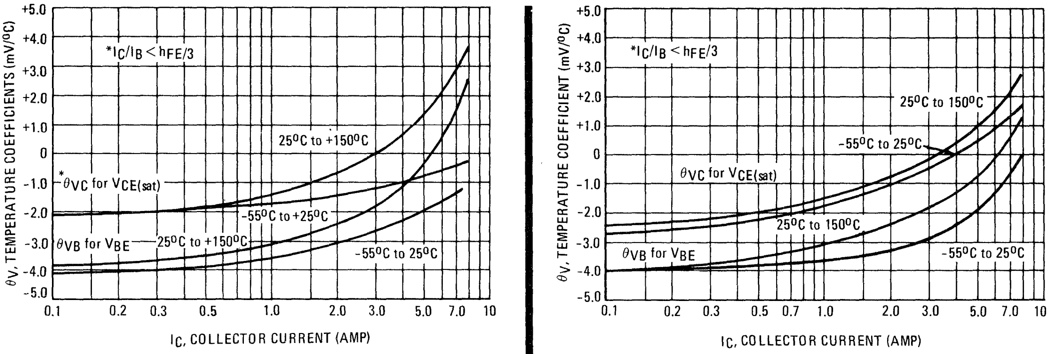


FIGURE 13 – COLLECTOR CUT-OFF REGION

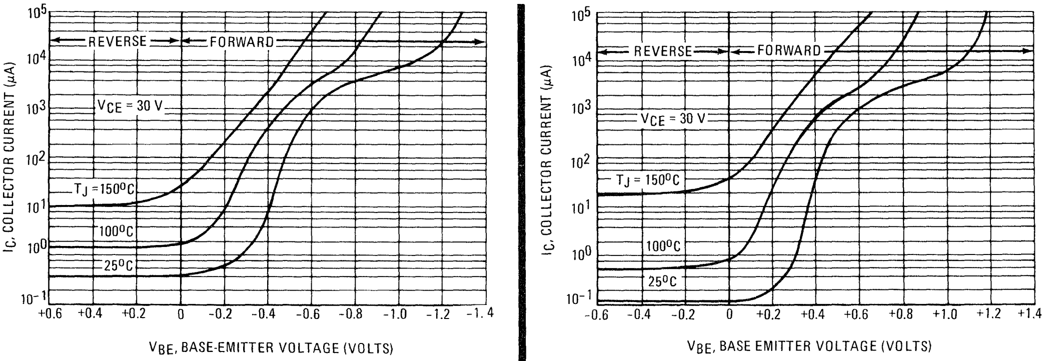
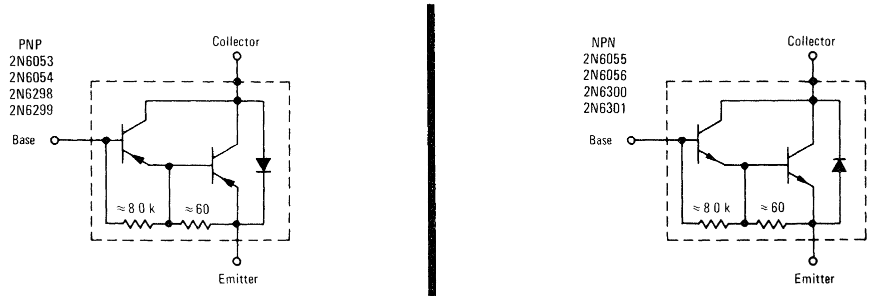


FIGURE 14 – DARLINGTON SCHEMATIC



2N6057 thru 2N6059 NPN (SILICON) For Specifications See 2N6050 Data.

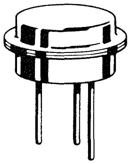
2N6064 (GERMANIUM)
2N6065
2N6066

PNP GERMANIUM POWER TRANSISTORS

. . . designed for high-voltage switching applications.

- Low Leakage Current —
  I_{CBO} = 3.0 mAdc (Max)
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.8 Vdc (Max) @ I_C = 10 Adc
- Switching Times — t_{on} = 10 μs @ 3.0 Adc
  t_{off} = 15 μs @ 3.0 Adc

10 AMPERE
POWER TRANSISTORS
PNP GERMANIUM
ALLOY DIFFUSED
80-120-160 VOLTS
56 WATTS



*MAXIMUM RATINGS

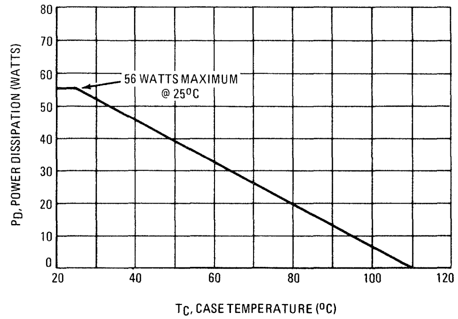
Rating	Symbol	2N6064	2N6065	2N6066	Unit
Collector-Emitter Voltage	V_{CEO}	80	120	160	Vdc
Collector-Base Voltage	V_{CB}	80	120	160	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous	I_C	← 10 →			Adc
Base Current	I_B	← 5.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 56 → ← 0.67 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +110 →			°C

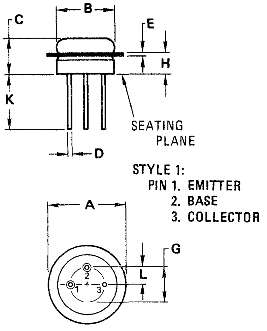
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.50	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.86	16.51	0.585	0.650
B	12.32	12.57	0.485	0.495
C	6.10	7.62	0.240	0.300
D	0.69	0.84	0.027	0.033
E	0.51	1.02	0.020	0.040
G	7.16 BSC		0.282 BSC	
H	4.19	4.70	0.165	0.185
K	9.14	11.18	0.360	0.440
L	3.58 BSC		0.141 BSC	

CASE 8

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N6064 2N6065 2N6066	$BV_{CEO(sus)}$	80 120 160	– – –	Vdc
Emitter Floating Potential (V_{CE} = 80 Vdc, I_B = 0) (V_{CE} = 120 Vdc, I_B = 0) (V_{CE} = 160 Vdc, I_B = 0)	2N6064 2N6065 2N6066	V_{EBF}	– – –	1.0 1.0 1.0	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 0.2 Vdc, T_C = +100°C) (V_{CE} = 120 Vdc, $V_{BE(off)}$ = 0.2 Vdc, T_C = +100°C) (V_{CE} = 160 Vdc, $V_{BE(off)}$ = 0.2 Vdc, T_C = +100°C)	2N6064 2N6065 2N6066	I_{CEX}	– – –	35 35 35	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 120 Vdc, I_E = 0) (V_{CB} = 160 Vdc, I_E = 0)	2N6064 2N6065 2N6066	I_{CBO}	– – –	3.0 3.0 3.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	50	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	20	50	–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 12 Vdc)		f_T	300	–	kHz
SWITCHING CHARACTERISTICS (SEE FIGURE 8)					
Turn-On Time (I_C = 3.0 Adc, I_{B1} = 0.3 Adc, V_{CC} = 30 Vdc)		t_{on}	–	10	µs
Turn-Off Time (I_C = 3.0 Adc, I_{B1} = I_{B2} = 0.3 Adc, V_{CC} = 30 Vdc)		t_{off}	–	15	µs

(1)Pulse Test: Pulse Width ≦300 µs, Duty Cycle ≦2.0%.

*Indicates JEDEC Registered Data.

FIGURE 2 – THERMAL RESPONSE

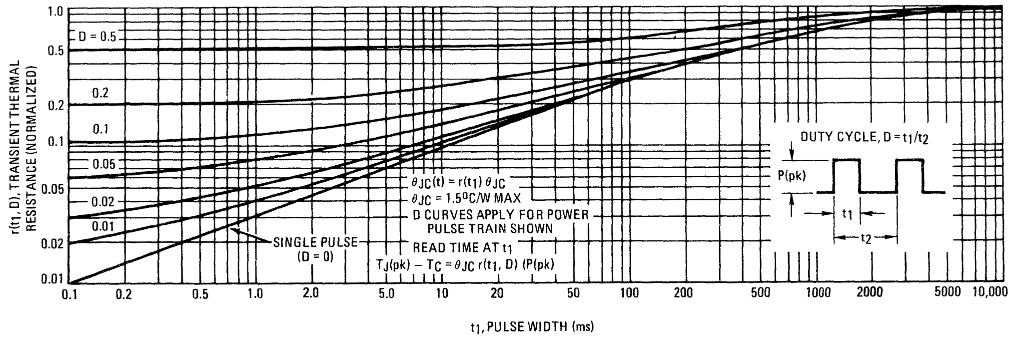


FIGURE 3 — CLAMPED INDUCTIVE SAFE OPERATING AREA

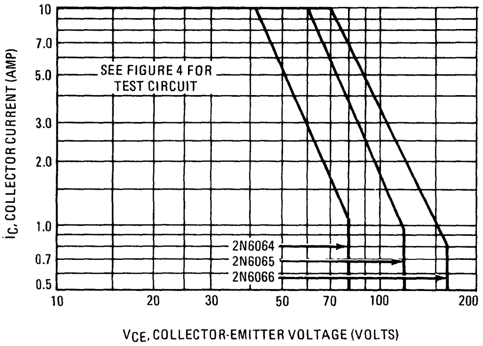


FIGURE 4 — CLAMPED INDUCTIVE TEST CIRCUIT

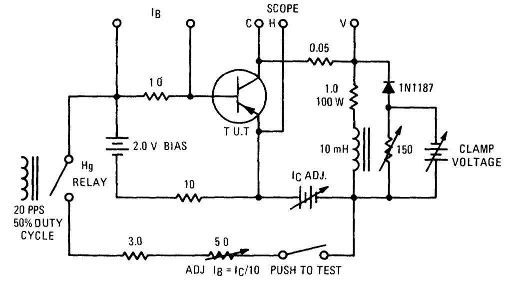


FIGURE 5 — ACTIVE-REGION SAFE-OPERATING AREA

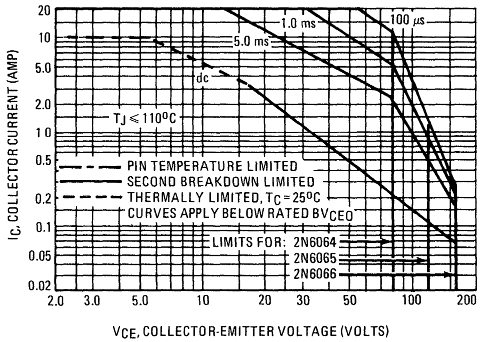


FIGURE 6 — CURRENT-GAIN—BANDWIDTH PRODUCT

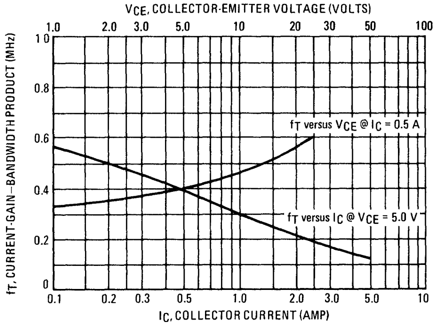


FIGURE 7 — SWITCHING TIMES

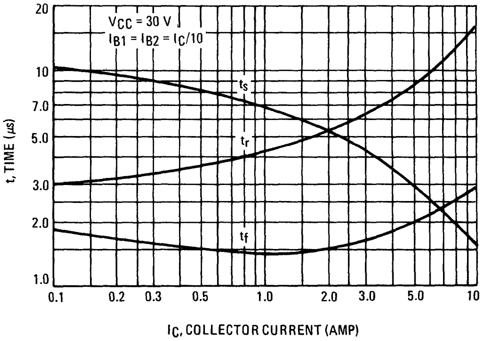


FIGURE 8 — SWITCHING TIMES TEST CIRCUIT

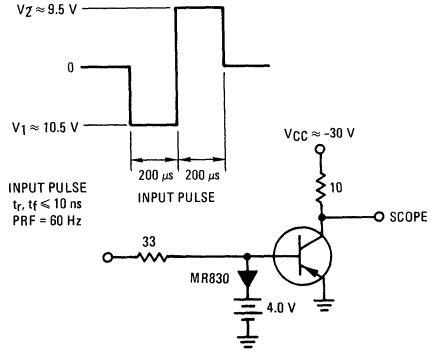


FIGURE 9 – DC CURRENT GAIN

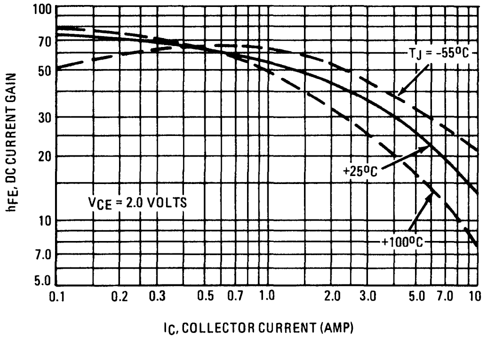


FIGURE 10 – COLLECTOR SATURATION REGION

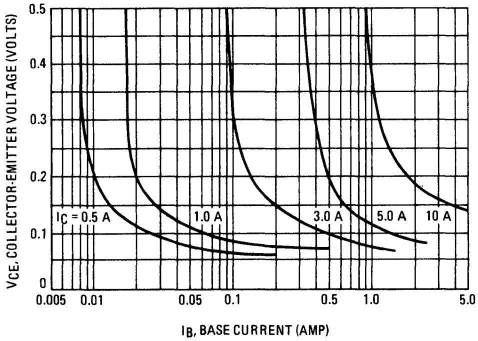


FIGURE 11 – "ON" VOLTAGES

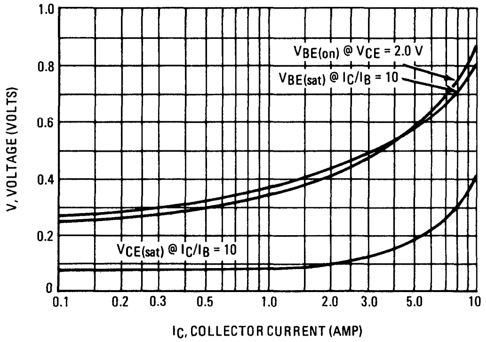


FIGURE 12 – TEMPERATURE COEFFICIENTS

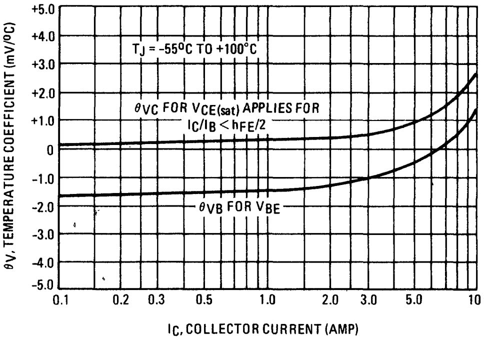


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE

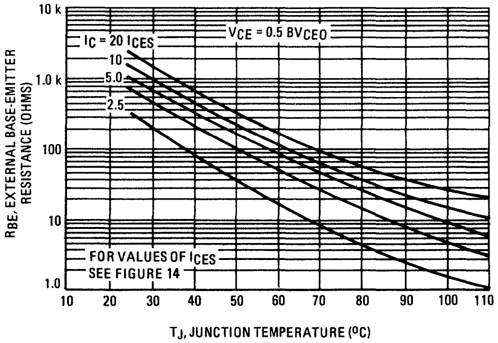
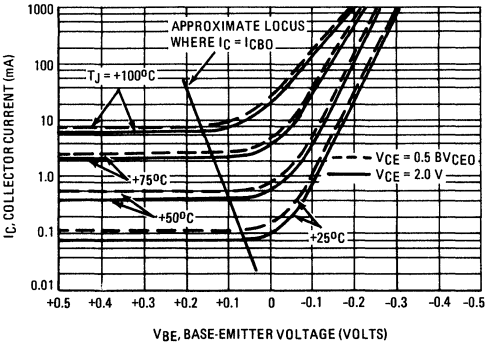


FIGURE 14 – COLLECTOR CUTOFF REGION



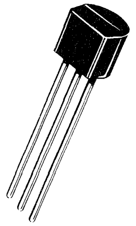
2N6067 (SILICON)

PNP SILICON ANNULAR TRANSISTOR

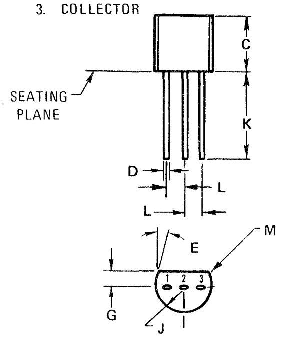
. . . designed for medium-current saturated switching and core driver applications.

- Fast Switching Times @ V_{CC} = 40 Vdc –
  t_{on} = 40 ns (Max)
  t_{off} = 80 ns (Max)
- Current-Gain–Bandwidth Product –
  f_T = 150 MHz (Min) @ I_C = 50 mAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 500 mAdc

PNP SILICON SWITCHING TRANSISTOR



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
C	4.450	4.700	0.175	0.185
D	0.407	0.482	0.016	0.019
E	5° NOM		5° NOM	
G	1.150	1.390	0.045	0.055
J	2.160	2.420	0.085	0.095
K	12.700	–	0.500	–
L	1.270 TP		0.050 TP	
M	0.076	0.330	0.003	0.013

CASE 29-01

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	1.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

*Indicates JEDEC Registered Data

2N6067 (continued)

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

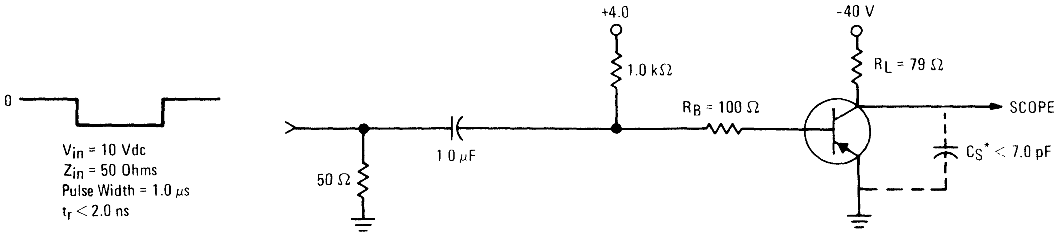
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ① (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	40	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	50	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	500	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
DC Current Gain ①	h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		40	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)		50	200	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		25	150	
Collector-Emitter Saturation Voltage ①	$V_{CE(sat)}$			Vdc
(I_C = 100 mAdc, I_B = 10 mAdc)		–	0.3	
(I_C = 500 mAdc, I_B = 50 mAdc)		–	0.6	
Base-Emitter Saturation Voltage ①	$V_{BE(sat)}$			Vdc
(I_C = 100 mAdc, I_B = 10 mAdc)		–	0.9	
(I_C = 500 mAdc, I_B = 50 mAdc)		0.8	1.1	
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product ② (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	150	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	–	16	pF
Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	80	pF
SWITCHING CHARACTERISTICS				
Turn-On Time (V_{CC} = 40 Vdc, I_C = 500 mAdc, I_{B1} = 50 mAdc, $V_{EB(off)}$ = 4.0 Vdc)	t_{on}	–	40	ns
Delay Time	t_d	–	17	ns
Rise Time	t_r	–	28	ns
Turn-Off Time (V_{CC} = 40 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc)	t_{off}	–	80	ns
Storage Time	t_s	–	70	ns
Fall Time	t_f	–	25	ns

*Indicates JEDEC Registered Data.

①Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

② f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



TYPICAL TRANSIENT CHARACTERISTICS

FIGURE 2 – DELAY TIME

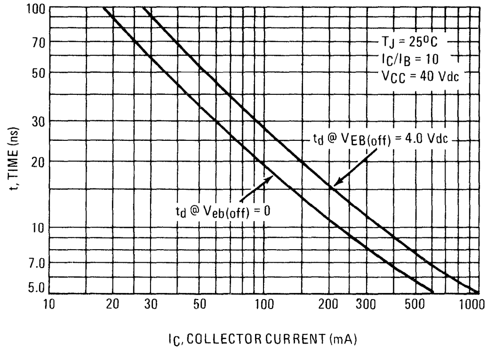


FIGURE 3 – RISE TIME

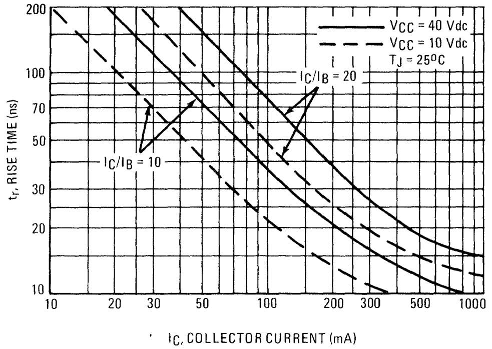


FIGURE 4 – STORAGE TIME

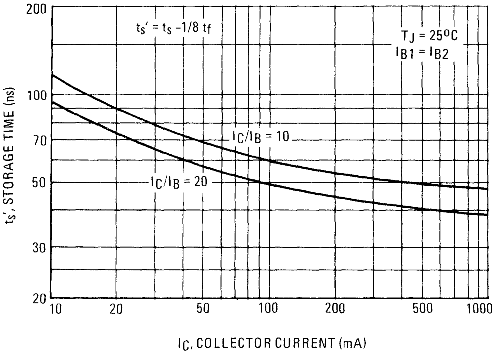


FIGURE 5 – STORAGE TIME CONTOURS

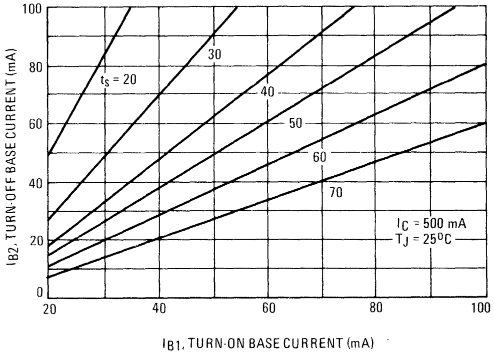


FIGURE 6 – FALL TIME

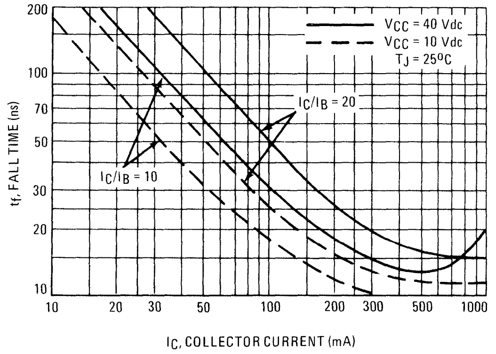
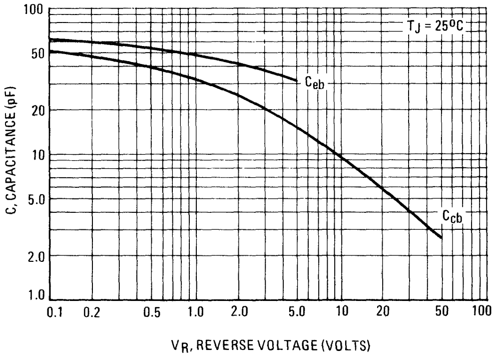


FIGURE 7 – CAPACITANCES



TYPICAL STATIC CHARACTERISTICS

FIGURE 8 – DC CURRENT GAIN

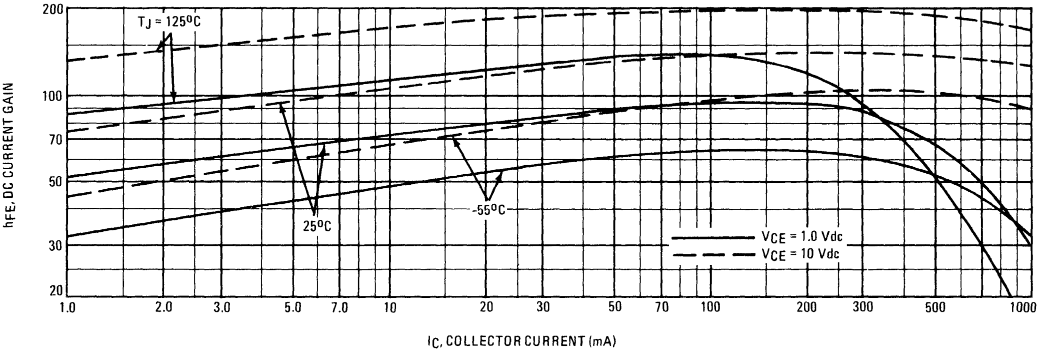


FIGURE 9 – SATURATION REGION

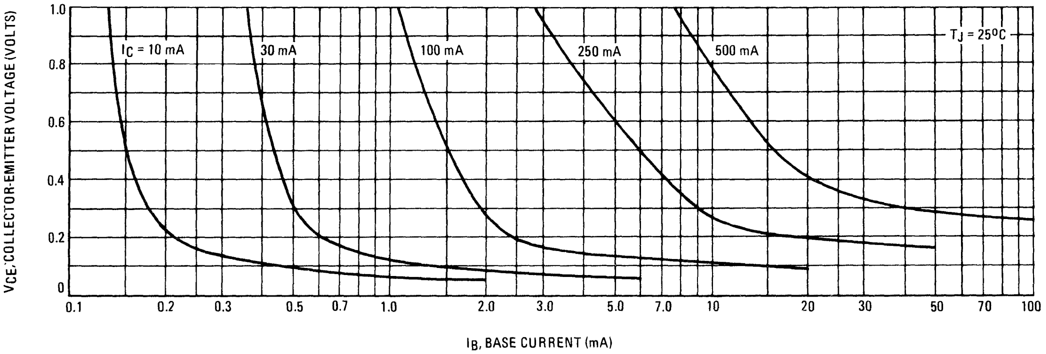


FIGURE 10 – "ON" VOLTAGES

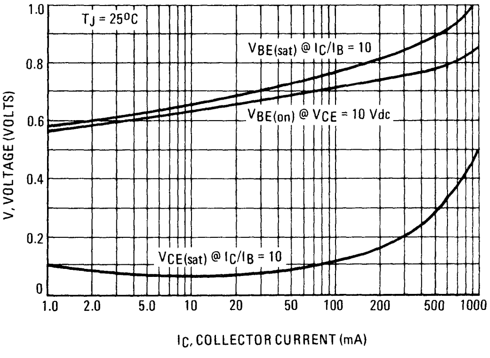
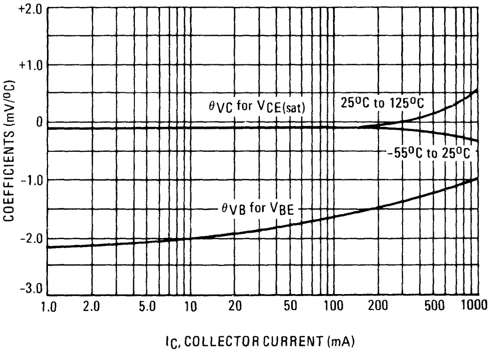


FIGURE 11 – TEMPERATURE COEFFICIENTS



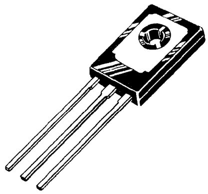
2N6068,A,B (SILICON)
thru
2N6075,A,B

SENSITIVE GATE

TRIACS (THYRISTORS)

4 AMPERES RMS

25 THRU 600 VOLTS



SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Sensitive Gate Triggering (A and B versions) Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions.
- Gate Triggering 2 Mode – 2N6068 thru 2N6075
  4 Mode – 2N6068A,B thru 2N6075A,B
- Blocking Voltages to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
*Repetitive Peak Off-State Voltage, Note 1 (T_J = 110°C)	2N6068,A,B	V_{DRM}	25	Volts
	2N6069,A,B		50	
	2N6070,A,B		100	
	2N6071,A,B		200	
	2N6072,A,B		300	
	2N6073,A,B		400	
	2N6074,A,B		500	
	2N6075,A,B		600	
*On-State Current RMS (T_C = 85°C)		$I_{T(RMS)}$	4.0	Amp
*Peak Surge Current (One Full cycle, 60 Hz, T_J = -40 to +110°C)		I_{TSM}	30	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)		I^2t	3.6	A^2s
*Peak Gate Power		P_{GM}	10	Watts
*Average Gate Power		$P_{G(AV)}$	0.5	Watt
*Peak Gate Voltage		V_{GM}	5.0	Volts
*Operating Junction Temperature Range		T_J	-40 to +110	°C
*Storage Temperature Range		T_{stg}	-40 to +150	°C
Mounting Torque (6-32 Screw), Note 2		–	8.0	in. lb.

THERMAL CHARACTERISTICS

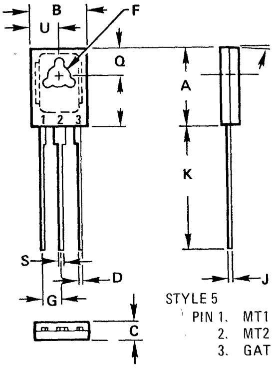
Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R\theta_{JC}$	3.5	°C/W
Thermal Resistance, Case to Ambient	$R\theta_{CA}$	60	°C/W

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.

   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 10 seconds. Consult factory for lead bending options.



STYLE 5
PIN 1. MT1
2. MT2
3. GATE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	11.43	0.390	0.450
B	6.86	8.38	0.270	0.330
C	1.78	3.30	0.070	0.130
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.29 BSC		0.090 BSC	
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
Q	3.30	4.45	0.130	0.175
S	0.64	0.89	0.025	0.035
U	3.81 NOM		0.150 NOM	

CASE 77-02

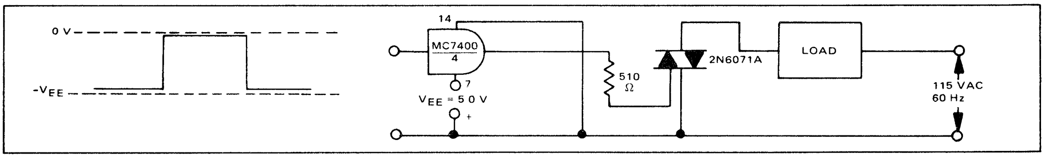
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

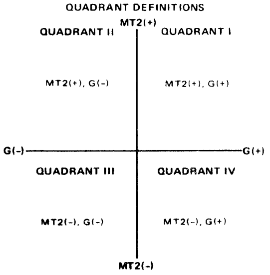
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 6.0 A Peak	V_{TM}	–	–	2.0	Volts
*Peak Gate Trigger Voltage	V_{GTM}				Volts
Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = –40°C					
MT2 (+), G(+); MT2 (-), G(-) All Types		–	1.4	2.5	
MT2 (+), G(-); MT2 (-), G(+) 2N6068A,B thru 2N6075A,B		–	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C					
MT2 (+), G(+); MT2 (-), G(-) All Types		0.2	–	–	
MT2 (+), G(-); MT2 (-), G(+) 2N6068A,B thru 2N6075A,B		0.2	–	–	
*Holding Current (Either Direction)	I_H				mA
Main Terminal Voltage = 12 Vdc, Gate Open, T_J = –40°C Initiating Current = 1.0 Adc					
2N6068 thru 2N6075		–	–	70	
2N6068A,B thru 2N6075A,B		–	–	30	
T_J = 25°C 2N6068 thru 2N6075		–	–	30	
2N6068A,B thru 2N6075A,B		–	–	15	
Turn-On Time (Either Direction) I_{TM} = 14 Adc, I_{GT} = 100 mAdc	t_{on}	–	1.5	–	µs
Blocking Voltage Application Rate at Commutation @ V_{DRM}, T_J = 85°C, Gate Open	dv/dt	–	5.0	–	V/µs

			QUADRANT (See Definition Below)			
	Type	I_{GTM} @ T_J	I mA	II mA	III mA	IV mA
*Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 ohms	2N6068 thru 2N6075	+25°C	30	–	30	–
		-40°C	60	–	60	–
Maximum Value	2N6068A thru 2N6075A	+25°C	5.0	5.0	5.0	10
		-40°C	20	20	20	30
	2N6068B thru 2N6075B	+25°C	3.0	3.0	3.0	5.0
		-40°C	15	15	15	20

*Indicates JEDEC Registered Data.

SAMPLE APPLICATION: TTL-SENSITIVE GATE 4 AMPERE TRIAC TRIGGERS IN MODES II AND III





Trigger devices are recommended for gating on Triacs. They provide

1. Consistent predictable turn-on points
2. Simplified circuitry
3. Fast turn-on time for cooler, more efficient and reliable operation

For 2N6068 Thru 2N6075

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 - 10 V	7.5 - 9.0 V	3.0 - 5.0 V
I_S	350 µA Max	120 µA Max	100 – 400 µA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches

SENSITIVE GATE LOGIC REFERENCE

IC LOGIC FUNCTIONS	FIRING QUADRANT			
	I	II	III	IV
TTL		2N6068A Series	2N6068A Series	
HTL		2N6068A Series	2N6068A Series	
McMOS (NAND)	2N6068B Series			2N6068B Series
McMOS (Buffer)		2N6068B Series	2N6068B Series	
Operational Amplifier	2N6068A Series			2N6068A Series
Zero Voltage Switch		2N6068A Series	2N6068A Series	

FIGURE 1 – AVERAGE CURRENT DERATING

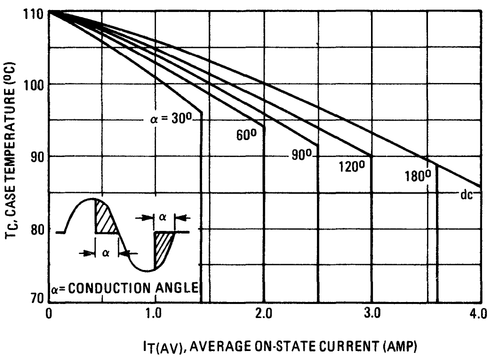


FIGURE 2 – RMS CURRENT DERATING

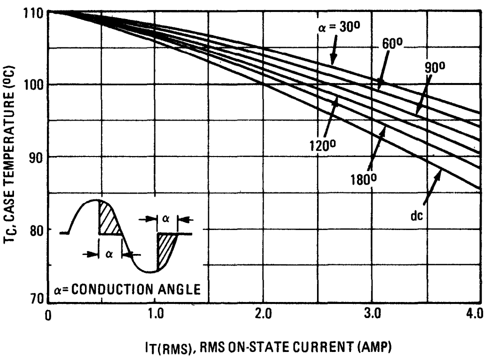


FIGURE 3 – POWER DISSIPATION

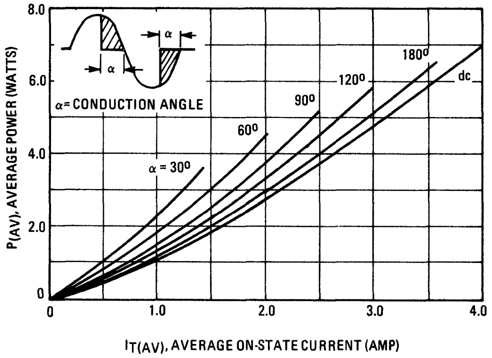


FIGURE 4 – POWER DISSIPATION

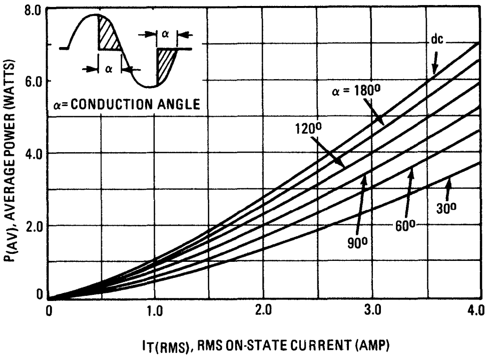


FIGURE 5 – TYPICAL GATE-TRIGGER VOLTAGE

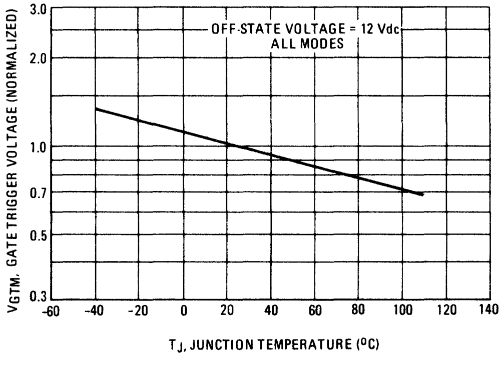


FIGURE 6 – TYPICAL GATE-TRIGGER CURRENT

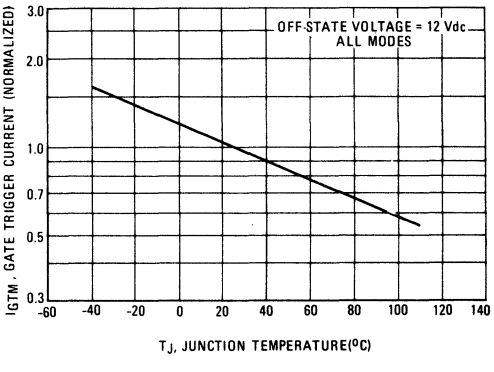


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

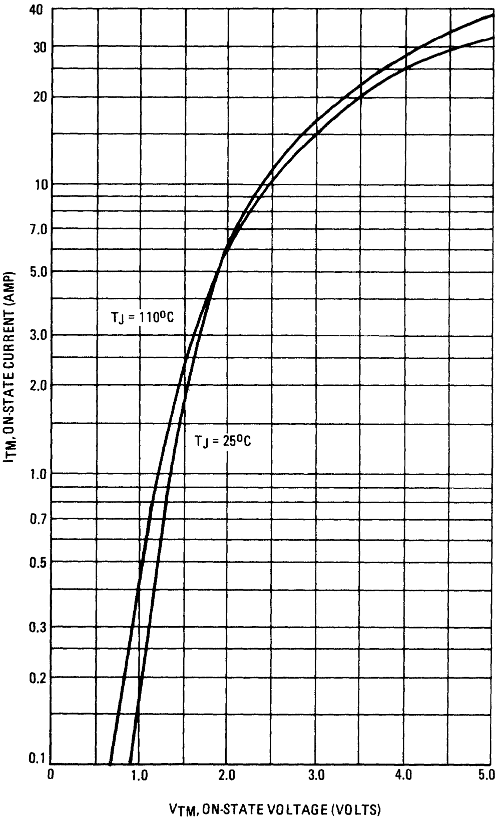


FIGURE 8 – TYPICAL HOLDING CURRENT

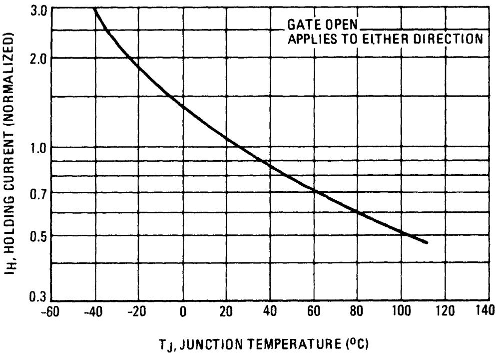


FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

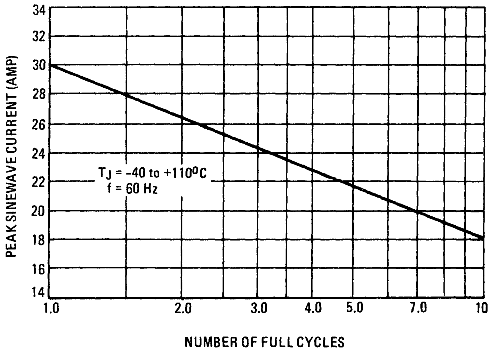
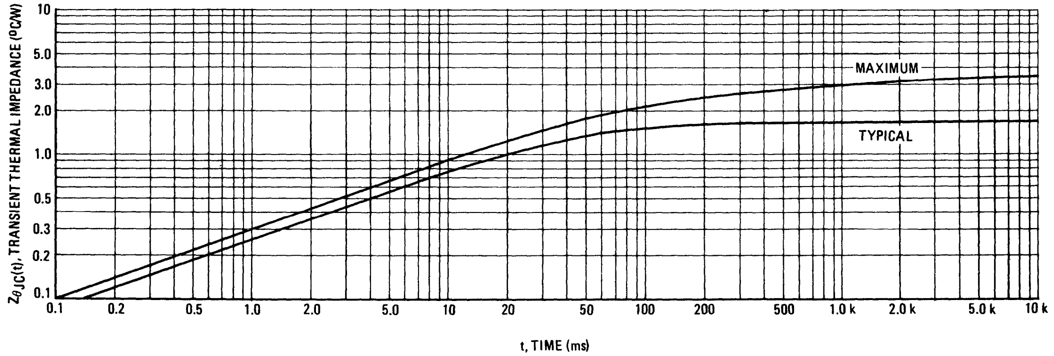


FIGURE 10 – THERMAL RESPONSE



2N6080 (SILICON)

The RF Line

4.0 W – 175 MHz

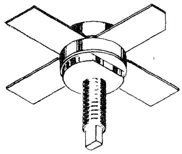
RF POWER
TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt VHF large-signal power amplifier applications required in military and industrial equipment operating to 300 MHz.

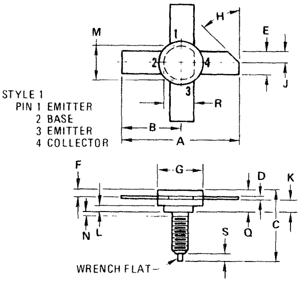
- Specified 12.5 Volt, 175 MHz Characteristics –
  Output Power = 4.0 W
  Minimum Gain = 12 dB
  Efficiency = 50%
- Characterized with Series Equivalent Large-Signal Impedance Parameters



***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	1.0	Adc
Total Device Dissipation @ T_C = 25°C (2) Derate above 25°C	P_D	12 68.5	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C
Stud Torque (1)	–	6.5	in. lb.

*Indicates JEDEC Registered Data.
(1) For repeated assembly use 5 in lb.
(2) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26 79	27 05	1 055	1 065
B	13 20	13 71	520	530
C	18 03	19 05	710	750
D	114	152	0045	006
E	5 59	5 84	220	230
F	2 16	2 41	085	095
G	9 40	9 78	370	385
H	45° NOM		45° NOM	
J	2 79	2 93	110	115
K	4 01	4 52	158	178
L	1 78	2 03	070	080
M	8 13	8 38	320	330
N	–	1 27	–	050
Q	6 35	6 89	250	275
R	7 59	7 80	299	307
S	2 54	3 30	100	130

NOTE
CASE 145A 01 USE 8 32NC2A STUD

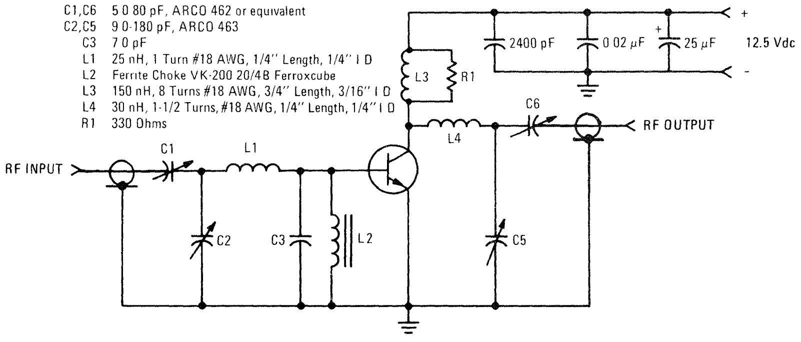
CASE 145A-01

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	BV_{CES}	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = +55°C)	I_{CES}	–	–	5.0	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.25 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	15	20	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 4.0 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	G_{PE}	12	–	–	dB
Collector Efficiency (P_{out} = 4.0 W, V_{CC} = 12.5 Vdc, f - 175 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data.

FIGURE 1 – 175 MHz TEST CIRCUIT



C1,C6	5 0 80 pF, ARCO 462 or equivalent
C2,C5	9 0-180 pF, ARCO 463
C3	7 0 pF
L1	25 nH, 1 Turn #18 AWG, 1/4" Length, 1/4" I D
L2	Ferrite Choke VK-200 20/4B Ferroxcube
L3	150 nH, 8 Turns #18 AWG, 3/4" Length, 3/16" I D
L4	30 nH, 1-1/2 Turns, #18 AWG, 1/4" Length, 1/4" I D
R1	330 Ohms

FIGURE 2 – OUTPUT POWER versus INPUT POWER

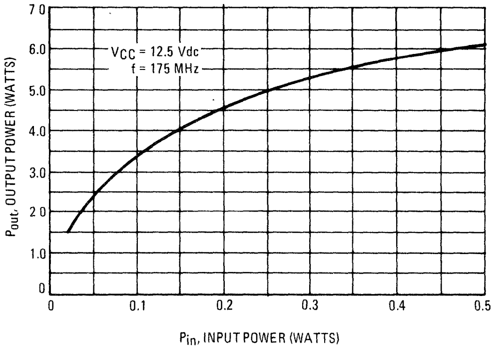


FIGURE 3 – OUTPUT POWER versus FREQUENCY

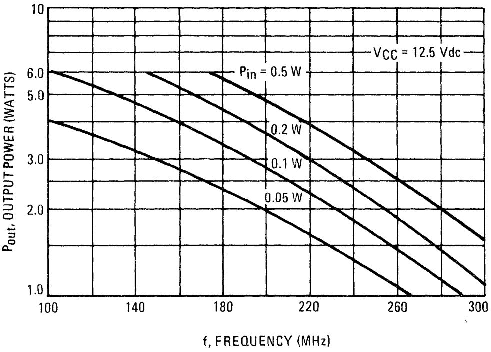


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

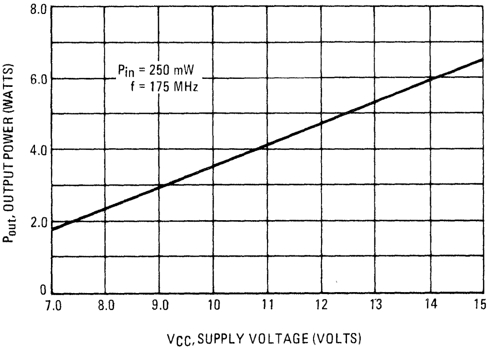
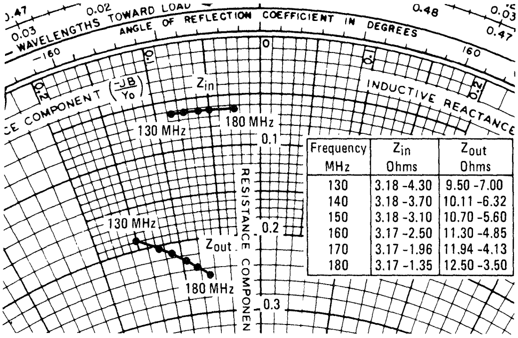


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{in} Ohms	Z_{out} Ohms
130	3.18 -4.30	9.50 -7.00
140	3.18 -3.70	10.11 -6.32
150	3.18 -3.10	10.70 -5.60
160	3.17 -2.50	11.30 -4.85
170	3.17 -1.96	11.94 -4.13
180	3.17 -1.35	12.50 -3.50

2N6081 (SILICON)
MRF211

The RF Line

NPN SILICON RF POWER TRANSISTORS

. . . designed for 12.5 Volt VHF large-signal power amplifier applications required in commercial and industrial equipment operating to 300 MHz.

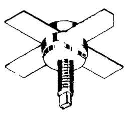
- Specified 12.5 Volt, 175 MHz Characteristics –
  Output Power = 15 W
  Minimum Gain = 6.3 dB
  Efficiency = 60%
- Characterized with Series Equivalent Large-Signal Impedance Parameters

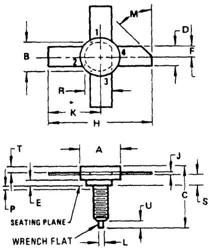
15 W – 175 MHz

RF POWER
TRANSISTORS

NPN SILICON

2N6081





STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	18.03	19.05	0.710	0.750
D	5.59	5.84	0.220	0.230
E	1.78	2.03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130

NOTE
CASE 145A 01 USE 8 32NC2A STUD

CASE 145A-01

*MAXIMUM RATINGS

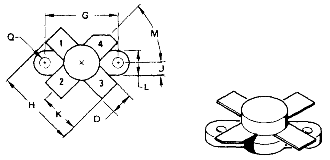
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	2.5	Adc
Total Device Dissipation @ $T_C = 25^{\circ}C$ (1) Derate above 25°C	P_D	31 177	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C
Stud Torque (2)	–	6.5	in. lb.

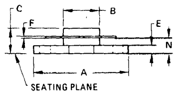
*Indicates JEDEC Registered Data for 2N6081.

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) For repeated assembly use 5 in. lb.

MRF221





STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.64	24.89	0.970	0.980
B	9.47	9.73	0.373	0.383
C	6.07	7.14	0.239	0.281
D	5.59	5.84	0.220	0.230
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	21.59	22.10	0.850	0.870
J	3.12	3.23	0.123	0.127
K	10.80	11.05	0.425	0.435
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.97	3.12	0.117	0.123

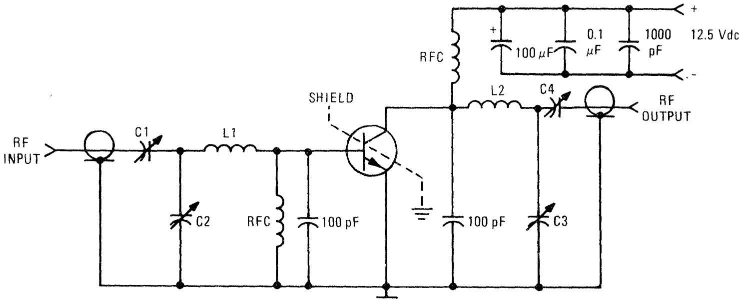
CASE 211-01

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	BV_{CEO}	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, V_{BE} = 0)	BV_{CES}	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = +55°C)	I_{CES}	–	–	8.0	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	70	85	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 15 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	G_{PE}	6.3	–	–	dB
Collector Efficiency (P_{out} = 15 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	η	60	–	–	%

*Indicates JEDEC Registered Data for 2N6081.

FIGURE 1 — 175 MHz TEST CIRCUIT



C1,2,3,4 5 0-80 pF ARCO 462
L1 Straight Wire, #14 AWG, 1-3/8" Long
L2 1 Turn, #14 AWG, 3/8" ID, Length Plus Leads = 1"
RFC VK200-20/4B, FERROXCUBE.

FIGURE 2 – OUTPUT POWER versus INPUT POWER

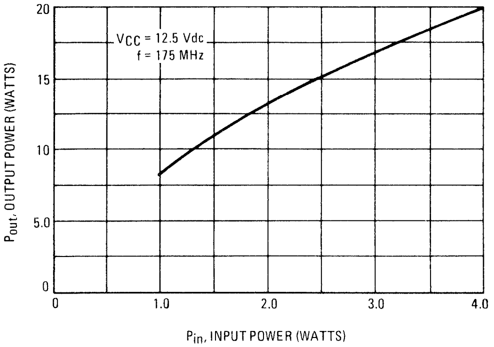


FIGURE 3 – OUTPUT POWER versus FREQUENCY

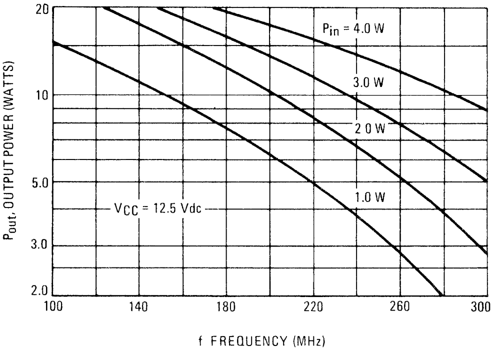


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

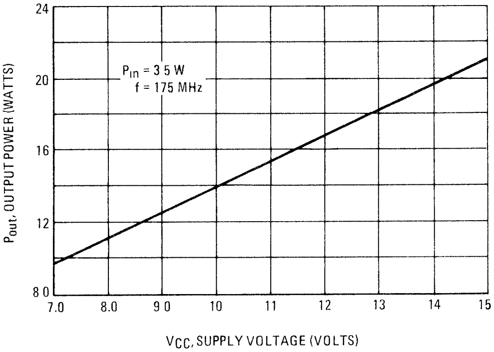
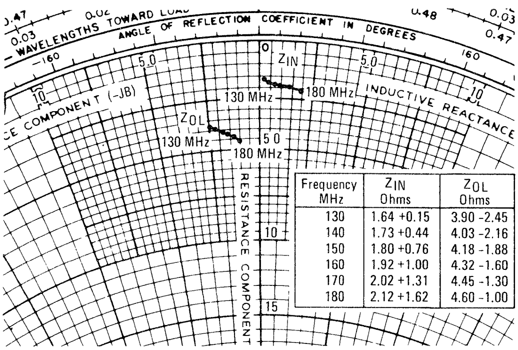


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{IN} Ohms	Z_{OL} Ohms
130	1.64 +0.15	3.90 -2.45
140	1.73 +0.44	4.03 -2.16
150	1.80 +0.76	4.18 -1.88
160	1.92 +1.00	4.32 -1.60
170	2.02 +1.31	4.45 -1.30
180	2.12 +1.62	4.60 -1.00

2N6082, 2N6083, 2N6084 (SILICON)

The RF Line

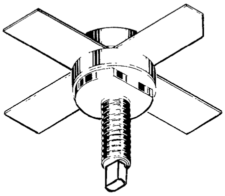
NPN SILICON RF POWER TRANSISTORS

. . . designed for 12.5 Volt VHF large-signal power amplifier applications required in military and industrial equipment operating to 225 MHz.

- Specified 12.5 Volt, 175 MHz Characteristics –
  Output Power = 25 W – 2N6082
  30 W – 2N6083
  40 W – 2N6084
  Minimum Gain = 6.2 dB – 2N6082
  5.7 dB – 2N6083
  4.5 dB – 2N6084
- Balanced Emitter Construction to provide the designer with the device technology that assures ruggedness and resists transistor damage caused by load mismatch

25, 30 and 40 W
175 MHz

RF POWER
TRANSISTORS
NPN SILICON



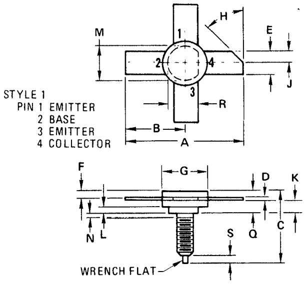
*MAXIMUM RATINGS

Rating	Symbol	2N6082 2N6083	2N6084	Unit
Collector-Emitter Voltage	V_{CEO}	18		Vdc
Collector-Base Voltage	V_{CBO}	36		Vdc
Emitter-Base Voltage	V_{EBO}	4.0		Vdc
Collector Current – Continuous	I_C	4.0	6.0	Adc
Total Device Dissipation @ $T_C = 75^{\circ}C$(2) Derate above 25°C	P_D	65 0.52	80 0.64	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +200		°C
Stud Torque(1)	–	6.5		in. lb.

*Indicates JEDEC Registered Data

(1)For Repeated Assembly Use 5 in. lb.

(2)These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.



STYLE 1
PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	26 79	27 05	1 055	1 065
B	13 20	13 71	520	530
C	18 03	19 05	710	750
D	114	152	0045	006
E	5 59	5 84	220	230
F	2 16	2 41	085	095
G	9 40	9 78	370	.385
H	45° NOM		45° NOM	
J	2 79	2 93	110	.115
K	4 01	4 52	158	178
L	1 78	2 03	.070	080
M	8 13	8 38	320	330
N	–	1 27	–	050
Q	6 35	6 89	250	275
R	7 59	7 80	299	.307
S	2 54	3 30	100	130

NOTE
CASE 145A-01 USE 8-32NC2A STUD

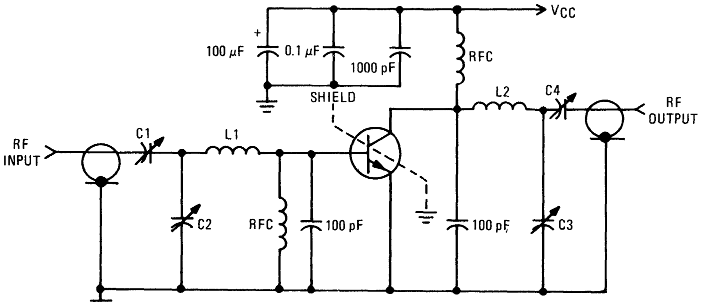
CASE 145A-01

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)		BV_{CEO}	18	–	–	Vdc
Collector-Emitter Breakdown Voltage		BV_{CES}				Vdc
(I_C = 15 mAdc, V_{BE} = 0)	2N6082,2N6083		36	–	–	
(I_C = 20 mAdc, V_{BE} = 0)	2N6084		36	–	–	
Emitter-Base Breakdown Voltage		BV_{EBO}				Vdc
(I_E = 5.0 mAdc, I_C = 0)	2N6082,2N6083		4.0	–	–	
(I_E = 10 mAdc, I_C = 0)	2N6084		4.0	–	–	
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = +55°C)		I_{CES}	–	–	10	mAdc
Collector Cutoff Current		I_{CBO}				mAdc
(V_{CB} = 15 Vdc, I_E = 0)	2N6082,2N6083		–	–	1.0	
	2N6084		–	–	2.5	
ON CHARACTERISTICS						
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS						
Output Capacitance		C_{ob}				pF
(V_{CB} = 15 Vdc, I_E = 0, f = 0.1 MHz)	2N6082,2N6083		–	110	130	
	2N6084		–	170	200	
FUNCTIONAL TEST						
Common-Emitter Amplifier Power Gain		G_{PE}				dB
(P_{out} = 25 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	2N6082		6.2	–	–	
(P_{out} = 30 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	2N6083		5.7	–	–	
(P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	2N6084		4.5	–	–	
Collector Efficiency		η				%
(P_{out} = 25 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	2N6082		65	–	–	
(P_{out} = 30 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	2N6083		65	–	–	
(P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	2N6084		70	–	–	

*Indicates JEDEC Registered Data

FIGURE 1 – 175 MHz TEST CIRCUIT



C1,2,3,4 5.0-80 pF ARCO 462
L1 Straight Wire, #14 AWG, 1-3/8" Long
L2 1 Turn, #14 AWG, 3/8" ID, Length Plus Leads = 1"
RFC VK200-20/4B, FERROXCUBE.

OUTPUT POWER versus INPUT POWER

FIGURE 2 – 2N6082, 2N6083

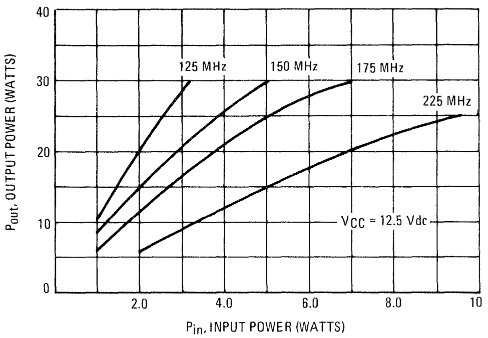
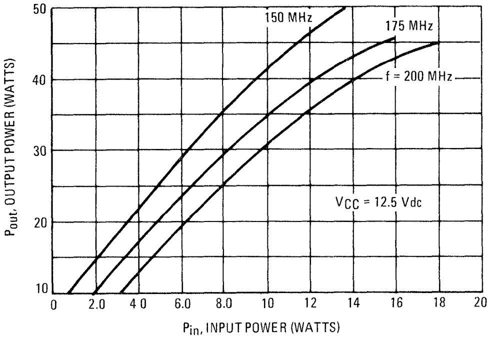


FIGURE 3 – 2N6084



OUTPUT POWER versus SUPPLY VOLTAGE

FIGURE 4 – 2N6082, 2N6083

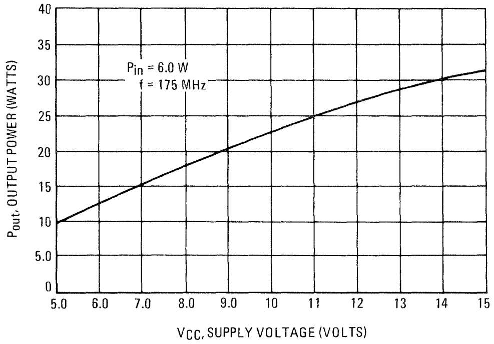
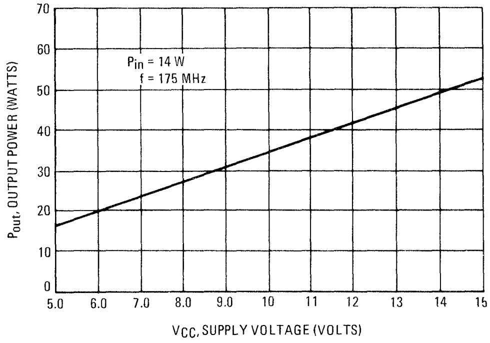


FIGURE 5 – 2N6084



PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

FIGURE 6 – 2N6082, 2N6083

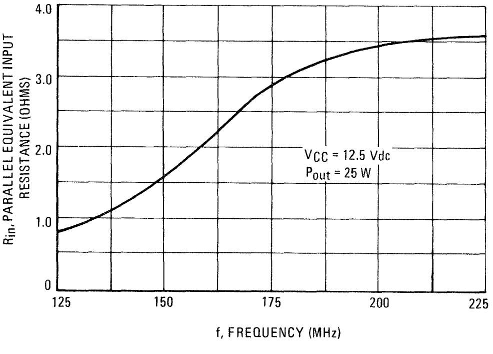
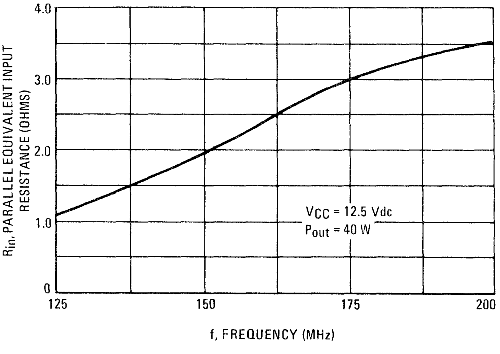


FIGURE 7 – 2N6084



PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

FIGURE 8 – 2N6082, 2N6083

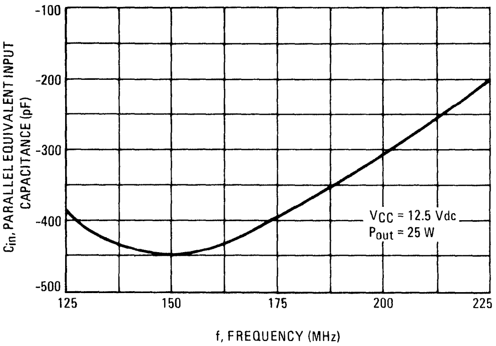
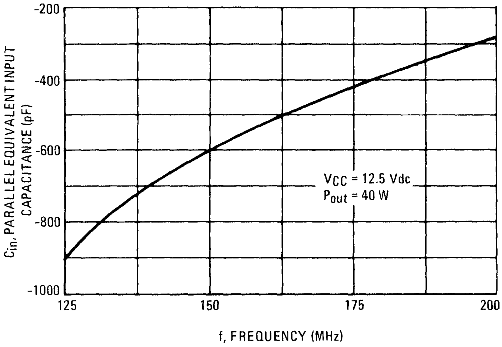


FIGURE 9 – 2N6084



PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

FIGURE 10 – 2N6082, 2N6083

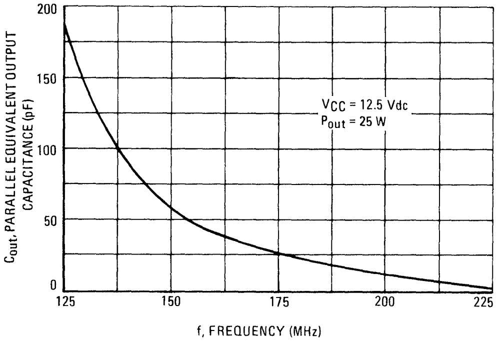
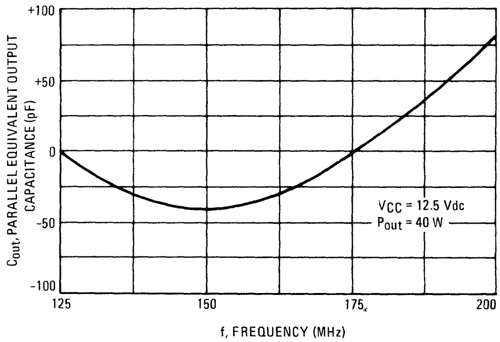


FIGURE 11 – 2N6084



TYPICAL 175 MHz AMPLIFIER BLOCK DIAGRAMS

FIGURE 12 – 160 WATTS OUTPUT

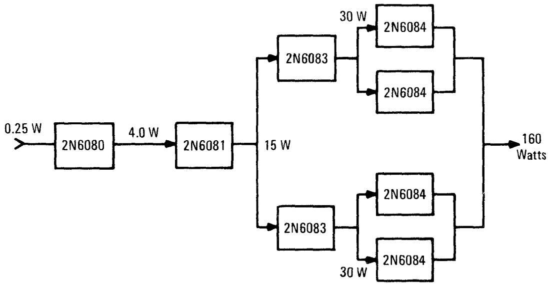
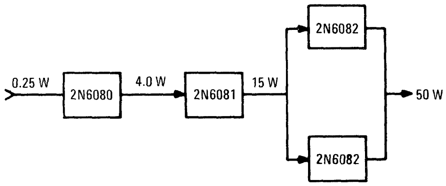


FIGURE 13 – 50 WATTS OUTPUT



2N6094 thru 2N6097 (SILICON)

The RF Line

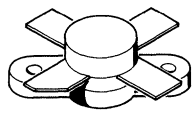
PNP SILICON RF POWER TRANSISTORS

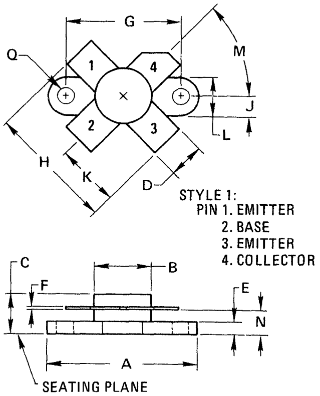
. . . designed for 12.5 Volt VHF large-signal amplifier applications required in military and industrial equipment operating to 250 MHz.

- Balanced Emitter Construction with Isothermal Resistor Design to Provide the Designer with the Optimum in Transistor Ruggedness
- Low Lead Inductance Stripline Packaging for Easier Design and Increased Broadband Capabilities
- Flange Package for Easy Mounting and Better Thermal Conductivity to Heat Sink
- Exceptional Power Output Stability versus Temperature

4.0, 15, 30, 40 WATTS - 175 MHz

**PNP SILICON
RF POWER
TRANSISTORS**





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.64	24.89	0.970	0.980
B	9.47	9.73	0.373	0.383
C	6.07	7.14	0.239	0.281
D	5.59	5.84	0.220	0.230
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	21.59	22.10	0.850	0.870
J	3.12	3.23	0.123	0.127
K	10.80	11.05	0.425	0.435
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.97	3.12	0.117	0.123

CASE 211-01

*MAXIMUM RATINGS

Rating	Symbol	2N6094	2N6095	2N6096	2N6097	Unit
Collector-Emitter Voltage	V_{CEO}	← 18 →				Vdc
Collector-Base Voltage	V_{CBO}	← 36 →				Vdc
Emitter-Base Voltage	V_{EBO}	← 4.0 →				Vdc
Collector Current – Continuous	I_C	1.0	2.5	4.0	6.0	Adc
Total Device Dissipation @ $T_C = 25^{\circ}C$	P_D(1)	8.0	20	40	60	Watts
Derate above 25°C		45.7	114	228	343	mW/°C
Storage Temperature Range	T_{stg}	← -65 to +200 →				°C

*Indicates JEDEC Registered Data.

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

OFF CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Collector-Emitter Breakdown Voltage		BV_{CEO}				Vdc
(I_C = 10 mAdc, I_B = 0)	2N6094		18	–	–	
(I_C = 20 mAdc, I_B = 0)	2N6095		18	–	–	
(I_C = 50 mAdc, I_B = 0)	2N6096		18	–	–	
(I_C = 100 mAdc, I_B = 0)	2N6097		18	–	–	
Collector Emitter Breakdown Voltage		BV_{CES}				Vdc
(I_C = 5.0 mAdc, V_{BE} = 0)	2N6094		36	–	–	
(I_C = 10 mAdc, V_{BE} = 0)	2N6095		36	–	–	
(I_C = 15 mAdc, V_{BE} = 0)	2N6096		36	–	–	
(I_C = 20 mAdc, V_{BE} = 0)	2N6097		36	–	–	
Emitter-Base Breakdown Voltage		BV_{EBO}				Vdc
(I_E = 1.0 mAdc, I_C = 0)	2N6094		4.0	–	–	
(I_E = 2.0 mAdc, I_C = 0)	2N6095		4.0	–	–	
(I_E = 5.0 mAdc, I_C = 0)	2N6096		4.0	–	–	
(I_E = 10 mAdc, I_C = 0)	2N6097		4.0	–	–	
Collector Cutoff Current		I_{CES}				mAdc
(V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 55°C)	2N6094		–	–	5.0	
	2N6095		–	–	8.0	
	2N6096		–	–	10	
	2N6097		–	–	10	
Collector Cutoff Current		I_{CBO}				
(V_{CB} = 15 Vdc, I_E = 0)	2N6094		–	–	250	µAdc
	2N6095		–	–	500	
	2N6096		–	–	1.0	mAdc
	2N6097		–	–	2.5	

ON CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
DC Current Gain		h_{FE}				–
(I_C = 0.25 Adc, V_{CE} = 5.0 Vdc)	2N6094		5.0	–	–	
(I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	2N6095,2N6096,2N6097		15	–	–	

DYNAMIC CHARACTERISTICS

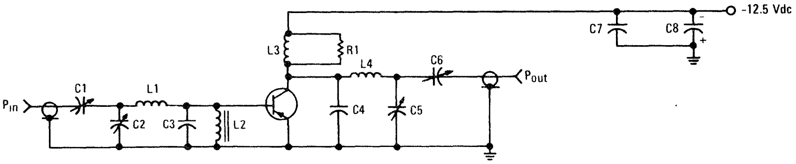
Characteristic		Symbol	Min	Typ	Max	Unit
Output Capacitance		C_{ob}				pF
(V_{CB} = 12.5 Vdc, I_E = 0, f = 100 kHz)	2N6094		–	17	20	
	2N6095		–	90	120	
	2N6096		–	150	190	
	2N6097		–	300	400	

FUNCTIONAL TEST

Characteristic		Symbol	Min	Typ	Max	Unit
Common-Emitter Amplifier Power Gain (Figure 1)		G_{PE}				dB
(P_{out} = 4.0 W, V_{CC} = 12.5 Vdc, I_C(max) = 0.62 Adc, f = 175 MHz)	2N6094		12	–	–	
(P_{out} = 15 W, V_{CC} = 12.5 Vdc, I_C(max) = 1.9 Adc, f = 175 MHz)	2N6095		6.3	–	–	
(P_{out} = 30 W, V_{CC} = 12.5 Vdc, I_C(max) = 3.4 Adc, f = 175 MHz)	2N6096		5.7	–	–	
(P_{out} = 40 W, V_{CC} = 12.5 Vdc, I_C(max) = 4.3 Adc, f = 175 MHz)	2N6097		4.5	–	–	
Collector Efficiency (Figure 1)		η				%
(P_{out} = 4.0 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	2N6094		50	–	–	
(P_{out} = 15 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	2N6095		55	–	–	
(P_{out} = 30 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	2N6096		60	–	–	
(P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	2N6097		60	–	–	

*Indicates JEDEC Registered Data

FIGURE 1 — 175 MHz TEST CIRCUIT



2N6094

C1,C2	ARCO 462 or Equivalent
C3,C4	7.0 pF Unelco J1HF
C5	ARCO 463 or Equivalent
C6	ARCO 461 or Equivalent
C7	1000 pF
C8	5.0 μF, 50 V
L1	25 nH, 1 Turn, #18 AWG, 1-1/4" Long, 1/4" I.D.
L2	VK200 20/4B Ferrite Choke, Ferroxcube
L3	150 nH, 8 Turns, #18 AWG, 3/4" Long, 3/16" I.D
L4	36 nH, 1-1/2 Turns, #18 AWG, 1-1/4" Long, 1/4" I.D.
R1	390 Ohms, 1/2 W

2N6095

C1,C6	ARCO 462 or Equivalent
C2	ARCO 464 or Equivalent
C3,C4	40 pF Unelco J1HF
C5	ARCO 463 or Equivalent
C7	1000 pF
C8	5.0 μF, 50 V
L1	Copper Strap 1/4" Wide, 1-1/4" Long, Straight
L2	VK200 20/4B Ferrite Choke, Ferroxcube
L3	150 nH, 4 Turns, #18 AWG, 3/4" Long, Wound on R1
L4	1 Turn, #18 AWG, 1-1/4" Long, 1/4" I.D
R1	390 Ohms, 1 W

2N6096

C1,C2	ARCO 462 or Equivalent
C3,C4	100 pF Unelco J1HF
C5,C6	ARCO 463 or Equivalent
C7	1000 pF
C8	5.0 μF, 50 V
L1	1/2 Turn, #16 AWG, 1-1/4" Long, 1/4" I.D.
L2	VK200 20/4B Ferrite Choke, Ferroxcube
L3	4 Turns, #18 AWG, 3/4" Long, Wound on R1
L4	1 Turn, #16 AWG, 1-1/4" Long, 1/4" I.D
R1	390 Ohms, 2 W

2N6097

C1,C2,C5	ARCO 462 or Equivalent
C6	ARCO 464 or Equivalent
C3,C4	100 pF Unelco J1HF
C7	1000 pF
C8	5.0 μF, 50 V
L1	18 nH, 1-1/4" Straight, #16 AWG
L2	VK200 20/4B Ferrite Choke, Ferroxcube
L3	5 Turns, #18 AWG, 3/4" Long, Wound on R1
L4	1 Turn, #18 AWG, 1-1/4" Long, 1/4" I.D.
R1	160 Ohms, 2 W

OUTPUT POWER versus FREQUENCY

(V_{CC} = -12.5 Vdc)

FIGURE 2 — 2N6094

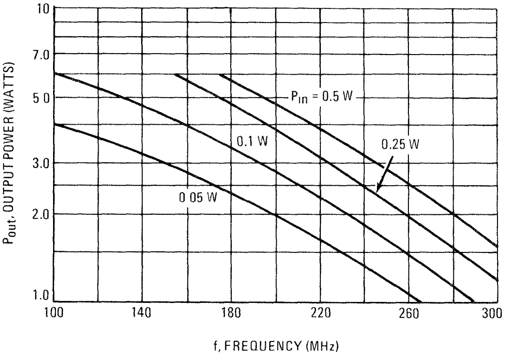


FIGURE 3 — 2N6095

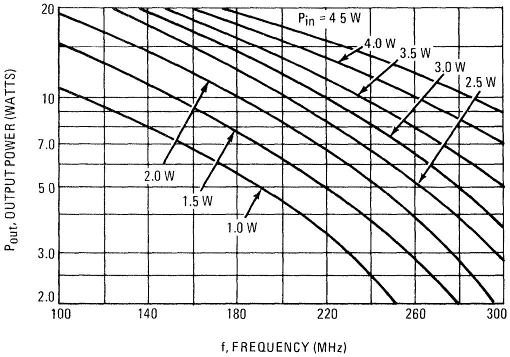


FIGURE 4 — 2N6096

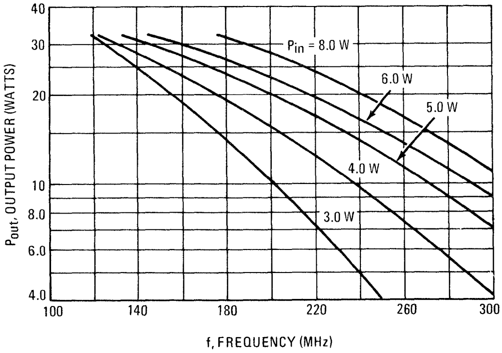
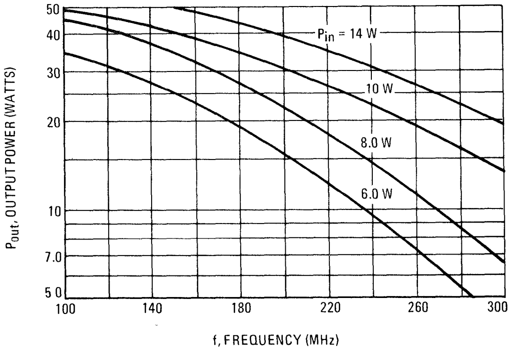


FIGURE 5 — 2N6097



TYPICAL PERFORMANCE DATA

OUTPUT POWER versus INPUT POWER

(V_{CC} = -12.5 Vdc, f = 175 MHz)

FIGURE 6 – 2N6094

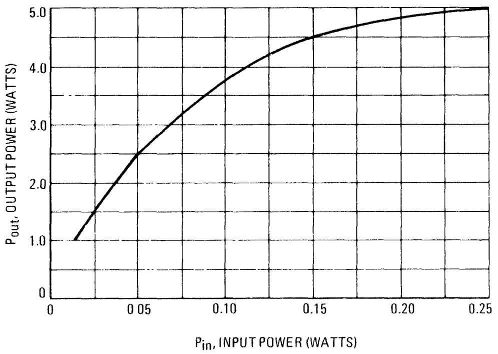


FIGURE 7 – 2N6095

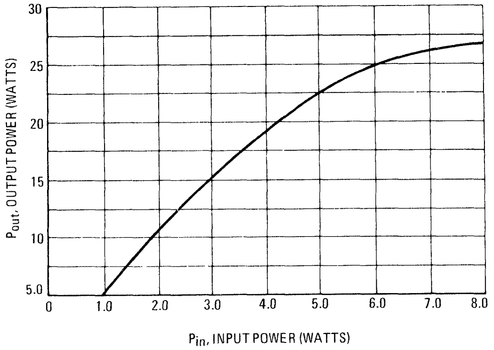


FIGURE 8 – 2N6096

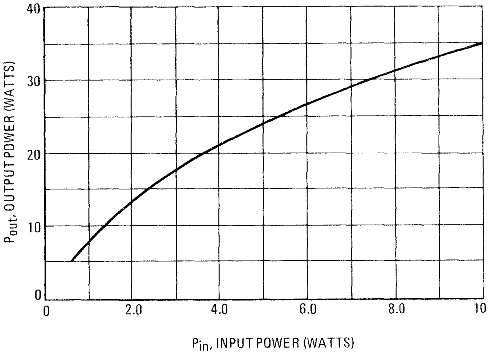
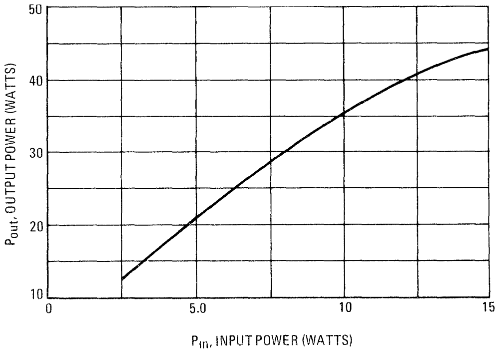


FIGURE 9 – 2N6097



CIRCUIT DESIGN DATA

OUTPUT POWER versus SUPPLY VOLTAGE

(f = 175 MHz)

FIGURE 10 – 2N6094

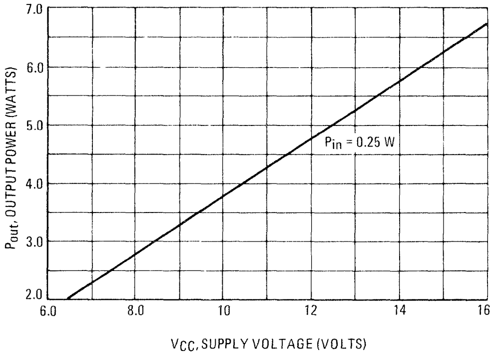
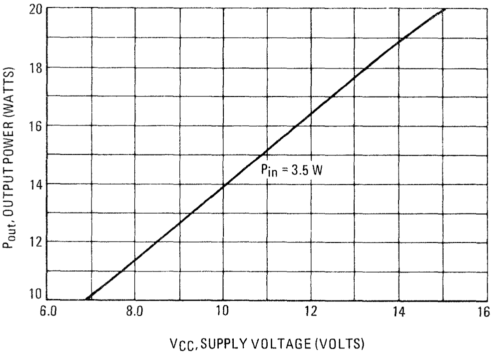


FIGURE 11 – 2N6095



CIRCUIT DESIGN DATA

OUTPUT POWER versus SUPPLY VOLTAGE

(f = 175 MHz)

FIGURE 12 – 2N6096

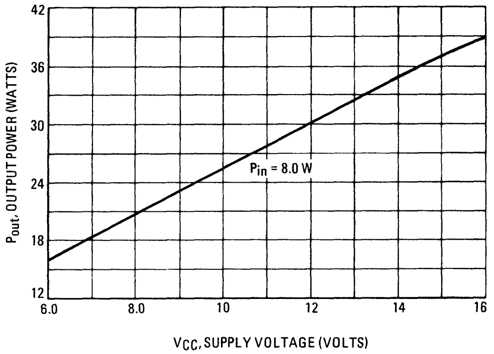
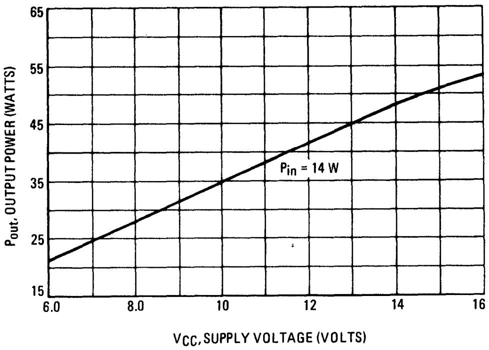


FIGURE 13 – 2N6097



PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

(V_{CC} = -12.5 Vdc)

FIGURE 14 – 2N6094

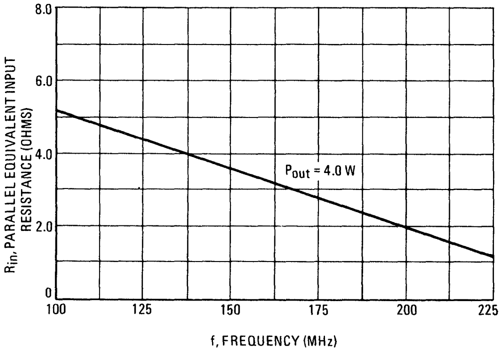


FIGURE 15 – 2N6095

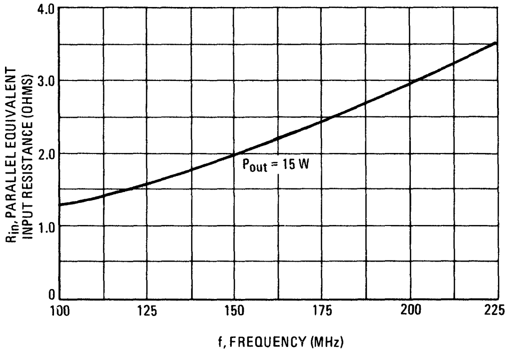


FIGURE 16 – 2N6096

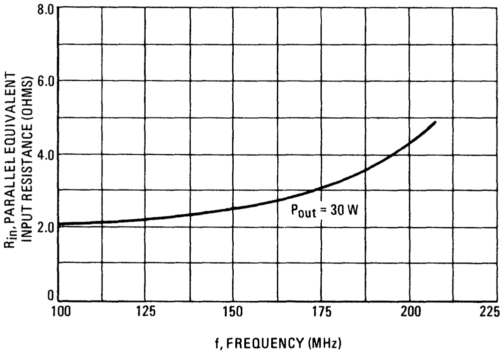
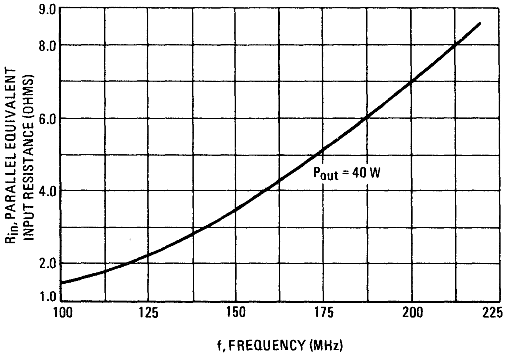


FIGURE 17 – 2N6097



CIRCUIT DESIGN DATA

PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

(V_{CC} = -12.5 Vdc)

FIGURE 18 — 2N6094

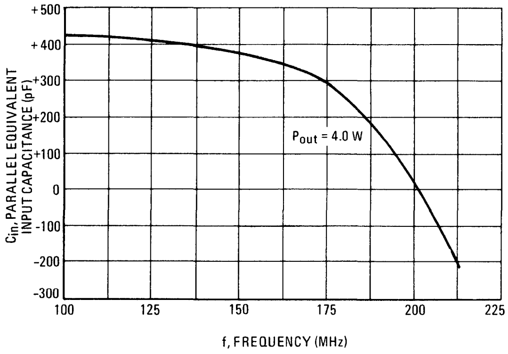


FIGURE 19 — 2N6095

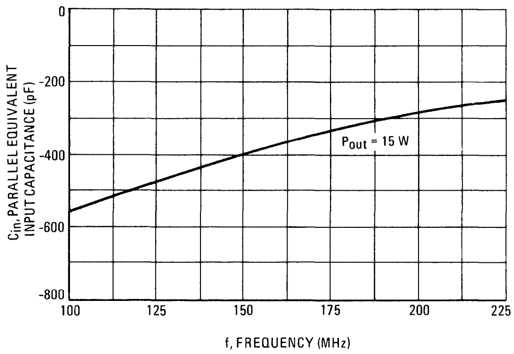


FIGURE 20 — 2N6096

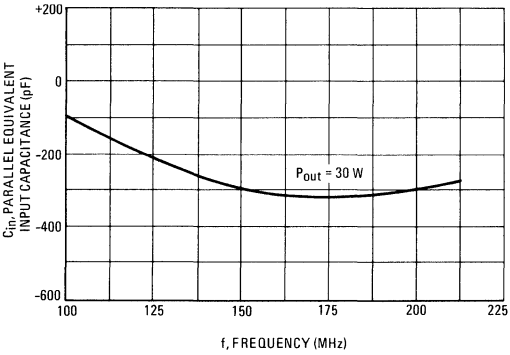
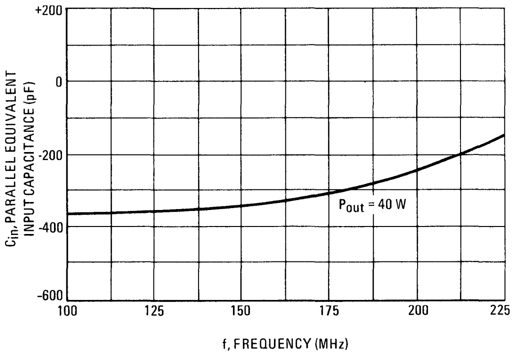


FIGURE 21 — 2N6097



PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

(V_{CC} = -12.5 Vdc)

FIGURE 22 — 2N6094

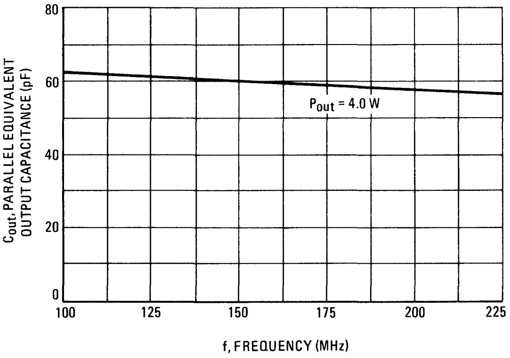
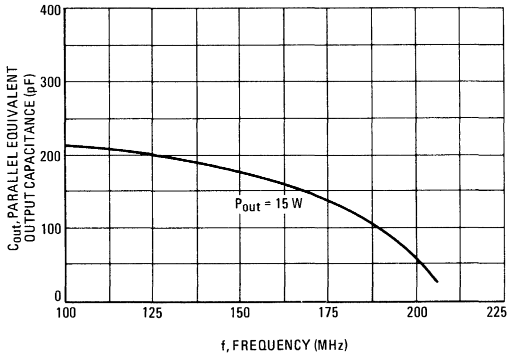


FIGURE 23 — 2N6095



CIRCUIT DESIGN DATA

PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

(V_{CC} = -12.5 Vdc)

FIGURE 24 – 2N6096

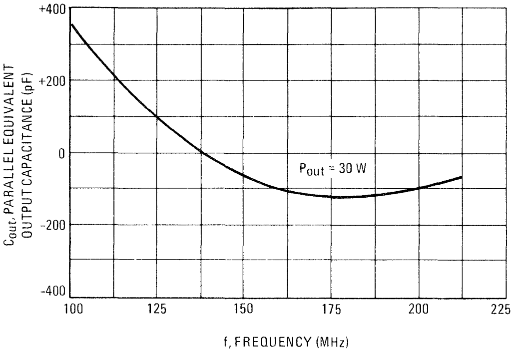
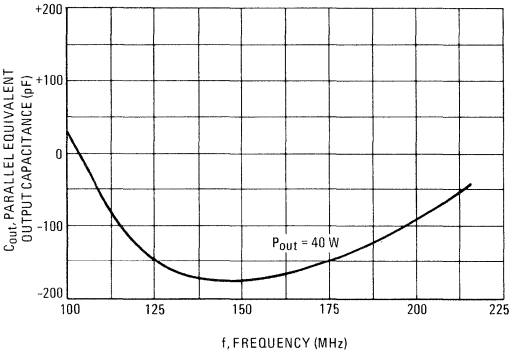


FIGURE 25 – 2N6097



TYPICAL OUTPUT POWER versus STUD TEMPERATURE

(V_{CC} = -12.5 Vdc, f = 175 MHz)

FIGURE 26 – 2N6094

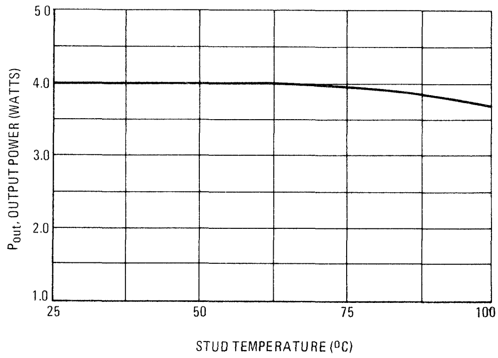


FIGURE 27 – 2N6095

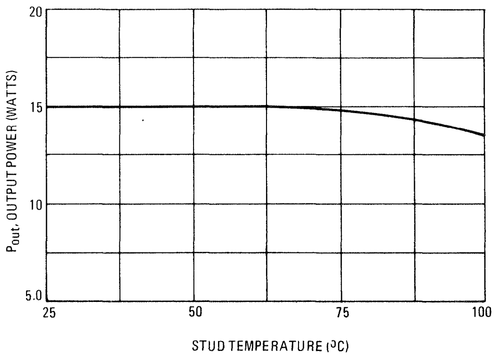


FIGURE 28 – 2N6096

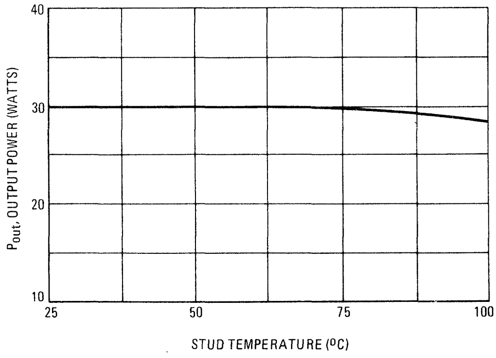
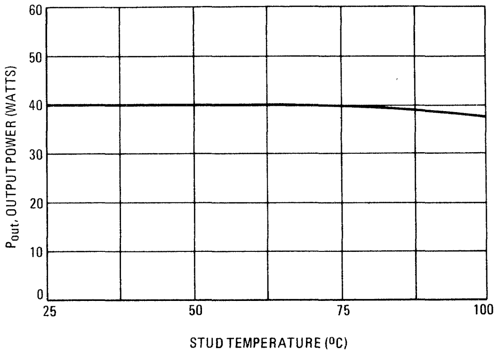


FIGURE 29 – 2N6097



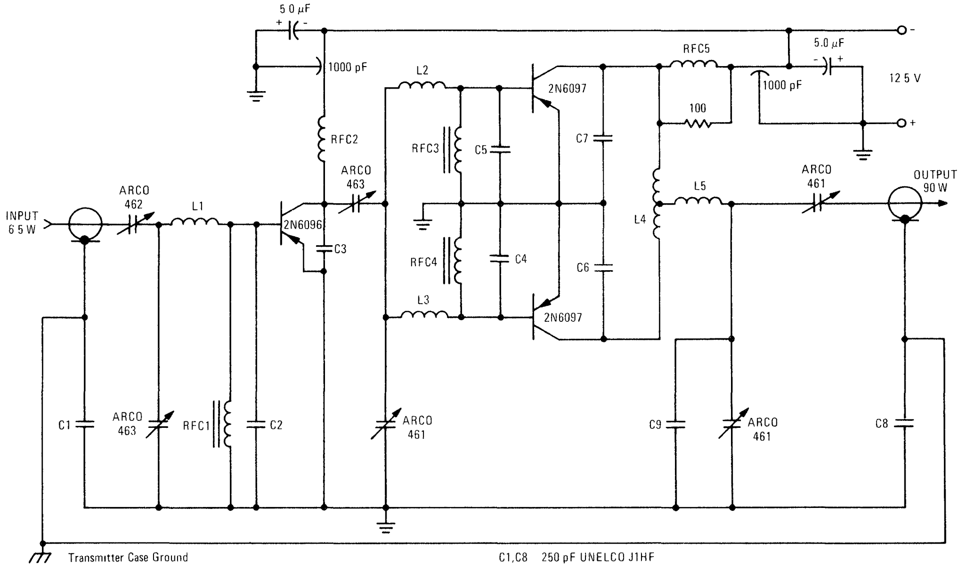


FIGURE 30 – 90-WATT, 175 MHz AMPLIFIER

C1,C8	250 pF UNELCO J1HF
C2,C3,C4,C5,C6,C7	100 pF UNELCO J1HF
C9	25 pF UNELCO J1HF
RFC1	VK200 – 20/4B Ferroxcube
RFC2	4 Turns, #18 AWG, L + Leads 1-1/2", 1/4" I D
RFC3, RFC4	0 15 μH Molded with Ferrite Bead on Ground Leg
RFC5	3 Turns, #16 AWG, on 2 W, 100 Ω Resistor
L1	1 Turn, #20 AWG, 1/4" I.D
L2, L3	ST PC , #18 AWG, 1-1/4" L
L4	1-1/4" x 1/4" x 0.03" Copper Strap Center Tapped
L5	1/2 Turn, #16 AWG, 1/4" I D., 1/2" L

This is an example of a PNP amplifier designed for negative or positive ground operation. Floating the coaxial connectors with bypasses causes no gain loss. The chassis material is Printed Circuit Board which may easily be isolated from the transmitter cabinet.

2N6114 (SILICON)
2N6115

SILICON COMPLEMENTARY UNIJUNCTION TRANSISTORS

. . . designed for oscillators, timers, frequency dividers and trigger circuits which require stability over wide temperature ranges.

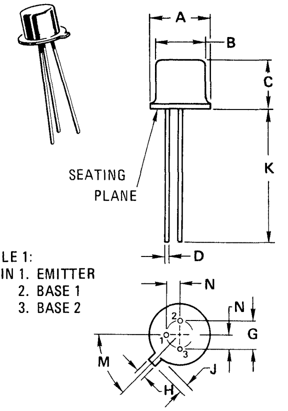
- Interbase Resistance Temperature Coefficient –
  αR_{BB} = 0.05 (Min) to 0.5 (Max) %/°C
- Low Leakage Current –
  I_{EB2O} = 0.1 nA (Typ)
- Low Saturation Voltage –
  $V_{EB1(sat)}$ = 1.5 Vdc (Max)
- Instrinsic Standoff Ratio –
  η = 0.58 (Min) to 0.62 (Max)

***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Emitter Current	I_E	150	mA
Peak-Pulse Emitter Current Note 1	i_e	2.0	Amp
Emitter Reverse Voltage	V_{EB2O}	8.0	Volts
Interbase Voltage	V_{B2B1}	30	Volts
Power Dissipation Derate above T_A = 25°C	P_D	300 3.0	mW mW/°C
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +200	°C

*Indicates JEDEC Registered Data.
Note 1: Duty Cycle ≤ 1%, PRR = 10 PPS (See Figure 14).

COMPLEMENTARY UNIJUNCTION TRANSISTORS



STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A

FIGURE 1 – STANDARD UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

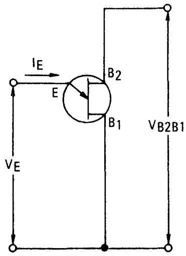


FIGURE 2 – COMPLEMENTARY UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

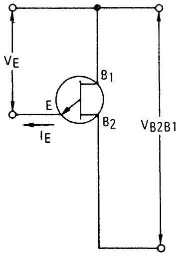
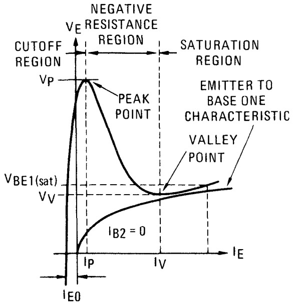


FIGURE 3 – STATIC EMITTER CHARACTERISTICS CURVES



***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Instrinsic Standoff Ratio (Note 2) ($V_{B2B1(1)}$ = 10 Vdc, $V_{B2B1(2)}$ = 5.0 Vdc)	η	0.58	–	0.62	–
Interbase Resistance (V_{B2B1} = 1.0 Vdc, I_E = 0) 2N6114 2N6115	R_{BB}	5.5 5.0	6.8 8.0	8.2 15	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 1.0 Vdc, I_E = 0, T_A = -55 to +100°C)	αR_{BB}	0.05	–	0.5	%/°C
Emitter Saturation Voltage (Note 3) (V_{B2B1} = 10 Vdc, I_E = 50 mA)	$V_{EB1(sat)}$	–	1.1	1.5	Volts
Modulated Interbase Current (V_{B2B1} = 10 Vdc, I_E = 50 mA)	$I_{B2(mod)}$	1.0	4.0	10	mA
Emitter Reverse Current (V_{EB2} = 5.0 Vdc, I_{B1} = 0) 2N6114 2N6115	I_{EB2O}	– –	0.1 0.1	100 10	nA
Peak-Point Emitter Current (V_{B2B1} = 10 Vdc) 2N6114 2N6115	I_P	– –	– –	5.0 15	μA
Valley-Point Emitter Current (Note 3) (V_{B2B1} = 10 Vdc)	I_V	1.0	4.5	–	mA
Peak-Point Voltage (V_{B2B1} = 5.0 Vdc) (V_{B2B1} = 10 Vdc)	V_P	3.2 6.1	3.45 6.45	3.7 6.8	Volts
Base-One Peak Pulse Voltage (Figure 15)	V_{OB1}	3.5	4.5	–	Volts
Emitter Breakdown Voltage (I_{EB1} = 10 μA)	V_{EB1O}	8.0	9.5	–	Volts
Diode Voltage (Note 2)	V_D	0.3	–	0.6	Volts
Minimum Charge to Trigger	Q_t	–	50	–	PC
Turn On Time	t_{on}	–	0.85	–	μs
Recovery Time	t_{rec}	–	7.0	–	μs

*Indicates JEDEC Registered Data.

Note 2: Intrinsic Standoff Ratio (η) is defined in terms of the Peak-Point Voltage (V_P) by means of the equation:

$$\eta = \frac{V_{P1} - V_{P2}}{V_{B2B1(1)} - V_{B2B1(2)}}$$

where $V_{B2B1(1)}$ = 10 Vdc ± 0.001 Vdc and $V_{B2B1(2)}$ = 5.0 Vdc.The associated Diode Voltage (V_D) is defined by the equation $V_D = V_{P2} - \eta V_{B2B1(2)}$.

Note 3: Use pulse techniques: PW ≈ 300 μs, duty cycle ⩽ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 4 – STATIC EMITTER CHARACTERISTICS

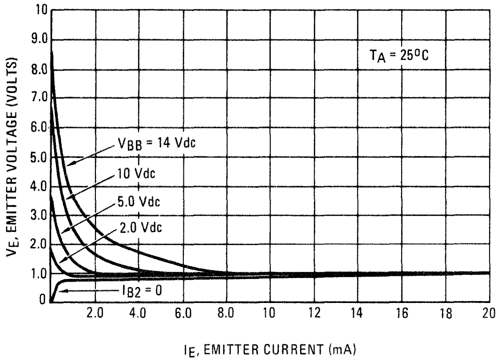
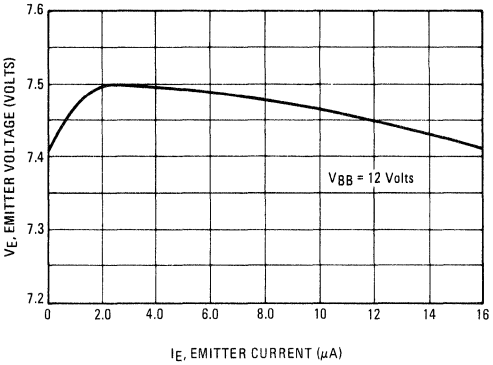


FIGURE 5 – PEAK POINT CHARACTERISTICS



PEAK POINT CURRENT

FIGURE 6 – EFFECT OF VOLTAGE

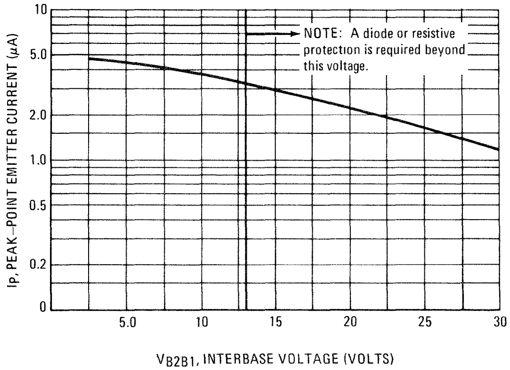
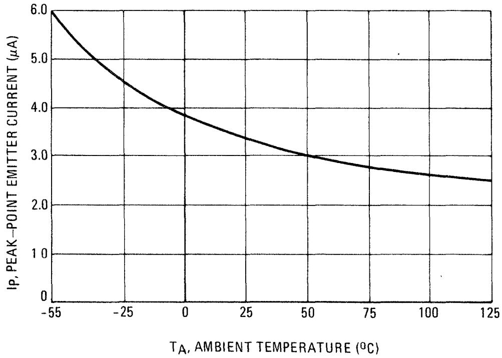


FIGURE 7 – EFFECT OF TEMPERATURE



VALLEY CURRENT

FIGURE 8 – EFFECT OF VOLTAGE

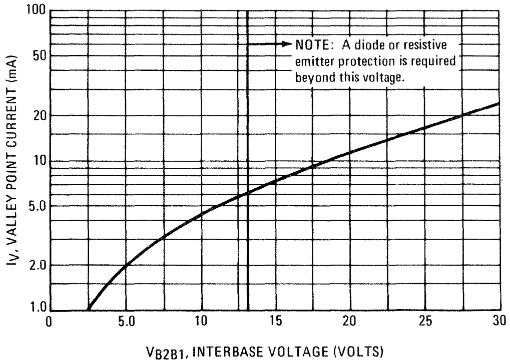


FIGURE 9 – EFFECT OF TEMPERATURE

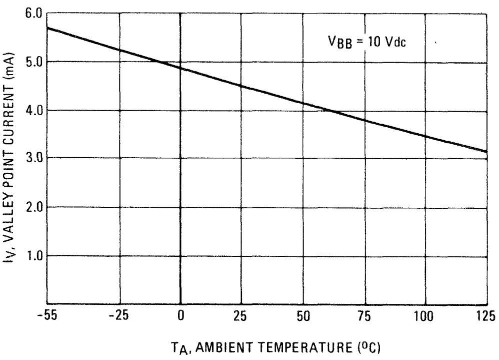


FIGURE 10 – DIODE VOLTAGE

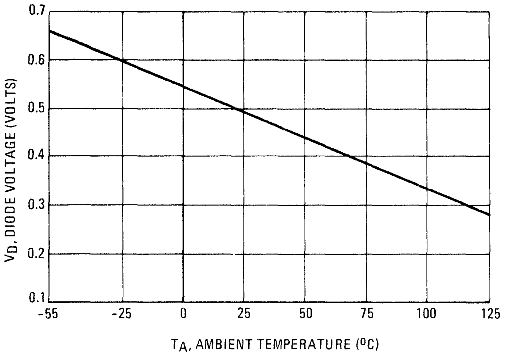


FIGURE 11 – EMITTER LEAKAGE CURRENT

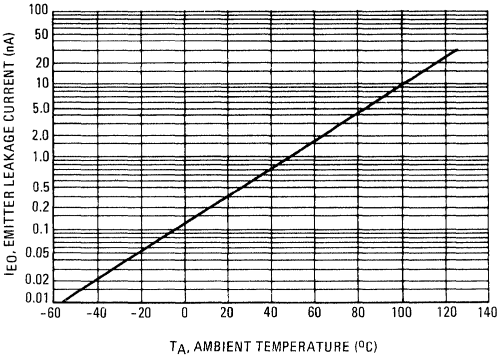


FIGURE 12 – STATIC INTERBASE CHARACTERISITCS

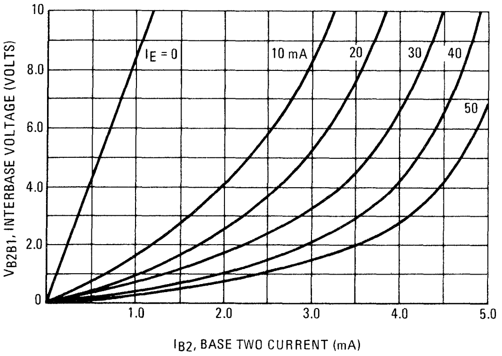


FIGURE 13 – INTERBASE RESISTANCE

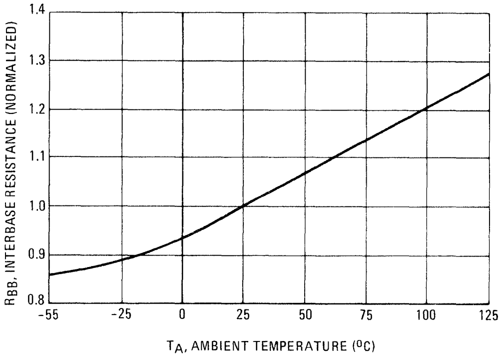


FIGURE 14 – PEAK EMITTER CURRENT TEST CIRCUIT AND WAVEFORM

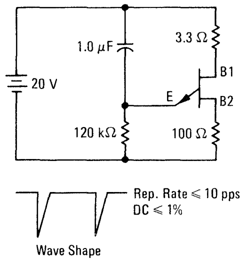


FIGURE 15 – BASE-ONE PEAK PULSE VOLTAGE CIRCUIT

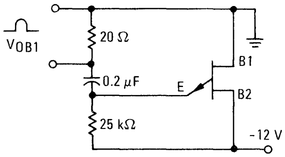
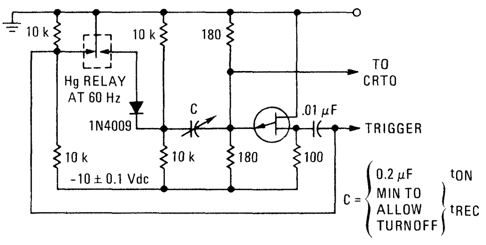
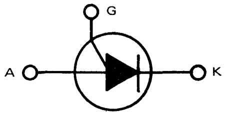


FIGURE 16 – SWITCHING CIRCUIT



2N6116 (SILICON)
2N6117
2N6118

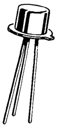


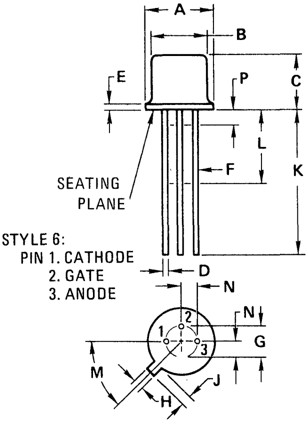
SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-triggor, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate.

- Programmable – R_{BB}, η, I_V and I_P
- Hermetic TO-18 Package
- Low On-State Voltage – 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 5.0 nA Maximum
- High Peak Output Voltage – 16 Volts Typical
- Low Offset Voltage – 0.35 Volt Typical (R_G = 10 k ohms)

SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS
40 VOLTS
250 mW





STYLE 6:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC notes and dimensions apply.

CASE 22-03
(TO-18)

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle 20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
DC Forward Anode Current Derate Above 25°C	I_T	200 2.0	mA mA/°C
DC Gate Current	I_G	±20	mA
Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
Gate to Cathode Reverse Voltage	V_{GKR}	5.0	Volt
Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
Anode to Cathode Voltage	V_{AK}	±40	Volt
Forward Power Dissipation @ T_A = 25°C Derate Above 25°C	P_F $1/\theta_{JA}$	250 2.5	mW mW/°C
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

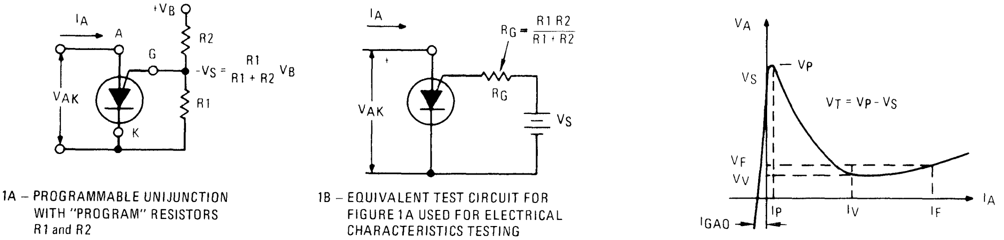
*Indicates JEDEC Registered Data

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Offset Voltage	2N6116	1	V_T	0.2	0.70	1.6	Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6117			0.2	0.50	0.6	
	2N6118			0.2	0.40	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	All Types			0.2	0.35	0.6	
Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	5.0	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	30	75	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
Peak Current	2N6116	2,9-14	I_p	–	1.25	2.0	μA
(V_S = 10 Vdc, R_G = 10 MΩ)	2N6117			–	0.19	0.3	
	2N6118			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6116			–	4.0	5.0	
	2N6117			–	1.20	2.0	
	2N6118			–	0.70	1.0	
Valley Current		1,4,5	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6116, 2N6117			–	18	50	
	2N6118			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6116			70	270	–	
	2N6117, 2N6118			50	270	–	
Forward Voltage (I_F = 50 mA Peak)		1,6	V_T	–	0.8	1.5	Volts
Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	16	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

*Indicates JEDEC Registered Data

FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – PROGRAMMABLE UNIJUNCTION WITH "PROGRAM" RESISTORS R1 and R2

1B – EQUIVALENT TEST CIRCUIT FOR FIGURE 1A USED FOR ELECTRICAL CHARACTERISTICS TESTING (ALSO SEE FIGURE 2)

1C – ELECTRICAL CHARACTERISTICS

FIGURE 2 – PEAK CURRENT (I_p) TEST CIRCUIT

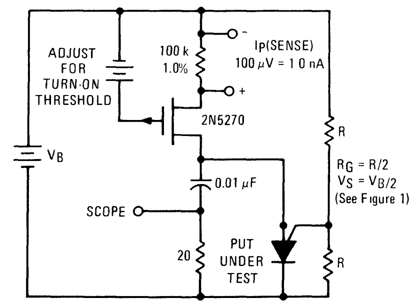
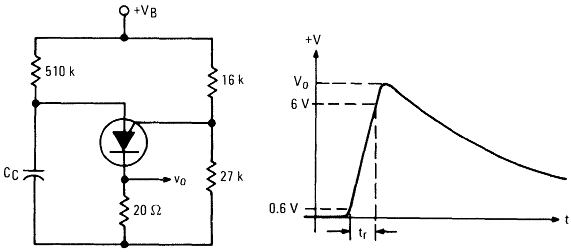


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

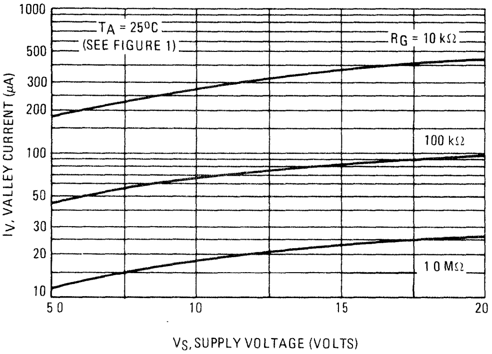


FIGURE 5 – EFFECT OF TEMPERATURE

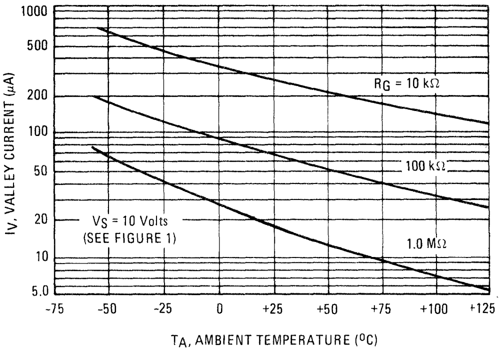


FIGURE 6 – FORWARD VOLTAGE

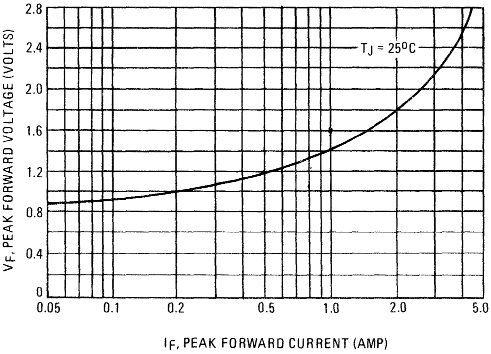


FIGURE 7 – PEAK OUTPUT VOLTAGE

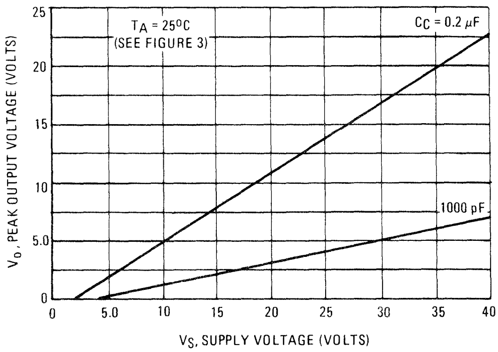
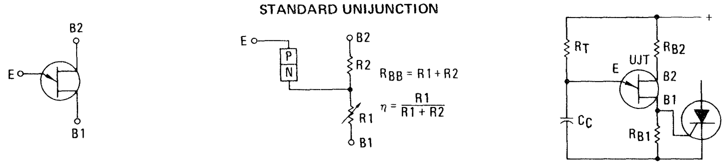


FIGURE 8 – STANDARD UNIJUNCTION COMPARED TO PROGRAMMABLE UNIJUNCTION

STANDARD UNIJUNCTION

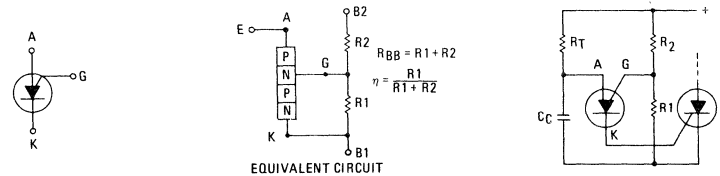


CIRCUIT SYMBOL

EQUIVALENT CIRCUIT

TYPICAL APPLICATION

PROGRAMMABLE UNIJUNCTION



CIRCUIT SYMBOL

EQUIVALENT CIRCUIT
WITH EXTERNAL "PROGRAM"
RESISTORS R1 and R2

TYPICAL APPLICATION

TYPICAL PEAK CURRENT BEHAVIOR

2N6116

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

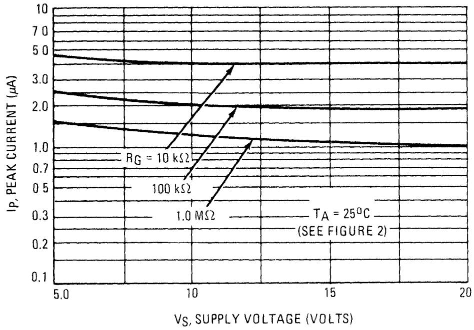
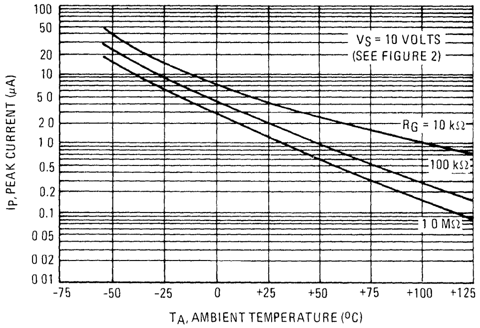


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



2N6117

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

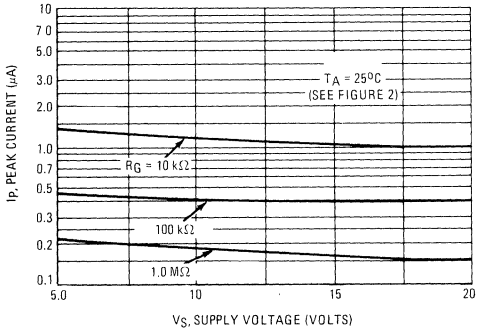
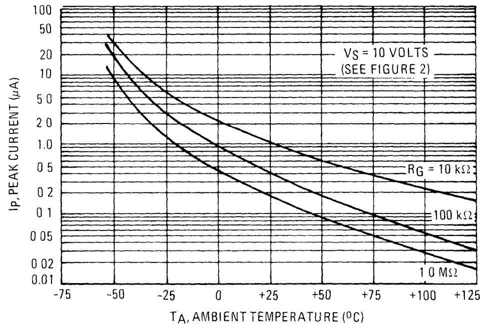


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



2N6118

FIGURE 13 – EFFECT OF SUPPLY VOLTAGE AND R_G

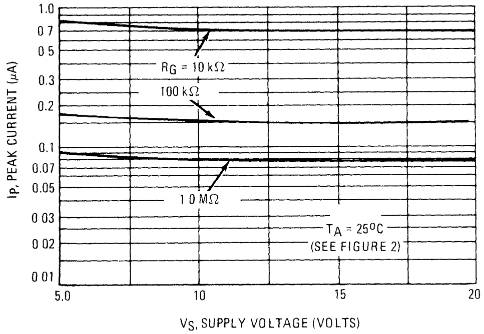
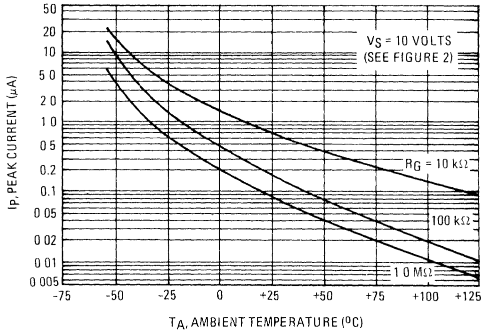


FIGURE 14 – EFFECT OF TEMPERATURE AND R_G



2N6136 (SILICON)

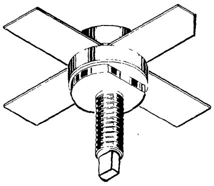
The RF Line

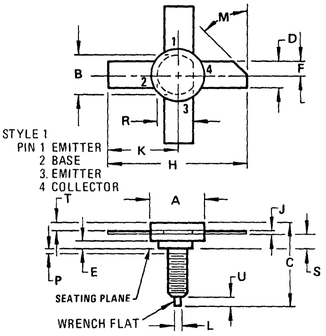
NPN SILICON RF POWER TRANSISTOR

. . .designed for 12.5 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating to 520 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics –
  Output Power = 25 Watts
  Minimum Gain = 4.0 dB
  Efficiency = 65%
- Overlay Construction Provides Protection Against Device Damage Due to Load Mismatch
- Characterized With Series Equivalent Large-Signal Impedance Parameters

25 W – 470 MHz
RF POWER
TRANSISTOR
NPN SILICON





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	18.03	19.05	0.710	0.750
D	5.59	5.84	0.220	0.230
E	1.78	2.03	0.070	0.080
F	2.79	2.92	0.110	0.115
H	26.42	28.70	1.040	1.130
J	0.10	0.15	0.004	0.006
K	13.21	14.35	0.520	0.565
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130

NOTE
CASE 145A-01 USE 8-32NC2A STUD

CASE 145A-01

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	6.0	Adc
Total Device Dissipation @ T_C = 25°C (2) Derate above 25°C	P_D	60 0.343	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C
Stud Torque (1)	–	6.5	in. lb.

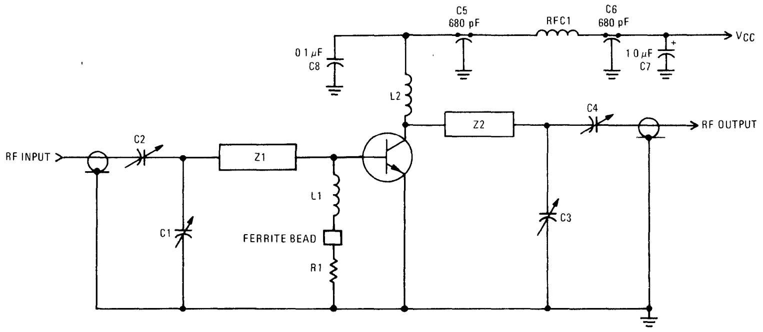
*Indicates JEDEC Registered Data
(1) For repeated assembly use 5 in. lb.
(2) This device is designed for RF operation. The total device dissipation rating applies only when the devices are operated as class B or C RF amplifiers.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	BV_{CEO}	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	BV_{CES}	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 50 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 55°C)	I_{CES}	–	–	20	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	55	70	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 25 W, V_{CC} = 12.5 Vdc, f = 470 MHz)	G_{PE}	4.0	–	–	dB
Collector Efficiency (P_{out} = 25 W, V_{CC} = 12.5 Vdc, f = 470 MHz)	η	65	–	–	%

*Indicates JEDEC Registered Data

FIGURE 1 — 470 MHz TEST CIRCUIT SCHEMATIC



Note: Test circuit layout shown in Figure 6.

FIGURE 2 — OUTPUT POWER versus INPUT POWER

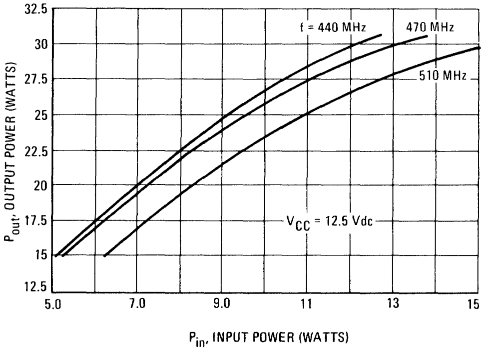


FIGURE 3 — OUTPUT POWER versus FREQUENCY

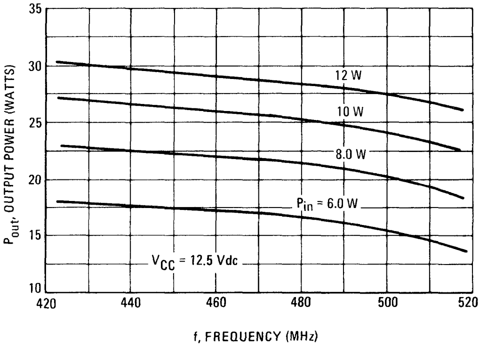


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

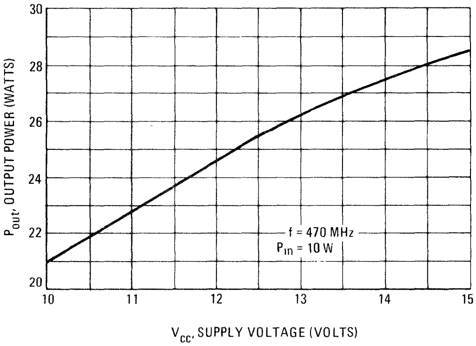


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE PARAMETERS

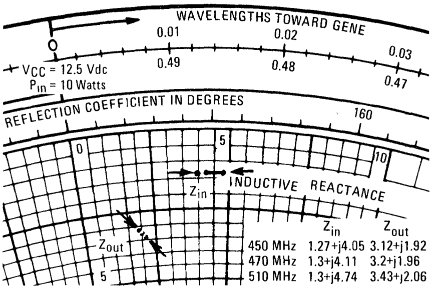
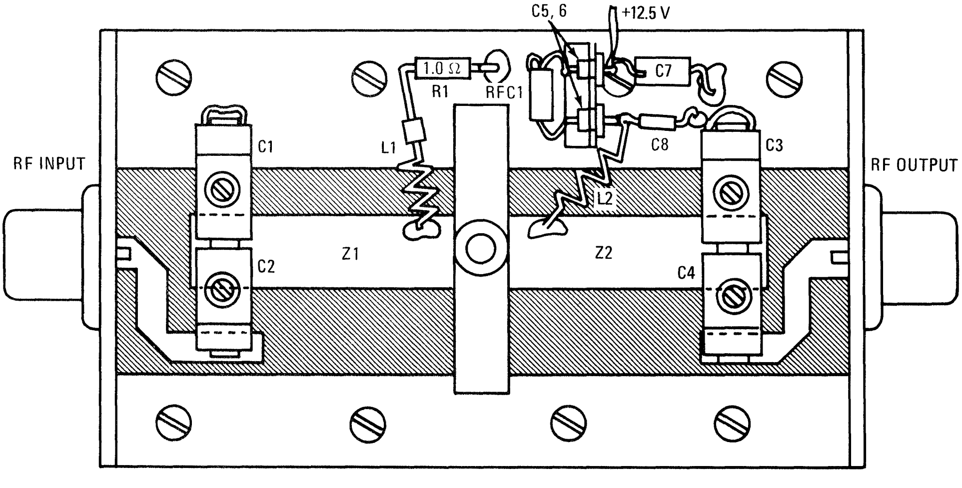


FIGURE 6 – 470 MHz TEST CIRCUIT LAYOUT (1:1 Scaled Drawing)



C1, 2, 3, 4 1.0-25pF ARCO 421 OR EQUIVALENT
UHF COMPRESSION
MICAS

L1, L2 5 Turns #20 AWG 0.2 I.D.
FERRITE BEAD, FERROXCUBE 56-590-65-3B
AS SHOWN ON L1

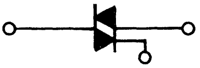
C5,6 – 680 pF FT CAPACITOR
C7 – 1.0 μF, 35V TANTALUM CAPACITOR
RFC1 – CHOKE FERROXCUBE VK 200-20-4B
C8 – 0.1 μF ERIE CK06

R1 1.0 OHM, 1/2 WATT
CONNECTORS ARE TYPE "N"
BOARD IS GLASS TEFLON
3" X 5" X 0.062" 1 oz COPPER BOTH SIDES
SHOWN TO SCALE
CLADDING REMOVED IN DARK AREAS
MOUNTING PLATE IS 3" X 5" X 0.75" ALUMINUM

Z1 and Z2 BASE AND COLLECTOR
LINES ARE 0.5" X 1.75"

Note: Figure 6 is 1:1 scaled layout of test circuit shown in Figure 1. This layout may be transferred directly to glass teflon board for easy reproduction of the test circuit.

2N6139 thru 2N6144 (SILICON)
2N6148 thru 2N6150



TRIACS
(THYRISTORS)

10 AMPERES RMS

SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Economical for a Wide Range of Uses
- High Surge Current – I_{TSM} = 100 Amp
- Low Forward "On" Voltage – 1.4 V typ @ I_{TM} = 14 A
- All Diffused and Passivated Junctions for Greater Stability
- Rugged Construction in Either 3 Lead, Stud or Isolated Stud Package
- Gate Triggering Guaranteed in Four Modes

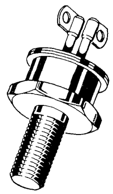
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage, Note 1 (T_J = -65 to +100°C, ½ Sine Wave 50 to 60 Hz, Gate Open)	V_{DRM}		Volts
*Peak Principle Voltage 2N6139, 2N6142, 2N6148 2N6140, 2N6143, 2N6149 2N6141, 2N6144, 2N6150		 200 400 600	
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS (-65 to +75°C) (Full Cycle Sine Wave, 50 to 60 Hz) (+90°C)	$I_{T(RMS)}$	10 5.0	Amp
*Peak Surge Current (One Full Cycle, 60 Hz, T_J = +75°C, preceded and followed by 10 A current)	I_{TSM}	100	Amp
Circuit Fusing Considerations (T_J = -65 to +100°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_J = +75°C, Pulse Width = 2.0 μ)	P_{GM}	20	Watts
*Average Gate Power (T_J = +75°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-65 to +100	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Stud Torque 2N6139 thru 2N6144	–	15	in. lb.

THERMAL CHARACTERISTICS

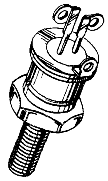
Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W
Thermal Resistance, Case to Ambient	$R_{\theta CA}$	50	°C/W

*Indicates JEDEC Registered Data



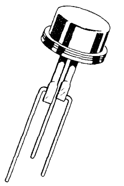
2N6139
2N6140
2N6141

CASE 86



2N6142
2N6143
2N6144

CASE 250



2N6148
2N6149
2N6150

CASE 87L

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 14 A Peak, Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤2.0 %	V_{TM}	–	1.4	1.8	Volts
Gate Trigger Current, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms, Minimum Gate Pulse Width = 2.0 µs	I_{GT}				mA
MT2 (+), G(+)		–	6.0	50	
MT2 (+), G(–)		–	6.0	75	
MT2 (–), G(–)		–	10	50	
MT2 (–), G(+)		–	25	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -65°C		–	–	125	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -65°C		–	–	150	
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms, Minimum Gate Pulse Width = 2.0 µs	V_{GT}				Volts
MT2 (+), G(+)		–	0.9	2.0	
MT2 (+), G(–)		–	0.9	2.5	
MT2 (–), G(–)		–	1.1	2.0	
MT2 (–), G(+)		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -65°C		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -65°C		–	–	3.0	
*Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 100°C		0.2	–	–	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 300 mA	I_H				mA
T_C = 25°C		–	6.0	40	
T_C = -65°C		–	–	150*	
*Turn-On Time Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 14 A, Gate Source Voltage = 12 V, R_S = 50 Ohms, Rise Time = 0.1 µs, Pulse Width = 2.0 µs	tgt	–	1.5	2.0	µs
Blocking Voltage Application Rate at Commutation, f=60 Hz, T_C=75°C On-State Conditions: I_{TM} = 14 A, Pulse Width = 4.0 ms, di/dt=5.3 A/ms Off-State Conditions: Main Terminal Voltage = Rated V_{DRM} (200 µs min), Gate Source Voltage = 0 V, R_S = 100 Ω	dv/dt	–	5.0	–	V/µs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

Trigger devices are recommended for gating on Triacs.

Triggers Provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

Electrical Characteristics	**For General Usage**		**For Lamp Dimmer**
Symbol	MBS4991	MBS4992	MBS100
V_S =	6.0 –10 V	7.5–9.0 V	3.0–5.0 V
I_S =	350 µA Max	120 µA Max	100–400 µA
V_{S1}–V_{S2} =	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient = 0.02%/°C Typ			

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

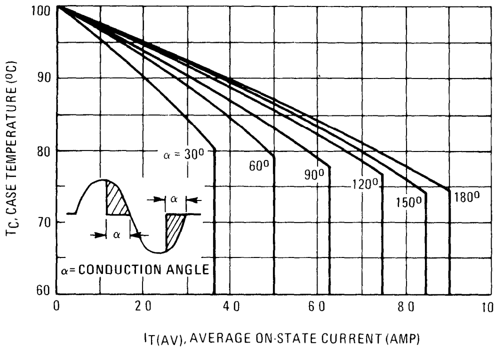


FIGURE 2 – RMS CURRENT DERATING

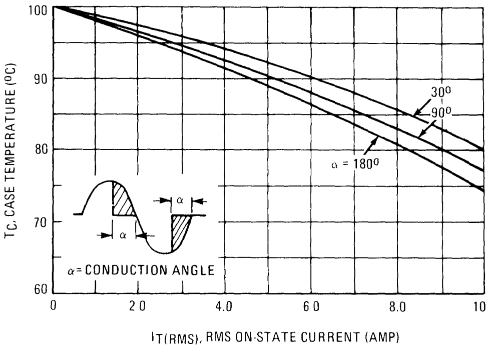


FIGURE 3 – POWER DISSIPATION

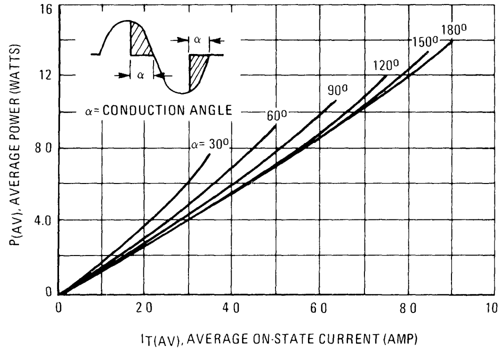


FIGURE 4 – POWER DISSIPATION

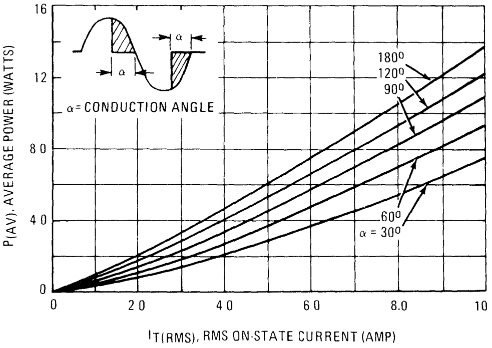


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

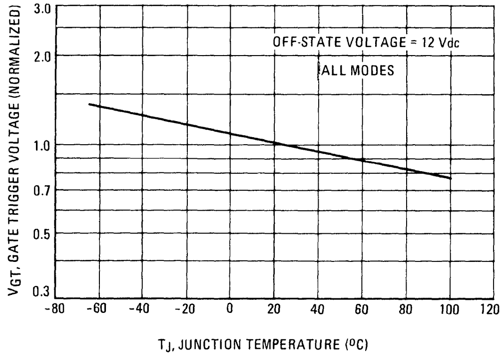


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

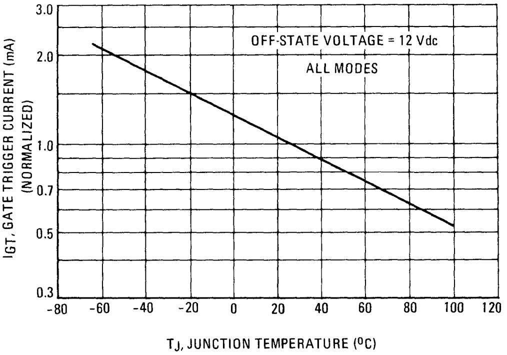


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

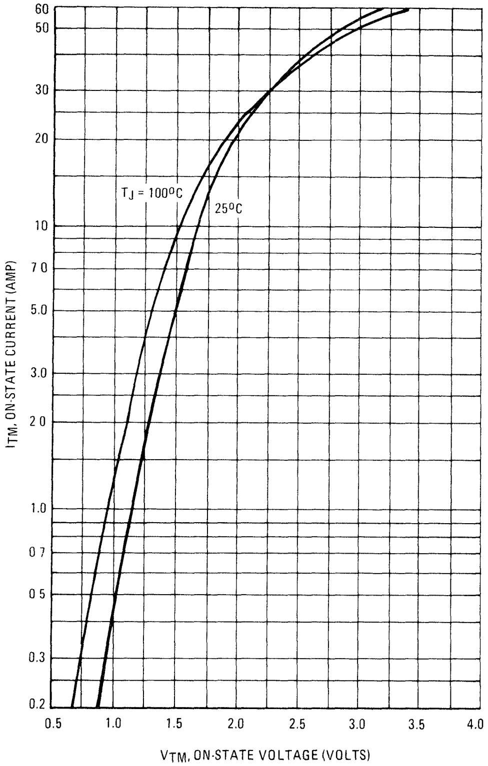


FIGURE 8 – TYPICAL HOLDING CURRENT

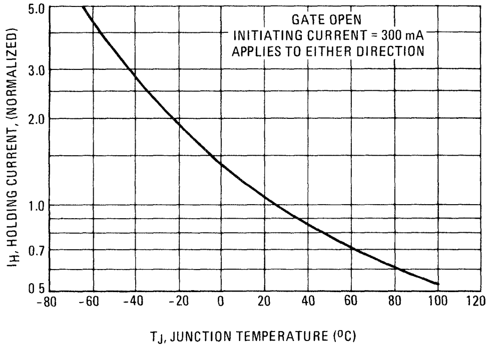


FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

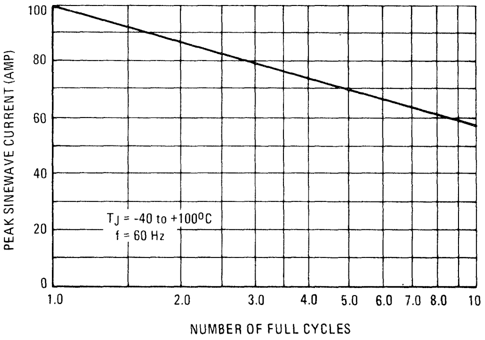
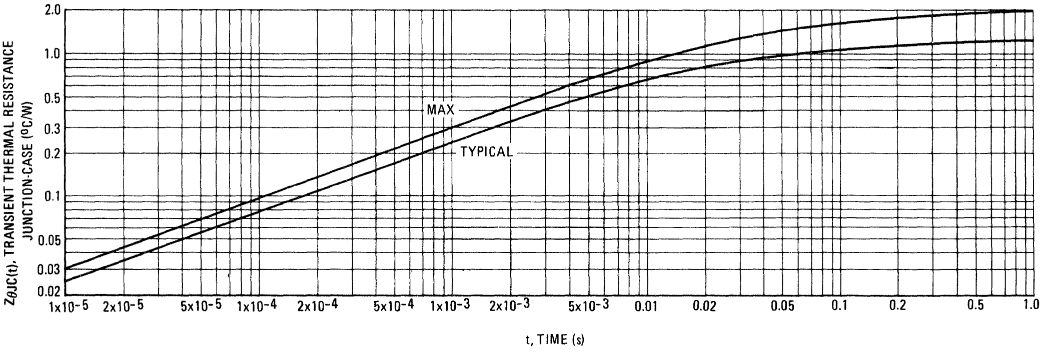
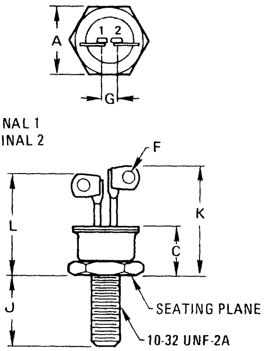


FIGURE 10 – THERMAL RESPONSE



STYLE 2:
PIN 1. GATE
2. MAIN TERMINAL 1
STUD: MAIN TERMINAL 2



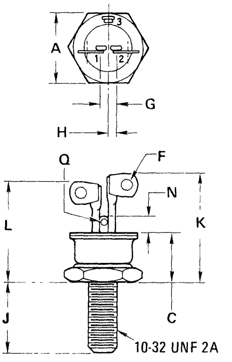
2N6139
2N6140
2N6141

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	11.10	–	0.437
C	–	7.87	–	0.310
F	1.78 TYP		0.070 TYP	
G	2.29	2.79	0.090	0.110
J	10.72	11.48	0.422	0.452
K	–	16.76	–	0.660
L	–	15.49	–	0.610

NOTE:
1. DIM "G" MEASURED AT CAN.

CASE 86

STYLE 2:
PIN 1. GATE
2. ANODE 1
3. ANODE 2
STUD – ISOLATED

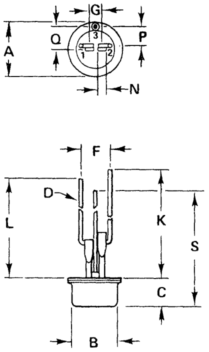


2N6142
2N6143
2N6144

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	11.10	–	0.437
C	–	10.92	–	0.430
F	1.65	1.91	0.065	0.075
G	2.29	2.79	0.090	0.110
H	1.14	1.40	0.045	0.055
J	10.72	11.48	0.422	0.452
K	–	16.76	–	0.660
L	—	15.49	–	0.610
N	3.43	3.68	0.135	0.145
Q	1.65	1.91	0.065	0.075

CASE 250-01

STYLE 2:
PIN 1. GATE
2. MAIN TERMINAL 1
3. MAIN TERMINAL 2



2N6148
2N6149
2N6150

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	10.92	–	0.430
B	–	8.89	–	0.350
C	–	5.97	–	0.235
D	0.76	0.86	0.030	0.034
F	4.83	5.33	0.190	0.210
G	2.29	2.79	0.090	0.110
K	33.53	–	1.320	–
L	31.50 TYP		1.240 TYP	
N	1.65	1.91	0.065	0.075
P	3.43	3.68	0.135	0.145
Q	4.57	5.08	0.180	0.200
S	30.48	–	1.20	–

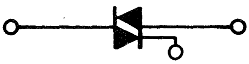
NOTES:
1. DIM. "G" MEASURED AT CAN.
2. LEAD NO. 3 ±7.5° DISPLACEMENT.

CASE 87L-01

2N6145 thru 2N6147 (SILICON)

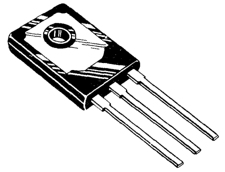
For Specifications, See 2N5571 Data.

2N6151 (SILICON)
thru
2N6156



TRIACS
(THYRISTORS)

10 AMPERES RMS



SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- All Diffused and Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two (2N6154, 2N6155, 2N6156) or Four Modes (2N6151, 2N6152, 2N6153)

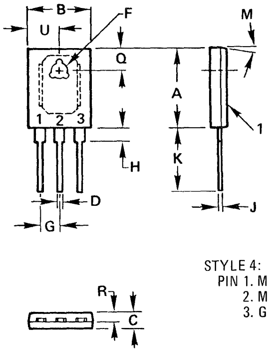
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
* Repetitive Peak Off-State Voltage, Note 1 (T_J = -40 to +100°C) ½ Sine Wave 50 to 60 Hz, Gate Open Peak Principle Voltage 2N6151, 2N6154 2N6152, 2N6155 2N6153, 2N6156	V_{DRM}	 200 400 600	Volts
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS (T_C = -40 to +75°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)	$I_{T(RMS)}$	10 5.0	Amp
*Peak Surge Current (One Full Cycle, 60 Hz, T_J = +75°C) preceded and followed by 10 A Current	I_{TSM}	100	Amp
Circuite Fusing Considerations (T_J = -40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_J = +75°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_J = +75°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
*Mounting Torque (6-32 Screw), Note 2	—	8.0	in. lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
* Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W
Thermal Resistance Case to Ambient	$R_{\theta CA}$	50	°C/W

*Indicates JEDEC Registered Data.



STYLE 4:
PIN 1. MT 1
2. MT 2
3. GATE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

CASE 90-05

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 14 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.8	Volts
Gate Trigger Current, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	I_{GT}				mA
MT2 (+), G(+) All Types		–	6.0	50	
MT2 (+), G(–) 2N6151 thru 2N6153		–	6.0	75	
MT2 (–), G(–) All Types		–	10	50	
MT2 (–), G(+) 2N6151 thru 2N6153		–	25	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6151 thru 2N6153		–	–	125	
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	V_{GT}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6151 thru 2N6153		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6151 thru 2N6153		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6151 thru 2N6153		–	–	3.0	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 100°C					
*MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–); MT2 (–), G(+) 2N6151 thru 2N6153		0.2	–	–	
Holding Current (Either Direction)	I_H				mA
Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA; T_C = 25°C		–	6.0	40	
Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA; T_C = –40°C		–	–	75*	
*Turn-On Time Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 14 A Gate Source Voltage = 12 V, R_S = 100 Ohms, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Blocking Voltage Application Rate at Commutation, f = 60 Hz, T_C = 75°C On-State Conditions: I_{TM} = 14 A, Pulse Width = 4.0 ms, di/dt = 5.3 A/ms Off-State Conditions: Main Terminal Voltage = Rated V_{DRM} (200 μs min), Gate Source Voltage = 0 V, R_S = 100 Ω	dv/dt	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19522 #6 or equivalent). Mounting torque in excess of 8 in. lbs. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common.
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +230°C.

Trigger devices are recommended for gating on Triacs
Triggers Provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

Electrical Characteristics	For General Usage		For Lamp Dimmer
Symbol	MBS4991	MBS4992	MBS100
V_S =	6.0 – 10 V	7.5–9.0 V	3.0–5.0 V
I_S =	350 μA Max	120 μA Max	100–400 μA
V_{S1}–V_{S2} =	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient = 0.02%/°C Typ			

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

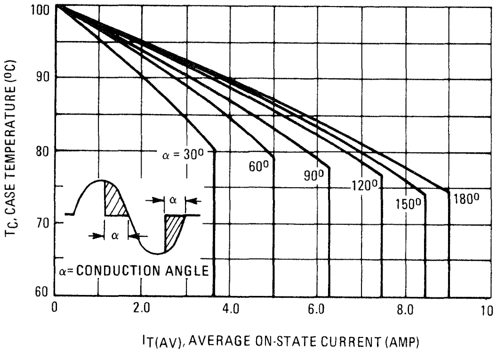


FIGURE 2 – RMS CURRENT DERATING

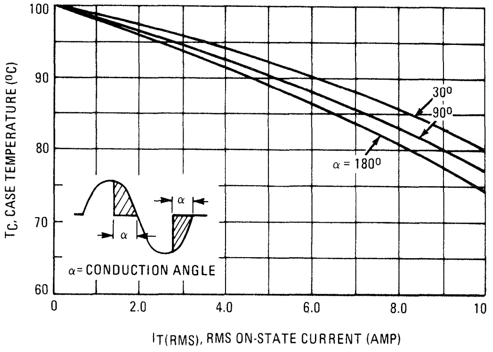


FIGURE 3 – POWER DISSIPATION

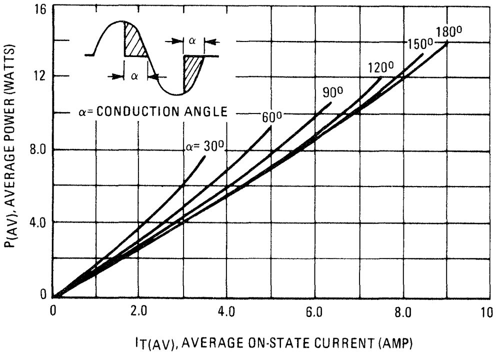


FIGURE 4 – POWER DISSIPATION

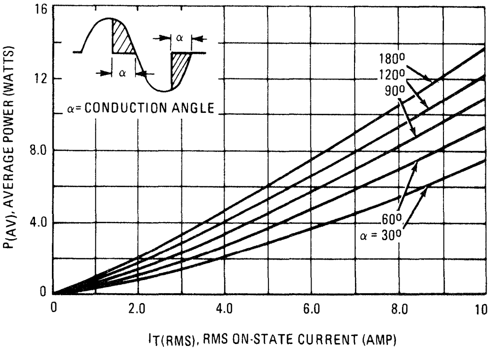


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

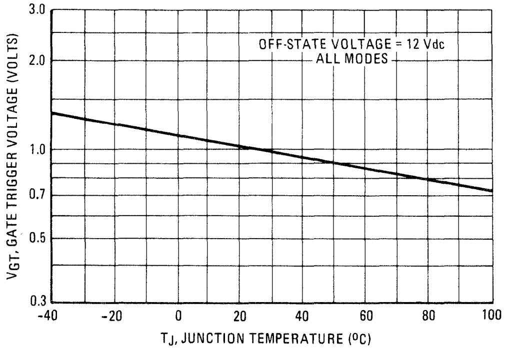


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

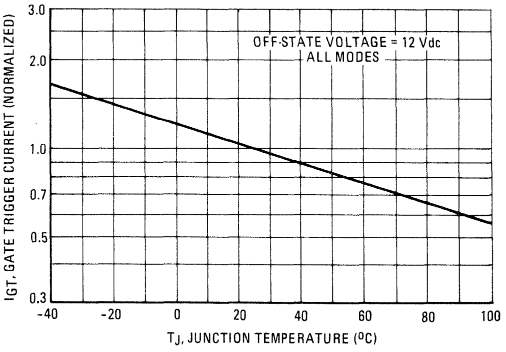


FIGURE 7 — MAXIMUM ON-STATE CHARACTERISTICS

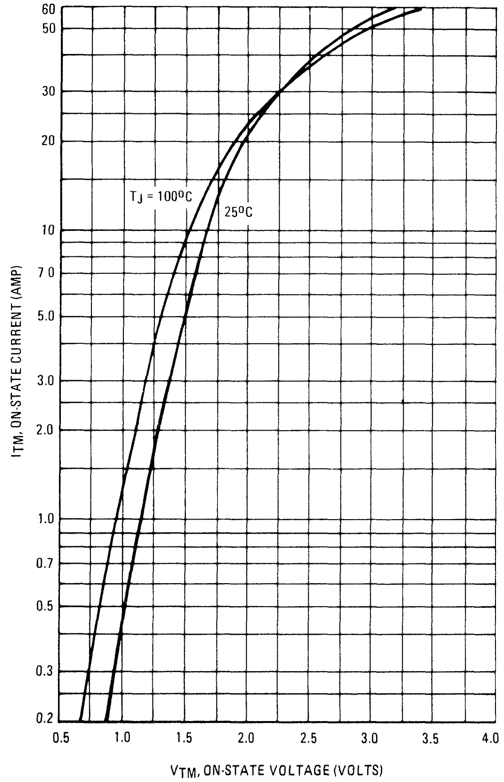


FIGURE 8 — TYPICAL HOLDING CURRENT

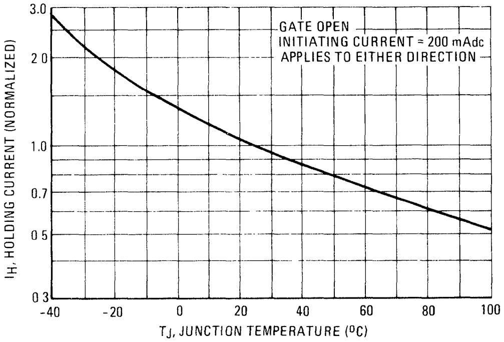


FIGURE 9 — MAXIMUM ALLOWABLE SURGE CURRENT

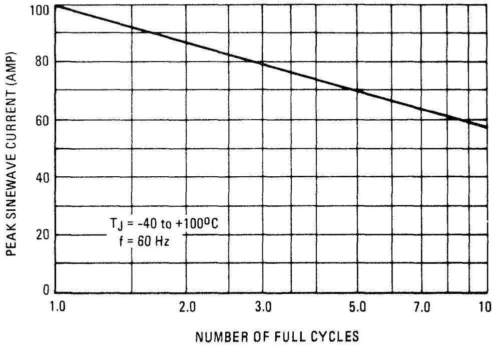
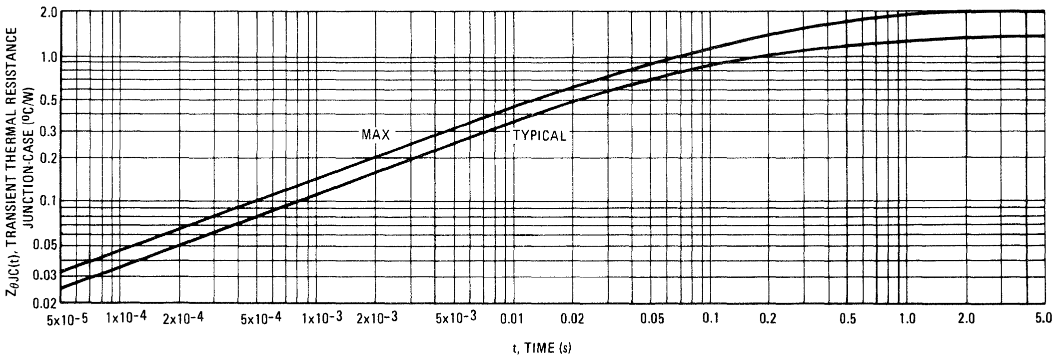


FIGURE 10 — THERMAL RESPONSE



2N6157 (SILICON)
thru
2N6165

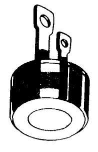
SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants

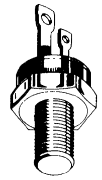
TRIACS (THYRISTORS)

30 AMPERES RMS



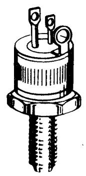
2N6157
2N6158
2N6159

CASE 174
TO-203



2N6160
2N6161
2N6162

CASE 175



2N6163
2N6164
2N6165

CASE 235

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage (1) (T_J = -65 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open *Peak Principal Voltage	V_{DRM}		Volts
2N6157, 2N6160, 2N6163		200	
2N6158, 2N6161, 2N6164		400	
2N6159, 2N6162, 2N6165		600	
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS	$I_{T(RMS)}$		Amp
(T_C = -65 to +85°C)		30	
(T_C = +100°C) Full Sine Wave, 50 to 60 Hz		20	
*Peak Surge Current (One Full Cycle of surge current at 60 Hz, preceeded and followed by a 30 ARMS current, T_J = +125°C)	I_{TSM}	250	Amp
Circuit Fusing Considerations (T_J = -65 to +125°C, t = 1.0 to 8.3 ms)	I^2t	210	A^2s
*Peak Gate Power (T_J = +80°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_J = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-65 to +125	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Stud Torque 2N6160 thru 2N6165	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

*Indicates JEDEC Registered Data.

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

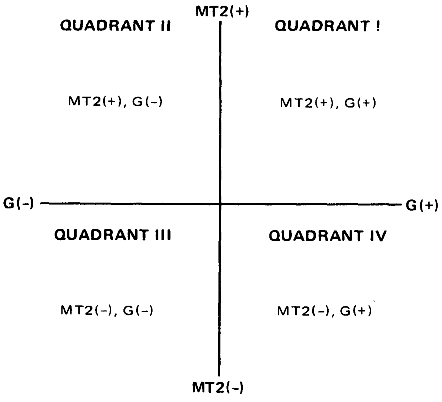
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
* Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 125°C	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 42 A Peak, Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≦ 2.0 %	V_{TM}	–	1.5	2.0	Volts
Gate Trigger Current, Continuous dc (1) Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	I_{GT}				mA
MT2 (+), G(+)		–	10	60	
MT2 (+), G(–)		–	13	70	
MT2 (–), G(–)		–	15	70	
MT2 (–), G(+)		–	20	100	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –65°C		–	–	200	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –65°C		–	–	250	
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	V_{GT}				Volts
MT2 (+), G(+)		–	0.7	2.0	
MT2 (+), G(–)		–	0.7	2.1	
MT2 (–), G(–)		–	0.8	2.1	
MT2 (–), G(+)		–	0.9	2.5	
*All Quadrants, T_C = –65°C)		–	–	3.4	
*Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = +125°C		2.0	–	–	
Holding Current Main Terminal Voltage = 12 Vdc, Gate Open Initiating Current = 500 mA	I_H				mA
MT2 (+)		–	5.0	70	
MT2 (–)		–	5.0	80	
*Either Direction, T_C = –65°C		–	–	200	
*Turn-On Time Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 42 A, Gate Source Voltage = 12 V, R_S = 50 Ohms, Rise Time = 0.1 µs, Pulse Width = 2.0 µs	t_{gt}	–	1.0	2.0	µs
Blocking Voltage Application Rate at Commutation, f = 60 Hz, T_C = 85°C On-State Conditions: I_{TM} = 42A, Pulse Width = 4.0 ms, di/dt = 17.5 A/ms Off State Conditions: Main Terminal Voltage = Rated V_{DRM} (200 µs min), Gate Source Voltage = 0 V, R_S = 50 Ω	dv/dt	–	5.0	–	V/µs

*Indicates JEDEC Registered Data.

(1) All voltage polarity reference to main terminal 1.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 – 10 V	7.5 – 9.0 V	3.0 – 5.0 V
I_S	350 µA Max	120 µA Max	100 – 400 µA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

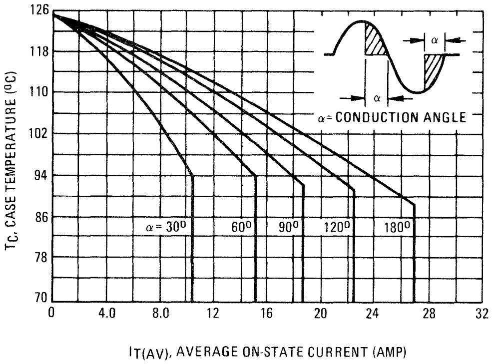


FIGURE 2 – RMS CURRENT DERATING

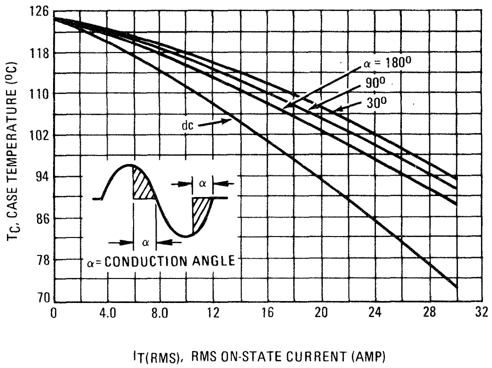


FIGURE 3 – POWER DISSIPATION

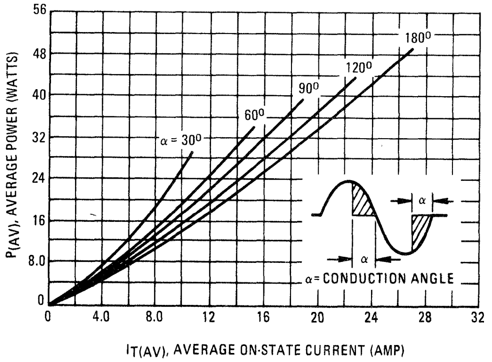


FIGURE 4 – POWER DISSIPATION

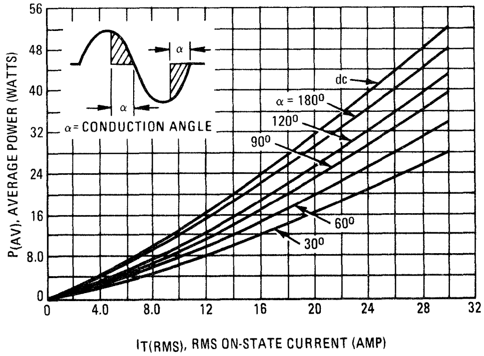


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

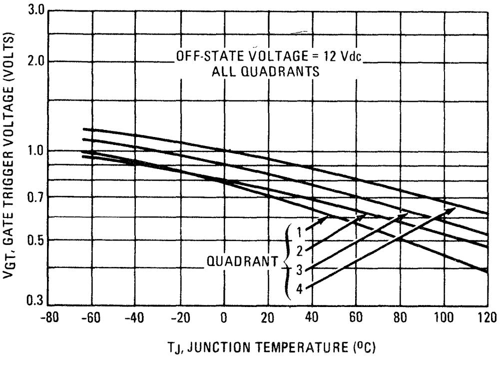


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

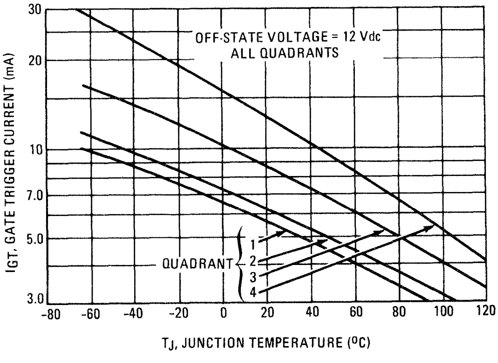


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

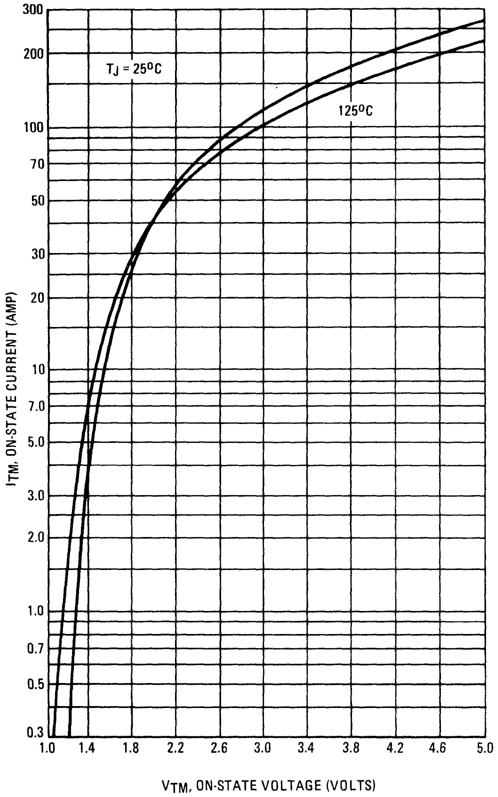


FIGURE 8 – TYPICAL HOLDING CURRENT

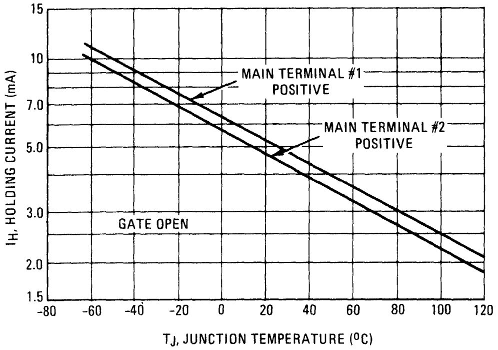


FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

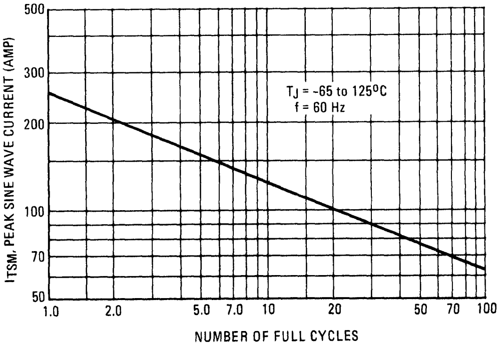
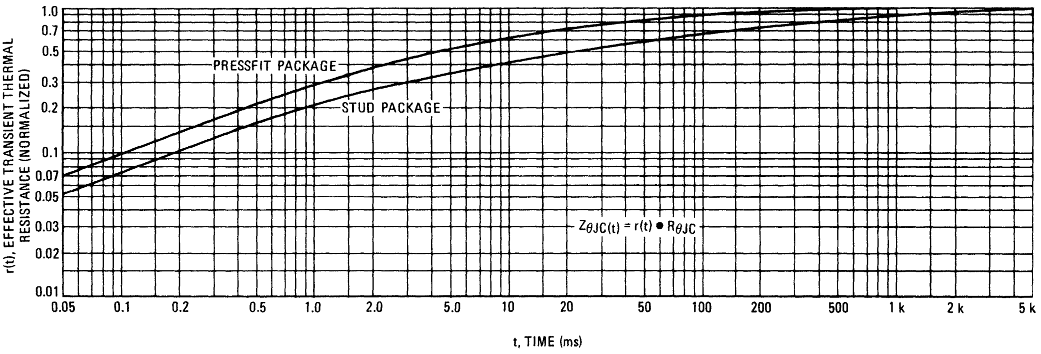
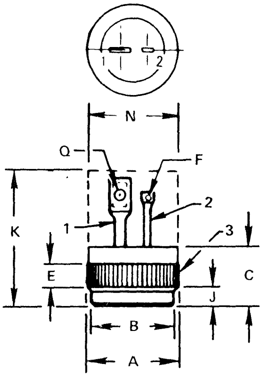


FIGURE 10 – TYPICAL THERMAL RESPONSE



2N6157
2N6158
2N6159



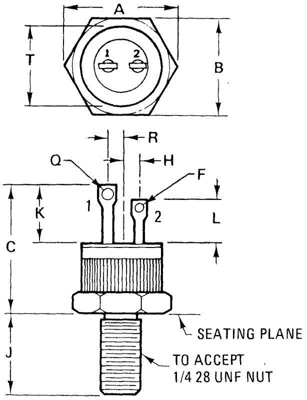
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.726	12.827	0.501	0.505
B	11.811	12.065	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	1.72	0.035	0.068
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.66	2.28	0.065	0.090

All JEDEC dimensions and notes apply

CASE 174-02
TO-203AA

STYLE 3:
TERM. 1. MAIN TERMINAL 1
2. GATE
CASE MAIN TERMINAL 2

2N6160
2N6161
2N6162

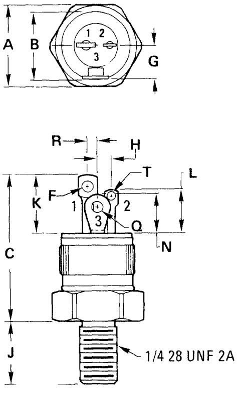


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	1.40	1.65	0.055	0.065
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	2.03	2.41	0.080	0.095
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

CASE 175

STYLE 3:
TERM. 1. MAIN TERMINAL 1
2. GATE
STUD: MAIN TERMINAL 2

2N6163
2N6164
2N6165



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	2.03	2.41	0.080	0.095
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	1.40	1.65	0.055	0.065

STYLE 2:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2
STUD-ISOLATED

CASE 235

2N6166 (SILICON)

The RF Line

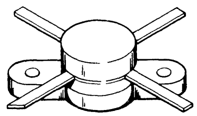
NPN SILICON RF POWER TRANSISTOR

. . . designed for VHF power amplifier applications in military and industrial equipment. Particularly suited for use in Class AB, B, or C amplifier applications to 200 MHz

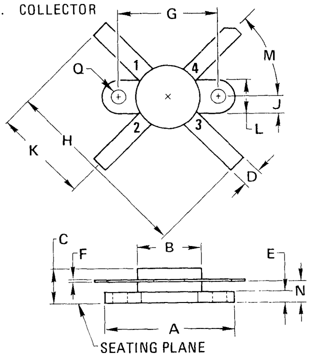
- High Output Power Capability –
  100 Watts Output @ f = 150 MHz
- Balanced Emitter Construction to Provide the Designer With the Device Technology that Assures Ruggedness and Resists Transistor Damage Caused by Load Mismatch.
- Flange Case for Ease of Mounting and Improved Thermal Conductivity

100 WATTS – 150 MHz

NPN SILICON
RF POWER
TRANSISTOR



PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.64	24.89	0.970	0.980
B	11.81	12.07	0.465	0.475
C	5.82	6.73	0.229	0.265
D	2.16	3.94	0.085	0.155
E	2.13	2.54	0.084	0.100
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	35.56	38.10	1.400	1.500
J	3.12	3.23	0.123	0.127
K	17.78	19.05	0.700	0.750
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.66	4.32	0.144	0.170
Q	2.97	3.12	0.117	0.123

CASE 211-02

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	9.0	Adc
Total Device Dissipation @ $T_C = 25°C$ (1) Derate above 25°C	P_D	117 0.667	Watts W/°C
Storage Temperature Range	Tstg	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.5	°C/W

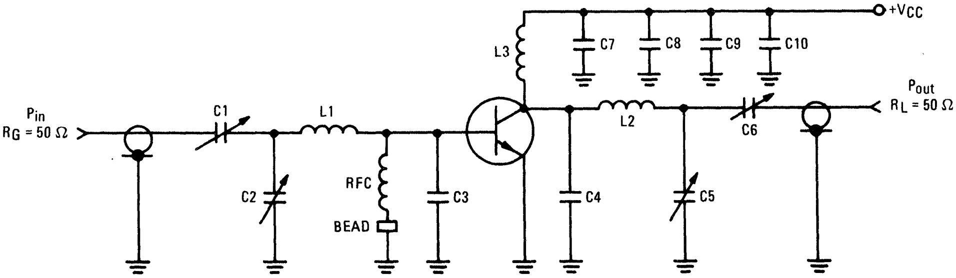
(1) This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

*Indicates JEDEC Registered Data

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

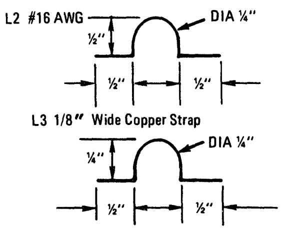
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	BV_{CEO}	35	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	BV_{CES}	65	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0, T_C = 55°C)	I_{CES}	–	5.0	mAdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	3.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	130	pF
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (P_{out} = 100 W, V_{CC} = 28 Vdc, I_C (Max) = 5.95 Adc, f = 150 MHz)	G_{PE}	6.0	–	dB
Common-Emitter Amplifier Power Gain (P_{out} = 30 W, V_{CC} = 13.5 V, f = 150 MHz)	G_{PE}	4.5	–	dB
Collector Efficiency (P_{out} = 100 W, V_{CC} = 28 Vdc, I_C (Max) = 5.95 Adc, f = 150 MHz)	η	60	–	%

FIGURE 1 — 150 MHz TEST CIRCUIT



C1, C6 2.7-30 pF, Arco 461 or Equivalent
C2, C5 9.0-180 pF, Arco 463 or Equivalent
C3 100 pF Underwood
C4 25 pF Underwood
C7 0.01 μF Ceramic Disc
C8 0.1 μF Ceramic Disc
C9 2400 pF Button
C10 5.0 μF/50 V
RFC 0.15 μH J. W. Miller
BEAD: FERROXCUBE 56-590-65-3B

L1 1¼" #16 AWG, Straight



OUTPUT POWER versus FREQUENCY

FIGURE 2 – V_{CC} = 28 Vdc

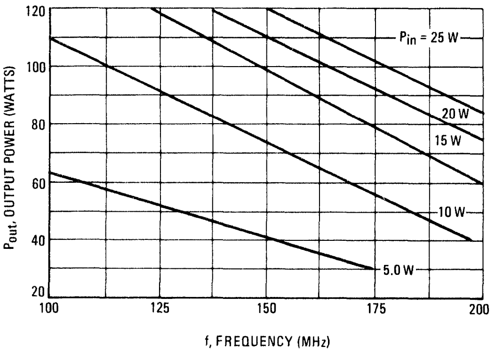


FIGURE 3 – V_{CC} = 13.5 Vdc

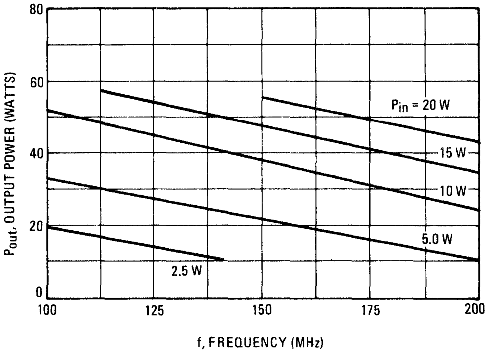


FIGURE 4 – OUTPUT POWER versus INPUT POWER

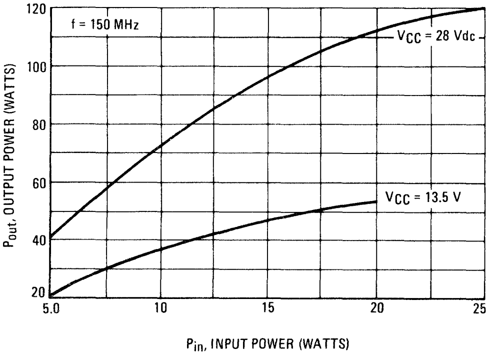


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE

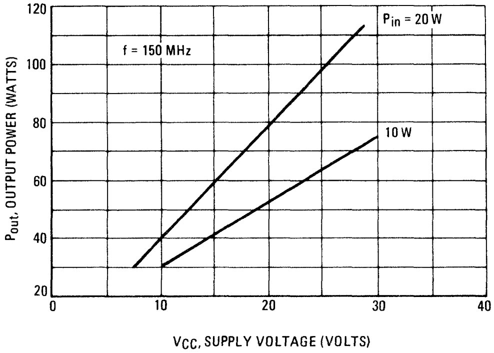


FIGURE 6 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

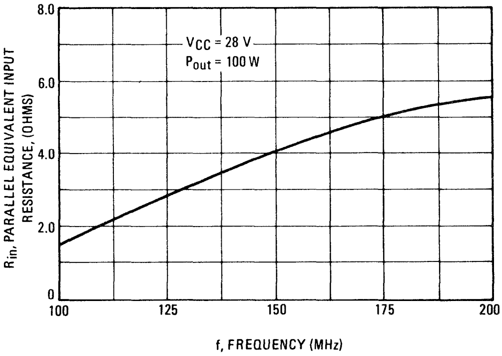


FIGURE 7 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

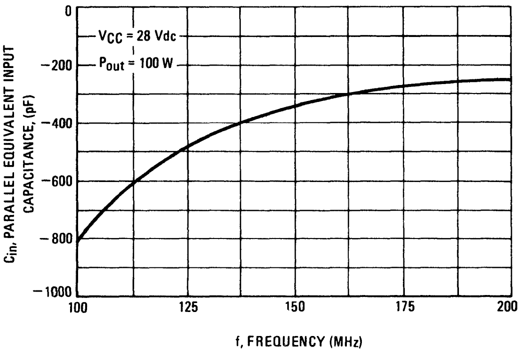
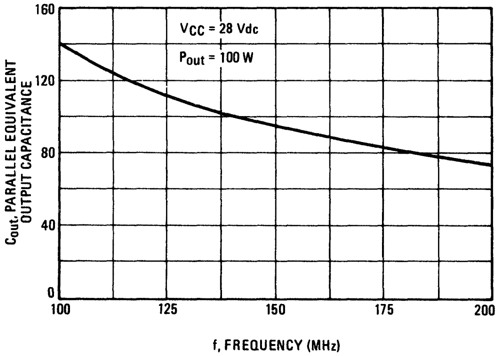


FIGURE 8 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY



2N6167 (SILICON)
thru
2N6170

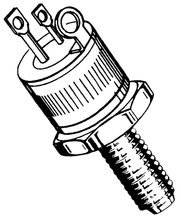
THYRISTORS
SILICON CONTROLLED RECTIFIERS

. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current – I_{TSM} = 240 Amp
- Rugged Construction in Isolated Stud Package

THYRISTORS
PNPN

20 AMPERES RMS
100-600 VOLTS



MAXIMUM RATINGS

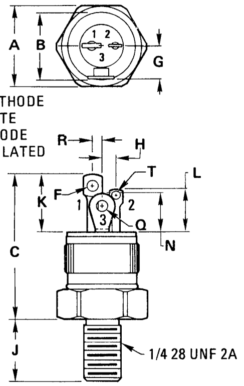
Rating	Symbol	Value	Unit
*Repetitive Peak Reverse Blocking Voltage (1) (T_J = -40 to +100°C) 1/2 Sine Wave, 50 to 400 Hz, Gate Open 2N6167 2N6168 2N6169 2N6170	V_{RRM}	 100 200 400 600	Volts
*Non-Repetitive Peak Reverse Blocking Voltage (t ⩽5.0 ms) 2N6167 2N6168 2N6169 2N6170	V_{RSM}	 150 250 450 650	Volts
*Average Forward Current (T_C = -40 to +65°C) (+85°C)	$I_{T(AV)}$	 13 6.5	Amp
*Peak Surge Current (One cycle, 60 Hz) (T_C = +65°C) (1.5 ms pulse @ T_J = 100°C Preceeded and followed by no current or Voltage	I_{TSM}	 240 560	Amp
Circuit Fusing Considerations (T_J = -40 to +100°C) (t = 1.0 to 8.3 ms)	I^2t	235	A^2s
*Peak Gate Power	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GFM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
*Stud Torque	–	30	in. lb.

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

*Indicates JEDEC Registered Data.

(1) Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.



STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE
STUD-ISOLATED

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	2.03	2.41	0.080	0.095
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	1.40	1.65	0.055	0.065

CASE 235

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
* Peak Forward Blocking Voltage (T_J = 100°C)	V_{RRM}				Volts
2N6167		100	–	–	
2N6168		200	–	–	
2N6169		400	–	–	
2N6170		600	–	–	
* Peak Forward Blocking Current (Rated V_{DRM}, gate open, T_J = 100°C)	I_{DRM}				mA
2N6167		–	1.0	2.0	
2N6168		–	1.0	2.5	
2N6169		–	1.0	3.0	
2N6170		–	1.0	4.0	
* Peak Reverse Blocking Current (Rated V_{RRM}, gate open, T_J = 100°C)	I_{RRM}				mA
2N6167		–	1.0	2.0	
2N6168		–	1.0	2.5	
2N6169		–	1.0	3.0	
2N6170		–	1.0	4.0	
*Peak Forward "On" Voltage (I_{TM} = 41 A Peak)	V_{TM}	–	1.5	1.7	Volts
Gate Trigger Current, Continuous dc *T_C = -40°C (V_{AK} = 12 V, R_L = 24 Ω) T_C = 25°C	I_{GT}	– –	– 2.1	75 40	mA
Gate Trigger Voltage, Continuous dc (V_{AK} = 12 V, R_L = 24 Ω) *T_C = -40°C T_C = 25°C	V_{GT}	– –	0.8 0.63	2.5 1.6	Volts
Holding Current *T_C = -40°C (V_{AK} = 12 V, Gate Open) T_C = 25°C Peak Initiating On-State Current = 200 mA	I_H	– –	– 3.5	90 50	mA
*Turn-On Time (t_d + t_r) (I_{TM} = 41 Adc, Rated V_{DRM}) I_{GT} = 200 mAdc, Rise Time = 0.05 μs, Pulse Width = 10 μs)	t_{on}	–	–	1.0	μs
Turn-Off Time (I_{TM} = 10 A, I_R = 10 A) (I_{TM} = 10 A, I_R = 10 A, T_J = 100°C)	t_{off}	– –	15 25	– –	μs
Forward Voltage Application Rate (T_J = 100°C)	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data

FIGURE 1 – AVERAGE CURRENT DERATING

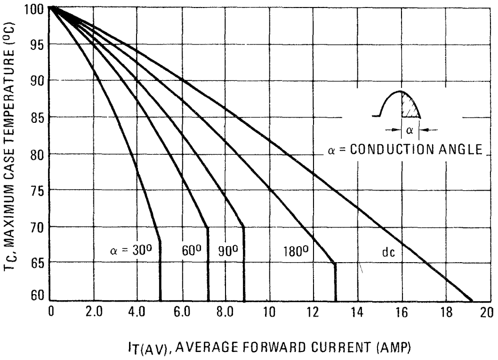


FIGURE 2 – POWER DISSIPATION

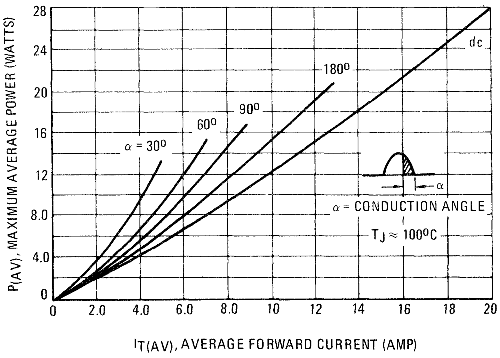


FIGURE 3 – MAXIMUM ON-STATE CHARACTERISTICS

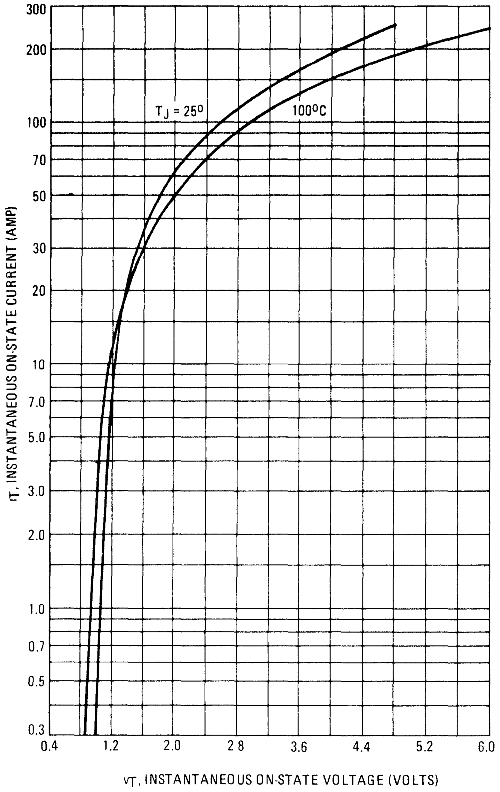


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

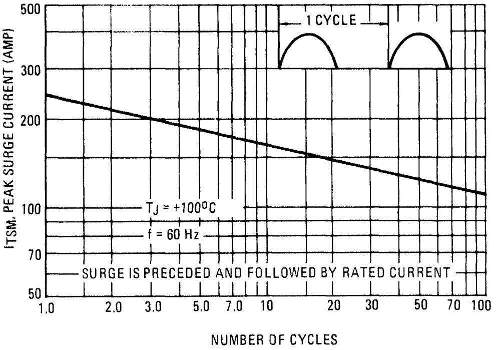


FIGURE 5 – CHARACTERISTICS AND SYMBOLS

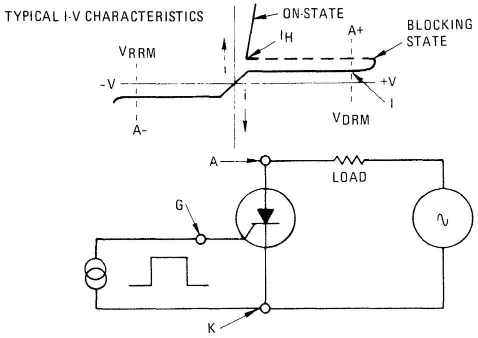


FIGURE 6 – THERMAL RESPONSE

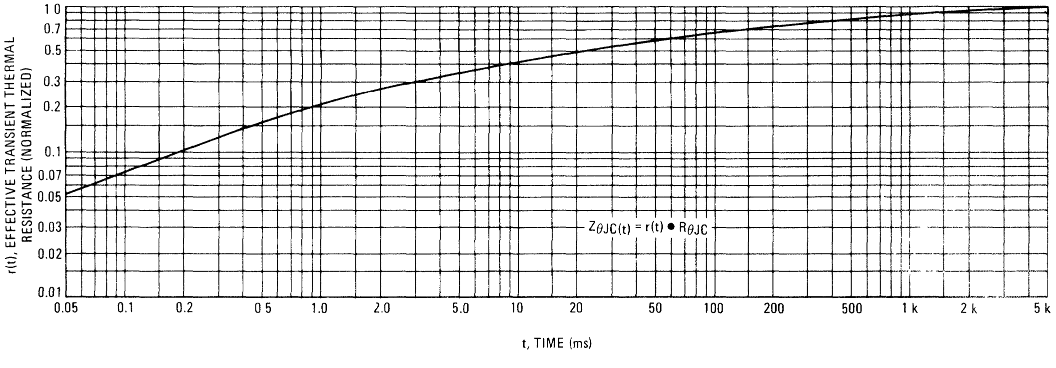


FIGURE 7 – TYPICAL GATE TRIGGER CURRENT

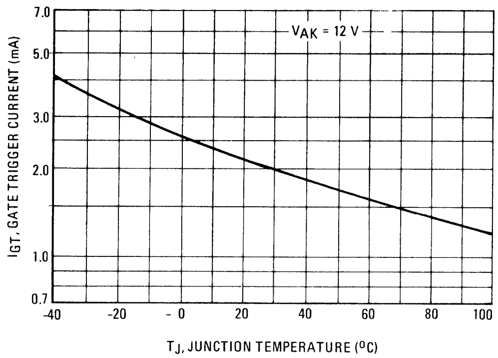


FIGURE 8 – TYPICAL GATE TRIGGER VOLTAGE

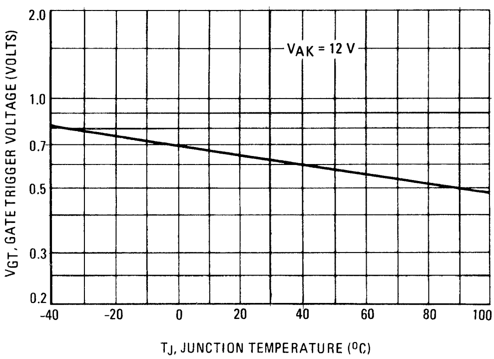
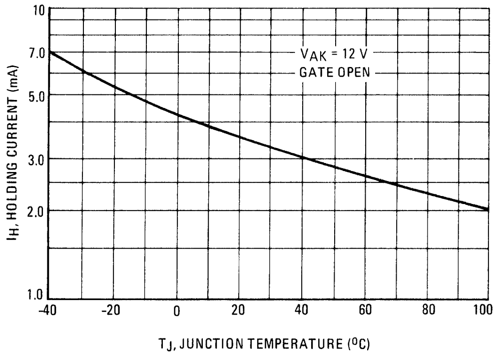


FIGURE 9 – TYPICAL HOLDING CURRENT



Selected Thyristor-Trigger Application Notes

AN-240	SCR Power Control Fundamentals
AN-295	Suppressing RFI in Thyristor Circuits
AN-422	Testers for Thyristors and Trigger Diodes
AN-453	Zero Point Switching Techniques

To obtain copies of these notes list the AN number(s) on your company letterhead and send your request to:

Technical Information Center
Motorola Semiconductor Products, Inc.
P.O. Box 20924
Phoenix, Arizona 85036

2N6171 thru 2N6174 (SILICON)

For Specifications, See 2N3870, Volume I.

2N6186 thru 2N6189 (SILICON)

MEDIUM-POWER PNP SILICON TRANSISTORS

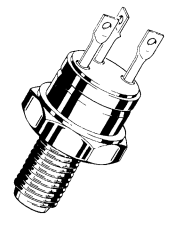
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)} = 1.2$ Vdc (Max) @ $I_C = 10$ Adc
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact, High Dissipation TO-59 Case
- Isolated Collector Configuration
- 2N6186 thru 2N6189 Complement to NPN 2N5346 thru 2N5349

10 AMPERE
POWER TRANSISTORS

PNP SILICON

80-100 VOLTS
60 WATTS



*MAXIMUM RATINGS

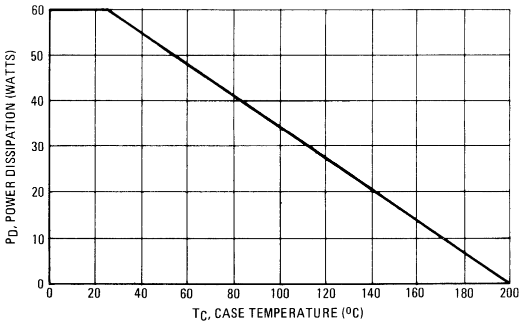
Rating	Symbol	2N6186 2N6187	2N6188 2N6189	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous	I_C	10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ $T_C = 25^{\circ}C$ Derate above 25°C	P_D	60 343		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

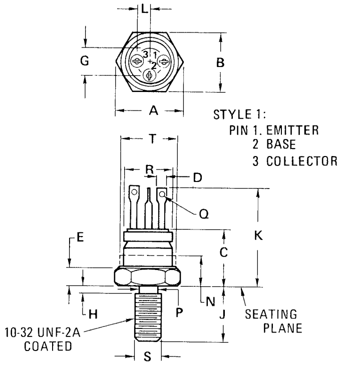
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.91	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER-TEMPERATURE DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	10.77	11.10	0.424	0.437
C	8.13	11.89	0.320	0.468
E	2.29	3.81	0.090	0.150
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	10.16	11.56	0.400	0.455
K	14.48	19.38	0.570	0.763
L	2.29	2.79	0.090	0.110
N	–	6.35	–	0.250
P	4.14	4.80	0.163	0.189
Q	1.02	1.65	0.040	0.065
R	8.08	9.65	0.318	0.380
S	4.212	4.310	0.1658	0.1697
T	9.65	11.10	0.380	0.437

All JEDEC dimensions and notes apply
Collector isolated from case

CASE 160-03
(TO-59)

2N6186 thru 2N6189 (continued)

*** ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

OFF CHARACTERISTICS

Characteristic		Fig. No.	Symbol	Min	Max	Unit
Collector-Emitter Sustaining Voltage (1)		–	$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6186, 87			80	–	
	2N6188, 89			100	–	
Collector Cutoff Current		–	I_{CEO}			µAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N6186, 87			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N6188, 89			–	100	
Collector Cutoff Current		12	I_{CEX}			µAdc
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6186, 87			–	10	
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6188, 89			–	10	
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6186, 87			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6188, 89			–	1.0	
Collector Cutoff Current		–	I_{CBO}			µAdc
(V_{CB} = Rated V_{CB}, I_E = 0)				–	10	
Emitter Cutoff Current		–	I_{EBO}			µAdc
(V_{BE} = 6 0 Vdc, I_C = 0)				–	100	

ON CHARACTERISTICS (1)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
DC Current Gain		8	h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88			30	–	
	2N6187, 89			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88			30	120	
	2N6187, 89			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88			20	–	
	2N6187, 89			40	–	
Collector-Emitter Saturation Voltage		9, 10, 11	$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 10 Adc, I_B = 1.0 Adc)				–	1.2	
Base-Emitter Saturation Voltage		10, 11	$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 10 Adc, I_B = 1.0 Adc)				–	2.0	

DYNAMIC CHARACTERISTICS

Characteristic	Fig. No.	Symbol	Min	Max	Unit
Current-Gain-Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{Test} = 10 MHz)	–	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	7	C_{ob}	–	300	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)	7	C_{ib}	–	1250	pF

SWITCHING CHARACTERISTICS

Delay Time	(V_{CC} = 40 Vdc, $V_{BE(off)}$ = 3.0 Vdc,	2, 3	t_d	–	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 200 mAdc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	–	2.0	µs
Fall Time	I_{B1} = I_{B2} = 200 mAdc)		t_f	–	200	ns

*Indicates JEDEC Registered Data

(1) Pulse Test Pulse Width ≈ 300 µs, Duty Cycle ≈ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{Test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

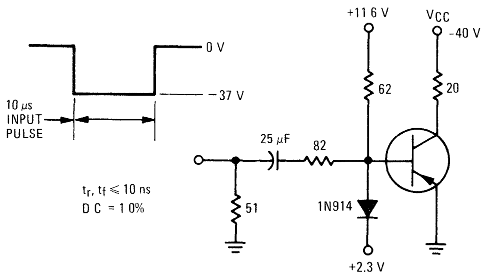


FIGURE 3 – TURN-ON TIME

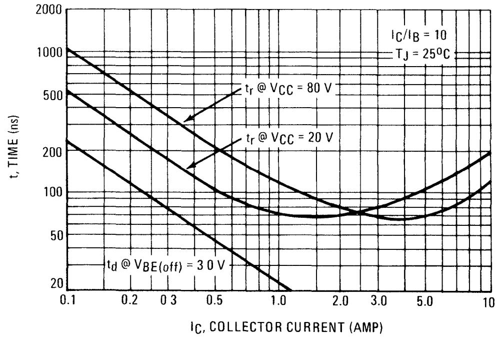


FIGURE 4 – THERMAL RESPONSE

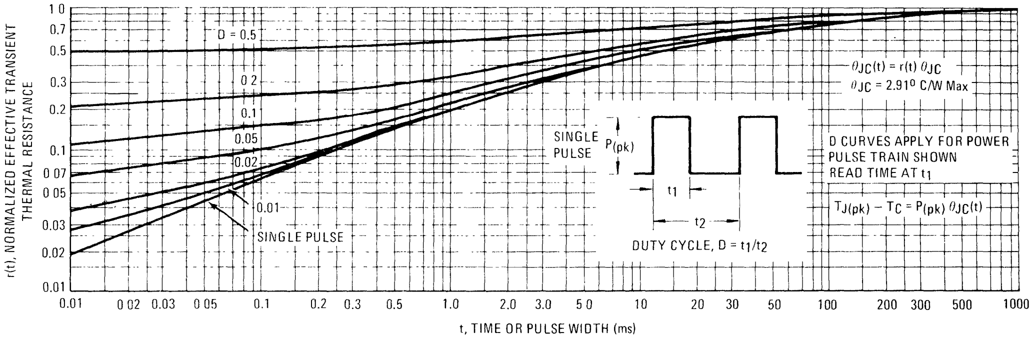
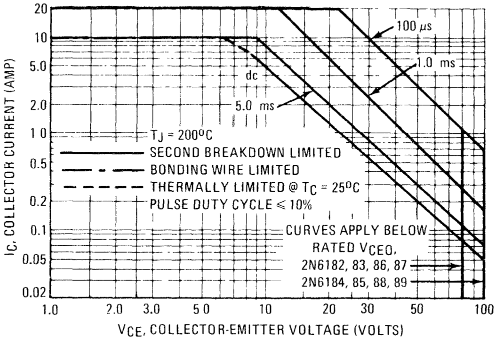


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitaitons imposed by second breakdown.

FIGURE 6 – TURN OFF TIME

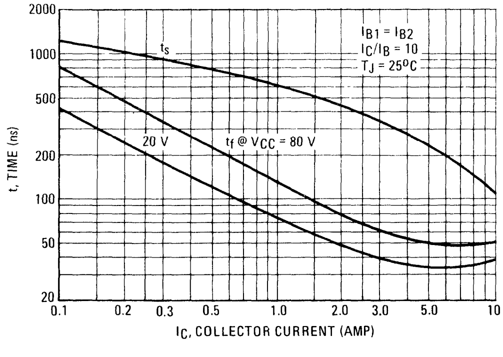


FIGURE 7 – CAPACITANCE versus VOLTAGE

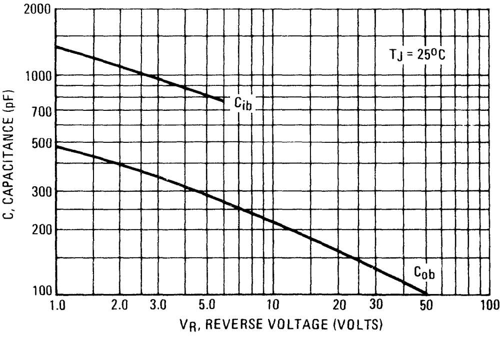


FIGURE 8 – DC CURRENT GAIN

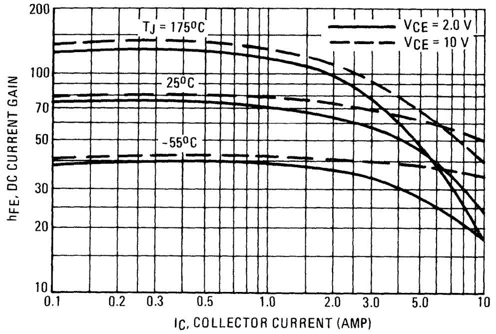


FIGURE 9 – COLLECTOR SATURATION REGION

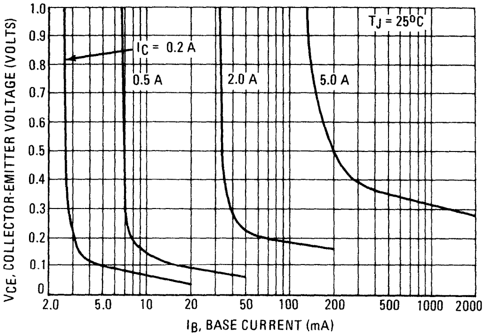


FIGURE 10 – "ON" VOLTAGES

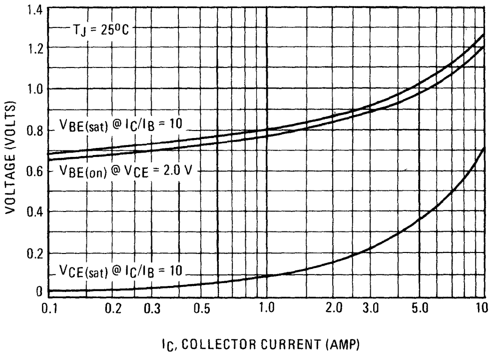


FIGURE 11 – TEMPERATURE COEFFICIENTS

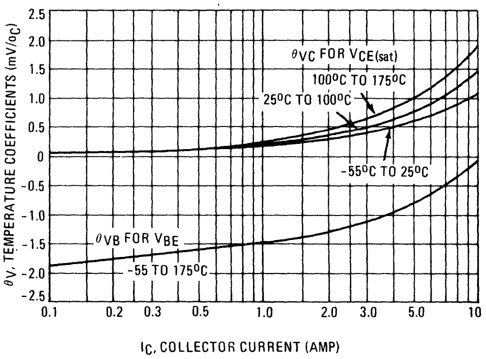


FIGURE 12 – COLLECTOR CUT-OFF REGION

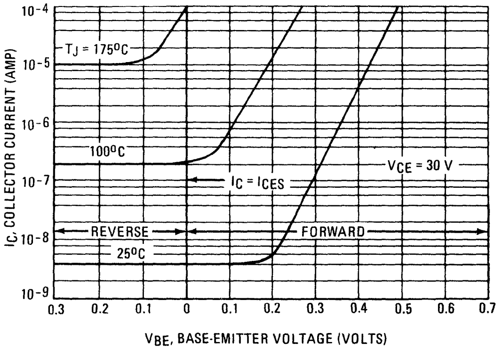
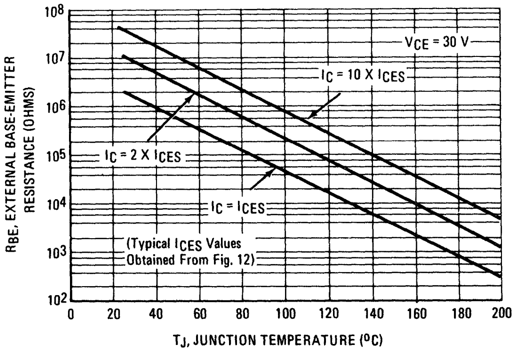


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N6190 (SILICON)
thru
2N6193

MEDIUM-POWER PNP SILICON TRANSISTORS

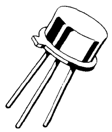
. . . designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 5.0 Amp
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-39 Case for Critical Space Limited Applications
- Complement to NPN 2N5336 thru 2N5339

5 AMPERE
POWER TRANSISTORS

PNP SILICON

80-100 VOLTS
10 WATTS



*MAXIMUM RATINGS

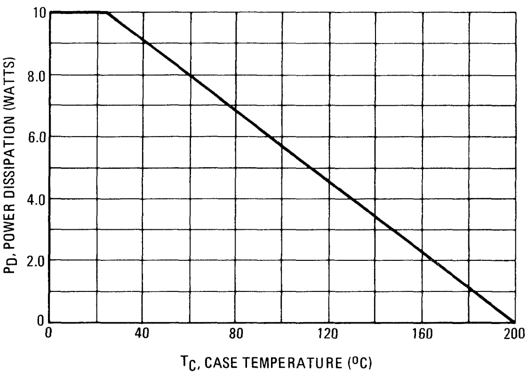
Rating	Symbol	2N6190 2N6191	2N6192 2N6193	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C	P_D	10		Watts
Derate above 25°C		57.1		mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

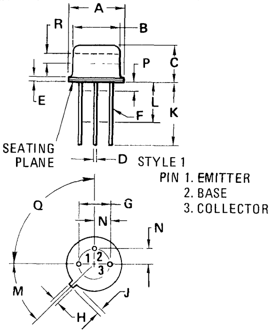
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER-TEMPERATURE DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0 370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0 016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

*** ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6190, 2N6191			80	–	
	2N6192, 2N6193			100	–	
Collector Cutoff Current		–	I_{CEO}			µAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N6190, 2N6191			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N6192, 2N6193			–	100	
Collector Cutoff Current		12	I_{CEX}			µAdc
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1 5 Vdc)	2N6190, 2N6191			-	10	
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6192, 2N6193			–	10	
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1 5 Vdc, T_C = 150°C)	2N6190, 2N6191			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1 5 Vdc, T_C = 150°C)	2N6192, 2N6193			–	1 0	
Collector Cutoff Current		–	I_{CBO}			µAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N6190, 2N6191			–	10	
(V_{CB} = 100 Vdc, I_E = 0)	2N6192, 2N6193			–	10	
Emitter Cutoff Current		–	I_{EBO}			µAdc
(V_{BE} = 6.0 Vdc, I_C = 0)				–	100	
ON CHARACTERISTICS (1)						
DC Current Gain		8	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 2 0 Vdc)	2N6190, 2N6192			30	–	
	2N6191, 2N6193			60	–	
(I_C = 2 0 Adc, V_{CE} = 2 0 Vdc)	2N6190, 2N6192			30	120	
	2N6191, 2N6193			60	240	
(I_C = 5 0 Adc, V_{CE} = 2 0 Vdc)	2N6190, 2N6192			20	–	
	2N6191, 2N6193			40	–	
Collector-Emitter Saturation Voltage		9,10,11	$V_{CE(sat)}$			Vdc
(I_C = 2 0 Adc, I_B = 0.2 Adc)				–	0 7	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				–	1 2	
Base-Emitter Saturation Voltage		10,11	$V_{BE(sat)}$			Vdc
(I_C = 2 0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				–	1 8	
DYNAMIC CHARACTERISTICS						
Current-Gain-Bandwidth Product (2)		–	f_T			MHz
(I_C = 0 5 Adc, V_{CE} = 10 Vdc, f_{Test} = 10 MHz)				30	–	
Output Capacitance		7	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)				–	300	
Input Capacitance		7	C_{ib}			pF
(V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)				–	1250	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{BE(off)}$ = 3.0 Vdc, I_C = 2.0 Adc, I_{B1} = 0 2 Adc)	2,3	t_d	–	100	ns
Rise Time			t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2 0 Adc, I_{B1} = I_{B2} = 0 2 Adc)	2,6	t_s	–	2 0	µs
Fall Time			t_f	–	200	ns

*Indicates JEDEC Registered Data

(1) Pulse Test Pulse Width ≤ 300 µs, Duty Cycle ≤ 2 0%

(2) $f_T = |h_{fe}| \cdot f_{Test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

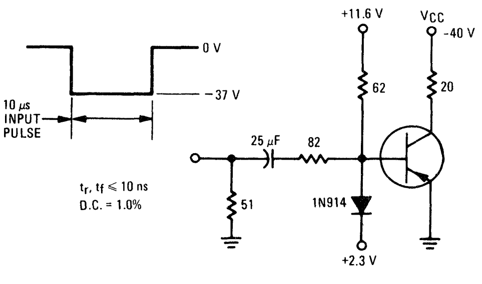


FIGURE 3 – TURN ON TIME

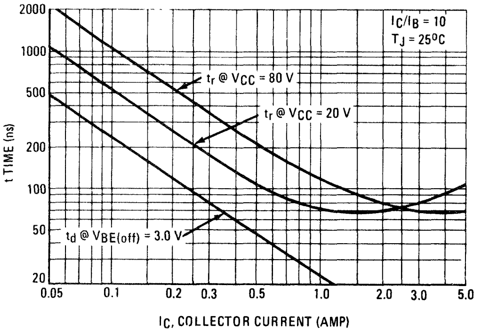


FIGURE 4 – THERMAL RESPONSE

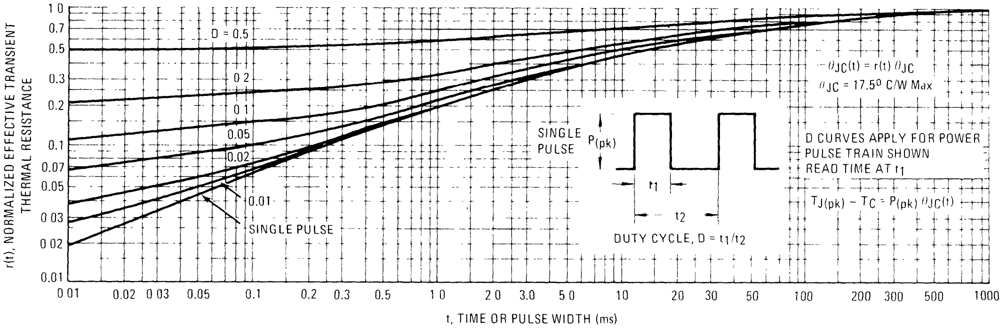
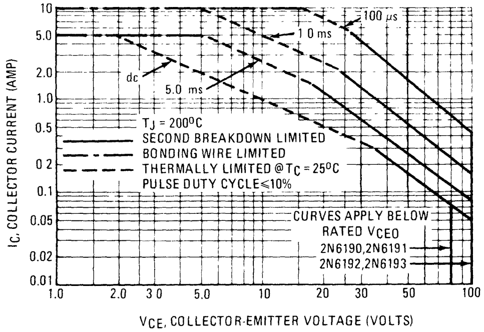


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor. average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitaitons imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

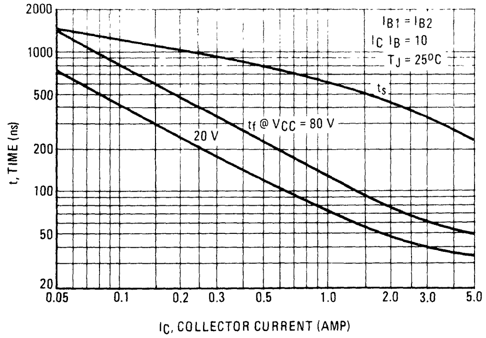


FIGURE 7 – CAPACITANCE versus VOLTAGE

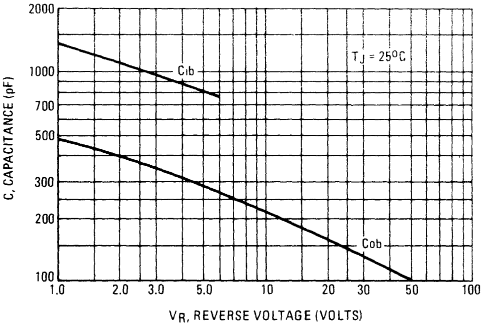


FIGURE 8 – DC CURRENT GAIN

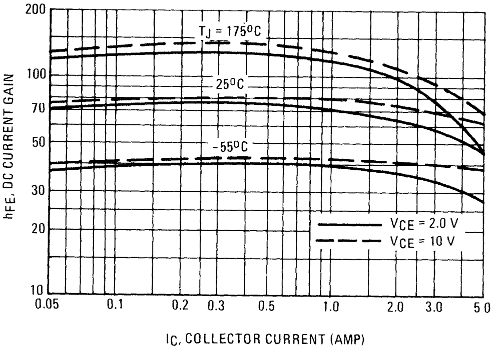


FIGURE 9 – COLLECTOR SATURATION REGION

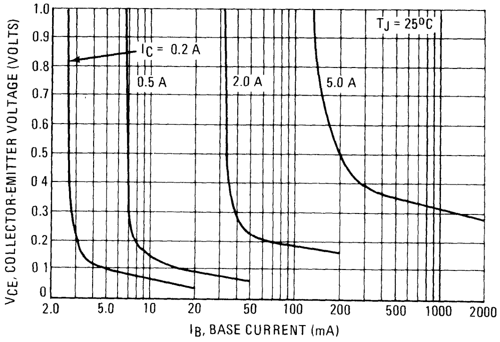


FIGURE 10 – ON VOLTAGES

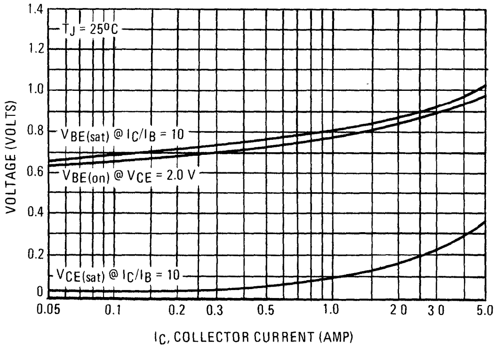


FIGURE 11 – TEMPERATURE COEFFICIENTS

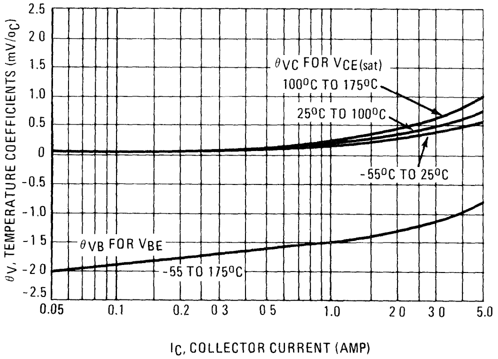


FIGURE 12 – COLLECTOR CUT-OFF REGION

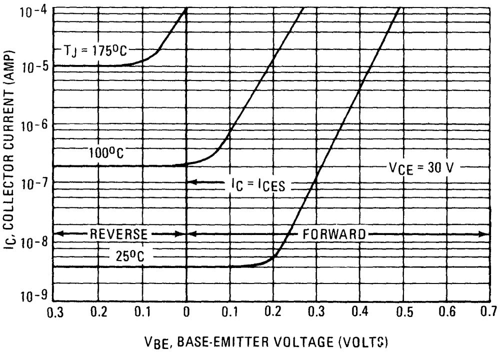
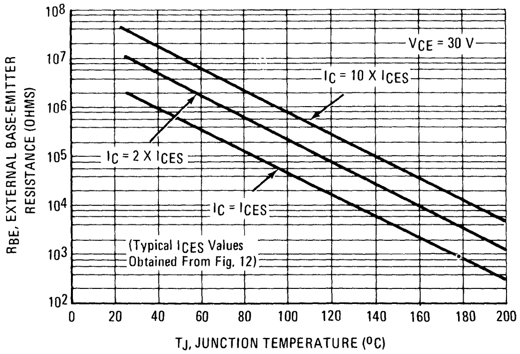


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N 6226 (SILICON)
2N 6227
2N 6228

HIGH-VOLTAGE HIGH-POWER PNP SILICON TRANSISTORS

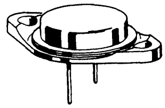
. . . designed for use in high-power audio amplifier applications and high-voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N6226
  = 120 Vdc (Min) – 2N6227
  = 140 Vdc (Min) – 2N6228
- DC Current Gain – @ I_C = 3.0 Adc
  h_{FE} = 25 (Min) – 2N6226
  = 20 (Min) – 2N6227
  = 15 (Min) – 2N6228
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 3.0 Adc
- Complement to NPN Transistors 2N5758, 2N5759, 2N5760

6 AMPERE
POWER TRANSISTORS

PNP SILICON

100-120-140 VOLTS
150 WATTS



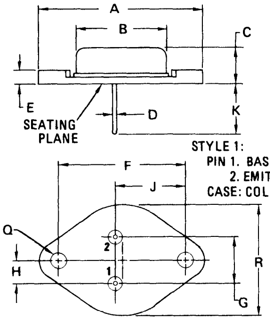
*MAXIMUM RATINGS

Rating	Symbol	2N6226	2N6227	2N6228	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 6.0 → ← 10 →			Adc
Base Current	I_B	← 4.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 150 → ← 0.857 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data.



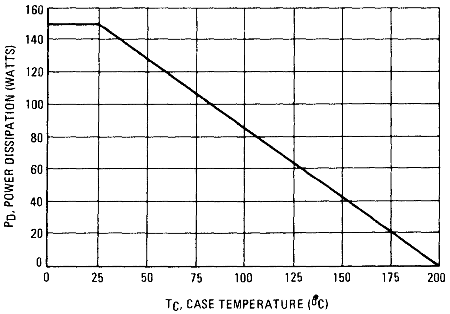
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01

NOTE:
1. DIM "Q" IS DIA. Collector connected to case.

FIGURE 1 – POWER DERATING



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

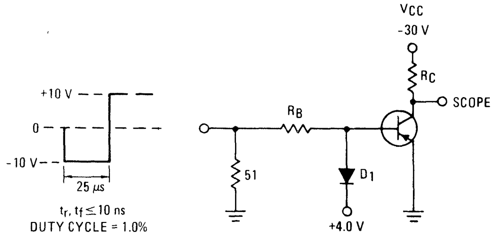
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0) 2N6226 2N6227 2N6228	$V_{CEO(sus)}$	 100 120 140	 – – –	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) 2N6226 (V_{CE} = 60 Vdc, I_B = 0) 2N6227 (V_{CE} = 70 Vdc, I_B = 0) 2N6228	I_{CEO}	 – – –	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 – –	 1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc) 2N6226 2N6227 2N6228 (I_C = 6.0 Adc, V_{CE} = 2.0 Vdc All Types	h_{FE}	 25 20 15 5.0	 100 80 60 –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc) (I_C = 6.0 Adc, I_B = 1.2 Adc)	$V_{CE(sat)}$	 – –	 1.0 2.0	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)	f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	450	pF
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	15	–	– –

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq$300 µs, Duty Cycle$\leq$2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE IB ≈100 mA
MSD6100 USED BELOW IB ≈100 mA

FIGURE 3 – TURN-ON TIME

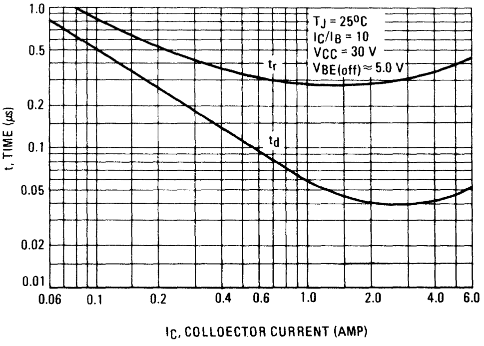


FIGURE 4 – THERMAL RESPONSE

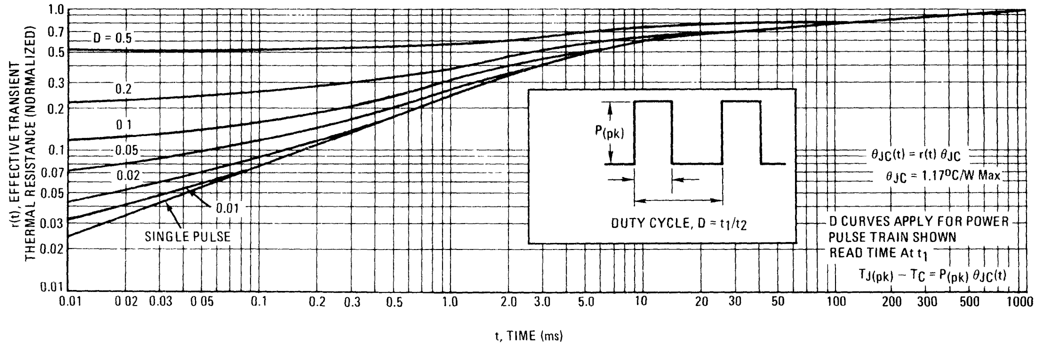
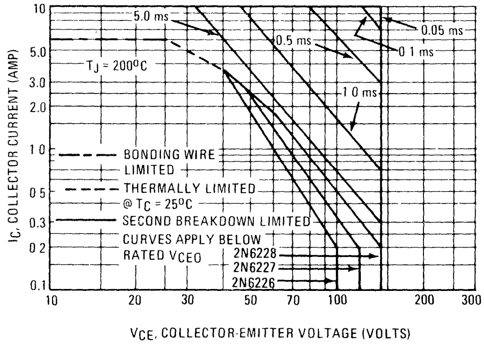


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

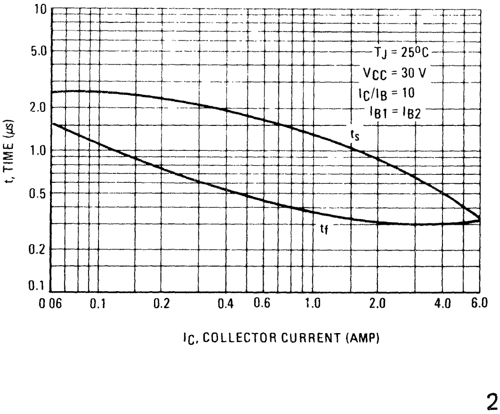


FIGURE 7 – CAPACITANCE

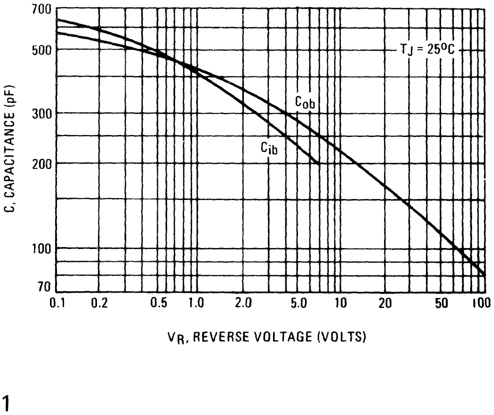


FIGURE 8 – DC CURRENT GAIN

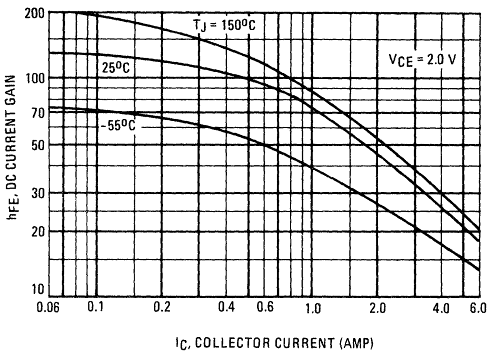


FIGURE 9 – COLLECTOR SATURATION REGION

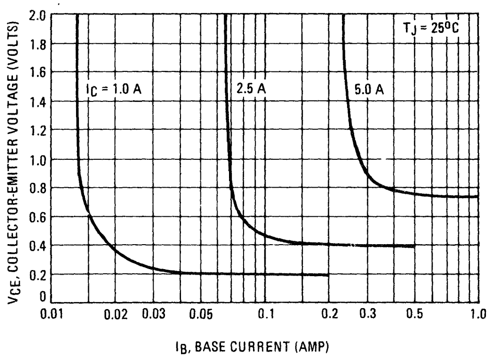


FIGURE 10 – "ON" VOLTAGES

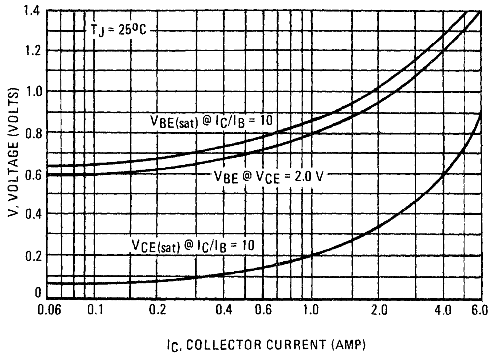


FIGURE 11 – TEMPERATURE COEFFICIENTS

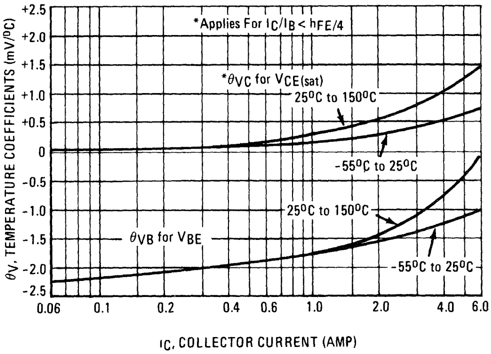


FIGURE 12 – COLLECTOR CUT-OFF REGION

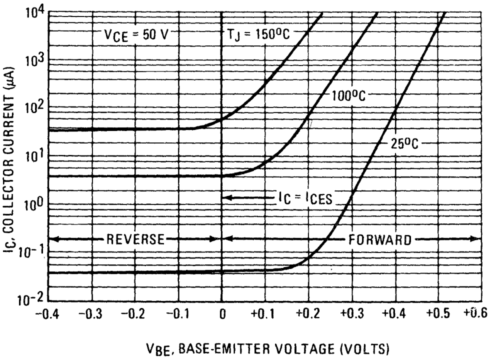
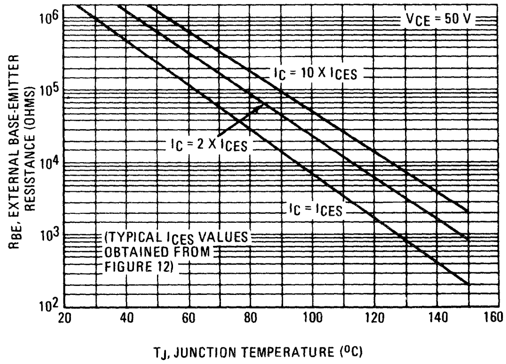


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N6229 (SILICON)
2N6230
2N6231

HIGH-VOLTAGE HIGH-POWER PNP SILICON TRANSISTORS

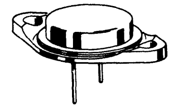
. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

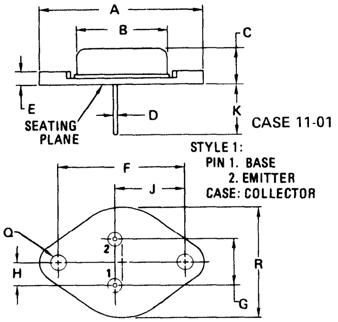
- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N6229
  = 120 Vdc (Min) – 2N6230
  = 140 Vdc (Min) – 2N6231
- High DC Current Gain — @ I_C = 5.0 Adc
  h_{FE} = 25 (Min) – 2N6229
  = 20 (Min) – 2N6230
  = 15 (Min) – 2N6231
- Low Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 7.5 Adc
- Complements to NPN 2N5632, 2N5633 and 2N5634

10 AMPERE POWER TRANSISTORS

PNP SILICON

100, 120, 140 VOLTS
150 WATTS





CASE 11-01

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

Collector connected to case.

*MAXIMUM RATINGS

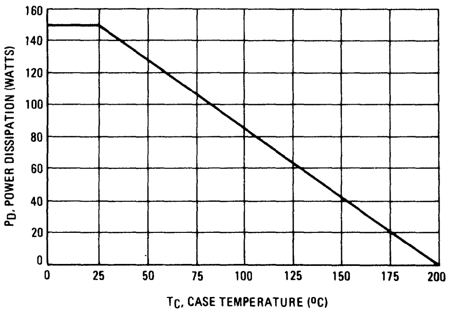
Rating	Symbol	2N6229	2N6230	2N6231	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	7.0			Vdc
Collector Current — Continuous Peak	I_C	10 15			Adc
Base Current	I_B	5.0			Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	150 0.857			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



2N6229, 2N6230, 2N6231 (continued)

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

OFF CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6229		100	–	
	2N6230		120	–	
	2N6231		140	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6229		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6230		–	1.0	
(V_{CE} = 70 Vdc, I_B = 0)	2N6231		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6229		–	1.0	
(V_{CE} = 120 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6230		–	1.0	
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6231		–	1.0	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6229		–	5.0	
(V_{CE} = 120 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6230		–	5.0	
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6231		–	5.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 100 Vdc, I_E = 0)	2N6229		–	1.0	
(V_{CB} = 120 Vdc, I_E = 0)	2N6230		–	1.0	
(V_{CB} = 140 Vdc, I_E = 0)	2N6231		–	1.0	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 7.0 Vdc, I_C = 0)			–	1.0	

ON CHARACTERISTICS (1)

Characteristic		Symbol	Min	Max	Unit
DC Current Gain		h_{FE}			–
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N6229		25	100	
	2N6230		20	80	
	2N6231		15	60	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	All		5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 7.5 Adc, I_B = 0.75 Adc)			–	1.0	
(I_C = 10 Adc, I_B = 2.0 Adc)			–	2.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 7.5 Adc, I_B = 0.75 Adc)			–	2.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)			–	1.5	

DYNAMIC CHARACTERISTICS

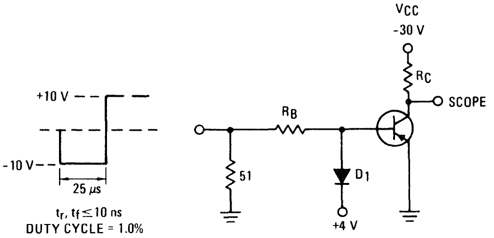
Characteristic	Symbol	Min	Max	Unit
Current-Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc), f_{test} = 0.5 MHz)	f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	600	pF
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	15	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq$ 300 µs, Duty Cycle = 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

FIGURE 3 – TURN-ON TIME

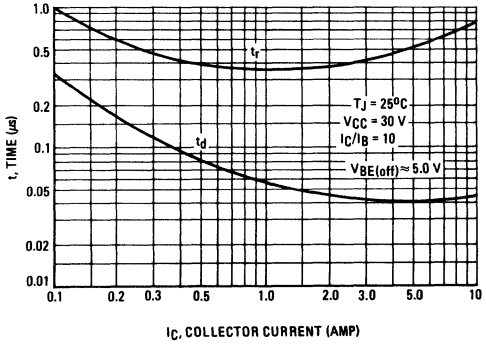


FIGURE 4 – THERMAL RESPONSE

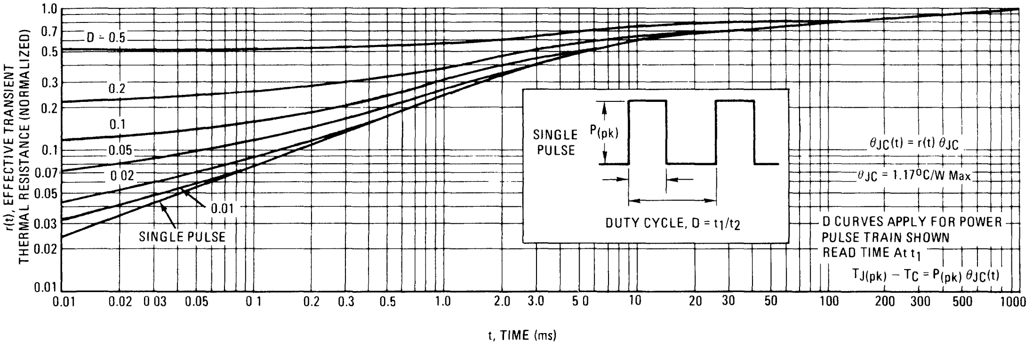
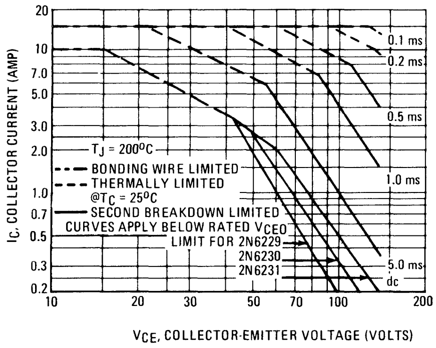


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

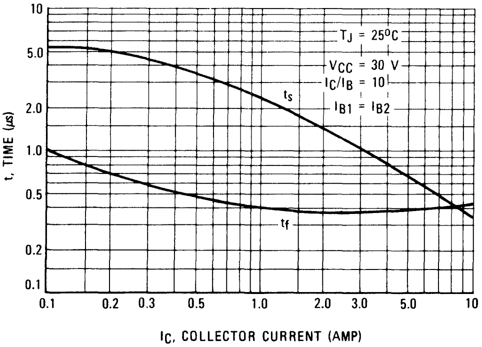


FIGURE 7 – CAPACITANCE

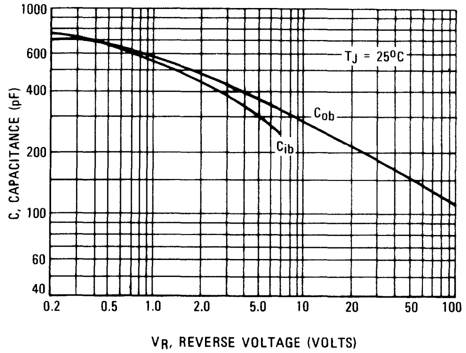


FIGURE 8 – DC CURRENT GAIN

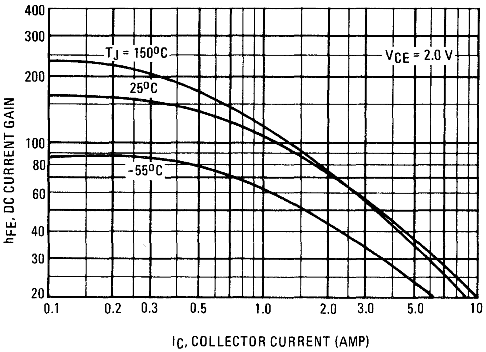


FIGURE 9 – COLLECTOR SATURATION REGION

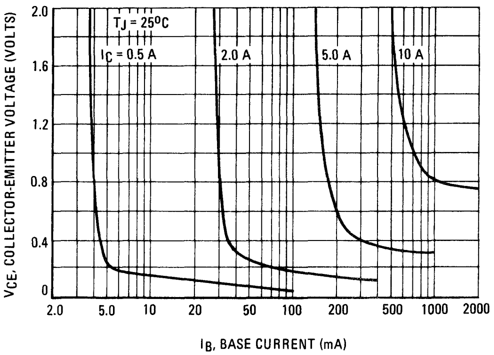


FIGURE 10 – "ON" VOLTAGES

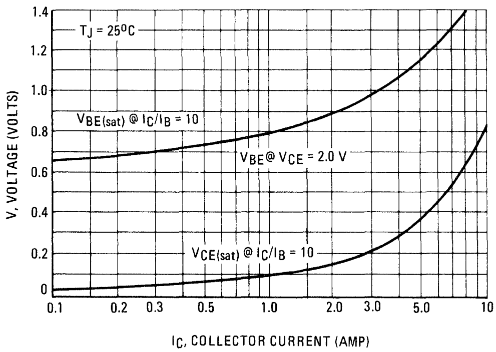


FIGURE 11 – TEMPERATURE COEFFICIENTS

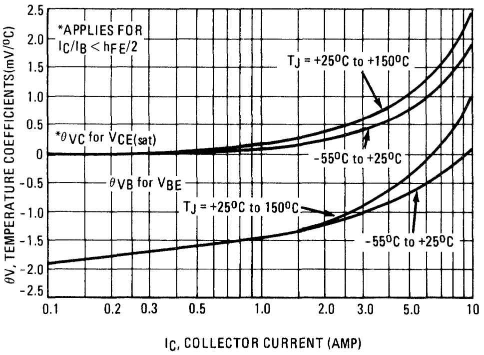


FIGURE 12 – COLLECTOR CUT-OFF REGION

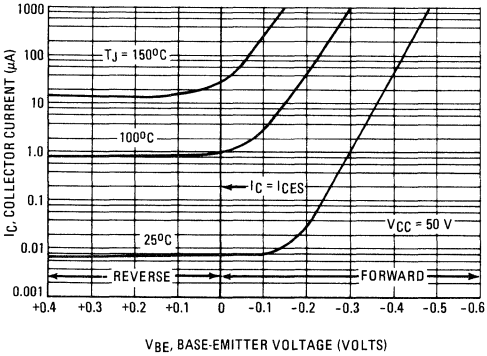
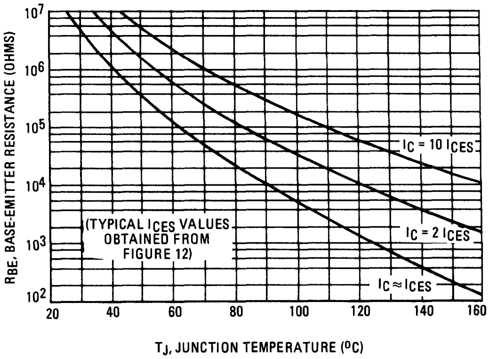


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N6233 (SILICON)
2N6234
2N6235

HIGH VOLTAGE NPN SILICON TRANSISTORS

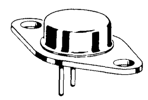
. . . designed for high reliability switching and pin diode driver applications **[SAFEGUARD]**

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 225 Vdc – 2N6233
  275 Vdc – 2N6234
  325 Vdc – 2N6235
- DC Current Gain – h_{FE} = 25 to 125 – I_C = 1.0 Adc
- Low Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 1.0 Adc
- High Frequency Response – f_T = 20 MHz (Min)
- Fast Switching Times @ 1.0 Adc –
  t_r = 0.5 μs (Max)
  t_s = 3.5 μs (Max)
  t_f = 0.5 μs (Max)
- Environment Test Data Available

5 AMPERE
POWER TRANSISTORS

NPN SILICON

225,275,325 VOLTS
50 WATTS



*MAXIMUM RATINGS

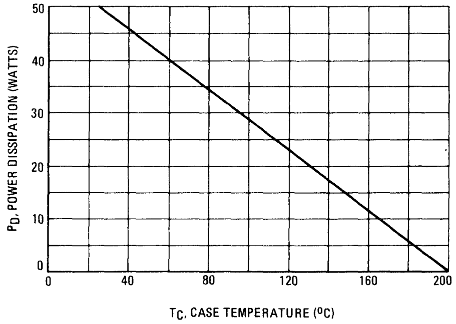
Rating	Symbol	2N6233	2N6234	2N6235	Unit
Collector-Emitter Voltage	V_{CEO}	225	275	325	Vdc
Collector-Base Voltage	V_{CB}	250	300	350	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous	I_C	← 5.0 →			Adc
Peak		← 10 →			
Base Current	I_B	← 2.0 →			Adc
Total Device Dissipation @ T_C = 25°C	P_D	← 50 →			Watts
Derate above 25°C		← 0.286 →			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

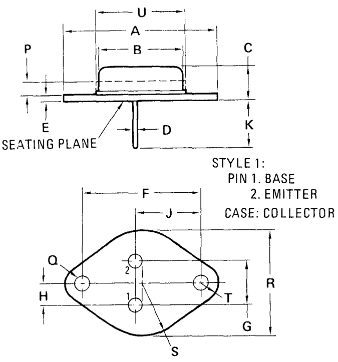
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER TEMPERATURE DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5 33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

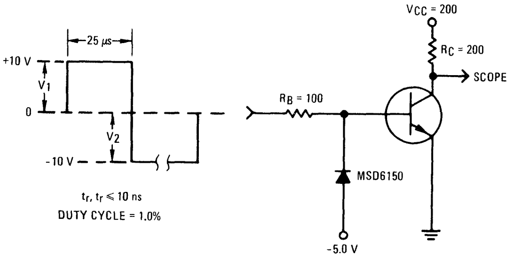
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 20 mAdc, I_B = 0)	2N6233		225	–	
	2N6234		275	–	
	2N6235		325	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 225, I_B = 0)	2N6233		–	1.0	
(V_{CE} = 275, I_B = 0)	2N6234		–	1.0	
(V_{CE} = 325, I_B = 0)	2N6235		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6233		–	1.0	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6234		–	1.0	
(V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6235		–	1.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 250 Vdc, I_E = 0)	2N6233		–	0.1	
(V_{CB} = 300 Vdc, I_E = 0)	2N6234		–	0.1	
(V_{CB} = 350 Vdc, I_E = 0)	2N6235		–	0.1	
Emitter Cutoff Current (V_{BE}= 6.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.1 Adc, V_{CE} = 5.0 Vdc)			25	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			25	125	
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)			–	0.5	
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	2.5	
Base Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)			–	1.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	2.0	
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (2) (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	20	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	250	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_B = 0.1 Adc)		t_r	–	0.5	µs
Storage Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)		t_s	–	3.5	µs
Fall Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)		t_f	–	0.5	µs

*Indicates JEDEC Registered Data

(1) Pulse Test Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR INFORMATION ON FIGURES 3 and 6 R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS, D_1 DISCONNECTED AND V_2 REDUCED TO 5 VOLTS FOR t_d MEASUREMENT.

FIGURE 3 – TURN-ON TIME

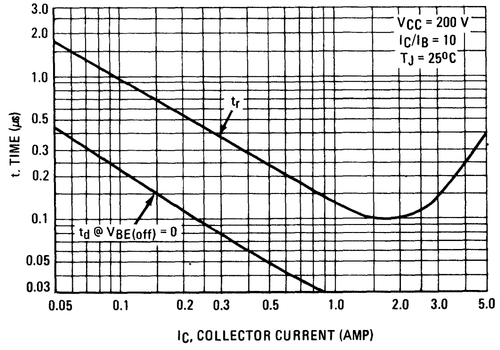


FIGURE 4 – THERMAL RESPONSE

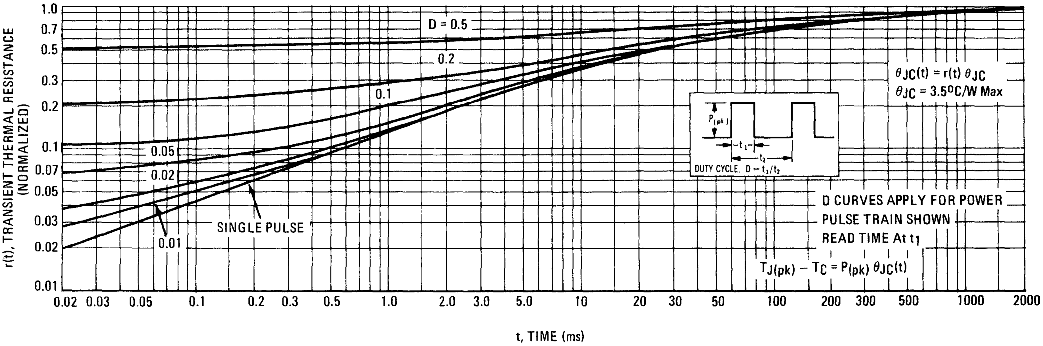


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA

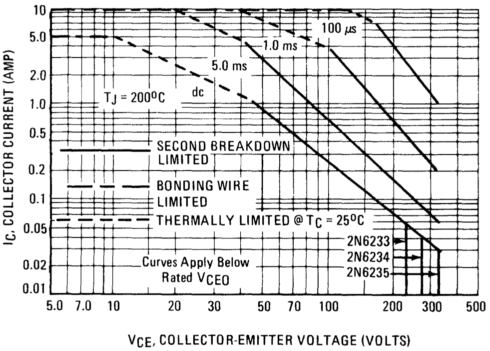


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FIGURE 6 – TURN-OFF TIME

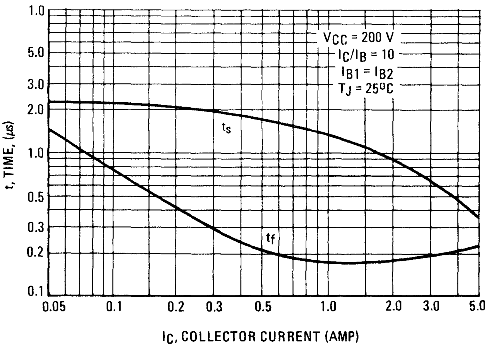


FIGURE 7 – CAPACITANCES

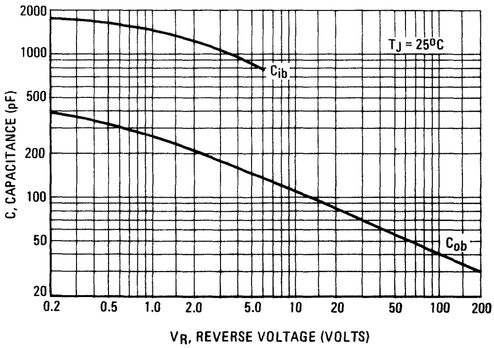


FIGURE 8 — DC CURRENT GAIN

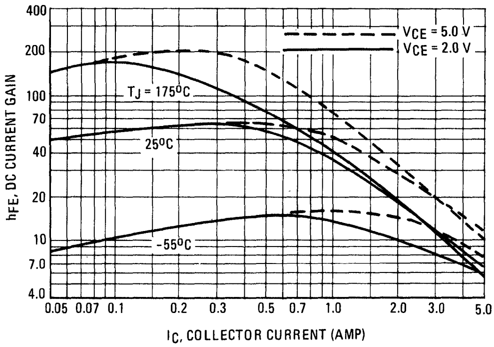


FIGURE 9 — COLLECTOR SATURATION REGION

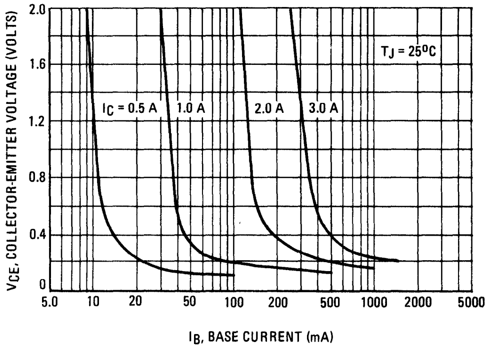


FIGURE 10 — "ON" VOLTAGES

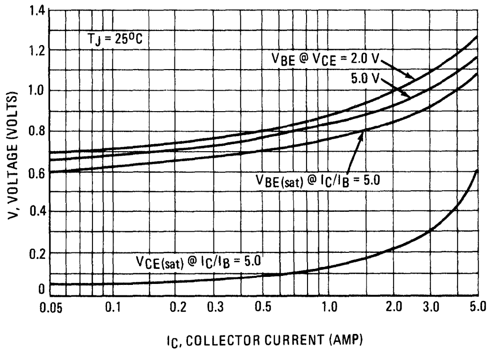


FIGURE 11 — TEMPERATURE COEFFICIENTS

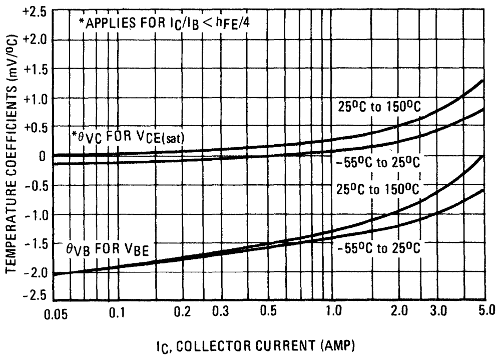


FIGURE 12 — COLLECTOR CUT-OFF REGION

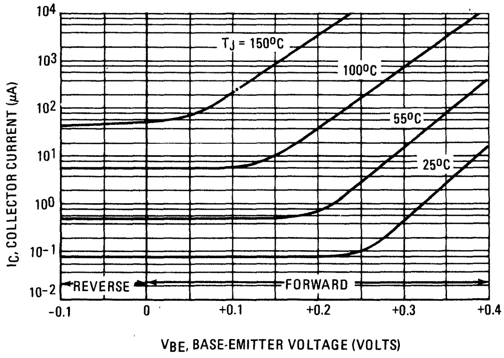
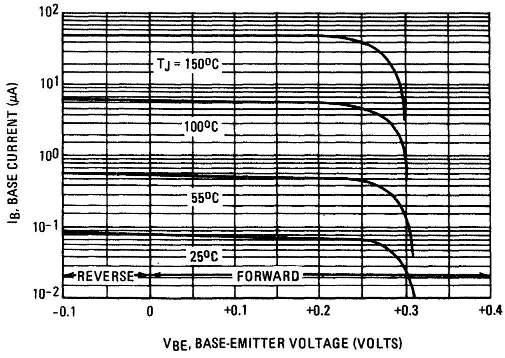
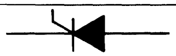


FIGURE 13 — BASE CUT-OFF REGION



2N6236 thru 2N6241 (SILICON)



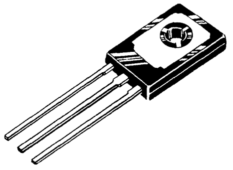
PLASTIC THYRISTORS (PLASTIC SILICON CONTROLLED RECTIFIERS)

. . . PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Recommended Electrical Replacement for C 106

THYRISTORS

4.0 AMPERES RMS
30 thru 600 VOLTS



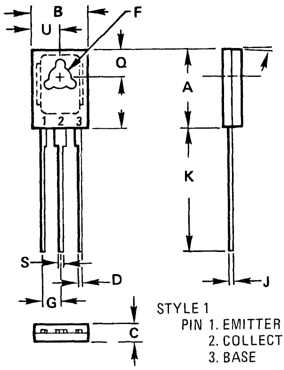
MAXIMUM RATINGS (T_J = 100°C unless otherwise noted.)

Rating		Symbol	Value	Unit
*Repetitive Peak Forward and Reverse Blocking Voltage (Note 1)		V_{DRM} V_{RRM}		Volts
(1/2 Sine Wave)	2N6236		30	
(Gate Open,	2N6237		50	
T_J = -40 to +110°C)	2N6238		100	
	2N6239		200	
	2N6240		400	
	2N6241		600	
*Non-Repetitive Peak Reverse Blocking Voltage		V_{RSM}		Volts
(1/2 Sine Wave,	2N6236		50	
Gate Open,	2N6237		100	
T_J = -40 to +110°C)	2N6238		150	
	2N6239		250	
	2N6240		450	
	2N6241		650	
*Average On-State Current		$I_{T(AV)}$		Amp
(T_C = -40 to +90°C)			2.6	
(T_C = +100°C)			1.6	
*Surge On-State Current		I_{TSM}		Amp
(1/2 Sine Wave, 60 Hz, T_C = +90°C)			25	
(1/2 Sine Wave, 1.5 ms, T_C = +90°C)			35	
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)		I^2t	2.6	A^2s
*Peak Gate Power (Pulse Width = 10 μs)		P_{GM}	0.5	Watts
*Average Gate Power (t = 8.3 ms)		$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current		I_{GM}	0.2	Amp
Peak Reverse Gate Voltage		V_{RGM}	6.0	Volts
*Operating Junction Temperature Range		T_J	-40 to +110	°C
*Storage Temperature Range		T_{stg}	-40 to +150	°C
Mounting Torque (Note 2)		—	6.0	in.lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	3.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	—	75	°C/W

*Indicates JEDEC Registered Data.



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	11.43	0.390	0.450
B	6.86	8.38	0.270	0.330
C	1.78	3.30	0.070	0.130
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.29 BSC		0.090 BSC	
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
Q	3.30	4.45	0.130	0.175
S	0.64	0.89	0.025	0.035
U	3.81 NOM		0.150 NOM	

CASE 77-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms.)

Characteristics	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (Note 1) (Rated V_{DRM}, T_J = 110°C)	I_{DRM}	–	–	200	μA
*Peak Reverse Blocking Current (Note 1) (Rated V_{RRM}, T_J = 110°C)	I_{RRM}	–	–	200	μA
*Peak Forward "On" Voltage (I_{TM} = 8.2 A Peak, Pulse Width = 1 to 2 ms, 2% Duty Cycle)	V_{TM}	–	–	2.2	Volts
Gate Trigger Current (Continuous dc) (V_{AK} = 12 Vdc, R_L = 24 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = −40°C)	I_{GT}	– –	– –	200 500	μA
Gate Trigger Voltage (Continuous dc) (Source Voltage = 12 V, R_S = 50 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = −40°C)	V_{GT}	–	–	1.0	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 Ohms, T_J = 110°C)	V_{GD}	0.2	–	–	Volts
Holding Current (V_{AK} = 12 Vdc, I_{GT} = 2.0 mA) T_J = 25°C *(Initiating On-State Current = 200 mA) T_J = −40°C	I_H	– –	– –	5.0 10	mA
*Total Turn-On Time (Source Voltage = 12 V, R_S = 6.0 k Ohms) (I_{TM} = 8.2 A, I_{GT} = 2.0 mA, Rated V_{DRM}) (Rise Time = 20 ns, Pulse Width = 10 μs)	t_{gt}	–	–	2.0	μs
Forward Voltage Application Rate (T_J = 110°C)	dv/dt	–	10	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)

   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C. For optimum results, an activated flux (oxide removing) is recommended.

CURRENT DERATING

FIGURE 1 — MAXIMUM CASE TEMPERATURE

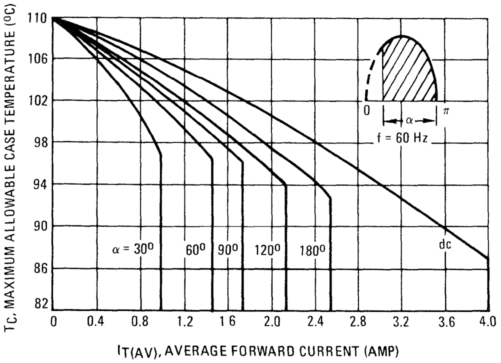
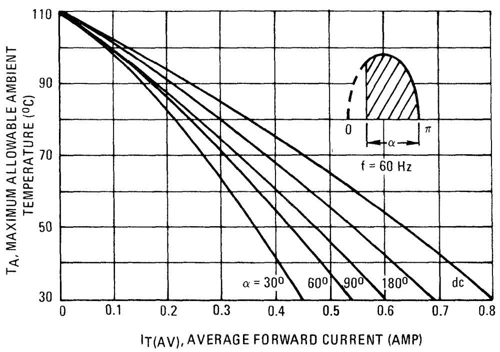


FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE



2N6255 (SILICON)

The RF Line

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt VHF large-signal amplifier applications required in industrial and commercial FM equipment.

- Specified 12.5 Volt, 175 MHz Characteristics –
  Output Power = 3.0 Watts
  Minimum Gain = 7.8 dB
  Efficiency = 50%

*MAXIMUM RATINGS

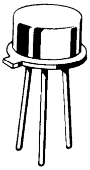
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.5	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

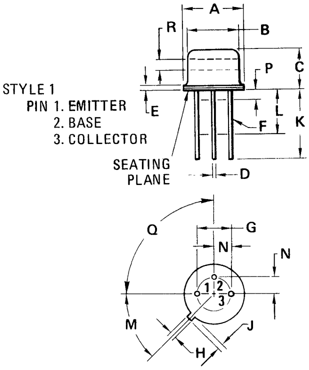
*Indicates JEDEC Registered Data.

This device is designed for RF operation. The total device dissipation applies only when the device is operated as an RF amplifier.

3.0 W-175 MHz
RF POWER
TRANSISTOR

NPN SILICON





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

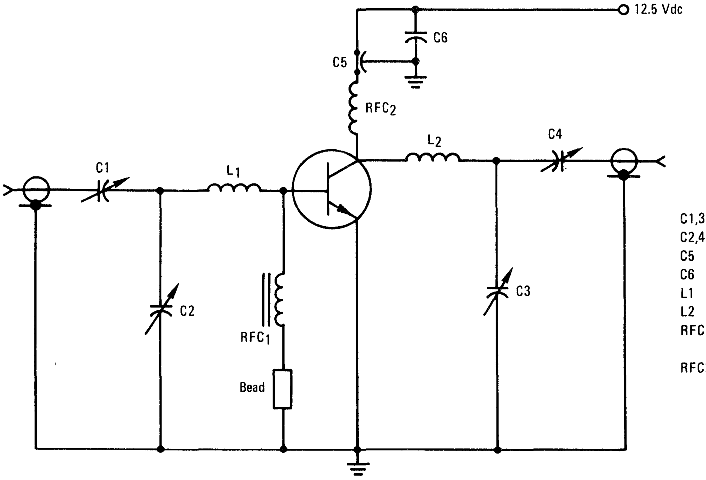
All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	BV_{CES}	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 55°C)	I_{CES}	–	–	5.0	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.25	mAdc
ON CHARACTERISTICS					
Dc Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	15	20	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 3.0 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	G_{PE}	7.8	–	–	dB
Collector Efficiency (P_{out} = 3.0 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	η	50	–	–	%

FIGURE 1 — 175 MHz CIRCUIT



C1,3	2.0-50 pF ARCO 461 ELMENCO
C2,4	5.0-80 pF ARCO 462 ELMENCO
C5	1000 pF FEED THRU
C6	5.0 μF
L1	1 TURN #18 AWG ¼" I.D.
L2	2½ TURNS #18 AWG ¼" I.D.
RFC1	0.15 μH MOLDED CHOKE WITH BEAD ON GROUND LEG
RFC2	0.15 μH MOLDED CHOKE

BEAD IS FERROXCUBE
56-570-65/3B

FIGURE 2 – OUTPUT POWER versus INPUT POWER

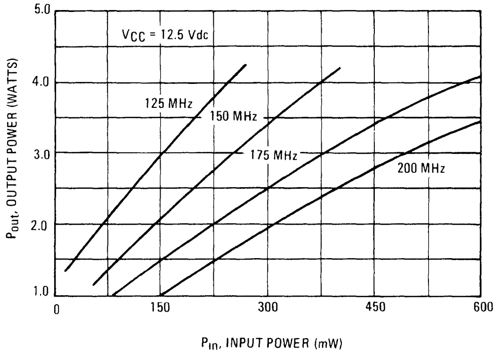


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE

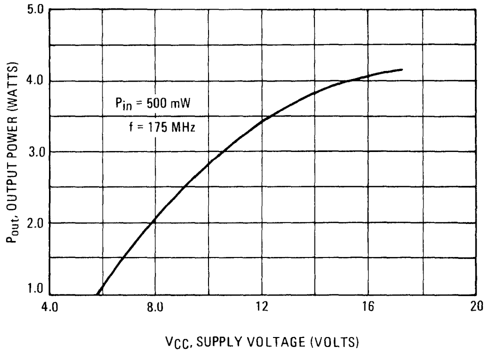


FIGURE 4 – COLLECTOR LOAD versus FREQUENCY

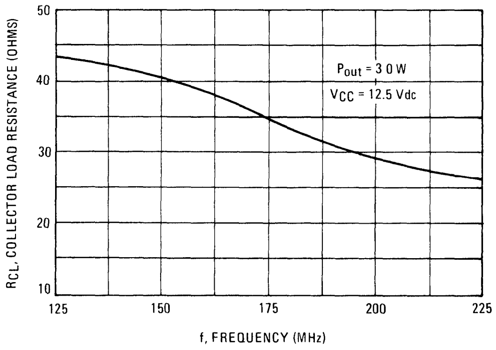


FIGURE 5 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

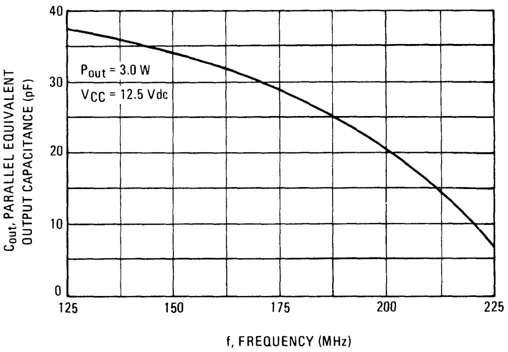


FIGURE 6 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

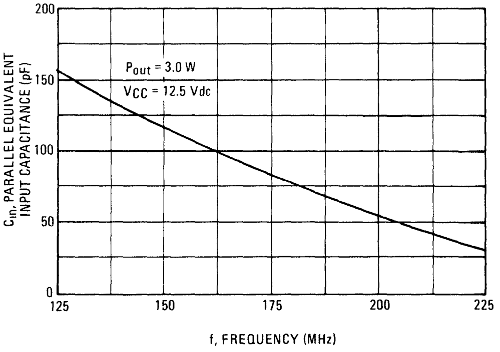
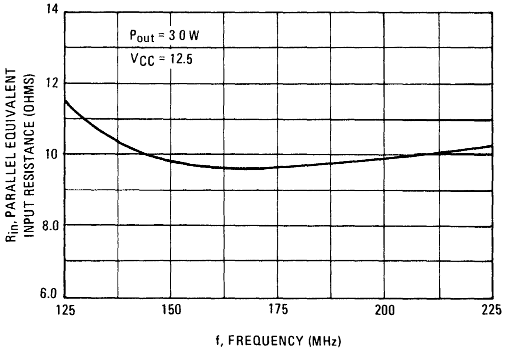
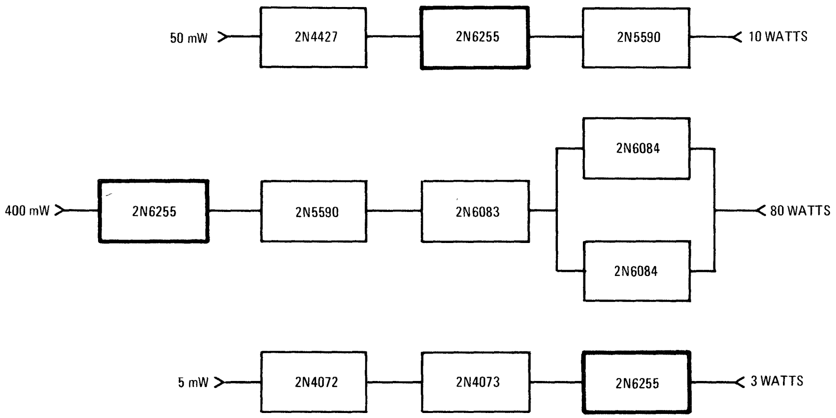


FIGURE 7 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY



175 MHz AMPLIFIER BLOCK DIAGRAMS

FIGURE 8 – V_{CC} = 12.5 VOLTS



2N6256 (SILICON)

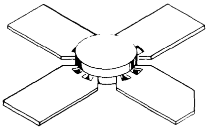
The RF Line

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt, VHF/UHF large signal Amplifier/Multiplier applications required in industrial and commercial FM equipment operating to 520 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics
  Power Output = 0.5 Watts
  Minimum Gain = 7.0 dB
  Efficiency = 60%
- Characterized with series equivalent large signal impedance parameters
- Driver for 2N5944 and 2N5945 UHF amplifiers
- Capable of withstanding severe load mismatch

0.5 WATT – 470 MHz
RF POWER
TRANSISTOR
NPN SILICON

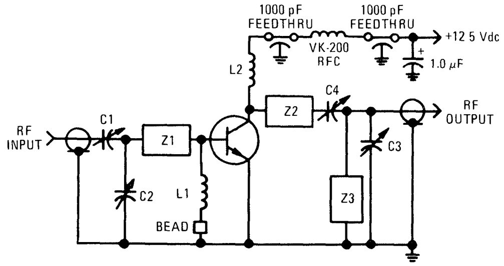


*MAXIMUM RATINGS

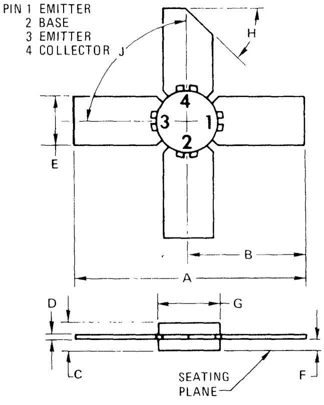
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	0.4	Adc
Total Continuous Device Dissipation @ $T_C = 25^{\circ}C$ – Derate above 25°C	P_D	2.0 11.4	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
* Indicates JEDEC Registered Data

FIGURE 1 – 470 MHz TEST CIRCUIT SCHEMATIC



NOTE: Test Circuit Layout and Component Descriptions Shown in Figure 6



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.800	27.050	1.055	1.065
B	13.340	13.600	0.525	0.535
C	2.920	3.350	0.115	0.132
D	0.102	0.152	0.004	0.006
E	5.590	5.840	0.220	0.230
F	1.400	1.650	0.055	0.065
G	7.060	7.260	0.278	0.286
H	40°	50°	40°	50°
J	90° TP		90° TP	

CASE 249-01

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	BV_{CEO}	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	BV_{CES}	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_A = 125°C)	I_{CES}	–	–	5.0	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
Dc Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	80	200	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	6.0	8.0	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Figures 1, 6) (P_{out} = 0.5 W, V_{CC} = 12.5 Vdc, f = 470 MHz)	G_{PE}	7.0	9.0	–	dB
Collector Efficiency (Figures 1, 6) (P_{out} = 0.5 W, V_{CC} = 12.5 Vdc, f = 470 MHz)	η	60	70	–	%

*Indicates JEDEC Registered Data.

Typical Output Power curves were measured in circuit shown in Figure 6.

FIGURE 2 – OUTPUT POWER versus FREQUENCY

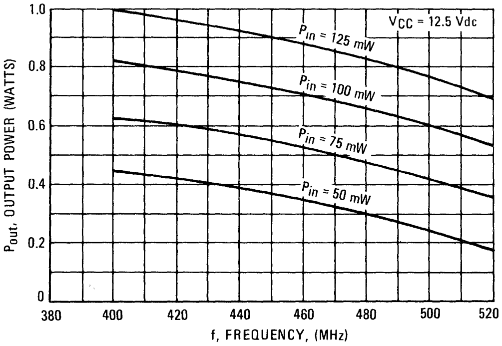


FIGURE 3 – OUTPUT POWER versus INPUT POWER

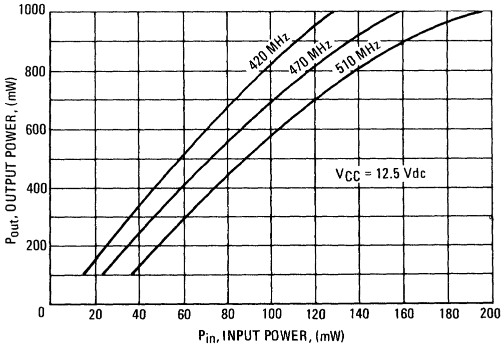


FIGURE 4 – OUTPUT POWER
versus SUPPLY VOLTAGE
(f = 470 MHz)

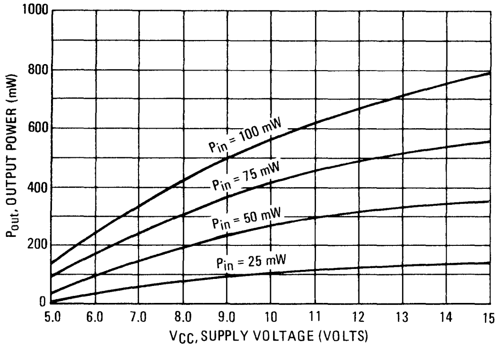


FIGURE 5 – SERIES EQUIVALENT
INPUT and OUTPUT IMPEDANCE
(V_{CC} = 12.5 Vdc, P_{out} = 0.5 Watts)

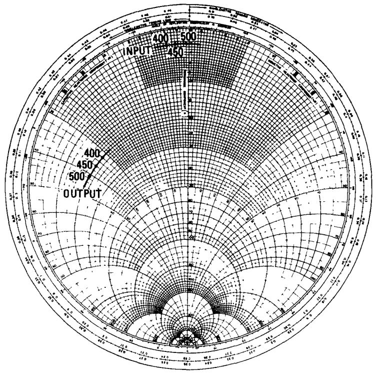
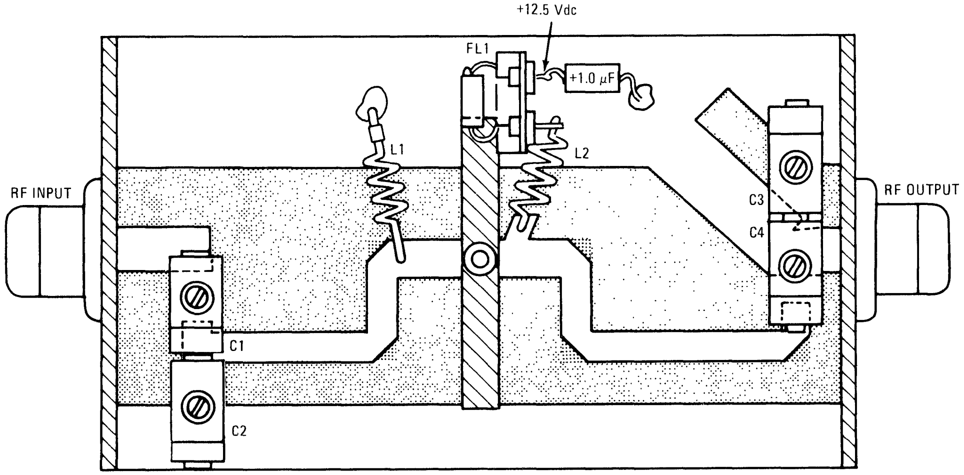


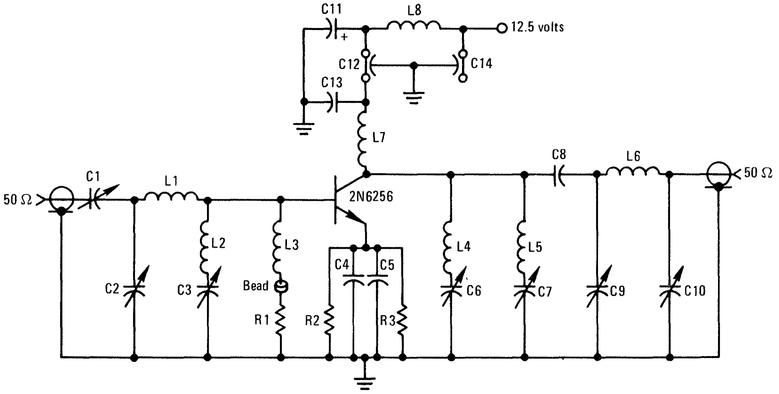
FIGURE 6 – 470 MHz TEST CIRCUIT LAYOUT
(See Figure 1 for Schematic Diagram)



C1,2	1.0-25 pF ARCO 421 OR EQUIVALENT
C3,4	1.0-25 pF ARCO 421 OR EQUIVALENT
L1,2	7 TURNS #22 AWG, 0.2" I.D. FERRITE BEAD FERROXCUBE 56-590-65-3B AS SHOWN ON L1
FL1	DC SUPPLY FILTER 2-1000 pF FT CAPACITOR 1-1.0 μF, 35 V CAPACITOR 1-CHOKE FERROXCUBE VK 200-20-4B

CONNECTORS ARE TYPE "N"
BOARD IS GLASS TEFLON
3" x 5" x 0.060"
MOUNTING PLATE IS 3" x 5" x 0.75"

FIGURE 7 – 150 MHz to 450 MHz
TRIPLER USING 2N6256



C1, 2, 3, 9, 10 1-7 pF ARCO 400 OR EQUIVALENT
C6, 7 1.5-20 pF ARCO 402 OR EQUIVALENT
C4, 5 470 pF ATC TYPE 100-B-420-m-ms
C8 1000 pF UNDERWOOD TYPE J-101
C11 0.47 μF TANTALUM
C12, 14 470 pF FEED THRU
C13 0.1 μF CERAMIC
R1-20 OHM
R2,3-160 OHM

L1 7 TURNS 1/4" I.D.
L2,6-4 TURNS 1/8" I.D.
L3 0.68 μH MOLDED CHOKE
L4 5 TURNS 1/4" I.D.
L5 6 TURNS 1/8" I.D.
L7 1 μH MOLDED CHOKE
L8 FERROXCUBE VK200-20/4B
FERRITE BEAD IS FERROXCUBE 56-590-65/3B

NOTE: ALL COILS AIR CORE SPACE WOUND WITH #20 AWG WIRE
UNLESS OTHERWISE SPECIFIED

Figure 7 shows the 2N6256 in a 150 MHz to 450 MHz tripler circuit. This circuit will typically produce 85 mW at 450 MHz with 30 mW at 150 MHz input (4.5 db gain). Collector efficiency is 25% and all unwanted harmonics are at least 30 db down from the 450 MHz output level.

It is important that each emitter lead be bypassed separately with a good hi-quality capacitor. The emitter resistor is likewise split in two with one-half on each emitter lead.

The input network is a modified "TEE" consisting of C1, C2, and L1, which matches the 50 Ohm input to the transistor impedance at 150 MHz; this is roughly 18-j20 Ohms. The combination of L2 and C3 form a 450 MHz idler to provide a base return for third harmonic current. L4, C6 and L5, C7 are 150 MHz and 300 MHz output idlers respectively. The output matching section is a pi network made up of L6, C9 and C10. All coils are air core space-wound (turns one wire diameter apart) with #20 AWG wire.

2N6274 (SILICON)
thru
2N6277

HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifer and switching circuit applications.

- High Collector Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N6274
  = 120 Vdc (Min) – 2N6275
  = 140 Vdc (Min) – 2N6276
  = 150 Vdc (Min) – 2N6277
- High DC Current Gain –
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max
  t_f = 0.25 μs (Max)

*MAXIMUM RATINGS

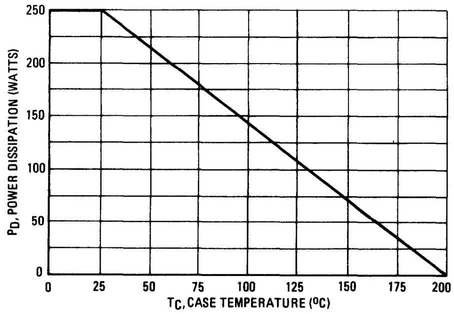
Rating	Symbol	2N6274	2N6275	2N6276	2N6277	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →				Vdc
Collector Current – Continuous Peak	I_C	← 50 → ← 100 →				Adc
Base Current	I_B	← 20 →				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 250 → ← 1.43 →				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

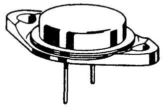
*Indicates JEDEC Registered Data.

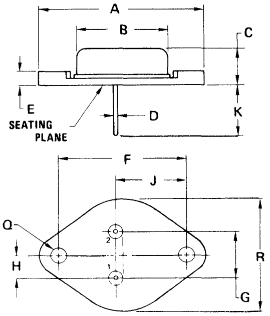
FIGURE 1 – POWER DERATING



50 AMPERE
POWER TRANSISTORS
NPN SILICON

100, 120, 140, 150 VOLTS
250 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

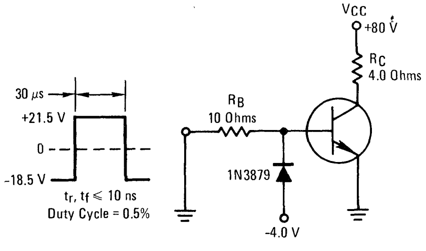
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6274		100	–	
	2N6275		120	–	
	2N6276		140	–	
	2N6277		150	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6274		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6275		–	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6276		–	50	
(V_{CE} = 75 Vdc, I_B = 0)	2N6277		–	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			–	10	μAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			50	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)			30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.0	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.8	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.5	
Base-Emitter On Voltage (I_C = 20 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	600	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc)		t_r	–	0.35	μs
Storage Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)		t_s	–	0.80	μs
Fall Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 — TURN-ON TIME

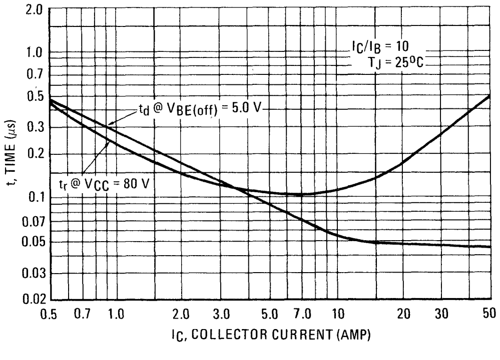


FIGURE 4 – THERMAL RESPONSE

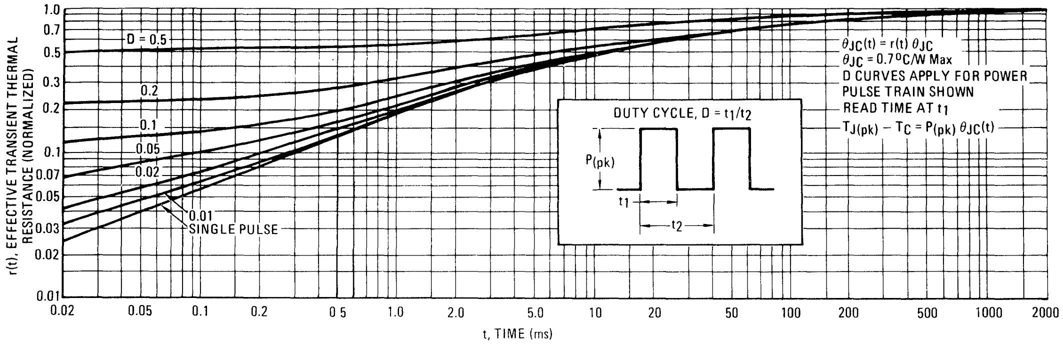
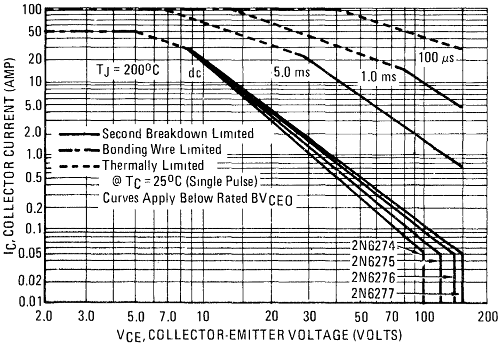


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

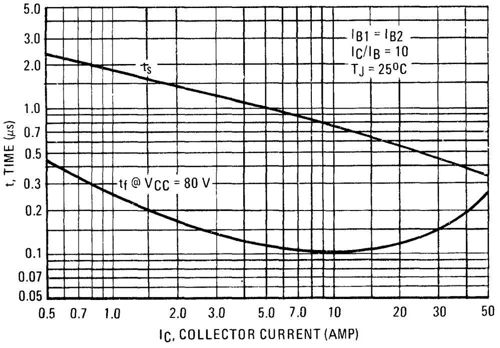


FIGURE 7 – CAPACITANCE

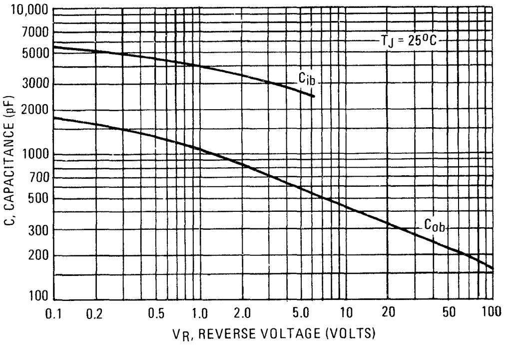


FIGURE 8 – DC CURRENT GAIN

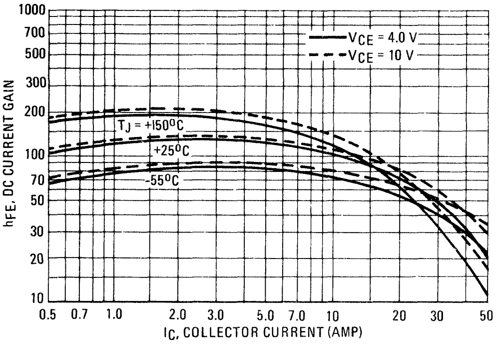


FIGURE 9 – COLLECTOR SATURATION REGION

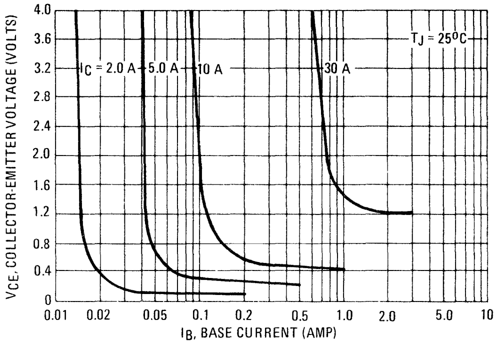


FIGURE 10 – "ON" VOLTAGES

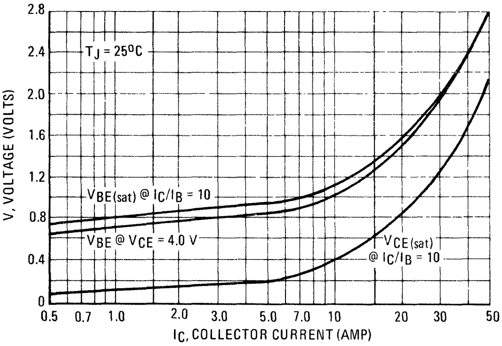


FIGURE 11 – TEMPERATURE COEFFICIENTS

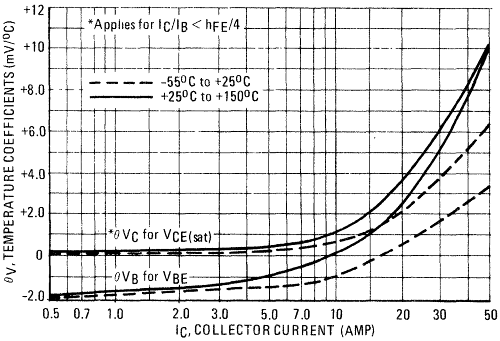


FIGURE 12 – COLLECTOR CUT-OFF REGION

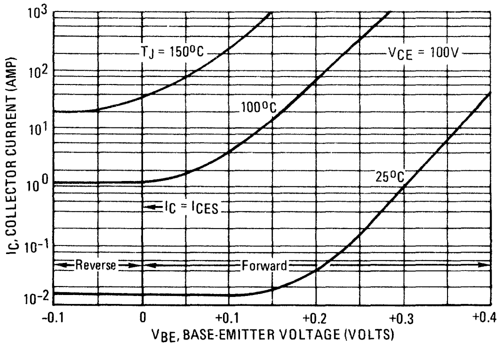
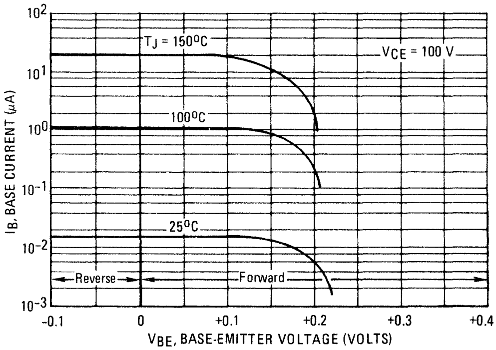


FIGURE 13 – BASE CUT-OFF REGION



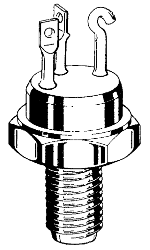
2N6278 thru 2N6281 (SILICON)

HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N6278
  = 120 Vdc (Min) – 2N6279
  = 140 Vdc (Min) – 2N6280
  = 150 Vdc (Min) – 2N6281
- High DC Current Gain –
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max)
  t_f = 0.25 μs (Max)

50 AMPERE
POWER TRANSISTORS
NPN SILICON
100, 120, 140, 150 VOLTS
250 WATTS



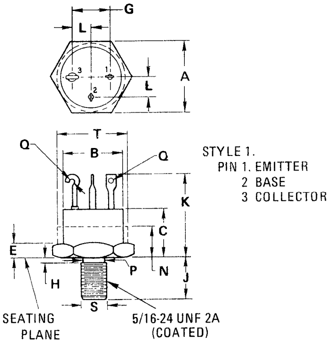
*MAXIMUM RATINGS

Rating	Symbol	2N6278	2N6279	2N6280	2N6281	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →				Vdc
Collector Current – Continuous Peak	I_C	← 50 → 100				Adc
Base Current	I_B	← 20 →				Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 250 → ← 1.43 →				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.70	°C/W

*Indicates JEDEC Registered Data



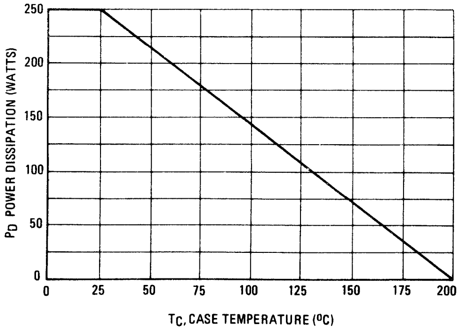
STYLE 1.
PIN 1. EMITTER
2 BASE
3 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.72	22.23	0.855	0.875
B	18.92	19.69	0.745	0.775
C	12.19	13.59	0.480	0.535
E	2.29	4.24	0.090	0.167
G	12.32	13.08	0.485	0.515
H	–	2.67	–	0.105
J	11.68	12.57	0.460	0.495
K	23.80	26.16	0.937	1.030
L	6.10	6.60	0.240	0.260
N	–	7.62	–	0.300
P	7.06	7.92	0.278	0.312
Q	1.52	2.67	0.060	0.105
S	7.127	7.249	0.2806	0.2854
T	19.69	22.23	0.775	0.875

All JEDEC notes and dimensions apply.

CASE 188
TO-63

FIGURE 1 – POWER DERATING

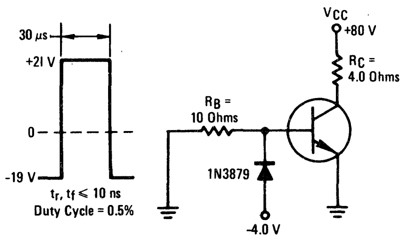


***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6278		100	–	
	2N6279		120	–	
	2N6280		140	–	
	2N6281		150	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6278		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6279		–	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6280		–	50	
(V_{CE} = 75 Vdc, I_B = 0)	2N6281		–	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			–	10	μAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C			–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			50	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)			30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–		Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.2	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.8	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.5	
Base-Emitter On Voltage (I_C = 20 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	600	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = 2.0 Adc, $V_{BE\ (off)}$ = 5.0 Vdc)		t_r	–	0.35	μs
Storage Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)		t_s	–	0.80	μs
Fall Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data (1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



Note: For information on Figures 3 & 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN ON TIME

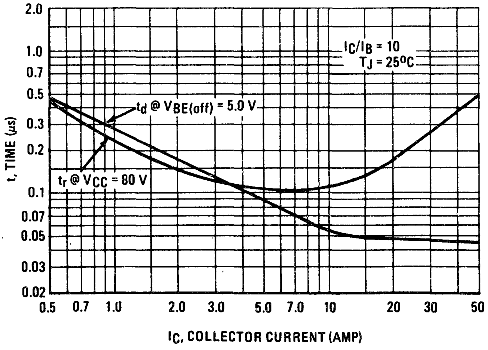


FIGURE 4 – THERMAL RESPONSE

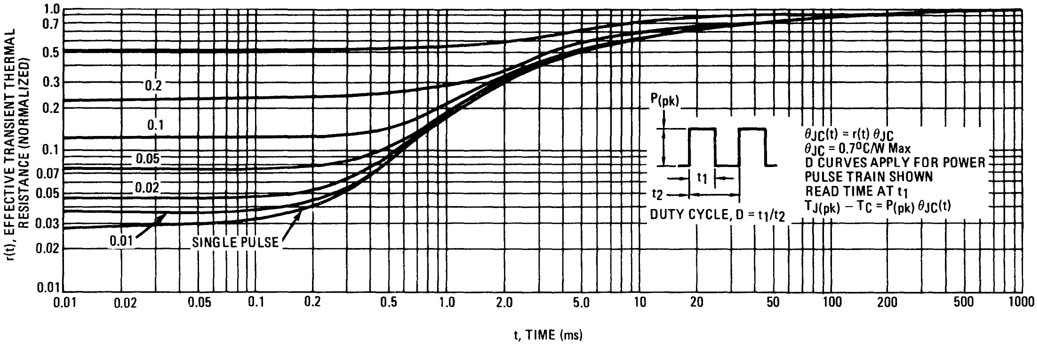
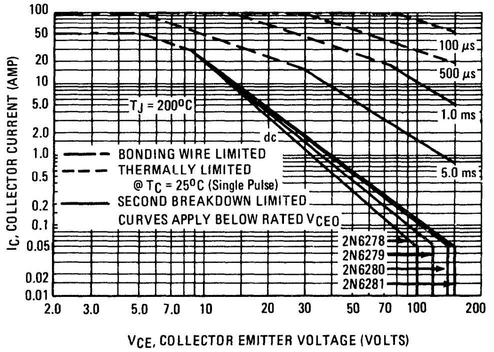


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN OFF TIME

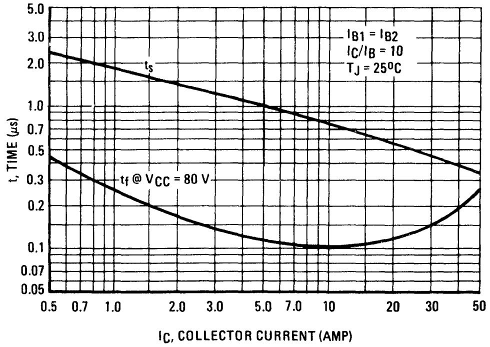


FIGURE 7 – CAPACITANCE

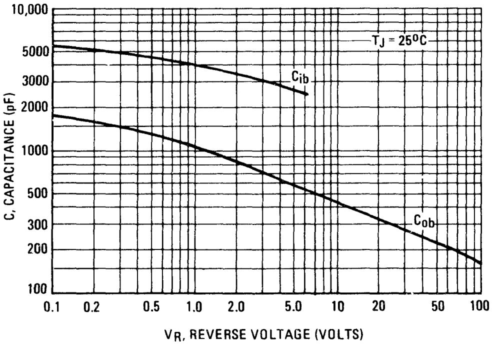


FIGURE 8 – DC CURRENT GAIN

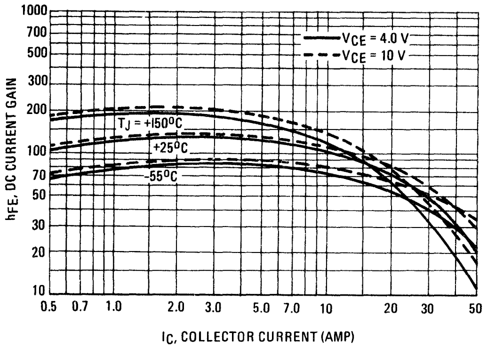


FIGURE 9 – COLLECTOR SATURATION REGION

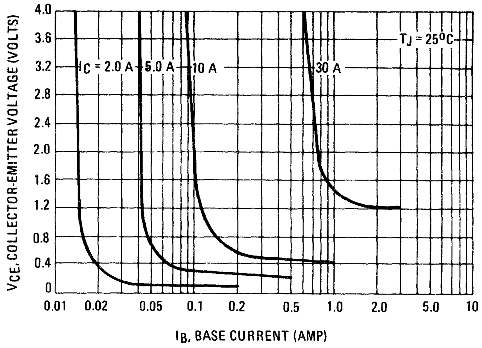


FIGURE 10 – ON VOLTAGES

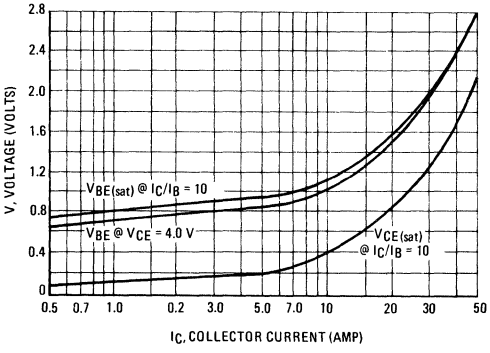


FIGURE 11 – TEMPERATURE COEFFICIENTS

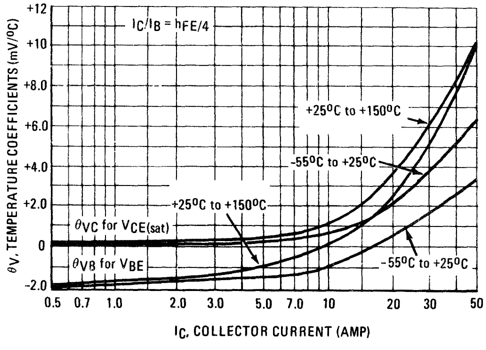


FIGURE 12 – COLLECTOR CUTOFF REGION

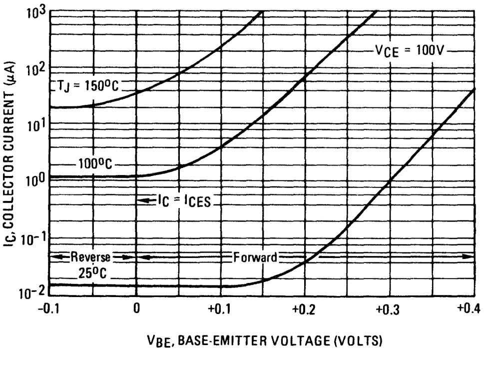
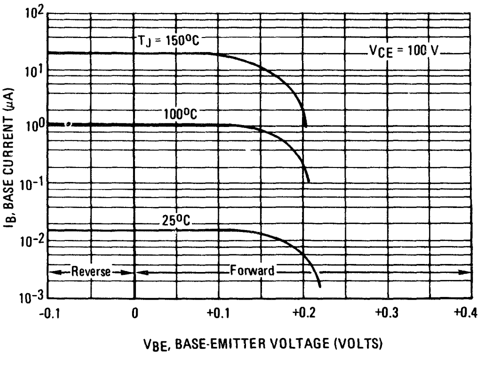


FIGURE 13 – BASE CUTOFF REGION



2N6282 thru 2N6284 NPN (SILICON)
2N6285 thru 2N6287 PNP

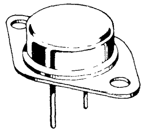
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain @ I_C = 10 Adc –
  h_{FE} = 2400 (Typ) – 2N6282, 2N6283, 2N6284
  = 4000 (Typ) – 2N6285, 2N6286, 2N6287
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6282, 2N6285
  = 80 Vdc (Min) – 2N6283, 2N6286
  = 100 Vdc (Min) – 2N6284, 2N6287
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
20 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS

60, 80, 100 VOLTS
160 WATTS



*MAXIMUM RATINGS

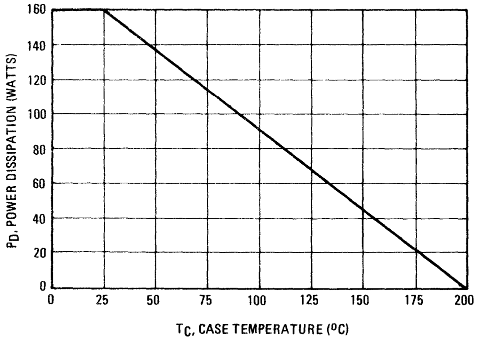
Rating	Symbol	2N6282 2N6285	2N6283 2N6286	2N6284 2N6287	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	20 40			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

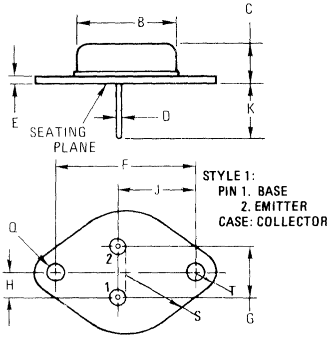
*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.09	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

2N6282, 2N6283, 2N6284 NPN, (continued)
2N6285, 2N6286, 2N6287 PNP

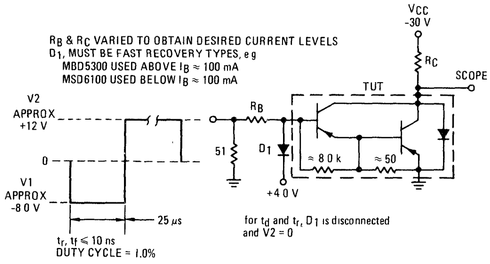
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N6282, 2N6285		60	–	
	2N6283, 2N6286		80	–	
	2N6284, 2N6287		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6282, 2N6285		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6283, 2N6286		–	1.0	
(V_{CE} = 50 Vdc, I_B = 0)	2N6284, 2N6287		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)			750	18,000	
(I_C = 20 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 40 mAdc)			–	2.0	
(I_C = 20 Adc, I_B = 200 mAdc)			–	3.0	
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6282, 83, 84		–	400	
	2N6285, 86, 87		–	600	
Small-Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data.

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2%

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 – SWITCHING TIMES

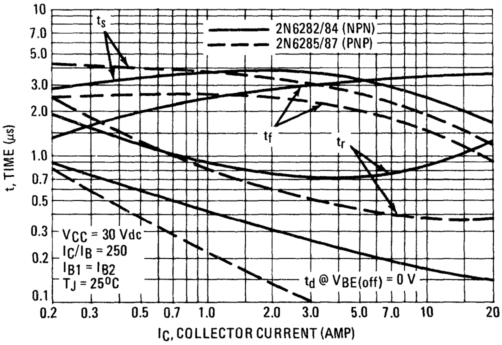
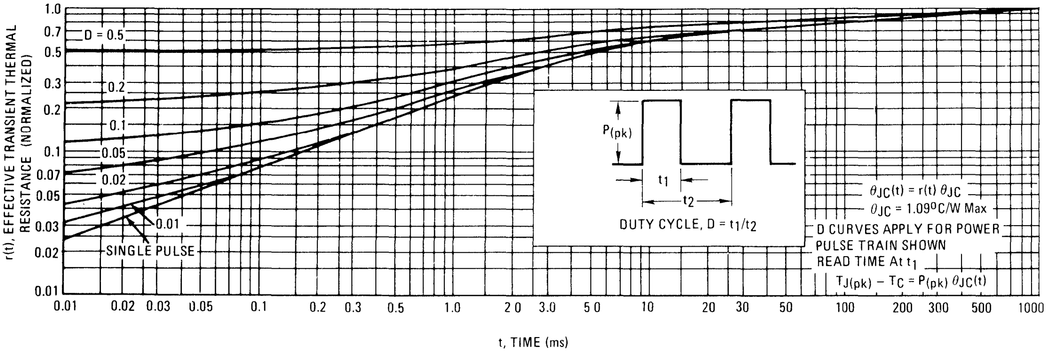


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6282, 2N6285

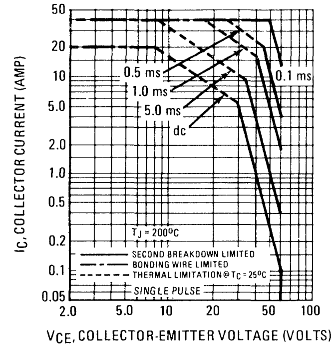


FIGURE 6 – 2N6283, 2N6286

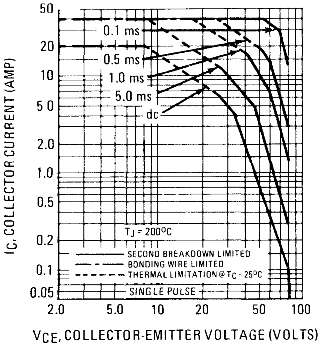
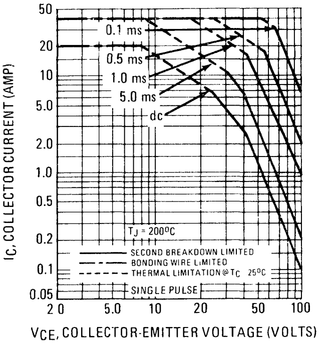


FIGURE 7 – 2N6284, 2N6287



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 8 – SMALL-SIGNAL CURRENT GAIN

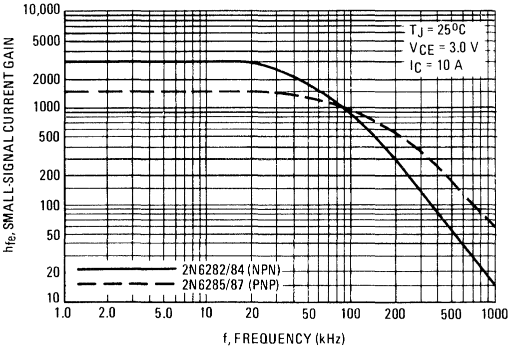
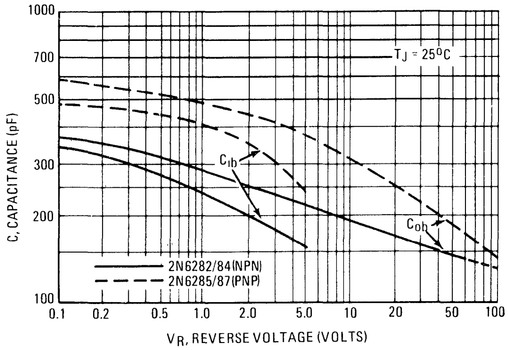


FIGURE 9 – CAPACITANCE



NPN
2N6282, 2N6283, 2N6284

PNP
2N6285, 2N6286, 2N6287

FIGURE 10 – DC CURRENT GAIN

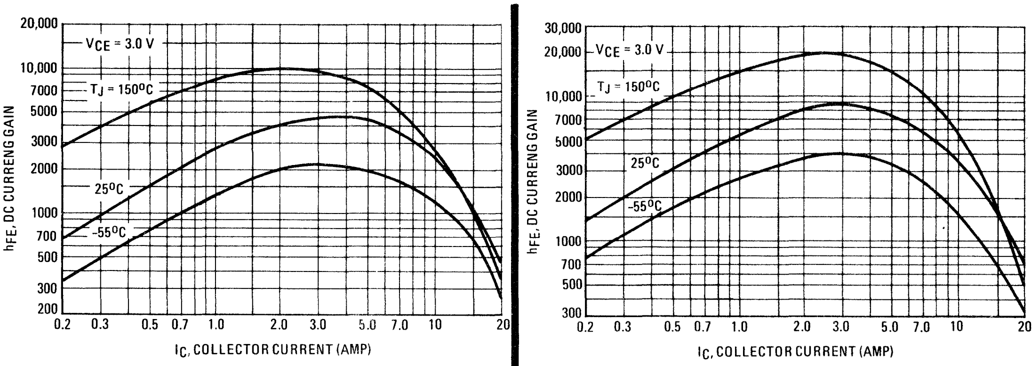


FIGURE 11 – COLLECTOR SATURATION REGION

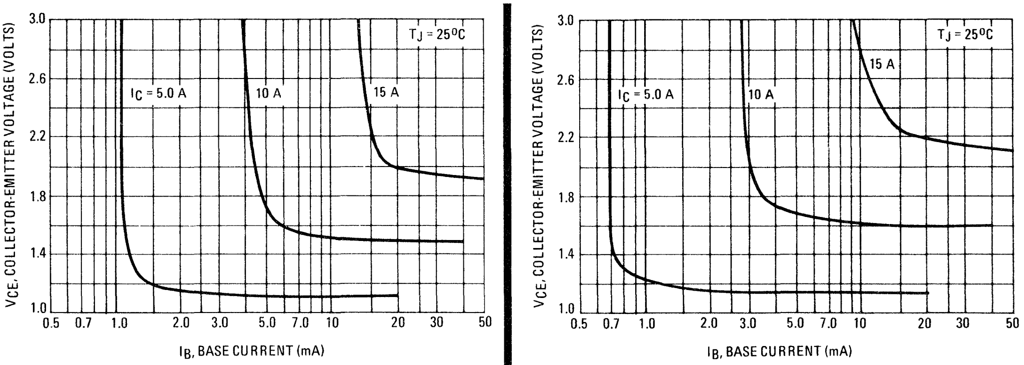
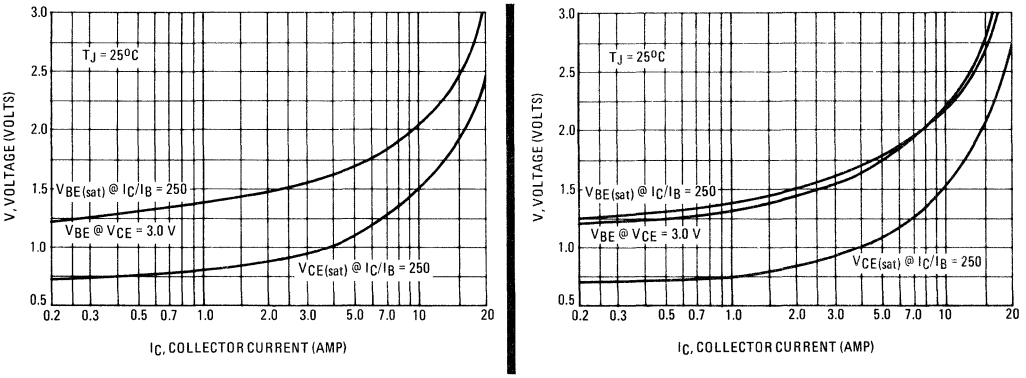


FIGURE 12 – "ON" VOLTAGES



NPN
2N6282, 2N6283, 2N6284

PNP
2N6285, 2N6286, 2N6287

FIGURE 13 – TEMPERATURE COEFFICIENTS

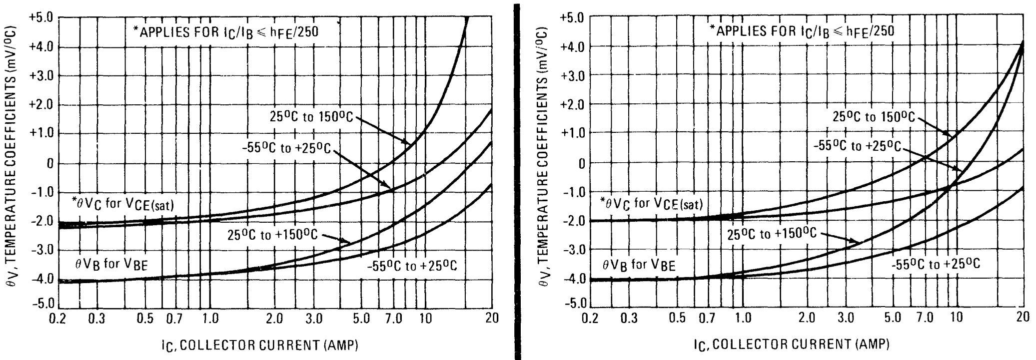


FIGURE 14 – COLLECTOR CUTOFF REGION

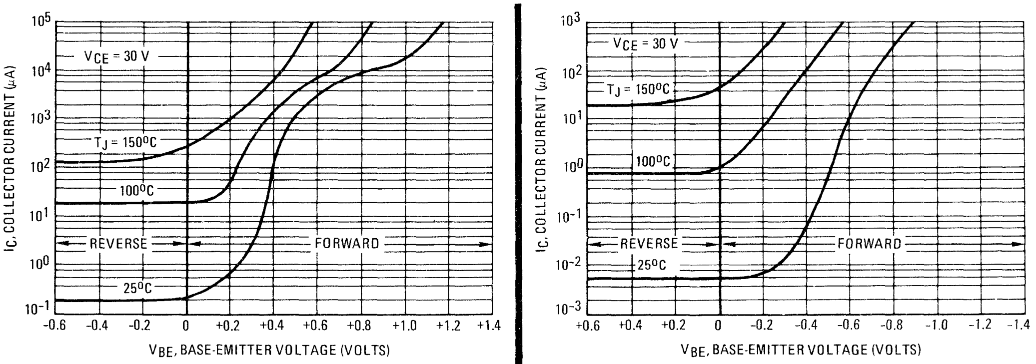
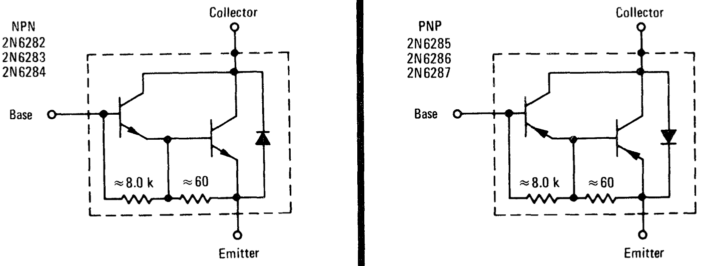


FIGURE 15 – DARLINGTON SCHEMATIC



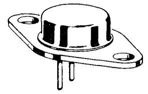
2N6294, 2N6295 NPN (SILICON)
2N6296, 2N6297 PNP

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier, low-speed switching and hammer driver applications.

- High DC Current Gain – h_{FE} = 3000 (Typ) @ I_C = 2.0 Adc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6294, 2N6296
  = 80 Vdc (Min) – 2N6295, 2N6297
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

4 AMPERES
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS
60, 80 VOLTS
50 WATTS



*MAXIMUM RATINGS

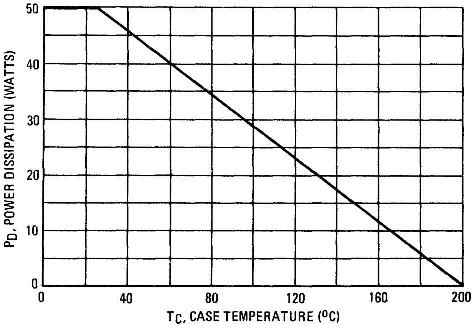
Rating	Symbol	2N6294 2N6296	2N6295 2N6297	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	4.0 8.0		Adc
Base Current	I_B	80		mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.286		Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200		°C

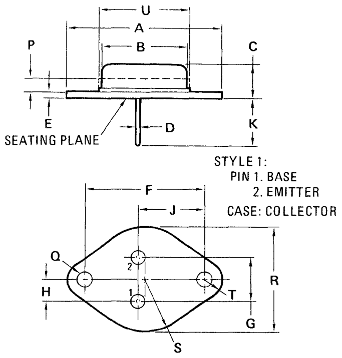
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

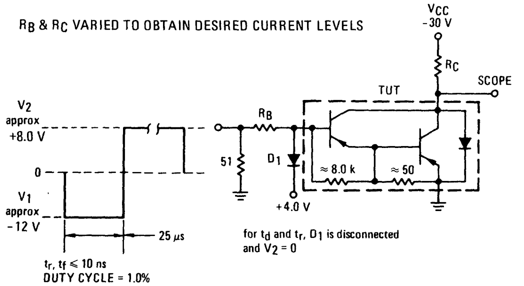
CASE 80-02
TO-66

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6294, 2N6296		60	–	
	2N6295, 2N6297		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6294, 2N6296		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N6295, 2N6297		–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)	2N6294, 2N6295		–	0.5	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)	2N6296, 2N6297		–	0.5	
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6294, 2N6295		–	5.0	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6296, 2N6297		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			750	18000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)			–	2.0	
(I_C = 4.0 Adc, I_B = 40 mAdc)			–	3.0	
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6294, 2N6295		–	120	
	2N6296, 2N6297		–	200	
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit, reverse all polarities.

FIGURE 3 – SWITCHING TIMES

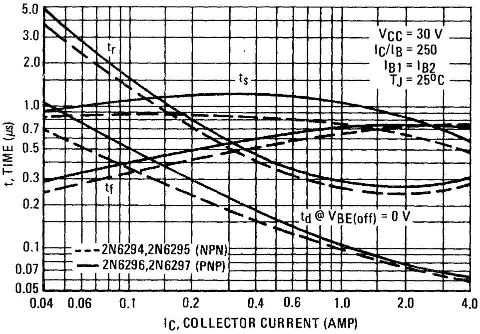


FIGURE 4 – THERMAL RESPONSE

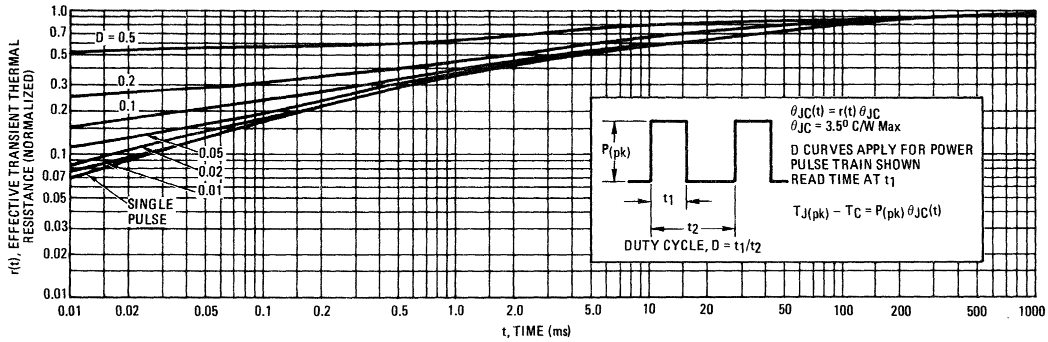
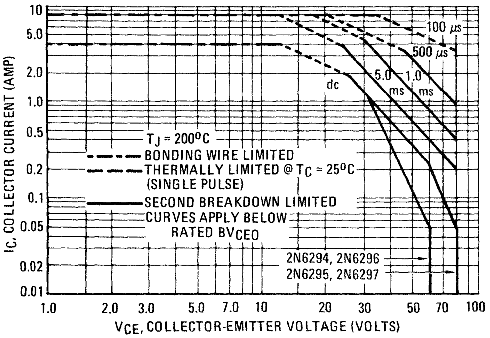


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

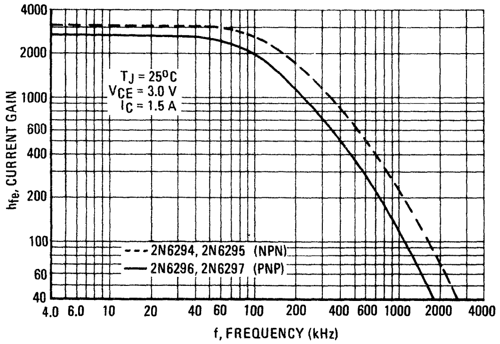
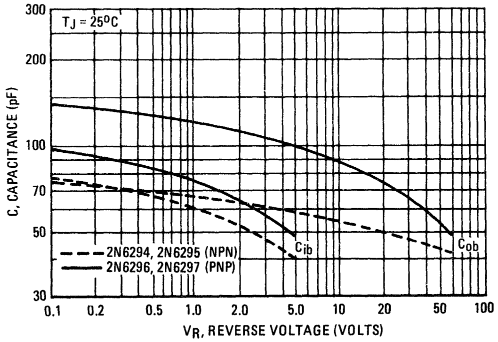


FIGURE 7 – CAPACITANCE



NPN
2N6294, 2N6295

PNP
2N6296, 2N6297

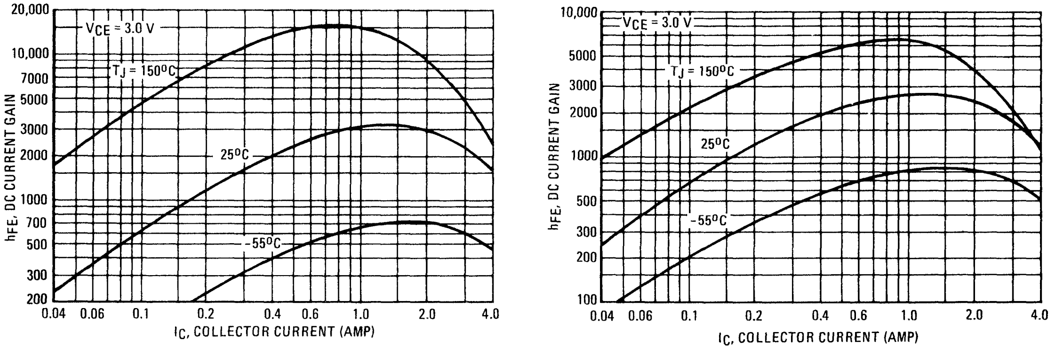


FIGURE 8 – DC CURRENT GAIN

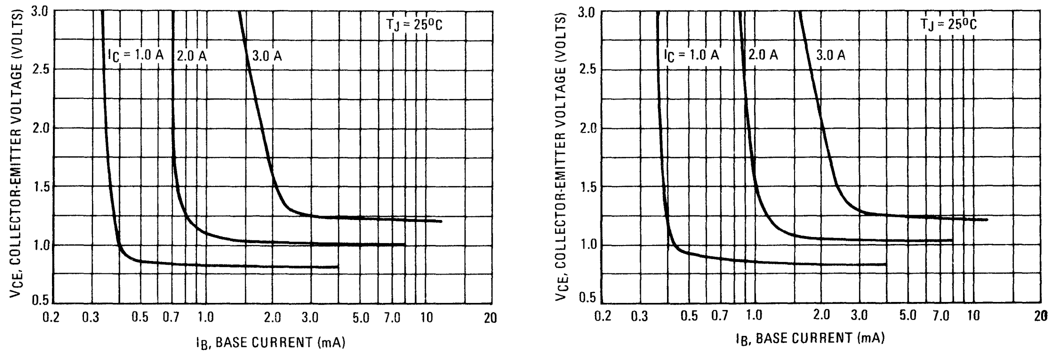


FIGURE 9 – COLLECTOR SATURATION REGION

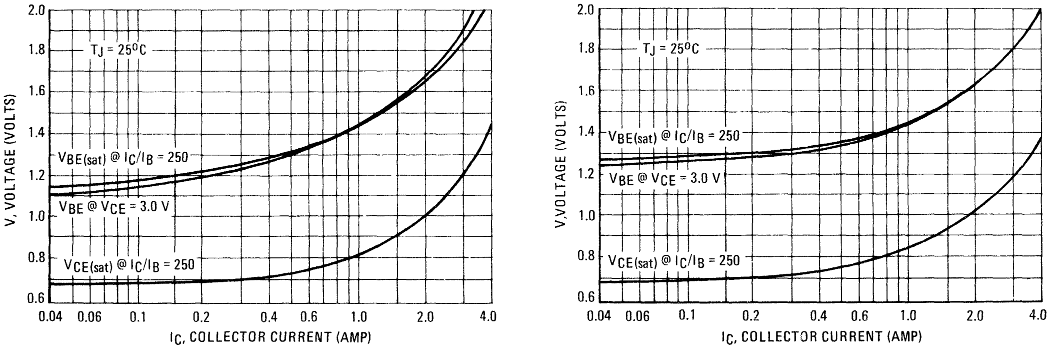


FIGURE 10 – "ON" VOLTAGES

NPN
2N6294, 2N6295

PNP
2N6296, 2N6297

FIGURE 11 – TEMPERATURE COEFFICIENTS

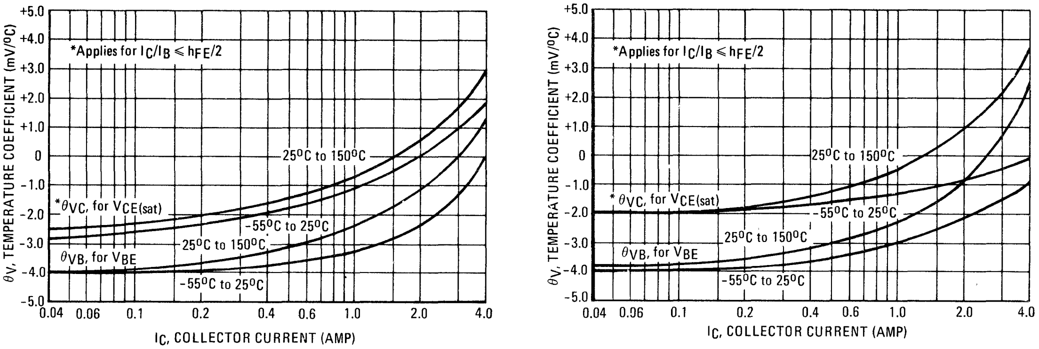


FIGURE 12 – COLLECTOR CUTOFF REGION

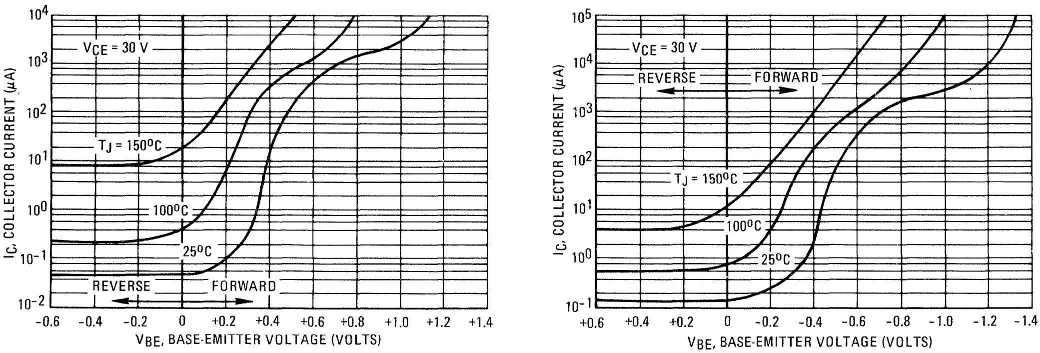
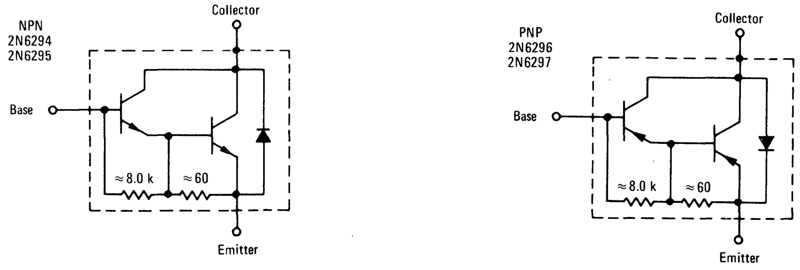


FIGURE 13 – DARLINGTON SCHEMATICS



2N6298 thru 2N6301 (SILICON)

For Specifications, See 2N6053 Data.

2N6303 (SILICON)

For Specifications, See 2N3719 Data, Volume I.

2N6304 (SILICON)
2N6305

The RF Line

NPN SILICON RF SMALL-SIGNAL TRANSISTORS

. . . designed primarily for use in broadband amplifiers to 1.0 GHz, including MATV applications. Also useful as a low-noise, high-gain, general purpose UHF small-signal amplifier.

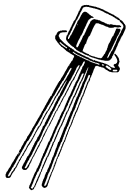
- High Current-Gain – Bandwidth Product –
  f_T = 1400 MHz (Min) @ I_C = 10 mAdc
- Low Noise Figure –
  NF = 4.5 dB (Max) @ f = 450 MHz
- High Power Gain –
  G_{pe} = 15 dB (Min) @ f = 450 MHz

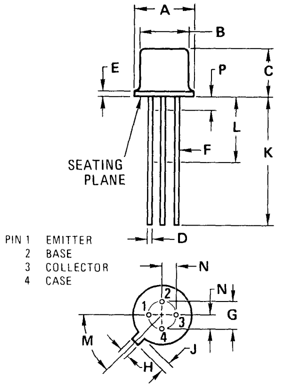
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage 1.0 to 20 mAdc	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector Current – Continuous	I_C	50	mAdc
Total Continuous Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data

HIGH-GAIN, LOW NOISE SMALL-SIGNAL UHF TRANSISTORS





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45°BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

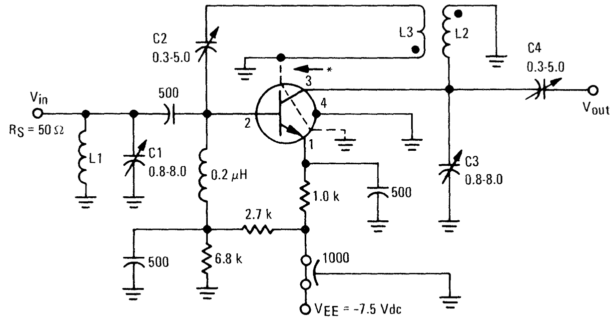
CASE 20-03
TO-72

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	BV_{CEO}	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	BV_{CBO}	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	BV_{EBO}	3.5	–	–	Vdc
Collector Cutoff Current (V_{CB} = 5.0 Vdc, I_E = 0)	I_{CBO}	–	–	10	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	25	–	250	–
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product 2N6304 (I_C = 10 mAdc, V_{CE}=5.0 Vdc, f≈100 MHz) 2N6305	f_T	1400 1200	– –	2400 2400	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	0.1	0.8	1.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	25	–	250	–
Collector-Base Time Constant 2N6304 (I_E = 2.0 mAdc, V_{CB} = 5.0 Vdc, f = 31.8 MHz) 2N6305	$r_b'C_c$	2.0 2.0	–	12 15	ps
Noise Figure (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, R_S = 50 ohms, f = 450 MHz) 2N6304 (Figure 1) 2N6305	NF	– –	– –	4.5 5.5	dB
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 450 MHz) 2N6304 (Figure 1) 2N6305	G_{pe}	15 12	– –	– –	dB

***Indicates JEDEC Registered Data**

FIGURE 1 – TEST CIRCUIT FOR NOISE FIGURE AND POWER GAIN



Capacitance values in pF

L1, L2 – Silver-plated brass rod, 1-1/2" long and 1/4" dia. Install at least 1/2" from nearest vertical chassis surface.

L3 – 1/2 turn #16 AWG wire, located 1/4" from and parallel to L2.

* – External interlead shield to isolate collector lead from emitter and base leads.

Neutralization Procedure:

(A) Connect 450-MHz signal generator (with R_S = 50 ohms) to input terminals of amplifier.

(B) Connect 50-ohm RF voltmeter across output terminals of amplifier.

(C) Apply V_{EE}, and with signal generator adjusted for 5 mV output from amplifier, tune C1, C3, and C4 for maximum output.

(D) Interchange connections to signal generator and RF voltmeter.

(E) With sufficient signal applied to output terminals of amplifier, adjust C2 for minimum indication at input.

(F) Repeat steps (A), (B), and (C) to determine if retuning is necessary.

FIGURE 2 – CURRENT-GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

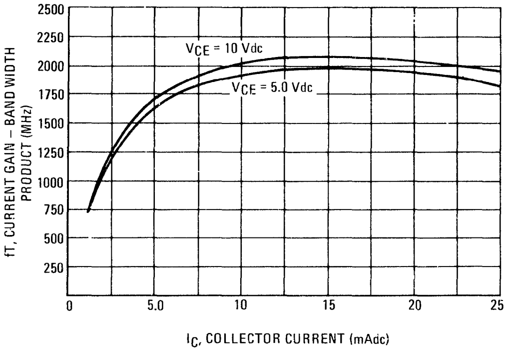


FIGURE 3 – COLLECTOR-BASE TIME CONSTANT versus EMITTER CURRENT

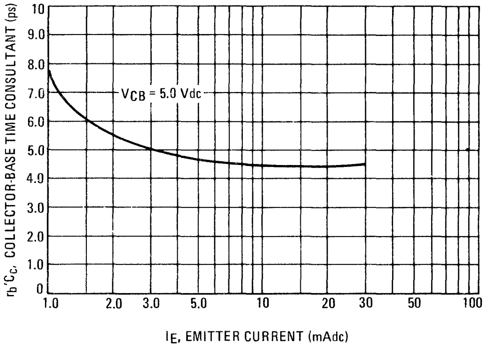


FIGURE 4 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY

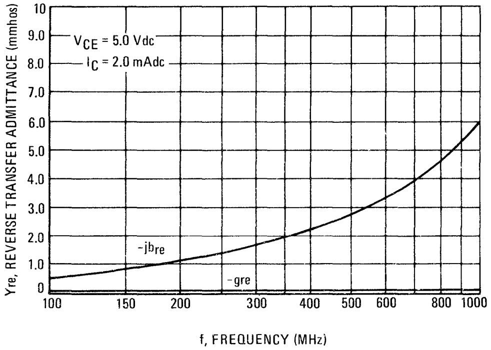


FIGURE 5 – INPUT ADMITTANCE versus FREQUENCY

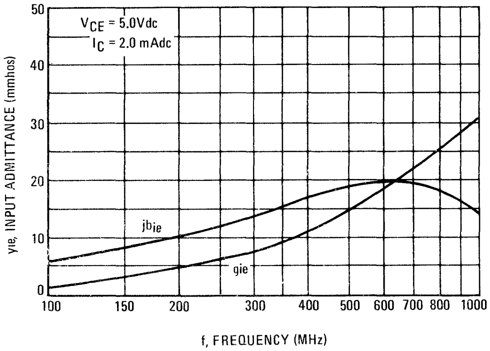


FIGURE 6 – OUTPUT ADMITTANCE versus FREQUENCY

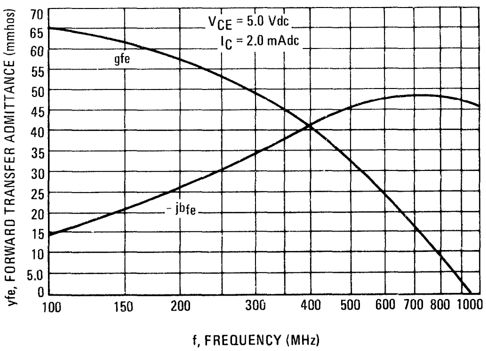


FIGURE 7 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

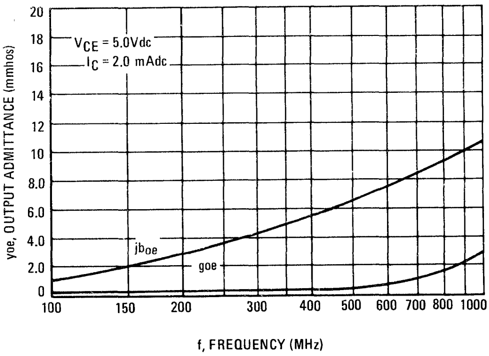


FIGURE 8 – COLLECTOR-BASE CAPACITANCE versus COLLECTOR BASE VOLTAGE

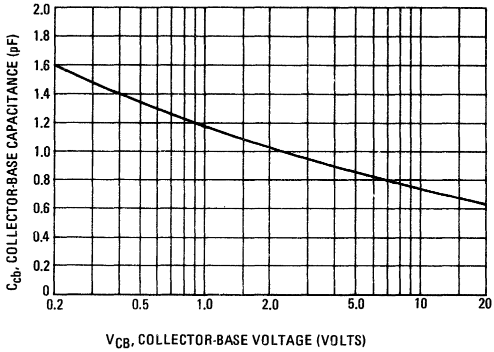


FIGURE 9 – S_{11}, INPUT REFLECTION COEFFICIENT

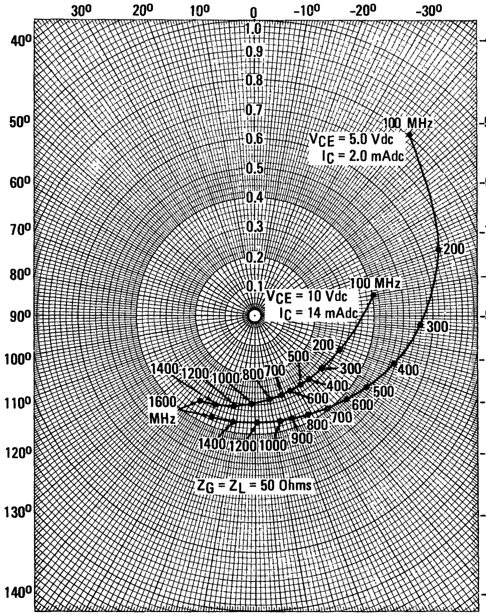


FIGURE 10 – S_{22}, OUTPUT REFLECTION COEFFICIENT

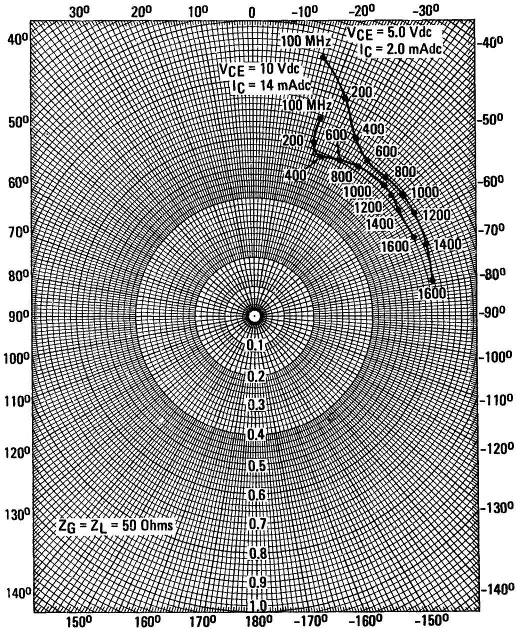


FIGURE 11 – S_{12}, REVERSE TRANSMISSION COEFFICIENT

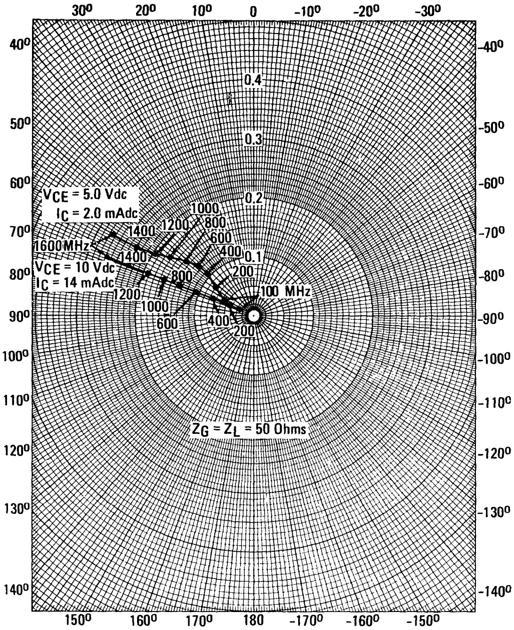


FIGURE 12 – S_{21}, FORWARD TRANSMISSION COEFFICIENT

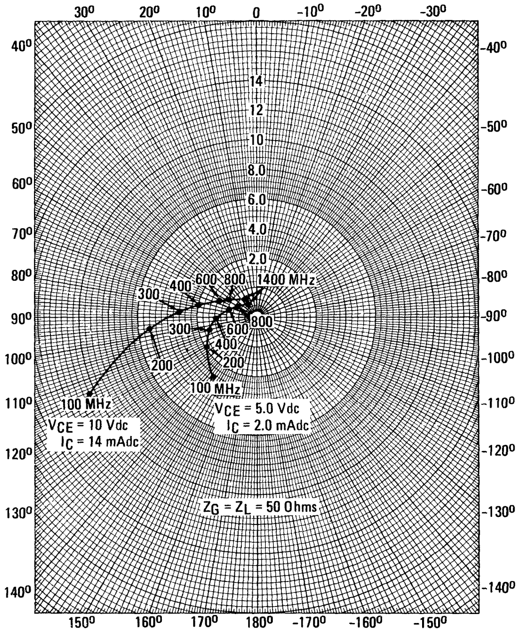
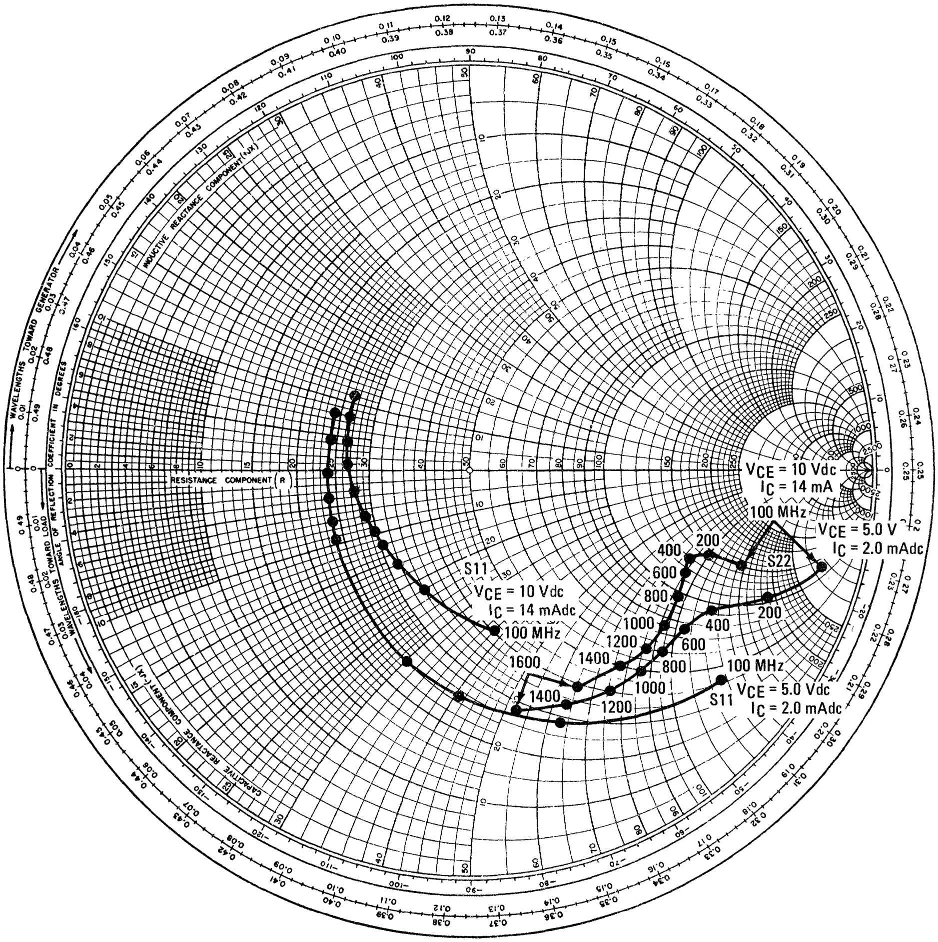


FIGURE 13 – S_{11}, INPUT REFLECTION COEFFICIENT AND S_{22}, OUTPUT REFLECTION COEFFICIENT



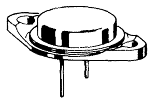
2N6306 (SILICON)
2N6307
2N6308

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

. . . designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications in associated consumer products.

- High Collector-Base Voltage –
  V_{CB} = 500 Vdc – 2N6306
  = 600 Vdc – 2N6307
  = 700 Vdc – 2N6308
- Excellent DC Current Gain @ I_C = 3.0 Adc
  h_{FE} = 15 - 75 – 2N6306, 2N6307
  = 12 -60 – 2N6308
- Low Collector-Emitter Saturation Voltage @ I_C = 3.0 Adc
  $V_{CE(sat)}$ = 0.8 Vdc (Max) – 2N6306
  = 1.0 Vdc (Max) – 2N6307
  = 1.5 Vdc (Max) – 2N6308
- Current Gain Bandwidth Product –
  f_T = 5.0 MHz (Min) @ I_C = 0.3 Adc

8 AMPERE
POWER TRANSISTORS
NPN SILICON
250-300-350 VOLTS
125 WATTS

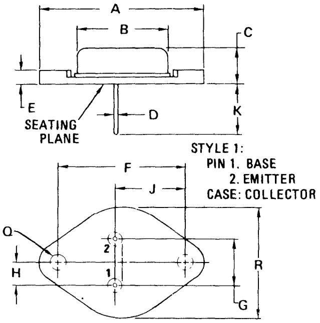


*MAXIMUM RATINGS

Rating	Symbol	2N6306	2N6307	2N6308	Unit
Collector-Base Voltage	V_{CB}	500	600	700	Vdc
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Emitter-Base Voltage	V_{EB}	← 8.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 8.0 → 16			Adc
Base Current	I_B	← 4.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 125 → 0.714			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.4	°C/W

*Indicates JEDEC Registered Data.



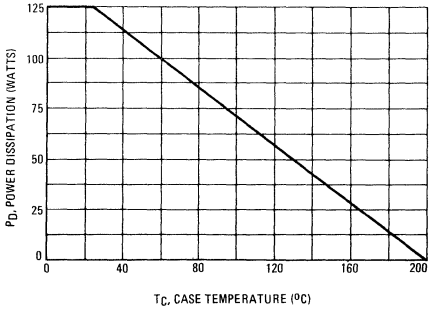
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

CASE 11-03

FIGURE 1 – POWER DERATING



*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6306		250	–	
	2N6307		300	–	
	2N6308		350	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = Rated V_{CEO}, I_B = 0)			–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 500 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6306		–	0.5	
(V_{CE} = 600 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6307		–	0.5	
(V_{CE} = 700 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6308		–	0.5	
(V_{CE} = 450 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6306		–	2.5	
(V_{CE} = 550 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6307		–	2.5	
(V_{CE} = 650 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6308		–	2.5	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 8.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		15	75	
	2N6308		12	60	
(I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		4.0	–	
	2N6308		3.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc)	2N6306		–	0.8	
	2N6307		–	1.0	
	2N6308		–	1.5	
(I_C = 8.0 Adc, I_B = 2.0 Adc)	2N6306, 2N6307		–	5.0	
(I_C = 8.0 Adc, I_B = 2.67 Adc)	2N6308		–	5.0	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 8.0 Adc, I_B = 2.0 Adc)	2N6306, 2N6307		–	2.3	
(I_C = 8.0 Adc, I_B = 2.67 Adc)	2N6308		–	2.5	
Base-Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		–	1.3	
	2N6308		–	1.5	
Second Breakdown Energy (Figure 2)		$E_{s/b}$			mJ
($I_{C(PK)}$ = 3.0 Adc, L = 40 mH, R_{BE} = 3 kΩ, V_{BB2} = 1.5 Vdc)			–	180	
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2)		f_T			MHz
(I_C = 0.3 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)			5.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	250	
SWITCHING CHARACTERISTICS					
Rise Time		t_r			µs
(V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_B = 0.6 Adc)			–	0.6	
Storage Time (3)		t_s			µs
(V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)					
	Pulse Width = 25 µs		–	1.6	
	Pulse Width = 5.0 µs		–	0.8	
Fall Time		t_f			µs
(V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)			–	0.4	

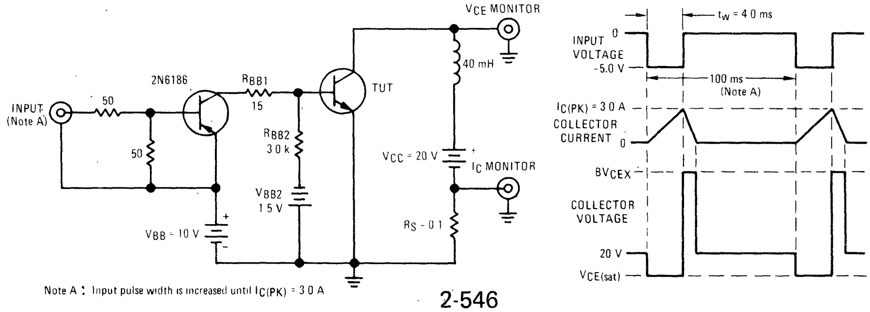
(1) Pulse Test Pulse Width ≤300 µs, Duty Cycle = 2.0%

(2) $f_T = |h_{fe}| \bullet f_{test}$

(3) "On" time is 25 µs t_s decreases with shorter pulse widths, being approximately 50% of the values shown at a 5.0 µs pulse width

*Indicates JEDEC Registered Data.

FIGURE 2 – SECOND BREAKDOWN ENERGY TEST CIRCUIT AND WAVEFORMS



Note A : Input pulse width is increased until $I_{C(PK)}$ = 3.0 A

FIGURE 3 – THERMAL RESPONSE

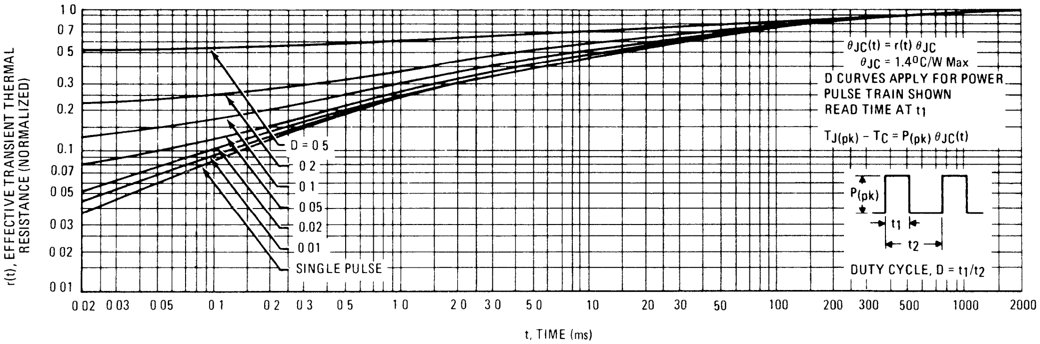
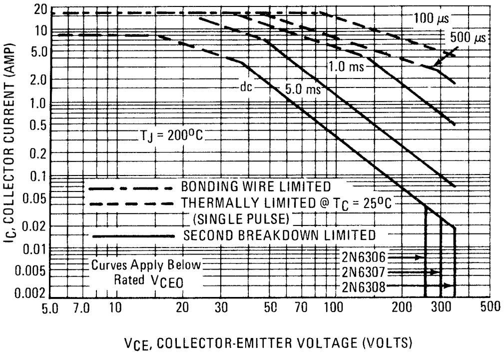


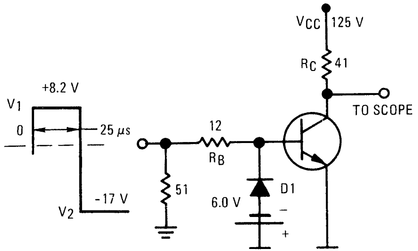
FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 5 – SWITCHING TIMES TEST CIRCUIT



DUTY CYCLE 1%
t_r, $t_f \leqslant 10$ ns
D_1 – 1N3879
COLLECTOR-BASE JUNCTION

FOR DATA IN FIGURE 6, R_B & R_C ARE VARIED TO OBTAIN DESIRED TEST CONDITIONS. D_1 OMITTED AND V_2 REDUCED TO 5.0 V FOR t_d and t_r MEASUREMENTS

FIGURE 6 – TURN-ON AND TURN-OFF TIMES

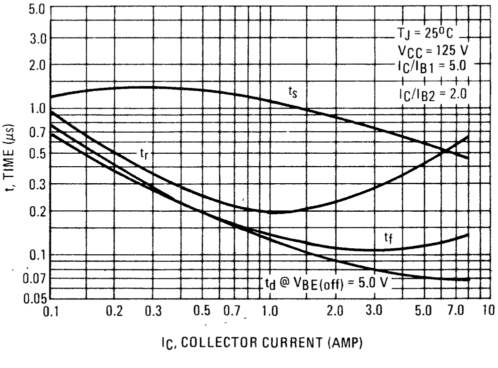


FIGURE 7 – DC CURRENT GAIN

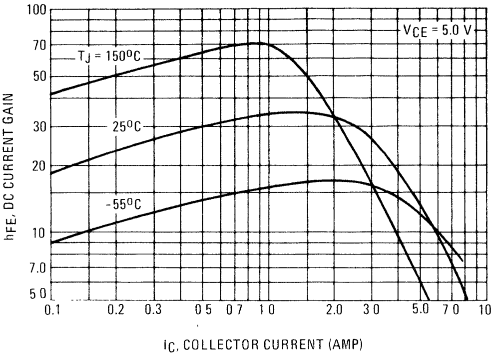


FIGURE 8 – COLLECTOR SATURATION REGION

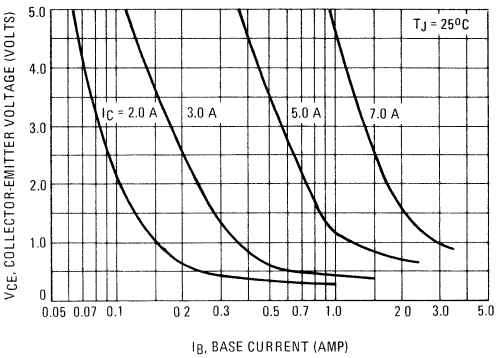


FIGURE 9 – "ON" VOLTAGES

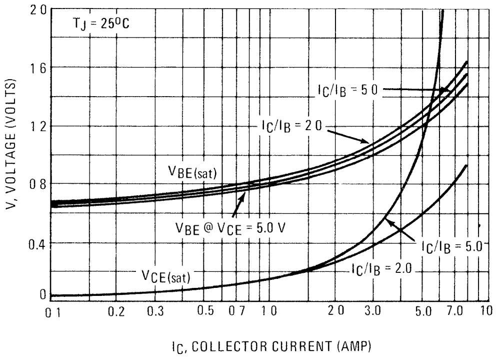


FIGURE 10 – TEMPERATURE COEFFICIENTS

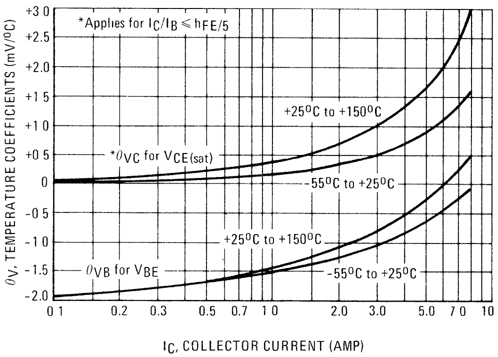


FIGURE 11 – COLLECTOR-CUTOFF REGION

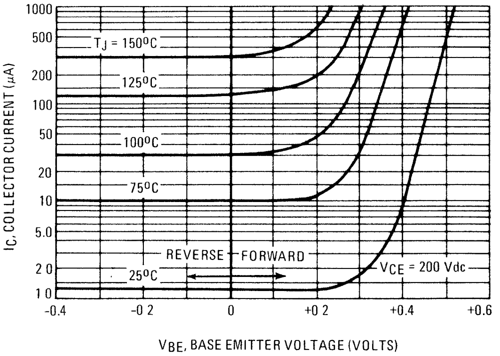
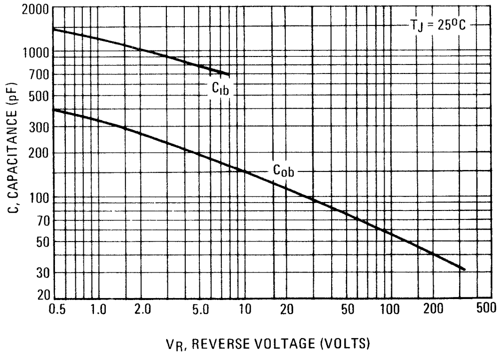


FIGURE 12 – CAPACITANCE



2N6312 thru 2N6314

For Specifications, See 2N4231A Data, Volume I.

2N6315 thru 2N6318

For Specifications, See 2N5871 Data.

2N6338 (SILICON)
thru
2N6341

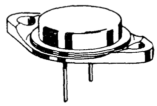
HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N6338
  = 120 Vdc (Min) – 2N6339
  = 140 Vdc (Min) – 2N6340
  = 150 Vdc (Min) – 2N6341
- High DC Current Gain –
  h_{FE} = 30-120 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 μs (Max)
  t_s = 1.0 μs (Max)
  t_f = 0.25 μs (Max)
- Hard Solder Construction

25 AMPERE
POWER TRANSISTORS
NPN SILICON

100, 120, 140, 150 VOLTS
200 WATTS



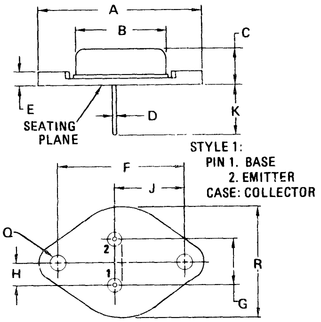
*MAXIMUM RATINGS

Rating	Symbol	2N6338	2N6339	2N6340	2N6341	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	6.0				Vdc
Collector Current – Continuous Peak	I_C	25 50				Adc
Base Current	I_B	10				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data



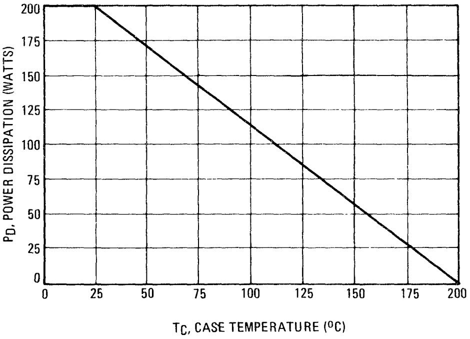
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01

FIGURE 1 – POWER DERATING



***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

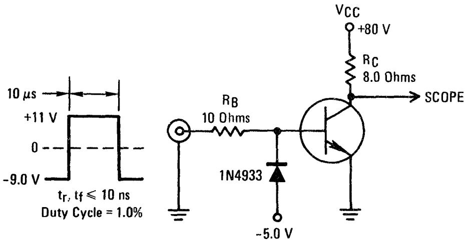
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6338		100	–	
	2N6339		120	–	
	2N6340		140	–	
	2N6341		150	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6338		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6339		–	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6340		–	50	
(V_{CE} = 75 Vdc, I_B = 0)	2N6341		–	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)			–	10	μAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			–	1.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			50	–	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			30	120	
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			12	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.0	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	1.8	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.8	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	2.5	
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	300	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 6.0 Vdc)		t_r	–	0.3	μs
Storage Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	–	1.0	μs
Fall Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

(2) $f_T = |h_{fe}| \cdot f_{test}$.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN-ON TIME

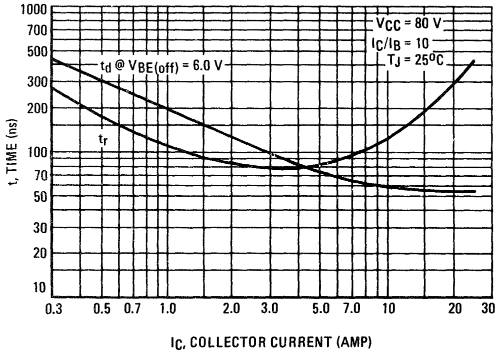


FIGURE 4 – THERMAL RESPONSE

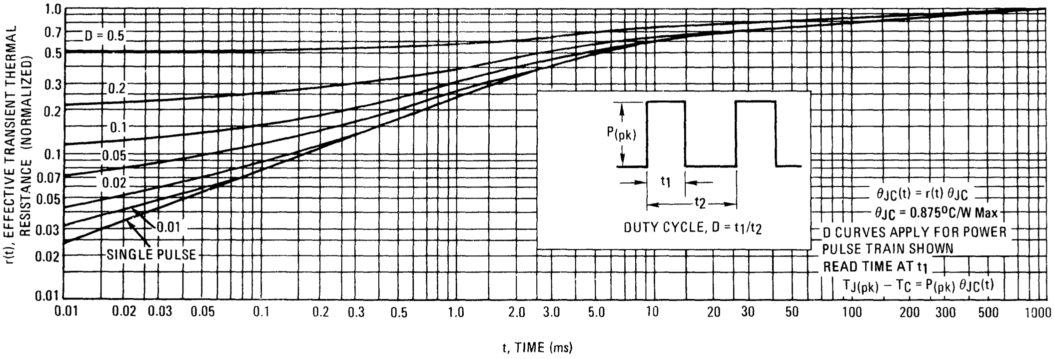
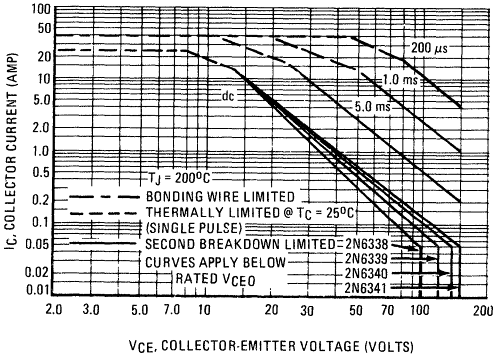


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

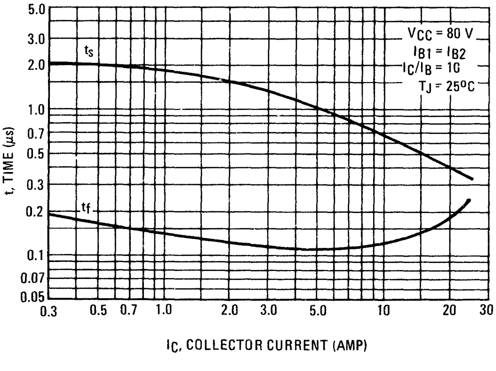


FIGURE 7 – CAPACITANCE

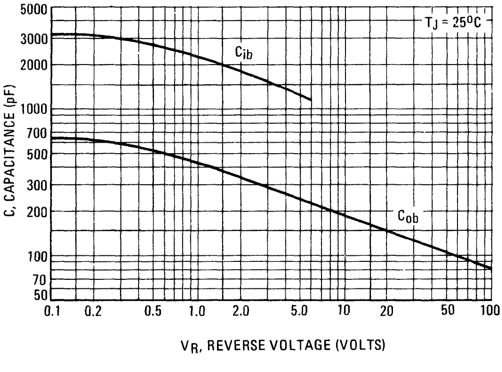


FIGURE 8 – DC CURRENT GAIN

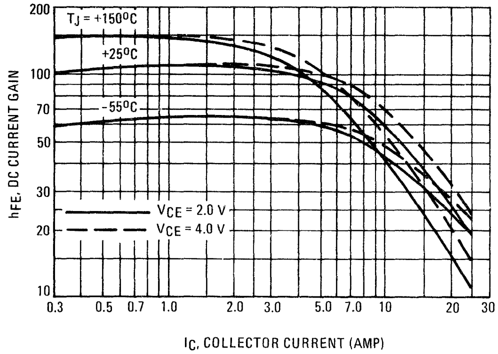


FIGURE 9 – COLLECTOR SATURATION REGION

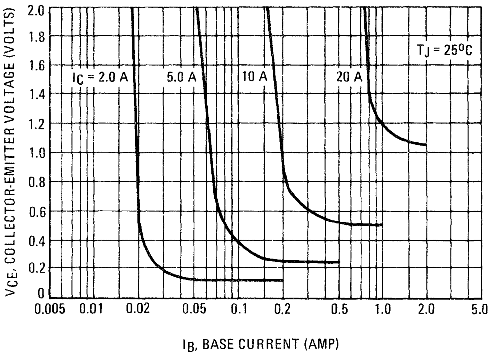


FIGURE 10 – "ON" VOLTAGES

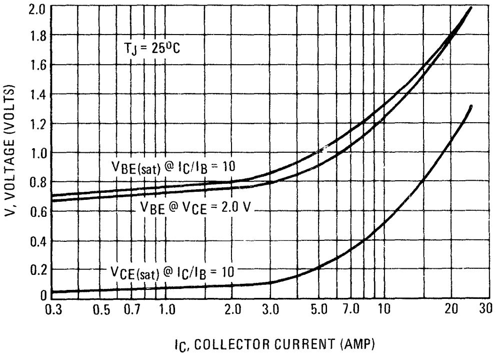


FIGURE 11 – TEMPERATURE COEFFICIENTS

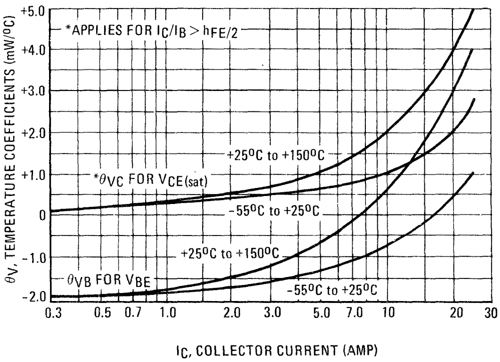


FIGURE 12 – COLLECTOR CUT-OFF REGION

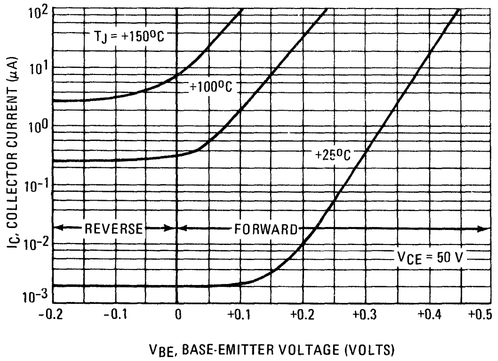
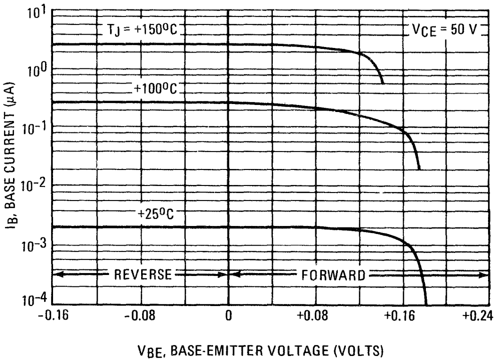
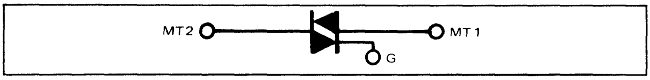


FIGURE 13 – BASE CUT-OFF REGION



2N6342 (SILICON)
thru
2N6349



SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342, 2N6343, 2N6344, 2N6345) or Four Modes (2N6346, 2N6347, 2N6348, 2N6349)
- For 400 Hz Operation, Consult Factory
- 12 Ampere Devices Available as 2N6342A thru 2N6349A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
* Repetitive Peak Off-State Voltage, Note 1 (T_J = -40 to +100°C) ½ Sine Wave 50 to 60 Hz, Gate Open 2N6342, 2N6346 2N6343, 2N6347 2N6344, 2N6348 2N6345, 2N6349	V_{DRM}	 200 400 600 800	Volts
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)	$I_{T(RMS)}$	8.0 4.0	Amp
*Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = +80°C) preceded and followed by 10 Rated Current	I_{TSM}	100	Amp
Circuit Fusing Considerations (T_J = -40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width ≤ 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

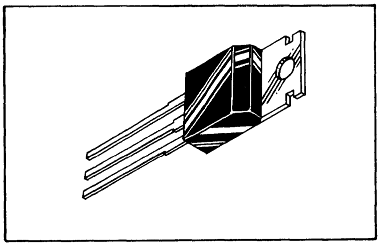
Characteristic	Symbol	Max	Unit
* Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

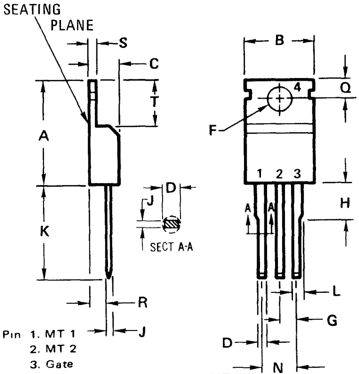
*Indicates JEDEC Registered Data

TRIACS (THYRISTORS)

8 AMPERES RMS

200-800 VOLTS





Pin 1. MT 1
2. MT 2
3. Gate
4. Mounting Tab Common to MT 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB

All JEDEC dimensions and notes apply

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

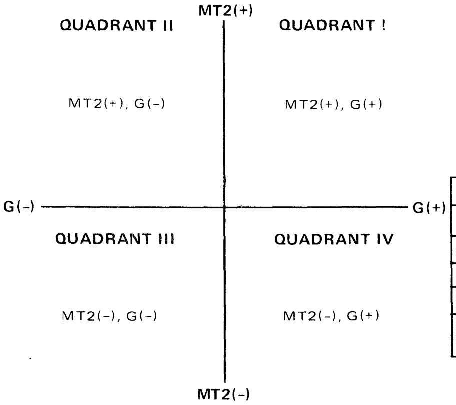
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage (Either Direction) I_{TM} = 11 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.55	Volts
Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	I_{GTM}				mA
MT2 (+), G(+) All Types		–	6.0	50	
MT2 (+), G(-) 2N6346 thru 2N6349		–	6.0	75	
MT2 (-), G(-) All Types		–	10	50	
MT2 (-), G(+) 2N6346 thru 2N6349		–	25	75	
*MT2 (+), G(+); MT2 (-), G(-) T_C = -40°C All Types		–	–	100	
*MT2 (+), G(-); MT2 (-), G(+) T_C = -40°C 2N6346 thru 2N6349		–	–	125	
Peak Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	V_{GTM}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(-) 2N6346 thru 2N6349		–	0.9	2.5	
MT2 (-), G(-) All Types		–	1.1	2.0	
MT2 (-), G(+) 2N6346 thru 2N6349		–	1.4	2.5	
*MT2 (+), G(+); MT2 (-), G(-) T_C = -40°C All Types		–	–	2.5	
*MT2 (+), G(-); MT2 (-), G(+) T_C = -40°C 2N6346 thru 2N6349		–	–	3.0	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 100°C					
*MT2 (+), G(+); MT2 (-), G(-) All Types		0.2	–	–	
*MT2 (+), G(-); MT2 (-), G(-) 2N6346 thru 2N6349		0.2	–	–	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA	I_H				mA
T_C = 25°C		–	6.0	40	
T_C = -40°C		–	–	75*	
*Turn-On Time Rated V_{DRM}, I_{TM} = 11 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 11 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C	dv/dt	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 – 10 V	7.5 – 9.0 V	3.0 – 5.0 V
I_S	350 μA Max	120 μA Max	100 – 400 μA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

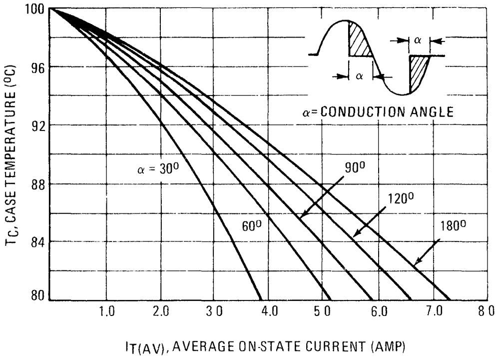


FIGURE 2 – RMS CURRENT DERATING

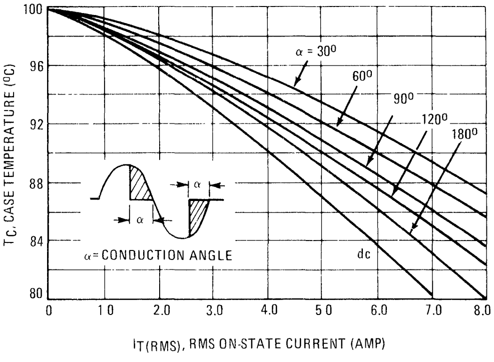


FIGURE 3 – ON-STATE POWER DISSIPATION

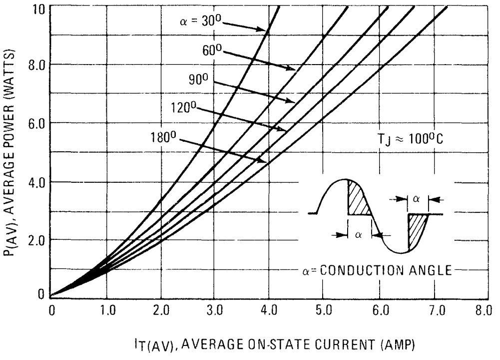


FIGURE 4 – ON-STATE POWER DISSIPATION

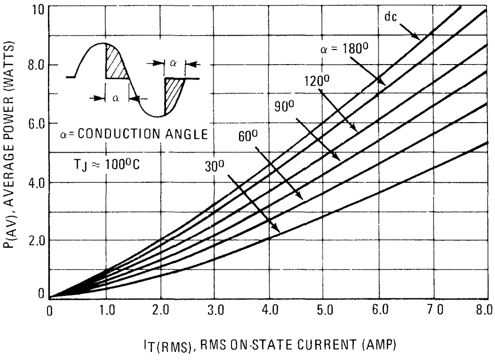


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

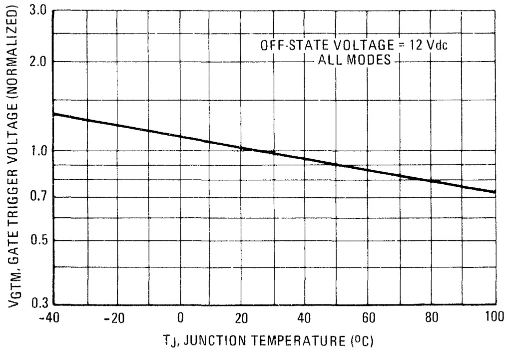


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

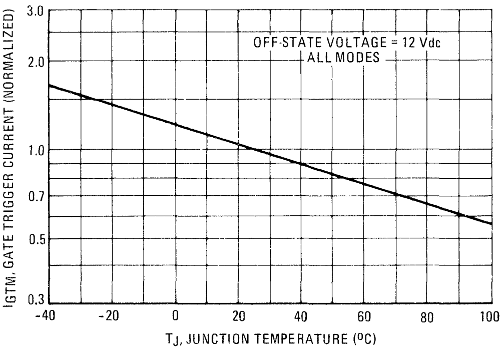


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

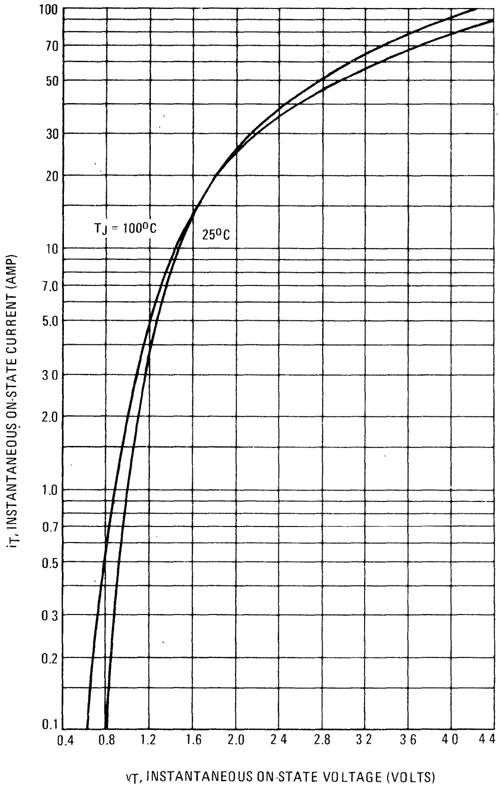


FIGURE 8 – TYPICAL HOLDING CURRENT

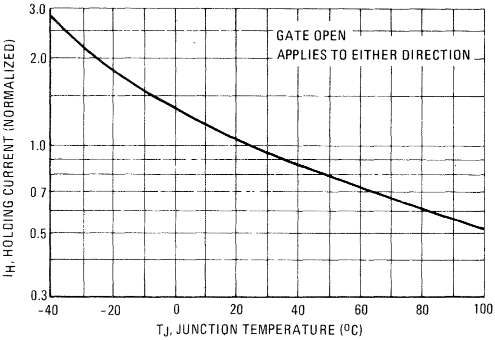


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

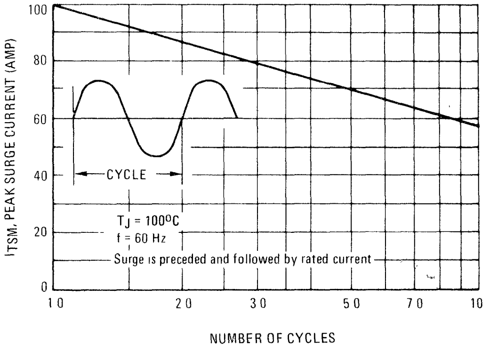
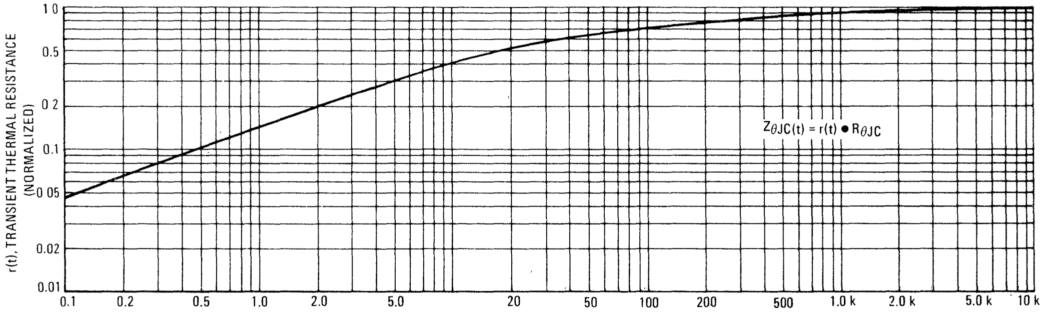


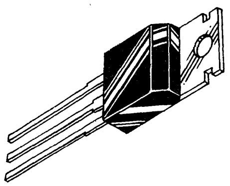
FIGURE 10 – THERMAL RESPONSE



2N6342A (SILICON)
thru
2N6349A

TRIACS
(THYRISTORS)

12 AMPERES RMS
200 – 800 VOLTS



SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342A, 2N6343A, 2N6344A, 2N6345A) or Four Modes (2N6346A, 2N6347A, 2N6348A, 2N6349A)
- For 400 Hz Operation, Consult Factory
- 8 Ampere Devices Available as 2N6342 thru 2N6349

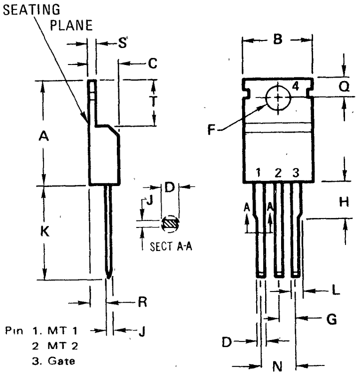
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage, Note 1 (T_J = -40 to +110°C) ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
2N6342A, 2N6346A		200	
2N6343A, 2N6347A		400	
2N6344A, 2N6348A		600	
2N6345A, 2N6349A		800	
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +95°C)	$I_{T(RMS)}$	12 6.0	Amp
*Peak Surge Current (One Full Cycle, 60 Hz, T_C = +80°C) preceded and followed by rated current	I_{TSM}	120	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2.0 μs	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-40 to +110	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

*Indicates JEDEC Registered Data.



Pin 1. MT 1
2. MT 2
3. Gate
4. Mounting Tab Common to MT 2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2 79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB

All JEDEC dimensions and notes apply

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

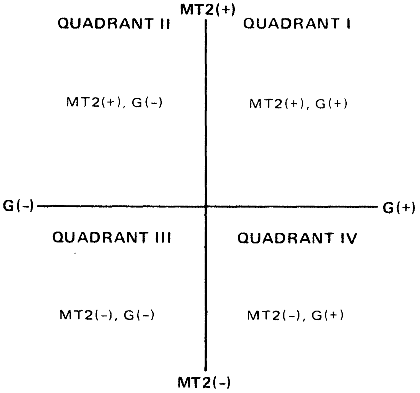
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage (Either Direction) I_{TM} = 17 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.75	Volts
Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 µs	I_{GTM}				mA
MT2 (+), G(+) All Types		–	6.0	50	
MT2 (+), G(-) 2N6346A thru 2N6349A		–	6.0	75	
MT2 (-), G(-) All Types		–	10	50	
MT2 (-), G(+) 2N6346A thru 2N6349A		–	25	75	
*MT2 (+), G(+); MT2 (-), G(-) T_C = -40°C All Types		–	–	100	
*MT2 (+), G(-); MT2 (-), G(+) T_C = -40°C 2N6346A thru 2N6349A		–	–	125	
Peak Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 µs	V_{GTM}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(-) 2N6346A thru 2N6349A		–	0.9	2.5	
MT2 (-), G(-) All Types		–	1.1	2.0	
MT2 (-), G(+) 2N6346A thru 2N6349A		–	1.4	2.5	
*MT2 (+), G(+); MT2 (-), G(-) T_C = -40°C All Types		–	–	2.5	
*MT2 (+), G(-); MT2 (-), G(+) T_C = -40°C 2N6346A thru 2N6349A		–	–	3.0	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C					
*MT2 (+), G(+); MT2 (-), G(-) All Types		0.2	–	–	
*MT2 (+), G(-); MT2 (-), G(+) 2N6346A thru 2N6349A		0.2	–	–	
Holding Current (Either Direction)	I_H				mA
Main Terminal Voltage = 12 Vdc, Gate Open, T_C = 25°C		–	6.0	40	
Initiating Current = 200 mA T_C = -40°C		–	–	75*	
*Turn-On Time Rated V_{DRM}, I_{TM} = 17A I_{GT} = 120 mA, Rise Time = 0.1 µs, Pulse Width = 2.0 µs	tgt	–	1.5	2.0	µs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 17A, Commutating di/dt = 6.5 A/ms, Gate Unenergized T_C = 80°C	dv/dt	–	5.0	–	V/µs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 – 10 V	7.5 – 9.0 V	3.0 – 5.0 V
I_S	350 µA Max	120 µA Max	100 – 400 µA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

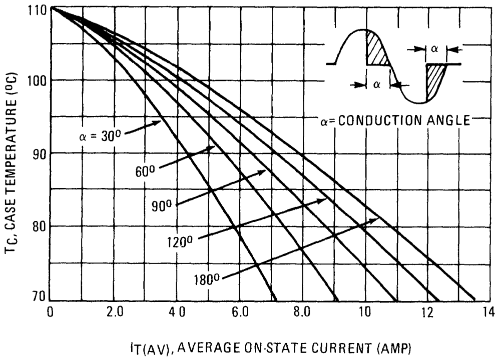


FIGURE 2 – RMS CURRENT DERATING

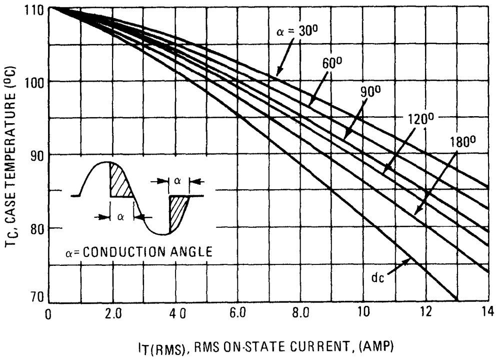


FIGURE 3 – ON-STATE POWER DISSIPATION

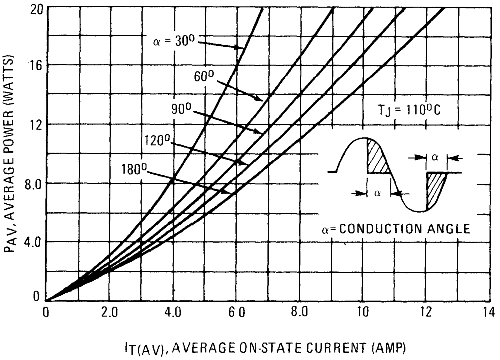


FIGURE 4 – ON-STATE POWER DISSIPATION

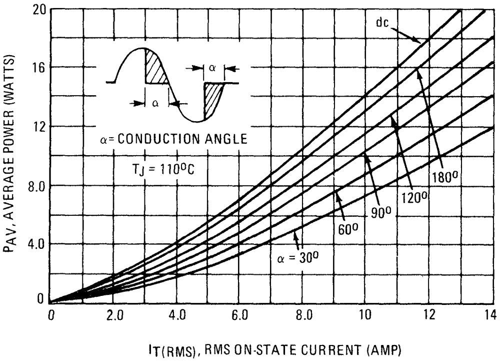


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

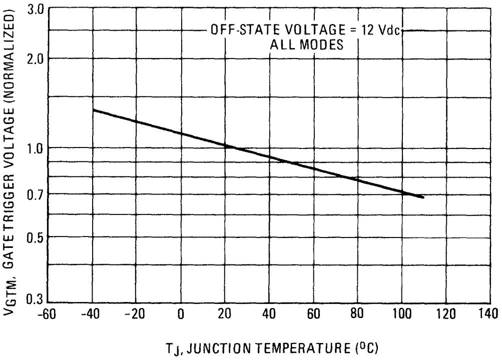


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

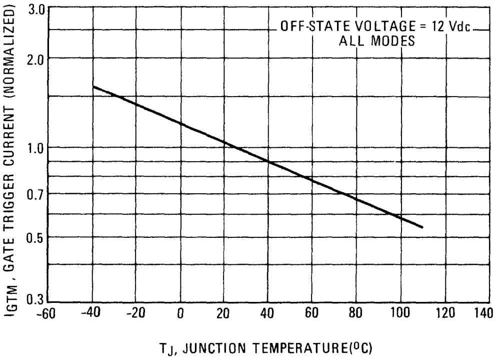


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

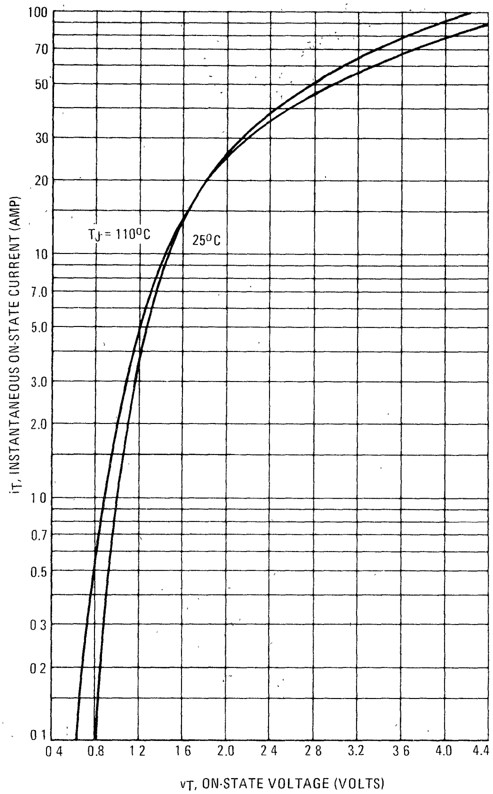


FIGURE 8 – TYPICAL HOLDING CURRENT

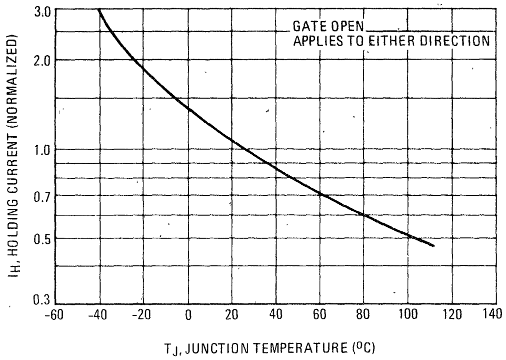


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

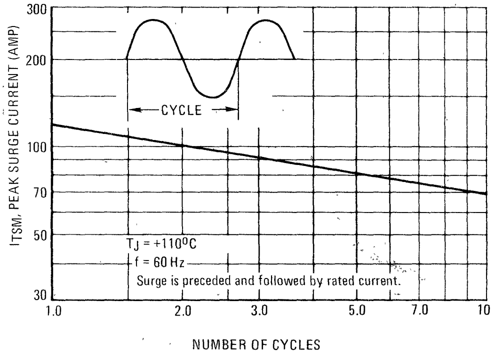
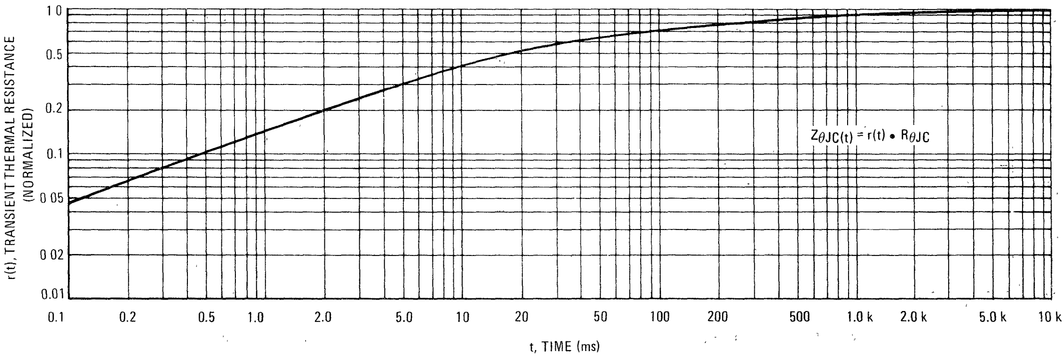


FIGURE 10 – THERMAL RESPONSE



2N6365, 2N6365A (GERMANIUM)

PNP GERMANIUM RF AMPLIFIER TRANSISTORS

. . . designed for use in high gain RF amplifier applications.

- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 25 Vdc (Min) @ I_C = 200 µAdc
- High Power Gain –
  G_{pe} = 30 dB (Typ) @ V_{CE} = 6.0 Vdc, f = 10 MHz
- Low Collector-Base Capacitance –
  C_{cb} = 2.0 pF (Max) @ V_{CB} = 10 Vdc

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage (1)	V_{CEO}	10	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	1.0	Vdc
Collector Current – Continuous	I_C	100	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	150 2.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +100	°C

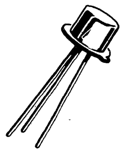
THERMAL CHARACTERISTICS

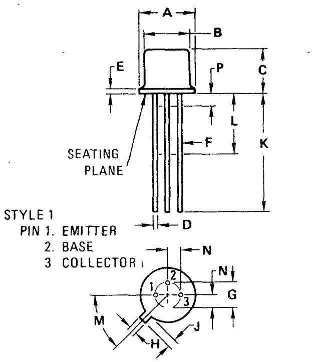
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(2)	500	°C/W

(1) Applicable from 10 µA to 10 mA

(2) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

PNP GERMANIUM
RF AMPLIFIER
TRANSISTORS





STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6,35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

CASE 22
TO-18

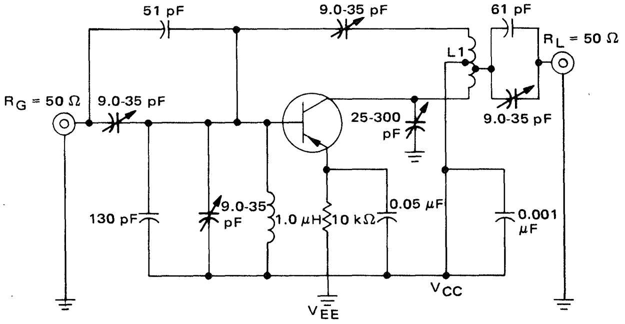
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 200 μAdc, V_{BE} = 0)	BV_{CES}	25	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	1.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 0.5 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc) 2N6365 2N6365A	h_{FE}	 20 20	 50 –	 100 80	–
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc) 2N6365 2N6365A	$V_{BE(sat)}$	 – –	 0.40 0.38	 0.50 0.42	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	200	500	800	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	1.0	2.0	pF
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc, f = 10 MHz)	h_{fe}	16	–	63	–
Input Resistance (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc, f = 250 MHz)	$Re(h_{ie})$	25	–	250	Ohms
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (V_{CE} = 6.0 Vdc, I_C = 1.0 mAdc, f = 10 MHz)	G_{pe}	25	30	–	dB

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 1 — POWER GAIN TEST CIRCUIT



L1 = 24 Turns of #28 AWG Wire
Load Tap — 5 Turns from Collector End
Supply Tap — 15 Turns from Collector End
Neutralization — 9 Turns

2N6366 (SILICON)

The RF Line

NPN SILICON RF POWER TRANSISTOR

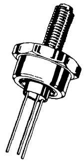
. . . designed for operation in driver and predriver stages for high power linear amplifiers, 2.0 to 30 MHz.

- Optimized for Operation from a 12.5 Volt Supply
- Power Gain @ 2.5 W (PEP) = 17 dB (Min)
- Intermodulation Distortion at Rated Power Output
  IMD = -35 dB (Max)

2.5 W (PEP)-30 MHz

**RF POWER
TRANSISTOR**

NPN SILICON

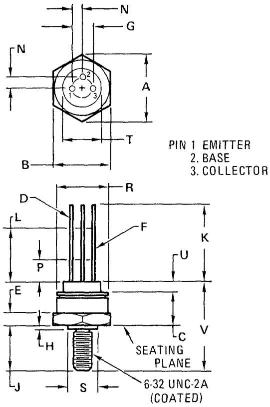


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	18	Vdc
*Collector-Base Voltage	V_{CBO}	36	Vdc
*Emitter-Base Voltage	V_{EBO}	4.0	Vdc
*Collector Current — Continuous	I_C	1.0	Adc
*Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 57.2	Watts mW/°C
*Storage Temperature Range	T_{stg}	-65 to +200	°C
Maximum Stud Torque (1)	–	2.1	in.-lb.

*Indicates JEDEC Registered Data.

(1) For repeated assembly use 1.8 in-lb maximum.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.49	11.00	0.413	0.433
B	9.19	9.53	0.362	0.375
C	5.33	5.72	0.210	0.225
D	0.406	0.533	0.016	0.021
E	1.65	1.78	0.065	0.070
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.508	0.889	0.020	0.035
J	6.73	7.42	0.265	0.292
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050
R	8.89	9.14	0.350	0.360
S	4.45	4.83	0.175	0.190
T	4.11	4.29	0.162	0.169
U	1.14	1.52	0.045	0.060

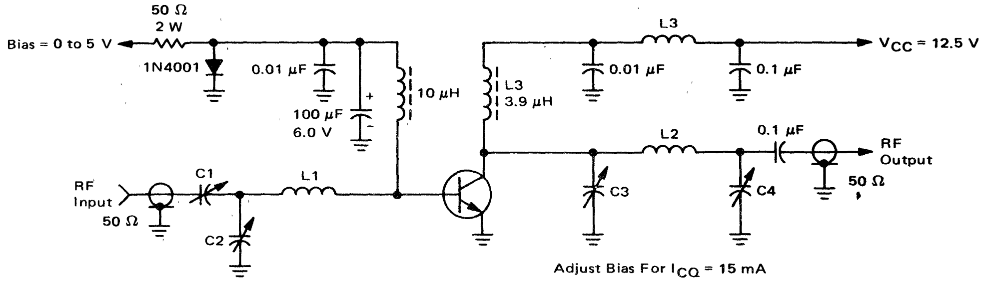
CASE 24
TO-102

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	BV_{CEO}	18	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	BV_{CES}	36	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.25 mAdc, I_C = 0)	BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_A = 125°C)	I_{CES}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	50	–
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 150 mAdc, V_{CE} = 12.5 Vdc, f = 50 MHz)	f_T	50	–	MHz
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	20	pF
FUNCTIONAL TESTS (Figure 1)				
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 2.5 W (PEP), f_1 = 30 MHz, f_2 = 30,001 MHz)	G_{PE}	17	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 2.5 W (PEP), f_1 = 30 MHz, f_2 = 30,001 MHz)	η	38.5	–	%
Intermodulation Distortion (V_{CC} = 12.5 Vdc, P_{out} = 2.5 W (PEP), f_1 = 30 MHz, f_2 = 30,001 MHz)	IMD	–	-35	dB

*Indicates JEDEC Registered Data

FIGURE 1 — 30 MHz TEST CIRCUIT



Adjust Bias For I_{CQ} = 15 mA

C1, C2	80-480 pF, ARCO 466 or equivalent
C3, C4	25-280 pF, ARCO 464 or equivalent
L1	0.1 µH Molded Choke
L2	0.15 µH Molded Choke
L3	Ferrite Choke, FERROXCUBE VK200 01-03B or equivalent

FIGURE 2 – LINEAR OUTPUT POWER versus FREQUENCY

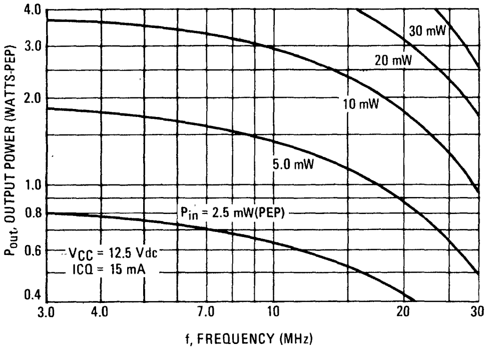


FIGURE 3 – OUTPUT POWER versus INPUT POWER (30 MHz)

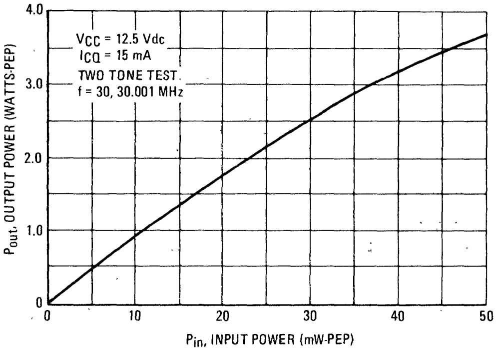


FIGURE 4 – OUTPUT POWER versus INPUT POWER (12 MHz)

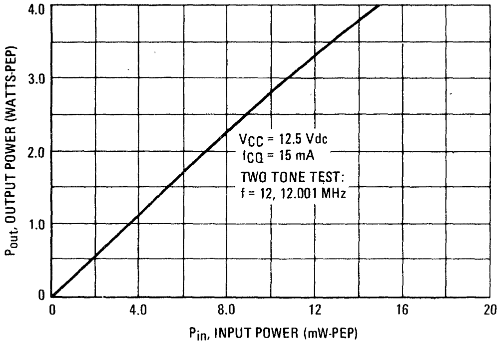


FIGURE 5 – OUTPUT POWER versus INPUT POWER (3.0 MHz)

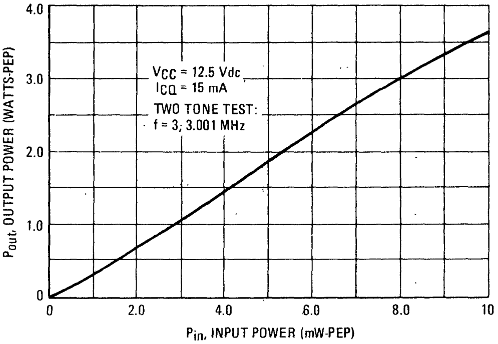


FIGURE 6 – INTERMODULATION DISTORTION versus OUTPUT POWER

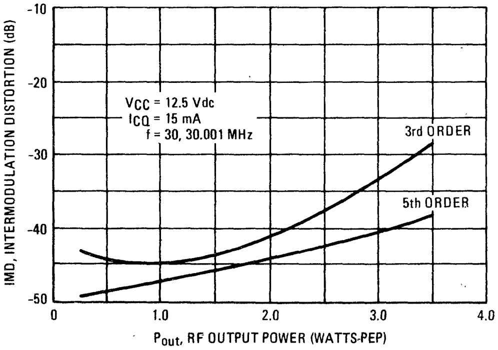


FIGURE 7 – LINEAR OUTPUT POWER versus SUPPLY VOLTAGE

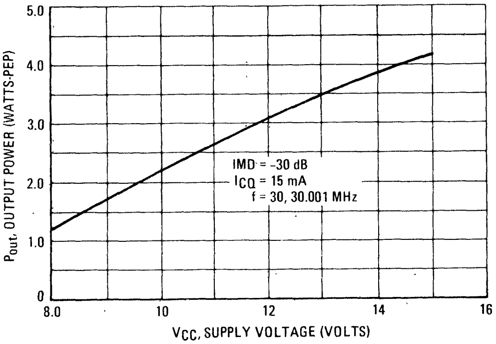


FIGURE 8 – PARALLEL EQUIVALENT INPUT RESISTANCE

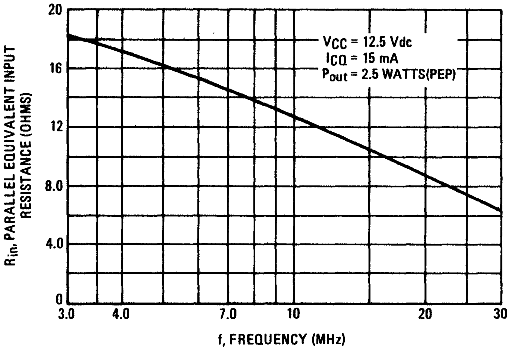


FIGURE 9 – PARALLEL EQUIVALENT INPUT CAPACITANCE

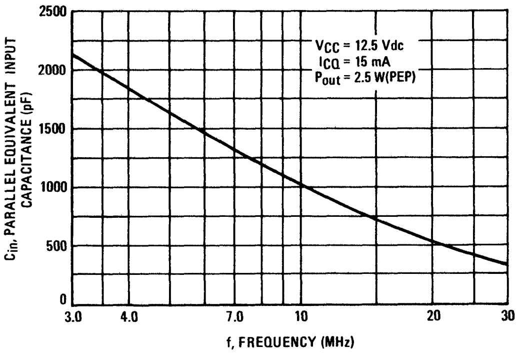


FIGURE 10 – PARALLEL EQUIVALENT OUTPUT RESISTANCE

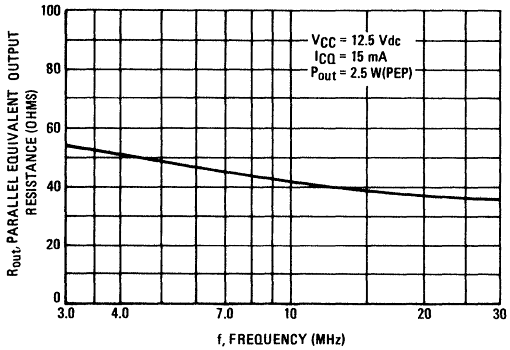


FIGURE 11 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE

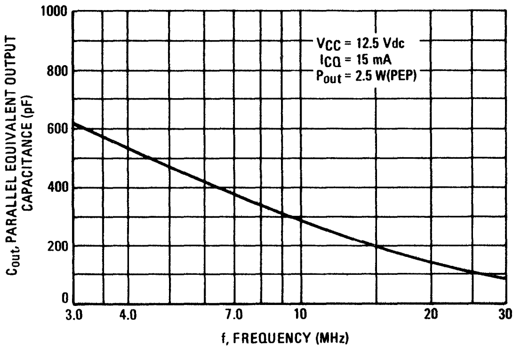


FIGURE 12 – CURRENT-GAIN – BANDWIDTH PRODUCT

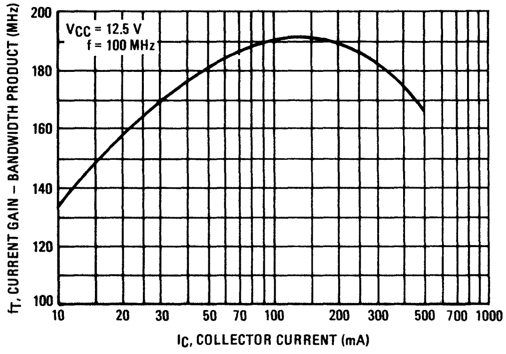


FIGURE 13 – COLLECTOR CURRENT versus BASE-EMITTER VOLTAGE

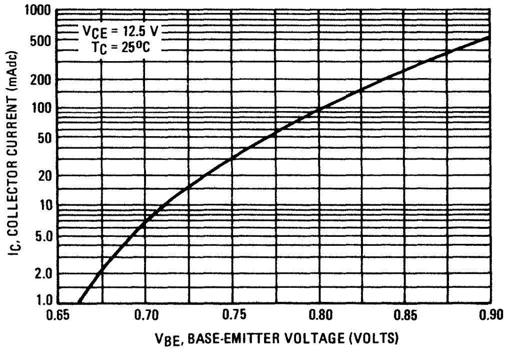


FIGURE 14 – OUTPUT CAPACITANCE versus VOLTAGE

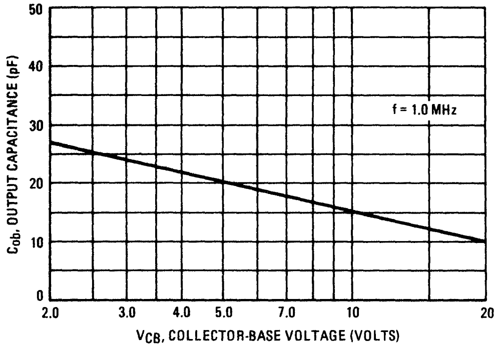


FIGURE 15 – INPUT CAPACITANCE versus VOLTAGE

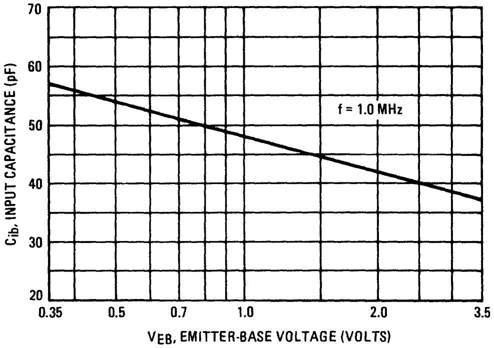


FIGURE 16 – DC SAFE OPERATING AREA

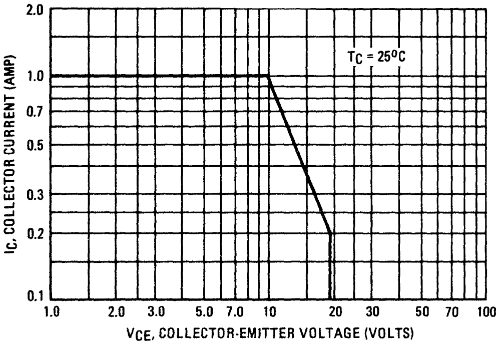
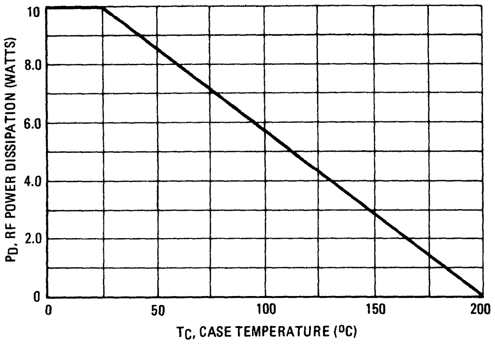


FIGURE 17 – RF POWER DISSIPATION



2N6367 (SILICON)

The RF Line

NPN SILICON RF POWER TRANSISTOR

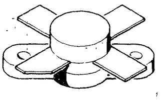
. . . designed primarily for driver applications in 12.5 volt single-sideband amplifiers from 2.0 to 30 MHz.

- Optimized for Operation from a 12.5 Volt Supply
- Power Output @ 12.5 Vdc, 30 MHz – 9.0 W (PEP)
- Intermodulation Distortion at Rated Power Output –
  IMD = -30 dB (Max)

9 W (PEP) – 30 MHz

RF POWER
TRANSISTOR

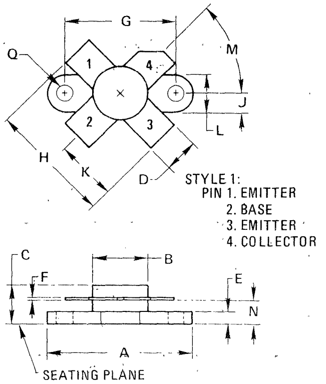
NPN SILICON



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.114	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

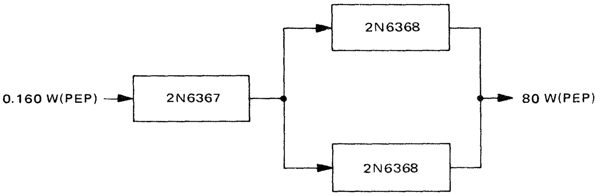


STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24 64	24.89	0.970	0.980
B	9.47	9.73	0.373	0 383
C	6.07	7.14	0.239	0.281
D	5.59	5.84	0.220	0.230
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	21 59	22.10	0.850	0.870
J	3.12	3.23	0.123	0.127
K	10.80	11.05	0.425	0.435
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.97	3.12	0.117	0.123

CASE 211-01

TYPICAL DRIVER APPLICATION
2-30 MHz WIDE BAND AMPLIFIER

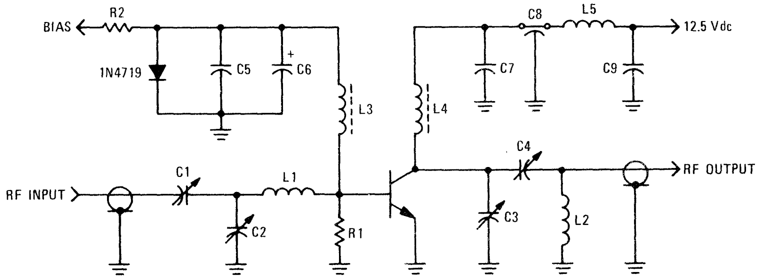


*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	BV_{CEO}	18	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	BV_{CES}	36	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 55°C)	I_{CES}	–	10	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	50	–
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 12.5 Vdc, f = 50 MHz)	f_T	50	–	MHz
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	90	pF
FUNCTIONAL TESTS				
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 9.0 W(PEP), $I_{C(max)}$ = 1.0 Adc, f_1 = 30 MHz, f_2 = 30.001 MHz)	G_{PE}	14	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 9.0 W(PEP), $I_{C(max)}$ = 1.0 Adc, f_1 = 30 MHz, f_2 = 30.001 MHz)	η	36	–	%
Intermodulation Distortion (V_{CC} = 12.5 Vdc, P_{out} = 9.0 W(PEP), $I_{C(max)}$ = 1.0 Adc, f_1 = 30 MHz, f_2 = 30.001 MHz)	IMD	–	-30	dB

*Indicates JEDEC Registered Data

FIGURE 1 – 30 MHz TEST CIRCUIT



C1, C3	25-280 pF, ARCO 464 OR EQUIVALENT	L2	5 TURNS #18 AWG, 1/4" ID, 5/16" LONG (0.13 μH)
C2, C4	170-780 pF, ARCO 469 OR EQUIVALENT	L3	3.3 μH
C5, C7, C9	0.1 μF	L4	1.0 μH
C6	500 μF TANTALUM	L5	FERROXCUBE VK 200 20/4B
C8	680 pF FEED THRU	R1	10 OHMS
L1	3 TURNS #18 AWG, 1/4" ID, 1/4" LONG (60 nH)	R2	50 OHMS

ADJUST BIAS FOR I_{CQ} = 35 mA WITH NO RF SIGNAL APPLIED

FIGURE 2 – LINEAR OUTPUT POWER versus FREQUENCY

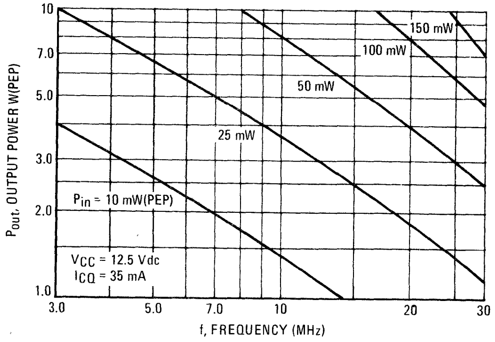


FIGURE 3 – OUTPUT POWER versus INPUT POWER

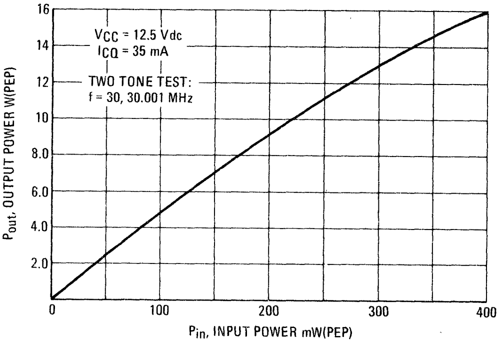


FIGURE 4 – OUTPUT POWER versus INPUT POWER

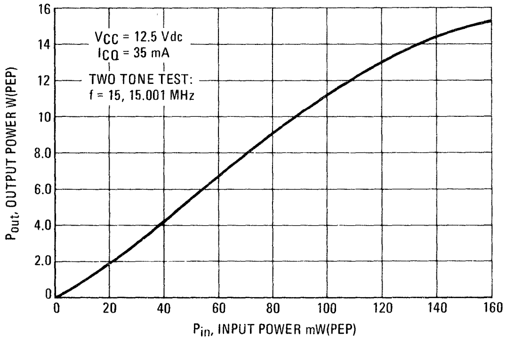


FIGURE 5 – OUTPUT POWER versus INPUT POWER

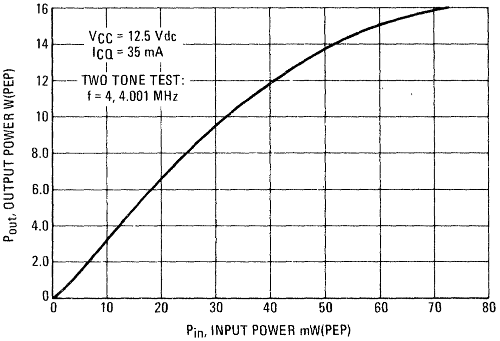


FIGURE 6 – INTERMODULATION DISTORTION versus OUTPUT POWER

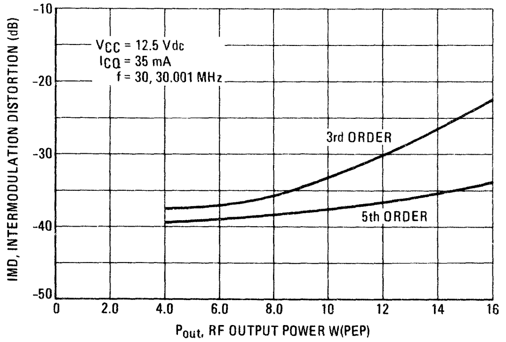


FIGURE 7 – LINEAR OUTPUT POWER versus SUPPLY VOLTAGE

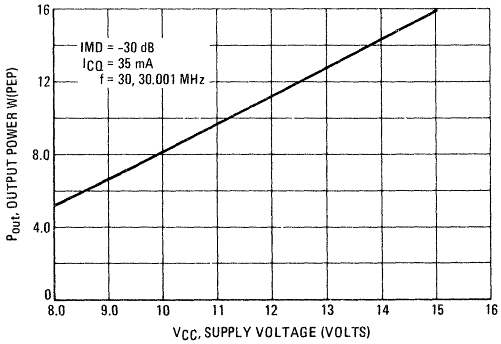


FIGURE 8 – PARALLEL EQUIVALENT INPUT RESISTANCE

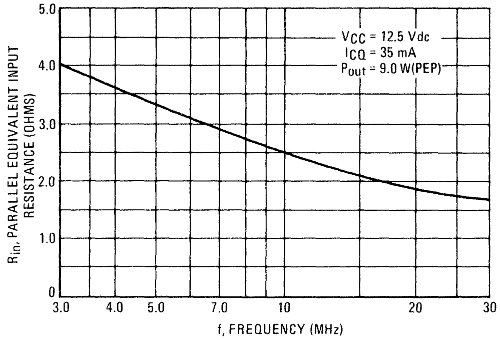


FIGURE 9 – PARALLEL EQUIVALENT INPUT CAPACITANCE

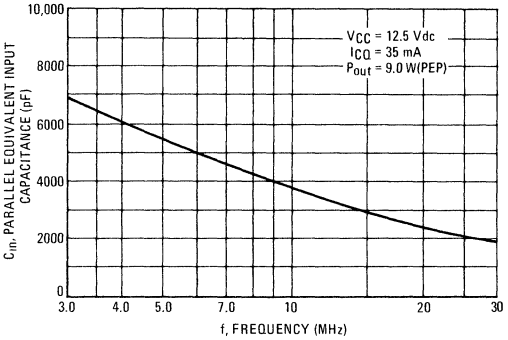


FIGURE 10 – PARALLEL EQUIVALENT OUTPUT RESISTANCE

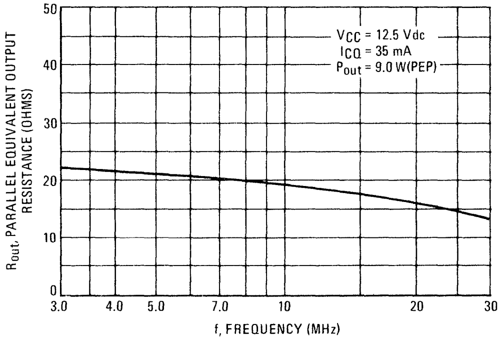


FIGURE 11 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE

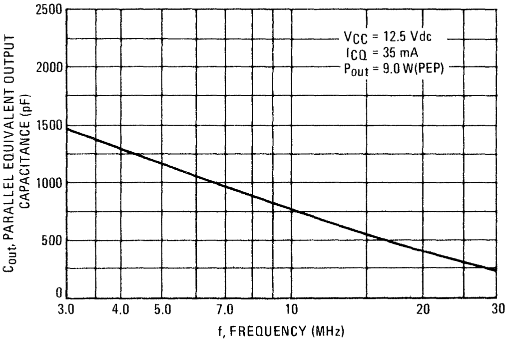


FIGURE 12 – CURRENT-GAIN – BANDWIDTH PRODUCT

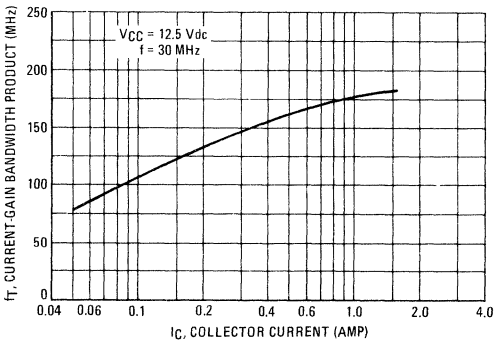


FIGURE 13 – COLLECTOR CURRENT versus BASE-EMITTER VOLTAGE

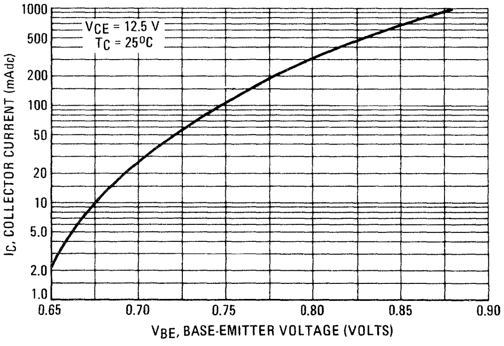


FIGURE 14 – OUTPUT CAPACITANCE

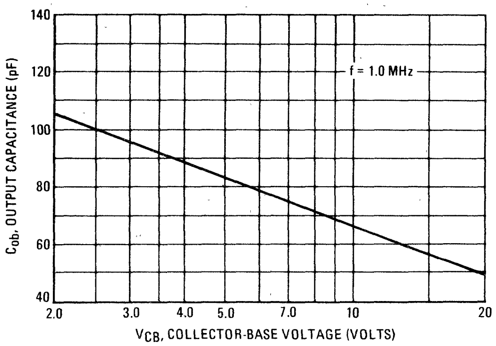


FIGURE 15 – INPUT CAPACITANCE

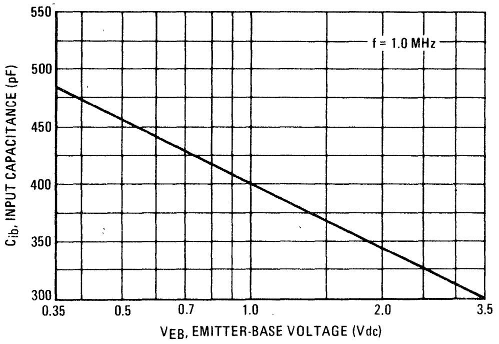


FIGURE 16 – DC SAFE OPERATING AREA

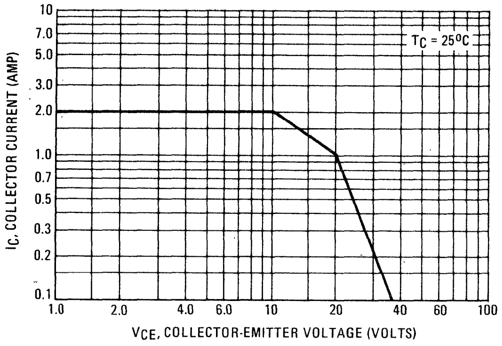
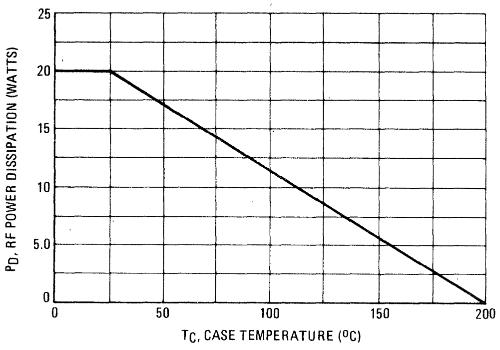


FIGURE 17 – RF POWER DISSIPATION



2N6368 (SILICON)

The RF Line

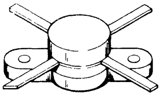
NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for applications as a high-power linear amplifier from 2.0 to 30 MHz.

- Optimized for Operation from a 12.5 Volt Supply
- Power Output @ 12.5 Vdc, 30 MHz = 40 W (PEP)
- Power Gain @ 30 MHz = 10 dB (Min)
- Intermodulation Distortion at Rated Power Output – IMD = -30 dB (Max)
- Isothermal-Resistor Design Results in Rugged Device

40 W (PEP) – 30 MHz

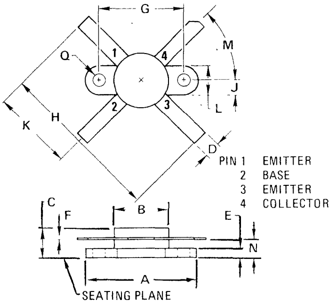
RF POWER TRANSISTOR
NPN SILICON



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	4 0	Vdc
Collector Current – Continuous	I_C	8.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	140 0.8	Watts $W/^oC$
Storage Temperature Range	T_{stg}	-65 to +200	^oC

*Indicates JEDEC Registered Data



PIN 1 EMITTER
2 BASE
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.64	24.89	0 970	0.980
B	11.81	12 07	0.465	0.475
C	5 82	6.73	0.229	0 265
D	2.16	3.94	0.085	0.155
E	2.13	2 54	0.084	0.100
F	0.10	0 15	0.004	0.006
G	18 29	18.54	0.720	0.730
H	35.56	38.10	1.400	1 500
J	3.12	3.23	0.123	0.127
K	17.78	19 05	0 700	0.750
L	6.22	6.48	0.245	0.255
M	40^0	50^0	40^0	50^0
N	3.66	4.32	0 144	0 170
Q	2 97	3 12	0 117	0.123

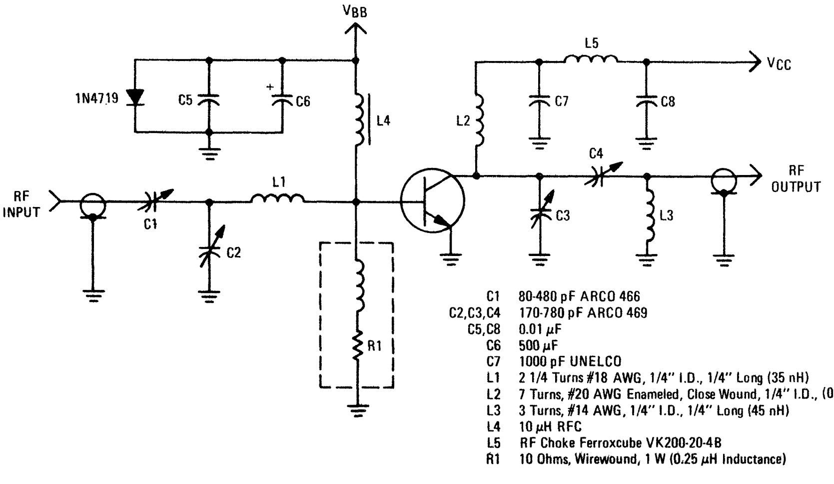
CASE 211-02

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	BV_{CEO}	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	BV_{CES}	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 12.5 Vdc, V_{BE} = 0, T_C = +55°C)	I_{CES}	–	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	20	–	–
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 12.5 Vdc, f = 50 MHz)	f_T	50	110	–	MHz
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	300	400	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 40 W (PEP), I_C = 4.7 Adc Max, V_{CC} = 12.5 Vdc, I_{CQ} = 50 mAdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	G_{PE}	10	11.2	–	dB
Intermodulation Distortion Ratio (Figure 1) (P_{out} = 40 W (PEP), I_C = 4.7 Adc Max, V_{CC} = 12.5 Vdc, I_{CQ} = 50 mAdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	IMD	–	-35	-30	dB
Collector Efficiency (Figure 1) (P_{out} = 40 W (PEP), I_C = 4.7 Adc Max, V_{CC} = 12.5 Vdc, I_{CQ} = 50 mAdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	η	34	40	–	%

*Indicates JEDEC Registered Data.

FIGURE 1 – 30 MHz TEST CIRCUIT



C1	80-480 pF ARCO 466
C2,C3,C4	170-780 pF ARCO 469
C5,C8	0.01 µF
C6	500 µF
C7	1000 pF UNELCO
L1	2 1/4 Turns #18 AWG, 1/4" I.D., 1/4" Long (35 nH)
L2	7 Turns, #20 AWG Enameled, Close Wound, 1/4" I.D., (0.2 µH)
L3	3 Turns, #14 AWG, 1/4" I.D., 1/4" Long (45 nH)
L4	10 µH RFC
L5	RF Choke Ferroxcube VK200-20-4B
R1	10 Ohms, Wirewound, 1 W (0.25 µH Inductance)

FIGURE 2 – LINEAR OUTPUT POWER versus FREQUENCY

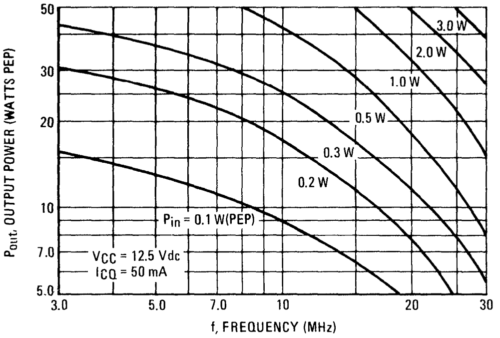


FIGURE 3 – OUTPUT POWER versus INPUT POWER

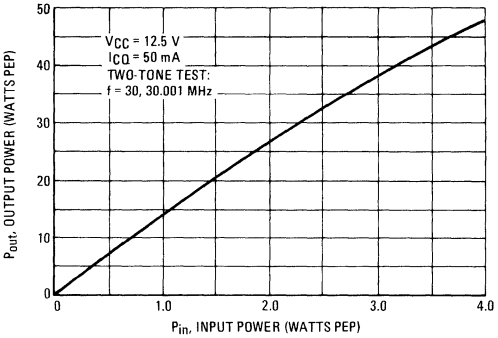


FIGURE 4 – OUTPUT POWER versus INPUT POWER

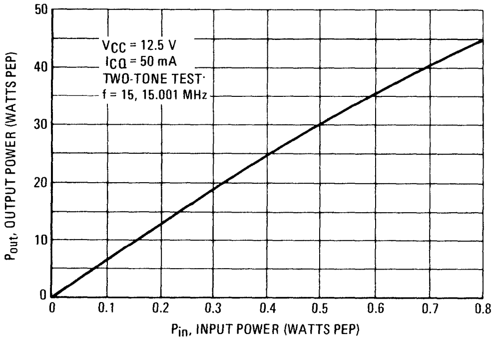


FIGURE 5 – OUTPUT POWER versus INPUT POWER

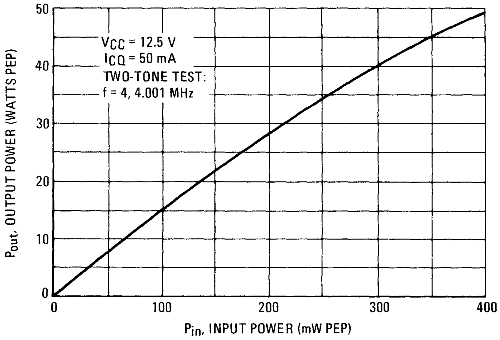


FIGURE 6 – INTERMODULATION DISTORTION versus OUTPUT POWER

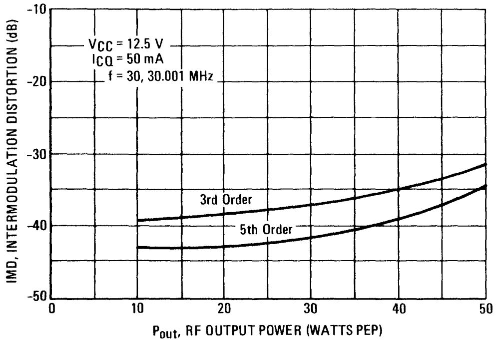


FIGURE 7 – LINEAR OUTPUT POWER versus SUPPLY VOLTAGE

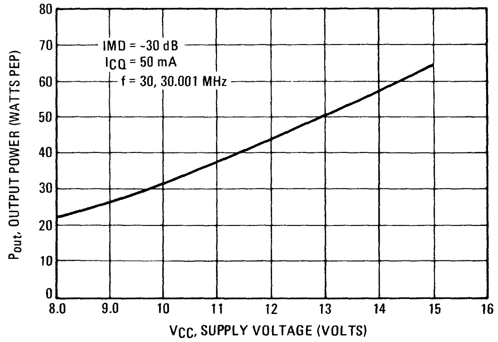


FIGURE 8 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

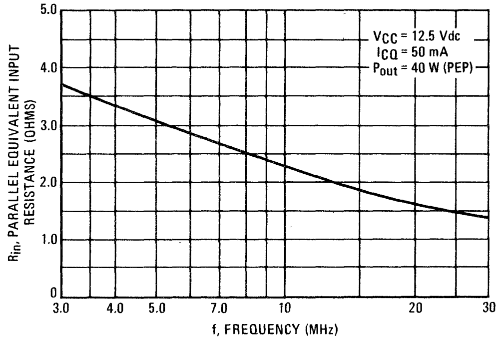


FIGURE 9 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

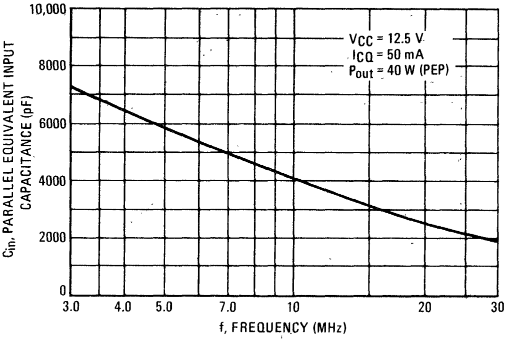


FIGURE 10 – PARALLEL EQUIVALENT OUTPUT RESISTANCE versus FREQUENCY

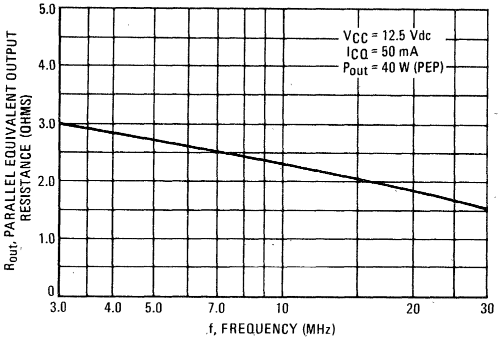


FIGURE 11 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

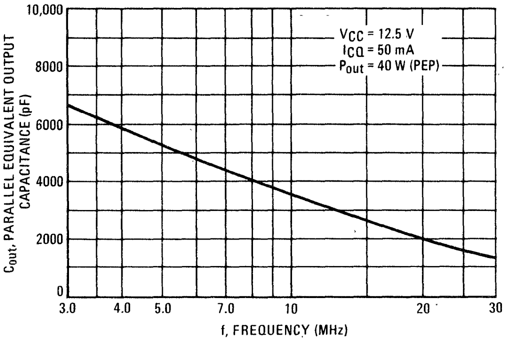


FIGURE 12 – CURRENT-GAIN – BANDWIDTH PRODUCT

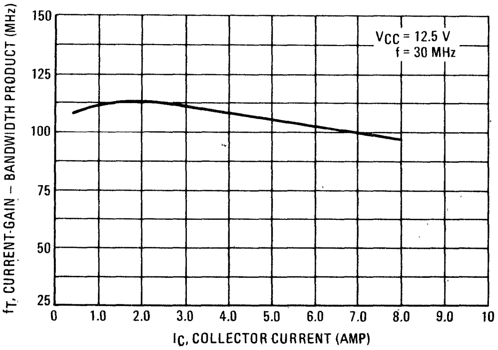


FIGURE 13 – COLLECTOR CURRENT versus BASE-EMITTER VOLTAGE

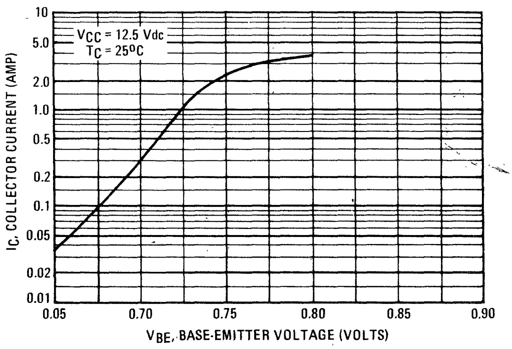


FIGURE 14 – OUTPUT CAPACITANCE versus VOLTAGE

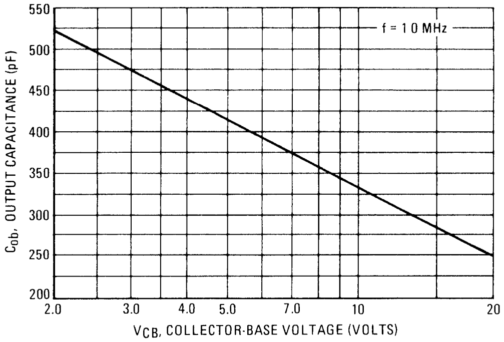


FIGURE 15 – INPUT CAPACITANCE versus VOLTAGE

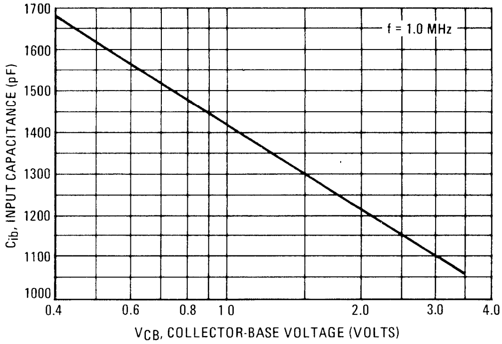


FIGURE 16 – DC SAFE OPERATING AREA

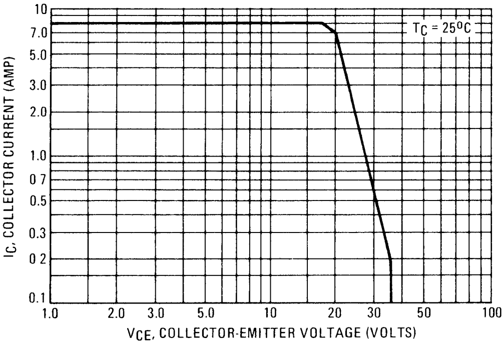
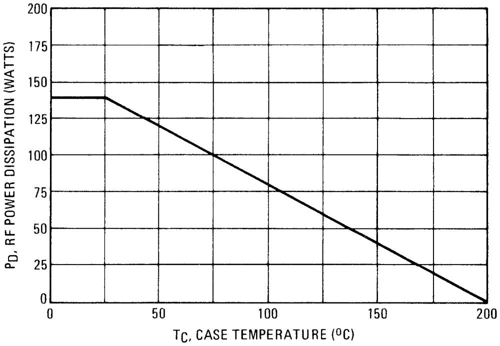


FIGURE 17 – RF POWER DISSIPATION



APPLICATIONS INFORMATION

The 2N6368 transistor is designed for linear power amplifier operation in the HF region (2 to 30 MHz). It features guaranteed linear amplifier performance rather than the conventional performance demonstrated in a class C* amplifier.

Class C operation is inherently non-linear, but in many power amplifier applications non-linear operation does not present major problems. With a single frequency driving signal, the only spurious signals generated are harmonics and these can be supressed in the amplifier tuned networks and output filter.

For single sideband (SSB), low level amplitude modulation (AM), and other types of complex signals, class C operation is generally not satisfactory. For instance, when a signal contains multiple frequencies at close spacings, odd-order non-linearities will generate spurious outputs which are within the passband of the tuned circuits and filters; therefore, the spurious outputs are not suppressed before they reach the antenna or other load. As a result, such complex signals require linear amplification if the amplified signal is to be free of spurious outputs.

A detailed analysis of spurious signals generated by non-linearities and linearity requirements of various applications is described in Chapter 12 of Reference 1.

The following discussion concerns itself with a detailed description of the 2N6368 characterization curves and general information on solid-state linear power amplifier design.

The Two-Tone Test

The 2N6368 functional test specifications consists of a linear power amplifier test with guaranteed limits on power output, gain, efficiency, and intermodulation distortion (IMD) output levels. A two-tone test signal is used with the test amplifier as shown in Figure 1.

The two-tone test is one of many methods commonly used for testing linear amplifier performance. This test involves driving the amplifier with two RF signals, of equal amplitude, separated in frequency from each other by approximately 1 kHz.

---

*"Class C", as used here refers to operation with the no signal conditions I_C = 0, and V_{BE} = 0, and a theoretical conduction angle of less than 180°, even though the actual conduction angle may be more than 180°.

APPLICATIONS INFORMATION (continued)

When a two-tone test signal consisting of frequencies f_1 and f_2 is passed through a non-linear amplifier, odd order non-linearities generate spurious signals near the desired carrier. The level of these spurious signals provides a measure of the degree of non-linearity of the amplifier. This type of non-linearity is called intermodulation distortion (IMD). The spurious signals generated by IMD are further classified according to the exponential order of the amplifier non-linearity, i.e., 3rd order IMD products, 5th order IMD products, etc. The 3rd and 5th order IMD products are usually the most significant encountered with linear power amplifiers. Data on both 3rd and 5th order IMD are included in the 2N6368 characterization.

Third order IMD generates spurious signals near the operating frequency at frequencies $2f_1 - f_2$ and $2f_2 - f_1$; and 5th order IMD spurious are at frequencies $3f_1 - 2f_2$ and $3f_2 - 2f_1$.

Specifications and Characterization

The two-tone functional amplifier test is performed in a manner identical to the conventional class C functional test with two exceptions: a two-frequency signal is used in place of a single frequency, and amplifier linearity is added to the items tested and specified.

The functional test procedure for the 2N6368 require driving the test amplifier with a two-frequency signal and measuring power output, gain, efficiency, and linearity.

Power output, gain and efficiency measurement methods are the same for both linear and class C amplifier.

Since a multiple frequency test signal has an instantaneous power level which varies with time, power levels are normally expressed in peak envelope power (PEP). This is the average power level of the envelope at its greatest amplitude point.

When the test signal consists of multiple signals with equal amplitudes and different frequencies, the relationship of average power and PEP is given by the following expression:

$$\text{Average power} = \frac{\text{PEP}}{N}$$

where N = the number of input frequencies.

Therefore, when measuring the power level of a standard two-tone test signal, a true average reading power meter will indicate 1/2 the PEP of the signal.

Linearity is tested by measuring the amplitudes of the 3rd and 5th order IMD products. The ratio of one of the 3rd order products to one of the two desired frequencies is then expressed as a power ratio in decibels (dB). This is repeated for the 5th order products. The smaller of these two ratios (usually the 3rd order) is then included in the electrical characteristics specifications as intermodulation distortion ratio (IMD).

2N6368 Performance Curves

Figures 2 through 5 show typical power output and gain characteristics versus frequency and/or input power. These curves are similar to those found on other RF power transistor data sheets with one exception, a two-frequency test signal was used rather than a single frequency signal.

The curves shown in Figure 6 are unique to transistors characterized for linear power amplifier service and show the typical IMD levels versus power output.

The 2N6368 features guaranteed IMD performance at the -30 dB level. However, the designer may desire IMD greater or less than -30 dB for a particular application. Figure 6 provides data on IMD levels that can be expected as a function of output power.

Figure 7 reflects the power output that can be obtained at a fixed IMD ratio for operation with dc supply voltages other than 12.5 Vdc.

Figures 8 through 11 show the large signal impedance characteristics of the 2N6368. These are similar to curves shown on other Motorola data sheets except a two-frequency test signal was used rather than a single frequency signal.

It must be stressed that the data shown in Figures 8 through 11 do not represent y, z, h, s, or any standard two-port parameter set. The actual transistor impedance levels during normal operation in a power amplifier are given. For a detailed discussion of RF power transistor large signal impedance, see Reference 2.

Linear Amplifier Design

The following is a discussion of some general design considerations for solid-state linear power amplifiers. While this is not a detailed analysis of linear amplifier design, some general guidelines are provided.

The major difference between linear power amplifiers and class C power amplifiers is in the dc bias circuitry. As stated in the introduction, class C operation usually involves a collector dc supply as the only bias voltage with $V_E = V_B = 0$. The collector current is zero until the input RF signal turns the transistor "on."

In contrast, a linear amplifier is normally operated with forward bias and some collector current flowing when no signal is present.

The magnitude of no-signal collector current and the bias circuitry may vary with the application. Optimum no-signal collector current for the 2N6368 was found to be approximately 50 mA.

The key to bias circuitry for good linearity lies in maintaining the base-emitter dc voltage relatively constant as the RF signal amplitude varies. The inherent nature of a forward-biased RF power transistor is to bias itself "off" with increasing RF drive signal. Therefore, a constant voltage source is required for base voltage.

Temperature effects also complicate the situation, since V_{BE} decreases with increasing temperature.

A simple solution to the bias problem involves the use of a forward-biased diode mounted on the transistor heat sink for thermal coupling to the transistor. A sample of this technique is shown in the test circuit of Figure 1. The reader is referred to reference 3 for a detailed description of the operation of this bias circuit. It is also possible to use complex active circuitry for biasing, and some rather exotic schemes have been developed to provide the same results.

Another important consideration is the collector-output network. Normally, a network with low impedance to ground for harmonics provides better linearity than a network with high harmonic impedances; therefore, some experimentation with network configuration is in order. Proper impedance matching remains the primary factor in both input and output network design. Further, it must also be stressed that the collector load impedance should be designed for the PEP, not the average power output. See Chapter 13 of Reference 1 for a detailed discussion of network design considerations.

Feedback may also be employed to improve linearity and may take the form of either neutralization or negative RF feedback. The possibilities here are limited only by the designer's imagination. Of course, negative RF feedback involves a decrease in gain to improve linearity.

REFERENCES

1. Pappenfus, Bruene, Schoenike, "Single Sideband Principles and Circuits", McGraw-Hill.
2. Hejhall, "Systemizing RF Power Amplifier Design", Motorola Semiconductor Products Inc., Application Note AN-282A.
3. Hejhall, "Solid-State Linear Power Amplifier Design," Motorola Semiconductor Products Inc., Application Note AN-546.

2N6370 (SILICON)

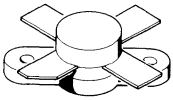
The RF Line

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily as a driver for high-power linear amplifier stages operating from 2.0 to 30 MHz with a 28-Volt supply.

- Power Output @ 28 Vdc, 30 MHz –
  10 W (PEP)
- Intermodulation Distortion at Rated Power Output –
  IMD = -30 dB (Max)

10 W (PEP) – 30 MHz
RF POWER
TRANSISTOR
NPN SILICON

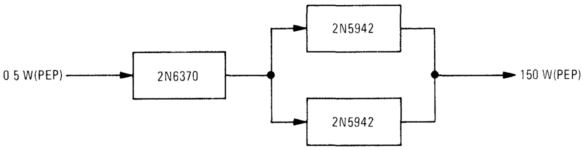


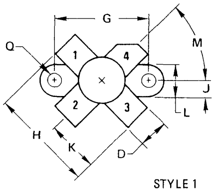
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	1.5	Adc
Total Device Dissipation @ $T_C = 25^{\circ}C$ Derate above 25°C	P_D	20 0.114	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

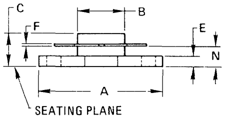
*Indicates JEDEC Registered Data

TYPICAL DRIVER APPLICATION





STYLE 1
PIN 1. EMITTER
2. BASE
3. EMITTER
4 COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.64	24.89	0.970	0.980
B	9.47	9.73	0.373	0.383
C	6.07	7.14	0.239	0.281
D	5.59	5 84	0.220	0.230
E	2.16	2.67	0.085	0.105
F	0 10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	21.59	22.10	0.850	0.870
J	3.12	3.23	0.123	0.127
K	10.80	11.05	0.425	0.435
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.97	3.12	0.117	0.123

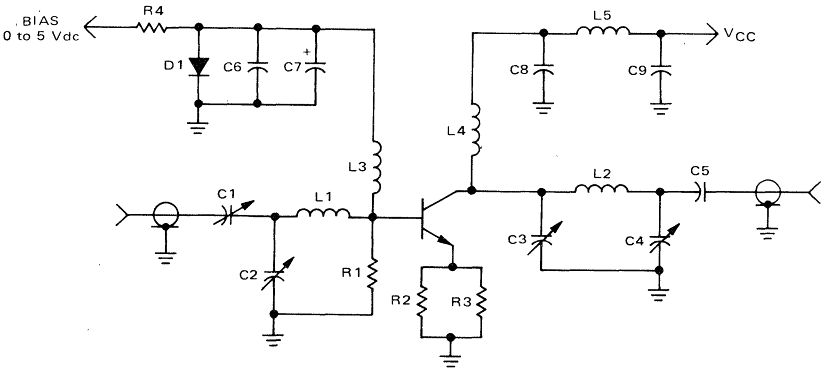
CASE 211-01

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	BV_{CEO}	35	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	BV_{CES}	65	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0, T_C = +55°C)	I_{CES}	–	10	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	50	–
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 15 Vdc, f = 50 MHz)	f_T	50	–	MHz
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	40	pF
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 10 W(PEP), I_C = 470 mAdc Max, V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	G_{PE}	12	–	dB
Intermodulation Distortion Ratio (Figure 1) (P_{out} = 10 W(PEP), I_C = 470 mAdc Max, V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	IMD	–	-30	dB
Collector Efficiency (P_{out} = 10 W(PEP), I_C = 470 mAdc Max, V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	η	38	–	%

*Indicates JEDEC Registered Data.

FIGURE 1 – 30 MHz TEST CIRCUIT



C1	80 – 480 pF	ARCO 466 or equivalent	L2	5 Turns, #18 AWG, 1/4" I.D., 5/16" Long (0.13 μH)
C2,C3,C4	170 – 780 pF	ARCO 469 or equivalent	L3	10 μH
C5	0.1 μF		L4	1.0 μH
C6,C9	0.01 μF		L5	RFC VK200 FERROXCUBE
C7	500 μF	TANTALUM or equivalent	R1	10 OHMS 1/2 W ALLEN BRADLEY or equivalent
C8	2000 pF	UNELCO or equivalent	R2,R3	1.5 OHMS 1/2 W ALLEN BRADLEY or equivalent
D1	1N4001		R4	50 OHMS 1/2 W ALLEN BRADLEY or equivalent
L1	4 Turns, #18 AWG, 1/2" I.D., 1/4" Long (0.1 μH)			

ADJUST BIAS FOR I_{CQ} = 10 mA

FIGURE 2 – LINEAR OUTPUT POWER
versus FREQUENCY

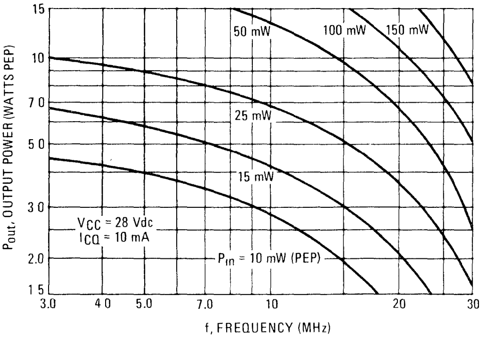


FIGURE 3 – OUTPUT POWER
versus INPUT POWER

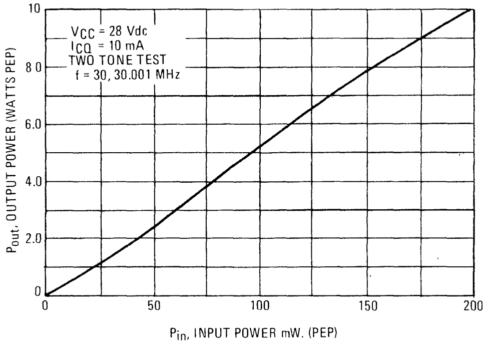


FIGURE 4 – OUTPUT POWER
versus INPUT POWER

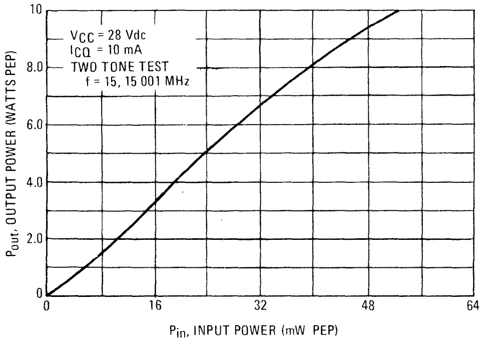


FIGURE 5 – OUTPUT POWER
versus INPUT POWER

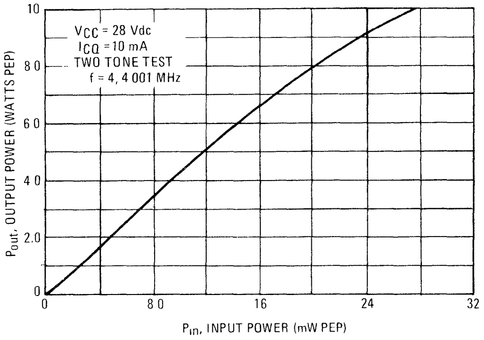


FIGURE 6 – INTERMODULATION DISTORTION
versus OUTPUT POWER

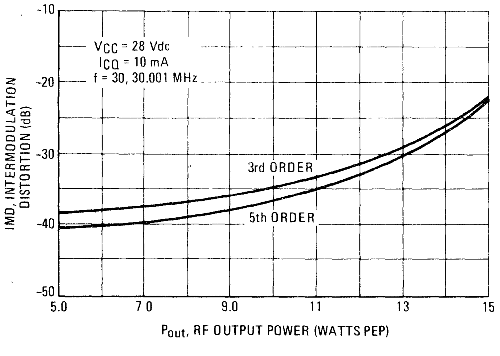


FIGURE 7 – LINEAR OUTPUT POWER
versus SUPPLY VOLTAGE

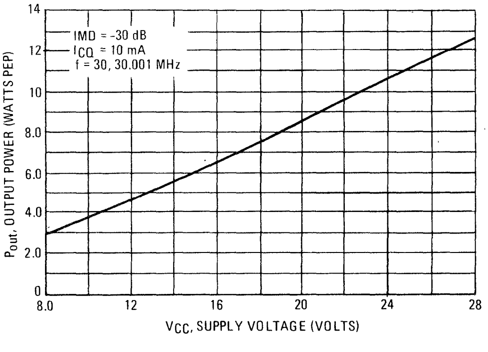


FIGURE 8 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

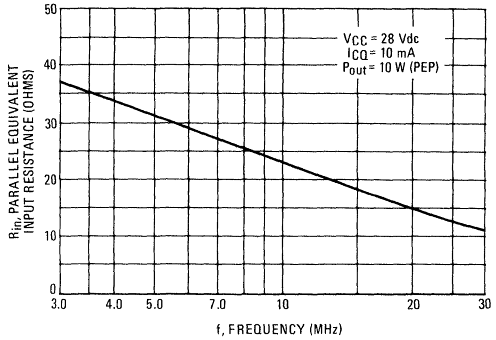


FIGURE 9 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

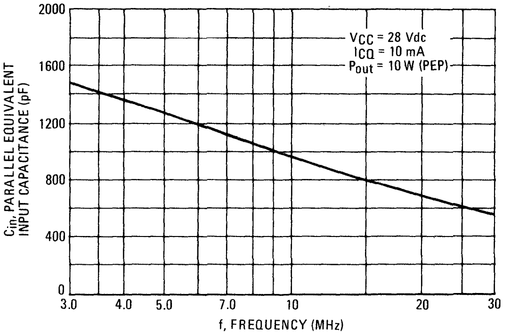


FIGURE 10 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

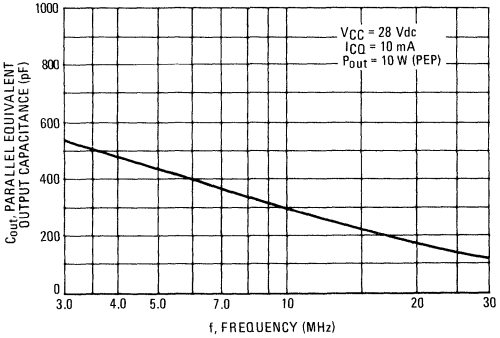


FIGURE 11 – CURRENT GAIN – BANDWIDTH PRODUCT

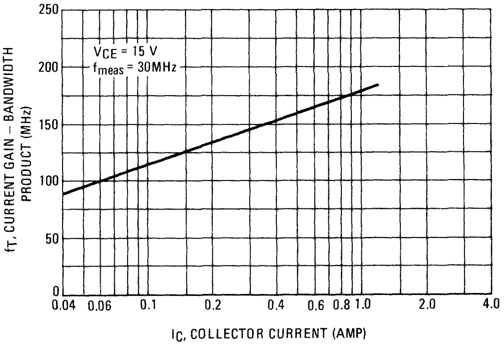


FIGURE 12 – INPUT CAPACITANCE versus EMITTER-BASE VOLTAGE

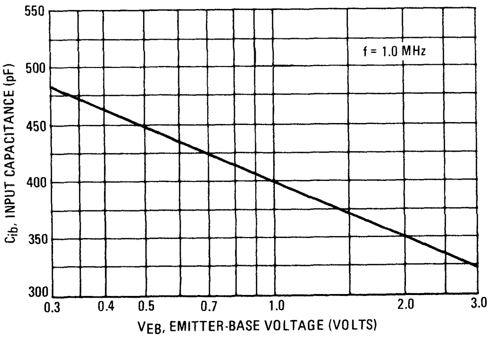


FIGURE 13 – OUTPUT CAPACITANCE versus COLLECTOR-BASE VOLTAGE

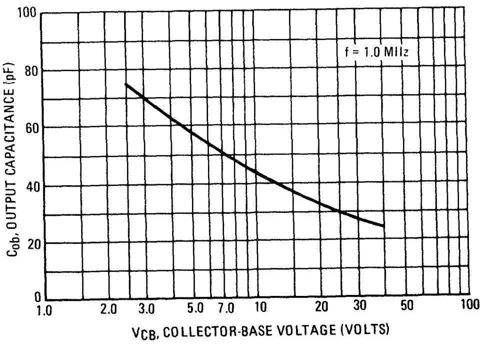


FIGURE 14 – COLLECTOR CURRENT versus BASE-EMITTER VOLTAGE

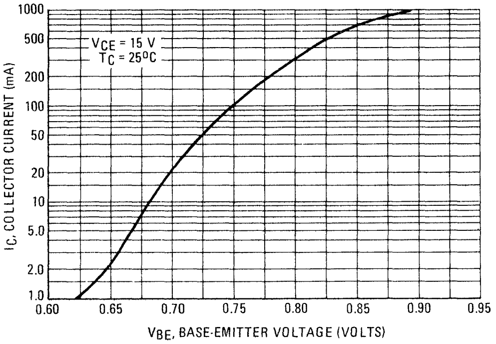


FIGURE 15 – RF POWER DERATING

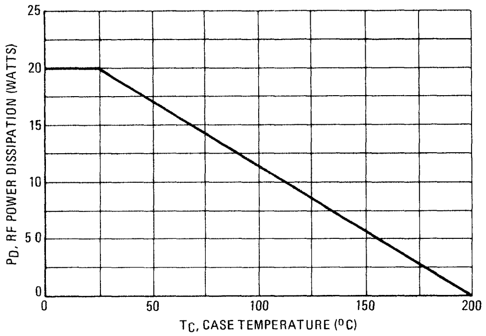
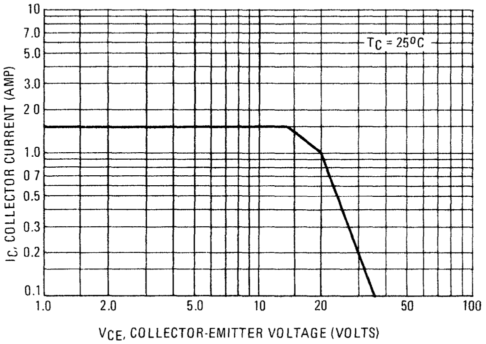


FIGURE 16 – DC SAFE OPERATING AREA



APPLICATIONS INFORMATION

The 2N6370 transistor is designed for linear power amplifier service in the driver or lower level stages of HF (2-30 MHz) single sideband (SSB) transmitters. It may also be used in amplitude modulated (AM) transmitters employing low level modulation in the exciter, or in any application requiring a linear amplifier. The device also has adequate gain for many VHF applications below 100 MHz.

Designed primarily for lower level stages and not the output stage of SSB transmitters, the 2N6370 does not employ internal emitter resistors. Therefore, for linear power amplifier applications which normally require forward bias for improved linearity, it is suggested that external emitter resistance be employed for improved DC operating point stability over the full temperature range. Typical resistor values for HF operation are illustrated in the test amplifier shown in Figure 1. The 2N6370 has more than adequate gain at HF, so the designer may wish to utilize unbypassed emitter resistance as shown in the circuit of Figure 1. Of course, bypassing may be included if more gain is desired.

The linear amplifier characterization data in Figures 2 through 10 were measured with the unbypassed emitter resistor configuration shown in Figure 1. For a more detailed discussion of linear power amplifier specifications and design, see Reference 1.

REFERENCES

1. "Solid-State Linear Power Amplifier Design", Motorola Semiconductor Products, Inc. Application Note AN-546
2. Pappenfus, Bruene, and Schoenike, "Single Sideband Principles and Circuits", McGraw – Hill.

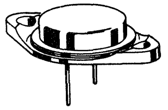
2N6377 thru 2N6379 (SILICON)

HIGH-POWER PNP SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage –
  $V_{CEO\ (sus)}$ = 80 Vdc (Min) – 2N6377
  = 100 Vdc (Min) – 2N6378
  = 120 Vdc (Min) – 2N6379
- High DC Current Gain –
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max)
  t_f = 0.25 μs (Max)

50 AMPERE
POWER TRANSISTORS
PNP SILICON
80, 100, 120 VOLTS
250 WATTS



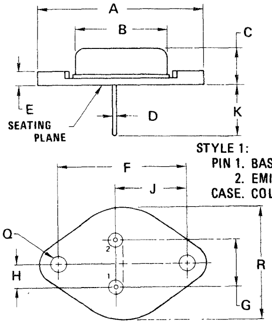
* MAXIMUM RATINGS

Rating	Symbol	2N6377	2N6378	2N6379	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 50 → ← 100 →			Adc
Base Current	I_B	← 20 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 250 → ← 1.43 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

*Indicates JEDEC Registered Data.

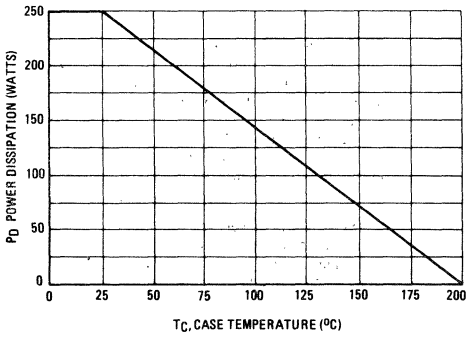


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

FIGURE 1 – POWER DERATING



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

*OFF CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N6380	$V_{CEO(sus)}$	80	–	Vdc
	2N6381		100	–	
	2N6382		120	–	
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	2N6380	I_{CEO}	–	50	µAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N6381		–	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6382		–	50	
Collector Cutoff Current (V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEX}	–	10	µAdc
(V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	µAdc

*ON CHARACTERISTICS (1)

Characteristic	Symbol	Min	Max	Unit
DC Current Gain	h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		50	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)		30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	–		Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)		–	1.2	
(I_C = 50 Adc, I_B = 10 Adc)		–	3.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)		–	1.8	
(I_C = 50 Adc, I_B = 10 Adc)		–	3.5	

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
*Current-Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	–	MHz
Input Capacitance (V_{EB} = 2.0 Vdc, I_C = 0, f = 0.1 MHz)	C_{ib}	–	7000	pF
*Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	1500	pF

*SWITCHING CHARACTERISTICS (Figure 2)

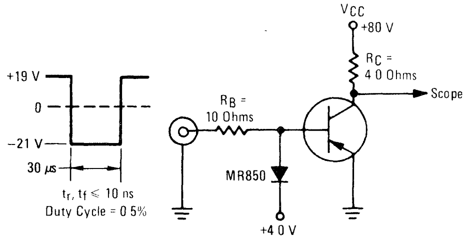
Characteristic	Conditions	Symbol	Min	Max	Unit
Rise Time	(V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)	t_r	–	0.35	µs
Storage Time		t_s	–	0.80	µs
Fall Time		t_f	–	0.25	µs

*Indicates JEDEC Registered Data.

(1) Pulse Test. Pulse Width = 300 µs, Duty Cycle = 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



Note For information on Figures 3 & 6, R_B and R_C were varied to obtain desired test conditions

FIGURE 3 – TURN ON TIME

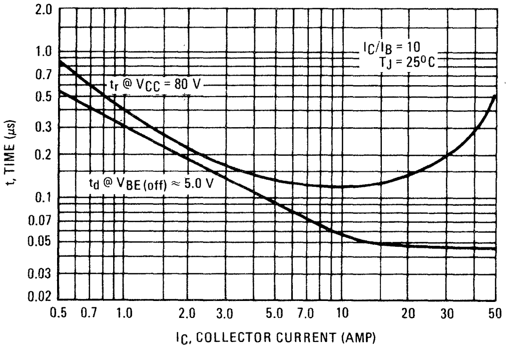


FIGURE 4 – THERMAL RESPONSE

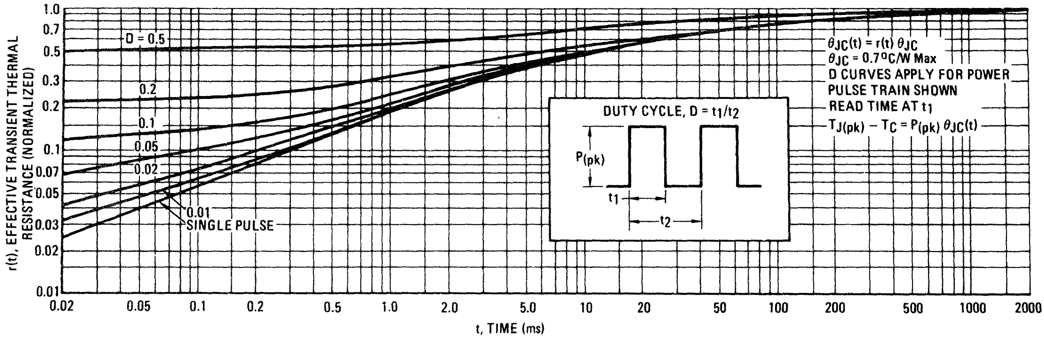
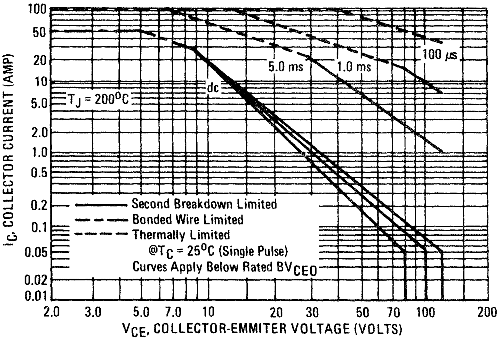


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

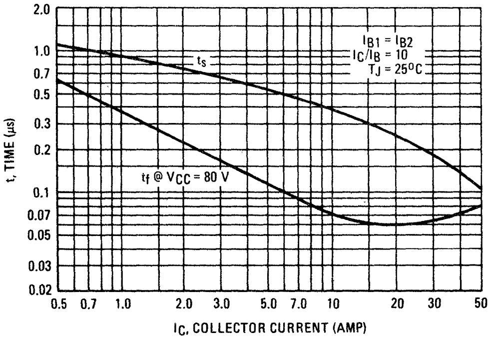


FIGURE 7 – CAPACITANCE

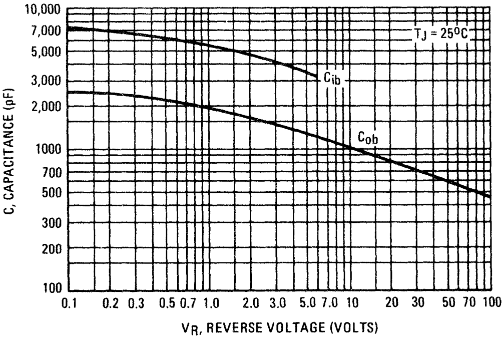


FIGURE 8 – DC CURRENT GAIN

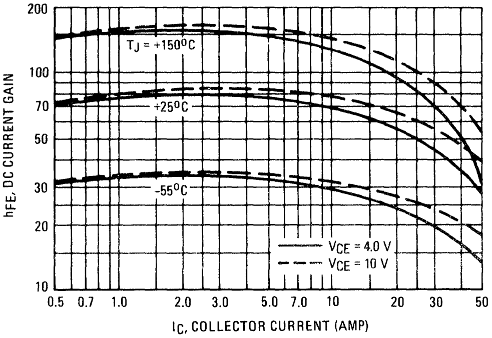


FIGURE 9 – COLLECTOR SATURATION REGION

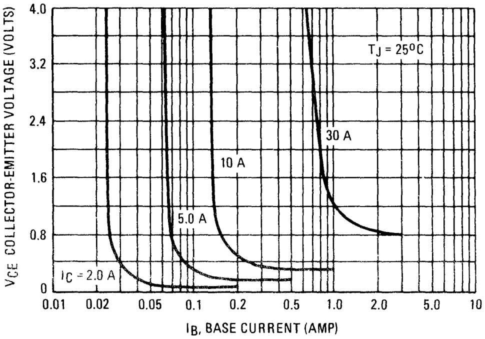


FIGURE 10 – "ON" VOLTAGES

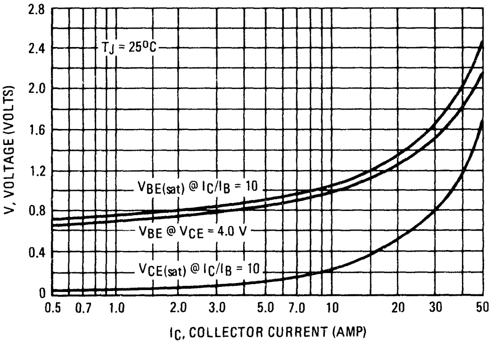


FIGURE 11 – TEMPERATURE COEFFICIENTS

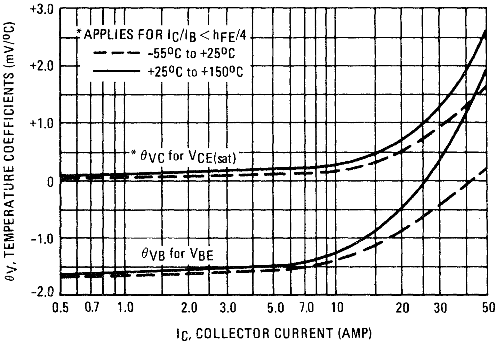


FIGURE 12 – COLLECTOR CUT-OFF REGION

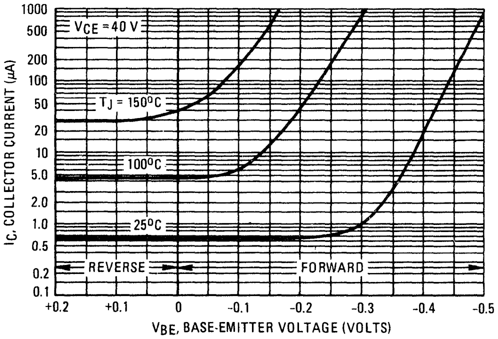
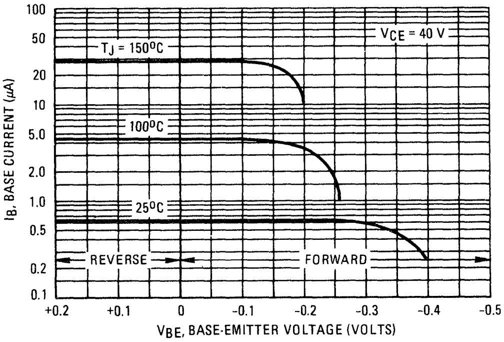


FIGURE 13 – BASE CUTOFF REGION



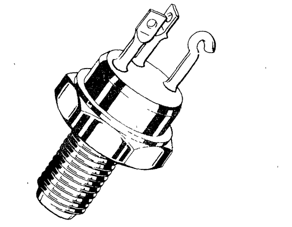
2N6380 thru 2N6382 (SILICON)

HIGH-POWER PNP SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage –
  $V_{CEO\ (sus)}$ = 80 Vdc (Min) – 2N6380
  = 100 Vdc (Min) – 2N6381
  = 120 Vdc (Min) – 2N6382
- High DC Current Gain –
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max)
  t_f = 0.25 μs (Max)

50 AMPERE
POWER TRANSISTORS
PNP SILICON
80, 100, 120 VOLTS
250 WATTS



*MAXIMUM RATINGS

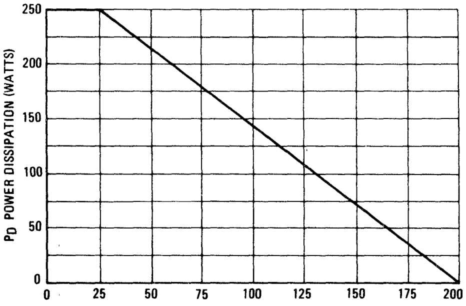
Rating	Symbol	2N6380	2N6381	2N6382	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 50 → ← 100 →			Adc
Base Current	I_B	← 20 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 250 → ← 1.43 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

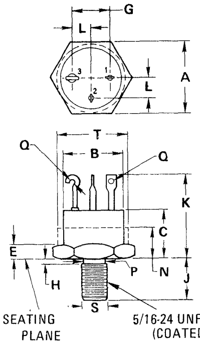
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.70	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.72	22.23	0.855	0.875
B	18.92	19.69	0.745	0.775
C	12.19	13.59	0.480	0.535
E	2.29	4.24	0.090	0.167
G	12.32	13.08	0.485	0.515
H	–	2.67	–	0.105
J	11.68	12.57	0.460	0.495
K	23.80	26.16	0.937	1.030
L	6.10	6.60	0.240	0.260
N	–	7.62	–	0.300
P	7.06	7.92	0.278	0.312
Q	1.52	2.67	0.060	0.105
S	7.127	7.249	0.2806	0.2854
T	19.69	22.23	0.775	0.875

All JEDEC notes and dimensions apply.

CASE 188
TO-63

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

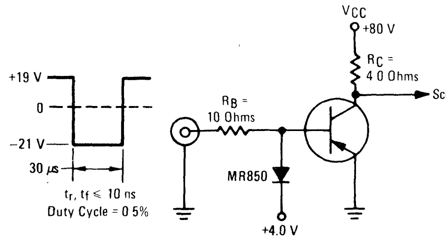
Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1)	$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0) 2N6380		80	–	
2N6381		100	–	
2N6382		120	–	
Collector Cutoff Current	I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0) 2N6380		–	50	
(V_{CE} = 60 Vdc, I_B = 0) 2N6381		–	50	
(V_{CE} = 70 Vdc, I_B = 0) 2N6382		–	50	
Collector Cutoff Current	I_{CEX}			
(V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)		–	10	μAdc
(V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
***ON CHARACTERISTICS** (1)				
DC Current Gain	h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		50	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)		30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	–		Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)		–	1.2	
(I_C = 50 Adc, I_B = 10 Adc)		–	3.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)		–	1.8	
(I_C = 50 Adc, I_B = 10 Adc)		–	3.5	
DYNAMIC CHARACTERISTICS				
*Current-Gain – Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	–	MHz
Input Capacitance (V_{EB} = 2.0 Vdc, I_C = 0, f = 0.1 MHz)	C_{ib}	–	7000	pF
*Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	1500	pF
***SWITCHING CHARACTERISTICS** (Figure 2)				
Rise Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)	t_r	–	0.35	μs
Storage Time	t_s	–	0.80	μs
Fall Time	t_f	–	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



Note: For information on Figures 3 & 6, R_B and R_C were varied to obtain desired test conditions

FIGURE 3 – TURN ON TIME

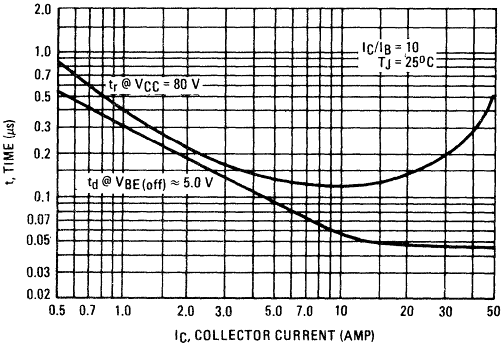


FIGURE 4 – THERMAL RESPONSE

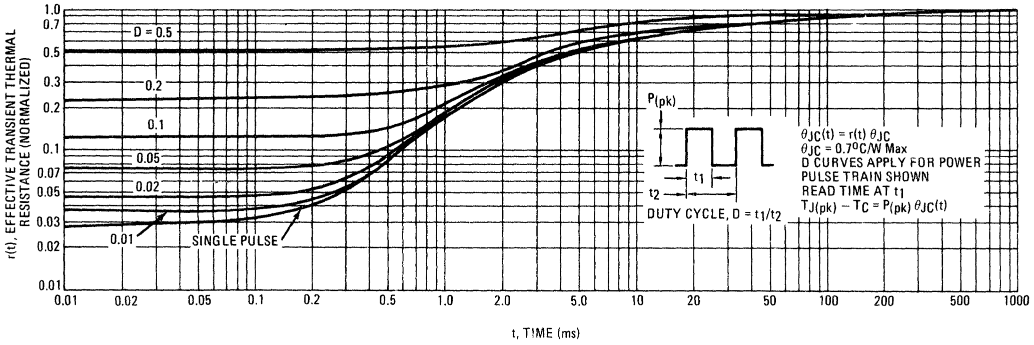
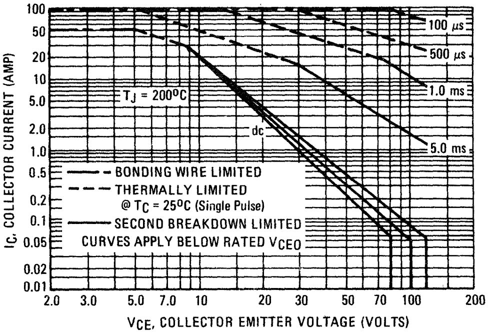


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

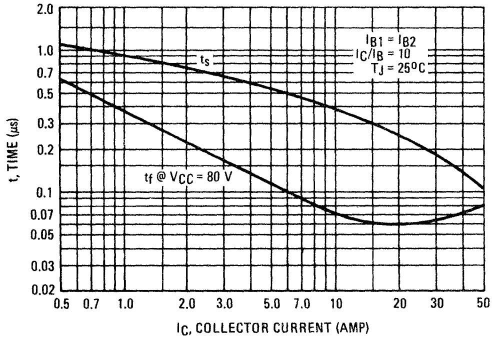


FIGURE 7 – CAPACITANCE

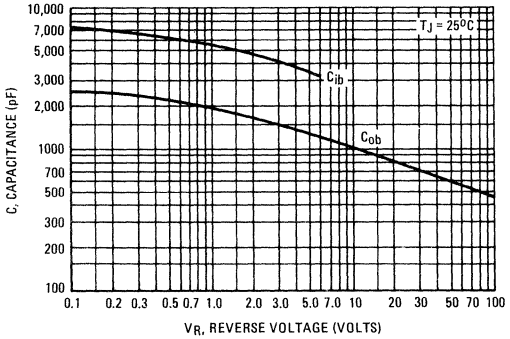


FIGURE 8 – DC CURRENT GAIN

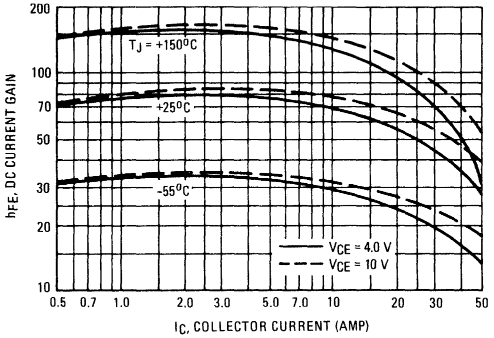


FIGURE 9 – COLLECTOR SATURATION REGION

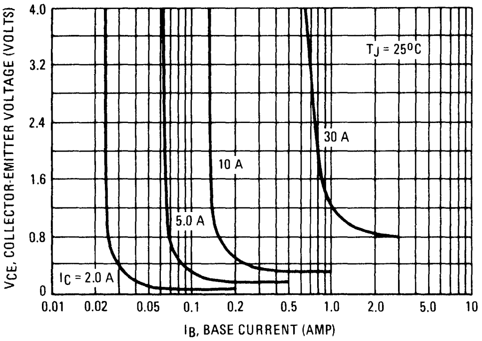


FIGURE 10 – "ON" VOLTAGES

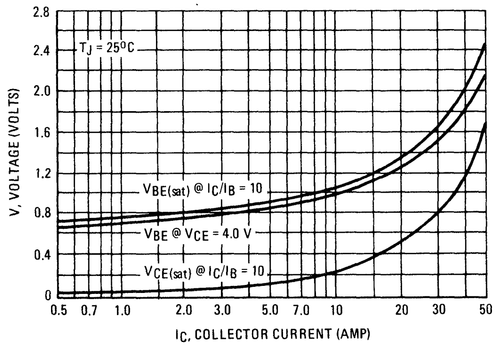


FIGURE 11 – TEMPERATURE COEFFICIENTS

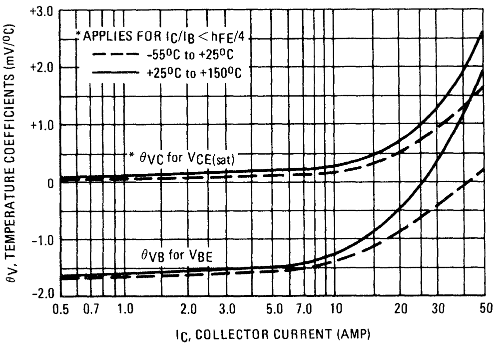


FIGURE 12 – COLLECTOR CUT-OFF REGION

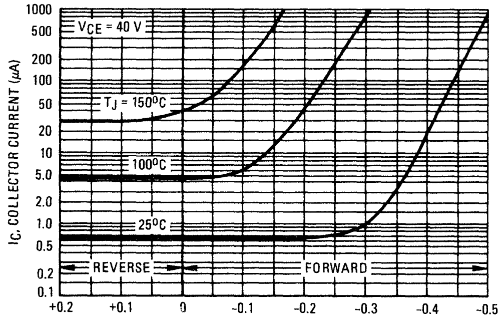
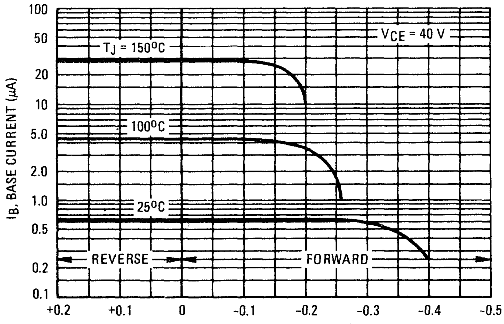
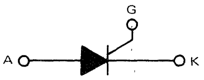


FIGURE 13 – BASE CUT-OFF REGION



2N6394 thru 2N6399 (SILICON)



SILICON CONTROLLED RECTIFIERS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1) 2N6394 2N6395 2N6396 2N6397 2N6398 2N6399	V_{RRM}	 50 100 200 400 600 800	Volts
Forward Current RMS $T_J = 125^{\circ}C$ (All Conduction Angles)	$I_{T(RMS)}$	12	Amps
Peak Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, $T_J = 125^{\circ}C$)	I_{TSM}	100	Amps
Circuit Fusing Considerations ($T_J = -40$ to $+125^{\circ}C$, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

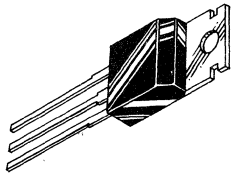
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

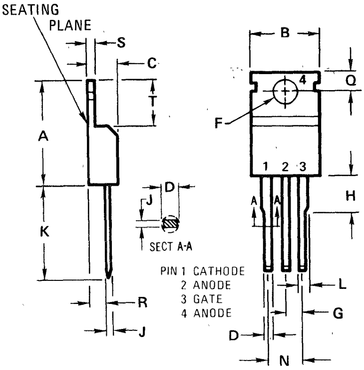
(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

* Indicates JEDEC Registered Data.

THYRISTORS

12 AMPERES RMS
50-800 VOLTS





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB

All JEDEC dimensions and notes apply

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
* Peak Forward Blocking Voltage (T_J = 125°C)	2N6394	V_{DRM}	50	–	–	Volts
	2N6395		100	–	–	
	2N6396		200	–	–	
	2N6397		400	–	–	
	2N6398		600	–	–	
	2N6399		800	–	–	
* Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)		I_{DRM}	–	–	2.0	mA
* Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)		I_{RRM}	–	–	2.0	mA
* Forward "On" Voltage (I_{TM} = 24 A Peak)		V_{TM}	–	1.7	2.2	Volts
* Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		I_{GT}	–	5.0	30	mA
* Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		V_{GT}	–	0.7	1.5	Volts
* Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2	–	–	Volts
* Holding Current (Anode Voltage = 12 Vdc)		I_H	–	6.0	40	mA
Turn-On Time (I_{TM} = 12 A, I_{GT} = 40 mAdc)		t_{gt}	–	1.0	2.0	μs
Turn-Off Time (V_{DRM} = rated voltage)		tq				μs
(I_{TM} = 12 A, I_R = 12 A)			–	15	–	
(I_{TM} = 12 A, I_R = 12 A, T_J = 125°C)			–	35	–	
Forward Voltage Application Rate (T_J = 125°C)		dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

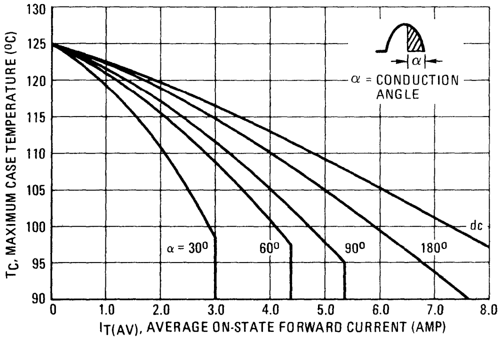


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

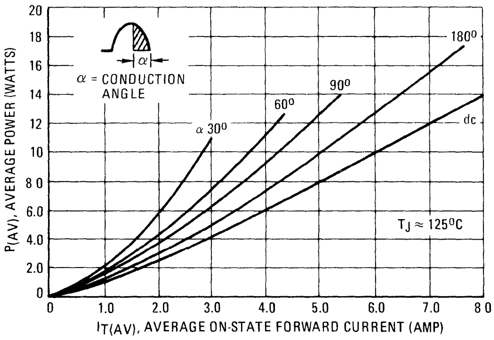


FIGURE 3 – MAXIMUM ON-STATE CHARACTERISTICS

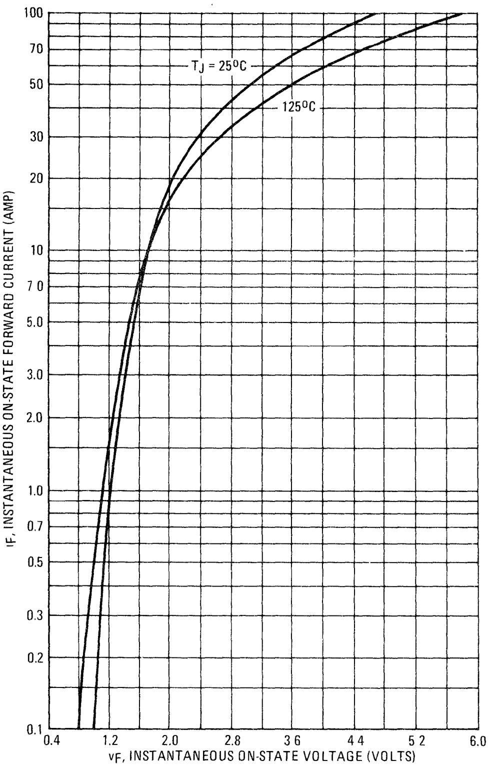


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

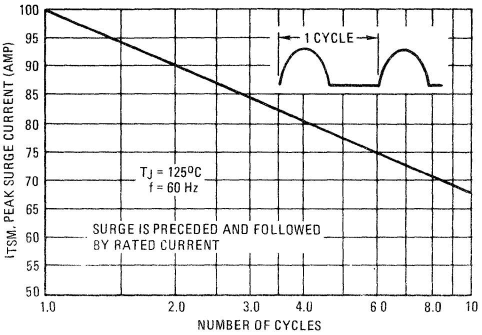


FIGURE 5 – CHARACTERISTICS AND SYMBOLS

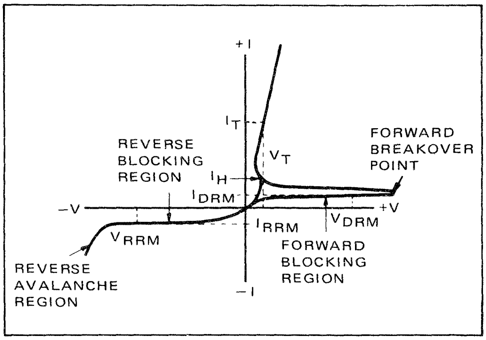
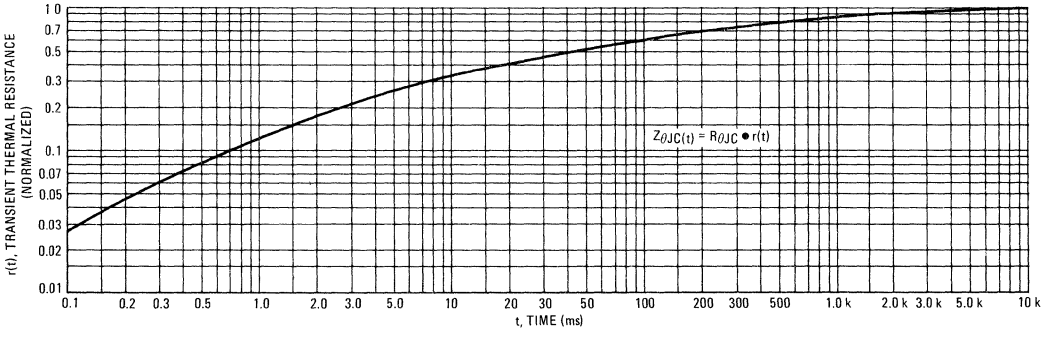


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 7 – PULSE TRIGGER CURRENT

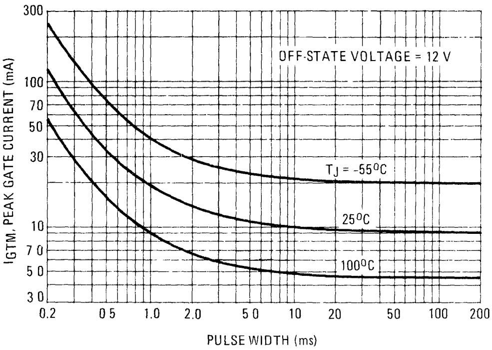


FIGURE 8 – GATE TRIGGER CURRENT

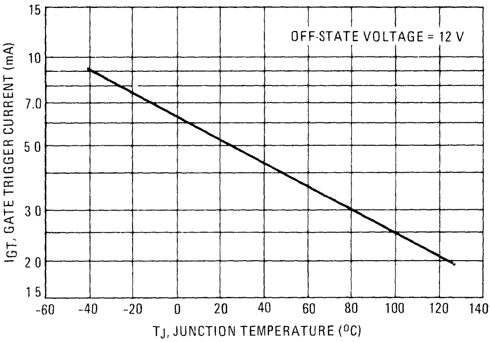


FIGURE 9 – GATE TRIGGER VOLTAGE

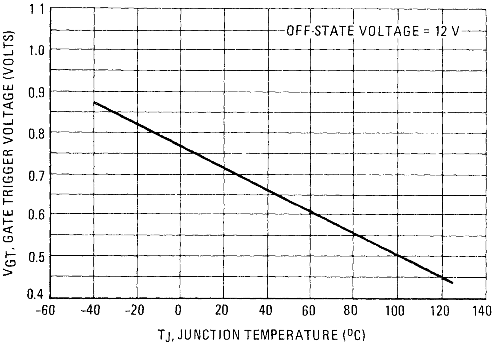
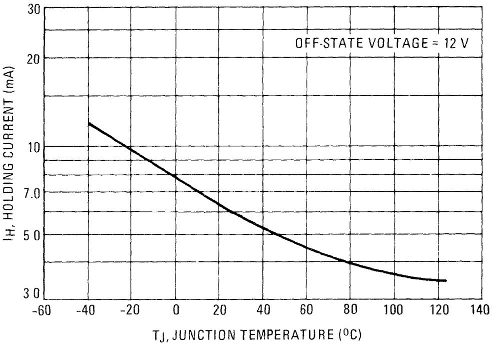


FIGURE 10 – HOLDING CURRENT



THYRISTER APPLICATION NOTES

AN-140	Characterization of SCR's as Switches for Line Type Modulators
AN-189	Solid-State Pulse Width Modulation DC Motor Control
AN-240	SCR Power Control Fundamentals
AN-295	Suppressing RFI in Thyristor Circuits
AN-413	Unijunction Trigger Circuits for Gated Thyristors
AN-441	SCR Slaving Circuits
AN-443	Directional and Speed Control for Series, Universal and Shunt Motors
AN-450	Induction Motor Speed Control
AN-453	Zero Point Switching Techniques
AN-482	Electronic Speed Control of Appliance Motors
AN-526	Theory, Characteristics and Applications of Silicon Unilateral and Bilateral Switches
AN-527	Theory, Characteristics and Applications of the Programmable Unijunction Transistor
AN-568	A Fuse-Thyristor Coordinator Primer

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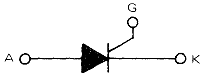
Technical Information Center
Motorola Semiconductor Products, Inc.
P.O Box 20924
Phoenix, Arizona 85036

2N6400 thru 2N6405 (SILICON)

THYRISTORS

16 AMPERES RMS
50-800 VOLTS



SILICON CONTROLLED RECTIFIERS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies, or where-ever half-wave silicon gate-controlled, solid-state devices are needed.

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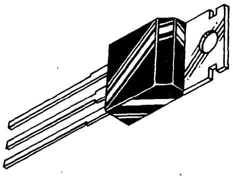
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts

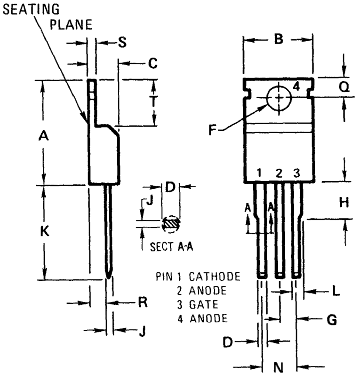


*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1)	V_{RRM}		Volts
2N6400		50	
2N6401		100	
2N6402		200	
2N6403		400	
2N6404		600	
2N6405		800	
Forward Current RMS ($T_C = 90^oC$) (All Conduction Angles)	$I_{T(RMS)}$	16	Amps
Peak Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, $T_J = 125^oC$)	I_{TSM}	160	Amps
Circuit Fusing Considerations (T_J = -40 to +125°C, t = 1.0 to 8.3 ms)	I^2t	100	A^2s
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB

All JEDEC dimensions and notes apply

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

*Indicates JEDEC Registered Data

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (T_J = 125°C)	2N6400 2N6401 2N6402 2N6403 2N6404 2N6405	V_{DRM}	50 100 200 400 600 800	– – – – – –	– – – – – –	Volts
*Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)		I_{DRM}	–	–	2.0	mA
*Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)		I_{RRM}	–	–	2.0	mA
*Forward "On" Voltage (I_{TM} = 32 A peak)		V_{TM}	–	–	1.7	Volts
*Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		I_{GT}	–	5.0	30	mA
*Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		V_{GT}	–	0.7	1.5	Volts
*Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2	–	–	Volts
*Holding Current (Anode Voltage = 12 Vdc)		I_H	–	6.0	40	mA
Turn-On Time (I_{TM} = 16 A, I_{GT} = 40 mAdc)		t_{gt}	–	1.0	–	μs
Turn-Off Time (V_{DRM} = rated voltage) (I_{TM} = 16 A, I_R = 16 A) (I_{TM} = 16 A, I_R = 16 A, T_J = 125°C)		t_q	 – –	 15 35	 – –	μs
Forward Voltage Application Rate (T_J = 125°C)		dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

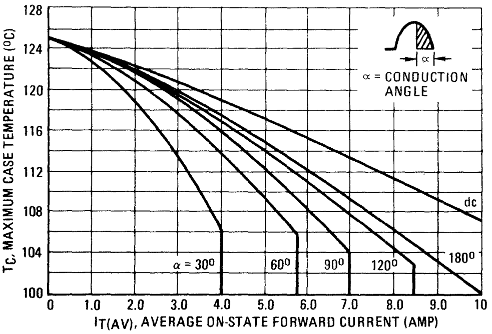


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

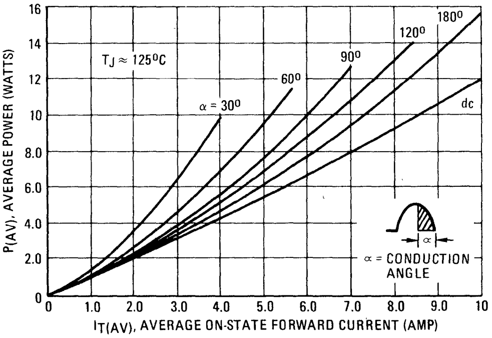


FIGURE 3 – MAXIMUM ON-STATE CHARACTERISTICS

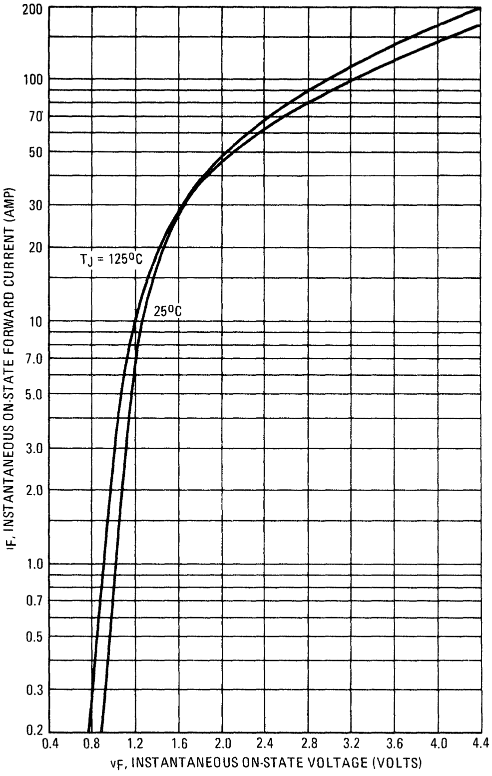


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

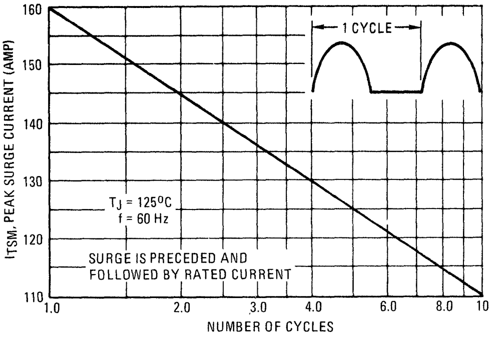


FIGURE 5 – CHARACTERISTICS AND SYMBOLS

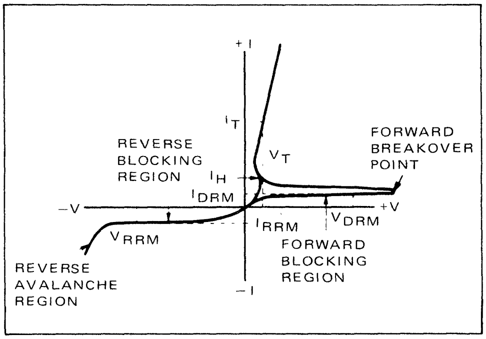
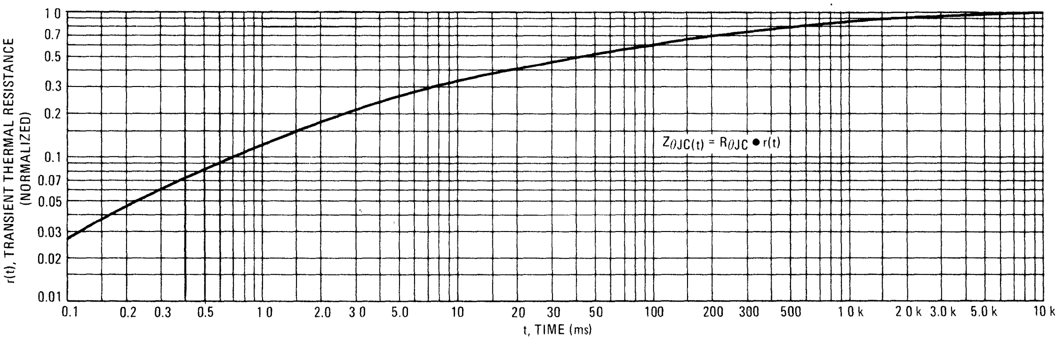


FIGURE 6 – THERMAL RESPONSE



TYPICAL TRIGGER CHARACTERISTICS

FIGURE 7 — GATE TRIGGER CURRENT

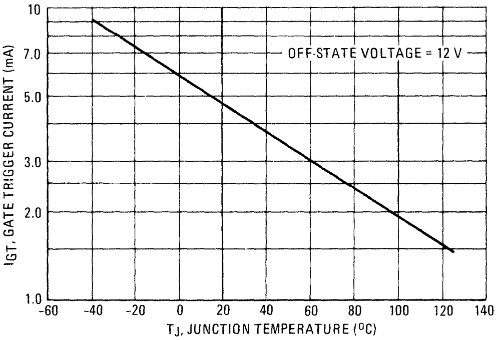


FIGURE 8 — GATE TRIGGER VOLTAGE

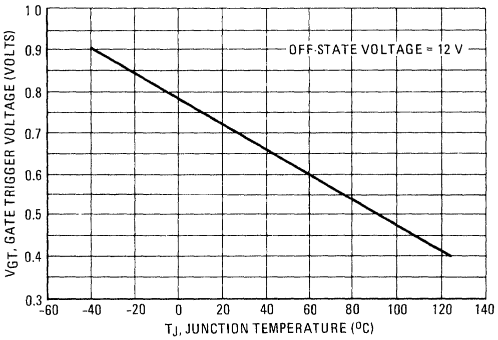
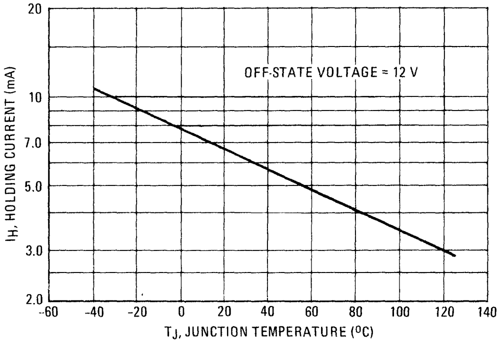


FIGURE 9 — HOLDING CURRENT



THYRISTER APPLICATION NOTES

AN-140	Characterization of SCR's as Switches for Line Type Modulators
AN-189	Solid-State Pulse Width Modulation DC Motor Control
AN-240	SCR Power Control Fundamentals
AN-295	Suppressing RFI in Thyristor Circuits
AN-413	Unijunction Trigger Circuits for Gated Thyristors
AN-441	SCR Slaving Circuits
AN-443	Directional and Speed Control for Series, Universal and Shunt Motors
AN-450	Induction Motor Speed Control
AN-453	Zero Point Switching Techniques
AN-482	Electronic Speed Control of Appliance Motors
AN-526	Theory, Characteristics and Applications of Silicon Unilateral and Bilateral Switches
AN-527	Theory, Characteristics and Applications of the Programmable Unijunction Transistor
AN-568	A Fuse-Thyristor Coordinator Primer

To obtain copies of these notes list the AN number(s) on your company letterhead and send your request to.

Technical Information Center
Motorola Semiconductor Products, Inc.
P.O Box 20924
Phoenix, Arizona 85036

2N6406, 2N6407 PNP (SILICON)
2N6408, 2N6409 NPN

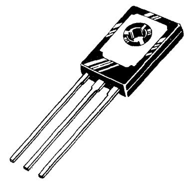
COMPLEMENTARY PLASTIC SILICON ANNULAR POWER TRANSISTORS

. . . designed for low power audio amplifier and low current, high speed switching applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc – 2N6406, 2N6408
  = 80 Vdc – 2N6407, 2N6409
- DC Current Gain —
  h_{FE} = 30 (Min) @ I_C = 0.5 Adc
  = 12 (Min) @ I_C = 1.5 Adc
- Current-Gain — Bandwidth Product —
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Pin Compatible With TO-220AB Package

2 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

60-80 VOLTS
12.5 WATTS



*MAXIMUM RATINGS

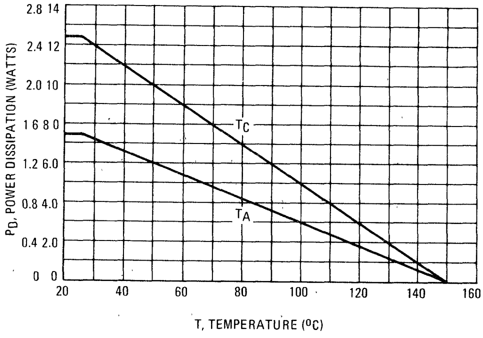
Rating	Symbol	2N6406 2N6408	2N6407 2N6409	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CBO}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →		Vdc
Collector Current — Continuous Peak	I_C	← 2.0 → ← 4.0 →		Adc
Base Current	I_B	← 1.0 →		Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	← 12.5 → ← 0.10 →		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →		°C

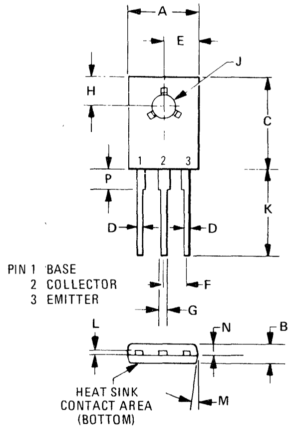
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.295	0.305	7.490	7.750
B	0.095	0.105	2.410	2.670
C	0.425	0.435	10.800	11.050
D	0.020	0.026	0.508	0.660
E	0.145	0.155	3.680	3.940
F	0.093 TP		2.360 TP	
G	0.025	0.035	0.635	0.889
H	0.148	0.158	3.760	4.010
J	0.115	0.118	2.920	3.000
K	0.595	0.645	15.110	16.380
L	0.015	0.025	0.381	0.635
M	3° TYP		3° TYP	
N	0.045	0.055	1.140	1.400
P	0.085	0.095	2.160	2.410

CASE 77-03

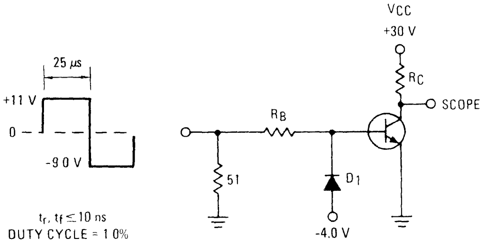
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0) 2N6406, 2N6408 2N6407, 2N6409	$V_{CEO(sus)}$	 60 80	 – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) 2N6406, 2N6408 (V_{CE} = 40 Vdc, I_B = 0) 2N6407, 2N6409	I_{CEO}	 – –	 500 500	μAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N6406, 2N6408 (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N6407, 2N6409 (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C) 2N6406, 2N6408 (V_{CE} = 50 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) 2N6407, 2N6409	I_{CEX}	 – – – –	 1.0 1.0 0.1 0.1	μAdc mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 100 mAdc, V_{CE} = 2.0 Vdc) (I_C = 500 mAdc, V_{CE} = 2.0 Vdc) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	 50 30 12 5.0	 250 – – –	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.5 Adc, I_B = 150 mAdc) (I_C = 2.0 Adc, I_B = 400 mAdc)	$V_{CE(sat)}$	 – – –	 0.5 1.4 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 150 mAdc)	$V_{BE(sat)}$	–	1.5	Vdc
Base-Emitter on Voltage (I_C = 100 mAdc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)	f_T	50	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) 2N6406, 2N6407 2N6408, 2N6409	C_{ob}	 – –	 50 30	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	10	–	–

*Indicates JEDEC Registered Data.

(1) Pulse test: Pulse Width $\leqslant$ 300 μs, Duty Cycle $\leqslant$ 2.0%.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES.

FIGURE 3 — TURN-ON TIME

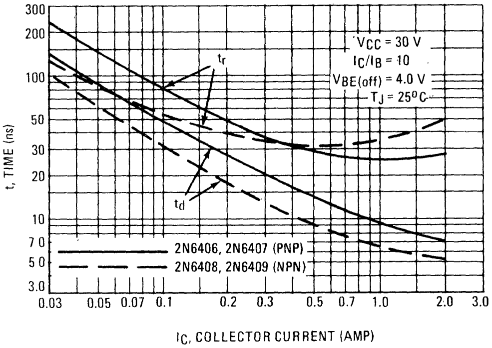
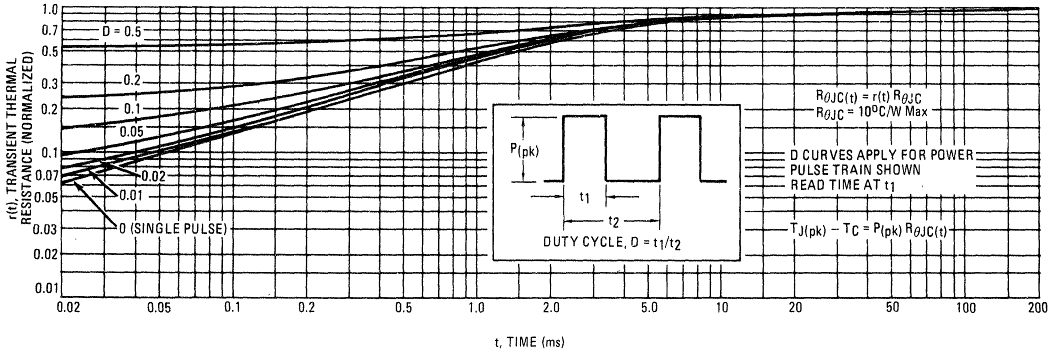


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6406, 2N6407

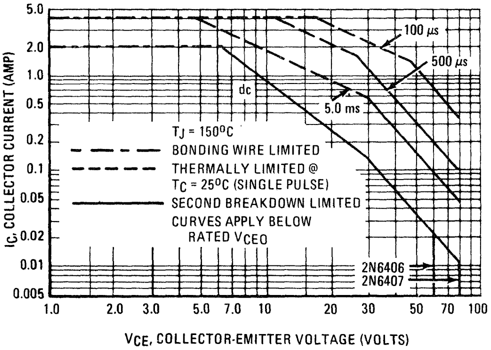
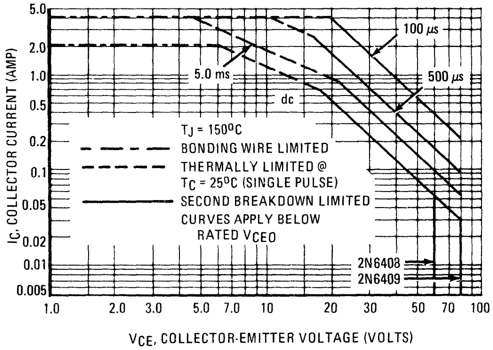


FIGURE 6 – 2N6408, 2N6409



There are two limitations on the power handling ability of a transistor – average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 7 – TURN-OFF TIME

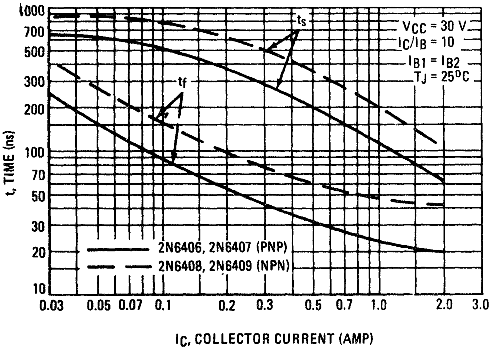
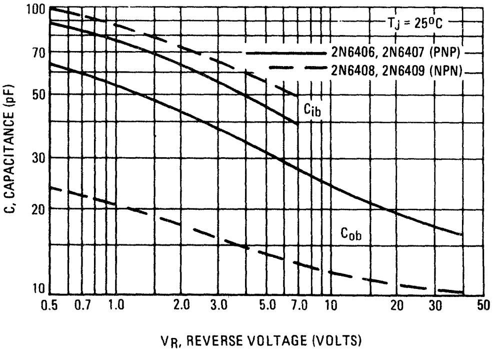


FIGURE 8 – CAPACITANCE



PNP
2N6406, 2N6407

NPN
2N6408, 2N6409

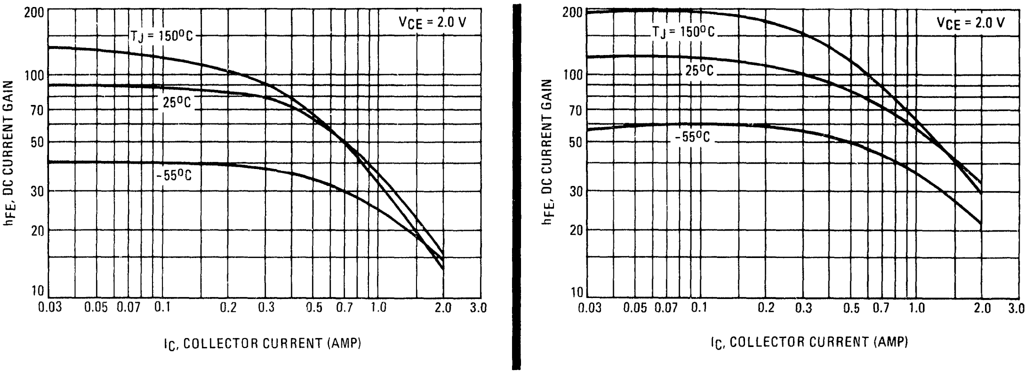


FIGURE 9 – DC CURRENT GAIN

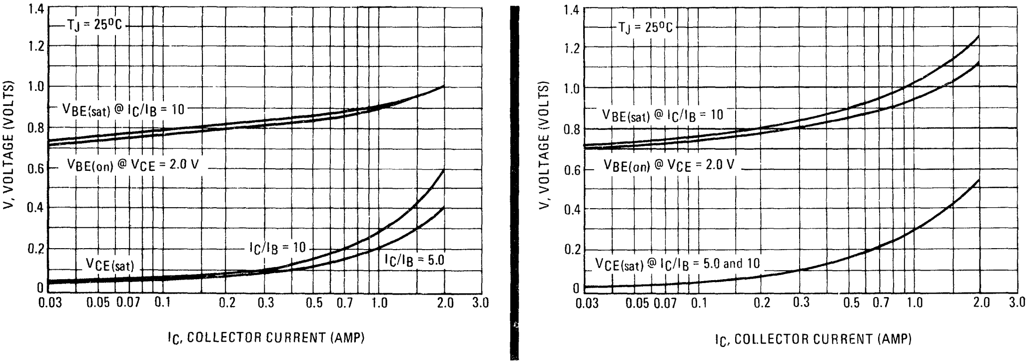


FIGURE 10 – "ON" VOLTAGES

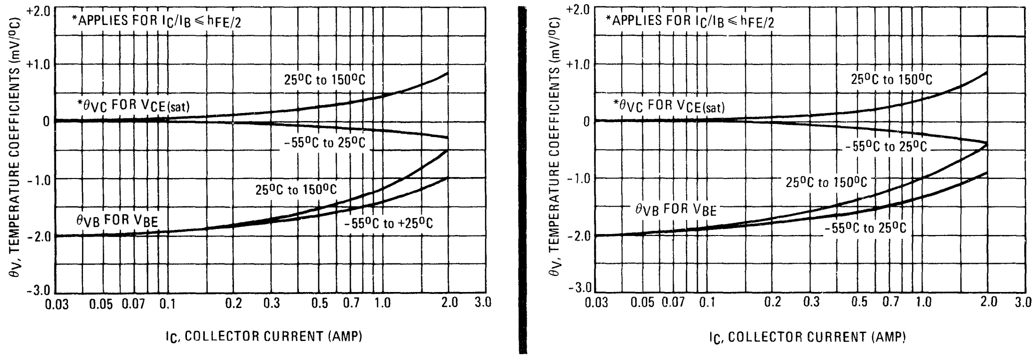


FIGURE 11 – TEMPERATURE COEFFICIENTS

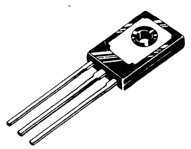
2N6410 NPN (SILICON)
2N6411 PNP

COMPLEMENTARY SILICON ANNULAR POWER PLASTIC TRANSISTORS

. . . designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage – $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain – h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2.0 Adc
  = 10 (Min) @ I_C = 4.0 Adc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 0.35 Vdc (Max) @ I_C = 500 mAdc
  = 0.8 Vdc (Max) @ I_C = 2.0 Adc
- High Current-Gain – Bandwidth Product – f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Pin Compatible with TO-220AB Package

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
25 VOLTS
15 WATTS



*MAXIMUM RATINGS

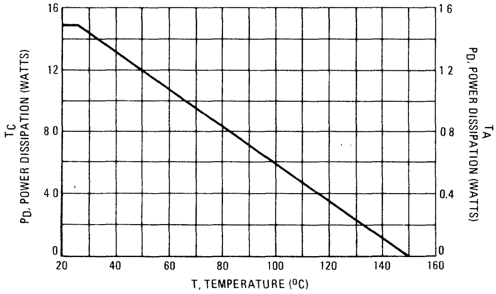
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous Peak	I_C	4.0 8.0	Adc Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

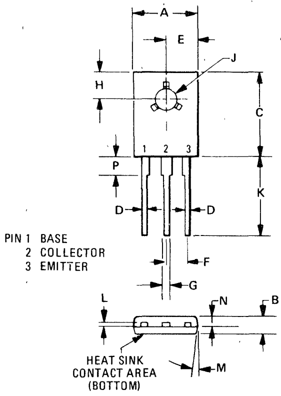
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.295	0 305	7 490	7.750
B	0.095	0 105	2.410	2.670
C	0.425	0.435	10 800	11.050
D	0.020	0.026	0.508	0.660
E	0.145	0.155	3.680	3 940
F	0.093 TP		2.360 TP	
G	0.025	0.035	0.635	0.889
H	0.148	0.158	3.760	4.010
J	0.115	0.118	2.920	3 000
K	0.595	0.645	15.110	16.380
L	0.015	0.025	0.381	0.635
M	3° TYP		3° TYP	
N	0.045	0.055	1 140	1.400
P	0.085	0.095	2 160	2.410

CASE 77-03

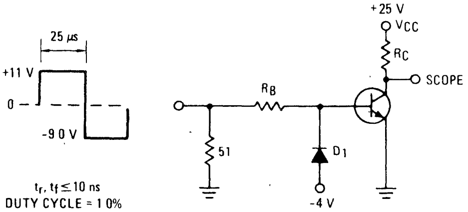
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	–	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	I_{CEO}	–	100	μAdc
Collector Cutoff Current	I_{CEX}			
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		–	1.0	μAdc
(V_{CE} = 20 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		–	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		70	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)		45	180	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)		–	0.35	
(I_C = 2.0 Adc, I_B = 200 mAdc)		–	0.8	
(I_C = 4.0 Adc, I_B = 400 mAdc)		–	1.5	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	–	1.6	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)	f_T	50	–	MHz
Output Capacitance	C_{ob}			pF
(V_{CB} = 10 Vdc, I_C = 0, f = 0.1 MHz) 2N6410		–	80	
2N6411		–	120	
Small-Signal Current Gain (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	50	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

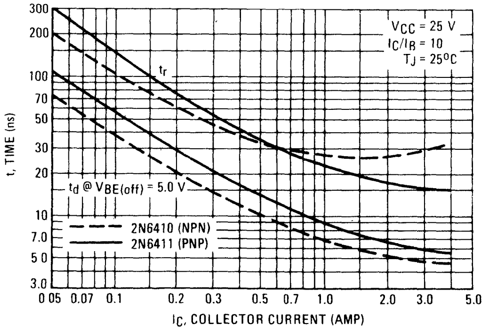


FIGURE 4 – THERMAL RESPONSE

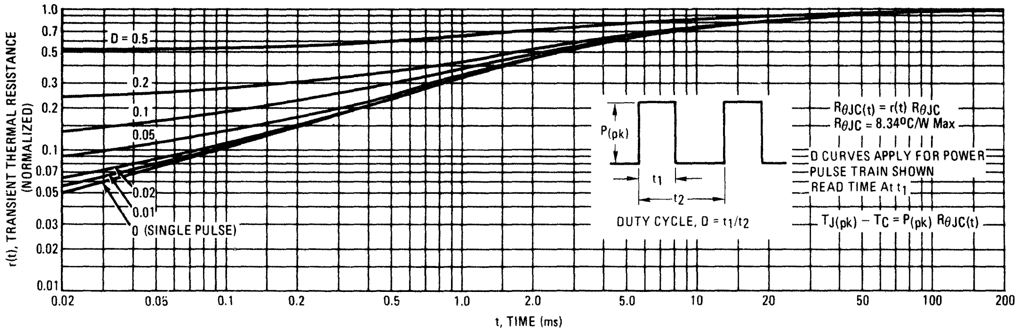
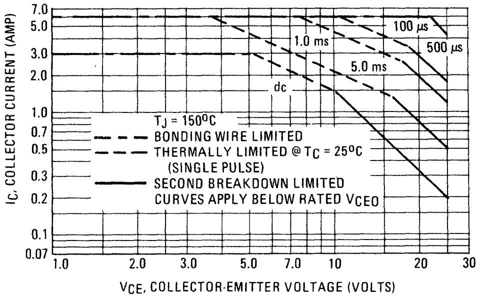


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

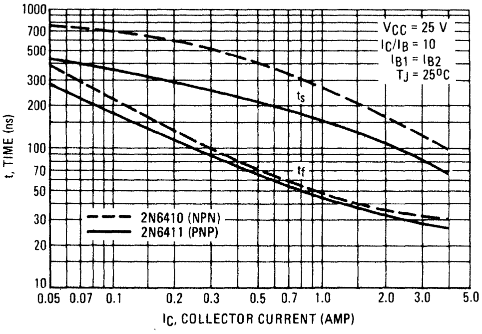
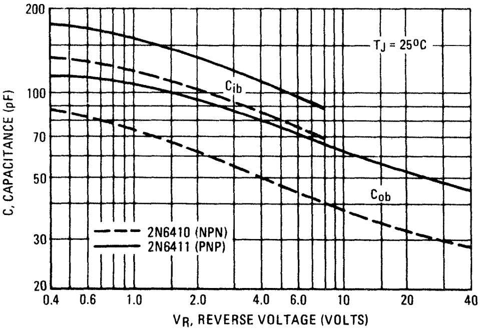


FIGURE 7 – CAPACITANCE



NPN
2N6410

PNP
2N6411

FIGURE 8 – DC CURRENT GAIN

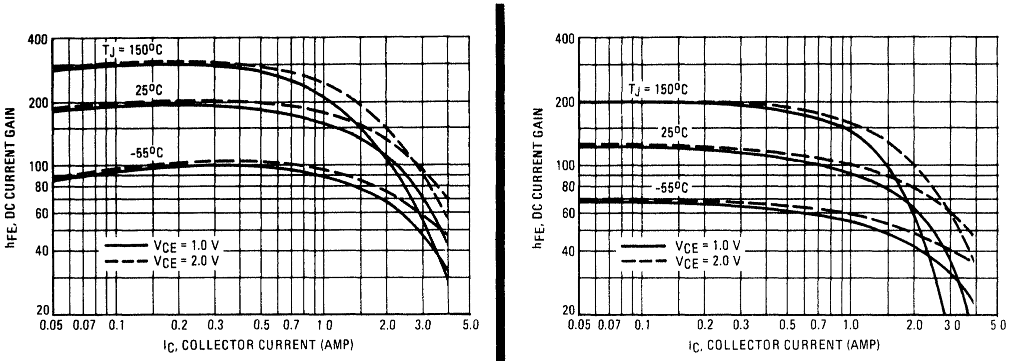


FIGURE 9 – "ON" VOLTAGE

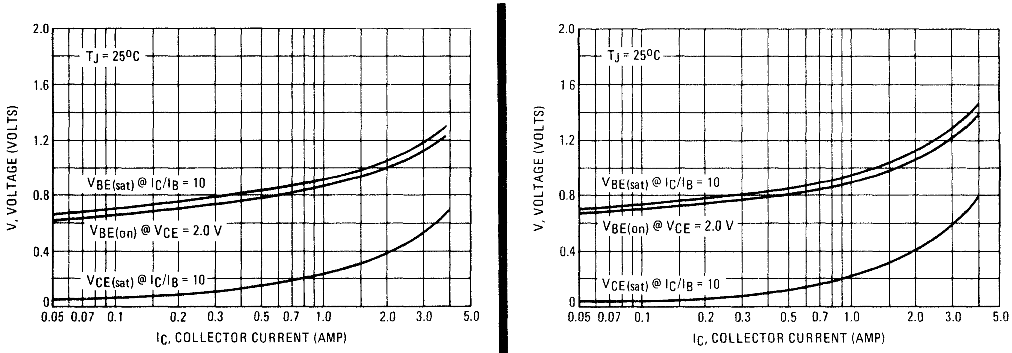
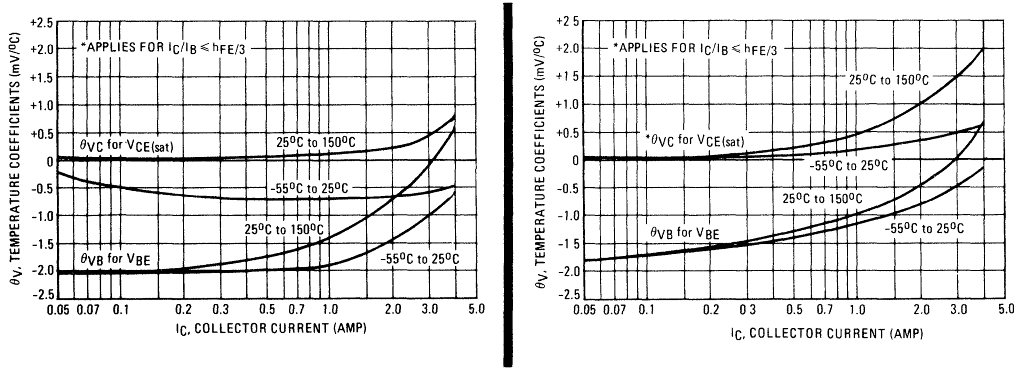


FIGURE 10 – TEMPERATURE COEFFICIENTS



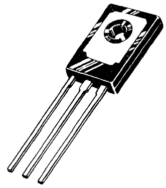
2N6412, 2N6413 NPN (SILICON)
2N6414, 2N6415 PNP

COMPLEMENTARY PLASTIC SILICON ANNULAR POWER TRANSISTORS

. . . designed for low power audio amplifier and low current, high-speed switching applications.

- Low Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N6412, 2N6414
  = 60 Vdc (Min) – 2N6413, 2N6415
- High Current-Gain – Bandwidth Product –
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- DC Current Gain Specified at 0.2, 1.0, 2.0 and 4.0 Adc
- Collector-Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc
- Pin Compatible With TO-220AB Package

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
40, 60 VOLTS
15 WATTS



*MAXIMUM RATINGS

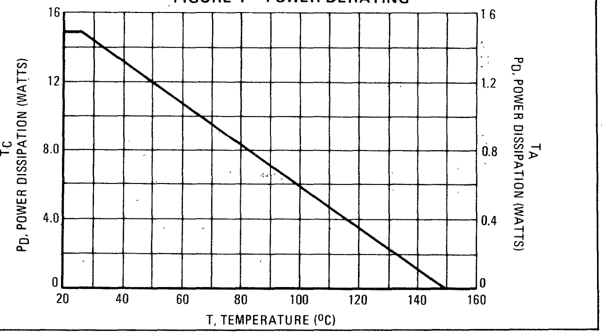
Rating	Symbol	2N6412 2N6414	2N6413 2N6415	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Base Voltage	V_{CBO}	60	80	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	4.0 8.0		Adc Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ $T_C = 25^{\circ}C$ Derate Above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

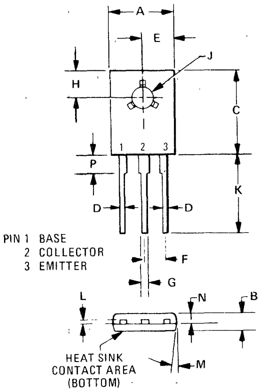
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.295	0.305	7.490	7.750
B	0.095	0.105	2.410	2.670
C	0.425	0.435	10.800	11.050
D	0.020	0.026	0.508	0.660
E	0.145	0.155	3.680	3.940
F	0.093 TP		2.360 TP	
G	0.025	0.035	0.635	0.889
H	0.148	0.158	3.760	4.010
J	0.115	0.118	2.920	3.000
K	0.595	0.645	15.110	16.380
L	0.015	0.025	0.381	0.635
M	3° TYP		3° TYP	
N	0.045	0.055	1.140	1.400
P	0.085	0.095	2.160	2.410

CASE 77-03

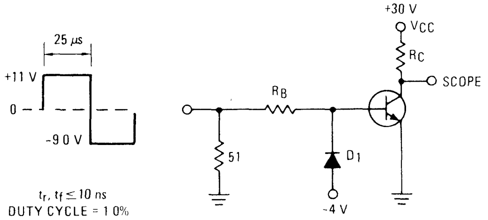
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	 2N6412, 2N6414 2N6413, 2N6415	$V_{CEO(sus)}$	 40 60	 – –	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0)	 2N6412, 2N6414 2N6413, 2N6415	I_{CEO}	 – –	 100 100	μAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	 2N6412, 2N6414	I_{CEX}	 –	 1.0	 μAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6413, 2N6415		–	1.0	
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6412, 2N6414		–	0.1	mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C	2N6413, 2N6415		–	0 1	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 3.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 40 25 20 5.0	 250 – – –	–
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 4.0 Adc, I_B = 800 mAdc)		$V_{CE(sat)}$	 – – – –	 0.4 0.6 0.8 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	1 8	Vdc
Base-Emitter on Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	50	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0) f = 0.1 MHz)	 2N6412, 2N6413 2N6414, 2N6415	C_{ob}	 – –	 50 70	pF
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	10	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE IB ~100 mA
MSD6100 USED BELOW IB ~100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

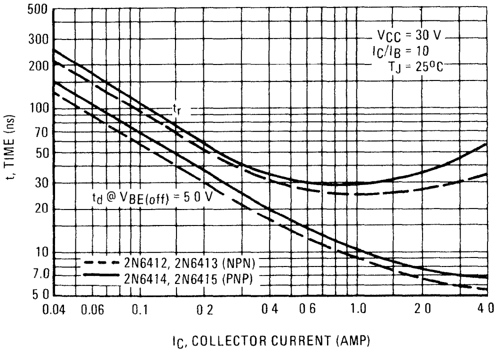


FIGURE 4 – THERMAL RESPONSE

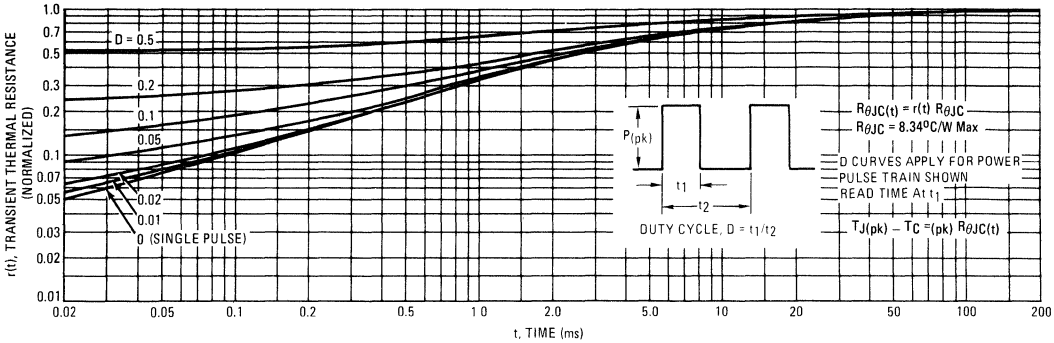
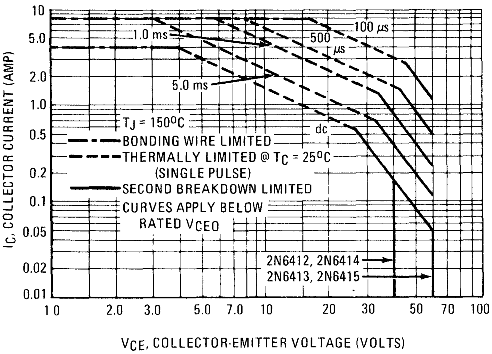


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i e , the transistor must not be subjected to greater dissipation than the curves indicate

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4 At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (See AN-415A)

FIGURE 6 – TURN-OFF TIME

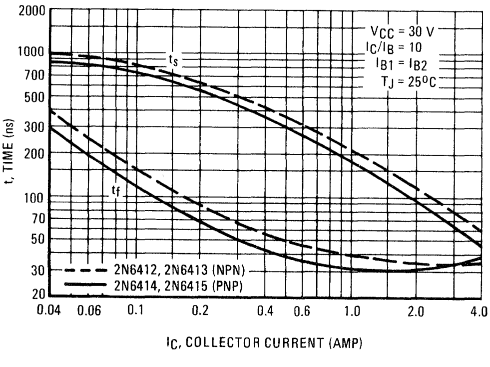
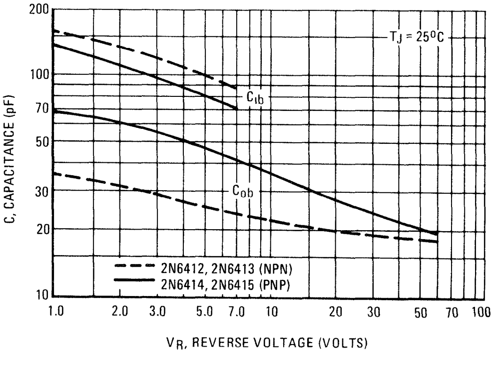


FIGURE 7 – CAPACITANCE



NPN
2N6412, 2N6413

PNP
2N6414, 2N6415

FIGURE 8 – DC CURRENT GAIN

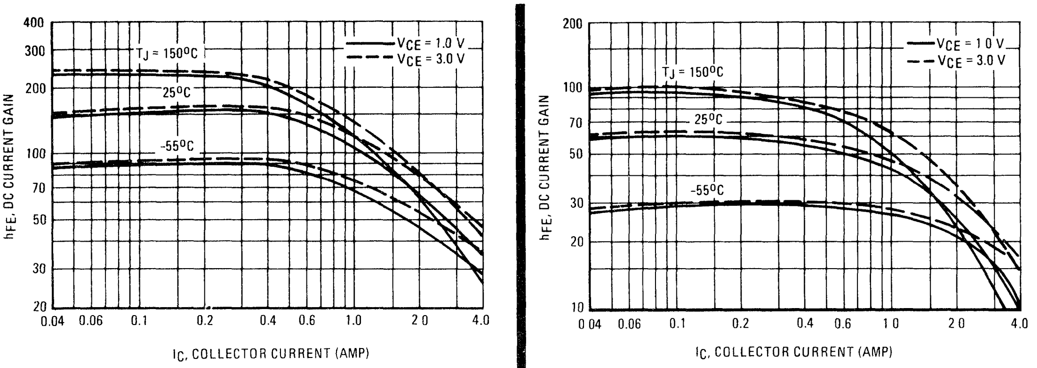


FIGURE 9 – "ON" VOLTAGES

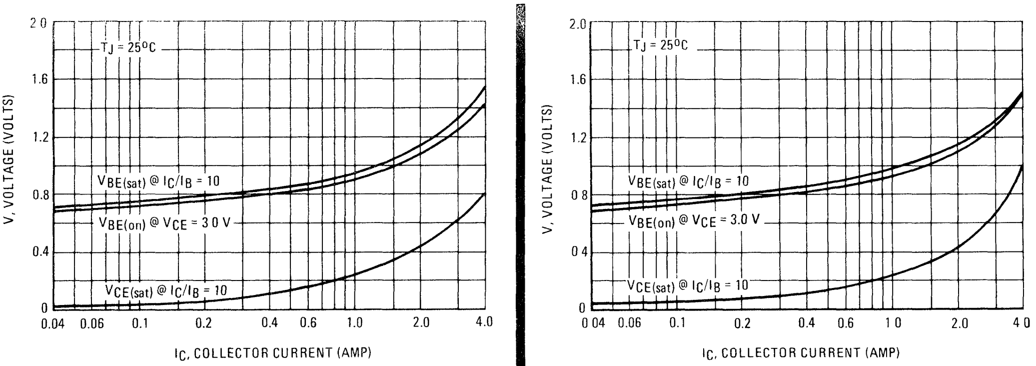
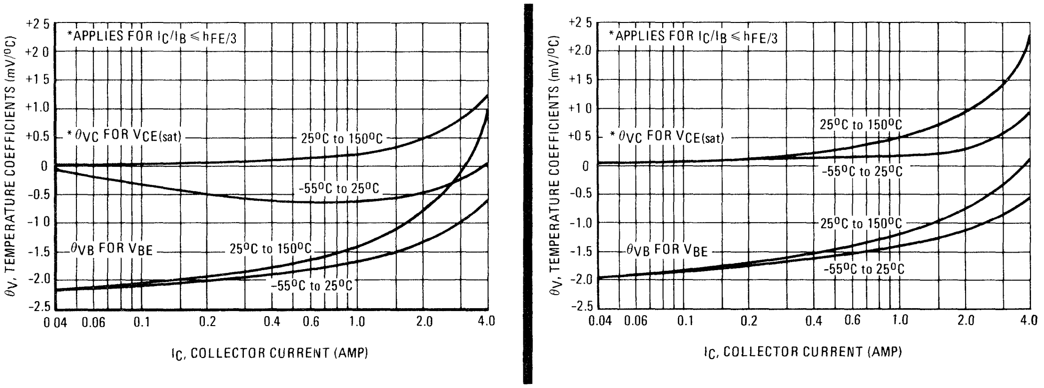


FIGURE 10 – TEMPERATURE COEFFICIENTS



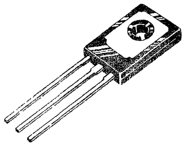
2N6416, 2N6417 NPN (SILICON)
2N6418, 2N6419 PNP

COMPLEMENTARY PLASTIC SILICON ANNULAR POWER TRANSISTORS

. . . designed for low power audio amplifier and low-current, high speed switching applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — 2N6416, 2N6418
  = 100 Vdc (Min) — 2N6417, 2N6419
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40-250
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain — Bandwidth Product —
  f_T = 40 MHz (Min) @ I_C = 100 mAdc)
- Pin Compatible With TO-220AB Package

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
80, 100 VOLTS
15 WATTS



*MAXIMUM RATINGS

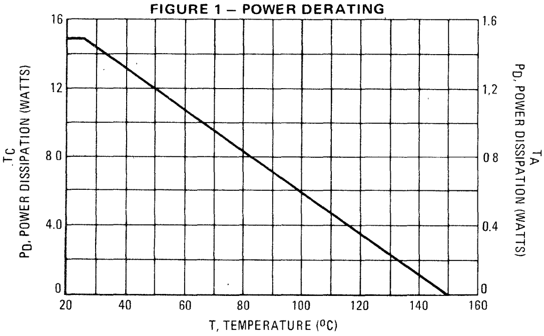
Rating	Symbol	2N6416 2N6418	2N6417 2N6419	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current — Continuous — Peak	I_C	3.0 6.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

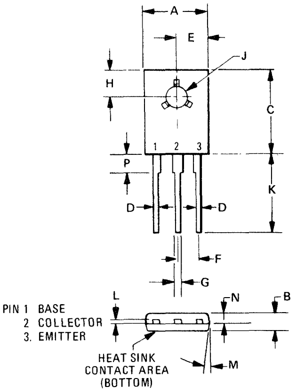
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0 295	0.305	7.490	7 750
B	0.095	0.105	2.410	2.670
C	0.425	0.435	10.800	11.050
D	0.020	0.026	0 508	0.660
E	0.145	0.155	3.680	3 940
F	0 093 TP		2.360 TP	
G	0 025	0.035	0 635	0.889
H	0.148	0.158	3 760	4.010
J	0.115	0.118	2.920	3.000
K	0.595	0.645	15.110	16.380
L	0.015	0 025	0.381	0.635
M	3° TYP		3° TYP	
N	0.045	0.055	1.140	1.400
P	0.085	0 095	2 160	2.410

CASE 77-03

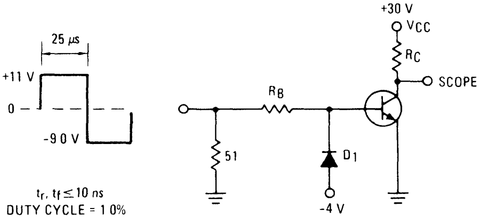
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	2N6416, 2N6418		80	–	
	2N6417, 2N6419		100	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6416, 2N6418		–	100	
(V_{CE} = 50 Vdc, I_B = 0)	2N6417, 2N6419		–	100	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6416, 2N6418		–	1.0	μAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6417, 2N6419		–	1.0	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6416, 2N6418		–	0.1	mAdc
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6417, 2N6419		–	0.1	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 3.0 Vdc)			40	250	
(I_C = 1.0 Adc, V_{CE} = 3.0 Vdc)			20	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			10	–	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
(I_C = 2.0 Adc, I_B = 200 mAdc)			–	2.5	
(I_C = 3.0 Adc, I_B = 600 mAdc)			–	3.0	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 200 mAdc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	40	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_C = 0, f = 0.1 MHz	2N6416,2N6417		–	50	
	2N6418,2N6419		–	70	
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	10	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

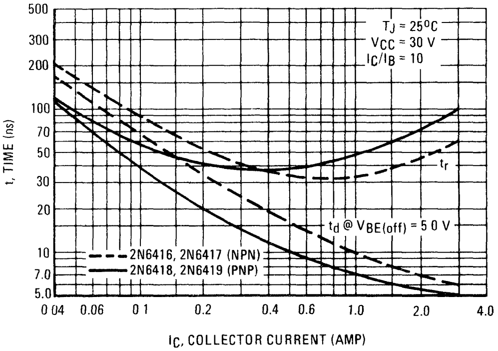


FIGURE 4 – THERMAL RESPONSE

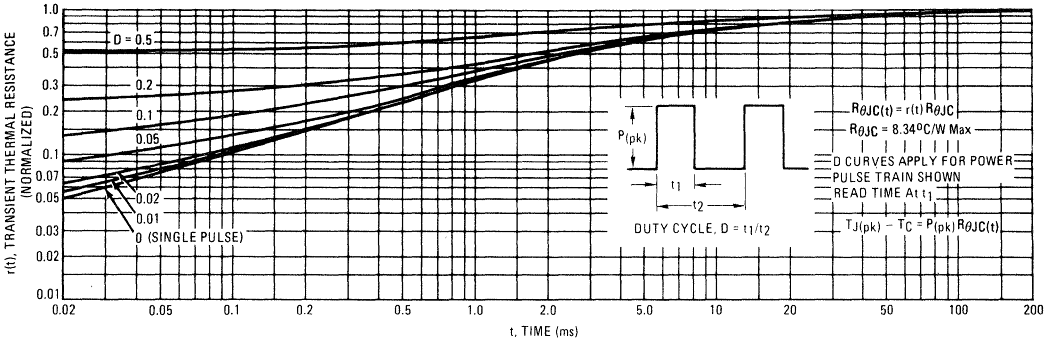
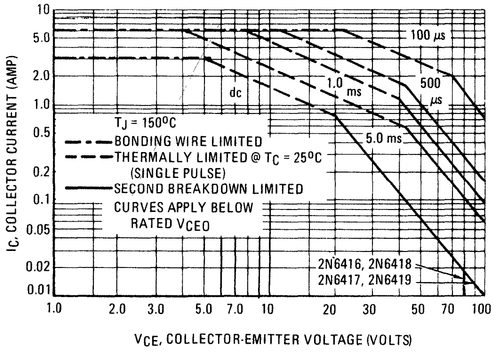


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

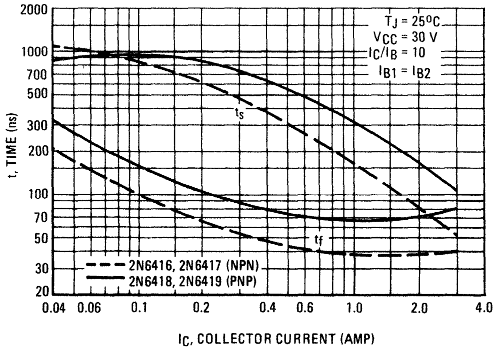
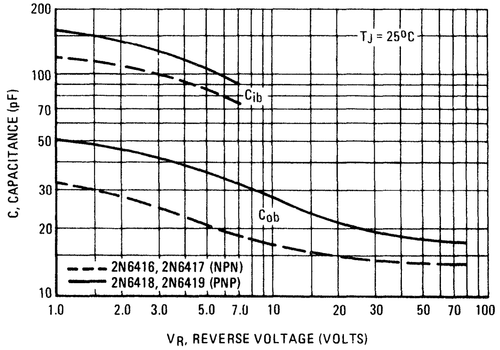


FIGURE 7 – CAPACITANCE



NPN
2N6416, 2N6417

PNP
2N6418, 2N6419

FIGURE 8 – DC CURRENT GAIN

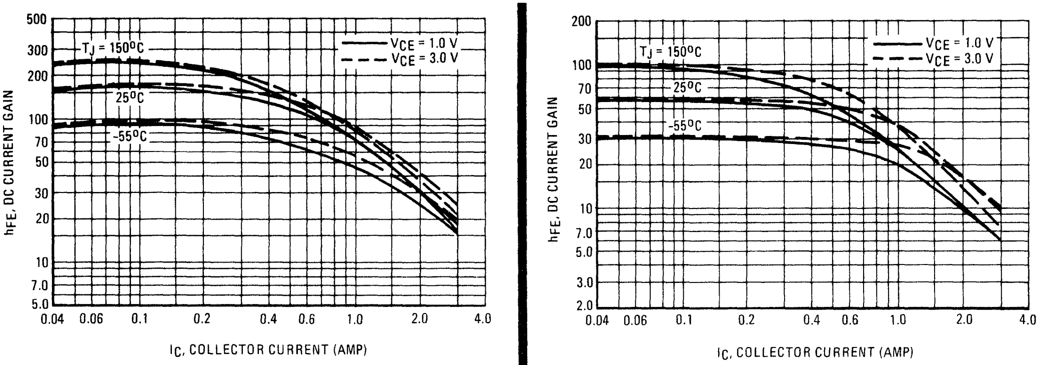


FIGURE 9 – "ON" VOLTAGES

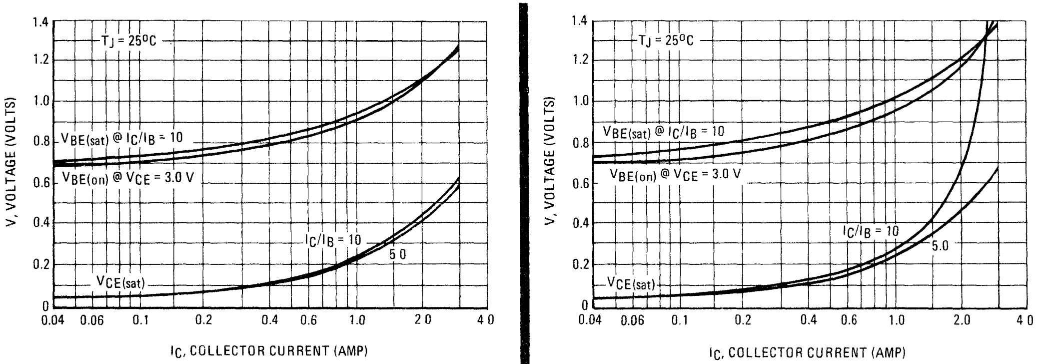
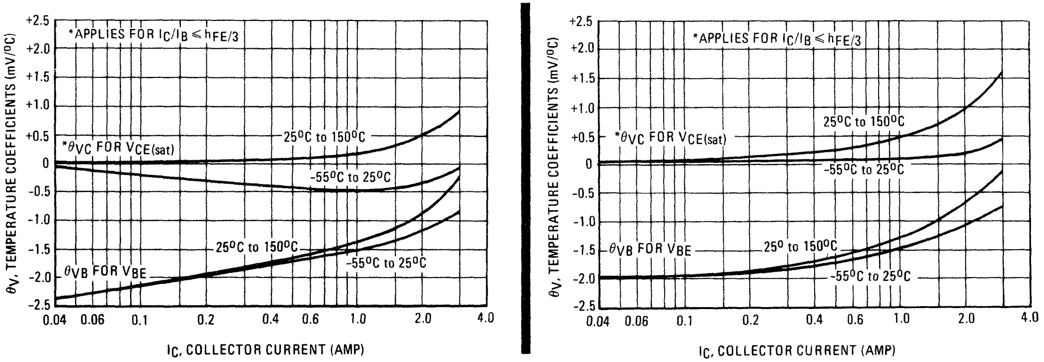


FIGURE 10 – TEMPERATURE COEFFICIENTS



2N6424, 2N6425

For Specifications, See 2N3837 Data, Volume I.

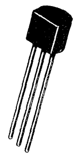
2N6426 (SILICON)
2N6427

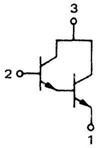
NPN SILICON ANNULAR DARLINGTON TRANSISTORS

. . . designed for use as high-gain amplifiers for audio, chroma, and control circuits; drivers for displays, lamps, buzzers and solenoids.

- Collector-Emitter Breakdown Voltage — BV_{CEO} = 40 Vdc (Min) @ I_C = 10 mAdc
- DC Current Gain specified from 10 mAdc to 500 mAdc
- Low Noise Figure — NF = 3.0 dB (Typ) @ I_C = 1.0 mAdc
- Monolithic Construction

NPN SILICON DARLINGTON TRANSISTORS





*MAXIMUM RATINGS

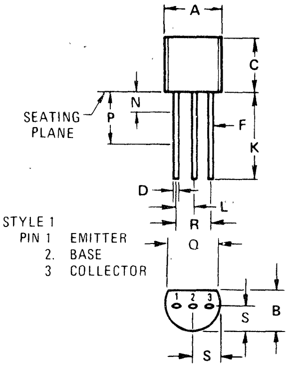
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	12	Vdc
Collector Current — Continous	I_C	500	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

*Indicates JEDEC Registered Data.

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

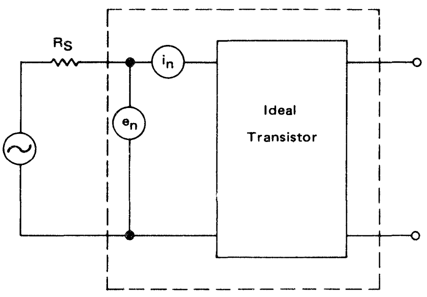
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)		BV_{CEO}	40	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	12	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	–	50	nAdc
Emitter Cutoff Current (V_{BE} = 10 Vdc, I_C = 0)		I_{EBO}	–	–	50	nAdc
Collector Cutoff Current ** (V_{CE} = 25 Vdc, I_B = 0)		I_{CEO}	–	–	1.0	μAdc
ON CHARACTERISTICS						
DC Current Gain (1)		h_{FE}				–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	2N6426		20,000	–	200,000	
	2N6427		10,000	–	100,000	
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	2N6426		30,000	–	300,000	
	2N6427		20,000	–	200,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	2N6426		20,000	–	200,000	
	2N6427		14,000	–	140,000	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
** (I_C = 50 mAdc, I_B = 0.5 mAdc)			–	0.71	1.2	
(I_C = 500 mAdc, I_B = 0.5 mAdc)			–	0.9	1.5	
Base-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 0.5 mAdc)		$V_{BE(sat)}$	–	1.52	2.0	Vdc
Base-Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.24	1.75	Vdc
SMALL-SIGNAL CHARACTERISTICS						
High Frequency Current Gain		$\lvert h_{fe} \rvert$				–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	2N6426		1.5	2.4	–	
	2N6427		1.3	2.4	–	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	5.4	7.0	pF
Input Capacitance (V_{BE} = 1.0 Vdc, I_C = 0, f = 1.0 MHz)		C_{ib}	–	10	15	pF
Input Impedance		h_{ie}				kΩ
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	2N6426		100	–	2000	
	2N6427		50	–	1000	
Small-Signal Current Gain		h_{fe}				–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	2N6426		20,000	–	–	
	2N6427		10,000	–	–	
Output Admittance (I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{oe}	–	–	1000	μmhos
Noise Figure (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, R_S = 100 kΩ, f = 10 kHz to 15.7 kHz)		NF	–	3.0	10	dB

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2.0%.

**Motorola guarantees this data in addition to JEDEC Registered Data.

FIGURE 1 – TRANSISTOR NOISE MODEL



NOISE APPLICATION NOTE

For a transistor, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4KT\,R_S + i_n^2\,R_S^2\right]^{1/2} \qquad (1)$$

(See Figure 1)

Where:

V_T = Total noise voltage at the transistor input (Volts/$\sqrt{\text{Hz}}$)

e_n = noise voltage of the transistor referred to the input (Figure 2)

i_n = noise current of the transistor referred to the input (Figure 3)

K = Boltzman's constant (1.38×10^{-23} j/°K)

T = temperature of the source resistance (°K)

R_S = source resistance (Ohms)

Example:

Find the total noise at the input of a 2N6426 for a collector current of 1.0 mA and a source impedance of 10 Kilohm at a frequency of 100 Hz and at a temperature of 25°C.

Read $e_n = 31$ nV/$\sqrt{\text{Hz}}$ from Figure 2. (Note that this is for a one cycle bandwidth)

Read $i_n = 0.38$ pA/$\sqrt{\text{Hz}}$ from Figure 3.

$$V_T = \left[(31 \times 10^{-9})^2 + (4)(1.38 \times 10^{-23})(300)\ (10 \times 10^3) + (0.38 \times 10^{-12})^2\ (10 \times 10^3)^2\right]^{1/2} = 3.38\ \text{nV}/\sqrt{\text{Hz}}$$

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by the Source Resistance}}$$

or:

$$NF = 20 \log_{10} \left(\frac{V_T^2}{4\ KT\ R_S}\right)^{1/2} \qquad (2)$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(33.8 \times 10^{-9})^2}{16.6 \times 10^{-17}}\right]^{1/2} = 8.4\ \text{dB}$$

To minimize noise in a transistor stage, one might use Figure 5 and deduce that noise is minimized when Noise Figure is minimum. This is not necessarily true as shown by Figure 4 where the total noise voltage is a minimum at small values of source impedance. This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For Constant transistor noise, multiply, V_T by the square root of bandwidth, i.e., $V'_T = V_T \bullet \Delta f^{1/2}$.
2. For variable transistor noise, plot V_T (where Δf = 1.0 Hz) versus frequency over the bandwidth and integrate the result.

Total noise voltage at the output of the transistor stage can be found by multiplying V_T or V'_T by the voltage gain of the stage.

NOISE CHARACTERISTICS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

FIGURE 2 — NOISE VOLTAGE

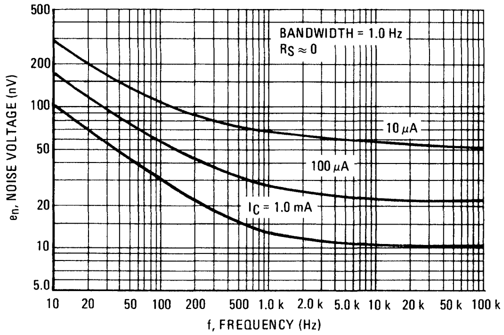


FIGURE 3 — NOISE CURRENT

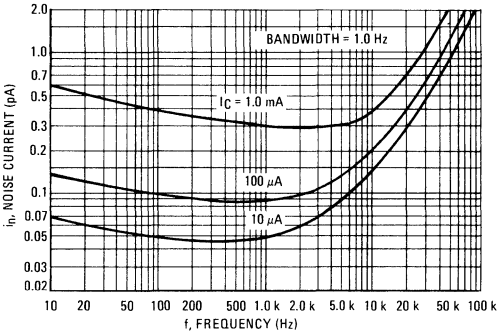


FIGURE 4 — TOTAL WIDEBAND NOISE VOLTAGE

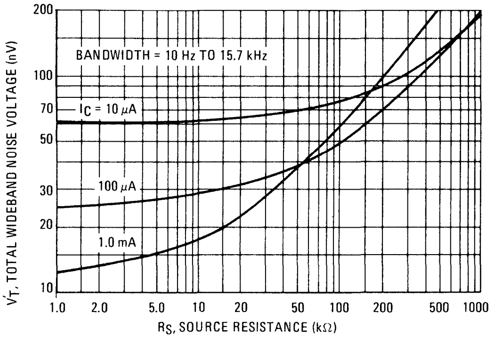
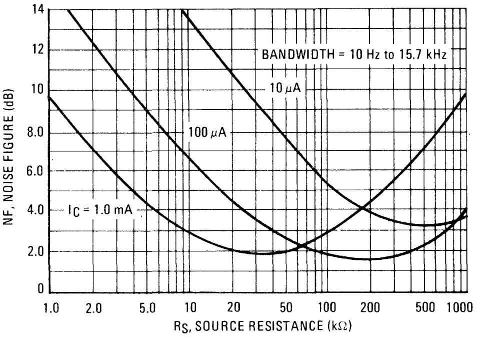


FIGURE 5 — WIDEBAND NOISE FIGURE



DYNAMIC CHARACTERISTICS

FIGURE 6 — CAPACITANCE

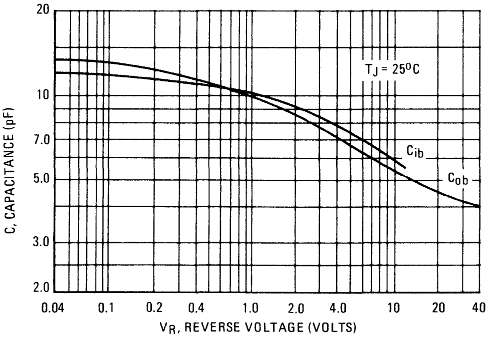


FIGURE 7 — HIGH FREQUENCY CURRENT GAIN

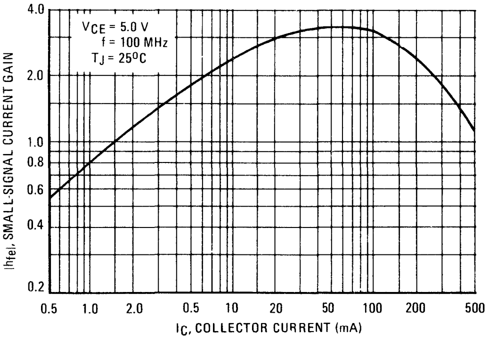


FIGURE 8 – DC CURRENT GAIN

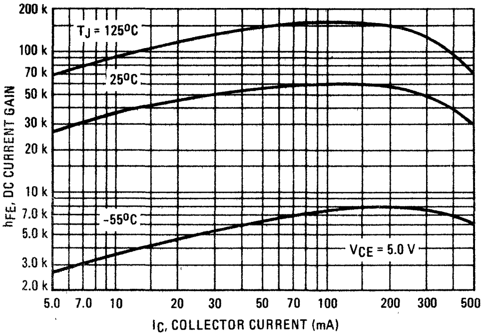


FIGURE 9 – COLLECTOR SATURATION REGION

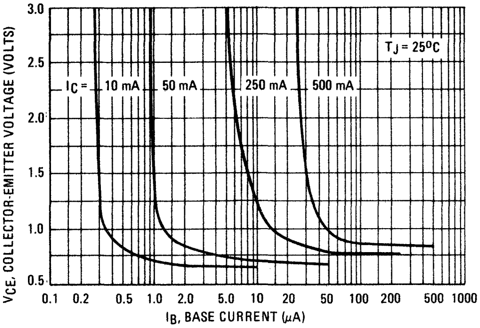


FIGURE 10 – "ON" VOLTAGES

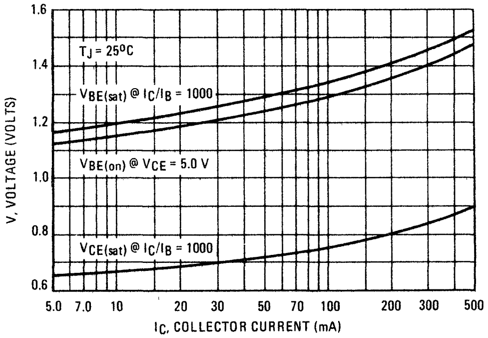


FIGURE 11 – TEMPERATURE COEFFICIENTS

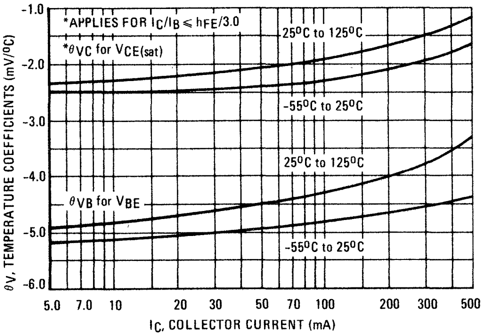


FIGURE 12 – THERMAL RESPONSE

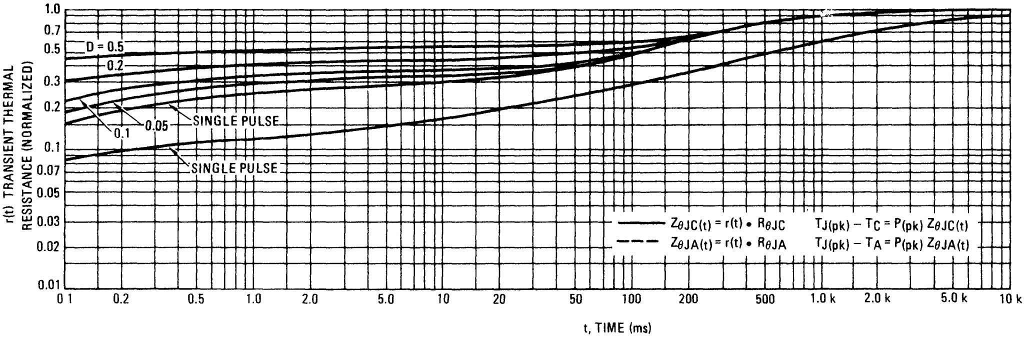
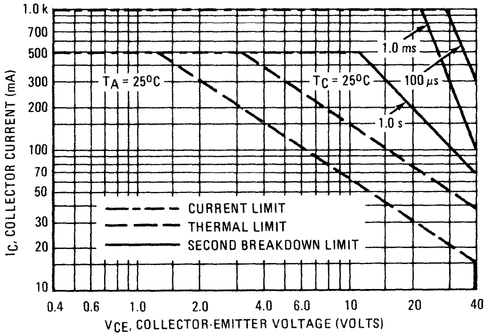


FIGURE 13 – ACTIVE REGION SAFE OPERATING AREA

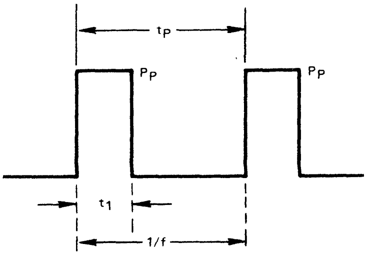


The safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 13 is based upon $T_{J(pk)} = 150^{\circ}C$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case or ambient temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

Figure A



Duty Cycle = $t_1 f = \frac{t_1}{t_P}$

Peak Pulse Power = P_P

A train of periodical power pulses can be represented by the model as shown in Figure A. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $Z_{\theta JC(t)}$, multiply the value obtained from Figure 12 by the steady state value $R_{\theta JC}$.

Example:

The 2N6426 is dissipating 2.0 watts under the following conditions:

$t_1 = 1.0$ ms, $t_P = 5.0$ ms. ($D = 0.2$)

Using Figure 12, at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.4.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_P \times R_{\theta JC} = 0.4 \times 2.0 \times 83.3 = 66.5^{\circ}C$$

For more information, see AN-569.

2N6436 (SILICON)
2N6437
2N6438

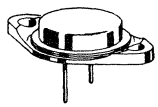
HIGH-POWER PNP SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 80 Vdc (Min) – 2N6436
  = 100 Vdc (Min) – 2N6437
  = 120 Vdc (Min) – 2N6438
- High DC Current Gain –
  h_{FE} = 20-80 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 μs (Max)
  t_s = 1.0 μs (Max)
  t_f = 0.25 μs (Max)
- Hard Solder Construction
- Complement to NPN 2N6338 thru 2N6341

25 AMPERE
POWER TRANSISTORS
PNP SILICON

80, 100, 120 VOLTS
200 WATTS



*MAXIMUM RATINGS

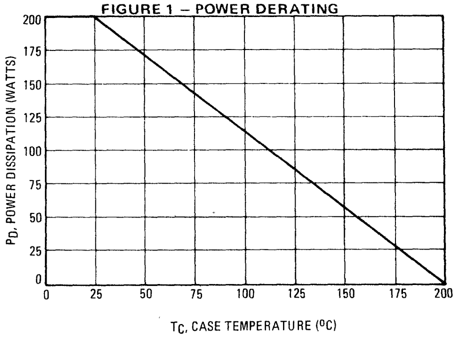
Rating	Symbol	2N6436	2N6437	2N6438	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 25 → ← 50 →			Adc
Base Current	I_B	← 10 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 200 → ← 1.14 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

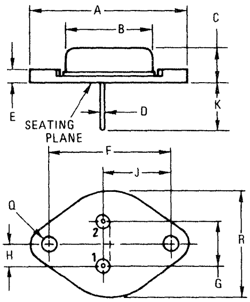
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE.
1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01

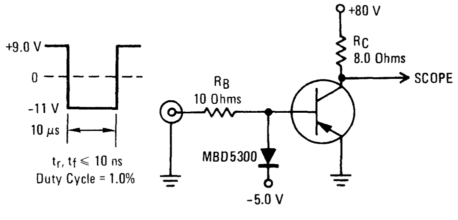
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6436		80	–	
	2N6437		100	–	
	2N6438		120	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6436		–	50	
(V_{CE} = 50 Vdc, I_B = 0)	2N6437		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6438		–	50	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = −1.5 Vdc)	2N6436		–	10	
(V_{CE} = 110 Vdc, $V_{BE(off)}$ = −1.5 Vdc)	2N6437		–	10	
(V_{CE} = 130 Vdc, $V_{BE(off)}$ = −1.5 Vdc)	2N6438		–	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = −1.5 Vdc, T_C = 150°C)	2N6436		–	1.0	mAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = −1.5 Vdc, T_C = 150°C)	2N6437		–	1.0	
(V_{CE} = 120 Vdc, $V_{BE(off)}$ = −1.5 Vdc, T_C = 150°C	2N6438		–	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 100 Vdc, I_E = 0)	2N6436		–	10	
(V_{CB} = 120 Vdc, I_E = 0)	2N6437		–	10	
(V_{CB} = 140 Vdc, I_E = 0)	2N6438		–	10	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			30	–	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			20	80	
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			12	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.0	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	1.8	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.8	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	2.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	–	MHz
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	700	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = 1.0 Adc)		t_r	–	0.3	μs
Storage (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	–	1.0	μs
Fall Time (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ⩽ 300 μs; Duty Cycle ⩽ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN-ON TIME

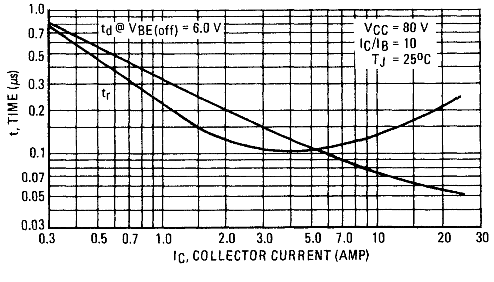


FIGURE 4 – THERMAL RESPONSE

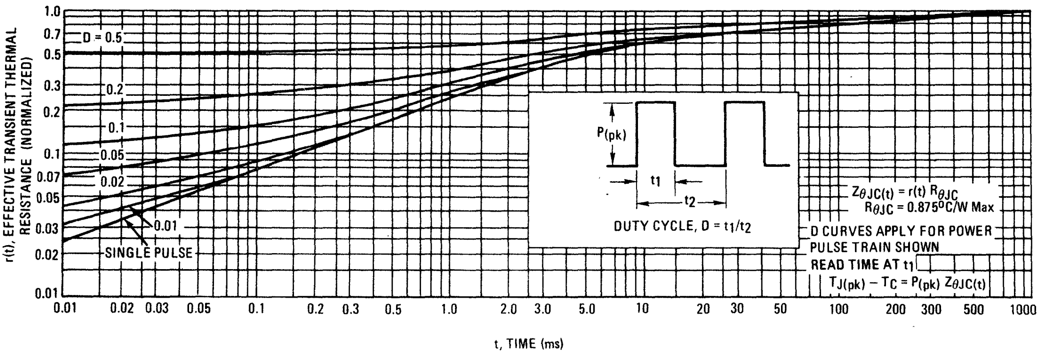
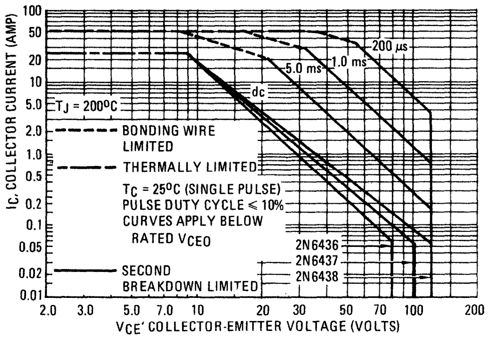


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

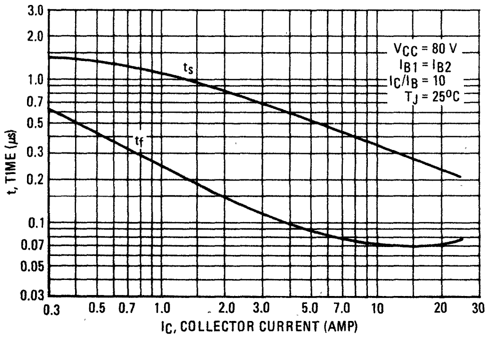
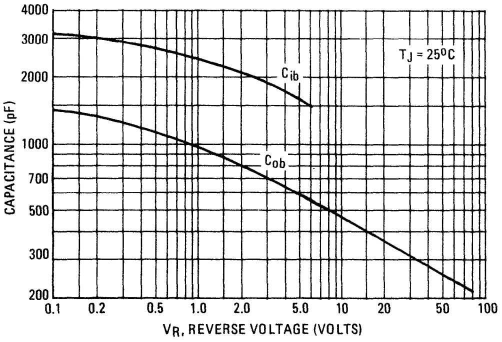


FIGURE 7 – CAPACITANCE



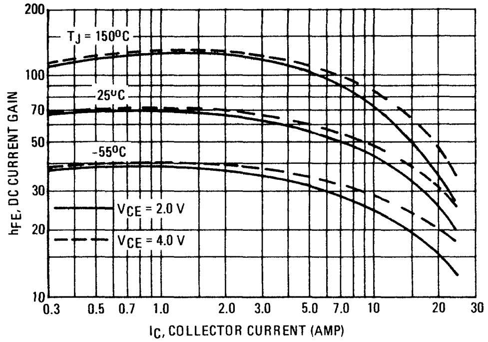


FIGURE 8 – DC CURRENT GAIN

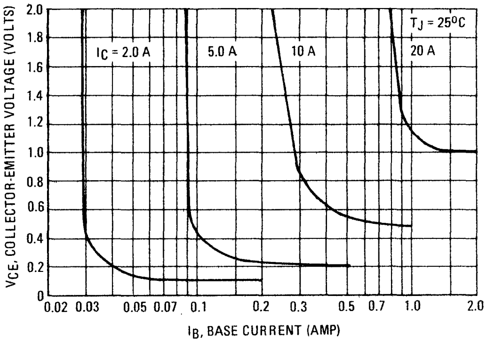


FIGURE 9 – COLLECTOR SATURATION REGION

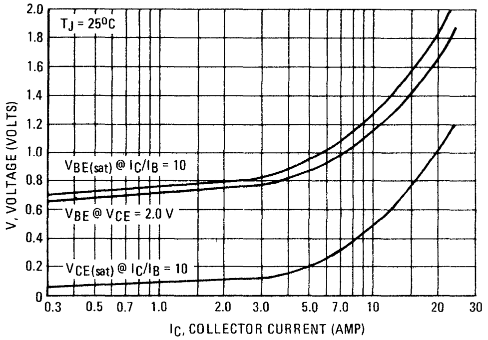


FIGURE 10 – "ON" VOLTAGE

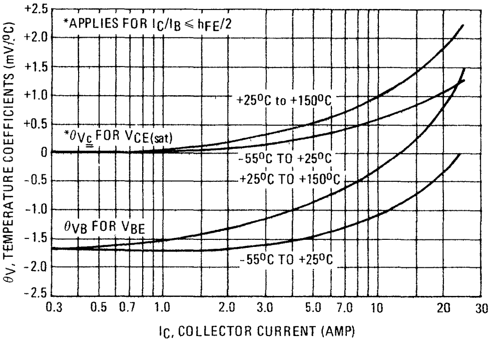


FIGURE 11 – TEMPERATURE COEFFICIENTS

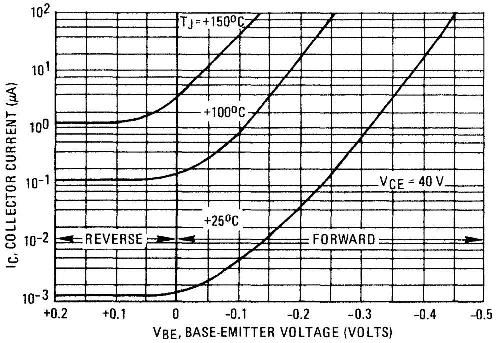


FIGURE 12 – COLLECTOR CUT-OFF REGION

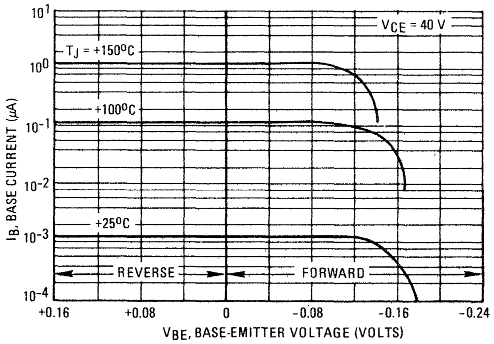


FIGURE 13 – BASE CUT-OFF REGION

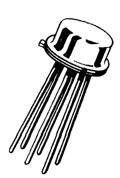
2N6441 (SILICON)
thru
2N6448

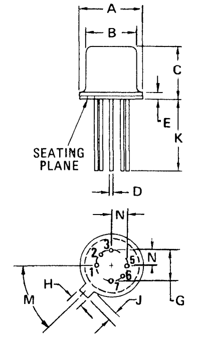
MULTIPLE SILICON ANNULAR MONOLITHIC TRANSISTORS

. . . designed for use as differential amplifiers, dual general-purpose amplifiers, front end detectors and temperature compensation applications.

- Excellent Temperature Tracking – 2N6445 thru 2N6448
  $\Delta|V_{BE1} - V_{BE2}|$ = 0.8 mVdc (Max) @ -55 to +25°C
  = 1.0 mVdc (Max) @ +25 to +125°C
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.1 Vdc (Typ) @ I_C = 1.0 mAdc
- DC Current Gain Specified – 10 μAdc to 1.0 mAdc
- High Current-Gain-Bandwidth Product–
  f_T = 500 MHz (Typ) @ I_C = 0.5 mAdc

NPN SILICON
MONOLITHIC
MULTIPLE
TRANSISTORS





STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. OMITTED
5. EMITTER
6. BASE
7. COLLECTOR
8. OMITTED

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.70	0.150	0.185
D	0.41	0.53	0.016	0.021
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

CASE 654-07

*MAXIMUM RATING

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	45	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous	I_C	10	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D(1)	550 3.14	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D(1)	1.4 8.0	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

(1) One die or both die with equal power

THERMAL CHARACTERISTICS

Characteristic		Junction to Case	Junction to Ambient	Unit
Thermal Resistance	Each Die Effective, 2 Die	125	319	°C/W
Coupling Factors		100	100	%

*Indicates JEDEC Registered Data

THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

(1) $\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2}$

Where ΔT_{J1} is the change in junction temperature of die 1
$R_{\theta 1}$ and $R_{\theta 2}$ is the thermal resistance of die 1 and die 2
P_{D1} and P_{D2} is the power dissipated in die 1 and die 2
$K_{\theta 2}$ is the thermal coupling between die 1 and die 2.

An effective package thermal resistance can be defined as follows:

(2) $R_{\theta(EFF)} = \Delta T_{J1}/P_{DT}$

Where P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to:

(3) $\Delta T_{J1} = R_{\theta 1} (P_{D1} + K_{\theta 2} P_{D2})$

For the conditions where $P_{D1} = P_{D2}$, $P_{DT} = 2\ P_D$, equation (3) can be further simplified and by substituting into equation (2) results in:

(4) $R_{\theta(EFF)} = R_{\theta 1} (1 + K_{\theta 2}) / 2$

Values for the coupling factors when either the case or the ambient is used as a reference are given in the table on page 1.

***ELECTRICAL CHARACTERISTICS** ($T_A = 25^{\circ}C$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 10$ mAdc, $I_B = 0$)	BV_{CEO}	45	–	Vdc
Collector-Base Breakdown Voltage ($I_C = 10\ \mu$Adc, $I_E = 0$)	BV_{CBO}	60	–	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\ \mu$Adc, $I_C = 0$)	BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$)	I_{CBO}	–	5.0	nAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}	–	5.0	nAdc
Collector Cutoff Current ($V_{CE} = 5.0$ Vdc, $I_B = 0$)	I_{CEO}	–	5.0	nAdc
Collector-Collector Leakage Current ($V_{C1-C2} = 100$ Vdc)	I_{C1-C2}	–	5.0	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
($I_C = 10\ \mu$Adc, $V_{CE} = 5.0$ Vdc) 2N6441, 43, 45, 47		60	240	
2N6442, 44, 46, 48		120	600	
($I_C = 100\ \mu$Adc, $V_{CE} = 5.0$ Vdc) 2N6441, 43, 45, 47		100	–	
2N6442, 44, 46, 48		200	–	
($I_C = 100\ \mu$Adc, $V_{CE} = 5.0$ Vdc, $T_A = -55^{\circ}C$)				
2N6441, 43, 45, 47		30	–	
2N6442, 44, 46, 48		60	–	
($I_C = 1.0$ mAdc, $V_{CE} = 5.0$ Vdc) 2N6441, 43, 45, 47		125	–	
2N6442, 44, 46, 48		250	–	
Collector-Emitter Saturation Voltage ($I_C = 1.0$ mAdc, $I_B = 0.1$ mAdc)	$V_{CE(sat)}$	–	0.3	Vdc
Base-Emitter On Voltage ($I_C = 100\ \mu$Adc, $V_{CE} = 5.0$ Vdc)	$V_{BE(on)}$	–	0.7	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (2) ($I_C = 0.5$ mAdc, $V_{CE} = 5.0$ Vdc, f = 20 MHz)	f_T	160	–	MHz
Collector-Base Capacitance ($V_{CB} = 5.0$ Vdc, $I_E = 0$, f = 140 kHz)	C_{cb}	–	1.5	pF
Collector-Collector Capacitance ($V_{C1-C2} = 0$)	C_{C1-C2}	–	1.5	pF
Emitter-Base Capacitance ($V_{BE} = 0.5$ Vdc, $I_C = 0$, f = 140 kHz)	C_{eb}	–	2.0	pF
Noise Figure	NF			dB
($I_C = 10\ \mu$Adc, $V_{CE} = 5.0$ Vdc, $R_S = 10$ k ohms, BW = 15.7 kHz)		–	4.0	
($I_C = 10\ \mu$Adc, $V_{CE} = 5.0$ Vdc, $R_S = 10$ k ohms, f = 10 kHz, BW = 20 Hz)		–	3.0	

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width $\leqslant 300\ \mu$s, Duty Cycle $\leqslant 2.0\%$
(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity

ELECTRICAL CHARACTERISTICS (continued)

Characteristic		Symbol	Min	Max	Unit
***MATCHING CHARACTERISTICS**					
DC Current Gain Ratio (3)		h_{FE1}/h_{FE2}			–
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc)	2N6441, 2N6442		0.6	1.0	
	2N6443, 2N6444		0.8	1.0	
	2N6445, 2N6446		0.9	1.0	
	2N6447, 2N6448		0.95	1.0	
Base-Emitter Voltage Differential		$\lvert V_{BE1}-V_{BE2}\rvert$			mVdc
(I_C = 10 μAdc, V_{CE} = 5.0 Vdc)	2N6441, 2N6442		–	10	
	2N6443, 2N6444		–	5.0	
	2N6445 thru 2N6448		–	3.0	
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc)	2N6441, 2N6442		–	10	
	2N6443, 2N6444		–	5.0	
	2N6445 thru 2N6448		–	3.0	
Base-Emitter Voltage Differential Change Due to Temperature		$\Delta\lvert V_{BE1}-V_{BE2}\rvert$			mVdc
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, T_A = -55 to +25°C)	2N6441, 2N6442		–	3.2	
	2N6443, 2N6444		–	1.6	
	2N6445 thru 2N6448		–	0.8	
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, T_A = +25 to +125°C)	2N6441, 2N6442		–	4.0	
	2N6443, 2N6444		–	2.0	
	2N6445 thru 2N6448		–	1.0	

*Indicates JEDEC Registered Data

(3) The lowest h_{FE} reading is taken as h_{FE1} for this ratio.

NOISE FIGURE
(V_{CE} = 5.0 Vdc, T_A = 25°C)

FIGURE 1 – FREQUENCY EFFECTS

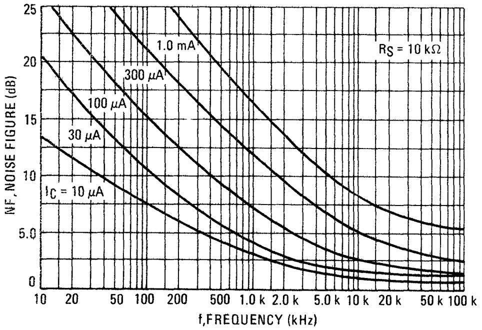


FIGURE 2 – SOURCE RESISTANCE EFFECTS

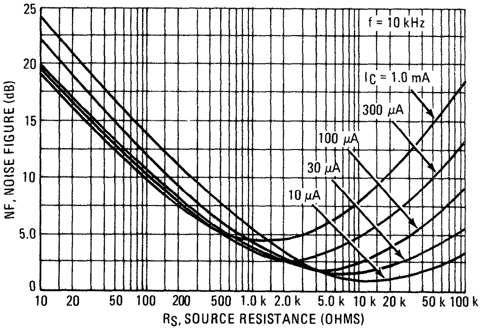


FIGURE 3 – DC CURRENT GAIN

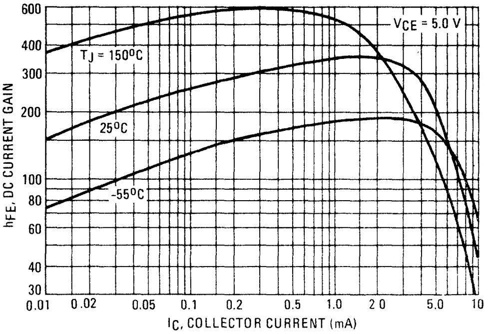


FIGURE 4 – "ON" VOLTAGES

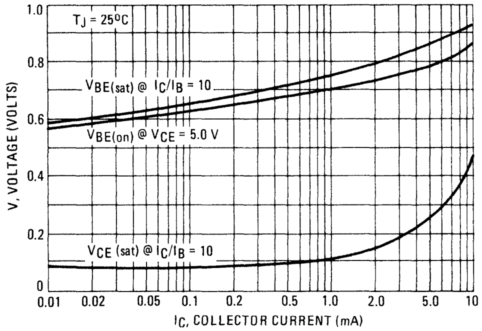


FIGURE 5 – TEMPERATURE COEFFICIENTS

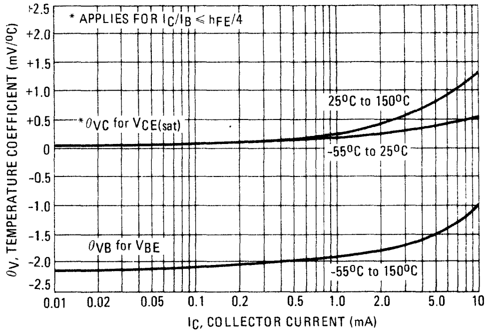


FIGURE 6 – CURRENT-GAIN–BANDWIDTH PRODUCT

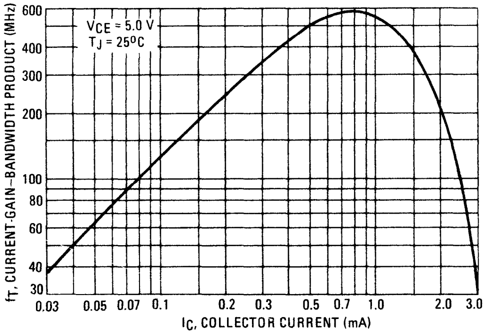
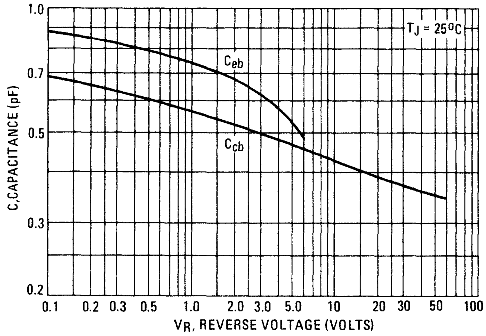


FIGURE 7 – CAPACITANCE



2N6497 (SILICON)
2N6498
2N6499

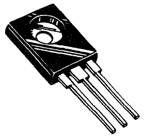
HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

· · · designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications in associated consumer products.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 250 Vdc (Min) – 2N6497
  = 300 Vdc (Min) – 2N6498
  = 350 Vdc (Min) – 2N6499
- Excellent DC Current Gain –
  h_{FE} = 10 – 75 @ I_C = 2.5 Adc
- Low Collector-Emitter Saturation Voltage @ I_C = 2.5 Adc –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) – 2N6497
  = 1.25 Vdc (Max) – 2N6498
  = 1.5 Vdc (Max) – 2N6499

5 AMPERE
POWER TRANSISTORS
NPN SILICON

250, 300, 350 VOLTS
80 WATTS



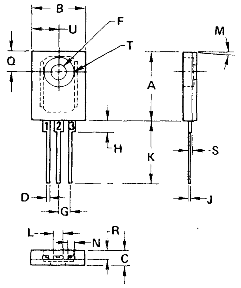
*MAXIMUM RATINGS

Rating	Symbol	2N6497	2N6498	2N6499	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous – Peak	I_C	← 5.0 → ← 10 →			Adc
Base Current	I_B	← 2.0 →			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 80 → ← 0.64 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C
Stud Torque	–	← 8.0 →			In. Lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W

*Indicates JEDEC Registered Data.



STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0 152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

1. DIM "G" IS TO CENTER LINE OF LEADS.

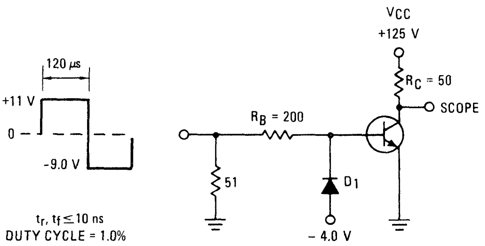
CASE 199-04

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$				Vdc
(I_C = 25 mAdc, I_B = 0)	2N6497		250	–	–	
	2N6498		300	–	–	
	2N6499		350	–	–	
Collector Cutoff Current		I_{CEX}				mAdc
(V_{CE} = 350 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6497		–	–	1.0	
(V_{CE} = 400 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6498		–	–	1.0	
(V_{CE} = 450 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6499		–	–	1.0	
(V_{CE} = 175 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	2N6497		–	–	10	
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	2N6498		–	–	10	
(V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	2N6499		–	–	10	
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				–
(I_C = 2.5 Adc, V_{CE} = 10 Vdc)			10	–	75	
(I_C = 5.0 Adc, V_{CE} = 10 Vdc)			3.0	–	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 500 mAdc)	2N6497		–	–	1.0	
	2N6498		–	–	1.25	
	2N6499		–	–	1.5	
(I_C = 5.0 Adc, I_B = 2.0 Adc)	All Devices		–	–	5.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 500 mAdc)			–	–	1.5	
(I_C = 5.0 Adc, I_B = 2.0 Adc)			–	–	2.5	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	5.0	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	–	150	pF
SWITCHING CHARACTERISTICS						
Rise Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = 0.5 Adc)		t_r	–	0.4	0.8	μs
Storage Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, V_{BE} = 5.0 Vdc, I_{B1} = I_{B2} = 0.5 Adc)		t_s	–	1.4	1.8	μs
Fall Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 Adc)		t_f	–	0.45	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FIGURE 2 – TURN-ON TIME

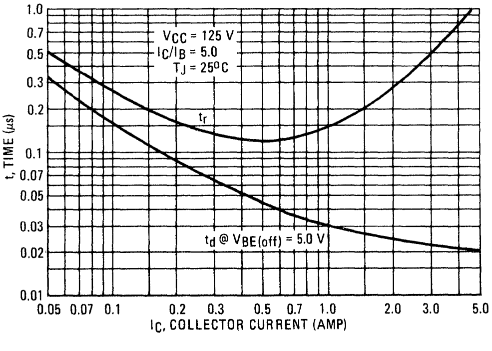


FIGURE 3 – THERMAL RESPONSE

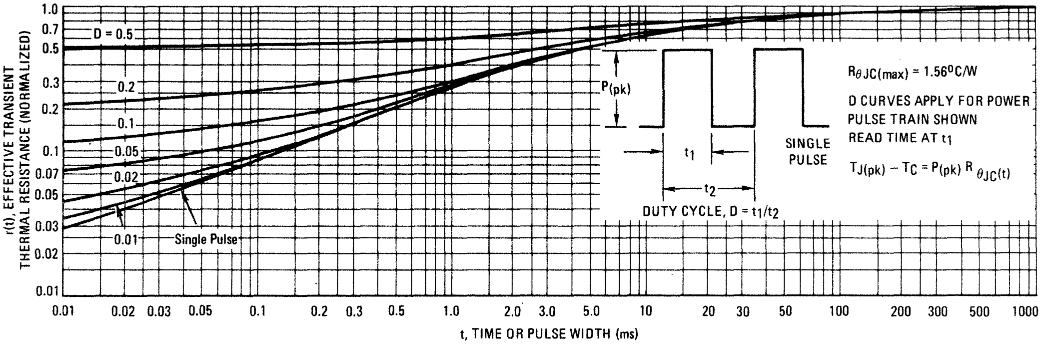
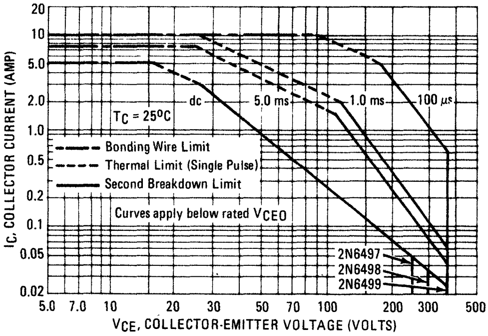


FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 4 may be found at any case temperature by using the appropriate curve on Figure 6.

FIGURE 5 – TURN-OFF TIME

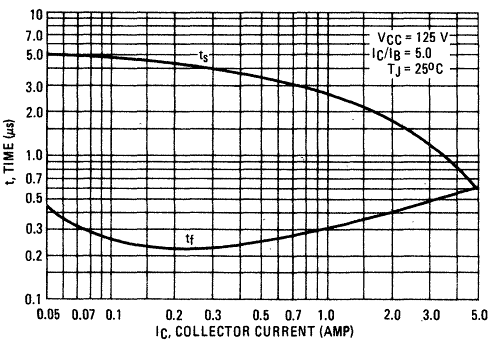


FIGURE 6 – POWER DERATING

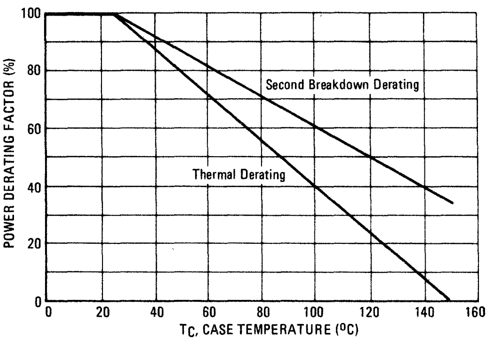


FIGURE 7 – DC CURRENT GAIN

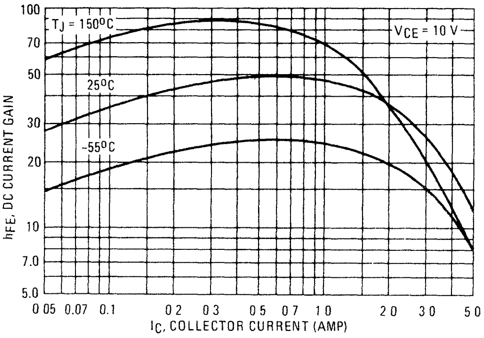


FIGURE 8 – COLLECTOR SATURATION REGION

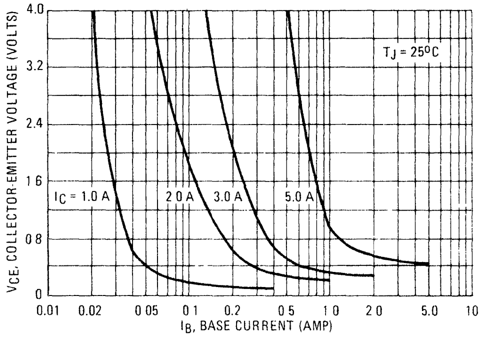


FIGURE 9 – "ON" VOLTAGES

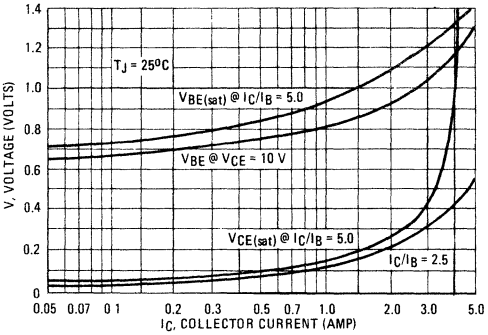


FIGURE 10 – TEMPERATURE COEFFICIENTS

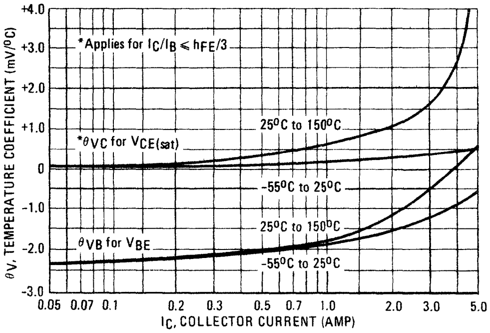


FIGURE 11 – COLLECTOR CUTOFF REGION

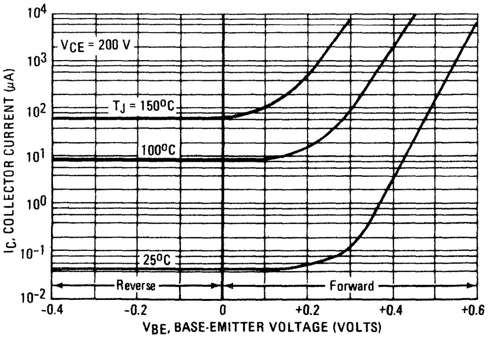
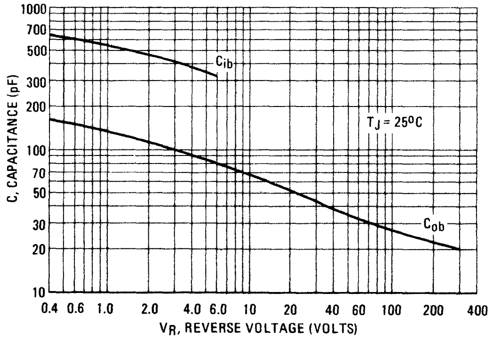
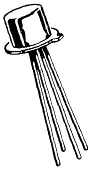


FIGURE 12 – CAPACITANCE

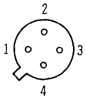


3N124 (SILICON)
3N125
3N126



N-channel silicon annular tetrode-connected field-effect transistors, designed for low-power switching and amplifier applications in the audio through VHF frequency range, features high breakdown voltage, low transfer capacitance, and tetrode configuration for a broad range of applications.

CASE 20
TO-72



STYLE 4
PIN 1. SOURCE
2. GATE
3. DRAIN
4. GATE 2 – SUBSTRATE AND CASE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Gate-Source Voltage			Vdc
Gate 1	V_{G1S}	50	
Gate 2	V_{G2S}	50	
Drain-Source Voltage	V_{DS}	50	Vdc
Drain-Gate Voltage			Vdc
Gate 1	V_{DG1}	50	
Gate 2	V_{DG2}	50	
Gate 1-Gate 2 Current	I_{G1G2}	1.0	mAdc
Gate 2-Gate 1 Current	I_{G2G1}	1.0	mAdc
Gate Current			mAdc
Gate 1	I_{G1}	20	
Gate 2	I_{G2}	20	
Drain Current	I_D	20	mAdc
Junction Operating Temperature	T_J	175	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C
Total Device Dissipation @ $T_A = 25°C$ Derate Above 25°C	P_D	300 1.71	mW mW/°C
Total Device Dissipation @ $T_C = 25°C$ Derate Above 25°C	P_D	800 4.57	mW mW/°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0, V_{G1G2} = 0)	$V_{(BR)GSS}$	50	-	Vdc
Gate Reverse Current (V_{GS} = 25 Vdc, V_{DS} = 0, V_{G1G2} = 0)	I_{GSS}	-	0.250	nAdc
(V_{GS} = 25 Vdc, V_{DS} = 0, V_{G1G2} = 0, T_A = +150°C)		-	250	
Zero-Gate-Voltage Drain Current (V_{DS} = 15 Vdc, V_{G1G2} = 0, V_{GS} = 0) 3N124	I_{DSS}	0.2	2.0	mAdc
3N125		1.5	4.5	
3N126		3.0	9.0	
Gate-Source Voltage (I_D = 20 μAdc, V_{DS} = 15 Vdc, V_{G1G2} = 0) 3N124	V_{GS}	0.2	2.0	Vdc
(I_D = 150 μAdc, V_{DS} = 15 Vdc, V_{G1G2} = 0) 3N125		1.0	3.0	
(I_D = 300 μAdc, V_{DS} = 15 Vdc, V_{G1G2} = 0) 3N126		1.5	5.5	
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc, V_{G1G2} = 0) 3N124	$V_{GS(off)}$	-	-2.5	Vdc
3N125		-	-4.0	
3N126		-	-6.5	
Gate 1-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc, V_{G2S} = 0) 3N124	$V_{G1S(off)}$	-	-5.0	Vdc
3N125		-	-8.0	
3N126		-	-18	
Gate 2-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc, V_{G1S} = 0) 3N124	$V_{G2S(off)}$	-	-8.0	Vdc
3N125		-	-14	
3N126		-	-26	
Gate 1-Gate 2 Reach Through Voltage (I_{G1G2} = 10 μAdc, I_S = 0, I_D = 0) 3N124	V_{G1G2}	1.0	-	Vdc
3N125		3.0	-	
3N126		5.0	-	
Gate 2-Gate 1 Reach Through Voltage (I_{G2G1} = 10 μAdc, I_S = 0, I_D = 0) 3N124	V_{G2G1}	2.0	-	Vdc
3N125		6.0	-	
3N126		10	-	
Gate 1-Gate 2 Reach Through Drain Current (V_{DS} = 15 Vdc, I_{G1} = 10 μAdc, V_{G2S} = 0)	I_D	-	1.0	μAdc
Gate 2-Gate 1 Reach Through Drain Current (V_{DS} = 15 Vdc, I_{G2} = 10 μAdc, V_{G1S} = 0)	I_D	-	1.0	μAdc

SMALL-SIGNAL COMMON-SOURCE CHARACTERISTICS

Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{G1S} = V_{G2S} = 0, f = 1.0 kHz)				μmhos
Gate 1-Gate 2 3N124	$\|y_{fs}\|$	500	2000	
3N125		800	2400	
3N126		1200	3600	
Gate 1 Only 3N124	$\|y_{fs1}\|$	250	1000	
3N125		400	1600	
3N126		600	2700	
Gate 2 Only 3N124	$\|y_{fs2}\|$	200	800	
3N125		250	1000	
3N126		400	1200	
(V_{DS} = 15 Vdc, V_{G1S} = V_{G2S} = 0, f = 100 MHz) Gate 1 Only 3N124	$\|y_{fs1}\|$	250	-	
3N125		400	-	
3N126		600	-	
Output Admittance (V_{DS} = 15 Vdc, V_{G1S} = V_{G2S} = 0, f = 1.0 kHz) 3N124	y_{os}	-	2.0	μmhos
3N125		-	10	
3N126		-	20	
Input Capacitance (V_{DS} = 15 Vdc, V_{G1S} = V_{G2S} = 0, f = 1.0 kHz)				pF
Gate 1-Gate 2	C_{iss}	-	14	
Gate 1 Only	C_{iss1}	-	5.0	
Gate 2 Only	C_{iss2}	-	9.0	
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G1S} = V_{G2S} = 0, f = 1.0 kHz)				pF
Gate 1-Gate 2	C_{rss}	-	2.0	
Gate 1 Only	C_{rss1}	-	0.5	
Gate 2 Only	C_{rss2}	-	1.5	
Spot Noise Figure (V_{DS} = 15 Vdc, V_{G1S} = V_{G2S} = 0, R_S = 1.0 megohm, f = 1.0 kHz, BW = 100 Hz)	NF	-	4.0	dB
		Typ		
Static Drain-Source "ON" Resistance (V_{GS} = 0, V_{DS} = 0) 3N124	$r_{DS(on)}$	1000		ohms
3N125		750		
3N126		500		

FIGURE 1 — DRAIN CURRENT versus GATE SOURCE VOLTAGE

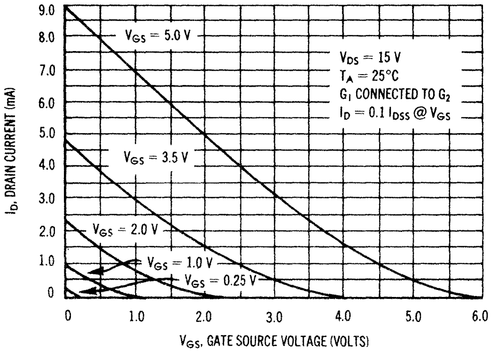


FIGURE 2 — PARAMETER INTER-RELATIONSHIPS

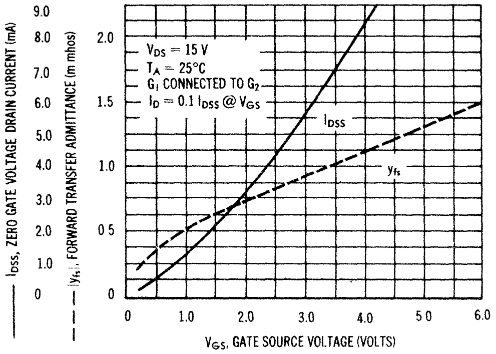


FIGURE 3 — FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

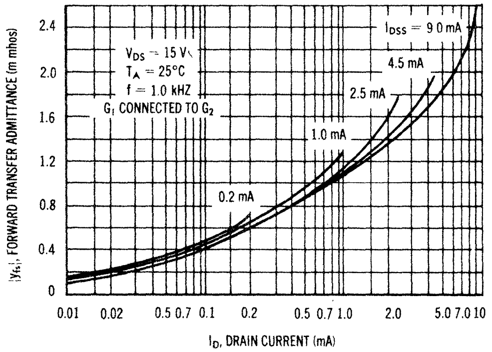
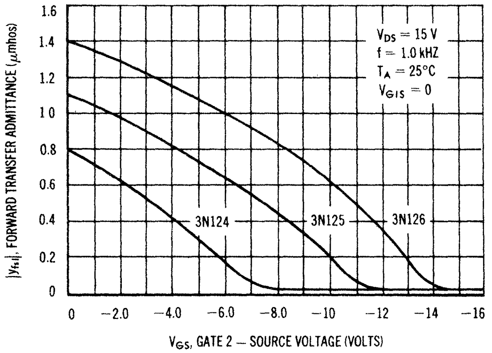


FIGURE 4 GATE 1 — FORWARD TRANSFER ADMITTANCE versus GATE 2 — SOURCE VOLTAGE



NOISE CHARACTERISTICS

V_{DS} = 15 Vdc, I_D = I_{DSS}, T_A = 25°C
GATE 1 CONNECTED TO GATE 2

FIGURE 5A — FREQUENCY VARIATIONS

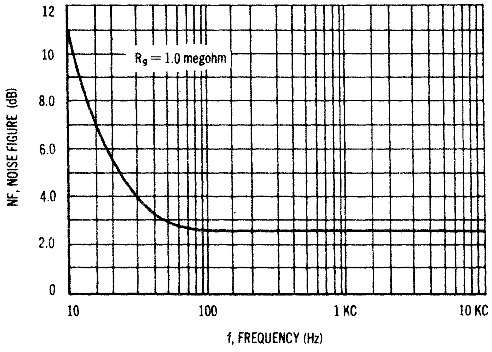
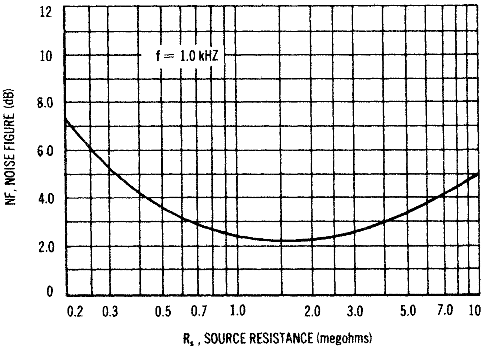


FIGURE 5B — SOURCE RESISTANCE VARIATIONS



HIGH FREQUENCY y PARAMETER CHARACTERISTICS

$V_{DS} = 15$ Vdc, $V_{GS} = 0$, $T_A = 25°C$ — GATE 2 CONNECTED TO SOURCE

FIGURE 6 — INPUT ADMITTANCE

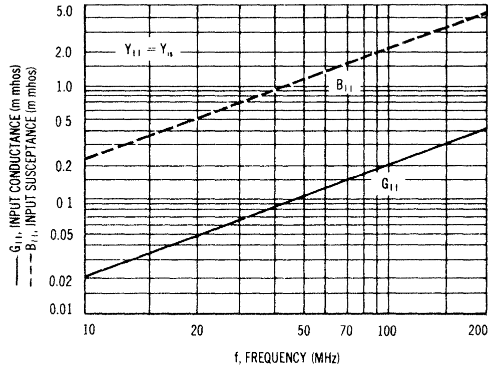


FIGURE 7 — REVERSE TRANSFER ADMITTANCE

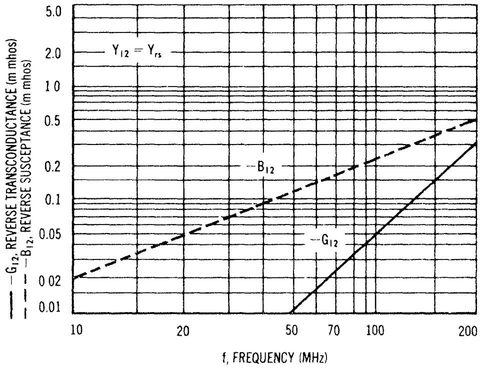


FIGURE 8 — FORWARD TRANSFER ADMITTANCE

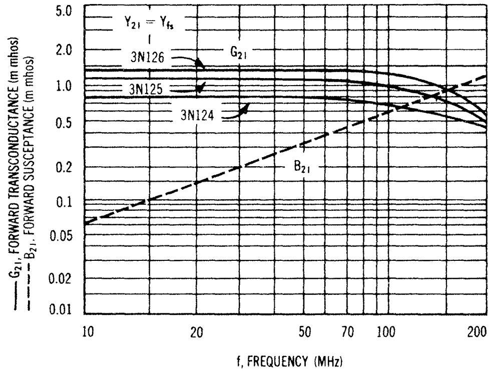
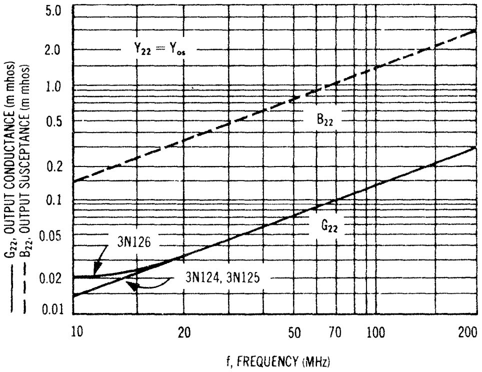
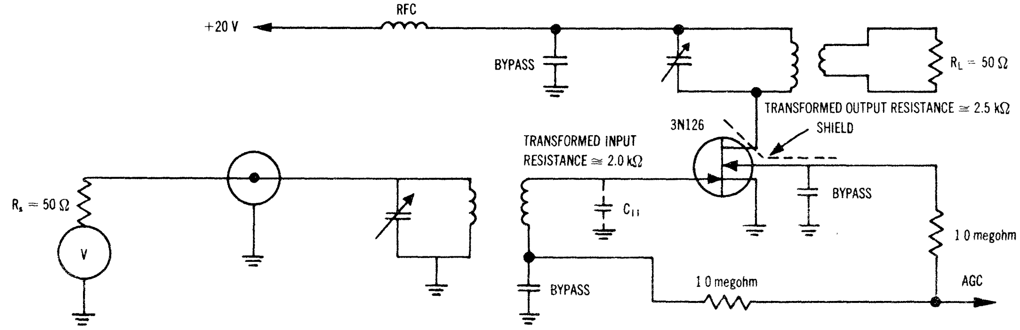


FIGURE 9 — OUTPUT ADMITTANCE



TYPICAL PERFORMANCE USING THE 3N126



CIRCUIT POWER GAIN = 8 0 dB* TYPICAL AT 105 MHz (AGC = 0V)

*Includes circuit losses.

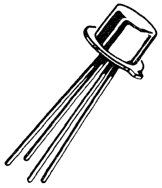
3N128 (SILICON)

SILICON N-CHANNEL MOS FIELD-EFFECT TRANSISTOR

. . . designed for VHF amplifier and oscillator applications in communications equipment.

- High Forward Transadmittance –
  $|y_{fs}| = 5000\ \mu$mhos (Min) @ f = 1.0 kHz
- Low Input Capacitance –
  $C_{iss} = 7.0$ pF (Max) @ f = 1.0 MHz
- Low Noise Figure –
  NF = 5.0 dB (Max) @ f = 200 MHz
- High Power Gain –
  $P_G = 13.5$ dB (Min) @ f = 200 MHz
- Complete "y" Parameter Curves
- Third Order Intermodulation Distortion Performance Curve Provided

N-CHANNEL MOS FIELD-EFFECT TRANSISTOR



* MAXIMUM RATINGS

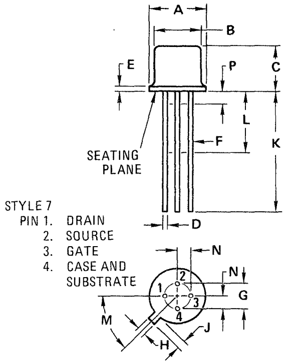
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	+20	Vdc
Drain-Gate Voltage	V_{DG}	+20	Vdc
Gate-Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	50	mAdc
Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	330 2.2	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175	°C

*Indicates JEDEC Registered Data.

HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.



STYLE 7
PIN 1. DRAIN
2. SOURCE
3. GATE
4. CASE AND SUBSTRATE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Source Breakdown Voltage (I_G = -10 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	-50	—	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 50 μAdc)	$V_{GS(off)}$	-0.5	-8.0	Vdc
Gate Reverse Current	I_{GSS}			nAdc
(V_{GS} = -8.0 Vdc, V_{DS} = 0)		—	0.05	
(V_{GS} = -8.0 Vdc, V_{DS} = 0, T_A = 125°C)		—	5.0	
ON CHARACTERISTICS				
Zero-Gate-Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	5.0	25	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transadmittance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 1.0 kHz)	$\lvert y_{fs} \rvert$	5000	12,000	μmhos
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 200 MHz)	$Re(y_{fs})$	5000	—	μmhos
Output Conductance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 200 MHz)	$Re(y_{os})$	—	500	μmhos
Input Conductance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 200 MHz)	$Re(y_{is})$	—	800	μmhos
Input Capacitance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 1.0 MHz)	C_{iss}	—	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 1.0 MHz)	C_{rss}	—	0.28	pF
Noise Figure (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 200 MHz)	NF	—	5.0	dB
Power Gain (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 200 MHz)	P_G	13.5	—	dB

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

TYPICAL CHARACTERISTICS

(T_A = 25°C)

FIGURE 1 — DRAIN CHARACTERISTICS

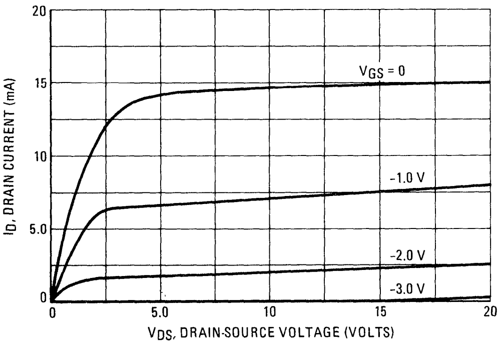
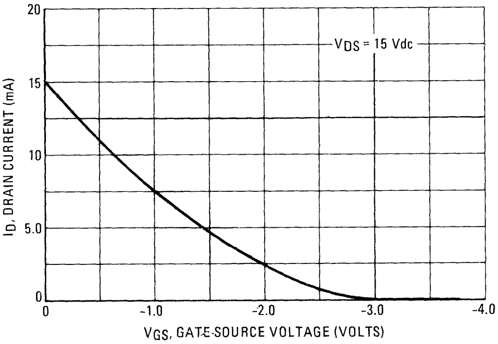


FIGURE 2 — TRANSFER CHARACTERISTICS



TYPICAL 1 kHz DRAIN CHARACTERISTICS

($T_A = 25^oC$, V_{DS} = 15 Vdc, f = 1.0 kHz)

FIGURE 3 – FORWARD TRANSADMITTANCE versus GATE BIAS VOLTAGE

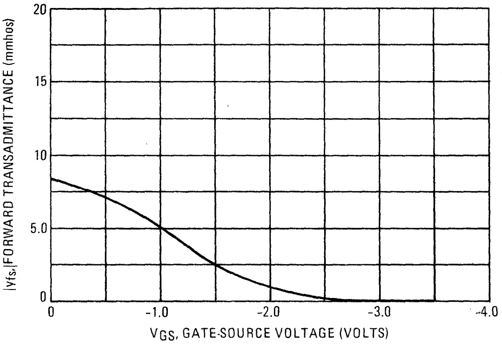
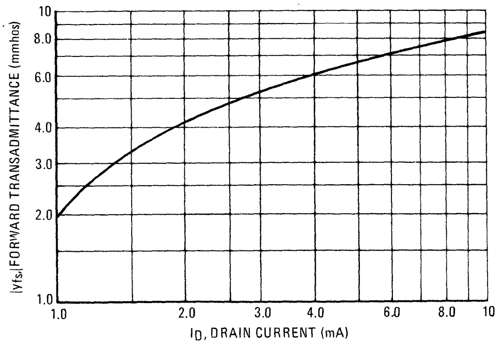


FIGURE 4 – FORWARD TRANSADMITTANCE versus DRAIN CURRENT



TYPICAL 200 MHz COMMON-SOURCE ADMITTANCE CHARACTERISTICS

($T_A = 25^oC$, V_{DS} = 15 Vdc, f = 200 MHz)

FIGURE 5 – INPUT ADMITTANCE (y_{is}) COMPONENTS

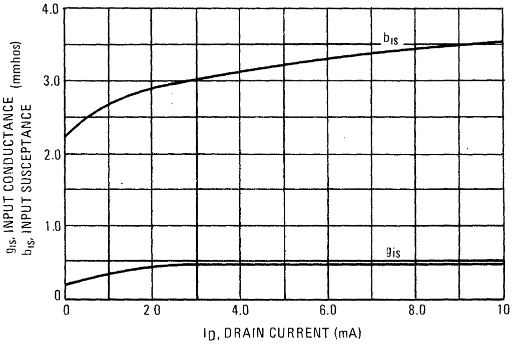


FIGURE 6 – FORWARD TRANSADMITTANCE (y_{fs}) COMPONENTS

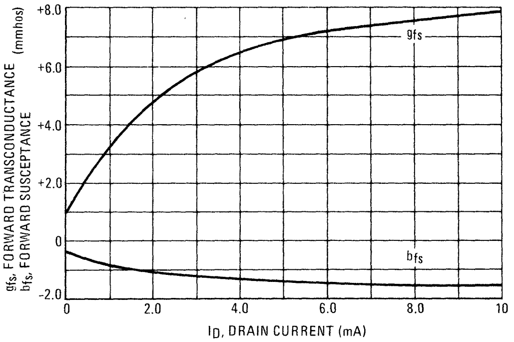


FIGURE 7 – REVERSE TRANSADMITTANCE (y_{rs}) COMPONENTS

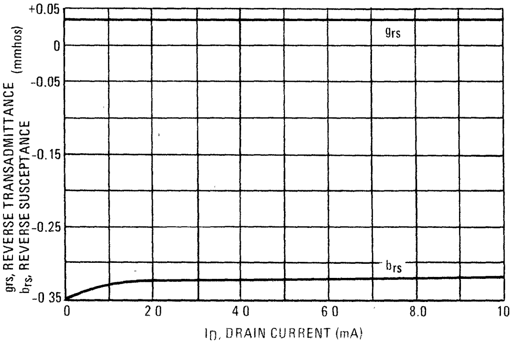


FIGURE 8 – OUTPUT ADMITTANCE (y_{os}) COMPONENTS

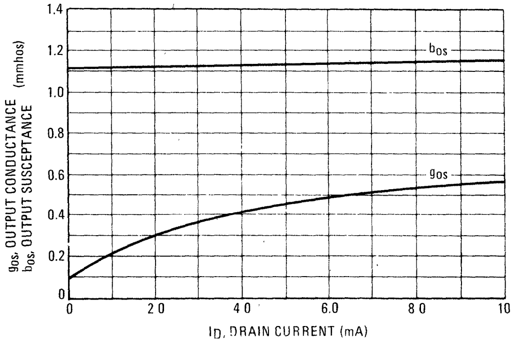


FIGURE 9 – POWER GAIN AND NOISE FIGURE versus DRAIN CURRENT

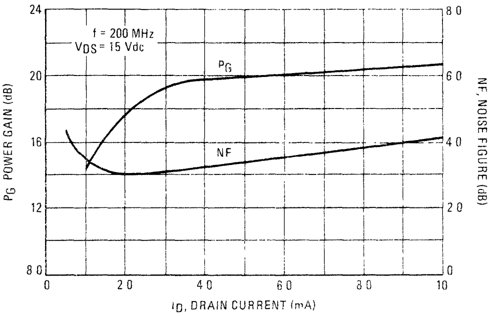


FIGURE 10 – POWER GAIN AND NOISE FIGURE versus DRAIN VOLTAGE

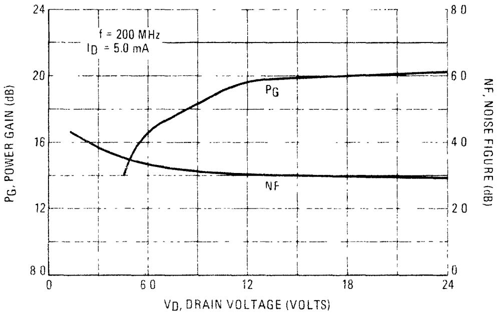


FIGURE 11 – THIRD ORDER INTERMODULATION DISTORTION

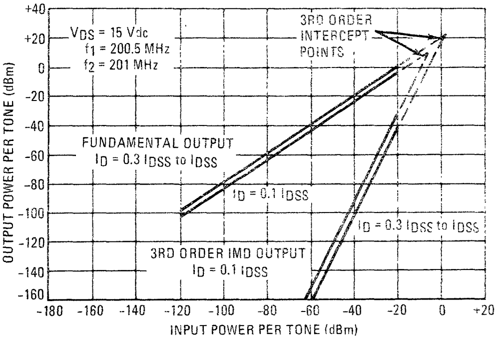
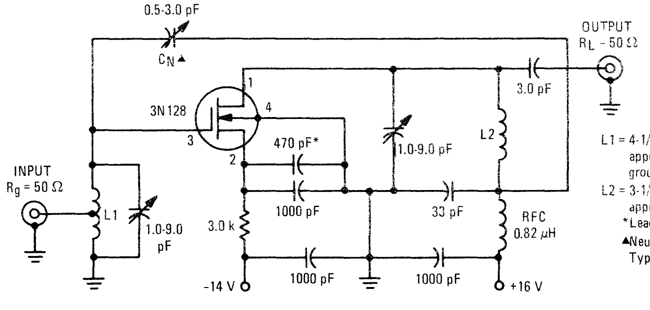


Figure 11 shows the typical third order intermodulation distortion (IMD) performance of the 3N128 at 200 MHz.

Both fundamental output and third order IMD output characteristics are plotted. The curves have been extrapolated to show the third order intermodulation output intercept point.

Performance for drain currents from I_{DSS} to $0.1\ I_{DSS}$, is given. The power gain and noise figure test amplifier shown in Figure 12 was used to generate the IMD data.

FIGURE 12 – POWER GAIN, NOISE FIGURE AND INTERMODULATION DISTORTION TEST CIRCUIT



L1 = 4-1/2 turns #20 AWG wire, 3/16" diameter, approximately 1/2" long, tapped 1 turn from ground end.
L2 = 3-1/2 turns #20 AWG wire, 3/8" diameter, approximately 1/2" long
*Leadless-type disc capacitor
▲Neutralization fixed for a Transistor having a Typical value of C_{rss} (0.13 pF)

3N140 (SILICON)

N-CHANNEL DUAL-GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTOR

Depletion mode (Type B) dual-gate transistor designed for VHF amplifier and mixer applications.

- Silicon-Nitride Passivation for Excellent Long Term Stability
- High Common-Source Power Gain – G_{ps} = 16 dB (Min) @ f = 200 MHz
- Low Reverse Transfer Capacitance – C_{rss} = 0.02 pF (Typ) @ V_{DS} = 13 Vdc

N-CHANNEL DUAL-GATE MOS FIELD-EFFECT TRANSISTOR

Type B

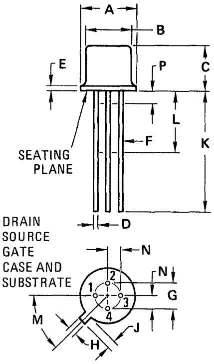
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	0 to +20	Vdc
Drain-Gate 1 Voltage	V_{DG1}	20	Vdc
Drain-Gate 2 Voltage	V_{DG2}	20	Vdc
Reverse Gate 1-Source Voltage	$V_{GS1(r)}$	-8.0	Vdc
Reverse Gate 2-Source Voltage	$V_{GS2(r)}$	-8.0 to 0.4 V_{DS}	Vdc
Forward Gate 1-Source Voltage	$V_{GS1(f)}$	+1.0	Vdc
Forward Gate 2-Source Voltage	$V_{GS2(f)}$	0.4 V_{DS}	Vdc
Drain Current	I_D	50	mAdc
Total Device Dissipation @T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175	°C

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. **To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.**
2. **Avoid unnecessary handling. Pick up devices by the case instead of the leads.**
3. **Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.**



STYLE 7
PIN 1. DRAIN
2. SOURCE
3. GATE
4. CASE AND SUBSTRATE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

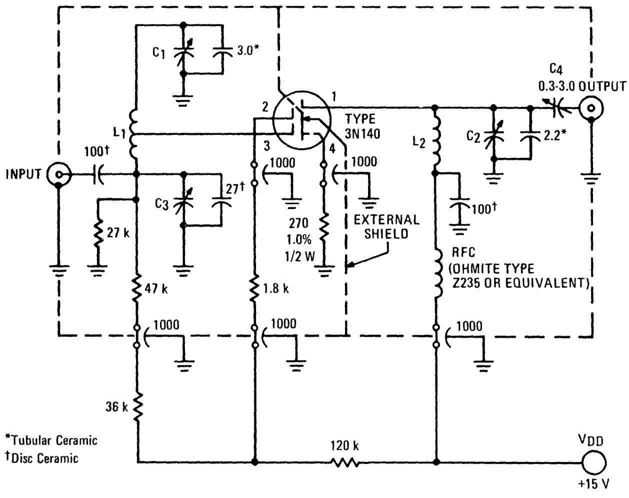
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate 1-Source Cutoff Voltage (V_{DS} = +16 Vdc, I_D = 200 μAdc, V_{G2S} = +4.0 Vdc)	$V_{G1S(off)}$	-0.5	-4.0	Vdc
Gate 2-Source Cutoff Voltage (V_{DS} = +16 Vdc, I_D = 200 μAdc, V_{G1S} = 0)	$V_{G2S(off)}$	-0.5	-4.0	Vdc
Gate 1-Reverse Current (V_{G1S} = 20 Vdc, V_{G2S} = 0, V_{DS} = 0)	I_{G1SS}	-	1.0	nAdc
(V_{G1S} = 20 Vdc, V_{DS} = 0, V_{G2S} = 0, T_A = 125°C)		-	0.2	μAdc
Gate 2-Reverse Current (V_{G2S} = 20 Vdc, V_{G1S} = 0, V_{DS} = 0)	I_{G2SS}	-	1.0	nAdc
(V_{G2S} = 20 Vdc, V_{DS} = 0, V_{G1S} = 0, T_A = 125°C)		-	0.2	μAdc
ON CHARACTERISTICS				
Zero-Gate Voltage Drain Current (V_{DD} = +14 Vdc, V_{G1S} = 0, V_{G2S} = +14 Vdc)	I_{DSS}	5.0	30	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transconductance (V_{DD} = +14 Vdc, I_D = 10 mAdc, V_{G2S} = +4.0 Vdc, f = 1.0 kHz)	$Re(y_{fs})$**	6000	18,000	μmhos
Input Capacitance (V_{DS} = +13 Vdc, I_D = 10 mAdc, V_{G2S} = +4.0 Vdc, f = 1.0 MHz)	C_{iss}	3.0	7.0	pF
Reverse Transfer Capacitance (V_{DS} = +13 Vdc, I_D = 10 mAdc, V_{G2S} = +4.0 Vdc, f = 1.0 MHz)	C_{rss}*	0.01	0.03	pF
Common-Source Noise Figure (See Figure 1) (V_{DD} = +15 Vdc, R_S = 275 Ohms, R_G = 50 Ohms, f = 200 MHz)	NF	-	4.5	dB
Power Gain (See Figure 1) (f = 200 MHz)	G_{ps}	16	22	dB
Bandwidth (See Figure 1) (f = 200 MHz)	BW	9.5	14.5	MHz

*Drain-to-Gate 1

**Gate 1-to-Drain

FIGURE 1 — 200 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT



*Tubular Ceramic
†Disc Ceramic

C_1, C_2: 1.5-5.0 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

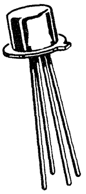
C_3: 1.0-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3.0 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.

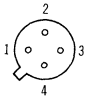
L_1: 5 turns silver-plated 0.02" thick, 0.07" – 0.03" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

3N155,A (SILICON)
3N156,A



P-channel silicon nitride passivated MOS field-effect enhancement mode transistors designed for chopper and switching application.



CASE 20
(TO-72)

STYLE 2
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SUBSTRATE AND CASE LEAD

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	35	Vdc
Drain-Gate Voltage	V_{DG}	35	Vdc
Gate-Source Voltage	V_{GS}	50	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.7	mW mW/°C
Operating Junction Temperature Range	T_J	-65 to +175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (I_D = -10 µAdc, V_G = V_S = 0)		$V_{(BR)DSS}$	35	-	-	Vdc
Gate Reverse Current (V_{GS} = +50 Vdc, V_{DS} = 0) (V_{GS} = +25 Vdc, V_{DS} = 0)		I_{GSS}	- -	- -	1000 10	pAdc
Zero-Gate Voltage Drain Current (V_{DS} = -10 Vdc, V_{GS} = 0)	3N155, 3N156 3N155A, 3N156A	I_{DSS}	- -	- -	1.0 0.25	nAdc
(V_{DS} = -10 Vdc, V_{GS} = 0, T_A = 125°C)	3N155, 3N156 3N155A, 3N156A		- -	- -	1000 250	
Resistance Drain Source (I_D = 0, V_{GS} = 0)		$R_{DS(off)}$	$1 \times 10^{+10}$	-	-	Ohms
Resistance Gate Source Input (V_{GS} = -25 Vdc)		R_{GS}	-	$1 \times 10^{+16}$	-	Ohms
ON CHARACTERISTICS						
Gate Source Threshold Voltage (V_{DS} = -10 Vdc, I_D = -10 µAdc)	3N155, 3N155A 3N156, 3N156A	$V_{GS(TH)}$	1.5 3.0	- -	3.2 5.0	Vdc
Drain Source "ON" Voltage (I_D = -2.0 mAdc, V_{GS} = -10 Vdc)		$V_{DS(on)}$	-	-	-1.0	Vdc
Gate Forward Leakage Current (V_{GS} = -50 Vdc, V_{DS} = 0) (V_{GS} = -25 Vdc, V_{DS} = 0)		$I_{G(f)}$	- -	- -	1000 10	pAdc
"ON" Drain Current (V_{DS} = -15 Vdc, V_{GS} = -10 Vdc)		$I_{D(on)}$	5.0	-	-	mAdc
Static Drain-Source "ON" Resistance (I_D = 0 mAdc, V_{GS} = -10 Vdc)	3N155, 3N156 3N155A, 3N156A	$r_{DS(on)}$	- -	- -	600 300	Ohms
SMALL-SIGNAL CHARACTERISTICS						
Drain-Source Resistance (V_{GS} = -10 Vdc, I_D = 0, f = 1.0 kHz)	3N155, 3N156 3N155A, 3N156A	$r_{ds(on)}$	- -	- -	600 300	Ohms
(V_{GS} = -15 Vdc, I_D = 0, f = 1.0 kHz)	3N155, 3N156 3N155A, 3N156A		- -	- -	500 250	
Forward Transfer Admittance (V_{DS} = -15 Vdc, I_D = -2.0 mAdc, f = 1.0 kHz)		$\lvert y_{fs} \rvert$	1000	-	4000	µmhos
Input Capacitance (V_{DS} = -15 Vdc, V_{GS} = -10 Vdc, f = 140 kHz)		C_{iss}	-	-	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)		C_{rss}	-	-	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = -10 Vdc, f = 140 kHz)		$C_{d(sub)}$	4.0	-	-	pF
SWITCHING CHARACTERISTICS						
Turn-On Delay	(V_{DD} = -10 Vdc, $I_{D(on)}$ = -2.0 mAdc, $V_{GS(on)}$ = -10 Vdc, $V_{GS(off)}$ = 0) Test Circuit given in Figure 1	t_d	-	-	45	µs
Rise Time		t_r	-	-	65	ns
Turn-Off Delay		t_s	-	-	60	ns
Fall Time		t_f	-	-	100	ns

FIGURE 1 – GATE VOLTAGE EFFECTS

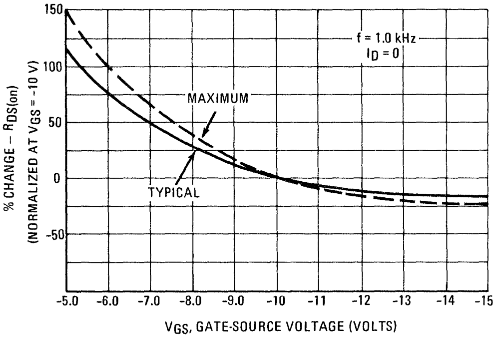


FIGURE 2 – TEMPERATURE EFFECTS

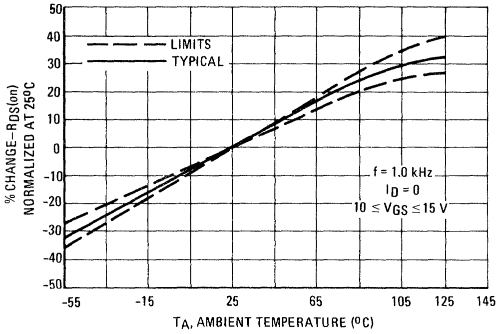


FIGURE 3 – DRAIN CURRENT versus TEMPERATURE

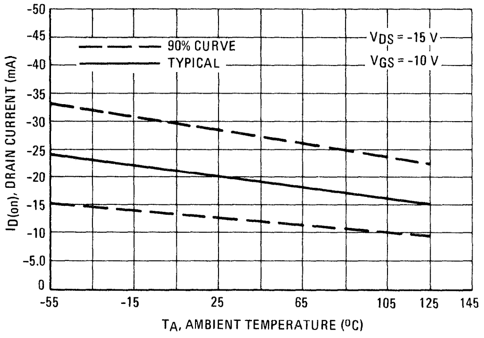


FIGURE 4 – "ON" DRAIN-SOURCE VOLTAGE

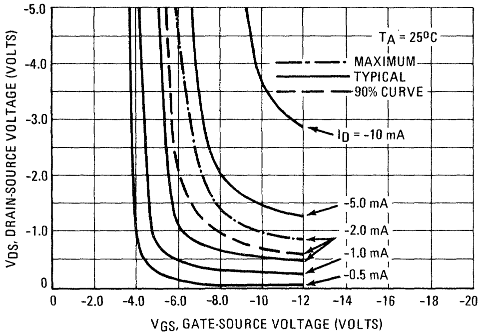


FIGURE 5 – LEAKAGE CURRENTS

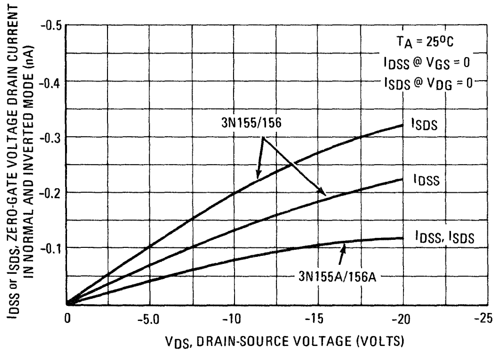
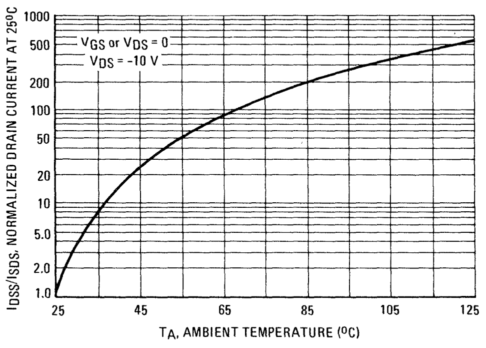


FIGURE 6 – LEAKAGE CURRENT versus TEMPERATURE



SWITCHING CHARACTERISTICS

$T_A = 25^\circ C$

FIGURE 7 – TURN-ON DELAY TIME

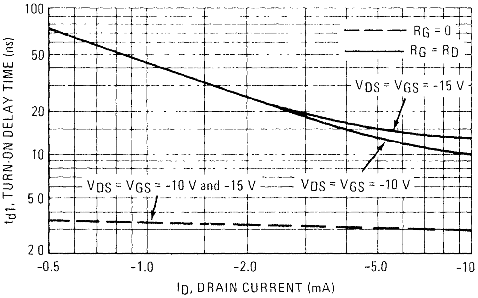


FIGURE 8 – RISE TIME

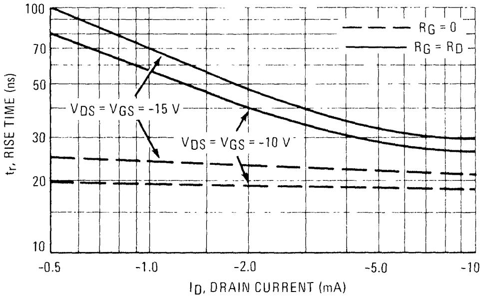


FIGURE 9 – TURN-OFF DELAY TIME

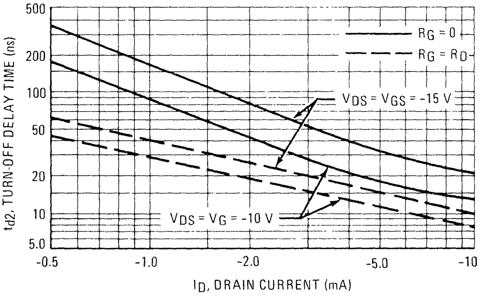


FIGURE 10 – FALL TIME

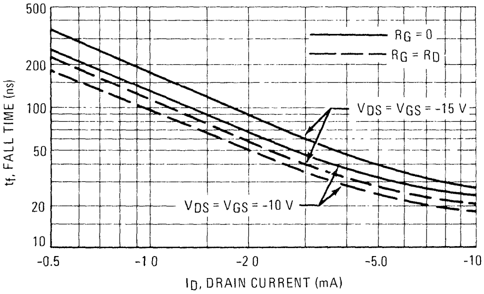
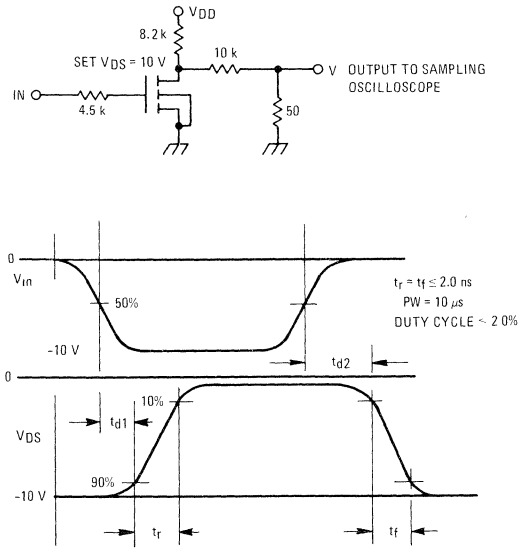


FIGURE 11 – SWITCHING CIRCUIT and WAVEFORMS



The switching characteristics shown above were measured in a test circuit similar to Figure 11. At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance ($C_{gs} = C_{iss} - C_{rss}$) has no charge. The drain voltage is at V_{DD}, and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

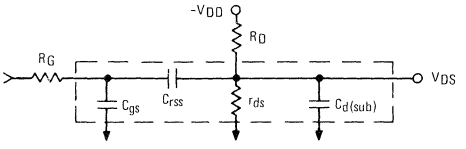
During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_G (generator impedance) (Figure 12). C_{rss} must be discharged to $V_{GS} - V_{D(on)}$ through R_G and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with d_s. During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 4) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

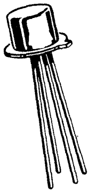
If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_G = 0$ and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with $R_G = R_D$ simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_G = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.

FIGURE 12 – SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL

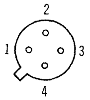


3N157,A (SILICON)
3N158,A



CASE 20
(TO-72)

P-channel silicon nitride passivated MOS field-effect enhancement mode transistors designed for chopper and switching application.



STYLE 2
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SUBSTRATE AND CASE LEAD

MAXIMUM RATINGS

Rating	Symbol	3N157 3N158	3N157A 3N158A	Unit
Drain-Source Voltage	V_{DS}	35	50	Vdc
Drain-Gate Voltage	V_{DG}	35	50	Vdc
Gate-Source Voltage	V_{GS}	50		Vdc
Drain Current	I_D	30		mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.7		mW mW/°C
Operating Junction Temperature Range	T_J	-65 to +175		°C
Storage Temperature Range	T_{stg}	-65 to +200		°C

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

3N157,A, 3N158,A (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = -10 μAdc, $V_G = V_S = 0$) 3N157, 3N158 3N157A, 3N158A	$V_{(BR)DSS}$	35 50	- -	- -	Vdc
Gate Reverse Current (V_{GS} = +25 Vdc, V_{DS} = 0)	I_{GSS}	-	-	10	pAdc
Zero-Gate Voltage Drain Current (V_{DS} = -15 Vdc, V_{GS} = 0) 3N157, 3N158 3N157A, 3N158A	I_{DSS}	- -	- -	1.0 0.25	nAdc
(V_{DS} = -35 Vdc, V_{GS} = 0) 3N157, 3N158		-	-	10	μAdc
(V_{DS} = -50 Vdc, V_{GS} = 0) 3N157A, 3N158A		-	-	10	
Input Resistance (V_{GS} = -25 Vdc)	R_{GS}	-	$1 \times 10^{+12}$	-	Ohms
ON CHARACTERISTICS					
Gate-Source Threshold Voltage (V_{DS} = -15 Vdc, I_D = -10 μAdc) 3N157, 3N157A 3N158, 3N158A	$V_{GS(TH)}$	1.5 3.0	- -	3.2 5.0	Vdc
Gate-Source Voltage (V_{DS} = -15 Vdc, I_D = -0.5 mAdc) 3N157, 3N157A 3N158, 3N158A	V_{GS}	1.5 3.0	- -	5.5 7.0	Vdc
Gate Forward Current (V_{GS} = -25 Vdc, V_{DS} = 0)	$I_{G(f)}$	-	-	10	pAdc
(V_{GS} = -25 Vdc, V_{DS} = 0, T_A = +55°C)		-	-	10	nAdc
"ON" Drain Current (V_{DS} = -15 Vdc, V_{GS} = -10 Vdc)	$I_{D(on)}$	5.0	-	-	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance (V_{DS} = -15 Vdc, I_D = -2.0 mAdc, f = 1.0 kHz)	$\|y_{fs}\|$	1000	-	4000	μmhos
(V_{DS} = -15 Vdc, V_{GS} = -15 Vdc, f = 1.0 kHz)		1800	-	-	
Output Admittance (V_{DS} = -15 Vdc, I_D = -2.0 mAdc, f = 1.0 kHz)	$\|y_{os}\|$	-	-	60	μmhos
Input Capacitance (V_{DS} = -15 Vdc, V_{GS} = 0, f = 140 kHz)	C_{iss}	-	-	5.0	pF
Reverse Transfer Capacitance (V_{DS} = -15 Vdc, V_{GS} = 0, f = 140 kHz)	C_{rss}	-	-	1.3	pF
Drain-Substrate Capacitance ($V_{D(sub)}$ = -10 Vdc, f = 140 kHz)	$C_{d(sub)}$	-	-	4.0	pF
Noise Voltage (R_S = 0, BW = 1.0 Hz, V_{DS} = -15 Vdc, I_D = -2.0 mAdc, f = 100 Hz)	e_n	-	300	-	NV/$\sqrt{\text{Hz}}$
(R_S = 0, BW = 1.0 Hz, V_{DS} = -15 Vdc, I_D = -2.0 mAdc, f = 1.0 kHz)		-	120	500	

FIGURE 1 – FORWARD TRANSCONDUCTANCE

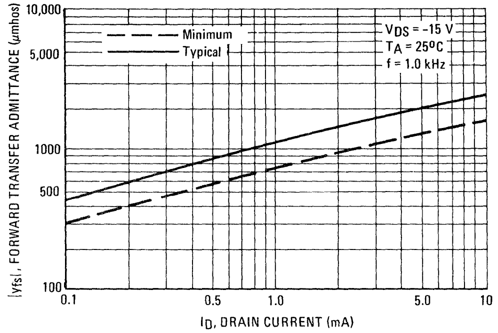


FIGURE 2 – OUTPUT TRANSCONDUCTANCE

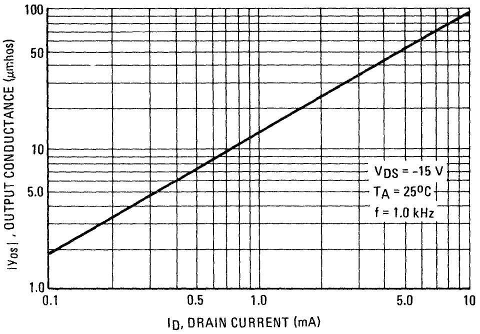


FIGURE 3 – FORWARD TRANSCONDUCTANCE versus TEMPERATURE

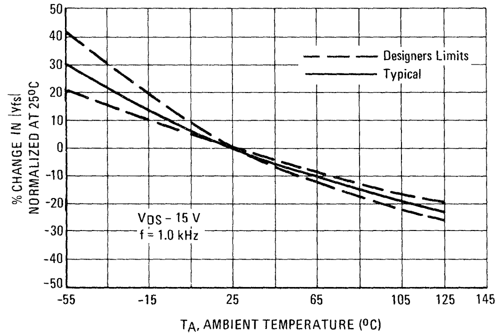


FIGURE 4 – BIAS CURVE

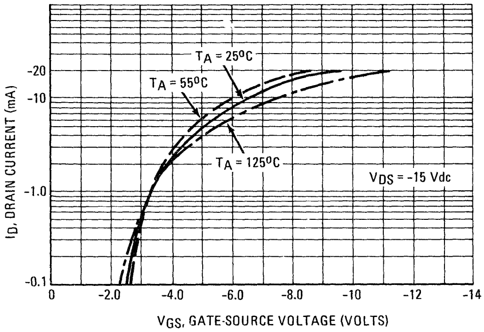


FIGURE 5 – "ON" DRAIN-SOURCE VOLTAGE

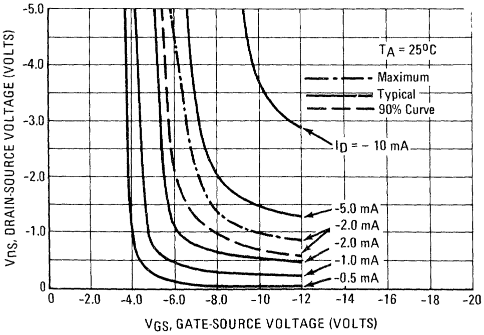
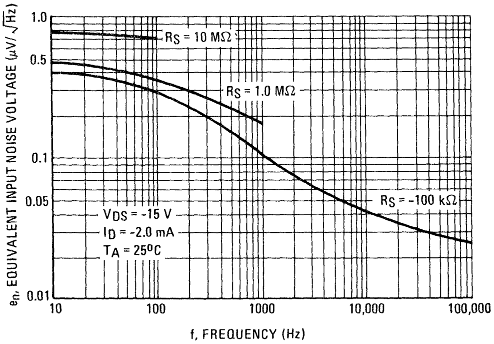


FIGURE 6 – EQUIVALENT INPUT NOISE VOLTAGE



SWITCHING CHARACTERISTICS

($T_A = 25^\circ C$)

FIGURE 7. – TURN-ON DELAY TIME

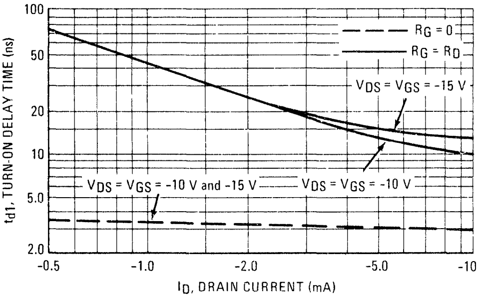


FIGURE 8 – RISE TIME

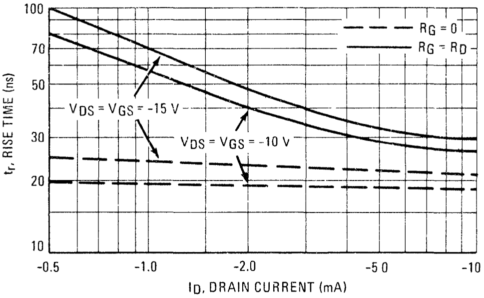


FIGURE 9 – TURN-OFF DELAY TIME

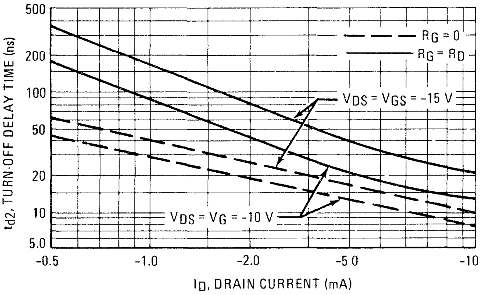


FIGURE 10 – FALL TIME

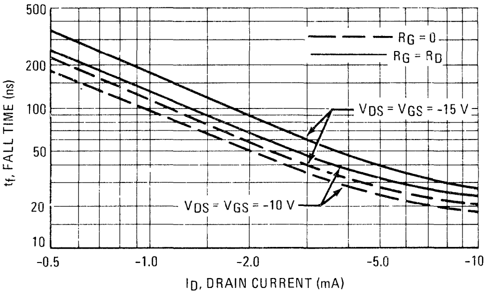
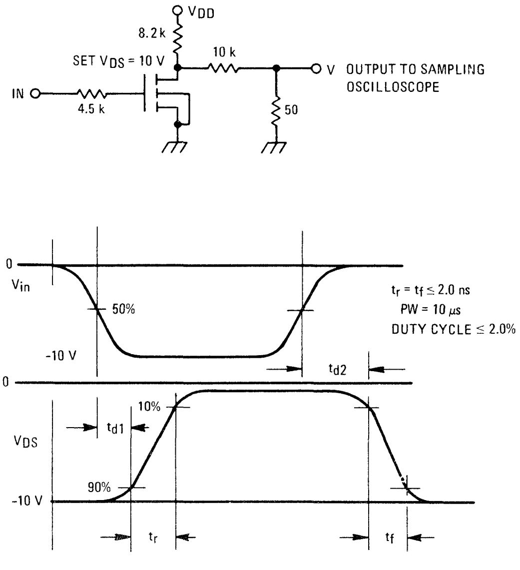


FIGURE 11 – SWITCHING CIRCUIT and WAVEFORMS



The switching characteristics shown above were measured in a test circuit similar to Figure 11 At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance ($C_{gs} = C_{iss} - C_{rss}$) has no charge. The drain voltage is at V_{DD}, and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

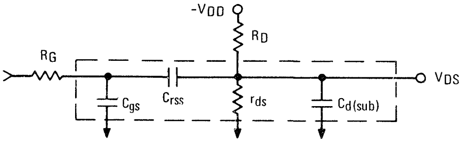
During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_G (generator impedance) (Figure 12). C_{rss} must be discharged to $V_{GS} - V_{D(on)}$ through R_G and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with r_{ds}. During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 5) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_G = 0$ and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with $R_G = R_D$ simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_G = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.

FIGURE 12 – SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL



3N169 (SILICON)
3N170
3N171

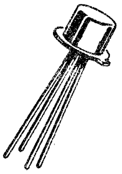
SILICON N-CHANNEL
MOS FIELD-EFFECT TRANSISTORS

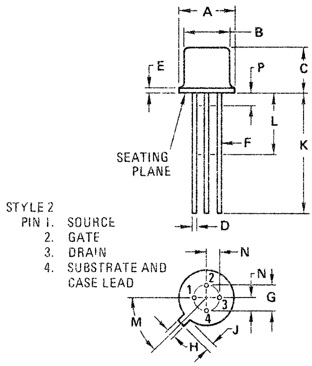
Enhancement Mode transistors designed for low-power switching applications.

- Low Switching Voltages – $V_{GS(th)} \leqslant 3.0$ Vdc
- Fast Switching Times — $t_r \leqslant 10$ ns
- Low Drain-Source Resistance $r_{ds(on)}$ = 200 Ohms (Max)
- Low Reverse Transfer Capacitance C_{rss} = 1.3 pF (Max)
- Manufactured Using the New Silicon Nitride Process Resulting in a Stable $V_{GS(th)}$ and Gate Oxide Breakdown Protection to Typical Transients of ±150 Volts Peak

MOS FIELD-EFFECT TRANSISTORS

N-CHANNEL





STYLE 2
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SUBSTRATE AND CASE LEAD

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	-	1.27	-	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
*Drain-Source Voltage	V_{DS}	25	Vdc
*Drain-Gate Voltage	V_{DG}	±35	Vdc
*Gate-Source Voltage	V_{GS}	±35	Vdc
*Drain Current	I_D	30	mAdc
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW/°C
*Power Dissipation @ T_C = 25°C *Derate above 25°C	P_D	800 4.56	mW mW/°C
Operating Junction Temperature	T_J	175	°C
*Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise noted)

Substrate connected to source.

Characteristic	Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_{GS} = 0)	–	$V_{(BR)DSS}$	25	–	Vdc
*Gate Leakage Current (V_{GS} = −35 Vdc, V_{DS} = 0) (V_{GS} = −35 Vdc, V_{DS} = 0, T_A = 125°C)	–	I_{GSS}	 – –	 10 100	pAdc
*Zero-Gate-Voltage Drain Current (V_{DS} = 10 Vdc, V_{GS} = 0) (V_{DS} = 10 Vdc, V_{GS} = 0, T_A = 125°C)	–	I_{DSS}	 – –	 10 1.0	nAdc μAdc
***ON CHARACTERISTICS**					
Gate-Source Threshold Voltage 3N169 (V_{DS} = 10 Vdc, I_D = 10 μAdc) 3N170 3N171	–	$V_{GS(th)}$	0.5 1.0 1.5	1.5 2.0 3.0	Vdc
"ON" Drain Current (V_{GS} = 10 Vdc, V_{DS} = 10 Vdc)	3	$I_{D(on)}$	10	–	mAdc
Drain-Source "ON" Voltage (I_D = 10 mAdc, V_{GS} = 10 Vdc)	–	$V_{DS(on)}$	–	2.0	Vdc
SMALL SIGNAL CHARACTERISTICS					
*Drain-Source Resistance (V_{GS} = 10 Vdc, I_D = 0, f = 1.0 kHz)	4	$r_{ds(on)}$	–	200	Ohms
Forward Transfer Admittance (V_{DS} = 10 Vdc, I_D = 2.0 mAdc, f = 1.0 kHz)	1	$\lvert y_{fs} \rvert$	1000	–	μmhos
*Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 1.0 MHz)	2	C_{rss}	–	1.3	pF
*Input Capacitance (V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 MHz)	2	C_{iss}	–	5.0	pF
*Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 Vdc, f = 1.0 MHz)	–	$C_{d(sub)}$	–	5.0	pF

***SWITCHING CHARACTERISTICS**

Characteristic	Conditions	Figure No.	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 10 Vdc, $I_{D(on)}$ = 10 mAdc, $V_{GS(on)}$ = 10 Vdc, $V_{GS(off)}$ = 0, R_G' = 50 Ohms)	6,10	$t_{d(on)}$	–	3.0	ns
Rise Time		7,10	t_r	–	10	ns
Turn-Off Delay Time		8,10	$t_{d(off)}$	–	3.0	ns
Fall Time		9,10	t_f	–	15	ns

*Indicates JEDEC Registered Data.

FIGURE 1 – FORWARD TRANSFER ADMITTANCE

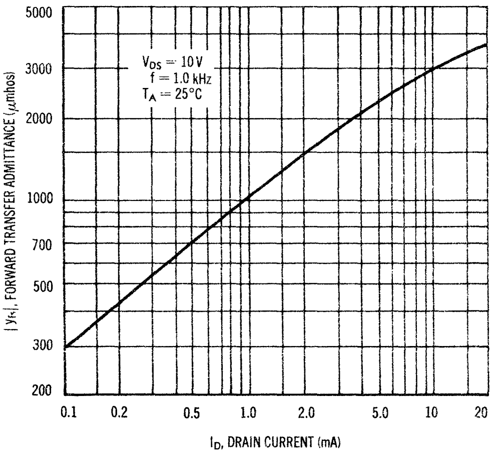


FIGURE 2 – CAPACITANCE

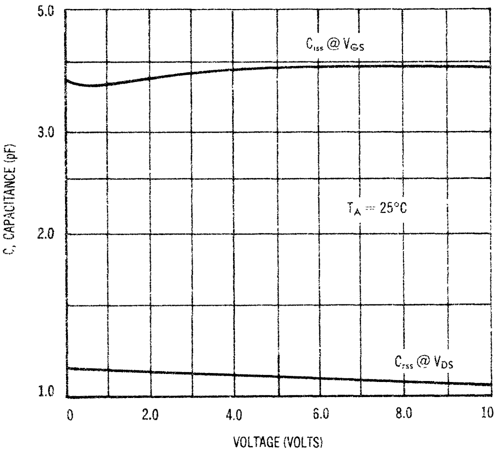


FIGURE 3 – TRANSFER CHARACTERISTICS

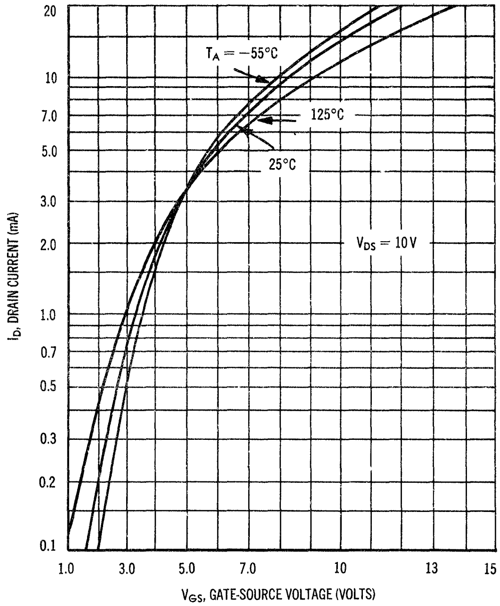


FIGURE 4 – DRAIN-SOURCE "ON" RESISTANCE

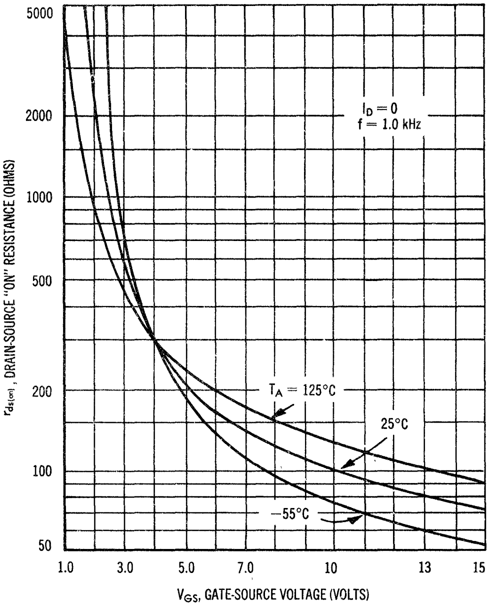
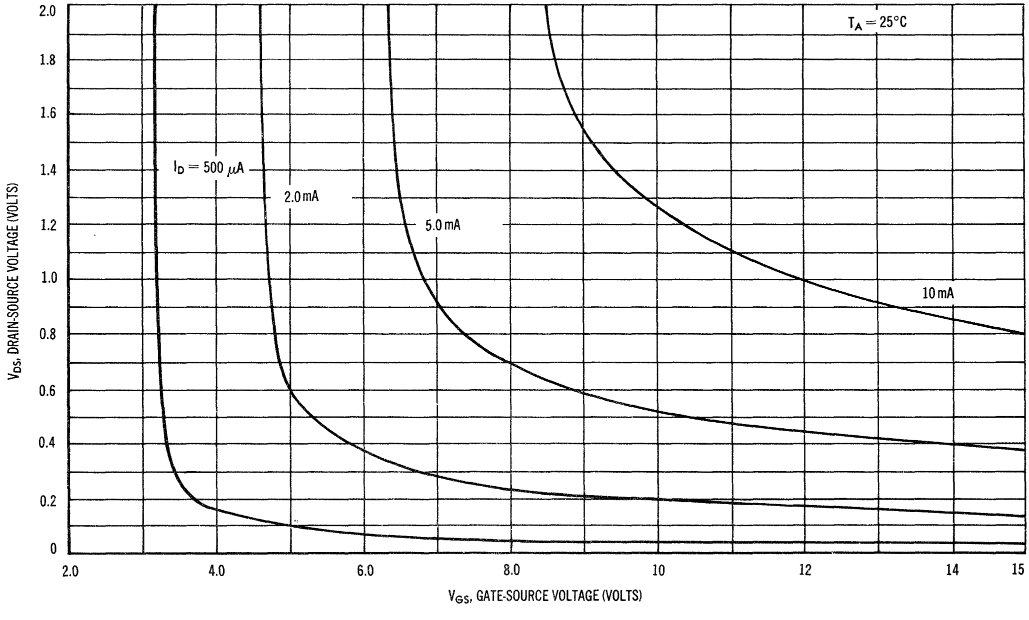


FIGURE 5 – "ON" DRAIN-SOURCE VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

$T_A = 25^oC$

FIGURE 6 – TURN-ON DELAY TIME

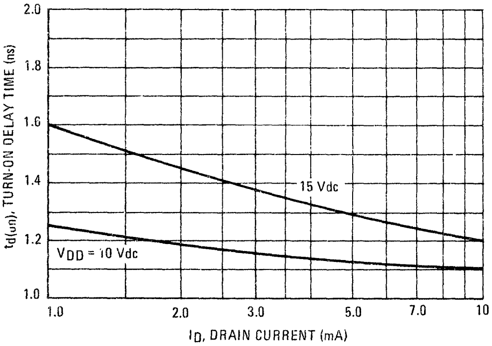


FIGURE 7 – RISE TIME

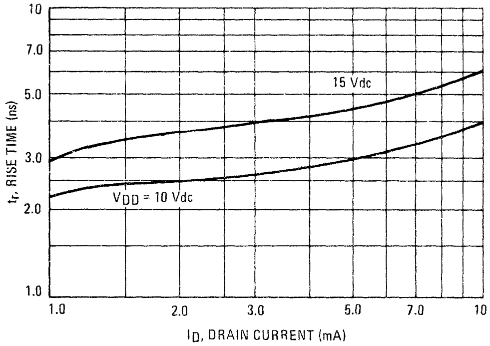


FIGURE 8 – TURN-OFF DELAY TIME

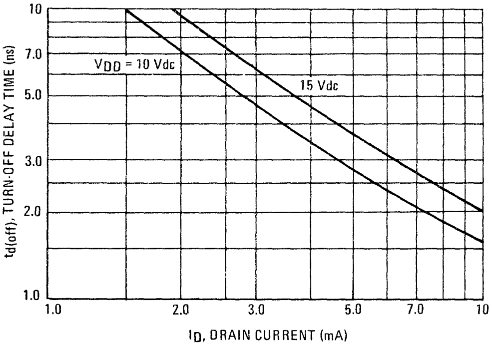


FIGURE 9 – FALL TIME

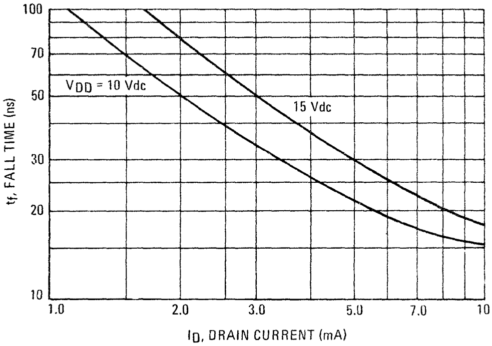
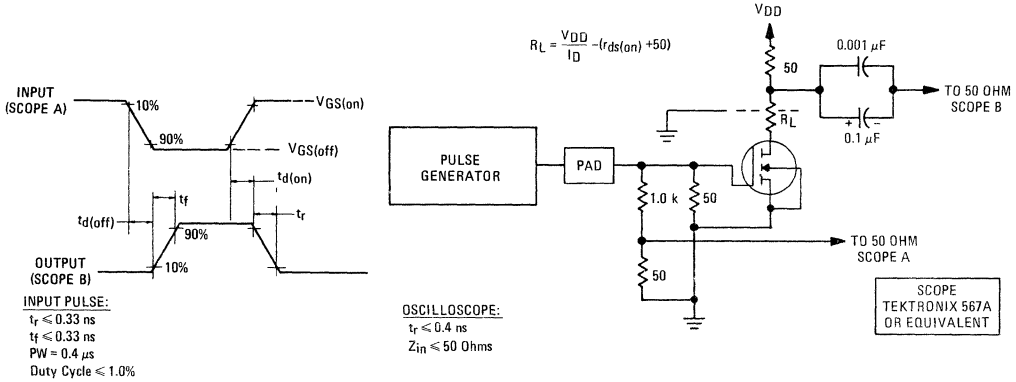


FIGURE 10 – SWITCHING TIME TEST CIRCUIT



3N209 (SILICON)
3N210

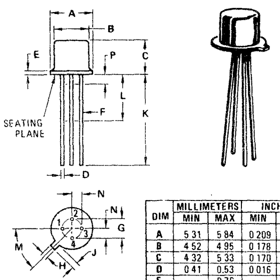
N-CHANNEL DUAL-GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTORS

. . . depletion mode dual gate transistors designed and characterized for UHF communications applications

- Two Packages Offered—
  - Hermetic Metal TO-72 – 3N209
  - Micro-H Plastic – 3N210
- Silicon Nitride Passivation for Excellent Long Term Stability
- Zener Diode Protected Gates
- Third Order Intermodulation Distortion Curve Provided
- Common Source Power Gain – G_{ps} = 10 dB (Min) @ f = 500 MHz
- Noise Figure – 6.0 dB Max @ f = 500 MHz

N-CHANNEL DUAL GATE MOS FIELD-EFFECT TRANSISTORS

3N209



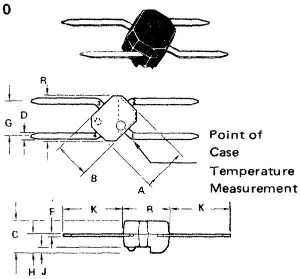
STYLE 9
PIN 1 DRAIN
2 GATE 2
3 GATE 1
4 SOURCE, SUBSTRATE AND CASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45°BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

3N210



STYLE 1
PIN 1 SOURCE
2 DRAIN
3 GATE 2
4 GATE 1

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.95	5.21	0.195	0.205
B	3.94	4.19	0.155	0.165
C	2.67	2.92	0.105	0.115
D	0.64	0.89	0.025	0.035
F	0.20	0.30	0.008	0.012
G	4.06 BSC		0.160 BSC	
H	1.57	1.83	0.062	0.072
J	0.51	0.76	0.020	0.030
K	6.35	7.62	0.250	0.300
R	5.21	5.46	0.205	0.215

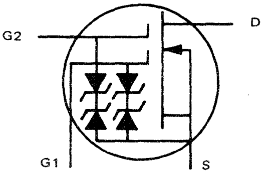
CASE 262-02

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
*Drain – Source Voltage	V_{DS}	25		Vdc
*Drain Gate Voltage	V_{DG1} V_{DG2}	30 30		Vdc Vdc
Gate Current	I_{G1R} I_{G1F} I_{G2R} I_{G2F}	-10 10 -10 10		mAdc mAdc mAdc mAdc
*Drain Current – Continuous	I_D	30		mAdc
		3N209	3N210	
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.71	350 2.80	mW mW/°C
*Storage Channel Temperature Range	T_{stg}	-65 to +200	-65 to +175	°C
*Operating Channel Temperature	$T_{channel}$	200	150	°C
*Lead Temperature, 1/16" From Seated Surface for 10 Seconds		260	260	°C

*Indicates JEDEC Registered Data.

FIGURE 1 – MOS FET CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) Substrate Connected to Source

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_{G1S} = -4.0 Vdc, V_{G2S} = 4.0 Vdc)	$V_{(BR)DS}$	25	–	–	Vdc
Gate 1 – Source Forward Breakdown Voltage (I_{G1} = 10 mAdc, V_{G2S} = V_{DS} = 0)	$V_{(BR)G1SSF}$	7.0	–	22	Vdc
Gate 1 – Source Reverse Breakdown Voltage (I_{G1} = -10 mAdc, V_{G2S} = V_{DS} = 0)	$V_{(BR)G1SSR}$	-7.0	–	-22	Vdc
Gate 2 – Source Forward Breakdown Voltage (I_{G2} = 10 mAdc V_{G1S} = V_{DS} = 0)	$V_{(BR)G2SSF}$	7.0	–	22	Vdc
Gate 2 – Source Reverse Breakdown Voltage (I_{G2} = -10 mAdc V_{G1S} = V_{DS} = 0)	$V_{(BR)G2SSR}$	-7.0	–	-22	Vdc
Gate 1 – Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 50 μAdc)	$V_{G1S(off)}$	-0.1	–	-4.0	Vdc
Gate 2 – Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0 Vdc, I_D = 50 μAdc)	$V_{G2S(off)}$	-0.1	–	-4.0	Vdc
Gate 1 – Terminal Forward Current (V_{G1S} = 6.0 Vdc, V_{G2S} = V_{DS} = 0)	I_{G1SSF}	–	–	20	nAdc
Gate 1 – Terminal Reverse Current (V_{G1S} = -6.0 Vdc, V_{G2S} = V_{DS} = 0) (V_{G1S} = -6.0 Vdc, V_{G2S} = V_{DS} = 0, T_A = 150°C)	I_{G1SSR}	– –	– –	-20 -10	nAdc μAdc
Gate 2 – Terminal Forward Current (V_{G2S} = 6.0 Vdc, V_{G1S} = V_{DS} = 0)	I_{G2SSF}	–	–	20	nAdc
Gate 2 – Terminal Reverse Current (V_{G2S} = -6.0 Vdc, V_{G1S} = V_{DS} = 0) (V_{G2S} = -6.0 Vdc, V_{G1S} = V_{DS} = 0, T_A = 150°C)	I_{G2SSR}	– –	– –	-20 -10	nAdc μAdc
***ON CHARACTERISTICS**					
Gate 1 – Zero Voltage Drain Current (V_{DS} = 15 Vdc, V_{G1S} = 0, V_{G2S} = 4.0 Vdc)	I_{DSS}	5.0	–	30	mAdc
SMALL SIGNAL CHARACTERISTICS					
*Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	y_{fs}	10	13	20	mmhos
*Input Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, $I_D \geqslant 5.0$ mAdc, f = 1.0 MHz)	C_{iss}	–	4.5	7.0	pF
*Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, $I_D \geqslant 5.0$ mAdc, f = 1.0 MHz)	C_{rss}	0.005	0.023	0.03	pF
*Output Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, $I_D \geqslant 5.0$ mAdc, f = 1.0 MHz)	C_{oss}	0.5	2.0	4.0	pF
*Common-Source Noise Figure (Figure 12) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 500 MHz)	NF	–	4.5	6.0	dB
*Common-Source Power Gain (Figure 12) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 500 MHz)	G_{ps}	10	13	20	dB
Bandwidth (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 500 MHz)	BW	7.0	–	17	MHz

*Indicates JEDEC Registered Data.

TYPICAL SCATTERING PARAMETERS

FIGURE 2 – S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY

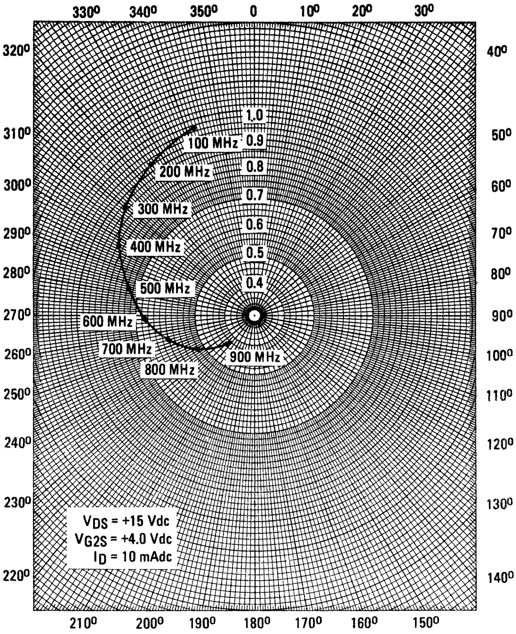


FIGURE 3 – S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY

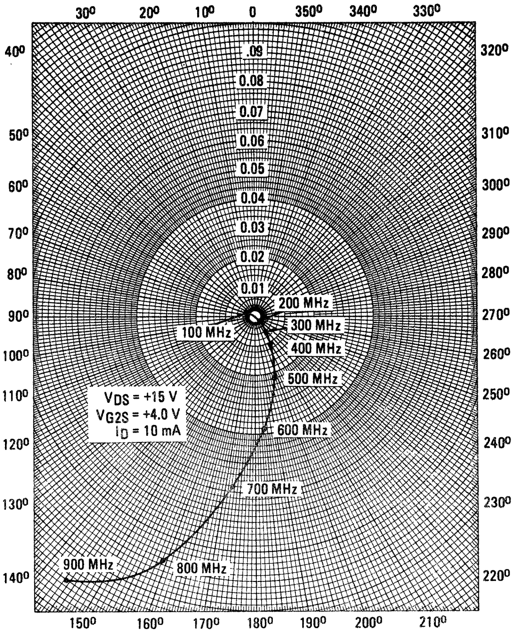


FIGURE 4 – S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY

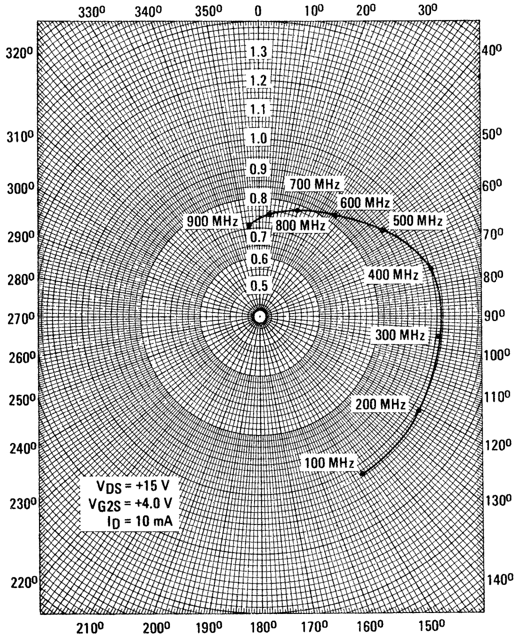
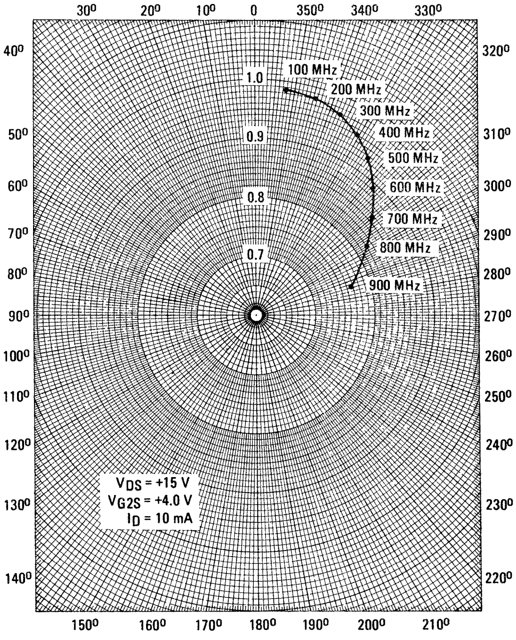


FIGURE 5 – S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY



TYPICAL COMMON-SOURCE ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, V_{GS2} = 4.0 Vdc, I_D = 10 mAdc)

FIGURE 6 – Y_{11}, INPUT ADMITTANCE versus FREQUENCY

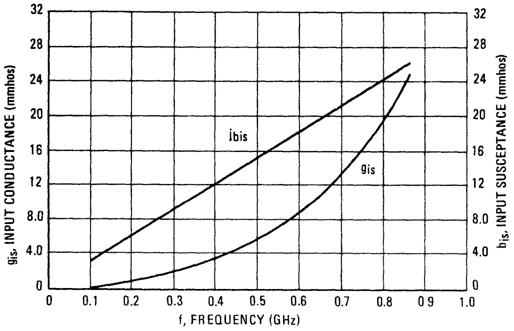


FIGURE 7 – Y_{12}, REVERSE TRANSFER ADMITTANCE versus FREQUENCY

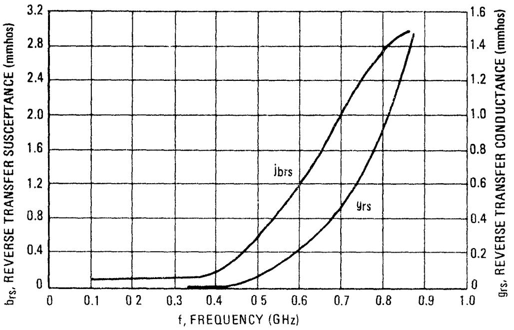


FIGURE 8 – Y_{21}, FORWARD TRANSFER ADMITTANCE versus FREQUENCY

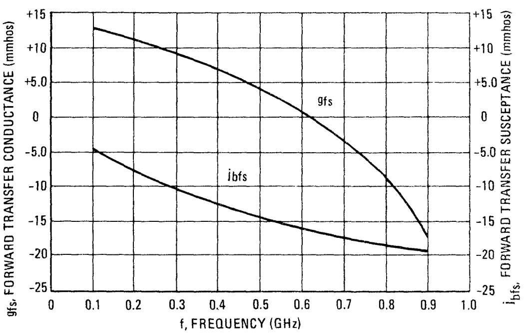
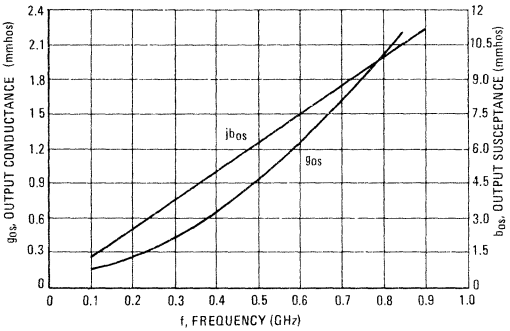


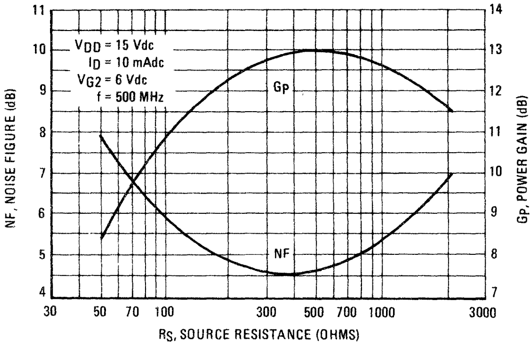
FIGURE 9 – Y_{22}, OUTPUT ADMITTANCE versus FREQUENCY



The S and Y Parameters were Measured with a Hewlett Packard HP8542A Network Analyzer.

FIGURE 10 – POWER GAIN AND NOISE FIGURE versus SOURCE RESISTANCE

(See Schematic Figure 12)



The Test Circuit shown in Figure 12 was used to generate Power Gain and Noise Figure as a function of Source Resistance curves.

FIGURE 11 – THIRD ORDER INTERMODULATION DISTORTION

(See Schematic Figure 12)

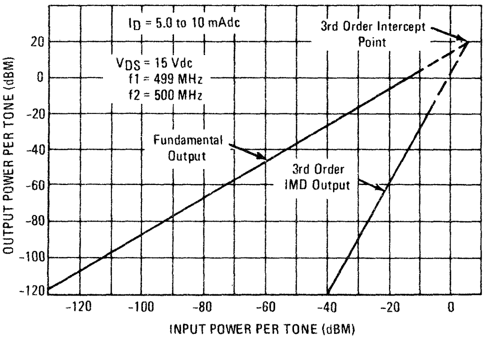
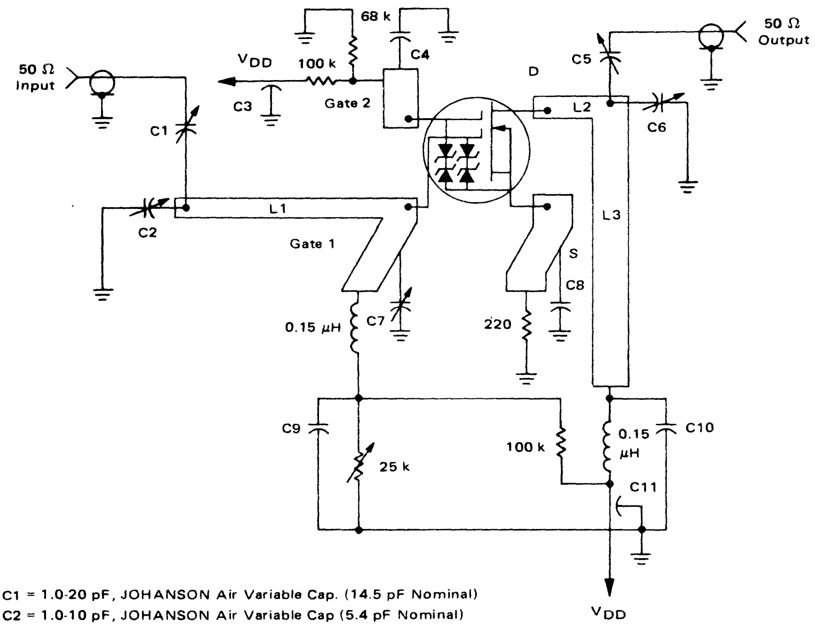


Figure 11 shows the typical third order intermodulation distortion (IMD) performance of the 3N209 and 3N210 at 500 MHz.

Both fundamental output and third order IMD output characteristics are plotted. The curves have been extrapolated to show the third order intermodulation output intercept point.

The performance is typical for I_D between 5.0 mAdc and 10 mAdc. The test circuit shown in Figure 12 was used to generate the IMD Data.

FIGURE 12 – TEST CIRCUIT FOR POWER GAIN, NOISE FIGURE AND THIRD ORDER INTERMODULATION DISTORTION



C1 = 1.0-20 pF, JOHANSON Air Variable Cap. (14.5 pF Nominal)
C2 = 1.0-10 pF, JOHANSON Air Variable Cap (5.4 pF Nominal)
C3, C11 = 470 pF, Low Inductance Feedthru Cap.
C4, C8, C9, C10 = 250 pF, Low Inductance, UNDERWOOD Cap. (J-101)
C5 = 0.4-6.0 pF, JOHANSON Air Variable Cap. (0.92 pF Nominal)
C6 = 1.0-10 pF, JOHANSON Air Variable Cap. (5.9 pF Nominal)
C7 = 1.0-10 pF, JOHANSON Air Variable Cap (3.0 pF Nominal)
L1 = 2.52 x 0.1 inches
L2 = 0.4 x 0.1 inches } On 2 sided glass Teflon®, 1 oz. copper clad, 1/16″ $\epsilon_R = 2.55$
L3 = 1.23 x 0.2 inches

® Trademark of E.I. Dupont, DeNemours and Co., Inc.

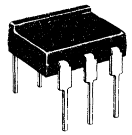
4N25
4N26
4N27
4N28

NPN PHOTOTRANSISTOR AND PN INFRARED EMITTING DIODE

. . . Gallium Arsenide LED optically coupled to a Silicon Photo Transistor designed for applications requiring electrical isolation, high-current transfer ratios, small package size and low cost; such as interfacing and coupling systems, phase and feedback controls, solid-state relays and general-purpose switching circuits.

- High Isolation Voltage –
  V_{ISO} = 2500 V (Min) – 4N25
  1500 V (Min) – 4N26, 4N27
  500 V (Min) – 4N28
- High Collector Output Current @ I_F = 10 mA –
  I_C = 5.0 mA (Typ) – 4N25, 4N26
  3.0 mA (Typ) – 4N27, 4N28
- Economical, Compact, Dual-In-Line Package
- Excellent Frequency Response – 300 kHz (Typ)
- Fast Switching Times @ I_C = 10 mA
  t_{on} = 0.87 μs (Typ) – 4N25, 4N26
  2.1 μs (Typ) – 4N27, 4N28
  t_{off} = 11 μs (Typ) – 4N25, 4N26
  5.0 μs (Typ) – 4N27, 4N28

INFRARED LIGHT EMITTING DIODE PHOTOTRANSISTOR COUPLED PAIR



*MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current – Continuous	I_F	80	mA
Forward Current – Peak Pulse Width = 300 μs, 2.0% Duty Cycle	I_F	3.0	Amp
Total Device Dissipation @ T_A 25°C Negligible Power in Transistor	P_D	150	mW
Derate above 25°C		2.0	mW/°C
PHOTOTRANSISTOR MAXIMUM RATINGS			
Collector-Emitter Voltage	V_{CEO}	30	Volts
Emitter-Collector Voltage	V_{ECO}	7.0	Volts
Collector-Base Voltage	V_{CBO}	70	Volts
Total Device Dissipation @ T_A = 25°C Negligible Power in Diode	P_D	150	mW
Derate above 25°C		2.0	mW/°C
TOTAL DEVICE RATINGS			
Total Device Dissipation @ T_A = 25°C Equal Power Dissipation in Each Element	P_D	250	mW
Derate above 25°C		3.3	mW/°C
Junction Temperature Range	T_J	-55 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)		260	°C

*Indicates JEDEC Registered Data.

FIGURE 1 – MAXIMUM POWER DISSIPATION

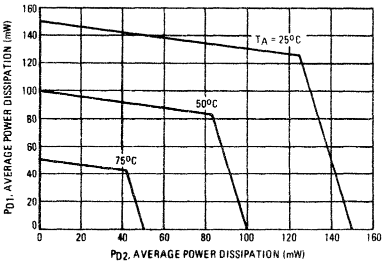


Figure 1 is based upon using limit values in the equation

$$T_{J1} - T_A = R_{\theta JA}(P_{D1} + K_\theta P_{D2})$$

where

T_{J1} Junction Temperature (100°C)

T_A Ambient Temperature

$R_{\theta JA}$ Junction to Ambient Thermal Resistance (500°C/W)

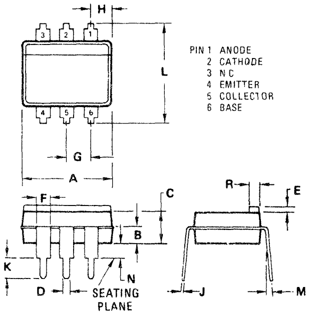
P_{D1} Power Dissipation in One Chip

P_{D2} Power Dissipation in Other Chip

K_θ Thermal Coupling Coefficient (20%)

Example

With P_{D1} = 90 mW in the LED @ T_A = 50°C, the transistor P_D (P_{D2}) must be less than 50 mW.



PIN 1 ANODE
2 CATHODE
3 N.C.
4 EMITTER
5 COLLECTOR
6 BASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.38	8.89	0.330	0.350
B	1.40	1.65	0.055	0.065
C	2.92	3.18	0.115	0.125
D	0.41	0.51	0.016	0.020
E	0.64	0.89	0.025	0.035
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	1.57	1.83	0.062	0.072
J	0.23	0.28	0.009	0.011
K	2.54	3.30	0.100	0.130
L	7.37	7.87	0.290	0.310
M	–	5°	–	5°
N	–	1.27	–	0.050
R	1.52	1.78	0.060	0.070

CASE 673-03

LED CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Reverse Leakage Current (V_R = 3.0 V, R_L = 1.0 M ohms)	I_R	–	0.05	100	μA
*Forward Voltage (I_F = 50 mA)	V_F	–	1.2	1.5	Volts
Capacitance (V_R = 0 V, f = 1.0 MHz)	C	–	150	–	pF

PHOTOTRANSISTOR CHARACTERISTICS (T_A = 25°C and I_F = 0 unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
*Collector-Emitter Dark Current (V_{CE} = 10 V, Base Open)	4N25, 4N26, 4N27 4N28	I_{CEO}	– –	3.5 –	50 100	nA
*Collector-Base Dark Current (V_{CB} = 10 V, Emitter Open)		I_{CBO}	–	–	20	nA
*Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)		BV_{CBO}	70	–	–	Volts
*Collector-Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0)		BV_{CEO}	30	–	–	Volts
*Emitter-Collector Breakdown Voltage (I_E = 100 μA, I_B = 0)		BV_{ECO}	7.0	–	–	Volts
DC Current Gain (V_{CE} = 5.0 V I_C = 500 μA)		h_{FE}	–	250	–	–

COUPLED CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
*Collector Output Current (1) (V_{CE} = 10 V, I_F = 10 mA, I_B = 0)	4N25,4N26 4N27,4N28	I_C	2.0 1.0	5.0 3.0	– –	mA
*Isolation Voltage (2)	4N25 4N26,4N27 4N28	V_{ISO}	2500 1500 500	– – –	– – –	Volts
Isolation Resistance (2) (V = 500 V)		–	–	10^{11}	–	Ohms
*Collector-Emitter Saturation (I_C = 2.0 mA, I_F = 50 mA)		$V_{CE(sat)}$	–	0.2	0.5	Volts
Isolation Capacitance (2) (V = 0, f = 1.0 MHz)		–	–	1.3	–	pF
Bandwidth (3) (I_C = 2.0 mA, R_L = 100 ohms, Figure 11)		–	–	300	–	kHz

SWITCHING CHARACTERISTICS

			Symbol	Min	Typ	Max	Unit
Delay Time	(I_C = 10 mA, V_{CC} = 10 V) Figures 6 and 8	4N25,4N26 4N27,4N28	t_d	– –	0.07 0.10	– –	μs
Rise Time		4N25,4N26 4N27,4N28	t_r	– –	0.8 2.0	– –	μs
Storage Time	(I_C = 10 mA, V_{CC} = 10 V) Figures 7 and 8	4N25,4N26 4N27,4N28	t_s	– –	4.0 2.0	– –	μs
Fall Time		4N25,4N26 4N27,4N28	t_f	– –	7.0 3.0	– –	μs

*Indicates JEDEC Registered Data (1) Pulse Test Pulse Width = 300 μs, Duty Cycle ≤ 2.0%

(2) For this test LED pins 1 and 2 are common and Photo Transistor pins 4, 5 and 6 are common

(3) I_F adjusted to yield I_C = 2.0 mA and i_c = 2.0 mA p-p at 10 kHz

DC CURRENT TRANSFER CHARACTERISTICS

FIGURE 2 – 4N25, 4N26

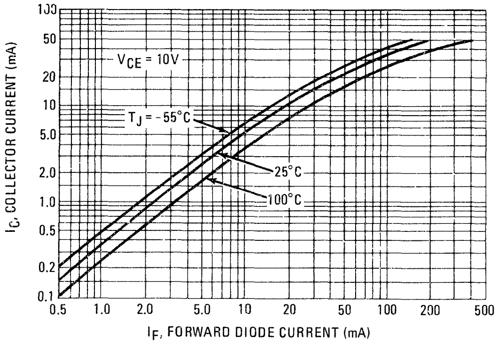
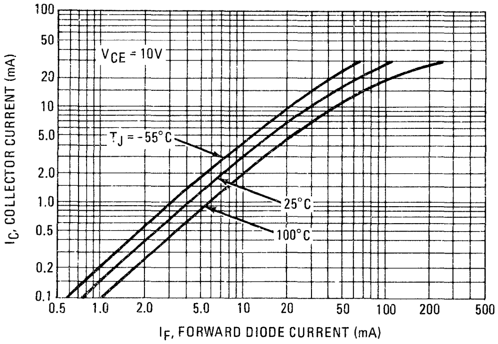


FIGURE 3 – 4N27, 4N28



TYPICAL ELECTRICAL CHARACTERISTICS

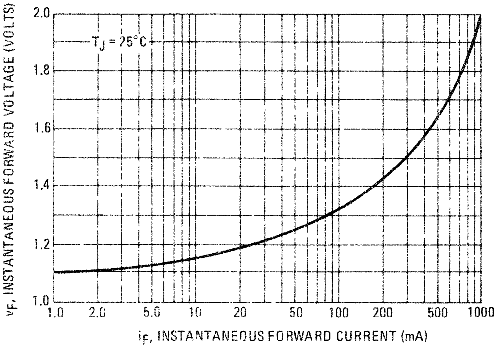


FIGURE 4 – DIODE FORWARD CHARACTERISTICS

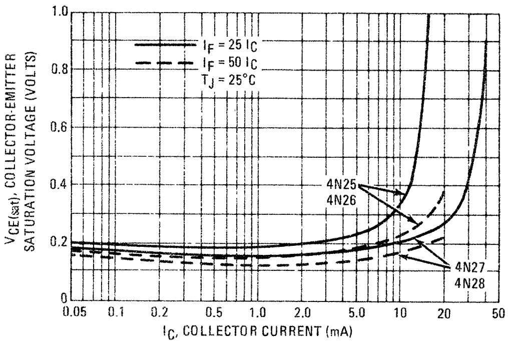


FIGURE 5 – COLLECTOR SATURATION VOLTAGE

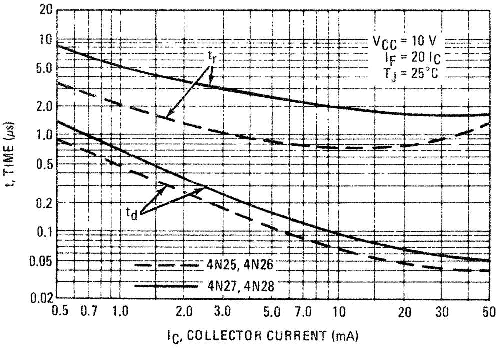


FIGURE 6 – TURN-ON TIME

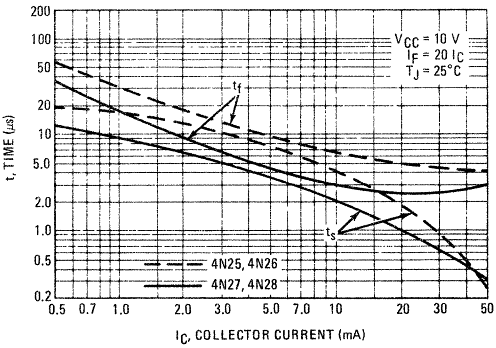


FIGURE 7 – TURN-OFF TIME

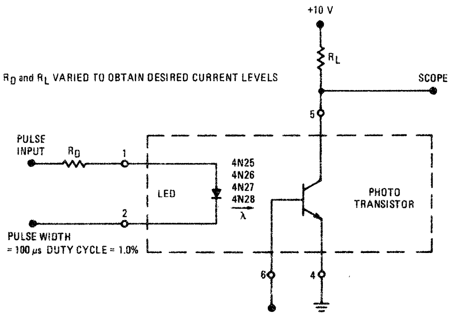


FIGURE 8 – SATURATED SWITCHING TIME TEST CIRCUIT

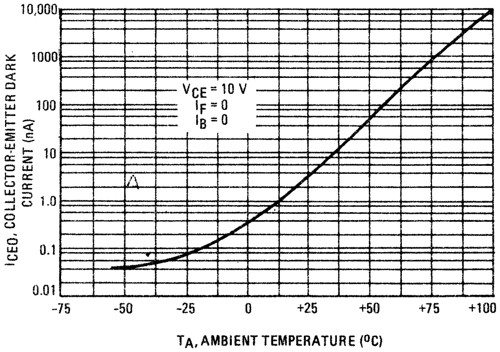


FIGURE 9 – DARK CURRENT versus AMBIENT TEMPERATURE

FIGURE 10 – FREQUENCY RESPONSE

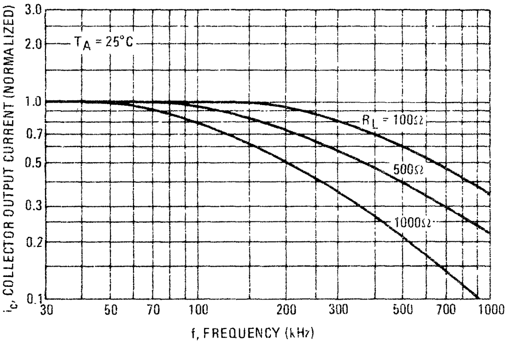
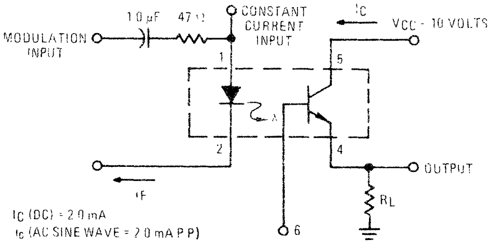


FIGURE 11 – FREQUENCY RESPONSE TEST CIRCUIT



TYPICAL APPLICATIONS

FIGURE 12 – ISOLATED MTTL TO MOS (P-CHANNEL) LEVEL TRANSLATOR

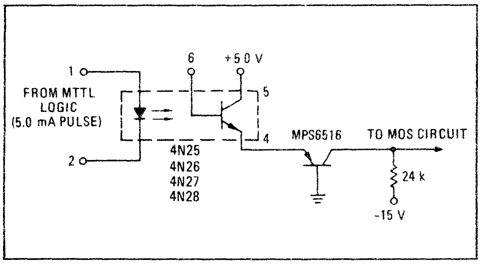


FIGURE 13 – COMPUTER/PERIPHERAL INTERCONNECT

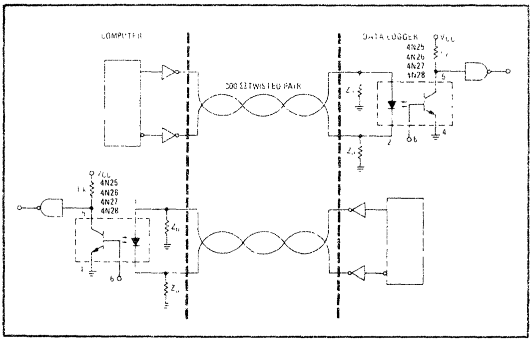


FIGURE 14 – POWER AMPLIFIER

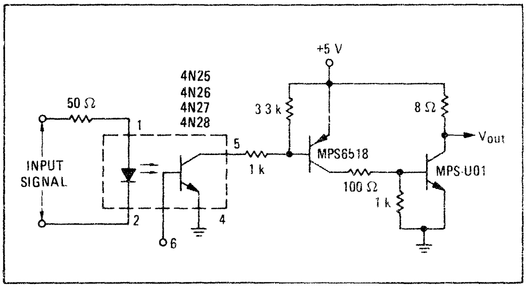
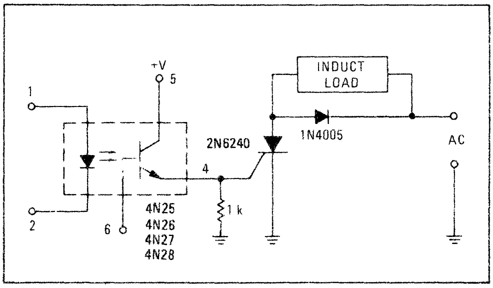


FIGURE 15 – INTERFACE BETWEEN LOGIC AND LOAD



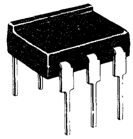
4N29, 4N30
4N31, 4N32, 4N33

NPN PHOTOTRANSISTOR AND PN INFRARED EMITTING DIODE

. . . Gallium Arsenide LED optically coupled to a Silicon Photo Darlington Transistor designed for applications requiring electrical isolation, high-current transfer ratios, small package size and low cost; such as interfacing and coupling systems, phase and feedback controls, solid-state relays and general-purpose switching circuits.

- High Isolation Voltage –
  V_{ISO} = 2500 V (Min) – 4N29,32
  1500 V (Min) – 4N30,31,33
- High Collector Output Current @ I_F = 10 mA –
  I_C = 50 mA (Min) – 4N32,33
  10 mA (Min) – 4N29,30
  5.0 mA (Min) – 4N31
- Economical, Compact, Dual-In-Line Package
- Excellent Frequency Response –
  30 kHz (Typ)
- Fast Switching Times @ I_C = 50 mA
  t_{on} = 0.6 μs (Typ)
  t_{off} = 17 μs (Typ) – 4N29,30,31
  45 μs (Typ) – 4N32,33

INFRARED LIGHT EMITTING DIODE
PHOTO DARLINGTON TRANSISTOR
COUPLED PAIR



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED-EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current – Continuous	I_F	80	mA
Forward Current – Peak (Pulse Width = 300 μs, 2.0% Duty Cycle)	I_F	3.0	Amp
Total Power Dissipation @ T_A = 25°C Negligible Power in Transistor	P_D	150	mW
Derate above 25°C		2.0	mW/°C
PHOTOTRANSISTOR MAXIMUM RATINGS			
Collector-Emitter Voltage	V_{CEO}	30	Volts
Emitter-Collector Voltage	V_{ECO}	5.0	Volts
Collector-Base Voltage	V_{CBO}	30	Volts
Total Power Dissipation @ T_A = 25°C Negligible Power in Diode	P_D	150	mW
Derate above 25°C		2.0	mW/°C
TOTAL DEVICE RATINGS			
Total Device Dissipation @ T_A = 25°C Equal Power Dissipation in Each Element	P_D	250	mW
Derate above 25°C		3.3	mW/°C
Operating Junction Temperature Range	T_J	-55 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)	–	260	°C

FIGURE 1 – MAXIMUM POWER DISSIPATION

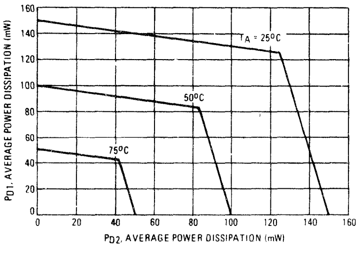


Figure 1 is based upon using limit values in the equation:

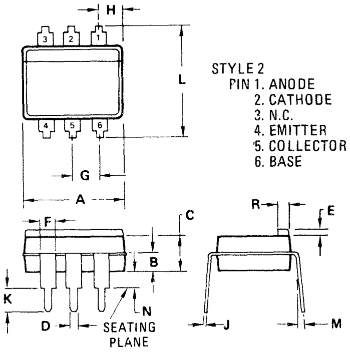
$$T_{J1} - T_A = R_{\theta JA} (P_{D1} + K_\theta P_{D2})$$

where

T_{J1}	Junction Temperature (100°C)
T_A	Ambient Temperature
$R_{\theta JA}$	Junction to Ambient Thermal Resistance (500°C/W)
P_{D1}	Power Dissipation in One Chip
P_{D2}	Power Dissipation in Other Chip
K_θ	Thermal Coupling Coefficient (20%)

Example.

With P_{D1} = 90 mW in the LED @ T_A = 50°C, the Darlington P_D (P_{D2}) must be less than 50 mW.



STYLE 2
PIN 1. ANODE
2. CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.38	8.89	0.330	0.350
B	1.40	1.65	0.055	0.065
C	2.92	3.18	0.115	0.125
D	0.41	0.51	0.016	0.020
E	0.64	0.89	0.025	0.035
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	1.57	1.83	0.062	0.072
J	0.23	0.28	0.009	0.011
K	2.54	3.30	0.100	0.130
L	7.37	7.87	0.290	0.310
M	–	5°	–	5°
N	–	1.27	–	0.050
R	1.52	1.78	0.060	0.070

CASE 673-03

LED CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Reverse Leakage Current (V_R = 3.0 V, R_L = 1.0 M ohms)	I_R	–	0.05	100	µA
*Forward Voltage (I_F = 50 mA)	V_F	–	1.2	1.5	Volts
Capacitance (V_R = 0 V, f = 1.0 MHz)	C	–	150	–	pF

PHOTOTRANSISTOR CHARACTERISTICS (T_A = 25°C and I_F = 0 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Collector-Emitter Dark Current (V_{CE} = 10 V, Base Open)	I_{CEO}	–	–	100	nA
*Collector-Base Breakdown Voltage (I_C = 100 µA, I_E = 0)	BV_{CBO}	30	–	–	Volts
*Collector-Emitter Breakdown Voltage (I_C = 100 µA, I_B = 0)	BV_{CEO}	30	–	–	Volts
*Emitter-Collector Breakdown Voltage (I_E = 100 µA, I_B = 0)	BV_{ECO}	5.0	–	–	Volts
DC Current Gain (V_{CE} = 5.0 V, I_C = 500 µA)	h_{FE}	–	5000	–	–

COUPLED CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Collector Output Current (1) (V_{CE} = 10 V, I_F = 10 mA, I_B = 0)	4N32, 4N33 4N29, 4N30 4N31	I_C	50 10 5.0	– – –	– – –	mA
*Isolation Voltage (2)	4N29, 4N32 4N30, 4N31, 4N33	V_{ISO}	2500 1500	– –	– –	Volts
Isolation Resistance (2) (V = 500 V)		–	–	10^{11}	–	Ohms
*Collector-Emitter Saturation Voltage (1) (I_C = 2.0 mA, I_F = 8.0 mA)	4N31 4N29, 4N30, 4N32, 4N33	$V_{CE(sat)}$	– –	– –	1.2 1.0	Volts
Isolation Capacitance (2) (V = 0, f = 1.0 MHz)		–	–	0.8	–	pF
Bandwidth (3) (I_C = 2.0 mA, R_L = 100 ohms, Figures 6 and 8)		–	–	30	–	kHz

SWITCHING CHARACTERISTICS (Figures 7 and 9), (4)

Turn-On Time (I_C = 50 mA, I_F = 200 mA, V_{CC} = 10 V)		t_{on}	–	0.6	5.0	µs
Turn-Off Time (I_C = 50 mA, I_F = 200 mA, V_{CC} = 10 V)	4N29,30,31 4N32,33	t_{off}	– –	17 45	40 100	µs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2.0%

(2) For this test LED pins 1 and 2 are common and Photo Transistor pins 4,5 and 6 are common.

(3) I_F adjusted to yield I_C = 2.0 mA and i_c = 2.0 mA P-P at 10 kHz.

(4) t_d and t_r are inversely proportional to the amplitude of I_F; t_s and t_f are not significantly affected by I_F.

DC CURRENT TRANSFER CHARACTERISTICS

FIGURE 2 – 4N29, 4N30, 4N31

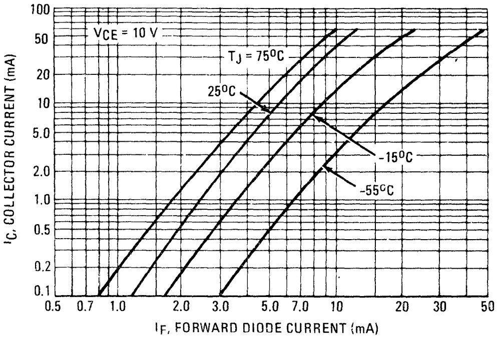
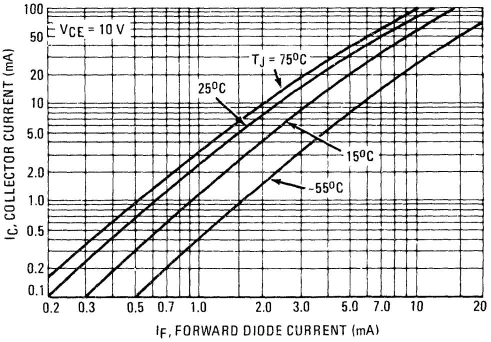


FIGURE 3 – 4N32, 4N33



TYPICAL ELECTRICAL CHARACTERISTICS

(Printed Circuit Board Mounting)

FIGURE 4 – DIODE FORWARD CHARACTERISTIC

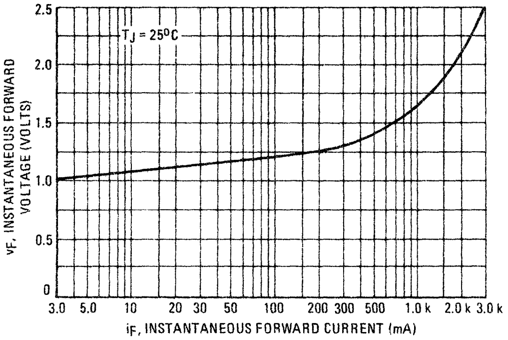


FIGURE 5 – COLLECTOR-EMITTER CUTOFF CURRENT

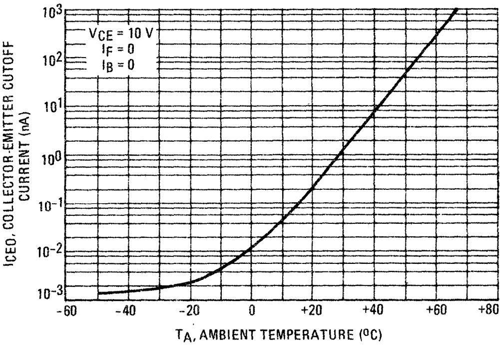


FIGURE 6 – FREQUENCY RESPONSE

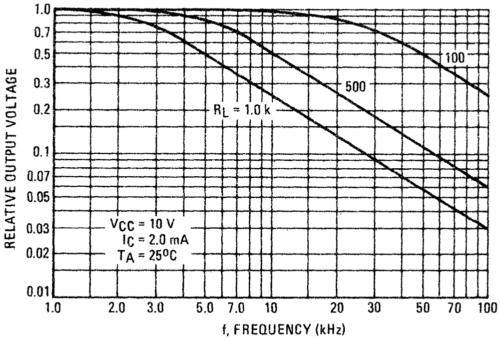


FIGURE 7 – SWITCHING TIMES

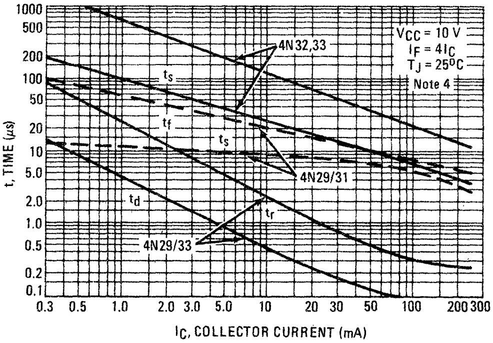


FIGURE 8 – FREQUENCY RESPONSE TEST CIRCUIT

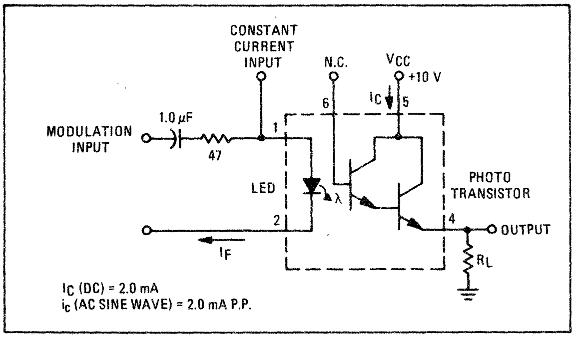
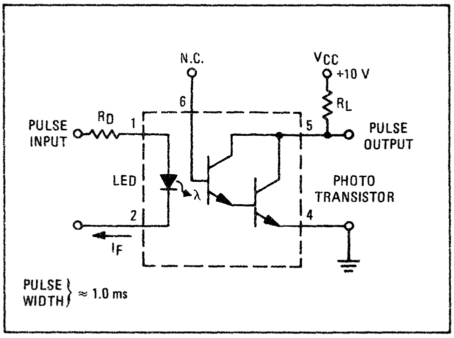


FIGURE 9 – SWITCHING TIME TEST CIRCUIT



TYPICAL APPLICATIONS

FIGURE 10 – VOLTAGE CONTROLLED TRIAC

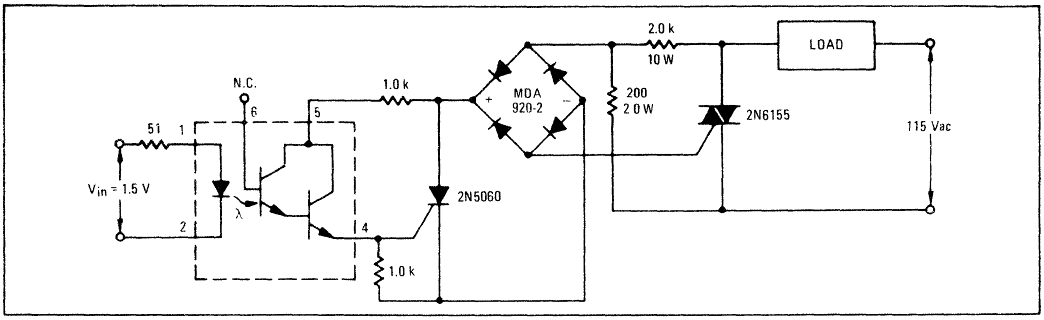


FIGURE 11 – AC SOLID STATE RELAY

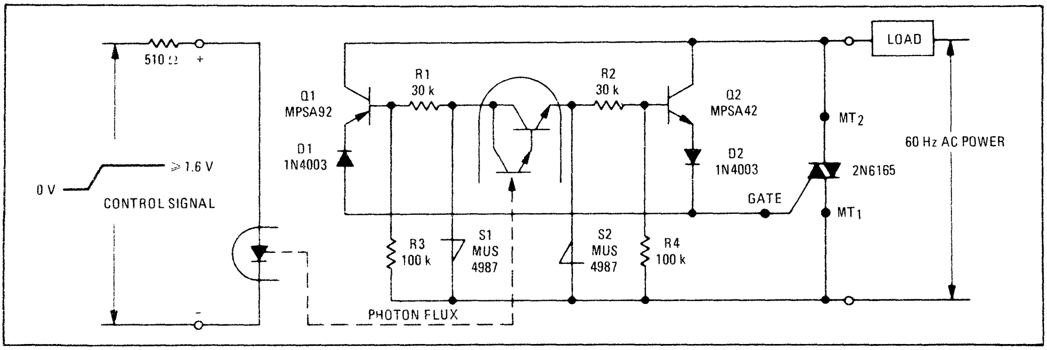


FIGURE 12 – OPTICALLY COUPLED ONE SHOT

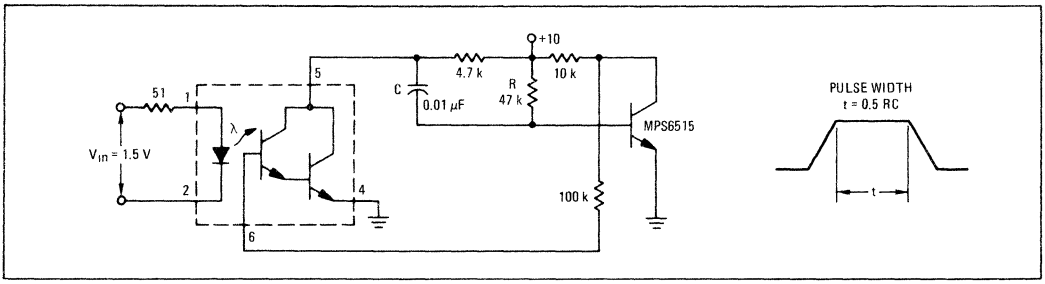
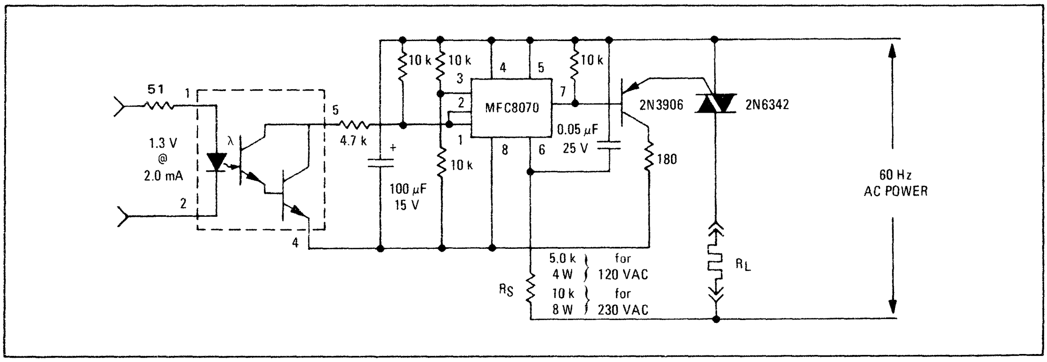


FIGURE 13 – ZERO VOLTAGE SWITCH



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