MOTOROLA

LINEAR

INTEGRATED CIRCUITS

MOTOROLA

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Prepared by
Technical Information Center

This Linear Integrated Circuits Data Book contains technical information on a portion of Motorola Linear's product offering. Detailed information on Comparators and Interface products is contained in a separate Interface Data Book. For your convenience, this book contains the following:

- Cross-Reference
- Selector Guides (by Product Category)
- Data Sheets
- Package Information and Mounting Hardware
- Abstracts Covering Application Notes and Engineering Bulletins.

Series C
Second Printing

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Master Index and Cross-Reference Guide

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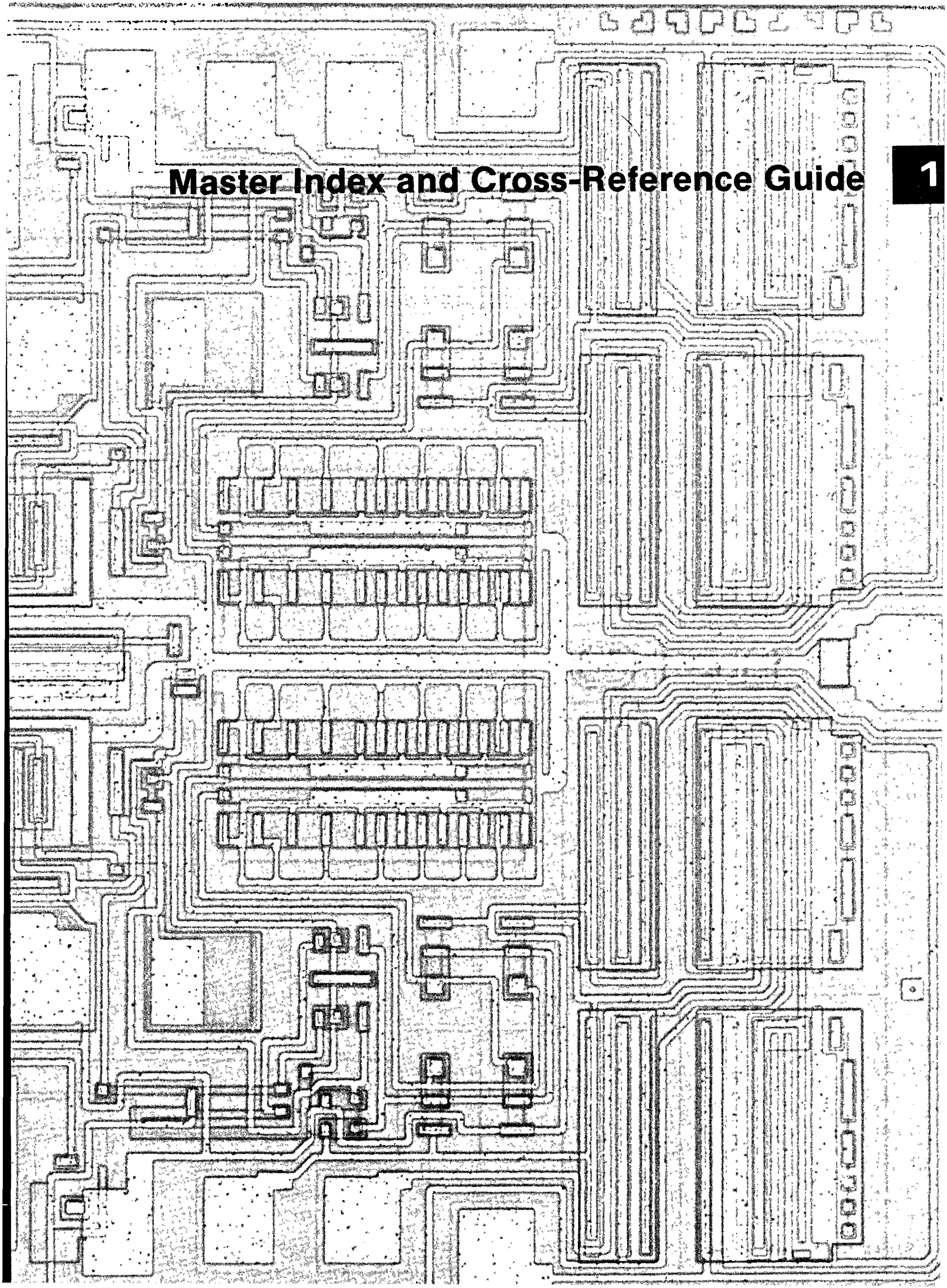

MASTER INDEX

This index includes *all* devices in Motorola Linear's product line. Devices with *Interface* in the page number column are fully characterized in the separate **Interface Data Book**; however, selection characteristics are given in Chapter 7 of this volume for your convenience.

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MOTOROLA — LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

. . . provides a complete interchangeability list linking over 3000 devices offered by most major Linear Integrated Circuits manufacturers to the nearest equivalent Motorola device. The "Motorola Direct Replacement" column lists devices with identical pin connections and package and the same or better electrical characteristics and temperature range. The "Motorola Functional Equivalent" column provides a device which performs the same function but with possible differences in package configurations, pin connections, temperature range or electrical specifications.

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
709BE	MC1709G	
709BH	MC1709F	
709CE	MC1709CG	
709CH	MC1709CF	
709CJ	MC1709CP2	
710BE	MC1710G	
710CE	MC1710CG	
711BE	MC1711G	
711BN	MC1711L	
711CE	MC1711CG	
711CJ	MC1711CP	
723BE	MC1723G	
723CE	MC1723CG	
723CJ	MC1723CL	
741BE	MC1741G	
741BH	MC1741F	
741BN	MC1741L	
741CE	MC1741CG	
747BE		MC1747G
747BN		MC1747L
747CE		MC1747CG
748BE		MC1748G
748CE		MC1748CG
809BE		MC1776G
809CE		MC1776CG
823AE		MC1723G
1458CE	MC1458CG	
3232		MC3232AL
3245	MC3245L	
6605J		MC3443P
6605L		MC3443P
8216		MC8T26AL
8226		MC8T28L
9614DC		MC75S110L
9614DM		MC75S110L
9615DC		MC75108L
9615DM		MC55108L
9615FM		MC55108L
9616CDC		MC1488L
9616EDC		MC1488L
9616DM		MC1488L
9617DC		MC1489AL
9620DC		MC75S110L
9620DM		MC75S110L
9621DC		MC75108L
9621DM		MC55108L
9622DC		MC75140P1
9622DM		MC75140P1
9624DC		MMH0026CL
9624DM		MMH0026CL
9625DC		MMH0026CL
9625DM		MMH0026CL
9627CDC		MC1489AL

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
9627DM		MC1489AL
9636AT	MC3488AP	
9637T		MC3486P
9638T		MC3487P
9640J	MC3443P	
9640D		MC3443P
9640DC		MC3440AP
9640NC	MC3440AP	
9665DC	MC1411L	
9665PC	MC1411P	
9666DC	MC1412L	
9666PC	MC1412P	
9667DC	MC1413L	
9667PC	MC1413P	
9668DC	MC1416L	
9668PC	MC1416P	
55107ADM	MC55107L	
55107BDM		MC55107L
55108ADM	MC55108L	
55108BDM		MC55108L
55110DM		MC75S110L
55121DM		MC8T13L
55122DM		MC8T14L
55207DM		MC55107L
55208DM		MC55108L
55325DM	MC55325L	
55325FM	MC55325L	
75107ADC	MC75107L	
75107APC	MC75107P	
75107BDC		MC75107L
75107BPC		MC75107P
75108ADC	MC75108L	
75108APC	MC75108P	
75108BDC		MC75108L
75108BPC		MC75108P
75110DC	MC75S110L	
75110PC	MC75S110P	
75121DC	MC8T13L	
75121PC	MC8T13P	
75122DC	MC8T14L	
75122PC	MC8T14P	
75123DC	MC8T23L	
75123PC	MC8T23P	
75124DC	MC8T24L	
75124PC	MC8T24P	
75207DC		MC75107L
75207PC		MC75107P
75208DC		MC75108L
75208PC		MC75108P
75325DC	MC75325L	
75325PC	MC75325P	
75450ADC	MC75450L	
75450APC	MC75450P	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
75450BDC		MC75450L
75450BPC		MC75450P
75451APC	MC75451U	
75451ATC	MC75451P	
75451BRC		MC75451U
75451BTC	SN75451BP	
75452ARC	MC75452U	
75452ATC	MC75452P	
75452BRC		MC75452U
75452BTC	SN75452BP	
75453ARC	MC75453U	
75453ATC	MC75453P	
75453BRC		MC75453U
75453BTC	SN75453BP	
75454ARC	MC75454U	
75454ATC	MC75454P	
75454BRC		MC75454U
75454BTC	SN75454BP	
75460DC		MC75450L
75460PC		MC75450P
75461RC	MC75461U	
75461TC	MC75461P	
75462RC	MC75462U	
75462TC	MC75462P	
75463RC	MC75463U	
75463TC	MC75463P	
75464RC	MC75464U	
75464TC	MC75464P	
75491DC		MC75491P
75491PC	MC75491P	
75491ADC		MC75491P
75491APC		MC75491P
75492DC		MC75492P
75492PC	MC75492P	
75492ADC		MC75492P
75492APC		MC75492P
AD301AL		LM301AH
AD505J		MC1776CG
AD505K		MC1776CG
AD505S		MC1776G
AD509J		LM301AH
AD509K		LM301AH
AD509S		LM101AH
AD518J		LM301AH
AD518K		LM301AH
AD518S		LM101AH
AD530		MC1595L
AD531		MC1595L
AD532J		MC1595G
AD559JD	MC1408L8	
AD559K	MC1408L8	
AD559KD	MC1408L8	
AD559S	MC1508L8	

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PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
AD559SD	MC1508L8	
AD580J		MC1403U
AD580K		MC1403P1
AD580M		MC1403AP1
AD580S		MC1503U
AD580T		MC1503AU
AD741CJ		MC1741CG
AD741J		MC1741G
AD741K		MC1741G
AD741L		MC1741G
AD741S		MC1741SG
AD7520D		MC3410L
AD7520F		MC3410L
AD7520N		MC3410L
AM26S10DC	MC26S10L	
AM26S10PC	MC26S10P	
AM26S11DC	MC26S11L	
AM26S11PC	MC26S11P	
AM725A31T		MC1556G
AM166039F		LM301AH
AM166039T		LM301AH
AMLM101	LM101AH	
AMLM101A	LM101AH	
AMLM101AD		LM101AH
AMLM101AF		LM101AH
AMLM101D		LM101AH
AMLM101F		LM101AH
AMLM105	LM105H	
AMLM105F		LM105H
AMLM105H	LM105H	
AMLM107	LM107H	
AMLM107D		LM107H
AMLM107F		LM107H
AMLM111D	LM111J	
AMLM111H	LM111H	
AMLM201	LM201AH	
AMLM201A	LM201AH	
AMLM201AD		LM201AN
AMLM201AF		LM201AH
AMLM201D		LM201AN
AMLM201F		LM201AH
AMLM205	LM205H	
AMLM205F		LM205H
AMLM205H	LM205H	
AMLM207	LM207H	
AMLM207D		LM207H
AMLM207F		LM207H
AMLM211D	LM211J	
AMLM211H	LM211H	
AMLM301	LM301AH	
AMLM301A	LM301AH	
AMLM301AD		LM301AJ
AMLM301D		LM301AJ
AMLM305	LM305H	
AMLM305A		LM305H
AMLM305F		LM305H
AMLM305H	LM305H	
AMLM311D	LM311J-8	
AMLM311H	LM311H	
AMU3F7733312		MC1733L
AMU3F7733393		MC1733CL
AMU3F7748312		MC1748G
AMU3I7741312	MC1741F	
AMU3I7741393	MC1741CL	
AMU5B7733312	MC1733G	
AMU5B7733393	MC1733CG	
AMU5B7741312	MC1741G	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
AMU5B7741393	MC1741CG	
AMU5B7747312	MC1747G	
AMU5B7747393	MC1747CG	
AMU5B7748312	MC1748G	
AMU5B7748393	MC1748CG	
AMU5R7723312	MC1723G	
AMU5R7723393	MC1723CG	
AMU6A7723312	MC1723L	
AMU6A7723393	MC1723CL	
AMU6A7733312	MC1733L	
AMU6A7733393	MC1733CL	
AMU6A7741312	MC1741L	
AMU6A7741393	MC1741CL	
AMU6A7748312		MC1748G
AMU6A7748393		MC1748CP1
AMU6W7747312	MC1747L	
AMU6W7747393	MC1747CL	
CA101AT	LM101AH	
CA101T	LM101AH	
CA107T	LM107H	
CA108AS	LM108AJ-8	
CA108AT	LM108AH	
CA108S	LM108J-8	
CA108T	LM108H	
CA139AG	LM139AJ	
CA139G	LM139J	
CA201AT	LM201AH	
CA201T		LM201AH
CA207T	LM207H	
CA208AT	LM208AH	
CA208S	LM208J-8	
CA208T	LM208H	
CA239AE	LM239AN	
CA239AG	LM239AJ	
CA239E	LM239N	
CA239G	LM239J	
CA301AT	LM301AH	
CA307T	LM307H	
CA308AS	LM308N	
CA308AT	LM308AH	
CA308S	LM308H	
CA339AE	LM339AN	
CA339AG	LM339AJ	
CA339E	LM339N	
CA339G	LM339J	
CA723CE	MC1723CP	
CA741CS	MC1741CP1	
CA741CT	MC1741CG	
CA741S	MC1741U	
CA741T	MC1741G	
CA747CE	MC1747CL	
CA747CF	MC1747CL	
CA747CT	MC1747CG	
CA747E	MC1747L	
CA747F	MC1747L	
CA747T	MC1747G	
CA748CS	MC1748CP1	
CA748CT	MC1748CG	
CA748S	MC1748U	
CA748T	MC1748G	
CA758E		MC1310P
CA1310E	MC1310P	
CA1352E	MC1352P	
CA1391E	MC1391P	
CA1394E	MC1394P	
CA1398E	MC1398P	
CA1458S	MC1458CP1	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
CA1458T	MC1458G	
CA1558S		MC1558U
CA1558T	MC1558G	
CA2111AE	MC1357P	
CA2111AQ	MC1357PQ	
CA3000		MC1550G
CA3001		MC1550G
CA3002		MC1550G
CA3004		MC1550G
CA3005		MC1550G
CA3006		MC1550G
CA3007		MC1550G
CA3008		MC1709F
CA3008A		MC1709F
CA3010		MC1709G
CA3010A		MC1709G
CA3011		MC1590G
CA3012		MC1590G
CA3013		MC1357P
CA3014		MC1357P
CA3015		MC1709G
CA3015A		MC1709G
CA3016		MC1709F
CA3016A		MC1709F
CA3020		MC1554G
CA3020A		MC1454G
CA3021		MC1590G
CA3022		MC1590G
CA3023		MC1590G
CA3026		CA3054
CA3028A		MC1550G
CA3028AF		MC1550G
CA3028AS		MC1550G
CA3028B		MC1550G
CA3028BF		MC1550G
CA3028BS		MC1550G
CA3029		MC1709P2
CA3029A		MC1709P2
CA3030		MC1709P2
CA3030A		MC1709P2
CA3031		MC1712G
CA3032		MC1712CG
CA3033		MC1533L
CA3033A		MC1533L
CA3035		MC1352P
CA3035V1		MC1352P
CA3037		MC1709L
CA3037A		MC1709L
CA3038		MC1709L
CA3038A		MC1709L
CA3040		MC1510G
CA3041		MC1351P
CA3042		MC1357P
CA3043		MC1357P
CA3044		MC1364P
CA3044V1		MC1364P
CA3045		MC3346P
CA3045F		MC3346P
CA3046	MC3346P	
CA3047		MC1433L
CA3047A		MC1433L
CA3048		MC3301P
CA3052		MC3301P
CA3053		MC1550G
CA3053F		MC1550G
CA3053S		MC1550G
CA3054	CA3054	

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PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
CA3056	MC1741CG	
CA3056A	MC1741G	
CA3058		CA3059
CA3059	CA3059	
CA3064		MC1364P
CA3064E	MC1364P	
CA3065	MC1358P	
CA3066		MC1399P
CA3067		MC1323P
CA3068		MC1352P
CA3070		MC1399P
CA3071		MC1399P
CA3072		MC1323P
CA3076		MC1590G
CA3078AS		MC1776G
CA3078AT		MC1776G
CA3078S		MC1776CG
CA3078T		MC1776CG
CA3079		CA3059
CA3085		MC1723G
CA3085A		MC1723G
CA3085AF		MC1723L
CA3085AS		MC1723G
CA3085B		MC1723G
CA3085BF		MC1723L
CA3085BS		MC1723G
CA3085F		MC1723L
CA3085S		MC1723G
CA3086	MC3386P	
CA3086F		MC3346P
CA3090AQ		MC1310P
CA3091D		MC1594L
CA3120E		MC1344P
CA3125E		MC1323P
CA3134E		TDA1190Z
CA3134EM		TDA1190Z
CA3134QM		TDA1190Z
CA3136A		MC3346P
CA3137E		MC1323P
CA3139	CA3139	
CA3146		MC3346P
CA3401E	MC3401P	
CA6078AS		MC1776G
CA6078AT		MC1776G
CA6741S		MC1776G
CA6741T		MC1776G
CA3302E	MC3302P	
CMP-01CJ		MC1556G
CMP-01CP		MC1556P
D555CJ		MC1555G
D3232	MC3232AP	
D3242	MC3242AP	
D3245	MC3245P	
D8216		MC8T26AL
D8226		MC8T28L
DAC-01		MC1506L
DAC-08		MC1408L8
DAC-IC10BC	MC3410L	
DM7820AD		MC75140P1
DM7820J		MC75140P1
DM7822J		MC1489AL
DM7837J		MC3437L
DM7838J		MC3438L
DM7887J		MC3490P
DM7887N		MC3490P
DM7889J		MC3491P
DM7889N		MC3491P

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
DM7897J		MC3494P
DM7897N		MC3494P
DM8820AN		MC75140P1
DM8820J		MC75140P1
DM8820N		MC75140P1
DM8822J		MC1489AL
DM8822N		MC1489AP
DM8837N	MC3437P	
DM8838N	MC3438P	
DM8861N		MC75491P
DM8863N		MC75492P
DM8887J		MC3490P
DM8889J		MC3491P
DM8897J		MC3494P
DM75491N	MC75491P	
DM75492N	MC75492P	
DS0026CG		MMH0026CG
DS0026CH	MMH0026CG	
DS0026CJ	MMH0026CL	
DS0026CN	DS0026CP1	
DS0026G		MMH0026G
DS0026H	DS0026G	
DS0026J	DS0026L	
DS0056CG		MMH0026CG
DS0056CH		MMH0026CG
DS0056CJ		MMH0026CL
DS0056CN		MMH0026CP1
DS0056G		MMH0026G
DS0056H		MMH0026G
DS0056J		MMH0026L
DS1488J	MC1488L	
DS1488N	MC1488P	
DS1489AJ	MC1489AL	
DS1489AN	MC1489AP	
DS1489J	MC1489L	
DS1489N	MC1489P	
DS3486J	MC3486L	
DS3486N	MC3486P	
DS3487J	MC3487L	
DS3487N	MC3487P	
DS3612H		MC1472U
DS3612N		MC1472P1
DS3632H		MC1472U
DS3632J		MC1472U
DS3632N		MC1472P1
DS3644J		MC3245L
DS3644N		MC3245P
DS3650J	MC3450L	
DS3650N	MC3450P	
DS3651J	MC3430L	
DS3651N	MC3430P	
DS3652J	MC3452L	
DS3652N	MC3452P	
DS3653J	MC3432L	
DS3653N	MC3432P	
DS3674J	MC3460L	
DS3674N	MC3460P	
DS55107J	MC55107L	
DS55107W		MC75107L
DS55108J	MC55108L	
DS55108W		MC55108L
DS55110J		MC75S110L
DS55121J		MC8T13L
DS55121W		MC8T13L
DS55122J		MC8T14L
DS55122W		MC8T14L
DS55325J	MC55325L	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
DS75107J	MC75107L	
DS75107N	MC75107P	
DS75108J	MC75108L	
DS75108N	MC75108P	
DS75110J	MC75S110L	
DS75110N	MC75S110P	
DS75121J	MC8T13L	
DS75121N	MC8T13P	
DS75122J	MC8T14L	
DS75122N	MC8T14P	
DS75123J	MC8T23L	
DS75123N	MC8T23P	
DS75124J	MC8T24L	
DS75124N	MC8T24P	
DS75207J		MC75107L
DS75207N		MC75107P
DS75208J		MC75108L
DS75208N		MC75108P
DS75325J	MC75325L	
DS75325N	MC75325P	
DS75450J	MC75450L	
DS75450N	MC75450P	
DS75451H		MC75451U
DS75451N	SN75451BP	
DS75452H		MC75452U
DS75452N	SN75452BP	
DS75453H		MC75453U
DS75453N	SN75453BP	
DS75454H		MC75454U
DS75454N	SN75454BP	
DS75461H		MC75461U
DS75461N	MC75461P	
DS75462H		MC75462U
DS75462N	MC75462P	
DS75463H		MC75463U
DS75463N	MC75463P	
DS75464H		MC75464U
DS75464N	MC75464P	
DS75491J		MC75491P
DS75491N	MC75491P	
DS75492J		MC75492P
DS75492N	MC75492P	
DS7837J		MC3437L
DS7837W		MC3437L
DS7838J		MC3438L
DS7838W		MC3438L
DS7887J		MC3490P
DS7889J		MC3491P
DS7897J		MC3494P
DS8833J		MC8T28L
DS8833N		MC8T28P
DS8834J		MC8T26AL
DS8834N		MC8T26AP
DS8835J		MC8T26AL
DS8835N		MC8T26AP
DS8837J	MC3437L	
DS8837N	MC3437P	
DS8838J	MC3438L	
DS8838N	MC3438P	
DS8839J		MC8T28L
DS8839N		MC8T28P
DS8887J		MC3490P
DS8887N		MC3490P
DS8889J		MC3491P
DS8889N		MC3491P
DS8897J		MC3494P
DS8897N		MC3494P

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
HA1199	HA1199	
ICB8000C		LM111J
ICB8001C		LM111J
ICB8741C		MC1741CG
ICH8500ATV		MC1776CG
ICH8500TV		MC1776CG
ICL101ALNDP		LM101AH
ICL101ALNFB		LM101AH
ICL101ALNTY		LM101AH
ICL301ALNPA		LM301AH
ICL301ALNTY		LM301AH
ICL741CLNPA		MC1741CP1
ICL741CLNTY		MC1741CP1
ICL741LNDP		MC1741L
ICL741LNFB		MC1741L
ICL741LNTY		MC1741L
ICL8001CTZ		LM111J
ICL8001MTZ		LM111J
ICL8007CTA		MC1709CG
ICL8007MTA		MC1709CG
ICL8008CPA		LM301AN
ICL8008CTY		LM301AN
ICL8013A		MC1594G
ICL8013B		MC1594G
ICL8013C		MC1594G
ICL8017CTW		LM301AN
ICL8017MTW		LM301AN
ICL8021C		MC1776G
ICL8021M		MC1776G
ICL8022C		MC1776G
ICL8022M		MC1776G
ICL8043CDE		MC1776G
ICL8043CPE		MC1776G
ICL8043MDE		MC1776G
ICL8048CDE		MC1776G
ICL8048DPE		MC1776G
IH5101IIE		MC1545G
IH5101MIE		MC1545G
ITT641		MC1385P
ITT652	MC1411P	
ITT654	MC1412P	
ITT656	MC1413P	
ITT1330	MC1330P	
ITT1352	MC1352P	
ITT3064	MC1364P	
ITT3065	MC1358P	
ITT3066		MC1399P
ITT3701		TDA1190Z
ITT3707		MC1399P
ITT3710		MC1391P
ITT3714		MC1394P
L144AP		LM324N
L201	MC1411P	
L202	MC1412P	
L203	MC1413P	
LD111CJ	MC1405L	
LF152D		LF155J
LF155AH	LF155AH	
LF155AJG	LF155AJ	
LF155AL	LF155AH	
LF155H	LF155H	
LF155JG	LF155J	
LF155L	LF155H	
LF156AH	LF156AH	
LF156AJG	LF156AJ	
LF156AL	LF156AH	
LF156H	LF156H	
LF156JG	LF156J	
LF156L	LF156H	
LF157AH	LF157AH	
LF157AJG	LF157AJ	
LF157AL	LF157AH	
LF157H	LF157H	
LF157JG	LF157J	
LF157L	LF157H	
LF252D		LF255J
LF255H	LF255H	
LF255JG	LF255J	
LF255L	LF255H	
LF255P	LF255J	
LF256H	LF256H	
LF256JG	LF256J	
LF256L	LF256H	
LF256P	LF256J	
LF257H	LF257H	
LF257JG	LF257J	
LF257L	LF257H	
LF257P	LF257J	
LF347N	MC34004P	
LF347AN	MC34004AP	
LF347BN	MC34004BP	
LF351H	MC34001G	
LF351AH	MC34001AG	
LF351BH	MC34001BG	
LF351N	MC34001P	
LF351AN	MC34001AP	
LF351BN	MC34001BP	
LF352D		LF355J
LF353H	MC34002G	
LF353AH	MC34002AG	
LF353BH	MC34002BG	
LF353N	MC34002P	
LF353AN	MC34002AP	
LF353BN	MC34002BP	
LF355AH	LF355AH	
LF355AJG	LF355AJ	
LF355AL	LF355AH	
LF355AP	LF355AN	
LF355BH	LF355BH	
LF355BJ	LF355BJ	
LF355BN	LF355BN	
LF355H	LF355H	
LF355JG	LF355J	
LF355L	LF355H	
LF355N	LF355N	
LF355P	LF355N	
LF356AH	LF356AH	
LF356AL	LF356AH	
LF356AJG	LF356AJ	
LF356AP	LF356AN	
LF356BH	LF356BH	
LF356BJ	LF356BJ	
LF356BN	LF356BN	
LF356H	LF356H	
LF356JG	LF356J	
LF356L	LF356H	
LF356N	LF356N	
LF356P	LF356N	
LF357AH	LF357AH	
LF357BH	LF357BH	
LF357BJ	LF357BJ	
LF357BN	LF357BN	
LF357H	LF357H	
LF357JG	LF357J	
LF357L	LF357H	
LF357N	LF357N	
LF357P	LF357N	
LH0001ACH		MC1776CG
LH0001AH		MC1776G
LH0001ACD		MC1776CG
LH0001AD		MC1776G
LH0001ACF		MC1776CG
LH0001AF		MC1776G
LH0002CH		MC1538R
LH0002H		MC1538R
LH0004CH		MC1436G
LH0004H		MC1536G
LH0042CH		MC1776G
LH101F		MC1741F
LH101H		MC1741G
LH201F		MC1741F
LH201H		MC1741G
LH740ACH		LF355H
LH740AH		LF155H
LH2101AD		MC1537L
LH2101AF		MC1537L
LH2201AD		MC1537L
LH2201AF		MC1537L
LH2301AD		MC1437L
LH2301AF		MC1437L
LM100F		LM105H
LM100H		LM105H
LM101AD		LM101AH
LM101AF		LM101AH
LM101AH	LM101AH	
LM101AJ		LM101AJ
LM101AJ-14		LM101AJ
LM101AJG	LM101AJ	
LM101AL	LM101AH	
LM101D		LM101AJ
LM101F		LM101AH
LM101H	LM101AH	
LM101J-14		LM101AJ
LM104F		LM104H
LM104H	LM104H	
LM104J		LM104H
LM104L	LM104H	
LM105F		LM105H
LM105H	LM105H	
LM105JG		LM105H
LM105L	LM105H	
LM106H		MC1710G
LM107F		LM107H
LM107H	LM107H	
LM107L	LM107H	
LM108AD	LM108AJ	
LM108AF	LM108AF	
LM108AH	LM108AH	
LM108AJ	LM108J-8	
LM108D	LM108J	
LM108F	LM108F	
LM108H	LM108H	
LM109H	LM109H	
LM109K	LM109K	
LM109LA	LM109K	
LM111D	LM111J	
LM111H	LM111H	
LM112D		MC1556L
LM112F		MC1556L
LM112H		MC1556G
LM117H	LM117H	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM117K	LM117K	
LM118D		MC1741SL
LM118F		MC1741SL
LM118H		MC1741SG
LM120H-5 0	LM120H-5.0	
LM120H-5.2		MC7905.2CK
LM120H-6 0	LM120H-6.0	
LM120H-8 0	LM120H-8.0	
LM120H-12	LM120H-12	
LM120H-15	LM120H-15	
LM120H-18	LM120H-18	
LM120H-24	LM120H-24	
LM120K-5.0	LM120K-5 0	
LM120K-5.2		MC7905 2CK
LM120K-6 0	LM120K-6 0	
LM120K-8.0	LM120K-8 0	
LM120K-12	LM120K-12	
LM120K-15	LM120K-15	
LM120K-18	LM120K-18	
LM120K-24	LM120K-24	
LM122F		MC1555G
LM122H		MC1555G
LM124AD		LM124J
LM124AF		LM124J
LM124AJ		LM124J
LM124D	LM124J	
LM124F		LM124J
LM124J	LM124J	
LM125H		MC1568G
LM126H		MC1568G
LM128H		MC1568G
LM139AD	LM139AJ	
LM139AJ	LM139AJ	
LM139D	LM139J	
LM139J	LM139J	
LM140K-5 0	LM140K-5 0	
LM140K-6 0	LM140K-6.0	
LM140K-8 0	LM140K-8.0	
LM140K-12	LM140K-12	
LM140K-15	LM140K-15	
LM140K-18	LM140K-18	
LM140K-24	LM140K-24	
LM140LAH-5 0		MC78L05ACG
LM140LAH-6 0		MC78L06ACG
LM140LAH-8 0		MC78L08ACG
LM140LAH-12		MC78L12ACG
LM140LAH-15		MC78L15ACG
LM140LAH-18		MC78L18ACG
LM140LAH-24		MC78L24ACG
LM143D		MC1536G
LM143F		MC1536G
LM143H		MC1536G
LM145K		MC7905CK
LM148D	LM148J	
LM148J	LM148J	
LM148F		MC4741L
LM149D		MC4741L
LM149F		MC4741L
LM158AH		LM158H
LM158H	LM158H	
LM158JG	LM158J	
LM158L	LM158H	
LM163J		MC3450L
LM171H		MC1590G
LM200F		LM205H
LM200H		LM205H
LM201AD		LM201AJ

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM201AF		LM201AH
LM201AH	LM201AH	
LM201AJ		LM201AJ
LM201AJG	LM201AJ	
LM201AL	LM201AH	
LM201AN		LM201AN
LM201AP	LM201AN	
LM201AJ-14		LM201AJ
LM201D		LM201AJ
LM201F		LM201AH
LM201H	LM201AH	
LM201J	LM201AJ	
LM201J-14		LM201AJ
LM204H	LM204H	
LM204F		LM204H
LM205F		LM205H
LM205H	LM205H	
LM206H		MC1710CG
LM207F		LM207H
LM207H	LM207H	
LM208AD	LM208AJ	
LM208AF	LM208AF	
LM208AH	LM208AH	
LM208AJ	LM208AJ-8	
LM208D		LM208J-8
LM208F	LM208F	
LM208H	LM208H	
LM209K	LM209K	
LM209H	LM209H	
LM211D	LM211J	
LM211H	LM211H	
LM212D		MC1556L
LM212F		MC1556L
LM212H		MC1456G
LM217H	LM217H	
LM217K	LM217K	
LM218D		MC1741SL
LM218F		MC1741SL
LM218H		MC1741SG
LM220H-5 0		MC7905CK
LM220H-5.2		MC7905 2CK
LM220H-6 0		MC7906CK
LM220H-8 0		MC7908CK
LM220H-12		MC7912CK
LM220H-15		MC7915CK
LM220H-18		MC7918CK
LM220H-24		MC7924CK
LM220K-5.0		MC7905CK
LM220K-5.2		MC7905.2CK
LM220K-6 0		MC7906CK
LM220K-8.0		MC7908CK
LM220K-12		MC7912CK
LM220K-15		MC7915CK
LM220K-18		MC7918CK
LM220K-24		MC7924CK
LM222H		MC1555G
LM224AD		LM224J
LM224AF		LM224J
LM224AJ		LM224J
LM224D	LM224J	
LM224F		LM224L
LM224J	LM224J	
LM225H		MC1568G
LM226H		MC1568G
LM228H		MC1568G
LM239AD	LM239AJ	
LM239AJ	LM239AJ	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM239D	LM239J	
LM239J	LM239J	
LM240LAH-5.0		MC78L05ACG
LM240LAH-6.0		MC78L06CG
LM240LAH-8 0		MC78L08ACG
LM240LAH-12		MC78L12ACG
LM240LAH-15		MC78L15ACG
LM240LAH-18		MC78L18ACG
LM240LAH-24		MC78L24ACG
LM240LAZ-5 0		MC78L05ACP
LM240LAZ-6 0		MC78L06ACP
LM240LAZ-8 0		MC78L08ACP
LM240LAZ-12		MC78L12ACP
LM240LAZ-15		MC78L15ACP
LM240LAZ-18		MC78L18ACP
LM240LAZ-24		MC78L24ACP
LM243H		MC1536G
LM245K		MC7905CK
LM248D	LM248J	
LM248J	LM248J	
LM249D		MC4741L
LM249J		MC4741L
LM258AH		LM258H
LM258H	LM258H	
LM2901N	LM2901N	
LM300F		LM305H
LM271H		MC1590G
LM300H		LM305H
LM301AD		LM301AJ
LM301AF		LM301AH
LM301AH	LM301AH	
LM301AJ	LM301AJ	
LM301AJG	LM301AJ	
LM301AL	LM301AH	
LM301AN	LM301AN	
LM301AP	LM301AN	
LM302H	LM310H	
LM304F		LM304H
LM304H	LM304H	
LM304J		LM304H
LM304L	LM304H	
LM304N		LM304H
LM305AH		LM305H
LM305AJG		LM305H
LM305AL		LM305H
LM305AP		LM305H
LM305F		LM305H
LM305H	LM305H	
LM305JG		LM305H
LM305L	LM305H	
LM305P		LM305H
LM306H		MC1710CG
LM307F		LM307H
LM307H	LM307H	
LM307L	LM307H	
LM307N	LM307N	
LM307P	LM307N	
LM308AD	LM308AJ	
LM308AF		LM308AJ
LM308AH	LM308AH	
LM308AH-1		LM308AH
LM308AH-2		LM308AH
LM308AJ	LM308AJ-8	
LM308D	LM308J	
LM308H	LM308H	
LM308N	LM308N	
LM309H	LM309H	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM309K	LM309K	
LM309KC	LM309K	
LM309LA	LM309K	
LM311D	LM311J	
LM311H	LM311H	
LM311N	LM311N	
LM311N-14	LM311J	
LM312D		MC1456L
LM312F		MC1456L
LM312H		MC1456G
LM317H	LM317H	
LM317K	LM317K	
LM317P	LM317T	
LM317T	LM317T	
LM318D		MC1741SCL
LM318F		MC1741SCL
LM318H		MC1741SCG
LM318N		MC1741SCP1
LM320H-5 0	LM320H-5 0	
LM320H-5.2		MC7905 2CK
LM320H-6 0	LM320H-6.0	
LM320H-8 0	LM520H-8 0	
LM320H-12	LM320H-12	
LM320H-15	LM320H-15	
LM320H-18	LM320H-18	
LM320H-24	LM320H-24	
LM320K-5.0	LM320K-5.0	
LM320K-6.0	LM320K-6 0	
LM320K-8 0	LM320K-8 0	
LM320K-12	LM320K-12	
LM320K-15	LM320K-15	
LM320K-18	LM320K-18	
LM320K-24	LM320K-24	
LM320MP-5 0		MC7905CT
LM320MP-5 2		MC7905 2CT
LM320MP-6 0		MC7906CT
LM320MP-8 0		MC7908CT
LM320MP-12		MC7912CT
LM320MP-15		MC7915CT
LM320MP-18		MC7918CT
LM320MP-24		MC7924CT
LM320T-5 0	LM320T-5.0	
LM320T-5 2		MC7905 2CT
LM320T-6.0	LM320T-6 0	
LM320T-8 0	LM320T-8 0	
LM320T-12	LM320T-12	
LM320T-15	LM320T-15	
LM320T-18	LM320T-18	
LM320T-24	LM320T-24	
LM322H		MC1455G
LM322N		MC1455P1
LM324AJ		LM324J
LM324AN		LM324N
LM324J	LM324J	
LM324N	LM324N	MC3403P
LM325AN		MC1468L
LM325H		MC1468G
LM325N		MC1468L
LM326H		MC1468G
LM326N		MC1468L
LM328AN		MC1468L
LM328H		MC1468G
LM328N		MC1468L
LM339AD	LM339AJ	
LM339AN	LM339AN	
LM339N	LM339N	
LM340K-5.0	LM340K-5 0	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM340K-6.0	LM340K-6 0	
LM340K-8 0	LM340K-8 0	
LM340K-12	LM340K-12	
LM340K-15	LM340K-15	
LM340K-18	LM340K-18	
LM340K-24	LM340K-24	
LM340KC-5 0	MC7805CK	
LM340KC-6 0	MC7806CK	
LM340KC-8 0	MC7808CK	
LM340KC-12	MC7812CK	
LM340KC-15	MC7815CK	
LM340KC-18	MC7818CK	
LM340KC-24	MC7824CK	
LM340LAH-5 0		MC78L05ACG
LM340LAH-6 0		MC78L06ACG
LM340LAH-8 0		MC78L08ACG
LM340LAH-12		MC78L12ACG
LM340LAH-15		MC78L15ACG
LM340LAH-18		MC78L18ACG
LM340LAH-24		MC78L24ACG
LM340LAZ-5 0		MC78L05ACP
LM340LAZ-6 0		MC78L06ACP
LM340LAZ-8 0		MC78L08ACP
LM340LAZ-12		MC78L12ACP
LM340LAZ-15		MC78L15ACP
LM340LAZ-18		MC78L18ACP
LM340LAZ-24		MC78L24ACP
LM340T-5 0	MC7805CT	
LM340T-6 0	MC7806CT	
LM340T-8 0	MC7808CT	
LM340T-12	MC7812CT	
LM340T-15	MC7815CT	
LM340T-18	MC7818CT	
LM340T-24	MC7824CT	
LM341P-5 0	MC78M05CT	
LM341P-6 0	MC78M06CT	
LM341P-8 0	MC78M08CT	
LM341P-12	MC78M12CT	
LM341P-15	MC78M15CT	
LM341P-18	MC78M18CT	
LM341P-24	MC78M24CT	
LM342P-5 0	MC78M05CT	
LM342P-6 0	MC78M06CT	
LM342P-8 0	MC78M08CT	
LM342P-12	MC78M12CT	
LM342P-15	MC78M15CT	
LM342P-18	MC78M18CT	
LM342P-24	MC78M24CT	
LM343D		MC1436G
LM343H		MC1436G
LM345K		MC7905CK
LM348D	LM348J	
LM348J	LM348J	
LM348N	LM348N	
LM349D		MC4741CL
LM349J		MC4741CL
LM349N		MC4741CL
LM358AH		LM358H
LM358AN		LM358N
LM358H	LM358H	
LM358JG	LM358J	
LM358L	LM358H	
LM358N	LM358N	
LM358P	LM358N	
LM363AJ		MC3450L
LM363AN		MC3450P
LM363J		MC3450L

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM363N		MC3450P
LM371H		MC1590G
LM376JG		LM305H
LM376L	LM305H	
LM376N		LM305H
LM376P		LM305H
LM386N		MC1306P
LM555CH	MC1455G	
LM555CN	MC1455P1	
LM555H	MC1555G	
LM556CD	MC3456L	
LM556CJ	MC3456L	
LM556CN	MC3456P	
LM556D	MC3556L	
LM556J	MC3556L	
LM565CH		NE565N
LM565CN	NE565N	
LM565H		NE565N
LM703LN		MC1350P
LM709AH	MC1709AG	
LM709AJ	MC1709AL	
LM709CH	MC1709CG	
LM709CJ	MC1709CL	
LM709CN	MC1709CP2	
LM709CN-8	MC1709CP1	
LM709H	MC1709G	
LM709J	MC1709L	
LM710CH	MC1710CG	
LM710CN	MC1710CP	
LM710H	MC1710G	
LM711CH	MC1711CG	
LM711CN	MC1711CP	
LM711H	MC1711G	
LM723CD	LM723CJ	
LM723CH	LM723CH	
LM723CJ	LM723CJ	
LM723CN	LM723CN	
LM723D	LM723J	
LM723H	LM723H	
LM723J	LM723J	
LM733CD	MC1733CL	
LM733CH	MC1733CG	
LM733CJ	MC1733CL	
LM733CN	MC1733CP	
LM733D	MC1733L	
LM733H	MC1733G	
LM733J	MC1733L	
LM741AD		MC1741L
LM741AF		MC1741F
LM741AH		MC1741G
LM741AJ-14		MC1741L
LM741CD	LM1741CJ	
LM741CF	LM741CF	
LM741CH	LM741CH	
LM741CJ	LM741CJ	
LM741CJ-14	LM741CJ-14	
LM741CN	LM741CN	
LM741CN-14	LM741CN-14	
LM741D	LM741J-14	
LM741ED		MC1741CL
LM741EH		MC1741CG
LM741EJ		MC1741CU
LM741EJ-14		MC1741CL
LM741EN		MC1741CP1
LM741F	LM741F	
LM741H	LM741H	
LM741J-14	LM741J-14	

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PART NO	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM746N		MC1323P
LM747CD	LM747CJ	
LM747CF	LM747CF	
LM747CH	LM747CH	
LM747CJ	LM747CJ	
LM747CN	LM747CN	
LM747D	LM747J	
LM747F	LM747F	
LM747H	LM747H	
LM747J	LM747J	
LM748CH	MC1748CG	
LM748CJ	MC1748CU	
LM748CN	MC1748CP1	
LM748H	MC1748G	
LM748J	MC1748U	
LM1310N	MC1310P	
LM1351N	MC1351P	
LM1391N	MC1391P	
LM1394N	MC1394P	
LM1414J	MC1414L	
LM1414N	MC1414P	
LM1458H	MC1458G	
LM1458J	MC1458U	
LM1458N	MC1458P1	
LM1458N-14	MC1458P2	
LM1488J	MC1488L	
LM1488N	MC1488P	
LM1489AJ	MC1489AL	
LM1489AN	MC1489AP	
LM1489J	MC1489L	
LM1489N	MC1489P	
LM1496H	MC1496G	
LM1496J	MC1496L	
LM1496N	MC1496P	
LM1514J	MC1514L	
LM1558H	MC1558G	
LM1558J	MC1558U	
LM1596H	MC1596G	
LM1596J	MC1596L	
LM1800AN		MC1310P
LM1800N		MC1310P
LM1805		MC1385P
LM1808N		TDA1190Z
LM1828N		MC1323P
LM1841N	MC1356P	
LM1845N		MC1344P
LM1848N		MC1323P
LM1850N		MC3426L
LM1900D		MC3301L
LM2111N	MC1357P	
LM2113N		MC1357P
LM2900J		MC3301L
LM2900N		MC3301P
LM2902J	LM2902J	
LM2902N	LM2902N	
LM2904N	LM2904N	
LM2905N		MC1455P1
LM3011H		MC1550G
LM3026		CA3054
LM3045		MC3346P
LM3046N	MC3346P	
LM3054	CA3054	
LM3064N	MC1364P	
LM3065N	MC1358P	
LM3066N		MC1399P
LM3067N		MC1323P
LM3070N		MC1399P

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM3071N		MC1399P
LM3075N	MC1375P	
LM3086N	MC3386P	
LM3126		MC1399P
LM3146		MC3346P
LM3146A		MC3346P
LM3301N	MC3301P	
LM3302J	MC3302L	
LM3302N	MC3302P	
LM3401N	MC3401P	
LM3900N		MC3401P
LM3905N		MC1455P1
LM4250CH		MC1776CG
LM4250CN		MC1776CP1
LM4250H		MC1776G
LM5525J	MC5525L	
LM5528J	MC5528L	
LM5529J	MC5529L	
LM5534J	MC5534L	
LM5535J	MC5535L	
LM5538J	MC5538L	
LM5529J	MC5539L	
LM7524J	MC7524L	
LM7524N	MC7524P	
LM7525J	MC7525L	
LM7805KC	MC7805CK	
LM7806KC	MC7806CK	
LM7808KC	MC7808CK	
LM7812KC	MC7812CK	
LM7815KC	MC7815CK	
LM7818KC	MC7818CK	
LM7824KC	MC7824CK	
LM78L05ACH	MC78L05ACG	
LM78L05ACZ	MC78L05ACP	
LM78L05CH	MC78L05CG	
LM78L05CZ	MC78L05CP	
LM78L08ACH	MC78L08ACG	
LM78L08ACZ	MC78L08ACP	
LM78L08CH	MC78L08CG	
LM78L08CZ	MC78L08CP	
LM78L12ACH	MC78L12ACG	
LM78L12ACZ	MC78L12ACP	
LM78L12CH	MC78L12CG	
LM78L12CZ	MC78L12CP	
LM78L15ACH	MC78L15ACG	
LM78L15ACZ	MC78L15ACP	
LM78L15CH	MC78L15CG	
LM78L15CZ	MC78L15CP	
LM78L18ACH	MC78L18ACG	
LM78L18ACZ	MC78L18ACP	
LM78L18CH	MC78L18CG	
LM78L18CZ	MC78L18CP	
LM78L24ACH	MC78L24ACG	
LM78L24ACZ	MC78L24ACP	
LM78L24CH	MC78L24CG	
LM78L24CZ	MC78L24CP	
LM55107AJ	MC55107L	
LM55108AJ	MC55108L	
LM55109J		MC75S110L
LM55110J		MC75S110L
LM55121J		MC8T13L
LM55122J		MC8T14L
LM55123J		MC8T23L
LM55124J		MC8T24L
LM55325N	MC55325L	
LM75107AJ	MC75107L	
LM75107AN	MC75107P	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM75108AJ	MC75108L	
LM75108AN	MC75108P	
LM75110J	MC75S110L	
LM75110N	MC75S110P	
LM75121J	MC8T13L	
LM75121N	MC8T13P	
LM75122J	MC8T14L	
LM75122N	MC8T14P	
LM75123J	MC8T23L	
LM75123N	MC8T23P	
LM75124J	MC8T24L	
LM75124N	MC8T24P	
LM75207L		MC75107L
LM75207N		MC75107P
LM75208J		MC75108L
LM75208N		MC75108P
LM75324J		MC75325L
LM75324N		MC75325P
LM75325J	MC75325P	
LM75325N	MC75325L	
LM75450N	MC75450P	
LM75451N	MC75451P	
LM75452N	MC75452P	
LM75453N	MC75453P	
LM75454N	MC75454P	
MC1310A	MC1310P	
MC1408B	MC1408P8	
MC1408F	MC1408L8	
MC1458JG	MC1458U	
MC1458L	MC1458G	
MC1458P	MC1458P1	
MC1558JG	MC1558U	
MC1558L	MC1558G	
MH0026H		MMH0026CG
MH0026CH	MMH0026CG	
MH0026CN	MMH0026CP1	
MH0026G		MMH0026CG
MH0026CG		MMH0026CG
MH0026F		MMH0026CL
MH0026CF		MMH0026C1
MIC709-1	MC1709G	
MIC709-5	MC1709CG	
MIC710-1C	MC1710G	
MIC710-5C	MC1710CG	
MIC711-1C	MC1711G	
MIC711-5C	MC1711CG	
MIC712-1B	MC1712F	
MIC712-1C	MC1712G	
MIC712-1D	MC1712L	
MIC712-5B	MC1712CF	
MIC712-5C	MC1712CG	
MIC712-5D	MC1712CL	
MIC723-1	MC1723G	
MIC723-5	MC1723CG	
MIC741-1C	MC1741G	
MIC741-1D	MC1741L	
MIC741-5C	MC1741CG	
MIC741-5D	MC1741CL	
ML101AF		LM101AH
ML101AM		LM101AH
ML101AT	LM101AH	
ML101F		LM101AH
ML101M		LM101AH
ML101T	LM101AH	
ML107F		LM107H
ML107M		LM107H
ML107T	LM107H	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
ML108AF		MC1556G
ML108AM	LM108AJ	
ML108AT	LM108AH	
ML108M	LM108J	
ML108T	LM108H	
ML111M	LM111J	
ML111S		LM111J
ML111T	LM111H	
ML118F		MC1741SG
ML118M		MC1741SG
ML118T		MC1741SG
ML201AF		LM201AH
ML201AM		LM201AH
ML201AT	LM201AH	
ML201F		LM201AH
ML201M		LM201AH
ML201T	LM201AH	
ML207F		LM207H
ML207M		LM207H
ML207T	LM207H	
ML208AF		MC1556G
ML208AM	LM208AJ	
ML208AT	LM208AH	
ML208M	LM208J	
ML208T	LM208H	
ML211M	LM211J	
ML211S	LM211N	
ML211T	LM211H	
ML218F		MC1741SG
ML218M		MC1741SG
ML218T		MC1741SG
ML301AP		LM301AN
ML301AS	LM301AN	
ML301AT	LM301AH	
ML301P		LM301AN
ML301S	LM301AN	
ML301T	LM301AN	
ML307P		LM307H
ML307S	LM307N	
ML307T	LM307H	
ML308AM	LM308AJ	
ML308AT	LM308AH	
ML308M	LM308J	
ML308T	LM308H	
ML311M	LM311J	
ML311P	LM311J	
ML311S	LM311N	
ML311T	LM311H	
ML318M		MC1741SCP1
ML318T		MC1741SCG
ML709AF	MC1709AF	
ML709AM	MC1709AL	
ML709AT	MC1709AG	
ML709CP	MC1709CP2	
ML709CT	MC1709CG	
ML709F	MC1709F	
ML709M	MC1709L	
ML709T	MC1709G	
ML723CF		MC1723CL
ML723CM	MC1723CL	
ML723CP	MC1723CL	
ML723CT	MC1723CG	
ML723F		MC1723L
ML723M	MC1723L	
ML723T	MC1723G	
ML741AF		MC1556G
ML741AM		MC1556G

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
ML741AT		MC1556G
ML741CP	MC1741CP2	
ML741CS	MC1741CP1	
ML741CT	MC1741CG	
ML741F	MC1741F	
ML741M	MC1741L	
ML741T	MC1741G	
ML747CP	MC1747CL	
ML747CT	MC1747CG	
ML747F	MC1747F	
ML747M	MC1747L	
ML747T	MC1747G	
ML748CP		LM301AN
ML748CS	LM301AN	
ML748CT	MC1748CG	
ML748F		MC1748G
ML748M		MC1748G
ML748T	MC1748G	
ML1436T	MC1436G	
ML1437P	MC1437P	
ML1458P	MC1458P2	
ML1458S	MC1458P1	
ML1458T	MC1458G	
ML1488M	MC1488L	
ML1489AM	MC1489AL	
ML1489M	MC1489L	
ML1536T	MC1536G	
ML1537M	MC1537L	
ML1558M	MC1558L	
ML1558T	MC1558G	
ML3046P	MC3346P	
ML4250T		MC1776G
ML4250CS		MC1776CG
ML4250CT		MC1776CG
ML4251T		MC1776G
ML4251CS		MC1776CG
ML4251CT		MC1776CG
ML6503M		MC1537L
ML7503M		MC1437L
N5065A	MC1358P	
N5070B		MC1399P
N5071A		MC1399P
N5072A		MC1323P
N5556T	MC1456G	
N5556V	MC1456P1	
N5558F	MC1458L	
N5558T	MC1458G	
N5558V	MC1458P1	
N5595A	MC1495L	
N5595F	MC1495L	
N5596A	MC1496L	
N5596K	MC1496G	
N5709A	MC1709CP2	
N5709G	MC1709CF	
N5709T	MC1709CG	
N5709V	MC1709CP1	
N5710A	MC1710CP	
N5710T	MC1710CG	
N5711A	MC1711CP	
N5711K	MC1711CG	
N5723A		MC1723CP
N5723T	MC1723CG	
N5733K	MC1733CG	
N5741A	MC1741CP2	
N5741T	MC1741CG	
N5741V	MC1741CP1	
N5747A	MC1747CL	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
N5747F	MC1747CL	
N5748A		MC1747CG
N5748T	MC1748CG	
N8T13B	MC8T13P	
N8T13P	MC8T13L	
N8T14B	MC8T14P	
N8T14E	MC8T14L	
N8T15A		MC1488L
N8T15F		MC1488L
N8T16A		MC1489L
N8T23B	MC8T23P	
N8T23E	MC8T23L	
N8T24B	MC8T24P	
N8T24E	MC8T24L	
N8T26AB	MC8T26AP	
N8T26AE	MC8T26AL	
N8T26B	MC8T26AP	
N8T28B	MC8T28P	
N8T37A	MC3437P	
N8T38A	MC3438P	
N8T95B	MC8T95P	
N8T95F	MC8T95L	
N8T96B	MC8T96P	
N8T96F	MC8T96L	
N8T97B	MC8T97P	
N8T97F	MC8T97L	
N8T98B	MC8T98P	
N8T98F	MC8T98L	
NE501A		MC1733CL
NE501K		MC1733CG
NE515A		MC1420G
NE515G		MC1520F
NE515K		MC1420G
NE516A		MC1420G
NE516G		MC1520F
NE516K		MC1420G
NE531G		MC1439G
NE531T		MC1439G
NE531V		MC1439P
NE533G		MC1776CG
NE533T		MC1776CG
NE533V		MC1776CG
NE537G		MC1456G
NE537T		MC1456G
NE540L		MC1554G
NE550A		MC1723CP
NE550L		MC1723CG
NE555JG	MC1455U	
NE555L	MC1455G	
NE555P	MC1455P1	
NE555T	MC1455G	
NE555V	MC1455P1	
NE556A	MC3456P	
NE556I	MC3456L	
NE565A	NE565N	
NE565K		NE565N
NE592A	NE592A	
NE592K	NE592K	
OP-01C		MC1536
OP-01G		MC1536
OP-01H		MC1536
OP-01J		MC1536G
OP-01L		MC1536G
OP-01P		MC1536P
OP-08		MC1776
OP-08A		MC1776
OP-08B		MC1776

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
OP-08C		MC1776
OP-08E		MC1776
PA239A		MC1303P
RC702T	MC1712CG	
RC709D	MC1709CL	
RC709DN	MC1709CP1	
RC709DP	MC1709CP2	
RC709T	MC1709CG	
RC710DC	MC1710CL	
RC710DP	MC1710CP	
RC710T	MC1710CG	
RC711DC	MC1711CL	
RC711DP	MC1711CP	
RC711T	MC1711CG	
RC723D	MC1723CL	
RC723T	MC1723CG	
RC733D	MC1733CL	
RC733T	MC1733CG	
RC741D	MC1741CL	
RC741DN	MC1741CP1	
RC741DP	MC1741CP2	
RC741Q	MC1741CF	
RC741T	MC1741CG	
RC747D	MC1747CL	
RC747T	MC1747CG	
RC748T	MC1748CG	
RC1414DC	MC1414L	
RC1414DP	MC1414P	
RC1488DC	MC1488L	
RC1489ADC	MC1489AL	
RC1489DC	MC1489L	
RC8T13DD	MC8T13L	
RC1437D	MC1437L	
RC1437DP	MC1437P	
RC1458DN	MC1458P1	
RC1458T	MC1458G	
RC1556T	MC1456CG	
RC1558T	MC1558G	
RC3302DB	MC3302P	
RC4131DP		MC1471SCP1
RC4131T		MC1741SG
RC4136D		MC3403L
RC4136DP		MC3403P
RC4136J		MC3403L
RC4136N		MC3403P
RC4195T		MC1468G
RC4195TK		MC1468R
RC4444R	MC3416L	
RC4558DN	MC4558CP1	
RC4558JG	MC4558CU	
RC4558L	MC4558CG	
RC4558P	MC4558CP1	
RC4558T	MC4558CG	
RC8T13MP	MC8T13P	
RC8T14DD	MC8T14L	
RC8T14MP	MC8T14P	
RC8T23DD	MC8T23L	
RC8T23MP	MC8T23P	
RC8T24DD	MC8T24L	
RC8T24MP	MC8T24P	
RC75107AD	MC75107L	
RC75107ADP	MC75107P	
RC75108AD	MC75108L	
RC75108ADP	MC75108P	
RC75109D		MC75S110L
RC75109DP		MC75S110P
RC75110D	MC75S110L	
RC75110DP	MC75S110P	
RC75325DD	MC75325L	
REF-01CJ		C1404U10
REF-01DJ		C1404U10
REF-01J		C1504AU10
REF-01HJ		C1404AU10
REF-02CJ		C1404U5
REF-02DJ		C1404U5
REF-02HJ		C1404AU5
REF-02J		C1504AU5
RM702Q	MC1712F	
RM702T	MC1721G	
RM709D	MC1709L	
RM709Q	MC1709F	
RM709T	MC1709G	
RM710D	MC1710L	
RM710T	MC1710G	
RM711DC	MC1711L	
RM711T	MC1711G	
RM723D	MC1723L	
RM723T	MC1723G	
RM733D	MC1733L	
RM733T	MC1733G	
RM741D	MC1741L	
RM741DP	MC1741P	
RM741Q	MC1741F	
RM741T	MC1741G	
RM747D	MC1747L	
RM747T	MC1747G	
RM748T	MC1748G	
RM1514DC	MC1514L	
RM1537D	MC1537L	
RM4136D		MC3503L
RM4136J		MC3503L
RM4195T		MC1568G
RM4195TK		MC1568R
RM4558D	MC4558U	
RM4558JG	MC4558U	
RM4558L	MC4558G	
RM4558T	MC4558G	
RM55107AD	MC55107L	
RM55325DD	MC55325L	
RV3301DB	MC3301P	
S8T13E		MC8T13L
S8T14E		MC8T14L
S5556T	MC1556G	
S5558E	MC1558L	
S5558T	MC1558G	
S5596F	MC1596L	
S5596K	MC1596G	
S5709G	MC1709F	
S5709T	MC1709G	
S5710T	MC1710G	
S5711K	MC1711G	
S5723T	MC1723G	
S5733K	MC1733G	
S5741T	MC1741G	
SE501K		MC1733G
SE515G		MC1520F
SE515K		MC1520G
SE516A		MC1520G
SE516G		MC1520F
SE516K		MC1520G
SE528E		MC1544L
SE528R		MC1544L
SE531G		MC1539G
SE531T		MC1539G
SE533G		MC1776G
SE533T		MC1776G
SE537G		MC1556G
SE537T		MC1556G
SE550L		MC1723G
SE555JG	MC1555U	
SE555L	MC1555G	
SE555T	MC1555G	
SE556A	MC3556L	
SE565A		MLM565CP
SE565K		MLM565CP
SE592A	SE592L	
SE592K	SE592G	
SG100T		MC1723G
SG101AD		LM101AH
SG101AT	LM101AH	
SG101J		LM101AH
SG101T	LM101AH	
SG104T	LM104H	
SG105N		LM105H
SG105T	LM105H	
SG107J		LM107H
SG107T	LM107H	
SG108AJ	LM108AJ	
SG108AT	LM108AH	
SG108J	LM108J	
SG108T	LM108H	
SG109K	LM109K	
SG109T	LM109H	
SG111D	LM111J	
SG111T	LM111H	
SG118J		MC1741SL
SG118T		MC1741SG
SG120K-05	LM120K-05	
SG120K-5 2		MC7905.2CK
SG120K-12	LM120K-12	
SG120K-15	LM120K-15	
SG120T-05	LM120T-05	
SG120T-5 2		MC7905 2CK
SG120T-12	LM120T-12	
SG120T-15	LM120T-15	
SG124J	LM124J	
SG140K-05	LM140K-5.0	
SG140K-06	LM140K-6 0	
SG140K-08	LM140K-8 0	
SG140K-12	LM140K-12	
SG140K-15	LM140K-15	
SG140K-18	LM140K-18	
SG140K-24	LM140K-24	
SG200T		MC1723G
SG201AD		LM201AH
SG201AM	LM201AN	
SG201AN		LM201AN
SG201AT	LM201AH	
SG201J		LM201AH
SG201M	LM201AN	
SG201N		LM201AN
SG201T	LM201AH	
SG204T	LM204H	
SG205N		LM205H
SG205T	LM205H	
SG207J		LM207H
SG207M		LM207H
SG207N		LM207H
SG207T	LM207H	
SG208AJ	LM208AJ	
SG208AM	LM208AJ-8	

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PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SG208AT	LM208AH	
SG208J	LM208J	
SG208M	LM208J-8	
SG208T	LM208H	
SG209K	LM209K	
SG209T	LM209H	
SG211D	LM211J	
SG211M	LM211N	
SG211T	LM211H	
SG218J		MC1741SL
SG218M		MC1741SL
SG218T		MC1741SG
SG224J	LM224J	
SG224N	LM224N	
SG300N		MC1723CP
SG300T		MC1723CG
SG301AD		LM301AH
SG301AM	LM301AN	
SG301AN		LM301AN
SG301AT	LM301AH	
SG304T	LM304H	
SG305AT		LM305H
SG305N		LM305H
SG305T	LM305H	
SG307J		LM307N
SG307M	LM307N	
SG307N		LM307N
SG307T	LM307H	
SG308AJ	LM308AJ	
SG308AM	LM308AN	
SG308AT	LM308AH	
SG308J	LM308J	
SG308M	LM308N	
SG308T	LM308H	
SG309K	LM309K	
SG309T	LM309H	
SG311D	LM311J	
SG311M	LM311N	
SG311T	LM311H	
SG318J		MC1741SCL
SG318M		MC1741CP1
SG318T		MC1741CG
SG320K-05	LM320K-5 0	
SG320K-5 2		MC7905 2CK
SG320K-12	LM320K-12	
SG320K-15	LM320K-15	
SG320T-05	LM320T-5 0	
SG320T-5 2		MC7905 2CT
SG320T-12	LM320T-12	
SG320T-15	LM320T-15	
SG324J	LM324J	
SG324N	LM324N	
SG340K-05	MC7805CK	
SG340K-06	MC7806CK	
SG340K-08	MC7808CK	
SG340K-12	MC7812CK	
SG340K-15	MC7815CK	
SG340K-18	MC7818CK	
SG340K-24	MC7824CK	
SG555CM	MC1455P1	
SG555CT	MC1455G	
SG555T	MC1555G	
SG556CJ	MC3456L	
SG556CN	MC3456P	
SG556J	MC3556L	
SG556N	MC3556L	
SG710CD	MC1710CL	
SG710CN	MC1710CP	
SG710CT	MC1710CG	
SG710D	MC1710L	
SG710N	MC1710CP	
SG710T	MC1710G	
SG711CD	MC1711CL	
SG711CN	MC1711CP	
SG711CT	MC1711CG	
SG711D	MC1711L	
SG711N	MC1711CP	
SG711T	MC1711G	
SG723CD	MC1723CL	
SG723CN	MC1723CP	
SG723CT	MC1723CG	
SG723D	MC1723L	
SG723T	MC1723G	
SG733CD	MC1733CL	
SG733CN		MC1733CP
SG733CT	MC1733CG	
SG733D	MC1733L	
SG733N		MC1733L
SG733T	MC1733G	
SG741CD	MC1741CL	
SG741CF	MC1741CF	
SG741CM	MC1741CP1	
SG741CN	MC1741CP2	
SG741CT	MC1741CG	
SG741D	MC1741L	
SG741F	MC1741F	
SG741T	MC1741G	
SG741SCM	MC1741SCP1	
SG741SCT	MC1741SCG	
SG741ST	MC1741SG	
SG747CJ	MC1747CL	
SG747CN	MC1747CP2	
SG747CT	MC1747CG	
SG747J	MC1747L	
SG747T	MC1747G	
SG748CD		MC1748CP1
SG748CM		MC1748CP1
SG748CN		MC1748CP1
SG748CT	MC1748CG	
SG748D		MC1748G
SG748T	MC1748G	
SG777CJ		LM308AJ
SG777CM		LM308AN
SG777CN		LM308AN
SG777CT		LM308AH
SG777J		LM108AJ
SG777T		LM108AH
SG1118AJ		LM108AJ
SG1118AT		LM108AH
SG1118J		LM108J
SG1118T		LM108H
SG1217		MC1741G
SG1217J		MC1741SL
SG1217T		MC1741SG
SG1250T		MC1776G
SG1401N		MC1533G
SG1401T		MC1533G
SG1402N		MC1594L
SG1402T		MC1594L
SG1436CT	MC1436CG	
SG1436M	MC1436U	
SG1436T	MC1436G	
SG1456CT	MC1456CG	
SG1456T	MC1456G	
SG1458M	MC1458P1	
SG1458T	MC1458G	
SG1468J	MC1468L	
SG1468N	MC1468L	
SG1468T	MC1468G	
SG1495D	MC1495L	
SG1495N	MC1495L	
SG1496D	MC1496L	
SG1496N		MC1496L
SG1496T	MC1496G	
SG1501AD		MC1568L
SG1501AT		MC1568G
SG1501D	MC1568L	
SG1501T	MC1568G	
SG1502D		MC1568L
SG1502N		MC1568L
SG1503	MC1503U	
SG1524J		MC3520L
SG1536T	MC1536G	
SG1556T	MC1556G	
SG1558T	MC1558G	
SG1595D	MC1595L	
SG1596D	MC1596L	
SG1596T	MC1596G	
SG1660D		LM301AH
SG1660J		LM308J
SG1660M		LM308N
SG1660T		LM308H
SG1760D		LM307H
SG1760F		LM307H
SG1760J		LM308J
SG1760M		LM&08N
SG1760T		LM308H
SG2118AJ		LM208AJ
SG2118AM		LM208AJ-8
SG2118AT		LM208AH
SG2118J		LM208J
SG2118M		LM208J-8
SG2118T		LM208H
SG2250T		MC1776G
SG2401N		MC1433G
SG2402N		MC1494L
SG2402T		MC1494L
SG2501AD		MC1468L
SG2501AT		MC1468G
SG2501D	MC1468L	
SG2501N	MC1468L	
SG2501T	MC1468G	
SG2502D		MC1468L
SG2502N		MC1468L
SG2502T		MC1468G
SG2503	MC1403AU	
SG2524J		MC3520L
SG3118AJ		MLM308AL
SG3118AM		MLM308AP1
SG3118AT		MLM308AG
SG3118J		MLM308L
SG3118M		MLM308P1
SG3118T		MLM308G
SG3250T		MC1776G
SG3401N		MC1433G
SG3401T		MC1433G
SG3402N		MC1494L
SG3402T		MC1494L
SG3501AD	MC1468L	
SG3501AT	MC1468G	

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PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SG3501D	MC1468L	
SG3501N	MC1468L	
SG3501T	MC1468G	
SG3502D		MC1468L
SG3502G		MC1468G
SG3502N		MC1468L
SG3503	MC1403U	
SG3524J		MC3420L
SG4250CM		MC1776CP1
SG4250CT		MC1776CG
SG4250T		MC1776G
SG4501D	MC1468L	
SG4501N	MC1468L	
SG4501T	MC1468G	
SG7805CK	MC7805CK	
SG7805K		MC7805CK
SG7806CK	MC7806CK	
SG7806K		MC7806CK
SG7808CK	MC7808CK	
SG7808K		MC7808CK
SG7812CK	MC7812CK	
SG7812K		MC7812CK
SG7815CK	MC7815CK	
SG7815K		MC7815CK
SG7818CK	MC7818CK	
SG7818K		MC7818CK
SG7824CK	MC7824CK	
SG7824K		MC7824CK
SH0013HC		MMH0026CG
SH0013HM		MMH0026G
SH2001FC		MC75462P
SH2001FM		MC75462P
SH2001HC		MC75462P
SH2001HM		MC75462P
SH2002FC		MC75462P
SH2002FM		MC75462P
SH2002HC		MC75462P
SH2002HM		MC75462P
SH2002HC		MC75462P
SH2200FC		MC75462P
SH2200FM		MC75462P
SH2200HC		MC75462P
SH2200HM		MC75462P
SH2200PC		MC75462P
SH8090FM		MC1508L8
SN5510FA	MC1510F	
SN5510L	MC1510G	
SN52101AL	LM101AH	
SN52104L	LM101H	
SN52105L	LM105H	
SN52106J		MC1710L
SN52106L		MC1710G
SN52107L	LM107H	
SN52108AL	LM108AH	
SN52108L	LM108H	
SN52109L	LM109H	
SN52510J		MC1710L
SN52510L		MC1710G
SN52514J	MC1514L	
SN52555L	MC1555G	
SN52558L	MC1558G	
SN52702AFA		MC1712F
SN52702AJ		MC1712L
SN52702AL		MC1712G
SN52702FA	MC1712F	
SN52702J	MC1712L	
SN52702L	MC1712G	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SN52709AFA	MC1709AF	
SN52709AJ	MC1709AL	
SN52709AL	MC1709AG	
SN52709FA	MC1709F	
SN52709J	MC1709L	
SN52709L	MC1709G	
SN52710FA	MC1710F	
SN52710J	MC1710L	
SN52710L	MC1710G	
SN52711FA	MC1711F	
SN52711J	MC1711L	
SN52711L	MC1711G	
SN52723FA	MC1723F	
SN52723J	MC1723L	
SN52723L	MC1723G	
SN52733J	MC1733L	
SN52733L	MC1733G	
SN52741FA	MC1741F	
SN52741J	MC1741L	
SN52741L	MC1741G	
SN52747FA	MC1747F	
SN52747J	MC1747L	
SN52747L	MC1747G	
SN52748L	MC1748G	
SN52770L		MC1556G
SN52771L		MC1556G
SN52810FA		MC1710F
SN52810J		MC1710L
SN52810L		MC1710G
SN52811FA		MC1711F
SN52811J		MC1711L
SN52811L		MC1711G
SN55107AJ	MC55107L	
SN55107BJ		MC55107L
SN55108AJ	MC55108L	
SN55108BJ		MC75108L
SN55109J		MC75S110L
SN55110J		MC75S110L
SN55244J	MC1544L	
SN55325J	MC55325L	
SN72301AL	LM301AH	
SN72301AP	LM301AN	
SN72304L	LM304H	
SN72305AL		LM305H
SN72305L	LM305H	
SN72306J		MC1710CL
SN72306L		MC1710CG
SN72306N		MC1710CP
SN72307L	LM307H	
SN72308AL	LM308AH	
SN72308L	LM308H	
SN72309L	LM309H	
SN72311L	LM311H	
SN72311P	LM311N	
SN72376L		LM305H
SN72440J		MC3370P
SN72440N		MC3370P
SN72510J		MC1710CL
SN72510L		MC1710CG
SN72510N		MC1710CP
SN72514J		MC1414L
SN72514N		MC1414P
SN72555L	MC1455G	
SN72555P	MC1455P1	
SN72558L	MC1458G	
SN72558P	MC1458P1	
SN72702J	MC1712CL	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SN72702L	MC1712CG	
SN72709J	MC1709CL	
SN72709L	MC1709CG	
SN72709N	MC1709CP2	
SN72709P	MC1709CP1	
SN72710J	MC1710CL	
SN72710L	MC1710CG	
SN72710N	MC1710CP	
SN72711J	MC1711CL	
SN72711L	MC1711CG	
SN72711N	MC1711CP	
SN72720J		MC1710CL
SN72720L		MC1710CG
SN72720N		MC1710CP
SN72723J	MC1723CL	
SN72723L	MC1723CG	
SN72733J	MC1733CL	
SN72733L	MC1733CG	
SN72741FA	MC1741CF	
SN72741J	MC1741CL	
SN74741L	MC1741CG	
SN72741N	MC1741CP2	
SN72741P	MC1741CP1	
SN72747FA	MC1747CF	
SN72747J	MC1747CL	
SN72747L	MC1747CG	
SN72747N	MC1747CP2	
SN72748L	MC1748CG	
SN72748P	MC1748CP1	
SN72770L		MC1456G
SN72771L		MC1456G
SN72810J		MC1710CL
SN72810L		MC1710CG
SN72810N		MC1710CP
SN72811J		MC1711CL
SN72811L		MC1711CG
SN72811N		MC1711CP
SN72905	MC7905CT	
SN72906	MC7906CT	
SN72908	MC7908CT	
SN72912	MC7912CT	
SN72915	MC7915CT	
SN72L022P		LM358N
SN72L044JA		LM324N
SN72L044N		LM324N
SN75107AJ	MC75107L	
SN75107AN	MC75107P	
SN75107BJ		MC75107L
SN75107BN		MC75107P
SN75108AJ	MC75108L	
SN75108AN	MC75108P	
SN75108BJ		MC75108L
SN75108BN		MC75108P
SN75121J	MC8T13L	
SN75121N	MC8T13P	
SN75122J	MC8T14L	
SN75122N	MC8T14P	
SN75123J	MC8T23L	
SN75123N	MC8T23P	
SN75124J	MC8T24L	
SN75124N	MC8T24P	
SN75125J	MC75125L	
SN75125N	MC75125P	
SN75126J		MC3481/5L
SN75126N		MC3481/5P
SN75127J	MC75127L	
SN75127N	MC75127P	

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PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SN75128J	MC75128L	
SN75128N	MC75128P	
SN75129J	MC75129L	
SN75129N	MC75129P	
SN75138N		MC3443P
SN75138J		MC3443P
SN75140P	MC75140P1	
SN75150J		MC1488L
SN75150N		MC1488P
SN75154J		MC1489L
SN75154N		MC1489P
SN75188J	MC1488L	
SN75188N	MC1488P	
SN75189AJ	MC1489AL	
SN75189J	MC1489L	
SN75189AN	MC1489AP	
SN75189N	MC1489P	
SN75207J		MC75107L
SN75207N		MC75107P
SN75208J		MC75108L
SN75208N		MC75108P
SN75261N		MC3245L
SN75322N		MC3245P
SN75362P		MMH0026CP
SN75365J	MC75365L	
SN75365N	MC75365P	
SN75368J	MC75368L	
SN75368N	MC75368P	
SN75369P	MMH0026CP1	
SN75450AJ	MC75450L	
SN75450AN	MC75450P	
SN75450BN		MC75450P
SN75450N	MC75450P	
SN75451AP	MC75451P	
SN75451P	MC75451P	
SN75452P	MC75452P	
SN75453P	MC75453P	
SN75454P	MC75454P	
SN75460AJ	MC75460L	
SN75460AN	MC75460P	
SN75461	MC75461	
SN75461AP	MC75461P	
SN75462	MC75462	
SN75462AP	MC75462P	
SN75463	MC75463	
SN75463AP	MC75463P	
SN75464	MC75464	
SN75464AP	MC75464P	
SN75461N	MC75491P	
SN75466J	MC1411L	
SN75466N	MC1411P	
SN75467J	MC1412L	
SN75467N	MC1412P	
SN75468J	MC1413L	
SN75468N	MC1413P	
SN75475P	MC1472P1	
SN75475JG	MC1472U	
SN75491N	MC75491P	
SN75492N	MC75492P	
SN76000P		MC1306P
SN76104N		MC1310P
SN76105N		MC1310P
SN76111N		MC1310P
SN76113N		MC1310P
SN76115N	MC1310P	
SN76116N		MC1310P
SN76117N		MC1310P

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SN76130N		MC1303P
SN76131N		MC1303P
SN76149N		MC1303P
SN76242N		MC1399P
SN76243N		MC1399P
SN76246N		MC1323P
SN76298N	MC1398P	
SN76514L		MC1496G
SN76514N	MC1496P	
SN76564N	MC1364P	
SN76565N	MC1364P	
SN76591P	MC1391P	
SN76594P	MC1394P	
SN76600P	MC1350P	
SN76642N	MC1357P	
SN76644N		MC1352P
SN76650N	MC1352P	
SN76651N	MC1351P	
SN76653N		MC1352P
SN76660N		MC 357P
SN76665N	MC1364P	
SN76666N	MC1358P	
SN76669N	MC1356P	
SN76675N	MC1375P	
SN76678P		MC1355P
SSS101AL		LM101AH
SSS101AJ	LM101AH	
SSS107J	LM107H	
SSS107P		LM107H
SSS201AJ	LM201AH	
SSS201AL		LM201AH
SSS201AP		LM201AN
SSS207J	LM207H	
SSS207P		LM207H
SSS301AJ	LM301AH	
SSS301AL		LM301AH
SSS301AP	LM301AN	
SSS741BJ		MC1741G
SSS741BL		MC1741F
SSS741BP	MC1741P2	
SSS741CJ		MC1741CG
SSS741CL		MC1741CF
SSS741CP	MC1741CP2	
SSS741GJ	MC1741SG	
SSS741GP		MC1741SG
SSS741J		MC1741G
SSS741L		MC1741F
SSS741P		MC1741P2
SSS747B2	MC1747F	
SSS747BP		MC1747L
SSS747CK		MC1747CG
SSS747CM		MC1747CF
SSS747CP		MC1747CL
SSS747GK		MC1747G
SSS747GM	MC1747F	
SSS747GP		MC1747L
SSS747L		MC1747F
SSS747P		MC1747L
SSS1408A-6Z	MC1408L6	
SSS1408A-7Z	MC1408L7	
SSS1408A-8Z	MC1408L8	
SSS1458J	MC1458G	
SSS1508A-8Z	MC1508L8	
SSS1558J	MC1558G	
TAA630		MC1327P
TBA120S		MC1358P
TBA440		MC1352P

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
TBA520		MC1327P
TBA920		MC1391P
TBA920S		MC1391P
TBA940		MC1344P
TBA950		MC1344P
TBA990		MC1327P
TBA1190Z	TBA1190Z	
TDA1190Z	TDA1190Z	
TDA2002	TDA2002	
TL022CJG		LM358J
TL022CL		LM358H
TL022CP		LM358N
TL022MJG		LM158J
TL022ML		LM158H
TL044CJ		LM324J
TL044CN		LM324N
TL044MJ		LM124J
TL071ACJG		MC34001BU
TL071ACL		MC34001BG
TL071ACP		MC34001BP
TL071BCJG		MC34001AU
TL071BCL		MC34001AG
TL071BCP		MC34001AP
TL071CJG		MC34001U
TL071CL		MC34001G
TL071CP		MC34001P
TL072ACJG		MC34002BU
TL072ACL		MC34002BG
TL072ACP		MC34002BP
TL072BCJG		MC34002AU
TL072BCL		MC34002AG
TL072BCP		MC34002AP
TL072CJG		MC34002U
TL072CL		MC34002G
TL072CP		MC34002P
TL074ACJ		MC34004BL
TL074ACN		MC34004BP
TL074BCJ		MC34004A
TL074BCN		MC34004AP
TL074CJ		MC34004L
TL074CN		MC34004P
TL081ACJG		MC34001BU
TL081ACL		MC34001BG
TL081ACP		MC34001BP
TL081BCJG		MC34001AU
TL081BCL		MC34001AG
TL081BCP		MC34001AP
TL081CJG		MC34001U
TL081CL		MC34001G
TL081CP		MC34001P
TL082ACJG		MC34002BU
TL082ACL		MC34002BG
TL082ACP		MC34002BP
TL082BCJG		MC34002AU
TL082BCL		MC34002AG
TL082BCP		MC34002AP
TL082CJG		MC34002U
TL082CL		MC34002G
TL082CP		MC34002P
TL084ACJ		MC34004BL
TL084ACN		MC34004BP
TL084BCJ		MC34004AL
TL084BCN		MC34004AP
TL084CJ		MC34004L
TL084CN		MC34004P
TL494CJ	TL494CJ	
TL494CN	TL494CN	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
TL495CJ	TL495CJ	
TL495CN	TL495CN	
TL497CJ		MC3420L
TL497CN		MC3420P
TL497MJ		MC3520L
UDN5711M	MC1471P1	
UDN5712M	MC1472P1	
UDN5713M	MC1473P1	
UDN5714M	MC1474P1	
UDN-6144A		MC3490P
UDN-6164A		MC3490P
UDN-6184A		MC3490P
UDN-7183A		MC3491P
UDN-7184A		MC3491P
UDN-7186A		MC3491P
UHD-490		MC3494P
UHD-491		MC3494P
UHP-490		MC3494P
UHP-491		MC3494P
UHP-495		MC3490P
ULN2001A	ULN2001A	
ULN2002A	ULN2002A	
ULN2003A	ULN2003A	
ULN2004A	ULN2004A	
ULN2111A	MC1357P	
ULN2111N	MC1357PQ	
ULN2113A		MC1357P
ULN2113N		MC1357P
ULN2114A		MC1323P
ULN2114K		MC1323P
ULN2114N		MC1323P
ULN2120A		MC1310P
ULN2121A		MC1310P
ULN2122A		MC1310P
ULN2124A		MC1399P
ULN2125A		MC1344P
ULN2127A		MC1399P
ULN2128A		MC1310P
ULN2136A	MC1356P	
ULN2139D		MC1439G
ULN2139G		MC1439G
ULN2139H		MC1439P2
ULN2139M		MC1439P1
ULN2151D		MC1741CG
ULN2151G		MC1741CF
ULN2151H		MC1741CP2
ULN2151M		MC1741CP1
ULN2156D		MC1456G
ULN2156G		MC1456G
ULN2156H		MC1456G
ULN2156M		MC1456G
ULN2157A		MC1458P2
ULN2157H		MC1458P2
ULN2157K		MC1458G
ULN2165A	MC1358P	
ULN2165N	MC1358PQ	
ULN2209A		MC1356P
ULN2210A	MC1310P	
ULN2224A	MC1324P	
ULN2228A		MC1323P
ULN2244A		MC1310P
ULN2262A		MC1399P
ULN2264A	MC1364P	
ULN2267A		MC1323P
ULN2298A	MC1398P	
ULN2741D		MC1741CG
ULN2747A		MC1747CL

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
ULS2139D		MC1539G
ULS2139G		MC1539G
ULS2139H		MC1539L
ULS2139M		MC1439P1
ULS2151D		MC1741G
ULS2151G		MC1741F
ULS2151H		MC1741L
ULS2151M		MC1741CP1
ULS2156D		MC1556G
ULS2156G		MC1556G
ULS2156H		MC1556G
ULS2156M		MC1556G
ULS2157A		MC1558L
ULS2157H		MC1558L
ULS2157K		MC1558G
μA0802DC-1	MC1408L8	
μA0802DC-2	MC1408L7	
μA0802DC-3	MC1408L6	
μA0802DM-1	MC1508L8	
μA0802PC-1	MC1408P8	
μA0802PC-2	MC1408P7	
μA0802PC-3	MC1408P6	
μA101AD		LM101AJ
μA101AF		LM101AJ
μA101AH	LM101AH	
μA101D		LM101AJ
μA101F		LM101AJ
μA101H	LM101AH	
μA104HM	LM104H	
μA105HM	LM105H	
μA107H	LM107H	
μA108AD	LM108AJ	
μA108AF	LM108AF	
μA108AH	LM108AH	
μA108D	LM108J	
μA108F	LM108F	
μA108H	LM108H	
μA109KM	LM109K	
μA201AD		LM201AJ
μA201AF		LM201AJ
μA201AH	LM201AH	
μA201D		LM201AJ
μA201F		LM201AJ
μA201H	LM201AH	
μA207H	LM207H	
μA208AD	LM208AJ	
μA208AF	LM208AF	
μA208AH	LM208AH	
μA208D	LM208J	
μA208F	LM208F	
μA208H	LM208H	
μA209KM	LM209K	
μA301AD		LM301AJ
μA301AH	LM301AH	
μA301AT	LM301AN	
μA304HC	LM304H	
μA305HC		LM305H
μA305HC	LM305H	
μA307H	LM307H	
μA307T	LM307N	
μA308AD	LM308AJ	
μA308AH	LM308AH	
μA308D	LM308J	
μA308H	LM308H	
μA309KC	LM309K	
μA311T	LM311N	
μA376TC		LM305H

PART NO	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA555HC	MC1455G	
μA555HM	MC1555G	
μA555TC	MC1455P1	
μA556DC	MC3456L	
μA556DM	MC3556L	
μA556PC	MC3456P	
μA702DC	MC1712CL	
μA702DM	MC1712L	
μA702FM	MC1712F	
μA702HC	MC1712CG	
μA702HM	MC1712G	
μA702MJ	MC1712L	
μA702ML	MC1712G	
μA709ADM	MC1709AL	
μA709AFM	MC1709AF	
μA709AHM	MC1709AG	
μA709AMJ	MC1709AL	
μA709AMJG	MC1709AU	
μA709AML	MC1709AG	
μA709CJ	MC1709CL	
μA709CJG	MC1709CU	
μA709CL	MC1709CG	
μA709CN	MC1709CP2	
μA709CP	MC1709CP1	
μA709DC	MC1709CL	
μA709DM	MC1709L	
μA709FM	MC1709F	
μA709HC	MC1709CG	
μA709HM	MC1709G	
μA709MJ	MC1709L	
μA709MJG	MC1709U	
μA709ML	MC1709G	
μA709TC	MC1709CP1	
μA709PC	MC1709CP2	
μA710DC	MC1710CL	
μA710DM	MC1710L	
μA710HC	MC1710CG	
μA710HM	MC1710G	
μA710PC	MC1710CP	
μA711DC	MC1711CL	
μA711DM	MC1711L	
μA711HC	MC1711CG	
μA711HM	MC1711G	
μA711PC	MC1711CP	
μA715DC		MC1741SCL
μA715DM		MC1741SL
μA715HC		MC1741SCG
μA715HM		MC1741SG
μA723CJ	MC1723CL	
μA723CL	MC1723CG	
μA723CN	MC1723CP	
μA723DC	μA723DC	
μA723DM	MC1723L	
μA723HC	μA723HC	
μA723HM	MC1723G	
μA723MJ	MC1723L	
μA723ML	MC1723G	
μA723PC	μA723PC	
μA725AHM		LM108AH
μA725EHC		LM308AH
μA725HC		LM308AH
μA725HM		LM108AH
μA727HC		MC1420G
μA727HM		MC1520G
μA730HC		MC1420G
μA730HM		MC1520G
μA732DC		MC1310P

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PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA732PC		MC1310P
μA733CJ	MC1733CL	
μA733CL	MC1733CG	
μA733CN	MC1733CP	
μA733DC	MC1733CL	
μA733DM	MC1733L	
μA733FM	MC1733F	
μA733HC	MC1733CG	
μA733HM	MC1733G	
μA733MJ	MC1733L	
μA733ML	MC1733G	
μA734DC		LM311J
μA734DM		LM311J
μA734HC		LM311H
μA734HM		LM311H
μA740HC		LF355H
μA740HM		LF155H
μA741ADM		MC1741L
μA741AFM		MC1741F
μA741AHM		MC1741G
μA741CJ	MC1741CL	
μA741CJG	MC1741CU	
μA741CL	MC1741CG	
μA741CN	MC1741CP2	
μA741CP	MC1741CP1	
μA741DC	μA741DC	
μA741DM	MC1741L	
μA741EDC		MC1741L
μA741EHC		MC1741G
μA741FC	MC1741CF	
μA741FM	MC1741F	
μA741HC	μA741HC	
μA741HM	MC1741G	
μA741MJ	MC1741L	
μA741MJG	MC1741U	
μA741ML	MC1741G	
μA741RC	MC1741CU	
μA741RM	MC1741U	
μA741PC	MC1741CP2	
μA741TC	μA741TC	
μA742DC		CA3059
μA746DC		MC1323P
μA746HC		MC1323P
μA747ADM		MC1747L
μA747AHM		MC1747G
μA747CJ	MC1741CL	
μA747CL	MC1747CG	
μA747CN	MC1747CP2	
μA747DC	MC1747CL	
μA747DM	MC1747L	
μA747EDC	MC1747CCBM	
μA747EHC	MC1747CICM	
μA747HC	MC1747CG	
μA747HM	MC1747G	
μA747MJ	MC1747L	
μA747ML	MC1747G	
μA747PC	MC1747CP2	
μA748AFM		MC1748F
μA748AHM		MC1748G
μA748CJ	MC1748CL	
μA748CJG	MC1748CU	
μA748CL	MC1748CG	
μA748CN	MC1748CP2	
μA748CP	MC1748CP1	
μA748DC	MC1748CL	
μA748DM	MC1748L	
μA748FM	MC1748F	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA748HC	MC1748CG	
μA748HM	MC1748G	
μA748MJ	MC1748L	
μA748MJG	MC1748U	
μA748ML	MC1748G	
μA748TC	MC1748CP1	
μA749DC		MC1435L
μA749DHC		MC1435G
μA749DM		MC1535L
μA749HC		MC1435G
μA753TC		MC1356P
μA754HC		MC1355P
μA754TC		MC1355P
μA757DC		MC1350P
μA757DM		MC1350P
μA758DC		MC1310P
μA758PC		MC1310P
μA767DC		MC1310P
μA767PC		MC1310P
μA772		MC1741S
μA775DC	LM339J	
μA775DM	LM339J	
μA775PC	LM339N	
μA776DC		MC1776CG
μA776DM		MC1776G
μA776HC	MC1776CG	
μA776HM	MC1776G	
μA776TC	MC1776CP1	
μA777CJ		LM308AJ-8
μA777CJG		LM308AJ-8
μA777CL		LM308AH
μA777CN		LM308AN
μA777CP		LM308AN
μA777DC		LM308AJ-8
μA777HC		LM308AH
μA777MJ		LM108AJ-8
μA777MJG		LM108AJ-8
μA777ML		LM108AH
μA777TC		LM308AN
μA780DC		MC1399P
μA780PC		MC1399P
μA781DC		MC1399P
μA781PC		MC1399P
μA786DC		MC1327P
μA787PC		MC1399P
μA791KC		MC1438R
μA791KM		MC1538R
μA791P5		MC1438R
μA796HC	MC1496G	
μA796HM	MC1596G	
μA796DC	MC1496L	
μA796DM	MC1596L	
μA798HC	MC3458G	
μA798HM	MC3558G	
μA798RC	MC3458U	
μA798RM	MC3558U	
μA798TC	MC3458P1	
μA799HC		MC1741G
μA799HM		MC1741G
μA1312PC	MC1312P	
μA1314PC	MC1314P	
μA1315PC	MC1315P	
μA1391PC	MC1391P	
μA1394PC	MC1394P	
μA1458CHC	MC1458CG	
μA1458CP	MC1458CP1	
μA1458CRC	MC1458CU	

PART NO	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA1458CTC	MC1458CP1	
μA1458E	MC1458G	
μA1458HC	MC1558G	
μA1458P	MC1458P1	
μA1458RC	MC1458U	
μA1458TC	MC1458P1	
μA1558E	MC1558G	
μA1558HM	MC1558G	
μA2136PC	MC1356P	
μA2240DC		MC1455U
μA2240DM		MC1555G
μA2240PC		MC1455P1
μA3026HM		CA3054
μA3045		MC3346P
μA3046DC	MC3346P	
μA3054DC	CA3054P	
μA3064PC	MC1364P	
μA3065PC	MC1358P	
μA3086DM	MC3386P	
μA3301P	MC3301P	
μA3302P	MC3302P	
μA3303P	MC3303P	
μA3401P	MC3401P	
μA3403D	MC3403L	
μA3403P	MC3403P	
μA4136DC		MC4741CL
μA4136DM		MC4741L
μA4136PC		MC4741CP
μA4558HC	MC4558CG	
μA4558HM	MC4558G	
μA4558TC	MC4558CP1	
μA7805CKC	MC7805CT	
μA7805KC	MC7805CK	
μA7805KM	MC7805K	
μA7805UC	MC7805CT	
μA7806CKC	MC7806CT	
μA7806KC	MC7806CK	
μA7806KM	MC7806K	
μA7806UC	MC7806CT	
μA7808CKC	MC7808CT	
μA7808KC	MC7808CK	
μA7808KM	MC7808K	
μA7808UC	MC7808CT	
μA7812CKC	MC7812CT	
μA7812KC	MC7812CK	
μA7812KM	MC7812K	
μA7812UC	MC7812CT	
μA7815CKC	MC7815CT	
μA7815KC	MC7815CK	
μA7815KM	MC7815K	
μA7815UC	MC7815CT	
μA7818CKC	MC7818CT	
μA7818KC	MC7818CK	
μA7818KM	MC7818K	
μA7818UC	MC7815CT	
μA7824CKC	MC7824CT	
μA7824KC	MC7824CK	
μA7824KM	MC7824K	
μA7824UC	MC7824CT	
μA78GHM		LM117K
μA78GKC		LM117K
μA78GKM		LM117K
μA78GU1C		LM317T
μA78H05KC		MC7805CK
μA78L02ACJG		MC78L02ACG
μA78L05ACJG		MC78L05ACG
μA78L05ACLP	MC78L05ACP	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

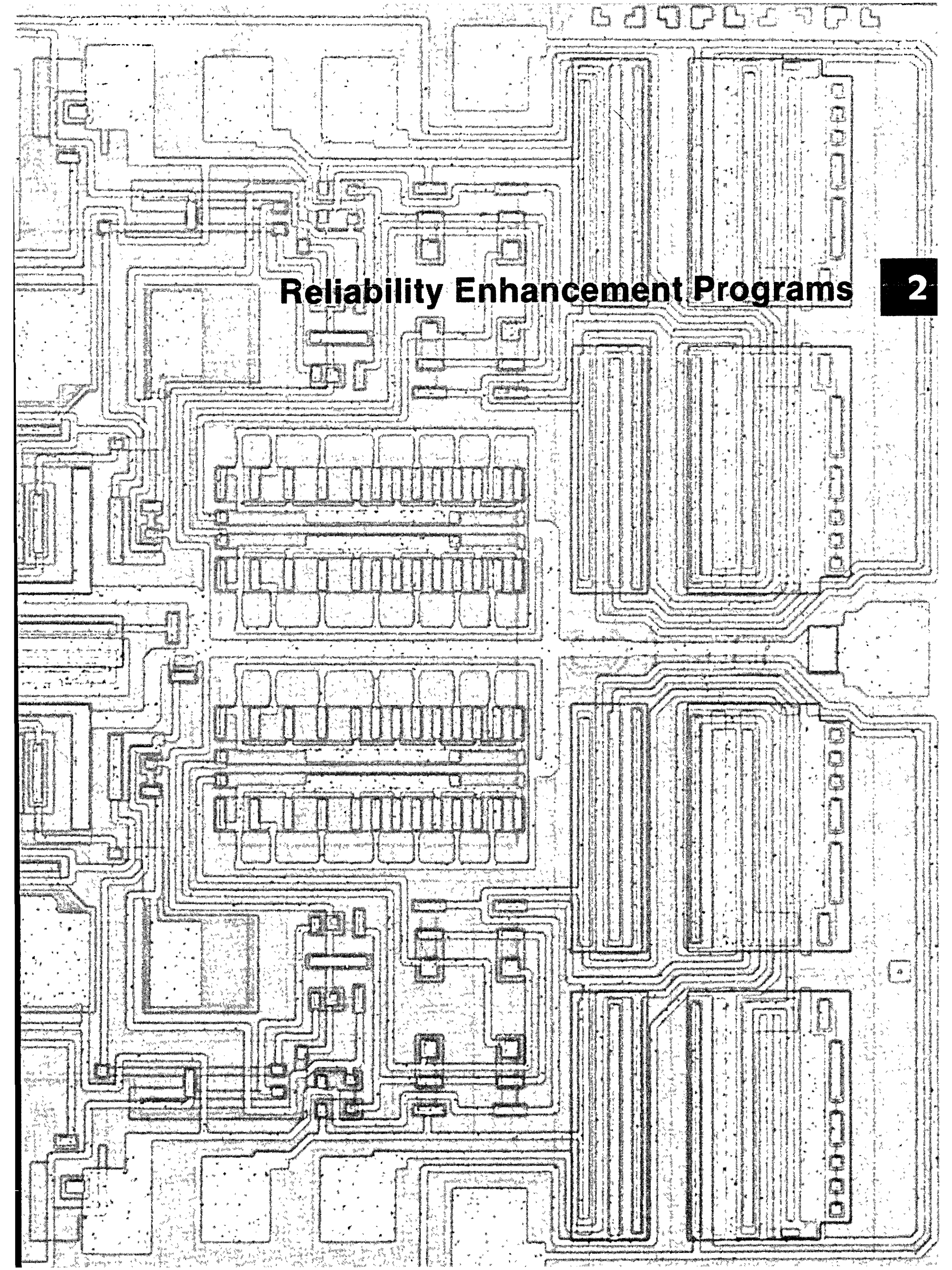
PART NO	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA78L05AHC	MC78L05ACG	
μA78L05AWC	MC78L05ACP	
μA78L05CJG		MC78L05CG
μA78L05CLP	MC78L05CP	
μA78L05HC	MC78L05CG	
μA78L05WC	MC78L05CP	
μA78L06ACJG		MC78L06ACG
μA78L06ACLP	MC78L06ACP	
μA78L06CJG		MC78L06CG
μA78L06CLP	MC78L06CP	
μA78L08ACJG		MC78L08ACG
μA78L08ACLP	MC78L08ACP	
μA78L08CJG		MC78L08CG
μA78L08CLP	MC78L08CP	
μA78L12ACJG		MC78L12ACG
μA78L12ACLP	MC78L12ACP	
μA78L12AHC	MC78L12ACG	
μA78L12AWC	MC78L12ACP	
μA78L12CJG		MC78L12CG
μA78L12CLP	MC78L12CP	
μA78L12HC	MC78L12CG	
μA78L12WC	MC78L12CP	
μA78L15ACJG		MC78L15ACG
μA78L15ACLP	MC78L15ACP	
μA78L15AHC	MC78L15ACG	
μA78L15AWC	MC78L15ACP	
μA78L15CJG		MC78L15CG
μA78L15CLP	MC78L15CP	
μA78L15HC	MC78L15CG	
μA78L15WC	MC78L15CP	
μA78L26AWC	MC7802ACP	
μA78MGHC		LM317H
μA78MGT2C		LM317T
μA78MGU1C		LM317T
μA78M05CKC	MC78M05CT	
μA78M05HC	MC78M05CG	
μA78M05HM		MC78M05CG
μA78M05UC	MC78M05CT	
μA78M06CKC	MC78M06CT	
μA78M06HC	MC78M06CG	
μA78M06HM		MC78M06CG
μA78M06UC	MC78M06CT	
μA78M08CKC	MC78M08CT	
μA78M08HC	MC78M08CG	
μA78M08HM		MC78M08CG
μA78M08UC	MC78M08CT	
μA78M12CKC	MC78M12CT	
μA78M12HC	MC78M12CG	
μA78M12HM		MC78M12CG
μA78M12UC	MC78M12CT	
μA78M15CKC	MC78M15CT	
μA78M15HC	MC78M15CG	
μA78M15HM		MC78M15CG
μA78M15UG	MC78M15CT	
μA78M18HC	MC78M18CG	
μA78M18HM		MC78M18CG
μA78M18UG	MC78M18CT	
μA78M20CKC	MC78M20CT	
μA78M20HC	MC78M20CG	
μA78M20HM		MC78M20CG
μA78M20UG	MC78M20CT	
μA78M24CKC	MC78M24CT	
μA78M24HC	MC78M24CG	
μA78M24HM		MC78M24CG
μA78M24UC	MC78M24CT	
μA7902KC	MC7902K	
μA7902KM		MC7902K

PART NO	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA7902UC	MC7902CT	
μA7905KC	MC7905CK	
μA7905KM		MC7905CK
μA7905UC	MC7905CT	
μA7906KC	MC7906CK	
μA7906KM		MC7906CK
μA7906UC	MC7906CT	
μA7908KC	MC7908CK	
μA7908KM		MC7908CK
μA7908UC	MC7908CT	
μA7912KC	MC7912CK	
μA7912KM		MC7912CK
μA7912UC	MC7912CT	
μA7915KC	MC7915CK	
μA7915KM		MC7915CK
μA7915UC	MC7915CT	
μA7918CKC	MC7918CT	
μA7918KC	MC7918CK	
μA7918KM		MC7918CK
μA7918UC	MC7918CT	
μA7924CKC	MC7924CT	
μA7924KC	MC7924CK	
μA7924KM		MC7924CK
μA7924UC	MC7924CT	
μA79L05AHC	MC79L05ACG	
μA79L05AWC	MC79L05ACP	
μA79L05HC	MC79L05CG	
μA79L05WC	MC79L05CP	
μA79L12AHC	MC79L12ACG	
μA79L12AWC	MC79L12ACP	
μA79L12HC	MC79L12CG	
μA79L12WC	MC79L12CP	
μA79L15AHC	MC79L15ACG	
μA79L15AWC	MC79L15ACP	
μA79L15HC	MC79L15CG	
μA79L15WC	MC79L15CP	
μA79M05AHM		MC7905CK
μA79M05AUC		MC7905CT
μA79M05CKC	MC7905CT	
μA79M05HM		MC7905CK
μA79M05UC		MC7905CT
μA79M06AHM		MC7906CK
μA79M06AUC		MC7906CT
μA79M06CKC	MC7906CT	
μA79M06HM		MC7906CK
μA79M06UC		MC7906CT
μA79M08AHM		MC7908CK
μA79M08AUC		MC7908CT
μA79M08CKC	MC7908CT	
μA79M08HM		MC7908CK
μA79M08UC		MC7908CT
μA79M12AHM		MC7912CK
μA79M12AUC		MC7912CT
μA79M12CKC	MC7912CT	
μA79M12HM		MC7912CK
μA79M12UC		MC7912CT
μA79M15AHM		MC7915CK
μA79M15AUC		MC7915CT
μA79M15CKC	MC7915CT	
μA79M15HM		MC7915CK
μA79M15UC		MC7915CT
μA79M18AHM		MC7918CK
μA79M18AUC		MC7918CT
μA79M18HM		MC7918CK
μA79M18UC		MC7918CT
μA79M24AHM		MC7924CK
μA79M24AUC		MC7924CT

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA79M24HM		MC7924CK
μA79M24UC		MC7924CT
μA8T13DC	MC8T13L	
μA8T13PC		

Reliability Enhancement Programs

2



2

The "Better" Program

Motorola's reliability and quality-enhancement program was developed to provide improved levels of quality and reliability for standard commercial products.

THE "BETTER" program is offered on CMOS, Linear, TTL, TTL/LS, DTL, HTL, and NMOS in dual-in-line ceramic and plastic packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industry's finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

The program is designed to:

- Eliminate incoming electrical inspection
- Eliminate need for independent test labs and associated extra time and costs
- Reduce field failures
- Reduce service calls
- Reduce equipment downtime
- Reduce board and system rework
- Reduce infant mortality
- Save time and money
- Increase end-customer satisfaction

BETTER PROCESSING – STANDARD PRODUCT PLUS:

100% SCREEN	LEVEL I "S"	LEVEL II "D"	LEVEL III "DS"
TEMP CYCLE, 10 CYCLES -25°C to +150°C	X		X
BURN-IN — MIL-STD-883		X	X
POST BURN-IN ELECTRICAL		X	X
100°C FUNCTIONAL	X		X
DC PARAMETRIC AT 25°C*	X	X	X
TIGHTENED QA SAMPLE	X	X	X

*NMOS does Functional and dc 100% at 100°C

"BETTER" AQL GUARANTEES

TEST	CONDITION	AQL LEVEL I	AQL LEVEL II	AQL LEVEL III
HIGH TEMPERATURE FUNCTIONAL	T_A = 100°C	0 15		0.15
DC PARAMETRIC	T_A = 25°C	0.28	0.28	0.28
DC PARAMETRIC	T_A MIN, TA MAX	0.40	0.40	0.40
DC PARAMETRIC (LINEAR AND NMOS)	T_A MIN, TA MAX	0 65	0 65	0.65
AC PARAMETRIC	T_A = 25°C	0.65	0.65	0.65
DYNAMIC TEST (LINEAR AND NMOS)	T_A = 25°C	0 65	0 65	0.65
EXTERNAL VISUAL AND MECHANICAL	MAJOR	0.11	0 11	0.11
	MINOR	2 50	2 50	2 50
HERMETICITY (NOT APPLICABLE TO PLASTIC PACKAGES)	GROSS	0 40	0 40	0 40
	FINE	1.00	1.00	1 00

HOW TO ORDER

MC14001B — **Part Identification**

CP — **Standard Package Suffix**

S — **BETTER PROCESSING**
LEVEL I = SUFFIX S
LEVEL II = SUFFIX D
LEVEL III = SUFFIX DS

PART MARKING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

The Motorola Standard HIGH REL Programs

Motorola, a pioneer in the manufacture of *high-reliability* integrated circuits*, now offers you a two-way program for Hi Rel products

1. A growing line of JAN-QUALIFIED integrated circuits.
2. An extensive program to supply JEDEC PROCESSED devices that approaches the Qualified Reliability goals without the delay and high cost of the actual qualification program.

Motorola stocks many circuits which meet JAN-QUALIFIED specifications, and is actively pursuing an expansion of this qualification listing with product in all IC categories — encompassing Bipolar Digital, Linear and MOS technologies.

Motorola JEDEC PROCESSED products complement JAN-QUALIFIED products by making available hi-rel versions of nearly all Motorola full-temperature range circuits, while adding the advantage of hi-rel standardization.

The Motorola JEDEC Program offers you these benefits:

1. Standardization of environmental and electrical test procedures.
2. Less specification writing required.
3. Less time required in negotiating specifications.
4. Fast delivery.
5. Lower costs.

*Motorola, in early 1971, was the first company to be qualified as a MIL-M-38510 approved facility by the Defense Electronics Supply Center of DOD

2

MIL-M-38510 JAN-Qualified Product

Screening Levels Available:
Class B & Class C

How to order
MIL-M-38510
JAN-Qualified Product

J	M38510	/XXX	XX	Y	Y	Y
INDICATES A QUALIFIED DEVICE	MILITARY DESIGNATOR	DETAIL SPECIFICATION NUMBER	DEVICE TYPE WITHIN DETAIL SPECIFICATION	CLASS B, OR C (SEE DEVICE CLASS TABLE)	CASE OUTLINE (SEE CASE OUTLINE TABLE)	LEAD FINISH (SEE LEAD FINISH TABLE)

Case Outline Table
Source: MIL-M-38510D Amendment I

Letter	Appendix C Designation	Description
A	F-1	14-lead FP (1/4" x 1/4")
B	F-3	14-lead FP (3/16" x 1/4")
C	D-1	14-lead DIP (1/4" x 3/4")
D	F-2	14-lead FP (1/4" x 3/8")
E	D-2	16-lead DIP (1/4" x 7/8")
F	F-5	16-lead FP (1/4" x 3/8")
G	A-1	8-lead can
H	F-4	10-lead FP (1/4" x 1/4")
I	A-2	10-lead can
J	D-3	24-lead DIP (1/4" x 1-1/4")
K	F-6	24-lead FP (3/8" x 5/8")
L	NONE	NONE
M	A-3	12-lead can
N	NONE	NONE
P	D-4	8-lead DIP (1/4" x 3/8")
Q	D-5	40-lead DIP (9/16" x 2-1/16")
R	D-8	20-lead DIP (1/4" x 1-1/16")
S	NONE	NONE
T	NONE	NONE
U	NONE	NONE
V	D-6	18-lead DIP (.300" x 1")
W	D-7	22-lead DIP (.400" x 1.1")
X Y Z	Reserved for use with "special" non-standard case outlines which are specified in the individual detail specifications.	

Features:

1. Manufactured in a government-approved facility.
2. G.S.I. (Government Source Inspection)

Example of MIL-M-38510 JAN-Qualified markings

ORDER: JM38510/00104BCB
MARKING: JM38510/00104BCB

Lead Finish Table
A—Type A or B Per MIL-M-38510 with hot solder dip
B—Type A or B Per MIL-M-38510 with acid tin plate
C—Type A or B Per MIL-M-38510 with gold plate
X—Any of the above, for ordering purposes only.

JEDEC Processed Product

Screening Levels Available: Class B & Class C

How to order JEDEC Processed Product

XXXX/	Y	Y	Y	JC
MOTOROLA DEVICE TYPE (WITHOUT LETTER PREFIX)	CLASS B, OR C (SEE DEVICE CLASS TABLE)	CASE OUTLINE (SEE CASE OUTLINE TABLE)	LEAD FINISH (SEE LEAD FINISH TABLE)	JEDEC DESIGNATOR PER JEDEC PUBLICATION NO 101

Case Outline Table
Source: MIL-M-38510D Amendment I

Letter	Appendix C Designation	Description
A	F-1	14-lead FP (1/4" x 1/4")
B	F-3	14-lead FP (3/16" x 1/4")
C	D-1	14-lead DIP (1/4" x 3/4")
D	F-2	14-lead FP (1/4" x 3/8")
E	D-2	16-lead DIP (1/4" x 7/8")
F	F-5	16-lead FP (1/4" x 3/8")
G	A-1	8-lead can
H	F-4	10-lead FP (1/4" x 1/4")
I	A-2	10-lead can
J	D-3	24-lead DIP (1/4" x 1-1/4")
K	F-6	24-lead FP (3/8" x 5/8")
L	NONE	NONE
M	A-3	12-lead can
N	NONE	NONE
P	D-4	8-lead DIP (1/4" x 3/8")
Q	D-5	40-lead DIP (9/16" x 2-1/16")
R	D-8	20-lead DIP (1/4" x 1-1/16")
S	NONE	NONE
T	NONE	NONE
U	NONE	NONE
V	D-6	18-lead DIP (.300" x 1")
W	D-7	22-lead DIP (.400" x 1.1")
X	Dual-in-line packages not listed above	
Y	Flat packages not listed above	
Z	All other configurations not listed above.	

Features:

1. Lower cost than JAN-Qualified.
2. Devices manufactured using design and processing guidelines contained in MIL-M-38510 and MIL-STD-883
3. Product supplied with Motorola standard data sheet electricals

Example of JEDEC Processed Markings

DEVICE: 5400/BCBJC
ORDER: 5400/BCBJC
MARKING: 5400/BCBJC

Lead Finish Table

A—Type A or B Per MIL-M-38510 with hot solder dip
B—Type A or B Per MIL-M-38510 with acid tin plate
C—Type A or B Per MIL-M-38510 with gold plate
X—Any of the above, for ordering purposes only.

Screening Procedures

For MIL-M-38510 Jan-Qualified and JEDEC Processed Product (To MIL-STD-883 Requirements)

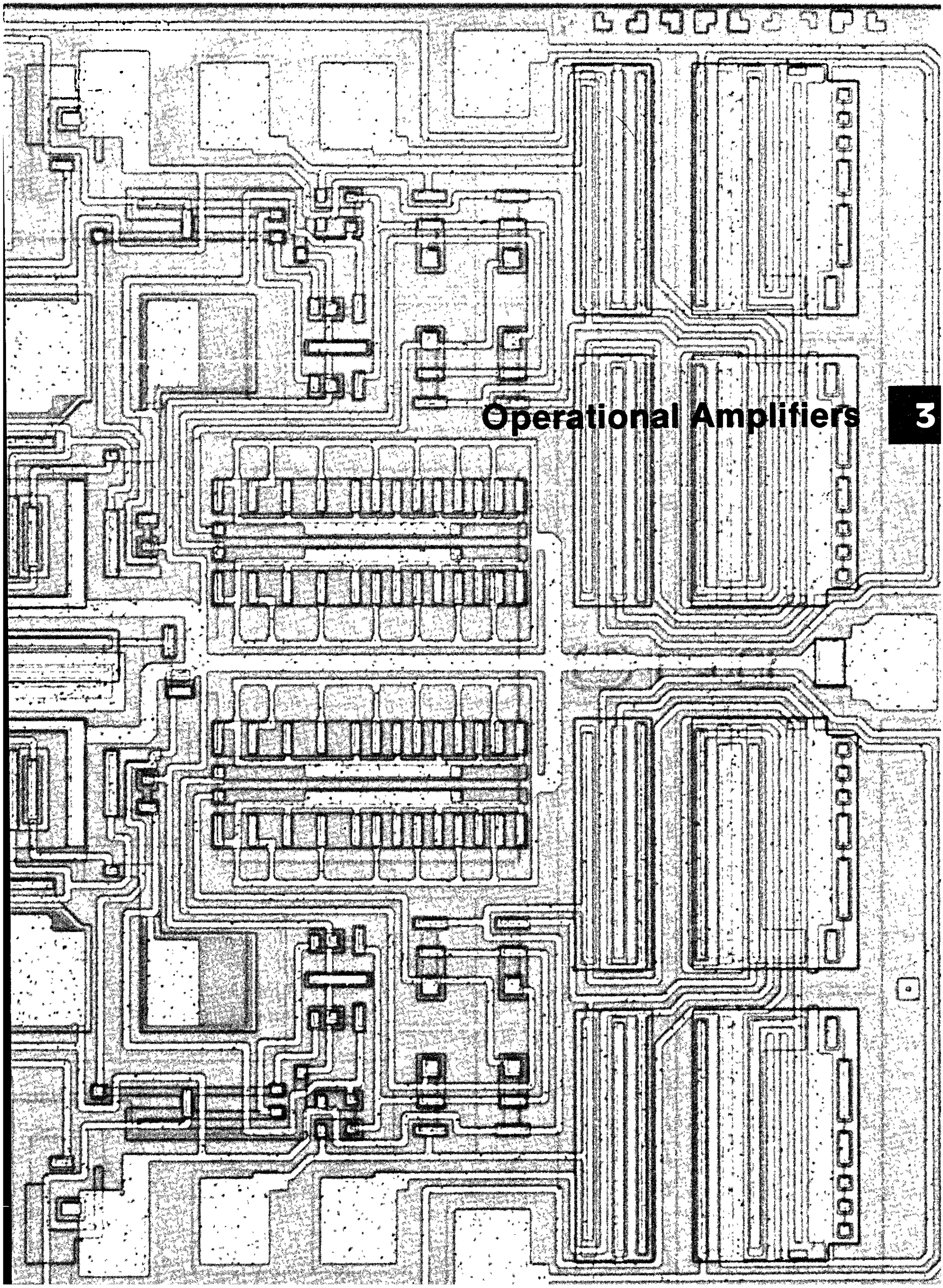
In recognition of the fact that the level of screening has a direct impact on the cost of the product, as well as its quality and reliability, two standard levels of screening are provided to coincide with two device classes, or levels of quality assurance.

Flexibility is provided in the choice of test conditions and stress levels to provide screens tailored to a particular product or application. Selection of a level better than that required for the specific product and application will result in unnecessary expense. A level less than that required may result in a risk that reliability requirements will not be met. For general hi-rel applications, the Class B screening levels should be considered.

Device Class Table

SCREEN	CLASS B METHOD	CLASS B RQMT	CLASS C METHOD	CLASS C RQMT
Internal Visual (Precap)	2010 Condition B and 38510	100%	2010 Condition B and 38510	100%
Stabilization Bake	1008, 24 hrs test Condition C or Equivalent	100 %	1008, 24 hrs test Condition C or Equivalent	100%
Temperature Cycling	1010 Condition C	100%	1010 Condition C	100%
Constant Acceleration	2001 Condition E Y_1 plane	100%	2001 Condition E Y_1 plane	100%
Seal (a) Fine (b) Gross	1014	100%	1014	100%
Interim Electrical Parameters	Per applicable device specification 1			—
Burn-In Test	1015 160 hrs @ 125°C or Equivalent	100%		—
Interim Electrical Parameters	Per applicable device specification 1	100%		—
Final Electrical Tests (a) Static tests (1) 25°C (subgroup 1, table 1, 5005) (2) Max. & min. rated operating temp. (subgroups 2 & 3, table 1, 5005) (b) Dynamic tests &/or switching tests @ 25°C (subgroup 4 and 9, table 1, 5005) (c) Functional test @ 25°C (subgroup 7, table 1 5005)	Per applicable device specification 2	 100% 100% 100% 100%	Per applicable device specification 2	 100% Sample at Group A Sample at Group A 100%
Qualification or Quality Conformance Inspection	5005 Class B 3	Sample per 38510	5005 Class C 3	Sample per 38510
External Visual	2009	100%	2009	100%

1 When specified in the applicable device specification 100% of the devices shall be tested
2 MIL-M-38510 QUALIFIED product is tested per applicable 38510 detail specification. JEDEC PROCESSED product is tested per the Motorola standard data sheet electrical specification
3 For JEDEC PROCESSED product, Groups A and B per 5005 and JEDEC Publication No 101. Groups C and D are available upon request



Operational Amplifiers

3

OPERATIONAL AMPLIFIERS

OPERATIONAL AMPLIFIERS

Motorola offers a broad line of operational amplifiers to meet a wide range of usages. From *low-cost industry-standard types to high precision circuits, the span encompasses a large range of* performance capabilities. These linear integrated circuits are available as single, dual, and quad monolithic devices in a variety of package styles as well as standard chips.

3

Single Operational Amplifiers

NONCOMPENSATED

Device	I_{IB} µA max	V_{IO} mV max	TC_{VIO} µV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/µs typ	Supply Voltage V min	max	Description	Packages
Military Temperature Range (-55°C to +125°C)											
LM101A	0 075	2.0	10	10	50K	1 0	0 5	±3 0	±22	General Purpose	601, 693
LM108	0 002	2 0	3.0	0 2	50K	1 0	0 3	±3 0	±20	Precision	601, 606, 693
LM108A	0 002	0 5	1.0	0 2	80K	1 0	0.3	±3 0	±20	Precision	601, 606, 693
MC1520	2 0	10	15	100	1K	10	5 0	±4 0	±8 0	Differential Output	603, 606
MC1530	10	5 0	15	2 0µA	4 5K	3.0	1 0	±4 0	±9.0	General Purpose	603B, 606, 632
MC1531	15	10	15	25	2.5K	2 0	1 0	±4 0	±9 0	General Purpose (Darlington Input)	603B, 606, 632
MC1533	1.0	5 0	15	150	40K	0 8	2 0	±4 0	±20	General Purpose	603B, 606, 632
MC1539	0 5	3 0	15	60	50K	2 0	4 2	±4 0	±18	High Slew Rate	601, 632
MC1709	0 5	5 0	15	200	25K	1 0	0.3	±3 0	±18	General Purpose	601, 606, 632, 693
MC1709A	0 6	3 0	5 0	100	25K	1 0	0 5	±3 0	±18	High Performance MC1709	601, 606, 632
MC1712	5 0	2 0	15	500	2 5K	7 0	1 5	+6.0 -3.0	+14 -7.0	Wideband DC Amplifier	601, 606, 632
MC1748	0 5	5 0	15	200	50K	1.0	0 5	±3 0	±22	General Purpose	601, 693
Industrial Temperature Range (0°C to +70°C)											
LM301A	0 25	7 5	10	50	25K	1.0	0 5	±3 0	±18	General Purpose	601, 626, 693
LM308	7 0	7.5	15	1 0	25K	1.0	0 3	±3 0	±18	Precision	601, 606, 626, 693
LM308A	7 0	0 5	5.0	1 0	80K	1.0	0 3	±3 0	±18	Precision	601, 606, 626, 693
MC1420	4 0	15	15	200	750	10	5 0	±4 0	±8 0	Differential Output	603, 606
MC1430	15	10	15	4 0µA	3K	3 0	1 0	±4 0	±8 0	General Purpose	603B, 606, 632, 646
MC1431	0 3	15	15	100	1 5K	2 0	1.0	±4 0	±8 0	General Purpose (Darlington Input)	603B, 606, 632, 646
MC1433	2 0	7.5	15	50	30K	0 8	2.0	±4 0	±18	General Purpose	603B, 606, 632, 646
MC1439	1 0	7 5	15	100	15K	2.0	4 2	±6 0	±18	High Slew Rate	601, 626, 632, 646
MC1709C	1 5	7.5	15	500	15K	1.0	0 3	±3 0	±18	General Purpose	601, 606, 626, 632, 646, 693
MC1712C	7 5	5 0	15	2 0µA	2K	7 0	1.5	+6 0 -3.0	+14 -7.0	Wideband DC Amplifier	601, 606, 632
MC1748C	0 5	6 0	15	200	20K	1.0	0 5	±3 0	±18	General Purpose	601, 626, 693

Single Operational Amplifiers

INTERNALLY COMPENSATED

Device	I_{IB} µA max	V_{IO} mV max	TC_{VIO} µV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/µs typ	Supply Voltage V min	Supply Voltage V max	Description	Packages
Military Temperature Range (-55°C to +125°C)											
LF155	100pA	5.0	5.0	20pA	50K	1 0	5 0	±5 0	±22	FET Input	601
LF155A	50pA	2.0	3.0	10pA	50K	1.0	5.0	±5 0	±22	FET Input	601
LF156	100pA	5 0	5.0	20pA	50K	2.0	15	±5.0	±22	FET Input	601
LF156A	50pA	2 0	3.0	10pA	50K	2.0	15	±5 0	±22	FET Input	601
LF157	100pA	5 0	5 0	20pA	50K	3 0	75	±5.0	±22	Wideband FET Input	601
LF157A	50pA	2.0	3 0	10pA	50K	3 0	75	±5 0	±22	Wideband FET Input	601
LM107	0.075	2.0	10	10	50K	1.0	0 5	±3 0	±22	General Purpose	601, 693
MC1536	0 02	5.0	10	3.0	100K	1.0	2.0	±15	±40	High Voltage	601
MC1556	0.015	4.0	10	2 0	100K	1 0	2.5	±3.0	±22	High Performance	601, 632
MC1733	0.20	–	–	3 0µA	90	90	–	±4 0	±8.0	Differential Wideband Video Amp	603, 632
MC1741	0 5	5 0	15	200	50K	1.0	0 5	±3 0	±22	General Purpose	601, 606, 632, 693
MC1741N	0 5	5.0	15	200	50K	1 0	0.5	±3 0	±22	Low Noise	601, 606, 632, 693
MC1741S	0.5	5.0	15	200	50K	1 0	10	±3 0	±22	High Slew Rate	601, 632, 693
MC1776	0 0075	5.0	15	3.0	200K	1.0	0 2	±1 5	±18	µPower Programmable	601, 632
MC35001	100pA	10	10	100pA	25K	4.0	13	±5 0	±22	TRIMFET Input	601, 693
MC35001A	75pA	2.0	10	25pA	50K	4.0	13	±5 0	±22	TRIMFET Input	601, 693
MC35001B	100pA	5 0	10	50pA	50K	4 0	13	±5 0	±22	TRIMFET Input	601, 693
Industrial Temperature Range (0°C to +70°C)											
LF355	200pA	10	5.0	50pA	50K	1 0	5 0	±5.0	±18	FET Input	601
LF355A	50pA	2.0	1 0	10pA	50K	1.0	5 0	±5 0	±18	FET Input	601
LF356	200pA	10	5 0	50pA	50K	2 0	15	±5 0	±18	FET Input	601
LF356A	50pA	2.0	1 0	10pA	50K	2.0	15	±5.0	±18	FET Input	601
LF357	200pA	10	5.0	50pA	50K	3 0	75	±5.0	±18	Wideband FET Input	601
LF357A	50pA	2.0	1 0	10pA	50K	3 0	75	±5 0	±18	Wideband FET Input	601
LM307	0.25	7.5	10	50	25K	1 0	0.5	±3 0	±18	General Purpose	601, 626, 693
MC1436	0 04	10	12	10	70K	1.0	2 0	±15	±34	High Voltage	601
MC1456	0 03	10	12	10	70K	1 0	2 5	±3 0	±18	High Performance	601, 632
MC1733C	30	–	–	5 0µA	80	90	–	±4 0	±8 0	Differential Wideband Video Amp	601, 632, 646
MC1741C	0 5	6.0	15	200	20K	1.0	0.5	±3 0	±18	General Purpose	601, 632, 626, 646, 693
MC1741NC	0 5	6 0	15	200	20K	1.0	0 5	±3 0	±18	Low Noise	601, 632, 626, 646, 693
MC1741SC	0 5	6 0	15	200	20K	1.0	10	±3.0	±18	High Slew Rate	601, 632, 626, 646, 693
MC1776C	0 003	6.0	15	3.0	100K	1 0	0.2	±1 5	±18	µPower, Programmable	601
MC3476	0.05	6.0	15	25	50K	1.0	0.2	±1.5	±18	Low Cost µPower, Programmable	601, 626
MC34001	200pA	10	10	100pA	25K	4.0	13	±5 0	±18	TRIMFET Input	601, 626, 693
MC34001A	100pA	2.0	10	50pA	50K	4.0	13	±5 0	±18	TRIMFET Input	601, 626, 693
MC34001B	200pA	5.0	10	100pA	50K	4 0	13	±5 0	±18	TRIMFET Input	601, 626, 693

Dual Operational Amplifiers

INTERNALLY COMPENSATED

Device	I_{IB} µA max	V_{IO} mV max	TC_{VIO} µV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/µs typ	Supply Voltage V min	Supply Voltage V max	Description	Packages
Military Temperature Range (-55°C to +125°)											
LM158	0 15	5 0	10	30	50K	1.0	0 6	±1 5 +3 0	±18 +36	Split Supplies Single Supply (Low Power Consumption)	601, 632, 693
MC1558	0 5	5 0	10	200	50K	1.1	0 8	±3 0	±22	Dual MC1741	601, 632, 693
MC1558N	0 5	5 0	10	200	50K	1 1	0 8	±3 0	±22	Low Noise	601, 632, 693
MC1558S	0 5	5 0	10	200	50K	1 0	10	±3 0	±22	High Slew Rate	601, 632, 693
MC1747	0 5	5 0	10	200	50K	1.0	0 5	±3 0	±22	Dual MC1741	601, 632
MC3558	0 5	5 0	10	50	50K	1.0	0 6	±1 5 +3 0	±18 +36	Split Supplies Single Supply	601, 632, 693
MC4558	0 5	5 0	10	200	50K	4 0	1.5	±3.0	±22	High Frequency	601, 632, 693
MC35002	100pA	10	10	100pA	25K	4 0	13	±5 0	±22	TRIMFET Input	601, 693
MC35002A	75pA	2 0	10	25pA	50K	4 0	13	±5 0	±22	TRIMFET Input	601, 693
MC35002B	100pA	5.0	10	50pA	50K	4.0	13	±5 0	±22	TRIMFET Input	601, 693
MC35022	150pA	2 0	5 0	70pA	25K	4 0	13	±5 0	±22	Precision TRIMFET Input	601, 693
MC35022A	60pA	0 5	5.0	25pA	50K	4 0	13	±5 0	±22	Precision TRIMFET Input	601, 693
MC35022B	75pA	1 0	5.0	50pA	50K	4 0	13	±5 0	±22	Precision TRIMFET Input	601, 693
Industrial Temperature Range (0°C to +70°C)											
LM358	0.25	6 0	7 0	50	25K	1 0	0 6	±1 5 +3 0	±18 +36	Split Supplies Single Supply (Low Power Consumption)	601, 626, 693
MC1458	0 5	6 0	10	200	20K	1 1	0 8	±3 0	±18	Dual MC1741	601, 626, 632, 646, 693
MC1458N	0 5	6 0	10	200	20K	1 1	0 8	±3 0	±18	Low Noise	601, 626, 632, 646, 693
MC1458S	0 5	6 0	10	200	20K	1 0	10	±3 0	±18	High Slew Rate	601, 626, 632 646, 693
MC1747C	0 5	6 0	10	200	25K	1 0	0 5	±3 0	±18	Dual MC1741	603, 632, 646
MC3458	0 5	10	7 0	50	20K	1 0	0 6	±1 5 +3 0	±18 +36	Split Supplies Single Supply (Low Crossover Distortion)	601, 626, 693
MC4558C	0 5	6 0	10	200	20K	3.0	1.5	±3 0	±18	High Frequency	601, 626, 693
MC34002	100pA	10	10	100pA	25K	4 0	13	±5 0	±18	TRIMFET Input	601, 626, 693
MC34002A	75pA	2 0	10	50pA	50K	4 0	13	±5.0	±18	TRIMFET Input	601, 626, 693
MC34002B	100pA	5 0	10	70pA	25K	4 0	13	±5 0	±18	TRIMFET Input	601, 626, 693
MC34022	150pA	2 0	5 0	70pA	25K	4 0	13	±5 0	±18	Precision TRIMFET Input	601, 626, 693
MC34022A	75pA	0.5	5 0	30pA	50K	4.0	13	±5.0	±18	Precision TRIMFET Input	601, 626, 693
MC34022B	150pA	1.0	5 0	70pA	50K	4 0	13	±5 0	±18	Precision TRIMFET Input	601, 626, 693
Automotive Temperature Range (-40°C to +85°C)											
MC3358	5 0	8.0	10	75	20K	1 0	0 6	±1.5 +3 0	±18 +36	Split Supplies Single Supply	626

NONCOMPENSATED

Device	I_{IB} µA max	V_{IO} mV max	TC_{VIO} µV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/µs typ	Supply Voltage V min	Supply Voltage V max	Description	Packages
Military Temperature Range (-55°C to +125°C)											
MC1535	3 0	3 0	10	300	4K	1 0	0 01	±2 0	±10	General Purpose	603B, 606, 632
MC1537	0 5	5 0	10	200	25K	1 0	0 25	±3 0	±18	Dual MC1709	632
Industrial Temperature Range (0°C to +70°C)											
MC1435	5 0	5 0	10	500	3 5K	1 0	0 01	±2.0	±9 0	General Purpose	603B, 607, 632
MC1437	1.5	7.5	10	500	15K	1 0	0 25	±3.0	±18	Dual MC1709	632, 646

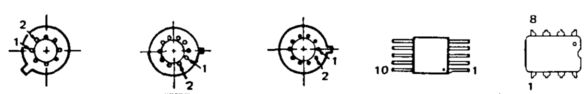
3

Quad Operational Amplifiers

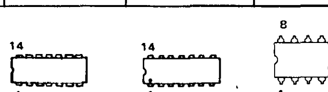
INTERNALLY COMPENSATED

Device	I_{IB} µA max	V_{IO} mV max	TCV_{IO} µV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/µs typ	Supply Voltage V min	max	Description	Packages
Military Temperature Range (-55°C to +125°C)											
LM124	0.15	5.0	7.0	30	50K	1.0	0.6	±1.5	±16	Low Power	632, 646
								+3.0	+32	Consumption	
MC3503	0.5	5 0	7.0	50	50K	1.0	0.6	±1 5	±18	General Purpose	632, 646
								+3 0	+36	Low Power	
MC4741	0.5	5.0	15	200	50K	1.0	0.5	±3 0	±22	Quad MC1741	632, 646
MC35004	100pA	10	10	100pA	25K	4.0	13	±5 0	±22	Trimmed FET Input	632
MC35004A	75pA	2.0	10	25pA	50K	4 0	13	±5 0	±22	Trimmed FET Input	632
MC35004B	100pA	5 0	10	50pA	50K	4 0	13	±5 0	±22	Trimmed FET Input	632
Industrial Temperature Range (0°C to 70°C)											
LM324	0.25	6.0	7.0	50	25K	1 0	0 6	±1 5	±16	Low Power	632, 646
								+3 0	+32	Consumption	
MC3401	0.3	–	–	–	1K	5 0	0.6	±1.5	±18	Norton Input	632, 646
								+3 0	+36		
MC3403	0 5	10	7.0	50	20K	1.0	0 6	±1 5	±18	No Crossover	632, 646
								+3 0	+36	Distortion	
MC4741C	0 5	6.0	15	200	20K	1.0	0 5	±3 0	±18	Quad MC1741	632, 646
MC34004	200pA	10	10	100pA	25K	4 0	13	±5 0	±18	Trimmed FET Input	632, 646
MC34004A	100pA	2.0	10	50pA	50K	4 0	13	±5 0	±18	Trimmed FET Input	632, 646
MC3400B	200pA	5 0	10	100pA	50K	4 0	13	±5 0	±18	Trimmed FET Input	632, 646
Automotive Temperature Range (-40°C to +85°C)											
LM2902	0 5	10	–	50	–	1 0	0 6	±1 5	±13	Differential	646
								+3 0	+26	Low Power	
MC3301	0.3	–	–	–	1K	4.0	0 6	±2 0	±15	Norton Input	646
								+4 0	+28		
MC3303	0 5	8 0	10	75	20K	1 0	0 6	±1 5	±18	Differential	646
								+3 0	+36	General Purpose	

Package Styles



LEAD CONFIGURATION					
CASE	601	603	603B	606	626
MATERIAL	Metal	Metal	Metal	Ceramic	Plastic
SUFFIX after type number	G, H	G, H	G, H	F	P, P1, N



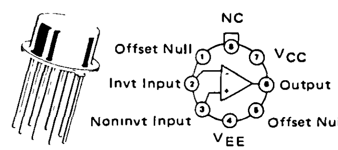
CASE	632	646	693
MATERIAL	Ceramic	Plastic	Ceramic
SUFFIX after type number	J, L	P, P2	J, U

LF155•LF156•LF157*
LF155A•156A•157A*
LF255•LF256•LF257*
LF355•LF356•LF357*
LF355A•356A•357A*
LF355B•356B•357B*

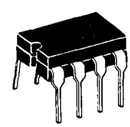
Specifications and Applications Information

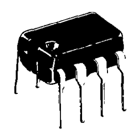
MONOLITHIC JFET OPERATIONAL AMPLIFIERS

H SUFFIX
METAL PACKAGE
CASE 601

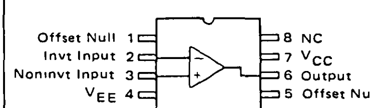


N SUFFIX
PLASTIC PACKAGE
CASE 626





J SUFFIX
CERAMIC PACKAGE
CASE 693



MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

These internally compensated operational amplifiers incorporate highly matched JFET devices on the same chip with standard bipolar transistors. The JFET devices enhance the input characteristics of these operational amplifiers by more than an order of magnitude over conventional amplifiers.

This series of op amps combines the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also, nulling the offset voltage does not degrade the drift or common mode rejection.

- Low Input Bias Current – 30 pA
- Low Input Offset Current – 3.0 pA
- Low Input Offset Voltage – 1.0 mV
- Temperature Compensation of Input Offset Voltage – 3.0 $\mu V/^{o}C$
- Low Input Noise Current – 0.01 $pA/\sqrt{Hz}$
- High Input Impedance – $10^{12}\Omega$
- High Common-Mode Rejection Ratio – 100 dB
- High DC Voltage Gain – 106 dB

SERIES FEATURES

- LF155 Series – Low Power Supply Current
- LF156 Series – Wide Bandwidth
- LF157 Series – **Wider** Bandwidth Decompensated (A_{Vmin} = 5)

	LF155A	LF156A	LF157A
Fast Settling Time to 0.01%	4.0 μs	1.5 μs	1.5 μs
Fast Slew Rate	5.0 V/μs	12 V/μs	50 V/μs
Wide Gain Bandwidth	2.5 MHz	5.0 MHz	20 MHz
Low Input Noise Voltage	20 $nV/\sqrt{Hz}$	12 $nV/\sqrt{Hz}$	12 $nV/\sqrt{Hz}$

APPLICATIONS

The LF series is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Specific applications include:

- Sample and Hold Circuits
- High Impedance Buffers
- Fast D/A and A/D Converters
- Precision High-Speed Integrators
- Wideband, Low Noise, Low Drift Amplifiers

***NOTE:** The LF 157 series is designed for wider bandwidth applications. The series is decompensated (A_{Vmin} = 5).

ORDERING INFORMATION
See back page

3

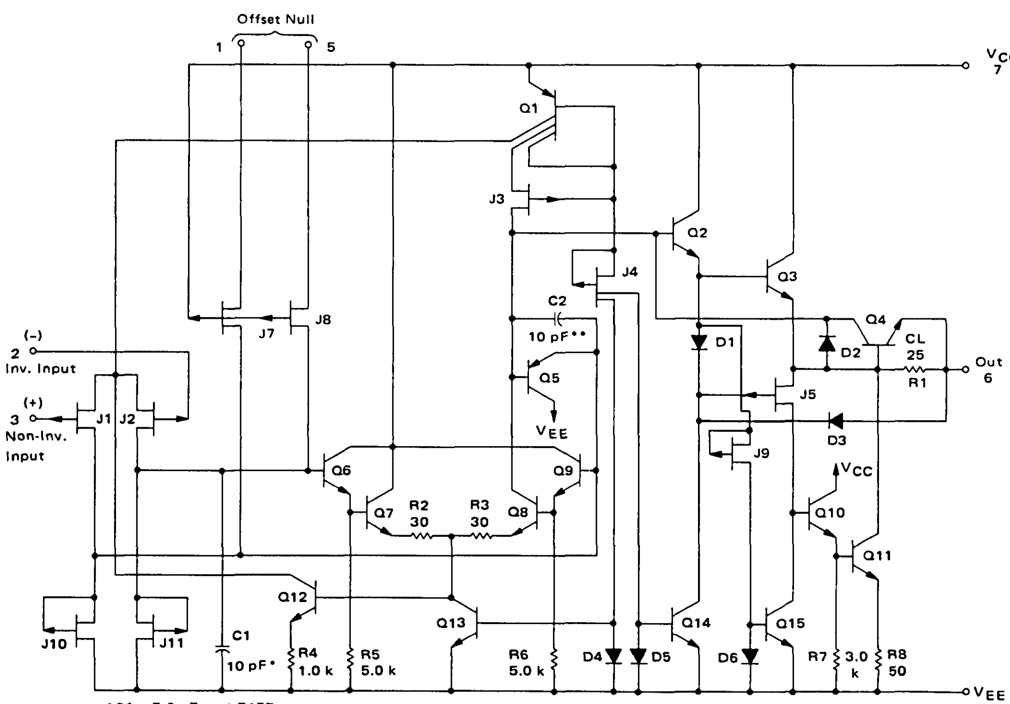
3

MAXIMUM RATINGS

Rating	Symbol	LF155A/ 156A/157A/ 155/156/157	LF255/ 256/257	LF355B/ 356B/357B	LF355A/ 356A/357A/ 355/356/357	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22			+18 −18	V
Differential Input Voltage	V_{ID}	±40			±30	V
Input Voltage Range (Note 1)	V_{IDR}	±20			±16	V
Output Short-Circuit Duration	t_S	Continuous				
Operating Ambient Temperature Range	T_A	−55 to +125	−25 to +85	0 to +70	0 to +70	°C
Operating Junction Temperature Metal and Ceramic Packages Platic Package	T_J	 150 –	 115 100			°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 −65 to +150 –	 −65 to +150 −55 to +125			°C

Note 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

CIRCUIT SCHEMATIC



*C1 = 5.0 pF on LF157.
**C2 = 2.0 pF on LF157.

A–SUFFIX DEVICES

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 to 20 V, V_{EE} = –15 to –20 V for LF155A/6A/7A; V_{CC} = 15 to 18 V, V_{EE} = –15 to –18 V for LF355A/6A/7A; T_A = T_{low} to T_{high} (Note 2) unless otherwise noted)

Characteristic	Symbol	LF155A/6A/7A Min	LF155A/6A/7A Typ	LF155A/6A/7A Max	LF355A/6A/7A Min	LF355A/6A/7A Typ	LF355A/6A/7A Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0)	V_{IO}							mV
(T_A = 25°C)		–	1.0	2.0	–	1.0	2.0	
(Over Temperature)		–	–	2.5	–	–	2.3	
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)	$\Delta V_{IO}/\Delta T$	–	3.0	5.0	–	3.0	5.0	µV/°C
Change in Average TC with V_{IO} Adjust (R_S = 50 Ω) (Note 3)	$\Delta TC/\Delta V_{IO}$	–	0.5	–	–	0.5	–	µV/°C per mV
Input Offset Current (V_{CM} = 0) (Note 4)	I_{IO}							
(T_J = 25°C)		–	3.0	10	–	3.0	10	pA
($T_J \leq T_{high}$) (Note 2)		–	–	10	–	–	1.0	nA
Input Bias Current (V_{CM} = 0) (Note 4)	I_{IB}							
(T_J = 25°C)		–	30	50	–	30	50	pA
($T_J \leq T_{high}$) (Note 2)		–	–	25	–	–	5.0	nA
Input Resistance (T_J = 25°C)	r_i	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k, V_{CC} = 15 V, V_{EE} = –15 V)	A_{VOL}							V/mV
(T_A = 25°C)		50	200	–	50	200	–	
(Over Temperature)		25	–	–	25	–	–	
Output Voltage Swing	V_O							V
(V_{CC} = 15 V, V_{EE} = –15 V, R_L = 10 kΩ)		±12	±13	–	±12	±13	–	
(V_{CC} = 15 V, V_{EE} = –15 V, R_L = 2.0 kΩ)		±10	±12	–	±10	±12	–	
Input Common-Mode Voltage Range (V_{CC} = 15 V, V_{EE} = –15 V)	V_{ICR}	±11	+15.1 –12.0	–	±11	+15.1 –12.0	–	V
Common-Mode Rejection Ratio	CMRR	85	100	–	85	100	–	dB
Supply Voltage Rejection Ratio (Note 5)	PSRR	85	100	–	85	100	–	dB
Supply Current (T_A = 25°C, V_{CC} = 15 V, V_{EE} = –15 V)	I_D							mA
LF155A/355A		–	2.0	4.0	–	2.0	4.0	
LF156A/7A		–	5.0	7.0	–	–	–	
LF356A/7A		–	–	–	–	5.0	10	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = –15 V, T_A = 25°C)

Characteristic	Symbol	LF155A/355A Min	LF155A/355A Typ	LF155A/355A Max	LF156A/356A Min	LF156A/356A Typ	LF156A/356A Max	LF157A/357A Min	LF157A/357A Typ	LF157A/357A Max	Unit
Slew Rate	SR										V/µs
(A_v = 1) LF155A/6A		3.0	5.0	–	10	12	–	–	–	–	
(A_v = 5) LF157A		–	–	–	–	–	–	40	50	–	
Gain-Bandwidth Product	BWp	–	2.5	–	4.0	5.0	–	15	20	–	MHz
Settling Time to 0.01% (Note 6)	t_s	–	4.0	–	–	1.5	–	–	1.5	–	µs
Equivalent Input Noise Voltage (R_S = 100 Ω)	e_n										nV/√Hz
(f = 100 Hz)		–	25	–	–	15	–	–	15	–	
(f = 1000 Hz)		–	20	–	–	12	–	–	12	–	
Equivalent Input Noise Current	i_n										pA/√Hz
(f = 100 Hz)		–	0.01	–	–	0.01	–	–	0.01	–	
(f = 1000 Hz)		–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_i	–	3.0	–	–	3.0	–	–	3.0	–	pF

NOTES

(1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

(2) T_{low} = –55°C for LF155A/156A/157A
0°C for LF355A/356A/357A
T_{high} = +125°C for LF155A/156A/157A
+70°C for LF355A/356A/357A

(3) The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 µV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

(4) The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(5) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

(6) Settling time is defined here, for a unity gain inverter connection using 2.0 k resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10 V step input is applied to the inverter. For the LF157, A_v = –5.0, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

BASIC AND B-SUFFIX DEVICES

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 to 20 V, V_{EE} = −15 to −20 V for LF155 series, LF255 series, and LF355B series; V_{CC} = 15 V, V_{EE} = −15 V for LF355 series; T_A = T_{low} to T_{high} (Note 2) unless otherwise noted)

Characteristic	Symbol	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0)	V_{IO}										mV
(T_A = 25°C)		–	3.0	5.0	–	3.0	5.0	–	3.0	10	
(Over Temperature)		–	–	7.0	–	–	6.5	–	–	13	
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)	$\Delta V_{IO}/\Delta T$	–	5.0	–	–	5.0	–	–	5.0	–	µV/°C
Change in Average TC with V_{IO} Adjust (R_S = 50 Ω) (Note 3)	$\Delta TC/\Delta V_{IO}$	–	0.5	–	–	0.5	–	–	0.5	–	µV/°C per mV
Input Offset Current (V_{CM} = 0) (Note 4)	I_{IO}										
(T_J = 25°C)		–	3.0	20	–	3.0	20	–	3.0	50	pA
(T_J < T_{high}) (Note 2)		–	–	20	–	–	1.0	–	–	2.0	nA
Input Bias Current (V_{CM} = 0) (Note 4)	I_{IB}										
(T_J = 25°C)		–	30	100	–	30	100	–	30	200	pA
(T_J < T_{high}) (Note 2)		–	–	50	–	–	5.0	–	–	8.0	nA
Input Resistance (T_J = 25°C)	r_i	–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k, V_{CC} = 15 V, V_{EE} = −15 V)	A_{VOL}										V/mV
(T_A = 25°C)		50	200	–	50	200	–	25	200	–	
(Over Temperature)		25	–	–	25	–	–	15	–	–	
Output Voltage Swing	V_O										V
(V_{CC} = 15 V, V_{EE} = −15 V, R_L = 10 kΩ)		±12	±13	–	±12	±13	–	±12	±13	–	
(V_{CC} = 15 V, V_{EE} = −15 V, R_L = 2 kΩ)		±10	±12	–	±10	±12	–	±10	±12	–	
Input Common-Mode Voltage Range (V_{CC} = 15 V, V_{EE} = −15 V)	V_{ICR}	±11	+15.1 −12.0	–	±11	+15.1 −12.0	–	±10	+15.1 −12.0	–	V
Common-Mode Rejection Ratio	CMRR	85	100	–	85	100	–	80	100	–	dB
Supply Voltage Rejection Ratio (Note 5)	PSRR	85	100	–	85	100	–	80	100	–	dB
Supply Current (T_A = 25°C, V_{CC} = 15 V, V_{EE} = −15 V)	I_D										mA
LF155/255/355B/355		–	2.0	4.0	–	2.0	4.0	–	2.0	4.0	
LF156/157/256/257/356B/357B		–	5.0	7.0	–	5.0	7.0	–	–	–	
LF356/357		–	–	–	–	–	–	–	5.0	10	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	LF155/255/ 355B/355			LF156/256/ 356B/356			LF157/257/ 357B/357			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate (Note 6)	SR										V/µs
(A_V = 1) LF 155/6		–	5.0	–	7.5	12	–	–	–	–	
(A_V = 5) LF157		–	–	–	–	–	–	30	50	–	
Gain-Bandwidth Product	BWp	–	2.5	–	–	5.0	–	–	20	–	MHz
Settling Time to 0.01% (Note 7)	t_s	–	4.0	–	–	1.5	–	–	1.5	–	µs
Equivalent Input Noise Voltage	e_n										nV/√Hz
(R_S = 100 Ω, f = 100 Hz)		–	25	–	–	15	–	–	15	–	
(R_S = 100 Ω, f = 1000 Hz)		–	20	–	–	12	–	–	12	–	
Equivalent Input Noise Current	i_n										pA/√Hz
(f = 100 Hz)		–	0.01	–	–	0.01	–	–	0.01	–	
(f = 1000 Hz)		–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_i	–	3.0	–	–	3.0	–	–	3.0	–	pF

NOTES

(1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

(2) T_{low} = −55°C for LF155/156/157
= −25°C for LF255/256/257
= 0°C for LF355/355B/356/356B/357/357B
T_{high} = +125°C for LF155/156/157
= +85°C for LF255/256/257
= +70°C for LF355/355B/356/356B/357/357B

(3) The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 µV/°C typically) for each mV of adjustment from its original unadjusted value Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

(4) The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(5) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

(6) The Min. slew rate limits apply for the LF156/256/356B and the LF157/257/357B, but do not apply for the LF356 or LF357.

(7) Settling time is defined here, for a unity gain inverter connection using 2.0 k resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10 V step input is applied to the inverter. For the LF157, A_V = −5 0, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

TYPICAL DC PERFORMANCE CHARACTERISTICS
(Curves are for LF155, LF156, and LF157 series unless otherwise specified)

INPUT BIAS CURRENT versus CASE TEMPERATURE

FIGURE 1 – (LF155 SERIES)

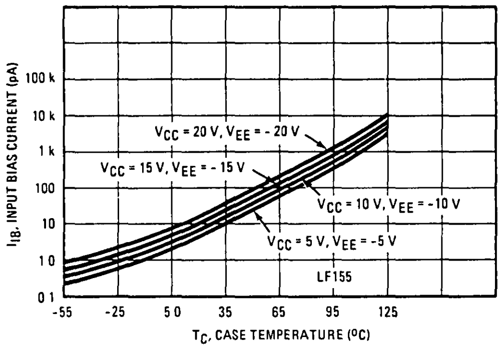


FIGURE 2 – (LF156 AND LF157 SERIES)

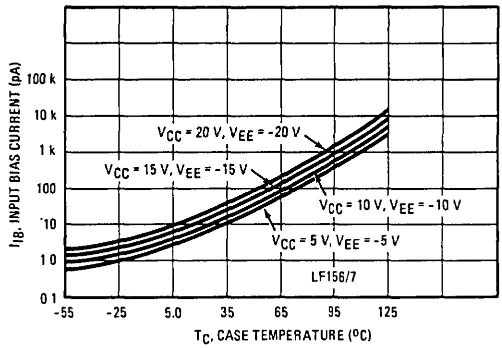


FIGURE 3 – INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

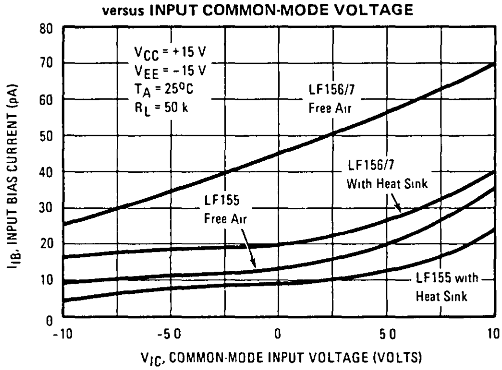
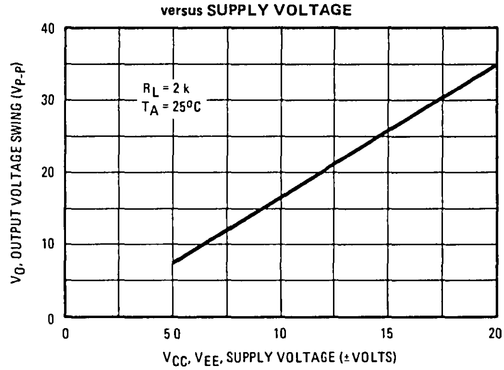


FIGURE 4 – OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE



SUPPLY CURRENT versus SUPPLY VOLTAGE

FIGURE 5 – (LF155 SERIES)

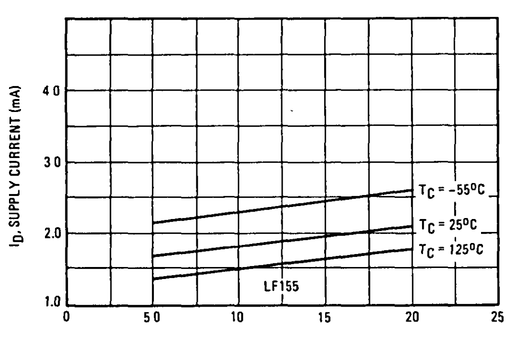
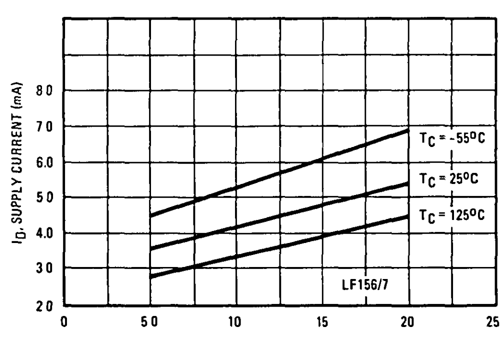


FIGURE 6 – (LF156 AND LF157 SERIES)



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TYPICAL DC PERFORMANCE CHARACTERISTICS (continued)

FIGURE 7 – NEGATIVE CURRENT LIMIT

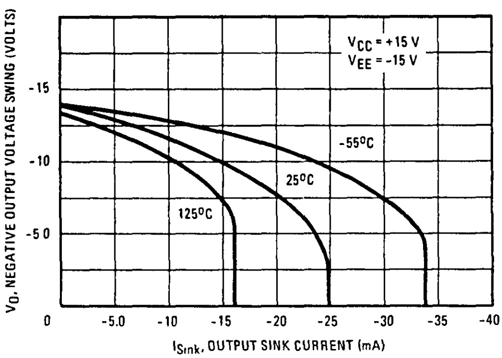


FIGURE 8 – POSITIVE CURRENT LIMIT

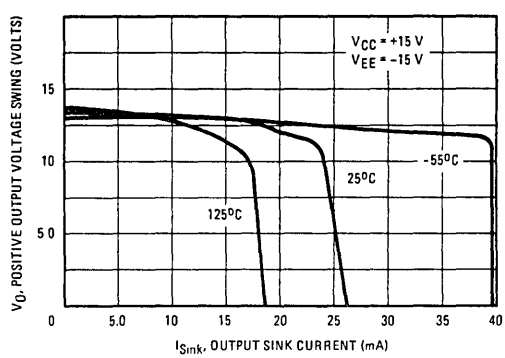


FIGURE 9 – POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT

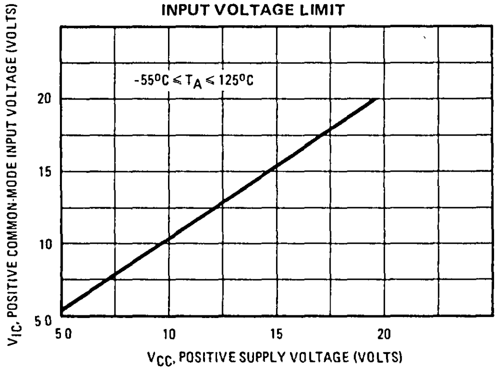


FIGURE 10 – NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT

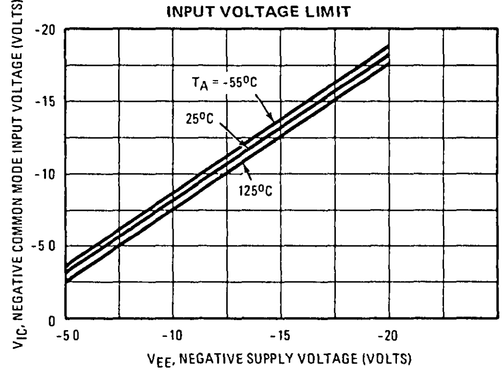


FIGURE 11 – OPEN LOOP VOLTAGE GAIN

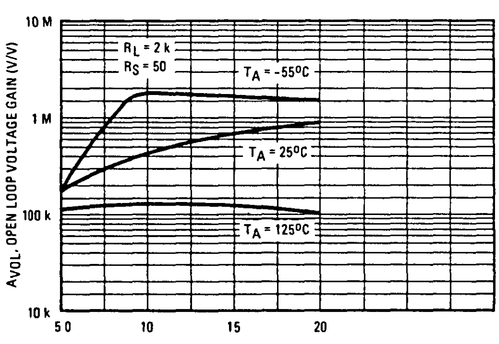
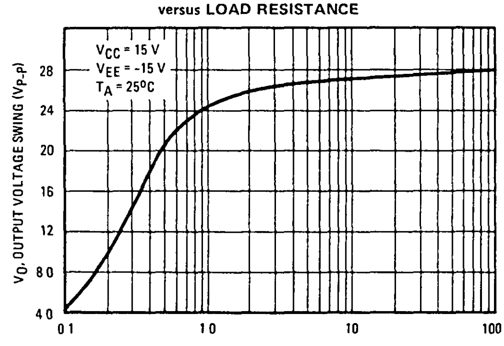


FIGURE 12 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



TYPICAL AC PERFORMANCE CHARACTERISTICS

GAIN BANDWIDTH PRODUCT

FIGURE 13 – (LF155 SERIES)

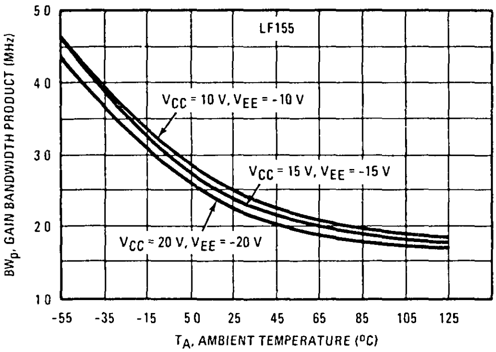
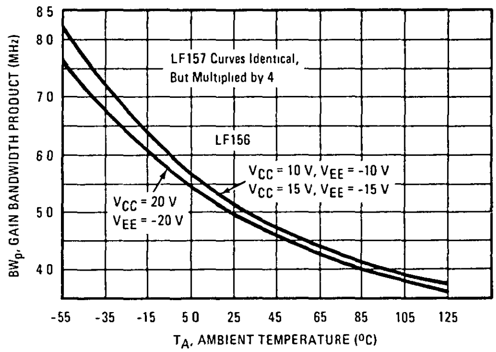


FIGURE 14 – (LF156/157 SERIES)



INVERTER SETTLING TIME

FIGURE 15 – (LF155 SERIES)

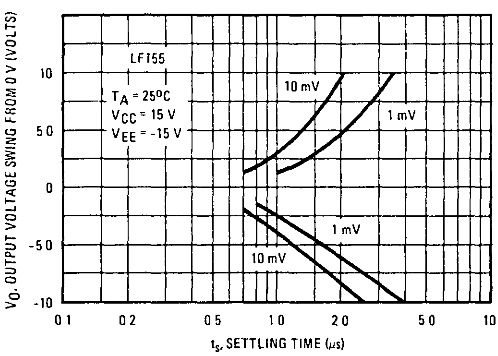


FIGURE 16 – (LF156 AND LF157 SERIES)

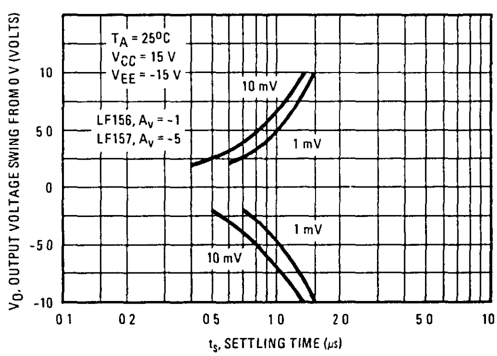


FIGURE 17 – NORMALIZED SLEW RATE

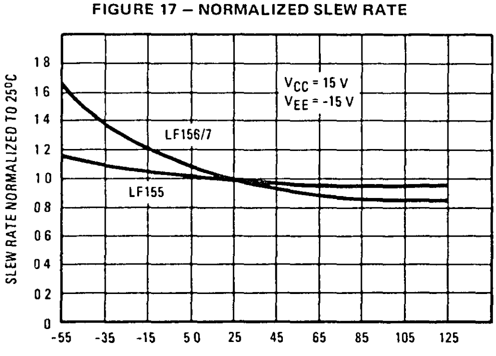
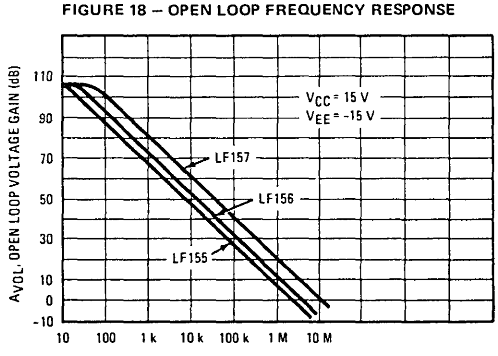


FIGURE 18 – OPEN LOOP FREQUENCY RESPONSE



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TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

BODE PLOT

FIGURE 19 – (LF155 SERIES)

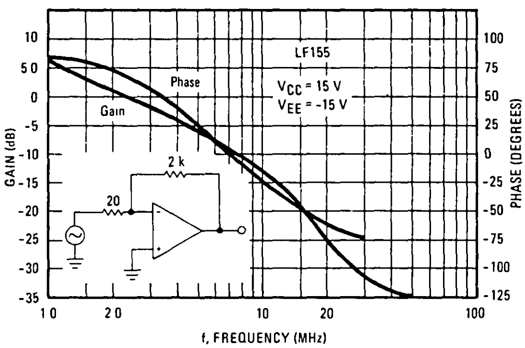


FIGURE 20 – (LF156 SERIES)

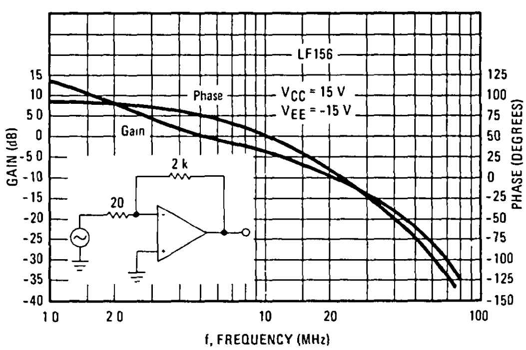
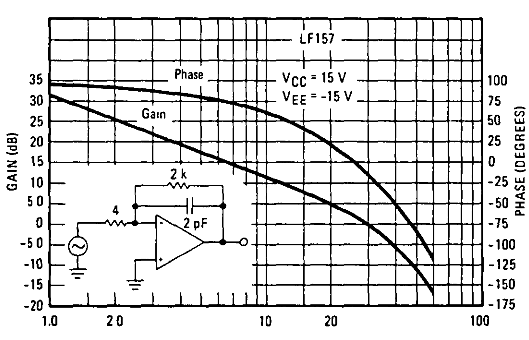


FIGURE 21 – (LF157 SERIES)



OUTPUT IMPEDANCE

FIGURE 22 – (LF155 SERIES)

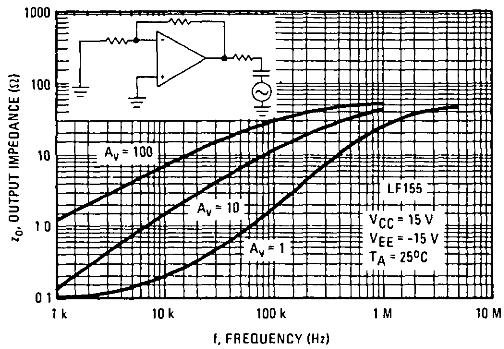


FIGURE 23 – (LF156 SERIES)

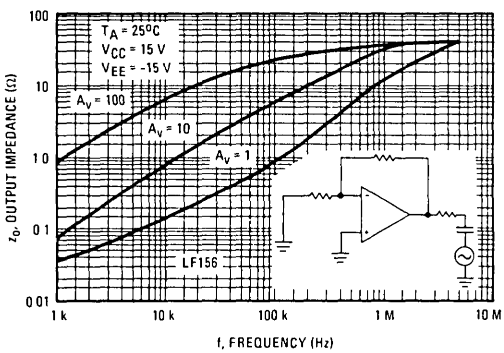
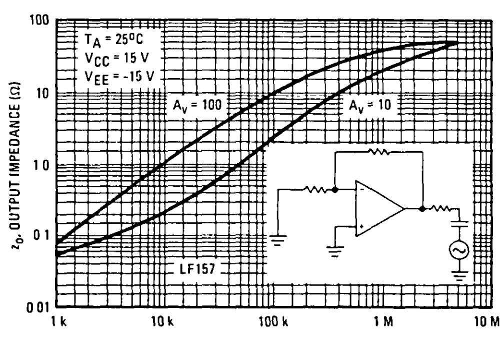


FIGURE 24 – (LF157 SERIES)



TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

FIGURE 25 – COMMON-MODE REJECTION RATIO

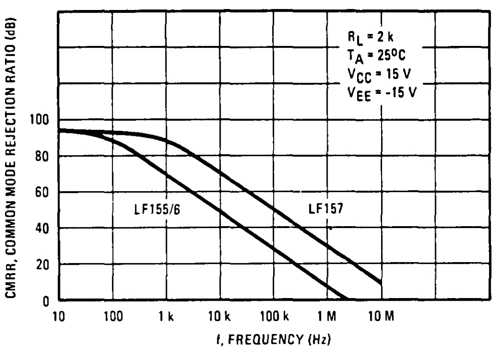
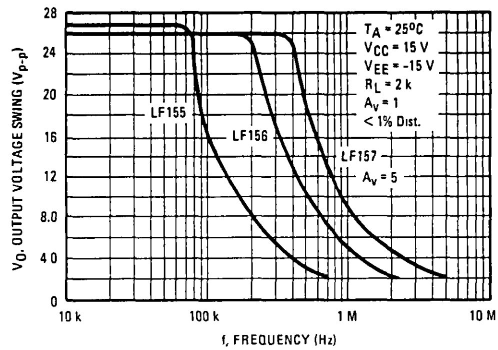


FIGURE 26 – UNDISTORTED OUTPUT VOLTAGE SWING



POWER SUPPLY VOLTAGE REJECTION RATIO

FIGURE 27 – (LF155 SERIES)

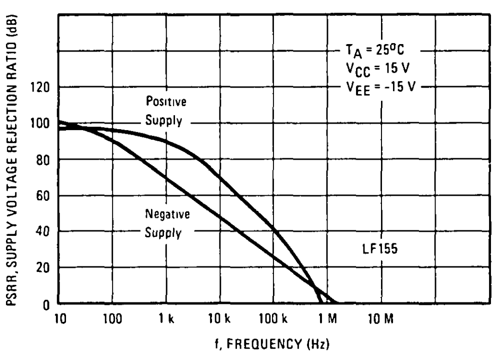
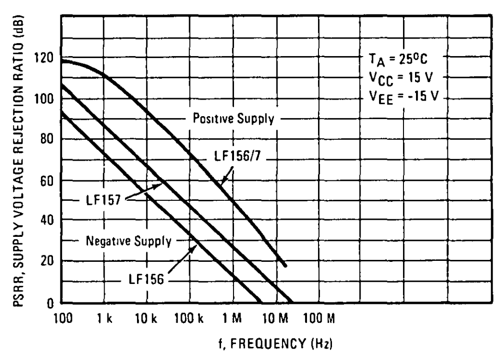


FIGURE 28 – (LF156 AND LF157 SERIES)



EQUIVALENT NOISE VOLTAGE

FIGURE 29 – (LF155/156/157 SERIES)

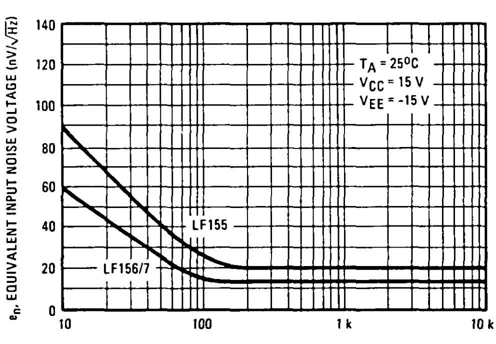
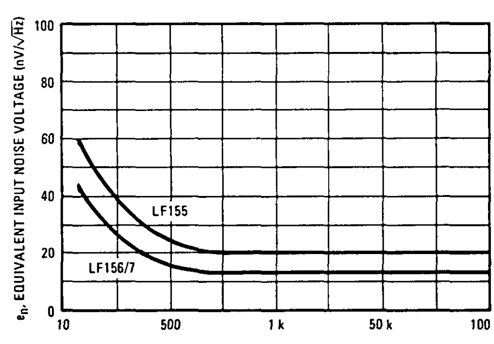
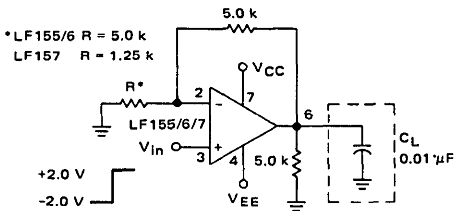


FIGURE 30 – (EXPANDED SCALE)



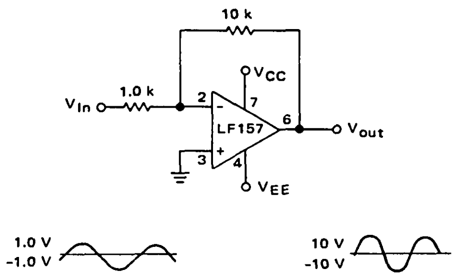
TYPICAL CIRCUIT CONNECTIONS

FIGURE 31 – DRIVING CAPACITIVE LOADS



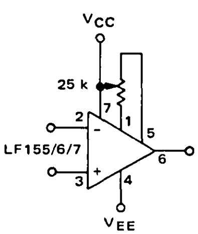
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.
$C_{L(max)} \cong 0.01\ \mu F$.
Overshoot ⩽ 20%
Settling time $(t_s) \cong 5.0\ \mu s$

FIGURE 32 – LARGE POWER BANDWIDTH AMPLIFIER



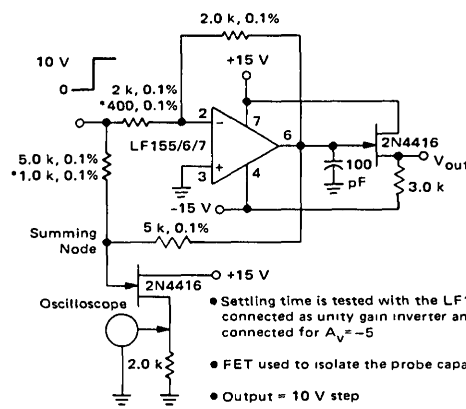
For distortion < 1% and a 20 Vp-p V_{Out} swing, power bandwidth is: 500 kHz.

FIGURE 33 – INPUT OFFSET VOLTAGE ADJUSTMENT



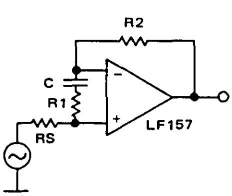
- V_{IO} is adjusted with a 25 k potentiometer
- The potentiometer wiper is connected to V_{CC}
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 µV/°C/mV of adjustment.
- Typical overall drift. 5.0 µV/°C ±(0.5 µV/°C/mV of adjustment.)

FIGURE 34 – SETTLING TIME TEST CIRCUIT



- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10 V step
- •$A_V = -5$ for LF 157

FIGURE 35 – NON-INVERTING UNITY GAIN OPERATION FOR LF157



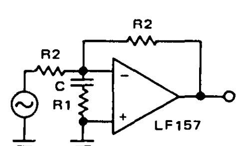
$R1C \geq \frac{1}{(2\pi)(5\ MHz)}$

$R1 = \frac{R2 + R_S}{4}$

$A_{V(DC)} = 1$

$f_{-3dB} \approx 5\ MHz$

FIGURE 36 – INVERTING UNITY GAIN FOR LF157



$R1C \geq \frac{1}{(2\pi)(5\ MHz)}$

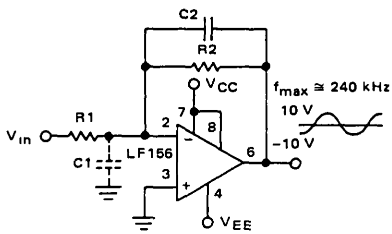
$R1 = \frac{R2}{4}$

$A_{V(DC)} = -1$

$f_{-3dB} \approx 5\ MHz$

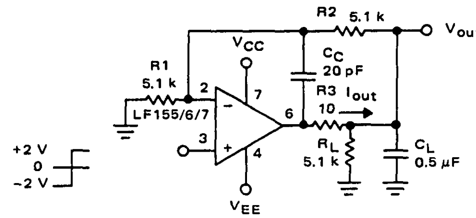
TYPICAL APPLICATIONS

FIGURE 37 — WIDE BW, LOW NOISE, LOW DRIFT AMPLIFIER



- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240$ kHz
- Parasitic input capacitance (C1 ≅ 3 pF for LF155, LF156, and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole To compensate add C2 such that: R2C2 ≅ R1C1.

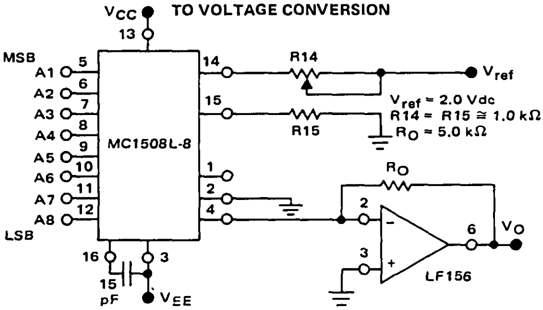
FIGURE 38 — ISOLATING LARGE CAPACITIVE LOADS



- Overshoot 6%
- $t_s = 10\ \mu s$
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

FIGURE 39 — 8-BIT D/A WITH OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

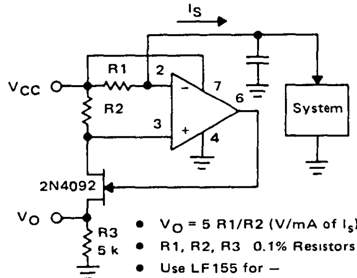
$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2V}{1k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

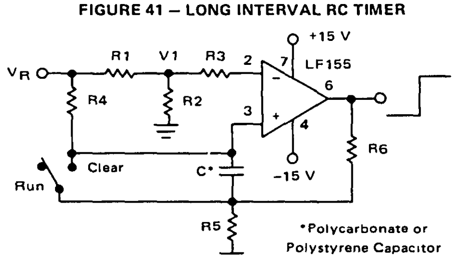
$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

FIGURE 40 — PRECISION CURRENT MONITOR



- $V_O = 5$ R1/R2 (V/mA of I_s)
- R1, R2, R3 0.1% Resistors
- Use LF155 for —
  - ▲ Common-Mode Range to Supply Range
  - ▲ Low I_{IB}
  - ▲ Low V_{IO}
  - ▲ Low Supply Current

FIGURE 41 — LONG INTERVAL RC TIMER



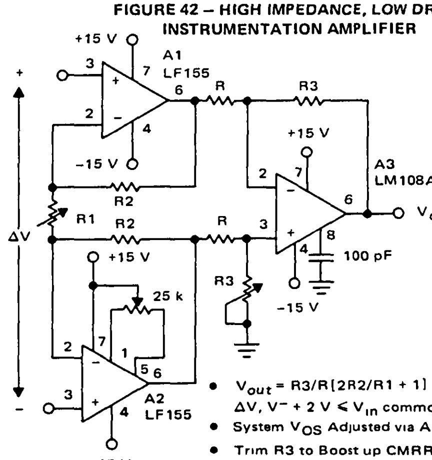
Time (t) = R4C ln (V_R/V_R−V_I), $R_3 = R_4$, $R_5 = 0.1$ R6

If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer

V_R = 10 V	C = 1 µF	R3 = R4 = 144 M
R6 = 20 k	R5 = 2 k	R1 = R2 = 1 k

FIGURE 42 — HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER



- V_{out} = R3/R[2R2/R1 + 1]
  ΔV, V^- + 2 V ≤ V_{in} common-mode ≤ V^+
- System V_{OS} Adjusted via A2 V_{OS} Adjust
- Trim R3 to Boost up CMRR to 120 dB

ORDERING INFORMATION

Device	Temperature Range	Package	Device	Temperature Range	Package
LF155AH, H	-55 to +125°C	Metal Can	LF256N	-25 to +85°C	Plastic DIP
LF155J	-55 to +125°C	Ceramic DIP	LF356AH, BH, H	0 to +70°C	Metal Can
LF255H	-25 to +85°C	Metal Can	LF356BJ, J	0 to +70°C	Ceramic DIP
LF255J	-25 to +85°C	Ceramic DIP	LF356BN, N	0 to +70°C	Plastic DIP
LF255N	-25 to +85°C	Plastic DIP			
LF355AH, BH, H	0 to +70°C	Metal Can	LF157AH, H	-55 to +125°C	Metal Can
LF355BJ, J	0 to +70°C	Ceramic DIP	LF157J	-55 to +125°C	Ceramic DIP
LF355BN, N	0 to +70°C	Plastic DIP	LF257H	-25 to +85°C	Metal Can
			LF257J	-25 to +85°C	Ceramic DIP
LF156AH, H	-55 to +125°C	Metal Can	LF257N	-25 to +85°C	Plastic DIP
LF156J	-55 to +125°C	Ceramic DIP	LF357AH, BH, H	0 to +70°C	Metal Can
LF256H	-25 to +85°C	Metal Can	LF357BJ, J	0 to +70°C	Ceramic DIP
LF256J	-25 to +85°C	Ceramic Dip	LF357BN, N	0 to +70°C	Plastic DIP

ORDERING INFORMATION

Device	Temperature Range	Package
LM101AH	−55°C to +125°C	Metal Can
LM101AJ	−55°C to +125°C	Ceramic DIP
LM201AH	−25°C to +85°C	Metal Can
LM201AN	−25°C to +85°C	Plastic DIP
LM201AJ	−25°C to +85°C	Ceramic DIP
LM301AH	0°C to +70°C	Metal Can
LM301AN	0°C to +70°C	Plastic DIP
LM301AJ	0°C to +70°C	Ceramic DIP

LM101A
LM201A
LM301A

OPERATIONAL AMPLIFIER

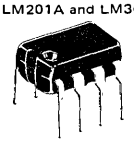
A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation summing amplifier slew rates to 10 V/μs can be obtained.

- Low Input Offset Current – 20 nA maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short-Circuit Protection
- Guaranteed Drift Characteristics

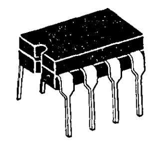
OPERATIONAL AMPLIFIER

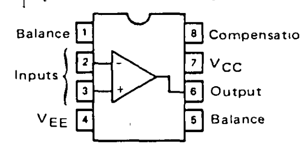
SILICON MONOLITHIC
INTEGRATED CIRCUIT

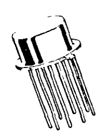
N SUFFIX
PLASTIC PACKAGE
CASE 626
(LM201A and LM301A)



J SUFFIX
CERAMIC PACKAGE
CASE 693







H SUFFIX
METAL PACKAGE
CASE 601

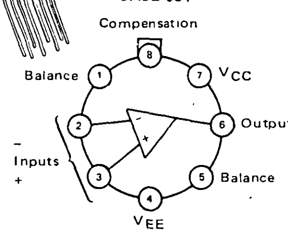


FIGURE 1 – STANDARD COMPENSATING AND OFFSET BALANCING CIRCUIT

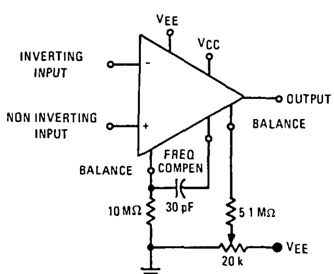
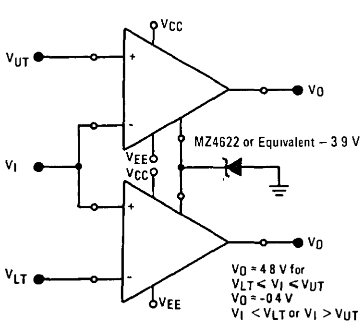
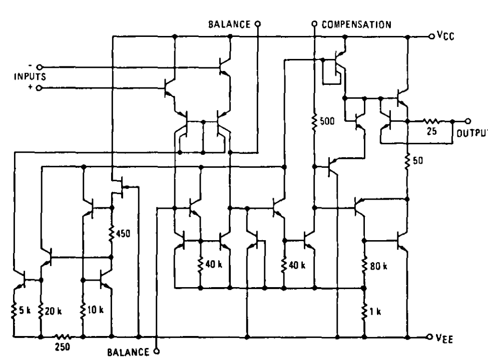


FIGURE 2 – DOUBLE-ENDED LIMIT DETECTOR



PINS NOT SHOWN ARE NOT CONNECTED

FIGURE 3 – REPRESENTATIVE CIRCUIT SCHEMATIC



MAXIMUM RATINGS

Rating	Symbol	VALUE LM101A	LM201A	LM301A	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±22	±22	±18	Vdc
Input Differential Voltage	V_{ID}	← ±30 →			Volts
Input Common-Mode Range (Note 1)	V_{ICR}	← ±15 →			Volts
Output Short-Circuit Duration	t_S	← Continuous →			
Power Dissipation (Package Limitation)	P_D				
Metal Can		← 500 →			mW
Derate above T_A = +75°C		← 6.8 →			mW/°C
Plastic Dual In-Line Package (MLM201A/301A)		–	625	625	mW
Derate above T_A = +25°C		–	5.0	5.0	mW/°C
Ceramic Package		← 750 →			mW
Derate above 25°C		← 6.6 →			mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	← -65 to +150 →			°C

Note 1 For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the LM101A and LM201A, and from ±5.0 V to ±15 V for the LM301A.

Characteristics	Symbol	LM101A LM201A Min	Typ	Max	LM301A Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leqslant$ 50 kΩ)	V_{IO}	–	0.7	2.0	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	1.5	10	–	3.0	50	nA
Input Bias Current	I_{IB}	–	30	75	–	70	250	nA
Input Resistance	r_i	1.5	4.0	–	0.5	2.0	–	Megohms
Supply Current	I_{CC}, I_{EE}							mA
V_{CC}/V_{EE} = ±20 V		–	1.8	3.0	–	–	–	
V_{CC}/V_{EE} = ±15 V		–	–	–	–	1.8	3.0	
Large Signal Voltage Gain V_{CC}/V_{EE} ±15 V, V_O = ± 10 V, R_L > 2.0 kΩ	A_V	50	160	–	25	160	–	V/mV

The following specifications apply over the operating temperature range.

Characteristics	Symbol	LM101A LM201A Min	Typ	Max	LM301A Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leqslant$ 50 kΩ)	V_{IO}	–	–	3.0	–	–	10	mV
Input Offset Current	I_{IO}	–	–	20	–	–	70	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(min) \leqslant T_A \leqslant T_A(max)$	$\Delta V_{IO}/\Delta T$	–	3.0	15	–	6.0	30	μV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
+25°C $\leqslant T_A \leqslant T_A(max)$		–	0.01	0.1	–	0.01	0.3	
$T_A(min) \leqslant T_A \leqslant$ 25°C		–	0.02	0.2	–	0.02	0.6	
Input Bias Current	I_{IB}	–	–	100	–	–	300	nA
Large Signal Voltage Gain V_{CC}/V_{EE} = ± 15 V, V_O = ± 10 V, R_L > 2.0 kΩ	A_V	25	–	–	15	–	–	V/mV
Input Voltage Range	V_I							V
V_{CC}/V_{EE} = ±20 V		±15	–	–	–	–	–	
V_{CC}/V_{EE} = ±15 V		–	–	–	±12	–	–	
Common-Mode Rejection Ratio $R_S \leqslant$ 50 kΩ	CMRR	80	96	–	70	90	–	dB
Supply Voltage Rejection Ratio $R_S \leqslant$ 50 kΩ	PSSR	80	96	–	70	96	–	dB
Output Voltage Swing	V_O							V
V_{CC}/V_{EE} = ±15 V, R_L = 10 kΩ		±12	±14	–	±12	+14	–	
R_L = 2.0 kΩ		±10	±13	–	±10	±13	–	
Supply Currents ($T_A = T_A(max)$, V_{CC}/V_{EE} = ±20 V)	I_{CC}, I_{EE}	–	1.2	2.5	–	–	–	mA

3

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 4 — MINIMUM INPUT VOLTAGE RANGE

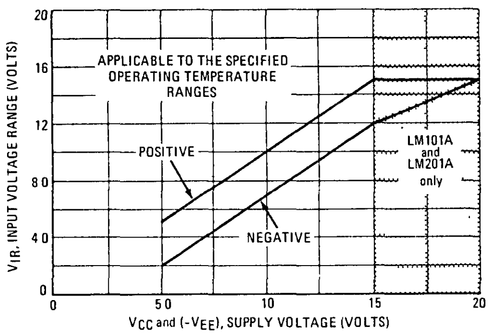


FIGURE 5 — MINIMUM OUTPUT VOLTAGE SWING

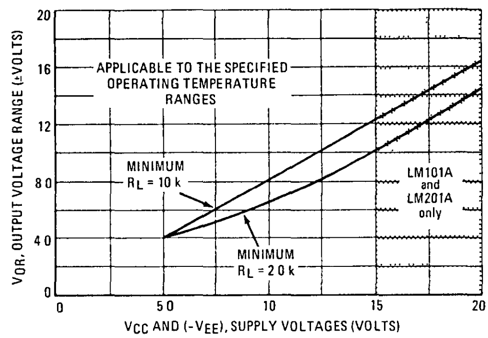


FIGURE 6 — MINIMUM VOLTAGE GAIN

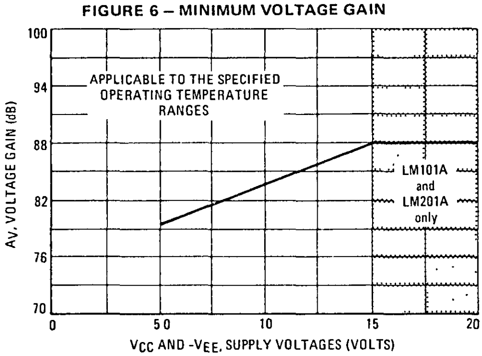


FIGURE 7 — TYPICAL SUPPLY CURRENTS

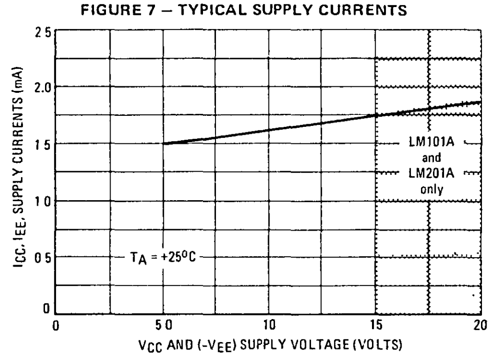


FIGURE 8 — OPEN-LOOP FREQUENCY RESPONSE

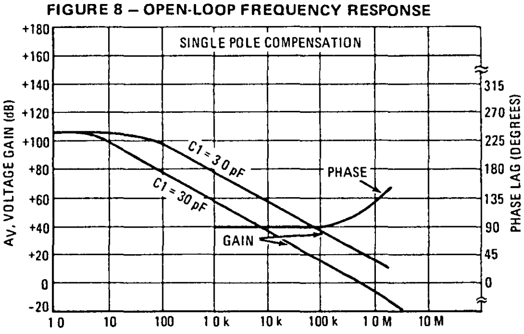
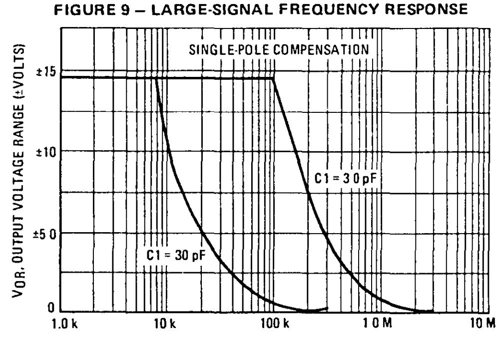


FIGURE 9 — LARGE-SIGNAL FREQUENCY RESPONSE



3

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – VOLTAGE FOLLOWER PULSE RESPONSE

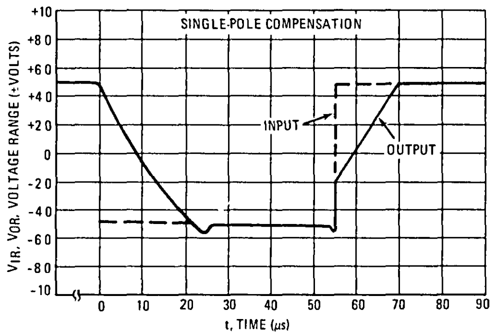


FIGURE 11 – OPEN-LOOP FREQUENCY RESPONSE

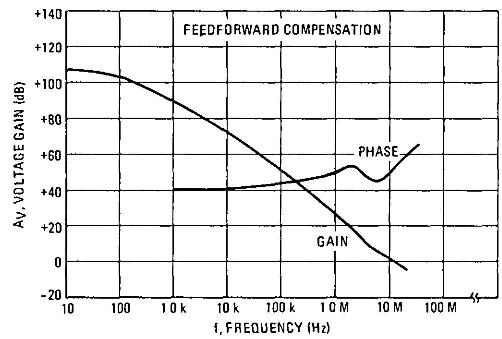


FIGURE 12 – LARGE-SIGNAL FREQUENCY RESPONSE

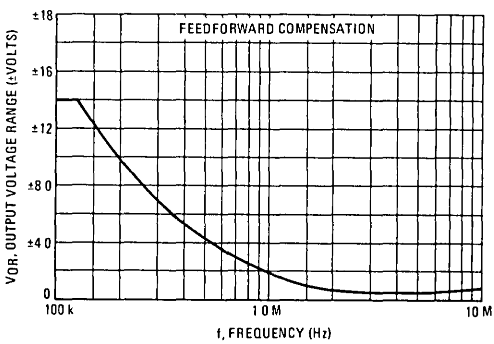
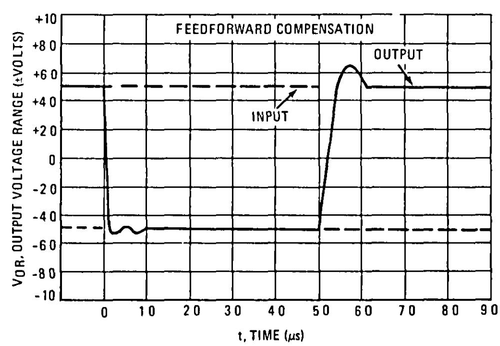
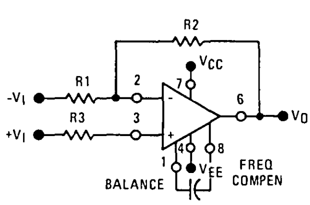


FIGURE 13 – INVERTER PULSE RESPONSE



TYPICAL COMPENSATION CIRCUITS

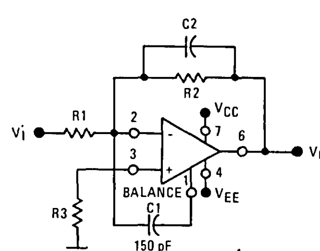
FIGURE 14 – SINGLE-POLE COMPENSATION



$C1 \geq \frac{R1\,C_s}{R1 + R2}$

C_s = 30 pF

FIGURE 15 – FEEDFORWARD COMPENSATION



$C2 = \frac{1}{2\pi f_o R2}$

f_o = 3.0 MHz

ORDERING INFORMATION

Device	Temperature Range	Package
MLM107H	−55°C to +125°C	Metal Can
MLM207H	−25°C to +85°C	Metal Can
MLM307H	0°C to +70°C	Metal Can
MLM307N	0°C to +70°C	Plastic DIP

LM107
LM207
LM307

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

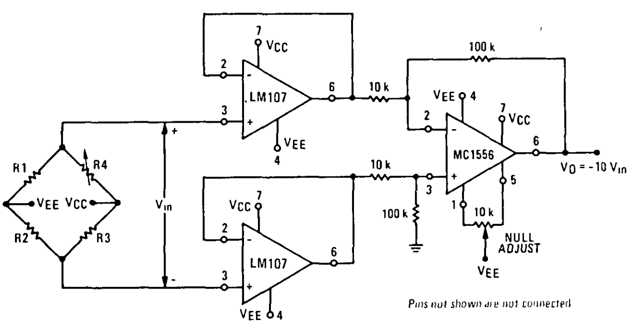
EPITAXIAL PASSIVATED

INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER

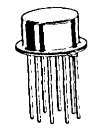
A general purpose operational amplifier series well suited for applications requiring lower input currents than are available with the popular MC1741. These improved input characteristics permit greater accuracy in sample and hold circuits and long interval integrators.

- Internally Compensated
- Low Offset Voltage: 2.0 mV max (LM107)
- Low Input Offset Current: 10 nA max (LM107)
- Low Input Bias Current: 75 nA max (LM107)

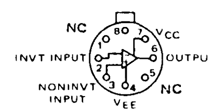
TYPICAL APPLICATION
HIGH IMPEDANCE BRIDGE AMPLIFIER



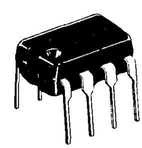
3



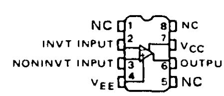
N SUFFIX
METAL PACKAGE
CASE 601



(Top View)

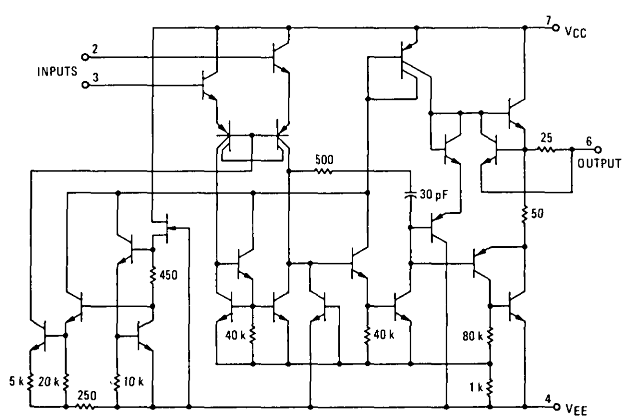


N SUFFIX
PLASTIC PACKAGE
CASE 626
(LM307 only)

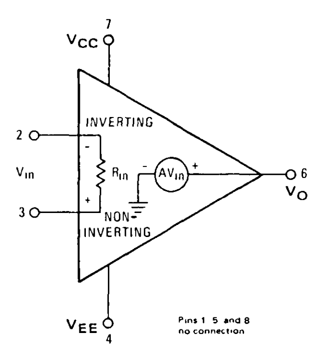


(Top View)

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	LM107	LM207	LM307	Unit
Power Supply Voltages	V_{CC} V_{EE}	+22 -22	+22 -22	+18 -18	Vdc
Differential Input Signal Voltage	V_{ID}	±30	±30	±30	Volts
Common-Mode Input Swing (Note 1)	V_{ICR}	±15	±15	±15	Volts
Output Short-Circuit Duration	t_{OS}	Indefinite			
Power Dissipation (Package Limitation) (Note 2)	P_D	500	500	500	mW
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted, see Note 3.)

Characteristics	Symbol	LM107 LM207 Min	LM107 LM207 Typ	LM107 LM207 Max	LM307 Min	LM307 Typ	LM307 Max	Unit
Input Offset Voltage	$\|V_{IO}\|$							mV
$R_S \le 10$ kΩ, T_A = +25°C		–	0.7	2 0	–	–	–	
$R_S \le 10$ kΩ, $T_A = T_{low}$ to T_{high}		–	–	3.0	–	–	–	
$R_S \le 50$ kΩ, T_A = +25°C		–	–	–	–	2 0	7 5	
$R_S \le 50$ kΩ, $T_A = T_{low}$ to T_{high}		–	–	–	–	–	10	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C		–	1 5	10	–	3 0	50	
$T_A = T_{low}$ to T_{high}		–	–	20	–	–	70	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	30	75	–	70	250	
$T_A = T_{low}$ to T_{high}		–	–	100	–	–	300	
Input Resistance	R_{in}*	1.5	4 0	–	0.5	2.0	–	Megohms
Supply Current	I_D							mA
V_S = ±20 V, T_A = +25°C		–	1.8	3.0	–	–	–	
V_S = ±20 V, $T_A = T_{high}$		–	1.2	2.5	–	–	–	
V_S = ±15 V, T_A = +25°C		–	–	–	–	1 8	3 0	
Large-Signal Voltage Gain	A_v							V/mV
V_S = ±15 V, V_O = ±10 V, $R_L > 2.0$ kΩ, T_A = +25°C		50	160	–	25	160	–	
V_S = ±15 V, V_O = ±10 V, $R_L \geq 2 0$ kΩ, $T_A = T_{low}$		25	–	–	15	–	–	
Average Temperature Coefficient of Input Offset Voltage $T_{low} \le T_A \le T_{high}$	$\|TC_{V_{IO}}\|$	–	3 0	15	–	6 0	30	µV/°C
Average Temperature Coefficient of Input Offset Current	$\|TC_{I_{IO}}\|$							nA/°C
+25°C $\le T_A \le T_{high}$		–	0.01	0.1	–	0 01	0 3	
$T_{low} \le T_A \le$ +25°C		–	0.02	0.2	–	0.02	0.6	
Output Voltage Swing ($T_A = T_{low}$ to T_{high})	V_O							V
V_S = ±15 V, R_L = 10 kΩ		±12	±14	–	±12	+14	–	
R_L = 2.0 kΩ		±10	±13	–	±10	±13	–	
Input Voltage Range ($T_A = T_{low}$ to T_{high})	$V_{in\,R}$							V
V_S = ±20 V		±15	–	–	–	–	–	
V_S = ±15 V		–	–	–	±12	–	–	
Common-Mode Rejection Ratio ($T_A = T_{low}$ to T_{high}) $R_S \leqslant 50$ kΩ	CMRR	80	96	–	70	90	–	dB
Supply-Voltage Rejection Ratio ($T_A = T_{low}$ to T_{high}) $R_S \leqslant 50$ kΩ	VSRR	80	96	–	70	96	–	dB

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage

Note 2. For operating at elevated temperatures, the device must be derated based on a maximum junction temperature of +150°C for the LM107, and 100°C for the LM207 and LM307. The TO-99 package is derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3 Unless otherwise noted, these specifications apply for

	T_{low}	T_{high}	
±5 0 V ≤ V_S ≤ ±20 V,	-55°C ≤ T_A ≤	+125°C,	LM107
±5.0 V ≤ V_S ≤ ±20 V,	-25°C ≤ T_A ≤	+85°C,	LM207
±5.0 V ≤ V_S ≤ ±15 V,	0°C ≤ T_A ≤	+70°C,	LM307

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 – MINIMUM INPUT VOLTAGE RANGE

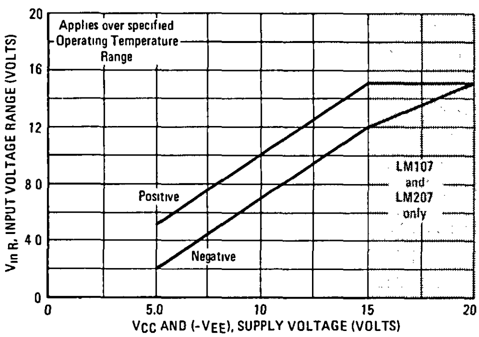


FIGURE 2 – MINIMUM OUTPUT VOLTAGE SWING

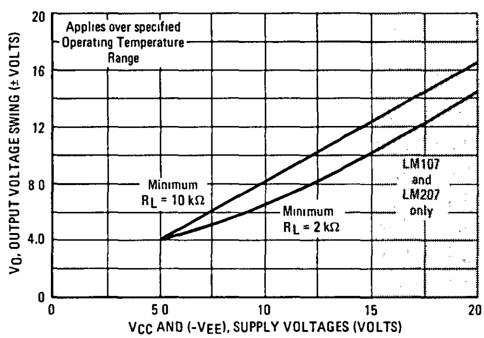


FIGURE 3 – MINIMUM VOLTAGE GAIN

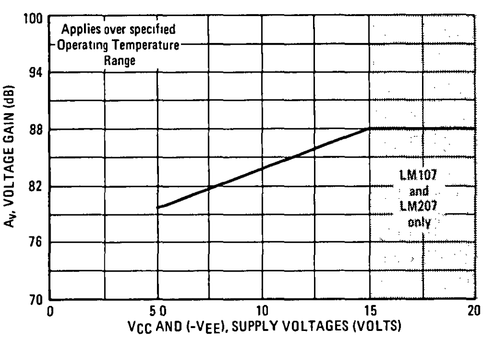


FIGURE 4 – TYPICAL SUPPLY CURRENTS

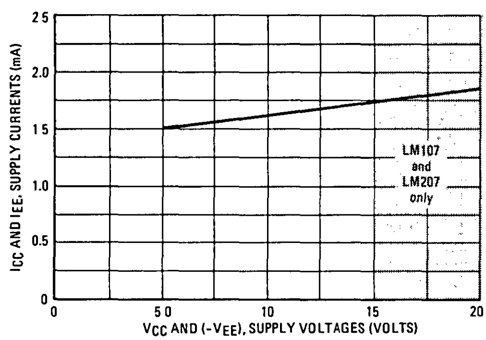


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

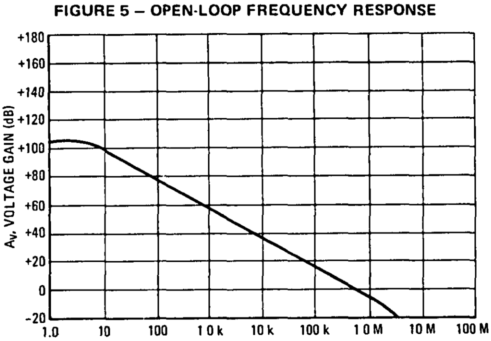
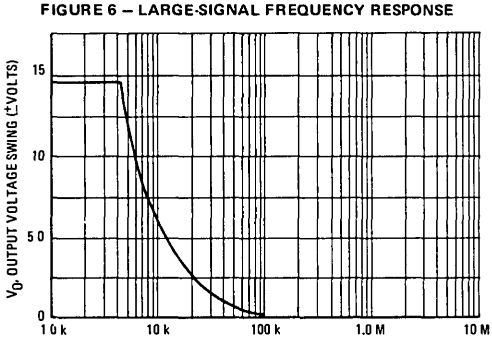


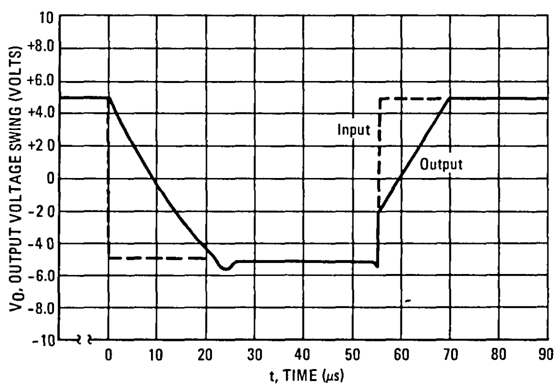
FIGURE 6 – LARGE-SIGNAL FREQUENCY RESPONSE



3

TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – VOLTAGE FOLLOWER PULSE RESPONSE



LM108, LM108A
LM208, LM208A
LM308, LM308A

PRECISION OPERATIONAL AMPLIFIERS

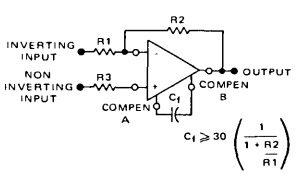
The LM108/LM208/LM308 Series operational amplifiers provide high input impedance, low input offsets and temperature drifts, and low noise. These characteristics are made possible by use of a special Super Beta processing technology. This series of amplifiers is particularly useful for applications where high-accuracy and low-drift performance are essential. In addition high-speed performance may be improved by employing feed-forward compensation techniques to maximize slew rate without compromising other performance criteria.

The LM108A/LM208A/LM308A Series offers extremely low input offset voltage and drift specifications allowing usage in even the most critical applications without external offset nulling.

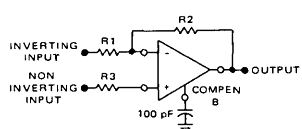
- Operation From a Wide Range of Power Supply Voltages
- Low Input Bias and Offset Currents
- Low Input Offset Voltage and Guaranteed Offset Voltage Drift Performance
- High Input Impedance
- Laser Trimmed and Ion Implanted

FREQUENCY COMPENSATION

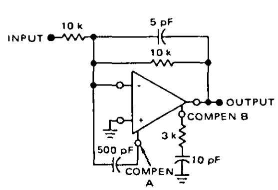
STANDARD COMPENSATION



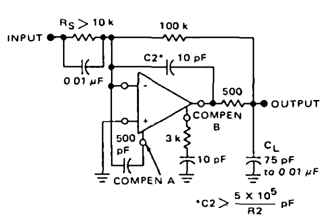
MODIFIED COMPENSATION



STANDARD FEEDFORWARD COMPENSATION



FEEDFORWARD COMPENSATION FOR DECOUPLING LOAD CAPACITANCE



DEVICE SELECTION TABLE

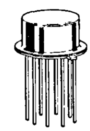
	OPERATING TEMPERATURE RANGE		
	-55 to +125°C	-25 to +85°C	0 to +70°C
STANDARD OFFSET VOLTAGE SPECIFICATION	LM108 Pkg. Suffix	LM208 Pkg. Suffix	LM308 Pkg Suffix
TIGHTENED OFFSET VOLTAGE SPECIFICATION	LM108A Pkg. Suffix	LM208A Pkg. Suffix	LM308A Pkg. Suffix

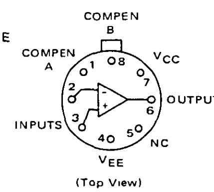
LASER TRIMMED SUPER GAIN OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

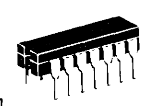
3

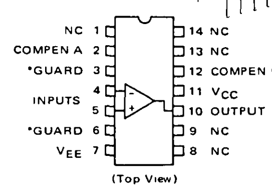
H SUFFIX
METAL PACKAGE
CASE 601



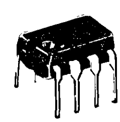


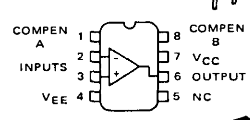
J SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116



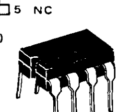


N SUFFIX
PLASTIC PACKAGE
CASE 626
(LM308 only)





D SUFFIX
CERAMIC PACKAGE
CASE 693



*Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	VALUE LM108, LM108A	LM208, LM208A	LM308, LM308A	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±20	±20	±18	Vdc
Input Voltage (See Note 1)	V_I	←±15→			Volts
Input Differential Current (See Note 2)	I_{ID}	←±10→			mA
Output Short-Circuit Duration	t_S	←Indefinite→			
Operating Ambient Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	←-65 to +150→			°C
Junction Temperature	T_J				°C
Metal, Ceramic Package		←+175→			
Plastic Package		←+150→			

Note 1. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.

Note 2. The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless some limiting resistance is used.

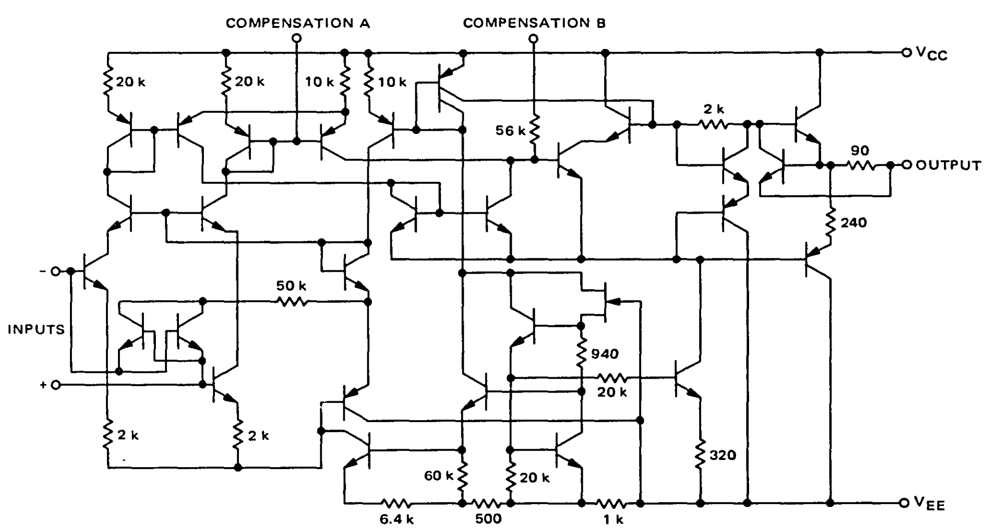
ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of +5.0 V ≤ V_{CC} ≤ +20 V and -5.0 V ≥ V_{EE} ≥ -20 V, T_A = +25°C.)

Characteristic	Symbol	LM108A LM208A Min	Typ	Max	LM108 LM208 Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	–	0.3	0.5	–	0.7	2.0	mV
Input Offset Current	I_{IO}	–	0.05	0.2	–	0.005	0.2	nA
Input Bias Current	I_{IB}	–	0.8	2.0	–	0.8	2.0	nA
Input Resistance	r_i	30	70	–	30	70	–	Megohms
Power Supply Currents V_{CC} = +20 V, V_{EE} = -20 V	I_{CC}, I_{EE}	–	±0.3	±0.6	–	±0.3	±0.6	mA
Large Signal Voltage Gain V_{CC} = |V_{EE}| = +15 V, V_O = ±10 V, R_L ≥ 10 kΩ	A_{VOL}	80	300	–	50	300	–	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage	V_{IO}	–	–	1.0	–	–	3.0	mV
Input Offset Current	I_{IO}	–	–	0.4	–	–	0.4	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(min)$ ≤ T_A ≤ $T_A(max)$	$\Delta V_{IO}/\Delta T$	–	1.0	5.0	–	3.0	15	µV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	0.5	2.5	–	0.5	2.5	pA/°C
Input Bias Current	I_{IB}	–	–	3.0	–	–	3.0	nA
Large Signal Voltage Gain V_{CC} = |V_{EE}| = +15 V, V_O = ±10 V, R_L = 10 kΩ	A_{VOL}	40	–	–	25	–	–	V/mV
Input Voltage Range V_{CC} = |V_{EE}| = +15 V	V_{IR}	±13.5	–	–	±13.5	–	–	V
Common-Mode Rejection Ratio	CMRR	96	110	–	85	100	–	dB
Power Supply Voltage Rejection Ratio	PSSR	96	100	–	80	96	–	dB
Output Voltage Range V_{CC} = |V_{EE}| = +15 V, R_L = 10 kΩ	V_{OR}	±13	±14	–	±13	±14	–	V
Supply Current (T_A = T_A(max))	I_{CC}, I_{EE}	–	±0.15	±0.4	–	±0.15	±0.4	mA

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of +5.0 V $\leqslant V_{CC} \leqslant$ +15 V and -5.0 V $\geqslant V_{EE} \geqslant$ -15 V, T_A = +25°C.)

Characteristic	Symbol	LM308A Min	LM308A Typ	LM308A Max	LM308 Min	LM308 Typ	LM308 Max	Unit
Input Offset Voltage	V_{IO}	–	0.3	0.5	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	0.2	1.0	–	0.2	1.0	nA
Input Bias Current	I_{IB}	–	1.5	7.0	–	1.5	7.0	nA
Input Resistance	r_i	10	40	–	10	40	–	Megohms
Power Supply Currents V_{CC} = +15 V, V_{EE} = -15 V	I_{CC}, I_{EE}	–	±0.3	±0.8	–	±0.3	±0.8	mA
Large Signal Voltage Gain V_{CC} = +15 V, V_{EE} = -15 V, V_O = ±10 V, $R_L \geqslant$ 10 kΩ	A_{VOL}	80	300	–	25	300	–	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage	V_{IO}	–	–	0.73	–	–	10	mV
Input Offset Current	I_{IO}	–	–	1.5	–	–	1.5	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(min) \leqslant T_A \leqslant T_A(max)$	$\Delta V_{IO}/\Delta T$	–	1.0	5.0	–	6.0	30	μV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	2.0	10	–	2.0	10	pA/°C
Input Bias Current	I_{IB}	–	–	10	–	–	10	nA
Large Signal Voltage Gain V_{CC} = +15 V, V_{EE} = -15 V, V_O = ±10 V, $R_L \geqslant$ 10 kΩ	A_{VOL}	60	–	–	15	–	–	V/mV
Input Voltage Range V_{CC} = +15 V, V_{EE} = -15 V	V_{IR}	±13.5	–	–	±13.5	–	–	V
Common-Mode Rejection Ratio $R_S \leqslant$ 50 kΩ	CMRR	96	110	–	80	100	–	dB
Supply Voltage Rejection Ratio $R_S \leqslant$ 50 kΩ	PSSR	96	110	–	80	96	–	dB
Output Voltage Range V_{CC} = +15 V, V_{EE} = -15 V, R_L = 10 kΩ	V_{OR}	±13	±14	–	±13	±14	–	V

REPRESENTATIVE CIRCUIT SCHEMATIC



3

TYPICAL CHARACTERISTICS

FIGURE 1 – INPUT BIAS AND INPUT OFFSET CURRENTS

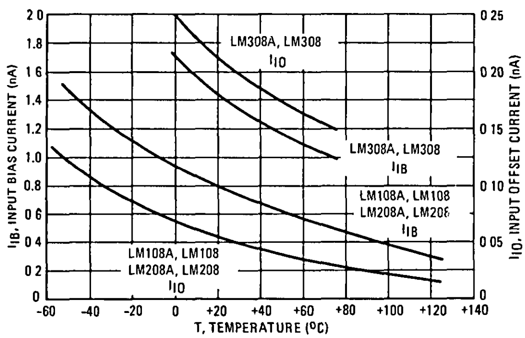


FIGURE 2 – MAXIMUM EQUIVALENT INPUT OFFSET VOLTAGE ERROR versus INPUT RESISTANCE

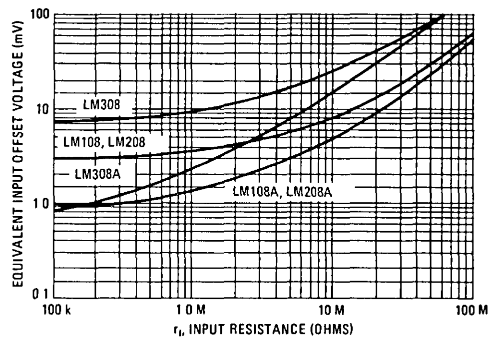


FIGURE 3 – VOLTAGE GAIN versus SUPPLY VOLTAGES

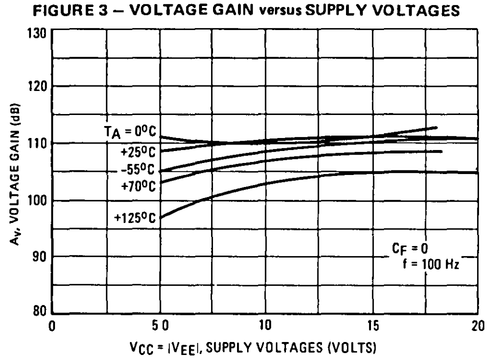


FIGURE 4 – POWER SUPPLY CURRENTS versus POWER SUPPLY VOLTAGE

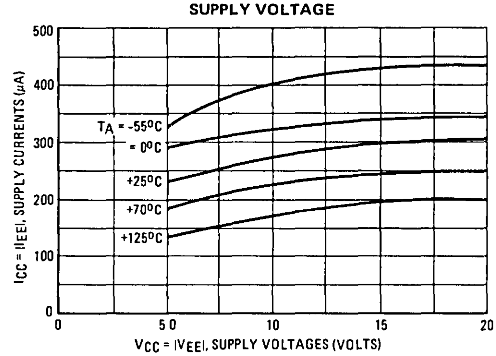


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

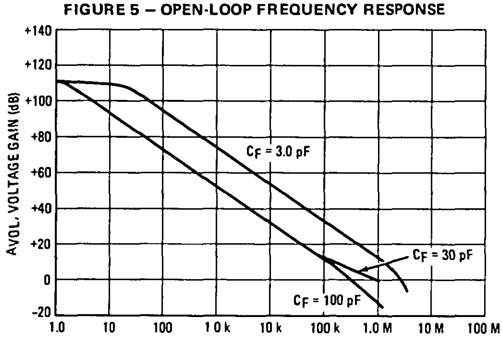
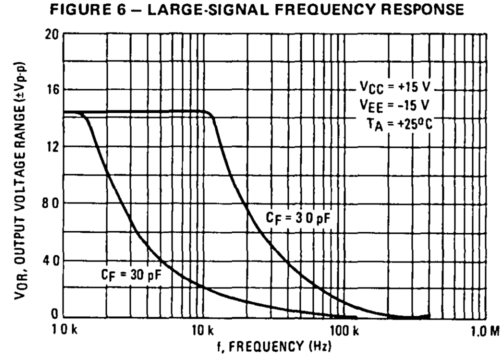
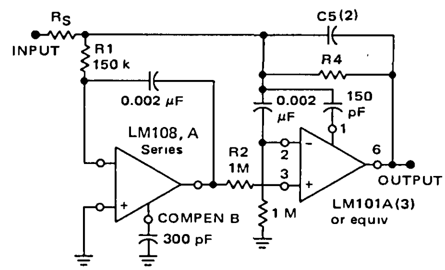


FIGURE 6 – LARGE-SIGNAL FREQUENCY RESPONSE



SUGGESTED DESIGN APPLICATIONS

FIGURE 7 – FAST (1) SUMMING AMPLIFIER WITH LOW INPUT CURRENT

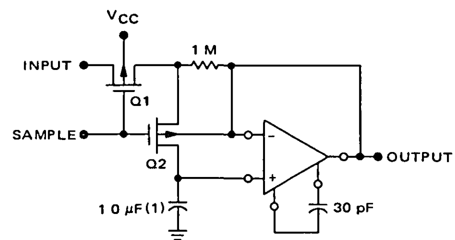


(1) Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/μs

(2) $C5 = \frac{6 \times 10^{-8}}{R1}$

(3) In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

FIGURE 8 – SAMPLE AND HOLD



(1) Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

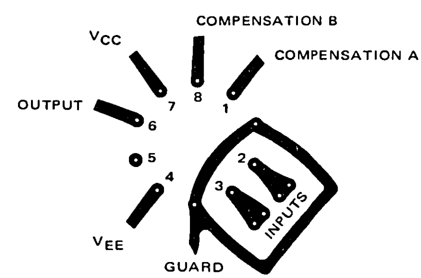
INPUT GUARDING

Special care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the LM108, A amplifier series. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at +125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 type package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the boards. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

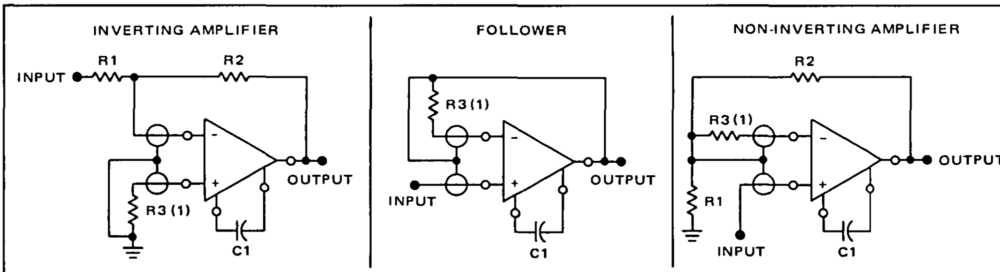
The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard MC1741 and LM101A pin configuration).

FIGURE 9 – SUGGESTED PRINTED CIRCUIT BOARD LAYOUT for INPUT GUARDING USING METAL PACKAGED DEVICE



(BOTTOM VIEW)

FIGURE 10 – CONNECTION OF INPUT GUARDS



(1) Used to compensate for large source resistances.

Note: $\frac{R1\,R2}{R1 + R2}$ must be an impedance.

LM124, LM224, LM324, LM2902

Specifications and Applications Information

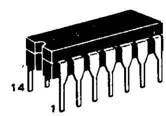
QUAD LOW POWER OPERATIONAL AMPLIFIERS

The LM124 Series are low-cost, quad operational amplifiers with true differential inputs. These have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 32 Volts with quiescent currents about one fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

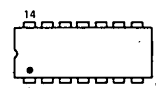
- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents: 250 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

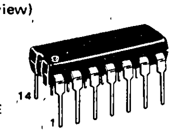
SILICON MONOLITHIC INTEGRATED CIRCUIT



J SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

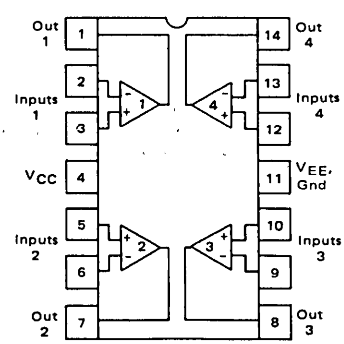


(top view)



N SUFFIX
PLASTIC PACKAGE
CASE 646
(LM224, LM324, LM2902 only)

PIN CONNECTIONS



(top view)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	LM124 LM224 LM324	LM2902	Unit
Power Supply Voltages				Vdc
Single Supply	V_{CC}	32	26	
Split Supplies	V_{CC}, V_{EE}	±16	±13	
Input Differential Voltage Range (1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	-0.3 to 32	-0.3 to 26	Vdc
Input Forward Current (3) (V_I < -0.3 V)	I_{IF}	50	–	mA
Output Short Circuit Duration	t_S	Continuous		
Junction Temperature	T_J			°C
Ceramic and Metal Packages		175		
Plastic Package		150		
Storage Temperature Range	T_{stg}			°C
Ceramic and Metal Packages		-65 to +150		
Plastic Package		-55 to +125		
Operating Ambient Temperature Range	T_A			°C
LM124		-55 to +125	–	
LM224		-25 to +85	–	
LM324		0 to +70	–	
LM2902		–	-40 to +85	

(1) Split Power Supplies
(2) For Supply Voltages less than 32 V for the LM124/224/324 and 26 V for the LM2902, the absolute maximum input voltage is equal to the supply voltage.
(3) This input current will only exist when the voltage is negative at any of the input leads. Normal output states will reestablish when the input voltage returns to a voltage greater than -0.3 V.

ORDERING INFORMATION

Device	Temperature Range	Package
LM124J	-55 to +125°C	Ceramic DIP
LM2902J	-40 to +85°C	Ceramic DIP
LM2902N	-40 to +85°C	Plastic DIP
LM224J	-25 to +85°C	Ceramic DIP
LM224N	-25 to +85°C	Plastic DIP
LM324J	0 to +70°C	Ceramic DIP
LM324N	0 to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	LM124/LM224 Min	LM124/LM224 Typ	LM124/LM224 Max	LM324 Min	LM324 Typ	LM324 Max	LM2902 Min	LM2902 Typ	LM2902 Max	Unit
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2902), V_{IC} = 0 V to V_{CC} − 1.7 V, $V_O \simeq$ 1.4 V, R_S = 0 Ω T_A = 25°C T_A = T_{high} to T_{low} (Note 1)	V_{IO}	– –	2.0 –	5.0 7.0	– –	2.0 –	7.0 9.0	– –	2.0 –	7.0 10	mV
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	–	7.0	–	µV/°C
Input Offset Current T_A = T_{high} to T_{low} (Note 1)	I_{IO}	– –	3.0 –	30 100	– –	5.0 –	50 150	– –	5.0 45	50 200	nA
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	pA/°C
Input Bias Current T_A = T_{high} to T_{low} (Note 1)	I_{IB}	– –	-45 -50	-150 -300	– –	-45 -50	-250 -500	– –	-45 -50	-250 -500	nA
Input Common-Mode Voltage Range (Note 2) V_{CC} = 30 V (26 V for LM2902) V_{CC} = 30 V (26 V for LM2902), T_A = T_{high} to T_{low}	V_{ICR}	0 0	– –	28.3 28	0 0	– –	28.3 28	0 0	– –	24.3 24	V
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open-Loop Voltage Gain R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing, T_A = T_{high} to T_{low} (Note 1)	A_{VOL}	50 25	100 –	– –	25 15	100 –	– –	– –	100 –	– –	V/mV
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	–	–	-120	–	–	-120	–	–	-120	–	dB
Common-Mode Rejection Ratio R_S ≤ 10 kΩ	CMRR	70	85	–	65	70	–	50	70	–	dB
Power Supply Rejection Ratio	PSRR	65	100	–	65	100	–	50	100	–	dB
Output Voltage Range R_L = 2 kΩ (R_L ≥ 10 kΩ for LM2902),	V_{OR}	0	–	3.3	0	–	3.3	0	–	3.3	V
Output Voltage–High Limit (T_A = T_{high} to T_{low})(Note 1) V_{CC} = 30 V (26 V for LM2902), R_L = 2 kΩ V_{CC} = 30 V (26 V for LM2902), R_L = 10 kΩ	V_{OH}	26 27	– 28	– –	26 27	– 28	– –	22 23	– 24	– –	V
Output Voltage–Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note 1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	100	mV
Output Source Current (V_{ID} = +1.0 V, V_{CC} = 15 V) T_A = 25°C T_A = T_{high} to T_{low} (Note 1)	I_{O+}	20 10	40 20	– –	20 10	40 20	– –	20 10	40 20	– –	mA
Output Sink Current V_{ID} = −1.0 V, V_{CC} = 15 V T_A = 25°C T_A = T_{high} to T_{low} (Note 1) V_{ID} = −1.0 V, V_O = 200 mV, T_A = 25°C	I_{O-}	10 5 12	20 8 50	– – –	10 5 12	20 8 50	– – –	10 5 –	20 8 –	– – –	mA µA
Output Short Circuit to Ground (Note 3)	I_{os}	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low})(Note 1) V_{CC} = 30 V (26 V for LM2902), V_O = 0 V, R_L = ∞ V_{CC} = 5 V, V_O = 0 V, R_L = ∞	I_{CC}	– –	1.5 0.7	3.0 1.2	– –	1.5 0.7	3.0 1.2	– –	1.5 0.7	3.0 1.2	mA

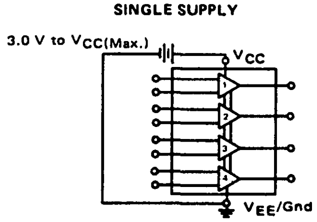
NOTES:

(1) T_{low} = −55°C for LM124; = −40°C for LM2902; = −25°C for LM224; = 0°C for LM324
T_{high} = +125°C for LM124; = +85°C for LM2902 and LM224; = +70°C for LM324

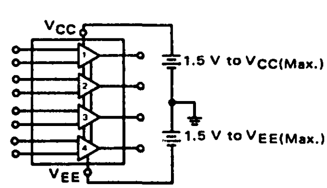
(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} − 1.7 V, but either or both inputs can go to +32 V without damage (+26 V for LM2902).

(3) Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

SINGLE SUPPLY

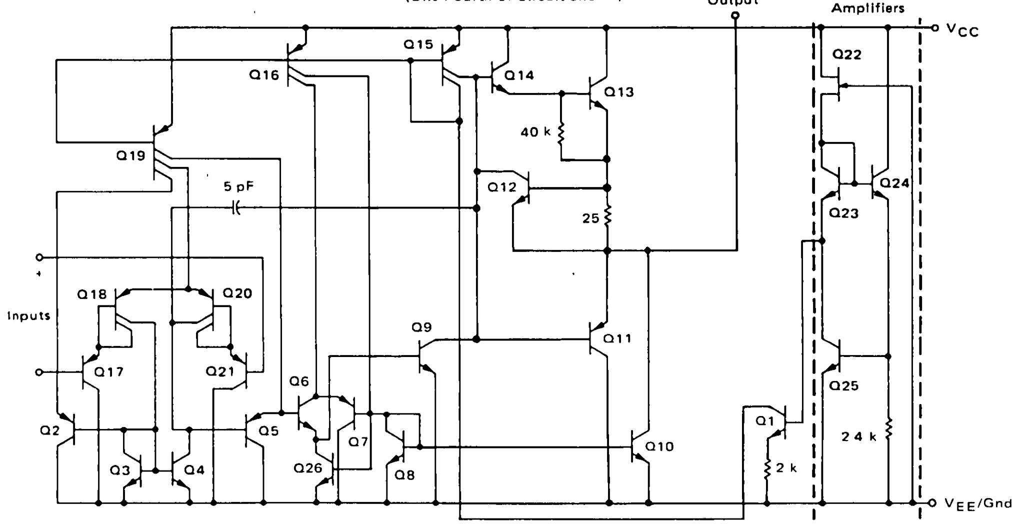


SPLIT SUPPLIES

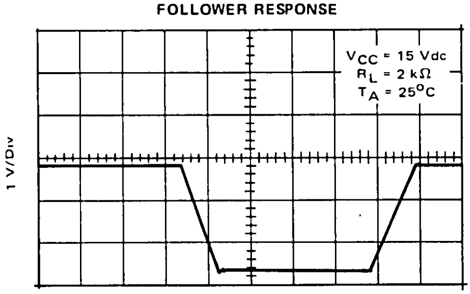


3

REPRESENTATIVE CIRCUIT SCHEMATIC
(One-Fourth of Circuit Shown)



LARGE SIGNAL VOLTAGE
FOLLOWER RESPONSE



CIRCUIT DESCRIPTION

The LM124 Series is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

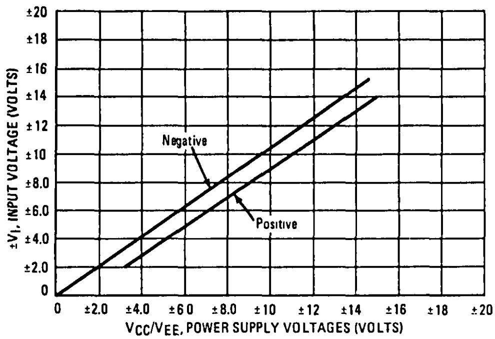


FIGURE 2 – OPEN LOOP FREQUENCY

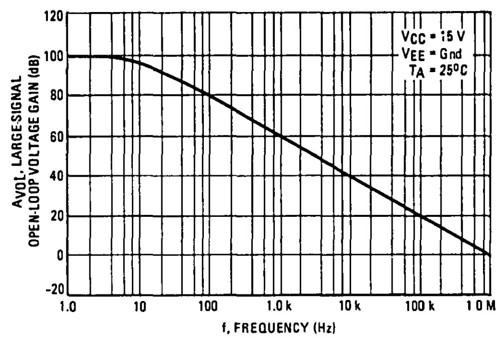


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

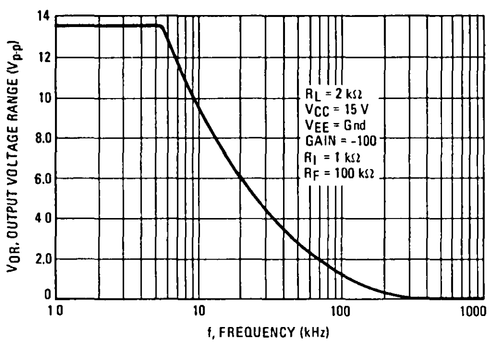


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)

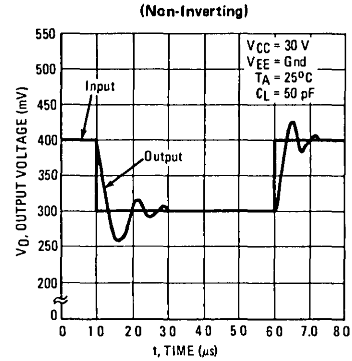


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

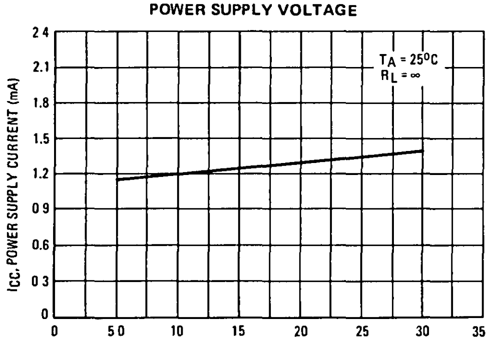
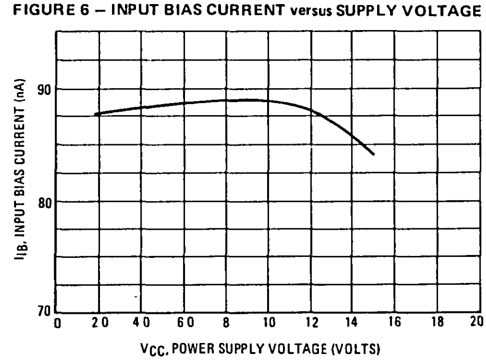


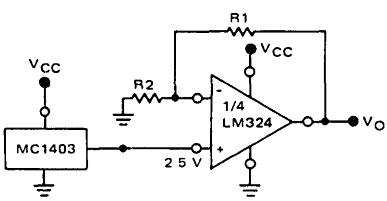
FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



3

APPLICATIONS INFORMATION

FIGURE 7 – VOLTAGE REFERENCE



$V_O = 2.5\ V(1 + \frac{R1}{R2})$

FIGURE 8 – WIEN BRIDGE OSCILLATOR

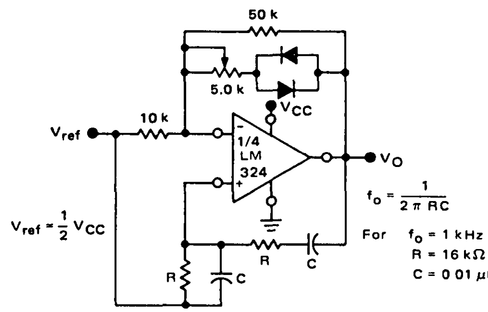
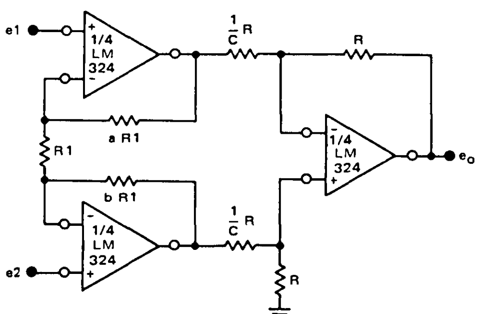
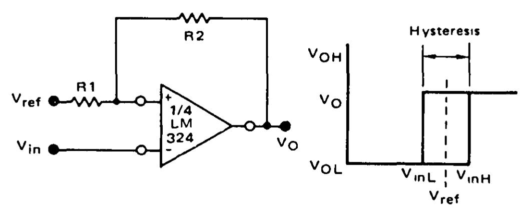


FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$e_o = C\ (1 + a + b)\ (e2 - e1)$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

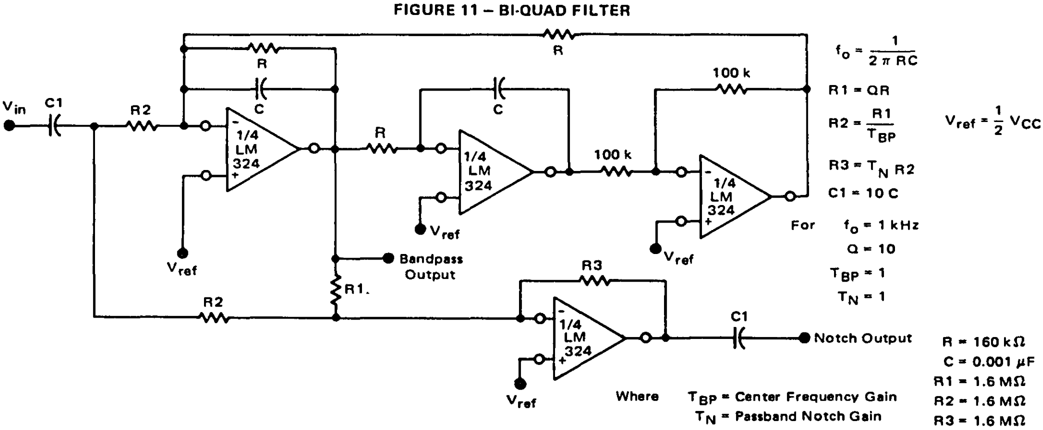


$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{ref}) + V_{ref}$

$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{ref}) + V_{ref}$

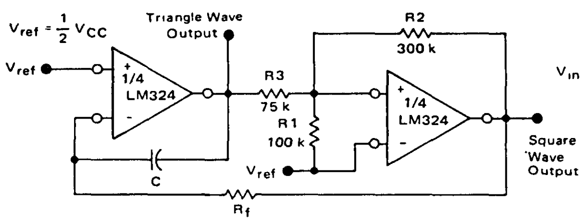
$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

FIGURE 11 – BI-QUAD FILTER



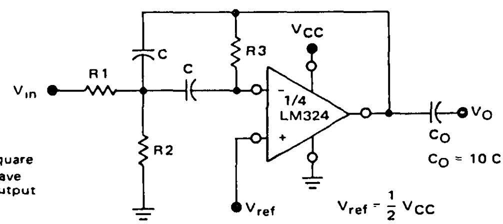
APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o\,f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

3

LM158, LM258, LM358, LM2904

Specifications and Applications Information

DUAL LOW POWER OPERATIONAL AMPLIFIERS

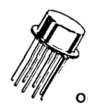
Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The LM158 Series is equivalent to one-half of an LM124.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 32 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

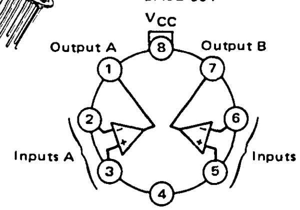
- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- Similar Performance to the Popular MC1558

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

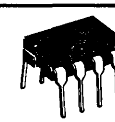
SILICON MONOLITHIC INTEGRATED CIRCUIT



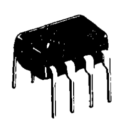
H SUFFIX
METAL PACKAGE
CASE 601



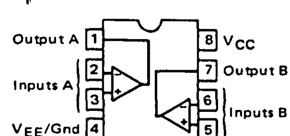
(Top View)



J SUFFIX
CERAMIC PACKAGE
CASE 693



N SUFFIX
PLASTIC PACKAGE
CASE 626
(LM258, LM358, LM2904 only)



(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	LM158 LM258 LM358	LM2904	Unit
Power Supply Voltages				Vdc
Single Supply	V_{CC}	32	26	
Split Supplies	V_{CC}, V_{EE}	±16	±13	
Input Differential Voltage Range (1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	-0.3 to 32	-0.3 to 26	Vdc
Input Forward Current (3) (V_I < -0.3 V)	I_{IF}	50	–	mA
Output Short Circuit Duration	t_S	Continuous		
Junction Temperature	T_J			°C
Ceramic and Metal Packages		175		
Plastic Package		150		
Storage Temperature Range	T_{stg}			°C
Ceramic and Metal Packages		-65 to +150		
Plastic Package		-55 to +125		
Operating Ambient Temperature Range	T_A			°C
LM158		-55 to +125	–	
LM258		-25 to +85	–	
LM358		0 to +70	–	
LM2904		–	-40 to +85	

(1) Split Power Supplies
(2) For Supply Voltages less than 32 V for the LM158/258/358 and 26 V for the LM2904, the absolute maximum input voltage is equal to the supply voltage.
(3) This input current will only exist when the voltage is negative at any of the input leads. Normal output states will reestablish when the input voltage returns to a voltage greater than -0.3 V.

ORDERING INFORMATION

Device	Temperature Range	Package
LM158H	-55 to +125°C	Metal Can
LM158J	-55 to +125°C	Ceramic DIP
LM2904H	-40 to +85°C	Metal Can
LM2904J	-40 to +85°C	Ceramic DIP
LM2904N	-40 to +85°C	Plastic DIP
LM258H	-25 to +85°C	Metal Can
LM258J	-25 to +85°C	Ceramic DIP
LM258N	-25 to +85°C	Plastic DIP
LM358H	0 to +70°C	Metal Can
LM358J	0 to +70°C	Ceramic DIP
LM358N	0 to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	LM158/LM258 Min	Typ	Max	LM358 Min	Typ	Max	LM2904 Min	Typ	Max	Unit
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2904), V_{IC} = 0 V to V_{CC} − 1.7 V, $V_O \simeq$ 1.4 V, R_S = 0 Ω	V_{IO}										mV
T_A = 25°C		–	2.0	5.0	–	2.0	7.0	–	2.0	7.0	
T_A = T_{high} to T_{low} (Note 1)		–	–	7.0	–	–	9.0	–	–	10	
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	–	7.0	–	μV/°C
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	50	–	5.0	50	nA
T_A = T_{high} to T_{low} (Note 1)		–	–	100	–	–	150	–	45	200	
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	pA/°C
Input Bias Current	I_{IB}	–	-45	-150	–	-45	-250	–	-45	-250	nA
T_A = T_{high} to T_{low} (Note 1)		–	-50	-300	–	-50	-500	–	-50	-500	
Input Common-Mode Voltage Range (Note 2)	V_{ICR}										V
V_{CC} = 30 V (26 V for LM2904)		0	–	28.3	0	–	28.3	0	–	24.3	
V_{CC} = 30 V (26 V for LM2904), T_A = T_{high} to T_{low}		0	–	28	0	–	28	0	–	24	
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open-Loop Voltage Gain	A_{VOL}										V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing,		50	100	–	25	100	–	–	100	–	
T_A = T_{high} to T_{low} (Note 1)		25	–	–	15	–	–	–	–	–	
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	–	–	-120	–	–	-120	–	–	-120	–	dB
Common-Mode Rejection Ratio R_S ≤ 10 kΩ	CMRR	70	85	–	65	70	–	50	70	–	dB
Power Supply Rejection Ratio	PSRR	65	100	–	65	100	–	50	100	–	dB
Output Voltage Range R_L = 2 kΩ (R_L ≥ 10 kΩ for LM2904)	V_{OR}	0	–	3.3	0	–	3.3	0	–	3.3	V
Output Voltage—High Limit (T_A = T_{high} to T_{low})(Note 1)	V_{OH}										V
V_{CC} = 30 V (26 V for LM2904), R_L = 2 kΩ		26	–	–	26	–	–	22	–	–	
V_{CC} = 30 V (26 V for LM2904), R_L = 10 kΩ		27	28	–	27	28	–	23	24	–	
Output Voltage—Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note 1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	mV
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	–	20	40	–	20	40	–	mA
Output Sink Current	I_{O-}										
V_{ID} = -1.0 V, V_{CC} = 15 V		10	20	–	10	20	–	10	20	–	mA
V_{ID} = -1.0 V, V_O = 200 mV		12	50	–	12	50	–	–	–	–	μA
Output Short Circuit to Ground (Note 3)	I_{os}	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low})(Note 1)	I_{CC}										mA
V_{CC} = 30 V (26 V for LM2904), V_O = 0 V, R_L = ∞		–	1.5	3.0	–	1.5	3.0	–	1.5	3.0	
V_{CC} = 5 V, V_O = 0 V, R_L = ∞		–	0.7	1.2	–	0.7	1.2	–	0.7	1.2	

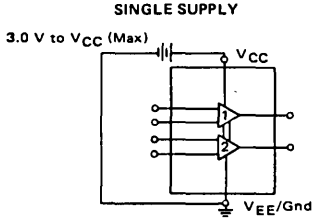
NOTES:

(1) T_{low} = -55°C for LM158 T_{high} = +125°C for LM158
= -40°C for LM2904 = +85°C for LM2904
= -25°C for LM258 and LM258
= 0°C for LM358 = +70°C for LM358

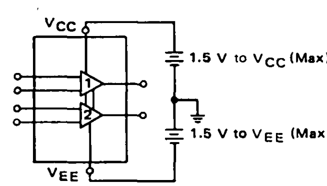
(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} − 1.7 V, but either or both inputs can go to +32 V without damage (+26 V for LM2904).

(3) Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

SINGLE SUPPLY

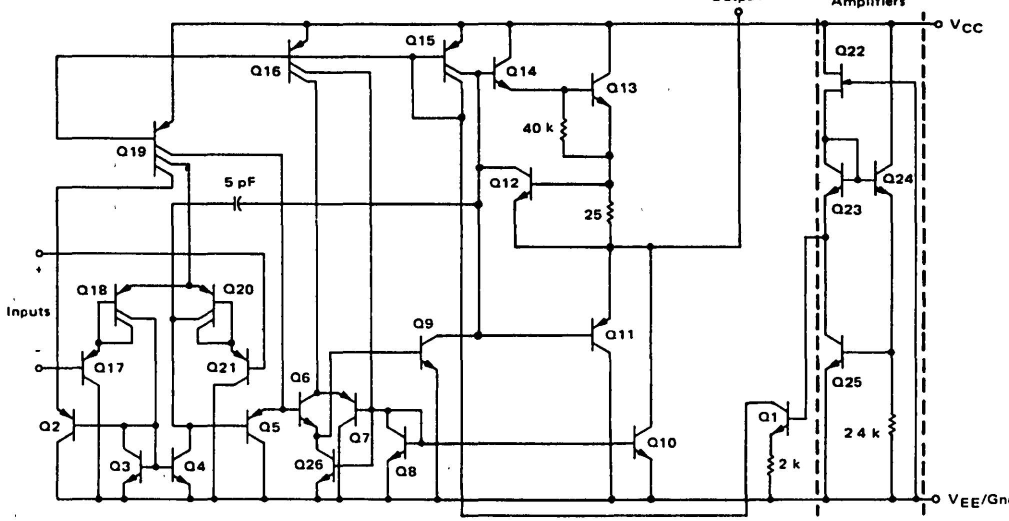


SPLIT SUPPLIES

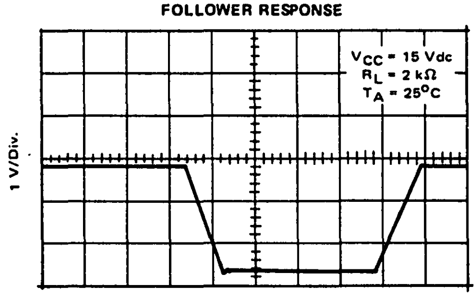


3

REPRESENTATIVE CIRCUIT SCHEMATIC
(One-Half of Circuit Shown)



LARGE SIGNAL VOLTAGE FOLLOWER RESPONSE



5.0 μs/Div.

CIRCUIT DESCRIPTION

The LM158 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

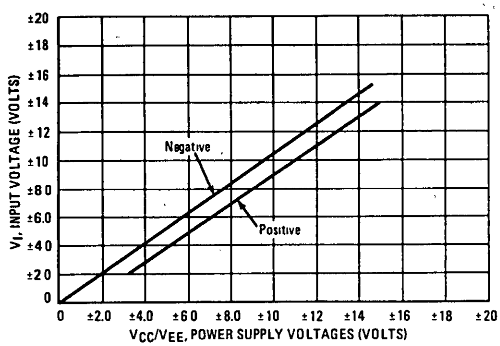


FIGURE 2 – OPEN LOOP FREQUENCY

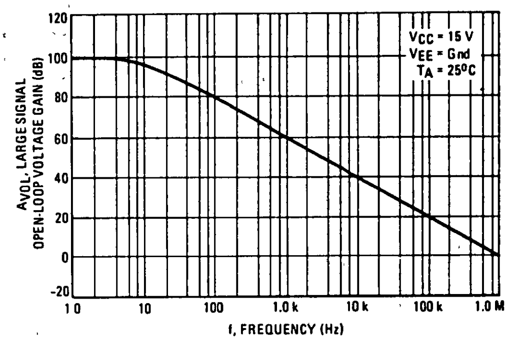


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

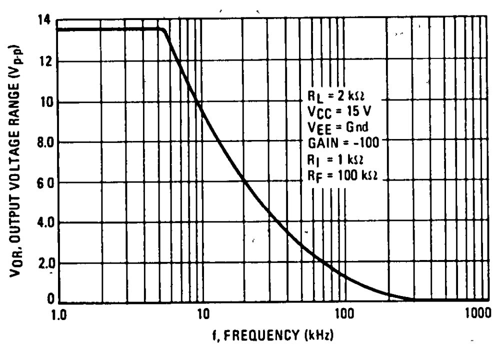


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)

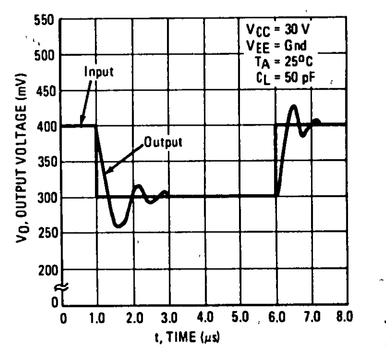


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

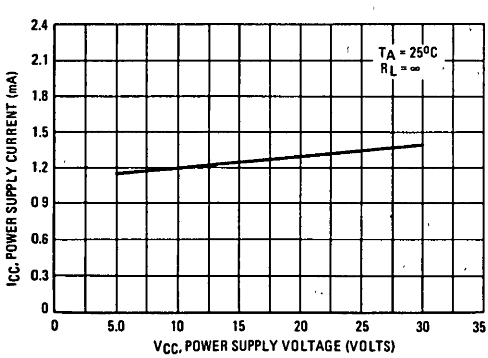
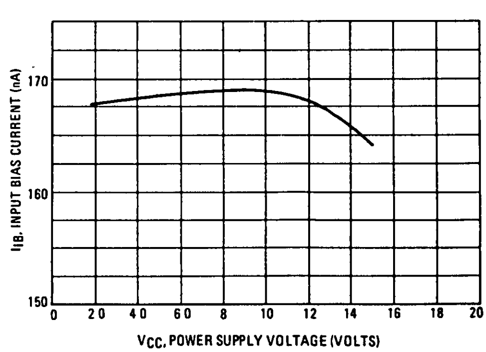


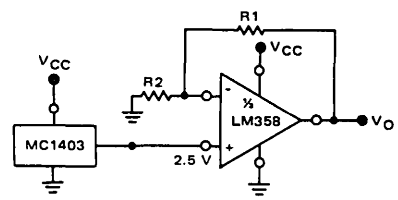
FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



3

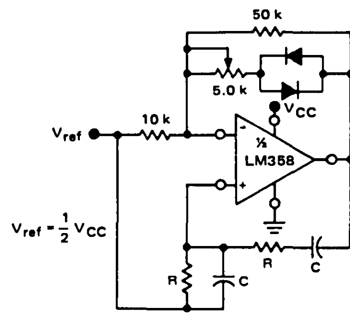
APPLICATIONS INFORMATION

FIGURE 7 – VOLTAGE REFERENCE



$$V_O = 2.5\ V\left(1 + \frac{R1}{R2}\right)$$

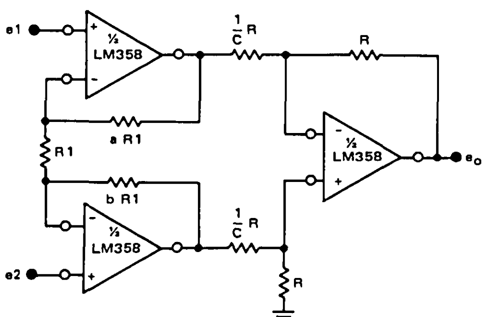
FIGURE 8 – WIEN BRIDGE OSCILLATOR



$$f_o = \frac{1}{2\pi RC}$$

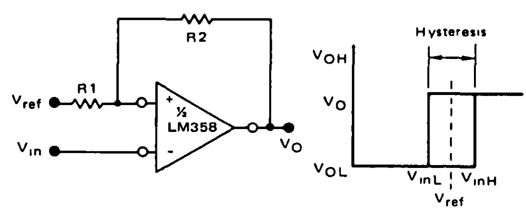
For $f_o = 1\ kHz$
$R = 16\ k\Omega$
$C = 0.01\ \mu F$

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$$e_o = C\ (1 + a + b)\ (e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

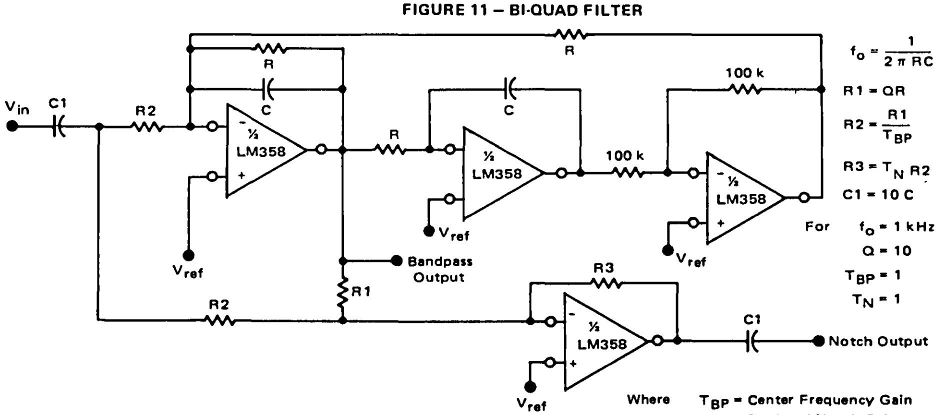


$$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER



$$f_o = \frac{1}{2\pi RC}$$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N\ R2$

$C1 = 10\ C$

$V_{ref} = \frac{1}{2} V_{CC}$

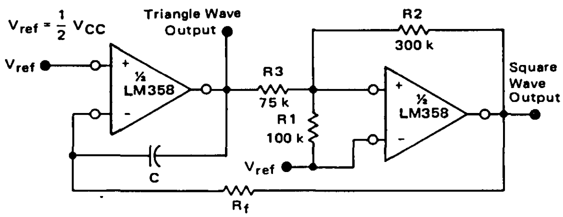
For $f_o = 1\ kHz$
$Q = 10$
$T_{BP} = 1$
$T_N = 1$

$R = 160\ k\Omega$
$C = 0.001\ \mu F$
$R1 = 1.6\ M\Omega$
$R2 = 1.6\ M\Omega$
$R3 = 1.6\ M\Omega$

Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

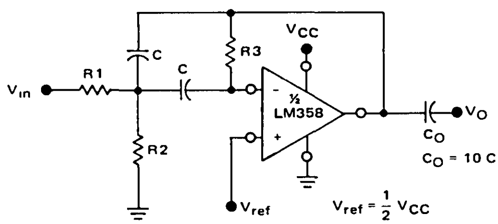
APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4\, C R_f\, R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2\, A(f_o)}$$

$$R2 = \frac{R1\ R3}{4Q^2\, R1 - R3}$$

For less than 10% error from operational amplifier

$\frac{Q_o f_o}{BW} < 0.1$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters

ORDERING INFORMATION

Device	Temperature Range	Package
MC1420G	0°C to +70°C	Metal Can
MC1520F	−55°C to +125°C	Ceramic Flat
MC1520G	−55°C to +125°C	Metal Can

MC1420
MC1520

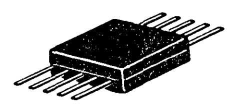
DIFFERENTIAL OUTPUT OPERATIONAL AMPLIFIER

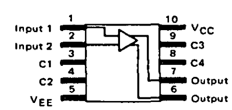
A wide-band, general-purpose operational amplifier which features both differential inputs and outputs. Open loop gain is approximately 3000 V/V but may be adjusted with external feedback components. This device is particularly useful in applications which require differential outputs.

- Differential Input and Differential Output
- Wide Closed-Loop Bandwidth; 10 MHz
- Differential Gain; 70 dB
- High Input Impedance; 2.0 Megohms:
- Low Output Impedance; 50 ohms

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



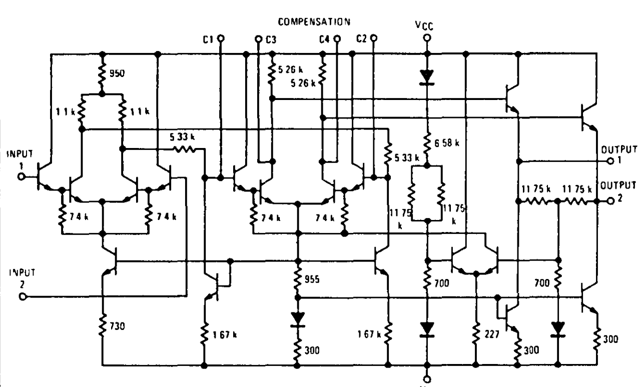


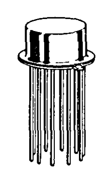
F SUFFIX
CERAMIC PACKAGE
CASE 606
(TO-91)

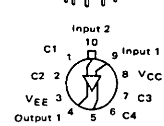
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 -8.0	Vdc
Differential Input Signal	V_{in}	±8.0	Vdc
Load Current	I_{L1}, I_{L2}	15	mA
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Flat Package Derate above T_A = +25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range MC1520 MC1420	T_A	-55 to +125 0 to + 75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – CIRCUIT SCHEMATIC







(TOP VIEW)
G SUFFIX
METAL PACKAGE
CASE 603

SINGLE-ENDED ELECTRICAL CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1520			MC1420			Unit
		Min	Typ	Max	Min	Typ	Max	
Open Loop Voltage Gain (T_{low} ② ≦ T_A ≦ T_{high} ②)	A_{vol}	1000 60	1500 64	– –	750 –	1500 64	– –	V/V dB
Output Impedance (f = 20 Hz)	z_{os}	–	50	100	–	50	–	ohms
Input Impedance (f = 20 Hz)	z_{is}	0.5	2.0	–	–	2.0	–	megohms
Output Voltage Swing (R_L = 7.0 kΩ [Figure 8])	V_O	±3.5	±4.0	–	±3.0	±4.0	–	V_{peak}
Input Common-Mode Voltage Swing	V_{ICR}	±2.0	±3.0	–	–	±3.0	–	V_{peak}
Common-Mode Rejection Ratio	CMRR	75	90	–	60	90	–	dB
Input Bias Current $\left(\left[I_{IB} = \frac{I_1 + I_2}{2}\right], T_A = +25^oC\right)$	I_{IB}	–	0.8	2.0	–	2.0	4.0	µA
Input Offset Current ($I_{IO} = I_1 - I_2$) ($I_{IO} = I_1 - I_2, T_A = T_{low}$) ($I_{IO} = I_1 - I_2, T_A = T_{high}$)	$\|I_{IO}\|$	– – –	30 – –	100 200 200	– – –	30 – –	200 – –	nA
Input Offset Voltage (T_A = +25°C)	$\|V_{IO}\|$	–	5.0	10	–	5.0	15	mV
Step Response Gain = 1.0, 10% Overshoot R_1 = 10 kΩ R_2 = 10 kΩ R_3 = 5.0 kΩ C_s = 39 pF	t_{THL} t_{PLH}, t_{PHL} dV_{out}/dt ①	– – –	80 70 5.0	– – –	– – –	80 70 5.0	– – –	ns ns V/µs
Gain = 10, 10% Overshoot R_1 = 10 kΩ R_2 = 100 kΩ R_3 = 10 kΩ C_s = 10 pF	t_{THL} t_{PLH}, t_{PHL} dV_{out}/dt ①	– – –	80 70 15	– – –	– – –	80 70 15	– – –	ns ns V/µs
Gain = 100, No Overshoot R_1 = 1.0 kΩ R_2 = 100 kΩ R_3 = 1.0 kΩ C_s = 1.0 pF	t_{THL} t_{PLH}, t_{PHL} dV_{out}/dt ①	– – –	80 70 30	– – –	– – –	80 70 30	– – –	ns ns V/µs
Open Loop, No Overshoot R_1 = 50 Ω R_2 = ∞ R_3 = 50 Ω C_s = 0	t_{THL} t_{PLH}, t_{PHL} dV_{out}/dt ①	– – –	180 70 35	– – –	– – –	180 70 35	– – –	ns ns V/µs
Bandwidth: (Open Loop [Figure 4]) (Closed Loop [Unity Gain]) (Figure 5)	–	– –	2.0 10	– –	– –	2.0 10	– –	MHz
Input Noise Voltage (Open Loop) (5.0 Hz – 5.0 MHz)	$V_{n(in)}$	–	11	15	–	11	–	µV(rms)
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low} to T_{high})	$\Delta V_{IO}/\Delta T$	–	2.0	–	–	2.0	–	µV/°C
DC Power Dissipation (V_O = 0)	P_D	–	120	240	–	120	240	mW
Power Supply Sensitivity (V_O = 0)	$S^{\pm}$	–	250	450	–	250	–	µV/V

① dV_{out}/dt = Slew Rate ② T_{low} = 0°C for MC1420, -55°C for MC1520; T_{high} = +75°C for MC1420, +125°C for MC1520

DIFFERENTIAL ELECTRICAL CHARACTERISTICS

(V_{CC} = +6 0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C, unless otherwise noted.)

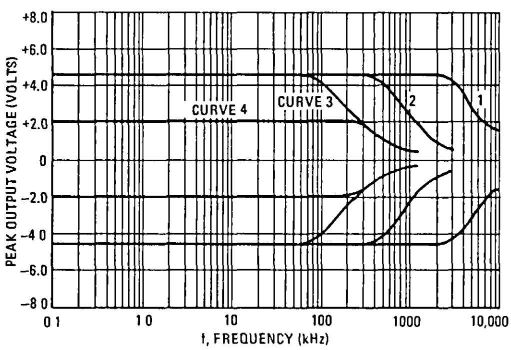
Characteristic	Symbol	MC1520 Min	MC1520 Typ	MC1520 Max	MC1420 Min	MC1420 Typ	MC1420 Max	Unit
Gain (Open Loop)	A_{vol}	2000 66	3000 70	– –	1500 64	3000 70	– –	V/V dB
Input Impedance (f = 20 Hz)	z_{id}	0.5	2.0	–	–	2.0	–	megohms
Output Impedance (f = 20 Hz)	z_{od}	–	100	200	–	100	–	ohms
Common-Mode Output Voltage	$V_{O(CM)}$	-0.5	0	+0.5	–	0	–	Vdc
Output Voltage Swing (R_L = 7.0 kΩ)	V_O	±7.0	±8.0	–	±6.0	±8.0	–	V_{peak}

3

TYPICAL CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6 0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY



TEST CIRCUIT

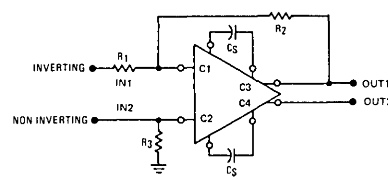


FIGURE NO	CURVE NO	MODE	VOLTAGE GAIN	TEST CONDITIONS R1 (Ω)	R2 (Ω)	R3 (Ω)	CS (pF)	NOISE OUTPUT mV (rms)
2	1	INVERTING	100	1 0 k	100 k	1 0 k	1 0	2 0
	2	INVERTING	10	10 k	100 k	10 k	10	0 55
	3	INVERTING	1 0	10 k	10 k	5 0 k	39	0 17
	4	NON INVERTING	1 0	∞	10 k	10 k	39	0 17
3	1	NON INVERTING	A_{vol}	0	∞	50	1 0	1 0
	2	NON INVERTING	A_{vol}	0	∞	50	10	2 0
	3	NON INVERTING	A_{vol}	0	∞	50	39	5 2
4	1	NON INVERTING	100	100	10 k	100	1 0	2 0
	2	NON INVERTING	10	1 0 k	9 1 k	910	10	0 55
	3	NON INVERTING	1 0	∞	10 k	10 k	39	0 17

FIGURE 3 – OPEN LOOP VOLTAGE GAIN

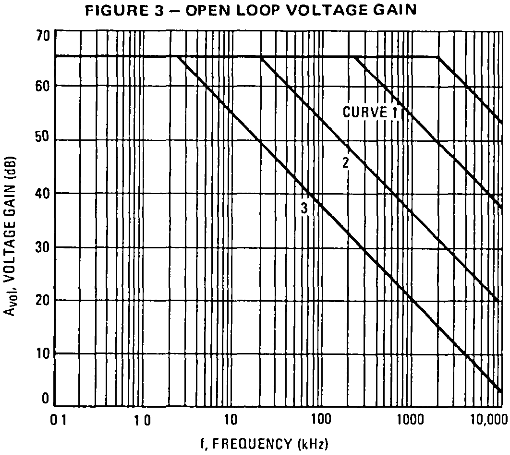
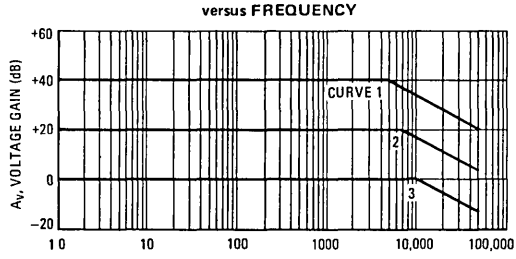


FIGURE 4 – CLOSED LOOP VOLTAGE GAIN versus FREQUENCY



TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = −6 0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

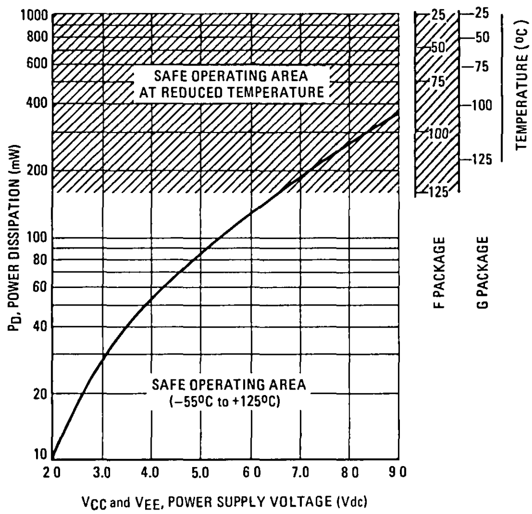


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

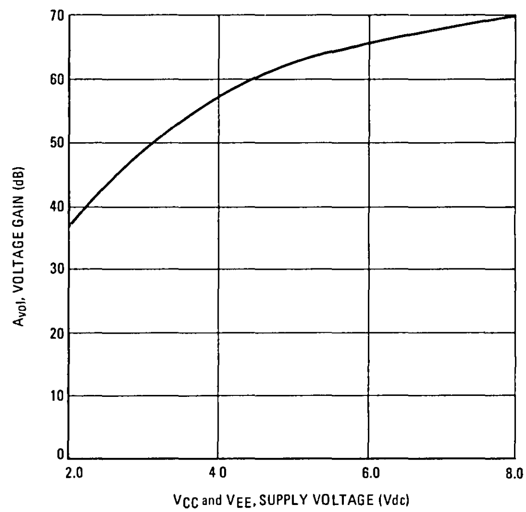


FIGURE 7 – SINGLE ENDED OUTPUT VOLTAGE versus LOAD RESISTANCE

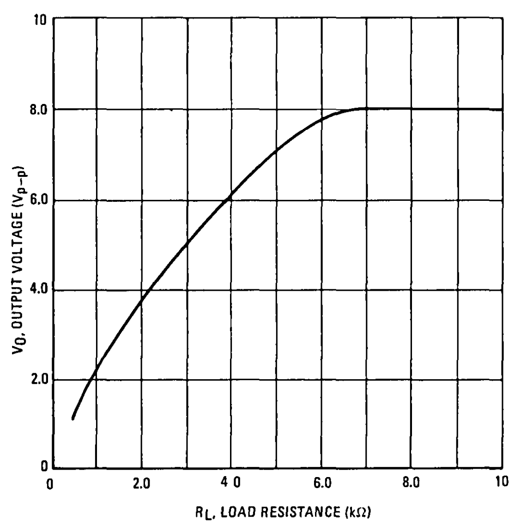
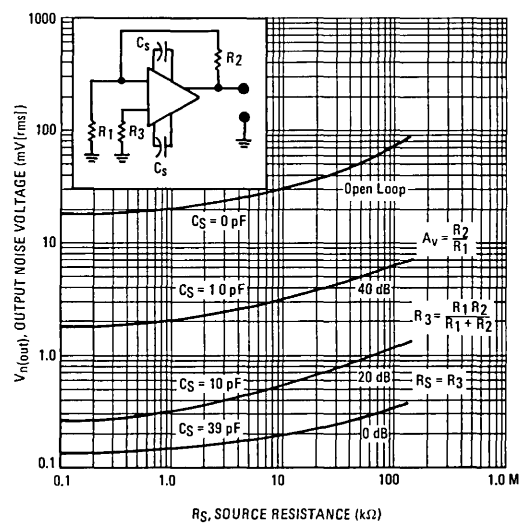


FIGURE 8 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1430F,1431F	0°C to +70°C	Ceramic Flat
MC1430G,1431G	0°C to +70°C	Metal Can
MC1430P,1431P	0°C to +70°C	Plastic DIP
MC1530F,1531F	−55°C to +125°C	Ceramic Flat
MC1530G,1531G	−55°C to +125°C	Metal Can

MC1430, MC1431
MC1530, MC1531

OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MC1531 (MC1431) is provided with Darlington inputs to increase input impedance; otherwise the MC1531 (MC1431) circuit is identical with the MC1530 (MC1430) circuit.

- High Open Loop Voltage Gain – 4500 min (MC1530)
  – 2500 min (MC1531)
- High Input Impedance – 10 Kilohms min (MC1530)
  – 1.0 Megohm min (MC1531)
- Low Output Impedance – 50 Ohms max
- High Slew Rate – 6.0 V/μs typ @ A_{VS} = 10
- High Open Loop Bandwidth – 2.0 MHz typ (MC1530)
  0.4 MHz typ (MC1531)

MAXIMUM RATINGS (T_A = 25°C unless otherwsie noted)

Rating	Symbol	Value	Unit
Power Supply Voltage MC1530, MC1531	V_{CC}, V_{EE}	+9.0, −9.0	Vdc
MC1430, MC1431	V_{CC}, V_{EE}	+8.0, −8.0	
Differential Input Voltage Range	V_{IDR}	± 5.0	Volts
Load Current	I_L	10	mA
Power Dissipation (Package Limitation)	P_D		
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Dual In-Line Plastic Package MC1430, MC1431		400	mW
Derate above +25°C		3.3	mW/°C
Operating Ambient Temperature Range	T_A		°C
MC1530, MC1531		−55 to +125	
MC1430, MC1431		0 to +75	
Storage Temperature Range	T_{stg}		°C
Metal and Ceramic Package		−65 to +175	
Plastic Package MC1430, MC1431		−55 to +150	

CIRCUIT SCHEMATICS

FIGURE 1 – MC1530/MC1430 (STANDARD INPUT)

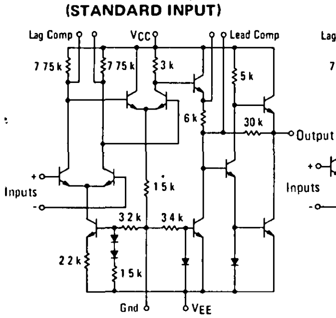
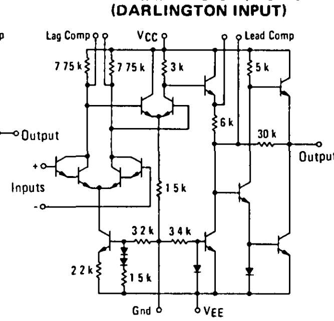
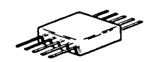


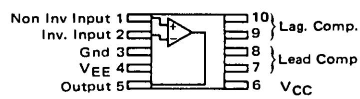
FIGURE 2 – MC1531/MC1431 (DARLINGTON INPUT)



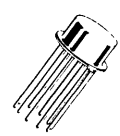
PIN CONNECTIONS

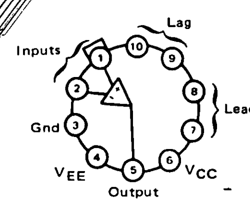
F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



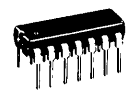


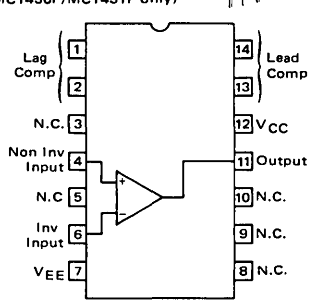
G SUFFIX
METAL PACKAGE
CASE 603 B





P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1430P/MC1431P only)



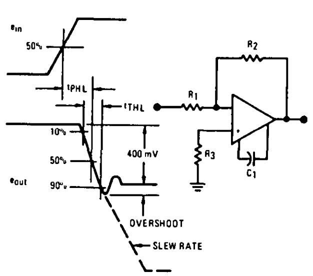


ELECTRICAL CHARACTERISTICS (V_{CC} = +6 0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1530 Min	MC1530 Typ	MC1530 Max	MC1430 Min	MC1430 Typ	MC1430 Max	Unit
Input Bias Current	I_{IB}	–	3 0	10	–	5 0	15	μAdc
Input Offset Current	I_{IO}	–	0 2	2 0	–	0 4	4 0	μAdc
Input Offset Voltage T_A = +25°C	V_{IO}	–	1 0	5 0	–	2 0	10	mVdc
T_A = T_{low} ①		–	–	6 0	–	–	11	
T_A = T_{high} ①		–	–	6 0	–	–	12	
Single-Ended Input Impedance (Open-Loop, f = 30 Hz)	z_{is}	10	20	–	5 0	15	–	k Ω
Common-Mode Input Voltage Swing	V_{ICR}	± 2 0	± 2 7	–	± 2 0	± 2 5	–	V_{pk}
Equivalent Input Noise Voltage (Open-Loop, R_s = 50 ohms, BW = 5 0 MHz)	e_N	–	10	–	–	10	–	μV(rms)
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	70	75	–	65	75	–	dB
Open-Loop Voltage Gain,	A_{vol}							V/V
T_A = +25°C		–	–	–	3000	5000	–	
T_A = T_{low} to T_{high}		4500	5000	12,500	–	–	–	
Bandwidth (Open-Loop, -3 0 dB, no roll-off capacitance)	BW	1 0	2.0	–	1 0	2 0	–	MHz
Output Impedance (f = 100 Hz)	z_O	–	25	50	–	25	50	ohms
Output Voltage Swing (R_L = 1 0 k ohms)	V_O	± 4 5	± 5 2	–	± 4 0	± 5 0	–	V_{pk}
Power Supply Sensitivity ($R_s \leqslant$ 10 k Ω)	PSRR	–	100	–	–	100	–	μV/V
Power Supply Current	I_{CC}, I_{EE}	–	9 2	12 5	–	9 2	12 5	mAdc
DC Quiescent Power Consumption (V_O = 0)	P_C	–	110	150	–	110	150	mW

ELECTRICAL CHARACTERISTICS (V_{CC} = +6 0 Vdc, V_{EE} = -6 0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1531 Min	MC1531 Typ	MC1531 Max	MC1431 Min	MC1431 Typ	MC1431 Max	Unit
Input Bias Current	I_{IB}	–	0 025	0 150	–	0 1	0 3	μAdc
Input Offset Current	I_{IO}	–	0 003	0 025	–	0 01	0 1	μAdc
Input Offset Voltage T_A = +25°C	V_{IO}	–	3 0	10	–	5 0	15	mVdc
T_A = T_{low} ①		–	–	18	–	–	–	
T_A = T_{high} ①		–	–	16 5	–	–	–	
Single-Ended Input Impedance (Open-Loop, f = 30 Hz)	z_{is}	1000	2000	–	300	600	–	k Ω
Common-Mode Input Voltage Swing	V_{ICR}	± 2 0	± 2 4	–	± 2 0	± 2 2	–	V_{pk}
Equivalent Input Noise Voltage (Open-Loop, R_s = 50 ohms, BW = 5.0 MHz)	e_N	–	20	–	–	20	–	μV(rms)
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	65	65	–	60	75	–	dB
Open-Loop Voltage Gain	A_{vol}							V/V
T_A = +25°C		–	–	–	1500	3500	–	
T_A = T_{low} to T_{high}		2500	3500	7000	–	–	–	
Bandwidth (Open-Loop, -3.0 dB, no roll-off capacitance)	BW	–	0 4	–	–	0 4	–	MHz
Output Impedance (f = 30 Hz)	z_O	–	25	50	–	25	50	ohms
Output Voltage Swing (R_L = 1 0 k ohms)	V_O	± 4 5	± 5.2	–	± 4 0	± 5 0	–	V_{pk}
Power Supply Sensitivity ($R_S \leqslant$ 10 k Ω)	PSRR	–	100	–	–	100	–	μV/V
Power Supply Current	I_{CC}, I_{EE}	–	9 2	12 5	–	9 2	12 5	mAdc
DC Quiescent Power Consumption (V_O = 0)	P_C	–	110	150	–	110	150	mW



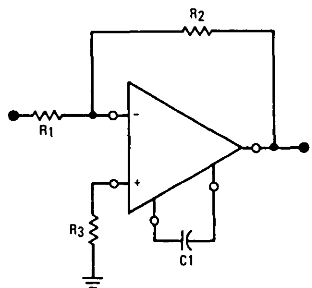
STEP RESPONSE, TYPICAL CHARACTERISTICS
(V_{CC} = +6 0 Vdc, V_{EE} = -6 0 Vdc, V_O = 400 mVdc, T_A = +25°C)

Step Response	Symbol	MC1530 MC1430	MC1531 MC1431	
Gain = 100, 0% overshoot, R_1 = 1 0 k ohm, R_2 = 100 k ohms, R_3 = 1 0 k ohm, C_1 = 750 pF	t_{THL}	0 13	0 36	μs
	t_{PHL}	0 11	0 21	μs
	SR	33	16	V/μs
Gain = 10, 10% overshoot, R_1 = 10 k ohms, R_2 = 100 k ohms, R_3 = 10 k ohms, C_1 = 6800 pF	t_{THL}	0 34	0 30	μs
	t_{PHL}	0 25	0 28	μs
	SR	6 0	5 5	V/μs
Gain = 1 0, 5 0% overshoot, R_1 = 10 k ohms, R_2 = 10 k ohms, R_3 = 5 0 k ohms, C_1 = 33,000 pF	t_{THL}	0 28	0 37	μs
	t_{PHL}	0 16	0 17	μs
	SR	1 7	1 4	V/μs

① T_{low} 0°C for MC1430, -55°C for MC1530; T_{high} +75°C for MC1430, +125°C for MC1530
T_{low} 0°C for MC1431, -55°C for MC1531; T_{high} +75°C for MC1431, +125°C MC1531

3

FIGURE 3 – TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C)

FIG NO	CURVE NO.	VOLTAGE GAIN	DEVICE NO	TEST CONDITIONS			
				R_1 (kΩ)	R_2 (kΩ)	R_3 (Ω)	C_1 (pF)
5	1,2	100	MC1530/MC1430, MC1531/MC1431	1.0	100	1.0 k	750
	3	10	MC1530/MC1430, MC1531/MC1431	10	100	10 k	6800
	4	1	MC1530/MC1430, MC1531/MC1431	10	10	5.0 k	33,000
6	1	100	MC1530/MC1430	1.0	100	1.0 k	750
	2	10	MC1530/MC1430	10	100	10 k	6800
	3	10	MC1530/MC1430	1.0	10	1.0 k	6800
	4	1	MC1530/MC1430	10	10	5.0 k	33,000
	5	1	MC1530/MC1430	1.0	1.0	500	33,000
7	1	100	MC1531/MC1431	1.0	100	1.0 k	750
	2	10	MC1531/MC1431	10	100	10 k	6800
	3	1	MC1531/MC1431	10	10	5.0 k	33,000
8	1	A_{VOL}	MC1530/MC1430	0	-	0	0
	2	A_{VOL}	MC1530/MC1430	0	-	0	750
	3	A_{VOL}	MC1530/MC1430	0	-	0	6800
	4	A_{VOL}	MC1530/MC1430	0	-	0	33,000
9	1	A_{VOL}	MC1531/MC1431	0	-	0	0
	2	A_{VOL}	MC1531/MC1431	0	-	0	750
	3	A_{VOL}	MC1531/MC1431	0	-	0	6800
	4	A_{VOL}	MC1531/MC1431	0	-	0	33,000

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

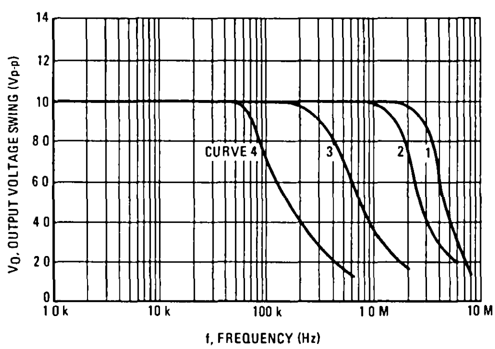


FIGURE 5 – MC1530/MC1430 VOLTAGE GAIN versus FREQUENCY

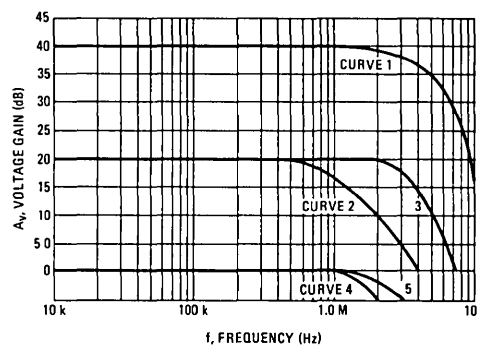


FIGURE 6 – MC1531/MC1431 VOLTAGE GAIN versus FREQUENCY

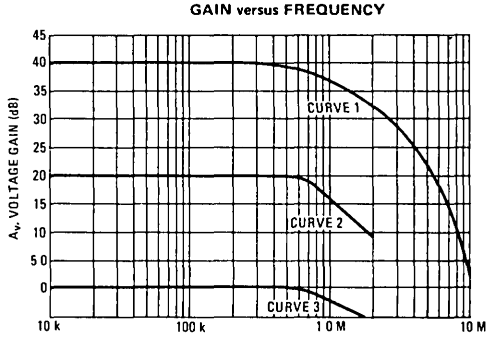


FIGURE 7 – MC1530/MC1430 OPEN LOOP VOLTAGE GAIN versus FREQUENCY

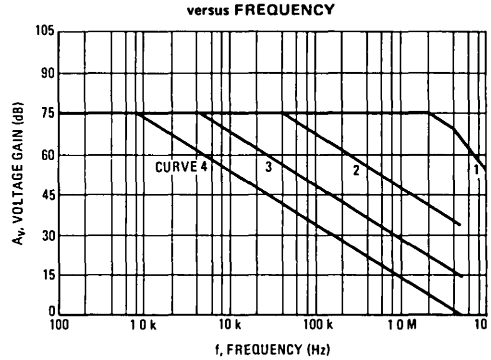


FIGURE 8 — MC1531/MC1431 OPEN LOOP VOLTAGE GAIN versus FREQUENCY

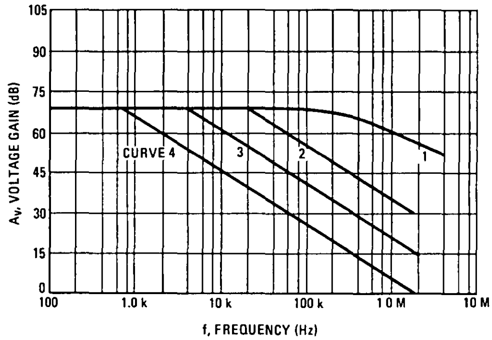


FIGURE 11 — COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

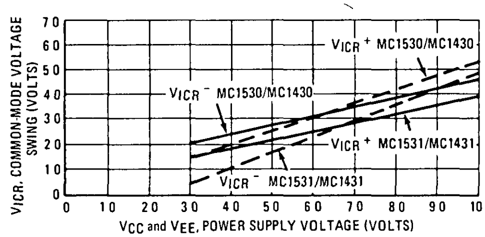


FIGURE 9 — VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

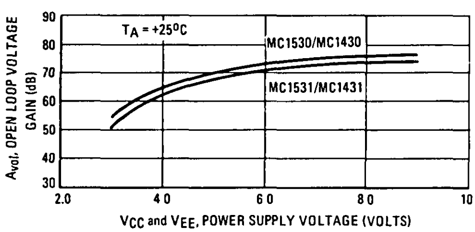


FIGURE 12 — POWER CONSUMPTION versus POWER SUPPLY VOLTAGE

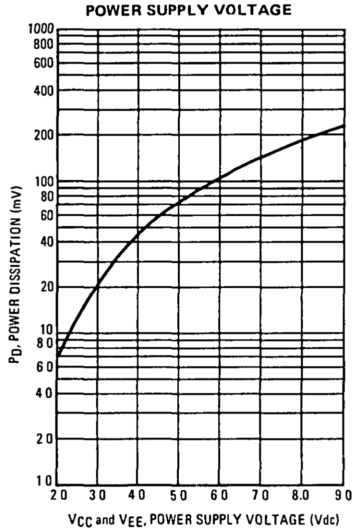
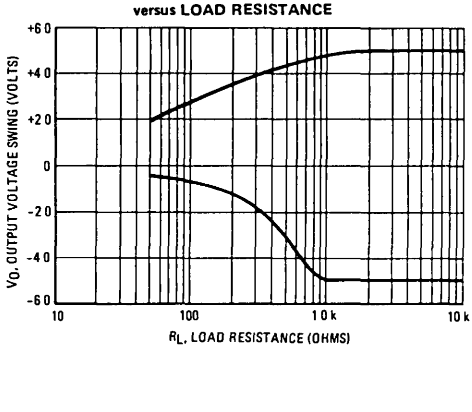


FIGURE 10 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1433F	0°C to +70°C	Ceramic Flat
MC1433G	0°C to +70°C	Metal Can
MC1433L	0°C to +70°C	Ceramic DIP
MC1433P	0°C to +70°C	Plastic DIP
MC1533F	−55°C to +125°C	Ceramic Flat
MC1533G	−55°C to +125°C	Metal Can
MC1533L	−55°C to +125°C	Ceramic DIP

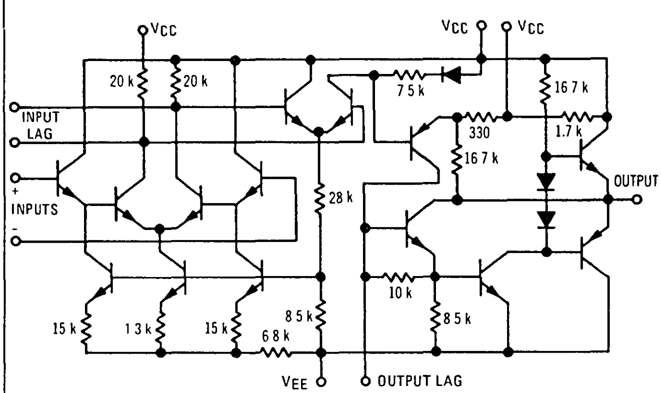
MC1433
MC1533

3

OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

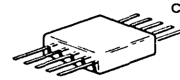
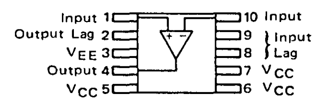
- High-Performance Open Loop Gain Characteristics
  A_{vol} = 60,000 typical
- Low Temperature Drift – ±5 μV/°C
- Large Output Voltage Swing –
  ±13 V typical @ ±15 V Supply
- Low Output Impedance – z_o = 100 ohms typical



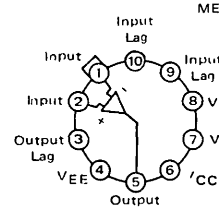
OPERATIONAL AMPLIFIER

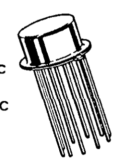
SILICON MONOLITHIC INTEGRATED CIRCUIT

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

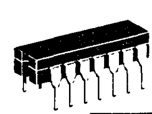
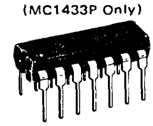
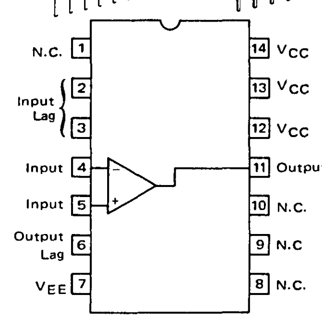
G SUFFIX
METAL PACKAGE
CASE 603B





L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1433P Only)

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1533 Min	MC1533 Typ	MC1533 Max	MC1433 Min	MC1433 Typ	MC1433 Max	Unit
Open Loop Voltage Gain	A_{VOL}							–
(T_A = +25°C)		40,000	60,000	–	30,000	60,000	–	
(T_A = T_{low} ① to T_{high} ①)		35,000	50,000	–	20,000	50,000	–	
Output Impedance (f = 20 Hz)	z_o	–	100	150	–	100	150	Ω
Input Impedance (f = 20 Hz)	z_i	500	1000	–	300	600	–	kΩ
Output Voltage Range	V_o							V_{peak}
(R_L = 10 kΩ)		±12	±13	–	±12	±13	–	
(R_L = 2 kΩ)		±11	±12	–	±10	±12	–	
Input Common Mode Voltage Range	V_{ICR}	+9.0 -8.0	+10 -9.0	– –	+8.0 -8.0	+9.0 -9.0	– –	V_{peak}
Common Mode Rejection Ratio	CMRR	90	100	–	80	100	–	dB
Input Bias Current	I_{IB}							µA
(T_A = +25°C)		–	0.5	1.0	–	0.5	2.0	
(T_A = T_{low})		–	–	3.0	–	–	4.0	
Input Offset Current	I_{IO}							µA
(T_A = +25°C)		–	0.03	0.15	–	0.1	0.50	
(T_A = T_{low})		–	–	0.5	–	–	0.75	
(T_A = T_{high})		–	–	0.2	–	–	0.75	
Input Offset Voltage ②	V_{IO}							mV
(T_A = +25°C)		–	1.0	5.0	–	1.0	7.5	
(T_A = T_{low}, T_{high})		–	–	6.0	–	–	10	
Step Response (C_2 = 10 pF)								
Gain = 100, 10% overshoot, R_1 = 10 kΩ, R_2 = 1.0 MΩ, R_3 = 100 Ω, C_1 = 0.01 µF	t_{TLH}	–	0.25	–	–	0.25	–	µs
	t_{pd}	–	0.1	–	–	0.1	–	µs
	SR	–	6.2	–	–	6.2	–	V/µs
Gain = 10, no overshoot, R_1 = 10 kΩ, R_2 = 100 kΩ, R_3 = 10 Ω, C_1 = 0.1 µF	t_{TLH}	–	0.3	–	–	0.3	–	µs
	t_{pd}	–	0.1	–	–	0.1	–	µs
	SR	–	2.9	–	–	2.9	–	V/µs
Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 10 Ω, C_1 = 1.0 µF	t_{TLH}	–	0.2	–	–	0.2	–	µs
	t_{pd}	–	0.1	–	–	0.1	–	µs
	SR	–	2.0	–	–	2.0	–	V/µs
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							µV/°C
(T_A = T_{low} to +25°C)		–	8.0	–	–	10	–	
(T_A = +25°C to T_{high})		–	5.0	–	–	8.0	–	
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
(T_A = T_{low} to T_{high})		–	0.1	–	–	0.1	–	
(T_A = +25°C to T_{high})		–	0.05	–	–	0.05	–	
DC Power Consumption (Power Supply = ±15 V, V_o = 0)	P_C	–	125	170	–	125	240	mW
Positive Supply Sensitivity (V_{EE} constant)	PSRR+	–	50	150	–	50	200	µV/V
Negative Supply Sensitivity (V_{CC} constant)	PSSR-	–	50	150	–	50	200	µV/V

① T_{high} = +75°C for MC1433, +125°C for MC1533; T_{low} = 0 for MC1433, -55°C for MC1533

② Input offset voltage (V_{IO}) may be adjusted to zero.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage MC1533,MC1433 MC1533,MC1433	V_{CC} V_{EE}	+20,+18 -20,-18	Vdc Vdc
Differential Input Voltage Range	V_{IDR}	±10	Volts
Common Mode Input Voltage Range	V_{ICR}	$\pm V_{CC}$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	0.1	s
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Flat Package Derate above T_A = +25°C Dual In-Line Ceramic Package Derate above T_A = +25°C Dual In-Line Plastic Package Derate above T_A = +25°C	P_D	 680 4 6 500 3 3 625 5 0 400 3 3	 mW mW/°C mW mW/°C mW mW/°C mW mW/°C
Operating Ambient Temperature Range MC1533 MC1433	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TYPICAL CHARACTERISTICS

FIGURE 2 — TEST CIRCUIT

V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C

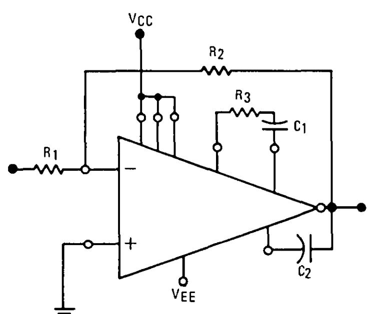


Fig. No.	Curve No.	Test Conditions				
		R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (μF)	C_2 (pF)
3	1	10 k	10 k	10	1 0	10
	2	10 k	100 k	10	0 1	10
	3	10 k	1.0 M	100	0.01	10
	3	1 0 k	1 0 M	390	0 002	10
4	1	10 k	10 k	10	1.0	10
	2	10 k	100 k	10	0.1	10
	3	10 k	1.0 M	100	0 01	10
	4	1 0 k	1.0 M	390	0 002	10
5	1	0	∞	10	1.0	10
	2	0	∞	10	0 1	10
	3	0	∞	100	0 01	10
	4	0	∞	390	0 002	10

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} -15 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 – LARGE-SIGNAL RANGE versus FREQUENCY

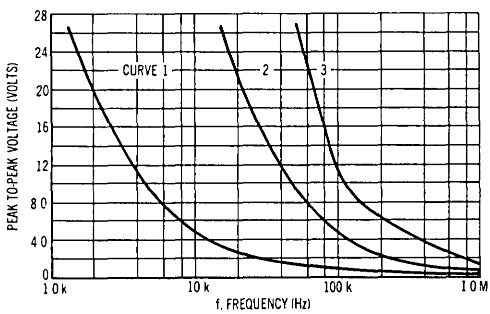


FIGURE 4 – VOLTAGE GAIN versus FREQUENCY

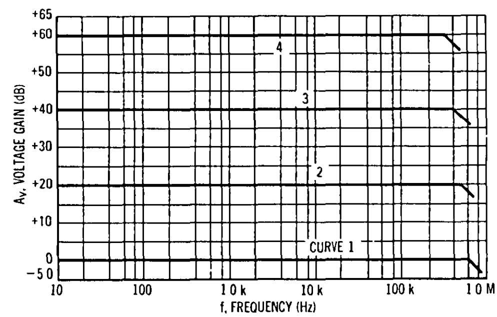


FIGURE 5 – OFFSET ADJUST CIRCUIT

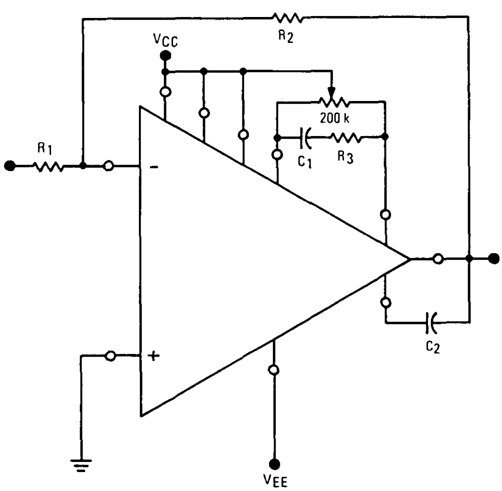
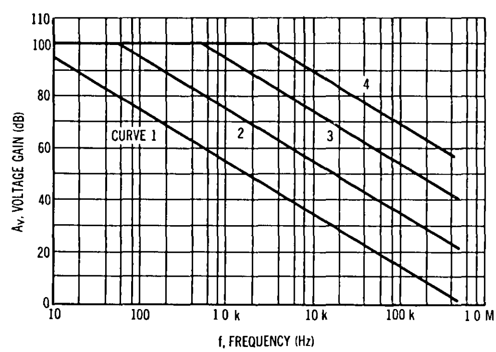


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY (HIGH GAIN CONFIGURATION)



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE

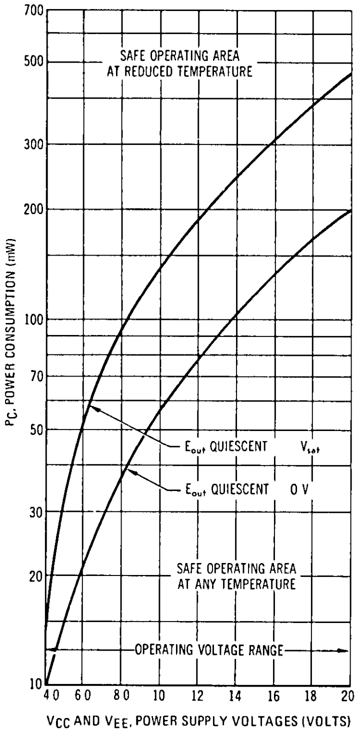


FIGURE 8 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

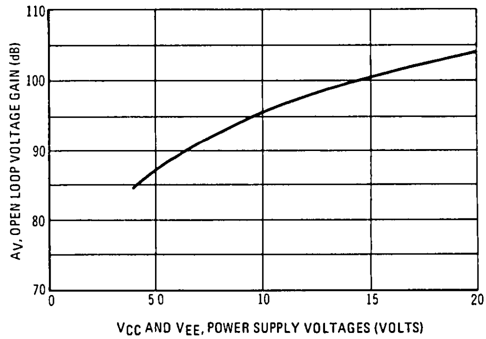


FIGURE 9 – COMMON MODE RANGE versus POWER SUPPLY VOLTAGE

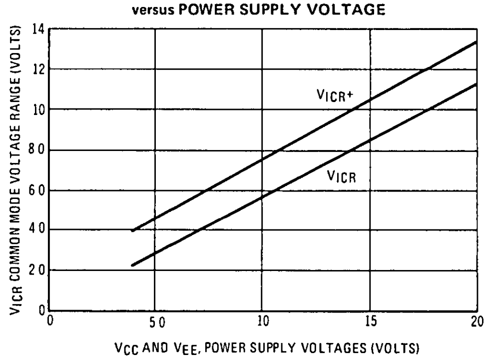
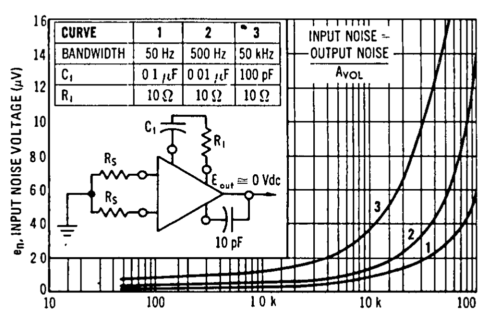


FIGURE 10 – INPUT NOISE VOLTAGE versus SOURCE RESISTANCE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1435F	0°C to +70°C	Ceramic Flat
MC1435G	0°C to +70°C	Metal Can
MC1435L	0°C to +70°C	Ceramic DIP
MC1435P	0°C to +70°C	Plastic DIP
MC1535F	−55°C to +125°C	Ceramic Flat
MC1535G	−55°C to +125°C	Metal Can
MC1535L	−55°C to +125°C	Ceramic DIP

MC1435
MC1535

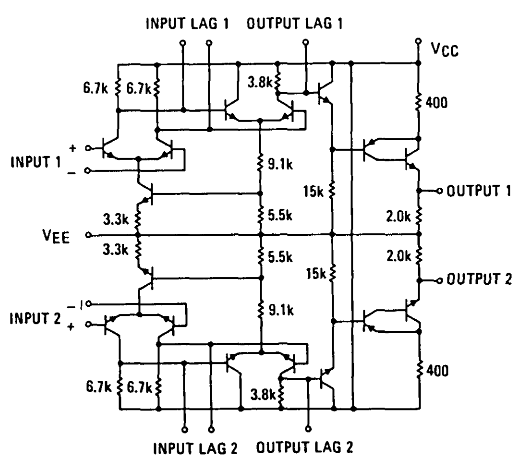
DUAL OPERATIONAL AMPLIFIERS

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

- High Open Loop Gain Characteristics – $A_{vol} = 7{,}000$
- Low Temperature Drift – ±10 μV/°C
- Low Input Offset Voltage – 1.0 mV
- Low Input Noise Voltage – 0.5 μV

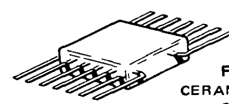
CIRCUIT SCHEMATIC



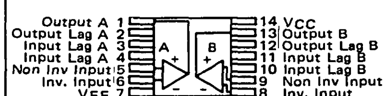
DUAL
OPERATIONAL AMPLIFIERS

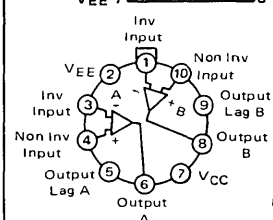
SILICON MONOLITHIC
INTEGRATED CIRCUIT

3

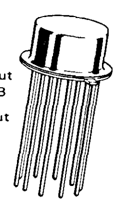


F SUFFIX
CERAMIC PACKAGE
CASE 607

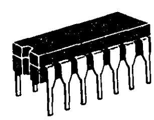




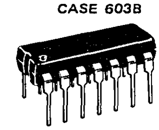
(TOP VIEW)



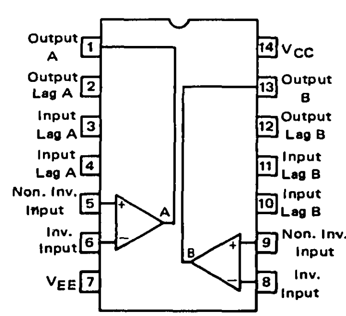
G SUFFIX
METAL PACKAGE
CASE 603B



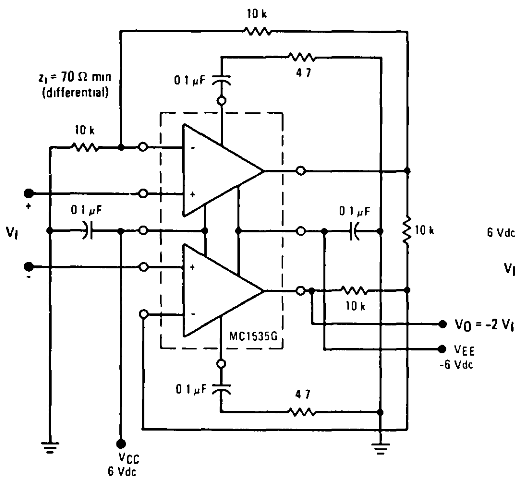
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



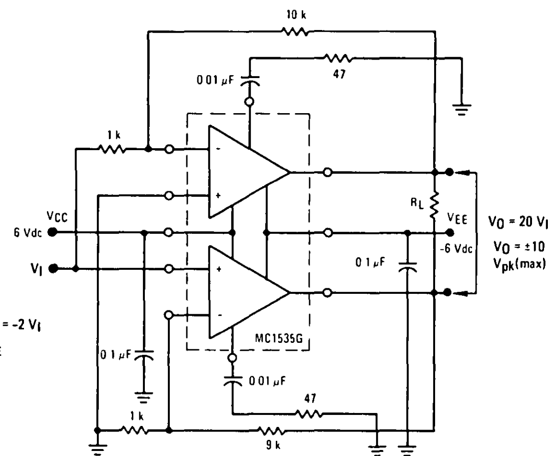
P SUFFIX
PLASTIC
PACKAGE
CASE 646



HIGH z_i, DIFFERENTIAL TO SINGLE-ENDED AMPLIFIER



LARGE OUTPUT SWING CONFIGURATION (FLOATING LOAD)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC1535	MC1435	Unit
Power Supply Voltage	V_{CC} V_{EE}	+10 -10	+9.0 -9.0	Vdc
Input Differential Voltage Range	V_{IDR}	±5.0	±5.0	Volts
Common-Mode Input Voltage Range	V_{ICR}	+5.0, -4.0	+5.0 -4.0	Volts
Load Current	I_L	20	20	mA
Output Short-Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation)	P_D			
Flat Ceramic Package		500		mW
Derate above T_A = +25°C		3.3		mW/°C
Metal Package		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Ceramic Dual In-Line Package		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Each Amplifier) (V_{CC} = +6.0 Vdc, V_{EE} = −6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristics	Symbol	MC1535			MC1435			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current $I_{IB} = \frac{I_1 + I_2}{2}$, T_A = +25°C T_A = T_{low} to T_{high} ①	I_{IB}	 – –	 1.2 –	 3 0 6.0	 – –	 1.2 –	 5.0 10	µAdc
Input Offset Current T_A = +25°C T_A = +25°C to T_{high} T_A = T_{low} to +25°C	I_{IO}	 – – –	 50 – –	 300 300 900	 – – –	 50 – –	 500 1500 1500	nAdc
Input Offset Voltage T_A = +25°C T_A = T_{low} to T_{high}	V_{IO}	 – –	 1.0 –	 3.0 5.0	 – –	 1.0 –	 5.0 7.5	mVdc
Differential Input Impedance (Open-Loop, f = 20 Hz) Parallel Input Resistance Parallel Input Capacitance	 r_i C_i	 10 –	 45 6.0	 – –	 10 –	 45 –	 – –	 k ohms pF
Common-Mode Input Impedance (f = 20 Hz)	z_i	–	250	–	–	250	–	Megohms
Common-Mode Input Voltage Swing See Figure 7.	V_{ICR}	+3 0 -2.0	+3.9 -2 7	– –	+3 0 -2 0	+3.9 -2.7	– –	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	e_n	–	45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	-70	-90	–	-70	-90	–	dB
Open Loop Voltage Gain (T_A = T_{low} to T_{high})	A_{vol}	4,000	7,000	12,000	3,500	7,000	–	V/V
Power Bandwidth (See Figure 2, Curve 3A.) (A_V = 1, R_L = 2.0 kohms, THD ≤ 5%, V_O = 20 Vp-p)	BW_p	–	40	–	–	40	–	kHz
Unity Gain Crossover Frequency (open-loop)	f_c	–	2.0	–	–	2.0	–	MHz
Phase Margin (open-loop, unity gain)	ϕm	–	75	–	–	75	–	degrees
Gain Margin	A_M	–	18	–	–	18	–	dB
Step Response Gain = 100, 30% overshoot, R1 = 4.7 kΩ, R2 = 470 kΩ, R3 = 150 Ω, C1 = 1,000 pF Gain = 10, 10% overshoot, R1 = 47 kΩ, R2 = 470 kΩ, R3 = 47 Ω, C1 = 0.01 µF Gain = 1, 5% overshoot, R1 = 47 kΩ, R2 = 47 kΩ, R3 = 4.7 Ω, C1 = 0.1 µF	 t_{PHL} t_p SR t_{PHL} t_p SR t_{PHL} t_p SR	 – – – – – – – – –	 0 3 0.1 0 167 1.9 0 3 0.111 27 0.25 0 013	 – – – – – – – – –	 – – – – – – – – –	 0.3 0.1 0.167 1.9 0.3 0.111 27 0.25 0 013	 – – – – – – – – –	 µs µs V/µs µs µs V/µs µs µs V/µs
Output Impedance (f = 20 Hz)	z_o	–	1.7	–	–	1.7	–	k ohms
Short-Circuit Output Current	I_{OS}	–	±17	–	–	±17	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±2.5	±2.8	–	±2.3	±2.7	–	V_{pk}
Power Supply Sensitivity V_{EE} = constant, $R_s \leq$ 10 k ohms V_{CC} = constant, $R_s \leq$ 10 k ohms	 PSS+ PSS-	 – –	 50 100	 – –	 – –	 50 100	 – –	µV/V
Power Supply Current (Total)	I_{CC} I_{EE}	– –	8 3 8.3	12.5 12.5	– –	8.3 8 3	15 15	mAdc
DC Quiescent Power Consumption (Total) (V_O = 0)	P_C	–	100	150	–	100	180	mW

MATCHING CHARACTERISTICS

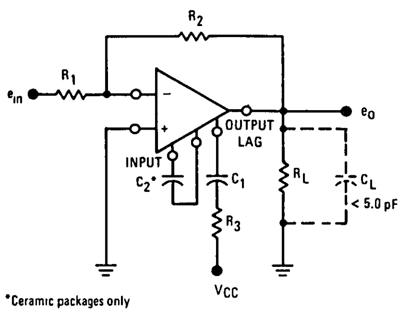
Characteristics	Symbol	MC1535 Min	MC1535 Typ	MC1535 Max	MC1435 Min	MC1435 Typ	MC1435 Max	Unit
Open Loop Voltage Gain	$A_{vol1} - A_{vol2}$	–	±1.0	–	–	±1.0	–	dB
Input Bias Current	$I_{IB1} - I_{IB2}$	–	±0.15	–	–	±0.15	–	µA
Input Offset Current	$I_{IO1} - I_{IO2}$	–	±0.02	–	–	±0.02	–	µA
Average Temperature Coefficient	$TCI_{IO1} - TCI_{IO2}$	–	±0.1	–	–	±0.1	–	nA/°C
Input Offset Voltage	$V_{IO1} - V_{IO2}$	–	±0.1	–	–	±0.1	–	mV
Average Temperature Coefficient	$TCV_{IO1} - TCV_{IO2}$	–	±0 5	–	–	±0.5	–	µV/°C
Channel Separation (See Fig. 10) (f = 10 kHz)	$\frac{e_{o1}}{e_{o2}}$	–	-60	–	–	-60	–	dB

① T_{low}: 0°C for MC1435
−55°C for MC1535
T_{high}: +75°C for MC1435
+125°C for MC1535

TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = −6.0 Vdc, T_A = +25°C.)

FIGURE 1 – TEST CIRCUIT



*Ceramic packages only

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS $R_1(\Omega)$	$R_2(\Omega)$	C_1(pF)	$R_3(\Omega)$	C_2(pF)	OUTPUT NOISE mV(RMS)
2	3	1	47 k	47 k	100,000	4 7	0	0.12
	3A	or 1	47 k	47 k	0	∞	50,000	0 46
3	1	100	4 7 k	470 k	1,000	150	0	1 7
		or 100	4 7 k	470 k	0	∞	510	2 1
	2	10	47 k	470 k	10,000	47	0	1 0
		or 10	47 k	470 k	0	∞	5,000	2.1
	3	1	47 k	47 k	100,000	4 7	0	0 12
		or 1	47 k	47 k	0	∞	50,000	0 46
4	1	or A_{vol}	100	∞	1,000	150	0	8 1
		A_{vol}	100	∞	0	∞	510	8 1
	2	or A_{vol}	100	∞	10,000	47	0	5 5
		A_{vol}	100	∞	0	∞	5,000	5 5
	3	A_{vol}	100	∞	100,000	4 7	0	4 4
		or A_{vol}	100	∞	0	∞	50,000	4 4

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

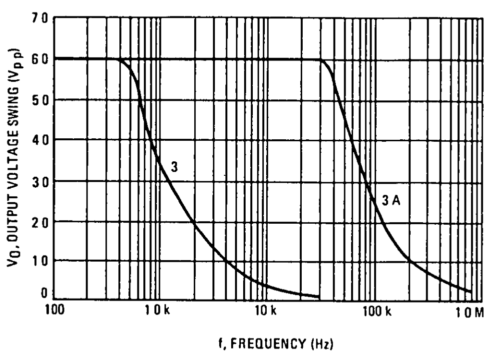


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

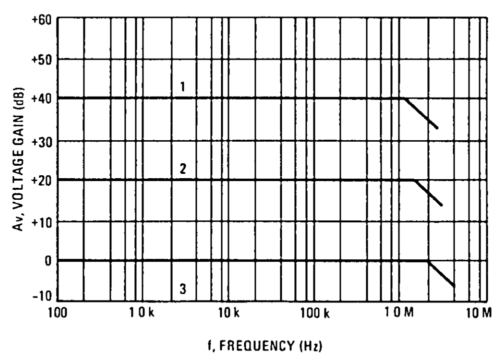


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

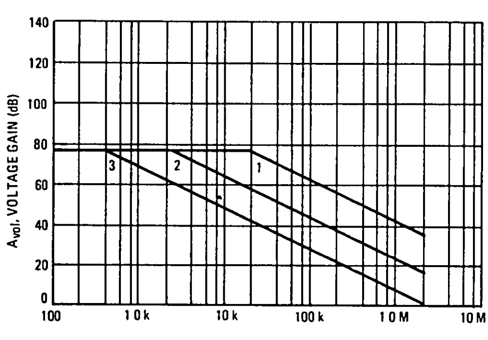
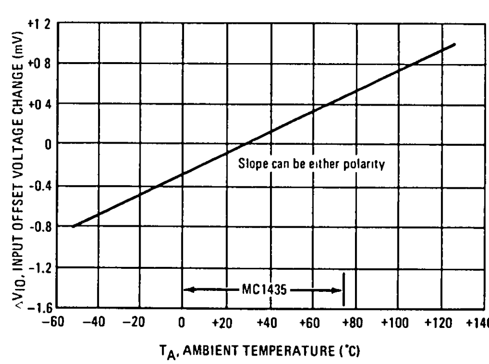


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

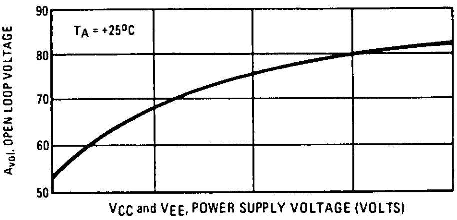


FIGURE 7 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

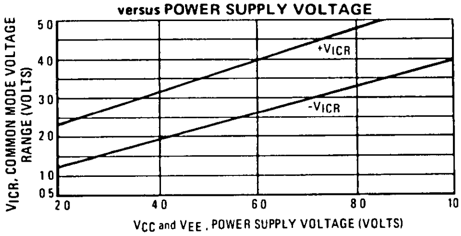


FIGURE 8 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE

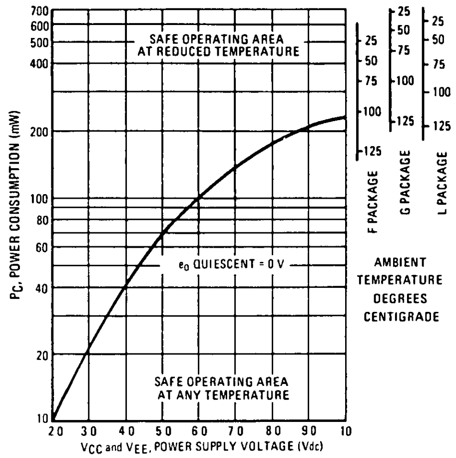
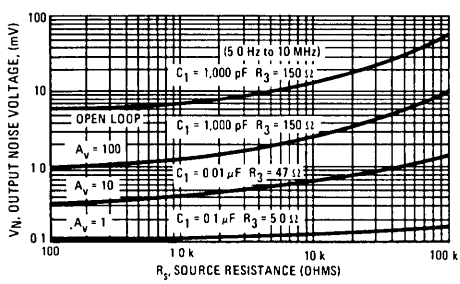


FIGURE 9 – OUTPUT WIDEBAND NOISE VOLTAGE versus SOURCE RESISTANCE



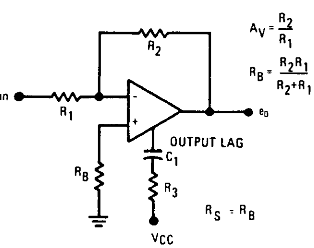
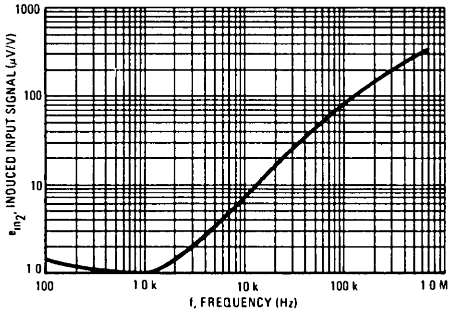
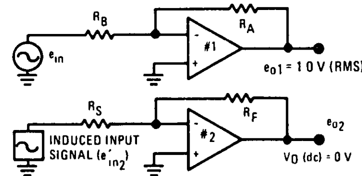


FIGURE 10 – INDUCED INPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced input signal (μV of induced input signal in amplifier = 2 per volt of output signal at amplifier = 1)

$e_{o2} = e'_{in2}\left(\frac{R_F}{R_S}\right)$, where e_{o2} is the component of e_{o2} due only to lack of perfect separation between the two amplifiers

ORDERING INFORMATION

Device	Temperature Range	Package
MC1436G	0°C to +70°C	Metal Can
MC1436U	0°C to +70°C	Ceramic DIP
MC1436CG	0°C to +70°C	Metal Can
MC1436CU	0°C to +70°C	Ceramic DIP
MC1536G	−55°C to +125°C	Metal Can
MC1536U	−55°C to +125°C	Ceramic DIP

MC1436
MC1436C
MC1536

3

HIGH VOLTAGE, INTERNALLY COMPENSATED OPERATIONAL AMPLIFIER

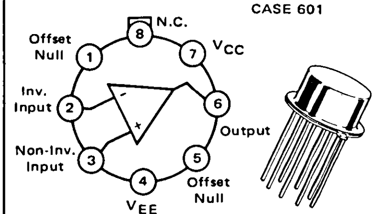
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage – ±40 Vdc (MC1536)
- Output Voltage Swing –
  ±30 $V_{pk(min)}$ (V_{CC} = +36 V, V_{EE} = -36 V) (MC1536)
  ±22 $V_{pk(min)}$ (V_{CC} = +28 V, V_{EE} = -28 V)
- Input Bias Current – 20 nA max (MC1536)
- Input Offset Current – 3.0 nA max (MC1536)
- Fast Slew Rate – 2.0 V/μs typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- A_{VOL} – 500,000 typ
- Characteristics Independent of Power Supply Voltages – (±5.0 Vdc to ±36 Vdc)

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

METAL PACKAGE
CASE 601



U SUFFIX
CERAMIC PACKAGE
CASE 693

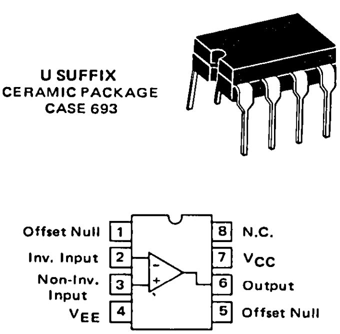


FIGURE 1 – DIFFERENTIAL AMPLIFIER WITH ± 20 V COMMON-MODE INPUT VOLTAGE RANGE

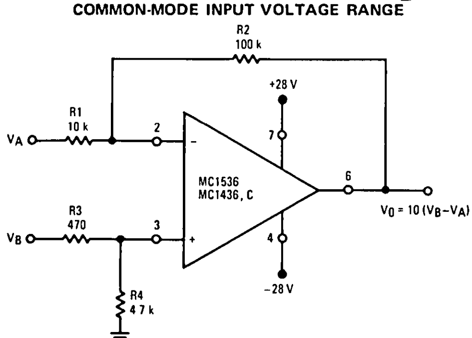


FIGURE 2 – TYPICAL NON-INVERTING X10 VOLTAGE AMPLIFIER

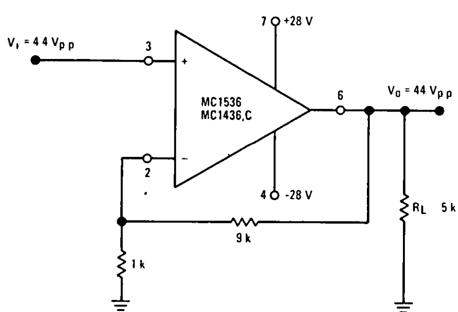
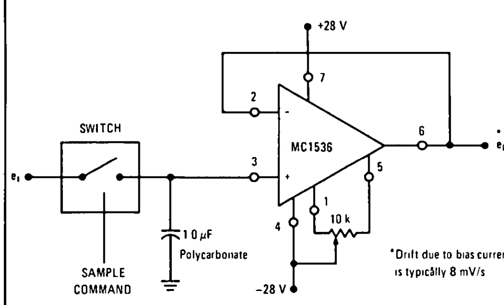


FIGURE 3 – LOW-DRIFT SAMPLE AND HOLD



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1536	MC1436	MC1436C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+40 -40	+34 -34	+30 -30	Vdc
Input Differential Voltage Range	V_{IDR}	± (V_{CC} + V_{EE}-3)			Volts
Input Common-Mode Voltage Range	V_{ICR}	+V_{CC}, - (V_{EE}-3)			Volts
Output Short Circuit Duration (V_{CC} = V_{EE} = 28 Vdc, V_o = 0)	t_S	5 0			s
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4 6			mW mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70		°C
Storage Temperature Range	T_{stg}	-65 to +150			°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +28 Vdc, V_{EE} = - 28 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1536 Min	MC1536 Typ	MC1536 Max	MC1436 Min	MC1436 Typ	MC1436 Max	MC1436C Min	MC1436C Typ	MC1436C Max	Unit
Input Bias Current T_A = +25°C T_A = T_{low} to T_{high} (See Note 1)	I_{IB}	 – –	 8 0 –	 20 35	 – –	 15 –	 40 55	 – –	 25 –	 90 –	nAdc
Input Offset Current T_A = +25°C T_A = +25°C to T_{high} T_A = T_{low} to +25°C	I_{IO}	 – – –	 1 0 – –	 3 0 4 5 7 0	 – – –	 5 0 – –	 10 14 14	 – – –	 10 – –	 25 – –	nAdc
Input Offset Voltage T_A = +25°C T_A = T_{low} to T_{high}	V_{IO}	 – –	 2 0 –	 5 0 7 0	 – –	 5 0 –	 10 14	 – –	 5 0 –	 12 –	mVdc
Differential Input Impedance (Open-Loop, f ≤ 5 0 Hz) Parallel Input Resistance Parallel Input Capacitance	 r_P C_P	 – –	 10 2 0	 – –	 – –	 10 2 0	 – –	 – –	 10 2 0	 – –	 Meg ohms pF
Common-Mode Input Impedance (f ≤ 5 0 Hz)	z_{ic}	–	250	–	–	250		–	250	–	Meg ohms
Input Common-Mode Voltage Range	V_{ICR}	±24	±25	–	±22	±25	–	±18	±20	–	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1 0 kHz, BW = 1 0 Hz)	e_n	 –	 50	 –	 –	 50	 –	 –	 50	 –	nV/(Hz)½
Common-Mode Rejection Ratio (dc)	CMRR	80	110	–	70	110	–	50	90	–	dB
Large Signal dc Open Loop Voltage Gain (V_o = ± 10 V, R_L = 100 k ohms) T_A = +25°C (V_o = ± 10 V, R_L = 100 k ohms) T_A = T_{low} to T_{high} (V_o = ±10 V, R_L = 10 k ohms, T_A = +25°C)	A_{VOL}	 100,000 50,000 –	 500,000 – 200,000	 – – –	 70,000 50,000 –	 500,000 – 200,000	 – – –	 50,000 – –	 500,000 – 200,000	 – – –	V/V
Power Bandwidth (Voltage Follower) (A_V = 1, R_L = 5 0 k ohms, THD ≤ 5%, V_o = 40 Vp-p)	BW_P	 –	 23	 –	 –	 23	 –	 –	 23	 –	kHz
Unity Gain Crossover Frequency (open-loop)	f_c	–	1 0	–	–	1 0	–	–	1 0	–	MHz
Phase Margin (open-loop, unity gain)	ϕm	–	50	-	–	50	–	–	50	–	degrees
Gain Margin	A_M	–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)	SR	–	2 0	–	–	2 0	–	–	2 0	–	V/µs
Output Impedance (f ≤ 5 0 Hz)	z_o	–	1 0	–	–	1 0	–	–	1 0	–	k ohms
Short-Circuit Output Current	I_{OS}	–	±17	–	–	±17	–	–	±19	–	mAdc
Output Voltage Range (R_L = 5 0 k ohms) V_{CC} = +28 Vdc, V_{EE} = -28 Vdc V_{CC} = +36 Vdc, V_{EE} = -36 Vdc	V_{OR}	 ±22 ±30	 ±23 ±32	 – -	 ±20 –	 ±22 –	 – –	 ±20 –	 ±22 –	 – –	V_{pk}
Power Supply Sensitivity (dc) V_{EE} = constant, R_s ≤ 10 k ohms V_{CC} = constant, R_s ≤ 10 k ohms	 PSS+ PSS-	 – –	 15 15	 100 100	 – –	 35 35	 200 200	 – –	 50 50	 – –	µV/V
Power Supply Current (See Note 2)	I_{CC} I_{EE}	– –	2 2 2 2	4 0 4 0	– –	2 6 2 6	5 0 5 0	– –	2 6 2 6	5 0 5 0	mAdc
DC Quiescent Power Consumption (V_o = 0)	P_C	 –	 124	 224	 –	 146	 280	 –	 146	 280	mW

Note 1 T_{low} 0°C for MC1436,C
-55°C for MC1536
T_{high} +70°C for MC1436,C
+125°C for MC1536

Note 2 V_{CC} = V_{EE} = 5 0 Vdc to 36 Vdc for MC1536
V_{CC} = V_{EE} = 5 0 Vdc to 30 Vdc for MC1436
V_{CC} = V_{EE} = 5 0 Vdc to 28 Vdc for MC1436C

FIGURE 4 — POWER BANDWIDTH

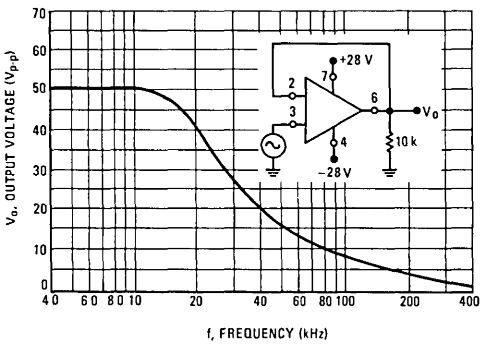


FIGURE 5 — PEAK OUTPUT VOLTAGE SWING versus POWER SUPPLY VOLTAGE

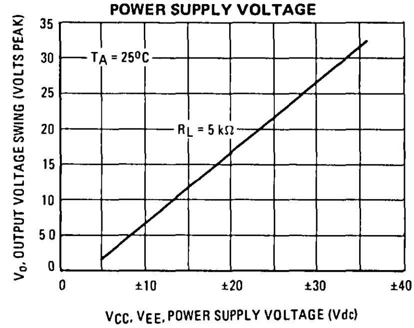


FIGURE 6 — OPEN-LOOP FREQUENCY RESPONSE

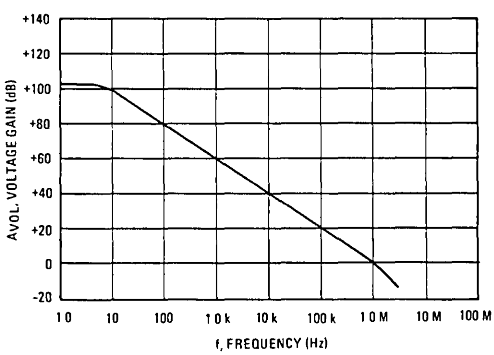


FIGURE 7 — OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

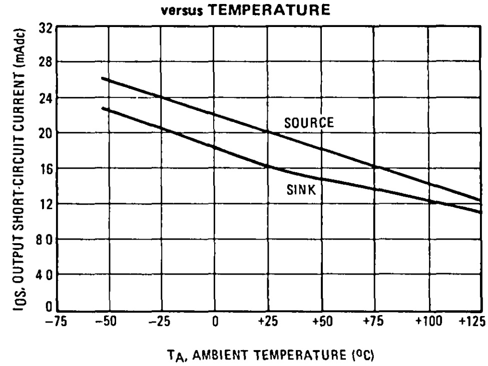


FIGURE 8 — INPUT BIAS CURRENT versus TEMPERATURE

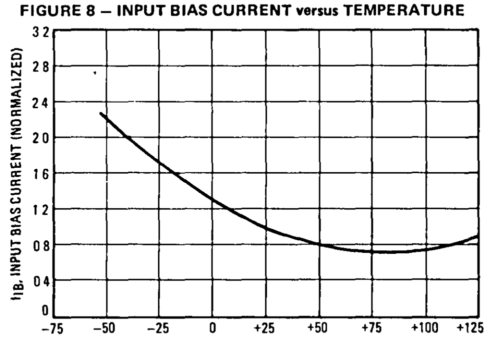
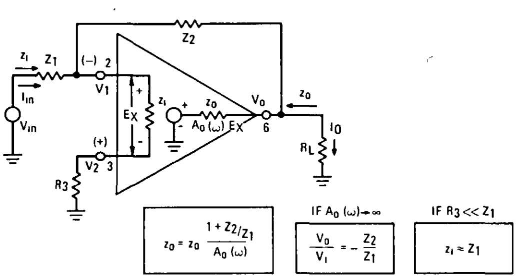


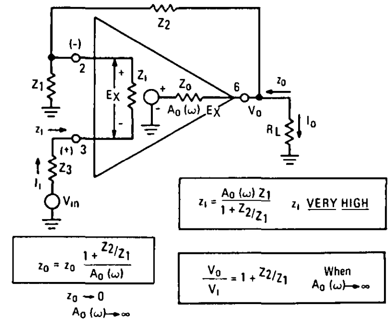
FIGURE 9 – INVERTING FEEDBACK MODEL



$$z_o = z_o \frac{1 + Z2/Z1}{A_o(\omega)}$$

$$\frac{V_o}{V_i} = -\frac{Z2}{Z1}$$

FIGURE 10 – NON-INVERTING FEEDBACK MODEL



$$z_i = \frac{A_o(\omega)\,Z1}{1 + Z2/Z1}$$

$$z_o = z_o \frac{1 + Z2/Z1}{A_o(\omega)}$$

$$\frac{V_o}{V_i} = 1 + Z2/Z1$$

FIGURE 11 – AUDIO AMPLIFIER

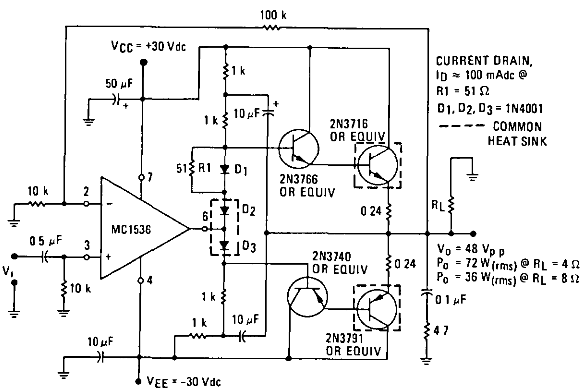
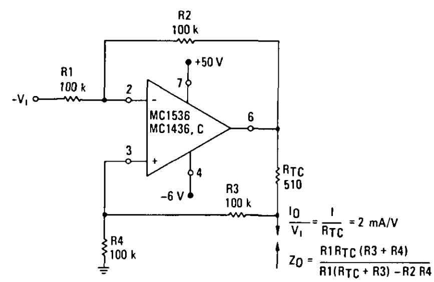


FIGURE 12 – VOLTAGE CONTROLLED CURRENT SOURCE or TRANSCONDUCTANCE AMPLIFIER WITH 0 TO 40 V COMPLIANCE



$$\frac{I_O}{V_i} = \frac{1}{R_{TC}} = 2\ \text{mA/V}$$

$$Z_O = \frac{R1\,R_{TC}\,(R3 + R4)}{R1(R_{TC} + R3) - R2\,R4}$$

FIGURE 13 – REPRESENTATIVE CIRCUIT SCHEMATIC

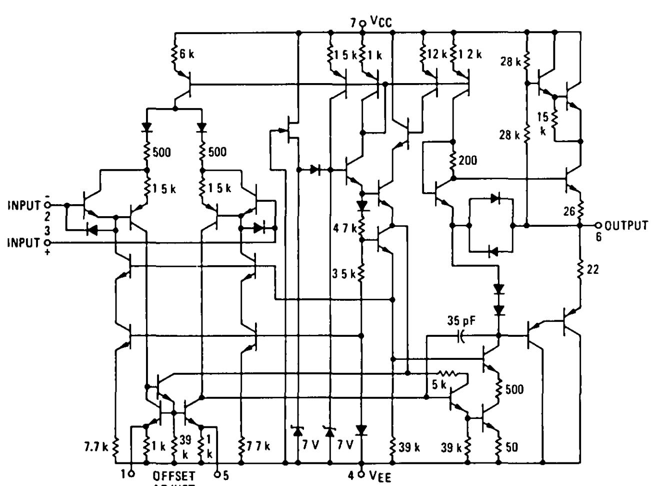
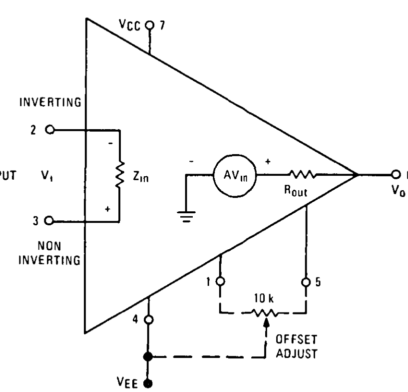


FIGURE 14 – EQUIVALENT CIRCUIT



3

ORDERING INFORMATION

Device	Temperature Range	Package
MC1437L	0°C to +70°C	Ceramic DIP
MC1437P	0°C to +70°C	Plastic DIP
MC1537L	−55°C to +125°C	Ceramic DIP

MC1437
MC1537

HIGHLY MATCHED DUAL OPERATIONAL AMPLIFIERS

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

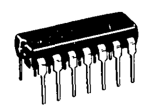
Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics – A_{VOL} = 45,000 typical
- Low Temperature Drift – ±3 µV/°C
- Large Output Voltage Swing – ±14 V typical @ ±15 V Supply

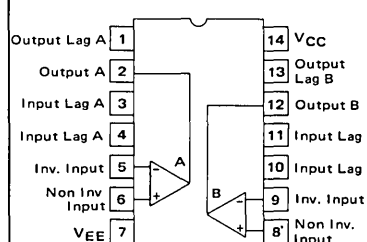
DUAL MC1709

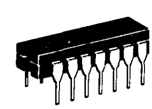
OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1437P only)



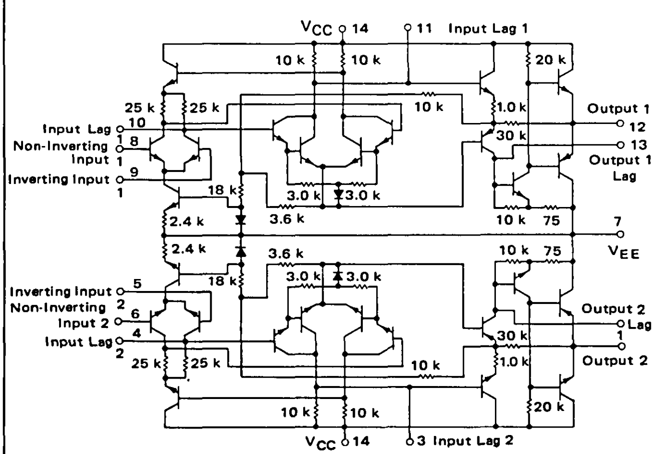


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	Vdc Vdc
Differential Input Voltage Range	V_{IDR}	±5.0	Volts
Common-Mode Input Voltage Range	V_{ICR}	$\pm V_{CC}$	Volts
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C Plastic Package MC1437P Derate above T_A = +25°C	P_D	 750 6.0 625 5.0	 mW mW/°C mW mW/°C
Operating Ambient Temperature Range MC1537 MC1437	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS – Each Amplifier (V_{CC} = +15 Vdc, V_{EE} = –15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1537 Min	MC1537 Typ	MC1537 Max	MC1437 Min	MC1437 Typ	MC1437 Max	Unit
Open Loop Voltage Gain (R_L = 5.0 kΩ, V_o = ±10 V, T_A = T_{low} ① to T_{high} ②)	A_{VOL}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	30	–	–	30	–	Ω
Input Impedance (f = 20 Hz)	z_i	150	400	–	50	150	–	kΩ
Output Voltage Range (R_L = 10 kΩ) (R_L = 2.0 kΩ)	V_{OR}	 ±12 ±10	 ±14 ±13	 – –	 ±12 –	 ±14 –	 – –	V_{peak}
Input Common-Mode Voltage Range	V_{ICR}	±8.0	±10	–	±8.0	±10	–	V_{peak}
Common-Mode Rejection Ratio	CMRR	70	100	–	65	100	–	dB
Input Bias Current $\left(I_{IB} = \frac{I_1 + I_2}{2}\right)$ (T_A = +25°C) (T_A = T_{low} ①)	I_{IB}	 – –	 0.2 0.5	 0.5 1.5	 – –	 0.4 –	 1.5 2.0	µA
Input Offset Current (I_{IO} = I_1 – I_2) (I_{IO} = I_1 – I_2, T_A = T_{low} ①) (I_{IO} = I_1 – I_2, T_A = T_{high} ②)	I_{IO}	 – – –	 0.05 – –	 0.2 0.5 0.2	 – – –	 0.05 – –	 0.5 0.75 0.75	µA
Input Offset Voltage (T_A = +25°C) (T_A = T_{low} ① to T_{high} ②)	V_{IO}	 – –	 1.0 –	 5.0 6.0	 – –	 1.0 –	 7.5 10	mV
Step Response (Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF)	 t_{TLH} t_{PLH}-t_{PHL} SR	 – – –	 0.8 0.38 12	 – – –	 – – –	 0.8 0.38 12	 – – –	 µs µs V/µs
(Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF)	t_{TLH} t_{PLH}-t_{PHL} SR	– – –	0.6 0.34 1.7	– – –	– – –	0.6 0.34 1.7	– – –	µs µs V/µs
(Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF)	t_{TLH} t_{PLH}-t_{PHL} SR	– – –	2.2 1.3 0.25	– – –	– – –	2.2 1.3 0.25	– – –	µs µs V/µs
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low} ① to T_{high} ②) (R_S ≦ 10 kΩ, T_A = T_{low} ① to T_{high} ②)	$\Delta V_{IO}/\Delta T$	 – –	 1.5 3.0	 – –	 – –	 1.5 3.0	 – –	µV/°C
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} ① to +25°C) (T_A = +25°C to T_{high} ②)	$\Delta I_{IO}/\Delta T$	 – –	 0.7 0.7	 – –	 – –	 0.7 0.7	 – –	nA/°C
DC Power Consumption (Total) (Power Supply = ±15 V, V_o = 0)	P_C	–	160	225	–	160	225	mW
Positive Supply Sensitivity (V_{EE} constant)	PSS+	–	10	150	–	10	200	µV/V
Negative Supply Sensitivity (V_{CC} constant)	PSS–	–	10	150	–	10	200	µV/V

① T_{low} = 0°C for MC1437
= –55°C for MC1537

② T_{high} = +70°C for MC1437
= +125°C for MC1537

MATCHING CHARACTERISTICS

Characteristic	Symbol	MC1537 Min	MC1537 Typ	MC1537 Max	MC1437 Min	MC1437 Typ	MC1437 Max	Unit
Open Loop Voltage Gain	A_{VOL1}-A_{VOL2}	–	±1.0	–	–	±1.0	–	dB
Input Bias Current	I_{IB1}-I_{IB2}	–	±0.15	–	–	±0.15	–	µA
Input Offset Current	I_{IO1}-I_{IO2}	–	±0.02	–	–	±0.02	–	µA
Average Temperature Coefficient	$\left\lvert\frac{\Delta I_{IO1}}{\Delta T}\right\rvert - \left\lvert\frac{\Delta I_{IO2}}{\Delta T}\right\rvert$	–	±0.2	–	–	±0.2	–	nA/°C
Input Offset Voltage	V_{IO1}-V_{IO2}	–	±0.2	–	–	±0.2	–	mV
Average Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO1}}{\Delta T}\right\rvert - \left\lvert\frac{\Delta V_{IO2}}{\Delta T}\right\rvert$	–	±0.5	–	–	±0.5	–	µV/°C
Channel Separation (f = 10 kHz)	$\frac{e_{o1}}{e_{o2}}$	–	90	–	–	90	–	dB

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT
V_{CC} = +15 Vdc, V_{EE} = 15 Vdc, T_A = 25°C

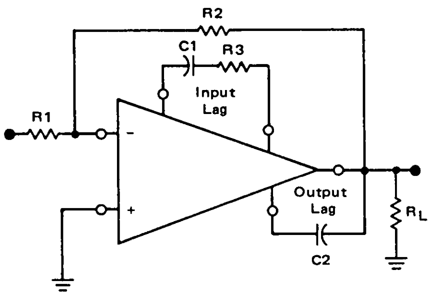


FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS					OUTPUT NOISE (mV(rms))
			R_1(Ω)	R_2(Ω)	R_3(Ω)	C_1(pF)	C_2(pF)	
4	1	1	10 k	10 k	1.5 k	5 0 k	200	0 10
	2	10	10 k	100 k	1 5 k	500	20	0 14
	3	100	10 k	1 0 M	1 5 k	100	3 0	0 7
	4	1000	1 0 k	1 0 M	0	10	3 0	5 2
5	1	1	10 k	10 k	1.5 k	5 0 k	200	0 10
	2	10	10 k	100 k	1 5 k	500	20	0 14
	3	100	10 k	1 0 M	1 5 k	100	3 0	0 7
	4	1000	1 0 k	1 0 M	0	10	3 0	5 2
6	1	A_{VOL}	0	∞	1 5 k	5 0 k	200	5 5
	2	A_{VOL}	0	∞	1 5 k	500	20	10 5
	3	A_{VOL}	0	∞	1 5 k	100	3 0	21 0
	4	A_{VOL}	0	∞	0	10	3 0	39 0
	5	A_{VOL}	0	∞	∞	0	3 0	—

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

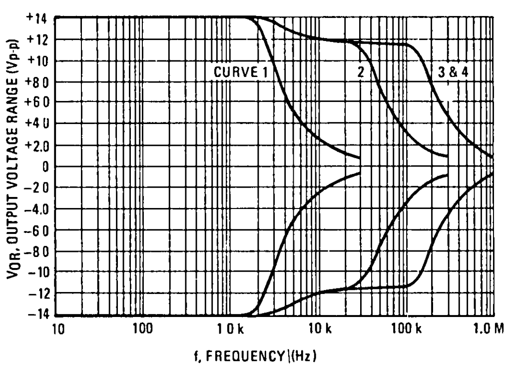


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

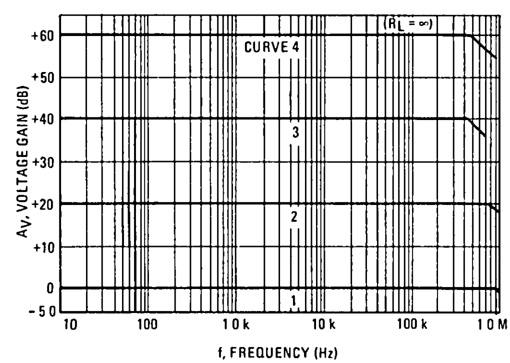


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

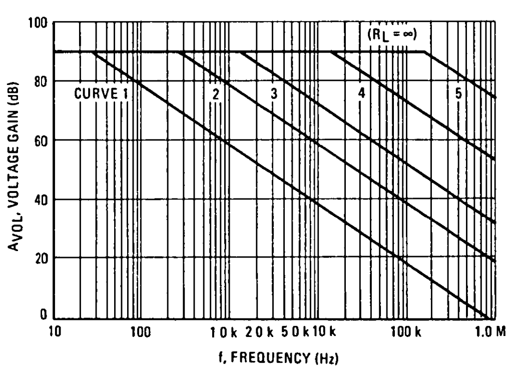
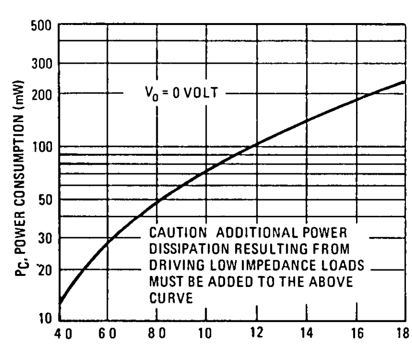


FIGURE 7 – TOTAL POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

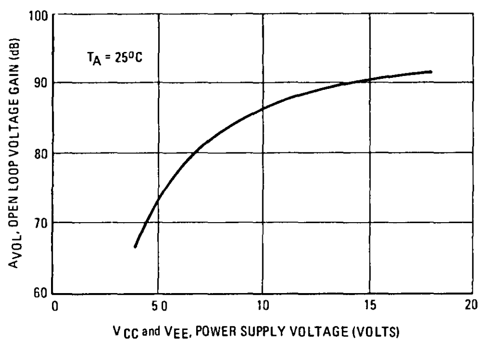


FIGURE 9 – COMMON INPUT SWING versus POWER SUPPLY VOLTAGE

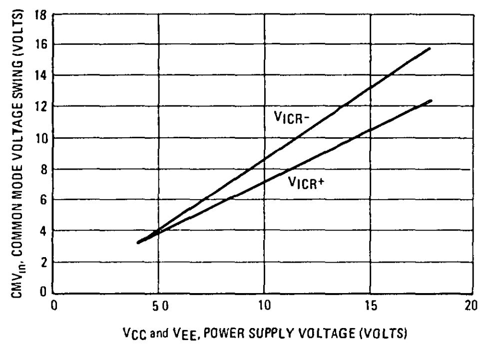


FIGURE 10 – INPUT OFFSET VOLTAGE versus TEMPERATURE

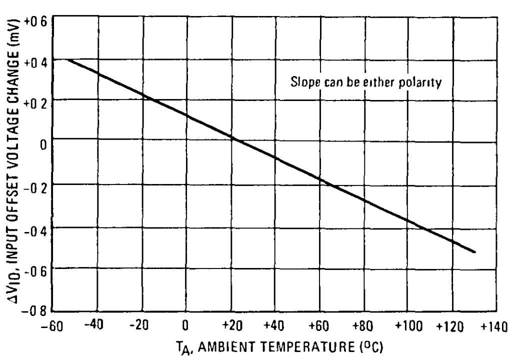


FIGURE 11 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE

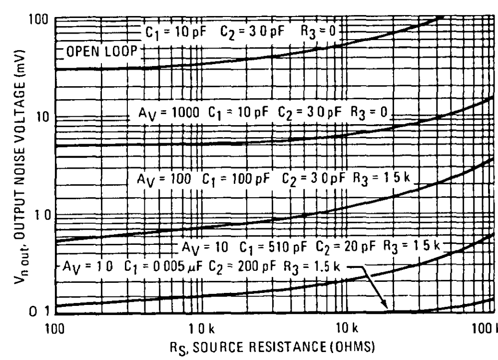
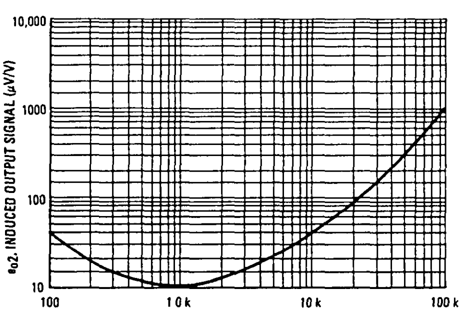
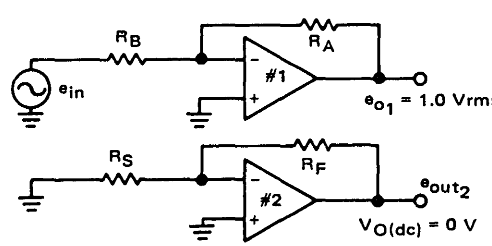


FIGURE 12 – INDUCED OUTPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced output signal (μV of induced output signal in amplifier #2 per volt of output signal at amplifier #1).

ORDERING INFORMATION

Device	Temperature Range	Package
MC1439G	0°C to +70°C	Metal Can
MC1439L	0°C to +70°C	Ceramic DIP
MC1439P1,P2	0°C to +70°C	Plastic DIP
MC1539G	−55°C to +125°C	Metal Can
MC1539L	−55°C to +125°C	Ceramic DIP

MC1439
MC1539

UNCOMPENSATED OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information see Motorola Application Note AN-439.

- Low Input Offset Voltage – 3.0 mV max
- Low Input Offset Current – 60 nA max
- Large Power-Bandwidth – 20 $V_{p\text{-}p}$ Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- High Slew Rate – 34 V/μs typ

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 – HIGH SLEW-RATE INVERTER

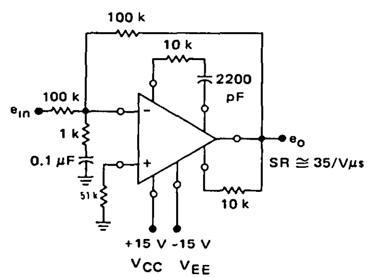
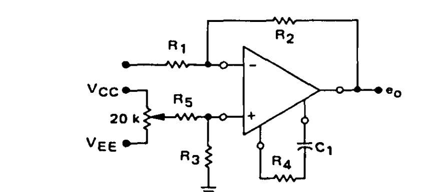
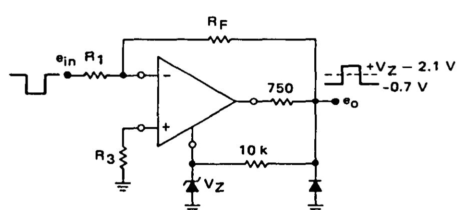


FIGURE 2 – OUTPUT NULLING CIRCUIT

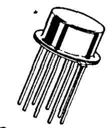


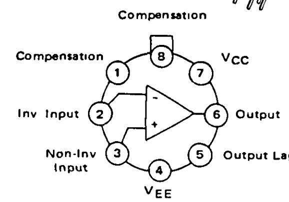
$10\ k \leqslant R_S \leqslant 100(R_3)\ (V_{CC})$

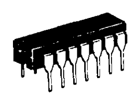
FIGURE 3 – OUTPUT LIMITING CIRCUIT



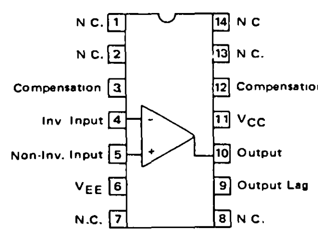
G SUFFIX
METAL PACKAGE
CASE 601





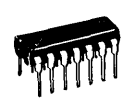


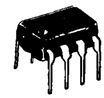
L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)



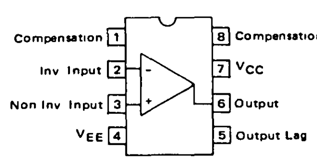
(V_{EE} thru Substrate on P2)

P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1439 only)





P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1439 only)



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1539 Min	MC1539 Typ	MC1539 Max	MC1439 Min	MC1439 Typ	MC1439 Max	Unit
Input Bias Current	I_{IB}							μA
(T_A = +25°C)		–	0.20	0.50	–	0.20	1.0	
(T_A = T_{low} ①)		–	0.23	0.70	–	0.23	1.5	
Input Offset Current	$\|I_{IO}\|$							nA
(T_A = T_{low})		–	–	75	–	–	150	
(T_A = +25°C)		–	20	60	–	20	100	
(T_A = T_{high} ①)		–	–	75	–	–	150	
Input Offset Voltage	$\|V_{IO}\|$							mV
(T_A = +25°C)		–	1.0	3.0	–	2.0	7.5	
(T_A = T_{low}, T_{high})		–	–	4.0	–	–	–	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} to T_{high})	$\|TC_{VIO}\|$							μV/°C
(R_S = 50 Ω)		–	3.0	–	–	3.0	–	
(R_S ≤ 10 kΩ)		–	5.0	–	–	5.0	–	
Input Impedance (f = 20 Hz)	z_{in}	150	300	–	100	300	–	kΩ
Input Common-Mode Voltage Range	V_{ICR}	±11	±12	–	±11	±12	–	V_{pk}
Equivalent Input Noise Voltage (R_S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	e_n	–	30	–	–	30	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 1.0 kHz)	CMRR	80	110	–	80	110	–	dB
Open-Loop Voltage Gain (V_O = ±10 V, R_L = 10 kΩ, R_5 = ∞) (T_A = +25°C to T_{high})	A_{vol}	50,000	120,000	–	15,000	100,000	–	–
(T_A = T_{low})		25,000	100,000	–	15,000	100,000	–	
Power Bandwidth (A_v = 1, THD ≤ 5%, V_O = 20 Vp-p)	PBW							kHz
(R_L = 2.0 kΩ)		–	–	–	10	50	–	
(R_L = 1.0 kΩ, R_5 = 10 k)		20	50	–	–	–	–	
Step Response								
Gain = 1000, no overshoot,	t_{THL}	–	130	–	–	130	–	ns
R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ,	t_{pd}	–	190	–	–	190	–	ns
R4 = 30 kΩ, R5 = 10 kΩ, C1 = 1000 pF	SR	–	6.0	–	–	6.0	–	V/μs
Gain = 1000, 15% overshoot,	t_{THL}	–	80	–	–	80	–	ns
R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ,	t_{pd}	–	100	–	–	100	–	ns
R4 = 0, R5 = 10 kΩ, C1 = 10 pF	SR	–	14	–	–	14	–	V/μs
Gain = 100, no overshoot,	t_{THL}	–	60	–	–	60	–	ns
R1 = 1.0 kΩ, R2 = 100 kΩ, R3 = 1.0 kΩ,	t_{pd}	–	100	–	–	100	–	ns
R4 = 10 kΩ, R5 = 10 kΩ, C1 = 2200 pF	SR	–	34	–	–	34	–	V/μs
Gain = 10, 15% overshoot,	t_{THL}	–	120	–	–	120	–	ns
R1 = 1.0 kΩ, R2 = 10 kΩ, R3 = 1.0 kΩ,	t_{pd}	–	80	–	–	80	–	ns
R4 = 1.0 kΩ, R5 = 10 kΩ, C1 = 2200 pF	SR	–	6.25	–	–	6.25	–	V/μs
Gain = 1, 15% overshoot,	t_{THL}	–	160	–	–	160	–	ns
R1 = 10 kΩ, R2 = 10 kΩ, R3 = 5.0 kΩ,	t_{pd}	–	80	–	–	80	–	ns
R4 = 390 Ω, R5 = 10 kΩ, C1 = 2200 pF	SR	–	4.2	–	–	4.2	–	V/μs
Output Impedance (f = 20 Hz)	z_o	–	4.0	–	–	4.0	–	kΩ
Output Voltage Swing	V_O							V_{pk}
(R_L = 2.0 kΩ, f = 1.0 kHz)		–	–	–	±10	±13	–	
(R_L = 1.0 kΩ, f = 1.0 kHz)		±10	±13	–	–	–	–	
Positive Supply Rejection Ratio (V_{EE} constant, R_5 = ∞)	PSRR+	–	50	150	–	50	200	μV/V
Negative Supply Rejection Ratio (V_{CC} constant, R_5 = ∞)	PSRR-	–	50	150	–	50	200	μV/V
Power Supply Current (V_O = 0)	I_{CC}	–	3.0	5.0	–	3.0	6.7	mAdc
	I_{EE}	–	3.0	5.0	–	3.0	6.7	

① T_{low} = 0°C for MC1439, −55°C for MC1539; T_{high} = +70°C for MC1439, +125°C for MC1539

3

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 +18	Vdc
Differential Input Voltage Range	V_{IDR}	$\pm(V_{CC} + \lvert V_{EE}\rvert)$	Vdc
Common-Mode Input Voltage Range	V_{ICR}	$+V_{CC}, -\lvert V_{EE}\rvert$	Vdc
Load Current	I_L	15	mA
Output Short-Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C Plastic Dual In-Line Packages MC1439 Derate above T_A = +25°C	P_D	 680 4.6 750 6.0 625 5.0	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range MC1539 MC1439	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 -65 to +150 -55 to +125	°C

FIGURE 4 – EQUIVALENT CIRCUIT SCHEMATIC

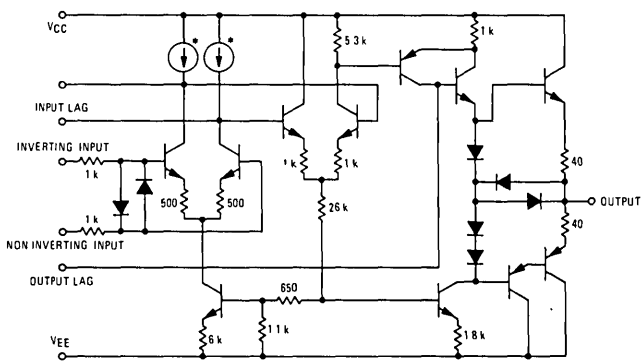


FIGURE 5 – EQUIVALENT CIRCUIT

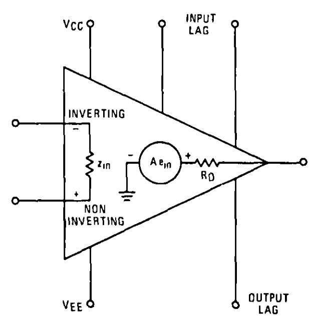
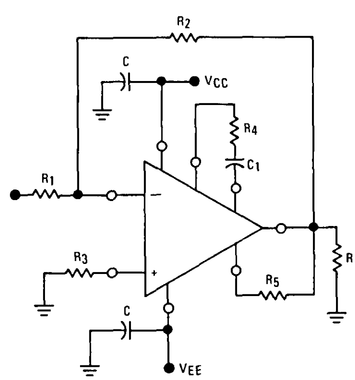


FIGURE 6 – TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc T_A = +25°C

FIGURE NO	CURVE NO	VOLTAGE GAIN	TEST CONDITIONS (FIGURE 6) R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	R_5 (Ω)	C_1 (pF)
7 10 12	1	A_{vol}	0	∞	0	∞	∞	0
	2	1	10 k	10 k	5.0 k	390	10 k	2200
	3	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
	4	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
	5	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	1000
	6	1000	1.0 k	1.0 M	1.0 k	0	10 k	10
8	1	A_{vol}	0	∞	0	∞	∞	0
	2	↓	↓	↓	↓	390	↓	2200
	3	↓	↓	↓	↓	1.0 k	↓	2200
	4	↓	↓	↓	↓	10 k	↓	2200
	5	↓	↓	↓	↓	30 k	↓	1000
	6	↓	↓	↓	↓	0	↓	10
13	ALL	1	10 k	10 k	5.0 k	390	10 k	2200
14	ALL	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
15	ALL	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
16	ALL	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	2200

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 7 — LARGE-SIGNAL SWING versus FREQUENCY

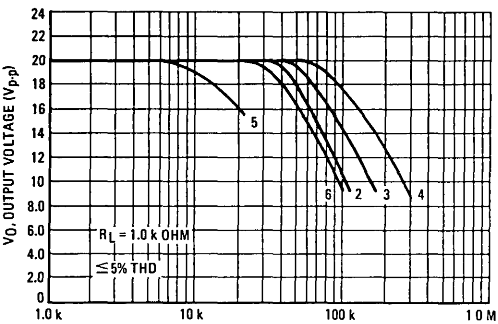


FIGURE 8 — OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

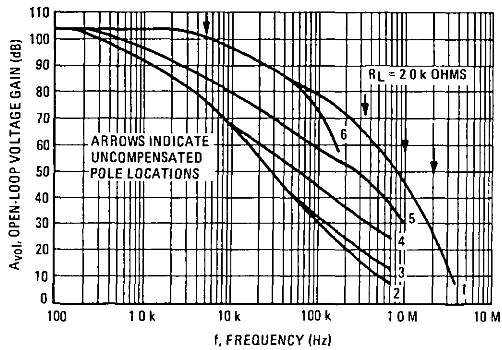


FIGURE 9 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

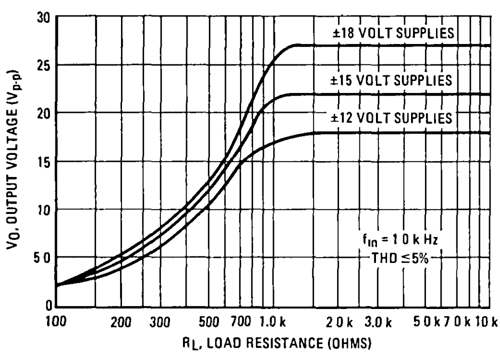


FIGURE 10 — OPEN-LOOP PHASE-SHIFT versus FREQUENCY

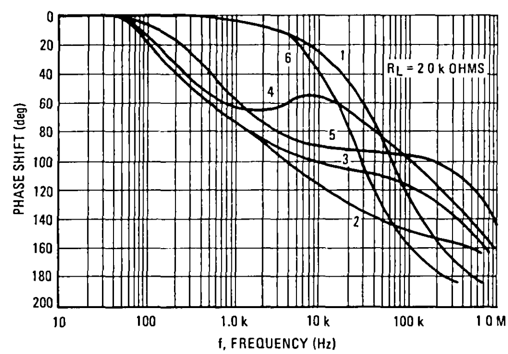


FIGURE 11 — OUTPUT VOLTAGE SWING (to clipping) versus SUPPLY

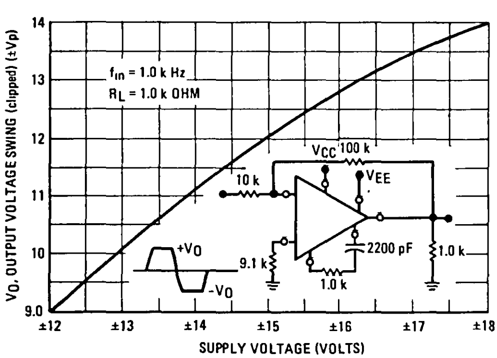
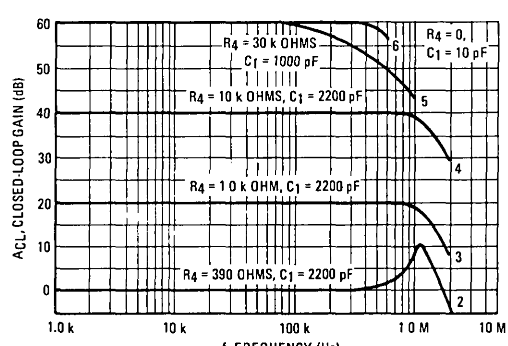


FIGURE 12 — CLOSED-LOOP GAIN versus FREQUENCY



*A_{CL} = Closed-Loop Gain

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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 13 – A_{CL}* = 1 RESPONSE versus TEMPERATURE

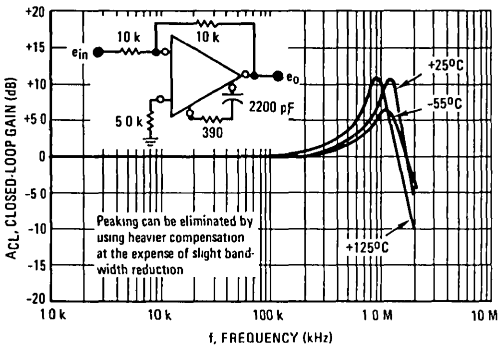


FIGURE 14 – A_{CL} = 10 RESPONSE versus TEMPERATURE

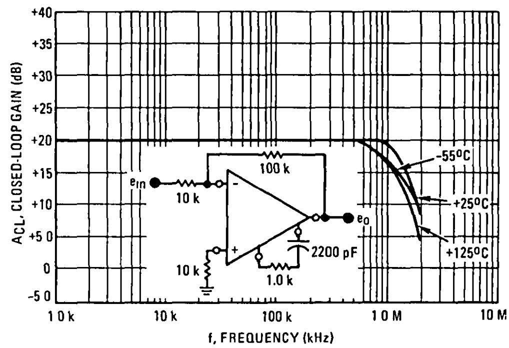


FIGURE 15 – A_{CL} = 100 RESPONSE versus TEMPERATURE

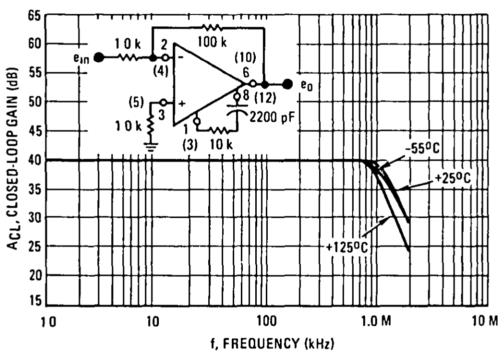


FIGURE 16 – A_{CL} = 1000 RESPONSE versus TEMPERATURE

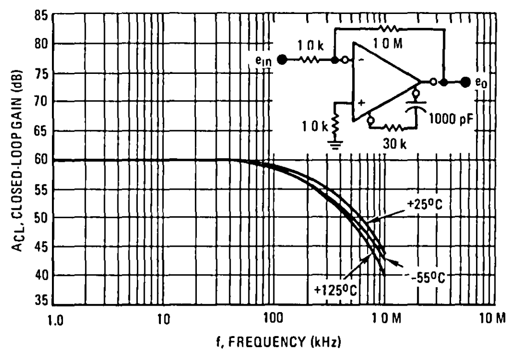


FIGURE 17 – SPECTRAL NOISE DENSITY

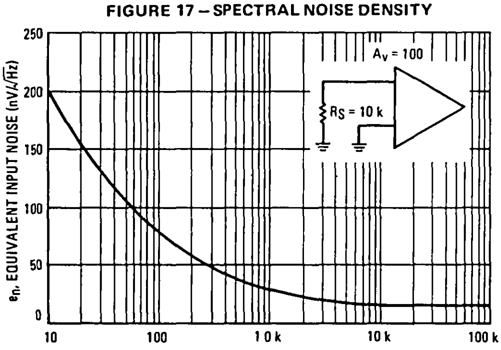
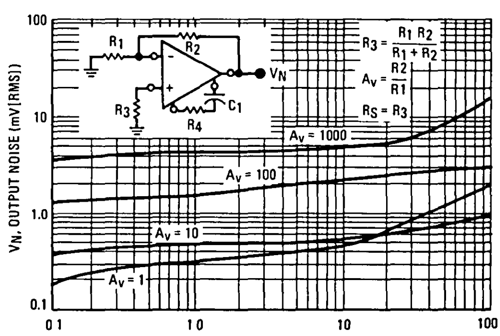


FIGURE 18 – OUTPUT NOISE versus SOURCE RESISTANCE



*A_{CL} = Closed-Loop Gain

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 19 – POWER DISSIPATION versus TEMPERATURE

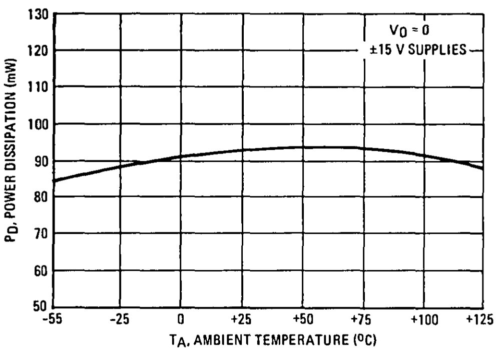


FIGURE 20 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

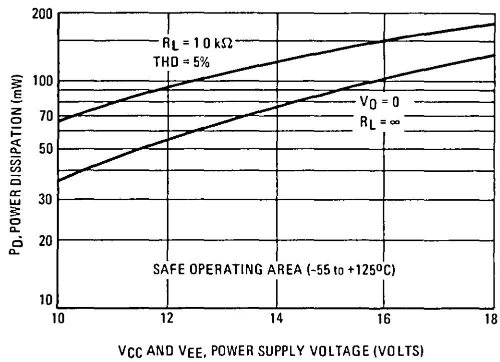


FIGURE 21 – POWER BANDWIDTH (LARGE-SIGNAL SWING versus FREQUENCY)

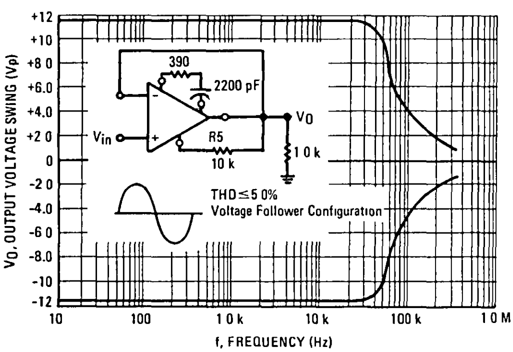


FIGURE 22 – COMMON-MODE INPUT VOLTAGE versus SUPPLY VOLTAGE

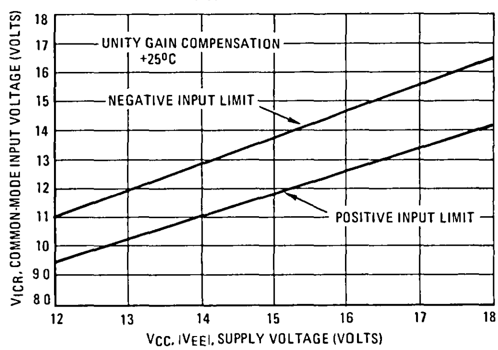


FIGURE 23 – COMMON-MODE REJECTION RATIO versus FREQUENCY

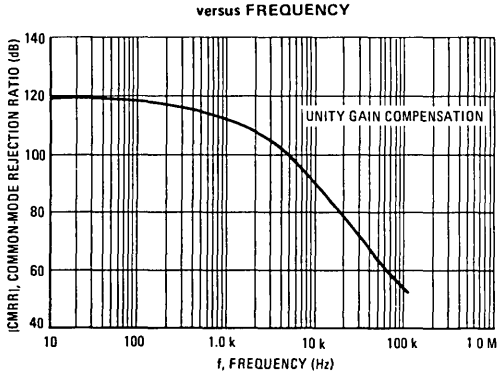


FIGURE 24 – COMMON-MODE REJECTION RATIO versus TEMPERATURE

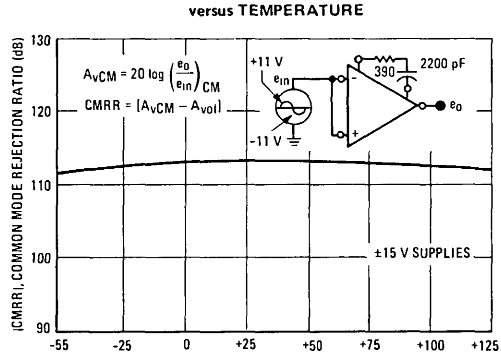


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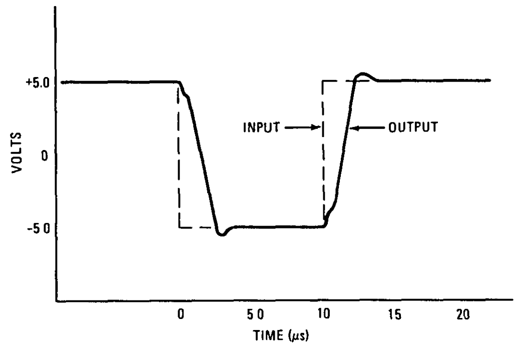
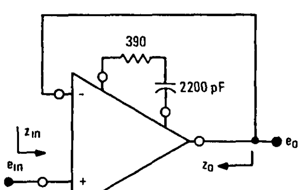
FIGURE 25 – VOLTAGE-FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

FIGURE 26 – VOLTAGE FOLLOWER

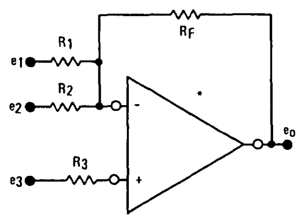


$e_{out} = e_{in} \pm V_{IO}$

$z_{in} > 40$ M OHMS

$$z_{oCL} = z_{oOL}\left[\frac{1+\frac{R_F}{R_I}}{A_{ol}}\right] = 4\,k\left[\frac{1+0}{10^5}\right] \approx 0.04 \text{ OHM}$$

FIGURE 27 – DIFFERENTIAL AMPLIFIER

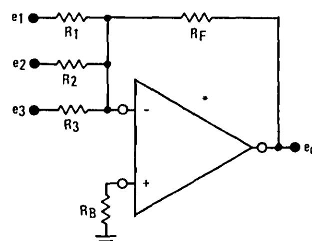


$$e_o = -\left[\frac{R_F}{R_1}e_1 + \frac{R_F}{R_2}e_2\right] + \left[1+\frac{R_F}{R_3}\right]e_3$$

For $R_3 = \frac{R_1, R_2}{R_1 + R_2}$

*Properly Compensated

FIGURE 28 – SUMMING AMPLIFIER

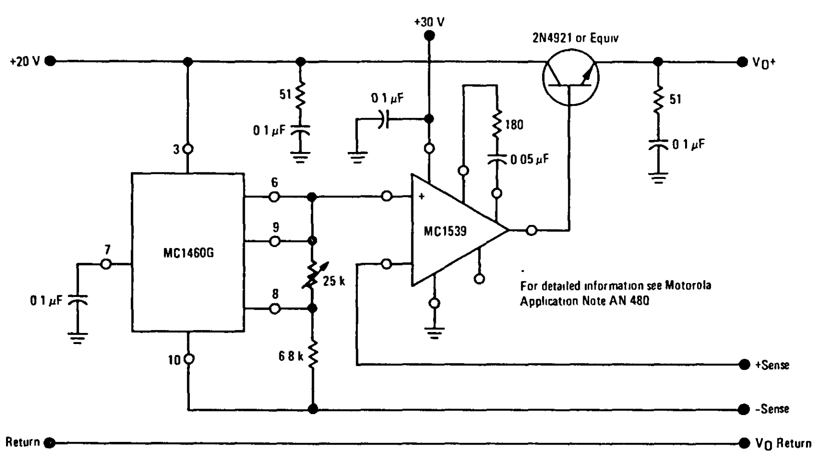


R_B = Parallel Combination of R_1, R_2, R_3, R_F.

$$e_o = -\left[\frac{R_F}{R_1}e_1 + \frac{R_F}{R_2}e_2 + \frac{R_F}{R_3}e_3\right]$$

*Properly Compensated

FIGURE 29 – +15 VOLT REGULATOR



*For detailed information see Motorola Application Note AN 480

TYPICAL APPLICATIONS (continued)

FIGURE 30 – LOAD REGULATION FOR CIRCUIT OF FIGURE 29

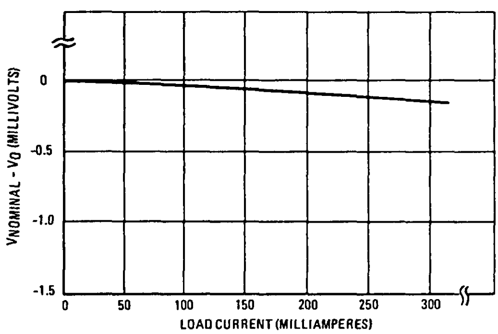
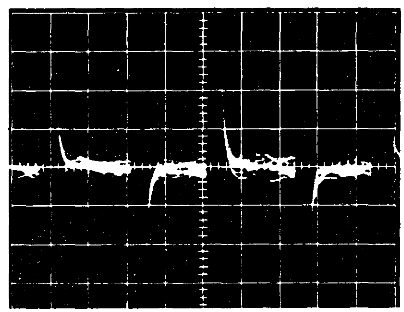


FIGURE 31 – REGULATOR OUTPUT VOLTAGE (under pulsed load condition)



Horizontal Scale 200 μs/Div
Vertical Scale 1 mV/Div

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1456G,CG	0°C to +70°C	Metal Can
MC1456CL,L,CU,U	0°C to +70°C	Ceramic DIP
MC1456CP1,P1	0°C to +70°C	Plastic DIP
MC1556G	−55°C to +125°C	Metal Can
MC1556L	−55°C to +125°C	Ceramic DIP
MC1556U	−55°C to +125°C	Ceramic DIP

MC1456
MC1456C
MC1556

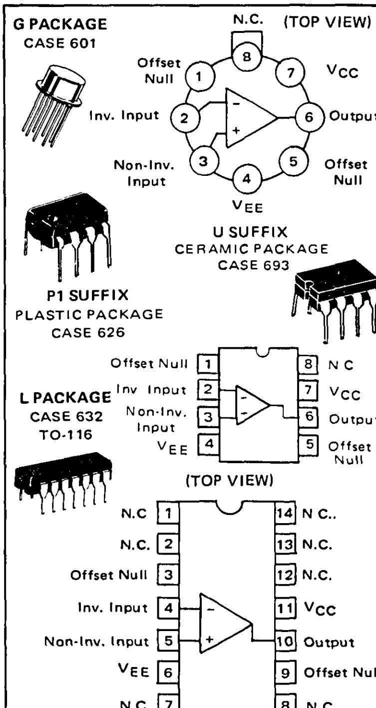
INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information, see Application Note AN-522.

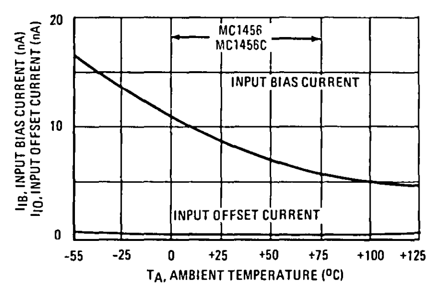
- Low Input Bias Current – 15 nA max
- Low Input Offset Current – 2.0 nA max
- Low Input Offset Voltage – 4.0 mV max
- Fast Slew Rate – 2.5 V/μs typ
- Large Power Bandwidth – 40 kHz typ
- Low Power Consumption – 45 mW max
- Offset Voltage Null Capability
- Output Short-Circuit Protection
- Input Over-Voltage Protection

OPERATIONAL AMPLIFIER

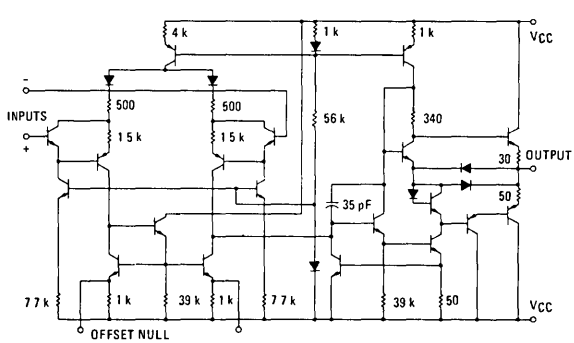
SILICON MONOLITHIC INTEGRATED CIRCUIT



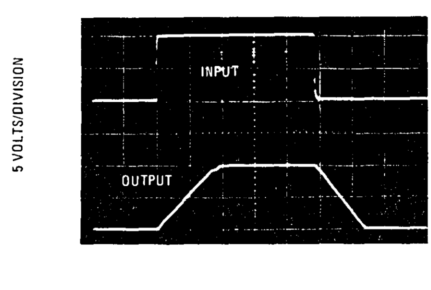
TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT versus TEMPERATURE for MC1556



REPRESENTATIVE CIRCUIT SCHEMATIC



VOLTAGE-FOLLOWER PULSE RESPONSE



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1556	MC1456 MC1456C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Voltage Range	V_{IDR}	$\pm V_{CC}$		Volts
Common-Mode Voltage Range	V_{ICR}	$\pm V_{CC}$		Volts
Load Current	I_L	20		mA
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = - 15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Fig.	Symbol	MC1556 Min	MC1556 Typ	MC1556 Max	MC1456 Min	MC1456 Typ	MC1456 Max	MC1456C Min	MC1456C Typ	MC1456C Max	Unit
Input Bias Current		I_{IB}										nAdc
T_A = +25°C			–	8.0	15	–	15	30	–	15	90	
$T_A = T_{low}$ to T_{high} (See Note 1)			–	–	30	–	–	40	–	–	–	
Input Offset Current		I_{IO}										nAdc
T_A = +25°C			–	1.0	2.0	–	5 0	10	–	5.0	30	
T_A = +25°C to T_{high}			–	–	3.0	–	–	14	–	–	–	
$T_A = T_{low}$ to +25°C			–	–	5.0	–	–	14	–	–	–	
Input Offset Voltage		V_{IO}										mVdc
T_A = +25°C			–	2.0	4.0	–	5.0	10	–	5.0	12	
$T_A = T_{low}$ to T_{high}			–	–	6.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f = 20 Hz)												
Parallel Input Resistance		r_p	–	5 0	–	–	3 0	–	–	3 0	–	Megohms
Parallel Input Capacitance		c_p	–	6.0	–	–	6 0	–	–	6 0	–	pF
Common-Mode Input Impedance (f = 20 Hz)		z_i	–	250	–	–	250		–	250	–	Megohms
Common-Mode Input Voltage Range	1	V_{ICR}	±12	±13	–	+11	±12	–	±10 5	±12	–	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1 0 kHz, BW = 1.0 Hz)	2	e_n	–	45			45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	3	CMRR	80	110	–	70	110	–	–	110	–	dB
Open-Loop Voltage Gain, (V_O = ± 10 V, R_L = 2 0 k ohms)	4,5,6	A_{VOL}										V/V
T_A = +25°C			100,000	200,000	–	70,000	100,000	–	25,000	100,000	–	
$T_A = T_{low}$ to T_{high}			40,000	–	–	40,000	–	–	–	–	–	
Power Bandwidth (A_V = 1, R_L = 2.0 k ohms, THD≤5%, V_O = 20 Vp-p)	9	BW_p	–	40	–	–	40	–		40	–	kHz
Unity Gain Crossover Frequency (open-loop)	5	BW	–	1.0	–	–	1 0	–	–	1 0	–	MHz
Phase Margin (open-loop, unity gain)	5,7		–	70	–	–	70	–	–	70	–	degrees
Gain Margin	5,7		–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)		SR	–	2.5	–	–	2.5	–	–	2 5	–	V/µs
Output Impedance (f = 20 Hz)		z_o	–	1 0	2.0	–	1.0	2 5	–	1.0	–	kohms
Short-Circuit Output Current	8	I_{OS}	–	-17, +9 0	–	–	-17, +9 0	–	–	-17, +9 0	–	mAdc
Output Voltage Swing (R_L = 2 0 k ohms)	10	V_{OR}	±12	±13	–	+11	±12	–	±10	±12	–	V_{pk}
Power Supply Rejection Ratio												µV/V
V_{CC} = constant, $R_S \leqslant$ 10 k ohms		PSRR+		50	100	–	75	200	–	75	–	
V_{EE} = constant, $R_S \leqslant$ 10 k ohms		PSRR-		50	100	–	75	200	–	75	–	
Power Supply Current		I_{CC}	–	1.0	1.5	–	1 3	3.0	–	1 3	4 0	mAdc
		I_{EE}	–	1.0	1.5	–	1.3	3.0	–	1.3	4 0	
DC Quiescent Power Dissipation (V_O = 0)	11	P_D	–	30	45	–	40	90	–	40	120	mW

Note 1 T_{low} 0° for MC1456 and MC1456C
-55°C for MC1556
T_{high} +70°C for MC1456 and MC1456C
+125°C for MC1556

3

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 1 – INPUT COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

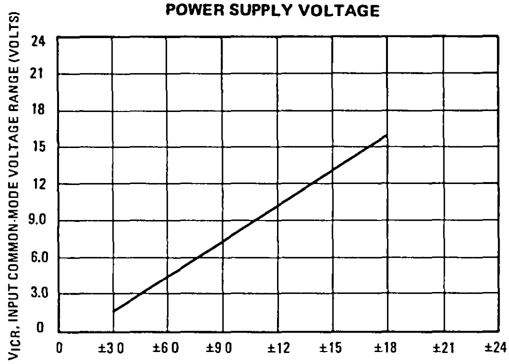


FIGURE 2 – SPECTRAL NOISE DENSITY

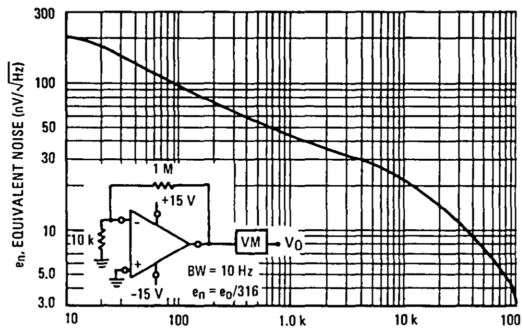


FIGURE 3 – COMMON-MODE REJECTION RATIO versus FREQUENCY

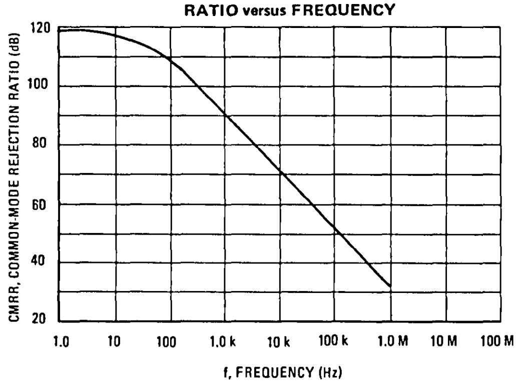


FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

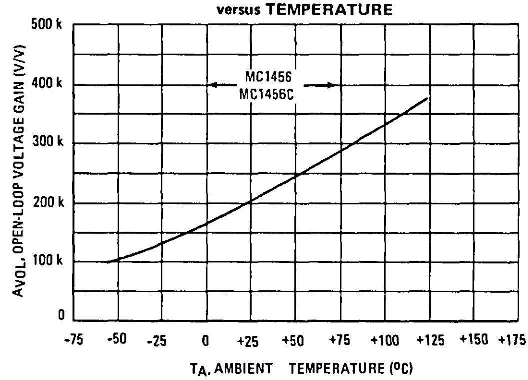


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

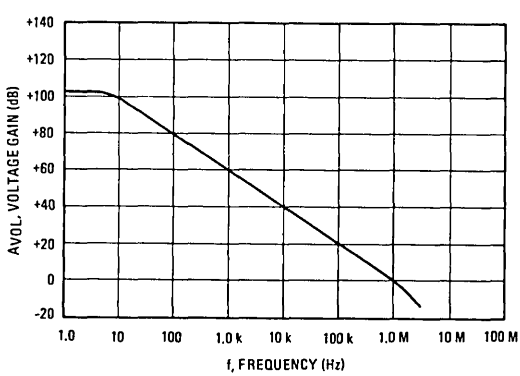
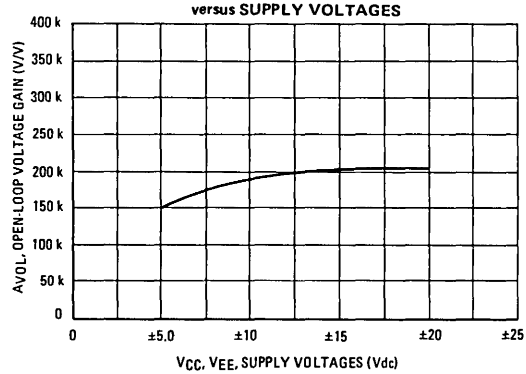


FIGURE 6 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGES



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OPEN-LOOP PHASE SHIFT

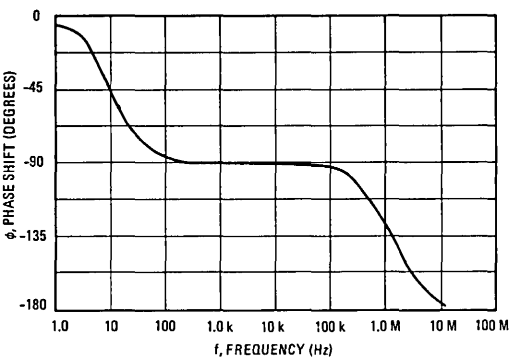


FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

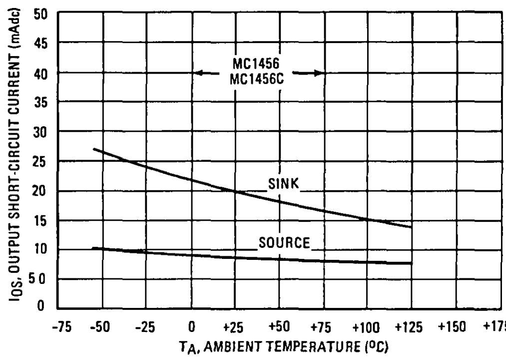


FIGURE 9 – POWER BANDWIDTH

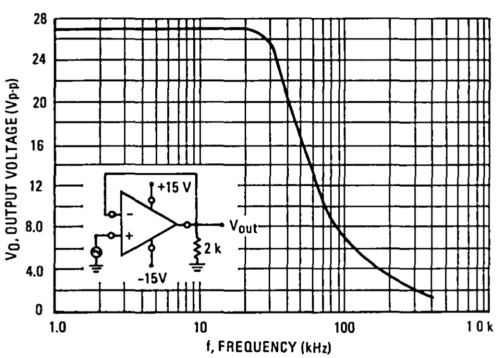


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

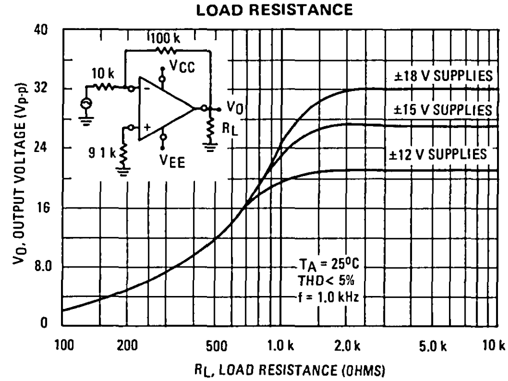
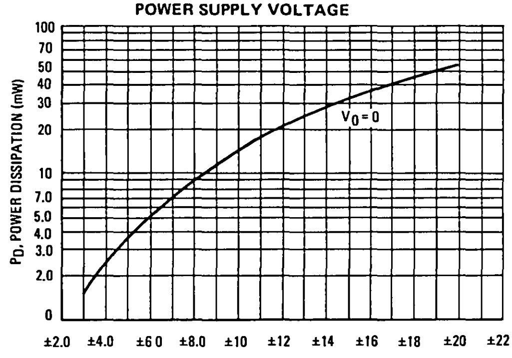


FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



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TYPICAL APPLICATIONS

Where values are not given for external components they must be selected by the designer to fit the requirements of the system.

FIGURE 12 – INVERTING FEEDBACK MODEL

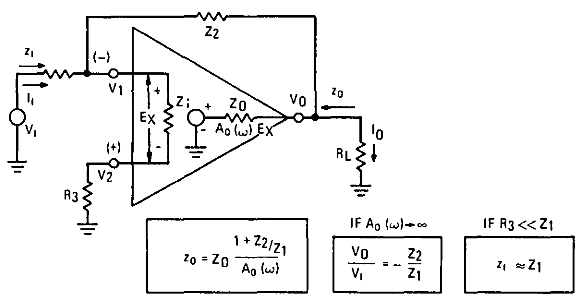


FIGURE 13 – NON-INVERTING FEEDBACK MODEL

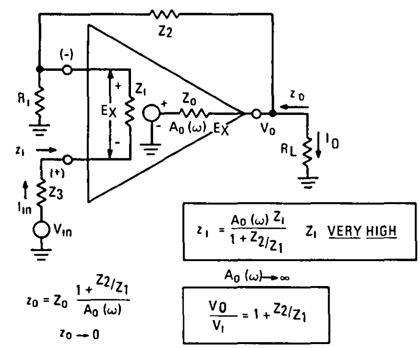


FIGURE 14 – LOW-DRIFT SAMPLE AND HOLD

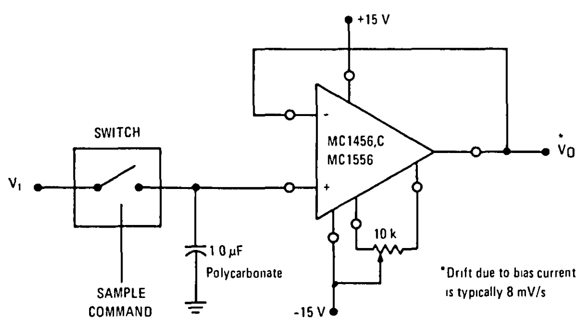
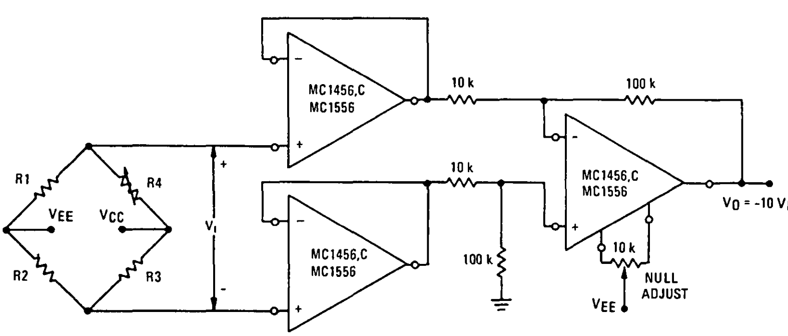


FIGURE 15 – HIGH IMPEDANCE BRIDGE AMPLIFIER



TYPICAL APPLICATIONS (continued)

FIGURE 16 – LOGARITHMIC AMPLIFIER

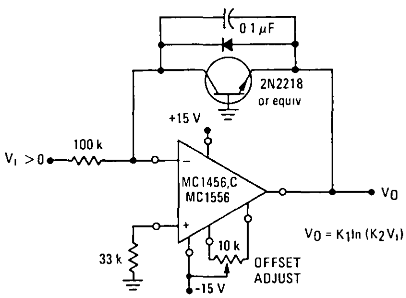


FIGURE 17 – VOLTAGE OFFSET NULL CIRCUIT

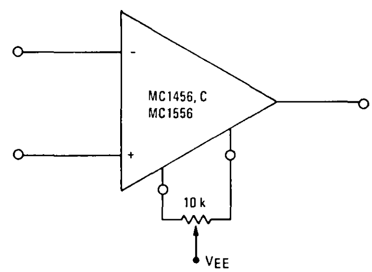


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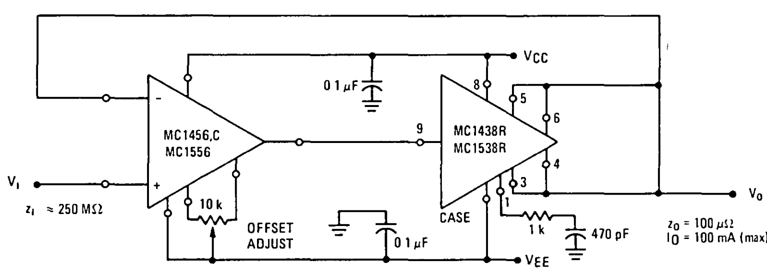
FIGURE 18 – HIGH INPUT IMPEDANCE, HIGH OUTPUT CURRENT VOLTAGE FOLLOWER



ORDERING INFORMATION

Device	Temperature Range	Package
MC1458G,CG,NG	0°C to +70°C	Metal Can
MC1558G,NG	−55°C to +125°C	Metal Can
MC1458CL,CU,L, NL,NU,U	0°C to +70°C	Ceramic DIP
MC1558L,NL,NU,U	−55°C to +125°C	Ceramic DIP
MC1458CP1,CP2, NP1,NP2,P1,P2	0°C to +70°C	Plastic DIP

MC1458 MC1458N
MC1458C
MC1558 MC1558N

(DUAL MC1741)

DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

DUAL MC1741
INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIERS

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered – N Suffix

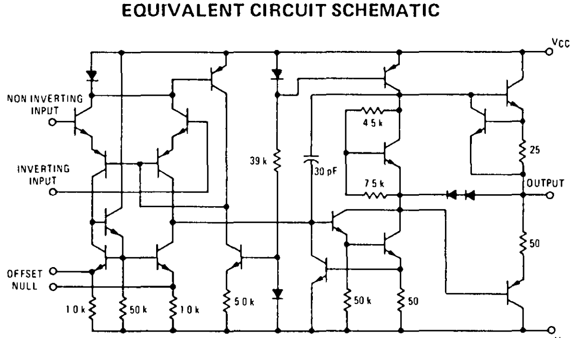
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1458	MC1558	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 175 150		°C

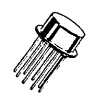
Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage

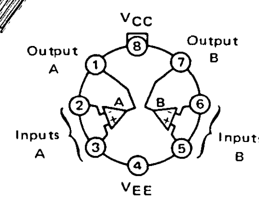
Note 2. Supply voltage equal to or less than 15 V

EQUIVALENT CIRCUIT SCHEMATIC



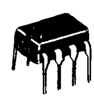
G SUFFIX
METAL PACKAGE
CASE 601



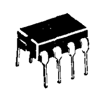


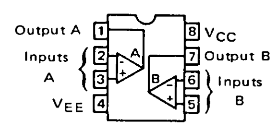
(TOP VIEW)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1458,MC1458C,MC1458N)

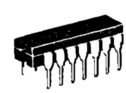


U SUFFIX
CERAMIC PACKAGE
CASE 693

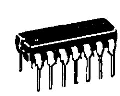


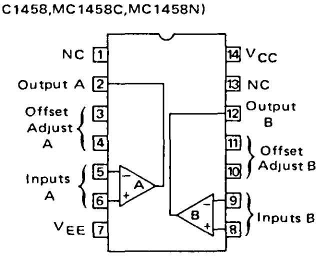


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1458,MC1458C,MC1458N)





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ELECTRICAL CHARACTERISTICS — Note 1. (V_{CC} = 15 V, V_{EE} = 15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq$ 10 k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	–	2 0	10	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	–	20	300	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	–	80	700	nA
Input Resistance	r_i	0.3	2 0	–	0 3	2.0	–	–	2.0	–	MΩ
Input Capacitance	C_i	–	1 4	–	–	1 4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_v										V/mV
(V_O = ±10 V, R_L = 2.0 k)		50	200	–	20	200	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	–	–	–	20	200	–	
Output Resistance	r_o	–	75	–	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq$ 10 k)	CMRR	70	90	–	70	90	–	60	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq$ 10 k)	PSRR	–	30	150	–	30	150	–	30	–	μV/V
Output Voltage Swing	V_O										V
($R_L \geq$ 10 k)		±12	±14	–	±12	±14	–	±11	±14	–	
($R_L \geq$ 2 k)		±10	±13	–	±10	±13	–	±9 0	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	–	20	–	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.0	–	2.3	5.6	–	2 3	8.0	mA
Power Consumption	P_C	–	70	150	–	70	170	–	70	240	mW
Transient Response (Unity Gain)											
(V_I = 20mV, $R_L \geq$ 2kΩ, $C_L \leq$ 100 pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	–	0.3	–	μs
(V_I = 20mV, $R_L \geq$ 2kΩ, $C_L \leq$ 100 pF) Overshoot	os	–	15	–	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq$ 2 kΩ, $C_L \leq$ 100 pF) Slew Rate	SR	–	0 5	–	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = 15 V, T_A = *T_{high} to T_{low} unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq$ 10 kΩ)	V_{IO}	–	1.0	6 0	–	–	7.5	–	–	12	mV
Input Offset Current	I_{IO}										nA
(T_A = 125°C)		–	7.0	200	–	–	–	–	–	–	
(T_A = -55°C)		–	85	500	–	–	–	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	–	–	400	
Input Bias Current	I_{IB}										nA
(T_A = 125°C)		–	30	500	–	–	–	–	–	–	
(T_A = -55°C)		–	300	1500	–	–	–	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	–	–	1000	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	–	–	–	V
Common Mode Rejection Ratio ($R_S \leq$ 10 k)	CMRR	70	90	–	–	–	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq$ 10 k)	PSRR	–	30	150	–	–	–	–	–	–	μV/V
Output Voltage Swing	V_O										V
($R_L \geq$ 10 k)		±12	±14	–	±12	±14	–	–	–	–	
($R_L \geq$ 2 k)		±10	±13	–	±10	±13	–	±9.0	±13	–	
Large Signal Voltage Gain	A_v										V/mV
(V_O = ±10 V, R_L = 2 k)		25	–	–	15	–	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	–	–	–	15	–	–	
Supply Currents (Both Amplifiers)	I_D										mA
(T_A = 125°C)		–	–	4 5	–	–	–	–	–	–	
(T_A = -55°C)		–	–	6 0	–	–	–	–	–	–	
Power Consumption (T_A = 125°C)	P_C	–	–	135	–	–	–	–	–	–	mW
(T_A = -55°C)		–	–	180	–	–	–	–	–	–	

*T_{high} = 125°C for MC1558 and 70°C for MC1458, MC1458C
T_{low} = -55°C for MC1558 and 0°C for MC1458, MC1458C

Note 1. Input pins of an unused amplifier must be grounded.

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NOISE CHARACTERISTICS (Applies for MC1558N and MC1458N only, V_{CC} = 15 V, V_{EE} = -15 V, T_A = 25°C)

Characteristic	Symbol	MC1558N			MC1458N			Unit
		Min	Typ	Max	Min	Typ	Max	
Burst Noise (Popcorn Noise) (BW = 1.0 Hz to 1.0 kHz, t = 10 s, R_S = 100 kΩ) (Input Referenced)	E_n	–	–	20	–	–	20	μVpeak

FIGURE 1 — BURST NOISE versus SOURCE RESISTANCE

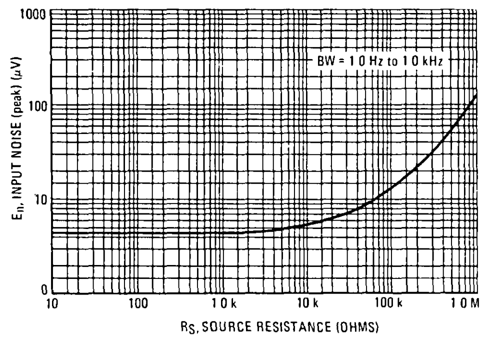


FIGURE 2 — RMS NOISE versus SOURCE RESISTANCE

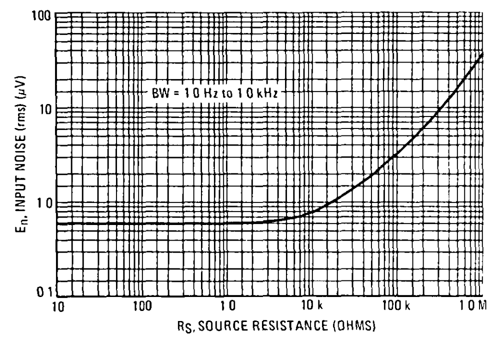


FIGURE 3 — OUTPUT NOISE versus SOURCE RESISTANCE

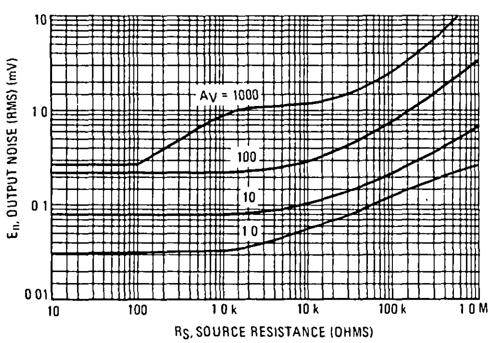


FIGURE 4 — SPECTRAL NOISE DENSITY

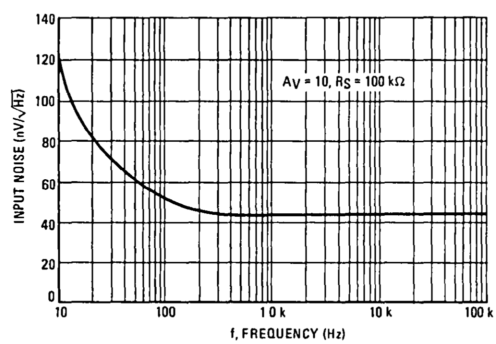
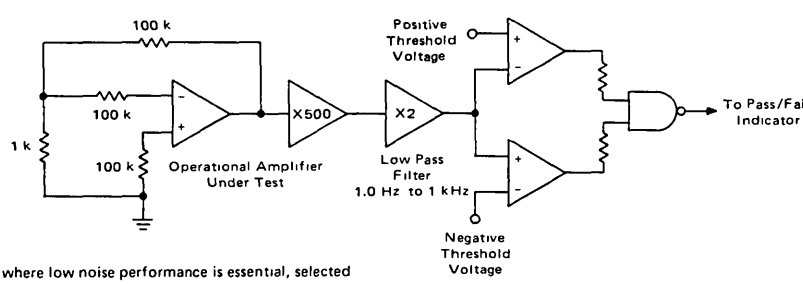


FIGURE 5 — BURST NOISE TEST CIRCUIT (N Suffixed Devices Only)



For applications where low noise performance is essential, selected devices denoted by an N suffix are offered These units have been 100% tested for burst noise pulses on a special noise test system Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

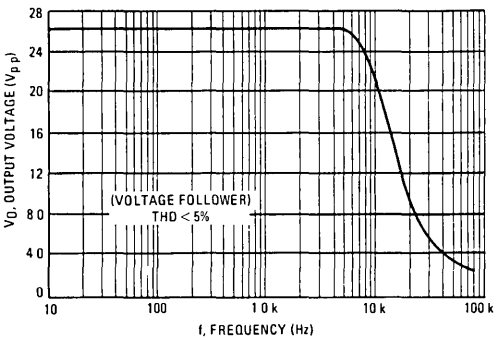


FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE

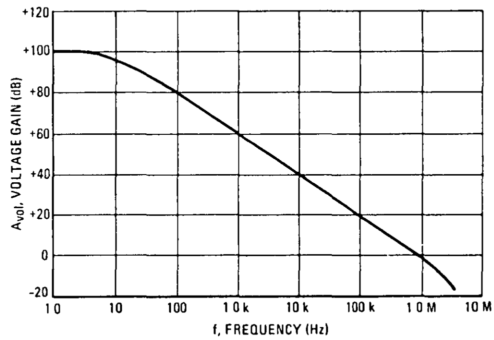


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

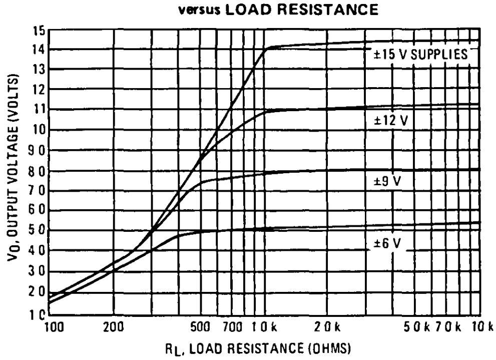


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

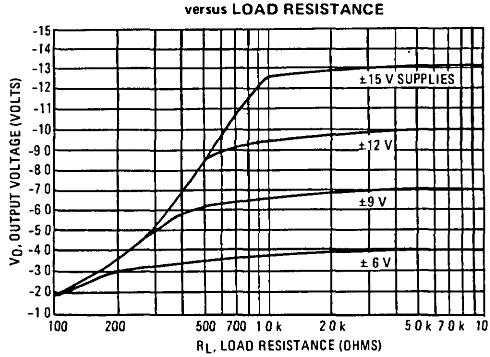


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

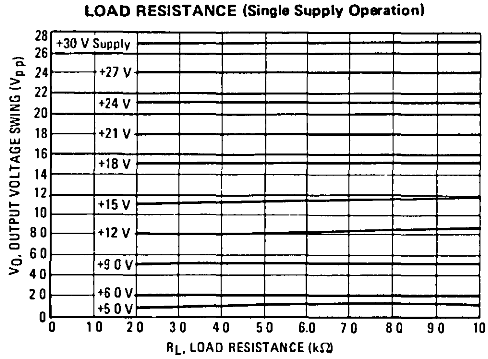


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER

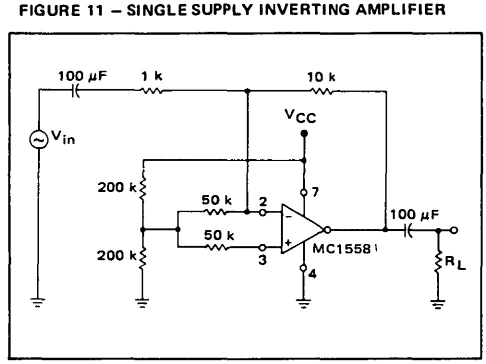


FIGURE 12 – NON-INVERTING PULSE RESPONSE

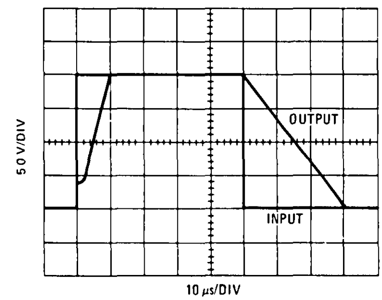


FIGURE 13 – TRANSIENT RESPONSE TEST CIRCUIT

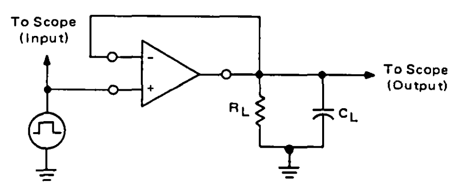
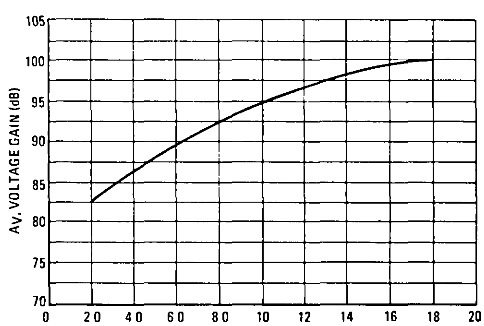


FIGURE 14 – OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1458SG	0°C to +70°C	Metal Can
MC1458SL	0°C to +70°C	Ceramic DIP
MC1458SP1	0°C to +70°C	Plastic DIP
MC1458SP2	0°C to +70°C	Plastic DIP
MC1458SU	0°C to +70°C	Ceramic DIP
MC1558SG	−55°C to +125°C	Metal Can
MC1558SL	−55°C to +125°C	Ceramic DIP
MC1558SU	−55°C to +125°C	Ceramic DIP

MC1458S
MC1558S

DUAL HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIERS

The MC1558S is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1558 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D/A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/μs Guaranteed Minimum (for inverting unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

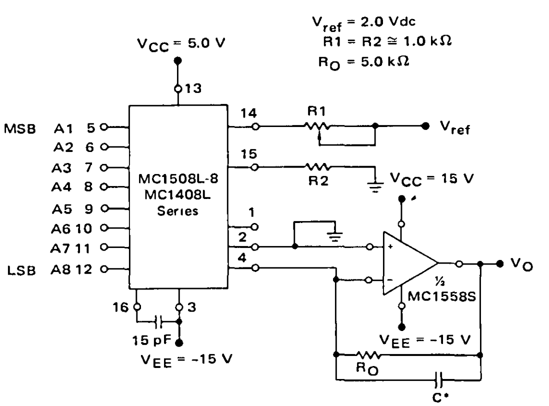
DUAL

OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

3

TYPICAL APPLICATION OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

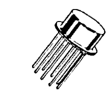
Theoretical V_O

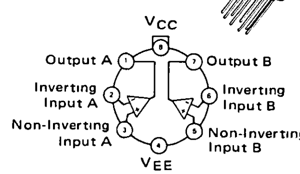
$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

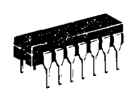
$$V_O = \frac{2\text{ V}}{1\text{ k}}(5\text{ k})\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\text{ V}\left[\frac{255}{256}\right] = 9.961\text{ V}$$

G SUFFIX
METAL PACKAGE
CASE 601



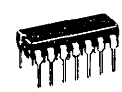


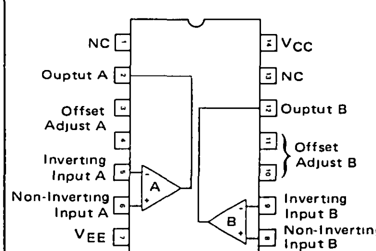
(TOP VIEW)



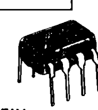
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1458S only)

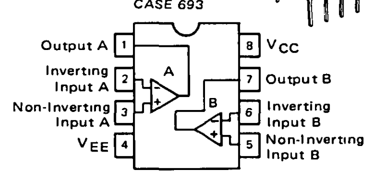




P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1458S Only)

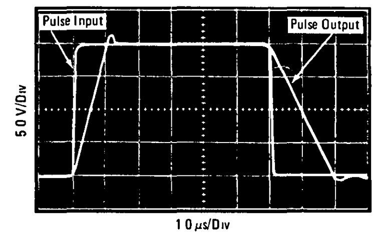


U SUFFIX
CERAMIC PACKAGE
CASE 693

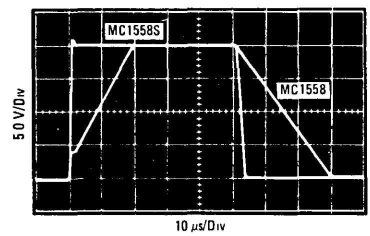


3

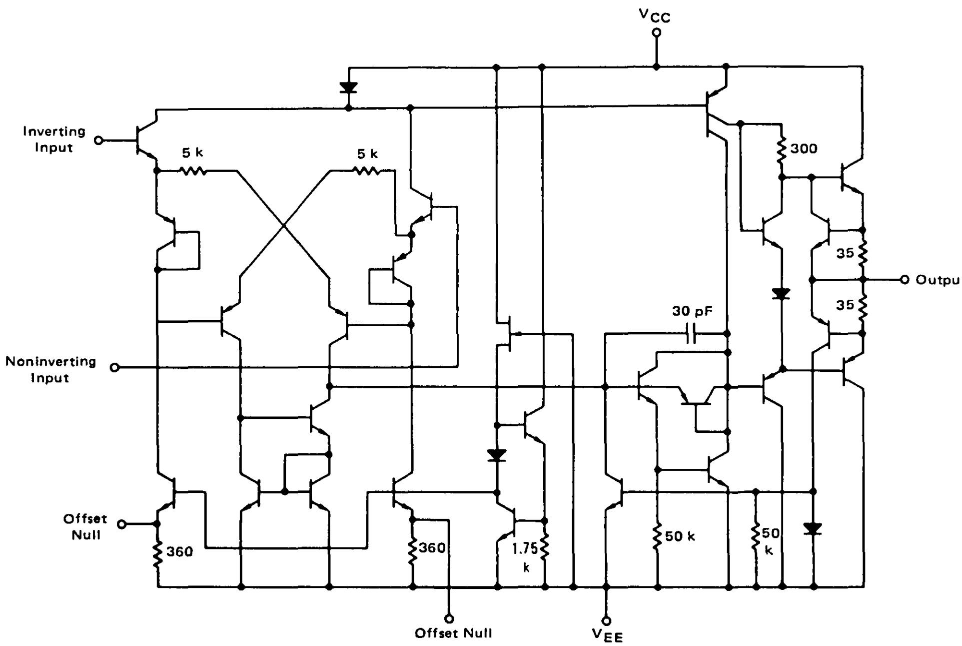
MC1558S LARGE-SIGNAL TRANSIENT RESPONSE
(Inverting Mode)



STANDARD MC1558 versus MC1558S RESPONSE COMPARISON
(Inverting Mode)



½ REPRESENTATIVE CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	MC1558S	MC1458S	Unit
Power Supply Voltage		V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Input Differential Voltage Range ①		V_{IDR}	±30		Volts
Input Common-Mode Voltage Range ②		V_{ICR}	±15		Volts
Output Short Circuit Duration		t_S	Continuous		
Operating Ambient Temperature Range		T_A	-55 to +125	0 to +70	°C
Storage Temperature Range		T_{stg}	-65 to +150	-65 to +150	°C
Junction Temperature	Ceramic and Metal Package Plastic Package	T_J	175 150	175 150	°C °C

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1558S			MC1458S			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Bandwidth (See Figure 3) A_V = 1, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)	BW_P	150	200	–	150	200	–	kHz
Large-Signal Transient Response Slew Rate (Figures 10 and 11)	SR							
V(–) to V(+)		10	20	–	10	20	–	V/µs
V(+) to V(–)		10	12	–	10	12	–	
Settling Time (Figures 10 and 11) (to within 0.1%)	t_{setlg}	–	3.0	–	–	3.0	–	µs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8)								
Rise Time	t_{TLH}	–	0.25	–	–	0.25	–	µs
Fall Time	t_{THL}	–	0.25	–	–	0.25	–	µs
Propagation Delay Time	t_{PLH}, t_{PHL}	–	0.25	–	–	0.25	–	µs
Overshoot	OS	–	20	–	–	20	–	%
Short-Circuit Output Currents	I_{OS}	±10	–	±45	±10	–	±45	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ) (See Figure 4) V_O = ±10 V	A_{vol}	50,000	200,000	–	20,000	100,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing	V_O							V_{pk}
R_L = 10 kΩ		±12	±14	–	±12	±14	–	
R_L = 2.0 kΩ		±10	±13	–	±10	±13	–	
Input Common-Mode Voltage Swing	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2)	I_{IB}	–	200	500	–	200	500	nA
Input Offset Current	$\|I_{IO}\|$	–	30	200	–	30	200	nA
Input Offset Voltage (R_S = ≤10 kΩ)	$\|V_{IO}\|$	–	1.0	5.0	–	2.0	6.0	mV
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0)	P_C	–	70	150	–	70	170	mW
Positive Voltage Supply Sensitivity (V_{EE} constant)	PSS+	–	2.0	150	–	2.0	150	µV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS-	–	10	150	–	10	150	µV/V

**Plastic package offered in limited temperature range device only

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 Vdc, V_{EE} = -15 Vdc, T_A = -55 to +125°C for MC1558S and T_A = 0 to 70°C for MC1458S, unless otherwise noted.)

Characteristic	Symbol	MC1558S			MC1458S			Unit
		Min	Typ	Max	Min	Typ	Max	
Open Loop Voltage Gain V_O = ±10 V	A_{VOL}	25,000	–	–	15,000	–	–	V/V
Output Voltage Swing	V_O							V_{pk}
R_L = 10 kΩ		±12	–	–	±12	–	–	
R_L = 2 kΩ		±10	–	–	±10	–	–	
Input Common-Mode Voltage Range	V_{ICR}	±12	–	–	–	–	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	–	–	–	–	–	dB
Input Bias Current	I_{IB}							nA
T_A = 125°C		–	200	500	–	–	–	
T_A = -55°C		–	500	1500	–	–	–	
T_A = 0 to 70°C		–	–	–	–	–	800	
Input Offset Current	I_{IO}							nA
T_A = 125°C		–	30	200	–	–	–	
T_A = -55°C		–	–	500	–	–	–	
T_A = 0 to 70°C		–	–	–	–	–	300	
Input Offset Voltage R_S ≤ 10 kΩ	V_{IO}	–	–	6.0	–	–	7.5	mV
DC Power Consumption V_O = 0 V	P_C	–	–	200	–	–	–	mW
Positive Power Supply Sensitivity V_{EE} = -15 V	P_{SS+}	–	–	150	–	–	–	µV/V
Negative Power Supply Sensitivity V_{CC} = 15 V	P_{SS-}	–	–	150	–	–	–	µV/V

3

3

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 1 – OFFSET ADJUST CIRCUIT

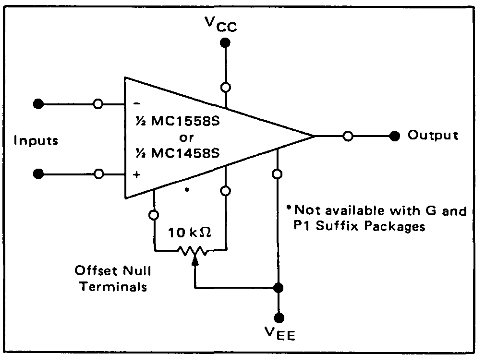


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

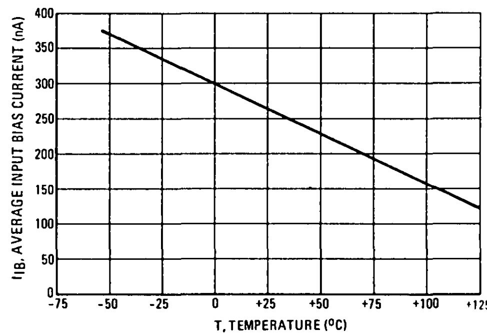


FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

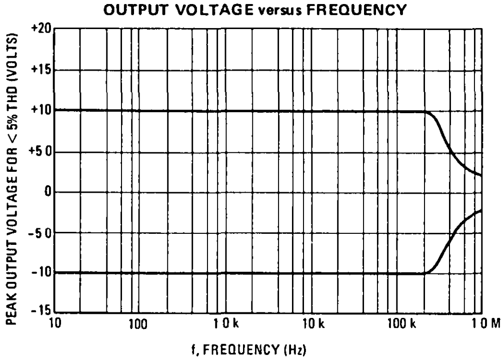


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

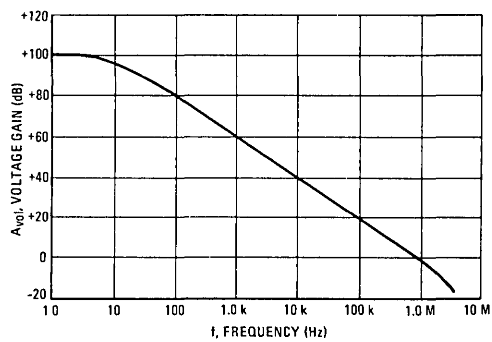
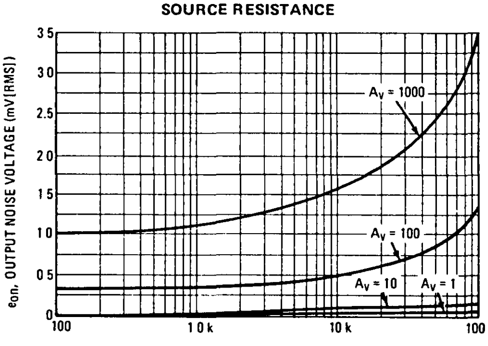


FIGURE 5 – OUTPUT NOISE versus SOURCE RESISTANCE



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 6 — SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

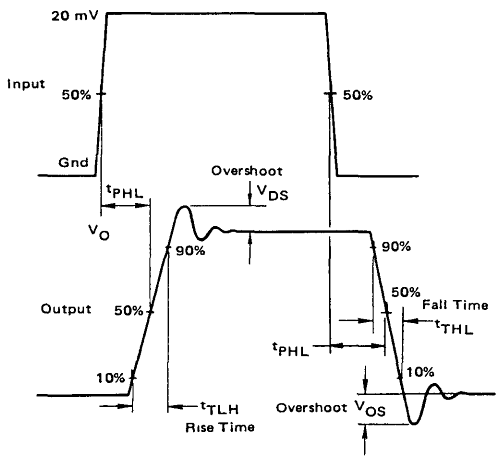


FIGURE 7 — SMALL-SIGNAL TRANSIENT RESPONSE

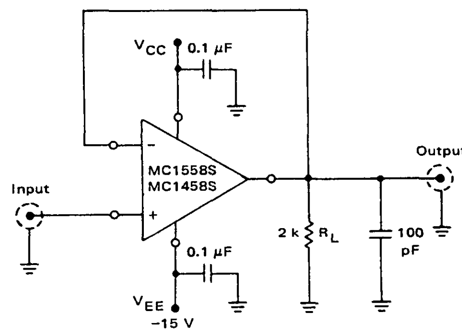


FIGURE 8 — POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

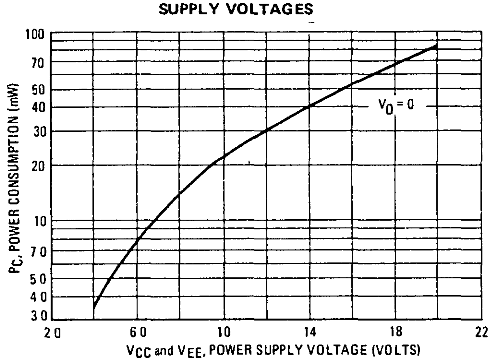


FIGURE 9 — LARGE-SIGNAL TRANSIENT WAVEFORMS

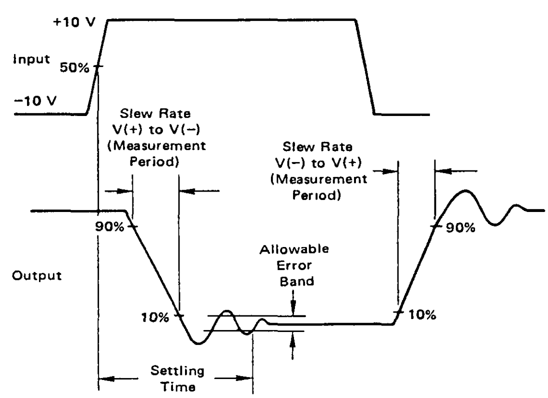
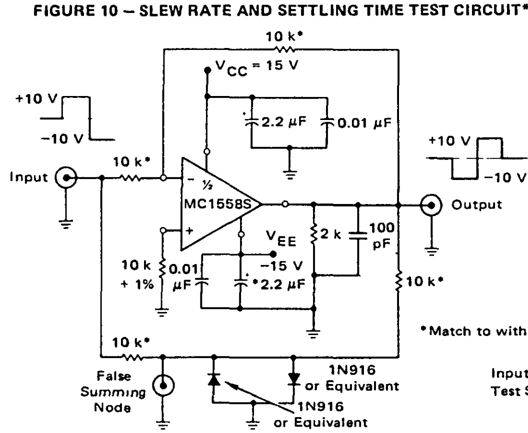


FIGURE 10 — SLEW RATE AND SETTLING TIME TEST CIRCUIT*



*Match to within 0.01%.

Inputs of Amplifier Not Under Test Should Be Grounded.

3

SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time
x = amplifier settling time (to be determined)
y = false summing junction settling time
z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1558S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L-8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

FIGURE 11 — WAVEFORM AT FALSE SUMMING NODE
(Inverting Mode)

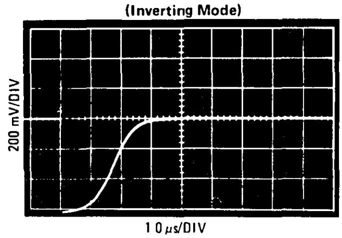
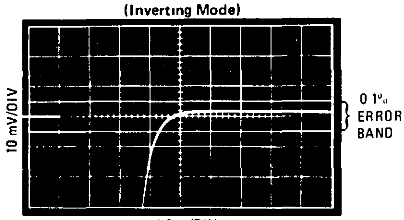
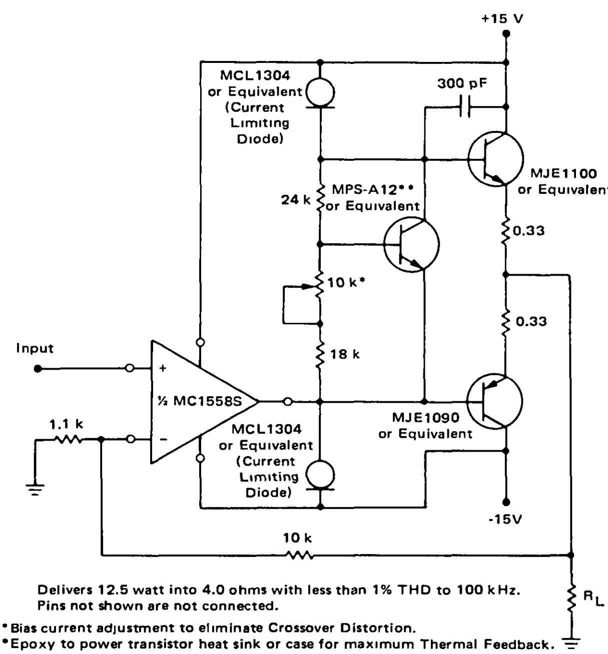


FIGURE 12 — EXPANDED WAVEFORM AT FALSE SUMMING NODE
(Inverting Mode)



TYPICAL APPLICATION

FIGURE 13 — 12.5-WATT WIDEBAND POWER AMPLIFIER



Delivers 12.5 watt into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.

*Bias current adjustment to eliminate Crossover Distortion.
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1709CF	0°C to +70°C	Ceramic Flat
MC1709CG	0°C to +70°C	Metal Can
MC1709CL,CU	0°C to +70°C	Ceramic DIP
MC1709CP1,CP2	0°C to +70°C	Plastic DIP
MC1709F,AF	−55°C to +125°C	Ceramic Flat
MC1709G,AG	−55°C to +125°C	Metal Can
MC1709L,AL,U	−55°C to +125°C	Ceramic DIP

MC1709
MC1709A
MC1709C

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

OPERATIONAL AMPLIFIER

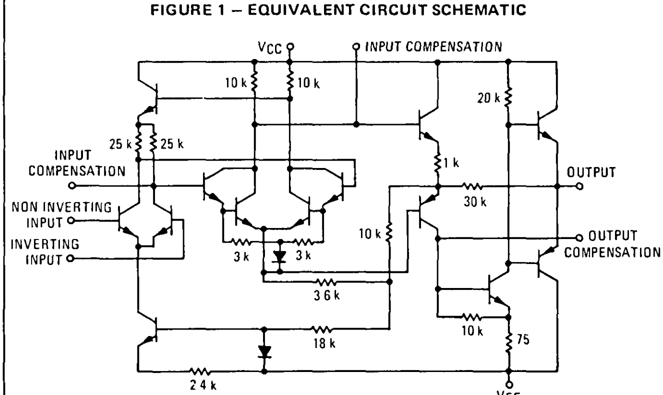
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
  A_{vol} = 45,000 typical
- Low Temperature Drift — ±3.0 μV/°C typical (MC1709)
- Large Output Voltage Swing — ±14 V typical @ ±15 V Supply
- Low Output Impedance — z_o = 150 ohms typical

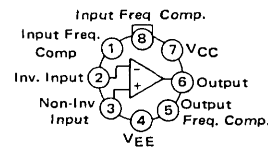
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	Vdc
Input Differential Voltage Range	V_{IDR}	±5.0	Volts
Input Common-Mode Range	V_{ICR}	±10	Volts
Output Load Current	I_L	10	mA
Output Short-Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C	P_D	 680 4.6	 mW mW/°C
Flat Package Derate above T_A = +25°C Plastic Dual In-Line Packages (MC1709C only) Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C		500 3.3 625 5.0 750 6.0	mW mW/°C mW mW/°C mW/°C mW/°C
Operating Ambient Temperature Range MC1709A, MC1709 MC1709C	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 -65 to +150 -55 to +125	°C

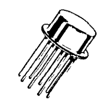
FIGURE 1 — EQUIVALENT CIRCUIT SCHEMATIC



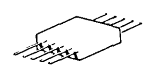
PIN CONNECTIONS

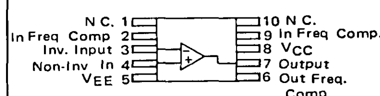


G SUFFIX
METAL PACKAGE
CASE 601

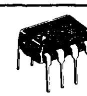


F SUFFIX
CERAMIC PACKAGE
CASE 606-04
TO-91

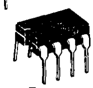


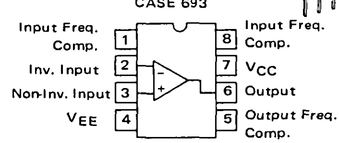


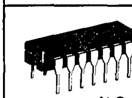
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1709C only)



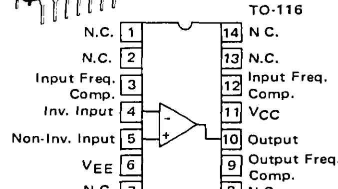
U SUFFIX
CERAMIC PACKAGE
CASE 693



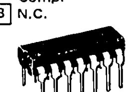




L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116



P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1709C only)



3

ELECTRICAL CHARACTERISTICS (unless otherwise noted, 9 0 V $\leq V_{CC} \leq$ 15 V, -9.0 V $\geq V_{EE} \geq$ -15 V, T_A = 25°C)

Characteristic	Symbol	MC1709A Min	MC1709A Typ	MC1709A Max	MC1709 Min	MC1709 Typ	MC1709 Max	Unit
Input Offset Voltage ($R_S \leq$ 10 kΩ)	V_{IO}	–	0.6	2.0	–	1.0	5 0	mV
Input Offset Current	I_{IO}	–	10	50	–	50	200	nA
Input Bias Current	I_{IB}	–	100	200	–	200	500	nA
Input Resistance	r_i	350	700	–	150	400	–	kΩ
Output Resistance	r_o	–	150	–	–	150	–	Ω
Power Supply Currents (V_{CC} = 15 V, V_{EE} = -15 V)	I_{CC}, I_{EE}	–	2 5	3.6	–	–	–	mA
Power Consumption (V_{CC} = 15 V, V_{EE} = -15 V)	P_C	–	75	108	–	80	165	mW
Transient Response (V_{CC} = 15 V, V_{EE} = -15 V) See Figure 8								
Risetime	t_{TLH}	–	–	1.5	–	0.3	1.0	µs
Overshoot	OS	–	–	30	–	10	30	%

ELECTRICAL CHARACTERISTICS (unless otherwise noted, 9.0 V $\leq V_{CC} \leq$ 15 V, -9 0 V $\geq V_{EE} \geq$ -15 V, T_A = -55°C to +125°C)

Characteristic	Symbol	MC1709A Min	MC1709A Typ	MC1709A Max	MC1709 Min	MC1709 Typ	MC1709 Max	Unit
Input Offset Voltage ($R_S \leq$ 10 kΩ)	V_{IO}	–	–	3.0	–	–	6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							µV/°C
(R_S = 50 Ω, T_A = 25°C to 125°C)		–	1.8	10	–	–	–	
(R_S = 50 Ω, T_A = -55°C to 25°C)		–	1.8	10	–	–	–	
(R_S = 50 Ω, T_A = -55°C to 125°C)		–	–	–	–	3.0	–	
(R_S = 10 kΩ, T_A = 25°C to 125°C)		–	2.0	15	–	–	–	
(R_S = 10 kΩ, T_A = -55°C to 25°C)		–	4.8	25	–	–	–	
(R_S = 10 kΩ, T_A = -55°C to 125°C)		–	–	–	–	6 0	–	
Input Offset Current	I_{IO}							nA
(T_A = -55°C)		–	40	250	–	100	500	
(T_A = 125°C)		–	3 5	50	–	20	200	
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
(T_A = -55°C to 25°C)		–	0.45	2 8	–	–	–	
(T_A = 25°C to 125°C)		–	0.08	0.5	–	–	–	
Input Bias Current (T_A = -55°C)	I_{IB}	–	300	600	–	500	1500	nA
Input Resistance (T_A = -55°C)	r_i	85	170	–	40	100	–	kΩ
Input Common-Mode Voltage Range (V_{CC} = 15 V, V_{EE} = -15 V)	V_{ICR}	±8 0	±10	–	±8.0	±10	–	V
Common Mode Rejection Ratio ($R_S \leq$ 10 kΩ)	CMRR	80	110	–	70	90	–	dB
Supply Voltage Rejection Ratio (V_{CC} = 15 V, V_{EE} = -15 V, $R_S \leq$ 10 kΩ)	PSRR	–	40	100	–	25	150	µV/V
Large Signal Voltage Gain (V_{CC} = 15 V, V_{EE} = -15 V, $R_L \geq$ 2 0 kΩ, V_O = ±15 V)	A_V	25	45	70	25	45	70	V/mV
Output Voltage Range (V_{CC} = 15 V, V_{EE} = -15 V)	V_{OR}							V
($R_L \geq$ 10 kΩ)		±12	±14	–	±12	±14	–	
($R_L \geq$ 2 0 kΩ)		±10	±13	–	±10	±13	–	
Power Supply Currents (V_{CC} = 15 V, V_{EE} = -15 V)	I_{CC}/I_{EE}							mA
(T_A = -55°C)		–	2.7	4.5	–	–	–	
(T_A = 125°C)		–	2.1	3.0	–	–	–	
Power Consumption (V_{CC} = 15, V_{EE} = -15 V)	P_C							mW
(T_A = -55°C)		–	81	135	–	–	–	
(T_A = 125°C)		–	63	90	–	–	–	

ELECTRICAL CHARACTERISTICS (unless otherwise noted, V_{CC} = 15 V, V_{EE} = -15 V, T_A = 25°C)

Characteristic	Symbol	MC1709C Min	MC1709C Typ	MC1709C Max	Unit
Input Offset Voltage ($R_S \leq$ 10 kΩ, 9.0 V ≤ 15 V, -9.0 V ≥ V_{EE} ≥ -15 V)	V_{IO}	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	100	500	nA
Input Bias Current	I_{IB}	–	300	1500	nA
Input Resistance	r_i	50	250	–	kΩ
Output Resistance	r_O	–	150	–	Ω
Power Consumption	P_C	–	80	200	mW
Large Signal Voltage Gain ($R_L \geq$ 2.0 kΩ, V_O = ±10 V)	A_V	15	45	–	V/mV
Output Voltage Range	V_{OR}				V
($R_L \geq$ 10 kΩ)		±12	±14	–	
($R_L \geq$ 2.0 kΩ)		±10	±13	–	
Input Common-Mode Voltage Range	V_{ICR}	±8.0	±10	–	V
Common Mode Rejection Ratio ($R_S \leq$ 10 kΩ)	CMRR	65	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq$ 10 kΩ)	PSRR	–	25	200	μV/V
Transient Response See Figure 8					
Rise Time	T_{TLH}	–	0.3	–	μs
Overshoot	OS	–	10	–	%

3

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC} = 15 V, V_{EE} = -15 V, T_A = 0°C to 70°C)

Parameter	Symbol	MC1709C Min	MC1709C Typ	MC1709C Max	Unit
Input Offset Voltage ($R_S \leq$ 10 kΩ, 9.0 V ≤ V_{CC} ≤ 15 V, -9.0 V ≥ V_{EE} ≥ 15 V)	V_{IO}	–	–	10	mV
Input Offset Current	I_{IO}	–	–	750	nA
Input Bias Current	I_{IB}	–	–	2.0	μA
Large Signal Voltage Gain ($R_L \geq$ 2.0 kΩ, V_O = ±10 V)	A_V	12	–	–	V/mV
Input Resistance	r_i	35	–	–	kΩ

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT
(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C)

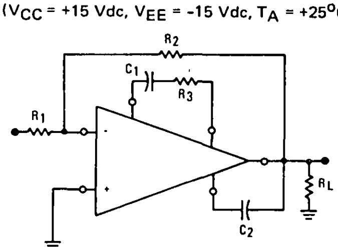


Fig. No.	Curve No.	Test Conditions R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (pF)	C_2 (pF)
3	1	10 k	10 k	1.5 k	5.0 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1.0 M	1.5 k	100	3.0
	4	1.0 k	1.0 M	0	10	3.0
4	1	1.0 k	1.0 M	0	10	3.0
	2	10 k	1.0 M	1.5 k	100	3.0
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5.0 k	200
5	1	0	∞	1.5 k	5.0 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3.0
	4	0	∞	0	10	3.0

3

FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY

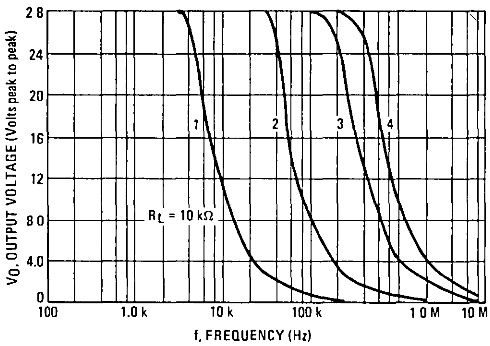


FIGURE 4 – CLOSED LOOP VOLTAGE GAIN versus FREQUENCY

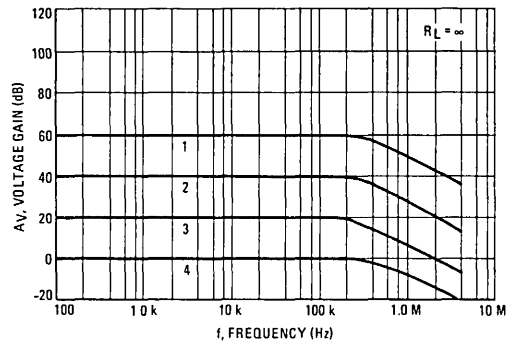


FIGURE 5 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

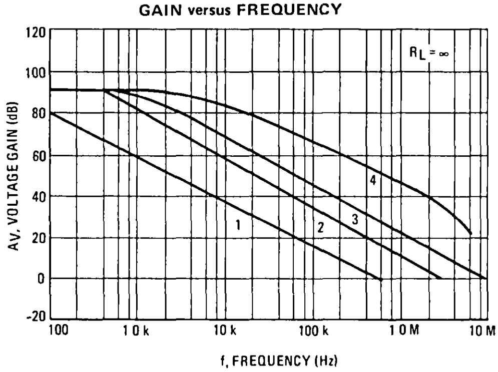


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

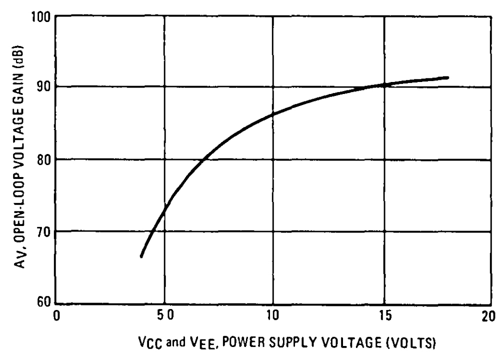


FIGURE 7 – SLEW RATE versus CLOSED LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

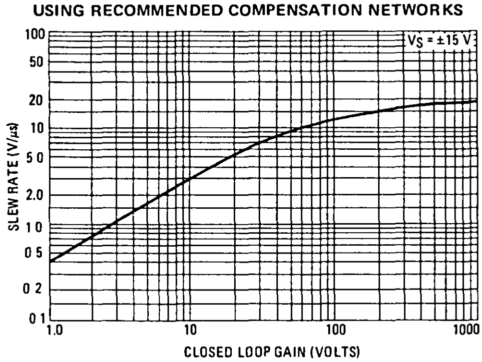
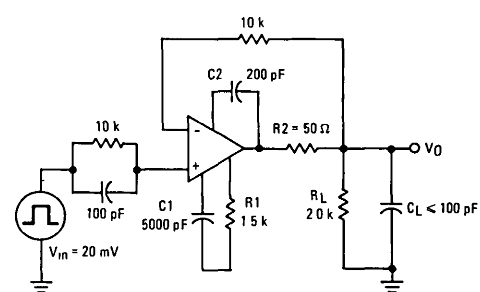


FIGURE 8 – TRANSIENT RESPONSE TEST CIRCUIT



ORDERING INFORMATION

Device	Temperature Range	Package
MC1712F	−55°C to +125°C	Ceramic Flat
MC1712G	−55°C to +125°C	Metal Can
MC1712L	−55°C to +125°C	Ceramic DIP
MC1712CF	0°C to +70°C	Ceramic Flat
MC1712CG	0°C to +70°C	Metal Can
MC1712CL	0°C to +70°C	Ceramic DIP
MC1712CP	0°C to +70°C	Plastic DIP

MC1712
MC1712C

WIDEBAND DC AMPLIFIER

. . designed for use as an operational amplifier utilizing operating characteristics as a function of the external feedback components.

- Open Loop Gain A_{VOL} = 3600 typical
- Low Temperature Drift – ±2.5 μV/°C
- Output Voltage Swing – ±5.3 V typical @ +12 V and -6 V Supplies
- Low Output Impedance – z_o = 200 ohms typical

WIDEBAND DC AMPLIFIER

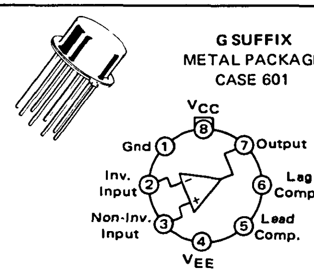
SILICON MONOLITHIC INTEGRATED CIRCUIT

3

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

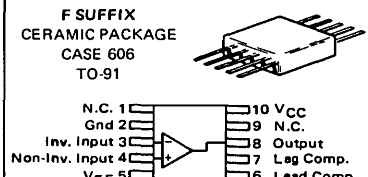
Rating	Symbol	Value	Unit
Power Supply Voltage (Total between V_{CC} and V_{EE} terminals)	$\|V_{CC}\| + \|V_{EE}\|$	21	Vdc
Input Differential Voltage Range	V_I	±5 0	Volts
Input Common Mode Range	V_{ICR}	+1.5 -6.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (Package Limitation)	P_D		
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Flat Ceramic Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Dual In-Line Ceramic Package		625	mW
Derate above T_A = +25°C		5 0	mW/°C
Operating Ambient Temperature Range MC1712 / MC1712C	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

G SUFFIX
METAL PACKAGE
CASE 601



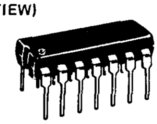
(TOP VIEW)

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

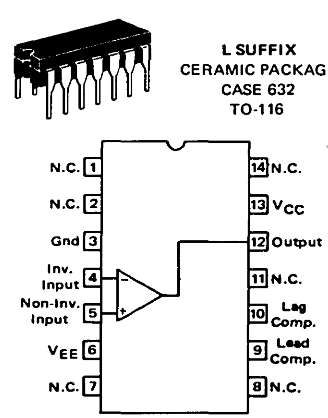


(TOP VIEW)

P SUFFIX
PLASTIC PACKAGE
CASE 646

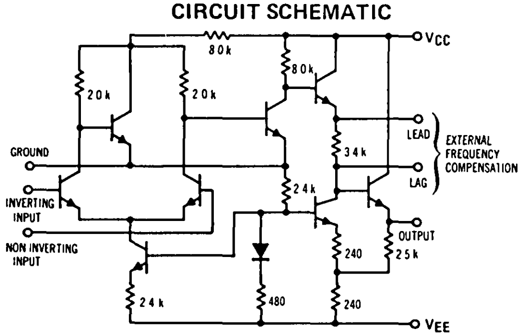


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



(TOP VIEW)

CIRCUIT SCHEMATIC



MC1712 ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	V_{CC} = 12 V, V_{EE} = -6.0 V			V_{CC} = 6.0 V, V_{EE} = -3.0 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 2$ kΩ)	V_{IO}	–	0.5	2.0	–	0.7	3.0	mV
Input Offset Current	I_{IO}	–	180	500	–	120	500	nA
Input Bias Current	I_{IB}	–	2.0	5.0	–	1.2	3.5	µA
Input Resistance	r_i	16	40	–	22	67	–	kΩ
Input Voltage Range	V_I	-4.0	–	+0.5	-1.5	–	+0.5	V
Common Mode Rejection Ratio ($R_S \le 2$ kΩ, f ≤ 1 kHz)	CMRR	80	100	–	80	100	–	dB
Large Signal Voltage Gain ($R_L \ge 100$ kΩ, V_{out} = ±5.0 V) ($R_L \ge 100$ kΩ, V_{out} = ±2.5 V)	A_{VOL}	 2000 –	 3600 –	 – –	 – 600	 – 900	 – –	
Output Resistance	r_o	–	200	500	–	300	700	Ω
Supply Current (V_{out} = 0)	I_D	–	5.0	6.7	–	2.1	3.3	mA
Power Consumption (V_{out} = 0)	P_C	–	90	120	–	19	30	mW
Transient Response (Unity-Gain) (C1 = 0.01 µF, R1 = 20 Ω, $R_L \le 100$ kΩ, V_{in} = 10 mV, $C_L \le 100$ pF) Rise Time Overshoot	 t_{TLH} OS	 – –	 25 10	 120 50	 – –	 – –	 – –	 ns %
Transient Response (x100 Gain) (C3 = 50 pF, $R_L \ge 100$ kΩ, V_{in} = 1 mV) Rise Time Overshoot	 t_{TLH} OS	 – –	 10 20	 30 40	 – –	 – –	 – –	 ns %

The following specifications apply for -55°C ≤ T_A ≤ +125°C:

Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 2$ kΩ)	V_{IO}	–	–	3.0	–	–	4.0	mV
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = 25°C to 125°C) (R_S = 50 Ω, T_A = 25°C to -55°C)	$\Delta V_{IO}/\Delta T$	 – –	 2.5 2.0	 10 10	 – –	 3.5 3.0	 15 15	 µV/°C µV/°C
Input Offset Current (T_A = +125°C) (T_A = -55°C)	I_{IO}	 – –	 80 400	 500 1500	 – –	 50 280	 500 1500	 nA nA
Average Temperature Coefficient of Input Offset Current (T_A = 25°C to +125°C) (T_A = 25°C to -55°C)	$\Delta I_{IO}/\Delta T$	 – –	 1.0 3.0	 5.0 16	 – –	 0.7 20	 4.0 13	 nA/°C nA/°C
Input Bias Current (T_A = -55°C)	I_{IB}	 –	 4.3	 10	 –	 2.6	 7.5	 µA
Input Resistance	r_i	6.0	–	–	8.0	–	–	kΩ
Common Mode Rejection Ratio ($R_S \le 2$ kΩ, f ≤ 1 kHz)	CMRR	70	95	–	70	95	–	dB
Supply Voltage Rejection Ratio (V_{CC} = 12 V, V_{EE} = -6.0 V to V_{CC} = 6.0 V, V_{EE} = -3.0 V, $R_S \le 2$ kΩ)	 PSRR	 –	 75	 200	 –	 75	 200	 µV/V
Large Signal Voltage Gain ($R_L \ge 100$ kΩ, V_{out} = ±5.0 V) ($R_L \ge 100$ kΩ, V_{out} = ±2.5 V)	A_{VOL}	 2000 –	 – –	 – –	 – 500	 – –	 – –	
Output Voltage Swing ($R_L \ge 100$ kΩ) ($R_L \ge 10$ kΩ)	V_O	 ±5.0 ±3.5	 ±5.3 ±4.0	 – –	 ±2.5 ±1.5	 ±2.7 ±2.0	 – –	 V V
Supply Current (T_A = +125°C, V_{out} = 0) (T_A = -55°C, V_{out} = 0)	I_D	 – –	 4.4 5.0	 6.7 7.5	 – –	 1.7 2.1	 3.3 3.9	 mA mA
Power Consumption (T_A = +125°C, V_{out} = 0) (T_A = -55°C, V_{out} = 0)	P_C	 – –	 80 90	 120 135	 – –	 15 19	 30 35	 mW mW

MC1712C ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	V_{CC} = 12 V, V_{EE} = -6.0 V Min	Typ	Max	V_{CC} = 6.0 V, V_{EE} = -3.0 V Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 2$ kΩ)	V_{IO}	–	1.5	5.0	–	1.7	6.0	mV
Input Offset Current	I_{IO}	–	0.5	2.0	–	0.3	2.0	µA
Input Bias Current	I_{IB}	–	2.5	7.5	–	1.5	5.0	µA
Input Resistance	r_i	10	32	–	16	55	–	kΩ
Input Voltage Range	V_I	-4.0	–	+0.5	-1.5	–	+0.5	V
Common Mode Rejection Ratio ($R_S \leq 2$ kΩ, f ≤ 1 kHz)	CMRR	70	92	–	70	92	–	dB
Large Signal Voltage Gain	A_{VOL}							
($R_L \geq 100$ kΩ, V_{out} = ±5.0 V)		2000	3400	–	–	–	–	
($R_L \geq 100$ kΩ, V_{out} = ±2.5 V)		–	–	–	500	800	–	
Output Resistance	r_o	–	200	600	–	300	800	Ω
Supply Current (V_{out} = 0)	I_D	–	5.0	6.7	–	2.1	3.3	mA
Power Consumption (V_{out} = 0)	P_C	–	90	120	–	19	30	mW
Transient Response (Unity-Gain) (C1 = 0.01 µF, R_I = 20 Ω, $R_L \leq 100$ kΩ, V_{in} = 10 mV, $C_L \leq 100$ pF)								
Rise Time	t_{TLH}	–	25	120	–	–	–	ns
Overshoot	OS	–	10	50	–	–	–	%
Transient Response (x100 Gain) (C3 = 50 pF, $R_L \geq 100$ kΩ, V_{in} = 1 mV)								
Rise Time	t_{TLH}	–	10	30	–	–	–	ns
Overshoot	OS	–	20	40	–	–	–	%

The following specifications apply for 0°C ≤ T_A ≤ +70°C

Characteristic	Symbol	V_{CC} = 12 V, V_{EE} = -6.0 V Min	Typ	Max	V_{CC} = 6.0 V, V_{EE} = -3.0 V Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 2$ kΩ)	V_{IO}	–	–	6.5	–	–	7.5	mV
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = +70°C to 0°C)	$\Delta V_{IO}/\Delta T$	–	5.0	20	–	7.5	25	µV/°C
Input Offset Current	I_{IO}	–	–	2.5	–	–	2.5	µA
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							
(T_A = 25°C to +70°C)		–	4.0	10	–	3.0	8.0	nA/°C
(T_A = 25°C to 0°C)		–	6.0	20	–	5.5	18	nA/°C
Input Bias Current (T_A = 0°C)	I_{IB}	–	4.0	12	–	2.7	8	µA
Input Resistance	r_i	6.0	18	–	9.0	27	–	kΩ
Common Mode Rejection Ratio ($R_S \leq 2$ kΩ, f ≤ 1 kHz)	CMRR	6.5	86	–	65	86	–	dB
Supply Voltage Rejection Ratio (V_{CC} = 12 V, V_{EE} = -6.0 V to V_{CC} = 6.0 V, V_{EE} = -3.0 V, $R_S \leq 2$ kΩ)	PSRR	–	90	300	–	90	300	µV/V
Large Signal Voltage Gain	A_{VOL}							
($R_L \geq 100$ kΩ, V_{out} = ±5.0 V)		1500	–	–	–	–	–	
($R_L \geq 100$ kΩ, V_{out} = ±2.5 V)		–	–	–	400	–	–	
Output Voltage Swing	V_O							
($R_L \geq 100$ kΩ)		±5.0	±5.3	–	±2.5	±2.7	–	V
($R_L \geq 10$ kΩ)		±3.5	±4.0	–	±1.5	±2.0	–	V
Supply Current (V_{out} = 0)	I_D	–	5.0	7.0	–	2.1	3.9	mA
Power Consumption (V_{out} = 0)	P_C	–	90	125	–	19	35	mW

3

TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = 12 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C)

FIGURE 1 – OPEN LOOP GAIN versus POWER SUPPLY VARIATIONS

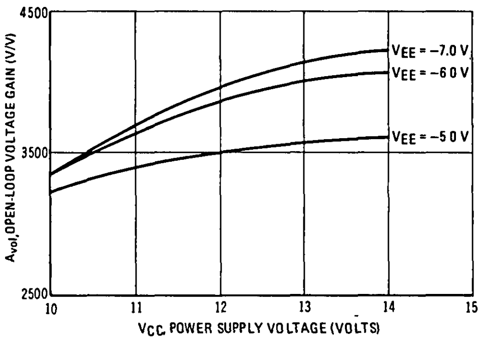


FIGURE 2 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

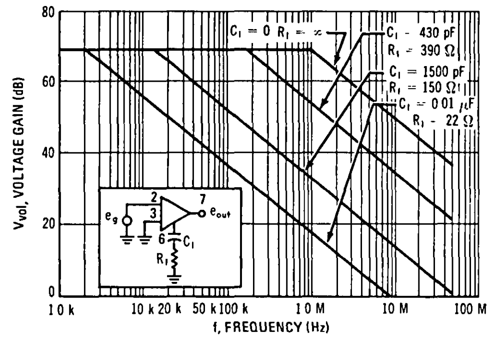


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

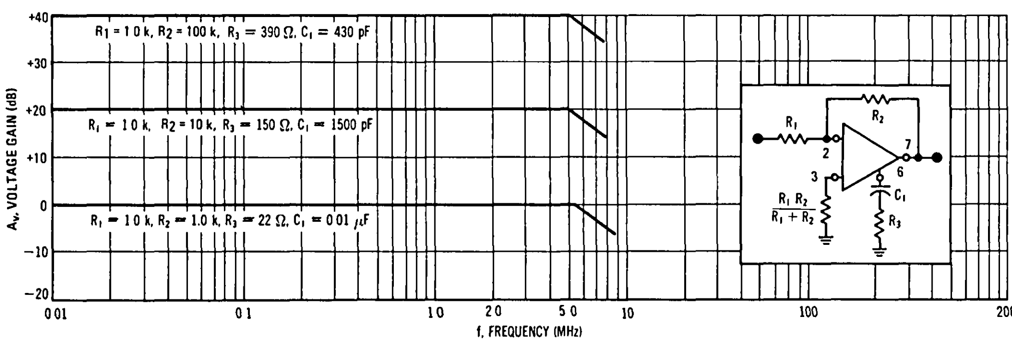


FIGURE 4 – MAXIMUM OUTPUT SWING versus FREQUENCY

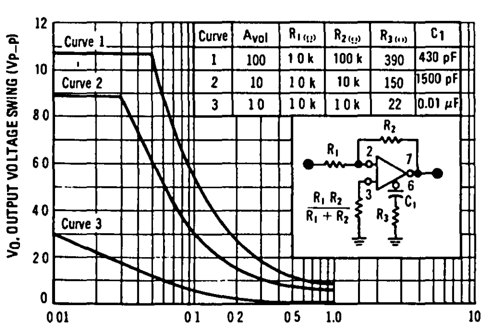
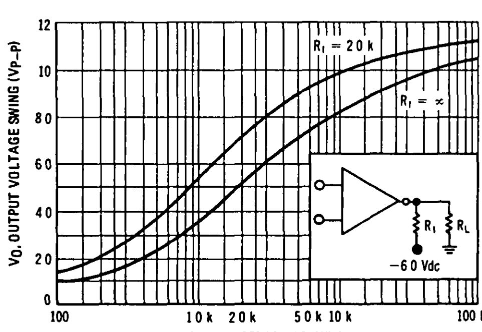


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – INPUT BIAS CURRENT versus TEMPERATURE

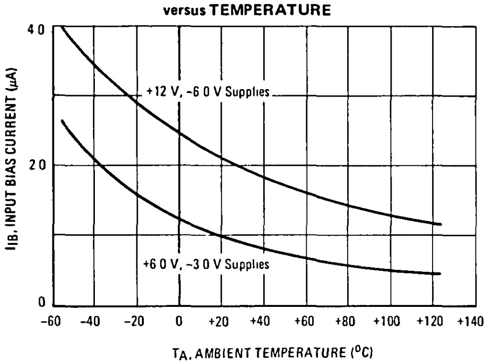


FIGURE 7 – INPUT OFFSET CURRENT versus TEMPERATURE

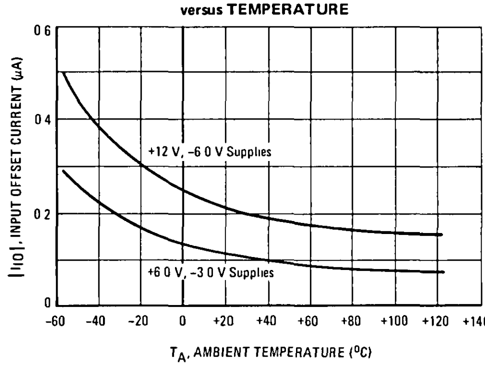


FIGURE 8 – INPUT OFFSET VOLTAGE versus TEMPERATURE

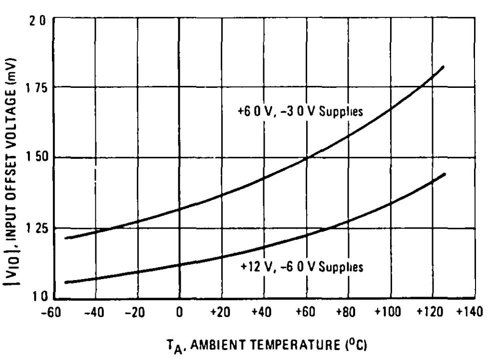
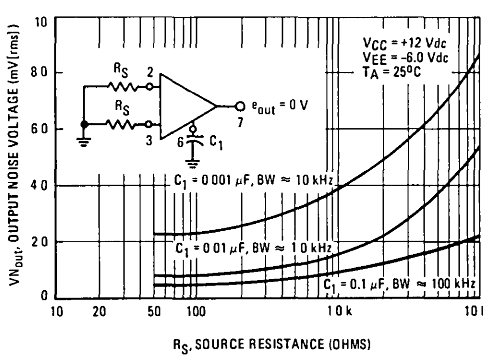


FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



See last page of data sheet for ordering information.

MC1741, MC1741C
MC1741N, MC1741NC

OPERATIONAL AMPLIFIER
SILICON MONOLITHIC
INTEGRATED CIRCUIT

INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered — N Suffix

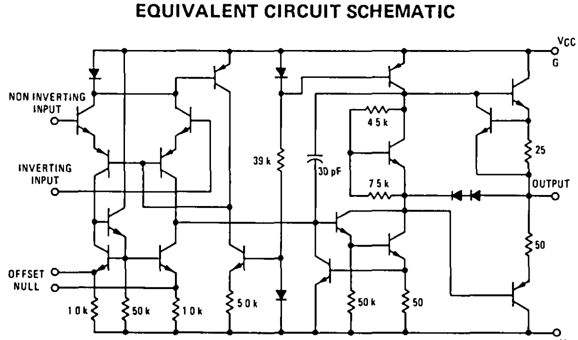
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1741C	MC1741	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	°C
Storage Temperature Range Metal, Flat and Ceramic Packages Plastic Packages	T_{stg}	 -65 to +150 -55 to +125		°C
Junction Temperature Range Metal and Ceramic Packages Plastic Packages	T_J	 175 150		°C

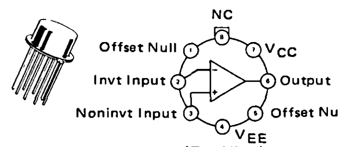
Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage

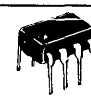
Note 2 Supply voltage equal to or less than 15 V

EQUIVALENT CIRCUIT SCHEMATIC



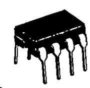
G SUFFIX
METAL PACKAGE
CASE 601

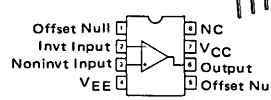


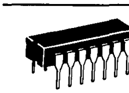


P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1741C,MC1741NC)

U SUFFIX
CERAMIC PACKAGE
CASE 693

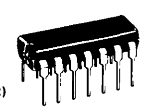


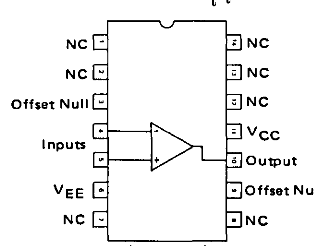




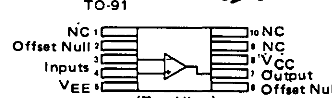
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1741C,MC1741NC)





F SUFFIX
CERAMIC PACKAGE
CASE 606-04
TO-91



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC1741 Min	MC1741 Typ	MC1741 Max	MC1741C Min	MC1741C Typ	MC1741C Max	Unit
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L ≥ 2.0 k)	A_v	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing	V_O							V
(R_L ≥ 10 k)		±12	±14	–	±12	±14	–	
(R_L ≥ 2 k)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	mA
Supply Current	I_D	–	1.7	2.8	–	1.7	2.8	mA
Power Consumption	P_C	–	50	85	–	50	85	mW
Transient Response (Unity Gain — Non-Inverting)								
(V_I = 20 mV, R_L ≥ 2 k, C_L ≤ 100 pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, R_L ≥ 2 k, C_L ≤ 100 pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, R_L ≥ 2 k, C_L ≤ 100 pF) Slew Rate	SR	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC1741 Min	MC1741 Typ	MC1741 Max	MC1741C Min	MC1741C Typ	MC1741C Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = 125°C)		–	7.0	200	–	–	–	
(T_A = −55°C)		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
(T_A = 125°C)		–	30	500	–	–	–	
(T_A = −55°C)		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing	V_O							V
(R_L ≥ 10 k)		±12	±14	–	–	–	–	
(R_L ≥ 2 k)		±10	±13	–	±10	±13	–	
Large Signal Voltage Gain (R_L ≥ 2 k, V_{out} = ±10 V)	A_v	25	–	–	15	–	–	V/mV
Supply Currents	I_D							mA
(T_A = 125°C)		–	1.5	2.5	–	–	–	
(T_A = −55°C)		–	2.0	3.3	–	–	–	
Power Consumption (T_A = +125°C)	P_C	–	45	75	–	–	–	mW
(T_A = −55°C)		–	60	100	–	–	–	

*T_{high} = 125°C for MC1741 and 70°C for MC1741C
T_{low} = −55°C for MC1741 and 0°C for MC1741C

NOISE CHARACTERISTICS (Applies for MC1741N and MC1741NC only, V_{CC} = 15 V, V_{EE} = -15 V, T_A = +25°C)

Characteristic	Symbol	MC1741N			MC1741NC			Unit
		Min	Typ	Max	Min	Typ	Max	
Burst Noise (Popcorn Noise) (BW = 1.0 Hz to 1.0 kHz, t = 10 s, R_S = 100 k) (Input Referenced)	E_n	–	–	20	–	–	20	µV/peak

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

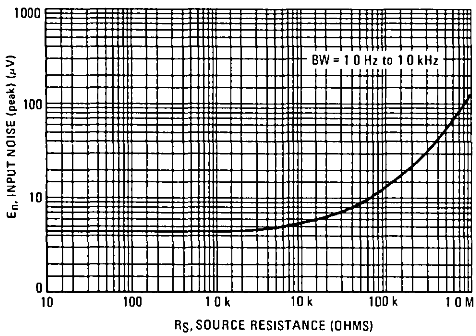


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

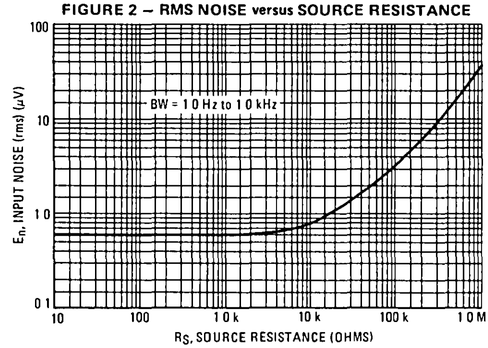


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

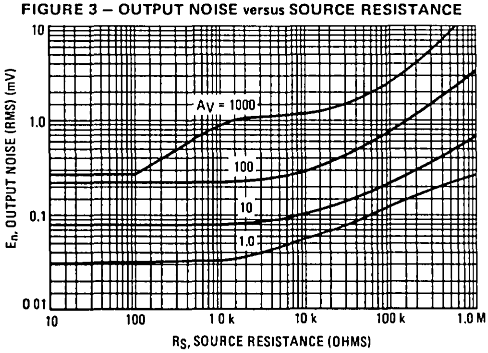


FIGURE 4 – SPECTRAL NOISE DENSITY

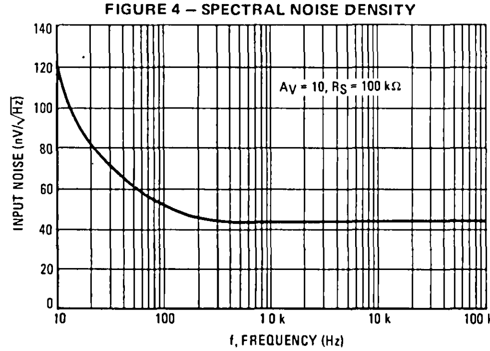
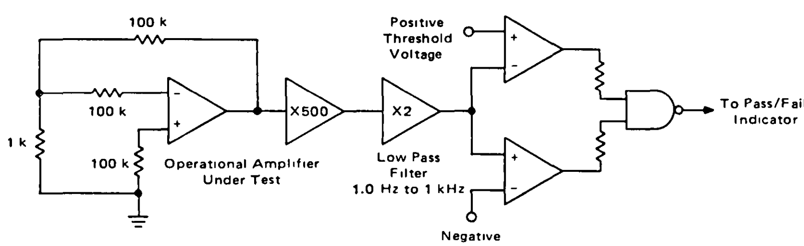


FIGURE 5 – BURST NOISE TEST CIRCUIT (N Suffixed Devices Only)



For applications where low noise performance is essential, selected devices denoted by an N suffix are offered These units have been 100% tested for burst noise pulses on a special noise test system. Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing

The test time employed is 10 seconds and the 20 µV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 6 — POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

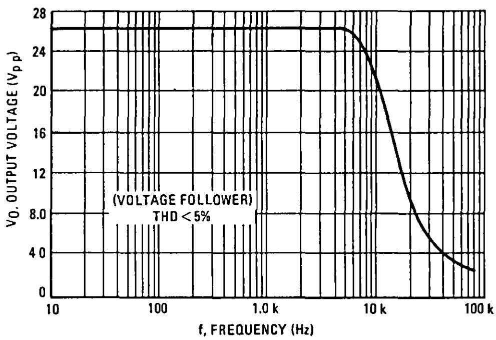


FIGURE 7 — OPEN LOOP FREQUENCY RESPONSE

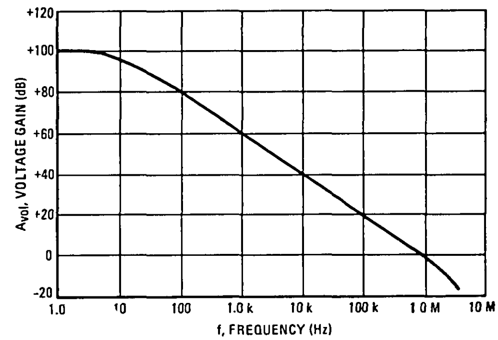


FIGURE 8 — POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

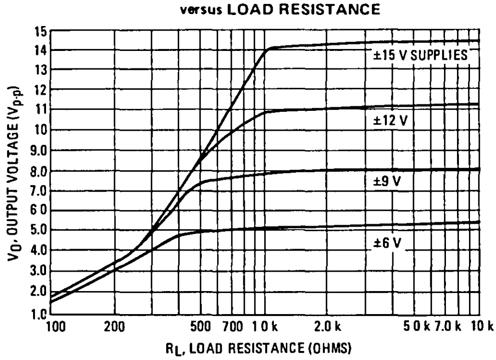


FIGURE 9 — NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

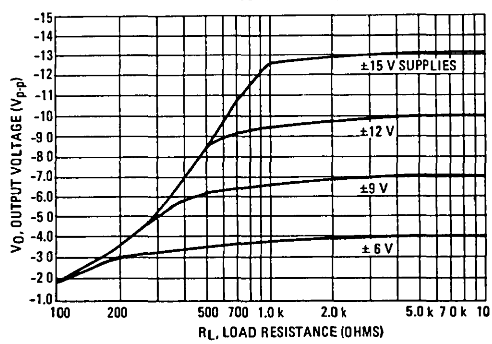


FIGURE 10 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

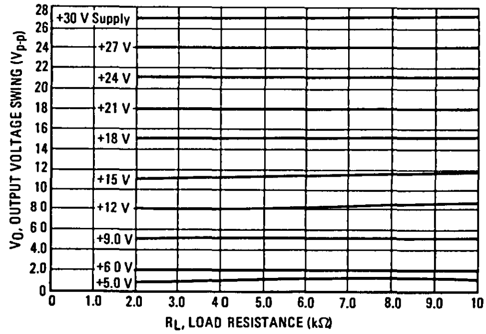


FIGURE 11 — SINGLE SUPPLY INVERTING AMPLIFIER

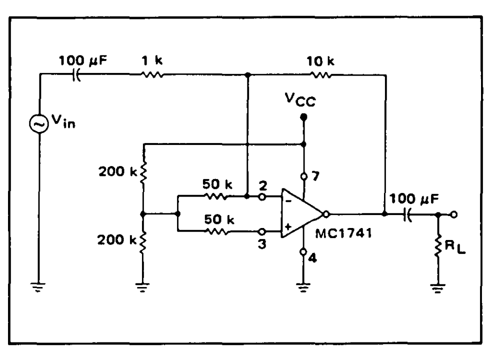


FIGURE 12 – NON-INVERTING PULSE RESPONSE

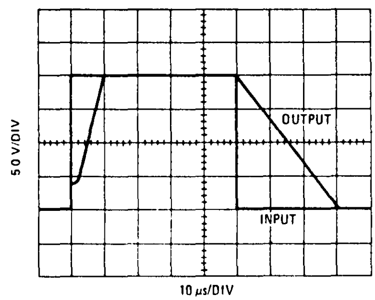


FIGURE 13 – TRANSIENT RESPONSE TEST CIRCUIT

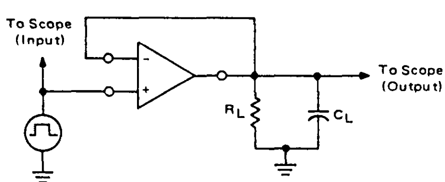
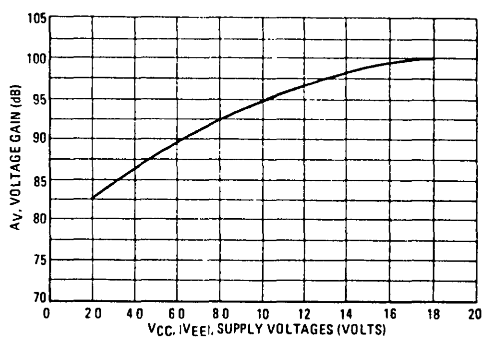


FIGURE 14 – OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1741CF,NCF	—	0°C to +70°C	Ceramic Flat
MC1741CG	LM741CD, μA741HC	0°C to +70°C	Metal Can
MC1741CL	LM741CD, μA741DC	0°C to +70°C	Ceramic DIP
MC1741CP1	LM741CN, μA741TC	0°C to +70°C	Plastic DIP
MC1741CP2, NCP1, NCP2	—	0°C to +70°C	Plastic DIP
MC1741CU,NCU	—	0°C to +70°C	Ceramic DIP
MC1741F,NF	—	−55°C to +125°C	Ceramic Flat
MC1741G,NG	—	−55°C to +125°C	Metal Can
MC1741L,NL	—	−55°C to +125°C	Ceramic DIP
MC1741U,NU	—	−55°C to +125°C	Ceramic DIP
MC1741NCG	—	0°C to +70°C	Metal Can
MC1741NCL	—	0°C to +70°C	Ceramic DIP

ORDERING INFORMATION

Device	Temperature Range	Package
MC1741SG	−55°C to +125°C	Metal Can
MC1741SU	−55°C to +125°C	Ceramic DIP
MC1741SCG	0°C to +70°C	Metal Can
MC1741SCP1	0°C to +70°C	Plastic DIP
MC1741SCU	0°C to +70°C	Ceramic DIP

MC1741S
MC1741SC

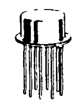
HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIER

The MC1741S/MC1741SC is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1741 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D-to-A converters due to its fast settling time and high slew rate.

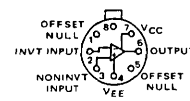
- High Slew Rate – 10 V/μs Guaranteed Minimum (for unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

OPERATIONAL AMPLIFIER

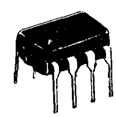
SILICON MONOLITHIC INTEGRATED CIRCUIT



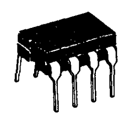
G SUFFIX
METAL PACKAGE
CASE 601-02



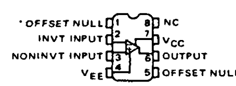
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

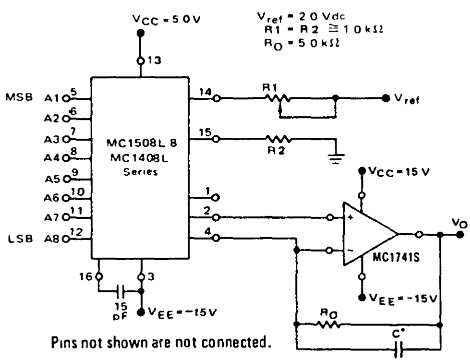


U SUFFIX
CERAMIC PACKAGE
CASE 693



(Top View)

TYPICAL APPLICATION OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Pins not shown are not connected.

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

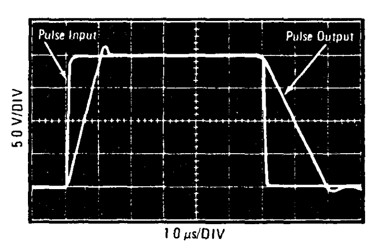
Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

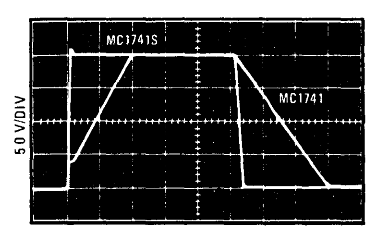
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\,V}{1\,k}(5\,k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\,V\left[\frac{255}{256}\right] = 9.961\,V$$

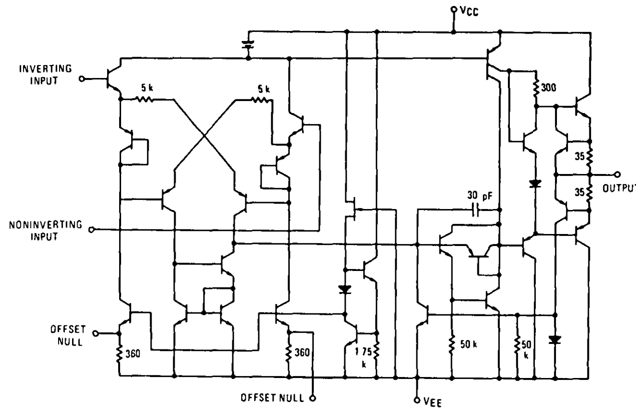
MC1741S LARGE-SIGNAL TRANSIENT RESPONSE



STANDARD MC1741 versus MC1741S RESPONSE COMPARISON



CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value MC1741SC	Value MC1741S	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Differential Input Signal Voltage	V_{ID}	±30		Volts
Common-Mode Input Voltage Swing (See Note 1)	V_{ICR}	±15		Volts
Output Short-Circuit Duration (See Note 2)	t_s	Continuous		
Power Dissipation (Package Limitation)	P_D			
Metal Package		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Plastic Dual In-Line Package		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	-55 to +125	°C
Storage Temperature Range	T_{stg}			°C
Metal Package		-65 to +150		
Plastic Package		-55 to +125		

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

FIGURE 1 – OFFSET ADJUST CIRCUIT

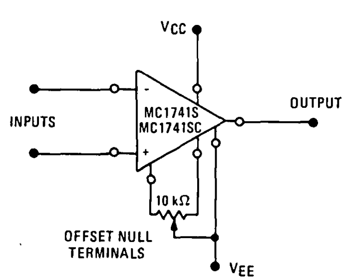
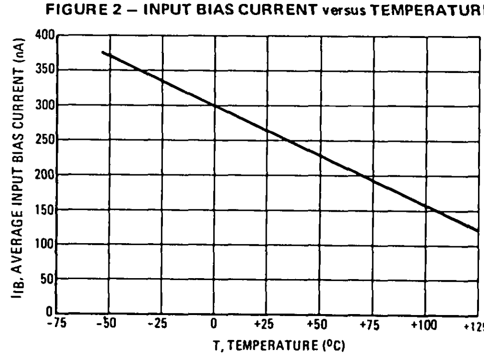


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1741S Min	MC1741S Typ	MC1741S Max	MC1741SC Min	MC1741SC Typ	MC1741SC Max	Unit
Power Bandwidth (See Figure 3)	BW_P							kHz
A_V = 1, R_L = 2 0 kΩ, THD = 5%, V_O = 20 V(p-p)		150	200	–	150	200	–	
Large-Signal Transient Response								
Slew Rate (Figures 10 and 11)	SR							
V(−) to V(+)		10	20	–	10	20	–	V/µs
V(+) to V(−)		10	12	–	10	12	–	
Settling Time (Figures 10 and 11) (to within 0 1%)	t_{setlg}	–	3 0	–	–	3 0	–	µs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8)								
Rise Time	t_{TLH}	–	0.25	–	–	0.25	–	µs
Fall Time	t_{THL}	–	0.25	–	–	0.25	–	µs
Propagation Delay Time	t_{PLH}, t_{PHL}	–	0 25	–	–	0.25	–	µs
Overshoot	OS	–	20	–	–	20	–	%
Short-Circuit Output Currents	I_{OS}	±10	–	±45	±10	–	±45	mA
Open-Loop Voltage Gain (R_L - 2 0 kΩ) (See Figure 4)	A_{vol}							–
V_O - ±10 V, T_A = +25°C		50,000	200,000	–	20,000	100,000	–	
V_O = ±10 V, T_A = T_{low}* to T_{high}*		25,000	–	–	15,000	–	–	
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0 3	1.0	–	0 3	1 0	–	MΩ
Output Voltage Swing	V_O							V_{pk}
R_L = 10 kΩ, T_A = T_{low} to T_{high} (MC1741S only)		±12	±14	–	±12	±14	–	
R_L = 2.0 kΩ, T_A = +25°C		±10	±13	–	±10	±13	–	
R_L = 2 0 kΩ, T_A = T_{low} to T_{high}		±10	–	–	±10	–	–	
Input Common-Mode Voltage Range T_A = T_{low} to T_{high} (MC1741S)	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz) T_A = T_{low} to T_{high} (MC1741S)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2)	I_{IB}							nA
T_A = +25°C and T_{high}		–	200	500	–	200	500	
T_A = T_{low}		–	500	1500	–	–	800	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C and T_{high}		–	30	200	–	30	200	
T_A = T_{low}		–	–	500	–	–	300	
Input Offset Voltage (R_S = ⩽10 kΩ)	$\|V_{IO}\|$							mV
T_A = +25°C		–	1 0	5 0	–	2 0	6.0	
T_A = T_{low} to T_{high}		–	–	6 0	–	–	7.5	
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0) T_A = T_{low} to T_{high}	P_C	–	50	85	–	50	85	mW
Positive Voltage Supply Sensitivity (V_{EE} constant) T_A = T_{low} to T_{high} on MC1741S	PSS+	–	2 0	100	–	2 0	150	µV/V
Negative Voltage Supply Sensitivity (V_{CC} constant) T_A = T_{low} to T_{high} on MC1741S	PSS−	–	10	150	–	10	150	µV/V

*T_{low} = 0 for MC1741SC
= −55 °C for MC1741S

T_{high} = +70°C for MC1741SC
= +125 °C for MC1741S

3

3

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

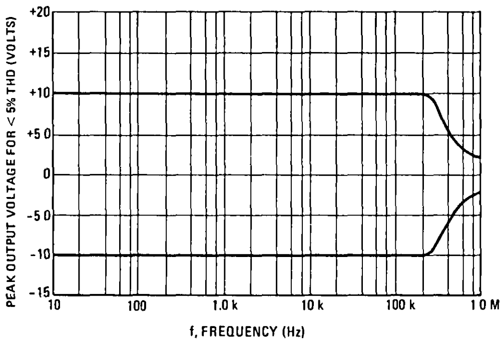


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

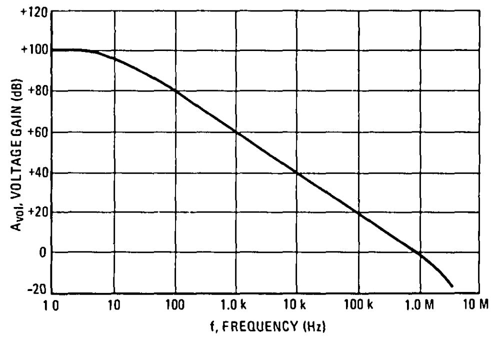


FIGURE 5 – NOISE versus FREQUENCY

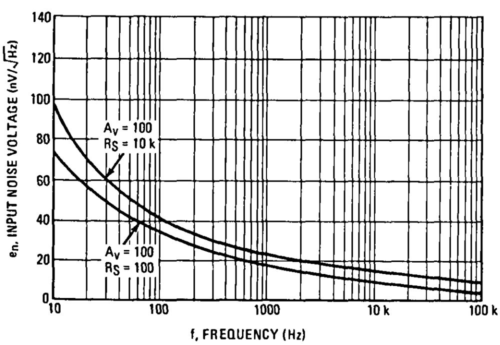


FIGURE 6 – OUTPUT NOISE versus SOURCE RESISTANCE

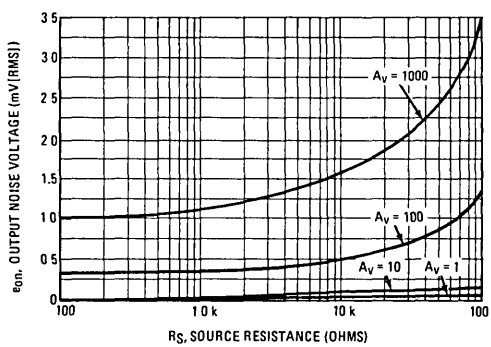


FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

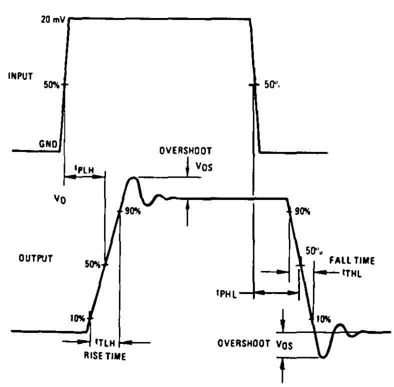
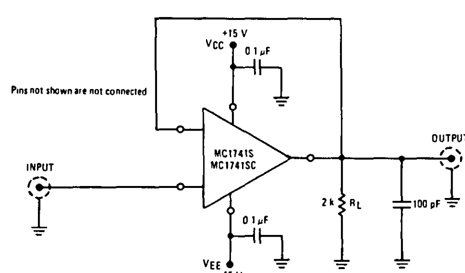


FIGURE 8 – SMALL-SIGNAL TRANSIENT RESPONSE TEST CIRCUIT



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C *unless otherwise noted.*)

FIGURE 9 — POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

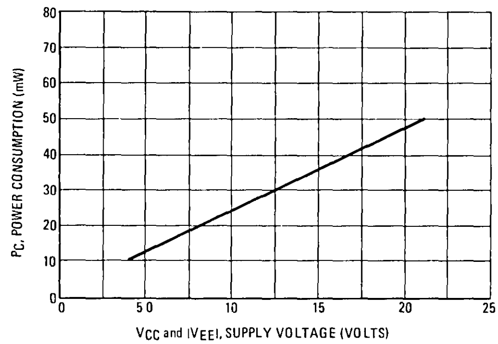


FIGURE 10 — LARGE-SIGNAL TRANSIENT WAVEFORMS

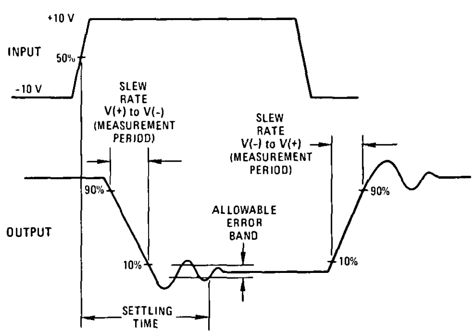
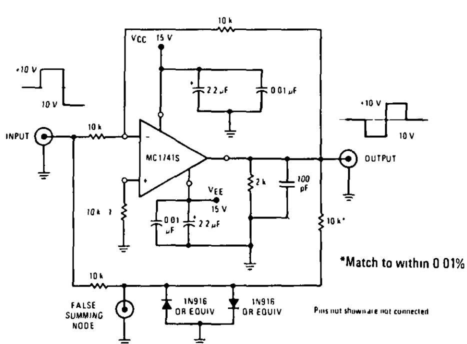


FIGURE 11 — SETTLING TIME AND SLEW RATE TEST CIRCUIT



SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time

x = amplifier settling time (to be determined)

y = false summing junction settling time

z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1741S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

3

FIGURE 12 – WAVEFORM AT FALSE SUMMING NODE

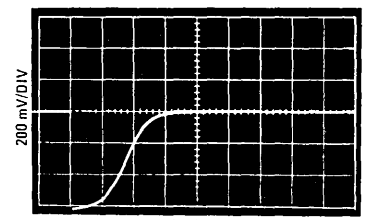
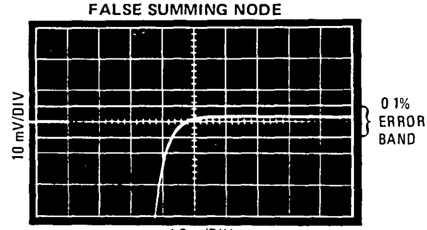
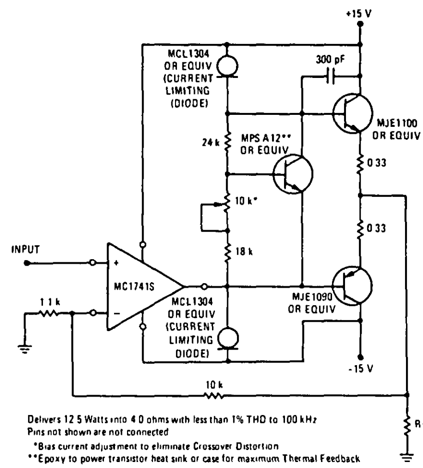


FIGURE 13 – EXPANDED WAVEFORM AT FALSE SUMMING NODE



TYPICAL APPLICATION

FIGURE 14 – 12.5-WATT WIDEBAND POWER AMPLIFIER



Delivers 12 5 Watts into 4 0 ohms with less than 1% THD to 100 kHz
Pins not shown are not connected
*Bias current adjustment to eliminate Crossover Distortion
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback

ORDERING INFORMATION

Device	Temperature Range	Package
MC1747F	−55°C to +125°C	Ceramic Flat
MC1747G	−55°C to +125°C	Metal Can
MC1747L	−55°C to +125°C	Ceramic DIP
MC1747CF	0°C to +75°C	Ceramic Flat
MC1747CG	0°C to +75°C	Metal Can
MC1747CL	0°C to +75°C	Ceramic DIP
MC1747CP2	0°C to +75°C	Plastic DIP

MC1747
MC1747C

3

DUAL MC1741
INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIER

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally, electrically, and pin-for-pin equivalent to the μA747 and μA747C respectively.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Offset Voltage Null Capability

(DUAL MC1741)

DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 – HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER

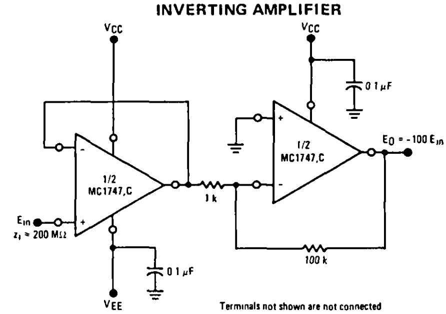
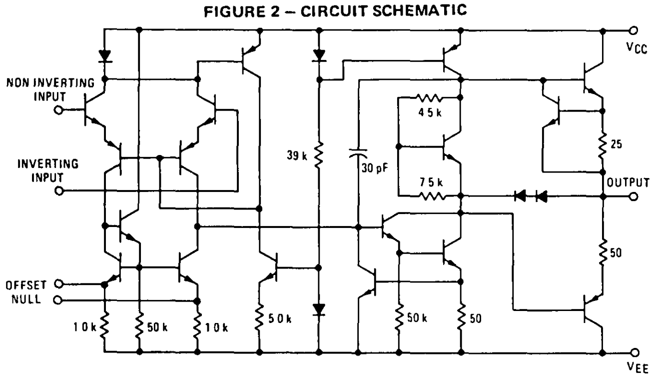
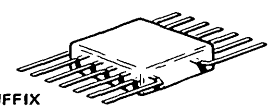


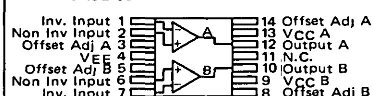
FIGURE 2 – CIRCUIT SCHEMATIC

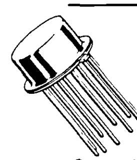


Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent right of Motorola Inc. or others.

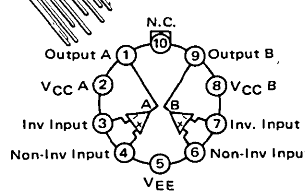


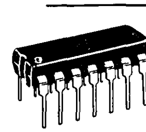
F SUFFIX
CERAMIC PACKAGE
CASE 607



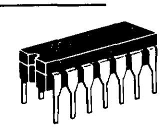


G SUFFIX
METAL PACKAGE
CASE 603

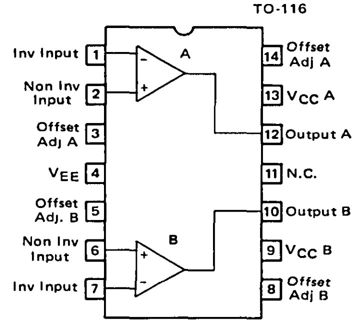




P2 SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC1747	MC1747C	Unit
Power Supply Voltages	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Signal Voltage ①	V_{ID}	± 30		Volts
Common-Mode Input Swing Voltage ②	V_{ICR}	± 15		Volts
Output Short-Circuit Duration	t_{OS}	Continuous		
Voltage (Measurement between Offset Null and V_{EE})		± 0.5		Volts
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C
Junction Temperature Ceramic and Metal Package Plastic Package	T_J	 175 150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristics	Symbol	MC1747 Min	MC1747 Typ	MC1747 Max	MC1747C Min	MC1747C Typ	MC1747C Max	Unit
Input Bias Current	I_{IB}							nAdc
T_A = +25°C		–	80	500	–	80	500	
$T_A = T_{high}$ ③		–	30	500	–	30	800	
$T_A = T_{low}$ ③		–	300	1500	–	30	800	
Input Offset Current	I_{IO}							nAdc
T_A = +25°C		–	20	200	–	20	200	
$T_A = T_{high}$		–	7.0	200	–	7.0	300	
$T_A = T_{low}$		–	85	500	–	7.0	300	
Input Offset Voltage ($R_S \leq$ 10 kΩ)	V_{IO}							mVdc
T_A = +25°C		–	1.0	5.0	–	1.0	6.0	
$T_A = T_{low}$ to T_{high}		–	1.0	6.0	–	1.0	7.5	
Offset Voltage Adjustment Range		–	± 15	–	–	± 15	–	mV
Differential Input Impedance (Open-loop, f = 20 Hz)								
Parallel Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Parallel Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Common-Mode Input Voltage Swing	V_{ICR}							Volts
$T_{low} \leq T_A \leq T_{high}$		± 12	± 13	–	± 12	± 13	–	
Common-Mode Rejection Ratio (R_S = 10 kΩ)	CMRR							dB
$T_{low} \leq T_A \leq T_{high}$		70	90	–	70	90	–	
Open-Loop Voltage Gain	A_{vol}							Volts
T_A = +25°C } (V_O = ±10 V, R_L = 2.0 kΩ)		50,000	200,000	–	25,000	200,000	–	
$T_A = T_{low}$ to T_{high} } (V_O = ±10 V, R_L = 2.0 kΩ)		25,000	–	–	15,000	–	–	
Transient Response (Unity Gain)								
(V_{in} = 20 mV, R_L = 2.0 kΩ, $C_L \leq$ 100 pF)								
Rise Time	t_{PLH}	–	0.3	–	–	0.3	–	µs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate (Unity Gain)	SR	–	0.5	–	–	0.5	–	V/µs
Output Impedance	z_o	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{OS}	–	25	–	–	25	–	mAdc
Channel Separation		–	120	–	–	120	–	dB
Output Voltage Swing ($T_{low} \leq T_A \leq T_{high}$)	V_{OR}							V_{pk}
R_L = 10 kΩ		± 12	± 14	–	± 12	± 14	–	
R_L = 2.0 kΩ		± 10	± 13	–	± 10	± 13	–	
Power Supply Sensitivity (T_{low} to T_{high})								µV/V
V_{EE} = Constant, $R_S \leq$ 10 kΩ	PSS+	–	30	150	–	30	150	
V_{CC} = Constant, $R_S \leq$ 10 kΩ	PSS-	–	30	150	–	30	150	
Power Supply Current (each amplifier)	I_{CC}, I_{EE}							mAdc
T_A = +25°C		–	1.7	2.8	–	1.7	2.8	
$T_A = T_{low}$		–	2.0	3.3	–	2.0	3.3	
$T_A = T_{high}$		–	1.5	2.5	–	2.0	3.3	
DC Power Consumption (each amplifier)	P_C							mW
T_A = +25°C		–	50	85	–	50	85	
$T_A = T_{low}$		–	60	100	–	60	100	
$T_A = T_{high}$		–	45	75	–	60	100	

① For supply voltages of less than ± 15 V, the maximum differential input voltage is equal to ± (V_{CC} + $|V_{EE}|$).
② For supply voltages of less than ± 15 V, the maximum input voltage is equal to the supply voltage (+V_{CC}, -$|V_{EE}|$).
③ T_{low}: 0°C for MC1747CL
-55°C for MC1747L
T_{high}: +75°C for MC1747CL
+125°C for MC1747L

FIGURE 3 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR TEST CIRCUIT

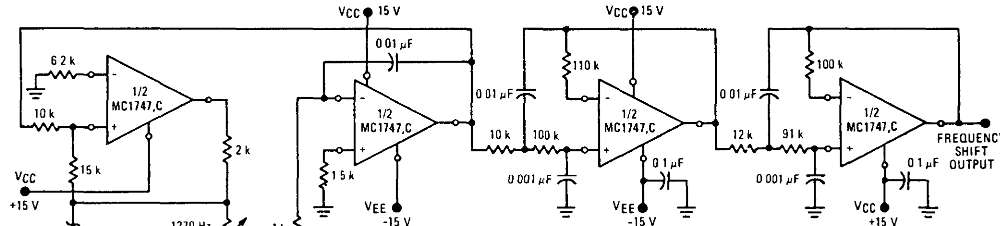
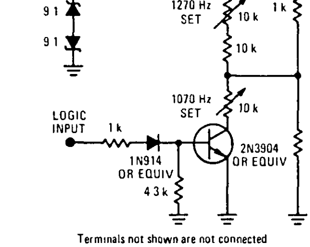
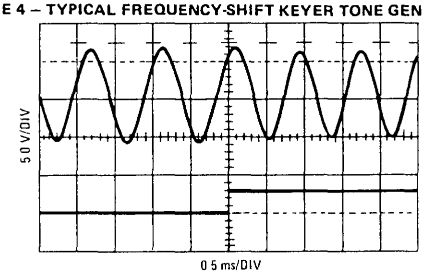



FIGURE 4 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE

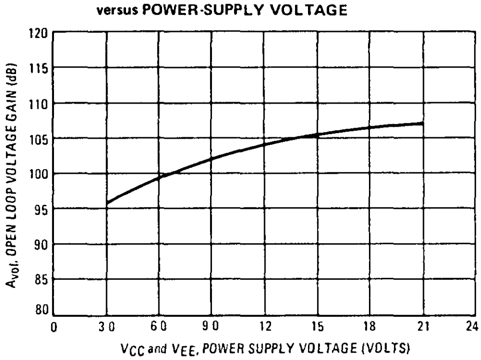


FIGURE 6 – OPEN-LOOP FREQUENCY RESPONSE

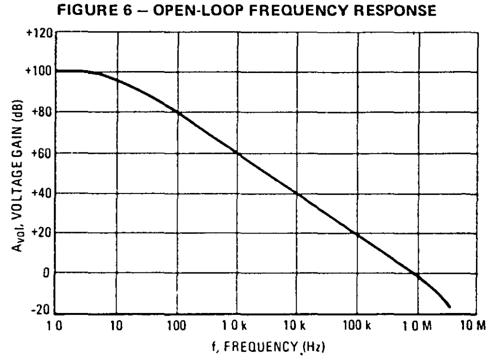


FIGURE 7 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

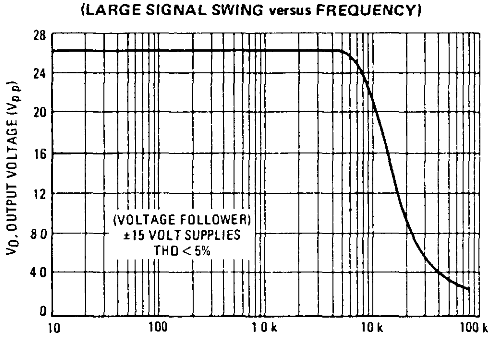
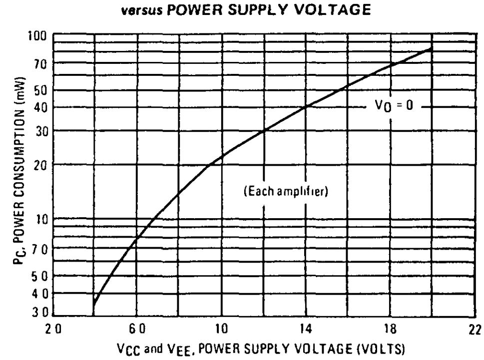


FIGURE 8 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

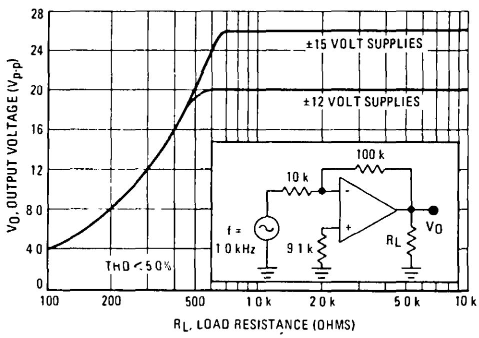
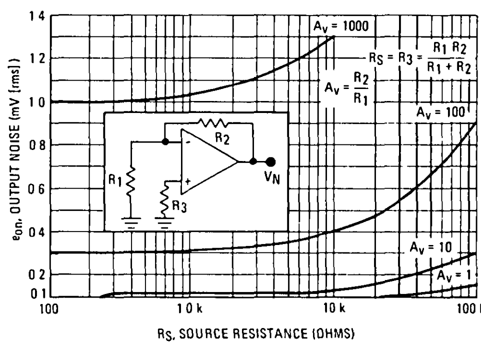


FIGURE 10 – OUTPUT NOISE versus SOURCE RESISTANCE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1748G	−55°C to +125°C	Metal Can
MC1748U	−55°C to +125°C	Ceramic DIP
MC1748CG	0°C to +70°C	Metal Can
MC1748CP1	0°C to +70°C	Plastic DIP
MC1748CU	0°C to +70°C	Ceramic DIP

MC1748
MC1748C

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

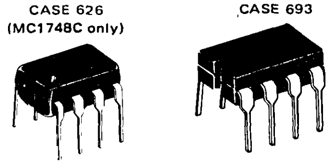
- Noncompensated MC1741
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

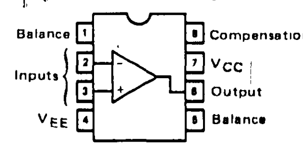
OPERATIONAL AMPLIFIER

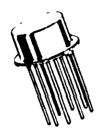
SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1748C only)

U SUFFIX
CERAMIC PACKAGE
CASE 693







G SUFFIX
METAL PACKAGE
CASE 601

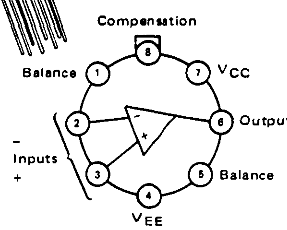
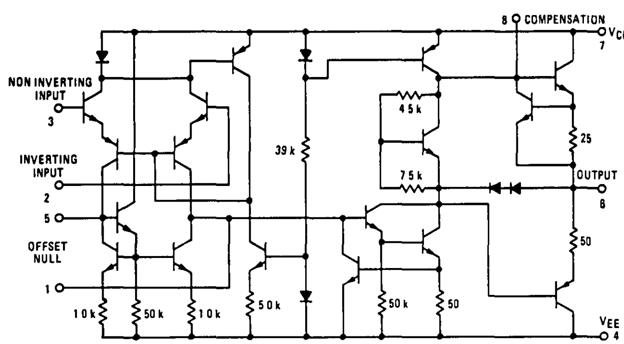


FIGURE 1 — CIRCUIT SCHEMATIC



TYPICAL COMPENSATION CIRCUITS

FIGURE 2 — OFFSET ADJUST AND FREQUENCY COMPENSATION

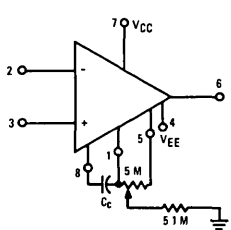


FIGURE 3 — SINGLE-POLE COMPENSATION

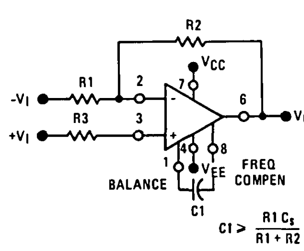
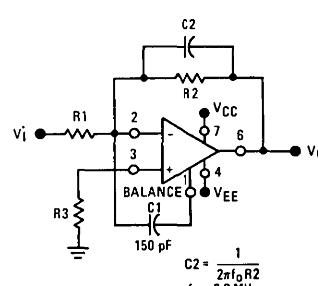


FIGURE 4 — FEEDFORWARD COMPENSATION



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1748	MC1748C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{in}	±30		Volts
Common-Mode Input Swing ①	V_{ICR}	±15		Volts
Output Short Circuit Duration	t_s	Continuous		
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4 6		mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1748			MC1748C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_{IB}							µAdc
T_A = +25°C		–	0 08	0 5	–	0 08	0 5	
T_A = T_{low} to T_{high} ②		–	0 3	1.5	–	–	0 8	
Input Offset Current	$\vert I_{IO}\vert$							µAdc
T_A = +25°C		–	0 02	0 2	–	0 02	0 2	
T_A = T_{low} to T_{high}		–	0 08	0 5	–	–	0 3	
Input Offset Voltage ($R_S \leq$ 10 k Ω)	$\vert V_{IO}\vert$							mVdc
T_A = +25°C		–	1.0	5 0	–	1.0	6.0	
T_A = T_{low} to T_{high}		–	–	6 0	–	–	7 5	
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	0.3	2.0	–	0 3	2 0	–	Megohm
Parallel Input Capacitance	C_p	–	1.4	–	–	1 4	–	pF
Common-Mode Input Impedance (f - 20 Hz)	z_{in}	–	200	–	–	200		Megohms
Common-Mode Input Voltage Swing	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	70	90	–	70	90	–	dB
Open-Loop Voltage Gain, (V_o = ±10 V, R_L = 2 0 k ohms)	A_{vol}							V/V
T_A = +25°C		50,000	200,000	–	20,000	200,000	–	
T_A = T_{low} to T_{high}		25,000	–	–	15,000	–	–	
Step Response (V_{in} = 20 mV, C_c = 30 pF, R_L = 2 kΩ, C_L = 100 pF)								
Rise Time	t_r	–	0 3	–	–	0 3	–	µs
Overshoot Percentage		–	5 0	–	–	5 0	–	%
Slew Rate	dV_{out}/dt	–	0 8	–	–	0 8	–	V/µs
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{sc}	–	25	–	–	25	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±12	±14	–	±12	±14	–	Vpk
R_L = 2 k ohms (T_A = T_{low} to t_{high})		±10	±13	–	±10	±13	–	
Power Supply Sensitivity								µV/V
V_{EE} = constant, $R_s \leq$ 10 k ohms	S+	–	30	150	–	30	150	
V_{CC} = constant, $R_s \leq$ 10 k ohms	S-	–	30	150	–	30	150	
Power Supply Current	I_D^+	–	1 67	2.83	–	1.67	2.83	mAdc
	I_D^-	–	1 67	2.83	–	1 67	2.83	
DC Quiescent Power Dissipation	P_D							mW
(V_o = 0)		–	50	85	–	50	85	

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.

② T_{low} · 0°C for MC1748C
-55°C for MC1748
T_{high} · +70° for MC1748C
+125°C for MC1748

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 — MINIMUM INPUT VOLTAGE RANGE

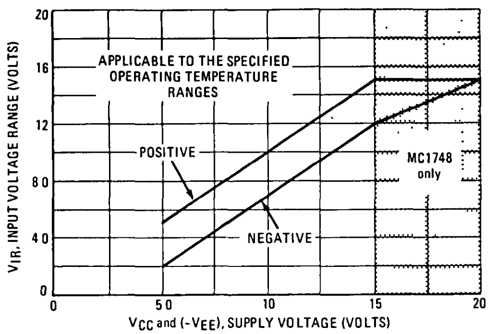


FIGURE 6 — MINIMUM OUTPUT VOLTAGE SWING

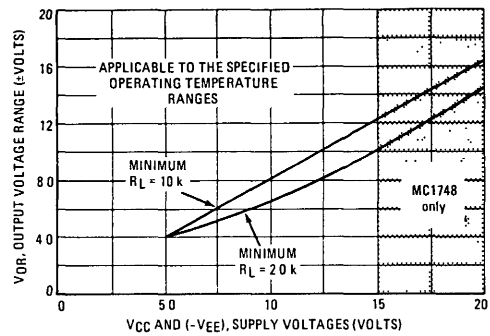


FIGURE 7 — MINIMUM VOLTAGE GAIN

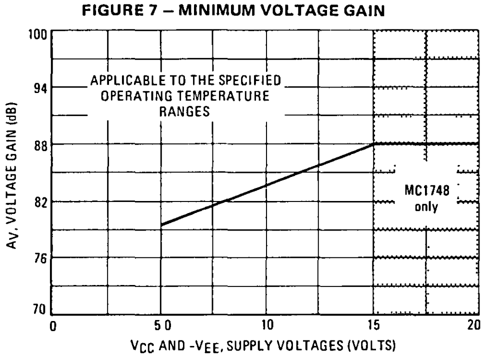


FIGURE 8 — TYPICAL SUPPLY CURRENTS

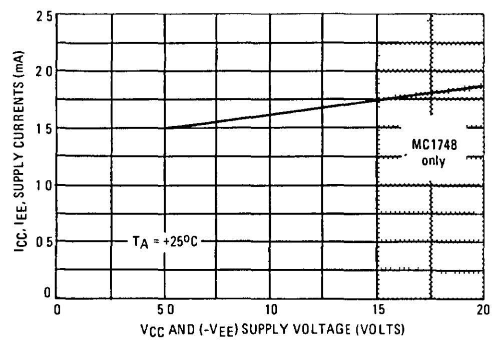


FIGURE 9 — OPEN-LOOP FREQUENCY RESPONSE

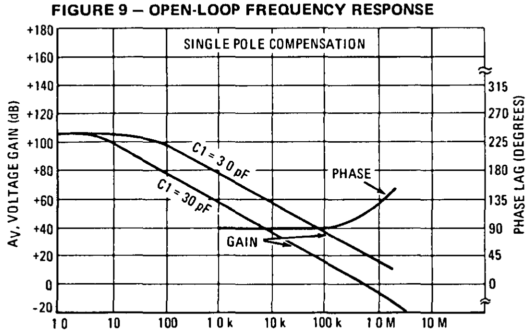
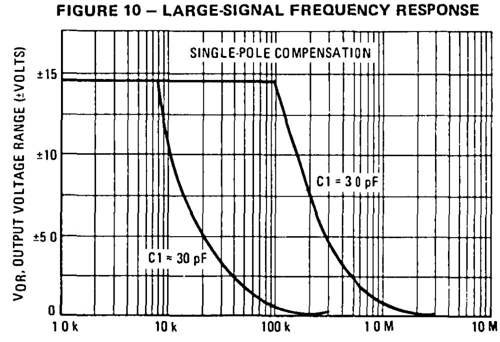


FIGURE 10 — LARGE-SIGNAL FREQUENCY RESPONSE



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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 – VOLTAGE FOLLOWER PULSE RESPONSE

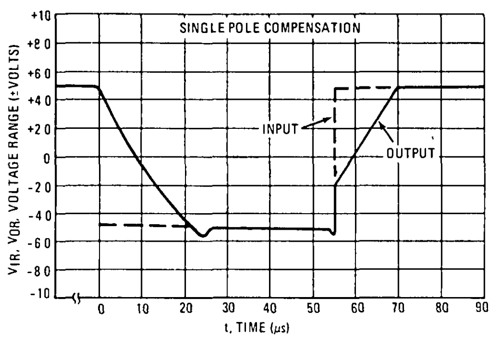


FIGURE 12 – OPEN-LOOP FREQUENCY RESPONSE

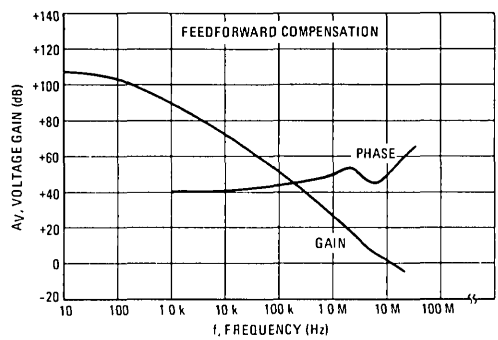


FIGURE 13 – LARGE-SIGNAL FREQUENCY RESPONSE

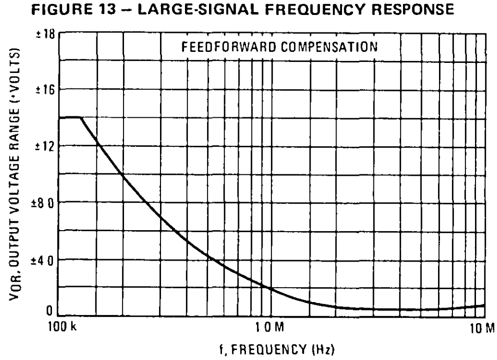
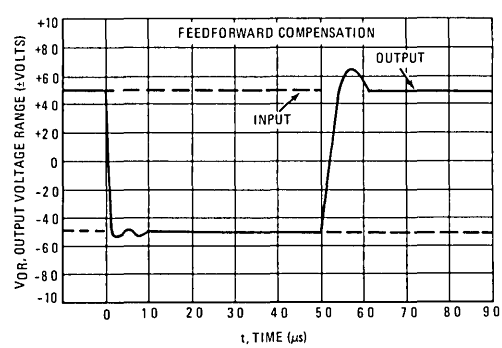


FIGURE 14 – INVERTER PULSE RESPONSE



MC1776
MC1776C

Specifications and Applications Information

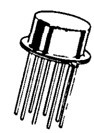
MONOLITHIC MICROPOWER PROGRAMMABLE OPERATIONAL AMPLIFIER

This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

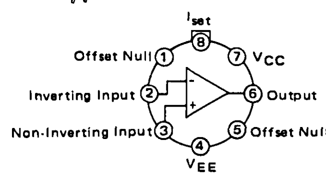
- ±1.2 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

PROGRAMMABLE OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



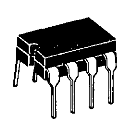
G SUFFIX
METAL PACKAGE
CASE 601

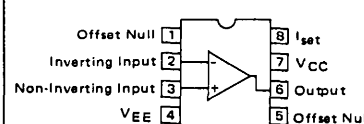


(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1776C only)

U SUFFIX
CERAMIC PACKAGE
CASE 693

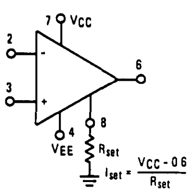




(Top View)

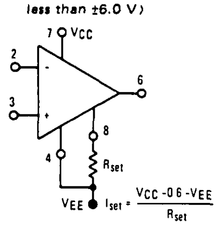
RESISTIVE PROGRAMMING (See Figure 1.)

R_{set} to GROUND



Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 μA	I_{set} = 15 μA
±6.0V	3.6 MΩ	360 kΩ
±10V	6.2 MΩ	620 kΩ
±12V	7.5 MΩ	750 kΩ
±15V	10 MΩ	1.0 MΩ

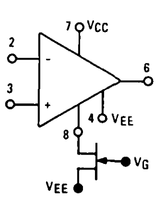
R_{set} to NEGATIVE SUPPLY
(Recommended for supply voltage less than ±6.0 V)



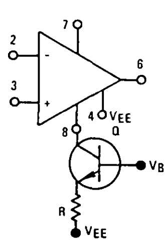
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 μA	I_{set} = 15 μA
±1.5V	1.6 MΩ	160 kΩ
±3.0V	3.6 MΩ	360 kΩ
±6.0V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

ACTIVE PROGRAMMING

FET CURRENT SOURCE



BIPOLAR CURRENT SOURCE



Pins not shown are not connected.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1776G	−55 to +125°C	Metal Can
MC1776U	−55 to +125°C	Ceramic DIP
MC1776CG	0 to +70°C	Metal Can
MC1776CP1	0 to +70°C	Plastic DIP
MC1776CU	0 to +70°C	Ceramic DIP

3

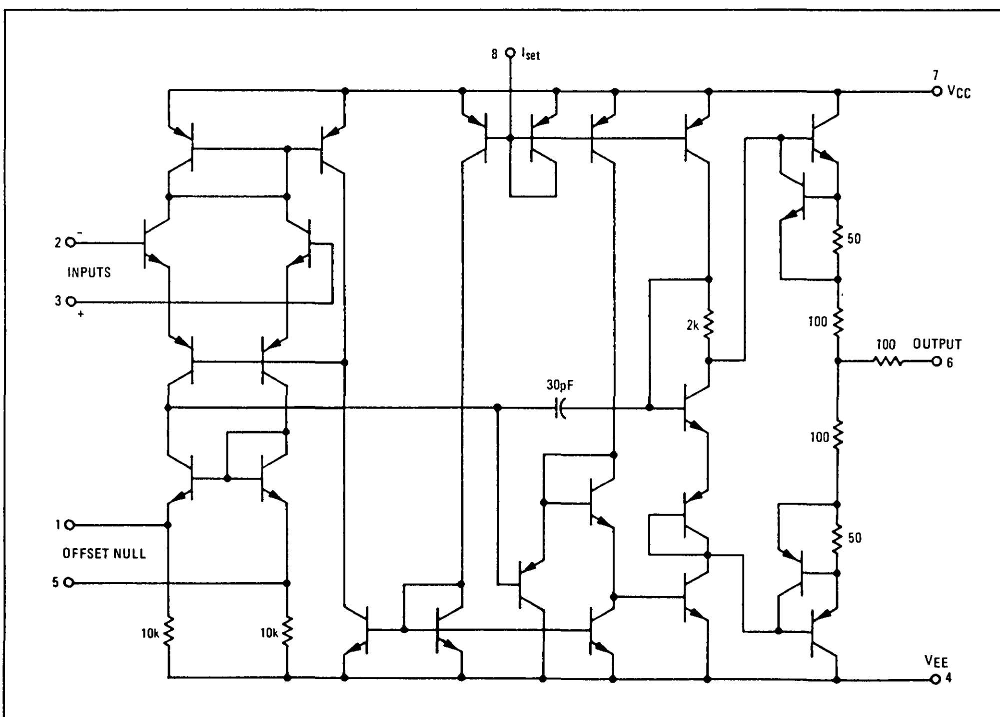
3

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Differential Input Voltage	V_{ID}	±30	Vdc
Common-Mode Input Voltage V_{CC} and $\|V_{EE}\| < 15$ V V_{CC} and $\|V_{EE}\| \geq 15$ V	V_{ICM}	 V_{CC}, V_{EE} ±15	Vdc
Offset Null to V_{EE} Voltage	$V_{off}-V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	500	μA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	(V_{CC}-2.0 V) to V_{CC}	Vdc
Output Short-Circuit Duration*	t_s	Indefinite	s
Operating Temperature Range MC1776 MC1776C	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 -65 to +150 -55 to +125	°C
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 175 150	°C

*May be to ground or either Supply Voltage. Rating applies up to a case temperature of +125°C or ambient temperature of +70°C and $I_{set} \leq 30$ μA.

SCHEMATIC DIAGRAM



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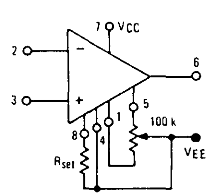
ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = -3.0 V, I_{set} = 1.5 μA, T_A = +25°C unless otherwise noted.)

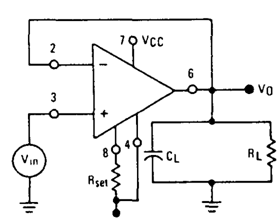
Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ T_A ≤ T_{high}*		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	–	9.0	–	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		–	0.7	3.0	–	0.7	6.0	
T_A = T_{high}		–	–	5.0	–	–	6.0	
T_A = T_{low}		–	–	10	–	–	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	2.0	7.5	–	2.0	10	
T_A = T_{high}		–	–	7.5	–	–	10	
T_A = T_{low}		–	–	20	–	–	20	
Input Resistance	r_i	–	50	–	–	50	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
T_{low} ≤ T_A ≤ T_{high}		±1.0	–	–	±1.0	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
R_L ≥ 75 kΩ, V_O = ±1.0 V, T_A = +25°C		50 k	200 k	–	25 k	200 k	–	
R_L ≥ 75 kΩ, V_O = ±1.0 V, T_{low} ≤ T_A ≤ T_{high}		25 k	–	–	25 k	–	–	
Output Voltage Swing	V_O							V
R_L ≥ 75 kΩ, T_{low} ≤ T_A ≤ T_{high}		±2.0	±2.4	–	±2.0	±2.4	–	
Output Resistance	r_o	–	5.0	–	–	5.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	3.0	–	–	3.0	–	mA
Common-Mode Rejection Ratio	CMRR							dB
R_S ≤ 10 kΩ, T_{low} ≤ T_A ≤ T_{high}		70	86	–	70	86	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
R_S ≤ 10 kΩ, T_{low} ≤ T_A ≤ T_{high}		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	13	20	–	13	20	
T_{low} ≤ T_A ≤ T_{high}		–	–	25	–	–	25	
Power Dissipation	P_D							μW
T_A = +25°C		–	78	120	–	78	120	
T_{low} ≤ T_A ≤ T_{high}		–	–	150	–	–	150	
Transient Response (Unity Gain)								
V_{in} = 20 mV, R_L ≥ 5.0 kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	3.0	–	–	3.0	–	μs
Overshoot	OS	–	0	–	–	0	–	%
Slew Rate (R_L ≥ 5.0 kΩ)	S_R	–	0.03	–	–	0.03	–	V/μs

*T_{low} = -55°C for MC1776, 0°C for MC1776C; T_{high} = +125°C for MC1776, +70°C for MC1776C

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT-RESPONSE TEST CIRCUIT



Pins not shown are not connected

3

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = −3.0 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ T_A ≤ T_{high}*		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	–	18	–	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		–	2.0	15	–	2.0	25	
T_A = T_{high}		–	–	15	–	–	25	
T_A = T_{low}		–	–	40	–	–	40	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	15	50	–	15	50	
T_A = T_{high}		–	–	50	–	–	50	
T_A = T_{low}		–	–	120	–	–	100	
Input Resistance	r_i	–	5.0	–	–	5.0	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
T_{low} ≤ T_A ≤ T_{high}		±1.0	–	–	±1.0	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
R_L ≥ 5.0 kΩ, V_O = ±1.0 V, T_A = +25°C		50 k	200 k	–	25 k	200 k	–	
R_L ≥ 5.0 kΩ, V_O = ±1.0 V, T_{low} ≤ T_A ≤ T_{high}		25 k	–	–	25k	–	–	
Output Voltage Swing	V_O							V
R_L ≥ 5.0 kΩ, T_{low} ≤ T_A ≤ T_{high}		±1.9	±2.1	–	±2.0	±2.1	–	
Output Resistance	r_o	–	1.0	–	–	1.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	5.0	–	–	5.0	–	mA
Common-Mode Rejection Ratio	CMRR							dB
R_S ≤ 10 kΩ, T_{low} ≤ T_A ≤ T_{high}		70	86	–	70	86	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
R_S ≤ 10 kΩ, T_{low} ≤ T_A ≤ T_{high}		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	130	160	–	130	170	
T_{low} ≤ T_A ≤ T_{high}		–	–	180	–	–	180	
Power Dissipation	P_D							μW
T_A = +25°C		–	780	960	–	780	1020	
T_{low} ≤ T_A ≤ T_{high}		–	–	1080	–	–	1080	
Transient Response (Unity Gain)								
V_{in} = 20 mV, R_L ≥ 5.0 kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	0.6	–	–	0.6	–	μs
Overshoot	OS	–	5.0	–	–	5.0	–	%
Slew Rate (R_L ≥ 5.0 kΩ)	S_R	–	0.35	–	–	0.35	–	V/μs

*T_{low} = −55°C for MC1776; 0°C for MC1776C
T_{high} = +125°C for MC1776; +70°C for MC1776C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, I_{set} = 1.5 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ T_A ≤ T_{high}*		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	–	9.0	–	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		–	0.7	3.0	–	0.7	6.0	
T_A = T_{high}		–	–	5.0	–	–	6.0	
T_A = T_{low}		–	–	10	–	–	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	2.0	7.5	–	2.0	10	
T_A = T_{high}		–	–	7.5	–	–	10	
T_A = T_{low}		–	–	20	–	–	20	
Input Resistance	r_i	–	50	–	–	50	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
T_{low} ≤ T_A ≤ T_{high}		±10	–	–	±10	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
R_L ≥ 75 kΩ, V_O = ±10 V, T_A = +25°C		200 k	400 k	–	50 k	400 k	–	
R_L ≥ 75 kΩ, V_O = ±10 V, T_{low} ≤ T_A ≤ T_{high}		100 k	–	–	50 k	–	–	
Output Voltage Swing	V_O							V
R_L ≥ 75 kΩ, T_A = +25°C		±12	±14	–	±12	±14	–	
R_L ≥ 75 kΩ, T_{low} ≤ T_A ≤ T_{high}		±10	–	–	±10	–	–	
Output Resistance	r_o	–	5.0	–	–	5.0	–	kΩ
Output Short-Circuit Current	I_{OS}	–	3.0	–	–	3.0	–	mA
Common-Mode Rejection Ratio	CMRR							dB
R_S ≤ 10 kΩ, T_{low} ≤ T_A ≤ T_{high}		70	90	–	70	90	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
R_S ≤ 10 kΩ, T_{low} ≤ T_A ≤ T_{high}		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	20	25	–	20	30	
T_{low} ≤ T_A ≤ T_{high}		–	–	30	–	–	35	
Power Dissipation	P_D							mW
T_A = +25°C		–	–	0.75	–	–	0.9	
T_{low} ≤ T_A ≤ T_{high}		–	–	0.9	–	–	1.05	
Transient Response (Unity Gain)								
V_{in} = 20 mV, R_L ≥ 5.0 kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	1.6	–	–	1.6	–	μs
Overshoot	OS	–	0	–	–	0	–	%
Slew Rate (R_L ≥ 5.0 kΩ)	S_R	–	0.1	–	–	0.1	–	V/μs

*T_{low} = -55°C for MC1776, 0°C for MC1776C; T_{high} = +125°C for MC1776, +70°C for MC1776C

3

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \le$ 10 kΩ)	V_{IO}							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ T_A ≤ T_{high}*		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	–	18	–	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		–	2.0	15	–	2.0	25	
T_A = T_{high}		–	–	15	–	–	25	
T_A = T_{low}		–	–	40	–	–	40	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	15	50	–	15	50	
T_A = T_{high}		–	–	50	–	–	50	
T_A = T_{low}		–	–	120	–	–	100	
Input Resistance	r_i	–	5.0	–	–	5.0	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
T_{low} ≤ T_A ≤ T_{high}		±10	–	–	±10	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
R_L ≥ 5.0 kΩ, V_O = ±10 V, T_A = +25°C		100 k	400 k	–	50 k	400 k	–	
R_L ≥ 75 kΩ, V_O = ±10 V, T_{low} ≤ T_A ≤ T_{high}		75 k	–	–	50 k	–	–	
Output Voltage Swing	V_O							V
R_L ≥ 5.0 kΩ, T_A = +25°C		±10	±13	–	±10	±13	–	
R_L ≥ 75 kΩ, T_{low} ≤ T_A ≤ T_{high}		±10	–	–	±10	–	–	
Output Resistance	r_o	–	1.0	–	–	1.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	12	–	–	12	–	mA
Common-Mode Rejection Ratio	CMRR							dB
R_S ≤ 10 kΩ, T_{low} ≤ T_A ≤ T_{high}		70	90	–	70	90	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
R_S ≤ 10 kΩ, T_{low} ≤ T_A ≤ T_{high}		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	160	180	–	160	190	
T_{low} ≤ T_A ≤ T_{high}		–	–	200	–	–	200	
Power Dissipation	P_D							mW
T_A = +25°C		–	–	5.4	–	–	5.7	
T_{low} ≤ T_A ≤ T_{high}		–	–	6.0	–	–	6.0	
Transient Response (Unity Gain)								
V_{in} = 20 mV, R_L ≥ 5.0 kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	0.35	–	–	0.35	–	μs
Overshoot	OS	–	10	–	–	10	–	%
Slew Rate (R_L ≥ 5.0 kΩ)	S_R	–	0.8	–	–	0.8	–	V/μs

*T_{low} = −55°C for MC1776; 0°C for MC1776C
T_{high} = +125°C for MC1776; +70°C for MC1776C

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

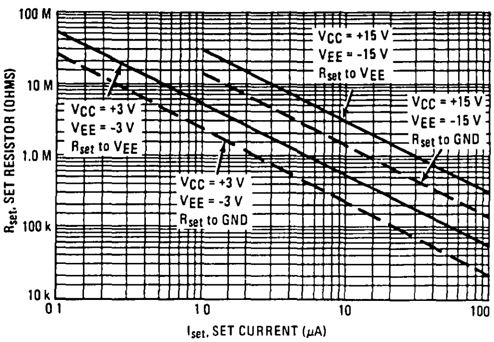


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

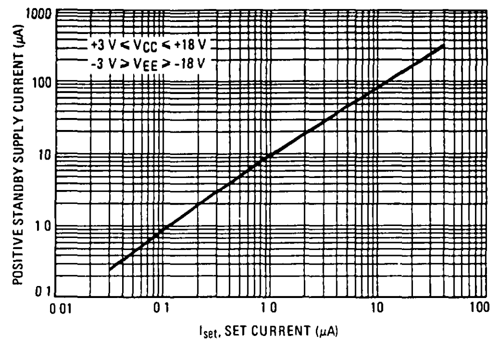


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

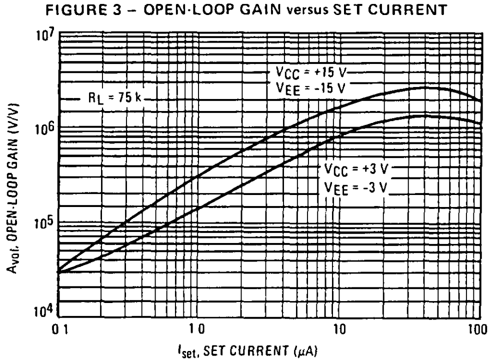


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

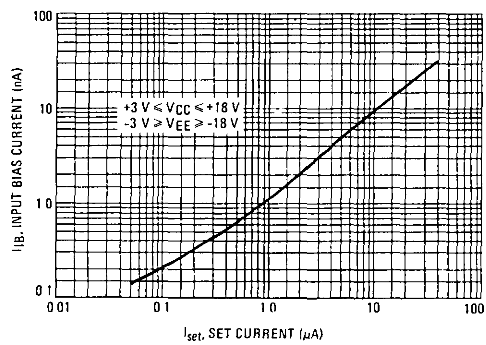


FIGURE 5 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

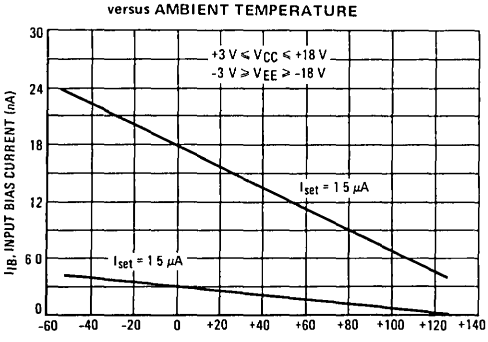
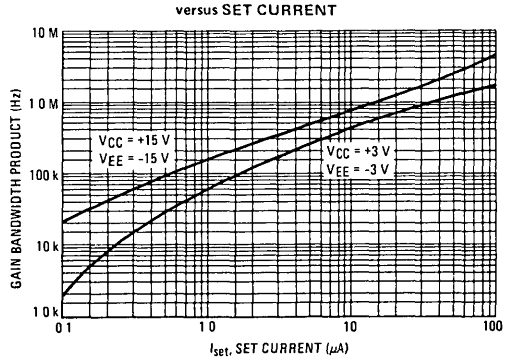


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



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TYPICAL CHARACTERISTICS (continued)

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

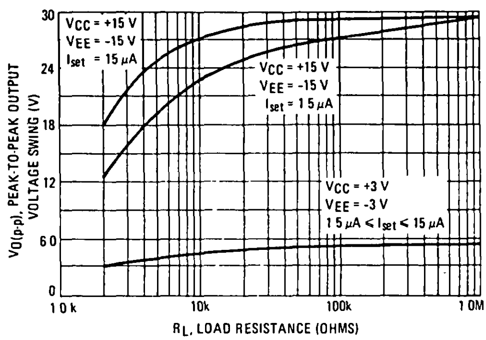


FIGURE 8 – SUPPLY CURRENT versus AMBIENT TEMPERATURE

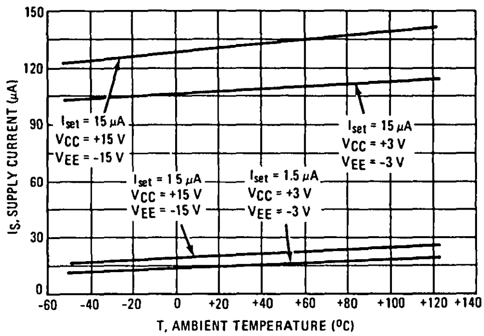


FIGURE 9 – OUTPUT SWING versus SUPPLY VOLTAGE

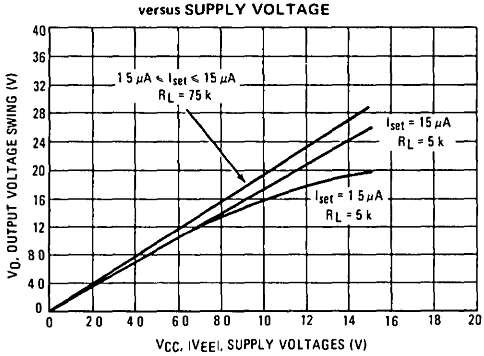


FIGURE 10 – SLEW RATE versus SET CURRENT

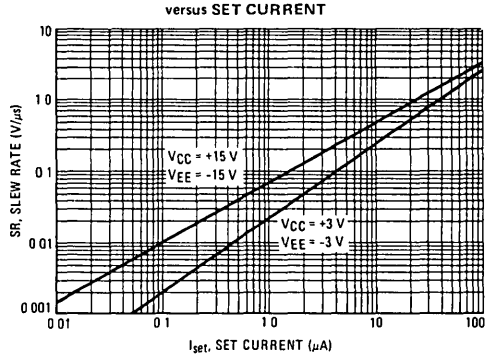


FIGURE 11 – INPUT NOISE VOLTAGE versus SET CURRENT

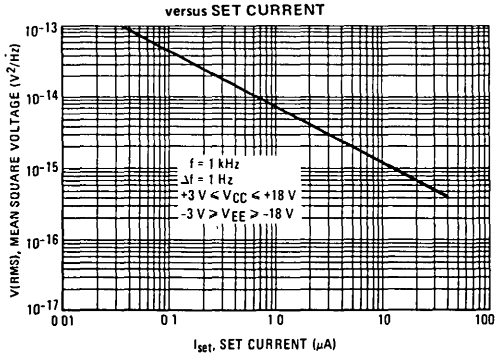
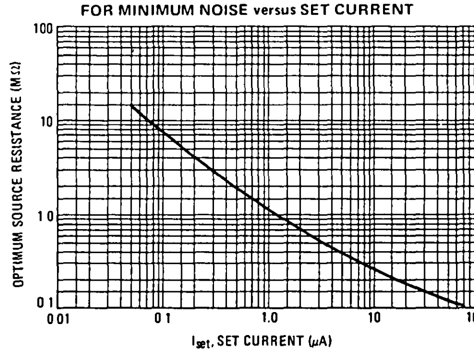


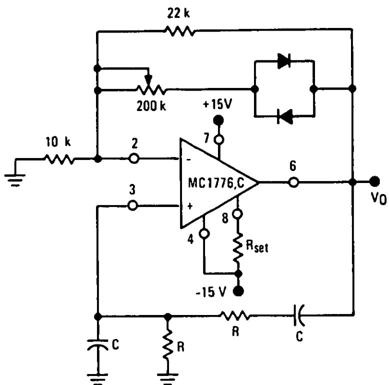
FIGURE 12 – OPTIMUM SOURCE RESISTANCE FOR MINIMUM NOISE versus SET CURRENT



3

APPLICATIONS INFORMATION

FIGURE 13 – WIEN BRIDGE OSCILLATOR

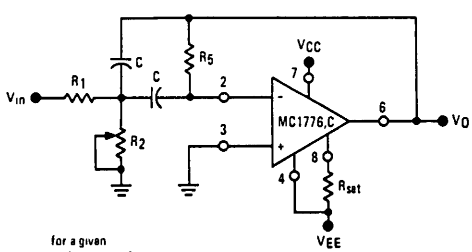


$$f_0 = \frac{1}{2\pi RC}$$

(for f_0 = 1 0 kHz)

R = 16 kΩ
C = 0 01 μF

FIGURE 14 – MULTIPLE FEEDBACK BANDPASS FILTER



for a given
f_0 = center frequency
A (f_0) = Gain at center frequency
Q = quality factor
Choose a value for C, then

$$R5 = \frac{Q}{\pi f_0 C}$$

$$R1 = \frac{R5}{2A(f_0)}$$

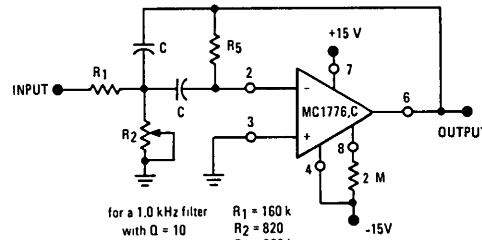
$$R2 = \frac{R1 R5}{4Q^2 R1 - R5}$$

To obtain less than 10% error from the operational amplifier

$$\frac{Q_0 f_0}{GBW} < 0 1$$

where f_0 and GBW are expressed in Hz. GBW is available from Figure 6 as a function of Set Current, I_{set}

FIGURE 15 – MULTIPLE FEEDBACK BANDPASS FILTER (1.0 kHz)



for a 1.0 kHz filter with Q = 10 and A (f_0) = 1

R_1 = 160 k
R_2 = 820
R_5 = 300 k
C = 0 01 μF

FIGURE 16 – GATED AMPLIFIER

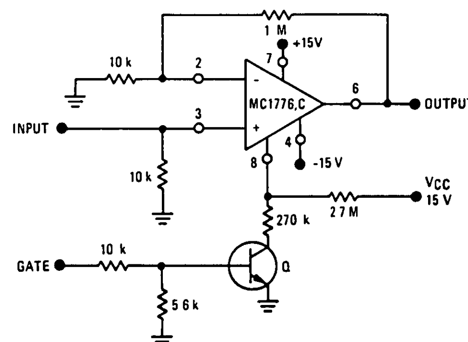
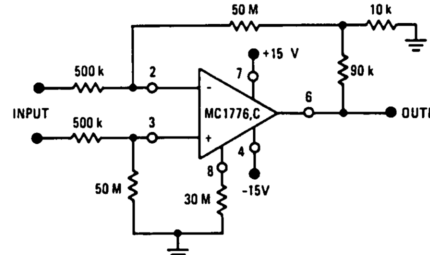


FIGURE 17 – HIGH INPUT IMPEDANCE AMPLIFIER



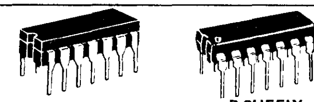
ORDERING INFORMATION

Device	Temperature Range	Package
MC3301L	−40°C to +85°C	Ceramic DIP
MC3301P	−40°C to +85°C	Plastic DIP

MC3301

QUAD OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER FOR AUTOMOTIVE APPLICATIONS

These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in automotive and consumer electronics. Each MC3301 contains four independent amplifiers – making it ideal for automotive safety, pollution, and comfort controls. Some typical applications are tachometer, voltage regulator, logic circuits, power control and other similar usages.

- Wide Operating Temperature Range – -40 to +85°C
- Single-Supply Operation – +4.0 to +28 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth – 4.0 MHz typical
- Low Input Bias Current – 50 nA typical
- High Open-Loop Gain – 2000 V/V typical

FIGURE 1 – EQUIVALENT CIRCUIT

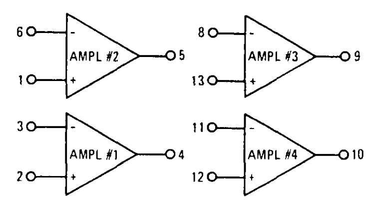
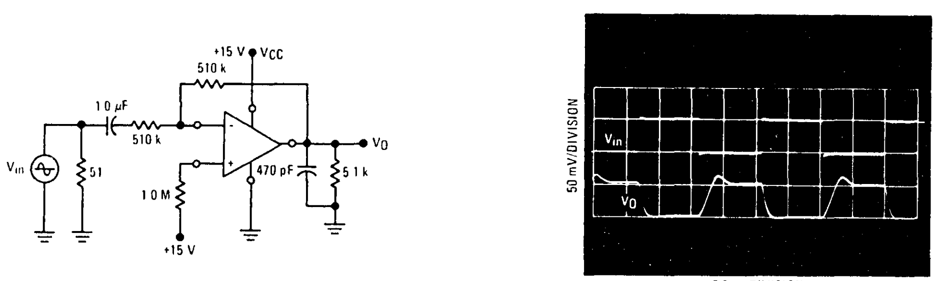


FIGURE 2 – SMALL-SIGNAL TRANSIENT RESPONSE



5.0 µs/DIVISION

FIGURE 3 – INVERTING AMPLIFIER

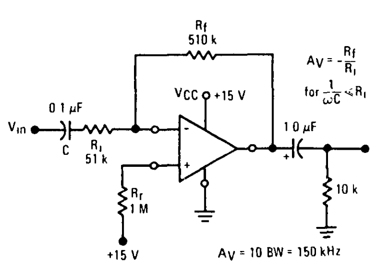
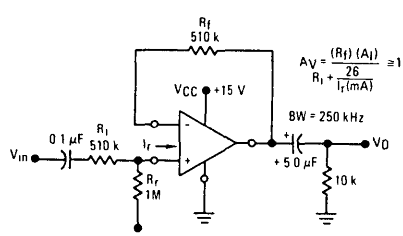


FIGURE 4 – NONINVERTING AMPLIFIER



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+28	Vdc
Noninverting Input Current	I_r	5 0	mA
Sink Current	I_{sink}	50	mA
Source Current	I_{source}	50	mA
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	625 5 0	mW mW/°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS [V_{CC} = +15 Vdc, R_L = 5 0 kΩ, T_A = +25°C (each amplifier) unless otherwise noted]

Characteristic	Fig.No.	Note	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain T_A = +25°C -40°C ≤ T_A ≤ +85°C	5		A_{vol}	 1000 –	 2000 1600	 – –	V/V
Quiescent Power Supply Current (Total for four amplifiers) Noninverting inputs open Noninverting inputs grounded	6	1	 I_{DO} I_{DG}	 – –	 6 9 7 8	 10 14	mAdc
Input Bias Current, R_L = ∞ T_A = +25°C -40°C ≤ T_A ≤ +85°C	7	2	I_{IB}	 – –	 50 100	 300 –	nAdc
Current Mirror Gain (I_r = 200 μAdc)	7	3	A_I	0 80	0 98	1 16	A/A
Current Mirror Gain Drift -40°C ≤ T_A ≤ +85°C				 –	 ±2 5	 –	%
Output Current Source Capability (V_{OH} = 0 4 Vdc) (V_{OH} = 9.0 Vdc) Sink Capability (V_{OL} = 0 4 Vdc)	8		 I_{source} I_{sink}	 3 0 – 0.5	 10 7.0 0 87	 – – –	mAdc
Output Voltage High Voltage Low Voltage (Inverting Input Driven) (Noninverting Input Driven)	6		 V_{OH} $V_{OL(inv)}$ $V_{OL(non)}$	 13 5 – –	 14 2 0 03 0 6	 – 0 1 –	Vdc
Input Resistance (Inverting input only)			R_{in}	0 1	1.0	–	Meg Ω
Slew Rate (C_L = 100 pF, R_L = 5 0 k)			SR	–	0 6	–	V/μs
Unity Gain Bandwidth		4	BW	–	4 0	–	MHz
Phase Margin		4	φm	–	70	–	Degrees
Power Supply Rejection (f = 100 Hz)			PSSR	–	55	–	dB
Channel Separation (f = 1.0 kHz)			e_{o1}/e_{o2}	–	65	–	dB

NOTES:

1 The quiescent current drain will increase approximately 0 3 mA for each inverting or noninverting input that is grounded.

2. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" – as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current

3 Current mirror gain is defined as the current demanded at the inverting input divided by the current into the noninverting input

4 Bandwidth and phase margin are defined with respect to the voltage gain from the inverting input to the output

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 5 – OPEN-LOOP VOLTAGE GAIN

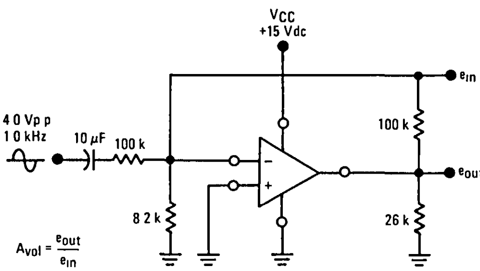
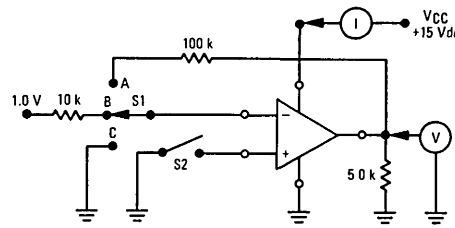


FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT



All four amplifiers operate in the same configuration simultaneously.

I_{DO}, S1 = A S2 = OPEN
I_{DG}, S1 = A S2 = CLOSED
$V_{OH}(-)$, S1 = C S2 = CLOSED
$V_{OL}(-)$, S1 = B S2 = CLOSED
$V_{OL}(+)$, S1 = A S2 = CLOSED

FIGURE 7 – INPUT BIAS CURRENT AND CURRENT MIRROR GAIN

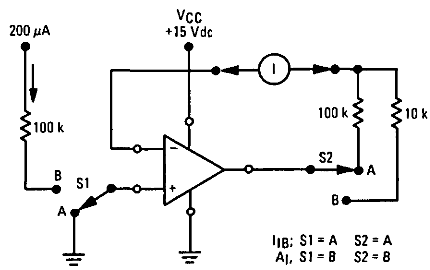
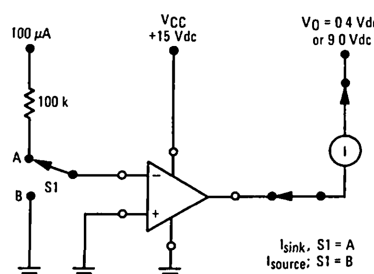


FIGURE 8 – OUTPUT CURRENT



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

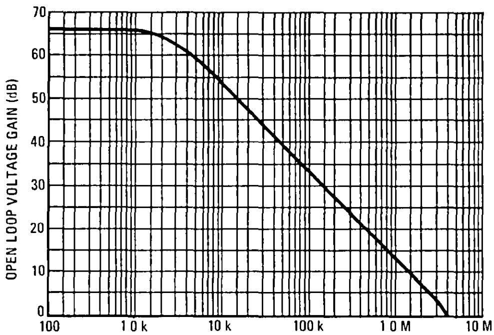


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

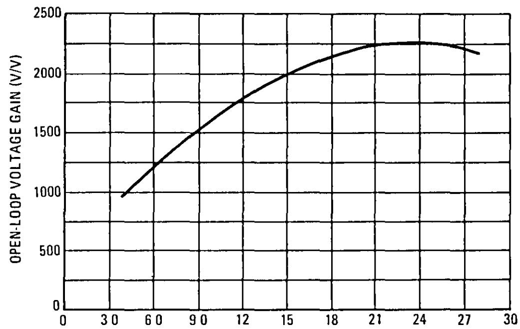


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

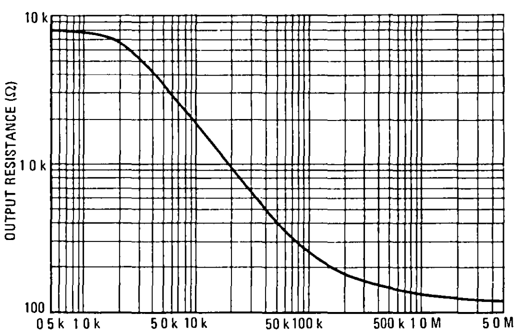


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

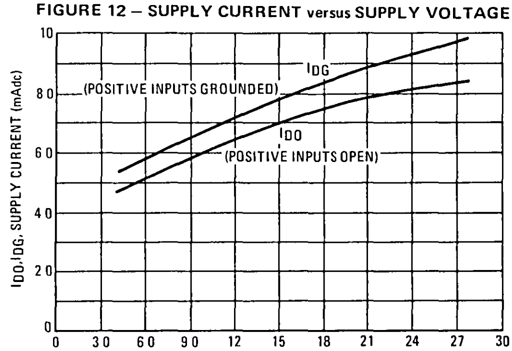


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

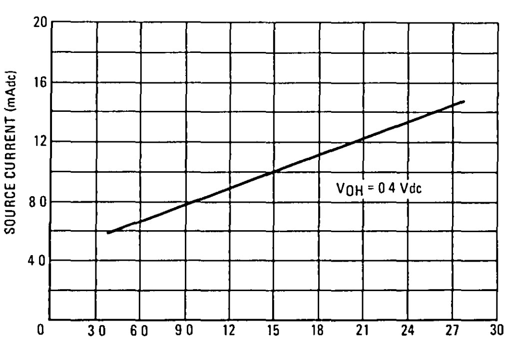
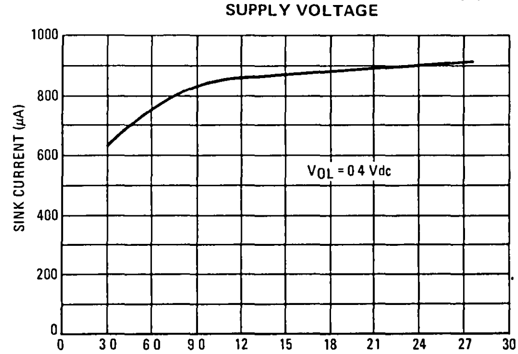


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE



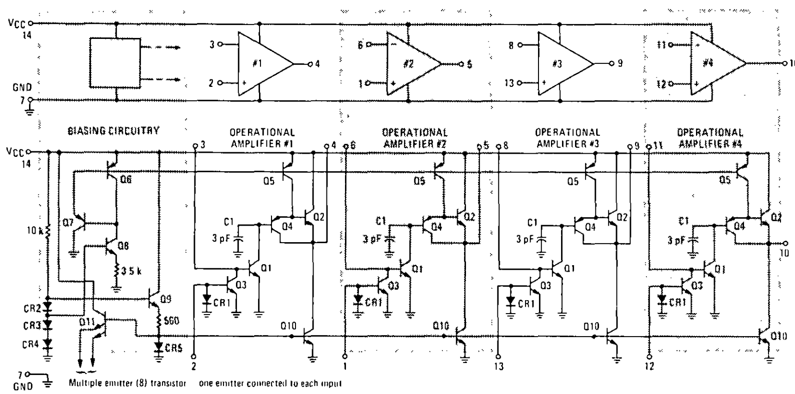
3

OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16 The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2 Q2 is biased class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output The sink current of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 volt resulting in an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18 on the following page No external compensation is required.

FIGURE 15
BLOCK DIAGRAM



A noninverting input is obtained by adding a current mirror as shown in Figure 17 Essentially all current which enters the noninverting input, I_r, flows through the diode CR1 The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_r. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to I_r also In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output Techniques for doing this are discussed in the "Normal Design Procedure" section

FIGURE 16 – A BASIC GAIN STAGE

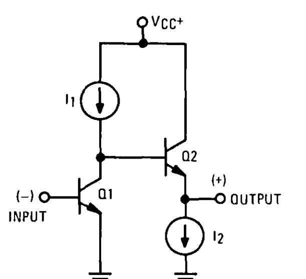
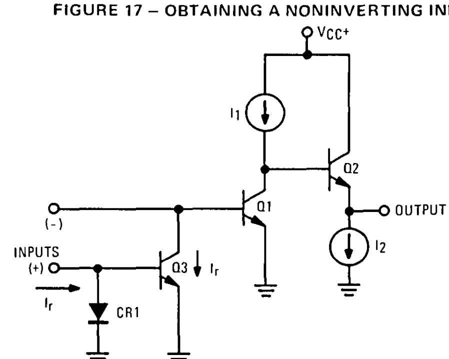


FIGURE 17 – OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19, see next page The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8 The PNP current sources (Q5, etc) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.) This technique results in current source magnitudes which are relatively independent of the supply voltage Q11 (Figure 15) provides circuit protection from signals that are negative with respect to ground.

OPERATION AND APPLICATIONS (continued)

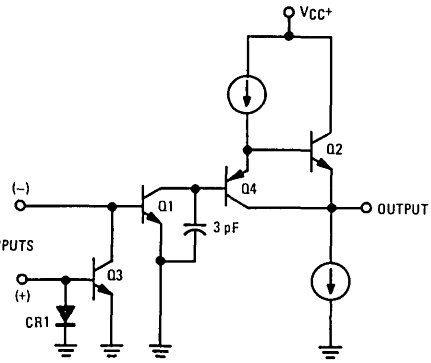


FIGURE 18 — A BASIC OPERATIONAL AMPLIFIER

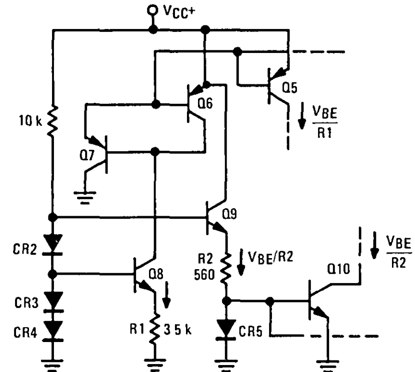


FIGURE 19 — BIASING CIRCUITRY

NORMAL DESIGN PROCEDURE

1 Output Q-Point Biasing

A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4 (see the first page of this specification). The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μA to 200 μA range.

B. V_{CC} Reference Voltage (see Figures 3 and 4)

The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 10 μA to 200 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows the maximum dynamic range of the output voltage.

C Reference Voltage other than V_{CC} (see Figure 20)

The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_r between 10 μA and 200 μA) the output dc level will be equal to V_r The expression for determining V_{Odc} is

$$V_{Odc} = \frac{(A_I)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_I\right)\phi$$

where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_I is the current mirror gain.

2. Gain Determination

A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

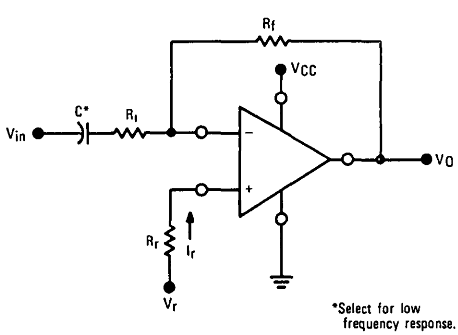


FIGURE 20 — INVERTING AMPLIFIER WITH ARBITRARY REFERENCE

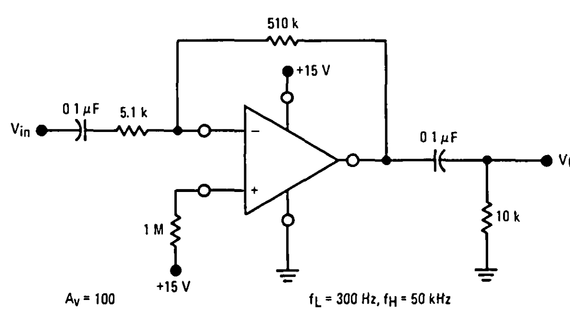


FIGURE 21 — INVERTING AMPLIFIER WITH A_v = 100 AND $V_r = V_{CC}$

NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier.

$$A_V = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 4.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 400 kHz with 20 dB of closed loop gain or 40 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

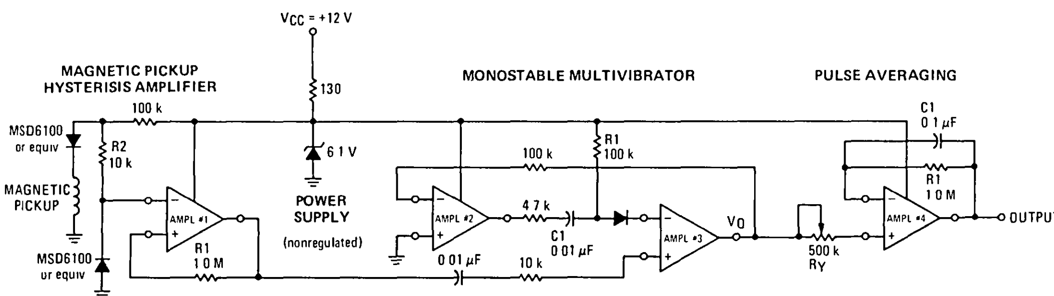
The MC3301 may be used in the noninverting mode (see Figure 4, first page). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting ac gain expression is given by

$$A_V = \frac{(R_f)(A_I)}{R_i + \frac{26}{I_r\,(mA)}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 22 – TACHOMETER CIRCUIT



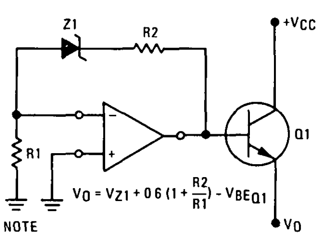
Hysterisis Voltage for Switching

$$V_H = \frac{A_I R2}{R1}\,(V_{CC} - 1.6)$$

Timing Interval $t \approx 0.7\ R1\,C1$

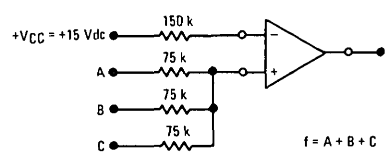
$$V_{p\,p} \cong \frac{(V_O - 0.6) \cdot A_I \cdot t}{R_Y C1}$$

FIGURE 23 – VOLTAGE REGULATOR



NOTE
For positive T_C zeners R2 and R1 can be selected to give 0 T_C output

FIGURE 24 – LOGIC "OR" GATE



TYPICAL APPLICATIONS (continued)

FIGURE 25 – LOGIC "NAND" GATE (Large Fan-In)

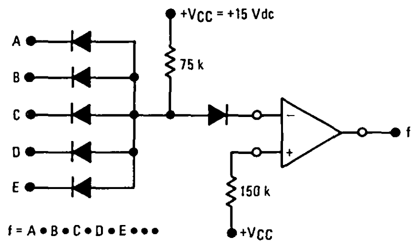


FIGURE 26 – LOGIC "NOR" GATE

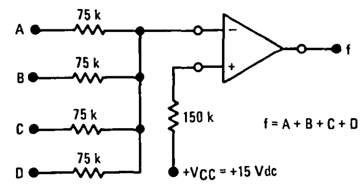


FIGURE 27 – R-S FLIP-FLOP

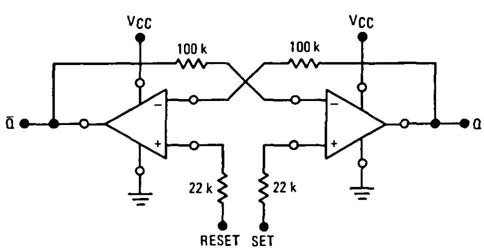


FIGURE 28 – ASTABLE MULTIVIBRATOR

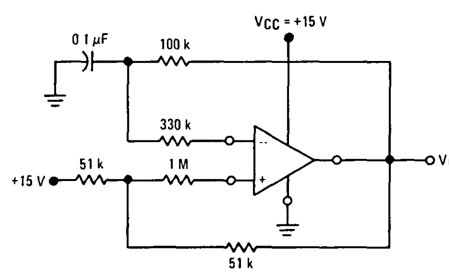


FIGURE 29 – POSITIVE-EDGE DIFFERENTIATOR

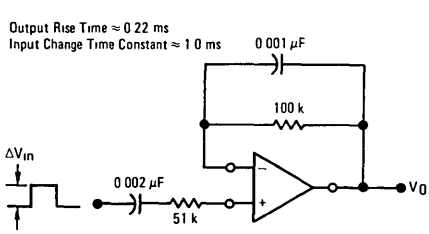
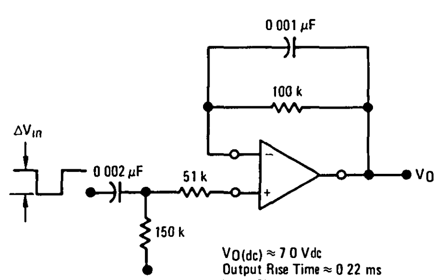


FIGURE 30 – NEGATIVE-EDGE DIFFERENTIATOR



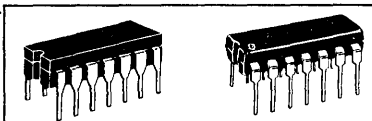
ORDERING INFORMATION

Device	Temperature Range	Package
MC3401L	0°C to +70°C	Ceramic DIP
MC3401P	0°C to +70°C	Plastic DIP

MC3401

Specifications and Applications Information

QUAD
OPERATIONAL AMPLIFIER
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

3

QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER

These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each MC3401 device contains four independent amplifiers – making it ideal for applications such as active filters, multi-channel amplifiers, tachometer, oscillator and other similar usages.

- Single-Supply Operation – +5.0 Vdc to +18 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth – 5.0 MHz typical
- Low Input Bias Current – 50 nA typical
- High Open-Loop Gain – 1000 V/V minimum

FIGURE 1 – EQUIVALENT CIRCUIT

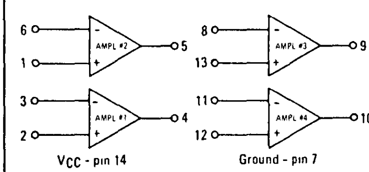


FIGURE 2 – SMALL-SIGNAL TRANSIENT RESPONSE

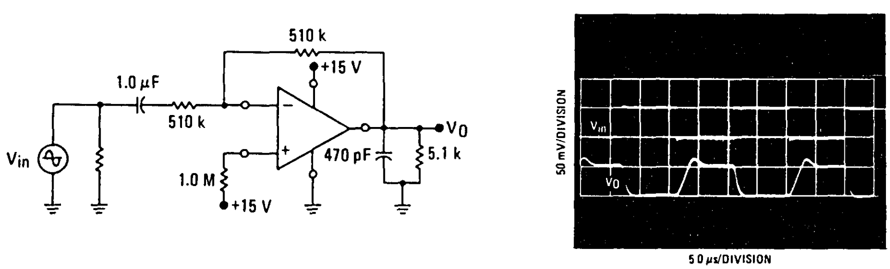


FIGURE 3 – INVERTING AMPLIFIER

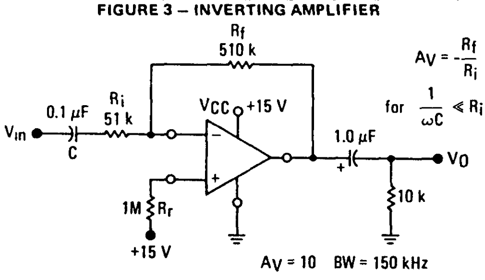
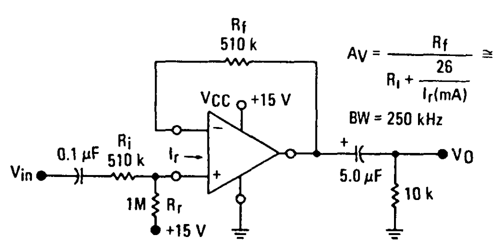


FIGURE 4 – NONINVERTING AMPLIFIER



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Non-inverting Input Current	I_{in}	5.0	mA
Power Dissipation Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS [V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C (each amplifier) unless otherwise noted]

Characteristic	Fig. No.	Note	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain T_A = +25°C 0°C ≤ T_A ≤ +70°C	5,9,10	1	A_{vol}	 1000 800	 2000 –	 – –	V/V
Quiescent Power Supply Current (Total for four amplifiers) Noninverting inputs open Noninverting inputs grounded	6,12	2	 I_{DO} I_{DG}	 – –	 6.9 7.8	 10 14	mAdc
Input Bias Current, R_L = ∞ T_A = +25°C 0°C ≤ T_A ≤ +70°C	5	3	I_{IB}	 – –	 50 –	 300 500	nAdc
Output Current Source Capability Sink Capability	5 13 14	4	 I_{source} I_{sink}	 5.0 0.5	 10 1.0	 – –	mAdc
Output Voltage High Voltage Low Voltage Undistorted Output Swing (0°C < T_A < +70°C)	 7 7 8	 5 5 6	 V_{OH} V_{OL} $V_{O(p-p)}$	 13.5 – 10	 14.2 0.03 13.5	 – 0.1 –	Vdc $V_{(p-p)}$
Input Resistance	5		R_{in}	0.1	1.0	–	MEG Ω
Slew Rate (C_L = 100 pF, R_L = 5.0 k)			SR	–	0.6	–	V/µs
Unity Gain Bandwidth			BW	–	5.0	–	MHz
Phase Margin			ϕ_m	–	70	–	Degrees
Power Supply Rejection (f = 100 Hz)		7	PSSR	–	55	–	dB
Channel Separation (f = 1.0 kHz)			e_{o1}/e_{o2}	–	65	–	dB

NOTES

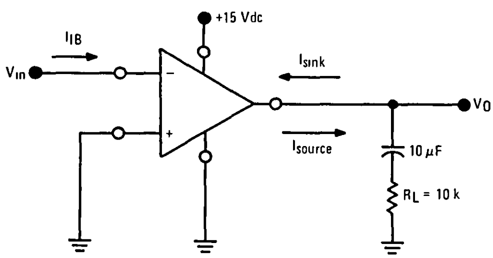
1. Open loop voltage gain is defined as the voltage gain from the inverting input to the output
2. The quiescent current will increase approximately 0.3 mA for each noninverting input which is grounded. Leaving the noninverting input open causes the apparent input bias current to increase slightly (100 nA) at high temperatures.
3. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" – as with a conventional IC operational amplifier As such this input does not have a requirement for input bias current.
4. Sink current is specified for linear operation. When the device is used as a gate or a comparator (non-linear operation), the sink capability of the device is approximately 5.0 milliamperes.
5. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.
6. Peak-to-peak restrictions are due to the variations of the quiescent dc output voltage in the standard configuration (Figure 8).
7. Power supply rejection is specified at closed loop unity gain, and therefore indicates the supply rejection of both the biasing circuitry and the feedback amplifier.

3

SIMPLIFIED TEST CIRCUITS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted)

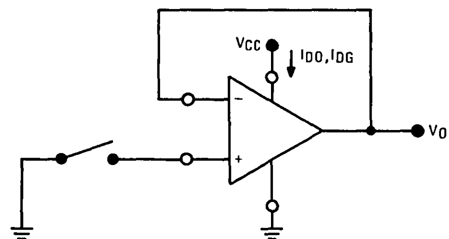
FIGURE 5 – OPEN-LOOP GAIN AND INPUT RESISTANCE (INPUT BIAS CURRENT, OUTPUT CURRENT)



$R_{in} = \frac{\Delta V_{in}}{\Delta I_{IB}}$ $A_{vol} = -\frac{\Delta V_O}{\Delta V_{in}}$

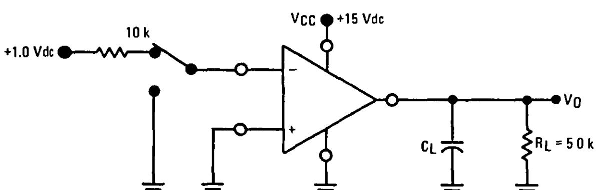
Amplifier must be biased (by V_{in}) in the linear operating region.

FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT



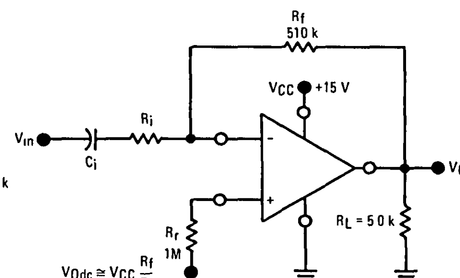
I_{DO} is total supply current with "+" input open
I_{DG} is total supply current with "+" input grounded

FIGURE 7 – OUTPUT VOLTAGE SWING



V_{OL} measured with "–" input biased up as shown
V_{OH} measured with "–" input grounded.

FIGURE 8 – PEAK-TO-PEAK OUTPUT VOLTAGE



$V_{Odc} \cong V_{CC} \frac{R_f}{R_r} \cong \frac{V_{CC}}{2}$

for $R_r \cong 2R_f$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

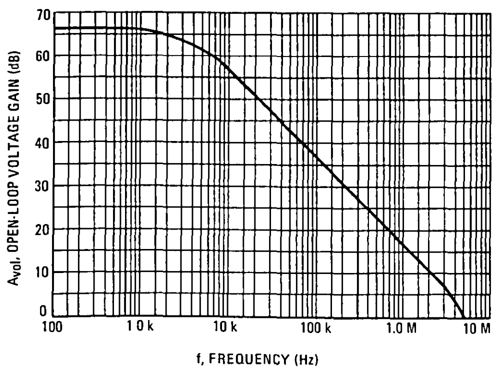


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

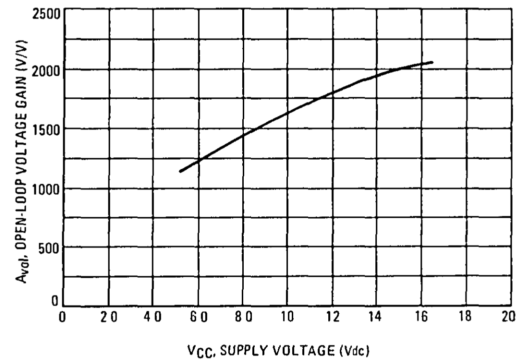


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

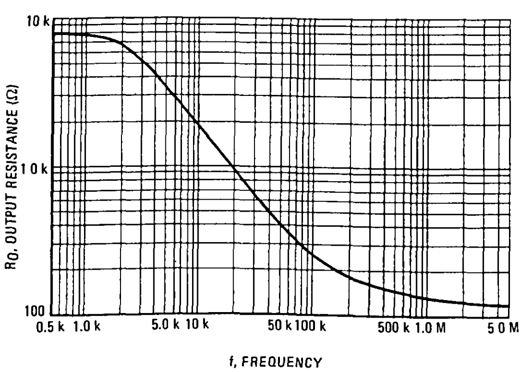


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

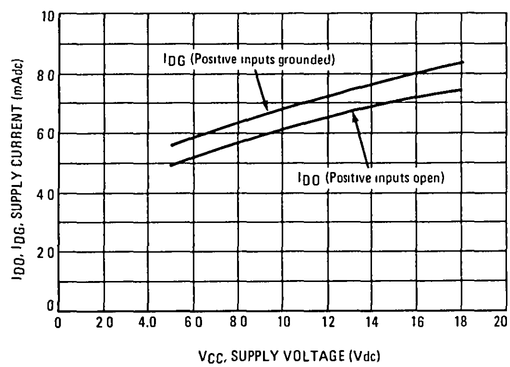


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

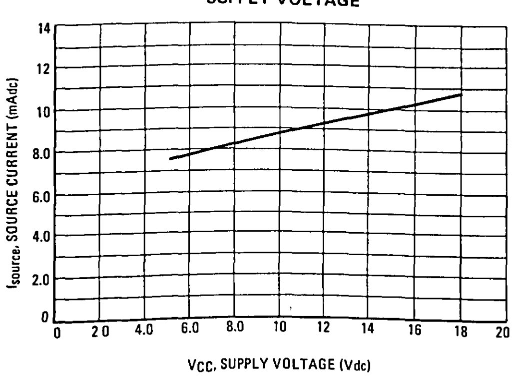
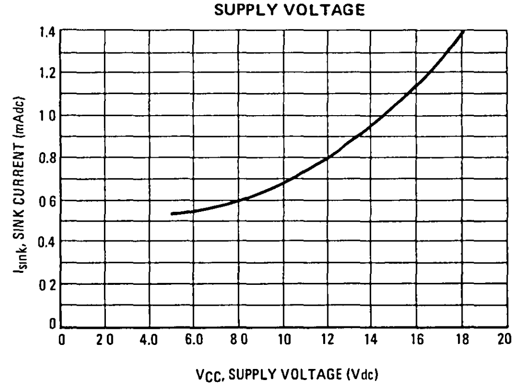


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE



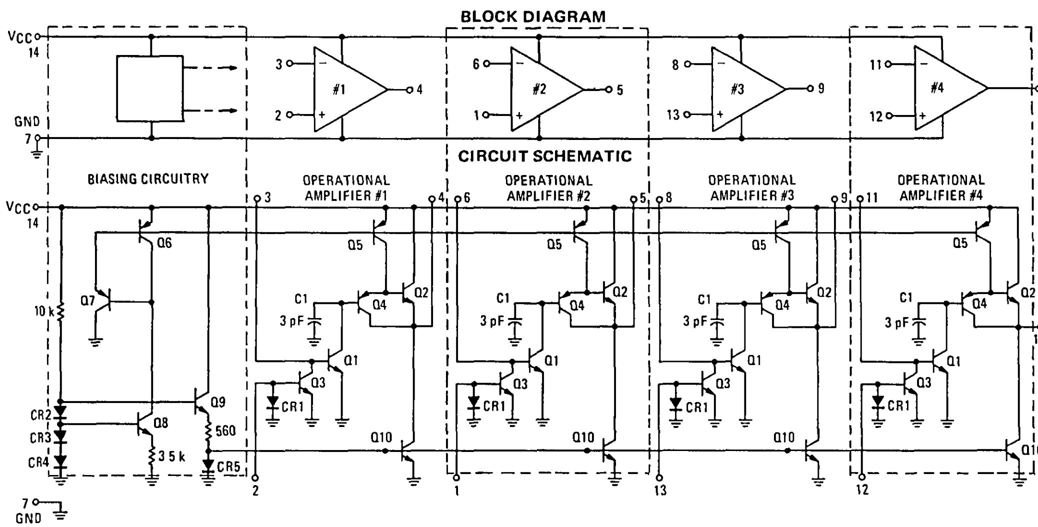
3

OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level with an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18. No external compensation is required.

FIGURE 15



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the noninverting input, I_{in2}, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in2}. Since the alpha current gain of Q3 $\approx$ 1, its collector current $\approx I_{in2}$ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 16 – A BASIC GAIN STAGE

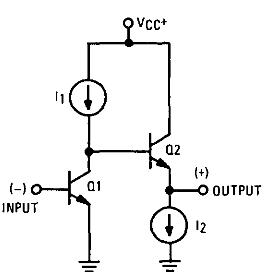
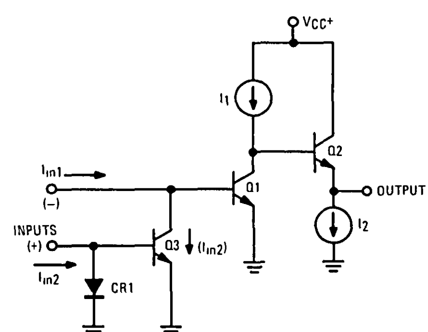


FIGURE 17 – OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage.

OPERATION AND APPLICATIONS (continued)

FIGURE 18 – A BASIC OPERATIONAL AMPLIFIER

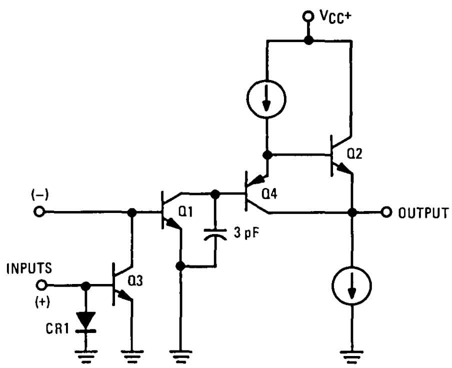
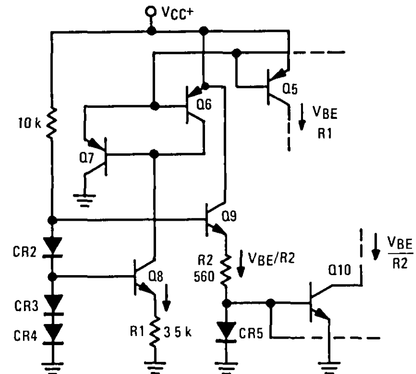


FIGURE 19 – BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. *Output Q-Point Biasing*

   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4. The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the *maximum loop gain for any particular configuration.* It is desirable that the noninverting input current be in the 5 μA to 100 μA range.

   B V_{CC} Reference Voltage (see Figures 3 and 4)

   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 5 μA to 100 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows for maximum dynamic range of the output voltage.

   C. Reference Voltage other than V_{CC} (See Figure 20).

   The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_r between 5 μA and 100 μA) the output dc level will be equal to V_r Neglecting error terms, the expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(V_r)\ (R_f)}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0 7 Vdc @ +25°C).

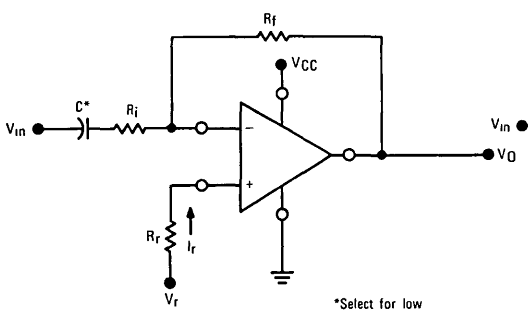
   The error terms not appearing in the above equation can cause the dc operating point to vary up to 20% from the expected value. Error terms are minimized by setting the input current within the range of 5 μA to 100 μA.

2. Gain Determination

   A. Inverting Amplifier

   The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

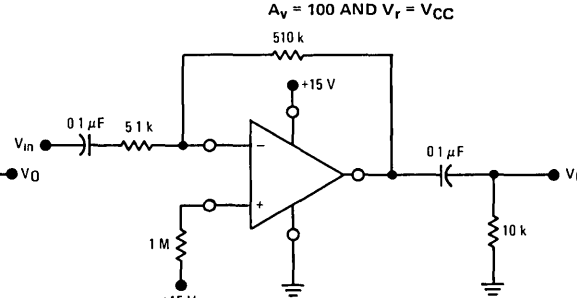
FIGURE 20 – INVERTING AMPLIFIER WITH ARBITRARY REFERENCE



$$V_O = \frac{V_r R_f}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

*Select for low frequency response.

FIGURE 21 – INVERTING AMPLIFIER WITH $A_v = 100$ AND $V_r = V_{CC}$



$A_v = 100$

$f_L = 300$ Hz, $f_H = 50$ kHz

NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device The limitation is less severe if the device is direct coupled In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier

$$A_V = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation The amplifier unity gain bandwidth is typically 5 0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 500 kHz with 20 dB of closed loop gain or 50 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3 0 pF.

B Noninverting Amplifier

Although recommended as an inverting amplifier, the MC 3401 may be used in the noninverting mode (see Figure 4). The amplifier gain in this configuration is subject to the same error terms that affect the output Q point biasing so the gain may deviate as much as ±20% from that expected. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes The noninverting gain expression is given by·

$$A_V = \frac{R_f}{R_i + \frac{26}{I_r\,(mA)}} \quad \pm 20\%.$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For, R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100 This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop

3

TYPICAL APPLICATIONS

FIGURE 22 – AMPLIFIER AND DRIVER FOR A 50-OHM LINE

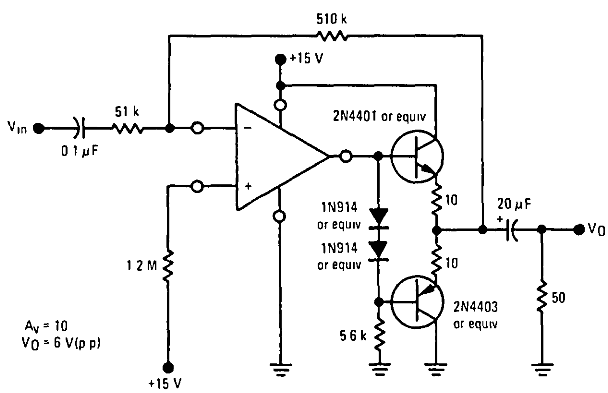
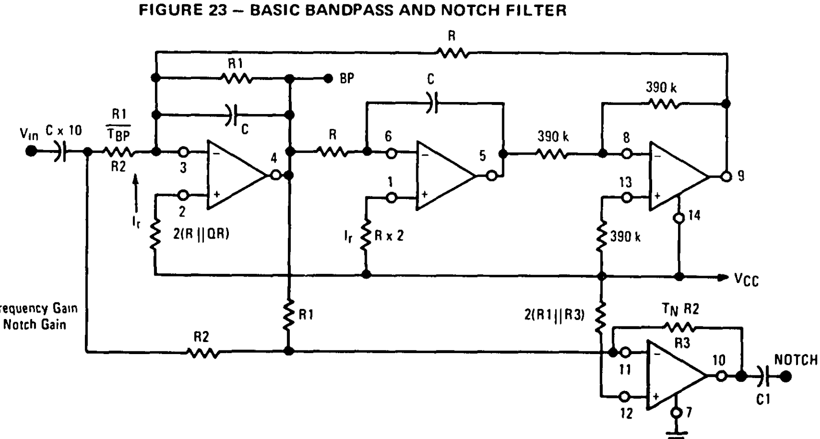


FIGURE 23 – BASIC BANDPASS AND NOTCH FILTER



TBP = Center Frequency Gain
TN = Passband Notch Gain

$\omega 0 = \frac{1}{RC}$

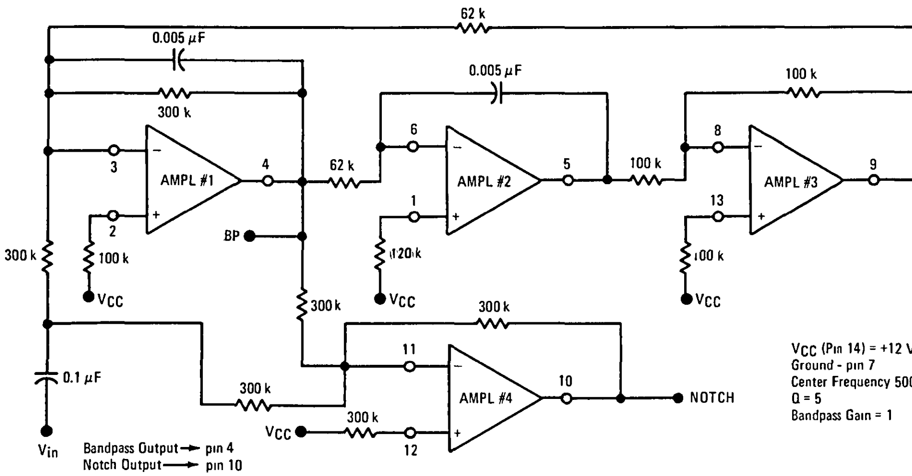
R1 = QR

$R2 = \frac{R1}{T_{BP}}$

R3 = T_N R2

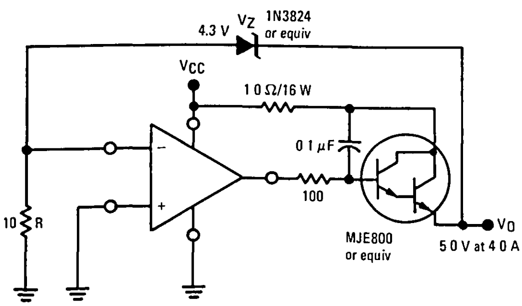
TYPICAL APPLICATIONS (continued)

FIGURE 24 – BANDPASS AND NOTCH FILTER



V_{CC} (Pin 14) = +12 Volts
Ground - pin 7
Center Frequency 500 Hz
Q = 5
Bandpass Gain = 1

FIGURE 25 – VOLTAGE REGULATOR

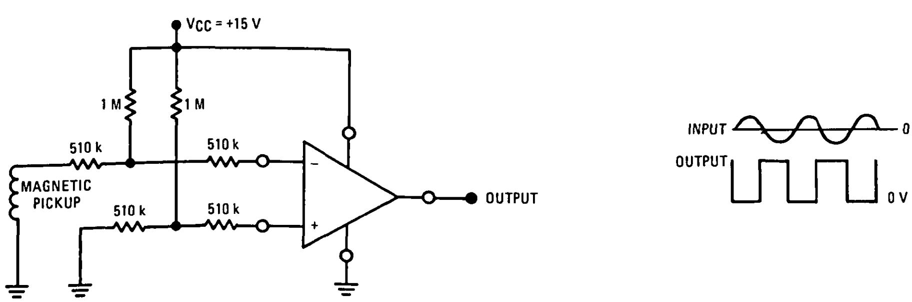


$V_O = V_Z + 0\ 6$ Vdc

NOTE 1. R is used to bias the zener.

NOTE 2 If the Zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈ 2 0 mV/°C), the output is zero-TC. A 7 0-Volt Zener will give approximately zero-TC.

FIGURE 26 – ZERO CROSSING DETECTOR



MC3403P,L
MC3503L
MC3303P,L

Specifications and Applications Information

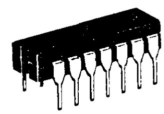
QUAD LOW POWER OPERATIONAL AMPLIFIERS

The MC3503 is a low-cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741. However, the MC3503 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one third of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

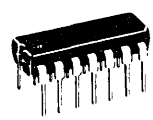
- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

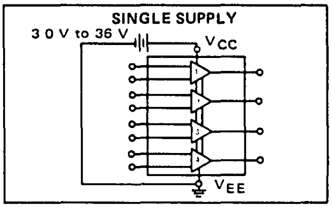


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

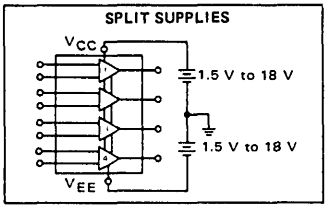


P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3403 and MC3303 only)

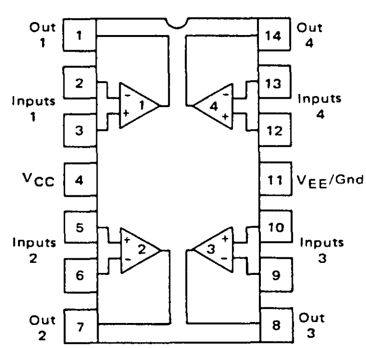
SINGLE SUPPLY



SPLIT SUPPLIES



PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	36	
Split Supplies	V_{CC}	+18	
	V_{EE}	-18	
Input Differential Voltage Range (1)	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range (1) (2)	V_{ICR}	±18	Vdc
Storage Temperature Range	T_{stg}		°C
Ceramic Package		-65 to +150	
Plastic Package		-55 to +125	
Operating Ambient Temperature Range	T_A		°C
MC3503		-55 to +125	
MC3403		0 to +70	
MC3303		-40 to +85	
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	

(1) Split Power Supplies.
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

Type	Temperature Range	Package
MC3303L	-40°C to +85°C	Ceramic DIP
MC3303P	-40°C to +85°C	Plastic DIP
MC3403L	0°C to +70°C	Ceramic DIP
MC3403P	0°C to +70°C	Plastic DIP
MC3503L	-55°C to +125°C	Ceramic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V for MC3503, MC3403; V_{CC} = +14 V, V_{EE} = Gnd for MCC3303. T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC3503 Min	MC3503 Typ	MC3503 Max	MC3403 Min	MC3403 Typ	MC3403 Max	MC3303 Min	MC3303 Typ	MC3303 Max	Unit
Input Offset Voltage $T_A = T_{high}$ to T_{low} (1)	V_{IO}	– –	2 0 –	5 0 6 0	– –	2 0 –	10 12	– –	2 0 –	8 0 10	mV
Input Offset Current $T_A = T_{high}$ to T_{low}	I_{IO}	– –	30 –	50 200	– –	30 –	50 200	– –	30 –	75 250	nA
Large Signal Open-Loop Voltage Gain V_O = ±10 V, R_L = 2 0 kΩ, $T_A = T_{high}$ to T_{low}	A_{VOL}	50 25	200 300	– –	20 15	200 –	– –	20 15	200 –	– –	V/mV
Input Bias Current $T_A = T_{high}$ to T_{low}	I_{IB}	– –	-200 -300	-500 -1500	– –	-200 –	-500 -800	– –	-200 –	-500 -1000	nA
Output Impedance f = 20 Hz	z_o	–	75	–	–	75	–	–	75	–	Ω
Input Impedance f = 20 Hz	z_i	0 3	1 0	–	0 3	1 0	–	0 3	1 0	–	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2 0 kΩ R_L = 2 0 kΩ, $T_A = T_{high}$ to T_{low}	V_{OR}	±12 ±10 ±10	±13 5 ±13 –	– – –	±12 ±10 ±10	±13 5 ±13 –	– – –	+12 +10 +10	+12 5 +12 –	– – –	V
Input Common-Mode Voltage Range	V_{ICR}	+13 V -V_{EE}	+13 5 V -V_{EE}	–	+13 V -V_{EE}	+13 5 V -V_{EE}	–	+12 V -V_{EE}	+12 5 V -V_{EE}	–	V
Common-Mode Rejection Ratio R_S ≤ 10 kΩ	CMRR	70	90	–	70	90	–	70	90	–	dB
Power Supply Current (V_O = 0) R_L = ∞	I_{CC}, I_{EE}	–	2 8	4 0	–	2 8	7 0	–	2 8	7 0	mA
Individual Output Short-Circuit Current (2)	I_{OS}±	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	–	30	150	µV/V
Negative Power Supply Rejection Ratio	PSRR-	–	30	150	–	30	150	–	–	–	µV/V
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	µV/°C
Power Bandwidth A_V = 1, R_L = 2 0 kΩ, V_o = 20 V(p-p), THD = 5%	BW_p	–	9 0	–	–	9 0	–	–	9 0	–	kHz
Small Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_o = 50 mV	BW	–	1 0	–	–	1 0	–	–	1 0	–	MHz
Slew Rate A_V = 1, V_i = -10 V to +10 V	SR	–	0 6	–	–	0 6	–	–	0 6	–	V/µs
Rise Time A_V = 1, R_L = 10 kΩ, V_o = 50 mV	t_{TLH}	–	0 35	–	–	0 35	–	–	0 35	–	µs
Fall Time A_V = 1, R_L = 10 kΩ, V_o = 50 mV	t_{THL}	–	0 35	–	–	0 35	–	–	0 35	–	µs
Overshoot A_V = 1, R_L = 10 kΩ, V_o = 50 mV	OS	–	20	–	–	20	–	–	20	–	%
Phase Margin A_V = 1, R_L = 2 0 kΩ, C_L = 200 pF	ϕm	–	60	–	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mVp-p, V_{out} = 2 0 Vp-p, f = 10 kHz)	–	–	1 0	–	–	1 0	–	–	1 0	–	%

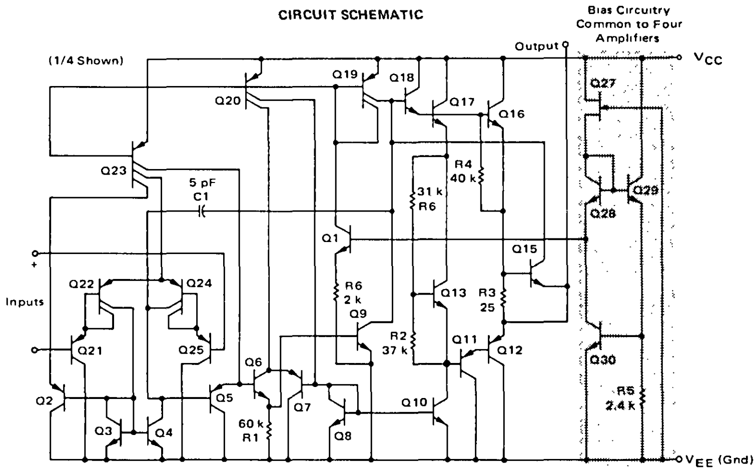
(1) T_{high} = 125°C for MC3503, 70°C for MC3403, 85°C for MC3303
T_{low} = -55°C for MC3503, 0°C for MC3403, -40°C for MC3303

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

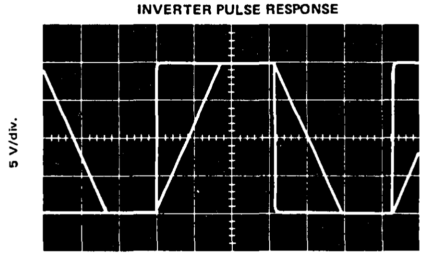
Characteristic	Symbol	MC3503 Min	MC3503 Typ	MC3503 Max	MC3403 Min	MC3403 Typ	MC3403 Max	MC3303 Min	MC3303 Typ	MC3303 Max	Unit
Input Offset Voltage	V_{IO}	–	2 0	5 0	–	2 0	10	–	–	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	–	-500	nA
Large Signal Open-Loop Voltage Gain R_L = 2 0 kΩ	A_{VOL}	10	200	–	10	200	–	10	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	–	–	150	µV/V
Output Voltage Range (3) R_L = 10 kΩ, V_{CC} = 5 0 V R_L = 10 kΩ, 5 0 V ≤ V_{CC} ≤ 30 V	V_{OR}	3 3 V_{CC}-1 7	3 5 V_{CC}-1 5	– –	3 3 V_{CC}-1 7	3 5 V_{CC}-1 5	– –	3 3 V_{CC}-1 7	3 5 V_{CC}-1 5	– –	Vp-p
Power Supply Current	I_{CC}	–	2 5	4 0	–	2 5	7 0	–	2 5	7 0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	-120	–	–	-120	–	–	-120	–	dB

(2) Not to exceed maximum package power dissipation.
(3) Output will swing to ground

CIRCUIT SCHEMATIC



INVERTER PULSE RESPONSE



CIRCUIT DESCRIPTION

The MC3503/3403/3303 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

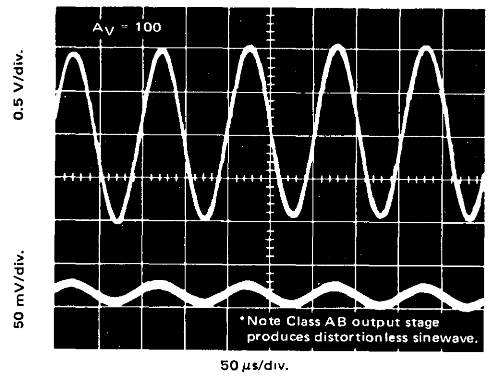


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

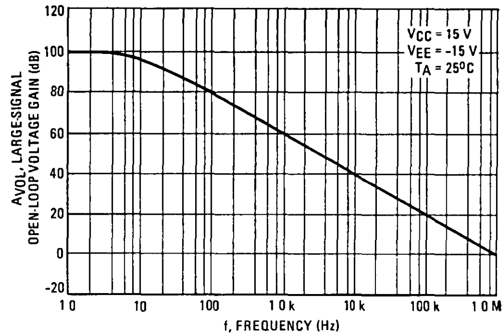


FIGURE 3 – POWER BANDWIDTH

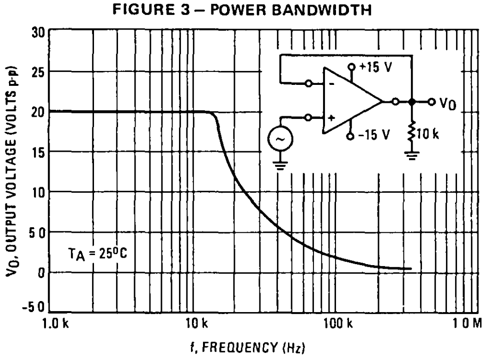


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

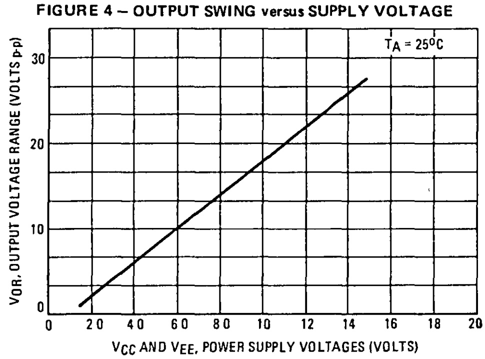


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

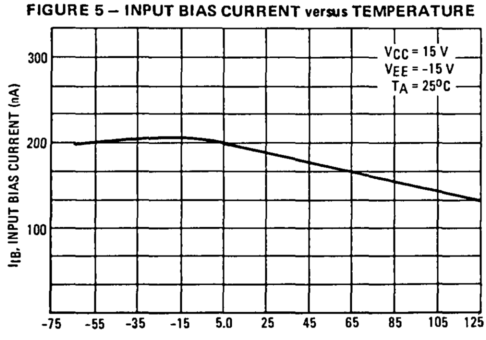
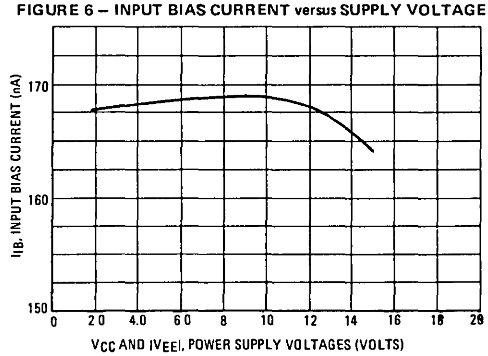


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

FIGURE 7 – VOLTAGE REFERENCE

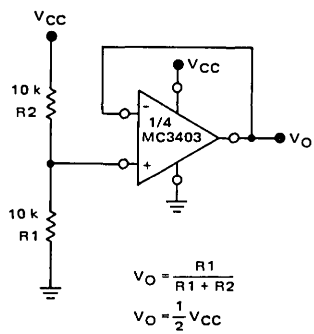


FIGURE 8 – WEIN BRIDGE OSCILLATOR

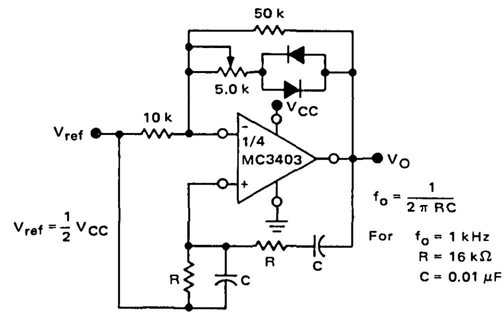


FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

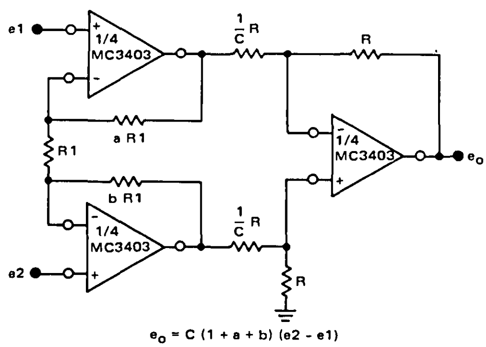


FIGURE 10 – COMPARATOR WITH HYSTERESIS

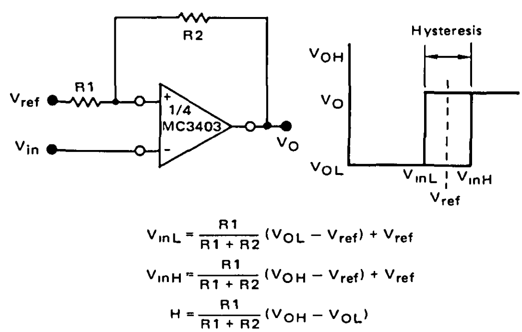


FIGURE 11 – BI-QUAD FILTER

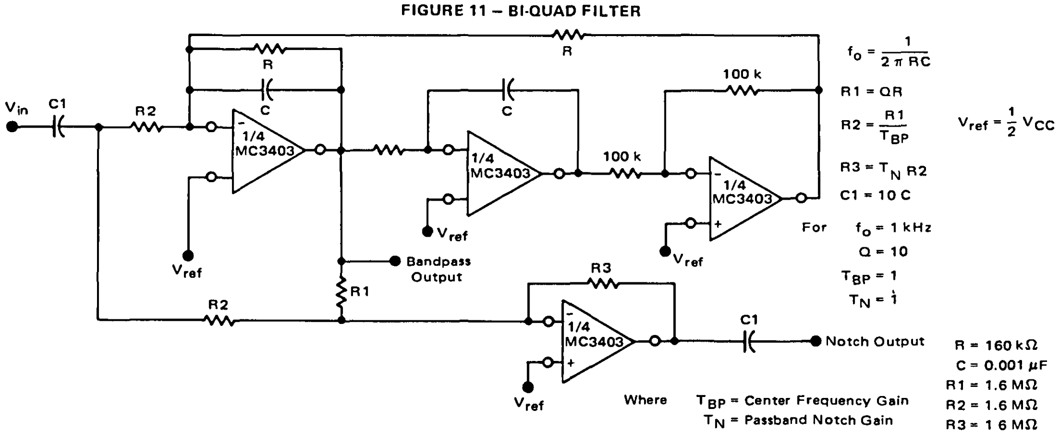
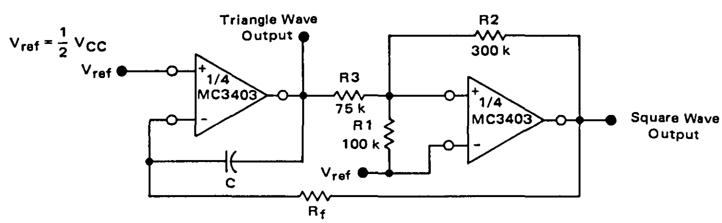
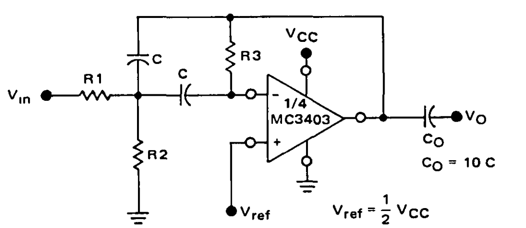


FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + RC}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then.

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R5}{4Q^2\,R1 - R5}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3358P1	−40°C to +85°C	Plastic DIP
MC3458G	0°C to +70°C	Metal Can
MC3458P1	0°C to +70°C	Plastic DIP
MC3458U	0°C to +70°C	Ceramic DIP
MC3558G	−55°C to +125°C	Metal Can
MC3558U	−55°C to +125°C	Ceramic DIP

MC3458
MC3558
MC3358

Specifications and Applications Information

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

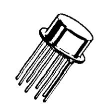
DUAL LOW POWER OPERATIONAL AMPLIFIERS

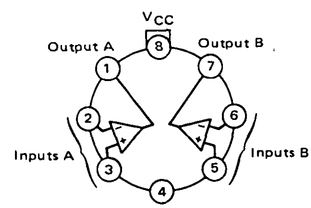
Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The MC3558 Series is equivalent to one-half of a MC3503.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation 3.0 to 36 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Class AB Output Stage for Minimum Crossover Distortion
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1558

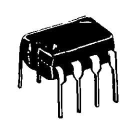
G SUFFIX
METAL PACKAGE
CASE 601



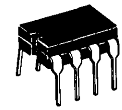


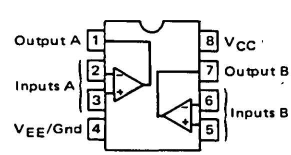
(TOP VIEW)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3458, MC3358 only)



U SUFFIX
CERAMIC PACKAGE
CASE 693





(TOP VIEW)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	36	
Split Supplies	V_{CC}	+18	
	V_{EE}	-18	
Input Differential Voltage Range (1)	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	±15	Vdc
Input Forward Current (V_I < -0.3 V)	I_{IF}	50	mA
Junction Temperature	T_J		°C
Ceramic and Metal Packages		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}		°C
Ceramic and Metal Packages		-65 to +150	
Plastic Package		-55 to +125	
Operating Ambient Temperature Range	T_A		°C
MC3558		-55 to +125	
MC3458		0 to +70	
MC3358		-40 to +85	

(1) Split Power Supplies

(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (For MC3558, MC3458, V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted) (For MC3358, V_{CC} = +14 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	MC3558 Min	MC3558 Typ	MC3558 Max	MC3458 Min	MC3458 Typ	MC3458 Max	MC3358 Min	MC3358 Typ	MC3358 Max	Unit
Input Offset Voltage T_A = T_{high} to T_{low} (1)	V_{IO}	– –	2 0 –	5 0 6 0	– –	2 0 –	10 12	– –	2 0 –	8 0 10	mV
Input Offset Current T_A = T_{high} to T_{low}	I_{IO}	– –	30 –	50 200	– –	30 –	50 200	– –	30 –	75 250	nA
Large Signal Open-Loop Voltage Gain V_O = ±10 V, R_L = 2 0 kΩ, T_A = T_{high} to T_{low}	A_{VOL}	 50 25	 200 300	 – –	 20 15	 200 –	 – –	 20 15	 200 –	 – –	V/mV
Input Bias Current T_A = T_{high} to T_{low}	I_{IB}	– –	-200 -300	-500 -1500	– –	-200 –	-500 -800	– –	-200 –	-500 -1000	nA
Output Impedance f = 20 Hz	z_o	–	75	–	–	75	–	–	75	–	Ω
Input Impedance f = 20 Hz	z_i	0 3	1 0	–	0 3	1 0	–	0 3	1 0	–	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2 0 kΩ R_L = 2 0 kΩ, T_A = T_{high} to T_{low}	V_{OR}	 ±12 ±10 ±10	 ±13 5 ±13 –	 – – –	 ±12 ±10 ±10	 ±13 5 ±13 –	 – – –	 12 10 10	 12 5 12 –	 – – –	V
Input Common Mode Voltage Range	V_{ICR}	+13 V -V_{EE}	+13 5 V -V_{EE}	–	+13 V -V_{EE}	+13 5V -V_{EE}	–	+12 V -V_{EE}	+12 5V -V_{EE}	–	V
Common-Mode Rejection Ratio R_S ≤ 10 kΩ	CMRR	70	90	–	70	90	–	70	90	–	dB
Power Supply Current (V_o = 0) R_L = ∞	I_{CC},I_{EE}	–	1 6	2 2	–	1 6	3 7	–	1 6	3 7	mA
Individual Output Short Circuit Current (2)	I_{OS}	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	–	30	150	µV/V
Negative Power Supply Rejection Ratio	PSRR-	–	30	150	–	30	150	–	–	–	µV/V
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	µV/°C
Power Bandwidth A_V = 1, R_L = 2 0 kΩ, V_o = 20 V(p p), THD = 5%	BW_P	–	9 0	–	–	9 0	–	–	9 0	–	kHz
Small-Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_o = 50 mV	BW	–	1 0	–	–	1 0	–	–	1 0	–	MHz
Slew Rate A_V = 1, V_i = -10 V to +10 V	SR	–	0 6	–	–	0 6	–	–	0 6	–	V/µs
Rise Time A_V = 1, R_L = 10 kΩ, V_o = 50 mV	t_{TLH}	–	0 35	–	–	0 35	–	–	0 35	–	µs
Fall Time A_V = 1, R_L = 10 kΩ, V_o = 50 mV	t_{THL}	–	0 35	–	–	0 35	–	–	0 35	–	µs
Overshoot A_V = 1, R_L = 10 kΩ, V_o = 50 mV	OS	–	20	–	–	20	–	–	20	–	%
Phase Margin A_V = 1, R_L = 2 0 kΩ, C_L = 200 pF	φm	–	60	–	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mVp-p, V_{out} = 2 0 Vp p, f = 10 kHz)	–	–	1 0	–	–	1 0	–	–	1 0	–	%

(1) T_{high} = 125°C for MC3558, 70°C for MC3458, 85°C for MC3358
T_{low} = -55°C for MC3558, 0°C for MC3458, -40°C for MC3358

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

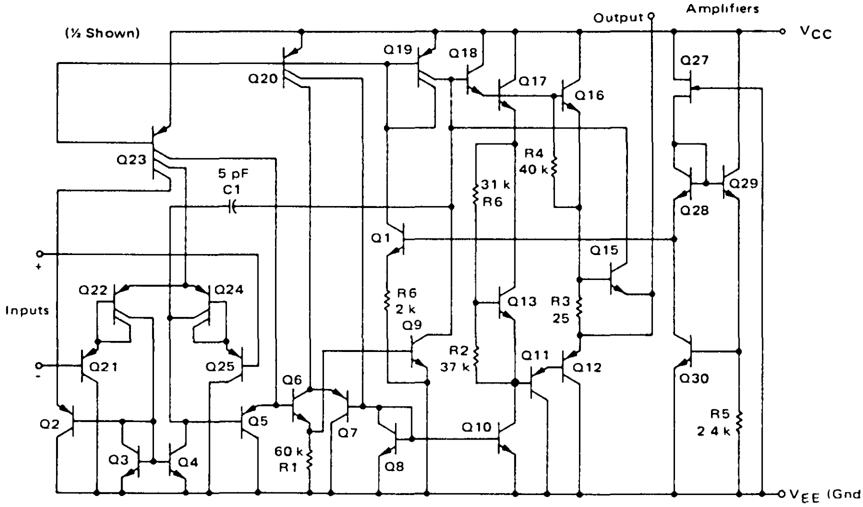
Characteristic	Symbol	MC3558 Min	MC3558 Typ	MC3558 Max	MC3458 Min	MC3458 Typ	MC3458 Max	MC3358 Min	MC3358 Typ	MC3358 Max	Unit
Input Offset Voltage	V_{IO}	–	2 0	5 0	–	2 0	10	–	2 0	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	–	-500	nA
Large-Signal Open Loop Voltage Gain R_L = 2 0 kΩ	A_{VOL}	20	200	–	20	200	–	20	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	–	–	150	µV/V
Output Voltage Range (3) R_L = 10 kΩ, V_{CC} = 5 0 V R_L = 10 kΩ, 5 0 V ≤ V_{CC} ≤ 30 V	V_{OR}	 3 3 –	 3 5 V_{CC}-1 7 V	 – –	 3.3 –	 3 5 V_{CC} -1 7 V	 – –	 3 3 –	 3.5 V_{CC} -1 7 V	 – –	Vp-p
Power Supply Current	I_{CC}	–	2 5	4 0	–	2 5	7 0	–	2 5	4 0	mA
Channel Separation f = 1 0 kHz to 20 kHz (Input Referenced)	–	–	-120	–	–	-120	–	–	-120	–	dB

(2) Not to exceed maximum package power dissipation
(3) Output will swing to ground

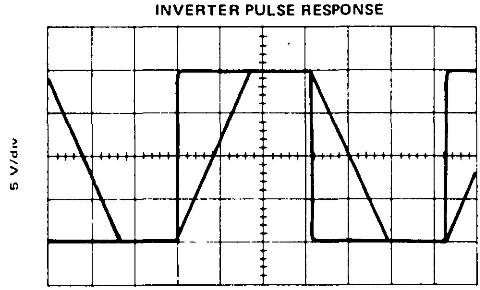
3

3

REPRESENTATIVE CIRCUIT SCHEMATIC



INVERTER PULSE RESPONSE



CIRCUIT DESCRIPTION

The MC3558 Series is made using two internally compensated, two-stage operational amplifiers The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

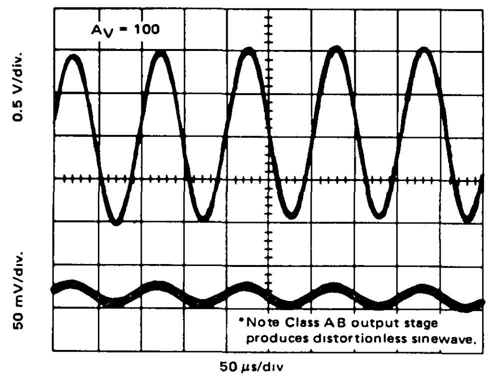


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

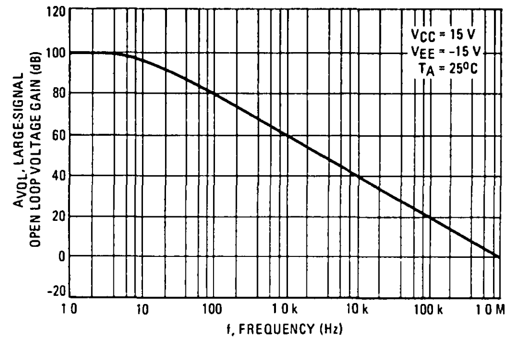


FIGURE 3 – POWER BANDWIDTH

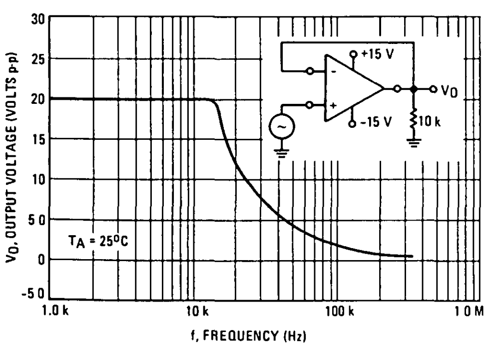


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

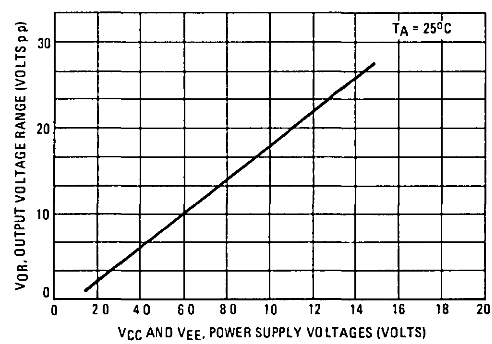


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

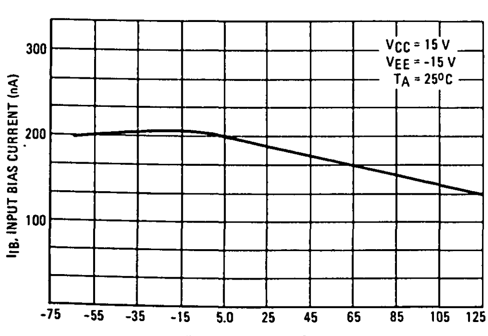
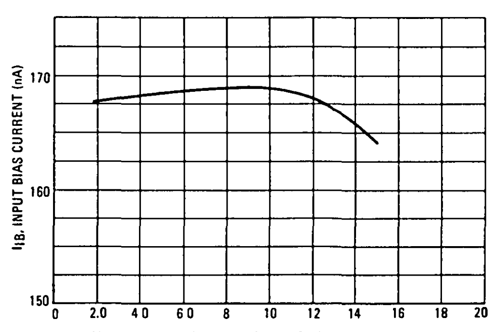


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



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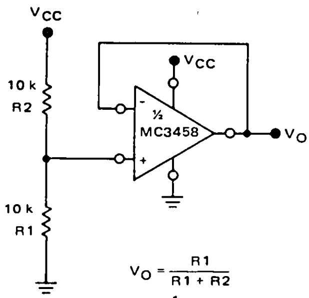
APPLICATIONS INFORMATION

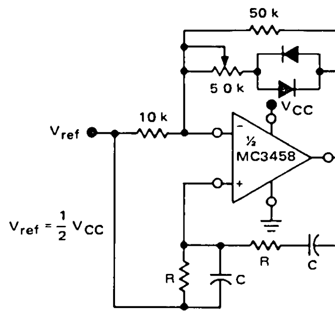
FIGURE 7 – VOLTAGE REFERENCE



$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 – WIEN BRIDGE OSCILLATOR

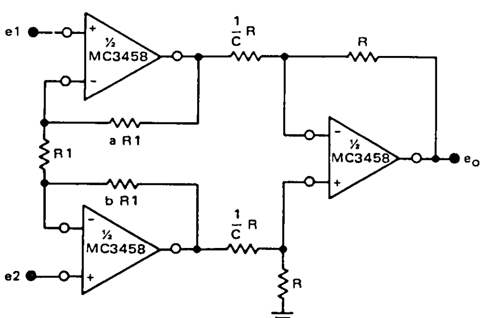


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2 \pi RC}$$

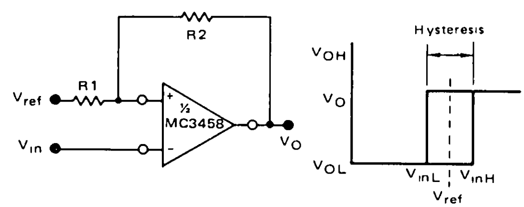
For f_o = 1 kHz
R = 16 kΩ
C = 0.01 µF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$$e_o = C\,(1 + a + b)\,(e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

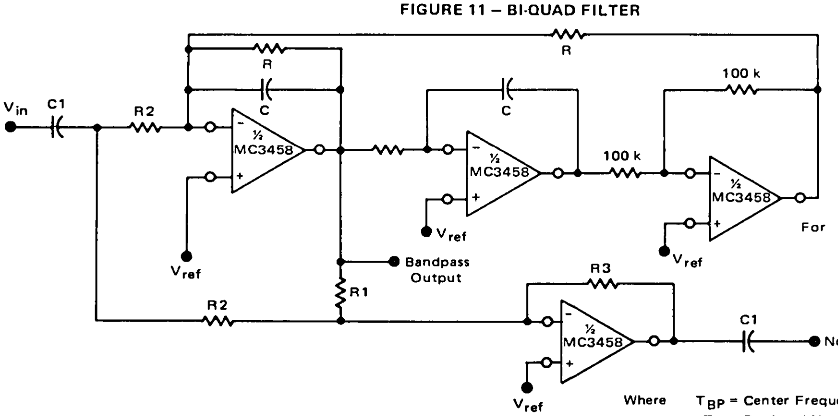


$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER



$$f_o = \frac{1}{2 \pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

$$V_{ref} = \frac{1}{2} V_{CC}$$

$R3 = T_N\,R2$

C1 = 10 C

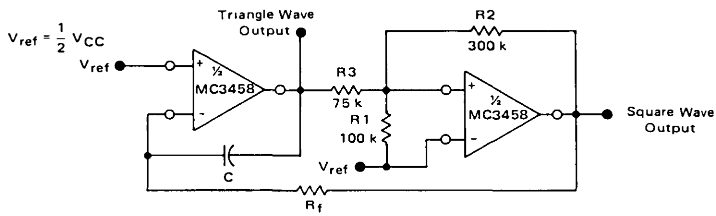
For f_o = 1 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 µF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

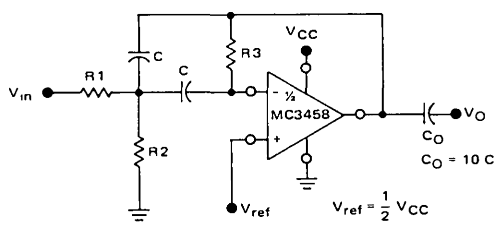
APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}.$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1 \qquad \text{Where } f_o \text{ and BW are expressed in Hz}$$

If source impedance varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters

MC3476

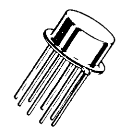
LOW-COST PROGRAMMABLE OPERATIONAL AMPLIFIER

The MC3476 is a low-cost selection of the popular, industry-standard MC1776 programmable operational amplifier. This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

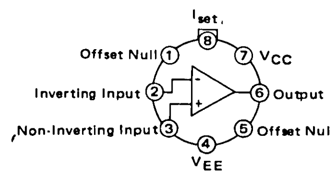
- ±6.0 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

LOW-COST PROGRAMMABLE OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



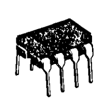
G SUFFIX
METAL PACKAGE
CASE 601

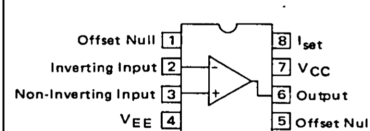


(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693





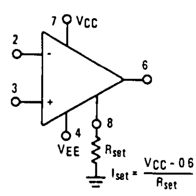
(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC3476G	0 to +70°C	Metal Can
MC3476P1	0 to +70°C	Plastic DIP
MC3476U	0 to +70°C	Ceramic DIP

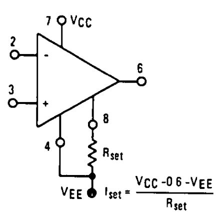
RESISTIVE PROGRAMMING (See Figure 1.)

R_{set} to GROUND



Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 10 µA	I_{set} = 15 µA
±6.0 V	560 kΩ	360 kΩ
±9.0 V	820 kΩ	560 kΩ
±12 V	1.0 MΩ	750 kΩ
±15 V	1.5 MΩ	1.0 MΩ

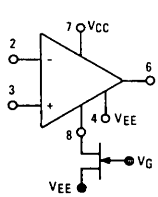
R_{set} to NEGATIVE SUPPLY



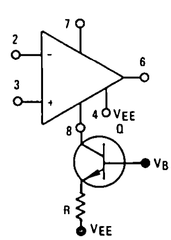
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 10 µA	I_{set} = 15 µA
±6.0 V	1.0 MΩ	820 kΩ
±9.0 V	1.8 MΩ	1.2 MΩ
±12 V	2.2 MΩ	1.5 MΩ
±15 V	2.7 MΩ	2.0 MΩ

ACTIVE PROGRAMMING

FET CURRENT SOURCE



BIPOLAR CURRENT SOURCE



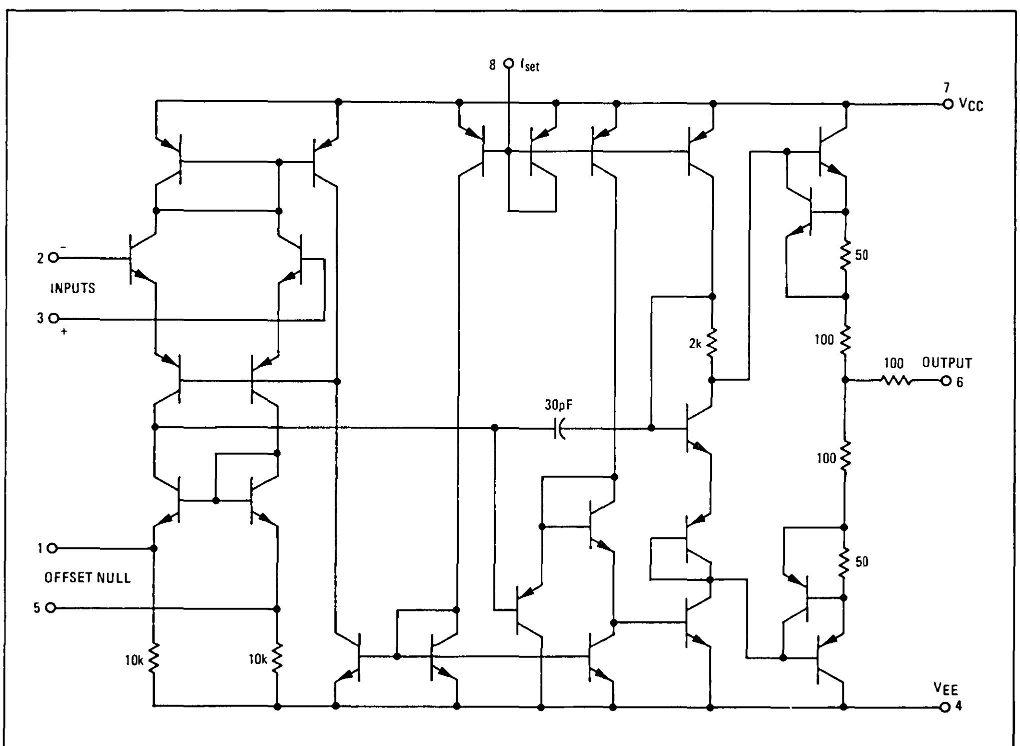
Pins not shown are not connected.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Input Differential Voltage Range	V_{IDR}	±30	Vdc
Input Common-Mode Voltage Range	V_{ICR}	V_{CC}, V_{EE}	Vdc
Offset Null to V_{EE} Voltage	$V_{off}-V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	200	µA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	(V_{CC}−0.6 V) to V_{CC}	Vdc
Output Short-Circuit Duration*	t_S	Indefinite	s
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperautre Range Metal and Ceramic Packages Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 175 150	°C

*Short-Circuit to ground with $I_{set} \leq 15$ µA. Rating applies up to ambient temperature of +70°C.

EQUIVALENT SCHEMATIC DIAGRAM



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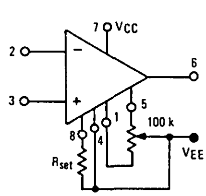
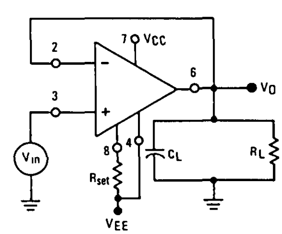
ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le$ 10 kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
0°C ≤ T_A ≤ 70°C		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	2.0	25	
T_A = 70°C		–	–	25	
T_A = 0°C		–	–	40	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	15	50	
T_A = 70°C		–	–	50	
T_A = 0°C		–	–	100	
Input Resistance	r_i	–	5.0	–	MΩ
Input Capacitance	C_i	–	2.0	–	pF
Input Common-Mode Voltage Range 0°C ≤ T_A ≤ 70°C	V_{ICR}	±10	–	–	V
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \ge$ 10 kΩ, V_O = ±10 V, T_A = +25°C		50 k	400 k	–	
$R_L \ge$ 10 kΩ, V_O = ±10 V, 0°C ≤ T_A ≤ 70°C		25 k	–	–	
Output Voltage Range	V_{OR}				V
$R_L \ge$ 10 kΩ, T_A = +25°C		±12	±13	–	
$R_L \ge$ 10 kΩ, 0°C ≤ T_A ≤ 70°C		±12	–	–	
Output Resistance	r_o	–	1.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	12	–	mA
Common-Mode Rejection Ratio $R_S \le$ 10 kΩ, 0°C ≤ T_A ≤ 70°C	CMRR	70	90	–	dB
Supply Voltage Rejection Ratio $R_S \le$ 10 kΩ, 0°C ≤ T_A ≤ 70°C	PSRR	–	25	200	μV/V
Supply Current	I_{CC}, I_{EE}				μA
T_A = +25°C		–	160	200	
0°C ≤ T_A ≤ 70°C		–	–	225	
Power Dissipation	P_D				mW
T_A = +25°C		–	4.8	6.0	
0°C ≤ T_A ≤ 70°C		–	–	6.75	
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \ge$ 10 kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	0.35	–	μs
Overshoot	OS	–	10	–	%
Slew Rate ($R_L \ge$ 10 kΩ)	SR	–	0.8	–	V/μs

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT-RESPONSE TEST CIRCUIT



Pins not shown are not connected

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

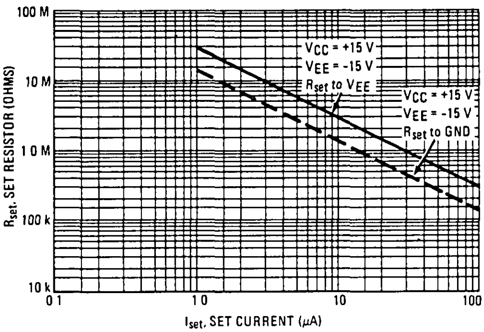


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

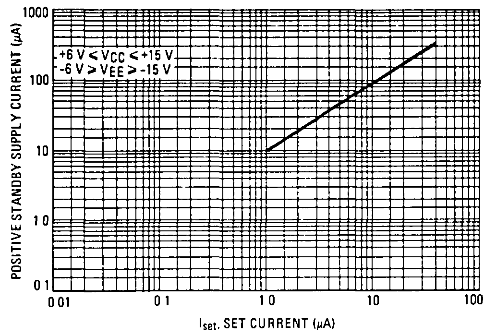


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

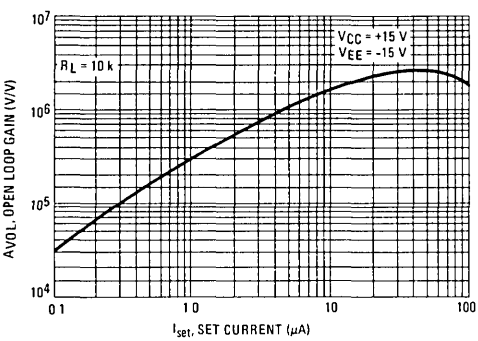


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

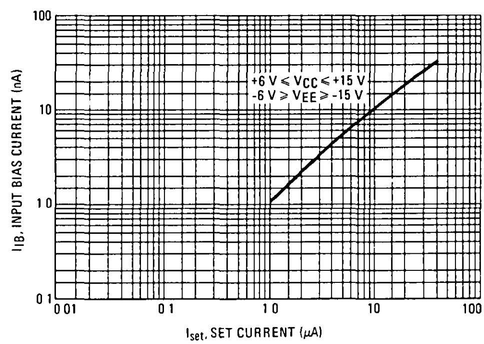


FIGURE 5 – SLEW RATE versus SET CURRENT

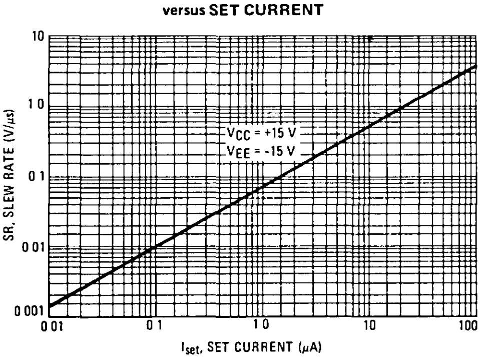
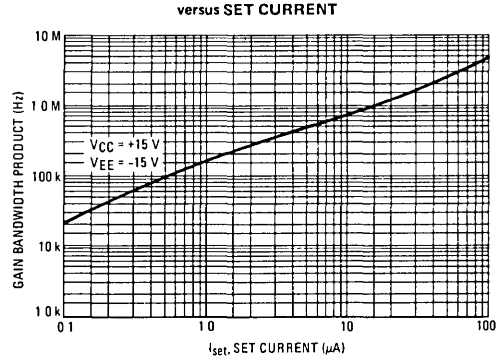


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



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TYPICAL CHARACTERISTICS (continued)
(T_A = +25°C unless otherwise noted.)

FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

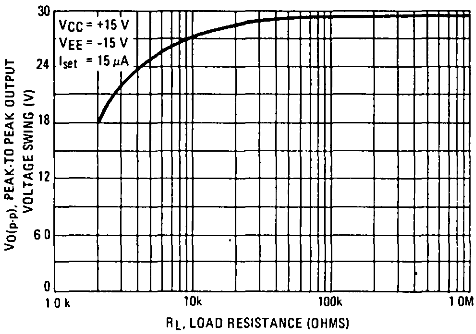
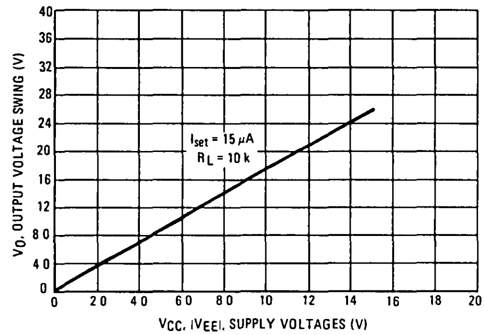


FIGURE 8 – OUTPUT SWING versus SUPPLY VOLTAGE



MC4558, MC4558AC, MC4558C, MC4558N, MC4558NC

DUAL WIDEBAND OPERATIONAL AMPLIFIER

The MC4558, MC4558AC, and MC4558C combine all the outstanding features of the MC1458 and, in addition, possess three times the unity gain bandwidth of the industry standard.

- **2.5 MHz Unity Gain Bandwidth Guaranteed on MC4558 and MC4558AC**
- **2 MHz Unity Gain Bandwidth Guaranteed on MC4558C**
- Internally Compensated
- Short-Circuit Protection
- Gain and Phase Match between Amplifiers
- Low Power Consumption
- Low Noise Selections Offered – N Suffix

DUAL WIDE BANDWIDTH OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

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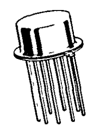
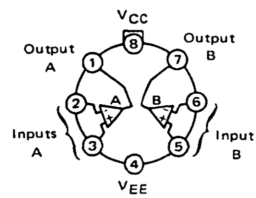
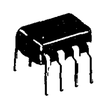


G SUFFIX
METAL PACKAGE
CASE 601

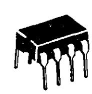


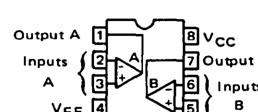
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693





(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC4558, NG	-55 to +125°C	Metal Can
MC4558NU, U	-55 to +125°C	Ceramic DIP
MC4558CG, NCG	0 to +70°C	Metal Can
MC4558ACP1, CP1, NCP1	0 to +70°C	Plastic DIP
MC4558CU, NCU	0 to +70°C	Ceramic DIP

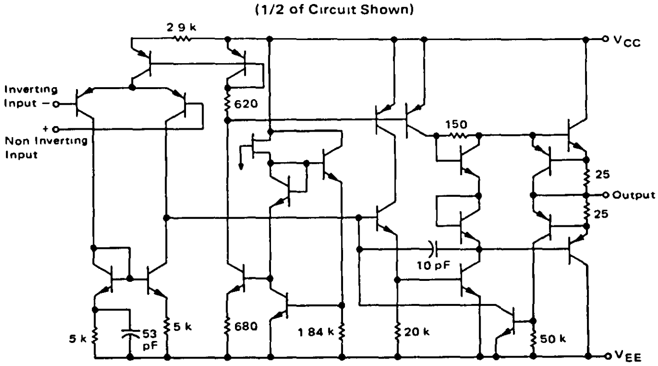
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC4558 MC4558AC	MC4558C	Unit
Power Supply Voltage	V_{CC}	+22	+18	Vdc
	V_{EE}	-22	-18	Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short-Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	See Ordering Information Below		
Storage Temperature Range	T_{stg}			°C
Metal and Ceramic Packages		-65 to +150		
Plastic Package		-55 to +125		
Junction Temperature	T_J			°C
Metal and Ceramic Packages		175		
Plastic Package		150		

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Short circuit may be to ground or either supply.

EQUIVALENT CIRCUIT SCHEMATIC
(1/2 of Circuit Shown)



FREQUENCY CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	MC4558, MC4558AC			MC4558C			Unit
		Min	Typ	Max	Min	Typ	Max	
Unity Gain Bandwidth	BW	2.5	2.8	–	2.0	2.8	–	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC4558, MC4558AC Min	MC4558, MC4558AC Typ	MC4558, MC4558AC Max	MC4558C Min	MC4558C Typ	MC4558C Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current†	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_V	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio (R_S ≤ 10 kΩ)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 kΩ)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing	V_O							V
(R_L ≥ 10 kΩ)		±12	±14	–	±12	±14	–	
(R_L ≥ 2 kΩ)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{os}	10	20	40	10	20	40	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.0	–	2.3	5.6	mA
Power Consumption (Both Amplifiers)	P_C	–	70	150	–	70	170	mW
Transient Response (Unity Gain)								
(V_I = 20 mV, R_L ≥ 2 kΩ, C_L ≤ 100 pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, R_L ≥ 2 kΩ, C_L ≤ 100 pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, R_L ≥ 2 kΩ, C_L ≤ 100 pF) Slew Rate	SR	1.5	1.6	–	1.0	1.6	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = *T_{high} to T_{low} unless otherwise noted).

Characteristic	Symbol	MC4558, MC4558AC Min	MC4558, MC4558AC Typ	MC4558, MC4558AC Max	MC4558C Min	MC4558C Typ	MC4558C Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = T_{high})		–	7.0	200	–	–	–	
(T_A = T_{low})		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
(T_A = T_{high})		–	30	500	–	–	–	
(T_A = T_{low})		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Common Mode Rejection Ratio (R_S ≤ 10 kΩ)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 kΩ)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing	V_O							V
(R_L ≥ 10 kΩ)		±12	±14	–	±12	±14	–	
(R_L ≥ 2 kΩ)		±10	±13	–	±10	±13	–	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2 kΩ)	A_V	25	–	–	15	–	–	V/mV
Supply Currents (Both Amplifiers)	I_D							mA
(T_A = T_{high})		–	–	4.5	–	–	5.0	
(T_A = T_{low})		–	–	6.0	–	–	6.7	
Power Consumption (Both Amplifiers)	P_C							mW
(T_A = T_{high})		–	–	135	–	–	150	
(T_A = T_{low})		–	–	180	–	–	200	

*T_{high} = 125°C for MC4558 and 70°C for MC4558C and MC4558AC.
T_{low} = −55°C for MC4558 and 0°C for MC4558C and MC4558AC.
† I_{IB} is out of the amplifier due to PNP input transistors.

NOISE CHARACTERISTICS (Applies for MC4558N and MC4558NC only, V_{CC} = 15 V, V_{EE} = -15 V, T_A = 25°C)

Characteristic	Symbol	MC4558N			MC4558NC			Unit
		Min	Typ	Max	Min	Typ	Max	
Burst Noise (Popcorn Noise) (BW = 1.0 Hz to 1.0 kHz, t = 10 s, R_S = 100 kΩ) (Input Referenced)	E_n	–	–	20	–	–	20	μVpeak

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

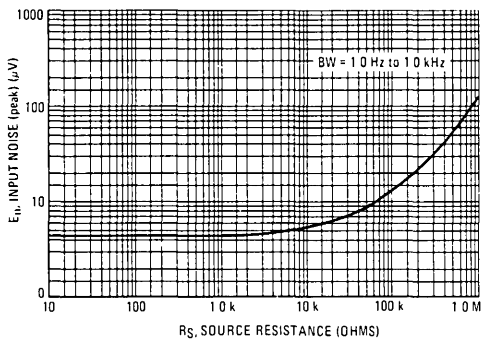


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

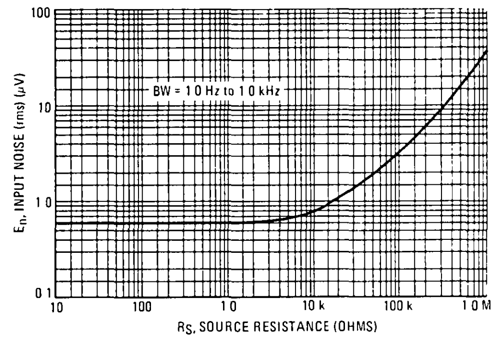


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

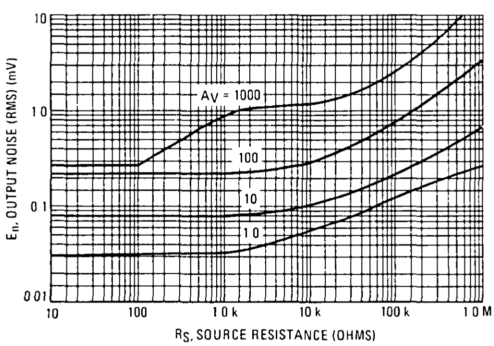


FIGURE 4 – SPECTRAL NOISE DENSITY

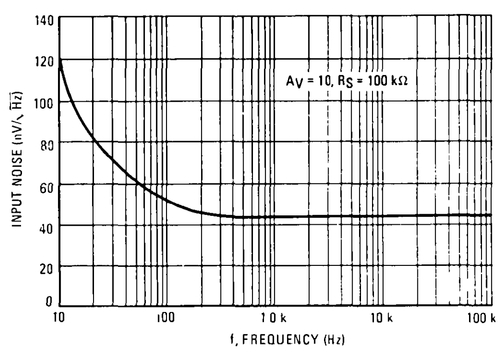
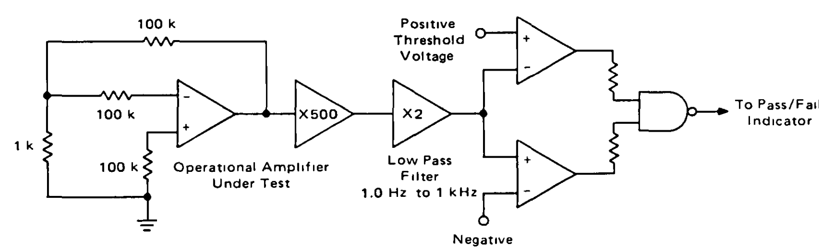


FIGURE 5 – BURST NOISE TEST CIRCUIT (N Suffixed Devices Only)



For applications where low noise performance is essential, selected devices denoted by an N suffix are offered. These units have been 100% tested for burst noise pulses on a special noise test system. Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

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FIGURE 6 – OPEN LOOP FREQUENCY RESPONSE

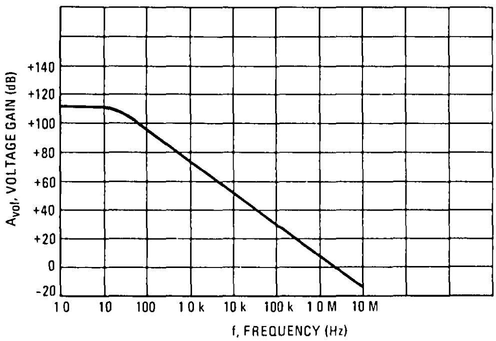


FIGURE 7 – PHASE MARGIN versus FREQUENCY

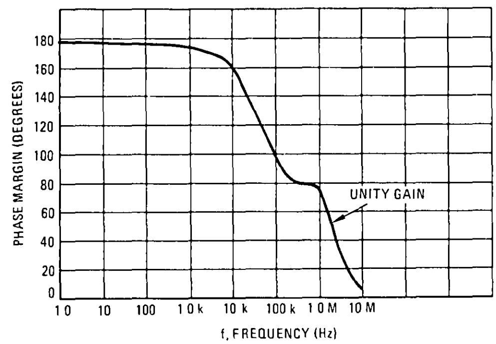


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

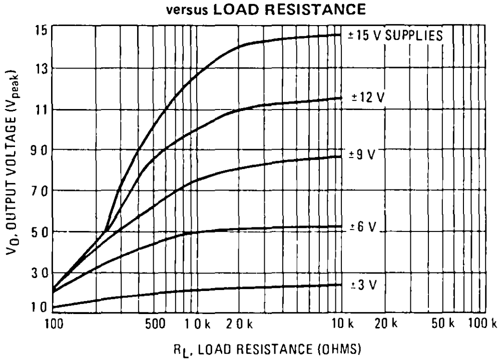


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

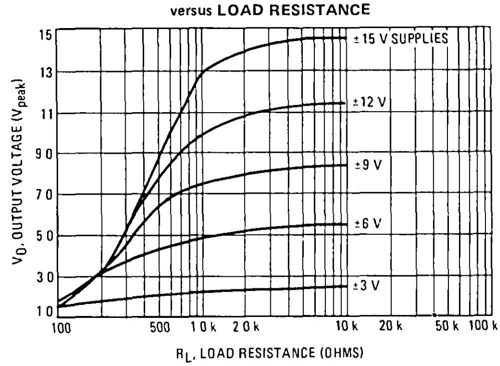


FIGURE 10 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

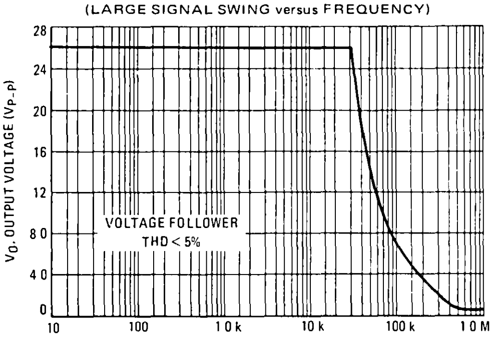
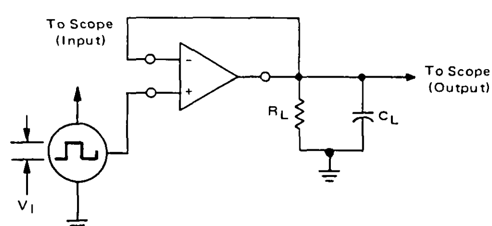


FIGURE 11 – TRANSIENT RESPONSE TEST CIRCUIT



ORDERING INFORMATION

Device	Temperature Range	Package
MC4741L	−55°C to +125°C	Ceramic DIP
MC4741CL	0°C to +70°C	Ceramic DIP
MC4741CP	0°C to +70°C	Plastic DIP

MC4741
MC4741C

QUAD MC1741
DIFFERENTIAL INPUT
OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

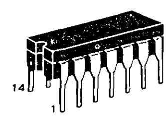
Specifications and Applications Information

QUAD MC1741 OPERATIONAL AMPLIFIERS

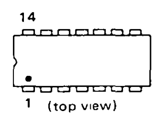
The MC4741 series is a true quad MC1741 Integrated on a single monolithic chip are four independent, low-power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance.

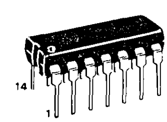
The MC4741 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Class AB Output Stage Eliminates Crossover Distortion
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)



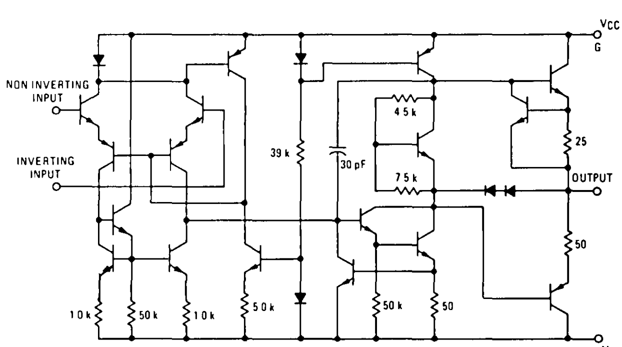
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



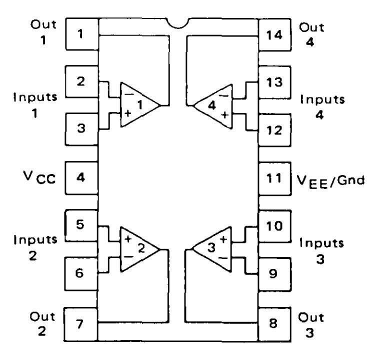


P SUFFIX
PLASTIC PACKAGE
CASE 646

EQUIVALENT CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)



PIN CONNECTIONS



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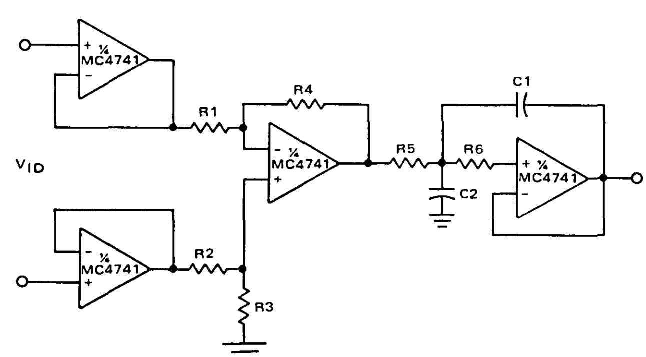
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC4741	MC4741C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc Vdc
Input Differential Voltage	V_{ID}	±44	±36	Volts
Input Common Mode Voltage	V_{ICM}	±22	±18	Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150		°C

TYPICAL APPLICATION

HIGH IMPEDANCE INSTRUMENTATION BUFFER/FILTER



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC4741			MC4741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L ≥ 2.0 k)	A_v	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing	V_O							V
(R_L ≥ 10 k)		±12	±14	–	±12	±14	–	
(R_L ≥ 2 k)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{OS}	–	20	–	–	20	–	mA
Supply Current – (All Amplifiers)	I_D	–	2.4	4.0	–	3.5	7.0	mA
Power Consumption (All Amplifiers)	P_C	–	72	120	–	105	210	mW
Transient Response (Unity Gain – Non-Inverting)								
(V_I = 20 mV, R_L ≥ 2 k, C_L ≤ 100 pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, R_L ≥ 2 k, C_L ≤ 100 pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, R_L ≥ 2 k, C_L ≤ 100 pF) Slew Rate	SR	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = *T_{high} to T_{low} unless otherwise noted.)

Characteristic	Symbol	MC4741			MC4741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = 125°C)		–	7.0	200	–	–	–	
(T_A = -55°C)		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
(T_A = 125°C)		–	30	500	–	–	–	
(T_A = -55°C)		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing	V_O							V
(R_L ≥ 10 k)		±12	±14	–	–	–	–	
(R_L ≥ 2 k)		±10	±13	–	±10	±13	–	
Large Signal Voltage Gain (R_L ≥ 2 k, V_{out} = ±10 V)	A_v	25	–	–	15	–	–	V/mV
Supply Currents – (All Amplifiers)	I_D							mA
(T_A = 125°C)		–	2.4	3.4	–	–	–	
(T_A = -55°C)		–	3.6	5.0	–	–	–	
Power Consumption (T_A = +125°C)	P_C	–	72	102	–	–	–	mW
(All Amplifiers) (T_A = -55°C)		–	108	150	–	–	–	

*T_{high} = 125°C for MC4741 and 70°C for MC4741C
T_{low} = -55°C for MC4741 and 0°C for MC4741C

3

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 1 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

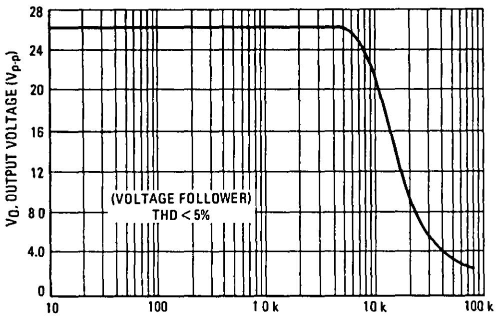


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

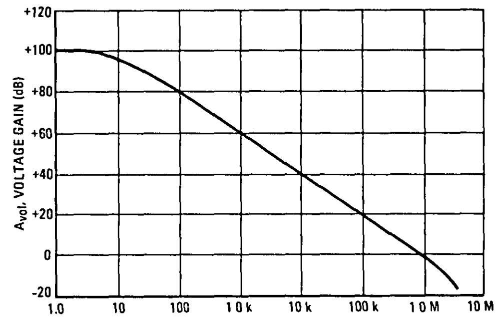


FIGURE 3 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

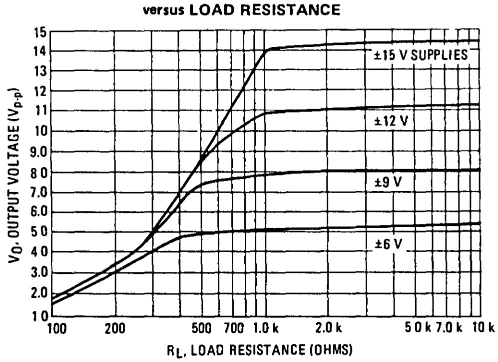


FIGURE 4 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

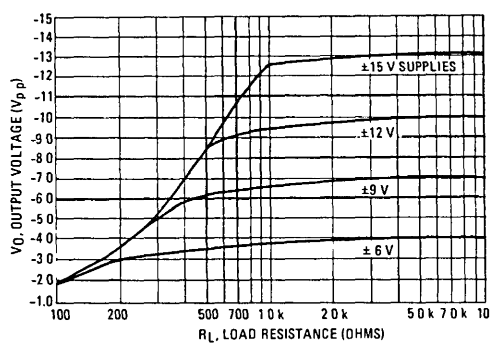


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

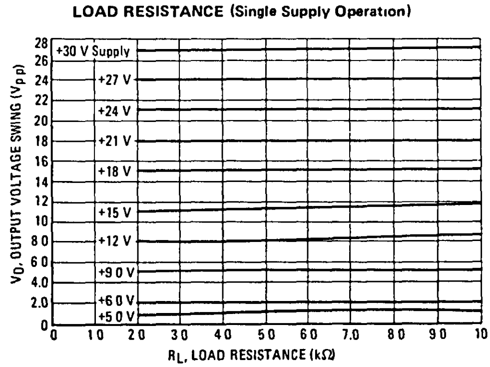


FIGURE 6 – BI-QUAD FILTER

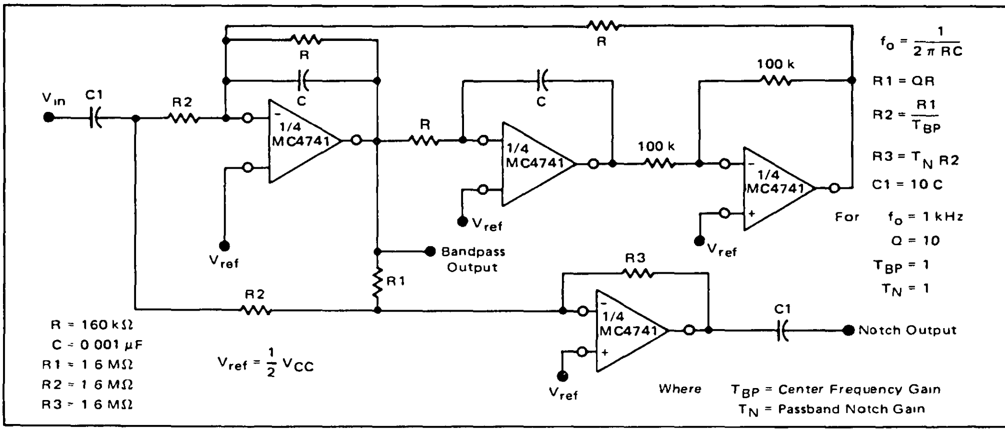


FIGURE 7 – NON-INVERTING PULSE RESPONSE

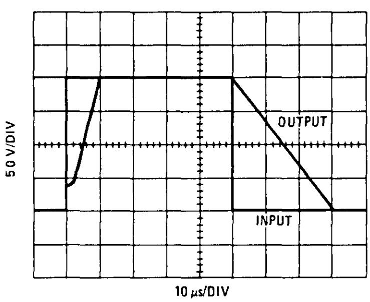


FIGURE 8 – OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

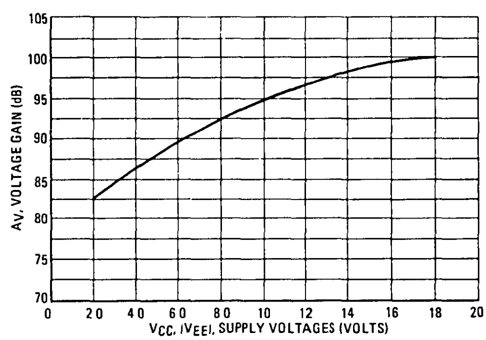


FIGURE 9 – TRANSIENT RESPONSE TEST CIRCUIT

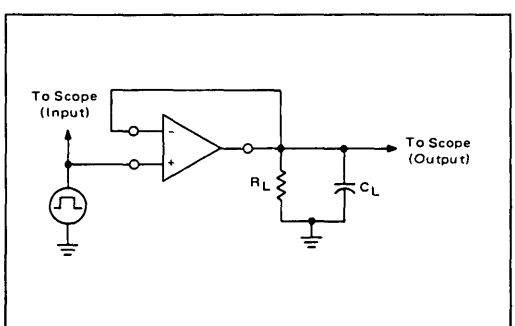


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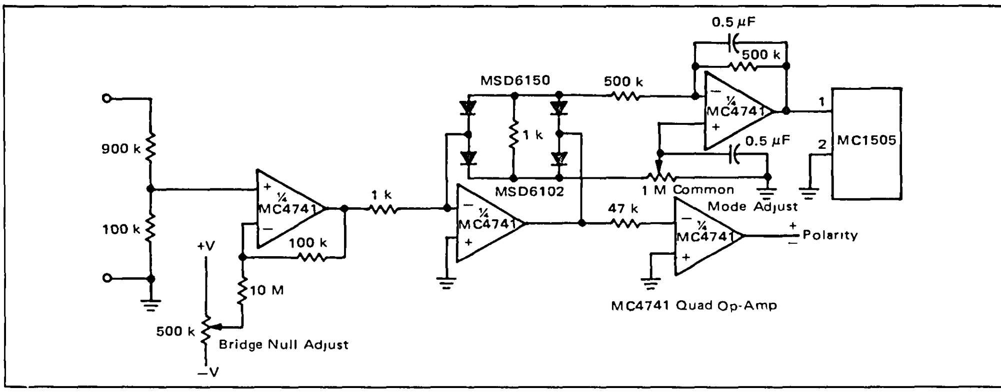
FIGURE 10 – ABSOLUTE VALUE DVM FRONT END



MC34001,MC35001
MC34002,MC35002
MC34004,MC35004

Advance Information

TRIMFET FAMILY OF JFET INPUT OPERATIONAL AMPLIFIERS

These low cost TRIMFET operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices with a laser trimmed input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. The laser trimming technology provides input offset voltage specification options which range from 2.0 to 10 millivolts maximum.

The Motorola TRIMFET family offers single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC35001/35002/35004 series are specified over the military operating temperature range of −55°C to +125°C and the MC34001/34002/34004 series are specified from 0°C to +70°C.

- Laser Trimmed Input Offset Voltage Options of 2.0, 5.0, and 10 mV Maximum
- Low Input Bias Current — 40 pA
- Low Input Offset Current — 10 pA
- Low Input Noise Voltage — 16 $nV/\sqrt{Hz}$
- Wide Gain Bandwidth — 4 MHz
- High Slew Rate — 13 V/μs
- Low Supply Current — 1.8 mA per Amplifier
- High Input Impedance — 10^{12} Ω
- High Common-Mode and Supply Voltage Rejection Ratios — 100 dB
- Industry Standard Pinouts

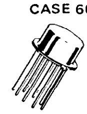
ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	MC34001AG,BG,G	0 to +70°C	Metal Can
	MC34001AP,BP,P	0 to +70°C	Plastic DIP
	MC34001AU,BU,U	0 to +70°C	Ceramic DIP
	MC35001AG,BG	−55 to +125°C	Metal Can
	MC35001AU,BU	−55 to +125°C	Ceramic Dip
Dual	MC34002AG,BG,G	0 to +70°C	Metal Can
	MC34002AP,BP,P	0 to +70°C	Plastic DIP
	MC34002AU,BU,U	0 to +70°C	Ceramic DIP
	MC35002AG,BG	−55 to +125°C	Metal Can
	MC35002AU,BU	−55 to +125°C	Ceramic DIP
Quad	MC34004AL,BL,L	0 to +70°C	Ceramic DIP
	MC34004AP,BP,P	0 to +70°C	Plastic DIP
	MC35004,AL,BL	−55 to +125°C	Ceramic DIP

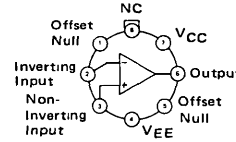
TRIMFET is a trademark of Motorola

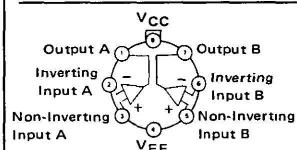
TRIMFET
FAMILY OF BIFET
OPERATIONAL AMPLIFIERS
LASER TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUITS

G SUFFIX
METAL PACKAGE
CASE 601

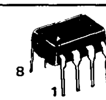


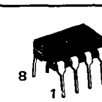
MC34001, MC35001
(Top View)





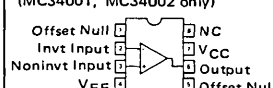
MC34002,
MC35002
(Top View)



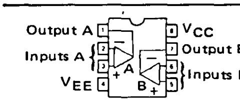


P SUFFIX
PLASTIC PACKAGE
CASE 626
(MC34001, MC34002 only)

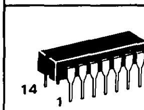
U SUFFIX
CERAMIC PACKAGE
CASE 693

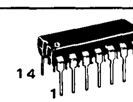


MC34001,
MC35001
(Top View)



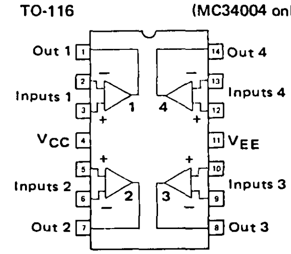
MC34002,
MC35002
(Top View)





L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC34004 only)



MC34004, MC35004 (Top View)

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MAXIMUM RATINGS

Rating	Symbol	MC35001 MC35002 MC35004	MC34001 MC34002 MC34004	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	V
Differential Input Voltage	V_{ID}	±40	±30	V
Input Voltage Range	V_{IDR}	±20	±16	V
Output Short-Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Operating Junction Temperature Metal and Ceramic Packages Plastic Packages	T_J	 150 —	 115 115	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 −65 to +150 —	 −65 to +150 −55 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC35001/35002/35004 Min	Typ	Max	MC34001/34002/34004 Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leqslant$ 10k)	V_{IO}							mV
MC3500XA, MC3400XA		—	1.0	2.0	—	1.0	2.0	
MC3500XB, MC3400XB		—	3.0	5.0	—	3.0	5.0	
MC3400X		—	—	—	—	5.0	10	
Average Temperature Coefficient of Input Offset Voltage $R_S \leqslant$ 10k, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0) (Note 2)	I_{IO}							pA
MC3500XA, MC3400XA		—	10	25	—	25	50	
MC3500XB, MC3400XB		—	10	50	—	25	100	
MC3400X		—	—	—	—	25	100	
Input Bias Current (V_{CM} = 0) (Note 2)	I_{IB}							pA
MC3500XA, MC3400XA		—	40	75	—	50	100	
MC3500XB, MC3400XB		—	40	100	—	50	200	
MC3400X		—	—	—	—	50	200	
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11	+15 −12	—	±11	+15 −12	—	V
Large Signal Voltage Gain (V_O = ±10V, R_L = 2.0 k)	A_{VOL}							V/mV
MC3500XA, MC3400XA		50	150	—	50	100	—	
MC3500XB, MC3400XB		50	150	—	50	100	—	
MC3400X		—	—	—	25	100	—	
Output Voltage Swing	V_O							V
($R_L \geqslant$ 10 k)		±12	±14	—	±12	±14	—	
($R_L \geqslant$ 2 k)		±10	±13	—	±10	±13	—	
Common Mode Rejection Ratio ($R_S \leqslant$ 10 k)	CMRR							dB
MC3500XA, MC3400XA		80	100	—	80	100	—	
MC3500XB, MC3400XB		80	100	—	80	100	—	
MC3400X		—	—	—	70	100	—	
Supply Voltage Rejection Ratio ($R_S \leqslant$ 10 k) (Note 3)	PSRR							dB
MC3500XA, MC3400XA		80	100	—	80	100	—	
MC3500XB, MC3400XB		80	100	—	80	100	—	
MC3400X		—	—	—	70	100	—	
Supply Current (Each Amplifier)	I_D							mA
MC3500XA, MC3400XA		—	1.8	2.5	—	1.8	2.5	
MC3500XB, MC3400XB		—	1.8	2.5	—	1.8	2.5	
MC3400X		—	—	—	—	1.8	2.7	
Slew Rate (A_V = 1)	SR	—	13	—	—	13	—	V/µs
Gain-Bandwidth Product	BWp	—	4.0	—	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100Ω, f = 1000 Hz)	e_n	—	16	—	—	16	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 1])

Characteristic	Symbol	MC35001/35002/35004 Min	Typ	Max	MC34001/34002/34004 Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leqslant$ 10 k)	V_{IO}							mV
MC3500XA, MC3400XA		–	3.0	4.0	–	3.0	4.0	
MC3500XB, MC3400XB		–	4.0	7.0	–	4.0	7.0	
MC3400X		–	–	–	–	8.0	13	
Input Offset Current (V_{CM} = 0) (Note 2)	I_{IO}							nA
MC3500XA, MC3400XA		–	–	20	–	–	2.0	
MC3500XB, MC3400XB		–	–	40	–	–	4.0	
MC3400X		–	–	–	–	–	4.0	
Input Bias Current (V_{CM} = 0) (Note 2)	I_{IB}							nA
MC3500XA, MC3400XA		–	–	50	–	–	4.0	
MC3500XB, MC3500XB		–	–	50	–	–	8.0	
MC3400X		–	–	–	–	–	8.0	
Common Mode Input Voltage Range	V_{ICR}	±11	+15 -12	–	±11	+15 -12	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}							V/mV
MC3500XA, MC3400XA		25	–	–	25	–	–	
MC3500XB, MC3400XB		25	–	–	25	–	–	
MC3400X		–	–	–	15	–	–	
Output Voltage Swing	V_O							V
($R_L \geqslant$ 10 k)		±12	±14	–	±12	±14	–	
($R_L \geqslant$ 2 k)		±10	±13	–	±10	±13	–	
Common Mode Rejection Ratio ($R_S \leqslant$ 10 k)	CMRR							dB
MC3500XA, MC3400XA		80	100	–	80	100	–	
MC3500XB, MC3400XB		80	100	–	80	100	–	
MC3400X		–	–	–	70	100	–	
Supply Voltage Rejection Ratio ($R_S \leqslant$ 10 k) (Note 3)	PSRR							dB
MC3500XA, MC3400XA		80	100	–	80	100	–	
MC3500XB, MC3400XB		80	100	–	80	100	–	
MC3400X		–	–	–	70	100	–	
Supply Current (Each Amplifier)	I_D							mA
MC3500XA, MC3400XA		–	2.0	2.8	–	2.0	2.8	
MC3500XB, MC3400XB		–	2.0	2.8	–	2.0	2.8	
MC3400X		–	–	–	–	2.0	3.0	

NOTES

(1) T_{low} = −55°C for MC35001A/35001B
MC35002A/35002B
MC35004A/35004B
= 0°C for MC34001/34001A/34001B
MC34002/34002A/34002B
MC34004/34004A/34004B
T_{high} = +125°C for MC35001A/35001B
MC35002A/35002B
MC35004A/35004B
= +70°C for MC34001/34001A/34001B
MC34002/34002A/34002B
MC34004/34004A/34004B

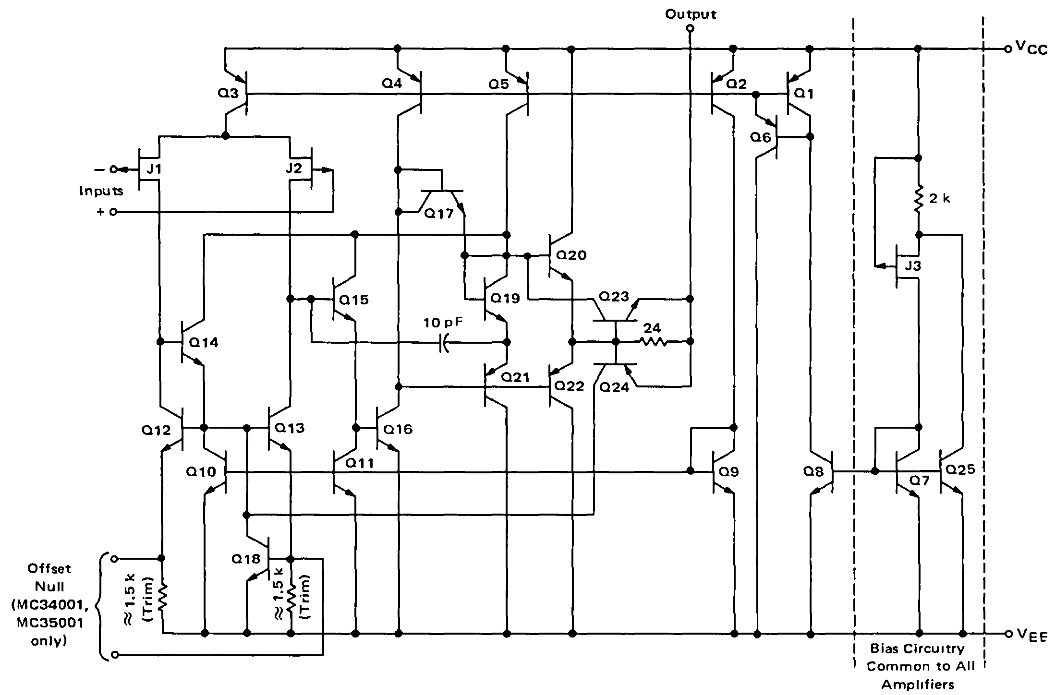
(2) The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

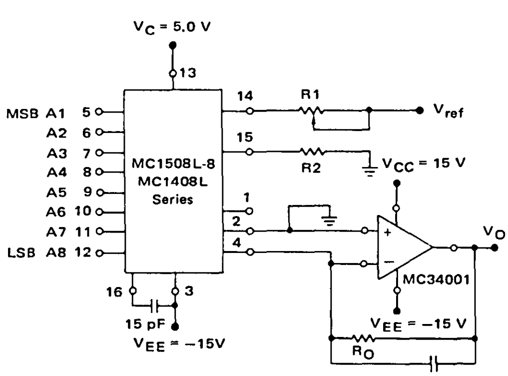
(4) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

3

REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)



TYPICAL APPLICATION: OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time all bits are switched

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0$ Vdc
$R1 = R2 \approx 1.0\ k\Omega$
$R_O = 5.0\ k\Omega$

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

MC34022
MC35022

Advance Information

TRIMFET PRECISION DUAL JFET INPUT OPERATIONAL AMPLIFIERS

The MC34022/35022 series of TRIMFET dual operational amplifiers combine two state-of-the-art linear technologies on a single monolithic chip to provide precision input characteristics at a low cost. These internally compensated operational amplifiers have well matched high voltage JFET input devices with laser trimmed input offset voltages. BIFET technology provides a wide bandwidth and a fast slew rate while maintaining low input bias currents, input offset currents, and supply currents. Laser trimming technology provides input offset voltage specification options which range from 0.5 to 2.0 millivolts maximum with a typical temperature coefficient of 5.0 μV/^{o}C.

These Motorola TRIMFET dual operational amplifiers are pin-compatible with the industry standard MC1458/1558 bipolar devices. The MC35022A/35022B series are specified over the military operating temperature range of −55°C to +125°C, and the MC34022/34022A/34022B series are specified from 0°C to +70°C.

- Laser Trimmed Input Offset Voltage Options of 0.5, 1.0, and 2.0 mV Maximum
- Temperature Coefficient of Input Offset Voltage — 5.0 μV/^{o}C
- Low Input Bias Current — 30 pA
- Low Input Offset Current — 10 pA
- Low Input Noise Voltage — 16 nV/$\sqrt{Hz}$
- Wide Gain Bandwidth — 4 MHz
- High Slew Rate — 13 V/μs
- Low Supply Current — 1 8 mA per Amplifier
- High Input Impedance — 10^{12} Ω
- High Common-Mode and Supply Voltage Rejection Ratios — 100 dB
- Industry Standard Pinouts

APPLICATIONS

The MC34022/35022 series of TRIMFET dual operational amplifiers is suggested for all general-purpose BIFET amplifier requirements where precision input characteristics are needed in addition to the features normally furnished by other BIFET amplifiers.

- Fast D/A and A/D Converters
- Sample and Hold Circuits
- Precision High-Speed Integrators
- High Impedance Buffers
- Wideband, High Slew, Low Current Amplifiers

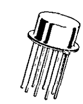
This is advance information and specifications are subject to change without notice.

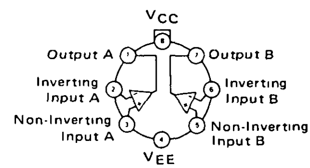
TRIMFET
PRECISION
DUAL BIFET
OPERATIONAL AMPLIFIERS

LASER TRIMMED
SILICON MONOLITHIC
INTEGRATED CIRCUIT

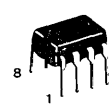
3

G SUFFIX
METAL PACKAGE
CASE 601



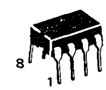


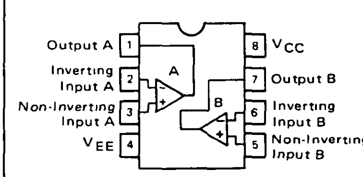
(Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 626
(MC34022 only)

U SUFFIX
CERAMIC PACKAGE
CASE 693





(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34022AG, BG, G	0 to +70°C	Metal Can
MC34022AP, BP, P	0 to +70°C	Plastic DIP
MC34022AU, BU, U	0 to +70°C	Ceramic DIP
MC35022AG, BG	-55 to +125°C	Metal Can
MC35022AU, BU	-55 to +125°C	Ceramic DIP

3

MAXIMUM RATINGS

Rating	Symbol	MC35022	MC34022	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	V
Differential Input Voltage	V_{ID}	±40	±16	V
Input Voltage Range	V_{IDR}	±20	+16	V
Output Short-Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Operating Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 150 —	 115 115	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 −65 to +150 —	 −65 to +150 −55 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted).

Characteristic	Symbol	MC35022 Min	MC35022 Typ	MC35022 Max	MC34022 Min	MC34022 Typ	MC34022 Max	Unit
Input Offset Voltage ($R_S \leqslant$ 10 k)	V_{IO}							mV
MC35022A, MC34022A		—	0.3	0.5	—	0.3	0.5	
MC35022B, MC34022B		—	0.5	1.0	—	0.5	1.0	
MC34022		—	—	—	—	1.0	2.0	
Average Temperature Coefficient of Input Offset Voltage $R_S \leqslant$ 10 k, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{IO}/\Delta T$	—	5.0	—	—	5.0	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 2)	I_{IO}							pA
MC35022A, MC34022A		—	10	25	—	15	30	
MC35022B, MC34022B		—	10	50	—	15	70	
MC34022		—	—	—	—	15	70	
Input Bias Current (V_{CM} = 0) (Note 2)	I_{IB}							pA
MC35022A, MC34022A		—	30	60	—	40	75	
MC35022B, MC34022B		—	30	75	—	40	150	
MC34022		—	—	—	—	40	150	
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11	+15 −12	—	±11	+15 −12	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}							V/mV
MC35022A, MC34022A		50	150	—	50	100	—	
MC35022B, MC34022B		50	150	—	50	100	—	
MC34022		—	—	—	25	100	—	
Output Voltage Swing	V_O							V
($R_L \geqslant$ 10 k)		±12	±14	—	±12	±14	—	
($R_L \geqslant$ 2 k)		±10	±13	—	±10	±13	—	
Common Mode Rejection Ratio ($R_S \leqslant$ 10 k)	CMRR							dB
MC35022A, MC34022A		80	100	—	80	100	—	
MC35022B, MC34022B		80	100	—	80	100	—	
MC34022		—	—	—	70	100	—	
Supply Voltage Rejection Ratio ($R_S \leqslant$ 10 k) (Note 3)	PSRR							dB
MC35022A, MC34022A		80	100	—	80	100	—	
MC35022B, MC34022B		80	100	—	80	100	—	
MC34022		—	—	—	70	100	—	
Supply Current (Each Amplifier)	I_D							mA
MC35022A, MC34022A		—	1.8	2.5	—	1.8	2.5	
MC35022B, MC34022B		—	1.8	2.5	—	1.8	2.5	
MC34022		—	—	—	—	1.8	2.7	
Slew Rate (A_V = 1)	SR	—	13	—	—	13	—	V/μs
Gain-Bandwidth Product	BWp	—	4.0	—	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	—	16	—	—	16	—	nV/√Hz
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	—	0.01	—	pA/√Hz

See notes on following page.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15V, V_{EE} = -15 V, T_A = T_{low} to T_{high} [Note 1])

Characteristic	Symbol	MC35022 Min	MC35022 Typ	MC35022 Max	MC34022 Min	MC34022 Typ	MC34022 Max	Unit
Input Offset Voltage ($R_S \leq$ 10 k)	V_{IO}							mV
MC35022A, MC34022A		–	0.7	1.5	–	0.7	1.5	
MC35022B, MC34022B		–	1.0	2.0	–	1.0	2.0	
MC34022		–	–	–	–	2.0	3.0	
Input Offset Current (V_{CM} = 0) (Note 2)	I_{IO}							
MC35022A, MC34022A		–	–	20	–	–	2.0	nA
MC35022B, MC34022B		–	–	40	–	–	4.0	
MC34022		–	–	–	–	–	4.0	
Input Bias Current (V_{CM} = 0) (Note 2)	I_{IB}							nA
MC35022A, MC34022A		–	–	50	–	–	4.0	
MC35022B, MC34022B		–	–	50	–	–	8.0	
MC34022		–	–	–	–	–	8.0	
Common Mode Input Voltage Range	V_{ICR}	±11	+15 −12	–	±11	+15 −12	–	V
Large Signal Voltage Gain (V_O = ± 10 V, R_L = 2 0 k)	A_{VOL}							V/mV
MC35022A, MC34022A		25	–	–	25	–	–	
MC35022B, MC34022B		25	–	–	25	–	–	
MC34022		–	–	–	15	–	–	
Output Voltage Swing	V_O							V
($R_L \geq$ 10 k)		±12	±14	–	±12	±14	–	
($R_L \geq$ 2 k)		±10	±13	–	±10	±13	–	
Common Mode Rejection Ratio ($R_S \leq$ 10 k)	CMRR							dB
MC35022A, MC34022A		80	100	–	80	100	–	
MC35022B, MC34022B		80	100	–	80	100	–	
MC34022		–	–	–	70	100	–	
Supply Voltage Rejection Ratio ($R_S \leq$ 10 k) (Note 3)	PSRR							dB
MC35022A, MC34022A		80	100	–	80	100	–	
MC35022B, MC34022B		80	100	–	80	100	–	
MC34022		–	–	–	70	100	–	
Supply Current (Each Amplifier)	I_D							mA
MC35022A, MC34022A		–	2 0	2.8	–	2 0	2 8	
MC35022B, MC34022B		–	2.0	2.8	–	2 0	2.8	
MC34022		–	–	–	–	2.0	3.0	

3

NOTES

(1) T_{low} = -55°C for MC35022A/35022B

= 0°C for MC34022/34022A/34022B

T_{high} = +125°C for MC35022A/35022B

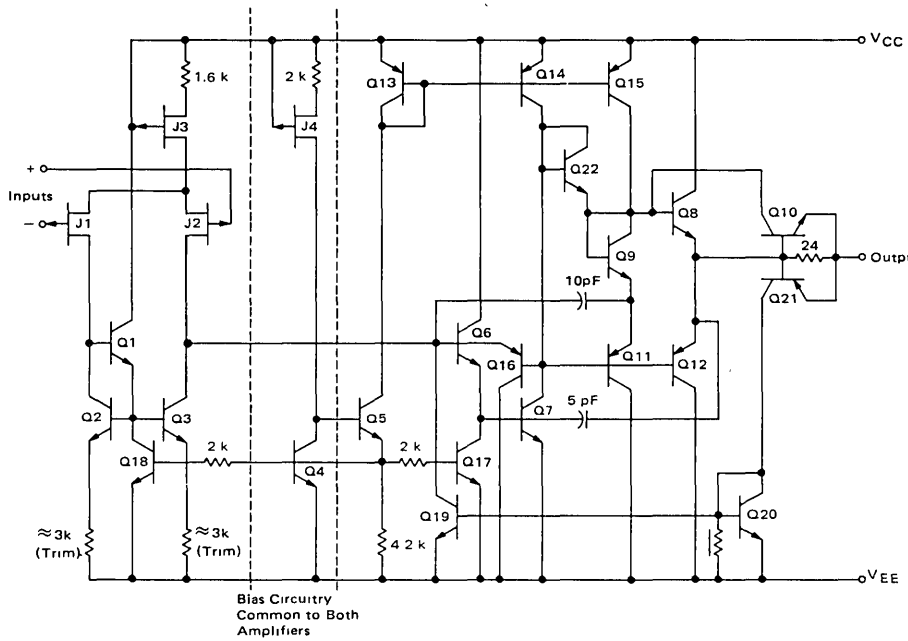
= +70°C for MC34022/34022A/34022B

(2) The input bias currents approximately double for every 10°C rise in junction temperature, T_J Due to limited test time, the input bias currents are correlated to junction temperature Use of a heat sink is recommended if input bias current is to be kept to a minimum

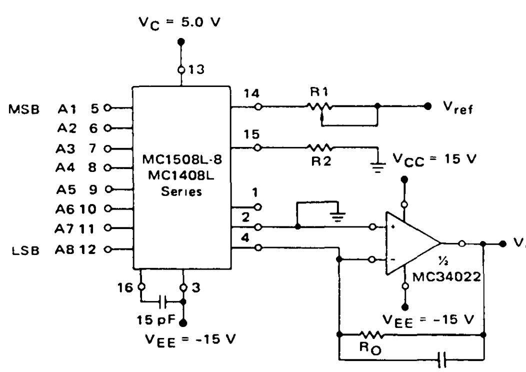
(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

(4) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

REPRESENTATIVE CIRCUIT SCHEMATIC
(One-Half of Circuit Shown)



TYPICAL APPLICATION: OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Setting time to within 1/2 LSB (± 19.5mV) is approximately 4.0 μs from the time that all bits are switched.

* The value of C may be selected to minimize overshoot and ringing ($C \approx 68$ pF).

Theoretical V_O

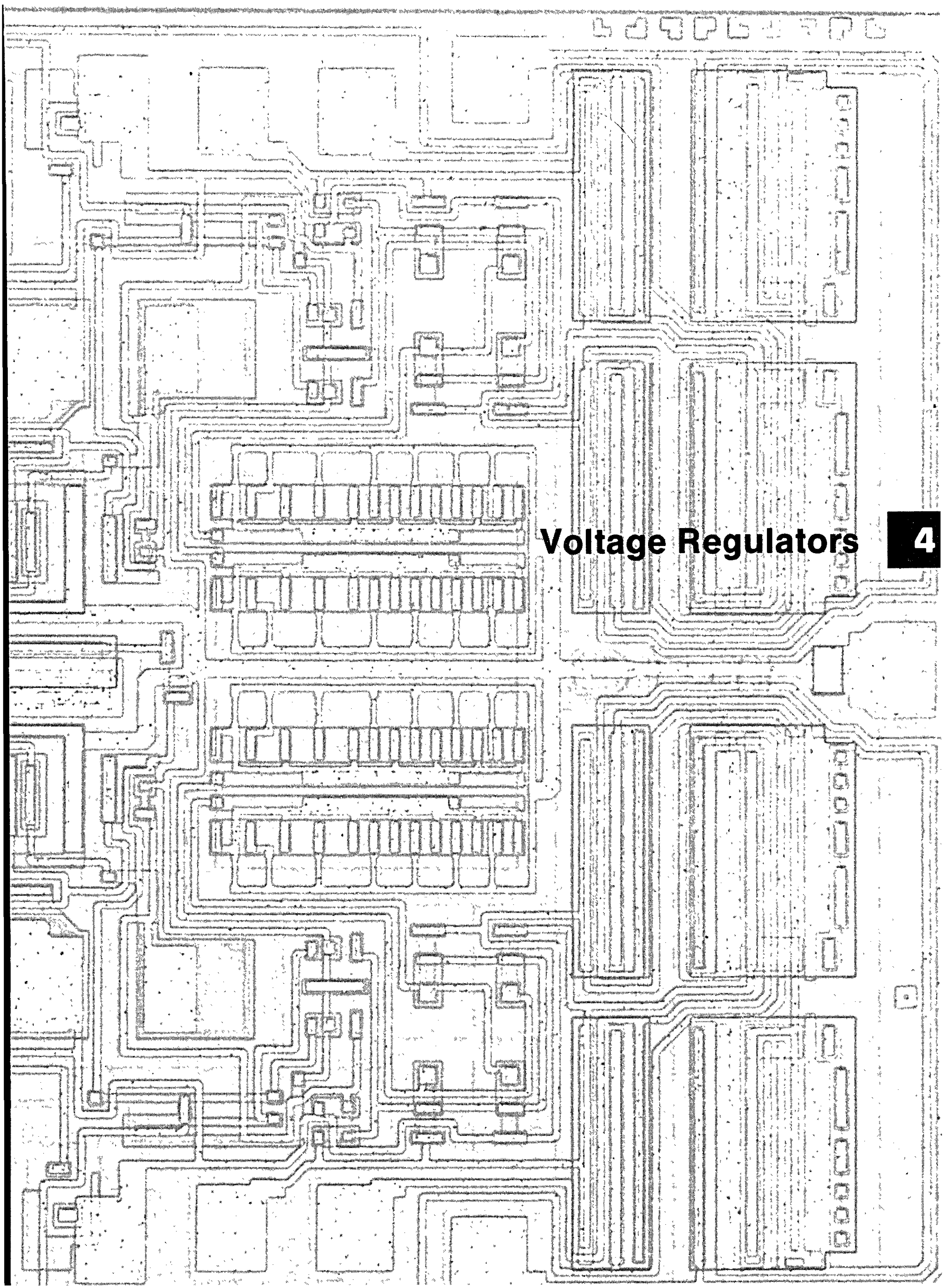
$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0$ Vdc
$R1 = R2 \cong 1.0\ k\Omega$
$R_O = 5.0\ k\Omega$

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$



Voltage Regulators

4

VOLTAGE REGULATORS

*-55 to 150°C

4

VOLTAGE REGULATORS

Fixed Output Voltage Regulators

- Low-cost monolithic circuits for positive and/or negative regulation at currents from 100 mA to 1.5A
- Ideal for on-card regulation of subsystems
- Internal current limiting thermal shutdown and safe-area compensation

FIXED-VOLTAGE, 3-TERMINAL REGULATORS FOR POSITIVE OR NEGATIVE POLARITY POWER SUPPLIES.

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Type Positive Output	Device Type Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case
2	±0 1	1500	–	MC7902C	5.5/35	40	120	1.0	1, 221A
3	±0 15	100	–	MC79L03AC	4.7/30	60	72	–	29, 79
	±0 3			MC79L03C		80			
5	±0 5	100	MC78L05C	MC79L05C	6.7/30	200	60	–	29, 79
	±0 25		MC78L05AC	MC79L05AC		150			
·		500	MC78M05C	–	7/35	100	100	1 0	79, 221A
	±0.4	1500	LM109	–				1.1	1, 79
			LM209	–					
	±0.25		LM309	–		50		1.0	
	±0 35		**MC7805*	–	8 0/35			0 6	1
	±0 25		MC7805C	MC7905C	7/35	100		1 0	1, 221A
	±0 2		**MC7805A*	–	7.5/35	10	50	0 6	1
			**MC7805AC	–			ı00		1, 221A
	±0 25		**LM140-5*	–	7/35	50	50		1
			**LM340-5	–					
5 2	±0 26	1500	–	MC7905 2C	7.2/35	105	105	1 0	1, 221A
6	±0 3	500	MC78M06C	–	8/35	100	120	1 0	79, 221A
	±0 35	1500	**MC7806*	–	9/35	60	100	0 7	1
	±0 3		MC7806C	MC7906C	8/35	120	120		1, 221A
	±0 24		**MC7806A*	–	8 6/35	11	50		1
			**MC7806AC	–			100		1, 221A
	±0 3		**LM140-6*	–	8/35	60	60		1
			**LM340 6	–					
8	±0 8	100	MC78L08C	–	9 7/30	200	80	–	29, 79
			MC78L08AC	–		175			
	±0 4	500	MC78M08C	–	10/35	100	160	1 0	79, 221A
		1500	**MC7808*	–	11 5/35	80	100		1
			MC7808C	MC7908C	10/35	160	160		1, 221A
	±0 3		**MC7808A*	–	10 6/35	13	50		1
			**MC7808AC	–			100		1, 221A
	±0 4		**LM140-8*	–	10 5/35	80	80		1
			**LM340-8	–					
12	±1 2	100	MC78L12C	MC79L12C	13.7/35	250	100	–	29, 79
	±0 6		MC78L12AC	MC79L12AC					
		500	MC78M12C	–	14/35	100	240	1 0	79, 221A
		1500	**MC7812*	–	15 5/35	120	120	1 5	1
			MC7812C	MC7912C	14 5/35	240	240		1, 221A
	±0 5		**MC7812A*	–	14 8/35	18	50		1
			**MC7812AC	–			100		1, 221A
	±0 6		**LM140-12*	–	14.5/35	120	120	1 5	1
			**LM340-12	–					

**1979 New Product Introductions
*T_J = -55 to +150°C
†Output Voltage Tolerance for Worst Case

(continued)

Fixed Output Voltage Regulators (continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Type Positive Output	Device Type Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case
15	±1.5	100	MC78L15C	MC79L15C	16.7/35	300	150	–	29, 79
	±0.75		MC78L15AC	MC79L15A					
		500	MC78M15C	–	17/35	100	300	1.0	79, 221A
		1500	**MC7815*	–	18.5/35	150	150	1.8	1
			MC7815C	MC7915C	17.5/35	300	300		1, 221A
	±0.6		**MC7815A*	–	17.9/35	22	50		1
			**MC7815AC	–			100		1, 221A
	±0 75		**LM140-15*	–	17.5/35	150	150		1
			**LM340-15	–					
18	±1 8	100	MC78L18C	MC79L18C	19.7/35	325	170	–	29, 79
	±0.9		MC78L18AC	MC79L18AC					
		500	MC78M18C	–	20/35	100	360	1.0	79, 221A
		1500	**MC7818*	–	22/35	180	180	2.3	1
			MC7818C	MC7918C	21/35	360	360		1, 221A
	±0.7		**MC7818A*	–		31	50		1
			**MC7818AC	–			100		1, 221A
	±0.9		**LM140-18*	–		180	180		1
			**LM340-18	–					
20	±1.0	500	MC78M20C	–	22/40	10	400	1 1	79, 221A
24	±2 4	100	MC78L24C	MC79L24C	25.7/40	350	200	–	29, 79
	±1.2		MC78L24AC	MC79L24AC		300			
		500	MC78M24C	–	26/40	100	480	1.2	79, 221A
		1500	**MC7824*	–	28/40	240	240	3 0	1
			MC7824C	MC7924C	27/40	480	480		1, 221A
	±1.0		**MC7824A*	–	27.3/40	36	50		1
			**MC7824AC	–	27/40		100		1, 221A
	±1 2		**LM140 24*	–		240	240		1
			**LM340-24	–					

**1979 New Product Introductions
*T_J = -55 to +150°C
†Output Voltage Tolerance for Worst Case

Variable Output Voltage Regulators

POSITIVE OUTPUT REGULATORS

I_O mA Max	Device Type	SUFFIX	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	$V_{in} - V_{out}$ Differential Volts Min	P_D Watts Max T_C = 25°C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Typ Line	Regulation Load	TC V_{out} Typ %/°C	T_J = °C Max	Case
20	LM305	H	4 5	40	8 5	50	3.0	0 4	1.3	0 06	0 1	0 007	85	601
	LM205							0.68	1.6				100	
	LM105			30					2.7				150	
100	**LM317L	H,Z	1.2	37	5.0	40	3 0	Internally Limited		0 04	0 5	0 006	125	29,79
	**LM217L									0 02	0 3	0 004	150	
	**LM117L*											0 003		
150	MC1723	CP	2.0	37	9 5	40	3 0	0 65	–	0 1	0 3	0 003	150	646
		CG						0 8	2.1	0 1		0 003		603C
		G								0 2		0 002		
		CL						1 0	–	0 1		0.003	175	632
		L							–	0 2		0.002		
250	MC1469	G	2.5	32	9	35	3 0	0 68	1.8	0 03	0 13	0.002	150	603
	MC1569			37	8 5	40	2 7			0 015				
600	MC1469	R	2 5	32	9.0	35	3 0	3.0	14.0	0 03	0.05	0.002	150	614
	MC1569			37	8 5	40	2.7			0 015				
1500	LM317	T	1.2	37	5 0	40	3 0	Internally Limited		0 07	1 5	0.006	125	221A
	LM317	H, K												79, 1
	LM217											0.004		
	LM117*									0.05	1.0	0 003	150	

*T_J = -55 to +150°C
**1979 New Product Introductions

Variable Output Voltage Regulators (continued)

NEGATIVE OUTPUT REGULATORS

I_O mA Max	Device Type	SUFFIX	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	$V_{in} - V_{out}$ Differential Volts Min	P_D Watts Max T_C = 25°C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Typ Line	Regulation % V_{out} @ T_A = 25°C Typ Load	TC V_{out} Typ %/°C	T_J = °C Max	Case
20	LM304	H	0 035	30	8 0	40	2.0	0 4	1 3	0 1	0 05	0.007	80	603
	LM204		0 015	40		50		0 68	1 6				100	
	LM104								2.7				150	
250	MC1463	G	3 8	32	9 0	35	3 0 ·	0 68	1 8	0 03	0 05	0 002	150	603
	MC1563		3 6	33	8.5	40	2 7			0 015	0 13			
600	MC1463	R	3 8	34	9 0	35	3 0	2 4	9 0	0 03	0 05	0 002	175	614
	MC1563		3 6	37	8 5	40	2.7			0 015				

Switching Regulators

Used as the control circuit in PWM, push-pull, bridge and series type switchmode supplies. The devices include the reference, oscillator, pulse-width modulator, phase splitter and output sections. Frequency and duty cycle are independently adjustable.

I_O ±mA Max	V_{CC} Volts Min	V_{CC} Volts Max	f_o kHz Min	f_o kHz Max	Device Number	Suffix	T_A °C	Case
40	10	30	2.0	100	MC3420	P	0 to +70	648
						L		620
					MC3520	L	-55 to +125	620

Special Regulators

FLOATING VOLTAGE AND CURRENT REGULATORS

Designed for laboratory type power supplies. Voltage is limited only by the breakdown voltage of associated, external, series-pass transistors.

V_{out} Volts Min	V_{out} Volts Max	I_O mA Max	Device Type	SUFFIX	V_{aux} Volts Min	V_{aux} Volts Max	P_D Watts Max	$\Delta V_{ref}/V_{ref}$ % Line	$\Delta V_{ref}/V_{ref}$ % Load	$\Delta I_L/I_L$ % Max	TC V_{out} %/°C Typ	Case
0	*	*	MC1466	L	21	30	0.75	0 015	0 015	0 2	0 01	632
			MC1566	L	20	35		0 004	0 004	0 1	0 006	

*Dependent on characteristics of external series-pass elements.

DUAL ±15 V TRACKING REGULATORS.

Internally, the device is set for ±15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.

V_{out} Volts Min	V_{out} Volts Max	I_O mA Max	V_{in} Volts Min	V_{in} Volts Max	Device Type	SUFFIX	P_D Watts Max	Reg_{line} mV	Reg_{load} mV	TC %/°C (T_{low} to T_{high}) Typ	T_A °C	Case
14.8	15.2	±100	17	30	MC1468	G	0.8	10	10	3 0	0 to +75	603C
						L	1 0					632
						R	2 4					614
					MC1568	G	0 8				-55 to +125	603C
						L	1.0					632
						R	2 4					614

4

Special Regulators (continued)

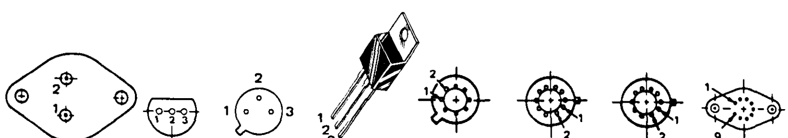
LOW TEMPERATURE DRIFT, LOW VOLTAGE REFERENCE

V_{out} Volts Typ	I_O mA Max	$\Delta V_{out}/\Delta T$ ppm/°C Max	Device Type	Suffix	Reg_{line} mV Max	Reg_{load} mV Max	T_A °C	Case
2.5 ± 25 mV	10	40	MC1403	U	3/4.5 (Note 1)	10 (Note 3)	0 to +70	693
		25	MC1403A					
		55	MC1503				-55 to +125	
		25	MC1503A					
5.0 ± 50 mV		40	MC1404U5		6.0 (Note 2)		0 to +70	
		25	MC1404AU5					
		55	MC1504U5				-55 to +125	
		25	MC1504AU5					
6.25 ± 60 mV		40	MC1404U6				0 to +70	
		25	MC1404AU6					
		55	MC1504U6				-55 to +125	
		25	MC1504AU6					
10 ± 100 mV		40	MC1404U10				0 to +70	
		25	MC1404AU10					
		55	MC1504U10				-55 to +125	
		25	MC1504AU10					

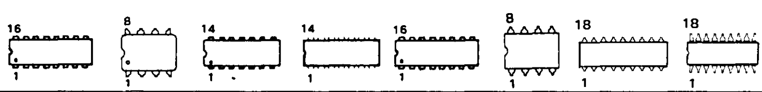
Notes 1. $4.5 \leq V_I \leq 15$ V/15 V $\leq V_I \leq 40$ V
2. $V_{in} = V_{out} + 2.5$ V to 40 V
3. 0 mA $< I_O <$ 10 mA

4

Package Styles



CASE	1 (TO-3)	29 (TO-92)	79 (TO-39)	221A (TO-220)	601	603 (TO-5 Type)	603C	614 (TO-66)
MATERIAL	Metal	Plastic	Metal	Plastic	Metal	Metal	Metal	Metal
SUFFIX	SK, K, KC	P, Z	G, H	T	G, H	G, H	G	R



CASE	620	626	632 (TO-116)	646	648	693	701	726
MATERIAL	Ceramic	Plastic	Ceramic	Plastic	Plastic	Ceramic	Ceramic	Plastic
SUFFIX	J, L	P or P1	L	P or P2	N, P	U	J	N

LM104
LM204
LM304

MONOLITHIC NEGATIVE VOLTAGE REGULATOR

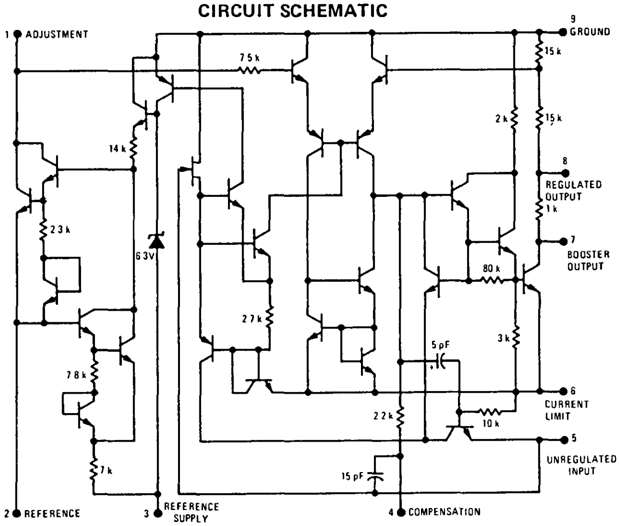
The LM104H, LM204H, and LM304H are precision negative voltage regulators which can be programmed by a single external resistor to supply an output voltage from 40 volts down to zero volts.

- Regulation No Load to Full Load – 1.0 mV
- Line Regulation – 0.01%/V
- Ripple Rejection – 0.2 mV/V
- Temperature Stability Over Temperature Range – 0.3%

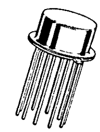
NEGATIVE VOLTAGE REGULATOR

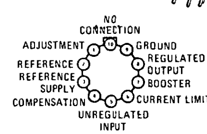
MONOLITHIC SILICON INTEGRATED CIRCUIT

CIRCUIT SCHEMATIC



H SUFFIX
METAL PACKAGE
CASE 603
(TO-100)
$R_{\theta JA}$ = 160°C/W





(TOP VIEW)

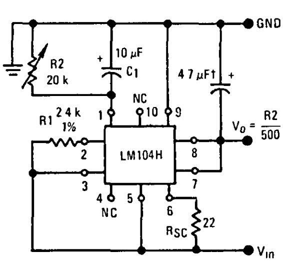
Pin 5 Electrically Connected to Case Through Substrate

ORDERING INFORMATION

Device	Temperature Range	Package
LM104H	-55°C to +125°C	Metal Can
LM204H	-25°C to +85°C	Metal Can
LM304H	0°C to +70°C	Metal Can

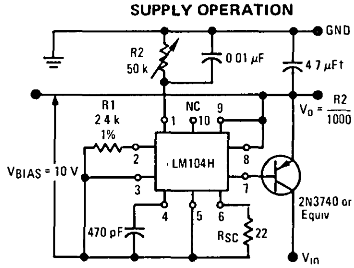
TYPICAL APPLICATIONS

FIGURE 1 – BASIC REGULATOR CIRCUIT



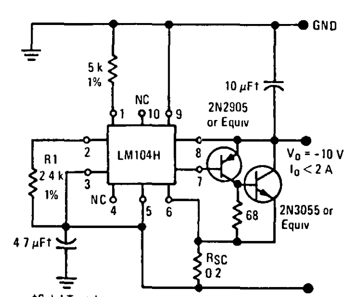
†Solid Tantalum
Trim R1 for exact scale factor

FIGURE 2 – SEPARATE BIAS SUPPLY OPERATION



†Solid Tantalum

FIGURE 3 – HIGH CURRENT REGULATOR



†Solid Tantalum

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	LM104	LM204	LM304	Unit
Input Voltage	V_{in}	50	50	40	Vdc
Input-Output Voltage Differential	$V_{in}-V_o$	50	50	40	Vdc
Power Dissipation (See Note 1)	P_D	680	680	680	mW
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C
Lead Temperature (soldering, t = 10 s)	T_S	300	300	300	°C

4

ELECTRICAL CHARACTERISTICS (See Note 2)

Characteristic	Symbol	LM104 LM204			LM304			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	-8.0	–	-50	-8.0	–	-40	Volts
Output Voltage Range	V_o	-0.015	–	-40	-0.035	–	-30	Volts
Output-Input Voltage Differential	$\|V_{in}-V_o\|$							Volts
I_o = 20 mA		2.0	–	50	2.0	–	40	
I_o = 5.0 mA		0.5	–	50	0.5	–	40	
Load Regulation $0 \leq I_o \leq 20$ mA, R_{SC} = 15Ω	Reg_{load}	–	1.0	5.0	–	1.0	5.0	mV
Line Regulation $V_o \leq -5.0$ V, ΔV_{in} = 0.1 V	Reg_{in}	–	0.056	0.1	–	0.056	0.1	%
Ripple Rejection (See Figure 1) (C_1 = 10 μF, f = 120 Hz)	Rej_R							mV/V
$V_{in} < -15$ V		–	0.2	0.5	–	0.2	0.5	
$-7.0\text{ V} \geq V_{in} \geq -15$ V		–	0.5	1.0	–	0.5	1.0	
Output Voltage Scale Factor R_1 = 2.4 kΩ (See Figures 1,2 and 3)	SF	1.8	2.0	2.2	1.8	2.0	2.2	V/kΩ
Temperature Stability	TCV_o $\Delta V_o/\Delta T$							%
$V_o \leq -1.0$ V		–	0.3	1.0	–	–	–	
$V_o \leq -1.0$ V, $0°C \leq T_A \leq +70°C$		–	–	–	–	0.3	1.0	
Output Noise Voltage (See Figure 1) (10 Hz ≤ f ≤ 10 kHz)	V_n							
$V_o \leq -5.0$ V, C_1 = 0		–	0.007	–	–	0.007	–	%
C_1 = 10 μF		–	15	–	–	15	–	μV
Standby Current Drain (I_L = 5.0 mA)	I_B							mA
V_o = 0		–	1.7	2.5	–	1.7	2.5	
V_o = -40 V		–	3.6	5.0	–	–	–	
V_o = -30 V		–	–	–	–	3.6	5.0	
Long Term Stability $V_o \leq -1.0$ V	S	–	0.1	1.0	–	0.1	1.0	%

Note 1:

The maximum junction temperature of the LM104 is +150°C, for the LM204 – +100°C, and for the LM304 – +85°C For operating at elevated temperatures, the package must be derated based on a thermal resistance of 150°C/W – junction to ambient, or 45°C/W – junction to case.

Note 2:

These specifications apply for junction temperatures of –55°C to +150°C for the LM104; –25°C to +100°C for the LM204, and 0 to +85°C for the LM304. The specifications also apply for input and output voltages within the indicated ranges (unless otherwise specified). Load and line regulation specifications given are for constant junction temperature. Temperature drift effects must be taken into account separately when the device is operating under conditions of high power dissipation.

LM105
LM205
LM305

MONOLITHIC POSITIVE VOLTAGE REGULATOR

The LM105H, LM205H, and LM305H are precision voltage regulators which can be programmed by a single external resistor to supply an output voltage from 4.5 volts to 40 volts.

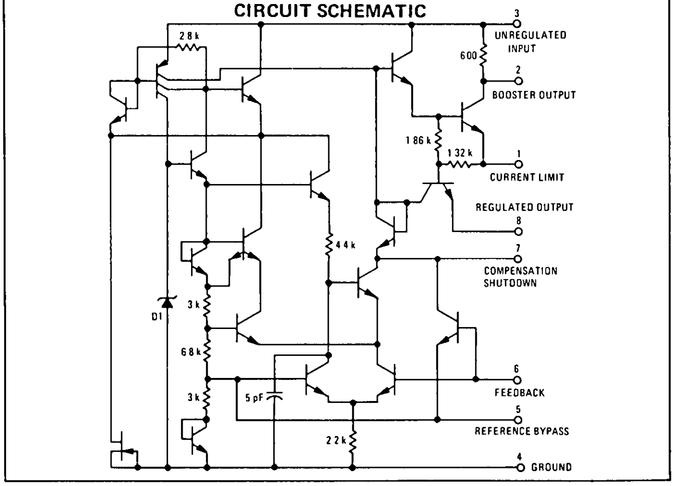
- Output Currents in Excess of 10 A Possible by Addition of External Transistors
- Load Regulation Better than 0.1%, Full Load with Current Limiting
- DC Line Regulation, 0.03%/V
- Ripple Rejection, 0.01%/V

POSITIVE VOLTAGE REGULATOR

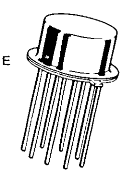
SILICON MONOLITHIC

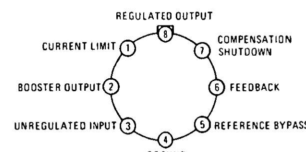
INTEGRATED CIRCUIT

CIRCUIT SCHEMATIC



H SUFFIX
METAL PACKAGE
CASE 601





Note: Pin 4 connected to case
(TOP VIEW)

ORDERING INFORMATION

Device	Temperature Range	Package
LM105H	-55°C to +125°C	Metal Can
LM205H	-25°C to +85°C	Metal Can
LM305H	0°C to +70°C	Metal Can

TYPICAL APPLICATIONS

FIGURE 1 – BASIC REGULATOR CIRCUIT

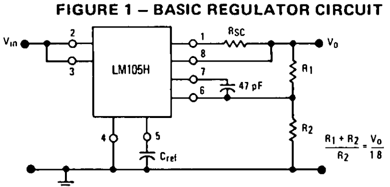


FIGURE 2 – 10 A REGULATOR with FOLDBACK CURRENT LIMITING

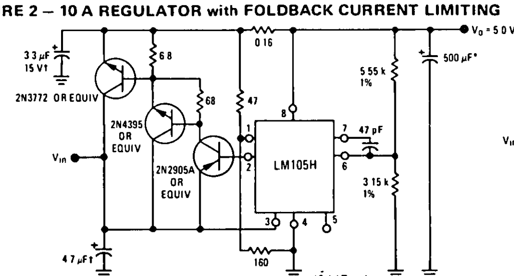
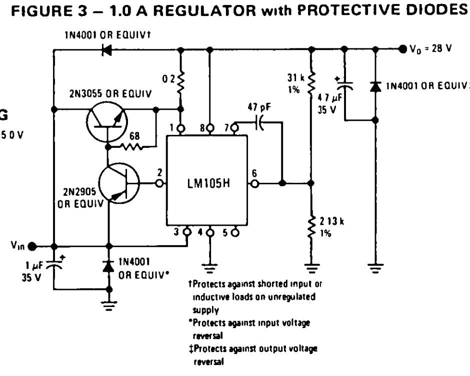


FIGURE 3 – 1.0 A REGULATOR with PROTECTIVE DIODES



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	LM105	LM205	LM305	Unit
Input Voltage	V_{in}	50	50	40	Vdc
Input-Output Voltage Differential	$\|V_{in}-V_O\|$	40	40	40	Vdc
Power-Dissipation (See Note 1)	P_D	680	680	680	mW
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C
Lead Temperature (soldering, t = 10 s)	T_S	300	300	300	°C

ELECTRICAL CHARACTERISTICS (See Note 2)

Characteristic	Symbol	LM105 LM205			LM305			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	8.5	–	50	8.5	–	40	Volts
Output Voltage Range	V_O	4.5	–	40	4.5	–	30	Volts
Output-Input Voltage Differential	$\|V_{in}-V_O\|$	3.0	–	30	3.0	–	30	Volts
Load Regulation (See Figure 1) ($0 \leqslant I_O \leqslant 12$ mA)	Reg_{load}							%
R_{SC} = 18 Ω, T_A = +25°C		–	0.02	0.05	–	0.02	0.05	
R_{SC} = 10 Ω, T_A = T_{high}*		–	0 03	0.1	–	0.03	0.1	
R_{SC} = 18 Ω, T_A = T_{low}**		–	0.03	0.1	–	0.03	0.1	
Line Regulation	Reg_{in}							%/V
$V_{in}-V_O \leqslant 5.0$ V		–	0.025	0.06	–	0.025	0.06	
$V_{in}-V_O > 5.0$ V		–	0.015	0.03	–	0.015	0.03	
Ripple Rejection (See Figure 1) C_{ref} = 10 μF, f = 120 Hz	$\frac{\Delta V_O}{V_O \Delta V_i}$	–	0.003	0.01	1.0	0.003	0.01	%/V
Temperature Stability $T_{low}** \leqslant T_A \leqslant T_{high}*$	TCV_O	–	0.3	1.0	–	0.3	1.0	%
Feedback Sense Voltage	V_{ref}	1.63	1.7	1.81	1.63	1.7	1.81	Volts
Output Noise Voltage (See Figure 1) ($10\ Hz \leqslant f \leqslant 10\ kHz$)	V_n							%
C_{Ref} = 0		–	0.005	–	–	0.005	–	
$C_{Ref} > 0.1$ μF		–	0.002	–	–	0.002	–	
Standby Current Drain	I_B							mA
V_{in} = 50 V		–	0.8	2.0	–	–	–	
V_{in} = 40 V		–	–	–	–	0.8	2.0	
Long Term Stability	S	–	0.1	1.0	–	0.1	1.0	%

*T_{high} = +125°C for LM105
+85°C for LM205
+70°C for LM305

**T_{low} = -55°C for LM105
-25°C for LM205
0°C for LM305

Note 1:

The maximum junction temperature of the LM105 is +150°C, for the LM205 – +100°C, and for the LM305 – +85°C For operating at elevated temperatures, the package must be derated based on a thermal resistance of 150°C/W – junction to ambient, or 45°C/W junction to case

Note 2:

These specifications apply for junction temperatures of −55°C to +150°C for the LM105, −25°C to +85°C for the LM205, and 0 to +70°C for the LM305 Specifications also apply for input and output voltages within the indicated ranges and for a divider impedance sensed by the feedback terminal of 2 0 kilohms (unless otherwise specified) Load and line regulation specifications given are for constant junction temperature Temperature drift effects must be taken into account separately when the device is operating under conditions of high power dissipation

LM109
LM209
LM309

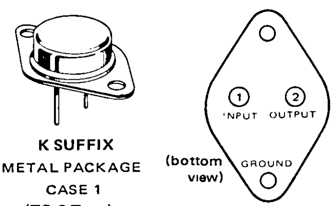
MONOLITHIC POSITIVE THREE - TERMINAL FIXED VOLTAGE REGULATOR

A versatile positive fixed +5.0-volt regulator designed for easy application as on on-card, local voltage regulator for digital logic systems. Current limiting and thermal shutdown are provided to make the units extremely rugged.

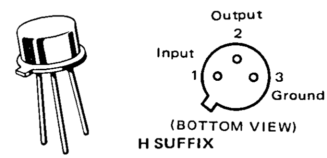
In most applications only one external component, a capacitor, is required in conjunction with the LM109 Series devices. Even this component may be omitted if the power-supply filter is not located an appreciable distance from the regulator.

- High Maximum Output Current – Over 1.0 Ampere in TO-3 type Package – Over 200 mA in TO-39 type Package.
- Minimum External Components Required
- Internal Short-Circuit Protection
- Internal Thermal Overload Protection
- Excellent Line and Load Transient Rejection
- Designed for Use with Popular MDTL and MTTL Logic

POSITIVE VOLTAGE REGULATOR



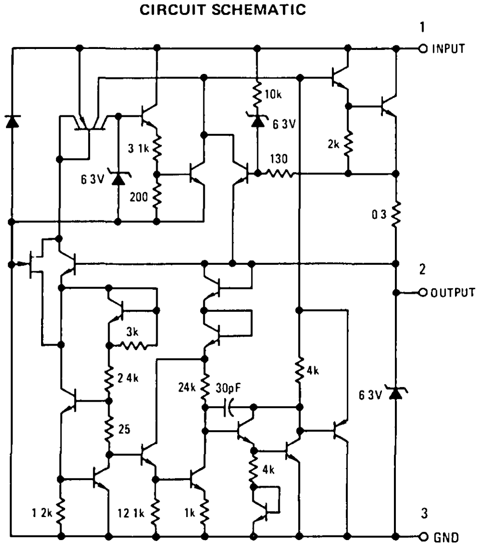
K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 Type)



H SUFFIX
METAL PACKAGE
CASE 79
(TO-39)

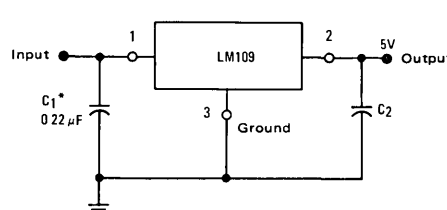
ORDERING INFORMATION		
Device	Temperature Range	Package
LM109H	T_J = –55°C to +150°C	Metal Can
LM109K	T_J = –55°C to +150°C	Metal Power
LM209H	T_J = –55°C to +150°C	Metal Can
LM209K	T_J = –55°C to +150°C	Metal Power
LM309H	T_J = 0°C to +125°C	Metal Can
LM309K	T_J = 0°C to +125°C	Metal Power

CIRCUIT SCHEMATIC



TYPICAL APPLICATION

FIXED 5.0 V REGULATOR



*Required if regulator is located an appreciable distance from power supply filter.
Although no output capacitor is needed for stability, it does improve transient response.

4

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation	P_D	Internally Limited	
Junction Temperature Range	T_J		°C
LM109		-55 to +150	
LM209		-55 to +150	
LM309		0 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (soldering, t = 60 s)	T_S	300	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	LM109/LM209 ①			LM309 ②			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4 7	5 05	5 3	4 8	5 05	5 2	Vdc
Input Regulation (T_J = +25°C) 7 0 ≤ V_{in} ≤ 25 V	Reg_{in}	–	4 0	50	–	4 0	50	mV
Load Regulation (T_J = +25°C)	Reg_{load}							mV
Case 11-01 (type TO-3) 5 0 mA ≤ I_O ≤ 1 5A		–	50	100	–	50	100	
Case 79-02 (TO-39) 5 0 mA ≤ I_O ≤ 0 5A		–	20	50	–	20	50	
Output Voltage Range 7 0 V ≤ V_{in} ≤ 25 V 5 0 mA ≤ I_O ≤ I_{max}, P ≤ P_{max}	V_O	4 6	–	5 4	4 75	–	5 25	Vdc
Quiescent Current (7 0 V ≤ V_{in} ≤ 25 V)	I_B	–	5 2	10	–	5 2	10	mAdc
Quiescent Current Change (7 0 V ≤ V_{in} ≤ 25 V)	ΔI_B		–	0 5	–	–	0 5	
5 0 mA ≤ I_O ≤ I_{max}		–	–	0 8	–	–	0 8	
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_N	–	40	–	–	40	–	µV
Long Term Stability	S	–	–	10	–	–	20	mV
Thermal Resistance, Junction to Case ③	θJC							°C/W
Case 1, (type TO-3)		–	3 0	–	–	3 0	–	
Case 79-02 (TO-39)		–	15	–	–	15	-	

NOTES

① Unless otherwise specified, these specifications apply for -55°C ≤ T_J ≤ +150° (-25°C ≤ T_J ≤ +150°C for the LM209) For Case 79 02 (TO 39) V_{in} - 10 V, I_O = 0 1 A, I_{max} = 0 2 A and P_{max} = 2 0 W For Case 1 (type TO-3) V_{in} = 10 V, I_O = 0 5 A, I_{max} = 1 0 A and P_{max} = 20 W

② Unless otherwise specified, these specifications apply for 0°C ≤ T_J ≤ +125°C, V_{in} = 10V For Case 79 02 (TO 39) I_O = 0 1A, I_{max} = 0 2A and P_{max} = 2 0 W For Case 1 (type TO 3) I_O = 0 5 A, I_{max} = 1 0 A and P_{max} = 20 W

③ Without a heat sink, the thermal resistance of the Case 79 02 (TO-39) package is about 150°C/W, while that of the Case 1 (type TO 3) package is aoproximately 35°C/W With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the heat sink

TYPICAL CHARACTERISTICS

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION (LM109K, LM209K)

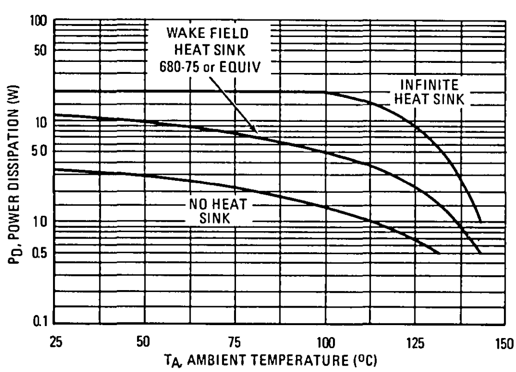
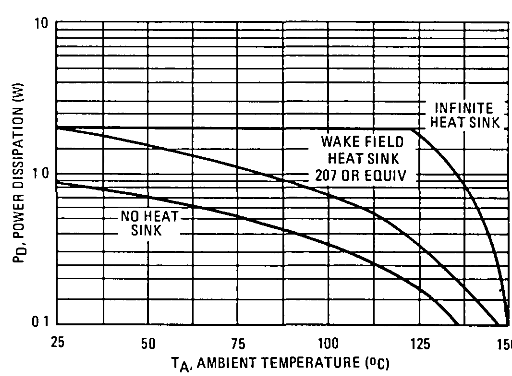


FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION (LM109H, LM209H)



TYPICAL CHARACTERISTICS (continued)

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 3 – MAXIMUM AVERAGE POWER DISSIPATION (LM309K)

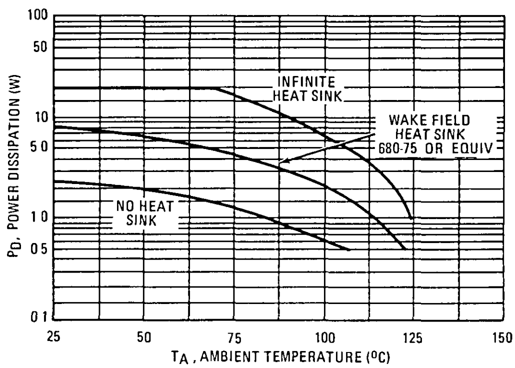


FIGURE 4 – MAXIMUM AVERAGE POWER DISSIPATION (LM309H)

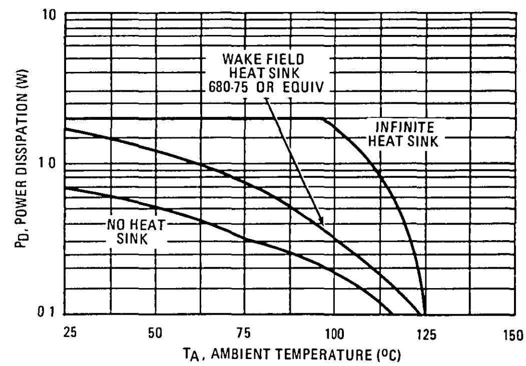


FIGURE 5 - OUTPUT IMPEDANCE versus FREQUENCY

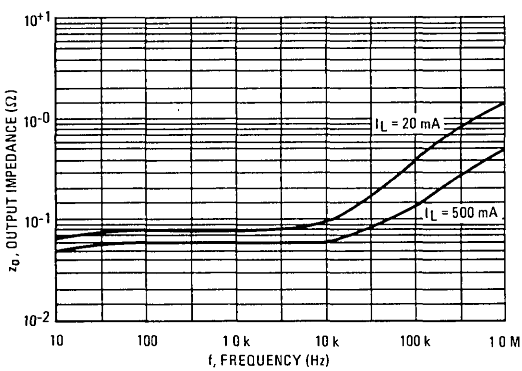


FIGURE 6 – PEAK OUTPUT CURRENT (K PACKAGE)

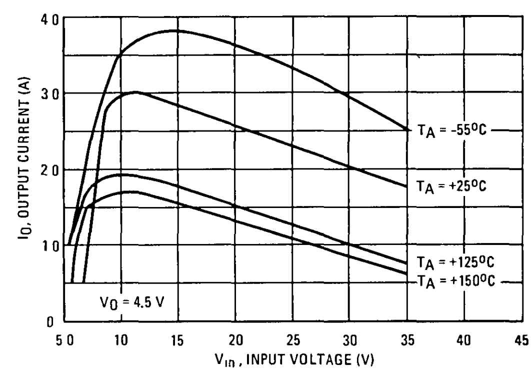


FIGURE 7 – PEAK OUTPUT CURRENT (H PACKAGE)

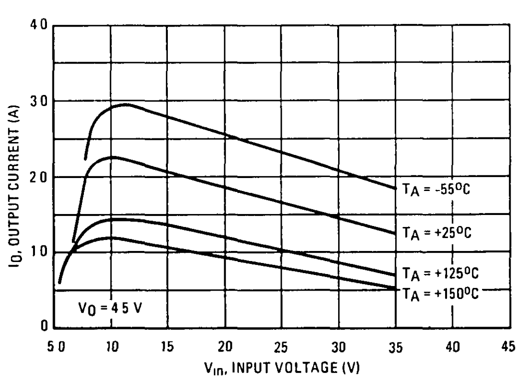
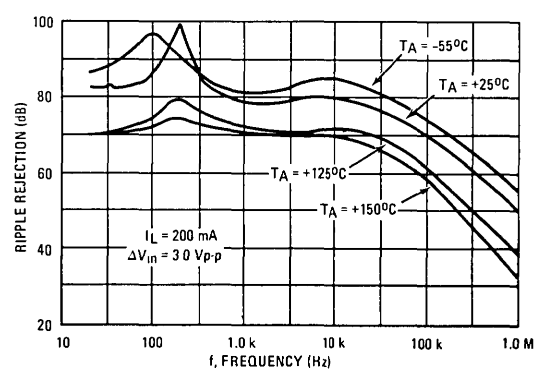


FIGURE 8 – RIPPLE REJECTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DROPOUT VOLTAGE

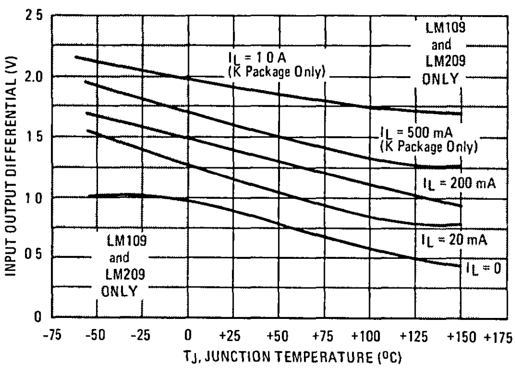


FIGURE 10 – DROPOUT CHARACTERISTIC (K PACKAGE)

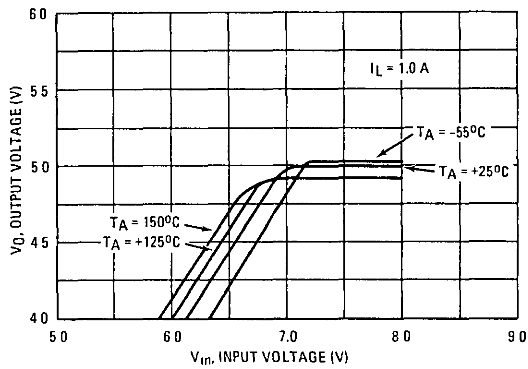


FIGURE 11 – OUTPUT VOLTAGE

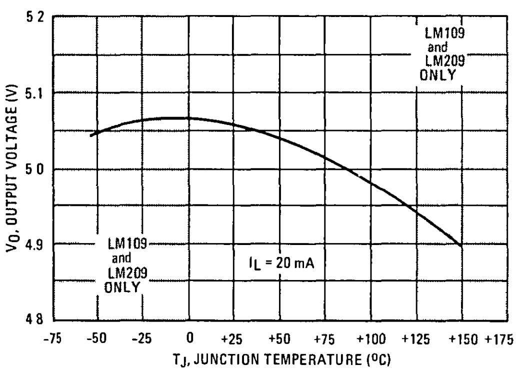


FIGURE 12 – OUTPUT NOISE VOLTAGE

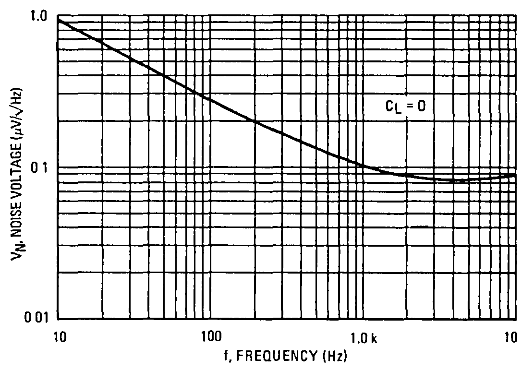


FIGURE 13 – QUIESCENT CURRENT

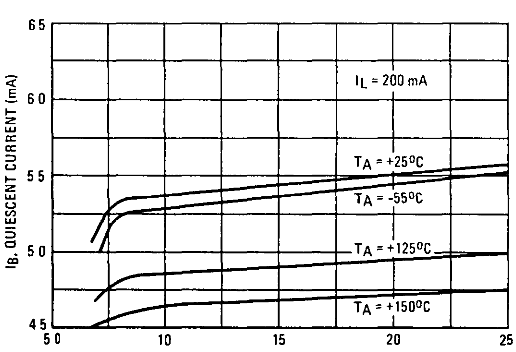
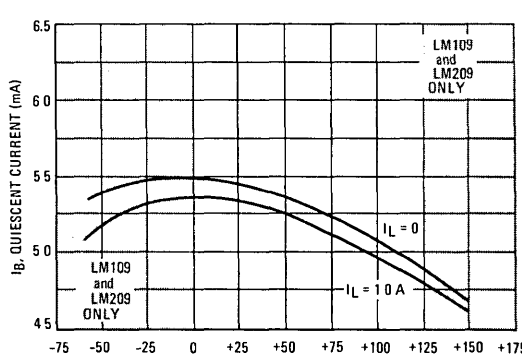


FIGURE 14 – QUIESCENT CURRENT



TYPICAL APPLICATIONS

FIGURE 15 – ADJUSTABLE OUTPUT REGULATOR

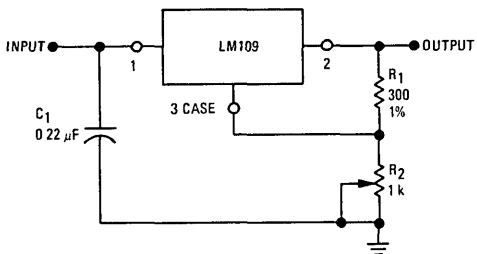


FIGURE 16 – CURRENT REGULATOR

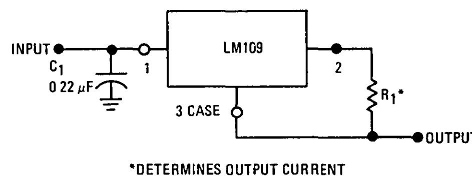


FIGURE 17 – 5.0-VOLT, 3.0-AMPERE REGULATOR
(with plastic boost transistor)

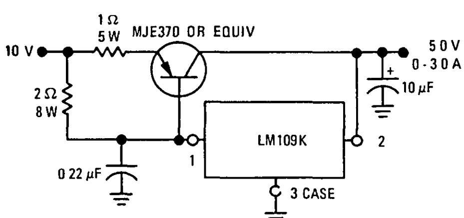


FIGURE 18 – 5.0 VOLT, 4.0-AMPERE TRANSISTOR
(with plastic Darlington boost transistor)

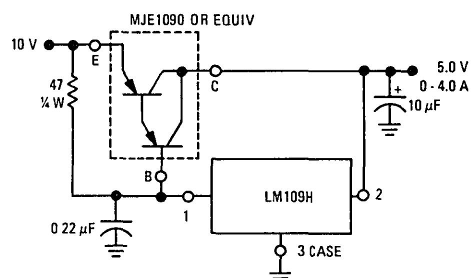


FIGURE 19 – 5.0-VOLT, 10-AMPERE REGULATOR

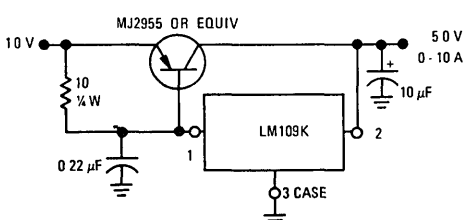
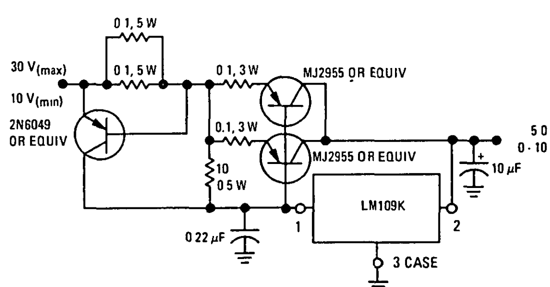


FIGURE 20 – 5.0-VOLT, 10-AMPERE REGULATOR
(with Short-Circuit Current Limiting for
Safe-Area Protection of pass transistors)



LM117
LM217
LM317

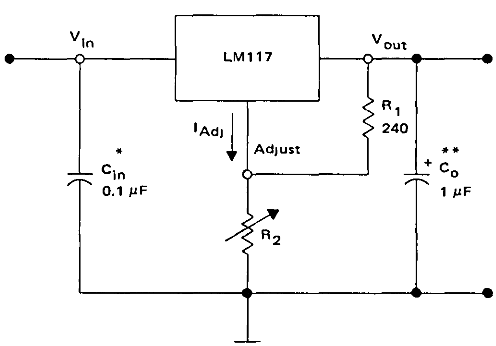
3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

The LM117/217/317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117 series serve a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in TO-3 and TO-220 Packages
- Output Current in Excess of 0.5 Ampere in TO-39 Package
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability, however it does improve transient response.

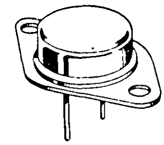
$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

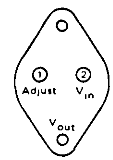
Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications

3-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 Type)

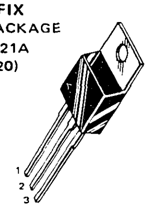




(Bottom View)

Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

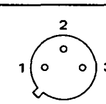
T SUFFIX
PLASTIC PACKAGE
CASE 221A
(TO-220)



Pin 1 Adjust
Pin 2 V_{out}
Pin 3 V_{in}

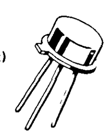
Heatsink surface connected to Pin 2

H SUFFIX
METAL PACKAGE
CASE 79
(TO-39)



(Bottom View)

(Case is output)



Pin 1 V_{in}
Pin 2 Adjust
Pin 3 V_{out}

ORDERING INFORMATION

Device	Temperature Range	Package
LM117H	T_J = -55°C to +150°C	Metal Can
LM117K	T_J = -55°C to +150°C	Metal Power
LM217H	T_J = -25°C to +150°C	Metal Can
LM217K	T_J = -25°C to +150°C	Metal Power
LM317H	T_J = 0°C to +125°C	Metal Can
LM317K	T_J = 0°C to +125°C	Metal Power
LM317T	T_J = 0°C to +125°C	Plastic Power

4

4

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J		°C
LM117		-55 to +150	
LM217		-25 to +150	
LM317		0 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_I - V_O$ = 5 V; I_O = 0.5 A for K and T packages; I_O = 0.1 A for H package; $T_J = T_{low}$ to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117/217 Min	LM117/217 Typ	LM117/217 Max	LM317 Min	LM317 Typ	LM317 Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	–	0.01	0.02	–	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}							
V_O ≤ 5 V			–	5	15	–	5	25	mV
V_O ≥ 5 V			–	0.1	0.3	–	0.1	0.5	% V_O
Adjustment Pin Current	3	I_{Adj}	–	50	100	–	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ $V_I - V_O$ ≤ 40 V 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1, 2	ΔI_{Adj}	–	0.2	5	–	0.2	5	μA
Reference Voltage (Note 4) 3 V ≤ $V_I - V_O$ ≤ 40 V 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 3) 3 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	–	0.02	0.05	–	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}							
V_O ≤ 5 V			–	20	50	–	20	70	mV
V_O ≥ 5 V			–	0.3	1	–	0.3	1.5	%V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.7	–	–	0.7	–	%V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O$ = 40 V)	3	I_{Lmin}	–	3.5	5	–	3.5	10	mA
Maximum Output Current $V_I - V_O$ ≤ 15 V, P_D ≤ P_{max}	3	I_{max}							A
K and T Packages			1.5	2.2	–	1.5	2.2	–	
H Package			0.5	0.8	–	0.5	0.8	–	
$V_I - V_O$ = 40 V, P_D ≤ P_{max}, T_A = 25°C									
K and T Packages			0.25	0.4	–	0.15	0.4	–	
H Package			–	0.07	–	–	0.07	–	
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 KHz	–	N	–	0.003	–	–	0.003	–	%V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5)	4	RR							dB
Without C_{ADJ}			–	65	–	–	65	–	
C_{ADJ} = 10 μF			66	80	–	66	80	–	
Long Term Stability, $T_J = T_{high}$ (Note 6) T_A = 25°C for Endpoint Measurements	3	S	–	0.3	1	–	0.3	1	%/1.0k Hrs
Thermal Resistance Junction to Case	–	$R_{\theta JC}$							°C/W
H Package (TO-39)			–	12	15	–	12	15	
K Package (TO-3)			–	2.3	3	–	2.3	3	
T Package (TO-220)			–	–	–	–	5	–	

NOTES:
(1) T_{low} = -55°C for LM117, T_{high} = +150°C for LM117
= -25°C for LM217, = +150°C for LM217
= 0°C for LM317, = +125°C for LM317
(2) I_{max} = 1.5 A for K (TO-3) and T (TO-220) Packages
= 0.5 A for H (TO-39) Package
P_{max} = 20 W for K (TO-3) and T (TO-220) Packages
= 2 W for H (TO-39) Package
(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
(4) Selected devices with tightened tolerance reference voltage available.
(5) C_{ADJ}, when used, is connected between the adjustment pin and ground.
(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

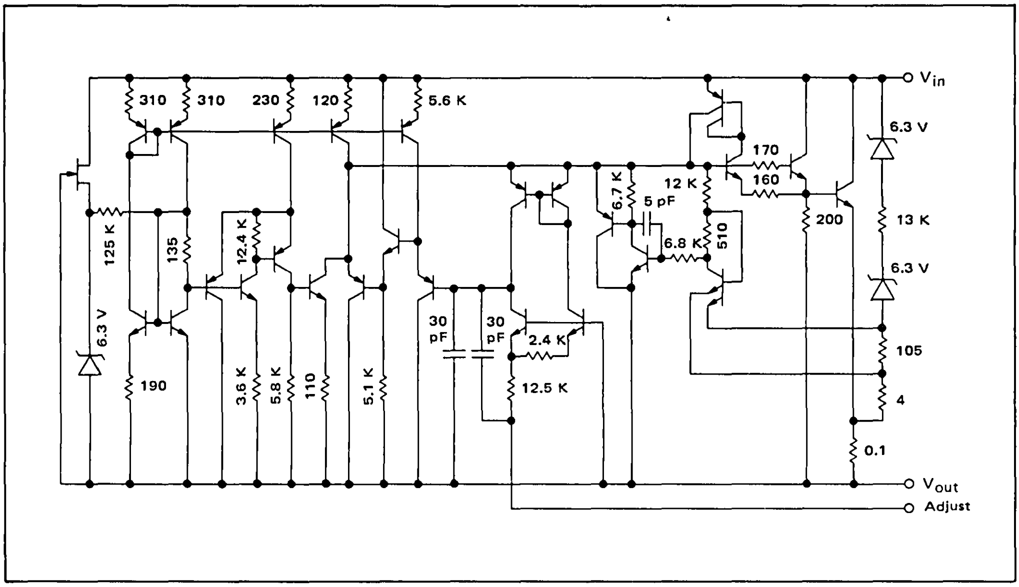


FIGURE 1 – LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

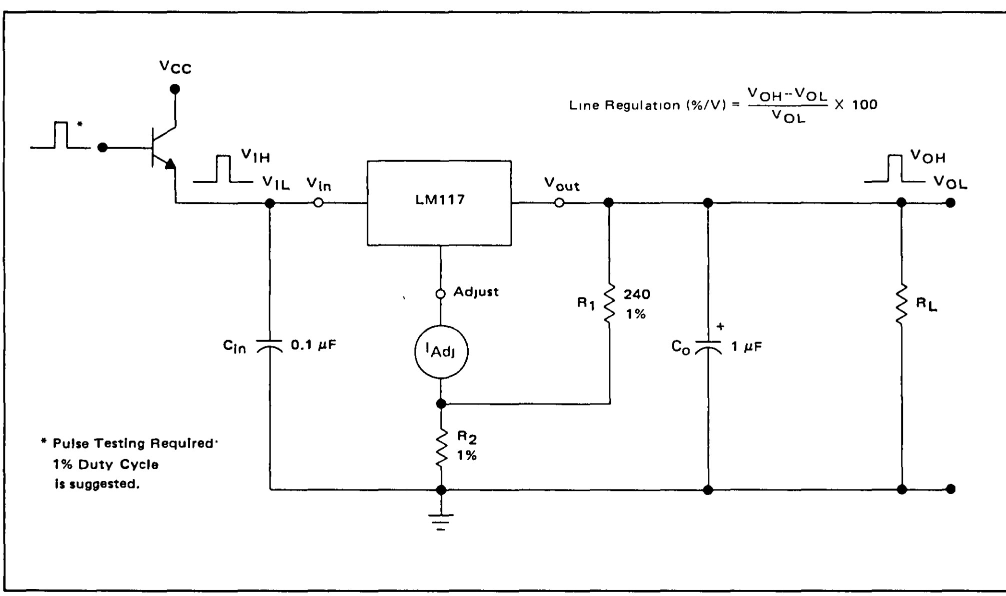


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FIGURE 2 – LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

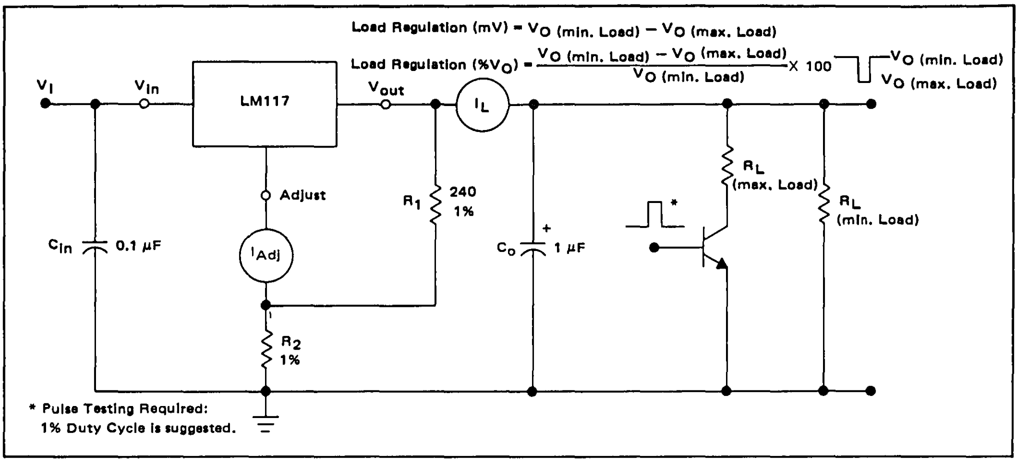


FIGURE 3 – STANDARD TEST CIRCUIT

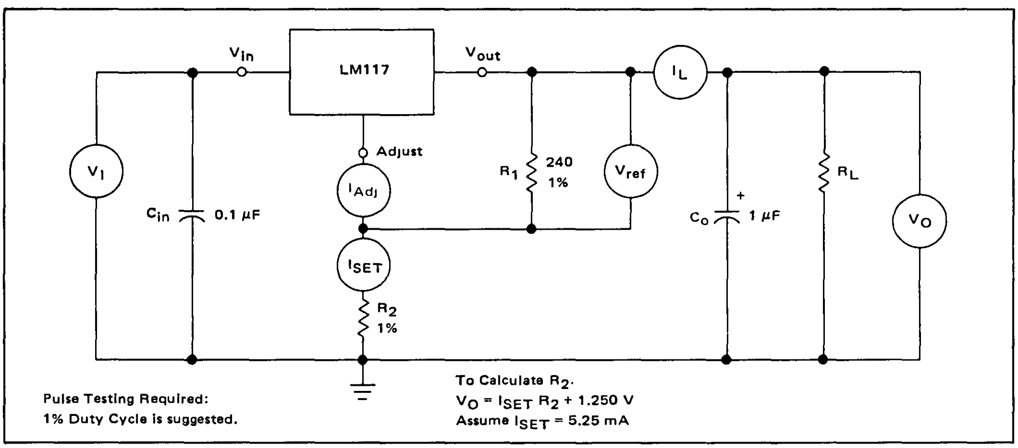


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT

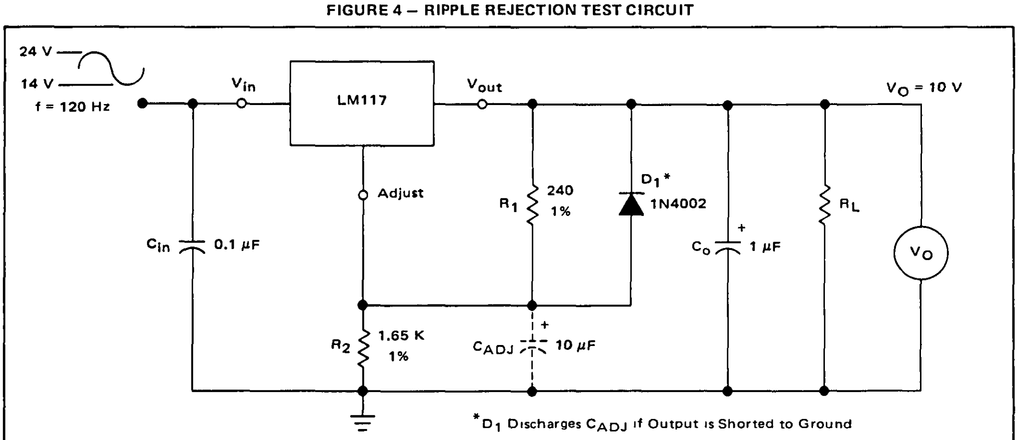


FIGURE 5 – LOAD REGULATION

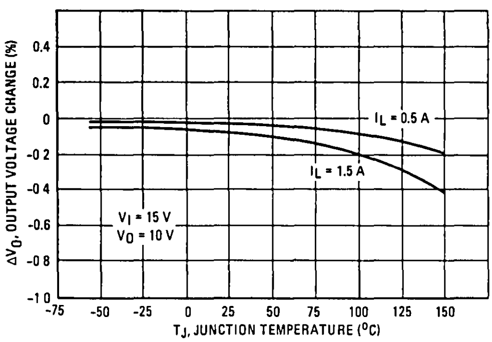


FIGURE 6 – CURRENT LIMIT

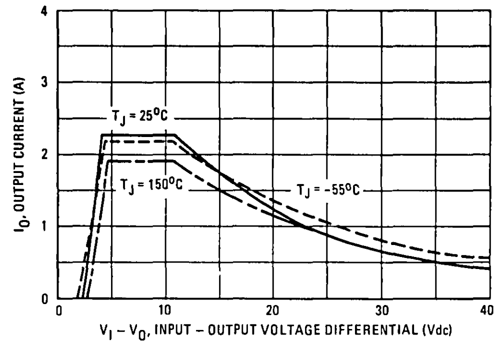


FIGURE 7 – ADJUSTMENT PIN CURRENT

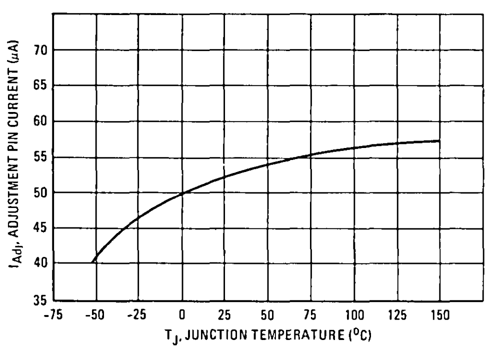


FIGURE 8 – DROPOUT VOLTAGE

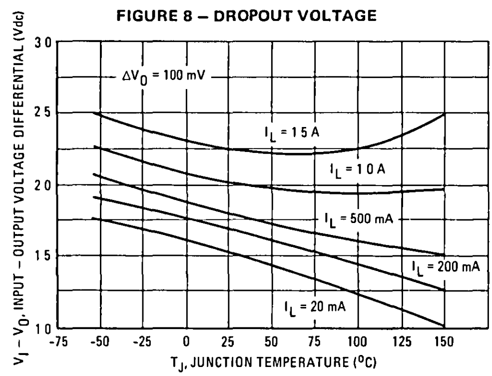


FIGURE 9 – TEMPERATURE STABILITY

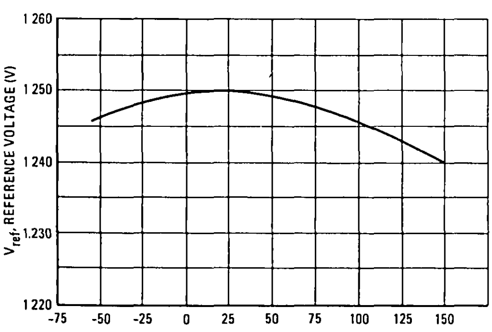


FIGURE 10 – MINIMUM OPERATING CURRENT

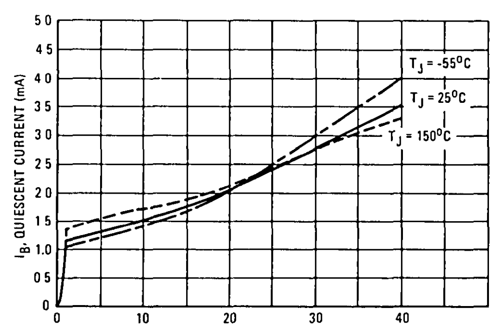


FIGURE 11 – RIPPLE REJECTION VS OUTPUT VOLTAGE

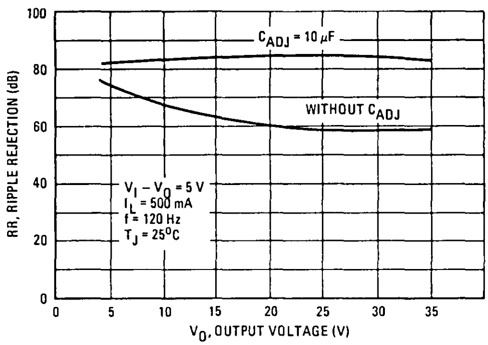


FIGURE 12 – RIPPLE REJECTION VS. OUTPUT CURRENT

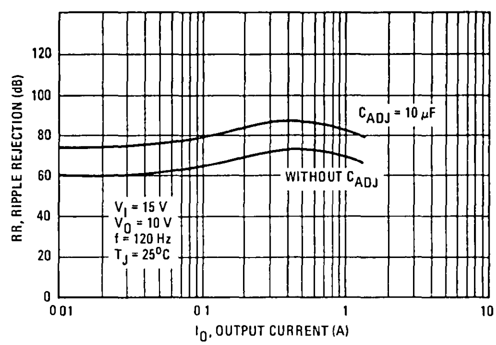


FIGURE 13 – RIPPLE REJECTION VS. FREQUENCY

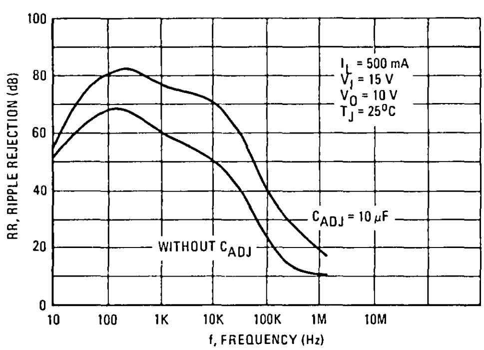


FIGURE 14 – OUTPUT IMPEDANCE

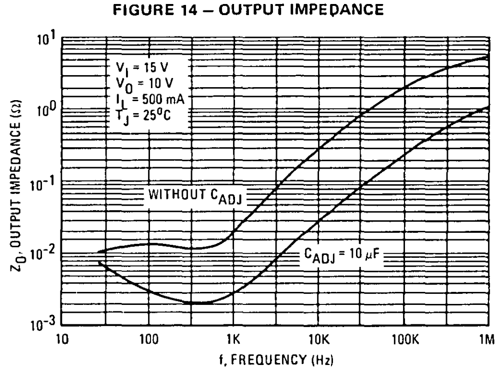


FIGURE 15 – LINE TRANSIENT RESPONSE

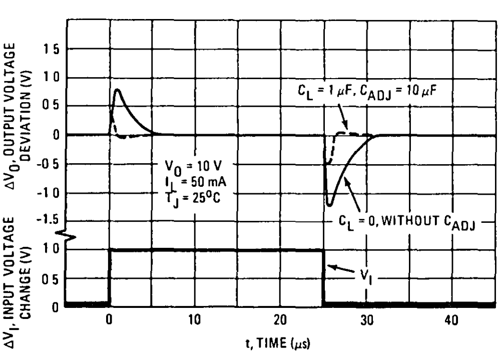
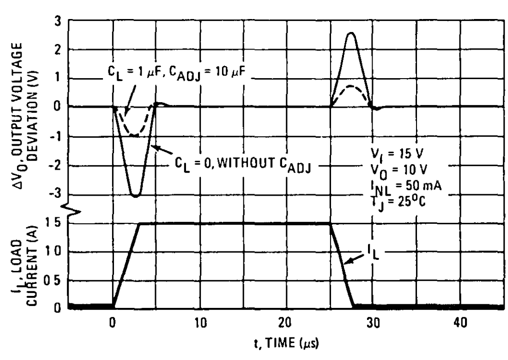


FIGURE 16 – LOAD TRANSIENT RESPONSE



4

APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

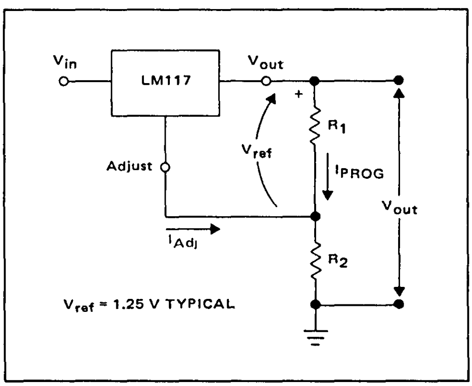
The LM117 is a 3-terminal floating regulator. In operation, the LM117 develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM117 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25\ \mu$F, $C_{ADJ} > 10\ \mu$F). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

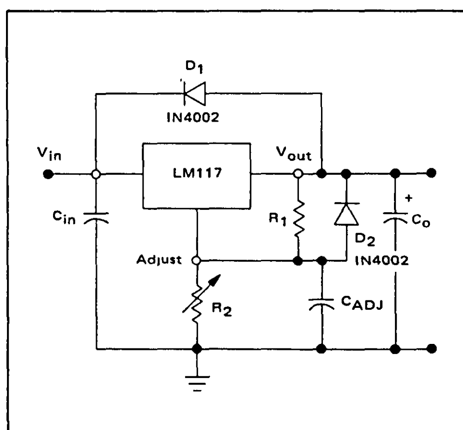


FIGURE 19 – "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE

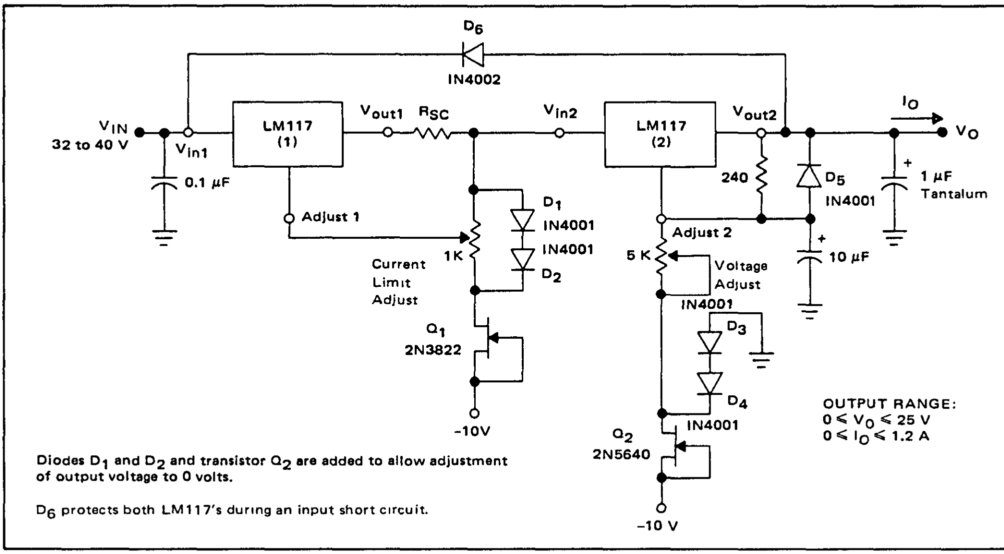


FIGURE 20 – ADJUSTABLE CURRENT LIMITER

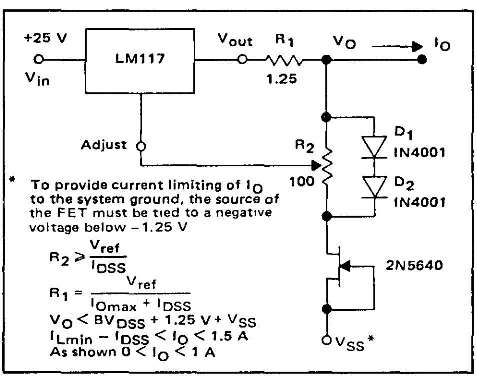


FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR

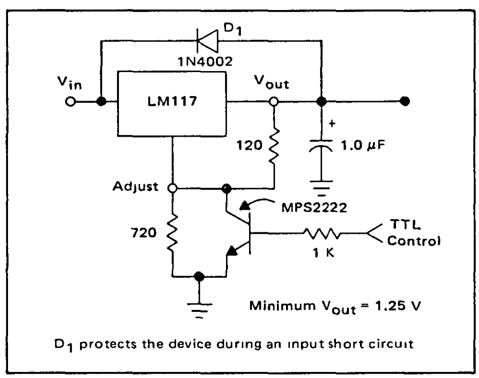


FIGURE 22 – SLOW TURN-ON REGULATOR

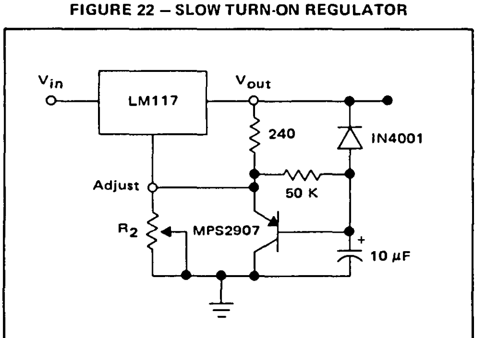
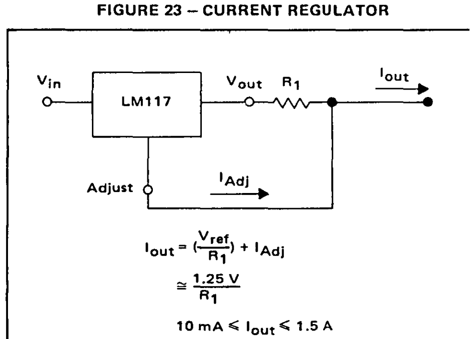


FIGURE 23 – CURRENT REGULATOR



4

LM117L
LM217L
LM317L

Advance Information

3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

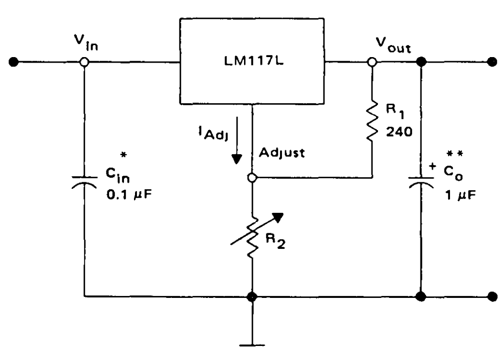
The LM117L/217L/317L are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117L series serves a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117L series can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

4

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications

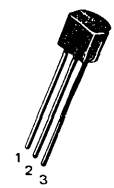
This is advance information and specifications are subject to change without notice.

LOW-CURRENT 3-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

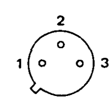
SILICON MONOLITHIC INTEGRATED CIRCUIT

Z SUFFIX
CASE 29
TO-92
PLASTIC PACKAGE
(LM317L only)

Pin 1 Adjust
Pin 2 V_{out}
Pin 3 V_{in}

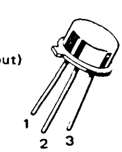


H SUFFIX
METAL PACKAGE
CASE 79
(TO-39)



(Bottom View)

(Case is output)



Pin 1 V_{in}
Pin 2 Adjust
Pin 3 V_{out}

ORDERING INFORMATION

Device	Temperature Range	Package
LM117LH	T_J = −55°C to +150°C	Metal Can
LM217LH	T_J = −25°C to +150°C	Metal Can
LM317LH	T_J = 0°C to +125°C	Metal Can
LM317LZ	T_J = 0°C to +125°C	Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J		°C
LM117L		-55 to +150	
LM217L		-25 to +150	
LM317L		0 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

4

ELECTRICAL CHARACTERISTICS

($V_I - V_O$ = 5 V; I_O = 40 mA; T_J = T_{low} to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117L/217L Min	LM117L/217L Typ	LM117L/217L Max	LM317L Min	LM317L Typ	LM317L Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	–	0.01	0.02	–	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 5 mA ≤ I_O ≤ I_{max}	2	Reg_{load}							
V_O ≤ 5 V			–	5	15	–	5	25	mV
V_O ≥ 5 V			–	0.1	0.3	–	0.1	0.5	% V_O
Adjustment Pin Current	3	I_{Adj}	–	50	100	–	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ $V_I - V_O$ ≤ 40 V 5 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1, 2	ΔI_{Adj}	–	0.2	5	–	0.2	5	μA
Reference Voltage (Note 4) 3 V ≤ $V_I - V_O$ ≤ 40 V 5 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 3) 3 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	–	0.02	0.05	–	0.02	0.07	%/V
Load Regulation (Note 3) 5 mA ≤ I_O ≤ I_{max}	2	Reg_{load}							
V_O ≤ 5 V			–	20	50	–	20	70	mV
V_O ≥ 5 V			–	0.3	1	–	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.7	–	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O$ = 40 V)	3	I_{Lmin}	–	3.5	5	–	3.5	5	mA
Maximum Output Current	3	I_{max}							
$V_I - V_O$ ≤ 20V, P_D ≤ P_{max} H Package			100	200	–	100	200	–	mA
$V_I - V_O$ ≤ 6 25 V, P_D ≤ P_{max} Z Package			100	200	–	100	200	–	
$V_I - V_O$ = 40 V, P_D ≤ P_{max}, T_A = 25°C H Package			–	50	–	–	50	–	nA
Z Package			–	20	–	–	20	–	
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 KHz	–	N	–	0.003	–	–	0.003	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5)	4	RR							dB
Without C_{ADJ}			–	65	–	–	65	–	
C_{ADJ} = 10 μF			–	80	–	–	80	–	
Long Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	–	0.3	1	–	0.3	1	%/1.0k Hrs
Thermal Resistance Junction to Case	–	$R_{\theta JC}$							°C/W
H Package (TO-39)			–	40	–	–	40	–	
Z Package (TO-92)			–	–	–	–	160	–	

NOTES: (1) T_{low} = -55°C for LM117L T_{high} = +150°C for LM117L
= -25°C for LM217L = +150°C for LM217L
= 0°C for LM317L = +125°C for LM317L

(2) I_{max} = 100 mA
P_{max} = 2 W for H (TO-39) Package
= 625 mW for Z (TO-92) Package

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{ADJ}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

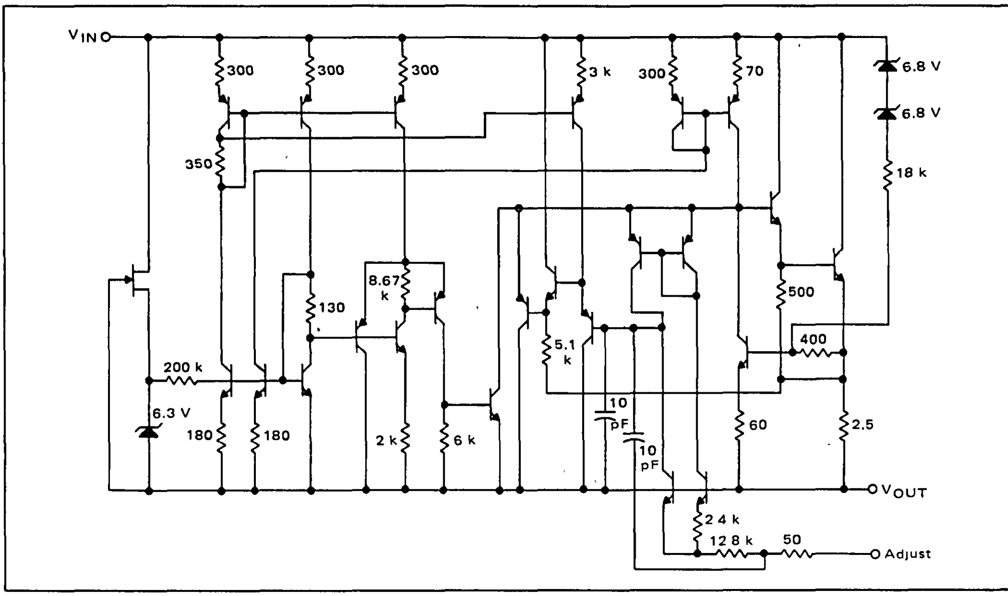


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FIGURE 1 – LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

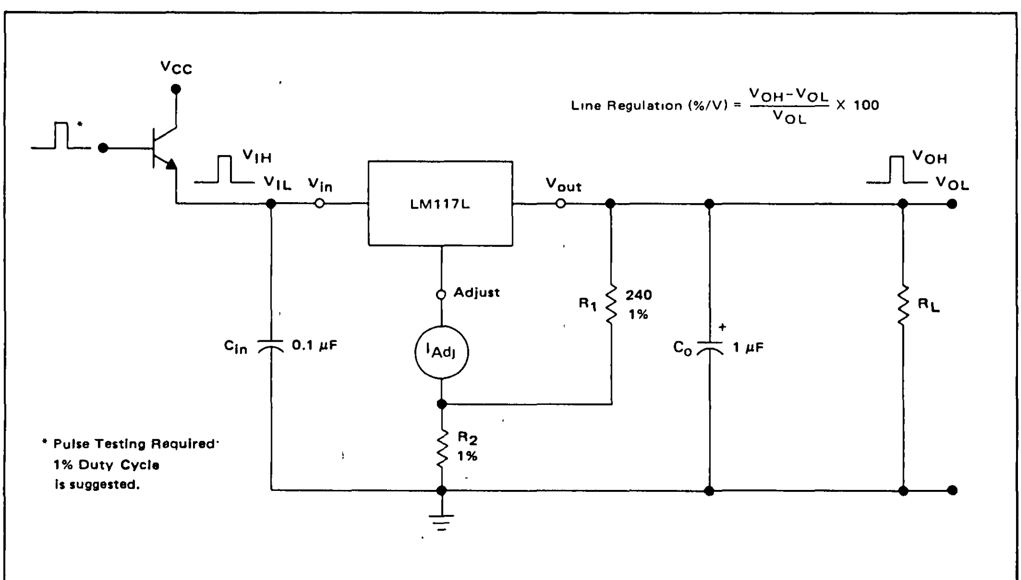

FIGURE 2 — LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

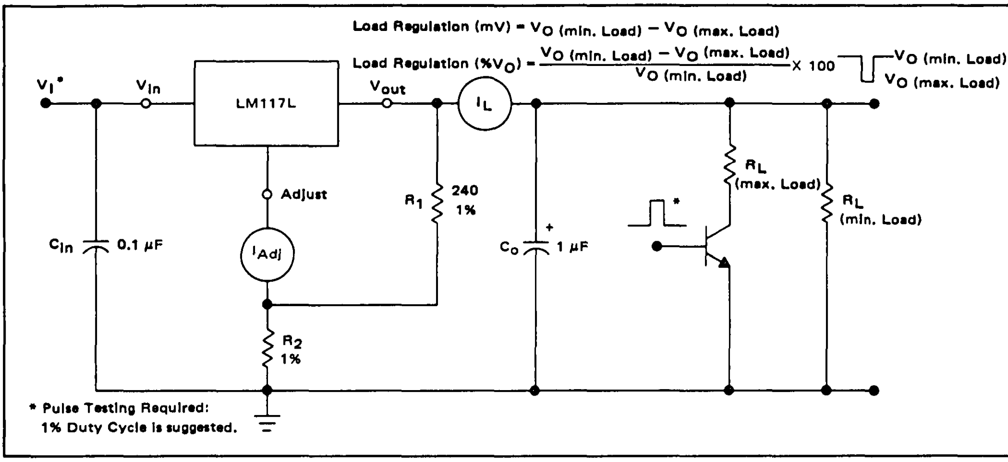

FIGURE 3 — STANDARD TEST CIRCUIT

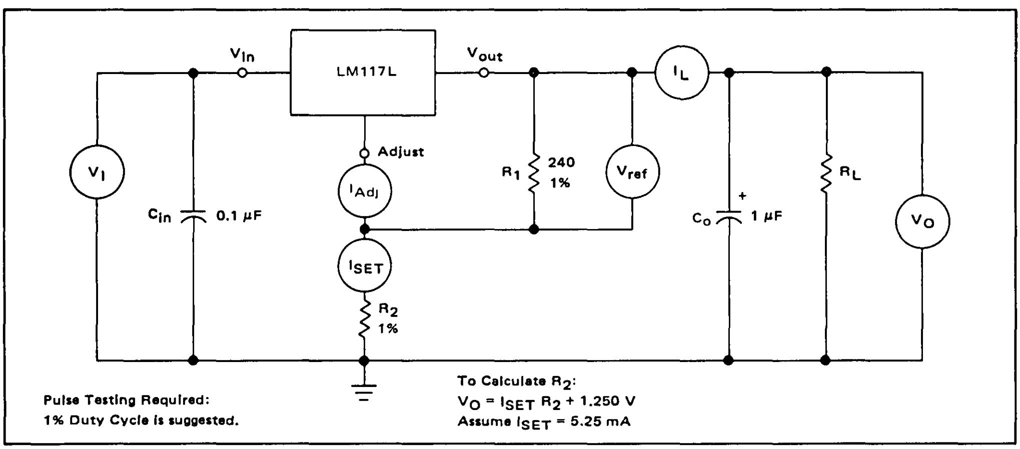

FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT

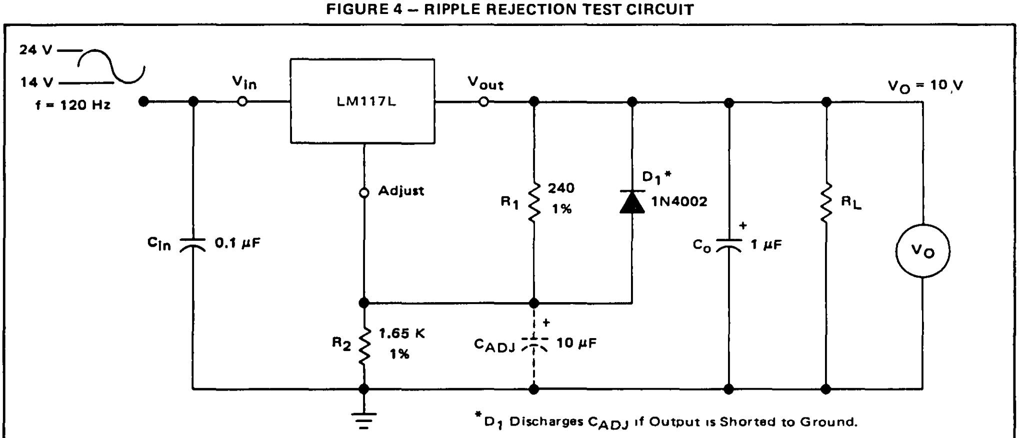

FIGURE 5 — LOAD REGULATION

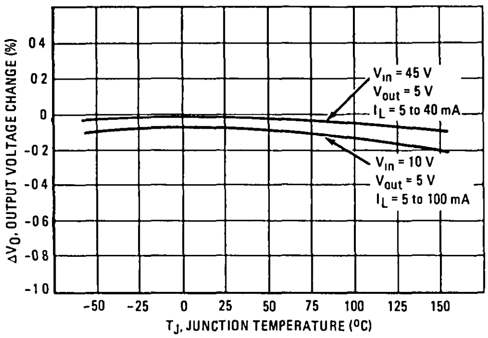

FIGURE 6 — RIPPLE REJECTION

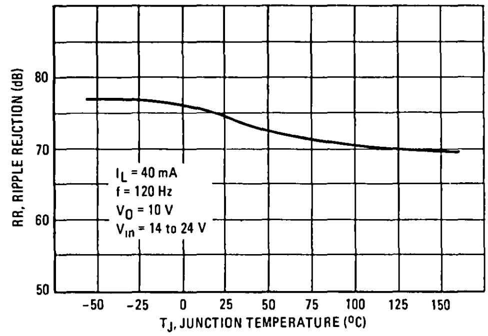

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FIGURE 7 — CURRENT LIMIT

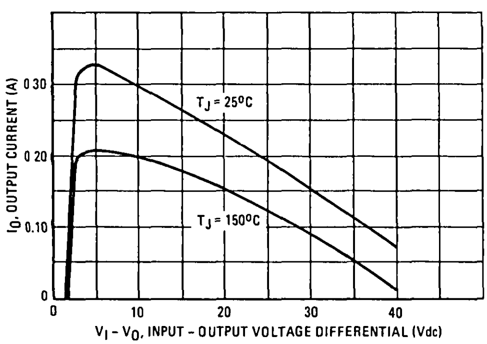


FIGURE 8 — DROPOUT VOLTAGE

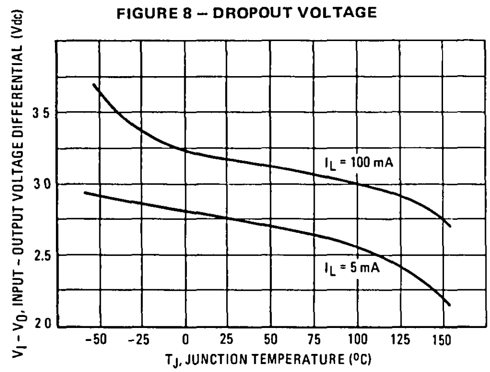


FIGURE 9 – TEMPERATURE STABILITY

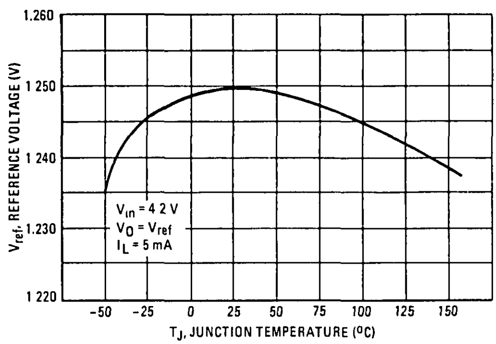


FIGURE 10 – ADJUSTMENT PIN CURRENT

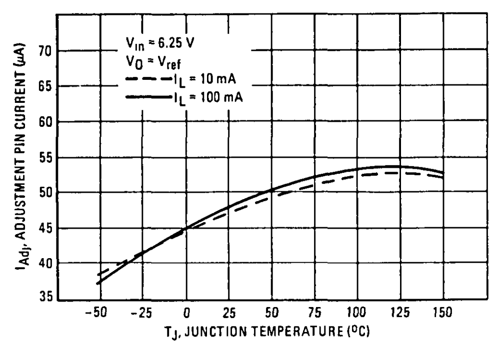


FIGURE 11 – LINE REGULATION

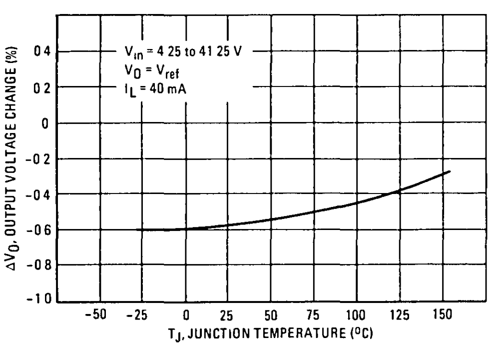
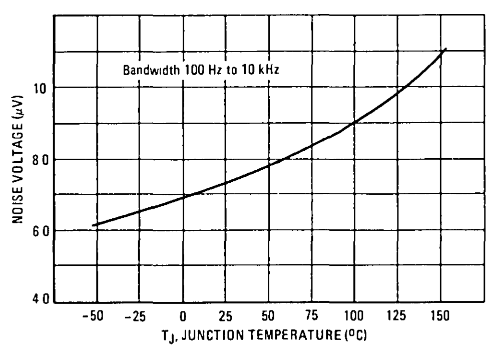


FIGURE 12 – OUTPUT NOISE



4

APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

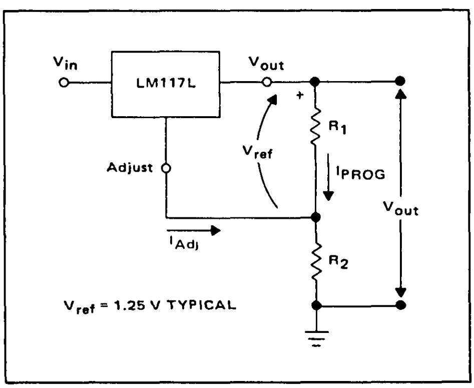
The LM117L is a 3-terminal floating regulator. In operation, the LM117L develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 13), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\, R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117L was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 13 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_o) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM117L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 10$ μF, $C_{ADJ} > 5$ μF). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 14 – VOLTAGE REGULATOR WITH PROTECTION DIODES

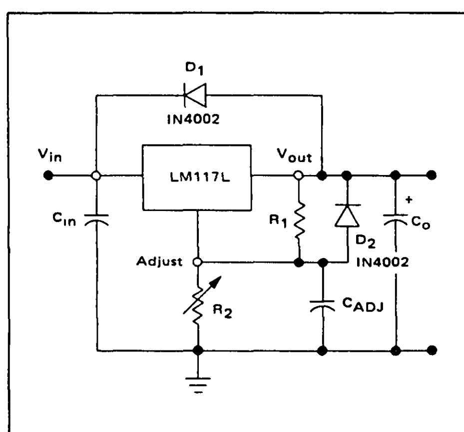


FIGURE 15 — ADJUSTABLE CURRENT LIMITER

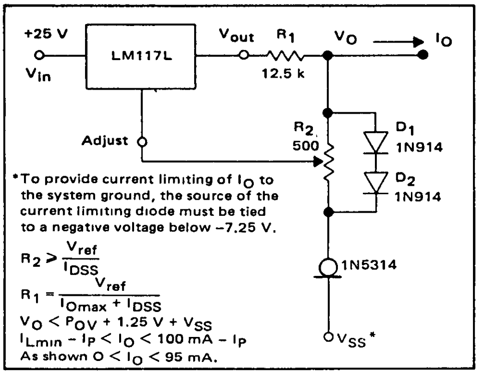


FIGURE 16 — 5 V ELECTRONIC SHUTDOWN REGULATOR

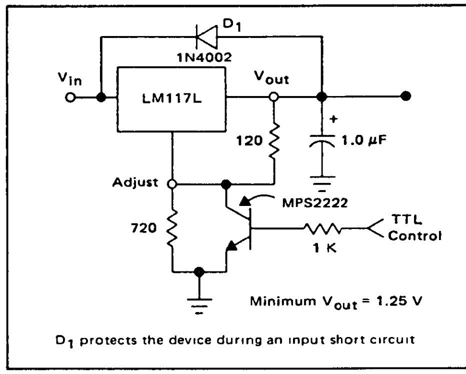


FIGURE 17 — SLOW TURN-ON REGULATOR

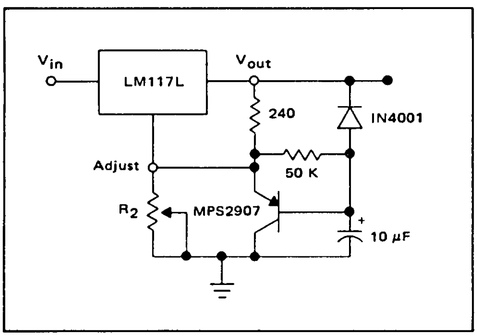
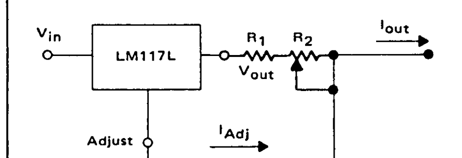


FIGURE 18 — CURRENT REGULATOR



$$I_{outmax} = \left(\frac{V_{ref}}{R_1}\right) + I_{adj} \cong \frac{1.25\ V}{R_1}$$

$$I_{outmin} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{adj} \cong \frac{1.25\ V}{R_1 + R_2}$$

$5\ mA < I_{out} < 100\ mA$

LM140 series
LM340 series

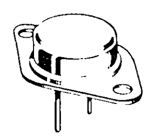
3-TERMINAL POSITIVE VOLTAGE REGULATORS

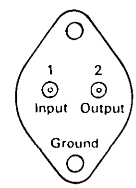
The LM140/340 series of three-terminal positive voltage regulators are monolithic integrated circuits designed for a wide variety of applications including local on-board regulation Available in seven fixed output voltage options from 5 0 to 24 volts, these regulators employ internal current limiting, thermal shutdown, and safe area compensation — making them virtually blowout proof The LM140/340 series is guaranteed to have line and load regulation that is a factor of two better than the 7800 series Although the LM140/340 series was designed primarily as a fixed regulator, it can be used with external components to obtain adjustable voltages

- Output Currents in Excess of 1 0 A
- Internal Thermal Overload Protection
- Internal Short Circuit Limiting
- Output Transistor Safe-Area Compensation
- No External Components Required
- Available in Both Commercial and Military Temperature Ranges

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 TYPE)





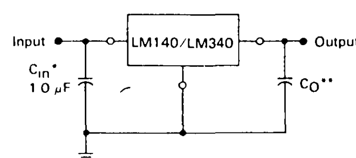
(bottom view)

Pins 1 and 2 electrically isolated from case Case is third electrical connection

ORDERING INFORMATION

Device	Voltage	Temperature Range (T_A)
LM140K-5 0	5 0 Volts	-55 to +125°C
LM140K-6 0	6 0 Volts	-55 to +125°C
LM140K-8 0	8 0 Volts	-55 to +125°C
LM140K-12	12 Volts	-55 to +125°C
LM140K-15	15 Volts	-55 to +125°C
LM140K-18	18 Volts	-55 to +125°C
LM140K-24	24 Volts	-55 to +125°C
LM340K-5 0	5 0 Volts	0 to +70°C
LM340K-6 0	6 0 Volts	0 to +70°C
LM340K-8 0	8 0 Volts	0 to +70°C
LM340K-12	12 Volts	0 to +70°C
LM340K-15	15 Volts	0 to +70°C
LM340K-18	18 Volts	0 to +70°C
LM340K-24	24 Volts	0 to +70°C

STANDARD APPLICATION



A common ground is required between the input and the output voltages The input voltage must remain typically 2 0 V above the output voltage even during the low point on the input ripple voltage

* = C_{in} (solid tantalum) is required, if regulator is located an appreciable distance from power supply filter

** = C_O is not needed for stability, however, it does improve transient response If needed, its value should be greater than 0 1 µF

LM140 series/LM340 series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Input Voltage	V_{in}		Vdc
(5 0 V - 18 V)		35	
(24 V)		40	
Power Dissipation and Thermal Characteristics			
(Metal Package)			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/R_{\theta JA}$	22 5	mW/°C
Thermal Resistance, Junction to Air	$R_{\theta JA}$	45	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +65°C (See Figure 2)	$1/R_{\theta JC}$	182	mW/°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5 5	°C/W
Storage Junction Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Range	T_J		°C
LM140		-55 to +150	
LM340		0 to +125	

NOTES

1 T_{low} = -55°C for LM140 T_{high} = +150°C for LM140
= 0°C for LM340 = +125°C for LM340

2 Load and line regulation are specified at constant junction temperature Changes in V_O due to heating effects must be taken into account separately Pulse testing with low duty cycle is used

4

LM140/340 — 5.0 ELECTRICAL CHARACTERISTICS

(V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.8	5.0	5.2	Vdc
Input Regulation (Note 2) 8.0 to 20 Vdc 7.0 to 25 Vdc (T_J = +25°C) 8.0 to 12 Vdc, I_O = 1.0 A 7.3 to 20 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{in}	 — — — —	 — — — —	 50 50 25 50	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — — —	 50 50 25	mV
Output Voltage LM140 8.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W LM340 7.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W	V_O	 4.75 4.75	 5.0 5.0	 5.25 5.25	Vdc
Quiescent Current I_O = 1.0 A LM140 LM340 LM140 (T_J = +25°C) LM340 (T_J = +25°C)	I_b	 — — — —	 4.0 4.0 4.0 4.0	 7.0 8.5 6.0 8.0	mA
Quiescent Current Change 8.0 ≤ V_{in} ≤ 25 Vdc — LM140 7.0 ≤ V_{in} ≤ 25 Vdc — LM340 5.0 mA ≤ I_O ≤ 1.0 A — LM140, LM340 8.0 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A — LM140 7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A — LM340	I_b	 — — — — —	 — — — — —	 0.8 1.0 0.5 0.8 1.0	mA
Ripple Rejection LM140 LM340 I_O = 1.0 A (T_J = +25°C) LM140 LM340	RR	 68 62 68 62	 80 80 — —	 — — — —	dB
Dropout Voltage	$V_{in} - V_O$	—	2.0	—	Vdc
Output Resistance	R_O	—	30	—	mΩ
Short-Circuit Current Limit	I_{sc}	—	2.0	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	40	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.6	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		7.3	—	—	Vdc

NOTES

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

4

4

LM140/340 — 6.0 ELECTRICAL CHARACTERISTICS

(V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5 0 mA to 1 0 A	V_O	5 75	6 0	6 25	Vdc
Input Regulation (Note 2) 9 0 to 21 Vdc 8 0 to 25 Vdc (T_J = +25°C) 9 0 to 13 Vdc, I_O = 1 0 A 8 3 to 21 Vdc, I_O = 1 0 A (T_J = +25°C)	Reg_{in}	 — — — —	 — — — —	 60 60 30 60	mV
Load Regulation (Note 2) 5 0 mA ≤ I_O ≤ 1 0 A 5 0 mA ≤ I_O ≤ 1 5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — — —	 60 60 30	mV
Output Voltage LM140 9 0 ≤ V_{in} ≤ 21 Vdc, 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W LM340 8 0 ≤ V_{in} ≤ 21 Vdc, 6 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W	V_O	 5 7 5 7	 6 0 5 0	 6 3 6 3	Vdc
Quiescent Current I_O = 1 0 A LM140 LM340 LM140 (T_J = +25°C) LM340 (T_J = +25°C)	I_b	 — — — —	 4 0 4 0 4 0 4 0	 7 0 8 5 6 0 8 0	mA
Quiescent Current Change 9 0 ≤ V_{in} ≤ 25 Vdc — LM140 8 0 ≤ V_{in} ≤ 25 Vdc — LM340 5 0 mA ≤ I_O ≤ 1 0 A — LM140, LM340 9 0 ≤ V_{in} ≤ 21 Vdc, I_O = 1 0 A — LM140 8 6 ≤ V_{in} ≤ 21 Vdc, I_O = 1 0 A — LM340	I_b	 — — — — —	 — — — — —	 0 8 1 0 0 5 0 8 1 0	mA
Ripple Rejection LM140 LM340 I_O = 1 0 A (T_J = +25°C) LM140 LM340	RR	 65 59 65 59	 78 78 — —	 — — — —	dB
Dropout Voltage	$V_{in} - V_O$	—	2 0	—	Vdc
Output Resistance	R_O	—	35	—	mΩ
Short-Circuit Current Limit	I_{sc}	—	1 9	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	45	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5 0 mA	TCV_O	—	±0 7	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2 4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1 0 A		8 3	—	—	Vdc

NOTES

1. T_{low} = −55°C for LM140 — T_{high} = +150°C for LM140
   = 0°C for LM340 — = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature Changes in V_O due to heating effects must be taken into account separately Pulse testing with low duty cycle is used

4

LM140/340 — 8.0 ELECTRICAL CHARACTERISTICS

(V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5 0 mA to 1 0 A	V_O	7 7	8 0	8 3	Vdc
Input Regulation (Note 2)	Reg_{in}				mV
11 to 23 Vdc		—	—	80	
10 5 to 25 Vdc (T_J = +25°C)		—	—	80	
11 to 17 Vdc, I_O = 1 0 A		—	—	40	
10 5 to 23 Vdc, I_O = 1 0 A (T_J = +25°C)		—	—	80	
Load Regulation (Note 2)	Reg_{load}				mV
5 0 mA ≤ I_O ≤ 1 0 A		—	—	80	
5 0 mA ≤ I_O ≤ 1 5 A (T_J = +25°C)		—	—	80	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	40	
Output Voltage	V_O				Vdc
LM140 11 5 ≤ V_{in} ≤ 23 Vdc, 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W		7 6	8 0	8 4	
LM340 10 5 ≤ V_{in} ≤ 23 Vdc, 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W		7 6	8 0	8 4	
Quiescent Current I_O = 1 0 A	I_b				mA
LM140		—	4 0	7 0	
LM340		—	4 0	8 5	
LM140 (T_J = +25°C)		—	4 0	6 0	
LM340 (T_J = +25°C)		—	4 0	8 0	
Quiescent Current Change	I_b				mA
11 5 ≤ V_{in} ≤ 25 Vdc LM140		—	—	0 8	
10 5 ≤ V_{in} ≤ 25 Vdc LM340		—	—	1 0	
5 0 mA ≤ I_O ≤ 1 0 A LM140, LM340		—	—	0 5	
11 5 ≤ V_{in} ≤ 23 Vdc, I_O = 1 0 A LM140		—	—	0 8	
10 6 ≤ V_{in} ≤ 23 Vdc, I_O = 1 0 A LM340		—	—	1 0	
Ripple Rejection	RR				dB
LM140		62	76	—	
LM340		56	76	—	
I_O = 1 0 A (T_J = +25°C)					
LM140		62	—	—	
LM340		56	—	—	
Dropout Voltage	V_{in} - V_O	—	2 0	—	Vdc
Output Resistance	R_O	—	40	—	mΩ
Short-Circuit Current Limit	I_{sc}	—	1 5	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	52	—	µV
Average Temperature Coefficient of Output Voltage I_O = 5 0 mA	TCV_O	—	±1 0	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2 4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1 0 A		10 5	—	—	Vdc

NOTES

1. T_{low} = −55°C for LM140; = 0°C for LM340. T_{high} = +150°C for LM140; = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used

LM140/340 — 12 ELECTRICAL CHARACTERISTICS

(V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11 5	12	12 5	Vdc
I_O = 5 0 mA to 1 0 A					
Input Regulation (Note 2)	Reg_{in}				mV
15 to 27 Vdc		—	—	120	
14 6 to 30 Vdc (T_J = +25°C)		—	—	120	
16 to 22 Vdc, I_O = 1 0 A		—	—	60	
14 6 to 27 Vdc, I_O = 1 0 A (T_J = +25°C)		—	—	120	
Load Regulation (Note 2)	Reg_{load}				mV
5 0 mA ≤ I_O ≤ 1 0 A		—	—	120	
5 0 mA ≤ I_O ≤ 1 5 A (T_J = +25°C)		—	—	120	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	60	
Output Voltage	V_O				Vdc
LM140					
15 5 ≤ V_{in} ≤ 27 Vdc, 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W		11 4	12	12 6	
LM340					
14 5 ≤ V_{in} ≤ 27 Vdc, 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W		11 4	12	12 6	
Quiescent Current	I_b				mA
I_O = 1 0 A					
LM140		—	4 0	7 0	
LM340		—	4 0	8 5	
LM140 (T_J = +25°C)		—	4 0	6 0	
LM340 (T_J = +25°C)		—	4 0	8 0	
Quiescent Current Change	I_b				mA
15 ≤ V_{in} ≤ 30 Vdc — LM140		—	—	0 8	
14 5 ≤ V_{in} ≤ 30 Vdc — LM340		—	—	1 0	
5 0 mA ≤ I_O ≤ 1 0 A — LM140, LM340		—	—	0 5	
15 ≤ V_{in} ≤ 27 Vdc, I_O = 1 0 A — LM140		—	—	0 8	
14 8 ≤ V_{in} ≤ 27 Vdc, I_O = 1 0 A — LM340		—	—	1 0	
Ripple Rejection	RR				dB
LM140		61	72	—	
LM340		55	72	—	
I_O = 1 0 A (T_J = +25°C)					
LM140		61	—	—	
LM340		55	—	—	
Dropout Voltage	$V_{in} - V_O$	—	2 0	—	Vdc
Output Resistance	R_O	—	75	—	mΩ
Short-Circuit Current Limit	I_{sc}	—	1 1	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5 0 mA	TCV_O	—	±1 5	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2 4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1 0 A		14 6	—	—	Vdc

NOTES

1 T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
= 0°C for LM340 = +125°C for LM340

2. Load and line regulation are specified at constant junction temperature Changes in V_O due to heating effects must be taken into account separately Pulse testing with low duty cycle is used

4

LM140/340 — 15 ELECTRICAL CHARACTERISTICS

(V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5 0 mA to 1.0 A	V_O	14 4	15	15 6	Vdc
Input Regulation (Note 2)	Reg_{in}				mV
18 5 to 30 Vdc		—	—	150	
17 5 to 30 Vdc (T_J = +25°C)		—	—	150	
20 to 26 Vdc, I_O = 1 0 A		—	—	75	
17 7 to 30 Vdc, I_O = 1 0 A (T_J = +25°C)		—	—	150	
Load Regulation (Note 2)	Reg_{load}				mV
5 0 mA ≤ I_O ≤ 1 0 A		—	—	150	
5 0 mA ≤ I_O ≤ 1 5 A (T_J = +25°C)		—	—	150	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	75	
Output Voltage	V_O				Vdc
LM140 18 5 ≤ V_{in} ≤ 30 Vdc, 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W		14 25	15	15 75	
LM340 17 5 ≤ V_{in} ≤ 30 Vdc, 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W		14 25	15	15 75	
Quiescent Current I_O = 1 0 A	I_b				mA
LM140		—	4 0	7 0	
LM340		—	4 0	8 5	
LM140 (T_J = +25°C)		—	4 0	6 0	
LM340 (T_J = +25°C)		—	4 0	8 0	
Quiescent Current Change	I_b				mA
18 5 ≤ V_{in} ≤ 30 Vdc LM140		—	—	0 8	
17 5 ≤ V_{in} ≤ 30 Vdc LM340		—	—	1 0	
5 0 mA ≤ I_O ≤ 1 0 A LM140, LM340		—	—	0 5	
18 5 ≤ V_{in} ≤ 30 Vdc, I_O = 1 0 A LM140		—	—	0 8	
17 9 ≤ V_{in} ≤ 30 Vdc, I_O = 1 0 A LM340		—	—	1 0	
Ripple Rejection	RR				dB
LM140		60	70	—	
LM340		54	70	—	
I_O = 1 0 A (T_J = +25°C) LM140		60	—	—	
LM340		54	—	—	
Dropout Voltage	V_{in} - V_O	—	2 0	—	Vdc
Output Resistance	R_O	—	95	—	mΩ
Short-Circuit Current Limit	I_{sc}	—	800	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	90	—	µV
Average Temperature Coefficient of Output Voltage I_O = 5 0 mA	TCV_O	—	±1 8	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2 4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1 0 A		17 7	—	—	Vdc

NOTES

1 T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
  = 0°C for LM340   = +125°C for LM340

2 Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately Pulse testing with low duty cycle is used

LM140/340 — 18 ELECTRICAL CHARACTERISTICS
(V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5 0 mA to 1 0 A	V_O	17 3	18	18 7	Vdc
Input Regulation (Note 2) 21 5 to 33 Vdc 21 to 33 Vdc (T_J = +25°C) 24 to 30 Vdc, I_O = 1 0 A 21 to 33 Vdc, I_O = 1 0 A (T_J = +25°C)	Reg_{in}	 — — — —	 — — — —	 180 180 90 180	mV
Load Regulation (Note 2) 5 0 mA ≤ I_O ≤ 1 0 A 5 0 mA ≤ I_O ≤ 1 5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — — —	 180 180 90	mV
Output Voltage LM140 22 ≤ V_{in} ≤ 33 Vdc, 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W LM340 21 ≤ V_{in} ≤ 33 Vdc, 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W	V_O	 17 1 17 1	 18 18	 18 9 18 9	Vdc
Quiescent Current I_O = 1 0 A LM140 LM340 LM140 (T_J = +25°C) LM340 (T_J = +25°C)	I_b	 — — — —	 4 0 4 0 4 0 4 0	 7 0 8 5 6 0 8 0	mA
Quiescent Current Change 22 ≤ V_{in} ≤ 33 Vdc LM140 21 ≤ V_{in} ≤ 33 Vdc LM340 5 0 mA ≤ I_O ≤ 1 0 A LM140, LM340 22 ≤ V_{in} ≤ 33 Vdc, I_O = 1 0 A LM140 21 ≤ V_{in} ≤ 33 Vdc, I_O = 1 0 A LM340	I_b	 — — — — —	 — — — — —	 0 8 1 0 0 5 0 8 1 0	mA
Ripple Rejection LM140 LM340 I_O = 1 0 A (T_J = +25°C) LM140 LM340	RR	 59 53 59 53	 69 69 — —	 — — — —	dB
Dropout Voltage	V_{in} - V_O	—	2 0	—	Vdc
Output Resistance	R_O	—	110	—	mΩ
Short-Circuit Current Limit	I_{sc}	—	500	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	110	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5 0 mA	TCV_O	—	±2 3	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2 4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1 0 A		21	—	—	Vdc

NOTES
1 T_{low} = -55°C for LM140 T_{high} = +150°C for LM140
= 0°C for LM340 = +125°C for LM340
2 Load and line regulation are specified at constant junction temperature Changes in V_O due to heating effects must be taken into account separately Pulse testing with low duty cycle is used

LM140/340 — 24 ELECTRICAL CHARACTERISTICS

(V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5 0 mA to 1 0 A	V_O	23	24	25	Vdc
Input Regulation (Note 2)	Reg_{in}				mV
28 to 38 Vdc		—	—	240	
27 to 38 Vdc (T_J = +25°C)		—	—	240	
30 to 36 Vdc, I_O = 1 0 A		—	—	120	
27 1 to 38 Vdc, I_O = 1 0 A (T_J = +25°C)		—	—	240	
Load Regulation (Note 2)	Reg_{load}				mV
5 0 mA ≤ I_O ≤ 1 0 A		—	—	240	
5 0 mA ≤ I_O ≤ 1 5 A (T_J = +25°C)		—	—	240	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	120	
Output Voltage	V_O				Vdc
LM140: 28 ≤ V_{in} ≤ 38 Vdc 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W		22 8	24	25 2	
LM340: 27 ≤ V_{in} ≤ 38 Vdc, 5 0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15 W		22 8	24	25 2	
Quiescent Current I_O = 1 0 A	I_b				mA
LM140		—	4 0	7 0	
LM340		—	4 0	8 5	
LM140 (T_J = +25°C)		—	4 0	6 0	
LM340 (T_J = +25°C)		—	4 0	8 0	
Quiescent Current Change	ΔI_b				mA
28 ≤ V_{in} ≤ 38 Vdc — LM140		—	—	0 8	
27 ≤ V_{in} ≤ 38 Vdc — LM340		—	—	1 0	
5 0 mA ≤ I_O ≤ 1 0 A — LM140, LM340		—	—	0 5	
28 ≤ V_{in} ≤ 38 Vdc, I_O = 1 0 A — LM140		—	—	0 8	
27 3 ≤ V_{in} ≤ 38 Vdc, I_O = 1 0 A — LM340		—	—	1 0	
Ripple Rejection	RR				dB
LM140		56	66	—	
LM340		50	66	—	
I_O = 1 0 A (T_J = +25°C) LM140		56	—	—	
LM340		50	—	—	
Dropout Voltage	V_{in} - V_O	—	2 0	—	Vdc
Output Resistance	R_O	—	150	—	mΩ
Short-Circuit Current Limit	I_{sc}	—	200	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	170	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5 0 mA	TCV_O	—	±3 0	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2 4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1 0 A		27 1	—	—	Vdc

NOTES

1 T_{low} = -55°C for LM140 = 0°C for LM340; T_{high} = +150°C for LM140 = +125°C for LM340

2 Load and line regulation are specified at constant junction temperature Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used

FIGURE 1 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE

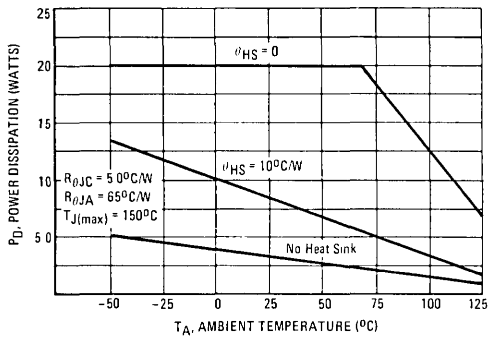


FIGURE 2 – DROPOUT CHARACTERISTICS

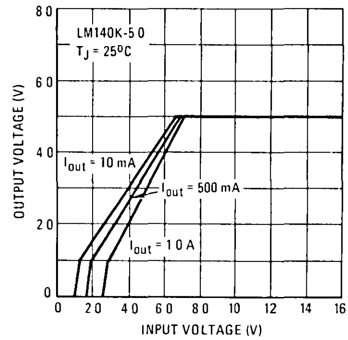


FIGURE 3 – INPUT-OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE

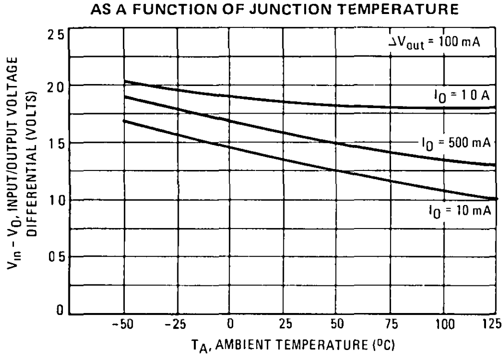


FIGURE 4 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

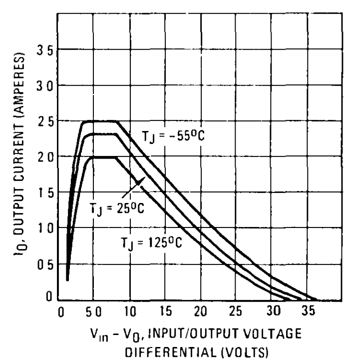


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

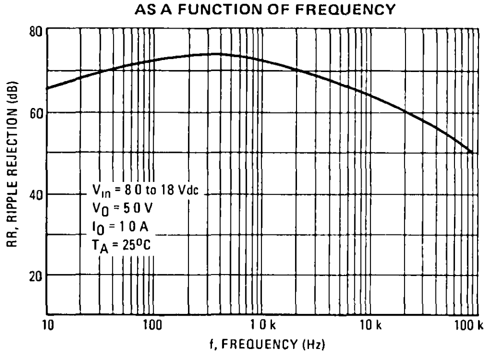
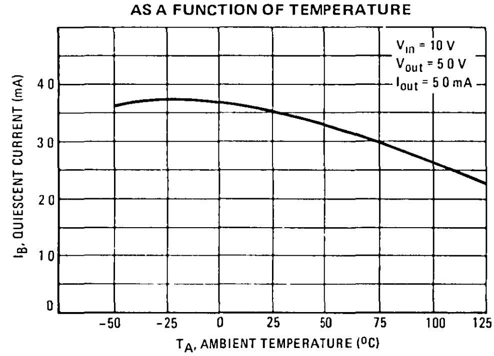


FIGURE 6 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



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MC1403,A
MC1503,A

LOW-VOLTAGE REFERENCE

A precision band-gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with Motorola MC1506, MC1508, and MC3510 D/A converters, and MC14433 A/D systems. Low temperature drift is a prime design consideration.

- Output Voltage = 2.5 V ±25 mV
- Input Voltage Range = 4.5 V to 40 V
- Quiescent Current = 1.2 mA typ
- Output Current = 10 mA
- Temperature Coefficient = 10 ppm/°C typ
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8-Pin DIP Package

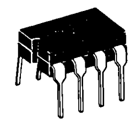
Typical Applications

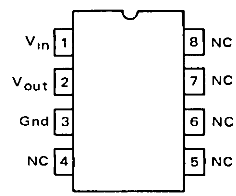
- Voltage Reference for 8-12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference

PRECISION LOW-VOLTAGE REFERENCE

LASER TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT

U SUFFIX
CERAMIC PACKAGE
CASE 693





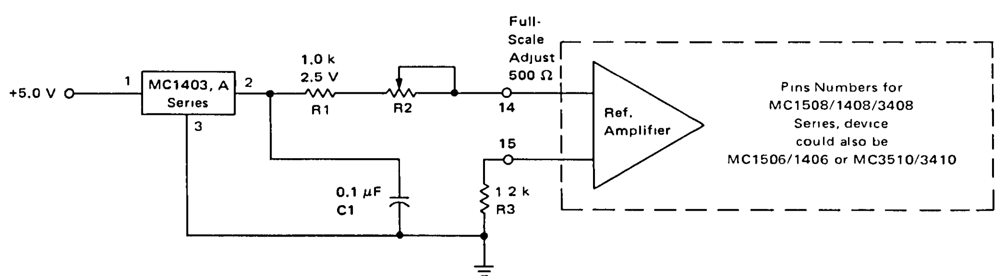
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	−65 to 150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temeprature Range	T_A		
MC1503,A		−55 to +125	°C
MC1403,A		0 to +70	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC1503U	−55 to +125°C	Ceramic DIP
MC1503AU	−55 to +125°C	Ceramic DIP
MC1403U	0 to +70°C	Ceramic DIP
MC1403AU	0 to +70°C	Ceramic DIP

FIGURE 1 — A REFERENCE FOR MOTOROLA MONOLITHIC D/A CONVERTERS



PROVIDING THE REFERENCE CURRENT FOR MOTOROLA MONOLITHIC D/A CONVERTERS

The MC1403/1503 makes an ideal reference for the Motorola monolithic D/A converters The MC1406/1506, MC1408/1508, MC3410/3510 and MC3408 D/A converters all require a stable current reference of nominally 2.0 mA This can be easily obtained from the MC1403/1503 with the addition of a series resistor, R1. A variable resistor, R2, is recommended to provide means for full-scale adjust on the D/A converter.

The resistor R3 improves temperature performance by matching the impedance on both inputs of the D/A reference amplifier The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.

A single MC1403/1503 reference can provide the required current input for up to five of the monolithic D/A converters.

ELECTRICAL CHARACTERISTICS (V_I = 15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_O	2.475	2.50	2.525	V
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
MC1503		–	–	55	
MC1503A		–	–	25	
MC1403		–	10	40	
MC1403A		–	10	25	
Output Voltage Change (over specified temperature range)	ΔV_O				mV
MC1503 } -55°C to +125°C		–	–	25	
MC1503A } -55°C to +125°C		–	–	11	
MC1403 } 0°C to +70°C		–	–	7.0	
MC1403A } 0°C to +70°C		–	–	4.4	
Line Regulation	Reg_{in}				mV
(15 V ≤ V_I ≤ 40 V)		–	1.2	4.5	
(4.5 V ≤ V_I ≤ 15 V)		–	0 6	3.0	
Load Regulation (0 mA < I_O < 10 mA)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0 mA)	I_I	–	1 2	1.5	mA

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FIGURE 2 – MC1403/1503 SCHEMATIC

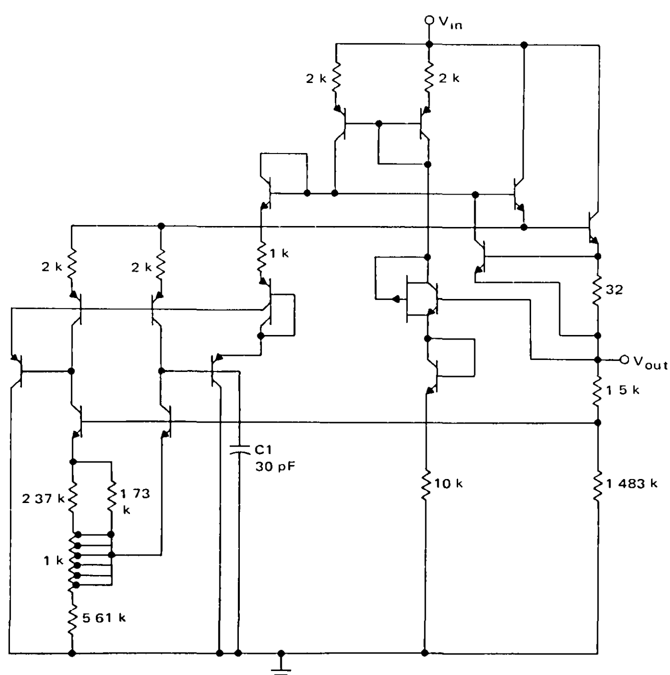

FIGURE 3 – TYPICAL CHANGE IN V_{out} versus V_{in} (NORMALIZED TO V_{in} = 15 V @ T_C = 25°C)

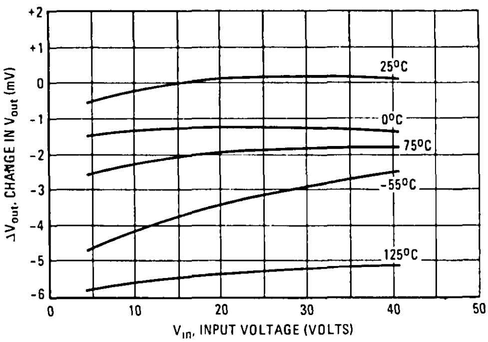

FIGURE 4 – CHANGE IN OUTPUT VOLTAGE versus LOAD CURRENT (NORMALIZED TO V_{out} @ V_{in} = 15 V, I_{out} = 0 mA)

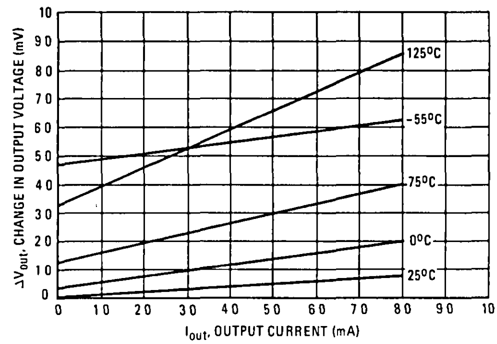

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FIGURE 5 – QUIESCENT CURRENT versus TEMPERATURE (V_{in} = 15 V, I_{out} = 0 mA)

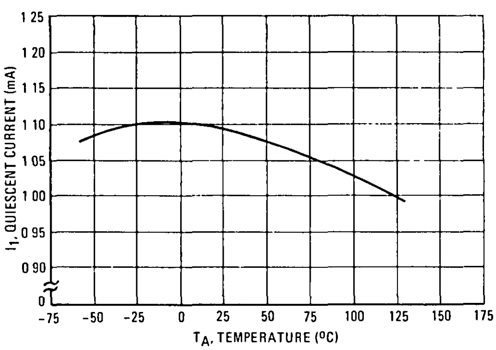


FIGURE 6 – CHANGE IN V_{out} versus TEMPERATURE (NORMALIZED TO V_{out} @ V_{in} = 15 V)

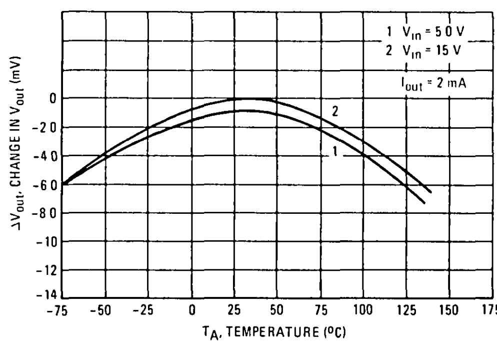
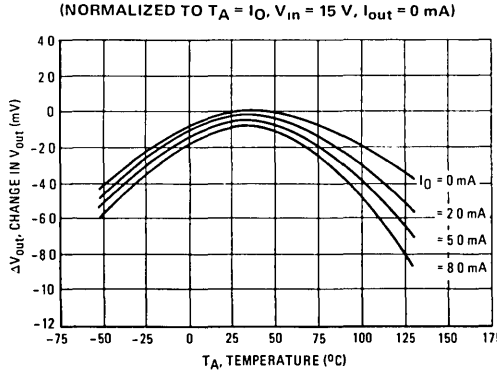


FIGURE 7 – CHANGE IN V_{out} versus TEMPERATURE (NORMALIZED TO T_A = I_O, V_{in} = 15 V, I_{out} = 0 mA)



3-1/2-DIGIT VOLTMETER – COMMON ANODE DISPLAYS, FLASHING OVERRANGE

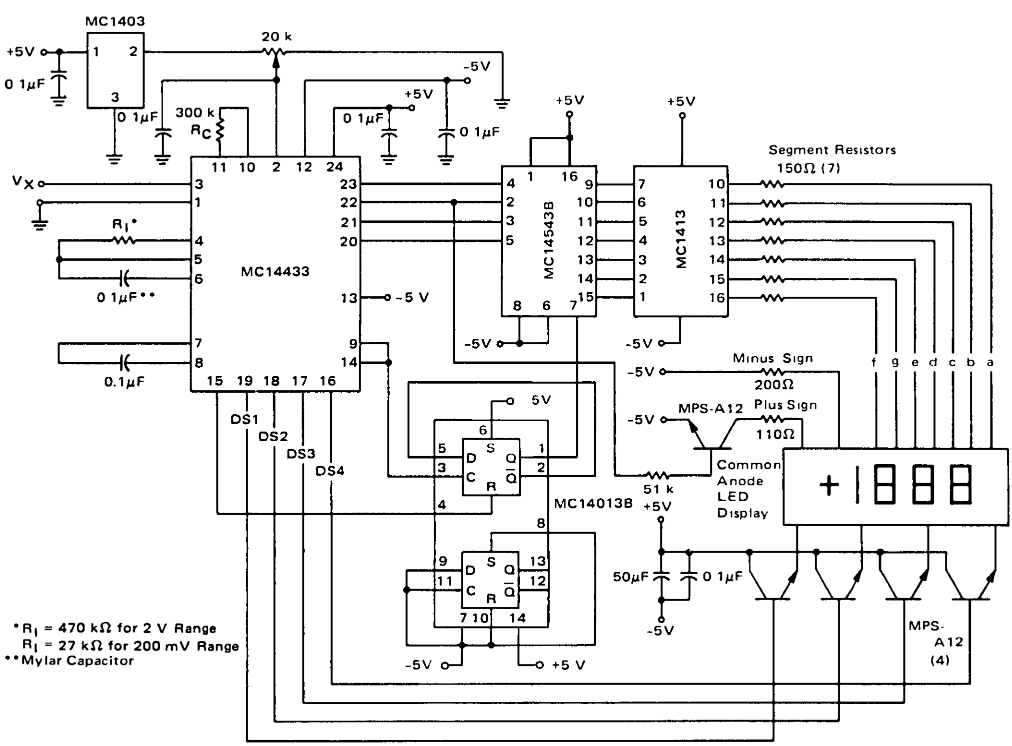
An example of a 3-1/2-digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with 1/2 MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter-follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in Figure 8.

FIGURE 8 – 3-1/2-DIGIT VOLTMETER



MC1404 MC1404A
MC1504 MC1504A

Advance Information

LOW-VOLTAGE REFERENCE FAMILY

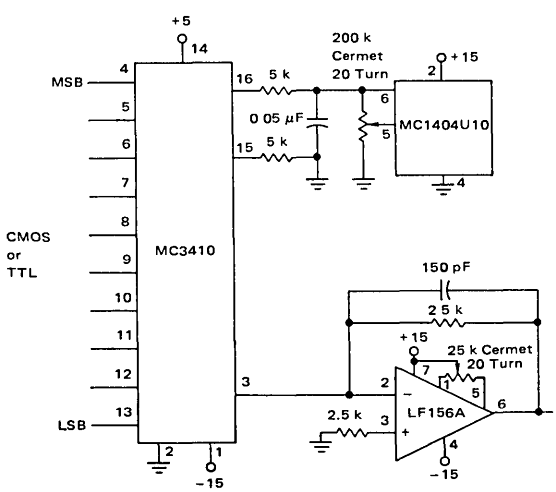
The MC1404 series of ICs is a family of temperature-compensated voltage references for precision data conversion applications, such as A/D, D/A, V/F, and F/V. Advances in laser-trimming and ion-implanted devices, as well as monolithic fabrication techniques, make these devices stable and accurate to 12 bits over both military and commercial temperature ranges. In addition to excellent temperature stability, these parts offer excellent long-term stability and low noise.

- Output Voltages: Standard, 5.0 V, 6.25 V, 10 V
- Trimmable Output: > ± 6%
- Wide Input Voltage Range: V_{REF} + 2.5 V to 40 V
- Low Quiescent Current: 1.25 mA Typical
- Temperature Coefficient: 10 ppm/°C Typical
- Low Output Noise: 12 μV p-p Typical
- Excellent Ripple Rejection: > 80 dB Typical

TYPICAL APPLICATIONS

- Voltage Reference for 8 – 12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- MPU D/A and A/D Applications

FIGURE 1 – VOLTAGE OUTPUT 10 BIT DAC USING MC1404U10

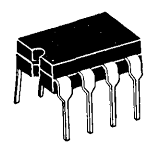


This is advance information and specifications are subject to change without notice.

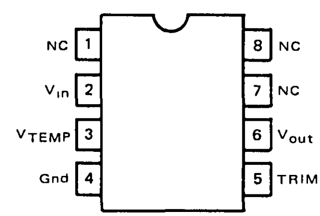
PRECISION LOW-DRIFT VOLTAGE REFERENCES

5.0, 6.25, and 10-VOLT OUTPUT VOLTAGES

LASER TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT



U SUFFIX
CERAMIC PACKAGE
CASE 693



ORDERING INFORMATION

PACKAGE (ALL TYPES)
Ceramic DIP

Device	Temperature Range
5.0 Volts	
MC1504U5	−55°C to +125°C
MC1504AU5	−55°C to +125°C
MC1404U5	0°C to +70°C
MC1404AU5	0°C to +70°C
6.25 Volts	
MC1504U6	−55°C to +125°C
MC1504AU6	−55°C to +125°C
MC1404U6	0°C to +70°C
MC1404AU6	0°C to +70°C
10 Volts	
MC1504U10	−55°C to +125°C
MC1504AU10	−55°C to +125°C
MC1404U10	0°C to +70°C
MC1404AU10	0°C to +70°C

ELECTRICAL CHARACTERISTICS (V_{in} = 15 Volts, T_A = 25°C and Trim Terminal not connected unless otherwise noted)

Characteristic	Symbol	MC1404,A Min	MC1404,A Typ	MC1404,A Max	MC1504,A Min	MC1504,A Typ	MC1504,A Max	Unit
Output Voltage (I_O = 0 mA)	V_O							Volt
U5, AU5		4.95	5.00	5.05	4.95	5.00	5.05	
U6, AU6		6.19	6.25	6.31	6.19	6.25	6.31	
U10, AU10		9.90	10	10.10	9.90	10	10.10	
Output Voltage Tolerance	–	–	±0.1	±1.0	–	±0.1	±1.0	%
Output Trim Range (Figure 10) (R_P = 100 kΩ)	ΔV_{TRIM}	±6.0	–	–	±6.0	–	–	%
Output Voltage Temperature Coefficient, Over Full Temperature Range	$\Delta V_O/\Delta T$							ppm/°C
MC1404, MC1504		–	10	40	–	–	55	
MC1404A, MC1504A		–	10	25	–	–	25	
Maximum Output Voltage Change Over Temperature Range	ΔV_O							mV
MC1404U5, MC1504U5		–	–	14	–	–	50	
MC1404AU5, MC1504AU5		–	–	9.0	–	–	23	
MC1404U6, MC1504U6		–	–	17.5	–	–	62	
MC1404AU6, MC1504AU6		–	–	11	–	–	28	
MC1404U10, MC1504U10		–	–	28	–	–	99	
MC1404AU10, MC1504AU10		–	–	18	–	–	45	
Line Regulation (1) (V_{in} = V_{out} + 2.5 V to 40 V, I_{out} = 0 mA)	Reg_{LINE}	–	2.0	6.0	–	2.0	6.0	mV
Load Regulation (1) (0 ≤ I_O ≤ 10 mA)	Reg_{LOAD}	–	–	10	–	–	10	mV
Quiescent Current (I_O = 0 mA)	I_I	–	1.2	1.5	–	1.2	1.5	mA
Short Circuit Current	I_{SC}	15	20	30	–	–	30	mA
Long Term Stability	–	–	25	–	–	25	–	ppm/1000 hrs

Note 1: Includes thermal effects

DYNAMIC CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C all voltage ranges unless otherwise noted)

Characteristic	Symbol	MC1404,A Min	MC1404,A Typ	MC1404,A Max	MC1504,A Min	MC1504,A Typ	MC1504,A Max	Unit
Turn-On Settling Time (to ±0.01%)	t_S	–	50	–	–	50	–	µs
Output Noise Voltage – P to P (Bandwidth 0.1 to 10 Hz)	e_n	–	12	–	–	12	–	µV
Small-Signal Output Impedance	r_o							Ω
120 Hz		–	0.15	–	–	0.15	–	
500 Hz		–	0.2	–	–	0.2	–	
Power Supply Rejection Ratio	PSRR	70	80	–	70	80	–	dB

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FIGURE 2 — SIMPLIFIED DEVICE DIAGRAM

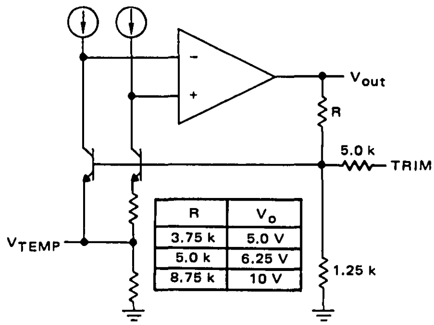


FIGURE 3 — LINE REGULATION versus TEMPERATURE

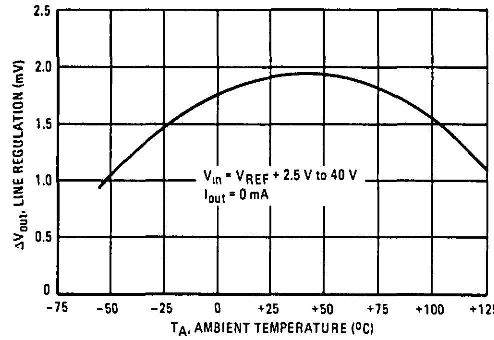


FIGURE 4 — OUTPUT VOLTAGE versus TEMPERATURE MC1404U10

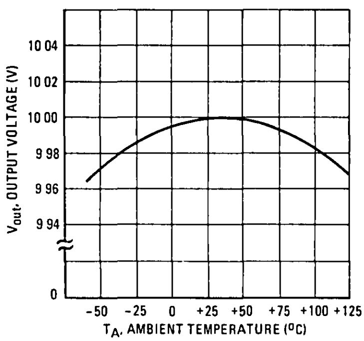


FIGURE 5 — LOAD REGULATION versus TEMPERATURE

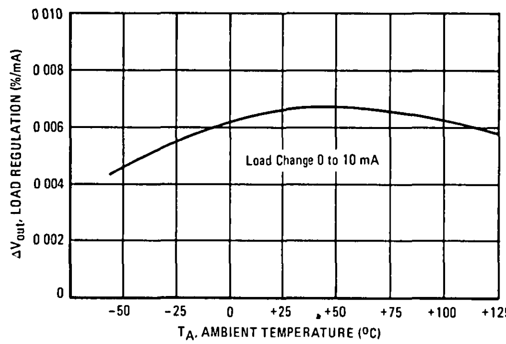


FIGURE 6 — POWER SUPPLY REJECTION RATIO versus FREQUENCY

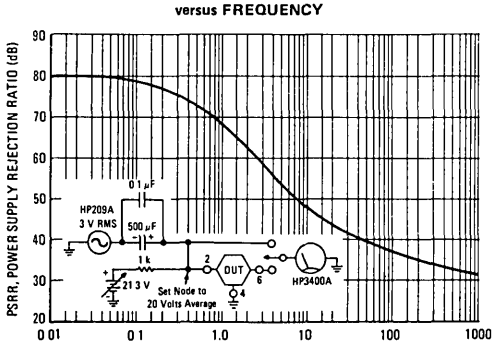


FIGURE 7 — QUIESCENT CURRENT versus TEMPERATURE

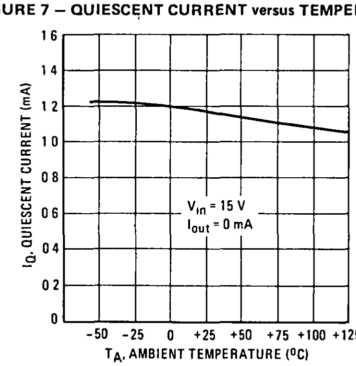


FIGURE 8 – SHORT CIRCUIT CURRENT versus TEMPERATURE

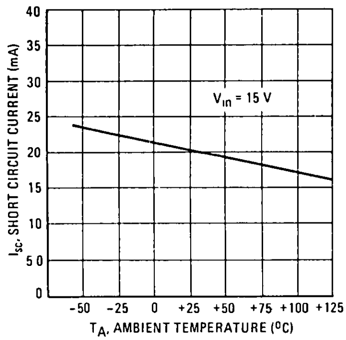


FIGURE 9 – V_{TEMP} OUTPUT versus TEMPERATURE

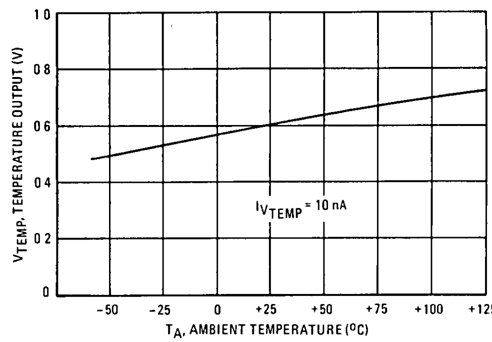
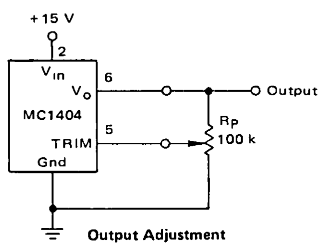


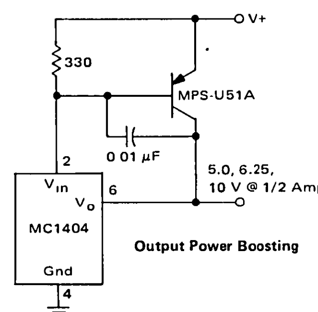
FIGURE 10 – OUTPUT TRIM CONFIGURATION



Output Adjustment

The MC1404 trim terminal can be used to adjust the output voltage over a ±6% range For example, the output can be set to 10.000 V or to 10 240 V for binary applications For trimming, Bourns type 3059, 100 kΩ or 200 kΩ trimpot is recommended

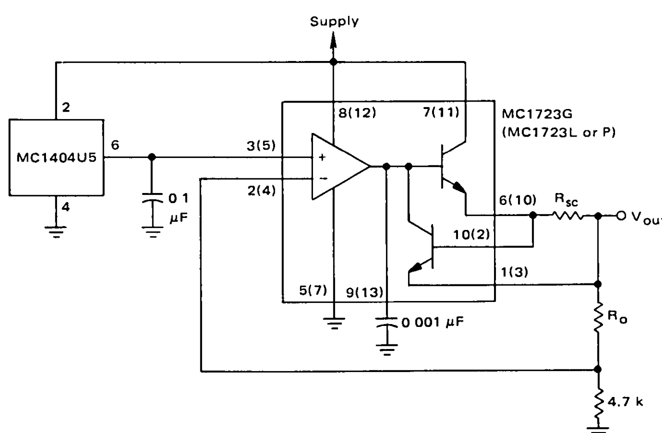
FIGURE 11 – PRECISION SUPPLY USING MC1404



Output Power Boosting

The addition of a power transistor, a resistor, and a capacitor converts the MC1404 into a precision supply with one ampere current capability. At V+ = 15 V, the MC1404 can carry in excess of 14 mA of load current with good regulation. If the power transistor current gain exceeds 75, a one ampere supply can be realized

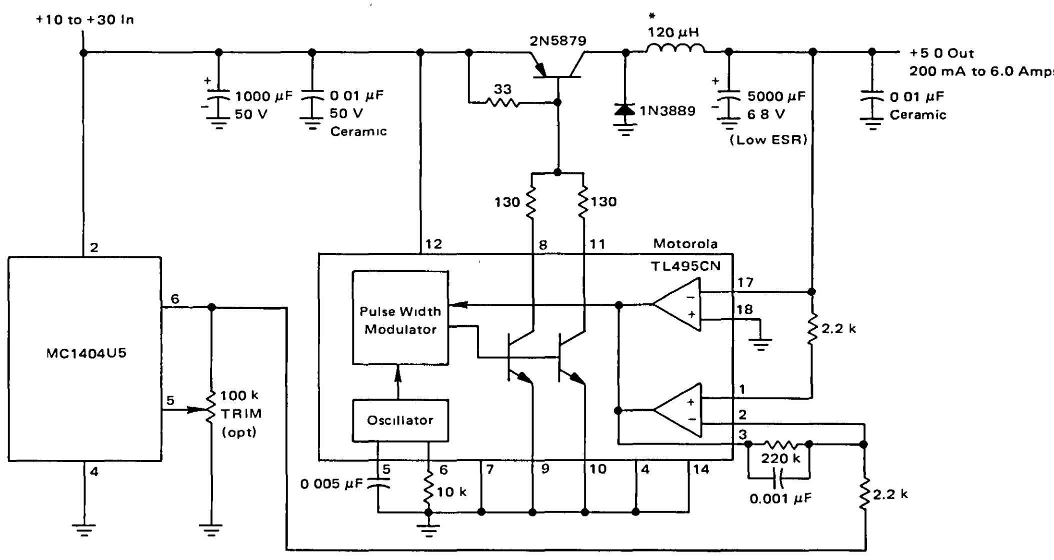
FIGURE 12 – ULTRA STABLE REFERENCE FOR MC1723 VOLTAGE REGULATOR



$$V_{out} = 5\,0\ V\left(\frac{R_o + 4\,7\ k}{4.7\ k}\right)$$

$$I_{omax} \approx \frac{0\,6\ V}{R_{sc}}$$

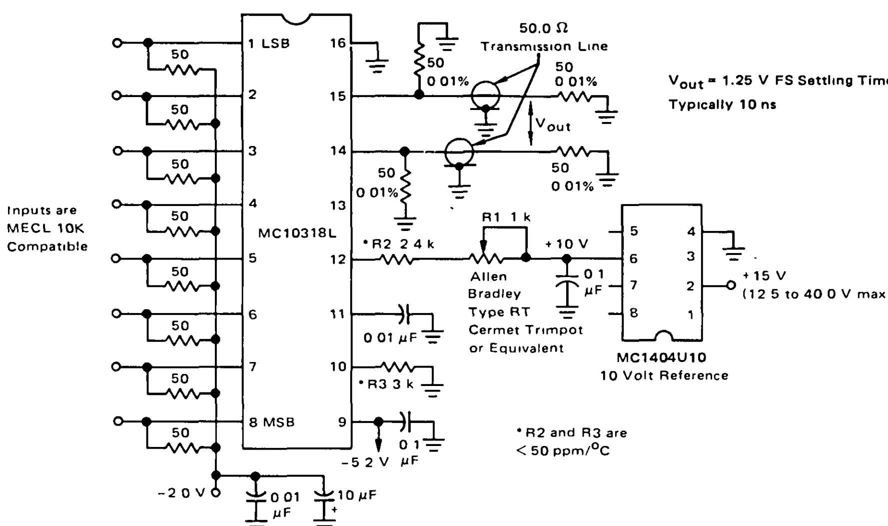
FIGURE 13 — 5.0 V, 6.0 AMP, 25 kHz SWITCHING REGULATOR WITH SEPARATE ULTRA-STABLE REFERENCE



*40 Turns #16 Wire, Arnold A-894075-2 Ferrite Core

FIGURE 14 — HIGH SPEED 8-BIT D/A CONVERTER USING MC1404U10

I_{FS} is set to 51 000 mA with R1



MC1463
MC1563

Specifications and Applications Information

NEGATIVE VOLTAGE REGULATOR

The MC1563/MC1463 is a "three terminal" negative regulator designed to deliver continuous load current up to 500 mAdc and provide a maximum negative input voltage of −40 Vdc. Output current capability can be increased to greater than 10 Adc through use of one or r .e external transistors.

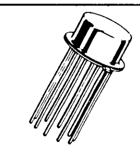
Specifications and performance of the MC1563/MC1463 Negative Voltage Regulator are nearly identical to the MC1569/MC1469 Positive Voltage Regulator. For systems requiring both a positive and negative power supply, these devices are excellent for use as complementary regulators and offer the advantage of operating with a common input ground.

The MC1563R/MC1463R case can be mounted directly to a grounded heat sink which eliminates the need for an insulator

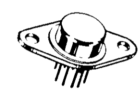
- Case is at Ground Potential (R package)
- Electronic "Shutdown" and Short-Circuit Protection
- Low Output Impedance – 20 Milliohms typical
- High Power Capability – 9.0 Watts
- Excellent Temperature Stability – $\Delta V_O/\Delta T = \pm 0.002\%/^{\circ}C$ typical
- High Ripple Rejection – 0.002% typical
- 500 mA Current Capability

NEGATIVE-POWER-SUPPLY VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 603



R SUFFIX
METAL PACKAGE
CASE 614

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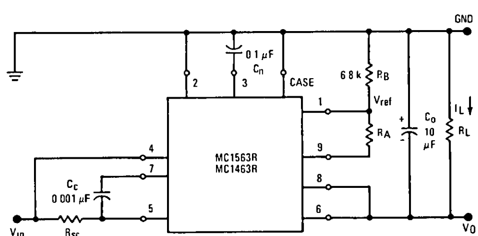
FIGURE 1 – TYPICAL CIRCUIT CONNECTION
$(|-3.5| \leqslant V_O \leqslant |-37|$ Vdc, $1 \leqslant I_L \leqslant 500$ mA)



Select R_A to Give Desired V_O $R_A \approx (2|V_O|-7)$ kΩ $V_O \approx -3.5(1+\frac{R_A}{R_B})$

FIGURE 2 – TYPICAL NPN CURRENT BOOST CONNECTION
(V_O = 5.2 Vdc, I_L = 10 Adc [max])

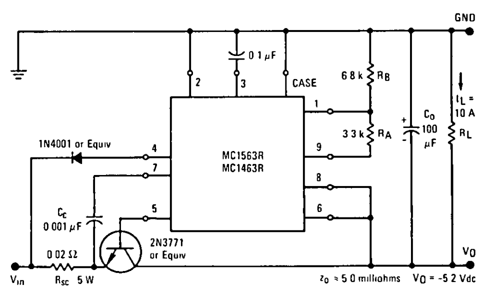
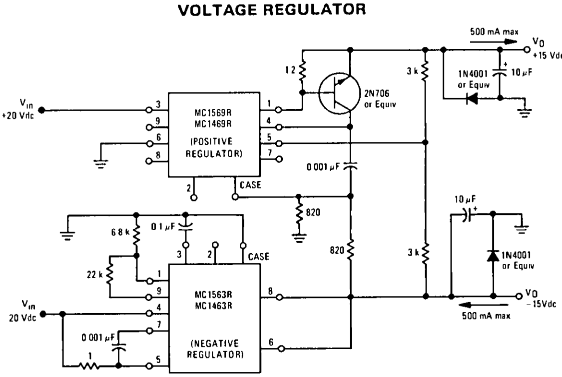


FIGURE 3 – ±15 V, ±400 mA COMPLEMENTARY TRACKING VOLTAGE REGULATOR



ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC1463G	0°C to +70°C	Metal Can
MC1463R	0°C to +70°C	Metal Power
MC1563G	−55°C to +125°C	Metal Can
MC1563R	−55°C to +125°C	Metal Power

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
Input Voltage MC1463 / MC1563	V_I	-35 / -40		Vdc
		G Package	R Package	
Load Current — Peak	I_L	250	600	mA
Current, Pin 2	I_2	10	10	mA
Power Dissipation and Thermal Characteristics				
T_A = 25°C	P_D	0.68	2.4	Watts
Derate above T_A = 25°C	$1/R_{\theta JA}$	5.44	16	mW/°C
Thermal Resistance, Junction to Air	$R_{\theta JA}$	184	62	°C/W
T_C = 25°C	P_D	1.8	9.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14.4	61	mW/°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	69.4	17	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

4

OPERATING TEMPERATURE RANGE

Operating Ambient Temperature Range MC1463 / MC1563	T_A	0 to +70 / -55 to +125	°C

ELECTRICAL CHARACTERISTICS (I_L = 100 mAdc, T_C = +25°C, V_{in} = 15 V, V_O = 10 V unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	MC1563 Min	MC1563 Typ	MC1563 Max	MC1463 Min	MC1463 Typ	MC1463 Max	Unit
Input Voltage ($T_A = T_{low}$ ① to T_{high} ② I_L = 1.0 mA)	4	1,6	V_I	-8.5	–	-40	-9.0	–	-35	Vdc
Output Voltage Range (I_L = 1.0 mA)	4	–	V_O	-3.6	–	-37	-3.8	–	-32	Vdc
Reference Voltage (Pin 1 to Ground)	4	–	V_{ref}	-3.4	-3.5	-3.6	-3.2	-3.5	-3.8	Vdc
Minimum Input-Output Voltage Differential (R_{sc} = 0)	4	2	$\|V_{in} - V_O\|$	–	1.5	2.7	–	1.5	3.0	Vdc
Bias Current (Standby Current) (I_L = 1.0 mAdc, $I_{IB} = I_I - I_L$)	4	–	I_{IB}	–	7.0	11	–	7.0	14	mAdc
Output Noise (C_n = 0.1 μF, f = 10 Hz to 5.0 MHz)	4	–	v_N	–	120	–	–	120	–	μV(rms)
Temperature Coefficient of Output Voltage	4	3	$\Delta V_O/\Delta T$	–	±0.002	–	–	±0.002	–	%/°C
Operating Load Current Range	4	–	I_{LR}							mAdc
(R_{sc} = 0.3 ohm) R Package				1.0	–	500	1.0	–	500	
(R_{sc} = 2.0 ohms) G Package				1.0	–	200	1.0	–	200	
Input Regulation (V_{in} = 1.0 V rms, f = 1.0 kHz)	4	4	Reg_{line}	–	0.002	0.015	–	0.003	0.030	%/V_O
Load Regulation	6	5	Reg_{load}							
(T_J = Constant [1.0 mA ≤ I_L ≤ 20 mA])				–	0.4	1.6	–	0.7	2.4	mV
(T_C = +25°C [1.0 mA ≤ I_L ≤ 50 mA]) R Package				–	0.005	0.05	–	0.005	0.05	%
G Package				–	0.01	0.13	–	0.01	0.13	
Output Impedance (f = 1.0 kHz)	7	-	z_o	–	20	–	–	35	–	milliohms
Shutdown Current (V_I = -35 Vdc)	8	–	I_{sd}	–	7.0	15	–	14	50	μAdc

① T_{low} = 0°C for MC1463
= -55°C for MC1563

② T_{high} = +70°C for MC1463
= +125°C for MC1563

Heat sink required for T_{high} testing of "G" package.

Note 1 "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode

Note 2 This parameter states that the MC1563/MC1463 will regulate properly with the input-output voltage differential $|V_I - V_O|$ as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with $|V_I - V_O|$ as low as 1 5 Vdc as shown in the typical column

Note 3 "Temperature Coefficient of Output Voltage" is defined as:

$$\Delta V_O/\Delta T = \frac{\pm (V_O \max - V_O \min)\ (100)}{\Delta T_A\ (V_O @ T_A = +25^oC)}$$

where ΔT_A = +180°C for the MC1563
+75°C for the MC1463

The output-voltage adjusting resistors (R_A and R_B) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature

Note 4. *Input regulation is the percentage change in output voltage* per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{v_O}{V_O\ (v_I)}\ 100\ \ (\%/V_O).$$

where v_o is the change in the output voltage V_o for the input change v_{in}.

The following example illustrates how to compute maximum output voltage change for the conditions given:

$Reg_{in} = 0.015\%/V_O$
$V_O = 10$ Vdc
$v_{in} = 1.0$ V(rms)

$$v_O = \frac{(Reg_{line})\ (v_I)\ (V_O)}{100} = \frac{(0.015)(1.0)(10)}{100} = 0.0015\ \text{V(rms)}$$

Note 5. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{V_O|_{I_L = 1.0\ mA} - V_O|_{I_L = 50\ mA}}{V_O|_{I_L = 1.0\ mA}} \times 100$$

Note 6. Not to exceed maximum package power dissipation.

4

TEST CIRCUITS

(I_L = 100 mAdc, T_C = +25°C unless otherwise noted.)

FIGURE 4 – GENERAL TEST CIRCUIT

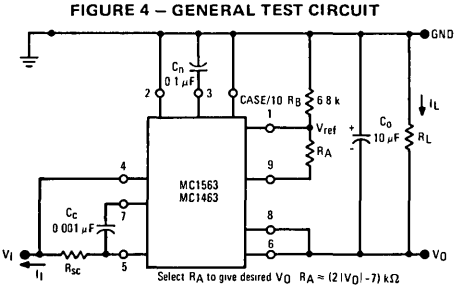


FIGURE 5 – LOAD TRANSIENT RESPONSE

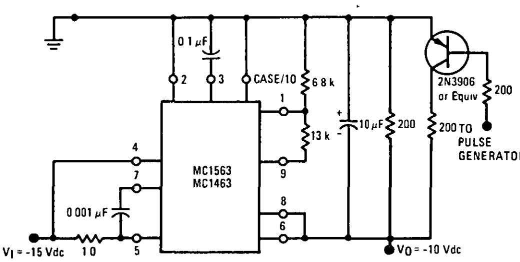


FIGURE 6 – LOAD REGULATION

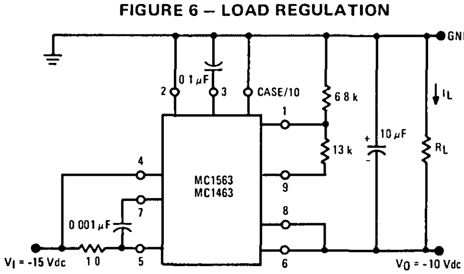


FIGURE 7 – OUTPUT IMPEDANCE

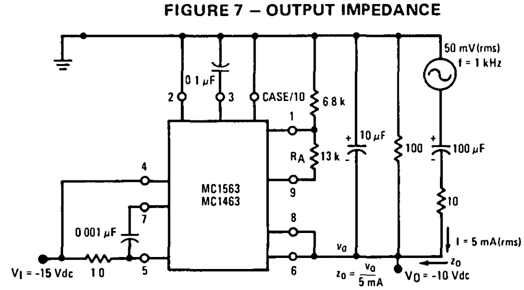
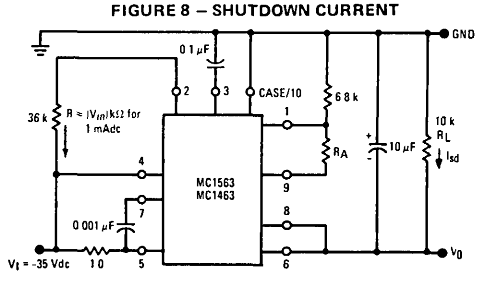


FIGURE 8 – SHUTDOWN CURRENT



GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
   a) Output Voltage is set by resistors R_A and R_B (see Figure 9). Set R_B = 6 8 k ohms and determine R_A from the graph of Figure 11 or from the equation:

   $$R_A \approx (2\,|V_O| - 7)\ k\Omega$$

   b) Output voltage can be varied by making R_A adjustable as shown in Figures 9 and 10.

   c) Output voltage, V_O, is determined by the ratio of R_A and R_B therefore optimum temperature performance can be achieved if R_A and R_B have the same temperature coefficient.

   d) $V_O = V_{ref}\,(1 + \frac{R_A}{R_B})$; therefore the tolerance on output voltage is determined by the tolerance of V_{ref} and R_A and R_B.

2. Short-Circuit Current, I_{SC}
   Short-Circuit Current, I_{SC} is determined by R_{SC}. R_{SC} may be chosen with the aid of Figure 11 when using the typical circuit connection of Figure 9.

3. Compensation, C_C
   A 0.001 μF capacitor (C_C, see Figure 9), will provide adequate compensation in most applications, with or without current boost. Smaller values of C_C will reduce stability and larger values of C_C will degrade pulse response and output impedance versus frequency. The physical location of C_C should be close to the MC1563/MC1463 with short lead lengths.

4. Noise Filter Capacitor, C_n
   A 0.1 μF capacitor, C_n, from Pin 3 to ground will typically reduce the output noise voltage to 120 μV(rms). The value of C_n can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of 0.001 μF is recommended.

5. Output Capacitor, C_O
   The value of C_O should be at least 10 μF in order to provide good stability.

6. Shutdown Control
   One method of turning "OFF" the regulator is to draw 1 mA from Pin 2 (See Figure 8). This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting. As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at Pin 2 will cause automatic shutdown for high junction temperatures. This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard Logic levels of MRTL, MDTL* or MTTL* can also be used to turn the regulator "ON" or "OFF".

7. Remote Sensing
   The connection to Pin 8 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on z_O can be greatly reduced.

FIGURE 9 – TYPICAL CIRCUIT CONNECTION

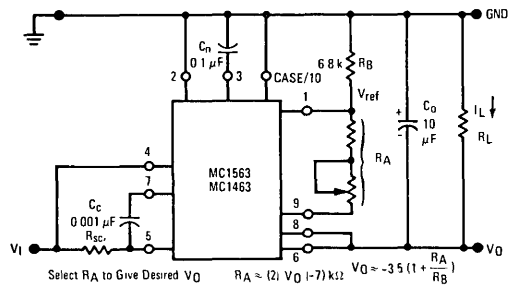


FIGURE 10 – R_A versus V_O

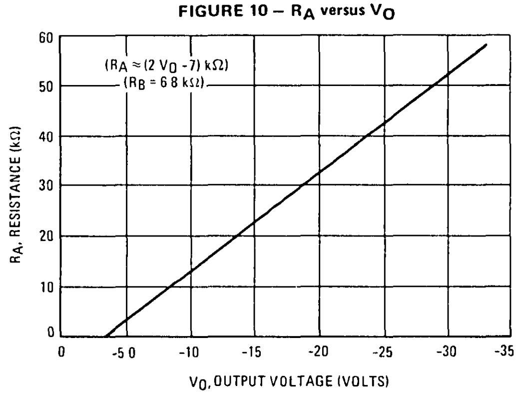
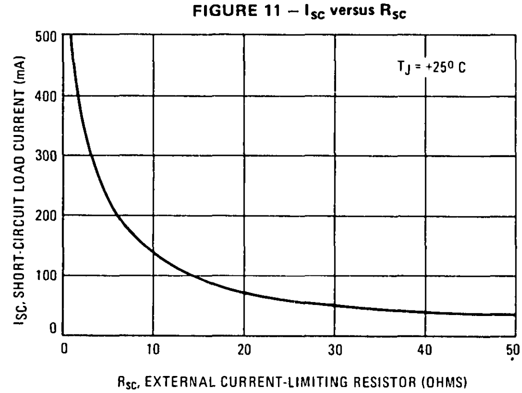


FIGURE 11 – I_{sc} versus R_{sc}



TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_n = 0.1\,\mu F$, $C_c = 0.001\,\mu F$, $C_o = 10\,\mu F$, $T_C = +25^oC$, $V_{I(nom)} = -15$ Vdc, $V_{O(nom)} = -10$ Vdc, $I_L = 100$ mAdc.

FIGURE 12 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

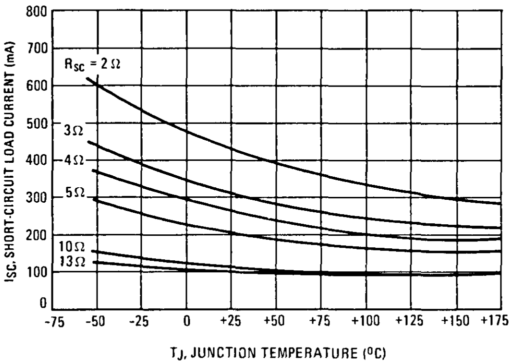


FIGURE 13 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE

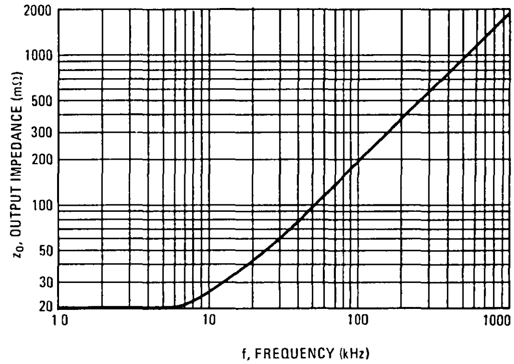


FIGURE 14 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

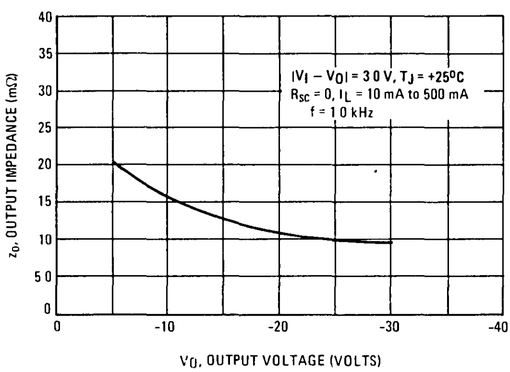


FIGURE 15 – OUTPUT IMPEDANCE versus R_{sc}

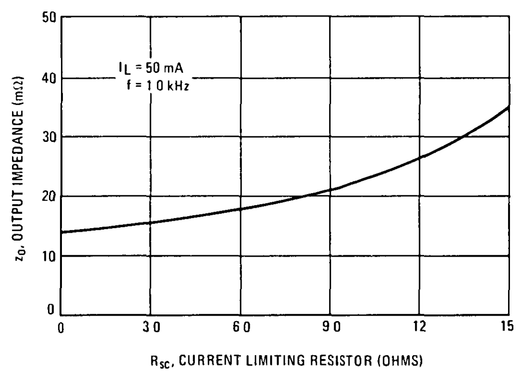
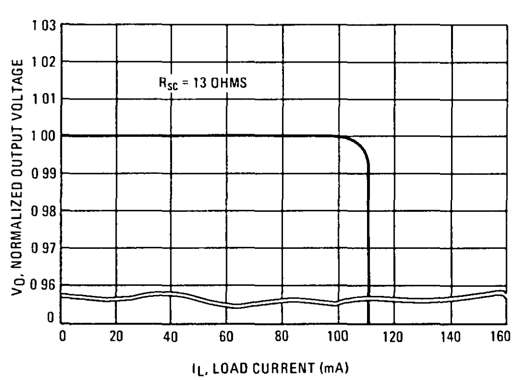


FIGURE 16 – CURRENT LIMITING CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

FIGURE 17 – BIAS CURRENT versus INPUT VOLTAGE

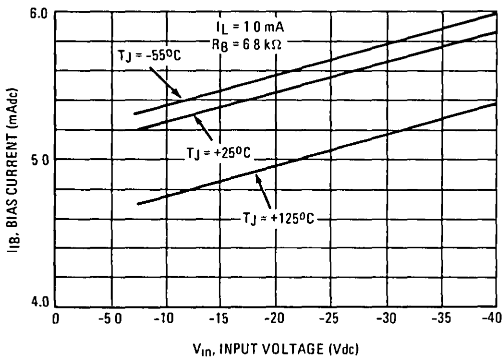


FIGURE 18 – EFFECTS OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

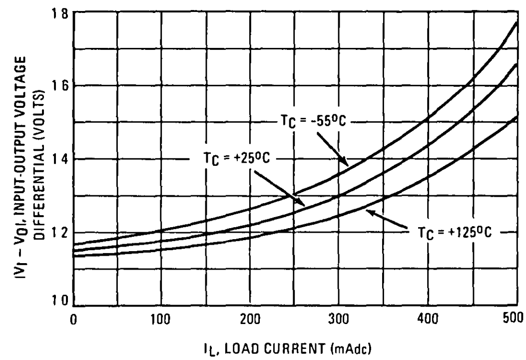


FIGURE 19 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

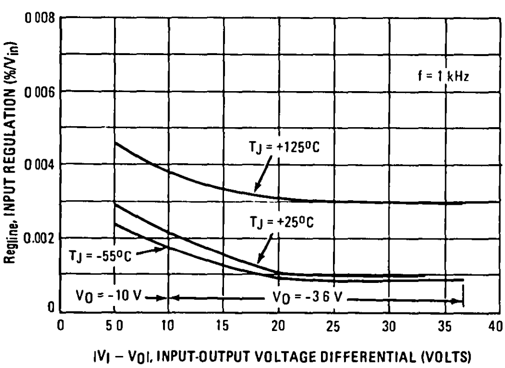


FIGURE 20 – INPUT TRANSIENT RESPONSE

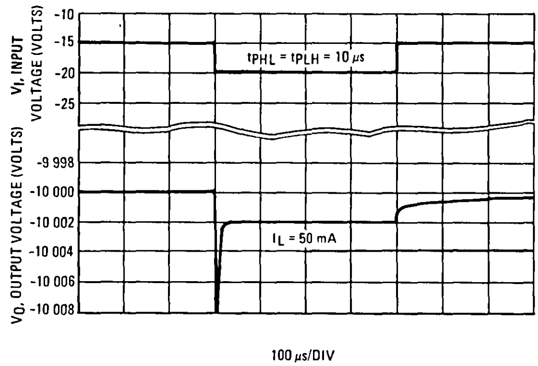


FIGURE 21 – LOAD TRANSIENT RESPONSE

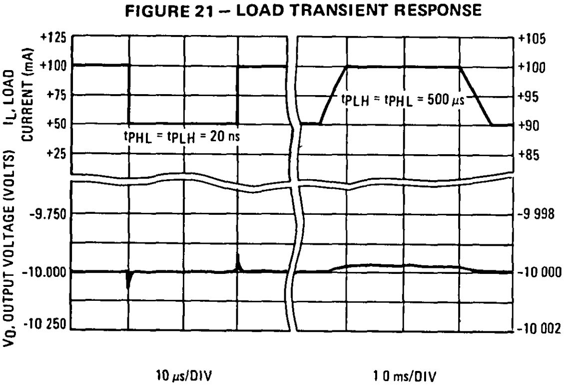
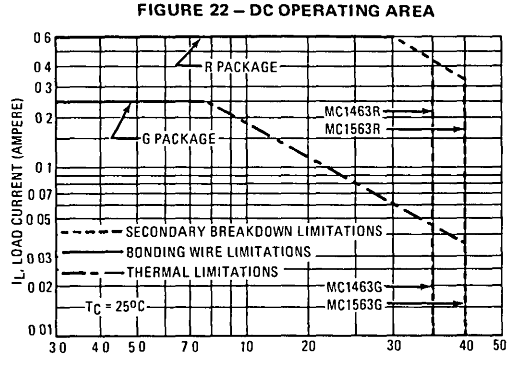


FIGURE 22 – DC OPERATING AREA



OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1563 (MC1463) negative voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE INDEX

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 23, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 24. The gain-determining resistors may be external, enabling a wide range of output voltages. This is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1563) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1563 negative voltage regulator.

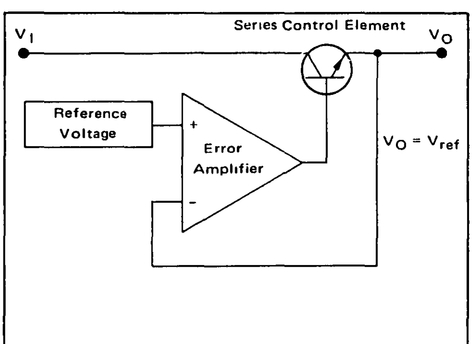


FIGURE 23 – Series Voltage Regulator

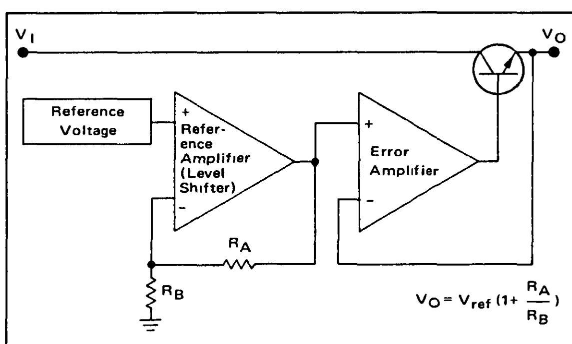
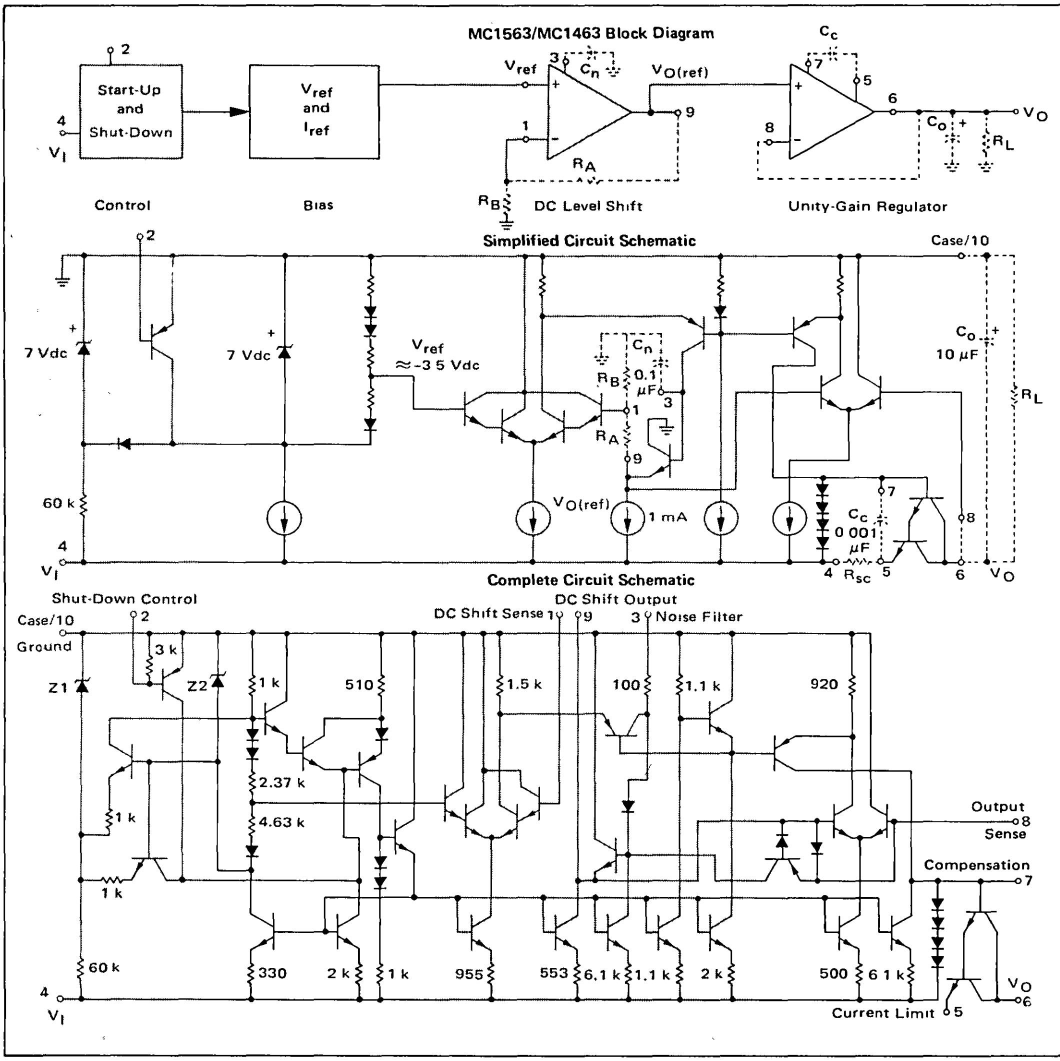


FIGURE 24 – The "Regulator-Within-A-Regulator" Approach

FIGURE 25
(Recommended External Circuitry is Depicted With Dotted Lines.)



MC1563 (MC1463) Operation

Figure 25 shows the MC1563 (MC1463) Negative Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

The shutdown control, in effect, consists of a PNP transistor across the reference zener diode. When this transistor is turned "ON", via Pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to V_{in}/60 kΩ or 500 μA for a -30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately -3.5 Vdc with a typical temperature coefficient of 0.002%/°C. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R_A and R_B) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_n, is introduced externally into the level shift network (via Pin 3) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is 0.1 μF and should have a voltage rating in excess of the desired output voltage. Smaller capacitors (0.001 μF minimum) may be used but will cause a slight increase in output noise. Larger values of C_n will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the shift amplifier is fed internally to the noninverting input of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (Pin 8) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{SC}, is connected in the emitter of this transistor to sample the full load current. This connection enables a four-diode string to limit the drive current to the power transistors in a conventional manner.

Stability and Compensation

As has been seen, the MC1563 employs two amplifiers, each using negative feedback. This implies the possibility of frequency instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (Pin 7) and Pin 5. The recommended value of 0.001 μF will insure stability and still provide acceptable transient response (see Figure 21). It is also necessary to use an output capacitor, C_O, (typically 10 μF) directly from the output (Pin 6) to ground. When an external transistor is used to boost the current, C_O = 100 μF is recommended (see Figure 26).

4

NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 2 or 26, are recommended. The circuit shown in Figure 26 can supply up to approximately 4.0 amperes (subject to safe area limitations). At higher currents the V_{BE} of the pass transistor may itself exceed the threshold of the current limit even for R_{SC} = 0. Figure 2 illustrates the use of an additional external diode from Pin 4 for higher current operation or for pass transistors exhibiting higher V_{BE}'s. It will probably be necessary to determine R_{SC} experimentally for each case where a pass transistor is used because V_{BE} varies from device to device. The circuit of Figure 26 when set up for a -10 V output

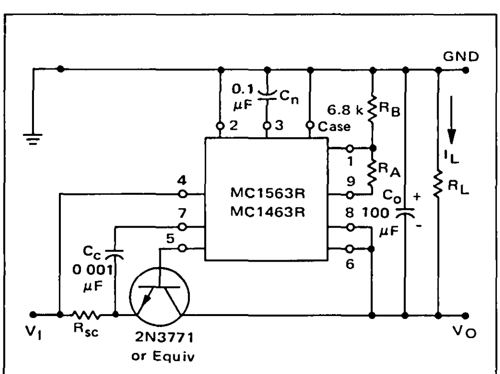


FIGURE 26 – Typical NPN Current Boost Connection

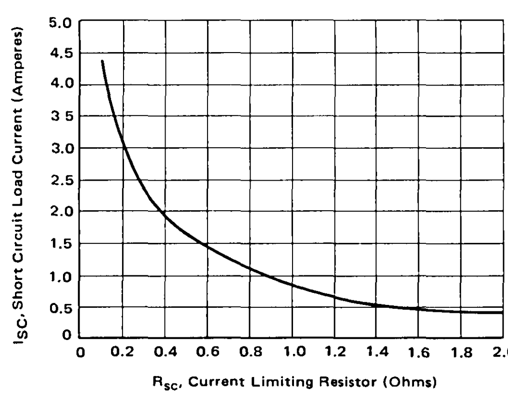


FIGURE 27 – I_{SC} versus R_{SC} (reference Figure 26)

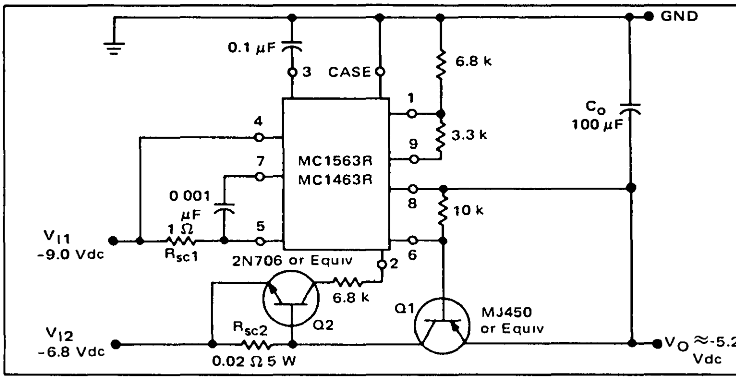


FIGURE 28 – PNP Current Boost Connection

(R_A = 13 kΩ) supply and operating with a - 15 V input, with a R_{SC} of 0.1 Ω, will yield a change in output voltage of only 26 mV over a load current range of from 1 mA to 3.5 A. This corresponds to a dc output impedance of only 7.5 milliohms or a percentage load regulation of 0.26% for a full 3.5-ampere load current change. Figure 27 indicates how the short circuit current varies with the value of R_{SC} for this circuit.

4

PNP CURRENT BOOSTING

A PNP power transistor can also be used to boost the load current capabilities. To improve the efficiency of the PNP boost configuration, particularly for small output voltages, the circuit of Figure 28, is recommended. An auxiliary -9 volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 10-ampere regulator of Figure 28 this represents a savings of 22 watts when compared with operating the regulator from the single -9 V supply. It can supply current to 10 amperes while requiring an input voltage to the collector of the pass transistor of -6.8 volts minimum. The pass transistor is limited to 10 amperes by the added short-circuit current network in its emitter (R_{SC2}) and the IC regulator is limited to 500 mA in the conventional manner (R_{SC1}). The MJ450 exhibits a minimum h_{FE} of 20 at 10 amperes, thus requiring only 500 mA from the MC1563R. Regulation of this circuit is comparable to that of the NPN boost configuration.

For higher output voltages the additional unregulated power supply is not required. The collector of the PNP boost transistor can tie directly to Pin 5 and the internal current limit circuit will provide short-circuit protection using R_{SC} (see Figure 11). Transistor Q2 and R_{SC2} will not be required and Pin 2 should be returned to ground.

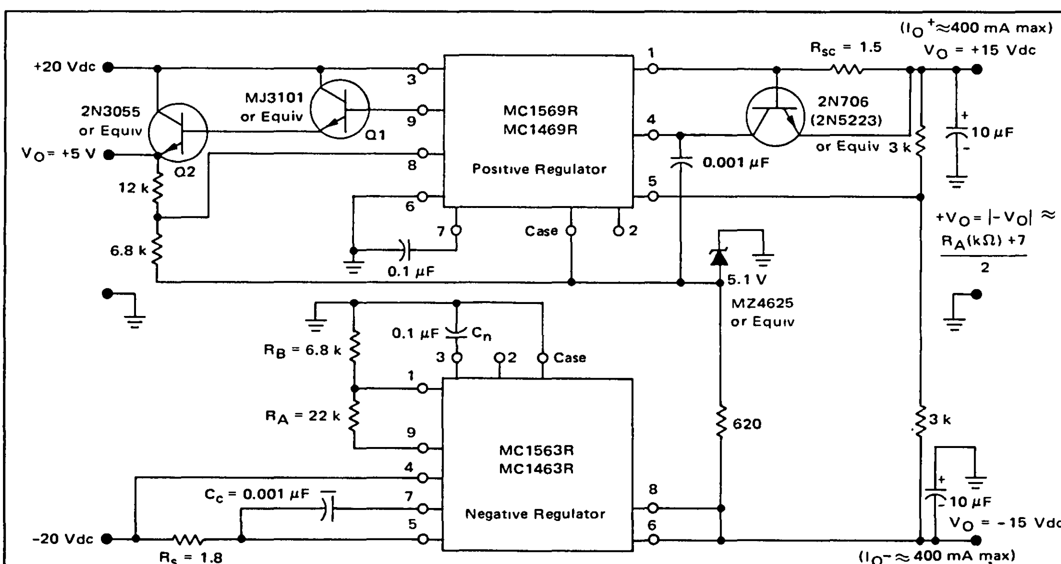
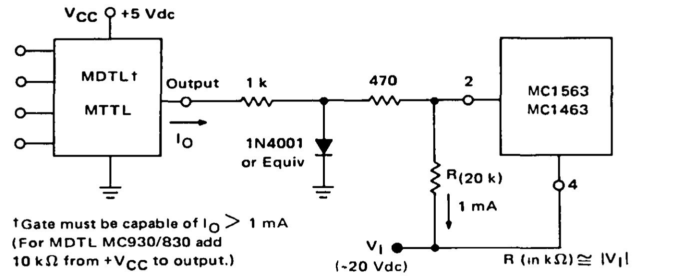


FIGURE 29 – A ±15 Vdc Complementary Tracking Regulator With Auxiliary +5.0 V Supply

FIGURE 30 – Saturated Logic Level Shutdown Circuit



POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1563 is driven from a floating source it is possible to use it as a positive regulator by grounding the negative output terminal. The MC1563 may also be used with the MC1569 to provide completely independent positive and negative power regulators with comparable performance. When used in this manner a silicon diode such as the 1N4001 must be connected as a clamp on the output with the cathode to ground and the anode to the negative output voltage. This is to prevent the positive voltage in the system from forcing the output to a positive value and preventing the MC1563 from starting up.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 3 and 29 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (Pin 6 of the MC1569) and using the other side (Pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3 k-ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at Pin 5 will be zero. When the voltage at pin 5 equals zero, $+|V_O|$ must equal $-|V_O|$.

For the configuration shown in Figure 29, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown, is not short-circuit protected.) The -15-volt supply varies less than 0.1 mV over a zero to -300 mAdc current range and the +15-volt supply tracks this variation. The +15-volt supply varies 20 mV over the zero to +300-mAdc load current range. The +5-volt supply varies less than 5 mV for $0 \leqslant I_L \leqslant 200$ mA with the other two voltages remaining unchanged. See MC1561 data sheet or MC1569 data sheet for information concerning latch-up when using plus and minus regulations.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1563 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of a PNP transistor, which, if turned "ON", will deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60 k-ohm start resistor (V_{in}/60 kΩ). This feature provides additional versatility in the applications of the MC1563. Various sub-systems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as over-heating, over-voltage, shorted output, etc.

As an illustration of the first case, consider a system consisting of both positive-supply logic (MTTL) and negative-supply logic (MECL). The MECL logic may be used in a high-speed arithmetic processor whose services are not continuously required. Substantial power may

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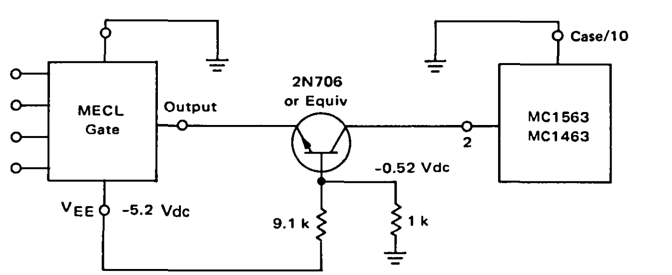
FIGURE 31 – MECL Logic Level Shutdown Circuit



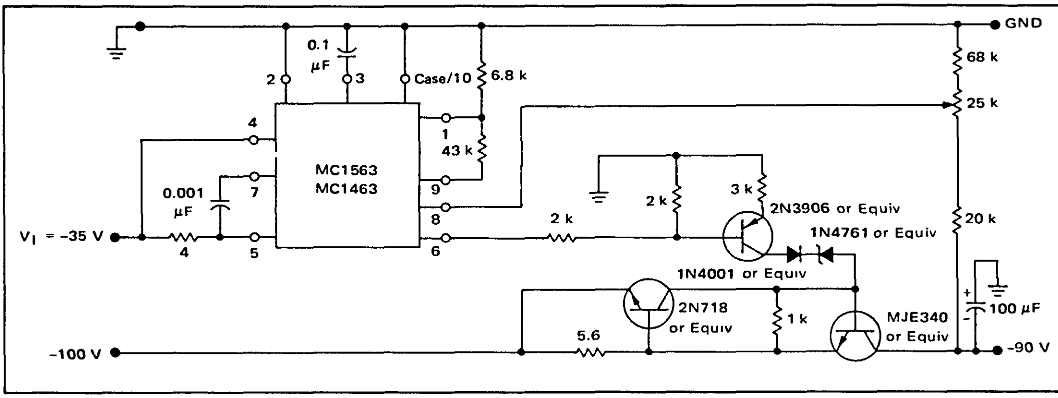


FIGURE 32 – Voltage Boosting Circuit

thus be conserved if the MECL circuitry remains unpowered except when needed. The negative regulator can be shutdown using any of the standard logic swings. For saturated logic control, Figure 30 shows a circuit that allows the normal positive output swing to cause the regulator to shutdown when the logic output is in the low voltage state. The negative output levels of a MECL gate can also be used for shutdown control as shown in Figure 31.

VOLTAGE BOOSTING

Some applications may require a high output voltage which may exceed the voltage rating of the MC1563. This must be solved by assuring that the IC regulator is operated within its limits. Three points in the regulator need to be considered:

1. The input voltage (Pin 4),
2. the output voltage (Pin 6) and,
3. the output sense lead (Pin 8).

A reduced input voltage can be provided by using a separate supply. The output voltage may be zener-level shifted, and the sense line can tie to a portion of the output voltage through a resistive divider. The voltage boost circuit of Figure 32 uses this approach to provide a -90 volt supply. This circuit will exhibit regulation of 0.001% over a 100 mA load current range.

REMOTE SENSING

The MC1563 offers a remote sensing capability. This is important when the load is remote from the regulator, as the resistances of the interconnecting lines (V_{EE} and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 33 shows how remote sensing is accomplished using both a separate sense line from Pin 8 and a separate ground line from the regulator to the remote load.

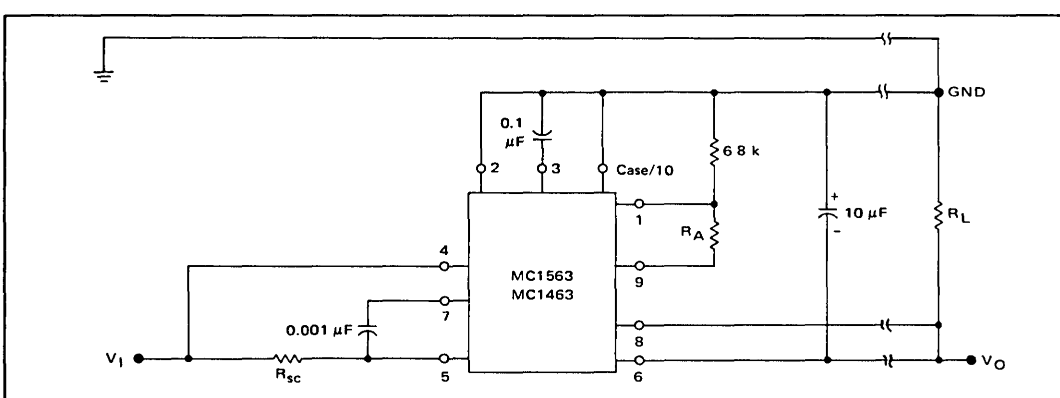


FIGURE 33 – Remote Sensing Circuit

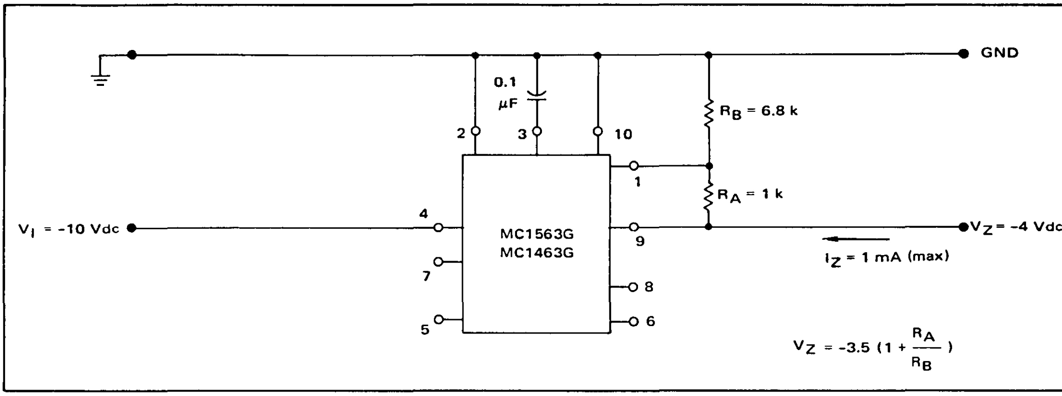


FIGURE 34 – An Adjustable "Zero-TC" Voltage Source

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AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE

The MC1563, when used in conjunction with low-TC resistors, makes an excellent reference-voltage generator. If the -3.5 volt reference voltage of the IC regulator is a satisfactory value, then Pins 1 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0 002%/°C. By adding two resistors, R_A and R_B, any voltage between -3.5 Vdc and -37 Vdc can be obtained with the same low TC (see Figure 34)

THERMAL SHUTDOWN

By setting a fixed voltage at Pin 2, the MC1563 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor (-1.9 x 10^{-3}V/°C). By setting -0.61 Vdc externally, at Pin 2, the regulator will shutdown when the chip temperature reaches approximately 140°C. Figure 35 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

In the case where an external pass transistor is employed; its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 36. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application,

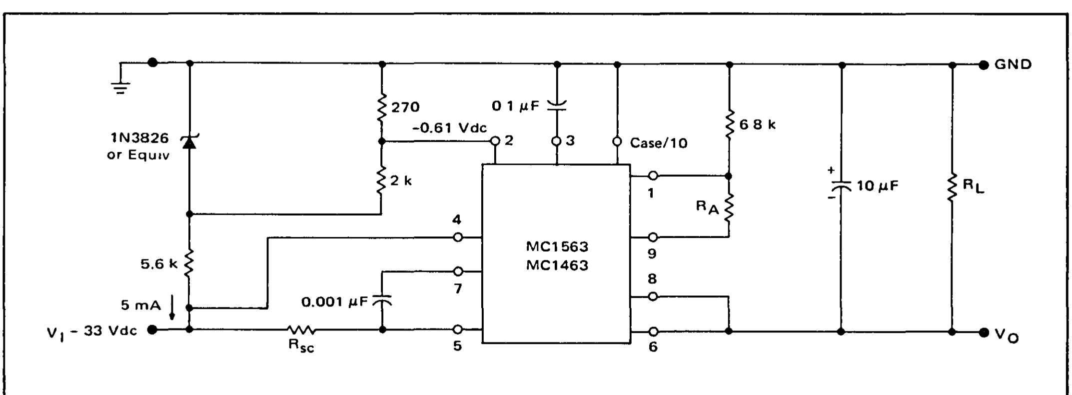

FIGURE 35 – Junction Temperature Limiting Shutdown Circuit

the designer must use caution not to exceed the specified maximum junction temperature (+175°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current (500 mA). Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 22).

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically +0.03%/watt for the MC1563R. For an example of the relative magnitudes of these effects, consider the following conditions:

Given: MC1563R

with $V_I = -10$ Vdc

$V_O = -5$ Vdc

and $I_L = 100$ mA to 200 mA

($\Delta I_L = 100$ mA)

assume $T_A = +25°C$

TO-66 Type Case with heatsink

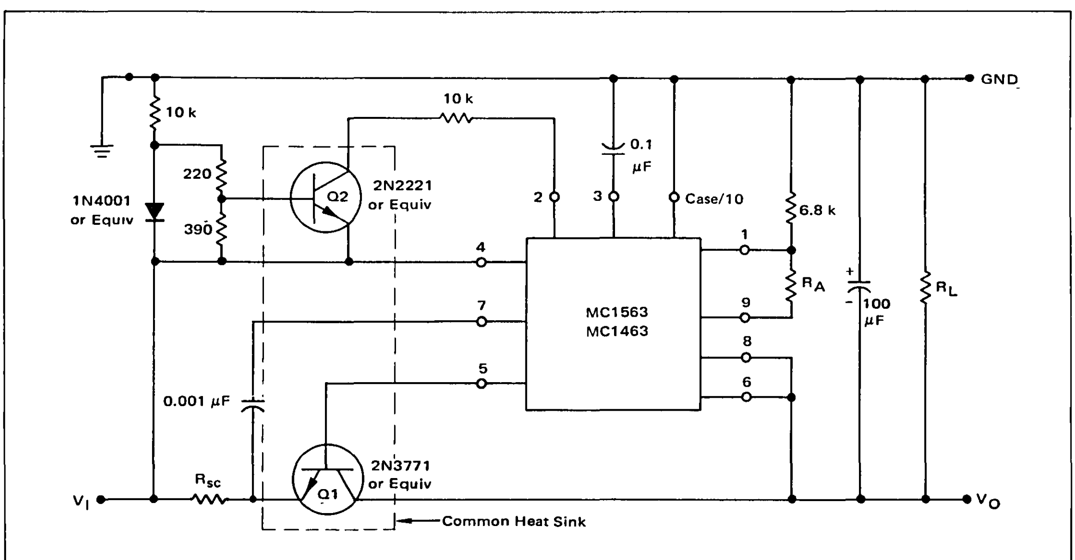

FIGURE 36 – Thermal Shutdown When Using External Pass Transistors

assume $R_{\theta CS} = 0.2^oC/W$

and $R_{\theta SA} = 2^oC/W$

It is desired to find the ΔV_O which results from this ΔI_L. Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_O due to ΔT_J

$$\Delta V_O = (V_O)(\Delta P_D)(\Delta V_O/\Delta T)(R_{\theta JC}+R_{\theta CS}+R_{\theta SA})$$

OR

$$\Delta V_O = (5\ V)(5\,V \times 0.1\ A)(\pm 0.002\%/^oC)(19.2^oC/W)$$

$$\Delta V_O \approx \pm 1.0\ mW$$

2. ΔV_O due to z_o

$$|\Delta V_O| = (-z_o)(I_L)$$

$$|\Delta V_O| = -(2 \times 10^{-2})(10^{-1}) = -2\ mV$$

3. ΔV_O due to gradient coefficient, $\Delta V_O/\Delta G$

$$|\Delta V_O| = (\Delta V_O/\Delta G)(V_O)(\Delta P_D)$$

$$|\Delta V_O| = (+3 \times 10^{-4}/W)(5\ volts)(5 \times 10^{-1}W)$$

$$|\Delta V_O| = +0.8\ mV$$

Therefore the total ΔV_O is given by

$$|\Delta V_O\ total| = \pm\ 1.0 - 2.0 + 0.8\ mV$$

OR

$$-2.2\ mV \leqslant |V_O\ total| \leqslant -0.2\ mV$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

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Typical Printed Circuit Board Layout

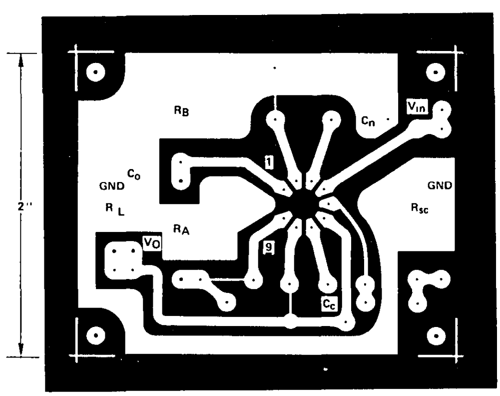
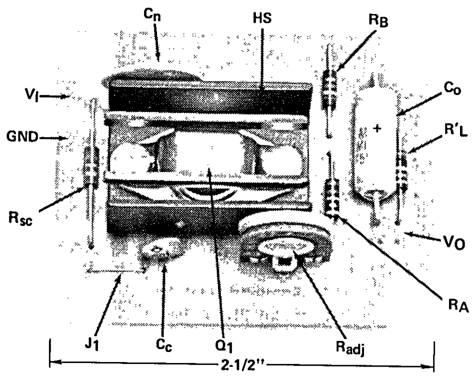


FIGURE 37 – Location of Components



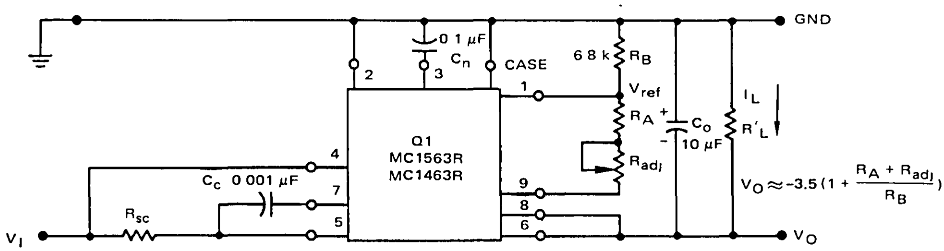
Note 1:
When R_{adj} is used it is necessary to remove the copper which shorts out R_{adj}.

Note 2:
Extra holes are available in the circuit board to permit two resistors to be paralleled to obtain the desired value of R_{sc}.

Note 3:
If Pin 2 is used to shut down the regulator, remove the copper which shorts Pin 2 to ground.

Note 4:
Remote sensing can be achieved by removing the copper which shorts Pin 8 to Pin 6 and connecting Pin 8 directly to the "minus" load terminal. The circuit board ground should be connected to the unregulated power supply ground at the "plus" load terminal

Typical Circuit Connection for Output Voltages Between -3.5 and -37 Volts



Select $R_A + R_{adj}$ to Give Desired V_O $R_A + R_{adj} \approx (2|V_O| - 7)$ kΩ with $R_B = 6.8$ kΩ

PARTS LIST

Component	Value	Description
R_A	Select	1/4 or 1/2 watt carbon
R_B	6.8 k	1/4 or 1/2 watt carbon
R_{adj}	Select	IRC Model X-201, Mallory Model MTC-1 or equivalent
R_{sc}	Select	1/2 watt carbon
R'_L	Select	For minimum current of 1 mAdc
C_o	10 µF	Sprague 1500 Series, Dickson D10C series or equivalent
C_n	0.1 µF	Ceramic Disc – Centralab DDA104, or equivalent
C_C	0.001 µF	Sprague TG-P10, or equivalent
J_1		Jumper
Q1		MC1563R or MC1463R
*HS		Heatsink Thermalloy #6168B or equivalent
*Socket	(Not Shown)	Robinson Nugent #0001306 or equivalent Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1 or equivalent
PC Board		Circuit DOT, Inc. #PC1113 or equivalent 1155 W. 23rd St. Tempe, Arizona 85281

*Optional

MC1466L
MC1566L

Specifications and Applications Information

MONOLITHIC VOLTAGE AND CURRENT REGULATOR

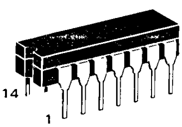
This unique "floating" regulator can deliver hundreds of volts – limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466/MC1566 integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.01% +1.0 mV
- Excellent Load Voltage Regulation, 0.01% +1.0 mV
- Excellent Current Regulation, 0.1% +1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

PRECISION WIDE-RANGE VOLTAGE and CURRENT REGULATOR

EPITAXIAL PASSIVATED INTEGRATED CIRCUIT

CERAMIC PACKAGE
CASE 632
TO-116



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ORDERING INFORMATION		
Device	Temperature Range	Package
MC1466L	0°C to +70° C	Ceramic DIP
MC1566L	−55°C to +125°C	Ceramic DIP

TYPICAL APPLICATIONS

FIGURE 1 – 0-TO-15 VDC, 10-AMPERES REGULATOR

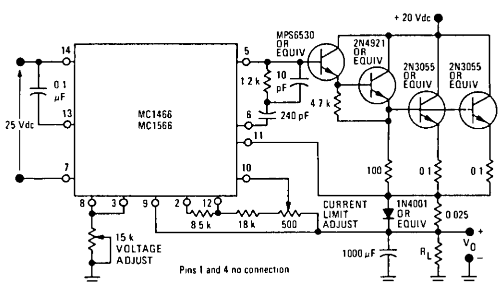


FIGURE 2 – 0-TO-40 VDC, 0.5-AMPERE REGULATOR

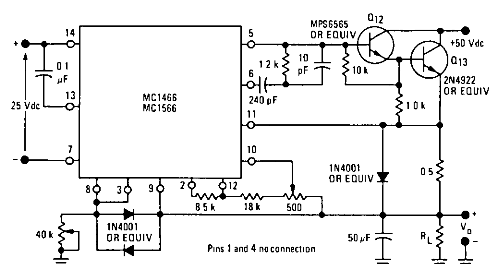


FIGURE 3 – 0-TO-250 VDC, 0.1-AMPERE REGULATOR

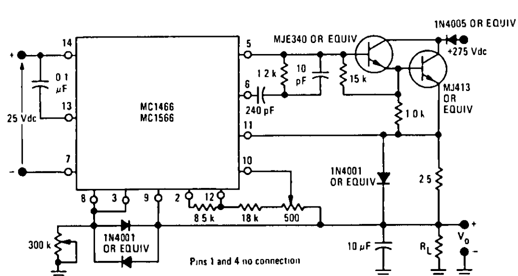
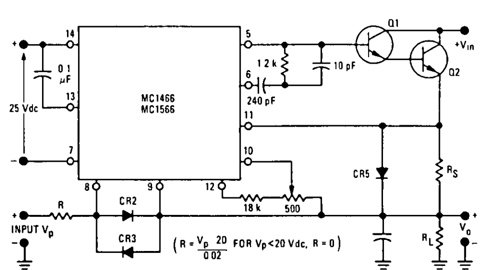


FIGURE 4 – REMOTE PROGRAMMING



MAXIMUM RATINGS (T_A = +25° unless otherwise noted)

Rating	Symbol	Value	Unit
Auxiliary Voltage	V_{aux}		Vdc
MC1466		30	
MC1566		35	
Power Dissipation (Package Limitation)	P_D	750	mW
Derate above T_A = +50°C	$1/\theta_{JA}$	6.0	mW/°C
Operating Temperature Range	T_A		°C
MC1466		0 to +70	
MC1566		−55 to +125	
Storage Temperature Range	T_{stg}	−65 to +150	°C

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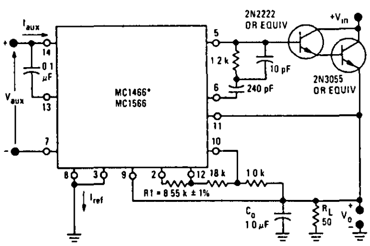
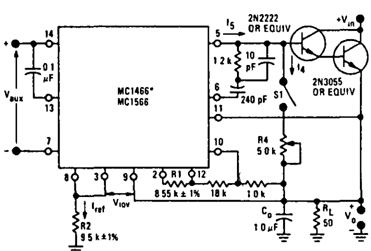
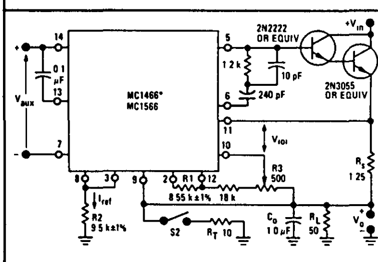
ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{aux} = +25 Vdc unless otherwise noted)

Characteristic Definition	Characteristic	Symbol	Min	Typ	Max	Units
	Auxiliary Voltage (See Notes 1 & 2) (Voltage from pin 14 to pin 7)	V_{aux}				Vdc
	MC1466		21	–	30	
	MC1566		20	–	35	
	Auxiliary Current	I_{aux}				mAdc
	MC1466		–	9.0	12	
	MC1566		–	7.0	8.5	
	Internal Reference Voltage (Voltage from pin 12 to pin 7)	V_{IR}				Vdc
	MC1466		17.3	18.2	19.7	
	MC1566		17.5	18.2	19	
	Reference Current (See Note 3)	I_{ref}				mAdc
	MC1466		0.8	1.0	1.2	
	MC1566		0.9	1.0	1.1	
	Input Current-Pin 8	I_8				µAdc
	MC1466		–	6.0	12	
	MC1566		–	3.0	6.0	
	Power Dissipation	P_D				mW
	MC1466		–	–	360	
	MC1566		–	–	300	
	Input Offset Voltage, Voltage Control Amplifier (See Note 4)	V_{iov}				mVdc
	MC1466		0	15	40	
	MC1566		3.0	15	25	
	Load Voltage Regulation (See Note 5)	ΔV_{iov}				
	MC1466		–	1.0	3.0	mV
	MC1566		–	0.7	1.0	
	MC1466	$\Delta V_{ref}/V_{ref}$	–	0.015	0.03	%
	MC1566		–	0.004	0.01	
	Line Voltage Regulation (See Note 6)	ΔV_{iov}				
	MC1466		–	1.0	3.0	mV
	MC1566		–	0.7	1.0	
	MC1466	$\Delta V_{ref}/V_{ref}$	–	0.015	0.03	%
	MC1566		–	0.004	0.01	
	Temperature Coefficient of Output Voltage	TCV_o				%/°C
	(T_A = 0 to +75°C) MC1466		–	0.01	–	
	(T_A = −55 to +25°C) MC1566		–	0.006	–	
	(T_A = +25 to +125°C) MC1566		–	0.004	–	
	Input Offset Voltage, Current Control Amplifier (See Note 4)	V_{ioi}				mVdc
	MC1466		0	15	40	
	(Voltage from pin 10 to pin 11) MC1566		3.0	15	25	
	Load Current Regulation (See Note 7)	$\Delta I_L/I_L$				
	MC1466		–	–	0.2	%
	MC1566		–	–	0.1	
	MC1466	ΔI_{ref}	–	–	1.0	mAdc
	MC1566		–	–	1.0	

*Pins 1 and 4 no connection.

NOTE 1.
The instantaneous input voltage, V_{aux}, must not exceed the maximum value of 30 volts for the MC1466 or 35 volts for the MC1566 The instantaneous value of V_{aux} must be greater than 20 volts for the MC1566 or 21 volts for the MC1466 for proper internal regulation

NOTE 2
The auxiliary supply voltage V_{aux}, must "float" and be electrically isolated from the unregulated high voltage supply, V_{in}.

NOTE 3.
Reference current may be set to any value of current less than 1 2 mAdc by applying the relationship

$$I_{ref}\,(mA) = \frac{8\ 55}{R_1\,(k\Omega)}$$

NOTE 4
A built-in offset voltage (15 mVdc nominal) is provided so that the power supply output voltage or current may be adjusted to zero

NOTE 5
Load Voltage Regulation is a function of two additive components, ΔV_{IOV} and ΔV_{ref}, where ΔV_{IOV} is the change in input offset voltage (measured between pins 8 and 9) and ΔV_{ref} is the change in voltage across R2 (measured between pin 8 and ground). Each component may be measured separately or the sum may be measured across the load. The measurement procedure for the test circuit shown is

a. With S1 open (I_4 = 0) measure the value of V_{IOV} (1) and V_{ref} (1)

b. Close S1, adjust R4 so that I_4 = 500 μA and note V_{IOV} (2) and V_{ref} (2).

Then $\Delta V_{IOV} = V_{IOV}(1) - V_{IOV}(2)$

% Reference Regulation =

$$\frac{[V_{ref}(1) - V_{ref}(2)]}{V_{ref}(1)}\,(100\%) = \frac{\Delta V_{ref}}{V_{ref}}\,(100\%)$$

Load Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\,(100\%) + \Delta V_{IOV}\,.$$

NOTE 6·
Line Voltage Regulation is a function of the same two additive components as Load Voltage Regulation, ΔV_{IOV} and ΔV_{ref} (see note 5) The measurement procedure is

a. **Set the auxiliary voltage, V_{aux}, to 22 volts for the MC1566 or the MC1466. Read the value of V_{IOV} (1) and V_{ref} (1).**

b. **Change the V_{aux} to 28 volts for the MC1566 or the MC1466 and note the value of V_{IOV} (2) and $V_{ref(2)}$. Then compute Line Voltage Regulation:**

$$\Delta V_{IOV} = \Delta V_{IOV}(1) - V_{IOV}(2)$$

% Reference Regulation =

$$\frac{[V_{ref}(1) - V_{ref}(2)]}{V_{ref}(1)}\,(100\%) = \frac{\Delta V_{ref}}{V_{ref}}\,(100\%)$$

Line Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\,(100\%) + \Delta V_{IOV}\,.$$

NOTE 7
Load Current Regulation is measured by the following procedure

a. With S2 open, adjust R3 for an initial load current, $I_{L(1)}$, such that V_O is 8.0 Vdc.

b With S2 closed, adjust R_T for V_O = 1 0 Vdc and read $I_{L(2)}$ Then Load Current Regulation =

$$\frac{[I_{L(2)} - I_{L(1)}]}{I_{L(1)}}\,(100\%) + I_{ref}$$

where I_{ref} is 1 0 mAdc, Load Current Regulation is specified in this manner because I_{ref} passes through the load in a direction opposite that of load current and does not pass through the current sense resistor, R_S

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FIGURE 5

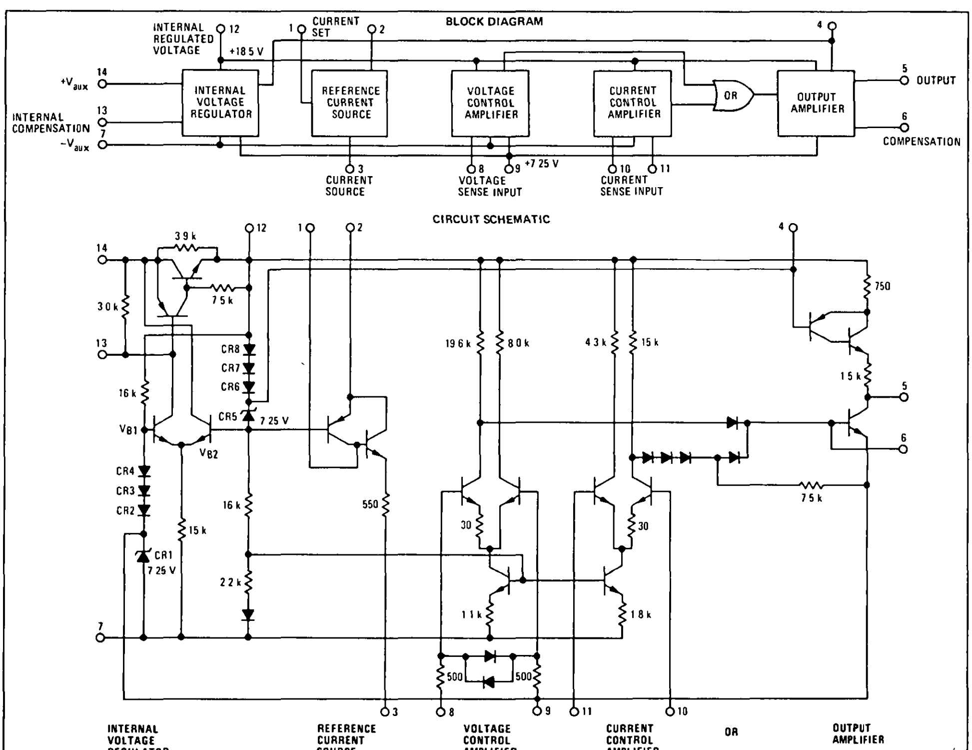
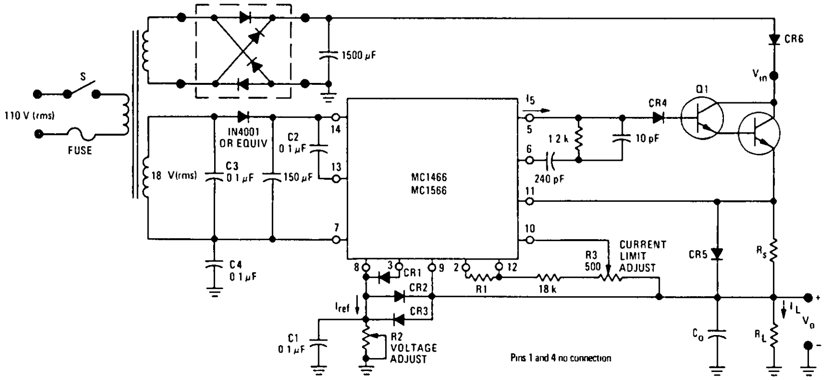
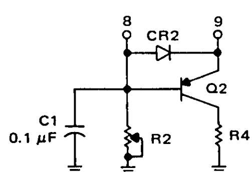


FIGURE 6 — TYPICAL CIRCUIT CONNECTION



NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

1. Constant Voltage:
   For constant voltage operation, output voltage V_O is given by
   $V_O = (I_{ref})(R_2)$
   where R2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.
   The recommended value of I_{ref} is 1.0 mAdc. Resistor R1 sets the value of I_{ref}:
   $I_{ref} = \frac{8.5}{R_1}$
   where R1 is the resistance between pins 2 and 12.
2. Constant Current:
   For constant current operation:
   (a) Select R_S for a 250 mV drop at the maximum desired regulated output current, I_{max}.
   (b) Adjust potentiometer R3 to set constant current output at desired value between zero and I_{max}.
3. If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466/MC1566 during short-circuit or transient conditions.
4. In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 μF to 2.0 μF). When R2 is bypassed, CR1 is necessary for protection during short-circuit conditions.
5. CR5 is recommended to protect the MC1466/MC1566 from simultaneous pass transistor failure and output short-circuit.
6. The RC network (10 pF, 240 pF, 1.2 k ohms) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_T of Q1 and Q2 is greater than 0.5 MHz.
7. For remote sense applications, the positive voltage sense terminal (pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2) is connected to the negative load terminal through a separate sense lead.
8. C_O may be selected by using the relationship:
   $C_O = (100\ \mu F)\ I_{L(max)}$, where $I_{L(max)}$ is the maximum load current in amperes.
9. C2 is necessary for the internal compensation of the MC1466/MC1566.
10. For optimum regulation, current out of pin 5, I_5, should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:
    $$\frac{I_{max}}{\beta 1 \beta 2} \leq 0.5\ \text{mAdc}$$
    where: I_{max} = maximum short-circuit load current (mAdc)
    $\beta 1$ = minimum beta of Q1
    $\beta 2$ = minimum beta of Q2
    Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5$ mAdc will result in a degradation in regulation.
11. CR6 is recommended when $V_O > 150$ Vdc and should be rated such that Peak Inverse Voltage $> V_O$.
12. In applications where R2 might be rapidly reduced in value, it is recommended that CR3 be replaced by Q2 and R4.



This design consideration prevents R2 from being destroyed by excessive discharge current from C_O. Components Q2 and R4 should be selected such that:

$$R4 = \frac{R2}{10} \text{ and}$$

$$BV_{CEO} \text{ of Q2} \geq V_O$$

OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1566/MC1466 voltage and current regulator and also provides information on useful applications.

SUBJECT SEQUENCE

Theory of Operation
Applications
Transient Failures
Voltage/Current-Mode Indicator

THEORY OF OPERATION

The schematic of Figure 5 can be simplified by breaking it down into basic functions, beginning with a simplified version of the voltage reference, Figure 7. Zener diodes CR1 and CR5 with their associated forward biased diodes CR2 through CR4 and CR6 through CR8 form the stable reference needed to balance the differential amplifier. At balance ($V_{B1} = V_{B2}$), the output voltage, ($V_{12} - V_7$), is at a value that is twice the drop across either of the two diode strings: $V_{12} - V_7 \doteq 2\ (V_{CR1} + V_{CR2} + V_{CR3} + V_{CR4})$. Other voltages, temperature compensated or otherwise, are also derived from these diodes strings for use in other parts of the circuit.

The voltage controlled current source (Figure 8) is a PNP-NPN composite which, due to the high NPN beta, yields a good working PNP from a lateral device working at a collector current of only a few microamperes. Its base voltage (V_{B2}) is derived from a temperature compensated portion of the diode string and consequently the overall current is dependent on the value of emitter resistor R1. Temperature compensation of the base emitter junction of Q3 is not important because approximately 9 volts exists between V_{B2} and V_{12}, making the ΔV_{BE}'s very small in percentage. Circuit reference voltage is derived from the product of I_R and R_R; if I_R is set at 1 mA (R1 = 8.5 kΩ), then R_R (in kΩ) = V_o. Other values of current may be used as long as the following restraints are kept in mind: 1) package dissipation will be increased by about 11 mW/mA and 2) bias current for the voltage control amplifier is 3 μA, temperature dependent, and is extracted from the reference current. The reference current should

FIGURE 7 — REFERENCE VOLTAGE REGULATOR

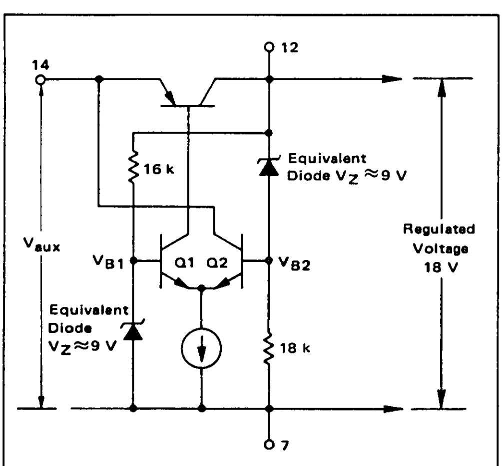
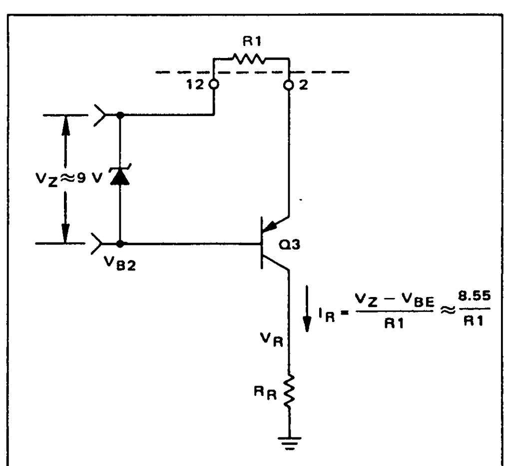


FIGURE 8 — VOLTAGE CONTROLLED CURRENT SOURCE



be at least two orders of magnitude above the largest expected bias current.

Loop amplification in the constant voltage mode is supplied by the voltage controlled amplifier (Figure 9), a standard high-gain differential amplifier. The inputs are diode-protected against differential overvoltages and an emitter degenerating resistor, R_{OS}, has been added to one of the transistors. For an emitter current in both Q5 and Q6 of 1/2 milliampere there will exist a preset offset voltage in this differential amplifier of 15 mV to insure that the output voltage will be zero when the reference voltage is zero. Without R_{OS}, the output voltage could be a few millivolts above zero due to the inherent offset. Since the load resistor is so large in this stage compared with the load (Q9) it will be more instructive to look at the gain on a transconductance basis rather than voltage gain. Transconductance of the differential stage is defined for small signals as:

$$g_m = \frac{1}{2r_e + R_E} \qquad (1)$$

where

$$r_e \approx \frac{0.026}{I_E} \text{ and}$$

R_E = added emitter degenerating resistance.

For I_E = 0.5 mA,

$$g_m = \frac{1}{104+30} = \frac{1}{134} = 7.5 \text{ mA/volt.} \qquad (2)$$

FIGURE 9 – VOLTAGE CONTROL AMPLIFIER

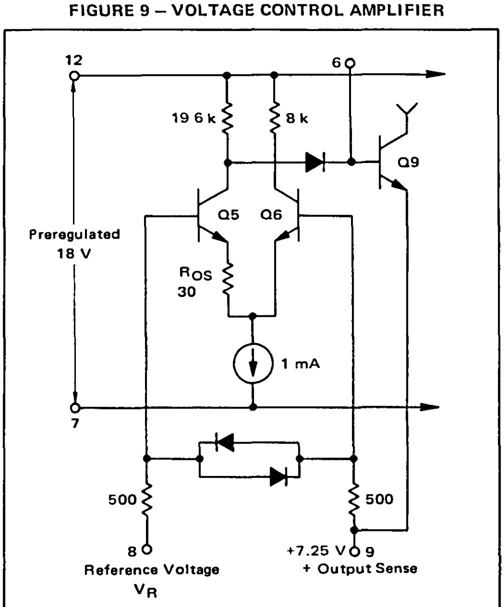
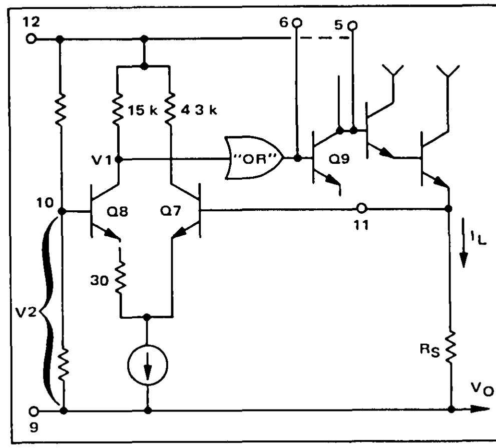


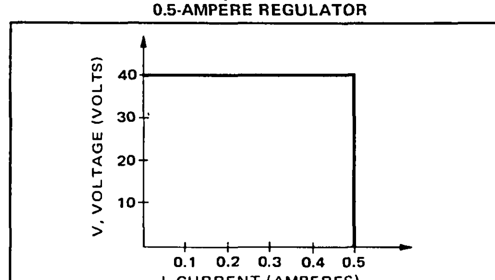
FIGURE 10 – CURRENT CONTROL CIRCUIT



This level is further boosted by the output stage such that in the constant voltage mode overall transconductance is about 300 mA/volt.

A second differential stage nearly identical to the first stage, serves as the current control amplifier (Figure 10). The gain of this stage insures a rapid crossover from the constant voltage to constant current modes and provides a convenient point to control the maximum deliverable load current. In use, a reference voltage derived from the preregulator and a voltage divider is applied to pin 10 while the output current is sampled across R_S by pin 11. When I_L R_S is 15 mV below the reference value, voltage V_1 begins to rapidly rise, eventually gaining complete control of Q9 and limiting output current to a value of V_2/R_S. If V_2 is derived from a variable source, short circuit current may be controlled over the complete output current capability of the regulator. Since the constant-voltage to constant-current change-over requires only a few millivolts the voltage regulation maintains its quality to the current limit and accordingly shows a very sharp "knee" (1% +1 mA, Figure 11). Note that the regulator can switch back into the constant voltage mode if the output voltage reaches a value greater than V_R. Operation through zero milliamperes is guaranteed by the inclusion of another emitter offsetting resistor.

FIGURE 11 – V_I CURVE FOR 0-TO-40 V, 0.5-AMPERE REGULATOR



Transistor Q9 and five diodes comprise the essential parts of the output stage (Figure 12). The diodes perform an "OR" function which allows only one mode of operation at a time - constant current or constant voltage. However, an additional stage (Q9) must be included to invert the logic and make it compatible with the driving requirements of series pass transistors as well as provide additional gain. A 1.5 mA collector current source sets the maximum deliverable output current and boosts the output impedance to that of the current source.

Note that the negative (substrate) side of the MC1566/MC1466 is 7.25 volts lower than the output voltage, and the reference regulator guarantees that the positive side is 11 volts above the output. Thus the IC remains at a voltage (relative to ground) solely dependent on the output, "floating" above and below V_O. V_{CE} across Q9 is only two or three V_{BE}'s depending on the number of transistors used in the series pass configuration.

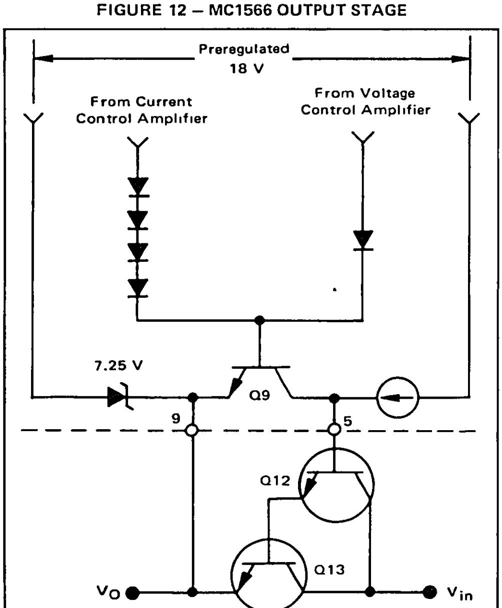
Performance characteristics of the regulator may be approximately calculated for a given circuit (Figure 2). Assuming that the two added transistors (Q12 and Q13) have minimum beta's of 20, then the overall regulator transconductance will be:

$$g_{mT} = (400)\,300\text{ mA/volt} = 120\text{ A/volt}. \quad (3)$$

For a change in current of 500 mA the output voltage will drop only.

$$\Delta V = \frac{0.5}{120} = 4.2\text{ mV}. \quad (4)$$

FIGURE 12 – MC1566 OUTPUT STAGE



The analysis thus far does not consider changes in V_R due to output current changes. If I_L increases by 500 mA the collector current of Q9 decreases by 1.25 mA, causing the collector current of Q5 to increase by 30 μA. Accordingly, I_R will be decreased by ≈0.30 μA which will drop the output by 0.03%. This figure may be improved considerably by either using high beta devices as the pass transistors, or by increasing I_R. Note again, however, that the maximum power rating of the package must be kept in mind. For example if I_R = 4 mA, power dissipation is

$$P_D = 20\text{ V }(8\text{ mA}) + (11\text{ V} \times 3\text{ mA}) = 193\text{ mW}. \quad (5)$$

This indicates that the circuit may be safely operated up to 118°C using 20 volts at the auxiliary supply voltage. If, however, the auxiliary supply voltage is 35 volts,

$$P_D = 35\text{ V }(8\text{ mA}) + 26\text{ V }(3\text{ mA}) = 358\text{ mW}. \quad (6)$$

which dictates that the maximum operating temperature must be less than 91°C to keep package dissipation within specified limits.

Line voltage regulation is also a function of the voltage change between pins 8 and 9, and the change of V_{ref}. In this case, however, these voltages change due to changes in the internal regulator's voltages, which in turn are caused by changes in V_{aux}. Note that line voltage regulation is not a function of V_{in}. Note also that the instantaneous value of V_{aux} must always be between 20 and 35 volts.

Figure 6 shows six external diodes (CR_1 to CR_6) added for protective purposes. CR_1 should be used if the output voltage is less than 20 volts and CR_2, CR_3 are absent. For V_o higher than 20 volts, CR_1 should be discarded in favor of CR_2 and CR_3. Diode CR_4 prevents IC failure if the series pass transistors develop collector-base shorts while the main power transistor suffers a simultaneous open emitter. If the possibility of such a transistor failure mode seems remote, CR_4 may be deleted. To prevent instantaneous differential and common-mode breakdown of the current sense amplifier, CR_5 must be placed across the current limit resistor R_S.

Load transients occasionally produce a damaging reversal of current flow from output to input $V_o > 150$ volts (which will destroy the IC). Diode CR_6 prevents such reversal and renders the circuit immune from destruction for such conditions, e.g., adding a large output capacitor after the supply is turned "on". Diodes CR_1, CR_2, CR_3, and CR_5 may be general purpose silicon units such as 1N4001 or equivalent whereas CR_4 and CR_6 should have a peak inverse voltage rating equal to V_{in} or greater.

APPLICATIONS

Figure 2 shows a typical 0-to-40 volts, 0.5-ampere regulator with better than 0.01% performance, The RC network between pins 5 and 6 and the capacitor between pins 13 and 14 provide frequency compensation for the MC1566/MC1466. The external pass transistors are used to boost load current, since the output current of the regulator is less than 2 mA.

4

Figure 1 is a 0-to-15 volts, 10-ampere regulator with the pass transistor configuration necessary to boost the load current to 10 amperes. Note that C_O has been increased to 1000 μF following the general rule:

$$C_O = 100\ \mu F/A\ I_L.$$

The prime advantage of the MC1566/MC1466 is its use as a high voltage regulator, as shown in Figure 3. This 0-to-250 volts 0.1-ampere regulator is typical of high voltage applications, limited only by the breakdown and safe areas of the output pass transistors.

The primary limiting factor in high voltage series regulators is the pass transistor. Figure 13 shows a safe area curve for the MJ413. Looking at Figure 3, we see that if the output is shorted, the transistor will have a collector current of 100 mA, with a V_{CE} approximately equal to 260 volts. Thus this point falls on the dc line of the safe area curve, insuring that the transistor will not enter secondary breakdown.

In this respect (Safe Operating Area) the foldback circuit of Figure 14 is superior for handling high voltages and yet is short-circuit protected. This is due to the fact that load current is diminished as output voltage drops (V_{CE} increases as V_O drops) as seen in Figure 15. By careful design the load current at a short, I_{SC} can be made low enough such that the combined V_{CE} (V_{in}) and I_{SC} still falls within the dc safe operating area of the transistor. For the illustrated design (Figure 14), an input voltage of 210 volts is compatible with a short-circuit current of 100 mA. Yet current foldback allows us to design for a maximum regulated load current of 500 mA. The pertinent design equations are:

$$\text{Let } R_2\ (k\Omega) = V_O$$

$$\alpha = \frac{0.25}{V_O}\left[\frac{I_k}{I_{SC}} - 1\right]$$

$$R_1\ (k\Omega) = \frac{\alpha}{1-\alpha}\ V_O$$

$$R_{SC} = \frac{0.25}{(1-\alpha)\ I_{SC}}.$$

FIGURE 13 — SAFE AREA CURVE FOR THE MJ413

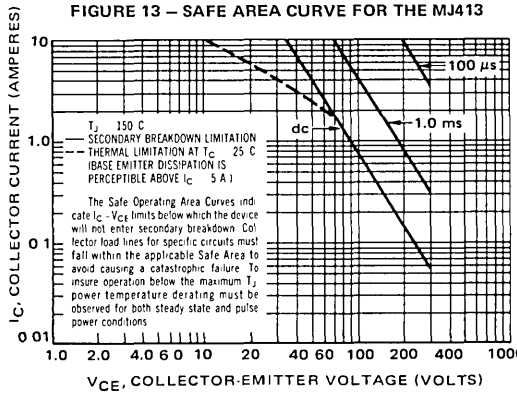
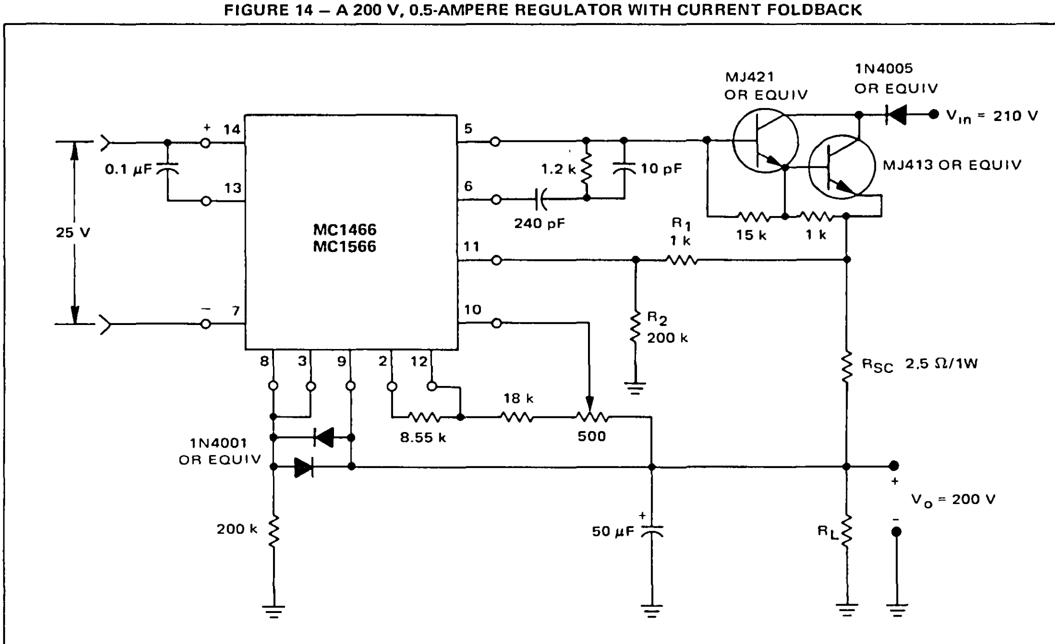


FIGURE 14 — A 200 V, 0.5-AMPERE REGULATOR WITH CURRENT FOLDBACK



The terms I_{SC} and I_K correspond to the short-circuit current and maximum available load current as shown in Figure 15.

FIGURE 15 – TYPICAL FOLDBACK PERFORMANCE

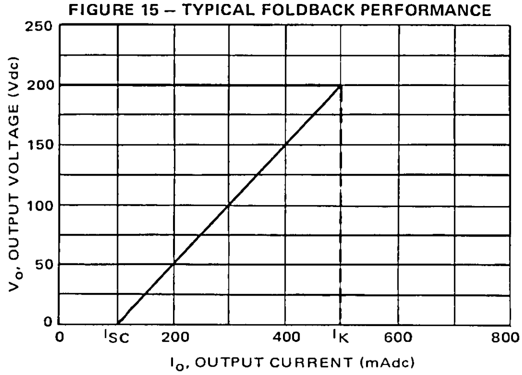


Figure 16 shows a remote sense application which should be used when high current or long wire lengths are used. This type of wiring is recommended for any application where the best possible regulation is desired. Since the sense lines draw only a small current, large voltage drops do not destroy the excellent regulation of the MC1566/MC1466.

TRANSIENT FAILURES

In industrial areas where electrical machinery is used the normal ac line often contains bursts of voltage running from hundreds to thousands of volts in magnitude and only microseconds in duration. Under some conditions this energy is dissipated across the internal zener connected between pins 9 and 7. This transient condition may produce a total failure of the regulator device without any apparent explanation. This type of failure is identified by absence of the 7-volt zener (CR1) between pin 9 and pin 7. To prevent this failure mode the use of a shielded power transformer is recommended, as shown in Figure 6. In addition, it is recommended that C1, C3 and C4 be included to aid in transient repression. These capacitors should have good high frequency characteristics.

If the possibility of transients on the output exists, the addition of a resistor and zener diode between pins 9 and 7 as shown on Figure 17 should be added.

VOLTAGE/CURRENT – MODE INDICATOR

There may be times when it is desirable to know when the MC1566/MC1466 is in the constant current mode or constant voltage mode. A mode indicator can be easily added to provide this feature. Figure 18 shows how a PNP transistor has replaced a protection diode between pins 8 and 9 of Figure 2. When the MC1566/MC1466 goes from constant voltage mode to constant current mode, V_O will drop below V_8 and the PNP transistor will turn on. The 1-mA current supplied by pin 8 will now be shunted to base of Q2 thereby turning on the indicator device I1.

FIGURE 16 – REMOTE SENSE

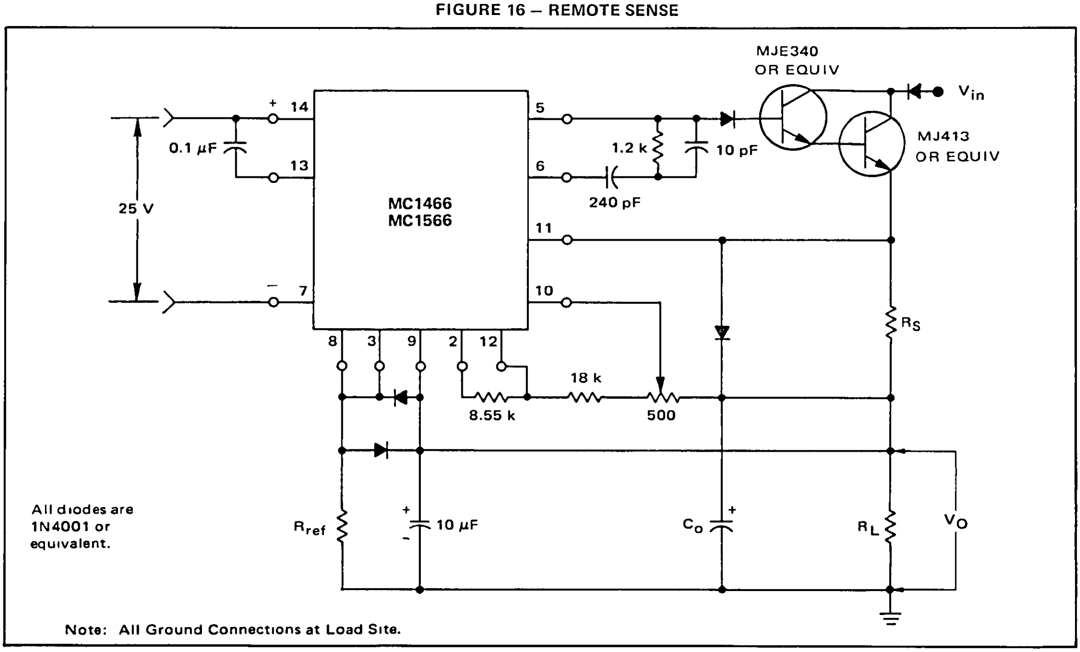


FIGURE 17 – A 0-TO-250 VOLT, 0.1-AMPERE REGULATOR

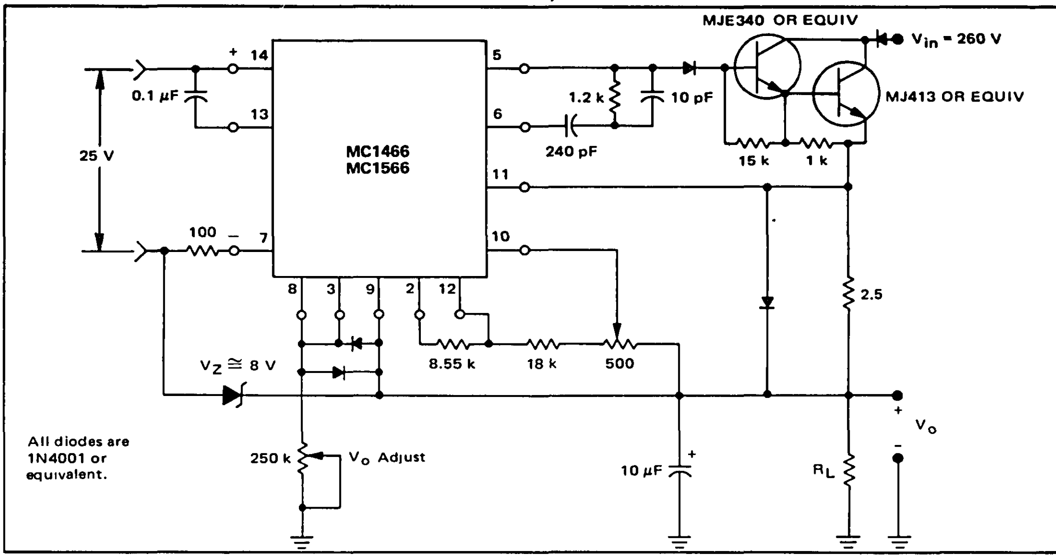
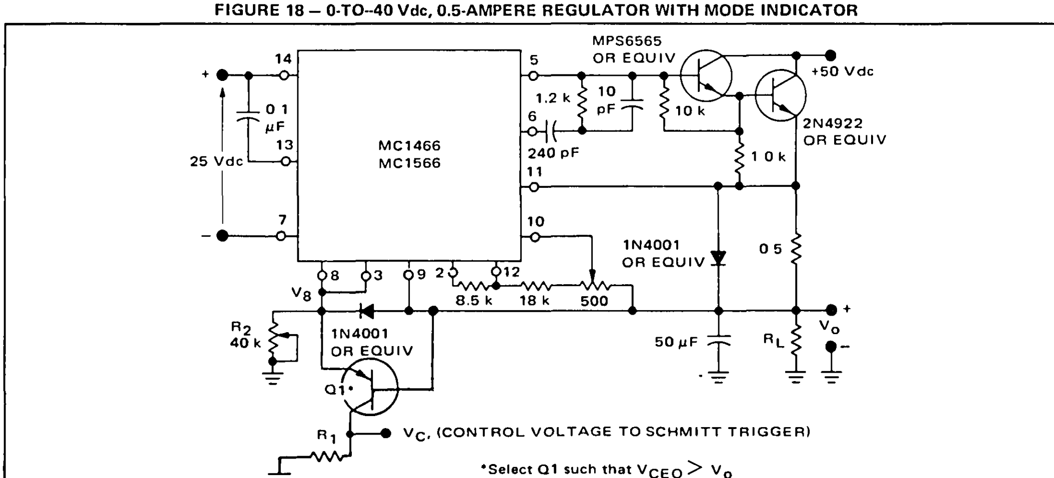


FIGURE 18 – 0-TO–40 Vdc, 0.5-AMPERE REGULATOR WITH MODE INDICATOR



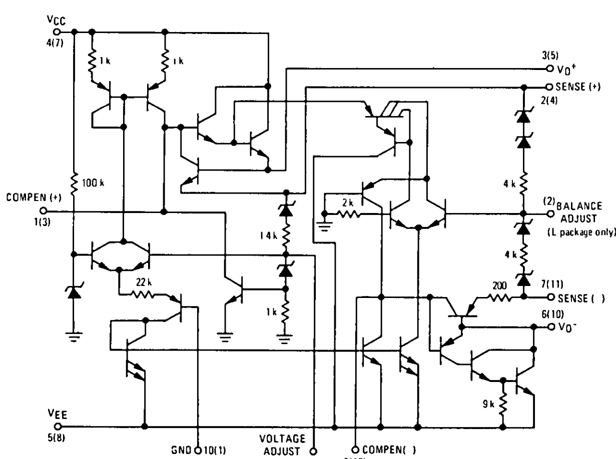
MC1468
MC1568

DUAL ±15-VOLT REGULATOR

The MC1568/MC1468 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100 mA. Internally, the device is set for ± 15-volt outputs but an external adjustment can be used to change both outputs simultaneously from 8.0 to 20 volts. Input voltages up to ± 30 volts can be used and there is provision for adjustable current limiting. The device is available in three package types to accomodate various power requirements.

- Internally set to ±15 V Tracking Outputs
- Output Currents to 100 mA
- Outputs Balanced to within 1% (MC1568)
- Line and Load Regulation of 0.06%
- 1% Maximum Output Variation due to Temperature Changes
- Standby Current Drain of 3.0 mA
- Externally Adjustable Current Limit
- Remote Sensing Provisions
- Case is at Ground Potential (R suffix package)

CIRCUIT SCHEMATIC

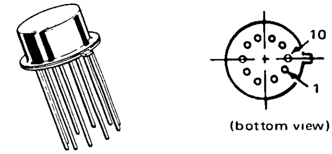


Pin numbers adjacent to terminals are for the G and R suffix packages only. Pin numbers in parentheses are for the L suffix package only.

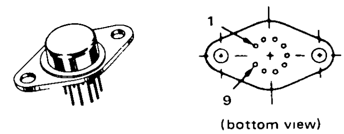
Pin 10 is ground for the G suffix package only. For the R package the case is ground.

DUAL ±15-VOLT TRACKING REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

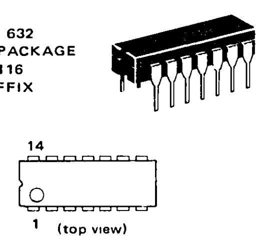


CASE 603C
METAL PACKAGE
TO-100
G SUFFIX



CASE 614
METAL PACKAGE
R SUFFIX

CASE 632
CERAMIC PACKAGE
TO-116
L SUFFIX



ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC1468G	0° C to +70° C	Metal Can
MC1468L	0° C to +70° C	Ceramic DIP
MC1468R	0° C to +70° C	Metal Power
MC1568G	−55° C to +125° C	Metal Can
MC1568L	−55° C to +125° C	Ceramic DIP
MC1568R	−55° C to +125° C	Metal Power

4

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
Input Voltage	$V_{CC}, \|V_{EE}\|$	30			Vdc
Peak Load Current	I_{PK}	100			mA
Power Dissipation and Thermal Characteristics		G Package	R Package	L Package	
T_A = +25°C	P_D	0.8	2.4	1.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	6.6	28.5	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	35	100	°C/W
T_C = +25°C	P_D	2.1	9.0	2.5	Watts
Derate above T_C = +25°C	$1/\theta_{JC}$	14	61	20	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	70	17	50	°C/W
Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175			°C
Minimum Short-Circuit Resistance	$R_{SC}(min)$	4.0			Ohms

4

OPERATING TEMPERATURE RANGE

Ambient Temperature		T_A		°C
	MC1468		0 to +70	
	MC1568		-55 to +125	

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, V_{EE} = -20 V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 μF, $R_{SC}^+ = R_{SC}^-$ = 4.0 Ω, $I_L^+ = I_L^-$ = 0, T_C = +25°C unless otherwise noted.) (See Figure 1.)

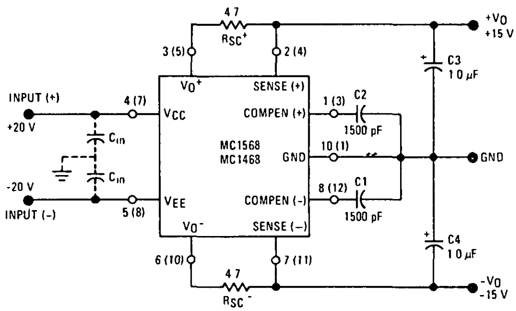
		MC1568			MC1468			
Characteristic	Symbol*	Min	Typ	Max	Min	Typ	Max	Unit
Output Voltage	V_O	±14.8	±15	±15.2	±14.5	±15	±15.5	Vdc
Input Voltage	V_{in}	–	–	±30	–	–	±30	Vdc
Input-Output Voltage Differential	$\|V_{in} - V_O\|$	2.0	–	–	2.0	–	–	Vdc
Output Voltage Balance	V_{Bal}	–	±50	±150	–	±50	±300	mV
Line Regulation Voltage	Reg_{in}							mV
(V_{in} = 18 V to 30 V)		–	–	10	–	–	10	
(T_{low} ① to T_{high} ②)		–	–	20	–	–	20	
Load Regulation Voltage	Reg_L							mV
(I_L = 0 to 50 mA, T_J = constant)		–	–	10	–	–	10	
(T_A = T_{low} to T_{high})		–	–	30	–	–	30	
Output Voltage Range	V_{OR}							Vdc
L Package (See Figure 4.)		±8.0	–	±20	±8.0	–	±20	
R and G Packages (See Figures 2 and 13.)		±14.5	–	±20	±14.5	–	±20	
Ripple Rejection (f = 120 Hz)	RR	–	75	–	–	75	–	dB
Output Voltage Temperature Stability (T_{low} to T_{high})	$\|TS_{V_O}\|$	–	0.3	1.0	–	0.3	1.0	%
Short-Circuit Current Limit (R_{SC} = 10 ohms)	I_{SC}	–	60	–	–	60	–	mA
Output Noise Voltage (BW = 100 Hz - 10 kHz)	V_N	–	100	–	–	100	–	μV(RMS)
Positive Standby Current (V_{in} = +30 V)	I_B^+	–	2.4	4.0	–	2.4	4.0	mA
Negative Standby Current (V_{in} = -30 V)	I_B^-	–	1.0	3.0	–	1.0	3.0	mA
Long-Term Stability	$\Delta V_O/\Delta t$	–	0.2	–	–	0.2	–	%/k Hr

① T_{low} = 0°C for MC1468
= -55°C for MC1568

② T_{high} = +70°C for MC1468
= +125°C for MC1568

TYPICAL APPLICATIONS

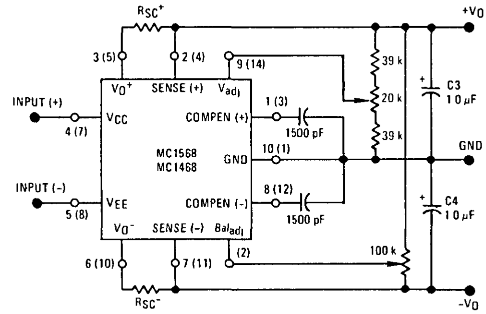
FIGURE 1 – BASIC 50-mA REGULATOR



C1 and C2 should be located as close to the device as possible A 0 1 μF ceramic capacitor (C_{in}) may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors

C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage At low temperature operation, it may be necessary to bypass C4 with a 0 1 μF ceramic disc capacitor

FIGURE 2 – VOLTAGE ADJUST AND BALANCE ADJUST CIRCUIT
(14.5 V ≤ V_{out} ≤ 20 V)



Balance adjust available in MC1568L, MC1468L ceramic dual in line package only

FIGURE 3 – ±1.5-AMPERE REGULATOR
(Short-Circuit Protected, with Proper Heatsinking)
(Metal-Packaged Devices Only, R Suffix)

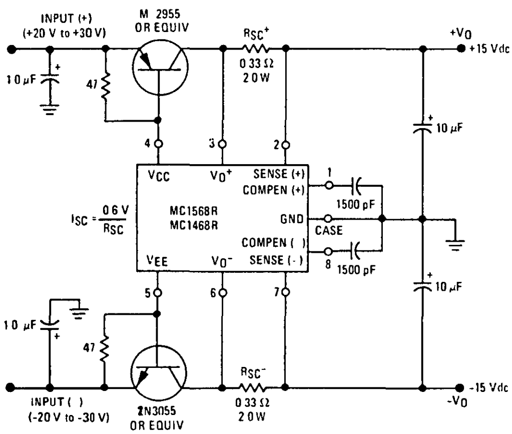
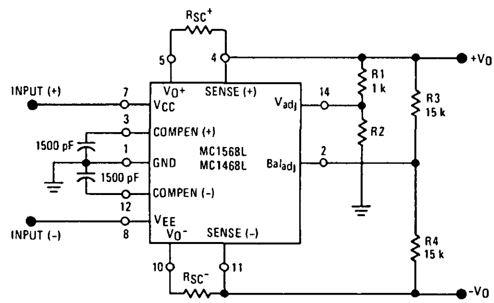


FIGURE 4 – OUTPUT VOLTAGE ADJUSTMENT FOR 8.0 V ≤ |±V_O| ≤ 14.5 V
(Ceramic-Packaged Devices Only, L Suffix.)



The presence of the Bal_{adj}, pin 2, on devices housed in the dual in line package (L suffix) allows the user to adjust the output voltages down to +8 0 V The required value of resistor R2 can calculated from

$$R2 = \frac{R1\,R_{int}(\phi + V_z)}{R_{int}(V_O - \phi - V_z) - \phi\,R1}$$

Where R_{int} = An Internal Resistor = R1 = 1 kΩ
ϕ = 0 68 V
V_z = 6 6 V

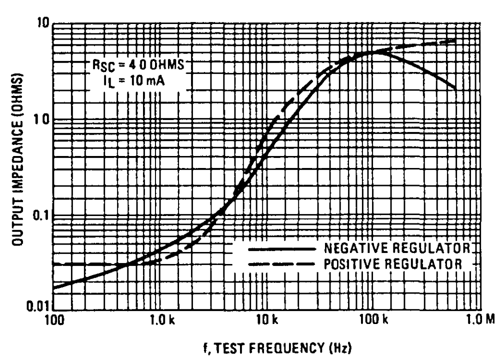
Some common design values are listed below

±V_O,V)	R2	T_C V_O (%/°C)	I_B + (mA)
14	1 2 k	0 003	10
12	1 8 k	0 022	7 2
10	3 5 k	0 025	5 0
8 0	∞	0 028	2 6

TYPICAL CHARACTERISTICS

(V_{CC} = +20 V, V_{EE} = -20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 – OUTPUT IMPEDANCE



TYPICAL CHARACTERISTICS

(V_{CC} = +20 V, V_{EE} = -20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 6 – LOAD REGULATION

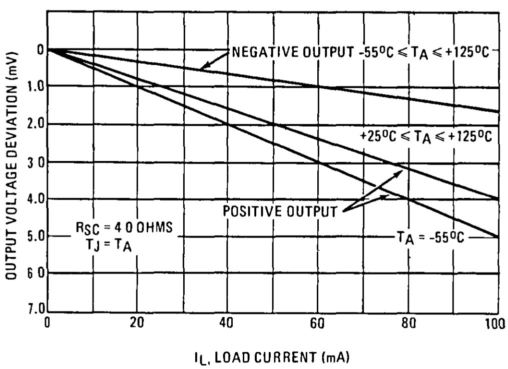


FIGURE 7 – REGULATOR DROPOUT VOLTAGE

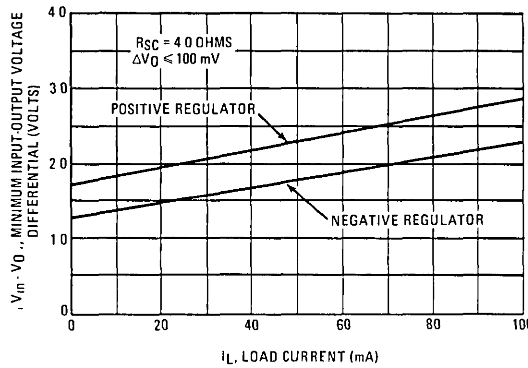


FIGURE 8 – MAXIMUM CURRENT CAPABILITY

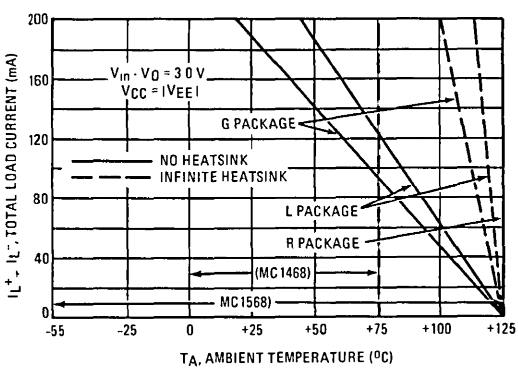


FIGURE 9 – MAXIMUM CURRENT CAPABILITY

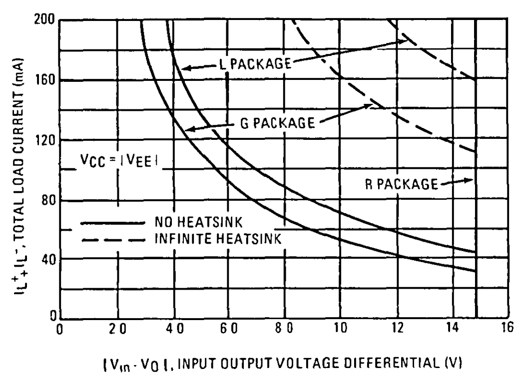


FIGURE 10 – I_{SC} versus R_{SC}

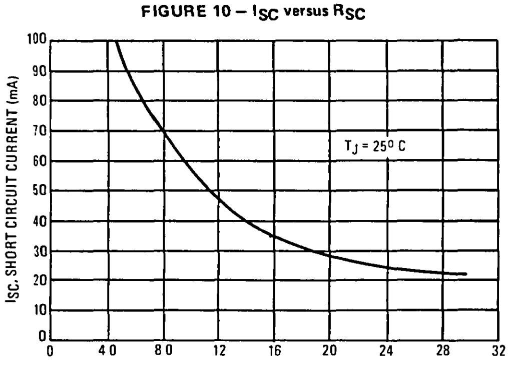
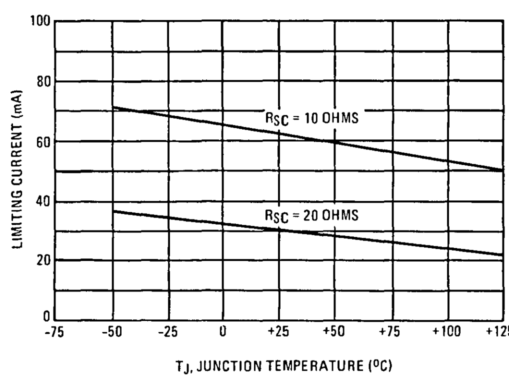


FIGURE 11 – CURRENT-LIMITING CHARACTERISTICS



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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +20 V, V_{EE} = −20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 12 – STANDBY CURRENT DRAIN

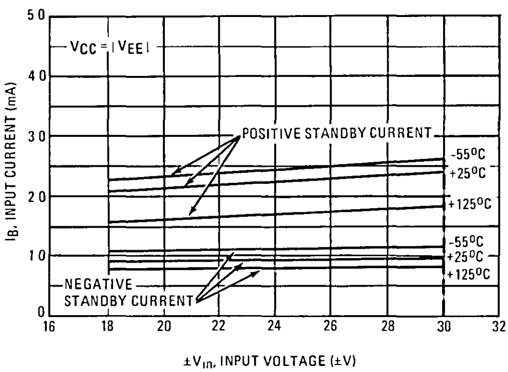


FIGURE 13 – STANDBY CURRENT DRAIN

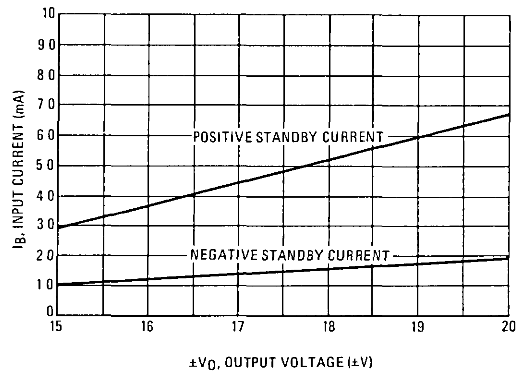


FIGURE 14 – TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

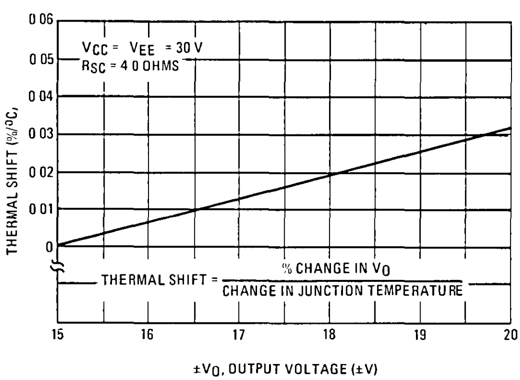


FIGURE 15 – LOAD TRANSIENT RESPONSE

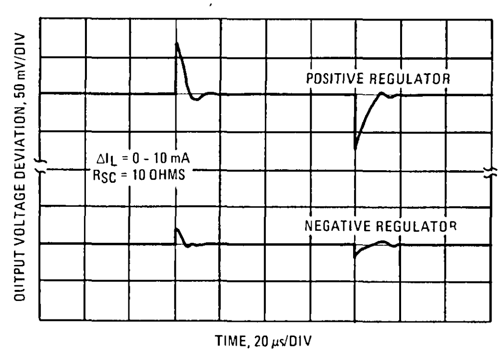


FIGURE 16 – LINE TRANSIENT RESPONSE

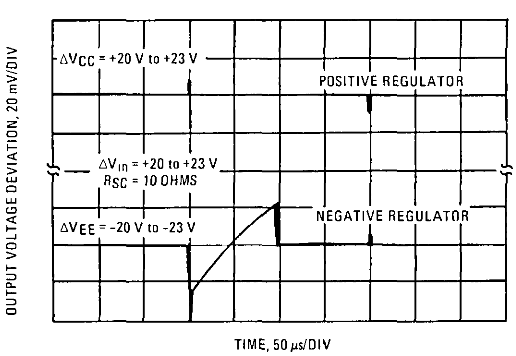
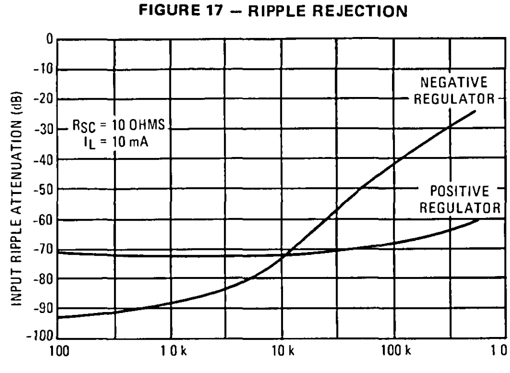


FIGURE 17 – RIPPLE REJECTION



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MC1469
MC1569

Specifications and Applications Information

MONOLITHIC VOLTAGE REGULATOR

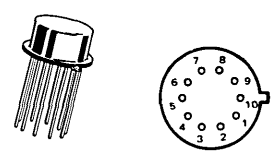
The MC1569/MC1469 is a positive voltage regulator designed to deliver continuous load current up to 500 mAdc. Output voltage is adjustable from 2.5 Vdc to 37 Vdc. The MC1569 is specified for use within the military temperature range (−55 to +125°C) and the MC1469 within the 0 to +70°C temperature range.

For systems requiring a positive regulated voltage, the MC1569 can be used with performance nearly identical to the MC1563 negative voltage regulator. Systems requiring both a positive and negative regulated voltage can use the MC1569 and MC1563 as complementary regulators with a common input ground.

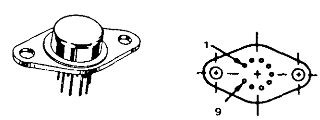
- Electronic "Shut-Down" Control
- Excellent Load Regulation (Low Output Impedance – 20 milli-ohms typ)
- High Power Capability: up to 17.5 Watts
- Excellent Temperature Stability: ±0.002 %/°C typ
- High Ripple Rejection: 0.002 %/V typ

POSITIVE VOLTAGE REGULATOR INTEGRATED CIRCUIT

SILICON NONOLITHIC
EPITAXIAL PASSIVATED



CASE 603
METAL PACKAGE
G SUFFIX



CASE 614
METAL PACKAGE
R SUFFIX

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC1469G	0° C to +70°C	Metal Can
MC1469R	0° C to +70° C	Metal Power
MC1569G	−55° C to +125° C	Metal Can
MC1569R	−55° C to +125° C	Metal Power

FIGURE 1 – ±15 V, ±400 mA COMPLEMENTARY TRACKING VOLTAGE REGULATOR

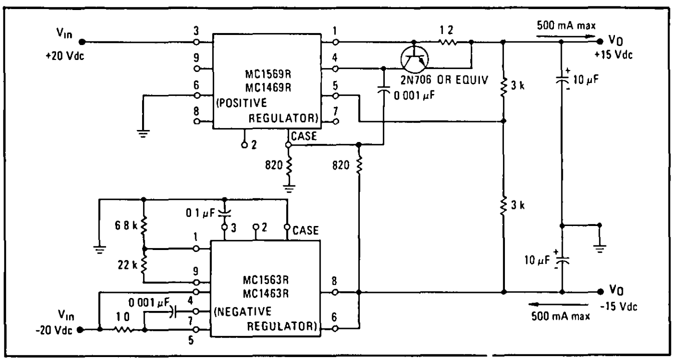


FIGURE 2 – TYPICAL CIRCUIT CONNECTION ($3.5 \leq V_O \leq 37$ Vdc, $1 \leq I_L \leq 500$ mA)

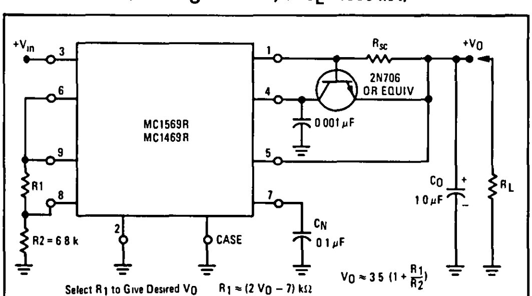
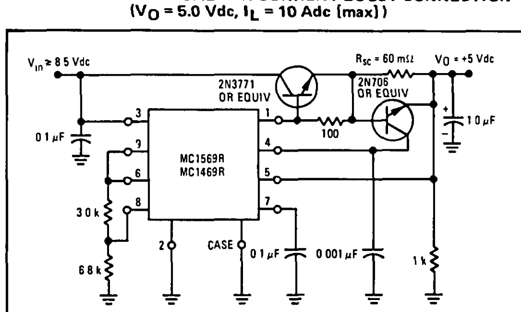


FIGURE 3 – TYPICAL NPN CURRENT BOOST CONNECTION (V_O = 5.0 Vdc, I_L = 10 Adc (max))



MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Input Voltage MC1469	V_{in}	35		Vdc
Input Voltage MC1569		40		
		G Package	R Package	
Peak Load Current	I_{PK}	250	600	mA
Current, Pin 2	$I_{pin\ 2}$	10	10	mA
Current, Pin 9	$I_{pin\ 9}$	5.0	5.0	
Power Dissipation and Thermal Characteristics				
T_A = +25°C	P_D	0.68	3.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	5.44	24	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	184	41.6	°C/W
T_C = +25°C	P_D	1.8	14	Watts
Derate above T_C = +25°C	$1/\theta_{JC}$	14.4	140	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	69.4	7.15	°C/W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150		°C

OPERATING TEMPERATURE RANGE

Ambient Temperature MC1469	T_A	0 to +70	°C
Ambient Temperature MC1569		-55 to +125	

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ELECTRICAL CHARACTERISTICS

(T_C = +25°C unless otherwise noted) (Load Current = 100 mA for "R" Package device, = 10 mA for "G" Package device, unless otherwise noted)

Characteristic	Fig.	Note	Symbol	MC1569 Min	MC1569 Typ	MC1569 Max	MC1469 Min	MC1469 Typ	MC1469 Max	Unit
Input Voltage ($T_A = T_{low}$ ① to T_{high} ②)	4	1	V_{in}	8.5	–	40	9.0	–	35	Vdc
Output Voltage Range	4,5		V_O	2.5	–	37	2.5	–	32	Vdc
Reference Voltage (Pin 8 to Ground, V_{in} = 15 V	4		V_{ref}	3.4	3.5	3.6	3.2	3.5	3.8	Vdc
Minimum Input-Output Voltage Differential (R_{sc} = 0)	4	2	$V_{in} - V_O$	–	2.1	2.7	–	2.1	3.0	Vdc
Bias Current (V_{in} = 15 V) (I_L = 1.0 mAdc, R_2 = 6.8 k ohms, $I_{IB} = I_{in} - I_L$)	4		I_{IB}	–	4.0	9.0	–	5.0	12	mAdc
Output Noise (C_N = 0.1 µF, f = 10 Hz to 5.0 MHz)	4		v_N	–	0.150	–	–	0.150	–	mV(rms)
Temperature Coefficient of Output Voltage	4	3	TCV_O	–	±0.002	–	–	±0.002	–	%/°C
Operating Load Current Range	4		I_L							mAdc
(R_{sc} ≤ 0.3 ohms) R Package				1.0	–	500	1.0	–	500	
(R_{sc} ≤ 2.0 ohms) G Package				1.0	–	200	1.0	–	200	
Input Regulation	6	4	Reg_{in}	–	0.002	0.015	–	0.003	0.030	%/V_O
Load Regulation	7	5	Reg_{load}							
(T_J = Constant [1.0 mA ≤ I_L ≤ 20 mA])				–	0.4	1.6	–	0 7	2.4	mV
(T_C = +25°C [1.0 mA ≤ I_L ≤ 50 mA]) R Package				–	0.005	0.05	–	0.005	0.05	%
G Package				–	0.01	0.13	–	0.01	0 13	
Output Impedance (C_c = 0.001 µF, R_{sc} = 1.0 ohm, f = 1.0 kHz, V_{in} = +14 Vdc, V_O = +10 Vdc)	8	6	z_o	–	20	–	–	35	–	milliohms
Shutdown Current (V_{in} = +35 Vdc)	9		I_{sd}	–	70	150	–	140	500	µAdc

① T_{low} = 0°C for MC1469
= -55°C for MC1569

② T_{high} = +70° C for MC1469
= +125°C for MC1569

Note 1 "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode. For output voltages greater than approximately 5.5 Vdc the minimum "total instantaneous input voltage" must increase to the extent that it will always exceed the output voltage by at least the "input-output voltage differential".

Note 2. This parameter states that the MC1569/MC1469 will regulate properly with the input-output voltage differential ($V_{in} - V_O$) as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with ($V_{in} - V_O$) as low as 2.1 Vdc as shown in the typical column. (See Figure 21.)

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$\text{MC1569, } TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min})\ (100)}{(180^\circ C)\ (V_O\ @\ 25^\circ C)} = \%/^\circ C$$

$$\text{MC1469, } TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min})\ (100)}{(75^\circ C)\ (V_O\ @\ 25^\circ C)} = \%/^\circ C$$

The output-voltage adjusting resistors (R1 and R2) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. Input regulation is the percentage change in output voltage per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{v_O}{V_O\ (v_{in})}\ 100\ (\%/V_O),$$

where v_O is the change in the output voltage V_O for the input change v_{in}.

The following example illustrates how to compute maximum output voltage change for the conditions given:

$$Reg_{in} = 0.015\ \%/V_O$$
$$V_O = 10\ \text{Vdc}$$
$$v_{in} = 1.0\ \text{V(rms)}$$
$$v_O = \frac{(Reg_{in})\ (v_{in})\ (V_O)}{100} = \frac{(0.015)\ (1.0)\ (10)}{100} = 0.0015\ \text{V(rms)}$$

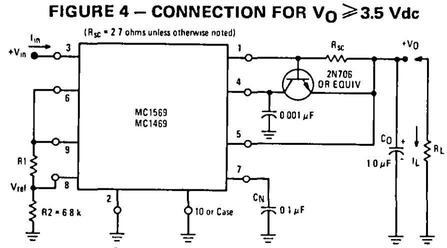
Note 5 Load regulation is specified for small ($\leqslant$+17°C) changes in junction temperature. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{[V_O|I_L = 1.0\ \text{mA}] - [V_O|I_L = 50\ \text{mA}]}{V_O\,|I_L = 1.0\ \text{mA}} \times 100$$

Note 6. The resulting low level output signal (v_O) will require the use of a tuned voltmeter to obtain a reading. Special care should be used to insure that the measurement technique does not include connection resistance, wire resistance, and wire lead inductance (i.e., measure close to the case). Note that No. 22 AWG hook-up wire has approximately 4.0 milliohms/in dc resistance and an inductive reactance of approximately 10 milliohms/in. at 100 kHz. Avoid use of alligator clips or banana plug-jack combination.

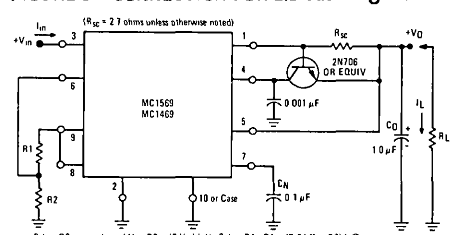
TEST CIRCUITS

FIGURE 4 — CONNECTION FOR $V_O \geqslant$ 3.5 Vdc



Select R1 to give desired V_O R1 ≈ (2 V_O 7) k Ω

FIGURE 5 — CONNECTION FOR 2.5 Vdc $\geqslant V_O \leqslant$ 3.5 Vdc



Select R2 to give desired V_O R2 ≈ (2 V_O) k Ω Select R1 R1 ≈ (7.0 kΩ – R2) k Ω

FIGURE 6 — INPUT REGULATION

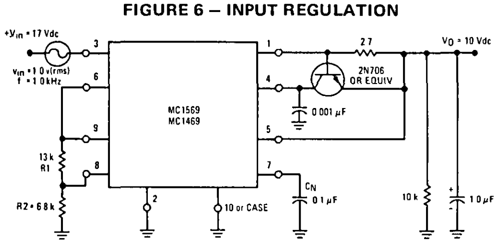


FIGURE 7 — LOAD REGULATION

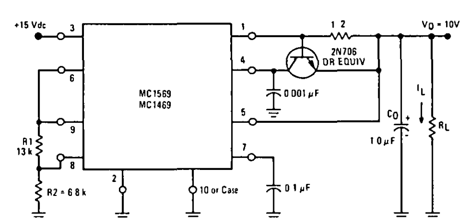


FIGURE 8 — OUTPUT IMPEDANCE

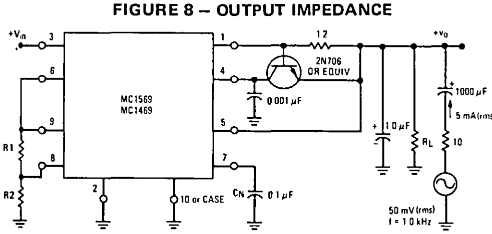
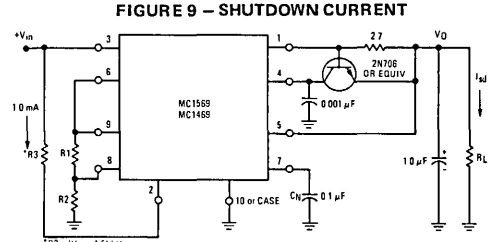


FIGURE 9 — SHUTDOWN CURRENT



*R3 = (V_{in} – 1.5) kΩ

GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
   a) For $V_O \geqslant 3.5$ Vdc – Output voltage is set by resistors R1 and R2 (see Figure 4). Set R2 = 6.8 k ohms and determine R1 from the graph of Figure 10 or from the equation:

   $$R1 \approx (2\,V_O - 7)\ k\Omega$$

   b) For $2.5 \leqslant V_O \leqslant 3.5$ Vdc – Output voltage is set by resistors R1 and R2 (see Figure 5). Resistors R1 and R2 can be determined from the graph of Figure 11 or from the equations:

   $$R2 \approx 2\,(V_O)\ k\Omega$$
   $$R1 \approx (7\ k\Omega - R2)\ k\Omega$$

   c) Output voltage, V_O, is determined by the ratio of R1 and R2, therefore optimum temperature performance can be achieved if R1 and R2 have the same temperature coefficient.
   d) Output voltage can be varied by making R1 adjustable as shown in Figure 43.
   e) If V_O = 3.5 Vdc (to supply MRTL* for example), tie pins 6, 8 and 9 together. R1 and R2 are not needed in this case.
2. Short Circuit Current, I_{sc}
   Short Circuit Current, I_{sc}, is determined by R_{sc}. R_{sc} may be chosen with the aid of Figure 12 or the expression:

   $$R_{sc} \approx \frac{0.6}{I_{sc}}\ \text{ohm}$$

   where I_{sc} is measured in amperes. This expression is also valid when current is boosted as shown in Figure 2.
3. Compensation, C_c
   A 0.001 μF capacitor, C_c, from pin 4 to ground will provide adequate compensation in most applications, with or without current boost. Smaller values of C_c will reduce stability and larger values of C_c will degrade pulse response and output impedance versus frequency. The physical location of C_c should be close to the MC1569/MC1469 with short lead lengths.
4. Noise Filter Capacitor, C_N
   A 0.1 μF capacitor, C_N, from pin 7 to ground will typically reduce the output noise voltage to 150 μV(rms). The value *of C_N can be increased or decreased, depending on the* noise voltage requirements of a particular application. A minimum value of 0.001 μF is recommended.
5. Output Capacitor, C_O
   The value of C_O should be at least 1.0 μF in order to provide good stability. The maximum value recommended is a function of current limit resistor R_{sc}:

   $$C_O\ \text{max} \approx \frac{250\ \mu F}{R_{sc}}$$

   where R_{sc} is measured in ohms. Values of C_O greater than this will degrade the pulse response characteristics and increase the settling time.
6. Shut-Down Control
   One method of turning "OFF" the regulator is to apply a dc voltage at pin 2. This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting. As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at Pin 2 will cause automatic shut-down for high junction temperatures. This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard Logic levels of MRTL, MDTL* or MTTL* can also be used to turn the regulator "ON" or "OFF".
7. Remote Sensing
   The connection to pin 5 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on z_O can be greatly reduced.

FIGURE 10 – R1 versus V_O
($V_O \geqslant 3.5$ Vdc, See Figure 4)

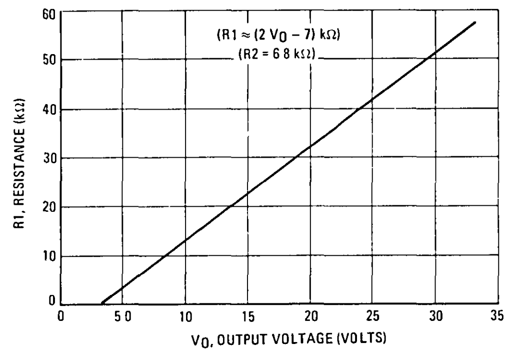


FIGURE 11 – R1 and R2 versus V_O
($2.5 \leqslant V_O \leqslant 3.5$ Vdc, See Figure 5)

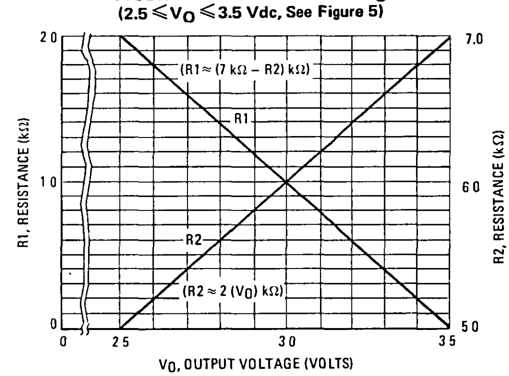
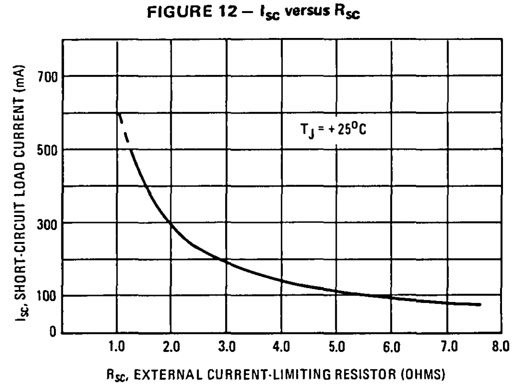


FIGURE 12 – I_{sc} versus R_{sc}



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TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_N = 0.1\ \mu F$, $C_c = 0.001\ \mu F$, $C_O = 1.0\ \mu F$, $T_C = +25^{\circ}C$,
V_{in} nom = +9.0 Vdc, V_O nom = +5.0 Vdc,
$I_L > 200$ mA for R package only.

FIGURE 13 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

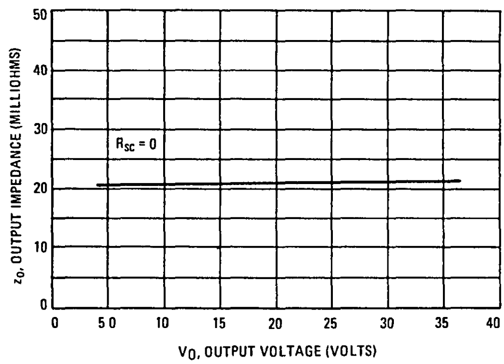


FIGURE 14 – OUTPUT IMPEDANCE versus R_{sc}

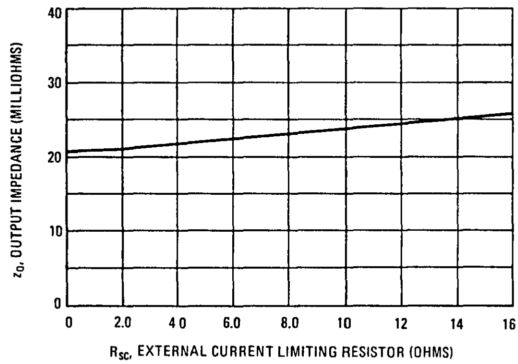


FIGURE 15 – FREQUENCY DEPENDENCE OF INPUT REGULATION, $C_O = 10\ \mu F$

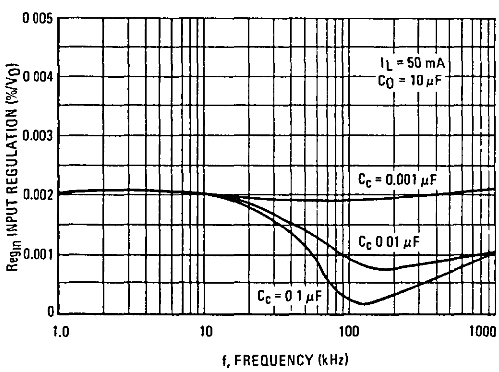


FIGURE 16 – FREQUENCY DEPENDENCE OF INPUT REGULATION, $C_O = 2.0\ \mu F$

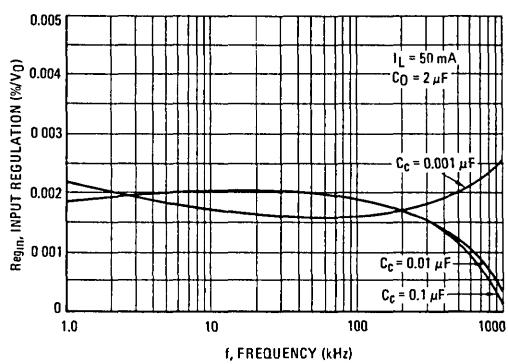


FIGURE 17 – CURRENT-LIMITING CHARACTERISTICS

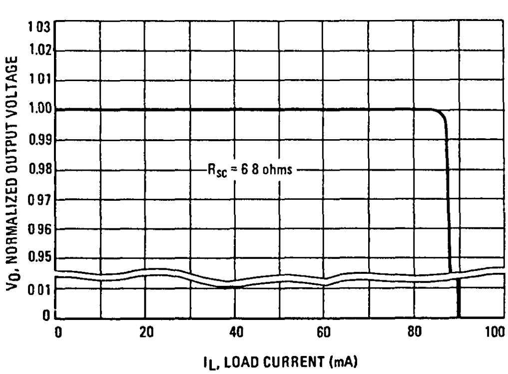
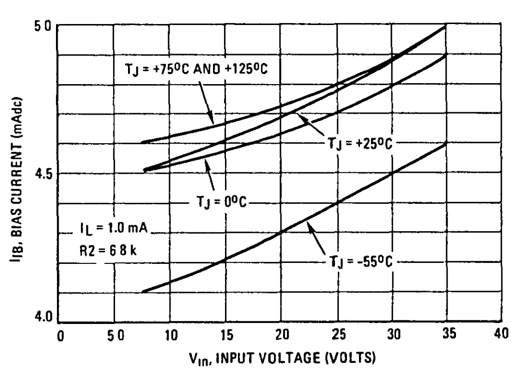


FIGURE 18 – BIAS CURRENT versus INPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted: C_N = 0.1 μF, C_c = 0.001 μF, C_O = 1.0 μF, T_C = +25°C,
V_{in} nom = +9.0 Vdc, V_O nom = +5.0 Vdc,
I_L > 200 mA for R package only.

FIGURE 19 – EFFECT OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

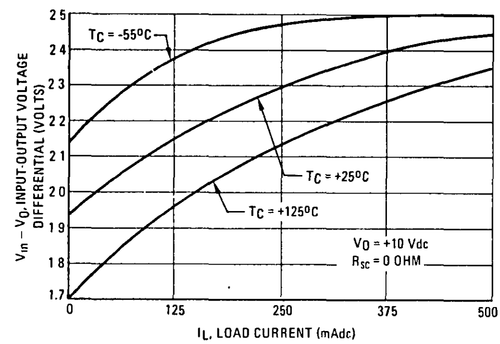


FIGURE 20 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

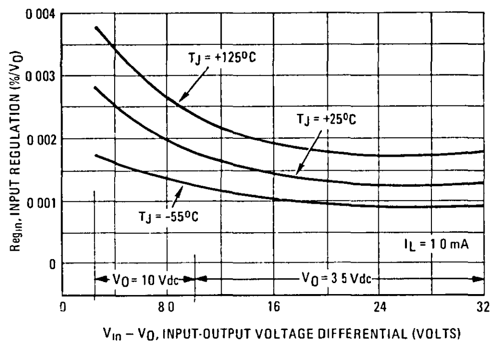


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FIGURE 21 – INPUT TRANSIENT RESPONSE

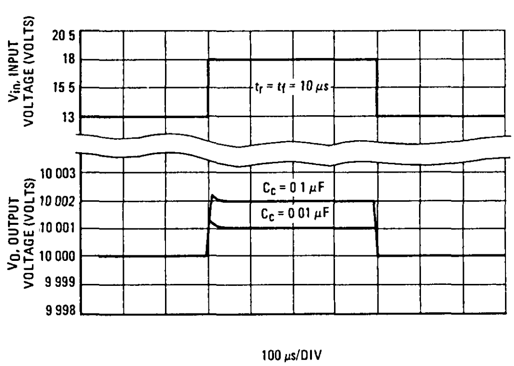


FIGURE 22 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

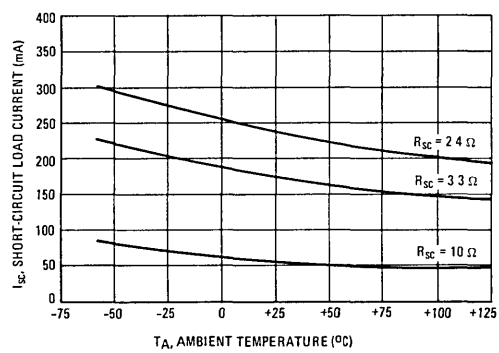


FIGURE 23 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, C_O = 10 μF

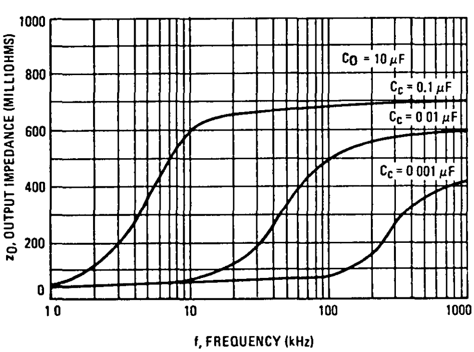
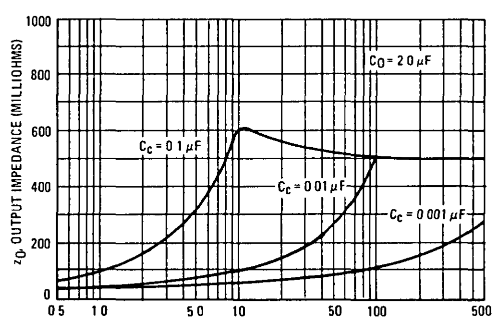


FIGURE 24 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, C_O = 2.0 μF



OPERATIONS AND APPLICATIONS

This section describes the operation and design of the MC1569 positive voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE

4

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 25, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 26. The gain-determining resistors may be external, enabling a wide range of output voltages. This is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1569) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1569 positive-voltage regulator.

FIGURE 25 – SERIES VOLTAGE REGULATOR

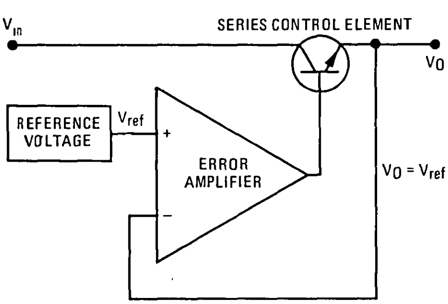


FIGURE 26 – THE "REGULATOR-WITHIN-A-REGULATOR" APPROACH

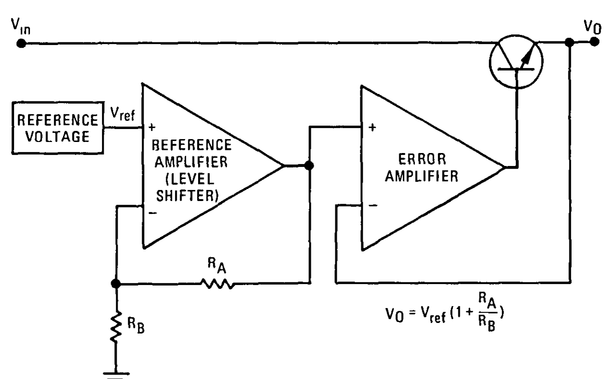
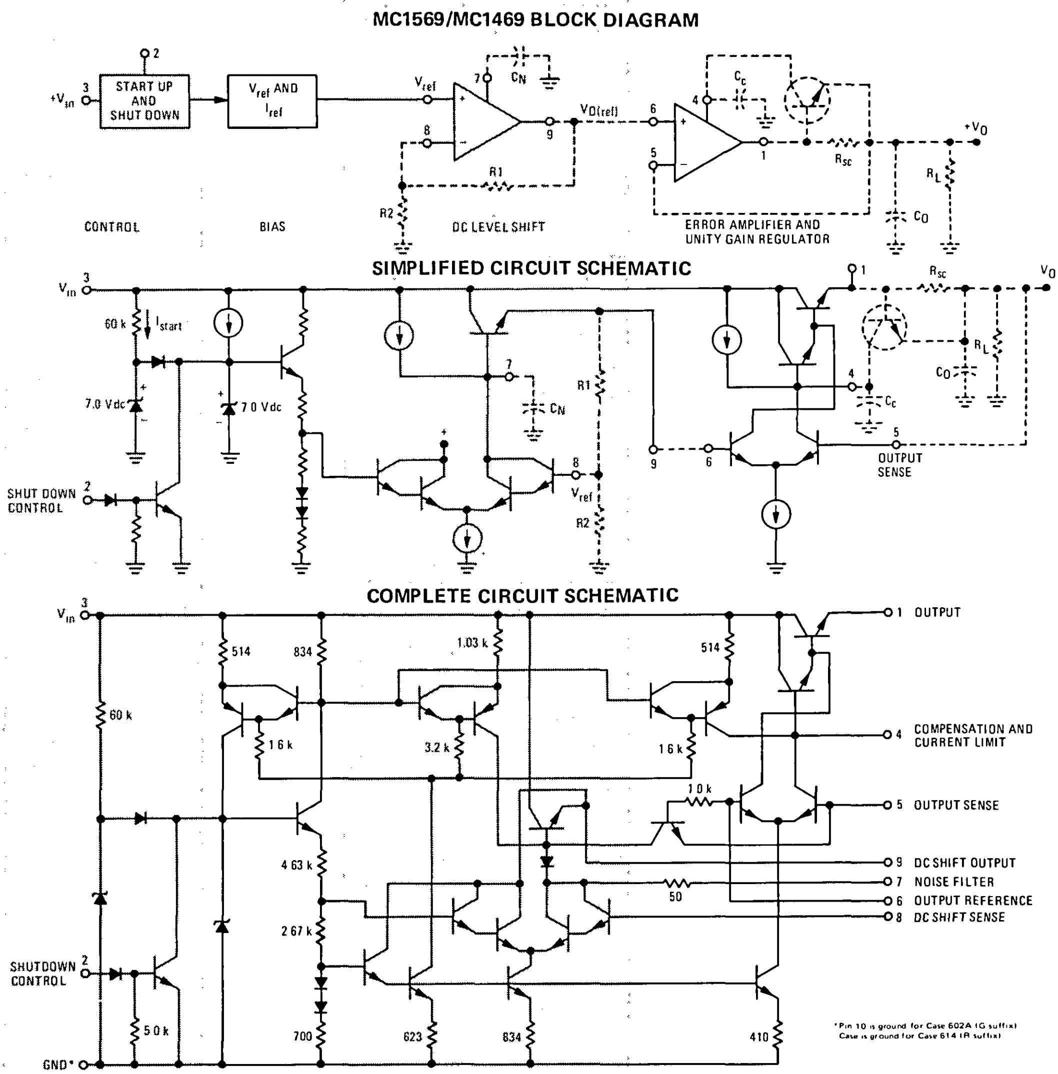


FIGURE 27
(Recommended External Circuitry is Depicted With Dotted Lines.)



MC1569 Operation

Figure 27 shows the MC1569 Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

The shutdown control consists of an NPN transistor across the reference zener diode. When this transistor is turned "ON", via pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to $V_{in}/60\ k\Omega$ or 500 μA for a 30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately 3.5 Vdc with a typical temperature coefficient of 0.002 %/°C. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

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DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R1 and R2) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_N, is introduced externally into the level shift network (via pin 7) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is 0.1 μF and should have a voltage rating in excess of the desired output voltage. Smaller capacitors (0.001 μF minimum) may be used but will cause a slight increase in output noise. Larger values of C_N will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the level shift amplifier (pin 9) is fed to the noninverting input (pin 6) of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (pin 5) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{SC}, is connected in the emitter of this transistor to sample the full load current. By placing an external low-level NPN transistor across R_{SC} as shown in Figure 27, output current can be limited to a predetermined value:

$$I_L\ max \approx \frac{0.6}{R_{SC}} \text{ or } R_{SC} = \frac{0.6}{I_L\ max}$$

where I_L max is the maximum load current (amperes) and R_{SC} is the value of the current limiting resistor (ohms).

Stability and Compensation

As has been seen, the MC1569 employs two amplifiers, each using negative feedback. This implies the possibility of instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (pin 4) and ground. The recommended value of 0.001 μF will insure stability and still provide acceptable transient response (see Figure 28, A and B). It is also necessary to use an output capacitor, C_O (typically 1.0 μF) from the output, V_O, to ground. When an external transistor is used to boost the current, C_O = 1.0 μF is also recommended (see Figure 2).

FIGURE 28A – LOAD TRANSIENT RESPONSE

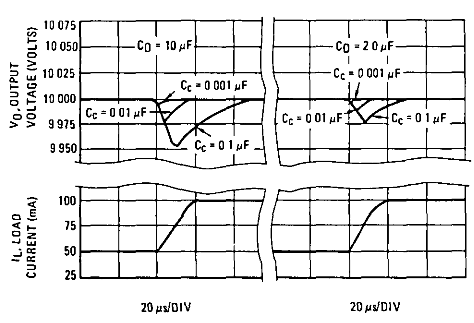
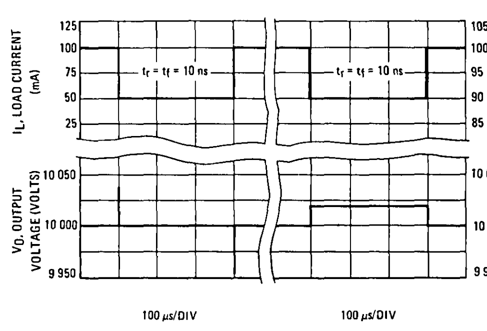


FIGURE 28B – LOAD TRANSIENT RESPONSE



TYPICAL NPN CURRENT BOOST CONNECTIONS

FIGURE 29A – 5 VOLT 5-AMPERE REGULATOR

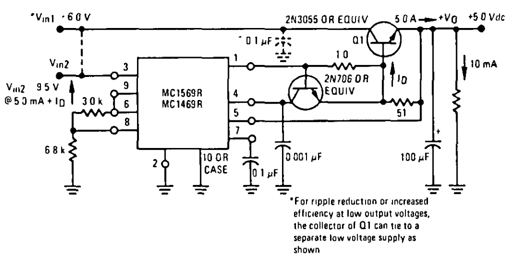


FIGURE 29B – 5-VOLT 5-AMPERE REGULATOR

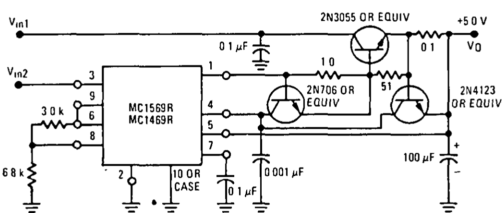
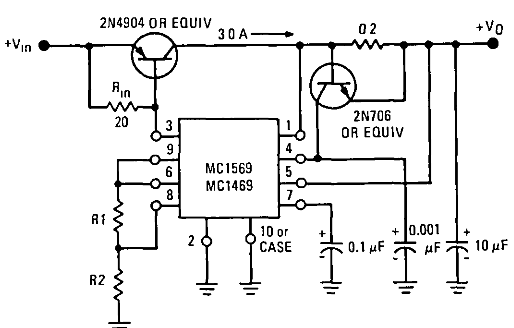


FIGURE 30 – PNP CURRENT BOOST CONNECTION



NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 3 or 29 are recommended. The transistor shown in Figure 29A, the 2N3055 can supply currents to 5.0 amperes (subject, of course, to the safe area limitations). To improve the efficiency of the NPN boost configuration, particularly for small output voltages, the circuit of Figure 29 is recommended. An auxiliary 9.5-volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 5.0 ampere regulator of Figure 29 this represents a savings of 17.5 watts when compared with operating the regulator from the single 9.5 V supply. It can supply current to 5.0 amperes while requiring an input voltage to the collector of the pass transistor of 6.0 volts minimum. The pass transistor is limited to 5.0 amperes by the added short-circuit current network in its emitter (R_{SC}), (Figure 29B).

PNP CURRENT BOOSTING

A typical PNP current boost circuit is shown in Figure 30. Voltages from 2.5 Vdc to 37 Vdc and currents of many amperes can be obtained with this circuit.

Since the PNP transistor must not be turned on by the MC1569 bias current (I_{IB}) the resistor R_{in} must meet the following condition

$$R_{in} < \frac{V_{BE}}{I_{IB}}$$

where V_{BE} is the base-to-emitter voltage required to turn on the PNP pass transistor, (typically 0.6 Vdc for silicon and 0.2 Vdc for germanium).

For germanium pass transistors, a silicon diode may be placed in series with the emitter to provide an additional voltage drop. This allows a larger value of R_{in} than would be possible if the diode were omitted. The diode will, however, be required to carry the maximum load current.

SELF-OSCILLATING SWITCHING REGULATOR

In all of the current boosting circuits shown thus far it has been assumed that the input-output voltage differential can be minimized to obtain maximum efficiency in both the external pass element as well as the MC1569. This may not be possible in applications where only a single supply voltage is available and high current levels preclude zener diode pre-regulating approaches. In such applications a switching-mode voltage regulator is highly desirable since the pass device is either ON or OFF. The theoretical efficiency of an ideal switching regulator is 100%. Realizable efficiencies of 90% are within the realm of possibility thus obviating the need for large power dissipating components. The output voltage will contain a ripple component; however, this can be made quite small if the switching frequency is made relatively high so filtering techniques are effective. Figure 31 shows a functional diagram for a self-oscillating voltage regulator. The comparator-driver will sense the voltage across the inductor, this voltage being related to the load current, I_L, by

$$L \frac{dI_L}{dt} = V.$$

For a first approximation this can be assumed to be a linear relationship.

Initially, V_O will be low and Q1 will be ON. The voltage at the non-inverting input will approach $\beta_1 V_{in}$, when:

$$\beta_1 V_{in} = \frac{V_{ref} R_a}{R_a + R_b} + \frac{V_c R_b}{R_a + R_b}.$$

When this output voltage is reached the comparator will switch, turning Q1 OFF. The diode, CR1, will now become forward biased and will supply a path for the inductor current. This current and the sense voltage will start to decrease until the output voltage reaches

$$\beta_2 V_{in} = \frac{V_{ref} R_a}{R_a + R_b}$$

where the comparator will again switch turning Q1 ON, and the cycle repeats. Thus the output voltage is approximately V_{ref} plus a ripple component.

The frequency of oscillation can be shown to be

$$f = \frac{V_O (V_{in} - V_O)}{L V_C\, I(max) - I_O)} \qquad (1)$$

where

I (max) = The maximum value of inductor current

I_O = The minimum inductor current.

Normally this frequency will be in the range of approximately 2 kHz to 6 kHz. In this range, inductor values can be small and are compatible with the switching times of the pass transistor and diode. The switching time of the comparator is quite fast since positive feedback aids both turn-on and turn-off times. The limiting factors are the diode and pass transistor rise and fall times which should be quite fast or efficiency will suffer.

Figure 32 shows a self oscillating switching regulator which in many respects is similar to the PNP current boost previously discussed. The 6.8 kΩ resistor in conjunction with R1 sets the reference voltage, V_{ref}. Q1 and CR1 are selected for fast switching times as well as the necessary power dissipation ratings. Since a linear inductor is assumed, the inductor cannot be allowed to saturate at maximum load currents and should be chosen accordingly. If core saturation does occur, peak transistor and diode currents will be large and power dissipation will increase.

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FIGURE 31 – BASIC SELF-OSCILLATING SWITCHING REGULATOR

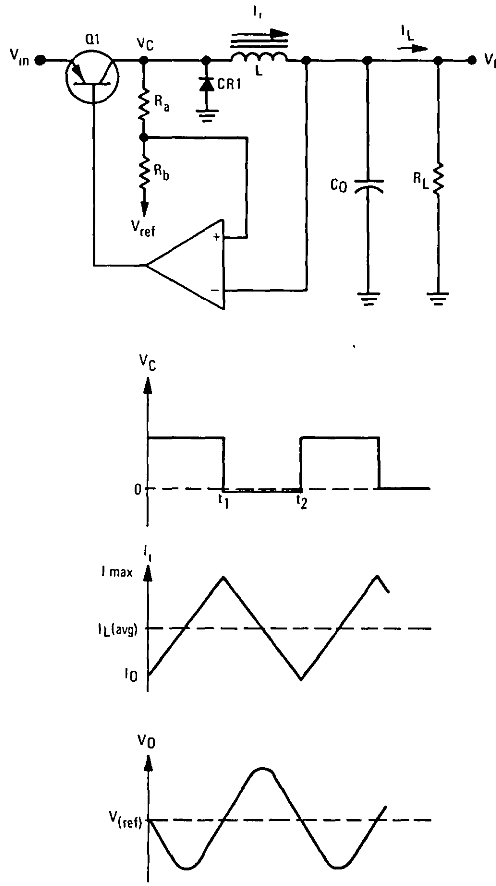
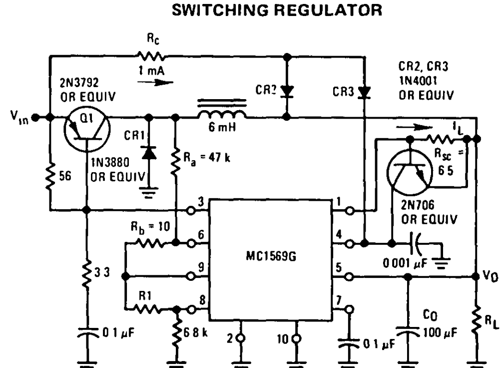


FIGURE 32 – MC1569 SELF-OSCILLATING SWITCHING REGULATOR



As a design center is required for a practical circuit, assume the following requirements:

$V_{in} = +28$ Volts

$V_O = +10$ Volts

$\Delta V_O = 50$ mV

$f \cong 5$ kHz

$I(max) = 1.125$ A

$I_O = 1$ A

$$\Delta V \approx V_{in} \frac{R_b}{R_a}. \quad (2)$$

Using Equation (1), the inductor value can be found:

$$L = \frac{(28-10)}{2(1.125-1)} \frac{10}{28} \left(\frac{1}{5 \times 10^3}\right)$$

$$\approx 7 \text{ mH}.$$

For the test circuit, a value of 6 mH was selected. Using for a first approximation

$$C_O = \frac{(V_{in} - V_O)(V_O)}{8L f^2 V_{in} (\Delta V)}$$

$$= \frac{(28 - 10)10}{8(7 \times 10^{-3})(5 \times 10^3)^2 (28)(50 \times 10^{-3})}$$

$$\approx 95\ \mu F.$$

As shown, a value of 100 μF was selected. Since little current is required at pin 6, R_a can be large. Assume R_a = 47 kΩ and then use Equation (2) to determine R_b:

$$50 \times 10^{-3} = \frac{28}{47 \text{ k}\Omega} R_b$$

$$R_b = \frac{47}{28} 50 \approx 85\Omega.$$

Since the internal impedance presented by pin 9 is on the order of 60Ω, a value of R_b = 10Ω is adequate.

Diodes CR2, CR3, and R_c may be added to prevent saturation of the error amplifier to increase switching speed. When the output stage of the error amplifier approaches saturation, CR2 becomes forward biased and clamps the error amplifier. Resistor R_c should be selected to supply a total of 1 mAdc to CR2 and CR3.

To show correlation between the predicted and tested specifications the following data was obtained:

$V_{in} = +28 (\pm 1\%)$ Volts

$V_O = +10$ Volts

$\Delta V_O = 60$ mV

$f = 7$ kHz

$@ I_L = 1$ A

which checks quite well with the predicted values. R_b can be adjusted to minimize the ripple component as well as to trim the operating frequency. Also this frequency will change with varying loads as is normal with this type of circuit. Pin 2 can still be used for shut-down if so desired. R_{SC} should be set such that the ratio of load current to base drive current is 10:1 in this case $I_1 \approx 100$ mA and $R_{SC} = 6.5\Omega$.

POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1569 is driven from a floating source it is possible to use it as a negative regulator by grounding the positive output terminal. The MC1569 may also be used with the MC1563 to provide completely independent positive and negative voltage regulators with comparable performance.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 1 and 33 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (pin 6 of the MC1569) and using the other side (pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3-k ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at pin 5 will be zero. When the voltage at pin 5 equals zero, $+V_O$ must equal $|-V_O|$.

For the configuration shown in Figure 33, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown,

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is not short-circuit protected.) The −15-volt supply varies less than 0.1 mV over a zero to −300 mAdc current range and the +15-volt supply tracks this variation. The +15-volt supply varies 20 mV over the zero to +300 mAdc load current range. The +5-volt supply varies less than 5 mV for $0 \leqslant I_L \leqslant 200$ mA with the other two voltages remaining unchanged. See page 19 for additional information.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1569 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of an NPN transistor; which, if turned "ON", will turn the zener "OFF" and deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60-k-ohm start resistor (V_{in}/60 kΩ). This feature provides additional versatility in the applications of the MC1569. Various subsystems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as overheating, over-voltage, shorted output, etc.

To activate shutdown, one simply applies a potential greater than two diode drops with a current capability of 1 mA. Note that if a hard supply (i.e., +3 V) is applied directly to pin 2, the shutdown circuitry will be destroyed since there is no inherent current limiting. Maximum rating for the drive current into pin 2 is 10 mA, while 1 mA is adequate for shutdown.

FIGURE 33 – A ±15 Vdc COMPLEMENTARY TRACKING REGULATOR WITH AUXILIARY +5.0 V SUPPLY

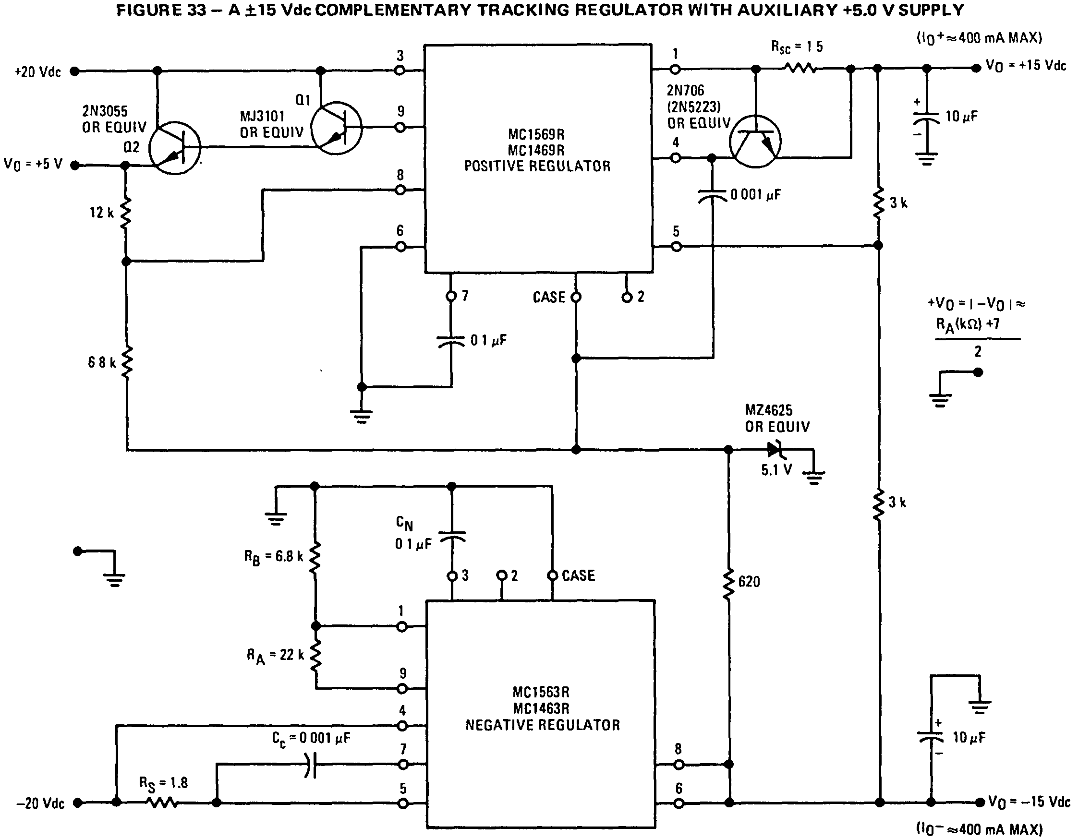

FIGURE 34 – ELECTRONIC SHUT-DOWN USING A MDTL GATE

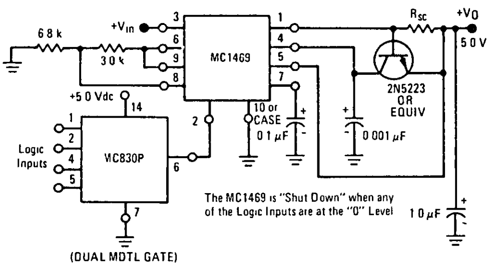

FIGURE 35 – AUTOMATIC LATCH INTO SHUT-DOWN WHEN OUTPUT IS SHORT-CIRCUITED WITH MANUAL RE-START

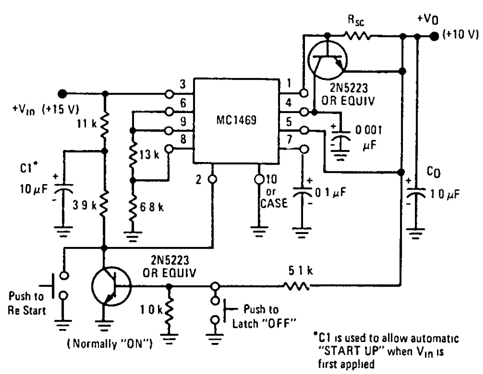

FIGURE 36 – VOLTAGE BOOSTING CIRCUIT

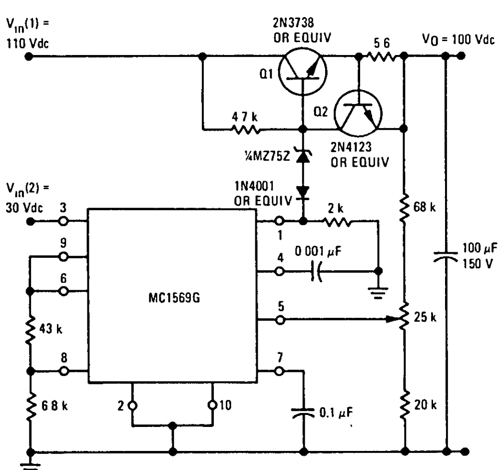

Figure 34 shows how the regulator can be controlled by a logic gate. Here, it is assumed that the regulator operates in its normal mode – as a positive regulator referenced to ground – and that the logic gate is of the saturating type, operating from a positive supply to ground. The high logic level should be greater than about 1.5 V and should source no more than 10 mA into pin 2.

The gate shown is of the MDTL type. MRTL and MTTL can also be used as long as the drive current is within safe limits (this is important when using MTTL, where the output stage uses an active pull-up).

In some cases a regulator can be designed which can handle the power dissipation resulting from normal operation but cannot safely dissipate the power resulting from a sustained short-circuit. The circuit of Figure 35 solves this problem by shutting down the regulator when the output is short-circuited.

4

VOLTAGE BOOSTING

The MC1569 has a maximum output voltage capability of 37 volts which covers the bulk of the user requirements. However, it is possible to obtain higher output voltages. One such voltage boosting circuit is shown in Figure 36.

Since high voltage NPN silicon devices are readily available, the only problem is the voltage limitations of the MC1569. This can be overcome by using voltage shift techniques to limit the voltage to 35 volts across the MC1569 while referencing to a higher output voltage.

The zener diode in the base lead of the NPN device is used to shift the output voltage of the MC1569 by approximately 75 volts to the desired high voltage level, in this case 100 volts. Another voltage shift is accomplished by the resistor divider on the output to accommodate the required 25 volt reference to the MC1569. The 2 kΩ resistor is used to bias the zener diode so the current through the 4.7 kΩ resistor can be controlled by the MC1569. The 1N4001 diode protects the MC1569 from supplying load current under short circuit conditions and Q2 serves to limit base current to Q1. For R_{SC} as shown, the short circuit current will be approximately 100 mA.

In order to use a single supply voltage, $V_{in}(2)$ can be derived from $V_{in}(1)$ with a zener diode, shunt pre-regulator.

It can be seen that loop gain has been reduced by the resistor divider and hence the closed loop bandwidth will be less. This of course will result in a more stable system, but regulator performance is degraded to some degree.

REMOTE SENSING

The MC1569 offers a remote sensing capability. This is important when the load is remote from the regulator, as the resistance of the interconnecting lines (V_O and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 37 shows how remote sensing is accomplished using both a separate sense line from pin 8 and a separate ground line from the regulator to the remote load.

AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE.

The MC1569, when used in conjunction with low TC resistors, makes an excellent reference-voltage generator. If the 3.5 volt reference voltage of the IC regulator is a satisfactory value, then pins 8 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, R1 and R2, any voltage between 3.5 Vdc and 37 Vdc can be obtained with the same low TC (see Figure 38).

THERMAL SHUTDOWN

By setting a fixed voltage at pin 2, the MC1569 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor and the diode in series with pin 2 (-3.4×10^{-3}V/°C). By setting 1.0 Vdc externally at pin 2, the regulator will shutdown when the chip temperature reaches approximately +140°C. Figure 39 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

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FIGURE 37 – REMOTE SENSING CIRCUIT

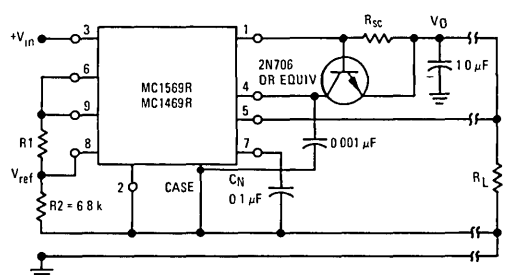


FIGURE 38 – AN ADJUSTABLE "ZERO-TC" VOLTAGE SOURCE

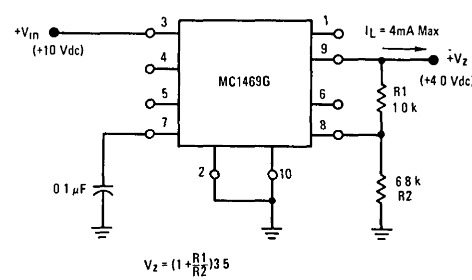
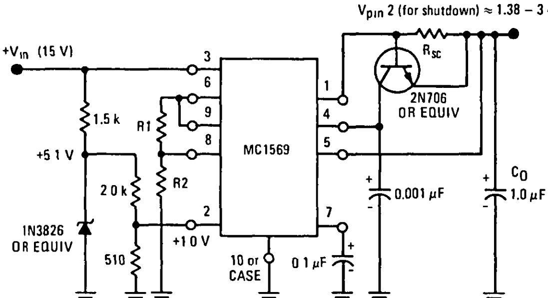


FIGURE 39 – JUNCTION TEMPERATURE LIMITING SHUTDOWN CIRCUIT

FIGURE 39A – USING A ZERO TC REFERENCE

FIGURE 39B – USING A T_A REFERENCE

$V_{pin\,2}$ (for shutdown) ≈ $1.38 - 3.4 \times 10^{-3} (T_J - 25°C)$



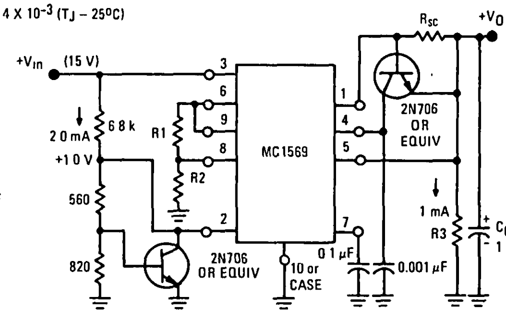


FIGURE 40 – THERMAL SHUTDOWN WHEN USING EXTERNAL PASS TRANSISTORS

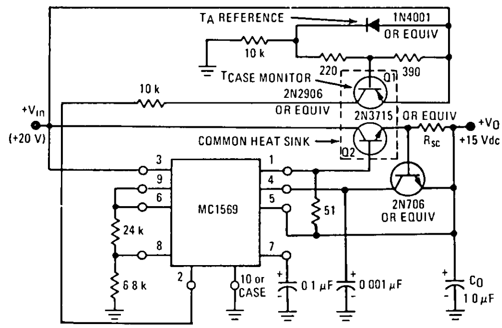
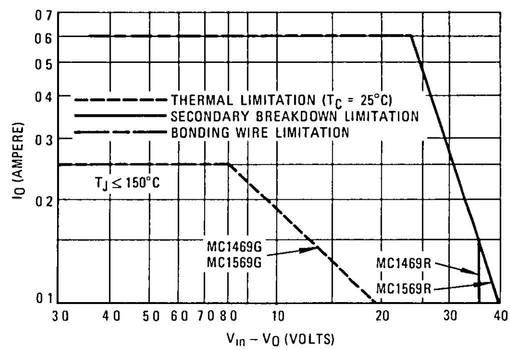


FIGURE 41 – DC SAFE OPERATING AREA



In the case where an external pass transistor is employed, its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 40. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application, the designer must use caution not to exceed the specified maximum junction temperature (+150°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current. Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 41).

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically –0.06%/watt for the MC1569. For an example of the relative magnitudes of these effects, consider the following conditions:

Given MC1569

with V_{in} = 10 Vdc

V_O = 5 Vdc

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

and I_L = 100 mA to 200 mA

(ΔI_L = 100 mA)

assume $T_A = +25°C$

TO-66 Case with heatsink

assume $\theta_{CS} = 0.2°C/W$

and $\theta_{SA} = 2°C/W$

$\theta_{JC} = 7.15°C/W$ (from maximum ratings table)

It is desired to find the ΔV_O which results from this ΔI_L. Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_O due to ΔT_J

$$\Delta V_O = (V_O)(\Delta P_D)(TCV_O)(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

OR

$$\Delta V_O = (5V)(5\ V \times 0.1A)(\pm 0.002\%/°C)(9.35°C/W)$$

$$\Delta V_O \approx \pm 0.5\ mV$$

2. ΔV_O due to z_o

$$|\Delta V_O| = (-z_o)(I_L)$$

$$|\Delta V_O| = -(2 \times 10^{-2})(10^{-1}) = -2\ mV$$

3. ΔV_O due to gradient coefficient, GCV_O

$$|\Delta V_O| = (GCV_O)(V_O)(\Delta P_D)$$

$$|\Delta V_O| = (-6 \times 10^{-4}/W)(5\ volts)(5 \times 10^{-1}W)$$

$$|\Delta V_O| = -1.6\ mV$$

Therefore the total ΔV_O is given by

$$|\Delta V_O\ total| = \pm 0.5 - 2.0 - 1.6\ mV$$

OR

$$-4.1\ mV \leqslant |V_O\ total| \leqslant -3.1\ mV$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT

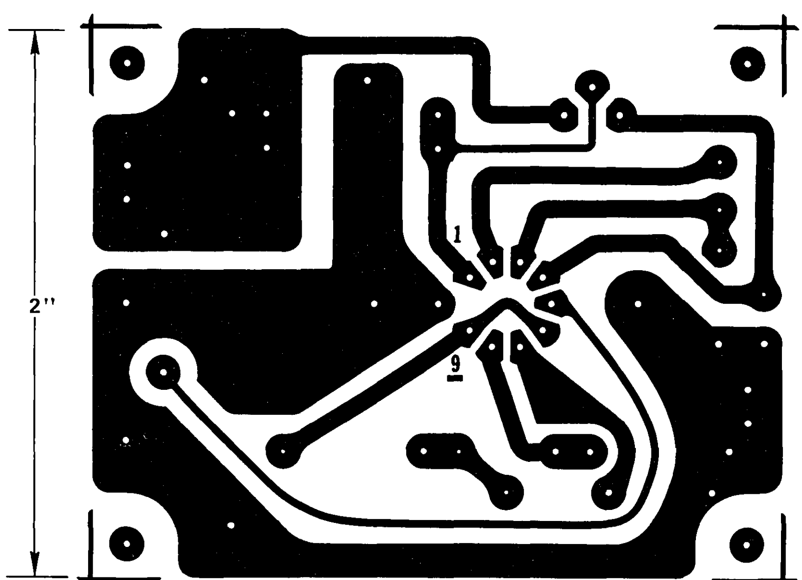
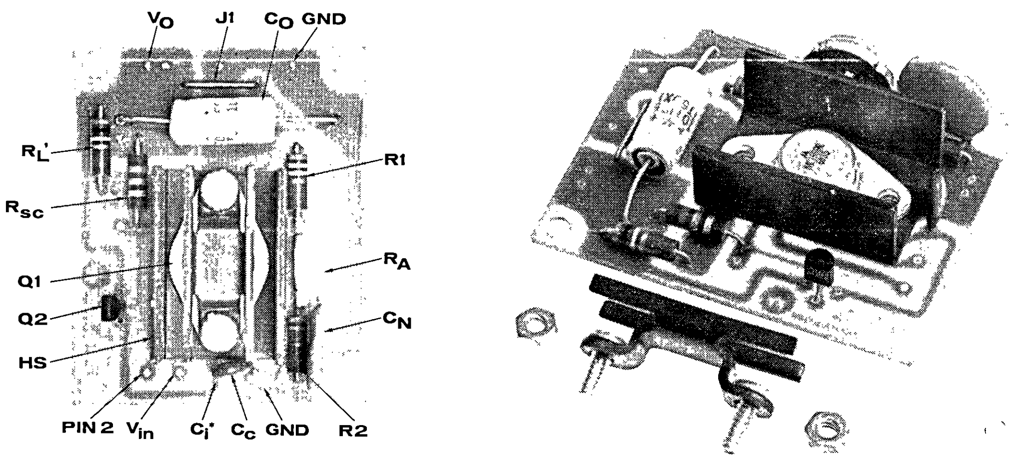
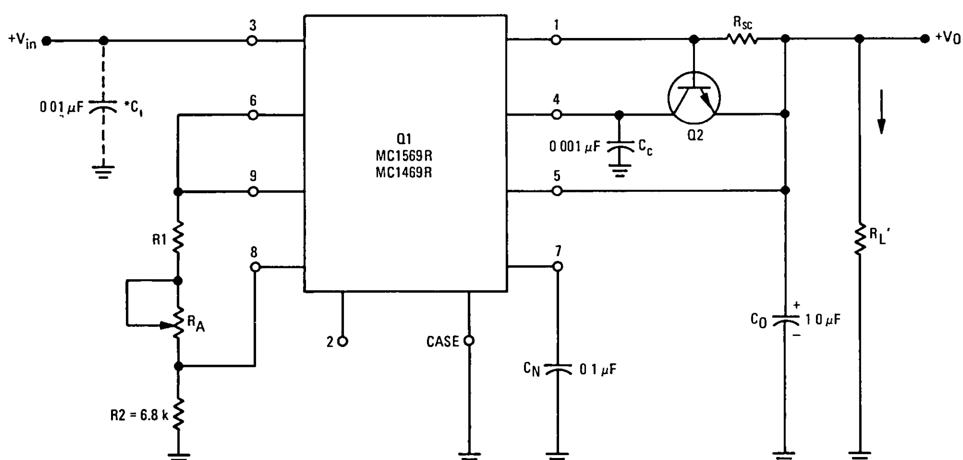


FIGURE 42 – LOCATION OF COMPONENTS



*Ci not shown

FIGURE 43 – CIRCUIT SCHEMATIC FOR PRINTED CIRCUIT BOARD (Pg. 17)
$3.5\ V \leq V_O \leq 37\ V,\ 1\ mA \leq I_L \leq 500\ mA$



Select R1 to give desired V_O. $R1 \approx (2 V_O - 7)$ kΩ

*C_i – May be required if long input leads are used.

PARTS LIST

Component	Value	Description
R1 R2	Select 6.8 k	1/4 or 1/2 watt carbon
*R_A	Select	IRC Model X-201 Mallory Model MTC-1 or equivalent
R_{sc}	Select	1/2 watt carbon
*R_L'	Select	For minimum current of 1 mAdc
C_O	1.0 μF	Sprague 1500 Series, Dickson D10C series or equivalent
C_N C_c *C_I	0.1 μF 0.001 μF 0.01 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or equivalent
Q1 Q2	MC1569R or MC1469R 2N5223, 2N706, or equivalent	
*HS	–	Heatsink Thermalloy #6168B
*Socket	(Not Shown)	Robinson Nugent #0001306 Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1
PC Board	–	Circuit Dot, Inc. #PC1113 1155 W. 23rd St., Tempe, Ariz. 85281
*Optional		

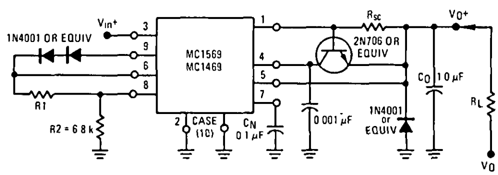
LATCH-UP

Latch-up of these and other regulators can occur if:

1. There are plus and minus voltages available
2. A load exists between V_O^+ and V_O^- (This "common load" may be something inconspicuous – e.g. an operational amplifier. Nearly everyone who uses + and – voltages will have a common load from V_{CC} to V_{EE}.)
3. V_{in}^+ and V_{in}^- are not applied at the same time.

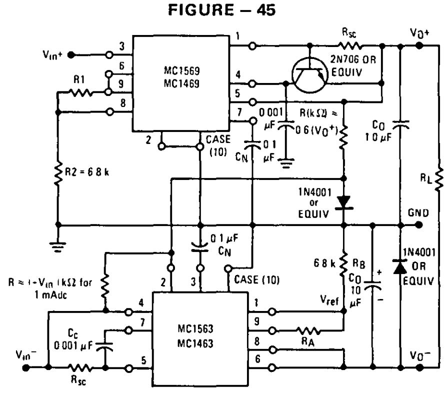
The above conditions result in one of the two outputs becoming reverse-biased which prevents the regulator from turning ON. Latch-up can be prevented by the circuit configurations shown in Figures 44 and 45.

FIGURE – 44



Note This configuration increases minimum input output differential voltage by ≈ 0.7 V

FIGURE – 45



MC1723
MC1723C

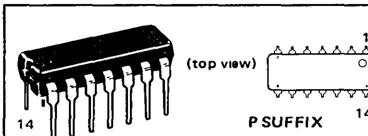
MONOLITHIC VOLTAGE REGULATOR

The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +70°C)

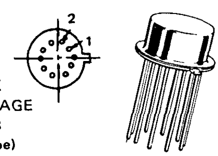
- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

VOLTAGE REGULATOR

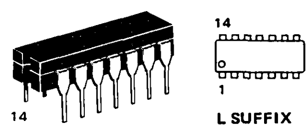
SILICON
MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646



(top view)
G SUFFIX
METAL PACKAGE
CASE 603
(TO-100 Type)

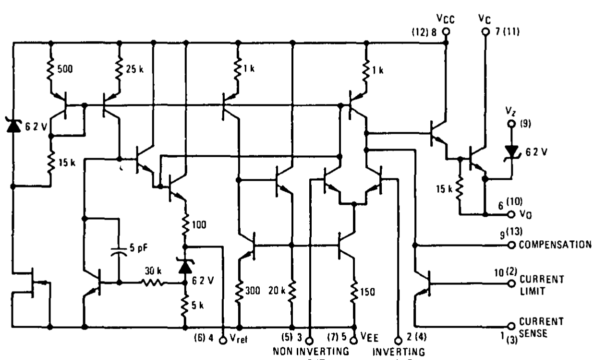


L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

ORDERING INFORMATION

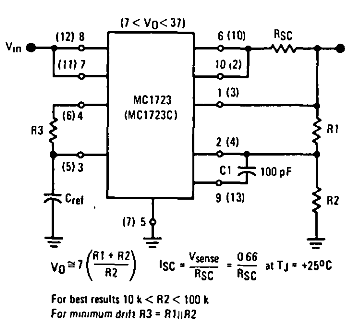
Device	Alternate	Temperature Range	Package
MC1723CG	LM723CH, μA723HC	0°C to 70°C	Metal Can
MC1723CL	LM723CJ, μA723DC	0°C to +70°C	Ceramic DIP
MC1723CP	LM723CN, μA723PC	0°C to +70°C	Plastic DIP
MC1723G	–	-55°C to +125°C	Metal Can
MC1723L	–	-55°C to +125°C	Ceramic DIP

FIGURE 1 – CIRCUIT SCHEMATIC



PIN NUMBERS ADJACENT TO TERMINALS ARE FOR THE METAL PACKAGE
PIN NUMBERS IN PARENTHESIS ARE FOR DUAL IN LINE PACKAGES

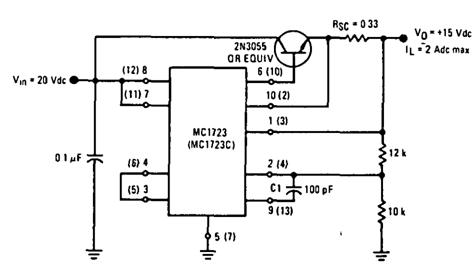
FIGURE 2 – TYPICAL CIRCUIT CONNECTION



$V_O \cong 7\left(\frac{R1 + R2}{R2}\right)$ $I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at $T_J = +25°C$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1||R2

FIGURE 3 – TYPICAL NPN CURRENT BOOST CONNECTION



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Pulse Voltage from V_{CC} to V_{EE} (50 ms)	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V_{CC} to V_{EE}	V_{in}	40	Vdc
Input-Output Voltage Differential	$V_{in} - V_O$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Current from V_z	I_z	25	mA
Voltage Between Non-Inverting Input and V_{EE}	V_{ie}	8.0	Vdc
Differential Input Voltage	V_{id}	±5.0	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	1.25	W
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Metal Package			
T_A = +25°C	P_D	1.0	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	6.6	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	°C/W
T_C = +25°C	P_D	2.1	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	14	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	35	°C/W
Dual In-Line Ceramic Package	P_D	1.5	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}		°C
Metal Package		-65 to +150	
Dual In-Line Ceramic and Ceramic Flat Packages		-65 to +175	
Operating Ambient Temperature Range	T_A		°C
MC1723C		0 to +70	
MC1723		-55 to +125	

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 2)

Characteristic	Symbol	MC1723			MC1723C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	9.5	–	40	9.5	–	40	Vdc
Output Voltage Range	V_O	2.0	–	37	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_O$	3.0	–	38	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{IB}	–	2.3	3.5	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_N							µV(RMS)
C_{ref} = 0		–	20	–	–	20	–	
C_{ref} = 5.0 µF		–	2.5	–	–	2.5	–	
Average Temperature Coefficient of Output Voltage (T_{low} ① < T_A < T_{high} ②)	TCV_O	–	0.002	0.015	–	0.003	0.015	%/°C
Line Regulation	Reg_{in}							%V_O
(T_A = +25°C) 12 V < V_{in} < 15 V		–	0.01	0.1	–	0.01	0.1	
(T_A = +25°C) 12 V ≤ V_{in} < 40 V		–	0.02	0.2	–	0.1	0.5	
(T_{low} ① < T_A < T_{high} ②) 12 V < V_{in} < 15 V		–	–	0.3	–	–	0.3	
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_{load}							%V_O
T_A = +25°C		–	0.03	0.15	–	0.03	0.2	
T_{low} ① < T_A < T_{high} ②		–	–	0.6	–	–	0.6	
Ripple Rejection (f = 50 Hz to 10 kHz)	Rej_R							dB
C_{ref} = 0		–	74	–	–	74	–	
C_{ref} = 5.0 µF		–	86	–	–	86	–	
Short Circuit Current Limit (R_{SC} = 10 Ω, V_O = 0)	I_{SC}	–	65	–	–	65	–	mAdc
Long Term Stability	$\Delta V_O/\Delta t$	–	0.1	–	–	0.1	–	%/1000 Hr

① T_{low} = 0°C for MC1723C
= -55°C for MC1723

② T_{high} = +70° C for MC1723C
= +125°C for MC1723

TYPICAL CHARACTERISTICS

(V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

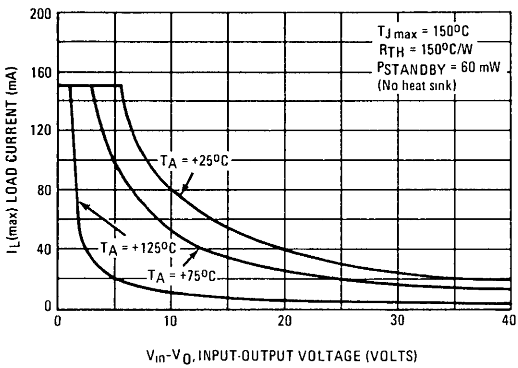

FIGURE 5 – LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

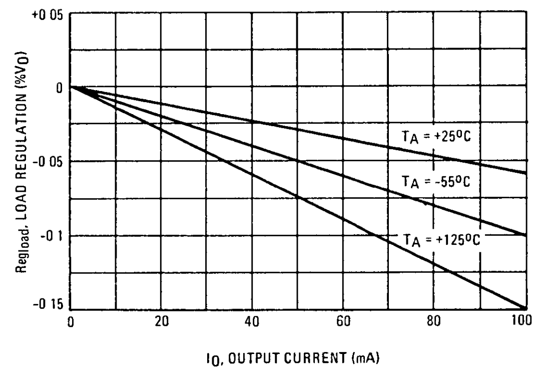

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FIGURE 6 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

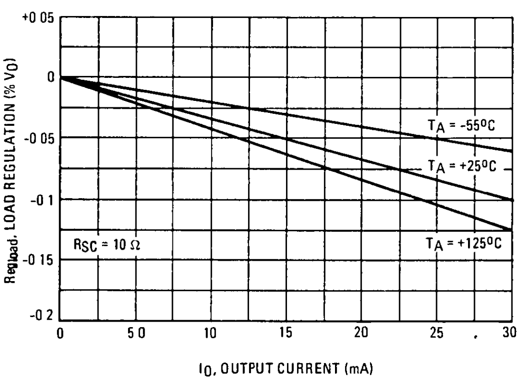


FIGURE 7 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

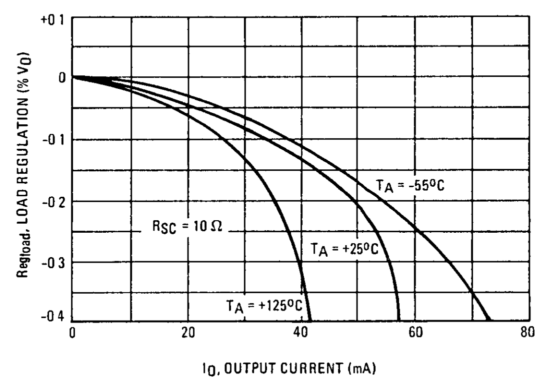


FIGURE 8 – CURRENT LIMITING CHARACTERISTICS

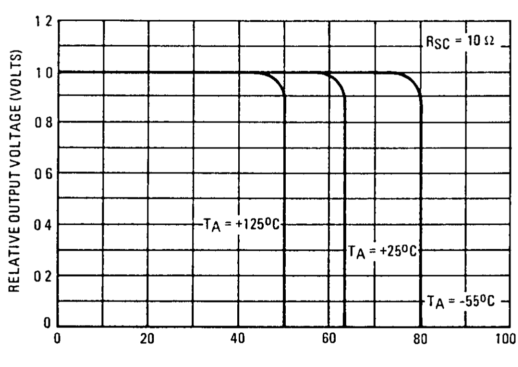
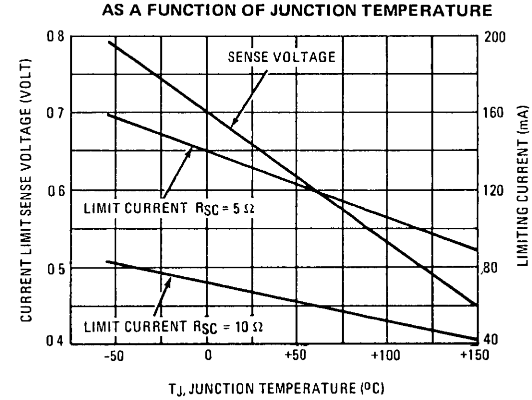


FIGURE 9 – CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 — LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

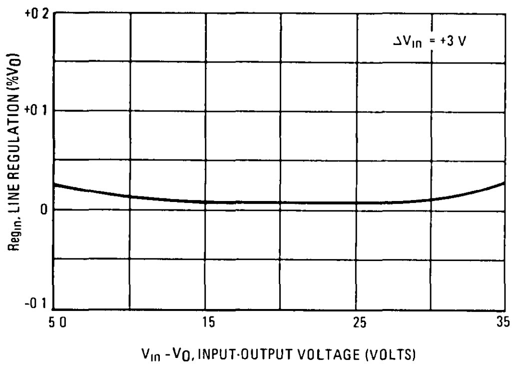


FIGURE 11 — LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

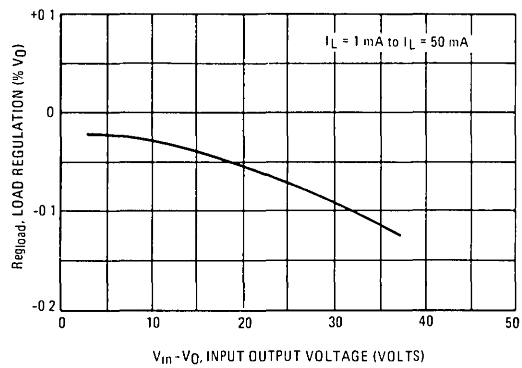


FIGURE 12 — STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

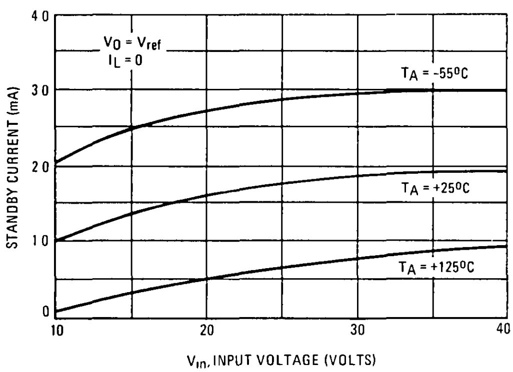


FIGURE 13 — LINE TRANSIENT RESPONSE

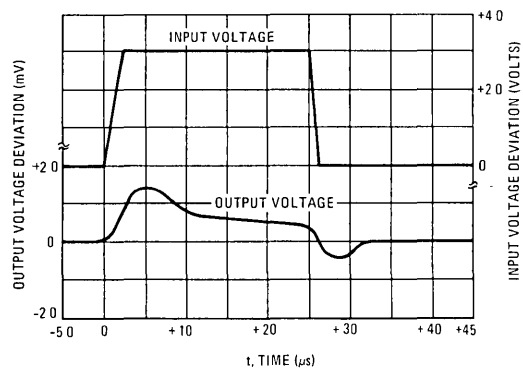


FIGURE 14 — LOAD TRANSIENT RESPONSE

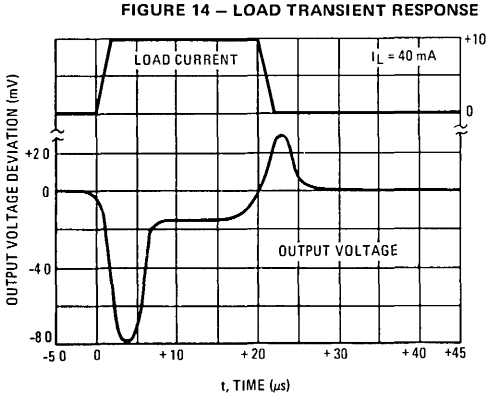
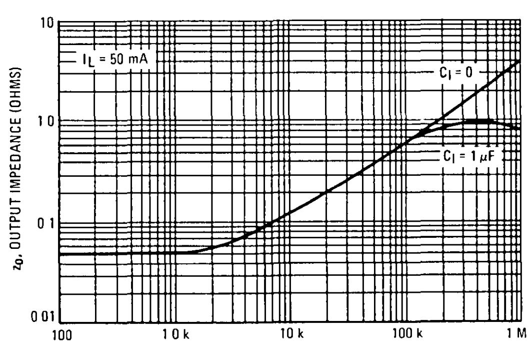


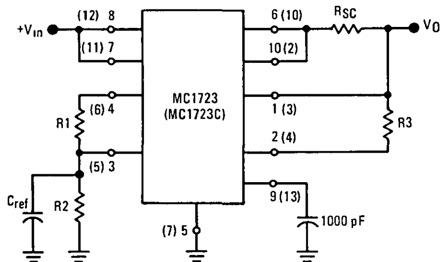
FIGURE 15 — OUTPUT IMPEDANCE AS FUNCTION OF FREQUENCY



TYPICAL APPLICATIONS

Pin numbers adjacent to terminals are for the metal package; pin numbers in parenthesis are for the dual in-line packages.

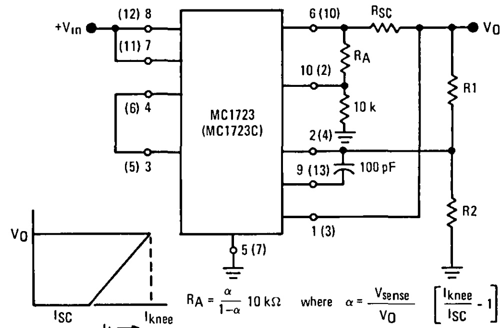
FIGURE 16 – TYPICAL CONNECTION FOR $2 < V_O < 7$



$V_O \cong 7\left[\frac{R2}{R1+R2}\right]$ $I_{SC} = \frac{V_{sense}}{R_{SC}} \cong \frac{0.66}{R_{SC}}$ at $T_J = +25^{\circ}C$

For best results 10 k < R1 + R2 < 100 k.
For minimum drift R3 = R1||R2

FIGURE 17 – MC1723,C FOLDBACK CONNECTION



$R_A = \frac{\alpha}{1-\alpha}\,10\,k\Omega$ where $\alpha = \frac{V_{sense}}{V_O}\left[\frac{I_{knee}}{I_{SC}} - 1\right]$

$R_{SC} = \frac{V_{sense}}{(1-\alpha)\,I_{SC}}$

FIGURE 18 – +5 V, 1-AMPERE SWITCHING REGULATOR

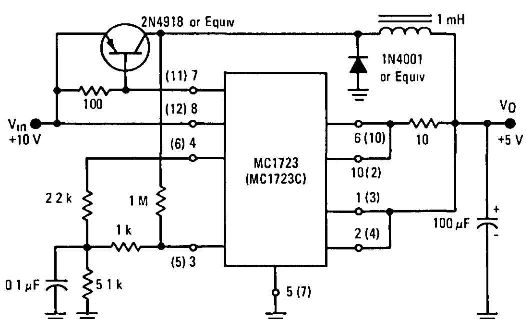


FIGURE 19 – +5 V, 1-AMPERE HIGH EFFICIENCY REGULATOR

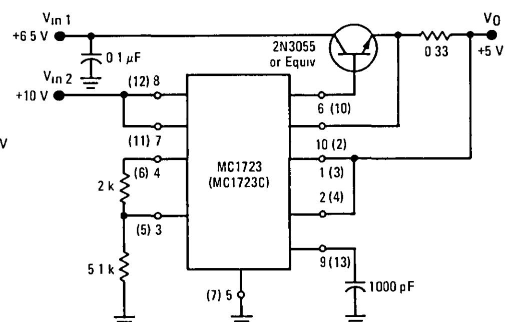


FIGURE 20 – +15 V, 1-AMPERE REGULATOR WITH REMOTE SENSE

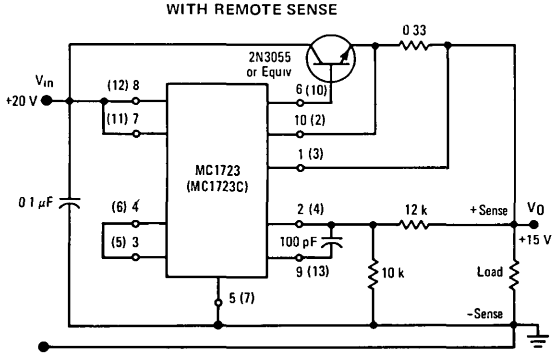
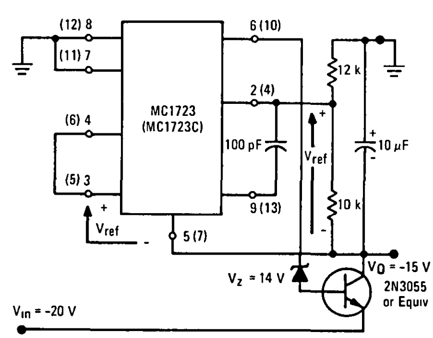


FIGURE 21 – -15 V NEGATIVE REGULATOR



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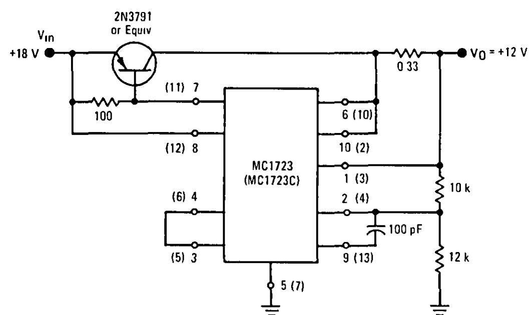
TYPICAL APPLICATIONS (continued)

FIGURE 22 – +12 V, 1-AMPERE REGULATOR USING PNP CURRENT BOOST



4

MC3420
MC3520

SWITCHMODE REGULATOR CONTROL CIRCUIT

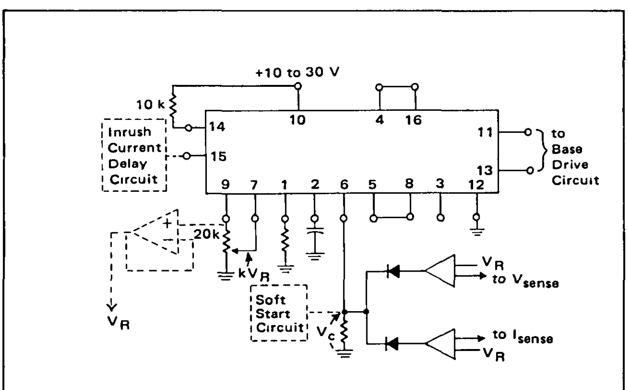
The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

These devices are designed to supply the pulse width modulated drive to the base of two external power transistors. Other applications where these devices can be used are in transformerless voltage doublers, transformer coupled dc-to-dc converters and other power control functions.

The MC3520 is specified over the military operating range of -55°C to +125°C. The MC3420 is specified from 0°C to +70°C.

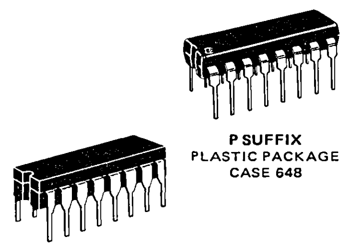
- Includes Symmetrical Oscillator
- On Chip Pulse Width Modulator, Voltage Reference, Dead Time Comparator, and Phase Splitter
- Output Frequency Adjustable (2 kHz to 100 kHz)
- Inhibit and Symmetry Correction Inputs Available
- Controlled Start-Up
- Frequency and Dead Time are Independently Adjustable (0% to 100%)
- Can be Slaved to Other MC3420s
- Open Collector Outputs
- Output Capability 50 mA (Max.)
- On Chip Protection Against Double Pulsing of Same Output During Load Transient Condition

FIGURE 1—TYPICAL APPLICATION



SWITCHMODE REGULATOR CONTROL CIRCUIT

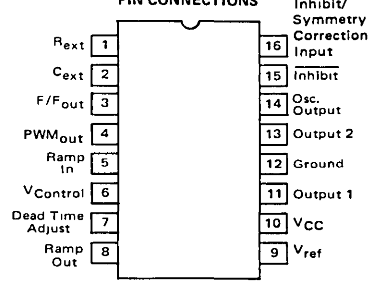
SILICON MONOLITHIC INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3420P	0 to +70°C	Plastic DIP
MC3420L	0 to +70°C	Ceramic DIP
MC3520L	-55 to +125°C	Ceramic DIP

4

MAXIMUM RATINGS

Rating	Symbol	MC3520	MC3420	Unit
Power Supply Voltage	V_{CC}	30		V
Output Voltage (pins 11 and 13)	V_{out}	40		V
Oscillator Output Voltage (pin 14)	V_{14}	30		V
Voltage at pin 4	V_4	2.0		V
Voltage at pins 3 and 8	V_3, V_8	5.0		V
Voltage at pin 5	V_5	7.0		V
Power Dissipation	P_D	See Thermal Information		
Operating Junction Temperature	T_J			°C
Plastic Package		–	125	
Ceramic Package		150	150	
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 to 30 V, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	MC3520 Min	MC3520 Typ	MC3520 Max	MC3420 Min	MC3420 Typ	MC3420 Max	Unit
REFERENCE SECTION									
Reference Voltage (I_{ref} = 400 μA)	5	V_{ref}	7.6	7.8	8.0	7.4	7.8	8.2	V
Temperature Coefficient of Reference Voltage (V_{CC} = 15 V, I_{ref} = 400 μA)	5	TCV_{ref}	–	0.008	0.03	–	0.008	0.03	%/°C
Input Regulation of Reference Voltage	5	$Reg_{(in)}$							mV/V
(I_{ref} = 400 μA)			–	3.0	7.5	–	4.0	7.5	
(I_{ref} = 1.0 mA)			–	5.0	–	–	5.0	–	
DC SUPPLY SECTION									
Supply Voltage	5	V_{in}	10	–	30	10	–	30	V
Supply Current (R_{ext} = 10 kΩ, excluding load and current and reference current)	5	I_D	–	–	16	–	–	22	mA
OSCILLATOR SECTION									
Line Frequency Stability	5								
(f = 20 kHz)		Δf	–	–	3.0	–	–	5.0	%
(f = 20 kHz, V_{CC} = 15 V, T_{low} to T_{high})		Δf	–	0.03	–	–	0.04	–	%/°C
Maximum Output Frequency (V_{CC} = 15 V)	6	f_{max}	100	200	–	100	200	–	kHz
Minimum Output Frequency (V_{CC} = 15 V)	6	f_{min}	–	2.0	5.0	–	2.0	5.0	kHz
Oscillator Output Saturation Voltage ($I_{14\ sink}$ = 5.0 mA)	11	$V_{osc(sat)}$	–	0.2	0.5	–	0.2	0.5	V
OUTPUT SECTION									
Output Saturation Voltage	7	$V_{CE(sat)}$							V
(I_L = 40 mA, T_{high} to T_{low})			–	0.33	0.5	–	0.33	0.5	
(I_L = 25 mA, T_{high} to T_{low})			–	0.22	–	–	0.22	–	
Output Leakage Current (V_{CE} = 40 V, pins 11 and 13)	8	I_{CE}	–	–	50	–	–	50	μA
COMPARATOR SECTION									
Pulse Width Adjustment Range	9	ΔPW	0	–	100	0	–	100	%
Dead Time Adjustment Range	9	ΔDT	0	–	100	0	–	100	%
Temperature Coefficient of Dead Time	–	TCDT	–	0.1	–	–	0.1	–	%/°C
Comparator Bias Currents	12, 13	I_{IB}	–	5.0	15	–	5.0	15	μA
	14	I_{IB}	–	10	30	–	10	30	μA

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	MC3520 Min	MC3520 Typ	MC3520 Max	MC3420 Min	MC3420 Typ	MC3420 Max	Unit
AUXILIARY INPUTS/OUTPUTS									
Ramp Voltage	5								V
Peak High		$V_{ramp(Hi)}$	5.5	6.0	6.5	5.5	6.0	6.5	
Peak Low		$V_{ramp(Low)}$	2.0	2.4	2.8	2.0	2.4	2.8	
Ramp Voltage Change ($V_{ramp\ Hi} - V_{ramp\ Low}$)	5	ΔV_{ramp}	3.0	3.5	4.0	3.0	3.5	4.0	V
Ramp Out Sink Current	5	I_{sink}	–	400	–	–	400	–	µA
Ramp Out Source Current	5	I_{source}	–	3.0	–	–	3.0	–	mA
$\overline{\text{Inhibit}}$ Input Current – High (V_{IH} = 2.0 V)	10	I_{IH}	–	–	40	–	–	40	µA
$\overline{\text{Inhibit}}$ Input Current – Low (V_{IL} = 0.8 V)	10	I_{IL}	–	-25	-180	–	-25	-180	µA
Symmetry Correction Input/Output 2 Inhibit Current – High (V_{SY} = 2.0 V, pin 16)	10	$I_{SY/H}$	–	–	40	–	–	40	µA
Symmetry Correction Input/Output 2 Inhibit Current – Low (V_{SY} = 0.8 V, pin 16)	10	$I_{SY/L}$	–	-10	-180	–	-10	-180	µA
F/F_{out} Source Current	–	I_{source}	–	2.0	–	–	2.0	–	mA
OUTPUT AC CHARACTERISTICS ($T_A = T_{high}$, V_{CC} = +15 V, f = 20 kHz)									
Rise Time	15	t_r	–	40	–	–	40	–	ns
Fall Time	15	t_f	–	150	–	–	150	–	ns
Overlap Time	15	t_{ov}	–	275	–	–	275	–	ns
Assymmetry (Duty Cycle = 50%)	15	$\frac{t_{on1} - t_{on2}}{t_{on1}}$	–	±1.0	–	–	±1.0	–	%

NOTE:
T_{high} = +125°C for MC3520
+70°C for MC3420
T_{low} = -55°C for MC3520
0°C for MC3420

FIGURE 2–EQUIVALENT CIRCUIT

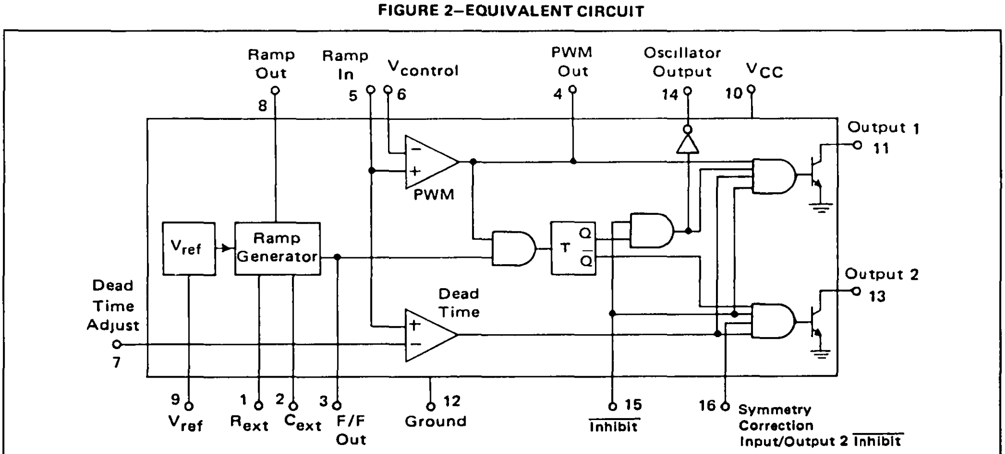
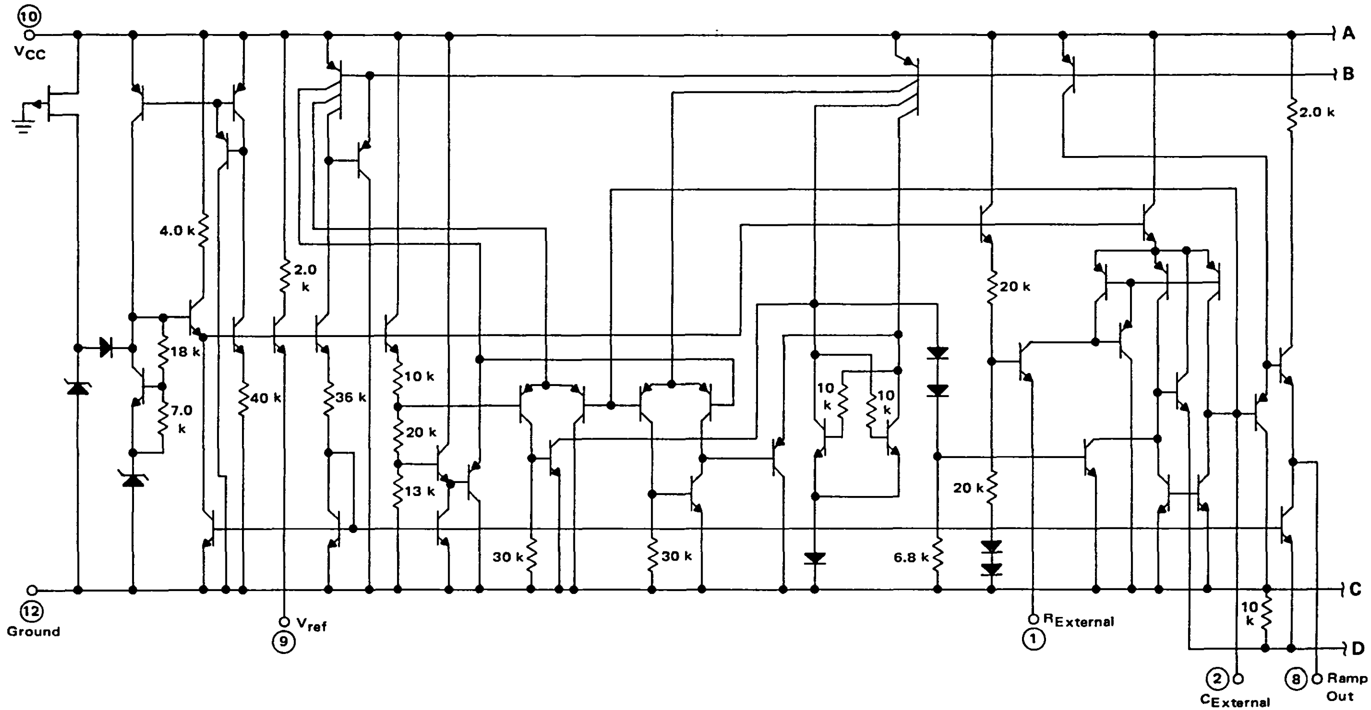
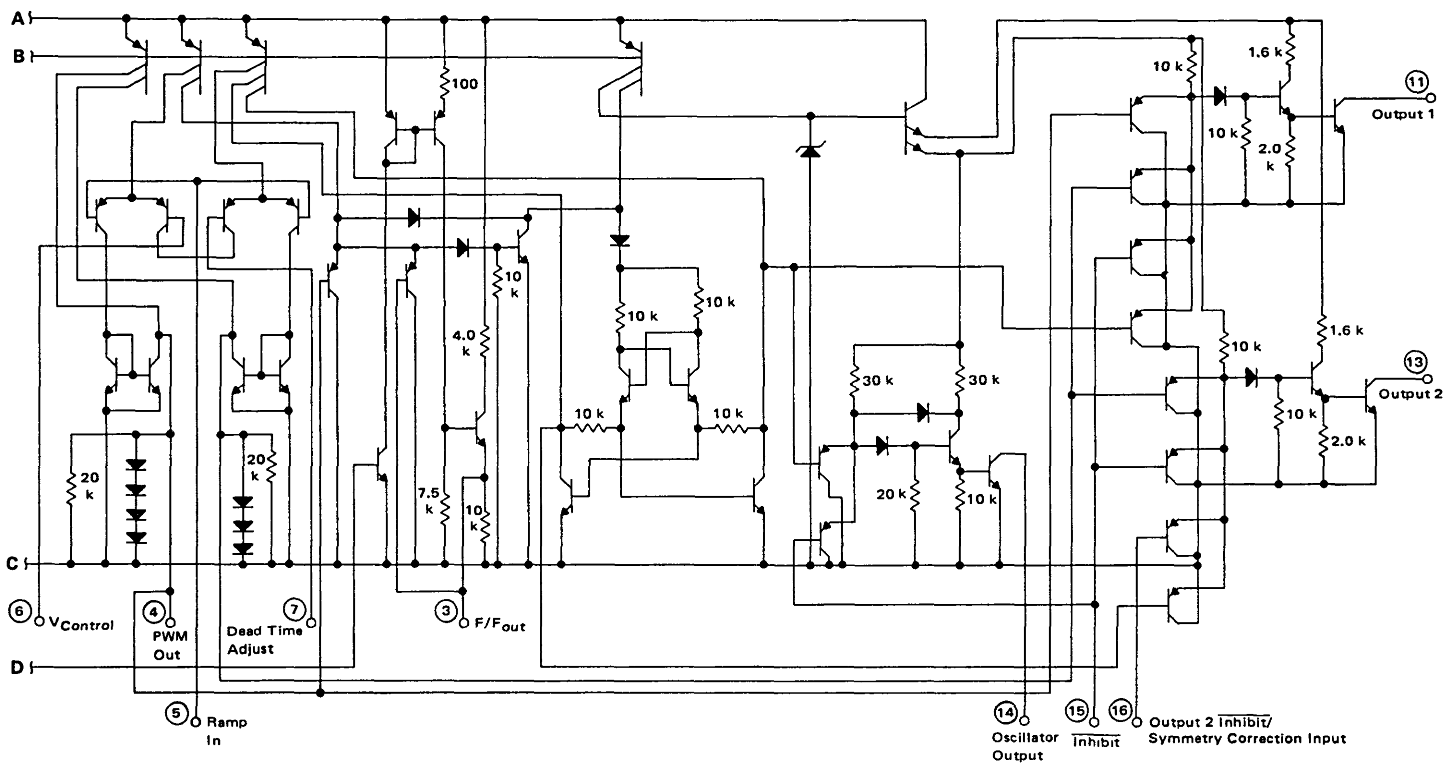


FIGURE 3 – CIRCUIT SCHEMATIC

(continued next page)



(continued) **FIGURE 3 – CIRCUIT SCHEMATIC**



GENERAL INFORMATION

The internal block diagram of the MC3420 is shown in Figure 2, and consists of the following sections:

Voltage Reference

A stable reference voltage is generated by the MC3420 primarily for internal use. However, it is also available externally at Pin 9 (V_{ref}) for use in setting the dead time (Pin 7) and for use as a reference for the external control loop error amplifiers.

Ramp Generator

The ramp generator section produces a symmetrical triangular waveform ramping between 2.4 V and 6.0 V, with frequency determined by an external resistor (R_{ext}) and capacitor (C_{ext}) tied from Pins 1 and 2, respectively, to ground.

PWM Comparator

The output of the ramp generator at pin 8 is normally connected to Pin 5, RAMP IN. The PWM (pulse width modulation) comparator compares the voltage at Pin 6 ($V_{control}$) to the ramp generator output. The level of $V_{control}$ determines the outputs' pulse width or duty cycle. The duty cycle of each output can vary, exclusive of dead time, from 50% (when $V_{control}$ is at approximately 2.4 V) to 0% ($V_{control}$ approximately 6.0 V).

Dead Time Comparator

An additional comparator has been included in MC3420 to allow independent adjustment of system dead time or maximum duty cycle. By dividing down V_{ref} at Pin 9 with a resistive divider or potentiometer, and applying this voltage to Pin 7, a stable dead time is obtained for prevention of inverter switching transistor cross conduction at high duty cycles due to storage time delays.

Phase Splitter

A phase splitter is included to obtain two 180° out of phase outputs for use in multiple transistor inverter systems. It consists of a toggle flip-flop whose clock signal is derived by "ANDing" the output of the PWM comparator and a signal from the ramp generator section. This "AND" gate ensures that the outputs truly alternate under control loop transient conditions. Better understanding of this feature and MC3420 operation may be gained by studying the circuit waveforms, shown in Figure 4.

FIGURE 4 – INTERNAL WAVEFORMS

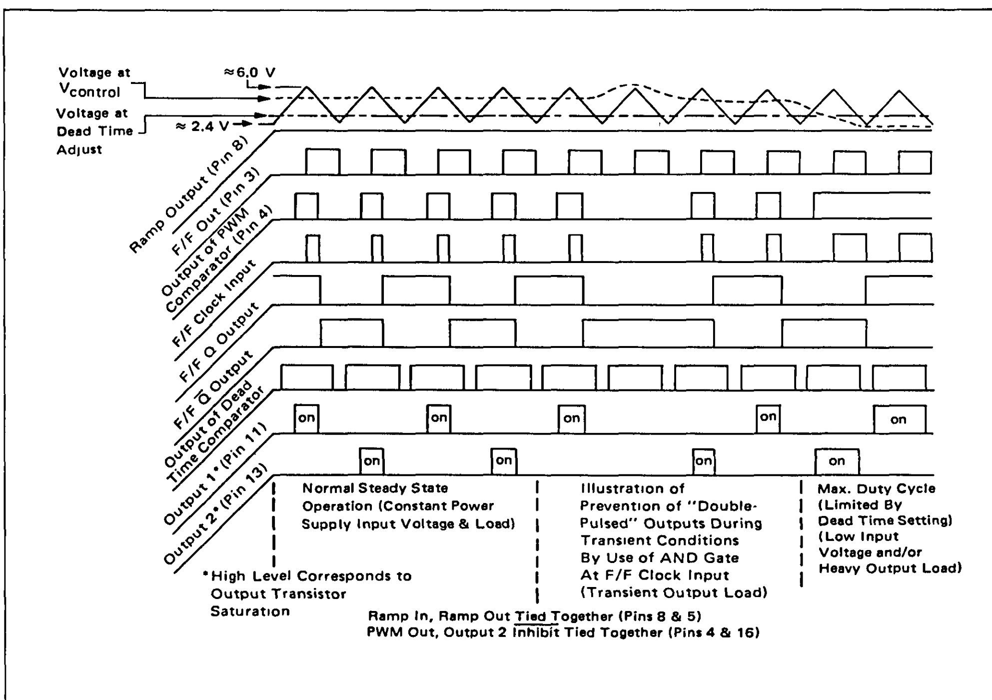


FIGURE 5 – STANDARD AC, DC TEST CIRCUIT

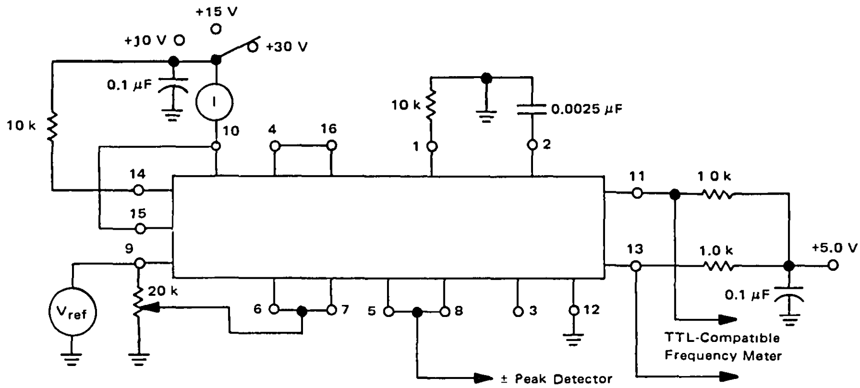


FIGURE 6 – FREQUENCY LIMIT TEST CIRCUIT

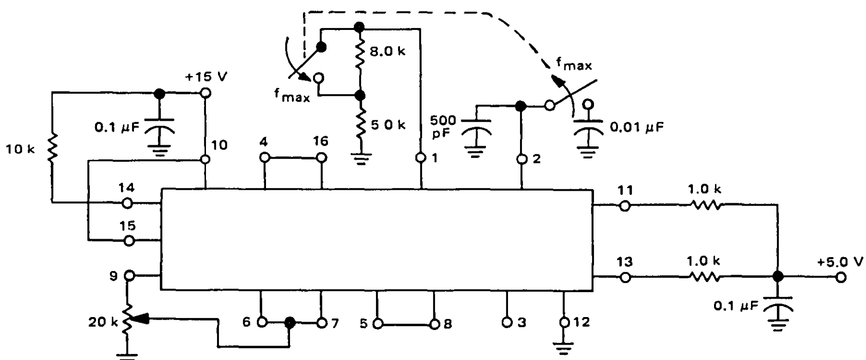
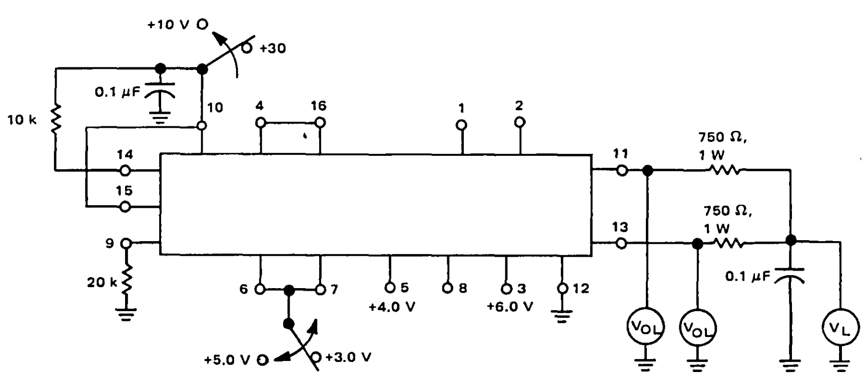
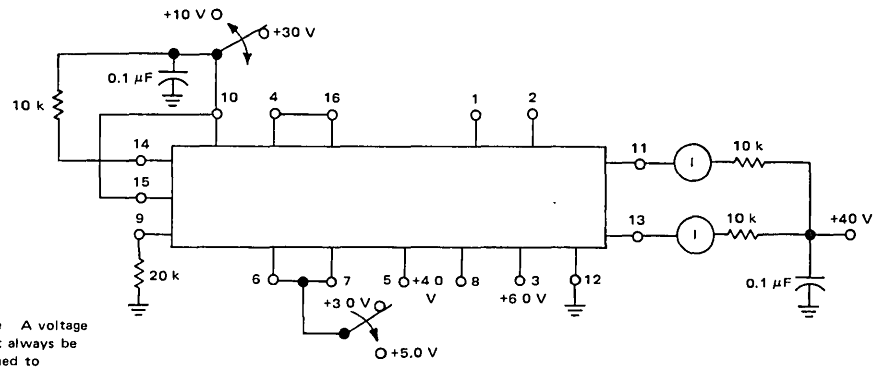


FIGURE 7 – OUTPUT SATURATION TEST CIRCUIT



Note: Use voltage change on pins 6, 7 to change output states.
A voltage must always be present on pins 6 and 7.

FIGURE 8 – OUTPUT LEAKAGE TEST CIRCUIT



Note A voltage must always be applied to pins 6 and 7.

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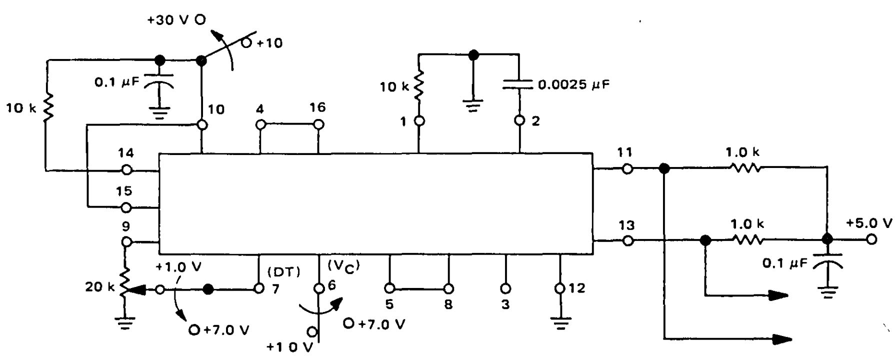
FIGURE 9 – OUTPUT DUTY CYCLE TEST CIRCUIT



TYPICAL DUTY CYCLE versus DEAD TIME VOLTAGE	
PIN 7. DEAD TIME VOLTAGE (V) ($V_{control}$ = 2.0 V)	% DUTY CYCLE (FOR EACH OUTPUT)
2.0	50
2.5	46
3.0	40
3.5	33
4.0	26
4.5	18
5.0	11
5.5	4.0
6.0	0

TYPICAL DUTY CYCLE versus PWM VOLTAGE ($V_{control}$)	
PIN 6. $V_{control}$ (V) (DEAD TIME VOLTAGE = 1.0 V)	% DUTY CYCLE (FOR EACH OUTPUT)
2.0	50
2.5	46
3.0	40
3.5	33
4.0	26
4.5	18
5.0	11
5.5	4.0
6.0	0

	V_6	V_7	
	Volts		
100% Adjust			
Dead Time	1.0	1.0	(Pin 11 + Pin 13 = Logic "1")
Pulse Width	1.0	1.0	
0% Adjust			
Dead Time	7.0	1.0	(Pin 11)(Pin 13) = Logic "1"
Pulse Width	1.0	7.0	

NOTE: Logic "1" is TTL-Compatible V_{OH}.

FIGURE 10 – INHIBIT/SYMMETRY TEST CIRCUIT

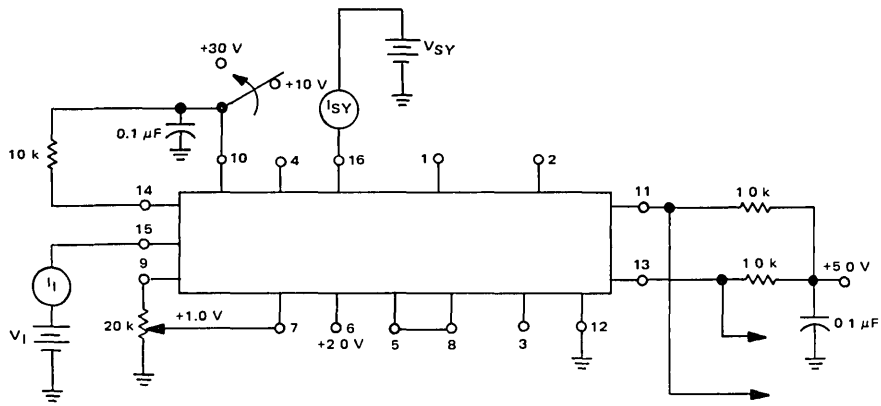


FIGURE 11 – OSCILLATOR OUTPUT (pin 14) TEST CIRCUIT

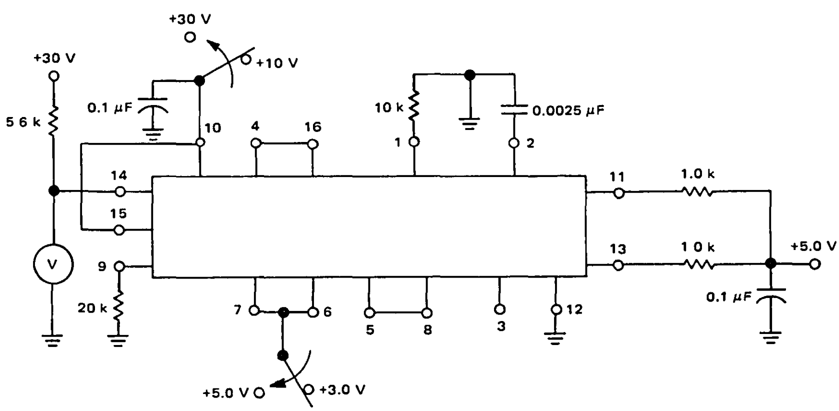


FIGURE 12 – $V_{Control}$ BIAS CURRENT TEST CIRCUIT

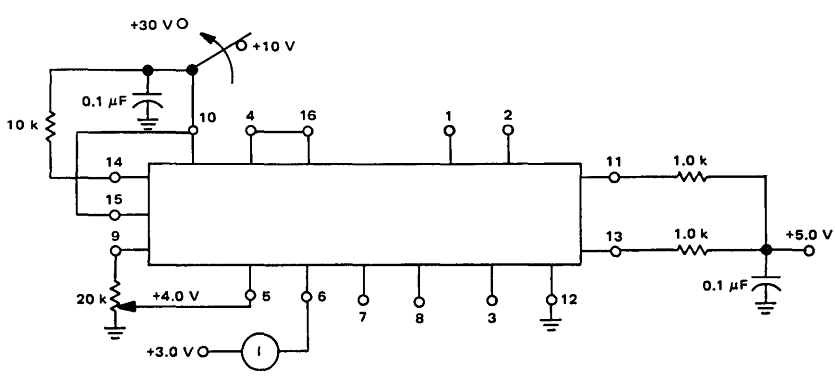


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FIGURE 13 – DEAD TIME BIAS CURRENT TEST CIRCUIT

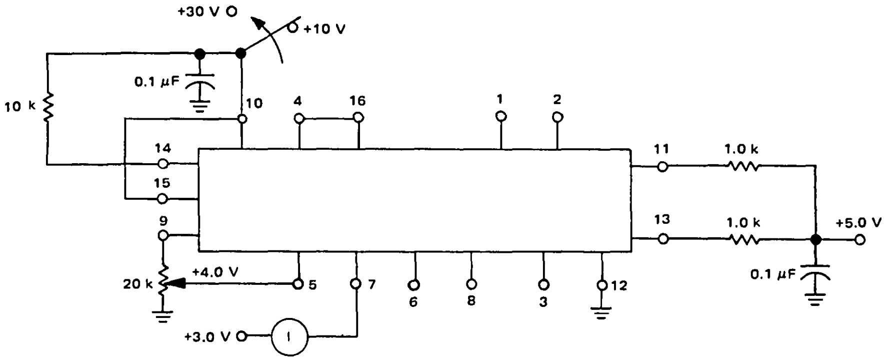


FIGURE 14 – RAMP IN BIAS CURRENT TEST CIRCUIT

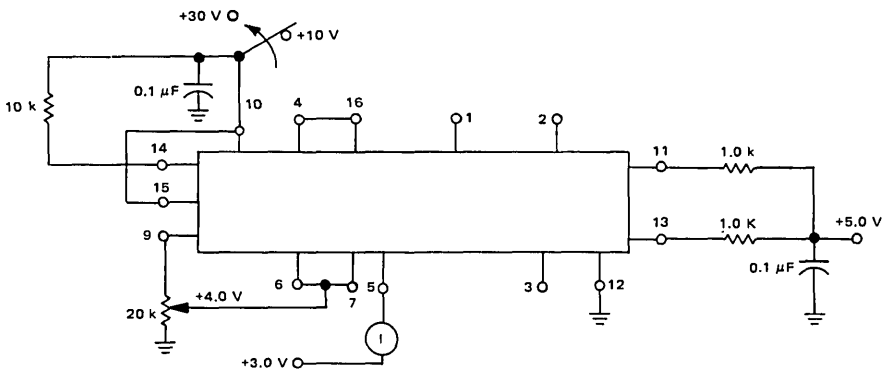
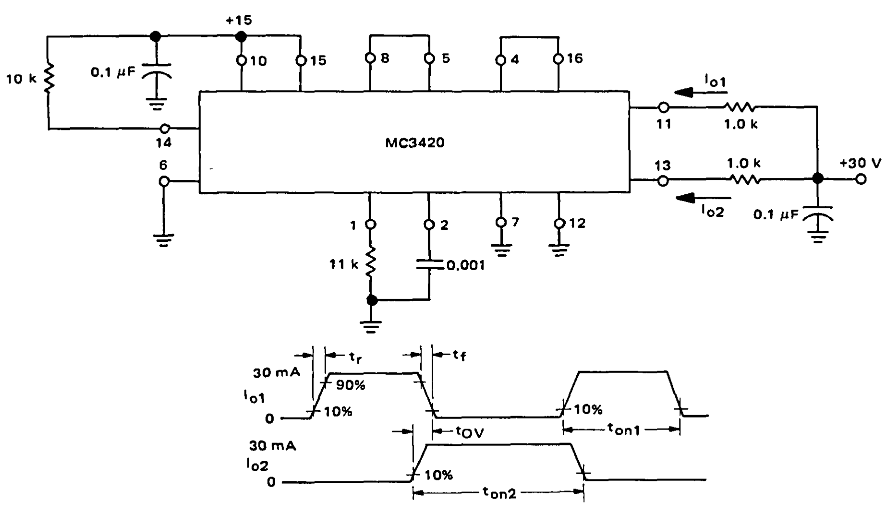


FIGURE 15 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 16 – OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

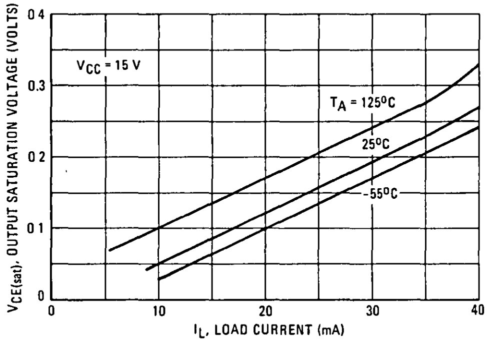


FIGURE 17 – REFERENCE VOLTAGE versus REFERENCE CURRENT

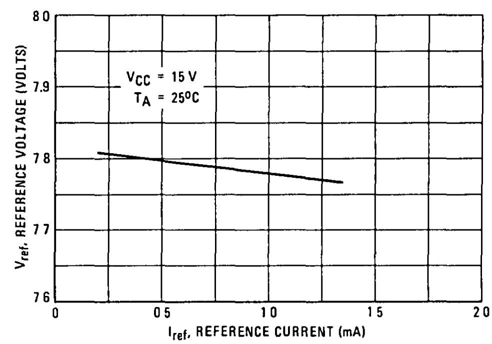


FIGURE 18 – DRAIN CURRENT versus EXTERNAL RESISTANCE

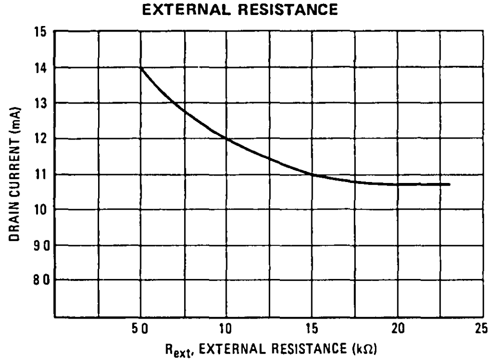


FIGURE 19 – PEAK FLIP-FLOP$_{out}$ VOLTAGE versus EXTERNAL RESISTANCE

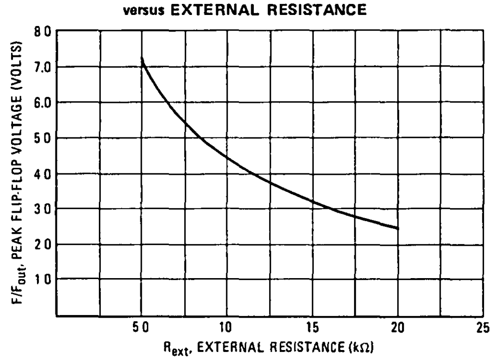


FIGURE 20 – DRAIN CURRENT versus TEMPERATURE

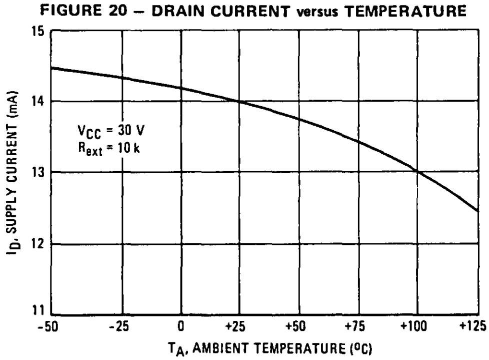
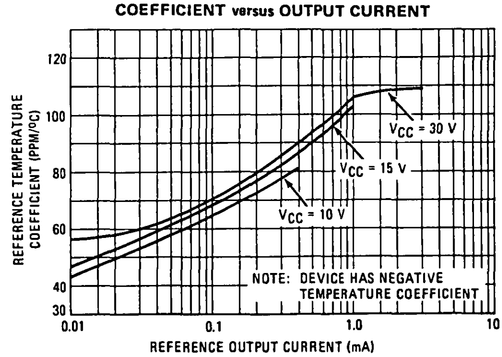


FIGURE 21 – REFERENCE VOLTAGE TEMPERATURE COEFFICIENT versus OUTPUT CURRENT

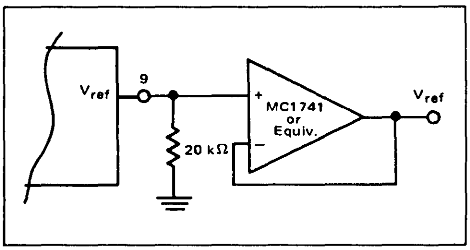


OPERATION AND APPLICATIONS INFORMATION

The Voltage Reference

The temperature coefficient of V_{ref} has been optimized for a 400 μA (≅20 kΩ) load. If increased current capability is required, an op amp buffer may be used, as shown in Figure 22.

FIGURE 22



Output Frequency

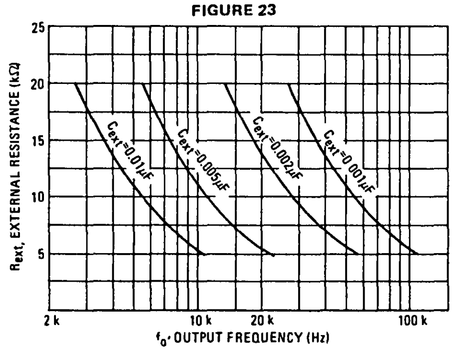
The values of R_{ext} and C_{ext} for a given output frequency, f_o, can be found from:

$$f_o \cong \frac{0.55}{R_{ext}\,C_{ext}};\ 5.0\ k\Omega \leq R_{ext} \leq 20\ k\Omega \quad \text{(Eq. 1)}$$

or from the graph shown in Figure 23.

Note that f_o refers to the frequency of Output 1 (Pin 11) or Output 2 (Pin 13). The frequency of the ramp generator output waveform at Pin 8 will be twice f_o.

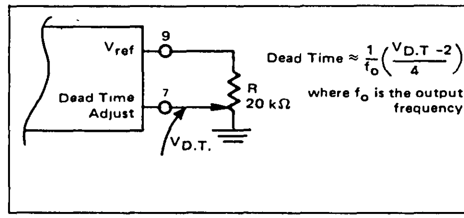
FIGURE 23



Dead Time

Figure 24 illustrates how to set or adjust the MC3420 outputs' dead time or maximum duty cycle. For minimum dead time drift with temperature or supply voltage, $V_{D.T.}$ should be derived from V_{ref} as shown.

FIGURE 24



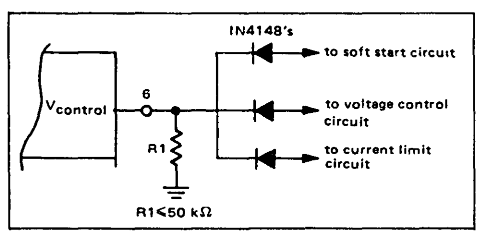
Connections to the $V_{control}$ Pin

In many systems, it is necessary to make multiple connections to the $V_{control}$ Pin in order to implement features in addition to voltage regulation such as current limiting, soft start, etc. These can be made by the use of a simple "diode-OR" connection, as shown in Figure 25. This allows whichever control element is seeking the lowest PWM duty cycle to dominate. Note that a resistor, R1, whose value is ≤ 50 kΩ is placed from the $V_{control}$ Pin to ground. This is necessary to provide a dc path for the PWM comparator input bias current under all conditions.

The system duty cycle is given by:

$$\text{D.C. (\%)} \cong \frac{V_{Control} - 2}{4} \times 100 \quad \text{(Eq. 2)}$$

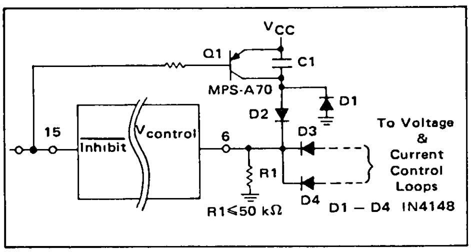
FIGURE 25



Soft Start

In most PWM switching supplies, a soft start feature is desired to prevent output voltage overshoots and magnetizing current imbalances in the power transformer primary. This feature forces the duty cycle of the switching elements to gradually increase from zero to their normal operating point during initial system power-up or after an inhibit. This feature can be easily implemented with the MC3420. One method is shown in Figure 26.

FIGURE 26



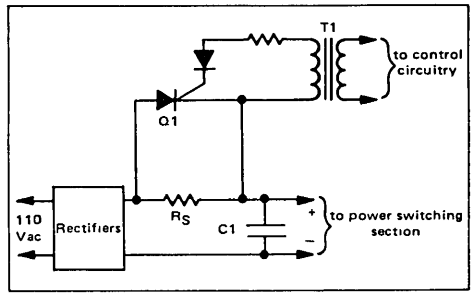
After an inhibit command or during power-up, the voltage on R1 and Pin 6 exponentially decays from V_{CC} toward ground with a time constant of R1C1, allowing a gradual increase in duty cycle. Diodes D2 – D4 provide a diode-or function at the $V_{control}$ Pin, while Q1 serves to reset the timing capacitor, C1, when an inhibit command is received thereby reinitializing the soft-start feature. D1 allows C1 to reset when power (V_{CC}) is turned off.

Inrush Current Limiting

Since many PWM switching supplies are operated directly off the rectified 110 Vac line with capacitive input filters, some means of preventing rectifier failure due to inrush surge currents is usually necessary. One method which can be used is shown in Figure 27.

In this circuit, a series resistor, R_S, is used to provide inrush surge current limiting. After the filter capacitor, C1, is charged, Q1 receives a trigger signal from the control circuitry through T1 and shorts R_S out of the circuit, eliminating its otherwise larger power dissipation. The trigger signal for Q1 may be derived from either the oscillator output (Pin 14) or one of the MC3420's outputs. If the oscillator output is used, it will be necessary

FIGURE 27

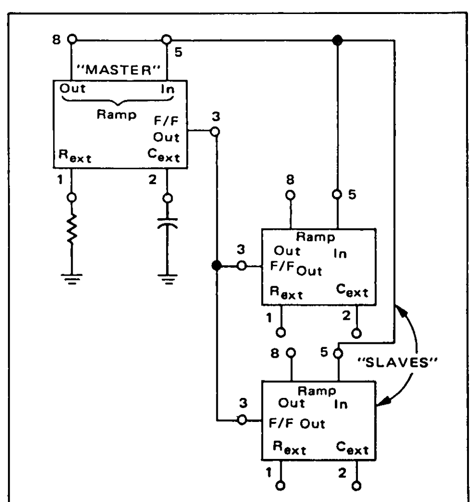


to provide a time delay on the inhibit pin to keep it low until the input filter capacitor, C1, has had time to charge, whereas the initial portion of the soft start timing cycle can be used for this delay if this signal is derived from one of the output pins. However, using the Oscillator Output Pin does offer the advantage that its waveform has a constant 50% duty cycle, independent of the outputs' duty cycle which can simplify the design of a drive circuit for T1.

Slaving

In some applications, as when one PWM inverter/converter is used to feed another, it may be desired that their frequencies be synchronized. This can be done with multiple MC3420s as shown in Figure 28. By omitting their R_{ext} and C_{ext}, up to two MC3420s may be slaved to a master MC3420.

FIGURE 28 – SLAVING THE MC3420



4

4

15 V, 2 A DC-to-DC Converter

Figure 29 illustrates the use of the MC3520 in a PWM switching power supply utilizing a single series switching element (see Appendix for description of PWM switching supply configurations). The series switching transistor, Q1, chops the dc input voltage, V_{in}, at a frequency of ≅ 25 kHz, and the resulting waveform is filtered by L1 and C1 to provide the dc output voltage. The frequency is set by R4 and C3, and since the outputs of the MC3520 are wire-ORed together, fo is twice that given by Equation 1 and Figure 23. V_o is regulated by comparing its value to the MC3520's reference voltage and amplifying the error voltage with U1. The output of U1 is fed into the MC3520 to provide PWM to Q1, thereby controlling its duty cycle and thus the value of V_o.

C2 provides a soft-start feature during power up to prevent output voltage overshoots and excessive start up currents through Q1.

Short circuit protection is provided by R_{SC}, Q3 and Q4. When an overcurrent condition occurs, Q3 is turned on by the voltage across R_{SC}; Q3 drives Q4 on, which raises the voltage at pin 6 ($V_{control}$) of the MC3520, reducing Q1's duty cycle and maintaining a constant output current of ≅ 2.5 A.

5 V, 50 A Line-Operated Supply

A 5 V, 50 A line-operated 20 kHz switching power supply using the MC3520 is shown in Figures 30a and b. An explanation of the operation of each section of the supply follows.

Input Section

The 120 Vac line is full wave voltage doubled by CR1, CR2, C1 and C2 to provide 310 Vdc to the power section of the supply. Inrush surge current limiting is provided by R1, which is shorted out of the circuit by Q1 after C1 and C2 are initially charged.

Power Section

The supply utilizes two switching transistors, Q2 and Q3, in a half-bridge configuration (see Appendix) to drive the high frequency power transformer, T2.

The bases of Q2 and Q3 are driven by T3 and T4, respectively, to provide isolation from the control and base drive sections of the supply. CR3, CR5, CR6, and CR8 constitute anti-saturation (Baker) clamps which provide increased and more uniform switching speeds for Q2 and Q3. CR4 and CR7 allow reverse base currents during turn off.

Output Section

The output of T2 is rectified by Schottky diodes, CR9 and CR10. VR1 is a transient suppressor to protect CR9 and CR10 from transients that might cause reverse breakdown. L1 and C4 constitute the output filter. C4 should have very low ESR (equivalent series resistance) at 20 kHz to provide the most effective filtering. L2 and C5 make up a high-frequency filter to reduce commutation spikes which pass L1 due to its interwinding capacitance. R_{SC} provides output overcurrent sensing to the control section.

Control Section

The MC3520 provides the PWM control for the supply. R2 is adjusted to obtain a 20 kHz operating frequency. R3 adjusts the dead time (≅ 5 μs each half-cycle). U1A and U1B are the output current and output voltage error amplifiers, respectively. R5 sets the output voltage while R4 determines the output current limit. C7 and C8 are the current and voltage loop compensation capacitors.

C6 provides the soft-start feature while Q4 ensures a soft-start after each system inhibit (pin 15 low).

Base Drive Section

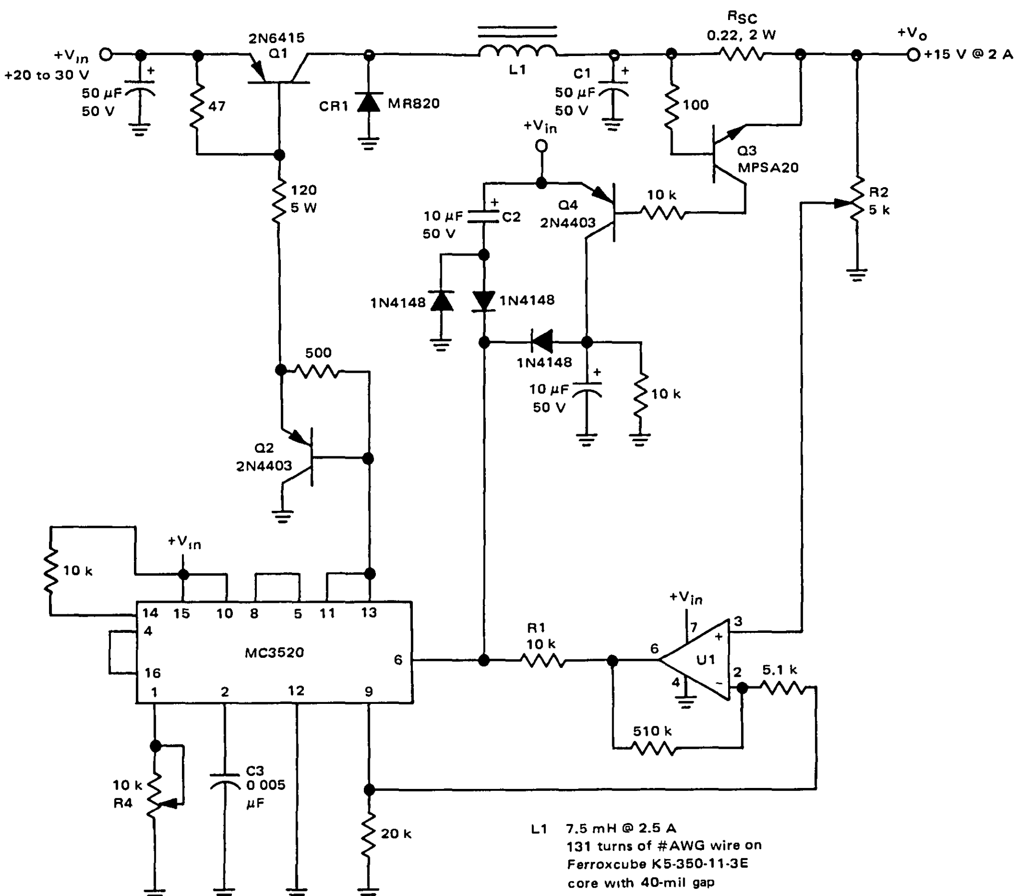
Turn on drive to the power section switching transistors occurs when each of the outputs of the MC3520 saturate. Q5 or Q6 are therefore turned on, and 15 V applied to the primaries of T3 or T4, supplying forward base drive to Q2 or Q3.

Turn off drive occurs when Q5 or Q6 turn off, and the magnetizing energy stored in T3 or T4's core is transformed into a negative "flyback" voltage at their secondaries, providing reverse base drive to Q2 or Q3. CR11 and CR12 act as clamps, to prevent this flyback voltage from exceeding -5 V at T3 or T4's secondary (30 V on Q5 or Q6's collector).

Q1 Driver Section

Q7 and T1 provide the gate drive to Q1. Q7 starts operating after an initial delay of 100 ms created by the soft-start circuit, thereby allowing C1 and C2 to charge up before firing Q1.

FIGURE 29 — 15 V, 2A DC-TO-DC CONVERTER

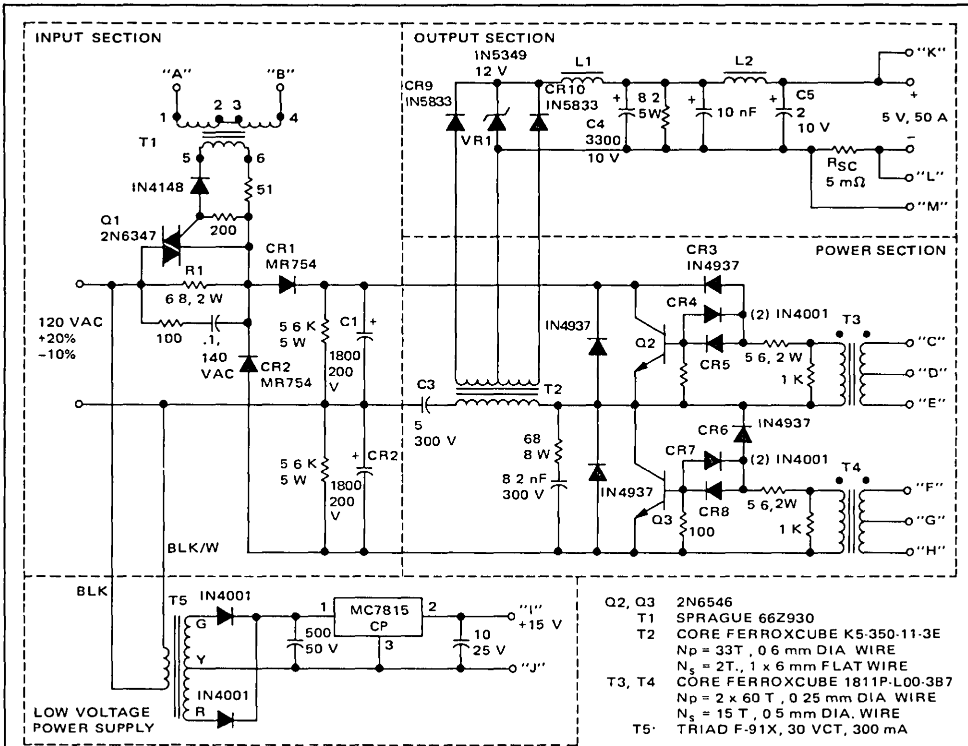


L1 7.5 mH @ 2.5 A
131 turns of #AWG wire on
Ferroxcube K5-350-11-3E
core with 40-mil gap

U1· MC1741CP1

4

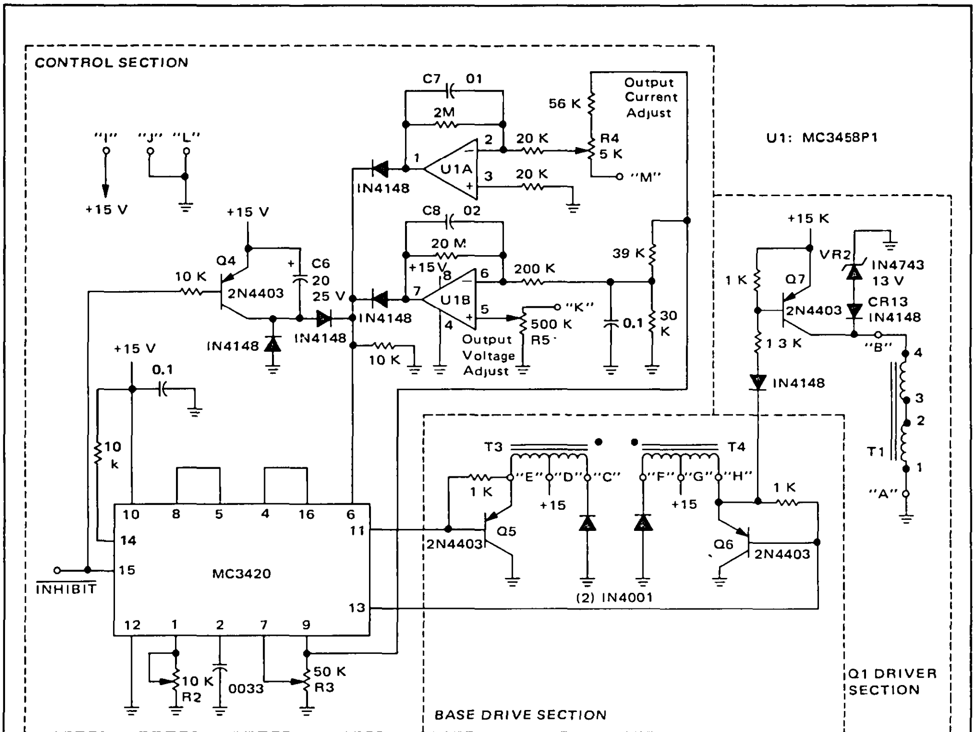
FIGURE 30a — 5 V, 50A LINE-OPERATED SUPPLY (continued on following page)



Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

Performance	
Line Regulation:	0.4%
Load Regulation:	0.25%
Output Ripple and Noise:	60 mV p-p
	25 mV rms
Line current surge at turn-on:	35 A max
Efficiency:	80%

FIGURE 30b



Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

APPENDIX: BASIC PWM SWITCHING SUPPLY POWER CIRCUIT CONFIGURATIONS

The material given in this section is intended to acquaint the designer with the basic switching transistor configurations used in PWM power supplies. Circuit configurations, collector voltage and current waveforms of the switching transistors, and required transistor specifications for the most commonly utilized configurations are shown in Figures 1A through 4A. It should be noted that the waveforms and specifications are idealized, in that the effects of leakage inductance voltage spikes, stray circuit capacitance, snubber networks, clamp diode overshoots, diode reverse recovery and saturation voltages have been neglected. For more information on these effects, the configurations, or switching supplies in general, consult the references listed in the References section.

Series Configuration

The single transistor series configuration is shown in *Figure 1A. This configuration is usually limited to applications in which* $0.2\ V_{CC} < V_o < 0.8\ V_{CC}$ and where input-output isolation is not required.

Push-Pull Configuration

Figure 2A shows the two-transistor push-pull configuration. Unlike the series configuration, it can be used to either step-up or step-down the input voltage, V_{CC}, and also provides input-output isolation. It does, however, have the disadvantage that additional circuitry must be used to provide symmetry correction for the prevention of transformer saturation.

Half-Bridge Configuration

The half-bridge configuration, shown in Figure 3A, does not suffer from the symmetry problems of the push-pull configuration since the transformer primary is capacitively coupled. This prevents transformer core saturation since no net dc current is allowed to flow in its primary.

Note that for the same input power, bus voltage, and duty cycle, the half-bridge requires switching transistors which have twice the current and half the voltage requirements as those of the push-pull configuration.

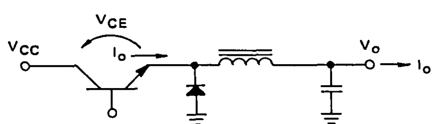
Full-Bridge Configuration

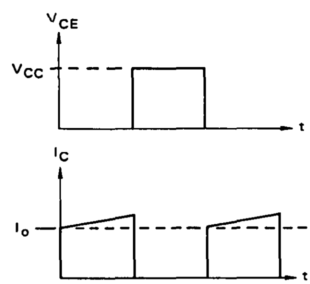
By replacing the bridge capacitors, C, of the half-bridge configuration of Figure 4A results. With this configuration, double the power of the half-bridge configuration can be obtained at the expense of two additional switching transistors and their associated circuitry.

ABBREVIATIONS USED IN FIGURES 1A THROUGH 4A

I_C:	Switching transistor collector current
V_{CE}:	Switching transistor collector-to-emitter-voltage
P_{in}:	Average input power
D.C.:	Inverter duty cycle
V_{CC}:	DC bus voltage
$V_{CEO(sus)}$:	V_{CE} that transistor must withstand during turn-on
V_{CEX}:	V_{CE} that transistor must block during non-conduction period.

FIGURE 1A – SERIES CONFIGURATION





TRANSISTOR REQUIREMENTS*

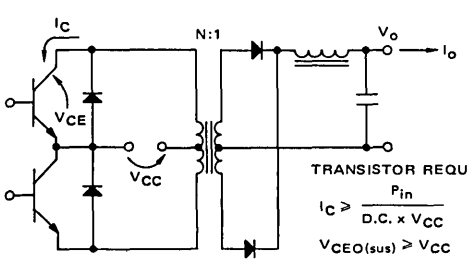
$I_C \geq I_o$

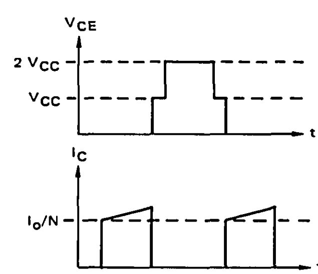
$V_{CEO(sus)} \geq V_{CC}$

$V_{CEX} \geq V_{CC}$

*See explanation of abbreviations in text.

FIGURE 2A – PUSH-PULL CONFIGURATION





TRANSISTOR REQUIREMENTS*

$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$

$V_{CEO(sus)} \geq V_{CC}$

$V_{CEX} \geq 2\,V_{CC}$

*See explanation of abbreviations in text.

FIGURE 3A – HALF-BRIDGE CONFIGURATION

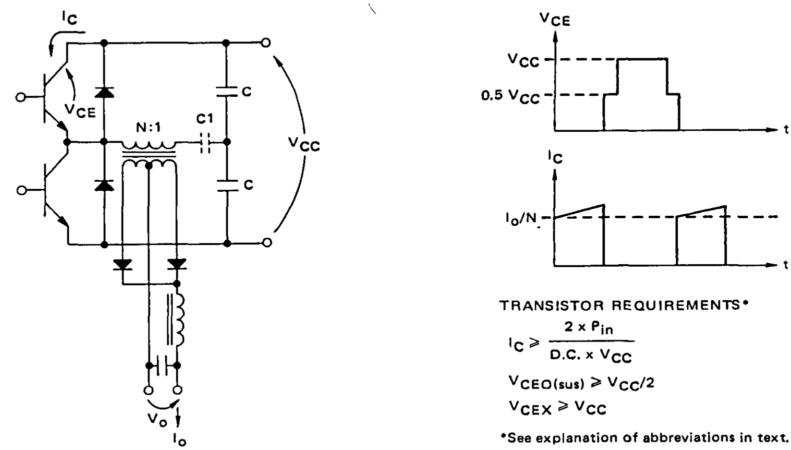
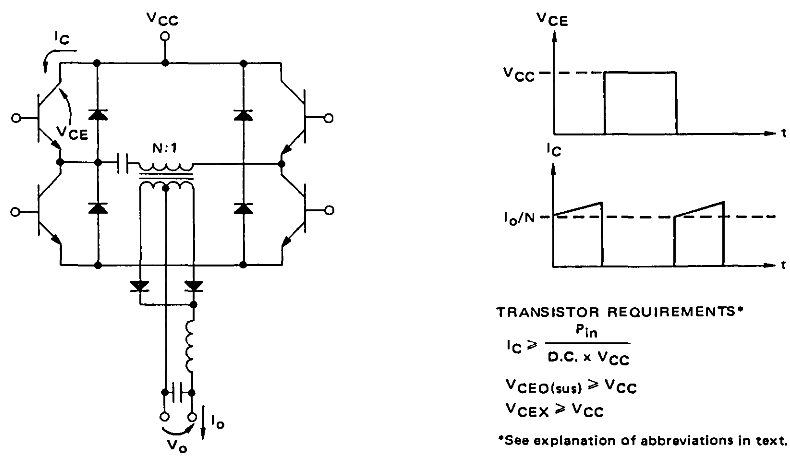


FIGURE 4A – FULL-BRIDGE CONFIGURATION



REFERENCES

More detailed information on switching power supplies may be obtained by consulting the following articles:

1. L. Jansson: "A Survey of Converter Circuits for SMPS," Mullard Technical Communications #119, July 1973.
2. R. Haver: "A New Approach to Switching Regulators," Motorola AN-719, May 1974.
3. R. Haver: "Switched Mode Power Supplies, a 5 V, 40 A Design," Motorola AN-737, December 1974.
4. W. Hersom: "Optimizing the High Current Transistor Converter," *Solid State Power Conversion,* March/April 1975.
5. W. Hirshberg: "Simplify Converter Designs with Flyback," *Solid State Power Conversion,* March/April 1975.
6. P. Wood: "Design of a 5 V, 100 Watt Power Supply, TRW AN #122, February 1975.
7. J. Turnbull: "Radio Frequency Interference Suppression in SMPS," Ferroxcube AN-F601.
8. W. Hetterscheid: "Base Circuit Design for High-Voltage Switching Transistors in Power Converters," Mullard Technical Communications (North American Phillips) #473, November 1974.
9. B. George: "6 V 100 A Switched-Mode Power Supply Operating Directly from the Mains," Mullard Technical Communications (North American Phillips) #123, July 1974.
10. B. Bailey: "Circuit Design and Semiconductor Selection for Square-Wave and Sine-Wave Inverters," *Proc. of Powercon 2,* October 1975.
11. B. Bailey: "Safe Reverse Bias Operation—A New Approach," *Proc. of Powercon 3,* June 1976.
12. Gutmann and Suva: "A Line-Operated, Regulated 5 V/50 A Switching Power Supply," Motorola AN-767, September 1976.

MC7800 Series

Advance Information

3-TERMINAL POSITIVE VOLTAGE REGULATORS

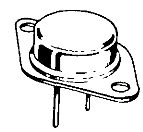
These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance

4

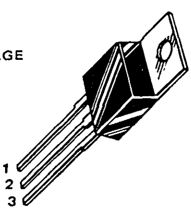
THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 TYPE)



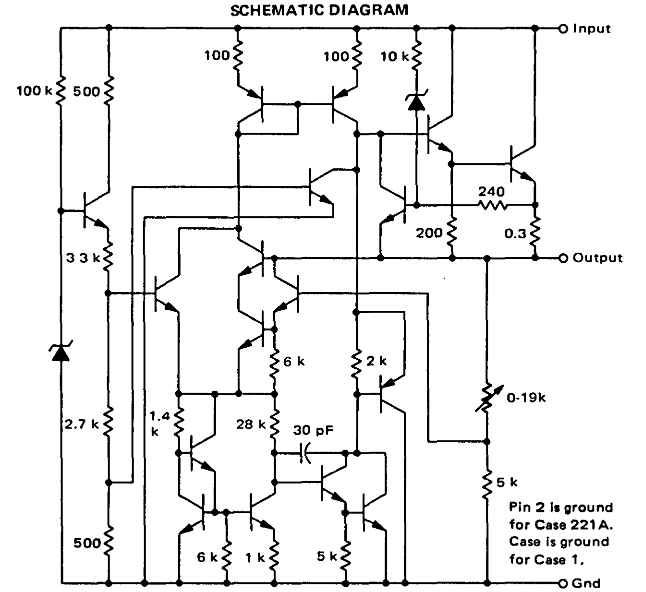
PIN 1. INPUT
2. OUTPUT
CASE GROUND

T SUFFIX
PLASTIC PACKAGE
CASE 221A
TO-220 TYPE

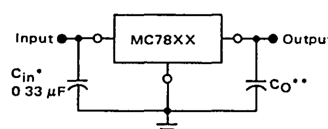


PIN 1. INPUT
2. GROUND
3 OUTPUT

SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

ORDERING INFORMATION

Device	Output Voltage Tolerance	Temperature Range	Package
MC78XXK	4%	−55 to +150°C	Metal Power
MC78XXAK	2%		
MC78XXCK	4%	0 to +125°C	
MC78XXACK	2%		
MC78XXCT	4%		Plastic Power
MC78XXACT	2%		

XX Indicates Nominal Voltage
This is advance information and specifications are subject to change without notice.

TYPE NO'/VOLTAGE			
MC7805	5.0 Volts	MC7815	15 Volts
MC7806	6.0 Volts	MC7818	18 Volts
MC7808	8.0 Volts	MC7824	24 Volts
MC7812	12 Volts		

MC7800 Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (24 V)		V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics				
Plastic Package				
T_A = +25°C		P_D	Internally Limited	Watts
Derate above T_A = +25°C		$1/\theta_{JA}$	15.4	mW/°C
Thermal Resistance, Junction to Air		θ_{JA}	65	°C/W
T_C = +25°C		P_D	Internally Limited	Watts
Derate above T_C = +95°C (See Figure 1)		$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case		θ_{JC}	5.0	°C/W
Metal Package				
T_A = +25°C		P_D	Internally Limited	Watts
Derate above T_A = +25°C		$1/\theta_{JA}$	22.5	mW/°C
Thermal Resistance, Junction to Air		θ_{JA}	45	°C/W
T_C = +25°C		P_D	Internally Limited	Watts
Derate above T_C = +65°C (See Figure 2)		$1/\theta_{JC}$	182	mW/°C
Thermal Resistance, Junction to Case		θ_{JC}	5.5	°C/W
Storage Junction Temperature Range		T_{stg}	−65 to +150	°C
Operating Junction Temperature Range	MC7800, A MC7800C, AC	T_J	−55 to +150 0 to +150	°C

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DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications

Quiescent Current – That part of the input current that is not delivered to the load

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MC7805, C
ELECTRICAL CHARACTERISTICS (V_{in} = 10V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted).

Characteristic	Symbol	MC7805			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4 8	5.0	5.2	4.8	5.0	5 2	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 7.0 Vdc ≤ V_{in} ≤ 20 Vdc 8.0 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	 – 4.65	 – 5 0	 – 5.35	 4.75 –	 5.0 –	 5.25 –	Vdc
Line Regulation (T_J = +25°C, Note 2) 7 0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc	Reg_{in}	 – –	 2 0 1.0	 50 25	 – –	 7.0 2.0	 100 50	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 25 8.0	 100 25	 – –	 40 15	 100 50	mV
Quiescent Current (T_J = +25°C)	I_B	–	3.2	6.0	–	4.3	8.0	mA
Quiescent Current Change 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8 0 Vdc ≤ V_{in} ≤ 25 Vdc 5 0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – 0.3 0 04	 – 0 8 0 5	 – – –	 – – –	 1.3 – 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	68	75	–	–	68	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in} - V_O	–	2.0	2.5	–	2.0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance f = 1.0 kHz	R_O	–	17	–	–	17	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0 2	1.2	–	0 2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2 5	3 3	–	2 2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±0.6	–	–	−1.1	–	mV/°C

MC7805A, AC
ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1 0 A, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted)

Characteristics	Symbol	MC7805A			MC7805AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.9	5.0	5.1	4.9	5 0	5.1	Vdc
Output Voltage (5 0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 7.5 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	4 8	5.0	5.2	4 8	5 0	5.2	Vdc
Line Regulation (Note 2) 7 5 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.0 Vdc ≤ V_{in} ≤ 12 Vdc 8 0 Vdc ≤ V_{in} ≤ 12 Vdc, T_J = +25°C 7 3 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C	Reg_{in}	 – – – –	 2.0 3.0 1.0 2.0	 10 10 4 0 10	 – – – –	 7.0 10 2.0 7.0	 50 50 25 50	mV
Load Regulation (Note 2) 5 0 mA ≤ I_O ≤ 1.5 A 5 0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – – –	 25 – – 8 0	 50 – – 25	 – – – –	 – 25 25 8 0	 – 100 100 50	mV
Quiescent Current T_J = + 25°C	I_B	 – –	 – 3.2	 5.0 4.0	 – –	 – 4 3	 6.0 6.0	mA
Quiescent Current Change 8 0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 0.3 0 2 0.04	 0 5 0 5 0 2	 – – –	 – – –	 0 8 0.8 0 5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, T_J = +25°C 8 0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 500 mA	RR	 68 68	 75 75	 – –	 – –	 – 68	 – –	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2 0	2 5	–	2 0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1 0 kHz)	R_O	–	17	–	–	17	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0.2	1.2	–	0 2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2 5	3 3	–	2 2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±0.6	–	–	−1.1	–	mV/°C

Notes 1. T_{low} = −55°C for MC78XX, A
= 0°C for MC78XXC, AC

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

4

MC7806, C

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7806			MC7806C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	5.75	6.0	6.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 8.0 Vdc ≤ V_{in} ≤ 21 Vdc 9.0 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	 – 5.65	 – 6.0	 – 6.35	 5.7 –	 6.0 –	 6.3 –	Vdc
Line Regulation (T_J = +25°C, Note 2) 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9 0 Vdc ≤ V_{in} ≤ 13 Vdc	Reg_{in}	 – –	 3 0 2.0	 60 30	 – –	 9 0 3.0	 120 60	mV
Load Regulation (T_J = +25°C, Note 2) 5 0 mA ≤ I_O ≤ 1 5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 27 9.0	 100 30	 – –	 43 16	 120 60	mV
Quiescent Current (T_J = +25°C)	I_B	–	3.2	6.0	–	4.3	8.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} 25 Vdc 9.0 Vdc ≤ V_{in} 25 Vdc 5 0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – 0.3 0 04	 – 0.8 0.5	 – – –	 – – –	 1.3 – 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz	RR	65	73	–	–	65	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2 0	2.5	–	2.0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	17	–	–	17	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0 2	1.2	–	0.2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2 5	3.3	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±0.7	–	–	0.8	–	mV/°C

MC7806A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 1 0 A, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7806A			MC7806AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	5.88	6.0	6.12	5 88	6 0	6.12	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 8 6 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	5.76	6.0	6.24	5.76	6.0	6 24	Vdc
Line Regulation (Note 2) 8.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 9.0 Vdc ≤ V_{in} ≤ 13 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc, T_J = +25°C 8.3 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = +25°C	Reg_{in}	 – – – –	 3 0 5.0 2.0 4 0	 11 15 5.0 11	 – – – –	 9.0 11 3 0 9 0	 60 60 30 60	mV
Load Regulation (Note 2) 5 0 mA ≤ I_O ≤ 1 5A 5 0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – – –	 27 – – 9 0	 50 – – 25	 – – – –	 – 43 43 16	 – 100 100 50	mV
Quiescent Current T_J = +25°C	I_B	– –	– 3 2	5.0 4.0	– –	– 4.3	6.0 6 0	mA
Quiescent Current Change 9.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.6 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1 0 A	ΔI_B	 – – –	 0.3 0.2 0 04	 0.5 0.5 0.2	 – – –	 – – –	 0.8 0 8 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, T_J = +25°C 9 0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, I_O = 500 mA	RR	 65 65	 73 73	 – –	 – –	 – 65	 – –	dB
Dropout Voltage (I_O = 1 0 A, T_J = +25°C)	V_{in}-V_O	–	2 0	2 5	–	2.0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1 0 kHz)	R_O	–	17	–	–	17	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0.2	1.2	–	0.2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2 5	3.3	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±0 7	–	–	-0.8	–	mV/°C

Notes: 1. T_{low} = −55°C for MC78XX, A
= 0°C for MC78XXC, AC

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7808, C
ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7808			MC7808C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.7	8.0	8 3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 10.5 Vdc ≤ V_{in} ≤ 23 Vdc 11.5 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	 – 7.6	 – 8 0	 – 8 4	 7 6 –	 8 0 – – –	 8 4 –	Vdc
Line Regulation (T_J = +25°C, Note 2) 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{in}	 – –	 3 0 2.0	 80 40	 – –	 12 5 0	 160 80	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 28 9.0	 100 40	 – –	 45 16	 160 80	mV
Quiescent Current (T_J = +25°C)	I_B	–	3 2	6.0	–	4.3	8.0	mA
Quiescent Current Change 10 5 Vdc ≤ V_{in} 25 Vdc 11.5 Vdc ≤ V_{in} 25 Vdc 5.0 mA ≤ I_O ≤ 1 0 A	ΔI_B	 – – –	 – 0 3 0 04	 – 0.8 0 5	 – – –	 – – –	 1.0 – 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz	RR	 62	 70	 –	 –	 62	 –	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2.0	2 5	–	2.0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	18	–	–	18	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0.2	1.2	–	0 2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3 3	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±1.0	–	–	–0.8	–	mV/°C

MC7808A, AC
ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7808A			MC7808AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.84	8.0	8 16	7.84	8 0	8.16	Vdc
Output Voltage (5 0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 10.6 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	7.7	8.0	8 3	7.7	8 0	8 3	Vdc
Line Regulation (Note 2) 10 6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 11 Vdc ≤ V_{in} ≤ 17 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc, T_J = +25°C 10 4 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = +25°C	Reg_{in}	 – – – –	 4.0 6.0 2 0 4.0	 13 20 6.0 13	 – – – –	 12 15 5 0 12	 80 80 40 80	mV
Load Regulation (Note 2) 5 0 mA ≤ I_O ≤ 1 5A 5 0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – – –	 28 – – 9 0	 50 – – 25	 – – – –	 – 45 45 16	 – 100 100 50	mV
Quiescent Current T_J = +25°C	I_B	– –	– 3 2	5 0 4.0	– –	– 4.3	6 0 6.0	mA
Quiescent Current Change 11 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 10 6 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 0 3 0 2 0 04	 0 5 0.5 0.2	 – – –	 – – –	 0.8 0.8 0 5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, T_J = +25°C 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	 62 62	 70 70	 – –	 – –	 – 62	 – –	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2.0	2.5	–	2 0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	18	–	–	18	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0.2	1.2	–	0 2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	–	2 2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±1.0	–	–	–0 8	–	mV/°C

Notes 1. T_{low} = –55°C for MC78XX, A
= 0°C for MC78XXC, AC

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7812, C
ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7812 Min	MC7812 Typ	MC7812 Max	MC7812C Min	MC7812C Typ	MC7812C Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.5	12	12 5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 14.5 Vdc ≤ V_{in} ≤ 27 Vdc 15.5 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	 – 11.4	 – 12	 – 12.6	 11.4 –	 12 –	 12.6 –	Vdc
Line Regulation (T_J = +25°C, Note 2) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc	Reg_{in}	 – –	 5.0 3 0	 120 60	 – –	 13 6.0	 240 120	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 30 10	 120 60	 – –	 46 17	 240 120	mV
Quiescent Current (T_J = +25°C)	I_B	–	3.4	6.0	–	4.4	8 0	mA
Quiescent Current Change 14 5 Vdc ≤ V_{in} ≤ 30 Vdc 15 Vdc ≤ V_{in} ≤ 30 Vdc 5 0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – 0.3 0.04	 – 0 8 0.5	 – – –	 – – –	 1 0 – 0 5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz	RR	61	68	–	–	60	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2 0	2.5	–	2.0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	18	–	–	18	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0.2	1.2	–	0 2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2 5	3.3	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±1.5	–	–	-1.0	–	mV/°C

MC7812A, AC
ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7812A Min	MC7812A Typ	MC7812A Max	MC7812AC Min	MC7812AC Typ	MC7812AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.75	12	12.25	11.75	12	12.25	Vdc
Output Voltage (5 0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 14.8 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	11.5	12	12.5	11.5	12	12.5	Vdc
Line Regulation 14 8 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 16 Vdc ≤ V_{in} ≤ 22 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc, T_J = +25°C 14 5 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = +25°C	Reg_{in}	 – – – –	 5 0 8 0 3 0 5.0	 18 30 9 0 18	 – – – –	 13 16 6.0 13	 120 120 60 120	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5A 5.0 mA ≤ I_O ≤ 1 0 A 5.0 mA ≤ I_O ≤ 1 5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – – –	 30 – – 10	 50 – – 25	 – – – –	 – 46 46 17	 – 100 100 50	mV
Quiescent Current T_J = +25°C	I_B	 – –	 – 3.4	 5 0 4 0	 – –	 – 4.4	 6.0 6 0	mA
Quiescent Current Change 15 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 14.8 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 0.3 0.2 0 04	 0 5 0.5 0.2	 – – –	 – – –	 0.8 0 8 0 5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, T_J = +25°C 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 500 mA	RR	 61 61	 68 68	 – –	 – –	 – 60	 – –	dB
Dropout Voltage (I_O = 1 0 A, T_J = +25°C)	V_{in}-V_O	–	2.0	2.5	–	2.0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	18	–	–	18	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0 2	1 2	–	0.2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±1.5	–	–	-1.0	–	mV/°C

Notes 1. T_{low} = -55°C for MC78XX, A
= 0°C for MC78XXC, AC

Thigh = +150°C for MC78XX, A
= +125°C for MC78XXC, AC

2 Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

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MC7815, C
ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted)

Characteristic	Symbol	MC7815			MC7815C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14 4	15	15 6	14 4	15	15.6	Vdc
Output Voltage (5 0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 17 5 Vdc ≤ V_{in} ≤ 30 Vdc 18 5 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	 – 14 25	 – 15	 – 15.75	 14 25 –	 15 –	 15 75 –	Vdc
Line Regulation (T_J = +25°C, Note 2) 17 5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc	Reg_{in}	 – –	 6.0 3 0	 150 75	 – –	 13 6 0	 300 150	mV
Load Regulation (T_J = +25°C, Note 2) 5 0 mA ≤ I_O ≤ 1 5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 32 10	 150 75	 – –	 52 20	 300 150	mV
Quiescent Current (T_J = +25°C)	I_B	–	3.4	6 0	–	4 4	8.0	mA
Quiescent Current Change 17 5 Vdc ≤ V_{in} ≤ 30 Vdc 18 5 Vdc ≤ V_{in} ≤ 30 Vdc 5 0 mA ≤ I_O ≤ 1 0 A	ΔI_B	 – – –	 – 0.3 0 04	 – 0 8 0 5	 – – –	 – – –	 1 0 – 0.5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28 5 Vdc, f = 120 Hz	RR	60	66	–	–	58	–	dB
Dropout Voltage (I_O = 1 0 A, T_J = +25°C)	V_{in}-V_O	–	2.0	2 5	–	2.0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1 0 kHz)	R_O	–	19	–	–	19	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0.2	1 2	–	0 2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1 3	2 5	3 3	–	2 2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±1.8	–	–	−1 0	–	mV/°C

MC7815A, AC
ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1 0 A, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted)

Characteristic	Symbol	MC7815A			MC7815AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14 7	15	15 3	14 7	15	15.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15W) 17 9 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	14 4	15	15 6	14 4	15	15 6	Vdc
Line Regulation (Note 2) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 20 Vdc ≤ V_{in} ≤ 26 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc, T_J = +25°C 17 5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C	Reg_{in}	 – – – –	 6 0 9 0 3 0 6 0	 22 30 10 22	 – – – –	 13 16 6.0 13	 150 150 75 150	mV
Load Regulation (Note 2) 5 0 mA ≤ I_O ≤ 1 5A 5 0 mA ≤ I_O ≤ 1 0 A 5 0 mA ≤ I_O ≤ 1 5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – – –	 32 – – 10	 50 – – 25	 – – – –	 – 52 52 20	 – 100 100 50	mV
Quiescent Current T_J = +25°C	I_B	 – –	 – 3 4	 5 5 4 5	 – –	 – 4 4	 6 0 6 0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1 0 A	ΔI_B	 – – –	 0 3 0.2 0 04	 0 5 0 5 0 2	 – – –	 – – –	 0 8 0.8 0 5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, T_J = +25°C 18.5 Vdc ≤ V_{in} ≤ 28 5 Vdc, f = 120 Hz, I_O = 500 mA	RR	 60 60	 66 66	 – –	 – –	 – 58	 – –	dB
Dropout Voltage (I_O = 1 0 A, T_J = +25°C)	V_{in}-V_O	–	2 0	2 5	–	2 0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1 0 kHz)	R_O	–	19	–	–	19	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0 2	1 2	–	0 2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2 5	3.3	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±1.8	–	–	−1 0	–	mV/°C

Notes 1. T_{low} = −55°C for MC78XX, A
= 0°C for MC78XXC, AC

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature Changes in V_O due to heating effects must be taken into account separately Pulse testing with low duty cycle is used.

MC7818, C
ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7818			MC7818C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	17.3	18	18.7	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 21 Vdc ≤ V_{in} ≤ 33 Vdc 22 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	 – 17.1	 – 18	 – 18.9	 17.1 –	 18 –	 18.9 –	Vdc
Line Regulation (T_J = +25°C, Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc	Reg_{in}	 – –	 7.0 4.0	 180 90	 – –	 25 10	 360 180	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 35 12	 180 90	 – –	 55 22	 360 180	mV
Quiescent Current (T_J = +25°C)	I_B	–	3.5	6.0	–	4.5	8.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc 22 Vdc ≤ V_{in} ≤ 33 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – 0.3 0.04	 – 0.8 0.5	 – – –	 – – –	 1.0 – 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz	RR	59	65	–	–	57	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	–	2.0	2.5	–	2.0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	19	–	–	19	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0.2	1.2	–	0.2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±2.3	–	–	–1.0	–	mV/°C

MC7818A, AC
ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7818A			MC7818AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.64	18	18.36	17.64	18	18.36	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 21 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	17.3	18	18.7	17.3	18	18.7	Vdc
Line Regulation (Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 24 Vdc ≤ V_{in} ≤ 30 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C 20.6 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = +25°C	Reg_{in}	 – – – –	 7.0 12 4.0 7.0	 31 45 15 31	 – – – –	 25 28 10 25	 180 180 90 180	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5A 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – – –	 35 – – 12	 50 – – 25	 – – – –	 – 55 55 22	 – 100 100 50	mV
Quiescent Current T_J = +25°C	I_B	 – –	 – 3.4	 5.5 4.5	 – –	 – 4.5	 6.0 6.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 21 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 0.3 0.2 0.04	 0.5 0.5 0.2	 – – –	 – – –	 0.8 0.8 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, T_J = +25°C 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, I_O = 500 mA	RR	 59 59	 65 65	 – –	 – –	 – 57	 – –	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	–	2.0	2.5	–	2.0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	19	–	–	19	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0.2	1.2	–	0.2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±2.3	–	–	–1.0	–	mV/°C

Notes: 1. T_{low} = –55°C for MC78XX, A
= 0°C for MC78XXC, AC

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

4

MC7824, C

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7824			MC7824C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23	24	25	23	24	25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1 0 A, P_O ≤ 15W)	V_O							Vdc
27 Vdc ≤ V_{in} ≤ 38 Vdc		–	–	–	22 8	24	25 2	
28 Vdc ≤ V_{in} ≤ 38 Vdc		22.8	24	25.2	–	–	–	
Line Regulation (T_J = +25°C, Note 2)	Reg_{in}							mV
27 Vdc ≤ V_{in} ≤ 38 Vdc		–	10	240	–	31	480	
30 Vdc ≤ V_{in} ≤ 36 Vdc		–	5 0	120	–	14	240	
Load Regulation (T_J = +25°C, Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A		–	40	240	–	60	480	
250 mA ≤ I_O ≤ 750 mA		–	15	120	–	25	240	
Quiescent Current (T_J = +25°C)	I_B	–	3 6	6.0	–	4.6	8 0	mA
Quiescent Current Change	ΔI_B							mA
27 Vdc ≤ V_{in} ≤ 38 Vdc		–	–	–	–	–	1.0	
28 Vdc ≤ V_{in} ≤ 38 Vdc		–	0 3	0 8	–	–	–	
5 0 mA ≤ I_O ≤ 1.0 A		–	0.04	0.5	–	–	0 5	
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz	RR	56	62	–	–	54	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2.0	2.5	–	2 0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	20	–	–	20	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0 2	1.2	–	0 2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2 5	3.3	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±3 0	–	–	-1.5	–	mV/°C

MC7824A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7824A			MC7824AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23.5	24	24.5	23 5	24	24 5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15W) 27.3 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	23	24	25	23	24	25	Vdc
Line Regulation (Note 2)	Reg_{in}							mV
27 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		–	10	36	–	31	240	
30 Vdc ≤ V_{in} ≤ 36 Vdc		–	15	60	–	35	240	
30 Vdc ≤ V_{in} ≤ 36 Vdc, T_J = +25°C		–	5.0	19	–	14	120	
26.7 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = +25°C		–	10	36	–	31	240	
Load Regulation (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A		–	40	50	–	–	–	
5 0 mA ≤ I_O ≤ 1 0 A		–	–	–	–	60	100	
5 0 mA ≤ I_O ≤ 1 5 A, T_J = +25°C		–	–	–	–	60	100	
250 mA ≤ I_O ≤ 750 mA		–	15	25	–	25	50	
Quiescent Current	I_B	–	–	6 0	–	–	6 0	mA
T_J = +25°C		–	3.6	5 0	–	4 6	6.0	
Quiescent Current Change	ΔI_B							mA
27.3 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		–	0 3	0 5		–	0.8	
27 3 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = +25°C		–	0 2	0.5	–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	0.04	0 2	–	–	0.5	
Ripple Rejection	RR							dB
28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, T_J = +25°C		56	62	–	–	–	–	
28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, I_O = 500 mA		56	62	–	–	54	–	
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2 0	2.5	–	2.0	–	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	40	–	10	–	µV/V_O
Output Resistance (f = 1 0 kHz)	R_O	–	20	–	–	20	–	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	–	0.2	1.2	–	0.2	–	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	±3.0	–	–	-1.5	–	mV/°C

Notes: 1. T_{low} = –55°C for MC78XX, A
= 0°C for MC78XXC, AC

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately Pulse testing with low duty cycle is used.

4

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 221A)

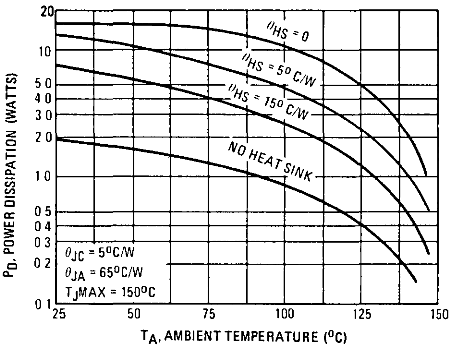


FIGURE 2 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 1)

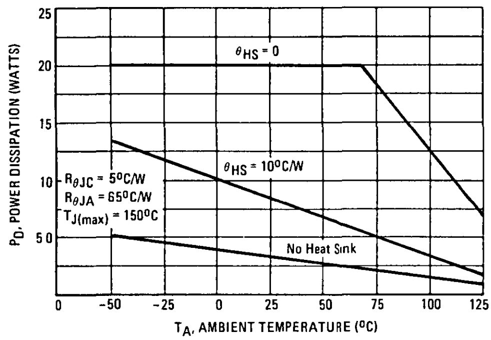


FIGURE 3 – INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC)

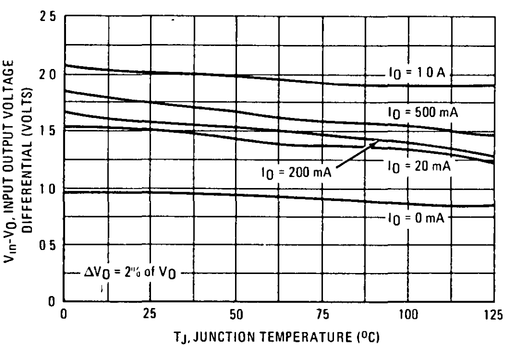


FIGURE 4 – INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XX, A)

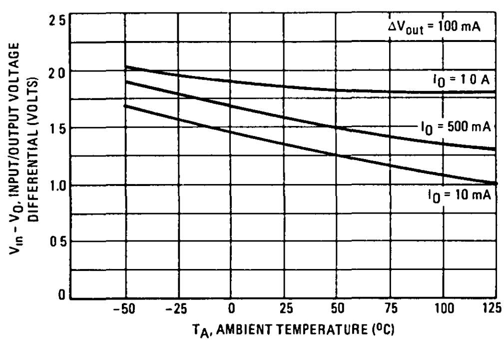


FIGURE 5 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE (MC78XXC, AC)

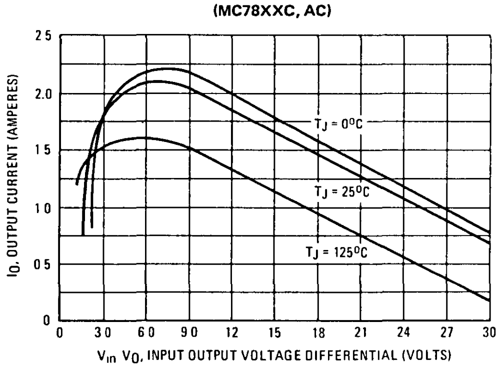
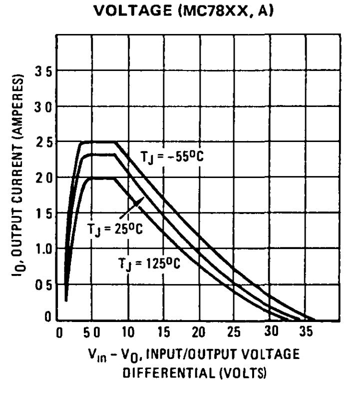


FIGURE 6 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE (MC78XX, A)



4

TYPICAL CHARACTERISTICS (continued)
(T_A = 25°C unless otherwise noted.)

FIGURE 7 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES (MC78XXC, AC)

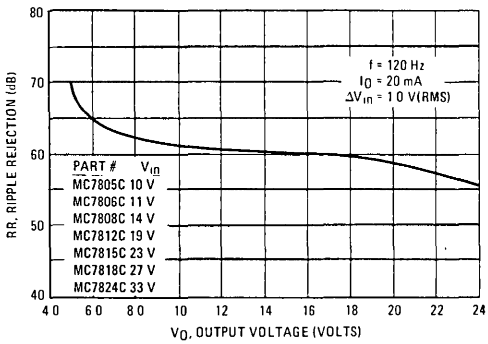


FIGURE 8 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY (MC78XXC, AC)

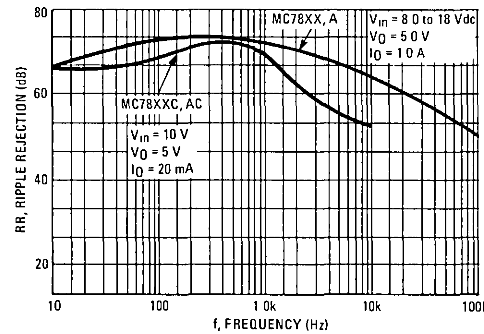


FIGURE 9 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC)

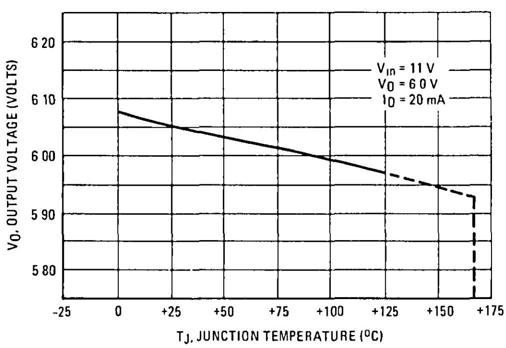


FIGURE 10 – OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE (MC78XXC, AC)

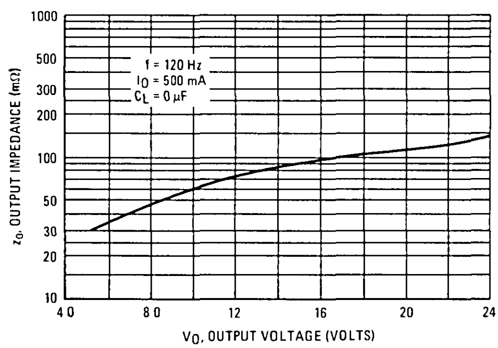


FIGURE 11 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE (MC78XXC, AC)

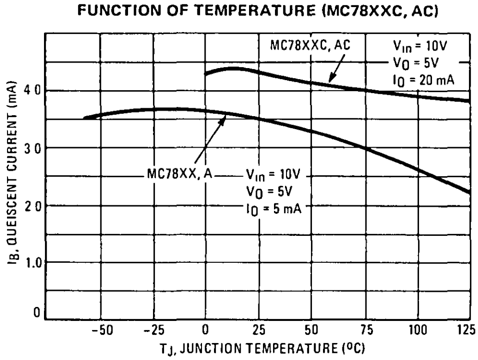
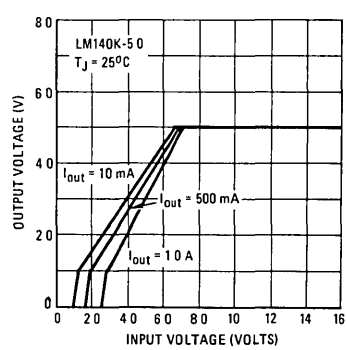


FIGURE 12 – DROPOUT CHARACTERISTICS (MC78XX, A)



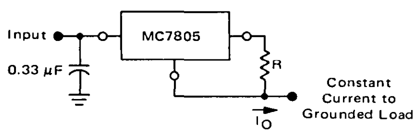
APPLICATIONS INFORMATION

Design Considerations

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead

FIGURE 13 – CURRENT REGULATOR



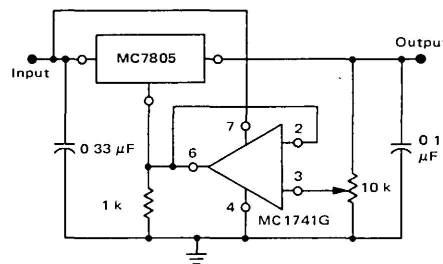
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows.

$$I_O = \frac{5\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts

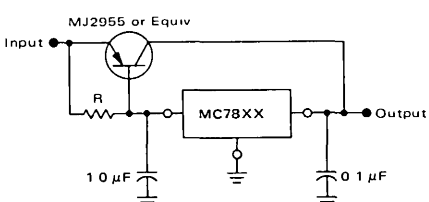
FIGURE 14 – ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
$V_{IN} - V_O \geq 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage

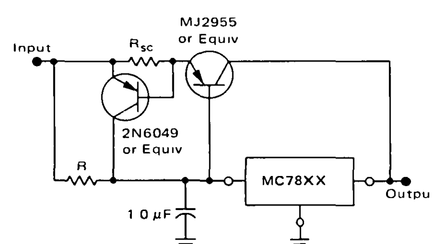
FIGURE 15 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting, this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor

FIGURE 16 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage

The circuit of Figure 15 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified

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MC78L00C,AC Series

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

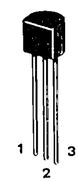
The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

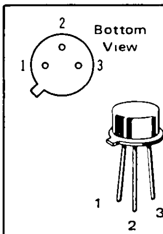
These devices offer a substantial performance advantage over the traditional zener diode-resistor combination. Output impedance is greatly reduced and quiescent current is substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

P SUFFIX
CASE 29
TO-92

Pin 1. Output
2. Ground
3. Input



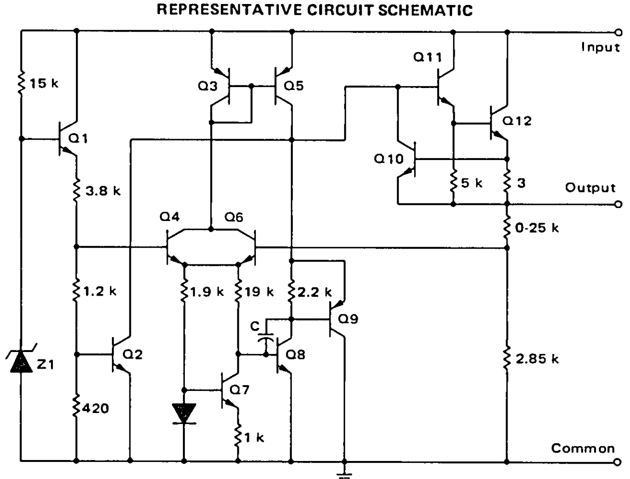


G SUFFIX
CASE 79
TO-39

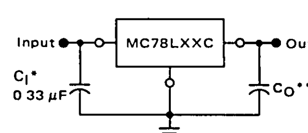
Pin 1. Input
2. Output
3. Ground

(Case connected to pin 3)

REPRESENTATIVE CIRCUIT SCHEMATIC



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response

Device No. ±10%	Device No. ±5%	Nominal Voltage
MC78L05C	MC78L05AC	5 0
MC78L08C	MC78L08AC	8 0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

ORDERING INFORMATION

Device	Temperature Range	Package
MC78LXXACG	T_J = 0°C to +150°C	Metal Can
MC78LXXACP	T_J = 0°C to +150°C	Plastic Transistor
MC78LXXCG	T_J = 0°C to +150°C	Metal Can
MC78LXXCP	T_J = 0°C to +150°C	Plastic Transistor

XX indicates nominal voltage

MC78L00 Series **MAXIMUM RATINGS** (T_A = +125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V – 8.0 V) (12 V – 18 V) (24 V)	V_I	30 35 40	Vdc
Storage Junction Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

MC78L05C, MC78L05AC ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L05C Min	MC78L05C Typ	MC78L05C Max	MC78L05AC Min	MC78L05AC Typ	MC78L05AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.6	5.0	5.4	4.8	5.0	5.2	Vdc
Input Regulation (T_J = +25°C, I_O = 40 mA) 7.0 Vdc ≤ V_I ≤ 20 Vdc 8.0 Vdc ≤ V_I ≤ 20 Vdc	Reg_{line}	 – –	 55 45	 200 150	 – –	 55 45	 150 100	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1 0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 11 5.0	 60 30	 – –	 11 5.0	 60 30	mV
Output Voltage (7 0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 10 V, 1 0 mA ≤ I_O ≤ 70 mA)	V_O	 4.5 4.5	 – –	 5 5 5.5	 4.75 4.75	 – –	 5.25 5.25	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.8 –	 6.0 5.5	 – –	 3.8 –	 6 0 5 5	mA
Input Bias Current Change (8.0 Vdc ≤ V_I ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0 2	 – –	 – –	 1 5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	12	–	–	12	–	mV/1.0 k Hrs
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V, T_J = +25°C)	RR	40	49	–	41	49	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1 7	–	–	1.7	–	Vdc

4

MC78L08C, MC78L08AC ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L08C Min	MC78L08C Typ	MC78L08C Max	MC78L08AC Min	MC78L08AC Typ	MC78L08AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.36	8.0	8.64	7.7	8.0	8.3	Vdc
Input Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
10.5 Vdc ≤ V_I ≤ 23 Vdc		–	20	200	–	20	175	
11 Vdc ≤ V_I ≤ 23 Vdc		–	12	150	–	12	125	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	15	80	–	15	80	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	6.0	40	–	8.0	40	
Output Voltage	V_O							Vdc
(10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		7.2	–	8.8	7.6	–	8.4	
(V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)		7.2	–	8.8	7.6	–	8.4	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.0	6.0	–	3.0	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
(11 Vdc ≤ V_I ≤ 23 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	52	–	–	60	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	20	–	–	20	–	mV/1 0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	36	55	–	37	57	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L12C, MC78L12AC ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0 33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L12C Min	MC78L12C Typ	MC78L12C Max	MC78L12AC Min	MC78L12AC Typ	MC78L12AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.1	12	12.9	11 5	12	12.5	Vdc
Input Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
14.5 Vdc ≤ V_I ≤ 27 Vdc		–	120	250	–	120	250	
16 Vdc ≤ V_I ≤ 27 Vdc		–	100	200	–	100	200	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	20	100	–	20	100	
(T_J = +25°C, 1 0 mA ≤ I_O ≤ 40 mA)		–	10	50	–	10	50	
Output Voltage	V_O							Vdc
(14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		10 8	–	13.2	11 4	–	12.6	
(V_I = 19 V, 1 0 mA ≤ I_O ≤ 70 mA)		10 8	–	13.2	11.4	–	12 6	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	4.2	6 5	–	4.2	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(16 Vdc ≤ V_I ≤ 27 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0 2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	80	–	–	80	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	24	–	–	24	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L15C, MC78L15AC ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted)

Characteristic	Symbol	MC78L15C Min	MC78L15C Typ	MC78L15C Max	MC78L15AC Min	MC78L15AC Typ	MC78L15AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	13.8	15	16.2	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
17.5 Vdc ≤ V_I ≤ 30 Vdc		–	130	300	–	130	300	
20 Vdc ≤ V_I ≤ 30 Vdc		–	110	250	–	110	250	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	25	150	–	25	150	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	12	75	–	12	75	
Output Voltage	V_O							Vdc
(17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		13.5	–	16.5	14.25	–	15.75	
(V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)		13.5	–	16 5	14.25	–	15.75	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	4.4	6.5	–	4.4	6.5	
(T_J = +125°C)		–	–	6 0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(20 Vdc ≤ V_I ≤ 30 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	30	–	–	30	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28 5 V, T_J = +25°C)	RR	33	39	–	34	39	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L18C, MC78L18AC ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0 1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L18C Min	MC78L18C Typ	MC78L18C Max	MC78L18AC Min	MC78L18AC Typ	MC78L18AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	16 6	18	19.4	17.3	18	18.7	Vdc
Input Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
21 4 Vdc ≤ V_I ≤ 33 Vdc		–	32	325				
20.7 Vdc ≤ V_I ≤ 33 Vdc					–	45	325	
22 Vdc ≤ V_I ≤ 33 Vdc		–	27	275				
21 Vdc ≤ V_I ≤ 33 Vdc					–	35	275	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	30	170	–	30	170	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	15	85	–	15	85	
Output Voltage	V_O							Vdc
(21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		16.2	–	17 8				
(20 7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					17.1	–	18.9	
(V_I = 27 V, 1 0 mA ≤ I_O ≤ 70 mA)		16 2	–	17.8				
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)					17.1	–	18.9	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(22 Vdc ≤ V_I ≤ 33 Vdc)		–	–	1.5				
(21 Vdc ≤ V_I = 33 Vdc)					–	–	1 5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	150	–	–	150	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	45	–	–	45	–	mV/1 0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1 7	–	–	1.7	–	Vdc

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MC78L24C, MC78L24AC ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L24C Min	MC78L24C Typ	MC78L24C Max	MC78L24AC Min	MC78L24AC Typ	MC78L24AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	22.1	24	25.9	23	24	25	Vdc
Input Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
27.5 Vdc ≤ V_I ≤ 38 Vdc		–	35	350	–	–	–	
28 Vdc ≤ V_I ≤ 38 Vdc		–	30	300	–	50	300	
27 Vdc < V_I ≤ 38 Vdc		–	–	–	–	60	350	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	40	200	–	40	200	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	20	100	–	20	100	
Output Voltage	V_O							Vdc
(28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		21 6	–	26.4				
(27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					22.8	–	25.2	
(28 Vdc ≤ V_I ≤ 33 V, 1.0 mA ≤ I_O ≤ 70 mA)		21 6	–	26 4				
(27 Vdc ≤ V_I ≤ 33 V, 1.0 mA ≤ I_O ≤ 70 mA)					22.8	–	25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(28 Vdc ≤ V_I ≤ 38 Vdc)		–	–	1.5	–	–	1 5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	200	–	–	200	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	56	–	–	56	–	mV/1 0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	30	43	–	31	45	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

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TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 — DROPOUT CHARACTERISTICS

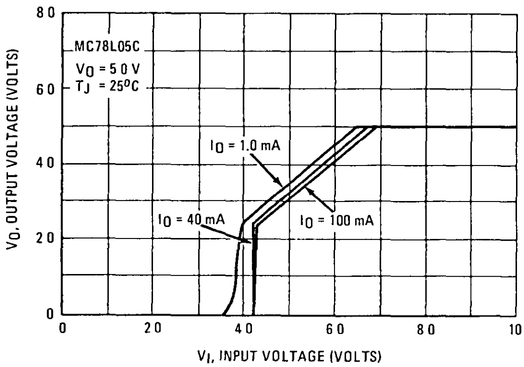


FIGURE 2 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

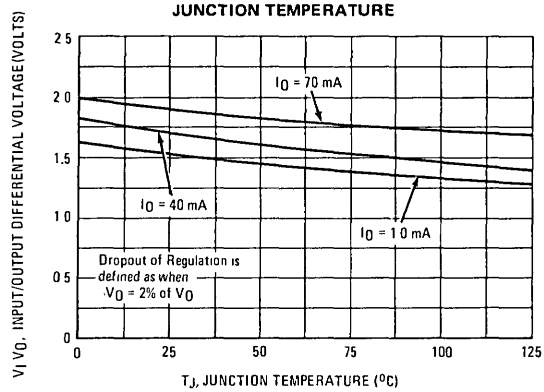


FIGURE 3 — INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

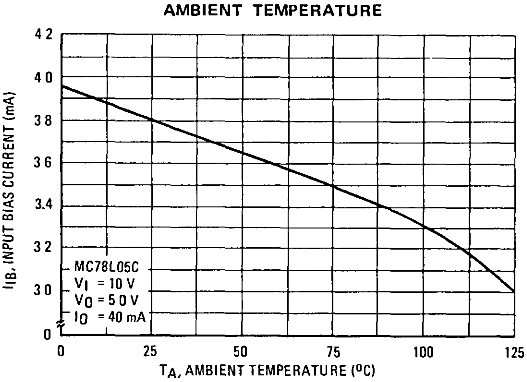


FIGURE 4 — INPUT BIAS CURRENT versus INPUT VOLTAGE

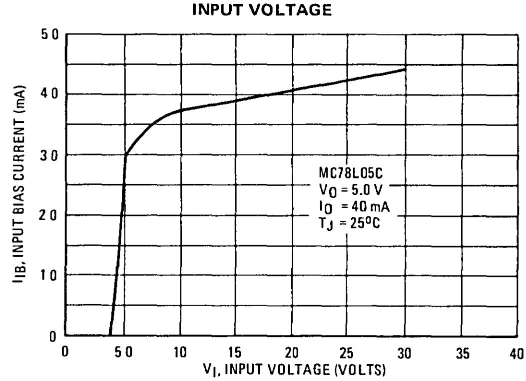


FIGURE 5 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-92 Type Package

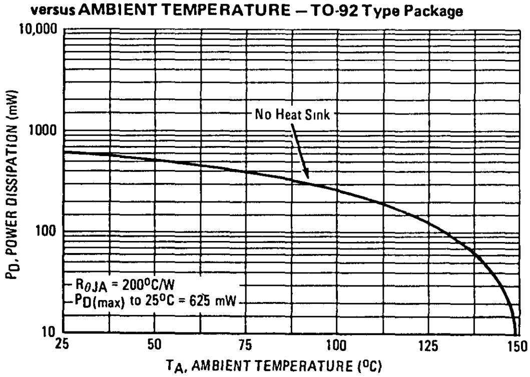
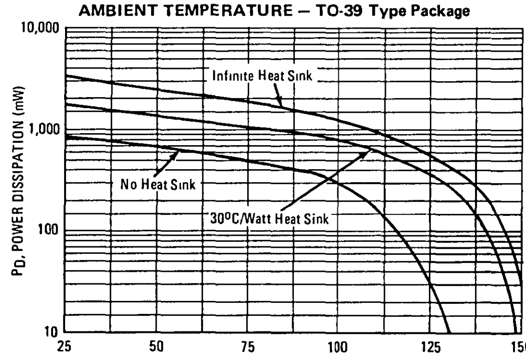


FIGURE 6 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-39 Type Package



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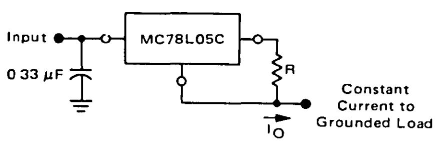
APPLICATIONS INFORMATION

Design Considerations

The MC78L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 – CURRENT REGULATOR



The MC78L00C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows

$$I_O = \frac{5\ V}{R} + I_{IB}$$

I_{IB} = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50-ohm, 1/2-W resistor and the output voltage compliance would be the input voltage less 7 volts.

FIGURE 8 – ±15 V TRACKING VOLTAGE REGULATOR

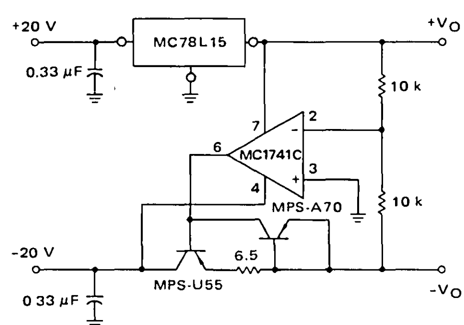
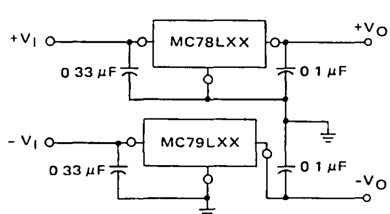


FIGURE 9 – POSITIVE AND NEGATIVE REGULATOR



MC78M00C series

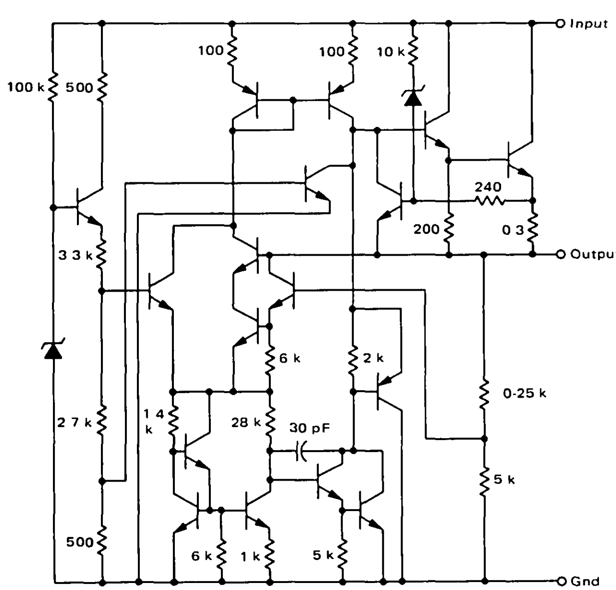
MC78M00C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC78M00 Series positive voltage regulators are identical to the popular MC7800C Series devices, except that they are specified for only one-third the output current. Like the MC7800C devices, the MC78M00C three-terminal regulators are intended for local, on-card voltage regulation.

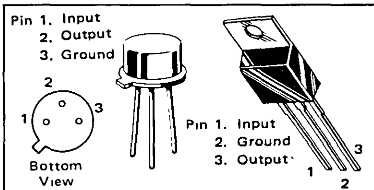
Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A and Case 79 (TO-220 and Hermetic TO-39)

REPRESENTATIVE SCHEMATIC DIAGRAM

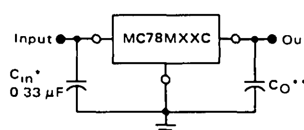


THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS



G SUFFIX	T SUFFIX
METAL PACKAGE	PLASTIC PACKAGE
CASE 79	CASE 221A
TO-39	(TO-220 Type)
(Case connected to Pin 3)	(Heatsink surface connected to Pin 2)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2 0 V above the output voltage even during the low point on the input ripple voltage

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC78MXXCG	T_J = 0° C to +150° C	Metal Can
MC78MXXCT	T_J = 0° C to +150° C	Plastic Power

XX indicates nominal voltage

TYPE NO./VOLTAGE

MC78M05C	5 0 Volts
MC78M06C	6.0 Volts
MC78M08C	8 0 Volts
MC78M12C	12 Volts
MC78M15C	15 Volts
MC78M18C	18 Volts
MC78M20C	20 Volts
MC78M24C	24 Volts

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MC78M00C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (20 V - 24 V)	V_I	35 40	Vdc
Power Dissipation (Package Limitation) Plastic Package T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 110°C Metal Package T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 85°C	 P_D θ_{JA} P_D θ_{JC} P_D θ_{JA} P_D θ_{JC}	 Internally Limited 70 Internally Limited 5.0 Internally Limited 185 Internally Limited 25	 °C/W °C/W °C/W °C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Operating Ambient Temperature Range	T_A	0 to +85	°C
Storage Temperature Range Plastic Package Metal Package	T_{stg}	 -65 to +150 -65 to +150	 °C °C

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MC78M05C ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5 0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation (T_J = +25°C) (7.0 Vdc ≤ V_I ≤ 25 Vdc) (8.0 Vdc ≤ V_I ≤ 25 Vdc)	Reg_{line}	 – –	 3.0 1.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 20 10	 100 50	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	4.75	–	5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	6 0	mA
Quiescent Current Change (8.0 Vdc ≤ V_I ≤ 25 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	40	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V) (I_O = 300 mA, f = 120 Hz, 8.0 ≤ V_I ≤ 18 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	300	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M06C ELECTRICAL CHARACTERISTICS (V_I = 11 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Line Regulation (T_J = +25°C) (8 0 Vdc ≤ V_I ≤ 25 Vdc) (9.0 Vdc ≤ V_I ≤ 25 Vdc)	Reg_{line}	 – –	 5 0 1.5	 100 50	mV
Load Regulation (T_J = +25°C, 5 0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5 0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 20 10	 120 60	mV
Output Voltage (8 0 Vdc ≤ V_I ≤ 25 Vdc, 5 0 mA ≤ I_O ≤ 200 mA)	V_O	5 7	–	6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	6.0	mA
Quiescent Current Change (9 0 Vdc ≤ V_I ≤ 25 Vdc) (5 0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	45	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 9 0 V ≤ V_I ≤ 19 V) (I_O = 300 mA, f = 120 Hz, 9 0 V ≤ V_I ≤ 19 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	270	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5 0 mA)	$\Delta V_O/\Delta T$	–	-1 0	–	mV/°C
Peak Output Current (T_J = 25°C) (T_J = 25°C)	I_O	–	700	–	mA

MC78M08C ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = +25°C) (10.5 Vdc ≤ V_I ≤ 25 Vdc) (11 Vdc ≤ V_I ≤ 25 Vdc)	Reg_{line}	 – –	 6.0 2 0	 100 50	mV
Load Regulation (T_J = +25°C, 5 0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5 0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 160 80	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 25 Vdc, 5 0 mA ≤ I_O ≤ 200 mA)	V_O	7.6	–	8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.6	6.0	mA
Quiescent Current Change (10 5 Vdc ≤ V_I ≤ 25 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	52	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V) (I_O = 300 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	250	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M12C ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = +25°C) (14.5 Vdc ≤ V_I ≤ 30 Vdc) (16 Vdc ≤ V_I ≤ 22 Vdc)	Reg_{line}	– –	8 0 2 0	100 50	mV
Load Regulation (T_J = +25°C, 5 0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5 0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	– –	25 10	240 120	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	11.4	–	12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.8	6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_I ≤ 30 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	– –	– –	0 8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	75	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V) (I_O = 300 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M15C ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5 0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C) (17.5 Vdc ≤ V_I ≤ 30 Vdc) (20 Vdc ≤ V_I ≤ 30 Vdc)	Reg_{line}	– –	10 3 0	100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	– –	25 10	300 150	mV
Output Voltage 17.5 Vdc ≤ V_I ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	14.25	–	15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.8	6.0	mA
Quiescent Current Change (18.5 Vdc ≤ V_I ≤ 30 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	– –	– –	0.8 0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	90	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V) (I_O = 300 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28 5 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

4

MC78M18C ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = +25°C) (21 Vdc ≤ V_I ≤ 33 Vdc) (24 Vdc ≤ V_I ≤ 33 Vdc)	Reg_{line}	 – –	 10 40	 100 50	mV
Load Regulation (T_J = +25°C, 5 0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5 0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 360 180	mV
Output Voltage (21 Vdc ≤ V_I ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	17.1	–	18.9	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.8	6.5	mA
Quiescent Current Change (21 Vdc ≤ V_I ≤ 33 Vdc) (5 0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0 5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	100	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V) (I_O = 300 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M20C ELECTRICAL CHARACTERISTICS (V_I = 29 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	19.2	20	20.8	Vdc
Line Regulation (T_J = +25°C) (23 Vdc ≤ V_I ≤ 35 Vdc) (24 Vdc ≤ V_I ≤ 35 Vdc)	Reg_{line}	 – –	 10 5.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5 0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 400 200	mV
Output Voltage (23 Vdc ≤ V_I ≤ 35 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	19	–	21	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.9	6.5	mA
Quiescent Current Change (23 Vdc ≤ V_I ≤ 35 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	110	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	80	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V) (I_O = 300 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.1	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M24C ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C)					
(27 Vdc ≤ V_I ≤ 38 Vdc)		–	10	100	
(28 Vdc ≤ V_I ≤ 38 Vdc)		–	5.0	50	
Load Regulation	Reg_{load}				mV
(T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA)		–	30	480	
(T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)		–	10	240	
Output Voltage (27 Vdc ≤ V_I ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	22 8	–	25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	5.0	7.0	mA
Quiescent Current Change	ΔI_{IB}				mA
(27 Vdc ≤ V_I ≤ 38 Vdc)		–	–	0.8	
(5.0 mA ≤ I_O ≤ 200 mA)		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	170	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V)	RR	–	70	–	dB
(I_O = 300 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V, T_J = 25°C)		–	70	–	
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-220 (CASE 313)

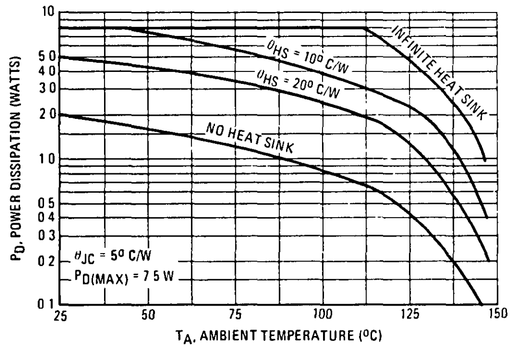


FIGURE 2 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-39 (CASE 79)

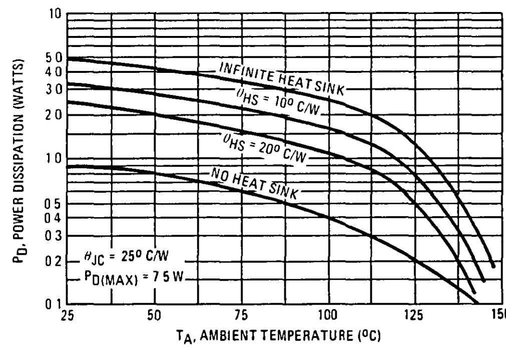


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

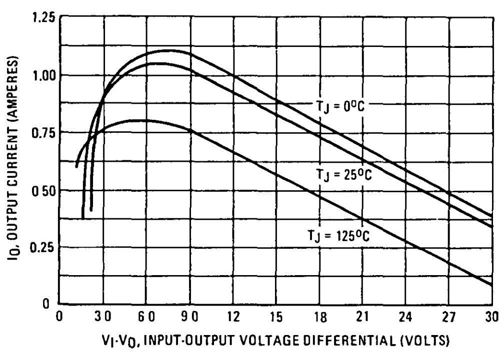
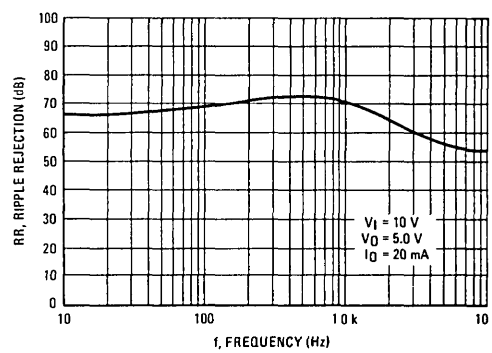


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



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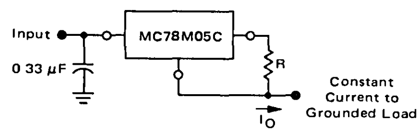
APPLICATIONS INFORMATION

Design Considerations

The MC78M00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 5 — CURRENT REGULATOR



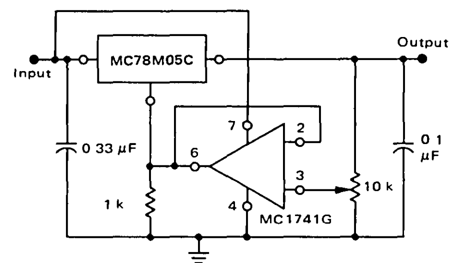
The MC7800C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows.

$$I_O = \frac{5\ V}{R} + I_Q$$

I_Q = 1.5 mA over line and load changes

For example, a 500 mA current source would require R to be a 10-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

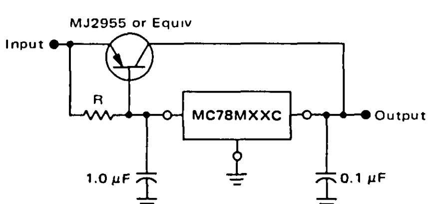
FIGURE 6 — ADJUSTABLE OUTPUT REGULATOR



V_O, 7 0 V to 20 V
$V_{IN} - V_O \geqslant 2\ 0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics The minimum voltage obtainable with this arrangement is 2 0 volts greater than the regulator voltage

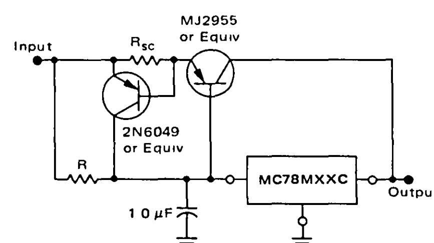
FIGURE 7 — CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage

The MC78M00C series can be current boosted with a PNP transistor The MJ2955 provides current to 5 0 amperes Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting, this circuit is not short-circuit proof Input-output differential voltage minimum is increased by V_{BE} of the pass transistor

FIGURE 8 — SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage

The circuit of Figure 7 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a two-ampere plastic power transistor is specified

MC7900C Series

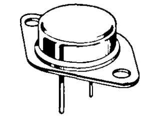
MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

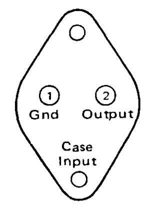
Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A and Case 1 (TO-220 and Hermetic TO-3)

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

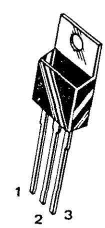


K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 TYPE)



(bottom view)

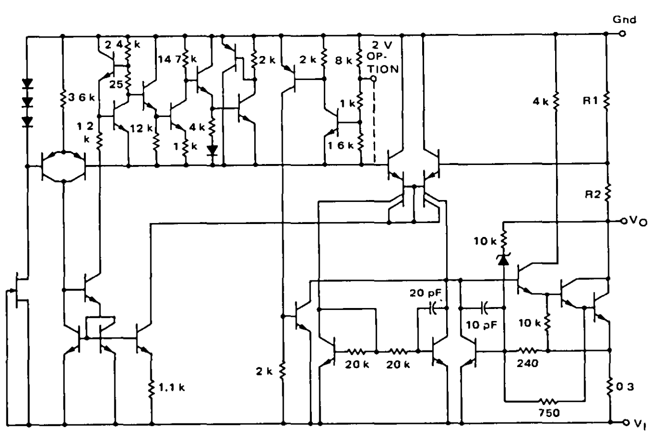
T SUFFIX
PLASTIC PACKAGE
CASE 221A



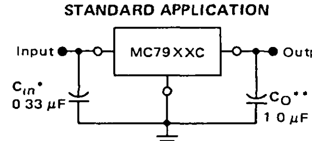
Pin 1. Ground
2. Input
3 Output

(Heatsink surface connected to Pin2)

SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C - 2.0 Volts	MC7906C - 6 0 Volts	MC7915C - 15 Volts
MC7905C - 5 0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C — 5 2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC79XXCK	$T_J = 0^{\circ}C$ to $+150^{\circ}C$	Metal Power
MC79XXCT	$T_J = 0^{\circ}C$ to $+150^{\circ}C$	Plastic Power
XX indicates nominal voltage		

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MC7900C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.0 V – 18 V) (24 V)	V_I	-35 -40	Vdc
Power Dissipation Plastic Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +95°C (See Figure 1) Metal Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +65°C	 P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$ P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$	 Internally Limited 15.4 Internally Limited 200 Internally Limited 22.2 Internally Limited 182	 Watts mW/°C Watts mW/°C Watts mW/°C Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient – Plastic Package – Metal Package	$R_{\theta JA}$	65 45	°C/W
Thermal Resistance, Junction to Case – Plastic Package – Metal Package	$R_{\theta JC}$	5 0 5 5	°C/W

MC7902C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-1.92	-2.00	-2.08	Vdc
Line Regulation (T_J = +25°C, I_O = 100 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc (T_J = +25°C, I_O = 500 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8 0 Vdc ≥ V_I ≥ -12 Vdc	Reg_{line}	 – – – –	 8.0 4.0 18 8 0	 20 10 40 20	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 70 20	 120 60	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 5 0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-1.90	–	-2.10	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change -7.0 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1 5 A	ΔI_{IB}	 – –	 – –	 1 3 0 5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	40	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1 0k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\|V_I - V_O\|$	–	3 5	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7905C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.8	-5.0	-5.2	Vdc
Line Regulation (T_J = +25°C, I_O = 100 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc (T_J = +25°C, I_O = 500 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc	Reg_{line}	 – – – –	 7.0 2.0 35 8.0	 50 25 100 50	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 11 4.0	 100 50	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.75	–	-5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change -7.0 Vdc ≥ V_{in} ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	40	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\vert V_I - V_O \vert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7905.2C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.0	-5.2	-5.4	Vdc
Line Regulation (T_J = +25°C, I_O = 100 mA) -7.2 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc (T_J = +25°C, I_O = 500 mA) -7.2 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc	Reg_{line}	 – – – –	 8.0 2.2 37 8.5	 52 27 105 52	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 12 4.5	 105 52	mV
Output Voltage -7.2 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.94	–	-5.46	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change -7.2 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	42	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	68	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\vert V_I - V_O \vert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

4

MC7906C ELECTRICAL CHARACTERISTICS (V_I = -11 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.75	-6.0	-6.25	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-8.0 Vdc ≥ V_I ≥ -25 Vdc		–	9.0	60	
-9.0 Vdc ≥ V_I ≥ -13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 500 mA)					
-8.0 Vdc ≥ V_I ≥ -25 Vdc		–	43	120	
-9.0 Vdc ≥ V_I ≥ -13 Vdc		–	10	60	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	13	120	
250 mA ≤ I_O ≤ 750 mA		–	5.0	60	
Output Voltage -8.0 Vdc ≥ V_I ≥ -21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	-5.7	–	-6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-8.0 Vdc ≥ V_I ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	45	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\|V_I-V_O\|$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7908C ELECTRICAL CHARACTERISTICS (V_I = -14 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-7.7	-8.0	-8.3	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-10.5 Vdc ≥ V_I ≥ -25 Vdc		–	12	80	
-11 Vdc ≥ V_I ≥ -17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 500 mA)					
-10.5 Vdc ≥ V_I ≥ -25 Vdc		–	50	160	
-11 Vdc ≥ V_I ≥ -17 Vdc		–	22	80	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	26	160	
250 mA ≤ I_O ≤ 750 mA		–	9.0	80	
Output Voltage -10.5 Vdc ≥ V_I ≥ -23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-7.6	–	-8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-10.5 Vdc ≥ V_I ≥ -25 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	52	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\|V_I-V_O\|$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7912C ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.5	-12	-12.5	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-14.5 Vdc ≥ V_I ≥ -30 Vdc		–	13	120	
-16 Vdc ≥ V_I ≥ -22 Vdc		–	6.0	60	
(T_J = +25°C, I_O = 500 mA)					
-14.5 Vdc ≥ V_I ≥ -30 Vdc		–	55	240	
-16 Vdc ≥ V_I ≥ -22 Vdc		–	24	120	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	46	240	
250 mA ≤ I_O ≤ 750 mA		–	17	120	
Output Voltage -14.5 Vdc ≥ V_I ≥ -27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-11.4	–	-12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-14.5 Vdc ≥ V_I ≥ -30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	75	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\|V_I - V_O\|$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7915C ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.4	-15	-15.6	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	14	150	
-20 Vdc ≥ V_I ≥ -26 Vdc		–	6.0	75	
(T_J = +25°C, I_O = 500 mA)					
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	57	300	
-20 Vdc ≥ V_I ≥ -26 Vdc		–	27	150	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	68	300	
250 mA ≤ I_O ≤ 750 mA		–	25	150	
Output Voltage -17.5 Vdc ≥ V_I ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-14.25	–	-15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	90	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\|V_I - V_O\|$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7918C ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-17.3	-18	-18.7	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-21 Vdc ≥ V_I ≥ -33 Vdc		–	25	180	
-24 Vdc ≥ V_I ≥ -30 Vdc		–	10	90	
(T_J = +25°C, I_O = 500 mA)					
-21 Vdc ≥ V_I ≥ -33 Vdc		–	90	360	
-24 Vdc ≥ V_I ≥ -30 Vdc		–	50	180	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A		–	110	360	
250 mA ≤ I_O ≤ 750 mA		–	55	180	
Output Voltage -21 Vdc ≥ V_I ≥ -33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-17.1	–	-18.9	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-21 Vdc ≥ V_I ≥ -33 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	110	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

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MC7924C ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-23	-24	-25	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-27 Vdc ≥ V_I ≥ -38 Vdc		–	31	240	
-30 Vdc ≥ V_I ≥ -36 Vdc		–	14	120	
(T_J = +25°C, I_O = 500 mA)					
-27 Vdc ≥ V_I ≥ -38 Vdc		–	118	480	
-30 Vdc ≥ V_I ≥ -36 Vdc		–	70	240	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A		–	150	480	
250 mA ≤ I_O ≤ 750 mA		–	85	240	
Output Voltage -27 Vdc ≥ V_I ≥ -38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-22.8	–	-25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.6	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-27 Vdc ≥ V_I ≥ -38 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	170	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220)

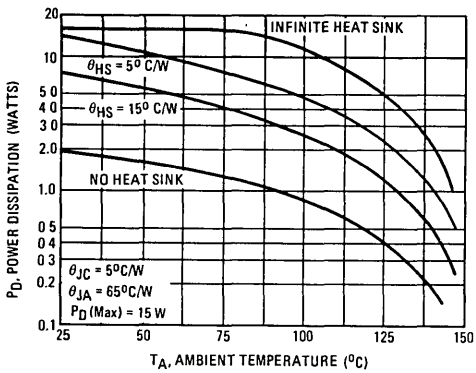

FIGURE 2 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3)

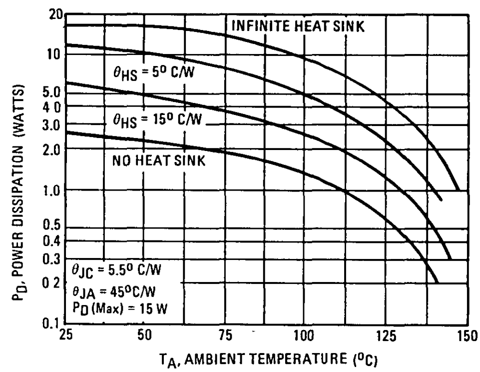

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FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

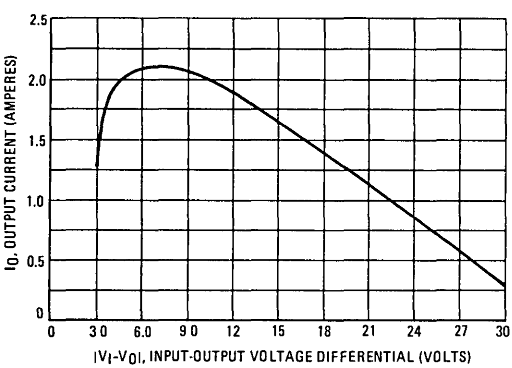


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

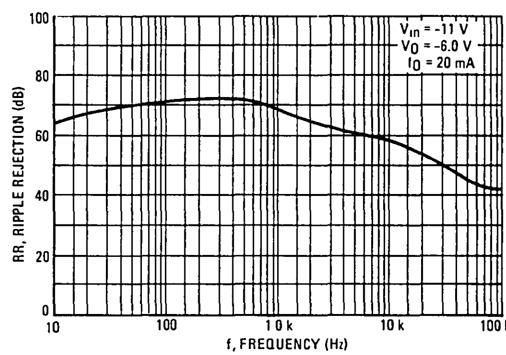


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

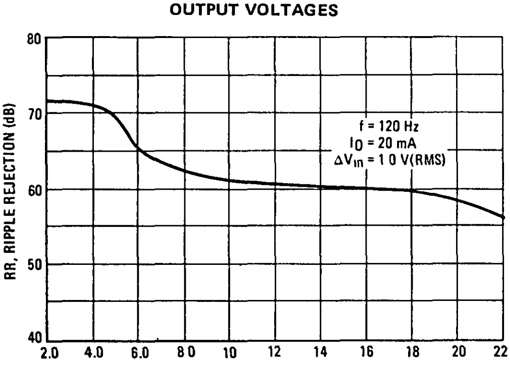
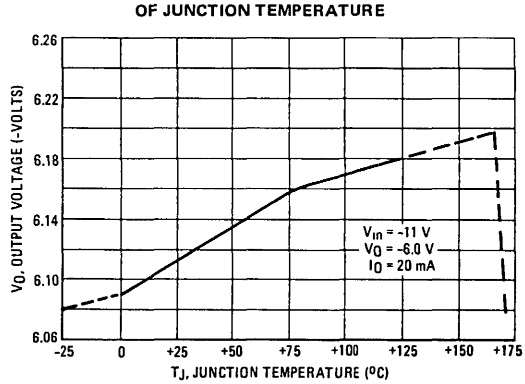
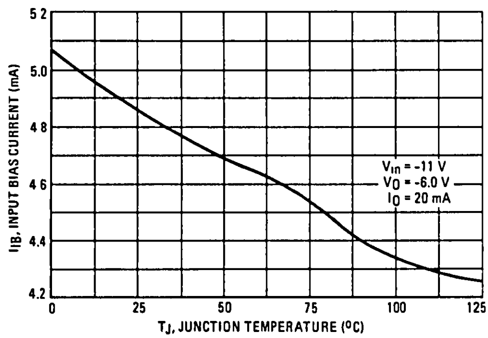


FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability - Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

4

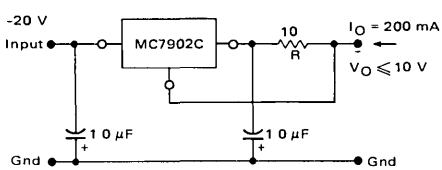
APPLICATIONS INFORMATION

Design Considerations

The MC7900C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased

In many low current applications, compensation capacitors are not required However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0 33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 — CURRENT REGULATOR

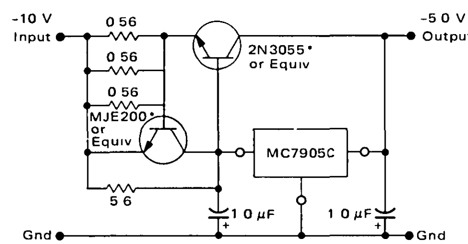


The MC7902, -2 0 V regulator can be used as a constant current source when connected as above The output current is the sum of resistor R current and quiescent bias current as follows

$$I_O = \frac{2\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 2.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage

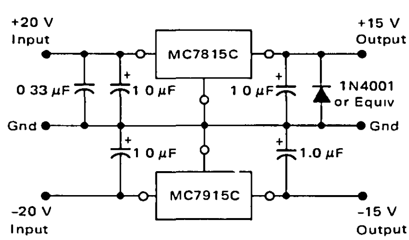
FIGURE 9 — CURRENT BOOST REGULATOR
(-5.0 V @ 4.0 A, with 5.0 A current limiting)



*Mounted on common heat sink, Motorola MS-10 or equivalent

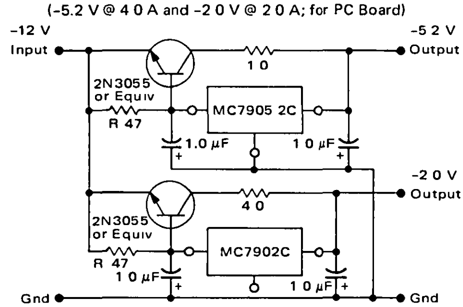
When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3 2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0 6 V/R_{SC} Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

FIGURE 10 — OPERATIONAL AMPLIFIER SUPPLY
(±15 V @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems.

FIGURE 11 — TYPICAL MECL SYSTEM POWER SUPPLY
(-5.2 V @ 4 0 A and -2 0 V @ 2 0 A; for PC Board)



When current-boost power transistors are used, 47-ohm base-to-emitter resistors (R) must be used to bypass the quiescent current at no load. These resistors, in conjunction with the V_{BE} of the NPN transistors, determine when the pass transistors begin conducting. The 1-ohm and 4-ohm dropping resistors were chosen to reduce the power dissipated in the boost transistors but still leave at least 2.0 V across these devices for good regulation.

MC79L00C, AC series

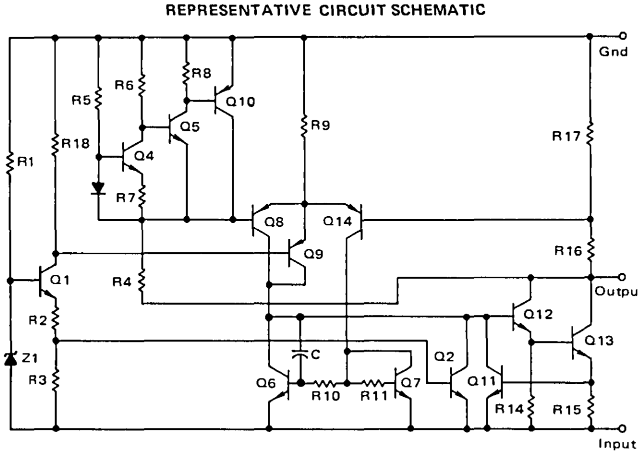
THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC79L00 Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

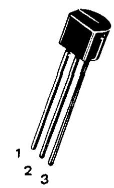
REPRESENTATIVE CIRCUIT SCHEMATIC



Device No. ±10%	Device No. ±5%	Nominal Voltage
MC79L03C	MC79L03AC	−3 0
MC79L05C	MC79L05AC	−5 0
MC79L12C	MC79L12AC	−12
MC79L15C	MC79L15AC	−15
MC79L18C	MC79L18AC	−18
MC79L24C	MC79L24AC	−24

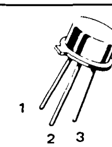
THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

P SUFFIX
CASE 29
TO-92

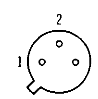


Pin 1. Ground
2. Input
3. Output

G SUFFIX
CASE 79
TO-39



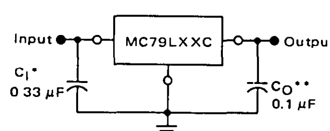
Pin 1. Ground
2. Output
3. Input



(Case connected to pin 3)

Bottom View

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION		
Device	Temperature Range	Package
MC79LXXACG	T_J = 0°C to +150°C	Metal Can
MC79LXXACP	T_J = 0°C to +150°C	Plastic Power
MC79LXXCG	T_J = 0°C to +150°C	Metal Can
MC79LXXCP	T_J = 0°C to +150°C	Plastic Power

XX indicates nominal voltage

MC79L00C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (-3,-5 V) (-12,-15,-18 V) (-24 V)	V_I	-30 -35 -40	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

MC79L03C, AC ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted)

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Characteristic	Symbol	MC79L03C			MC79L03AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-2.76	-3.00	-3.24	-2.88	-3 0	-3 12	Vdc
Input Regulation (T_J = +25°C) -7 0 Vdc ≥ V_I ≥ -20 Vdc -8.0 Vdc ≥ V_I ≥ -20 Vdc	Reg_{line}	 – –	 – –	 80 60	 – –	 – –	 60 40	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 72 36	 – –	 – –	 72 36	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 -2.7 -2.7	 – –	 -3.3 -3.3	 -2.85 -2.85	 – –	 -3.15 -3.15	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.0 5.5	 – –	 – –	 6.0 5.5	mA
Input Bias Current Change -8.0 Vdc ≥ V_I ≥ -20 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 -1 5 -0.2	 – –	 – –	 -1.5 -0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	30	–	–	30	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	10	–	–	10	–	mV/1 0 k Hrs.
Ripple Rejection (-8.0 ≥ V_I ≥ -18 Vdc, f = 120 Hz, T_J = 25°C)	RR	44	51	–	45	51	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I-V_O/$	–	1 7	–	–	1.7	–	Vdc

MC79L05C, AC Series ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L05C Min	MC79L05C Typ	MC79L05C Max	MC79L05AC Min	MC79L05AC Typ	MC79L05AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.6	-5.0	-5.4	-4.8	-5.0	-5.2	Vdc
Input Regulation (T_J = +25°C) -7.0 Vdc ≥ V_I ≥ -20 Vdc -8.0 Vdc ≥ V_I ≥ -20 Vdc	Reg_{line}	 – –	 – –	 200 150	 – –	 – –	 150 100	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 60 30	 – –	 – –	 60 30	mV
Output Voltage -7 0 Vdc ≥ V_I ≥ -20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 -4.5 -4.5	 – –	 -5 5 -5.5	 -4.75 -4.75	 – –	 -5.25 -5 25	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.0 5.5	 – –	 – –	 6.0 5.5	mA
Input Bias Current Change -8.0 Vdc ≥ V_I ≥ -20 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	12	–	–	12	–	mV/1.0 k Hrs.
Ripple Rejection (-8.0 ≥ V_I ≥ 18 Vdc, f = 120 kHz, T_J = 25°C)	RR	40	49	–	41	49	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I-V_O/$	–	1.7	–	–	1.7	–	Vdc

MC79L12C, AC ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted)

Characteristic	Symbol	MC79L12C Min	MC79L12C Typ	MC79L12C Max	MC79L12AC Min	MC79L12AC Typ	MC79L12AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11 1	-12	-12.9	-11.5	-12	-12.5	Vdc
Input Regulation (T_J = +25°C) -14.5 Vdc ≥ V_I ≥ -27 Vdc -16 Vdc ≥ V_I ≥ -27 Vdc	Reg_{line}	 – –	 – –	 250 200	 – –	 – –	 250 200	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1 0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 100 50	 – –	 – –	 100 50	mV
Output Voltage -14.5 Vdc ≥ V_I ≥ -27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -19 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 -10.8 -10 8	 – –	 -13.2 -13.2	 -11.4 -11.4	 – –	 -12 6 -12.6	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change -16 Vdc ≥ V_I ≥ -27 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 1 5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	80	–	–	80	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	24	–	–	24	–	mV/1.0 k Hrs.
Ripple Rejection (-15 ≤ V_I ≤ -25 Vdc, f = 120 Hz, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I-V_O/$	–	1.7	–	–	1.7	–	Vdc

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MC79L15C, AC ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L15C			MC79L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-13.8	-15	-16.2	-14.4	-15	-15.6	Vdc
Input Regulation (T_J = +25°C) -17.5 Vdc ≥ V_I ≥ -30 Vdc -20 Vdc ≥ V_I ≥ -30 Vdc	Reg_{line}	 – –	 – –	 300 250	 – –	 – –	 300 250	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 150 75	 – –	 – –	 150 75	mV
Output Voltage -17.5 Vdc ≥ V_I ≥ -30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -23 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 -13.5 -13.5	 – –	 -16.5 -16 5	 -14.25 -14.25	 – –	 -15.75 -15.75	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change -20 Vdc ≥ V_I ≥ -30 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	–	90	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	30	–	–	30	–	mV/1 0 k Hrs.
Ripple Rejection (-18.5 ≤ V_I ≤ -28.5 Vdc, f = 120 Hz)	RR	33	39	–	34	39	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I-V_O/$	–	1.7	–	–	1.7	–	Vdc

MC79L18C, AC ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 40 mA, C_I = 0 33 µF, C_O = 0 1 µF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-16 6	-18	-19 4	-17 3	-18	-18.7	Vdc
Input Regulation (T_J = +25°C) -20.7 Vdc ≥ V_I ≥ -33 Vdc -21.4 Vdc ≥ V_I ≥ -33 Vdc -22 Vdc ≥ V_I ≥ -33 Vdc -21 Vdc ≥ V_I ≥ -33 Vdc	Reg_{line}	 – – -- --	 – – – –	 – 325 275 –	 – – – –	 – – – –	 325 – – 275	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1 0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 170 85	 – –	 – –	 170 85	mV
Output Voltage -20.7 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA -21 4 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -27 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 – -16 2 -16 2	 – – –	 – -19 8 -19 8	 -17 1 – -17.1	 – – –	 -18.9 – -18.9	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6 5 6.0	 – –	 – –	 6.5 6 0	mA
Input Bias Current Change -21 Vdc ≥ V_I ≥ -33 Vdc -27 Vdc ≥ V_I ≥ -33 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – – –	 – – –	 – 1.5 0.2	 – – –	 – – –	 1 5 – 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	150	–	–	150	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	45	–	–	45	–	mV/1.0 k Hrs.
Ripple Rejection (-23 ≤ V_I ≤ -33 Vdc, f = 120 Hz, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I-V_O/$	–	1.7	–	–	1.7	–	Vdc

MC79L24C, AC ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 40 mA, C_I = 0 33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L24C			MC79L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-22.1	-24	-25.9	-23	-24	-25	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C)								
-27 Vdc ⩾ V_I ⩾ -38 V		–	–	–	–	–	350	
-27.5 Vdc ⩾ V_I ⩾ -38 Vdc		–	–	350	–	–	–	
-28 Vdc ⩾ V_I ⩾ -38 Vdc		–	–	300	–	–	300	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ⩽ I_O ⩽ 100 mA		–	–	200	–	–	200	
1.0 mA ⩽ I_O ⩽ 40 mA		–	–	100	–	–	100	
Output Voltage	V_O							Vdc
-27 Vdc ⩾ V_I ⩾ -38 V, 1 0 mA ⩽ I_O ⩽ 40 mA		–	–	–	-22 8	–	-25.2	
-28 Vdc ⩾ V_I ⩾ -38 Vdc, 1 0 mA ⩽ I_O ⩽ 40 mA		-21.4	–	-26.4	–	–	–	
V_I = -33 Vdc, 1.0 mA ⩽ I_O ⩽ 70 mA		-21 4	–	-26.4	-22.8	–	-25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6 0	
Input Bias Current Change	ΔI_{IB}							mA
-28 Vdc ⩾ V_I ⩾ -38 Vdc		–	–	1.5	–	–	1 5	
1.0 mA ⩽ I_O ⩽ 40 mA		–	–	0.2	–	–	0 1	
Output Noise Voltage (T_A = +25°C, 10 Hz ⩽ f ⩽ 100 kHz)	V_N	–	200	–	–	200	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	56	–	–	56	–	mV/1.0 k Hrs.
Ripple Rejection (-29 ⩽ V_I ⩽ -35 Vdc, f = 120 Hz, T_J = 25°C)	RR	30	43	–	31	47	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I-V_O/$	–	1.7	–	–	1.7	–	Vdc

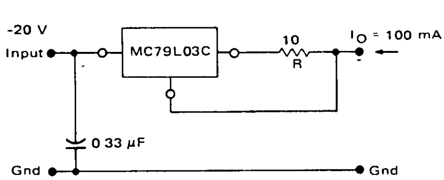
APPLICATIONS INFORMATION

Design Considerations

The MC79L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass

In many low current applications, compensation capacitors are not required However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0 33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

CURRENT REGULATOR

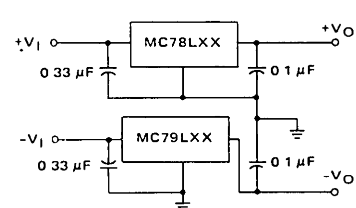


The MC79L03, -3 0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows

$$I_O = \frac{3\,V}{R} + I_B$$

The quiescent current for this regulator is typically 3 8 mA. The -3.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6 0 V below the input voltage

POSITIVE AND NEGATIVE REGULATOR



TYPICAL CHARACTERISTICS

(TA = +25°C unless otherwise noted.)

FIGURE 1 — DROPOUT CHARACTERISTICS

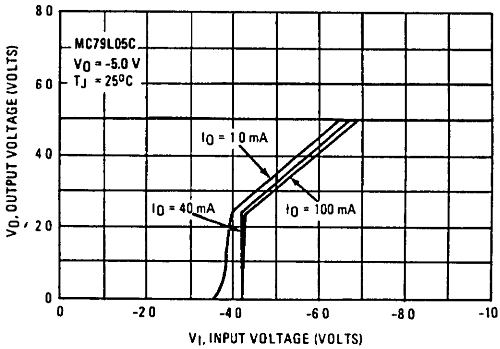


FIGURE 2 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

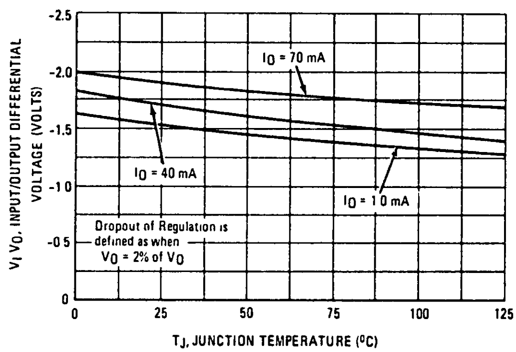


FIGURE 3 — INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

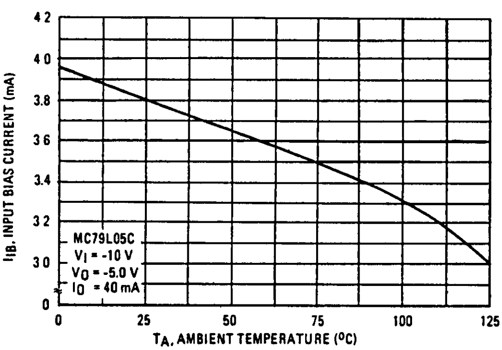


FIGURE 4 — INPUT BIAS CURRENT versus INPUT VOLTAGE

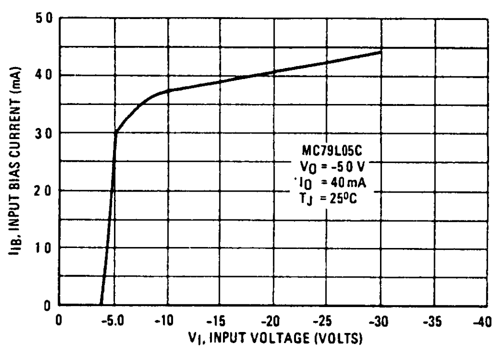


FIGURE 5 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-92 Type Package

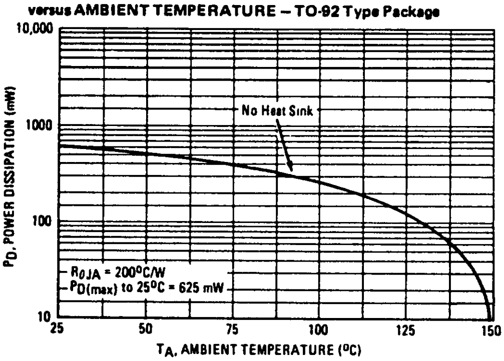
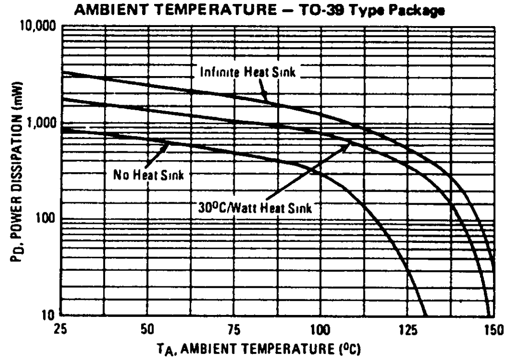


FIGURE 6 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-39 Type Package



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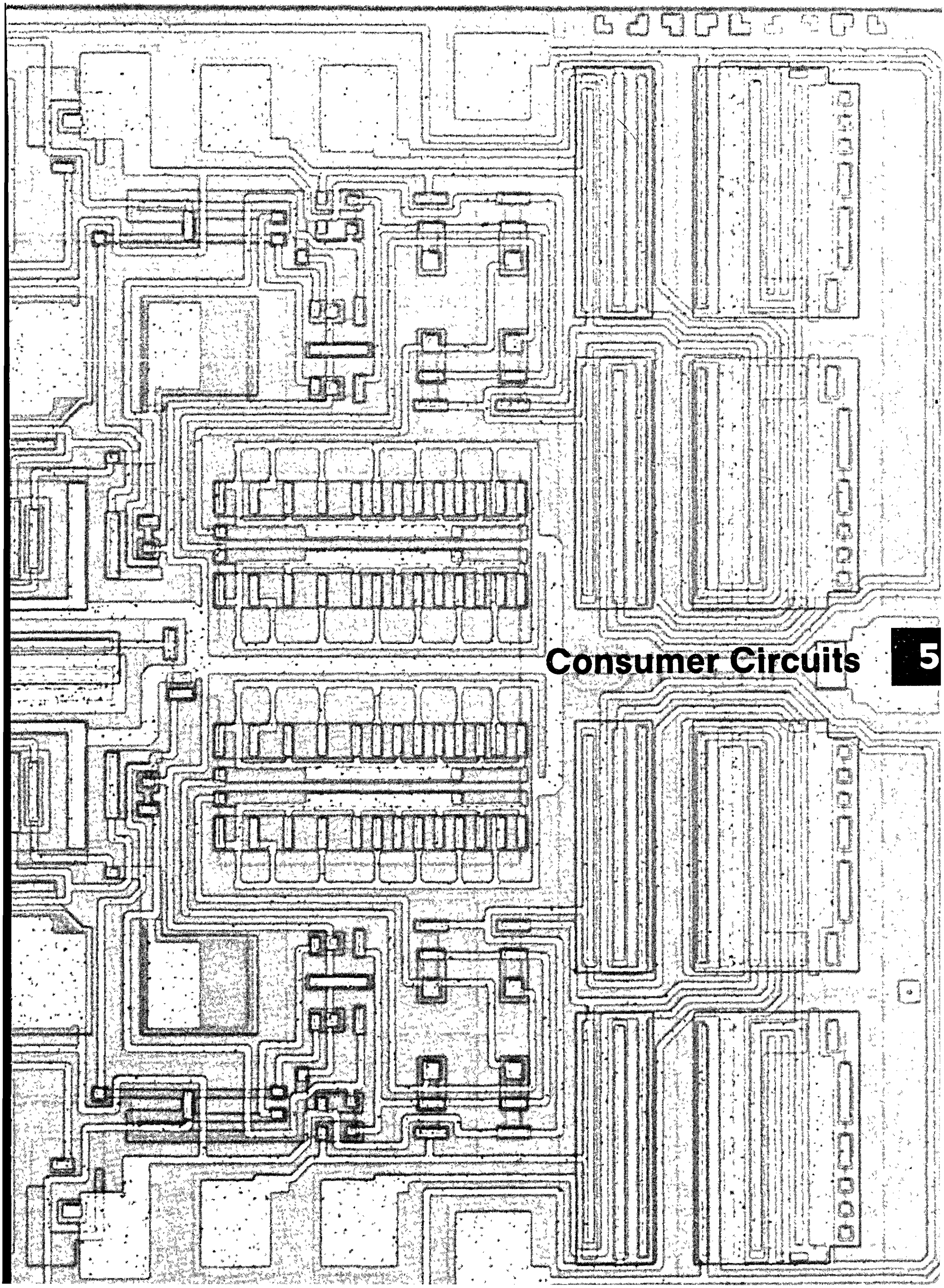

Consumer Circuits

5

CONSUMER CIRCUITS

CIRCUITS FOR CONSUMER APPLICATIONS

... reflecting Motorola's continuing commitment to semiconductor products necessary for consumer system designs. This tabulation is arranged to simplify first-order selection of consumer integrated circuit devices that satisfy the primary functions for Television, Audio, Radio, Citizens Band, Automotive and Organ applications.

Television Circuits

SOUND

Function	Features	Case	Type
Sound IF, Detector, Limiter, Audio Preamplifier	80 μV, 3 dB Limiting Sensitivity, 3.5 V (RMS) Output, Sufficient for Single Transistor Output Stage	646	MC1351
Sound IF Detector	Interchangeable with ULN2111A	646	MC1357
Sound IF Detector, dc Volume Control, Preamplifier	Excellent AMR, Interchangeable with CA3065	646	MC1358
Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier, Power Amplifier	Complete TV Sound System; 100 μV, 3 dB Limiting Sensitivity; 4 Watts Output; V_{CC} = 24 V; R_L = 16 Ω	722A	TDA1190Z
	750 mW Output	648	TDA1190P

VIDEO

Function	Features	Case	Type
1st and 2nd Video IF Amplifier	IF Gain @ 45 MHz = 60 dB typ, AGC Range = 70 dB min	626	MC1349
	IF Gain @ 45 MHz =50 dB typ, AGC Range = 60 dB min	626	MC1350
1st and 2nd Video IF, AGC Keyer and Amplifier	IF Gain @ 45 MHz = 53 dB typ, AGC Range = 75 dB min, "Forward AGC" Provided for Tuner	646	MC1352
3rd IF, Video Detector, Video Buffer, and AFC Buffer	Low-Level Detection, Low Harmonic Generation, Zero Signal dc Output Voltage of 7.0 to 8.2 V	626	MC1330A1
	Same as MC1330A1 except zero signal dc output voltage of 7.8 to 9.0 V	626	MC1330A2
Automatic Fine Tuning	High Gain AFT System, Interchangeable with CA3064	646	MC1364
Automatic Fine Tuning with Intercarrier Mixer/Amplifier	AFT Circuit that Provides an AFT Voltage and an Amplified 4.5 MHz Intercarrier Sound Signal	646	CA3139

CHROMA

Function	Features	Case	Type
Chroma IF Amplifier and Subcarrier System	Includes Complete Chroma IF, AGC, dc Gain and Tint Controls Injection Locked Oscillator, Low Peripheral Parts Count	646	MC1398
Chroma IF Amplifier and Subcarrier System (PLL)	Includes Complete Chroma IF, AGC, dc Chroma and Hue Controls, Phase-Locked Loop (PLL) Oscillator, Color Killer Threshold Adjustment	648	MC1399
Dual Chroma Demodulators	Dual Doubly-Balanced Demodulator with RGB Matrix and Chroma Driver Stages	646	MC1324
	Dual Doubly-Balanced Demodulator with RGB Matrix and PAL Switch	646	MC1327
Triple Chroma Demodulator	Triple Doubly-Balanced Demodulator with Adjustable Output Matrix, Contains Three Independent Demodulators	648	MC1323

DEFLECTION

Function	Features	Case	Type
Horizontal Processor	Includes Linear Balanced Phase Detector, Oscillator and Predriver, Adjustable dc Loop Gain	626	MC1391
	Same as MC1391 except designed to accept negative sawtooth sync pulse	626	MC1394
Vertical Processor	Includes Oscillator and Complementary Driver, Low Thermal Drift, Retrace Pulse for Effective Blanking	648	MC1393A

TV GAMES/DISPLAY

Function	Features	Case	Type
Color TV Video Modulator	Includes Chroma Oscillator and Clock Driver, Lead and Lag Network, Chroma Modulator, RF Oscillator, and Modulator.	646	MC1372
	Includes RF Oscillator and Modulator	626	MC1373

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Audio Circuits

POWER AMPLIFIERS

Features	P_O Watts	V_{CC} Vdc Max	V_{in} @ rated P_O mV Typ	I_D mA Typ	R_L Ohms	Case	Type
Audio Power Amplifiers	0.5	15	3.0	4.0	8.0	626	MC1306
	0.25	12	3.0	3.0	16	626	MC3360
	8.0	28	50	55	2.0	314A, 314B	TDA2002

Radio Circuits

IF AMPLIFIERS

Function	Gain @ 10.7 MHz dB Typ	3 dB Limiting @ 10.7 MHz mV (RMS) typ	AMR dB Typ	Recovered Audio Output f = ±75 kHz mV (RMS)	Power Supply Volts Max	Case	Type
IF Amplifier	58	0.175	60	690	18	626	MC1350
Limiting FM-IF Amplifier	—	0.600	45	480	18	646	MC1355
Limiting IF Ampl/Quad Detector	53	0.4	45	480	16	646	MC1357
IF Amplifier	42	60	50	500	18	626	MC3310
Low-Power FM-IF for Dual Conversion Scanning Receivers	—	0.005	50	350 (f = ±3.0 kHz)	8.0	648	MC3357

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DECODERS

Function	Channel Separation dB Typ	THD % Typ	Stereo—Indicator Lamp Driver mA Max	Features	Case	Type
FM Multiplex Stereo Decoder	47	0.06	50	Coilless Operation; 4.5 V Operation	646	MC1309
	40	0.3	75	Coilless Operation	646	MC1310
	45	0.2	100	Variable Separation	648	TCA4500A

AM RECEIVER

Features	Function	Case	Type
AM Radio Subsystem	RF Amplifier, AGC, Mixer, Oscillator, 1st IF Amplifier, 2nd IF Amplifier and Detector	648	HA1199

Organ Circuits

FREQUENCY DIVIDER

Function	V_{CC} Range Vdc	f_{Tog} MHz Typ	V_{OH} Vdc Min	Case	Type
7-Stage Divider	6–16	1.0	12.0/15.0	646	MC1302

ATTENUATOR

Function	V_{CC} Range Vdc	THD % Typ	A_V dB Typ	Attenuation Range dB Typ	Case	Type
Electronic Attenuator	9.0-18	0.6	13	90	626	MC3340

Automotive Circuits

OPERATIONAL AMPLIFIER

Function	V_{CC} Range Vdc	A_{VOl} V/V Min	I_{IB} μA Max	Unity Gain Bandwidth MHz Typ	Case	Type
Quad Operational Amplifier	4.0-28	1000	0.3	4.0	646	MC3301
	3.0-26	—	0.25	1.0	646	LM2902
Dual Operational Amplifier	3.0-26	—	0.25	1.0	626	LM2904

COMPARATORS

Function	V_{CC} Range Vdc	V_{IO} mV Max	I_{IO} nA Max	I_{IB} nA Max	Sink Current mA Typ	Case	Type
Quad Comparators	2.0-28	±20	—	500	6.0	646, 632	MC3302
	2.0-36	±7.0	±50	250	16.0	646	LM2901
		±5.0				646, 632	LM239
		±2.0				646, 632	LM239A

VOLTAGE REGULATOR

Function	Features	Case	Type
Automotive Voltage Regulator	Designed for use with NPN Darlington; Overvoltage Protection; "Open Sense" Shut Down; Selectable Temperature Coefficient for Use in a Floating Field Alternator Charging System	646	MC3325
Flip-Chip Automotive Voltage Regulator	Same as MC3325	—	MCCF3326

ELECTRONIC IGNITION

Electronic Ignition Circuit	Designed for use in High Energy Variable Dwell Electronic Ignition Systems with Variable Reluctance Sensors. Dwell and Spark Energy are Externally Adjustable	646	MC3333
Flip-Chip Electronic Ignition Circuit	Same as MC3333	—	MCCF3333

SPECIAL FUNCTION

Programmable Frequency Switch (Engine RPM Switch)	Wide Input Frequency Range (10 Hz to 100 kHz) Adjustable Hysteresis Wide Supply Operating Range (7 to 24 V)	646, 632	MC3344

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Transistor Arrays

GENERAL-PURPOSE

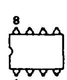
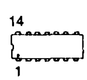
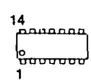
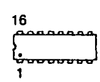
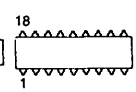
Function	I_C (max) mA	V_{CEO} Volts Max	V_{CBO} Volts Max	V_{EBO} Volts Max	Case	Type
One Differentially Connected pair and Three Isolated Transistors	50	15	20	5.0	646	MC3346 MC3386
Dual Independent Differential Amplifiers with Associated Constant Current Transistors	50	15	20	5.0	646	CA3054

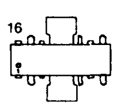
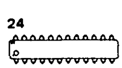
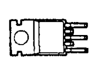
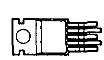
Special Functions

Function	Features	Case	Type
Emitter-Coupled Astable Multivibrator	Useful as DC-DC Converter, Power Regulator or Multivibrator. Toggle Freq = 100 kHz (typ)	626	MC3380
Phase-Locked Loop	Contains Voltage Controlled Oscillator and Double Balanced Phase Detector	646	NE565

5

Package Styles

Lead Configuration					
Case	626	632	646	648	701
Material	Plastic	Ceramic	Plastic	Plastic	Plastic
Suffix after Type Number	P or PL	L	P	P	P

Lead Configuration				
Case	722A	724	314A	314B
Material	Plastic	Plastic	Plastic	Plastic
Suffix after Type Number	P	P	H	V

CA3054

Advance Information

DUAL INDEPENDENT DIFFERENTIAL AMPLIFIER

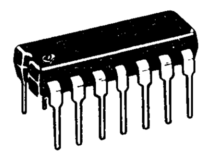
The CA3054 consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six NPN transistors which comprise the amplifiers are general purpose devices useful from dc to 120 MHz.

The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers which makes this device particularly useful in dual channel applications where matched performance of the two channels is required.

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage — ±5 mV

GENERAL PURPOSE TRANSISTOR ARRAY

SILICON MONOLITHIC INTEGRATED CIRCUIT

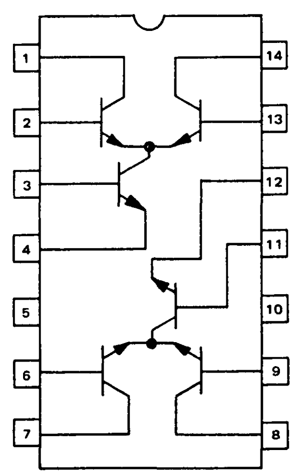


PLASTIC PACKAGE
CASE 646-04
$R_{\theta JA}$ = 100° C/W TYP.
(NO SUFFIX)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current — Continuous	I_C	50	mAdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN CONNECTIONS



Pin 5 is connected to substrate

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER					
Input Offset Voltage (V_{CB} = 3 0 Vdc)	V_{IO}	–	–	5.0	mV
Input Offset Current (V_{CB} = 3 0 Vdc)	I_{IO}	–	–	2.0	μA
Input Bias Current (V_{CB} = 3.0 Vdc)	I_{IB}	–	–	24	μA
STATIC CHARACTERISTICS FOR EACH TRANSISTOR					
Base-Emitter Voltage	V_{BE}				Vdc
(V_{CB} = 3.0 Vdc, I_C = 50 μA)		–	–	0.70	
(V_{CB} = 3.0 Vdc, I_C = 1 0 mA)		–	–	0 80	
(V_{CB} = 3.0 Vdc, I_C = 3.0 mA)		–	–	0.85	
(V_{CB} = 3.0 Vdc, I_C = 10 mA)		–	–	0.90	
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	100	nA
Collector-Emitter Breakdown Voltage (I_C = 1.0 mA)	BV_{CEO}	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μA)	BV_{CBO}	20	–	–	Vdc
Collector-Substrate Breakdown Voltage (I_C = 10 μA)	BV_{CIO}	20	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μA)	BV_{EBO}	5.0	–	–	Vdc

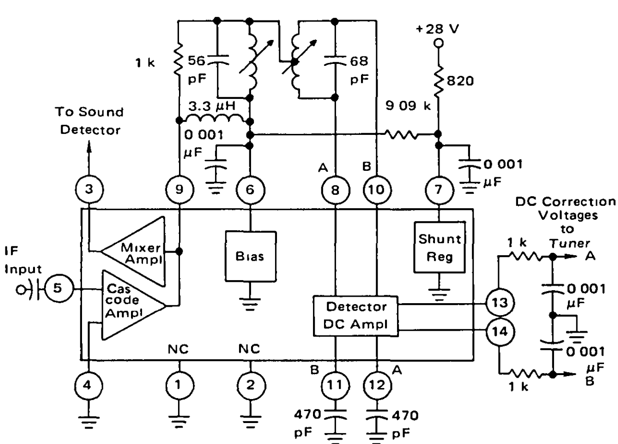
CA3139

TV AUTOMATIC FINE TUNING CIRCUIT WITH INTERCARRIER MIXER/AMPLIFIER

The CA3139 is a monolithic TV Automatic Fine Tuning (AFT) circuit that provides an AFT voltage and an amplified 4.5 MHz intercarrier sound signal. When connected to an output of an IF amplifier the CA3139 provides the signal processing (amplification and detection) necessary to generate the AFT correction signals required by the TV tuner. It also mixes the video and sound IF carriers and amplifies the resultant 4.5 MHz intercarrier sound signal.

- Cascode Type High Gain Amplifier (15 mV input for rated output)
- AFT Differential Peak Detector
- Differential Amplifier
- Bipolar Outputs
- Five Stage Intercarrier Mixer/Amplifier
- Internal Voltage Regulator
- For Use in Either Color or Monochrome Receivers

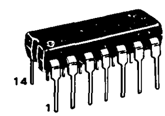
FIGURE 1 — BLOCK DIAGRAM AND TYPICAL APPLICATION



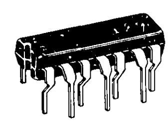
All resistor values are in ohms.

TV AUTOMATIC FINE TUNING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

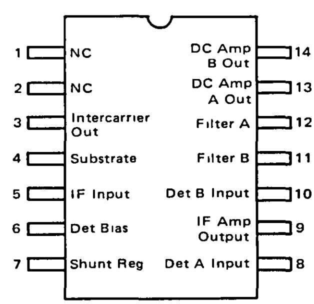


E SUFFIX
PLASTIC PACKAGE
CASE 646



Q SUFFIX
PLASTIC PACKAGE
CASE 647

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
CA3139E	−40 to +85°C	Plastic DIP
CA3139Q	−40 to +85°C	Plastic QIL

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Shunt Regulator Input Current	I_7	50	mA
Detector Bias Current	I_6	2	mA
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 28 Vdc, V_{in} = 0, T_A = 25°C, Test Circuit—Figure 2)*

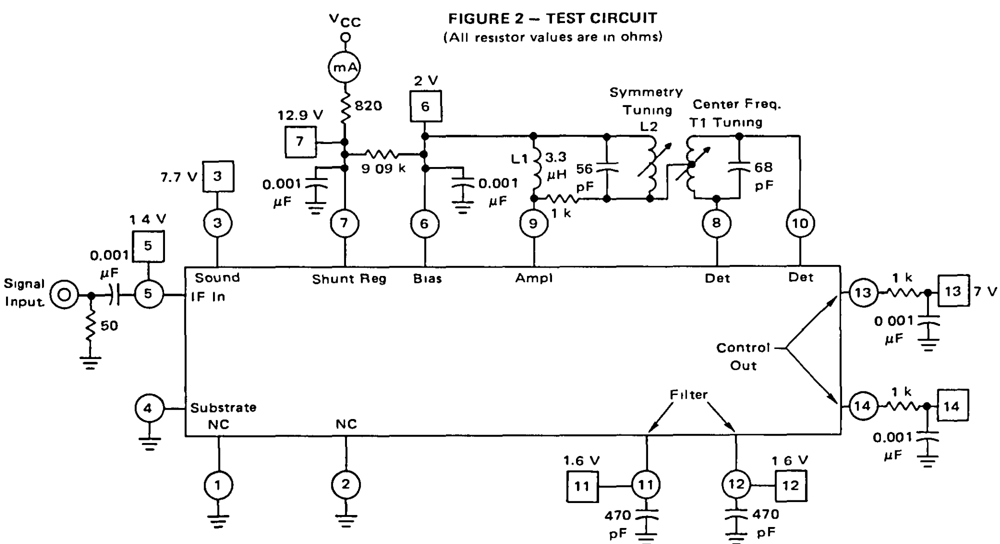
Characteristics		Min	Typ	Max	Unit
Supply Current I+		15	18	20	mA
Shunt Regulator Voltage		12	13	14.5	Vdc
Quiescent Voltage at Pin 3		4.5	7.7	10	V
Quiescent Voltage(1) at Pins 13 and 14. Pins 13 and 14 Connected		6	7	8.5	Vdc
Quiescent Voltage Differential, Pins 13 to 14		-0.8	–	+0.8	Vdc
Quiescent Voltage at Pin 6		1.4	2.3	2.6	Vdc
Correction Voltage at Pin 13 (See Note 2)	f = 44.65 MHz	2.2	–	4.7	Vdc
	f = 45.69 MHz	1.2	–	4.4	
	f = 45.81 MHz	9.6	–	13.8	
	f = 46.85 MHz	9.1	–	12.1	
Correction Voltage at Pin 14 (See Note 2)	f = 44.65 MHz	9.1	–	12.1	Vdc
	f = 44.69 MHz	9.6	–	13.8	
	f = 45.81 MHz	1.2	–	4.4	
	f = 45.85 MHz	2.2	–	4.7	
4.5 MHz Output (See Note 2)	Two-Tone Input f_1 = 45.75 MHz at 15 mV f_2 = 41.25 MHz at 5 mV	50	–	200	mVrms

*Unless otherwise specified.

NOTES: 1. V_{13} = 0.55 V_Z ±0.7 V.

2. Resistor from Pin 6 to Pin 7 = 9.09 kΩ. Crossover steepens and "Bow Tie" width increases when resistor is decreased in value. Total peak swing decreases slightly.

FIGURE 2 — TEST CIRCUIT
(All resistor values are in ohms)



NOTES:

1. Use 10 kΩ Isolation Resistor at dc voltmeter probe tip when making dc measurements
2. Typical no-signal dc potentials are shown.
3. Boxes represent test points.

L2 — 4-1/2 turns #22 wire; O.D. = 0.25" (typ); Q (unloaded) = 100 (min); f = 41.25 MHz; Inductance = 0.18 µH (typ).

T1 — 3-1/2 turns (center tapped) #20 wire; O.D. = 0.25" (typ); Q (unloaded) = 140 (min); f = 46.75 MHz, Inductance = 0.18 µH (typ).

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CIRCUIT DESCRIPTION

The five functional blocks of the CA3139 as shown in Figure 1 are briefly described below.
(See Figure 3 for schematic diagram.)

1. **Cascode Amplifier** – consists of Q1, emitter-follower; Q2, common-emitter amplifier; and Q3, common-base amplifier. The input to the cascode amplifier (pin 5) is normally AC coupled since Q1 is internally biased.

2. **Bias Circuit** – Transistor Q4 and resistors R1, R4, R5, and an external resistor (shown as 9.09 kΩ in Figure 1) connected to pin 7 make up the bias circuit. Lower values of the external resistor will increase the gain of the amplifier (9.1 kΩ is nominal) thereby increasing the AFT "Bow Tie" width and crossover slope (reduced values of the external resistor will have the opposite effect).

3. **Mixer/Amplifier** – The cascode amplifier output (pin 9) is internally connected to the base of Q13. Transistors Q13 through Q17 make up the intercarrier mixer/amplifier. Q14 is used in the down-conversion of the video IF carrier (41.25 MHz) to give a 4.5 MHz FM signal. The video IF carrier, sound IF carrier and upper conversion signals are removed using a low-pass filter. Q16 and C3 are used to further amplify and filter the 4.5 MHz signal. This 4.5 MHz signal output is at pin 3.

4. **AFT Detector and DC Amplifier** – Detection and amplification is accomplished by Q6 through Q12. The detector inputs (pins 8 and 10) are connected to the discriminator transformer and biased through the transformer at pin 6 voltage. Q7 and Q8 total current is held constant by Q10, Q11, and Q12 (current-mirror transistors). Peak detection is assured through the use of external filter capacitors at pins 11 and 12. Correction voltages at pins 13 and 14 are given in the Electrical Characteristics Table.

5. **Voltage Regulator** – consisting of D1, D2, Z1, Z2, and Q5 is an active shunt type and is used to reduce the dynamic resistance.

FIGURE 3 – CIRCUIT SCHEMATIC
(Resistors are measured in ohms)

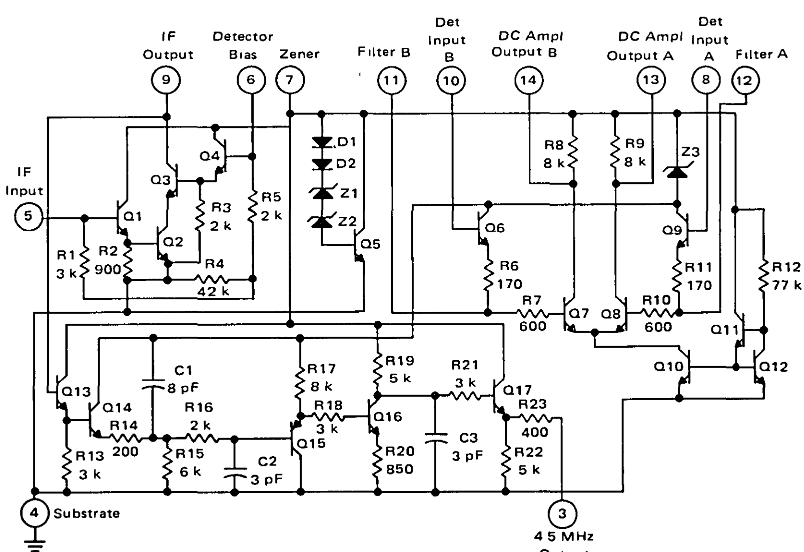

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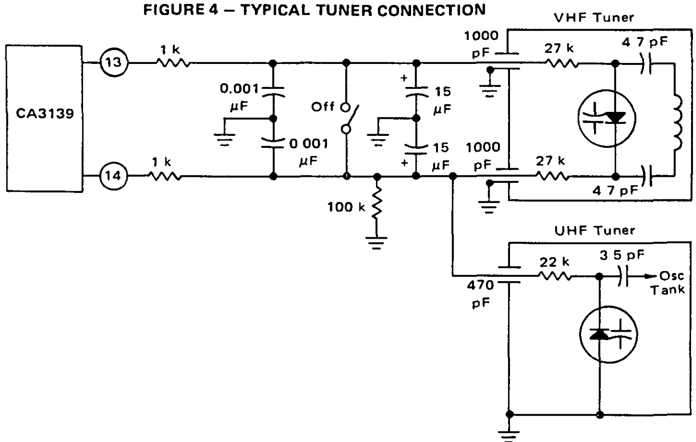
FIGURE 4 – TYPICAL TUNER CONNECTION



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HA1199P

Advance Information

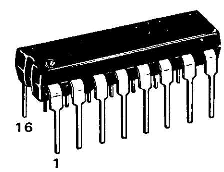
AM SUBSYSTEM FOR CAR RADIO

The HA1199P is a complete one-chip radio subsystem for car radio applications. Automatic dynamic range magnitude control at the RF stage provides good high input signal-handling characteristics (THD = 1% typ at 130 dBμ).

- High AGC FOM — 63 dB Typ
- Good Usable Sensitivity — 23 dBμ Typ
- Low Distortion — 0.4% Typ at 74 dBμ
- Supply Voltage Range — 10.8 to 15.6 Volts

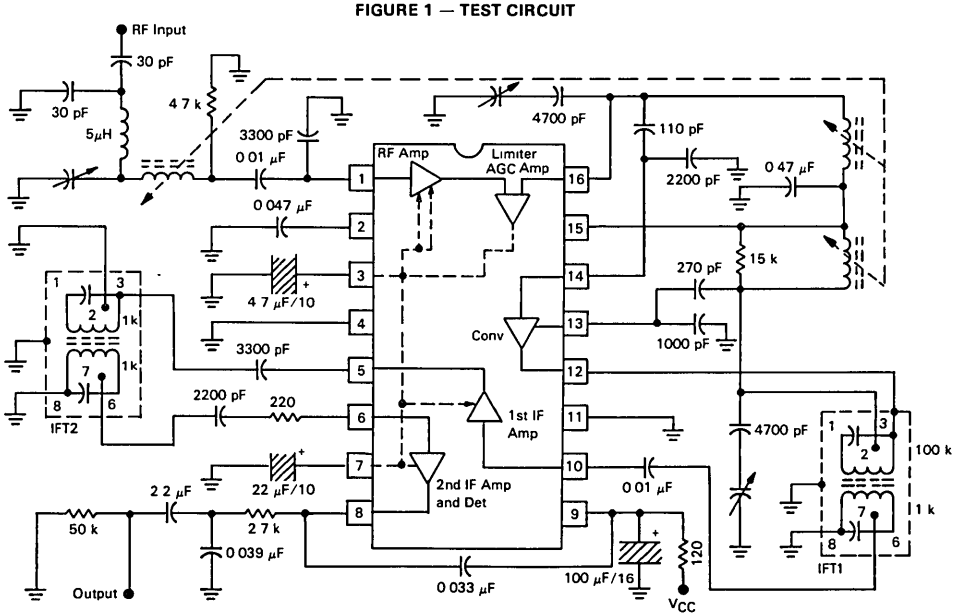
AM RADIO SUBSYSTEM

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 — TEST CIRCUIT



PIN CONNECTIONS

1 RF Amplifier Input	5 First IF Amplifier Output	9 V_{CC}	13 Lo Input
2 RF Bypass	6 Second IF Amplifier Input	10 First IF Amplifier Input	14 Converter Input
3 AGC Bypass	7 AGC Bypass	11 Gnd	15 V_{CC}'
4 Gnd	8 Detector Output	12 Converter Output	16 RF Amplifier Output

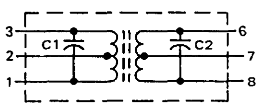
This is advance information and specifications are subject to change without notice

MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage	16	Volts
Junction Temperature	150	°C
Operating Temperature Range (Ambient)	-30 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 13.2 V, f_c = 1.0 MHz, f_{mod} = 400 Hz, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Drain Current at Zero Signal	—	15	—	mA
Signal-to-Noise Ratio Input = 34 dBμ, 30% Modulation	25.5	30	—	dB
AGC FOM Test @ 10 dB Output Down, 30% Modulation 1) Output @ 74 dBμ Input 2) Output @ 86 dBμ Input	 — 51	 57 63	 — —	dB
Detector Output Input = 74 dBμ, 30% Modulation	80	120	157	mV
Distortion Input = 114 dBμ, 30% Modulation	—	0.4	5.0	%
Sensitivity Input @ S/N = 20 dB, 30% Modulation	—	23	—	dBμ



SPECIFICATION OF THE IFTs

	Q0	Number of Turns				C1 (pF)	C2 (pF)	Tuned Frequency (kHz)
		1-2	2-3	6-7	7-8			
First IFT	70	66	220	260	26	180	180	262 5
Second IFT	70	271	23	271	23	180	180	262 5

MC1302

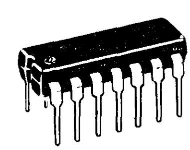
7-STAGE DIVIDER

This monolithic circuit is designed for use as a frequency divider in electronic organs It contains 7 flip-flops with all inputs and outputs externally accessible.

- Wide Operating Voltage Range – 6.0 to 16 Volts
- Regulated Supply Not Required
- Maximum Design Flexibility – Allows for Two to Seven-Stage Cascades

7-STAGE DIVIDER

SILICON MONOLITHIC INTEGRATED CIRCUIT



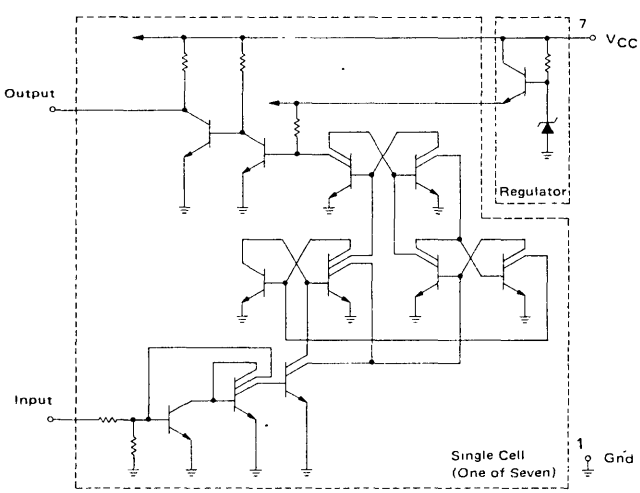
P SUFFIX
PLASTIC PACKAGE
CASE 646

5

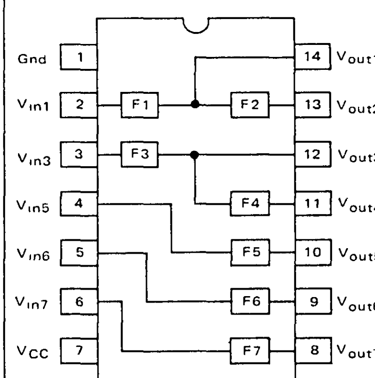
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Volts
Power Supply Voltage	19	Vdc
Output Sinking Current	10	mA
Negative Input Voltage	0 5	Vdc
Junction Temperature	150	°C
Operating Temperature Range	0 to +75	°C

FIGURE 1 – CIRCUIT SCHEMATIC



PIN CONNECTIONS



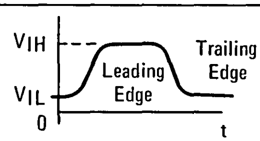
ORDERING INFORMATION

Device	Temperature Range	Package
MC1302P	0 to +75	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 16 Vdc, V_{in} = 4 0 V, Square Pulse, f = 10 kHz, 50% Duty Cycle, t_{PHL} = 1 0 V/µs, T_A = +25°C, unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Operating Power Supply Voltage	6 0	—	16	Vdc
Toggle Frequency	—	1 0	—	MHz
Output Voltage (High) Pins 8, 9, 10, 11, & 13				Vdc
(V_{CC} = 6.0 Vdc)	5 5	—	—	
(V_{CC} = 16 Vdc)	15.0	—	—	
Output Voltage (High) Pins 12 S 14				Vdc
(V_{CC} = 6 0 Vdc)	4.5	—	—	
(V_{CC} = 16 Vdc)	12	—	—	
Operating Drain Current				mAdc
(V_{CC} = 16 Vdc)	—	26	—	
Output Sinking Current				mAdc
(V_O < 0 5 Vdc)	—	10	—	
Rise Time	—	100	—	ns
Propagation Delay	—	700	—	ns
Fall Time	—	50	—	ns
Input Resistance	10	—	—	kΩ
Output Resistance (Output High)	—	—	5 0	kΩ

INPUT PULSE REQUIREMENTS



Characteristic	Min	Max	Unit
Pulse Magnitude	+4 0	—	Volts
Zero Level	—	+1.0	Volts
Leading Edge	No Requirement		
Trailing Edge dv/dt	-1.0	—	Volts/ms

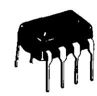
MC1306P

1/2-WATT AUDIO AMPLIFIER

The MC1306P is a monolithic complementary power amplifier and preamplifier designed to deliver 1/2-Watt into a loudspeaker with a 3.0 mV(rms) typical input. Gain and bandwidth are externally adjustable. Typical applications include portable AM-FM radios, tape recorder, phonographs, and intercoms.

- 1/2-Watt Power Output (12 Vdc Supply, 8-Ohm Load)
- High Overall Gain – 3.0 mV(rms) Sensitivity for 1/2-Watt Output
- Low Zero-Signal Current Drain – 4.0 mAdc @ 9.0 V typ
- Low Distortion – 0.5% at 250 mW typ

1/2-WATT AUDIO AMPLIFIER



PLASTIC PACKAGE
CASE 626

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TYPICAL APPLICATIONS

FIGURE 1 – AM-FM RADIO, AUDIO SECTION

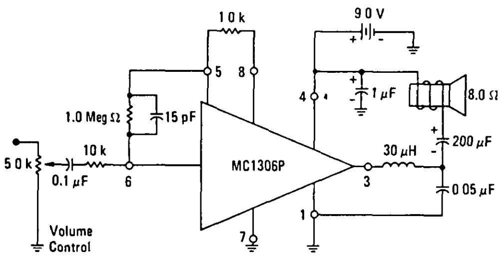
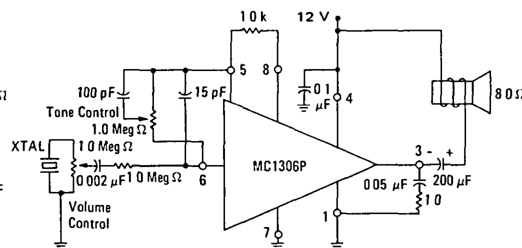
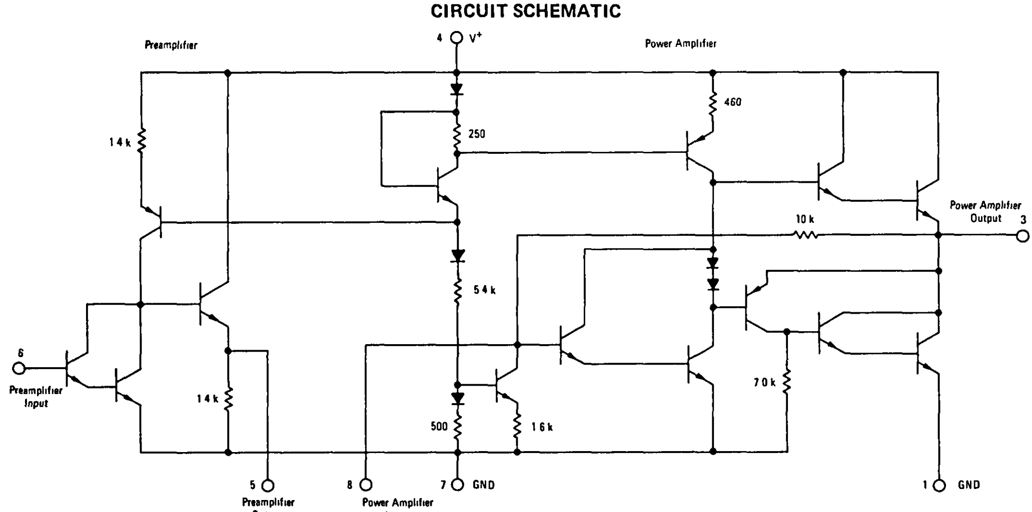


FIGURE 2 – PHONOGRAPH AMPLIFIER (CERAMIC CARTRIDGE)



CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	15	Vdc
Load Current	I_L	400	mAdc
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	P_D $1/\theta_{JA}$	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 9.0 V, R_L = 8.0 ohms, f = 1.0 kHz, (using test circuit of Figure 3), T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Open Loop Voltage Gain Pre-amplifier R_L = 1.0 k ohm Power-amplifier R_L = 16 ohms	A_{VOL}	 – –	 270 360	 – –	V/V
Sensitivity (P_o = 500 mW)	S	–	3.0	–	mV(rms)
Output Impedance (Power-amplifier)	Z_o	–	0.5	–	Ohm
Signal to Noise Ratio (P_o = 150 mW, f = 300 Hz to 10 kHz)	S/N	–	55	–	dB
Total Harmonic Distortion (P_o = 250 mW)	THD	–	0.5	–	%
Quiescent Output Voltage	V_o	–	$V^+/2$	–	Vdc
Output Power (THD ≤10%, V^+ = 12 V)	P_o	500	570	–	mW
Current Drain (zero signal)	I_D	–	4.0	–	mA
Power Dissipation (zero signal)	P_D	–	36	–	mW

FIGURE 3 – TEST CIRCUIT

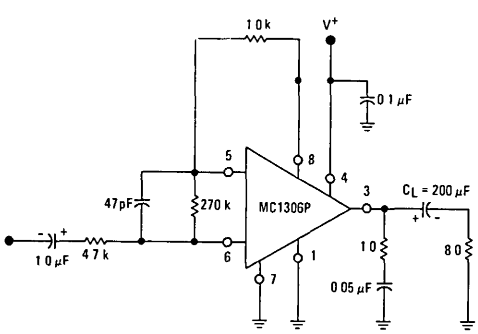
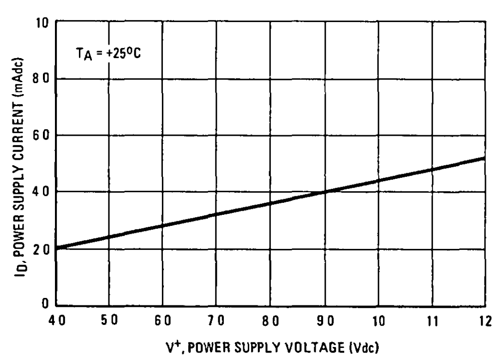


FIGURE 4 – ZERO SIGNAL BIAS CURRENT



TYPICAL CHARACTERISTICS
(V^+ = 9.0 V, f = 1.0 kHz, T_A = +25°C unless otherwise noted)

FIGURE 5 – EFFICIENCY

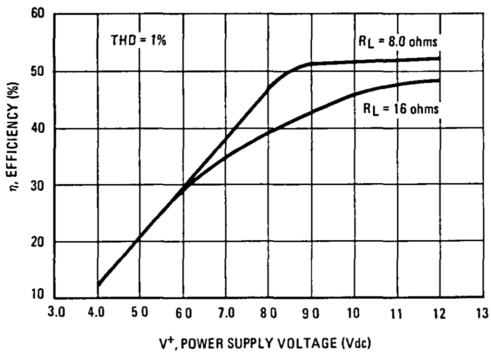


FIGURE 6 – OUTPUT POWER

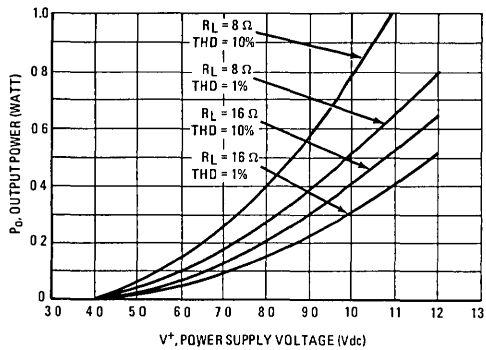


FIGURE 7 – TOTAL HARMONIC DISTORTION

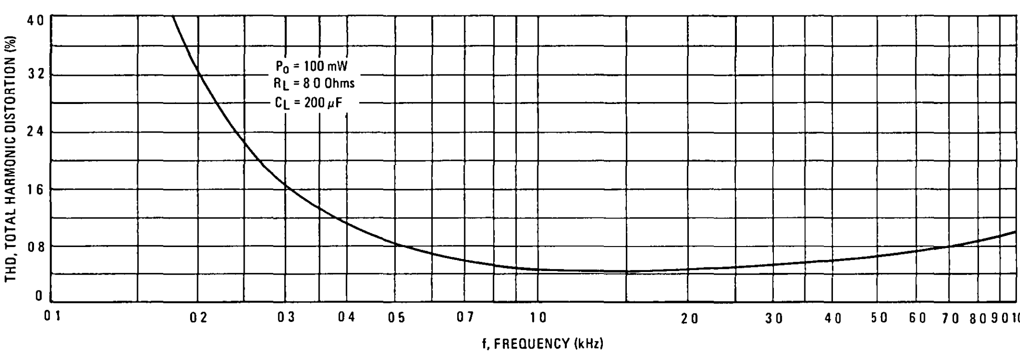


FIGURE 8 – EFFECT OF BATTERY AGING ON LOW-LEVEL DISTORTION

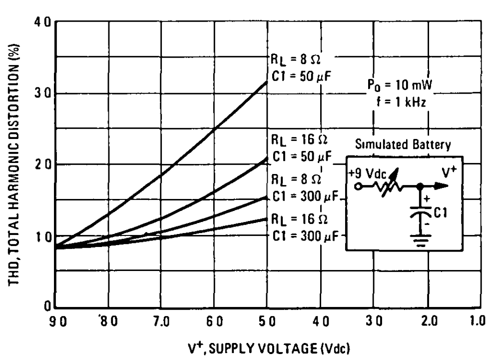


FIGURE 9 – DISTORTION

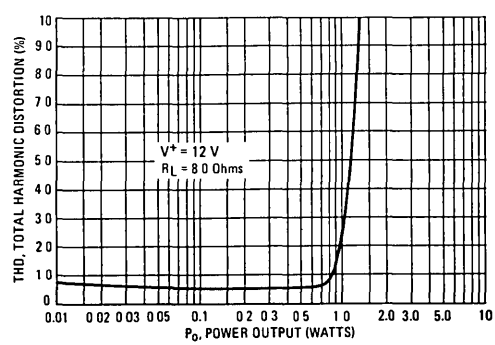


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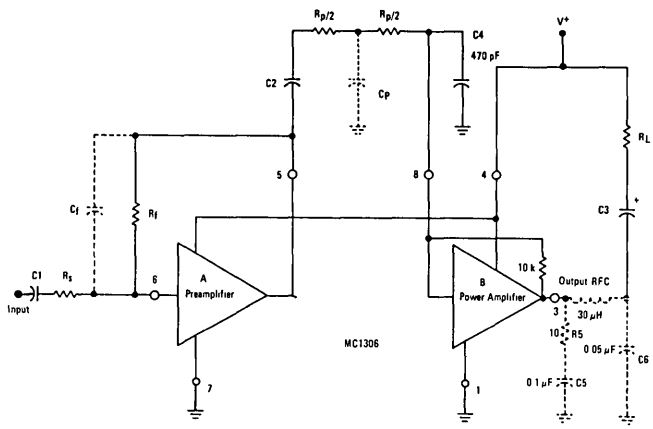
FIGURE 10 – TYPICAL CIRCUIT CONNECTION



DESIGN CONSIDERATIONS

The MC1306P provides the designer with a means to control preamplifier gain, power amplifier gain, input impedance, and frequency response. The following relationships will serve as guides.

1. Gain

The Preamplifier Stage Voltage Gain is:

$$A_{V_A} \approx \frac{R_f}{R_s}$$

and is limited only by the open-loop gain (270 V/V). For good preamplifier dc stability R_f should be no larger than 1.0-megohm.

The Power Amplifier Voltage Gain is controlled in a similar manner where.

$$A_{V_B} \approx \frac{10\text{ k}}{R_p}$$

The 10-k ohm feedback resistor is provided in the integrated circuit.

Recommended values of R_p range from 500-ohms to 3.3-k ohms. The low end is limited primarily by low-level distortion and the upper end is limited due to the voltage drive capabilities of the pre-amplifier. (A resistor can be added in the dc feedback loop, from pin 6 to ground, to increase this drive). The Overall Voltage Gain, then, is:

$$A_{VT} = \frac{R_f\ 10\text{ k}}{R_s\ R_p}$$

2. Input Impedance

The Preamplifier Input Impedance is:

$$Z_{in\,A} \approx R_s$$

and the Power Amplifier Input Impedance is:

$$Z_{in\,B} \approx R_p$$

3. Frequency Response

The low frequency response is controlled by the cumulative effect of the series coupling capacitors C1, C2, and C3. High-frequency response can be determined by the feedback capacitor, C_f, and the -3.0 dB point occurs when

$$X_{C_f} = R_f$$

Additional high frequency roll-off and noise reduction can be achieved by placing a capacitor from the center point of R_p to ground as shown in Figure 10.

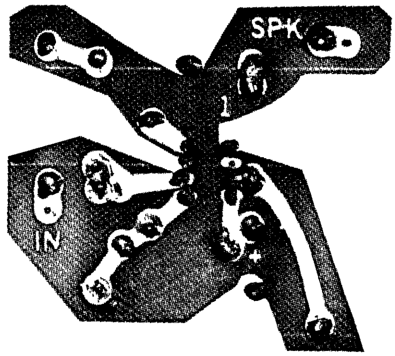
Capacitor C4 and the RC network shown in dotted lines may be needed to prevent high frequency parasitic oscillations. The RF choke, shown in series with the output, and capacitor C6 are used to prevent the high-frequency components in a large-signal clipped audio output waveform from radiating into the RF or IF sections of a radio (Figure 10).

4. Battery Operation

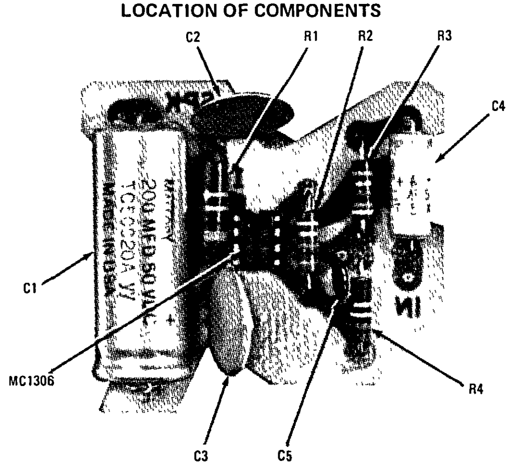
The increase of battery resistance with age has two undesirable effects on circuit performance. One effect is the increasing of amplifier distortion at low signal levels. This is readily corrected by increasing the size of the filter capacitor placed across the battery (as shown in Figure 8; a 300-µF filter capacitor gives distortions at low-tonal levels that are comparable to the "stiff" supply). The second effect of supply impedance is a lowering of power output capability for steady signals. This condition is not correctable, but is of questionable importance for music and voice signals.

5. Application Examples: (1) The audio section of the AM-FM radio (Figure 1) is adjusted for a preamplifier gain of 100 with an input impedance of 10-k ohms. The power amplifier gain is set at 10, which gives an overall voltage gain of 1000. The bandwidth has been set at 10-kHz. (2) The phono amplifier (Figure 2) is designed for a preamplifier gain of unity and a power amplifier gain of 10. The input impedance is 1.0-megohm. An adjustable treble control is provided within the feedback loop.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT



LOCATION OF COMPONENTS



See Figure 3 for schematic diagram.

PARTS LIST

Component	Value
C1	200 µF
C2	0.1 µF
C3	0.05 µF
C4	1.0 µF
C5	47 pF
R1	1 ohm
R2	1 k ohm
R3	4.7 k ohms
R4	270 k ohms
MC1306	–
PC Board	–

5

MC1309

Advance Information

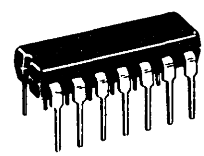
PHASE LOCK LOOP FM STEREO DEMODULATOR

. . . a monolithic device using I^2L and ION Implant technology for use in solid-state stereo receivers.

- Requires No Inductors
- Low External Part Count
- Excellent Channel Separation Without Adjustment
- Only Single Potentiometer Oscillator Frequency Adjustment Necessary
- 50 mA Lamp or LED Driving Capability With Current Limiting
- Automatic, Transient-Free Stereo/Mono Switching
- Wide Dynamic Range: 0.25-1.7 V(p-p) Composite Input Signal
- Wide Supply Range: 4.5-16 Vdc
- Low Distortion: Typically 0.08% at 850 mV(p-p) Composite Input Signal
- Excellent SCA Rejection
- Gain Adjustable By Changing Load Resistors

PHASE LOCK LOOP FM STEREO DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

5

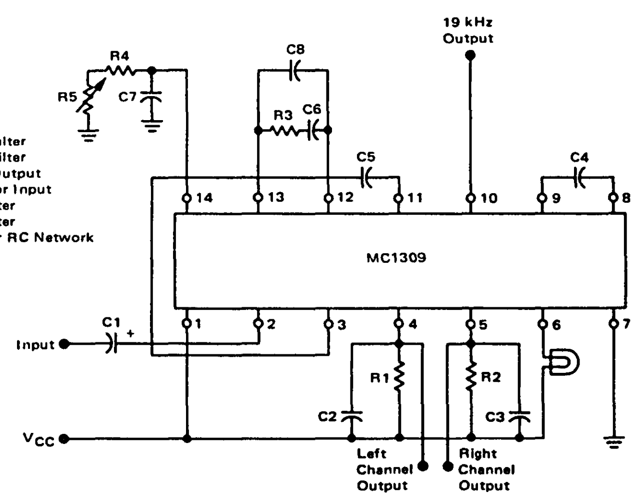
FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT

Pin Functions

Pin 1 = V_{CC}	Pin 8 = Switch Filter
Pin 2 = Input	Pin 9 = Switch Filter
Pin 3 = Amplifier Output	Pin 10 = 19 kHz Output
Pin 4 = Left Channel Output	Pin 11 = Modulator Input
Pin 5 = Right Channel Output	Pin 12 = Loop Filter
Pin 6 = Lamp Indicator	Pin 13 = Loop Filter
Pin 7 = Ground	Pin 14 = Oscillator RC Network

Parts List

C1 = 2.0 μF	C8 = 0.25 μF
C2 = 0.022 μF	R1 = 3.3 kΩ
C3 = 0.022 μF	R2 = 3.3 kΩ
C4 = 0.25 μF	R3 = 1.0 kΩ
C5 = 0.05 μF	R4 = 16 kΩ
C6 = 0.5 μF	R5 = 5.0 kΩ
C7 = 470 pF	



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = +25° unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	16	Volts
Lamp Current	50	mA
Junction Temperature	150	°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS Unless otherwise noted; V_{CC} = +9 Vdc, T_A = +25°C, 1.7 V(p-p) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 10% pilot level for stereo tests: 1.7 V(p-p) 1 kHz input signal for monaural tests; using circuit in Figure 1.

Characteristic	Min	Typ	Max	Unit
Current Drain	–	11	–	mAdc
Maximum Standard Composite Input Signal (0.5% THD)*				$V_{(p-p)}$
(V_{CC} = 9.0 V)	1.7	2.1	–	
(V_{CC} = 6.0 V)	0.85	1.7	–	
Maximum Monaural Input Signal (1.0% THD)*				$V_{(p-p)}$
(V_{CC} = 9.0 V)	1.7	2.2	–	
(V_{CC} = 6.0 V)	0.85	1.7	–	
Channel Balance	–	0	1.0	dB
Stereo THD (V_{in} = 0.85 V[p-p])	–	0.06	–	%
Monaural THD (V_{in} = 0.85 V[p-p]	–	0.08	–	%
Channel Separation				dB
(f = 100 Hz)	–	45	–	
(f = 1.0 kHz)	30	47	–	
(f = 10 kHz)	–	40	–	
Monaural Gain	0.6	0.9	–	V/V
Input Impedance	15	30	–	kΩ
Ultrasonic Frequency Rejection 19 kHz	–	35	–	dB
38 kHz	–	45	–	
SCA Rejection	–	75	–	dB
Stereo Switch Level				mV
Lamp "On"	–	9.0	12	
Lamp "Off"	2.0	4 5	–	
Mono/Stereo Switching Transient – No Lamp	–	0	–	mV
Capture Range (Pilot = 60 mV[RMS])	–	±7.0	–	%

*THD and Channel Separation are measured after a Bandpass Filter (200 Hz-10 kHz), unless otherwise specified.

5

ORDERING INFORMATION

Device	Temperature Range	Package
MC1310P	−40°C to +85°C	Plastic DIP

MC1310

Specifications and Applications Information

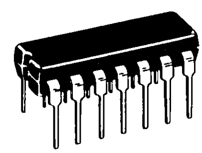
FM STEREO DEMODULATOR

. . . a monolithic device designed for use in solid-state stereo receivers.

- Requires no Inductors
- Low External Part Count
- Only Oscillator Frequency Adjustment Necessary
- Integral Stereo/Monaural Switch 75 mA Lamp Driving Capability
- Wide Dynamic Range: 0.5–2.8 V(p-p) Composite Input Signal
- Wide Supply Range: 8–14 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range
- Low Distortion: Typically 0.3% THD at 560 mV (RMS) Composite Input Signal
- Excellent SCA Rejection

FM STEREO DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



CASE 646

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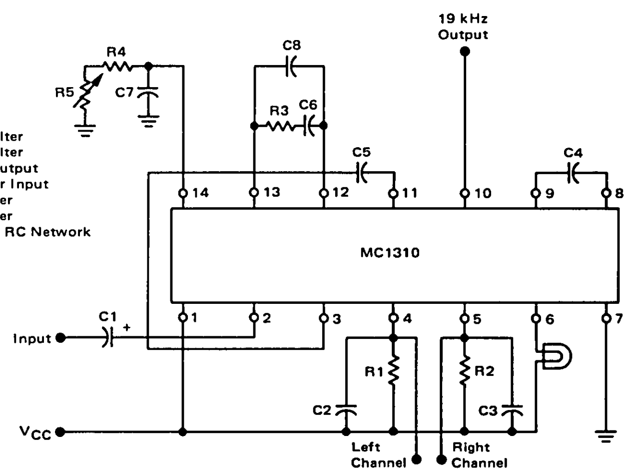
FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT

Pin Functions

Pin 1 = V_{CC}	Pin 8 = Switch Filter
Pin 2 = Input	Pin 9 = Switch Filter
Pin 3 = Amplifier Output	Pin 10 = 19 kHz Output
Pin 4 = Left Channel Output	Pin 11 = Modulator Input
Pin 5 = Right Channel Output	Pin 12 = Loop Filter
Pin 6 = Lamp Indicator	Pin 13 = Loop Filter
Pin 7 = Ground	Pin 14 = Oscillator RC Network

Parts List

C1 = 2.0 µF	C8 = 0.25 µF
C2 = 0.02 µF	R1 = 3.9 kΩ
C3 = 0.02 µF	R2 = 3.9 kΩ
C4 = 0.25 µF	R3 = 1.0 kΩ
C5 = 0.05 µF	R4 = 16 kΩ
C6 = 0.5 µF	R5 = 5.0 kΩ
C7 = 470 pF	



MAXIMUM RATINGS (T_A = +25° unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	14	Volts
Lamp Current	75	mA
Power Dissipation (Package limitation)	625	mW
Derate above T_A = +25°C	5.0	mW/°C
Operating Temperature Range (Ambient)	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS Unless otherwise noted, V_{CC} = +12 Vdc, T_A = +25°C, 560 mV(RMS) (2.8 $V_{(p-p)}$) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1

Characteristic	Min	Typ	Max	Unit
Maximum Standard Composite Input Signal (0.5% THD)	2.8	–	–	$V_{(p-p)}$
Maximum Monaural Input Signal (1.0% THD)	2.8	–	–	$V_{(p-p)}$
Input Impedance	20	50	–	kΩ
Stereo Channel Separation	30	40	–	dB
Audio Output Voltage (desired channel)	–	485	–	mV(RMS)
Monaural Channel Balance (pilot tone "off")	–	–	1.5	dB
Total Harmonic Distortion	–	0.3	–	%
Ultrasonic Frequency Rejection 19 kHz	–	34.4	–	dB
38 kHz	–	45	–	
Inherent SCA Rejection (f = 67 kHz; 9.0 kHz beat note measured with 1.0 kHz modulation "off")	–	75	–	dB
Stereo Switch Level				mV(RMS)
19 kHz input level for lamp "on"	–	–	20	
19 kHz input level for lamp "off"	5.0	–	–	
Capture Range (permissible tuning error of internal oscillator, reference circuit values of Figure 1)	–	±3.5	–	%
Current Drain (lamp "off")	–	13	–	mAdc

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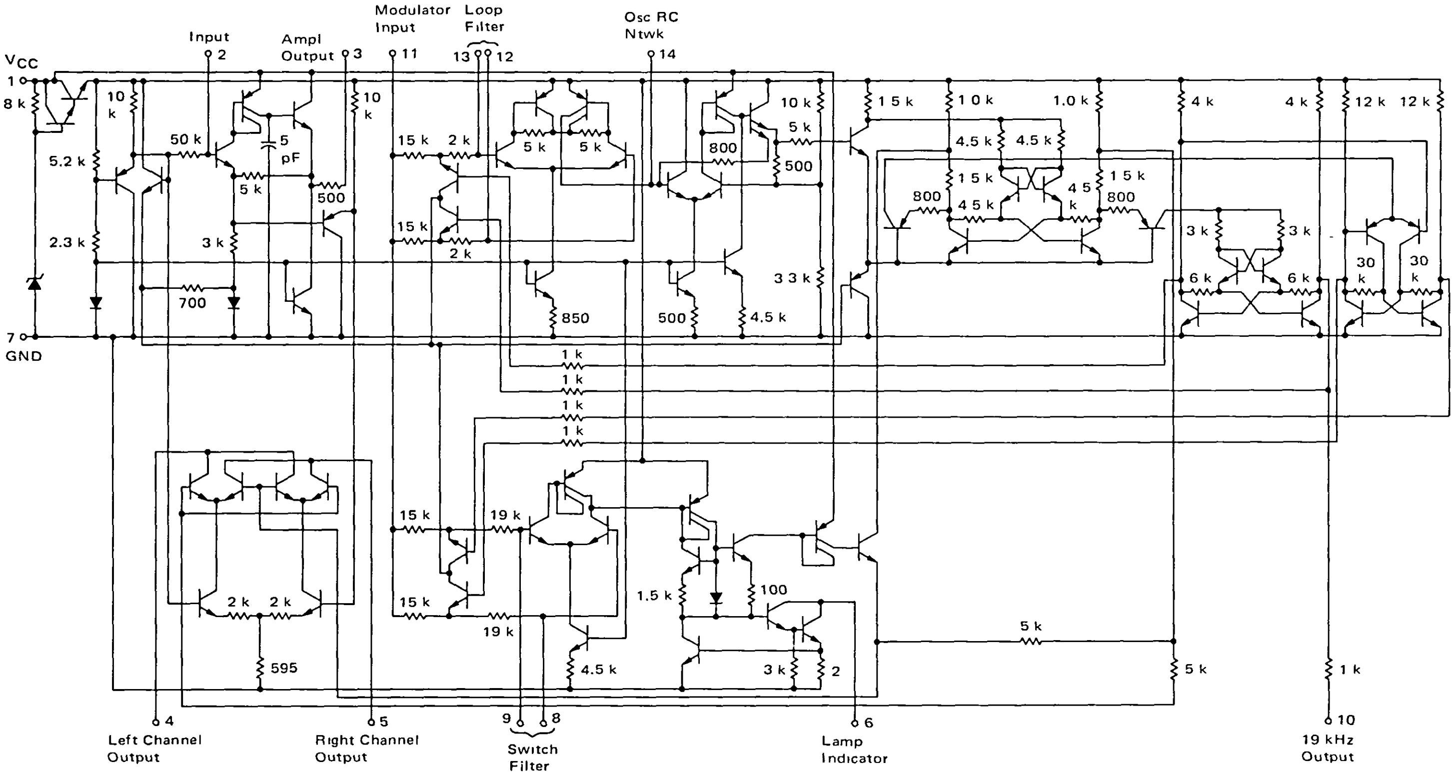
FIGURE 2 – CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

Unless otherwise noted: V_{CC} = +12 Vdc, T_A = +25°C, 560 mV(RMS) (2.8 $V_{[p\text{-}p]}$) standard multiplex composite signal with L or R channel only modulated at 1 0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

FIGURE 3 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL

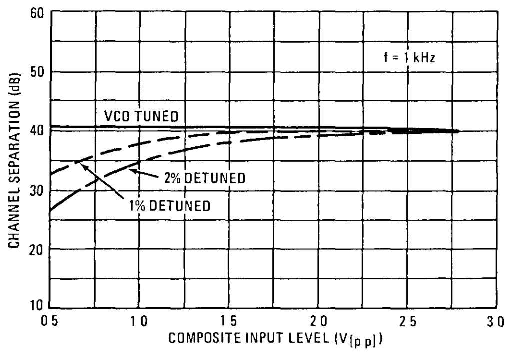


FIGURE 4 – CHANNEL SEPARATION versus FREQUENCY

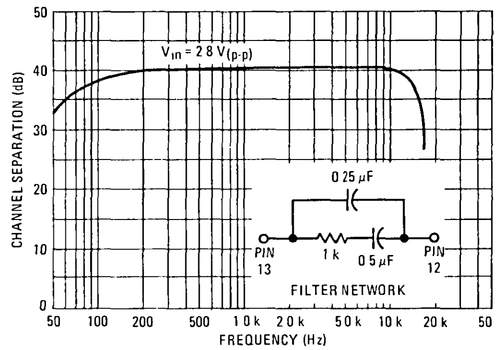


FIGURE 5 – CHANNEL SEPARATION versus VCO FREE-RUNNING FREQUENCY

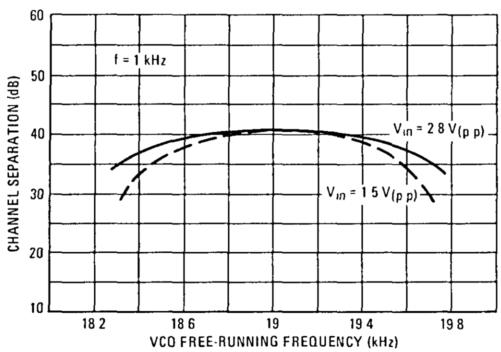


FIGURE 6 – CHANNEL SEPARATION versus SUPPLY VOLTAGE

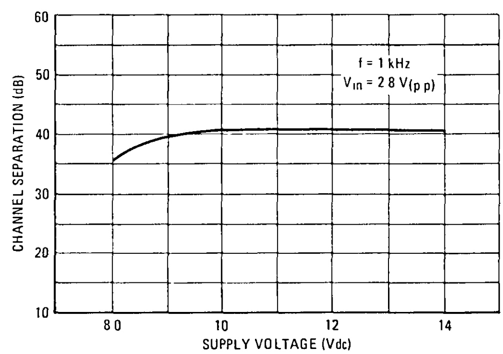


FIGURE 7 – THD versus COMPOSITE INPUT LEVEL*

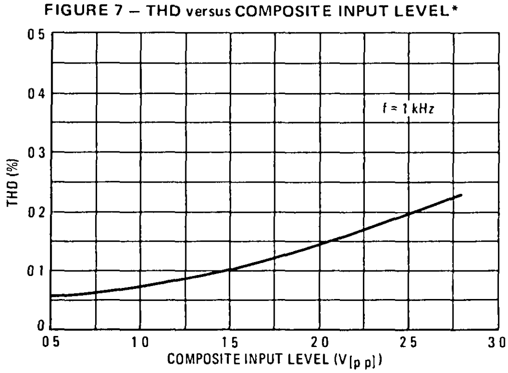
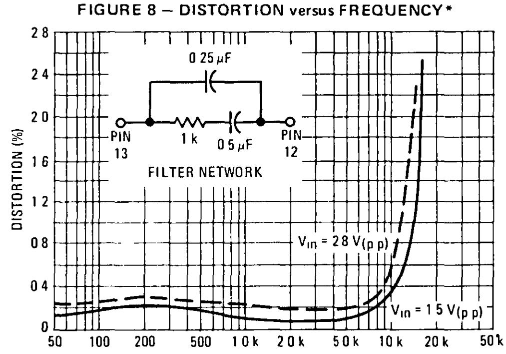


FIGURE 8 – DISTORTION versus FREQUENCY*



*Measured with Low Pass Filter (BW = 15 kHz).

TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DISTORTION versus FREQUENCY*

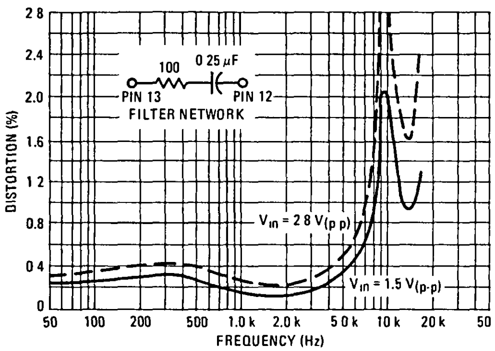


FIGURE 10 – VCO FREE-RUNNING FREQUENCY versus TEMPERATURE

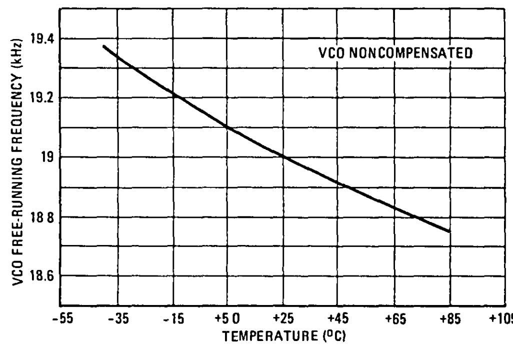
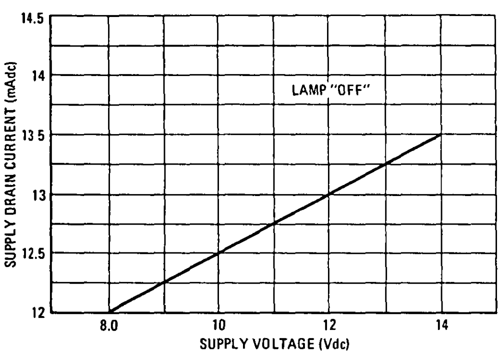


FIGURE 11 – CURRENT DRAIN versus SUPPLY VOLTAGE



*Measured with Low Pass Filter (BW = 15 kHz)

FIGURE 12 – PILOT LEVEL REQUIRED FOR VCO LOCKUP versus VCO FREE-RUNNING FREQUENCY

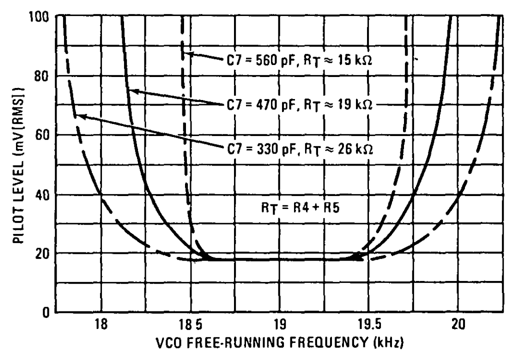
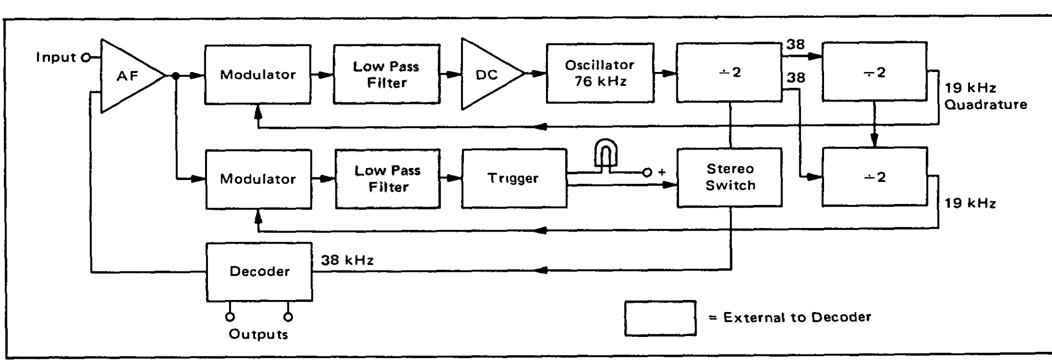


FIGURE 13 – SYSTEM BLOCK DIAGRAM



CIRCUIT OPERATION

Figure 13, on the previous page, shows the system block diagram. The upper line, comprising the 38-kHz regeneration loop operates as follows: the internal oscillator running at 76-kHz and feeding through two divider stages returns a 19-kHz signal to the input modulator. There the returned signal is multiplied with the incoming signal so that when a 19-kHz pilot tone is received a dc component is produced. The dc component is extracted by the low pass filter and used to control the frequency of the internal oscillator which consequently becomes phase-locked to the pilot tone. With the oscillator phase-locked to the pilot the 38-kHz output from the first divider is in the correct phase for decoding a stereo signal. The decoder is essentially another modulator in which the incoming signal is multiplied by the regenerated 38-kHz signal. The regenerated 38-kHz signal is fed to the stereo decoder via an internal switch, which closes when a sufficiently large 19 kHz pilot tone is received.

The 19-kHz signal returned to the 38-kHz regeneration loop modulator is in quadrature with the 19-kHz pilot tone when the loop is locked. With the third divider state appropriately connected, a 19-kHz signal in phase with the pilot tone is generated. This is multiplied with the incoming signal in the stereo switch modulator yielding a dc component proportional to the pilot tone amplitude. This component after filtering is applied to the trigger circuit which activates both the stereo switch and an indicator lamp.

APPLICATIONS INFORMATION

(Component numbers refer to Figure 1)

External Component Functions and Values

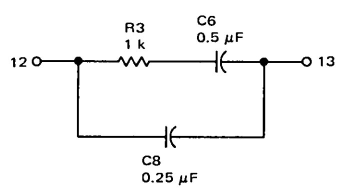
C1 — Input coupling capacitor; 2.0 µF is recommended but a lower value is permissible if reduced separation at low frequencies is acceptable.

R1, R2, C2, C3 — See Maximum Load Resistance section.

C4 — Filter capacitor for stereo switch level detector; time constant is C4 x 53 kilohms ±30%, maximum dc voltage appearing across C4 is 0.25 V (pin 8 positive) at 100 mV(RMS) pilot level. The signal voltage across C4 is negligible.

C5 — See Phase Compensation section.

R3, C6, C8 — Phase-locked loop filter components; the following network is recommended.



When less performance is required a simpler network consisting of R3 = 100 ohms and C6 = 0.25 µF may be used (omit C8). See Figure 9.

R4, R5, C7 — Oscillator timing network; recommended values:

C7 = 470 pF	1%	
R4 = 16 kΩ	1%	
R5 = 5 kΩ	Preset	

These values give ±3.5% typical capture range. Capture range may be increased by reducing C7 and increasing R4, R5 proportionally but at the cost of increasing beat-note distortion (due to oscillator-phase jitter) at high-signal levels. See Figure 12.

Stereo Lamp — Nominal rating up to 75 mA at 12 V; the circuit includes surge limiting which restricts cold-lamp current to approximately 250 mA.

19-kHz Output — A buffer output providing a 3.0-V_{pk} square wave at 19 kHz is available at pin 10. A frequency counter may be connected to this point to measure the oscillator free-running frequency for alignment. See Alignment section.

External Monaural/Stereo Switching

If it is desired to maintain the circuit in monaural mode, the following procedure must be followed. First, the stereo switch must be disabled to prevent false lamp triggering. This can be accomplished by connecting pin 8 negative or pin 9 positive by 0.3 volt. Pin 8 may be grounded directly if desired Note that the voltage across C4 increases to approximately 2 volts with pin 9 positive when pin 8 is grounded.

Second, the 76-kHz oscillator must be killed to prevent interference when on AM. This can be accomplished by connecting pin 14 to ground via a current limiting resistor (3.3 kilohms is recommended).

Phase Compensation/IF Roll-off Compensation

Phase-shifts in the circuit cause the regenerated 38-kHz sub-carrier to lead the original 38 kHz by approximately 2°. The coupling capacitor C5 generates an

APPLICATIONS INFORMATION (continued)

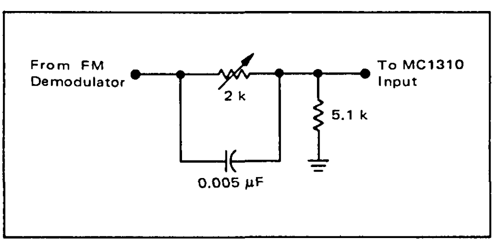
additional lead of 3.5° (for C5 = 0.05 μF) giving a total lead of 5.5°.

The circuit is so designed that phase lag may be generated by adding a capacitor from pin 3 to ground. The source resistance at this point is 500 ohms. A capacitance of 820 pF compensates the 5.5° phase lead: increase above this value causes the regenerated subcarrier to lag the original. However, a 5.5° phase error if left noncompensated will not degrade separation appreciably.

Note that these phase shifts occur within the phase-locked loop and affect only the regenerated 38-kHz sub-carrier: the circuit causes no significant phase or amplitude variation in the actual stereo signal prior to decoding.

Most IF amplifiers have a frequency response that limits separation to a value significantly lower than the capability of the MC1310. For example, if the response produces a 1-dB roll-off at 38 kHz, the separation will be limited to about 32 dB. This error can be compensated by using an RC lead network as shown in Figure 14. The exact values will be determined by the IF amplifier design. However, the values shown in Figure 14 are suitable for use with the MC1357 and MC1375 IF amplifiers.

FIGURE 14 – IF COMPENSATION NETWORK



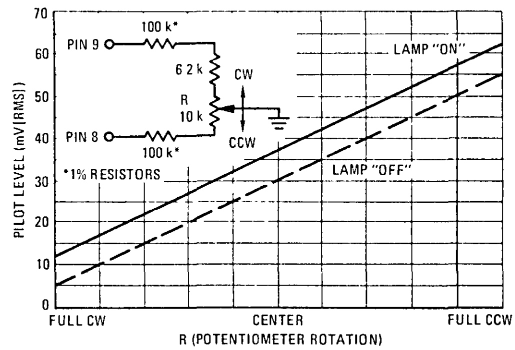
Voltage Control Oscillator Compensation

Figure 10 illustrates noncompensated Oscillator Drift versus temperature. The recommended T_C of the R4, R5, C7 combination is -300 PPM. This will hold the oscillator drift to approximately ±1% over a temperature range of -40 to +85°C. Allowing ±2% for aging of the timing components acceptable performance is still obtained.

Lamp Sensitivity

It may be desirable in some cases, to change the lamp sensitivity due to differing signal levels produced by various FM detectors. The lamp sensitivity can be changed by making use of the external circuit shown. Typical sensitivities versus potentiometer rotation are also shown in Figure 15.

FIGURE 15 – PILOT SENSITIVITY versus POTENTIOMETER ROTATION



Alignment Procedure

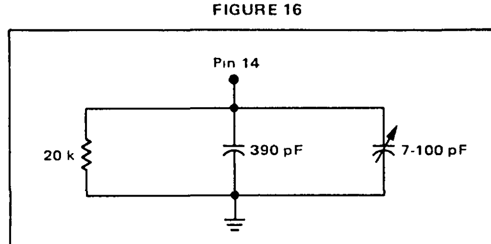
The optimum alignment procedure, with no input signal applied, is to adjust R5 until 19.00 kHz is read at pin 10 on the frequency counter.

Another procedure requiring no equipment, other than the receiver itself, will result in separation of within a few dB of optimum. This latter method is merely to tune the receiver to a stereo broadcast and adjust R5 until the pilot lamp turns "on". To find the center of the lock-in range, rotate the potentiometer back and forth until the center of the lamp "on" range is found. This completes the alignment.

Alternate Timing Network

The alternate timing network shown, incorporating a trimmer capacitor rather than a potentiometer, may be used if desired. Again, to provide correct temperature compensation, the temperature coefficient of the timing network must be approximately -300 PPM.

FIGURE 16

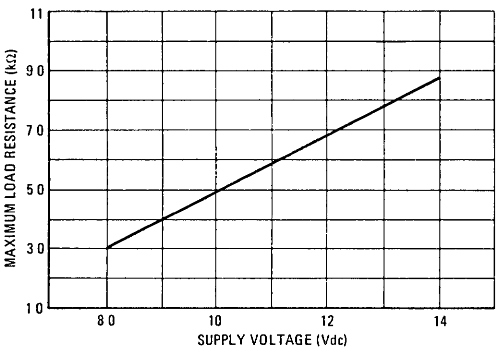


Maximum Load Resistance

The curve shown gives absolute maximum load resistance values versus supply voltage used for full-signal handling capability. With desired load resistance choose C2, C3 capacitors to provide standard 75 μs de-emphasis.

APPLICATIONS INFORMATION (continued)

FIGURE 17 – MAXIMUM LOAD RESISTANCE versus SUPPLY VOLTAGE



Audio Output

The ratio $G = \frac{\text{p-p audio output (one-channel)}}{\text{p-p input signal}}$ for different types of input is as follows:

INPUT

Single-Channel Composite Signal	Monaural Signal
0.45	0.5

These figures are for 3.9-kilohm load resistors and for low-audio frequencies where de-emphasis roll-off is insignificant.

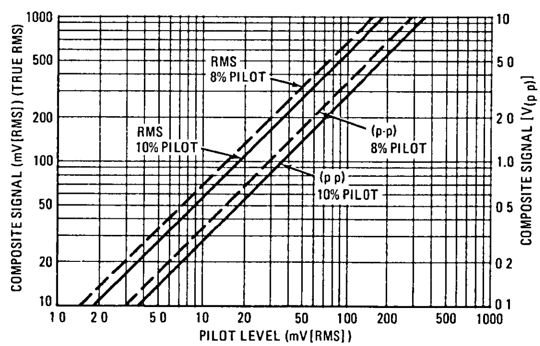
Capture Range versus Timing Components

The capture range can be changed to some extent by use of different timing components. Typical values are shown in Figure 12.

Composite Signal

Due to confusion concerning the measurement of the stereo composite signal, a curve showing both RMS and p-p composite levels versus pilot level follows, see Figure 18.

FIGURE 18 – COMPOSITE LEVEL versus PILOT (L or R Modulation Only)



ORDERING INFORMATION

Device	Temperature Range	Package
MC1323P	0°C to +75°C	Plastic DIP
MC1323PW	0°C to +75°C	Heat Spreader Plastic DIP

MC1323P
MC1323PW

TRIPLE DOUBLY BALANCED CHROMA DEMODULATOR WITH ADJUSTABLE OUTPUT MATRIX

. . . designed for use in solid-state color television receivers. May be used in any conventional color picture tube application.

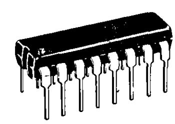
For next generation single-gun color picture tube applications, the MC1323P/PW features three independent demodulators with each gain adjustable with no change to dc output levels.

The MC1323PW package is suited for higher power, higher ambient temperature applications.

- Low Differential Output DC Offset Voltage – < 500 mV (Max)
- Complete Freedom in Choice of Demodulation Axes
- High Blue Output Voltage Swing – 10 V(p-p) (Typ)
- Guaranteed Chroma Sensitivity – 450 mV(p-p) (Max)
- Brightness Input Provided
- Blanking Input Provided
- Circuit Regulated – 16 to 22 V Operating Window
- Power Dissipation @ T_A = 25°C –
  P_D = 2.2 W – MC1323PW
  = 1.25 W – MC1323P

TRIPLE DOUBLY BALANCED CHROMA DEMODULATOR WITH ADJUSTABLE OUTPUT MATRIX

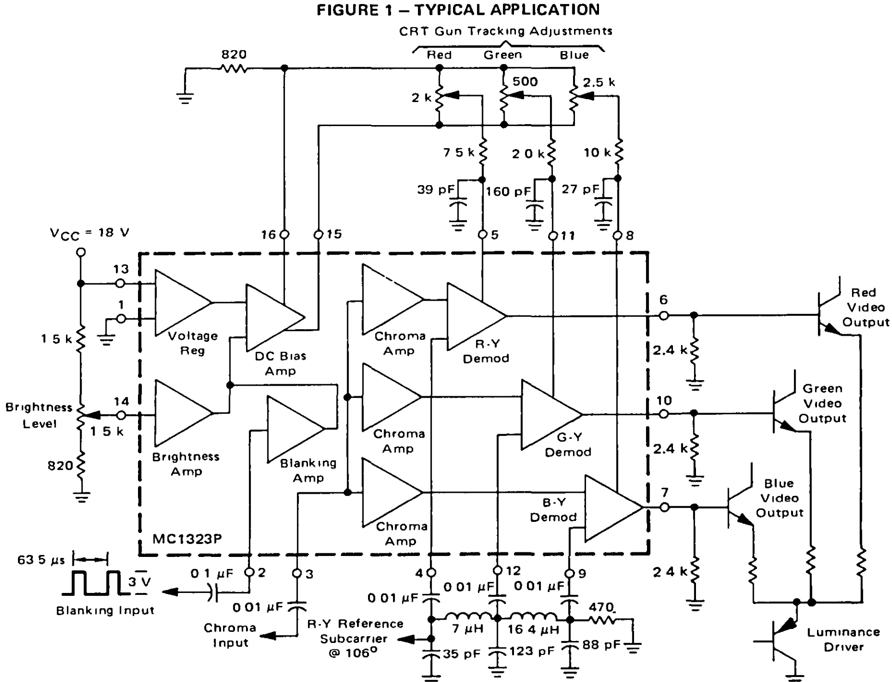
SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

5

FIGURE 1 – TYPICAL APPLICATION



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	MC1323P	MC1323PW	Unit
Power Supply Voltage	22		Vdc
Blanking Signal Input Voltage	6 0		V(p-p)
Minimum Load Resistance (Pins 6,7,10)	2 2		kΩ
Brightness Input Range – Max Min	10.7 4 5		Vdc
Operating Ambient Temperature Range	0 to +75		°C
Storage Temperature Range	-65 to +150		°C
Power Dissipation @ T_A = 25°C Derate above +25°C	1 25 10	2.2 17	W mW/°C

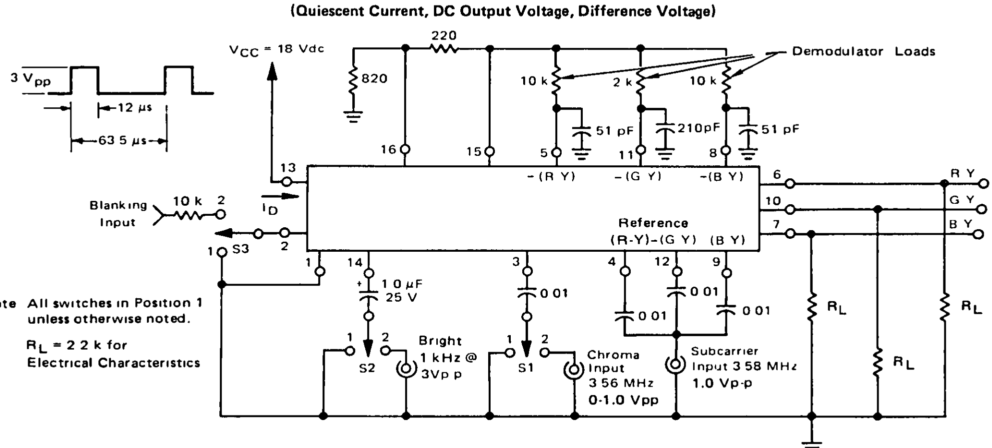
THERMAL CHARACTERISTICS

Characteristic	Max	Unit
Thermal Resistance, Junction to Ambient MC1323PW	59	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = +18 Vdc, R_L = 2 2 kΩ, V_{REF} = 1 0 V(p-p), T_A = +25°C unless otherwise noted.)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS (Figure 2) S1, S2, and S3 in Position 1)					
Quiescent Input Current From Supply	13	–	37	–	mA
Quiescent Output Voltage	6,7,10	9.8	10 8	11.8	Vdc
Differential Output Voltage	6-7,7-10,6-10	–	200	500	mVdc
Differential Voltage	15,16	1.5	1 65	–	Vdc
Pin 15 Output Voltage	15	10 6	11 3	12	Vdc
DYNAMIC CHARACTERISTICS (Figure 2)					
Chroma Input Voltage (Pin 6 Output = 5 V(p-p) S1 in Position 2)	3	–	0.35	0 45	V(p-p)
Detected Output Voltage (Pin 6 Output = 5 V(p-p) S1 in Position 2	7 10	4 6 0.92	5 0 1.0	5 4 1 08	V(p-p) V(p-p)
Blanking Output Voltage (S3 in Position 2)	6,7,10	5 2	5.4	5 6	V(p-p)
Maximum Output Voltage Swing (S1 in Position 2)	6	–	10	–	V(p-p)
Brightness Output Swing (S2 in Position 2)	6,7,10	2.9	–	–	V(p-p)

FIGURE 2 – TEST CIRCUIT WITH REFERENCE INPUT SIGNAL
(Quiescent Current, DC Output Voltage, Difference Voltage)



Note All switches in Position 1 unless otherwise noted.

R_L = 2 2 k for Electrical Characteristics

CIRCUIT DESCRIPTION

The MC1323P is a doubly balanced chroma demodulator that offers several novel features. Three separate independent demodulator sections are used to obtain the (R-Y), (B-Y) and (G-Y) outputs allowing complete freedom in the choice of demodulation axes and individual demodulator conversion gain.

The (R-Y) demodulator is shown in Figure 10 (both (B-Y) and (G-Y) are similar), and is a conventional doubly balanced circuit. The chroma input, which is common to all three demodulators, is applied at Pin 3 to the balanced pair Q15, Q16, which are evenly dividing the 1 mA bias current from the current source Q14. The upper switching pairs Q17, Q18, Q19 and Q20 are driven with approximately 1 Vpp of reference subcarrier applied at Pin 4. If the subcarrier at Pin 4 has a relative angle of 109^{o}, then the output from the switching pairs will be the desired (R-Y) signal. Similarly, for the (B-Y) demodulator, the reference phase at Pin 9 is approximately 3^{o}. To avoid unnecessarily wide phase shift networks to provide the 256^{o} reference phase for the (G-Y) demodulator, the chroma input is phase reversed and the reference angle becomes 76^{o} at Pin 12.

The demodulator is unique in the manner in which the demodulated signals are connected to the output pins. Instead of feeding load resistors returned to the supply voltage rail, the collectors of Q17, Q19 are coupled to the current mirror Q21, Q22, Q23. At balance, with no chroma input signal, Q17, Q19 current (mirrored in Q23) matches Q18, Q20 and the net current at Pin 5 is zero. If a load resistor is connected from Pin 5 to some convenient voltage source, the base of Q25 will be at that voltage regardless of the size of load resistor. Therefore, the conversion gain of the demodulator (defined by the size of the resistor at Pin 5) can be easily changed, yet changes in gain do not result in a change of the dc voltage level at the demodulator output (Pin 6). The ability to change gain, together with a complete choice of demodulation axes, allows the designer to compensate for non-standard CRT phosphors, different color temperatures, and allows easy implementation of automatic hue or color level control circuits.

In order to provide temperature stability of the output dc levels, a reference voltage for the load resistors (Pins 5, 8, and 11) is supplied at Pin 15 with a nominally zero TC. Since the demodulator output dc levels are defined by the voltage source to which the load resistors are returned, another voltage source is provided at Pin 16 and is approximately 1.5 volts lower than Pin 15. Returning the load resistors to the wiper arms of potentiometers connected between Pins 15 and 16 will allow the output dc level of each demodulator to be changed independently over a 1.5 V range. If the potentiometers have a comparatively low resistance compared to the load resistors, negligible change in ac gain will occur with wiper arm rotation and the dc shift can be used to help set up the picture tube grey scale tracking. The voltage source at Pin 16 is obtained by providing a temperature compensated current in Q5 emitter load. This current is "mirrored" in Q8, producing the 1.5 V difference between the bases of Q11 and Q12.

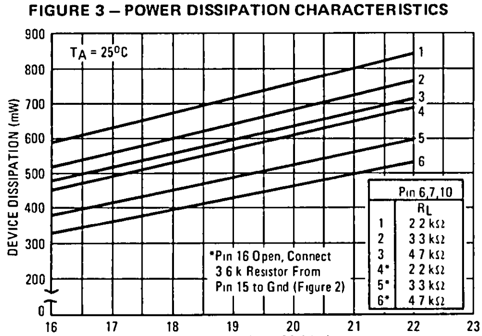
The brightness input at Pin 14 allows the dc output level of all three demodulators to be changed and is a convenient point for a brightness control or brightness range/brightness limiter function.

Output blanking during retrace is achieved by applying a +3 V pulse at Pin 2 (Q13 base). The outputs become clamped to Q2 emitter voltage preventing the demodulator upper pairs from becoming saturated during blanking and giving a very well defined blanking pulse amplitude.

TYPICAL DESIGN CHARACTERISTICS (V_{CC} = +18 Vdc, R_L = 2 2 kΩ, V_{REF} = 1 0 V(p-p), T_A = +25^{o}C)

Characteristic	Pin No.	Min	Typ	Max	Unit
Output Voltage Temperature Coefficient (Reference Input Voltage = 1.0 V(p-p), T_A = +25 to +75^{o}C)	6,7,10	–	1.5	–	mV/^{o}C
Chroma Input Voltage	3	–	1 8	–	Vdc
Reference Input Voltage	4,9,12	–	3 2	–	Vdc
Brightness Input Voltage	14	–	9 2	–	Vdc
Differential Blanking Output Voltage (S3 in Position 2)	6-7,7-10,6-10	–	200	–	mV(p-p)

FIGURE 3 – POWER DISSIPATION CHARACTERISTICS



TYPICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted. Refer to Figure 2 except where noted.)

FIGURE 4 – DEMODULATOR GAIN LINEARITY AND TOTAL HARMONIC DISTORTION CHARACTERISTICS

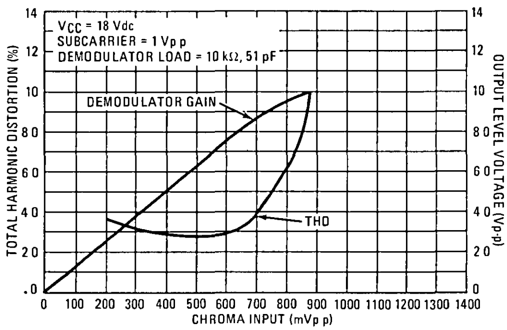


FIGURE 5 – CHROMA BANDWIDTH

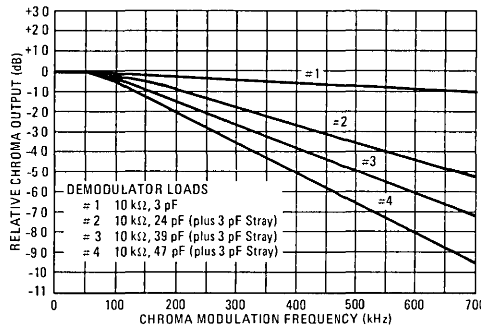


FIGURE 6 – DETECTED OUTPUT VOLTAGE

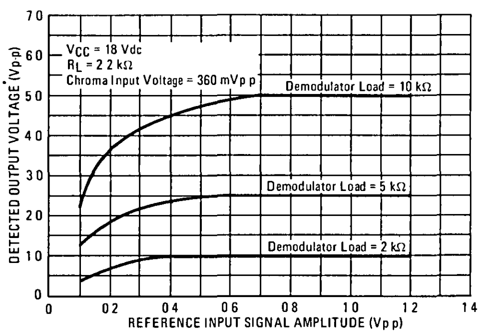


FIGURE 7 – DETECTED OUTPUT VOLTAGE versus SUPPLY VOLTAGE

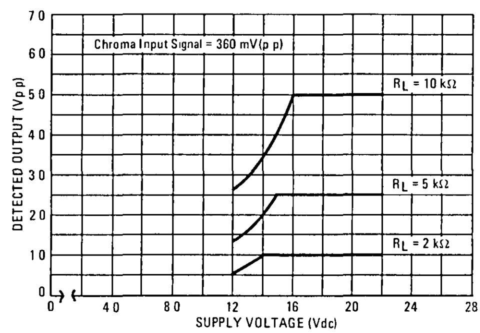


FIGURE 8 – DC OUTPUT VOLTAGE versus LUMINANCE INPUT

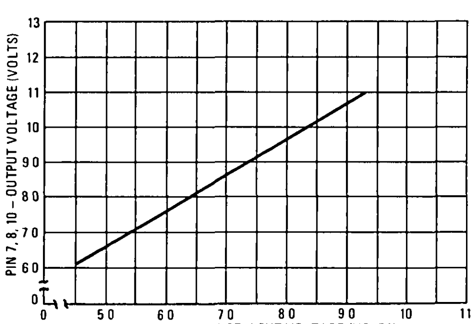


FIGURE 9 – DC OUTPUT VOLTAGE versus SUPPLY VOLTAGE

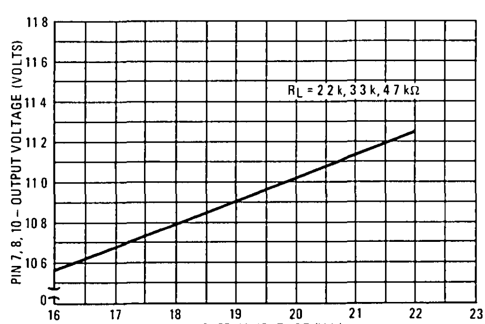
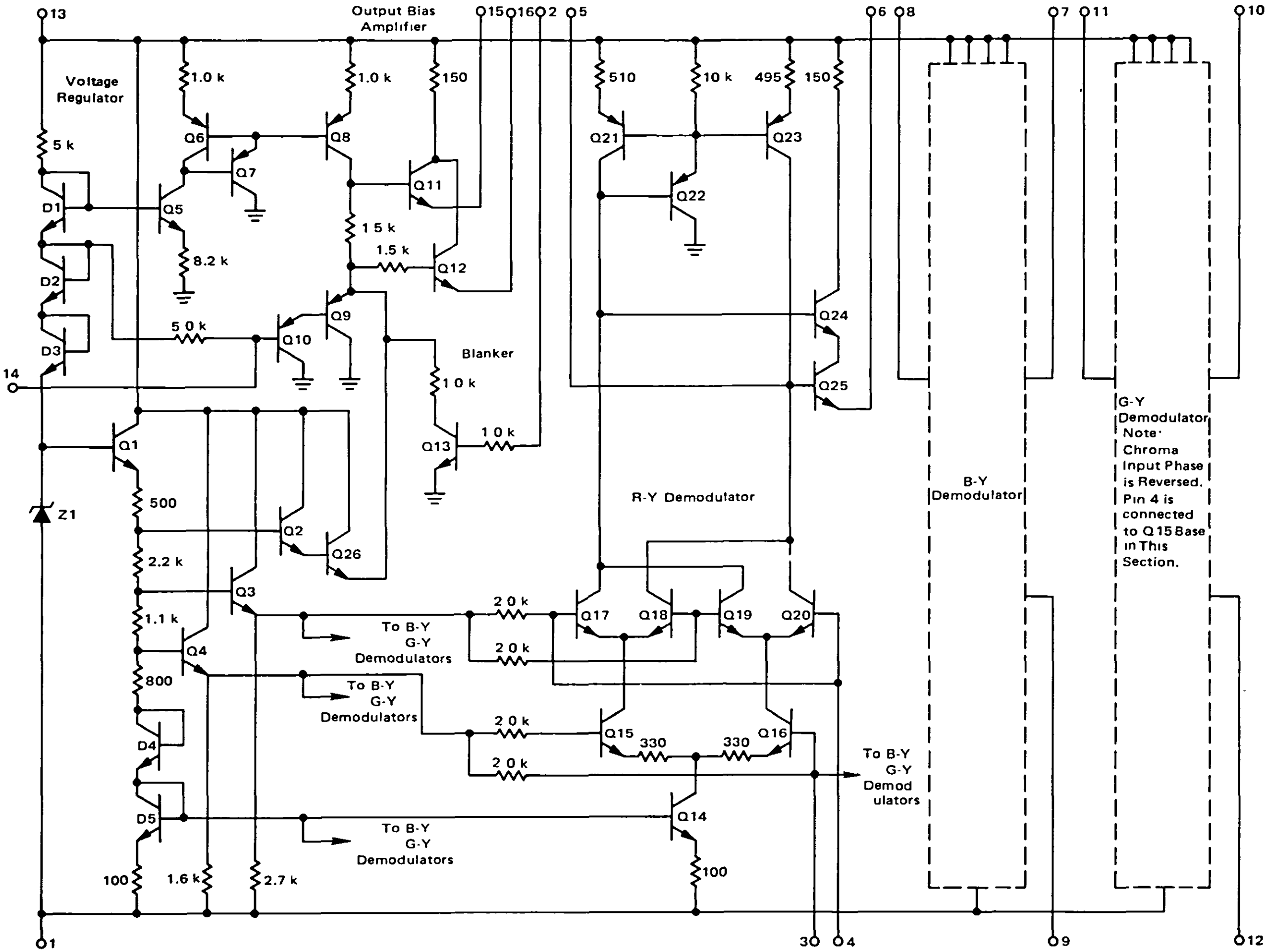


FIGURE 10 – CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC1324P	0°C to +75°C	Plastic DIP

MC1324

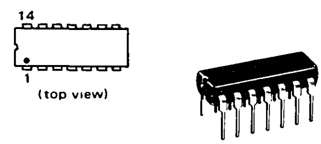
DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B MATRIX AND CHROMA DRIVER STAGES

. . . a monolithic device designed for use in solid-state color television receivers.

- Luminance Input Provided
- Good Chroma Sensitivity – 0.36 Vp-p Input for 5 Vp-p Output
- Low Differential Output DC Offset Voltage – 0.6 V max
- DC Temperature Stability – 3 mV/°C typ
- Negligible Change in Output Voltage Swing and Varying 3.58-MHz Reference Input Signal
- High Ripple Rejection Achieved with MOS Filter Capacitors
- High Blue Output Voltage Swing – 10 V(p-p) typ
- Blanking Input Provided
- Improved MC1326
- Short-Circuit Protected Outputs

DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B OUTPUT MATRIX

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

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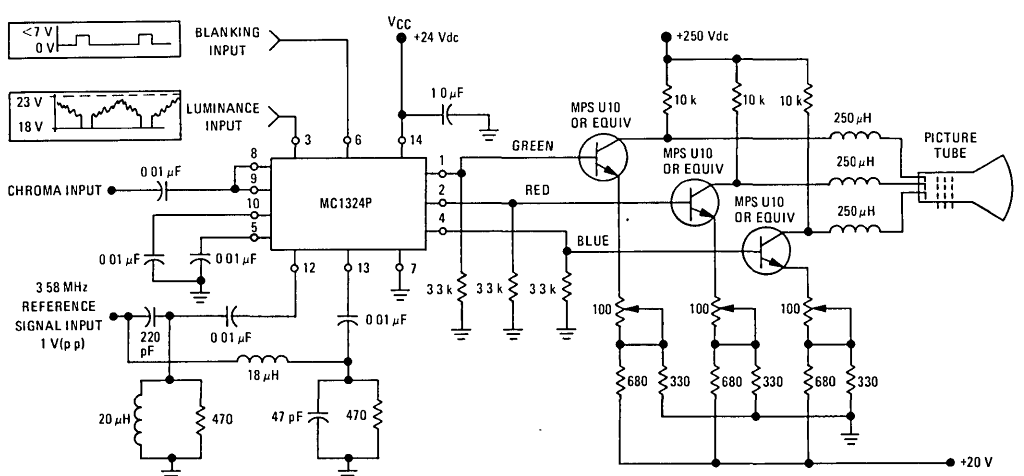
FIGURE 1 – MC1324 TYPICAL APPLICATION



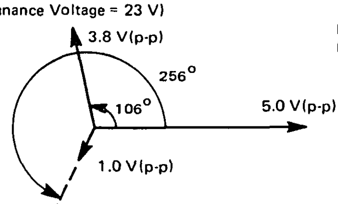
A typical application is given above to indicate the requirements and output functions of this chroma demodulator

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5.0	V(pk)
Reference Signal Input Voltage	5.0	V(pk)
Minimum Load Resistance	2.2	k ohms
Luminance Input Voltage	12	V(p-p)
Blanking Input Voltage	7.0	V(p-p)
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, V_{ref} = 1.0 V(p-p), R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted.)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS (See Figure 2.)					
Quiescent Output Voltage	1,2,4	14.3	15	16.3	Vdc
Quiescent Input Current (R_L = ∞) (R_L = 3.3 k ohms)		 – 16.5	 6.0 19	 – 25.5	mA
Reference Input dc Voltage	5,12,13	–	6.8	–	Vdc
Chroma Input dc Voltage	8,9,10	–	3.6	–	Vdc
Differential Output Voltage	1,2,4	–	0.3	0 6	Vdc
Output Temperature Coefficient (Reference Input Voltage = 1.0 V(p-p), +25° to +65°C)	1,2,4	–	3.0	–	mV/°C
DYNAMIC CHARACTERISTICS (See Figure 3.)					
Detected Output Voltage (See Note 1.) +(B-Y) -(B-Y)	4	 4 0 4 0	 5 0 5.0	 – –	V(pk)
Chroma Input Voltage (B-Y Output = 5.0 V[p-p]) (See Note 2.)	8	–	0.36	0.7	V(p-p)
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz)	1,2,4	 – –	 0 95 0.5	 – –	–
Blanking Input Resistance 1.0 Vdc 0 Vdc	6	 – –	 1.1 75	 – –	kΩ
Detected Output Voltage (Adjust B-Y Output to 5.0 V(p-p), Luminance Voltage = 23 V) G-Y Output R-Y Output	4 1 2	 0.75 3.5	 1.0 3.8	 1.25 4.2	V(p-p)
Relative Output Phase (B-Y Output = 5.0 V(p-p), Luminance Voltage = 23 V) B-Y to R-Y Output B-Y to G-Y Output	 4,2 4,1	 101 248	 106 256	 111 264	Degrees



Characteristic	Pin No.	Min	Typ	Max	Unit
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1,2,4	–	100	500	mV(p-p)
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B-Y Output = 5 0 V[p-p])	1,2,4	–	–	1.0	V(p-p)
Reference Input Resistance	12,13	–	2.0	–	kΩ
Reference Input Capacitance	12,13	–	6.0	–	pF
Chroma Input Resistance	9,10	–	2.0	–	kΩ
Chroma Input Capacitance	9,10	–	2.0	–	pF

NOTES:

1. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 1.2 V(p-p).
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5 V(p-p). The Chroma Input Voltage at this point should be equal to or less than 0.7 V(p-p)

TEST CIRCUITS

(V_{CC} = 24 Vdc, R_L = 3.3 Kilohms, T_A = +25°C unless otherwise noted.)

FIGURE 2 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

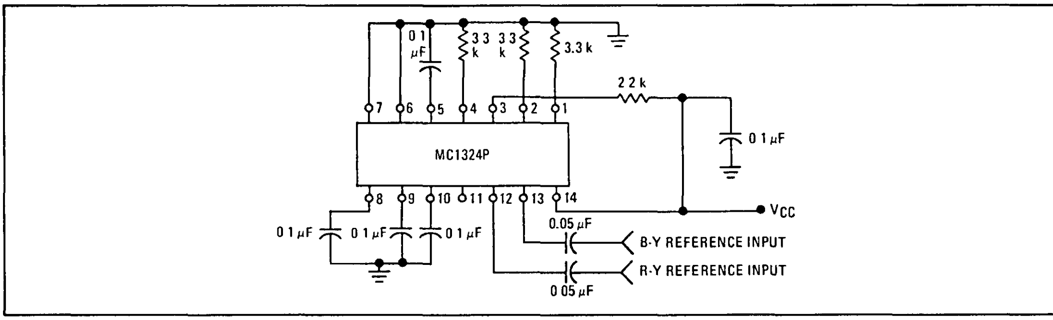
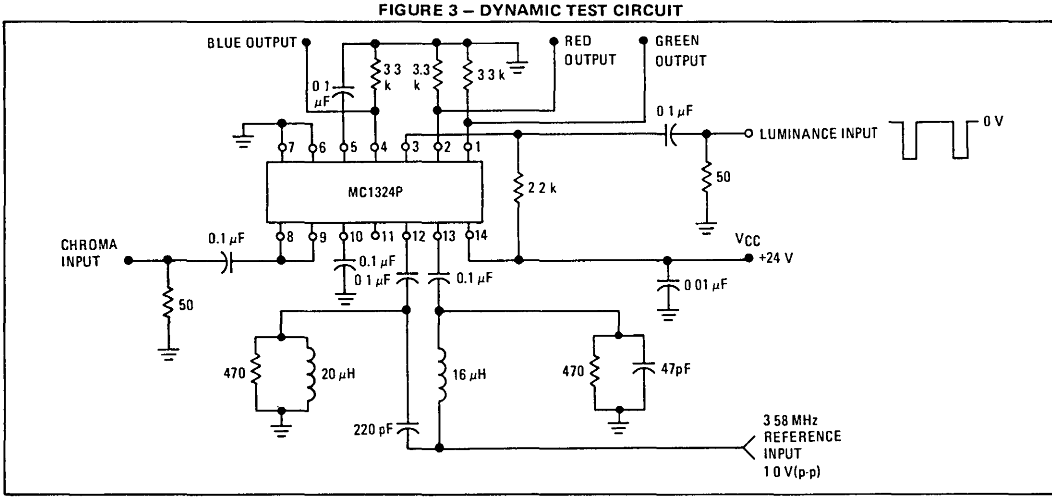


FIGURE 3 – DYNAMIC TEST CIRCUIT



TYPICAL CHARACTERISTICS

FIGURE 4 – DETECTED OUTPUT VOLTAGE
(Test Circuit of Figure 3)

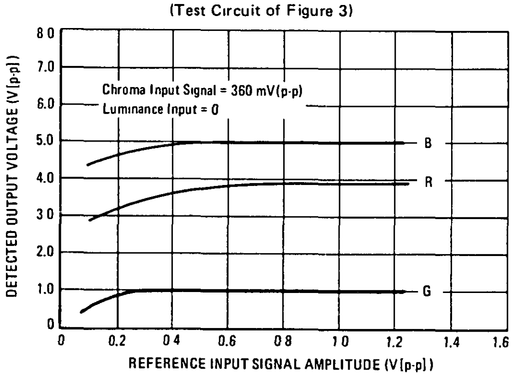


FIGURE 5 – POWER DISSIPATION

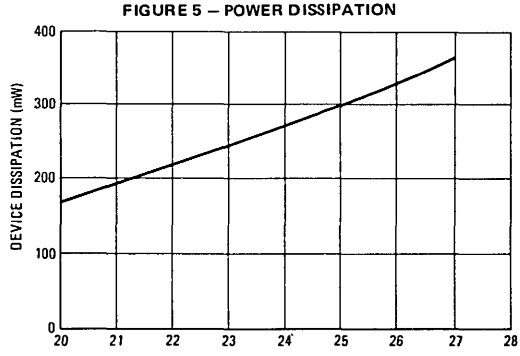


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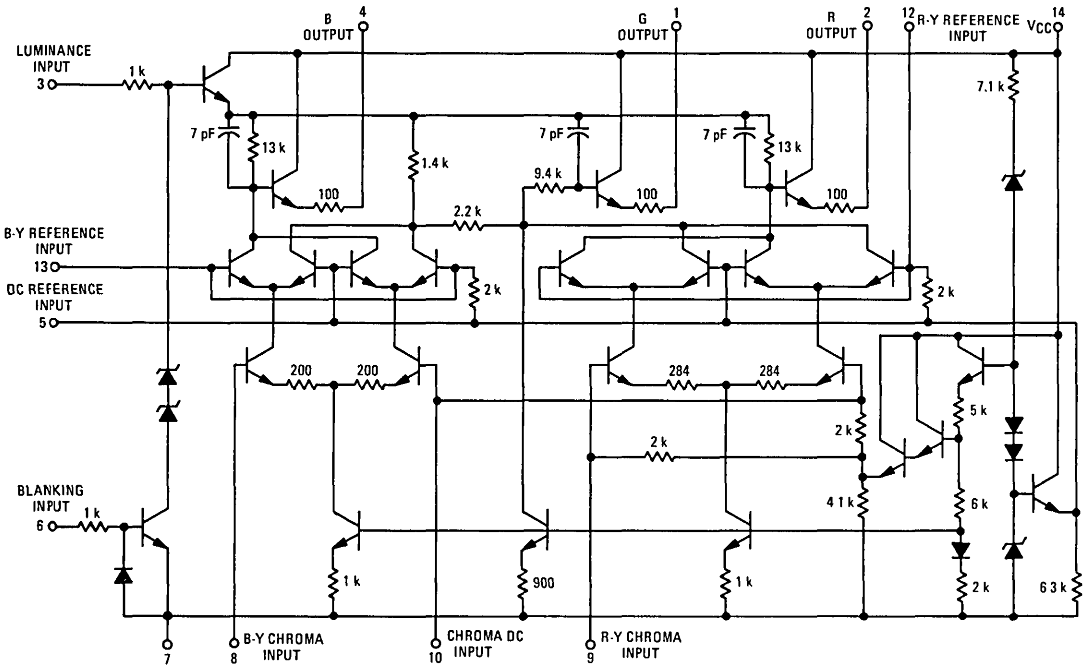
FIGURE 6 — CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC1327P	−20°C to +75°C	Plastic DIP

MC1327

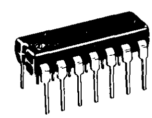
DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH RGB MATRIX, PAL SWITCH, AND CHROMA DRIVER STAGES

. . . a monolithic device designed for use in solid-state color television receivers.

- Good Chroma Sensitivity — 0.28 Vp-p Input Typical for 5.0 Vp-p Output
- Low Differential Output DC Offset Voltage — 0.6 V Maximum
- Differential DC Temperature Stability — 0.7 mV/°C
- High Blue Output Voltage Swing — 10 Vp-p Typical
- Blanking Input Provided
- Luminance Bandwidth Greater than 5.0 MHz

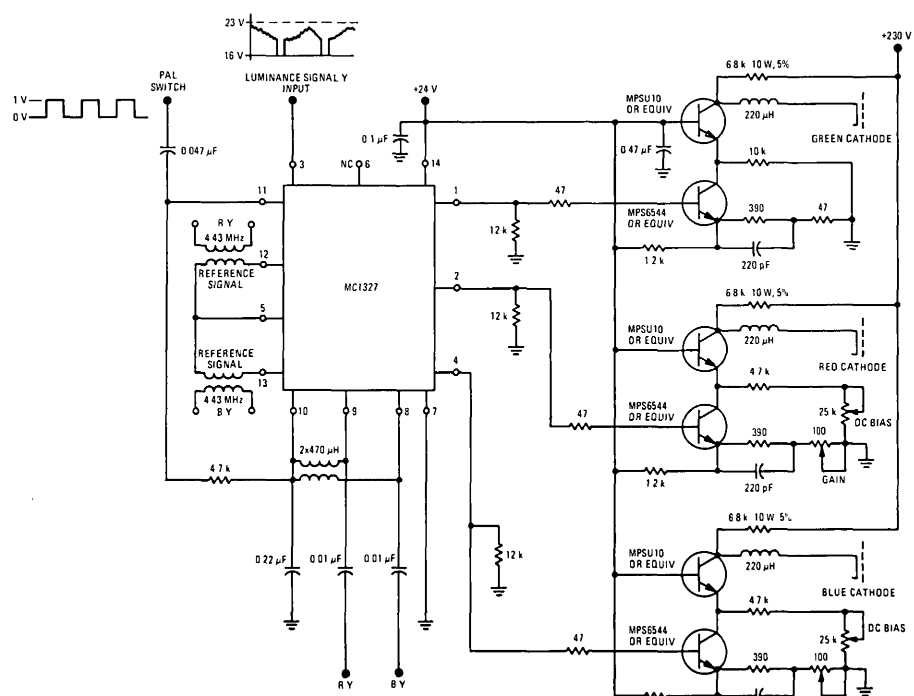
DUAL DOUBLY BALANCED CHROMA DEMODULATOR with RGB OUTPUT MATRIX AND PAL SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

FIGURE 1 — TYPICAL APPLICATION CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5 0	Vpk
Reference Signal Input Voltage	5 0	Vpk
Minimum Load Resistance	3 0	k ohms
Luminance Input Voltage	12	Vp-p
Blanking Input Voltage	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5 0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3 3 k ohms, T_A = +25°C unless otherwise noted)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Quiescent Output Voltage (See Figure 2)	1,2,4	13.2	14.5	15 8	Vdc
Quiescent Input Current from Supply (Figure 2) (R_L = ∞) (R_L = 3.3 k ohms)		 – 16	 7 5 19	 – 26	mA
Reference Input DC Voltage (Figure 2)	5,12,13	–	6 2	–	Vdc
Chroma Reference Input DC Voltage (Figure 2)	8,9,10	–	3 4	–	Vdc
Differential Output Voltage (See Note 1 and Figure 2)	1,2,4	–	0 3	0 6	Vdc
Differential Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C)	1,2,4	–	0 7	–	mV/°C
Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C)	1,2,4	–	+0 5	±5 0	mV/°C
DYNAMIC CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3 3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)					
Blue Output Voltage Swing (See Note 2 and Figure 3)	4	8 0	10	–	Vp-p
Chroma Input Voltage (B Output = 5 0 Vp-p) (See Note 3 and Figure 3)	8	–	280	550	mVp-p
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5 0 MHz, reference at 100 kHz)	1,2,4	 – –	 0 95 -1.8	 – –	– dB
Differential Luminance Gain, RGB Outputs (@ 5 0 MHz)		–	0 3	–	dB
Blanking Input Resistance (1 0 Vdc) (0 Vdc)	6	 – –	 1 1 75	 – –	kΩ
Detected Output Voltage (Adjust B Output to 5 0 Vp-p, Luminance Voltage = 23 V) (See Note 4) G Output R Output	4 1 2	 1 4 2 5	 1 8 2.9	 2 2 3 3	Vp-p
PAL Switch Operating Voltage Range (7.8 kHz Square Wave)	11	0 3	–	3 0	Vp-p
R-Y Output dc Offset with PAL Switch Operation		–	–	100	mVdc
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1,2,4	–	200	300	mVp-p
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B Output = 5 0 Vp-p)	1,2,4	–	0 6	1.0	Vp-p
Reference Input Resistance (Chroma Input = 0)	12,13	–	2.0	–	kΩ
Reference Input Capacitance (Chroma Input = 0)	12,13	–	6.0	–	pF
Chroma Input Resistance	8,9,10	–	2.0	–	kΩ
Chroma Input Capacitance	8,9,10	–	2.0	–	pF

NOTES:
1. Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage = 1.0 Vp p
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 1.2 Vp-p
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5 0 Vp-p
4. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5 0 Vp-p At this point, the Red and Green voltages will fall within the specified limits.

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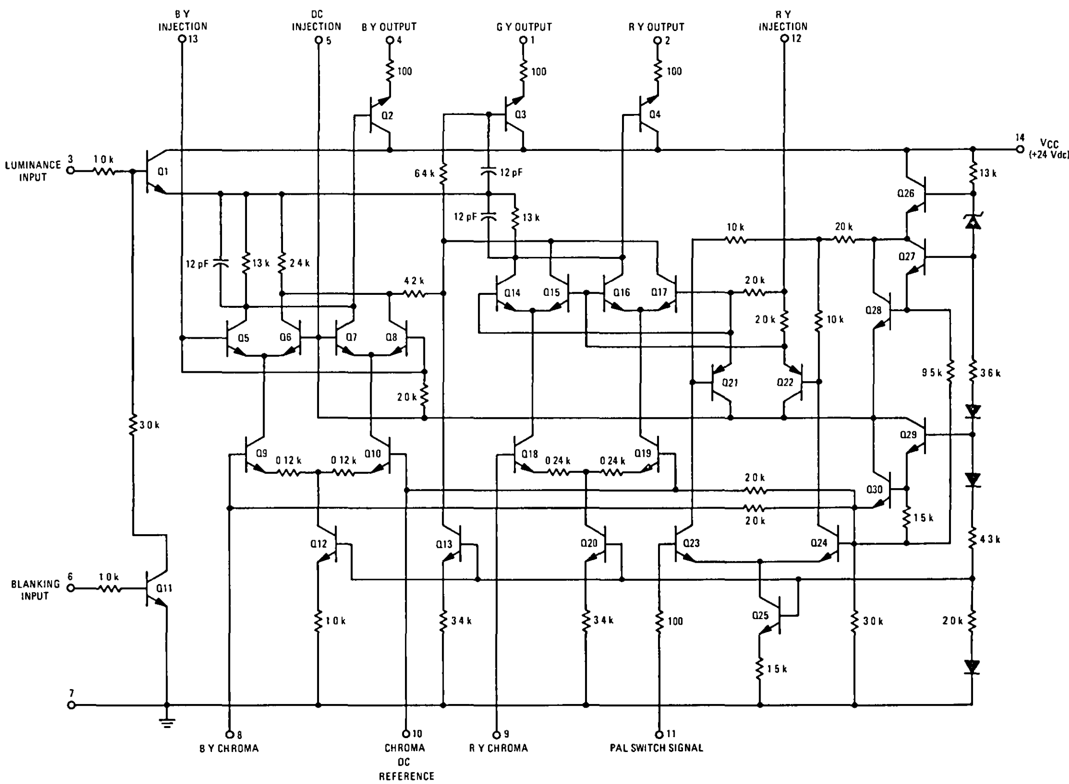
MC1327 CHROMA DEMODULATOR (PAL)



TEST CIRCUITS

(VCC = 24 Vdc, RL = 3.3 kilohms, TA = +25°C unless otherwise noted)

FIGURE 2 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

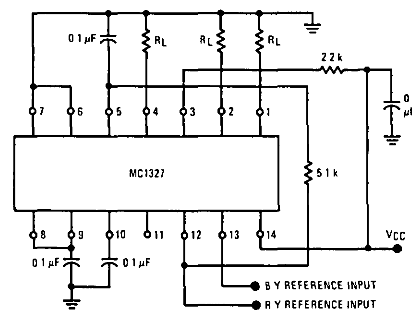
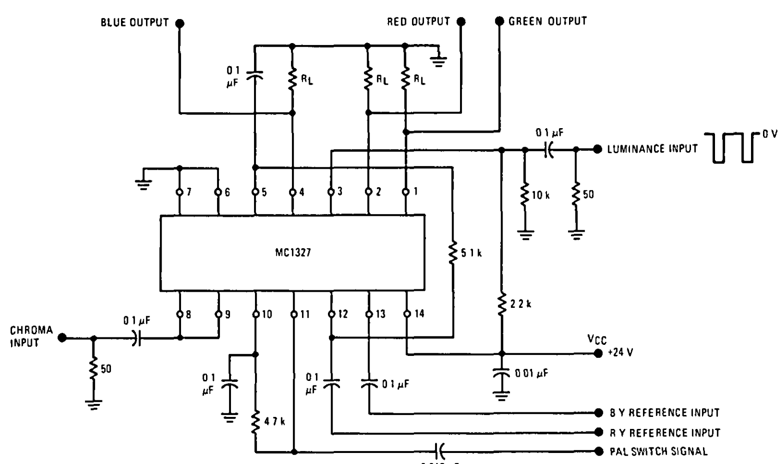


FIGURE 3 – DYNAMIC TEST CIRCUIT



ORDERING INFORMATION

Device	Temperature Range	Package
MC1330A1P	0°C to +75°C	Plastic DIP
MC1330A2P	0°C to +75°C	Plastic DIP

MC1330A1P
MC1330A2P

LOW-LEVEL VIDEO DETECTOR

. . . an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

- Conversion Gain – 33 dB (Typ)
- Excellent Differential Phase and Gain
- High Rejection of IF Carrier Feedthrough
- High Video Output – 8.0 V(p-p)
- Fully Balanced Detector
- Output Temperature Compensated
- Improved Versions of the MC1330P

CIRCUIT DESCRIPTION

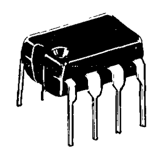
The MC1330A video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wide band, > 8.0 MHz, with normal negative polarity. A separate narrow bandwidth, positive video output is also provided.

LOW-LEVEL VIDEO DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

OUTPUT VOLTAGE SELECTION

The MC1330A1P is identical to the MC1330A2P with the following exception:

	ZERO SIGNAL DC OUTPUT VOLTAGE
MC1330A1P	7.0 to 8.2 Vdc
MC1330A2P	7.8 to 9.0 Vdc

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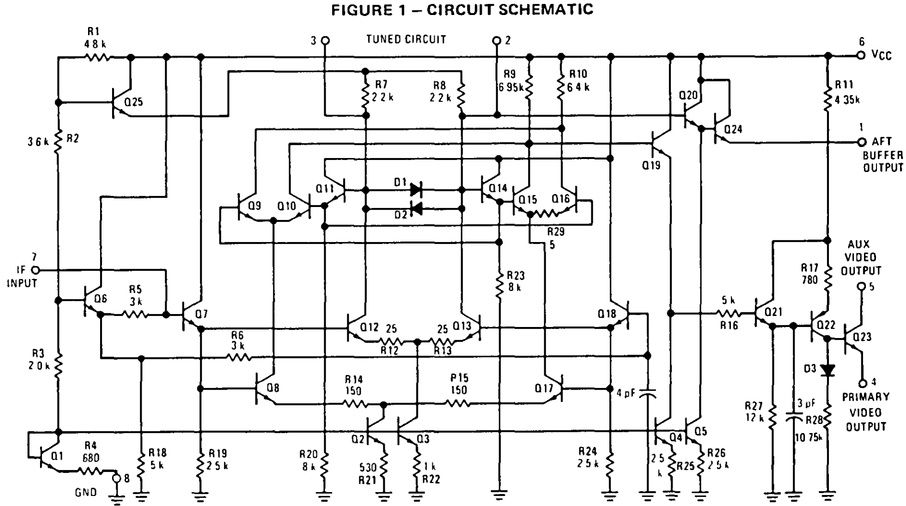
FIGURE 1 – CIRCUIT SCHEMATIC



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MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage	24	Vdc
DC Video Output Current	5.0	mAdc
DC AFT Output Current	2.0	mAdc
Junction Temperature	150	°C
Operating Ambient Temperature Range	0 to 75	°C
Storage Temperature Range	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, fc = 45.75 MHz, T_A = +25°C unless otherwise noted)

Characteristic		Pin	Min	Typ	Max	Unit
Zero Signal dc Output Voltage	MC1330A1P	4	7.0	–	8.2	Vdc
	MC1330A2P	4	7.8	–	9.0	Vdc
Supply Current		5, 6	11	17.5	20	mA
Maximum Signal dc Output Voltage		4	–	0	0.5	Vdc
Conversion Gain for 1.0 Vp-p Output (30% Modulation)		7	25	36	65	mVrms
AFT Buffer Output at Carrier Frequency		1	300	475	650	mVp-p

FIGURE 2 – TEST FIXTURE CIRCUIT

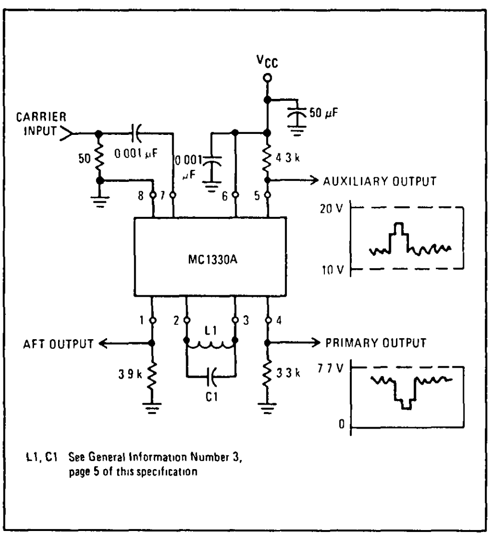


FIGURE 3 – INPUT ADMITTANCE

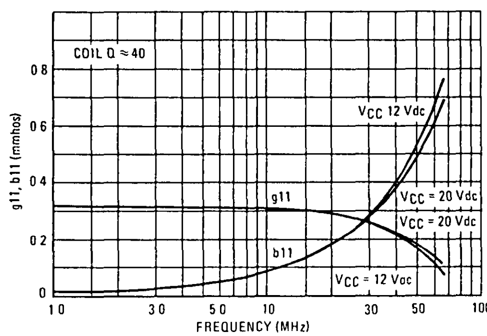
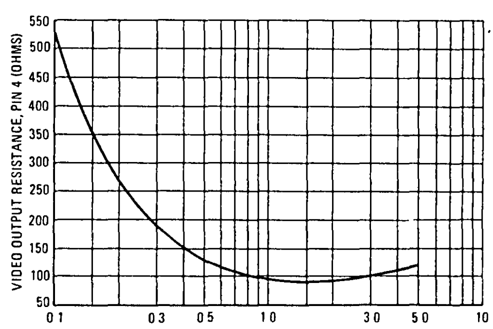


FIGURE 4 – VIDEO DETECTOR OUTPUT RESISTANCE



DESIGN CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, f_c = 45.75 MHz, T_A = +25°C unless otherwise noted)

Characteristic	Pin	Typ	Unit
Input Resistance Input Capacitance	7 7	4.9 1.5	kΩ pF
Internal Resistance (Across Tuned Circuit) Internal Capacitance (Across Tuned Circuit)	2, 3 2, 3	4.4 1.0	kΩ pF
Negative Video Output Bandwidth (Figure 10) Positive Video Output Bandwidth (Figure 10)	4 5	10.8 2.2	MHz MHz
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6 Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6	 4 4	 7.0 4.0	 Degrees %
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3 0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ	 4 4	 8.0 6.0	 Degrees %
920 kHz Beat Output (dB Below 100% Modulated Video, See Figure 11) 45.75 MHz = Reference 42.17 MHz = - 6 dB 41.25 MHz = -20 dB	4	−38	dB
Video Output Resistance @ 1 MHz, 2 mA	4	94	Ω
Input Overload (Carrier Level at Input to Caused Detector Output, Pin 4, To Go Positive 0.1 Vdc From Ground.) V_{CC} = 12 Vdc V_{CC} = 15 Vdc V_{CC} = 20 Vdc V_{CC} = 24 Vdc	7	2.0 2.6 3.6 4.6	Volts
Power Supply Voltage Range	5	10 to 24	Volts

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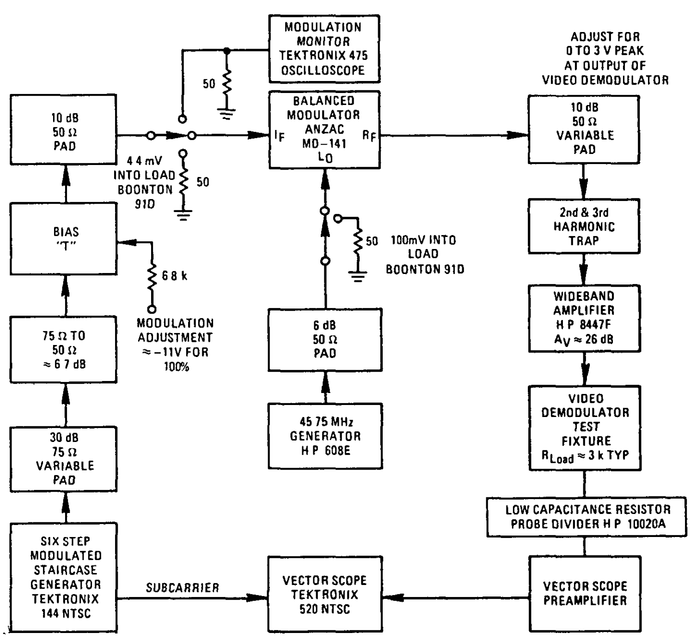
FIGURE 5 – DIFFERENTIAL PHASE AND GAIN TEST SET UP



TYPICAL CHARACTERISTICS

(V_{CC} = +20 Vdc, T_A = +25°C Unless Otherwise Noted)

FIGURE 6 – OUTPUT VOLTAGE TRANSFER FUNCTION

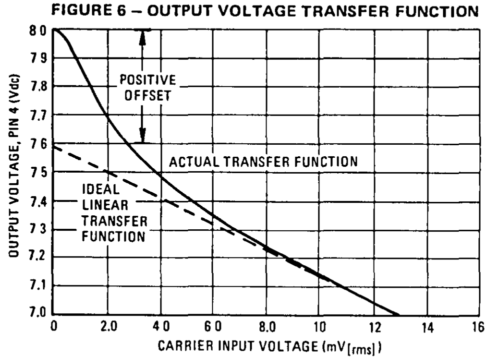


FIGURE 7 – OUTPUT VOLTAGE TRANSFER FUNCTION

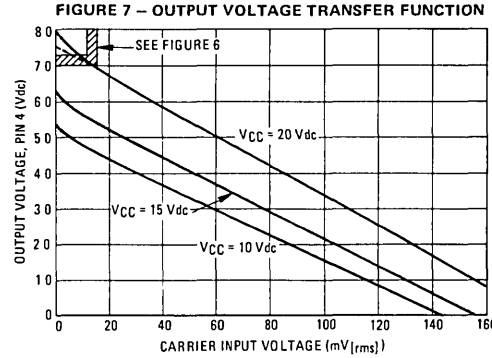


FIGURE 8 – OUTPUT VOLTAGE, SUPPLY CURRENT

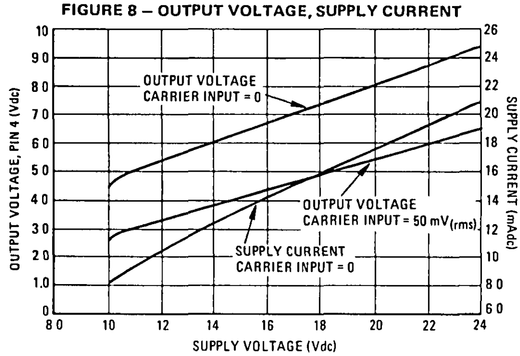


FIGURE 9 – AFT LIMITING

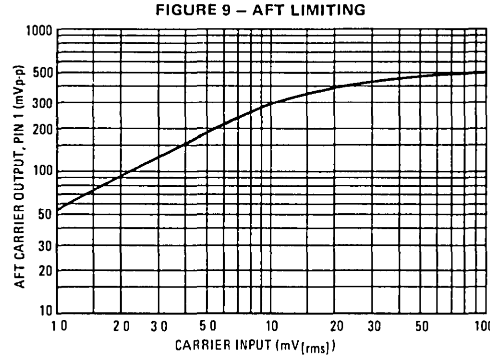


FIGURE 10 – VIDEO OUTPUT RESPONSE

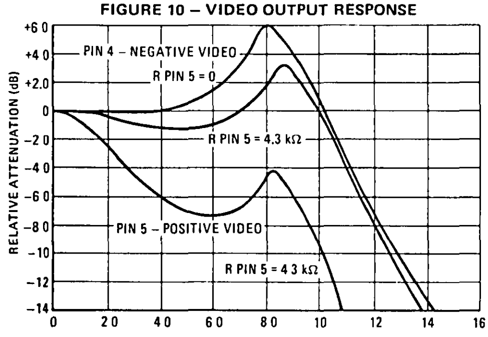
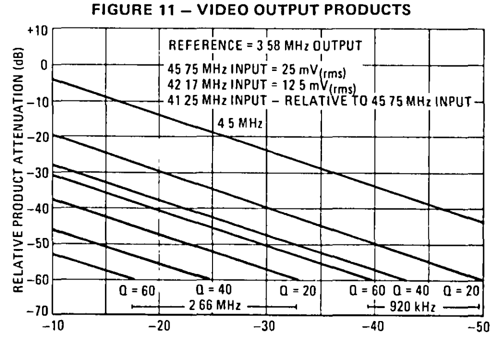


FIGURE 11 – VIDEO OUTPUT PRODUCTS



TV-IF Amplifier Information

A very compact high performance IF amplifier constructed as shown in Figure 14 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 93 dB voltage gain and can accomodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1349P input.

The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3 volt peak-to-peak output can be varied from 0 to 7.0 V with excellent linearity and freedom from spurious output products.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude. See Figures 12 and 13 below. For a more detailed description of the MC1330AP see application note AN-545.

MC1330A General Information

The MC1330A offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode.

Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:

1. The device provides excellent linearity of output versus input, as shown in Figures 6 and 7. These graphs also show that video peak-to-peak amplitude (ac) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)

2. The dc output level does change linearly with supply voltage shown in Figure 8. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.

3. The choice of Q for the tuned circuit of pins 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. See Figure 11. Values of Q from 20 to 50 are recommended. (Note the internal resistance.)

4. A video output with positive-going sync is available at pin 5 if required. This signal has a higher output impedance than pin 4 so it must be handled with greater care. If not used, pin 5 may be connected directly to the supply voltage (pin 6).The video response will be altered somewhat. See Figure 10.

5. An AFT output (pin1) provides 460 mV of IF carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.

6. AGC lockout can occur if the input signal presented in the MC1330A is greater than that shown in the input overload section of the design characteristics shown on Page 3. If these values are exceeded, the turns ratio between the primary and secondary of T_1 should be increased. Another solution to the problem is to use an input clamp diode D_1 shown in Figure 14.

7. The total I.F. noise figure at high gain reductions can be improved by reflecting ≈ 1 k source impedance to the input of the MC1330AP. This will cause some loss in overall IF voltage gain.

FIGURE 12 – BYPASS DISPLAYED BY CONVENTIONAL SWEEP

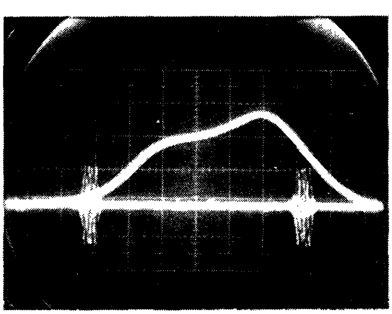


FIGURE 13 – BYPASS DISPLAY WITH THE ADDITION OF CARRIER INJECTION

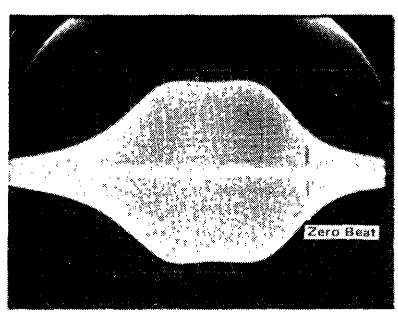


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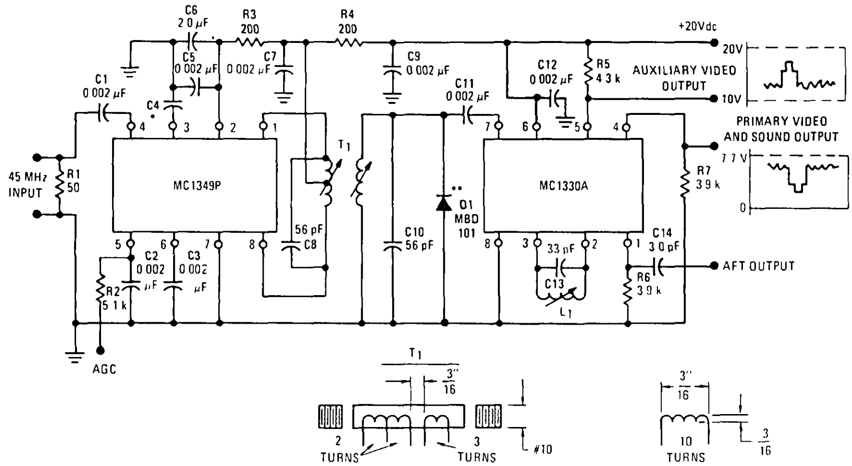
FIGURE 14 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330A LOW-LEVEL VIDEO DETECTOR CIRCUIT



All windings 22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10-32, or equivalent

L_1 wound with 26 AWG tinned nylon acetate wire tuned by distorting winding

*See Note 1 (page 3), and C4, Parts List (page 4) for this specification on the MC1349P Data Sheet
**See Input Overload Section of the Design Characteristics Page 3, and General Information, Page 5, Note 6

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FIGURE 15 – PRINTED CIRCUIT BOARD PARTS LAYOUT

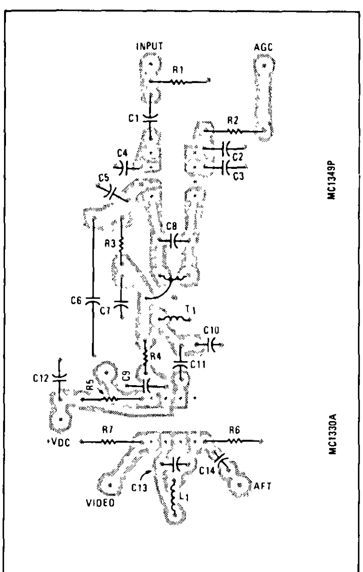
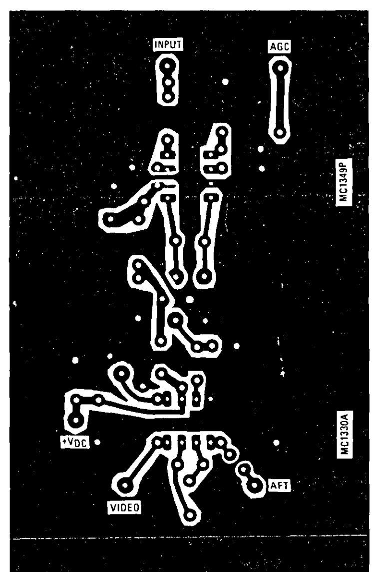


FIGURE 16 – PRINTED CIRCUIT BOARD LAYOUT



ORDERING INFORMATION

Device	Temperature Range	Package
MC1349P	0°C to +70°C	Plastic DIP

MC1349P

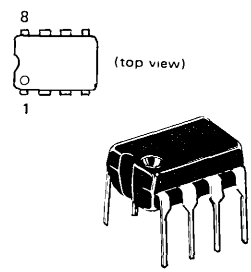
IF AMPLIFIER

. . . *an integrated circuit* featuring wide range AGC for use as an IF amplifier in radio and television applications over the temperature range 0 to +70°C.

- Power Gain – 60 dB typ at 45 MHz (pin 3 open)
  - – 56 dB typ at 58 MHz (pin 3 open)
  - – 61 dB typ at 45 MHz (pin 3 bypassed)
  - – 59 dB typ at 58 MHz (pin 3 bypassed)
- AGC Range – 80 dB typ, dc to 45 MHz
- High Output Impedance
- Low Reverse Transfer Admittance
- 15-Volt Operation, Single-Polarity Power Supply
- Improved Noise Figure versus AGC

IF AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

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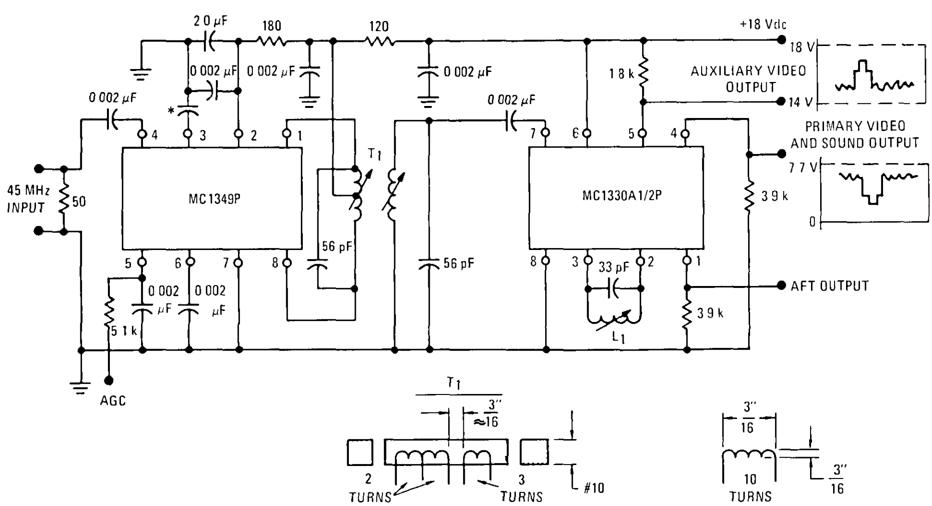
FIGURE 1 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT



All windings #22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10 32, or equivalent

L1 wound with =26 AWG tinned nylon acetate wire tuned by distorting winding

*See Note 1 (page 3), and C4, Parts List (page 4) of this specification

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating	Value	Unit
Power Supply Voltage (V_{CC1})	+18	Vdc
Output Supply Voltage (V_{CC2})	+18	Vdc
AGC Supply Voltage	≦ V_{CC1} (pin 2)	Vdc
Differential Input Voltage	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

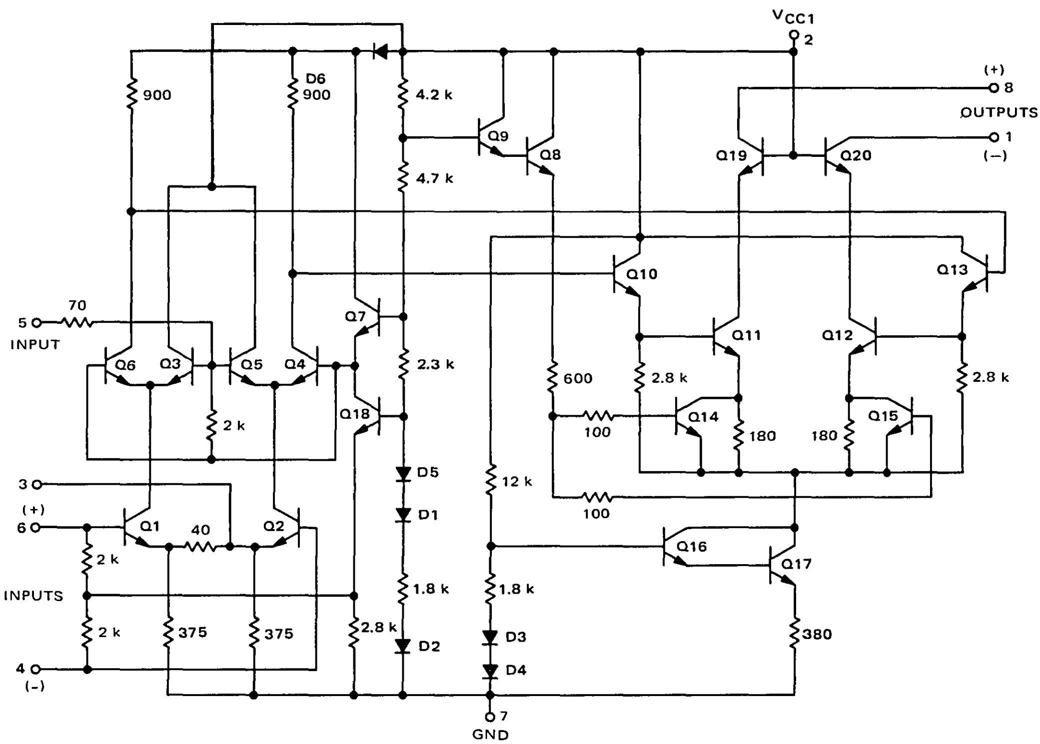
ELECTRICAL CHARACTERISTICS (V_{CC1} = +12 Vdc [pin 2], V_{CC2} = +15 Vdc [pins 1 and 8], T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.5 V) (Figure 3)	70	80	–	dB
Power Gain (Pin 5 grounded via 5.1 kΩ resistor, input pin 4) f = 45 MHz, BW (3 dB) = 4.5 MHz, Tuned Input, pin 3 open Untuned Input, pin 3 bypassed f = 58 MHz, BQ (3 dB) = 4.5 MHz, Tuned Input, pin 3 open Untuned Input, pin 3 bypassed	 52 – – –	 60 61 56 59	 – – – –	dB
Maximum Differential Output Voltage Swing	–	6.0	–	Vp-p
Output Stage Current (pins 1 and 8)	–	9.0	–	mA
Amplifier Current (pin 2)	–	15	20	mAdc
Power Dissipation	–	315	400	mW
Noise Figure f = 45 MHz, Tuned Input, pin 3 open, Gain Reduction = 15 dB	–	8.5	–	dB

DESIGN PARAMETERS (V_{CC1} = +12 Vdc, [pin 2], V_{CC2} = +15 Vdc, [pins 1 and 8], T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Frequency		Unit
		45 MHz	58 MHz	
Single-Ended Input Admittance, input pin 4, AGC min Pin 3 open Pin 3 open Pin 3 bypassed Pin 3 bypassed	 g11 b11 g11 b11	 0.74 1.9 4.1 6.5	 0.95 2.4 5.4 6.9	mmhos
Differential Output Admittance, AGC max	 g22 b22	 5.5 270	 8.3 360	μmhos
Reverse Transfer Admittance (magnitude)		1.5	2.0	μmhos
Forward Transfer Admittance Magnitude, pin 3 open Angle (0 dB AGC), pin 3 open Magnitude, pin 3 bypassed Angle (0 dB AGC), pin 3 bypassed		 520 100 1020 120	 400 130 800 400	 mmhos degrees mmhos degrees
Single-Ended Input Capacitance, AGC min Pin 3 open Pin 3 bypassed		 6.8 2.3	 6.7 20	pF
Differential Output Capacitance (AGC max)		1.0	1.0	pF

FIGURE 2 – CIRCUIT SCHEMATIC



GENERAL INFORMATION

The MC1349P is an improved version of the MC1350P. Featuring higher gain, a lower noise figure, and greater AGC range; in addition, an emitter of the input amplifier is available for bypassing. This provides a low input impedance with good gain, useful for untuned input configurations.

Both input and output IF amplifier sections are gain-controlled in the MC1349P, with the input amplifier also serving as an AGC amplifier for the output section. During the initial part of AGC gain reduction, the gain of the input amplifier decreases only a few dB while the output section decreases 15 dB; further AGC acts upon the input section. Although the gain reduction curve was taken with 5.1 kilohms at pin 5, higher series resistance can be used to reduce the voltage and temperature sensitivity of the AGC. Pin 5 currents are shown on the AGC curve, see Figure 10.

In use, it is important to bypass pin 2, both for IF frequencies and for low frequencies, (as shown in the test circuits). This is due to the dual function of the input amplifier. If replacing MC-1350P take precaution not to ground pin 3, (not used in the MC1350P). Due to the significantly higher gain of the MC1349P, extra care in layout should be exercised.

NOTE 1: The references to bypasses at pin 3 do not give specific values (C4, see Figures 1 and 4). In all cases, measurements were taken with a bypass at a standard value as near as possible to series resonance. The values are dependent on test frequency and circuit layout. Fully bypassing pin 3 reduces the input signal handling capability before distortion from over 100 mV(RMS) to approximately 25 mV(RMS). C4 = 0.002 μF at f = 45 MHz is a typical value for printed circuit applications.

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TEST CIRCUITS

FIGURE 3 – TUNED INPUT
(PIN 3 OPEN)

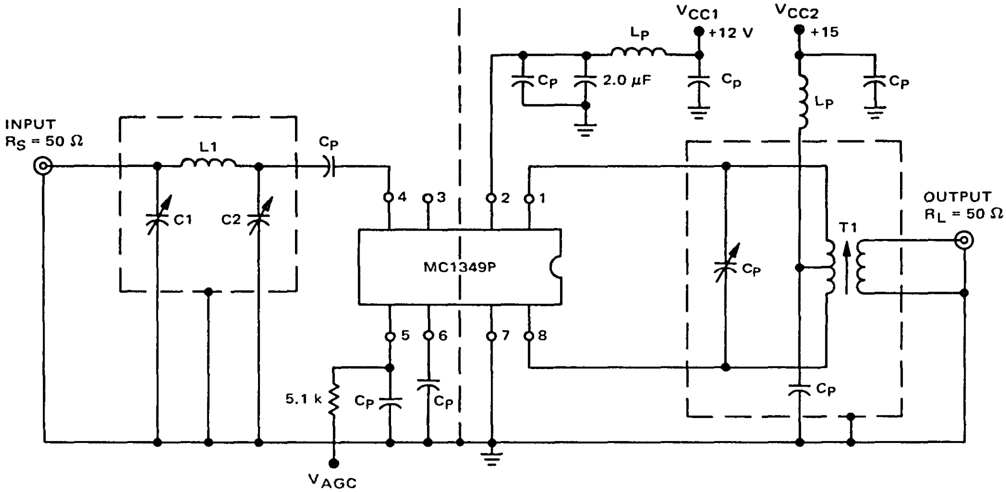
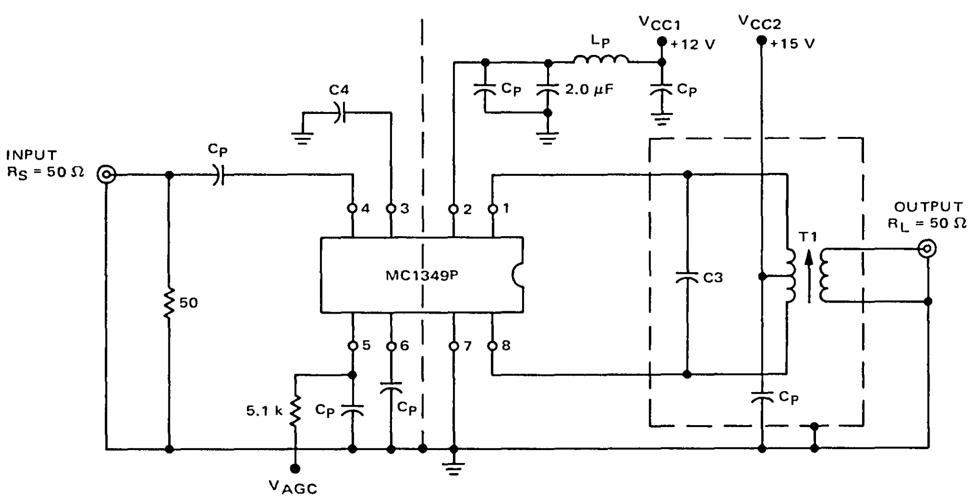


FIGURE 4 – UNTUNED INPUT
(PIN 3 BYPASSED TO GROUND)



PARTS LIST

COMPONENT	45 MHz	58 MHz
C1	8-60 pF	50-100 pF
C2	3-35 pF	3-35 pF
C3	1-7.0 pF	1-7.0 pF
C4	82-470 pF	82-470 pF
C_P	0.0015 μF	0.001 μF
L1	0.84 μH	0.33 μH
L_P	10 μH	10 μH

T1 Primary 14 turns center-tapped
Secondary 2½ turns (45 MHz tuned input pin #3 open) 1½ turns (all other fixtures) wound over primary
Wire. #26 AWG tinned nylon acetate wound on 1/4" diameter coil form
Core Arnold Type TH, 1/2" long or equivalent

TYPICAL CHARACTERISTICS

FIGURE 5 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 OPEN)

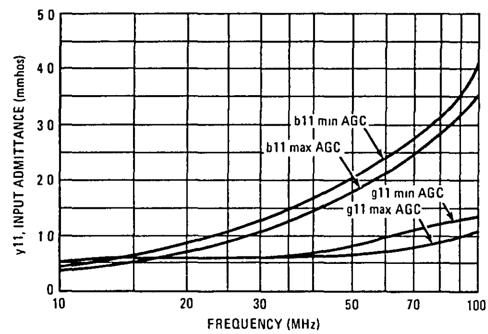


FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 BYPASSED TO GROUND)

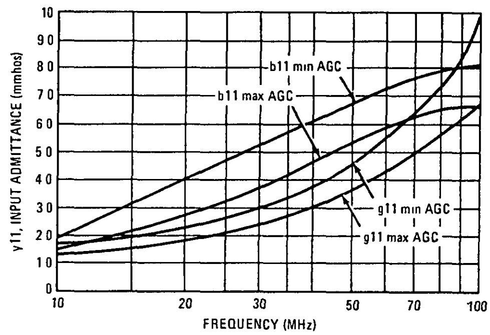


FIGURE 7 – SINGLE-ENDED FORWARD TRANSFER ADMITTANCE

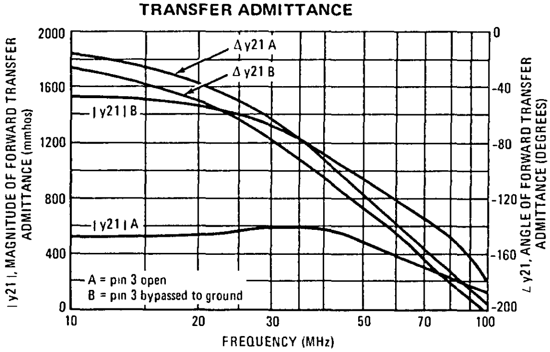


FIGURE 8 – DIFFERENTIAL OUTPUT ADMITTANCE (MAXIMUM AGC)

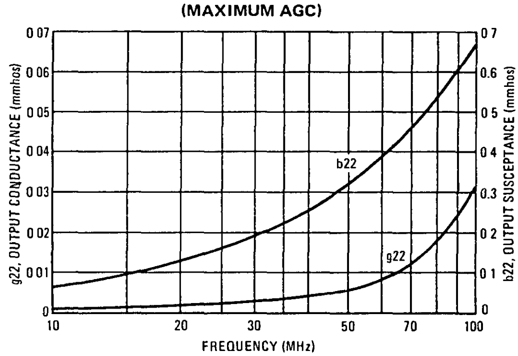


FIGURE 9 – NOISE FIGURE

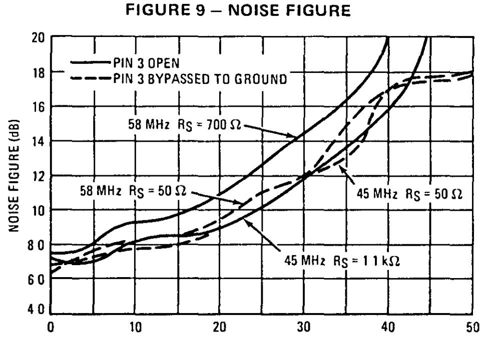
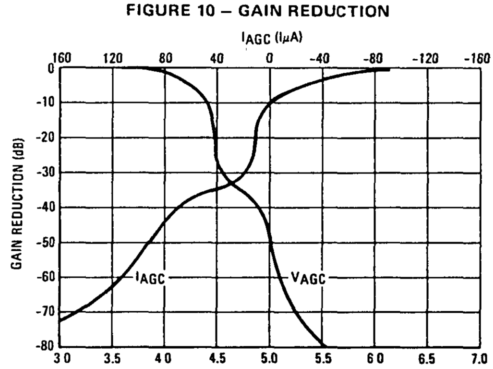


FIGURE 10 – GAIN REDUCTION



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ORDERING INFORMATION

Device	Temperature Range	Package
MC1350P	0°C to +75°C	Plastic DIP

MC1350

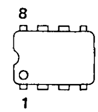
MONOLITHIC IF AMPLIFIER

. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over the temperature range 0 to +75°C. The MC1352 is similar in design but has a keyed-AGC amplifier as an integral part of the same chip.

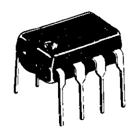
- Power Gain – 50 dB typ at 45 MHz,
  – 48 dB typ at 58 MHz
- AGC Range – 60 dB min, dc to 45 MHz
- Nearly Constant Input and Output Admittance Over the Entire AGC Range
- y_{21} Constant (-3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance — << 1.0 μmho typ
- 12-Volt Operation, Single-Polarity Power Supply

IF AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



(top view)



PLASTIC PACKAGE
CASE 626

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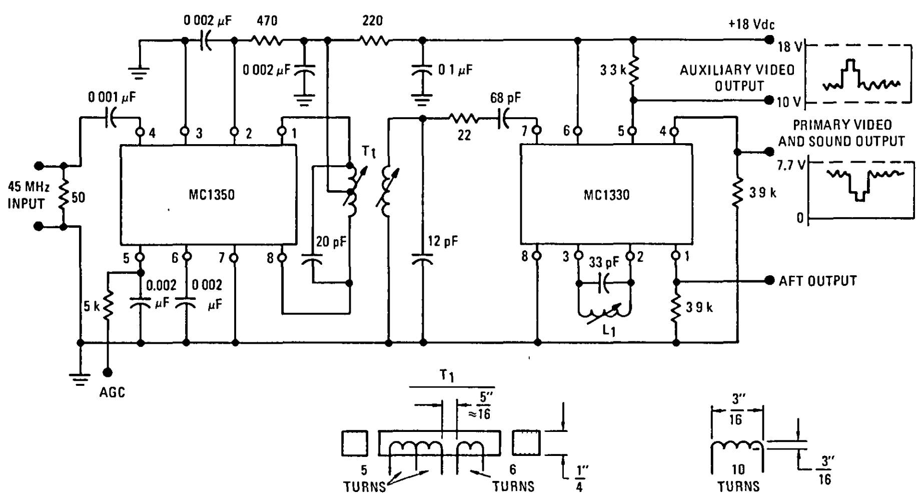
FIGURE 1 – TYPICAL MC1350 VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT



All windings #30 AWG tinned nylon acetate wire tuned with Arnold Type TH slugs

L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc; T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)		60	68	–	dB
Power Gain (Pin 5 grounded via a 5.1 kΩ resistor) f = 58 MHz, BW = 4.5 MHz } See Figure 5 f = 45 MHz, BW = 4.5 MHz } f = 10.7 MHz, BW = 350 kHz } See Figure 6 f = 455 kHz, BW = 20 kHz }	A_p	 – 46 – –	 48 50 58 62	 – – – –	dB
Maximum Differential Voltage Swing 0 dB AGC -30 dB AGC	V_o	 – –	 20 8.0	 – –	V_{p-p}
Output Stage Current (Pins 1 and 8)	$I_1 + I_8$	–	5.6	–	mA
Total Supply Current (Pins 1, 2 and 8)	I_S	–	14	17	mAdc
Power Dissipation	P_D	–	168	204	mW

DESIGN PARAMETERS, Typical Values (V+ = +12 Vdc, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Frequency				Unit
		455 kHz	10.7 MHz	45 MHz	58 MHz	
Single-Ended Input Admittance	g_{11} b_{11}	0.31 0.022	0.36 0.50	0.39 2.30	0.5 2.75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	– –	– –	60 0	– –	μmhos
Differential Output Admittance	g_{22} b_{22}	4.0 3.0	4.4 110	30 390	60 510	μmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	– –	– –	4.0 90	– –	μmhos
Reverse Transfer Admittance (Magnitude)	$\|y_{12}\|$	<<1.0	<<1.0	<<1.0	<<1.0	μmho
Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (-30 dB AGC)	 $\|y_{21}\|$ $\angle y_{21}$ $\angle y_{21}$	 160 -5.0 -3.0	 160 -20 -18	 200 -80 -69	 180 -105 -90	 mmhos degrees degrees
Single-Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_o	1.2	1.2	1.3	1.6	pF

FIGURE 2 – TYPICAL GAIN REDUCTION
(Figures 5 and 6)

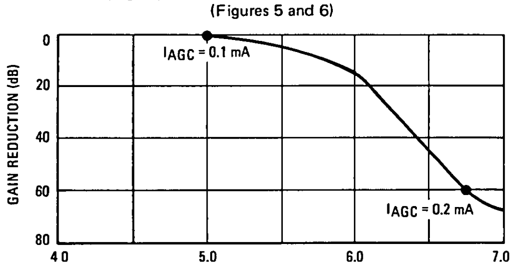
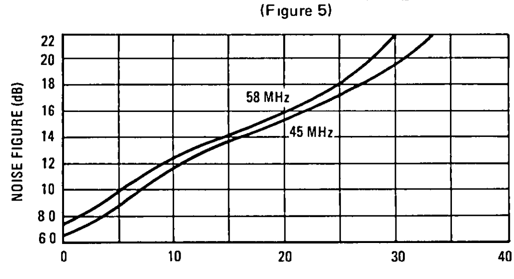


FIGURE 3 – NOISE FIGURE
(Figure 5)



GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

FIGURE 4 – CIRCUIT SCHEMATIC

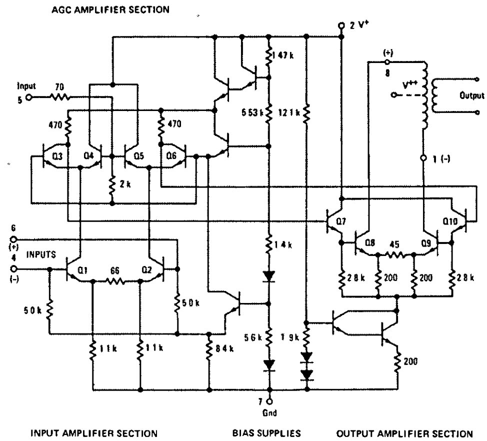
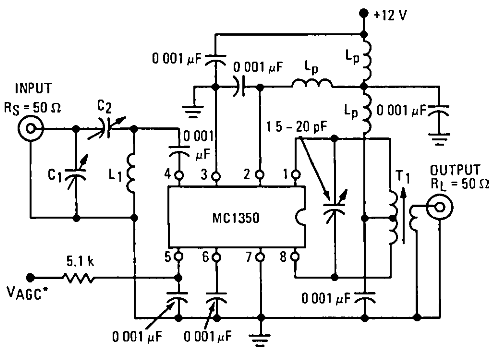


FIGURE 5 – POWER GAIN, AGC and NOISE FIGURE TEST CIRCUIT (45 MHz and 58 MHz)

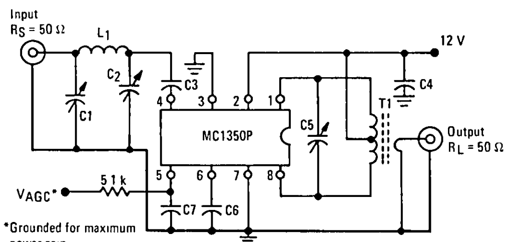


*Connect to ground for maximum power gain test
All power-supply chokes (L_p), are self-resonate at input frequency. $L_p \geq 20$ kΩ
See Figure 10 for frequency response curve

L_1 @ 45 MHz = 7 1/4 Turns on a 1/4" coil form.
@ 58 MHz = 6 Turns on a 1/4" coil form
T_1 Primary Winding = 18 Turns on a 1/4" coil form, center-tapped
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Arnold TH Material 1/2" Long

	45 MHz		58 MHz	
L_1	0.4 µH	Q ≥ 100	0.3 µH	Q ≥ 100
T_1	1.3 - 3.4 µH	Q ≥ 100 @ 2 µH	1.2 - 3.8 µH	Q ≥ 100 @ 2 µH
C_1	50 - 160 pF		8 - 60 pF	
C_2	8 - 60 pF		3 - 35 pF	

FIGURE 6 – POWER GAIN and AGC TEST CIRCUIT (455 kHz and 10.7 MHz)



*Grounded for maximum power gain

Note 1. Primary: 120 µH (center-tapped)
Q_u = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13

Note 2. Primary: 6.0 µH
Primary winding = 24 turns #36 AWG (close-wound on 1/4" dia. form)
Core = Arnold Type TH or equiv.
Secondary winding = 1-1/2 turns #36 AWG, 1/4" dia. (wound over center-tap)

Component	Frequency	
	455 kHz	10.7 MHz
C1	–	80–450 pF
C2	–	5.0–80 pF
C3	0.05 µF	0.001 µF
C4	0.05 µF	0.05 µF
C5	0.001 µF	36 pF
C6	0.05 µF	0.05 µF
C7	0.05 µF	0.05 µF
L1	–	4.6 µH
T1	Note 1	Note 2

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TYPICAL CHARACTERISTICS
(V^+ = 12 V, T_A = +25°C)

FIGURE 7 – SINGLE-ENDED INPUT ADMITTANCE

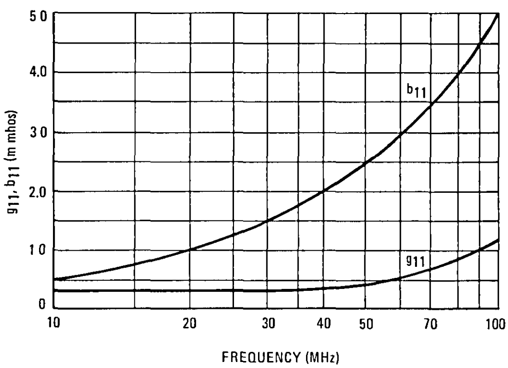


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

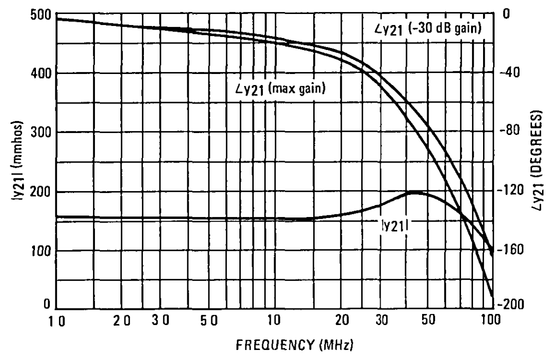


FIGURE 9 – DIFFERENTIAL OUTPUT ADMITTANCE

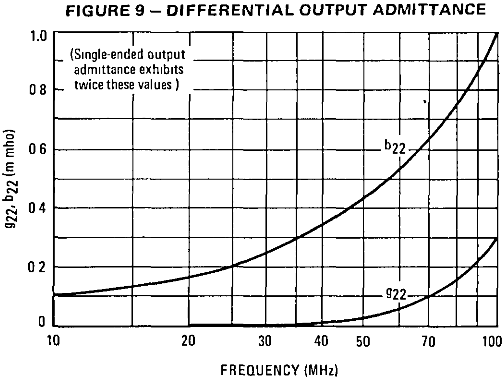


FIGURE 10 – TEST CIRCUIT RESPONSE CURVE
(45 and 58 MHz)

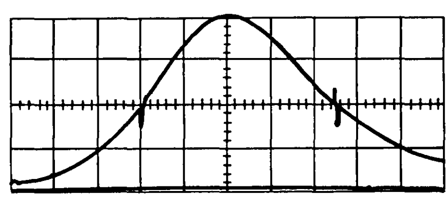
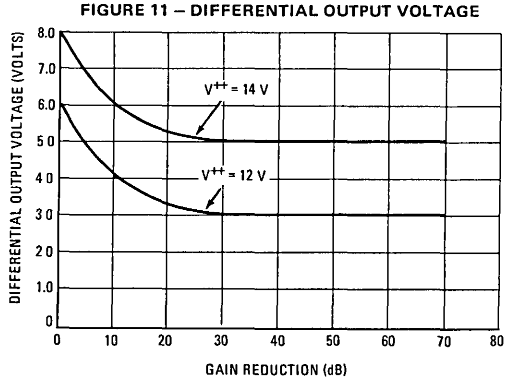


FIGURE 11 – DIFFERENTIAL OUTPUT VOLTAGE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control", by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1351P	0°C to +75°C	Plastic DIP

MC1351

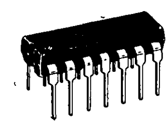
WIDE-BAND FM-AMPLIFIER; LIMITER, DETECTOR, AND AUDIO AMPLIFIER

. . . designed for IF limiting, detection, audio preamplifier and driver for the sound portion of a TV receiver.

- Excellent Limiting with 80 μV(rms) Input Signal typ
- Large Output-Voltage Swing – to 3.5 V(rms) typ
- High IF Voltage Gain – 65 dB typ
- Zener Power-Supply Regulation Built-In
- Short-Circuit Protection
- A Coincidence Discriminator that Requires Only One RLC Phase Shift Network
- Preamplifier to Drive a Single External-Transistor Class-A Audio-Output Stage

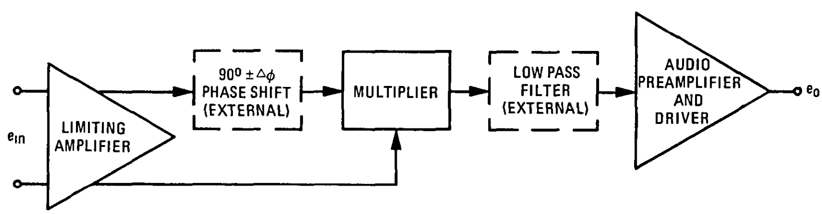
TV SOUND CIRCUIT

MONOLITHIC SILICON INTEGRATED CIRCUIT

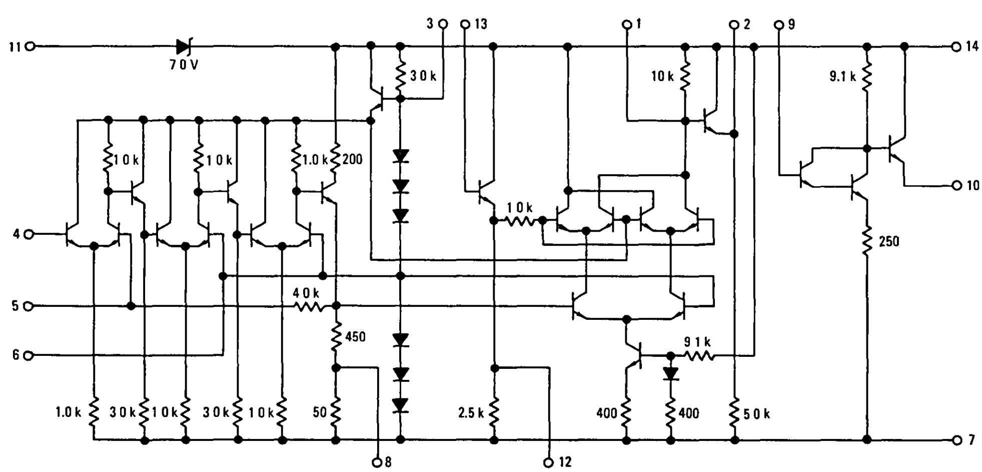


P SUFFIX
PLASTIC PACKAGE
CASE 646

BLOCK DIAGRAM



CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25° unless otherwise noted)

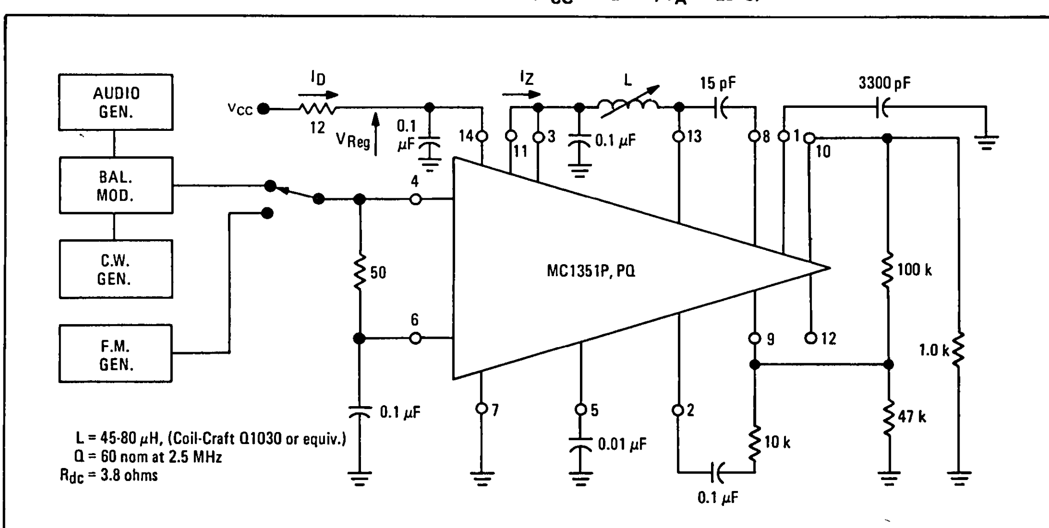
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+16	Vdc
Input Voltage	V_{in}	0.7	V(rms)
Power Dissipation (Package Limitation) Plastic Packages Derate above +25°C	 P_D $1/\theta_{JA}$	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = +25°C, f = 4.5 MHz, Deviation = ±25 kHz unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Input Voltage (-3.0 dB Limiting)	–	80	160	µV(rms)
AM Rejection (V_{in} = 20 mV(rms), AM = 30%) (See Note 1) AMR = 20 log $\frac{V_{OFM}}{V_{OAM}}$ { f = 4.5 MHz, Deviation = ±25 kHz, Q_L = 24 f = 5.5 MHz, Deviation = ±50 kHz, Q_L = 30	 – –	 45 45	 – –	dB
Total Harmonic Distortion (Q_L = 24) (See Note 1) (7.5 kHz Deviation)	–	1.0	–	%
Maximum Undistorted Audio Output Voltage (Pin 10) (See Note 1) (Audio Gain Adjusted Externally) (Q = 24)	–	3.5	–	V(rms)
Recovered Audio (Pin 2) (See Note 1) (f = 4.5 MHz, Deviation = ±25 kHz, Q_L = 24) (f = 5.5 MHz, Deviation = ±50 kHz, Q_L = 30)	 0.35 –	 0.50 0.80	 – –	V(rms)
Audio Preamplifier Open Loop Gain	–	25	–	dB
IF Voltage Gain	–	65	–	dB
Parallel Input Resistance	–	9 0	–	kΩ
Parallel Input Capacitance	–	6.0	–	pF
Nominal Zener Voltage (I_Z = 5.0 mAdc)	–	11.6	–	Vdc
Power Supply Current (I_Z = 5.0 mAdc)	–	31	–	mAdc
Power Dissipation (I_Z = 5.0 mAdc)	–	300	375	mW

Note 1. Q_L is loaded circuit Q.

FIGURE 1 – TEST CIRCUIT (V_{CC} = +12 Vdc, T_A = +25°C)



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TYPICAL CHARACTERISTICS

FIGURE 2 – DETECTED AUDIO OUTPUT versus INPUT LEVEL @ f = 4.5 MHz, ±25 kHz DEVIATION

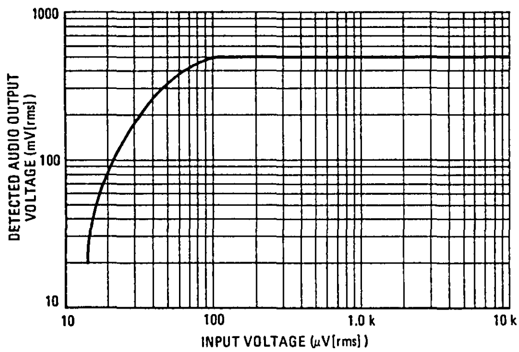

FIGURE 3 – DETECTED AUDIO OUTPUT versus INPUT LEVEL @ f = 5.5 MHz, ±50 kHz DEVIATION

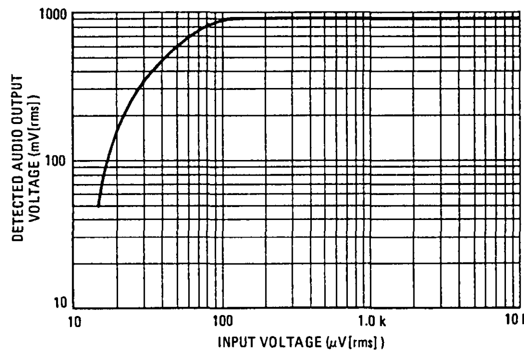

FIGURE 4 – DETECTOR "S" CURVE @ f = 4.5 MHz, BW = 200 kHz, Q = 24

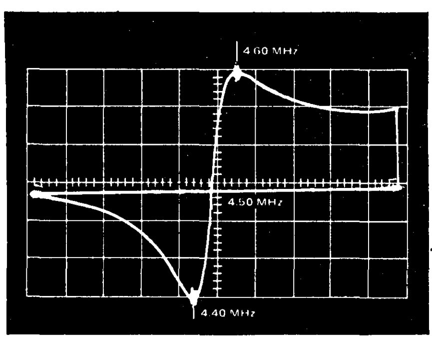

FIGURE 5 – DETECTOR "S" CURVE @ f = 5.5 MHz, BW = 220 kHz, Q = 30

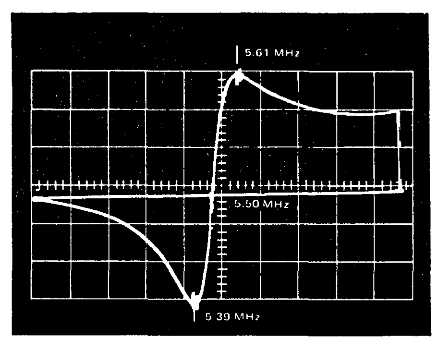

FIGURE 6 – IF VOLTAGE GAIN versus FREQUENCY

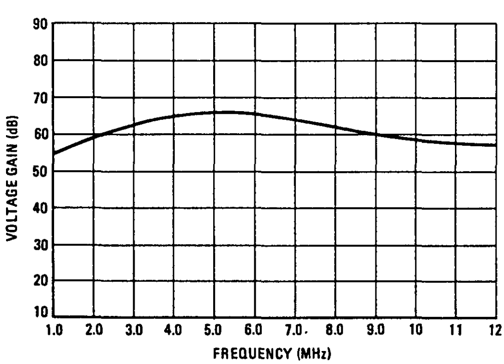

FIGURE 7 – AM REJECTION

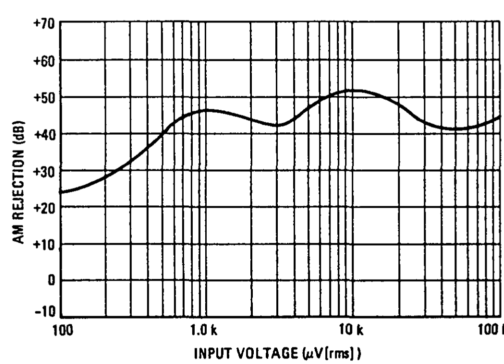

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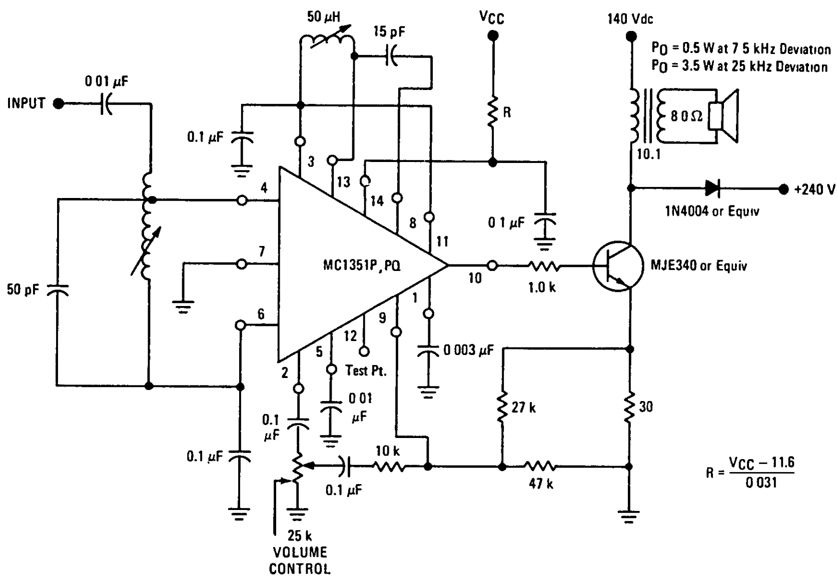
FIGURE 8 — 4.5 MHz TYPICAL APPLICATION



ORDERING INFORMATION

Device	Temperature Range	Package
MC1352P	0°C to +70°C	Plastic DIP

MC1352

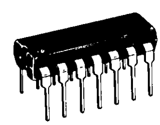
TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

. . . a monolithic IF amplifier with a complete gated wide-range AGC system for use as the 1st and 2nd IF stages and AGC keyer and amplifier in color or monochrome TV receivers.

- Power Gain at 45 MHz, 52 dB typ
- Extremely Low Reverse-Transfer Admittance – << 1.0 μmho typ
- Nearly Constant Input and Output Admittance Over AGC Range
- Single-Polarity Power-Supply Operation
- High-Gain Gated AGC System for Either Positive or Negative-Going Video Signals
- Control Signal Available for Delayed AGC of Tuner

TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



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CASE 646

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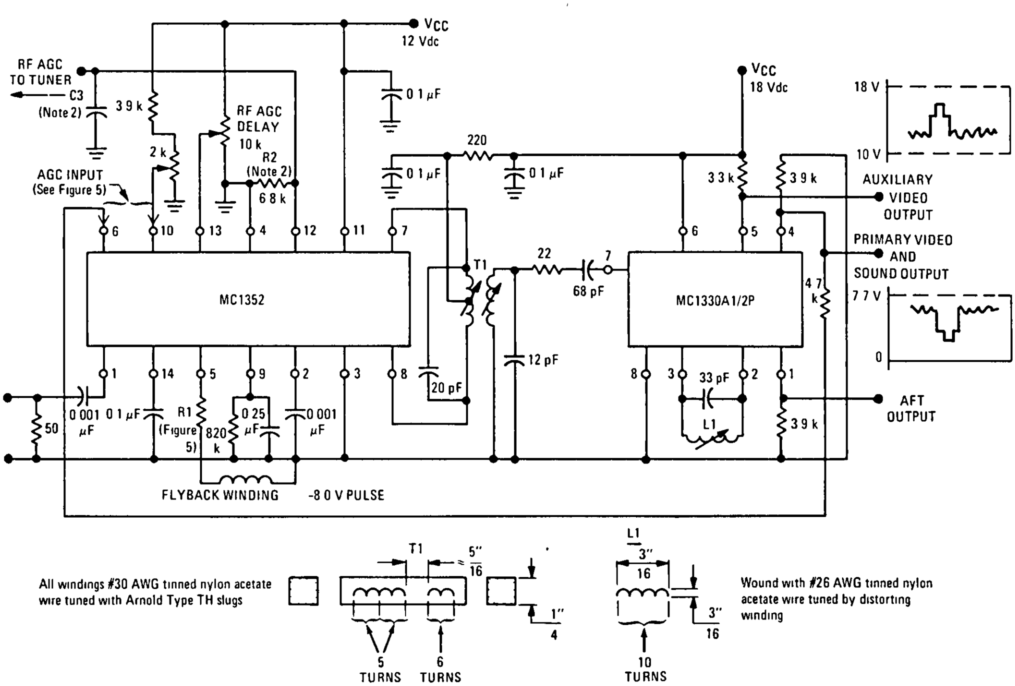
FIGURE 1 – TYPICAL VIDEO IF AMPLIFIER APPLICATION



MAXIMUM RATINGS (Voltages referenced to pin 4, ground; T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply (Pin 11)	+18	Vdc
Output Supply (Pins 7 and 8)	+18	Vdc
Signal Input Voltage (Pin 1 or 2, other pin ac grounded)	10	V_{p-p}
AGC Input Voltage (Pin 6 or 10, other pin ac grounded)	+6 0	Vdc
Gating Voltage, Pin 5	+10, -20	Vdc
Power Dissipation Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, Voltages referenced to pin 4, ground; T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
AGC Range	–	75	–	dB
Power Gain f = 35 MHz or 45 MHz f = 58 MHz	 – –	 52 50	 – –	dB
Maximum Differential Output Voltage Swing 0 dB AGC -30 dB AGC	 – –	 16.8 8.4	 – –	V_{p-p}
Voltage Range for RF-AGC at Pin 12 Maximum Minimum	 – –	 7.0 0 2	 – –	Vdc
IF Gain Change Over RF-AGC Range	–	10	–	dB
Output Stage Current ($I_7 + I_8$)	–	5.7	–	mAdc
Total Supply Current ($I_7 + I_8 + I_{11}$)	–	27	31	mAdc
Total Power Dissipation	–	325	370	mW

DESIGN PARAMETERS, TYPICAL VALUES (V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted)

Parameters	Symbol	f = 35 MHz	f = 45 MHz	f = 58 MHz	Unit
Single-Ended Input Admittance	g_{11} b_{11}	0.55 2.25	0.70 2 80	1.1 3 75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	50 0	60 0	– –	μmhos
Differential Output Admittance	g_{22} b_{22}	20 430	40 570	75 780	μmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	3 0 80	4.0 100	– –	μmhos
Reverse Transfer Admittance	$\lvert y_{12} \rvert$	<<1 0	<<1.0	<<1.0	μmho
Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (-30 dB AGC)	 $\lvert y_{12} \rvert$ $\angle y_{21}$ $\angle y_{21}$	 260 -73 -52	 240 -100 -72	 210 -135 -96	 mmhos degrees
Single-Ended Input Capacitance	–	9.5	10	10.5	pF
Differential Output Capacitance	–	2.0	2.0	2.5	pF

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FIGURE 2 – CIRCUIT SCHEMATIC

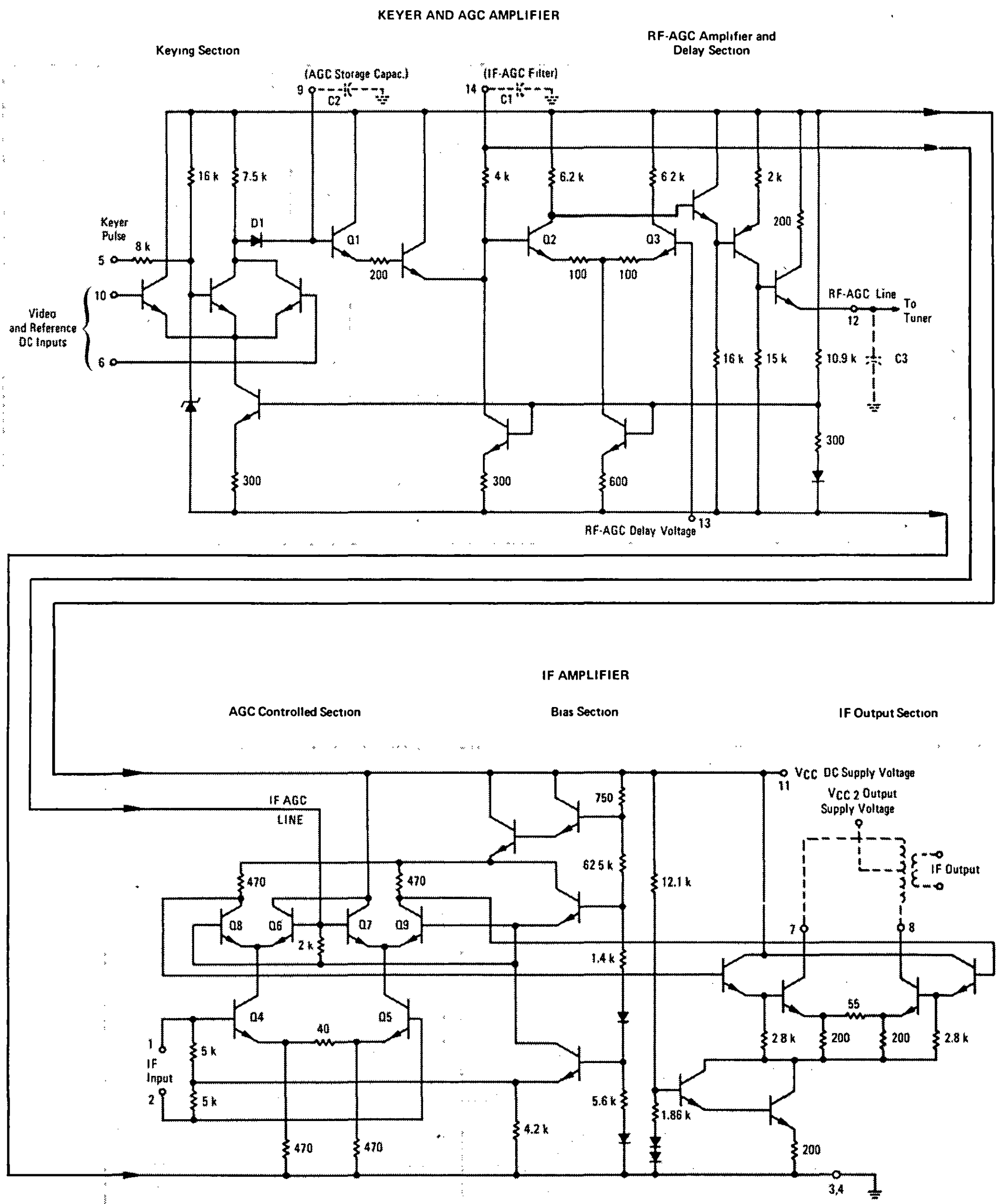
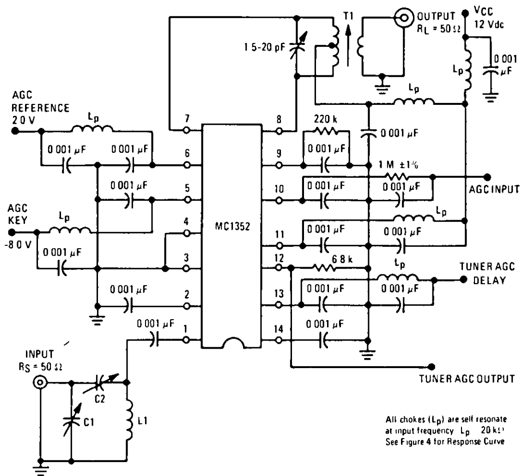


FIGURE 3 – POWER GAIN, AGC AND NOISE TEST CIRCUIT



	35 and 45 MHz		58 MHz	
L1	0 4 µH	Q ≥ 100	0 3 µH	Q ≥ 100
T1	1 3-3 4 µH	Q ≥ 100 @ 2 µH	1 2-3 8 µH	Q ≥ 100 @ 2 µH
C1	48-100 pF		40-80 pF	
C2	8-60 pF		12-45 pF	

L1 and T1 = #26 AWG Tinned Nylon Acetate Wire

L1 @ 35 or 45 MHz = 7 1/4 Turns on a 1/4 coil form
@ 58 MHz = 6 Turns on a 1/4 coil form
T1 Primary Winding = 18 Turns on a 1/4 coil form
Secondary Winding = 2 Turns Wound Evenly over Primary Winding for 35 or 45 MHz and 1 Turn for 58 MHz
Slug = Arnold TH Material 1/2 long

GENERAL OPERATING INFORMATION

The MC1352 consists of an AGC section and an IF signal amplifier (Figure 2) subdivided into different functions as indicated by the illustration.

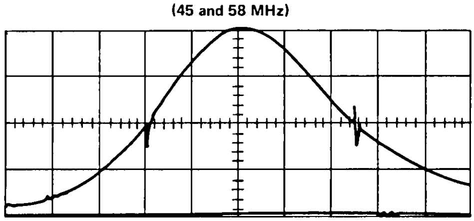
A gating pulse, a reference level, and a composite video signal are required for proper operation of the AGC section. Either positive or negative-going video may be used; necessary connections and signal levels are shown in Figure 1. The essential difference is that the video is fed into Pin 10 and the AGC reference level is applied to Pin 6 for a video signal with positive-going sync while the input connections are reversed for negative-going sync.

The action of the gating section is such that the proper voltage, V_C, is maintained across the external capacitor, C2, for a particular video level and dc reference setting. The voltage V_C, is the result of the charge delivered through D1 and the charge drained by Q1. The charge delivered occurs during the time of the gating pulse, and its magnitude is determined by the amplitude of the video signal relative to the dc reference level. The voltage V_C is delivered via the IF-AGC amplifier and applied to the variable gain stage of the IF signal amplifier and is also applied to the RF-AGC amplifier, where it is compared to the fixed RF-AGC delay voltage reference by the differential amplifier, Q2 and Q3. The following stages amplify the output signal of Q2 and shift the dc levels causing the RF-AGC voltage to vary.

The input amplifiers (Q4 and Q5) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac). Terminals 1 and 2 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q6 and Q7 causing those transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q8 and Q9. The output amplifiers are fed from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant.

FIGURE 4 – TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)



Scale 1 MHz/cm

NOTES:

1. The 12-V supply must have a low ac impedance to prevent low-frequency instability in the RF-AGC loop. This can be achieved by a 12-V zener diode and a large decoupling capacitor. (5 µF).

2. Choices of C1, C2 and C3 depend somewhat on the set designers' preference concerning AGC stability versus AGC recovery speed Typical values are C1 = 0.1 µF, C2 = 0 25 µF, C3 = 10 µF

3. To set a fixed IF-AGC operating point (e g , for receiver alignment) connect a 22 kΩ resistor from pin 9 to pin 11 to give minimum gain, then bias pin 14 to give the correct operating point using a 200 kΩ variable resistor to ground

4. Although the unit will normally be operating with a very high power gain, the pin configuration has been carefully chosen so that shielding between input and output terminals will not normally be necessary even when a standard socket is used.

FIGURE 5 – TYPICAL AGC APPLICATION CHART

Video Polarity	Pin 6 Voltage	Pin 10 Voltage	Pin 5 R1 (Ω)
Negative-Going Sync	5.5 / 2 0 / 0 (waveform)	Adj. 1.0–4 0 Vdc Nom 2.0 V	0
Positive-Going Sync	Adj 1.0–8.0 Vdc Nom 4 5 V	4 5 / 0 (waveform)	3 9 k

TYPICAL CHARACTERISTICS

(V_{CC} = +12 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE

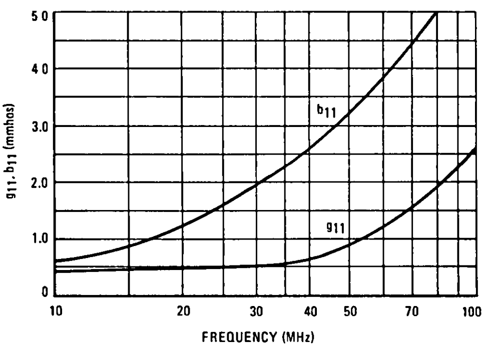


FIGURE 7 – DIFFERENTIAL OUTPUT ADMITTANCE

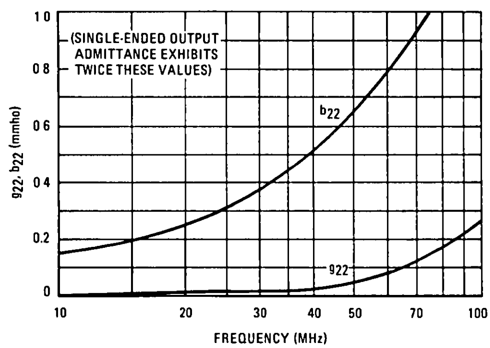


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

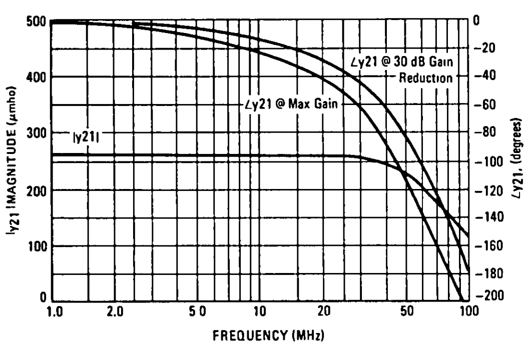


FIGURE 9 – DIFFERENTIAL OUTPUT VOLTAGE

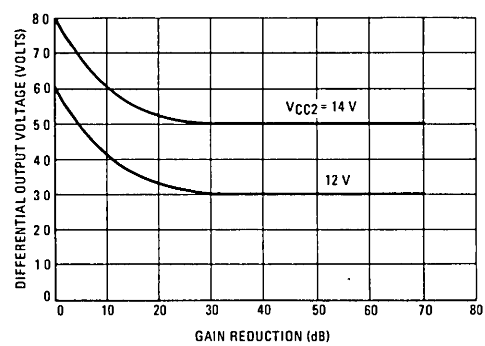


FIGURE 10 – AGC CHARACTERISTICS

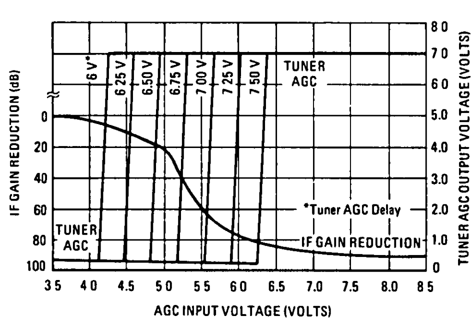
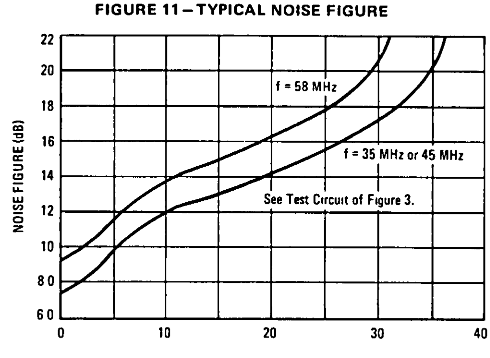


FIGURE 11 – TYPICAL NOISE FIGURE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1355P	0°C to +75°C	Plastic DIP

MC1355

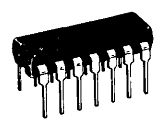
BALANCED FOUR-STAGE HIGH-GAIN FM/IF AMPLIFIER

. . . designed for use with Foster-Seeley discriminator or ratio detector in high quality FM systems.

- High AM Rejection (60 dB typ)
- Wide Range of Supply Voltages (8 to 18 Vdc)
- Low Distortion (0.5% typ)

LIMITING FM IF AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

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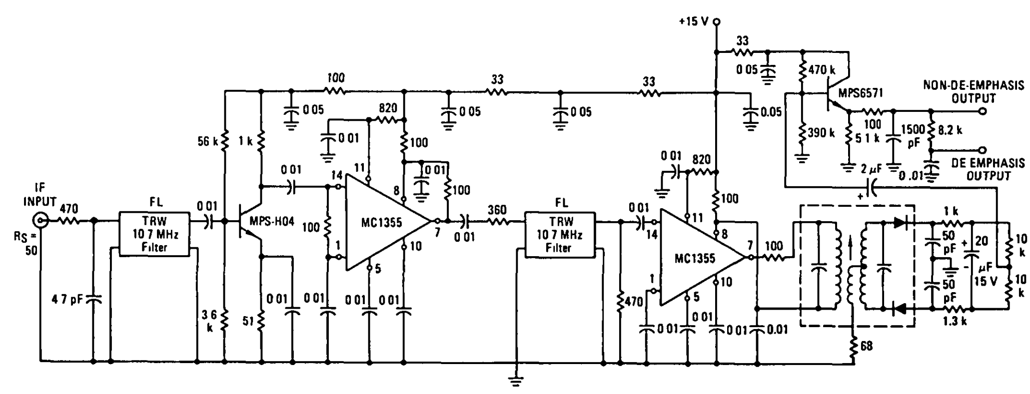
FIGURE 1 – DUAL MC1355 FM IF APPLICATION



*All other pins grounded
T-Ratio Detector (input impedance ≅ 1.5 k) G.I. #36231 or equivalent

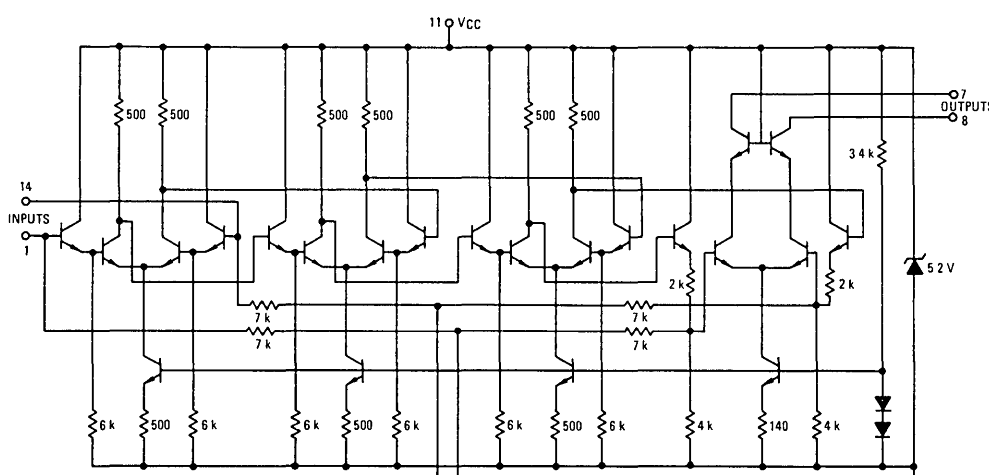
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Output Voltage (pins 7 & 8)	40	Vdc
Supply Current to pin 11	20	mA
Input Signal Voltage (single-ended)	5.0	Vp-p
Input Signal Voltage (differential)	10	Vp-p
Power Dissipation (package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 Vdc, f = 10 7 MHz, T_A = +25°C)

Characteristic	Min	Typ	Max	Units
Power Supply Voltage Range	8 0	15	18	Vdc
Total Circuit Current	–	16	–	mAdc
Total Output Stage Current	–	4.2	–	mA
Device Dissipation	–	125	–	mW
Internal Zener Voltage	–	5.2	–	Vdc
Input Signal for 3 dB Limiting	–	175	300	µV(rms)
Output Current Swing	3.5	4.2	5.0	mA p-p
AM Rejection (10 mv to 1.0 v (rms) input, FM @ 100%, AM @ 80%, Foster Seeley detector)	–	60	–	dB
Admittance Parameters Y_{11}	–	120 + j320	–	µmhos
Y_{12}	–	j0.6	–	µmho
Y_{21}	–	8 + j5 9	–	mhos
Y_{22}	–	15 + j230	–	µmhos

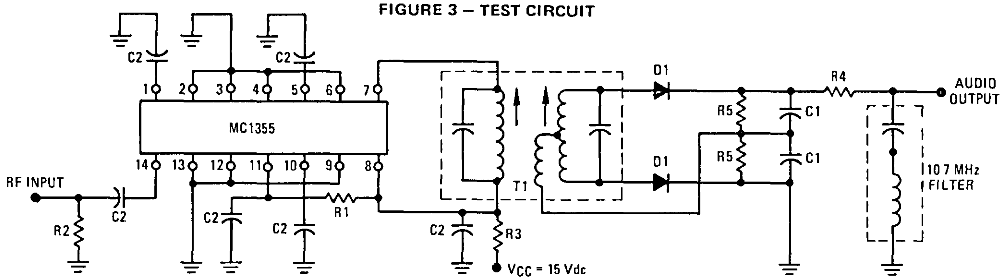
FIGURE 2 – CIRCUIT SCHEMATIC



Pins 2, 3, 6, 9, 12, and 13 are not internally connected but should be grounded for maximum stability

TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT



R1 820 ohms
R2 50 ohms
R3 100 ohms
R4 5 kilohms
R5 12 kilohms

C1 50 pF
C2 0 01 μF
T1 10 7 MHz Foster Seeley Discriminator, Primary Impedance = 3 9 k, Peak to-Peak Separation = 600 kHz

D1 Small Signal Germanium Diode (1N542 or equiv)

Specifications are given for a Foster-Seeley discriminator. Improved AM rejection at low signal levels can be obtained with a ratio detector.

For optimum circuit stability it is important to ground pins 2, 3, 4, 6, 9, 12, and 13.

FIGURE 4 – AM REJECTION TEST BLOCK DIAGRAM

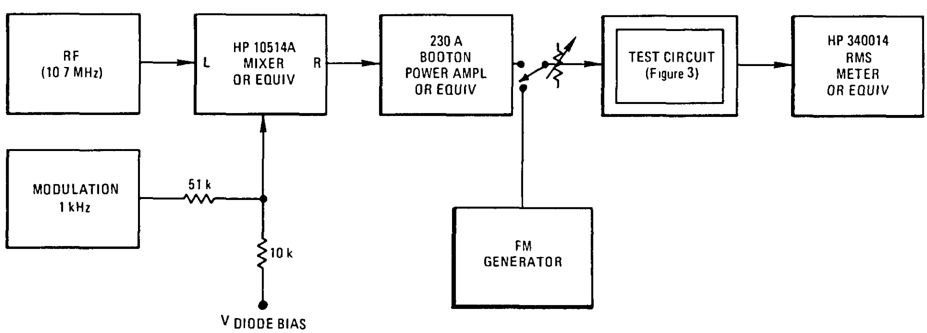


FIGURE 5 – LIMITING

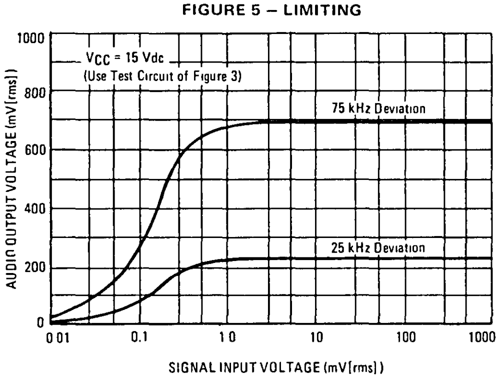
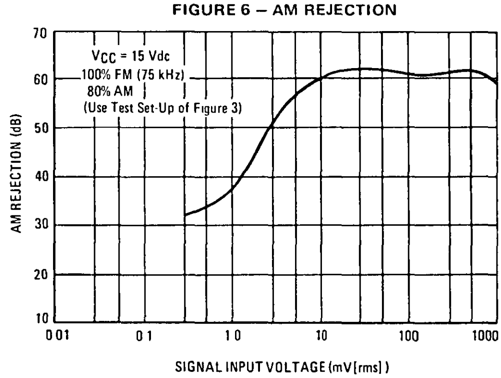


FIGURE 6 – AM REJECTION



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TYPICAL CHARACTERISTICS (continued)

FIGURE 7 — OUTPUT DISTORTION

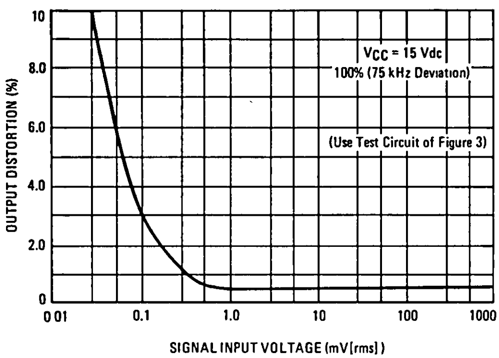


FIGURE 8 — SIGNAL-TO-NOISE RATIO SIGNAL

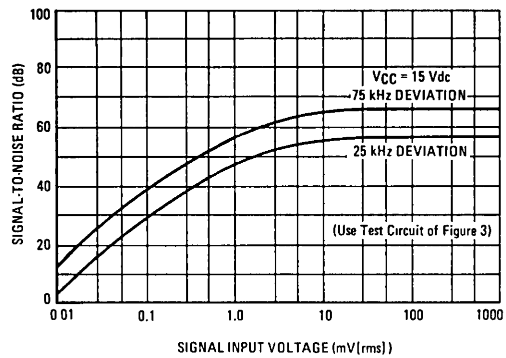
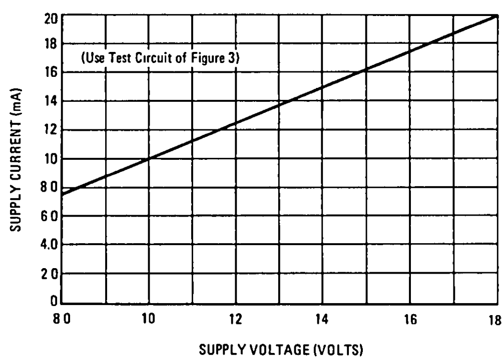


FIGURE 9 — TOTAL SUPPLY CURRENT



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ORDERING INFORMATION

Device	Temperature Range	Package
MC1357P	0°C to +75°C	Plastic DIP

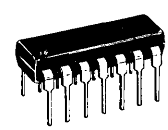
MC1357

TV SOUND IF OR FM IF AMPLIFIER WITH QUADRATURE DETECTOR

- A Direct Replacement for the ULN2111A
- Greatly Simplified FM Demodulator Alignment
- Excellent Performance at V_{CC} = 8.0 Vdc

IF AMPLIFIER AND QUADRATURE DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

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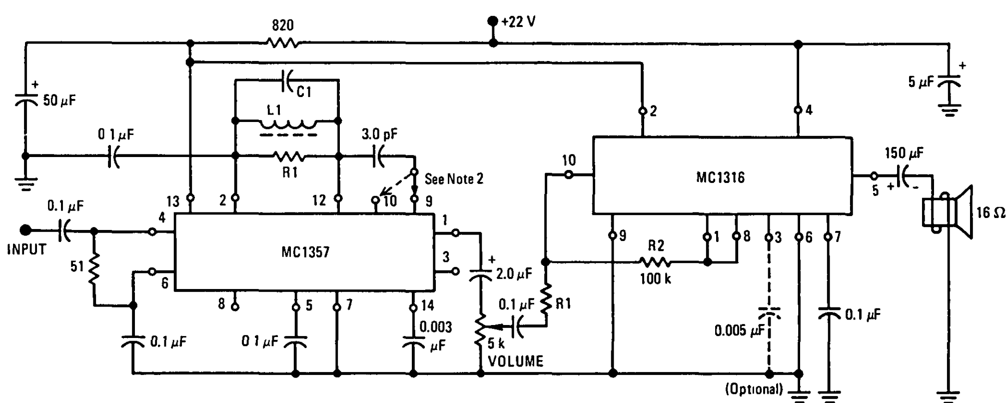
FIGURE 1 – TV TYPICAL APPLICATION CIRCUIT



Typical Performance.
2 Watts Output
2% Distortion
250 µV Sensitivity (3 dB Lim.)

C1 = 120 pF
L1 = 14 µH
R1 = 20 kΩ
Q = 30

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Vdc
Input Voltage (Pin 4)	3.5	V_p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic		Pin	Min	Typ	Max	Units
Drain Current	V_{CC} = 8 V V_{CC} = 12 V	13	10 –	12 15	19 21	mA
Amplifier Input Reference Voltage		6	–	1.45	–	Vdc
Detector Input Reference Voltage		2	–	3.65	–	Vdc
Amplifier High Level Output Voltage		10	1.25	1.45	1.65	Vdc
Amplifier Low Level Output Voltage		9	–	0.145	0.2	Vdc
Detector Output Voltage	V_{CC} = 8 V V_{CC} = 12 V	1	– –	3.7 5.4	– –	Vdc
Amplifier Input Resistance		4	–	5.0	–	kΩ
Amplifier Input Capacitance		4	–	11	–	pF
Detector Input Resistance		12	–	70	–	kΩ
Detector Input Capacitance		12	–	2.7	–	pF
Amplifier Output Resistance		10	–	60	–	ohms
Detector Output Resistance		1	–	200	–	ohms
De-Emphasis Resistance		14	–	8.8	–	kΩ

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DYNAMIC CHARACTERISTICS (FM Modulation Freq. = 1.0 kHz, Source Resistance = 50 ohms, T_A = +25°C for all tests.)

(V_{CC} = 12 Vdc, f_o = 4.5 MHz, Δf = ±25 kHz, Peak Separation = 150 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \le 50$ μV[rms])	10	–	60	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	36	–	dB
Input Limiting Threshold Voltage	4	–	250	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.72	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	3	–	%

(V_{CC} = 12 Vdc, f_o = 5.5 MHz, Δf = ±50 kHz, Peak Separation = 260 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \le 50$ μV[rms])	10	–	60	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	40	–	dB
Input Limiting Threshold Voltage	4	–	250	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	1.2	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	5	–	%

(V_{CC} = 8.0 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \le 50$ μV[rms])	10	–	53	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	37	–	dB
Input Limiting Threshold Voltage	4	–	600	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.30	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	1.4	–	%

(V_{CC} = 12 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \le 50$ μV[rms])	10	–	53	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	45	–	dB
Input Limiting Threshold Voltage	4	–	600	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.48	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	1.4	–	%

*100% FM, 30% AM Modulation

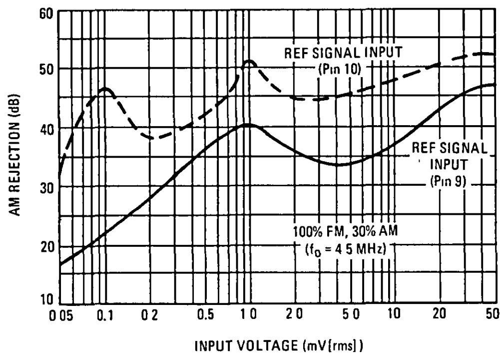
TYPICAL CHARACTERISTICS

(V_{CC} = 12 V, T_A = +25°C unless otherwise noted)

(Use Test Circuit of Figure 13)

(f_o = 4.5 MHz)

FIGURE 2 – AM REJECTION



(f_o = 5.5 MHz)

FIGURE 3 – AM REJECTION

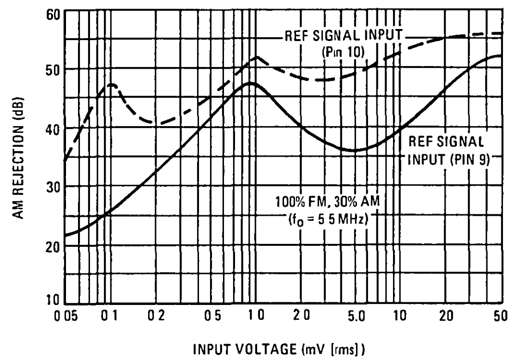


FIGURE 4 – DETECTED AUDIO OUTPUT

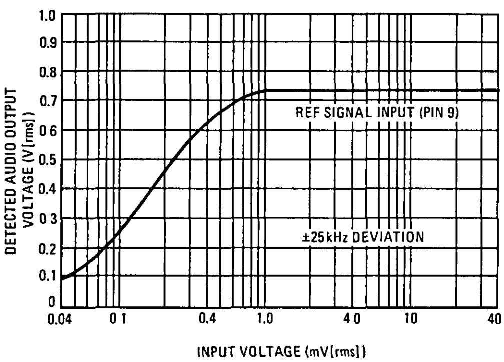


FIGURE 5 – DETECTED AUDIO OUTPUT

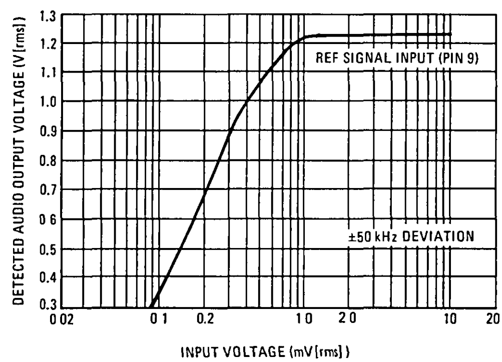


FIGURE 6 – DETECTOR TRANSFER CHARACTERISTIC

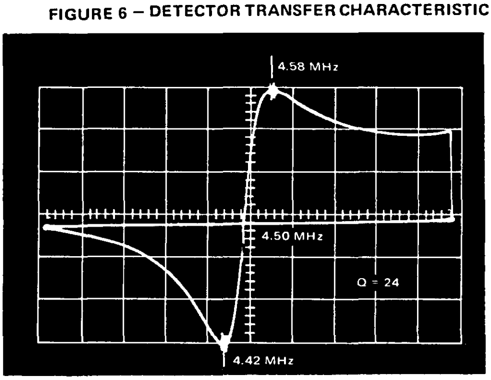
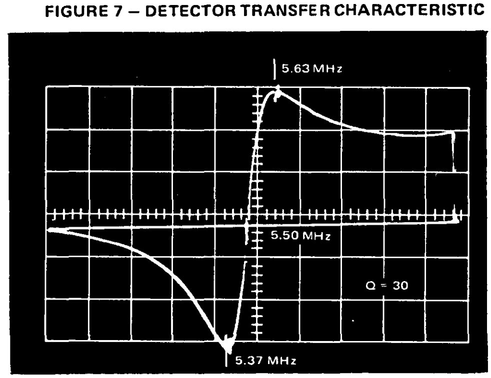


FIGURE 7 – DETECTOR TRANSFER CHARACTERISTIC



TYPICAL CHARACTERISTICS (continued)

(f_o = 10.7 MHz, T_A = +25°C unless otherwise noted.)
(Use Test Circuit of Figure 13)

FIGURE 8 – AM REJECTION

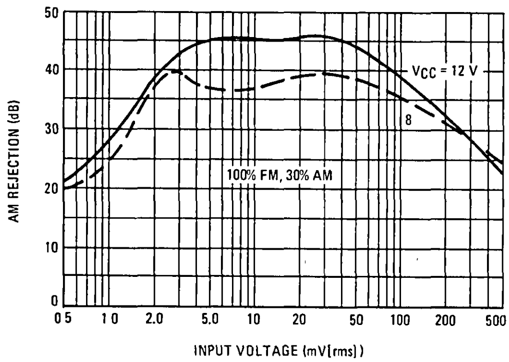


FIGURE 9 – AFC VOLTAGE DRIFT (1.0 mV INPUT CARRIER @ 10.7 MHz)

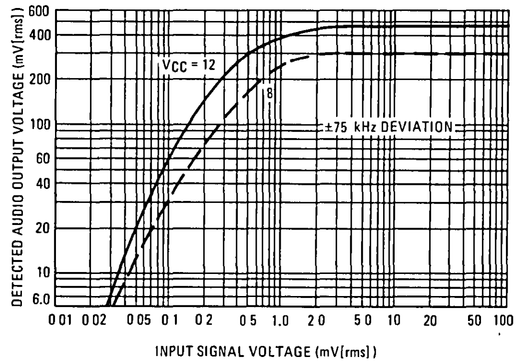


FIGURE 10 – LIMITING

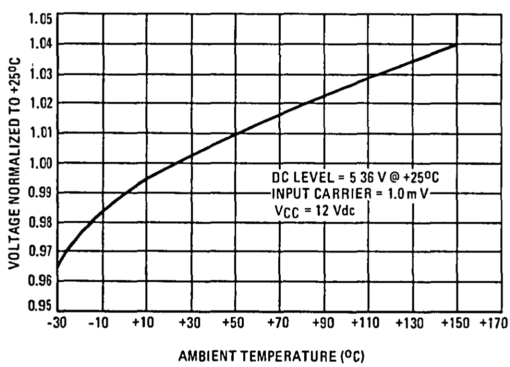


FIGURE 11 – SIGNAL-TO-NOISE RATIO

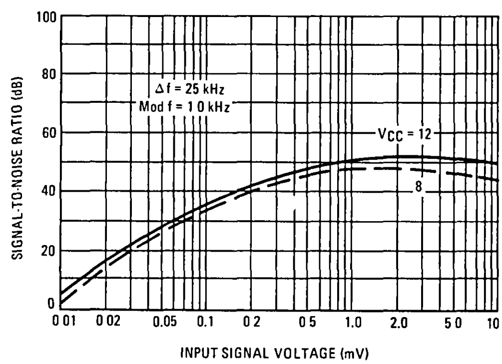


FIGURE 12 – DETECTOR TRANSFER CHARACTERISTIC

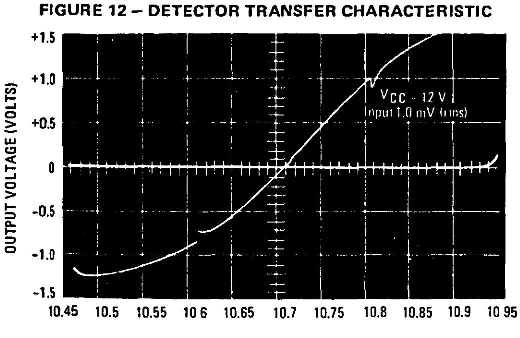
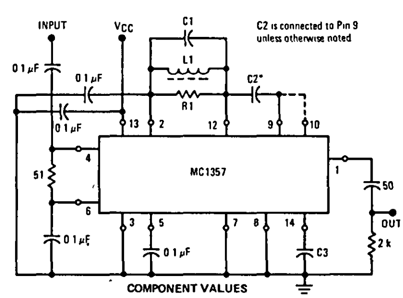


FIGURE 13 – TEST CIRCUIT



COMPONENT VALUES

f	L1	C1	R1	Q(R1, L1)	C2	C3
MHz	μH	pF	kΩ		pF	μF
4 5	14	120	20	30	3 0	0 003
5 5	8 0	100	20	30	3 0	0 003
10.7	2.0	120	3.9	30	4.7	0.01

FIGURE 14 – FM RADIO TYPICAL APPLICATION CIRCUIT

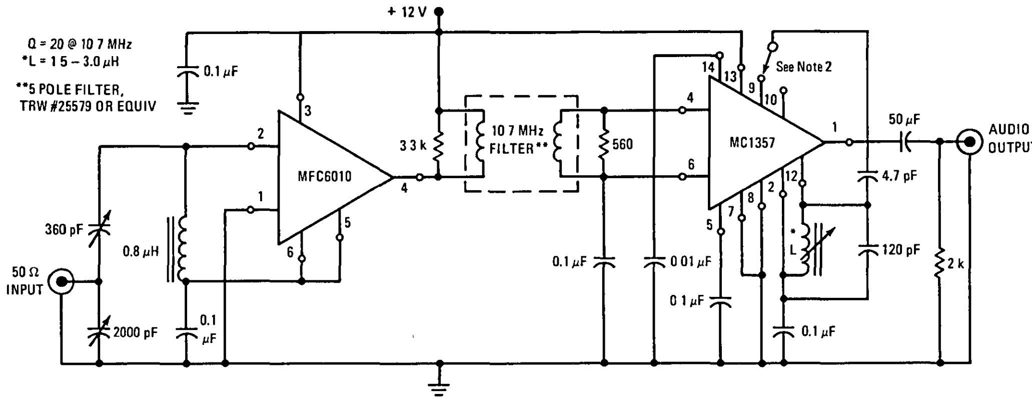
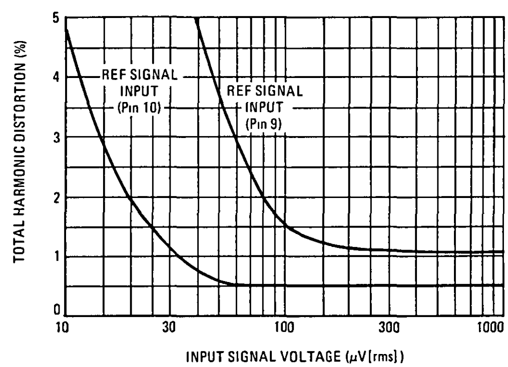


FIGURE 15 – OUTPUT DISTORTION



Note 1:
Information shown in Figures 15, 16, and 17 was obtained using the circuit of Figure 14.

Note 2:
Optional input to the quadrature coil may be from either pin 9 or pin 10 in the applications shown. Pin 9 has commonly been used on this type of part to avoid overload with various tuning techniques. For this reason, pin 9 is used in tests on the preceding pages (except as noted). However, a significant improvement of limiting sensitivity can be obtained using pin 10, see Figure 17, and no overload problems have been incurred *with this tuned circuit configuration.*

FIGURE 16 – SIGNAL-TO-NOISE RATIO

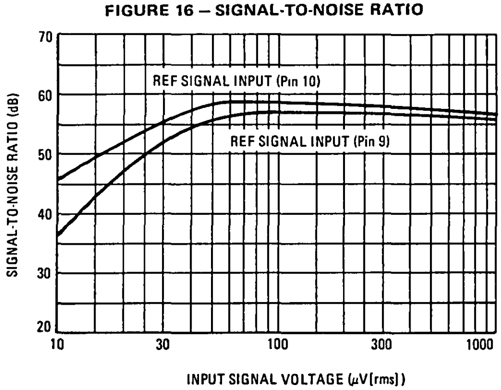


FIGURE 17 – RECOVERED AUDIO OUTPUT

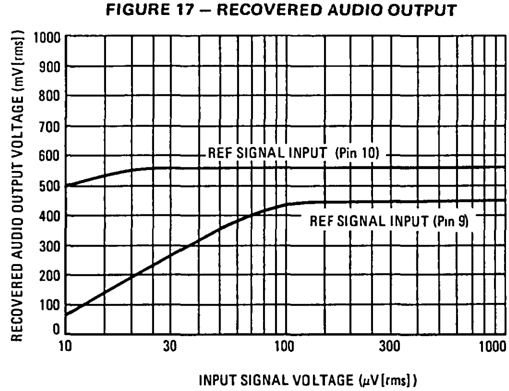
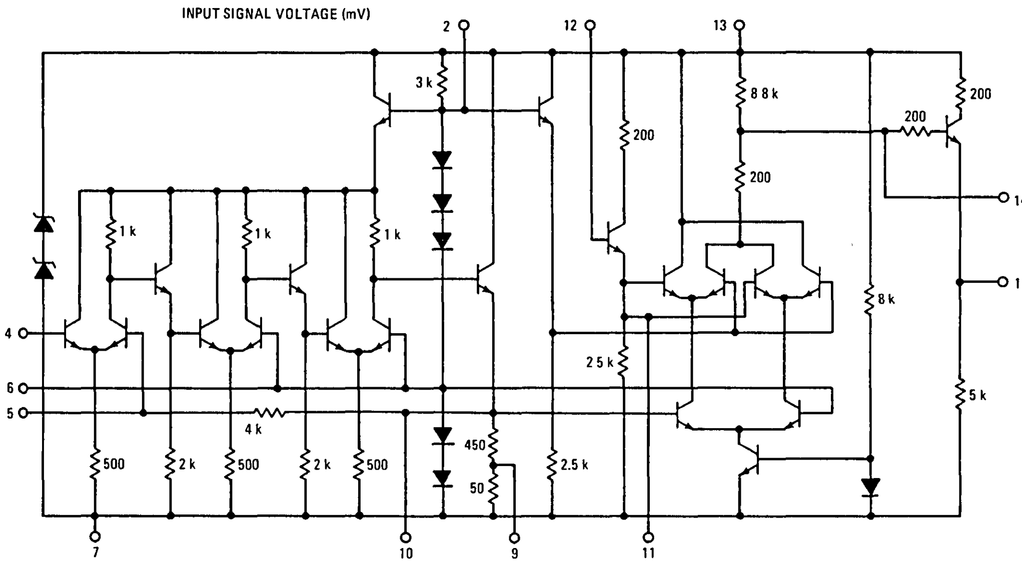


FIGURE 18 — CIRCUIT SCHEMATIC



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ORDERING INFORMATION

Device	Temperature Range	Package
MC1358P	−20°C to +75°C	Plastic DIP
MC1358PQ	−20°C to +75°C	Plastic

MC1358

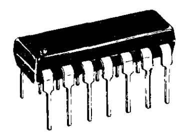
TV SOUND IF AMPLIFIER

. . . a versatile monolithic device incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

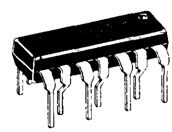
- Direct Replacement for the CA3065
- Differential Peak Detector Requiring a Single Tuned Circuit
- Electronic Attenuator Replaces Conventional ac Volume Control — Range > 60 dB
- Excellent AM Rejection @ 4.5 and 5.5 MHz
- High Stability
- Low Harmonic Distortion
- Audio Drive Capability — 6.0 mAp-p
- Minimum Undesirable Output Signal @ Maximum Attenuation

IF AMPLIFIER, LIMITER, FM DETECTOR, AUDIO DRIVER, ELECTRONIC ATTENUATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

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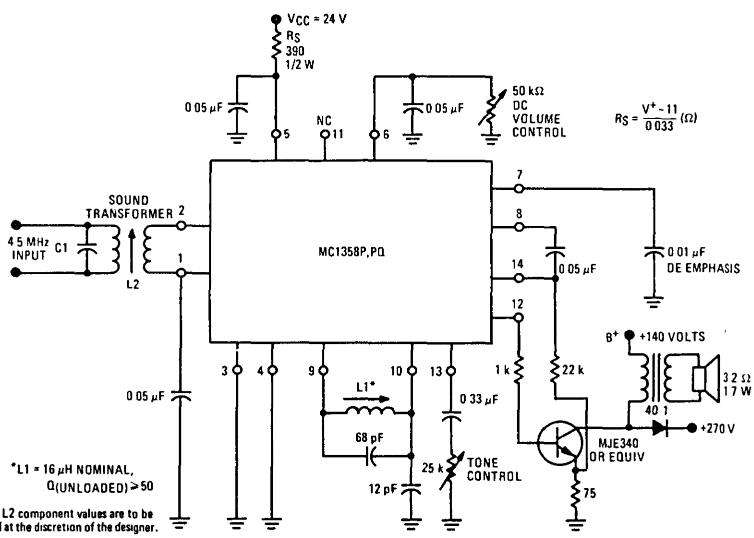
FIGURE 1 — TYPICAL TV APPLICATION CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Input Signal Voltage (Pins 1 and 2)	±3.0	Vdc
Power Supply Current	50	mA
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C unless otherwise noted).

Characteristic	Pin	Min	Typ	Max	Unit
Regulated Voltage	5	10.3	11	12.2	Vdc
DC Supply Current (V^+ = 9 Vdc, R_S = 0)	5	10	16	24	mA
Quiescent Output Voltage	12	–	5.1	–	Vdc

DYNAMIC CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C unless otherwise noted).

Characteristic	Min	Typ	Max	Unit
IF AMPLIFIER AND DETECTOR				
f_o = 4.5 MHz, Δf = ±25 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	51	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	0 5	0.70	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.4	2.0	%
f_o = 5.5 MHz, Δf = ±50 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	53	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV [rms])	0.5	0 91	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.9	–	%
Input Impedance Components (f = 4.5 MHz, measurement between pins 1 and 2) Parallel Input Resistance Parallel Input Capacitance	 – –	 17 4.0	 – –	 kΩ pF
Output Impedance Components (f = 4.5 MHz, measurement between pin 9 and GND) Parallel Output Resistance Parallel Output Capacitance	 – –	 3.25 3.6	 – –	 kΩ pF
Output Resistance, Detector Pin 7 Pin 8	 – –	 7.5 250	 – –	 kΩ Ω
ATTENUATOR				
Volume Reduction Range (See Figure 8) (dc Volume Control = ∞)	60	–	–	dB
Maximum Undesirable Signal (See Note 1) (dc Volume Control = ∞)	–	0.07	1.0	mV
AUDIO AMPLIFIER				
Voltage Gain (V_{in} = 0.1 V(rms), f = 400 Hz)	17.5	20	–	dB
Total Harmonic Distortion (V_o = 2.0 V(rms), f = 400 Hz)	–	2.0	–	%
Output Voltage (THD = 5%, f = 400 Hz)	2.0	3.0	–	V(rms)
Input Resistance (f = 400 Hz)	–	70	–	kΩ
Output Resistance (f = 400 Hz)	–	270	–	Ω

*100% FM, 30% AM Modulation.

Note 1. Undesirable signal is measured at pin 8 when volume control is set for minimum output.

TYPICAL CHARACTERISTICS

(V_{CC} = 24 Vdc, T_A = +25°C unless otherwise noted)

(f_o = 4.5 MHz)

FIGURE 2 – AM REJECTION

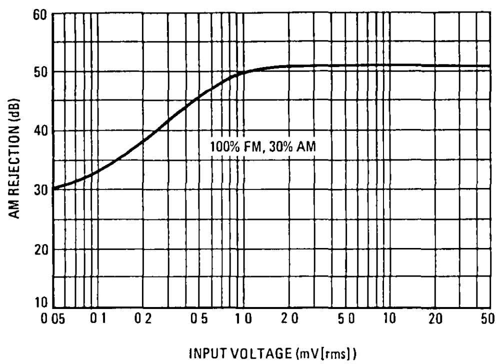


FIGURE 4 – DETECTED AUDIO OUTPUT

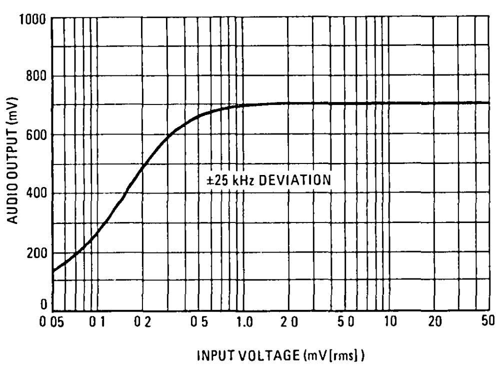
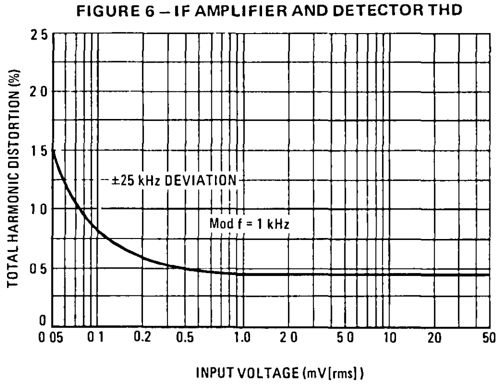


FIGURE 6 – IF AMPLIFIER AND DETECTOR THD



(f_o = 5.5 MHz)

FIGURE 3 – AM REJECTION

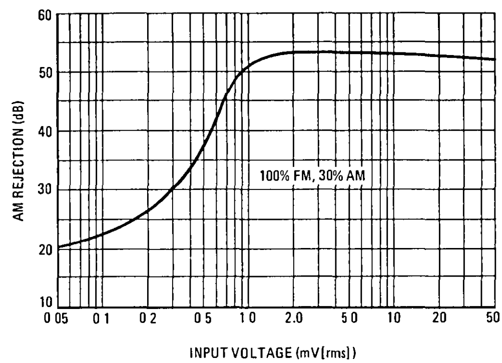


FIGURE 5 – DETECTED AUDIO OUTPUT

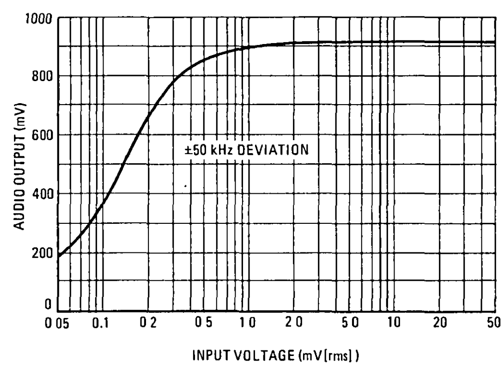
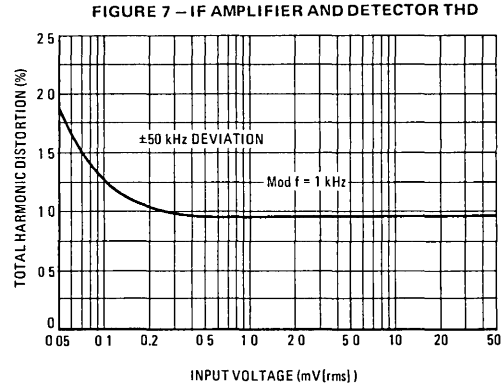


FIGURE 7 – IF AMPLIFIER AND DETECTOR THD



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TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – GAIN REDUCTION OF ATTENUATOR

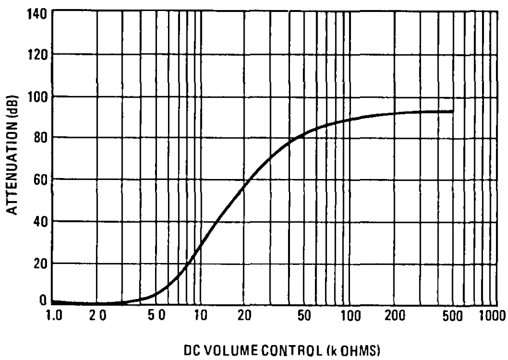

FIGURE 9 – AUDIO AMPLIFIER THD

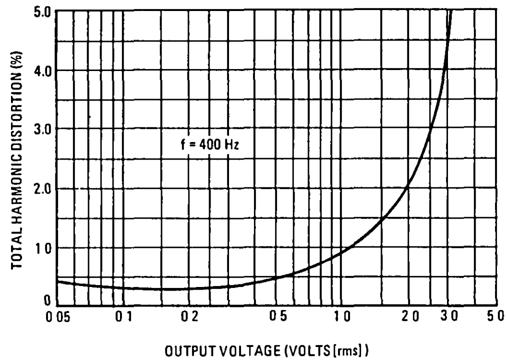

FIGURE 10 – IF FREQUENCY RESPONSE

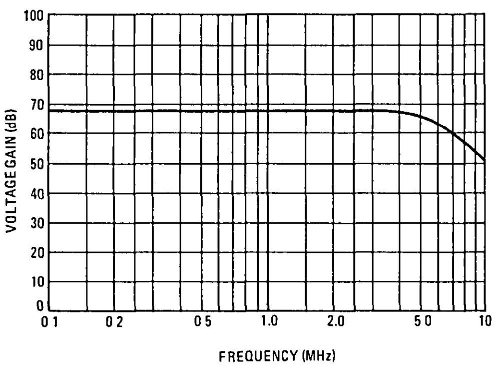

FIGURE 11 – IF FREQUENCY RESPONSE TEST CIRCUIT

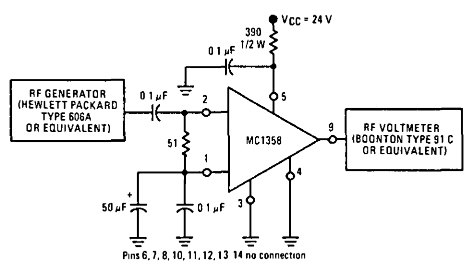

FIGURE 12 – AM REJECTION, DETECTED AUDIO, THD, ATTENUATION TEST CIRCUIT

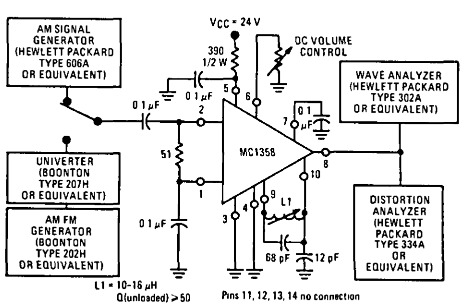

FIGURE 13 – AUDIO VOLTAGE GAIN, AUDIO THD TEST CIRCUIT

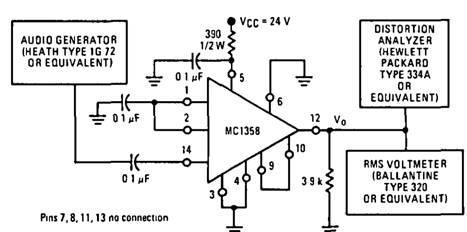

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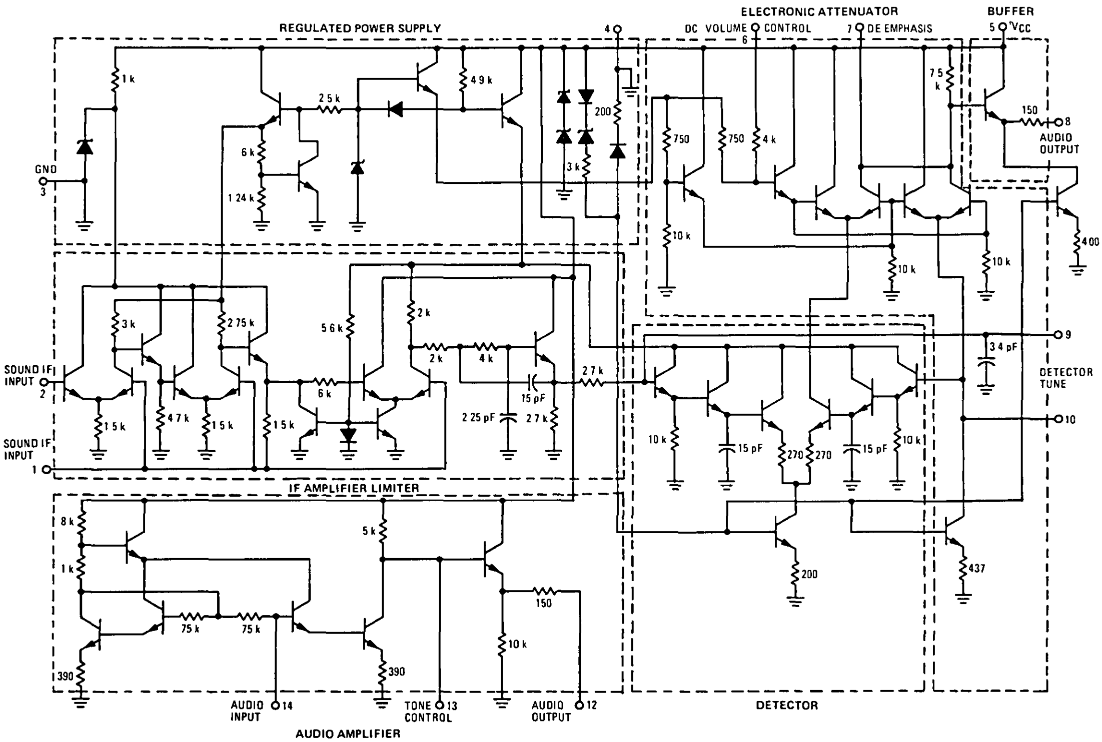
FIGURE 14 — CIRCUIT SCHEMATIC



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ORDERING INFORMATION

Device	Temperature Range	Package
MC1364P	0°C to +75°C	Plastic DIP

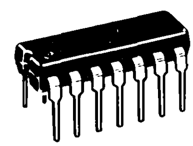
MC1364

TV AUTOMATIC FREQUENCY CONTROL

- High Gain Amplifier – 18 mV Input for Full Output
- Direct Replacement for the CA3064
- Also Available in the 14-Lead Dual In-Line Package

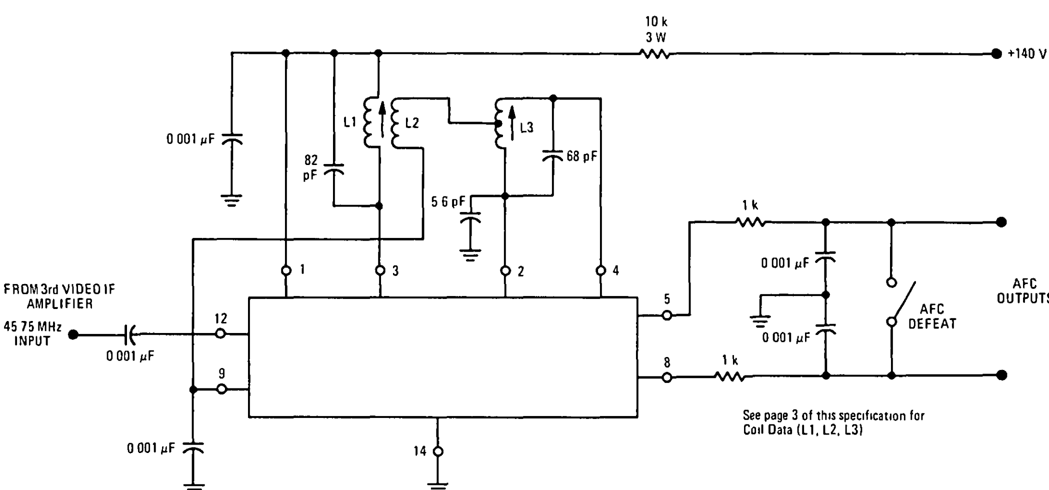
AUTOMATIC FREQUENCY CONTROL

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
CASE 646
PLASTIC PACKAGE

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



See page 3 of this specification for Coil Data (L1, L2, L3)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	MC1364P	Unit
Input Signal Voltage (Pin 12 to 14)	+2 0, -10	Vdc
Output Collector Voltage (Pins 3 and 14)	20	Volts
Power Dissipation (Package Limitation) Derate above T_A = +25°C	625 5 0	mW mW/°C
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	-65 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +30 Vdc, T_A = +25°C, see Test Circuit of Figure 4 unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Total Device Dissipation	–	140	–	mW
Total Supply Current	–	12	–	mA
Current Drain, Total (Reduce V_{CC} so that V10 = 10 5 Vdc)	4 0	6 5	9.5	mA
Zener Regulating Voltage	10 9	11 8	12 8	V
Quiescent Current to Pin 3	1.0	2.0	4 0	mA
Quiescent Voltage at Pin 5 or Pin 8	5 0	6 6	8.0	V
Output Offset Voltage (Pin 5 to Pin 8)	-1.0	0	+1.0	V

DESIGN PARAMETERS, TYPICAL VALUES (V_{CC} = +30 Vdc, R_S = 1.5 k, f = 45.75 MHz)

Parameter	Symbol	Typ	Unit
Input Admittance	y_{11}	0 4 + j1	mmho
Reverse Transfer Admittance	y_{12}	0 + j3 4	μmho
Forward Transfer Admittance	y_{21}	110 + j140	mmhos
Output Admittance (Pin 3)	y_{22}	0.02 + j1	mmho

TYPICAL CHARACTERISTICS

(See Test Circuit of Figure 2)

FIGURE 2 – TYPICAL NARROW BAND DYNAMIC CHARACTERISTICS

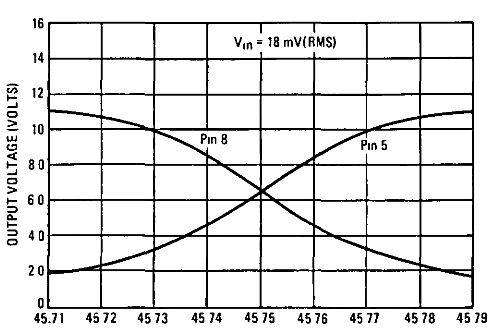


FIGURE 3 – TYPICAL WIDE BAND DYNAMIC CHARACTERISTICS

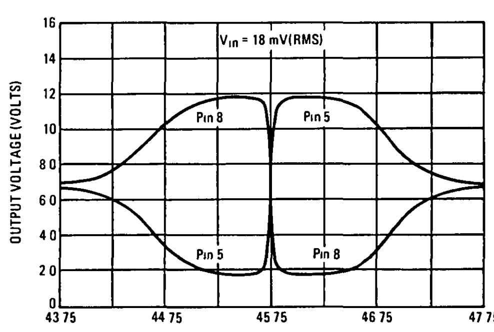
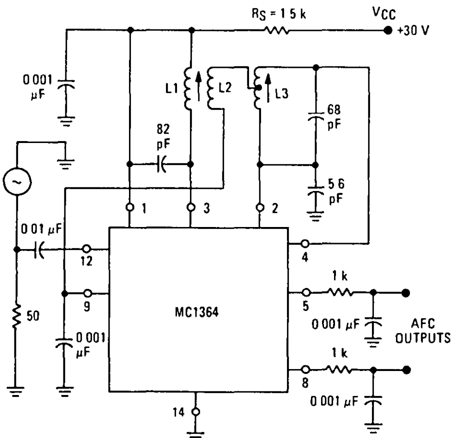


FIGURE 4 – TEST CIRCUIT



$$R_S = \frac{V_{CC} - 11.8}{0.012} \text{ ohms}$$

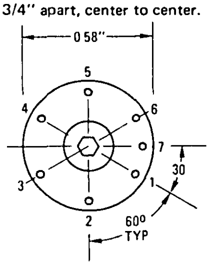
COIL DATA FOR DISCRIMINATOR WINDINGS FOR FIGURES 1 AND 4

L1 – Discriminator Primary. 3-1/6 turns; AWG #20 enamel-covered wire – close-wound, at bottom of coil form. Inductance of L1 = 0.165 µH; Q_O = 120 at f_O = 45.75 MHz.
Start winding at Terminal #6, finish at Terminal #1. See Notes below.

L2 – Tertiary Windings. 2-1/6 turns; AWG #20 enamel-covered wire – close-wound over bottom end of L1.
Start winding at Terminal #3, finish at Terminal #4. See Notes below.

L3 – Discriminator Secondary. 3-1/2 turns; AWG #20 enamel-covered wire, center-tapped, space wound at bottom of coil form.
Start winding at Terminal #2, finish at Terminal #5, connect center tap to Terminal #7. See Notes below.

Notes:
1. Coil Forms, Cylindrical, -0.30" Dia. Max.
2. Tuning Core: 0.250" Dia. x 0.37" Length. Material: Carbinal J or equivalent.
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.
5. Mount the coils 3/4" apart, center to center.



(Bottom view of coil form)

FIGURE 5 – CIRCUIT SCHEMATIC

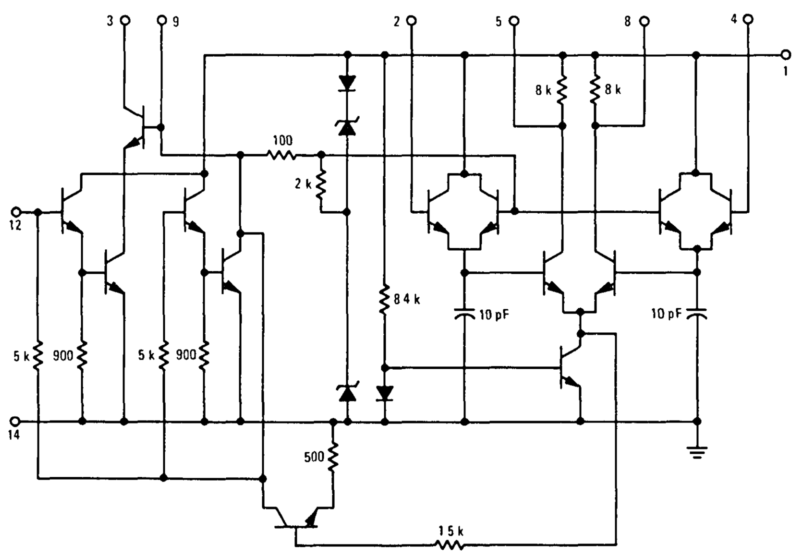
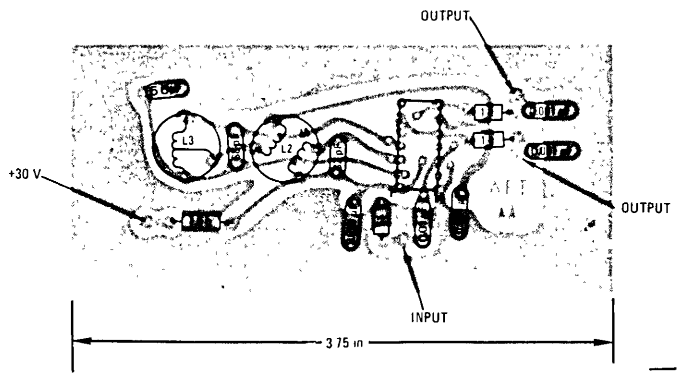


FIGURE 6 – PRINTED CIRCUIT BOARD AND PARTS ARRANGEMENT
(Copper Side)



MC1372

COLOR TV VIDEO MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

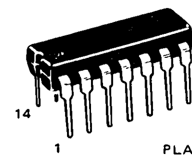
COLOR TV VIDEO MODULATOR

. . . an integrated circuit used to generate an RF TV signal from baseband color-difference and luminance signals.

The MC1372 contains a chroma subcarrier oscillator, lead and lag network, a quasi-quadrature suppressed carrier DSB chroma modulator, an RF oscillator and modulator, and a TTL compatible clock driver with adjustable duty cycle.

The MC1372 is a companion part to the MC6847 Video Display Generator, providing and accepting the correct dc interconnection levels. This device may also be used as a general-purpose modulator with a variety of video signal generating devices such as video games, test equipment, video tape recorders, etc.

- Single 5.0 Vdc Supply Operation for NMOS and TTL Compatibility
- Minimal External Components
- Compatible with MC6847 Video Display Generator
- Sound Carrier Addition Capability
- Modulates Channel 3 or 4 Carrier with Encoded Video Signal
- Low Power Dissipation
- Linear Chroma Modulators for High Versatility
- Composite Video Signal Generation Capability
- Ground-Referenced Video Prevents Overmodulation



P SUFFIX
PLASTIC PACKAGE
CASE 646

Pin Connections

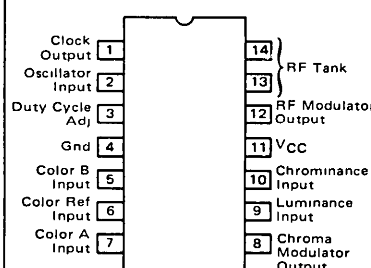
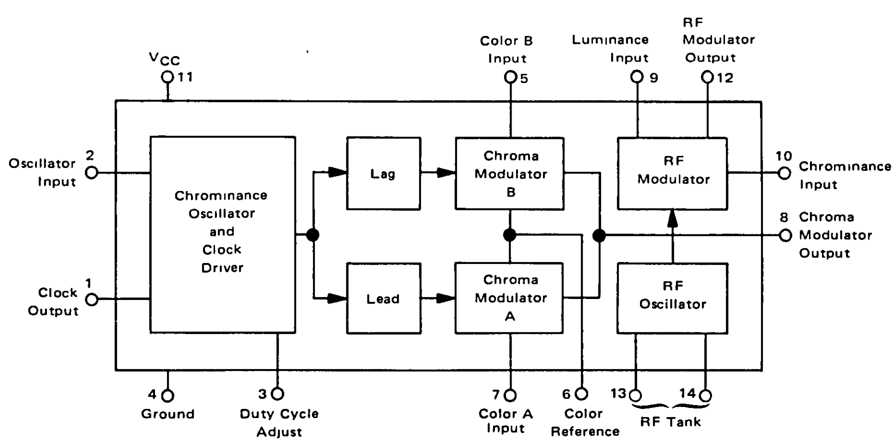


FIGURE 1 – BLOCK DIAGRAM



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Value	Unit
Supply Voltage	8.0	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C
Junction Temperature	150	°C
Power Dissipation, Package Derate above 25°C	1.25 13	Watts mW/°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	5.0	Vdc
Luma Input Voltage — Sync Tip Peak White	1.0 0.35	Vdc
Color Reference Voltage	1.5	Vdc
Color A, B Input Voltage Range	1.0 to 2.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 Vdc, T_A = 25°C, Test Circuit 1 unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Operating Supply Voltage	4.75	5.0	5.25	Volts
Supply Current	—	25	—	mA
CHROMA OSCILLATOR/CLOCK DRIVER (Measured at Pin 1 unless otherwise noted)				
Output Voltage (V_{OL}) (V_{OH})	— 2.4	— —	0.4 —	Vdc
Rise Time (V1 = 0.4 to 2.4 Vdc)	—	—	50	ns
Fall Time (V1 = 2.4 to 0.4 Vdc)	—	—	50	ns
Duty Cycle Adjustment Range (V3 = 5.0 Vdc) (Measured at V1 = 1.4 V)	70	—	30	%
Inherent Duty Cycle (No connection to Pin 3)	—	50	—	%
CHROMA MODULATOR (V5 = V6 = V7 = 1.5 Vdc unless otherwise noted)				
Input Common Mode Voltage Range (Pins 5, 6, 7)	0.8	—	2.3	Vdc
Oscillator Feedthrough (Measured at Pin 8)	—	15	31	mV(p-p)
Modulation Angle [θ8(V7 = 2.0 Vdc) − θ8(V5 = 2.0 Vdc)]	85	100	115	degrees
Conversion Gain [V8/(V7 − V6); V8/(V5 − V6)]	—	0.6	—	V(p-p)/Vdc
Input Current (Pins 5, 6, 7)	—	—	−20	µA
Input Resistance (Pins 5, 6, 7)	100	—	—	kΩ
Input Capacitance (Pins 5, 6, 7)	—	—	5.0	pF
Chroma Modulator Linearity (V5 = 1.0 to 2.0 V; V7 = 1.0 to 2.0 V)	—	4.0	—	%
RF MODULATOR				
Luma Input Dynamic Range (Pin 9, Test Circuit 2)	0	—	1.5	Volts
RF Output Voltage (f = 67.25 MHz, V9 = 1.0 V)	—	15	—	mVrms
Luma Conversion Gain (ΔV12/ΔV9; V9 = 0.1 to 1.0 Vdc) Test Circuit 2	—	0.8	—	V/V
Chroma Conversion Gain (ΔV12/ΔV10; V10 = 1.5 Vp-p, V9 = 1.0 Vdc) Test Circuit 2	—	0.95	—	V/V
Chroma Linearity (Pin 12, V10 = 1.5 Vp-p) Test Circuit 2	—	1.0	—	%
Luma Linearity (Pin 12, V9 = 0 to 1.5 Vdc) Test Circuit 2	—	2.0	—	%
Input Current (Pin 9)	—	—	−20	µA
Input Resistance (Pin 10)	—	800	—	Ω
Input Resistance (Pin 9)	100	—	—	kΩ
Input Capacitance (Pins 9, 10)	—	—	5.0	pF
Residual 920 kHz (Measured at Pin 12) See Note 1	—	50	—	dB
Output Current (Pin 12, V9 = 0 V) Test Circuit 2	—	1.0	—	mA
TEMPERATURE CHARACTERISTICS (V_{CC} = 5 Vdc, T_A = 0 to 70°C, IC only)				
Chroma Oscillator Deviation (f_o = 3.579545 MHz)	—	±50	—	Hz
RF Oscillator Deviation (f_o = 67.25 MHz)	—	±250	—	kHz
Clock Drive Duty Cycle Stability	±5.0	—	—	%

NOTE 1. V9 = 1.0 Vdc, V_C = 300 mV(p-p) @ 3.58 MHz,
V_S = 250 mV(p-p) @ 4.5 MHz, Source Impedance = 75 Ω.

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FIGURE 2 — TEST CIRCUIT 1

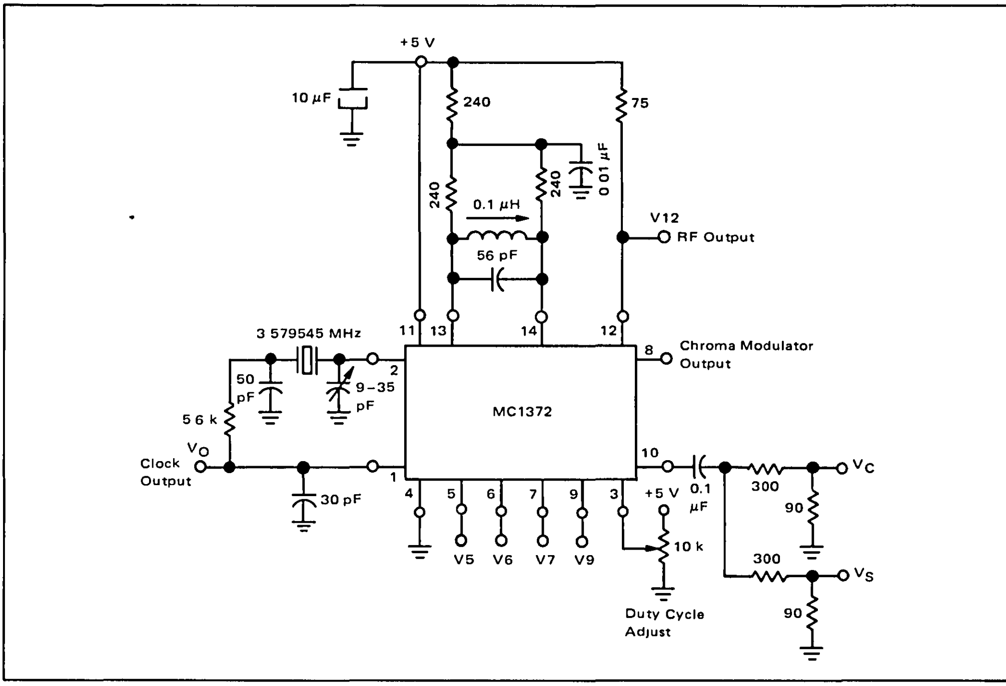

FIGURE 3 — TEST CIRCUIT 2

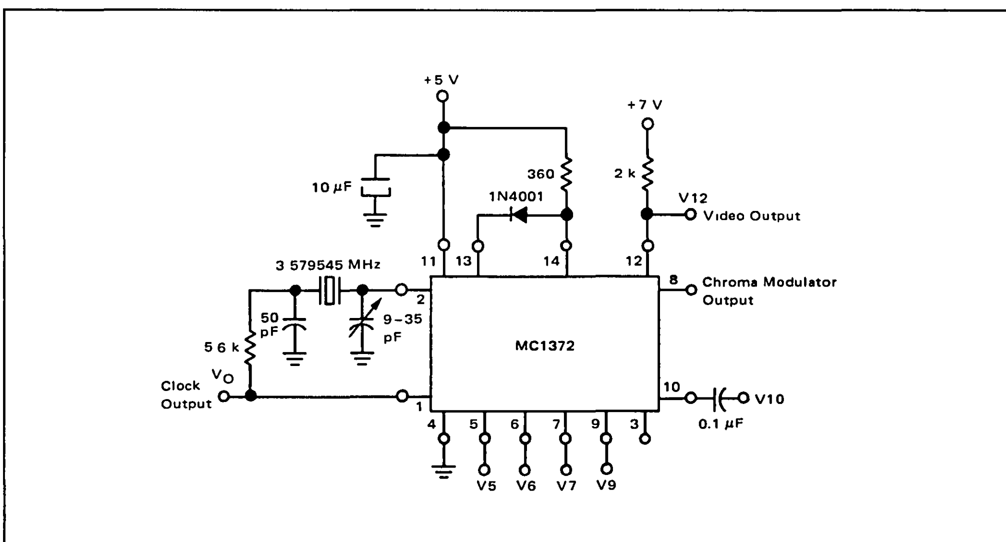

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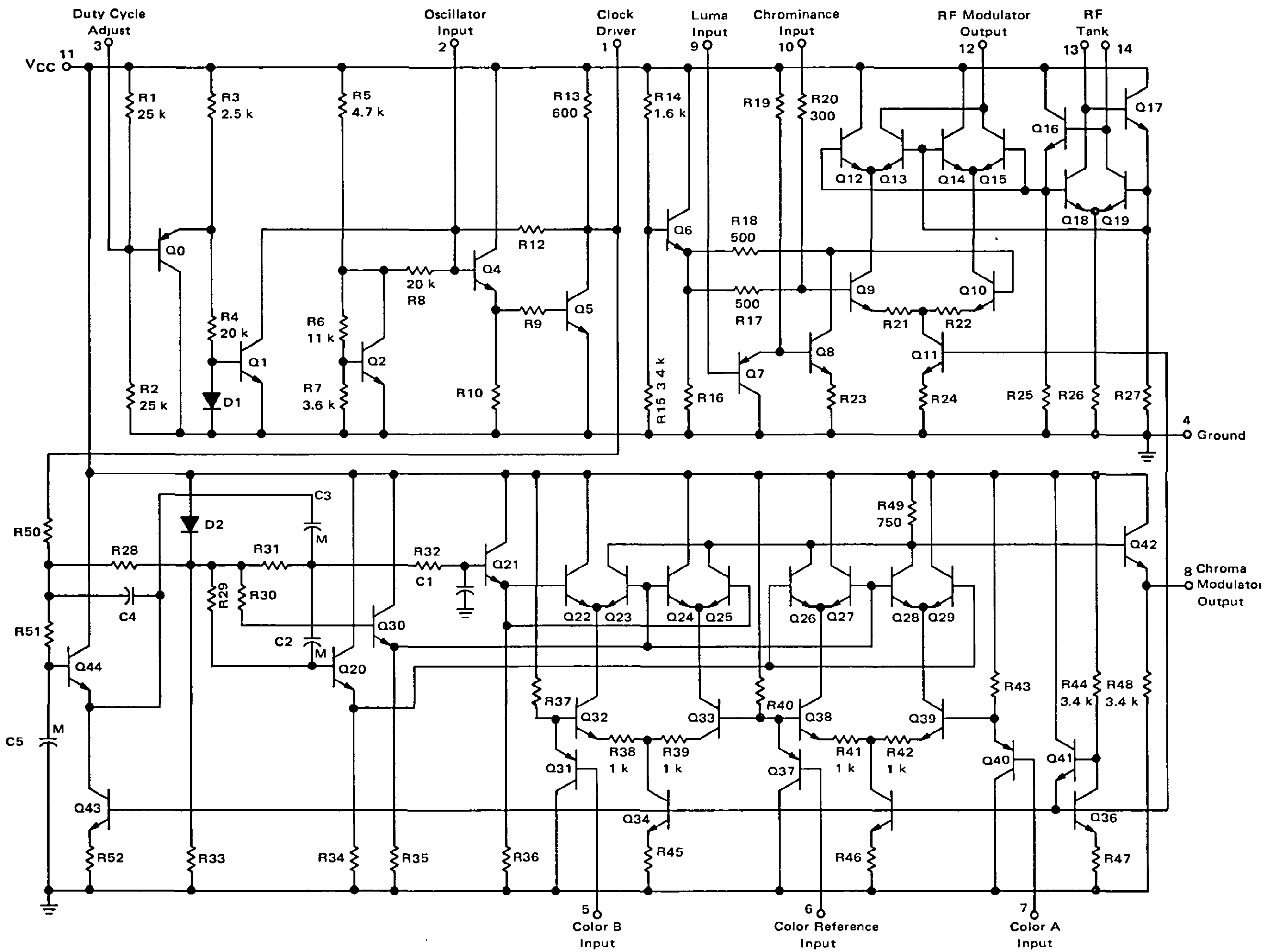
FIGURE 4 — SCHEMATIC DIAGRAM



OPERATIONAL DESCRIPTION

Pin 1 — Clock Output
Provides a rectangular pulse output waveform with frequency equal to the chrominance subcarrier oscillator. This output is capable of driving one LS-TTL load.

Pin 2 — Oscillator Input
Color subcarrier oscillator feedback input. Signal from the clock output is externally phase shifted and ac coupled to this pin.

Pin 3 — Duty Cycle Adjust
A dc voltage applied to this pin adjusts the duty cycle of the clock output signal. If the pin is left unconnected, the duty cycle is approximately 50%.

Pin 4 — Ground

Pin 5 — Color B Input
Dc coupled input to Chroma Modulator B, whose phase leads modulator A by approximately 100°. The modulator output amplitude and polarity correspond to the voltage difference between this pin and the Color Reference Voltage at Pin 6.

Pin 6 — Color Reference Input
The dc voltage applied to this pin establishes the reference voltage to which Color A and Color B inputs are compared.

Pin 7 — Color A Input
Dc coupled input to Chroma Modulator A, whose phase lags modulator B by approximately 100°. The modulator output amplitude and polarity correspond to the voltage difference between this pin and the Color Reference Voltage at Pin 6.

Pin 8 — Chroma Modulator Output
Low impedance (emitter follower) output which provides the vectorial sum of chroma modulators A and B.

Pin 9 — Luminance Input
Input to RF modulator. This pin accepts a dc coupled luminance and sync signal. The amplitude of the RF signal output increases with positive voltage applied to the pin, and ground potential results in zero output (i.e., 100% modulation). A signal with positive-going sync should be used.

Pin 10 — Chrominance Input
Input to the RF modulator. This pin accepts ac coupled chrominance provided by the Chroma Modulator Output (pin 8). The signal is reduced by an internal resistor divider before being applied to the RF modulator. The resistor divider consists of a 300 ohm series resistor and a 500 ohm shunt resistor. Additional gain reduction may be obtained by the addition of external series resistance to pin 10.

Pin 11 — V_{CC}
Positive supply voltage

Pin 12 — RF Modulator Output
Common collector of output modulator stage. Output impedance and stage gain may be selected by choice of resistor connected between this pin and dc supply.

Pins 13 and 14 — RF Tank
A tuned circuit connected between these pins determines the RF oscillator frequency. The tuned circuit must provide a low dc resistance shunt. Applying a dc offset voltage between these pins results in baseband composite video at the RF Modulator Output.

MC1372 CIRCUIT DESCRIPTION

The chrominance oscillator and clock driver consist of emitter follower Q4 and inverting amplifier Q5. Signal presented at clock driver output pin 1 is coupled to oscillator input pin 2 through an external RC and crystal network, which provides 180° phase shift at the resonant frequency. The duty cycle of the output waveform is determined by the dc component at pin 1 internally coupled through R12 to the base of Q4. As pin 1 dc voltage increases, a smaller portion of the sinusoidal feedback signal at pin 2 exceeds the Q4 base voltage of two times V_{BE} required for conduction. As the dc level is reduced, device Q4 and thus Q5 is turned on for a longer percentage of the cycle. Transistors Q0, Q1, Q2 and diode D1 provide the biasing network which determines the dc operating level of the oscillator. The transistor Q2 and resistors R5, R6, and R7 form a voltage reference of four times V_{BE} at the collector of Q2. The dc voltage at pin 1 is determined by the values of R4, R8, and R12 and the applied duty cycle adjust voltage at pin 3. Since these resistors are nominally equal, the voltage at pin 1 will always approximate the dc voltage at pin 3.

The oscillator signal at pin 1 is internally coupled to active filter Q44. This filter reduces the frequency content above 4 MHz. The output of the filter at the emitter of Q44 is ac coupled through C3 to the input of the lead/lag network. R32 and C1 provide approximately 50° of phase lag, while C2 and R29 provide approximately 50° of phase lead. These two quasi-quadrature waveforms are used to switch chroma modulators B and A, respectively. The transistors Q22 through Q25 and Q32–Q33 form a doubly balanced modulator. The input signal applied at pin 5 is compared to the color dc reference voltage applied at pin 6 in differential amplifier Q32–Q33. The source current provided by transistor Q34 is partitioned in transistors Q32 and Q33 according to the differential input signal. The bases of transistors Q23 and Q24 are connected to the dc reference voltage at the emitter of Q30. The bases of transistors Q22 and Q25 are connected to the phase delayed oscillator signal at the emitter of buffer transistor Q21. The differential signal currents provided by Q32 and Q33 are switched in transistors Q22 through Q25 and the resultant signal voltage is developed across R49. This signal has the phase and frequency of the oscillator signal at the emitter of Q21. The amplitude is proportional to the differential input signal applied between pins 5 and 6. Transistors Q26 through Q29 and Q38–Q39 form chroma modulator B. This modulator develops a signal voltage which is proportional to the differential voltage applied between pins 7 and 6. The phase and frequency of the output is equal to the phase advanced chroma oscillator at the emitter of buffer transistor Q20. Both chroma modulators A and B share the same output resistor, R49, so the output signal presented at the emitter of Q42 (pin 8) is the algebraic sum of modulators A and B.

The RF oscillator consists of differential amplifier Q18 and Q19 cross-coupled through emitter followers Q16 and Q17. The oscillator will operate at the parallel resonant frequency of the network connected between pins 13 and 14. The oscillator output is used to switch the doubly balanced RF modulator, Q9 through Q15. Transistors Q7 and Q9 provide level shifting and a high input impedance to the luminance input pin 9. The bases of transistors Q9 and Q10 are both biased through resistors R17 and R18, respectively, to the same dc reference voltage at Q6 emitter. The base voltage at Q10 may only be offset in a negative direction by luminance signal current source Q8. This design insures that overmodulation due to the luminance signal will never occur. The chrominance signal developed at pin 8 is externally ac coupled to pin 10 where it is reduced by resistor dividers R20 and R17, and added to the luminance signal in Q9. The resultant differential composite video currents are switched at the appropriate RF frequency in Q12 through Q15. The output signal current is presented at pin 12.

Transistors Q36, Q41 and resistors R44, R47 provide a highly stable voltage reference for biasing current sources Q43, Q34, Q35, and Q11.

MC1372 APPLICATION INFORMATION

Chrominance Oscillator

The oscillator is used as a clock signal for driving associated external circuitry, in addition to providing a switching signal for the chroma modulators. The IC uses an external crystal in a Colpitts configuration, as shown in Figure 5. Resistor R1 provides current limiting to reduce the signal swing. Capacitor C2 is adjusted for the exact frequency desired (3.579545 MHz).

In some applications, the duty cycle of the clock signal at pin 1 must be modified to overcome gate delays in associated equipment. The duty cycle may be adjusted by varying the dc voltage applied to pin 3. This adjustment may be made with the use of a potentiometer (10 kΩ) between supply and ground. With no connection to pin 3, the duty cycle is approximately 50%.

Chroma Modulator

The chrominance oscillator is internally phase shifted and applied to chroma modulators A and B. No external lead/lag networks are necessary. The phase relationship between the modulators is approximately 100°, which was chosen to provide the best rendition of colors using equal amplitude color-difference signals. The voltage applied to pin 5, 6, or 7 must always be within the Input Common Mode Voltage Range. Since the amplitude of chrominance output is proportional to the voltage difference between pins 5 and 6 or 7 and 6, it is desirable to select the Color Reference Voltage applied to pin 6 to be midway between $V5_{max}$ and $V5_{min}$ (which should be $V7_{max}$ and $V7_{min}$). The Chroma B Modulator will be defined as a (B-Y) modulator if a burst flag signal is applied to the Color B Input (pin 5) at the appropriate time. This voltage should be negative with respect to the Color Reference Voltage, and typically has an amplitude equal to $1/2[V6-V5_{min}]$. Since the phase of burst is always defined as −(B-Y), the Chroma A Modulator approximates an (R-Y) modulator; however, the phase is offset by 10° from the nominal 90°, to provide the 100° phase shift as discussed previously.

RF Modulator and Oscillator

The coil and capacitor connected between pins 13 and 14 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 μH shown in Figure 5 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz (C = 75 pF, L = 0.1 μH). Resistors R4 and R5 are chosen to provide an adequate amplitude of switching voltage, whereas R6 is used to lower the maximum dc level of switching voltage below V_{CC}, thus preventing saturation within the IC.

Composite Luminance and Sync should be dc coupled to Luminance Input, pin 9. This signal must be within the Luma Input Dynamic Range to insure linearity. Since an increase in dc voltage applied to pin 9 results in an increase in RF output, the input signal should have positive-going sync to generate an NTSC compatible signal. As long as the input signal is positive, overmodulation is prevented by the integrated circuit.

Chrominance information should be ac coupled to Chrominance Input, pin 10. This pin is internally connected to a resistor divider consisting of a series 300 ohms and a shunt 500 ohms resistor. The input impedance is thus 800 ohms, and a coupling capacitor should be appropriately chosen.

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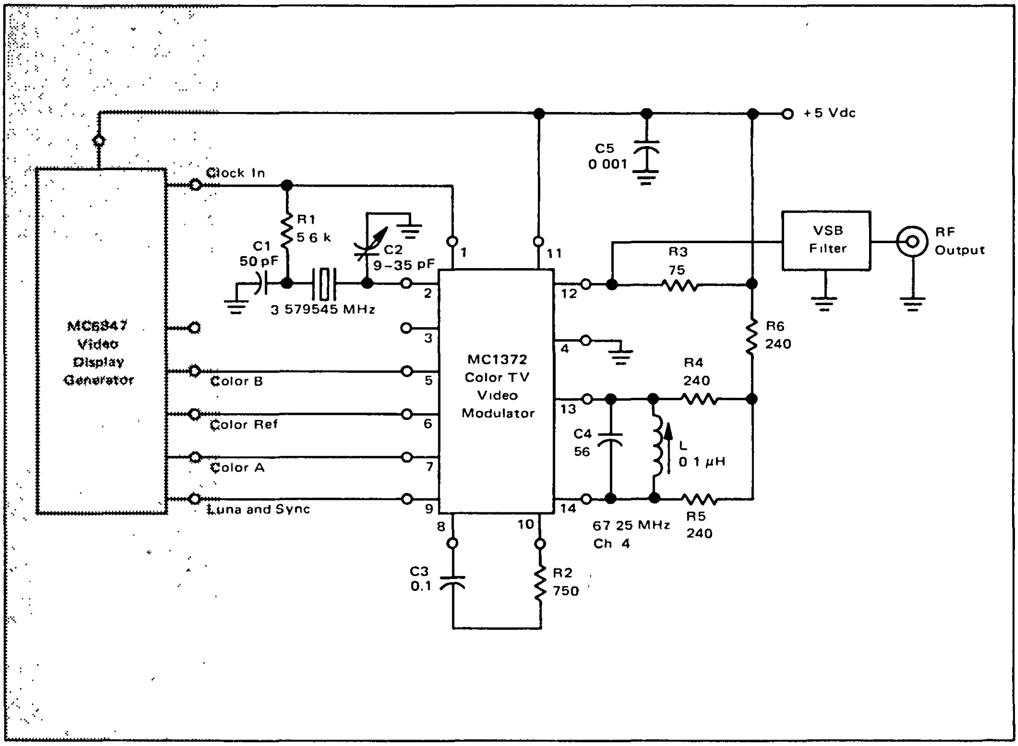
FIGURE 5 – TYPICAL APPLICATION CIRCUIT



The Luminance to Chrominance ratio (L:C) may be modified with the addition of an external resistor in series with pin 10 (as shown in Figure 5). The unmodified L:C (A_O) is determined by the ratio of the respective Conversion Gain for equal amplitude signals (typically, 0.883 = −1.6 dB). The modified L:C will be governed by the equation $A_O(1 + R_{ext}/800)$ for equal amplitude input signals.

The internal chrominance modulators are not internally connected to the RF modulator; therefore, the user has the option of connecting an externally generated chrominance signal to the RF modulator. In addition, the RF modulator is wideband, and a 4.5 MHz FM audio signal may be added to the chrominance input at pin 10. This may be accomplished by selecting an appropriate series input resistor to provide the correct Luminance:Sound ratio.

The modulated RF signal is presented as a current at RF Modulator Output, pin 12. Since this pin represents a current source, any load impedance may be selected for matching purposes and gain selection, as long as the voltage at pin 12 is high enough to prevent the output devices from reaching saturation (approximately 4.5 V with components in Figure 5). The peak current out of pin 12 is typically 2 mA. Hence, a load resistance of up to 250 ohms may be safely used with a 5 V supply.

Composite Video Signal Generation

The RF modualtor may be easily used as a composite video generator by replacing the RF oscillator tank circuit with a diode as shown in Figure 3. This results in the output modulator being biased so the summation of luminance and chrominance appears unswitched at pin 12. The polarity of the output waveform is controlled by the direction of the diode. *Inverted video:* Anode to pin 14, cathode to pin 13. *Non-inverted video:* Anode to pin 13, cathode to pin 14. Note that the supply resistor must always be connected to the anode of the diode.

The amplitude of signal may be increased by increasing the load resistor on pin 12 and returning it to a higher supply voltage. Any voltage up to the Absolute Maximum Rating may be used.

Applications with MC6847 Video Display Generator

The MC1372 may be easily interfaced to the MC6847 as shown in Figure 5. The dc levels generated and required by the VDG are compatible with the MC1372, so that pins 1, 5, 6, 7, and 9 may be directly coupled to the appropriate MC6847 pins. Both integrated circuits as well as any associated NMOS MPU may be driven from a common 5 Vdc supply.

Recommended Chroma-Luma Signals

A chroma modulation angle of 100° was chosen to facilitate a desirable selection of colors with a minimum number of input signal levels. The following table demonstrates applicable signal levels for a variety of colors.

RECOMMENDED CHROMA-LUMA SIGNALS

	Pin #9 Luminance Input (Vdc)	Pin #7 Color A (Vdc)	Pin #6 Color Ref. (Vdc)	Pin #5 Color B (Vdc)
Sync	1.0	1.5	1.5	1.5
Blanking	0.75	1.5	1.5	1.5
Burst	0.75	1.5	1.5	1.25
Black	0.70	1.5	1.5	1.5
Green	0.50	1.0	1.5	1.0
Yellow	0.38	1.5	1.5	1.0
Blue	0.62	1.5	1.5	2.0
Red	0.62	2.0	1.5	1.5
Cyan	0.50	1.0	1.5	1.5
Magenta	0.50	2.0	1.5	2.0
Orange	0.50	2.0	1.5	1.0
Buff	0.38	1.5	1.5	1.5

MC1373

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Advance Information

TV VIDEO MODULATOR

. . . an RF oscillator and dual-input modulator to generate a TV signal from baseband video inputs.

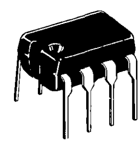
Applications include video games, home computer display, video tape recorders, and test equipment.

The very low level of intermodulation products, compact package and small external component count make this device superior to simple discrete circuits.

- Single 5.0 Vdc Supply
- Channel 3 or 4 Operation
- Excellent Oscillator Stability to 100 MHz
- Color and Sound Compatibility
- Dual Input Modulator for Ease of Signal
- Low Intermodulation (−50 dB 920 kHz Beat)
- Overmodulation Protection

TV VIDEO MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



CASE 626
P SUFFIX

PIN CONNECTIONS

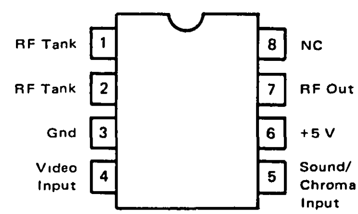
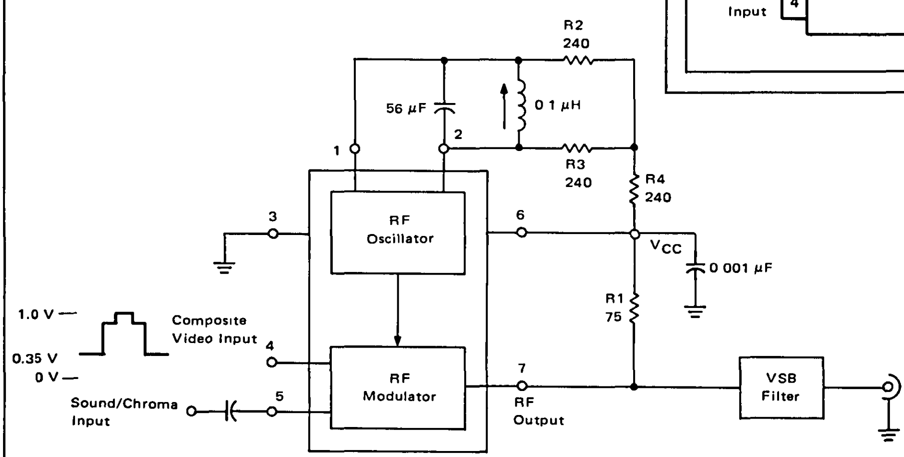


FIGURE 1 — BLOCK DIAGRAM AND APPLICATION CIRCUIT



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Value	Unit
Supply Voltage	8.0	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C
Junction Temperature	150	°C
Power Dissipation, Package Derate above 25°C	1.25 13	Watts mW/°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	5.0	Vdc
Luma Input Voltage — Sync Tip Peak White	1.0 0.35	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 Vdc, T_A = 25°C, Test Circuit 1 unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Operating Supply Voltage	4.75	5.0	5.25	Volts
Supply Current	—	12	—	mA
RF MODULATOR				
Luma Input Dynamic Range (Pin 4, Test Circuit 2)	0	—	1.5	Volts
RF Output Voltage (f = 67.25 MHz, V4 = 1.0 V)	—	15	—	mVrms
Luma Conversion Gain (ΔV7/ΔV4, V4 = 0.1 to 1.0 Vdc) Test Circuit 2	—	0.8	—	V/V
Chroma Conversion Gain (ΔV7/ΔV5; V5 = 1.5 Vp-p; V4 = 1.0 Vdc) Test Circuit 2	—	0.95	—	V/V
Chroma Linearity (Pin 7, V5 = 1.5 Vp-p) Test Circuit 2	—	1.0	—	%
Luma Linearity (Pin 7, V4 = 0 to 1.5 Vdc) Test Circuit 2	—	2.0	—	%
Input Current (Pin 4)	—	—	−20	μA
Input Resistance (Pin 5)	—	800	—	Ω
Input Resistance (Pin 4)	100	—	—	kΩ
Input Capacitance (Pins 4, 5)	—	—	5.0	pF
Residual 920 kHz (Measured at Pin 7) See Note 1	—	60	—	dB
Output Current (Pin 7, V4 = 0 V) Test Circuit 2	—	1.5	—	mA
TEMPERATURE CHARACTERISTICS (V_{CC} = 5 Vdc, T_A = 0 to 70°C, IC only)				
RF Oscillator Deviation (f_o = 67.25 MHz)	—	±250	—	kHz

NOTE 1. RF Reference Level = 6.0 mV @ Pin 7 Load Impedance = 75 Ω.
RF + 4.5 MHz = −13 dB.
RF + 3.58 MHz = −20 dB.

FIGURE 2 — TEST CIRCUIT 1

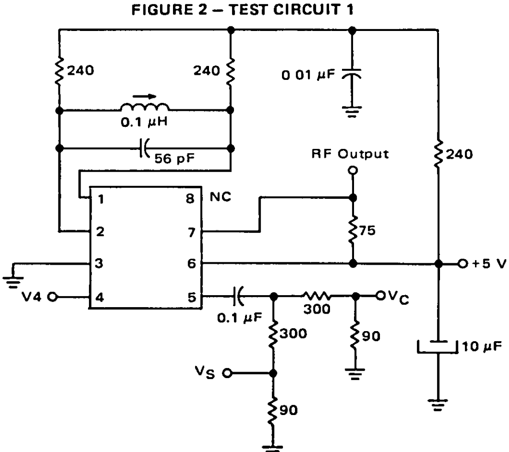


FIGURE 3 — TEST CIRCUIT 2

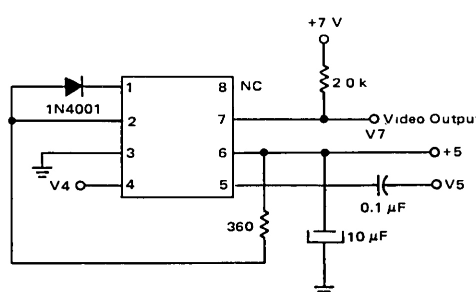


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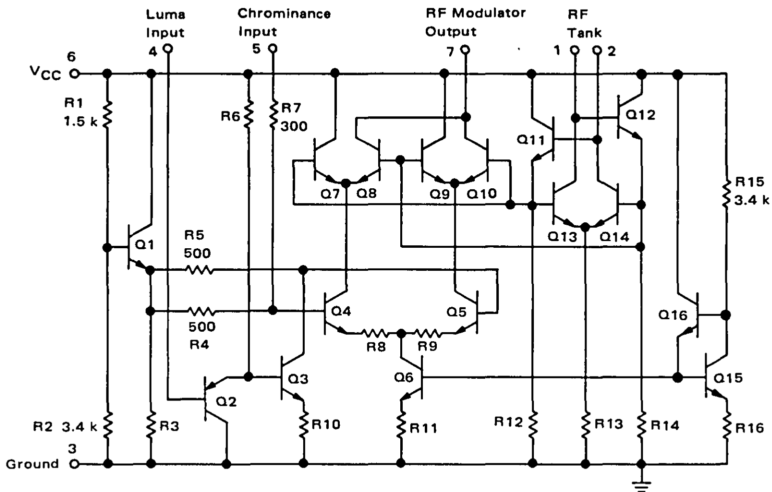
FIGURE 4 – SCHEMATIC DIAGRAM



SCHEMATIC DESCRIPTION

The RF oscillator consists of differential amplifier Q13 and Q14 cross-coupled through emitter followers Q11 and Q12. The oscillator will operate at the parallel resonant frequency of the network connected between pins 1 and 2. The oscillator output is used to switch the doubly balanced RF modulator, Q4 through Q10. Transistors Q2 and Q3 provide level shifting and a high input impedance to the luminance input pin 4. The bases of transistors Q4 and Q5 are both biased through resistors R4 and R5, respectively, to the same dc reference voltage at Q1 emitter. The base voltage at Q5 may only be offset in a negative direction by luminance signal current source Q3. This design insures that overmodulation due to the luminance signal will never occur. The chrominance signal is externally ac coupled to pin 5 where it is reduced by resistor dividers R7 and R4, and added to the luminance signal in Q4. The resultant differential composite video currents are switched at the appropriate RF frequency in Q7 through Q10. The output signal current is presented at pin 7.

Transistors Q15, Q16 and resistors R15, R16 provide a highly stable voltage reference for biasing the current source Q6.

OPERATIONAL DESCRIPTION

Pins 1 and 2 – RF Tank. A tuned circuit connected between these pins determines the RF oscillator frequency. The tuned circuit must provide a low dc resistance shunt. Applying a dc offset voltage between these pins results in baseband composite video at the RF Modulator Output.

Pin 3 – Ground.

Pin 4 – Luminance Input. Input to RF modulator. This pin accepts a dc coupled luminance and sync signal. The amplitude of the RF signal output increases with positive voltage applied to the pin, and ground potential results in zero output (i.e., 100% modulation). A signal with positive-going sync should be used.

Pin 5 – Chrominance/Sound Input. Input to the RF modulator. This pin accepts an ac coupled chrominance signal. The signal is reduced by an internal resistor divider before being applied to the RF modulator. The resistor divider consists of a 300 ohm series resistor and a 500 ohm shunt resistor. A 4.5 MHz FM audio signal may be added to the input by selecting an appropriate series input resistor to provide the correct Luminance:Sound ratio.

Pin 6 – V_{CC}. Positive supply voltage.

Pin 7 – RF Modulator Output. Common collector of output modulator stage. Output impedance and stage gain may be selected by choice of resistor connected between this pin and dc supply.

Pin 8 – No Connection.

APPLICATIONS INFORMATION (Refer to Figure 1)

RF Modulator and Oscillator

The coil and capacitor connected between pins 1 and 2 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 μH shown in Figure 1 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz (C = 75 pF, L = 0.1 μH). Resistors R2 and R3 are chosen to provide an adequate amplitude of switching voltage, whereas R4 is used to lower the maximum dc level of switching voltage below V_{CC}, thus preventing saturation within the IC.

Composite Luminance and Sync should be dc coupled to Luminance Input, pin 4. This signal must be within the Luma Input Dynamic Range to insure linearity. Since an increase in dc voltage applied to pin 4 results in an increase in RF output, the input signal should have positive-going sync to generate an NTSC compatible signal. As long as the input signal is positive, overmodulation is prevented by the integrated circuit.

Chrominance information should be ac coupled to Chrominance Input, pin 5. This pin is internally connected to a resistor divider consisting of a series 300 ohms and a shunt 500 ohms resistor. The input impedance is thus 800 ohms, and a coupling capacitor should be appropriately chosen.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1391P	0°C to +75°C	Plastic DIP
MC1394P	0°C to +75°C	Plastic DIP

MC1391P
MC1394P

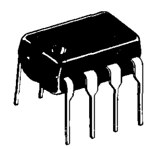
TV HORIZONTAL PROCESSOR

. . . low-level horizontal sections including phase detector, oscillator and pre-driver — a device designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ±300 Hz Typical Pull-In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable dc Loop Gain
- MC1391P — Positive Flyback Inputs
- MC1394P — Negative Flyback Inputs

TV HORIZONTAL PROCESSOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

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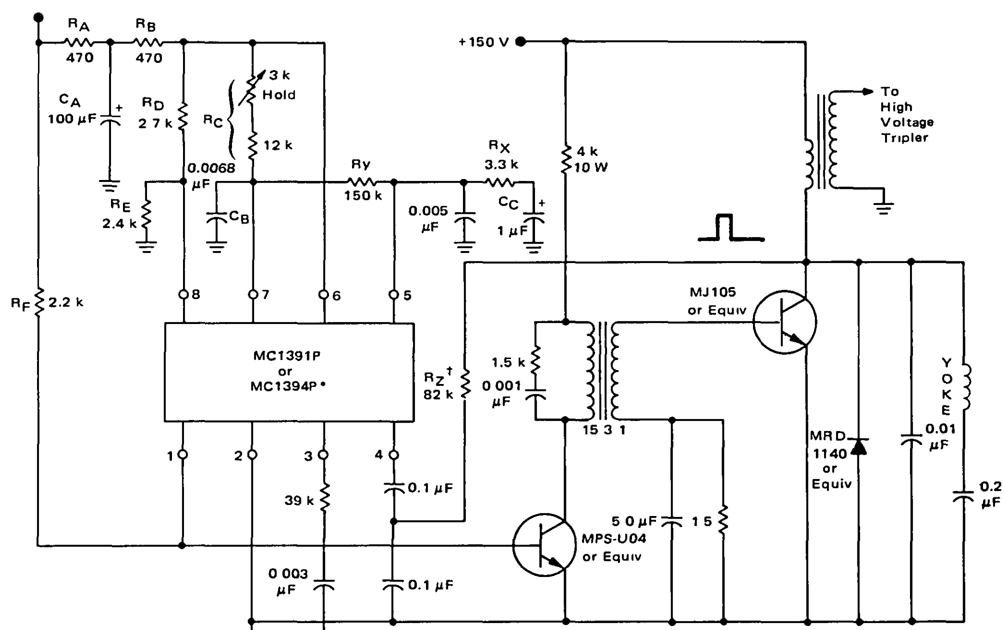
FIGURE 1 — TYPICAL APPLICATION CIRCUIT



*MC1394P designed to accept reverse polarity sawtooth at Pin 4 if sync pulse not derived from MJ105 collector.

†R_Z = 6 8 k per 100 V of flyback amplitude

This circuit has an oscillator pull-in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Supply Current	40	mAdc
Output Voltage	40	Vdc
Output Current	30	mAdc
Sync Input Voltage (Pin 3)	5.0	$V_{(p-p)}$
Flyback Input Voltage (Pin 4)	5.0	$V_{(p-p)}$
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	−65 to +150	°C

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ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.) (See Test Circuit of Figure 2, all switches in position 1.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (Pin 6)	8.0	8.6	9.0	Vdc
Supply Current (Pin 6)	–	20	–	mAdc
Collector-Emitter Saturation Voltage (Output Transistor Q1 in Figure 6) (I_C = 20 mA, Pin 1) Vdc	–	0.15	0.25	Vdc
Voltage (Pin 4)	–	2.0	–	Vdc
Oscillator Pull-in Range (Adjust R_H in Figure 2)	–	±300	–	Hz
Oscillator Hold-in Range (Adjust R_H in Figure 2)	–	±900	–	Hz
Static Phase Error (Δf = 300 Hz)	–	0 5	–	μs
Free-running Frequency Supply Dependance (S1 in position 2)	–	±3.0	–	Hz/Vdc
Phase Detector Leakage (Pin 5) (All switches in position 2)	–	–	±1.0	μA
Sync Input Voltage (Pin 3)	2.0	–	5.0	V(p-p)
Sawtooth Input Voltage (Pin 4)	1.0	–	3.0	V(p-p)

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 2 – TEST CIRCUIT

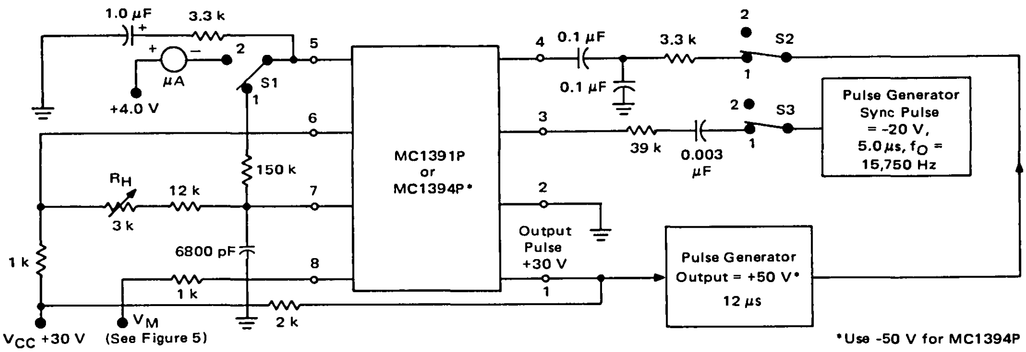


FIGURE 3 – FREQUENCY versus TEMPERATURE

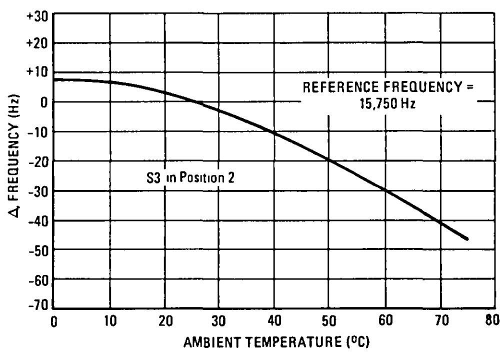


FIGURE 4 – FREQUENCY DRIFT versus WARM-UP TIME

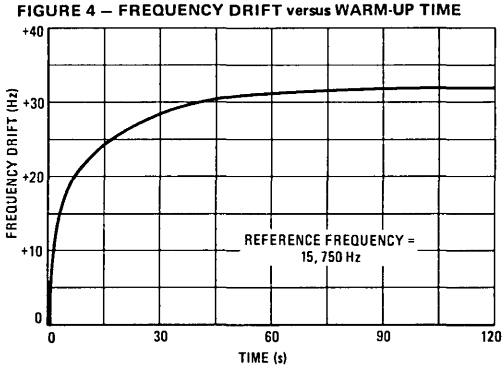


FIGURE 5 – MARK-SPACE RATIO

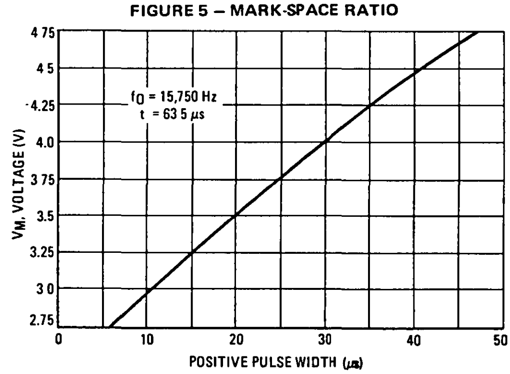
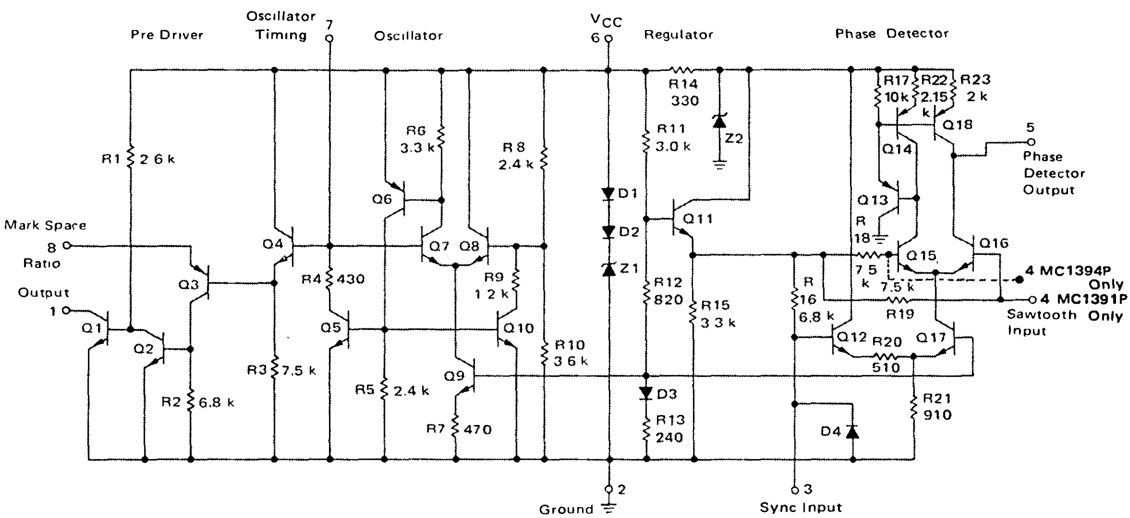


FIGURE 6 – CIRCUIT SCHEMATIC



CIRCUIT OPERATION

The MC1391P and MC1394P contain the oscillator, phase detector and predriver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor (R_C) connected to Pin 6 As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 and Q10. Transistor Q10 will set a new, lower potential at the base of Q8 determined by R8, R9 and R10. Then, transistor Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate either tube or transistor horizontal output stages

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each for half the sync pulse period The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5 This pin is connected via an external low-pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1

APPLICATION INFORMATION

Although it is an integrated circuit, the MC1391P and MC1394P have all the flexibility of a conventional discrete component horizontal APC loop.

The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2mA for the external dividers

$$R_A + R_B = \frac{V_{nonreg(min)} - 8.8}{20 \times 10^{-3}}$$

Components R_A, R_B and C_A are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 Volt supply) then R_A and R_B can be combined and C_A omitted.

The output pulse width can be varied from 6 μs to 48 μs by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible to prevent ringing which can result in erroneous output pulses at Pin 1. The parallel impedance of R_D and R_E should be close to 1 kΩ to ensure stable pulse widths.

For 15 mA drive at saturation

$$R_F = \frac{V_{nonreg} - 0.3}{15 \times 10^{-3}}$$

The oscillator free-running frequency is set by R_C and C_B connected to Pin 7. For values of $R_C \gg R_{discharge}$ (R4 in Figure 6), a useful approximation for the free-running frequency is

$$f_O = \frac{1}{0.6 R_C C_B}$$

Proper choice of R_C and C_B will give a wide range of oscillator frequencies — operation at 31.5 kHz for count-down circuits is possible for example. As long as the product $R_C C_B \approx 10^{-4}$ many combinations of values of R_C and C_B will satisfy the free-running frequency requirement of 15 734 kHz However, the sensitivity of the oscillator (β) to control-current from the phase detector is directly dependent on the magnitude of R_C, and this provides a convenient method of adjusting the dc loop gain (fc).

For a given phase detector sensitivity (μ) = 1.60×10^{-4} A/rad

$$fc = \mu\beta \text{ and } \beta = 3.15 \times R_C \text{ Hz/mA}$$

Increasing R_C will raise the dc loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop (ω_n) and give a wider pull-in range from an out-of-lock condition. The loop will also tend to be underdamped with fast pull-in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the dc loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the dc loop gain has been selected for adequate S.P.E. performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor R_X with respect to R_Y which modifies the ac/dc gain ratio (m) of the loop. Lowering this ratio will reduce the pull-in range and noise bandwidth (fnn). (Note. very large values of R_Y will limit the control capability of the phase detector with a corresponding reduction in hold-in range).

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT

NOTE.

In adjusting the loop parameters, the following equations may prove useful.

$$f_{nn} = \frac{1 + \chi^2 T\omega_c}{4 \chi T} \qquad \chi = \frac{R_X}{R_Y}$$

$$\omega_n = \sqrt{\frac{\omega_c}{(1 + \chi) T}} \qquad \omega_c = 2\pi fc \qquad T = R_Y C_C$$

$$K = \frac{\chi^2 T\omega_c}{4}$$

where:

K = loop damping coefficient

5

MC1393A

5

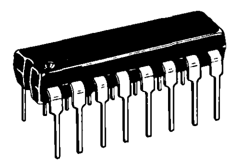
TV VERTICAL PROCESSOR

. . . designed for universal use in black and white as well as large-screen color television receivers.

- Injection Locked Oscillator
- Greater Than 12 Hz Injection
- Low Thermal Drift
- Eliminates Centering Control
- Independent Vertical Hold and Size Controls
- Scan Current Independent of Yoke Variations
- Retrace Pulse for Effective Blanking
- Linear Sawtooth Amplification

TV VERTICAL PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

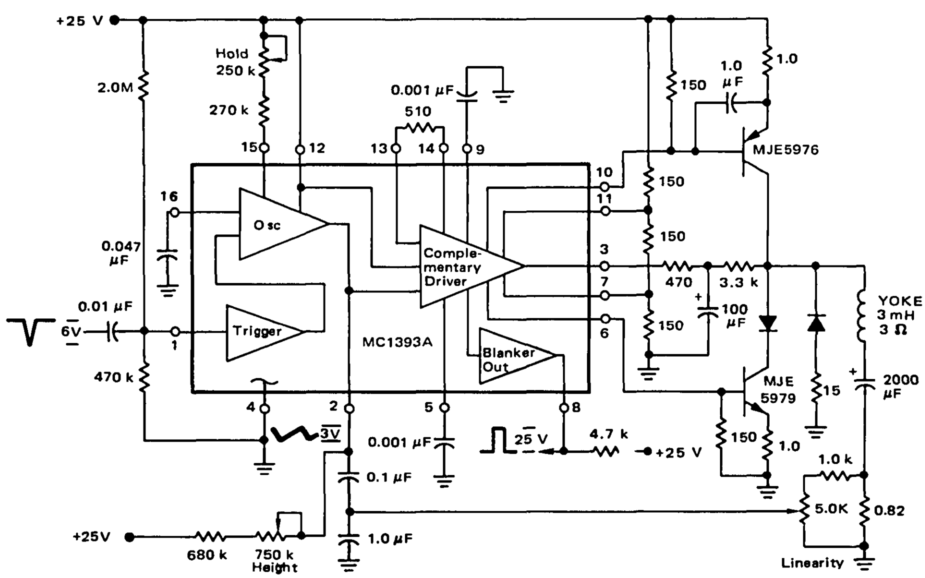


PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

Device	Temperature Range	Package
MC1393A	0 to +70°C	Plastic DIP

FIGURE 1 — TYPICAL APPLICATION CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Junction Temperature	150	°C
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +25 V, T_A = +25°C) (Figure 1)

Characteristic	Typ	Unit
Supply Drain(1)	525	mAdc
Oscillator Frequency (Pin 16)	60	Hz
Oscillator Supply Sensitivity	0.3	Hz/V
Oscillator Drift	130	PPM/°C
Oscillator Injection (Pull-In)	12	Hz
Driver Input Sawtooth Amplitude (Pin 2)	3.0	$V_{(p-p)}$
Output Current (Yoke)	3.0	$A_{(p-p)}$
Scan Non-Linearity	8.0	%

Note 1: Total Current Includes Current in Circuit External to the IC.

5

CIRCUIT DESCRIPTION

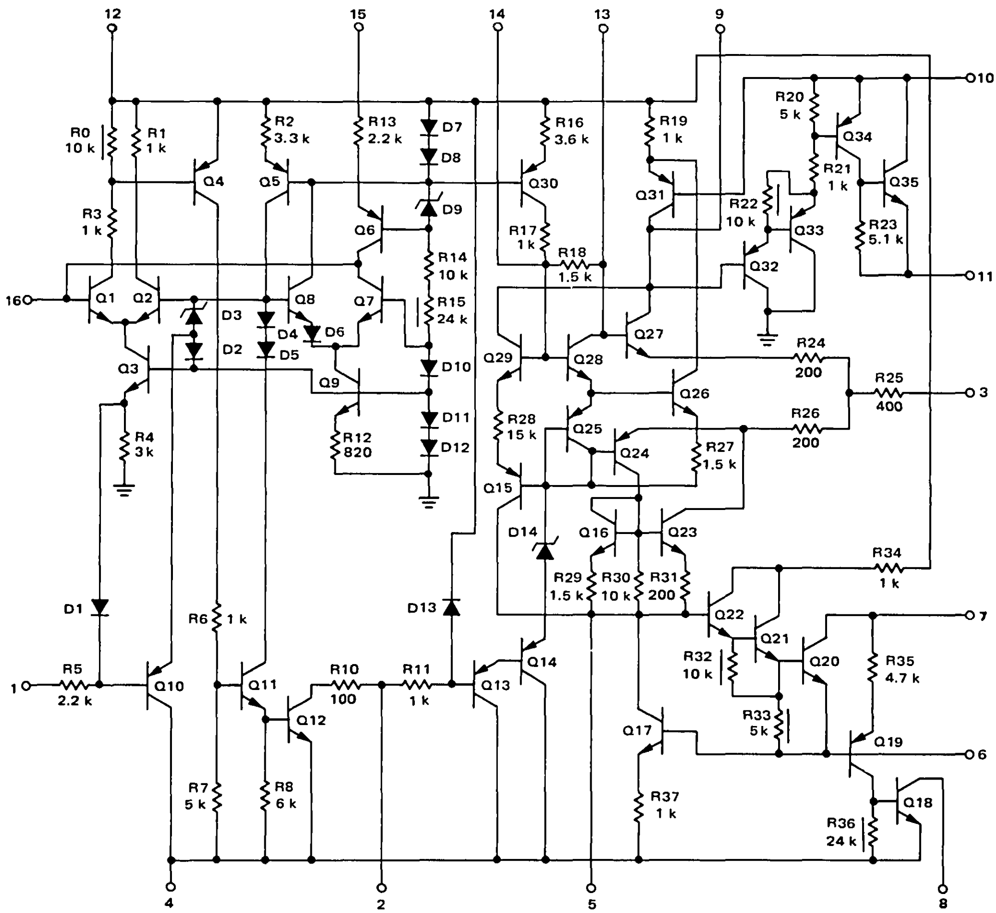
Oscillator

The oscillator employs two differential amplifiers (Q1, Q2, and Q7, Q8). A capacitor at Pin 16 is charged by a current source Q6 until it reaches a voltage that turns on Q1. Q7 is turned on by Q1 providing a discharge path for the voltage stored at Pin 16. Q12 is on during the same period as Q1, and provides a discharge path for a ramp generated at Pin 2. Q1 stays on until the capacitor voltage is discharged to a level that turns Q7 off. A negative sync pulse at Pin 1 turns Q10 on and increases the oscillator frequency by lowering the Q1 switching voltage.

Complementary Driver

A sawtooth generated at Pin 2 is level shifted to the driver inputs Q24 and Q27. Q17 and an NPN output transistor at Pin 6 are a current driver function for one-half of the output. Q20 acts as a current amplifier providing base current for the NPN output transistor. The current gain between Q20 and the output transistor is inversely proportional to the resistance ratio of R37 and the output emitter resistor. 1.0 mA of current through R37 will produce 1.0 A through a 1.0 ohm output-emitter resistor, thus providing a gain of 1000. Q20, Q31 and a PNP output transistor at Pin 10 are a second current driver function, making up the other half of the complementary output. Q35 provides base current for the output. The maximum amount of base current drive is determined by the current in the voltage divider on Pins 7 and 11. Pin 3 is a return path for the dc and provides for automatic centering. Pin 8 is the collector output of Q18 providing a positive blanking pulse.

FIGURE 2 – CIRCUIT SCHEMATIC



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ORDERING INFORMATION

Device	Temperature Range	Package
MC1398P	−20°C to +75°C	Plastic DIP

MC1398

TV COLOR PROCESSING CIRCUIT

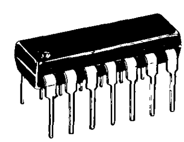
. . . a chroma IF amplifier with automatic chroma control, color killer, dc chroma control, and injection lock reference system followed by dc hue control.

MC1398P is a monolithic device designed for use in solid-state color television receivers.

- Minimum Number of External Components
- DC Control of Both Chroma Amplitude and Hue Shift
- Crystal-Controlled Internal Feedback Oscillator
- Built-in Noise Immunity
- Schmitt Trigger Color Killer
- Automatic Chroma Control
- Internal Burst Gate and Gate Pulse Shaping Circuit
- High Oscillator Lock-in Sensitivity
- Built-in Supply Regulation

TV COLOR PROCESSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

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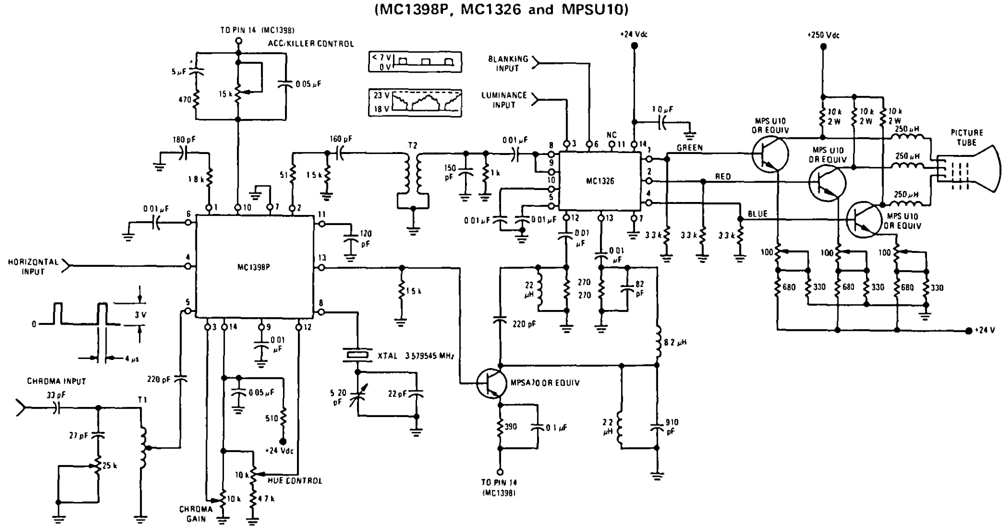
FIGURE 1 – TYPICAL CHROMA APPLICATIONS CIRCUIT
(MC1398P, MC1326 and MPSU10)



T1 T2 See Figure 10 for coil data

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Current	35	mAdc
Horizontal Pulse Input Current	250	µA Peak
Power Dissipation (package limitation) Derate above T_A = +25°C	625 5 0	mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, R_S = 390 ohms, T_A = +25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (I_S = 35 mA) (I_S = 27 mA)	9.0 –	9 6 9.2	11 5 –	Vdc
Maximum Undistorted Chroma Output, See Note 1, $E_{(pin\ 3)} = E_{(pin\ 14)}$	0 8	1.75	–	V(p-p)
Maximum Chroma Gain $E_{(pin\ 3)} = E_{(pin\ 14)}$, See Note 1	34	40	–	dB
Automatic Chroma Control Range (ACC) -3 0 dB down from maximum undistorted output ,see Note 1	–	19	–	dB
Chroma Burst Level to Kill, See Note 1	–	1 4	–	mV(p-p)
Manual Chroma Gain Control Range ($\Delta V_{(pin\ 3)}$ ($V_{(pin\ 14)}$ to 0 Vdc)	50	60	–	dB
Chroma Input Resistance	–	2.3	–	k ohms
Chroma Input Capacitance	–	13	–	pF
Chroma Output Impedance	–	15	–	ohms
Horizontal Input Pulse	2.2	3.0	4 0	Vp
Oscillator Output	100	–	–	mV(RMS)
Oscillator Output Impedance	–	15	–	ohms
Hue Control Range ($\Delta V_{(pin\ 12)}$ ($V_{(pin\ 14)}$ to 4.3 Vdc)	100	126	–	degrees
Oscillator Pull-In Range	1200	–	–	Hz
Oscillator Noise Bandwidth (f_N)	–	900	–	Hz
Static Phase Error with Oscillator Detuning 25 mV(p-p) Burst Amplitude 2.0 mV(p-p) Burst Amplitude	 – –	 0.20 0.25	 – –	degrees/Hz

Note 1: With 5.0 mV(p-p) burst input at pin 5 set $E_{(pin\ 10)}$ to just "unkill"

FIGURE 2 – MC1398P TEST CIRCUIT

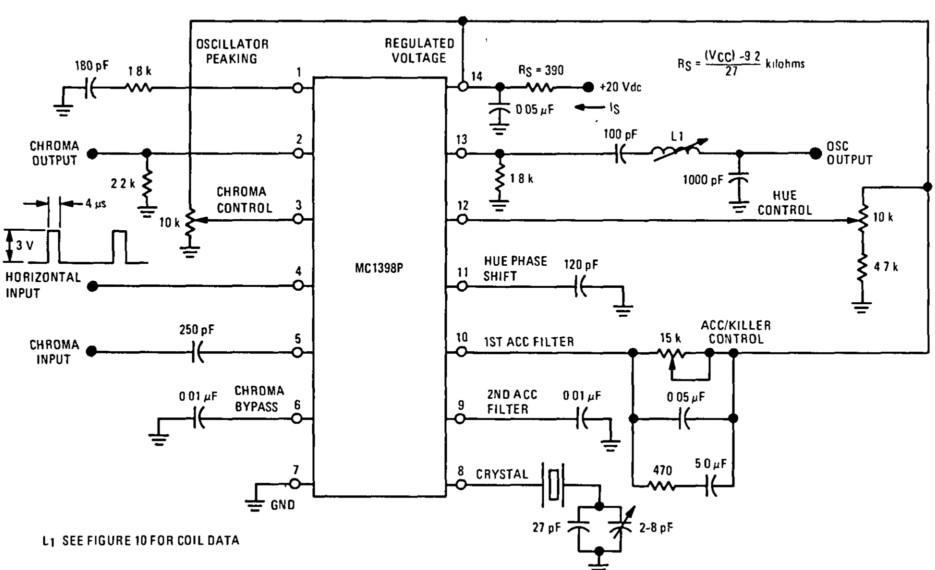
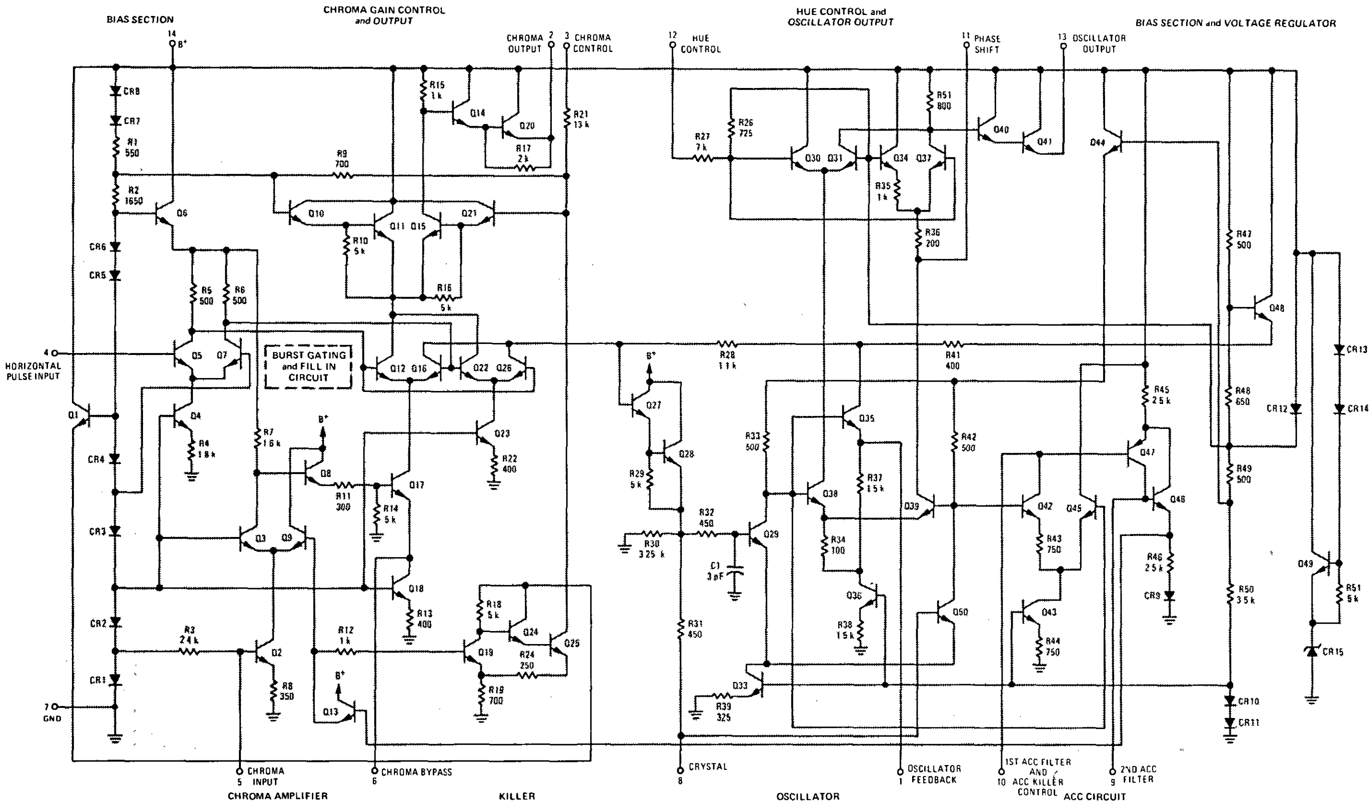


FIGURE 3 – MC1398 CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

(Figures 4 through 9, See Test Circuit of Figure 2.)

FIGURE 4 – INPUT/OUTPUT CHARACTERISTICS

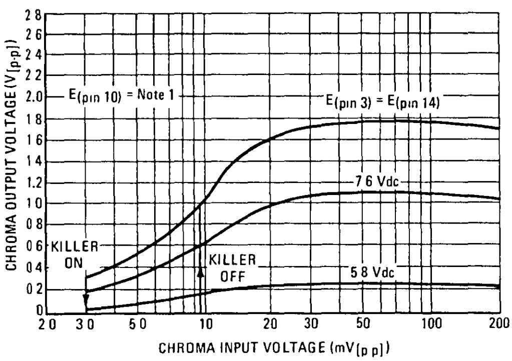


FIGURE 5 – REGULATED VOLTAGE

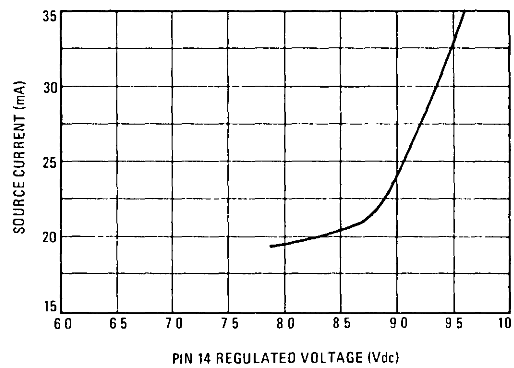


FIGURE 6 – HUE CONTROL OPERATION

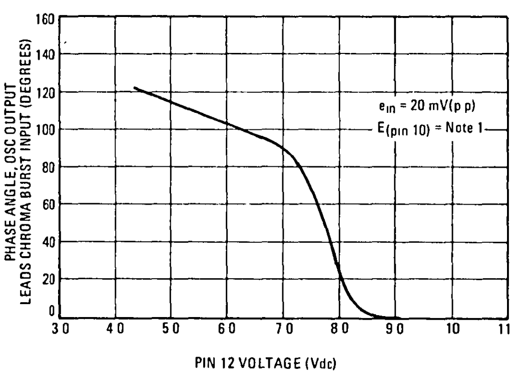


FIGURE 7 – OSCILLATOR OUTPUT versus PIN 12 VOLTAGE

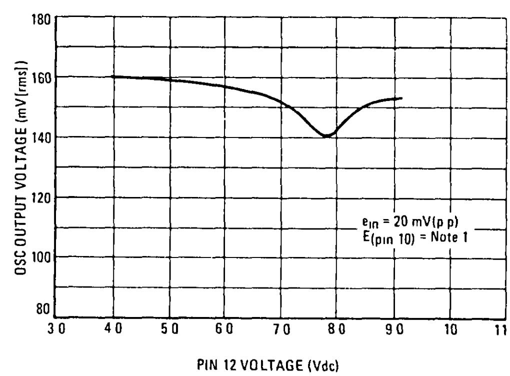


FIGURE 8 – STATIC PHASE ERROR

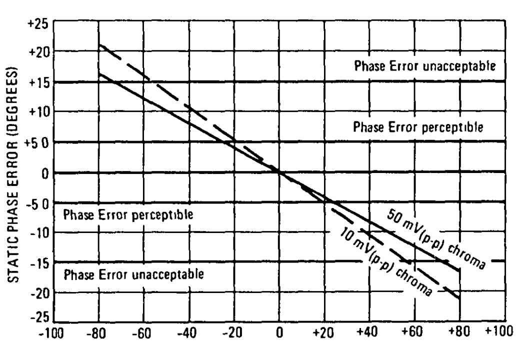
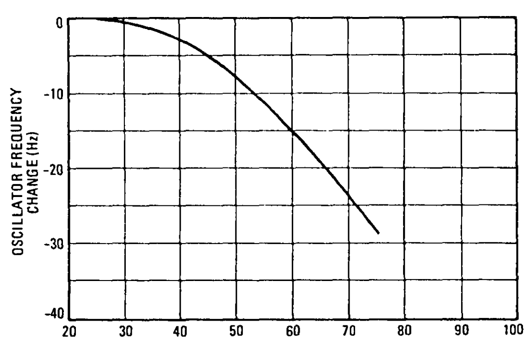
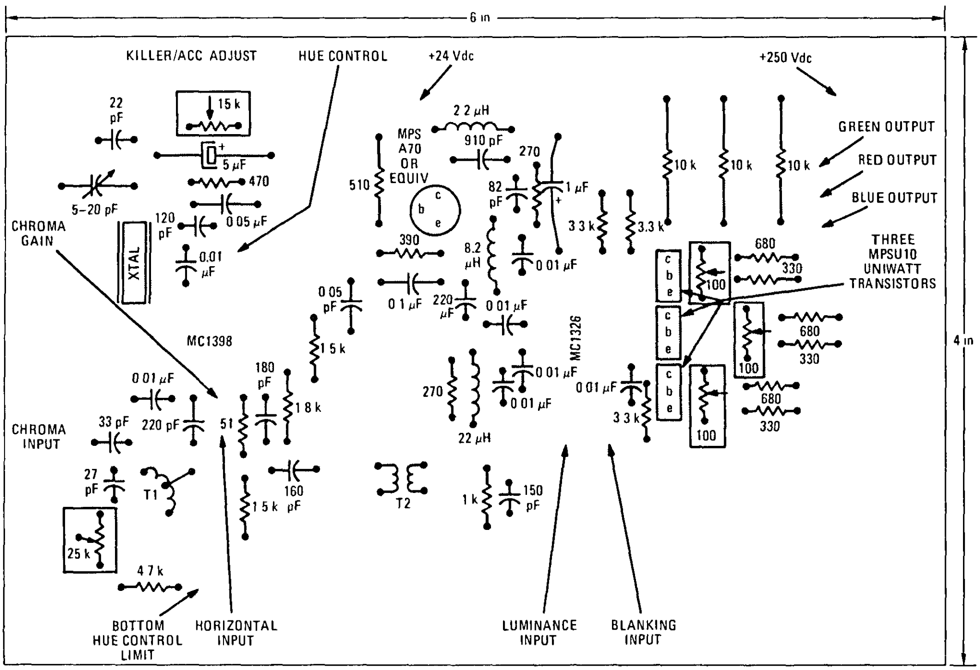


FIGURE 9 – TEMPERATURE STABILITY of the MC1398 OSCILLATOR

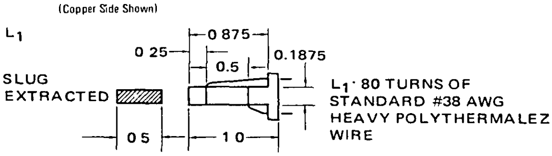
(I/C only subjected to temperature change)





NOTES
All resistors are 1/4 W unless otherwise noted
(Copper Side Shown)

L_1



MC1398P APPLICATIONS INFORMATION

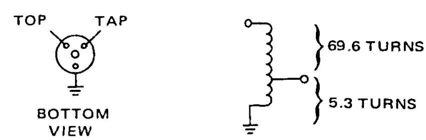
MC1398P is a multifunction circuit with considerable gain associated with the chroma amplifier and oscillator sections. It is important to the circuit layout utilizing the MC1398P that the chroma amplifier, oscillator, and oscillator output/hue section grounds are separated from each other. Ground loop problems will interfere with oscillation stability and lock-up if this precaution is not observed.

Care must be exercised to avoid coupling from the oscillator output to the crystal circuitry connected to pin 8. Stray coupling of these two points can result in excessive oscillator shift; or in some cases, oscillator drop-out during adjustment of the hue control.

A suitable circuit layout for the MC1398P is shown in Figure 10.

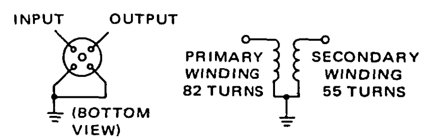
An adjustable capacitor (1.5–20 pF in parallel with a fixed 22 pF capacitor) is shown in series with the 3.58 MHz crystal. This capacitor is used to adjust the oscillator exactly on frequency, and ensures excellent oscillator lock-up. However, acceptable oscillator performance can be obtained with a fixed value of capacitance (this value is dependent on the designers' choice of crystals).

T_1:



COILCRAFT FORM #10-32 OR EQUIV
UNIVERSAL AWG #36 WIRE OR EQUIV
L = 26 μH

T_2:



COILCRAFT FORM #10-32 OR EQUIV
UNIVERSAL AWG #36 WIRE OR EQUIV
L_P = 12 μH primary winding
L_S = 8 8 μH secondary winding
K = 0.4

This coil data is intended as an aid only. It is expected that many designers will want to use other approaches.

MC1398P CIRCUIT DESCRIPTION

The MC1398P is capable of providing the entire color processing function between the second detector and the demodulator for television color receivers.

A band pass filter from the second detector provides a 50 mV (p-p) signal (for a saturated color bar pattern) at the input to the first chroma amplifier stage (Q_2, Q_3, Q_8, Q_9). Because of Q_2 emitter load resistor the input impedance is determined primarily by the bias resistor (R_3) and is about 2.3 kilohms. Since Q_2 is the current source for the differential pair (Q_3 and Q_9), the chroma information will pass to the load resistor (R_7) and then to the second chroma amplifier (Q_{17}). To avoid overload of Q_{17}, the maximum gain to Q_{17} base is only X3 and by varying the bias at the base of Q_9 it is possible to reduce the stage gain by 23 dB without signal distortion; the signal being "dumped" by Q_9 collector into the supply. Since this automatic chroma control action will vary the dc bias at Q_{17} base the emitter load of Q_{17} is the current source Q_{18}, maintaining the dc operating current. Q_{18} collector is bypassed externally to prevent ac signal attenuation.

During picture scan time, the chroma signal passes through the output level control amplifier (Q_{10}, Q_{11}, Q_{15}, Q_{21}). By changing the bias on Q_{11} and Q_{15} bases the signal can either pass to the output pin 2 or be "dumped" into the supply through Q_{11}. The use of buffer stages Q_{10} and Q_{21} prevent distortion at low-signal levels and the control range is better than 70 dB. The signal output is also buffered by Q_{14} and Q_{20}, thus providing a low impedance drive of up to 2.0 V (p-p) to the demodulator, with an overall gain between pins 5 and 2 of 40 dB. To enable the chroma signal output to reach the amplifiers from Q_{17} collector, Q_{12} is held in conduction by Q_5 which in the absence of any input on pin 4 is not conducting. This high collector voltage also holds Q_{26} in conduction, clamping the input to the burst channel and preventing chroma information reaching the oscillator. During picture retrace time, a positive-going 4.0 µs pulse from the line sweep transformer will turn Q_5 "on" and Q_7 "off". When Q_5 collector goes low, Q_{12} will become "cut-off" preventing the burst signal at Q_{17} collector from reaching the output pin 2. At the same time, Q_{26} turns "off" opening the burst channel. The high collector voltage of Q_7 turns on Q_{16} and Q_{22}. Q_{16} passes the burst signal from Q_{17} collector to the subcarrier regenerator and Q_{22} "fills-in" for Q_{12} during the gate period to prevent a dc shift in the pin 2 output voltage.

The gated burst signal is applied to the oscillator through Q_{27} and Q_{28}. Q_{29}, Q_{50} and Q_{35} together with Q_{27} and Q_{28} form an injection locked oscillator circuit. At series resonance of the crystal connected to pin 8 the impedance of pin 8 is very low, thereby reducing the 3.579545 MHz carrier level at the base of Q_{50}. The signal at the base of Q_{29} is not reduced but the output voltages in R_{33} and R_{42} will change. Any signals outside the response band of the crystal will appear equally at Q_{50} and Q_{29} bases and be suppressed in the output by the differential amplifier common-mode rejection ratio (about 40 dB). To maintain oscillation, a feedback signal with the correct phase is passed by Q_{35} back to the input of Q_{27}. Careful control of the resistor ratios ensures that Q_{29} and Q_{50} are operated linearly with about 350 mV (p-p) at R_{33} and R_{42}, due to self oscillation. A burst signal as low as 2.0 mV (p-p) at the chroma input is sufficient to cause the oscillator to lock to the reference phase and frequency.

As the burst amplitude increases, the level at Q_{29} and Q_{50} collectors changes and this shift is used to provide the automatic chroma control function. Q_{42} and Q_{45} form a modified differential amplifier and with zero offset bias Q_{45} conducts most of the current from Q_{43}. As an increasing burst level swings Q_{29} and Q_{50} collectors, the current from Q_{43} is shunted into Q_{42}. At a point predetermined by the setting of the automatic chroma control connected to pin 10, the composite lateral PNP of Q_{47} and Q_{46} will be biased into conduction. This amplifier has a gain of unity and a filter capacitor (connected to Q_{46} base) prevents any tendency to oscillations. Diode CR_9 provides thermal compensation to ensure a steady color-killer threshold point. The increasing current through Q_{13} emitter is used to control Q_9 base, attenuating the input signal as the burst amplitude increases. The current from Q_{13} also keeps Q_{19} in saturation. When the input signal becomes too small for satisfactory color rendition, Q_{13} current falls and Q_{19} comes out of saturation. This means Q_{25} will saturate, clamping Q_{21} base and "killing" the chroma output stage. R_{24} in the Schmitt trigger circuit ensures that the color-killer will have hysteresis to prevent fluttering between "on" and "off" states

The oscillator output voltages at R_{33} and R_{42} are used to drive Q_{38} and Q_{39} into limiting so that as the burst amplitude increases the oscillator activity to around 700 mV (p-p), there will be no change in the oscillator output amplitude at pin 13 Q_{38} and Q_{39} are used as current sources with a 180° phase difference for the differential pairs Q_{30} and Q_{31}, Q_{34} and Q_{37}. A small capacitor attached externally to Q_{39} collector adjusts the total phase difference to 135°. Since the signal appearing in the load resistor R_{51} will be the vector sum of Q_{31} and Q_{37} signals, varying the base bias of Q_{30} and Q_{34} will change the oscillator output phase over the 135° range. Q_{40} and Q_{41} buffer the oscillator output providing a low impedance drive at pin 13 for the demodulator.

To minimize crosstalk between the burst and chroma channels, separate bias chains are used. Further, the oscillator bias chain is zener regulated to prevent phase shifts in the reference output with power-supply variations.

5

MC1399

Advance Information

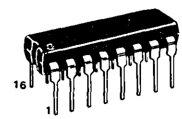
TV COLOR PROCESSING CIRCUIT

The MC1399 contains a chroma IF amplifier with automatic chroma control, color killer, linear dc chroma control, and a phase lock loop subcarrier regenerator system followed by a dc hue control.

- High Gain Automatic Chroma Control (ACC)
- High Gain Phase Lock Loop Subcarrier Regenerator System
- Color Killer with Externally Defined Threshold
- Critical Design Parameters Externally Adjustable
- Linear dc Chroma Control
- DC Hue Control with Well Defined Range and Center
- Internal Gating for Color Burst
- Built-In Supply Regulator
- Compatible with Most Existing Demodulators

TV COLOR PROCESSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION		
Device	Temperature Range	Package
MC1399P	-20 to +75°C	Plastic DIP

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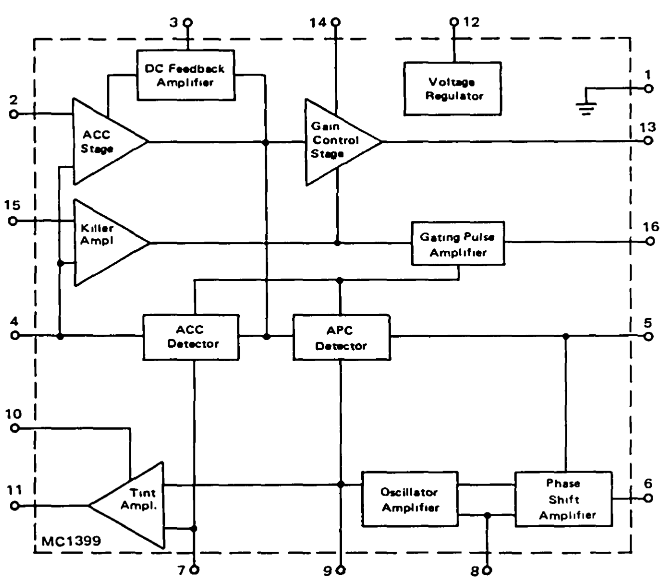
FIGURE 1– MC1399 BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Current	60	mA
Horizontal Pulse Input Current	4 2	mA
Minimum Load Resistance (Pins 11, 13)	2.7	kΩ
Junction Temperature	150	°C
Operating Ambient Temperature Range	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS See Test Circuit, Figure 5. (All Switches in Position 1 Unless Otherwise Noted.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (V_C) (Pin 12)	–	12.6	–	Vdc
Load Regulation (Pin 12) (V_{CC} from +22 V to +26 V)	–	100	–	mVdc
APC Set Up Voltage (R2)	0 61	–	0 81	%V_{CC}
ACC Set Up Voltage (R1)	0.57	–	0.79	%V_{CC}
Chroma Control Output Voltage				
(S1 Position 2)	–	1.25	–	Vp-p
(S1 Position 3)	–	625	–	mVp-p
(S1 Position 4)	–	12	–	mVp-p
Oscillator Output				
(S2 Position 2)	–	2.2	–	Vp-p
(S2 Position 1)	–	1.6	–	Vp-p
(S2 Position 3)	–	2.2	–	Vp-p
Oscillator Output Phase (Referred to Chroma Output Pin 13)				
(S2 Position 1)	–	231	–	Deg.
(S2 Position 2)	–	185	–	Deg.
(S2 Position 3)	–	268	–	Deg.
Static Phase Error (SPE) with Oscillator Detuned	–	0.02	–	Degrees/Hz
Automatic Chroma Control (ACC)				
Chroma Output for Input of:				
+6.0 dB (360 mVp-p Burst)	–	2.65	–	Vp-p
-14 dB (36 mVp-p Burst)	–	2.1	–	Vp-p
Chroma Output Voltage (Pin 13) for Input of -20 dB (Killer On) (18 mVp-p Burst @ Pin 2)	–	10	–	mVp-p

TYPICAL DESIGN CHARACTERISTICS (Figure 5)

Characteristic		Typ	Unit
Input Impedance	Pin 2	2.0	kΩ
		2.0	pF
	Pin 7	10	kΩ
		2.0	pF
	Pin 9	10	kΩ
		2.0	pF
Output Impedance Pins 6, 11, 13		50	Ω
Oscillator Drift with Temperature (Device Only)		0.7	PPM/°C
Oscillator Δf with V_{CC}		+20	Hz/Volt
Chroma Output Level Drift with Temperature (Device Only, 25 to 75°C)		10	%
Chroma Output Level Sensitivity to V_{CC} (Device Only)		2.0	%/Volt
Pull-In Range		±500	Hz
Noise Bandwidth (f_{nn})		150	Hz
Oscillator Control Sensitivity (β)		1.2	Hz/mV
APC Phase Detector Sensitivity (μ)		42	mV/Degree

FIGURE 2 – ACC CHARACTERISTICS

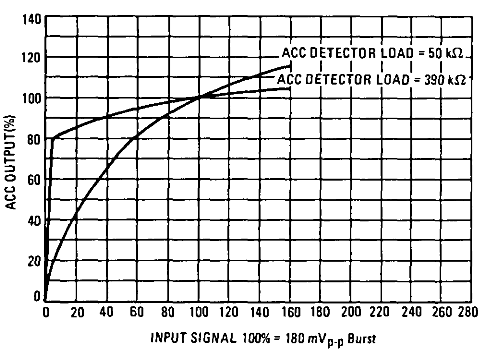


FIGURE 3 – GAIN CONTROL CHARACTERISTICS

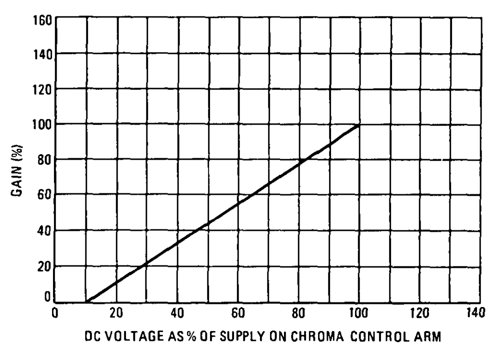


FIGURE 4 – TINT CONTROL CHARACTERISTICS

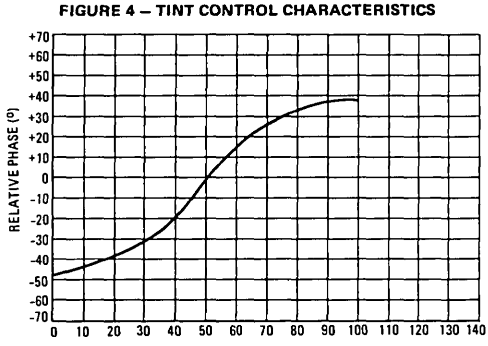


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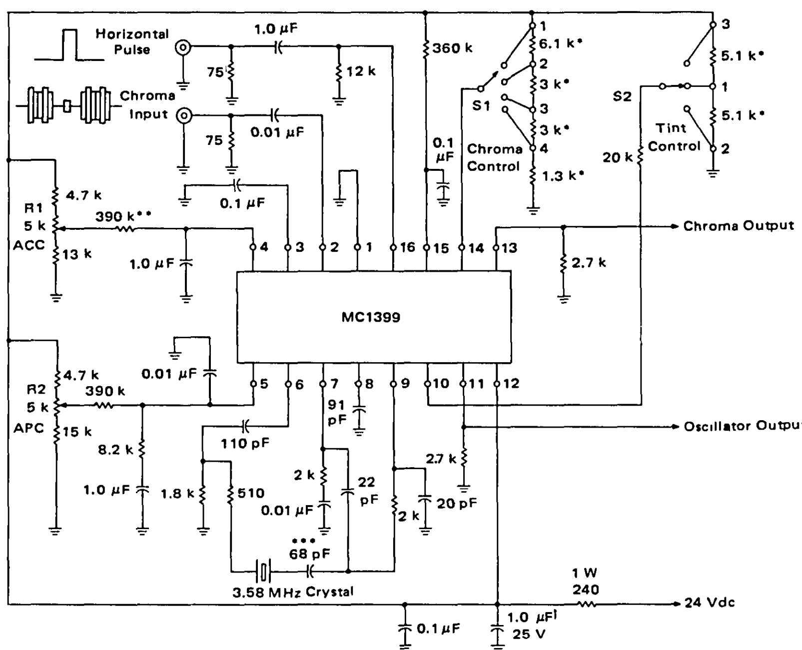
FIGURE 5 — DYNAMIC CHARACTERISTIC TEST CIRCUIT



Set-Up: Apply 6 μs, 15.734 kHz Horizontal Pulse 3 Vp-p, Centered on Burst.
Adjust APC Control for 3.579545 MHz with No Chroma Input.
Apply NTSC 75% Bar Chart, (Luminance, Sync and Set-up Removed) and Adjust ACC Control for 2.5 Vp-p Red Bar at Chroma Output.

*1% Resistor Tolerance

**Determines ACC loop gain, see Figure 2.

***Value determined by crystal.

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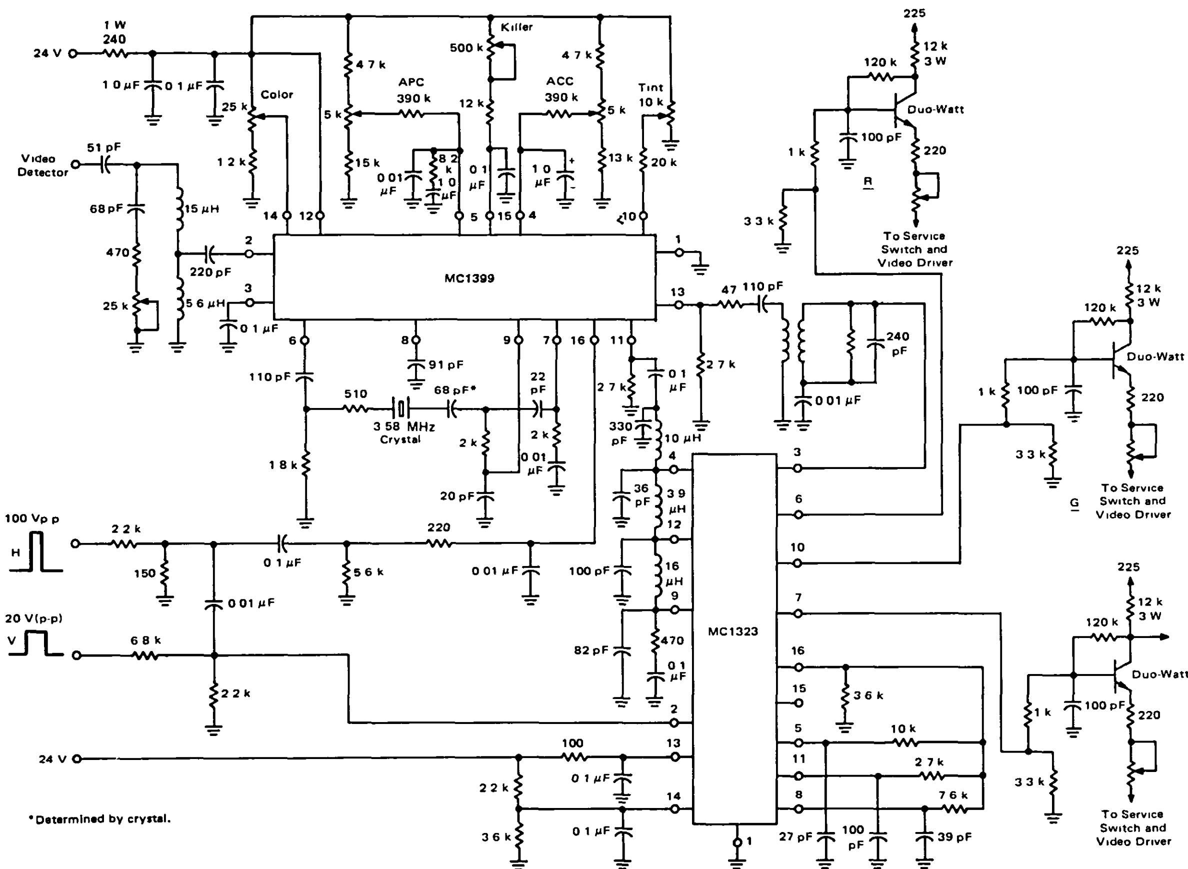

24 V
1 W
240
1 0 µF
0 1 µF
Color
25 k
1 2 k
Video Detector
51 pF
68 pF
15 µH
470
25 k
220 pF
5 6 µH
0 1 µF
4 7 k
5 k
15 k
APC
390 k
0 01 µF
8 2 k
1 0 µF
500 k
Killer
12 k
0 1 µF
ACC
390 k
4 7 k
5 k
1 0 µF
13 k
Tint
10 k
20 k
MC1399
110 pF
510
3 58 MHz Crystal
68 pF*
22 pF
2 k
2 k
0 01 µF
20 pF
1 8 k
91 pF
47
110 pF
2 7 k
240 pF
0 01 µF
2 7 k
0 1 µF
330 pF
10 µH
36 pF
3 9 µH
16 µH
100 pF
82 pF
470
0 1 µF
100 Vp p
H
2 2 k
150
0 1 µF
5 6 k
220
0 01 µF
0 01 µF
20 V(p-p)
V
6 8 k
2 2 k
24 V
100
0 1 µF
2 2 k
3 6 k
0 1 µF
MC1323
3 6 k
10 k
2 7 k
7 6 k
27 pF
100 pF
39 pF
*Determined by crystal.
225
12 k
3 W
120 k
Duo-Watt
100 pF
1 k
220
3 3 k
R
To Service Switch and Video Driver
G
To Service Switch and Video Driver
To Service Switch and Video Driver

5

ORDERING INFORMATION

Device	Temperature Range	Package
MC3310P	0°C to +75°C	Plastic DIP

MC3310P

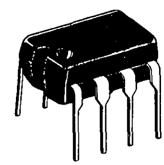
WIDE-BAND AMPLIFIER

. . . designed for FM/IF and low-level audio applications.

- High Audio Gain — 60 dB minimum
- Useful as a Microphone Amplifier and in Tape Recorders and Cassettes
- Excellent Performance as a 10.7 MHz FM/IF Amplifier
- High Transconductance (g_m) Ideally Suited to Low Impedance Ceramic Filters
- Formerly MFC4010A in Case 206A Package

WIDE-BAND AMPLIFIER

SILICON MONOLITHIC FUNCTIONAL CIRCUIT



CASE 626-03

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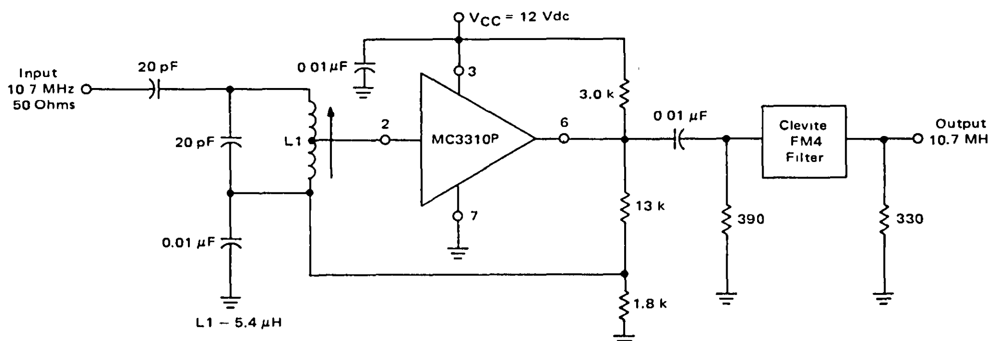
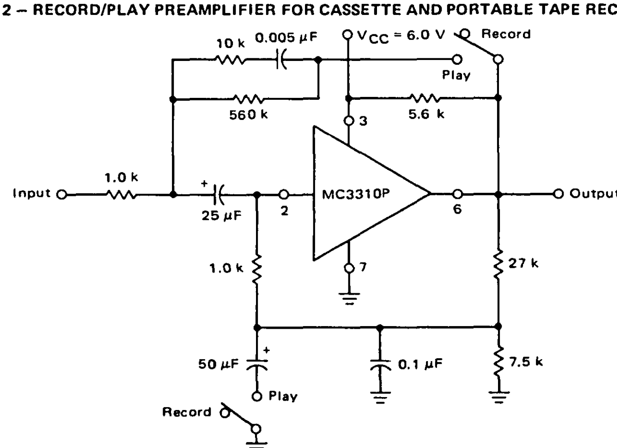
FIGURE 1 — FM/IF AMPLIFIER



L1 — 5.4 µH
36 Turns, #30 AWG Wire Wound on 1/4" Slug Tuned Form, Tapped 8 Turns from Ground End
Slug· T H. Material 1/4" Dia , 1/2" Length

FIGURE 2 — RECORD/PLAY PREAMPLIFIER FOR CASSETTE AND PORTABLE TAPE RECORDERS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	21	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation)	1.2	Watts
Derate above 25°C	10	mW/°C
Operating Ambient Temperature Range	0 to +75	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic		Min	Typ	Max	Unit
Open Loop Voltage Gain (Figure 3) (f = 1.0 kHz)		60	68	–	dB
h Parameters(1) (f = 1.0 kHz)	h_{11}	–	1.0	–	k ohms
	h_{12}	–	10^{-6}	–	–
	h_{21}	–	1000	–	–
	h_{22}	–	10^{-5}	–	mhos
Output Noise Voltage (Figure 3)		–	3.0	–	mV(RMS)
(BW = 20 Hz to 20 kHz, R_S = 1.0 k ohms)		–	3.0	–	
Current Drain		–	3.0	–	mA

HIGH FREQUENCY CHARACTERISTICS (V_{CC} = 12 Vdc, f = 10.7 MHz, T_A = 25°C unless otherwise noted)

Characteristic		Min	Typ	Max	Unit
Power Gain (Figure 1) e_{in} = 0.1 mVRMS)		–	42	–	dB
Noise Figure (Figure 1) ($R_S \approx$ 740 Ohms)		–	6.0	–	dB
y Parameters(1) (f = 10.7 MHz, I_2 = 2.0 mA)	y_{11}	–	1.3 + j1.5	–	mmhos
	y_{12}	–	-3.4 + j8.1	–	μmhos
	y_{21}	–	-0.33 + j0.68	–	mho
	y_{22}	–	120 + j0	–	μmhos

(1) Device only, without external passive components

FIGURE 3 – AUDIO TEST CIRCUIT

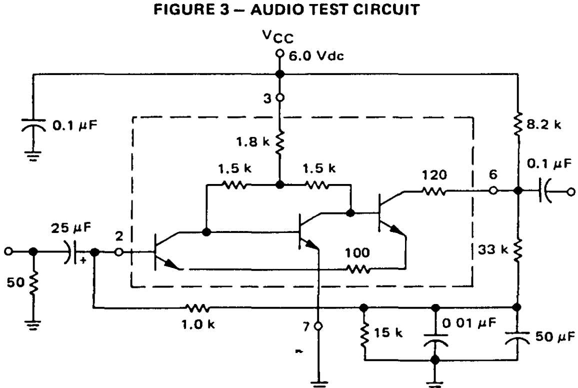
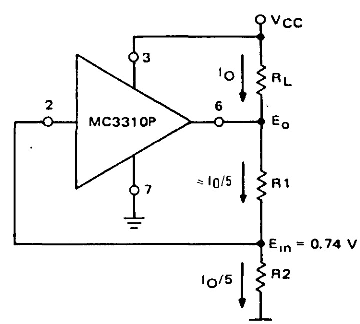


FIGURE 4 – BIASING RECOMMENDATIONS



Select	V_{CC}, E_o, and I_O
Solve for	$R_L = (V_{CC} - E_o)/I_O$
Let	$R2 = 5(0.74)/I_O$
Then.	$R1 = R2\,(E_o - 0.74)/0.74$

TYPICAL CHARACTERISTICS

AUDIO PERFORMANCE CHARACTERISTICS
(for Test Circuit Figure 3)

FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

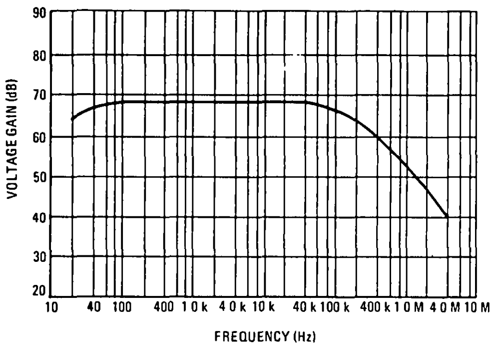
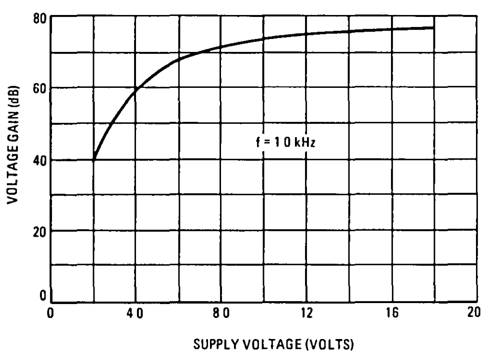


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY



*TAPE PREAMPLIFIER PERFORMANCE
(for Circuit Figure 2)

FIGURE 7 – RECORD VOLTAGE GAIN versus FREQUENCY

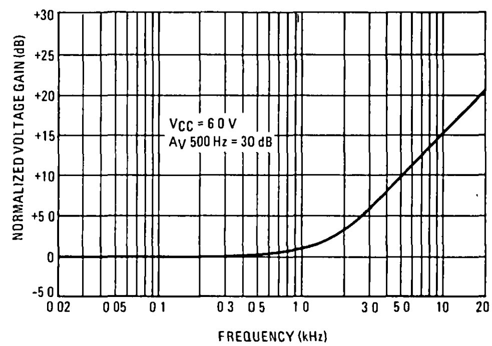
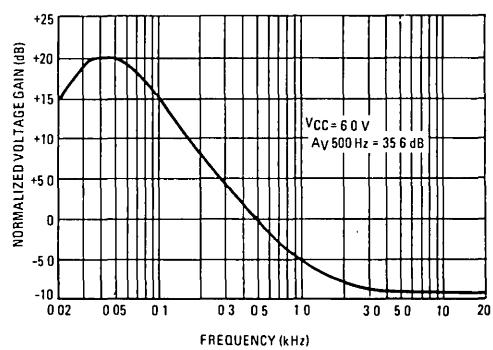


FIGURE 8 – PLAYBACK VOLTAGE GAIN versus FREQUENCY



Note

The record/playback characteristics shown in Figures 8 and 9 were taken with the preamplifier driven by a 50 ohm source The curves are typical of a desired response for the preamplifier, however, every type of tape recording and playback head is different and this circuit will not necessarily satisfy all requirements No particular tape head was used as a basis for circuit design. The circuit is only an example showing the equalization network configuration

The ideal preamplifier will have an input impedance approximately 10 times the highest impedance of the tape head and every preamplifier circuit must be designed using a test tape to verify the response of the design

10.7 MHz y PARAMETERS

FIGURE 9 – INPUT ADMITTANCE

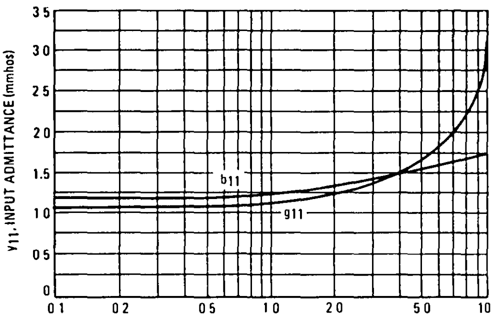


FIGURE 10 – REVERSE TRANSFER ADMITTANCE

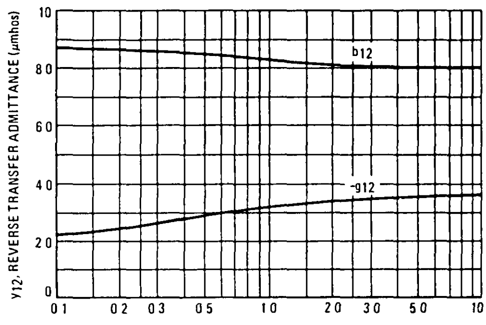


FIGURE 11 – FORWARD TRANSFER ADMITTANCE

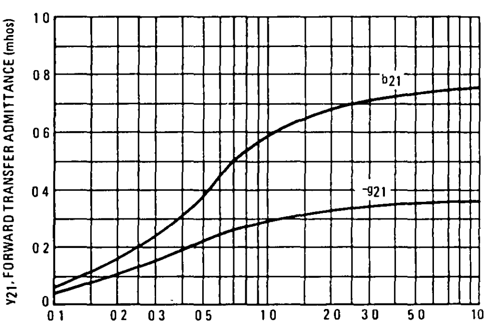
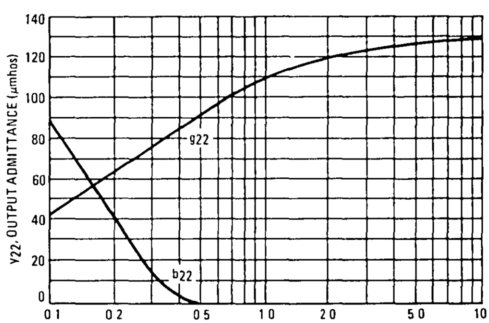


FIGURE 12 – OUTPUT ADMITTANCE



10.7 MHz PERFORMANCE
(Circuit of Figure 1)

FIGURE 13 – POWER GAIN versus SUPPLY VOLTAGE

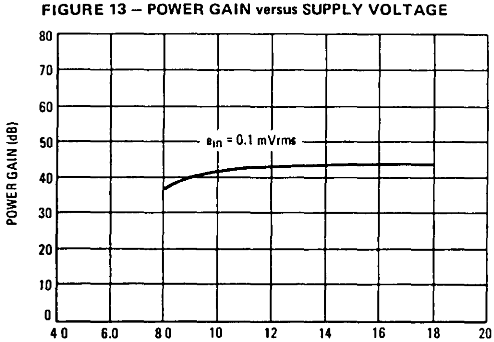
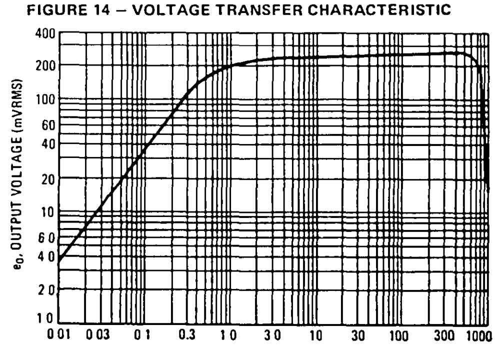


FIGURE 14 – VOLTAGE TRANSFER CHARACTERISTIC



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MC3325

Advance Information

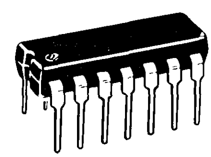
AUTOMOTIVE VOLTAGE REGULATOR

. . . designed for use in conjunction with an NPN Darlington transistor in a floating field alternator charging system.

- Overvoltage Protection
- Shut-Down on Loss of Battery Sense
- Selectable Temperature Coefficient
- Available in Chip Form for Hybrid Assembly

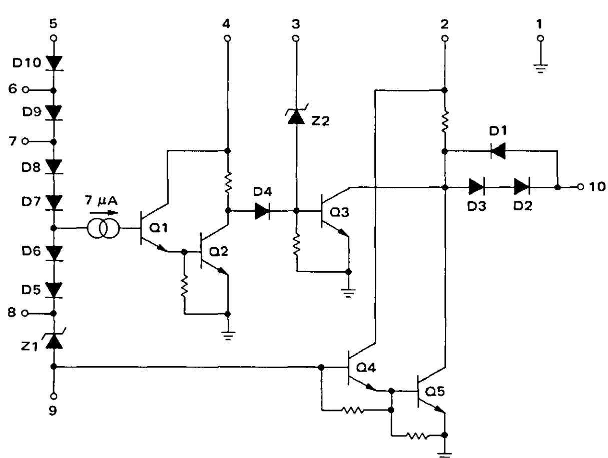
AUTOMOTIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

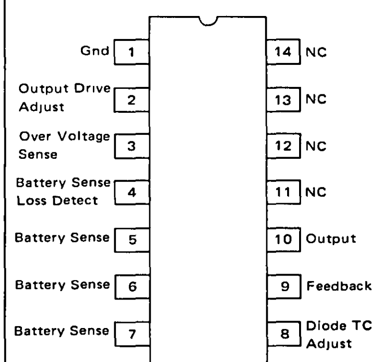


P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116

CIRCUIT SCHEMATIC



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3325P	-40 to +85°C	Plastic DIP

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Current Into Pins 5, 6, and 7	$I_{5, 6, or 7}$	50	mA
Current Into Pin 3	I_3	20	mA
Current Into Pin 4	I_4	20	mA
Current Into Pin 2	I_2	120	mA
Current Into Pin 8	I_8	50	mA
Current Into Pin 9	I_9	50	mA
Current Into Pin 10	I_{10}	50	mA
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Diode TC Adjust: Threshold Voltage on Pin 8 (Figure 1)	V_8	7 9	–	8.8	V
Battery Sense: Threshold Voltage on Pin 5 (Figure 1)	V_5	11.8	–	13.3	V
Battery Sense: Threshold Voltage on Pin 6 (Figure 1)	V_6	11.1	–	12.6	V
Battery Sense: Threshold Voltage on Pin 7 (Figure 1)	V_7	10.5	–	11.8	V
Battery Sense Loss Detect: Threshold Current Into Pin 4 (Figure 2)	I_4	–	–	600	μA
Battery Sense Loss Detect: Threshold Voltage at Pin 4 ($I_4 \leq 600$ μA, Figure 2)	V_4	1.3	–	1.7	V
Overvoltage Sense: Threshold Current Into Pin 3 (Figure 2)	I_3	–	–	600	μA
Overvoltage Sense: Threshold Voltage at Pin 3 ($I_3 \leq 600$ μA, Figure 2)	V_3	6.7	–	9.0	V
Output Drive Adjust: Voltage Drop from Pin 2 to Pin 10 (I_2 = 10 mA, Figure 3)	V_2	1.9	–	2.4	V
Low State Output Voltage at Pin 10 (I_3 = 12 mA, I_2 = 120 mA, Figure 4)	V_{10}	–	–	0.7	V

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TEST CIRCUITS

FIGURE 1

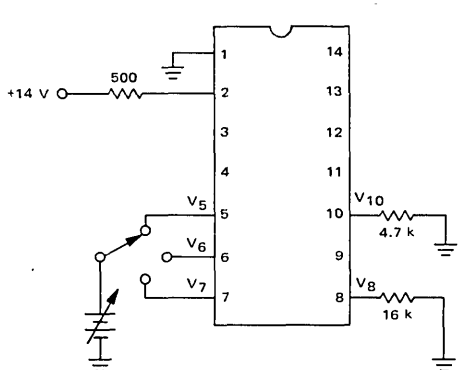

FIGURE 2

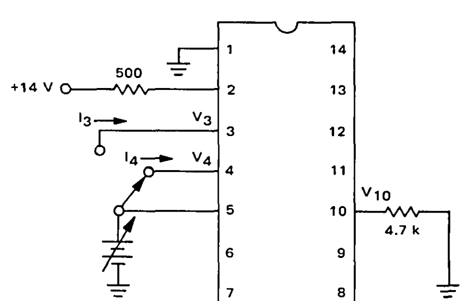

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FIGURE 3

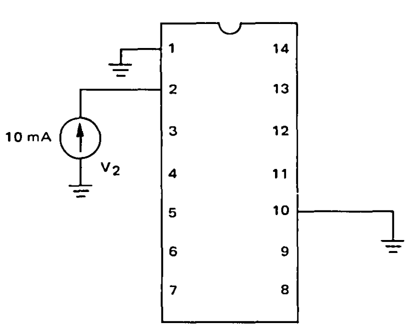


FIGURE 4

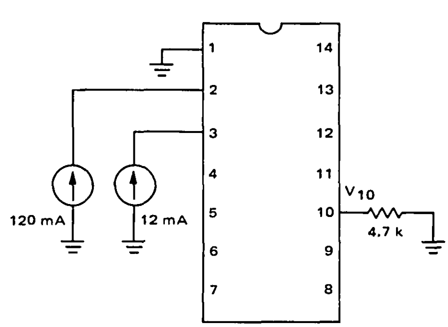
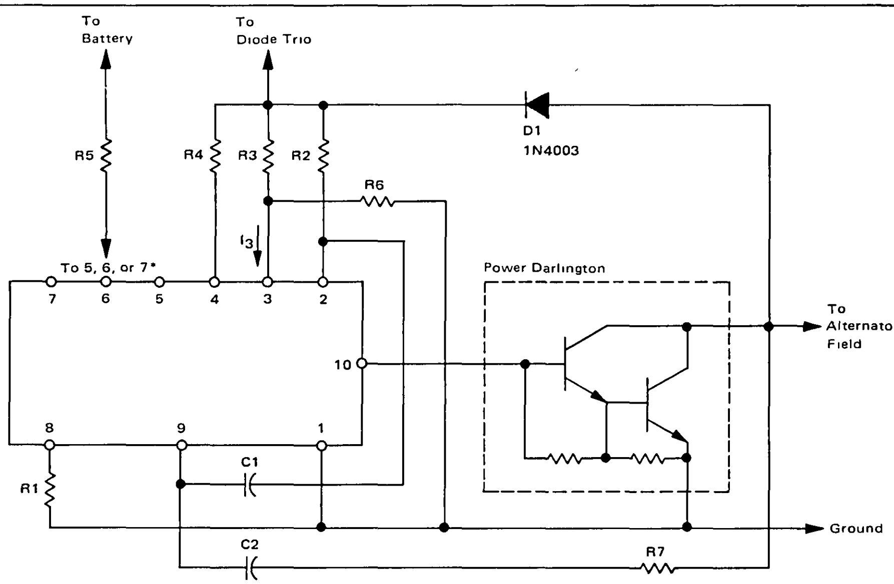


FIGURE 5 – APPLICATION CIRCUIT



*Note: The temperature coefficient of the battery voltage sense terminal is determined by the number of diodes used in the diode string (i.e., whether Pin 5, 6, or 7 is used). The approximate temperature coefficient for a diode at 1.0 mA is -2.0 mV/°C, and for a zener diode it is +3.0 mV/°C. Counting from ground (see circuit schematic) we have -2.0 mV for Q5, -2.0 mV for Q4, +3.0 mV for Z1, -8.0 mV for D5 thru D8, and an additional -2.0 mV each for D9 and D10 if used. The total temperature coefficient can be varied from approximately -9.0 mV/°C to -13 mV/°C depending on the number of the diodes in the diode string that are utilized.

APPLICATIONS CIRCUIT INFORMATION
(See Figure 5)

R1 Determines the temperature coefficient by setting the value of current in the diode string. As the value of R1 decreases, so does the effective TC. R1 should be chosen so that the current in the diode string is between 0.5 mA and 1.0 mA.

R5 This resistor determines the V_{reg} voltage as defined by the following equation:

$$V_{reg} = \left(1 + \frac{R5}{R1}\right) 8.4 + \left(n + \frac{R5}{5k}\right)(0.7)$$

n = number of diodes used in diode string ($4 \leq n \leq 6$)

R4 Used as a current limiting resistor on Pin 4 in case of an open battery voltage sense lead.

R3 Used as a current limiting resistor on Pin 3 in case of overvoltage at the diode trio. Voltage at Pin 3 will run approximately 7.5 volts. R3 should be chosen so that the current (I_3) at maximum overvoltage is between 2.0 mA and 6.0 mA.

R2 This resistor determines the output drive current. Refer to specifications for the darlington driver and select the value for R2 that will provide enough drive to the output when the diode trio voltage is at a minimum.

$$I_{Drive} \cong \frac{V_{min} - 2.8\ V}{R2 + 50\ \Omega}$$

R6 This resistor in conjunction with R3 is used to set the maximum overvoltage.

$$\text{Maximum overvoltage} \cong \frac{R3 + R6}{R6}\ (7.5)$$

R7 Used for compensation (Approximately 3.0 kΩ)

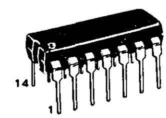
C1, C2 Used for compensation (Approximately 0.01 μF)

MC3333

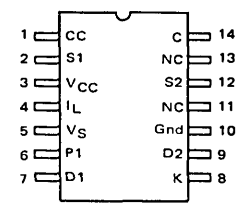
VARI-DWELL IGNITION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 646



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3333P	-40 to +85	Plastic DIP

VARI-DWELL IGNITION CIRCUIT

. . . designed for use in conjunction with a flux averaging sensor and a high energy ignition coil to provide regulated current pulses to the coil from information supplied by the sensor.

- Wide Supply Voltage Operating Range (4 to 24 V)
- Externally Adjustable Overvoltage Shutdown
- Externally Adjustable Dwell Time and Spark Energy
- Extremely Stable Output Current Pulses
- Variable Input Threshold Compensates for Low Supply Voltage Conditions
- Low Static Current Drain
- Also Available in Flip-Chip (MCCF3333) and Standard Chip (MCC3333) Form

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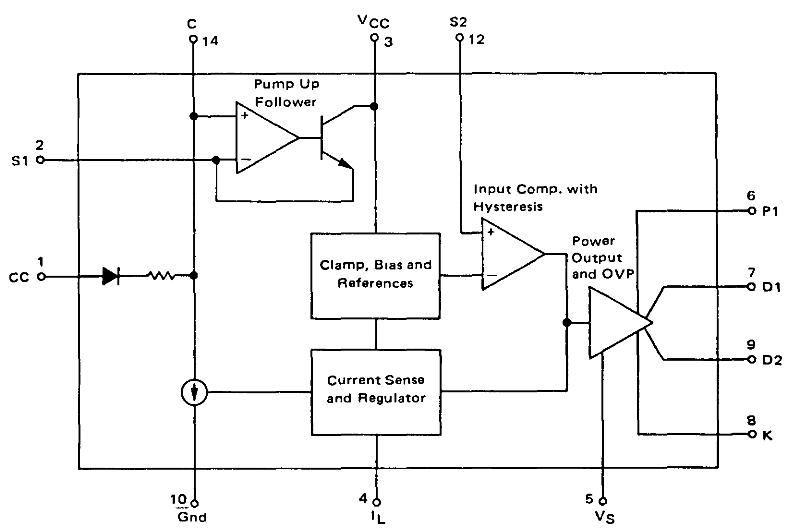
FIGURE 1 — BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage Steady State (Through 400 Ω, see Fig 2)	V_{CC}	24	Vdc
Transients of 300 ms or less		90	
Peak Output Sink Current	$I_{S(PEAK)}$		A
Transients of 300 ms or less		1 3	
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.5 V, T_A = 25°C unless otherwise specified; Figure 2.)

Characteristic	Symbol	Pin(s) Under Test	S1	S2	S3	S4	S5	S6	Min	Typ	Max	Unit
Current Drain	I_D	3	A	A	A	A	A	A	8.0	15	25	mA
Pre-Driver On	V_{P1}	6	A	A	A	A	A	A	–	.90	2.0	V
D1, D2 Output On	$V_{D1, D2}$	7&9	A	A	A	A	A	A	–	110	500	mV
Kelvin Contact	V_K	8	A	A	A	A	A	A	–	40	200	mV
CC Charge Circuit	V1	1	B	A	A	A	A	E	700	800	900	mV
S1 Follower	V_{S1}	2	A	B	A	A	A	C	1 4	1.6	1.8	V
C Clamp High	V_c	14	A	A	A	A	A	D	–	8 4	8.8	V
S2 Turn On (measure V_{S2} ramp value at P1 switch point)	V_{S2}	12	A	A	A	A	B	A	1.6	1.9	2.1	V
Overvoltage Protection	V_S	5	A	A	A	B	C	A	8 0	9.1	10	V
Current Limit Trip	V_{IL}	4	A	A	B	A	C	B	150	180	220	mV

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FIGURE 2 — TEST CIRCUIT

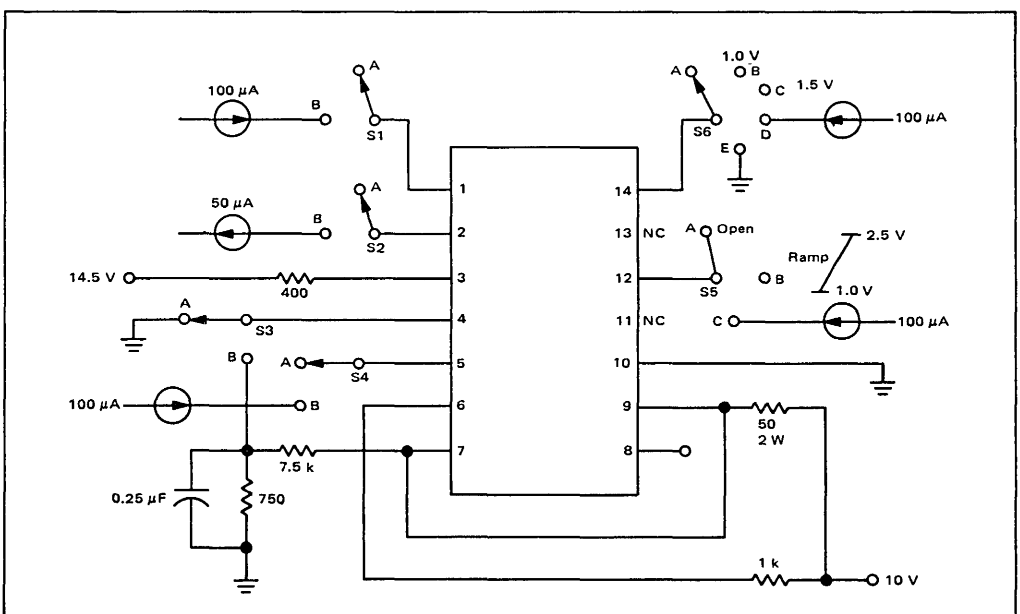
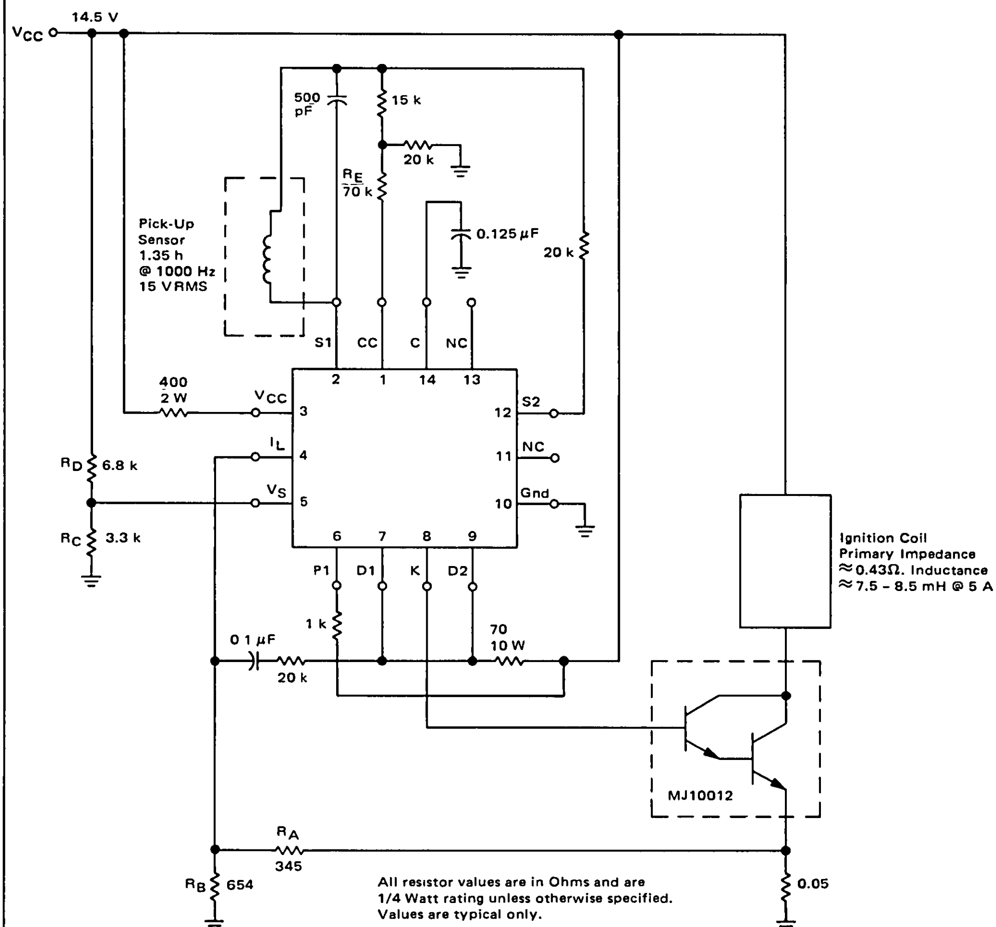


FIGURE 3 – TYPICAL APPLICATION CIRCUIT



All resistor values are in Ohms and are 1/4 Watt rating unless otherwise specified. Values are typical only.

Notes:

1. The ratio of R_A to R_B controls the ignition coil regulated current.

$$I_{COIL} \approx 3.6 \left(\frac{R_A + R_B}{R_B}\right) \qquad R_A + R_B \approx 1\ k\Omega$$

2. The ratio of R_D to R_C sets the over-voltage shutdown point with respect to B+.

$$B+_{overvoltage} \approx 8 \left(\frac{R_C + R_D}{R_C}\right) \qquad R_C + R_D \approx 10\ k\Omega$$

3. R_E is active region dwell control. R_E = 70 kΩ results in output current limit time of approximately 10% at 1000 RPM (with respect to one distributor cycle in an 8 cylinder engine). Values less than 70 kΩ lengthen this limit time and values higher shorten this limit time.
4. The 0.1 µF capacitor at pin 4 may be eliminated and stability maintained. A readjustment of the R_A and R_B resistors will be required.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3340P	0°C to +75°C	Plastic DIP

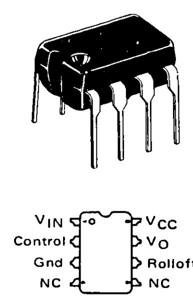
MC3340P

ELECTRONIC ATTENUATOR

- Designed for use in:
  - DC Operated Volume Control
  - Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 8-Pin Dual In-Line Package
- Formerly MFC6040 in Case 643A Package

ELECTRONIC ATTENUATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

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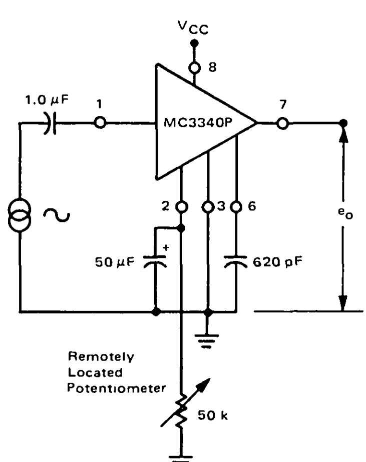
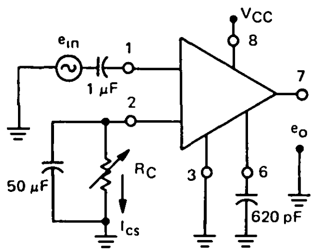
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	20	Vdc
Power Dissipation @ T_A = 25°C Derate above T_A = 25°C	1.2 10	Watts mW/°C
Operating Ambient Temperature Range	0 to +75	°C

FIGURE 1 — TYPICAL DC "REMOTE" VOLUME CONTROL

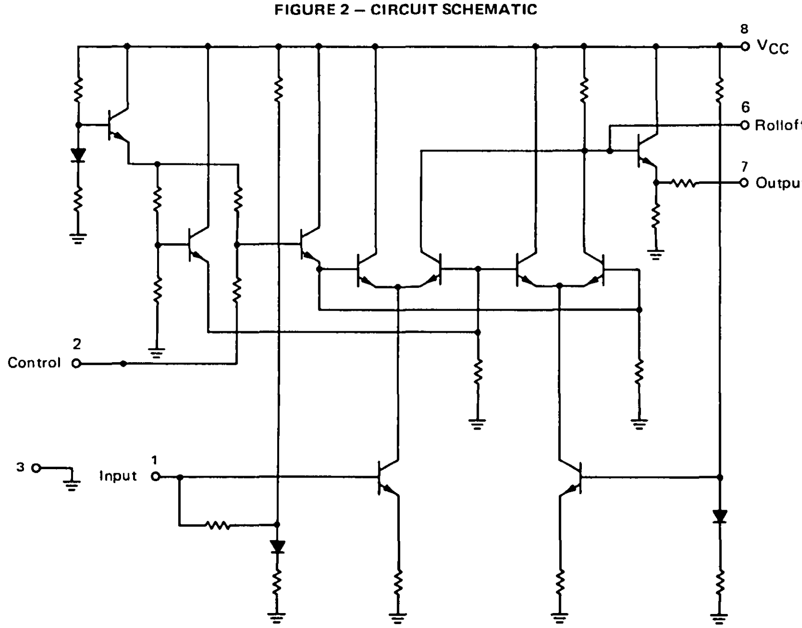


ELECTRICAL CHARACTERISTICS (e_{in} = 100 mV (RMS), f = 1.0 kHz, R1 = 0, V_{CC} = 16 Vdc, T_A = +25°C unless otherwise noted.)

Circuit	Characteristic	Min	Typ	Max	Unit
	Operating Power Supply Voltage	9.0	–	18	Vdc
	Control Terminal Sink Current (e_{in} = 0)	–	–	2.0	mAdc
	Maximum Input Voltage	–	–	0.5	V(RMS)
	Voltage Gain	11	13	–	dB
	Attenuation Range (R_C = 33 k ohms)	70	90	–	dB
	Total Harmonic Distortion (Pin 2 Gnd) (e_{in} = 100 mV (RMS), e_o = A_v x e_{in})	–	0.6	1.0	%

5

FIGURE 2 – CIRCUIT SCHEMATIC



TYPICAL ELECTRICAL CHARACTERISTICS

(V_{CC} = 16 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – ATTENUATION versus DC CONTROL VOLTAGE

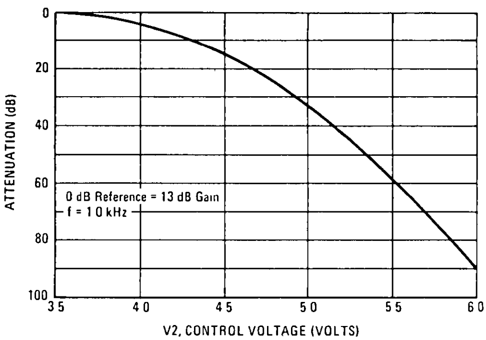


FIGURE 4 – ATTENUATION versus CONTROL RESISTOR

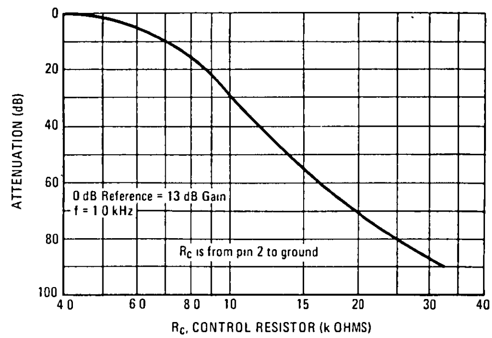


FIGURE 5 – FREQUENCY RESPONSE

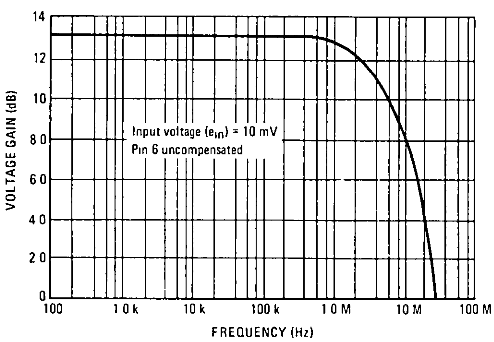


FIGURE 6 – OUTPUT VOLTAGE SWING

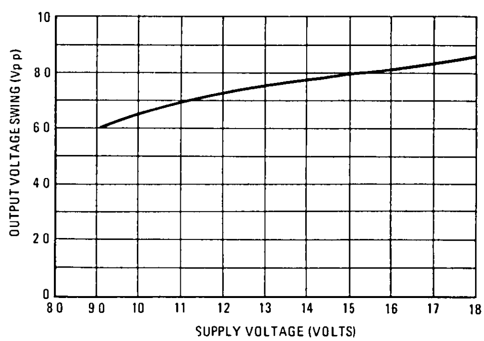
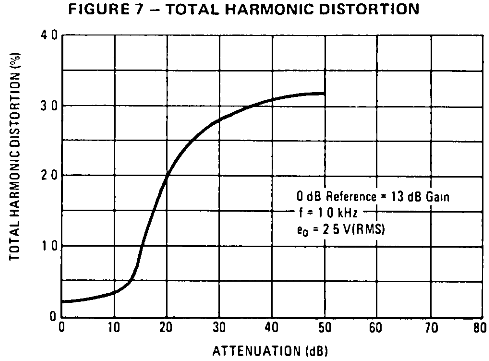


FIGURE 7 – TOTAL HARMONIC DISTORTION



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ORDERING INFORMATION

Device	Temperature Range	Package
MC3346P	−40°C to +85°C	Plastic DIP
MC3386P	−40°C to +85°C	Plastic DIP

MC3346
MC3386

ONE DIFFERENTIALLY-CONNECTED PAIR AND THREE ISOLATED TRANSISTOR ARRAY

The MC3346 and MC3386 are designed for general-purpose, low power applications for consumer and industrial designs.

- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified – 10 μA to 10 mA
- Five General-Purpose Transistors in One Package

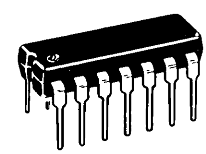
GENERAL-PURPOSE TRANSISTOR ARRAY

SILICON MONOLITHIC INTEGRATED CIRCUIT

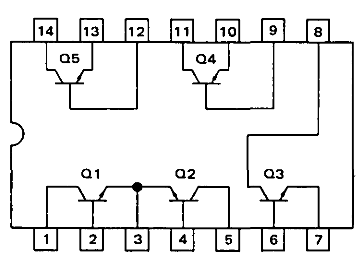
5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5 0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current – Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C Derate Each Transistor @ 25°C	P_D	1.2 10 300	Watts mW/°C mW/°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



P SUFFIX
PLASTIC PACKAGE
CASE 646



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MC3346P Min	MC3346P Typ	MC3346P Max	MC3386P Min	MC3386P Typ	MC3386P Max	Unit
STATIC CHARACTERISTICS								
Collector-Base Breakdown Voltage (I_C = 10 μAdc)	BV_{CBO}	20	60	–	20	60	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc)	BV_{CEO}	15	–	–	15	–	–	Vdc
Collector-Substrate Breakdown Voltage (I_C = 10 μA)	BV_{CIO}	20	60	–	20	60	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc)	BV_{EBO}	5.0	7.0	–	5.0	7.0	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	40	–	–	100	nAdc
DC Current Gain	h_{FE}							–
(I_C = 10 mAdc, V_{CE} = 3.0 Vdc)		–	140	–	–	–	–	
(I_C = 1.0 mAdc, V_{CE} = 3.0 Vdc)		40	130	–	40	130	–	
(I_C = 10 μAdc, V_{CE} = 3.0 Vdc)		–	60	–	–	–	–	
Base-Emitter Voltage	V_{BE}							Vdc
(V_{CE} = 3.0 Vdc, I_E = 1 0 mAdc)		–	0.72	–	–	0.72	–	
(V_{CE} = 3 0 Vdc, I_E = 10 mAdc)		–	0 80	–	–	0.80	–	
Input Offset Current for Matched Pair Q1 and Q2 (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\|I_{IO1}-I_{IO2}\|$	–	0.3	2.0	–	0.3	–	μAdc
Magnitude of Input Offset Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	–	–	0 5	5.0	–	0.5	–	mVdc
Temperature Coefficient of Base-Emitter Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\frac{\Delta V_{BE}}{\Delta T}$	–	-1 9	–	–	-1.9	–	mV/°C
Temperature Coefficient	$\frac{\|\Delta V_{IO}\|}{\Delta T}$	–	1.0	–	–	1.0	–	μV/°C
Collector-Emitter Cutoff Current (V_{CE} = 10 Vdc, I_B = 0)	I_{CEO}	–	–	0.5	–	–	5.0	μAdc
DYNAMIC CHARACTERISTICS								
Low Frequency Noise Figure (V_{CE} = 3.0 Vdc, I_C = 100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	–	3.25	–	–	3 25	–	dB
Forward Current Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{FE}	–	110	–	–	110	–	–
Short-Circuit Input Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{ie}	–	3 5	–	–	3.5	–	kΩ
Open-Circuit Output Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{oe}	–	15 6	–	–	15.6	–	μmhos
Reverse Voltage Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{re}	–	1.8	–	–	1.8	–	$\times 10^{-4}$
Forward Transfer Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	Y_{fe}	–	31-j1.5	–	–	31-j1.5	–	–
Input Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	Y_{ie}	–	0 3+j0.04	–	–	0.3+j0.04	–	–
Output Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	Y_{oe}	–	0.001+j0.03	–	–	0 001+j0.03	–	–
Current-Gain — Bandwidth Product (V_{CE} = 3.0 Vdc, I_C = 3.0 mAdc)	f_T	300	550	–	–	550	–	MHz
Emitter-Base Capacitance (V_{EB} = 3.0 Vdc, I_E = 0)	C_{eb}	–	0.6	–	–	0.6	–	pF
Collector-Base Capacitance (V_{CB} = 3.0 Vdc, I_C = 0)	C_{cb}	–	0 58	–	–	0.58	–	pF
Collector-Substrate Capacitance (V_{CS} = 3.0 Vdc, I_C = 0)	C_{CI}	–	2 8	–	–	2.8	–	pF

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TYPICAL CHARACTERISTICS

FIGURE 1 – COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)

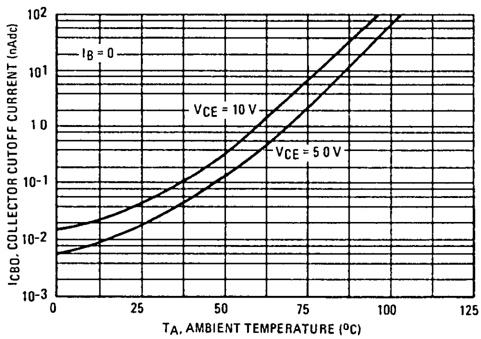


FIGURE 2 – COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)

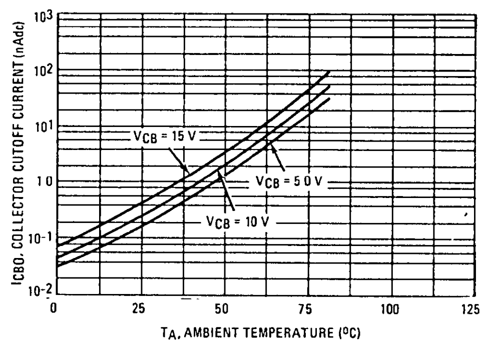


FIGURE 3 – INPUT OFFSET CHARACTERISTICS FOR Q1 and Q2

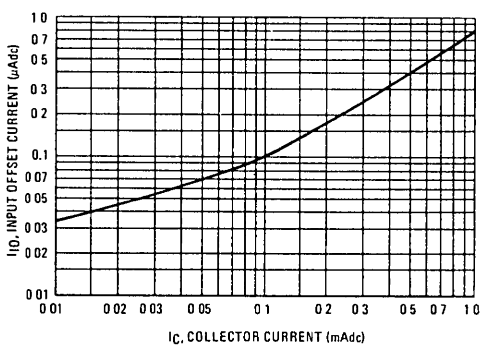


FIGURE 4 – BASE-EMITTER AND INPUT OFFSET VOLTAGE CHARACTERISTICS

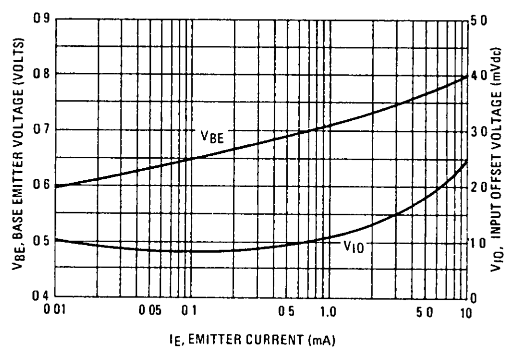
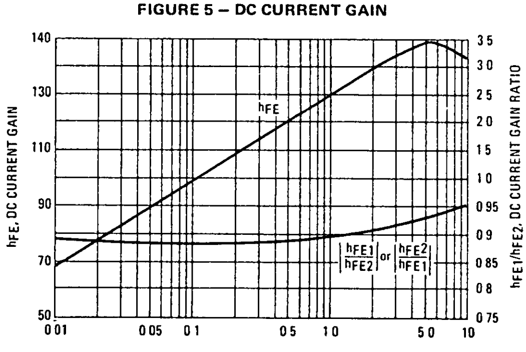


FIGURE 5 – DC CURRENT GAIN



MC3357

Advance Information

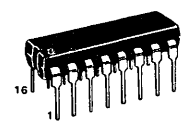
LOW POWER NARROW BAND FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typ) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage — (-3.0 dB) = 5.0 μV (Typ)
- Low Number of External Parts Required

LOW POWER FM IF

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
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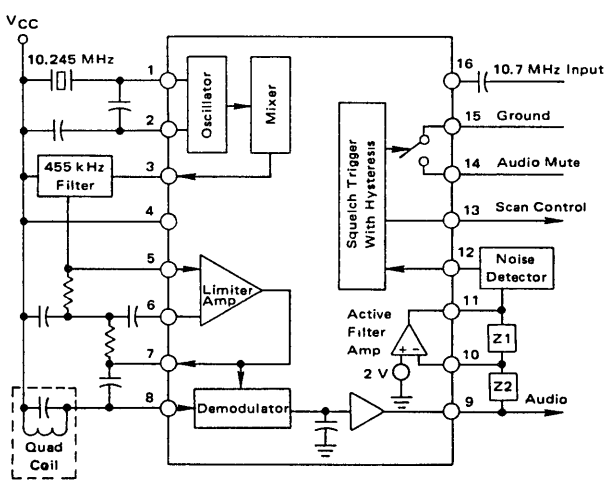
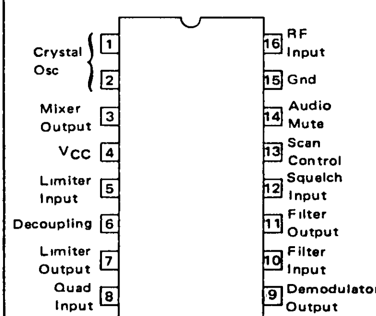
CASE 648

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



This is advance information and specifications are subject to change without notice

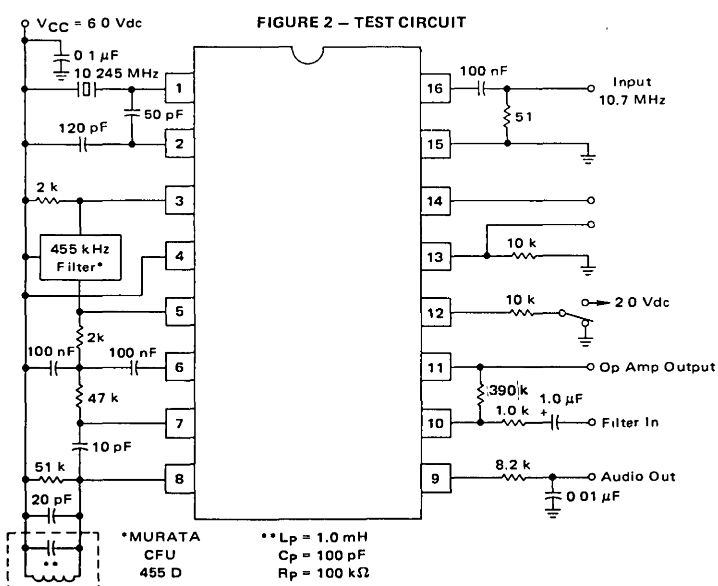
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	$V_{CC}(max)$	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	–	1.0	Vp-p
Input Voltage (V_{CC} ≥ 6.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	-0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	-30 to +70	°C
Storage Temperature Range	–	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, fo = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current	4				mA
Squelch Off		–	2.0	–	
Squelch On		–	3.0	5.0	
Input Limiting Voltage (-3 dB Limiting)	16	–	5 0	10	μV
Detector Output Voltage	9	–	3.0	–	Vdc
Detector Output Impedance	–	–	400	–	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	200	350	–	mVrms
Filter Gain (10 kHz) (V_{in} = 5 mV)	–	40	46	–	dB
Filter Output Voltage	11	1.8	2 0	2 5	Vdc
Trigger Hysteresis	–	–	100	–	mV
Mute Function Low	14	–	15	50	Ω
Mute Function High	14	1.0	10	–	MΩ
Scan Function Low (Mute Off) (V_{12} = 2 Vdc)	13	–	0	0 5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	5.0	–	–	Vdc
Mixer Conversion Gain	3	–	20	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

FIGURE 2 — TEST CIRCUIT



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer-oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly-balanced to reduce spurious responses. The input impedance at pin 16 is set by a 3 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at pin 3 must be dc connected to B+, below which it can swing 0.5 V.

After suitable bandpass filtering (ceramic or LC) the signal goes to the input of a five-stage limiter at pin 5. The output of the limiter at pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at pin 7 is also used to supply dc feedback to pin 5. The other side of the first limiter stage is decoupled at pin 6.

The recovered audio is partially filtered, then buffered giving an impedance of around 400 Ω at pin 9. The signal still requires de-emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at pin 11 providing dc bias (externally) to the input at pin 10 which is referred internally to 2 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to pin 12.

An external positive bias to pin 12 sets up the squelch trigger circuit such that pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (pin 14) is open circuit. If pin 12 is pulled down to 0.7 V by the noise or tone detector, pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 μA and pin 14 is internally short-circuited to ground. There is 100 mV of hysteresis at pin 12 to prevent jitter. Audio muting is accomplished by connecting pin 14 to a high-impedance ground-reference point in the audio path between pin 9 and the audio amplifier.

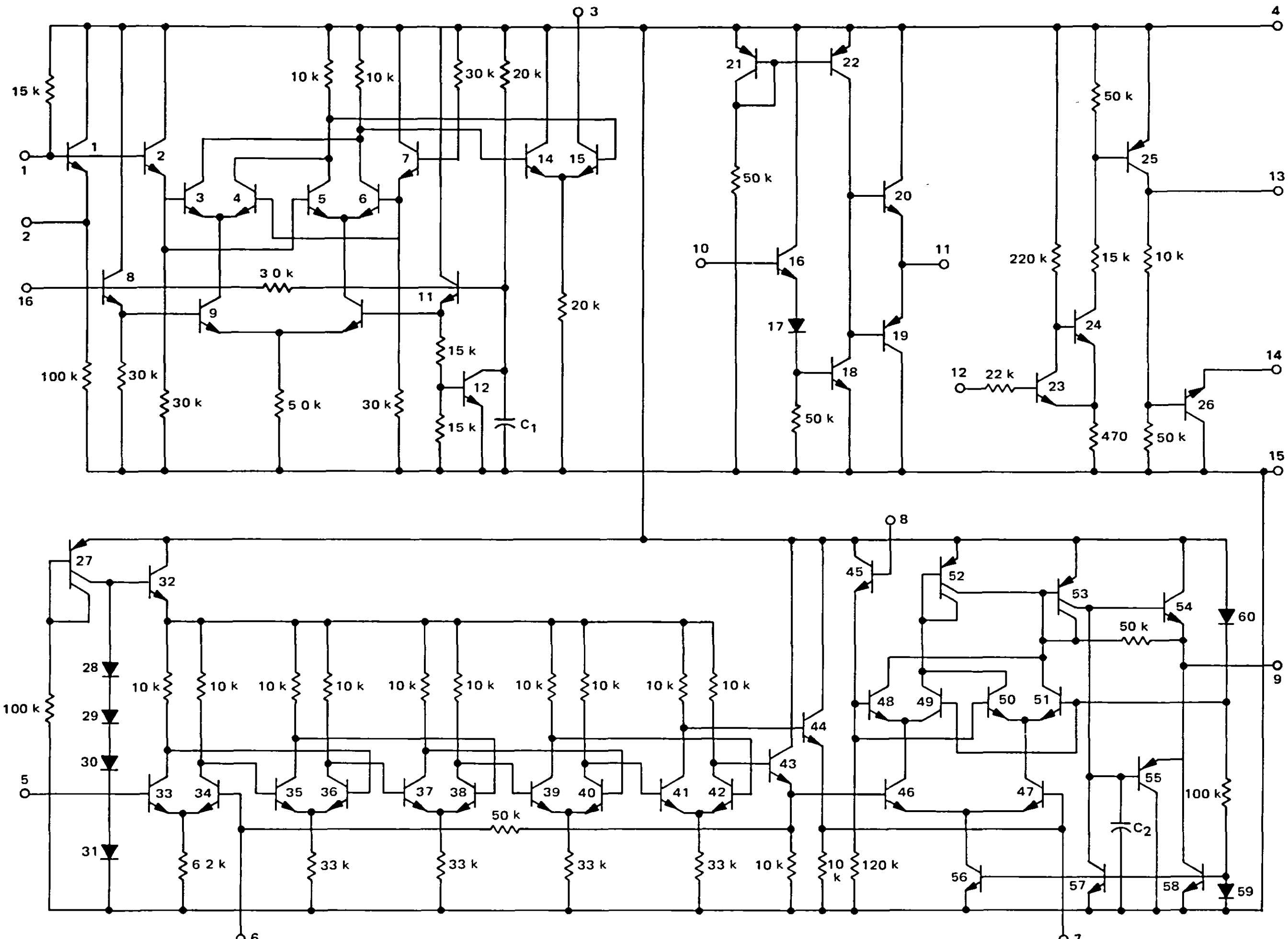


FIGURE 3 — CIRCUIT SCHEMATIC

ORDERING INFORMATION

Device	Temperature Range	Package
MC3360P	−10°C to +75°C	Plastic DIP

MC3360P

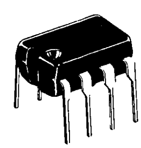
1/4-WATT AUDIO AMPLIFIER

. . . designed for the output stage of battery-powered portable radios.

- 250 mW of Audio Output Power
- Low Standby Current – 3.5 mA typical
- Low Harmonic Distortion
- Reduces Component Count in Portable Radios
- Formerly MFC4000B Packaged in Plastic Case 206A.

1/4-WATT AUDIO AMPLIFIER

SILICON MONOLITHIC FUNCTIONAL CIRCUIT

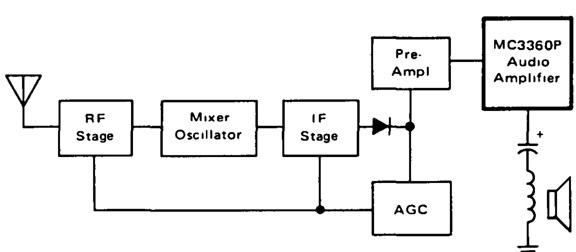


PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	12	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	1.2 10	Watts mW/°C
Operating Ambient Temperature Range	-10 to +75	°C

TYPICAL APPLICATION

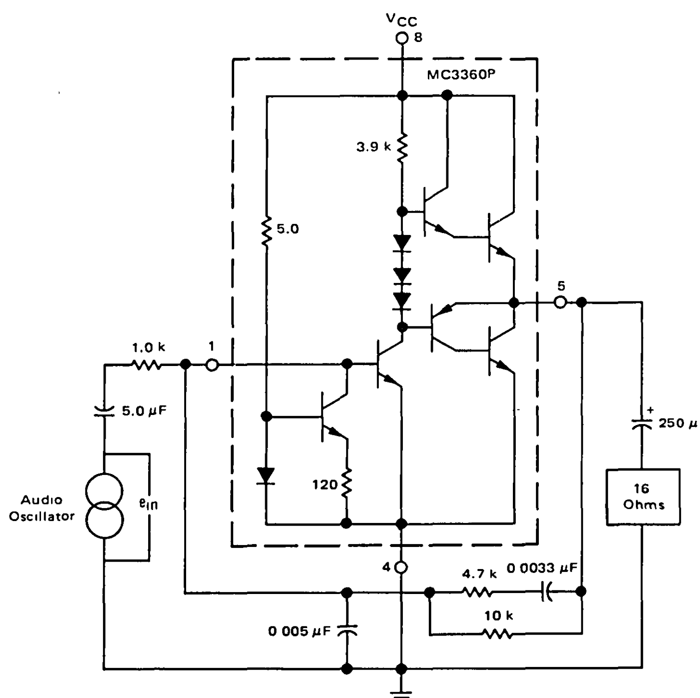


ELECTRICAL CHARACTERISTICS* (V_{CC} = 9.0 Vdc, R_L = 16 Ohms, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Zero Signal Current Drain	–	3 0	5 0	mAdc
Sensitivity P_O = 250 mW(RMS)	–	–	240	mV(RMS)
Output Power Total Harmonic Distortion ≤ 10%	250	350	–	mW(RMS)
Total Harmonic Distortion P_O = 50 mW(RMS) P_O = 50 mW(RMS), V_{CC} = 6 0 Vdc	 – –	 0 7 4 5	 – –	%

*As measured in test circuit shown in Figure 1

FIGURE 1 — TEST CIRCUIT



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TOTAL HARMONIC DISTORTION versus OUTPUT POWER

FIGURE 2 – V_{CC} = 9.0 Vdc

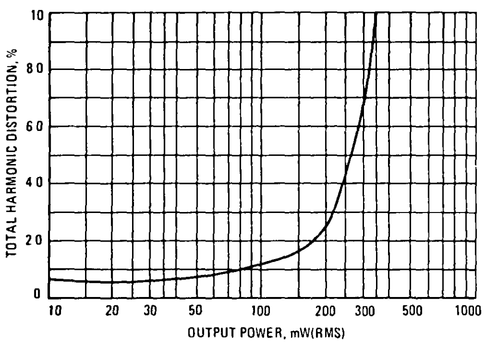


FIGURE 3 – V_{CC} = 6.0 Vdc

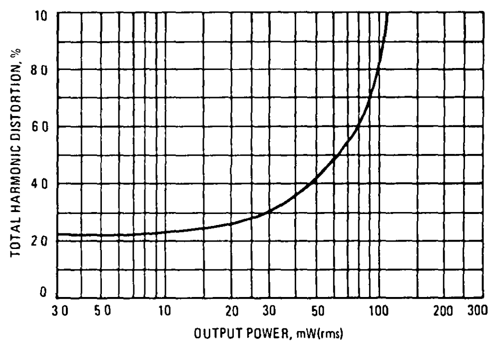


FIGURE 4 – CURRENT DRAIN versus OUTPUT POWER

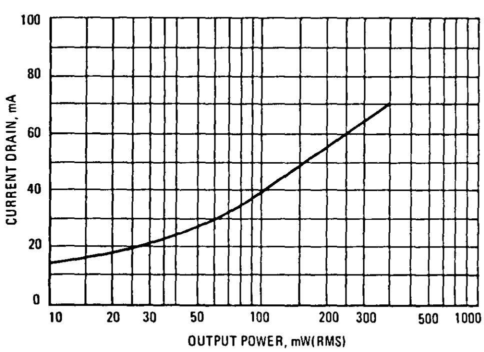


FIGURE 5 – TOTAL HARMONIC DISTORTION versus SUPPLY VOLTAGE

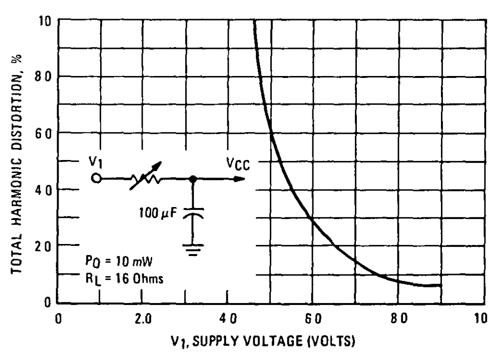
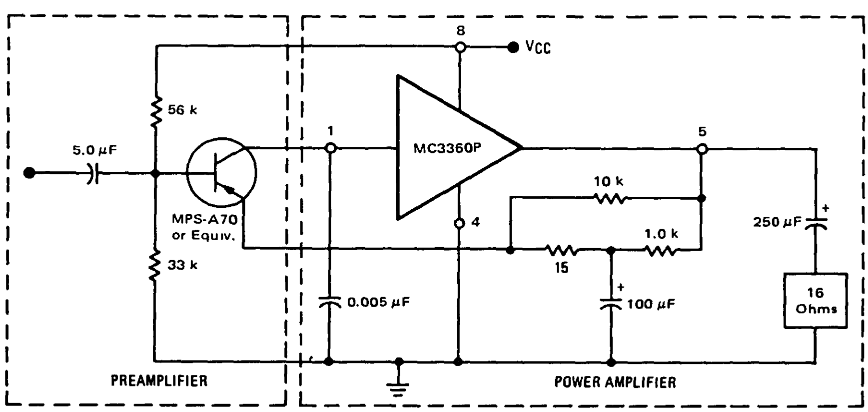


FIGURE 6 – TYPICAL CIRCUIT APPLICATION



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ORDERING INFORMATION

Device	Temperature Range	Package
MC3380P	0°C to +75°C	Plastic DIP

MC3380P

EMITTER COUPLED ASTABLE MULTIVIBRATOR
With Programmable Pulse Width and Current-Controlled Pulse Repetition Rate

The MC3380P is a monolithic device designed for use as a general building block in control and power supply applications.

Its extremely flexible design makes it useful in dc-dc converter applications and power supply regulator circuits. Its fixed pulse width, variable frequency mode of operation makes it useful in switching regulator applications with either fixed or variable loads. This device is capable of stepping up (Figures 5 and 9) or stepping down (Figure 14) dc input voltages, and can produce regulated multiple output dc voltages of either positive or negative polarity (Figure 14).

This device can also be used as a frequency source when configured as a multivibrator.

- As a DC-DC Converter —
  - Differential Line Regulation (Figure 9) — = 1 V (Max) @ V_{CC} = 3 to 7.5 V
- As a Power Regulator —
  - Load Regulation (Figure 5) — 0.2% (Typ) @ P_D = 1 to 3 Watts
- As a Multivibrator —
  - High Toggle Frequency = 100 kHz (Typ)

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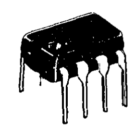
EMITTER COUPLED ASTABLE MULTIVIBRATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

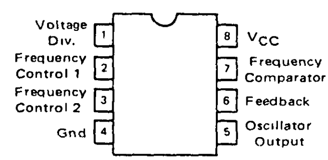
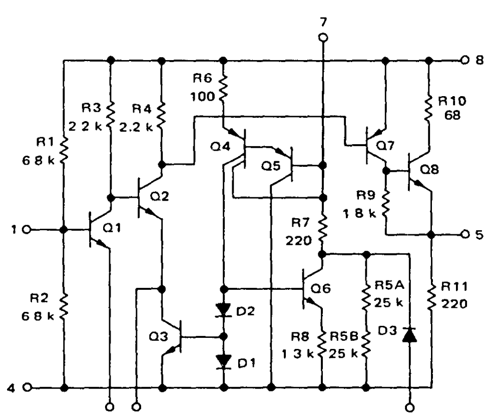


FIGURE 1 — CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Output Current - Pin 8	I_O	100	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 3 0	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 Vdc, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
EMITTER-COUPLED ASTABLE MULTIVIBRATOR					
Rise Time (C = 0.0034 μF, R1 = R2 = 10 kΩ, f = 100 kHz, Figure 4)	t_r	–	12	–	ns
Fall Time (C = 0.0034 μF, R1 = R2 = 10 kΩ, f = 100 kHz, Figure 4)	t_f	–	45	–	ns
Toggle Frequency (C = 0 002 μF, R1 = R2 = 10 k, Figures 2, 3, 4)	–	–	100	–	kHz
3-WATT REGULATOR					
Power Efficiency (Figure 5) (V_O = 200 Vdc @ 15 mAdc)	–	–	60	–	%
Load Regulation (Figure 5) (P_{out} < 3 0 W)	Reg_{load}	–	0 2	–	%
Line Regulation (Figure 5) (V_{CC} = 4 0 -6.0 Vdc)	Reg_{line}	–	0 3	–	%
Output Voltage (Figure 5)	V_O	–	200	–	V
Output Current (Figure 5)	I_O	–	15	–	mA
Supply Voltage (Figure 5)	V_{CC}	3 0	–	10	V
Supply Current (Figure 6) (I_{FB} = 0, R_L = ∞)	I_D	–	20	30	mA
Output Voltage High (Figure 6) (I_O = 2.0 mA, I_{FB} = 250 μA) (I_O = 25 mA, I_{FB} = 250 μA)	V_{OH}	 2.4 1 2	 3.5 1 5	 – –	V
Output Voltage Low (Figure 6) (I_O = -1 0 mA, I_{FB} = 600 μA)	V_{OL}	–	150	300	mV
Rise Time (Figure 7)	t_r	–	12	–	ns
On Time (Figure 7)	t_{on}	–	20	–	μs
Fall Time (Figure 7)	t_f	–	45	–	ns
Off Time (Figure 7)	t_{off}	–	20	–	μs
DC - DC CONVERTER					
Zener Bias Current (Figure 10) (V_{CC} = 5.0 Vdc, V_O > 2.4 Vdc) (V_{CC} = 5.0 Vdc, V_O < 0.4 Vdc)	 I_{FB1} I_{FB2}	 – 600	 – –	 250 –	 μA μA
Output Current (Figure 11) (V_{CC} = 5.0 Vdc)	I_{OH}	25	35	–	mA
Output Resistance (Figure 12) (V_{CC} = 5.0 Vdc, I_O = -1.0 mA)	r_o	150	220	300	Ω
Shutdown Voltage (Figure 13) (V_O < 0.5 V)	V_{CC}	–	–	1.6	V
Supply Voltage (Figure 9)		3.0	–	7.0	V
Differential Line Regulation (Figure 9) (ΔV_{CC} = 3 0 to 7.0 Vdc)	ΔV_{reg}	-1.0	–	+1 0	V
Feedback Voltage (Figure 9) (V_{CC} = 5.0 Vdc)	V_F	0.6	–	1.1	V
Voltage Efficiency (Figure 9) (V_{CC} = 5.0 Vdc, Eff(%) = (V_{out}^2/(3.3 k) (I_{CC}) (V_{CC}))	–	40	–	–	%

5

FIGURE 2 – TYPICAL CAPACITANCE versus FREQUENCY

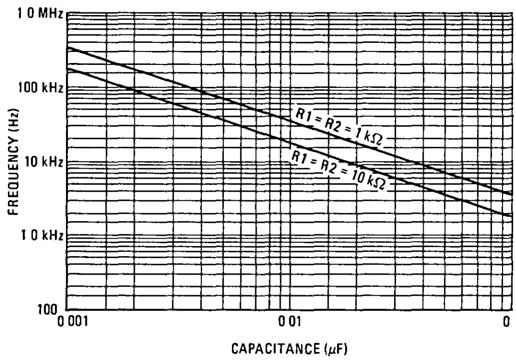


FIGURE 3 – TYPICAL DUTY CYCLE and FREQUENCY CHARACTERISTICS

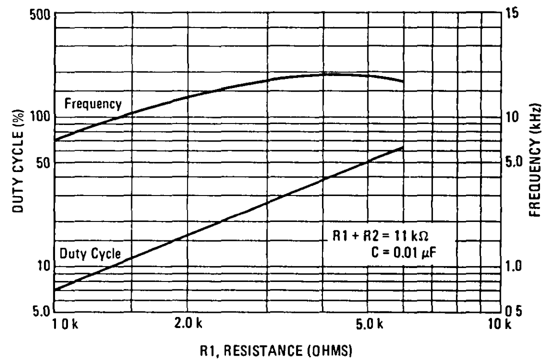


FIGURE 4 – ASTABLE MULTIVIBRATOR TEST CIRCUIT

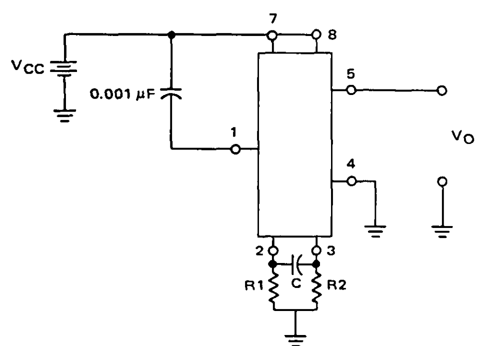
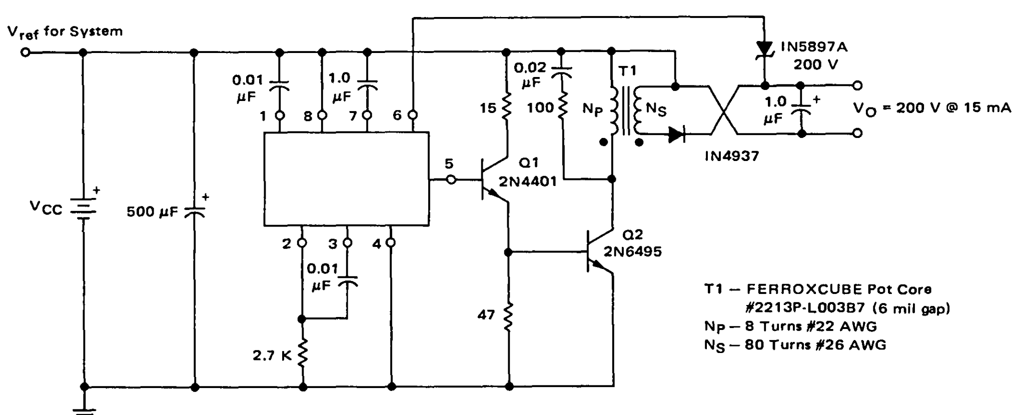


FIGURE 5 – 3-WATT SWITCHING REGULATOR APPLICATION CIRCUIT



3-Watt Switching Regulator - converts 5 V to 200 V for gas discharge displays such as Burroughs Panaplex and Beckman.

FIGURE 6 – STATIC TEST CIRCUIT

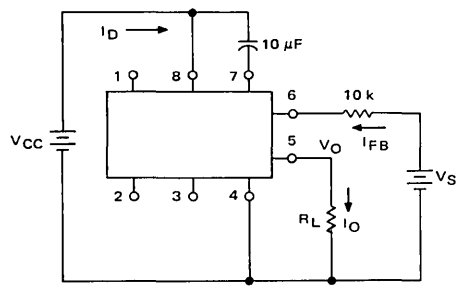


FIGURE 7 – DYNAMIC TEST CIRCUIT

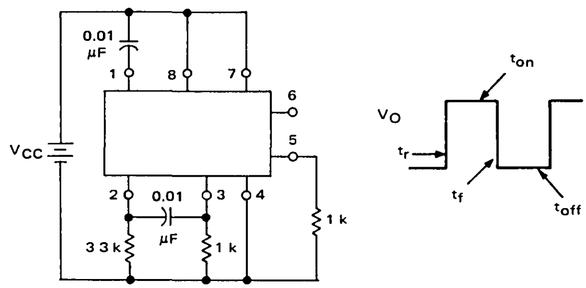


FIGURE 8 – SWITCHING WAVEFORMS AT Q2

Collector Current and Voltage Waveforms of 2N6495 (Q2) From Figure 5

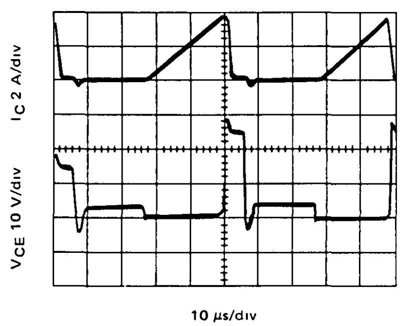
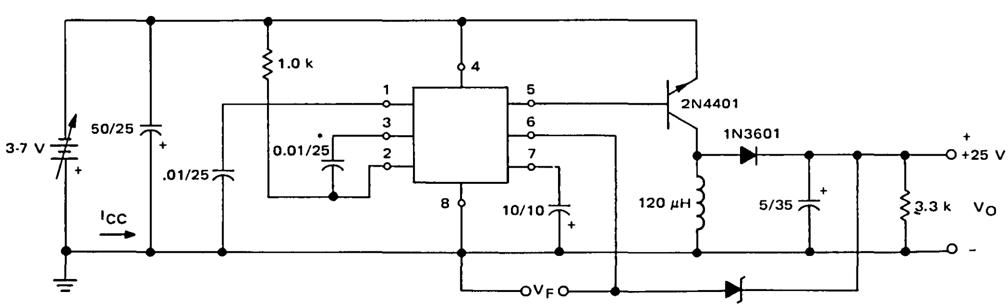


FIGURE 9 – TYPICAL APPLICATION IN 3 - 25 V
DC-DC CONVERTER CONFIGURATION



Notes
1. All resistor values in ohms, ± 1%, 1/4 W
2. All capacitor values in µF, = 20%, except • ± 5%.
3. All inductors ± 4%.

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DC - DC CONVERTER TEST CIRCUITS

FIGURE 10 – ZENER BIAS CURRENT TEST

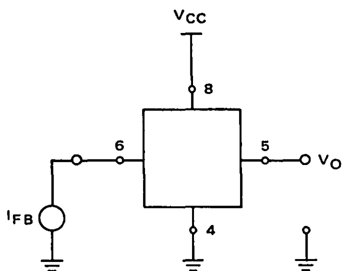


FIGURE 11 – OUTPUT CURRENT TEST

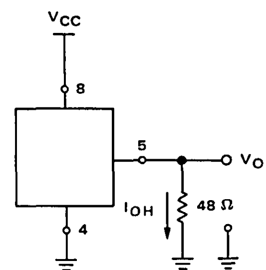
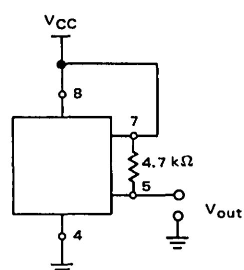


FIGURE 12 – OUTPUT RESISTANCE TEST



(Note: $r_O = \frac{V_{out}}{1\ mA}$)

FIGURE 13 – SHUTDOWN VOLTAGE AND TEST
(NOTE: Decrease V_{CC} until V_O < 0.5 V)

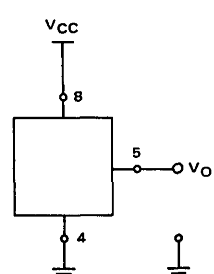
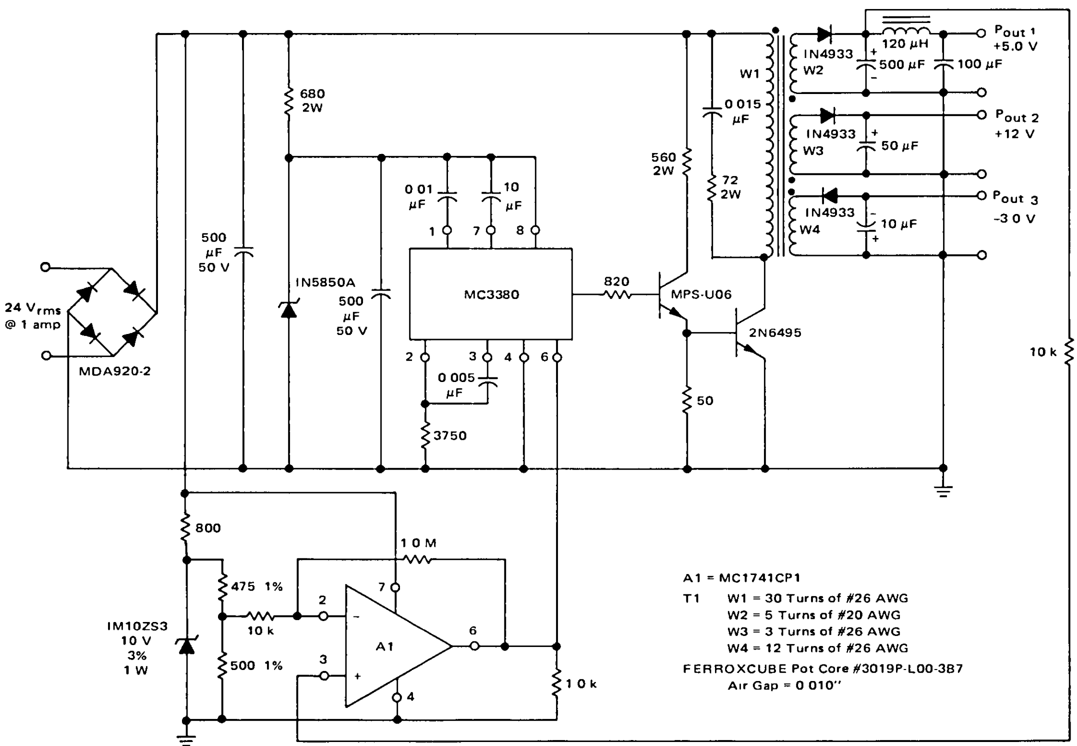


FIGURE 14 – TYPICAL APPLICATION AS MULTIPLE OUTPUT SWITCHING REGULATOR FOR USE WITH MPU'S



TYPICAL PERFORMANCE

P_{out1} = 4 Watts
(V_O = 5 V ± 5%)

5 V Ripple Component = 50 mV
(120 Hz + 20 kHz)

P_{out2} = 600 mW
(V_O = 12 V ± 10%)

P_{out3} = 3 mW
(V_O = -3 V ± 10%)

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MC3393P

Advance Information

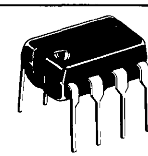
TWO MODULUS PRESCALER

The MC3393P can divide by 15 and 16, and can be used with Motorola CMOS frequency synthesizers MC145146, 52, 56 for commercial AM-FM radio, land mobile and marine two-way radios, avionic radios, and scanner receivers.

- 140 MHz (typ) Toggle Frequency
- ÷15/16
- TTL and CMOS Compatible Output
- Active Pullup and Pulldown
- +5.0 V Supply
- Buffered Clock Input
- 100-400 mV (typ) Input Sensitivity
- 200 Milliwatts (typ)

TWO MODULUS PRESCALER

SILICON MONOLITHIC INTEGRATED CIRCUIT



N SUFFIX
PLASTIC PACKAGE
CASE 626

FIGURE 1 — LOGIC DIAGRAM

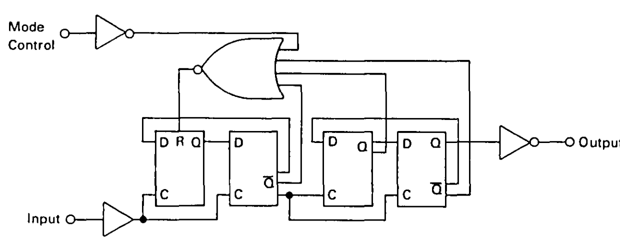
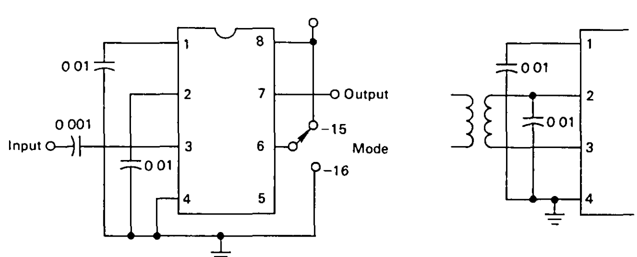


FIGURE 2 — TEST CIRCUITS



Capacitor Coupled Input

Link Coupled Input

Pin Outs
1 Bias Decouple
2 Bias Decouple
3 Input
4 Ground
5 NC
6 Input
7 Output
8 V_{CC}

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6.0	Vdc
Input Mode Control Voltage	V_{ICR}	10	Vdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PRELIMINARY ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = +5 0 Vdc, T_A = 25°C, f_{in} = 100 MHz)

Characteristics	Min	Typ	Max	Units
Power Supply Voltage	4 5	—	5 5	Vdc
Current Drain	—	40	—	mA
Input Voltage	100	—	400	mV(rms)
Input Impedance Real Part Capacitance	— —	900 6 0	— —	Ohms pF
Mode Control Voltage for 15 Count	2 7	—	10	Vdc
Mode Control Voltage for 16 Count	0	—	0 8	Vdc
Output High at 30 μA Source	2 7	4 3	—	Vdc
Output Low at 1 6 mA Sink	—	0 3	0 8	Vdc
Propagation Delay Time	—	25	—	ns
Set up Time (16 to 15 Count) Measured before Rising Edge of Clock on Count 15	—	20	—	ns
Release Time (15 to 16 Count) Measured before Falling Edge of Clock Preceding Count 15	—	15	—	ns
Thermal Resistance, $R_{\theta JC}$	—	100	—	°C/W

MCCF3326

Advance Information

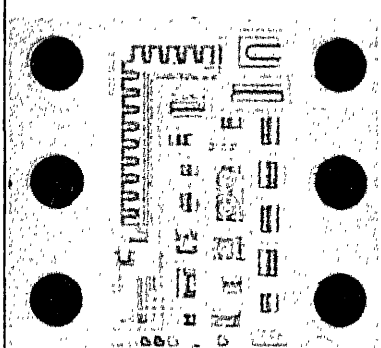
AUTOMOTIVE VOLTAGE REGULATOR FLIP-CHIP

. . . designed for use in conjunction with an NPN Darlington transistor in a floating field alternator charging system.

- Overvoltage Protection
- Shut Down on Loss of Battery Sense
- Adjustable Temperature Coefficient

FLIP-CHIP AUTOMOTIVE VOLTAGE REGULATOR

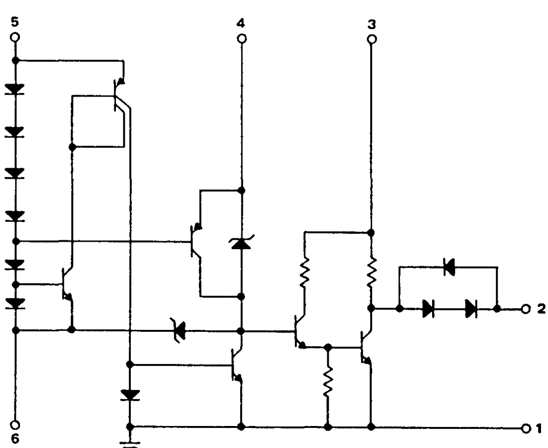
SILICON MONOLITHIC INTEGRATED CIRCUIT



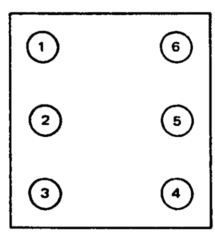
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Current Into Pin 5	I_5	50	mA
Current Into Pin 4	I_4	20	mA
Current Into Pin 3	I_3	120	mA
Current Into Pin 6	I_6	50	mA
Current Into Pin 2	I_2	50	mA
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



SOLDER BUMP CONNECTIONS



1 – GND
2 – Output
3 – Output Drive Adjust
4 – Overvoltage Sense and Battery Sense Loss Detect
5 – Battery Sense
6 – Diode TC Adjust

This is advance information and specifications are subject to change without notice.

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MCCF3326

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Diode TC Adjust (Threshold Voltage on Pin 6)	1	V_6	7.9	–	8.8	V
Battery Sense (Threshold Voltage on Pin 5)	1	V_5	11.8	–	13.3	V
Overvoltage Sense and Battery Sense Loss Detect (Threshold Current Into Pin 4)	2	I_4	–	–	600	μA
Overvoltage Sense and Battery Sense Loss Detect (Threshold Voltage at Pin 4, $I_4 \leq 400\ \mu A$)	2	V_4	7.4	–	9.7	V
Output Drive Adjust (Voltage Drop from Pin 3 to Pin 2, I_3 = 10 mA)	3	V_3	1.4	–	2.0	V
Low State Output Voltage at Pin 2 (I_4 = 12 mA, I_3 = 120 mA)	4	V_2	–	–	0.7	V

TEST CIRCUITS

FIGURE 1

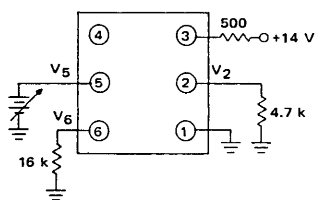


FIGURE 2

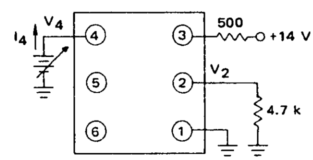


FIGURE 3

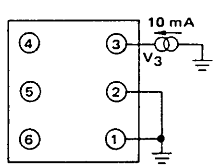
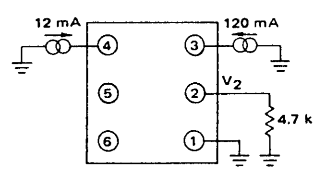


FIGURE 4



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APPLICATIONS CIRCUIT INFORMATION

R1 Determines the temperature coefficient by setting the value of current in the diode string. As the value of R1 decreases, so does the effective TC. R1 should be chosen so that the current in the diode string is between 0.5 mA and 1.0 mA.

R5 This resistor determines the V_{reg} voltage as approximated by the following equation:

$$V_{reg} \cong (1 + \frac{R5}{R1})\, 8.4 + n(0.7)$$

n = number of diodes used in diode string = 6

R4 Used as a current limiting resistor on pin 4 in case of overvoltage at the diode trio, or an open battery voltage sense lead. Voltage at pin 4 will run approximately 8.6 volts. R4 should be chosen so that the current (I_4) at maximum overvoltage is between 2 mA and 6 mA.

R3 This resistor determines the output drive current. Refer to specifications for the Darlington driver and select the value for R3 that will provide enough drive to the output when the diode trio voltage is at a minimum.

$$I_{Drive} \cong \frac{V_{min} - 2.8\ V}{R3 + 10\ \Omega}$$

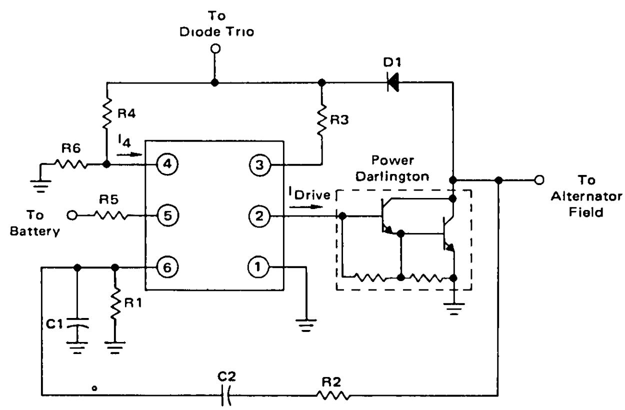
R6 This resistor in conjunction with R4 is used to set the maximum overvoltage

$$\text{Maximum Overvoltage} = \frac{R4 + R6}{R6}\ (8.6)$$

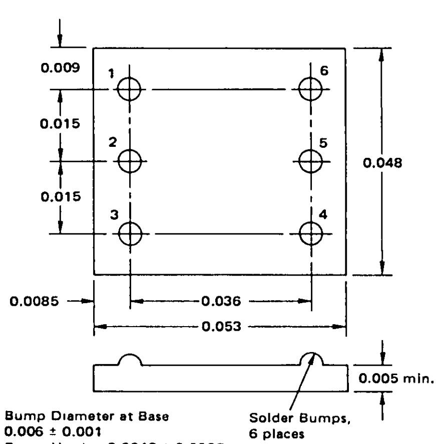
R2 Used for compensation (Approximately 3 kΩ)

C1, C2 Used for compensation (Approximately 0.01 µF)

FIGURE 5 – APPLICATIONS CIRCUIT



BONDING DIAGRAM AND DEVICE DIMENSIONS



PACKAGING AND HANDLING

The flip-chip consists of a silicon chip with solder bumps on the geometry surface to provide easy mechanical mounting and electrical connection. These devices are protected by a thin layer of phosphorsilicate passivation which covers the interconnect metalization and active areas of the die.

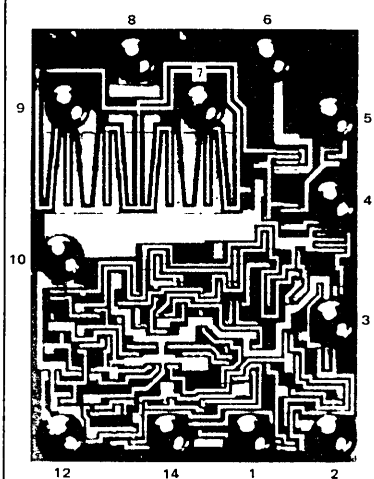
Care must be exercised when removing the dice from the shipping carrier to avoid scratching the solder bumps. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCCF3333

VARI-DWELL IGNITION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

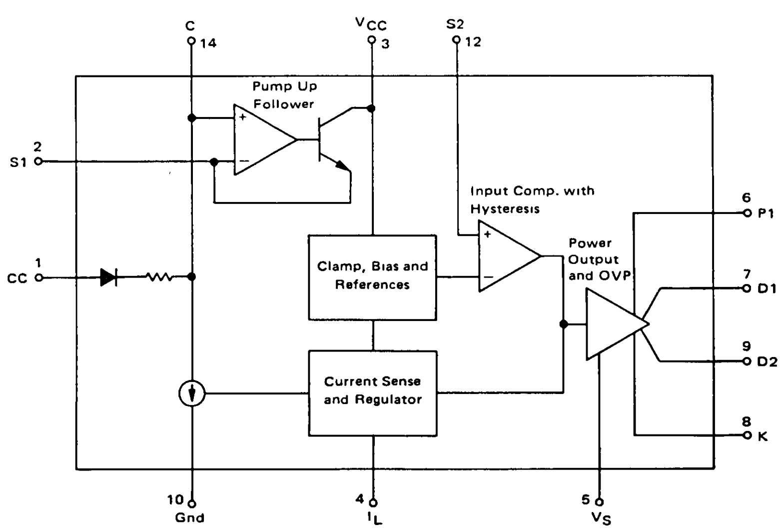


FLIP-CHIP VARI-DWELL IGNITION CIRCUIT

. . . designed for use in conjunction with a flux averaging sensor and a high energy ignition coil to provide regulated current pulses to the coil from information supplied by the sensor.

- Wide Supply Voltage Operating Range (4 to 24 V)
- Externally Adjustable Overvoltage Shutdown
- Externally Adjustable Dwell Time and Spark Energy
- Extremely Stable Output Current Pulses
- Variable Input Threshold Compensates for Low Supply Voltage Conditions
- Low Static Current Drain
- Also Available in Plastic Package (MC3333P) and Standard Chip (MCC3333) Form

FIGURE 1 – BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage Steady State (Through 400 Ω, see Figure 2) Transients of 300 ms or less	V_{CC}	24 90	Vdc
Peak Output Sink Current Transients of 300 ms or less	$I_{S(PEAK)}$	1.3	A
Junction Temperature Range	T_J	-65 to +150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 5 V, T_A = 25°C unless otherwise specified; Figure 2)

Characteristic	Symbol	Pin(s) Under Test	S1	S2	S3	S4	S5	S6	Min	Typ	Max	Unit
Current Drain	I_D	3	A	A	A	A	A	A	8 0	15	25	mA
Pre-Driver On	V_{P1}	6	A	A	A	A	A	A	–	90	2 0	V
D1, D2 Output On	$V_{D1, D2}$	7&9	A	A	A	A	A	A	–	110	500	mV
Kelvin Contact	V_K	8	A	A	A	A	A	A	–	40	200	mV
CC Charge Circuit	V1	1	B	A	A	A	A	E	700	800	900	mV
S1 Follower	V_{S1}	2	A	B	A	A	A	C	1.4	1 6	1 8	V
C Clamp High	V_c	14	A	A	A	A	A	D	–	8 4	8 8	V
S2 Turn On (measure V_{S2} ramp value at P1 switch point)	V_{S2}	12	A	A	A	A	B	A	1.6	1.9	2 1	V
Overvoltage Protection	V_S	5	A	A	A	B	C	A	8 0	9 1	10	V
Current Limit Trip	V_{IL}	4	A	A	B	A	C	B	150	180	220	mV

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FIGURE 2 – TEST CIRCUIT

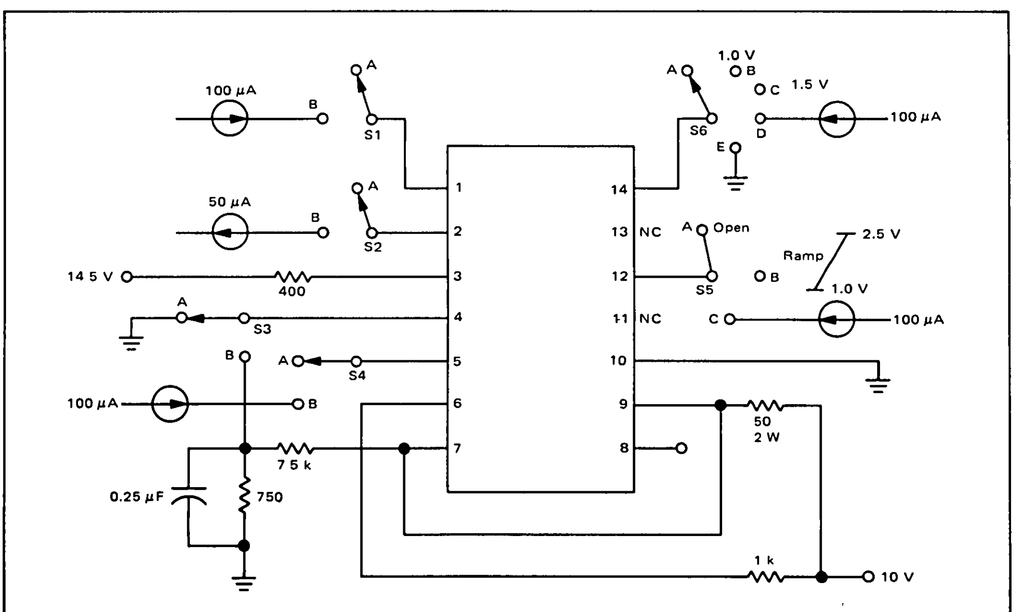
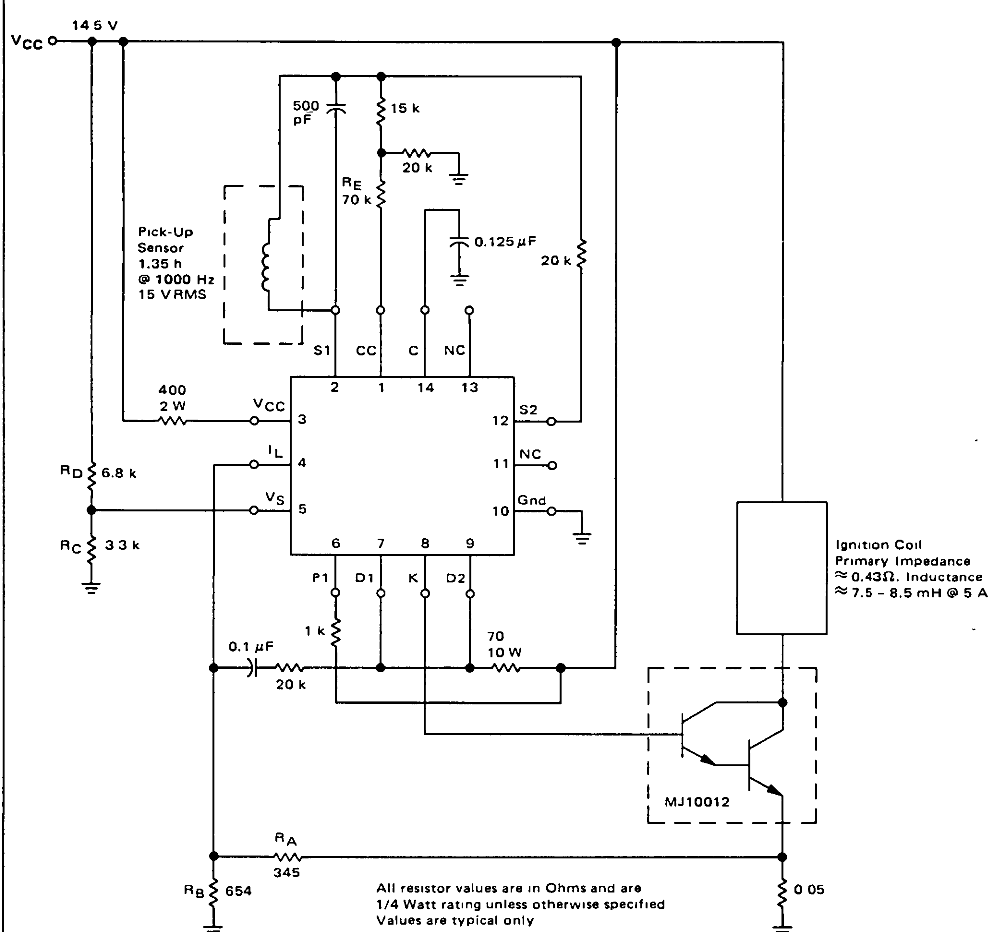


FIGURE 3 — TYPICAL APPLICATION CIRCUIT



Notes

1. The ratio of R_A to R_B controls the ignition coil regulated current:

$$I_{COIL} \approx 3.6 \left(\frac{R_A + R_B}{R_B}\right) \qquad R_A + R_B \approx 1\ k\Omega$$

2. The ratio of R_D to R_C sets the over-voltage shutdown point with respect to B+.

$$B+_{overvoltage} \approx 8 \left(\frac{R_C + R_D}{R_C}\right) \qquad R_C + R_D \approx 10\ k\Omega$$

3. R_E is active region dwell control. R_E = 70 kΩ results in output current limit time of approximately 10% at 1000 RPM (with respect to one distributor cycle in an 8 cylinder engine). Values less than 70 kΩ lengthen this limit time and values higher shorten this limit time.
4. The 0.1 µF capacitor at pin 4 may be eliminated and stability maintained. A readjustment of the R_A and R_B resistors will be required.

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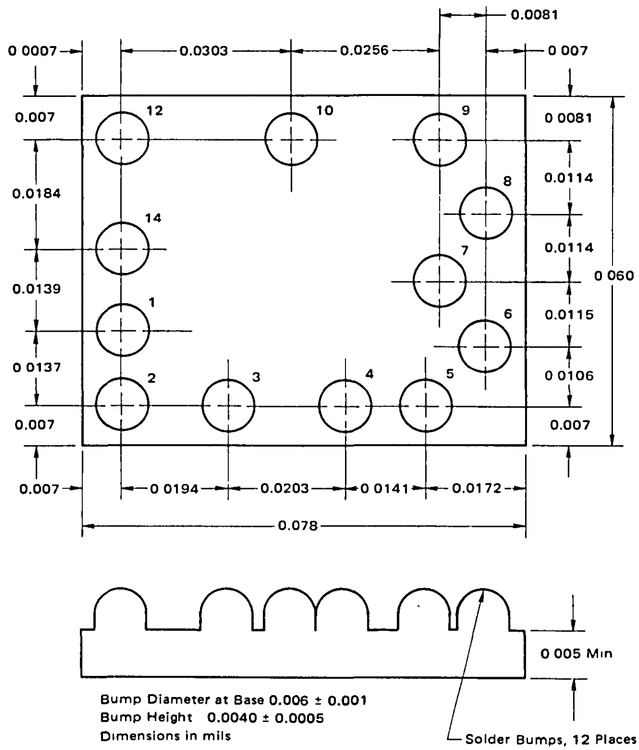
MCCF3333
BONDING DIAGRAM AND DEVICE DIMENSIONS



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PACKAGING AND HANDLING

The flip-chip consists of a silicon chip with solder bumps (90-10 solder on a chrome-copper-gold base) on the geometry surface to provide easy mechanical mounting and electrical connection. These devices are protected by a thin layer of phosphorsilicate passivation which covers the interconnect metallization and active areas of the die.

Care must be exercised when removing the dice from the shipping carrier to avoid scratching the solder bumps. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Dice are placed in the carrier with geometry side up.

TCA4500A

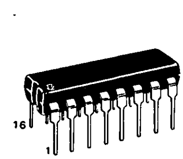
Advance Information

FM STEREO DEMODULATOR
DESIGNED FOR USE IN HI-FI STEREO RECEIVERS AND CAR RADIOS

- Wide Supply Range: 8 – 16 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range (Fixed or Adjustable)
- Variable Blend Control
- Low Distortion: 0.3% THD at 2.5 Vp-p Composite Input Signal
- Excellent Rejection of ARI Subcarrier (57 kHz)
- Excellent Rejection of Pilot Tone Harmonics including 114 kHz
- Wide Dynamic Range: 0.5 – 2.5 Vp-p Composite Input Signal
- Up to 6 dB Gain (Monaural)
- Low Output Impedance
- Transient-free Mono/Stereo Switching
- 50 dB Supply Ripple Rejection
- Integrated Stereo/Monaural Switch – 100 mA Lamp Driving Capability
- Requires No Inductors

FM STEREO DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

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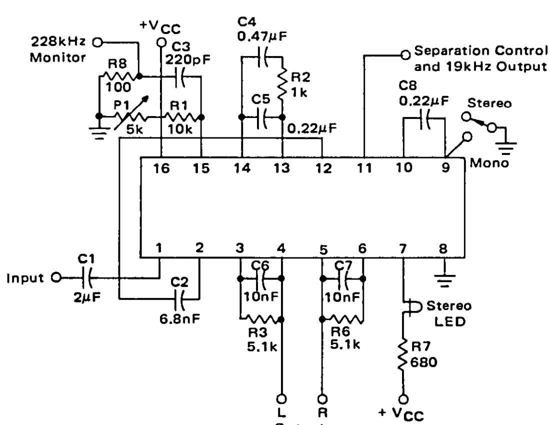
FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT



PIN FUNCTIONS

1 – Input
2 – Preamplifier output
3 – Left amplifier input
4 – Left channel output
5 – Right channel output
6 – Right amplifier input
7 – Stereo indicator Lamp
8 – Ground
9 – Stereo switch filter
10 – Stereo switch filter
11 – 19 kHz output/blend
12 – Modulator input
13 – Loop filter
14 – Loop filter
15 – Oscillator RC network
16 – V_{CC}

This is advance information and specifications are subject to change without notice

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Volts
Power Dissipation (Package limitation) Derate above T_A = +25°C	1800 15	mW mW/°C
Operating Temperature Range (Ambient)	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
Lamp Drive Voltage (Max. voltage at pin 7 with lamp "off")	30	Volts
Lamp Current	100	mA
Blend Control Input Voltage (pin 11)	10	Volts

5

ELECTRICAL CHARACTERISTICS Unless otherwise noted V_{CC} = +12 Vdc, T_A = 25°C, 2 5 Vp-p standard multiplex composite signal with L or R channel only modulated at 1 0 kHz and with 10% pilot level, using circuit of Figure 1.

Characteristic	Min.	Typ.	Max.	Unit
Stereo Channel Separation Unadjusted Optimised on other channel[1]	30 40	– –	– –	dB
Monaural Voltage Gain[1]	0 8	1 0	1 2	
THD at 2.5 Vp-p Composite Input Signal at 1.5 Vp-p Composite Input Signal	– –	– 0.2	0 3 –	%
Signal/Noise Ratio RMS 20 Hz - 15 kHz	–	90	–	dB
Ultrasonic Frequency Rejection 19 kHz 38 kHz	– –	31 50	– –	dB
Stereo Switch Level (19 kHz input level for lamp "on") Hysteresis	12 –	16 6 0	20 –	mVrms dB
Quiescent Output Voltage Change with Mono/Stereo Switching	–	5 0	20	mVdc
Stereo Blend Control Voltage (pin 11) 3 dB Separation (see Fig 2) 30 dB Separation	– –	0.7 1.7	– –	V V
Minimum Separation (pin 11 at 0 V)	–	–	1 0	dB
Monaural Channel Imbalance (pilot tone off)	–	–	0.3	dB
ARI 57 kHz Pilot Tone Influence on THD[2]	–	–	0 5	%
Sub-carrier Harmonic Rejection 76 kHz 114 kHz 152 kHz	– – –	45 50 50	– – –	dB
Supply Ripple Rejection	–	50	–	dB
Input Impedance	–	50	–	KΩ
Output Impedance	–	100	–	Ω
Blend Control Current[1]	–	–	-300	µA
Capture Range	–	±5 0	–	%
Operating Supply Voltage	8.0	–	16	V
Current Drain (lamp off)	–	35	–	mA

Notes [1] See Applications Information and Circuit Description
[2] ARI Test – Input signal· 1.5 Vp-p standard composite signal, 1 kHz modulation added to a CW 50 mVrms signal at 57.3 kHz.

TYPICAL CHARACTERISTICS

Unless otherwise noted V_{CC} = +12 V, T_A = +25°C, Input Signal is Modulated L or R with 10% Pilot Level. (See Fig. 16.)

———— · High Loop Gain Circuit

— — — . Normal Circuit

FIGURE 2 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL

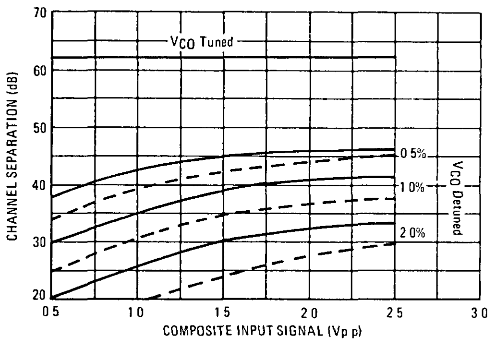


FIGURE 3 – V_{CO} FREE-RUNNING FREQUENCY versus TEMPERATURE

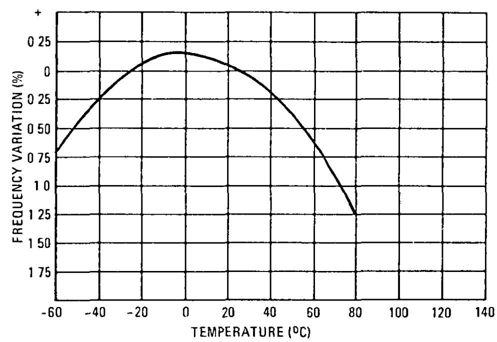


FIGURE 4 – STEREO SWITCH LEVEL versus V_{CO} FREE-RUNNING FREQUENCY

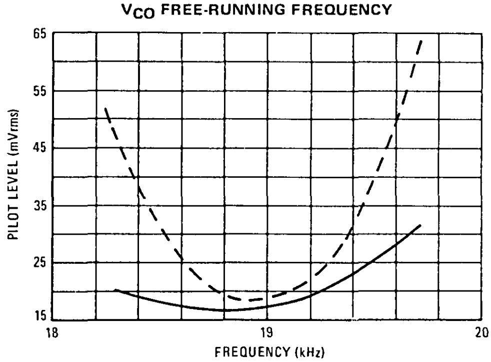


FIGURE 5 – SUPPLY RIPPLE REJECTION versus SUPPLY VOLTAGE

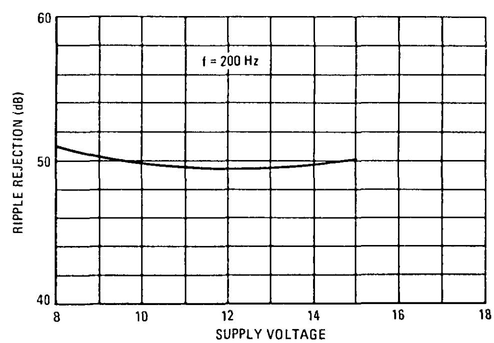


FIGURE 6 – THD versus COMPOSITE INPUT LEVEL

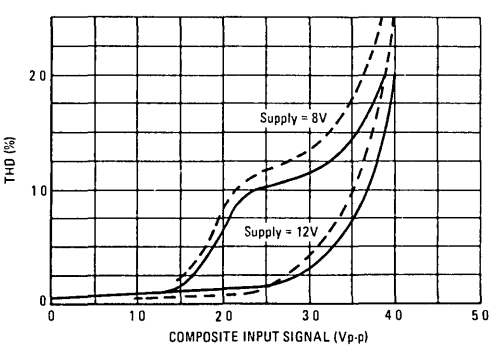


FIGURE 7 – CAPTURE and HOLDING RANGE WITH 20 mV PILOT LEVEL

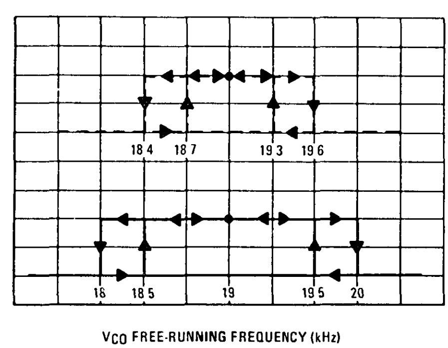


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FIGURE 8 — CHANNEL SEPARATION versus FREQUENCY

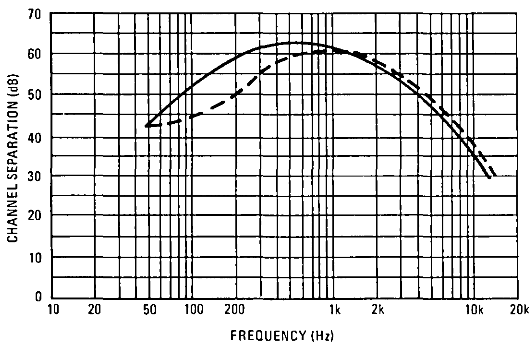


FIGURE 9 — THD versus FREQUENCY

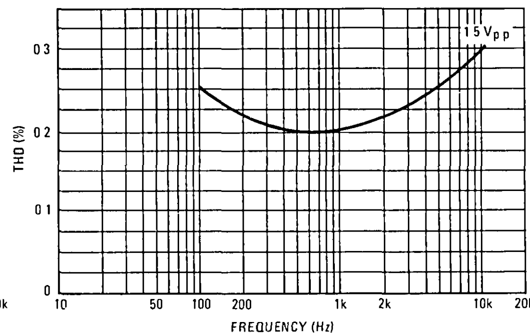
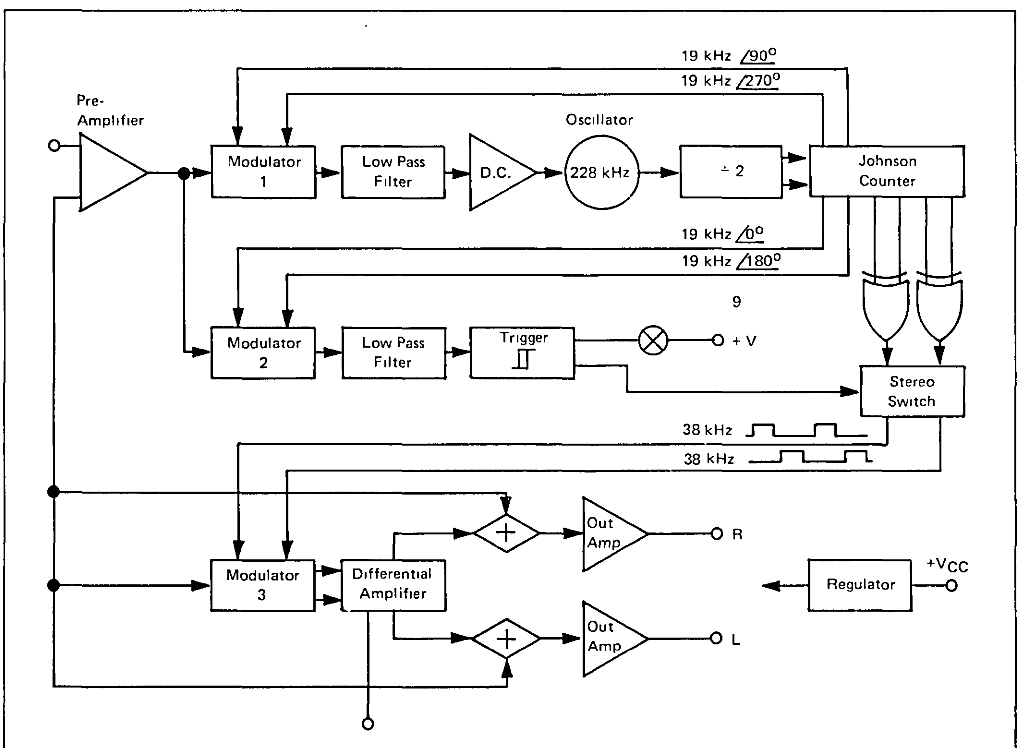


FIGURE 10 — SYSTEM BLOCK DIAGRAM



CIRCUIT DESCRIPTION

INTRODUCTION

The TCA4500A is a phase-lock-loop stereo decoder which incorporates a variable separation control, and in which sensitivity to the third harmonics of both the pilot and sub-carrier frequencies has been eliminated by the use of appropriate, digitally generated, waveforms in the phase-lock-loop and decoder sections.

The variable separation control may be operated manually, or by a receiver's AGC or S meter signals, to provide smooth transitions between monaural and stereo reception. It operates only during stereo reception: the circuit switches automatically to monaural if the 19 kHz pilot tone is absent.

The elimination of sensitivity to the third harmonic (114 kHz) of the sub-carrier (38 kHz) excludes interference from the 100 kHz (European Spacing) spaced side bands of adjacent transmitters, while elimination of sensitivity to the third harmonic (57 kHz) of the pilot tone (19 kHz) excludes interference from the ARI* system employed in Europe.

*Auto Radio Information.

CIRCUIT OPERATION

The block diagram of the circuit, shown in Fig. 10, consists of three sections: the phase-lock-loop, including the digital waveform generator: the stereo switch: and the decoder, in which the composite stereo signal is demodulated and matrixed to separate L and R channels.

In the phase-lock-loop the internal RC oscillator, operating at 228 kHz, feeds a 3 stage Johnson counter, via a binary divider, to generate a series of 19 kHz square waves. By the use of suitably connected NAND and EXCLUSIVE OR gates, the waveforms shown in Fig. 11, which are used to drive the various modulators in the circuit, are developed.

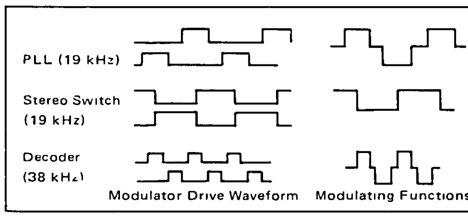
The use of such drive waveforms produces the modulating functions also shown in Fig. 11. The usual square-waveforms have been replaced in the PLL and decoder sections by 3-level forms which contain no third harmonic (actually no harmonics which are multiples of 2 or 3 are present). This eliminates the frequency translation of interference from these bands into the low frequency region. Such translation may produce audible components in the decoder section from the sidebands of adjacent channel FM signals, and may produce phase jitter, and consequent intermodulation distortion, in the PLL, from the modulated 57 kHz tones of the ARI system. The TCA 4500A is inherently free from these effects.

The stereo switch section is of conventional form (e.g. MC1310).

The decoder section consists of a modulator (driven by the waveforms shown in Fig. 11) whose outputs are the inverted and non-inverted channel difference signals. These signals pass to the output amplifiers via the variable blend circuit in which they are partially combined and hence mutually attenuated, according to the control voltage applied.

Matrixing occurs at the inputs of the output amplifiers, where the unmodified composite signal is added to the blended channel difference signals. The stereo separation may be progressively reduced from maximum to zero, dependent on the blending. The control law has been made non-linear, as the major redistribution of sound energy occurs at very low separation levels. For monaural, or very weak stereo signals, the modulator in the decoder section is disactivated by the stereo switch circuit. The variable separation control is thus, also, automatically disabled.

FIGURE 11 – DIGITAL WAVEFORM



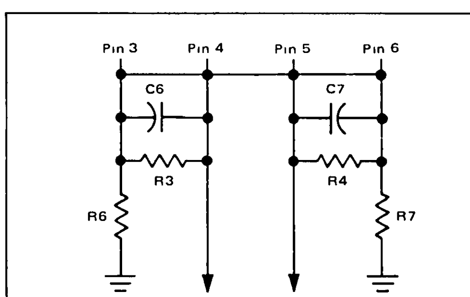
APPLICATION INFORMATION

GAIN AND DE-EMPHASIS

The gain and de-emphasis characteristics of the circuit are defined by shunt feedback via the external RC networks (R3, C6, R4, C7 of Fig. 1) around the output amplifiers. The gain is unity when resistors of 5.1 kΩ are used. Higher gains may be obtained by using networks of the form shown in Fig. 12.

The resistors R6, R7 are added to correct the output quiescent voltage levels which are optimized for R3, R4 = 5.1 kΩ and which would, if uncorrected, become too low with higher value resistors. Suitable network values are as follows:

FIGURE 12 – OUTPUT AMPLIFIER FEEDBACK NETWORKS



APPLICATION INFORMATION (continued)

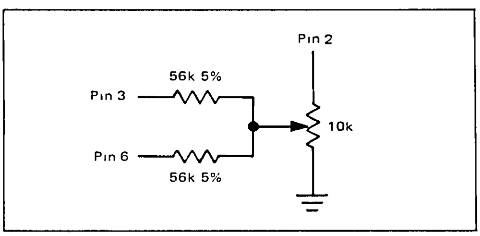
Gain (dB)	R3, R4	C6, C7		R6, R7
		50 µs	75 µs	
0	5.1kΩ	10 nF	15 nF	
3	6 8kΩ	6.8 nF	10 nF	47k ±10%
6	10k	4.7 nF	6 8 nF	27k ±10%

The maximum output level is 1 Vrms, consequently the max. input is limited to 1.4 Vp-p if the gain is set to 6 dB.

SEPARATION ADJUSTMENT

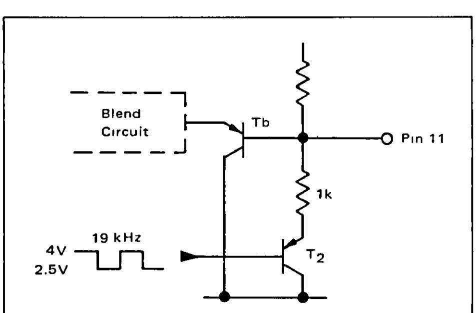
A separation adjustment may be added, as shown below, (Fig. 13), to compensate for the receiver's IF characteristics.

FIGURE 13 – NETWORK PROVIDING ADJUSTABLE SEPARATION



This network reduces the amplification of the channel sum signal in the decoder, to compensate the attenuation of the channel difference signal in the receiver's IF section. The network shown will compensate for up to 2 dB attenuation at 38 kHz. The decoder gain is, obviously, reduced by an amount equal to the compensation required. When used as described, the adjustment also corrects the inherent separation of the decoder, which may be optimized on one channel. Optimization of both channels is possible if separate potentiometers are used to feed each output amplifier.

FIGURE 14 – BLEND CONTROL INPUT CIRCUIT



VARIABLE SEPARATION (BLEND) CONTROL AND 19 kHz OUTPUT

To retain the 16-pin package, the blend control has been combined with the 19 kHz output on pin 11. The internal circuit providing this combination is shown in Fig.14.

If pin 11 is left open-circuit, the 19 kHz signal appears at a mean dc level of 4 V. The blend circuit is inoperative at this level and the decoder provides full separation. The 19 kHz signal can be used to tune the internal oscillator.

To reduce the separation, the voltage on pin 11 is lowered. At 3.2 V, T2 ceases conduction and the 19 kHz signal disappears.

At 2.3 V, the blend circuit comes into operation and the separation decreases according to the curve shown in Fig. 15.

FIGURE 15 – SEPARATION CONTROL VOLTAGE

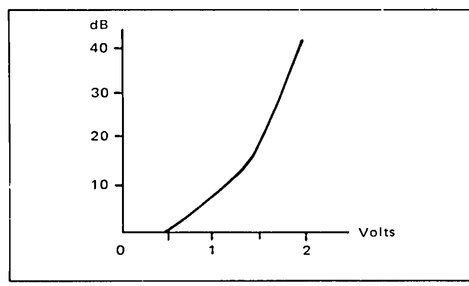
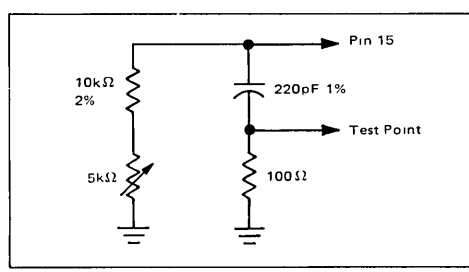


FIGURE 16 – OSCILLATOR NETWORK FOR DIRECT FREQUENCY MEASUREMENT



OSCILLATOR TUNING

If the variable separation facility is not required, pin 11 is left open-circuit and the 19 kHz signal which then appears may be used to indicate the oscillator frequency. If the variable separation is used, and the drive circuit prevents access to the 19 kHz signal, then the oscillator frequency must be measured directly. A test point should be obtained by modifying the oscillator RC network as shown in Fig. 16.

The output is a pulse train of approximately 1.5 Volts amplitude. Connecting frequency counters of up to 300 pF input capacitance produces less than 0.3% change of the oscillator frequency, which should be set to 228 kHz.

HIGH LOOP GAIN COMPONENTS

For applications demanding operation under low pilot level (e.g., car radio) the following component changes to Fig. 1 are recommended.

R1 = 12k	C3 = 150 pF
R2 = 1.5k	C4 = 330 nF
R8 = 330	C5 = 150 nF
P1 = 10k	

EXTERNAL MONO-STEREO SWITCHING AND OSCILLATOR KILLING

If required, the TCA 4500A can be forced into mono mode simply by grounding pin 9 (see Fig. 1). The 228 kHz oscillator will be automatically killed.

The conditions governing Mono/Stereo switching on pin 9 are the following:

- Quiescent voltage: +2.3 Vdc
- Current required to ensure mono operaton (with 100 mVrms pilot level): 10 μA (from pin 9 to ground) Hysteresis: 0.7μA
- Stereo/mono switching and oscillator killing: less than +500 mV
- Maximum stray capacitance between pin 9 and ground. 100 pF

EXTERNAL COMPONENT FUNCTIONS

P1 – 19 kHz frequency adjustment

P2 – channel separation adjustment and compensation for IF roll-off

R3, R6 – gain fixing resistors. The values shown in the schematic are for unity gain.

C6, C7 – de-emphasis capacitors Value to give: RC = 50 μs.

Values shown in Fig. 1 are recommended for applications with input level higher than 1.0 Vrms.

5

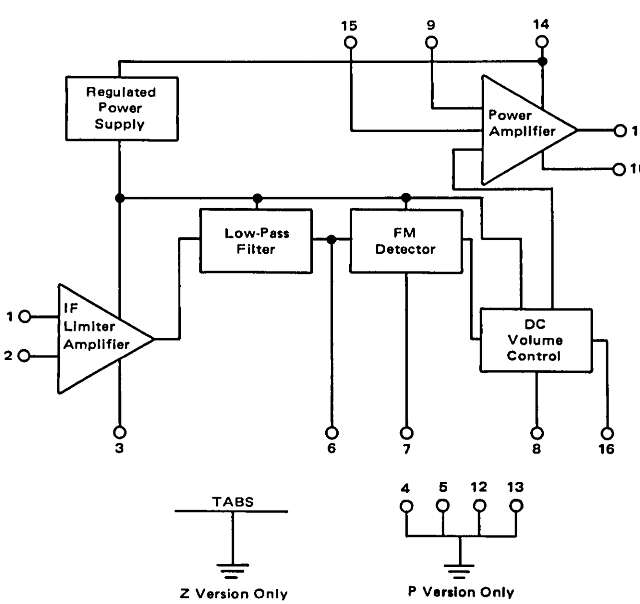
TDA1190Z
TDA1190P

TV SOUND SYSTEM

The TDA1190Z 4.0 watt sound system is designed for television and related applications. The TDA1190P is a low-power version. Functions performed by these devices include: IF Limiting, IF amplifier, low pass filter, FM detector, DC volume control, audio preamplifier, and audio power amplifier.

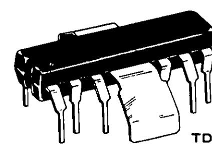
- 4.0 Watts Output Power – TDA1190Z (V_{CC} = 24 V, R_L = 16 Ω)
- 1.3 Watts Output Power – TDA1190P (V_{CC} = 18 V, R_L = 32 Ω)
- Linear Volume Control
- High AM Rejection
- Low Harmonic Distortion
- High Sensitivity

BLOCK DIAGRAM

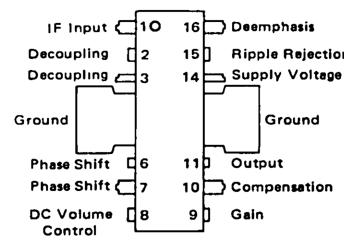


TV SOUND SYSTEM

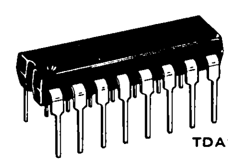
SILICON MONOLITHIC INTEGRATED CIRCUIT



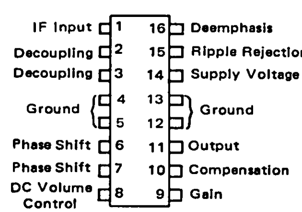
TDA1190Z



PLASTIC PACKAGE
CASE 722A



TDA1190P



PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

Device	Temperature Range	Package
TDA1190Z, P	0 to +75°C	Plastic

5

MAXIMUM RATINGS

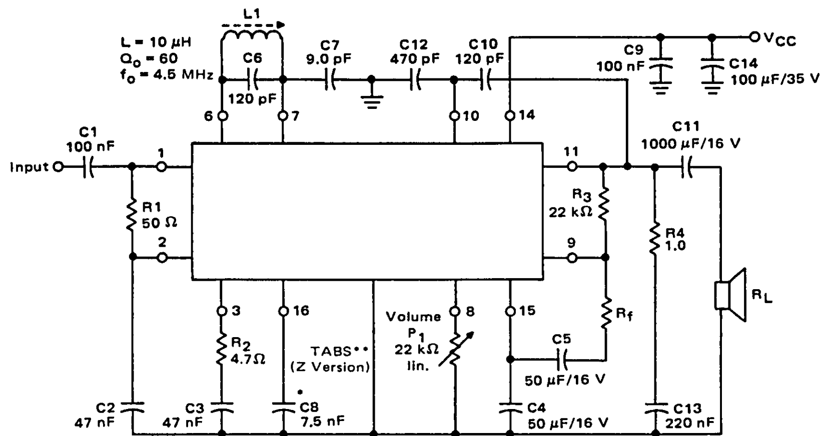
Rating	Symbol	TDA1190Z	TDA1190P	Unit
Supply Voltage Range	V_{CC}	9.0 to 28	9.0 to 22	V
Output Peak Current (Non-repetitive) (Repetitive)	I_o	2.0 1.5	1.5 1.0	A
Input Signal Voltage	V_I	1.0		V
Operating Temperature Range	T_A	0 to +75		°C
Junction Temperature	T_J	150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, f_o = 4.5 MHz, Δf = ±25 kHz, T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ.	Max.	Unit
Quiescent Output Voltage (pin 11)		V_O				V
V_{CC} = 24 V	TDA1190Z		11	12	13	
V_{CC} = 18 V	TDA1190P		8.0	9.0	10	
V_{CC} = 12 V	Both		5.1	6.0	6.9	
Quiescent Drain Current (P1 = 22 kΩ)		I_D				mA
V_{CC} = 24 V	TDA1190Z		11	22	35	
V_{CC} = 18 V	TDA1190P		11	22	35	
V_{CC} = 12 V	Both		–	19	–	
Output Power		P_O				W
(d = 10%, f_m = 400 Hz)						
V_{CC} = 24 V, R_L = 16 Ω	TDA1190Z		–	4.2	–	
V_{CC} = 12 V, R_L = 8.0 Ω	TDA1190Z		–	1.5	–	
V_{CC} = 18 V, R_L = 32 Ω	TDA1190P		1.0	1.3	–	
V_{CC} = 12 V, R_L = 16 Ω	TDA1190P		0.7	0.9	–	
(d = 2%, f_m = 400 Hz)						
V_{CC} = 24 V, R_L = 16 Ω	TDA1190Z		–	3.5	–	
V_{CC} = 12 V, R_L = 8.0 Ω	TDA1190Z		–	1.4	–	
V_{CC} = 18 V, R_L = 32 Ω	TDA1190P		–	1.0	–	
V_{CC} = 12 V, R_L = 16 Ω	TDA1190P		–	0.7	–	
Input Limiting Threshold Voltage (-3.0 dB) at pin 1 Δf = ±7.5 kHz, f_m = 400 Hz, Set P1 for 2.0 Vrms on pin 11		V_I				μV
	TDA1190Z		–	40	100	
	TDA1190P		–	60	100	
Distortion (P_O = 50 mW, f_m = 400 Hz, Δf = ±7.5 kHz)						%
V_{CC} = 24 V, R_L = 16 Ω	TDA1190Z		–	0.75	–	
V_{CC} = 18 V, R_L = 32 Ω	TDA1190P		–	1.0	–	
V_{CC} = 12 V, R_L = 16 Ω	Both		–	1.0	–	
Frequency Response of Audio Amplifier (-3.0 dB) (R_L = 16 Ω, C_{10} = 120 pF, C_{12} = 470 pF, P_1 = 22 kΩ)		B				Hz
R_f = 82 Ω			–	70 to 12 k	–	
R_f = 47 Ω			–	70 to 7.0 k	–	
Recovered Audio Voltage (pin 16) ($V_I \geq$ 1 mV, f_m = 400 Hz, Δf = ±7.5 kHz, P_1 = 0)		V_o	–	120	–	mV
Amplitude Modulation Rejection ($V_I \geq$ 1.0 mV, f_m = 400 Hz, m = 30%)		AMR	–	55	–	dB
Signal and Noise to Noise Ratio ($V_I \geq$ 1.0 mV, V_o = 4.0 V, f_m = 400 Hz)		$\frac{S+N}{N}$	50	65	–	dB
Input Resistance (pin 1) (V_I = 1.0 mV)		r_i	–	30	–	kΩ
Input Capacitance (pin 1) (V_I = 1.0 mV)		C_i	–	5.0	–	pF
DC Volume Control Attenuation (P1 = 12 kΩ)		–	–	90	–	dB

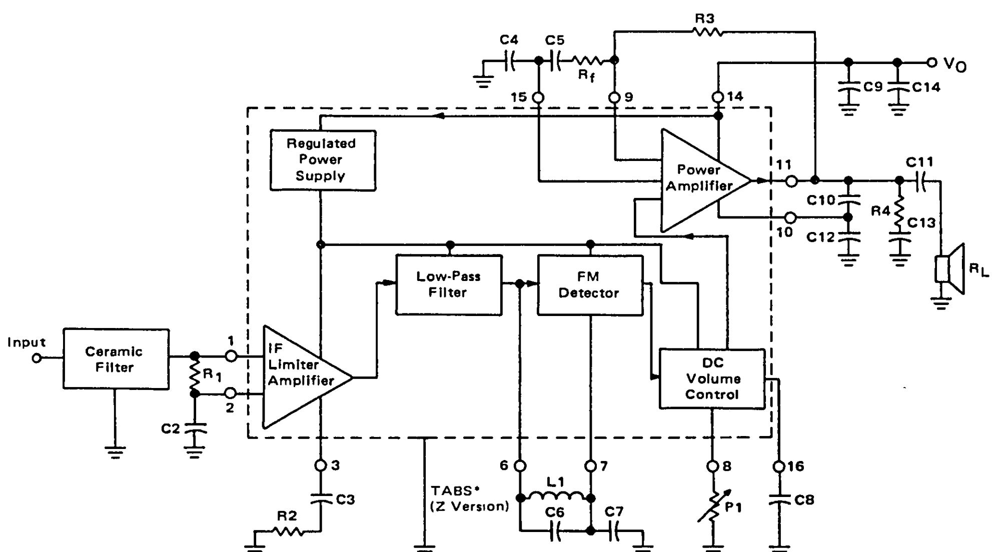
5

TEST CIRCUIT



	TDA1190Z		TDA1190P		
V_{CC}	12	24	12	18	V
R_L	8	16	16	32	Ω
R_f	82	47	150	82	Ω

TYPICAL CIRCUIT CONFIGURATION



TDA2002
TDA2002A

8 WATT AUDIO POWER AMPLIFIER

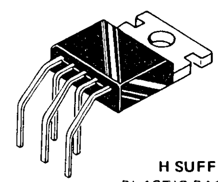
The TDA2002 and TDA2002A are Class B power amplifiers designed for automotive and general-purpose audio applications. High output current capability (3.5 A) enables these devices to drive low-impedance loads (down to 1.6 Ω) with low harmonic and crossover distortion. High-voltage protection is available (TDA2002) which enables the amplifier to withstand 40 V transients. These devices provide an output power of 8 watts (typ) with $R_L = 2\ \Omega$ and 4.8 watts (min) with $R_L = 4\ \Omega$ at 14.4 volts

- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Supply Over Voltage Protection
- Wide Supply Voltage Range (8 – 18 Volts)
- Low External Component Count

8 WATT

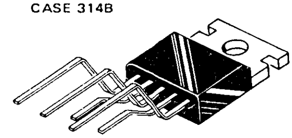
AUDIO POWER AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

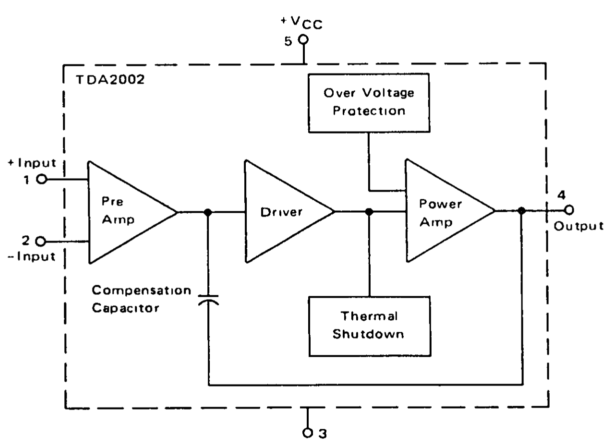


H SUFFIX
PLASTIC PACKAGE
CASE 314A

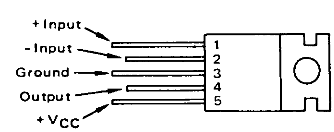
V SUFFIX
PLASTIC PACKAGE
CASE 314B



BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION		
Device	**Temperature Range**	**Plastic Package**
TDA2002H *	-40 to +85°C	Case 314A
TDA2002V *	-40 to +85°C	Case 314B
TDA2002AH	-40 to +85°C	Case 314A
TDA2002AV	-40 to +85°C	Case 314B

*High Voltage

5

MAXIMUM RATINGS (T_A = +25°C)

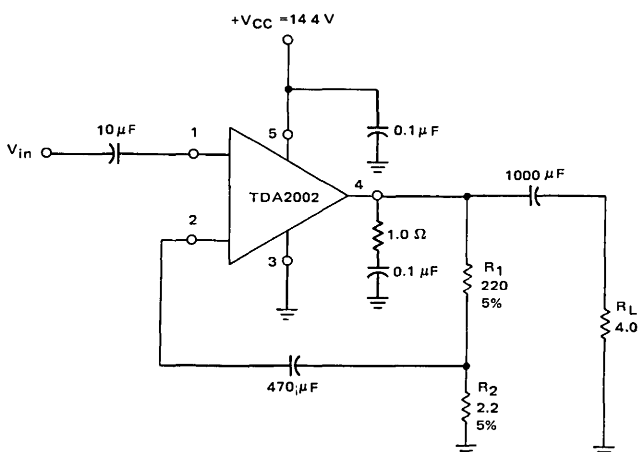
Rating	Value	Unit
Peak Supply Voltage TDA2002 (Transients of 50 ms or less) TDA2002/2002A (Steady State)	 40 28	V
Operating Power Supply Voltage	18	V
Peak Output Current (Nonrepetitive) (Repetitive)	4 5 3.5	A
Junction Temperature	150	°C
Storage Temperature Range	-65 to +150	°C
Operating Temperature Range	-40 to +85	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 4 Vdc, R_L = 4 0 Ω, f= 1 0 kHz, T_A = 25°C unless otherwise noted) *

Characteristic	Symbol	Min	Typ	Max	Unit
Quiescent Drain Current (V_{in} = 0)	I_D	–	–	80	mA
Quiescent Output Voltage (V_{in} = 0)	V_O	6.4	7.2	8.0	V
Power Output – 10% Distortion (V_{CC} = 14.4 V, R_L = 4.0 Ω) (V_{CC} = 14.4 V, R_L = 2.0 Ω) (V_{CC} = 16 V, R_L = 4 0 Ω) (V_{CC} = 16 V, R_L = 2.0 Ω)	P_o	 4 8 7.0 – –	 5.2 8 0 6.5 10	 – – – –	W
Input Resistance (Pin 1)	r_i	70	150	–	kΩ
Equivalent Input Noise Voltage (R_S = 0, Bandpass = 20 Hz to 15 kHz)	e_n	–	4	–	μV
Equivalent Input Noise Current (R_S = 0, Bandpass = 20 Hz to 15 kHz)	i_n	–	0 1	–	nA
Power Supply Rejection Ratio (f_{ripple} = 100 Hz)	P_{SRR}	30	35	–	dB

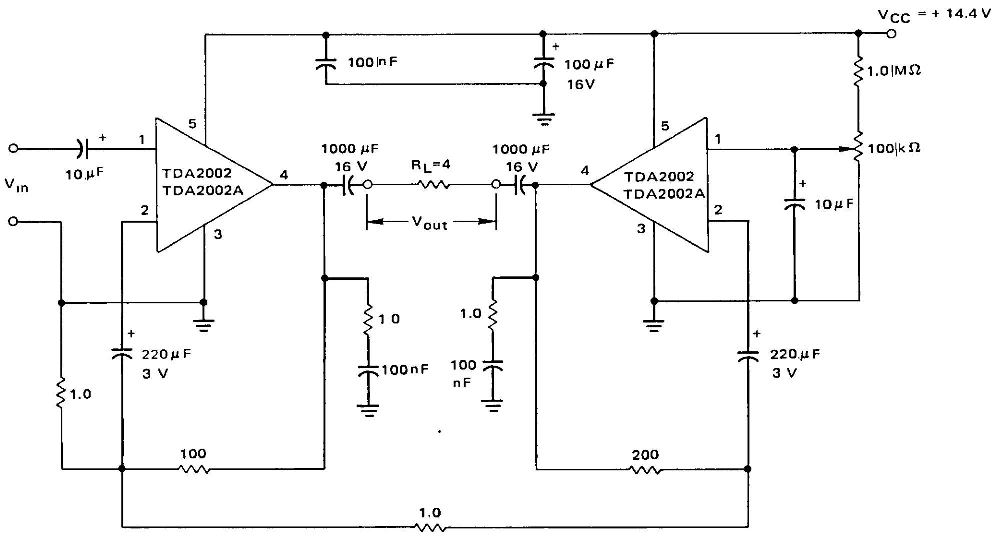
*See Test Circuit – Figure 1.

FIGURE 1 – APPLICATION AND TEST CIRCUIT



5

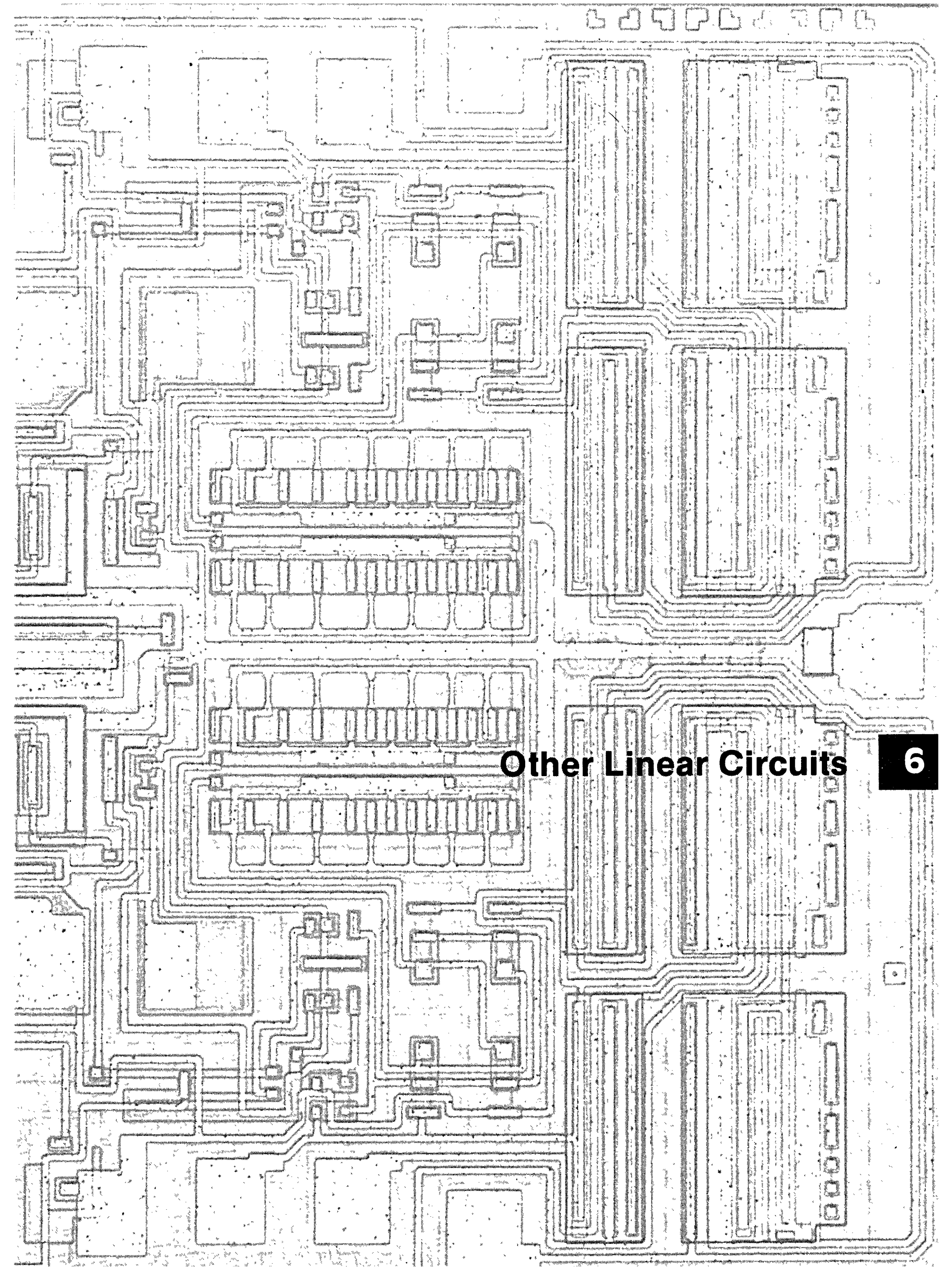
FIGURE 2 — 15 WATT APPLICATION CIRCUIT
(Typical Bridge Configuration)



Note: The TDA2002, A is not compensated for operation with a closed loop gain of 20 or less. Operation below a gain of 20 may cause stability problems.

5

5



Other Linear Circuits

6

OTHER LINEAR CIRCUITS

HIGH FREQUENCY AMPLIFIERS

A variety of high-frequency circuits with features ranging from low-cost simplicity to multi-function versatility marks Motorola's line of integrated RF/IF amplifiers. Devices described here are intended for industrial and communications applications. For devices especially dedicated to consumer products, i.e., TV and entertainment radio, see "Circuits for Consumer Applications".

NON-AGC Amplifiers

SE/NE592 – Differential Two Stage Video Amplifier

A monolithic, two state differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

MC1733/MC1733C – Video Amplifier

Differential input and output amplifier provides three fixed gain options with bandwidth to 120 MHz. External resistor permits any gain setting from 10 to 400 v/v. Extremely fast rise time (2.5 ns typ) and propagation delay time (3.6 ns typ) makes this unit particularly useful as pulse amplifier in tape, drum, or disc memory read applications.

MC1552/MC1553 – Low Distortion Amplifier

A high performance amplifier with internal series feedback for stable voltage gain and low distortion. Temperature compensation stabilizes operating point. Has selectable gain option and well characterized data that permits accurate response shaping. Useful for critical applications such as wideband linear amplifiers or fast-rise pulse amplifiers.

AGC Amplifiers

MC1550 – Low Cost Building Block

Single-stage cascade connected amplifier with delayed AGC characteristics, for operation at frequencies to 100 MHz. Has typical power gain of 25 dB @ 60 MHz.

MC1545/MC1445 – Gated 2-Channel Input

Differential input and output amplifier with gated 2-channel input for a wide variety of switching purposes. Typical 75 MHz bandwidth makes it suitable for high-frequency applications such as video switching, FSK circuits, multiplexers, etc. Gating circuit is useful for AGC control.

MC1590 – Wide-Band General Purpose

Has differential inputs and outputs with unneutralized power gain as high as 35 dB typical at 100 MHz in tuned amplifier service. Effective AGC voltage range from 5 to 7 volts for a 30 dB gain reduction.

Electrical Specifications

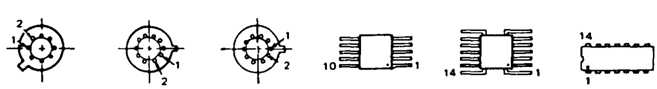
AGC AMPLIFIERS

Operating Temperature Range -55 to +125°C	0 to +75°C	A_V dB	Band width MHz	V_{CC}/V_{EE} Vdc	Case
MC1550	–	22 Min	22	+6/-	603B,606
MC1590	–	44 Typ @ 4 Typ @	10 100	+12/-	601
MC1545	MC1445	19 Typ @	75	+5/-5	603,607 632

NON AGC AMPLIFIERS

MC1733	MC1733C	52 @ 40 20	40 90 120	+6/-6	603,632
MC1553	–	46 @ 52	35 15	+6/-6	603B
MC1552	–	34 @ 40 @	40 35	+6/-6	603B
SE592	NE592	55 @ 45 @	40 90	+6/-6	603,632

Package Styles



CASE	601	603	603B	606	607	632
MATERIAL	Metal	Metal	Metal	Ceramic	Ceramic	Ceramic
SUFFIX after type number	G	G	G	F	F	L

SPECIAL PURPOSE CIRCUITS

The linear-integrated-circuits listed in this section were developed by Motorola for the system design engineer to fill special-purpose requirements. Temperature ranges and package availability are tailored to provide price/performance versatility.

Linear Four-Quadrant Multipliers

MC1594/1494

This device is designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/MC1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

MC1595/MC1495

Similar to the MC1594/1494, but without internal level shift and voltage regulator circuits.

Balanced Modulator-Demodulator

MC1596/MC1496

Designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection and chopper applications.

Timing Circuits

MC1555/MC1455/MC1422

These devices are highly stable timing circuits capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits. Timing from Microseconds through Hours. The MC1422 has variable threshold level, adjustable externally.

	Timing Error (typ)
MC1555	0.5%
MC1455	1.0%
MC1422	1.0%

MC3556/MC3456

Dual Version of the MC1555/MC1455

Low Frequency Power Amplifier

MC1554/MC1454

One-watt power amplifier for single or split supply operation. Typical voltage gain of 10, 18, or 36 V/V with 0.4% THD.

Power Control Circuits

MC3370

Electronic switch for triac triggering applications. Features zero-crossing detector to eliminate RFI, differential input with dual sensor inputs, input open and short protection, and built-in regulator permitting AC line operation.

CA3059/3079

Zero voltage switches designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz.

6

Monolithic Dual OP Amp and Dual Comparator

MC3505/MC3405

This device contains two differential input operational amplifiers and two comparators each set capable of single supply operation. This operational amplifier-comparator circuit will find its applications as a general purpose product for automotive circuits and as an industrial "building block".

- Op Amp Equivalent in Performance to MC3403
- Comparator Similar in Performance to LM339
- Op Amps are Internally Frequency Compensated
- Supply Operation 3.0 Volts to 36.0 Volts
- Dual Supply Operation also Available

Package Styles

Operating Temperature Range		
-55 to +125°C	0 to +70°C	Case
MC1554	MC1454	603B
MC1555		601, 693
	MC1455	601, 626, 693
MC1594	MC1494	620
MC1595	MC1495	632
MC1596		603, 632
	MC1496	603, 632, 646
	MC1422	601, 626
MC3505		632
	MC3405	632, 646
MC3523		693
	MC3423	626, 693
MC3556		632
	MC3456	632, 646
	MC3370	626
	CA3059* CA3079*	646

*-40 to +85°C

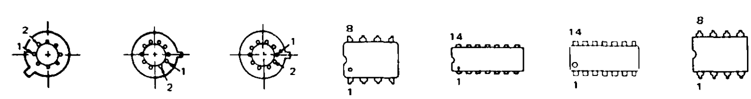
Overvoltage Protection Circuit

MC3523/MC3423

OVPs protect sensitive circuitry from transients or regulator failures when used with an external "crowbar" SCR. They sense the overvoltage and quickly "crowbar" or short circuit the supply, forcing it into current limiting or opening fuse or CB.

Voltage threshold is adjustable and OVPs can be programmed for minimum duration before tripping, supplying noise immunity.

I_O ±mA	V_{CC} Volts		V_{Sense} Volts					
Max	Min	Max	Min	Max	Device Number	Suffix	T_A °C	Case
300	4.5	40	2.45	2.75	MC3423	P	0 to +70	626
						U	0 to +70	693
					MC3523	U	-55 to +125	693



CASE	601	603	603B	626	632	646	693
MATERIAL	Metal	Metal	Metal	Plastic	Ceramic	Plastic	Ceramic
SUFFIX after type number	G	G	G	P or P1	L	P	U

CA3059
CA3079

ZERO VOLTAGE SWITCHES

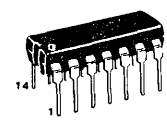
. . . designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V @ 50/60 Hz.

Applications:

- Relay Control
- Heater Control
- Valve Control
- Lamp Control
- Synchronous Switching of Flashing Lights
- On-Off Motor Switching
- Differential Comparator With Self-Contained Power Supply for Industrial Applications
- Photosensitive Control
- Power One-Shot Control

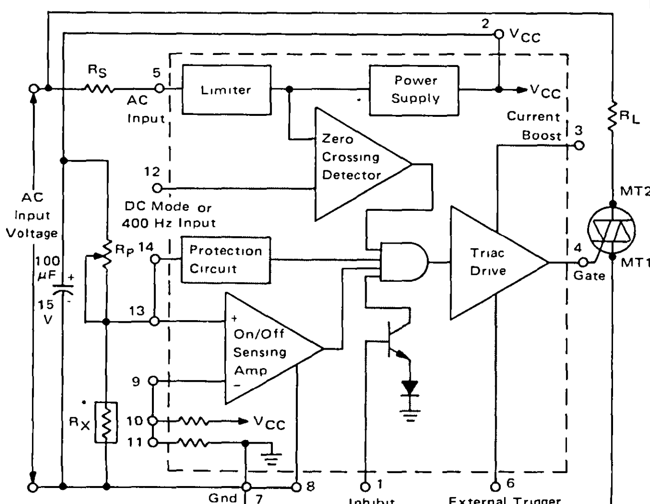
ZERO VOLTAGE SWITCHES

SILICON MONOLITHIC INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 646
TO-116

FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM



*NTC Sensor
NOTE Shaded Area Not Included With CA3079

TABLE A

AC Input Voltage (50/60 Hz) vac	Input Series Resistor (R_S) kΩ	Dissipation Rating for R_S W
24	2.0	0.5
120	10	2.0
208/230	20	4.0
277	25	5.0

FUNCTIONAL BLOCK DESCRIPTION

1. **Limiter-Power Supply** — Allows operation of the CA3059/79 directly from an ac line. Suggested dropping resistor (R_S) values are given in Table A.

2. **Differential On/Off Sensing Amplifier** — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented using this block.

3. **Zero-Crossing Detector** — Synchronizes the output pulses to the zero voltage point of the ac cycle. This synchronization eliminates RFI when used with resistive loads.

4. **Triac Drive** — Supplies high-current pulses to the external power controlling thyristor.

5. **Protection Circuit (CA3059 only)** — A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive current from the external triac.

6. **Inhibit Capability (CA3059 only)** — Thyristor firing may be inhibited by the action of an internal diode gate at Pin 1.

7. **High Power DC Comparator Operation (CA3059 only)** — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector). When Pin 13 is positive with respect to Pin 9, current to the thyristor is continuous

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
DC Supply Voltage (Between Pins 2 and 7	CA3059	V_{CC}	12	Vdc
	CA3079		10	
DC Supply Voltage (Between Pins 2 and 8)	CA3059	V_{CC}	12	Vdc
	CA3079		10	
Peak Supply Current (Pins 5 and 7)		$I_{5,7}$	±50	mA
Fail-Safe Input Current (Pin 14)		I_{14}	2 0	mA
Output Pulse Current (Pin 4)		I_{out}	150	mA
Junction Temperature		T_J	150	°C
Operating Temperature Range		T_A	-40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Operation @ 120 Vrms, 50-60 Hz, T_A = 25°C)**

Characteristic	Test Circuits	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	Fig 2	V_S				Vdc
Inhibit Mode						
R_S = 10 k, I_L = 0			6 1	6 5	7 0	
R_S = 5 0 k, I_L = 2 0 mA			–	6.1	–	
Pulse Mode						
R_S = 10 k, I_L = 0			6 0	6 4	7 0	
R_S = 5.0 k, R_L = 2 0 mA			–	6 2	–	
Gate Trigger Current (V_{GT} = 1.0 V, Pins 3 and 2 connected)	Fig 3	I_{GT}	–	160	–	mA
Peak Output Current, Pulsed	Fig. 3	I_{OM}				mA
With Internal Power Supply, V_{GT} = 0						
Pin 3 Open			50	125	–	
Pins 3 and 2 Connected			90	190	–	
With External Power Supply, V_{CC} = 12 V, V_{GT} = 0	Fig. 4					
Pin 3 Open			–	230	–	
Pins 3 and 2 Connected			–	300	–	
Inhibit Input Ratio (Ratio of Voltage @ Pin 9 to Pin 2)	Fig. 5	V_9/V_2	0.465	0.485	0 520	–
Total Gate Pulse Duration (C_{Ext} = 0)	Fig 6					µs
Positive dv/dt		tp	70	100	140	
Negative dv/dt		tn	70	100	140	
Pulse Duration After Zero Crossing (C_{Ext} = 0, R_{Ext} = ∞)	Fig 6					µs
Positive dv/dt		tp_1	–	50	–	
Negative dv/dt		tn_1	–	60	–	
Output Leakage Current Inhibit Mode***	Fig 3	I_4	–	0.001	10	µA
Input Bias Current CA3059	Fig 7	I_{IB}	–	0 15	1 0	µA
CA3079			–	0 15	2 0	
Common Mode Input Voltage Range (Pins 9 and 13 Connected)	–	V_{CMR}	–	1 4 to 5 0	–	Vdc
Inhibit Input Voltage CA3059 only	Fig 8	V_1	–	1.4	1.6	Vdc
External Trigger Voltage CA3059 only	–	V_6-V_4	–	1.4	–	Vdc

*Care must be taken, especially when using an external power supply, that total package dissipation is not exceeded.

**The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration test. However, the series resistor (R_S) must have the indicated value, shown in Table A for the specified input voltage.

***I_4 out of Pin 4
2 V on Pin 1
S1 position 2

6

TEST CIRCUITS

(All resistor values are in ohms)

FIGURE 2 – DC SUPPLY VOLTAGE

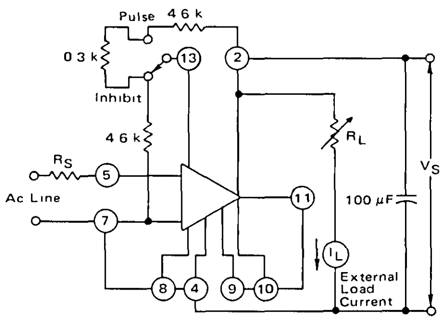


FIGURE 3 – PEAK OUTPUT (PULSED) AND GATE TRIGGER CURRENT WITH INTERNAL POWER SUPPLY

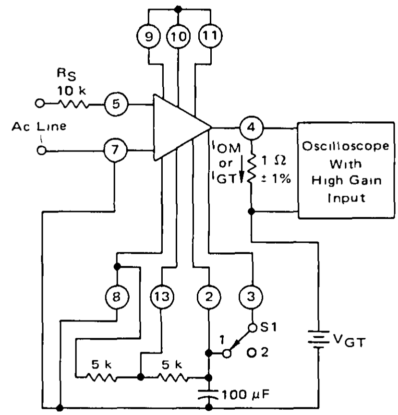


FIGURE 4 – PEAK OUTPUT CURRENT (PULSED) WITH EXTERNAL POWER SUPPLY

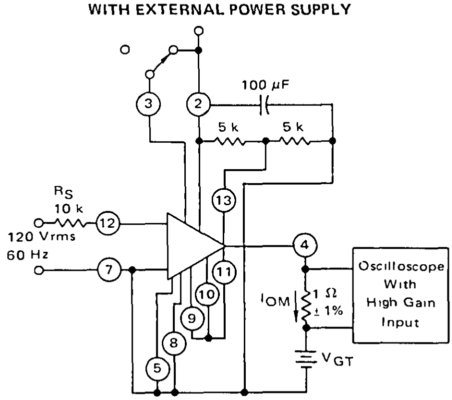


FIGURE 5 – INPUT INHIBIT RATIO

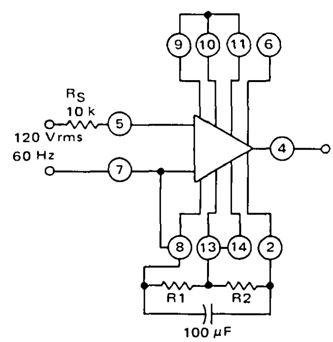


FIGURE 6 – GATE PULSE DURATION TEST CIRCUIT WITH ASSOCIATED WAVEFORM

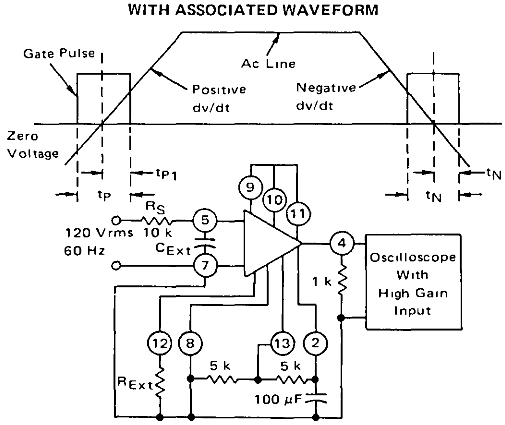
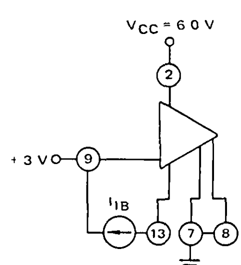


FIGURE 7 – INPUT BIAS CURRENT TEST CIRCUIT



6

TYPICAL CHARACTERISTICS

FIGURE 8 – INHIBIT INPUT VOLTAGE TEST

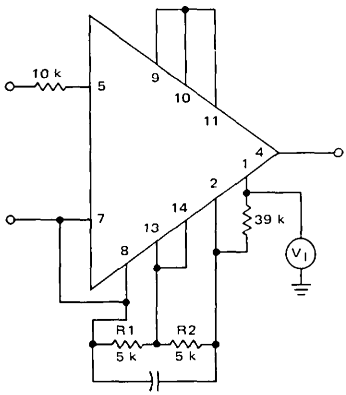


FIGURE 9 – PEAK OUTPUT CURRENT (PULSED) versus EXTERNAL POWER SUPPLY VOLTAGE

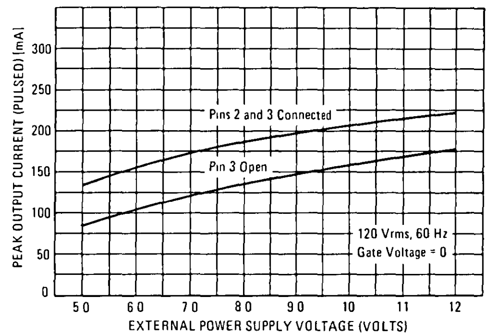


FIGURE 10 – PEAK OUTPUT CURRENT (PULSED) versus AMBIENT TEMPERATURE

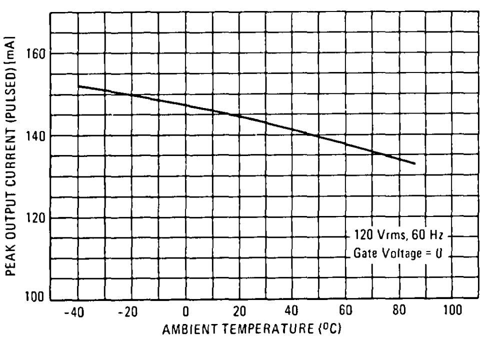


FIGURE 11 – TOTAL PULSE WIDTH versus AMBIENT TEMPERATURE

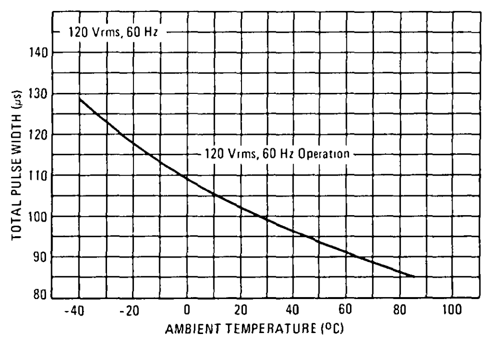


FIGURE 12 – INTERNAL SUPPLY versus AMBIENT TEMPERATURE

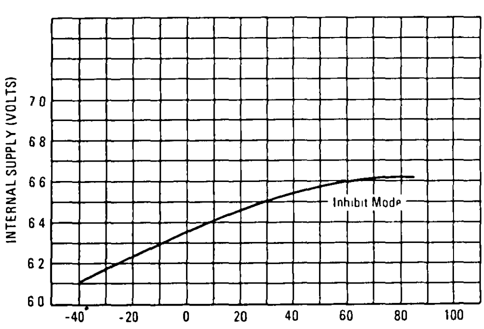


FIGURE 13 – INHIBIT VOLTAGE RATIO versus AMBIENT TEMPERATURE

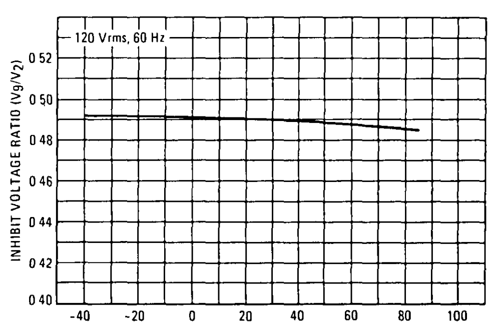
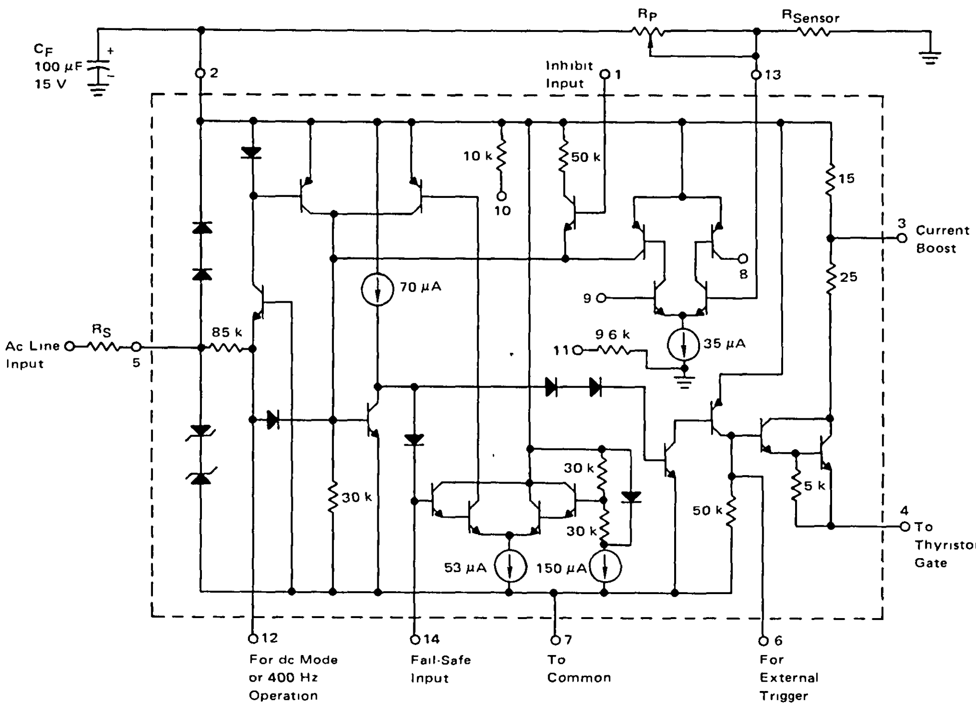


FIGURE 14 – CIRCUIT SCHEMATIC



NOTE. Current sources are established by an internal reference
Pins 1, 6, 12, and 14 are not used with CA3079

6

APPLICATION INFORMATION

Power Supply

The CA3059 and CA3079 are self-powered circuits, powered from the ac line through an appropriate dropping resistor (see Table A). The internal supply is designed to power the auxiliary power circuits.

In applications where more output current from the internal supply is required, an external power supply of higher voltage should be used. To use an external power supply, connect pin 5 and pin 7 together and apply the synchronizing voltage to pin 12 and the dc supply voltage to pin 2 as shown in Figure 4.

Operation of Protection Circuit (CA3059 Only)

The protection circuit, when connected, will remove current drive from the triac if an open or shorted sensor is detected. This circuit is activated by connecting pin 13 to pin 14 (see Figure 1).

The following conditions should be observed when the protection circuit is utilized:

A. The internal supply should be used and the external load current must be limited to 2 mA with a 5 kΩ dropping resistor.

B. Sensor Resistance (R_X) and Rp values should be between 2 kΩ and 100 kΩ.

C. The relationship $0.33 < R_X/R_P < 3$ must be met over the anticipated temperature range to prevent undesired activation of the circuit. A shunt or series resistor may have to be added.

External Inhibit Function (CA3059 Only)

A priority inihibit command applied to pin 1 will remove current drive from the thyristor. A command of at least +1.2 V @ 10 µA is required. A DTL or T^2L logic 1 applied to pin 1 will activate the inhibit function.

DC Gate Current Mode (CA3059 Only)

When comparator operation is desired or inductive loads are being switched, pins 7 and 12 should be connected. This connection disables the zero-crossing detector to permit the flow of gate current from the differential sensing amplifier on demand. Care should be exercised to avoid possible overloading of the internal power supply when operating the device in this mode. A resistor should be inserted between pin 4 and the thyristor gate in order to limit the current.

MC1422

Specifications and Applications Information

MONOLITHIC TIMING CIRCUIT WITH EXTERNALLY ADJUSTABLE THRESHOLD LEVEL

The MC1422 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Useable as a Differential Comparator Timer
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0 005% per °C
- Normally "On" or Normally "Off" Output

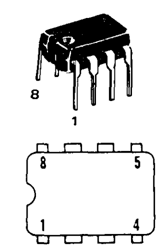
TYPICAL APPLICATIONS

- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

TIMING CIRCUIT WITH ADJUSTABLE THRESHOLD

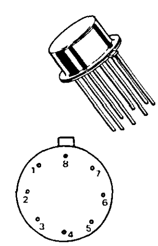
MONOLITHIC SILICON INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(Top View)



1. Ground
2. Trigger
3. Output
4. Reset
5. Variable Threshold Reference
6. Threshold
7. Discharge
8. V_{CC}

G SUFFIX
METAL PACKAGE
CASE 601
TO-99



(Top View)

1. Ground
2. Trigger
3. Output
4. Reset
5. Variable Threshold Reference
6. Threshold
7. Discharge
8. V_{CC}

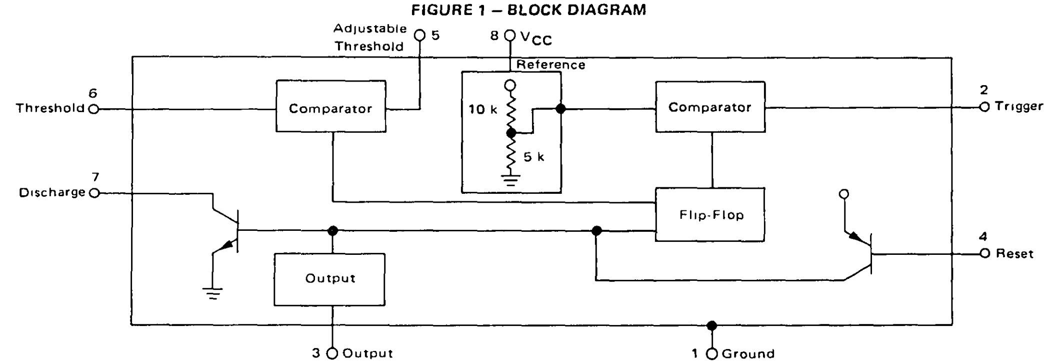
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+16	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range (Ambient)	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ORDERING INFORMATION

Type	Temperature Range	Package
MC1422G	0 to +70°C	Metal Can
MCC1422P1	0 to +70°C	Plastic DIP

FIGURE 1 — BLOCK DIAGRAM



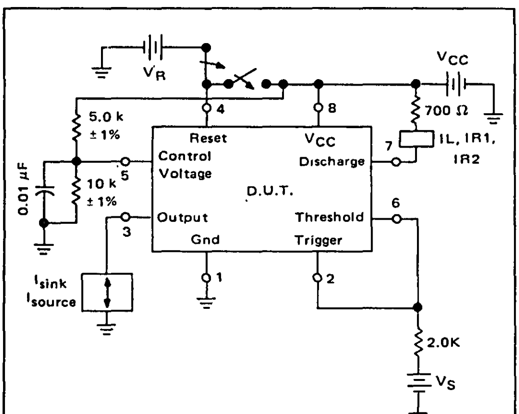
ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +14 V unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	–	14	V
Supply Current	I_D				mA
V_{CC} = 5.0 V, $R_L = \infty$		–	3.0	6.0	
V_{CC} = 14 V, $R_L = \infty$		–	10	15	
Low State (Note 1)					
Timing Error (Note 2)					
R_A, R_B = 1.0 kΩ to 100 kΩ					
Initial Accuracy C = 0.1 μF		–	1.0	–	%
Drift with Temperature		–	50	–	PPM/°C
Drift with Supply Voltage		–	0.01	–	%/Volt
Threshold Voltage (Figure 2)	V_{th}	–	2/3	–	xV_{CC}
Trigger Voltage	V_T				V
V_{CC} = 14 V		–	5.0	–	
V_{CC} = 5.0 V		–	1.67	–	
Trigger Current	I_T	–	0.5	–	μA
Discharge Leakage Current	I_{dis}	–	–	250	nA
Reset Current	I_R	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	–	1.0	μA
Output Voltage Low	V_{OL}				V
(V_{CC} = 14 V)					
I_{sink} = 10 mA		–	0.1	0.35	
I_{sink} = 50 mA		–	0.4	1.0	
I_{sink} = 100 mA		–	2.0	3.5	
I_{sink} = 200 mA		–	2.5	–	
Output Voltage High	V_{OH}				V
(I_{source} = 25 mA)					
V_{CC} = 14 V		11.75	13.3	–	
V_{CC} = 5.0 V		2.75	3.3	–	
Rise Time of Output	t_{OLH}	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	ns

NOTES:

1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 14 V.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

FIGURE 2 – DC TEST CIRCUIT



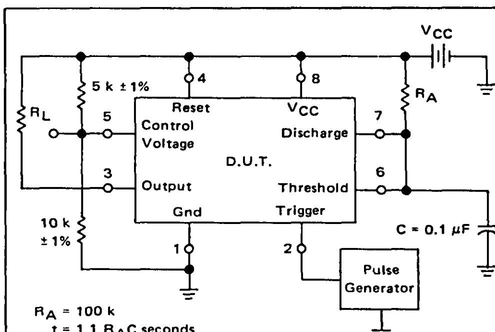
Notes:

V_{CC} = Supply Voltage. 5.0 V ≤ V_{CC} ≤ 14 V Range
V_S = Switching Voltage: 1.4 V ≤ V_S ≤ 11.0 V Range

When $V_S \geq 2/3\ V_{CC}$, V_O is low ≅ 0 at $R_L = \infty$
When $V_S \leq 1/3\ V_{CC}$, V_O is high ≅ V_{CC} at $R_L = \infty$

V_R = Reset Voltage: V_R = 0.4 V or 1.0 V during Reset Test
During other tests, Pin 4 tied to V_{CC}.

FIGURE 3 – AC TEST CIRCUIT



R_A = 100 k
t = 1.1 R_AC seconds

External components must be bridged so that exact values are used in the frequency formula.

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

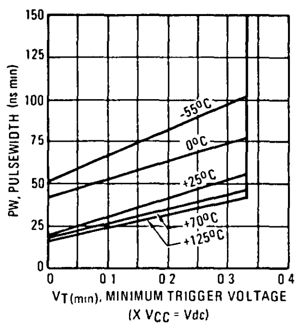


FIGURE 5 – SUPPLY CURRENT

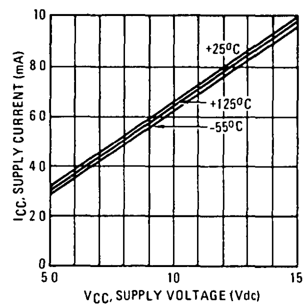


FIGURE 6 – HIGH OUTPUT VOLTAGE

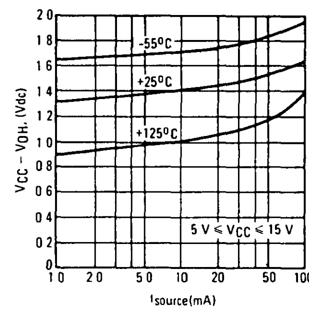


FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

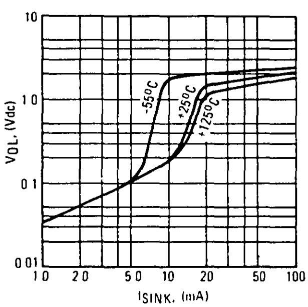


FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

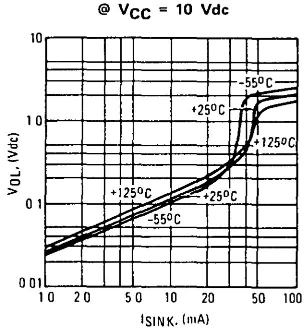


FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

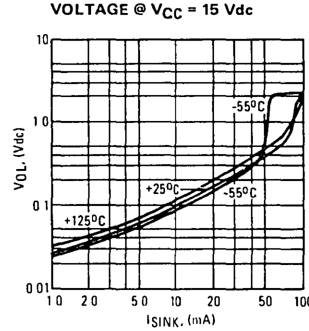


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

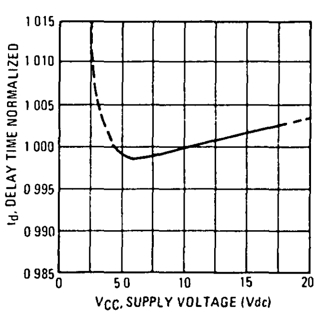


FIGURE 11 – DELAY TIME versus TEMPERATURE

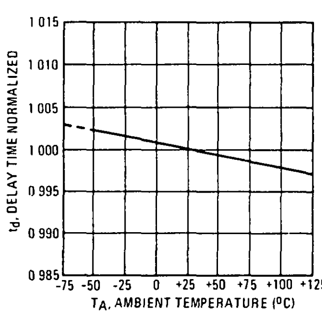


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE

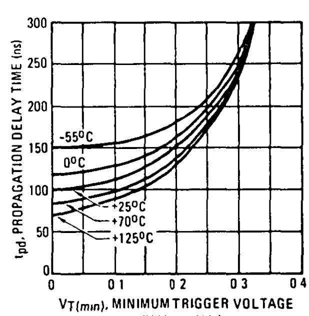
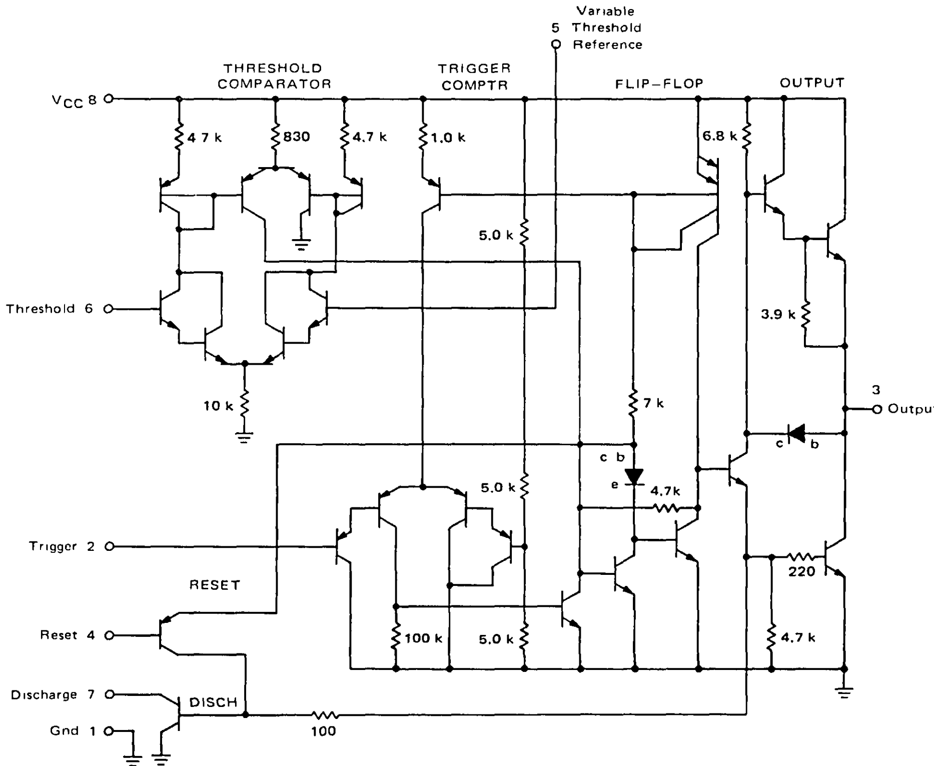


FIGURE 13 — CIRCUIT SCHEMATIC CONTROL VOLTAGE



GENERAL INFORMATION

The MC1422 is a monolithic timing circuit similar in performance and function to the MC1455 timer. It can be used in both the astable and monostable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are offered. The reference voltage of the trigger comparator is a fixed ratio of the supply voltage while the reference voltage of the threshold comparator is completely adjustable.

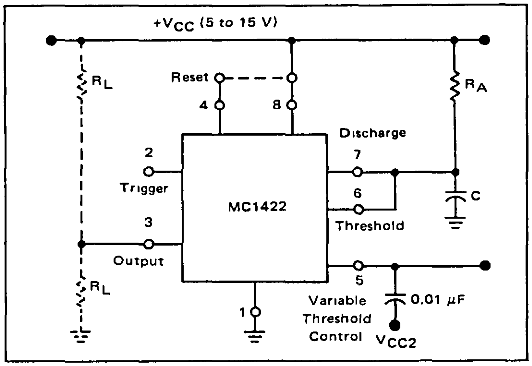
The MC1422 offers a completely independent variable threshold terminal. This feature allows it to be used as a modulation terminal as well as a synchronization terminal giving an additional degree of freedom in circuit design. The reference voltage pin (pin 5) for the threshold comparator is completely adjustable.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain low. The reset pin should be tied to the supply voltage when not in use.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches the external reference voltage the threshold comparator resets the flip-flop. This discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 15. The trigger pulse width must be less than the timing period.

FIGURE 14 – MONOSTABLE CIRCUIT



APPLICATIONS INFORMATION

In general, the MC1422 can be used in any application where the MC1455/NE555 is currently being used as long as an external reference is supplied. (Refer to MC1455 data sheet for these applications.) The applications listed below are unique to the MC1422 and its design.

Zero Crossing Cycler

This circuit (see Figure 15) is most useful where it is necessary to cycle a thyristor at some frequency and duty cycle at line zero crossing only. This cycling at zero crossing only will reduce EMI, and current surges if capacitive loads are used.

Circuit Description

In order to have exact zero crossing cycling a phase shift network (R3)(C2) is used. Diodes C_{R1} and C_{R2} limit the line voltage to V- and V+. This limited line voltage, which appears somewhat like a square wave, is used as a sync pulse when differentiated by C1 and attenuated to 1/3 by R1 and R2. Cycle time is dependent on R4 and C3. The duty cycle is set by potentiometer R4.

It should be noted that this zero crossing cycler is intended for low frequency cycling, much lower than the line frequency used.

$$T_{cycle} = 0.69\ (R4)(C3) \text{ or } f_{cycle} = \frac{1.44}{(R4)(C3)}$$

FIGURE 15 – ZERO CROSSING CYCLER

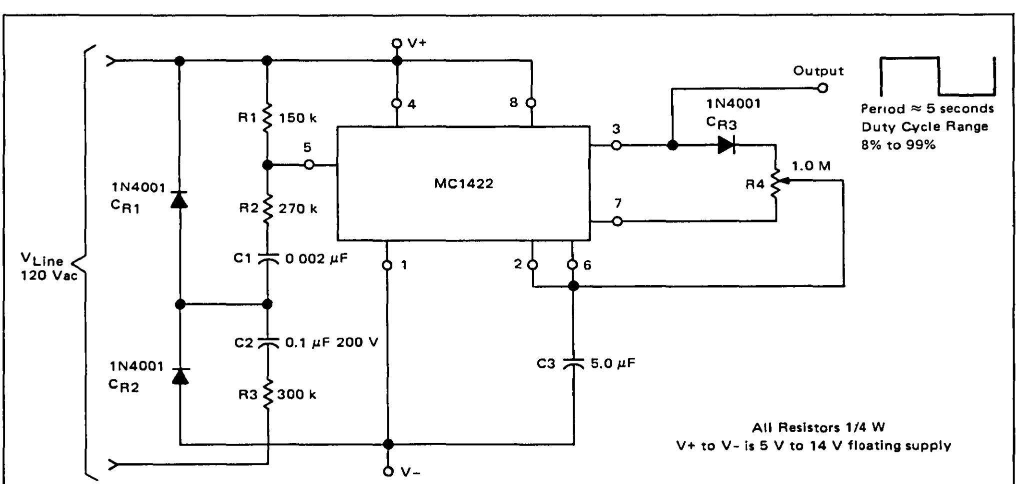


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FIGURE 16 – PULSE WIDTH MODULATOR

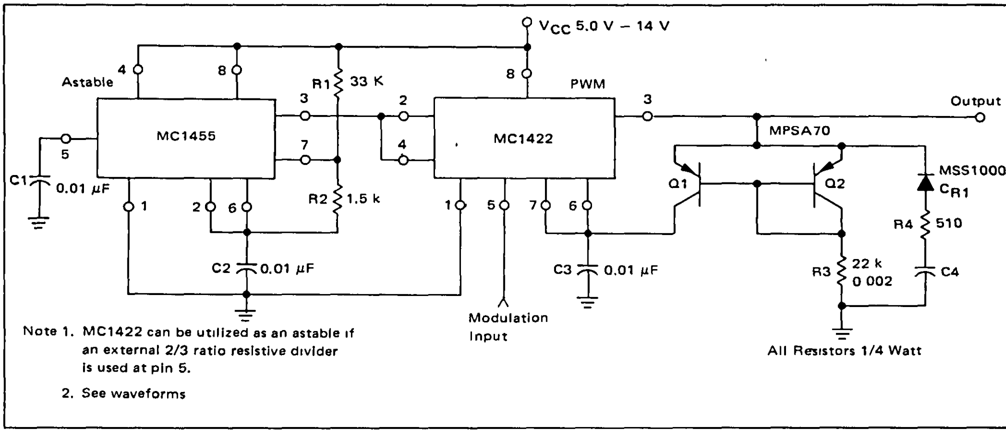
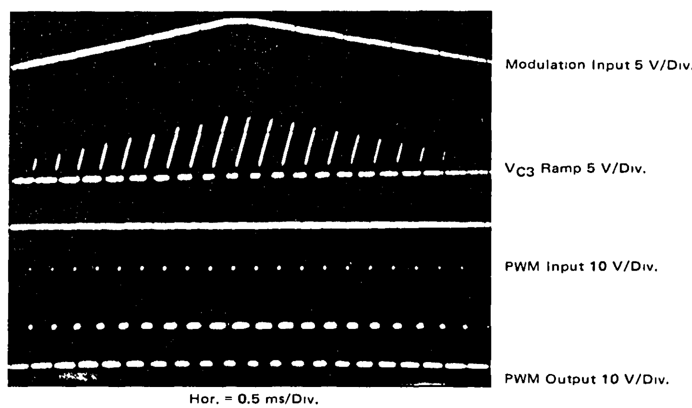


FIGURE 17 – PULSE WIDTH MODULATOR WAVEFORMS



Pulse Width Modulator

The MC1422 is used as a pulse width modulator (PWM) with the MC1455 being utilized as an astable. The MC1422 can be used as an astable in place of the MC1455 if an external reference of approximately 2/3 V_{CC} is used at Pin 5.

The transistors Q1 and Q2 are configured as a current mirror to provide a linear voltage ramp across C3. This constant current scheme attributes a relatively linear transfer characteristic for the pulse width modulator.

Several considerations must be made when using this circuit.

1. The minimum duty cycle out is limited to the complement of the input signal. (i.e., a 95% duty cycle astable driving the PWM will give a minimum duty cycle output of ≃ 5%.)

   The maximum duty cycle out will also be limited to the maximum duty cycle in.

2. For the astable frequency:

$$f = 1/T = \frac{1.44}{(R_1 + 2R_2)C}$$

3. Duty cycle (D.C.) for the astable:

$$DC = \frac{R_2}{R_1 + 2R_2}$$

For best results the charge time of C3 in the pulse width modulator should be equal to the period of the astable.

$$\frac{I_{Q1}}{C3\,(V_{CC} - 1)} = f_{in} = \frac{1}{T_{C3}} \quad I_{Q1} \simeq I_{Q2} = \frac{V_{CC} - V_{BE}}{R3}$$

V_{CC} = 10 V linearity typically 3% modulation input from 2 volts to 8 volts.

Voltage Controlled Oscillator

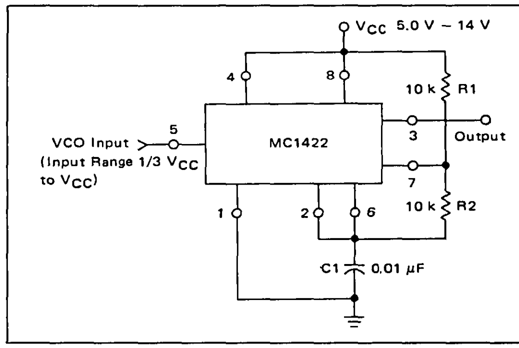
The VCO circuit, which has a nonlinear transfer characteristic will operate satisfactorily up to 200 kHz. The VCO input range is effective from 1/3 V_{CC} to V_{CC} - 2 V, with the highest control voltage producing the lowest output frequency. The equation for the frequency is:

$$f_{out} \simeq \frac{1}{\ln\left(1 - \frac{V5 - 1/3\,V_{CC}}{2/3\,V_{CC}}\right)(R1+R2)C1 + \ln\left(\frac{V5 - 1/3\,V_{CC}}{V5}\right) R2C1}$$

V5 = VCO input control voltage

It should be noted that, the output duty cycle will vary somewhat over the VCO input control range.

FIGURE 18 – VOLTAGE CONTROLLED OSCILLATOR



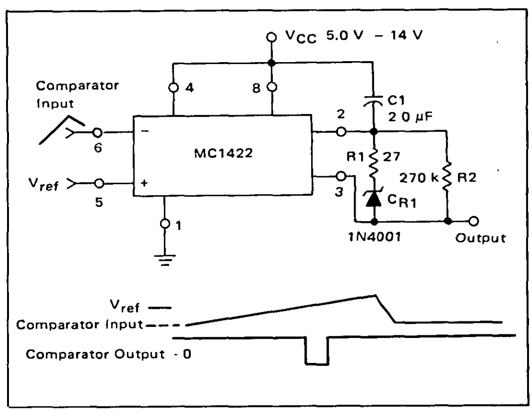
Comparator with Time Out

The MC1422 is used as a comparator with the capability of a timing output pulse when the inverting input (Pin 6) is ⩾ the non-inverting input (Pin 5). The frequency of the pulses for the values of R2 and C1 as shown in Figure 19 is approximately 2.0 Hz, and the pulse width 0.3 ms, f_p = frequency of pulses while Pin 6 voltage is above voltage at Pin 5.

The function of R1 is to limit di/dt, when charging C1.

$$f_p \simeq \frac{1}{R2C1} \text{ or } T_p \simeq R2C1 .$$

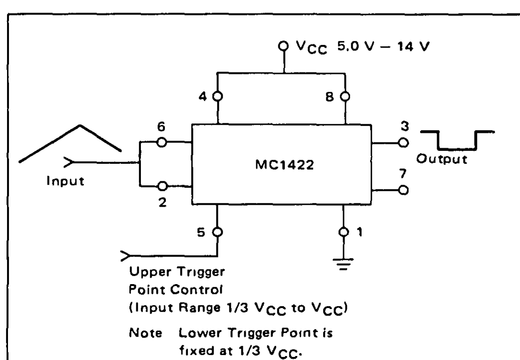
FIGURE 19



Schmitt Trigger

The MC1422 is very useful as a Schmitt Trigger as shown in Figure 20. The lower trigger point is fixed at 1/3 V_{CC}, but the upper trigger point is adjustable by means of Pin 5 from 1/3 V_{CC} to slightly less than V_{CC}. The Schmitt trigger will operate with input frequencies up to 50 kHz.

FIGURE 20



ORDERING INFORMATION

Device	Temperature Range	Package
MC1438R	0°C to +70°C	Metal Power
MC1538R	−55°C to +125°C	Metal Power

MC1438R
MC1538R

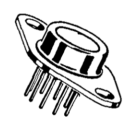
POWER BOOSTER

The MC1538/MC1438 is designed as a high current gain amplifier (70 dB), with unity voltage gain that can deliver load currents up to ±300 mAdc. This device is ideally suited to follow an operational amplifier (such as MC1556/MC1456) for driving low impedance loads and improving the overall circuit performance.

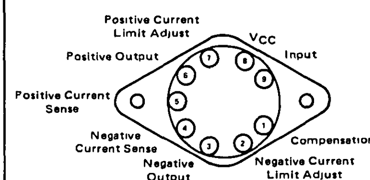
- High Input Impedance – 0.4 Meg-Ohm typ – when driving the MC1538/MC1438, the gain of an operational amplifier will approach the unloaded open-loop gain. Internal power dissipation of the operational amplifier will be independent of output voltage and therefore thermal drift will be reduced.
- Large Power Bandwidth – 1.5 MHz typ – considerably better than present operational amplifiers. Bandwidth and slew rate will be limited by the operational amplifier, not the MC1538/MC1438.
- Low Output Impedance – 10 Ohms typ – allows the MC1538/MC1438 to drive a capacitive load with greatly reduced phase shift compared with an operational amplifier. Output voltage swing capability is much increased when driving small load impedances.
- Adjustable Current Limit – ±5.0 mAdc to ±300 mAdc
- Excellent Power-Supply Rejection – 1.0 mV/V typ
- Current Gain – 3000 typ

OPERATIONAL AMPLIFIERS
POWER BOOSTER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

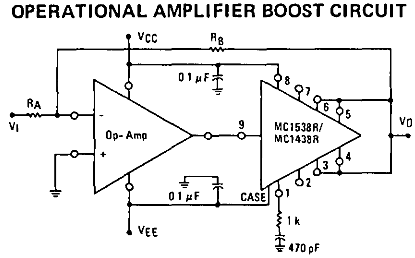


R SUFFIX
CASE 614

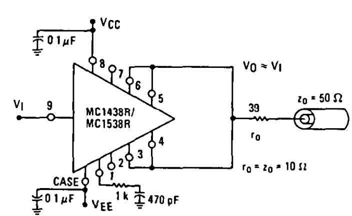


TYPICAL APPLICATIONS

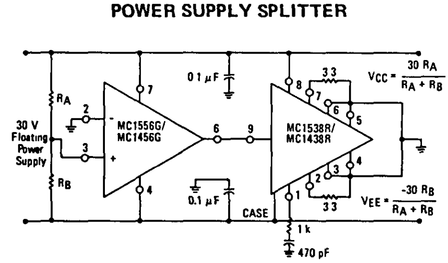
OPERATIONAL AMPLIFIER BOOST CIRCUIT



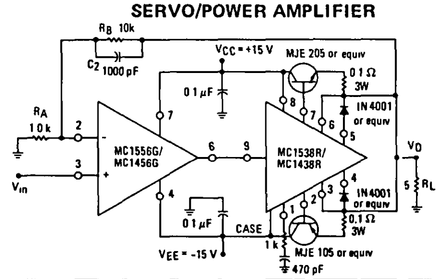
DIGITAL OR ANALOG LINE DRIVER



POWER SUPPLY SPLITTER



SERVO/POWER AMPLIFIER



Under some conditions of circuit layout and loading, the MC1538R/MC1438R will oscillate when driven into current limiting. Oscillation during positive current limiting can usually be suppressed by placing a 0.02 µF capacitor between Pins 7 and 5. Oscillations during negative current limit can usually be suppressed by placing a 0.02 µF capacitor between Pins 1 and 2. 100 Ohms in series with this capacitor will reduce any cross-over distortion occurring when driving extremely low impedance loads.

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	MC1538R	MC1438R	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Input Voltage Swing	$\|V_{in}\|$	V_{CC} or V_{EE}		Vdc
Load Current	I_L	350		mAdc
Power Dissipation @ T_A = +25°C Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	3.0 24		Watts mW/°C
Power Dissipation @ T_C = +25°C Derate above T_C = +25°C	P_D $1/R_{\theta JC}$	17.5 140		Watts mW/°C
Operating Ambient Temperature Range MC1438R MC1538R	T_A	0 to + 70 -55 to +125		°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	41 6	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.15	°C/W

ELECTRICAL CHARACTERISTICS

(R_L = 300 ohms, T_C = +25°C unless otherwise noted.)

				MC1538R 5.0 V ≤ V_{CC} = $\|V_{EE}\|$ ≤ 20 V			MC1438R V_{CC} = +15 V, V_{EE} = -15 V			
Characteristic (Linear Operation)	Fig	Note	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Voltage Gain (f = 1.0 kHz)	1	–	A_V	0 9	0.95	1.0	0.85	0.95	1.0	V/V
Current Gain ($A_I = \Delta I_O/\Delta I_I$)	1	–	A_I	–	3000	–	–	3000	–	A/A
Output Impedance (f = 1.0 kHz)	1	–	z_o	–	10	–	–	10	–	Ohms
Input Impedance (f = 1.0 kHz)	1	–	z_i	–	400	–	–	400	–	k ohms
Output Voltage Swing (See Note 3)	1	3	V_O	±12	±13	–	±11	±12	–	Vdc
Input Bias Current	2	–	I_{IB}	–	60	200	–	60	300	µAdc
Output Offset Voltage	2	1	V_{OO}	–	25	150	–	25	200	mVdc
Small Signal Bandwidth (R_L = 300 ohms) (V_I = 0 Vdc, V_I = 100 mV [rms])	1	–	BW	–	8.0	–	–	8.0	–	MHz
Power Bandwidth (See Note 3) (V_O = 20 V_{p-p}, THD = 5%)	1	–	BW_P	–	1.5	–	–	1.5	–	MHz
Total Harmonic Distortion (Note 3) (f = 1.0 kHz, V_O = 20 V_{p-p})	1	–	THD	–	0.5	–	–	0.5	–	%
Output Short-Circuit Current			I_{OS}							mAdc
(R1 = R2 = ∞)	3	2		75	95	125	65	95	140	
(R1 = R2 = 3.3. ohms)	3			–	300	–	–	300	–	
Adjustable Range	4,5			–	5.0 to 300	–	–	5.0 to 300	–	
Power Supply Sensitivity	2	–	PSRR							mV/V
(V_{EE} constant)				–	1.0	–	–	1.0	–	
(V_{CC} constant)				–	1.0	–	–	1.0	–	
Power Supply Current (R_L ∞, V_I = 0)	2	–	I_{CC} I_{EE}	4.5	6.0	10	2.5	6.0	15	mAdc
Power Dissipation (See Note 3) (R_L ∞, V_I = 0)	2	3	P_C	150	180	300	75	180	450	mW

Note 1. Output offset Voltage is the quiescent dc output voltage with the input grounded.

Note 2. Short-Circuit Current, I_{SC}, is adjustable by varying R1, R2, R3 and R4. The positive current limit is set by R1 or R3, and the negative current limit is set by R2 or R4. See Figures 4 and 5 for curves of short-circuit current versus R1, R2, R3 and R4.

Note 3. V_{CC} = +15 V, V_{EE} = -15 V.

6

TEST CIRCUITS

FIGURE 1

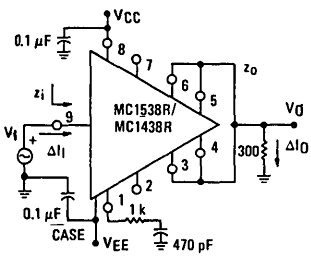


FIGURE 2

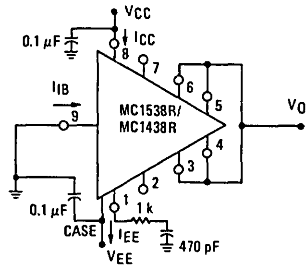
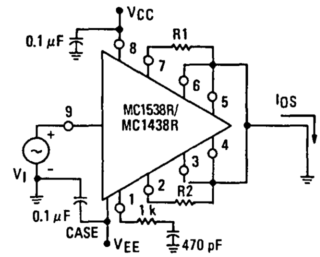
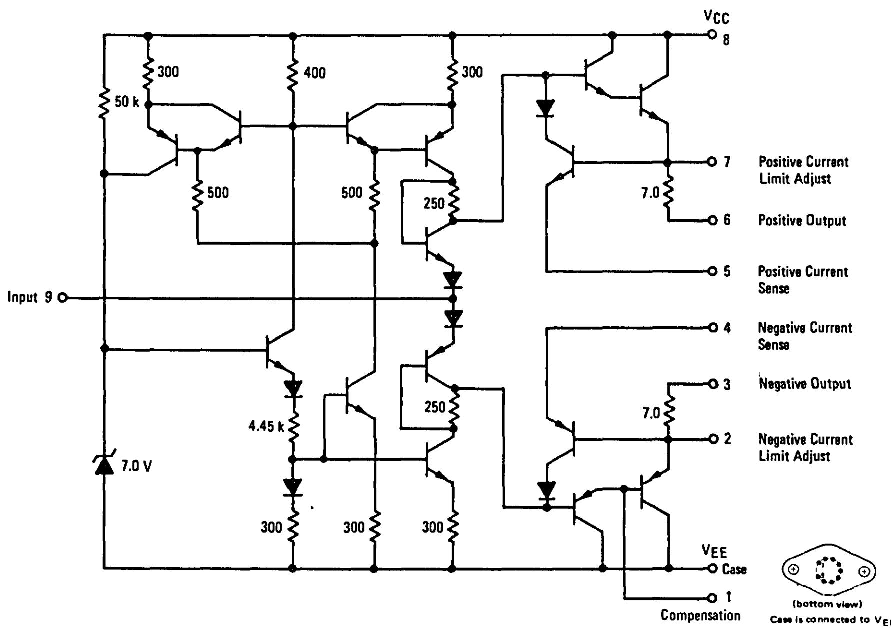


FIGURE 3



CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 4 – SHORT-CIRCUIT CURRENT versus R1 OR R2 (100 mA to 300 mA)

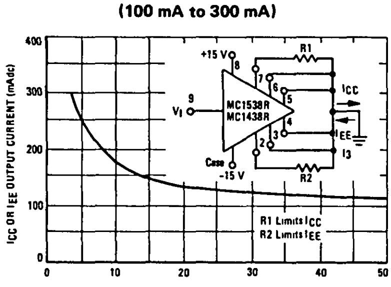
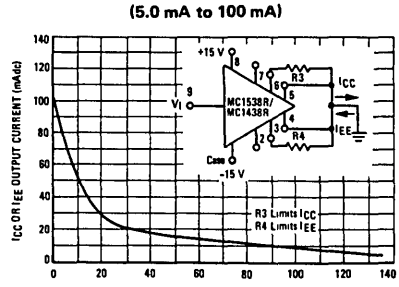


FIGURE 5 – SHORT-CIRCUIT CURRENT versus R3 OR R4 (5.0 mA to 100 mA)



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – POWER SUPPLY CURRENT versus SHUNT RESISTANCE

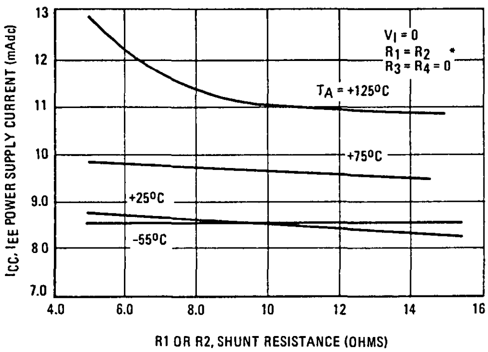


FIGURE 7 – SMALL SIGNAL GAIN AND PHASE RESPONSE

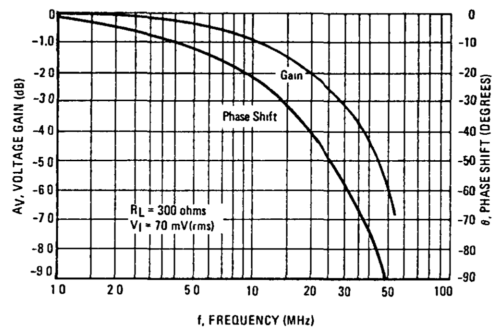


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD CURRENT

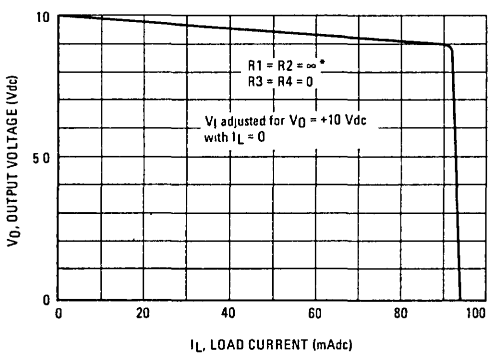


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD CURRENT

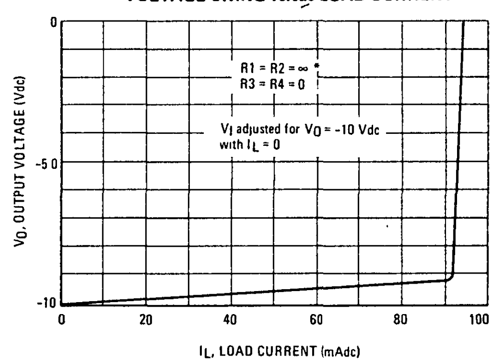


FIGURE 10 – OUTPUT OFFSET VOLTAGE versus TEMPERATURE

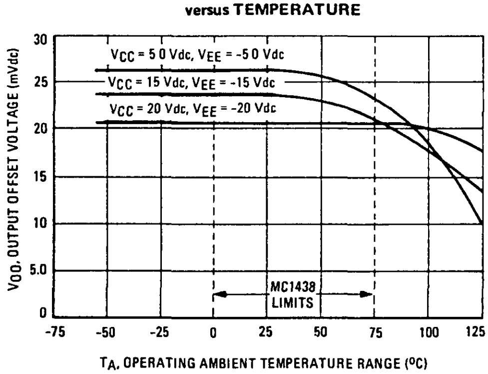
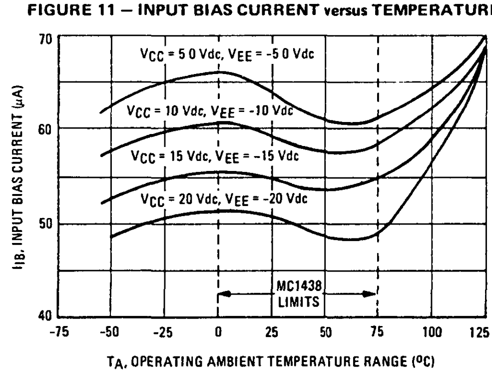


FIGURE 11 – INPUT BIAS CURRENT versus TEMPERATURE



*See figures 4 and 5 for definition of R1, R2, R3, and R4.

6

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 12 – PULSE RESPONSE CHARACTERISTICS

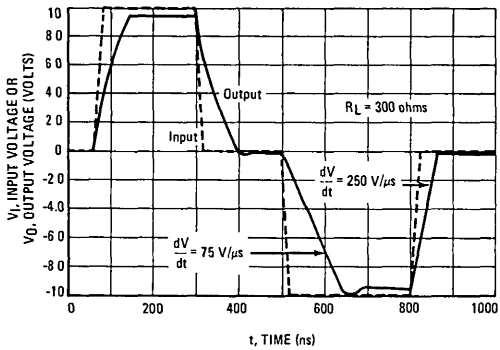
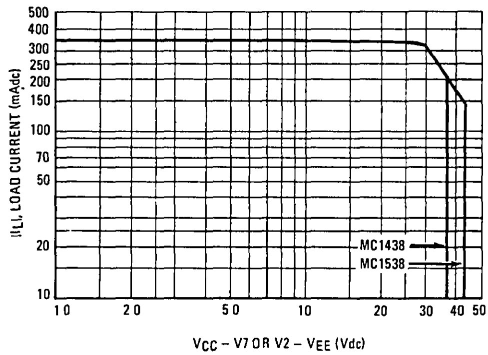


FIGURE 13 – DC SAFE OPERATING AREA



TYPICAL APPLICATIONS

FIGURE 14 – NON-INVERTING AC POWER AMPLIFIER

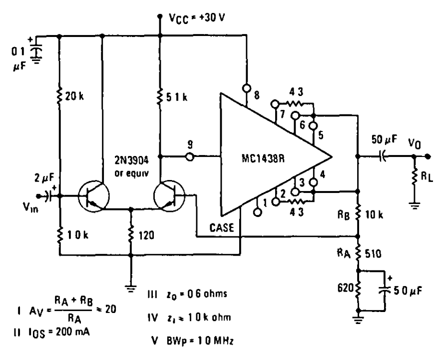


FIGURE 15 – NON-INVERTING POWER AMPLIFIER

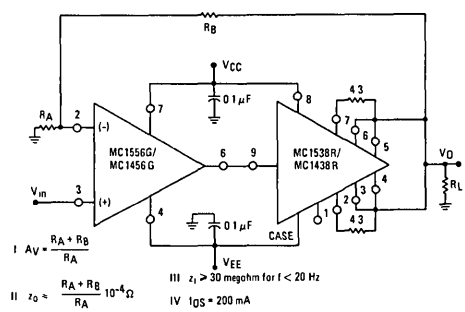


FIGURE 16 – NON-INVERTING VOLTAGE FOLLOWER

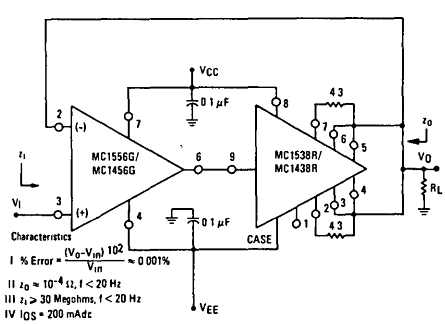
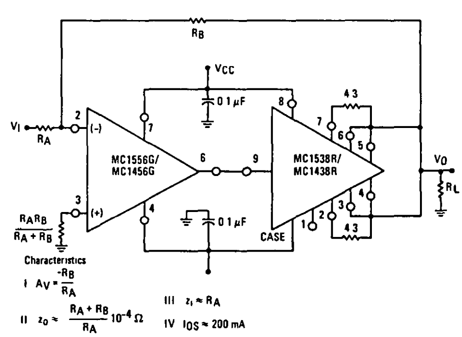
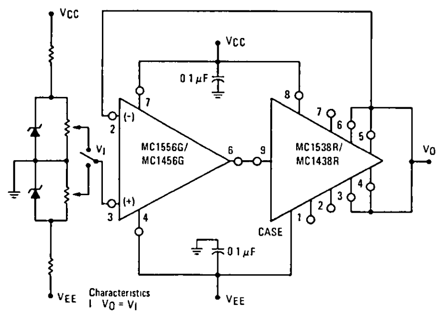


FIGURE 17 – INVERTING POWER AMPLIFIER



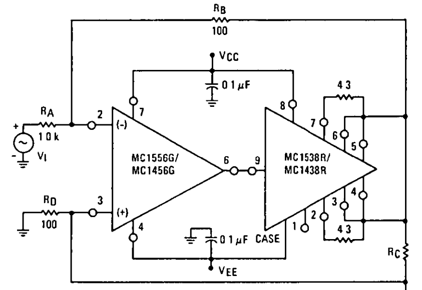
TYPICAL APPLICATIONS (continued)

FIGURE 18 – PROGRAMMABLE VOLTAGE SOURCE



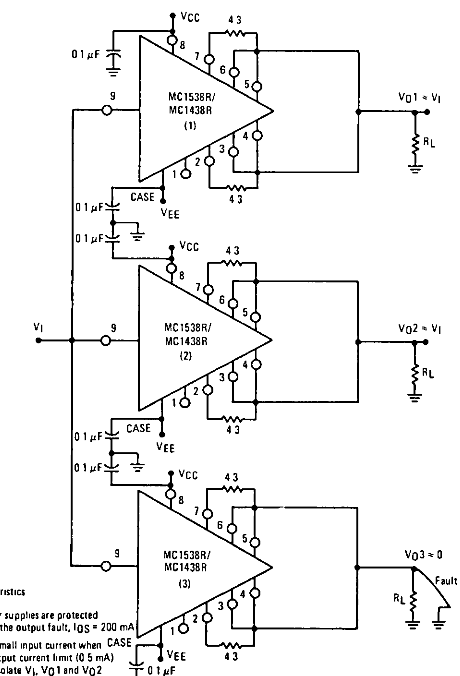
Characteristics
I $V_O = V_I$
II $z_O << 1.0$ milli ohm, f = 20 Hz

FIGURE 19 – CONSTANT CURRENT SOURCE OR TRANSCONDUCTANCE AMPLIFIER



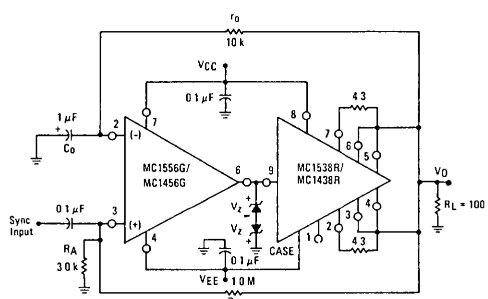
Characteristics
I $\frac{I_L}{V_I} = \frac{1}{R_D} = 10 \frac{mA}{V}$
II For optimum linearity $\frac{R_A}{R_B} = \frac{R_D}{R_C}$

FIGURE 20 – SIGNAL DISTRIBUTION



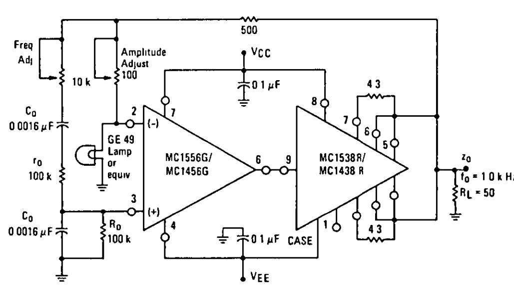
Characteristics
I Power supplies are protected from the output fault, I_{OS} = 200 mA
II The small input current when in output current limit (0.5 mA) will isolate V_I, V_O1 and V_O2 from the fault at V_O3

FIGURE 21 – ASTABLE MULTIVIBRATOR



Characteristics
I $f_0 = \frac{1}{2\ r_0C_0\ \ln(1 + \frac{2R_A}{R_B})}$
II I_{OS} = 200 mA
III $V_{O(pk)} = \pm(V_z + 0.7)$ Volts

FIGURE 22 – WIEN BRIDGE OSCILLATOR



Characteristics
I $f_0 = \frac{1}{2\pi r_0 C_0}$ from 0.01 Hz to 10 kHz
II I_{OS} = 200 mA

ORDERING INFORMATION

Device	Temperature Range	Package
MC1445F	0°C to +75°C	Ceramic Flat
MC1445G	0°C to +75°C	Metal Can
MC1445L	0°C to +75°C	Ceramic DIP
MC1545F	−55°C to +125°C	Ceramic Flat
MC1545G	−55°C to +125°C	Metal Can
MC1545L	−55°C to +125°C	Ceramic DIP

MC1445
MC1545

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

. . . designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN491 for design details.

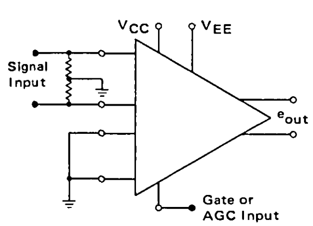
- Large Bandwidth, 50 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

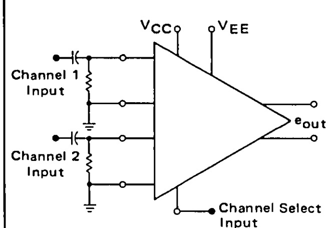
SILICON MONOLITHIC INTEGRATED CIRCUIT

TYPICAL APPLICATIONS

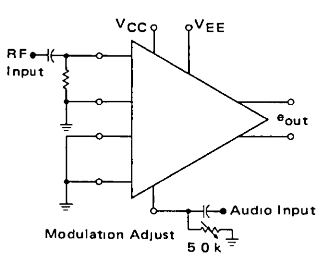
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC



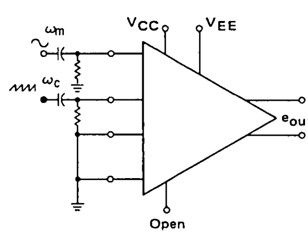
MULTIPLEX OR FSK



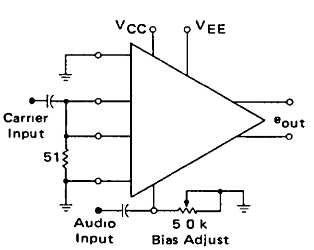
AMPLITUDE MODULATOR



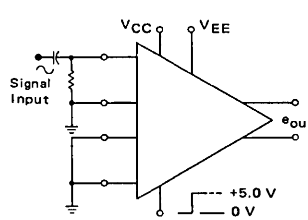
PULSE-WIDTH MODULATOR

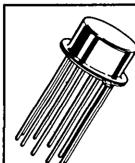


BALANCED MODULATOR

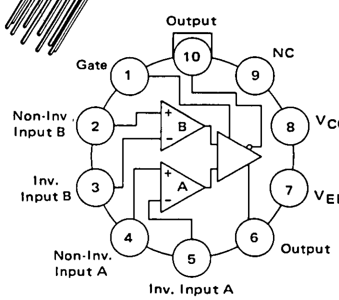


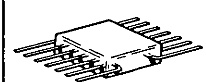
ANALOG SWITCH



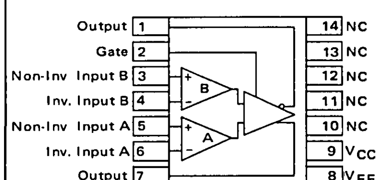


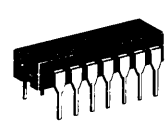
G SUFFIX
METAL PACKAGE
CASE 603
(top view)



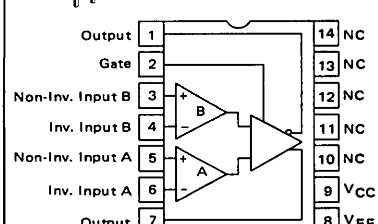


F SUFFIX
CERAMIC PACKAGE
CASE 607





L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+12 -12	Vdc Vdc
Input Differential Voltage Range	V_{IDR}	±5.0	Volts
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Flat Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C Metal Can Derate above T_A = +25°C	P_D	 500 3.3 625 5 0 680 4.6	 mW mW/°C mW mW/°C mW mW/°C
Operating Ambient Temperature Range MC1445 MC1545	T_A	0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 0 Vdc, V_{EE} = 5 0 Vdc, at T_A = +25°C, specifications apply to both input channels unless otherwise noted)

Characteristic	Fig. No.	Symbol	MC1545			MC1445			Unit
			Min	Typ	Max	Min	Typ	Max	
Single-Ended Voltage Gain	1,12	A_{vs}	16	19	21	16	19 5	23	dB
Bandwidth	1,12	BW	40	50	–	–	50	–	MHz
Input Impedance (f = 50 kHz)	5,14	z_i	4 0	10	–	3 0	10	–	k ohms
Output Impedance (f = 50 kHz)	6,15	z_o	–	25	–	–	25	–	Ohms
Output Differential Voltage Range (R_L = 1 0 k ohm, f = 50 kHz)	4,13	V_{ODR}	1 5	2.5	–	1.5	2 5	–	Vp-p
Input Bias Current	16	I_{IB}	–	15	25	–	15	30	μAdc
Input Offset Current	16	I_{IO}	–	2 0	–	–	2 0	–	μAdc
Input Offset Voltage	17	V_{IO}	–	1 0	5.0	–	–	7.5	mVdc
Quiescent Output dc Level	17	V_O	–	0.1	–	–	0.1	–	Vdc
Output dc Level Change (Gate Input Voltage Change +5 0 V to 0 V)	17	ΔV_O	–	±15	–	–	±15	–	mV
Common-Mode Rejection Ratio (f = 50 kHz)	9,18	CMRR	–	85	–	–	85	–	dB
Input Common-Mode Voltage Range	18	V_{ICR}	–	±2 5	–	–	±2 5	–	Vp
Gate Characteristics Gate Input Voltage – Low Logic State (Note 1) Gate Input Voltage – High Logic State (Note 2)	8	$V_{IL(G)}$ $V_{IH(G)}$	0.40 –	0.70 1.5	– 2.2	0 2 –	0.4 1 3	– 3 0	Vdc
Gate Input Current – Low Logic State ($V_{IL(G)}$ = 0 V)	18	$I_{IL(G)}$	–	–	2 5	–	–	4.0	mA
Gate Input Current – High Logic State ($V_{IH(G)}$ = +5.0 V)	18	$I_{IH(G)}$	–	–	2.0	–	–	4 0	μA
Step Response (e_{in} = 20 mV)	19	t_{PLH} t_{PHL} t_{TLH} t_{THL}	– – – –	6 5 6.3 6.5 7.0	10 10 15 15	– – – –	6.5 6 3 6 5 7 0	– – – –	ns
Wideband Input Noise (5.0 Hz – 10 MHz, R_S = 50 ohms)	10,20	e_n	–	25	–	–	25	–	μV(rms)
DC Power Consumption	11,20	P_C	–	70	110	–	70	150	mW

Note 1. $V_{IL(G)}$ is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
Note 2. $V_{IH(G)}$ is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

FIGURE 1 – SINGLE-ENDED VOLTAGE GAIN versus FREQUENCY

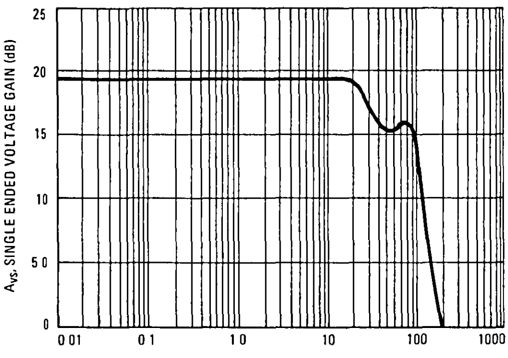


FIGURE 2 – SINGLE-ENDED VOLTAGE GAIN versus TEMPERATURE

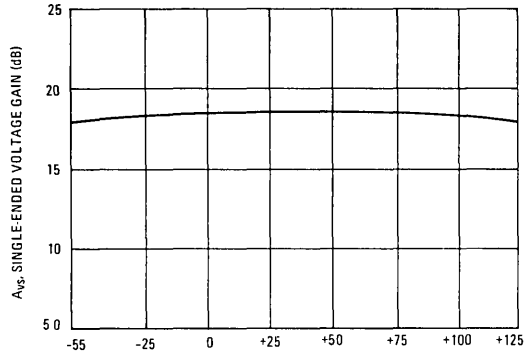


FIGURE 3 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGES

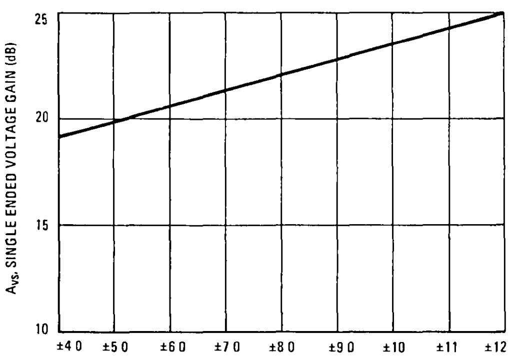


FIGURE 4 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

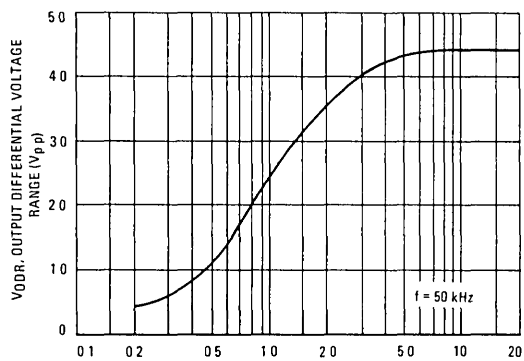


FIGURE 5 – INPUT Cp AND Rp versus FREQUENCY (BOTH CHANNELS)

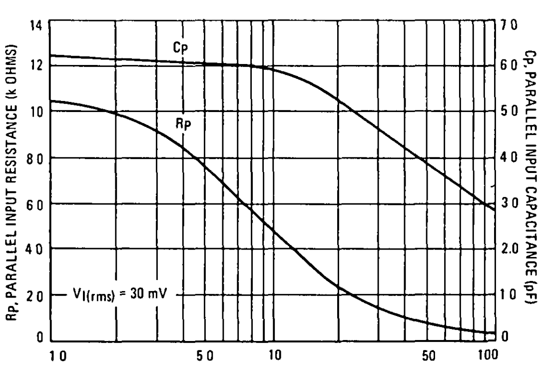


FIGURE 6 – OUTPUT IMPEDANCE versus FREQUENCY

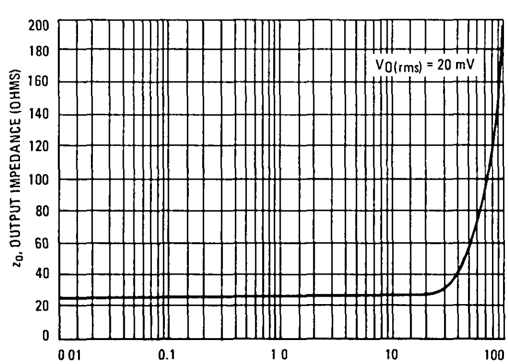


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FIGURE 7 – CHANNEL SEPARATION versus FREQUENCY

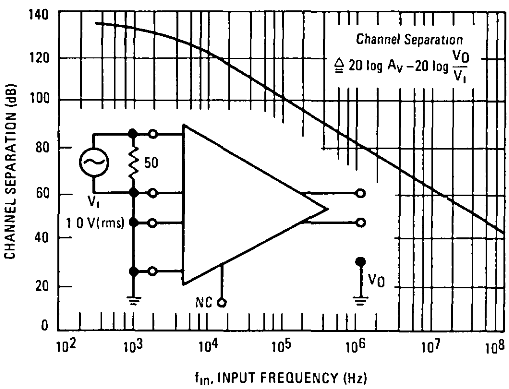


FIGURE 8 – GATE CHARACTERISTICS

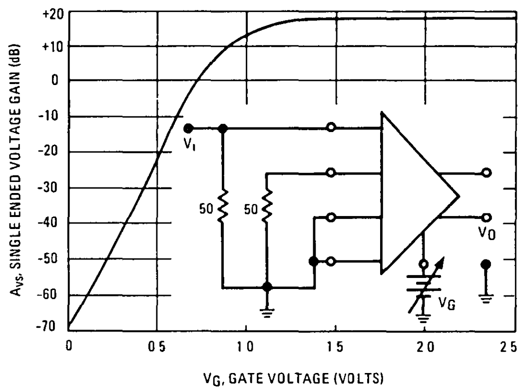


FIGURE 9 – COMMON MODE REJECTION RATIO versus FREQUENCY

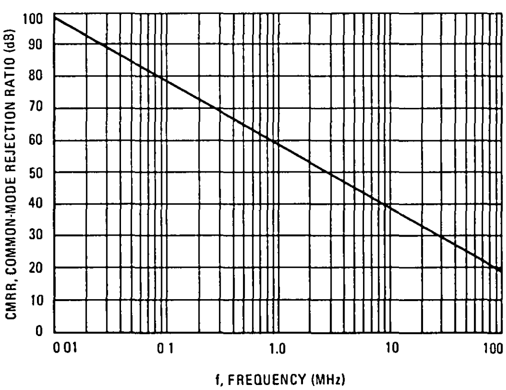


FIGURE 10 – INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

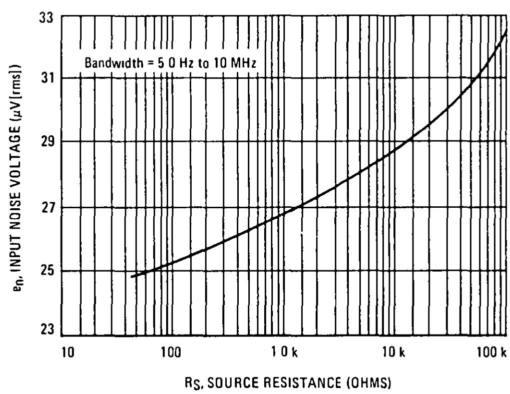


FIGURE 11 – CIRCUIT SCHEMATIC

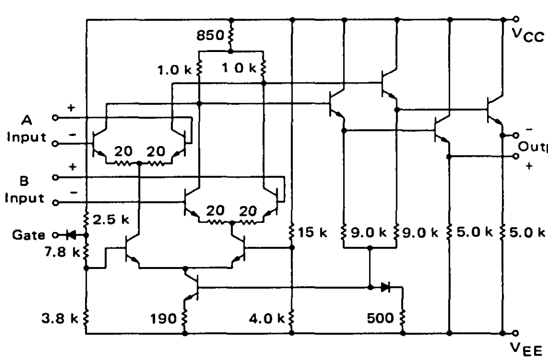
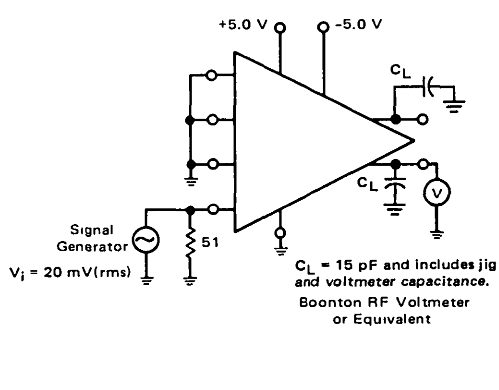


FIGURE 12 – SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT



6

FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

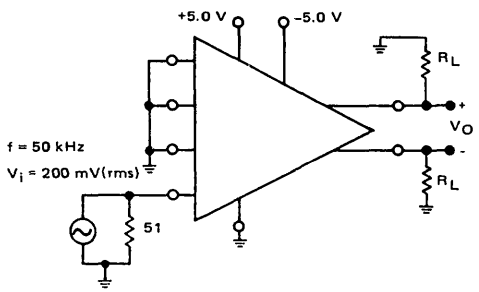


FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

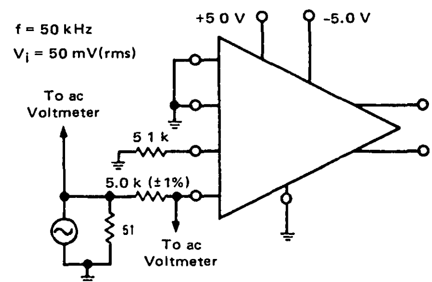


FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

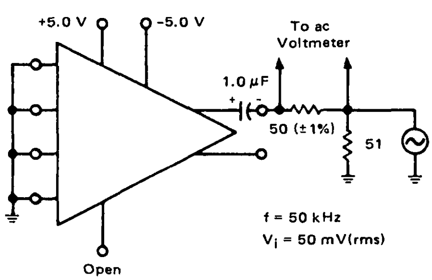


FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT

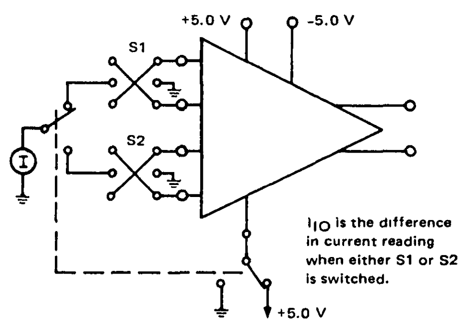


FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT

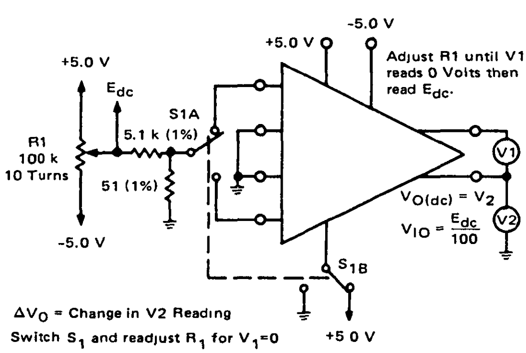


FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT

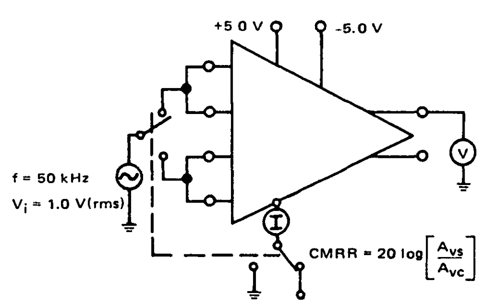
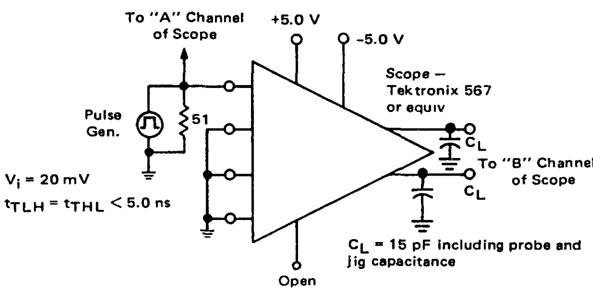


FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT



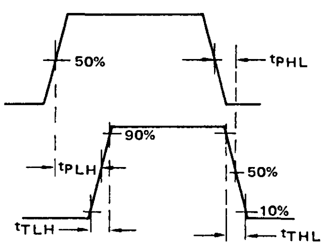


FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT

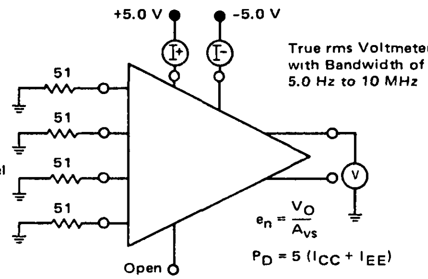
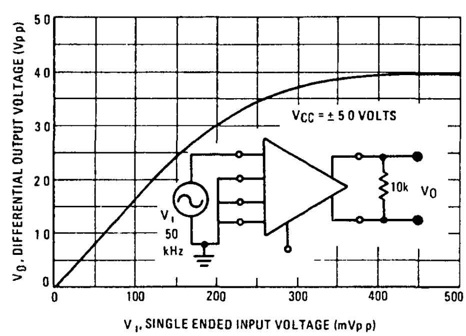


FIGURE 21 – LIMITING CHARACTERISTIC



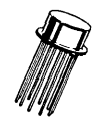
ORDERING INFORMATION

Device	Temperature Range	Package
MC1550F	−55°C to +125°C	Ceramic Flat
MC1550G	−55°C to +125°C	Metal Can

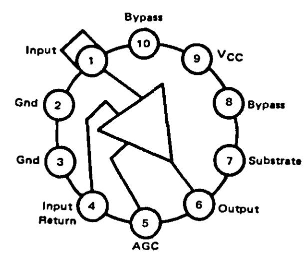
MC1550G

RF – IF AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 603B



RF – IF AMPLIFIER

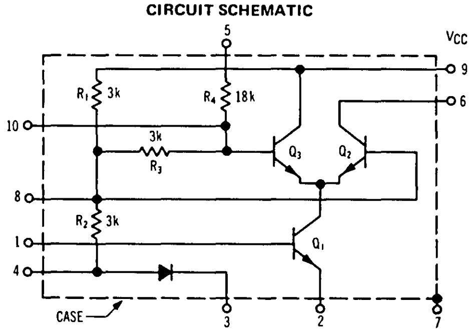
. . . a versatile, common-emitter, common-base cascode circuit for use in communications applications. See Application Note AN-215A for additional information.

- Constant Input Impedance over entire AGC range
- Extremely Low y_{12} – 4.3 μmhos at 60 MHz
- High Power Gain – 30 dB @ 60 MHz (0.5 MHz BW)
- Good Noise Figure – 5 dB @ 60 MHz

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V_{CC}	20	Vdc
AGC Supply Voltage	V_{AGC}	20	Vdc
Input Differential Voltage, Pin 1 to Pin 4 (R_S = 500 ohms)	V_{ID}	±5.0	V(rms)
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1550 is built with monolithic fabrication techniques utilizing diffused resistors and small–geometry transistors. Excellent AGC performance is obtained by shunting the signal through the AGC transistor Q_3 maintaining the operating point of the input transistor Q_1. This keeps the input impedance constant over the entire AGC range.

The amplifier is intended to be used in a common-emitter, common-base configuration (Q_1 and Q_2) with Q_3 acting as an AGC transistor. The input signal is applied between pins 1 and 4, where pin 4 is ac-coupled to ground. DC source resistance between pins 1 and 4 should be small (less than 100 ohms). Pins 2 and 3 should be connected together and grounded. Pins 8 and 10 should be bypassed to ground. The positive supply voltage is applied at pin 9 and at higher frequencies, pin 9 should also be bypassed to ground. The output is taken between pins 6 and 9. The substrate is connected to pin 7 and should be grounded. AGC voltage is applied to pin 5.

ELECTRICAL CHARACTERISTICS (V^+ = +6 Vdc, T_A = +25°C)

Characteristic	Conditions	Figure	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS							
Output Voltage	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	V_O	3.80 5.90	– –	4.65 6.00	Vdc
Test Voltage	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	V8	2.85 3.25	– –	3.40 3.80	Vdc
Supply Drain Current	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	I_D	– –	– –	2.2 2.5	mAdc
AGC Supply Drain Current	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	I_{AGC}	– –	– –	-0.2 0.18	mAdc
SMALL-SIGNAL CHARACTERISTICS							
Small-Signal Voltage Gain	f = 500 kHz	2	A_V	22	–	29	dB
Bandwidth	-3 0 dB	2	BW	22	–	–	MHz
Transducer Power Gain	f = 60 MHz, BW = 6 MHz f = 100 MHz, BW = 6 MHz	3	Ap	– –	25 21	– –	dB

TYPICAL CHARACTERISTICS

(V_{CC} = 6 0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 1 – DC CHARACTERISTICS TEST CIRCUIT

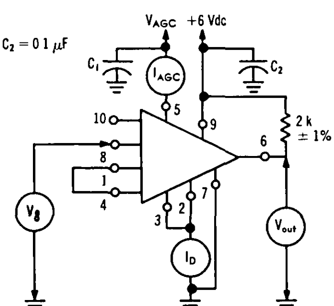


FIGURE 2 – VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT

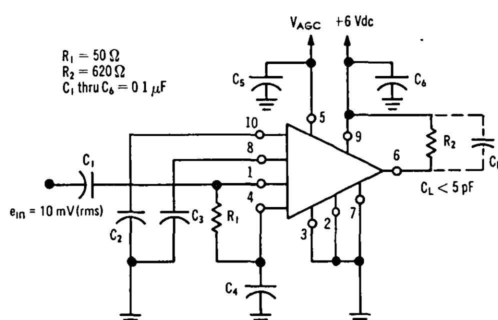


FIGURE 3 – POWER GAIN TEST CIRCUIT @ 60 MHz

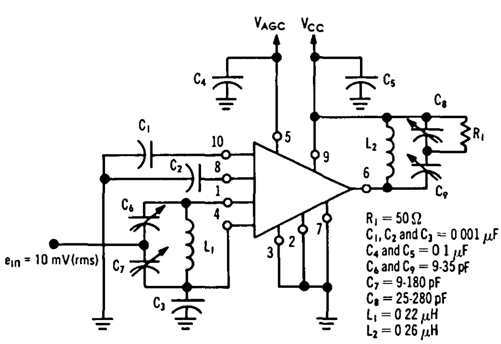
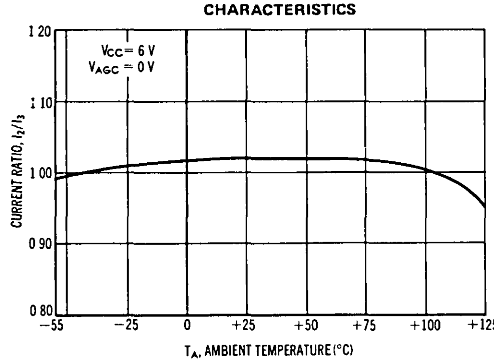


FIGURE 4 – DRAIN CURRENT TEMPERATURE CHARACTERISTICS



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TYPICAL CHARACTERISTICS (continued)

FIGURE 5 – INPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

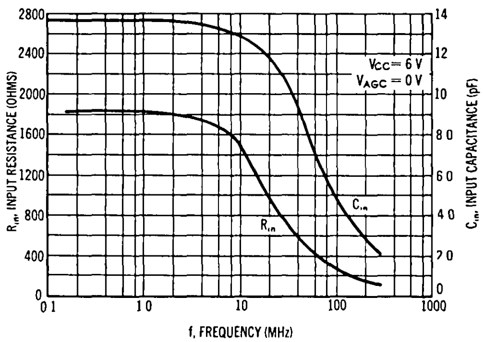


FIGURE 6 – INPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

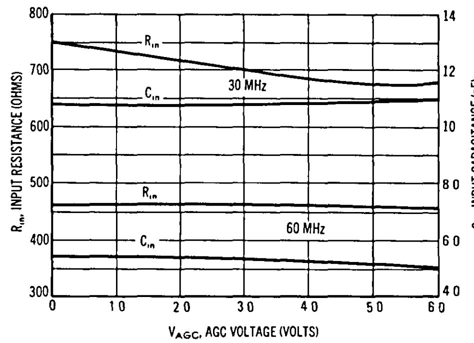


FIGURE 7 – OUTPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

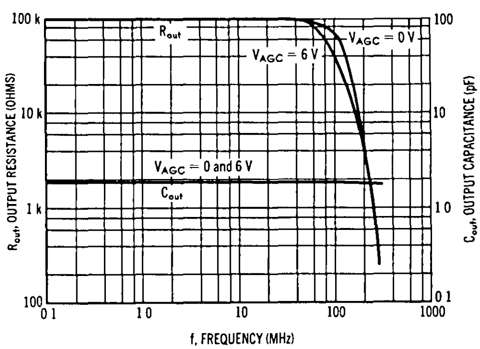


FIGURE 8 – OUTPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

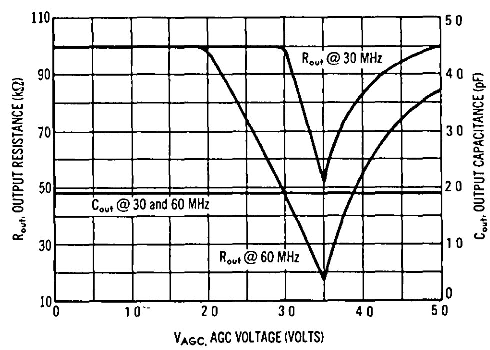


FIGURE 9 – MAXIMUM TRANSDUCER POWER GAIN versus FREQUENCY

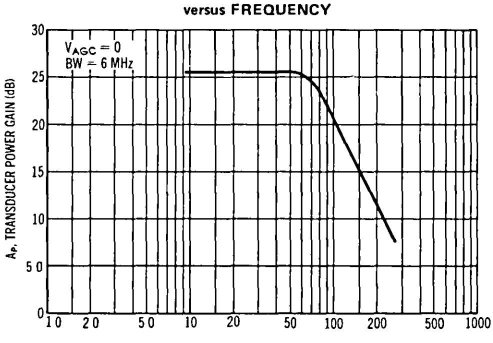
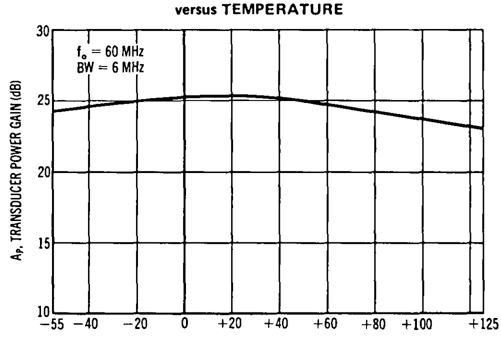


FIGURE 10 – TRANSDUCER POWER GAIN versus TEMPERATURE



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TYPICAL CHARACTERISTICS (continued)

FIGURE 11 – TRANSDUCER POWER BANDWIDTH versus AGC VOLTAGE

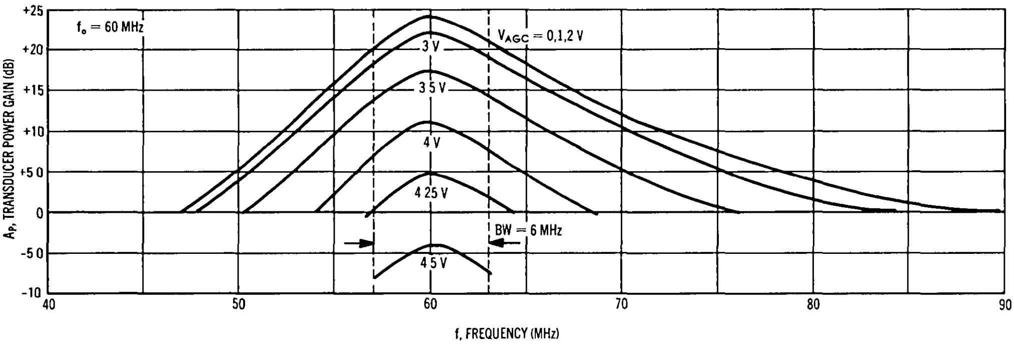


FIGURE 12 – NOISE FIGURE AND OPTIMUM SOURCE RESISTANCE versus FREQUENCY

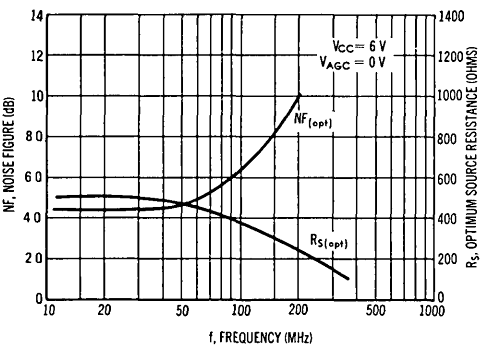


FIGURE 13 – NOISE FIGURE versus SOURCE RESISTANCE

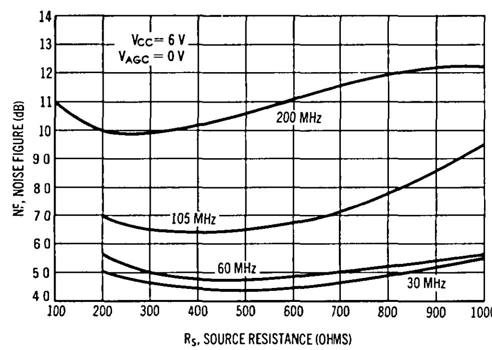


FIGURE 14 – y_{21}, FORWARD-TRANSFER ADMITTANCE versus FREQUENCY

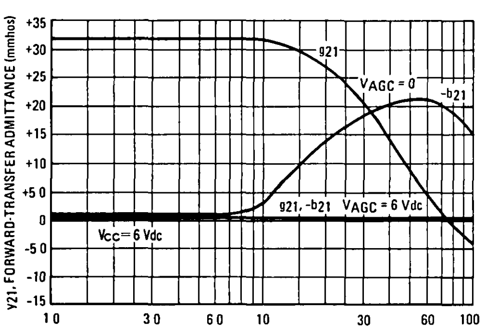
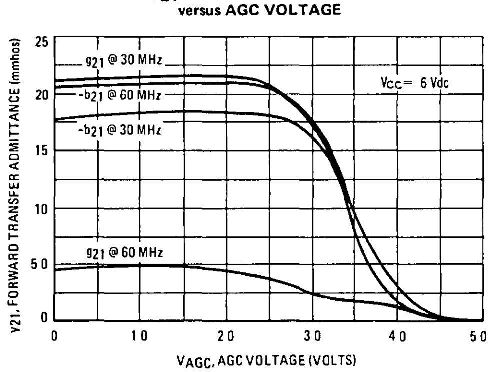


FIGURE 15 – y_{21}, FORWARD-TRANSFER ADMITTANCE versus AGC VOLTAGE



6

TYPICAL CHARACTERISTICS

(V_{CC} = 6 0-Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 16 – y_{12}, REVERSE TRANSFER-ADMITTANCE versus FREQUENCY

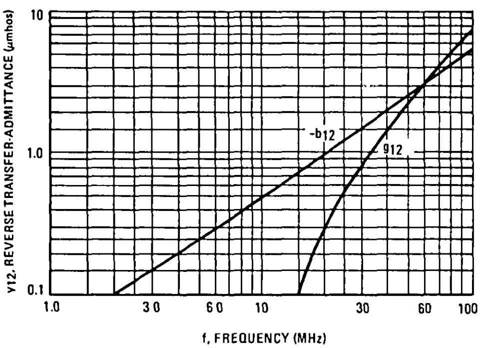


FIGURE 17 – y_{11}, INPUT-ADMITTANCE versus FREQUENCY

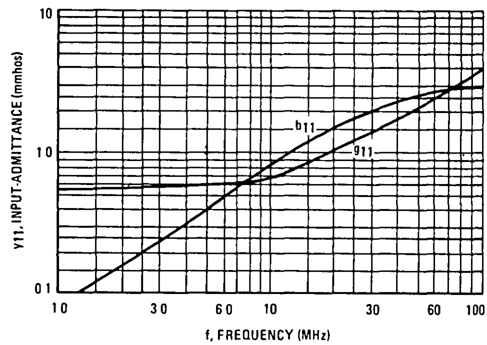
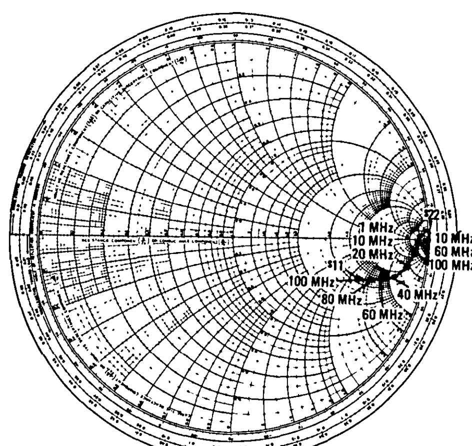


FIGURE 19 – s_{11} AND s_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT



The y_{12} shown in Figure 16 illustrates the extremely low feedback of the MC1550 with no contribution from the external mounting circuitry However, in many cases the external circuitry may contribute as much or more to the total feedback than does the MC1550

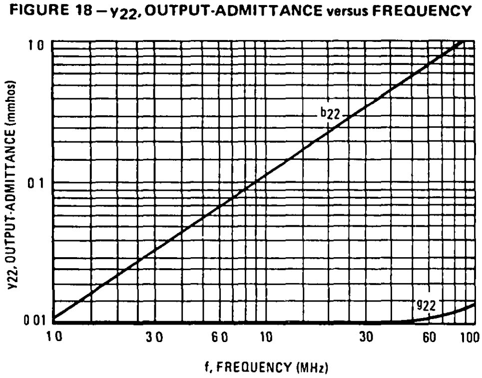
To perform more accurate design calculations of gain, stability, and input - output impedances it is recommended that the designer first determine the total feed back of device plus circuitry

This can be done in one of two ways

(1) Measure the total y_{12} or s_{12} of the MC1550 installed in its mounting circuitry, or

(2) Measure the y_{12} of the circuitry alone (without the MC1550 installed) and add the circuit y_{12} to the y_{12} for the MC1550 given in Figure 16

FIGURE 18 – y_{22}, OUTPUT-ADMITTANCE versus FREQUENCY



6

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = 6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 20 – s_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY

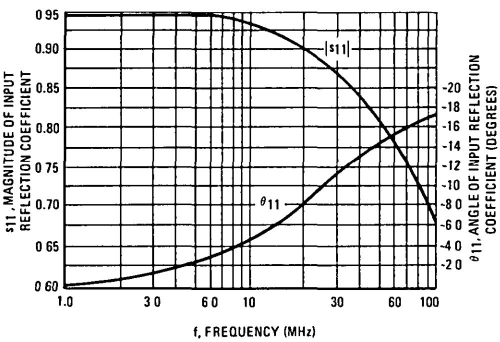


FIGURE 21 – s_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

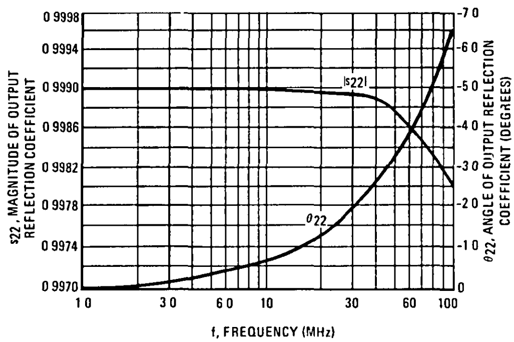


FIGURE 22 – s_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

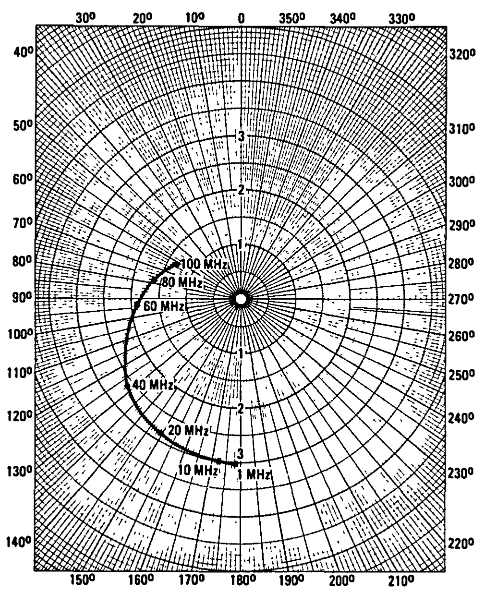
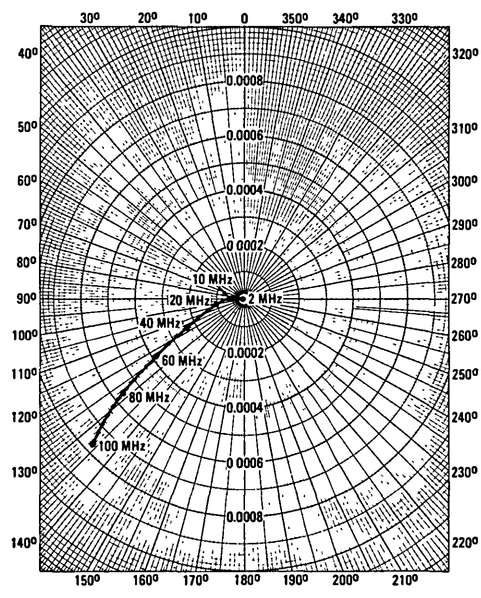


FIGURE 23 – s_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



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ORDERING INFORMATION

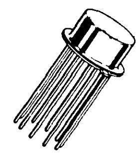
Device	Temperature Range	Package
MC1552G	−55°C to +125°C	Metal Can
MC1553G	−55°C to +125°C	Metal Can

MC1552G
MC1553G

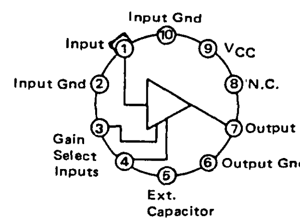
HIGH FREQUENCY VIDEO AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

CASE 603B
METAL PACKAGE



PIN CONNECTIONS



(Top View)

VIDEO AMPLIFIERS

These devices consist of a three-stage, direct-coupled, common-emitter cascade incorporating series feedback to achieve stable voltage gain, low distortion, and wide bandwidth. They employ a temperature-compensated dc feedback loop to stabilize the operating point and a current-biased emitter follower output and are intended for use as either wide-band linear amplifiers or as fast rise pulse amplifiers.

- High Gain – 34 dB ± 1 dB (MC1552)
  52 dB ± 1 dB (MC1553)
- Wide Bandwidth – 40 MHz (MC1552)
  35 MHz (MC1553)
- Low Distortion – 0.2% at 200 kHz
- Low Temperature Drift – ±0.002 dB/°C

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V_{CC}	9.0	Vdc
Input Differential Voltage, Pin 1 to Pin 2 (R_S = 500 ohms)	V_{ID}	1.0	V(rms)
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6	mW mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

REPRESENTATIVE CIRCUIT SCHEMATICS

FIGURE 1 – MC1552 (LOW GAIN)

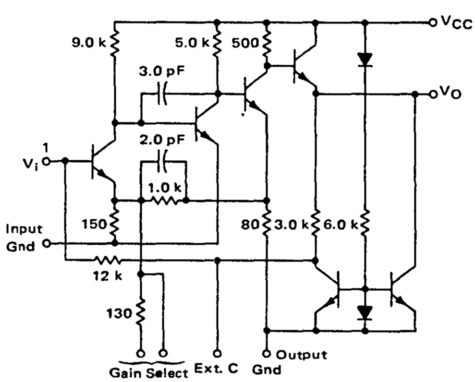
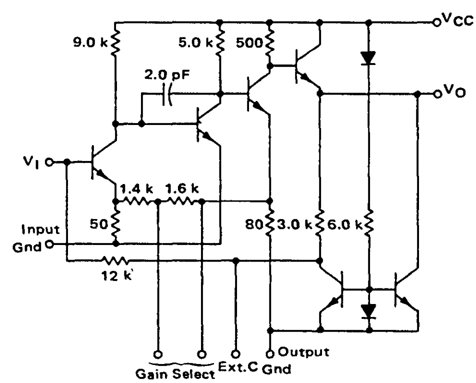


FIGURE 2 – MC1553 (HIGH GAIN)



ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_A = 25°C, V_{CC} = 6 0 V and specification applies for all Gain Selection options

Characteristic	Test Figure	Symbol	MC1552G Min	MC1552G Typ	MC1552G Max	MC1553G Min	MC1553G Typ	MC1553G Max	Unit
Voltage Gain	3	A_V							V/V
(Gain Option = 50)			44	50	56	–	–	–	
(Gain Option = 100)			87	100	113	–	–	–	
(Gain Option = 200)			–	–	–	175	200	225	
(Gain Option = 400)			–	–	–	350	400	450	
$-55°C \le T_A \le 125°C$									
(Gain Option = 50)			42	–	58	–	–	–	
(Gain Option = 100)			83	–	117	–	–	–	
(Gain Option = 200)			–	–	–	171	–	230	
(Gain Option = 400)			–	–	–	342	–	461	
Voltage Gain Variation ($-55°C \le T_A \le 125°C$)	3	ΔA_V	–	±0 2	–	–	±0 2	–	dB
Small-Signal Bandwidth	3,6	BW							MHz
(Gain Option = 50)			21	40	–	–	–	–	
(Gain Option = 100)			17	35	–	–	–	–	
(Gain Option = 200)			–	–	–	17	35	–	
(Gain Option = 400)			–	–	–	7 5	15	–	
Input Impedance (f = 100 kHz, R_L = 1 0 kΩ)		z_i	7 0	10	–	7 0	10	–	kΩ
Output Impedance (f = 100 kHz, R_S = 50 Ω)		z_o	–	16	50	–	16	50	Ω
DC Output Voltage	3	V_O	2 5	2 9	3 2	2 5	2 9	3 2	Vdc
($-55°C \le T_A \le 125°C$)			2 3	–	3.4	2.4	–	3 3	
DC Output Voltage Variation ($-55°C \le T_A \le 125°C$)	3	ΔV_O	–	±0 05	–	–	±0 05	–	Vdc
Output Voltage Range ($z_L \le$ 1 0 kΩ, C_i = 100 mV rms)	3	V_{OR}	3 6	4 2	–	3 6	4 2	–	V p p
($-55°C \le T_A \le 125°C$)						3 4			
Power Supply Current	–	I_{CC}	–	12 5	20	–	12 5	20	mA
($-55°C \le T_A \le 125°C$)			–	–	24	–	–	23	
Propagation Delay Time	3,4	t_{PHL}							ns
(Gain Option = 50)			–	8 0	–	–	–	–	
(Gain Option = 100)			–	9 0	–	–	–	–	
(Gain Option = 200)			–	–	–	–	10	–	
(Gain Option = 400)			–	–	–	–	25	–	
Transition (Rise) Time	3,4	t_{THL}							ns
(Gain Option = 50)			–	9 0	16	–	–	–	
(Gain Option = 100)			–	12	20	–	–	–	
(Gain Option = 200)			–	–	–	–	11	20	
(Gain Option = 400)			–	–	–	–	30	45	
Overshoot	3,4	100 V_{OS}/V_P	–	5 0	–	–	5 0	–	%
Noise Figure (R_S = 400 Ω, f_o = 30 MHz, BW = 3 0 MHz) (See Figure 14)	–	NF	–	3 0	–	–	3 0	–	dB
Total Harmonic Distortion (V_o = 2.0 V p-p, f = 200 kHz, R_L = 1 0 kΩ)	–	THD	–	0 2	–	–	0 2	–	%

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NOTES

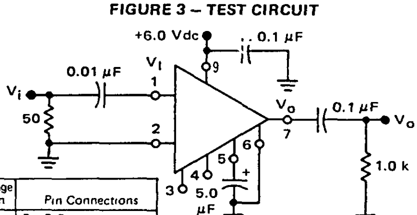
1. Ground Pin 6 as close to package as possible to minimize overshoot. Best results are usually obtained by directly grounding the package.
2. If large input and output coupling capacitors are used, place a shield between them to avoid input-output coupling.
3. A high-frequency capacitor must always be used to by-pass the power supply. This capacitor should be as close to the circuit as possible.
4. Voltage gain can be adjusted to any value between 50 and 3000 by connecting an external resistor from Pin 4 to ground on MC1552, or from Pin 3 to ground on MC1553, as shown in Figure 8. Under these conditions, the following equations must be used to determine C1 and C2 rather than the circuits shown in Figure 5.

Fig. 5b $C1 = \frac{1}{2\pi f_c(1.7 \times 10^4)}$ Farads; $C2 = 8\,C1(V_o/V_i)$ Farads

Fig. 5c $C1 = \frac{V_o/V_i}{2\pi f_c(1.5 \times 10^4)}$ Farads

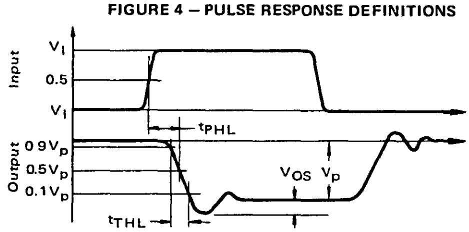
Fig. 5d $C2 = \frac{V_o/V_i}{2\pi f_c(3 \times 10^3)}$ Farads

FIGURE 3 – TEST CIRCUIT



Type	Voltage Gain	Pin Connections
MC1552	50	Pin 3 Open
	100	Ground Pin 3
MC1553	200	Connect Pin 3 to Pin 4
	400	Pins 3 and 4 Open

FIGURE 4 – PULSE RESPONSE DEFINITIONS



TYPICAL CHARACTERISTICS

$T_A = +25^oC$

FIGURE 5a – FREQUENCY RESPONSE

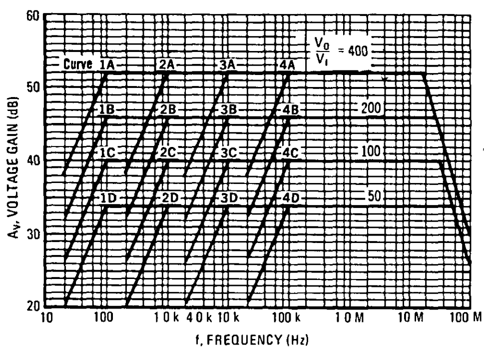
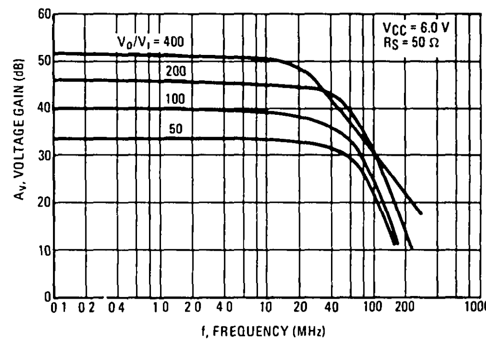
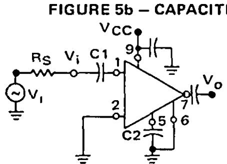


FIGURE 6 – VOLTAGE GAIN versus FREQUENCY



TEST CIRCUITS FOR FREQUENCY RESPONSE

FIGURE 5b – CAPACITIVE COUPLED INPUT (R_s < 5 kΩ)



Curve No.	C1 (μF)	C2 (μF)
1A	0.1	250
1B	0 1	150
1C	0.1	70
1D	0.1	40

Curve No.	C1 (μF)	C2 (μF)
2A	0.01	30
2B	0 01	18
2C	0.01	8.0
2D	0.01	4.0
	(pF)	
3A	1000	3.0
3B	1000	1.8
3C	1000	0 8
3D	1000	0 4
4A	100	0.3
4B	100	0.18
4C	100	0.08
4D	100	0 04

FIGURE 7 – MAXIMUM NEGATIVE SWING SLEW RATE versus LOAD CAPACITANCE

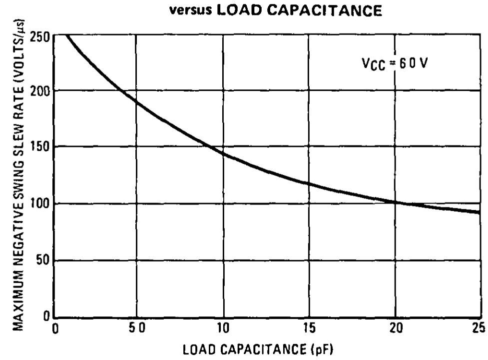
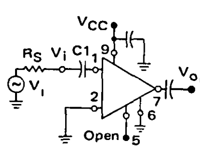


FIGURE 5c – CAPACITIVE COUPLED INPUT (R_s <500 Ω)



Curve No.	C1 (μF)	Curve No.	C1 (μF)
1A	20	3A	0.4
1B	10	3B	0.2
1C	7.0	3C	0.1
1D	3.0	3D	0.06
2A	3.0	4A	0.04
2B	1.0	4B	0.02
2C	0.8	4C	0.01
2D	0.5	4D	0.007

FIGURE 8 – VOLTAGE GAIN ADJUSTMENT BY USE OF EXTERNAL RESISTOR

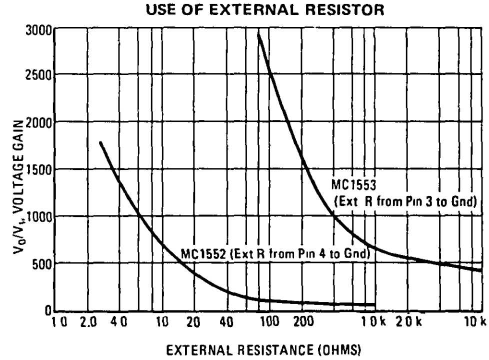
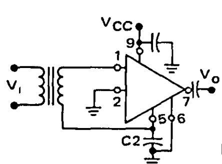


FIGURE 5d – TRANSFORMER COUPLED INPUT



Curve No.	C2 (μF)	Curve No.	C1 (μF)
1A	200	3A	2.0
1B	100	3B	1.0
1C	70	3C	0.7
1D	30	3D	0.3
2A	20	4A	0.2
2B	10	4B	0.1
2C	7.0	4C	0.07
2D	3.0	4D	0.03

6

INPUT ADMITTANCE

(V_{CC} = 6.0 Vdc, R_L = 1.0 kΩ, T_A = +25°C)

FIGURE 9 – GAIN = 50

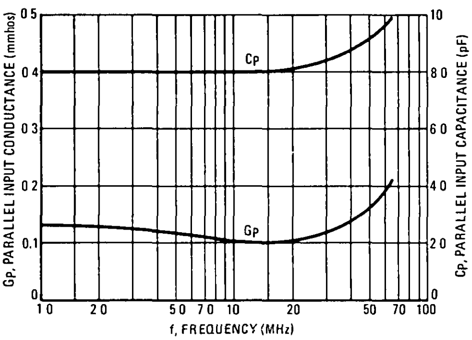


FIGURE 10 – GAIN = 100

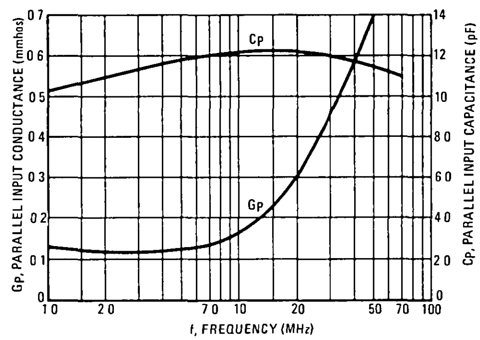


FIGURE 11 – GAIN = 200

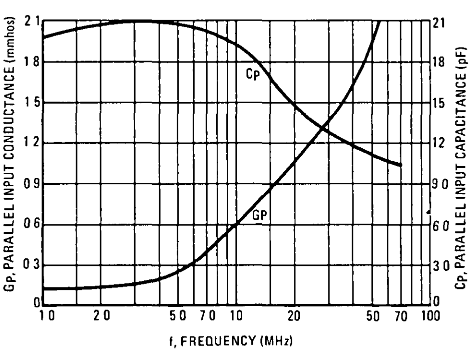


FIGURE 12 – GAIN = 400

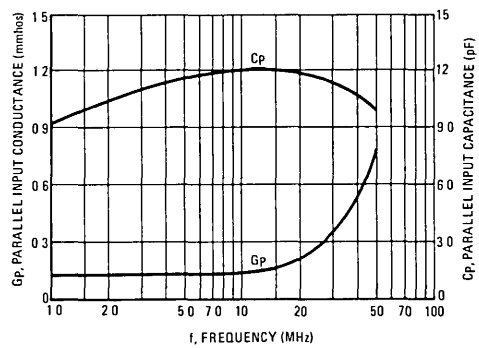


FIGURE 13 – OUTPUT IMPEDANCE versus FREQUENCY

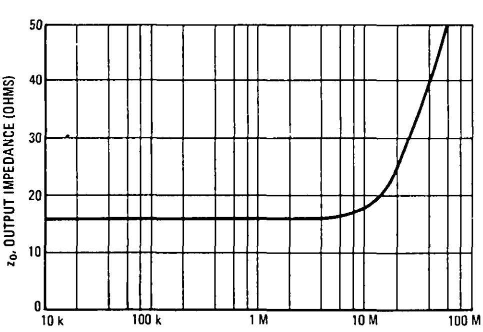
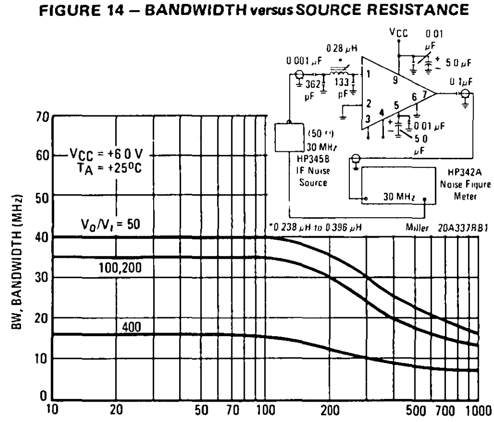


FIGURE 14 – BANDWIDTH versus SOURCE RESISTANCE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1454G	0°C to +70°C	Metal Can
MC1554G	−55°C to +125°C	Metal Can

MC1454G
MC1554G

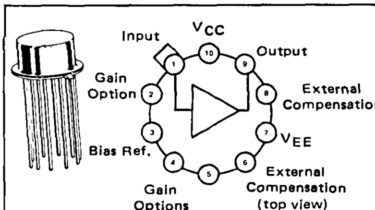
1-WATT POWER AMPLIFIERS

. . . designed to amplify signals to 300-kHz with 1-Watt delivered to a direct coupled or capacitively coupled load.

- Low Total Harmonic Distortion – 0.4% (Typ) @ 1 Watt
- Low Output Impedance – 0.2 Ohm
- Excellent Gain – Temperature Stability

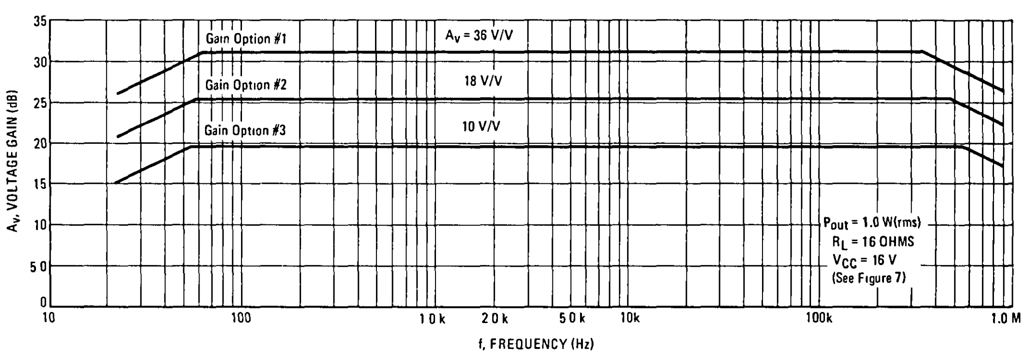
1-WATT POWER AMPLIFIER INTEGRATED CIRCUIT

SILICON MONOLITHIC EPITAXIAL PASSIVATED

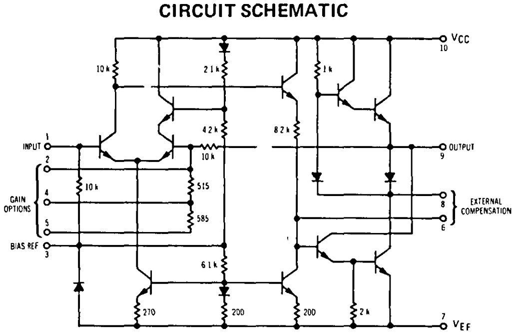


G SUFFIX
CASE 603B

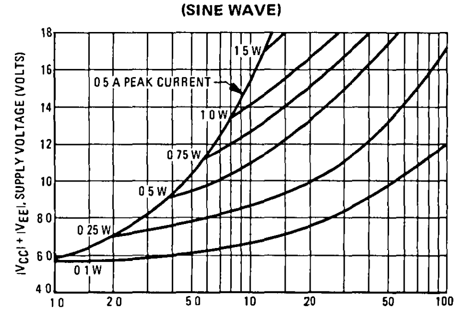
VOLTAGE GAIN versus FREQUENCY (R_L = 16 OHMS)



CIRCUIT SCHEMATIC



MAXIMUM AVAILABLE OUTPUT POWER (SINE WAVE)



ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)
Frequency compensation shown in Figures 6 and 7.

Characteristic	Figure	R_L (Ohms)	Gain Option*	Symbol	MC1554 (-55 to +125°C) Min	MC1554 Typ	MC1554 Max	MC1454 (0 to +70°C) Min	MC1454 Typ	MC1454 Max	Unit
Output Power (for e_{out}<5.0% THD)	1	16	–	P_{out}	1.0	1.1	–	–	1.0	–	Watt
Power Dissipation (@ P_{out} = 1.0 W)	1	16	–	P_D	–	0.9	1.2	–	0.9	–	Watt
Voltage Gain	1	16	10	A_V	8.0	10	12	–	10	–	V/V
		16	18		–	18	–	–	18	–	
		16	36		–	36	–	–	36	–	
Input Impedance	1	–	10	z_{in}	7.0	10	–	3.0	10	–	kΩ
Output Impedance	1	–	10	z_o	–	0.2	–	–	0.4	–	Ω
Power Bandwidth (for e_{out}<5.0% THD)	2	16	10	BW	–	270	–	–	270	–	kHz
		16	18		–	250	–	–	250	–	
		16	36		–	210	–	–	210	–	
Total Harmonic Distortion (for e_{in}<0.05% THD, f = 20 Hz to 20 kHz)	2			THD							%
P_{out} = 1.0 Watt (sinewave)		16	10		–	0.4	–	–	0.4	–	
P_{out} = 0.1 Watt (sinewave)		16	10		–	0.5	–	–	0.5	–	
Zero Signal Current Drain	3	∞	–	I_D	–	11	15	–	11	20	mAdc
Output Noise Voltage	3	16	10	V_n	–	0.3	–	–	0.3	–	mV(rms)
Output Quiescent Voltage (Split Supply Operation)	4	16	–	V_o (dc)	–	±10	±30	–	±10	–	mVdc
Positive Supply Sensitivity (V_{EE} constant)	5	∞	–	S^+	–	-40	–	–	-40	–	mV/V
Negative Supply Sensitivity (V_{CC} constant)	5	∞	–	S^-	–	-40	–	–	-40	–	mV/V

*To obtain the voltage gain characteristic desired, use the following pin connections

Voltage Gain	Pin Connection
10	Pins 2 and 4 open, Pin 5 to ac ground
18	Pins 2 and 5 open, Pin 4 to ac ground
36	Pin 2 connected to Pin 5, Pin 4 to ac ground

6

Characteristic Definitions
(Linear Operation)

FIGURE 1

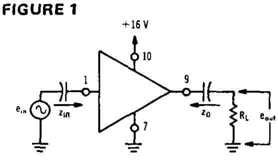


FIGURE 3

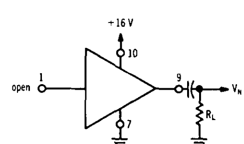


FIGURE 4

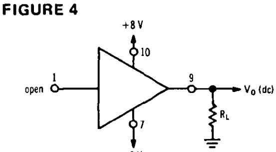
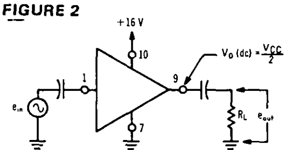


FIGURE 2



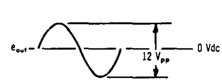
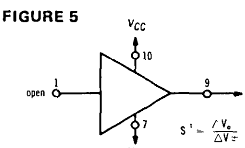


FIGURE 5



MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Total Power Supply Voltage		$\|V_{CC}\| + \|V_{EE}\|$	18	Vdc
Peak Load Current		I_{out}	0.5	Ampere
Audio Output Power		P_{out}	1.8	Watts
Power Dissipation (package limitation)				
T_A = +25°C		P_D	600	mW
Derate above 25°C		$1/\theta_{JA}$	4.8	mW/°C
T_C = +25°C		P_D	1.8	Watts
Derate above 25°C		$1/\theta_{JC}$	14.4	mW/°C
Operating Temperature Range	MC1454	T_A	0 to +70	°C
	MC1554		-55 to +125	
Storage Temperature Range		T_{stg}	-55 to +150	°C

TYPICAL CONNECTIONS

FIGURE 6 – SPLIT SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx$ 25 Hz

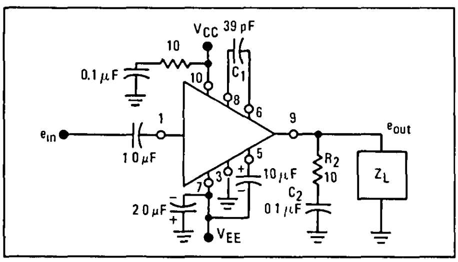
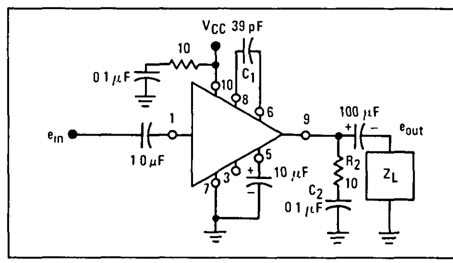


FIGURE 7 – SINGLE SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx$ 100 Hz



RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to.

1 An R-C stabilizing network (0 1 µF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 6 and 7, using short leads, to eliminate local VHF instability caused by lead inductance to the load

2 Excessive lead inductance from the V_{CC} supply to pin 10 can cause high frequency instability To prevent this, the V_{CC} by-pass capacitor should be connected with short leads from the V_{CC} pin to ground If this capacitor is remotely located a series R C network (0 1 µF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 6 and 7

3 Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads This can be assured by either (a) use of short leads which are well isolated, (b) narrow banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low pass filter in combination with the source impedance, or (c) use of a shielded input cable In applications which require upper band edge control the input low pass filter is recommended

TYPICAL CHARACTERISTICS

FIGURE 8 – TOTAL HARMONIC DISTORTION versus LOAD RESISTANCE

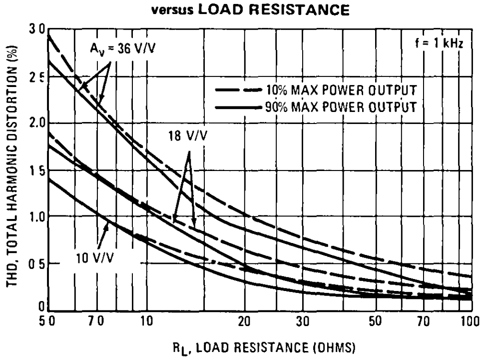
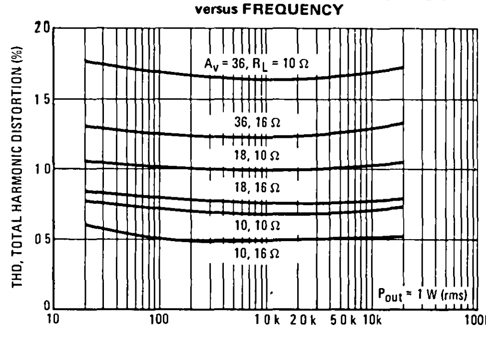


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – VOLTAGE GAIN versus TEMPERATURE

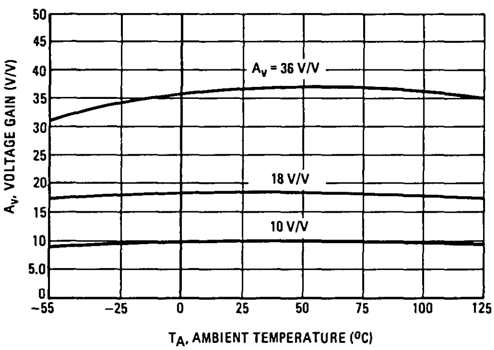


FIGURE 11 – OUTPUT VOLTAGE CHANGE

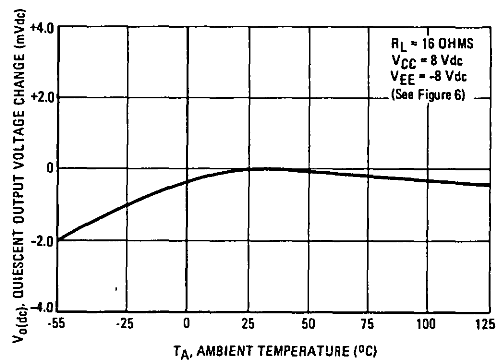


FIGURE 12 – VOLTAGE GAIN versus FREQUENCY ($R_L = \infty$)

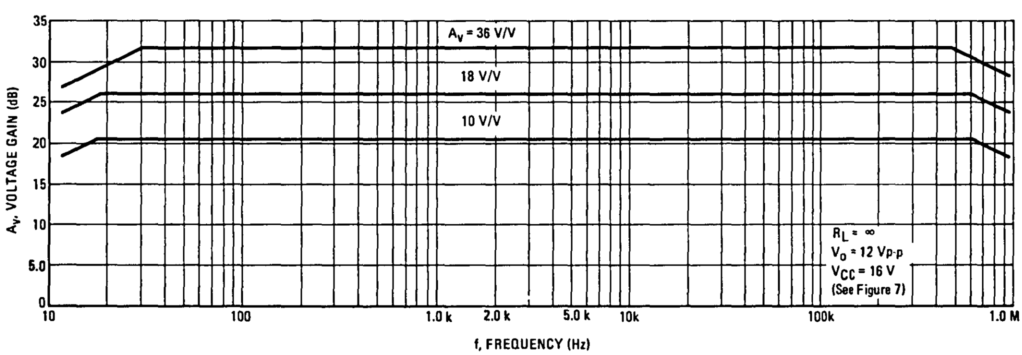
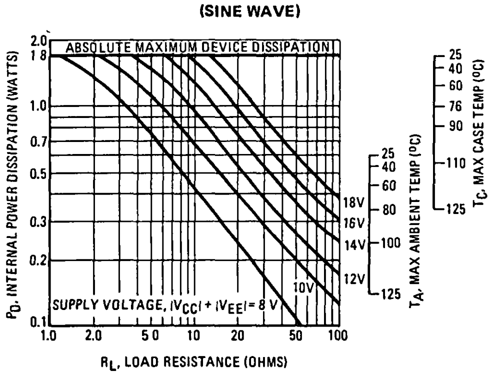


FIGURE 13 – MAXIMUM DEVICE DISSIPATION (SINE WAVE)



6

MC1455
MC1555

Specifications and Applications Information

TIMING CIRCUIT

The MC1555/MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE555/SE555 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output

FIGURE 1 – 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

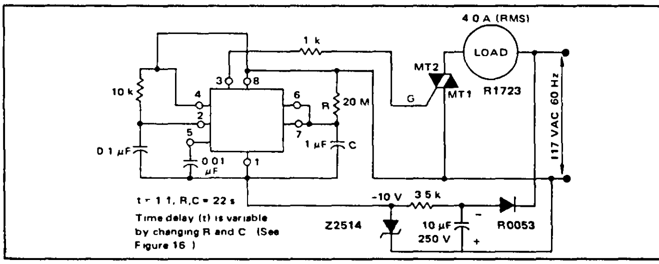
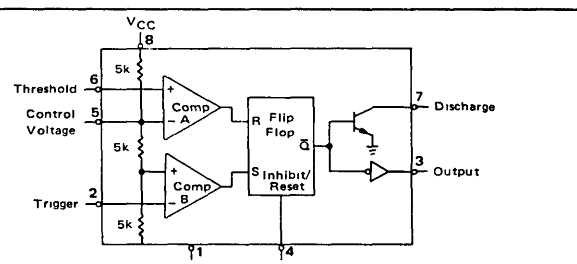


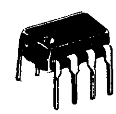
FIGURE 2 – BLOCK DIAGRAM

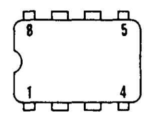


TIMING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

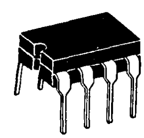
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(Top View)
(MC1455P1 only)

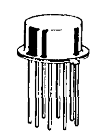




1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

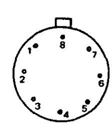
U SUFFIX
CERAMIC PACKAGE
CASE 693





G SUFFIX
METAL PACKAGE
CASE 601

(Top View)



1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1455G	–	0°C to +70°C	Metal Can
MC1455P1	NE555V	0°C to +70°C	Plastic DIP
MC1455U	–	0°C to +70°C	Ceramic DIP
MC1555G	–	-55°C to +125°C	Metal Can
MC1555U	–	-55°C to +125°C	Ceramic DIP

TYPICAL APPLICATIONS

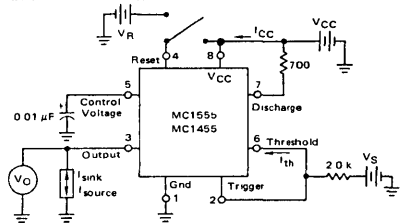
- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

6

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range (Ambient)	T_A		°C
MC1555		-55 to +125	
MC1455		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters
(to set output and measure parameters)
a) When $V_S \geq 2/3\ V_{CC}$, V_O is low
b) When $V_S \leq 1/3\ V_{CC}$, V_O is high
c) When V_O is low, pin 7 sinks current. To test for Reset, set V_O, high, apply Reset voltage, and test for current flowing into pin 7. When Reset is not in use, it should be tied to V_{CC}

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	MC1555			MC1455			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	–	18	4.5	–	16	V
Supply Current	I_{CC}							mA
V_{CC} = 5.0 V, $R_L = \infty$		–	3.0	5.0	–	3.0	6.0	
V_{CC} = 15 V, $R_L = \infty$		–	10	12	–	10	15	
Low State, (Note 1)								
Timing Error (Note 2)								
R = 1.0 kΩ to 100 kΩ								
Initial Accuracy C = 0.1 µF		–	0.5	2.0	–	1.0	–	%
Drift with Temperature		–	30	100	–	50	–	PPM/°C
Drift with Supply Voltage		–	0.05	0.20	–	0.10	–	%/Volt
Threshold Voltage	V_{th}	–	2/3	–	–	2/3	–	xV_{CC}
Trigger Voltage	V_T							V
V_{CC} = 15 V		4.8	5.0	5.2	–	5.0	–	
V_{CC} = 5.0 V		1.45	1.67	1.9	–	1.67	–	
Trigger Current	I_T	–	0.5	–	–	0.5	–	µA
Reset Voltage	V_R	0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.1	0.25	–	0.1	0.25	µA
Discharge Leakage Current (Pin 7)	I_{dis}	–	–	100	–	–	100	nA
Control Voltage Level	V_{CL}							V
V_{CC} = 15 V		9.6	10	10.4	9.0	10	11	
V_{CC} = 5.0 V		2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Low	V_{OL}							
(V_{CC} = 15 V)								V
I_{sink} = 10 mA		–	0.1	0.15	–	0.1	0.25	
I_{sink} = 50 mA		–	0.4	0.5	–	0.4	0.75	
I_{sink} = 100 mA		–	2.0	2.2	–	2.0	2.5	
I_{sink} = 200 mA		–	2.5	–	–	2.5	–	
(V_{CC} = 5.0 V)								
I_{sink} = 8.0 mA		–	0.1	0.25	–	–	–	
I_{sink} = 5.0 mA		–	–	–	–	0.25	0.35	
Output Voltage High	V_{OH}							V
(I_{source} = 200 mA)								
V_{CC} = 15 V		–	12.5	–	–	12.5	–	
(I_{source} = 100 mA)								
V_{CC} = 15 V		13	13.3	–	12.75	13.3	–	
V_{CC} = 5.0 V		3.0	3.3	–	2.75	3.3	–	
Rise Time of Output	t_{OLH}	–	100	–	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	–	100	–	ns

NOTES:
1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
Monostable mode
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

6

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 4 — TRIGGER PULSE WIDTH

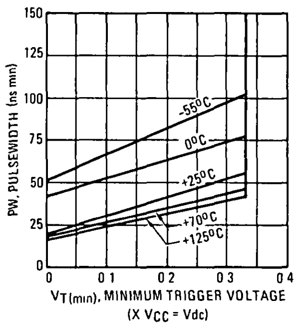


FIGURE 5 — SUPPLY CURRENT

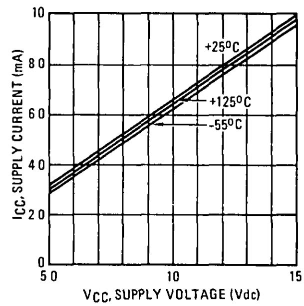


FIGURE 6 — HIGH OUTPUT VOLTAGE

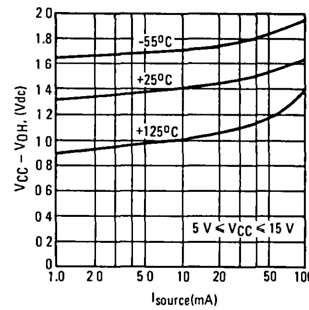


FIGURE 7 — LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

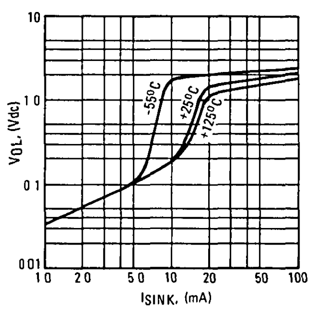


FIGURE 8 — LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

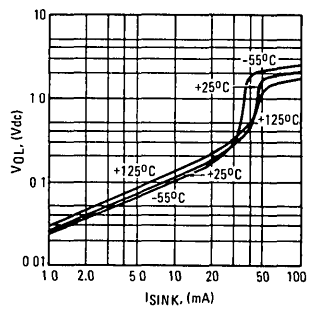


FIGURE 9 — LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

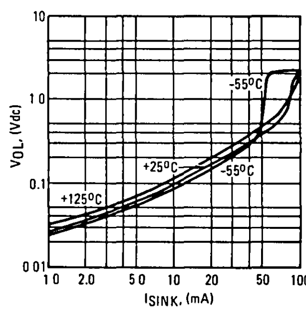


FIGURE 10 — DELAY TIME versus SUPPLY VOLTAGE

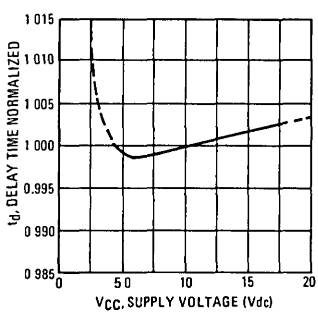


FIGURE 11 — DELAY TIME versus TEMPERATURE

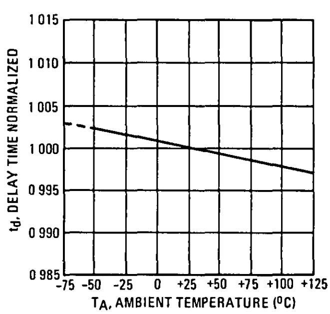


FIGURE 12 — PROPAGATION DELAY versus TRIGGER VOLTAGE

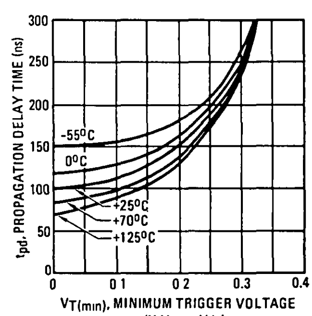


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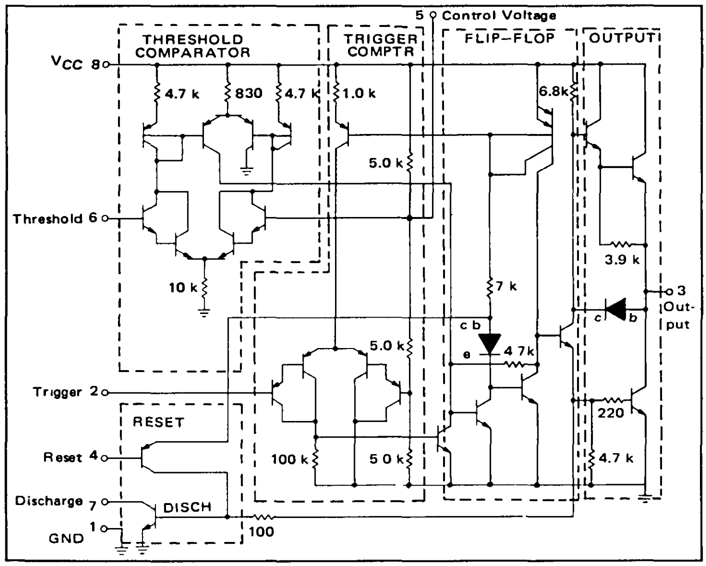
FIGURE 13 – REPRESENTATIVE CIRCUIT SCHEMATIC



GENERAL OPERATION

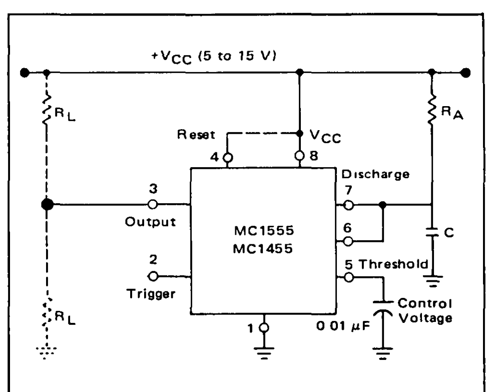
The MC1555 is a monolithic timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

FIGURE 14 – MONOSTABLE CIRCUIT



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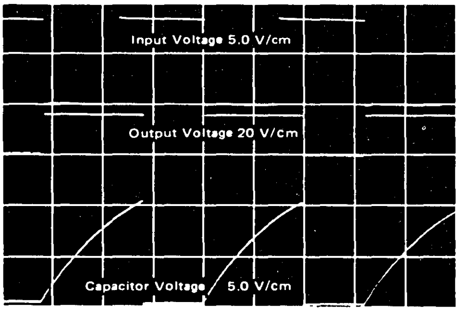
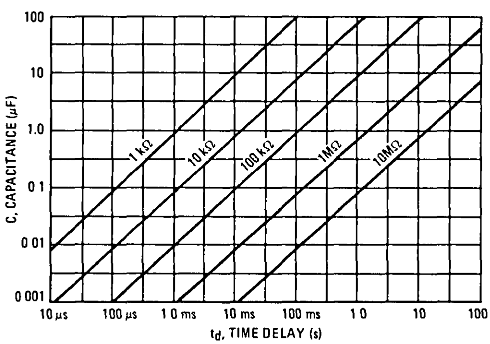
GENERAL OPERATION (continued)

FIGURE 15 – MONOSTABLE WAVEFORMS



t = 50 µs/cm
(R_A = 10 kΩ, C = 0.01 µF, R_L = 1.0 kΩ, V_{CC} = 15 V)

FIGURE 16 – TIME DELAY



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Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695 (R_A+R_B) C$

The discharge time (output low) by: $t_2 = 0.695 (R_B) C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695 (R_A+2R_B) C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B) C}$

and may be easily found as shown in Figure 19.

The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\ (Vdc)}{I_7\ (A)} \geq \frac{V_{CC}\ (Vdc)}{0.2}$$

FIGURE 17 – ASTABLE CIRCUIT

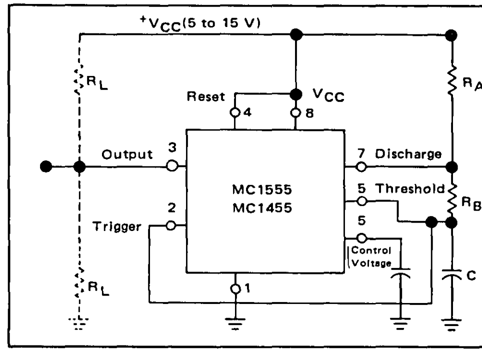
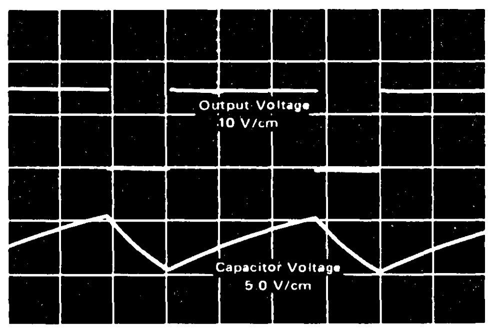


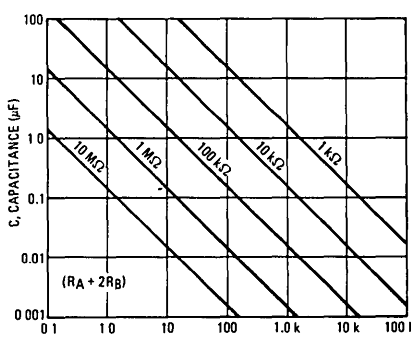
FIGURE 18 – ASTABLE WAVEFORMS



t = 20 µs/cm

(R_A = 5.1 kΩ, C = 0.01 µF, R_L = 1.0 kΩ;
R_B = 3.9 kΩ, V_{CC} = 15 V)

FIGURE 19 – FREE-RUNNING FREQUENCY



APPLICATIONS INFORMATION

Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 to 2/3 V_{CC}. The linear ramp time is given by $t = \frac{2}{3} \frac{V_{CC}}{I}$

where $I = \frac{V_{CC} - V_B - V_{BE}}{R_E}$. If V_B is much larger than V_{BE}, then t can be made independent of V_{CC}.

Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

FIGURE 20 – LINEAR VOLTAGE SWEEP CIRCUIT

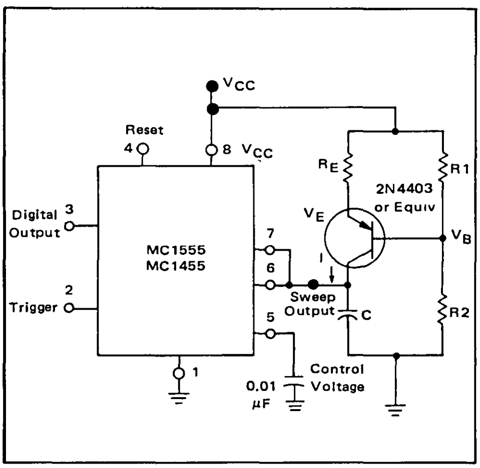


FIGURE 22

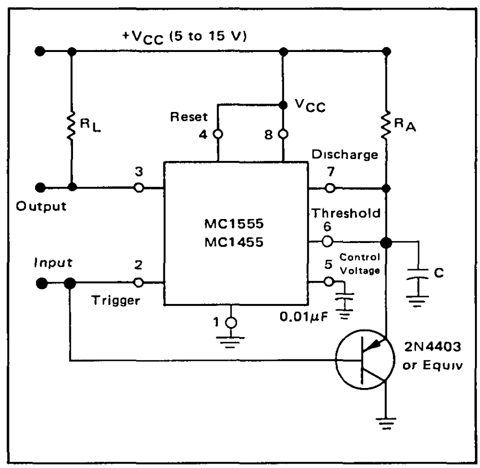
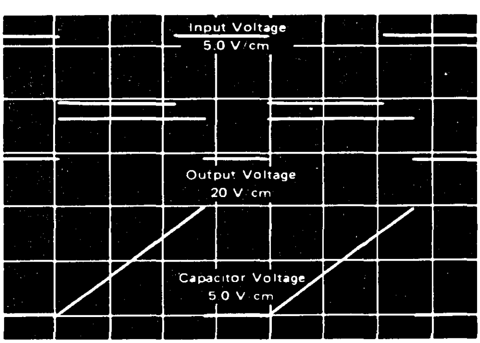
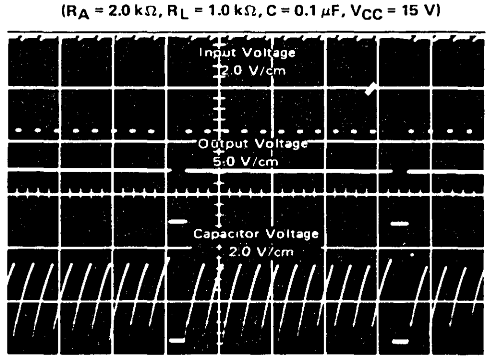


FIGURE 21 – LINEAR VOLTAGE RAMP WAVEFORMS
(R_E = 10 kΩ, R2 = 100 kΩ, R1 = 39 kΩ, C = 0.01 µF, V_{CC} = 15 V)



t = 100 µs/cm

FIGURE 23 – MISSING PULSE DETECTOR WAVEFORMS
(R_A = 2.0 kΩ, R_L = 1.0 kΩ, C = 0.1 µF, V_{CC} = 15 V)



t = 500 µs/cm

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APPLICATIONS INFORMATION (continued)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 24

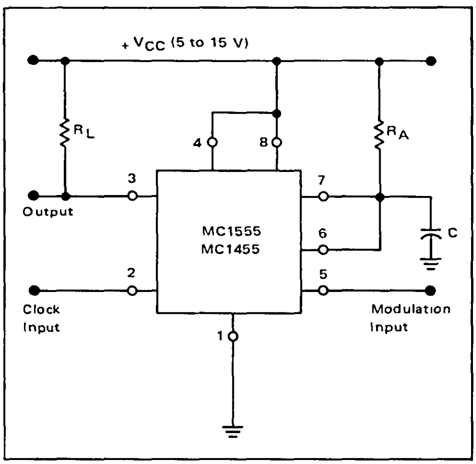
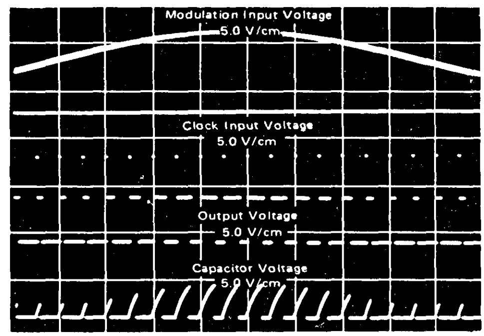


FIGURE 25 – PULSE WIDTH MODULATION WAVEFORMS
(R_A = 10 kΩ, C = 0.02 μF, V_{CC} = 15 V)

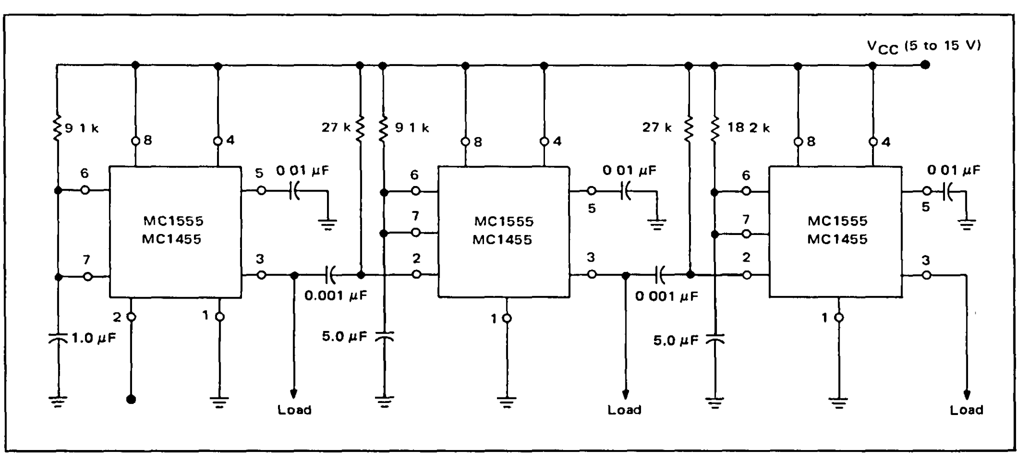


t = 0.5 ms/cm

Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 26



MC1590

RF/IF/AUDIO AMPLIFIER

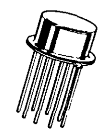
. . . an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, -55 to +125°C. See Motorola Application Note AN-513 for design details.

- High Power Gain – 50 dB typ at 10 MHz
  45 dB typ at 60 MHz
  35 dB typ at 100 MHz
- Wide-Range AGC – 60 dB min, dc to 60 MHz
- Low Reverse Transfer Admittance – <10 μmhos typ at 60 MHz
- 6.0 to 15-Volt Operation, Single-Polarity Power Supply

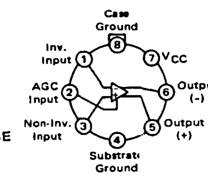
WIDEBAND AMPLIFIER WITH AGC

SILICON MONOLITHIC INTEGRATED CIRCUIT

PIN CONNECTIONS



G SUFFIX
METAL PACKAGE
CASE 601
TO-99



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol*	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Output Supply	V_O	+18	Vdc
AGC Supply	$V_{2(AGC)}$	V_{CC}	Vdc
Differential Input Voltage	V_I	5.0	Vdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	+175	°C

ADMITTANCE PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C)

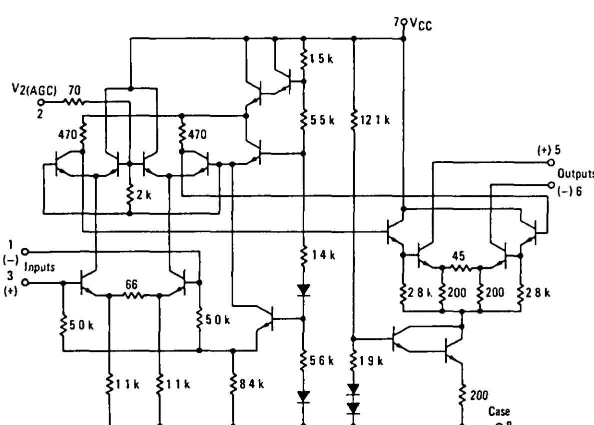
Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Single-Ended Input Admittance	g_{11} b_{11}	0.4 1.2	0.6 -3.0	mmhos
Single-Ended Output Admittance	g_{22} b_{22}	0.05 0.50	0.1 1.0	mmho
Forward Transfer Admittance (Pin 1 to Pin 5)	$\lvert Y_{21} \rvert$ θ_{21} (Polar)	175 -30	150 -105	mmhos degrees
Reverse Transfer Admittance*	g_{12} b_{12}	-0 -5.0	-0 -10	μmhos

*The value of Reverse Transfer Admittance includes the feedback admittance of the test circuit used in the measurement. The total feedback capacitance (including test circuit) is 0.025 pF and is a more practical value for design calculations than the internal feedback of the device alone. (See Figure 10.)

SCATTERING PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Input Reflection Coefficient	$\lvert S_{11} \rvert$ θ_{11}	0.95 -7.3	0.93 -16	– degrees
Output Reflection Coefficient	$\lvert S_{22} \rvert$ θ_{22}	0.99 -3.0	0.98 -5.5	– degrees
Forward Transmission Coefficient	$\lvert S_{21} \rvert$ θ_{21}	16.8 128	14.7 64.3	– degrees
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	– degrees

REPRESENTATIVE CIRCUIT SCHEMATIC



Pins 4 and 8 should both be connected to circuit ground

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ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = −55°C to 125°C unless otherwise noted)

Characteristic	Fig.	Symbol	MC1590 Min	MC1590 Typ	MC1590 Max	Unit
AGC Range ($V_{2(AGC)}$ = 5.0 V to 7.0 V) ($V_{2(AGC)}$ = 5.0 V to 7.0 V, T_A = 25°C)	 24	M_{AGC}	 58 60	 – 68	 – –	dB
Single-Ended Power Gain (T_A = 25°C)	 24	G_p	37 40	– 45	–	dB
Noise Figure (R_s optimized for best NF) (T_A = 25°C)	 24	NF	–	6.0	7.0	dB
Output Voltage Swing Differential Output (0 dB AGC) (0 dB AGC, T_A = 25°C) (-30 dB AGC) (-30 dB AGC, T_A = 25°C)	 25	V_{ODR}	 10 13 4.0 5.0	 – 14 – 6.0	 – – – –	Vpp
Single-Ended Output (Pin 5, 6) (0 dB AGC) (0 dB AGC, T_A = 25°C) (-30 dB AGC) (-30 dB AGC, T_A = 25°C)	25	V_{OCR}	 5.0 6.5 2.0 2.5	 – 7.0 – 3.0	 – – – –	Vpp
Output Stage Current (Sum of Pins 5 and 6) (T_A = 25°C)	32	I_O	 3.5 4.0	 – 5.6	 8.0 7.5	mA
Output Current Matching (Magnitude of Difference of Output Currents) (I_5 - I_6) (T_A = 25°C)	32	ΔI_O	–	0.7	–	mA
Power Supply Current (V_O = 0 V) (V_O = 0 V, T_A = 25°C)	32	I_{CC}	 – –	 – 14	 20 17	mA
Power Consumption (12 x I_{CC}) (V_I = 0 V) (V_I = 0 V, T_A = 25°C)	–	P_C	 – –	 – 168	 240 204	mW

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FIGURE 1 – UNNEUTRALIZED POWER GAIN versus FREQUENCY (Tuned Amplifier, See Figure 24)

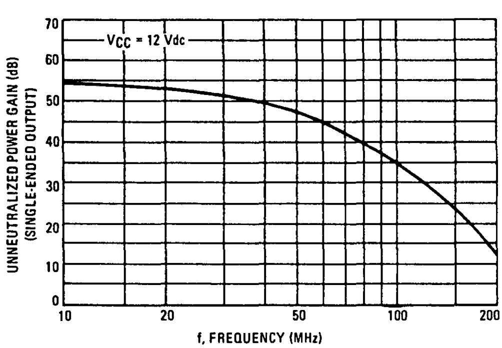
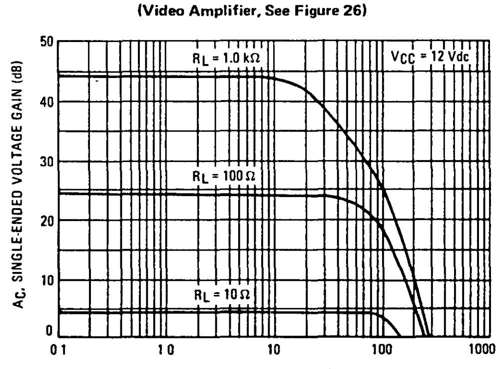


FIGURE 2 – VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 26)



TYPICAL CHARACTERISTICS

($V_{2\,(AGC)} = 0$, $V_{CC} = 12$ Vdc, $T_A = +25°C$ unless otherwise noted)

FIGURE 3 — DYNAMIC RANGE: OUTPUT VOLTAGE versus INPUT VOLTAGE (Video Amplifier, See Figure 26)

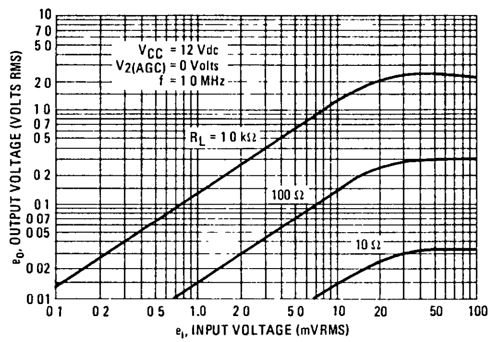


FIGURE 4 — VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 26)

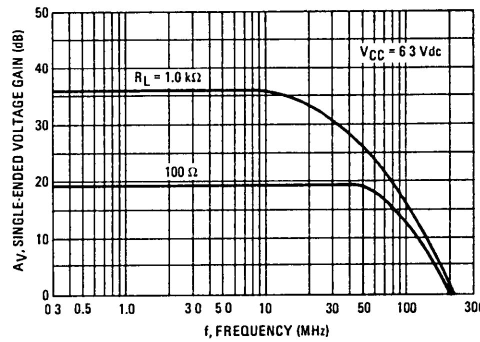


FIGURE 5 — VOLTAGE GAIN AND SUPPLY CURRENT versus SUPPLY VOLTAGE (Video Amplifier, See Figure 26)

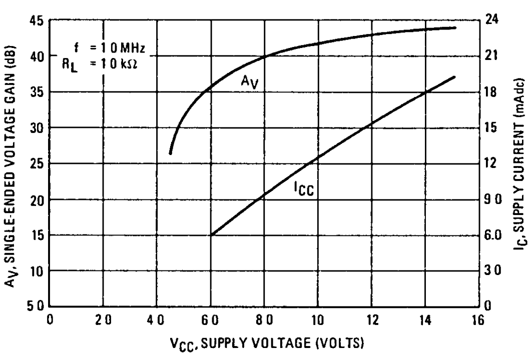


FIGURE 6 — TYPICAL GAIN REDUCTION versus AGC VOLTAGE

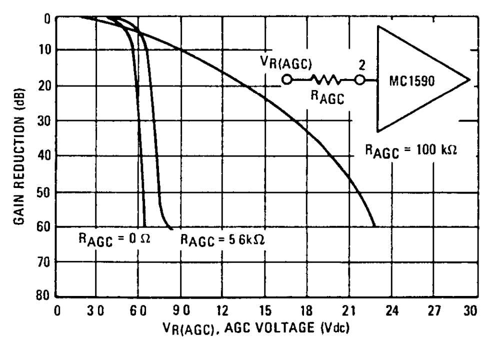


FIGURE 7 — TYPICAL GAIN REDUCTION versus AGC CURRENT

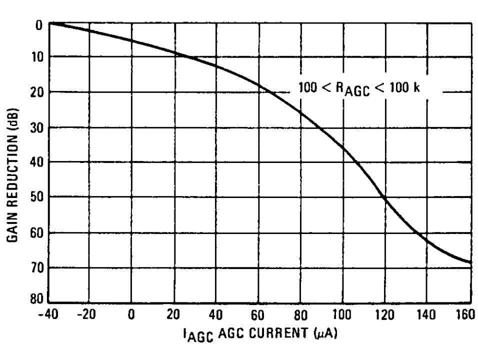
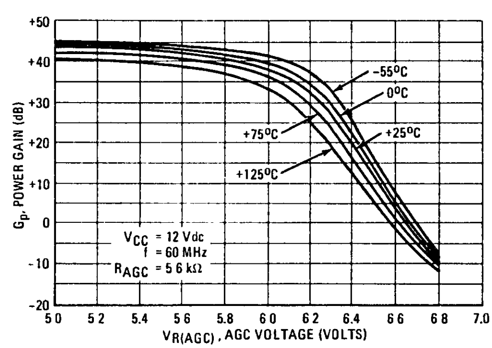


FIGURE 8 — FIXED TUNED POWER GAIN REDUCTION versus TEMPERATURE (See Test Circuit, Figure 24)



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TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – POWER GAIN versus SUPPLY VOLTAGE (See Test Circuit, Figure 24)

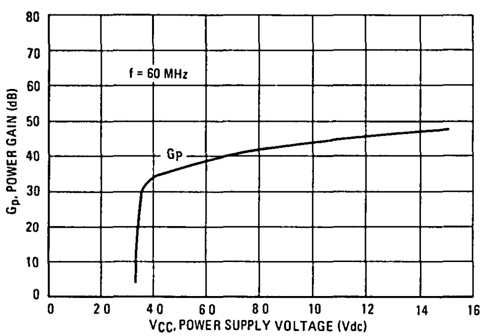


FIGURE 10 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY (See Parameter Table, Page 1)

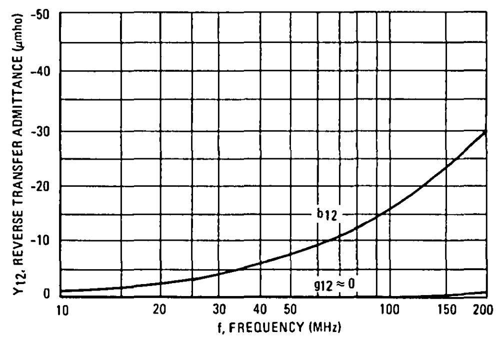


FIGURE 11 – NOISE FIGURE versus FREQUENCY

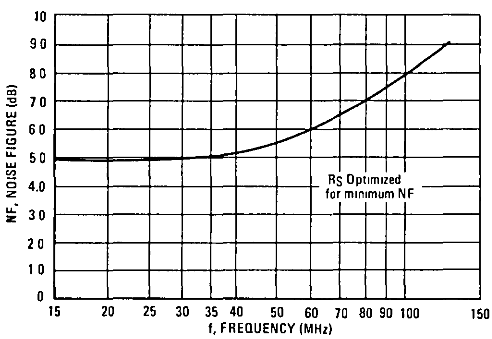


FIGURE 12 – NOISE FIGURE versus SOURCE RESISTANCE

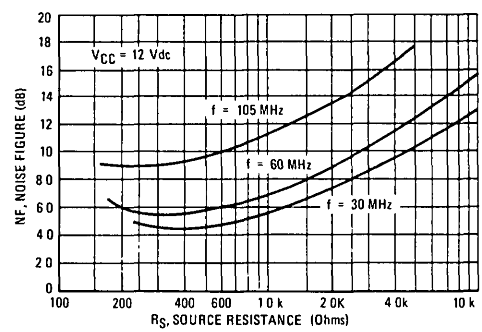
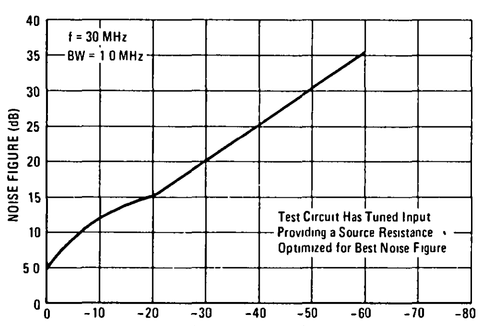


FIGURE 13 – NOISE FIGURE versus AGC GAIN REDUCTION



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TYPICAL CHARACTERISTICS (continued)

FIGURE 14 — SINGLE-ENDED OUTPUT ADMITTANCE

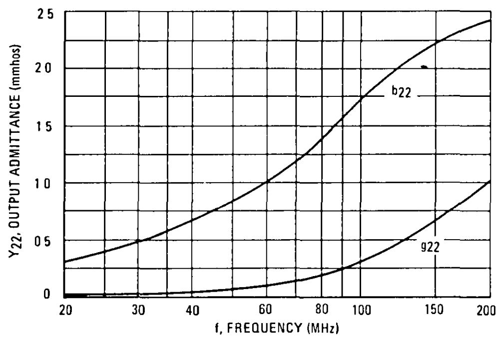


FIGURE 15 — SINGLE-ENDED INPUT ADMITTANCE

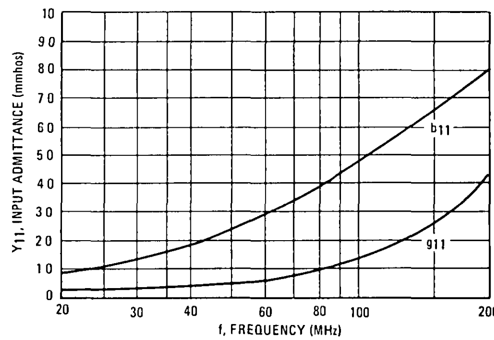


FIGURE 16 — HARMONIC DISTORTION versus AGC GAIN REDUCTION FOR AM CARRIER (For Test Circuit, See Figure 17)

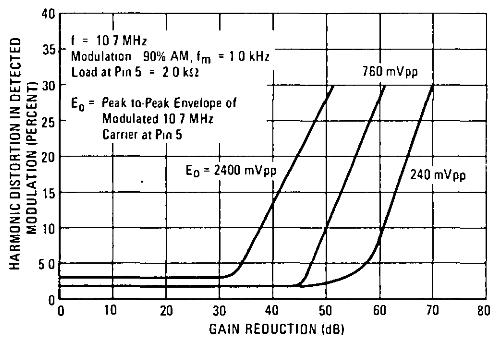


FIGURE 17 — 10.7-MHz AMPLIFIER
Gain ≃ 55 dB, BW ≃ 100 kHz

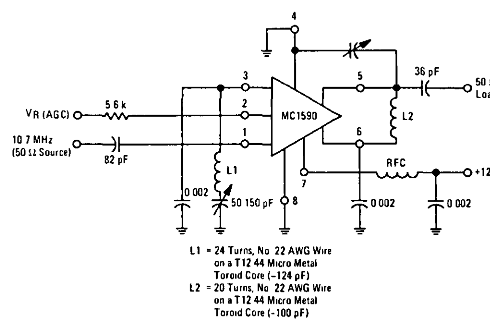


FIGURE 18 — Y_{21}, FORWARD TRANSFER ADMITTANCE RECTANGULAR FORM

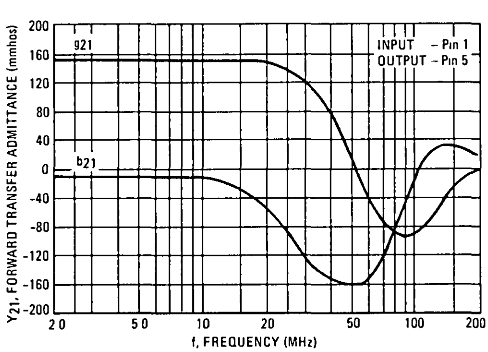
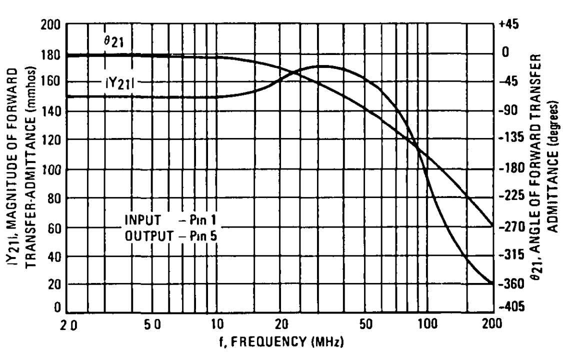


FIGURE 19 — Y_{21}, FORWARD TRANSFER ADMITTANCE POLAR FORM



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TYPICAL CHARACTERISTICS (continued)

FIGURE 20 – S_{11} AND S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

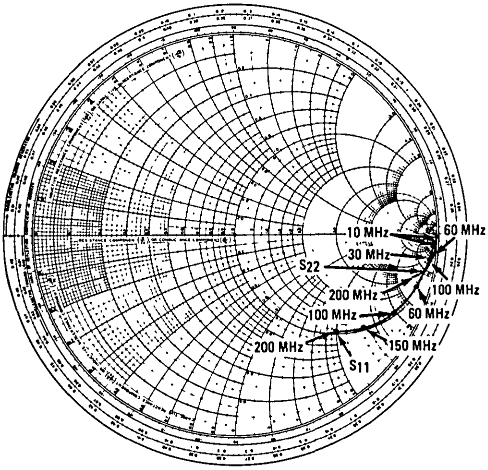


FIGURE 21 – S_{11} AND S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

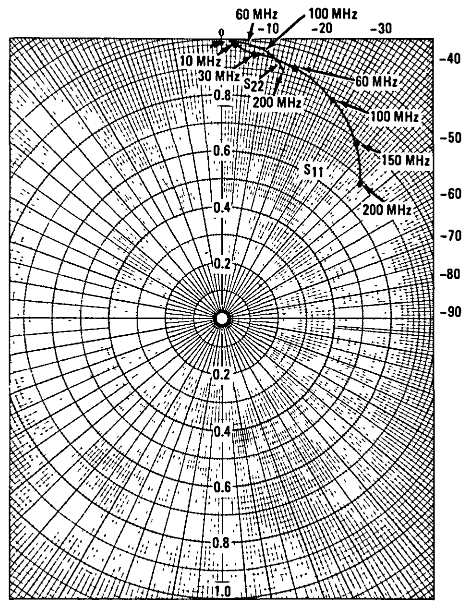


FIGURE 22 – S_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

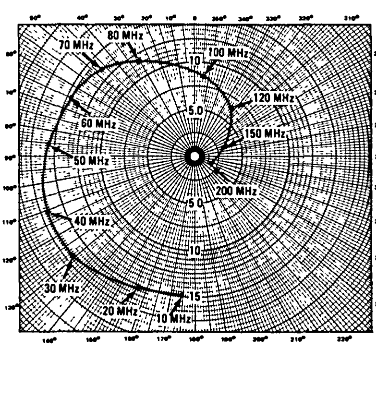
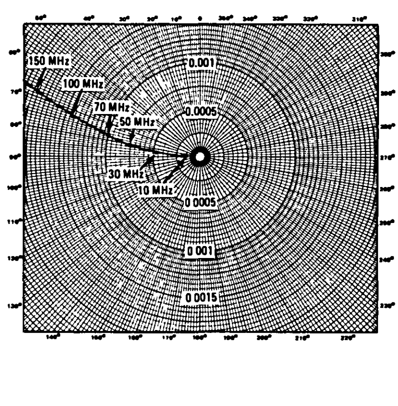
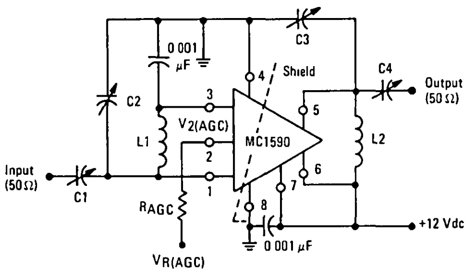


FIGURE 23 – S_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



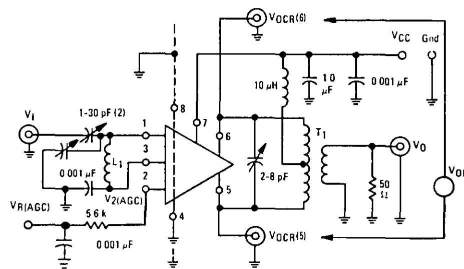
TYPICAL APPLICATIONS

FIGURE 24 – 60-MHz POWER GAIN TEST CIRCUIT



L1 = 7 Turns, #20 AWG Wire, 5/16" Dia, 5/8" Long
L2 = 6 Turns, #14 AWG Wire, 9/16" Dia, 3/4" Long
C1,C2,C3 = (1-30) pF
C4 = (1-10) pF

FIGURE 25 – DIFFERENTIAL OUTPUT VOLTAGE SWING, (V5, V6) (60 MHz)



L1 7 Turns, – 22 AWG Wire on 5/16" Dia Form, 5/8" Long
T1 Close Wound Over 1/4" Form
Primary Winding - 16 Turns = 26 AWG, Center Tapped
Secondary Winding = 2 Turns = 26 AWG

FIGURE 25a – PROCEDURE FOR SET–UP USING FIGURES 24 OR 25

Test	e_{in}	V2(AGC)	RAGC(kΩ)
MAGC	2 23 mV (-40dBm)	5-7 V	0
Gp	1.0 mV (-47dBm)	≤5 0 V	5 6
NF	1 0 mV (-47dBm)	≤5 0 V	5 6
VOCR(5) VOCR(6) VODR			5 6
(0dB)	Adjust e_{in} for Square Wave Output V2(AGC) = VR(AGC) = 0 V	>0 dB Limit	
(-30 dB)	Adjust e_{in} to 1 0 mV Adjust VR(AGC) so that output is -30 dB then reset e_{in} to Square Wave Output	>-30 dB Limit	

FIGURE 26 – VIDEO AMPLIFIER

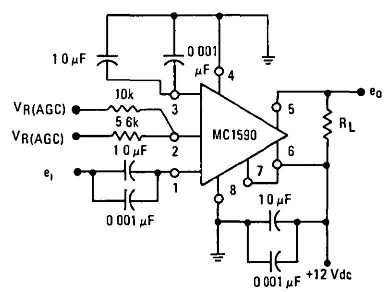
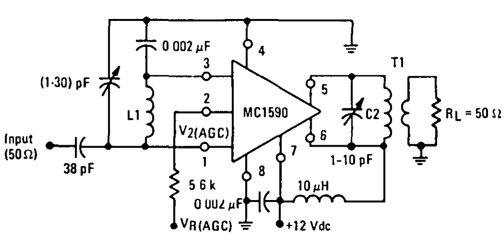
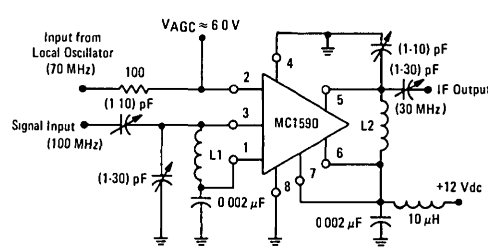


FIGURE 27 – 30-MHz AMPLIFIER (Power Gain = 50 dB, BW ≈ 1.0 MHz)



L1 = 12 Turns #22 AWG Wire on a Toroid Core, (T37-6 Micro Metal or Equiv)
T1 Primary = 17 Turns #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)
Secondary = 2 Turns #20 AWG Wire

FIGURE 28 – 100 MHz MIXER



L1 = 5 Turns, #16 AWG Wire, 1/4" ID, 5/8" Long
L2 = 16 Turns, #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)

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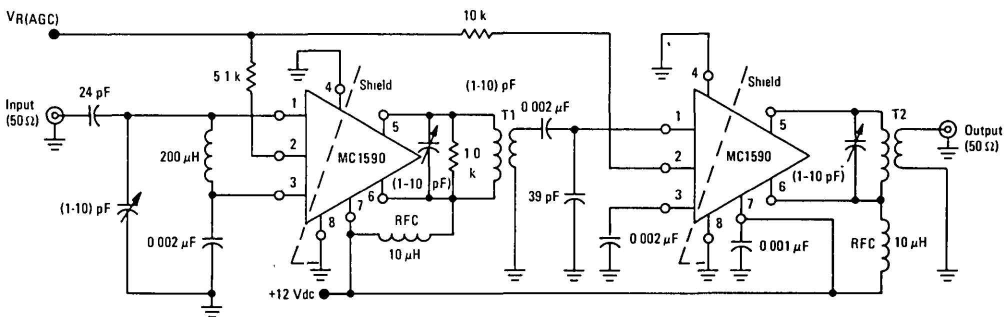
TYPICAL APPLICATIONS (continued)

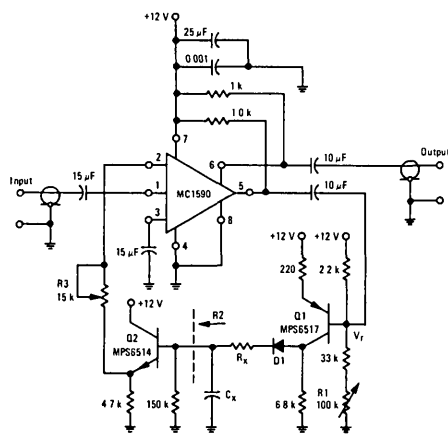
FIGURE 29 – TWO-STAGE 60 MHz IF AMPLIFIER (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)



T1: Primary Winding = 15 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 4 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 2 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

FIGURE 30 – SPEECH COMPRESSOR



DESCRIPTION OF SPEECH COMPRESSOR

The amplifier drives the base of a PNP MPS6517 operating common-emitter with a voltage gain of approximately 20. The control R1 varies the quiescent Q point of this transistor so that varying amounts of signal exceed the level V_r. Diode D1 rectifies the positive peaks of Q1's output only when these peaks are greater than $V_r \simeq 7.0$ Volts. The resulting output is filtered by C_x, R_x.

R_x controls the charging time constant or attack time. C_x is involved in both charge and discharge. R2 (the 150 kΩ and input resistance of the emitter-follower Q2) controls the decay time. Making the decay long and attack short is accomplished by making R_x small and R2 large. (A Darlington emitter-follower may be needed if extremely slow decay times are required.)

The emitter-follower Q2 drives the AGC Pin 2 of the MC1590 and reduces the gain. R3 controls the slope of signal compression. The following graph (Figure 31) details performance with R3 set to 15 kΩ.

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FIGURE 31 – OUTPUT VOLTAGE versus INPUT VOLTAGE

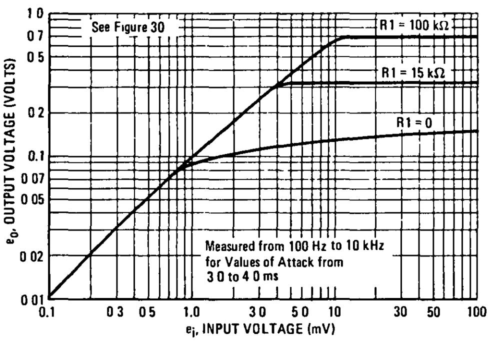

FIGURE 32 – OUTPUT CURRENT, CURRENT MATCH AND I_{CC} FIXTURE

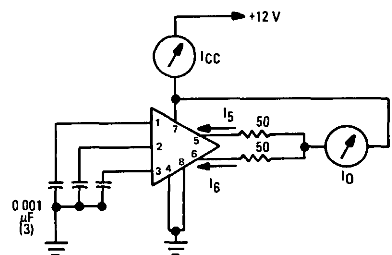

TABLE I – DISTORTION versus FREQUENCY

FREQUENCY	DISTORTION		DISTORTION	
	10 mV e_i	100 mV e_i	10 mV e_i	100 mV e_i
100 Hz	3.5%	12%	15%	27%
300 Hz	2%	10%	6%	20%
1.0 kHz	1.5%	8%	3%	9%
10 kHz	1.5%	8%	1%	3%
100 kHz	1.5%	8%	1%	3%
	Notes 1 and 2		Notes 3 and 4	

Note: (1) Decay = 300 ms
Attack = 20 ms
(2) C_X = 7.5 µF
R_X = 0 (Short)
(3) Decay = 20 ms
Attack = 3 ms
(4) C_X = 0.68 µF
R_X = 1.5 kΩ

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1494L	0°C to +70°C	Ceramic DIP
MC1594L	−55°C to +125°C	Ceramic DIP

MC1494L
MC1594L

Specifications and Applications Information

MONOLITHIC FOUR-QUADRANT MULTIPLIER

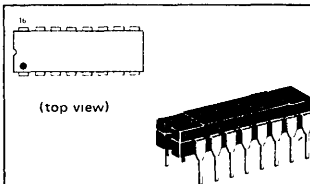
. . . designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

- Operates With ±15 V Supplies
- Excellent Linearity – Maximum Error (X or Y): ± 0.5% (MC1594) ± 1.0% (MC1494)
- Wide Input Voltage Range – ±10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single-Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small-Signal) – 1.0 MHz
- Power Supply Sensitivity – 30 mV/V typical

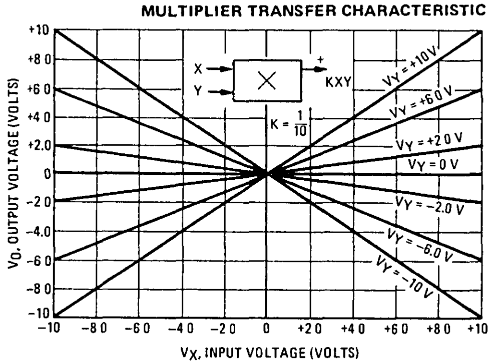
LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

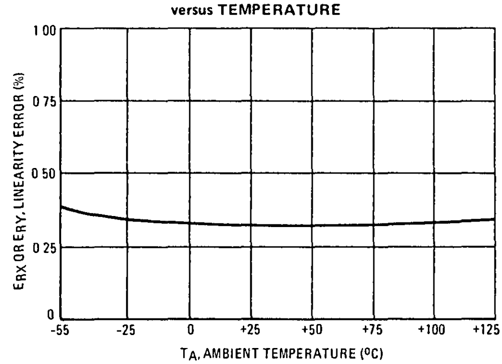


CERAMIC PACKAGE
CASE 620

FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC



TYPICAL LINEARITY ERROR versus TEMPERATURE



CONTENTS

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	V_9-V_6 $V_{10}-V_{13}$	$\pm\|6+I_1 R_Y\| < 30$ $\pm\|6+I_1 R_X\| < 30$	Vdc
Common-Mode Input Voltage $V_{CMY} = V_9 = V_6$ $V_{CMX} = V_{10} = V_{13}$	 V_{CMY} V_{CMX}	 ±11 5 ±11 5	Vdc
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	 P_D $1/\theta_{JA}$	 750 5 0	 mW mW/°C
Operating Temperature Range MC1594 MC1494	T_A	 -55 to +125 0 to + 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 V, V^- = -15 V, T_A = +25°C, R1 = 16 kΩ, R_X = 30 kΩ, R_Y 62 kΩ, R_L = 47 kΩ unless otherwise noted)

Characteristic	Fig	Symbol	MC1594 Min	MC1594 Typ	MC1594 Max	MC1494 Min	MC1494 Typ	MC1494 Max	Unit
Linearity	1	E_{RX} or E_{RY}							%
Output error in Percent of full scale									
$-10\ V < V_x < +10\ V$ ($V_y = \pm 10\ V$)									
$-10\ V < V_y < +10\ V$ ($V_x = \pm 10\ V$)									
T_A = +25°C			–	± 0 3	± 0 5	–	± 0 5	± 1 0	
$T_A = T_{high}$ ①			–	–	± 0 8	–	–	± 1.3	
$T_A = T_{low}$ ②			–	–	± 0 8	–	–	± 1 3	
Input	2,3,4								
Voltage Range ($V_X = V_Y = V_{in}$)		V_{in}	±10	–	–	±10	–	–	V_{pk}
Resistance (X or Y Input)		R_{in}	–	300	–	–	300	–	MΩ
Offset Voltage (X Input) (Note 1)		$\|V_{iox}\|$	–	0 1	1 6	–	0 2	2 5	V
(Y Input) (Note 1)		$\|V_{ioy}\|$	–	0 4	1 6	–	0 8	2 5	
Bias Current (X or Y Input)		I_b	–	0 5	1 5	–	1 0	2 5	µA
Offset Current (X or Y Input)		$\|I_{io}\|$	–	28	150	–	50	400	nA
Output	3,4								
Voltage Swing Capability		V_o	±10	–	–	±10	–	–	V_{pk}
Impedance		R_o	–	850	–	–	850	–	kΩ
Offset Voltage (Note 1)		$\|V_{oo}\|$	–	0 8	1 6	–	1 2	2 5	V
Offset Current (Note 1)		$\|I_{oo}\|$	–	17	34	–	25	52	µA
Temperature Stability (Drift)									
$T_A = T_{high}$ to T_{low}									
Output Offset (X = 0, Y = 0) Voltage		$\|TCV_{oo}\|$	–	1 3	–	–	1 3	–	mV/°C
Current		$\|TCI_{oo}\|$	–	27	–	–	27	–	nA/°C
X Input Offset (Y = 0)		$\|TCV_{iox}\|$	–	0 3	–	–	0 3	–	mV/°C
Y Input Offset (X = 0)		$\|TCV_{ioy}\|$	–	1 5	–	–	1 5	–	
Scale Factor		$\|TCK\|$	–	0.07	–	–	0.07	–	%/°C
Total dc Accuracy Drift (X = 10, Y = 10)		$\|TCE\|$	–	0.09	–	–	0.09	–	
Dynamic Response	5								
Small Signal (3 dB) X		$BW_{3dB(X)}$	–	0 8	–	–	0 8	–	MHz
Y		$BW_{3dB(Y)}$	–	1 0	–	–	1 0	–	
Power Bandwidth (47 k)		P_{BW}	–	440	–	–	440	–	kHz
3° Relative Phase Shift		$f\phi$	–	240	–	–	240	–	
1% Absolute Error		$f\theta$	–	30	–	–	30	–	
Common Mode	6								
Input Swing (X or Y)		CMV	±10 5	–	–	±10 5	–	–	V_{pk}
Gain (X or Y)		A_{CM}	–	-65	–	–	-65	–	dB
Power Supply	7								
Current		I_d^+	–	6 0	9 0	–	6 0	12	mAdc
		I_d^-	–	6 5	9 0	–	6 5	12	
Quiescent Power Dissipation		P_d	–	185	260	–	185	350	mW
Sensitivity		S^+	–	13	50	–	13	100	mV/V
		S^-	–	30	100	–	30	200	
Regulated Offset Adjust Voltages	7								
Positive		V_R^+	+3 5	+4 3	+5 0	+3 5	+4 3	+5 0	Vdc
Negative		V_R^-	-3.5	-4 3	-5 0	-3 5	-4 3	-5 0	
Temperature Coefficient (V_R^+ or V_R^-)		TCV_R	–	0 03	–	–	0 03	–	mV/°C
Power Supply Sensitivity (V_R^+ or V_R^-)		S_R^+, S_R^-	–	0 6	–	–	0 6	–	mV/V

Note 1 Offsets can be adjusted to zero with external potentiometers

① T_{high} = +125°C for MC1594
+ 70°C for MC1494

② T_{low} = -55°C for MC1594
0°C for MC1494

6

TEST CIRCUITS

FIGURE 1 – LINEARITY

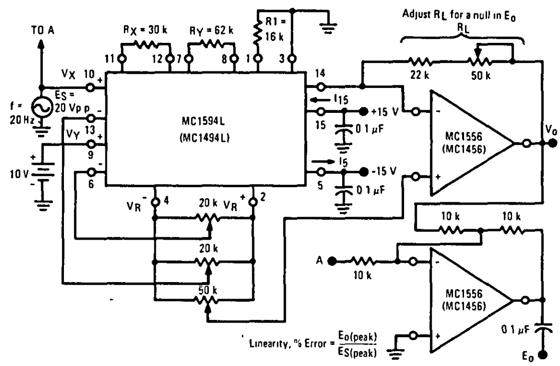


FIGURE 2 – INPUT RESISTANCE

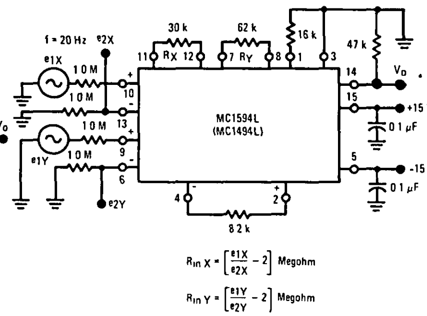


FIGURE 3 – OFFSET VOLTAGES, GAIN

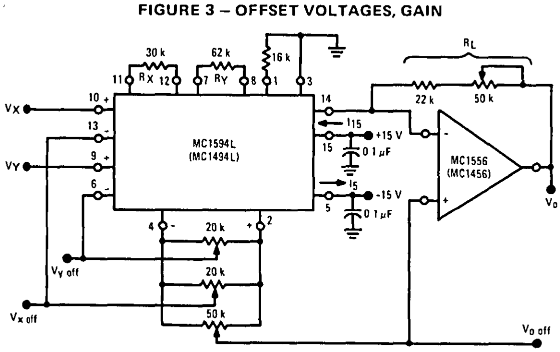


FIGURE 4 – INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE

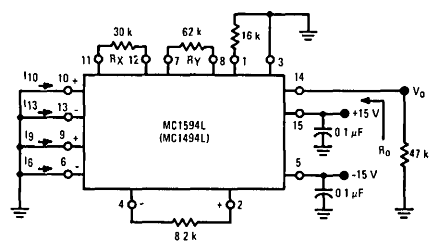


FIGURE 5 – FREQUENCY RESPONSE

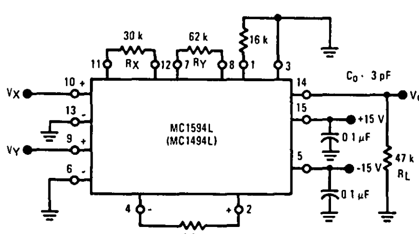


FIGURE 6 – COMMON-MODE

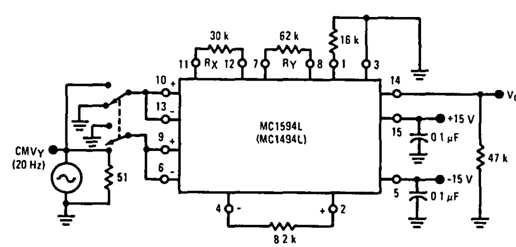


FIGURE 7 – POWER-SUPPLY SENSITIVITY

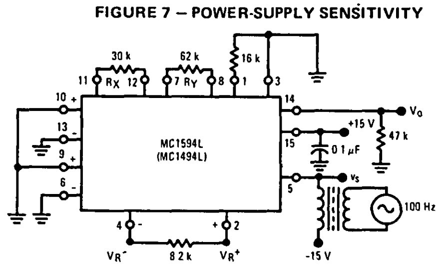
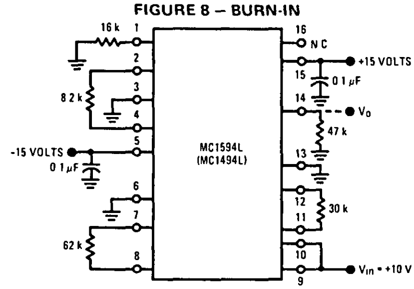


FIGURE 8 – BURN-IN



6

TYPICAL CHARACTERISTICS

(Unless otherwise noted, $V^+ = +15$ V, $V^- = -15$ V, R1 = 16 kΩ, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, $R_L = 47$ kΩ, $T_A = +25°C$)

FIGURE 9 – FREQUENCY RESPONSE OF Y INPUT versus LOAD RESISTANCE

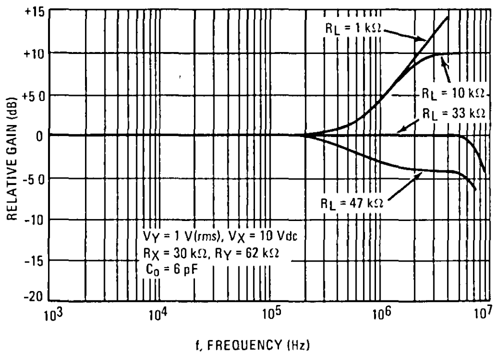


FIGURE 10 – FREQUENCY RESPONSE OF X INPUT versus LOAD RESISTANCE

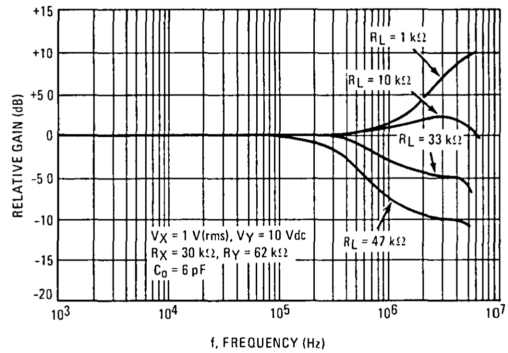


FIGURE 11 – LARGE SIGNAL VOLTAGE versus FREQUENCY

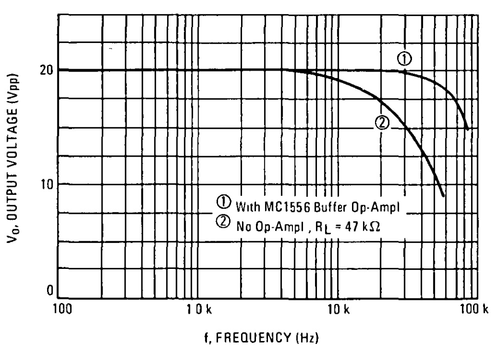


FIGURE 12 – LINEARITY versus R_X OR R_Y WITH K = 1/10

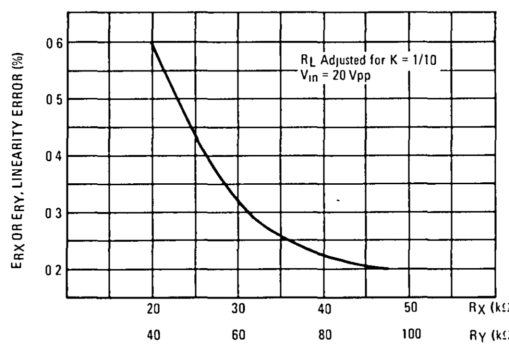


FIGURE 13 – LINEARITY versus R_X OR R_Y WITH K = 1

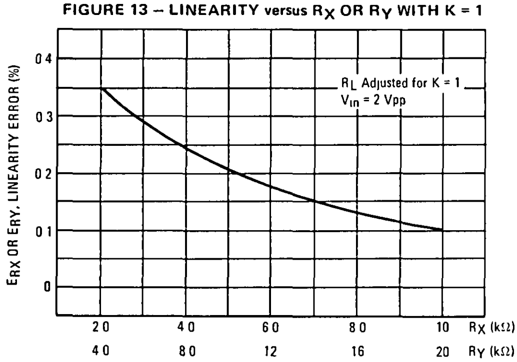
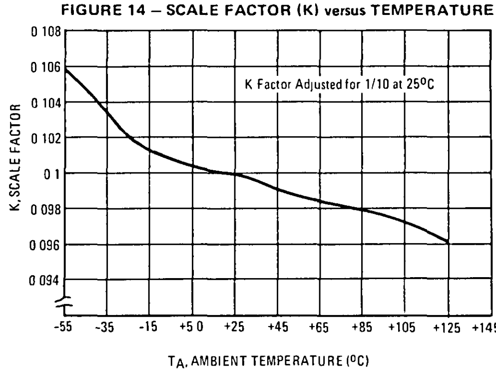


FIGURE 14 – SCALE FACTOR (K) versus TEMPERATURE



6

GENERAL INFORMATION

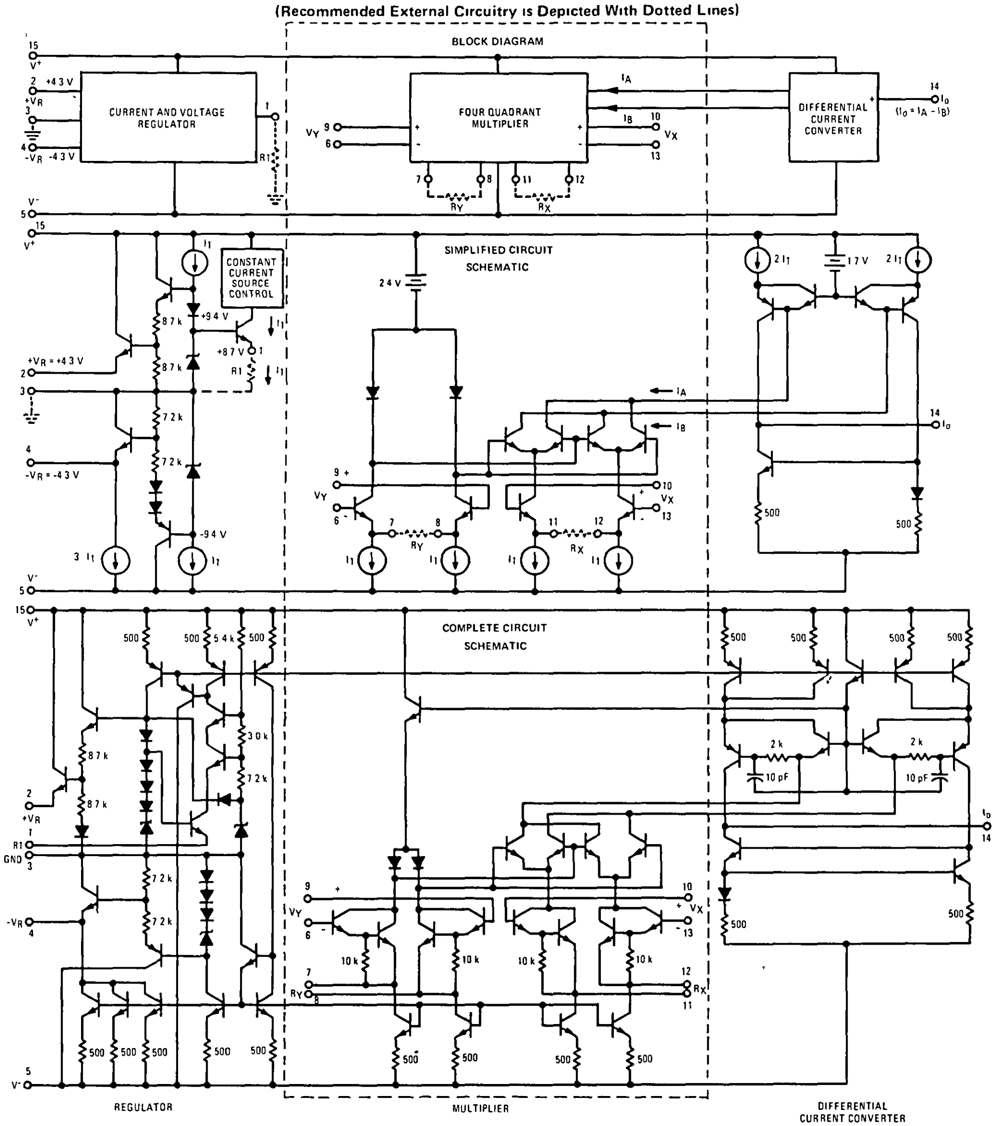
1. CIRCUIT DESCRIPTION

1.1 Introduction

The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features.

FIGURE 15
(Recommended External Circuitry is Depicted With Dotted Lines)



1.2 Regulator (Figure 15)

The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately -4 3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ) As will be shown later, there will normally be two 20 k-ohm potentiometers and one 50 k-ohm potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all current sources are related to current I_1 which is determined by R1. For best temperature performance, R1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications

1.3 Multiplier (Figure 15)

The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595" The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages

1.4 Differential Current Converter (Figure 15)

This portion of the circuitry converts the differential output current $(I_A - I_B)$ of the multiplier to a single-ended output current (I_O):

$$I_O = I_A - I_B$$

or

$$I_O = \frac{2V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (pin 14) to ground (Figure 17) or by using an op-ampl as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by.

$$V_O = \frac{2R_L V_X V_Y}{R_X R_Y I_1} = KV_X V_Y$$

$$\text{where K (scale factor)} = \frac{2R_L}{R_X R_Y I_1}$$

2. DC OPERATION

2.1 Selection of External Components

For low frequency operation the circuit of Figure 16 is recommended For this circuit, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, R1 = 16 kΩ and hence $I_1 \approx 0.5$ mA Therefore, to set the scale factor, K, equal to 1/10, the value of R_L can be calculated to be

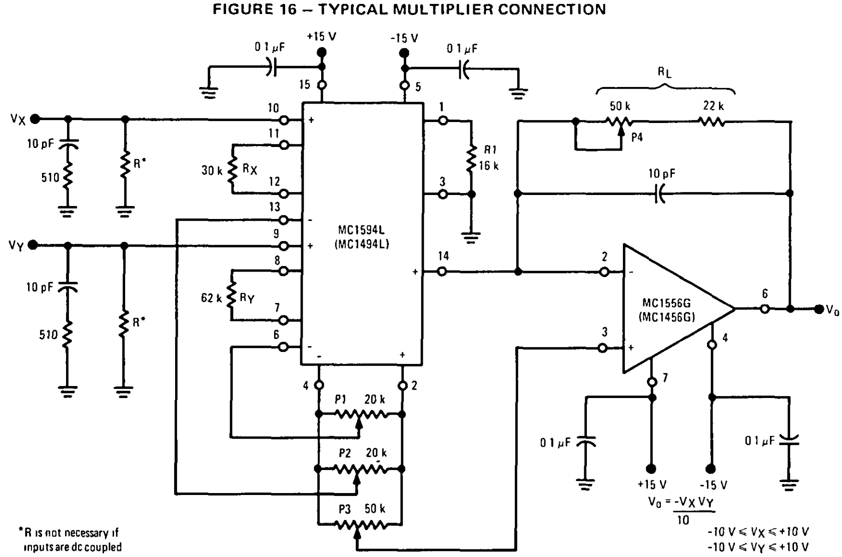
$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

$$\text{or} \quad R_L = \frac{R_X R_Y I_1}{(2)(10)} = \frac{(30\text{ k})(62\text{ k})(0.5\text{ mA})}{20}$$

$$R_L = 46.5\text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 kΩ resistor. However, if it is desired

FIGURE 16 – TYPICAL MULTIPLIER CONNECTION



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that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ±10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten For many applications it may be desirable to set K = 1/2 or K = 1 or even K = 100. This can be accomplished by adjusting R_X, R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 16 that R_Y is 62 kΩ while R_X is 30 kΩ. The reason for this is that the "Y" side of the multiplier exhibits a second order non-linearity whereas the "X" side exhibits a simple non-linearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the "X" and "Y" sides are made equal The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations

$R_X \geq 3\ V_X$ (max) in kΩ when V_X is in volts

$R_Y \geq 6\ V_Y$ (max) in kΩ when V_Y is in volts

For example, if the maximum input on the "X" side is ±1 volt, resistor R_X can be selected to be 3 kΩ. If the maximum input on the "Y" side is also ±1 volt, then resistor R_Y can be selected to be 6 kΩ (6 2 kΩ nominal value). If a scale factor of K = 10 is desired, the load resistor is found to be 47 kΩ In this example, the multiplier provides a gain of 20 dB.

2.2 Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op-ampl Since the offset current and bias currents of the op-ampl. will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-ampl., the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-ampl

2.3 Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op-ampls.) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-ampl. might be employed using slightly heavier compensation than that recommended for unity-gain operation

2.4 Offset Adjustment

The non-inverting input of the op-ampl. provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

2.5 Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is

A. X Input Offset
- (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 9)
- (b) connect "X" input (pin 10) to ground
- (c) adjust X-offset potentiometer, P2 for an ac null at the output

B Y Input Offset
- (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 10)
- (b) connect "Y" input (pin 9) to ground
- (c) adjust Y-offset potentiometer, P1 for an ac null at the output

C Output Offset
- (a) connect both "X" and "Y" inputs to ground
- (b) adjust output offset potentiometer, P3, until the output voltage V_O, is zero volts dc

D Scale Factor
- (a) apply +10 Vdc to both the "X" and "Y" inputs
- (b) adjust P4 to achieve -10 00 V at the output
- (c) apply -10 Vdc to both "X" and "Y" inputs and check for V_O = -10.00 V

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

2.6 Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components Previous discussion shows the direct dependence on R_X, R_Y, and R_L and indirect dependence on R1 (through I_1). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

2.7 Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current (≈ 0.5 μA) resistors, R (Figure 16) can be omitted. If the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 kΩ. For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

2.8 Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network is to reduce the "Q" of the source-tuned circuits which cause the oscillation.

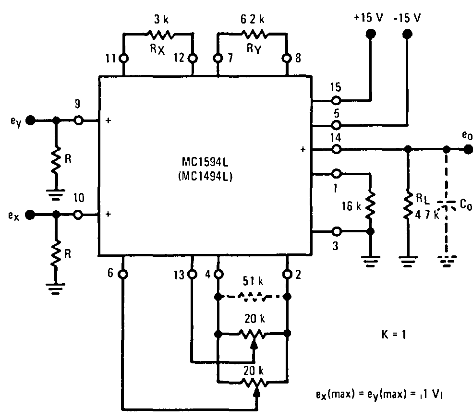
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation

3. AC OPERATION

3.1 General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc, the op-ampl. will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform Figure 17

FIGURE 17 – WIDEBAND MULTIPLIER



shows a typical ac multiplier circuit with a scale factor $K \approx 1$. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1594 is typically 17 μA and 35 μA maximum Thus, the maximum output offset would be about 160 mV.

3.2 Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance (C_O) of 10 pF, the 3 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The effect of these transmission "zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with the "X" input. For R_X = 30 kΩ and R_Y = 62 kΩ, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for ac applications; (1) the value of resistors R_X, R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole (R_L, C_O) cancels the input zero (R_X, 3 5 pF or R_Y, 3 5 pF) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10 Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal.

For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC1596 may be used up to 100 MHz For wideband multiplier applications, the MC1595 (using small collector loads and ac coupling) can be used

3.3 Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-ampl. is Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew-Rate} \ \frac{\Delta V_O}{\Delta T} = \frac{I_O}{C}$$

Thus, if C_O is 10 pF, the maximum slew-rate would be·

$$\frac{\Delta V_O}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50\ \text{V}/\mu\text{s}$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer.

3.4 Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector

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error is best explained by an example. If the "X" input is described in vector notation as

$$X = A \measuredangle 0^{o}$$

and the "Y" input is described as

$$Y = B \measuredangle 0^{o}$$

then the output product would be expected to be

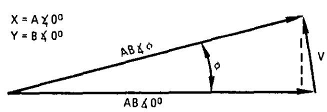
$$V_o = AB \measuredangle 0^{o} \text{ (see Figure 18)}$$

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by

$$V_o = AB \measuredangle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector, V, associated with this error is the "phase-vector error". The startling fact about the phase-vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57° will result in a 1% phase-vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase-vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase-vector error will represent a 1% amplitude error at the phase angle of interest.

FIGURE 18 – PHASE-VECTOR ERROR



3.5 **Circuit Layout**

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across R_X and R_Y should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

4. DC APPLICATIONS

4.1 Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_o = KV^2$$

where K is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_o = K(V_x + V_{iox} - V_{x\,off})(V_y + V_{ioy} - V_{y\,off}) + V_{oo}$$

(See "Definitions" for an explanation of terms).

With $V_x = V_y = V$ (squaring) and defining

$$\epsilon_x = V_{iox} - V_{x\,off}$$

$$\epsilon_y = V_{ioy} - V_{y\,off}$$

The output voltage equation becomes

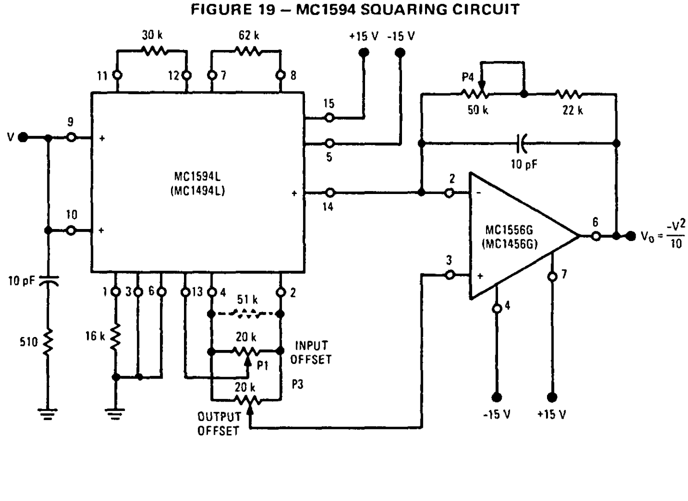
$$V_o = K\,V_x^2 + KV_x(\epsilon_x + \epsilon_y) + K\epsilon_x\epsilon_y + V_{oo}$$

This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, ϵ_x is determined by the internal offset, V_{iox}, but ϵ_y is adjustable to the extent that the $(\epsilon_x + \epsilon_y)$ term can be zeroed. Then the output offset adjustment is used to adjust the V_{oo} term and thus zero the remaining error terms. An ac procedure for nulling with three adjustments is:

A. AC Procedure.

1. Connect oscillator (1 kHz, 15 Vpp) to input
2. Monitor output at 2 kHz with tuned voltmeter and adjust P4 for desired gain (Be sure to peak response of voltmeter)
3. Tune voltmeter to 1 kHz and adjust P1 for a minimum output voltage
4. Ground input and adjust P3 (output offset) for zero volts dc out
5. Repeat steps 1 through 4 as necessary.

FIGURE 19 – MC1594 SQUARING CIRCUIT



B. DC Procedure:

1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_o = 0.0$ Vdc
2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is -0.100 volts
3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is -10.00 volts
4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10$V

Repeat steps 1 through 4 as necessary.

4.2 Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21

The characteristic "failure" mode of the divide circuit is latch-up One way it can occur is if V_X is allowed to go negative or, in some cases, if V_X approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-ampl. Thus, operation is in the negative feedback mode and the circuit is dc stable. Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from V_X being near zero is a result of the transfer through the multiplier being near zero. The op-ampl. is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-ampl. exceeding the rated common-mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-ampl. to approximately ± 10 7 volts. Five-percent tolerance, 10-volt zeners are used to assure adequate output swing but still limit the output voltage of the op-ampl. from exceeding the common-mode input range of the MC1594.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P3) until the output voltage (V_O) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 volt and +10 volts.
2. Maintain V_Z at 0 volts, set V_X at +10 volts and adjust the Y input offset potentiometer (P1) until $V_o = 0$ volts.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily - 10 volts) constant value as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiometer (R_L) until the average value of V_o is -10 volts as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-

FIGURE 20 — BASIC DIVIDE CIRCUIT USING MULTIPLIER

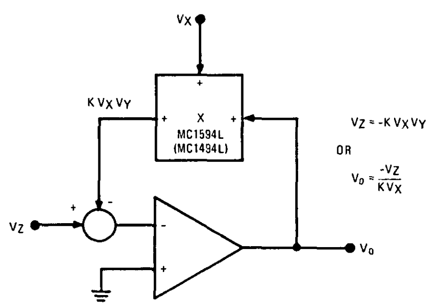


FIGURE 21 — PRACTICAL DIVIDE CIRCUIT

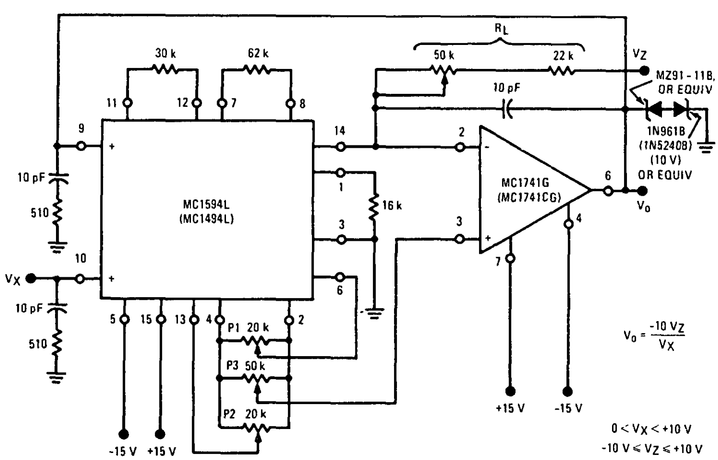
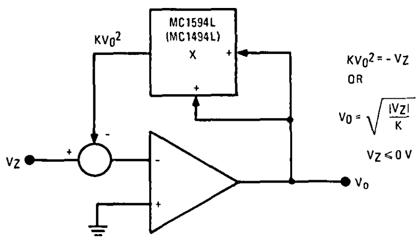


FIGURE 22 – BASIC SQUARE ROOT CIRCUIT



nator voltage. As a result, if V_X is set to 10 volts and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1 volt.

In accordance with an earlier statement, V_X may have only one polarity, positive, while V_Z may be either polarity.

4.3 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode

1. Set V_Z = -0.01 Vdc and adjust P3 (output offset) for V_O = 0.316 Vdc.
2. Set V_Z to -0.9 Vdc and adjust P2 ("X" adjust) for V_O = +3 Vdc.
3. Set V_Z to -10 Vdc and adjust P4 (gain adjust) for V_O = +10 Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy

Note. Operation near zero volts input may prove very inaccurate, hence, it may not be possible to adjust V_O to 0 but rather only to within 100 to 400 mV of zero.

5. AC APPLICATIONS

5.1 Wideband Amplifier With Linear AGC

If one input to the MC1594 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control

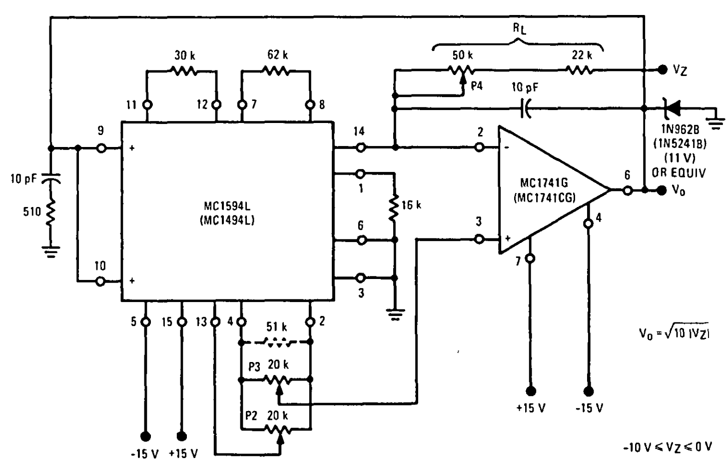
In addition to the advantage of Linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage-swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1 V(rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1 MHz.

5.2 Balanced Modulator

When two-time variant signals are used as inputs, the result-

FIGURE 23 – SQUARE ROOT CIRCUIT



ing output is suppressed-carrier double-sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

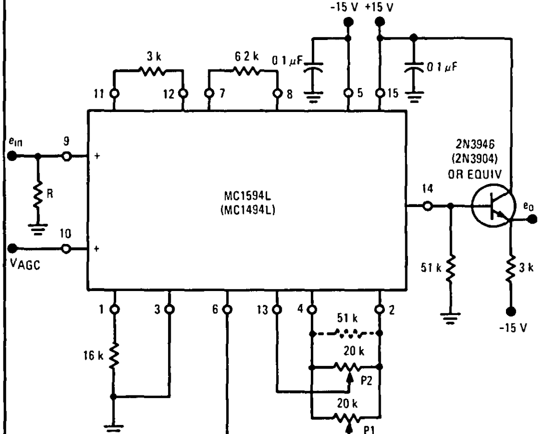
$$V_o = K(e_1 \cos\omega_m t)(e_2 \cos\omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_o = \frac{Ke_1e_2}{2}\left[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t\right]$$

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

FIGURE 24 – WIDEBAND AMPLIFIER WITH LINEAR AGC

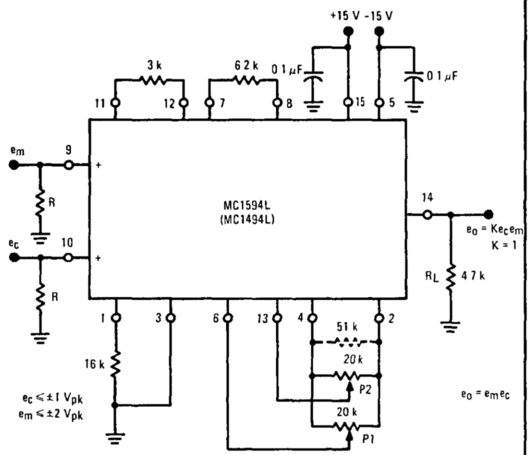


Notice that the resistor values for R_X, R_Y, and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1 volt peak and e_m as high as 2 volts peak. No output offset adjust is employed since we are interested only in the ac output components.

The input R's are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of ≥70 dB from 10 kHz to 1.5 MHz.

FIGURE 25 – BALANCED MODULATOR



The adjustment procedure for this circuit is quite simple.

(1) Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.

(2) Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

5.3 Frequency Doubler

If for Figure 25 both inputs are identical;

$$e_m = e_c = E\cos\omega t$$

Then the output is given by

$$e_o = e_me_c = E^2\cos^2\omega t$$

which reduces to

$$e_o = \frac{E^2}{2}(1 + \cos 2\omega t)$$

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

5.4 Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modu-

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lation input. This procedure places a dc offset on the modulation input of the multiplier such that the carrier still passes thru the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with K = 1,

$$e_o = (E + E_m \cos\omega_m t)\,(E_c \cos\omega_c t)$$

where E is the dc input offset adjust voltage. This expression can be written as.

$$e_o = E_o\,[1 + M \cos\omega_c t]\,\cos\omega_c t$$

where $E_o = EE_c$

and $M = \frac{E_m}{E}$ = modulation index

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, E_m. This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

5.5 Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency but having a relative phase shift the output will be a dc signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos\omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos\omega_c t \cos(\omega_c t + \phi)$$

or

$$e_o = \frac{E_c E_m}{2}\,[\cos\phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

6. DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

6.1 Multiplier Transfer Function

The output of the multiplier may be expressed by this equation:

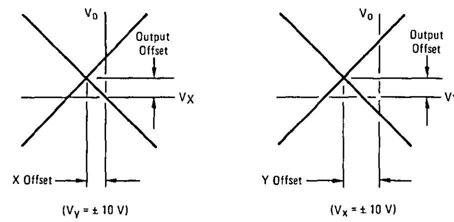
$$V_o = K\,(V_x \pm V_{iox} - V_{x\,off})\,(V_y \pm V_{ioy} - V_{y\,off}) \pm V_{oo} \quad (1)$$

where K = scale factor (see 6.5)

V_x = "x" input voltage
V_y = "y" input voltage
V_{iox} = "x" input offset voltage
V_{ioy} = "y" input offset voltage
$V_{x\,off}$ = "x" input offset adjust voltage
$V_{y\,off}$ = "y" input offset adjust voltage
V_{oo} = output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

FIGURE 26



6.2 Linearity

Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for V_x and V_y separately either using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_o = \frac{V_x V_y}{10} \pm (0.0035)\,(10 \text{ volts})$$

6.3 Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for V_x and V_y separately and is defined to be that dc input offset adjust voltage ("x" or "y") that will result in minimum ac output when ac (5 Vpp, 1 kHz) is applied to the other input ("y" or "x" respectively). From Equation (1) we have:

$$V_{o(ac)} = K\,(0 \pm V_{iox} - V_{x\,off})\,(\sin\omega t)$$

adjust $V_{x\,off}$ so that $(\pm V_{iox} - V_{x\,off}) = 0$

6.4 Output Offset Current and Voltage

Output offset current (I_{oo}) is the dc current flowing in the output lead when $V_x = V_y = 0$ and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage (V_{oo}) is

$$V_{oo} = I_{oo} R_L$$

where R_L is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

6.5 Scale Factor

Scale factor is the K term in Equation (1). It determines the "gain" of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_x R_y I_1} \text{ where } R_x \text{ and } R_y \gg \frac{kT}{qI_1}$$

and I_1 is the current out of pin 1.

6.6 Total DC Accuracy

The total dc accuracy of a multiplier is defined as error in multiplier output with dc (±10 Vdc) applied to both inputs It is expressed as a percent of full scale Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

6.7 Temperature Stability (Drift)

Each term defined above will have a finite drift with temperature The temperature specifications are obtained by re-adjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by

$$\Delta V_O = \pm[K \pm K\ (TCK)\ (\Delta T)\ ]\ [\ (TCV_{IOX})\ (\Delta T)\ ]\ [\ (TCV_{IOY})\ (\Delta T)\ ]\ \pm\ (TCV_{OO})\ (\Delta T)$$

6.8 Total DC Accuracy Drift

This is the temperature drift in output voltage with 10 volts applied to each input The output is adjusted to 10 volts at $T_A = +25^oC$ Assuming initial offset voltages have been adjusted to zero at $T_A = +25^oC$, then

$$V_O = [K \pm K\ (TCK)\ (\Delta T)\ ]\ [10 \pm (TCV_{IOX})\ (\Delta T)\ ]\ [10 \pm (TCV_{IOY})\ (\Delta T)\ ]\ \pm\ (TCV_{OO})\ (\Delta T)$$

6.9 Power Supply Rejection

Variation in power supply voltages will cause undesired variation of the output voltage It is measured by superimposing a 1-volt, 100-Hz signal on each supply (±15 V) with each input grounded The resulting change in the output is expressed in mV/V

6.10 Output Voltage Swing

Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (note-output offset is adjusted to zero)

If an op-ampl is used, the multiplier output becomes a virtual ground — the swing is then determined by the scale factor and the op-ampl. selected

GENERAL INFORMATION INDEX

ORDERING INFORMATION

Device	Temperature Range	Package
MC1495L	0°C to +70°C	Ceramic DIP
MC1595L	−55°C to +125°C	Ceramic DIP

MC1495L
MC1595L

Specifications and Applications Information

WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

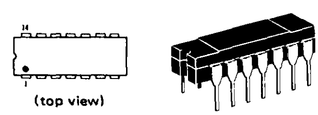
. . . designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

- Wide Bandwidth
- Excellent Linearity – 1% max Error on X-Input, 2% max Error on Y-Input – MC1595L
- Excellent Linearity – 2% max Error on X-Input, 4% max Error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 – FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC

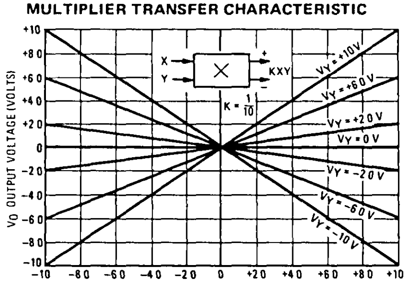


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

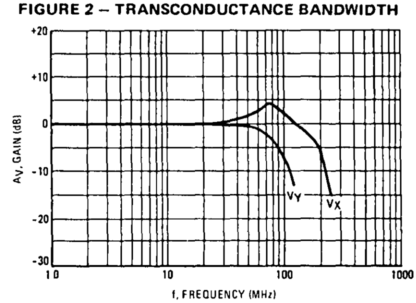
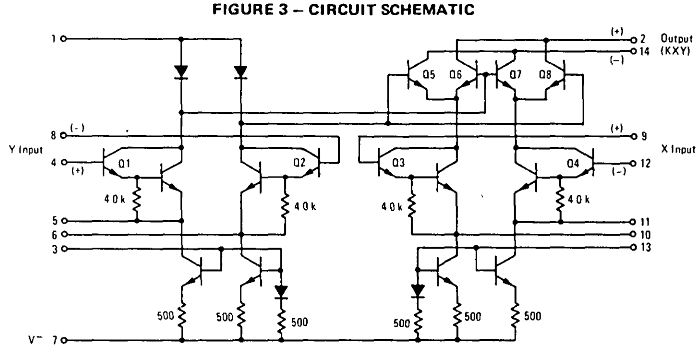


FIGURE 3 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (V^+ = +32V, V^- = -15 V, T_A = +25°C, $I_3 = I_{13}$ = 1 mA, $R_X = R_Y$ = 15 kΩ, R_L = 11 kΩ unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Linearity:							
Output Error in Percent of Full Scale:		5					%
T_A = +25°C							
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)	MC1495		E_{RX}	–	± 1.0	± 2.0	
	MC1595			–	± 0.5	± 1.0	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)	MC1495		E_{RY}	–	± 2.0	± 4.0	
	MC1595			–	± 1.0	± 2.0	
T_A = 0 to +70°C	MC1495						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	–	± 1.5	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	–	± 3.0	–	
T_A = -55°C to +125°C	MC1595						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	–	± 0.75	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	–	± 1.50	–	
Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment		5	E_{SQ}				%
T_A = +25°C	MC1495			–	± 0.75	–	
	MC1595			–	± 0.5	–	
T_A = 0 to +70°C	MC1495			–	± 1.0	–	
T_A = -55°C to +125°C	MC1595			–	± 0.75	–	
Scale Factor (Adjustable) $\left(K = \frac{2R_L}{I_3 R_X R_Y}\right)$		–	K		0.1	–	–
Input Resistance (f = 20 Hz)	MC1495	7	R_{INX}	–	20	–	MegOhms
	MC1595			–	35	–	
	MC1495		R_{INY}	–	20	–	
	MC1595			–	35	–	
Differential Output Resistance (f = 20 Hz)		8	R_o	–	300	–	k Ohms
Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	MC1495	6	I_{bx}	–	2.0	12	μA
	MC1595			–	2.0	8.0	
	MC1495		I_{by}	–	2.0	12	
	MC1595			–	2 0	8.0	
Input Offset Current $\lvert I_9 - I_{12} \rvert$	MC1495	6	$\lvert I_{iox} \rvert$	–	0.4	2.0	μA
	MC1595			–	0.2	1.0	
$\lvert I_4 - I_8 \rvert$	MC1495		$\lvert I_{ioy} \rvert$	–	0.4	2.0	
	MC1595			–	0.2	1.0	
Average Temperature Coefficient of Input Offset Current		6	$\lvert TC_{Iio} \rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495			–	2.0	–	
(T_A = -55°C to +125°C)	MC1595			–	2.0	–	
Output Offset Current $\lvert I_{14} - I_2 \rvert$		6	$\lvert I_{oo} \rvert$				μA
	MC1495			–	20	100	
	MC1595			–	10	50	
Average Temperature Coefficient of Output Offset Current		6	$\lvert TC_{Ioo} \rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495			–	1.0	–	
(T_A = -55°C to +125°C)	MC1595			–	1.0	–	
Frequency Response							
3.0 dB Bandwidth, R_L = 11 kΩ		9,10	BW_{3dB}	–	3.0	–	MHz
3.0 dB Bandwidth, R_L = 50 Ω (Transconductance Bandwidth)			$T_{BW3\,dB}$	–	80	–	MHz
3° Relative Phase Shift Between V_X and V_Y			f_ϕ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift			f_θ	–	30	–	kHz
Common Mode Input Swing (Either Input)		11	CMV				Vdc
	MC1495			±10.5	±12	–	
	MC1595			±11.5	±13	–	
Common Mode Gain (Either Input)		11	A_{CM}				dB
	MC1495			-40	-50	–	
	MC1595			-50	-60	–	
Common Mode Quiescent Output Voltage		12	V_{o1}	–	21	–	Vdc
			V_{o2}	–	21	–	
Differential Output Voltage Swing Capability		9	V_o	–	±14	–	V_{peak}
Power Supply Sensitivity		12	S^+	–	5.0	–	mV/V
			S^-	–	10	–	
Power Supply Current		12	I_7	–	6.0	7.0	mA
DC Power Dissipation		12	P_D	–	135	170	mW

6

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2-V_1, $V_{14}-V_1$, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, $V_{12}-V_7$, V_9-V_7, V_8-V_7, V_4-V_7)	ΔV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+I_{13}R_X)$ $\pm(6+I_3R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 750 5.0	 mW mW/°C
Operating Temperature Range MC1495 MC1595	T_A	 0 to +70 -55 to +125	°C °C
Storage Temperature Range	T_{stg}	-65 to +150	°C

6

TEST CIRCUITS

FIGURE 4 — LINEARITY (USING NULL TECHNIQUE)

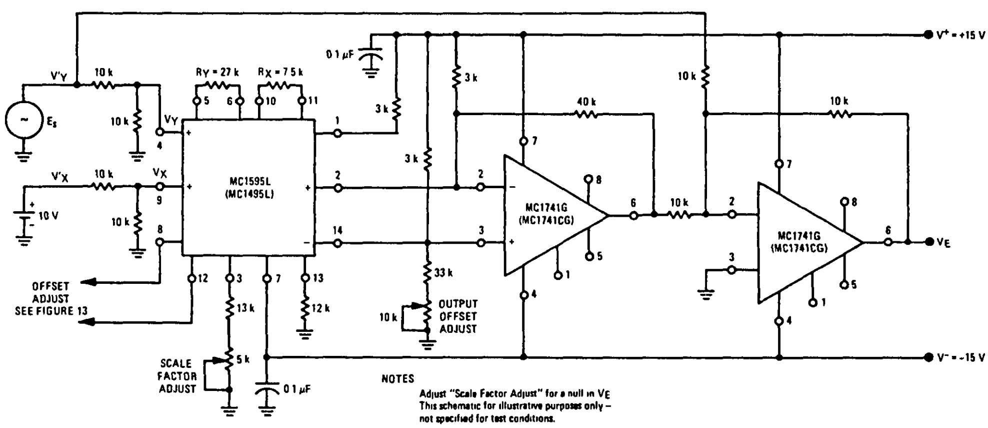
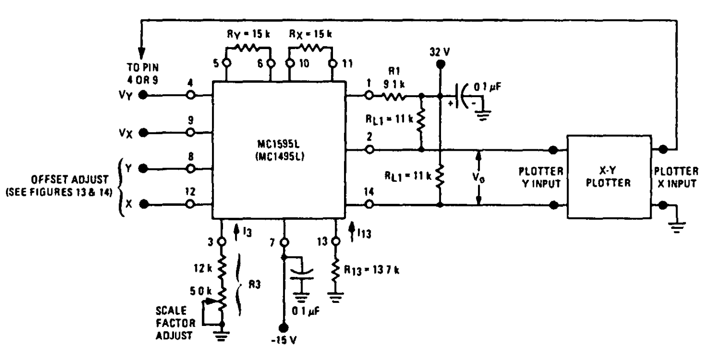


FIGURE 5 — LINEARITY (USING X-Y PLOTTER TECHNIQUE)



TEST CIRCUITS (continued)

FIGURE 6 — INPUT AND OUTPUT CURRENT

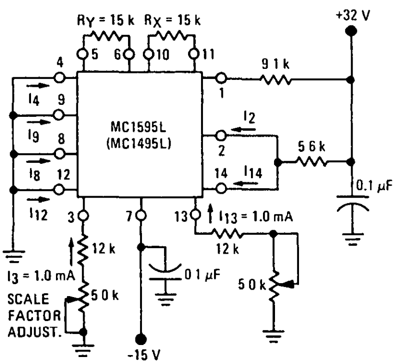


FIGURE 7 — INPUT RESISTANCE

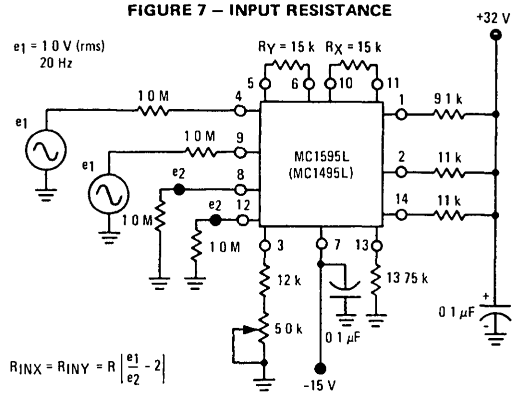


FIGURE 8 — OUTPUT RESISTANCE

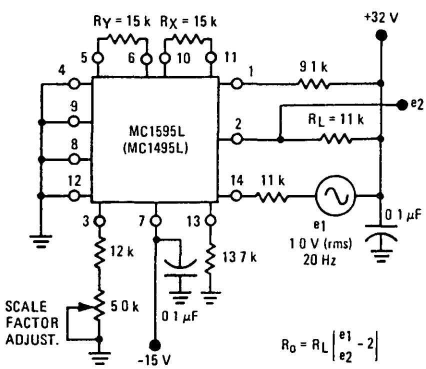


FIGURE 9 — BANDWIDTH (RL = 11 kΩ)

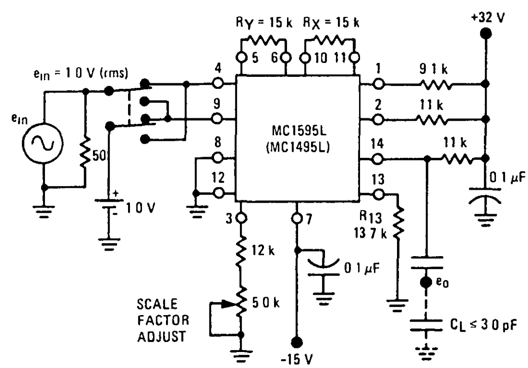


FIGURE 10 — BANDWIDTH (RL = 50 Ω)

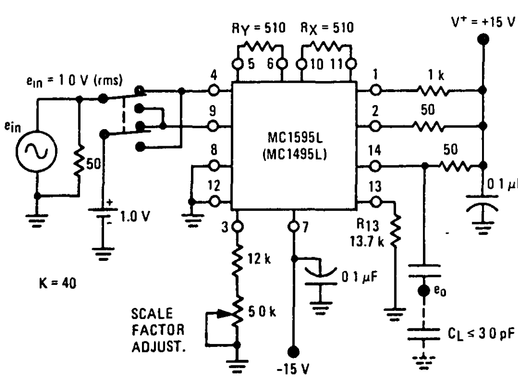
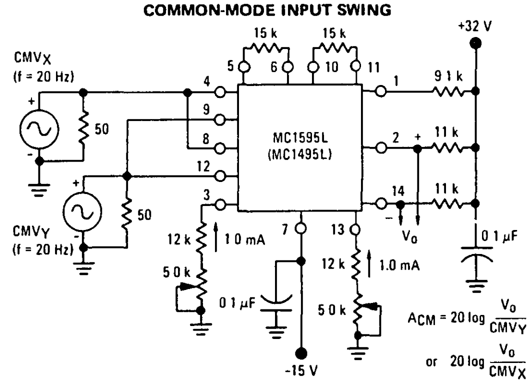


FIGURE 11 — COMMON-MODE GAIN and COMMON-MODE INPUT SWING



TEST CIRCUITS (continued)

FIGURE 12 – POWER SUPPLY SENSITIVITY

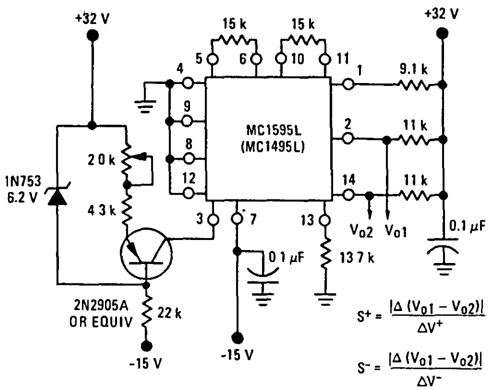
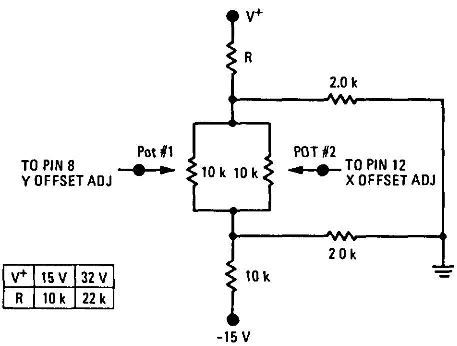
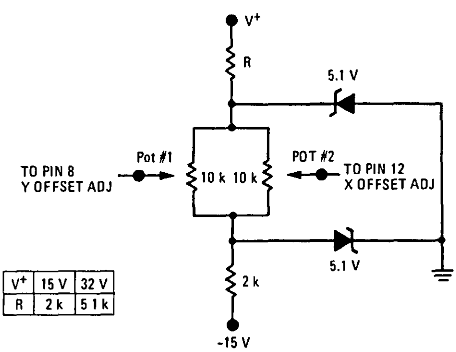


FIGURE 13 – OFFSET ADJUST CIRCUIT



V+	15 V	32 V
R	10 k	22 k

FIGURE 14 – OFFSET ADJUST CIRCUIT (ALTERNATE)



V+	15 V	32 V
R	2 k	5.1 k

TYPICAL CHARACTERISTICS

FIGURE 15 – LINEARITY versus TEMPERATURE

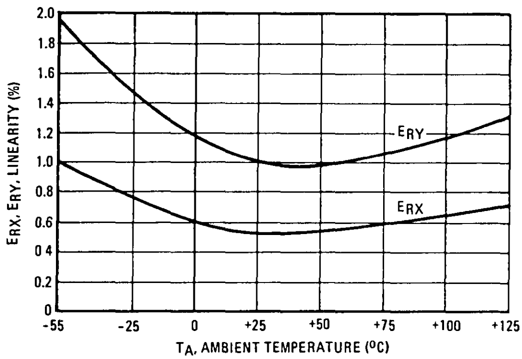


FIGURE 16 – SCALE FACTOR versus TEMPERATURE

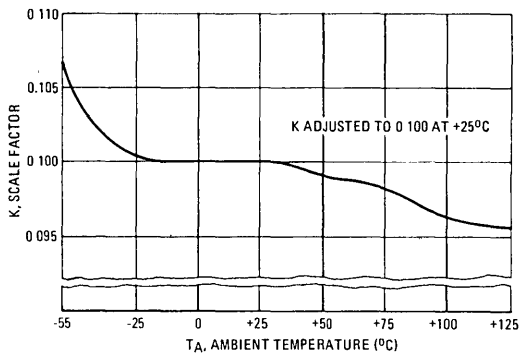


FIGURE 17 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

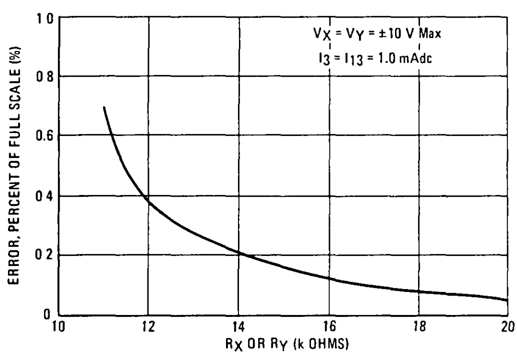


FIGURE 18 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

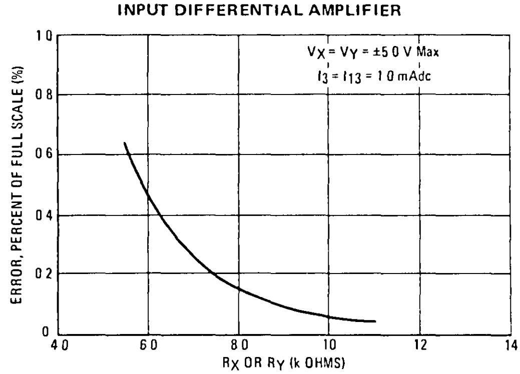
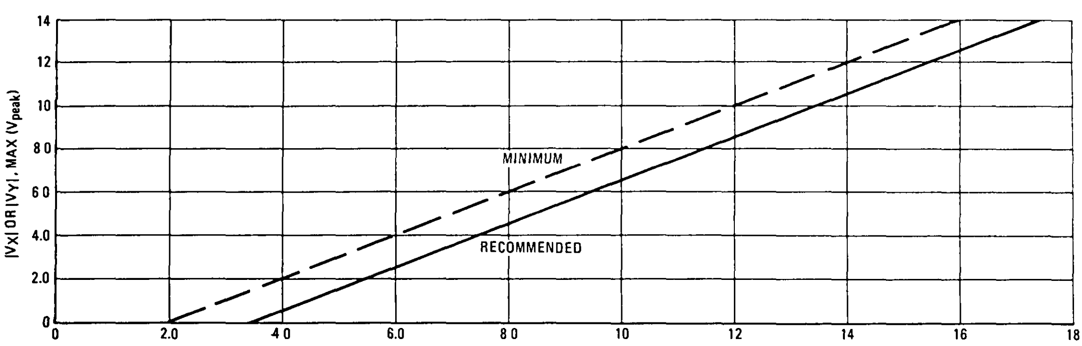


FIGURE 19 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



6

6

OPERATION AND APPLICATIONS INFORMATION

1. Theory of Operation

The MC1595 (MC1495) is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. The detailed theory of operation is covered in Application Note AN-489, Analysis and Basic Operation of the MC1595. The result of this analysis is that the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_XV_Y}{R_XR_YI_3}$$

where I_A and I_B are the currents into pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals

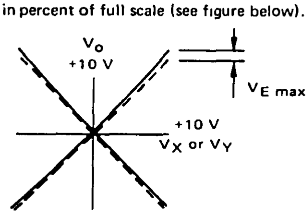
2. Design Considerations

2 1 General

The MC1595 (MC1495) permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

2.1.1 Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 volts, then the percentage error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X – Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_{E(max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

2.1.2 3 dB-Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

2.1.3 Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ maximum input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y.$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause non-linear operation.

Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ volts;

$$R_X = R_Y > \frac{10\ V}{1\ 0\ mA} = 10\ k\Omega.$$

The equation $I_A - I_B = \dfrac{2V_XV_Y}{R_XR_YI_3}$

is derived from $I_A - I_B = \dfrac{2V_XV_Y}{\left(R_X + \frac{2kT}{qI_{13}}\right)\left(R_Y + \frac{2kT}{qI_3}\right) I_3}$

with the assumption $R_X \gg \dfrac{2kT}{qI_{13}}$ and $R_Y \gg \dfrac{2kT}{qI_3}$.

At $T_A = +25°C$ and $I_{13} = I_3 = 1$ mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

Therefore, with $R_X = R_Y = 10$ kΩ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of Section 3 (General Design Procedure) for further details.

2.1.4 Maximum Output Voltage Swing

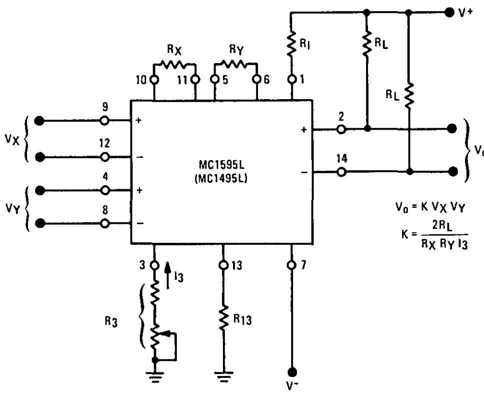
The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7, and Q_8. This potential

OPERATION AND APPLICATIONS INFORMATION (continued)

should be related so that negative swing at pins 2 or 14 does not saturate those transistors. See Section 3 for further information regarding selection of these potentials.

FIGURE 20 – BASIC MULTIPLIER



If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

3. General Design Procedure

Selection of component values is best demonstrated by the following example. assume resistive dividers are used at the X and Y inputs to limit the maximum multiplier input to ±5.0 volts ($V_X = V_{Y[max]}$) for a ±10-volt input ($V_X' = V_Y'_{[max]}$). (See Figure 21). If an overall scale factor of 1/10 is desired, then

$$V_o = \frac{V_X' \, V_Y'}{10} = \frac{(2V_X)\,(2V_Y)}{10} = 4/10 \; V_X V_Y .$$

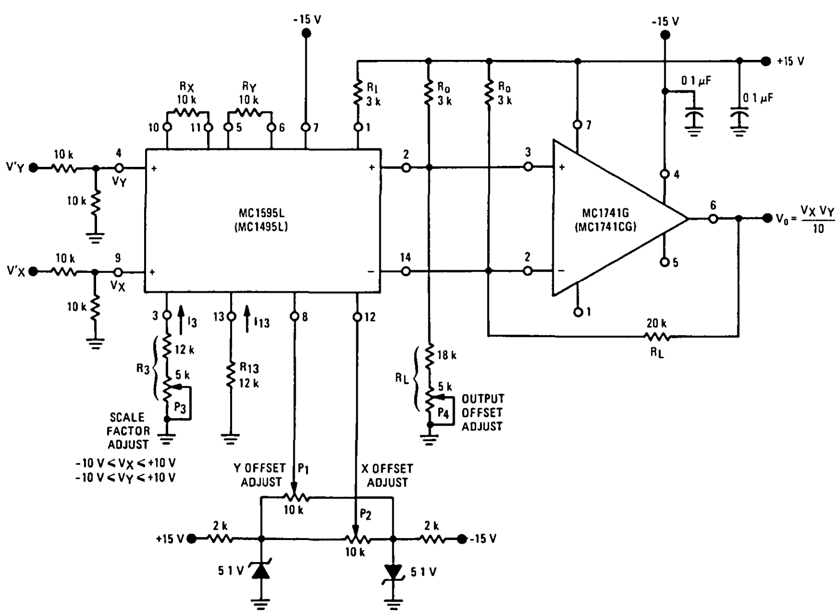
Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The first step is to select current I_3 and current I_{13}. There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be one or two milliamperes. Further, I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1 \text{ mA}.$$

To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between pin 13 and ground, and between pin 3 and ground. From the schematic shown in Figure 3,

FIGURE 21 – MULTIPLIER WITH OP-AMPL. LEVEL SHIFT



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OPERATION AND APPLICATIONS INFORMATION (continued)

it can be seen that the resistor values necessary are given by:

$$R_{13} + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_{13}}$$

$$R_3 + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_3}$$

Let $V^- = -15\ V$

Then $R_{13} + 500 = \frac{14.3\ V}{1\ mA}$ or $R_{13} = 13.8\ k\Omega$

Let $R_{13} = 12\ k\Omega$

Similarly, $R_3 = 13.8\ k\Omega$

Let $R_3 = 15\ k\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the single resistor would have a value of one-half the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \qquad \frac{V_Y}{R_Y} < I_3.$$

A good rule of thumb is to make $I_3R_Y \geqslant 1.5\ V_{Y(max)}$ and $I_{13}R_X \geqslant 1.5\ V_{X(max)}$.

The larger the I_3R_Y and $I_{13}R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y = 10\ k\Omega$

Then $I_3R_Y = 10\ V$

$I_{13}R_X = 10\ V$

since $V_{X(max)} = V_{Y(max)} = 5.0$ volts the value of $R_X = R_Y = 10\ k\Omega$ is sufficient

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined

$$K = \frac{2R_L}{R_XR_YI_3} = \frac{4}{10}$$

or $$\frac{(2)\ (R_L)}{(10\ k)\ (10\ k)\ (1\ mA)} = \frac{4}{10}$$

Thus $R_L = 20\ k\Omega$.

Step 4. To determine what power-supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_X' = V_Y' = 10$ V or $V_X = 5.0$ V, $V_Y = 5.0$ V), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 are at a potential which is two diode-drops below the voltage at pin 1. Thus, the voltage at pin 1 should be about two volts higher than the maximum input voltage. Therefore, to handle +5.0 volts at the inputs, the voltage at pin 1 must be at least +7.0 volts. Let $V_1 = 9.0$ Vdc.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, R_1 from pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

Let $V^+ = +15\ V$

Then $R_1 = \frac{15\ V - 9\ V}{(2)\ (1\ mA)}$

$R_1 = 3\ k\Omega$.

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode-drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive-supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

Step 5. Level Shifting

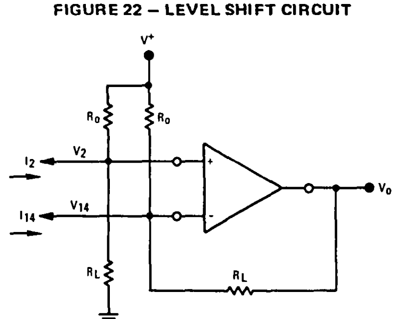
For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_o = (I_2 - I_{14})\, R_L$$

And since $I_A - I_B = I_2 - I_{14} = \frac{2I_XI_Y}{I_3} = \frac{2\ V_XV_Y}{I_3R_XR_Y}$

Then $V_o = \frac{2R_LV_X'V_Y'}{4R_XR_XI_3}$ where $V_X'V_Y'$ is the voltage at the input to the voltage dividers.

FIGURE 22 — LEVEL SHIFT CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common-mode input voltage range as well as a high common-mode rejection ratio. The MC1556, and MC1741 operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20 kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 volts. From this information, R_o can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V_2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_o}$$

And for this example, $\frac{11\ V}{20\ k\Omega} + 1\ mA = \frac{15\ V - 11\ V}{R_o}$

Solving for R_o, R_o = 2.6 kΩ

Thus, select R_o = 3.0 kΩ

For R_o = 3.0 kΩ, the voltage at pins 2 and 14 is calculated to be

$$V_2 = V_{14} = 10.4 \text{ volts.}$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity, and R_X decreased somewhat so as not to materially affect the X linearity, this avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1595 (MC1495) allows the user to to optimize its performance for various input and output signal levels.

4. Offset and Scale Factor Adjustment

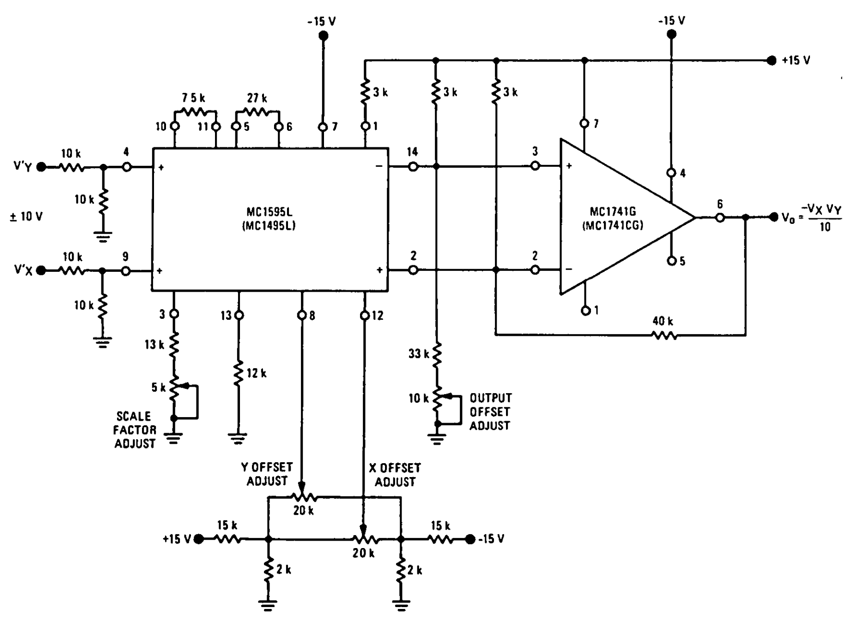
4.1 Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output-offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function.

$$V_o = K(V_X \pm V_{IOX} \pm V_{X\ off})(V_Y \pm V_{IOY} \pm V_{Y\ off}) \pm V_{oo} \quad (1)$$

Where K = scale factor
- V_X = X input voltage
- V_Y = Y input voltage
- V_{IOX} = X input offset voltage
- V_{IOY} = Y input offset voltage
- $V_{X\ off}$ = X input offset adjust voltage
- $V_{Y\ off}$ = Y input offset adjust voltage
- V_{oo} = output offset voltage.

FIGURE 23 — MULTIPLIER WITH IMPROVED LINEARITY



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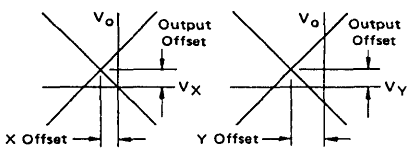
OPERATION AND APPLICATIONS INFORMATION (continued)

X, Y and Output Offset Voltages



For most dc applications, all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (See Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

4.2 Scale Factor

The scale factor, K, is set by P_3(Figure 21). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one-half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (See Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see Section 3, General Design Procedure).

4.3 Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 21)

1. X Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 4)
   (b) Connect "X" input (pin 9) to ground
   (c) Adjust X offset potentiometer, P_2, for an ac null at the output
2. Y Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 9)
   (b) Connect "Y" input (pin 4) to ground
   (c) Adjust "Y" offset potentiometer, P_1, for an ac null at the output
3. Output Offset
   (a) Connect both "X" and "Y" inputs to ground
   (b) Adjust output offset potentiometer, P_4, until the output voltage V_o is zero volts dc
4. Scale Factor
   (a) Apply +10 Vdc to both the "X" and "Y" inputs
   (b) Adjust P_3 to achieve + 10.00 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1595 (MC1495) depends upon the characteristics of potentiometers P_1 through P_4. Multi-turn, infinite resolution potentiometers with low-temperature coefficients are recommended.

5. DC Applications

5.1 Multiply

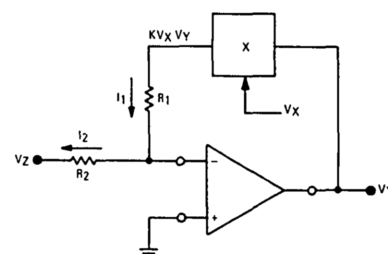
The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large – however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

5.2 Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_o = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

1. AC Procedure:
   (a) Connect oscillator (1 kHz, 15 Vpp) to input
   (b) Monitor output at 2 kHz with tuned voltmeter and adjust P_3 for desired gain (be sure to peak response of the voltmeter)
   (c) Tune voltmeter to 1 kHz and adjust P_1 for a minimum output voltage
   (d) Ground input and adjust P_4 (output offset) for zero volts dc output
   (e) Repeat steps a through d as necessary.
2. DC Procedure:
   (a) Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_o = 0.0$ Vdc
   (b) Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y input offset potentiometer) such that the output voltage is +0.100 volts
   (c) Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is +10.00 volts
   (d) Set $V_X = V_Y = -10$ Vdc. Repeat steps a through d as necessary.

FIGURE 24 – BASIC DIVIDE CIRCUIT



5.3 Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (–) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \tag{1}$$

Solving for V_Y,

$$V_Y = \frac{-R1}{R2\,K}\,\frac{V_Z}{V_X}. \tag{2}$$

If R1 = R2

$$V_Y = \frac{-V_Z}{KV_X} \tag{3}$$

If R1 = KR2

$$V_Y = \frac{-V_Z}{V_X}. \tag{4}$$

OPERATION AND APPLICATIONS INFORMATION (continued)

Hence, the output voltage is the ratio of V_Z to V_X and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be

$$V_Y = -\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X} + \frac{\Delta E}{K V_X} \qquad (5)$$

where ΔE is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y. For example, assume that R1 = R2, and K = 1/10. For these conditions the output of the divide circuit is given by

$$V_Y = \frac{-10\,V_Z}{V_X} + \frac{10\,\Delta E}{V_X}\,. \qquad (6)$$

From equation 6, it is seen that only when V_X = 10 V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small, (0.1 volt) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from equation (5),

$$P.E._D = \frac{\dfrac{\Delta E}{K V_X}}{\left[\dfrac{R1}{R2\,K}\right]\dfrac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z}\,. \qquad (7)$$

From equation 7, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25.

1. The input voltage (V'_X) must be greater than zero and must be positive. This insures that the current out of pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z.
2. Pins 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

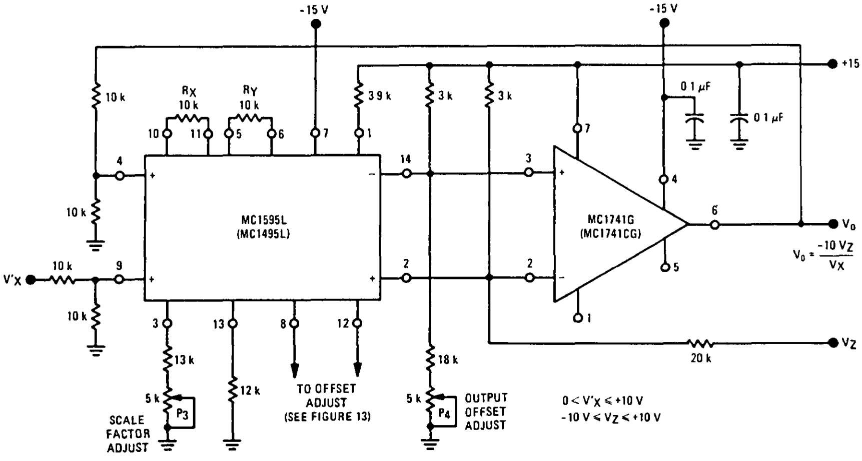
A Suggested Adjustment Procedure for the Divide Circuit

1. Set V_Z = 0 volts and adjust the output offset potentiometer (P_4) until the output voltage (V_o) remains at some (not necessarily zero) constant value as V_X' is varied between +1.0 volt and +10 volts.
2. Keep V_Z at 0 volts, set V_X' at +10 volts and adjust the Y input offset potentiometer (P_1) until V_o = 0 volts.
3. Let V_X' = V_Z and adjust the X input offset potentiometer (P_2) until the output voltage remains at some (not necessarily − 10 volts) constant value as V_Z = V_X' is varied between +1.0 and +10 volts
4. Keep V_X' = V_Z and adjust the scale factor potentiometer (P_3) until the average value of V_o is − 10 volts as V_Z = V_X' is varied between +1.0 volt and +10 volts
5. Repeat steps 1 through 4 as necessary to achieve optimum performance

5.4 Square Root

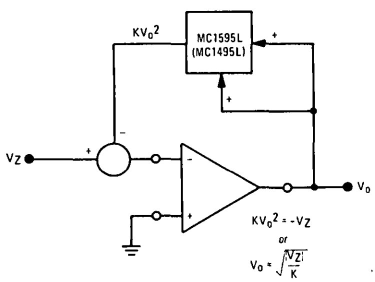
A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function

FIGURE 25 — DIVIDE CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 26 – BASIC SQUARE ROOT CIRCUIT



as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set V_Z to −0 01 volts and adjust P_4 (output offset) for V_o = +0 316 volts, being careful to approach the output from the positive side to preclude the effect of the output diode clamping
2. Set V_Z to −0 9 volts and adjust P_2 (X adjust) for V_o = +3.0 volts.
3. Set V_Z to −10 volts and adjust P_3 (scale factor adjust) for V_o = +10 volts.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

6. AC Applications

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications

6.1 Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling

$$e_o = KE^2 \cos^2 \omega t$$

$$e_o = \frac{KE^2}{2}(1 + \cos 2\omega t).$$

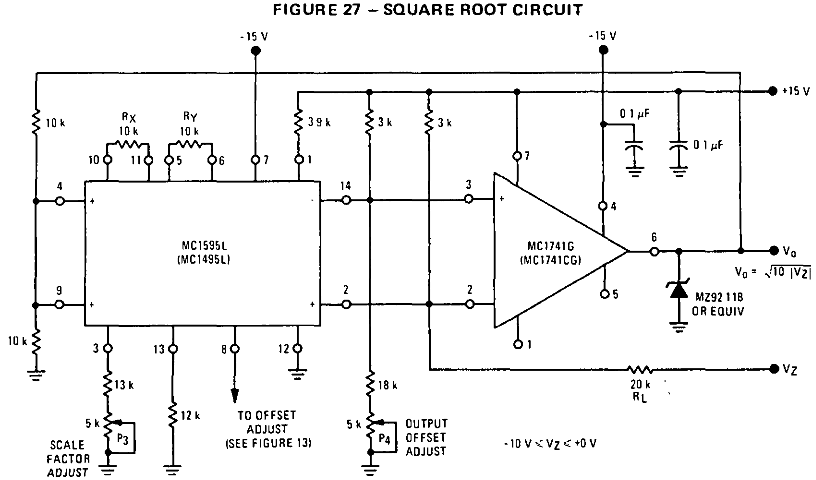
A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplifier. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15-volt supplies are used. An input dynamic range of 5.0 volts peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

A slightly modified version of the MC1595 (MC1495) – the MC1596 (MC1496) – has been successfully used as a doubler to obtain 400 MHz. (See Figure 28)

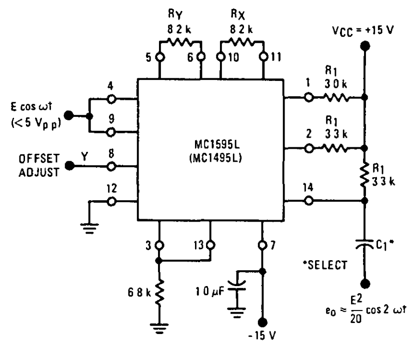
6.2 Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

FIGURE 27 – SQUARE ROOT CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

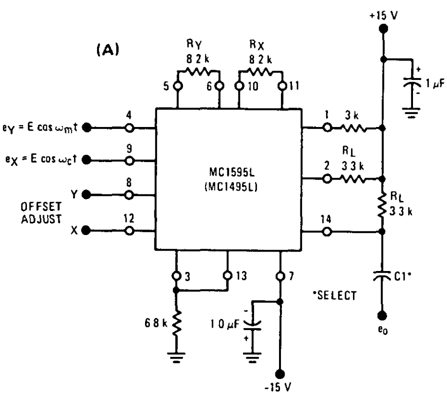
FIGURE 28 – FREQUENCY DOUBLER



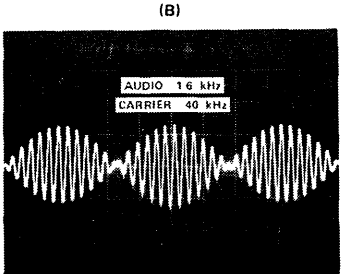
When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

FIGURE 29 – BALANCED MODULATOR

(A)



(B)



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)\,(E_c \cos \omega_c t) =$$

$$\frac{KE_cE_m}{2}\,[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier, a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form

$$e_{ssb} = A \cos(\omega_c + \omega_m)t$$

and if multiplied by the appropriate carrier waveform, $\cos \omega_c t$,

$$e_{ssb}e_{carrier} = \frac{AK}{2}\,[\cos(2\omega_c + \omega_m)t + \cos(\omega_c)t].$$

If the frequency of the band-limited carrier signal, ω_c, is ascertained in advance the designer can insert a low-pass filter and obtain the (AK/2) ($\cos \omega_c t$) term with ease. He also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low-pass filter.

6.3 Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulation, when a dc term is added to the modulating signal with the Y offset adjust potentiometer. (See Figure 30.)

Here, the identity is

$$E_m(1 + m \cos \omega_m t)\,E_c \cos \omega_c t = KE_mE_c \cos \omega_c t +$$

$$\frac{KE_mE_cm}{2}\,[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where m indicates the degree of modulation. Since m is adjustable, via potentiometer P_1, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where ω_c and ω_m are the same as in the balanced-modulator example.

6.4 Linear Gain Control

To obtain linear gain control, the designer can feed to one of the two MC1595 (MC1495) inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sine wave, 1.0 volt peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage V_C is 0 to +1.0 volt. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200-kHz operating frequency, load resistors of 100 ohms were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency. (See Figure 31.)

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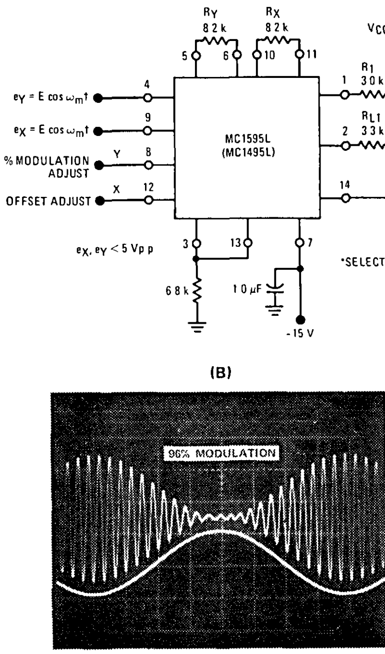
OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 30 – AMPLITUDE MODULATION



The signal is applied to the unit's Y input. Since the total input range is limited to 1.0 volt p-p, a 2.0-volt swing, a current source of 2.0 mA and an R_Y value of 1.0 kilohm is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X input varies between 0 and +1.0 volt, the current source selected was 1.0 mA and the R_X value chosen was 2.0 kilohms. This also insures linear operation over the X input dynamic range.

Choosing $R_L = 100$ assures wide-bandwidth operation. Hence, the scale factor for this configuration is

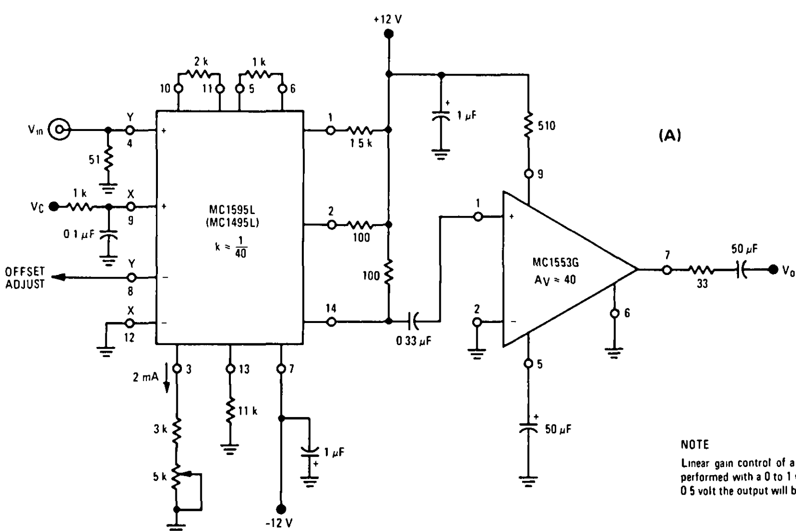
$$K = \frac{R_L}{R_X R_Y I_3} = \frac{100}{(2\,k)(1\,k)(2 \times 10^{+3})}\ V^{-1} = \frac{1}{40}\ V^{-1}.$$

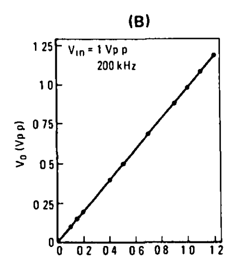
The 2 in the numerator of the equation is missing in this scale-factor expression because the output is single-ended and ac coupled.

To recover the gain, an MC1552 video amplifier with a gain of 40 is used. An operational amplifier also could have been used with frequency compensation to allow a gain of 40 at 200 kHz. The MC1539 operational amplifier can be tailored for this use; and the MC1520 operational amplifier does it directly.

6

FIGURE 31 – LINEAR GAIN CONTROL





NOTE
Linear gain control of a 1 volt peak to peak signal is performed with a 0 to 1 volt control voltage. If V_C is 0.5 volt the output will be 0.5 volt p-p.

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1496G	0°C to +70°C	Metal Can
MC1496L	0°C to +70°C	Ceramic DIP
MC1496P	0°C to +70°C	Plastic DIP
MC1596G	−55°C to +125°C	Metal Can
MC1596L	−55°C to +125°C	Ceramic DIP

MC1496
MC1596

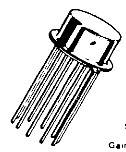
BALANCED MODULATOR – DEMODULATOR

. . . designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

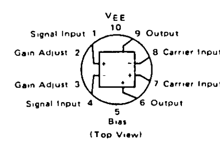
- Excellent Carrier Suppression – 65 dB typ @ 0.5 MHz
  – 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common-Mode Rejection – 85 dB typ

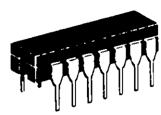
BALANCED MODULATOR – DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

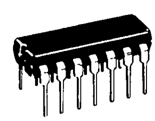


G SUFFIX
METAL PACKAGE
CASE 603

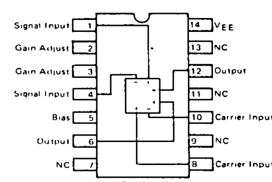




L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1496 only)



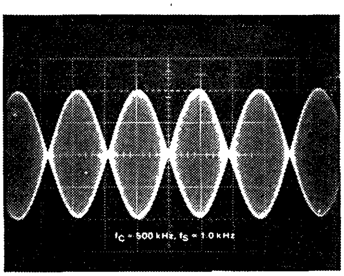


FIGURE 1 – SUPPRESSED CARRIER OUTPUT WAVEFORM

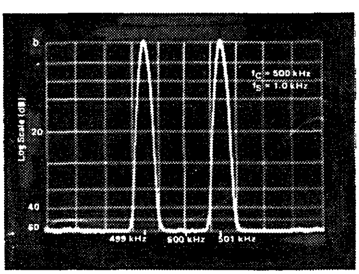


FIGURE 2 – SUPPRESSED-CARRIER SPECTRUM

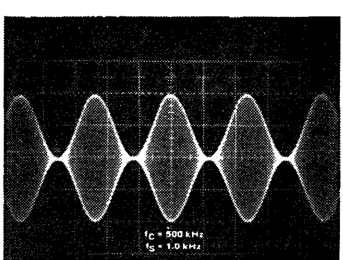
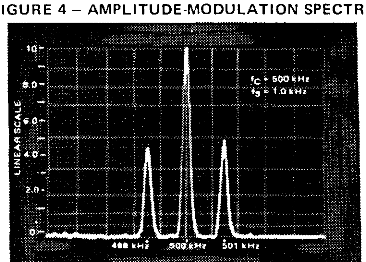


FIGURE 3 – AMPLITUDE-MODULATION OUTPUT WAVEFORM

FIGURE 4 – AMPLITUDE-MODULATION SPECTRUM



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MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage ($V_6 - V_7$, $V_8 - V_1$, $V_9 - V_7$, $V_9 - V_8$, $V_7 - V_4$, $V_7 - V_1$, $V_8 - V_4$, $V_6 - V_8$, $V_2 - V_5$, $V_3 - V_5$)	ΔV	30	Vdc
Differential Input Signal	$V_7 - V_8$ $V_4 - V_1$	+5 0 ±(5+I_5R_e)	Vdc
Maximum Bias Current	I_5	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		575	mW
Derate above T_A = +25°C		3 85	mW/°C
Metal Package		680	mW
Derate above T_A = +25°C		4 6	mW/°C
Operating Temperature Range	T_A		°C
MC1496		0 to +70	
MC1596		-55 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS* (V_{CC} = +12 Vdc, V_{EE} = -8.0 Vdc, I_5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C unless otherwise noted) (All input and output characteristics are single-ended unless otherwise noted.)

				MC1596			MC1496			
Characteristic	Fig	Note	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Carrier Feedthrough	5	1	V_{CFT}							μV(rms)
V_C = 60 mV(rms) sine wave and offset adjusted to zero, f_C = 1.0 kHz				–	40	–	–	40	–	
f_C = 10 MHz				–	140	–	–	140	–	
V_C = 300 mVp-p square wave:										mV(rms)
offset adjusted to zero, f_C = 1 0 kHz				–	0 04	0.2	–	0 04	0 4	
offset not adjusted, f_C = 1 0 kHz				–	20	100	–	20	200	
Carrier Suppression	5	2	V_{CS}							dB
f_S = 10 kHz, 300 mV(rms)										
f_C = 500 kHz, 60 mV(rms) sine wave				50	65	–	40	65	–	
f_C = 10 MHz, 60 mV(rms) sine wave				–	50	–	–	50	–	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 ohms)	8	8	BW_{3dB}							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave, f_S = 1.0 kHz, 300 mV(rms) sine wave				–	300	–	–	300	–	
Signal Input Port, V_S = 300 mV(rms) sine wave, $\|V_C\|$ = 0.5 Vdc				–	80	–	–	80	–	
Signal Gain, V_S = 100 mV(rms), f = 1.0 kHz, $\|V_C\|$ = 0 5 Vdc	10	3	A_{VS}	2 5	3 5	–	2 5	3.5	–	V/V
Single-Ended Input Impedance, Signal Port, f = 5 0 MHz	6	–								
Parallel Input Resistance			r_{ip}	–	200	–	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2 0	–	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz	6	–								
Parallel Output Resistance			r_{op}	–	40	–	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	–	5.0	–	pF
Input Bias Current $I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_7 + I_8}{2}$	7	–								μA
			I_{bS}	–	12	25	–	12	30	
			I_{bC}	–	12	25	–	12	30	
Input Offset Current $I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$	7	–								μA
			$\|I_{ioS}\|$	–	0.7	5.0	–	0.7	7 0	
			$\|I_{ioC}\|$	–	0.7	5 0	–	0 7	7 0	
Average Temperature Coefficient of Input Offset Current (T_A = -55°C to +125°C)	7	–	$\|TC_{Iio}\|$	–	2 0	–	–	2.0	–	nA/°C
Output Offset Current ($I_6 - I_9$)	7	–	$\|I_{oo}\|$	–	14	50	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = -55°C to +125°C)	7	–	$\|TC_{Ioo}\|$	–	90	–	–	90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	–	5.0	–	–	5 0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1 0 kHz, $\|V_C\|$ = 0 5 Vdc	9	–	ACM	–	-85	–	–	-85	–	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	–	V_o	–	8 0	–	–	8 0	–	Vdc
Differential Output Voltage Swing Capability	10	–	V_{out}	–	8.0	–	–	8 0	–	Vp-p
Power Supply Current	7	6								mAdc
$I_6 + I_9$			I_{CC}	–	2.0	3 0	–	2 0	4.0	
I_{10}			I_{EE}	–	3 0	4 0	–	3.0	5 0	
DC Power Dissipation	7	5	P_D	–	33	–	–	33	–	mW

* Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

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GENERAL OPERATING INFORMATION *

Note 1 — Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 5).

Note 2 — Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair — or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Note 3 and Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 — Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5

$$V_S \le I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1 volt peak.

Note 4 — Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 — Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_9 = V_6$, $I_5 = I_6 = I_9$ and ignoring base current, $P_D = 2\, I_5\, (V_6 - V_{10}) + I_5\, (V_5 - V_{10})$ where subscripts refer to pin numbers.

Note 6 — Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for R_e equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V^- - \phi}{I_5} - 500\ \Omega$$

where: R_5 is the resistor between pin 5 and ground
ϕ = 0.75 V at T_A = +25°C

The MC1596 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L$$

Note 7 — Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table,

$$30 \text{ Vdc} \ge [(V_6, V_9) - (V_7, V_8)] \ge 2 \text{ Vdc}$$

$$30 \text{ Vdc} \ge [(V_7, V_8) - (V_1, V_4)] \ge 2.7 \text{ Vdc}$$

$$30 \text{ Vdc} \ge [(V_1, V_4) - (V_5)] \ge 2.7 \text{ Vdc}$$

The foregoing conditions are based on the following approximations.

$$V_6 = V_9, \quad V_7 = V_8, \quad V_1 = V_4$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 — Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$y_{21C} = \left.\frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}}\right|_{V_o = 0}$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$y_{21S} = \left.\frac{i_o \text{ (signal)}}{v_s \text{ (signal)}}\right|_{V_c = 0.5 \text{ Vdc},\ V_o = 0}$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

Note 9 — Coupling and Bypass Capacitors C_1 and C_2

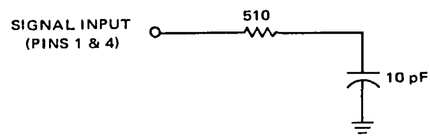
Capacitors C_1 and C_2 (Figure 5) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Note 10 — Output Signal, V_o

The output signal is taken from pins 6 and 9, either balanced or single-ended Figure 12 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Note 11 — Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the *source-tuned circuits that cause the oscillation.*



An alternate method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case *input current drift may cause serious degradation of carrier suppression*

TEST CIRCUITS

FIGURE 5 — CARRIER REJECTION AND SUPPRESSION

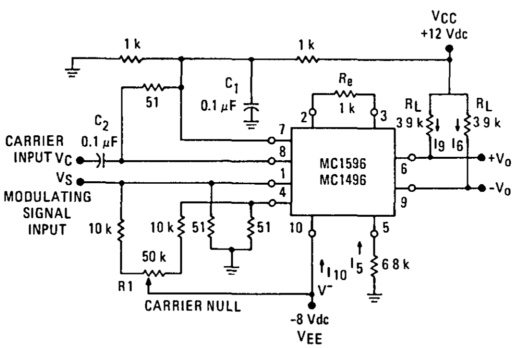


FIGURE 6 — INPUT-OUTPUT IMPEDANCE

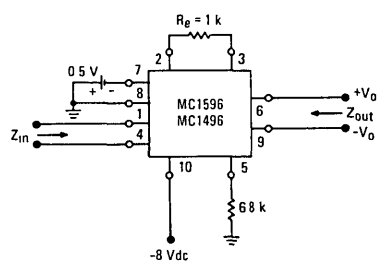


FIGURE 7 — BIAS AND OFFSET CURRENTS

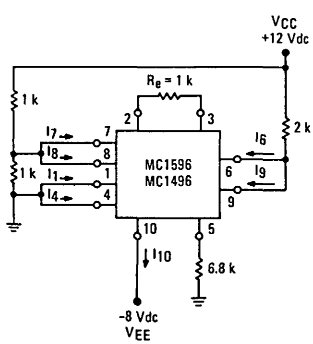
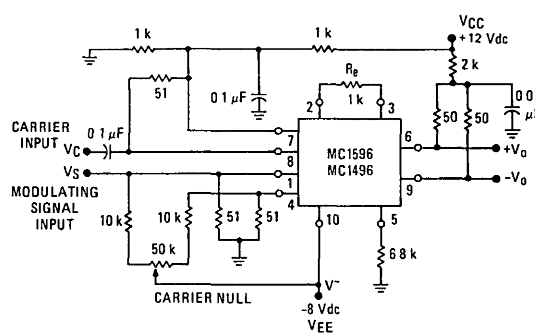


FIGURE 8 — TRANSCONDUCTANCE BANDWIDTH



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TEST CIRCUITS (continued)

FIGURE 9 – COMMON-MODE GAIN

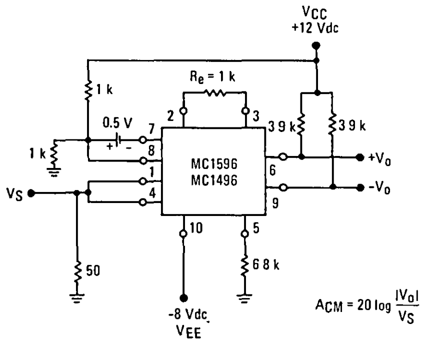
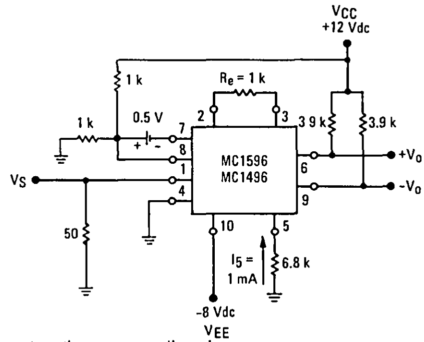


FIGURE 10 – SIGNAL GAIN AND OUTPUT SWING



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 11 – SIDEBAND OUTPUT versus CARRIER LEVELS

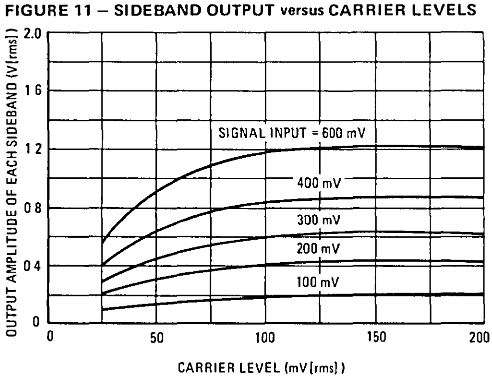


FIGURE 12 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

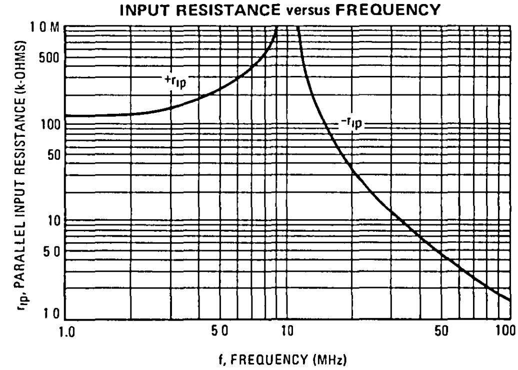


FIGURE 13 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

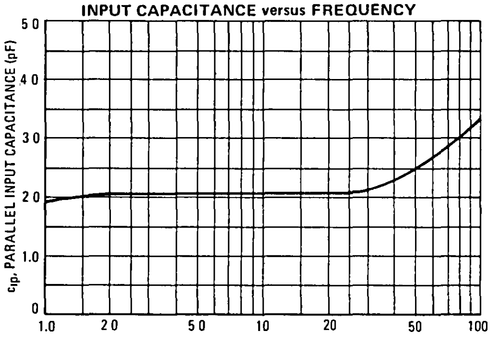
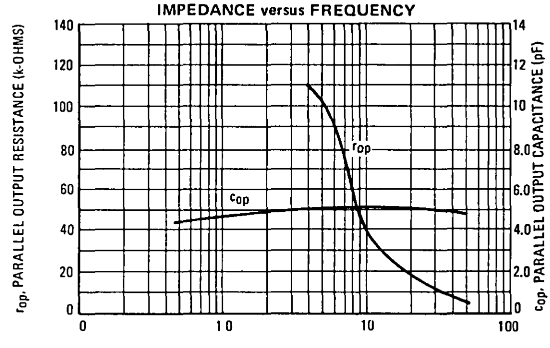


FIGURE 14 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 15 – SIDEBAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

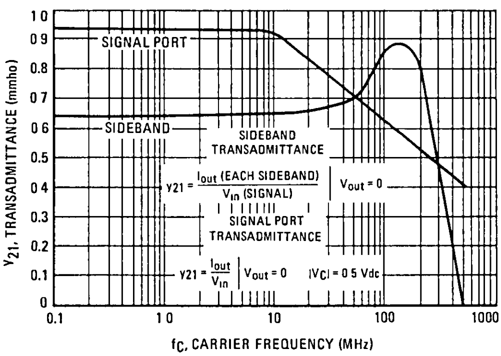


FIGURE 16 – CARRIER SUPPRESSION versus TEMPERATURE

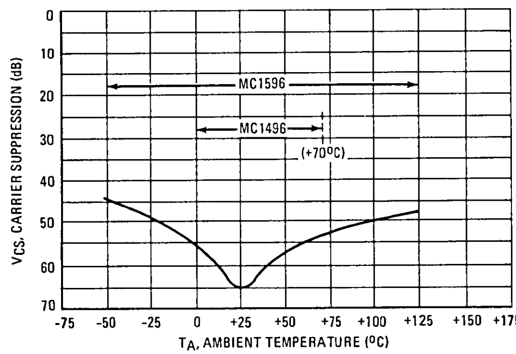


FIGURE 17 – SIGNAL-PORT FREQUENCY RESPONSE

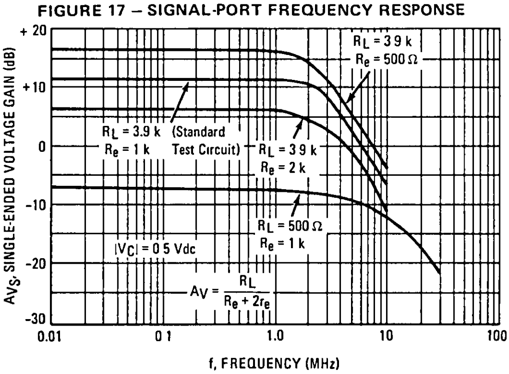


FIGURE 18 – CARRIER SUPPRESSION versus FREQUENCY

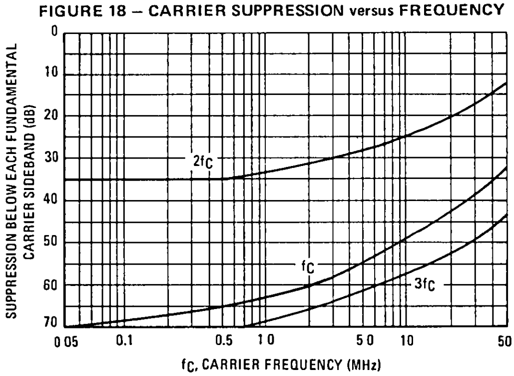


FIGURE 19 – CARRIER FEEDTHROUGH versus FREQUENCY

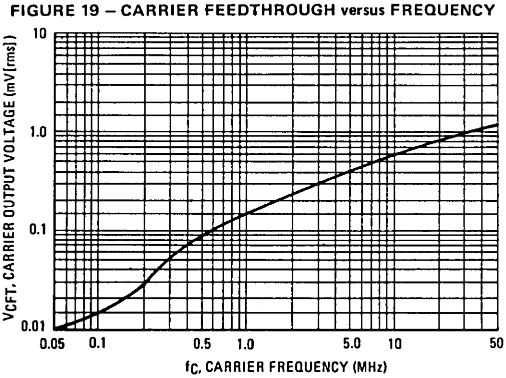
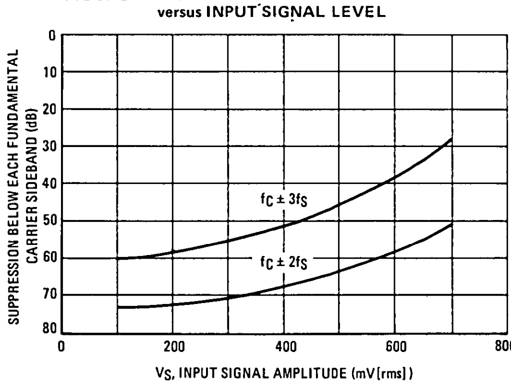


FIGURE 20 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



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TYPICAL CHARACTERISTICS (continued)

FIGURE 21 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

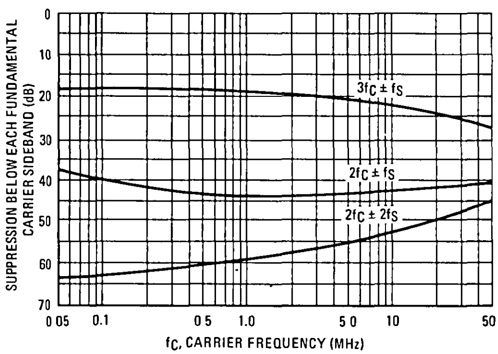
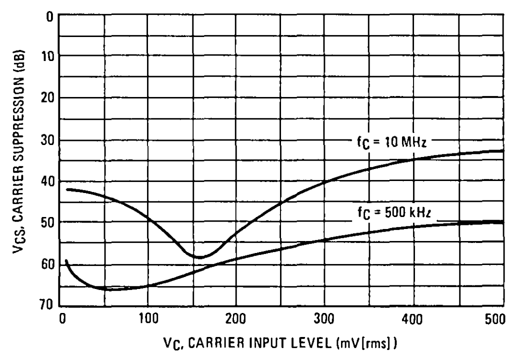


FIGURE 22 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

FIGURE 23 – CIRCUIT SCHEMATIC

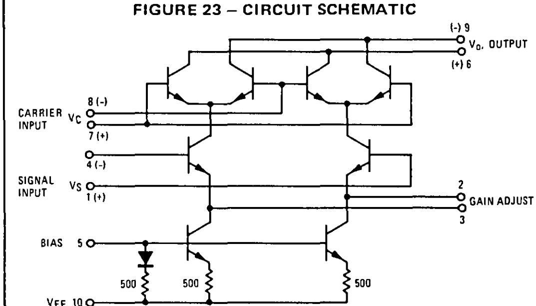
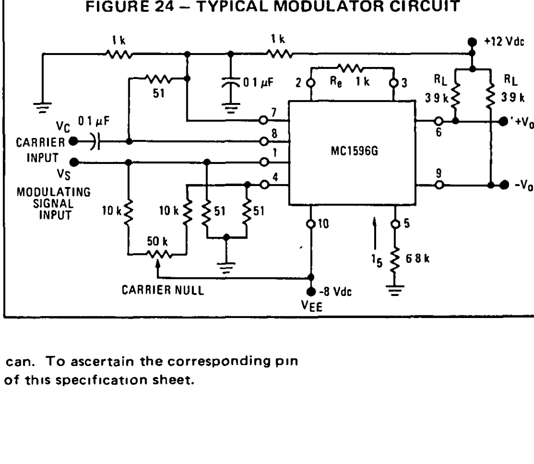


FIGURE 24 – TYPICAL MODULATOR CIRCUIT



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

OPERATIONS INFORMATION (continued)

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression

$$V = (I_5)(R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude

FIGURE 25 – TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637 R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions

1) Low-level dc
2) High-level dc
3) Low-level ac
4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal

NOTES
1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two
4. R_L = Load resistance
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at +25°C,

$$r_e \approx \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26 \text{ mV at room temperature}$$

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APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 µF capacitors on pins 7 and 8 should be increased to 1.0 µF. Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

APPLICATIONS INFORMATION (continued)

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR (+12 Vdc SINGLE SUPPLY)

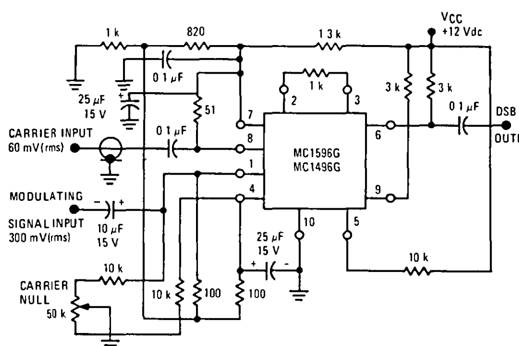


FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

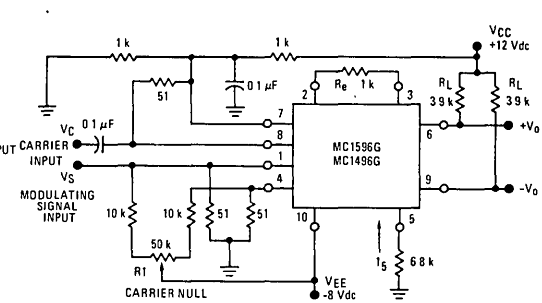


FIGURE 28 – AM MODULATOR CIRCUIT

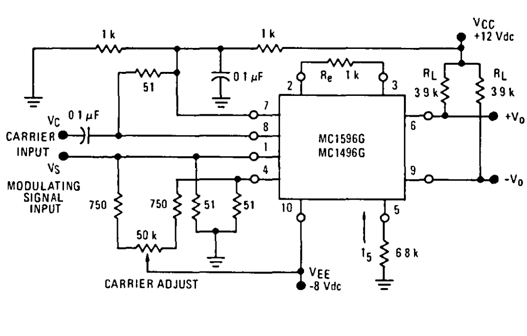
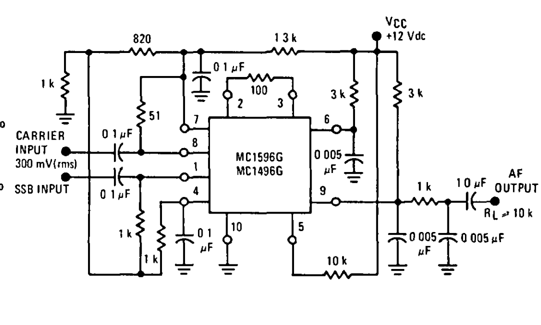
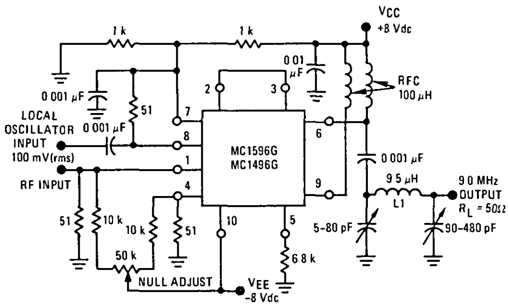


FIGURE 29 – PRODUCT DETECTOR (+12 Vdc SINGLE SUPPLY)



TYPICAL APPLICATIONS (continued)

FIGURE 30 – DOUBLY BALANCED MIXER (BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)



L1 = 44 TURNS AWG NO. 28 ENAMELED WIRE, WOUND ON MICROMETALS TYPE 44-6 TOROID CORE

FIGURE 31 – LOW-FREQUENCY DOUBLER

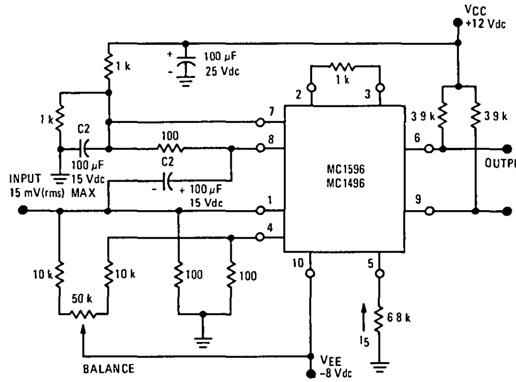
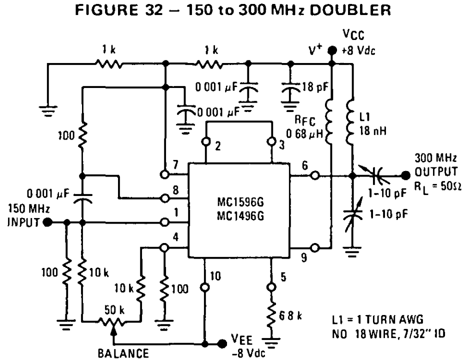
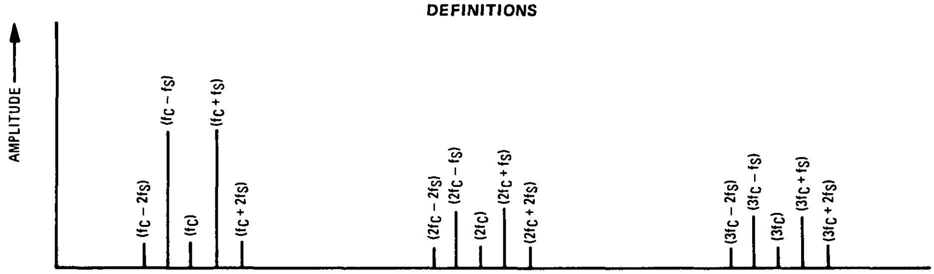


FIGURE 32 – 150 to 300 MHz DOUBLER



DEFINITIONS



FREQUENCY ——→ BALANCED MODULATOR SPECTRUM

f_C	CARRIER FUNDAMENTAL	$f_C \pm nf_S$	FUNDAMENTAL CARRIER SIDEBAND HARMONICS
f_S	MODULATING SIGNAL	nf_C	CARRIER HARMONICS
$f_C \pm f_S$	FUNDAMENTAL CARRIER SIDEBANDS	$nf_C \pm nf_S$	CARRIER HARMONIC SIDEBANDS

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1733G	−55°C to +125°C	Metal Can
MC1733L	−55°C to +125°C	Ceramic DIP
MC1733CG	0°C to +70°C	Metal Can
MC1733CL	0°C to +70°C	Ceramic DIP
MC1733CP	0°C to +70°C	Plastic DIP

MC1733
MC1733C

DIFFERENTIAL VIDEO AMPLIFIER

. . . a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

- Bandwidth — 120 MHz typical @ A_{vd} = 10
- Rise Time — 2.5 ns typical @ A_{vd} = 10
- Propagation Delay Time — 3.6 ns typical @ A_{vd} = 10

FIGURE 1 — BASIC CIRCUIT

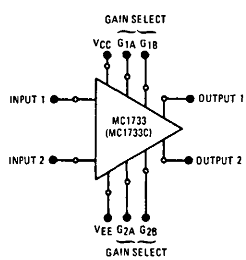


FIGURE 2 — VOLTAGE GAIN ADJUST CIRCUIT

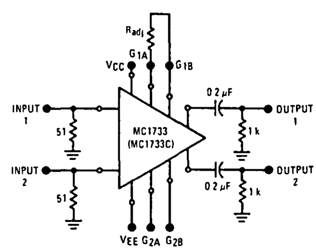
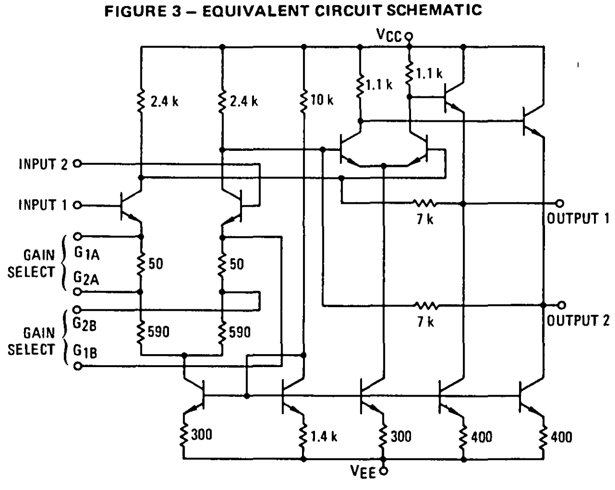


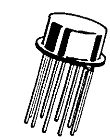
FIGURE 3 — EQUIVALENT CIRCUIT SCHEMATIC

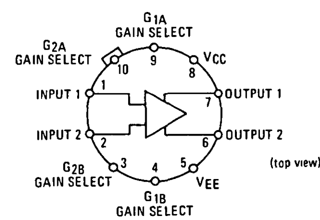


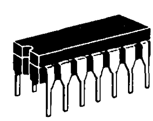
DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 603
TO-100

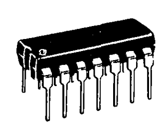


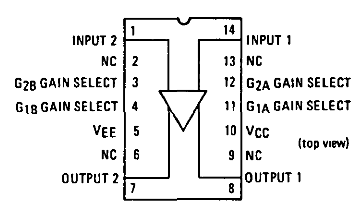




L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646





MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 -8.0	Volts
Differential Input Voltage	V_{in}	±5.0	Volts
Common-Mode Input Voltage	V_{ICM}	±6.0	Volts
Output Current	I_O	10	mA
Internal Power Dissipation (Note 1) Metal Can Package Ceramic Dual In-Line Package	P_D	 500 500	mW
Operating Temperature Range MC1733C MC1733	T_A	0 to +70 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, at T_A = +25°C unless otherwise noted.)

		MC1733			MC1733C			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Differential Voltage Gain Gain 1 (Note 2) Gain 2 (Note 3) Gain 3 (Note 4)	A_{vd}	 300 90 9.0	 400 100 10	 500 110 11	 250 80 8.0	 400 100 10	 600 120 12	V/V
Bandwidth (R_s = 50 Ω) Gain 1 Gain 2 Gain 3	BW	 – – –	 40 90 120	 – – –	 – – –	 40 90 120	 – – –	MHz
Rise Time (R_s = 50 Ω, V_O = 1 Vp-p) Gain 1 Gain 2 Gain 3	t_{TLH} t_{THL}	 – – –	 10.5 4.5 2.5	 – 10 –	 – – –	 10.5 4 5 2.5	 – 12 –	ns
Propagation Delay (R_s = 50 Ω, V_O = 1 Vp-p) Gain 1 Gain 2 Gain 3	t_{PLH} t_{PHL}	 – – –	 7.5 6.0 3.6	 – 10 –	 – – –	 7.5 6.0 3.6	 – 10 –	ns
Input Resistance Gain 1 Gain 2 Gain 3	R_{in}	 – 20 –	 4.0 30 250	 – – –	 – 10 –	 4 0 30 250	 – – –	kΩ
Input Capacitance (Gain 2)	C_{in}	–	2.0	–	–	2.0	–	pF
Input Offset Current (Gain 3)	$\|I_{IO}\|$	–	0.4	3.0	–	0.4	5.0	µA
Input Bias Current (Gain 3)	I_{IB}	–	9.0	20	–	9.0	30	µA
Input Noise Voltage (R_s = 50 Ω, BW = 1 kHz to 10 MHz)	V_n	–	12	–	–	12	–	µV(rms)
Input Voltage Range (Gain 2)	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio Gain 2 (V_{CM} = ±1 V, f ≤ 100 kHz) Gain 2 (V_{CM} = ±1 V, f = 5 MHz)	CMRR	 60 –	 86 60	 – –	 60 –	 86 60	 – –	dB
Supply Voltage Rejection Ratio Gain 2 (ΔV_s = ±0.5 V)	PSRR	 50	 70	 –	 50	 70	 –	dB
Output Offset Voltage Gain 1 Gain 2 and Gain 3	V_{OO}	 – –	 0.6 0.35	 1.5 1.0	 – –	 0.6 0.35	 1.5 1.5	V
Output Common-Mode Voltage (Gain3)	V_{CMO}	2.4	2.9	3.4	2.4	2 9	3.4	V
Output Voltage Swing (Gain 2)	V_O	3.0	4.0	–	3.0	4.0	–	Vp-p
Output Sink Current (Gain 2)	I_O	2.5	3.6	–	2.5	3.6	–	mA
Output Resistance	R_{out}	–	20	–	–	20	–	Ω
Power Supply Current (Gain 2)	I_D	–	18	24	–	18	24	mA

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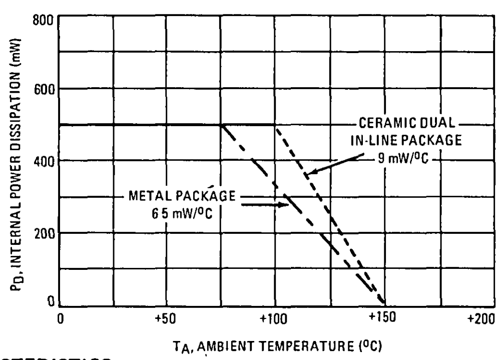
ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, at T_A = T_{high} to T_{low} unless otherwise noted.)*

Characteristic	Symbol	MC1733			MC1733C			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain	A_{vd}							V/V
Gain 1 (Note 2)		200	–	600	250	–	600	
Gain 2 (Note 3)		80	–	120	80	–	120	
Gain 3 (Note 4)		8.0	–	12	8.0	–	12	
Input Resistance Gain 2	R_{in}	8.0	–	–	8.0	–	–	kΩ
Input Offset Current (Gain 3)	$\|I_{IO}\|$	–	–	5.0	–	–	6.0	μA
Input Bias Current (Gain 3)	I_{IB}	–	–	40	–	–	40	μA
Input Voltage Range (Gain 2)	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio Gain 2 (V_{CM} = ±1 V, f ≤ 100 kHz)	CMRR	50	–	–	50	–	–	dB
Supply Voltage Rejection Ratio Gain 2 (ΔV_s = ±0.5 V)	PSRR	50	–	–	50	–	–	dB
Output Offset Voltage	V_{OO}							V
Gain 1		–	–	1.5	–	–	1.5	
Gain 2 and Gain 3		–	–	1.2	–	–	1.5	
Output Voltage Swing (Gain 2)	V_O	2.5	–	–	2.5	–	–	Vp-p
Output Sink Current (Gain 2)	I_O	2.2	–	–	2.5	–	–	mA
Power Supply Current (Gain 2)	I_D	–	–	27	–	–	27	mA

*T_{low} = 0°C for MC1733C, -55°C for MC1733
T_{high} = +70°C for MC1733C, +125°C for MC1733.

FIGURE 4 – MAXIMUM ALLOWABLE POWER DISSIPATION



NOTES

Note 1: Derate metal package at 6 5 mW/°C for operation at ambient temperatures above 75°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required (MC1733) a heatsink may be necessary to limit maximum junction temperature to 150°C. Thermal resistance, junction-to-case, for the metal package is 69.4°C per Watt.

Note 2: Gain Select pins G_{1A} and G_{1B} connected together.

Note 3: Gain Select pins G_{2A} and G_{2B} connected together.

Note 4: All Gain Select pins open.

TYPICAL CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

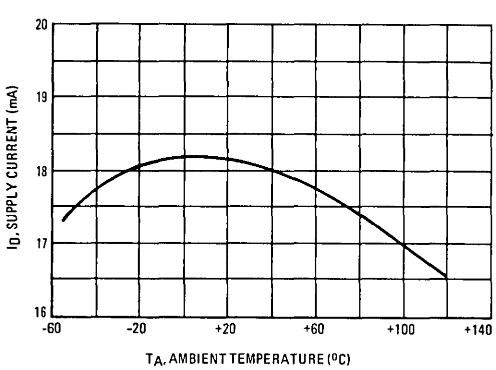
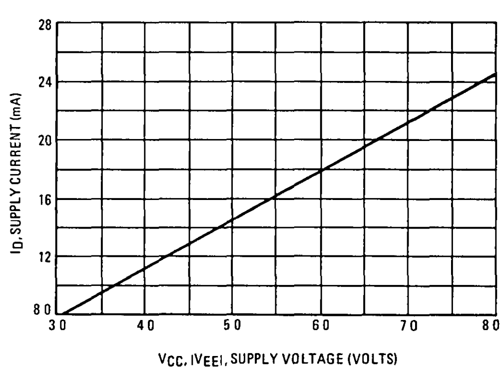


FIGURE 6 – SUPPLY CURRENT versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)
(V_{CC} = +6.0 Vdc, V_{EE} = −6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 7 – GAIN verus TEMPERATURE

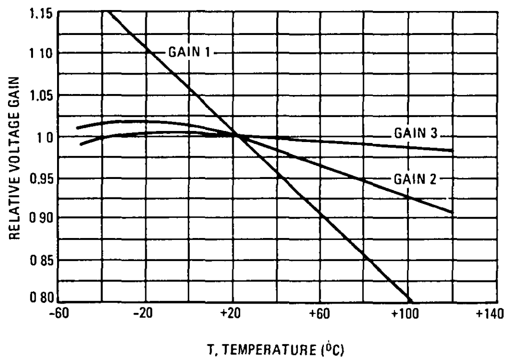


FIGURE 8 – GAIN versus FREQUENCY

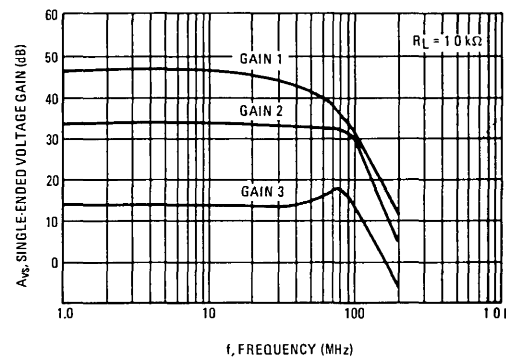


FIGURE 9 – GAIN versus SUPPLY VOLTAGE

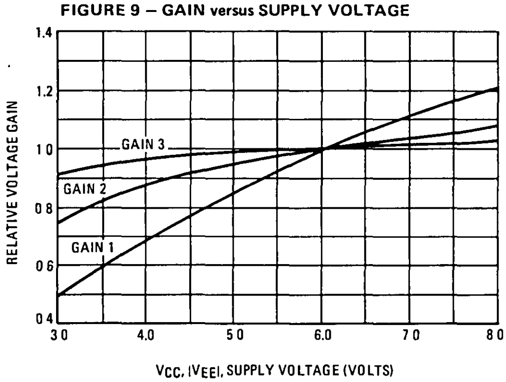


FIGURE 10 – GAIN versus R_{ADJUST}

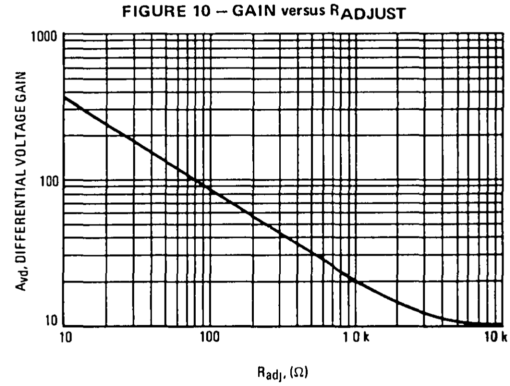


FIGURE 11 – GAIN versus FREQUENCY and SUPPLY VOLTAGE

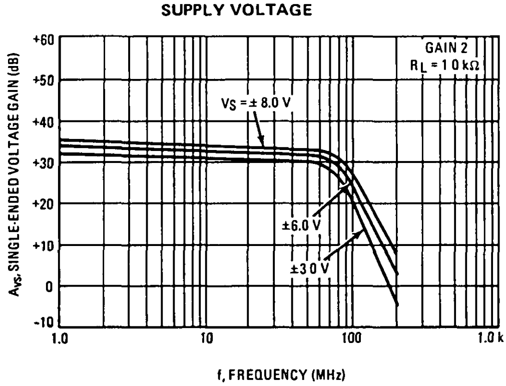
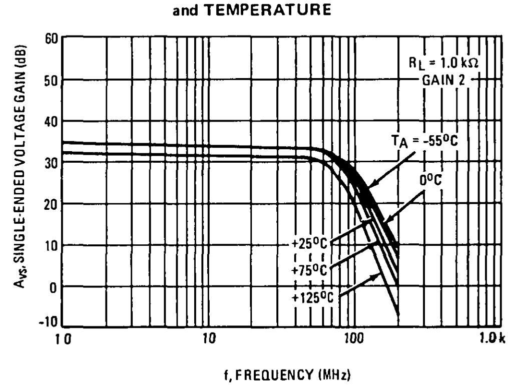


FIGURE 12 – GAIN versus FREQUENCY and TEMPERATURE



6

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 13 – PULSE RESPONSE versus GAIN

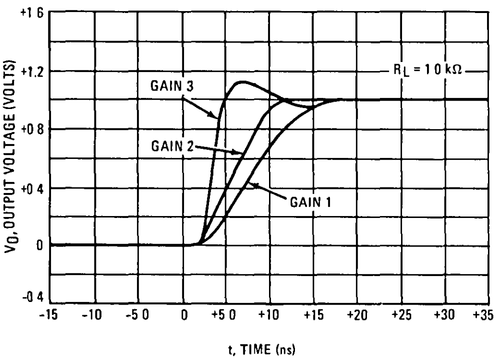


FIGURE 14 – PULSE RESPONSE versus SUPPLY VOLTAGE

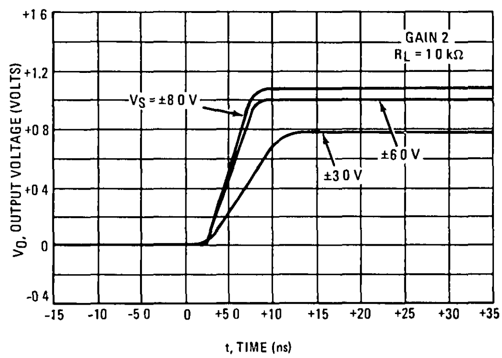


FIGURE 15 – PULSE RESPONSE versus TEMPERATURE

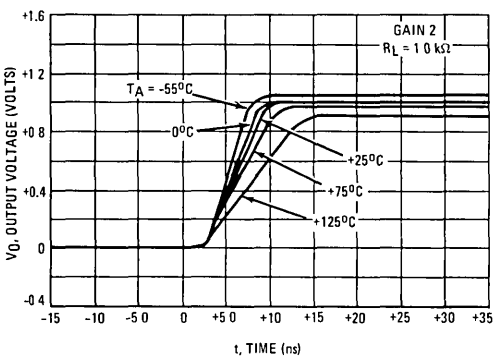


FIGURE 16 – DIFFERENTIAL OVERDRIVE RECOVERY TIME

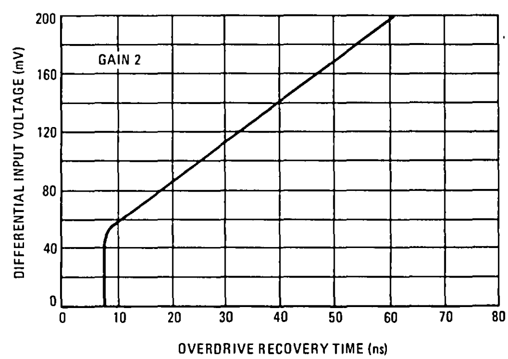


FIGURE 17 – PHASE SHIFT versus FREQUENCY

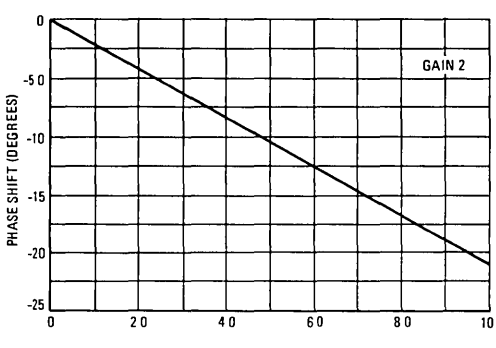
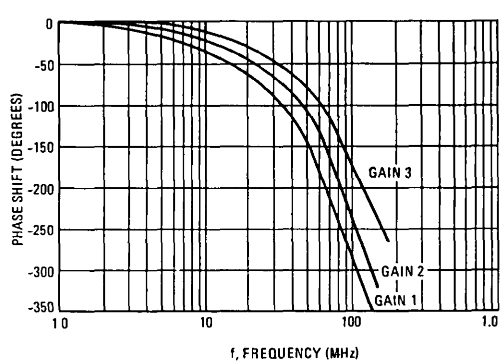


FIGURE 18 – PHASE SHIFT versus FREQUENCY



TYPICAL CHARACTERISTICS (Continued)

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 19 – INPUT RESISTANCE versus TEMPERATURE

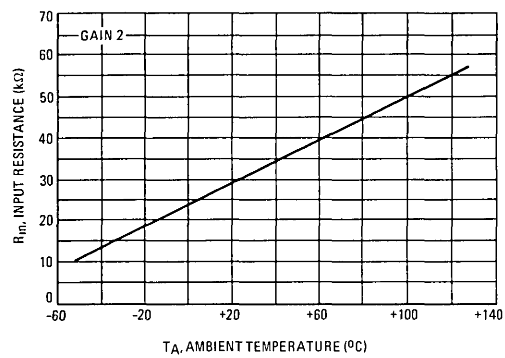


FIGURE 20 – INPUT NOISE VOLTAGE

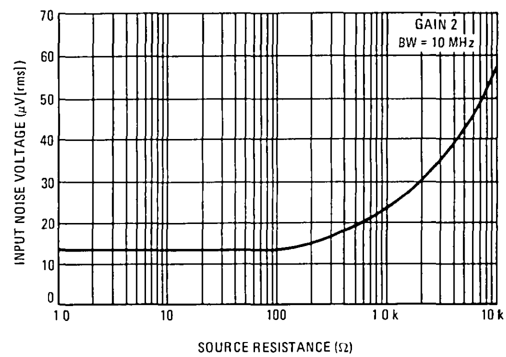


FIGURE 21 – OUTPUT VOLTAGE SWING and SINK CURRENT versus SUPPLY VOLTAGE

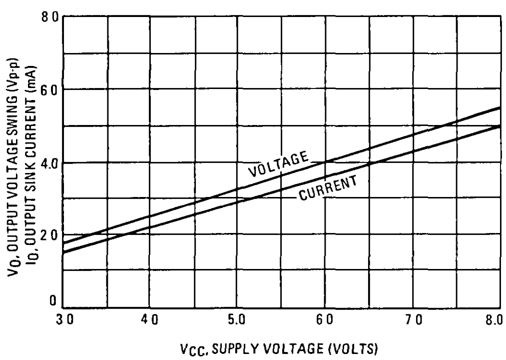


FIGURE 22 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

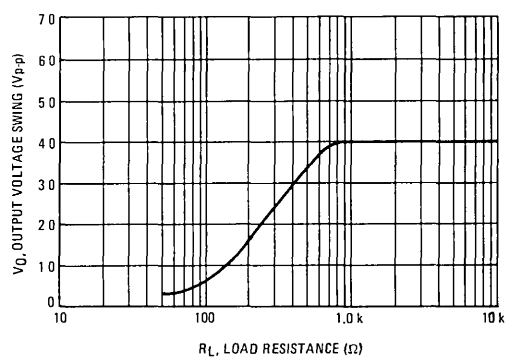


FIGURE 23 – OUTPUT VOLTAGE SWING versus FREQUENCY

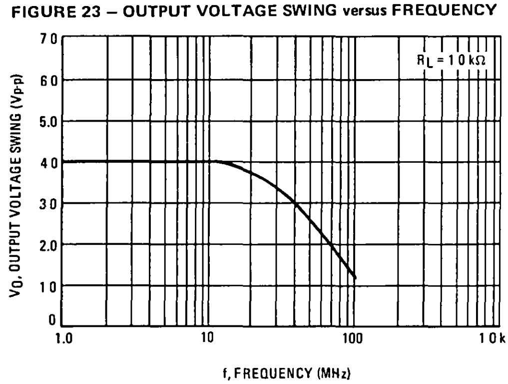
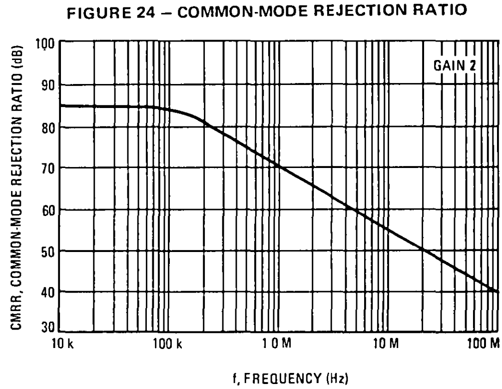
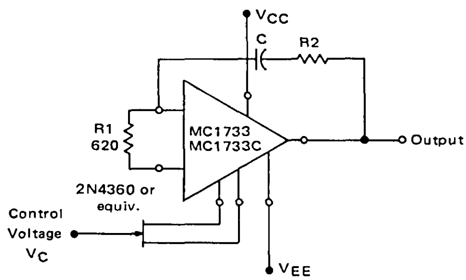


FIGURE 24 – COMMON-MODE REJECTION RATIO



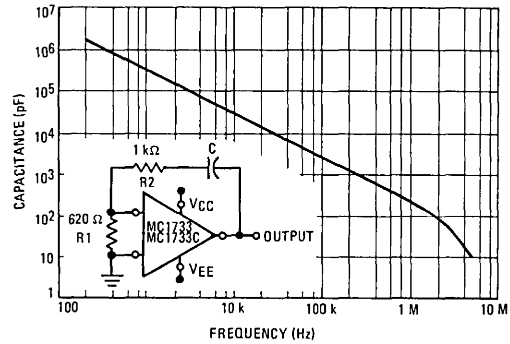
APPLICATIONS INFORMATION

FIGURE 25 – VOLTAGE CONTROLLED OSCILLATOR



By changing the voltage V_C the gain will vary over a range of 10 to 400. This will give a frequency variation about the value set by the capacitor and shown in Figure 26.

FIGURE 26 – OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



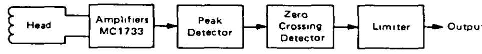
TAPE, DRUM OR DISC MEMORY READ AMPLIFIERS

The first of several methods to be discussed is shown in Figure 27. This block diagram describes a simple Read circuit with no threshold circuitry. Each block represents a basic function that must be performed by the Read circuit. The first block, referred to as "amplfiication", increases the level of the signal available from the Read head to a level adequate to drive the peak detector. Obviously, these signal levels will vary depending on factors such as tape speed, whether the system used is disc or tape, and the type of head and the circuitry used. For a representative tape system, levels of 7 to 25 mV for the signal from the Read head and 2 V for the signal to the peak detector are typical. These signal levels are "peak-to-peak" unless otherwise specified. On the basis of the signal levels mentioned above, the overall amplification required is 38 to 49 dB.

How the overall gain requirement is implemented will depend somewhat on the system used. For instance, a tape cassette system with variable tape speed may utilize a first stage for gain and a second stage primarily for gain control. Thus, a typical circuit would utilize 35 dB in the first stage and 10 to 15 dB in the second stage.

Devices suitable for use as amplifiers fall into one of two categories, operational amplifiers or wideband video amplifiers. Lower speed equipment with low transfer rates commonly uses low cost operational amplifiers. Examples of these are the MC1741, MC1458, MC1709, and MLM301. Equipment requiring higher transfer rates, such as disc systems normally use wideband amplifiers such as the MC1733. The actual cross-over point where wideband amplifiers are used exclusively varies with equipment design. For purposes of comparison, the MLM301 has slightly less than a 40 dB open-loop gain at 100 kHz; the MC1741, a compensated op-amp, has approximately 20 dB open loop gain at 100 kHz; the MC1733 has approximately 33 dB of gain out to 100 MHz (depending on gain option and loading).

FIGURE 27 – TYPICAL READ CIRCUIT (METHOD 1)



There are a number of ways to implement the peak detector function. However, the simplest and most widely used method is a passive differentiator that generates "zero-crossings" for each of the data peaks in the Read signal.

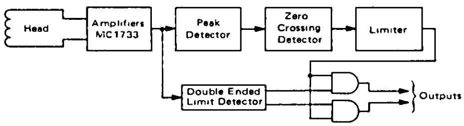
The actual circuitry used to differentiate the Read signal varies from a differential LC type in disc systems to a simple RC type in reel and cassette systems. Either type, of course, attenuates the signal by an amount depending on the circuit used and system specifications. A good approximation of attenuation using the RC type is 20 dB. Thus, the 2 V signal going into the differentiator is reduced to 200 mV.

The next block in Figure 27 to be discussed is the zero-crossing detector. In most cases detection of the zero-crossings is combined with the limiter. These functions serve to generate a TTL compatible pulse waveform with "edges" corresponding to zero-crossings. For low transfer rates, the circuit often used consists of an operational amplifier with series or shunt limiting. For higher transfer rates (greater than 100K B/S) comparators are used.

The method described above is often modified to include threshold sensing. In Figure 28, the function called "double-ended, limit-detector" enables the output NAND gate when either the negative or positive data peaks of the Read signal exceed a predetermined threshold. This function can be implemented in either of two ways. One method first rectifies the signal before it is applied to a comparator with a set threshold. The other method utilizes two comparators, one comparator for positive-going peaks and the other for negative-going peaks. These comparator outputs are then combined in the output logic gates.

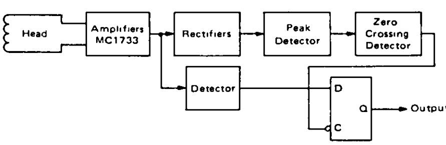
APPLICATIONS INFORMATION (continued)

FIGURE 28 — READ CIRCUIT (METHOD 2)



Another common technique is shown in Figure 29. The branch labeled rectifiers, peak detector, etc., provides a clock transition of the D flip-flop that corresponds to the peak of both the positive and negative-going data peaks. This branch may include threshold circuitry prior to the peak detector. The detector in the lower path detects whether the signal peaks are positive or negative and feeds this data to the flip-flop. This detector can be implemented using a comparator with pre-set threshold.

FIGURE 29 — READ CIRCUIT (METHOD 3)

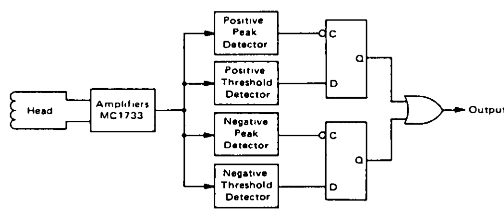


The technique shown in Figure 30 uses separate circuits with threshold provisions for both negative and positive peaks. The peak detectors and threshold detectors may be implemented with two comparators and two passive differentiators.

Each of the methods shown offer certain intrinsic advantages or disadvantages. The overall decision as to which method to use however often involves other important considerations. These could include cost and system requirements or circuitry other than simply the Read circuitry. For instance, if cost is the predominate overall factor, then approach one may be the only feasible alternative.

Method four was included as a design example because it illustrates several unique advantages. First, it uses threshold sensing to reduce noise peak errors. Second, it may be implemented using only integrated circuits. Third, it offers separate, direct threshold sensing for both positive and negative peaks.

FIGURE 30 — READ CIRCUIT (Method 4)



6

ORDERING INFORMATION

Device	Temperature Range	Package
MC3344L	−40°C to +85°C	Ceramic DIP
MC3344P	−40°C to +85°C	Plastic DIP

MC3344

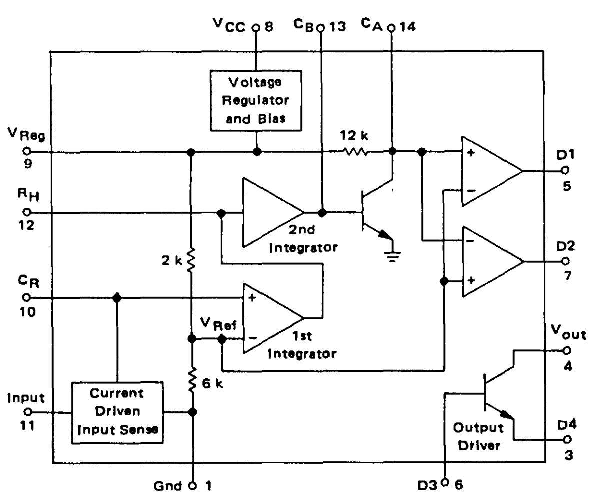
Advance Information

PROGRAMMABLE FREQUENCY SWITCH WITH ADJUSTABLE HYSTERESIS

The MC3344 is a general purpose programmable frequency switch designed for use in systems where a load must be switched on or off at a predetermined frequency. Switch frequency is determined by an external resistor (R_R) and capacitor (C_R). Hysteresis is adjustable and determined by an external resistor (R_H).

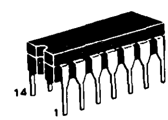
- Isolated Driver Transistor
- Complementary Outputs
- Adjustable Hysteresis
- Wide Supply Operating Range (7 to 24 Volts)
- Wide Input Frequency Range (10 Hz to 100 kHz)
- Internal Regulator
- Ideal for Automotive and Industrial Applications

FIGURE 1 — CIRCUIT BLOCK DIAGRAM



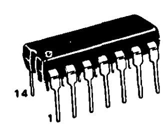
PROGRAMMABLE FREQUENCY SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

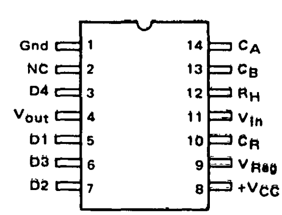


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO - 116

P SUFFIX
PLASTIC PACKAGE
CASE 646



PIN CONNECTIONS



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	24	Vdc
Peak Input Current	I_I	10	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +15 Vdc unless otherwise specified)

Characteristic	Test Ckts	Symbol	Min	Typ	Max	Unit
Supply Current	2	I_D	–	2.5	4.0	mA
Trigger Reset Voltage	3					Vdc
I_{in} = 200 μA		V_{CR1}	0.25	–	–	
I_{in} = 600 μA		V_{CR2}	–	–	0.25	
Regulator Output Voltage	4	V_{Reg}	4.0	4.5	5.0	Vdc
Threshold Output Voltage $V_{TCR} = V_{CR}/V_{Reg}$	5	V_{TCR}	0.739	0.750	0.761	V/V
Hysteresis Sink Current	6	I_H	100	400	–	μA
Second Comparator Output	7					
D1 Leakage		I_{D1L}	–	–	100	nA
D2 Source		I_{D2S}	100	250	–	μA
D1 Source		I_{D1S}	100	200	–	μA
D2 Leakage		I_{D2L}	–	–	100	nA
Output Driver Gain I_C = 5.0 mA	8	h_{FE1}	50	100	–	–
Output Driver Voltage Standoff I_D = 5.0 mA	9	BV_{CEO}	25	30	–	Vdc
Integrator Transistor Gain $h_{FE2} = \Delta I_C/\Delta I_B$, I_{C1} = 0.4 mA, I_{C2} = 0.6 mA	10	h_{FE2}	50	200	300	–

6

TEST CIRCUITS

FIGURE 2 – SUPPLY CURRENT

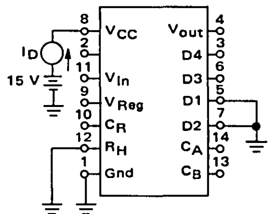
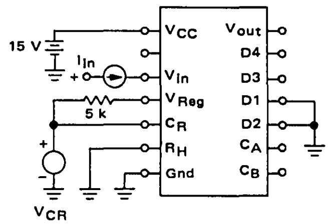


FIGURE 3 – TRIGGER RESET VOLTAGE



I_{in} = 200 µA, $V_{CR} \geq 0.25$ V
I_{in} = 600 µA, $V_{CR} \leq 0.25$ V

FIGURE 4 – REGULATOR OUTPUT VOLTAGE

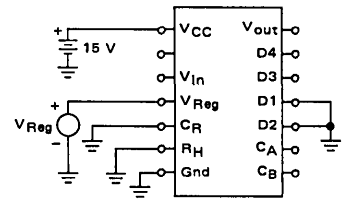
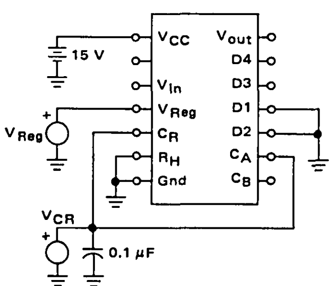


FIGURE 5 – THRESHOLD VOLTAGE RATIO



$V_{TCR} = V_{CR}/V_{Reg}$

FIGURE 6 – HYSTERESIS SINK CURRENT

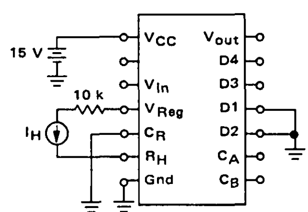
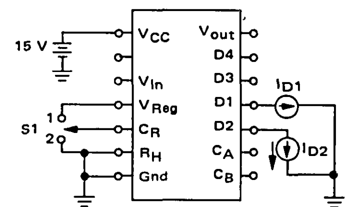


FIGURE 7 – I_{D1L}/I_{D2S}, I_{D2L}/I_{D1S}



I_{D1L}/I_{D2S} – S1 in position 1
I_{D2L}/I_{D1S} – S1 in position 2

FIGURE 8 – OUTPUT DRIVER GAIN

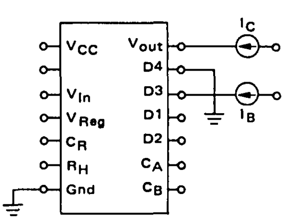


FIGURE 9 – BV_{CEO} OF OUTPUT TRANSISTOR

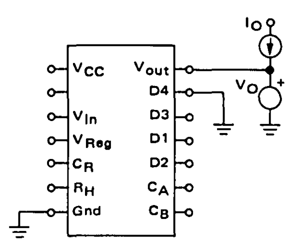
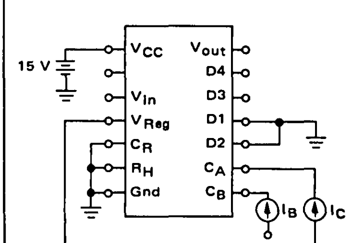


FIGURE 10 – INTEGRATOR TRANSISTOR GAIN



APPLICATIONS INFORMATION

The voltage regulator and bias section provides the proper biasing and regulated supply voltage to the integrated circuit.

A square wave, when applied to the RC differentiator, provides input current pulses to the IC. The input circuit discharges and clamps, for a predetermined time, the voltage across capacitor C_R. This establishes the initial ramp voltage (V_{sat}) and allows initiation of a new voltage ramp after each positive transistion of the input waveform.

The voltage, V_{CR}, ramps from V_{sat} to the final value, V_{Reg}, charging through R_R.

If V_{CR} is never allowed to reach V_{Ref} due to quick reset pulses, the second integrator amplifier will not be activated, and capacitor C_{AB} is allowed to charge through the 12 kΩ resistor until V_{CA} is greater than V_{Ref}. At this point, D1 will switch ON and D2 will switch OFF. By connecting either D1 or D2 to the D3 drive pin, the output drive transistor may be either switched ON or OFF at the switch point.

If V_{CR} is allowed to ramp above V_{Ref} before being reset, the second integrator amplifier is driven ON which discharges and resets capacitor C_{AB} keeping V_{CA} low with respect to V_{Ref}.

V_{CA} will always be low with respect to V_{Ref} if the time from reset C_R to $V_{CR} = V_{Ref}$ is less than the time from reset C_{AB} to $V_{CA} = V_{Ref}$.

Resistor R_H provides hysteresis around the switch point (i.e., frequency to switch the output driver ON, when connected to the D1 terminal, is higher than the frequency required to switch the output driver OFF). If no hysteresis is desired then the R_H resistor should be omitted and pin 12 grounded.

Circuit Equations:

The first integrator time constant is $T1 = R_H \parallel R_R\ C_R$. If R_H is omitted then $T1 = R_R\ C_R$.

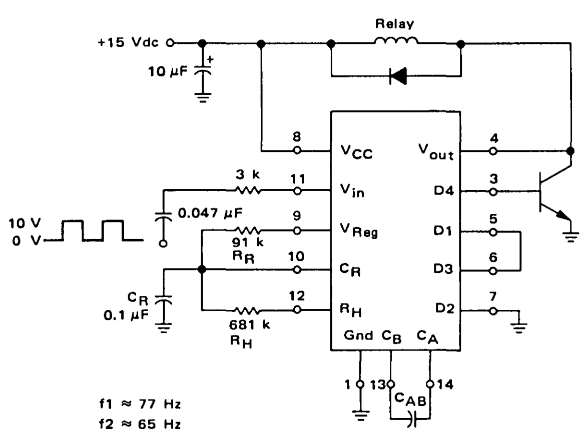
The second integrator time constant is $T2 = (12\ k)\ (h_{FE2})\ (C_{AB})$.

$$f1 = \text{Switch Point frequency} \cong \frac{1}{1.39\ R_R\ C_R}$$

$f2$ = Hysteresis Switch Point frequency ≈

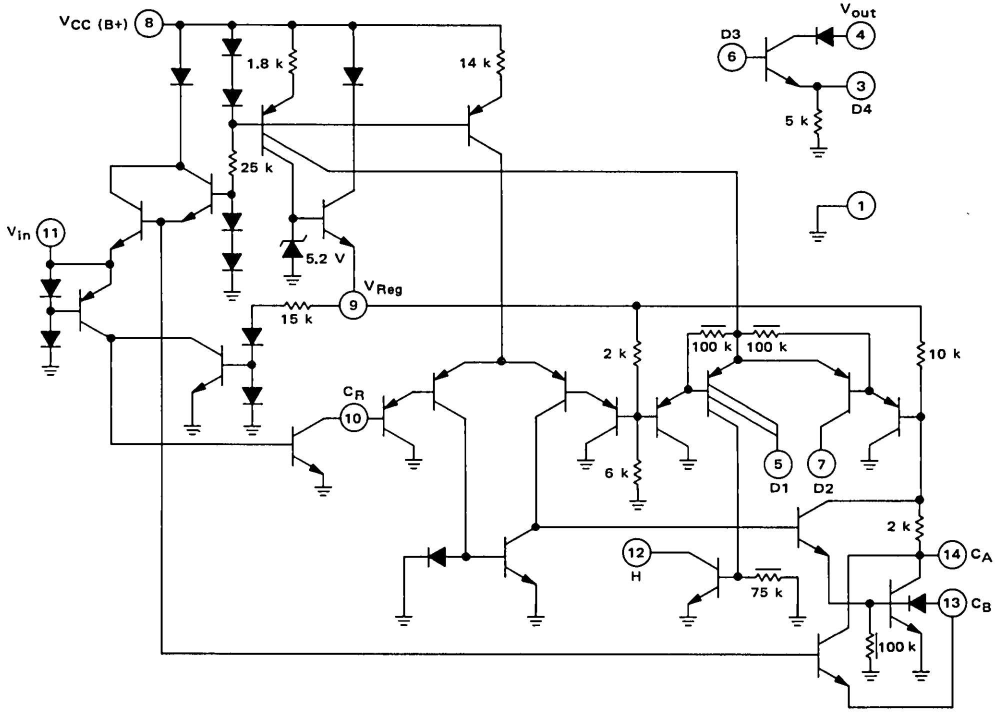
$$\frac{1}{R_R \parallel R_H\ C_R \ln\left[\frac{R_H}{0.25\ R_H - 0.75\ R_R}\right]}$$

FIGURE 11 — TYPICAL APPLICATION



6

FIGURE 12 — CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC3370P	−10°C to +75°C	Plastic DIP

MC3370P

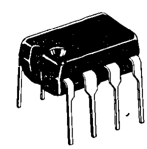
ZERO VOLTAGE SWITCH

. . designed for use in ac power switching applications with output drive capable of triggering triacs. Other operational features include; (1) a built-in voltage regulator that allows direct ac line operation, (2) a differential input with dual sensor inputs capable of testing the condition of two external sensors and controlling the gate pulse to a triac accordingly, (hysteresis or proportional control to this section may be added if desired) (3) sensor input "open and short" protection, this insures that the triac will never be turned "on" if either of the inputs are shorted or opened (4) a zero crossing detector that synchronizes the triac gate pulses with the zero crossing of the ac line voltage. This eliminates radio frequency interference (RFI) when used with resistive loads.

- Heater Controls
- Photo Controls
- Threshold Detector
- Lamp Driver
- Valve Control
- On-Off Power Controls
- Relay Driver
- Flasher Control
- Formerly MFC8070 in Case 644A Package

ZERO VOLTAGE SWITCH

SILICON MONOLITHIC
FUNCTIONAL CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626

FIGURE 1 – CIRCUIT SCHEMATIC

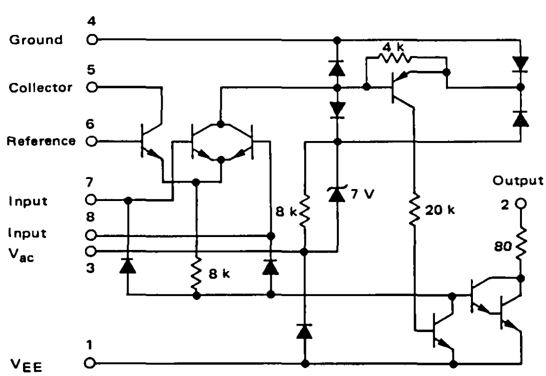
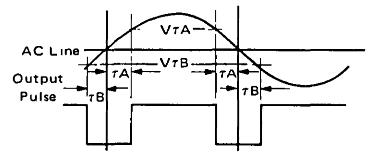


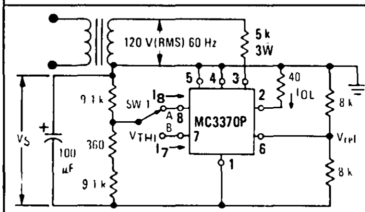
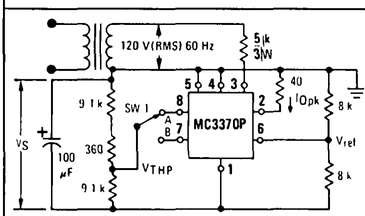
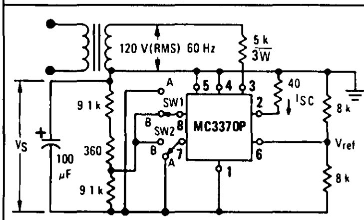
FIGURE 2 – OUTPUT PULSE DEFINITION



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
DC Voltage	$V_{4\text{-}1}$	15	Vdc
DC Voltage	$V_{5\text{-}1}$	15	Vdc
DC Voltage	$V_{2\text{-}1}$	15	Vdc
Peak Supply Current	I_3	35	mA
Power Dissipation Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1.2 10	Watts mW/°C
Operating Ambient Temperature Range	T_A	-10 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	V_S with Inhibit Output (Sw 1 A or B)	V_{SIO}	–	9.0	11	Vdc
	Output Leakage Current (Sw 1 A or B)	I_{OL}	–	5.0	100	µA
	Input Current 8 (Sw 1 A)	I_8	–	5.0	15	µA
	Input Current 7 (Sw 1 B)	I_7	–	5.0	15	µA
	Inhibit Threshold Voltage (Sw 1 A or B)	V_{THI}	V_{ref} +100 mV	V_{ref} +10 mV	–	Vdc
	V_S with Pulse Output (Sw 1 A or B)	V_{SPO}	6.0	8.5	–	Vdc
	Peak Output Current (Sw 1 A or B)	$I_{O\,pk}$	50	80	–	mA
	Pulse Threshold Voltage (Sw 1 A or B)	V_{THP}	–	V_{ref} -10 mV	V_{ref} -100 mV	Vdc
	Output Pulse Width (Sw 1. A or B, See Figure 2)	τA, τB VτA, VτB	–	70 ±4.5	– –	µs V
	Output Current With Input Short (Sw 1: B; Sw 2: A) (Sw 1: A; Sw 2. B)	I_{SC}	 – –	 5.0 5.0	 100 100	µA

TEST CIRCUIT AND TYPICAL CHARACTERISTICS

FIGURE 3 – CIRCUIT WITH INCREASED PULSE WIDTH AND TRIAC DRIVER TO CONTROL HIGH-CURRENT SCR's

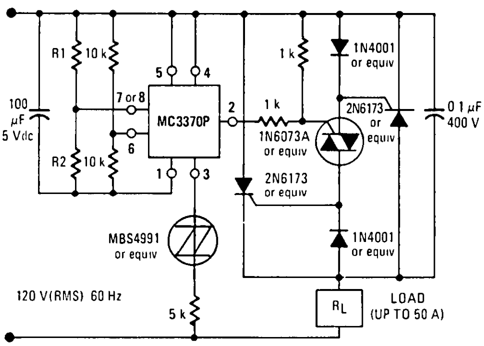
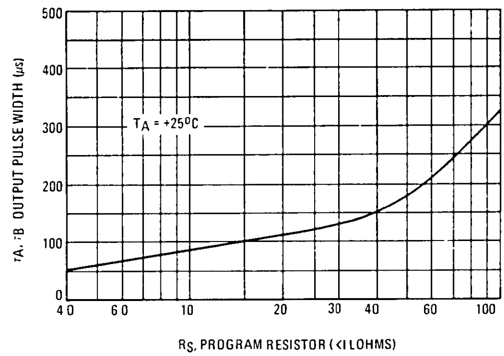
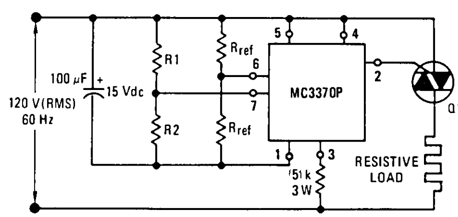


FIGURE 4 – OUTPUT PULSE WIDTH versus SOURCE RESISTANCE (See Figure 6.)



TYPICAL ZERO VOLTAGE SWITCH APPLICATIONS FOR TRIAC CONTROL

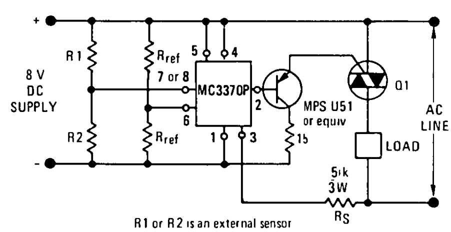
FIGURE 5 – TRIAC CONTROL CIRCUIT



R1 or R2 is an external sensor

Basic triac trigger circuit utilizing the zero crossing detector and the input comparator to control triacs with gate current requirements to 500 mA

FIGURE 6 – TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING DC SUPPLY



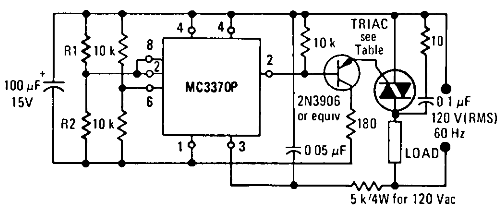
R1 or R2 is an external sensor

Basic dc trigger application using the input comparator to control a PNP capable of furnishing gate drive of approximately 0 5 A

Suggested circuit to vary output pulse width by value of R_S (See Figure 4)

R2 must be the external sensor for the internal short and open protection to be operative

FIGURE 7 – TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING AC SUPPLY



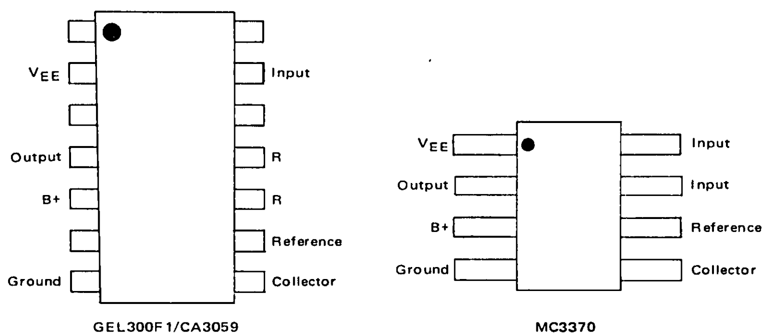
Zero crossing triac control circuit for gate current requirements to 100 mA

Recommended Motorola triacs for use in circuit.

Maximum Continuous Current (A [RMS])	Triac Family	Case No.
10	2N6151/2N6153 2N6346A/2N6349A	90 (Plastic) 221-024 (Plastic)
10	2N6139/2N6144	86, 250
25	2N6157/2N6165	174, 175, 235
40	2N5441/2N5446	237, 238, 239

6

PIN COMPARISON OF MC3370P AND GEL300F1 (PA424/CA3059)



6

MC3405
MC3505

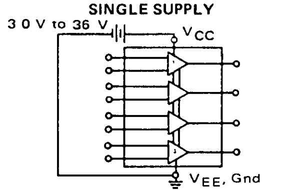
DUAL OPERATIONAL AMPLIFIER AND DUAL COMPARATOR

The MC3405/3505 contains two differential-input operational amplifiers and two comparators, each set capable of single supply operation. This operational amplifier-comparator circuit fulfills its applications as a general purpose product for automotive and consumer circuits as well as an industrial building block.

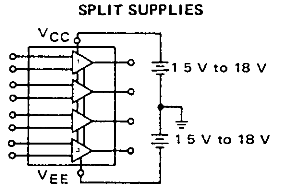
The MC3405 is specified over the commercial operating temperature range of 0 to +70°C, while the MC3505 is specified over the military operating range of -55 to +125°C.

- Operational Amplifiers Equivalent in Performance to MC3403/3503
- Comparators Similar in Performance to LM339/139
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Supply Current Drain
- Operational Amplifiers Are Internally Frequency Compensated
- Comparators TTL and CMOS Compatible

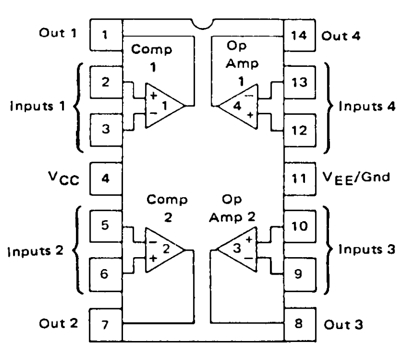
SINGLE SUPPLY



SPLIT SUPPLIES



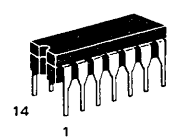
PIN CONNECTIONS



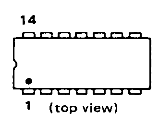
(Top View)

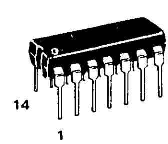
DUAL OPERATIONAL AMPLIFIER AND DUAL VOLTAGE COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116





P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3405 only)

ORDERING INFORMATION

Device	Temperature Range	Package
MC3405L	0 to +70°C	Ceramic DIP
MC3405P	0 to +70°C	Plastic DIP
MC3505L	-55 to +125°C	Ceramic DIP

OPERATIONAL AMPLIFIER SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage—Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	±18	Vdc
Operating Ambient Temperature Range—MC3505 MC3405	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range—Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	°C
Operating Junction Temperature Range—Ceramic Package Plastic Package	T_J	175 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MC3505 Min	MC3505 Typ	MC3505 Max	MC3405 Min	MC3405 Typ	MC3405 Max	Unit
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	nA
Large-Signal Open-Loop Voltage Gain (R_L = 2.0 kΩ)	A_{VOL}	20	200	–	20	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	µV/V
Output Voltage Range (Note 1) (R_L = 10 kΩ, V_{CC} = 5.0 V) (R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V)	V_{OR}	 3.3 V_{CC} -1.7	 3 5 V_{CC} -1.5	 – –	 3.3 V_{CC} -1.7	 3.5 V_{CC} -1.5	 – –	Vp-p
Power Supply Current (Notes 2 and 3)	I_{CC}	–	2.5	4 0	–	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	-120	–	–	-120	–	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MC3505 Min	MC3505 Typ	MC3505 Max	MC3405 Min	MC3405 Typ	MC3405 Max	Unit
Input Offset Voltage (T_A = T_{low} to T_{high}) (Note 4)	V_{IO}	– –	2.0 –	5.0 6.0	– –	2 0 –	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	–	15	–	µV/°C
Input Offset Current (T_A = T_{low} to T_{high}) (Note 4)	I_{IO}	– –	– –	50 200	– –	– –	50 200	nA
Input Bias Current (T_A = T_{low} to T_{high} (Note 4)	I_{IB}	– –	-200 -300	-500 -1500	– –	-200 –	-500 -800	nA
Input Common Mode Voltage Range	V_{ICR}	+13 -V_{EE}	–	–	+13-V_{EE}	–	–	Vdc
Large Signal Open Loop Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) (T_A = T_{low} to T_{high}) (Note 4)	A_{VOL}	 50 25	 200 100	 – –	 20 15	 200 100	 – –	V/mV
Common Mode Rejection Ratio	CMRR	70	90	–	70	90	–	dB
Power Supply Rejection Ratio	PSRR	–	30	150	–	30	150	µV/V
Output Voltage (R_L = 10 kΩ) (R_L = 2.0 kΩ) (R_L = 2.0 kΩ, T_A = T_{low} to T_{high}) (Note 4)	V_O	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	Vdc
Output Short-Circuit Current	I_{OS}	±10	±30	±45	±10	±20	±45	mA
Power Supply Current (Notes 2 and 3)	I_{CC}, I_{EE}	–	2 8	4 0	–	2.8	7.0	mA
Phase Margin	ϕm	–	60	–	–	60	–	Degrees
Small-Signal Bandwidth (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	BW	–	1.0	–	–	1.0	–	MHz
Power Bandwidth (A_V = 1, R_L = 2.0 kΩ, V_O = 20 V (p-p), THD = 5%)	BW_P	–	9.0	–	–	9.0	–	kHz
Rise Time/Fall Time	t_{TLH}, t_{THL}	–	0.35	–	–	0.35	–	µs
Overshoot (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	OS	–	20	–	–	20	–	%
Slew Rate	SR	–	0.6	–	–	0.6	–	V/µs

NOTES:
1. Output will swing to ground
2. Not to exceed maximum package power dissipation.
3. For Operational Amplifier and Comparator.
4. T_{low} = -55°C for MC3505 = 0°C for MC3405; T_{high} = +125°C for MC3505 = +70°C for MC3405

6

COMPARATOR SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage—Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Sink Current	I_{sink}	20	mA
Operating Ambient Temperature Range—MC3505 MC3405	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range—Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	°C
Operating Junction Temperature Range—Ceramic Package Plastic Package	T_J	175 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

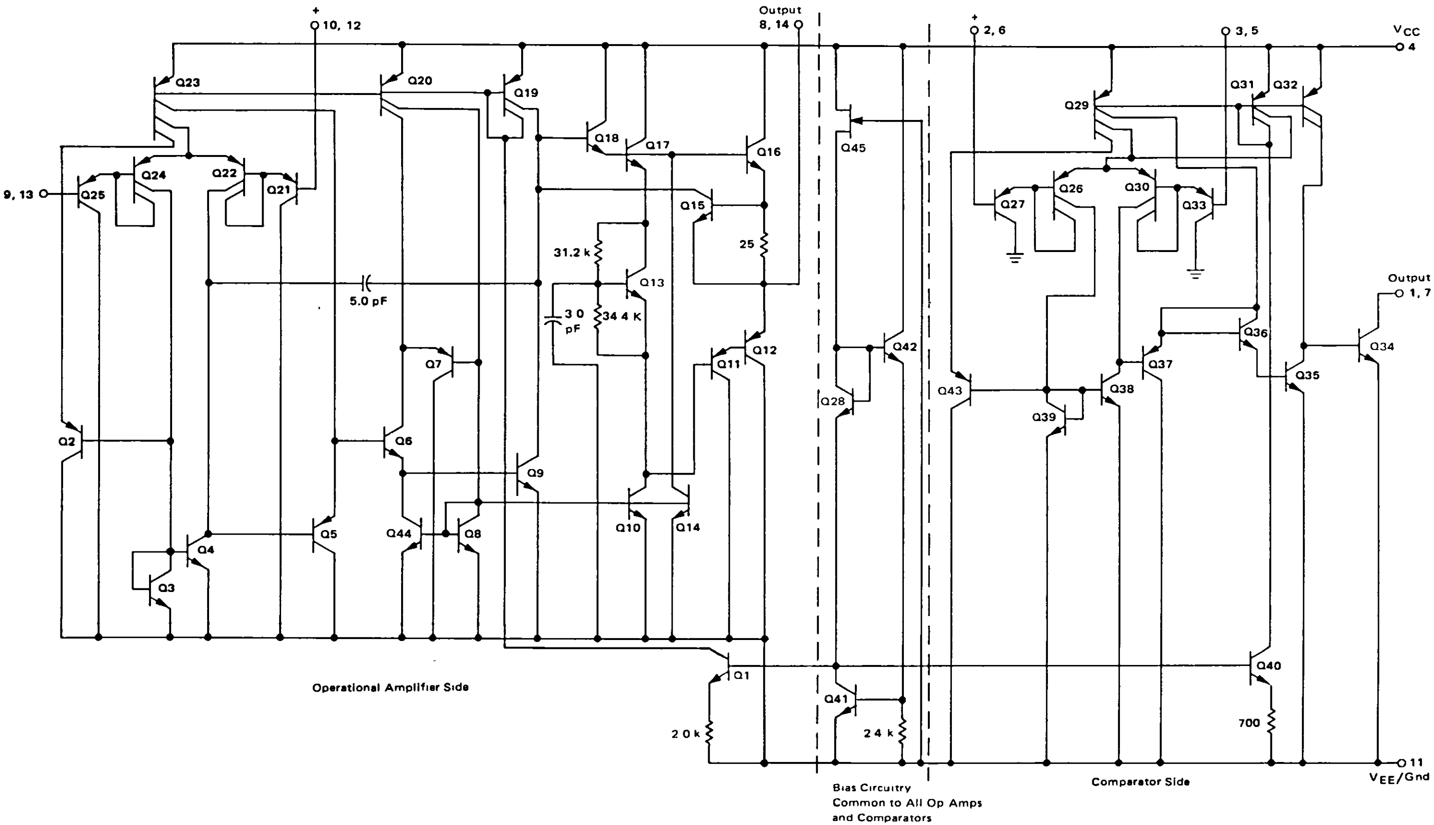
Characteristic	Symbol	MC3505			MC3405			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (T_A = T_{low} to T_{high}) (Notes 1 and 2)	V_{IO}	– –	2.0 –	5 0 9.0	– –	2 0 –	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	–	15	–	μV/°C
Input Offset Current (T_A = T_{low} to T_{high}) (Note 1)	I_{IO}	– –	50 –	75 150	– –	50 –	100 200	nA
Input Bias Current (T_A = T_{low} to T_{high}) (Note 1)	I_{IB}	– –	-125 –	-500 -1500	– –	-125 –	-500 -800	nA
Input Common Mode Voltage Range (T_A = T_{low} to T_{high}) (Note 1)	V_{ICR}	0 0	V_{CC} -1.5 V_{CC} -1.7	V_{CC} -1.7 V_{CC} -2 0	0 0	V_{CC} -1 5 V_{CC} -1.7	V_{CC} -1 7 V_{CC} -2 0	V
Input Differential Voltage (All V_{in} ≥ 0 Vdc)	V_{ID}	–	–	36	–	–	36	V
Large-Signal Open-Loop Voltage Gain (R_L = 15 kΩ)	A_{VOL}	–	200	–	–	200	–	V/mV
Output Sink Current (V_{in} (-) ≥ 1 0 Vdc, V_{in} (+) = 0, V_O ≤ 1 5 V)	I_{sink}	6.0	16	–	6.0	16	–	mA
Low Level Output Voltage (V_{in} (+) = 0 V, V_{in} (-) = 1 0 V, I_{sink} = 4 0 mA) (T_A = T_{low} to T_{high}) (Note 1)	V_{OL}	– –	350 –	500 700	– –	350 –	500 700	mV
Output Leakage Current (V_{in} (+) ≥ 1 0 Vdc, V_{in} (-) = 0, V_O = 5.0 Vdc) (T_A = T_{low} to T_{high}) (Note 1)	I_{OL}	– –	0.1 0.1	1.0 1.0	– –	0.1 0.1	1 0 1.0	μA
Large-Signal Response	–	–	300	–	–	300	–	ns
Response Time (Note 3) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	–	–	1.3	–	–	1.3	–	μs

NOTES: 1 T_{low} = -55°C for MC3505 T_{high} = +125°C for MC3505
= 0°C for MC3405 = +70°C for MC3405

2. V_O ≅ 1.4 V, R_S = 0 Ω with V_{CC} from 5 0 Vdc to 30 Vdc, and over the input common mode range 0 to V_{CC} – 1.7 V.
3. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals 300 ns is typical.

6

CIRCUIT SCHEMATIC
(1/2 OF CIRCUIT SHOWN)



OPERATIONAL AMPLIFIER SECTION

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

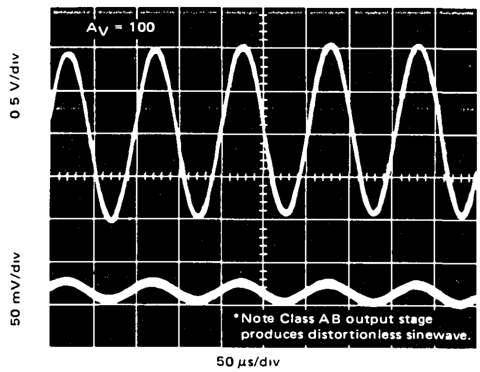


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

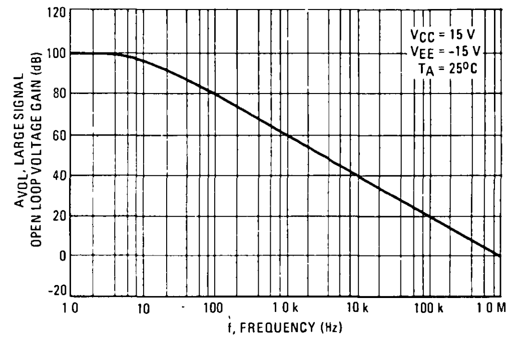


FIGURE 3 – POWER BANDWIDTH

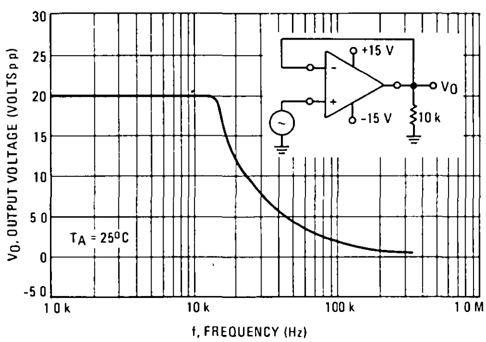


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

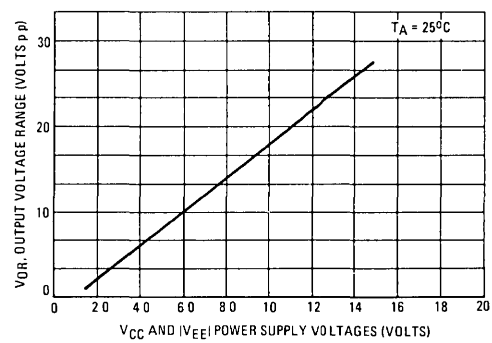


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

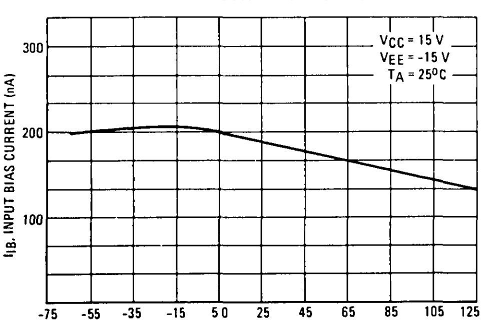
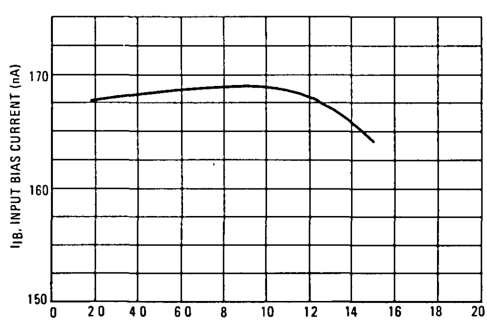


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



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COMPARATOR SECTION

TYPICAL PERFORMANCE CURVES

FIGURE 7 – NORMALIZED INPUT OFFSET VOLTAGE

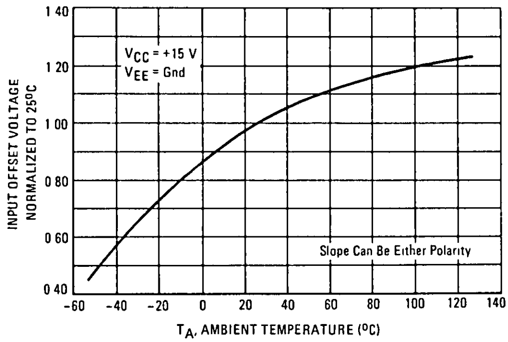


FIGURE 8 – INPUT BIAS CURRENT

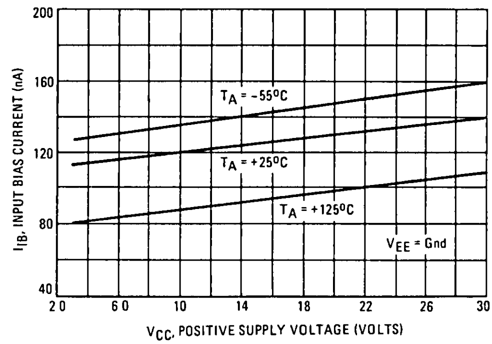


FIGURE 9 – NORMALIZED INPUT OFFSET CURRENT

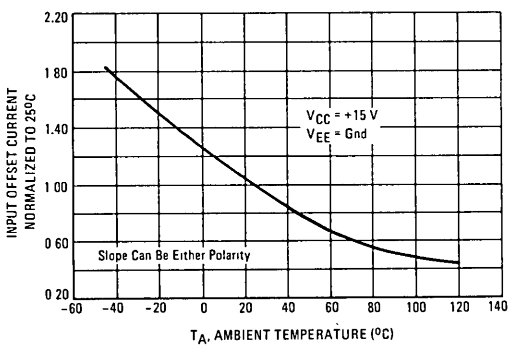
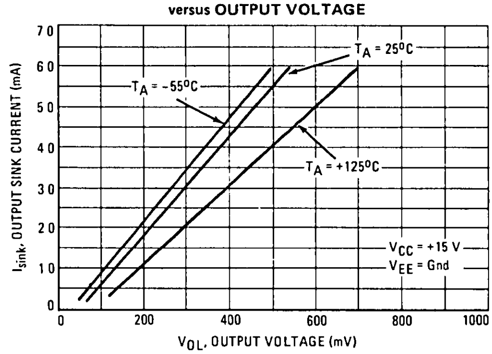
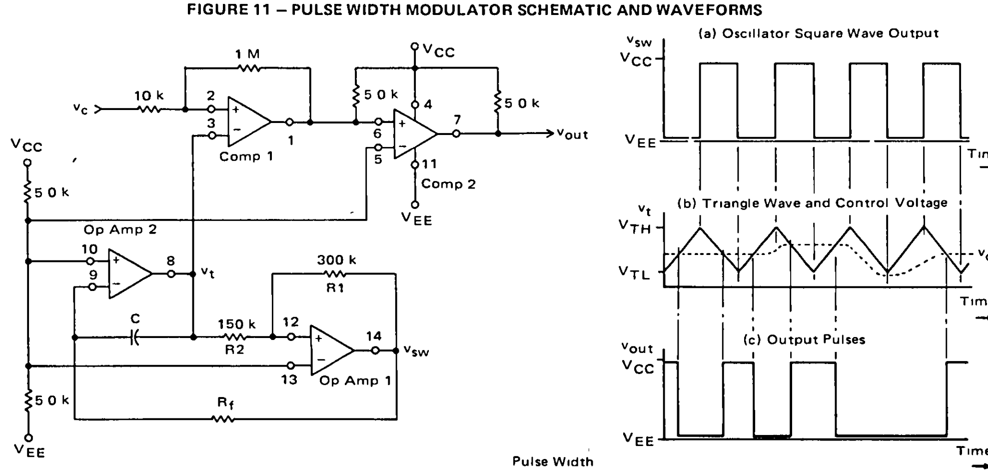


FIGURE 10 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



APPLICATIONS INFORMATION

FIGURE 11 – PULSE WIDTH MODULATOR SCHEMATIC AND WAVEFORMS



$$V_{TH} = \frac{1}{2} V_S (1 + R2/R1) + V_{EE} \qquad V_S = V_{CC} - V_{EE}$$

$$V_{TL} = \frac{1}{2} V_S (1 - R2/R1) + V_{EE}$$

Oscillator Frequency

$$f = \frac{R1}{4 R_f C R2}$$

Pulse Width

$$P.W. = \left(\frac{1}{f}\right)\left(\frac{v_c - V_{TL}}{V_{TH} - V_{TL}}\right) \quad \text{When. } V_{TL} < V_C < V_{TH}$$

Duty Cycle in %

$$D.C. = \left(\frac{v_c - V_{TL}}{V_{TH} - V_{TL}}\right)(100)$$

FIGURE 12 – WINDOW COMPARATOR

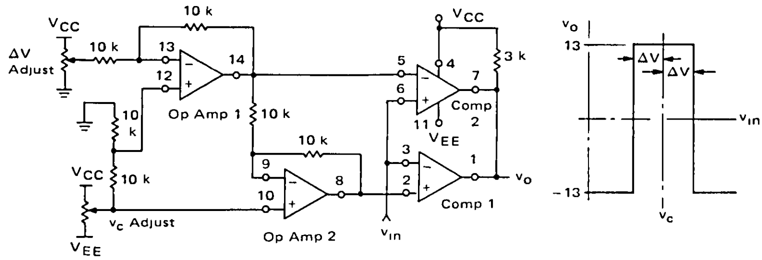
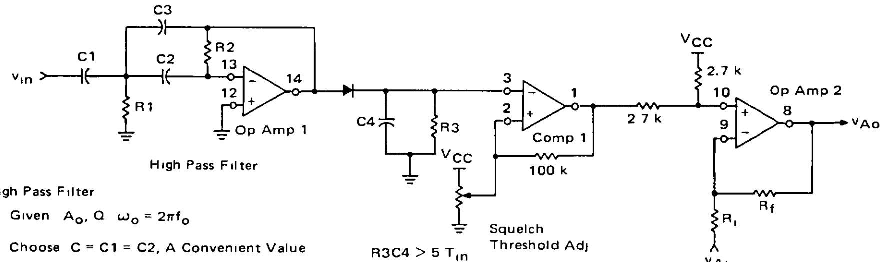


FIGURE 13 – SQUELCH CIRCUIT FOR AM OR FM



High Pass Filter

Given A_o, Q $\omega_o = 2\pi f_o$

Choose C = C1 = C2, A Convenient Value

Calculate $R2 = \frac{Q}{\omega_o C}(2A_o + 1)$

$C3 = \frac{C}{A_o}$

$R1 = \frac{A_o}{Q\omega_o C(2A_o + 1)}$

$R3C4 > 5\ T_{in}$

Where T_{in} is the period of v_{in}

Q = Quality Factor

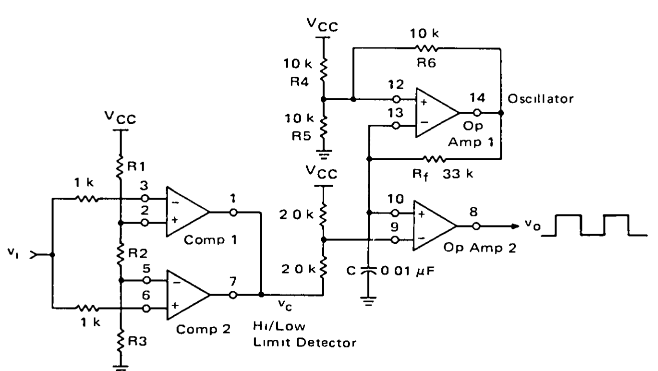
A_o = High Frequency Gain

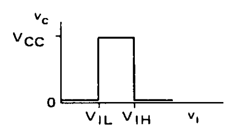
ω_o = Break Frequency

Gain of Audio Stage

$A_{cl} = -\frac{R_f}{R_i}$

FIGURE 14 – HIGH/LOW LIMIT ALARM





$V_{IL} = V_{CC}\frac{R3}{R1 + R2 + R3}$

$V_{IH} = V_{CC}\frac{R2 + R3}{R1 + R2 + R3}$

Oscillator

If R4 = R5 = R6

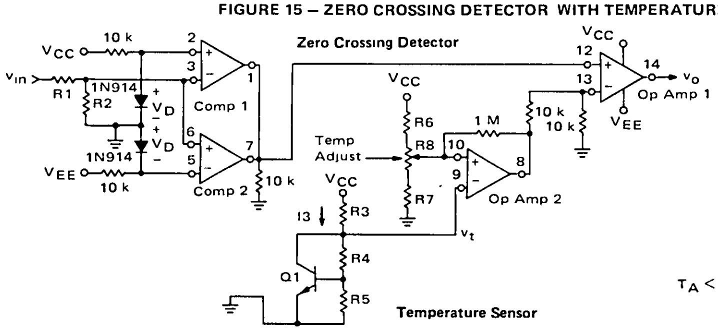
$f = 0.72/R_fC$

As Shown, f = 2.2 kHz

v_o Will Oscillate If $V_{IH} < v_i$, or $V_{IL} > v_i$

v_o Will Be Low If $V_{IL} < v_i < V_{IH}$

FIGURE 15 – ZERO CROSSING DETECTOR WITH TEMPERATURE SENSOR



$v_t = (V_{BE}\ \text{of Q1})\left(\frac{R4 + R5}{R5}\right)$

$I3 > \frac{2V_{BE}}{R5}$

R1 and R2 control the switching voltage of the zero crossing detector

$\pm V_s = \pm V_D \frac{R1 + R2}{R2}$

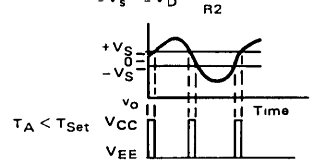
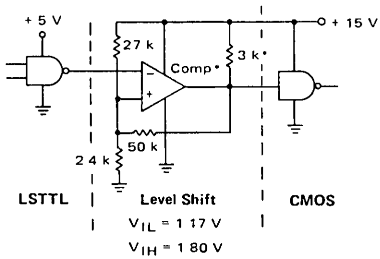
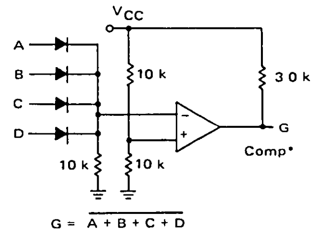


FIGURE 16 – LSTTL to CMOS INTERFACE WITH HYSTERESIS



*The same configuration may be used with an Op Amp if the 3 k resistor is removed

FIGURE 17 – "NOR" GATE



*The same configuration may be used with an Op Amp if the 3 k resistor is removed

6

MC3423
MC3523

Specifications and Applications Information

OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

These overvoltage protection circuits (OVP) protect sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. They sense the overvoltage condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

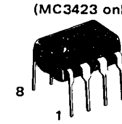
The protection voltage threshold is adjustable and the MC3423/3523 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423/3523 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.

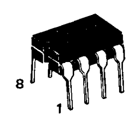
OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3423 only)



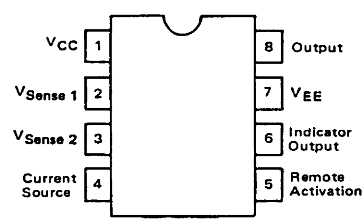
U SUFFIX
CERAMIC PACKAGE
CASE 693



MAXIMUM RATINGS

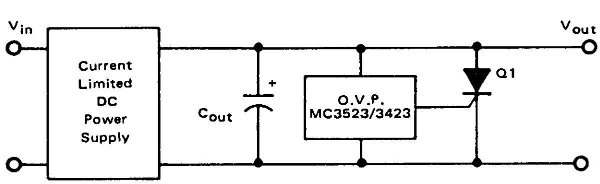
Rating	Symbol	Value	Unit
Differential Power Supply Voltage	V_{CC}-V_{EE}	40	Vdc
Sense Voltage (1)	$V_{Sense\ 1}$	6.5	Vdc
Sense Voltage (2)	$V_{Sense\ 2}$	6.5	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range MC3423 MC3523	T_A	 0 to +70 −55 to +125	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

PIN CONNECTIONS



(top view)

TYPICAL APPLICATION



NOTE: A 2N6504 or equivalent is suggested for Q1.

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3423P1	0 to +70°C	Plastic DIP
MC3423U	0 to +70°C	Ceramic DIP
MC3523U	−55 to +125°C	Ceramic DIP

6

ELECTRICAL CHARACTERISTICS (5 V < V_{CC} - V_{EE} < 36 V, T_{low} < T_A < T_{high} unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}-V_{EE}	4.5	–	40	Vdc
Output Voltage (I_O = 100 mA)	V_O	V_{CC}-2.2	V_{CC}-1.8	–	Vdc
Indicator Output Voltage ($I_{O(Ind)}$ = 1.6 mA)	V_{OL}(Ind)	–	0.1	0.4	Vdc
Sense Voltage (T_A = 25°C)	$V_{Sense\ 1}$, $V_{Sense\ 2}$	2.45	2.6	2.75	Vdc
Temperature Coefficient of $V_{Sense\ 1}$ (Figure 2)	TCV_{S1}	–	0.06	–	%/°C
Remote Activation Input Current					μA
(V_{IH} = 2.0 V, V_{CC}-V_{EE} = 5.0 V)	I_{IH}	–	5.0	40	
(V_{IL} = 0.8 V, V_{CC}-V_{EE} = 5.0 V)	I_{IL}	–	-120	-180	
Source Current	I_{source}	0.1	0.2	0.3	mA
Output Current Risetime (T_A = 25°C)	t_r	–	400	–	mA/μs
Propagation Delay (T_A = 25°C)	t_{pd}	–	0.5	–	μs
Supply Current	I_D				mA
MC3423		–	6.0	10	
MC3523		–	5.0	7.0	

T_{low} = -55°C for MC3523
= 0°C for MC3423

T_{high} = +125°C for MC3523
= +70°C for MC3423

FIGURE 1 – BLOCK DIAGRAM

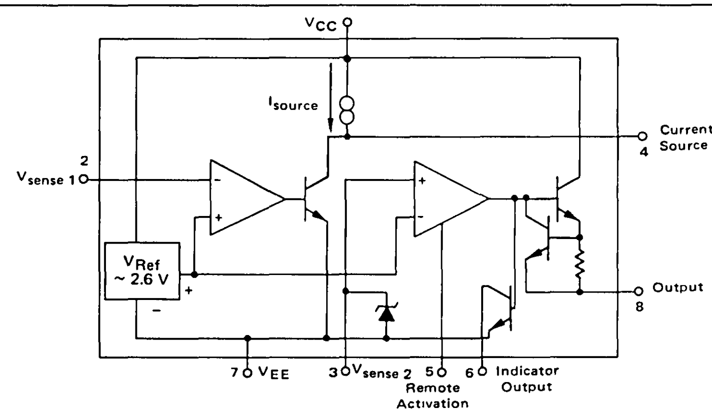
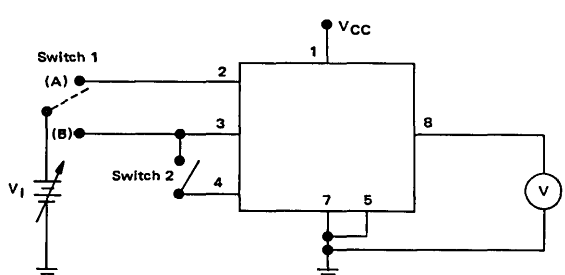


FIGURE 2 – SENSE VOLTAGE TEST CIRCUIT

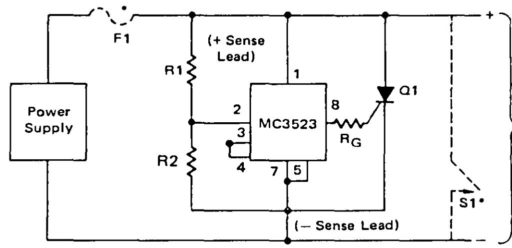


	Switch 1	Switch 2
$V_{Sense\ 1}$	Position A	Closed
$V_{Sense\ 2}$	Position B	Open

Ramp V_I until output goes high; this is the V_{Sense} threshold.

6

FIGURE 3 — BASIC CIRCUIT CONFIGURATION



$V_{trip} = V_{ref}\,(1+\frac{R1}{R2}) \approx 2.6\ V\,(1+\frac{R1}{R2})$

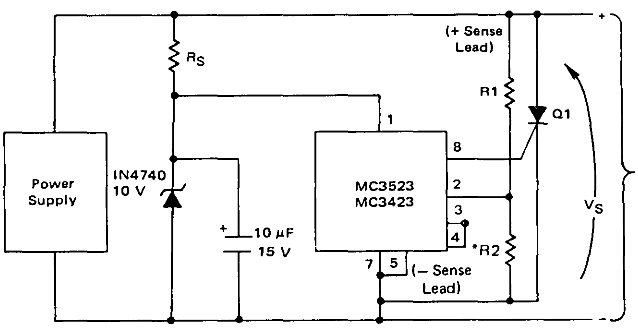
R2 ≤ 10 kΩ for minimum drift

For minimum value of R_G, see Figure 9

Q1 is 2N6504 or equivalent

*See text for explanation

FIGURE 4 — CIRCUIT CONFIGURATION FOR SUPPLY VOLTAGE ABOVE 36 V



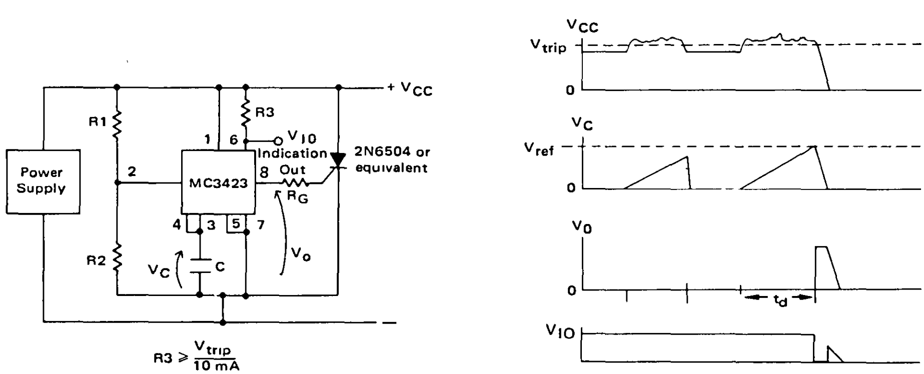
To Load $R_S = (\frac{V_S - 10}{25})\ k\Omega$

$V_{trip} = V_{ref}\,(1+\frac{R1}{R2}) \approx 2.6\ V\,(1+\frac{R1}{R2})$

*R2 ≤ 10 kΩ

Q1 $V_S \leq 50$ V; 2N6504 or equivalent
$V_S \leq 100$ V, 2N6505 or equivalent
$V_S \leq 200$ V, 2N6506 or equivalent
$V_S \leq 400$ V, 2N6507 or equivalent
$V_S \leq 600$ V; 2N6508 or equivalent
$V_S \leq 800$ V, 2N6509 or equivalent

FIGURE 5 — BASIC CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP



$R3 \geq \frac{V_{trip}}{10\ mA}$

$t_d = \frac{V_{ref}}{I_{source}} \times C \approx (12 \times 10^3)\ C$ (See Figure 10)

6

APPLICATIONS INFORMATION

BASIC CIRCUIT CONFIGURATION

The basic circuit configuration of the MC3423/3523 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423/3523 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, R_G, is given in Figure 9. Using this value of R_G, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423/3523. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

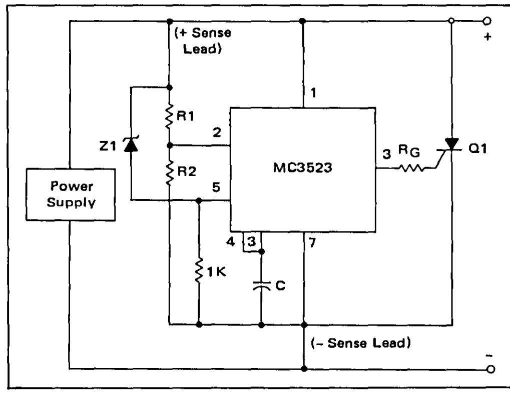
The circuit configurations shown in Figures 3 and 4 will have a typical propogation delay of 1.0 μs. If faster operation is desired, pin 3 may be connected to pin 2 with pin 4 left floating. This will result in decreasing the propogation delay to approximately 0.5 μs at the expense of a slightly increased TC for the trip voltage value.

CONFIGURATION FOR PROGRAMMABLE MINIMUM DURATION OF OVERVOLTAGE CONDITION BEFORE TRIPPING

In many instances, the MC3423/3523 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423/3523 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from pin 3 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging the capacitor, C, connected to pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds V_{Z1} + 1.4 V.

FIGURE 6 – CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP/WITH IMMEDIATE TRIP AT HIGH OVERVOLTAGES



ADDITIONAL FEATURES

1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V as in Figure 5. This output can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423/3523 is its remote activation input, pin 5. If the volage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

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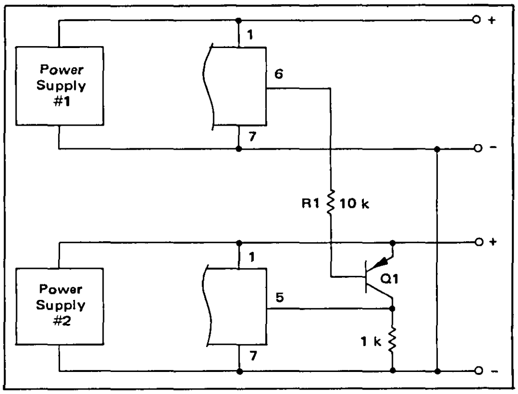
FIGURE 7 – CIRCUIT CONFIGURATION FOR ACTIVATING ONE MC3523 FROM ANOTHER



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

FIGURE 8 – R1 versus TRIP VOLTAGE

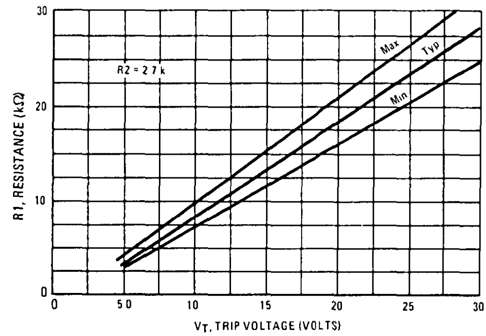


FIGURE 9 – MINIMUM R_G versus SUPPLY VOLTAGE

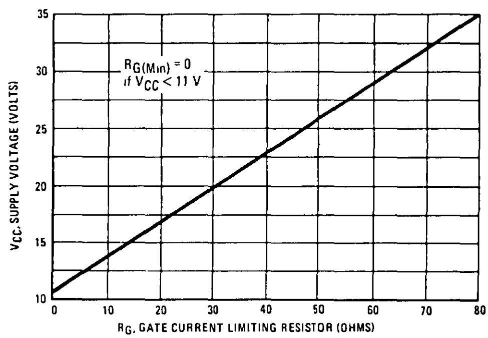
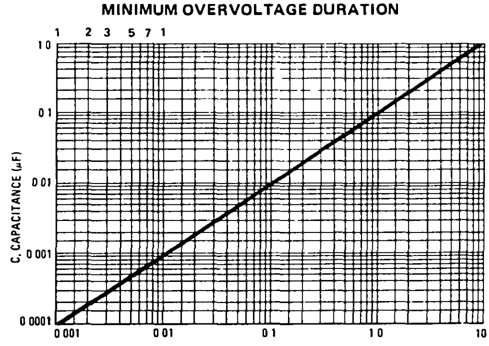


FIGURE 10 – CAPACITANCE versus MINIMUM OVERVOLTAGE DURATION



CROWBAR SCR CONSIDERATIONS

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}[1]. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the application make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

[1]C_{out} consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps.

FIGURE 11 – TYPICAL CROWBAR OVP CIRCUIT CONFIGURATIONS

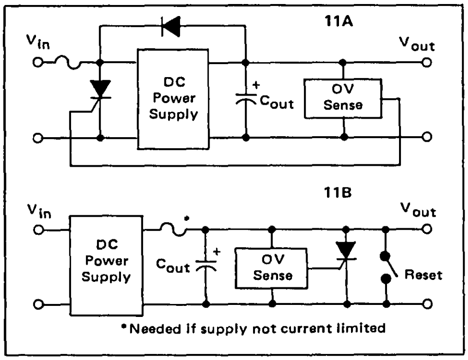


FIGURE 12 – CROWBAR SCR SURGE CURRENT WAVEFORM

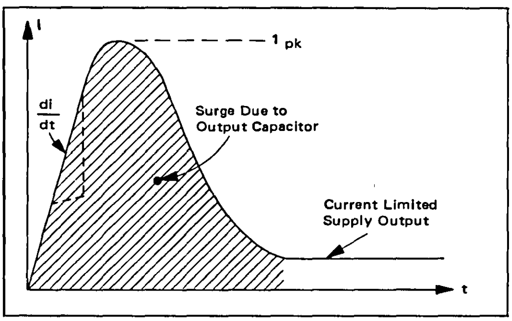
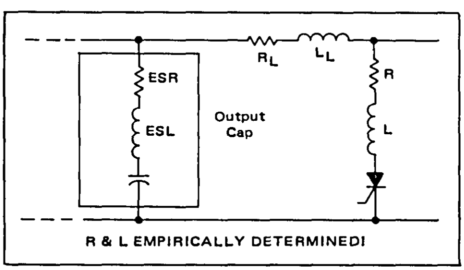


FIGURE 13 – CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{TSM}	PACKAGE
2N6400 Series	16A	160A	TO220 Plastic
2N6504 Series	25A	160A	TO220 Plastic
2N1842 Series	16A	125A	Metal Stud
2N2573 Series	25A	260A	Metal TO-3 Type
2N681 Series	25A	200A	Metal Stud
MCR3935-1 Series	35A	350A	Metal Stud
MCR81-5 Series	80A	1000A	Metal Stud

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast (< 1 μs) rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 Arms rating might be 200 A/μs, assuming a gate current of five times I_{GT} and < 1 μs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance – see Figure 13) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Refering back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC3456L	—	0°C to +70°C	Ceramic DIP
MC3456P	NE556A	0°C to +70°C	Plastic DIP
MC3556L	—	−55°C to +125°C	Ceramic DIP

MC3456
MC3556

Specifications and Applications Information

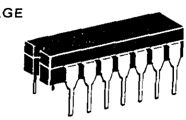
DUAL
TIMING CIRCUIT
SILICON MONOLITHIC
INTEGRATED CIRCUIT

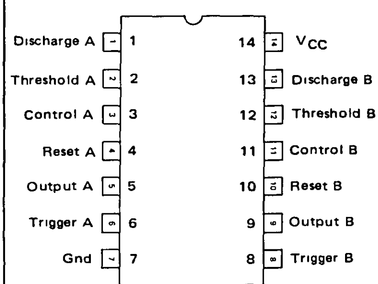
DUAL TIMING CIRCUIT

The MC3556/MC3456 dual timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor per timer. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor per timer. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE556/SE556 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output
- Dual Version of the Popular MC1555/MC1455 Timer

L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116





(top view)

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3456 only)

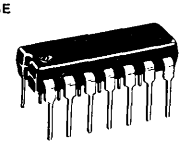


FIGURE 1 — 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

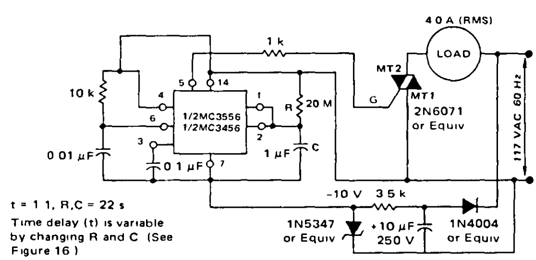
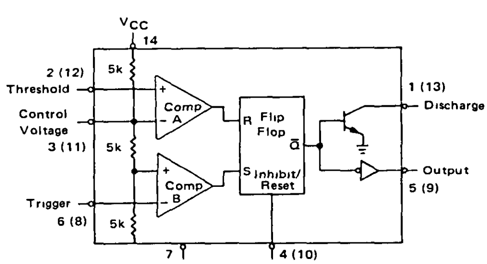


FIGURE 2 — BLOCK DIAGRAM (1/2 SHOWN)



MTTL is a Trademark of Motorola Inc.

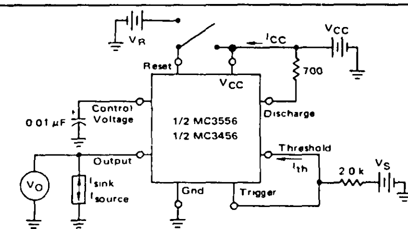
TYPICAL APPLICATIONS

- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current	I_{dis}	200	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual-In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Ambient Temperature Range	T_A		°C
MC3556		-55 to +125	
MC3456		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters
(to set output and measure parameters)
a When $V_S \geq 2/3\ V_{CC}$ V_O is low
b When $V_S \leq 1/3\ V_{CC}$, V_O is high
c When V_O is low, pin 7 sinks current To test for Reset set V_O high, apply Reset voltage, and test for current flowing into discharge pin When Reset is not in use it should be tied to V_{CC}

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5 0 V to +15 V unless otherwise noted)

Characteristics	Symbol	MC3556			MC3456			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4 5	–	18	4 5	–	16	V
Supply Current (Per timer, double for both halfs)	I_{CC}							mA
V_{CC} = 5 0 V, $R_L = \infty$		–	3 0	5 0	–	3 0	6 0	
V_{CC} = 15 V, $R_L = \infty$		–	10	12	–	10	15	
Low State, (Note 1)								
Timing Error (Note 2)								
Monostable Mode								
R_A = 2 0 kΩ to 100 kΩ								
Initial Accuracy C = 0 1 µF		–	0 5	1 5	–	0 75	–	%
Drift with Temperature		–	30	100	–	50	–	PPM/°C
Drift with Supply Voltage		–	0 15	0 2	–	0 1	–	%/Volt
Astable Mode								
$R_A = R_B$ = 2 0 kΩ to 100 kΩ								
C = 0 01 µF								
Initial Accuracy		–	1 5	–	–	2 25	–	%
Drift with Temperature		–	90	–	–	150	–	PPM/°C
Drift with Supply Voltage		–	0 15	–	–	0 3	–	%/Volt
Threshold Voltage	V_{th}	–	2/3	–	–	2/3	–	xV_{CC}
Trigger Voltage	V_T							V
V_{CC} = 15 V		4 8	5 0	5 2	–	5 0	–	
V_{CC} = 5 0 V		1 45	1 67	1 9	–	1 67	–	
Trigger Current	I_T	–	0 5	–	–	0 5	–	µA
Reset Voltage	V_R	0 4	0 7	1 0	0 4	0 7	1 0	V
Reset Current	I_R	–	0 1	–	–	0 1	–	mA
Threshold Current (Note 3)	I_{th}	–	0 03	0 1	–	0 03	0 1	µA
Control Voltage Level	V_{CL}							V
V_{CC} = 15 V		9 6	10	10 4	9 0	10	11	
V_{CC} = 5 0 V		2 9	3 33	3 8	2 6	3 33	4 0	
Output Voltage Low	V_{OL}							
(V_{CC} = 15 V)								V
I_{sink} = 10 mA		–	0 1	0 15	–	0 1	0 25	
I_{sink} = 50 mA		–	0 4	0 5	–	0 4	0 75	
I_{sink} = 100 mA		–	2 0	2 25	–	2 0	2 75	
I_{sink} = 200 mA		–	2 5	–	–	2 5	–	
(V_{CC} = 5 0 V)								
I_{sink} = 8 0 mA		–	0 1	0 25	–	–	–	
I_{sink} = 5 0 mA		–	–	–	–	0 25	0 35	
Output Voltage High	V_{OH}							V
(I_{source} = 200 mA)								
V_{CC} = 15 V		–	12 5	–	–	12 5	–	
(I_{source} = 100 mA)								
V_{CC} = 15 V		13	13 3	–	12 75	13 3	–	
V_{CC} = 5 0 V		3 0	3 3	–	2 75	3 3	–	
Toggle Rate (Figures 17, 19)								
R_A = 3 3 kΩ, R_B = 6 8 kΩ, C = 0 003 µF	–	–	100	–	–	100	–	kHz
Discharge Leakage Current	I_{dis}	–	20	100	–	20	100	nA
Rise Time of Output	t_{OLH}	–	100	–	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	–	100	–	ns
Matching Characteristics Between Sections								
(Monostable)								
Initial Timing Accuracy		–	0 5	1 0	–	1 0	2 0	%
Timing Drift with Temperature		–	± 10	–	–	± 10	–	ppm/°C
Drift with Supply Voltage		–	0 1	0 2	–	0 2	0 5	%/V

NOTES
1 Supply current when output is high is typically 2 0 mA less
2 Tested at V_{CC} = 5 0 V and V_{CC} = 15 V
3 This will determine the maximum value of $R_A + R_B$ for 15 V operation The maximum total R = 20 megohms

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TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 4 – TRIGGER PULSE WIDTH

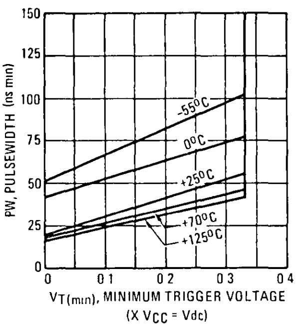


FIGURE 5 – SUPPLY CURRENT

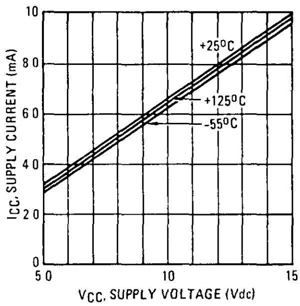


FIGURE 6 – HIGH OUTPUT VOLTAGE

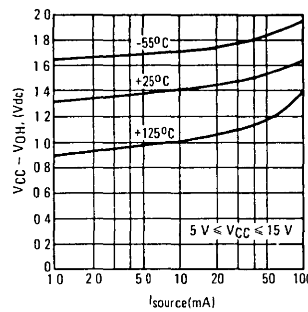


FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

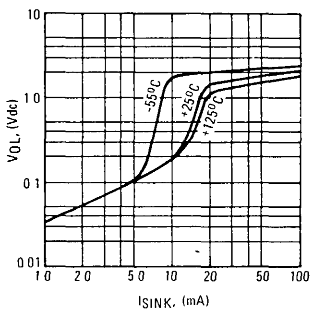


FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

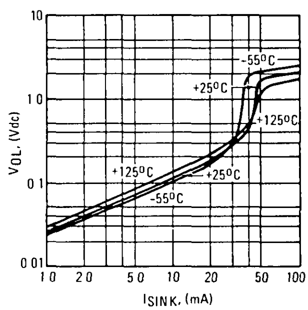


FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

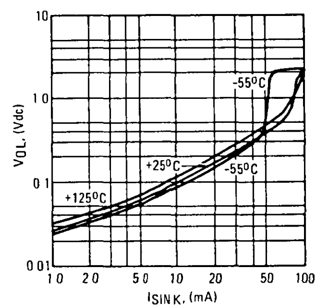


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

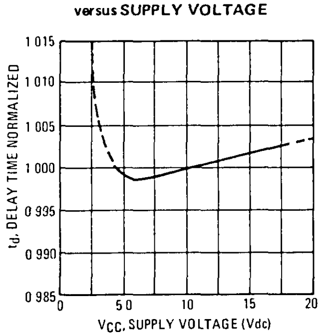


FIGURE 11 – DELAY TIME versus TEMPERATURE

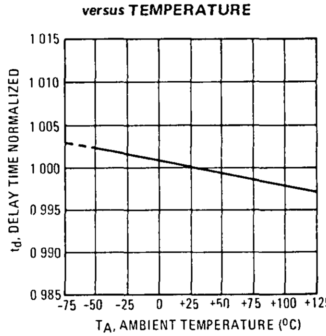
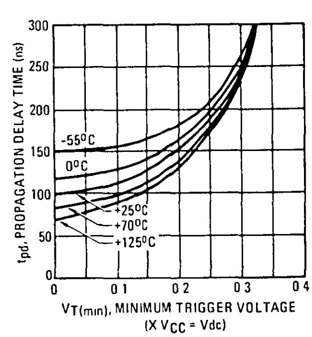
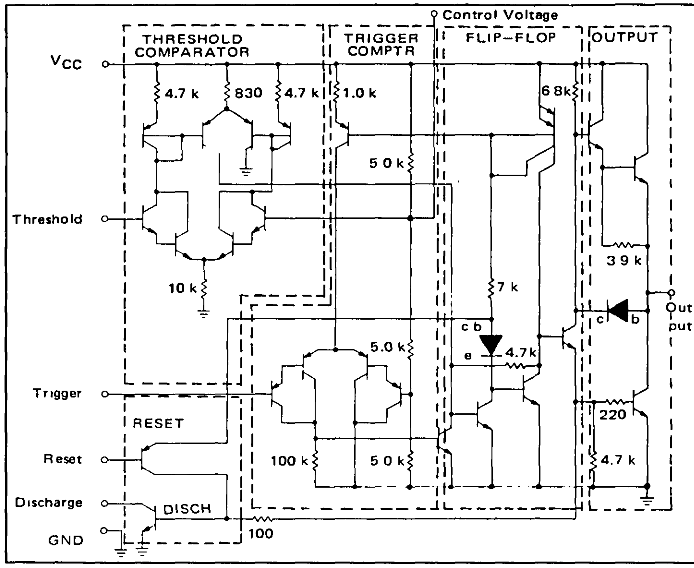


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE



6

FIGURE 13 – 1/2 REPRESENTATIVE CIRCUIT SCHEMATIC



GENERAL OPERATION

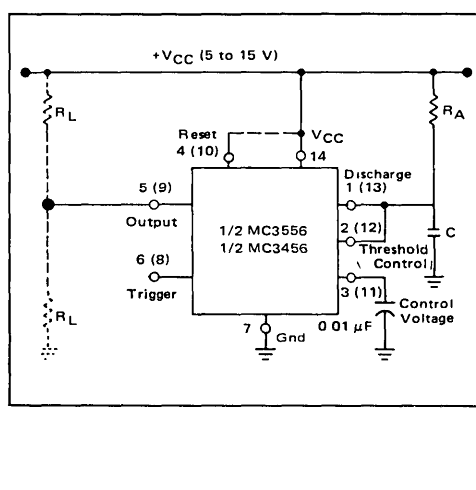
The MC3556 is a dual timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

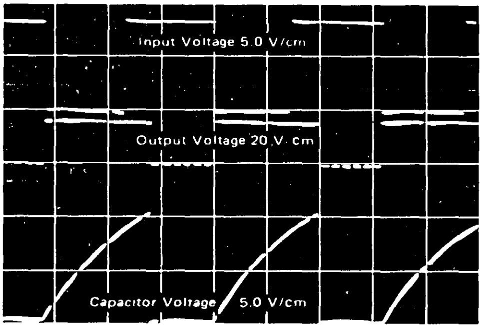
A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

FIGURE 14 – MONOSTABLE CIRCUIT



GENERAL OPERATION (continued)

FIGURE 15 – MONOSTABLE WAVEFORMS



t = 50 µs/cm
(R_A = 10 kΩ, C = 0.01 µF, R_L = 1.0 kΩ, V_{CC} = 15 V)

FIGURE 16 – TIME DELAY

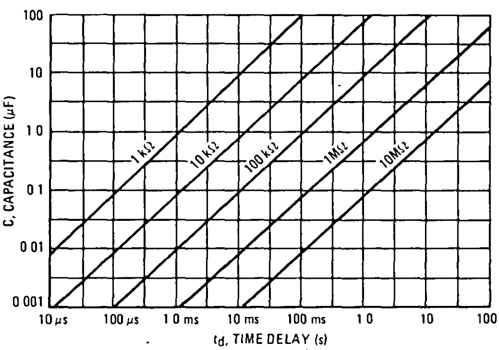


FIGURE 17 – ASTABLE CIRCUIT

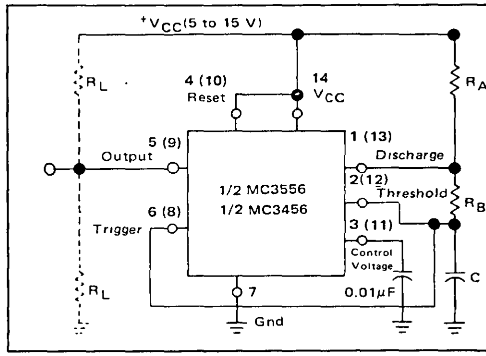
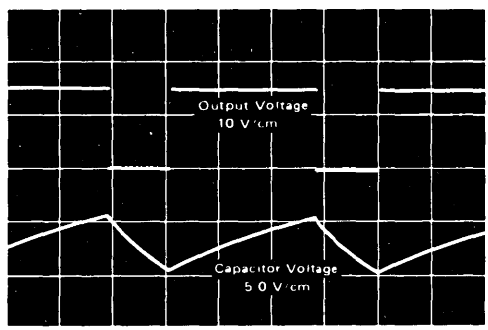


FIGURE 18 – ASTABLE WAVEFORMS



t = 20 µs/cm
(R_A = 5.1 kΩ, C = 0.01 µF, R_L = 1.0 kΩ;
R_B = 3.9 kΩ, V_{CC} = 15 V)

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by $t_1 = 0.695\,(R_A+R_B)\,C$

The discharge time (output low) by $t_2 = 0.695\,(R_B)\,C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695\,(R_A+2R_B)\,C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B)\,C}$

and may be easily found as shown in Figure 19.

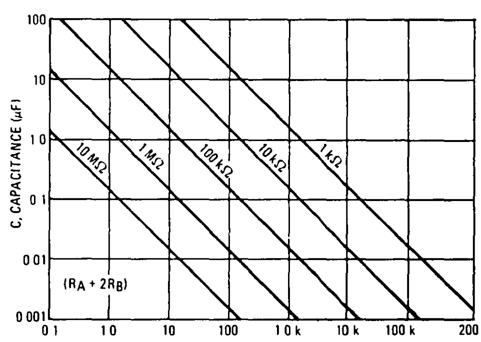
The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\,(Vdc)}{I_7\,(A)} \geq \frac{V_{CC}\,(Vdc)}{0.2}$$

FIGURE 19 – FREE-RUNNING FREQUENCY



6

APPLICATIONS INFORMATION

TONE BURST GENERATOR

For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at Pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.

DUAL ASTABLE MULTIVIBRATOR

This dual astable multivibrator provides versatility not available with single timer circuits. The duty cycle can be adjusted from 5% to 95%. The two outputs provide two phase clock signals often required in digital systems. It can also be inhibited by use of either reset terminal.

FIGURE 20 – TONE BURST GENERATOR

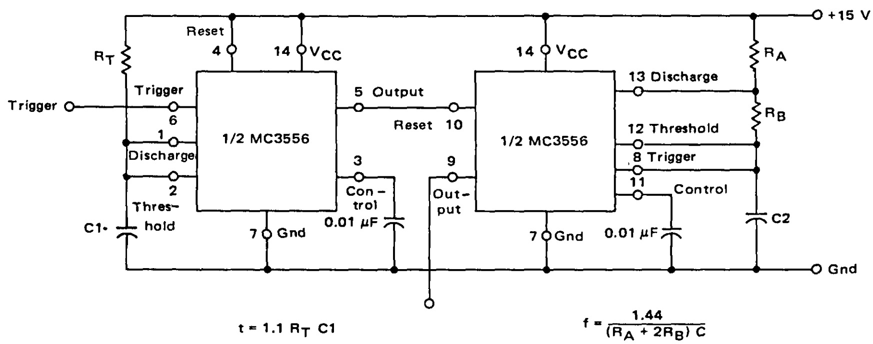
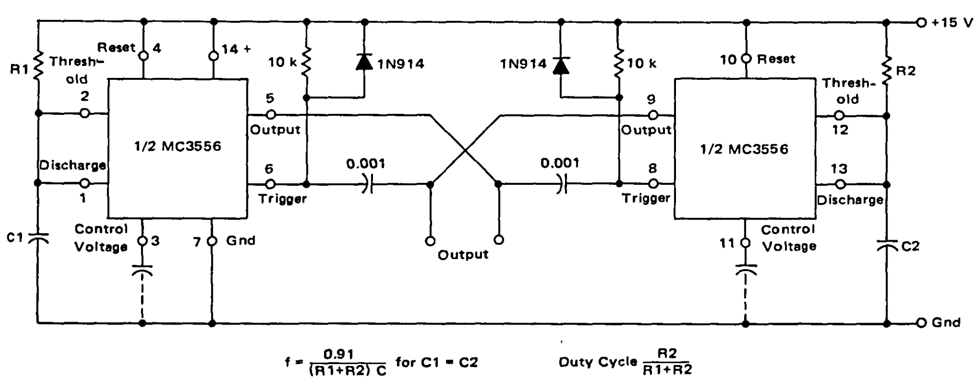


FIGURE 21 – DUAL ASTABLE MULTIVIBRATOR



6

APPLICATIONS INFORMATION (continued)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 3. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 22

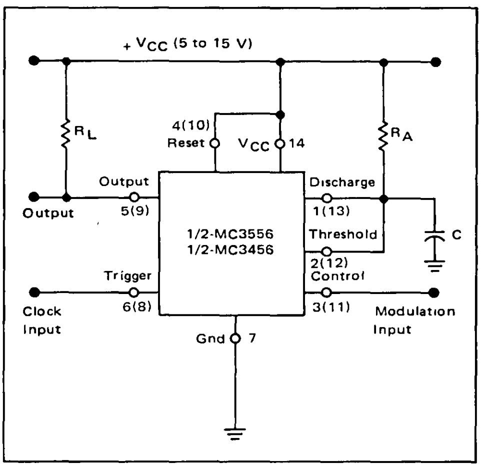
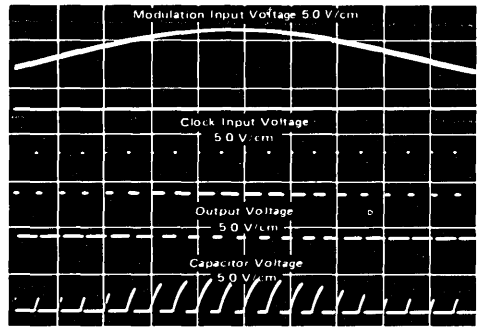


FIGURE 23 – PULSE WIDTH MODULATION WAVEFORMS
(R_A = 10 kΩ, C = 0.02 µF, V_{CC} = 15 V)

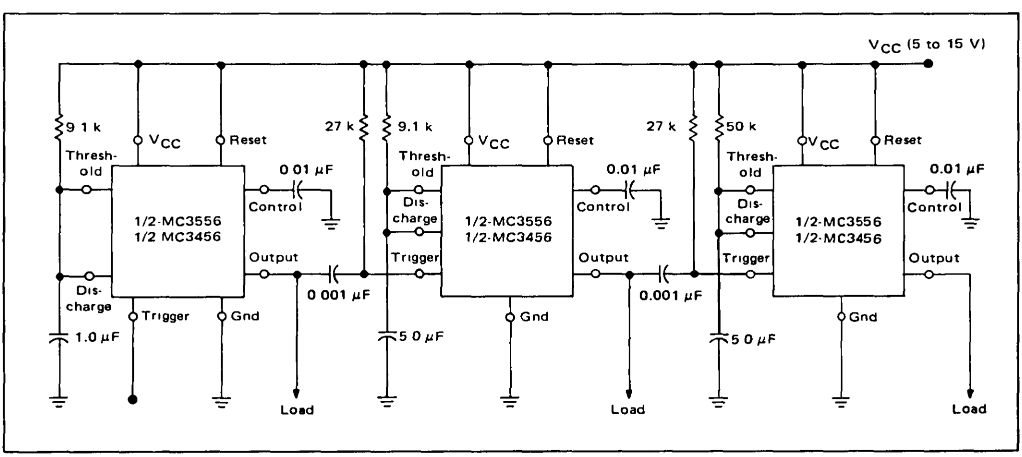


t = 0.5 ms/cm

Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 24 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 24



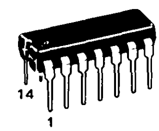
NE565N

PHASE-LOCKED LOOP
SILICON MONOLITHIC INTEGRATED CIRCUIT

PHASE-LOCKED LOOP

The NE565N is designed for general-purpose phase-locked loop applications to 500 kHz.

- Stable Center Frequency – 200 ppm/°C (Typ)
- Flexible Power Supply Range – ±5 to ±12 Volts with Small Frequency Drift – 100 ppm/% (Typ)
- Low Total Harmonic Distortion of Demodulator Output – 1.5% (Max)
- Linear Triangle Wave Output – 0.5% (Typ)
- TTL, DTL Compatible Inputs and Outputs
- Adjustable Hold In Range – ±1% to >±60%.



N SUFFIX
Plastic Package
CASE 646

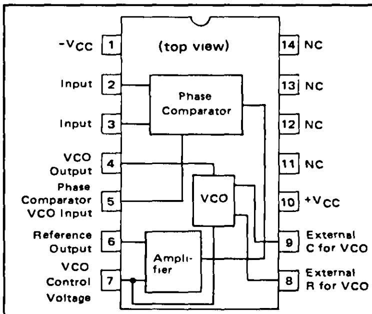


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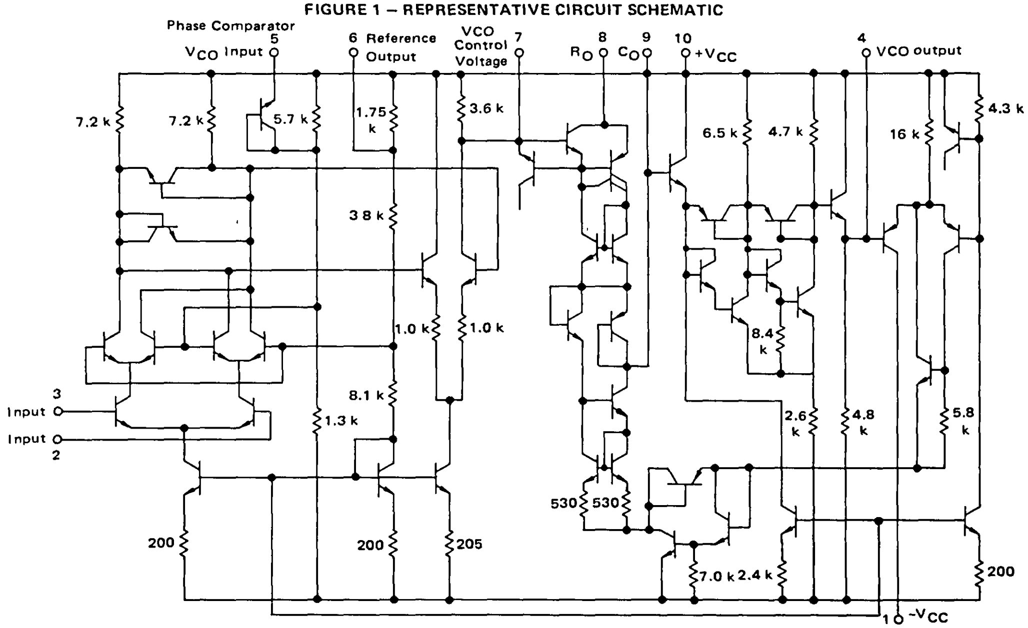
FIGURE 1 – REPRESENTATIVE CIRCUIT SCHEMATIC



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	±12	Vdc
Power Dissipation (Package Limitation) Derate above 25°C	P_D	8.25 6.6	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Test Circuit Figure 2, T_A = 25°C, V_{CC} = ±6.0 Vdc unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Power Supply Current*	–	8.0	12.5	mA
Input Impedance (Pins 2, 3) -4.0 V < V2, V3 < 0 V	–	5.0	–	kΩ
Input Level Required for Tracking f_o = 10 kHz, ±10% Frequency Deviation	10	–	–	mVrms
VCO Maximum Operating Frequency C_o = 2.7 pF	–	500	–	kHz
Operating Frequency Temperature Coefficient	–	200	–	ppm/°C
Frequency Drift with Supply Voltage	–	200	–	ppm/%
Triangle Wave Ouptut Voltage	2.0	2.4	3.0	Vp-p
Triangle Wave Output Linearity	–	0.5	–	%
Square Wave Output Level	4.7	5.4	–	Vp-p
VCO Output Impedance (Pin 4)	–	5.0	–	kΩ
Square Wave Duty Cycle	40	50	60	%
Square Wave Rise Time	–	20	–	ns
Square Wave Fall Time	–	50	–	ns
Output Current Sink (Pin 4)	0.6	1.0	–	mA
VCO Sensitivity	–	6600	–	Hz/V
Demodulated Output Voltage (Pin 7) f_o = 10 kHz, ±10% Frequency Deviation	200	300	–	mVp-p
Total Harmonic Distortion f_o = 10 kHz, ±10% Frequency Deviation	–	0.2	1.5	%
Output Impedance (Pin 7)	–	3.5	–	kΩ
DC Output Voltage Level (Pin 7)	4.0	4.5	5.0	V
Output Offset Voltage (Input = 0) /V7-V6/	–	50	200	mV
Temperature Drift of /V7-V6/	–	500	–	μV/°C
AM Rejection	–	40	–	dB
Phase Detector Sensitivity K_D	–	0.68	–	V/radian

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FIGURE 2 – TEST CIRCUIT SCHEMATIC

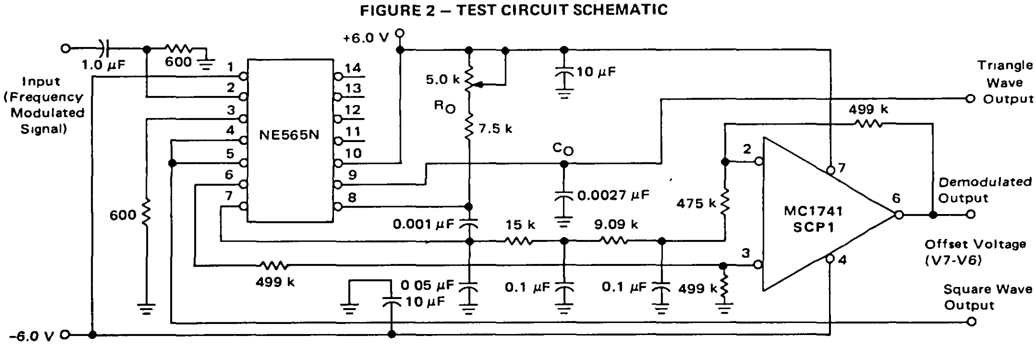


FIGURE 3 – POWER SUPPLY CHARACTERISTICS

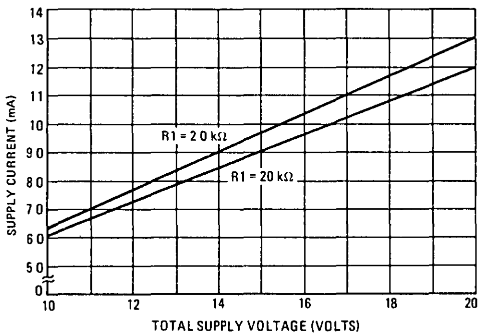


FIGURE 4 – VCO CONVERSION GAIN

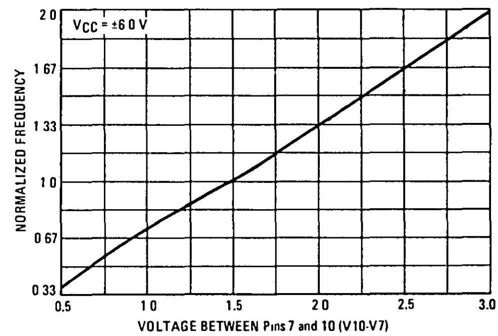


FIGURE 5 – LOCK RANGE versus INPUT VOLTAGE

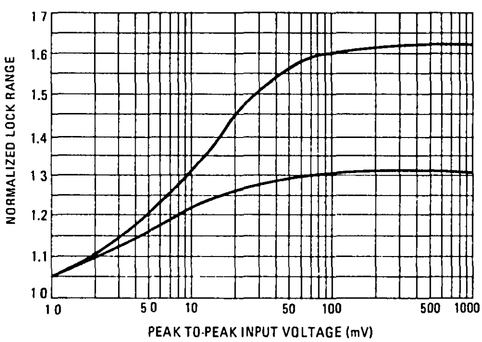


FIGURE 6 – OSCILLATOR OUTPUT WAVEFORMS

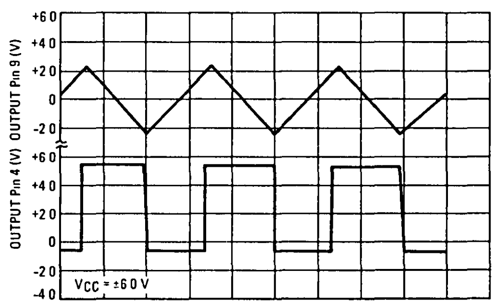


FIGURE 7 – LOCK RANGE
(As a Function of Gain Setting Resistance)

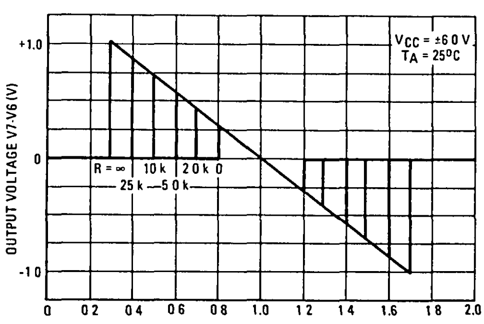
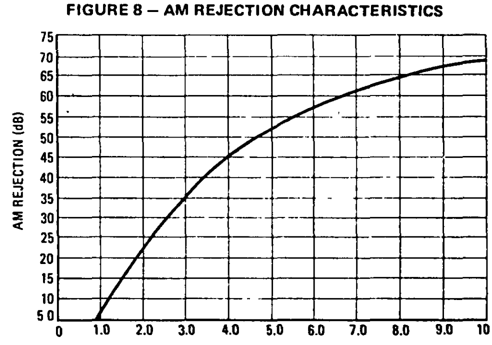


FIGURE 8 – AM REJECTION CHARACTERISTICS



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GENERAL APPLICATIONS INFORMATION

The following formulas are useful when designing with the NE565N:

1. Center Frequency – $f_O \approx \frac{1}{3.7\ R_O C_O}$

   Where: f_O is the frequency of the VCO without input signal. For R_O, C_O circuit location see Figure 2.

2. Loop Gain – $K_O K_D A$

   Definitions:

   K_O – VCO Conversion Gain – the conversion factor between VCO frequency and control voltage. $K_O = 4.12\ f_O$ (units are in radians/sec/volt)

   Example: for VCO Sensitivity @ 10 kHz (in Hz/volt)

   $$K_O = \frac{4.12 \times 10^4}{2\pi \text{ radians}} = 6600 \text{ Hz/Volt}$$

   K_D – Phase Detector Gain Factor – the conversion factor between the phase detector output voltage and the phase difference between input and VCO signals. Units are in volts/radian.

   $$K_D = \frac{8.1 \bullet A}{V_{CC}}$$

   Where: A = f(R6 to R7)

   Hence: $K_D = \frac{8.1}{V_{CC}}\ [f(R6\text{-}R7)]$

   Where: V_{CC} is total system supply voltage, f(R6-R7) is internal amplifier gain (See Figure 9). V_{CC} - total supply voltage to the circuit.

3. Lock Range – $f_L = \pm \frac{8 f_O}{V_{CC}}$

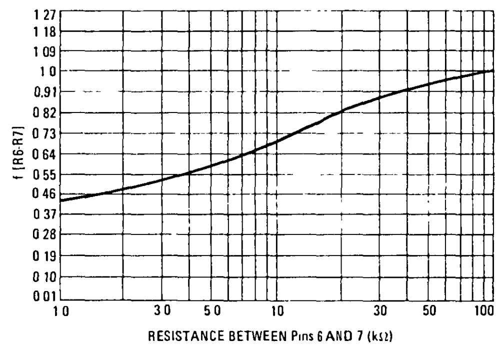
   Where: f_L is the range of frequencies in the area of f_O over which the VCO, once locked to the input signal, will remain locked.

4. Capture Range – $f_C \approx \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

   Where: f_C is that range of frequencies around f_O over which the loop will acquire lock with an input signal initially starting out of lock.

   (τ = Time Constant at Pin 7)

FIGURE 9 – INTERNAL AMPLIFIER GAIN CHARACTERISTICS



6

NE592
SE592

VIDEO AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

DIFFERENTIAL TWO-STAGE VIDEO AMPLIFIER

The SE/NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the MC1733.

- 90 MHz Bandwidth
- Adjustable Gains From 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required

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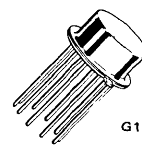
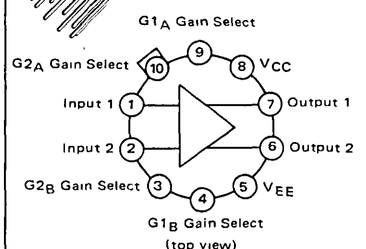
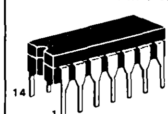


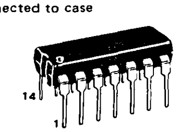
K SUFFIX
METAL PACKAGE
CASE 603



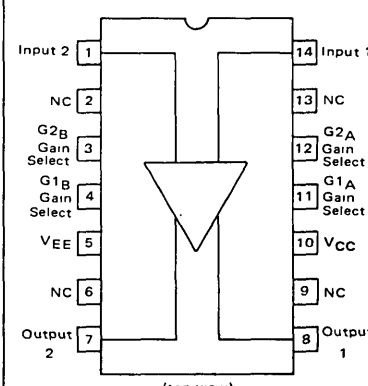
Pin 5 connected to case



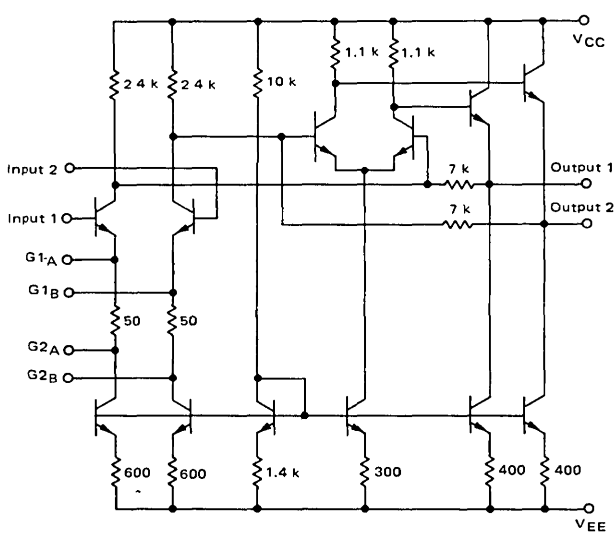
F SUFFIX
CERAMIC PACKAGE
CASE 632



N SUFFIX
PLASTIC PACKAGE
CASE 646



CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
NE592N	0 to 70°C	Plastic DIP
NE592K	0 to 70°C	Metal Can
NE592F	0 to 70°C	Ceramic DIP
SE592K	-55 to +125°C	Metal Can
SE592F	-55 to +125°C	Ceramic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8 0 −8.0	Volts
Differential Input Voltages	V_{ID}	±5.0	Volts
Common-Mode Input Voltage	V_{IC}	±6 0	Volts
Output Current	I_o	10	mA
Operating Ambient Temperature Range SE592 NE592	T_A	 -55 to +125 0 to +70	°C
Operating Junction Temperature Range Metal and Ceramic Packages Plastic Package	T_J	 175 150	°C
Storage Temperature Range Metal and Ceramic Packagee Plastic Package	T_{stg}	 -65 to +150 -55 to +125	°C

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted. (V_{CC} = +6.0 V, V_{EE} = -6.0 V, V_{CM} = 0)

Characteristic	Symbol	SE592			NE592			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain – Figure 3 (R_L = 2 kΩ, e_{out} = 3 Vp-p) (Gain 1, Note 1) (Gain 2, Note 2)	A_{vd}	 300 90	 400 100	 500 110	 250 80	 400 100	 600 120	V/V
Bandwidth – Figure 3 (Gain 1, Note 1) (Gain 1, Note 2)	BW	 – –	 40 90	 – –	 – –	 40 90	 – –	MHz
Rise Time – Figure 3 (Gain 1, e_{out} = 1 Vp-p, Note 1) (Gain 2, e_{out} = 1 Vp-p, Note 2)	 t_{TLH} t_{THL}	 – –	 10 5 4 5	 – 10	 – –	 10 5 4 5	 – 12	ns
Propagation Delay – Figure 3 (Gain 1, e_{out} = 1 Vp-p, Note 1) (Gain 2, e_{out} = 1 Vp-p, Note 2)	 t_{PLH} t_{PHL}	 – –	 7 5 6 0	 – 10	 – –	 7 5 6 0	 – 10	ns
Input Resistance (Gain 1, Note 1) (Gain 2, Note 2)	R_{in}	 – 20	 4 0 30	 – –	 – 10	 4 0 30	 – –	kΩ
Input Capacitance (Gain 2, Note 2)	C_{in}	–	2 0	–	–	2 0	–	pF
Input Offset Current (Gain 3, Note 3) – Fig. 2	I_{IO}	–	0 4	3 0	–	0 4	5 0	μA
Input Bias Current (Gain 3, Note 3) – Fig. 2	I_{IB}	–	9 0	20	–	9 0	30	μA
Input Noise Voltage (Gain 1 and Gain 2) (BW = 1 kHz to 10 MHz) – Figure 1	V_n	–	12	–	–	12	–	μV(rms)
Input Voltage Range (Gain 2, Note 2) – Fig. 3	V_{in}	±1 0	–	–	±1 0	–	–	V
Common-Mode Rejection Ratio – Figure 3 (Gain 2, V_{CM} = ±1 V, f ≤ 100 kHz) (Gain 2, V_{CM} = ±1 V, f = 5 MHz)	CMRR	 60 –	 86 60	 – –	 60 –	 86 60	 – –	dB
Supply Voltage Rejection Ratio – Figure 2 (Gain 2, Δ V_s = ±0 5 V)	PSRR	50	70	–	50	70	–	dB
Output Offset Voltage – Figure 2 (Gain 3, R_L = ∞, Note 3)	V_{OO}	–	0 35	0.75	–	0 35	0.75	V
Output Common-Mode Voltage – Figure 2 (R_L = ∞, Gain 3, Note 3)	V_{CMO}	2 4	2 9	3 4	2 4	2.9	3 4	V
Output Voltage Swing – Figure 3 (R_L = 2k, Gain 2, Note 2)	V_O	3.0	4 0	–	3.0	4 0	–	Vp-p
Output Resistance	r_o	–	20	–	–	20	–	Ω
Power Supply Current – Figure 2 (R_L = ∞, Gain 2, Note 2)	I_D	–	18	24	–	18	24	mA

Note 1. Gain select pins $G1_A$ and $G1_B$ connected together.

Note 2. Gain select pins $G2_A$ and $G2_B$ connected together.

Note 3. All gain select pins open.

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ELECTRICAL CHARACTERISTICS $T_A = T_{high}$ to T_{low} unless otherwise noted.* (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, V_{CM} = 0)

Characteristic	Symbol	SE592 Min	SE592 Typ	SE592 Max	NE592 Min	NE592 Typ	NE592 Max	Units
Differential Voltage Gain – Figure 3 (R_L = 2 kΩ, e_{out} = 3 Vp-p)	A_{vd}							V/V
(Gain 1, Note 1)		200	–	600	250	–	600	
(Gain 2, Note 2)		80	–	120	80	–	120	
Input Resistance (Gain 2)	R_{in}	8.0	–	–	8.0	–	–	kΩ
Input Offset Current (Gain 3) – Figure 2	$\lvert I_{IO} \rvert$	–	–	5.0	–	–	6.0	µA
Input Bias Current (Gain 3) – Figure 2	I_{IB}	–	–	40	–	–	40	µA
Input Voltage Range (Gain 2) – Figure 3	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio – Figure 3 (Gain 2, V_{CM} = ±1 V, f ≤ 100 kHz)	CMRR	50	–	–	50	–	–	dB
Supply Voltage Rejection Ratio – Figure 2 (Gain 2, Δ V_s = ±0.5 V)	PSRR	50	–	–	50	–	–	dB
Output Offset Voltage (Gain 3) – Figure 2	V_{OO}	–	–	1.2	–	–	1.5	V
Output Voltage Swing (Gain 2) – Figure 3	V_O	2.5	–	–	2.5	–	–	Vp-p
Power Supply Current (Gain 2) – Figure 2	I_D	–	–	27	–	–	27	mA

*T_{low} = 0°C for NE592, -55°C for SE592
T_{high} = +70°C for NE592, +125°C for SE592

GENERAL TEST CIRCUITS

FIGURE 1

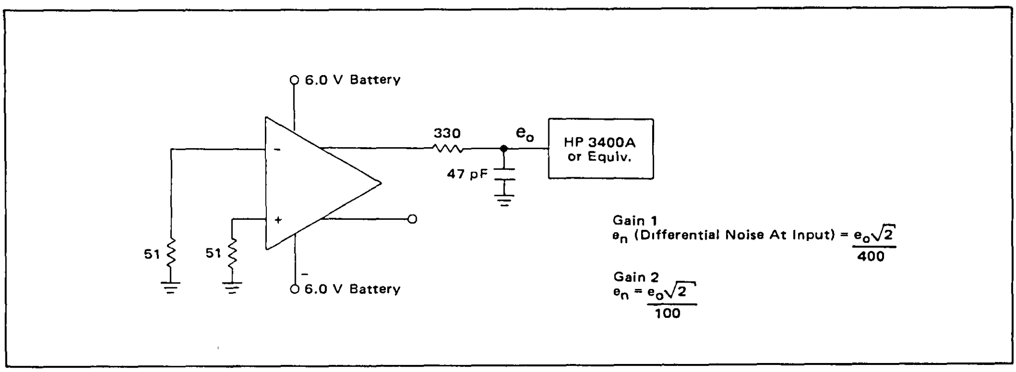


FIGURE 2

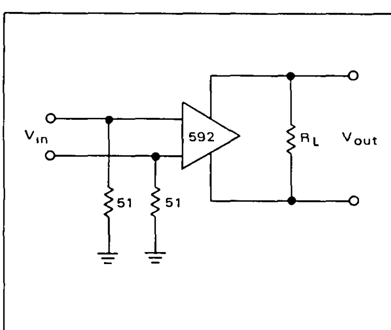
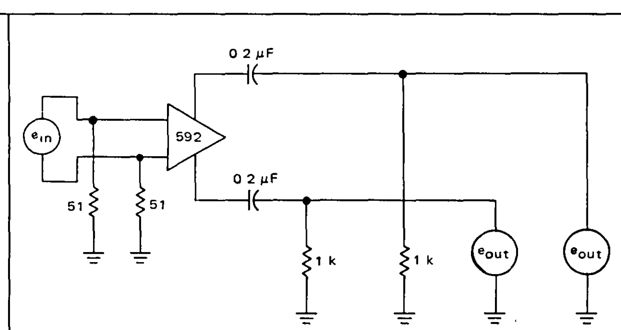


FIGURE 3



6

FIGURE 4 – GAIN 1 versus FREQUENCY

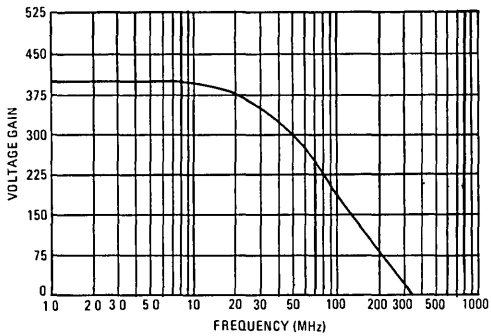


FIGURE 5 – GAIN 2 versus FREQUENCY

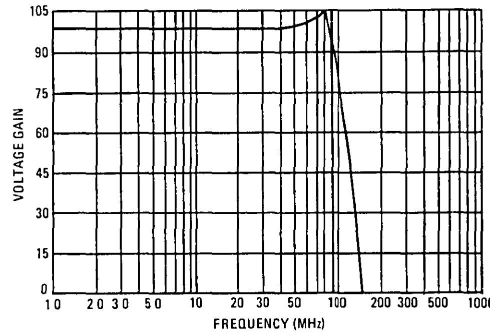


FIGURE 6 – OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

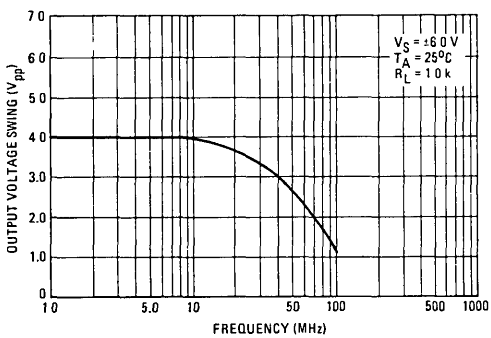


FIGURE 7 – OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

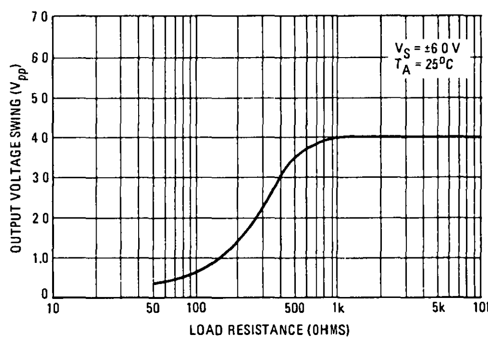
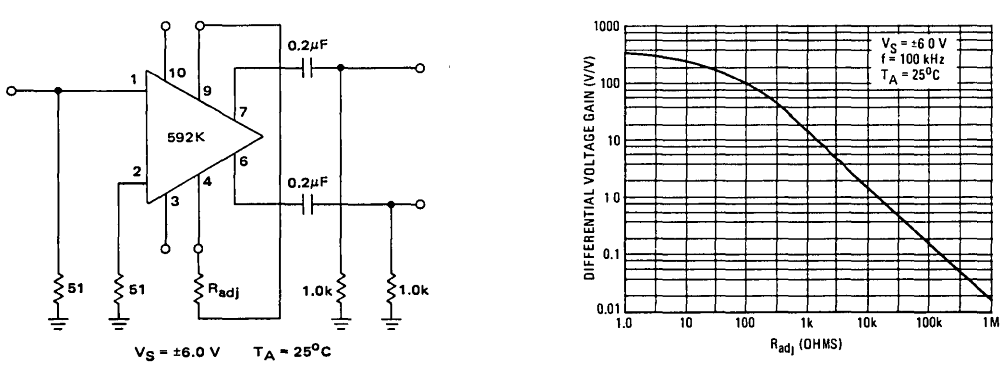


FIGURE 8 – VOLTAGE GAIN AS A FUNCTION OF R_{adj} RESISTANCE



6

FIGURE 9 – DISK/TAPE PHASE MODULATED READBACK SYSTEMS

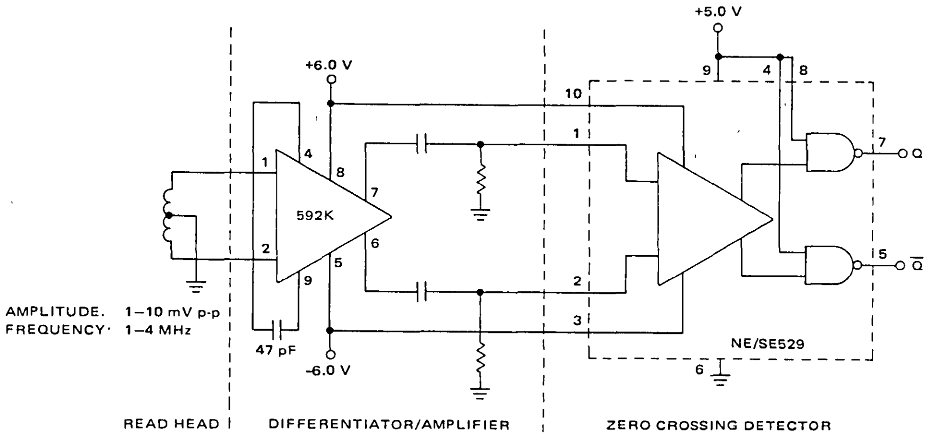
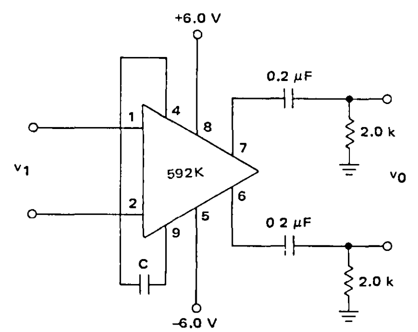


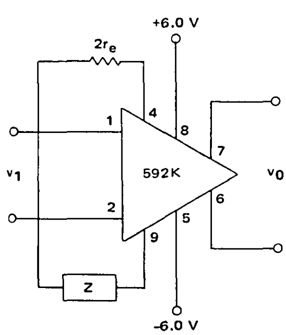
FIGURE 10 – DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



FOR FREQUENCY $f_1 << 1/2\pi(32)C$

$$v_O \cong 1\,4 \times 10^4 C \frac{dv_1}{dt}$$

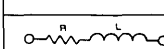
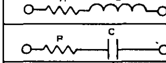
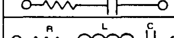
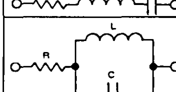
FIGURE 11 – FILTER NETWORKS



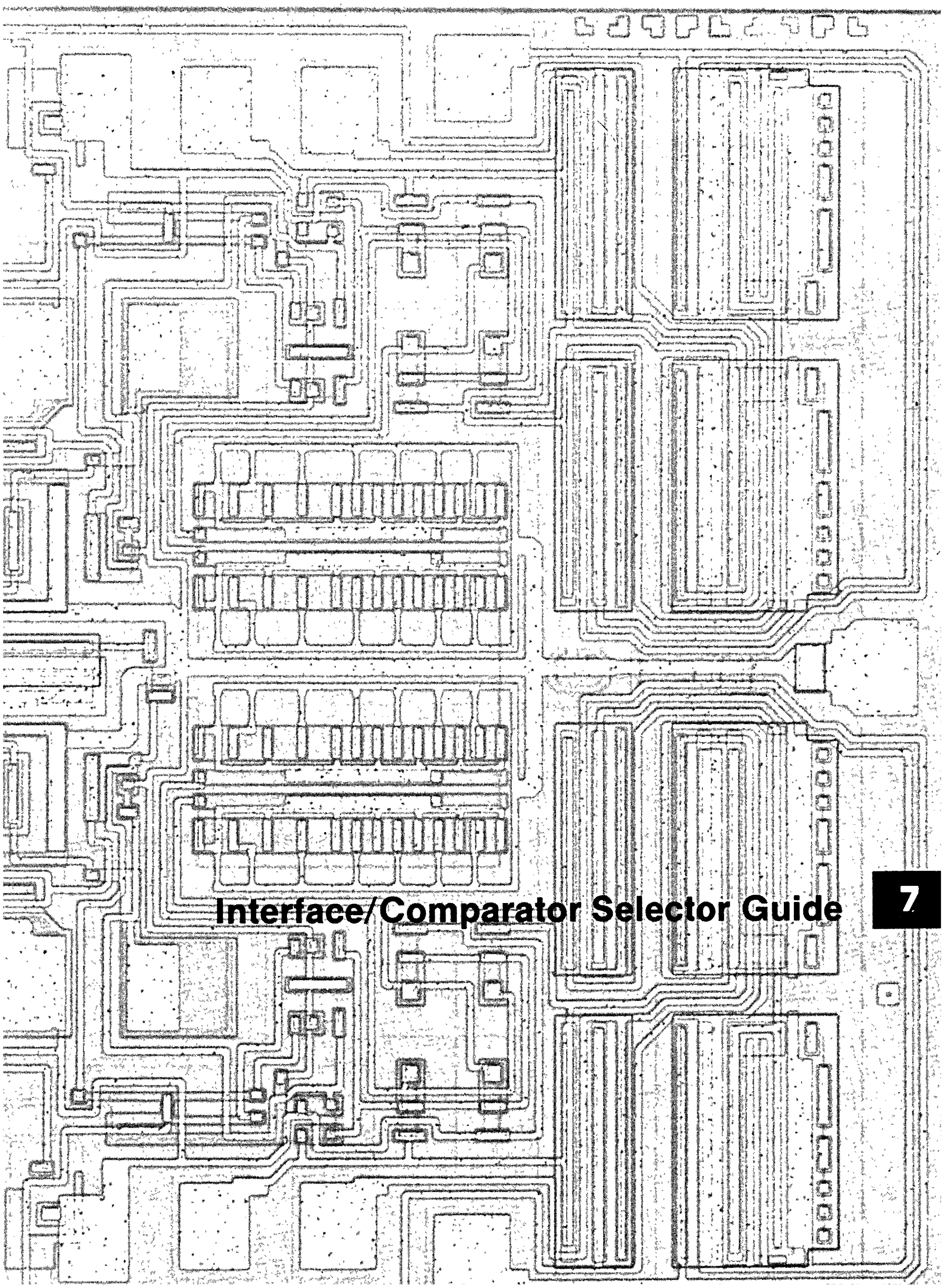
$$\frac{v_O(s)}{v_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$\frac{v_O(s)}{v_1(s)}$ TRANSFER FUNCTION
	Low Pass	$\frac{1\,4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	High Pass	$\frac{1\,4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	Band Pass	$\frac{1\,4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\,s + 1/LC}\right]$
	Band Reject	$\frac{1\,4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE
In the networks above the R value used is assumed to include 2 r_e or approximately 30 Ohms



Interface/Comparator Selector Guide

Microprocessor Bus

This family of devices is designed to extend the limited drive capabilities of today's standard 6800 and 8080 type NMOS microprocessors. All devices are fabricated with Schottky TTL technology for high speed.

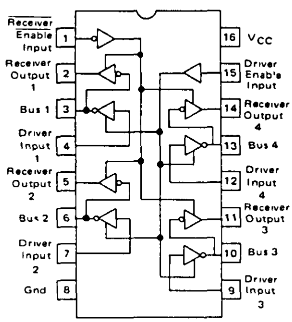
General features include:

- Single +5.0 V Power Supply Requirement
- Three-State Logic Output
- Low Input Loading – 200 μA Max.

DATA BUS EXTENDERS

Quad, Bidirectional, with 3-State Outputs

MC6880A/MC8T26A# – Inverting

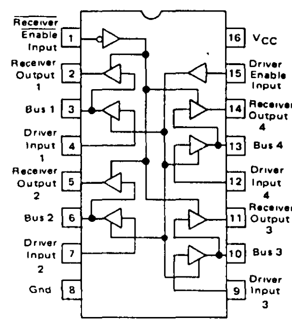


#These devices may be ordered by either of the paired numbers

Both types
T_A = 0 to 75°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

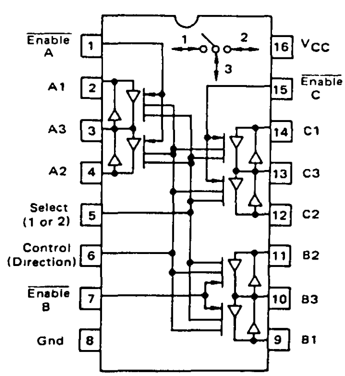
MC6889/MC8T28# – Non-inverting



Device Number	Input Current I_{IH} μA Max	I_{IL} μA Max	I_{OHL} Output Disabled Leakage Current – High Logic State μA Max	t_{PLH}, t_{PHL} Propagation Delay Time – High to Low or Low to High ns Max
MC6880A/MC8T26A	25	-200	100	14
MC6889/MC8T28	25	-200	100	17

BIDIRECTIONAL BUS SWITCH

MC6881/MC3449# – For exchanging TTL level digital information between selected pairs of ports in a 3-port network.



#This device may be ordered by either of the numbers.

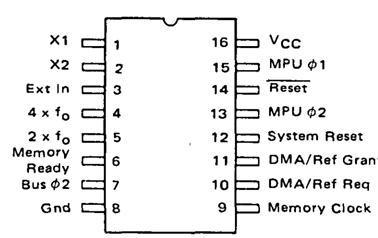
Both types:
T_A = 0 to 70°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

V_{OL} @ I_{OL} = 8.0 mA Volts Max	I_{OD} @ V_O = 2.7 V μA Max	I_{IL} @ V_{IL} = 0.4 V μA Max	I_{IH} @ V_{IH} = 2.7 V μA Max
0.5	25	-200	40

M6800 CLOCK GENERATOR

MC6875 – Provides the non-overlapping two-phase clock signals for M6800 MPU systems.



V_{OLC} = 0.3 V Max
V_{OHC} = V_{CC} – 0.3 V Min
f_{op} = 2.0 MHz Typ

MC6881/MC3449 TRUTH TABLE

Enable	Select	Control	Data Flow
0	0	0	2→3
0	0	1	3→2
0	1	0	1→3
0	1	1	3→1
1	X	X	High Impedance

X - Don't Care

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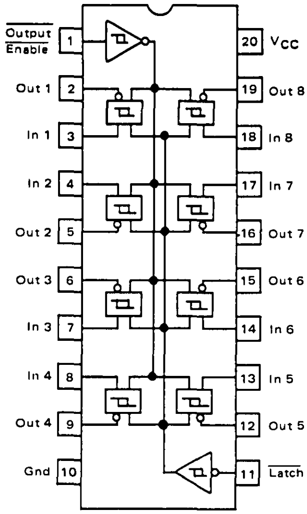
ADDRESS AND CONTROL BUS EXTENDERS

Octal, Buffer/Latch Unidirectional with 3-State Outputs

MC6882A/MC3482A# – Inverting



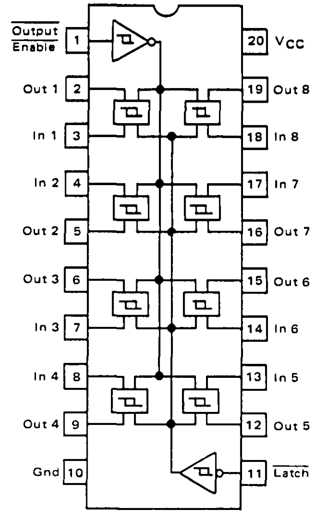
Output Enable	Latch	Input	Output
0	1	0	1
0	1	1	0
0	0	X	Q_0
1	X	X	Z

#These devices may be ordered by either of the paired numbers.

All types:
T_A = 0 to 75°C

Packages:
L Suffix – Case 732
P Suffix – Case 738

MC6882B/MC3482B# – Non-inverting

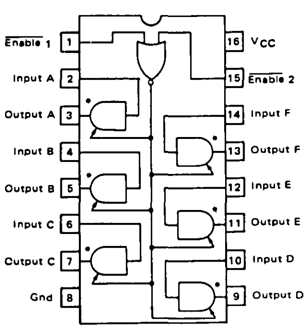


Output Enable	Latch	Input	Output
0	1	0	0
0	1	1	1
0	0	X	Q_0
1	X	X	Z

Device Number	V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OH} @ I_{OH} = –5.2 mA Volts Min	I_{OS} mA Typ	t_{PHL} ns Typ
MC6882A/MC3482A	0.5	2.4	–80	8.0
MC6882B/MC3482B	0.5	2.4	–80	10

Hex, Unidirectional, with 3-State Outputs

MC6885/MC8T95# – Non-inverting
MC6886/MC8T96# – Inverting
Two-input Enable controls all six buffers.

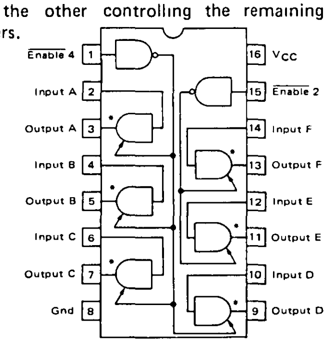


•Add inverter for MC6886/MC8T96.

All four types:
T_A = 0 to 75°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

MC6887/MC8T97# – Non-inverting
MC6888/MC8T98# – Inverting
Two Enable inputs, one controlling four buffers and the other controlling the remaining two buffers.

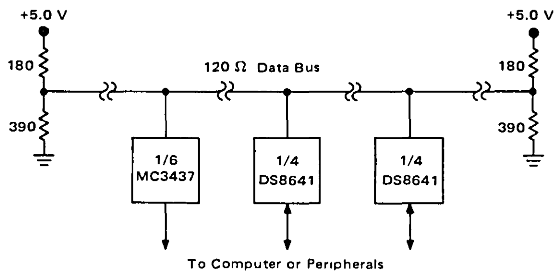


•Add inverter for MC6888/MC8T98.

V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OH} @ I_{OH} = –5.2 mA Volts Min	I_{OS} mA Typ	t_{PLH} ns Typ	$t_{P(Enable)}$ ns Typ
0.5	2.4	–80	6.0	11

Minicomputer Bus

Transceivers and receivers for bus organized minicomputers employing 120-ohm terminated lines.



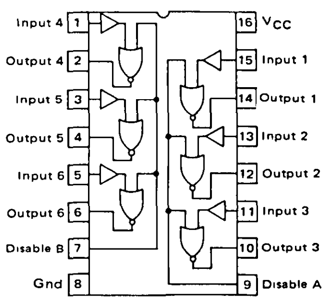
All three devices:
T_A = 0 to 70°C

Packages:

MC3437	
MC3438	DS8641
L Suffix — Case 620 — J Suffix	
P Suffix — Case 648 — N Suffix	

HEX RECEIVERS

MC3437 — Hysteresis-equipped for improved noise immunity. DS8837 equivalent.

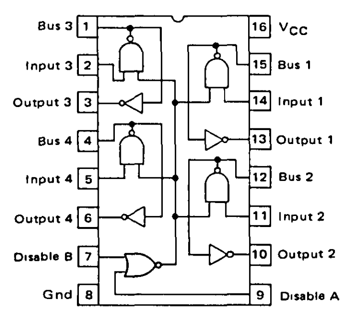


$I_{I(R)}$ @ $V_{I(R)}$ = 4.0 V µA Max	Hysteresis Volts Min	$t_{PLH(R)}$ @ C_L = 15 pF ns Max
50	0 5	30

QUAD TRANSCEIVERS

DS8641-MC3438

Open collector driver outputs allow wire-OR connection. MC3438 has hysteresis-equipped receiver for improved noise immunity (not available with DS8641). MC3438 is equivalent to the DS8838.



Receiver Hysteresis Volts Min	$V_{L(BUS)}$ @ I_{BUS} = 50 mA Volts Max	I_{BUS} @ $V_{IH(BUS)}$ = 4.0 V µA Max	$t_{PLH(D)}$ @ C_L = 15 pF ns Max	$t_{PLH(R)}$ @ C_L = 15 pF ns Max
0 25*	0 7	100	25	30

*MC3438 only.

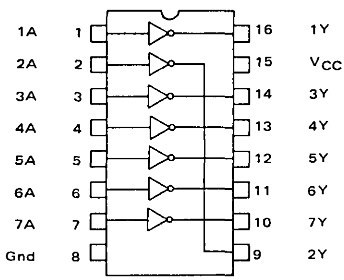
Computer Bus

NEW IBM 360/370 I/O INTERFACE

Line Receivers and Drivers designed to operate compatibly. The MC75125/MC75127 Seven-Channel Receivers, MC75128/MC75129 Eight-Channel Receivers, and the MC3481/MC3485 Drivers meet the new IBM System 360/370 I/O standard requirements.

SEVEN-CHANNEL LINE RECEIVERS

MC75125

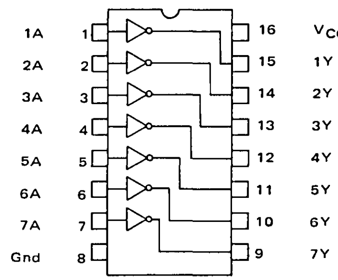


Logic: $Y = \overline{A}$

All types:
T_A = 0 to 70°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

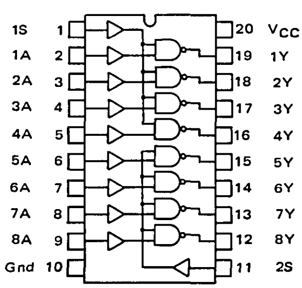
MC75127 – Standard V_{CC} and Ground Pinouts.



Logic: $Y = \overline{A}$

EIGHT-CHANNEL LINE RECEIVERS
(To be introduced)

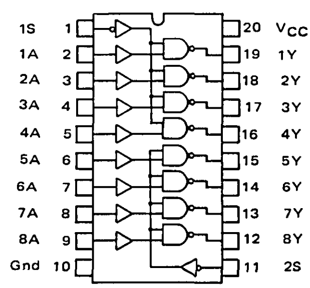
MC75128 – Active-High Strobe



Packages:
L Suffix – Case 732
P Suffix – Case 738

positive logic: Y = AS

MC75129 – Active-Low Strobe



Device Number	Input Resistance kΩ Min/Max	$I_{IH(R)}$ @ V_{IH} = 3.11 V mA Max	t_{PLH} @ C_L = 50 pF ns Max
MC75125/75127	7.4/20	0.42	25
MC75128/75129	7.4/20	0.42	25

7

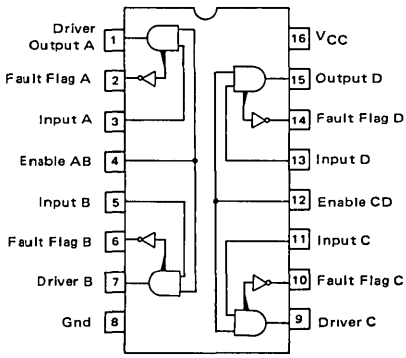
New IBM 360/370 I/O Interface (continued)

QUAD LINE DRIVERS
(To be introduced)

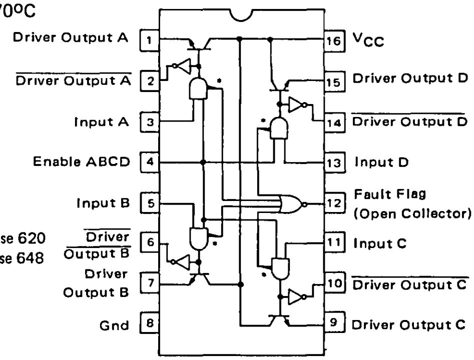
MC3481 – Open emitter driver with individual fault flags.

MC3485 – Open emitter driver with combined open collector fault flag and inverted outputs.

Both types:
T_A = 0 to 70°C



Packages:
L Suffix – Case 620
P Suffix – Case 648



Device Number	V_{OH} @ I_{OH} = −59.3 mA Volts Max	I_{OS}* @ V_O = 0 mA Max	t_{PLH} @ C_L = 100 pF ns Typ
MC3481/3485	3.11	0.0	25

*Fault Protection

GENERAL-PURPOSE I/O INTERFACE

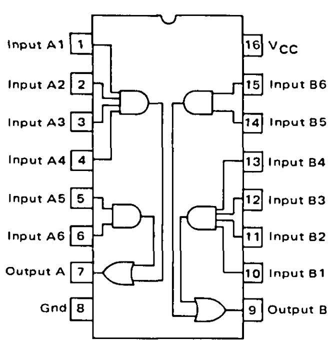
Line drivers and receivers designed to operate compatibly. The MC8T13/MC8T14 combination is specified for general TTL system applications. The MC8T23/MC8T24 combination is oriented toward older IBM 360/370 system requirements.

DUAL LINE DRIVERS

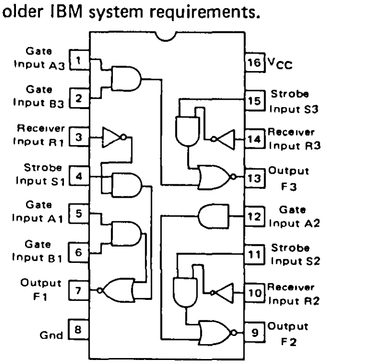
MC8T13 – Open emitter driver; specified for general TTL systems.
MC8T23 – Open emitter driver; specified to meet older IBM system requirements.

TRIPLE LINE RECEIVERS

MC8T14 – Hysteresis-equipped receiver; specified for general TTL systems.
MC8T24 – Hysteresis-equipped receiver; specified to meet older IBM system requirements.



All four devices.
T_A = 0 to 75°C
Packages
L Suffix – Case 620
P Suffix – Case 648



Device Number	V_{OH} @ I_{OH} = −75 mA @ I_{OH} = −59.3 mA* Volts Max	I_{OS} @ V_O = 0 mA Max	t_{PLH} @ C_L = 15 pF ns Max
MC8T13	2.4	−30	20
MC8T23	3.11*	−30	20

Device Number	$V_{H(R)}$ Volts Min	$I_{IH(R)}$ @ $V_{IH(R)}$ = 3.8 V @ $V_{IH(R)}$ = 3.11 V* mA Max	$t_{PLH(R)}$ @ C_L = 15 pF ns Max
MC8T14	0.3	0.17	30
MC8T24	0.2	0.17*	30

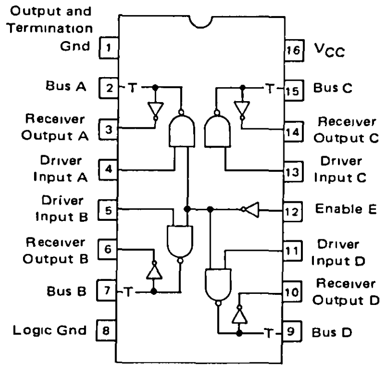
7

Instrumentation Bus

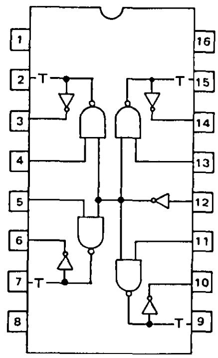
QUAD INTERFACE TRANSCEIVERS

These devices are designed to meet the GPIB bus specification of IEEE Standard 488-1978, for the interconnection of Measurement Apparatus.

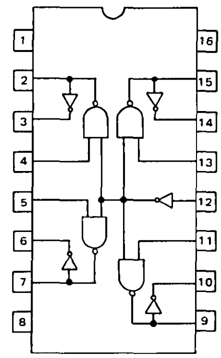
MC3440AP — Three drivers with common Enable input; one driver without Enable.



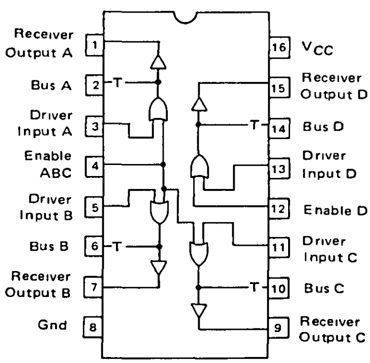
MC3441AP — Four drivers with common Enable input.



MC3443P — Four drivers with common Enable input; no termination resistors.



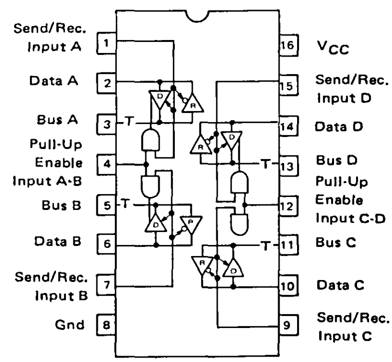
MC3446AP — For low-power instruments, including MOS.

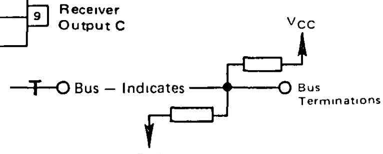


Packages
L Suffix — Case 620
P Suffix — Case 648

All types.
$T_A = 0$ to $70^{\circ}C$

MC3448A — For common Send-Receive bus; bidirectional.





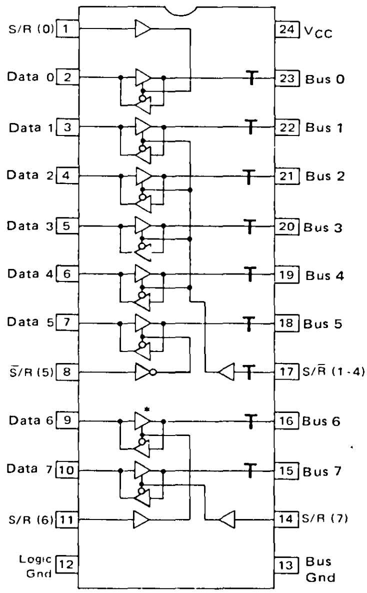
Device Number	Receiver Input Hysteresis mV Min	Drive Output Voltage @ I_{OL} = 48 mA; Volts Max	t_{PHL} (Driver or Receiver) ns Max
MC3440AP	400	0.5	30
MC3441AP	400	0.5	30
MC3443P	400	0.4	25(D) 22 (R)
MC3446AP	400	0.5	50 (D) 40 (R)
MC3448A	400	0.5	17 (D) 23 (R)

Instrumentation Bus (continued)

OCTAL LOW-POWER INTERFACE TRANSCEIVER

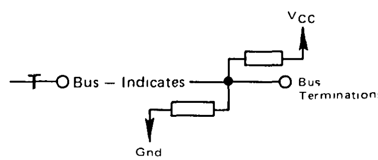
These devices are designed to meet the GPIB bus specifications of IEEE Standard 488-1978, for the interconnection of Measurement Apparatus.

MC3447 — Open collector, 3-State outputs with terminations.



All types.
T_A = 0 to 70°C

Packages.
L Suffix — Case 623
P3 Suffix — Case 724 (Narrow)



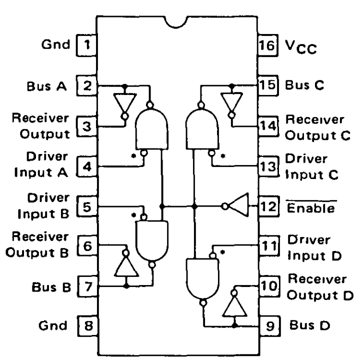
Device Number	Receiver Input Hysteresis mV Min	Drive Output Voltage @ I_{OL} = 48 mA; Volts Max	t_{PHL} (Driver or Receiver) ns Max
MC3447	400	0 5	30 (D) 22 (R)*

*Fast Channel.

HIGH-CURRENT PARTY-LINE BUS TRANSCEIVERS

Devices for industrial control and data communication.

MC26S10 — Inverting
MC26S11 — Non-inverting
Quad transceivers with open-collector drivers and PNP-buffered inputs for MOS compatibility.



*Inverter on MC26S11 only.

Packages:
L Suffix — Case 620
P Suffix — Case 648

Test	Condition	Limits
V_{OL} (D)	I_{OL} = 100 mA	0.8 Volts Max
I_O (D)	V_{OH} = 4.5 V	100 μA Max
I_{O1}(D)	V_{CC} = 0 V, V_{OH} = 4.5 V	100 μA Max
I_{IH} (D)	V_{IH} = 2.7 V	30 μA Max
I_{IL} (D)	V_{IL} = 0.4 V	-0.54 mA Max
t_P (D)	MC26S10 MC26S11	15 ns Max 19 ns Max
t_P (R)	Both Types	15 ns Max

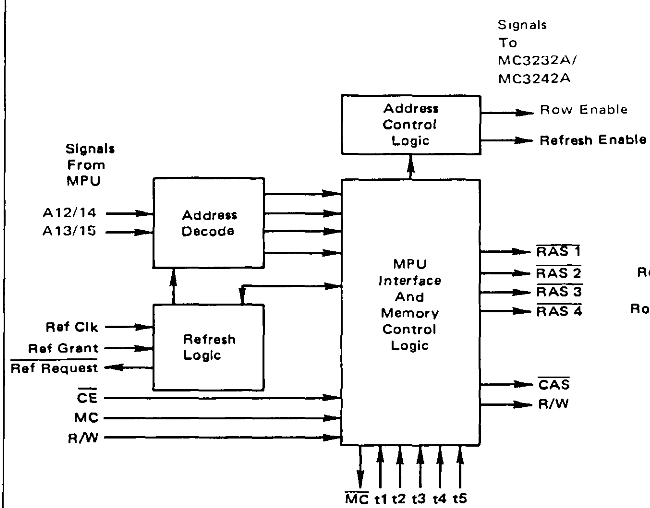
NMOS Memories to TTL Systems

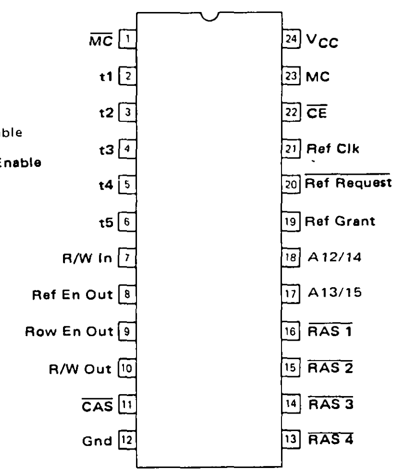
MULTIPLEXED 16-PIN RAM CONTROL
(For 4K, 16K, and 64K Dynamic Memories)

MC3480 – Memory Controller. Used with all three levels of RAM.

The memory controller chip is designed to greatly simplify the interface logic required to control popular 16-pin 4K, 16K, or 64K dynamic NMOS RAMs in a microprocessor system such as the M6800. The controller will generate, on command from the microprocessor, the proper $\overline{RAS}$ and timing signals required to successfully transfer data between the microprocessor and the NMOS memories. The controller, in conjunction with an oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

With Schottky TTL technology for high performance, and high input impedance for minimum loading of the MPU bus, the MC3480 reduces package count, and reduces system access/cycle times by 30%. The chip enable allows expansion to larger-word capacity.





T_A = 0 to 70°C

Packages:
L Suffix – Case 623
P Suffix – Case 649

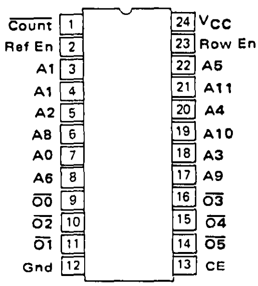
Designed to interface directly with MC3232A or MC3242A address/multiplexers/refresh counters.

NMOS Memories to TTL Systems (continued)
Multiplexed 16-Pin RAM Control (continued)
(For 4K, 16K, and 64K Dynamic Memories)

MC3232A – 6-Bit (4K RAM) Address Multiplexer/Refresh Counter
MC3242A – 7-Bit (16K RAM) Address Multiplexer/Refresh Counter
MC3482A/B – 8-Bit Address Multiplexer (See Microprocessor Bus Section)

MC3232A – Designed for multiplexing 12 address lines into 6 for the 16-pin multiplexed 4K RAMs, while also containing a 6-bit refresh counter.

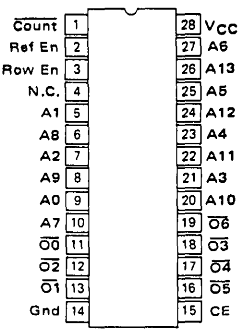
MC3242A – Designed for multiplexing 14 address lines into 7 for the 16-pin multiplexed 16K RAMs, while also containing a 7-bit refresh counter.

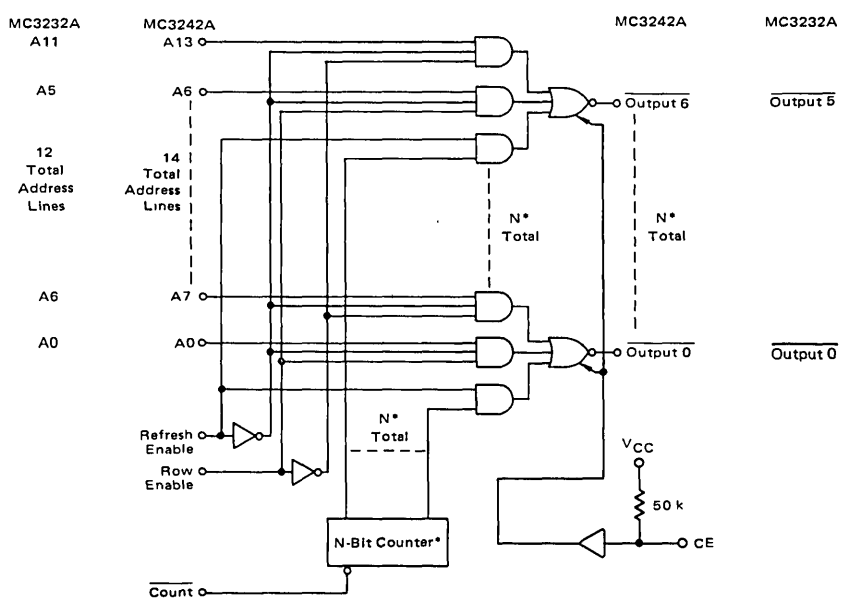


Both types:
T_A = 0 to 75°C

Packages:
MC3232A – L Suffix – Case 623
P Suffix – Case 649

MC3242A – L Suffix – Case 733
P Suffix – Case 710





*N = 6-Bit for MC3232A
= 7-Bit for MC3242A

NMOS Memories to TTL Systems (continued)

BUS EXTENSION
(See Microprocessor Bus)

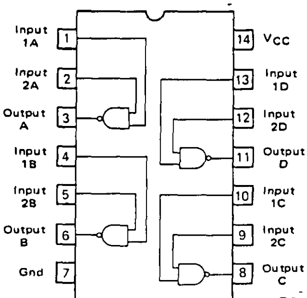
Data Bus (Bidirectional) Extenders
- MC6880A/MC8T26A – Inverting
- MC6889/MC8T28A – Non-inverting

Address Bus (Unidirectional) Extenders
- MC6885/MC8T95 – Hex Non-inverting
- MC6886/MC8T96 – Hex Inverting
- MC6887/MC8T97 – Hex Non-inverting
- MC6888/MC8T98 – Hex Inverting
- MC6882A/MC3482A – Octal Inverting
- MC6882B/MC3482B – Octal Non-inverting

Bus Switches
- MC3449 – Triple Bidirectional

DATA AND ADDRESS LINE DRIVERS
(Low Level)

MC3459 – Quad Address Line Driver



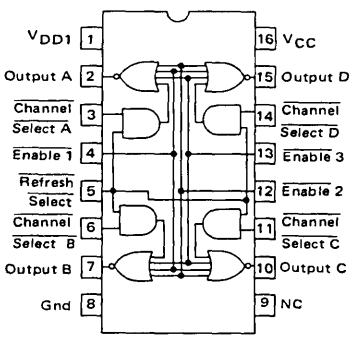
T_A = 0 to 70°C

Packages:
- L Suffix – Case 632
- P Suffix – Case 646

Device Number	V_{OH} Volts Min	@ I_{OH} mA	V_{OL} Volts Max	@ I_{OL} mA	Propagation Delay ns Max	@ C_L pF	Features
MC3459	2.4	–2.0	0.7	80	26	360	High fan-out capability

CLOCK AND CHIP ENABLE LINE DRIVERS
(High Level)

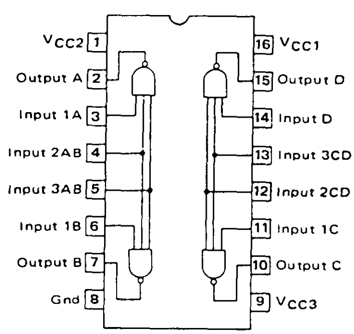
MC3245 – Quad Clock Drivers with Refresh Select Logic



T_A = 0 to 70°C

Packages:
- L Suffix – Case 620
- P Suffix – Case 648

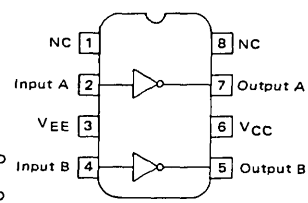
MC75365 – Quad Clock Driver or High-Current NAND Gate



T_A = 0 to 70°C

Packages:
- L Suffix – Case 620
- P Suffix – Case 648

MMH0026 / MMH0026C – Dual Clock Driver



(Pin Connections for U or P1 Package)

T_A:
- MMH0026 – –55 to 125°C
- MMH0026C – 0 to 70°C

Packages
- G Suffix – Case 601
- L Suffix – Case 632
- U Suffix – Case 693
- P1 Suffix – Case 626 (For MMH0026C only)

Device Number	V_{OH} Volts Min	@ I_{OH} mA	V_{OL} Volts Max	@ I_{OL} mA	t_{DHL} ns Max	@ C_L pF	Feature
MC3245	V_{DD} – 0 5	–1.0	0 45	5 0	32	250	Does not require second high voltage supply. Low input loading.
MC75365	V_{CC2} – 0.3	–0.1	0 3	10	18	200	Derives V_{CC1} power from TTL 5-V supply, and V_{CC2} and V_{CC3} from V_{SS} and V_{BB} supplies from NMOS memories.
MMH0026 MMH0026C	V_C – 1.0	0.4 V*	V_{EE} + 1.0	2 4 V*	12	1000	For very high capacitance loads.

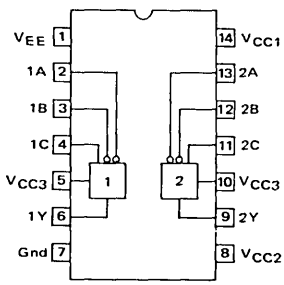
*@ V_I – V_{EE}

NMOS Memories to MECL Systems

DRIVER/TRANSLATORS

MECL-to-MOS driver/translators convert standard MECL 10,000 input signals to suitable levels for NMOS memory systems. The MC75368 may also be used as positive logic NOR or non-inverting gates.

MC75368 – Dual Clock Line Drivers suitable for driving address, control, and timing inputs.



Maximum Supply Voltage:
MC75368 = 18 V

T_A = 0 to 70°C

Packages.
L Suffix – Case 632
P Suffix – Case 646

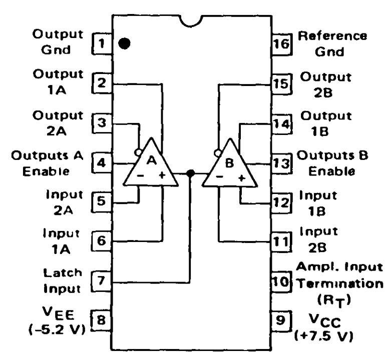
Device Number	V_{OH} Volts Min	@	I_{OH} mA	V_{OL} Volts Max	@	I_{OL} mA	t_{DHL} ns Max	@	C_L pF
MC75368	V_{CC2} - 0.3		0.1	0.3		10	26		300

SENSE AMPLIFIER

MC3461L – Dual Sense Amplifier with MECL 10,000-compatible control inputs and complementary, open-emitter outputs. Designed for 7001 and 2105 type NMOS 1K RAMs.

I_{TH} µA Max	t_{PD} (Amplifier) ns Max	t_{PD} (Enable) ns Max
±200	10	5.0

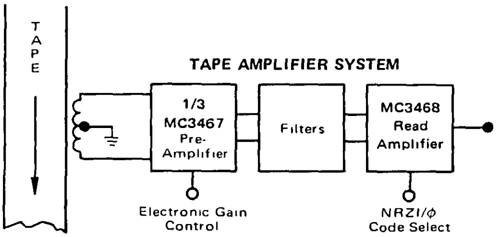
T_A = 0 to 75°C
Package:
Case 620



Magnetic Memories to TTL Systems

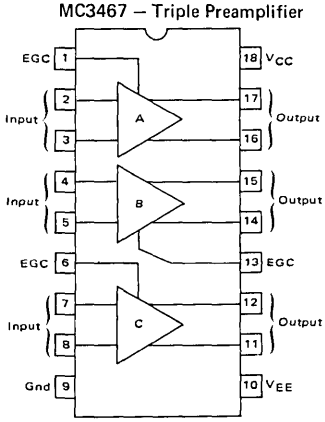
SENSE AMPLIFIERS

. . . for Magnetic Tape Memories

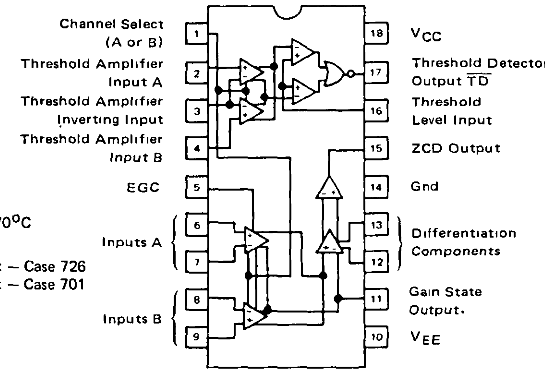


A two-component preamplifier/amplifier combination that provides the interface between magnetic tape heads and digital logic. Suitable for both open reel and cartridge tape systems. Triple preamp has individually adjustable gain controls. LSI Read Amplifier performs peak detection and threshold detection functions, as required for NRZI/phase encoded recording formats.

MC3467 – Triple Preamplifier



MC3468 – Read Amplifier

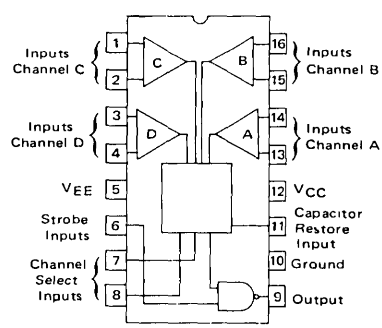


Both types:
T_A = 0 to 70°C
Packages.
L Suffix – Case 726
P Suffix – Case 701

. . . for Plated Wire and Thin-Film Memories
and other low-level sensing applications.

MC1544 – T_A = -55 to 125°C
MC1444 – T_A = 0 to 70°C

Features 4-channel input with decoded channel selection and strobed output capability.



Packages·
MC1544/MC1444
L Suffix – Case 620

Device Number	V_{TH} mV	V_{OH} @ I_{OH} = -400 µA Volts Min	V_{OL} @ I_{OL} = 10 mA Volts Max	t_{PD} ns Max
MC1544	0.5 to 1.5	2.4	0.5	25
MC1444	0.3 to 2.3	2.4	0.5	25

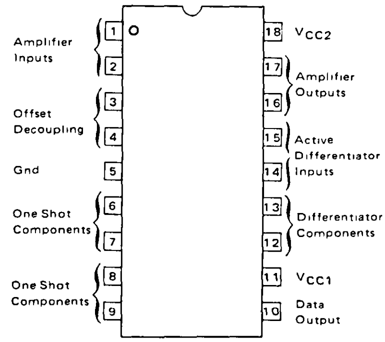
7

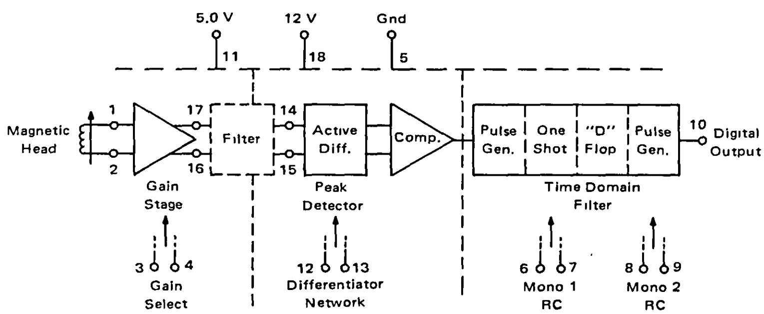
Magnetic Memories to TTL Systems (continued)

FLOPPY DISK READ AMPLIFIER SYSTEM

MC3470 – Designed as a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output. It combines all the active circuitry to perform the floppy disk READ amplifier function in one circuit, and is guaranteed to have a maximum peak shift of 5.0%, adjustable to zero.

T_A = 0 to 70°C
Package.
P Suffix – Case 701

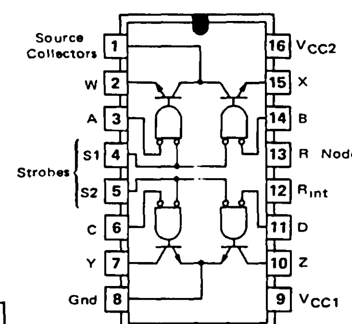




CORE DRIVER

MC55325 – T_A = -55 to 125°C
MC75325 – T_A = 0 to 70°C
Contains two source switches and two sink switches. Source and sink selection is determined by one of two logic inputs, and turn-on is determined by the appropriate strobe.

Packages.
L Suffix – Case 620
P Suffix – Case 648 (MC75325 only)



Device Number	V_{sat} @ I_{sink} or I_{source} = 600 mA Volts Max	I_{off} @ V_{CC2} = 24 V µA Max	t_{PLH} (Source) ns Max	t_{PLH} (Sink) ns Max
MC55325	0.70	150	50	45
MC75325	0.75	200	50	45

7

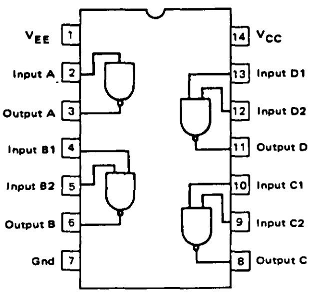
LINE DRIVERS AND RECEIVERS for Modem/Terminal Applications

Voltage Mode

RS-232C SPECIFICATION

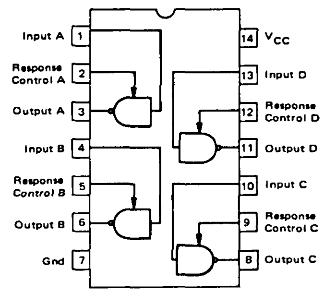
DRIVER

MC1488 – Quad; output current limiting.



RECEIVERS

MC1489 – Quad; 0.25 V input hysteresis.
MC1489A – Quad; 1.1 V input hysteresis.



All devices:
T_A = 0 to 70°C
Package:
L Suffix – Case 632

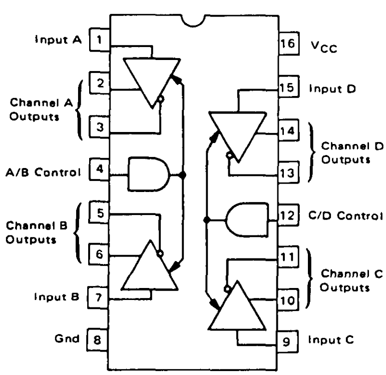
V_{OH} @ V_{CC}/V_{EE} = ±9.0 V Volts Min	V_{OL} @ V_{CC}/V_{EE} = ±9.0 V Volts Max	I_{OS} mA	t_{PHL} @ C_L = 15 pF ns Max
6.0	-6.0	±6.0 to 12	175

Device Number	Input V_{IHL} Volts	Input V_{ILH} Volts	t_{PHL} @ R_L = 390 Ω ns Max
MC1489	1.0 to 1.5	0.75 to 1.25	50
MC1489A	1.75 to 2.25	0.75 to 1.25	50

RS-422/423 SPECIFICATION

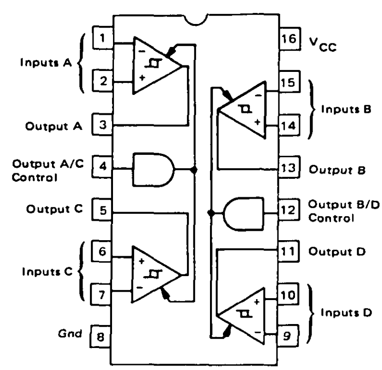
DRIVER

MC3487 – Quad; three-state outputs.



RECEIVER

MC3486 – Quad; three-state outputs and input hysteresis.



Both devices:
T_A = 0 to 70°C
Packages:
L Suffix – Case 620
P Suffix – Case 648

V_{OH} @ I_{OH} = 50 mA Volts Min	V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OD} (Differential) @ R_L = 100 Ω Volts Min	t_{PLH}/t_{PHL} ns Typ
2.0	0.5	2.0	15

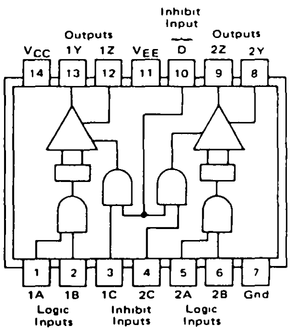
$V_{TH(D)}$ @ V_{ICM} = ±7.0 V Volts Max	I_{ID} @ V_{ID} = ±10 V V_{CC} = 0 to 5.25 V mA Max	t_{PHL}/t_{PLH} ns Typ	$t_{P(Control)}$ ns Typ
±0.2	±3.25	20/25	25

Line Drivers and Receivers for Modem/Terminal Applications (continued)

Differential Current Mode

DRIVERS

MC75S110 – Dual; industry standard.

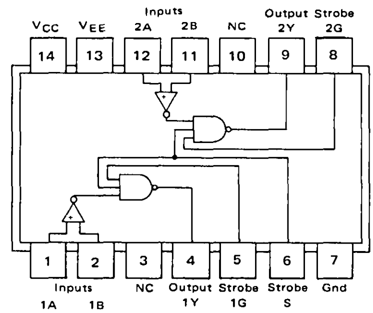


T_A = 0 to 70°C (MC75xxx)
-55 to 125°C (MC55xxx)

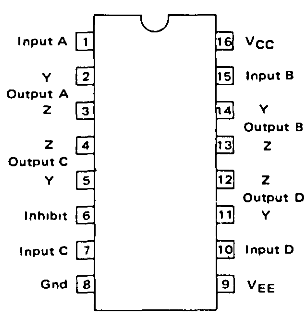
Packages:
L Suffix – Case 632
P Suffix – Case 646 (MC75xxx only)

RECEIVERS

MC75107/MC55107 – Dual; active pullup output.
MC75108/MC55108 – Dual; open collector output.



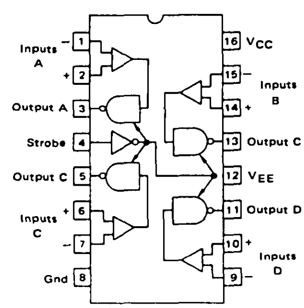
MC3453 – Quad; common inhibit input; current sink approximately 12 mA.



All three devices:
T_A = 0 to 70°C
Packages:
L Suffix – Case 620
P Suffix – Case 648

MC3450 – Quad; active pullup outputs; common three-state enable.

MC3452 – Quad; open collector outputs.



BOTH DRIVERS

I_O (on) mA Min	I_O (off) µA Max	t_{PHL} ns Max
6.5	100	15

ALL RECEIVERS

Input V_{TH} mV Max	I_{IH} @ V_{ID} = 0.5 V µA Max	I_{IL} @ V_{ID} = -2.0 V µA Max	t_{PLH} ns Max
±25	75	-10	25

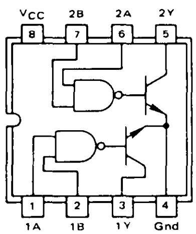
7

Dual Drivers

. . . for relays, lamps, and other peripherals requiring more power than generally available from logic gates.

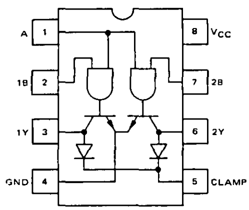
Representative Diagrams

MC754xx Series



(MC75451/MC75461)

MC147x Series



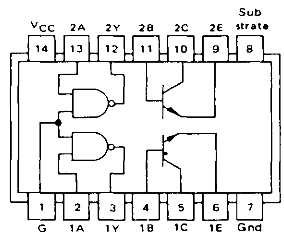
(MC1472)

Logic gates vary to provide output shown

Logic Output (Including Transistor Inversion)	BV_{CER}			
	30 V	30 V	35 V	70 V Hi-Z Input
AND	MC75451	SN75451B*	MC75461	
NAND	MC75452	SN75452B*	MC75462	MC1472
OR	MC75453	SN75453B*	MC75463	
NOR	MC75454	SN75454B*	MC75464	

*Same as equivalent MC types, but with guaranteed switching limits.

MC75450 — Similar to MC75451, but with uncommitted output transistors.



All Devices
T_A = 0 to 70°C

Packaging:
- MC75450
  - L Suffix — Case 632
  - P Suffix — Case 646
- MC75451–54/MC75461–64
  - P Suffix — Case 626
  - U Suffix — Case 693
- MC1472
  - P1 Suffix — Case 626
  - U Suffix — Case 693

Driver Arrays

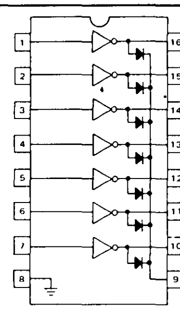
. . . Seven Darlington transistors with output clamp diodes.

Device Number	Application	Input Element
MC1411	General Purpose	Basic
MC1412	14–25 V PMOS	Zener and Series 10.5 kΩ resistor
MC1413	5 V CMOS or TTL	Series 2.7 kΩ resistor
MC1416	8–18 V MOS	Series 10.5 kΩ resistor

All Types:
V_{Max} = 50 V
I_{Max} = 500 mA

T_A = 0 to 85°C

Packages:
- L Suffix — Case 620
- P Suffix — Case 648

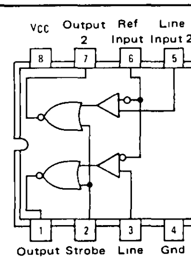


Dual Receiver

MC75140P1 — Dual single-ended receiver with common strobe and reference inputs for maximizing noise immunity. Useful for bus-organized (party line) TTL systems.

V_{TH}	V_{Ref}	$t_{PLH(L)}$
±100 V	1.5 to 3.5 V	35 ns

T_A = 0 to 70°C
Package — Case 626



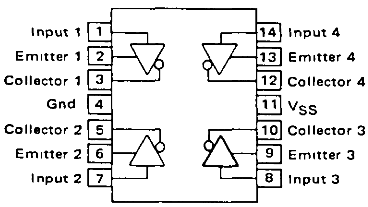
7

NUMERIC DISPLAY INTERFACE

. . . for mating multiplexed LED or gas discharge numeric displays to MOS or TTL logic systems.

LED Drivers for Common-Cathode Displays

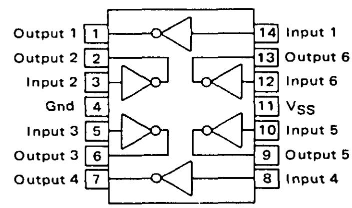
MC75491 – Quad segment driver



Both Devices:
T_A = 0 to 70°C

Packages:
L Suffix – Case 632
P Suffix – Case 646

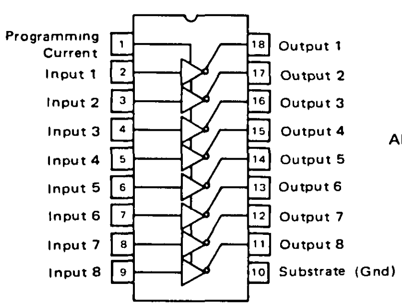
MC75492 – Hex digit driver



Device Number	I_I @ V_I = 10 V mA Max	V_{OL} Volts Max	@ I_{OL} mA	V_{SS} Volts Max
MC75491	3.3	1.2	250	10
MC75492	3.3	1.2	50	10

Gas Discharge Drivers

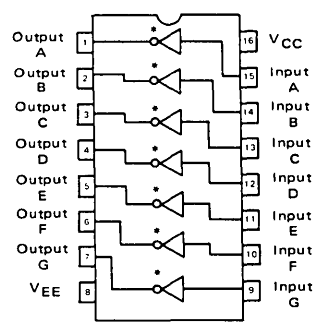
MC3491
MC3492 – Eight segment cathode drivers with programmable current.



All Devices:
T_A = 0 to 70°C

Package: P Suffix – Case 701

MC3490 – High Level
MC3494 – Low Level
Seven digit anode drivers



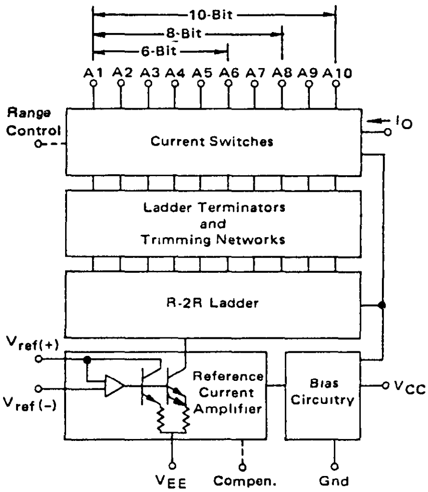
*Inverter on MC3494 only.
Package: P Suffix – Case 648

Device Number	Output ON Current mA Max	Breakdown Voltage Volts Min	Current Deviation (All 8 Outputs) % Max	Output Voltage Compliance Range Volts
MC3491	1.85	80	10	5.0 to 50
MC3492	5.25	80	10	5.0 to 50

Device Number	Breakdown Voltage Volts Min	Input Voltage (OFF-State) Volts	Input Voltage (ON-State) Volts	Input Current μA Max
MC3490	48	-5.0 Min	-2.0 Max	450
MC3494	48	-2.0 Max	-5.0 Min	-350

Low-cost building blocks for construction of D-A/A-D systems. Involves use of advanced technologies such as ion implantation, laser trimming and CMOS processing where necessary to achieve the required functional capability, operating accuracy and production repeatability.

D-A Converters — General Purpose



--- Dotted terminals available on 6- and 8-bit units only.

Multiplying D-A converters designed to supply an output current that is a linear product of an analog input reference voltage and a digital input word. Devices for 6-, 8- and 10-bit digital word inputs are available.

Device Number	Error % Max	P_D @ V_{EE} = -5 V mW Max	$t_{Settling}$ ns Typ	I_O @ V_{Ref} = 2 V mA	Suffix	Case
6-Bit						
MC1506*	±0.78	120	150	1.9 to 2.1	L	632
MC1406						
8-Bit						
MC1508L8*	±0.19	170	300	1.9 to 2.1	L	620
MC1408L8					L, P	620, 648
MC1408L7	±0.39					
MC1408L6	±0.78					
MC3408	±0.5				L	620
10-Bit						
MC3510*	±0.05	220	250	3.8 to 4.2	L	690
MC3410					L, P	690, 648
MC3410C	±0.1					

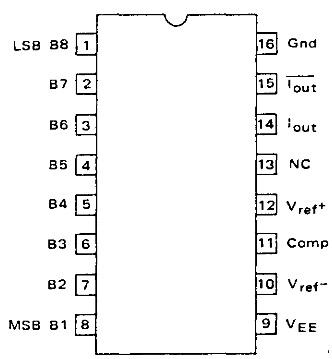
*T_A = -55 to 125°C,
Devices without asterisk T_A = 0 to 70°C.

D-A Converters — High Speed

MC10318 — A high speed 8-bit D/A converter capable of data conversion rates in excess of 25 MHz. It is intended for applications in high speed instrumentation and communication equipment, display processing, storage oscilloscopes, radar processing, and TV broadcast systems. The inputs are compatible with MECL 10,000 series logic, while the complementary current outputs have 51 mA full scale capability. 8-bit accurate (± 1/2 LSB) and monotonic over the full temperature range, the outputs typically settle in less than 15 ns.

T_A = 0 to 70°C

Packages:
L Suffix — Case 620/690

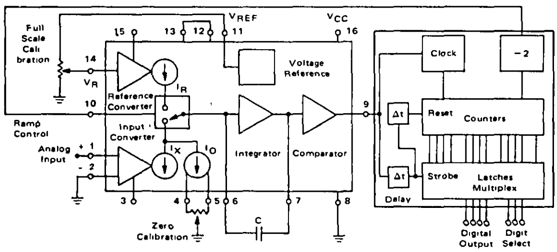


Device Number	Error % Max	P_D @ V_{EE} = -5.2 V mW Max	$t_{Settling}$ ns Typ	I_O & $\overline{I_O}$ @ V_{Ref} = 10.56 V mA Typ
MC10318L	±0.19	675	15	51
MC10318L9	±0.10	675	15	51

7

A-D Subsystems

2-Chip A-D Converter System Functional Diagram



MC1505/1405 — A-D Converter MC14435 — Digital Logic
(See CMOS Data Book for data.)

These devices are relatively complex subsystems. The bipolar, dual-ramp A-D converter has up to 4-1/2-digit conversion capability. The CMOS logic subsystem specifically adapts the A-D converter to a 3-1/2-digit DVM function.

MC1505L — T_A = -55 to 125°C — Case 620
MC1405L — T_A = 0 to 70°C — Case 620

Linearity Error % Max	Voltage Reference Volts	Temperature Coefficient of Reference %/°C	I_{CC} @ V_{CC} = 5.0 V mA Max
±0.05	1.15 to 1.35	0.005	12

MC14435EFL/EVL* — T_A = -55 to 125°C — Case 620
MC14435FL/VL* — T_A = -40 to 85°C — Case 620
MC14435FP/VP* — T_A = -40 to 85°C — Case 648

$P_{C(quiescent)}$ @ V_{DD} = 5.0 V mW Max	I_{OL} @ V_{DD} = 5.0 V (Digit Selects) mA Min	I_{OL} @ V_{DD} = 5.0 V (BCD Outputs) mA Min	I_{OL} @ V_{DD} = 5.0 V (All Outputs) mA Min
1.75	1.6	1.6	-0.2

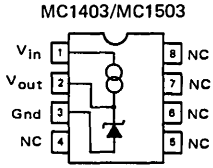
*MC14435EFL/FL/FP: V_{DD} = 3.0 to 18 Vdc
MC14435EVL/VL/VP: V_{DD} = 3.0 to 6.0 Vdc

VOLTAGE REFERENCES

Precision Low-Voltage References

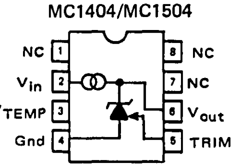
A family of precision low-voltage bandgap voltage reference, these devices are designed for applications requiring low temperature drift.

MC1403/MC1503



Packages:
U Suffix — Case 693

MC1404/MC1504



Low Temperature Drift, Low Voltage Reference

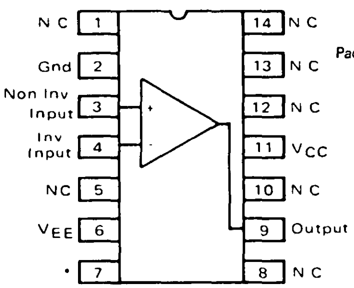
V_{out} Volts Typ	I_O mA Max	$\Delta V_{out}/\Delta T$ ppm/°C Max	Device Number	Reg_{line} 4.5< V_I ≤15 V/ 15 V< V_I ≤40 V mV Max	Reg_{line} V_{in} = V_{out}+ 2.5 V to 40 V mV Max	Reg_{load} 0.0 mA I_O<10 mA mV Max	T_A °C
2.5 ± 25 mv	10	40	MC1403	3.0/4.5	N/A	10	0 to +70
		25	MC1403A				
		55	MC1503				-55 to +125
		25	MC1503A				
5.0 ± 50 mV	10	40	MC1404U5	N/A	6.0	10	0 to +70
		25	MC1404AU5				
		55	MC1504U5				-55 to +125
		25	MC1504AU5				
6.25 ± 60 mV	10	40	MC1404U6	N/A	6.0	10	0 to +70
		25	MC1404AU6				
		55	MC1504U6				-55 to +125
		25	MC1504AU6				
10 ± 100 mV	10	40	MC1404U10	N/A	6.0	10	0 to +70
		25	MC1404AU10				
		55	MC1504U10				-55 to +125
		25	MC1504AU10				

7

General Purpose Comparators

. . . for detecting the polarity relationship between two analog levels and giving a corresponding TTL output.

MC1710 – T_A = -55 to 125°C
MC1710C – T_A = 0 to 70°C
Single comparators

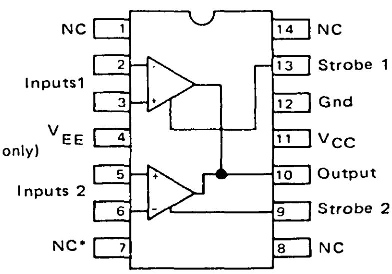


•Connected to pin 6 via the substrate on some plastic units.

Packages:
G Suffix – Case 601 (MC1710)
G Suffix – Case 603 (MC1711)
L Suffix – Case 632
P Suffix – Case 646 (for MC1710C, MC1711C only)

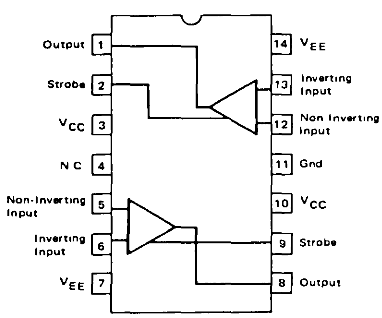
(Pin Connections for L or P Package)

MC1711 – T_A = -55 to 125°C
MC1711C – T_A = 0 to 70°C
Dual comparators with strobes and wire-ORed outputs



•Connected to pin 4 via the substrate on some plastic units.

MC1514 – T_A = -55 to 125°C
MC1414 – T_A = 0 to 70°C
Dual comparators with strobes.

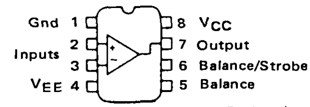


Packages:
L Suffix – Case 632
P Suffix – Case 646 (MC1414 only)

Device Number	V_{IO} mV Max	I_{IB} µA Max	A_{VOL} V/V Min
MC1710C	5.0	25	1000
MC1710	2.0	20	1250
MC1711C	5.0	100	700
MC1711	3.5	75	700
MC1514	2.0	20	1250
MC1414	5.0	25	1000

7

Precision Comparators



(Pin Connections for J-8 or N Package)

Packages:
- H Suffix – Case 601
- J-8 Suffix – Case 693
- J Suffix – Case 632
- N Suffix – Case 626 (LM311 only)

. . . featuring low input loading, high voltage gain, and a choice of either dual or single positive power supply operation.

LM111 – T_A = -55 to 125°C
LM211 – T_A = -25 to 85°C
LM311 – T_A = 0 to 70°C
Single comparators; high gain, high input impedance; strobe and balance inputs provided.

Device Number	V_{IO} mV Max	I_{IB} nA Max	V_{OL} @ I_{OL} = 50 mA Volts Max
LM111	3.0	100	1.5
LM211	3.0	100	1.5
LM311	7.5	250	1.5

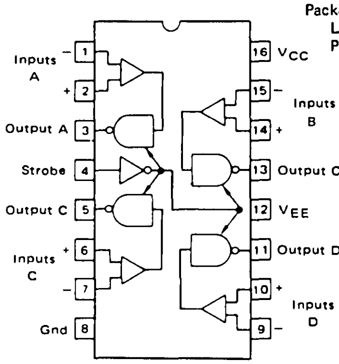
Quad Comparators . . . for applications requiring multiple comparators.

MC3430, MC3431 – High-speed quad comparators with three-state Enable common to all four devices; ±5 volt supply; T_A = 0 to 70°C.

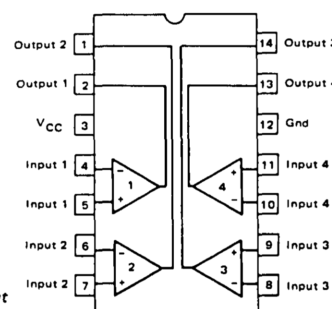
MC3432, MC3433 – Quad comparators with open collector outputs, common strobe input; ±5 volt supply; T_A = 0 to 70°C.

LM139, LM139A – T_A = -55 to 125°C
MC3302, LM2901, LM239, LM239A – T_A = -40 to 85°C
LM339, LM339A – T_A = 0 to 70°C

Single supply voltage comparators.



Packages:
- L Suffix – Case 620
- P Suffix – Case 648



Packages:
- J Suffix – Case 632
- N Suffix – Case 646 (For all devices *except* LM139, LM139A)

Device Number	V_{IS} mV Max	I_{IB} µA Max	t_{PHL} ns Max
MC3430	±6.0	20	45
MC3431	± 10	20	45
MC3432	±6.0	20	50
MC3433	± 10	20	50

Device Number	V_{IO} @ 25°C mV Max	I_{IB} @ 25°C nA Max	I_{sink} @ V_{OL} = 500 mV mA Min	V_{OL} @ I_{OL} = 2.0 mA* @ I_{OL} = 3.0 mA** @ I_{OL} = 4.0 mA mV Max
MC3302	20	1000	–	400*
LM2901	7 0	250	6 0	400**
LM139	5.0	100	6.0	500
LM139A	2.0	100	6.0	500
LM239	5.0	250	6.0	500
LM239A	2.0	250	6.0	500
LM339	5.0	250	6.0	500
LM339A	2.0	250	6.0	500

7

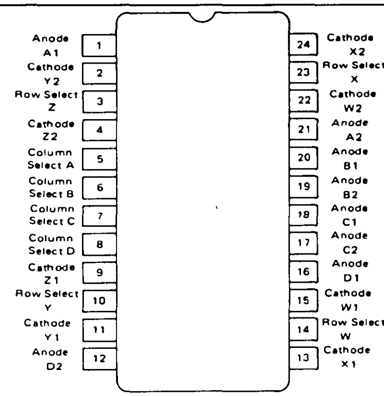
Crosspoint Switch

MC3416 — Low-cost solid-state crosspoint switch offers important advantages in modern telephone exchanges employing space-division switching. Features 4 x 4 two-wire monolithic structure for PABX applications. Select inputs are both CMOS and TTL compatible.

T_A = 0 to 70°C

Packages:
P Suffix — Case 649
L Suffix — Case 623

r_{off} @ V_{AK} = 10 V MΩ Min	r_{on} @ I_{AK} = 20 mA Ohms Max	BV_{AK} BV_{KA} Volts Min	V_{AK} @ I_{AK} = 20 mA Volts Max
100	10	25	1.1



Voice Encoding/ Decoding

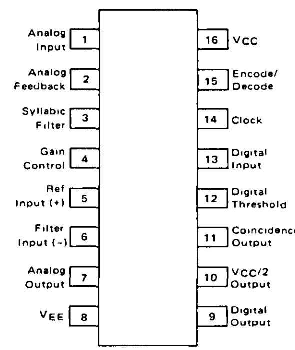
Simplified voice encoding/decoding using continuous Variable Slope Delta Modulator (CVSD) technique.

MC3417/MC3517 — 3-bit algorithm; for military secure communication and general-purpose low-sampling rate applications.

MC3418/MC3518 — 4-bit algorithm; telephone quality.

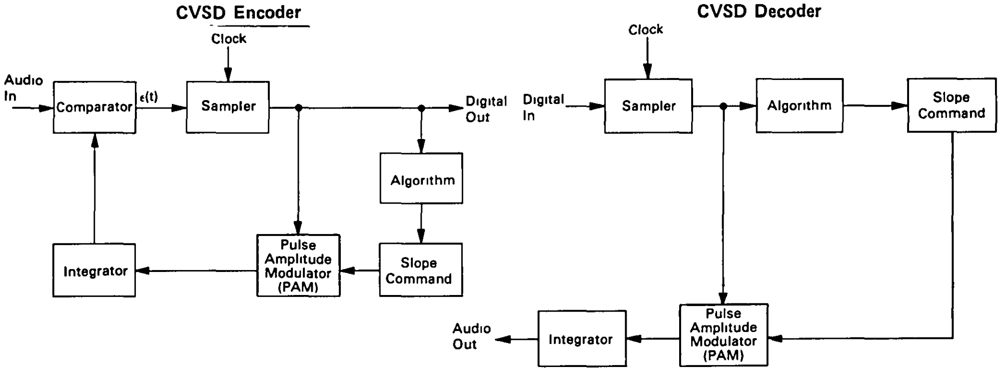
T_A = 0 to 70°C — MC3417/MC3418
= −55 to +125°C — MC3517/MC3518

Packages:
L Suffix — Case 620
P Suffix — Case 648



Device Number	Sample Rate Samples/s Typ	Total Loop Offset Voltage mV Max	t_{PD}, Clock Trigger to Output µs Max
MC3417/MC3517	16 k	±5.0	2.5
MC3418/MC3518	38 k	±2.0	2.5

CVSD Encoder　　　CVSD Decoder



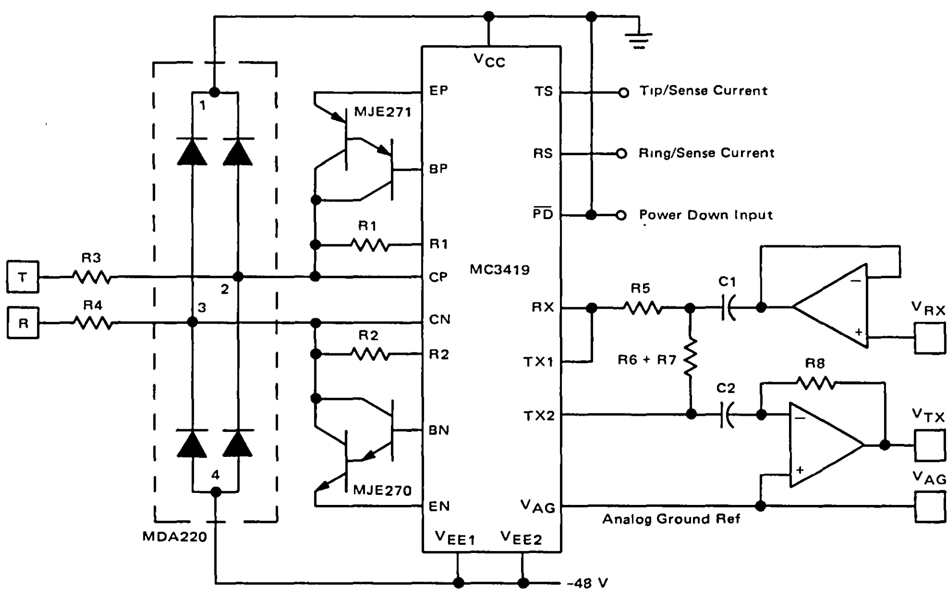
Digital Voice Channel

SUBSCRIBER LOOP INTERFACE CIRCUIT

MC3419/MC3519 — Designed to replace the hybrid transformer in Class 5, PBAX and Subscriber Carrier Equipment, this circuit provides signal separation for two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input. The transhybrid gain is externally selected and provides dc line current for powering the telset. It operates from up to a 60 V supply. On-hook power is below 5 mW and current sensing outputs are provided for off-hook status from both tip and ring leads. It offers size and weight reduction over present approaches and is compatible with IEEE and REA specifications.

T_A = 0 to 70°C – MC3419
= –40 to +85°C – MC3519

Packages:
L Suffix – Case 726
P Suffix – Case 701



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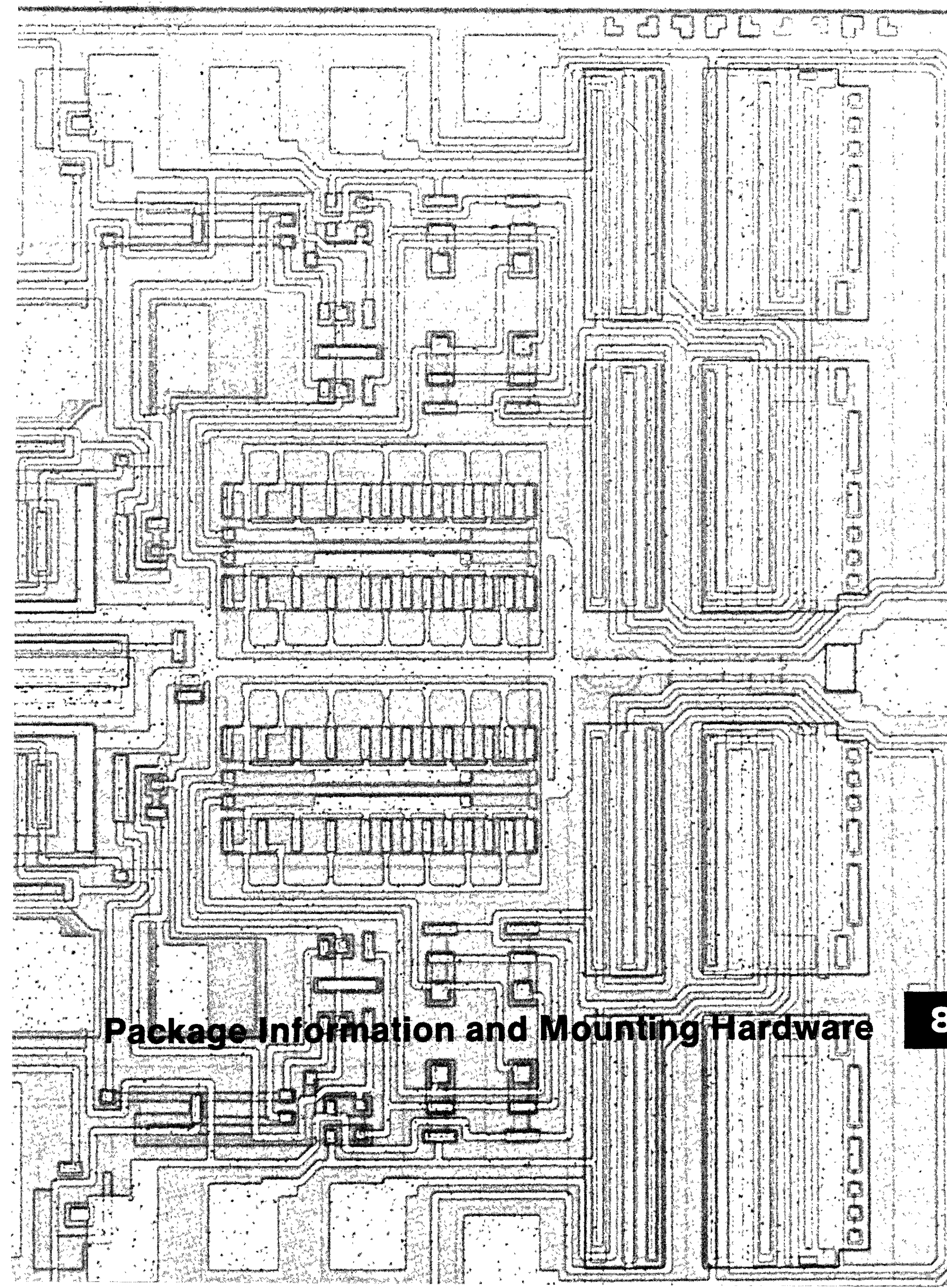


Package Information and Mounting Hardware

8

CASE OUTLINE DIMENSIONS

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.

T_A = Maximum Desired Operating Ambient Temperature

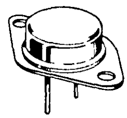
$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

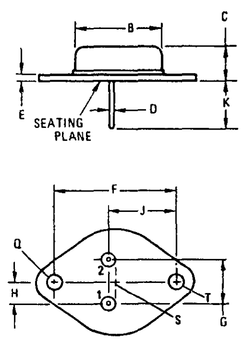
CASE 1 (TO-3)

Metal Package

$R_{\theta JA} = 45^{\circ}$ C/W(Typ)

$R_{\theta JC} = 5.5^{\circ}$ C/W(Typ)



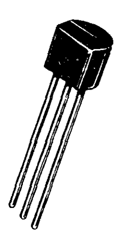


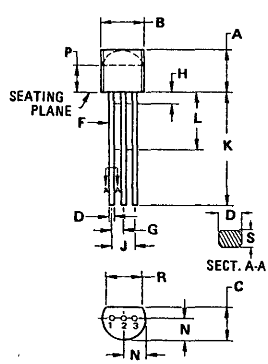
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22 23	–	0 875
C	6 35	11 43	0 250	0 450
D	0 97	1 09	0 038	0 043
E	–	3 43	–	0 135
F	29 90	30 40	1 177	1 197
G	10 67	11 18	0 420	0 440
H	5 21	5 72	0 205	0 225
J	16 64	17 15	0 655	0 675
K	7 92	—	0 312	–
Q	3 84	4 09	0 151	0 161
S	–	13 34	–	0 525
T	–	4 78	–	0 188

CASE 29 (TO-92)

Plastic Transistor

$R_{\theta JA} = 200^{\circ}$ C/W





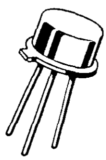
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4 32	5 33	0.170	0.210
B	4.44	5 21	0 175	0 205
C	3.18	4.19	0 125	0.165
D	0.41	0 56	0.016	0.022
F	0 41	0 48	0 016	0.019
G	1.14	1.40	0 045	0 055
H	–	2.54	–	0 100
J	2.41	2 67	0 095	0 105
K	12.70	–	0.500	–
L	6 35	–	0 250	–
N	2.03	2.92	0 080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0 36	0.41	0 014	0 016

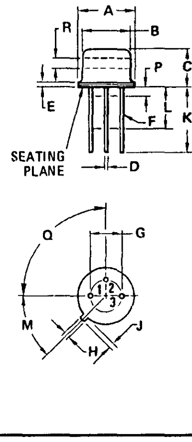
8

CASE 79 (TO-39)

Metal Package

$R_{\theta JA}$ = 185° C/W(Typ)



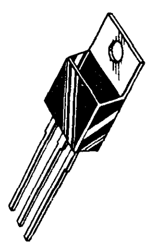


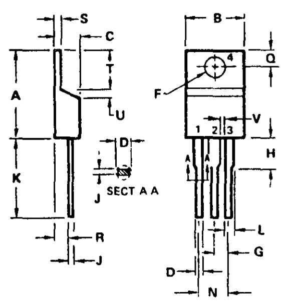
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9 02	9 30	0 355	0 366
B	8 00	8 51	0 315	0 335
C	4 19	4 57	0 165	0 180
D	0 43	0 53	0 017	0 021
E	0 43	0 89	0 017	0 035
F	0 41	0 48	0 016	0 019
G	4 83	5 33	0 190	0 210
H	0 71	0 86	0 028	0 034
J	0 74	1 02	0 029	0 040
K	12 70	–	0 500	–
M	45° NOM		45° NOM	
N	2 54 TYP		0 100 TYP	
Q	90° NOM		90° NOM	

CASE 221A (TO-220 Type)

Plastic Power

$R_{\theta JA}$ = 65° C/W (Typ)



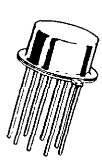


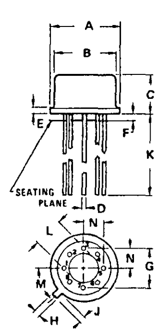
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15 11	15 75	0 595	0 620
B	9 65	10.29	0 380	0 405
C	4 06	4.82	0 160	0 190
D	0 64	0.89	0 025	0 035
F	3 61	3 73	0 142	0 147
G	2 41	2 67	0 095	0 105
H	2 79	3.30	0 110	0 130
J	0 36	0 56	0 014	0 022
K	12 70	14.27	0 500	0 562
L	1 14	1 27	0 045	0 050
N	4 83	5 33	0 190	0 210
Q	2 54	3 04	0 100	0 120
R	2 04	2 79	0 080	0 110
S	1 14	1.39	0 045	0 055
T	5 97	6.48	0 235	0 255
U	0 76	1.27	0 030	0 050
V	1 14	-	0 045	-

CASE 601

Metal Package

$R_{\theta JA}$ = 160° C/W(Typ)



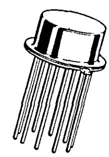


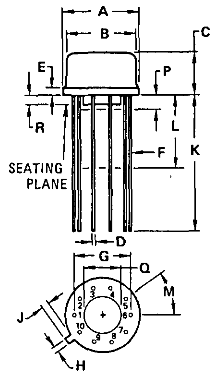
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8 51	9 40	0 335	0 370
B	7 75	8 51	0 305	0 335
C	4 19	4 70	0 165	0 185
D	0 41	0 48	0 016	0 019
E	0 25	1 02	0 010	0 040
F	0 25	1 02	0 010	0 040
G	5 08 BSC		0 200 BSC	
H	0 71	0 86	0 028	0 034
J	0 74	1 14	0 029	0 045
K	12 70	–	0 500	–
L	3 05	4 06	0 120	0 160
M	45° BSC		45° BSC	
N	2 41	2 67	0 095	0 105

CASE 603

Metal Can

$R_{\theta JA}$ = 160° C/W



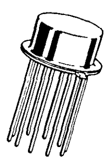


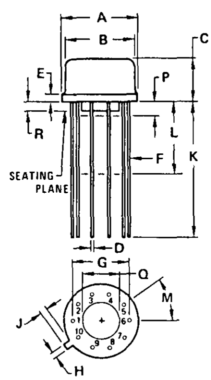
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.407	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	–	0.500	–
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	–	1.27	–	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

Case 603B has tab at pin1.

CASE 603C (TO-100 Type)

$R_{\theta JA}$ = 150° C/W(Typ)



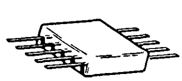


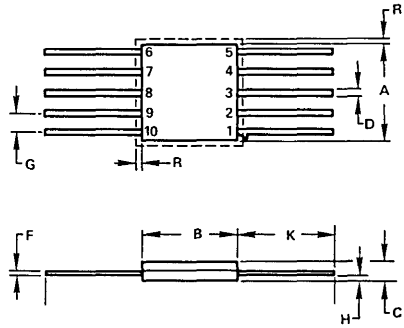
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	6.73	0.165	0.265
D	0.407	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	–	0.500	–
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	–	1.27	–	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

CASE 606 (TO-91)

Ceramic Package

$R_{\theta JA}$ = 165° C/W(Typ)





NOTE
1 LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION (AT BODY)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	7.36	0.240	0.290
B	6.10	6.60	0.240	0.260
C	0.762	1.77	0.030	0.070
D	0.254	0.482	0.010	0.019
F	0.077	0.152	0.003	0.006
G	1.15	1.39	0.045	0.055
H	0.127	0.889	0.005	0.035
K	1.78	–	0.070	–
R	–	0.381	–	0.015

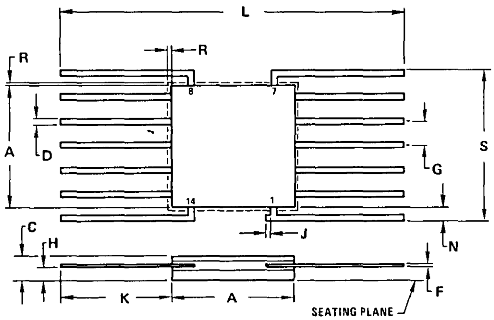
All JEDEC dimensions and notes apply

8

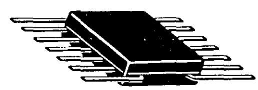
CASE 607 (TO-86 Type)

Ceramic Package

$R_{\theta JA}$ = 165° C/W(Typ)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6 10	6 60	0 240	0 260
C	0 76	1 78	0 030	0 070
D	0 33	0 48	0 013	0 019
F	0 08	0 15	0 003	0 006
G	1 27 BSC		0 050 BSC	
H	0 30	0 89	0 012	0 035
J	–	0 38	–	0 015
K	6 35	9 40	0 250	0 370
L	18 80	–	0 740	–
N	0 25	–	0 010	–
R	–	0 38	–	0 015
S	7 62	8 38	0 300	0 330

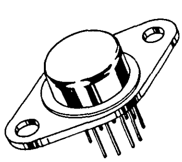


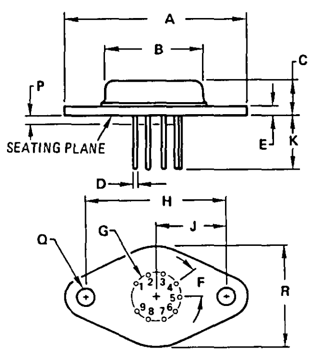
CASE 614 (TO-66 Type)

Metal Package

$R_{\theta JA}$ = 35° C/W(Typ)

$R_{\theta JC}$ = 6° C/W(Typ)



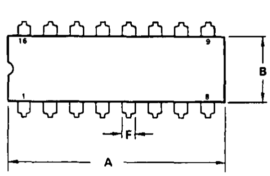


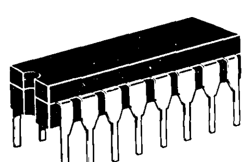
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	31 80	–	1 252
B	11 94	12 70	0 470	0 500
C	6 35	8 64	0 250	0 340
D	0 71	0 81	0 028	0 032
E	1 27	1 90	0 050	0 075
F	36° BSC		36° BSC	
G	8 26 BSC		0 325 BSC	
H	24 33	24 43	0 958	0 962
J	12 17	12 22	0 479	0 481
K	9 14	–	0 360	–
P	1 40 BSC		0 055 BSC	
Q	3 61	3 86	0 142	0 152
R	–	17 78	–	0 700

CASE 620

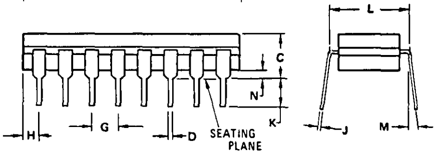
Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19 81	0 750	0 780
B	6 22	6 98	0 245	0 275
C	4 06	5 08	0 160	0 200
D	0 38	0 51	0 015	0 020
F	1 40	1 65	0 055	0 065
G	2 54 BSC		0.100 BSC	
H	0 51	1 14	0 020	0 045
J	0 20	0 31	0 008	0 012
K	3.18	0 30	0 125	0 160
L	7 37	7 87	0 290	0 310
M	–	15°	–	15°
N	0 51	1 02	0 020	0 040



NOTES

1 LEADS WITHIN 0 13 mm (0 005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION'

2 PKG INDEX NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT'

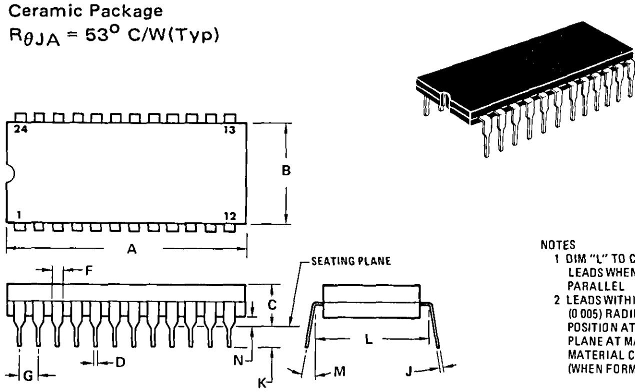
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL'

8

CASE 623

Ceramic Package

$R_{\theta JA}$ = 53° C/W(Typ)



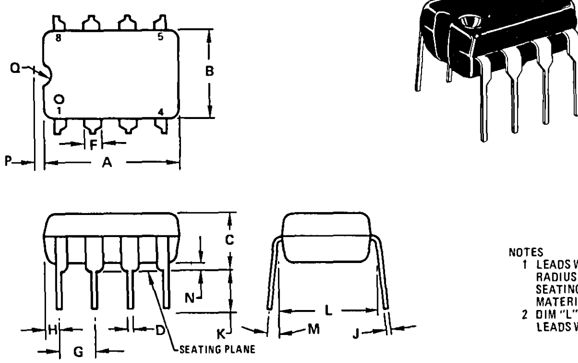
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31 24	32 77	1 230	1 290
B	12 70	15 49	0 500	0 610
C	4 06	5 59	0 160	0 220
D	0 41	0 51	0 016	0 020
F	1 27	1 52	0 050	0 060
G	2 54 BSC		0 100 BSC	
J	0 20	0 30	0 008	0 012
K	2 29	4 06	0 090	0 160
L	15 24 BSC		0 600 BSC	
M	0°	15°	0°	15°
N	0 51	1 27	0 020	0 050

NOTES
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL
2. LEADS WITHIN 0 13 mm (0 005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL)

CASE 626

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)



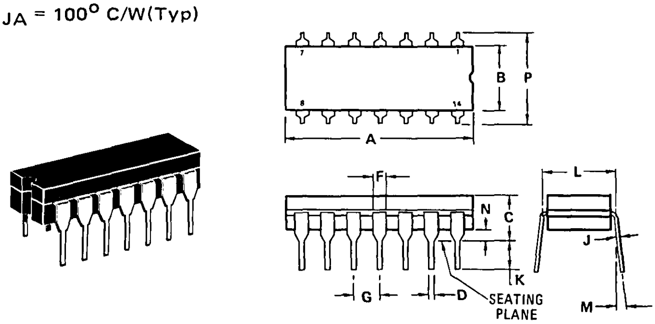
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9 40	10 16	0 370	0 400
B	6 10	6 60	0 240	0 260
C	3 94	4 45	0 155	0 175
D	0 38	0 51	0 015	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	0 76	1 27	0 030	0 050
J	0 20	0 30	0 008	0 012
K	2 92	3 43	0 115	0 135
L	7 62 BSC		0 300 BSC	
M	–	10°	–	10°
N	0 51	0 76	0 020	0 030

NOTES
1. LEADS WITHIN 0 13 mm (0 005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 632 (TO-116)

Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16 8	19.9	0 660	0.785
B	5 59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0 381	0 584	0 015	0.023
F	0 77	1.77	0 030	0.070
G	2 54 BSC		0 100 BSC	
J	0 203	0 381	0 008	0.015
K	2.54	–	0.100	–
L	7 62 BSC		0 300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0 020	0 030
P	–	8 25	–	0.325

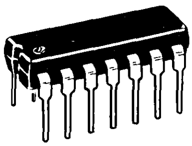
All JEDEC dimensions and notes apply

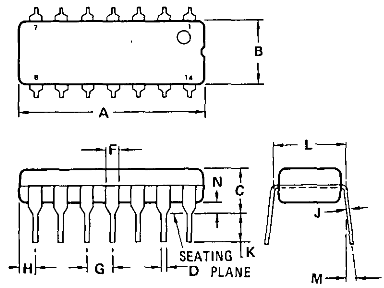
DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 646

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





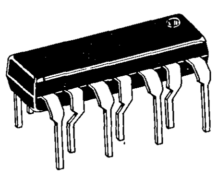
NOTES
1 LEADS WITHIN 0 13 mm (0 005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2 DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

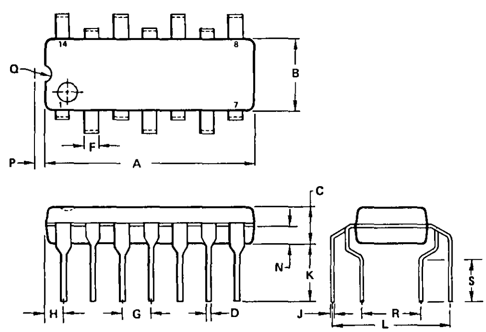
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18 16	19 56	0 715	0 770
B	6 10	6 60	0 240	0 260
C	4 06	5 08	0 160	0 200
D	0 38	0 53	0 015	0 021
F	1 02	1 78	0 040	0 070
G	2 54 BSC		0 100 BSC	
H	1 32	2 41	0 052	0 095
J	0 20	0 38	0 008	0 015
K	2 92	3 43	0 115	0 135
L	7 62 BSC		0 300 BSC	
M	0°	10°	0°	10°
N	0 51	1 02	0 020	0 040

CASE 647

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





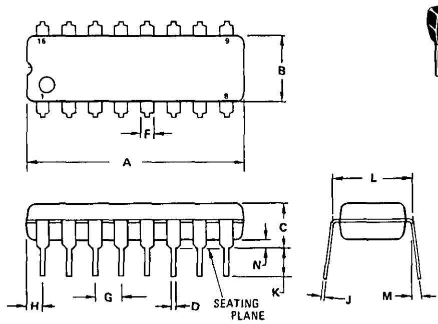
NOTE
1 LEADS WITHIN 0 13 mm (0 005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION

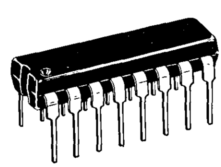
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18 16	18 80	0 715	0 740
B	6 10	6 60	0 240	0 260
C	3 30	3 81	0 130	0 150
D	0 38	0 51	0 015	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 32	1 83	0 052	0 072
J	0 20	0 30	0 008	0 012
K	2 79	4 06	0 110	0 0160
L	9 52	10 92	0 375	0 430
N	1 02	1 52	0 040	0 060
P	0 13	0 38	0 005	0 015
Q	0 51	0 76	0 020	0 030
R	4 70	5 97	0 185	0 235
S	2 54	3 43	0 100	0 135

CASE 648

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





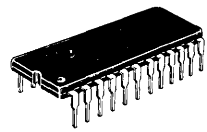
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18 80	21 34	0 740	0 840
B	6 10	6 60	0 240	0 260
C	4 06	5 08	0 160	0 200
D	0 38	0 53	0 015	0 021
F	1.02	1 78	0 040	0 070
G	2 54 BSC		0 100 BSC	
H	0 38	2 41	0 015	0 095
J	0 20	0 38	0 008	0 015
K	2 92	3 43	0 115	0 135
L	7 62 BSC		0 300 BSC	
M	0°	10°	0°	10°
N	0 51	1 02	0 020	0 040

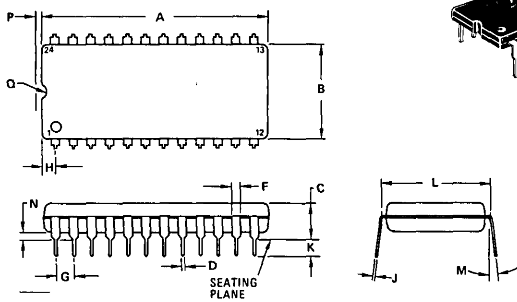
NOTE
1 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 649

Plastic Package

$R_{\theta JA} = 90^{\circ}$ C/W(Typ)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31 50	32 13	1 240	1 265
B	13 21	13 72	0 520	0 540
C	4 70	5 21	0 185	0 205
D	0 38	0 51	0 015	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	2 92	3 43	0 115	0 135
L	14 99	15 49	0 590	0 610
M	–	10°	–	10°
N	0 51	1 02	0 020	0 040
P	0 13	0 38	0 005	0 015
Q	0 51	0 76	0 020	0 030

NOTES

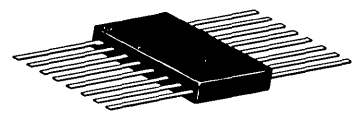
1 LEADS WITHIN 0 13 mm (0 005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION

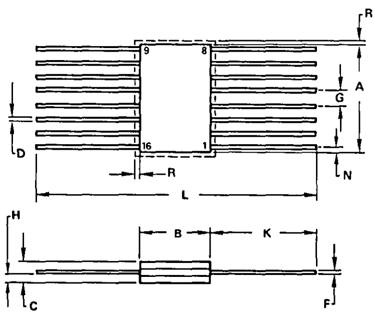
2 DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 650

Ceramic Package

$R_{\theta JA} = 140^{\circ}$ C/W(Typ)





NOTES

1 LEAD NO 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER

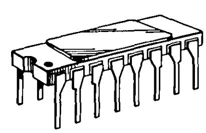
2 LEADS WITHIN 0 13 mm (0 005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION

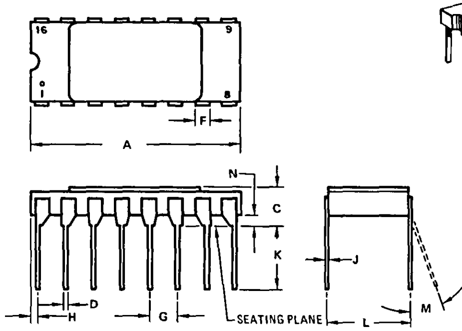
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9 40	10 16	0 370	0 400
B	6 22	6 60	0 245	0 260
C	1 52	2 03	0 060	0 080
D	0 38	0 48	0 015	0 019
F	0 08	0 15	0 003	0 006
G	1 27 BSC		0 050 BSC	
H	0 64	0 89	0 025	0 035
K	6 35	9 40	0 250	0 370
L	18 92	–	0 745	–
N	–	0 51	–	0 020
R	–	0 38	–	0 015

CASE 690

Ceramic Package

$R_{\theta JA} = 100^{\circ}$ C/W(Typ)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20 07	20 57	0 790	0 810
B	7 11	7 62	0 280	0 300
C	2 67	3 94	0 105	0 155
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 30	0 008	0 012
K	3 18	5 08	0 125	0 200
L	7 62 BSC		0 300 BSC	
M	–	10°	–	10°
N	0 38	1 40	0 015	0 055

NOTE

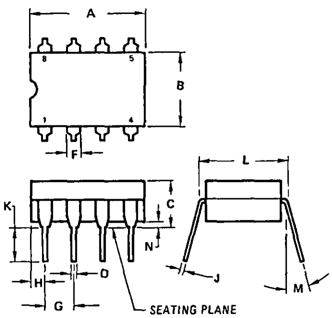
1. LEADS WITHIN 0 13 mm (0 005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION

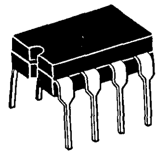
8

CASE 693

Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)





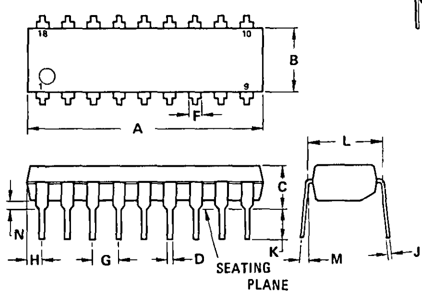
NOTES
1 LEADS WITHIN 0 13 mm (0 005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2 DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

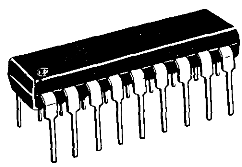
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9 91	10 92	0 390	0 430
B	6 22	6 99	0 245	0 275
C	4 32	5 08	0 170	0 200
D	0 41	0 51	0 016	0 020
F	1 40	1 65	0 055	0 065
G	2 54 BSC		0 100 BSC	
H	1 14	1 65	0 045	0 065
J	0 20	0 30	0 008	0 012
K	3 18	4 06	0 125	0 160
L	7 37	7 87	0 290	0 310
M	–	15°	–	15°
N	0 51	1 02	0 020	0 040

CASE 701

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23 11	23 88	0 910	0 940
B	6 10	6 60	0 240	0 260
C	4 06	4 57	0 160	0 180
D	0 38	0 51	0 015	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 32	1 83	0 052	0 072
J	0 20	0 30	0 008	0 012
K	2 92	3 43	0 115	0 135
L	7 37	7 87	0 290	0 310
M	0°	10°	0°	10°
N	0 51	1 02	0 020	0 040

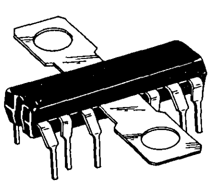
NOTES
1 LEADS WITHIN 0 13 mm (0 005) RADIUM OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G")
2 DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

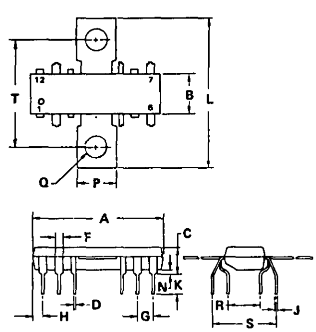
CASE 722

Plastic Package

$R_{\theta JA}$ = 60° C/W(Typ)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20 70	21 34	0 815	0 840
B	6 10	6 60	0 240	0 260
C	4 06	4 57	0 160	0 180
D	0 43	0 56	0 017	0 022
F	1 02	1.52	0 040	0 060
G	2 41	2 67	0 095	0 105
H	1 32	1 83	0 052	0 072
J	0 33	0 46	0 013	0 018
K	3 30	3 94	0 130	0 155
L	25 15	27 94	0 990	1.100
N	0 51	1 02	0 020	0 040
P	6 27	6 53	0 247	0 257
Q	3 48	3 73	0 137	0 147
R	4 83	5 33	0 190	0 210
S	9 91	10 41	0 390	0 410
T	16 26	16 76	0 640	0 660



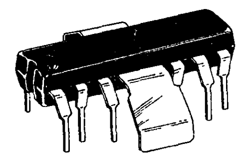


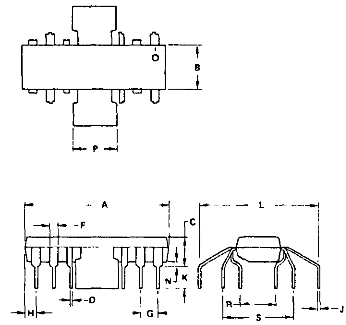
8

CASE 722A

Plastic Package

$R_{\theta JA} = 60^{\circ}$ C/W(Typ)



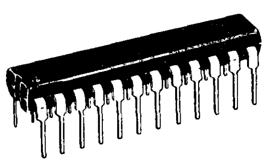


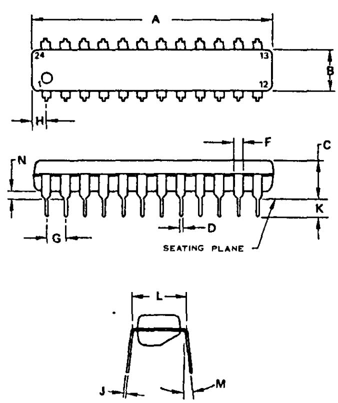
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20 70	21 34	0 815	0 840
B	6.10	6 60	0 240	0 260
C	4 06	4 57	0 160	0 180
D	0 43	0 56	0 017	0 022
F	1 02	1 52	0 040	0 060
G	2 41	2 67	0 095	0 105
H	1 32	1 83	0 052	0 072
J	0 33	0 46	0 013	0 018
K	3 30	3 94	0.130	0 155
L	16 94	17 45	0 667	0 687
N	0 51	1 02	0 020	0 040
P	6 27	6 53	0 247	0 257
R	4 83	5 33	0 190	0.210
S	9 91	10 41	0 390	0 410
T	2 54	3 81	0 100	0 150

CASE 724

Plastic Package

$R_{\theta JA} = 100^{\circ}$ C/W(Typ)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31 24	32 13	1 230	1 265
B	6 35	6 86	0 250	0 270
C	4 06	4 57	0 160	0 180
D	0 38	0 51	0 015	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 60	2 11	0 063	0 083
J	0 18	0 30	0 007	0 012
K	2 92	3 43	0 115	0 135
L	7 37	7 87	0 290	0 310
M	–	10°	–	10°
N	0 51	1 02	0 020	0 040

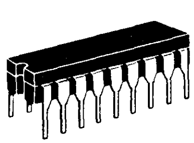
NOTE

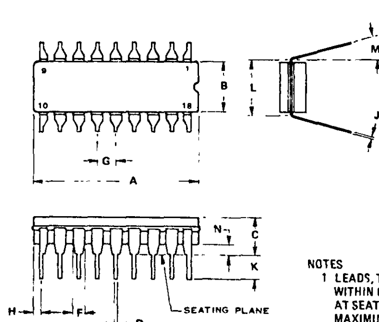
1 LEADS, TRUE POSITIONED WITHIN 0 25 mm (0 010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D)

CASE 726

Ceramic Package

$R_{\theta JA} = 100^{\circ}$ C/W(Typ)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22 35	23 11	0 880	0 910
B	6 63	7 24	0 261	0 285
C	–	5 08	–	0 200
D	0 41	0 51	0 016	0 020
F	1,40	1 65	0 055	0 065
G	2.54 BSC		0 100 BSC	
H	0 76	1 02	0 030	0 040
J	0 13	0 38	0 005	0 015
K	–	4 44	–	0 175
L	7.37	8 00	0 290	0 315
M	0°	15°	0°	15°
N	0 51	0 76	0 020	0 030

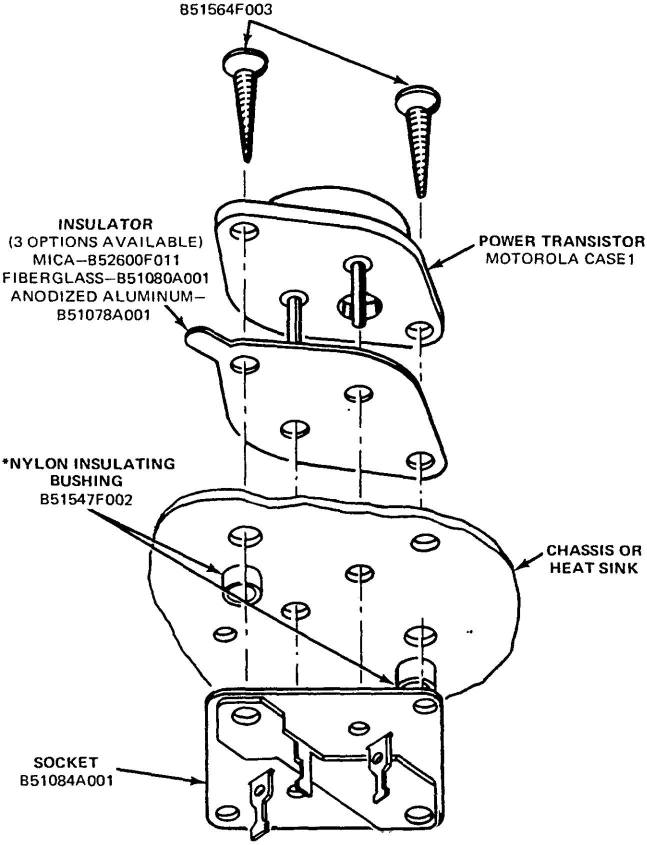
NOTES

1 LEADS, TRUE POSITIONED WITHIN 0.25 mm (0 010) DIA AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION

2 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

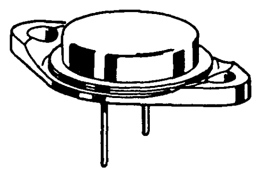
3 DIM "A" & "B" INCLUDES MENISCUS.

MOUNTING HARDWARE TO-3



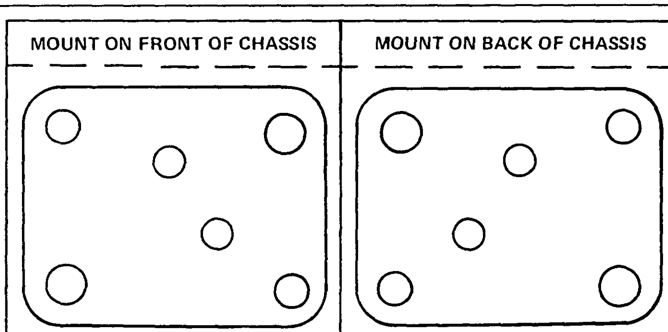
*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

This hardware is applicable to the following packages.



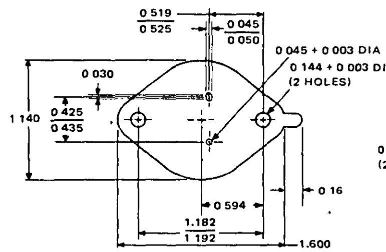
CASE 1 (TO-3)
CASE 3

FRONT TEMPLATE
B51087A001

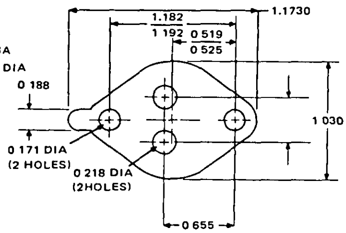


BACK TEMPLATE
B51087A002

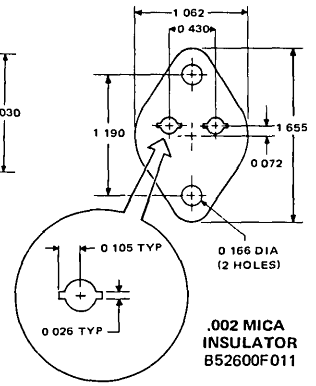
8



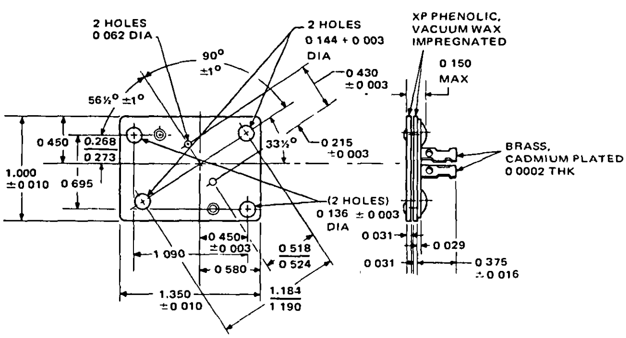
0.003 TEFLON-COATED FIBERGLASS INSULATOR
B51080A001



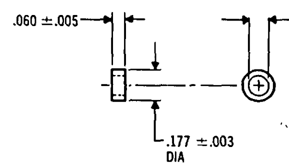
.020 ALUMINUM INSULATOR
B51078A001



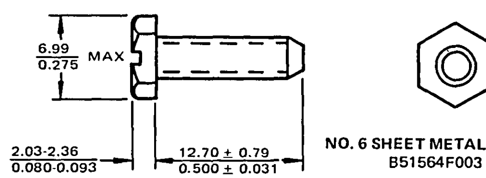
.002 MICA INSULATOR
B52600F011



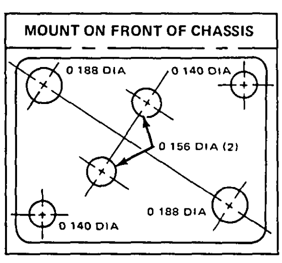
TRANSISTOR SOCKET
B51084A001



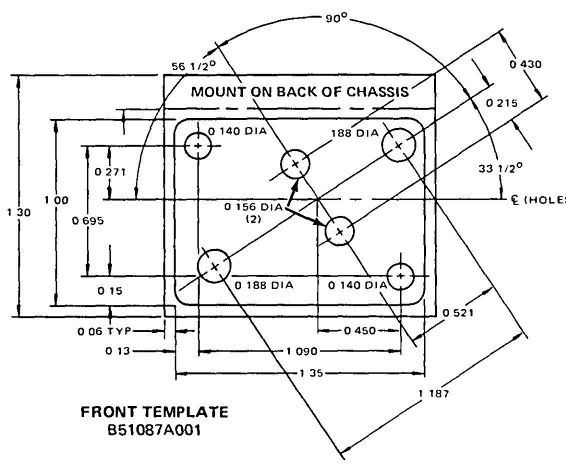
NYLON INSULATING BUSHING
B51547F002



NO. 6 SHEET METAL SCREW
B51564F003



BACK TEMPLATE
B51087A002



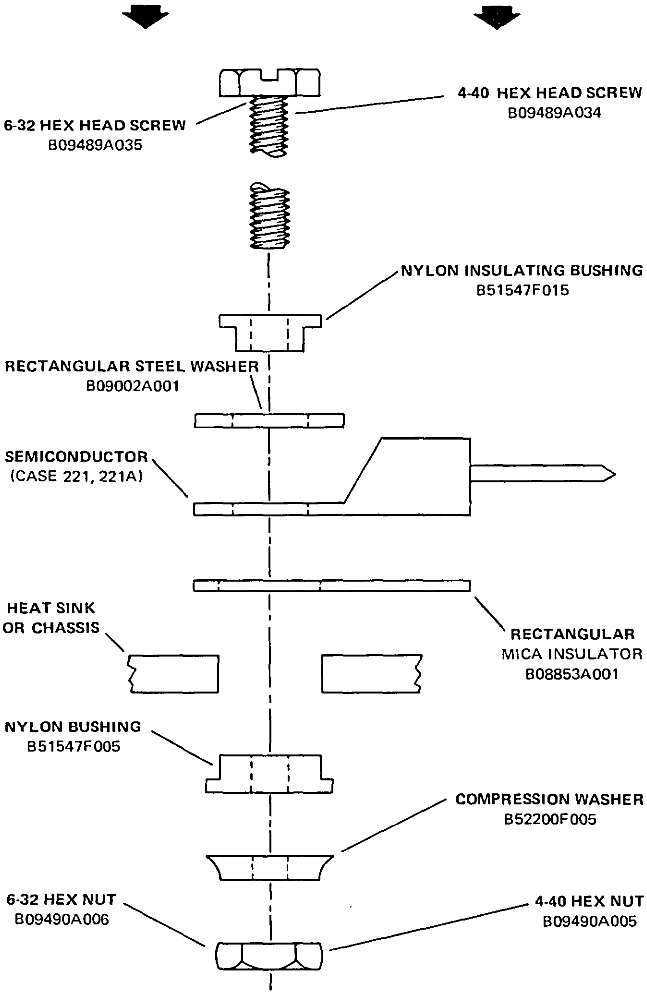
FRONT TEMPLATE
B51087A001

8

MOUNTING HARDWARE TO-220AB

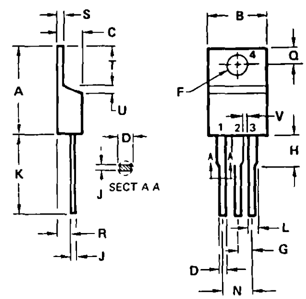
Part numbers in this column for **NON-INSULATED MOUNTING**

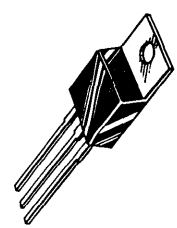
Part numbers in this column for **INSULATED MOUNTING**



TORQUE REQUIREMENTS

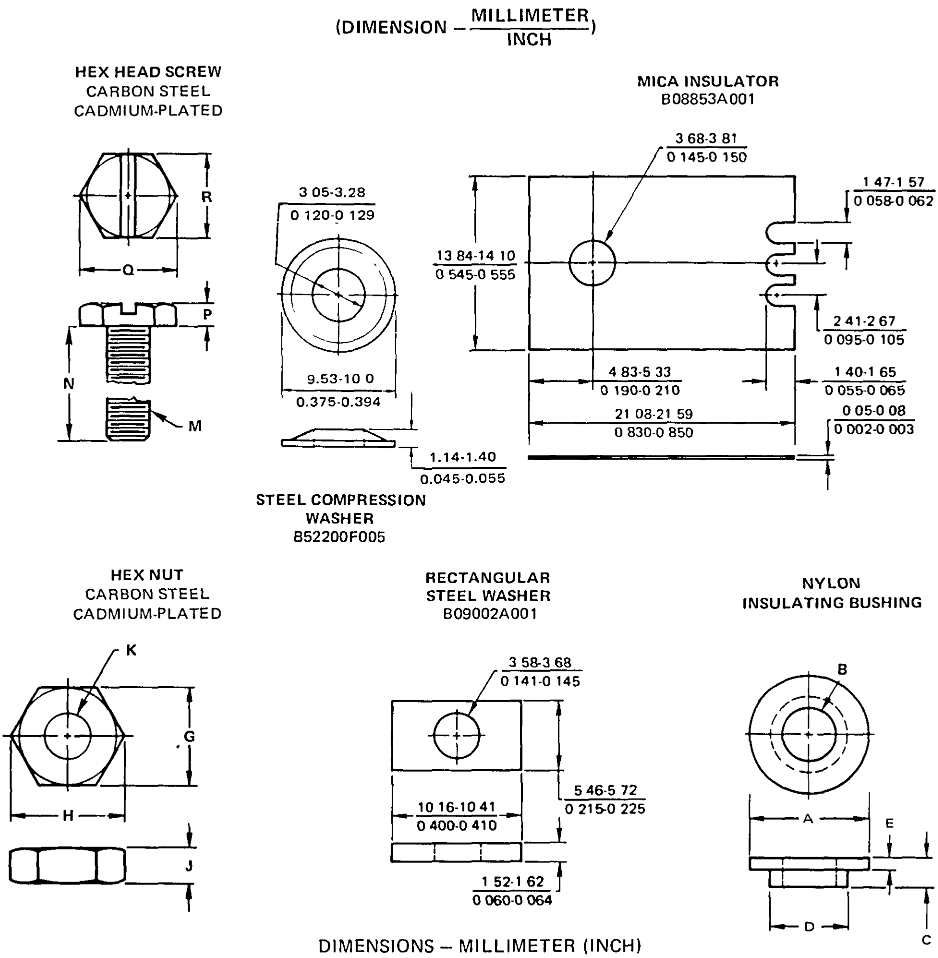
INSULATED 0.68 N-M (6 IN-LBS) MAX
NON-INSULATED 0.9 N-M (8 IN-LBS) MAX





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15 11	15 75	0 595	0 620
B	9 65	10 29	0 380	0 405
C	4 06	4 82	0 160	0 190
D	0 64	0 89	0 025	0 035
F	3 61	3 73	0 142	0 147
G	2 41	2 67	0 095	0 105
H	2 79	3 30	0 110	0 130
J	0 36	0 56	0 014	0 022
K	12 70	14 27	0 500	0 562
L	1 14	1 27	0 045	0 050
N	4 83	5 33	0 190	0 210
Q	2 54	3 04	0 100	0 120
R	2 04	2 79	0 080	0 110
S	1 14	1 39	0 045	0 055
T	5 97	6 48	0 235	0 255
U	0 76	1 27	0 030	0 050
V	1 14		0 045	-

CASE 221A
TO-220 Type



DIMENSIONS – MILLIMETER (INCH)

NYLON BUSHING

PART NO.	DIM A	DIM B	DIM C	DIM D	DIM E
B51547F005	9 40-9 65 (0.370-0 380)	3 84-4 09 (0.151-0.161)	2.16-2.41 (0.085-0 095	6.10 6.35 (0.240-0.250)	1.02-1.27 (0 040-0.050)
B51547F015	5.59-6.10 (0.220-0 240)	3.05-3.15 (0 120-0.124)	1.57-1 68 (0 062-0.066)	3.56-3 66 (0.140-0 144)	0.51-0 64 (0 020.0 025)

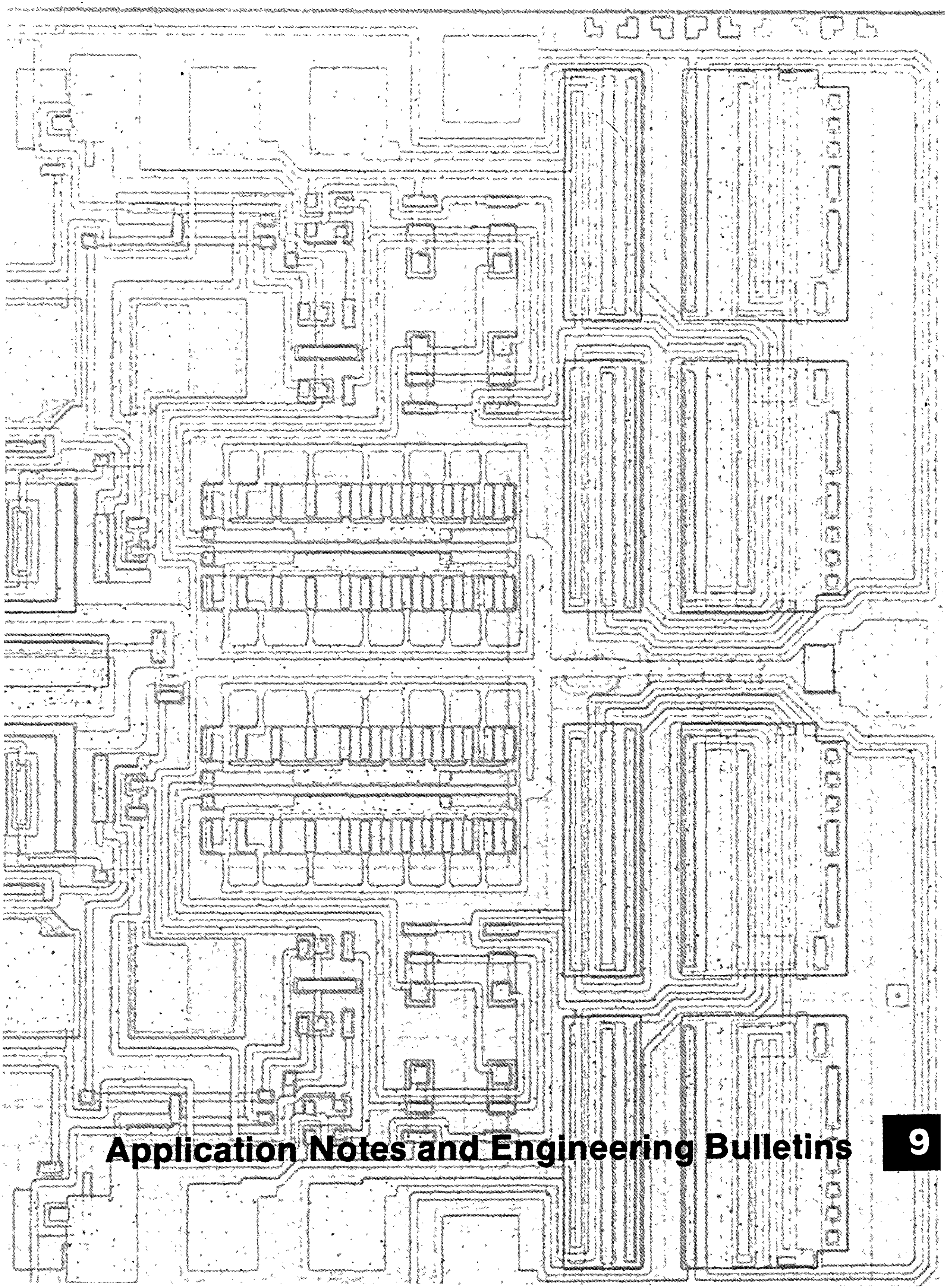
HEX NUT

TYPE	PART NO	DIM G	DIM H	DIM J	DIM K
4-40	B09490A005	6 12-6 35 (0 241-0 250)	6 98-7 34 (0 275-0 289)	2 21-2 49 (0 087-0 098)	2 84 NOM (0 112 NOM)
6-32	B09490A006	7 67-7 92 (0 302-0 312)	8 74-9 17 (0 344 0 361)	2 59-2 90 (0 102-0 114)	3 50 NOM (0 138 NOM)

HEX HEAD SCREW

TYPE	PART NO.	DIM M	DIM P	DIM Q	DIM R
4-40	B09484A034	0 112-40	1 24-1 52 (0 049-0 060)	5 13 MIN (0 202 MIN)	4 60-4 75 (0 181-0 187)
6-32	B09484A035	0 138-32	2 03 2 36 (0 080-0 093)	6 91 MIN (0 272 MIN)	6 20-6 35 (0 244-0 250)

8



Application Notes and Engineering Bulletins

9

APPLICATION NOTE ABSTRACTS

The application notes listed in this section have been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the AN number or numbers and send your request on your company letterhead to: Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

AN-245A An Integrated Core Memory Sense Amplifier

This application note discusses core memories and related design considerations for a sense amplifier. Performance and environmental specifications for the amplifier design are carefully established so that the circuit will work with any computer using core memories. The final circuit design is then analyzed and measured performance is discussed. The amplifier features a small uncertainty region (6 mV max), adjustable voltage gain, and fast cycle time (0.5 μs).

AN-273A More Value out of Integrated Operational Amplifier Data Sheets

The operational amplifier is rapidly becoming a basic building block in present day solid state electronic systems. The purpose of this application note is to provide a better understanding of the open loop characteristics of the amplifier and their significance to overall circuit operation. Also, each parameter is defined and reviewed with respect to closed loop considerations. The importance of loop gain stability and bandwidth is discussed at length. Input offset circuits are also reviewed with respect to closed loop operation.

AN-290B Mounting Procedure for, and Thermal Aspects of, Thermopad Plastic Power Devices

Many Motorola power devices are now available in the Plastic Thermopad packages. Three package types are presently available. This application note provides information concerning the handling and mounting of these packages, as well as information on some thermal aspects.

AN-401 The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier

This application note discusses four different applications for the MC1554, along with a circuit description including DC characteristics, frequency response, and distortion. A section of the note is also devoted to package power dissipation calculations including the use of the curves on the power amplifier data sheet.

AN-404 A Wideband Monolithic Video Amplifier

This note describes the basic principles of AC and DC operation of the MC1552G and MC1553G, characteristics obtained as a function of the device operating modes, and typical circuit applications.

AN-411 The MC1535 Monolithic Dual Op Amp

This note discusses two dual operational amplifier applications and an input compensation scheme for fast slew rate for the MC1535. A complete AC and DC circuit analysis is presented in addition to many of the pertinent electrical characteristics and how they might affect the system performance.

AN-421 Semiconductor Noise Figure Considerations

A summary of many of the important noise figure considerations related with the design of low noise amplifiers is presented. The basic fundamentals involving noise, noise figure, and noise figure-frequency characteristics are then discussed with the emphasis on characteristics common to all semiconductors. A brief introduction is made to various methods of data sheet presentation of noise figure and a summary is given for the various methods of measurement. A discussion of low noise circuit design, utilizing many of the previously discussed considerations, is included.

AN-471 Analog-to-Digital Conversion Techniques

The subject of analog-to-digital conversion and many of the techniques that can be used to accomplish it are discussed. The paper is written in general terms from a system point of view and is intended to assist the reader in determining which conversion technique is best suited for a given application.

AN-489 Analysis and Basic Operation of the MC1595

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance that is characteristic of the device. A few basic applications are given to assist the designer in system design.

AN-491 Gated Video Amplifier Applications Using The MC1545

This application note reviews the basic operation of the MC1545 and discusses some of the more popular applications for the MC1545. Included are several modulator types, temperature compensation of the active gate, AGC, gated oscillators, FSK systems, and single supply operation.

AN-513 A High Gain Integrated Circuit RF-IF Amplifier with Wide Range AGC

This note describes the operation and application of the MC1590G, a monolithic RF-IF amplifier. Included are several applications for IF amplifiers, a mixer, video amplifiers, single and two-stage RF amplifiers.

AN-522 The MC1556 Operational Amplifier and its Applications

This application note discusses the MC1556, a second generation, internally compensated monolithic operational amplifier. Particular emphasis is placed on its distinct advantages over the early 709-type amplifier and the more recent 741-type amplifier.

Along with a description of its operation this note presents a discussion on various applications of the MC1556, highlighting its capabilities, and points out its characteristics so the reader may make effective use of the device.

AN-531 MC1596 Balanced Modulator

The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators for AM, SSB, and suppressed carrier AM; demodulators for the previously mentioned modulation forms; frequency doublers and HF/VHF double balanced mixers.

AN-533 Semiconductors for Plated-Wire Memories

An introduction to the operation and electrical characteristics of plated-wire memories is provided in conjunction with the applications of semiconductors that interface with the plated-wire memories.

Devices discussed include drivers, sense amplifiers, and decoders. Memory organization and memory-related semiconductor applications are also mentioned.

AN-543A Integrated Circuit IF Amplifiers for AM/FM and FM Radios

This application note discusses the design and performance of four IF amplifiers using integrated circuits. The IF amplifiers discussed include a high performance circuit, a circuit utilizing a quadrature detector, a composite AM/FM circuit, and an economy model for use with an external discriminator.

AN-545 Television Video IF Amplifier Using Integrated Circuits

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, MC1353 and the MC1330.

AN-547 A High-Speed Dual Differential Comparator, The MC1514

This application note discusses a few of the many uses for the MC1514 dual comparator. Many applications such as sense amplifiers, multibvibrators, and peak level detectors are presented.

AN-553 A New Generation of Integrated Avionic Synthesizers

The need to generate signals of a multitude of different frequencies for avionic systems has resulted in complex solutions in the past. With the introduction of certain standard product integrated circuits, frequency synthesis using digital phase locked loop techniques presents a more practical solution. Several different types of servo phase locked loop systems are discussed and a practical design example is given. Results of design examples are presented along with possible applications.

AN-557 Analog-to-Digital Cyclic Converter

The A/D cyclic converter discussed in this note provides medium speed (1-5μs/ bit) and medium accuracy (7 or 8 bits) operation. A Cyclic converter uses the successive approximation technique in which an unknown analog input voltage is successively compared to a reference voltage to determine each bit of the digital output.

The cyclic converter offers continuous operation, automatic generation of the digital output in Gray-code form, and a building block structure. This structure uses a separate but identical circuit for each resolution bit. The cyclic converter finds use primarily in control and process applications.

AN-559 Simple Ramp A/D Converter

A simple single ramp A/D converter which incorporates a calibration cycle to insure an accuracy of 12 bits is discussed. The circuit uses standard ICs and requires only one precision part—the reference voltage used in the calibration. This converter is useful in a number of instrumentation and measurement applications.

AN-564 An ADF Frequency Synthesizer Utilizing Phase-Locked Loop Integrated Circuits

This application note describes an IC phase locked-loop frequency synthesizer suitable for the local oscillator function in aircraft Automatic Direction Finder (ADF) equipment.

AN-587 Analysis and Design of the Op Amp Current Source

A voltage controlled current source utilizing an operational amplifier is discussed. Expressions for the transfer function and output impedances are developed using both the ideal and non-ideal op amp models. A section on analysis of the effects of op amp parameters and temperature variations on circuit performance is presented.

AN-590 Servo Motor Drive Amplifiers

The design of transformerless, AC servo amplifiers using power darlington transistors and IC op amps are discussed. Two types of power amplifiers are illustrated, one using single +28 Volt power supply, the second using high voltage transistors in complementary configuration for operating directly off the line.

Four different op amp preamplifiers and 90° phase shifters are also described.

AN-599 Mounting Techniques for Metal Packaged Power Semiconductors

For cooler, more reliable operation, proper mounting procedures must be followed if the interface thermal resistance between the semiconductor package and heat sink is to be minimized. Discussed are aspects of preparing the mounting surface, using thermal compounds, and fastening techniques. Typical interface thermal resistance is given for a number of packages.

AN-702 High Speed Digital-To-Analog and Analog-To-Digital Techniques

A brief overview of some of the more popular techniques for accomplishing D/A and A/D techniques. In particular those techniques which lead themselves to high speed conversion.

AN-703 Designing Digitally-Controlled Power Supplies

This application note shows two design approaches; a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in an application.

AN-708A Line Driver and Receiver Considerations

This report discusses many line driver and receiver design considerations such as system description, definition of terms, important parameter measurements, design procedures and application examples. An extensive line of devices is available from Motorola to provide the designer with the tools to implement the data transmission requirements necessary for almost every type of transmission system.

AN-710 Communication System Transmission Losses

This report shows the derivation of the equations used to calculate the insertion loss associated with various component parts of a communications channel. The combinations of components form a system whose overall loss may not be equal to the sum of the losses of the various parts.

AN-711 The Recovery of Recorded Digital Information in Drum, Disk and Tape Systems

The use of magnetic recording techniques has long been an important means of sorting digital information, as evidenced by the wide variety of equipment currently in use. Representative systems utilize drums, disks and tape as the recording medium.

All three techniques share the common problem of recovering the recorded digital information. The analog signal obtained by passing the recording medium by a magnetic sensor (Read Head) must be converted to a suitable digital format.

This application note reviews the general problem and discusses a number of specific circuit approaches.

AN-713 Binary D/A Converters can Provide BCD-Coded Conversion

This note describes the application and use of integrated circuit D/A converters for use in providing a BCD-coded conversion. The technique is illustrated using a 2-1/2 digit digital voltmeter.

AN-714 A Personalized Heart-Rate Monitor with Ditigal Readout

Using the micropower operational amplifier MC1776 and CMOS digital integrated circuits, entirely self-contained portable electro-medical monitoring equipment can be built. This note details the construction of a heart-rate monitor giving a digital indication, beat-by-beat.

AN-716 Successive Approximation A/D Conversion

Recent advances in integrated circuit design and technology have resulted in reduced cost of high performance successive approximation analog to digital converters. This note describes and illustrates two examples of how modern IC components have changed this well known technique.

AN-717 Battery Powered 5-MHz Frequency Counter

This application note describes a battery-powered 5-MHz frequency counter using the McMOS logic family for low-power operation. The basic counter is optimized, at a 12-volt supply for maximum performance with a linear input-signal conditioner. Several options are discussed which optimize the basic counter for minimum power dissipation. These options include a CMOS input signal-conditioner and multiplexed LED displays.

AN-719 A New Approach to Switching Regulators

This article describes a 24-Volt, 3-Ampere switching mode supply. It operates at 20 kHz from a 120 Vac line with an overall efficiency of 70%. New techniques are used to shape the load line. The control portion uses a quad comparator and an opto coupler and features short circuit protection.

AN-720 Interfacing with MECL 10,000

This article describes some of the MECL circuits used to interface with signals not meeting MECL input or output requirements. The characteristics of these circuits such as; input impedance, output drive, gain and bandwidth allow the system designer to use these parts to optimize his system. MECL interface circuits overcome a problem area of many system designs, which is the efficient coupling of non-compatible signals.

AN-732A A Non-Volatile Microprocessor Memory Using 4K N-Channel MOS RAMs

NMOS semiconductor technology has made inroads into high density/high performance circuit design. The one-chip microprocessor, Random Access Memories, and Read Only Memories, are changing system implementation from random logic designs to software and firmware programmable microcomputing systems. Such systems frequently require relatively large amounts of memory.

This paper describes the design of an 8192-byte non-volatile Random Access Memory system using the MCM6605A 4Kx1 RAM. The syste is designed to work with the Motorola MC6800, an 8-bit microprocessor.

AN-737A Switched Mode Power Supplies—Highlighting A 5-V, 40-A Inverter Design

This application note identifies the features of various regulator circuits that are in use today in AC to DC power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators because they fill the present need for energy and space savings.

A complete 5-V, 40-A line operated inverter supply is described in detail including design procedures for the magnetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an optoelectronic coupler. It operates with a full load efficiency of 80% at a frequency of 20 kHz.

AN-739 A Synthetic Spectrum Tuning System for TV

A tuning system is described which uses a complete spectrum of TV channel markers to achieve precise tuning to any channel.

AN-741 Interface Considerations for Numeric Display Systems

This application note describes several methods of multiplexing multi-digit, seven-segment displays. The logic devices illustrated are primarily CMOS with two examples describing TTL. The displays discussed are liquid crystal, LED, gas discharge, incandescent and fluorescent. How to interface between the logic and these displays, and what the interface considerations are, are described in detail.

AN-744 A Phase-Locked Loop Tuning System for Television

This note describes a frequency domain tuning system which utilizes direct digital countdown of the varactor tuner's local oscillator to obtain the proper local oscillator frequency for the channel number selected. The system features direct-channel access with equal ease of tuning and an exact channel readout for all VHF and UHF channels.

AN-746 A 3½ Digit DVM Using an Integrated Circuit Dual Ramp System

This application note describes the design of a 3½-digit DVM (digital voltmeter) using the MC1405 and the MC14435 dual ramp A/D system. The performance criteria is that of a lab quality DVM with both 3½-digit resolution and accuracy while still retaining a low cost and low parts count instrument. Features of the DVM include circuitry for a high impedance input, autopolarity and overrange indication.

AN-751 A Disassociated Intercarrier Television Video IF Amplifier

This application note discusses a unique video IF system, incorporating the MC1331, low-level multiplier detector. Problem areas in IF design are discussed and the specific solutions are shown.

AN-752 An 80-Watt Switching Regulator for CATV and Industrial Applications

This application note describes a 24-Volt, 3-Ampere switching, regulated power supply that operates above 18 kHz from a 40-to 60-Volt, 60-Hz square wave source (CATV power line from a ferroresonant transformer) or a dc standby source with input output isolation. The control circuit consists of a dual operational amplifier and a linear integrated circuit timer which are used to vary the on time of a new high-speed power transistor. The circuit provides good efficiency, good regulation, low output ripple and incorporates input and output voltage over shutdown protection.

AN-757 Analog-to-Digital Conversion Techniques with the MC6800 Microprocessor System

This application note describes several analog-to-digital conversion systems implemented with the M6800 microprocessor and external linear and digital IC's. Systems consisting of an 8- and 10-bit successive approximation approach, as well as dual ramp techniques of 3½-and 4½digit BCD and 12-bit binary, are shown with flow diagrams, source programs and hardware schematics. System tradeoffs of the various schemes and programs for binary-to-BCD and BCD-to-7 segment code are discussed.

AN-760 Application of The MC3416 Crosspoint Switch

The operation and application of the MC3416 4 x 4 balanced crosspoint switch is described in detail. Special emphasis is given to balanced switching systems like those in space division PABX. Discussion of the total system design using the MC3416 is also included.

AN-763 The MC1323—A Fully Programmable Demodulator

The MC1323 is a monolithic integrated circuit demodulator specifically designed for decoding the NTSC color television signal, even when non-standard receiver display tube phosphor primaries are used. The unique design allows independent adjustment of demodulator conversion gains and demodulation axes. This note describes the circuit operation of the MC1323 and several applications including low cost driving of unitized gun picture tubes and obtaining R-G-B demodulated outputs.

AN-765 An Approach To A Low-Noise TV IF System

This note describes a technique of measurement of the IF contribution and ways of minimization of the IF noise. An IF design, following these procedures, is described to meet the desired noise performance.

AN-767 A Line Operated, Regulated 5V/50A Switching Power Supply

This application note describes a regulated 220 V ac to 5 Vdc converter using high voltage switching transistors and Schottky barrier rectifiers. The control functions are all performed by integrated circuits.

AN-775 M6800 Systems Utilizing the MC6875 Clock Generator/Driver

This application note describes the use of the MC6875 clock generator/driver in M6800 based systems. Design examples will demonstrate the capabilities of the driver in systems using slow and/or dynamic memories. Multiprocessing and DMA methods are also covered.

AN-781 Revised Data-Interface Standards

Revised data-interface standards permit faster data rates and longer cables. New chips, and RS232 adapters, simplify their use.

AN-787 An M6800 Clock System That Handles DMA and Memory Refresh Cycle Stealing

Dynamic memory and three-state cycle stealing for Direct Memory Access transfers require a clock generator and priority logic to maintain proper refresh times of the dynamic MPU and dynamic memory. The design presented here demonstrates use of the MC6875 clock generator with an MC6800 MPU.

ENGINEERING BULLETIN ABSTRACTS

EB-20 Multiplier/Op Amp Circuit Detects True RMS
Two op amps and two multipliers are used in the circuit described by EB-20 to obtain the true rms of an input voltage ranging from 2 to 10 Vpk.

EB-21 DAC Key To Inexpensive 2⅔ Digit Voltmeter.
EB-21 presents an idea for the core of an economical 2⅔ digit voltmeter. Built around Motorola's MC1408 8-bit D/A converter, the meter can measure to 2.55 V in 10 mV steps.

EB-24A Input Buffer Circuits For The MC1505 Dual Ramp A-To-D Converter Subsystem
Several bipolar op amp buffers of medium-high impedance are described in this bulletin. It also discusses FET input op amp buffers providing high impedance and temperature drift under 1 mV over the 0°C to 50°C range.

EB-50 Build This Simple, Battery-Powered 3½ Digit DVM From Standard Parts
EB-50 describes a simple, battery-powered 3½ digit DVM capable of measuring up to 20 volts that can be built from readily obtained standard parts. Sufficient information is provided to construct the circuit including schematic, PC board layout, parts list and calibration instructions.

EB-51 Successive Approximation BCD A/D Converter
A successive approximation A/D converter in which a digital-to-analog converter in a feedback loop produces a BCD digital output from an analog input is described in EB-51.

EB-52 Control Your Switching Regulator With The MC3380 Astable Multivibrator
Engineering Bulletin EB-52 describes the operation and characteristics of the MC3380 astable multivibrator and details the design of a 200 volt switching regulator circuit for gas discharge displays using this device as the control element.

EB-57 An Economical FM Transmitter Voice Processor from a Single IC
An MC3401 Quad OP-Amp is used as a Microphone/Modulation interface in an FM transmitter.

EB-58 Analog Data Acquisition Network for Digital Processing Using the MC1405-MC14435 A/D System
An MC1405-MC14435 combination is used to form a dual-slope A/D converter for analog data acquisition.

EB-66 A Symmetry Correcting Circuit for Use with the MC3420
EB-66 shows a method of implementing an external symmetry-correction circuit with the MC3420 Switchmode Regulator Control IC to insure balanced operation of the power transformer in push-pull inverter configurations.

EB-78 NEW ICs In Switching Supplies
This bulletin describes a regulated 220 Vac to 5 Vdc converter design incorporating the MC3420 and MC3423 for the control and ancillary functions.

EB-85 Full-Bridge Switching Power Supplies
This bulletin provides selection information on devices for a full-bridge configuration supply in the 500-1000 watt power range.

EB-86 Half-Bridge Switching Power Supplies
This bulletin provides selection information on devices for a half-bridge configuration supply in the 100-500 watt power range.

EB-87 Flyback Switching Power Supplies
This bulletin provides selection information on devices for a flyback configuration supply in the 100-250 watt power range.

EB-88 Push-Pull Switching Power Supplies
This bulletin provides selection information on devices for a push-pull configuration supply in the 100-500 watt power range.

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